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Texas Instruments OMAP™ Family of Products

Version I

Technical Reference Manual

PRELIMINARY

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Read This First

NOTE: OMAP™ 4 processors are intended for manufacturers of Smartphones and other mobile devices.

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Register, Field, and Bit Calls

The naming convention applied for a call consists of:

- For a register call: <*Module name*>.<*Register name*>; for example: UART.UASR
- For a bit field call:
  - <*Module name*>.<*Register name*>*[End:Start]* <*Field name*> *field*; for example, UART.UASR[4:0] SPEED bit field
  - <*Field name*> *field* <*Module name*>.<*Register name*>*[End:Start]*; for example, SPEED bit field UART.UASR[4:0]
- For a bit call:
  - <*Module name*>.<*Register name*>*[pos]* <*Bit name*> *bit*; for example, UART.UASR[5] BIT_BY_CHAR bit
  - <*Bit name*> *bit* <*Module name*>.<*Register name*>*[pos]*; for example, BIT_BY_CHAR bit UART.UASR[5]

To help the reader navigate the document, each register call is hyperlinked to its register description in the register manual section. After each register description, a table summarizes all hyperlinked register calls.

To navigate in the PDF documents, see Acrobat Reader Tips.

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Coding Rules

The programming models or code listings follow the rules:

Type	Definition	Example
File	Starts with the module name	PRCM_test1.c MCBSP1_init.h
Variable	Global variables are prefixed by "g_" Pointers are prefixed by "p" Global pointers are prefixed by "g_p"	g_SDMA_LogicalChan pAddrCounter g_pSDMA_LogicalChan
Function	Starts with the module name	PRCM_SetupClocks() ArmIntC_MaskInterrupts()
Typedef	Ends with "_t"	PRCM_Struct_t
Definition	Starts with the module name and is followed by the register name	#define SMS_ERR_TYPE *((volatileUint32*)0x680080F4) #define MCBSP2_RCR1_REG *((volatile Uint32*)0x4807401C)
Enumeration	Starts with the module name	Typedef enum DMA_Mode_Label { INPUT_MODE OUTPUT_MODE } DMA_Mode_t;

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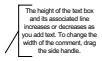
Flow Chart Rules

Flow charts follow the following rules:

Shape	Name	Definition
	Process	Any computational steps or processing function of a program; defined operation(s) causing change in value, form, or location of information
	Decision	A decision or switching-type operation that determines which of a number of alternate paths is followed
	Predefined process or sub-process	One or more named operations or program steps specified in a subroutine or another set of flow charts
	Data or I/O	General I/O function; information available for processing (input) or recording of processed information (output)
	Terminator	Terminal point in a flow chart: start, stop, halt, delay, or interrupt; may show exit from a closed subroutine
	Annotation	Additional descriptive clarification, comment
	On page connector (reference)	Exit to, or entry from, another part of chart in the same page
	Off page connector (reference)	The flow continues on a different page.
	Summing Junction	Logical AND
	Or	Logical OR
	Parallel mode (ISO)	Beginning or end of two or more simultaneous operations
	Flow Line	Lines indicate the sequence of steps and the direction of flow.

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Acrobat includes two methods to search for words in a PDF:

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History

The following table summarizes the OMAP4460 Public TRM versions.

Version	Literature Number	Date	Notes
B	SWPU235	February 2011	See (1)
C	SWPU235	March 2011	See (2)
D	SWPU235	April 2011	See (3)
E	SWPU235	May 2011	See (4)
F	SWPU235	June 2011	See (5)

(1) Public Version of *OMAP4440 Multimedia Device Silicon Revision 1.0 Technical Reference Manual,* version B (SWPU235B) - Initial release to the public domain.

(2) Public Version of *OMAP4460 Multimedia Device Silicon Revision 1.0 Technical Reference Manual,* version C (SWPU235C)
Chapters impacted between version B and version C:
- TI has shifted from OMAP4440 to OMAP4460 naming as OMAP4 adoption expands in new markets worldwide.
- Chapter 1: Introduction
- Chapter 2: Memory Mapping
- Chapter 3: Power, Reset, and Clock Management
- Chapter 8: Imaging Subsystem
- Chapter 10: Display Subsystem
- Chapter 15: Memory Subsystem
- Chapter 16: sDMA
- Chapter 18: Control Module
- Chapter 22: Timers
- Chapter 23: Serial Communication Interfaces - High-Speed USB OTG Controller section
- Chapter 23: Serial Communication Interfaces - Full-Speed USB Host Controller section
- Chapter 27: Initialization

(3) Public Version of *OMAP4460 Multimedia Device Silicon Revision 1.0 Technical Reference Manual,* version D (SWPU235D)
Chapters impacted between version C and version D:
- Chapter 1: Introduction
- Chapter 8: Imaging Subsystem
- Chapter 10: Display Subsystem
- Chapter 15: Memory Subsystem
- Chapter 18: Control Module
- Chapter 23: Serial Communication Interfaces - Multimaster High-Speed I^2C Controller section
- Chapter 23: Serial Communications Interfaces - Multichannel Buffered Serial Port (McBSP) section
- Chapter 23: Serial Communication Interfaces - Multichannel Audio Serial Port section
- Chapter 24: MMC/SD/SDIO

(4) Public Version of *OMAP4460 Multimedia Device Silicon Revision 1.0 Technical Reference Manual,* version E (SWPU235E)
Chapters impacted between version D and version E:
- Chapter 3: Power, Reset, and Clock Management
- Chapter 6: IVA-HD Subsystem
- Chapter 8: Imaging Subsystem
- Chapter 10: Display Subsystem
- Chapter 15: Memory Subsystem
- Chapter 18: Control Module
- Chapter 20: Memory Management Units
- Chapter 23: Serial Communication Interfaces - Multichannel Audio Serial Port section
- Chapter 24: MMC/SD/SDIO
- Chapter 27: Initialization

(5) Public Version of *OMAP4460 Multimedia Device Silicon Revision 1.0 Technical Reference Manual,* version F (SWPU235F)
Chapters impacted between version E and version F:
- Chapter 3: Power, Reset, and Clock Management
- Chapter 4: Dual Cortex-A9 MPU Subsystem
- Chapter 8: Imaging Subsystem
- Chapter 10: Display Subsystem
- Chapter 15: Memory Subsystem
- Chapter 16: sDMA
- Chapter 18: Control Module
- Chapter 23: Serial Communication Interfaces - Multichannel Audio Serial Port section
- Chapter 24: MMC/SD/SDIO
- Chapter 27: Initialization

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Version	Literature Number	Date	Notes
G	SWPU235	July 2011	See (6)
H	SWPU235	August 2011	See (7)
I	SWPU235	September 2011	See (8)

(6) Public Version of *OMAP4460 Multimedia Device Silicon Revision 1.x Technical Reference Manual,* version G (SWPU235G)
Chapters impacted between version F and version G:
- Chapter 1: Introduction
- Chapter 3: Power, Reset, and Clock Management
- Chapter 4: Dual Cortex-A9 MPU Subsystem
- Chapter 10: Display Subsystem
- Chapter 11: 2D/3D Graphics Accelerator
- Chapter 15: Memory Subsystem
- Chapter 18: Control Module
- Chapter 23: Serial Communication Interfaces - Multimaster High-Speed I^2C Controller section
- Chapter 23: Serial Communication Interfaces - UART/IrDA/CIR section
- Chapter 23: Serial Communication Interfaces - Multichannel Serial Port Interface section
- Chapter 23: Serial Communication Interfaces - Multichannel PDM Controller section
- Chapter 23: Serial Communication Interfaces - MIPI-HSI section
- Chapter 26: Keyboard Controller
- Chapter 27: Initialization

(7) Public Version of *OMAP4460 Multimedia Device Silicon Revision 1.x Technical Reference Manual,* version H (SWPU235H)
Chapters impacted between version G and version H:
- Chapter 1: Introduction
- Chapter 2: Memory Mapping
- Chapter 3: Power, Reset, and Clock Management
- Chapter 10: Display Subsystem
- Chapter 15: Memory Subsystem
- Chapter 18: Control Module
- Chapter 23: Serial Communication Interfaces - Multichannel Serial Port Interface section
- Chapter 23: Serial Communication Interfaces - MIPI-HSI section
- Chapter 25: General-Purpose Interface
- Chapter 27: Initialization

(8) Public Version of*OMAP4460 Multimedia Device Silicon Revision 1.x Technical Reference Manual,* version I (SWPU235I).
Chapters impacted between version H and version I:
- Chapter 1: Introduction
- Chapter 3: Power, Reset, and Clock Management
- Chapter 10: Display Subsystem
- Chapter 15: Memory Subsystem
- Chapter 18: Control Module
- Chapter 23: Serial Communication Interface – Multimaster High-Speed I^2C Controller section
- Chapter 23: Serial Communication Interface – Multichannel Buffered Serial Port (McBSP) section
- Chapter 23: Serial Communication Interface – MIPI-HSI section
- Chapter 28: On-Chip Debug Support

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Introduction

This chapter introduces the features, subsystems, and architecture of the OMAP4460 high-performance multimedia device.

Topic **Page**

1.1 Overview **262**
1.2 Environment **263**
1.3 Description **264**
1.4 Package-On-Package Concept **275**
1.5 OMAP4460 Family and Device Identification **276**

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1.1 Overview

The OMAP4460 high-performance multimedia application device is based on enhanced OMAP™ architecture and uses 45-nm technology.

- The architecture is designed to provide best-in-class video, image, and graphics processing for 2.5/3G wireless terminals, high-performance personal digital assistants (PDAs). For that purpose, the device supports the following functions:
  - Streaming video up to full high definition (HD) (1920 × 1080 p, 30 fps)
  - 2-dimensional (2D)/3-dimensional (3D) mobile gaming
  - Video conferencing
  - High-resolution still image (up to 16 Mp)
- The device supports high-level operating systems (OSs) such as:
  - Linux®
  - Palm OS™
  - Symbian OS™
  - Windows™ CE, WinMobile™
- The device is composed of the following subsystems:
  - Cortex™-A9 microprocessor unit (MPU) subsystem, including two ARM® Cortex-A9 cores
  - Digital signal processor (DSP) subsystem
  - Image and video accelerator high-definition (IVA-HD) subsystem
  - Cortex™-M3 MPU subsystem, including two ARM Cortex-M3 microprocessors
  - Display subsystem
  - Audio back-end (ABE) subsystem
  - Imaging subsystem (ISS), consisting of image signal processor (ISP) and still image coprocessor (SIMCOP) block
  - 2D/3D graphic accelerator (SGX) subsystem
  - Emulation (EMU) subsystem
- The device includes state-of-art power-management techniques required for high-performance mobile products.
- Comprehensive power management is integrated into the device.
- The device also integrates:
  - On-chip memory
  - External memory interfaces
  - Memory management
  - Level 3 (L3) and level 4 (L4) interconnects
  - System and connecting peripherals

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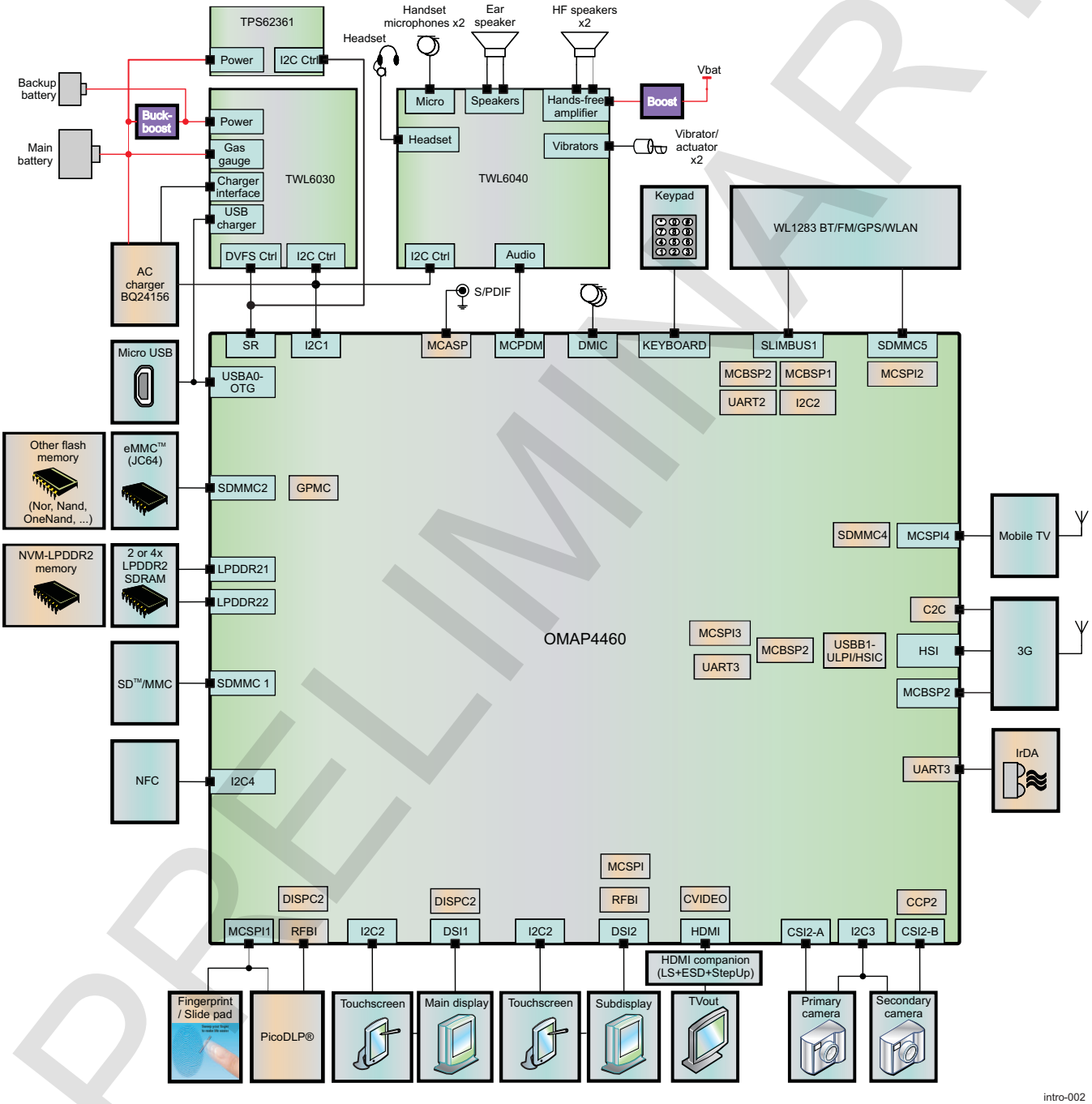
1.2 Environment

This section provides an overview of the OMAP environment. The device is associated with power and audio integrated circuits (ICs). TI provides a global solution with the TWL6030/TWL6040 devices.

Figure 1-1 is an overview of a nonexhaustive environment for the high-tier OMAP4460 device.

Figure 1-1. OMAP4460 High-Tier Environment



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1.3 Description

The device is offered in a 547-ball, 12 × 12 × 0.73-mm, 0.4-mm (bottom) ball pitch package. Some balls are available at the top of the device to allow memory stacking.

Figure 1-2 is the block diagram of the OMAP4460 device.

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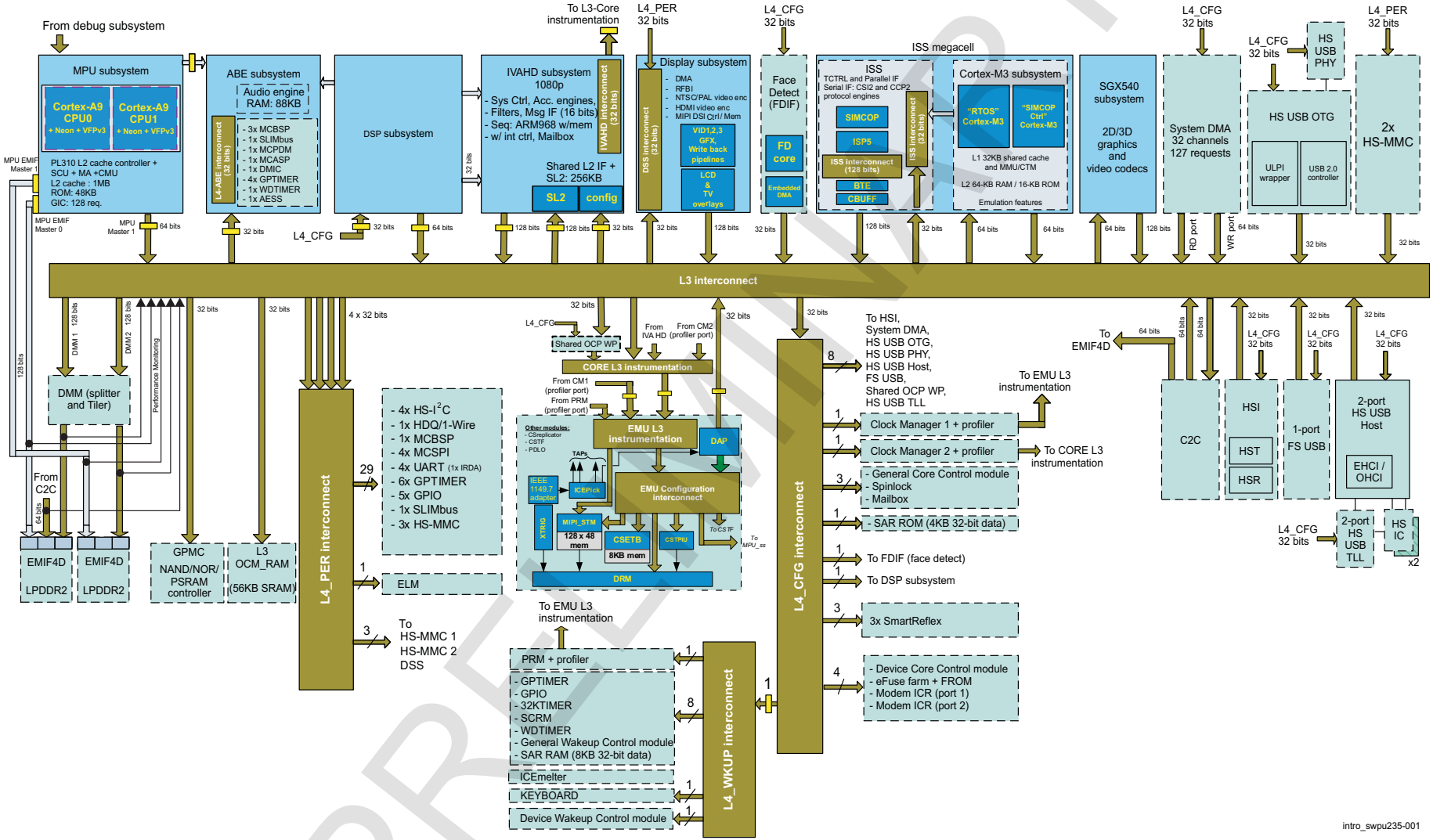
Figure 1-2. OMAP4460 Block Diagram



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1.3.1 Cortex-A9 MPU Subsystem Description

The Cortex-A9 MPU subsystem integrates the following submodules:

- ARM Cortex-A9 MPCore
  - Two ARM Cortex-A9 central processing units (CPUs)
  - ARM Version 7 ISA™: Standard ARM instruction set plus Thumb®-2, Jazelle® RCT and Jazelle DBX Java™ accelerators
  - Neon™ SIMD coprocessor and VFPv3 per CPU
  - Interrupt controller (Cortex-A9 MPU INTC) with up to 128 interrupt requests
  - One general-purpose timer and one watchdog timer per CPU
  - Debug and trace features
  - 32-KB instruction and 32-KB data level 1 (L1) caches per CPU
- Shared 1-MB level 2 (L2) cache
- 48 KB bootable ROM
- Local power, reset, and clock management (PRCM) module
- Emulation features
- Digital phase-locked loop (DPLL)

1.3.2 IVA-HD Subsystem Description

The IVA-HD subsystem is a set of video encoder/decoder hardware accelerators. It supports up to 1080p × 30 fps, slow-motion camcorder, triple play (HD and SD capture and JPEG capture), real-time transcoding of up to 720p, and video conferencing up to 720p.

The IVA-HD subsystem is composed of:

- Improved motion estimation acceleration engine (iME3), which is used in encoding processing
- Improved loop filter acceleration engine (iLF3), which performs deblocking filtering
- Improved sequencer (iCONT1) based on the ARM968E-S™ microcontroller. It includes memory and INTC and is used as a primary sequencer.
- Intraprediction estimation engine (iPE3). It is used in encoding processing.
- Calculation engine (CALC3), which performs transform and quantization calculations
- Motion compensation engine (MC3), which creates an interprediction macroblock with given motion vectors and modes from the reference data
- Entropy coder/decoder (ECD3), which uses Huffman and arithmetic codes during the process of encoding and decoding the stream
- Video DMA processor (iCONT2), which is also based on the ARM968E-S microcontroller and can be used as secondary sequencer
- Video DMA engine (vDMA), which is a DMA engine for data transmission between external memories and shared L2 memory
- Synchronization box (SyncBox) embedded in each hardware accelerator and in both iCONTs
- Mailbox for communication between IVA-HD and external to it processors (DSP, Cortex-A9, and Cortex-M3)
- Shared L2 interface and memory
- Video local interconnect for connection between the submodules of the IVA-HD, and between the IVA-HD and DSP subsystems
- IVA-HD system control module (SYSCTRL), which controls the clocks in the subsystem and PRCM handshaking

The IVA-HD subsystem can process three data formats for internal data: picture or slice, macroblock header, and residual data.

The IVA-HD supports the following formats:

- MPEG-1/-2/-4 such as MPEG-2 MP, ML, and MPEG-4 as SP/ASP

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- Divx 5.02 and above
- Sorenson Spark (decode)
- H.263 P0 (encode and decode) and P3 (decode)
- H.264 Annex G (scalable baseline profile up to 720p)
- H.264 BL/MP/HP
- H.264 Annex H (partial)
- Stereoscopic video
- JPEG (encode/decode)
- VC-1 SP/MP/AP
- AVS-1.0
- RealVideo® 8/9/10 (decode only)
- On2® VP6.2/VP7 (decode only)

1.3.3 Cortex-M3 MPU Subsystem Description

The Cortex-M3 MPU subsystem includes the following components:

- Two Cortex-M3 CPUs: One for SIMCOP control, and the other for RTOS, ISP, and display subsystem control
- ARMv7-M and Thumb-2 instruction set architecture
- Dedicated INTC with up to 64 physical interrupt events
- Two-level memory subsystem hierarchy
  - L1
    - 32-KB shared cache memory
  - L2 ROM + RAM
    - 64-KB RAM
    - 16-KB bootable ROM
- Cortex-M3 system bus directly connected to the ISS interconnect
- MMU for address translation
- Integrated power management
- Emulation feature embedded in the Cortex-M3

1.3.4 Display Subsystem Description

The display subsystem provides the control signals required to interface the OMAP system memory frame buffer (SDRAM) directly to the displays. It supports hardware cursor, independent gamma curve on all interfaces, multiple-buffer, and programmable color phase rotation. The display subsystem allows low-power display refresh and arbitration between normal and low-priority pipelines.

The display subsystem consists of the following sections:

- Display controller: It can read and display the encoded pixel data stored in memory and write the output of one of the overlays or one of the pipelines into the system memory. It supports the following components:
  - Three video pipelines, one graphic pipeline, and one write-back pipeline. The graphic pipeline supports pixel formats such as: ARGB16-4444, RGB16-565, ARGB16-1555, ARGB32-8888, RGBA32-8888, RGB24-888, and BITMAP (1, 2, 4, or 8 bits per pixel). It allows selection of the color-depth expansion.
  - Write-back pipeline: it uses poly-phase filtering for independent horizontal and vertical resampling (upsampling and downsampling). It allows programmable color space conversion of RGB24 into YUV4:2:2-UYVY, YUV4:2:2-YUV2, or YUV4:2:0-NV12, and selection of color-depth reduction from RGB24 to RGB16.
  - Two LCD outputs, each one with dedicated overlay manager, for support of passive matrix color and monochrome displays (up to 8-bit interface) and active matrix color displays (up to 24-bit

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interface). Secondary LCD output is available through parallel CMOS interface for MIPI®-DPI 1.0 support.
  - One TV output with dedicated overlay manager
  - Own direct memory access (DMA) engine
- Remote frame buffer interface (RFBI) module.
  - Support for MIPI-DBI protocol
  - 8-/9-/16-bit parallel interface
  - Programmable pixel modes and output formats
- Two MIPI display serial interfaces (DSIs) with the following main features:
  - Support for MIPI-DSI (four data-lane complex inputs/outputs (I/Os) for DSI1 and two data-lane complex I/Os for DSI2)
  - Support for video mode and command mode
  - Data interleaving support for synchronous and asynchronous streams
  - Bidirectional data link support
- High-definition multimedia interface (HDMI) encoder with the following main features:
  - HDMI 1.3, HDCP 1.2, and DVI 1.0 compliant
    - Including support for the 3D Stereoscopic frame-packing formats of HDMI v1.4 standard (720p, 50Hz, 720p, 60Hz and 1080p, 24Hz)
  - Deep-color mode support (10-bit for up to 1080p and up to 12-bit for 1080i/720p)
  - Support for uncompressed multichannel audio
  - Integrated high-bandwidth digital content protection (HDCP) encryption engine for transmitting protected audio and video content
  - Integrated transition minimized differential signaling (TMDS) and TERC4 encoders for data island support
- NTSC/PAL video encoder with the following main features:
  - Output to on-chip video digital-to-analog converter (VDAC) providing composite analog output signal: NTSC-J, M; PAL-B, D, G, H, I; PAL-M
  - Support for square pixel sampling
  - Programmable horizontal synchronization, vertical timing, and waveforms

NOTE: The NTSC/PAL video encoder and VDAC function are not supported.

1.3.5 ABE Subsystem Description

The ABE subsystem handles audio processing for the application. It manages the audio and voice streams between the Cortex-A9 MPU subsystem and/or DSP, and the physical interfaces.

The ABE subsystem allows:

- Buffering of audio samples
- Mixing audio with voice downstream and/or microphone upstream (sidetone)
- Postprocessing of equalization, 3D effects, bass-boost

The ABE subsystem consists of:

- Audio engine (AE) subsystem, which performs real-time signal processing such as:
  - Muxing and mixing voice and data streams
  - Postprocessing operations such as sampling rate conversion, volume control, 3D effects
  - Execution of whole data transfers in the ABE subsystem using audio traffic controller (ATC)

    The AE subsystem includes an AE and has the following on-chip memories available: 64-KB data memory (DMEM); 6-KB coefficient memory (CMEM); and 18-KB sample memory (SMEM).

    The ATC manages the data movement in the ABE subsystem and is in charge of interrupt

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generation to the DSP and Cortex-A9 MPU subsystems.

- Four general-purpose timers (GPTIMERs) and one watchdog timer (WDTIMER)
- Peripheral interfaces:
  - Three multichannel buffered serial ports (McBSPs) for inter-IC sound (I^2S™) external connectivity
  - One multichannel audio serial port (McASP) supporting Sony/Philips digital interconnect format (S/PDIF) output
  - One MIPI SLIMbus interface to support new generations of MIPI-compliant components
  - One digital microphone (DMIC) for three stereo digital microphones support
  - One multichannel pulse-density modulation (McPDM) interface, which ensures communication with the TWL6040 audio companion chip
- Internal interfaces for connection with the DSP and Cortex-A9 MPU subsystems and other modules in the device
- Dedicated power domain (ABE power domain)

1.3.6 ISS Description

The ISS processes data coming from the image sensor, memory, and IVA-HD subsystem. The ISS is responsible for multimedia applications such as: camera viewfinder; video record with up to 1080 p at 30 fps with digital zoom and still image processing, such as image capture up to 16 Mp with digital zoom and rotation. The ISS supports a pixel throughput of up to 200 Mp/s. It assures good performance with sensors up to 16 Mp and more (higher resolution can be achieved through multiple passes). The ISS can implement third-party algorithms for further flexibility when working with image sensors.

The ISS consists of:

- The ISP, which deals with on-the-fly or memory-to-memory data processing. It allows data collection for autoexposure, autowhite balance, autofocus, resizing, and histogram generation. The ISP consists of:
  - Image pipe interface (IPIPEIF) for synchronization signals (HD, VD) for the ISIF, IPIPE, RSZ, and hardware 3A (H3A) modules, and data transfer from video port, SDRAM, ISIF. Various pixel data manipulation functions.
  - Image pipe (IPIPE) front-end and back-end modules for raw data processing and RGB and YUV data processing, respectively. They support:
    - Sensor data linearization for dynamic range extension
    - Programmable 2D lens shading compensation correction
    - Black-level compensation
    - Gamma correction
    - RGB color correction
    - RGB to YUV4:2:2 color conversion
    - 3D look up table (LUT) for color correction
    - 2D edge enhancement
    - False chroma suppression
  - H3A for autowhite balance, autoexposure, and autofocus
  - Pattern generator (PG) for internal data generation for test purposes. It provides the ability to test some of the ISP submodules without the use of an external image sensor.
  - Two independent resizers, which allow YUV4:2:2 to YUV4:2:0 planar Chroma filtering and downsampling. The resizers support input and output flows with up to 200 Mp/s, and memory-to-memory rescaling in the range ×1/4096 scale down, and ×20 scale up.
  - Image sensor interface (ISIF) can process the incoming data and supports the following main functions:
    - Sensor data linearization
    - Supports VGA read out mode

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    - Color space conversion
    - Digital clamp with horizontal/vertical offset drift compensation
    - Vertical line defect correction
    - Programmable 2D-matrix lens shading correction
    - 10-to-8 bits A-Law compression table inside
  - Buffer logic (BL), which processes and manages the requests to the module and memory subsystem
- Peripheral serial interfaces for connection with sensors and memories:
  - Two PHYs, CSIPHY1 and CSIPHY2, for physical connection to external sensors
  - Peripheral serial interfaces CSI2-A and CSI2-B/CCP2 for image data transfer from sensors to memory or ISP
- Peripheral 16-bit parallel interface, BT656 and SYNC mode
- SIMCOP module for memory-to-memory operation; JPEG encode/decode hardware acceleration; high-ISO filtering; block-based rotation; warping and fusion; and general-purpose imaging acceleration. The SIMCOP includes the following main submodules:
  - Two imaging extension (iMX) modules – programmable image and video processing engines
  - Noise filter 2 (NSF2) – for advanced noise filtering and edge-enhancement
  - Variable-length coder/decoder for JPEG (VLCDJ) module
  - Discrete cosine transform (DCT) module
  - Lens distortion correction (LDC) module
  - Rotation accelerator (ROT) engine
  - Hardware sequencer, which offloads sequencing tasks from the MPU
  - Shared buffers/memories
  - DMA controller
- Timing control module for CAM global reset control, CAM flash strobe, and CAM shutter
- System interfaces and interconnects comprising:
  - Two configuration interfaces
  - One 128-bit master data interface
  - Internal ISS interconnects for image data and configuration
  - On-chip RAM interface
  - Circular buffer (CBUFF) and burst-translation engine (BTE) for efficient communication with external memory (SDRAM/TILER support)

1.3.7 2D/3D Graphics Accelerator Description

The 2D/3D graphics accelerator subsystem is based on POWERVR® SGX540 core from Imagination Technologies. It supports phone/PDA and handheld gaming applications. The SGX can process different data types simultaneously, such as: pixel data, vertex data, video data, and general-purpose data processing.

The SGX subsystem has the following features:

- Universal scalable shader engine (USSE™), multithreaded engine incorporating pixel and vertex shader functionality to reduce die area
- Advanced shader feature set in excess of Microsoft VS3.0, PS3.0, and OGL2.0
- Industry-standard API supports Direct3D™ Mobile, OGL-ES 1.1 and 2.0, OpenVG™ 1.1, and OpenMAX™
- Fine-grained task switching, load balancing, and power management
- Programmable high-quality image antialiasing
- Advanced geometry DMA driven operation for minimum CPU interaction
- Fully virtualized memory addressing for OS operation in a unified memory architecture

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- Advanced and standard 2D operations, such as vector graphics, BLTs, ROPs, etc.
- Programmable video encode and decode support for H.264, H.263, MPEG-4 (SP), WMV9, and JPEG

1.3.8 Face Detect Module Description

The face detect module is a stand-alone module that performs face detection and tracking on a picture stored in the SDRAM memory. It communicates with the Cortex-A9 MPU, DSP, and Cortex-M3 MPU subsystems.

Face detect is typically used on:

- Video encoding
- Face-based priority auto-focusing
- Red-eye removal

The face detect module comprises:

- Face detection core with embedded DMA engine for data memory access
- RAM and ROM memories
- L3 and L4 port interfaces

1.3.9 On-Chip Debug Support Description

The on-chip debug support has the following features:

- Multiprocessor debugging lets users control multiple CPU cores embedded in the device, such as:
  - Global starting and stopping of individual or multiple processors
  - Each processor can generate triggers that can be used to alter the execution flow of other processors
  - System clocking and power down
  - Interconnection of multiple devices
  - Channel triggering
- Target debugging, using IEEE1149.1 (JTAG®), or IEEE1149.7 (complementary superset of JTAG) port
- Reduction of power consumption in normal operating mode
- Real-time software trace allows the OMAP software masters to transmit trace data from OS processes or tasks on 256 different channels.

The debug subsystem includes:

- IEEE1149.7 adapter
- Generic TAP for emulation and test control (ICEPick-D™)
- Debug access port (DAP)
- Processor trace subsystem
- System trace subsystem
- EMU configuration interconnect
- Cross-triggering unit (XTRIGGER)
- Debug resource manager (DRM)

ICEMelter:

- Controls the wake-up and power-down of the emulation power domain

CORE instrumentation interconnect:

- Initiator ports:
  - L3 interconnect (for software instrumentation and performance probes)
  - OCP-WP
  - IVA-HD instrumentation (HWA profiling)
  - CM2 instrumentation

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- Target port:
  - EMU instrumentation interconnect

OCP watch-point (OCP-WP):

- Monitors L3 interconnect transaction when target transaction attributes match the user-defined attributes or trigger on external debug event
- Only one instance, shared among the following L3 targets:
  - GPMC
  - L4_PER
  - L4_CFG

Power management events profiler (PM instrumentation)

Clock management events profiler (CM instrumentation)

Statistics collector (performance probes)

1.3.10 Power, Reset, and Clock Management Description

The PRCM module allows efficient control of clocks and power according to the required performance, and reduction of power consumption.

The PRCM module is divided into:

- Power and reset management (PRM), based on the SmartReflex™ framework with the following features:
  - Dynamic clock gating
  - Dynamic voltage and frequency scaling (DVFS)
  - Dynamic power switching (DPS)
  - Static leakage management (SLM)
  - Adaptive body bias (ABB)
  - Retention-till-access (RTA) for memories
- Clock management 1 (CM1) for clock generation, distribution, and management for the Cortex-A9 MPU, ABE, and CORE always-on power domains. The clock management allows reduction of dynamic consumption.
- Clock management 2 (CM2) for clock generation, distribution, and management for other modules

1.3.11 On-Chip Memory Description

The on-chip memory is divided into L3 OCM RAM, SAR ROM, SAR RAM, and memories in the subsystems (Cortex-A9, Cortex-M3, ABE, and IVA-HD).

- The L3 OCM RAM consists of 56KB of on-chip SRAM.
- The save-and-restore (SAR) ROM consists of 4KB and contains a linked list of descriptors used by the system DMA (sDMA).
- The SAR RAM consists of 8KB divided into four blocks. It is used as context-saving memory when the device goes into off mode.

1.3.12 Memory Management Description

The memory management is performed from:

- sDMA controller with up to 127 requests, 32 prioritizable logical channels, and 256 × 64-bit FIFO
- Dynamic memory management (DMM) module, which performs global address translation, address rotation (tiling), and access interleaving

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1.3.13 External Memory Interface Description

There are two main interfaces for connection to external memories: general-purpose memory controller (GPMC) and dual-channel SDRAM controller (SDRC).

The GPMC supports:

- Asynchronous SRAM memories
- Asynchronous/synchronous NOR flash memories
- NAND flash memories
- Pseudo-SRAM devices

The SDRC/EMIF allows:

- Connection between the device and LPDDR2-type memory. It supports double-data rate (DDR) and single-data rate (SDR) protocols. The EMIF is the interface between LPDDR2 SDRAM/NVM and the Cortex-A9 MPU subsystem, ISS, IVA-HD subsystem, SGX, and DMA controllers.
- PHY is the DDR physical interface, which implements data-rate conversion in compliance with LPDDR2 JEDEC requirements.

1.3.14 System and Connection Peripherals

The OMAP device supports a comprehensive set of peripherals to provide flexible and high-speed (HS) interfacing and on-chip programming resources.

1.3.14.1 System Peripherals

- Seven general-purpose timers (GPTIMER)
- One watchdog timer (WDTIMER)
- One 32-kHz synchronization timer (32KTIMER)
- System control module, which contains registers for the following functions:
  - Static device configuration
  - Debug and observability
  - Status
  - Pad configuration
  - I/O configuration
  - eFuse logic
  - Analog function control
  - System boot decoding logic
- System mailbox with eight mailbox message queues
- One SPINLOCK module with 32 hardware semaphores, which can service tasks between the Cortex-A9 MPU, DSP, and Cortex-M3 MPU subsystems
- One chip-to-chip (C2C) interface, which services the communication between the OMAP device and external devices

1.3.14.2 Connection Peripherals

- Three universal asynchronous receiver/transmitter (UART) modules as serial-communication interfaces
- One UART + IrDA SIR up to FIR + TV remote control interface (CIR)
- McBSP module to provide full-duplex serial communication between the OMAP and other applications chips and codecs
- Five HS I^2C™ controller modules; four of them are general-purpose modules with rates up to 3.4 Mbps, and the fifth one, in the PRCM module, performs dynamic voltage control and power sequencing with an external power IC.
- HDQ™/ 1-Wire® – Benchmarq HDQ and Dallas Semiconductor 1-Wire protocols interface
- Two HS MMC/SD/SDIO modules with 8-bit data bus interface, that can act as an initiator on L3

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interconnect thanks to an embedded DMA

- Three HS MMC/SD/SDIO modules with 4-bit data bus interface
- Six general-purpose input/output (GPIO) modules with 32 I/Os each
- One keyboard controller, which supports up to 9 × 9 matrix keypads
- One MIPI SLIMbus interface
- Four multichannel serial peripheral interface (MCSPI) modules
- One HS universal serial bus (USB) On-The-Go (OTG) module with embedded PHY, compliant with the USB2.0 (up to 480 Mbps) standard for HS functions and with the OTG supplement
- One HS multiport USB host module, which can be used for interchip connection or with an off-chip transceiver. It is compliant with the USB2.0 standard. The USB host module allows communication with USB peripherals with data rates up to 480 Mbps for HS, up to 12 Mbps for full-speed, and up to 1.5 Mbps for low-speed.
- One full-speed USB module compliant with the USB1.1 standard for full-speed functions
- One MIPI high-speed synchronous serial interface (HSI) module with two full-duplex serial communication interfaces. It is used for communication between the OMAP device and an external device, with data rates up to 192 Mbps for transmission, and up to 225 Mbps for reception. The MIPI HSI supports 16 logical channels on each destination (RX/TX).

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1.4 Package-On-Package Concept

The OMAP4460 die uses flip-chip technology. The OMAP4460 package-on-page (POP) device supports memory stacking using a POP implementation.

The OMAP4460 die provides two LPDDR2 interfaces. Because each interface supports up to two chip-selects (CSs), up to four LPDDR2 memory dies are supported. Those interfaces are available only on device top ball out.

The two stacked memory packages are directly connected to the two LPDDR2 EMIF4D interfaces of the OMAP4460 die.

Figure 1-3 shows the concept of the POP solution, and Figure 1-4 shows stacked memory package on the POP device.

Figure 1-3. POP Concept

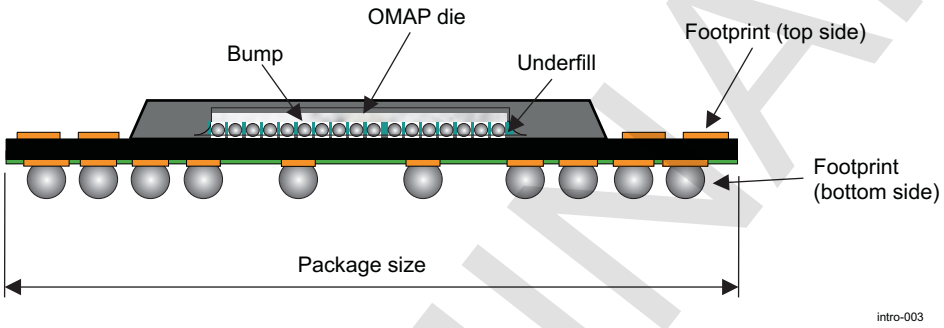
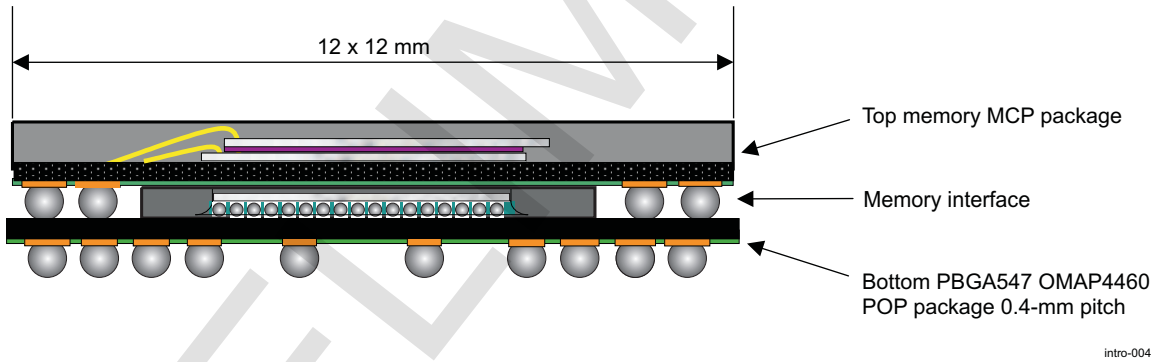


Figure 1-4. Stacked Memory Package on the POP Device



Two types of LPDDR-SDRAM memories are supported in the POP package: S4 and S2, with size up to 2GB and 32-bit data width.

The POP device includes feedthroughs. The feedthroughs are defined from the bottom ball-grid array (BGA) to the stacked memory. The purpose of some of the feedthroughs is to provide power supply to the stacked memories.

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1.5 OMAP4460 Family and Device Identification

The OMAP4460 family is composed of the following devices:

- OMAP4460-1200
- OMAP4460-1500

Table 1-1 describes the identification registers.

The identification registers include the data registers listed in Table 1-2 and Table 1-3. These registers are read-only accessed ports that are programmed into eFuses FARM FROM.

Table 1-1. Device Identification Registers

Register Name	Alias Name	Physical Address	Address Offset	Size
STD_FUSE_DIE_ID_0[31:0]	DIE_ID[31:0]	0x4A00 2200	0x200	32
ID_CODE[31:0]	ID_CODE[31:0]	0x4A00 2204	0x204	32
STD_FUSE_DIE_ID_1[31:0]	DIE_ID[63:32]	0x4A00 2208	0x208	32
STD_FUSE_DIE_ID_2[31:0]	DIE_ID[95:64]	0x4A00 220C	0x20C	32
STD_FUSE_DIE_ID_3[31:0]	DIE_ID[127:96]	0x4A00 2210	0x210	32
STD_FUSE_PROD_ID_0[31:0]	PROD_ID[31:0]	0x4A00 2214	0x214	32
STD_FUSE_PROD_ID_1[31:0]	PROD_ID[63:32]	0x4A00 2218	0x218	32

Table 1-2. STD_FUSE_DIE_ID

Field	Alias Name	Bits	Value
STD_FUSE_DIE_ID_0[31:0]	DIE_ID[31:0]	–	Single die identifier
STD_FUSE_DIE_ID_1[31:0]	DIE_ID[63:32]	–	Single die identifier
STD_FUSE_DIE_ID_2[31:0]	DIE_ID[95:64]	–	Single die identifier
STD_FUSE_DIE_ID_3[31:0]	DIE_ID[127:96]	–	Single die identifier

The product type can be read in the value of the RAMP_SYSTEM bit field of the Table 1-3 register. The silicon revision can be read in the value of the VERSION bit field of the Table 1-3 register.

Table 1-3. ID_CODE

Field	Bits	Value	Comment
ID_CODE[31:28]	VERSION	See Table 1-5.	Revision number
ID_CODE[27:12]	RAMP_SYSTEM	See Table 1-4.	Ramp system number
ID_CODE[11:1]	TI_IDM	0x17	Manufacturer identity (TI)
ID_CODE[0]	–	0x1	Always set to 1

The ramp system number is hardcoded in the design. Table 1-4 lists the ramp system number values, and Table 1-5 lists the revision number values.

Table 1-4. Ramp System Number Values

Silicon Type	Field	Value
OMAP4460 ES1.0 and ES1.1	ID_CODE[27:12]	0xB94E

Table 1-5. Revision Number Values

Silicon Type	Field	Value
OMAP4460 ES1.0	ID_CODE[31:28]	0x0
OMAP4460 ES1.1	ID_CODE[31:28]	0x2

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Table 1-6. ID_CODE Values

Silicon Type	Field	Value
OMAP4460 ES1.0	ID_CODE[31:0]	0x0B94E02F
OMAP4460 ES1.1	ID_CODE[31:0]	0x2B94E02F

The device type can be read in the Table 1-7 register.

Table 1-7. STD_FUSE_PROD_ID_0

Address Offset	0x0000 0214		
Physical Address	0x4A00 2214	**Instance**	GENERAL
Description	This register shows the device type.		
Type	R		

31 ... 8	7 6 5 4 3 2 1 0
RESERVED	DEVICE_TYPE

Bits	Field Name	Description	Type	Reset Value
31:8	RESERVED	Reserved	R	0x-
7:0	DEVICE_TYPE	Define the device type 0xF0 = GP device Other values = Reserved	R	0x-

NOTE: The CONTROL_STATUS[10:0] DEVICE_TYPE bit field can also be used as a source for device type identification.

Table 1-8. STD_FUSE_PROD_ID_1

Address Offset	0x0000 0218		
Physical Address	0x4A00 2218	**Instance**	GENERAL
Description	This register shows the device type.		
Type	R		

31 30 29 28 27 26 25 24	23 22 21 10 19 18	17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
RESERVED		SILICON_TYPE	RESERVED	

Bits	Field Name	Description	Type	Reset Value
31:18	RESERVED	Reserved	R	0x-
17:16	SILICON_TYPE	Define the silicon performance type 0x1: Standard performance (1.2 GHz) 0x2: High performance (1.5 GHz) Other values: Reserved	R	0x-
15:0	RESERVED	Reserved	R	0x-

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Memory Mapping

This chapter describes the memory mapping in the device.

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2.1 Introduction

The Cortex™-A9 microprocessor unit (MPU) has a 32-bit address port, which allows it to handle a 4-GB space divided into several regions, depending on the target type.

The memory map comprises the following features that are shared among the initiators (for example, the Cortex-A9 MPU subsystem or the image and video accelerator [IVA-HD] subsystem).

- Memory space: General-purpose memory controller (GPMC)
- Dynamic memory management controller (DMM)
- Register spaces: Level 3 (L3) and level 4 (L4) interconnects
- Dedicated spaces: IVA-HD subsystem, graphic accelerator (SGX), etc.

The GPMC and DMM are dedicated to memory connection. The GPMC is used for NOR/NAND flash and static RAM (SRAM) memories. The DMM is used for synchronous dynamic random access memory (SDRAM) memories, such as regular SDR (single-data rate)-SDRAM or mobile DDR (double-data rate)-SDRAM. For more information, see Section 15.2, *Dynamic Memory Manager*, and Section 15.3, *EMIF Controller*.

The L3 interconnect allows the sharing of resources, such as peripherals and external or on-chip memories, among all the initiators of the platform. The L4 interconnects control access to the peripherals.

Transfers across the platform between initiators and targets are physically conditioned by the chip interconnect and can be logically conditioned by firewalls. For more information about the intercommunication (L3 and L4 interconnects) and protection mechanisms implemented in the device, see Section 13.2, *L3 Interconnect*, and Section 13.3, *L4 Interconnects*.

Figure 2-1 shows the interconnect of the device and the main modules and subsystems in the platform.

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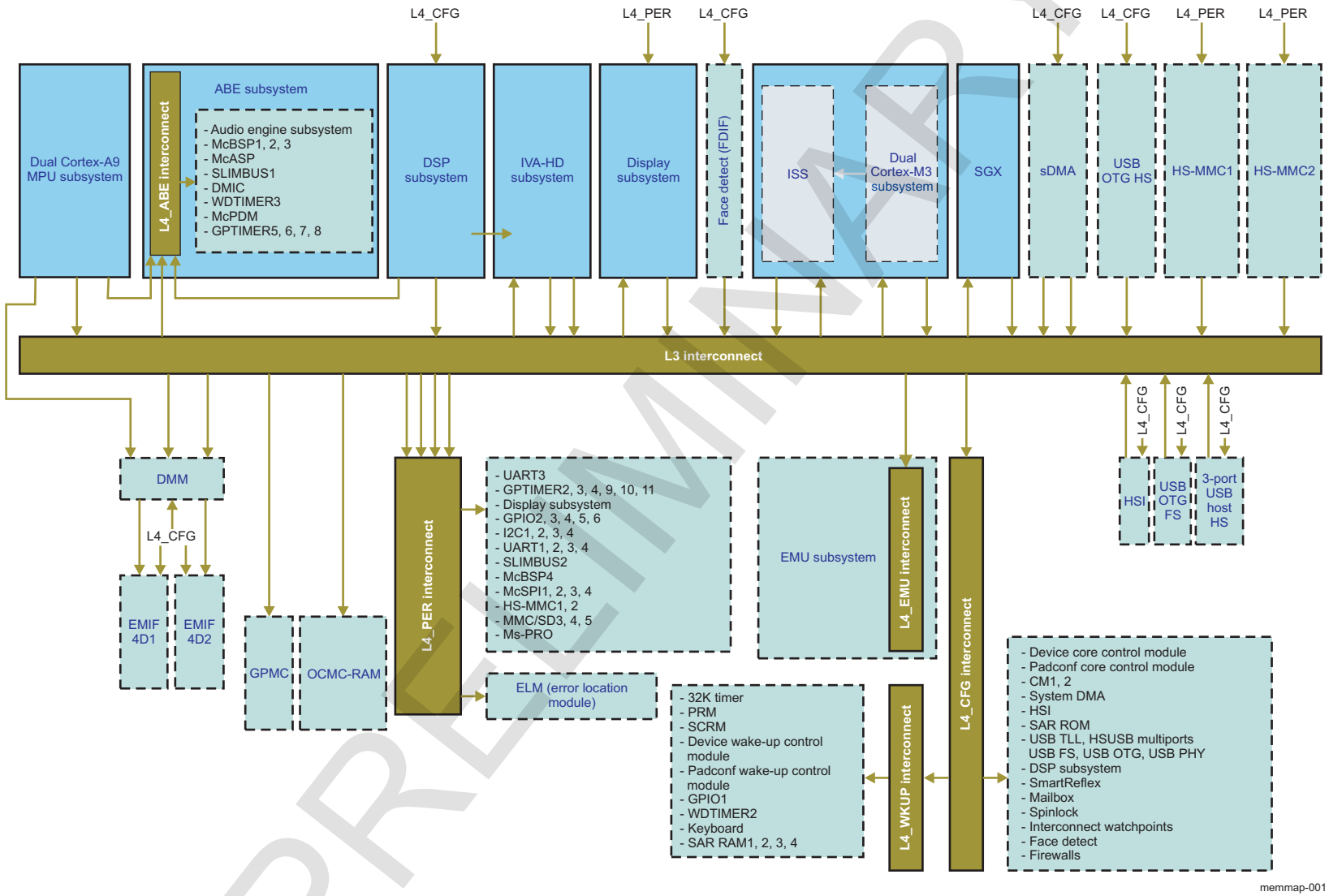
Figure 2-1. Interconnect Overview



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2.2 L3 Memory Space Mapping

The memory space system is hierarchical: level 1 (L1), level 2 (L2), L3, and L4. L1 and L2 are memories in the Cortex-A9 MPU, Cortex™-M3 MPU, and the digital signal processor (DSP) subsystems. L3 handles many types of data transfers, including data exchange with system on-chip/external memories. The chip-level interconnect, which consists of one L3 and four L4s, enables communication among all modules and subsystems.

This section provides a global view of the memory mapping of the device at the L3 interconnect and describes the boot, GPMC, and SDRAM controller (SDRC) (EMIF/DMM) spaces.

The system memory mapping is flexible, with two levels of granularity for target address space allocation:

- L1: Four quarters are labeled Q0, Q1, Q2, and Q3. Each quarter corresponds to a 1-GB address space (total address space is 4GB).
- L2: Each quarter is divided into eight blocks of 32MB, with target spaces mapped in the blocks.

This organization allows all target spaces to be decoded based on the 7 most-significant bits (MSBs) of the 32-bit address ([31:25]).

- Boot space:

  The system has a 48-KB boot space in the on-chip boot ROM or on the GPMC space.

  When booting from the on-chip ROM with the appropriate external sys_boot pin configuration, the 48-KB memory space is redirected to the on-chip boot ROM address space [0x4002 0000–0x4002 BFFF].

  When booting from the GPMC with the appropriate external sys_boot pins configuration, the memory space is part of the GPMC space. At reset, the 0x0000 0000 address is available on chip-select 0(CS0) for a memory size of 16MB.

  For more information about sys_boot pins configuration, see Section 15.4, *General-Purpose Memory Controller*, and Chapter 27, *Initialization*.

- GPMC space:

  Eight independent GPMC chip-selects (gpmc_ncs0 to gpmc_ncs7) are available in the first quarter (Q0) of the addressing space to access NOR/NAND flash and SRAM. The chip-selects have a programmable start address and programmable size (16MB, 32MB, 64MB, or 128MB) in a total memory space of 1GB.

- EMIF1/EMIF2 CS0 space:

  Q2 addressing space is interleaved on two LPDDR-memory controllers (EMIF1|EMIF2), each activating its CS0 line (lpddr21_ncs0 and lpddr22_ncs0). These chip-selects can address 64, 128, 256, 512, 1024, and 2048MBs. Interleaving occurs from 128-byte granularity up to 512-byte granularity.

  Both memories must be of the same kind (SDRAM or nonvolatile memory [NVM]).

  The EMIF1-CS0 base address is always 0x8000 0000 at reset, and occupies a 1-GB address space at reset (interleaving disabled at reset).

- EMIF1/EMIF2 CS1 space:

  Q3 addressing space is interleaved on two LPDDR-memory controllers (EMIF1|EMIF2), each activating its CS1 line (lpddr21_ncs1 and lpddr22_ncs1). These chip-selects can be programmed to 64, 128, 256, 512, and 1024MBs. Interleaving occurs at 128-MB granularity.

  EMIF1-CS1 and EMIF2-CS1 are disabled at reset. Their base address is programmable to achieve a continuous address space with the respective CS0, regardless of the address range programmed.

  EMIF1-CS1 is disabled if EMIF1-CS0 memory density is set to 2048MB (2GBs) when interleaving is disabled, or if EMIF1-CS0 + EMIF2-CS0 memory density are set to 1024MB (1GB) when interleaving is enabled.

- Tiler space:

  Q3 addressing space is also used to access the Tiler system. This space is visible only for the imaging subsystem (ISS) and display subsystem.

Table 2-1 describes the global memory space mapping.

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Table 2-1. Global Memory Space Mapping

Quarter	Module Name	Start Address (hex)	End Address (hex)	Size	Description
Q0 (1GB)	Boot space GPMC (1)	0x0000 0000	0x3FFF FFFF	1GB	
	GPMC	0x0000 0000	0x3FFF FFFF	1GB	8/16 Ex(2)/R/W
Q1 (1GB)	On-chip memory	0x4000 0000	0x7FFF FFFF	1GB	ROM/SRAM address space
	Reserved	0x4000 0000	0x4002 7FFF	160KB	Reserved
	Boot ROM internal	0x4003_0000	0x4003_0000	48KB	32-bit Ex(2)/R Boot ROM
	Reserved	0x4003 4000	0x400F FFFF	816KB	Reserved
	Audio back-end (ABE)	0x4010 0000	0x401F FFFF	1MB	ABE domain (direct Cortex-A9 MPU access). See Table 2-6.
	Reserved	0x4020 0000	0x402F FFFF	1MB	Reserved
	L3 OCM_RAM	0x4030 0000	0x4030 DFFF	56KB	32-bit Ex/R/W
	Reserved	0x4030 E000	0x43FF FFFF	63MB	Reserved
	L3 configuration registers	0x4400 0000	0x47FF FFFF	64MB	L3 configuration registers
	L4_PER domain	0x4800 0000	0x48FF FFFF	16MB	Peripheral domain (see Table 2-5)
	L4_ABE domain	0x4900 0000	0x49FF FFFF	16MB	ABE domain (double-mapped for Cortex-A9 MPU)
	L4_CFG domain	0x4A00 0000	0x4AFF FFFF	16MB	Configuration register domain (see Section 2.2, *L3 Memory Space Mapping*). Also Includes L4_WKUP.
	Reserved	0x4B00 0000	0x4BFF FFFF	16MB	Reserved
	EMIF1 registers	0x4C00 0000	0x4CFF FFFF	16MB	Configuration registers
	EMIF2 registers	0x4D00 0000	0x4DFF FFFF	16MB	Configuration registers
	DMM registers	0x4E00 0000	0x4FFF FFFF	32MB	Configuration registers
	GPMC	0x5000 0000	0x51FF FFFF	32MB	Configuration registers
	ISS	0x5200 0000	0x53FF FFFF	32MB	ISP5 (128KB) + SIMCOP (128KB)
	L3_EMU domain	0x5400 0000	0x54FF FFFF	16MB	Emulation domain (see Table 2-2)
	Dual Cortex-M3 subsystem target	0x5500 0000	0x55FF FFFF	16MB	Dual Cortex-M3 subsystem target
	SGX	0x5600 0000	0x57FF FFFF	32MB	3D SGX540 domain
	Display subsystem	0x5800 0000	0x58FF FFFF	16MB	Display subsystem domain
	Reserved			16MB	Reserved
	IVA-HD configuration	0x5A00 0000	0x5AFF FFFF	16MB	IVA-HD domain
	IVA-HD SL2	0x5B00 0000	0x5BFF FFFF	16MB	IVA-HD SL2 domain
	C2C	0x5C00 0000	0x5FFF FFFF	64MB	Chip-to-chip domain
	Tiler	0x6000 0000	0x7FFF FFFF	512MB	Tiler address mapping
Q2 (1GB)	DRAM address space	0x8000 0000	0xBFFF FFFF	1GB	DDR-SDRAM CS0 address space
	EMIF1-CS0 SDRAM	0x8000 0000	0xBFFF FFFF	1GB	DDR Ctrl1 chip-select 0
	EMIF2-CS0 SDRAM	0x8000 0000	0xBFFF FFFF	1GB	DDR Ctrl2 chip-select 0
Q3 (1GB)	DRAM address space	0xC000 0000	0xFFFF FFFF	1 GB	DDR-SDRAM CS1 address space
	EMIF1-CS1 SDRAM	0xC000 0000	0xFFFF FFFF	1GB	DDR Ctrl1 chip-select 1
	EMIF2-CS1 SDRAM	0xC000 0000	0xFFFF FFFF	1GB	DDR Ctrl2 chip-select 1
	Tiler view (visible only for ISS and display subsystem)				
	Tiler view 0	0x1 0000 0000	0x1 1FFF FFFF	512MB	Natural view
	Tiler view 1	0x1 2000 0000	0x1 3FFF FFFF	512MB	0° view with vertical mirror
	Tiler view 2	0x1 4000 0000	0x1 5FFF FFFF	512MB	0° view with horizontal mirror
	Tiler view 3	0x1 6000 0000	0x1 7FFF FFFF	512MB	180° view
	Tiler view 4	0x1 8000 0000	0x1 9FFF FFFF	512MB	90° view with vertical mirror

(1) Boot space location depends on the external sys_boot[5:0] pins.
(2) Ex = Executable

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Table 2-1. Global Memory Space Mapping (continued)

Quarter	Module Name	Start Address (hex)	End Address (hex)	Size	Description
	Tiler view 5	0x1 A000 0000	0x1 BFFF FFFF	512MB	270° view
	Tiler view 6	0x1 C000 0000	0x1 DFFF FFFF	512MB	90° view
	Tiler view 7	0x1 E000 0000	0x1 FFFF FFFF	512MB	90° view with horizontal mirror

2.2.1 L3_EMU Memory Space Mapping

The L3_EMU interconnect is a 2-MB space composed of the L3_EMU interconnect configuration registers and module registers.

Table 2-2 describes the mapping of the registers for the L3_EMU interconnect.

Table 2-2. L3_EMU Memory Space Mapping

Region Name	Start Address (hex)	End Address (hex)	Size
MIPI_STM [256 × 4K channels] (address space 0)	0x5400 0000	0x540F FFFF	1MB
MIPI_STM [256 × 1K channels] (address space 1)	0x5410 0000	0x5413 FFFF	256KB
Cortex-A9 CPU0 debug/PMU	0x5414 0000	0x5414 1FFF	8KB
Cortex-A9 CPU1 debug/PMU	0x5414 2000	0x5414 3FFF	8KB
Reserved	0x5414 4000	0x5414 7FFF	16KB
CTI0 component	0x5414 8000	0x5414 8FFF	4KB
CTI1 component	0x5414 9000	0x5414 9FFF	4KB
Reserved	0x5414 A000	0x5414 BFFF	8KB
PTM0 component	0x5414 C000	0x5414 CFFF	4KB
PTM1 component	0x5414 D000	0x5414 DFFF	4KB
Reserved	0x5414 E000	0x5415 7FFF	8KB
Trace funnel	0x5415 8000	0x5415 8FFF	4KB
DAP_PC	0x5415 9000	0x5415 9FFF	4KB
Reserved	0x5415 A000	0x5415 EFFF	20KB
APB bridge control and time-out register	0x5415 F000	0x5415 FFFF	4KB
DRM (interconnect)	0x5416 0000	0x5416 0FFF	4KB
MIPI_STM (interconnect)	0x5416 1000	0x5416 1FFF	4KB
ETB (APBv3)	0x5416 2000	0x5416 2FFF	4KB
CS_TPIU (APBv3)	0x5416 3000	0x5416 3FFF	4KB
CS_TF0 (APBv3)	0x5416 4000	0x5416 4FFF	4KB
Reserved	0x5416 5000	0x5416 6FFF	8KB
Technology-specific interconnect registers	0x5416 7000	0x5416 7FFF	4KB
Reserved	0x5416 8000	0x5417 FFFF	96KB
Technology-specific interconnect registers	0x5418 0000	0x5418 0FFF	4KB
Reserved	0x5418 1000	0x541F FFFF	508KB

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2.3 L4 Memory Space Mapping

Four L4 interconnects handle transfers with peripherals. Each interconnect is in a distinct power domain:

- L4_CFG: CORE power domain
- L4_WKUP: WKUP power domain
- L4_PER: PER power domain
- L4_ABE: ABE power domain

As with the L3 interconnect, the L4 interconnect can be configured to tune the access according to the characteristics of each module.

The following sections describe the register mapping of the L4 interconnect. Software configures these registers.

2.3.1 L4_CFG Memory Space Mapping

The L4_CFG interconnect is a 16-MB space composed of the L4_CFG interconnect configuration registers and the module registers.

Table 2-3 describes the mapping of the registers for the L4_CFG interconnect.

NOTE: All memory spaces described as modules provide direct access to module registers outside the L4_CFG interconnect. All other accesses are internal to the L4_CFG interconnect.

Table 2-3. L4_CFG Memory Space Mapping

Module Name	Start Address (hex)	End Address (hex)	Size	Description
L4_CFG configuration	0x4A00 0000	0x4A00 07FF	2KB	Address/protection (AP)
	0x4A00 0800	0x4A00 0FFF	2KB	Link agent (LA)
	0x4A00 1000	0x4A00 1FFF	4KB	Initiator port (IP0)
SYSCTRL_GENERAL_CORE	0x4A00 2000	0x4A00 2FFF	4KB	Module
	0x4A00 3000	0x4A00 3FFF	4KB	L4 interconnect
CM1: Manages Cortex-A9 MPU, DSP, IVA, ABE, memory interface, digital phase-locked loops (DPLLs) for Cortex-A9 MPU, DSP, ABE, CORE	0x4A00 4000	0x4A00 4FFF	4KB	Module region A
	0x4A00 5000	0x4A00 5FFF	4KB	L4 interconnect
Reserved	0x4A00 6000	0x4A00 7FFF	8KB	Reserved
CM2 (manages all others)	0x4A00 8000	0x4A00 9FFF	8KB	Module
	0x4A00 A000	0x4A00 AFFF	4KB	L4 interconnect
Reserved	0x4A00 B000	0x4A05 5FFF	300KB	Reserved
System DMA (sDMA)	0x4A05 6000	0x4A05 6FFF	4KB	Module
	0x4A05 7000	0x4A05 7FFF	4KB	L4 interconnect
HSI	0x4A05 8000	0x4A05 8FFF	4KB	HSI top
	0x4A05 9000	0x4A05 9FFF	4KB	HSI DMA
	0x4A05 A000	0x4A05 AFFF	4KB	HSI port 1
	0x4A05 B000	0x4A05 BFFF	4KB	HSI port 2
	0x4A05 C000	0x4A05 CFFF	4KB	L4 interconnect
Reserved	0x4A05 D000	0x4A05 DFFF	4KB	Reserved
SAR_ROM (save and restore)	0x4A05 E000	0x4A05 FFFF	8KB	Module
	0x4A06 0000	0x4A06 0FFF	4KB	L4 interconnect
Reserved	0x4A06 1000	0x4A06 1FFF	4KB	Reserved
HSUSBTLL	0x4A06 2000	0x4A06 2FFF	4KB	Module
	0x4A06 3000	0x4A06 3FFF	4KB	L4 interconnect

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Table 2-3. L4_CFG Memory Space Mapping (continued)

Module Name	Start Address (hex)	End Address (hex)	Size	Description
HSUSBHOST	0x4A06 4000	0x4A06 4FFF	4KB	Module
	0x4A06 5000	0x4A06 5FFF	4KB	L4 interconnect
DSP subsystem	0x4A06 6000	0x4A06 6FFF	4KB	Module
	0x4A06 7000	0x4A06 7FFF	4KB	L4 interconnect
Reserved	0x4A06 8000	0x4A0A 8FFF	266KB	Reserved
FSUSB	0x4A0A 9000	0x4A0A 9FFF	4KB	Module
	0x4A0A A000	0x4A0A AFFF	4KB	L4 interconnect
HSUSBOTG	0x4A0A B000	0x4A0A BFFF	4KB	Module
	0x4A0A C000	0x4A0A CFFF	4KB	L4 interconnect
USBPHY	0x4A0A D000	0x4A0A DFFF	4KB	Module
	0x4A0A E000	0x4A0A EFFF	4KB	L4 interconnect
Reserved	0x4A0A F000	0x4A0D 8FFF	144KB	Reserved
SR_MPU (SmartReflex™ MPU)	0x4A0D 9000	0x4A0D 9FFF	4KB	Port SR MPU
	0x4A0D A000	0x4A0D AFFF	4KB	L4 interconnect
SR_IVA (SmartReflex IVA)	0x4A0D B000	0x4A0D BFFF	4KB	Port SR IVA
	0x4A0D C000	0x4A0D CFFF	4KB	L4 interconnect
SR_CORE (SmartReflex core)	0x4A0D D000	0x4A0D DFFF	4KB	Port SR core
	0x4A0D E000	0x4A0D EFFF	4KB	L4 interconnect
Reserved	0x4A0D F000	0x4A0F 3FFF	86KB	Reserved
Mailbox	0x4A0F 4000	0x4A0F 4FFF	4KB	Module
	0x4A0F 5000	0x4A0F 5FFF	4KB	L4 interconnect
Spinlock	0x4A0F 6000	0x4A0F 6FFF	4KB	Module
	0x4A0F 7000	0x4A0F 7FFF	4KB	L4 interconnect
Reserved	0x4A0F 8000	0x4A0F FFFF	32KB	Reserved
SYSCTRL_PADCONF_CORE	0x4A10 0000	0x4A10 0FFF	4KB	Module
	0x4A10 1000	0x4A10 1FFF	4KB	L4 interconnect
OCP-WP – Shared	0x4A10 2000	0x4A10 2FFF	4KB	Module
	0x4A10 3000	0x4A10 3FFF	4KB	L4 interconnect
Reserved	0x4A10 4000	0x4A10 9FFF	24KB	Reserved
Face detect	0x4A10 A000	0x4A10 AFFF	4KB	Module
	0x4A10 B000	0x4A10 BFFF	4KB	L4 interconnect
Reserved	0x4A10 C000	0x4A20 3FFF	992KB	Reserved
C2C-Init firewall	0x4A20 4000	0x4A20 4FFF	4KB	Module
	0x4A20 5000	0x4A20 5FFF	4KB	L4 interconnect
C2C-Target firewall	0x4A20 6000	0x4A20 6FFF	4KB	Module
	0x4A20 7000	0x4A20 7FFF	4KB	L4 interconnect
Reserved	0x4A20 8000	0x4A20 9FFF	8KB	Reserved
MA firewall	0x4A20 A000	0x4A20 AFFF	4KB	Memory adapter configuration registers
	0x4A20 B000	0x4A20 BFFF	4KB	L4 interconnect
EMIF firewall	0x4A20 C000	0x4A20 CFFF	4KB	Configuration registers
	0x4A20 D000	0x4A20 DFFF	4KB	L4 interconnect
Reserved	0x4A20 E000	0x4A20 FFFF	8KB	Reserved
GPMC firewall	0x4A21 0000	0x4A21 0FFF	4KB	Configuration registers
	0x4A21 1000	0x4A21 1FFF	4KB	L4 interconnect
OCMC RAM firewall	0x4A21 2000	0x4A21 2FFF	4KB	Module
	0x4A21 3000	0x4A21 3FFF	4KB	L4 interconnect

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Table 2-3. L4_CFG Memory Space Mapping (continued)

Module Name	Start Address (hex)	End Address (hex)	Size	Description
GFX-T firewall	0x4A21 4000	0x4A21 4FFF	4KB	Module
	0x4A21 5000	0x4A21 5FFF	4KB	L4 interconnect
ISS-T firewall	0x4A21 6000	0x4A21 6FFF	4KB	Module
	0x4A21 7000	0x4A21 7FFF	4KB	L4 interconnect
Dual Cortex-M3-T firewall	0x4A21 8000	0x4A21 8FFF	4KB	Module
	0x4A21 9000	0x4A21 9FFF	4KB	L4 interconnect
Reserved	0x4A21 A000	0x4A21 BFFF	8KB	Reserved
DSS-T firewall	0x4A21 C000	0x4A21 CFFF	4KB	Module
	0x4A21 D000	0x4A21 DFFF	4KB	L4 interconnect
SL2-T firewall	0x4A21 E000	0x4A21 EFFF	4KB	Module
	0x4A21 F000	0x4A21 FFFF	4KB	L4 interconnect
IVAHD-CFG-T firewall	0x4A22 0000	0x4A22 0FFF	4KB	Module
	0x4A22 1000	0x4A22 1FFF	4KB	L4 interconnect
Reserved	0x4A22 2000	0x4A22 5FFF	16KB	Reserved
L4-EMU firewall	0x4A22 6000	0x4A22 6FFF	4KB	Module
	0x4A22 7000	0x4A22 7FFF	4KB	L4 interconnect
L4_ABE firewall	0x4A22 8000	0x4A22 8FFF	4KB	Module
	0x4A22 9000	0x4A22 9FFF	4KB	L4 interconnect
Reserved	0x4A22 A000	0x4A2F FFFF	856KB	Reserved
L4_WKUP	0x4A30 0000	0x4A33 FFFF	256KB	WKUP domain (see Section 2.3.2, *L4_WKUP Memory Space Mapping*)
	0x4A34 0000	0x4A34 0FFF	4KB	L4 interconnect
Reserved	0x4A34 1000	0x4AFF FFFF	13052KB	Reserved

2.3.2 L4_WKUP Memory Space Mapping

The L4_WKUP interconnect is a 256-KB space composed of the L4_WKUP interconnect configuration registers and the module registers.

Table 2-4 describes the mapping of the registers for the L4_WKUP interconnect.

NOTE: All memory spaces described as modules provide direct access to module registers outside the L4_WKUP interconnect. All other accesses are internal to the L4_WKUP interconnect.

Table 2-4. L4_WKUP Peripheral Space Mapping

Module Name	Start Address (hex)	End Address (hex)	Size	Description
L4_WKUP configuration	0x4A30 0000	0x4A30 07FF	2KB	Address/protection (AP)
	0x4A30 0800	0x4A30 0FFF	2KB	Link agent (LA)
	0x4A30 1000	0x4A30 1FFF	4KB	Initiator port (IP0)
Reserved	0x4A30 2000	0x4A30 3FFF	8KB	Reserved
32KTIMER	0x4A30 4000	0x4A30 4FFF	4KB	Module
	0x4A30 5000	0x4A30 5FFF	4KB	L4 interconnect
PRM (power and reset manager)	0x4A30 6000	0x4A30 7FFF	8KB	Module
	0x4A30 8000	0x4A30 8FFF	4KB	L4 interconnect
Reserved	0x4A30 9000	0x4A30 9FFF	4KB	Reserved
SCRM	0x4A30 A000	0x4A30 AFFF	4KB	Module
	0x4A30 B000	0x4A30 BFFF	4KB	L4 interconnect

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Table 2-4. L4_WKUP Peripheral Space Mapping (continued)

Module Name	Start Address (hex)	End Address (hex)	Size	Description
SYSCTRL_GENERAL_WKUP	0x4A30 C000	0x4A30 CFFF	4KB	Module
	0x4A30 D000	0x4A30 DFFF	4KB	L4 interconnect
Reserved	0x4A30 E000	0x4A30 FFFF	8KB	Reserved
GPIO1	0x4A31 0000	0x4A31 0FFF	4KB	Module
	0x4A31 1000	0x4A31 1FFF	4KB	L4 interconnect
Reserved	0x4A31 2000	0x4A31 3FFF	8KB	Reserved
WDTIMER2	0x4A31 4000	0x4A31 4FFF	4KB	Module
	0x4A31 5000	0x4A31 5FFF	4KB	L4 interconnect
Reserved	0x4A31 6000	0x4A31 7FFF	8KB	Reserved
GPTIMER1	0x4A31 8000	0x4A31 8FFF	4KB	Module
	0x4A31 9000	0x4A31 9FFF	4KB	L4 interconnect
Reserved	0x4A31 A000	0x4A31 BFFF	8KB	Module – Address space 0
Keyboard	0x4A31 C000	0x4A31 CFFF	4KB	Module
	0x4A31 D000	0x4A31 DFFF	4KB	L4 interconnect
SYSCTRL_PADCONF_WKUP	0x4A31 E000	0x4A31 EFFF	4KB	Module
	0x4A31 F000	0x4A31 FFFF	4KB	L4 interconnect
Reserved	0x4A32 0000	0x4A32 5FFF	24KB	Reserved
SAR_RAM	0x4A32 6000	0x4A32 6FFF	4KB	Module – SAR space 1
	0x4A32 7000	0x4A32 73FF	1KB	Module – SAR space 2
	0x4A32 7400	0x4A32 7FFF	3KB	Reserved
	0x4A32 8000	0x4A32 87FF	2KB	Module – SAR space 3
	0x4A32 8800	0x4A32 8FFF	2KB	Reserved
	0x4A32 9000	0x4A32 93FF	1KB	Module – SAR space 4
	0x4A32 9400	0x4A32 9FFF	3KB	Reserved
	0x4A32 A000	0x4A32 AFFF	4KB	L4 interconnect
Reserved	0x4A32 B000	0x4A33 FFFF	84KB	Reserved

NOTE: 8-bit and 16-bit peripherals are aligned on 32-bit address boundaries.

2.3.3 L4_PER Memory Space Mapping

The L4_PER interconnect is a 16-MB space composed of the L4_PER interconnect configuration registers and the module registers.

Table 2-5 describes the mapping of the registers for the L4_PER interconnect.

NOTE: All memory spaces described as modules provide direct access to the module registers outside the L4_PER interconnect. All other accesses are internal to the L4_PER interconnect.

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Table 2-5. L4_PER Memory Space Mapping

Module Name	Start Address (hex)	End Address (hex)	Size	Description
L4_PER	0x4800 0000	0x4800 07FF	2KB	Address protection (AP)
	0x4800 0800	0x4800 0FFF	2KB	Link agent (LA)
	0x4800 1000	0x4800 13FF	1KB	Initiator port 0 (IP0)
	0x4800 1400	0x4800 17FF	1KB	Initiator port 1 (IP1)
	0x4800 1800	0x4800 1BFF	1KB	Initiator port 2 (IP2)
	0x4800 1C00	0x4800 1FFF	1KB	Initiator port 3 (IP3)
Reserved	0x4800 2000	0x4801 FFFF	120KB	Reserved
UART3	0x4802 0000	0x4802 0FFF	4KB	Module
	0x4802 1000	0x4802 1FFF	4KB	L4 interconnect
Reserved	0x4802 2000	0x4803 1FFF	64KB	Reserved
GPTIMER2	0x4803 2000	0x4803 2FFF	4KB	Module
	0x4803 3000	0x4803 3FFF	4KB	L4 interconnect
GPTIMER3	0x4803 4000	0x4803 4FFF	4KB	Module
	0x4803 5000	0x4803 5FFF	4KB	L4 interconnect
GPTIMER4	0x4803 6000	0x4803 6FFF	4KB	Module
	0x4803 7000	0x4803 7FFF	4KB	L4 interconnect
Reserved	0x4803 8000	0x4803 DFFF	24KB	Reserved
GPTIMER9	0x4803 E000	0x4803 EFFF	4KB	Module
	0x4803 F000	0x4803 FFFF	4KB	L4 interconnect
Display subsystem	0x4804 0000	0x4804 FFFF	64KB	Display subsystem – Configuration + data
	0x4805 0000	0x4805 0FFF	4KB	L4 interconnect
Reserved	0x4805 1000	0x4805 4FFF	16KB	Reserved
GPIO2	0x4805 5000	0x4805 5FFF	4KB	Module
	0x4805 6000	0x4805 6FFF	4KB	L4 interconnect
GPIO3	0x4805 7000	0x4805 7FFF	4KB	Module
	0x4805 8000	0x4805 8FFF	4KB	L4 interconnect
GPIO4	0x4805 9000	0x4805 9FFF	4KB	Module
	0x4805 A000	0x4805 AFFF	4KB	L4 interconnect
GPIO5	0x4805 B000	0x4805 BFFF	4KB	Module
	0x4805 C000	0x4805 CFFF	4KB	L4 interconnect
GPIO6	0x4805 D000	0x4805 DFFF	4KB	Module
	0x4805 E000	0x4805 EFFF	4KB	L4 interconnect
Reserved	0x4805 F000	0x4805 FFFF	4KB	Reserved
I2C3	0x4806 0000	0x4806 0FFF	4KB	Module
	0x4806 1000	0x4806 1FFF	4KB	L4 interconnect
Reserved	0x4806 2000	0x4806 9FFF	32KB	Reserved
UART1	0x4806 A000	0x4806 AFFF	4KB	Module
	0x4806 B000	0x4806 BFFF	4KB	L4 interconnect
UART2	0x4806 C000	0x4806 CFFF	4KB	Module
	0x4806 D000	0x4806 DFFF	4KB	L4 interconnect
UART4	0x4806 E000	0x4806 EFFF	4KB	Module
	0x4806 F000	0x4806 FFFF	4KB	L4 interconnect
I2C1	0x4807 0000	0x4807 0FFF	4KB	Module
	0x4807 1000	0x4807 1FFF	4KB	L4 interconnect
I2C2	0x4807 2000	0x4807 2FFF	4KB	Module
	0x4807 3000	0x4807 3FFF	4KB	L4 interconnect
Reserved	0x4807 4000	0x4807 5FFF	8KB	Reserved

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Table 2-5. L4_PER Memory Space Mapping (continued)

Module Name	Start Address (hex)	End Address (hex)	Size	Description
SLIMBUS2	0x4807 6000	0x4807 6FFF	4KB	Module
	0x4807 7000	0x4807 7FFF	4KB	L4 interconnect
ELM (error locator module)	0x4807 8000	0x4807 8FFF	4KB	Module
	0x4807 9000	0x4807 9FFF	4KB	L4 interconnect
Reserved	0x4807 A000	0x4808 5FFF	48KB	Reserved
GPTIMER10	0x4808 6000	0x4808 6FFF	4KB	Module
	0x4808 7000	0x4808 7FFF	4KB	L4 interconnect
GPTIMER11	0x4808 8000	0x4808 8FFF	4KB	Module
	0x4808 9000	0x4808 9FFF	4KB	L4 interconnect
Reserved	0x4808 A000	0x4809 5FFF	48KB	Reserved
McBSP4	0x4809 6000	0x4809 6FFF	4KB	Module
	0x4809 7000	0x4809 7FFF	4KB	L4 interconnect
McSPI1	0x4809 8000	0x4809 8FFF	4KB	Module
	0x4809 9000	0x4809 9FFF	4KB	L4 interconnect
McSPI2	0x4809 A000	0x4809 AFFF	4KB	Module
	0x4809 B000	0x4809 BFFF	4KB	L4 interconnect
HSMMC1	0x4809 C000	0x4809 CFFF	4KB	Module
	0x4809 D000	0x4809 DFFF	4KB	L4 interconnect
Reserved	0x4809 E000	0x480A CFFF	60KB	Reserved
MMC/SD3	0x480A D000	0x480A DFFF	4KB	Module
	0x480A E000	0x480A EFFF	4KB	L4 interconnect
Reserved	0x480A F000	0x480B 1FFF	12KB	Reserved
HDQ™ (1-Wire®)	0x480B 2000	0x480B 2FFF	4KB	Module
	0x480B 3000	0x480B 3FFF	4KB	L4 interconnect
HSMMC2	0x480B 4000	0x480B 4FFF	4KB	Module
	0x480B 5000	0x480B 5FFF	4KB	L4 interconnect
Reserved	0x480B 6000	0x480B 6FFF	8KB	Reserved
MCSPI3	0x480B 8000	0x480B 8FFF	4KB	Module
	0x480B 9000	0x480B 9FFF	4KB	L4 interconnect
MCSPI4	0x480B A000	0x480B AFFF	4KB	Module
	0x480B B000	0x480B BFFF	4KB	L4 interconnect
Reserved	0x480B C000	0x480D 0FFF	84KB	Reserved
MMC/SD4	0x480D 1000	0x480D 1FFF	4KB	Module
	0x480D 2000	0x480D 2FFF	4KB	L4 interconnect
Reserved	0x480D 3000	0x480D 4FFF	8KB	Reserved
MMC/SD5	0x480D 5000	0x480D 5FFF	4KB	Module
	0x480D 6000	0x480D 6FFF	4KB	L4 interconnect
Reserved	0x480D 7000	0x4834 FFFF	2532KB	Reserved
I2C4	0x4835 0000	0x4835 0FFF	4KB	Module
	0x4835 1000	0x4835 1FFF	4KB	L4 interconnect
Reserved	0x4835 2000	0x48FF FFFF	13MB	Reserved

2.3.4 L4_ABE Memory Space Mapping

The L4_ABE interconnect is a 16-MB space composed of the L4_ABE interconnect configuration registers and the module registers.

ABE modules are dual-mapped inside the Cortex-A9 MPU/DSP address space:

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- Mapped in L3 as the L4 ABE space
- Mapped in Cortex-A9 MPU and DSP nonshared device map

NOTE: All memory spaces described as modules provide direct access to the module registers outside the L4_ABE interconnect. All other accesses are internal to the L4_ABE interconnect.

Table 2-6 describes the mapping of the registers for the L4_ABE interconnect in the Cortex-A9 MPU nonshared (private) device address range (L4_ABEP).

Table 2-6. ABE Cortex-A9 MPU Memory Space Mapping

Module Name	Start Address (hex)	End Address (hex)	Size	Description
L3_ABE	0x4010 0000	0x4010 3FFF	16KB	ABE domain (direct MPU access)
Reserved	0x4010 4000	0x4012 1FFF	120KB	Reserved
McBSP1	0x4012 2000	0x4012 2FFF	4KB	Module
	0x4012 3000	0x4012 3FFF	4KB	L4 interconnect
McBSP2	0x4012 4000	0x4012 4FFF	4KB	Module
	0x4012 5000	0x4012 5FFF	4KB	L4 interconnect
McBSP3	0x4012 6000	0x4012 6FFF	4KB	Module
	0x4012 7000	0x4012 7FFF	4KB	L4 interconnect
McASP	0x4012 8000	0x4012 8FFF	4KB	McASP CFG port
	0x4012 9000	0x4012 9FFF	4KB	L4 interconnect
	0x4012 A000	0x4012 AFFF	4KB	McASP data port
	0x4012 B000	0x4012 BFFF	4KB	L4 interconnect
SLIMBUS1	0x4012 C000	0x4012 CFFF	4KB	Module
	0x4012 D000	0x4012 DFFF	4KB	L4 interconnect
DMIC	0x4012 E000	0x4012 EFFF	4KB	Module
	0x4012 F000	0x4012 FFFF	4KB	L4 interconnect
WDTIMER3	0x4013 0000	0x4013 0FFF	4KB	Module
	0x4013 1000	0x4013 1FFF	4KB	L4 interconnect
McPDM	0x4013 2000	0x4013 2FFF	4KB	Module
	0x4013 3000	0x4013 3FFF	4KB	L4 interconnect
Reserved	0x4013 4000	0x4013 7FFF	16KB	Reserved
GPTIMER5	0x4013 8000	0x4013 8FFF	4KB	Module
	0x4013 9000	0x4013 9FFF	4KB	L4 interconnect
GPTIMER6	0x4013 A000	0x4013 AFFF	4KB	Module
	0x4013 B000	0x4013 BFFF	4KB	L4 interconnect
GPTIMER7	0x4013 C000	0x4013 CFFF	4KB	Module
	0x4013 D000	0x4013 DFFF	4KB	L4 interconnect
GPTIMER8	0x4013 E000	0x4013 EFFF	4KB	Module
	0x4013 F000	0x4013 FFFF	4KB	L4 interconnect
Reserved	0x4014 0000	0x4017 FFFF	256KB	Reserved
DMEM (64KB)	0x4018 0000	0x4018 FFFF	64KB	Data memory
	0x4019 0000	0x4019 0FFF	4KB	L4 interconnect
Reserved	0x4019 1000	0x4019 FFFF	60KB	Reserved
CMEM (4KB)	0x401A 0000	0x401A FFFF	64KB	Coefficient memory
	0x401B 0000	0x401B 0FFF	4KB	L4 interconnect
Reserved	0x401B 1000	0x401B FFFF	60KB	Reserved
SMEM (32KB)	0x401C 0000	0x401C FFFF	64KB	Module
	0x401D 0000	0x401D 0FFF	4KB	L4 interconnect

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Table 2-6. ABE Cortex-A9 MPU Memory Space Mapping (continued)

Module Name	Start Address (hex)	End Address (hex)	Size	Description
Reserved	0x401D 1000	0x401F 0FFF	128KB	Reserved
AESS configuration	0X401F 1000	0x401F 1FFF	4KB	Module
	0X401F 2000	0x401F 2FFF	4KB	L4 interconnect
Reserved	0x401F 3000	0x401F FFFF	52KB	Reserved

Table 2-7 describes the mapping of the registers for the L3 interconnect.

Table 2-7. ABE L3 Memory Space Mapping

Module Name	Start Address (hex)	End Address (hex)	Size	Description
L4 ABE	0x4900 0000	0x4900 3FFF	16KB	ABE domain (double-mapped for MPU)
Reserved	0x4900 4000	0x4902 1FFF	120KB	Reserved
McBSP1	0x4902 2000	0x4902 2FFF	4KB	Module
	0x4902 3000	0x4902 3FFF	4KB	L4 interconnect
McBSP2	0x4902 4000	0x4902 4FFF	4KB	Module
	0x4902 5000	0x4902 5FFF	4KB	L4 interconnect
McBSP3	0x4902 6000	0x4902 6FFF	4KB	Module
	0x4902 7000	0x4902 7FFF	4KB	L4 interconnect
McASP	0x4902 8000	0x4902 8FFF	4KB	McASP CFG port
	0x4902 9000	0x4902 9FFF	4KB	L4 interconnect
	0x4902 A000	0x4902 AFFF	4KB	McASP data port
	0x4902 B000	0x4902 BFFF	4KB	L4 interconnect
SLIMBUS1	0x4902 C000	0x4902 CFFF	4KB	Module
	0x4902 D000	0x4902 DFFF	4KB	L4 interconnect
DMIC	0x4902 E000	0x4902 EFFF	4KB	Module
	0x4902 F000	0x4902 FFFF	4KB	L4 interconnect
WDTIMER3	0x4903 0000	0x4903 0FFF	4KB	Module
	0x4903 1000	0x4903 1FFF	4KB	L4 interconnect
McPDM	0x4903 2000	0x4903 2FFF	4KB	Module
	0x4903 3000	0x4903 3FFF	4KB	L4 interconnect
Reserved	0x4903 4000	0x4903 7FFF	16KB	Reserved
GPTIMER5	0x4903 8000	0x4903 8FFF	4KB	Module
	0x4903 9000	0x4903 9FFF	4KB	L4 interconnect
GPTIMER6	0x4903 A000	0x4903 AFFF	4KB	Module
	0x4903 B000	0x4903 BFFF	4KB	L4 interconnect
GPTIMER7	0x4903 C000	0x4903 CFFF	4KB	Module
	0x4903 D000	0x4903 DFFF	4KB	L4 interconnect
GPTIMER8	0x4903 E000	0x4903 EFFF	4KB	Module
	0x4903 F000	0x4903 FFFF	4KB	L4 interconnect
Reserved	0x4904 0000	0x4907 FFFF	256KB	Reserved
DMEM (64KB)	0x4908 0000	0x4908 FFFF	64KB	Data memory
	0x4909 0000	0x4909 0FFF	4KB	L4 interconnect
Reserved	0x4909 1000	0x4909 FFFF	60KB	Reserved
CMEM (4KB)	0x490A 0000	0x490A FFFF	64KB	Coefficient memory
	0x490B 0000	0x490B 0FFF	4KB	L4 interconnect
Reserved	0x490B 1000	0x490B FFFF	60KB	Reserved
SMEM (32KB)	0x490C 0000	0x490C FFFF	64KB	Module
	0x490D 0000	0x490D 0FFF	4KB	L4 interconnect

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Table 2-7. ABE L3 Memory Space Mapping (continued)

Module Name	Start Address (hex)	End Address (hex)	Size	Description
Reserved	0x490D 1000	0x490F 0FFF	128KB	Reserved
AESS configuration	0x490F 1000	0x490F 1FFF	4KB	Module
	0x490F 2000	0x490F 2FFF	4KB	L4 interconnect
Reserved	0x490F 3000	0x490F FFFF	52KB	Reserved

Table 2-8 describes the mapping of the registers for the DSP subsystem.

Table 2-8. ABE DSP Memory Space Mapping

Module Name	Start Address (hex)	End Address (hex)	Size	Description
L4 ABE	0x0000 0000	0x0000 3FFF	16KB	Boot space
Reserved	0x0000 4000	0x0002 1FFF	120KB	Reserved
McBSP1	0x0002 2000	0x0002 2FFF	4KB	Module
	0x0002 3000	0x0002 3FFF	4KB	L4 interconnect
McBSP2	0x0002 4000	0x0002 4FFF	4KB	Module
	0x0002 5000	0x0002 5FFF	4KB	L4 interconnect
McBSP3	0x0002 6000	0x0002 6FFF	4KB	Module
	0x0002 7000	0x0002 7FFF	4KB	L4 interconnect
McASP	0x0002 8000	0x0002 8FFF	4KB	McASP CFG port
	0x0002 9000	0x0002 9FFF	4KB	L4 interconnect
	0x0002 A000	0x0002 AFFF	4KB	McASP data port
	0x0002 B000	0x0002 BFFF	4KB	L4 interconnect
SLIMBUS1	0x0002 C000	0x0002 CFFF	4KB	Module
	0x0002 D000	0x0002 DFFF	4KB	L4 interconnect
DMIC	0x0002 E000	0x0002 EFFF	4KB	Module
	0x0002 F000	0x0002 FFFF	4KB	L4 interconnect
WDTIMER3	0x0003 0000	0x0003 0FFF	4KB	Module
	0x0003 1000	0x0003 1FFF	4KB	L4 interconnect
McPDM	0x0003 2000	0x0003 2FFF	4KB	Module
	0x0003 3000	0x0003 3FFF	4KB	L4 interconnect
Reserved	0x0003 4000	0x0003 7FFF	16KB	Reserved
GPTIMER5	0x0003 8000	0x0003 8FFF	4KB	Module
	0x0003 9000	0x0003 9FFF	4KB	L4 interconnect
GPTIMER6	0x0003 A000	0x0003 AFFF	4KB	Module
	0x0003 B000	0x0003 BFFF	4KB	L4 interconnect
GPTIMER7	0x0003 C000	0x0003 CFFF	4KB	Module
	0x0003 D000	0x0003 DFFF	4KB	L4 interconnect
GPTIMER8	0x0003 E000	0x0003 EFFF	4KB	Module
	0x0003 F000	0x0003 FFFF	4KB	L4 interconnect
Reserved	0x0004 0000	0x0007 FFFF	256KB	Reserved
DMEM (64KB)	0x0008 0000	0x0008 FFFF	64KB	Data memory
	0x0009 0000	0x0009 0FFF	4KB	L4 interconnect
Reserved	0x0009 1000	0x0009 FFFF	60KB	Reserved
CMEM (4KB)	0x000A 0000	0x000A FFFF	64KB	Coefficient memory
	0x000B 0000	0x000B 0FFF	4KB	L4 interconnect
Reserved	0x490B 1000	0x490B FFFF	60KB	Reserved
SMEM (32KB)	0x000C 0000	0x000C FFFF	64KB	Module
	0x000D 0000	0x000D 0FFF	4KB	L4 interconnect

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Table 2-8. ABE DSP Memory Space Mapping (continued)

Module Name	Start Address (hex)	End Address (hex)	Size	Description
Reserved	0x000D 1000	0x000F 0FFF	128KB	Reserved
AESS configuration	0x000F 1000	0x000F 1FFF	4KB	Module
	0x000F 2000	0x000F 2FFF	4KB	L4 interconnect
Reserved	0x000F 3000	0x000F FFFF	52KB	Reserved

2.4 Dual Cortex-M3 Subsystem Memory Space Mapping

Table 2-9 describes the mapping of the registers for the dual Cortex-M3.

Table 2-9. Dual Cortex-M3 Memory Space Mapping

Module Name	Start Address (hex)	End Address (hex)	Size
Private Memory Map (can also be accessed by the slave port)			
ROM (16KB)	0x5500 0000	0x5500 3FFF	16KB
RAM (64KB)	0x5502 0000	0x5502 FFFF	64KB
Shared cache/MMU configuration registers	0x5508 0000	0x5508 0FFF	4KB
WKUGEN masks	0x5508 1000	0x5508 1FFF	4KB
Reserved	0x5503 0000	0x5503 FFFF	64KB
32-Bit OCP Port (master port to ISS)			
ISP5	0x5504 0000	0x5505 FFFF	128KB
SIMCOP	0x5506 0000	0x5507 FFFF	128KB
Reserved	0x5508 2000	0x55FF FFFF	16MB–384KB
Bit-Band Mapping (supported at the dual Cortex-M3 interface)			
Bit band region 1	0x2000 0000	0x200F FFFF	1MB
Bit band alias 1	0x2200 0000	0x23FF FFFF	32MB
Bit band region 2	0x4000 0000	0x400F FFFF	1MB
Bit band alias 2	0x4200 0000	0x43FF FFFF	32MB
Private Peripheral Map (accessible only from the dual Cortex-M3)			
Reserved	0xE000 0000	0xE000 0FFF	4KB
DWT	0xE000 1000	0xE000 1FFF	4KB
FPB	0xE000 2000	0xE000 2FFF	4KB
Reserved	0xE000 3000	0xE000 DFFF	44KB
NVIC	0xE000 E000	0xE000 EFFF	4KB
Reserved	0xE000 F000	0xE004 1FFF	204KB
External private peripheral bus	0xE0042000	0xE00F EFFF	756KB
ROM table (registers)	0xE00F F000	0xE00F FFFF	4KB
64-Bit Interconnect Master Port (to L3)			
Boot space[(1)]	0x0000 0000	0x0000 3FFF	–
L3	0x0000 0000	0x5FFF FFFF	1.5GB–1MB
Tiler	0x6000 0000	0x7FFF FFFF	512MB

(1) At reset, the MMU is loaded with page 0, which forces the L2 ROM or L2 RAM to be at address 0x0. The reset page also includes the L2 ROM, L2 RAM, shared cache MMU register, and WUGEN registers.

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2.5 DSP Subsystem Memory Space Mapping

The DSP subsystem can access the ABE and IVA-HD blocks.

ABE has three different address spaces:

- ABE NC: This region is for accesses to registers in ABE. For more information about ABE peripheral memory mapping, see Table 2-6.
- ABE: This region is for accesses to memory in ABE. Memory in the ABE subsystem can be cached in DSP L1 and L2. When enhanced direct memory access (eDMA) tries to access this space, L1/L2 is snooped and if data is present in DSP subsystem caches, data is provided to eDMA from DSP caches. However, if data is not present in DSP caches, the shared cache sends the access to ABE and data returned is not allocated into DSP cache; instead, it is sent to eDMA.
- ABE locked region: This region is similar to the ABE region, except that data from ABE is allocated into DSP caches and returned to eDMA.

The IVA-HD region is for accesses to IVA-HD accelerator memories and registers in IVA-HD. SL2 is the L2 cache in IVA-HD. There are three ways to access the IVA-HD accelerator memories:

- SL2 - L1 region: This region is for accesses to SL2 memory that can be mapped to DSP L1. When eDMA tries to access this space, L1/L2 is snooped and if data is present in DSP caches, the data is provided to eDMA from DSP caches. However, if data is not present in DSP caches, the shared cache sends the access to SL2 and data returned is not allocated into DSP L1 cache; instead, it is sent to eDMA.
- SL2 - L2 region: This region is for accesses to SL2 memory that can be mapped to DSP L2. When eDMA tries to access this space, L1/L2 is snooped and if data is present in DSP caches, the data is provided to eDMA from DSP caches. However, if data is not present in DSP caches, the shared cache sends the access to SL2 and data returned is not allocated into DSP L2 cache; instead, it is sent to eDMA.
- SL2 locked region: This region is similar to the previous regions, except that data is allocated into DSP caches and returned to eDMA.

Table 2-10 describes the mapping of the registers for the DSP subsystem.

Table 2-10. DSP Subsystem Memory Space Mapping

Region Name	Start Address (hex)	End Address (hex)	Size
DSP EDM registers	0x01BC 0000	0x01BC 0FFF	4KB
3PCC_CONFIG	0x01C0 0000	0x01C0 FFFF	64KB
3PTC0_CONFIG	0x01C1 0000	0x01C1 03FF	1KB
3PTC1_CONFIG	0x01C1 0400	0x01C1 07FF	1KB
SYSC_CONFIG	0x01C2 0000	0x01C2 0FFF	4KB
WUGEN	0x01C2 1000	0x01C2 1FFF	4KB
L1 configuration registers	0x01C3 0000	0x01C3 00FF	256B
L2 configuration registers	0x01C3 0200	0x01C3 02FF	256B
Shared cache debug	0x01C3 0400	0x01C3 05FF	512B
Attr MMU	0x01C3 0800	0x01C3 0FFF	2KB
DSP CPU configuration registers	0x01C4 0000	0x01C4 0FFF	4KB
Interrupt controller	0x01C5 0000	0x01C5 FFFF	64KB
DSP unique ID	0x01C6 1000	0x01C6 1FFF	4KB
DSP revision ID	0x01C6 2000	0x01C6 2FFF	4KB
ABE NC region	0x01D0 0000	0x01DF FFFF	1MB
IVA-HD (accelerator memories, NC region)	0x01E0 0000	0x01EF FFFF	1MB
Interconnect registers	0x01F0 0000	0x01FF FFFF	1MB
SL2 - L1	0x1080 0000	0x1081 FFFF	128KB
SL2 - L2	0x1082 0000	0x1083 FFFF	128KB
SL2 locked region - L2/ L1 locked	0x1090 0000	0x1093 FFFF	256KB
ABE	0x10D0 0000	0x10DF FFFF	1MB

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Table 2-10. DSP Subsystem Memory Space Mapping (continued)

Region Name	Start Address (hex)	End Address (hex)	Size
ABE locked region	0x10E0 0000	0x10EF FFFF	1MB
External SOC memories and peripherals	0x2000 0000	0xFFFF FFFF	3584MB

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2.6 Display Subsystem Memory Space Mapping

The display subsystem integrates a display controller (DISPC), a remote frame buffer interface (RFBI), two MIPI® display serial interfaces (DSI1 with four data lanes, and DSI2 with two data lanes), an HDMI link with its PHY (high-definition multimedia interface, digital part), and a video PAL/NTSC encoder (VENC) with video DAC (and TV out buffer).

The DISPC is connected through an interconnect master port to the L3 interconnect and has its own DMAs to fetch the data from the system memory.

There are two views (from the L3_PER and L4_PER interconnects) of the display subsystem memory space mapping.

NOTE: The video DAC (VDAC) function is not supported.

2.6.1 L3 Interconnect View of the Display Memory Space

Table 2-11 lists the display subsystem memory space mapping from the perspective of the Cortex-A9 MPU subsystem through the L3 interconnect.

Table 2-11. L3 Access – Display Subsystem Space Mapping

Module Name	Start Address (hex)	End Address (hex)	Size	Description
Display subsystem registers	0x5800 0000	0x5800 0FFF	4KB	Display subsystem and DSI registers
DISPC	0x5800 1000	0x5800 1FFF	4KB	Display controller
RFBI	0x5800 2000	0x5800 2FFF	4KB	Remote frame buffer interface
VENC	0x5800 3000	0x5800 3FFF	4KB	Video encoder
DSI1	0x5800 4000	0x5800 4FFF	4KB	Display serial interface 1
DSI2	0x5800 5000	0x5800 5FFF	4KB	Display serial interface 2
HDMI	0x5800 6000	0x5800 6FFF	4KB	HDMI configuration registers
HDCP	0x5800 7000	0x5800 7FFF	4KB	HDCP registers
Reserved	0x5800 8000	0x58FF FFFF	16MB	Reserved

2.6.2 L4 Interconnect View of the Display Memory Space

Table 2-12 lists the display subsystem memory space mapping internally from the perspective of the Cortex-A9 MPU subsystem through the L4 interconnect.

Table 2-12. L4_PER Access – Display Subsystem Space Mapping

Module Name	Start Address (hex)	End Address (hex)	Size	Description
Display subsystem registers	0x4804 0000	0x4804 0FFF	4KB	Display subsystem and DSI registers
DISPC	0x4804 1000	0x4804 1FFF	4KB	Display controller
RFBI	0x4804 2000	0x4804 2FFF	4KB	Remote frame buffer interface
VENC	0x4804 3000	0x4804 3FFF	4KB	Video encoder
DSI1	0x4804 4000	0x4804 4FFF	4KB	Display serial interface 1
DSI2	0x4804 5000	0x4804 5FFF	4KB	Display serial interface 2
HDMI	0x4804 6000	0x4804 6FFF	4KB	HDMI configuration registers
HDCP	0x4804 7000	0x4804 7FFF	4KB	HDCP registers
Reserved	0x4804 8000	0x4804 8FFF	32KB	Reserved

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Power, Reset and Clock Management

This chapter describes the power, reset and clock management in the device.

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3.1 Device Power Management Introduction

Power management (efficient use of the limited battery resources on a mobile device) is one of the most important design aspects of any mobile system. It imposes strong control over limited available power resources to ensure they function for the longest possible length of time.

The device power-management architecture ensures maximum performance and operation time for user satisfaction (audio/video support) while offering versatile power-management techniques for maximum design flexibility, depending on application requirements.

This introduction contains the following information:

- Power-management architecture building blocks for the device
- State-of-the-art power-management techniques supported by the power-management architecture of the device

3.1.1 Device Power-Management Architecture Building Blocks

To provide a versatile architecture supporting multiple power-management techniques, the power-management framework is built with three levels of resource management: clock, power, and voltage management.

These management levels are enforced by defining the managed entities or building blocks of the power-management architecture, called the clock, power, and voltage domains.

A domain is a group of modules or subsections of the device that share a common entity (for example, common clock source, common voltage source, or a common power switch). The group forming the domain is managed by a policy manager. For example, a clock for a clock domain is managed by a dedicated clock manager within the power, reset, and clock management (PRCM) module. The clock manager takes into consideration the joint clocking constraints of all the modules belonging to that clock domain (and, hence, receiving that clock).

NOTE: In the following sections, the term *module* is used to represent the device IPs (that is, modules or subsystems), other than the PRCM module, that receive clock, reset, or power signals from the PRCM module.

3.1.1.1 Clock Management

The PRCM module manages the gating (that is, switching off) and enabling of the clocks to the device modules. The clocks are managed based on the requirement constraints of the associated modules. The following sections identify the module clock characteristics, management policy, clock domains, and clock domain management.

3.1.1.1.1 Module Interface and Functional Clocks

Each module within the device has specific clock input characteristics requirements. Based on the characteristics of the clocks delivered to the modules, the clocks are divided into two categories: interface clocks and functional clocks (see Figure 3-1).

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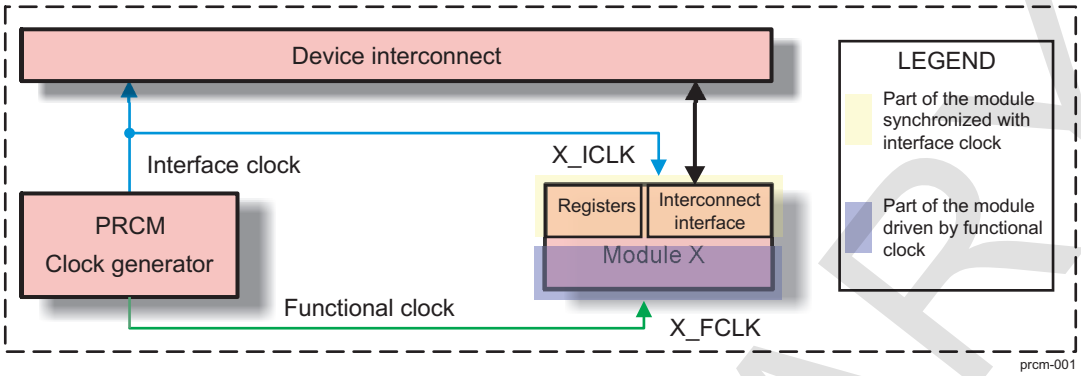
Figure 3-1. Functional and Interface Clocks



The interface clocks have the following characteristics:

- They ensure proper communication between any module/subsystem and the interconnect.
- In most cases, they supply the system interconnect interface and registers of the module.
- A typical module has one interface clock, but modules with multiple interface clocks may also exist (that is, when connected to multiple interconnect buses).
- Interface clock management is done at the device level.
- From the standpoint of the PRCM module, an interface clock is identified with an _ICLK suffix.

Functional clocks have the following characteristics:

- They supply the functional part of a module or a subsystem.
- A module can have one or more functional clocks. Some functional clocks are mandatory, while others are optional for its functioning. A module needs its mandatory clock(s) to be operational. The optional clocks are used for specific features and can be shut down without stopping the module activity (for example, the clock for the camera).
- From the standpoint of the PRCM module, a functional clock is directly distributed to the related modules through a dedicated clock tree. It is identified with an _FCLK suffix.

NOTE: At the module level, the interface clocks are always fed by the interface clock outputs of the PRCM module. The functional clocks are fed either by a PRCM module functional clock output, or by a PRCM module interface clock output. In the latter case, the functional and interface module clocks inherit the clock-management features (autoidle features) of the PRCM module interface clock.

3.1.1.1.2 Module-Level Clock Management

Each module in the device may also have specific clock requirements. Certain module clocks must be *active* when operating in specific modes, or may be gated otherwise. Globally, the activation and gating of the module clocks are managed by the PRCM module. Hence, the PRCM module must be aware of when to activate and when to gate the module clocks.

The PRCM module differentiates the clock-management behavior for device modules based on whether the module can initiate transactions on the device interconnect (called master module) or it cannot initiate transactions and only responds to the transactions initiated by the master (called slave module). Thus, two hardware-based power-management protocols are used:

- Master standby protocol: Clock-management protocol between the PRCM and master modules
- Slave idle protocol: Clock-management protocol between the PRCM and slave modules

Master standby protocol:

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This protocol is used to indicate that a master module must initiate a transaction on the device interconnect and requests specific (functional and interface) clocks for the purpose. The PRCM module ensures that the required clocks are active when the master module requests the PRCM module to enable them. This is called a module wake-up transition and the module is said to be functional after this transition completes.

Similarly, when the master module no longer requires the clocks, it informs the PRCM module, and the PRCM module can then gate the clocks to the module. The master module is then said to be in standby mode.

Although the protocol is completely hardware-controlled, the software must configure the clock management behavior for the module. This is done by setting the module register bit field ***Module***_SYSCONFIG. MIDLEMODE or ***Module***_SYSCONFIG. STANDBYMODE, as presented in Table 3-1. The behavior, identified by standby mode values, must be configured.

Table 3-1. Master Module Standby Mode Settings

Standby Mode Value	Selected Mode	Description
0x0	Force-standby	The module unconditionally asserts the standby request to the PRCM module, regardless of its internal operations. The PRCM module may gate the functional and interface clocks to the module. This mode must be used carefully because it does not prevent any loss of data at the time the clocks are gated.
0x1	No-standby	The module never asserts the standby request to the PRCM module. This mode is safe from a module point of view as it ensures that the clocks remain active; however, it is not efficient from a power-saving perspective because it never allows the PRCM module output clocks to be gated.
0x2	Smart-standby	The module asserts the standby request based on its internal activity status. The standby signal is asserted only when all ongoing transactions are complete and the module is idled. The PRCM module can then gate the clocks to the module.
0x3	Smart-standby wakeup-capable mode	The module asserts the standby request based on its internal activity status. The standby signal is asserted only when all ongoing transactions are complete and the module is idle. The PRCM module can then gate the clocks to the module. The module may generate (master-related) wake-up events when in standby state. The mode is relevant only if the appropriate module mwakeup output is implemented.

NOTE:

- Smart-standby mode is the preferred mode of operation, while forced-standby and no-standby modes are intended for debugging purposes.
- A master module may support all or some of the standby modes listed in Table 3-1. See the power management section in the module chapter to identify the supported standby mode.

The standby status of a master module is indicated by the CM_***Power domain_Module***_CLKCTRL[x]. STBYST bit in the PRCM module. Table 3-2 describes the master module standby status.

Table 3-2. Master Module Standby Status

STBYST Bit Value	Description
0x0	The module is functional.
0x1	The module is in standby mode.

Table 3-3 lists he enabling conditions for the master module clocks managed by the standby protocol.

Table 3-3. Master Module Clock Enabling Conditions

Relation		Condition
AND		Clock domain is ready.
	OR	Master module standby request is deasserted.

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Table 3-3. Master Module Clock Enabling Conditions (continued)

Relation		Condition
		Master module wake-up request is asserted.

Slave idle protocol:

This hardware protocol allows the PRCM module to control the state of a slave module. The PRCM module informs the slave module, through assertion of an idle request, when its clocks (interface and functional) can be gated. The slave can then acknowledge the request from the PRCM module and the PRCM module is then allowed to gate the clocks to the module. A slave module is said to be in IDLE state when its clocks are gated by the PRCM module.

Similarly, an idled slave module may need to be woken up because of a service request from a master module or as a result of an event (called a wake-up event, for example, interrupt or DMA request) received by the slave module. In this situation the PRCM module enables the clocks to the module and then deasserts the idle request to signal the module to wake up.

Although the protocol is completely hardware-controlled, software must configure the clock management behavior for the slave module. This is done by setting the module register bit field Module_SYSCONFIG.SIDLEMODE or Module_SYSCONFIG.IDLEMODE, as presented in Table 3-4. The behavior, identified by the Idle Mode Value column, must be configured by software.

Table 3-4. Module Idle Mode Settings

Idle Mode Value	Selected Mode	Description
0x0	Force-idle	The module unconditionally acknowledges the idle request from the PRCM module, regardless of its internal operations. This mode must be used carefully because it does not prevent any loss of data at the time the clock is switched off.
0x1	No-idle	The module never acknowledges any idle request from the PRCM module. This mode is safe from a module point of view as it ensures the clocks remain active; however it is not efficient from a power-saving perspective because it does not allow the PRCM module output clock to be shut off, and thus the power domain to be set to a lower power state.
0x2	Smart-idle	The module acknowledges the idle request basing its decision on its internal activity. Namely, the acknowledge signal is asserted only when all pending transactions, interrupts, or direct memory access (DMA) requests are processed. This is the best approach to an efficient system power management.
0x3	Smart-idle wakeup-capable mode	The module acknowledges the idle request basing its decision on its internal activity. Namely, the acknowledge signal is asserted only when all pending transactions, interrupts, or DMA requests are processed. This is the best approach to efficient system power management. The module may generate (IRQ- or DMA-request-related) wake-up events when in idle state. The mode is relevant only if the appropriate module swakeup output(s) is implemented.

NOTE:

- Smart-idle mode is the preferred mode of operation, while forced-idle and no-idle modes are intended for debugging purposes.
- A slave module may support all or some of the idle modes listed in Table 3-4. See the power-management section in the module chapter to identify the supported idle modes.

The idle status of a slave module is indicated by the CM_Power domain_Module_CLKCTRL[x] IDLEST bit field in the PRCM module. Table 3-5 lists the possible idle statuses for a slave module.

Table 3-5. Slave Module Idle Status

IDLEST Bit Value	Idle Status	Description
0x0	Functional	The module is fully functional. The interface and functional clocks are active.
0x1	In transition	The module is performing a wake-up or a sleep transition.

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Table 3-5. Slave Module Idle Status (continued)

IDLEST Bit Value	Idle Status	Description
0x2	Interface idle	The module interface clock is idled. The module may remain functional if using a separate functional clock.
0x3	Full idle	The module is fully idle. the interface and functional clocks are gated.

When configured in smart-idle mode, the slave module may acknowledge the idle request of the PRCM module based on the activity of its interface and/or functional clocks. To define which module clocks (that is, interface and/or functional) should be considered when responding to the PRCM module request, the software must configure the Module_SYSCONFIG[x] CLOCKACTIVITY bit field.

The CLOCKACTIVITY setting is used internally by the module to determine on which part of the module the conditions to acknowledge the PRCM module idle request is tested. As an example, if the functional clock must remain active when the module is in idle mode, then the module must acknowledge PRCM module idle request by only considering the interface clock gating conditions (that is, there is no pending activity on the interconnect).

NOTE: See the power-management section in the module chapter to identify whether this feature is configurable.

Using the CLOCKACTIVITY setting along with the smart-idle mode ensures that the clock remains active for the module features that must remain available during the module idle mode. Table 3-6 describes the possible CLOCKACTIVITY settings for a module:

Table 3-6. Slave Module Clock Activity Settings

CLOCKACTIVITY Bit Value	Module Interface Clock	Module Functional Clock	Description
0x0	Gated	Gated	The interface and functional clocks are considered when generating the acknowledgement. This setting also means both clocks may be gated upon a PRCM module idle request.
0x1	Active	Gated	The interface clock is not shut down and is not considered when generating the acknowledgement to the PRCM module idle request. Only the functional clock is considered.
0x2	Gated	Active	The functional clock is not shut down and is not considered when generating the acknowledgement to the PRCM module idle request. Only the interface clock is considered.
0x3	Active	Active	The interface and functional clocks are not shut down. The module can acknowledge the idle request without checking the internal functionalities linked to its clocks.

(1) Optional if it concerns all features.

NOTE:

- The software configuration of the CLOCKACTIVITY settings may not be available for a given module. For some modules, the CLOCKACTIVITY settings can be hardwired.
- A slave module may support all or some of the CLOCKACTIVITY settings listed in Table 3-6.

See the power-management section in the specific module chapter to identify the supported idle feature and settings.

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The PRCM module does not have any hardware means to read the CLOCKACTIVITY settings of the module. Software must ensure a consistent programming between the CLOCKACTIVITY settings of the module and the PRCM module clock gating control bits. The PRCM module must be configured (where software control is available) not to gate the module clock, which should remain active according to the CLOCKACTIVITY settings of the module.

For the idle protocol management on the PRCM module side, the behavior of PRCM module is configured in the CM_Power domain_module_CLKCTRL[x] MODULEMODE bit field. Based on the configured behavior, the PRCM module asserts the idle request to the module either unconditionally (that is, immediately when the software requests), or through hardware control when the module idle conditions are satisfied. Table 3-7 describes the configurable behavior of MODULEMODE.

Table 3-7. Slave Module Mode Settings in PRCM

MODULEMODE Bit Value	Selected Mode	Description
0x0	Disabled	The PRCM module unconditionally asserts the module idle request. This request applies to the gating of the functional and interface clocks to the module. If acknowledged by the module, the PRCM module can gate all clocks to the module (that is, the module is completely disabled). It can only react to an asynchronous wake-up event (that is, a wake-up event that does not require the module functional clock to be active).
0x1	Auto	This mode applies to a module when the PRCM module only manages its interface clock and not its functional clock. The PRCM module automatically asserts/deasserts the module idle request based on the clock-domain transitions. If acknowledged by the module, the PRCM module can gate the interface clock to the module.
0x2	Enabled	This mode applies to a module when the PRCM module manages its interface and functional clocks. The functional clock to the module remains active unconditionally, while the PRCM module automatically asserts/deasserts the module idle request based on the clock-domain transitions. If acknowledged by the module, the PRCM module can only gate the interface clock to the module.
0x3	Reserved	Not available.

NOTE: The PRCM module may support all or some of the MODULEMODE module settings listed in Table 3-7. See the CM_Power domain_module_CLKCTRL[x] MODULEMODE bit field description for the module to identify the supported settings.

Table 3-8 and Table 3-9 list the enabling conditions for the slave module clocks managed by the Idle protocol.

Table 3-8. Slave Module Interface Clock Enabling Conditions

Relation		Condition
AND		Clock domain is ready.
	OR	Slave module idle status is 0x0 (fully functional).
		Slave module idle status is 0x1 (in transition).
		Slave module wake-up request is asserted.

Table 3-9. Slave Module Functional Clock Enabling Conditions

Relation		Condition
AND		Clock domain is ready.
	OR	Slave module idle status is 0x0 (fully functional).
		Slave module idle status is 0x1 (in transition).

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Table 3-9. Slave Module Functional Clock Enabling Conditions (continued)

Relation		Condition
		Slave module idle status is 0x2 (interface clock is idled).
		Slave module wake-up request is asserted.

The module clock domain must be ready for the optional clocks to the module, and any associated clock-enable control is asserted.

NOTE: A given clock can be used by more that one module. Clock enabling conditions are then ORed together (that is, the clock is provided as soon as one of the enabling conditions is true). As a consequence, the clock is disabled only when all related enabling conditions are false.

Module wake-up request:

In IDLE state, a slave module may have to wake-up to generate an interrupt or a DMA request. This may be the result of an external request (for example, to the I/O port of a general-purpose input/output [GPIO] module) or an internally generated event (for example, WDTIMER time-up). The slave module, with wake-up capability, sends a wake-up request to the PRCM module. The PRCM module then activates the module clocks and acknowledges the module wake-up request.

In IDLE state, some slave modules may require functional clock(s) to generate a wake-up event. Such requests are called synchronous wake-up events on the PRCM module side, while the events generated when the functional or interface module clocks are gated are called asynchronous wake-up events.

NOTE: See the power-management section in the module chapter to identify whether its wake-up event is synchronous or asynchronous.

The standby and idle clock-management protocols allow the configuration of the module-level clock-management interaction between the PRCM module and individual modules of the device. However, the PRCM module may not necessarily gate the clock to the module immediately after the module switches to standby or idle mode at the end of this interaction. This is because the same clock can be shared by other modules that are active and need this shared clock to complete their activity. As a result, the PRCM module provides a second level of clock management called the clock domain level, as explained in Section 3.1.1.1.3.

3.1.1.1.3 Clock Domain

A clock domain is a group of modules fed by clock signals controlled by the same clock manager in the PRCM module (see Figure 3-2). By gating the clocks in a clock domain, the clocks to all the modules belonging to that clock domain can be cut to lower their active power consumption (that is, the device is on and the clocks to the modules are dynamically switched to ACTIVE or INACTIVE (Gated) states). Thus, a clock domain allows control of the dynamic power consumption of the device.

The device is partitioned into multiple clock domains and each clock domain is controlled by an associated clock manager within the PRCM module. This allows the PRCM module to individually activate and gate each clock domain of the device.

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Figure 3-2. Generic Clock Domain

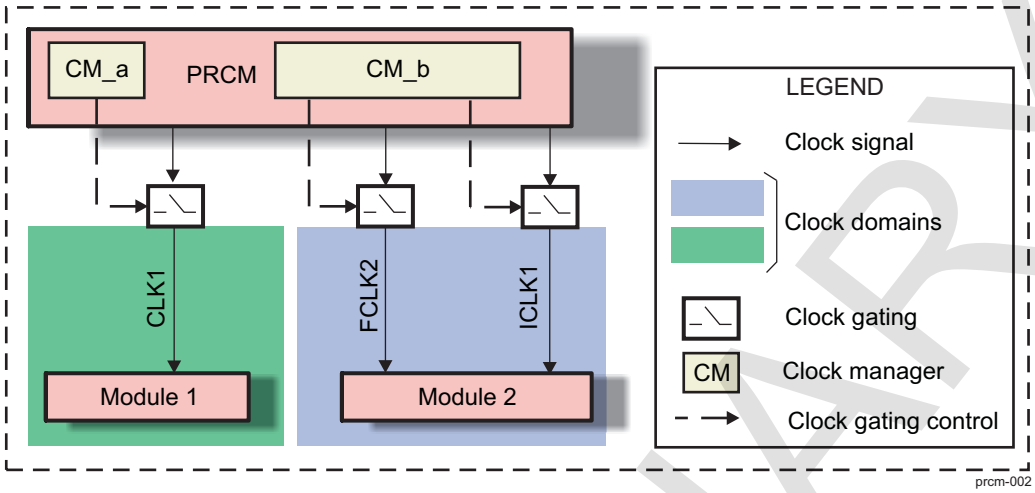

Figure 3-2 presents an example of two clock managers: CM_a and CM_b. Each clock manager manages a clock domain. The clock domain of CM_b is composed of two clocks: a functional clock (FCLK2) and an interface clock (ICLK1), while that of CM_a consists of a clock (CLK1) that is used by the module as functional and interface clock. The clocks to Module 2 can be gated independently of the clock to Module 1, thus ensuring power savings when Module 2 is not in use.

The PRCM module lets software check the status of the clock domain functional clocks. The CM_Clock domain_CLKSTCTRL[x] CLKACTIVITY_FCLK/Clock name_FCLK bit in the PRCM module identifies the state of the functional clock(s) within the clock domain. Table 3-10 lists the two possible states of the functional clock.

Table 3-10. Clock Domain Functional Clock States

CLKACTIVITY Bit Value	Status	Description
0x0	Gated	The functional clock of the clock domain is inactive.
0x1	Active	The functional clock of the clock domain is running.

3.1.1.1.4 Clock Domain-Level Clock Management

The domain clock manager can automatically (that is, based on hardware conditions) and jointly manage the interface clocks within the clock domain. The functional clocks within the clock domain are managed through software settings.

A clock domain can switch between three possible states: ACTIVE, IDLE_TRANSITION, or INACTIVE. Figure 3-3 identifies the sleep and wake-up transitions of the clock domain between the ACTIVE and INACTIVE states.

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Figure 3-3. Clock Domain State Transitions

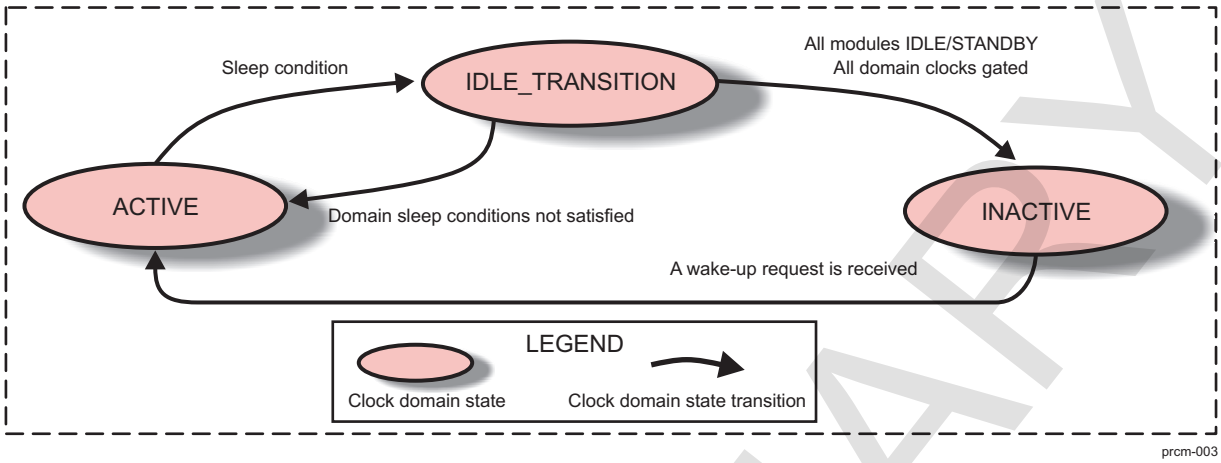

Table 3-11 defines the clock domain states.

Table 3-11. Clock Domain Clock States

State	Description
ACTIVE	• Every nondisabled slave module (that is, those whose MODULEMODE value is not set to disabled) is put out of IDLE state. • All functional clocks to the active slave modules (that is, not idled) of the clock domain are provided. • All interface clocks to the nondisabled slave modules in the clock domain are provided. • All functional and interface clocks to the active master modules (that is, not in STANDBY state) in the clock domain are provided. • Every enabled optional clocks to the modules in the clock domain are provided.
IDLE_TRANSITION	This is a transitory state. • Every master module in the clock domain is in STANDBY state. • Every idle request to all the slave modules in the clock domain is asserted. • The functional clocks to the slave module in enabled state (that is, those whose MODULEMODE values are set to enabled) remain active. • Every enabled optional clocks to the modules in the clock domain are provided.
INACTIVE	All clocks within the clock domain are gated. • Every slave module in the clock domain (that is, those whose MODULEMODE is set to disabled or auto) is in IDLE state and set to disabled or auto mode. • Every master module in the clock domain is in STANDBY state. • Every optional functional clock in the clock domain is gated.

Each clock domain transition behavior is managed by an associated register bit field in the CM_Clock domain_CLKSTCTRL[x] CLKTRCTRL PRCM module.

Table 3-12 describes the clock domain clock transition mode settings.

Table 3-12. Clock Domain Clock Transition Mode Settings

CLKTRCTRL Bit Value	Selected Mode	Description
0x0	NO_SLEEP	A clock domain sleep transition is never initiated, irrespective of the hardware conditions.
0x1	SW_SLEEP	A software-forced sleep transition. The transition is initiated when the associated hardware conditions are satisfied (see Table 3-14).
0x2	SW_WKUP	A software-forced clock domain wake-up transition is initiated, irrespective of the hardware conditions identified in Table 3-13.

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Table 3-12. Clock Domain Clock Transition Mode Settings (continued)

CLKTRCTRL Bit Value	Selected Mode	Description
0x3	HW_AUTO	Hardware-controlled automatic sleep and wake-up transition is initiated by the PRCM module when the associated hardware conditions are satisfied (see Table 3-14 and Table 3-13).

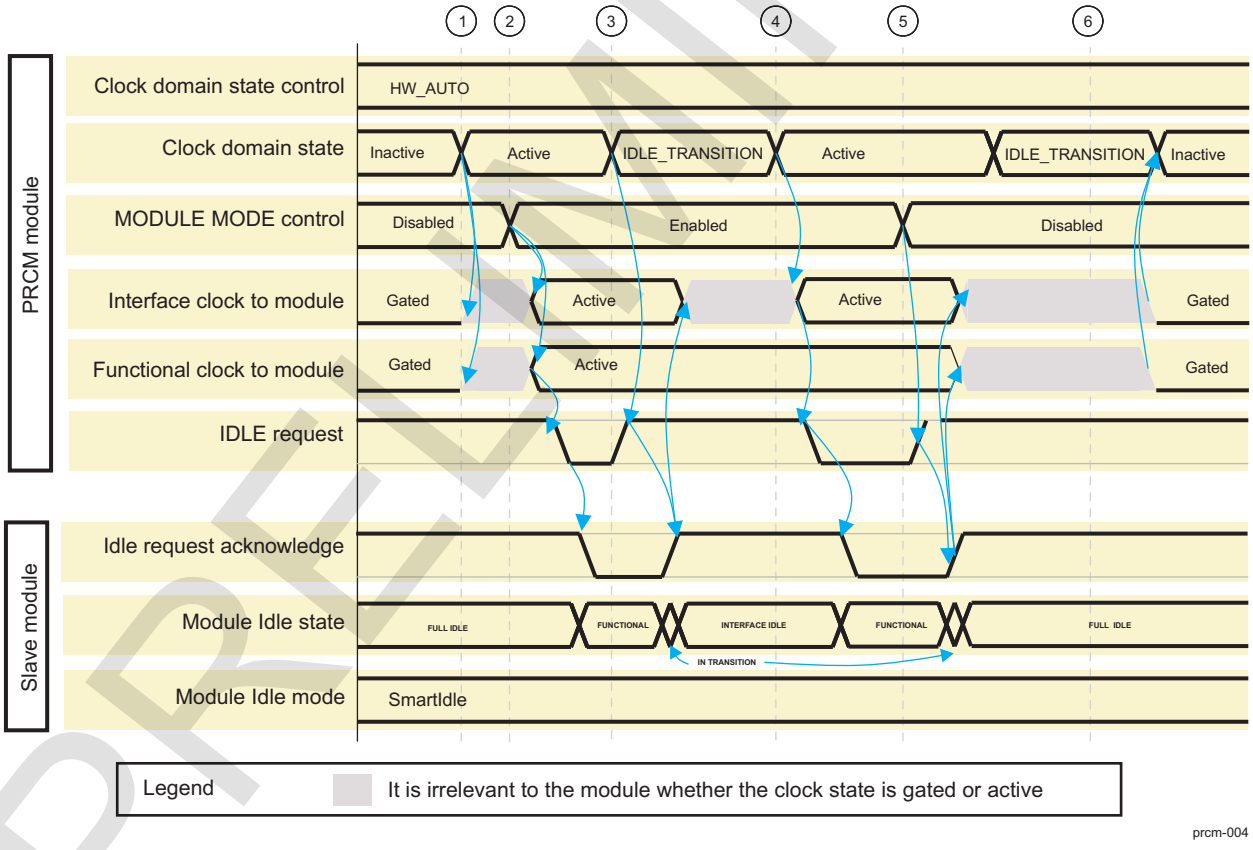
NOTE: Depending on the characteristics of a clock domain, it may or may not support all the clock transition mode settings described in Table 3-12. See the clock domain clock management section of the specific clock domain to identify the supported clock transition mode settings.

3.1.1.1.5 Clock Domain HW_AUTO Mode Sequences

The sequence diagrams in Figure 3-4 through Figure 3-6 identify the PRCM module hardware-controlled enabling and gating of the functional and interface clocks to the module. They highlight the changes in the module state based on the changes to the clock domain state and module mode settings.

Figure 3-4 highlights the behavior of a slave module receiving the interface and functional clocks and having two configurable module modes: Disabled and Enabled.

Figure 3-4. Clock Domain/Slave Module Clock-Management Interaction Sequence 1



Initially, the clock domain, which includes the slave module, is inactive. The module is in FULL-IDLE state and its functional and interface clocks are gated.

1. The clock domain wakes up and changes state to Active. As the Module Mode control is still Disabled, this event has no effect on the module state. The functional and interface clocks may still be restarted automatically, based on the requirements of other modules sharing these clocks.

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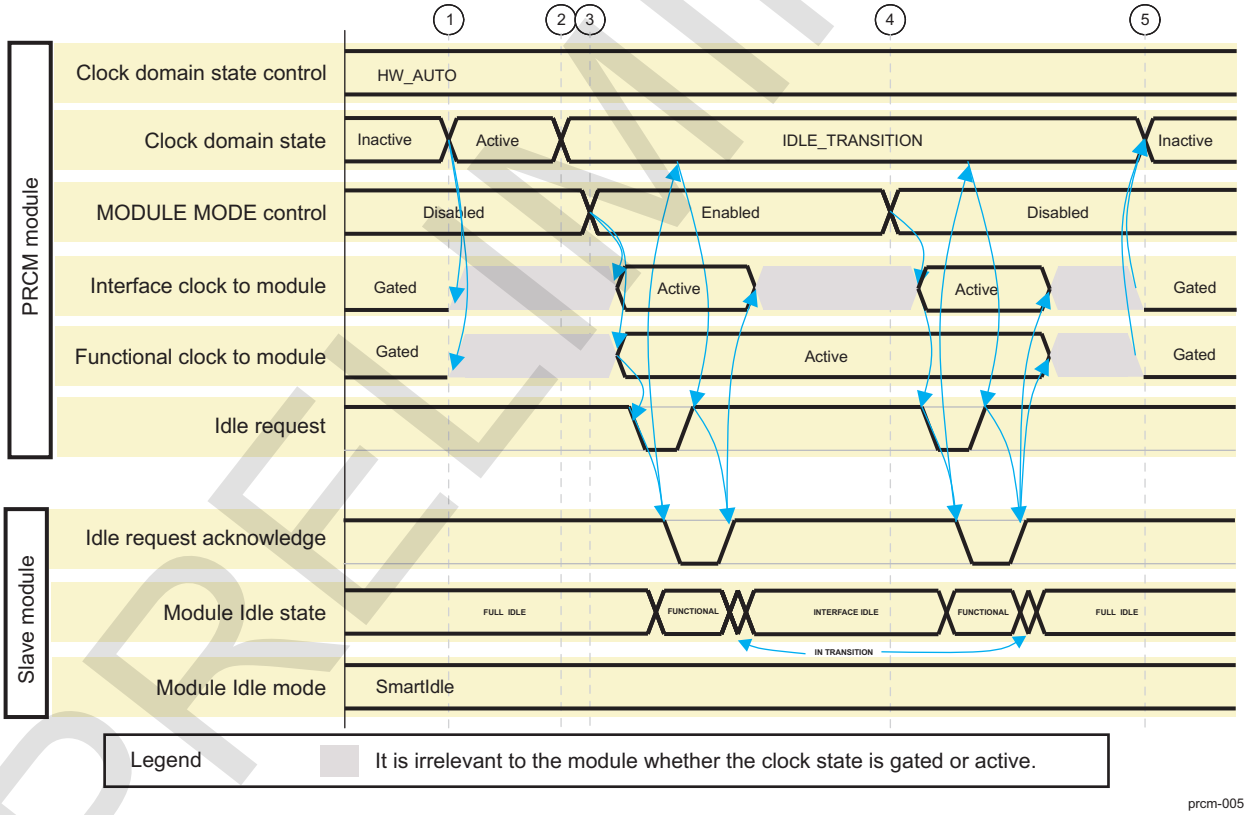
2. Software changes the module mode to Enabled. The clocks to the module are restarted automatically. The PRCM module then deasserts a hardware idle request signal to the module. The module sends an idle request acknowledge to the PRCM module. The module is now effectively awake. The module Idle state is functional. If the module is enabled before the clock domain wakes up, Steps 1 and 2 are simultaneous.
3. The clock domain switches to IDLE_TRANSITION state. In turn, the PRCM module requests the module to go into IDLE state by asserting the idle request signal. When acknowledged, the clock to the module can be gated, depending on other modules sharing the same clock. The functional clock of the module remains enabled as the module is in Enabled mode.
4. The clock domain does not have all conditions to complete the sleep transition, and wakes up again. In turn, the interface clock to the module is automatically restarted, if applicable, then the module is put out of IDLE state.
5. Software disables the module. The PRCM module requests the module to go to IDLE state by asserting the idle request signal. When acknowledged, the clock to the module can be gated, depending on other modules sharing the same clock.
6. The clock domain switches to the IDLE_TRANSITION state. When the clock domain sleep transition conditions are satisfied, the clocks (functional and interface) are gated. The clock domain then switches to INACTIVE state. This has no effect on the module, which is already in FULL-IDLE state.

Figure 3-5 highlights the behavior of the same slave module, receiving the interface and functional clocks, when the module mode is changed while the clock domain state is Idle_Transition.

Figure 3-5. Clock Domain/Slave Module Clock-Management Interaction Sequence 2



Initially, the clock domain, which includes the slave module, is inactive. The module is in FULL-IDLE state and its functional and interface clocks are gated.

1. The clock domain wakes up and changes state to Active. As the Module Mode control is Disabled, this event has no effect on the module state. The functional and interface clocks may still be restarted automatically, based on the requirements of other modules sharing these clocks.
2. The clock domain goes into the IDLE_TRANSITION state. As the Module Mode control is Disabled, this event has no effect on the module state.

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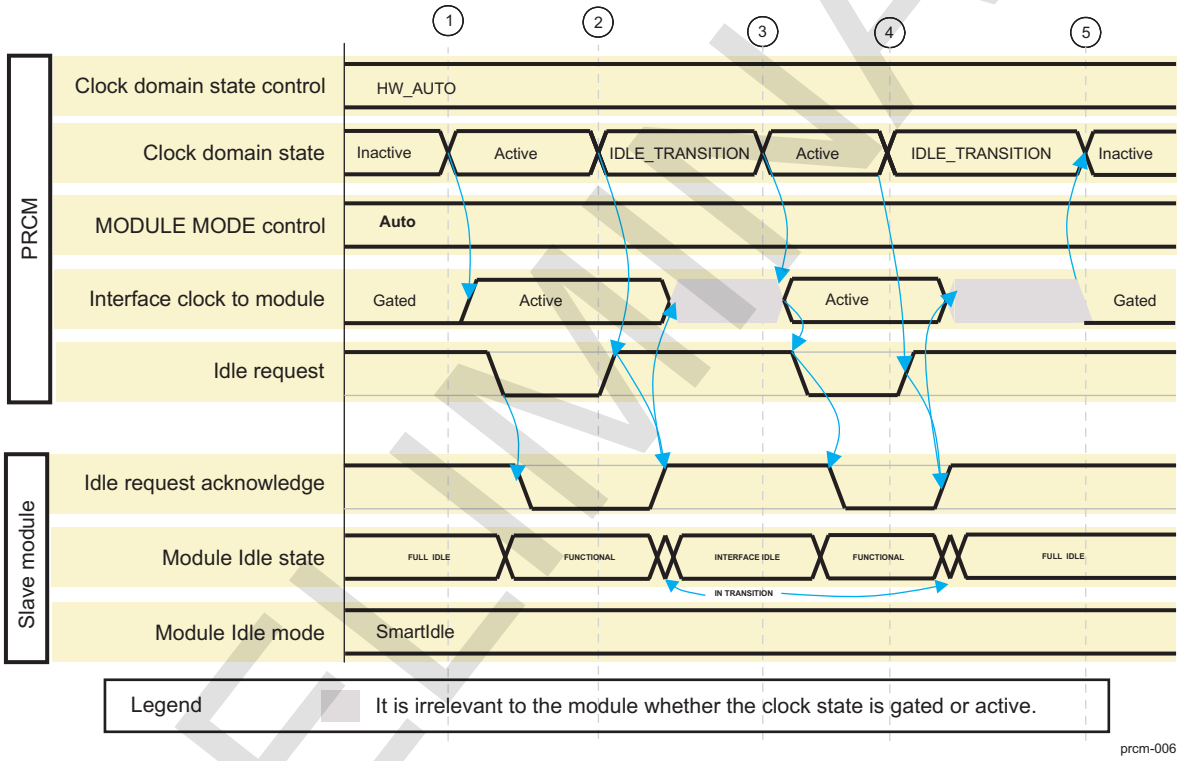
3. Software changes the module mode to Enabled. The clocks to the module are restarted automatically and then the module is put out of IDLE state. As soon as acknowledged, the module is requested to go back to IDLE state with gating of the interface clock only (that is, the INTERFACE IDLE state). The interface clock to the module can be gated, depending on other modules sharing the same clocks.
4. Software disables the module. The interface clock to the module is restarted automatically. The PRCM module requests the module to go to IDLE state by asserting the idle request signal. When acknowledged, the interface and the functional clocks to the module can be gated, depending on other modules sharing the same clock.
5. When the clock domain sleep transition conditions are satisfied and the functional and interface clocks are gated, the clock domain switches to INACTIVE state. This has no effect on the module, which is already in FULL-IDLE state.

Figure 3-6 highlights the behavior of a slave module receiving only interface clock and supporting the configurable Auto module mode.

Figure 3-6. Clock Domain/Slave Module Clock-Management Interaction Sequence 3



Initially, the clock domain, which includes the slave module, is inactive. The module is in FULL-IDLE state and its interface clock is gated.

1. The clock domain wakes up and changes state to Active. In turn, the interface clock to the module is automatically restarted. The PRCM module then deasserts a hardware idle request signal to the module. The module sends an idle request acknowledge to the PRCM module. The module is now effectively awake, that is, the module Idle state is functional.
2. The clock domain switches to the IDLE_TRANSITION state. The PRCM module requests the module to go to IDLE state by asserting the idle request signal. When acknowledged, the interface clock to the module can be gated, depending on other modules sharing the same clock.
3. The clock domain does not have all conditions to complete the sleep transition, and wakes up again. In turn, the interface clock to the module is automatically restarted if applicable, then the module is put out of IDLE state.
4. Same as Step 2.
5. The clock domain has all conditions to complete the sleep transition. The module is under IDLE state and its clock is gated.

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3.1.1.1.6 Clock Domain Sleep/Wakeup

The clock domain manager initiates a domain wake-up transition when the conditions listed in Table 3-13 are satisfied.

Table 3-13. Clock Domain Wake-Up Conditions

Relation	Condition
OR	The SW_WKUP clock transition mode for the clock domain is set. (CLKTRCTRL = 0x2)
	At least one wake-up request asserted by one of the modules of the clock domain.
	At least one dynamic dependency(1) from another clock domain is active.
	At least one static dependency(1) from another clock domain is active.
	At least one wake-up dependency(1) from a module in another clock domain is active.

(1) The dynamic, static dependency and the wake-up dependency are explained in Section 3.1.1.1.7, *Clock Domain Dependency*.

The clock domain manager initiates a domain sleep transition when the conditions listed in Table 3-14 are satisfied.

Table 3-14. Clock Domain Sleep Conditions

Relation			Condition
AND			All master modules in the clock domain are in STANDBY state.
			No wake-up request is asserted by any module of the clock domain.
			No dynamic domain dependency(1) from any other domain is active.
			No wake-up dependency(1) from any module in another domain is active.
	OR		The SW_SLEEP clock transition mode is set for the clock domain (CLKTRCTRL = 0x1).
		AND	The HW_AUTO clock transition mode is set for the clock domain (CLKTRCTRL = 0x3).
			No static domain dependency(1) from any other domain is active

(1) The dynamic, static dependency and the wake-up dependency are explained in Section 3.1.1.1.7, *Clock Domain Dependency*.

3.1.1.1.7 Clock Domain Dependency

A domain dependency is a binary relationship between two clock domains. A clock domain A is said to depend on a clock domain B when a module in clock domain B provides services to a module in clock domain A. As a result, clock domain B must be active when clock domain A is active so that the module in clock domain B is accessible by the module in clock domain A.

The dependency between two clock domains may also exist if one clock domain serves to ensure communication between two modules (for example, the clock domain of the device interconnect).

Thus, a clock domain may support the types of clock domain dependencies described in the following subsections.

3.1.1.1.7.1 Static Dependency

If clock domain A has a master module that can access a slave module in clock domain B, then clock domain A can have a static dependency with clock domain B. Similarly, a static dependency can also exist between domain A and B if domain B conveys the transactions from domain A module toward a module in any other domain. For example, CD_DSP can have a static dependency with CD_L3_1 because this domain has the L3 interconnect to carry the transactions from the DSP module.

This static dependency consists of forcing clock domain B to stay active, as long as there is at least one master module of clock domain A that is not in STANDBY state. If clock domains A and B are initially in GATED state, then clock domain B becomes active as soon as clock domain A becomes active when a wake-up request from the master module is received by the PRCM module.

Similarly, as a result of the static dependency, clock domain B can only be gated if all the master modules of clock domain A that can access the slave modules in clock domain B are in STANDBY state.

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The static dependency between a source clock domain and a destination clock domain is configured in the PRCM module by setting CM_Source Clock domain_STATICDEP[x] Destination Clock domain_STATDEP bit. As a result, the source clock domain forces the destination clock domain to become active and stay active as long as the source clock domain is active.

3.1.1.1.7.2 Dynamic Dependency

When clock domains A and B contain modules directly linked to a common device interconnect, these clock domains can have a dynamic dependency.

A dynamic dependency consists of forcing clock domain B to stay active as long as a module from clock domain A is communicating with the module in clock domain B through the interconnect. Clock domain B becomes active as soon as the communication is initiated. This is automatically managed by the PRCM module by monitoring the communication on the interconnect between the modules of the two clock domains.

Similarly, the inverse condition of this dependency can be stated: Clock domain B can be inactive only if all modules between clock domains A and B are quiet for a given sampling delay, identified as a sliding window duration on the interconnect activity status.

The size of the sliding window is based on the number of cycles of a prescaled L4 clock whose frequency is configured by setting the CM_DYN_DEP_PRESCAL[5:0] PRESCAL bit field. The prescaled clock frequency is given as:

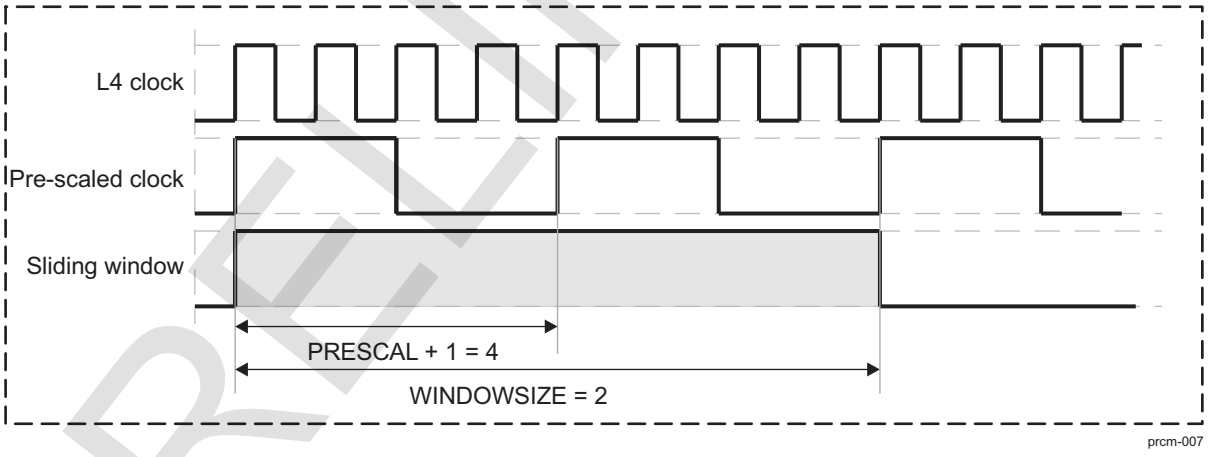
Prescaled clock frequency = L4 interface clock frequency/(PRESCAL + 1)

The size of the sliding window is fixed by setting the CM_Clock domain_DYNAMICDEP[27:24] WINDOWSIZE bit field. It is given as:

Sliding window duration = WINDOWSIZE Period of Prescaled clock cycle

Figure 3-7 presents an example of the sliding window duration equal to eight clock cycles of L4 clock when PRESCAL is set to 3 and WINDOWSIZE is set to 2.

Figure 3-7. Sliding window for Dynamic Dependency



This dynamic dependency is also referred to as the autosleep/autowake-up feature.

NOTE:

- The static dependency between two clock domains can be configured by software (PRCM module registers) or hardwired in the PRCM module.
- The dynamic dependency between two clock domains is hardwired in the PRCM module.

A dynamic dependency is said to be active when:

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- At least one master module or a slave interconnect module from clock domain A to domain B is active (that is, the master module is not in STANDBY state and/or the interconnect slave module is not in IDLE state), and
- There has been one or more transaction on the interconnect within the sliding window duration.

It is said to be inactive otherwise.

The dynamic dependency between a source clock domain and a destination clock domain can be read in the PRCM module from the corresponding read-only CM_Source Clock domain_DYNAMICDEP[x] Destination Clock domain_DYNDEP bit.

3.1.1.1.7.3 Wake-Up Dependency

A wake-up dependency is a dependency between the clock domain of a module that owns one or several wake-up signals, toward the clock domain of another module needed to service the associated wake-up event. As a result of this dependency, the wake-up event to a module not only activates its clock domain, but also the clock domain of the servicing module.

NOTE: The wake-up signal that triggers a wake-up dependency stays active as long as the source of the event is not serviced, to ensure that clock domain of the servicing module remains active.

Wake-up dependencies allow acceleration of the wake-up transition of multiple domains needed to service the wake-up event by initiating their transition in parallel. The static and dynamic dependencies can allow the wake-up of related domains but the complete wake-up transition of all the associated domains is slower because of the sequential cascading of their wake-up transitions.

In the device, the source event of the wake-up signal to a slave module can be one of following types:

- Interrupt request to microprocessor (MPU) or digital signal processor (DSP) interrupt controller (INTC)
- DMA request to a DMA controller

Upon wakeup by these types of wake-up events, and for as long as they remain asserted, the PRCM module takes the following actions:

- The power domain of the servicing module (for example, MPU, DSP, or DMA) is forced to POWER ON state and the clock domain becomes active.
- The power domain of the device interconnect between servicing module and the module originator of the wake-up event is forced to POWER ON state and the clock domain becomes active.
- The power domain of the slave module originator of the wake-up event is forced to POWER ON state and the clock domain becomes active.
- The slave module originator of the wake-up event is switched from IDLE to ACTIVE state.

On assertion of a wake-up event of a standalone master module, and as long as it remains asserted, the PRCM module takes the following action:

- The power domain of the master module originator of the wake-up event is forced to POWER ON state and the clock domain becomes active

NOTE: For slave modules, the static and dynamic dependencies of a clock domain are not impacted by its wake-up dependency settings. For master modules, the static dependencies are not impacted.

Hence, in addition to the activation of the clock domains identified in Section 3.1.1.1.7.3 above, all clock domains associated by static dependencies are also activated.

However, the clock domains associated with the waking up clock domain through dynamic dependencies are only activated if a transaction is initiated to these clock domains.

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For each wake-up signal coming from a slave module, the type of the corresponding event can be configured in the PM_Power domain_Originator Module _WKDEP[x] WKUPDEP_Originator Module_Servicing Module bit of the PRCM module. Where Power domain is the name of the power domain of the originator module of the wake-up event identified as Originator Module. Servicing Module refers to the module servicing the wake-up event.

NOTE: When only one event type is associated with the wake-up signal of a slave module, the WKUPDEP wake-up dependency for the module clock domain is not be configurable and may be hardwired in the PRCM module.

In case of the master modules, there is no configurable wake-up dependency. Their power domain is switched on and their clock domain is activated by the PRCM module when they assert their wake-up signal.

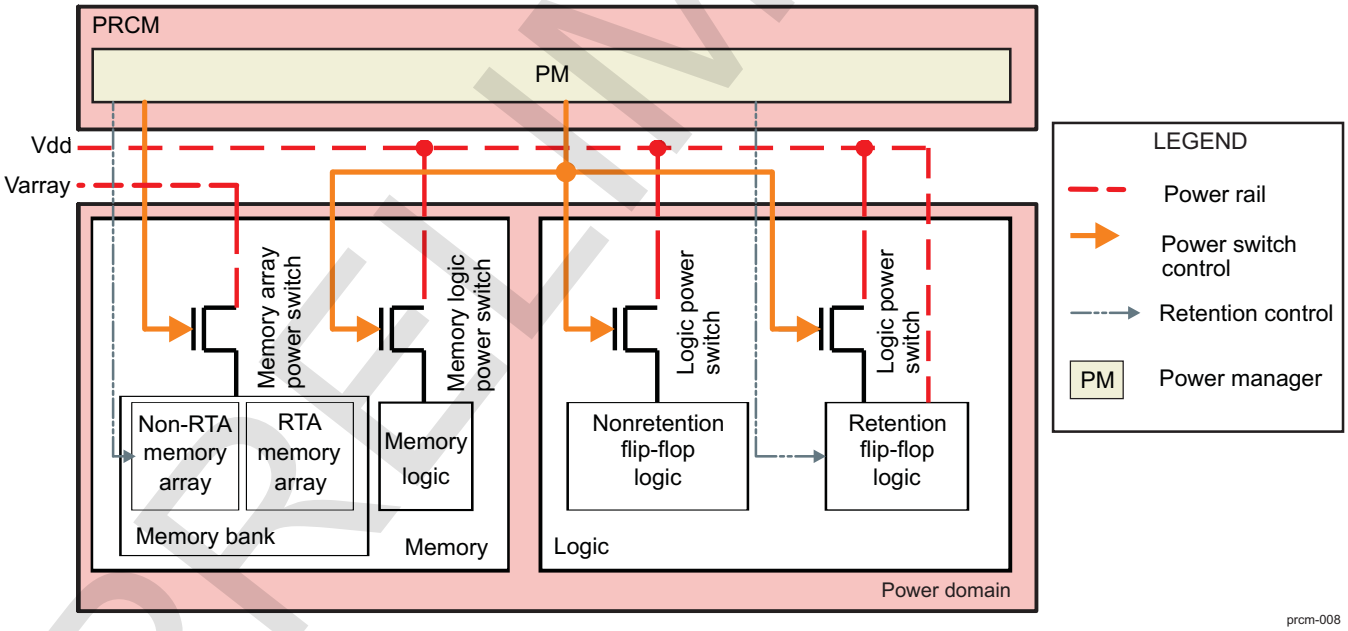
3.1.1.2 Power Management

The PRCM module manages the switching on and off of the power supply to the device modules. The power to the modules can be switched off when they are not in use to minimize device power consumption. Independent power control of sections of the device allow the PRCM module to turn on and off specific sections of the device without affecting the others.

3.1.1.2.1 Power Domain

A power domain is a section (that is, a group of modules) of the device with independent and dedicated power manager (see Figure 3-8). A power domain can be turned on and off without affecting the other parts of the device.

Figure 3-8. Generic Power Domain



To minimize device power consumption, the modules are grouped into power domains. A power domain can be split into some logic area and some memory area.

The memory area contains two entities:

- Memory bank: The memory bank is composed of memory arrays. It is powered by a dedicated voltage rail and an associated power switch (for example, Varray and memory array power switches). The memory array within the memory bank can be of RTA (retention-till-access), see Section 3.1.1.2.3, *Module Logic and Memory Context* or non-RTA type.

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- Memory logic: The memory logic is powered by the same voltage source as the logic area of the power domain, but has its dedicated power switch (for example, Vdd and memory logic power switches).

The logic area in the power domain can also be split between retention flip-flops (RFFs) or nonretention flip-flops (DFFs).

Table 3-15 lists the possible states and substates of the logic area in a power domain.

Table 3-15. States of a Logic Area in a Power Domain

State	Substate	Description
ON	ON-ACTIVE	Logic is fully powered and at least one enclosed clock domain is active.
	ON-INACTIVE	Logic is fully powered and all enclosed clock domains are idled.
RETENTION	CSWR (close switch retention)	Logic is fully powered and all enclosed clock domains are idled.
	OSWR (open switch retention)	Logic is powered down, except the RFF-based logic retains its value. The DFF is lost and reset. Vdd can be lowered to its retention voltage level if all power domains associated are in this or lower states.
OFF		Logic power switches are off. All the logic (DFF and RFF) is lost except for the context, which has been saved in the scratchpad memory of an always-on power domain. Vdd can be set to 0 V if all associated power domains are in this state.

NOTE: A power domain that does not have RFF logic may still support the open-switch retention power state. In this case, all its logic context is lost, yet its memory area context may remain valid if programmed to retention mode (see Table 3-16 and Table 3-19).

The RETENTION state is useful for quick switching to low-power idle mode (in which the domain clocks are gated and the domain voltage is less than the on-voltage level) without losing the context, and then quickly switching back to ON-ACTIVE state when necessary. In RETENTION state power consumption is less than in On Power state.

Similarly, in RETENTION state the CSWR state has the advantage of faster turn-on times over the OSWR state, because in the latter case the entire context is maintained. However, CSWR state has the disadvantage of higher leakage currents over OSWR state.

The behavior of the memory array power switch and memory logic power switch can be selected through software settings in the PRCM module, or can be hardwired. Once the behavior is selected, the PRCM module hardware automatically handles these elements to ensure correct power transition sequencing between the power domain states.

Software can also initiate the memory array power state changes when the associated power domain is in On Power state. This allows the memory array to be turned off and on as needed.

The memory area can be configured to any of the power states identified in Table 3-16.

Table 3-16. States of a Memory Area in a Power Domain

State	Description
ON	The memory array is powered and fully functional. Additionally, the RTA feature may put part or all of the memory array automatically into retention when not accessed, if this feature exists and is enabled on a given memory instance.
RETENTION	The memory array is fully powered, but memory is not accessible. The array can be put into retention either through applicable direct retention control signal, or automatically if the RTA feature exists and is enabled on a given memory instance. Data in memory are always retained.
OFF	The memory array is powered down. Data in memory are lost.

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3.1.1.2.2 Module Logic and Memory Context

In case of a power state transition in the logic area or the memory area, the context of the module may no longer be valid. This can also be the case when the domain resets are asserted by the device. A specific RM_Clock Domain Name_Module Name_CONTEXT register provides the status of the device logic and memory context.

- The module logic context is made of simple flip-flops (DFFs) if module has no logic RFFs.
- If module has logic retention (full or partial), it is assumed that the context is made only of RFFs.

NOTE: The display subsystem (DSS) is an exception where the status of DFF and RFF context is presented, because only HMDI keys are retained, while most of the DSS is nonretained.

These context status bits must be cleared by software.

3.1.1.2.3 Retention-Till-Access Memory Feature

Most high-density memories within the device support the RTA feature. It consists of automatically putting part of or the entire memory array into retention when no access is made to the corresponding locations. This is managed within the memory bank by hardware and is completely transparent to the user software. As a consequence, RTA memories do not have any retention mode control signal coming from the PRCM module.

The RTA feature is controlled (enabled and disabled) from:

- eFuse bits configuration in the system control module, automatically loaded to the PRCM module.
- Software-controlled override capability through a bit field per voltage domain in the PRCM module (that is, PRM_LDO_SRAM_Memory Voltage Domain_SETUP[0] DISABLE_RTA_EXPORT).
- Hardware override capability controlled by the PRCM module through control of embedded static random-access memory (SRAM) low-dropout linear regulator (LDO) controller.

3.1.1.2.4 Power Domain Management

The power manager associated with each power domain is assigned the task of managing the domain power transitions. It ensures that all hardware conditions are satisfied before it can initiate a power domain transition from a source to a target power state (for example, from ON-ACTIVE state to OSWR RETENTION state).

The hardware condition for power domain transition from ON-ACTIVE to any other transition state is:

- All clock domain managers in the power domain are in INACTIVE state: All modules in the domain are in IDLE or STANDBY state, and there is no constraining dependency (static, dynamic, or wake-up dependency) between the clock domains blocking the clock domain sleep transition.

Figure 3-9 shows all possible power domain state transitions.

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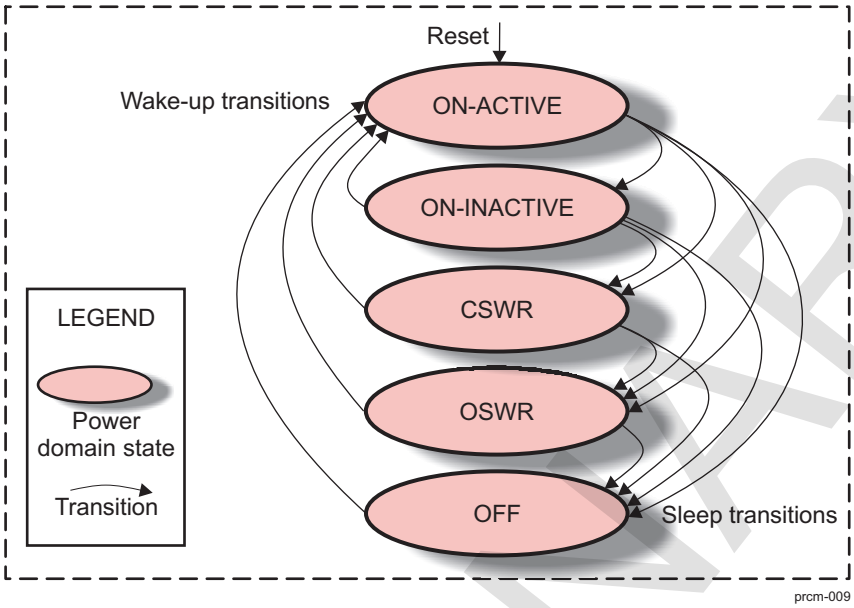
Figure 3-9. Power Domain Transitions



Successive power-down transitions can be performed by lowering the power state from ON-ACTIVE to ON-INACTIVE to RETENTION, and then to OFF, as long as the hardware condition is satisfied.

However, the power domain wake-up transition from any low-power state (ON-INACTIVE, CSWR, OSWR, or OFF) to ON-ACTIVE is always direct. For example, user software cannot request a power domain transition from OSWR state to CSWR state, but only to ON-ACTIVE state.

The power domain manager initiates a power domain wake-up transition when the conditions listed in Table 3-17 are satisfied.

Table 3-17. Power Domain Wake-Up Conditions

Relation		Condition
AND		Voltage domain is on.
	OR	There is at least a wake-up condition for one enclosed functional clock domain.
		There is a request for clock generation or distribution enclosed in the power domain.
		There is a PRCM module service request (applicable only to power domains, including PRCM module logic).

The power domain manager initiates a domain sleep transition when the conditions listed in Table 3-18 are satisfied.

Table 3-18. Power Domain Sleep Conditions

Relation	Condition
AND	All functional clock domains enclosed in the power domain are idled.
	All clock generation or distribution enclosed in the power domain is quiet, and corresponding input clocks are gated. For example, DPLL, if present, must be in stop mode.
	There is no PRCM module service request (applicable only to power domains, including PRCM module logic).

Table 3-19 lists the PRCM module power domain control and status features.

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Table 3-19. Power Domain Control and Status Registers

Register/Bit Field	Type	Description
PM_Power domain_PWRSTCTRL[1:0] POWERSTATE	Control	Selects the target power state of the power domain among OFF, ON-ACTIVE, ON-INACTIVE, and RETENTION.
PM_Power domain_PWRSTCTRL[x] LOWPOWERSTATECHANGE	Control	Power state change request when domain has already performed a sleep transition. Allows going into deeper LOW-POWER state without waking up the power domain.
PM_Power domain_PWRSTCTRL[2] LOGICRETSTATE	Control	Selects whether the Power domain logic is in CSWR or OSWR RETENTION state when the domain transitions to RETENTION state.
PM_Power domain_PWRSTCTRL[x] memory bank_RETSTATE	Control	Selects whether the memory bank in the power domain is in ON or RETENTION state when the power domain is in RETENTION state. The memory bank can not be in ON state when the power domain is in RETENTION state.
PM_Power domain_PWRSTCTRL[x] memory bank_ONSTATE	Control	Selects whether the memory bank is in ON, RETENTION, or OFF state when the power domain is in ON state.
PM_Power domain_PWRSTST[1:0] POWERSTATEST	Status	Identifies the current state of the power domain. It can be OFF, RETENTION, ON-INACTIVE, or ON-ACTIVE.
PM_Power domain_PWRSTST[2] LOGICSTATEST	Status	Identifies the current state of the logic area in the power domain. It can be OFF or ON.
PM_Power domain_PWRSTST[20] INTRANSITION	Status	Identifies whether a power domain power state transition is in progress or there is no ongoing transition.
PM_Power domain_PWRSTST[x] memory bank_STATEST	Status	Identifies the current power state of the memory bank in the power domain. It can be OFF, RETENTION, or ON. For memory with RTA feature, the ON and RETENTION memory states are equivalent.

3.1.1.3 Voltage Management

The PRCM module controls the voltage scaling (that is, switching the voltage in discrete steps or in a continuum within a range of possible values) of the power sources of the device. This allows control of the device power consumption according to the performance criteria defined. Higher performance is ensured with higher voltage and clock frequencies (and hence higher power consumption), while lower performance can be supported with lowered power consumption by reducing or completely gating the power supply to specific areas of the device and gating the associated clocks.

3.1.1.3.1 Voltage Domain

A voltage domain is a section of the device supplied by a dedicated voltage source (that is, an internal LDO or external switch mode power supply [SMPS]). A voltage domain may or may not be controlled by the PRCM module. When a voltage domain is controlled by the PRCM module, a dedicated voltage manager is associated. The voltage manager allows regulation of the voltage level of the source for the voltage domain, independently of other voltage domains of the device.

The voltage managers in the PRCM module can be of two types:

- Dynamically configurable by software to scale the domain voltage level to specific values within the device operational voltage range. This is called adaptive voltage scaling (AVS).
- Hardware controlled to automatically switch the domain voltage levels according to the associated hardware conditions.

Figure 3-10 shows a voltage domain.

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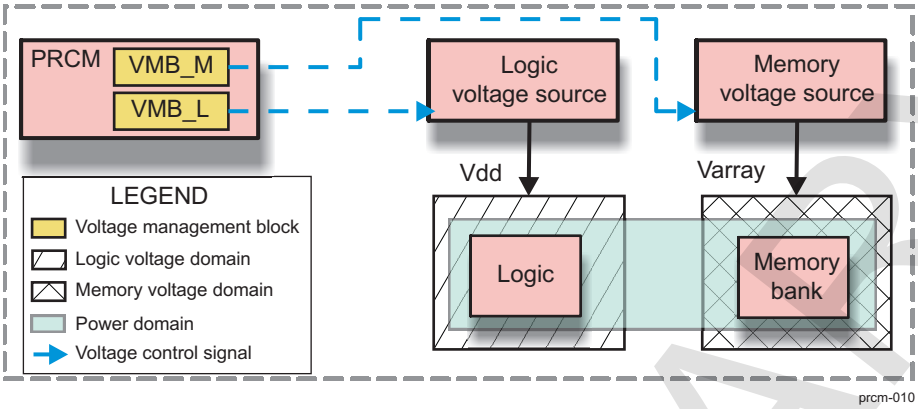
Figure 3-10. Generic Voltage Domain



By partitioning the device into independent voltage domains, different operating voltages can be assigned to the different sections of the device (that is, group of modules or memory banks). The independent voltage control allows voltage scaling of device subsections to ensure that each module or memory bank operates at the optimized operating voltage level based on the application performance requirements. When all modules within a voltage domain are idle (that is, have no ongoing transaction), the domain voltage can be lowered to reduce power consumption and then switched back to normal operating voltage level when a wake-up event is received by one of the modules of the voltage domain. Similarly, when a memory bank is not in use, it may be switched to retention or off voltage levels to ensure power savings.

Table 3-20 describes the different states of the logic voltage domain.

Table 3-20. States of Logic Voltage Domain

State	Description
ON	The voltage regulator source for the voltage domain is active and operating in its normal voltage range for the current operating performance point (OPP) and can deliver up to the maximum load current defined for the current OPP.
SLEEP	The voltage regulator source is operating in its normal voltage range but it can only deliver a limited load current (no logic activity on this voltage domain). In sleep mode, regulator power consumption is reduced.
RETENTION	The voltage regulator source is operating at retention voltage level. It delivers the minimal load current required to maintain the voltage domain logic context.
OFF	The voltage regulator source is inactive and its output voltage is 0 volts. No supply current is provided in this mode.

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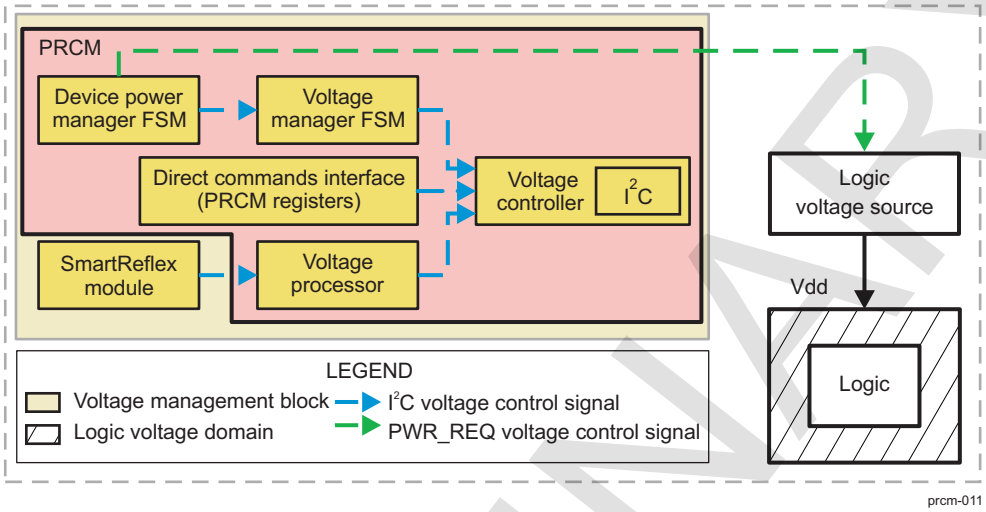
3.1.1.3.2 Voltage Domain Management

Figure 3-11 highlights the different voltage control paths available within a generic logic voltage management block to control the voltage supply to the device logic voltage domains.

Figure 3-11. Generic Logic Voltage Management



3.1.1.3.2.1 Logic Voltage PWR_REQ Voltage Control

A PWR_REQ signal is deasserted when the device enters the OFF state. The external power integrated circuit (IC) can use it to properly manage turn-off or turn-on of the logic voltage source.

3.1.1.3.2.2 Logic Voltage I^2C Voltage Control

The PRCM module allows three voltage control paths to a dedicated inter-integrated circuit (I^2C™) interface for the logic voltage domains managed by it.

1. The PRCM module hardware-managed voltage changes from device power manager voltage finite state-machine (FSM) through voltage manager FSM based on hardware conditions. It sends the voltage commands when the device enters in RETENTION or OFF state and upon device wakeup.
2. Direct control by user software through the PRCM module registers for voltage scaling.
3. Adaptive voltage scaling (see Section 3.1.1.3.3, *AVS Overview*) with SmartReflex™ voltage control commands through the voltage processor.

NOTE: An I^2C host module (not controlled by the PRCM module) can be used to program the external power IC. Because this procedure completely bypasses PRCM module, see Section 23.1 *I^2C*.

Figure 3-12 highlights the voltage control path available within a generic memory voltage management block to control the voltage supply to the device memory voltage domains.

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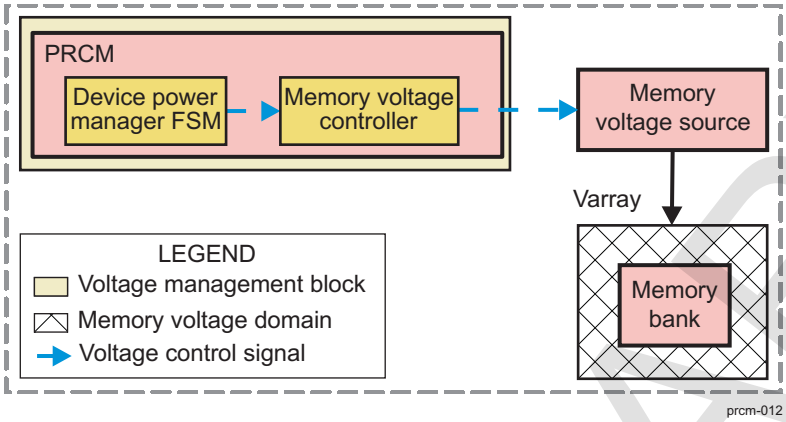
Figure 3-12. Generic Memory Voltage Management



The PRCM hardware supports automatic scaling down of the memory array supply whenever they transition to RETENTION or OFF power state. The device power manager FSM manages the voltage scaling of memory voltage domains through memory voltage controller (or LDO).

3.1.1.3.3 AVS Overview

SmartReflex is a power-management technique used for controlling the operating voltage of a device to reduce its active power consumption.

With SmartReflex, the power-supply voltage is adapted to the silicon performance in two ways:

- Statically adapted to the manufacturing process of a given device
- Dynamically adapted to the temperature-induced current performance of the device

SmartReflex achieves optimal performance/power trade-off for all devices across the technology process spectrum and across temperature variations.

The static correction of the device voltage level (see Figure 3-13) is based on the desired performance level and silicon performance characteristics of the device. Due to process dispersion, each die has its specific silicon performance. The range of the process distribution defines the weak devices (low-performance silicon) and the strong devices (high-performance silicon).

A weak device is a device with the lowest performance tolerated for a process distribution; that is, at the typical voltage, the inherent maximum frequency is the lowest frequency of the chip distribution. Considered as the worst case, weak devices are used to constrain the target frequency of all the chips (OPP definition).

A strong device is a device with the highest performance tolerated for a process distribution. The inherent maximum frequency at the typical voltage is greater than the targeted frequency.

Figure 3-13 identifies the fact that, with SmartReflex voltage-control architecture, it is possible to compensate for the device silicon characteristics and obtain optimal performance characteristics. Based on the device characteristics, the device voltage level can be adjusted for specific performance level.

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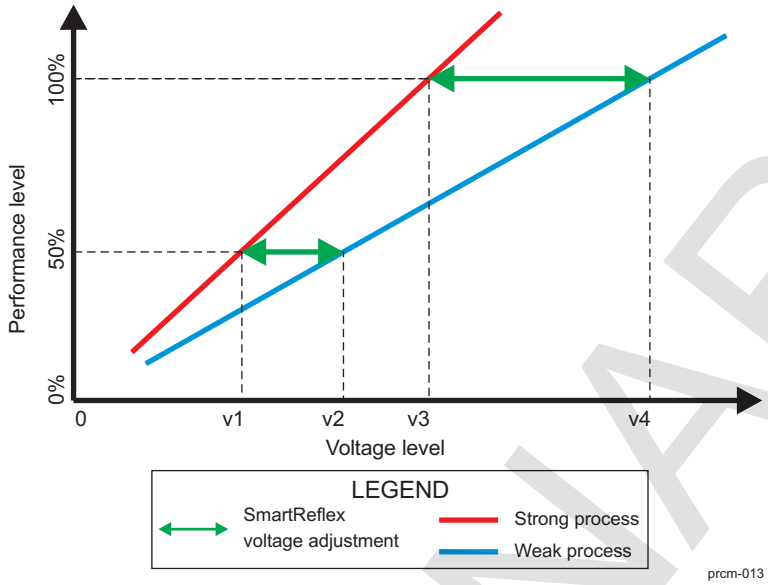
Figure 3-13. SmartReflex Static Voltage Adjustment

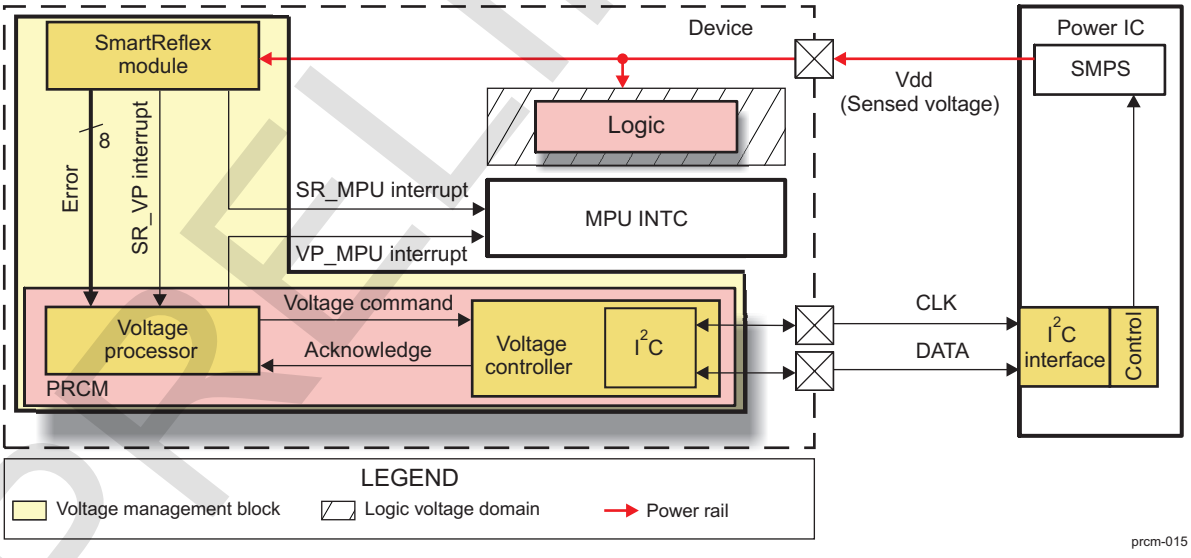


The dynamic correction of the device voltage is based on the real-time comparison of predefined performance points to the on-chip measured performance level. The device voltage level is raised or lowered to compensate for temperature-induced performance variations.

Without SmartReflex, the voltage variation is around the nominal voltage level and not controlled through any active dynamic compensation. This leads to power waste.

Figure 3-14 is a functional overview of the SmartReflex voltage-control architecture of the device connected to an external power IC.

Figure 3-14. SmartReflex Voltage Control Functional Overview



SmartReflex voltage control consists of the following modules:

- SmartReflex
- MPU INTC
- Voltage processor
- Voltage controller

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- I²C interface
- SMPS

The SmartReflex module senses input voltage (Vdd) and generates an error value that identifies the difference between the desired optimal voltage and the actual value of the SMPS. This error value is set in an internal register (for software read, if necessary) and is also passed to the voltage processor.

The voltage processor converts the error value to a voltage command that defines the change in the output voltage of the SMPS required to bring it to the desired voltage level.

The voltage command is sent to the voltage controller, which passes it to the power IC through the dedicated I²C interface. The power IC then adjusts the output voltage of the SMPS according to the command.

In this way, the SmartReflex module dynamically adjusts the SMPS voltage to compensate for voltage variations.

The device supports two operational modes for SmartReflex voltage control:

- Class-2 or software-controlled
- Class-3 or hardware-controlled

3.1.1.3.3.1 Class-2 SmartReflex Voltage Control

In software voltage control, the SmartReflex module interrupts the MPU when the voltage level crosses the defined voltage limits (minimum/maximum). The MPU reads the error value and determines the new voltage command to be sent to the SMPS to return the voltage to within the limits. The new voltage command is sent to the voltage controller, which passes the command to the SMPS and acknowledges its reception.

In class-2 control, the voltage processor is bypassed.

3.1.1.3.3.2 Class-3 SmartReflex Voltage Control

In hardware voltage control, the SmartReflex module interrupts the voltage processor when the voltage level crosses the defined voltage limits (minimum/maximum). The voltage processor reads the error value and determines the new voltage command to be sent to the SMPS to return the voltage to within the limits. The new voltage command is sent to the voltage controller, which passes the command to the SMPS and acknowledges its reception.

In class-3 mode, the software does not intervene in voltage control; the entire loop is handled by the hardware modules.

3.1.2 Power-Management Techniques

The following sections describe the state-of-the-art power-management techniques supported by the device.

NOTE: The values in Figure 3-15 through Figure 3-17, which show power-management techniques, are hypothetical. They do not represent valid test results on the device.

3.1.2.1 Standby Leakage Management

Standby leakage management (SLM) is a power-management technique that reduces standby power consumption by reducing power leakage.

With SLM, the device switches into low-power system modes automatically or in response to user requests during system standby (that is, in situations when no application is started and system activity is negligible or limited).

When applying SLM, the system remains in the lowest static power mode compatible with the system response time requirement.

This technique trades static power consumption for wake-up latency.

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3.1.2.2 Dynamic Voltage and Frequency Scaling

Dynamic voltage and frequency scaling (DVFS) consists of minimizing the idle time of the system. The DVFS technique uses dynamic selection of the optimal operating frequency and voltage to allow a task to be performed in the required length of time. This reduces the active power consumption (power consumed while executing a task) of the device while still meeting task requirements.

NOTE: The values in Figure 3-15 are hypothetical. They are meant only to clarify the concept and do not represent valid test results on the device.

Figure 3-15. Comparison of Energy Consumed With/Without DVFS

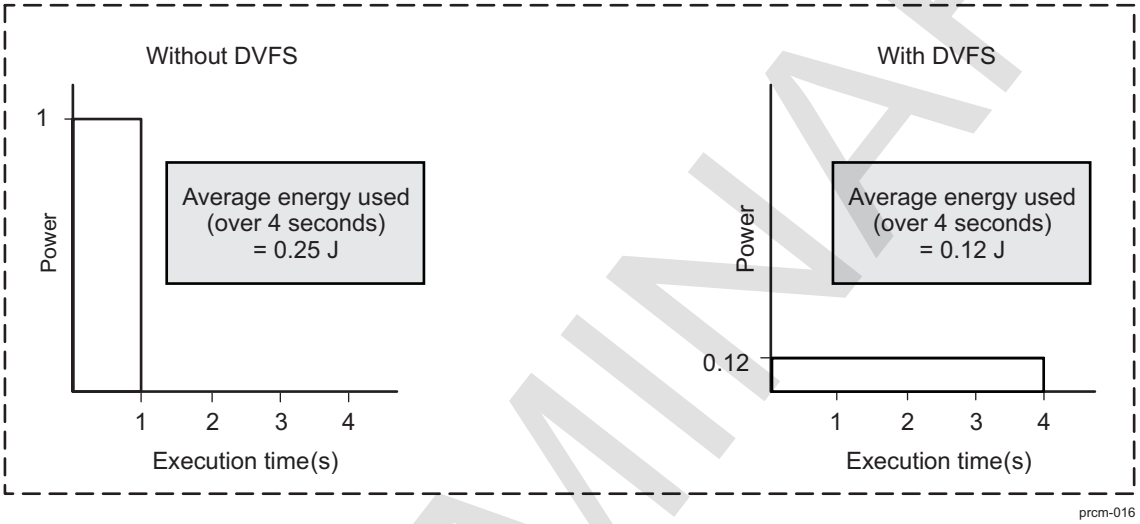

Figure 3-15 shows the DVFS technique by comparing a process executed at maximum frequency and operating voltage without applying DVFS to the same process executed at optimal frequency and voltage using DVFS, based on the task requirements. If a task that must terminate in 4 seconds is performed at maximum operating frequency (left side of the figure), it terminates in 1 second, and the remaining 3 seconds are spent in idle mode. With DVFS (right side of the figure), the operating frequency is reduced to an optimal level; the task takes the full 4 seconds to complete, but power consumption is reduced. In addition, the voltage can be reduced further to save power so the dynamic and leakage power consumption are reduced.

DVFS requires control over the clock frequency and the operating voltage of the device elements. By intelligently switching the individual elements of the device to their OPPs, the power consumption of the device for a given task can be minimized.

For practical reasons related to device making (flow, tools), DVFS can be used only for a few discrete steps, not over a continuum of voltage and frequency values. Each step, or OPP, is composed of a voltage (V) and frequency (F) pair. For an OPP, the frequency corresponds to the maximum frequency allowed at a voltage, or reciprocally; the voltage corresponds to the minimum voltage allowed for a frequency.

When applying DVFS, a processor or system always runs at the lowest OPP that meets the performance requirement at a given time. The user determines the optimal OPP for a given task and then switches to that OPP to save power.

3.1.2.3 Dynamic Power Switching

Like DVFS, dynamic power switching (DPS) is a power-management technique aimed at reducing active power consumption of a device. However, whereas DVFS reduces the dynamic and leakage power consumption, DPS reduces only leakage power consumption, at the expense of a slight overhead in dynamic power consumption.

With DPS, the system switches dynamically between high- and low-consumption system power modes

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during system active time. When DPS is applied, a processor or system runs at the highest OPP (maximum frequency and voltage) to complete its tasks quickly, followed by an automatic switch to a low-power mode, for minimum power consumption. DPS is useful when a real-time application is waiting for an event. The system can switch into a low-power system mode if the wake-up latency conditions allow it.

This technique consists of maximizing the idle period of the system to reduce its power consumption.

NOTE: The values in Figure 3-16 are hypothetical. They are meant to clarify the concept only and do not represent valid test results on the device.

Figure 3-16. Comparison of Energy Consumed With/Without DPS

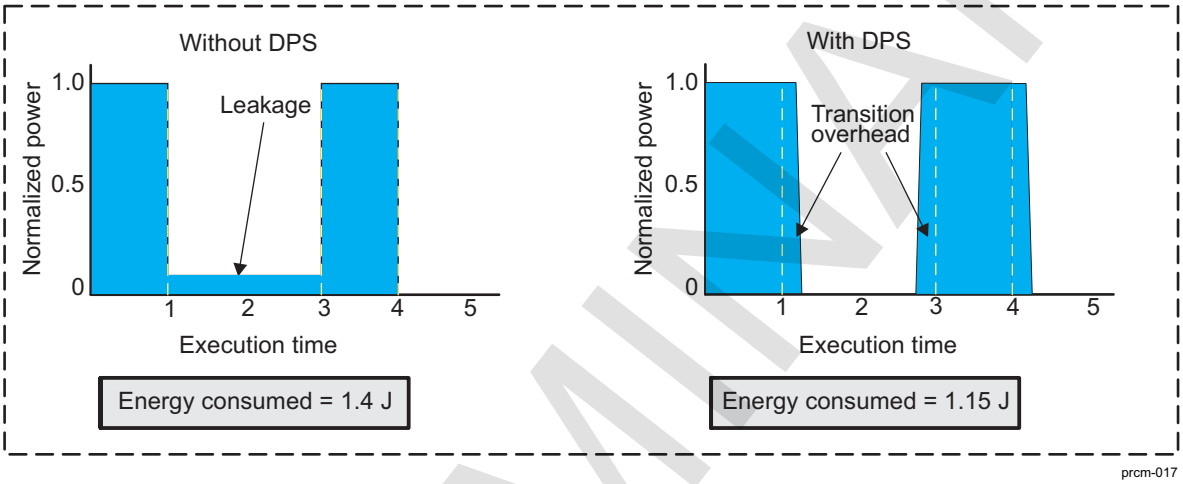

Figure 3-16 compares the behavior of power consumption for the same device operation without DPS (left side of the figure) and with DPS (right side of the figure). When operating without DPS, the device has a constant leakage current in idle mode. By using DPS, the system reduces the leakage current to zero. However, the transitions between system power modes may require storing the information before entering a low-power inactive state and restoring the information after a wake-up event (see Figure 3-16). This results in additional dynamic power consumption, referred to as the transition overhead (see Figure 3-16). Transition overhead must be considered for a DPS operation.

For efficient deployment of DPS techniques, it is necessary to predict dynamically the performance requirement of the applications running on the processor. The DPS controller must account for the overhead of wake-up latencies related to domain switching and ensure that they do not significantly affect the performance of the device. Even with transition overhead, however, the user can identify an optimal idle-time limit, after which the DPS is useful for dynamic power-saving.

3.1.2.4 Adaptive Voltage Scaling

SmartReflex-based AVS is a power-management technique for automatic control of the operating voltages of the device to reduce active power consumption.

With SmartReflex, power-supply voltage is adapted to silicon performance, either statically (based on performance points predefined in the manufacturing process of a given device) or dynamically (based on the temperature-induced real-time performance of the device). A comparison of these predefined performance points to the real-time on-chip measured performance determines whether to raise or lower the power-supply voltage.

AVS achieves the optimal performance/power trade-off for all devices across the technology process spectrum and across temperature variation. The device voltage is automatically adapted to maintain performance of the device. This ensures optimal power consumption for a given OPP.

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With AVS, the frequency steps are identified and the voltage is adapted according to the silicon performance of the device. In this case, instead of a voltage step for each frequency step, there is a corresponding range of voltages. The range depends on the fabrication process of the device and its real-time operating state (temperature) at a given frequency.

3.1.2.5 Adaptive Body Bias

The device implements transistor body bias techniques for the following situation:

- Forward body-bias (FBB) for operating clock frequency boost for operation at higher OPPs.

Adaptive body bias (ABB) is based on the process corner and the current OPP. This is configured in the efuse at the device characterization and is not continuously updated. A dedicated LDO, that is, VBBLDO, is used to produce the voltage bias.

3.1.2.6 Combining Power-Management Techniques

The power-management techniques previously described have specific features and are most effective when used under the specific operating conditions of the device. Hence, the best active power savings are obtained by combining the DVFS, DPS, SLM, and AVS techniques. For a given operating state, one or more of the power-saving techniques can be applied to ensure optimal operation with maximum power saving.

AVS can be used at boot time to adapt the voltage to device process characteristics (strong/weak) and then used continuously to compensate temperature variations. AVS can also ensure maximum available application performance of the device at a given OPP.

When medium application performance is required, or when application performance requirements vary, DVFS can be applied. The voltage and frequency can be scaled to match the closest OPP that meets the performance requirement.

When application performance requirements fall between two OPPs, or when a low application performance is required that is below the lowest performance OPP, DPS can be applied to switch to low-power mode.

When combining DVFS and DPS, the operating frequency must not be scaled to match the performance requirement without scaling the voltage. Lower operating frequency increases task completion time and reduces idle time. This prevents DPS or reduces its efficiency (DPS becomes more effective as idle time increases). Unless DPS cannot be applied for other reasons, for a given operating point of DVFS the operating frequency must always be set to the maximum allowed at a given voltage. This ensures optimal process completion time and application of DPS.

If DPS cannot be applied in a given context, scaling the frequency while keeping the voltage constant does not save energy; it does, however, reduce peak power consumption. This can have a positive effect on temperature dissipation and battery life.

SLM must be used when no applications are running and performance requirement drops to zero.

NOTE: The OPPs shown in Figure 3-17 are only for indication and clarity of text. They do not correspond to validated OPPs of the device.

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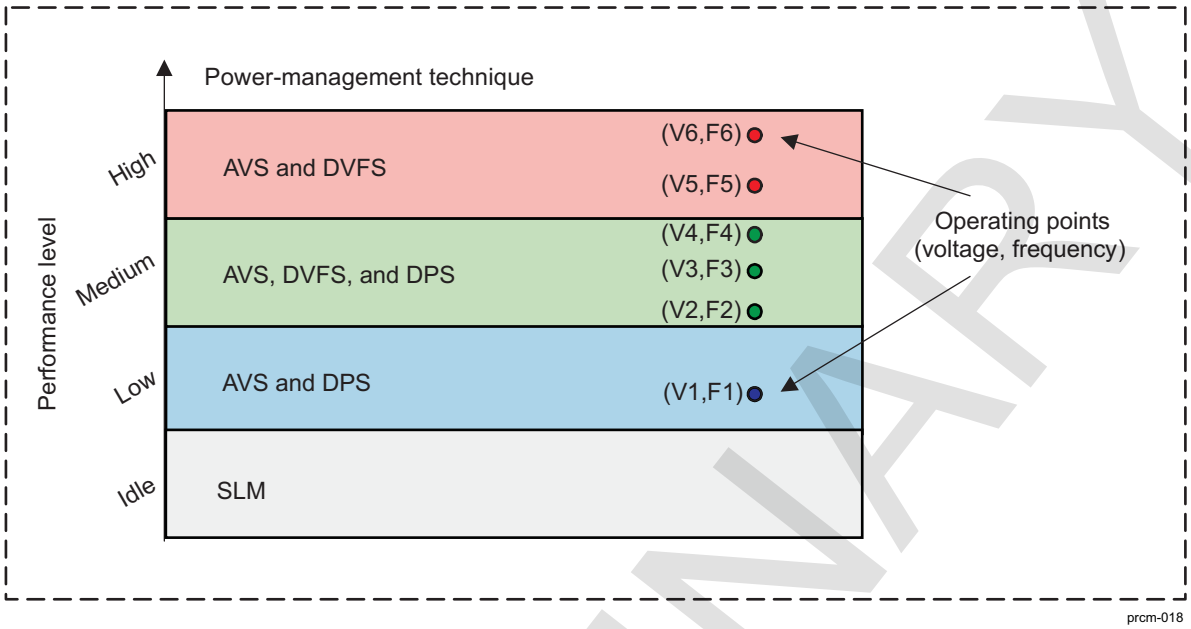
Figure 3-17. Performance Level and Applied Power-Management Techniques



3.1.2.6.1 DPS Versus SLM

DPS and SLM are similar concepts: they consist of switching the system between high- and low-power consumption modes. However, their operating timescales differ, principally in the latency allowed for mode transitions.

DPS is generally used in an applicative context (tasks are started). Therefore, mode transitions are related to system performance requirements or the processor load. DPS transition latencies must be small (typically between 10 µs and 100 µs) compared to the time constraints or deadlines of the application so that they do not degrade application performance. DPS requires performance prediction to ensure that transition latencies do not deteriorate device performance to the point that real-time application deadlines are missed or the user experience degrades too much for an interactive application.

SLM is not used in an applicative context (no task started). Mode transitions are related more to system responsiveness, and the transition latencies must be small compared to user sensitivity so that they do not degrade the user experience. For SLM, transition latencies are typically 1 ms to 10 ms or more.

DPS and SLM also differ in the type of wake-up event used to exit low-power idle mode. For DPS, wake-up events are application-related (timer, DMA request, peripheral interrupt, etc.); for SLM, wake-up events are user-related (touch screen, key pressed, peripheral connections, etc.).

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3.2 PRCM Subsystem Overview

3.2.1 Introduction

The power-management framework of the device significantly reduces dynamic power consumption and static leakage current to extend the life of the battery in the end product. This framework incorporates support for state-of-the-art power-management techniques. It ensures optimal device operation with significantly reduced power consumption. The power-management framework (PMFW) of the device is split over following modules:

- SCRM: Handles system-level (with one or more devices) clock and reset distribution and management.
- PRCM: A logical module composed of following three physical submodules:
  - PRM: Handles device-level power and reset management. It also handles some clocks in the device. This module always remains on, unless no power is supplied to the device pads.
  - CM1: Handles device-level clock management 1. This module remains always on unless either the device is switched to off mode or no power is supplied to the device pads.
  - CM2: Handles device-level clock management 2. This module does not remain always on. It is switched to full-retention mode when its power domain (PD_CORE) is in RETENTION state. It is off when either the device is switched to off mode or no power is supplied to the device pads.
- SR_MPU, SR_IVA, and SR_CORE (SmartReflex): Handle AVS features

Together, these modules provide enhanced power-management features with the centralized control for the clock, reset, and power-management signals in the device.

The device supports the power-management techniques with the following features:

- Partitioning of the device into voltage, power, clock, and reset domains
- Domain isolation that allows any combination of domain on/off states
- Clock tree with selective clock-gating conditions
- Hardware-controlled reset sequencing management
- Power, reset, and clock control hardware mechanism to manage sleep and wake-up dependencies of power domains
- Support for hardware-controlled autogating of module clocks
- Memory retention capability for preserving memory contents in low-power sleep mode
- DVFS support for the processor and peripherals
- AVS support for the processor and peripherals, for real-time performance adjustments
- Support for low-power device off mode input/output (I/O) pad configuration for minimum power consumption when in OFF power state

The PMFW interfaces with all the components of the device for power, clock, and reset management through associated control signals. It integrates enhanced features to let the device adapt energy consumption dynamically according to changing application and performance requirements. The innovative hardware architecture allows a substantial reduction in leakage current.

The power-management modules are fully configurable through their level 4 (L4) interface ports.

Figure 3-18 is an overview of the power-management modules and their internal connections with a generic power domain.

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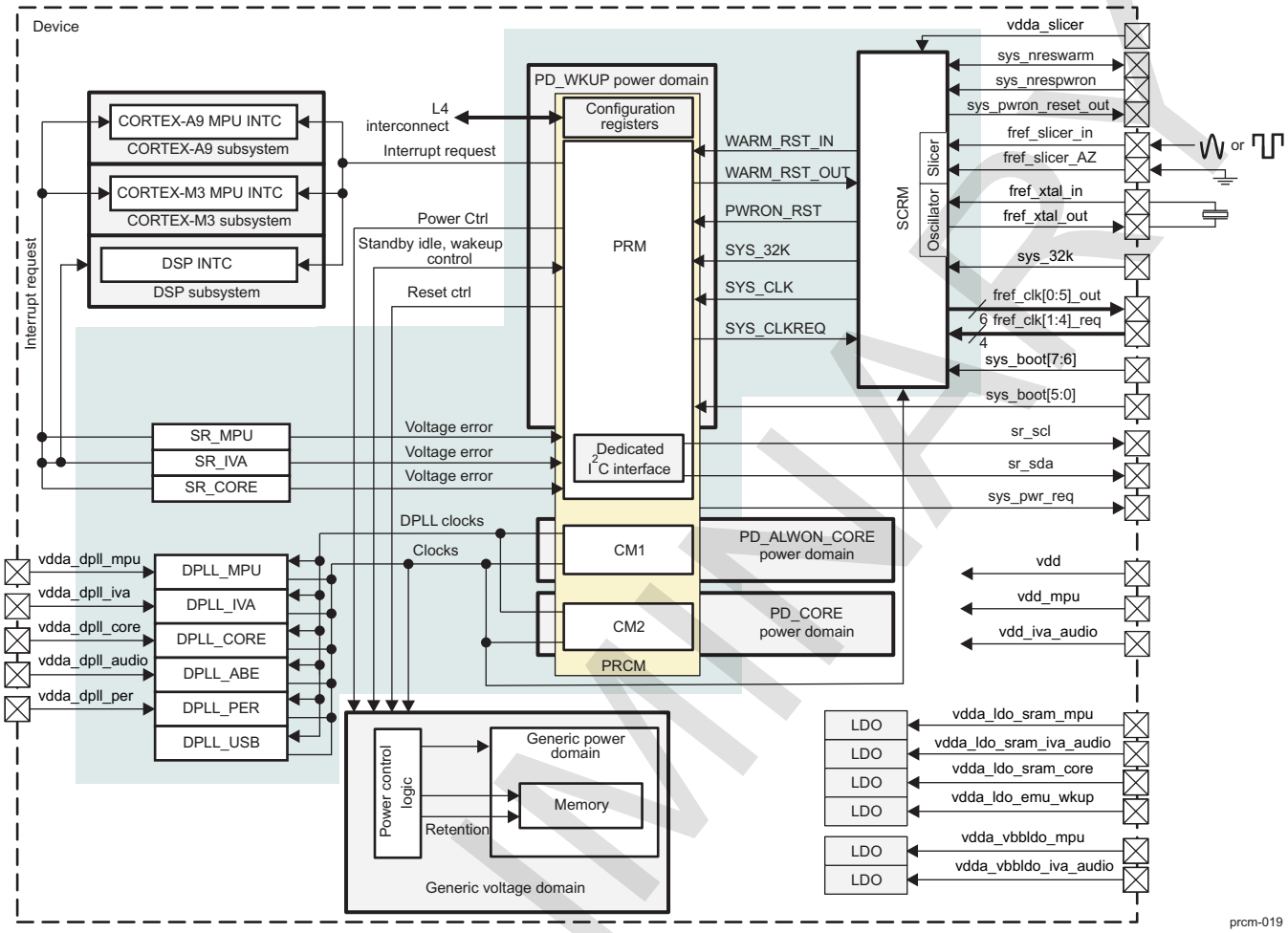
Figure 3-18. PMFW Overview



3.2.2 Power-Management Framework Features

The power-management modules have the following features:

- Manage independent power domains
- Control scalable logic voltage domains and selectable voltage modes for memory voltage domains
- Handle standby, idle, and wake-up procedures for the modules of the device
- Allow software and partial hardware control
- Monitor and handle wake-up events
- Control system clock and reset input sources
- Manage and distribute clocks and resets with high control granularity
- Handle power-up sequences
- Debug and emulation features
- Allow adaptive and dynamic voltage scaling feature through dedicated high-speed (HS) master I^2C interface
- Control of RFF of device modules to support DPS

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3.3 PRCM Subsystem Environment

The modules of the PMFW receive the external reset, clock, and power signals. See Figure 3-18.

NOTE: In the remainder of this chapter, power IC refers to a peripheral power source IC that is interfaced with the device. It receives power control commands (voltage scaling and power switching) from the device and provides the necessary voltages and reset signals.

The following sections describe the interfaces for external clock, reset, and power sources.

3.3.1 External Clock Signals

The SCRM module receives a low-frequency clock input, sys_32k, at 32-kHz frequency. It can receive high-frequency system clock through two possible inputs: fref_slicer_in or fref_xtal_in. The fref_slicer_in supplies the input clock to an on-chip slicer, while fref_xtal_in can be used as external crystal connection for internal high-frequency clock generation through an on-chip oscillator.

The SCRM can output six alternate clocks, fref_clk[0:5]_out. Output clocks 1 to 4 can be gated or enabled through associated clock request signals, fref_clk[1:4]_req.

Table 3-21 lists the external clock pins, signal names, their direction, associated modules, description, and reset values of the signals. If the signal is input to the device, the module is the destination module for the signal. If the signal is an output from the device, the module is the source module of the signal.

Table 3-21. External Clock Signals

Pin	Signal	I/O [1]	PMFW Module	Description	Module Reset Value
sys_32k	SYS_32K	I	SCRM	32-kHz clock input	Z
fref_clk_ioreq	SYSCLK_REQ	I/O	SCRM	System clock request. Input when pins sysboot6=0 and sysboot7=0. Otherwise output.	
fref_slicer_in	SLICER_IN	I	SCRM	System clock input to the slicer. It can be sinusoidal or square input signal. Otherwise, it may serve as alternate clock input (SYS_ALTCLK) to internal peripheral (for example, video DAC [VDAC]).[2]	Z
fref_slicer_AZ	SLICER_AZ	I	SCRM	Connected to ground at package level	Z
fref_xtal_in	XTAL_IN	I/O	SCRM	Oscillator drive input from crystal or alternate square clock input (SYS_ALTCLK). [2]	Unknown
fref_xtal_out	XTAL_OUT	O	SCRM	Oscillator drive output to crystal	Unknown
fref_clk[1:4]_req	CLK[1:4]_REQ	I	SCRM	Auxiliary clocks request	Z
fref_clk[0:5]_out	CLK[0:5]_OUT	O	SCRM	Auxiliary clocks outputs 0 to 5	0

(1) I = Input; O = Output; I/O = Input and Output (bidirectional)

(2) SYS_ALTCLK can be sourced by fref_slicer_in or fref_xtal_in based on SYSBOOT[7:6] settings. For more information, see Section 27.2.4.1, *Clock Source Selection*.

The auxiliary clocks are controlled by the configuration of the SCRM.AUXCLK <clock id> (where clock ID can be 0 to 5); for example, fref_clk1_out is controlled by the SCRM.AUXCLK0 register. It controls the following features:

- Select the clock off output polarity
- Source clock input:
  - System clock
  - Clock from DPLL_CORE
  - Clock from DPLL_PER
- Initiate software generated request
- Software-controlled clock gating
- Divide factor configuration between 1 and 16

The bidirectional fref_clk_ioreq pad can be used to manage the external system clock request and

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auxiliary clock request 0. With this implementation, it is not expected to externally drive the system clock request when the SOC is the clock requester. This implementation requires programming the SCRM accordingly, in case the SOC needs the external system clock request. The programming consists in setting AUXCLK0[9] DISABLECLK = 1 and AUXCLKREQ0[4:2] MAPPING = 0. Without these settings the SCRM would incorrectly interpret an external clock request as an auxiliary clock request 0.

The SCRM must enable the output buffer of this bidirectional pad as long as it needs to request the external clock source, and the output buffer must be put in high-Z when it no longer needs the system clock source.

3.3.2 External Boot Signals

PRM receives SYSBOOT[5:0] information by external pins sys_boot[5:0]. They are used to select interfaces or devices for the booting list. For more information, see Section 27.2.4.2, *Booting Device Order Selection*.

PRM receives SYSBOOT[7:6] information by external pins sys_boot[7:6]. It defines device source clock configuration. For more information, see Section 27.2.4.1, *Clock Source Selection*.

Table 3-22 lists the external boot pins, signal names, their direction, associated modules, description, and reset values of the signals. If the signal is input to the device, the module is the destination module for the signal. If the signal is an output from the device, the module is the source module of the signal.

Table 3-22. External Boot Signals

Pin	Signal	I/O [1]	PMFW Module	Description	Module Reset Value
sys_boot0	SYSBOOT0	I	PRM	System boot configuration pin 0	Z
sys_boot1	SYSBOOT1	I	PRM	System boot configuration pin 1	Z
sys_boot2	SYSBOOT2	I	PRM	System boot configuration pin 2	Z
sys_boot3	SYSBOOT3	I	PRM	System boot configuration pin 3	Z
sys_boot4	SYSBOOT4	I	PRM	System boot configuration pin 4	Z
sys_boot5	SYSBOOT5	I	PRM	System boot configuration pin 5	Z
sys_boot6	SYSBOOT6	I	SCRM	System boot configuration pin 6	Z
sys_boot7	SYSBOOT7	I	SCRM	System boot configuration pin 7	Z

(1) I = Input; O = Output; I/O = Input and Output (bidirectional)

3.3.3 External Reset Signals

The SCRM manages three reset signals:

- Power-on reset input on sys_nrespwron pin
- Power-on reset output on sys_pwron_reset_out pin
- Warm reset on sys_nreswarm pin

sys_nrespwron is asserted at device power up to reset the full logic in the device. The SCRM asserts the sys_pwron_reset_out signal to reset any associated external peripherals.

sys_nreswarm is a bidirectional pin. It can be activated at any time by an external device or an external reset push button action to cause a global warm reset event. The SCRM then holds sys_nreswarm to be driven out and maintained for a limited length of time at the boundary of the device. In this way, the device and its related peripherals are reset together.

The sys_reswarm and sys_nrespwron signals are active low. The sys_pwron_reset_out signal is also active low, and active means that the peripheral is under reset.

Table 3-23 lists the external reset pins, signal names, their direction, associated modules, description and reset values of the signals. If the signal is input to the device, the module is the destination module for the signal. If the signal is an output from the device, the module is the source module of the signal.

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Table 3-23. External Reset Signals

Pin	Signal	I/O [1]	PMFW Module	Description	Module Reset Value
sys_nreswarm	SYS_WARM_RST	I/O	SCRM	Warm reset input and output	Z
sys_nrespwron	SYS_PWRON_RST_IN	I	SCRM	Power-on reset input	Z
sys_pwron_reset_out	SYS_PWRON_RST_OUT	O	SCRM	Power-on reset to external peripherals	0

(1) I = Input; O = Output

3.3.4 External Power Control Signals

The power control signals let the PMFW modules control the device voltage levels.

The voltage level of the scalable voltage sources in the external power IC can be scaled by sending commands to the power IC through a PRCM module dedicated I^2C interface. The sr_scl and sr_sda are the clock and data pins, respectively, for this I^2C interface.

The PRCM module can also command the external power IC to switch the device voltages to off level when the device is in off mode and reactivate them when it wakes up. This is managed through the signal on the sys_pwr_req pin.

Table 3-24 lists the signals, I/Os, and module reset values for the signals to the external power IC.

Table 3-24. Power Control Interface

Pin	Signal	I/O [1]	PMFW Module	Description	Module Reset Value
sr_scl	SR_SCL	I/O	PRM	The SmartReflex dedicated I^2C interface clock line	1
sr_sda	SR_SDA	I/O	PRM	The SmartReflex dedicated I^2C interface data line	1
sys_pwr_req	PWR_REQ	O	PRM	Power request to external power IC, to exit device off mode.	Unknown

(1) I = Input; O = Output

3.3.5 External Voltage Inputs

Table 3-25 lists the external voltage sources related to the PRCM module.

NOTE: Table 3-25 highlights only the voltage sources that are either directly managed by the PRCM module or are received by parts of the PRCM module (for example, DPLLs, LDOs, etc.). It does not give the device voltage sources not directly associated with the PRCM module.

Table 3-25. Voltage Sources

Pin	Signal	Managed by the PRCM	Description
vdd	VDD_CORE_L	Yes (AVS and DVFS)	Supplies VDD_CORE_L logic voltage domain
vdd_mpu	VDD_MPU_L	Yes (AVS and DVFS)	Supplies VDD_MPU_L logic voltage domain
vdd_iva_audio	VDD_IVA_L	Yes (AVS and DVFS)	Supplies VDD_IVA_L logic voltage domain (that is, DSP and IVAHD)
vdda_dpll_core	VDDA_DPLL_CORE	No (fixed)	DPLL_CORE analog power supply
vdda_dpll_mpu	VDDA_DPLL_MPU	No (fixed)	DPLL_MPU analog power supply
vdda_dpll_iva	VDDA_DPLL_IVA	No (fixed)	DPLL_IVA analog power supply
vdda_dpll_per	VDDA_DPLL_PER	No (fixed)	DPLL_PER analog power supply
vdda_dpll_audio	VDDA_DPLL_AUDIO	No (fixed)	DPLL_AUDIO analog power supply

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Table 3-25. Voltage Sources (continued)

Pin	Signal	Managed by the PRCM	Description
vdda_slicer	VDDA_SLICER	No (fixed)	Clock slicer power supply
vdd_osc	VDD_OSC	No (fixed)	Clock oscillator core power supply
vdda_ldo_sram_mpu	VDDA_LDO_SRAM_MPU	No	Supplies LDO_MPU_M for MPU Cortex-A9 SRAM
vdda_ldo_sram_iva_audio	VDDA_LDO_SRAM_IVA_AUDIO	No	Supplies LDO_IVA_M for IVA SRAM
vdda_ldo_sram_core	VDDA_LDO_SRAM_CORE	No	Supplies LDO_CORE_M for CORE SRAM
vdda_ldo_emu_wkup	VDDA_LDO_EMU_WKUP	No	Supplies LDO_WAKEUP for WAKEUP/EMU logic
vdda_bdgp	VDDA_BDGP	No (fixed)	Bandgap supply input
vdda_vbbldo_mpu	VDDA_VBBLDO_MPU	No	MPU VBB LDO supply input
vdda_vbbldo_iva_audio	VDDA_VBBLDO_IVA	No	IVA VBB LDO supply input

3.3.6 External Wake-Up Signals

A pre-wakeup request input goes directly to the PRCM module. It is used to wake up the device before the C2C_WAKEREQ_IN is asserted.

Table 3-26 lists the wake-up signal information.

Table 3-26. Wake-Up Signals

Pin	Signal	Description
c2c_pwkup	C2C_PWKUP	C2C pre-wakeup

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3.4 PRCM Subsystem Integration

The internal configuration registers of the power-management modules can be accessed for configuration and control through their respective WKUP_L4 interconnect. In addition to the L4 interconnect, the internal modules interface contains the following interfaces and signals:

- A set of signals for idle/wake-up control for each module
- Clocks and reset signals for the modules
- Power control signals (switches and memories) to the power domains
- Interrupts to the MPU Cortex-A9, MPU Cortex-M3, and DSP INTCs
- Voltage error commands from the SmartReflex modules to the external power IC
- Phase-locked loop (PLL) control commands for recalibration and bypass of the digital phase-locked loops (DPLLs)

Figure 3-18 shows details of the control interface to a generic power domain.

3.4.1 Device Power-Management Layout

The PMFW sees the device split into voltage domains, power domain, and clock domains. Table 3-27 lists the device-level view with modules association to clock domains, power domains, and voltage domains.

Table 3-27. PMFW Device-Level Layout

Voltage Domain	Power Domain	Clock Domain	Module
LDO_WAKEUP	PD_EMU	CD_EMU	DEBUG
		N/A (the PRCM module itself)	CM1_EMU
	PD_WKUP	CD_WKUP	SYSCTRL_PADCONF_WKUP
			BANDGAP
			SYSCTRL_GENERAL_WKUP
			GPIO1
			Keyboard
			SAR_RAM
			32KTIMER
			GPTIMER1
			WDTIMER2
			L4_WKUP interconnect
		N/A (the PRCM module itself)	PRM
		N/A (the PRCM module itself)	SCRM
VDD_CORE_L	PD_ALWON_CORE	CD_L4_ALWON_CORE	SR_CORE
			SR_IVA
			SR_MPU
		N/A (the PRCM module itself)	CM1
		N/A (clock generator)	DPLL_ABE
		N/A (clock generator)	DPLL_CORE
		N/A (clock generator)	DPLL_PER
		N/A (not clocked by the PRCM)	CORTEXM3_WKUPGEN
		N/A (not clocked by the PRCM)	SDMA_WKUPGEN
		N/A (not clocked by the PRCM)	SPINNER
	PD_CAM	CD_CAM	Face detect
			ISS
	PD_CORE	CD_L4_CFG	SYSCTRL_PADCONF_CORE
			SYSCTRL_GENERAL_CORE
			SPINLOCK
			L4_CFG interconnect

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Table 3-27. PMFW Device-Level Layout (continued)

Voltage Domain	Power Domain	Clock Domain	Module
			Mailbox
			SAR_ROM
		CD_EMIF	DDRPHY
			DLL
			DMM
			EMIF1
			EMIF2
			EMIF_FW
		CD_CORTEXM3	CORTEXM3
		CD_L3_2	GPMC
			L3_2 interconnect
			OCMC_RAM
		CD_L3_INSTR	L3_3 interconnect
			L3_INSTR interconnect
			OCP_WP1
		CD_L3_1	L3_1 interconnect
		CD_C2C	C2C
			C2C_FW
		CD_DMA	sDMA
		N/A (the PRCM module itself)	CM2
	PD_DSS	CD_DSS	DSS
	PD_SGX	CD_SGX	SGX
	PD_L3_INIT	CD_L3_INIT	HSI
			HSMMC1
			HSMMC2
			USBPHY
			FSUSB
			HSUSBHOST
			HSUSBOTG
			HSUSBTLL
		N/A (the PRCM module itself)	CM1_USB
		N/A (clock generator)	DPLL_USB
	PD_L4_PER	CD_L4_PER	GPTIMER10
			GPTIMER11
			GPTIMER2
			GPTIMER3
			GPTIMER4
			GPTIMER9
			ELM
			GPIO2
			GPIO3
			GPIO4
			GPIO5
			GPIO6
			HDQ
			I2C1
			I2C2

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Table 3-27. PMFW Device-Level Layout (continued)

Voltage Domain	Power Domain	Clock Domain	Module
			I2C3
			I2C4
			L4_PER interconnect
			MCBSP4
			MCSPI1
			MCSPI2
			MCSPI3
			MCSPI4
			HSMMC3
			HSMMC4
			HSMMC5
			SLIMBUS2
			UART1
			UART2
			UART3
			UART4
	PD_STD_EFUSE	CD_STD_EFUSE	STD_EFUSE
VDD_IVA_L	PD_ALWON_DSP	N/A (clock generator)	DPLL_IVA
		N/A (not clocked by the PRCM)	DSP_WKUPGEN
	PD_AUDIO	CD_ABE	Audio engine
			DMIC
			L4_ABE interconnect
			MCASP1
			MCBSP1
			MCBSP2
			MCBSP3
			MCPDM
			SLIMBUS1
			GPTIMER5
			GPTIMER6
			GPTIMER7
			GPTIMER8
			WDTIMER3
		N/A (the PRCM module itself)	CM1_ABE
	PD_IVAHD	CD_IVAHD	IVAHD
			SL2
	PD_DSP	CD_DSP	DSP
VDD_MPU_L	PD_ALWON_MPU	N/A (clock generator)	DPLL_MPU
		N/A (not clocked by the PRCM)	CORTEXA9_MPU_INTC
	PD_MPU	CD_CORTEXA9	CORTEXA9

3.4.2 Power-Management Scheme, Reset, and Interrupt Requests

3.4.2.1 Power Domain

Table 3-28 lists the PMFW modules and their associated power domains.

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Table 3-28. PMFW Module Power Domains

PMFW Module	Power Domain
SCRM	PD_WKUP
PRM	PD_WKUP
CM1	PD_ALWON_CORE
CM2	PD_CORE
SR_MPU	PD_ALWON_CORE
SR_IVA	PD_ALWON_CORE
SR_CORE	PD_ALWON_CORE

The PRM part of the PRCM module is in the PD_WKUP power domain, which is continuously active. It is composed of the logic that must be permanently supplied to manage domain power-state transitions and detect wake-up events.

The CM1 part of the PRCM module is in the PD_ALWON_CORE power domain, which is an always-on power domain, while the CM2 part of the PRCM module is in the PD_CORE power domain, which can be activated and deactivated according to the requirements of the executing applications.

3.4.2.2 Resets

The PMFW modules are reset by independent reset signals (see Table 3-29).

Table 3-29. PMFW Module Reset Signals

PMFW Module	Reset Signal
SCRM	SYS_PWRON_RST_IN
PRM	SYS_PWRON_RST_IN
CM1	ALWON_CM1_PWRON_RST
	ALWON_CM1_RST
CM2	CM2_PWRON_RET_RST
	CM2_RET_RST
SR_MPU	ALWON_CORE_RST
SR_IVA	ALWON_CORE_RST
SR_CORE	ALWON_CORE_RST

NOTE: See Section 3.5.3, *Reset Sources* for details on the reset trigger sources and assertion conditions.

3.4.2.3 Interrupt Requests

The PMFW modules can generate following interrupts listed in Table 3-30.

Table 3-30. PMFW Module Interrupts

Source PMFW Module	Source Signal Name	Destination Interrupt Controller	Destination Signal Name
PRCM	PRCM_MPU_IRQ	CORTEX-A9_MPU_INTC	MA_IRQ_11
PRCM	PRCM_M3_IRQ	CORTEX-M3_MPU_INTC	MM_IRQ_31
PRCM	PRCM_DSP_IRQ	DSP_INTC	D_IRQ_57
SR_IVA	SR_IVA_IRQ	CORTEX-A9_MPU_INTC	MA_IRQ_102
SR_MPU	SR_MPU_IRQ	CORTEX-A9_MPU_INTC	MA_IRQ_18
SR_CORE	SR_CORE_IRQ	CORTEX-A9_MPU_INTC	MA_IRQ_19

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3.5 Reset Management Functional Description

3.5.1 Overview

In the device the reset scheme is managed by the following modules:

- SCRM: System-level reset management. It provides correct reset routing and sequencing when one or more devices are stacked together in the same package.
- PRM: Device-level reset management

3.5.1.1 SCRM Reset Management Functional Description

The SCRM handles the device power-on and warm reset pads: sys_nrespwron and sys_nreswarm resets. Its tasks basically consist of:

- Extending reset duration beyond the pad reset release
- Routing the device pad resets to the reset manager in the PRM module

The SCRM is functionally sensitive to the device power-on reset. However, some of the register bits of SCRM registers are reset when a device warm reset occurs.

3.5.1.1.1 Power-On Reset

The SCRM receives the device power-on reset on the sys_nrespwron reset pad of the device. It extends the power-on reset duration to the device PRM module at least until a stable 32-kHz clock can be provided to it. The 32-kHz clock version of the device is active once the SCRM releases the internal power-on reset. The SCRM automatically deasserts the reset.

The SCRM automatically requests the system clock under a power-on reset condition. This mechanism is functionally active on the 32-kHz clock.

The power-on reset can also be asserted through software control. Software must enable the software reset assertion feature by setting the SRCM.EXTPWRONRSTCTRL[0] ENABLE bit and then by setting the SCRM.EXTPWRONRSTCTRL[1] PWRONRST bit to assert the reset.

3.5.1.1.2 Warm Reset

The device warm reset can be received from an external source through warm reset pad sys_nreswarm or from the device PRM module as a result of internal event.

The SCRM extends the device pad warm reset duration to the device PRM module.

The SCRM routes a warm reset source (that is, sys_nreswarm pad/PRM module) to a warm reset destination (that is, PRM module).

This routing of reset from the device pad to the PRM is enabled and disabled using the SCRM.EXTWARMRSTCTRL register. It is enabled by default.

The source of a warm reset, for each destination is logged in the corresponding SCRM.EXTWARMRSTST_REG register. The status of the reset source is logged when the destination reset is released. This is done at 32-kHz clock.

Software must clear the reset status bit.

3.5.1.2 PRM Reset Management Functional Description

The PRM module manages the resets to all power domains inside the device.

NOTE: The PRM module has no knowledge or control over resets generated locally within a module (for example, through configuration register bit Module name_SYSCONFIG[x] SOFTRESET). Software reset has the same effect on the module logic as a hardware reset.

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All PRM reset outputs are asynchronously asserted, while the deassertion is synchronous to the SYS_CLK clock. The reset managers in PRM use this clock for internal stall (delay) counter to delay deassertion of reset when the input reset source is deasserted.

In each power domain, one or more reset domains are defined. A reset domain is defined by a unique reset signal that originates from the reset manager and is connected to one or more modules of the device. All the connected modules of the reset domain are reset simultaneously when the reset signal is asserted. Independent control of these reset domains allows sequencing of the release of resets and ensures a safe reset of the entire power domain.

NOTE: All internal reset signals are active low, except for the DPLL reset signals, which are active high.

3.5.2 General Characteristics of Reset Signals

Reset signals can be categorized based on four criteria:

- Scope: Global or local reset
- Occurrence: Cold or warm reset
- Source type: Software or hardware triggered reset
- Retention type: Retention reset or nonretention reset

3.5.2.1 Scope

A reset signal can be categorized according to its scope (the area of the device affected by the reset):

- Global reset: Affects the entire logic of the device; all modules are reset. Generally, occurs when the device powers up or an abnormal operation is detected (the eFuse bad device is detected, etc.).
- Local reset: Affects one power domain, reset domain, or module. Generally, when a power domain transitions from off mode to active mode, or when a software-reset control bit for a domain is set, only the group of modules within that domain is affected.

3.5.2.2 Occurrence

A reset signal can be categorized depending on when the reset occurs:

- Cold reset: Occurs only on device power up or in certain emulation modes. The cold reset is a global reset that affects every module in the device. It usually corresponds to the initial power-on reset.
- Warm reset: Occurs when the device is in normal operating state. A module may use a warm reset to reset a subset of its logic. This is often done to speed up reset recovery time; that is, the time to transition to a safe operating state, compared to the time required upon receipt of a cold reset. Warm reset events include software-triggered reset per power domain, watchdog time-out, externally triggered and emulation initiated.

Modules that behave differently in cold reset and warm reset have two reset signals: RST and PWRON_RST. These reset signals reconstruct warm reset and cold reset in modules that require them.

The following modules are reset upon global cold reset events and not upon global warm reset events:

- All DPLLs associated with the PRCM
- All eFuses
- EMIF
- Control module – All the module instances in the PD_WKUP power domain

NOTE: For information about the PRCM module registers affected by the global warm reset, see the register description in Section 3.11, *PRCM Register Manual*.

3.5.2.3 Source Type

A reset can be categorized depending on whether it is software-controlled or hardware-triggered:

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- Software reset: Triggered by setting a bit in a configuration register of the PRCM module
- Hardware reset: Triggered by a signal from a hardware module inside or outside the PRCM module

3.5.2.4 Retention Type

The Power Domain Manager in PRM controls the assertion of two types of local cold reset sources, retention and nonretention reset. They are identified by the naming convention PowerDomain_DOM_RET_RST and PowerDomain_DOM_RST, respectively.

Upon transitioning a power domain to the ON-ACTIVE power state from the OFF power state:

- Retention type reset source is always asserted.
- Nonretention type reset source is always asserted.

Upon transitioning a power domain to the ON-ACTIVE power state from the RETENTION power state:

- Retention type reset source is never asserted.
- Nonretention type reset source is optionally asserted. The software-selectable option enables the PRM to support two retention mechanisms: CSWRET and OSWRET. Nonretention type reset source has following behavior:
  - It is asserted in-case of power domain state transition from OSWR-RETENTION state.
  - It is not asserted in-case of power domain state transition from CSWR-RETENTION state.

3.5.3 Reset Sources

The reset sources triggering the reset managers in the PRM are listed in this section.

3.5.3.1 Global Reset Sources

Table 3-31 lists the global reset sources of the device. The global reset source signals received by the reset manager trigger the reset of all the device modules. For all hardware reset signals, the source of the reset is identified; for the software reset signals, the reset triggering bit is identified.

Table 3-31. Global Reset Sources

Type (1)	Name	Source/Control	Description
H/C	SYS_PWRON_RST	Received from SCRM through input pin or through software control	The entire device is reset on power up.
H/W	SYS_WARMIN_RST	Received from SCRM through input pin or through software control	External hardware warm reset
S/C	GLOBAL_COLD_SW_RST	PRCM module.PRM_RSTCTRL[1] RST_GLOBAL_COLD_SW	Global software cold reset
S/W	GLOBAL_WARM_SW_RST	PRCM module.PRM_RSTCTRL[0] RST_GLOBAL_WARM_SW	Global software warm reset
H/W	VDD_CORE_VOLT_MGR_RST	PRCM	Asserted by the voltage manager FSMs when no response from the power IC is received during wake-up transition from retention or off mode
H/W	VDD_IVA_VOLT_MGR_RST	PRCM	
H/W	VDD_MPU_VOLT_MGR_RST	PRCM	
H/W	ICEPICK_RST	ICEPick module	It is used in emulation mode only.
H/W	ICEPICKPOR_RST	ICEPick module	It is used in emulation mode only.
H/W	CORTEXA9_WDT_RST	Either WDTIMER2 or MPU_A9 subsystem	It is triggered by a time-out event.
H/W	C2C_WARM_RST	C2C module	Global hardware warm reset.

(1) H = Hardware reset, S = Software reset, C = Cold reset, W = Warm reset

3.5.3.2 Local Reset Sources

In addition to the global reset sources the device can have a number of local reset sources for each power domain. The local reset sources can be cold or warm reset sources. They can be software or hardware

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triggered. Table 3-32 identifies the possible types of hardware-triggered local cold reset sources. Some power domains may support one or both of these local cold reset sources. The table does not highlight the software-triggered local warm reset sources which are listed in the reset management section of the respective power domains. A local reset source signal received by the reset manager resets only a specific part of the device (for example, some modules/subsystems within the power domain).

Table 3-32. Local Reset Sources

Type (1)	Name	Source/Control	Description
H/C	Power domain_RET_RST	PRCM	Asserted only for a power domain state transition from OFF to ON-ACTIVE state
H/C	Power domain_RST	PRCM	Asserted for any power domain transition from OFF or OSWR-RETENTION state to ON-ACTIVE state

(1) H = Hardware reset, C = Cold reset

3.5.4 Reset Domains

A power domain may receive power-on reset (PWRON_RST) and/or normal reset (RST) signals. These signals reset nonretention logic and behave as follows:

- On any global or local cold reset, RST and PWRON_RST are asserted.
- On any global or local warm reset, only RST is asserted.

A power domain may receive two additional retention logic reset signals: power-on retention reset (PWRON_RET_RST) and/or retention reset (RET_RST). These signals behave as follows:

- On any global cold reset or wakeup from OFF state to ON-ACTIVE state, RET_RST and PWRON_RET_RST are asserted.
- On any global warm reset, only RET_RST is asserted.
- On wakeup from RETENTION state, these signals are not asserted.

This section presents the trigger sources and attributes for all reset domains of the device. See Section 3.5.3, *Reset Sources,* for an explanation of each reset trigger source of the device.

Table 3-33 identifies the associated power and rest domains for each module.

Table 3-33. Modules, Power Domains and Reset Domains Association

Module	Power Domain	Reset Domains
CM1	PD_ALWON_CORE	ALWON_CM1_PWRON_RST, ALWON_CM1_RST
DPLL_ABE	PD_ALWON_CORE	ALWON_CORE_PWRON_RST
DPLL_CORE	PD_ALWON_CORE	ALWON_CORE_PWRON_RST
DPLL_PER	PD_ALWON_CORE	ALWON_CORE_PWRON_RST
CORTEXM3_WKUPGEN	PD_ALWON_CORE	None
SDMA_WKUPGEN	PD_ALWON_CORE	None
SR_CORE	PD_ALWON_CORE	ALWON_CORE_RST
SR_IVA	PD_ALWON_CORE	ALWON_CORE_RST
SR_MPU	PD_ALWON_CORE	ALWON_CORE_RST
SPINNER	PD_ALWON_CORE	None
DPLL_IVA	PD_ALWON_DSP	DPLL_IVA_PWRON_RST
DSP_WKUPGEN	PD_ALWON_DSP	ALWON_IVA_RST
DPLL_MPU	PD_ALWON_MPU	DPLL_MPU_PWRON_RST
CORTEXA9_MPU_INTC	PD_ALWON_MPU	ALWON_MPU_RST
AUDIO ENGINE	PD_AUDIO	AUDIO_RST
CM1_ABE	PD_AUDIO	AUDIO_PWRON_RST
DMIC	PD_AUDIO	AUDIO_RST
L4_ABE interconnect	PD_AUDIO	AUDIO_RST

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Table 3-33. Modules, Power Domains and Reset Domains Association (continued)

Module	Power Domain	Reset Domains
MCASP1	PD_AUDIO	AUDIO_RST
MCBSP1	PD_AUDIO	AUDIO_RST
MCBSP2	PD_AUDIO	AUDIO_RST
MCBSP3	PD_AUDIO	AUDIO_RST
MCPDM	PD_AUDIO	AUDIO_RST
SLIMBUS1	PD_AUDIO	AUDIO_RST
GPTIMER5	PD_AUDIO	AUDIO_RST
GPTIMER6	PD_AUDIO	AUDIO_RST
GPTIMER7	PD_AUDIO	AUDIO_RST
GPTIMER8	PD_AUDIO	AUDIO_RST
WDTIMER3	PD_AUDIO	AUDIO_RST
FACE DETECT	PD_CAM	CAM_RST
ISS	PD_CAM	CAM_RST
SYSCTRL_PADCONF_CORE	PD_CORE	CORE_PWRON_RET_RST
CM2	PD_CORE	CM2_PWRON_RET_RST, CM2_RET_RST
DDRPHY	PD_CORE	EMIF_PWRON_RST
SYSCTRL_GENERAL_CORE	PD_CORE	CORE_PWRON_RET_RST
DLL	PD_CORE	DLL_RST
DMM	PD_CORE	CORE_RET_RST, CORE_RST
CORTEXM3	PD_CORE	CORTEXM3_PWRON_RST, CORTEXM3_RET_RST, CORTEXM3_RST1, CORTEXM3_RST2, CORTEXM3_RST3
EMIF1	PD_CORE	CORE_PWRON_RET_RST
EMIF2	PD_CORE	CORE_PWRON_RET_RST
EMIF_FW	PD_CORE	CORE_PWRON_RET_RST, CORE_RST
GPMC	PD_CORE	CORE_RET_RST
SPINLOCK	PD_CORE	CORE_RET_RST
L3_2 interconnect	PD_CORE	CORE_PWRON_RET_RST, CORE_RST
L3_3 interconnect	PD_CORE	CORE_PWRON_RET_RST, CORE_RST
L3_1 interconnect	PD_CORE	CORE_PWRON_RET_RST, CORE_RST
L3_INSTR interconnect	PD_CORE	CORE_RST
OCP_WP1	PD_CORE	CORE_PWRON_RET_RST, CORE_RST
L4_CFG interconnect	PD_CORE	CORE_PWRON_RET_RST, CORE_RST
Mailbox	PD_CORE	CORE_RET_RST
OCMC_RAM	PD_CORE	CORE_RST
C2C	PD_CORE	CORE_RET_RST, CORE_RST
C2C_FW	PD_CORE	CORE_PWRON_RET_RST, CORE_RST
SAR_ROM	PD_CORE	CORE_RST
sDMA	PD_CORE	SDMA_RET_RST
DSS	PD_DSS	DSS_RET_RST, DSS_RST
CM1_EMU	PD_EMU	EMU_PWRON_RST
DEBUG	PD_EMU	EMU_EARLY_PWRON_RST, EMU_PWRON_RST, EMU_RST
SGX	PD_SGX	SGX_RST
IVAHD	PD_IVAHD	IVAHD_PWRON_RST, IVAHD_RST, IVAHD_SEQ1_RST, IVAHD_SEQ2_RST
SL2	PD_IVAHD	IVAHD_RST

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Table 3-33. Modules, Power Domains and Reset Domains Association (continued)

Module	Power Domain	Reset Domains
CM1_USB	PD_L3_INIT	L3_INIT_PWRON_RST
DPLL_USB	PD_L3_INIT	DPLL_L3_INIT_PWRON_RET_RST
HSI	PD_L3_INIT	L3_INIT_RET_RST
HSMMC1	PD_L3_INIT	L3_INIT_RET_RST
HSMMC2	PD_L3_INIT	L3_INIT_RET_RST
USBPHY	PD_L3_INIT	L3_INIT_RST
FSUSB	PD_L3_INIT	L3_INIT_RET_RST
HSUSBHOST	PD_L3_INIT	L3_INIT_RET_RST
HSUSBOTG	PD_L3_INIT	L3_INIT_RET_RST
HSUSBTLL	PD_L3_INIT	L3_INIT_RET_RST
GPTIMER10	PD_L4_PER	L4_PER_RST
GPTIMER11	PD_L4_PER	L4_PER_RST
GPTIMER2	PD_L4_PER	L4_PER_RST
GPTIMER3	PD_L4_PER	L4_PER_RST
GPTIMER4	PD_L4_PER	L4_PER_RST
GPTIMER9	PD_L4_PER	L4_PER_RST
ELM	PD_L4_PER	L4_PER_RST
GPIO2	PD_L4_PER	L4_PER_RET_RST
GPIO3	PD_L4_PER	L4_PER_RET_RST
GPIO4	PD_L4_PER	L4_PER_RET_RST
GPIO5	PD_L4_PER	L4_PER_RET_RST
GPIO6	PD_L4_PER	L4_PER_RET_RST
HDQ	PD_L4_PER	L4_PER_RST
I2C1	PD_L4_PER	L4_PER_RET_RST
I2C2	PD_L4_PER	L4_PER_RST
I2C3	PD_L4_PER	L4_PER_RST
I2C4	PD_L4_PER	L4_PER_RST
L4_PER interconnect	PD_L4_PER	L4_PER_PWRON_RET_RST, L4_PER_RST
MCBSP4	PD_L4_PER	L4_PER_RST
MCSPI1	PD_L4_PER	L4_PER_RST
MCSPI2	PD_L4_PER	L4_PER_RST
MCSPI3	PD_L4_PER	L4_PER_RST
MCSPI4	PD_L4_PER	L4_PER_RST
HSMMC3	PD_L4_PER	L4_PER_RST
HSMMC4	PD_L4_PER	L4_PER_RST
HSMMC5	PD_L4_PER	L4_PER_RST
SLIMBUS2	PD_L4_PER	L4_PER_RST
UART1	PD_L4_PER	L4_PER_RET_RST
UART2	PD_L4_PER	L4_PER_RET_RST
UART3	PD_L4_PER	L4_PER_RET_RST
UART4	PD_L4_PER	L4_PER_RET_RST
CORTEXA9	PD_MPU	CORTEXA9_PWRON_RST, CORTEXA9_RST, MPU_MA_RST, MPU_MA_RET_RST, MPU_MA_PWRON_RET_RST
STD_EFUSE	PD_STD_EFUSE	STD_EFUSE_PWRON_RST
DSP	PD_DSP	DSP_RST, DSP_PWRON_RST, DSP_RET_RST, DSP_SYS_RST

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Table 3-33. Modules, Power Domains and Reset Domains Association (continued)

Module	Power Domain	Reset Domains
SYSCTRL_PADCONF_WKUP	PD_WKUP	WKUP_PWRON_RST
BANDGAP	PD_WKUP	WKUP_PWRON_RST
SYSCTRL_GENERAL_WKUP	PD_WKUP	WKUP_PWRON_RST
GPIO1	PD_WKUP	WKUP_RST
Keyboard	PD_WKUP	WKUP_RST
SAR_RAM	PD_WKUP	WKUP_RST
32KTIMER	PD_WKUP	WKUP_RST, WKUP_SYS_PWRON_RST
GPTIMER1	PD_WKUP	WKUP_RST
WDTIMER2	PD_WKUP	WKUP_RST
L4_WKUP interconnect	PD_WKUP	WKUP_RST

Table 3-34 lists the reset sources that trigger the reset domains of the device.

Table 3-34. Reset Sources For the Reset Domains

Reset Domain	Reset Source	Reset Source Type
AUDIO_PWRON_RST	GLOBAL_COLD_SW_RST	Global cold
	ICEPICKPOR_RST	Global cold
	SYS_PWRON_RST	Global cold
AUDIO_RST	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	CORTEXA9_WDT_RST	Global warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_IVA_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	C2C_WARM_RST	Global warm
	ICEPICK_RST	Global warm
ALWON_CM1_PWRON_RST	GLOBAL_COLD_SW_RST	Global cold
	ICEPICKPOR_RST	Global cold
	SYS_PWRON_RST	Global cold
ALWON_CM1_RST	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	CORTEXA9_WDT_RST	Global warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_IVA_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	C2C_WARM_RST	Global warm
	ICEPICK_RST	Global warm
ALWON_CORE_PWRON_RST	GLOBAL_COLD_SW_RST	Global cold
	ICEPICKPOR_RST	Global cold
	SYS_PWRON_RST	Global cold
ALWON_CORE_RST	GLOBAL_COLD_SW_RST	Global cold

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Table 3-34. Reset Sources For the Reset Domains (continued)

Reset Domain	Reset Source	Reset Source Type
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	CORTEXA9_WDT_RST	Global warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_IVA_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	C2C_WARM_RST	Global warm
	ICEPICK_RST	Global warm
ALWON_IVA_RST	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	CORTEXA9_WDT_RST	Global warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_IVA_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	C2C_WARM_RST	Global warm
	ICEPICK_RST	Global warm
ALWON_MPU_RST	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	CORTEXA9_WDT_RST	Global warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_IVA_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	C2C_WARM_RST	Global warm
	ICEPICK_RST	Global warm
CAM_RST	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	CORTEXA9_WDT_RST	Global warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_IVA_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	C2C_WARM_RST	Global warm
CM2_PWRON_RET_RST	GLOBAL_COLD_SW_RST	Global cold
	ICEPICKPOR_RST	Global cold
	SYS_PWRON_RST	Global cold
CM2_RET_RST	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm

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Table 3-34. Reset Sources For the Reset Domains (continued)

Reset Domain	Reset Source	Reset Source Type
	ICEPICKPOR_RST	Global cold
	CORTEXA9_WDT_RST	Global warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_IVA_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	C2C_WARM_RST	Global warm
CORE_PWRON_RET_RST	GLOBAL_COLD_SW_RST	Global cold
	ICEPICKPOR_RST	Global cold
	ICEPICK_RST	Global warm
CORE_RET_RST	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	CORTEXA9_WDT_RST	Global warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_IVA_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	C2C_WARM_RST	Global warm
	ICEPICK_RST	Global warm
CORE_RST	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	CORTEXA9_WDT_RST	Global warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_IVA_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	C2C_WARM_RST	Global warm
	ICEPICK_RST	Global warm
DLL_RST	DLL_FREQCHANGE_RST	Local Warm
	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	CORTEXA9_WDT_RST	Global warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_IVA_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	C2C_WARM_RST	Global warm
	ICEPICK_RST	Global warm
DPLL_IVA_PWRON_RST	GLOBAL_COLD_SW_RST	Global cold
	ICEPICKPOR_RST	Global cold

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Table 3-34. Reset Sources For the Reset Domains (continued)

Reset Domain	Reset Source	Reset Source Type
	SYS_PWRON_RST	Global cold
DPLL_L3_INIT_PWRON_RET_RST	GLOBAL_COLD_SW_RST	Global cold
	ICEPICKPOR_RST	Global cold
	SYS_PWRON_RST	Global cold
DPLL_MPU_PWRON_RST	GLOBAL_COLD_SW_RST	Global cold
	ICEPICKPOR_RST	Global cold
	SYS_PWRON_RST	Global cold
DSS_RET_RST	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	CORTEXA9_WDT_RST	Global warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_IVA_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	C2C_WARM_RST	Global warm
	ICEPICK_RST	Global warm
DSS_RST	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	CORTEXA9_WDT_RST	Global warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_IVA_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	C2C_WARM_RST	Global warm
	ICEPICK_RST	Global warm
CORTEXM3_PWRON_RST	GLOBAL_COLD_SW_RST	Global cold
	ICEPICKPOR_RST	Global cold
	SYS_PWRON_RST	Global cold
CORTEXM3_RET_RST	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	CORTEXA9_WDT_RST	Global warm
	RM_CORTEXM3_RSTCTRL_RST3	Local Warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_IVA_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	C2C_WARM_RST	Global warm
	ICEPICK_RST	Global warm
CORTEXM3_RST1	CORTEXM3_ICECRUSHER1_RST	Local Warm
	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm

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Table 3-34. Reset Sources For the Reset Domains (continued)

Reset Domain	Reset Source	Reset Source Type
	ICEPICKPOR_RST	Global cold
	CORTEXA9_WDT_RST	Global warm
	RM_CORTEXM3_RSTCTRL_RST1	Local Warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_IVA_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	C2C_WARM_RST	Global warm
	ICEPICK_RST	Global warm
CORTEXM3_RST2	CORTEXM3_ICECRUSHER2_RST	Local Warm
	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	CORTEXA9_WDT_RST	Global warm
	RM_CORTEXM3_RSTCTRL_RST2	Local Warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_IVA_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	C2C_WARM_RST	Global warm
	ICEPICK_RST	Global warm
CORTEXM3_RST3	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	CORTEXA9_WDT_RST	Global warm
	RM_CORTEXM3_RSTCTRL_RST3	Local Warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_IVA_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	C2C_WARM_RST	Global warm
	ICEPICK_RST	Global warm
EMIF_PWRON_RST	GLOBAL_COLD_SW_RST	Global cold
	ICEPICKPOR_RST	Global cold
	SYS_PWRON_RST	Global cold
EMU_EARLY_PWRON_RST	GLOBAL_COLD_SW_RST	Global cold
	SYS_PWRON_RST	Global cold
EMU_PWRON_RST	GLOBAL_COLD_SW_RST	Global cold
	ICEPICKPOR_RST	Global cold
	SYS_PWRON_RST	Global cold
EMU_RST	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	CORTEXA9_WDT_RST	Global warm

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Table 3-34. Reset Sources For the Reset Domains (continued)

Reset Domain	Reset Source	Reset Source Type
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_IVA_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	C2C_WARM_RST	Global warm
	ICEPICK_RST	Global warm
SGX_RST	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	CORTEXA9_WDT_RST	Global warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_IVA_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	C2C_WARM_RST	Global warm
	ICEPICK_RST	Global warm
IVAHD_PWRON_RST	GLOBAL_COLD_SW_RST	Global cold
	ICEPICKPOR_RST	Global cold
	SYS_PWRON_RST	Global cold
IVAHD_RST	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	CORTEXA9_WDT_RST	Global warm
	RM_IVAHD_RSTCTRL_RST3	Local Warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_IVA_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	C2C_WARM_RST	Global warm
	ICEPICK_RST	Global warm
IVAHD_SEQ1_RST	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	IVAHD_ICECRUSHER1_RST	Local Warm
	CORTEXA9_WDT_RST	Global warm
	RM_IVAHD_RSTCTRL_RST1	Local Warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_IVA_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	C2C_WARM_RST	Global warm
	ICEPICK_RST	Global warm
IVAHD_SEQ2_RST	GLOBAL_COLD_SW_RST	Global cold

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Table 3-34. Reset Sources For the Reset Domains (continued)

Reset Domain	Reset Source	Reset Source Type
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	IVAHD_ICECRUSHER2_RST	Local Warm
	CORTEXA9_WDT_RST	Global warm
	RM_IVAHD_RSTCTRL_RST2	Local Warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_IVA_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	C2C_WARM_RST	Global warm
	ICEPICK_RST	Global warm
L3_INIT_PWRON_RST	GLOBAL_COLD_SW_RST	Global cold
	ICEPICKPOR_RST	Global cold
	SYS_PWRON_RST	Global cold
L3_INIT_RET_RST	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	CORTEXA9_WDT_RST	Global warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_IVA_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	C2C_WARM_RST	Global warm
	ICEPICK_RST	Global warm
L3_INIT_RST	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	CORTEXA9_WDT_RST	Global warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_IVA_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	C2C_WARM_RST	Global warm
	ICEPICK_RST	Global warm
L4_PER_PWRON_RET_RST	GLOBAL_COLD_SW_RST	Global cold
	ICEPICKPOR_RST	Global cold
	SYS_PWRON_RST	Global cold
L4_PER_RET_RST	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	CORTEXA9_WDT_RST	Global warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm

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Table 3-34. Reset Sources For the Reset Domains (continued)

Reset Domain	Reset Source	Reset Source Type
	VDD_IVA_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	C2C_WARM_RST	Global warm
L4_PER_RST	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	CORTEXA9_WDT_RST	Global warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_IVA_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	C2C_WARM_RST	Global warm
	ICEPICK_RST	Global warm
CORTEXA9_PWRON_RST	GLOBAL_COLD_SW_RST	Global cold
	ICEPICKPOR_RST	Global cold
	SYS_PWRON_RST	Global cold
CORTEXA9_RST	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	CORTEXA9_ICECRUSHER_RST	Local Warm
	CORTEXA9_WDT_RST	Global warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_IVA_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	C2C_WARM_RST	Global warm
	ICEPICK_RST	Global warm
MPU_MA_PWRON_RET_RST	GLOBAL_COLD_SW_RST	Global cold
	ICEPICKPOR_RST	Global cold
	SYS_PWRON_RST	Global cold
MPU_MA_RET_RST	GLOBAL_WARM_SW_RST	Global warm
	CORTEXA9_WDT_RST	Global warm
	SYS_WARMIN_ARST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_IVA_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	C2C_WARM_RST	Global warm
	ICEPICK_RST	Global warm
	GLOBAL_COLD_SW_RST	Global cold
	ICEPICKPOR_RST	Global cold
	SYS_PWRON_RST	Global cold
MPU_MA_RST	GLOBAL_WARM_SW_RST	Global warm
	CORTEXA9_WDT_RST	Global warm
	SYS_WARMIN_ARST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm

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Table 3-34. Reset Sources For the Reset Domains (continued)

Reset Domain	Reset Source	Reset Source Type
	VDD_IVA_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	C2C_WARM_RST	Global warm
	ICEPICK_RST	Global warm
	GLOBAL_COLD_SW_RST	Global cold
	ICEPICKPOR_RST	Global cold
	SYS_PWRON_RST	Global cold
SDMA_RET_RST	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	CORTEXA9_WDT_RST	Global warm
	SDMA_RESTORE_RST	Local Warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_IVA_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	C2C_WARM_RST	Global warm
	ICEPICK_RST	Global warm
STD_EFUSE_PWRON_RST	SYS_PWRON_RST	Global cold
DSP_RST	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	CORTEXA9_WDT_RST	Global warm
	RM_DSP_RSTCTRL_RST1	Local Warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	DSP_EMU_RESET_REQ_TR	Local Warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_IVA_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	C2C_WARM_RST	Global warm
	ICEPICK_RST	Global warm
DSP_PWRON_RST	GLOBAL_COLD_SW_RST	Global cold
	ICEPICKPOR_RST	Global cold
	SYS_PWRON_RST	Global cold
	ICEPICK_RST	Global warm
DSP_RET_RST	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	CORTEXA9_WDT_RST	Global warm
	RM_DSP_RSTCTRL_RST2	Local Warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_IVA_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm

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Table 3-34. Reset Sources For the Reset Domains (continued)

Reset Domain	Reset Source	Reset Source Type
	C2C_WARM_RST	Global warm
	ICEPICK_RST	Global warm
DSP_SYS_RST	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	CORTEXA9_WDT_RST	Global warm
	RM_DSP_RSTCTRL_RST2	Local Warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_IVA_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	C2C_WARM_RST	Global warm
	ICEPICK_RST	Global warm
WKUP_PWRON_RST	GLOBAL_COLD_SW_RST	Global cold
	ICEPICKPOR_RST	Global cold
	SYS_PWRON_RST	Global cold
WKUP_RST	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	CORTEXA9_WDT_RST	Global warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_IVA_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	C2C_WARM_RST	Global warm
	ICEPICK_RST	Global warm
WKUP_SYS_PWRON_RST	SYS_PWRON_RST	Global cold

Table 3-35 lists the attributes of the reset manager associated with the reset domains. The clock to the reset manager, the delay count before release of reset, and the reset release stall conditions for the reset domains are listed. Apart from the identified reset release stall conditions, a universal release stall condition (that is, applicable to all reset signals) is the eFuse scan completion.

Table 3-35. Reset Domains Attributes

Reset Domain	RM Clock	RM Clock Count	Release Stall Conditions
AUDIO_PWRON_RST	SYS_CLK	0x0	None
AUDIO_RST	SYS_CLK	0x0	None
ALWON_CM1_PWRON_RST	SYS_CLK	0x2	None
ALWON_CM1_RST	SYS_CLK	0x2	L4_ROOT_CLK clock is not active.
ALWON_CORE_PWRON_RST	SYS_CLK	0x0	None
ALWON_CORE_RST	SYS_CLK	0x0	None
ALWON_IVA_RST	SYS_CLK	0x0	None
ALWON_MPU_RST	SYS_CLK	0x0	MPU_CLK is not active.
CAM_RST	SYS_CLK	0x0	None
CM2_PWRON_RET_RST	SYS_CLK	0x2	None

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Table 3-35. Reset Domains Attributes (continued)

Reset Domain	RM Clock	RM Clock Count	Release Stall Conditions
CM2_RET_RST	SYS_CLK	0x2	L4_ICLK clock is not active.
CORE_PWRON_RET_RST	SYS_CLK	0x0	None
CORE_RET_RST	SYS_CLK	0x0	None
CORE_RST	SYS_CLK	0x0	None
DLL_RST	SYS_CLK	0x3	None
DPLL_IVA_PWRON_RST	SYS_CLK	0x0	None
DPLL_L3_INIT_PWRON_RET_RST	SYS_CLK	0x0	None
DPLL_MPU_PWRON_RST	SYS_CLK	0x0	None
DSS_RET_RST	SYS_CLK	0x0	None
DSS_RST	SYS_CLK	0x0	None
CORTEXM3_PWRON_RST	SYS_CLK	ResetTime2(1)	MPU_M3_CLK clock is not active, RM_MPU_M3_RSTCTRL[2] RST3 is cleared, and automatic restore is complete.
CORTEXM3_RET_RST	SYS_CLK	ResetTime2(1)	MPU_M3_CLK clock is not active and subsystem is reset.
CORTEXM3_RST1	SYS_CLK	ResetTime2(1)	MPU_M3_CLK clock is not active and subsystem is reset.
CORTEXM3_RST2	SYS_CLK	ResetTime2(1)	MPU_M3_CLK clock is not active.
CORTEXM3_RST3	SYS_CLK	ResetTime2(1)	MPU_M3_CLK clock is not active and subsystem is reset.
EMIF_PWRON_RST	SYS_CLK	0x0	None
EMU_EARLY_PWRON_RST	SYS_CLK	0x2	None
EMU_PWRON_RST	SYS_CLK	ResetTime2(1)	EMU_SYS_CLK clock is not active.
EMU_RST	SYS_CLK	ResetTime2(1)	EMU_SYS_CLK clock is not active.
SGX_RST	SYS_CLK	0x0	None
IVAHD_PWRON_RST	SYS_CLK	ResetTime2(1)	IVAHD_ROOT_CLK clock is not active and RM_IVAHD_RSTCTRL[2] RST3 is cleared.
IVAHD_RST	SYS_CLK	ResetTime2(1)	IVAHD_ROOT_CLK clock is not active.
IVAHD_SEQ1_RST	SYS_CLK	ResetTime2(1)	IVAHD_ROOT_CLK clock is not active and IVAHD and SL2 are not idle.
IVAHD_SEQ2_RST	SYS_CLK	ResetTime2(1)	IVAHD_ROOT_CLK clock is not active and IVAHD and SL2 are not idle.
L3_INIT_PWRON_RST	SYS_CLK	0x0	None
L3_INIT_RET_RST	SYS_CLK	0x0	None
L3_INIT_RST	SYS_CLK	0x0	None
L4_PER_PWRON_RET_RST	SYS_CLK	0x0	None
L4_PER_RET_RST	SYS_CLK	0x0	None
L4_PER_RST	SYS_CLK	0x0	None
CORTEXA9_PWRON_RST	SYS_CLK	ResetTime2(1)	MPU_DPLL_CLK clock is not active.
CORTEXA9_RST	SYS_CLK	ResetTime2(1)	MPU_DPLL_CLK clock is not active, subsystem is reset, and automatic restore is complete.

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Table 3-35. Reset Domains Attributes (continued)

Reset Domain	RM Clock	RM Clock Count	Release Stall Conditions
SDMA_RET_RST	SYS_CLK	0x0	None
STD_EFUSE_PWRON_RST	SYS_CLK	ResetTime2(1)	STDEFUSE_SYS_CLK clock is not active and logic voltages are in ON state.
DSP_RST	SYS_CLK	ResetTime2(1)	DSP_ROOT_CLK clock is not active and subsystem is reset.
DSP_PWRON_RST	SYS_CLK	ResetTime2(1)	DSP_ROOT_CLK clock is not active, RM_DSP_RSTCTRL[1] RST2 is cleared, and automatic restore is complete.
DSP_RET_RST	SYS_CLK	ResetTime2(1)	DSP_ROOT_CLK clock is not active and subsystem is reset.
DSP_SYS_RST	SYS_CLK	ResetTime2(1)	DSP_ROOT_CLK clock is not active and subsystem is reset.
WKUP_PWRON_RST	SYS_CLK	0x0	None
WKUP_RST	SYS_CLK	0x0	None
WKUP_SYS_PWRON_RST	None	N/A	None

(1) ResetTime2 is set in the PRM_RSTTIME[14:10] RSTTIME2 bit field.

NOTE: WKUP_SYS_PWRON_RST is directly connected to SYS_PWRON_RST source reset.

3.5.5 Reset Logging

A reset of the device is logged in two ways. First, dedicated registers in the PRCM module (the RM_Power domain_RSTST) log the reset sources to power domain. Second, the Control Module logs the device reset activity in dedicated registers.

3.5.5.1 PRCM Module Reset Logging Mechanism

The reset status registers RM_power domain_RSTST and RM_RSTST are reset asynchronously on assertion of a global cold reset. However, a reset status bit is always logged when the reset is released to the domain.

For this reason, after the assertion of a global cold reset, the reset status register is cleared to 0. When the domain reset is released, the register bit to log the global cold reset (the RM_Power domain_RSTST[0] GLOBALCOLD_RST bit) is updated to 1. For the same reason, the reset status register of domains released from reset by software is updated only when software releases the domain reset.

The assertion of a global cold reset prevents logging any other source of reset until after the release of the domain reset. This is valid in the following situations:

- A source of reset other than global cold reset is asserted before, during, or after the active period of a global cold source of reset and before the release of the domain reset signal.
- A source of reset other than global cold reset was asserted and then released, but a global cold reset source was asserted before the release of the domain reset signal.

3.5.6 Reset Sequences

3.5.6.1 SCRM Power-on Reset Sequence

Figure 3-19 shows the power-on reset sequence as the reset is received by the SCRM and resulting interaction between SCRM and PRCM modules. Figure 3-20 shows the power-on reset sequence within the PRCM module.

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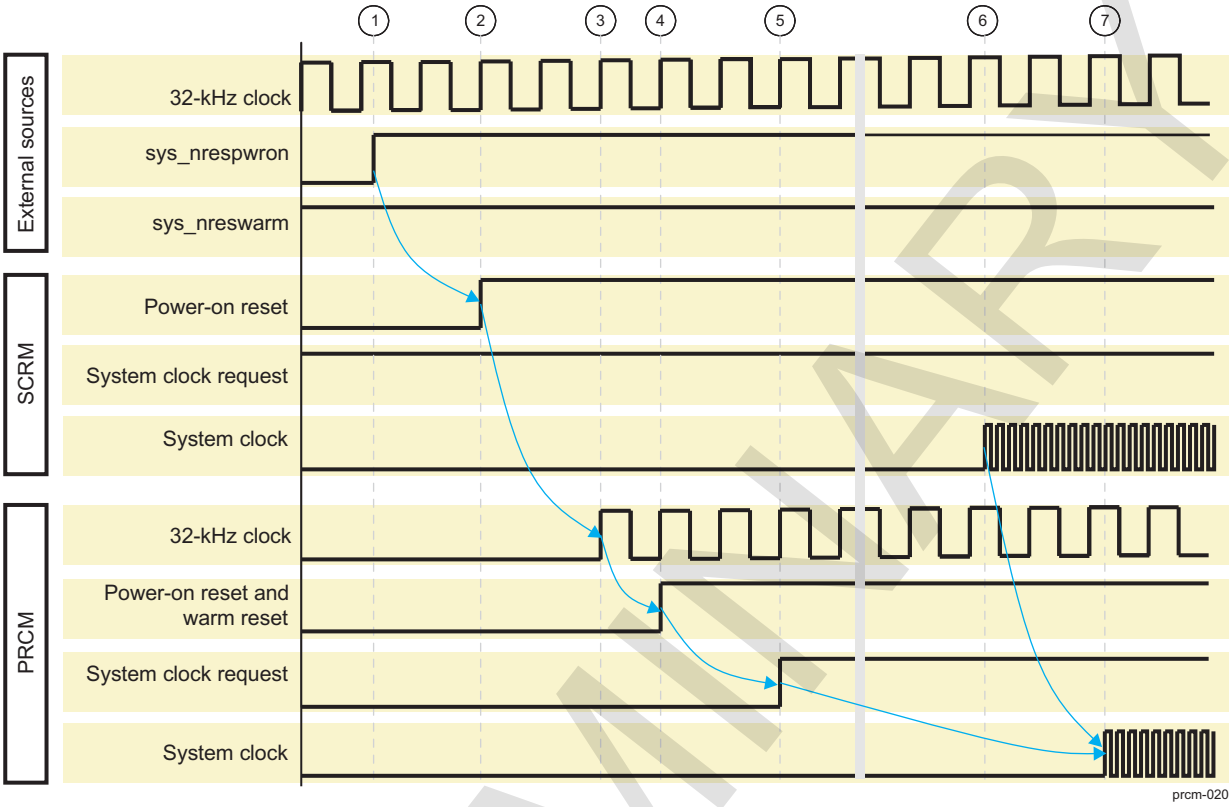
Figure 3-19. SCRM Power-On Reset Sequence



1. The power-on reset pad is released from reset while the 32 kHz is already active.
2. SCRM releases its internal power-on reset clocked at the 32-kHz clock.
3. SCRM delays the release of PRCM module resets to account for the stabilization time of the system clock source. It routes the 32-kHz clock to the PRCM module.
4. SCRM releases from reset (both power-on and warm reset) the PRCM module.
5. The PRCM module asserts a system clock request to the SCRM.
6. Once the system clock setup time counter overflows, the internal system clock version of SCRM is stable.
7. SCRM ungates the system clock to the PRCM module.

3.5.6.2 PRCM Module Power-On Reset Sequence

Figure 3-20 shows the power-on reset sequence.

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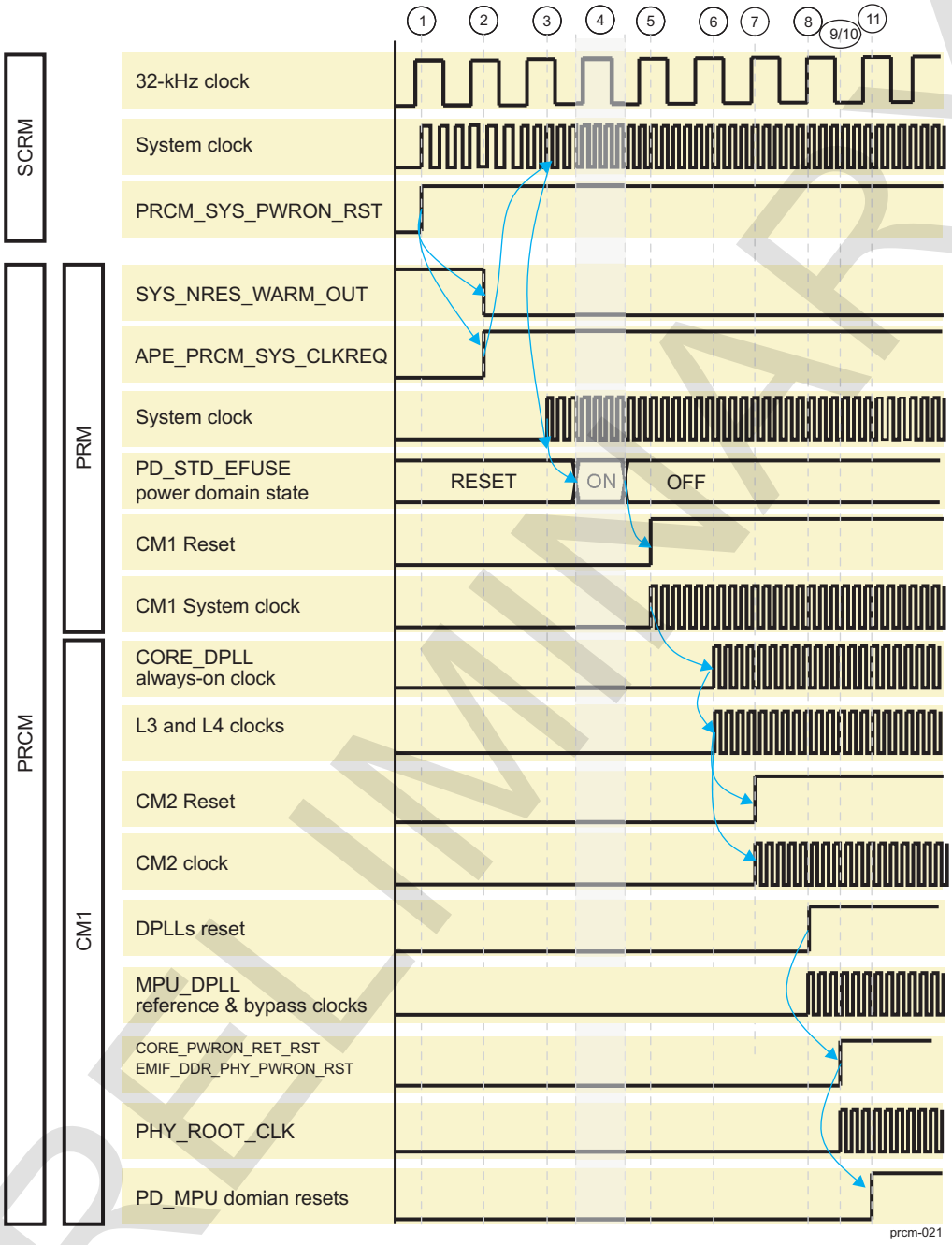
Figure 3-20. PRCM Module Power-On Reset Sequence



The assumptions are:

- All the logic and memory voltage sources are at their nominal voltage levels.
- The SCRM module is supplying the 32-kHz clock to the PRCM module and the clock is stable.
- The power-on reset SYS_PWRON_RST_IN has been released by the external power IC.

The power-up sequence is:

1. The SCRM releases global power-on reset to the PRCM module (that is, PRCM_SYS_PWRON_RST). As a result, the PRCM module starts the power-on reset sequence.
2. The PRCM module releases the SYS_NRES_WARM_OUT to the SCRM (only after all voltage domains have ramped-up) after some 32-kHz clock cycles, and it also asserts the APE_PRCM_SYS_CLKREQ to the SCRM module to request the system clock.

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3. SCRM provides the system clock to the PRCM module when the system clock source is stable.
4. Once the Standard eFuse controller clock has been enabled by the PRCM module, the PRM releases the standard eFuse controller domain from reset. This starts the eFuse sensing sequence. Upon completion of the eFuse auto load sequence, the PRM turns off the Standard eFuse controller clock. It also powers down the standard efuse controller power domain PD_STD_EFUSE.
5. The PRM logic is then released from reset. The PRM provides the CM1 with a version of the system clock and releases the CM1 from reset.
6. The CM1 starts the reference clock (and also bypass clock) of the CORE DPLL. In turn, the CORE DPLL, which is configured in bypass mode, generates the L3 clock (running at the system clock frequency at this stage). Now the CM1 logic is fully operational: CM1 logic is released from reset and L3 clock is running.
7. The CM1 starts the L4 clock version for the CM2 and the PRM deasserts the reset of the CM2.
8. The DPLLs are released from reset. The DPLLs can be released from reset before the L3 clock is running. The DPLL being under reset does not prevent the output clock from running. The CM1 starts the reference and bypass clocks to the DPLL_MPU.
9. The CORE is released from reset, provided the L3 clock is running. The EMIF comes out of reset as soon as CORE power domain power on retention reset (CORE_PWRON_RET_RST, see Table 3-35) is released by the PRCM module. The PRCM module also releases the EMIF_DDR_PHY_PWRON_RST. The PHY_ROOT_CLK is not running at this point, hence all the PHYs are asynchronously reset at the same time. The DDR_PHY_CLK clock is started later.
10. The PRCM module releases the idle request signal to the EMIF module once the EMIF functional clock is enabled. The EMIF then acknowledges the deassertion of idle request and becomes active.
11. The Cortex-A9 MPU subsystem is released from reset provided its clock is active and the L3 interconnect is operational.

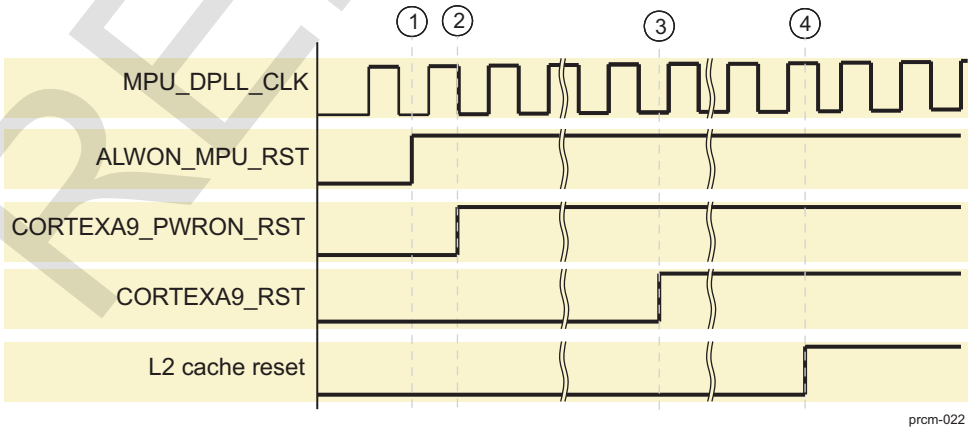
NOTE:

- PD_DSP and PD_IVAHD power domains are held under reset after power up by the assertion of software source of reset.
- PD_DSS, PD_SGX, PD_AUDIO, and PD_CAM are held under reset after power up until the PRCM module enables their interface clock.

3.5.6.3 Cortex-A9 MPU Subsystem Power-On Reset Sequence

Figure 3-21 shows the power-on reset sequence of the Cortex-A9 MPU subsystem.

Figure 3-21. Cortex-A9 MPU Power-On Reset Sequence



The assumptions after power-on reset assertion are:

- The PRCM module provides the DPLL_MPU reference clock and the bypass clock.
- The PRCM module has released DPLL_MPU reset and the DPLL_MPU is in bypass mode providing the clock (that is, bypass clock) to all the modules inside the Cortex-A9 MPU subsystem.

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The power-on reset sequence is:

1. The PRCM module releases asynchronously in PD_ALWON_MPU the ALWON_MPU_RST reset to the CORTEXA9_MPU_INTC module inside the Cortex-A9 MPU subsystem.
2. The PRCM module releases in PD_MPU the CORTEXA9_PWRON_RST (only after the MPU_DPLL_CLK is active) to the Cortex-A9 MPU subsystem and waits until the subsystem completes its internal reset sequence.
3. Once the Cortex-A9 MPU subsystem internal reset sequence completes, the PRCM module releases in PD_MPU the CORTEXA9_RST signal and the Cortex-A9 MPU starts booting.
4. The PRCM module releases the reset to L2 cache memory in the Cortex-A9 MPU subsystem 16 MPU_DPLL_CLK cycles after the release of CORTEXA9_PWRON_RST and CORTEXA9_RST.

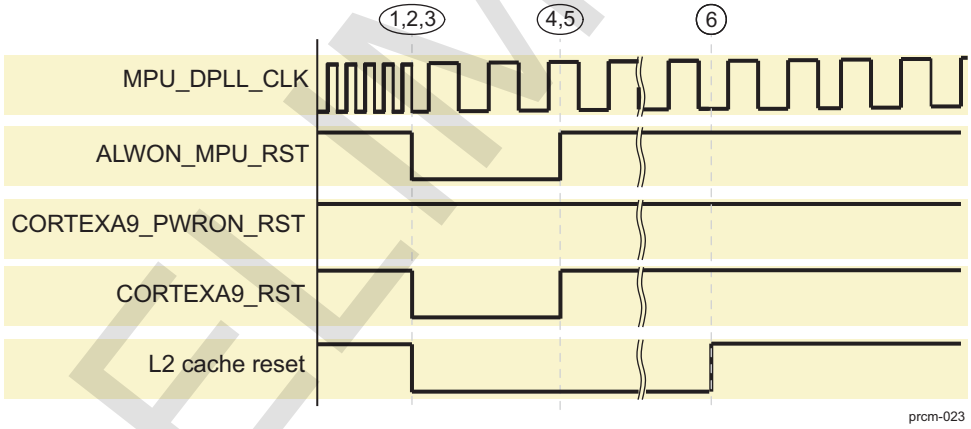
NOTE:

- The reset to the L2 cache memory in the Cortex-A9 MPU subsystem is asserted during initial power-on reset (that is, when the PD_MPU wakes-up from OFF state). It is also asserted during local or global warm reset. However, it is not asserted when the PD_MPU wakes-up from RETENTION state, that is (when the logic is off and L2 memory is in RETENTION state). This ensures that the L2 cache is retained on wake-up.
- The L1 cache memory in the Cortex-A9 MPU subsystem is not retained on PD_MPU wake-up.

3.5.6.4 Cortex-A9 MPU Subsystem Warm Reset Sequence

Figure 3-22 shows the warm reset sequence of the Cortex-A9 MPU subsystem.

Figure 3-22. Cortex-A9 MPU Warm Reset Sequence



The assumptions are:

- The DPLL_MPU is locked and providing the clock to the Cortex-A9 MPU subsystem.
- A global or local warm reset to the Cortex-A9 MPU subsystem is asserted.

The warm reset sequence is:

1. The PRCM module asserts in PD_ALWON_MPU the ALWON_MPU_RST reset to the CORTEXA9_MPU_INTC module inside Cortex-A9 MPU subsystem.
2. The PRCM module asserts in PD_MPU the CORTEXA9_RST reset to the Cortex-A9 MPU subsystem.
3. The PRCM module resets the L2 cache memory in the Cortex-A9 MPU subsystem by asserting its reset.
4. The PRCM module releases the ALWON_MPU_RST reset to the CORTEXA9_MPU_INTC module.
5. The PRCM module releases the CORTEXA9_RST, only after the DPLL_MPU is in bypass mode and MPU_DPLL_CLK is stable and active.
6. The PRCM module releases the reset to L2 cache memory in the Cortex-A9 MPU subsystem 16

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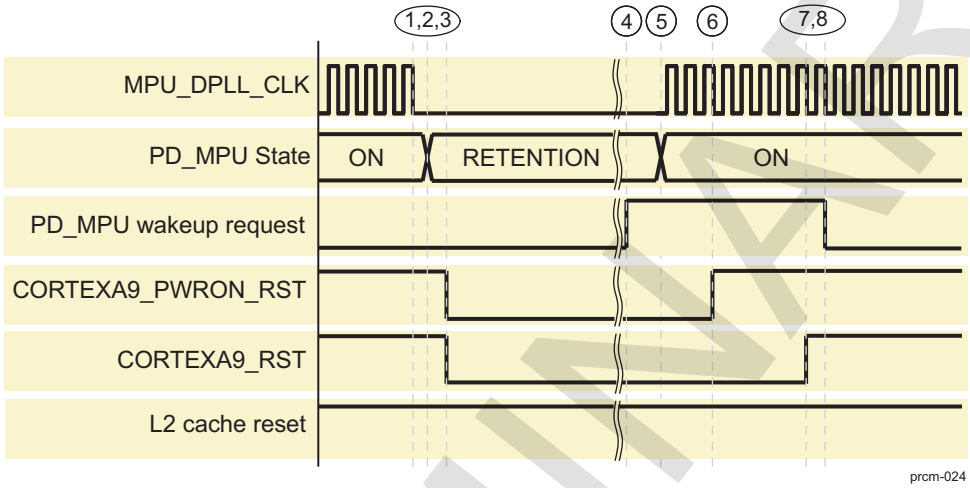
MPU_DPLL_CLK cycles after the release of CORTEXA9_RST.

3.5.6.5 Cortex-A9 MPU Subsystem Reset Sequence On Sleep and Wake-Up Transitions From RETENTION or OFF State

Figure 3-22 shows the sleep and wake-up transitions reset sequence from RETENTION or OFF state of the Cortex-A9 MPU subsystem.

Figure 3-23. Cortex-A9 MPU Reset Sequence on Sleep and Wake-Up Transition



The assumption is:

- The DPLL_MPU is locked and providing the clock to the Cortex-A9 MPU subsystem.

The sleep and wake-up transitions reset sequence is:

1. The PRCM module gates the MPU_DPLL_CLK to Cortex-A9 MPU subsystem.
2. The PRCM module switches the PD_MPU to RETENTION state.
3. The PRCM module asserts CORTEXA9_PWRON_RST and CORTEXA9_RST resets to Cortex-A9 MPU subsystem. The entire logic in the PD_MPU is held in reset. The reset to the L2 cache memory in the Cortex-A9 MPU subsystem is not asserted if the logic in the PD_MPU is held in reset.
4. The PRCM module resets the L2 cache memory in the Cortex-A9 MPU subsystem by asserting its reset.
5. The PRCM module releases the ALWON_MPU_RST reset to the CORTEXA9_MPU_INTC module.
6. The PRCM module releases the CORTEXA9_RST, only after the DPLL_MPU is in bypass mode and MPU_DPLL_CLK is stable and active.
7. The PRCM module releases the reset to L2 cache memory in the Cortex-A9 MPU subsystem 16 MPU_DPLL_CLK cycles after the release of CORTEXA9_RST.

3.5.6.6 IVAHD Subsystem Power-On Reset Sequence

Figure 3-24 shows the power-on reset sequence of the IVAHD subsystem.

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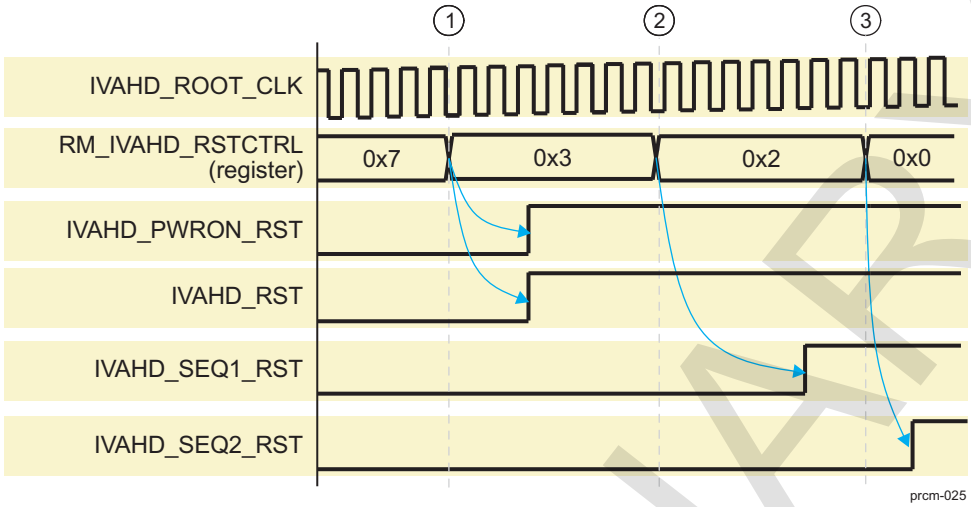
Figure 3-24. IVAHD Power-On Reset Sequence



The power-on reset to IVAHD is applied when PD_IVAHD is powered. The assumptions after power-on reset assertion are:

- The PRCM module provides the functional clock IVAHD_ROOT_CLK to the IVAHD subsystem and it has been enabled by the software control.

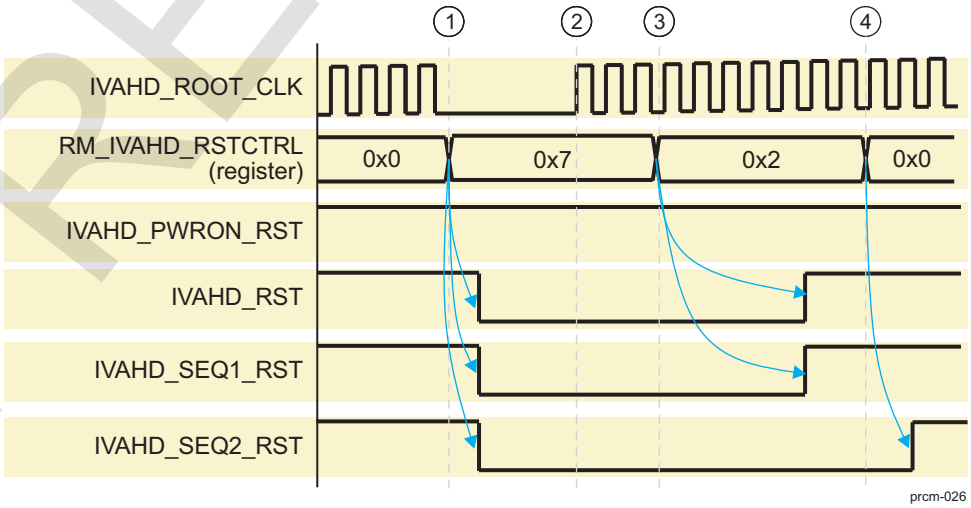
The power-on reset sequence is:

1. Software clears the RM_IVAHD_RSTCTRL[2] RST3 bit. This causes the PRCM module to release the IVAHD_PWRON_RST reset used inside IVAHD to reset mainly the emulation logic and the IVAHD_RST reset used to reset all logic inside IVAHD. Then software can download data into TCM memory while keeping the sequencer CPUs under reset.
2. Software clears the RM_IVAHD_RSTCTRL[0] RST1 bit. This releases the IVAHD_SEQ1_RST reset to the Sequencer1 CPU.
3. Similarly, software can clear the RM_IVAHD_RSTCTRL[1] RST2 bit. This releases the IVAHD_SEQ2_RST reset to the Sequencer2 CPU.

3.5.6.7 IVAHD Subsystem Software Warm Reset Sequence

Figure 3-25 shows the software warm reset sequence of the IVAHD Subsystem.

Figure 3-25. IVAHD Software Warm Reset Sequence



Before asserting the software reset to the IVAHD subsystem the MPU software must ensure that:

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- IVAHD sequencer CPUs are in IDLE state (CM_IVAHD_IVAHD_CLKCTRL[17:16] IDLEST).
- The IVA HD subsystem is in STANDBY state (CM_IVAHD_IVAHD_CLKCTRL[18] STBYST).
- The functional clock to the IVAHD subsystem has been gated by the PRCM module (CM_IVAHD_CLKSTCTRL[8] CLKACTIVITY_IVAHD_CLK).

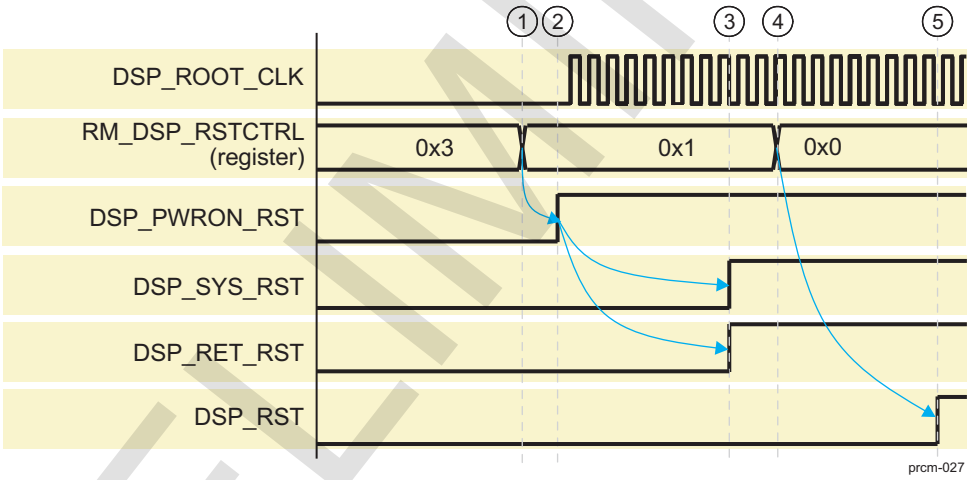
The software reset sequence is:

1. The MPU software sets the RM_IVAHD_RSTCTRL[2] RST3, RM_IVAHD_RSTCTRL[1] RST2, and RM_IVAHD_RSTCTRL[0] RST1 bits. This causes the PRCM module to assert the IVAHD_RST, IVAHD_SEQ1_RST, and IVAHD_SEQ2_RST resets to the IVAHD subsystem. The IVAHD_PWRON_RST remains deasserted.
2. The MPU software enables the functional clock to the IVAHD subsystem.
3. The MPU software clears the RM_IVAHD_RSTCTRL[2] RST3 and RM_IVAHD_RSTCTRL[0] RST1 bits. This causes the PRCM module to release the IVAHD_RST and IVAHD_SEQ1_RST resets to the IVAHD subsystem.
4. The MPU software clears the RM_IVAHD_RSTCTRL[1] RST2 bit. This releases the IVAHD_SEQ2_RST reset to the Sequencer2 CPU.

3.5.6.8 DSP Subsystem Power-On Reset Sequence

Figure 3-26 shows the power-on reset sequence of the DSP subsystem.

Figure 3-26. DSP Subsystem Power-On Reset Sequence



The assumptions on power-on reset assertion are:

- The PD_DSP is on.
- The MPU software sets the CM_DSP_DSP_CLKCTRL[1:0] MODULEMODE bit field to Auto.
- The MPU software sets the CM_DSP_CLKSTCTRL[1:0] CLKTRCTRL bit field to SW_WKUP or HW_AUTO.
- The DPLL_IVA is active and providing the DSP_ROOT_CLK. It can be locked prior to this sequence.

The power-on reset sequence is:

1. The MPU software clears the RM_DSP_RSTCTRL[1] RST2 bit in the PRCM module register to release from reset the DSP, MMU, and CACHE interface.
2. The PRCM module releases DSP_PWRON_RST once the reset manager counter (PRM_RSTTIME[14:10] RSTTIME2) has reached its limit. Upon the deassertion of power-on reset signal, the DSP subsystem starts the initialization sequence. During this initialization sequence all the internal registers inside DSP are properly reset and it also completes the reset for DSP, MMU, and CACHE interface.
3. Once the reset sequence of Step 2 completes and the reset manager counter (PRM_RSTTIME[14:10] RSTTIME2) has expired, the PRCM module releases DSP_SYS_RST and DSP_RET_RST signals.

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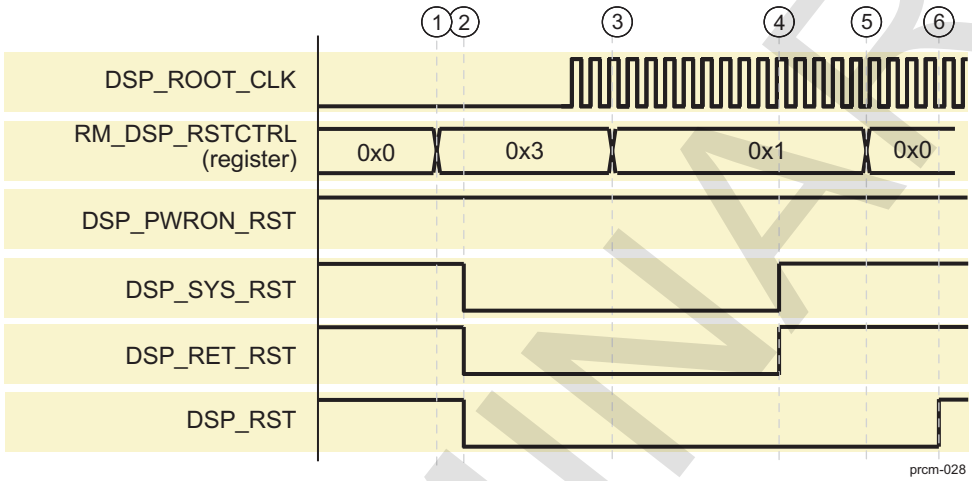
4. The MPU software must configure the MMU once the MMU is out of reset. After MMU configuration is done, the MPU software clears the RM_DSP_RSTCTRL[0] RST1 bit in the PRCM module register.
5. The PRCM module releases DSP_RST, which causes the DSP to start booting.

3.5.6.9 DSP Subsystem Software Warm Reset Sequence

Figure 3-27 shows the software warm reset sequence of the DSP subsystem.

Figure 3-27. DSP Subsystem Software Warm Reset Sequence



The assumptions on power-on reset assertion are:

- The DSP is in IDLE state.
- The DSP_ROOT_CLK is gated.

The power-on reset sequence is:

1. The MPU software sets the RM_DSP_RSTCTRL[1] RST2 and RM_DSP_RSTCTRL[0] RST1 bits.
2. The PRCM module asserts the DSP_SYS_RST, DSP_RET_RST, and DSP_RST reset signals. DSP_PWRON_RST remains deasserted in this case.
3. The MPU software re-enables the DSP_ROOT_CLK and clears the RM_DSP_RSTCTRL[1] RST2 bit in the PRCM module register to reset DSP, MMU, and CACHE interface. The DSP subsystem starts the partial initialization sequence for the warm reset.
4. Once the reset sequence of Step 3 completes and the reset manager counter (PRM_RSTTIME[14:10] RSTTIME2) has expired, the PRCM module releases the DSP_SYS_RST and DSP_RET_RST signals.
5. The MPU software clears the RM_DSP_RSTCTRL[0] RST1 bit in the PRCM module register.
6. The PRCM module releases DSP_RST, which causes the DSP to start booting.

3.5.6.10 DSP Subsystem Reset Sequence On Wake-Up Transitions From OSWR RETENTION State

Figure 3-28 shows the reset sequence of the DSP subsystem on wake-up transitions from OSWR RETENTION state.

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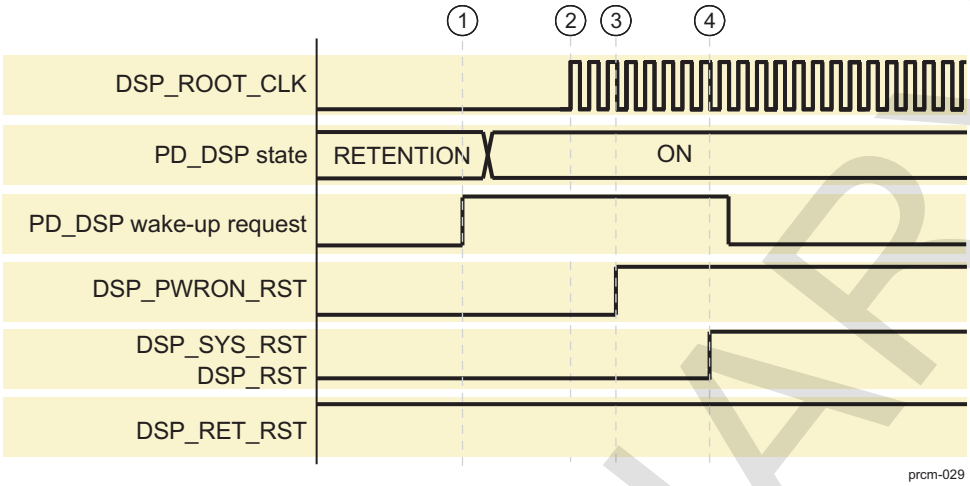
Figure 3-28. DSP Subsystem Reset Sequence On Wake-Up Transitions From OSWR RETENTION State



The assumptions on power-on reset assertion are:

- The DSP is in INACTIVE state.
- The DSP_ROOT_CLK is gated.
- The PD_DSP is in OSWR RETENTION state.
- The DSP_PWRON_RST, DSP_SYS_RST, and DSP_RST resets are held asserted, while DSP_RET_RST is not asserted by the PRCM module.

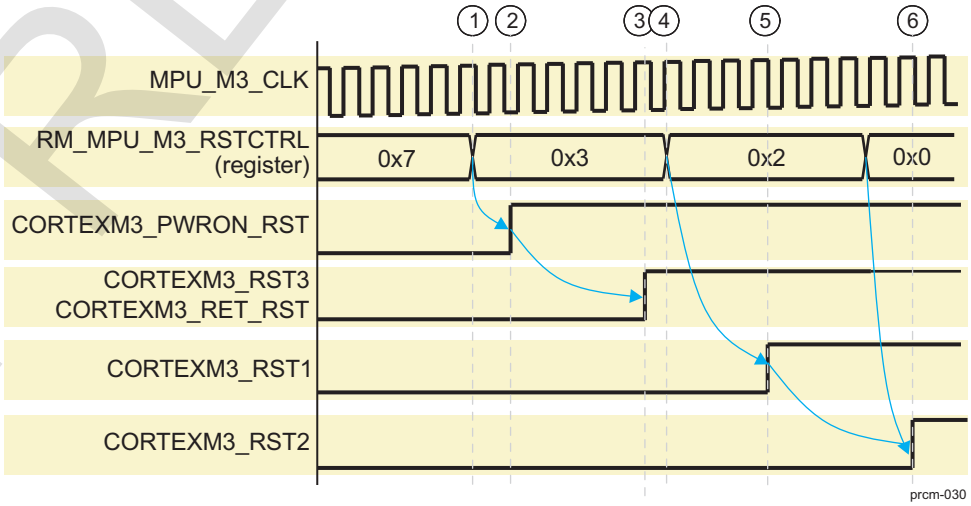
The power-on reset sequence is:

1. A wake-up request is received by the PRCM module and it switches the PD_DSP to ON state
2. The PRCM module then enables the DSP_ROOT_CLK and switches the CD_DSP to ACTIVE state.
3. The PRCM module releases DSP_PWRON_RST once the reset manager counter (PRM_RSTTIME[14:10] RSTTIME2) has reached its limit. Upon the deassertion of the power-on reset signal, the DSP subsystem starts the initialization sequence.
4. Once the reset sequence of Step 3 completes the PRCM module releases the DSP_SYS_RST and DSP_RST signals.

3.5.6.11 Cortex-M3 MPU Subsystem Power-On Reset Sequence

Figure 3-29 shows the power-on reset sequence of the Cortex-M3 MPU subsystem.

Figure 3-29. Cortex-M3 MPU Power-On Reset Sequence



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The assumptions on power-on reset assertion are:

- The Cortex-M3 MPU subsystem is held in reset by the PRCM module and the CORTEXM3_PWRON_RST, CORTEXM3_RET_RST, CORTEXM3_RST1, CORTEXM3_RST2, and CORTEXM3_RST3 are asserted.

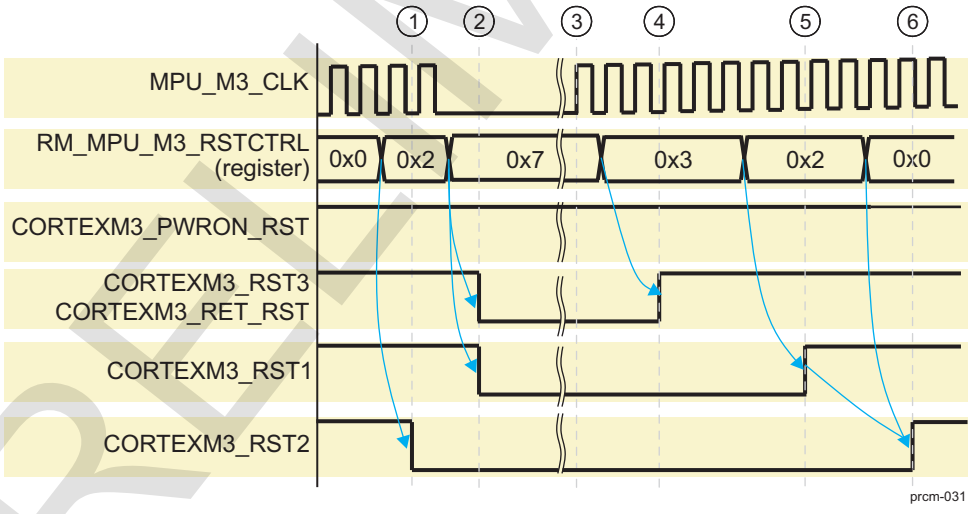
The power-on reset sequence is:

1. Software clears the RM_MPU_M3_RSTCTRL[2] RST3 bit in the PRCM module register to release from reset the MPU M3 Cache and MMU.
2. The PRCM module releases CORTEXM3_PWRON_RST once the reset manager counter (PRM_RSTTIME[14:10] RSTTIME2) has reached its limit and the MPU_M3_CLK is running. Upon the deassertion of the power-on reset signal, the Cortex-M3 MPU subsystem starts the CPU and MMU initialization sequence.
3. Once the reset sequence of Step 2 completes and the reset manager counter (PRM_RSTTIME[14:10] RSTTIME2) has expired, the PRCM module releases the CORTEXM3_RST3 and CORTEXM3_RET_RST signals.
4. The MPU software must configure the MMU once the MMU is out of reset. After MMU configuration and cache initialization is done, the MPU software clears the RM_MPU_M3_RSTCTRL[0] RST1 bit in the PRCM module register.
5. The PRCM module releases CORTEXM3_RST1, which causes the Cortex-M3 MPU Core 1 to start booting.
6. The MPU software can clear the RM_MPU_M3_RSTCTRL[1] RST2 bit in the PRCM module register so that the PRCM module releases the CORTEXM3_RST2 to the Cortex-M3 MPU Core 2.

3.5.6.12 Cortex-M3 MPU Subsystem Software Warm Reset Sequence

Figure 3-30 shows the software warm reset sequence of the Cortex-M3 MPU subsystem.

Figure 3-30. Cortex-M3 MPU Subsystem Software Warm Reset Sequence



The assumptions on power-on reset assertion are:

- The Cortex-M3 MPU Core 2 is in Idle state.

The power-on reset sequence is:

1. The Cortex-M3 MPU Core 1 software or Cortex-A9 MPU software sets the RM_MPU_M3_RSTCTRL[1] RST2 bit. The PRCM module asserts the CORTEXM3_RST2 reset signal to the Cortex-M3 Core 2.
2. The Cortex-A9 MPU cuts the MPU_M3_CLK and software sets the RM_MPU_M3_RSTCTRL[2] RST3 and RM_MPU_M3_RSTCTRL[0] RST1 bits.
3. The PRCM module asserts the CORTEXM3_RST3, CORTEXM3_RET_RST, and CORTEXM3_RST1 reset signals. The CORTEXM3_PWRON_RST remains deasserted in this case.
4. The MPU software re-enables the MPU_M3_CLK and the initialization sequence starts inside

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Cortex-M3 subsystem. Software clears the RM_MPU_M3_RSTCTRL[2] RST3 bit in the PRCM module register.

5. Once the reset sequence of Step 4 completes and the reset manager counter (PRM_RSTTIME[14:10] RSTTIME2) has expired, the PRCM module releases CORTEXM3_RST3, CORTEXM3_RET_RST, and CORTEXM3_RST1 reset signals. The Cortex-M3 MPU Core 1 starts rebooting.
6. Software can then clear the RM_MPU_M3_RSTCTRL[1] RST2 bit in the PRCM module register.. The PRCM module releases the CORTEXM3_RST2 reset signal to the Cortex-M3 MPU Core 2 to start booting.

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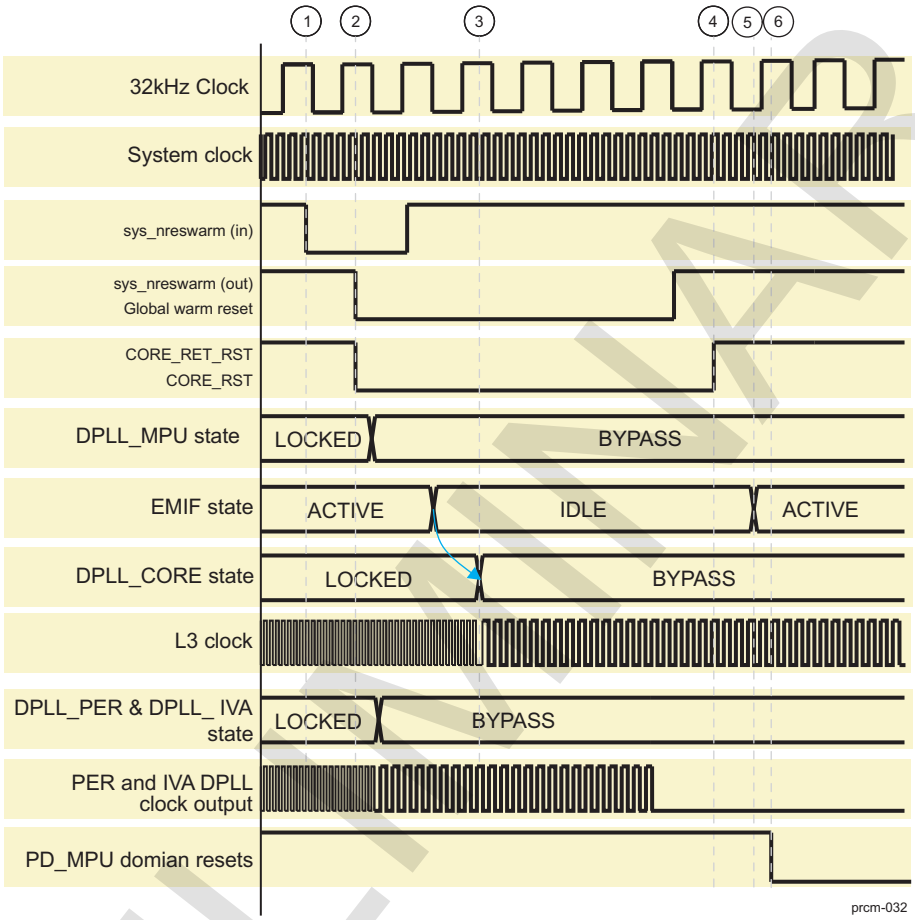
3.5.6.13 Global Warm Reset Sequence

This section describes the global warm reset sequence.

Figure 3-31 shows the global warm reset sequence.

Figure 3-31. Global Warm Reset Sequence



The assumptions are:

- All the logic and memory voltage sources are at their nominal voltage levels.
- The device is active:
  - All resets are released.
  - MPU, CORE, and DSP DPLLs are locked.

The steps of a global warm reset sequence are:

1. On assertion of any global warm reset source the PRM signals the EMIF that a global warm reset event has occurred. The EMIF initiates IDLE state transition. The PRCM module delays global warm reset to the device for minimum 16 L3 clock cycles so that the EMIF switches to IDLE state and switches the external SDRAM memory to self-refresh mode.
2. The reset managers in PRM assert the following resets:
   - The external warm reset SYS_WARM_RST (output) to the SCRM.
   - All power domain warm resets are asserted.
   - DPLL resets are not asserted.
     - DPLL_MPU transitions to bypass mode.
     - DPLL_CORE transitions to bypass mode once the EMIF has switched to IDLE state.
     - DPLL_IVA and DPLL_PER transition to bypass mode.

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  - DPLL_ABE configuration is not changed.
- The system clock remains active.
- The PRM and CM registers, sensitive to warm reset, are asynchronously reset.
- CM gates the clocks not needed, as per their default reset setting in the associated registers.

3. After the warm reset source is released, the global warm reset and extended until the following conditions are met:
   - Device reset manager counter overflows. It is set up by the PRM_RSTTIME[9:0] RSTTIME1 bit field.

     During this time, the DPLL_ABE control registers are reset and DPLL_ABE transitions to bypass mode when the system clock restarts and the DPLL_ABE outputs are no longer used.
   - All logic voltage sources (VDD_IVA, VDD_MPU, and VDD_CORE) are stable.

   NOTE: Voltage stabilization is an additional condition if voltage scaling was performed before the assertion of the warm reset.
4. The CORE power domain is released from reset (that is, warm reset sensitive modules in the CORE power domain).
5. The PRCM module switches the EMIF back to ACTIVE state from IDLE state.
6. PD_MPU is released from reset when the clocks to the Cortex-A9 MPU subsystem are active. The Cortex-A9 MPU reboots.

NOTE:

- PD_DSP and PD_IVAHD power domains are held under reset after global warm reset by assertion of the software source of the reset.
- PD_L4_PER, PD_L3_INIT, PD_DSS, PD_SGX, and PD_CAM are held under reset after global warm reset until the PRCM module enables their interface clock.
- The reset to the standard eFuse power domain, PD_STD_EFUSE, is not asserted on a global warm reset.

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3.6 Clock Management Functional Description

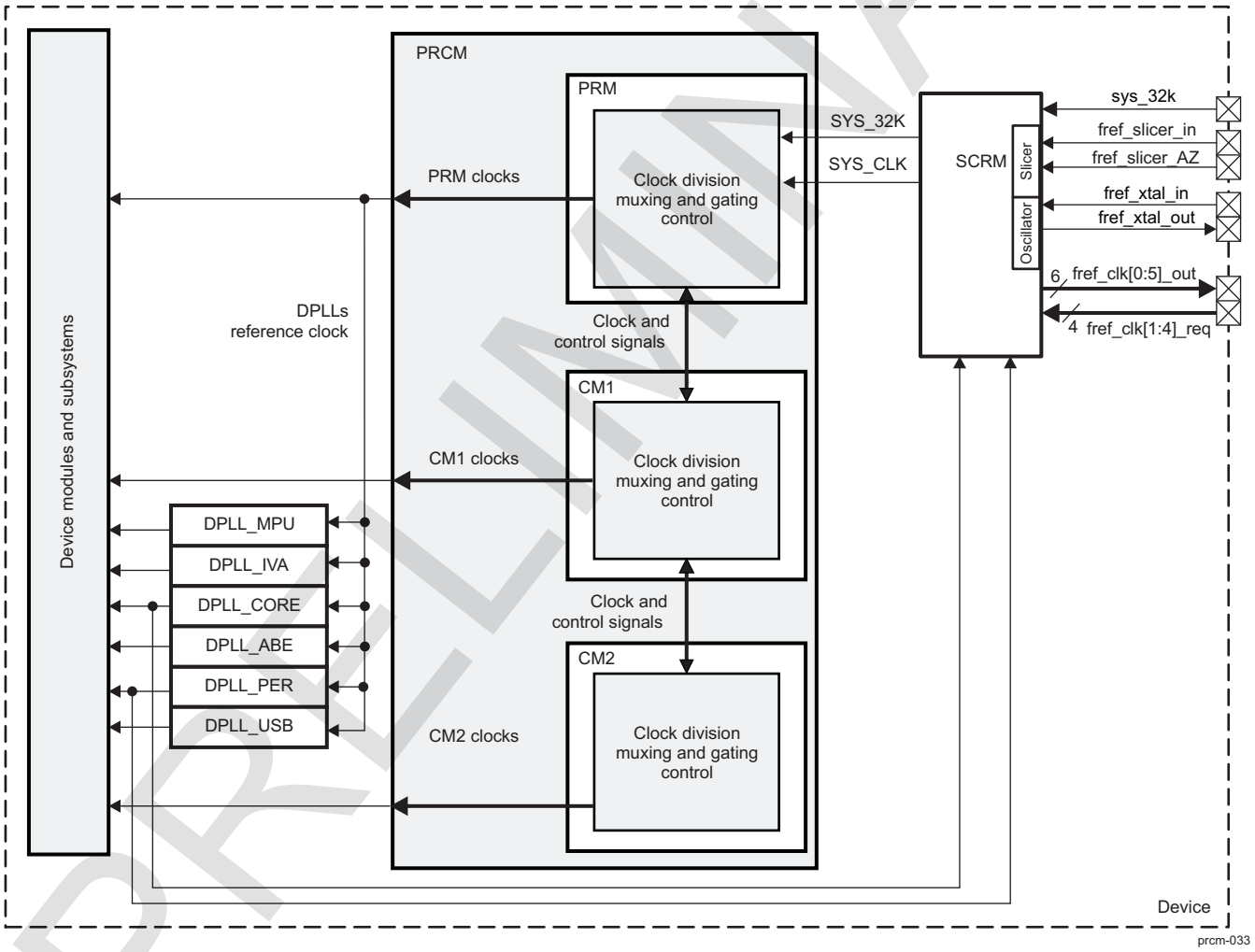
3.6.1 Overview

The PRCM module provides control for clock generation, division, distribution, synchronization, and gating. It distributes the clock sources to all modules in the device. See Section 3.1.1.1, *Clock Management*, for information on the clock-management functional architecture of the device.

The high-frequency system clock is received by the device from an external source or generated within the device (internal oscillator) by the SCRM. The SCRM also receives the 32-kHz low-frequency clock from the external source.

The stable versions of the system and 32-kHz clock are provided by the SCRM to the PRCM module. The PRCM module provides clocks to the internal DPLLs for internal high-frequency clocks generation. Clock division and gating are handled by the PRM, the CM1 and CM2 sections of the PRCM module. Figure 3-32 shows the high-level clock-management scheme in the device.

Figure 3-32. PRCM Module Clock Manager Overview



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3.6.2 External Clock Inputs

3.6.2.1 sys_32k Clock Input

The 32-kHz frequency is used for low-frequency operation (timer, debouncing, etc.). It supplies the wake-up domain for operation in lowest power mode and as clock source to the DPLL_ABE module (for audio back-end [ABE]).

3.6.2.2 High-Frequency System Clock Input

The system clock, SYS_CLK, is the main source clock of the device. SYS_CLK is received directly from the SCRM by the PRM subsection of the PRCM module. It is supplied as the reference clock to the DPLLs as well as functional clock to several modules.

3.6.3 Internal Clock Sources/Generators

The PRCM module clock sources/generators are split into the following parts:

- PRM clock source that receives the 32-kHz and system clocks from SCRM
- CM1 and CM2 clock sources that distribute high-frequency clocks
- DPLL clock generators that synthesize high-frequency clocks for the device

3.6.3.1 PRM Clock Source

The PRM clock source receives the SYS_32K and SYS_CLK clocks from the SCRM. It sources various versions (through gating controls) of these clocks to supply:

- PRCM-managed DPLLs with a reference clock, which is permanently supplied with always-on buffers
- The SR modules with a reference clock, which is permanently supplied with always-on buffers
- The DSS with a reference clock, which is permanently supplied with always-on buffers
- eFuse controller clocks (gated SYS_CLK clock), which are permanently supplied with always-on buffers
- The clocks for CM clock generator and the CORE power domain
- A version of SYS_CLK to ABE supplied by always-on buffers

Figure 3-33 and Figure 3-34 present a logical representation of the PRM clock source.

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Figure 3-33. PRM Clock Manager Overview (a)

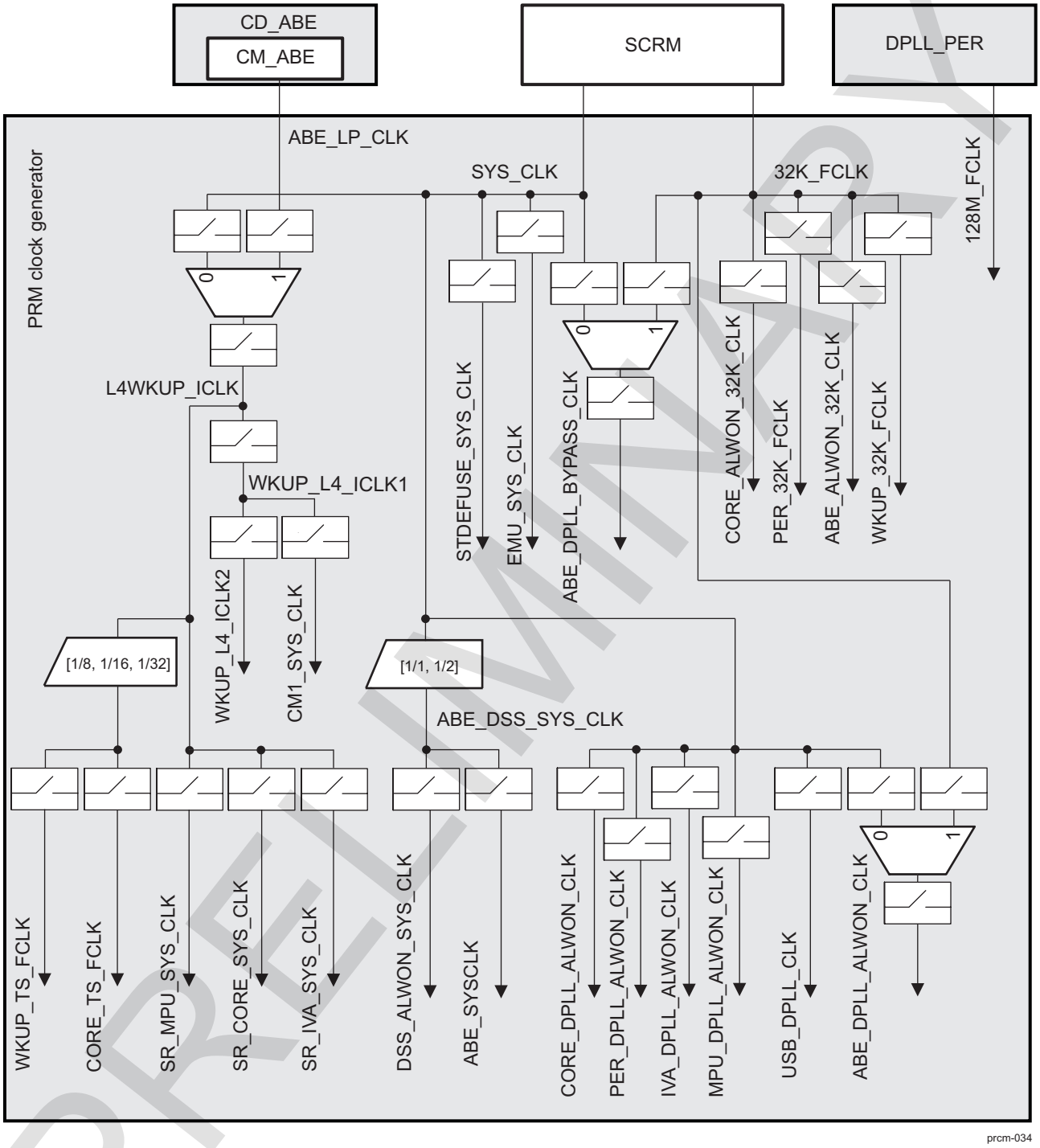

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Figure 3-34. PRM Clock Manager Overview (b)

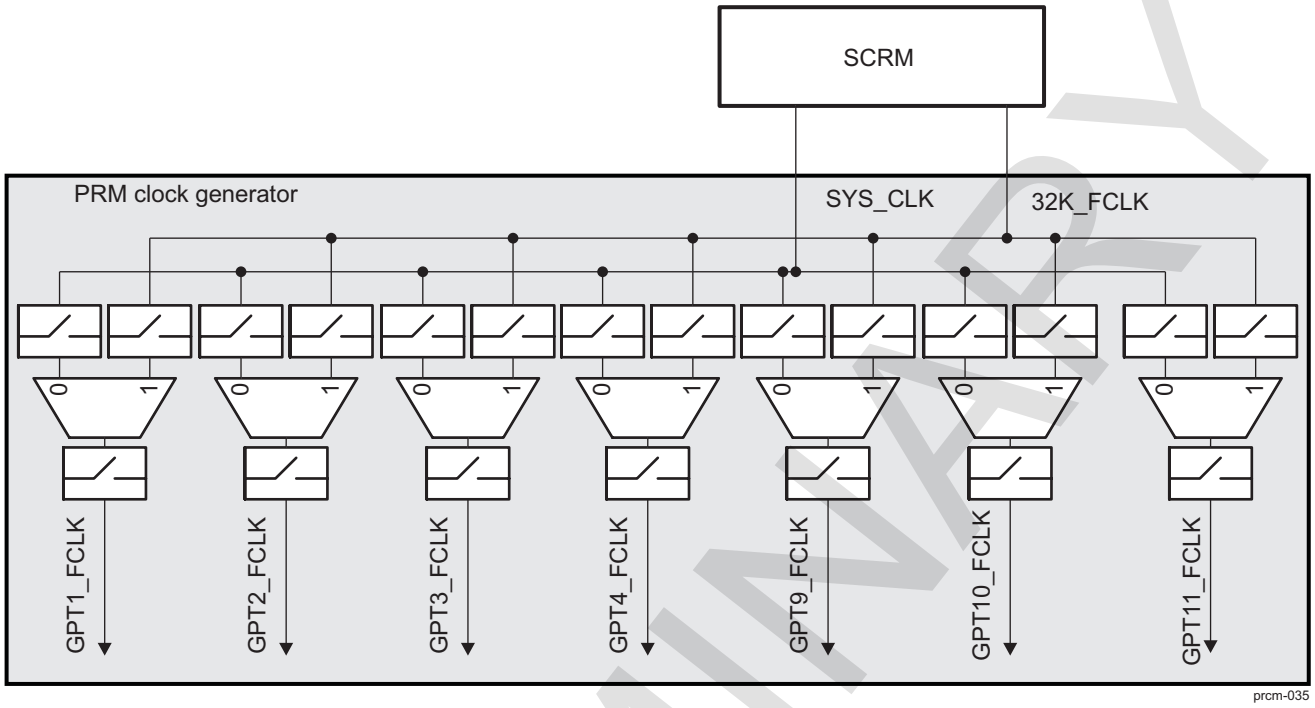

Table 3-36 identifies controls for clock dividers or muxes in the PRM.

Table 3-36. PRM Clock Division and Muxing Control

Divider/Mux	Control Bit Field
Mux ABE_DPLL_ALWON_CLK	CM_ABE_PLL_REF_CLKSEL[0] CLKSEL
Mux GPT1_FCLK	CM_WKUP_GPTIMER1_CLKCTRL[24] CLKSEL
Mux GPT2_FCLK	CM_L4PER_GPTIMER2_CLKCTRL[24] CLKSEL
Mux GPT3_FCLK	CM_L4PER_GPTIMER3_CLKCTRL[24] CLKSEL
Mux GPT4_FCLK	CM_L4PER_GPTIMER4_CLKCTRL[24] CLKSEL
Mux GPT9_FCLK	CM_L4PER_GPTIMER9_CLKCTRL[24] CLKSEL
Mux GPT10_FCLK	CM_L4PER_GPTIMER10_CLKCTRL[24] CLKSEL
Mux GPT11_FCLK	CM_L4PER_GPTIMER11_CLKCTRL[24] CLKSEL
Mux L4WKUP_ICLK	CM_L4_WKUP_CLKSEL[0] CLKSEL
Mux ABE_DPLL_BYPASS_CLK	CM_L4_WKUP_CLKSEL[0] CLKSEL
Divider WKUP_TS_FCLK, CORE_TS_FCLK	CM_WKUP_BANDGAP_CLKCTRL[25:24] CLKSEL

PRM provides 32-kHz gated and ungated clock for use by portions of PD_WKUP power domain and some peripherals outside the PD_WKUP power domain.

It also provides the system clock to the display subsystem (DSS), and gated and buffered version to L4WKUP_ICLK interconnect clock, and the DPLLs controlled by the PRCM module. The gated version of the SYS_CLK is also provided to the SmartReflex modules of the device.

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3.6.3.2 CM Clock Source

The clock manager (CM) is primarily responsible for generating interface and functional clocks from the internal clocks provided by DPLL_CORE and DPLL_PER. The CM is physically divided into two independent entities, CM1 placed in PD_ALWON_CORE always-on power domain and CM2 placed in PD_CORE switchable power domain. The split is done to provide control over various entities like modules, DPLLs and clocks during low power use case scenarios when the PD_CORE power domain can be switched to RETENTION state.

3.6.3.2.1 CM1 Clock Generator

CM1 receives system clock from the PRM, which serves as its functional clock. CM1 provides gated clock to PD_AUDIO and some DPLLs. It also provides clock to the L3 and L4 interconnects in the device.

Figure 3-35 shows the various functional and interface clocks generated by CM1:

Figure 3-35. CM1 Overview

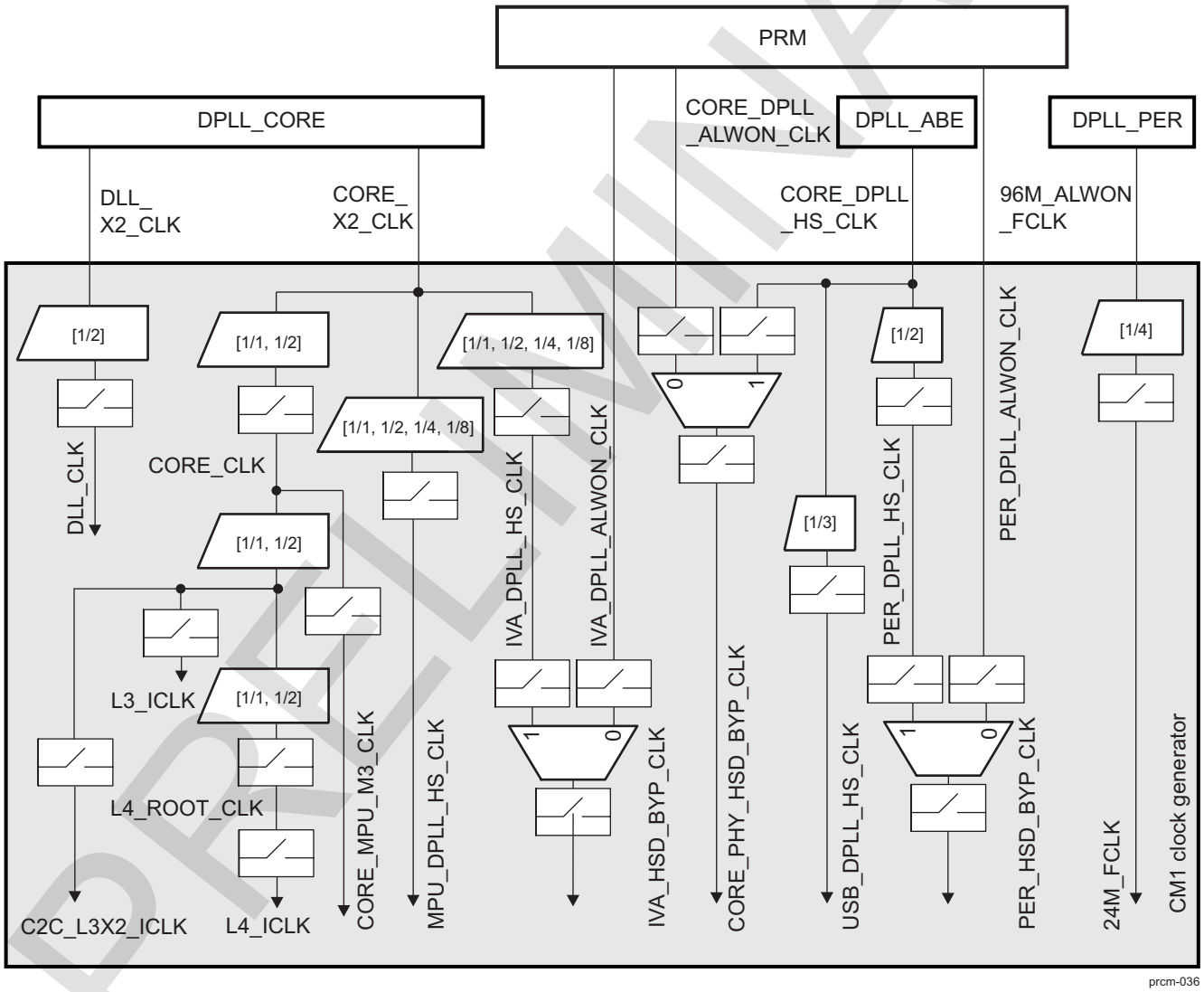

Table 3-37 identifies controls for clock dividers or muxes in the CM1 clock source.

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Table 3-37. CM1 Clock Division and Muxing Control

Divider/Mux	Control Bit Field
Divider CORE_CLK	CM_CLKSEL_CORE[0] CLKSEL_CORE
Divider L3_ICLK	CM_CLKSEL_CORE[4] CLKSEL_L3
Divider L4_ROOT_CLK	CM_CLKSEL_CORE[8] CLKSEL_L4
Divider MPU_DPLL_HS_CLK	CM_BYPCLK_DPLL_MPU[1:0] CLKSEL
Divider IVA_DPLL_HS_CLK	CM_BYPCLK_DPLL_IVA[1:0] CLKSEL
Mux IVA_HSD_BYP_CLK	CM_CLKSEL_DPLL_IVA[23] DPLL_BYP_CLKSEL
Mux PER_HSD_BYP_CLK	CM_CLKSEL_DPLL_PER[23] DPLL_BYP_CLKSEL
Mux CORE_PHY_HSD_BYP_CLK	CM_CLKSEL_DPLL_CORE[23] DPLL_BYP_CLKSEL

3.6.3.2.2 CM1_USB Clock Generator

CM_USB receives system clock from USBPHY and DPLL_USB. It provides gated clock to CD_L3_INIT.

Figure 3-36 shows the various functional and interface clocks generated by CM1_USB:

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Figure 3-36. CM1_USB Clock Manager Overview

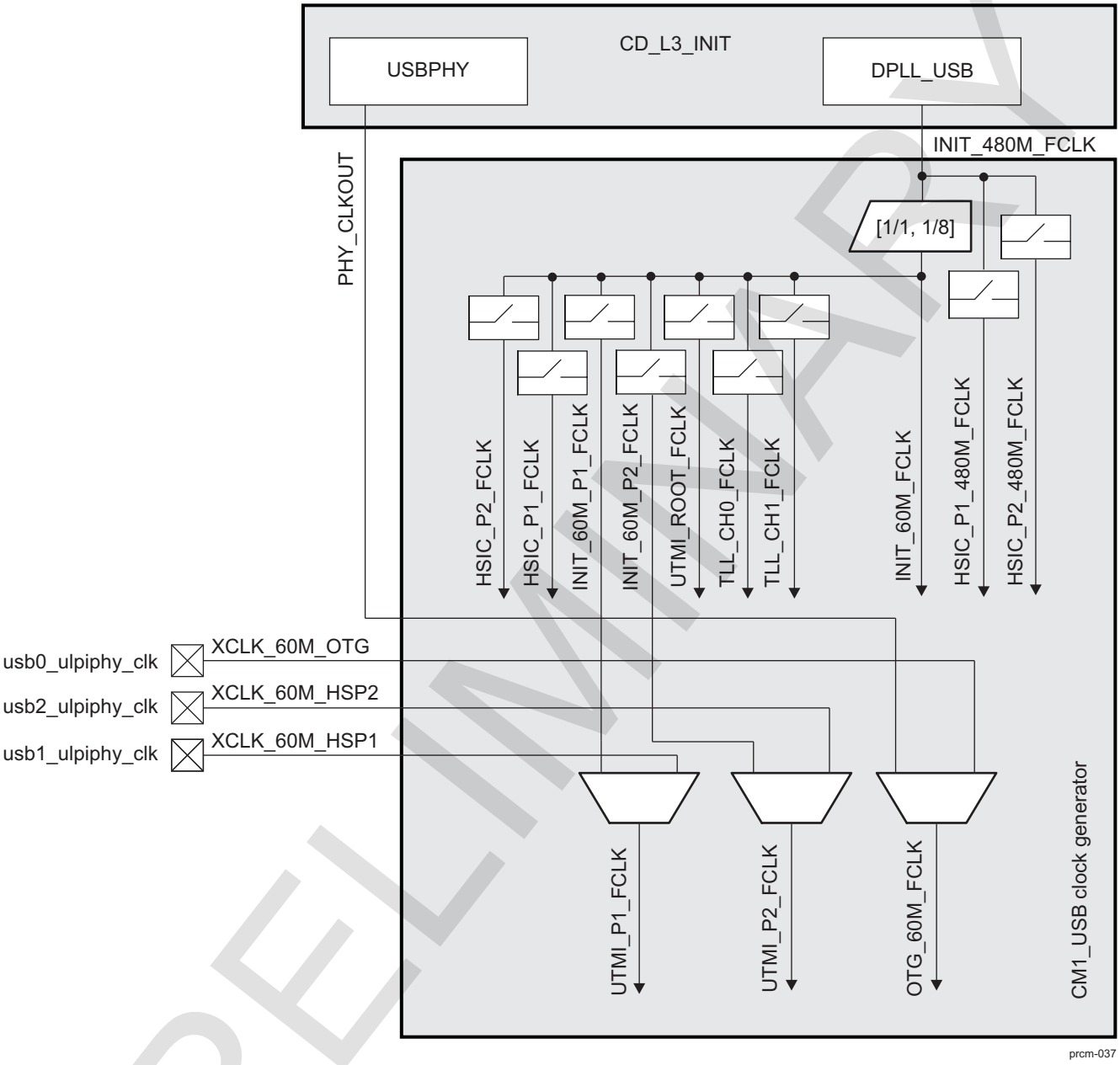

Table 3-38 identifies controls for clock dividers or muxes in the CM1_USB clock source.

Table 3-38. CM1_USB Clock Division and Muxing Control

Divider/Mux	Control Bit Field
Divider INIT_60M_FCLK	CM_CLKSEL_USB_60MHZ[0] CLKSEL
Mux UTMI_P1_FCLK	CM_L3INIT_HSUSBHOST_CLKCTRL[24] CLKSEL_U TMI_ P1
Mux UTMI_P2_FCLK	CM_L3INIT_HSUSBHOST_CLKCTRL[25] CLKSEL_U TMI_ P2
Mux OTG_60M_FCLK	CM_L3INIT_HSUSBOTG_CLKCTRL[24] CLKSEL_6 0M

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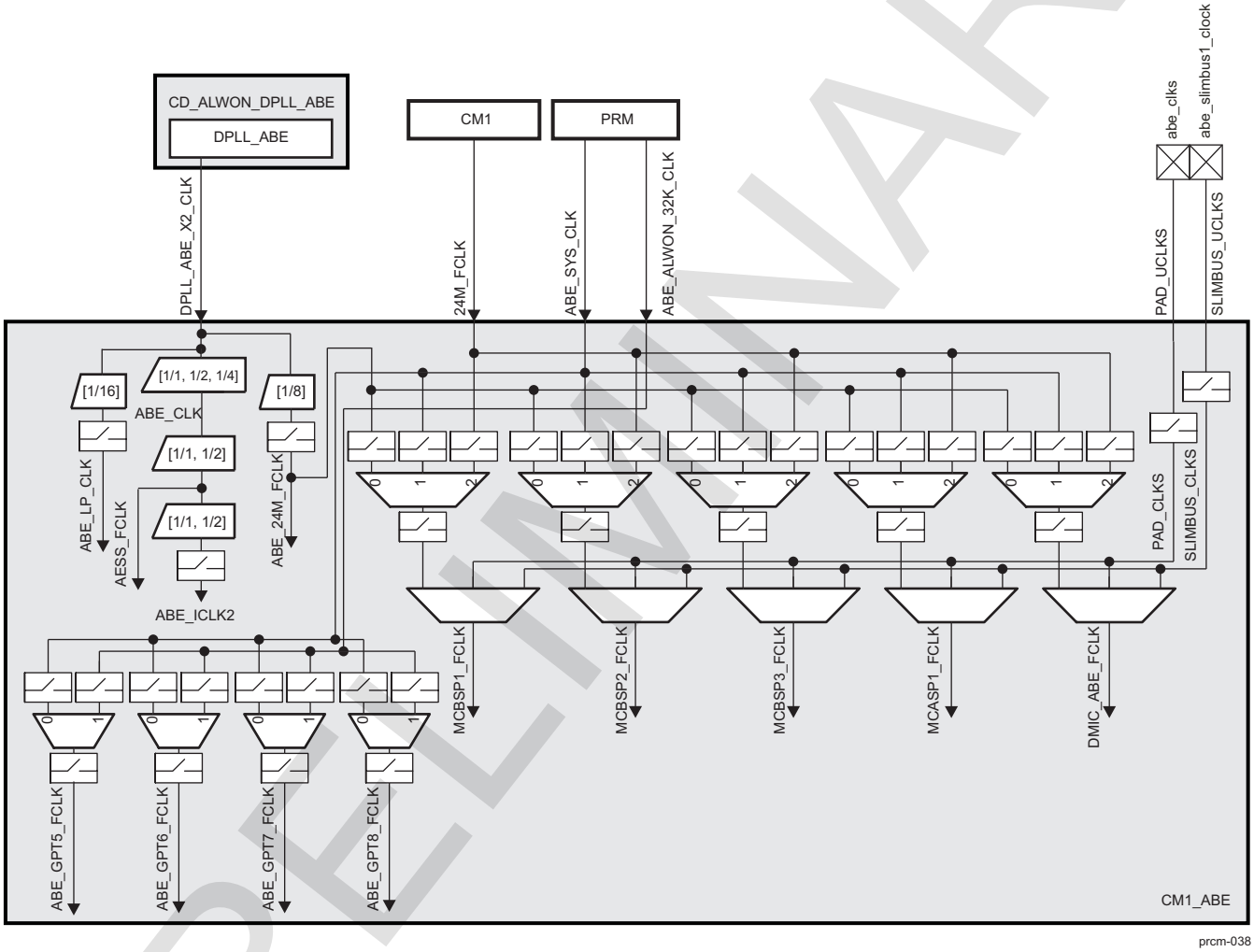
NOTE: For the clock status bits see Table 3-120

3.6.3.2.3 CM1_ABE Clock Generator

CM1_ABE receives system clock from PRM. It provides gated clock to CD_L4_PER.

Figure 3-37 show the various functional and interface clocks generated by CM1_ABE clock source.

Figure 3-37. CM1_ABE Clock Manager Overview



prcm-038

Table 3-39 identifies controls for clock dividers or muxes in the CM1_ABE.

Table 3-39. CM1_ABE Clock Division and Muxing Control

Divider/Mux	Control Bit Field
Clock switch PAD_CLKS	CM_CLKSEL_ABE[8] PAD_ CLKS_GAT E
Clock switch SLIMBUS_CLKS	CM_CLKSEL_ABE[10] SLIMBUS_ CLK_GATE
Divider ABE_CLK	CM_CLKSEL_ABE[1:0] CLKSEL_OPP
Divider AESS_FCLK and ABE_ICLK2(1)	CM1_ABE_AESS_CLKCTRL[24] CLKSEL_AESS_FCLK
Mux ABE_GPT5_FCLK	CM1_ABE_GPTIMER5_CLKCTRL[24] CLKSEL
Mux ABE_GPT6_FCLK	CM1_ABE_GPTIMER6_CLKCTRL[24] CLKSEL
Mux ABE_GPT7_FCLK	CM1_ABE_GPTIMER7_CLKCTRL[24] CLKSEL

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Table 3-39. CM1_ABE Clock Division and Muxing Control (continued)

Divider/Mux	Control Bit Field
Mux ABE_GPT8_FCLK	CM1_ABE_GPTIMER8_CLKCTRL[24] CLKSEL
Mux DMIC_FCLK	CM1_ABE_DMIC_CLKCTRL[25:24] CLKSEL_SOURCE
Mux DMIC_INT_FCLK	CM1_ABE_DMIC_CLKCTRL[27:26] CLKSEL_INTERNAL_SOURCE
Mux MCASP_INT_FCLK	CM1_ABE_MCASP_CLKCTRL[27:26] CLKSEL_INTERNAL_SOURCE
Mux MCASP_FCLK	CM1_ABE_MCASP_CLKCTRL[25:24] CLKSEL_SOURCE
Mux MCBSP1_FCLK	CM1_ABE_MCBSP1_CLKCTRL[25:24] CLKSEL_SOURCE
Mux MCBSP1_INT_FCLK	CM1_ABE_MCBSP1_CLKCTRL[27:26] CLKSEL_INTERNAL_SOURCE
Mux MCBSP2_FCLK	CM1_ABE_MCBSP2_CLKCTRL[25:24] CLKSEL_SOURCE
Mux MCBSP2_INT_FCLK	CM1_ABE_MCBSP2_CLKCTRL[27:26] CLKSEL_INTERNAL_SOURCE
Mux MCBSP3_FCLK	CM1_ABE_MCBSP3_CLKCTRL[25:24] CLKSEL_SOURCE
Mux MCBSP3_INT_FCLK	CM1_ABE_MCBSP3_CLKCTRL[27:26] CLKSEL_INTERNAL_SOURCE

(1) ABE_ICLK2 depends on the divider settings of the AESS_FCLK and is always divided by 2 of the ABE_CLK. So when AESS_FCLK divider is set to 1, then ABE_ICLK2 divider is set to 2 and vice versa.

NOTE: For the ABE subsystem, functional clock DPLL_ABE_X2_CLK must be set to 196.608 MHz in DPLL_ABE. ABE_CLK, which is sourced by the DPLL_ABE_X2_CLK, can be configured in the CM_CLKSEL_ABE[1:0] CLKSEL_OPP bit field according to the OPP. AESS_FCLK can be the same as ABE_CLK or ABE_CLK divided by 2, depending on the CM1_ABE_AESS_CLKCTRL[24] CLKSEL_AESS_FCLK bit.

For more information about setting DPLL parameters, see Section Section 3.6.3.3.1.

3.6.3.2.4 CM2 Clock Generator

CM2 provides gated functional clocks to various modules of the device.

Figure 3-38 and Figure 3-39 show the various functional and interface clocks generated by CM2:

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Figure 3-38. CM2 Overview (a)

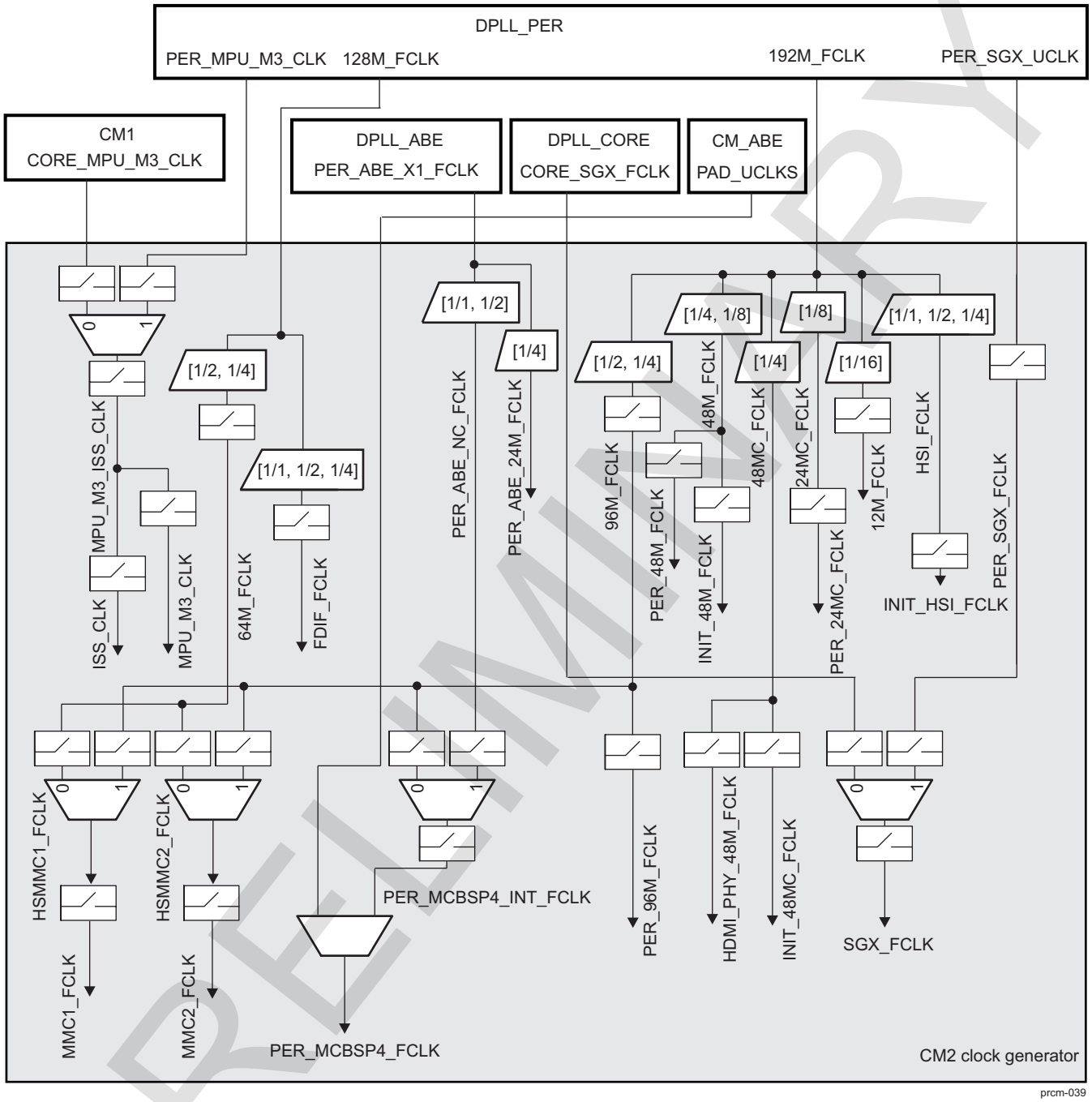

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Figure 3-39. CM2 Overview (b)

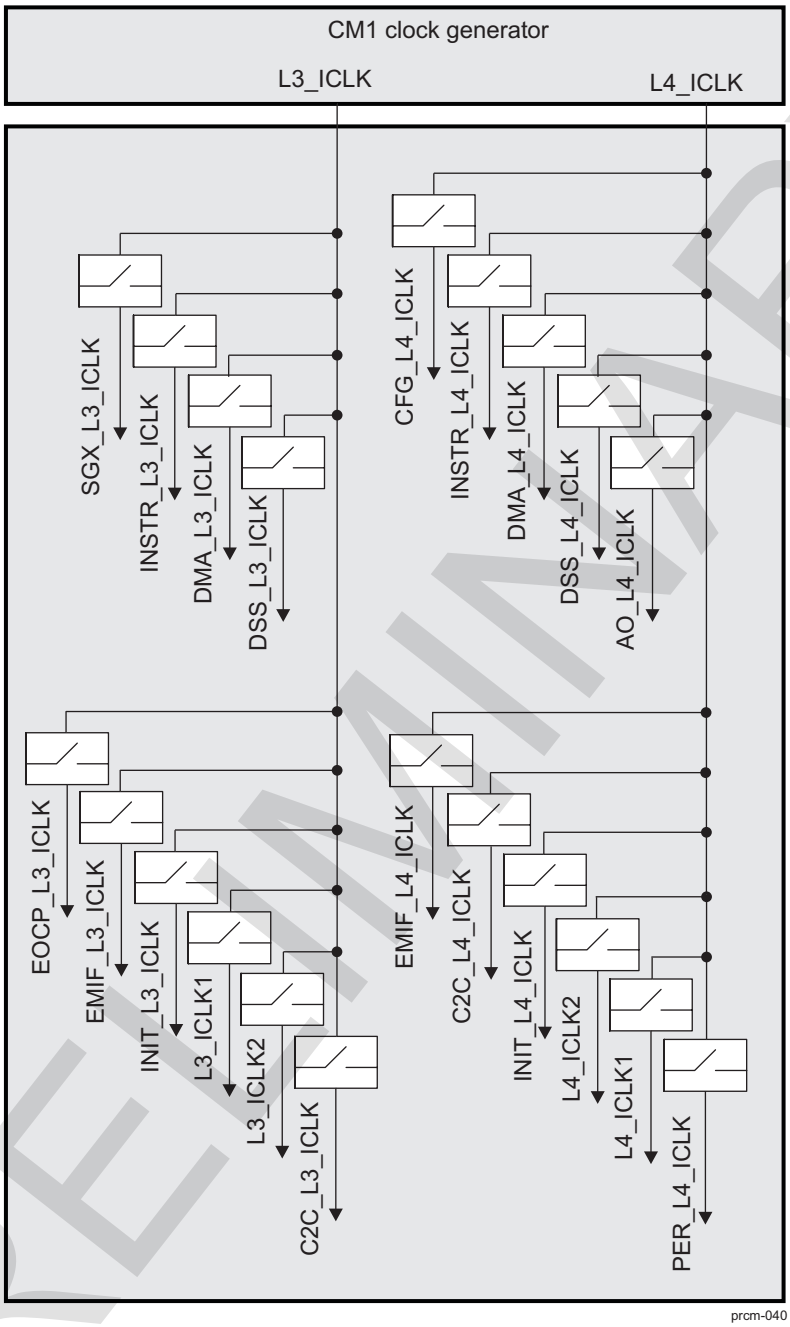

Table 3-40 identifies controls for clock dividers or muxes in the CM2 clock source.

Table 3-40. CM2 Clock Division and Muxing Control

Divider/Mux	Control Bit Field
Divider FDIF_FCLK	CM_CAM_FDIF_CLKCTRL[25:24] CLKSEL_FCLK
Divider HSI_FCLK	CM_L3INIT_HSI_CLKCTRL[25:24] CLKSEL
Mux HSMMC1_FCLK	CM_L3INIT_HSMMC1_CLKCTRL[24] CLKSEL
Mux HSMMC2_FCLK	CM_L3INIT_HSMMC2_CLKCTRL[24] CLKSEL
Mux MPU_M3_ISS_CLK	CM_CLKSEL_MPU_M3_ISS_ROOT[0] CLKSEL
Mux PER_MCBSP4_FCLK	CM_L4PER_MCBSP4_CLKCTRL[24] CLKSEL_SOURCE

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Table 3-40. CM2 Clock Division and Muxing Control (continued)

Divider/Mux	Control Bit Field
Mux PER_MCBSP4_INT_FCLK	CM_L4PER_MCBSP4_CLKCTRL[25] CLKSEL_INTERNAL_SOURCE
Mux SGX_FCLK	CM_SGX_SGX_CLKCTRL[24] CLKSEL_SGX_FCLK
Divider PER_ABE_NC_FCLK, 96M_FCLK, 64M_FCLK and 48M_FCLK	CM_SCALE_FCLK[0] SCALE_FCLK

3.6.3.3 Generic DPLL Overview

To generate high-frequency clocks, the device supports multiple on-chip DPLLs controlled directly by the PRCM module. They are of two types, identified as type A and type B DPLLs.

Following DPLLs belong to type A:

- DPLL_MPU
- DPLL_IVA
- DPLL_CORE
- DPLL_PER
- DPLL_ABE

Following DPLL belongs to type B:

- DPLL_USB

All DPLLs support the features presented in the following sections, unless identified otherwise.

NOTE: This chapter discusses only the DPLLs that are directly controlled by the PRCM module. The other DPLLs embedded in and managed by other subsystems are covered in the description of their respective subsystems. For example, Chapter 10, *Display Subsystem,* discusses the DPLL in the display subsystem.

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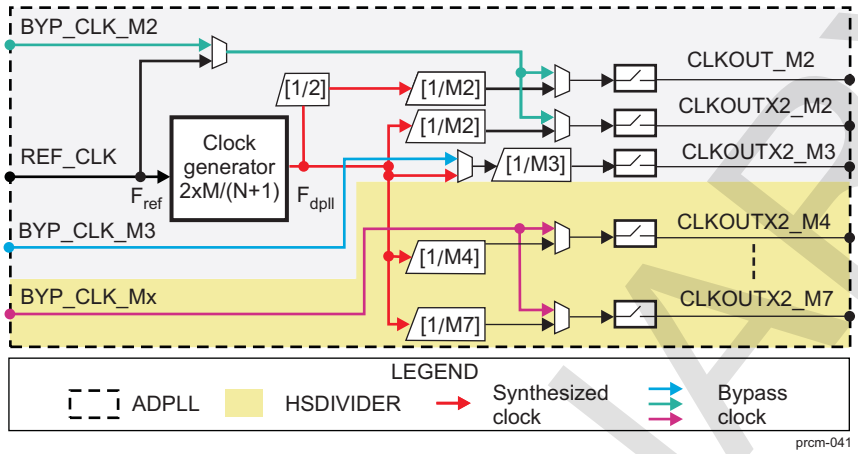
3.6.3.3.1 DPLLs Output Clocks Parameters

Figure 3-40 shows the functional architecture of a generic DPLL.

Figure 3-40. Generic DPLL Functional Diagram



The DPLL has three input clocks:

- REF_CLK: used to generated the synthesized clock but can also be used as the bypass clock for two outputs of the DPLL, whenever the DPLL enters a bypass mode. It is mandatory for the DPLL clock synthesis.
- BYP_CLK_M2: Selectable bypass clock for the output of an M2 post-divider (optional).
- BYP_CLK_M3: Selectable bypass clock for the output of an M3 post-divider (optional).

The DPLL can be programmed to be locked at any frequency given by the following equation:

- Fdpll = Fref x 2 x M/(N+1) or
- Fdpll = Fref x 2 x (4 x M/(N+1)) in case REGM4XEN bit field is set (only applicable to DPLL_ABE).

Where:

- Fdpll is the DPLL lock frequency.
- Fref is the REF_CLK frequency.
- M is the software-configured multiplication ratio binary value.
- N is the software-configured division ratio binary value.

It internally generates three main clocks: CLKOUT_M2, CLKOUTX2_M2, and CLKOUTX2_M3 as presented in Table 3-41.

Table 3-41. CLKOUT_M2, CLKOUTX2_M2, and CLKOUTX2_M3Frequencies With DPLL State

Output	Equation	DPLL Mode
CLKOUT_M2	Fdpll/(2 x M2)	Locked
	Fref or BYP_CLK_M2	Before lock or during relock
CLKOUTX2_M2	Fdpll/M2	Locked
	Frefl or BYP_CLK_M2	Before lock or during relock
CLKOUTX2_M3	Fdpll/M3 or BYP_CLK_M3/M3	Locked
	0	Before lock or during relock

Where:

- M2 is the software-configured division ratio binary value.
- M3 is the software-configured division ratio binary value.
- CLKOUT_M2 and CLKOUTX2_M2 bypass clock input can be switched when the DPLL is not in locked state, using the M2 Bypass Clock Select Control bit.

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- CLKOUTX2_M3 output clock can be switched when the DPLL is in locked state, using the M3 Clock Select Control bit.

NOTE:

- Zero-value for M2 and M3 division ratios is not allowed. They are set to 1 after reset.
- CLKOUT_M2 is generated based on a fix divide-by-2 ratio, except in bypass mode.

NOTE: The following rules apply for the DPLL internal clock, Fint = CLKINP / (N + 1):

- CLKINP / (N + 1) must be between 0.032 and 52 MHz for DPLL_MPU, DPLL_IVA, DPLL_ABE, DPLL_CORE, and DPLL_PER.
- CLKINP / (N + 1) must be between 0.5 and 2.5 MHz for DPLL_USB.

The DPLL may contain an HSDIVIDER module to produce more clocks with divided ratio based on the DPLL synthesized clock frequency. HSDIVIDER provides four extra post-dividers from M4 to M7. The HSDIVIDER output clocks frequency is given by the equations in Table 3-42:

Table 3-42. CLKOUTX2_Mn Frequencies With DPLL State

Equation	DPLL Mode
CLKOUTX2_Mn = Fdpll/Mn	Locked
CLKOUTX2_Mn = BYP_CLK_Mx	Before lock or during relock

Where:

- Fdpll is the DPLL lock frequency.
- Mn is the software configured division ratio binary value.
- n is in the range from 4 to 7.

NOTE: Mn division ratio is set to 1 after reset and 31 (0x1f) is an illegal value.

All clock outputs of the DPLL can be gated. The PRCM module provides the DPLL with a clock gating control signal to enable or disable the clock, and the DPLL provides the PRCM module with a clock activity status signal to let the PRCM module hardware know when the clock is effectively running or effectively gated.

The type B DPLL (only DPLL_USB) has two outputs: CLKOUT and CLKDCOLDO. The DPLL can be programmed to be locked with the output clock frequencies given by the following equation:

- Fclkout = Fref × (M / (N + 1)) × (1 / M2)
- Fclkdcoldo = Fref × (M / (N + 1))

Where:

- Fclkout is the frequency of the clock at output CLKOUT.
- Fclkdcoldo is the frequency of the clock at output CLKDCOLDO.
- Fref is the REF_CLK frequency.
- M is the software-configured multiplication ratio binary value.
- N is the software-configured division ratio binary value.
- M2 is the software-configured division ratio binary value.

  CLKOUT supports the same bypass modes as identified earlier. CLKDCOLDO does not support bypass mode.

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3.6.3.3.2 Enable Control, Status, and Low-Power Operation Mode

The DPLL has a Manual Mode Control bit field, which allows the setting of the different operating modes of the DPLL. When the DPLL is switched to lock mode the current values of the multiplication ratio (M) and the division ratio (N) are latched in the DPLL. The DPLL then starts the lock or relock sequence, to synthesize the corresponding output frequency clock.

The status of the synthesized clock output of the DPLL is represented by the CLKOUT status bit. It can be gated or active.

The DPLL can be switched to low-power operation mode (also called LPMODE) to optimize DPLL power consumption when the input and output clock frequencies are low. This mode can be software enabled using the low-power mode control bit of the DPLL.

It must only be enabled if both of the following operating conditions are satisfied:

- Fref/(N+1) is less than or equal to 1 MHz.
- Fref x M/(N+1) is less than or equal to 100 MHz.

With:

- Fref is the REF_CLK frequency.
- M is the software-configured multiplication ratio binary value.
- N is the software-configured division ratio binary value.

3.6.3.3.3 DPLL Power Modes

DPLL may supports several power modes. Each mode results in a tradeoff between power savings and relock time.

Table 3-43 shows the DPLL power modes.

Table 3-43. DPLL Power Modes

Power Mode	CLKOUT State	Logic Current (mA)	Analog Current (mA)	Freq Lock Time	Phase Lock Time
Low-power stop	Clock stopped	0.05 (leakage)	0.001 (leakage)	1.5 µs + (20 x 1/Fref)	1.5 µs + (100 x 1/Fref)
Fast-relock stop	Clock stopped	0.05 (leakage)	0.25 (leakage)	0.05 µs + (20 x 1/Fref)	0.05 µs + (100 x 1/Fref)
MN bypass	Bypass clock	0.05 (leakage)	0.001 (leakage)	1.5 µs + (350 x 1/Fref)	1.5 µs + (500 x 1/Fref)
Low-power bypass	Bypass clock/Clock stopped	0.05 (leakage)	0.001 (leakage)	1.5 µs + (20 x 1/Fref)	1.5 µs + (100 x 1/Fref)
Fast-relock bypass	Bypass clock/Clock stopped	0.05 (leakage)	0.25 (leakage)	0.05 µs + (20 x 1/Fref)	0.05 µs + (100 x 1/Fref)
Lock	Synthesized clock	0.55 (active)	1.95 (active)	N/A	N/A

Where:

- Fref is the REF_CLK frequency.

A DPLL power mode can be achieved on a software request (manual) and/or automatically (automatic), depending on the specific hardware conditions.

A DPLL can switch from one mode to the other as a result of the following:

- Software-programmed transition (manual): The software configures the dedicated DPLL Manual Mode Control feature for the next desired DPLL mode. It must ensure that the transition can be performed based on the clock activity on the device.
- Combined software-programmed and hardware-conditions-based transition (auto): This mode allows the DPLL to automatically transition to a low-power state (that is, any state other than MN BYPASS and the LOCK state) when the output clocks are gated or the destination clock domain is inactive. And to switch back to the LOCK state when the output clock is needed (that is, the clock is ungated or the clock domain becomes active). The desired low-power state for the automatic transition is configured in

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dedicated Auto Mode Control parameter of the DPLL.

NOTE: With REF_CLK period = 1/Fref = (N + 1)/CLKINP; (Fref = CLKINP/(N + 1)):

This formula indicates that a smaller N divider value provides a smaller time for switching the clock after an M2 post-divider change.

A compromise is necessary between the clock switching latency and power consumption. Having a smaller N value:

- Requires a higher M2 post-divider value to obtain the same target frequency.
- Results in a higher DPLL lock frequency, and then higher power consumption.

NOTE:

- A manual transition can be performed from any power mode to any other power mode.
- An automatic transition can be performed from lock mode to any low-power mode, except for the MN bypass mode.

3.6.3.3.4 DPLL Recalibration

Each time the DPLL is reset or performs a lock sequence (following a change in multiplier M or divider N value), it performs a recalibration of the output frequency, based on voltage and temperature conditions. In the locked mode the DPLL maintains a steady lock frequency output by compensating for voltage and temperature changes within a certain range. However, if the voltage or temperature drifts outside the range or shows a significant or fast change, the DPLL may not be able to track and compensate it. It would need a recalibration, which is signaled by assertion of a recalibration flag.

NOTE:

- The recalibration mechanism is active only while the DPLL is in locked mode. When the DPLL is in off or bypass mode (low-power or fast-relock), it does not assert the recalibration flag.
- If the DPLL drifts out of the operating range limits while not locked, then when it tries to relock it fails to lock within the normal delay and recalibrates automatically before eventually locking. The only difference between this case and a standard relock is the recalibration delay.

During recalibration, the DPLL loses lock and output clock switches to the bypass clock.

The DPLL can automatically start recalibration when the recalibration flag is asserted, or recalibration can be triggered by software control. The trigger setting of the recalibration can be configured by the corresponding registers of the DPLL in the PRCM module. The software-controlled recalibration mode is selected by default.

Software-controlled recalibration: The DPLL continues its tracking mechanism as long as the recalibration is not triggered by software (that is, by enabling the Recalibration-Enable control parameter). If the DPLL reaches upper or lower bounds of the DCO control code and software has still not triggered recalibration, the DPLL stops its tracking mechanism. The output clock remains active, but frequency and jitter are not ensured to meet the requirement.

Automatic recalibration: The DPLL immediately starts the recalibration as soon as the recalibration flag is asserted.

NOTE: Automatic recalibration of the DPLL can start at any time. While relocking, the DPLL switches to bypass mode, which introduces a frequency change. For modules that are sensitive to frequency change while operating, this can introduce operational instability. For example, the external memory (EMIF) controller is sensitive to a frequency change on the DPLL because its embedded DLL relocks on a frequency change. Any EMIF access during this DLL relock period can be corrupted. It is, therefore, important to stall EMIF access during DPLL recalibration.

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To allow the software to recalibrate the DPLL at the correct time depending on the device activity, the PRCM module can generate a wake-up event on processor power domain followed by an interrupt on the processor subsystem when the DPLL recalibration flag is asserted.

Table 3-44 shows the DPLL recalibration and control parameters.

Table 3-44. DPLL Recalibration Control Parameters

Parameter	Description
Recalibration-Enable control	Enable/disable the DPLL automatic recalibration feature.
Recalibration-Interrupt mask control	Mask/unmask the DPLL recalibration interrupt to processor.
Recalibration-Interrupt status	Status of the DPLL recalibration interrupt to processor

3.6.3.3.5 DPLL Spread Spectrum Clocking

The synthesized clock output of the DPLL has a stable frequency. This periodicity generates a significant power peak at the selected frequency, which in turn causes an electromagnetic interference (EMI) disturbance to the environment. In communication devices, this clock signal generates unwanted spurious signals that interfere with the decoding of information received. It results in performance degradation, for example, in the form of high bit-error rates in case of a wireless communication interface.

To reduce the power peaks (and the electromagnetic noise generated at a specific frequency), an internal frequency modulation of the DPLL is used to distribute the energy to many different frequencies, thus reducing the power peaks. This is called spread spectrum clocking (SSC).

SSC in the DPLL is performed by changing the feedback divider (M) in a triangular pattern. This varies the frequency of the output clock in a triangular pattern. The frequency of this pattern is the modulation frequency (fm). It is programmed as a ratio of the REF_CLK/4. This frequency modulation feature is integrated directly into some DPLLs of the device.

Figure 3-41 is a diagram of a DPLL that supports the SSC feature.

Figure 3-41. DPLL With SSC Reduction Feature

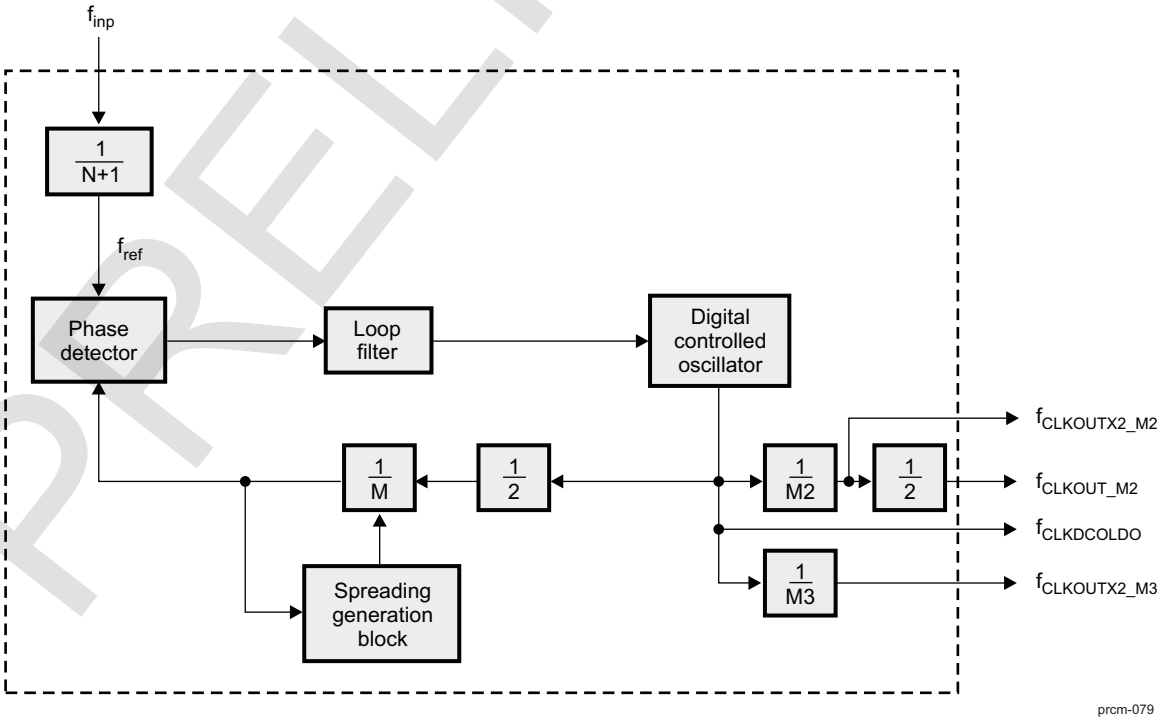

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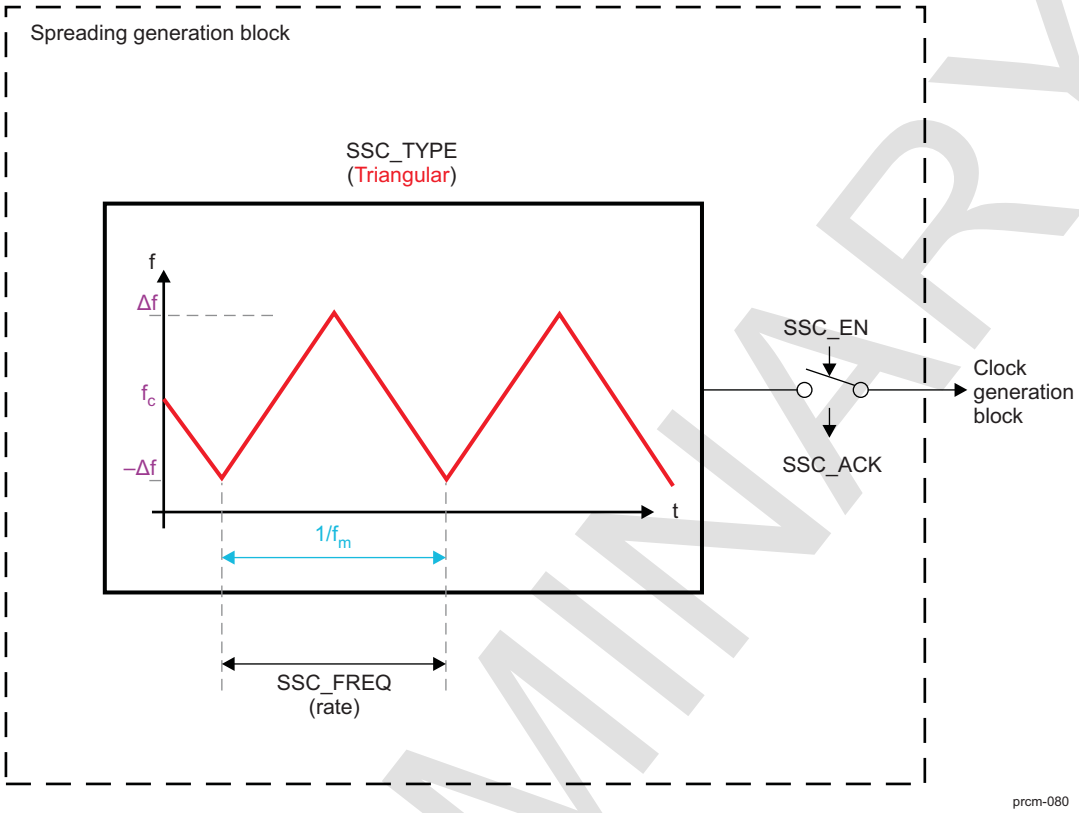
Figure 3-42 shows the spreading generation block diagram.

Figure 3-42. Spreading Generation Block Diagram



NOTE: Δf is the deviation from the center frequency. The total spreading deviation is equal to twice Δf. The peak (ΔM) or the amplitude of the triangular/square pattern as a percent of M is equal to the percent of the frequency spread (Δf), $\Delta M/M = \Delta f/f_c$.

f_c is the original output clock frequency.

f_m is the spreading frequency.

This additional block generates the required waveform used to reduce EMI. This waveform is then modulated with the initial signal to add some controlled deviation to the clock signal frequency, which spreads the energy of the clock and its harmonics into a band of frequencies, and then reduces EMI. SSC_DOWNSPREAD can control the position of the generated signal. It is controlled by the CM_CLKMODE_DPLL_<module>[14] DPLL_SSC_DOWNSPREAD bit of the corresponding registers (where <module> is the name of the concerned DPLLs). If the DOWNSPREAD bit is set to 1, the frequency spread on the lower side is twice the programmed value. The frequency spread on the higher side is 0.

The value of SSC_FREQ controls the rate of the generated signal. It can be programmed as a ratio of the reference clock: $f_{ref}/4$. The value that must be programmed is calculated as follows:

$ModFreqDivider = f_{ref}/(4 \times f_m)$

where $f_m < f_{ref}/70$, $f_{ref} = f_{inp}/(1 + N)$, and f_{inp} is the input clock for the DPLL

The ModFreqDivider is split into mantissa and exponent:

$ModFreqDivider = Mantissa \times 2^{Exponent}$

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The same value of ModFreqDivider can be obtained by different combinations of mantissa and exponent values. However, it is recommended to set the target ModFreqDivider by programming a maximum mantissa and a minimum exponent. This is controlled by the CM_SSC_MODFREQDIV_DPLL_<module>[10:8] MODFREQDIV_EXPONENT and CM_SSC_MODFREQDIV_DPLL_<module>[6:0] MODFREQDIV_MANTISSA bit fields of the corresponding registers (where <module> is the name of the concerned DPLL).

To define the modulation-frequency divider step size (ΔM) for triangular SSC, a DeltaMStep parameter must be programmed. DeltaMStep is split into integer and fractional parts. The step size can be calculated as follows:

ΔM = ModFreqDivider × DeltaMStep, if Exponent ≤3

ΔM = 8 × Mantissa × DeltaMStep, if Exponent > 3

It is controlled by the PRCM.CM_SSC_DELTAMSTEP_DPLL_<module>[19:0] DELTAMSTEP bit field of the corresponding register (where <module> is the name of the concerned DPLL). The PRCM.CM_SSC_DELTAMSTEP_DPLL_<module>[19:18] bit field defines the integer part, while the PRCM.CM_SSC_DELTAMSTEP_DPLL_<module>[17:0] bit field defines the fractional part. The DeltaMStep parameter must be programmed to define the modulation-frequency divider step size for trapezoidal SSC. It is split into integer and fractional parts. The step size can be calculated as follows:

ΔM = DeltaMStep

The DeltaMStep integer part is controlled by the CM_SSC_DELTAMSTEP_DPLL_<module>[19:14] bit field, while the fractional part is controlled by the CM_SSC_DELTAMSTEP_DPLL_<module>[13:0] bit field (where <module> is the name of the concerned DPLL).

The SSC_EN signal enables and disables the frequency modulation feature of the DPLL. It is controlled by the PRCM.CM_CLKMODE_DPLL_<module>[12] DPLL_SSC_EN bit of the corresponding registers (where <module> is the name of the concerned DPLL).

The SSC_ACK signal notifies of the exact start and SSC end of the DPLL. It can be read by the PRCM.CM_CLKMODE_DPLL_<module>[13] DPLL_SSC_ACK bit of the corresponding registers (where <module> is the name of the concerned DPLL).

The following restriction applies to the range of M values: M – ΔM must be ≥ 20. Also, M + ΔM must be ≤ 2045. If DOWNSPREAD is enabled, M – 2 × ΔM must be ≥ 20, and M ≤ 2045. In any case, the frequency modulation is programmed and does not generally have to be changed in real time.

Table 3-45 shows the DPLL SSC control parameters.

Table 3-45. DPLL SSC Control Parameters

Parameter	Description
SSC enable control	Enable/disable the DPLL SSC feature. When set to disable, SSC is disabled only after completion of one full cycle of the modulation pattern to maintain the average frequency.
SSC acknowledge	Notifies the exact start and end of SSC
Modulation Frequency Divider setting (Mantissa and Exponent)	Set the ratio of the modulation frequency with respect to the REF_CLK/4 frequency.
M step size setting (DeltaMStepInteger and DeltaMStepFraction)	Set the feedback divider variation step-size.

3.6.3.3.5.1 Definition

The SSC adds a variation to the frequency of an original clock, which spreads the generated interference over a larger band of frequencies.

In theory, SSC means that the clock signal is varied around the desired frequency. For example, for a 1-GHz clock, the frequency may be 999.5 MHz at one time and 1.0005 GHz at another time. Doing this constantly causes the power of the tone to be spread out more over a broader band of tight frequencies (centered at the desired tone). To realize this constant variation on the original signal, a modulation with an additional signal (called spreading waveform) is realized.

Creating an SSC by spreading the initial clock frequency is done by defining the following parameters:

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- The spreading frequency (deviation), which is the ratio of the range of spreading frequency over the original clock frequency
- The modulation rate (f_m), which is used to determine the clock-frequency spreading-cycling rate, and is the time during which the generated clock frequency varies through f and returns to the original frequency
- The modulation waveform, which describes the variation curve over time

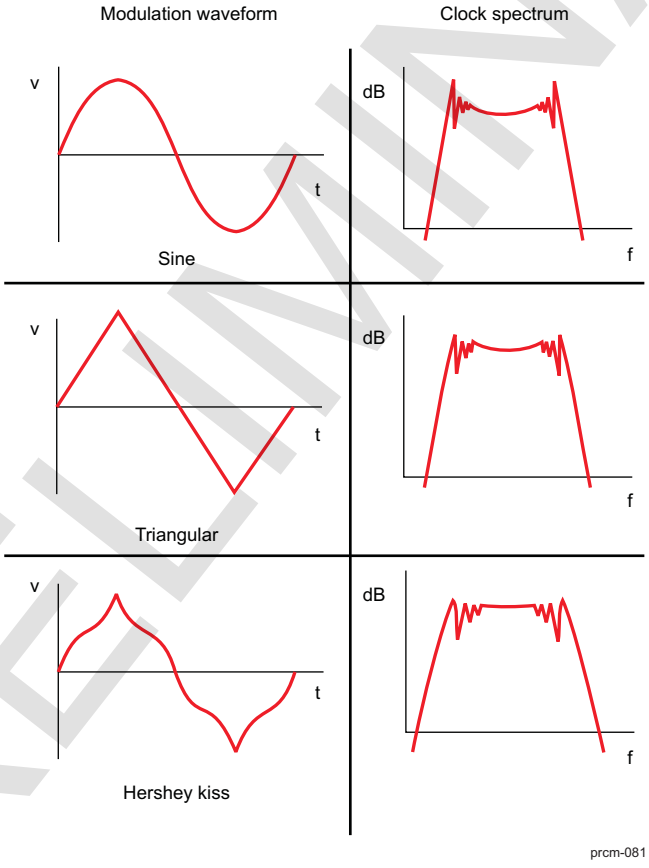
The spectral power reduction in the DPLL clocks is dependent on the modulation index (K), which is a ratio of spreading frequency, calculated from the frequency deviation (f) and the modulation rate (f_m).

3.6.3.3.5.2 Modulation Waveforms

The shape (profile) of the generated clock signal depends on the modulation waveform used during the frequency modulation. Several profiles can be used, according to the desired shaping for the energy spreading.

Figure 3-43 shows three examples of modulation waveforms and the spectrum of the corresponding modulated clock signal.

Figure 3-43. Modulation Profiles



The triangular wave gives a relatively flat spectrum and is easy to generate.

3.6.3.3.5.3 Effects on the Clock Signal

Figure 3-44 shows an example of the effect of triangular spreading on a clock signal.

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Figure 3-44. Effect of the SSC in Frequency

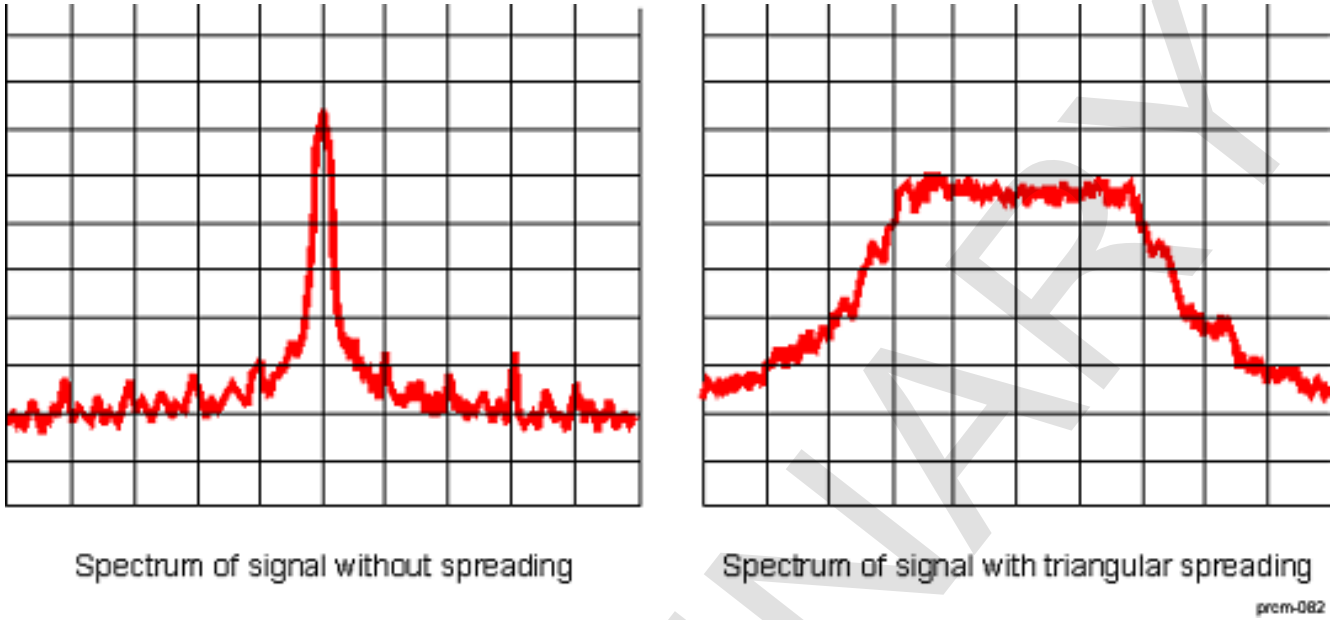
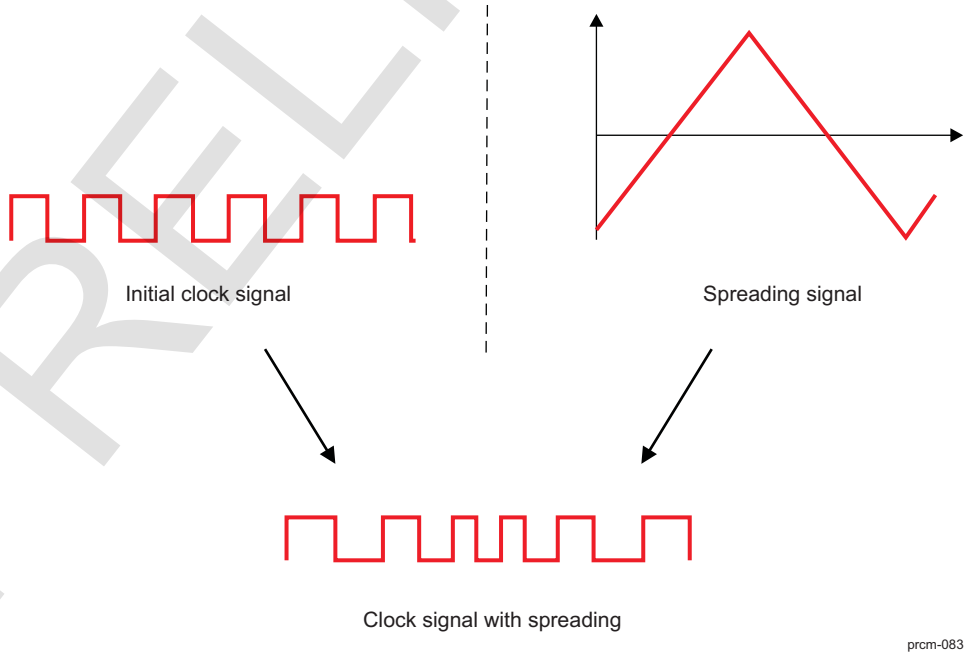


Figure 3-44 shows the power reduction of the main peak, and also the flatter aspect of the modulated signal. The minimum level of the second signal is higher than the first one. This effect is normal and is due to the noise added for the modulation.

NOTE: The spreading technique scatters the energy of the peaks on the other frequencies, which reduces the power of the peaks, but also increases the global noise of the signal.

Figure 3-45 shows the effect of triangular spreading on a clock signal in the time domain.

Figure 3-45. Effect of the SSC in the Time Domain



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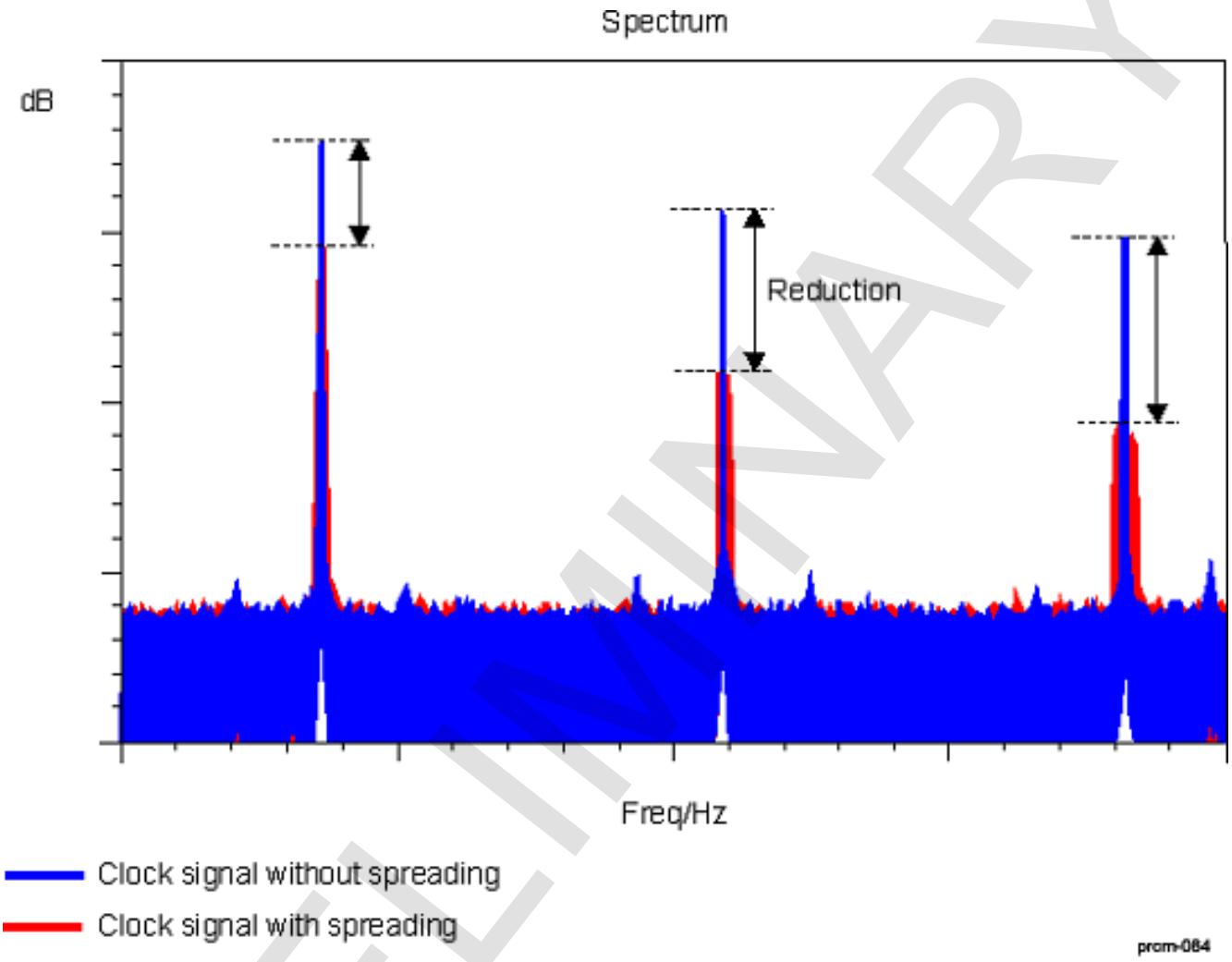
3.6.3.3.5.4 Estimation of the EMI Reduction Level

Figure 3-46 shows the effect of spreading on a clock and its harmonics.

Figure 3-46. Peaks Reduction Due to Spreading



EMI reduction can be estimated using the following equation:

(1) Peak_power_reduction = 10 × log ((Deviation × f_c)/f_m) – 10

Where:

- Peak_power_reduction in dB
- Deviation in percentage of the initial clock frequency (f_c), is equal to $\Delta f/f_c$.
- f_c is the original clock frequency, in MHz.
- f_m is the spreading frequency, in MHz.

According to equation (1), the deviation can also be calculated, and then f for a required reduction in peak-power:

(2) Deviation = (f_m/f_c) × $10^{((Peak_power_reduction + 10)/10)}$

Example:

For f_c = 160 MHz, Deviation = 1% peak from f_c (Δf = 1.6 MHz) and f_m = 16 kHz, the estimated peak power reduction is 10 dB.

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3.6.3.3.5.5 Bandwidth Calculation (Carson's Bandwidth Rule)

Carson's bandwidth rule defines the approximate bandwidth requirements of communications system components for a carrier signal that is frequency-modulated by a continuous or broad spectrum of frequencies rather than by a single frequency.

Carson's bandwidth rule is expressed by the relation CBR = 2 × (f + f_m), where CBR is the bandwidth requirement, f is the peak frequency deviation, and f_m is the highest frequency in the modulating signal. For example, an FM signal with a 5-kHz peak deviation and a maximum audio frequency of 3 kHz requires an approximate bandwidth of 2 × (5 + 3) = 16 kHz.

Theoretically, any FM signal has an infinite number of sidebands and, hence, an infinite bandwidth. In practice, all significant sideband energy (98 percent or more) is concentrated within the bandwidth defined by Carson's bandwidth rule.

3.6.3.3.5.6 SSC Configuration

The configuration of the spreading feature is not mandatory when programming the DPLL. This feature is usually enabled when the DPLL clocks generate harmonics, which can potentially interfere with the GSM carrier frequencies.

Once the clock generation control registers are configured, the spreading on the clock signal can be configured as follows:

1. Calculate ModFreqDivider and DeltaMStep based on the desired peak-power reduction.
2. Configure the MODFREQDIV_EXPONENT, MODFREQDIV_MANTISSA, and DELTAMSTEP bit fields according to the calculated values.
3. Enable the spreading using the DPLL_SSC_EN bit.

NOTE: Spreading on a clock must be carefully configured to avoid adding noise on frequencies that are used by another module. For example, adding spreading on a clock to reduce noise on GSM frequencies can move the generated noise to the frequency of the memory controller and thus degrade its performance.

Example:

For f_c = 160 MHz, Deviation = 1% peak from f_c (Δf = 1.6 MHz) and f_m = 16 kHz, the estimated peak power reduction is 10 dB.

The output clock can be calculated using the following equation: f_c= (f_{inp} × M)/((N + 1) × M2) (where M is a software-controlled multiplier, N is a software-controlled divider, M2 is a software-controlled output divider, f_c stands for f_{CLKOUT_M2}; for the calculation of other output clock frequencies and for more information, see , *DPLLs Output Clocks Parameters*, and the Clock Tree Tool).

The input clock is f_{inp} = 38.4 MHz. The following settings of the DPLL are required to have f_c = 160 MHz: M = 25, N = 2, M2 = 2. The value of M satisfies the restrictions: M – ΔM > = 20. Also, M + ΔM < = 2045.

f_{ref} can be calculated using the following equation:

f_{ref} = f_{inp}/(1 + N) = 12.8 MHz

ModFreqDivider can be calculated using the following equation:

ModFreqDivider = f_{ref}/(4 × f_m) = 200

The exponent and mantissa of ModFreqDivider can now be calculated (where ModFreqDivider = Mantissa × $2^{Exponent}$ and it must be used as the minimal value for the exponent):

Mantissa = 100, Exponent = 1

Knowing the deviation and M, ΔM can now be calculated:

ΔM/M = 1% ≥ ΔM = 0.01 × 25 = 0.25

DeltaMStep can be calculated as follows:

DeltaMStep = ΔM/ModFreqDivider = 0.00125

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The integer and fractional part of DeltaMStep can now be determined:

Integer part = 0, Fractional part = 0.00125 × 2^{18} = 327 (for an 18-bit fractional part)

The DPLL can be configured as follows:

- MODFREQDIV_EXPONENT = 1
- MODFREQDIV_MANTISSA = 100
- DELTAMSTEP = 327

The state of the modulation feature can be monitored with the DPLL_SSC_ACK bit of the corresponding register.

NOTE: Because this is in-band modulation for the DPLL, the modulation frequency must be within the DPLL loop bandwidth ($f_m < f_{ref}/70$). A higher modulation frequency results in less spreading in the output clock.

When deactivating the spreading (DPLL_SSC_EN = 0), the end-of-spreading is synchronous to the internal spreading cycle. Thus, there is no residual average frequency error.

3.6.3.3.6 DPLL Output Power Down

The DCO clock LDO (DCOCLKLDO) of the DPLL can be powered down if all output dividers of the DPLL are powered down. The PRCM module automatically re-enables the power to the LDO when an output divider is powered up or the DPLL switches to bypass mode.

Similarly, all the output dividers (M2, M3, and the Mn) can be powered down when their output clocks are gated and powered up when the clocks are needed again.

Table 3-46. DPLL Power-Down Control Parameters

Parameter	Description
DCO clock LDO power down control	Enable/disable automatic power-down feature if the all the output dividers are powered down.
M2, M3, and Mn (where n = 4 to 7)	Enables/disables automatic power-down feature of the corresponding output divider if the output clocks of the divider are gated.

3.6.3.3.7 DPLL Output Clock Gating

A clock gating control for DPLL output clocks allows selection between automatic clock gating and forcing the clock state. This control is done by the DPLL_CLKOUT_GATE_CTRL bit of the CM_DIV_Mn_DPLL name registers.

These bits are used for debug purposes. They are not required by any high-level operating system (HLOS). This does not apply to the CM_DIV_M3_DPLL_CORE[8] DPLL_CLKOUTHIF_GATE_CTRL and CM_DIV_M3_DPLL_PER[8] DPLL_CLKOUTHIF_GATE_CTRL bits. They enable the CORE_DPLL_SCRM_CLK and PER_DPLL_SCRM_CLK clocks that can be used as an SCRM auxiliary clock source.

3.6.3.4 DPLL_PER Description

3.6.3.4.1 Overview

Figure 3-47 shows the overview of the DPLL. See Section 3.6.3.3, *Generic DPLL Overview*, for a functional overview of a generic DPLL module.

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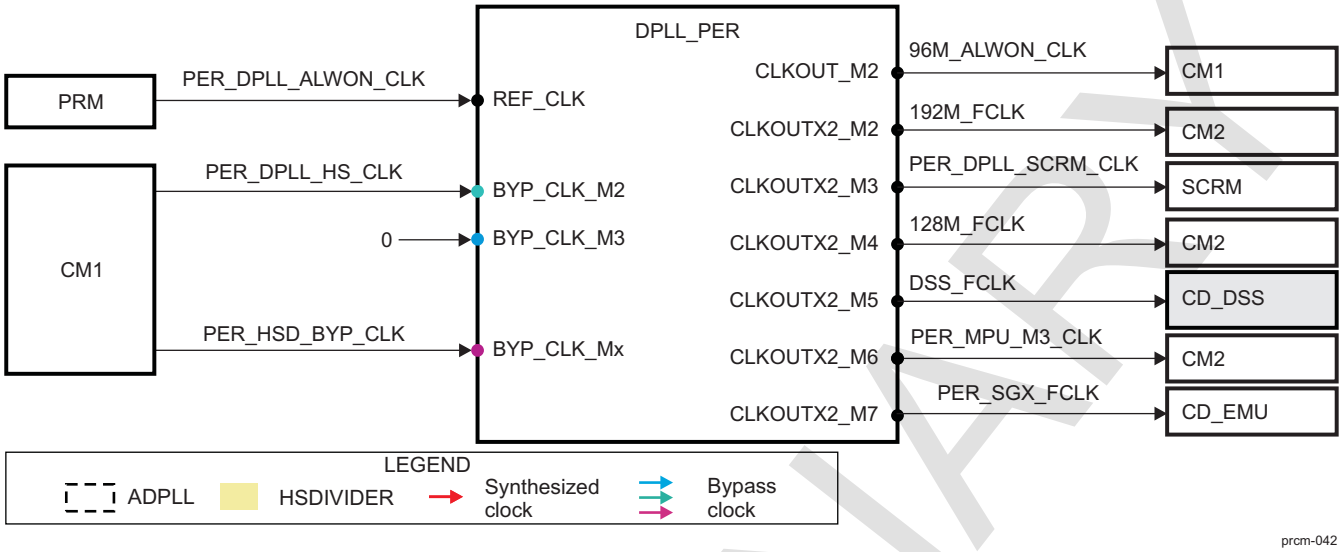
Figure 3-47. DPLL_PER Overview



3.6.3.4.2 Synthesized Clock Parameters

This section presents the clock synthesis and clock out divider parameters of the DPLL. See Section 3.6.3.3, *Generic DPLL Overview*, for an explanation of the clock synthesis and output divider parameters of the DPLL module.

Table 3-47 lists the clock synthesis parameters of the DPLL.

Table 3-47. DPLL_PER Clock Synthesis Parameters

Parameter Name	Control Bit Field
M	CM_CLKSEL_DPLL_PER[18:8] DPLL_MULT
N	CM_CLKSEL_DPLL_PER[6:0] DPLL_DIV

Table 3-48 lists the clock output divider parameters of the DPLL.

Table 3-48. DPLL_PER Clock Output Parameters

Clock Output/Divider	Parameter Name	Control/Status Bit Field
CLKOUT_M2	Status	CM_DIV_M2_DPLL_PER[9] ST_DPLL_CLKOUT
CLKOUT_M2	Gating Control	CM_DIV_M2_DPLL_PER[8] DPLL_CLKOUT_GATE_CTRL
CLKOUT_M2	Divider Acknowledge	CM_DIV_M2_DPLL_PER[5] DPLL_CLKOUT_DIVCHACK
CLKOUTX2_M2	Status	CM_DIV_M2_DPLL_PER[11] ST_DPLL_CLKOUTX2
CLKOUTX2_M2	Gating Control	CM_DIV_M2_DPLL_PER[10] DPLL_CLKOUTX2_GATE_CTRL
CLKOUT_M2	Divider Control	CM_DIV_M2_DPLL_PER[4:0] DPLL_CLKOUT_DIV
CLKOUTX2_M3	Status	CM_DIV_M3_DPLL_PER[9] ST_DPLL_CLKOUTHIF
CLKOUTX2_M3	Gating Control	CM_DIV_M3_DPLL_PER[8] DPLL_CLKOUTHIF_GATE_CTRL
CLKOUTX2_M3	Divider Acknowledge	CM_DIV_M3_DPLL_PER[5] DPLL_CLKOUTHIF_DIVCHACK

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Table 3-48. DPLL_PER Clock Output Parameters (continued)

Clock Output/Divider	Parameter Name	Control/Status Bit Field
CLKOUTX2_M3	Divider Control	CM_DIV_M3_DPLL_PER[4:0] DPLL_CLKOUTHIF_DIV
CLKOUTX2_M4	Status	CM_DIV_M4_DPLL_PER[9] ST_HSDIVIDER_CLKOUT1
CLKOUTX2_M4	Gating Control	CM_DIV_M4_DPLL_PER[8] HSDIVIDER_CLKOUT1_GATE_CTRL
CLKOUTX2_M4	Divider Acknowledge	CM_DIV_M4_DPLL_PER[5] HSDIVIDER_CLKOUT1_DIVCHACK
CLKOUTX2_M4	Divider Control	CM_DIV_M4_DPLL_PER[4:0] HSDIVIDER_CLKOUT1_DIV
CLKOUTX2_M5	Status	CM_DIV_M5_DPLL_PER[9] ST_HSDIVIDER_CLKOUT2
CLKOUTX2_M5	Gating Control	CM_DIV_M5_DPLL_PER[8] HSDIVIDER_CLKOUT2_GATE_CTRL
CLKOUTX2_M5	Divider Acknowledge	CM_DIV_M5_DPLL_PER[5] HSDIVIDER_CLKOUT2_DIVCHACK
CLKOUTX2_M5	Divider Control	CM_DIV_M5_DPLL_PER[4:0] HSDIVIDER_CLKOUT2_DIV
CLKOUTX2_M6	Status	CM_DIV_M6_DPLL_PER[9] ST_HSDIVIDER_CLKOUT3
CLKOUTX2_M6	Gating Control	CM_DIV_M6_DPLL_PER[8] HSDIVIDER_CLKOUT3_GATE_CTRL
CLKOUTX2_M6	Divider Acknowledge	CM_DIV_M6_DPLL_PER[5] HSDIVIDER_CLKOUT3_DIVCHACK
CLKOUTX2_M6	Divider Control	CM_DIV_M6_DPLL_PER[4:0] HSDIVIDER_CLKOUT3_DIV
CLKOUTX2_M7	Status	CM_DIV_M7_DPLL_PER[9] ST_HSDIVIDER_CLKOUT4
CLKOUTX2_M7	Gating Control	CM_DIV_M7_DPLL_PER[8] HSDIVIDER_CLKOUT4_GATE_CTRL
CLKOUTX2_M7	Divider Acknowledge	CM_DIV_M7_DPLL_PER[5] HSDIVIDER_CLKOUT4_DIVCHACK
CLKOUTX2_M7	Divider Control	CM_DIV_M7_DPLL_PER[4:0] HSDIVIDER_CLKOUT4_DIV

3.6.3.4.3 Power Modes

This section identifies the operating modes supported by the DPLL and also identify the control bit fields to set its operating modes. See Section 3.6.3.3.2, *Enable Control, Status and Low-Power Operation Mode*, and Section 3.6.3.3.3, *DPLL Power Modes*, for an explanation of the DPLL operating modes, and associated control and status features.

Table 3-49 lists the operating modes supported by the DPLL.

Table 3-49. DPLL_PER Modes

Low-Power Stop	Fast-Relock Stop	MN Bypass	Low-Power Bypass	Fast-Relock Bypass	Lock
Not available	Not available	Available (default)	Available	Available	Available

Table 3-50 lists the control bit fields for the operating mode control of the DPLL.

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Table 3-50. DPLL_PER Mode Control Parameters

Parameter Name	Control Bit Field
Low-Power Mode Control	CM_CLKMODE_DPLL_PER[10] DPLL_LPMODE_EN
Manual Mode Control	CM_CLKMODE_DPLL_PER[2:0] DPLL_EN
Auto Mode Control	CM_AUTOIDLE_DPLL_PER[2:0] AUTO_DPLL_MODE

3.6.3.4.4 Recalibration

Table 3-51 lists the control bit fields for the recalibration feature enable and interrupts of the DPLL. See Section 3.6.3.3.4, *DPLL Recalibration*, for an explanation of the DPLL recalibration feature.

Table 3-51. DPLL_PER Recalibration Feature Parameters

Parameter Name	Control/Status Bit Field
Recalibration - Enable Control	CM_CLKMODE_DPLL_PER[8] DPLL_DRIFTGUARD_EN
Recalibration - Interrupt Status	PRM_IRQSTATUS_MPU_A9[3] DPLL_PER_RECAL_ST
Recalibration - Interrupt MASK Control	PRM_IRQENABLE_MPU_A9[3] DPLL_PER_RECAL_EN
Recalibration - Interrupt Status	PRM_IRQSTATUS_MPU_M3[3] DPLL_PER_RECAL_ST
Recalibration - Interrupt MASK Control	PRM_IRQENABLE_MPU_M3[3] DPLL_PER_RECAL_EN

3.6.3.4.5 Spread Spectrum Clocking

Table 3-52 lists the control bit fields associated with the SSC features of the DPLL. See Section 3.6.3.3.5, *DPLL Spread Spectrum Clocking*, for an explanation of the DPLL SSC feature.

Table 3-52. DPLL_PER Spread-Spectrum Clocking Feature Parameters

Parameter Name	Control Bit Field
SSC Downspread	CM_CLKMODE_DPLL_PER[14] DPLL_SSC_DOWNSPREAD
SSC Acknowledge	CM_CLKMODE_DPLL_PER[13] DPLL_SSC_ACK
SSC Enable Control	CM_CLKMODE_DPLL_PER[12] DPLL_SSC_EN
Modulation Step Size Setting	CM_SSC_DELTAMSTEP_DPLL_PER[19:0] DELTAMSTEP
Modulation Frequency Divider - Exponent	CM_SSC_MODFREQDIV_DPLL_PER[10:8] MODFREQDIV_EXPONENT
Modulation Frequency Divider - Mantissa	CM_SSC_MODFREQDIV_DPLL_PER[6:0] MODFREQDIV_MANTISSA

3.6.3.4.6 Output Power Down

Table 3-53 lists the control bit fields for the output power down features of the DPLL. See Section 3.6.3.3.6, *DPLL Output Power-Down*, for an explanation of the DPLL output power down feature.

Table 3-53. DPLL_PER Clock Output Power-down Parameters

Parameter Name	Control/Status Bit Field
Clock Divider - HSDIVIDER-Power Down Control	CM_DIV_M4_DPLL_PER[12] HSDIVIDER_CLKOUT1_PWDN
Clock Divider - HSDIVIDER-Power Down Control	CM_DIV_M5_DPLL_PER[12] HSDIVIDER_CLKOUT2_PWDN
Clock Divider - HSDIVIDER-Power Down Control	CM_DIV_M6_DPLL_PER[12] HSDIVIDER_CLKOUT3_PWDN
Clock Divider - HSDIVIDER-Power Down Control	CM_DIV_M7_DPLL_PER[12] HSDIVIDER_CLKOUT4_PWDN

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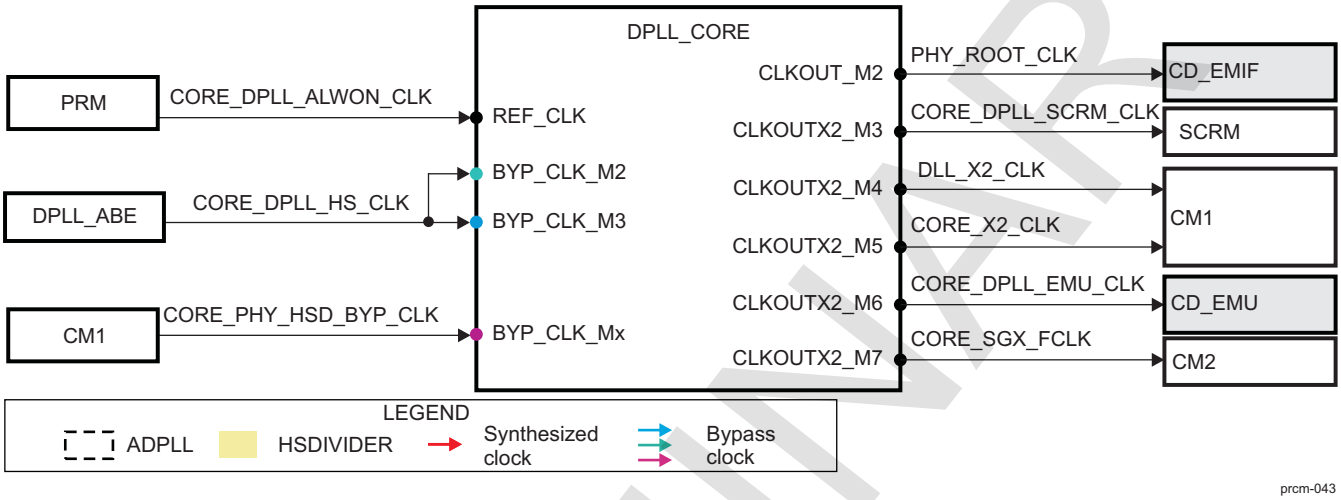
3.6.3.5 DPLL_CORE Description

3.6.3.5.1 Overview

Figure 3-48 shows the overview of the DPLL. See Section 3.6.3.3, *Generic DPLL Overview*, for a functional overview of a generic DPLL module.

Figure 3-48. DPLL_CORE Overview



3.6.3.5.2 Synthesized Clock Parameters

This section presents the clock synthesis and clock out divider parameters of the DPLL. See Section 3.6.3.3, *Generic DPLL Overview*, for an explanation of the clock synthesis and output divider parameters of the DPLL module.

Table 3-54 lists the clock synthesis parameters of the DPLL.

Table 3-54. DPLL_CORE Clock Synthesis Parameters

Parameter Name	Control Bit Field
M	CM_CLKSEL_DPLL_CORE[18:8] DPLL_MULT
N	CM_CLKSEL_DPLL_CORE[6:0] DPLL_DIV
M (Restore)	CM_CLKSEL_DPLL_CORE_RESTORE[18:8] DPLL_MULT
N (Restore)	CM_CLKSEL_DPLL_CORE_RESTORE[6:0] DPLL_DIV

Table 3-55 lists the clock output divider parameters of the DPLL.

Table 3-55. DPLL_CORE Clock Output Parameters

Clock Output/Divider	Parameter Name	Control/Status Bit Field
CLKOUT_M2	Status	CM_DIV_M2_DPLL_CORE[9] ST_DPLL_CLKOUT
CLKOUT_M2	Gating Control	CM_DIV_M2_DPLL_CORE[8] DPLL_CLKOUT_GATE_CTRL
CLKOUT_M2	Divider Acknowledge	CM_DIV_M2_DPLL_CORE[5] DPLL_CLKOUT_DIVCHACK
CLKOUT_M2	Divider Control	CM_DIV_M2_DPLL_CORE[4:0] DPLL_CLKOUT_DIV
CLKOUTX2_M3	Status	CM_DIV_M3_DPLL_CORE[9] ST_DPLL_CLKOUTHIF
CLKOUTX2_M3	Gating Control	CM_DIV_M3_DPLL_CORE[8] DPLL_CLKOUTHIF_GATE_CTRL

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Table 3-55. DPLL_CORE Clock Output Parameters (continued)

Clock Output/Divider	Parameter Name	Control/Status Bit Field
CLKOUTX2_M3	Divider Acknowledge	CM_DIV_M3_DPLL_CORE[5] DPLL_CLKOUTHIF_DIVCHACK
CLKOUTX2_M3	Divider Control	CM_DIV_M3_DPLL_CORE[4:0] DPLL_CLKOUTHIF_DIV
CLKOUTX2_M4	Status	CM_DIV_M4_DPLL_CORE[9] ST_HSDIVIDER_CLKOUT1
CLKOUTX2_M4	Gating Control	CM_DIV_M4_DPLL_CORE[8] HSDIVIDER_CLKOUT1_GATE_CTRL
CLKOUTX2_M4	Divider Acknowledge	CM_DIV_M4_DPLL_CORE[5] HSDIVIDER_CLKOUT1_DIVCHACK
CLKOUTX2_M4	Divider Control	CM_DIV_M4_DPLL_CORE[4:0] HSDIVIDER_CLKOUT1_DIV
CLKOUTX2_M5	Status	CM_DIV_M5_DPLL_CORE[9] ST_HSDIVIDER_CLKOUT2
CLKOUTX2_M5	Gating Control	CM_DIV_M5_DPLL_CORE[8] HSDIVIDER_CLKOUT2_GATE_CTRL
CLKOUTX2_M5	Divider Acknowledge	CM_DIV_M5_DPLL_CORE[5] HSDIVIDER_CLKOUT2_DIVCHACK
CLKOUTX2_M5	Divider Control	CM_DIV_M5_DPLL_CORE[4:0] HSDIVIDER_CLKOUT2_DIV
CLKOUTX2_M6	Status	CM_DIV_M6_DPLL_CORE[9] ST_HSDIVIDER_CLKOUT3
CLKOUTX2_M6	Gating Control	CM_DIV_M6_DPLL_CORE[8] HSDIVIDER_CLKOUT3_GATE_CTRL
CLKOUTX2_M6	Divider Acknowledge	CM_DIV_M6_DPLL_CORE[5] HSDIVIDER_CLKOUT3_DIVCHACK
CLKOUTX2_M6	Divider Control	CM_DIV_M6_DPLL_CORE[4:0] HSDIVIDER_CLKOUT3_DIV
CLKOUTX2_M7	Status	CM_DIV_M7_DPLL_CORE[9] ST_HSDIVIDER_CLKOUT4
CLKOUTX2_M7	Gating Control	CM_DIV_M7_DPLL_CORE[8] HSDIVIDER_CLKOUT4_GATE_CTRL
CLKOUTX2_M7	Divider Acknowledge	CM_DIV_M7_DPLL_CORE[5] HSDIVIDER_CLKOUT4_DIVCHACK
CLKOUTX2_M7	Divider Control	CM_DIV_M7_DPLL_CORE[4:0] HSDIVIDER_CLKOUT4_DIV

3.6.3.5.3 Power Modes

This section identifies the operating modes supported by the DPLL and also identifies the control bit fields to set its operating modes. See Section 3.6.3.3.2, *Enable Control, Status and Low-Power Operation Mode,* and Section 3.6.3.3.3, *DPLL Power Modes*, for an explanation of the DPLL operating modes, and associated control and status features.

Table 3-56 lists the operating modes supported by the DPLL.

Table 3-56. DPLL_CORE Modes

Low-Power Stop	Fast-Relock Stop	MN Bypass	Low-Power Bypass	Fast-Relock Bypass	Lock
Not available	Not available	Available (default)	Available	Available	Available

Table 3-57 lists the control bit fields for the operating mode control of the DPLL.

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Table 3-57. DPLL_CORE Mode Control Parameters

Parameter Name	Control Bit Field
Low-Power Mode Control	CM_CLKMODE_DPLL_CORE[10] DPLL_LPMODE_EN
Manual Mode Control	CM_CLKMODE_DPLL_CORE[2:0] DPLL_EN
Auto Mode Control	CM_AUTOIDLE_DPLL_CORE[2:0] AUTO_DPLL_MODE
Low-Power Mode Control (Restore)	CM_CLKMODE_DPLL_CORE_RESTORE[10] DPLL_LPMODE_EN
Manual Mode Control (Restore)	CM_CLKMODE_DPLL_CORE_RESTORE[2:0] DPLL_EN
Auto Mode Control (Restore)	CM_AUTOIDLE_DPLL_CORE_RESTORE[2:0] AUTO_DPLL_MODE

3.6.3.5.4 Recalibration

Table 3-58 lists the control bit fields for the recalibration feature enable and interrupts of the DPLL. See Section 3.6.3.3.4, *DPLL Recalibration*, for an explanation of the DPLL recalibration feature.

Table 3-58. DPLL_CORE Recalibration Feature Parameters

Parameter Name	Control/Status Bit Field
Recalibration - Enable Control	CM_CLKMODE_DPLL_CORE[8] DPLL_DRIFTGUARD_EN
Recalibration - Enable Control	CM_CLKMODE_DPLL_CORE_RESTORE[8] DPLL_DRIFTGUARD_EN
Recalibration - Interrupt Status	PRM_IRQSTATUS_MPU_A9[0] DPLL_CORE_RECAL_ST
Recalibration - Interrupt mask Control	PRM_IRQENABLE_MPU_A9[0] DPLL_CORE_RECAL_EN
Recalibration - Interrupt Status	PRM_IRQSTATUS_MPU_M3[0] DPLL_CORE_RECAL_ST
Recalibration - Interrupt Mask Control	PRM_IRQENABLE_MPU_M3[0] DPLL_CORE_RECAL_EN

3.6.3.5.5 Spread Spectrum Clocking

Table 3-59 lists the control bit fields associated with the SSC features of the DPLL. See Section 3.6.3.3.5, *DPLL Spread Spectrum Clocking*, for an explanation of the DPLL SSC feature.

Table 3-59. DPLL_CORE Spread-Spectrum Clocking Feature Parameters

Parameter Name	Control Bit Field
SSC Downspread	CM_CLKMODE_DPLL_CORE[14] DPLL_SSC_DOWNSPREAD
SSC Acknowledge	CM_CLKMODE_DPLL_CORE[13] DPLL_SSC_ACK
SSC Enable Control	CM_CLKMODE_DPLL_CORE[12] DPLL_SSC_EN
Modulation Step Size Setting	CM_SSC_DELTAMSTEP_DPLL_CORE[19:0] DELTAMSTEP
Modulation Frequency Divider - Exponent	CM_SSC_MODFREQDIV_DPLL_CORE[10:8] MODFREQDIV_EXPONENT
Modulation Frequency Divider - Mantissa	CM_SSC_MODFREQDIV_DPLL_CORE[6:0] MODFREQDIV_MANTISSA
Restore Modulation Step Size setting	CM_SSC_DELTAMSTEP_DPLL_CORE_RESTORE[19:0] DELTAMSTEP
Restore Modulation Frequency Divider - Exponent	CM_SSC_MODFREQDIV_DPLL_CORE_RESTORE[10:8] MODFREQDIV_EXPONENT
Restore Modulation Frequency Divider - Mantissa	CM_SSC_MODFREQDIV_DPLL_CORE_RESTORE[6:0] MODFREQDIV_MANTISSA
Restore SSC Downspread	CM_CLKMODE_DPLL_CORE_RESTORE[14] DPLL_SSC_DOWNSPREAD
Restore SSC Acknowledge	CM_CLKMODE_DPLL_CORE_RESTORE[13] DPLL_SSC_ACK
Restore SSC Enable Control	CM_CLKMODE_DPLL_CORE_RESTORE[12] DPLL_SSC_EN

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3.6.3.5.6 Output Power-Down

Table 3-60 lists the control bit fields for the output power down features of the DPLL. See Section 3.6.3.3.6, *DPLL Output Power Down*, for an explanation of the DPLL output power-down feature.

Table 3-60. DPLL_CORE Clock Output Power-Down Parameters

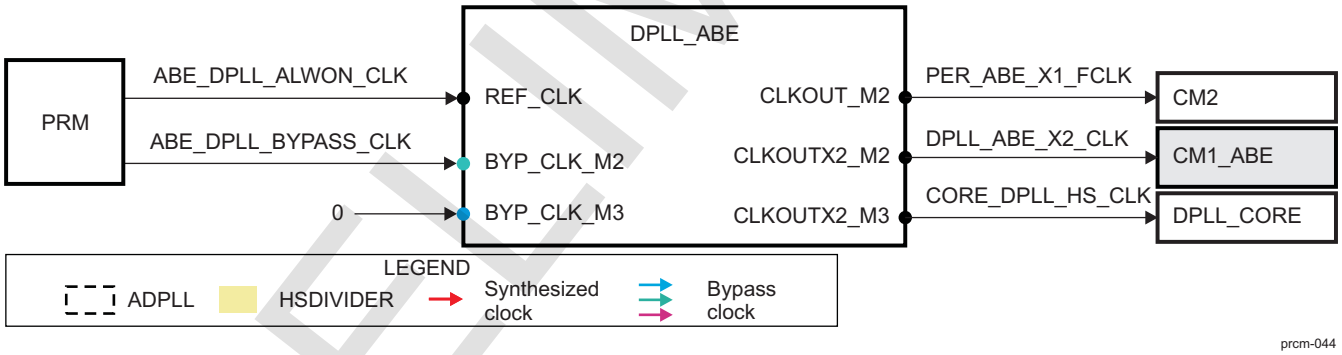
Parameter Name	Control/Status Bit Field
Clock Divider - HSDIVIDER-Power Down Control	CM_DIV_M4_DPLL_CORE[12] HSDIVIDER_CLKOUT1_PWDN
Clock Divider - HSDIVIDER-Power Down Control	CM_DIV_M5_DPLL_CORE[12] HSDIVIDER_CLKOUT2_PWDN
Clock Divider - HSDIVIDER-Power Down Control	CM_DIV_M6_DPLL_CORE[12] HSDIVIDER_CLKOUT3_PWDN
Clock Divider - HSDIVIDER-Power Down Control	CM_DIV_M7_DPLL_CORE[12] HSDIVIDER_CLKOUT4_PWDN
Restore Clock Divider - HSDIVIDER-Power Down Control	CM_DIV_M4_DPLL_CORE_RESTORE[12] HSDIVIDER_CLKOUT1_PWDN
Restore Clock Divider - HSDIVIDER-Power Down Control	CM_DIV_M5_DPLL_CORE_RESTORE[12] HSDIVIDER_CLKOUT2_PWDN
Restore Clock Divider - HSDIVIDER-Power Down Control	CM_DIV_M6_DPLL_CORE_RESTORE[12] HSDIVIDER_CLKOUT3_PWDN
Restore Clock Divider - HSDIVIDER-Power Down Control	CM_DIV_M7_DPLL_CORE_RESTORE[12] HSDIVIDER_CLKOUT4_PWDN

3.6.3.6 DPLL_ABE Description

3.6.3.6.1 Overview

Figure 3-49 shows the overview of the DPLL. See Section 3.6.3.3, *Generic DPLL Overview*, for a functional overview of a generic DPLL module.

Figure 3-49. DPLL_ABE Overview



3.6.3.6.2 Synthesized Clock Parameters

This section presents the clock synthesis and clock out divider parameters of the DPLL. See Section 3.6.3.3, *Generic DPLL Overview*, for an explanation of the clock synthesis and output divider parameters of the DPLL module.

Table 3-61 lists the clock synthesis parameters of the DPLL.

Table 3-61. DPLL_ABE Clock Synthesis Parameters

Parameter Name	Control Bit Field
M	CM_CLKSEL_DPLL_ABE[18:8] DPLL_MULT
N	CM_CLKSEL_DPLL_ABE[6:0] DPLL_DIV

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Table 3-62 lists the clock output divider parameters of the DPLL.

Table 3-62. DPLL_ABE Clock Output Parameters

Clock Output/Divider	Parameter Name	Control/Status Bit Field
CLKOUT_M2	Status	CM_DIV_M2_DPLL_ABE[9] ST_DPLL_CLKOUT
CLKOUT_M2	Gating Control	CM_DIV_M2_DPLL_ABE[8] DPLL_CLKOUT_GATE_CTRL
CLKOUT_M2	Divider Acknowledge	CM_DIV_M2_DPLL_ABE[5] DPLL_CLKOUT_DIVCHACK
CLKOUTX2_M2	Status	CM_DIV_M2_DPLL_ABE[11] ST_DPLL_CLKOUTX2
CLKOUTX2_M2	Gating Control	CM_DIV_M2_DPLL_ABE[10] DPLL_CLKOUTX2_GATE_CTRL
CLKOUT_M2	Divider Control	CM_DIV_M2_DPLL_ABE[4:0] DPLL_CLKOUT_DIV
CLKOUTX2_M3	Status	CM_DIV_M3_DPLL_ABE[9] ST_DPLL_CLKOUTHIF
CLKOUTX2_M3	Gating Control	CM_DIV_M3_DPLL_ABE[8] DPLL_CLKOUTHIF_GATE_CTRL
CLKOUTX2_M3	Divider Acknowledge	CM_DIV_M3_DPLL_ABE[5] DPLL_CLKOUTHIF_DIVCHACK
CLKOUTX2_M3	Divider Control	CM_DIV_M3_DPLL_ABE[4:0] DPLL_CLKOUTHIF_DIV

3.6.3.6.3 Power Modes

This section identifies the operating modes supported by the DPLL and also identify the control bit fields to set its operating modes. See Section 3.6.3.3.2, *Enable Control, Status and Low-Power Operation Mode*, and Section 3.6.3.3.3, *DPLL Power Mode*, for an explanation of the DPLL operating modes, and associated control and status features.

Table 3-63 lists the operating modes supported by the DPLL.

Table 3-63. DPLL_ABE Modes

Low-Power Stop	Fast-Relock Stop	MN Bypass	Low-Power Bypass	Fast-Relock Bypass	Lock
Not available	Not available	Available (Default)	Available	Available	Available

Table 3-64 lists the control bit fields for the operating mode control of the DPLL.

Table 3-64. DPLL_ABE Mode Control Parameters

Parameter Name	Control Bit Field
Low-Power Mode Control	CM_CLKMODE_DPLL_ABE[10] DPLL_LPMODE_EN
Manual Mode Control	CM_CLKMODE_DPLL_ABE[2:0] DPLL_EN
Auto Mode Control	CM_AUTOIDLE_DPLL_ABE[2:0] AUTO_DPLL_MODE

3.6.3.6.4 Recalibration

Table 3-65 lists the control bit fields for the recalibration feature enable and interrupts of the DPLL. See Section 3.6.3.3.4, *DPLL Recalibration*, for an explanation of the DPLL recalibration feature.

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Table 3-65. DPLL_ABE Recalibration Feature Parameters

Parameter Name	Control/Status Bit Field
Recalibration - Enable Control	CM_CLKMODE_DPLL_ABE[8] DPLL_DRIFTGUARD_EN
Recalibration - Interrupt Status	PRM_IRQSTATUS_MPU_A9[4] DPLL_ABE_RECAL_ST
Recalibration - Interrupt Mask Control	PRM_IRQENABLE_MPU_A9[4] DPLL_ABE_RECAL_EN

3.6.3.6.5 Spread Spectrum Clocking

Table 3-66 lists the control bit fields associated with the SSC features of the DPLL. See Section 3.6.3.3.5, *DPLL Spread Spectrum Clocking*, for an explanation of the DPLL SSC feature.

Table 3-66. DPLL_ABE Spread-Spectrum Clocking Feature Parameters

Parameter Name	Control Bit Field
SSC Downspread	CM_CLKMODE_DPLL_ABE[14] DPLL_SSC_DOWNSPREAD
SSC Acknowledge	CM_CLKMODE_DPLL_ABE[13] DPLL_SSC_ACK
SSC Enable Control	CM_CLKMODE_DPLL_ABE[12] DPLL_SSC_EN
Modulation Step Size Setting	CM_SSC_DELTAMSTEP_DPLL_ABE[19:0] DELTAMSTEP
Modulation Frequency Divider - Exponent	CM_SSC_MODFREQDIV_DPLL_ABE[10:8] MODFREQDIV_EXPONENT
Modulation Frequency Divider - Mantissa	CM_SSC_MODFREQDIV_DPLL_ABE[6:0] MODFREQDIV_MANTISSA

3.6.3.7 DPLL_MPU Description

3.6.3.7.1 Overview

Figure 3-50 shows the overview of the DPLL. See Section 3.6.3.3, *Generic DPLL Overview*, for a functional overview of a generic DPLL module.

Figure 3-50. DPLL_MPU Overview

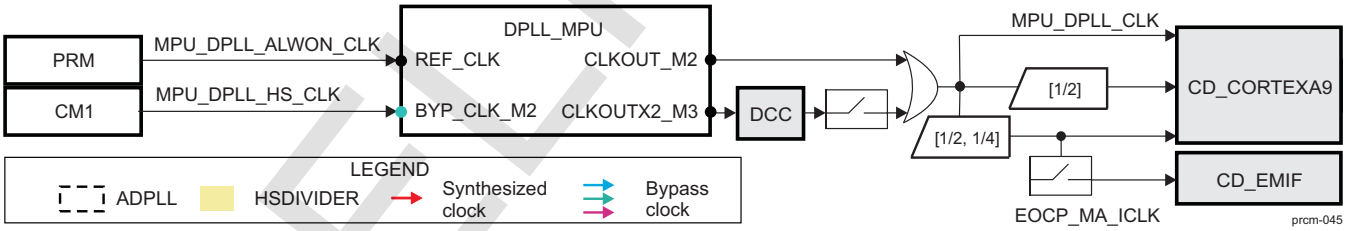

Table 3-67. MPU SS Clock Division Control

Divider/Mux	Control Bit Field
Divider EOCP_MA_ICLK	CM_MPU_MPU_CLKCTRL[24] CLKSEL_EMIF_DIV_MODE

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NOTE: For more information about setting the CM_MPU_MPU_CLKCTRL[24] CLKSEL_EMIF_DIV_MODE and CM_MPU_MPU_CLKCTRL[25] CLKSEL_ABE_DIV_MODE bits, see the *Data Manual Operating Condition Addendum*.

3.6.3.7.2 Tactical Clocking Adjustment

Figure 3-50 includes the clocking adjustment scheme for DPLL_MPU. To obtain MPU_DPLL_CLK frequency higher than 1 GHz, the CLKOUTX2_M3 output is used instead of the CLKOUT_M2 output. The M3 output divider is hardwired to value 1 and a duty cycle correction circuit (DCC) is used to recover a correct duty cycle (48–52 percent maximum). The CM_CLKSEL_DPLL_MPU[22] DCC_EN bit must be set for DPLL_MPU for the DCC to be used.

There is a subsequent clock gating element after the DCC instance. The selection between CLKOUT_M2 and CLKOUTX2_M3 source clock is performed in a glitch-free manner using an OR gate and non-overlapping input clock technique. Additional FSM is added into the CM1 to control the clock switching sequence. The FSM includes a counter for a clock ramp step (configured by the CM_CLKSEL_DPLL_MPU[31:24] DCC_COUNT_MAX bit field) during which the output frequency is Fdpll/(2*M2). This clock ramp step is used for two purposes:

- Allows enough time for DCC to lock (1.5 µs)
- Eventually avoids a transient load issue on the power IC by programming a bigger value (up to 81.6 µs)

Principles:

- When DCC_EN = 0, the DCC FSM is transparent and the CLKOUTX2_M3 gating element and the gating element after the DCC instance are off.
- When DCC_EN = 1:
  - CLKOUT_M2 is ungated as soon as the MPU clock is requested. The two other gating elements are off.
  - CLKOUTX2_M3 is ungated as soon as the DPLL is locked and the FSM starts the counter.
  - When the counter ends, CLKOUT_M2 is gated, and the DCC clock output is ungated with an assured 10-ns minimal nonoverlap time.
  - In case MPU clock is no longer requested, the DCC clock output is gated, and then the CLKOUTX2_M3 is gated.

3.6.3.7.3 Synthesized Clock Parameters

This section describes the clock synthesis and clock out divider parameters of the DPLL. See Section 3.6.3.3, *Generic DPLL Overview*, for an explanation of the clock synthesis and output divider parameters of the DPLL module.

Table 3-68 lists the clock synthesis parameters of the DPLL.

Table 3-68. DPLL_MPU Clock Synthesis Parameters

Parameter Name	Control Bit Field
M	CM_CLKSEL_DPLL_MPU[18:8] DPLL_MULT
N	CM_CLKSEL_DPLL_MPU[6:0] DPLL_DIV

Table 3-69 lists the clock output divider parameters of the DPLL.

Table 3-69. DPLL_MPU Clock Output Parameters

Clock Output/Divider	Parameter Name	Control/Status Bit Field
CLKOUT_M2	Status	CM_DIV_M2_DPLL_MPU[9] ST_DPLL_CLKOUT
CLKOUT_M2	Gating Control	CM_DIV_M2_DPLL_MPU[8] DPLL_CLKOUT_GATE_CTRL

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Table 3-69. DPLL_MPU Clock Output Parameters (continued)

Clock Output/Divider	Parameter Name	Control/Status Bit Field
CLKOUT_M2	Divider Acknowledge	CM_DIV_M2_DPLL_MPU[5] DPLL_CLKOUT_DIVCHACK
CLKOUT_M2	Divider Control	CM_DIV_M2_DPLL_MPU[4:0] DPLL_CLKOUT_DIV

3.6.3.7.4 Power Modes

This section identifies the operating modes supported by the DPLL and also identify the control bit fields to set its operating modes. See Section 3.6.3.3.2, *Enable Control, Status and Low-Power Operation Mode*, and Section 3.6.3.3.3, *DPLL Power Modes*, for an explanation of the DPLL operating modes and associated control and status features.

Table 3-70 lists the operating modes supported by the DPLL.

Table 3-70. DPLL_MPU Modes

Low-Power Stop	Fast-Relock Stop	MN Bypass	Low-Power Bypass	Fast-Relock Bypass	Lock
Not available	Not available	Available (Default)	Available	Available	Available

Table 3-71 lists the control bit fields for the operating mode control of the DPLL.

Table 3-71. DPLL_MPU Mode Control Parameters

Parameter Name	Control Bit Field
Low-Power Mode Control	CM_CLKMODE_DPLL_MPU[10] DPLL_LPMODE_EN
Manual Mode Control	CM_CLKMODE_DPLL_MPU[2:0] DPLL_EN
Auto Mode Control	CM_AUTOIDLE_DPLL_MPU[2:0] AUTO_DPLL_MODE

3.6.3.7.5 Recalibration

Table 3-72 lists the control bit fields for the recalibration feature enable and interrupts of the DPLL. See Section 3.6.3.3.4, *DPLL Recalibration*, for an explanation of the DPLL recalibration feature.

Table 3-72. DPLL_MPU Recalibration Feature Parameters

Parameter Name	Control/Status Bit Field
Recalibration - Enable Control	CM_CLKMODE_DPLL_MPU[8] DPLL_DRIFTGUARD_EN
Recalibration - Interrupt Status	PRM_IRQSTATUS_MPU_A9[1] DPLL_MPU_RECAL_ST
Recalibration - Interrupt Mask Control	PRM_IRQENABLE_MPU_A9[1] DPLL_MPU_RECAL_EN

3.6.3.7.6 Spread Spectrum Clocking

Table 3-73 lists the control bit fields associated with the SSC features of the DPLL. See Section 3.6.3.3.5, *DPLL Spread Spectrum Clocking*, for an explanation of the DPLL SSC feature.

Table 3-73. DPLL_MPU Spread-Spectrum Clocking Feature Parameters

Parameter Name	Control Bit Field
SSC Downspread	CM_CLKMODE_DPLL_MPU[14] DPLL_SSC_DOWNSPREAD
SSC Acknowledge	CM_CLKMODE_DPLL_MPU[13] DPLL_SSC_ACK
SSC Enable Control	CM_CLKMODE_DPLL_MPU[12] DPLL_SSC_EN
Modulation Step Size Setting	CM_SSC_DELTAMSTEP_DPLL_MPU[19:0] DELTAMSTEP
Modulation Frequency Divider - Exponent	CM_SSC_MODFREQDIV_DPLL_MPU[10:8] MODFREQDIV_EXPONENT

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Table 3-73. DPLL_MPU Spread-Spectrum Clocking Feature Parameters (continued)

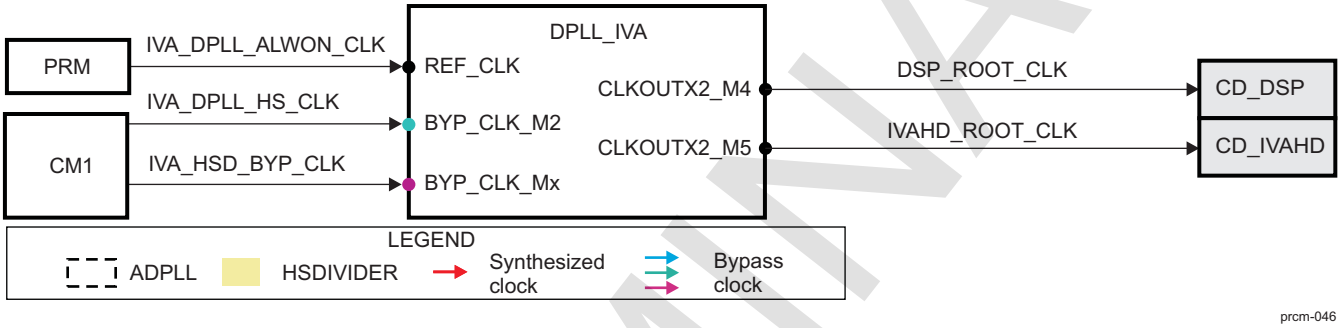
Parameter Name	Control Bit Field
Modulation Frequency Divider - Mantissa	CM_SSC_MODFREQDIV_DPLL_MPU[6:0] MODFREQDIV_MANTISSA

3.6.3.8 DPLL_IVA Description

3.6.3.8.1 Overview

Figure 3-51 shows the overview of the DPLL. See Section 3.6.3.3, *Generic DPLL Overview*, for a functional overview of a generic DPLL module.

Figure 3-51. DPLL_IVA Overview



3.6.3.8.2 Synthesized Clock Parameters

This section presents the clock synthesis and clock out divider parameters of the DPLL. See Section 3.6.3.3, *Generic DPLL Overview*, for an explanation of the clock synthesis and output divider parameters of the DPLL module.

Table 3-74 lists the clock synthesis parameters of the DPLL.

Table 3-74. DPLL_IVA Clock Synthesis Parameters

Parameter Name	Control Bit Field
M	CM_CLKSEL_DPLL_IVA[18:8] DPLL_MULT
N	CM_CLKSEL_DPLL_IVA[6:0] DPLL_DIV

Table 3-75 lists the clock output divider parameters of the DPLL.

Table 3-75. DPLL_IVA Clock Output Parameters

Clock Output/Divider	Parameter Name	Control/Status Bit Field
CLKOUTX2_M4	Status	CM_DIV_M4_DPLL_IVA[9] ST_HSDIVIDER_CLKOUT1
CLKOUTX2_M4	Gating Control	CM_DIV_M4_DPLL_IVA[8] HSDIVIDER_CLKOUT1_GATE_CTRL
CLKOUTX2_M4	Divider Acknowledge	CM_DIV_M4_DPLL_IVA[5] HSDIVIDER_CLKOUT1_DIVCHACK
CLKOUTX2_M4	Divider Control	CM_DIV_M4_DPLL_IVA[4:0] HSDIVIDER_CLKOUT1_DIV
CLKOUTX2_M5	Status	CM_DIV_M5_DPLL_IVA[9] ST_HSDIVIDER_CLKOUT2
CLKOUTX2_M5	Gating Control	CM_DIV_M5_DPLL_IVA[8] HSDIVIDER_CLKOUT2_GATE_CTRL

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Table 3-75. DPLL_IVA Clock Output Parameters (continued)

Clock Output/Divider	Parameter Name	Control/Status Bit Field
CLKOUTX2_M5	Divider Acknowledge	CM_DIV_M5_DPLL_IVA[5] HSDIVIDER_CLKOUT2_DIVCHACK
CLKOUTX2_M5	Divider Control	CM_DIV_M5_DPLL_IVA[4:0] HSDIVIDER_CLKOUT2_DIV

3.6.3.8.3 Power Modes

This section identifies the operating modes supported by the DPLL and also identify the control bit fields to set its operating modes. See Section 3.6.3.3.2, *Enable Control, Status and Low-Power Operation Mode* and Section 3.6.3.3.3, *DPLL Power Modes* for explanation on the DPLL operating modes, and associated control and status features.

Table 3-76 presents the operating modes supported by the DPLL.

Table 3-76. DPLL_IVA Modes

Low-Power Stop	Fast-Relock Stop	MN Bypass	Low-Power Bypass	Fast-Relock Bypass	Lock
Not available	Not available	Available (Default)	Available	Available	Available

Table 3-77 presents the control bit fields for the operating mode control of the DPLL.

Table 3-77. DPLL_IVA Mode Control Parameters

Parameter Name	Control Bit Field
Low-Power Mode Control	CM_CLKMODE_DPLL_IVA[10] DPLL_LPMODE_EN
Manual Mode Control	CM_CLKMODE_DPLL_IVA[2:0] DPLL_EN
Auto Mode Control	CM_AUTOIDLE_DPLL_IVA[2:0] AUTO_DPLL_MODE

3.6.3.8.4 Recalibration

Table 3-78 lists the control bit fields for the recalibration feature enable and interrupts of the DPLL. See Section 3.6.3.3.4, *DPLL Recalibration*, for an explanation of the DPLL recalibration feature.

Table 3-78. DPLL_IVA Recalibration Feature Parameters

Parameter Name	Control/Status Bit Field
Recalibration - Enable Control	CM_CLKMODE_DPLL_IVA[8] DPLL_DRIFTGUARD_EN
Recalibration - Interrupt Status	PRM_IRQSTATUS_MPU_A9[2] DPLL_IVA_RECAL_ST
Recalibration - Interrupt Mask Control	PRM_IRQENABLE_MPU_A9[2] DPLL_IVA_RECAL_EN
Recalibration - Interrupt Status	PRM_IRQSTATUS_MPU_M3[2] DPLL_IVA_RECAL_ST
Recalibration - Interrupt Mask Control	PRM_IRQENABLE_MPU_M3[2] DPLL_IVA_RECAL_EN

3.6.3.8.5 Spread Spectrum Clocking

Table 3-79 lists the control bit fields associated with the SSC features of the DPLL. See Section 3.6.3.3.5, *DPLL Spread Spectrum Clocking*, for an explanation of the DPLL SSC feature.

Table 3-79. DPLL_IVA Spread-Spectrum Clocking Feature Parameters

Parameter Name	Control Bit Field
SSC Downspread	CM_CLKMODE_DPLL_IVA[14] DPLL_SSC_DOWNSPREAD
SSC Acknowledge	CM_CLKMODE_DPLL_IVA[13] DPLL_SSC_ACK
SSC Enable Control	CM_CLKMODE_DPLL_IVA[12] DPLL_SSC_EN

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Table 3-79. DPLL_IVA Spread-Spectrum Clocking Feature Parameters (continued)

Parameter Name	Control Bit Field
Modulation Step Size Setting	CM_SSC_DELTAMSTEP_DPLL_IVA[19:0] DELTAMSTEP
Modulation Frequency Divider - Exponent	CM_SSC_MODFREQDIV_DPLL_IVA[10:8] MODFREQDIV_EXPONENT
Modulation Frequency Divider - Mantissa	CM_SSC_MODFREQDIV_DPLL_IVA[6:0] MODFREQDIV_MANTISSA

3.6.3.8.6 Output Power Down

Table 3-80 lists the control bit fields for the output power down features of the DPLL. See Section 3.6.3.3.6, *DPLL Output Power-Down*, for an explanation of the DPLL output power-down feature.

Table 3-80. DPLL_IVA Clock Output Power-down Parameters

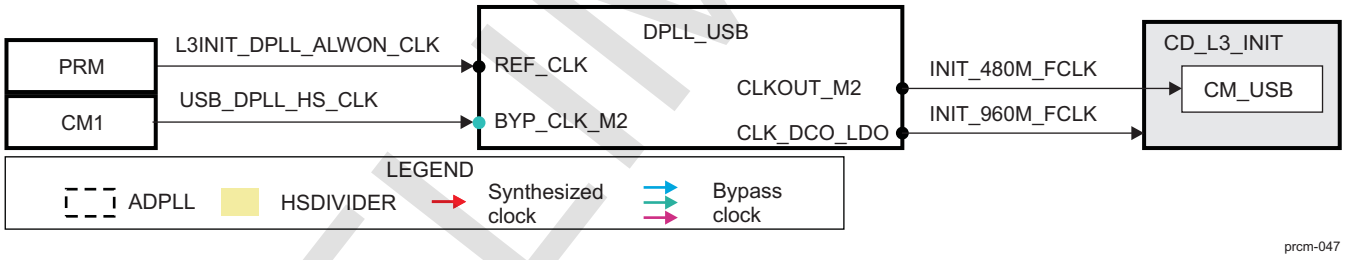
Parameter Name	Control/Status Bit Field
Clock Divider - HSDIVIDER-Power Down Control	CM_DIV_M4_DPLL_IVA[12] HSDIVIDER_CLKOUT1_PWDN
Clock Divider - HSDIVIDER-Power Down Control	CM_DIV_M5_DPLL_IVA[12] HSDIVIDER_CLKOUT2_PWDN

3.6.3.9 DPLL_USB Description

3.6.3.9.1 Overview

Figure 3-52 shows the overview of the DPLL. See Section 3.6.3.3, *Generic DPLL Overview*, for a functional overview of a generic DPLL module.

Figure 3-52. DPLL_USB Overview



3.6.3.9.2 Synthesized Clock Parameters

This section presents the clock synthesis and clock out divider parameters of the DPLL. See Section 3.6.3.3, *Generic PDLL Overview*, for an explanation of the clock synthesis and output divider parameters of the DPLL module.

Table 3-81 lists the clock synthesis parameters of the DPLL.

Table 3-81. DPLL_USB Clock Synthesis Parameters

Parameter Name	Control Bit Field
M	CM_CLKSEL_DPLL_USB[19:8] DPLL_MULT
N	CM_CLKSEL_DPLL_USB[7:0] DPLL_DIV

Table 3-82 lists the clock output divider parameters of the DPLL.

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Table 3-82. DPLL_USB Clock Output Parameters

Clock Output/Divider	Parameter Name	Control/Status Bit Field
CLKOUT_M2	Status	CM_DIV_M2_DPLL_USB[9] ST_DPLL_CLKOUT
CLKOUT_M2	Gating Control	CM_DIV_M2_DPLL_USB[8] DPLL_CLKOUT_GATE_CTRL
CLKOUT_M2	Divider Acknowledge	CM_DIV_M2_DPLL_USB[7] DPLL_CLKOUT_DIVCHACK
CLKOUT_M2	Divider Control	CM_DIV_M2_DPLL_USB[6:0] DPLL_CLKOUT_DIV

3.6.3.9.3 Power Modes

This section identifies the operating modes supported by the DPLL and also identifies the control bit fields to set its operating modes. See Section 3.6.3.3.2, *Enable Control, Status and Low-Power Operation Mode,* and Section 3.6.3.3.3, *DPLL Power Modes*, for an explanation of the DPLL operating modes, and associated control and status features.

Table 3-83 lists the operating modes supported by the DPLL.

Table 3-83. DPLL_USB Modes

Low-Power Stop	Fast-Relock Stop	MN Bypass	Low-Power Bypass	Fast-Relock Bypass	Lock
Available	Not available	Available (Default)	Available	Not available	Available

Table 3-84 lists the control bit fields for the operating mode control of the DPLL.

Table 3-84. DPLL_USB Mode Control Parameters

Parameter Name	Control Bit Field
Manual Mode Control	CM_CLKMODE_DPLL_USB[2:0] DPLL_EN
Auto Mode Control	CM_AUTOIDLE_DPLL_USB[2:0] AUTO_DPLL_MODE

3.6.3.9.4 Spread Spectrum Clocking

Table 3-85 lists the control bit fields associated with the SSC features of the DPLL. See Section 3.6.3.3.5, *DPLL Spread Spectrum Clocking*, for an explanation of the DPLL SSC feature.

Table 3-85. DPLL_USB Spread-Spectrum Clocking Feature Parameters

Parameter Name	Control Bit Field
SSC Downspread	CM_CLKMODE_DPLL_USB[14] DPLL_SSC_DOWNSPREAD
SSC Acknowledge	CM_CLKMODE_DPLL_USB[13] DPLL_SSC_ACK
SSC Enable Control	CM_CLKMODE_DPLL_USB[12] DPLL_SSC_EN
Modulation Step Size Setting	CM_SSC_DELTAMSTEP_DPLL_USB[19:0] DELTAMSTEP
Modulation Frequency Divider - Exponent	CM_SSC_MODFREQDIV_DPLL_USB[10:8] MODFREQDIV_EXPONENT
Modulation Frequency Divider - Mantissa	CM_SSC_MODFREQDIV_DPLL_USB[6:0] MODFREQDIV_MANTISSA

3.6.3.10 DPLLs Cascading

To reduce the device power consumption in certain low-power use cases of the device, the DPLLs in the device can be cascaded so that functional clock to a power domain is provided by a DPLL upstream without locking the DPLL associated with the domain. In such a case, the unlocked DPLLs can be kept in the low-power bypass mode shows the scheme for cascading DPLLs.

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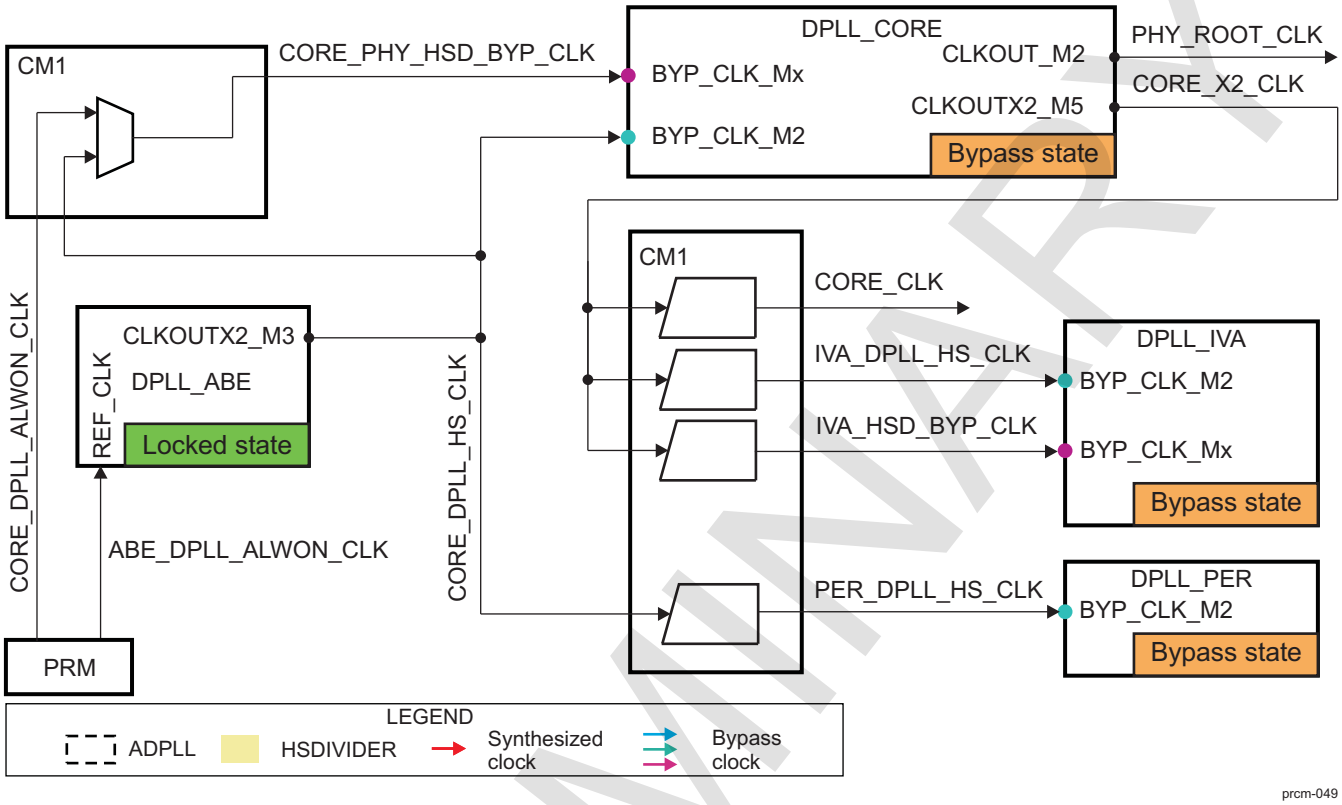
Figure 3-53 shows a generic scheme for cascading DPLLs.

Figure 3-53. DPLLs Cascading Overview



The sequence of enabling the DPLL cascading is given below:

1. DPLL_ABE is locked by software request. Other DPLLs down stream must not be moved to bypass mode before DPLL_ABE is locked. This ensures that the output clocks of these DPLLs are not stopped when they switch to the DPLL_ABE output clock.
2. Internal EMIF shadow registers are set to take PHY clock and DLL reference clock derived from DPLL_ABE.
3. Bypass paths for DPLL_IVA is set up by configuring the programmable dividers in CM1 responsible for providing the bypass clock. The setting is based upon the OPP requirements.
4. DPLL_IVA is put into bypass mode by software (any of the bypass mode is allowed) and the output of the DPLL, if already enabled, switches from locked clock to bypass clock from DPLL_CORE
5. DPLL_PER is put into bypass mode as well by software, if required. The outputs of the DPLL, if enabled, switch to the divided clock of DPLL_ABE CLKOUTX2_M3.
6. DPLL_CORE is set in bypass mode by configuring the bypass clocks input mux and the CM_SHADOW_FREQ_CONFIG1[10:8] DPLL_CORE_DPLL_EN bit field to a bypass mode in the DVFS shadow register in CM1 and setting CM_SHADOW_FREQ_CONFIG1[0] FREQ_UPDATE = 1 by software. This step triggers the handshake with EMIF to safely unlock the DPLL and move the output clock of DPLL_CORE to CORE_DPLL_HS_CLK. Ensure that the CORE_CLK divider in CM1 is correctly programmed to handle the OPP needs of the CORE power domain before this step.
7. Software can then switch the L4_WKUP interface clock from SYS_CLK to ABE_LP_CLK to allow for deasserting of the SYS_CLK request line to SCRM, if SYS_CLK is not requested by any other dependency.

The sequence of disabling the DPLL cascading is given below:

1. Software switches the L4_WKUP interface clock from ABE_LP_CLK to SYS_CLK requesting the restart of SYS_CLK by the SCRM, if not already present.

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2. Software programs the EMIF internal shadow registers to prepare the switchback of EMIF interface from using DPLL_ABE clock to DPLL_CORE clock.
3. DPLL_IVA bypass path is correctly set for the targeted DPLL_CORE frequency by programming the bypass dividers for the DPLL in CM1.
4. DPLL_CORE is relocked using the DVFS shadow register in CM1. The PRCM module ensures that this step is executed with proper handshake with EMIF to allow for a frequency update on the EMIF interface.
5. Other DPLLs are locked as well if required, to fully exit from the DPLL cascading mode.
6. DPLL_ABE might be forced into STOPMODE or bypass mode by software or may enter one of the auto modes if so programmed.

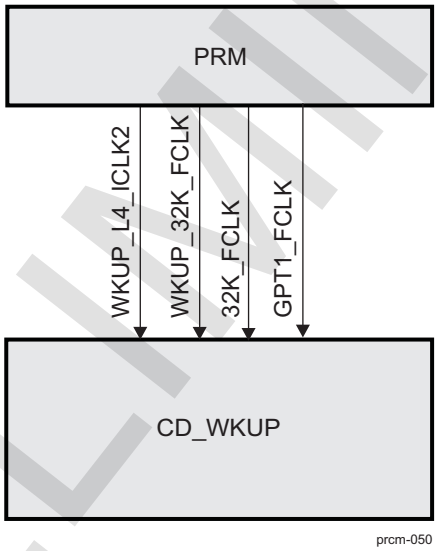
3.6.4 CD_WKUP Clock Domain

This section identifies the modes supported by the clock domain, the associated control and status bits. It also identifies its dependencies with other clock domains of the device.

3.6.4.1 Overview

Figure 3-54 shows the overview of the clock domain.

Figure 3-54. CD_WKUP Overview



3.6.4.2 Clock Domain Modes

Table 3-86 lists the clock domain modes supported by the clock domain.

Table 3-86. CD_WKUP Clock Domain Modes

NO_SLEEP	SW_SLEEP	SW_WKUP	HW_AUTO
Available	Not available	Not available	Available

Table 3-87 lists the clock domain state transition control and status bits for the clock in this clock domain.

Table 3-87. CD_WKUP Control and Status Parameters

Parameter Name	Control/Status Bit Field
ABE_LP_CLK clock status	CM_WKUP_CLKSTCTRL[9] CLKACTIVITY_ABE_LP_CLK
WKUP_L4_ICLK2 clock status	CM_WKUP_CLKSTCTRL[12] CLKACTIVITY_WKUP_L4_ICLK2
SYS_CLK clock status	CM_WKUP_CLKSTCTRL[8] CLKACTIVITY_SYS_CLK

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Table 3-87. CD_WKUP Control and Status Parameters (continued)

Parameter Name	Control/Status Bit Field
WKUP_32K_FCLK clock status	CM_WKUP_CLKSTCTRL[11] CLKACTIVITY_WKUP_32K_FCLK
Clock Domain State Transition Control	CM_WKUP_CLKSTCTRL[1:0] CLKTRCTRL

3.6.4.3 Clock Domain Dependency

CD_WKUP has no static dependency or dynamic dependency with any other clock domain of the device.

3.6.4.3.1 Wake-Up Dependency

Table 3-88 lists the wake-up dependency settings for the modules of this clock clock domain.

Table 3-88. CD_WKUP Wake-Up Dependency Association Parameters

Originator Module	Originator Clock Domain	Servicing Clock Domain	Default Setting	Control Bit Field	Access Type
GPIO1	CD_WKUP	CD_DSP	Always enabled	PM_WKUP_GPIO1_WKDEP[6] WKUPDEP_GPIO1_IRQ2_DSP	Read only
GPIO1	CD_WKUP	CD_CORTEXM3	Disabled	PM_WKUP_GPIO1_WKDEP[1] WKUPDEP_GPIO1_IRQ1_MPU_M3	Read/Write
GPIO1	CD_WKUP	CD_CORTEXA9	Disabled	PM_WKUP_GPIO1_WKDEP[0] WKUPDEP_GPIO1_IRQ1_MPU	Read/Write
KEYBOARD	CD_WKUP	CD_CORTEXA9	Always enabled	PM_WKUP_KEYBOARD_WKDEP[0] WKUPDEP_KEYBOARD_MPU	Read only
GPTIMER1	CD_WKUP	CD_CORTEXA9	Always enabled	PM_WKUP_GPTIMER1_WKDEP[0] WKUPDEP_TIMER1_MPU	Read only
WDTIMER2	CD_WKUP	CD_CORTEXM3	Disabled	PM_WKUP_WDTIMER2_WKDEP[1] WKUPDEP_WDT2_MPU_M3	Read/Write
WDTIMER2	CD_WKUP	CD_CORTEXA9	Disabled	PM_WKUP_WDTIMER2_WKDEP[0] WKUPDEP_WDT2_MPU	Read/Write

3.6.4.4 Clock Domain Module Attributes

Table 3-89 lists for each module of the clock domain the clocks received by it and the role (that is, functional or interface clock).

Table 3-89. CD_WKUP Modules Clocks Association

Module	Clock	Clock Type
SYSCTRL_PADCONF_WKUP	WKUP_L4_ICLK2	Functional
BANDGAP	WKUP_TS_FCLK	Functional
SYSCTRL_GENERAL_WKUP	WKUP_L4_ICLK2	Functional
GPIO1	WKUP_L4_ICLK2	Interface
	WKUP_32K_FCLK	Functional

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Table 3-89. CD_WKUP Modules Clocks Association (continued)

Module	Clock	Clock Type
Keyboard	WKUP_L4_ICLK2	Interface
	WKUP_32K_FCLK	Functional
SAR_RAM	WKUP_L4_ICLK2	Interface
32KTIMER	32K_FCLK	Functional
	WKUP_L4_ICLK2	Interface
GPTIMER1	GPT1_FCLK	Functional
	WKUP_L4_ICLK2	Interface
WDTIMER2	WKUP_L4_ICLK2	Interface
	WKUP_32K_FCLK	Functional
L4_WKUP interconnect	WKUP_L4_ICLK2	Interface

Table 3-90 lists the supported wake-up request generation capability for each module of the clock domain.

Table 3-90. CD_WKUP Modules Wake-Up Request

Module	Wake-Up Feature
SYSCTRL_PADCONF_WKUP	None
BANDGAP	None
SYSCTRL_GENERAL_WKUP	None
GPIO1	Slave wake-up request (MPU_A9 -IRQ, MPU_M3 -IRQ, DSP -IRQ)
Keyboard	Slave wake-up request (MPU_A9 -IRQ)
SAR_RAM	None
32KTIMER	None
GPTIMER1	Slave wake-up request (MPU_A9 -IRQ)
WDTIMER2	Slave wake-up request (MPU_A9 -IRQ, MPU_M3 -IRQ)
L4_WKUP interconnect	None

Table 3-91 lists the supported clock-management modes and associated software control bit fields for each module of the power domain.

Table 3-91. CD_WKUP Modules Clock-Management Modes and Control

Module	Clock-Management Protocol	Status Bit Field	Role
GPIO1	Slave	CM_WKUP_GPIO1_CLKCTRL [17:16] IDLEST	Idle status
KEYBOARD	Slave	CM_WKUP_KEYBOARD_CLKCTRL[17:16] IDLEST	Idle status
SAR_RAM	Slave	CM_WKUP_SARRAM_CLKCTRL[17:16] IDLEST	Idle status
32KTIMER	Slave	CM_WKUP_32KTIMER_CLKCTRL[17:16] IDLEST	Idle status
GPTIMER1	Slave	CM_WKUP_GPTIMER1_CLKCTRL[17:16] IDLEST	Idle status
WDTIMER2	Slave	CM_WKUP_WDTIMER2_CLKCTRL[17:16] IDLEST	Idle status
L4_WKUP interconnect	Slave	CM_WKUP_L4WKUP_CLKCTRL[17:16] IDLEST	Idle status

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Table 3-92 lists the supported clock management modes and associated software control bit fields for each module of the power domain.

Table 3-92. CD_WKUP Modules Slave Clock-Management Modes and Control

Module	Disabled	Auto	Enabled	Control Bit Field	Access Type
GPIO1	Available	Available	N/A	CM_WKUP_GPIO1_CLKCTRL[1:0] MODULEMODE	Read/Write
KEYBOARD	Available	N/A	Available	CM_WKUP_KEYBOARD_CLKCTRL[1:0] MODULEMODE	Read/Write
SAR_RAM	N/A	Available	N/A	CM_WKUP_SARRAM_CLKCTRL[1:0] MODULEMODE	Read only
32KTIMER	N/A	Available	N/A	CM_WKUP_32KTIMER_CLKCTRL[1:0] MODULEMODE	Read only
GPTIMER1	Available	N/A	Available	CM_WKUP_GPTIMER1_CLKCTRL[1:0] MODULEMODE	Read/Write
WDTIMER2	Available	N/A	Available	CM_WKUP_WDTIMER2_CLKCTRL[1:0] MODULEMODE	Read/Write
L4_WKUP interconnect	N/A	Available	N/A	CM_WKUP_L4WKUP_CLKCTRL[1:0] MODULEMODE	Read only

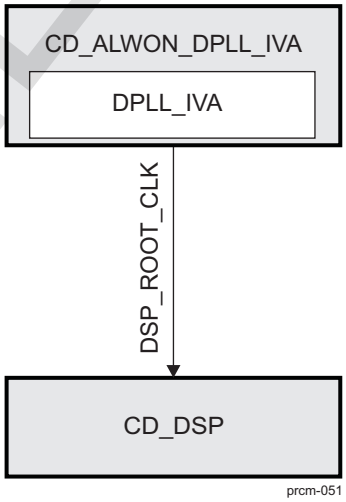
3.6.5 CD_DSP Clock Domain

This section identifies the modes supported by the clock domain, the associated control and status bits. It also identifies its dependencies with other clock domains of the device.

3.6.5.1 Overview

Figure 3-55 shows the overview of the clock domain.

Figure 3-55. CD_DSP Overview



3.6.5.2 Clock Domain Modes

Table 3-93 lists the clock domain modes supported by the clock domain.

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Table 3-93. CD_DSP Clock Domain Modes

NO_SLEEP	SW_SLEEP	SW_WKUP	HW_AUTO
Available	Available	Available	Available

Table 3-94 lists the clock domain state transition control and status bits for the clock in this clock domain.

Table 3-94. CD_DSP Control and Status Parameters

Parameter Name	Control/Status Bit Field
DSP_ROOT_CLK clock status	CM_DSP_CLKSTCTRL[8] CLKACTIVITY_DSP_ROOT_CLK
Clock Domain State Transition Control	CM_DSP_CLKSTCTRL[1:0] CLKTRCTRL

3.6.5.3 Clock Domain Dependency

CD_DSP has no module wake-up dependency with any other clock domain of the device.

3.6.5.3.1 Static Dependency

Table 3-95 lists the static dependency of the clock domain with respect to other clock domains of the device.

Table 3-95. CD_DSP Static Dependency Association Parameters

Clock Domain Name	Default Setting	Control Bit Field	Access Type
CD_ABE	Disabled	CM_DSP_STATICDEP[3] ABE_STATDEP	Read/Write
CD_CAM	Always disabled	CM_DSP_STATICDEP[9] ISS_STATDEP	Read only
CD_IVAHD	Disabled	CM_DSP_STATICDEP[2] IVAHD_STATDEP	Read/Write
CD_L3_1	Disabled	CM_DSP_STATICDEP[5] L3_1_STATDEP	Read/Write
CD_L3_2	Disabled	CM_DSP_STATICDEP[6] L3_2_STATDEP	Read/Write
CD_L3_INIT	Disabled	CM_DSP_STATICDEP[7] L3INIT_STATDEP	Read/Write
CD_L4_CFG	Disabled	CM_DSP_STATICDEP[12] L4CFG_STATDEP	Read/Write
CD_L4_PER	Disabled	CM_DSP_STATICDEP[13] L4PER_STATDEP	Read/Write
CD_EMIF	Disabled	CM_DSP_STATICDEP[4] MEMIF_STATDEP	Read/Write

3.6.5.3.2 Dynamic Dependency

Table 3-96 lists the dynamic dependency of the clock domain with respect to other clock domains of the device.

Table 3-96. CD_DSP Dynamic Dependency Association Parameters

Clock Domain Name	Default Setting	Control Bit Field	Access Type
CD_ABE	Always enabled	CM_DSP_DYNAMICDEP[3] ABE_DYNDEP	Read only
CD_IVAHD	Always enabled	CM_DSP_DYNAMICDEP[2] IVAHD_DYNDEP	Read only
CD_L3_1	Always enabled	CM_DSP_DYNAMICDEP[5] L3_1_DYNDEP	Read only

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3.6.5.4 Clock Domain Module Attributes

Table 3-97 lists for each module of the clock domain the clocks received by it and the role (that is, functional or interface clock).

Table 3-97. CD_DSP Modules Clocks Association

Module	Clock	Clock Type
DSP	DSP_ROOT_CLK	Interface and functional

Table 3-98 lists the supported wake-up request generation capability for each module of the clock domain.

Table 3-98. CD_DSP Modules Wake-Up Request

Module	Wake-Up Feature
DSP	Master wake-up request

Table 3-99 lists the supported clock-management modes and associated software control bit fields for each module of the power domain.

Table 3-99. CD_DSP Modules Clock-Management Modes and Control

Module	Clock-Management Protocol	Status Bit Field	Role
DSP	Master/Slave	CM_DSP_DSP_CLKCTRL[18] STBYST	Standby status
		CM_DSP_DSP_CLKCTRL[17:16] IDLEST	Idle status

Table 3-100 lists the supported clock-management modes and associated software control bit fields for each module of the power domain.

Table 3-100. CD_DSP Modules Slave Clock-Management Modes and Control

Module	Disabled	Auto	Enabled	Control Bit Field	Access Type
DSP	Available	Available	N/A	CM_DSP_DSP_CLKCTRL[1:0] MODULEMODE	Read/Write

3.6.6 CD_STD_EFUSE Clock Domain

This section identifies the modes supported by the clock domain, the associated control and status bits. It also identifies its dependencies with other clock domains of the device.

3.6.6.1 Overview

Figure 3-56 shows the overview of the clock domain.

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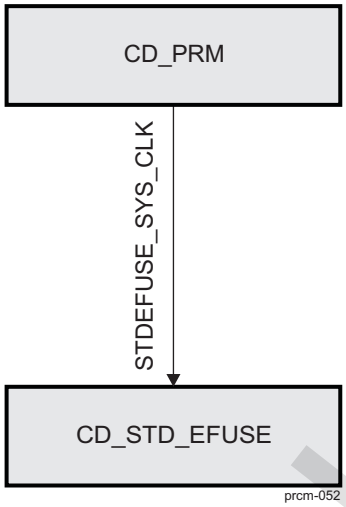
Figure 3-56. CD_STD_EFUSE Overview



CD_STD_EFUSE is hardware-controlled by the PRCM module and has no software control or status bit fields. Similarly, it has no static, dynamic and wake-up dependency with respect to other clock domains of the device

3.6.6.2 Clock Domain Module Attributes

The STD_EFUSE module of the clock domain is automatically controlled by the PRCM module hardware and has no software configurable module mode control or status bit fields.

Table 3-101 identifies for each module of the clock domain the clocks received by it and the role (that is, functional or interface clock).

Table 3-101. CD_STD_EFUSE Modules Clocks Association

Module	Clock	Clock Type
STD_EFUSE	STDEFUSE_SYS_CLK	Functional

Table 3-102 lists the supported wake-up request generation capability for each module of the clock domain.

Table 3-102. CD_STD_EFUSE Modules Wake-Up Request

Module	Wake-Up Feature
STD_EFUSE	None

3.6.7 CD_CORTEXA9 Clock Domain

This section identifies the modes supported by the clock domain, the associated control and status bits. It also identifies its dependencies with other clock domains of the device.

3.6.7.1 Overview

Figure 3-57 shows the overview of the clock domain.

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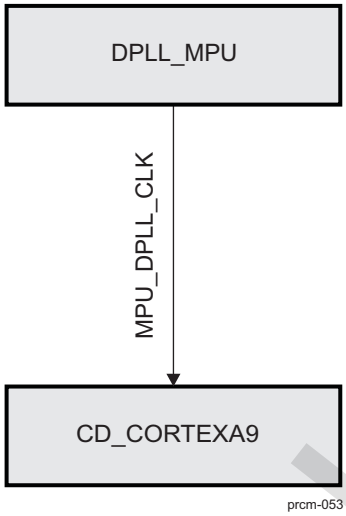
Figure 3-57. CD_CORTEXA9 Overview



3.6.7.2 Clock Domain Modes

Table 3-103 lists the clock domain modes supported by the clock domain.

Table 3-103. CD_CORTEXA9 Clock Domain Modes

NO_SLEEP	SW_SLEEP	SW_WKUP	HW_AUTO
Available	Not available	Available	Available

Table 3-104 lists the clock domain state transition control and status bits for the clock in this clock domain.

Table 3-104. CD_CORTEXA9 Control and Status Parameters

Parameter Name	Control/Status Bit Field
MPU_DPLL_CLK clock status	CM_MPU_CLKSTCTRL[9] CLKACTIVITY_MPU_DPLL_CLK
Clock Domain State Transition Control	CM_MPU_CLKSTCTRL[1:0] CLKTRCTRL

3.6.7.3 Clock Domain Dependency

CD_CORTEXA9 has no module wake-up dependency with any other clock domain of the device.

3.6.7.3.1 Static Dependency

Table 3-105 lists the static dependency of the clock domain with respect to other clock domains of the device.

Table 3-105. CD_CORTEXA9 Static Dependency Association Parameters

Clock Domain Name	Default Setting	Control Bit Field	Access Type
CD_ABE	Disabled	CM_MPU_STATICDEP[3] ABE_STATDEP	Read/Write
CD_C2C	Always disabled	CM_MPU_STATICDEP[18] C2C_STATDEP	Read only
CD_DSS	Disabled	CM_MPU_STATICDEP[8] DSS_STATDEP	Read/Write
CD_CORTEXM3	Disabled	CM_MPU_STATICDEP[0] MPU_M3_STATDEP	Read/Write
CD_SGX	Disabled	CM_MPU_STATICDEP[10] SGX_STATDEP	Read/Write

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Table 3-105. CD_CORTEXA9 Static Dependency Association Parameters (continued)

Clock Domain Name	Default Setting	Control Bit Field	Access Type
CD_CAM	Always disabled	CM_MPU_STATICDEP[9] ISS_STATDEP	Read only
CD_IVAHD	Disabled	CM_MPU_STATICDEP[2] IVAHD_STATDEP	Read/Write
CD_L3_1	Enabled	CM_MPU_STATICDEP[5] L3_1_STATDEP	Read/Write
CD_L3_2	Enabled	CM_MPU_STATICDEP[6] L3_2_STATDEP	Read/Write
CD_L3_INIT	Enabled	CM_MPU_STATICDEP[7] L3INIT_STATDEP	Read/Write
CD_L4_CFG	Enabled	CM_MPU_STATICDEP[12] L4CFG_STATDEP	Read/Write
CD_L4_PER	Enabled	CM_MPU_STATICDEP[13] L4PER_STATDEP	Read/Write
CD_EMIF	Enabled	CM_MPU_STATICDEP[4] MEMIF_STATDEP	Read/Write
CD_DMA	Always disabled	CM_MPU_STATICDEP[11] SDMA_STATDEP	Read only
CD_DSP	Disabled	CM_MPU_STATICDEP[1] DSP_STATDEP	Read/Write

3.6.7.3.2 Dynamic Dependency

Table 3-106 lists the dynamic dependency of the clock domain with respect to other clock domains of the device.

Table 3-106. CD_CORTEXA9 Dynamic Dependency Association Parameters

Clock Domain Name	Default Setting	Control Bit Field	Access Type
CD_ABE	Always enabled	CM_MPU_DYNAMICDEP[3] ABE_DYNDEP	Read only
CD_L3_1	Always enabled	CM_MPU_DYNAMICDEP[5] L3_1_DYNDEP	Read only
CD_EMIF	Always enabled	CM_MPU_DYNAMICDEP[4] MEMIF_DYNDEP	Read only

3.6.7.4 Clock Domain Module Attributes

Table 3-107 lists for each module of the clock domain the clocks received by it and the role (that is, functional or interface clock).

Table 3-107. CD_CORTEXA9 Modules Clocks Association

Module	Clock	Clock Type
CORTEXA9	MPU_DPLL_CLK	Interface and Functional

Table 3-108 lists the supported wake-up request generation capability for each module of the clock domain.

Table 3-108. CD_CORTEXA9 Modules Wake-Up Request

Module	Wake-Up Feature
CORTEXA9	Master wake-up request

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Table 3-109 lists the supported clock-management modes and associated software control bit fields for each module of the power domain.

Table 3-109. CD_CORTEXA9 Modules Clock-Management Modes and Control

Module	Clock-Management Protocol	Status Bit Field	Role
CORTEXA9	Master/Slave	CM_MPU_MPU_CLKCTRL[18] STBYST	Standby status
		CM_MPU_MPU_CLKCTRL[17:16] IDLEST	Idle status

Table 3-110 lists the supported clock-management modes and associated software control bit fields for each module of the power domain.

Table 3-110. CD_CORTEXA9 Modules Slave Clock-Management Modes and Control

Module	Disabled	Auto	Enabled	Control Bit Field	Access Type
CORTEXA9	N/A	Available	N/A	CM_MPU_MPU_CLKCTRL[1:0] MODULEMODE	Read only

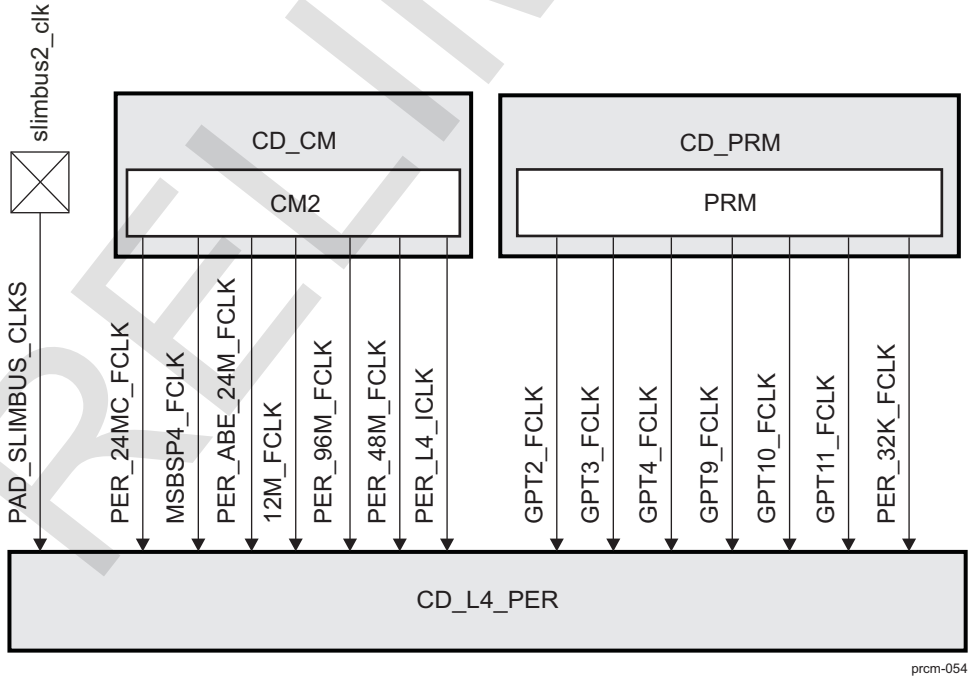
3.6.8 CD_L4_PER Clock Domain

This section identifies the modes supported by the clock domain, the associated control and status bits. It also identifies its dependencies with other clock domains of the device.

3.6.8.1 Overview

Figure 3-58 shows the overview of the clock domain.

Figure 3-58. CD_L4_PER Overview



3.6.8.2 Clock Domain Modes

Table 3-111 lists the clock domain modes supported by the clock domain.

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Table 3-111. CD_L4_PER Clock Domain Modes

NO_SLEEP	SW_SLEEP	SW_WKUP	HW_AUTO
Available	Available	Available	Available

Table 3-112 lists the clock domain state transition control and status bits for the clock in this clock domain.

Table 3-112. CD_L4_PER Control and Status Parameters

Parameter Name	Control/Status Bit Field
GPT10_FCLK clock status	CM_L4PER_CLKSTCTRL[9] CLKACTIVITY_GPT10_FCLK
GPT11_FCLK clock status	CM_L4PER_CLKSTCTRL[10] CLKACTIVITY_GPT11_FCLK
GPT2_FCLK clock status	CM_L4PER_CLKSTCTRL[11] CLKACTIVITY_GPT2_FCLK
GPT3_FCLK clock status	CM_L4PER_CLKSTCTRL[12] CLKACTIVITY_GPT3_FCLK
GPT4_FCLK clock status	CM_L4PER_CLKSTCTRL[13] CLKACTIVITY_GPT4_FCLK
GPT9_FCLK clock status	CM_L4PER_CLKSTCTRL[14] CLKACTIVITY_GPT9_FCLK
12M_FCLK clock status	CM_L4PER_CLKSTCTRL[15] CLKACTIVITY_12M_FCLK_FCLK
PER_L4_ICLK clock status	CM_L4PER_CLKSTCTRL[8] CLKACTIVITY_L4_PER_ICLK
PER_24MC_FCLK clock status	CM_L4PER_CLKSTCTRL[16] CLKACTIVITY_PER_24MC_FCLK
PER_32K_FCLK clock status	CM_L4PER_CLKSTCTRL[17] CLKACTIVITY_PER_32K_FCLK
PER_48M_FCLK clock status	CM_L4PER_CLKSTCTRL[18] CLKACTIVITY_PER_48M_FCLK
PER_96M_FCLK clock status	CM_L4PER_CLKSTCTRL[19] CLKACTIVITY_PER_96M_FCLK
PER_ABE_24M_FCLK clock status	CM_L4PER_CLKSTCTRL[25] CLKACTIVITY_PER_ABE_24M_FCLK
MCBSP4_FCLK clock status	CM_L4PER_CLKSTCTRL[22] CLKACTIVITY_PER_MCBSP4_FCLK
Clock Domain State Transition Control	CM_L4PER_CLKSTCTRL[1:0] CLKTRCTRL

3.6.8.3 Clock Domain Dependency

CD_L4_PER has no static dependency with any other clock domain of the device.

3.6.8.3.1 Dynamic Dependency

Table 3-113 lists the dynamic dependency of the clock domain with respect to other clock domains of the device.

Table 3-113. CD_L4_PER Dynamic Dependency Association Parameters

Clock Domain Name	Default Setting	Control Bit Field	Access Type
CD_DSS	Always enabled	CM_L4PER_DYNAMICDEP[8] DSS_DYNDEP	Read only
CD_L3_INIT	Always enabled	CM_L4PER_DYNAMICDEP[7] L3_INIT_DYNDEP	Read only

3.6.8.3.2 Wake-Up Dependency

Table 3-114 lists the wake-up dependency settings for the modules of this clock clock domain.

Table 3-114. CD_L4_PER Wake-Up Dependency Association Parameters

Originator Module	Originator Clock Domain	Servicing Clock Domain	Default Setting	Control Bit Field	Access Type
GPTIMER10	CD_L4_PER	CD_CORTEXA9	Always enabled	PM_L4PER_GPTIMER10_WKDEP[0] WKUPDEP_DMTIMER10_MPU	Read only

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Table 3-114. CD_L4_PER Wake-Up Dependency Association Parameters (continued)

Originator Module	Originator Clock Domain	Servicing Clock Domain	Default Setting	Control Bit Field	Access Type
GPTIMER11	CD_L4_PER	CD_CORTEXM3	Disabled	PM_L4PER_GPTIMER11_WKDEP[1] WKUPDEP_DMTIMER11_MPU_M3	Read/Write
GPTIMER11	CD_L4_PER	CD_CORTEXA9	Disabled	PM_L4PER_GPTIMER11_WKDEP[0] WKUPDEP_DMTIMER11_MPU	Read/Write
GPTIMER2	CD_L4_PER	CD_CORTEXA9	Always enabled	PM_L4PER_GPTIMER2_WKDEP[0] WKUPDEP_DMTIMER2_MPU	Read only
GPTIMER3	CD_L4_PER	CD_CORTEXM3	Disabled	PM_L4PER_GPTIMER3_WKDEP[1] WKUPDEP_DMTIMER3_MPU_M3	Read/Write
GPTIMER3	CD_L4_PER	CD_CORTEXA9	Disabled	PM_L4PER_GPTIMER3_WKDEP[0] WKUPDEP_DMTIMER3_MPU	Read/Write
GPTIMER4	CD_L4_PER	CD_CORTEXM3	Disabled	PM_L4PER_GPTIMER4_WKDEP[1] WKUPDEP_DMTIMER4_MPU_M3	Read/Write
GPTIMER4	CD_L4_PER	CD_CORTEXA9	Disabled	PM_L4PER_GPTIMER4_WKDEP[0] WKUPDEP_DMTIMER4_MPU	Read/Write
GPTIMER9	CD_L4_PER	CD_CORTEXM3	Disabled	PM_L4PER_GPTIMER9_WKDEP[1] WKUPDEP_DMTIMER9_MPU_M3	Read/Write
GPTIMER9	CD_L4_PER	CD_CORTEXA9	Disabled	PM_L4PER_GPTIMER9_WKDEP[0] WKUPDEP_DMTIMER9_MPU	Read/Write
GPIO2	CD_L4_PER	CD_DSP	Always enabled	PM_L4PER_GPIO2_WKDEP[6] WKUPDEP_GPIO2_IRQ2_DSP	Read only
GPIO2	CD_L4_PER	CD_CORTEXM3	Disabled	PM_L4PER_GPIO2_WKDEP[1] WKUPDEP_GPIO2_IRQ1_MPU_M3	Read/Write
GPIO2	CD_L4_PER	CD_CORTEXA9	Disabled	PM_L4PER_GPIO2_WKDEP[0] WKUPDEP_GPIO2_IRQ1_MPU	Read/Write
GPIO3	CD_L4_PER	CD_DSP	Always enabled	PM_L4PER_GPIO3_WKDEP[6] WKUPDEP_GPIO3_IRQ2_DSP	Read only
GPIO3	CD_L4_PER	CD_CORTEXA9	Disabled	PM_L4PER_GPIO3_WKDEP[0] WKUPDEP_GPIO3_IRQ1_MPU	Read only
GPIO4	CD_L4_PER	CD_DSP	Always enabled	PM_L4PER_GPIO4_WKDEP[6] WKUPDEP_GPIO4_IRQ2_DSP	Read only

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Table 3-114. CD_L4_PER Wake-Up Dependency Association Parameters (continued)

Originator Module	Originator Clock Domain	Servicing Clock Domain	Default Setting	Control Bit Field	Access Type
GPIO4	CD_L4_PER	CD_CORTEXA9	Disabled	PM_L4PER_GPIO4_WKDEP[0] WKUPDEP_GPIO4_IRQ1_MPU	Read only
GPIO5	CD_L4_PER	CD_DSP	Always enabled	PM_L4PER_GPIO5_WKDEP[6] WKUPDEP_GPIO5_IRQ2_DSP	Read only
GPIO5	CD_L4_PER	CD_CORTEXA9	Always enabled	PM_L4PER_GPIO5_WKDEP[0] WKUPDEP_GPIO5_IRQ1_MPU	Read only
GPIO6	CD_L4_PER	CD_DSP	Always enabled	PM_L4PER_GPIO6_WKDEP[6] WKUPDEP_GPIO6_IRQ2_DSP	Read only
GPIO6	CD_L4_PER	CD_CORTEXA9	Always enabled	PM_L4PER_GPIO6_WKDEP[0] WKUPDEP_GPIO6_IRQ1_MPU	Read only
I2C1	CD_L4_PER	CD_DMA, CD_L3_1, CD_L3_2	Always enabled	PM_L4PER_I2C1_WKDEP[7] WKUPDEP_I2C1_DMA_SDMA	Read only
I2C1	CD_L4_PER	CD_CORTEXM3	Disabled	PM_L4PER_I2C1_WKDEP[1] WKUPDEP_I2C1_IRQ_MPU_M3	Read/Write
I2C1	CD_L4_PER	CD_CORTEXA9	Disabled	PM_L4PER_I2C1_WKDEP[0] WKUPDEP_I2C1_IRQ_MPU	Read/Write
I2C2	CD_L4_PER	CD_DMA, CD_L3_1, CD_L3_2	Always enabled	PM_L4PER_I2C2_WKDEP[7] WKUPDEP_I2C2_DMA_SDMA	Read only
I2C2	CD_L4_PER	CD_CORTEXM3	Disabled	PM_L4PER_I2C2_WKDEP[1] WKUPDEP_I2C2_IRQ_MPU_M3	Read/Write
I2C2	CD_L4_PER	CD_CORTEXA9	Disabled	PM_L4PER_I2C2_WKDEP[0] WKUPDEP_I2C2_IRQ_MPU	Read/Write
I2C3	CD_L4_PER	CD_DMA, CD_L3_1, CD_L3_2	Always enabled	PM_L4PER_I2C3_WKDEP[7] WKUPDEP_I2C3_DMA_SDMA	Read only
I2C3	CD_L4_PER	CD_CORTEXM3	Disabled	PM_L4PER_I2C3_WKDEP[1] WKUPDEP_I2C3_IRQ_MPU_M3	Read/Write
I2C3	CD_L4_PER	CD_CORTEXA9	Disabled	PM_L4PER_I2C3_WKDEP[0] WKUPDEP_I2C3_IRQ_MPU	Read/Write
I2C4	CD_L4_PER	CD_DMA, CD_L3_1, CD_L3_2	Always enabled	PM_L4PER_I2C4_WKDEP[7] WKUPDEP_I2C4_DMA_SDMA	Read only

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Table 3-114. CD_L4_PER Wake-Up Dependency Association Parameters (continued)

Originator Module	Originator Clock Domain	Servicing Clock Domain	Default Setting	Control Bit Field	Access Type
I2C4	CD_L4_PER	CD_CORTEXM3	Disabled	PM_L4PER_I2C4_WKDEP[1] WKUPDEP_I2C4_IRQ_MPU_M3	Read/Write
I2C4	CD_L4_PER	CD_CORTEXA9	Disabled	PM_L4PER_I2C4_WKDEP[0] WKUPDEP_I2C4_IRQ_MPU	Read/Write
MCBSP4	CD_L4_PER	CD_DMA, CD_L3_1, CD_L3_2	Disabled	PM_L4PER_MCBSP4_WKDEP[3] WKUPDEP_MCBSP4_SDMA	Read/Write
MCBSP4	CD_L4_PER	CD_DSP	Disabled	PM_L4PER_MCBSP4_WKDEP[2] WKUPDEP_MCBSP4_DSP	Read/Write
MCBSP4	CD_L4_PER	CD_CORTEXA9	Disabled	PM_L4PER_MCBSP4_WKDEP[0] WKUPDEP_MCBSP4_MPU	Read/Write
MCSPI1	CD_L4_PER	CD_DMA, CD_L3_1, CD_L3_2	Disabled	PM_L4PER_MCSPI1_WKDEP[3] WKUPDEP_MCSPI1_SDMA	Read/Write
MCSPI1	CD_L4_PER	CD_DSP	Disabled	PM_L4PER_MCSPI1_WKDEP[2] WKUPDEP_MCSPI1_DSP	Read/Write
MCSPI1	CD_L4_PER	CD_CORTEXM3	Disabled	PM_L4PER_MCSPI1_WKDEP[1] WKUPDEP_MCSPI1_MPU_M3	Read/Write
MCSPI1	CD_L4_PER	CD_CORTEXA9	Disabled	PM_L4PER_MCSPI1_WKDEP[0] WKUPDEP_MCSPI1_MPU	Read/Write
MCSPI2	CD_L4_PER	CD_DMA, CD_L3_1, CD_L3_2	Disabled	PM_L4PER_MCSPI2_WKDEP[3] WKUPDEP_MCSPI2_SDMA	Read/Write
MCSPI2	CD_L4_PER	CD_CORTEXM3	Disabled	PM_L4PER_MCSPI2_WKDEP[1] WKUPDEP_MCSPI2_MPU_M3	Read/Write
MCSPI2	CD_L4_PER	CD_CORTEXA9	Disabled	PM_L4PER_MCSPI2_WKDEP[0] WKUPDEP_MCSPI2_MPU	Read/Write
MCSPI3	CD_L4_PER	CD_DMA, CD_L3_1, CD_L3_2	Disabled	PM_L4PER_MCSPI3_WKDEP[3] WKUPDEP_MCSPI3_SDMA	Read/Write
MCSPI3	CD_L4_PER	CD_CORTEXA9	Disabled	PM_L4PER_MCSPI3_WKDEP[0] WKUPDEP_MCSPI3_MPU	Read/Write
MCSPI4	CD_L4_PER	CD_DMA, CD_L3_1, CD_L3_2	Disabled	PM_L4PER_MCSPI4_WKDEP[3] WKUPDEP_MCSPI4_SDMA	Read/Write

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Table 3-114. CD_L4_PER Wake-Up Dependency Association Parameters (continued)

Originator Module	Originator Clock Domain	Servicing Clock Domain	Default Setting	Control Bit Field	Access Type
MCSPI4	CD_L4_PER	CD_CORTEXA9	Disabled	PM_L4PER_MCSPI4_WKDEP[0] WKUPDEP_MCSPI4_MPU	Read/Write
HSMMC3	CD_L4_PER	CD_DMA, CD_L3_1, CD_L3_2	Disabled	PM_L4PER_MMCSD3_WKDEP[3] WKUPDEP_MMCSD3_SDMA	Read/Write
HSMMC3	CD_L4_PER	CD_CORTEXM3	Disabled	PM_L4PER_MMCSD3_WKDEP[1] WKUPDEP_MMCSD3_MPU_M3	Read/Write
HSMMC3	CD_L4_PER	CD_CORTEXA9	Disabled	PM_L4PER_MMCSD3_WKDEP[0] WKUPDEP_MMCSD3_MPU	Read/Write
HSMMC4	CD_L4_PER	CD_DMA, CD_L3_1, CD_L3_2	Disabled	PM_L4PER_MMCSD4_WKDEP[3] WKUPDEP_MMCSD4_SDMA	Read/Write
HSMMC4	CD_L4_PER	CD_CORTEXM3	Disabled	PM_L4PER_MMCSD4_WKDEP[1] WKUPDEP_MMCSD4_MPU_M3	Read/Write
HSMMC4	CD_L4_PER	CD_CORTEXA9	Disabled	PM_L4PER_MMCSD4_WKDEP[0] WKUPDEP_MMCSD4_MPU	Read/Write
HSMMC5	CD_L4_PER	CD_DMA, CD_L3_1, CD_L3_2	Disabled	PM_L4PER_MMCSD5_WKDEP[3] WKUPDEP_MMCSD5_SDMA	Read/Write
HSMMC5	CD_L4_PER	CD_CORTEXM3	Disabled	PM_L4PER_MMCSD5_WKDEP[1] WKUPDEP_MMCSD5_MPU_M3	Read/Write
HSMMC5	CD_L4_PER	CD_CORTEXA9	Disabled	PM_L4PER_MMCSD5_WKDEP[0] WKUPDEP_MMCSD5_MPU	Read/Write
SLIMBUS2	CD_L4_PER	CD_DMA, CD_L3_1, CD_L3_2	Disabled	PM_L4PER_SLIMBUS2_WKDEP[7] WKUPDEP_SLIMBUS2_DMA_SDMA	Read/Write
SLIMBUS2	CD_L4_PER	CD_DSP	Disabled	PM_L4PER_SLIMBUS2_WKDEP[6] WKUPDEP_SLIMBUS2_DMA_DSP	Read/Write
SLIMBUS2	CD_L4_PER	CD_DSP	Disabled	PM_L4PER_SLIMBUS2_WKDEP[2] WKUPDEP_SLIMBUS2_IRQ_DSP	Read/Write
SLIMBUS2	CD_L4_PER	CD_CORTEXA9	Disabled	PM_L4PER_SLIMBUS2_WKDEP[0] WKUPDEP_SLIMBUS2_IRQ_MPU	Read/Write
UART1	CD_L4_PER	CD_DMA, CD_L3_1, CD_L3_2	Disabled	PM_L4PER_UART1_WKDEP[3] WKUPDEP_UART1_SDMA	Read/Write

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Table 3-114. CD_L4_PER Wake-Up Dependency Association Parameters (continued)

Originator Module	Originator Clock Domain	Servicing Clock Domain	Default Setting	Control Bit Field	Access Type
UART1	CD_L4_PER	CD_CORTEXA9	Disabled	PM_L4PER_UART1_WKDEP[0] WKUPDEP_UART1_MPU	Read/Write
UART2	CD_L4_PER	CD_DMA, CD_L3_1, CD_L3_2	Disabled	PM_L4PER_UART2_WKDEP[3] WKUPDEP_UART2_SDMA	Read/Write
UART2	CD_L4_PER	CD_CORTEXA9	Disabled	PM_L4PER_UART2_WKDEP[0] WKUPDEP_UART2_MPU	Read/Write
UART3	CD_L4_PER	CD_DMA, CD_L3_1, CD_L3_2	Disabled	PM_L4PER_UART3_WKDEP[3] WKUPDEP_UART3_SDMA	Read/Write
UART3	CD_L4_PER	CD_DSP	Disabled	PM_L4PER_UART3_WKDEP[2] WKUPDEP_UART3_DSP	Read/Write
UART3	CD_L4_PER	CD_CORTEXM3	Disabled	PM_L4PER_UART3_WKDEP[1] WKUPDEP_UART3_MPU_M3	Read/Write
UART3	CD_L4_PER	CD_CORTEXA9	Disabled	PM_L4PER_UART3_WKDEP[0] WKUPDEP_UART3_MPU	Read/Write
UART4	CD_L4_PER	CD_DMA, CD_L3_1, CD_L3_2	Disabled	PM_L4PER_UART4_WKDEP[3] WKUPDEP_UART4_SDMA	Read/Write
UART4	CD_L4_PER	CD_CORTEXA9	Disabled	PM_L4PER_UART4_WKDEP[0] WKUPDEP_UART4_MPU	Read/Write

3.6.8.4 Clock Domain Module Attributes

Table 3-115 lists for each module of the clock domain the clocks received by it and the role (that is, functional or interface clock).

Table 3-115. CD_L4_PER Modules Clocks Association

Module	Clock	Clock Type
GPTIMER10	GPT10_FCLK	Functional
	PER_L4_ICLK	Interface
GPTIMER11	GPT11_FCLK	Functional
	PER_L4_ICLK	Interface
GPTIMER2	GPT2_FCLK	Functional
	PER_L4_ICLK	Interface
GPTIMER3	GPT3_FCLK	Functional
	PER_L4_ICLK	Interface
GPTIMER4	GPT4_FCLK	Functional
	PER_L4_ICLK	Interface
GPTIMER9	GPT9_FCLK	Functional

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Table 3-115. CD_L4_PER Modules Clocks Association (continued)

Module	Clock	Clock Type
	PER_L4_ICLK	Interface
ELM	PER_L4_ICLK	Interface
GPIO2	PER_L4_ICLK	Interface
	PER_32K_FCLK	Functional
GPIO3	PER_L4_ICLK	Interface
	PER_32K_FCLK	Functional
GPIO4	PER_L4_ICLK	Interface
	PER_32K_FCLK	Functional
GPIO5	PER_L4_ICLK	Interface
	PER_32K_FCLK	Functional
GPIO6	PER_L4_ICLK	Interface
	PER_32K_FCLK	Functional
HDQ	12M_FCLK	Functional
	PER_L4_ICLK	Interface and functional
I2C1	PER_L4_ICLK	Interface
	PER_96M_FCLK	Functional
I2C2	PER_L4_ICLK	Interface
	PER_96M_FCLK	Functional
I2C3	PER_L4_ICLK	Interface
	PER_96M_FCLK	Functional
I2C4	PER_L4_ICLK	Interface
	PER_96M_FCLK	Functional
L4_PER interconnect	PER_L4_ICLK	Interface
MCBSP4	PER_L4_ICLK	Interface
	MCBSP4_FCLK	Functional
MCSPI1	PER_L4_ICLK	Interface
	PER_48M_FCLK	Functional
MCSPI2	PER_L4_ICLK	Interface
	PER_48M_FCLK	Functional
MCSPI3	PER_L4_ICLK	Interface
	PER_48M_FCLK	Functional
MCSPI4	PER_L4_ICLK	Interface
	PER_48M_FCLK	Functional
HSMMC3	PER_L4_ICLK	Interface
	PER_48M_FCLK	Functional
HSMMC4	PER_L4_ICLK	Interface
	PER_48M_FCLK	Functional
HSMMC5	PER_L4_ICLK	Interface
	PER_48M_FCLK	Functional
SLIMBUS2	PER_L4_ICLK	Interface
	PAD_SLIMBUS_CLKS	Functional
	PER_24MC_FCLK	Functional
	PER_ABE_24M_FCLK	Functional
UART1	PER_L4_ICLK	Interface
	PER_48M_FCLK	Functional
UART2	PER_L4_ICLK	Interface
	PER_48M_FCLK	Functional

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Table 3-115. CD_L4_PER Modules Clocks Association (continued)

Module	Clock	Clock Type
UART3	PER_L4_ICLK	Interface
	PER_48M_FCLK	Functional
UART4	PER_L4_ICLK	Interface
	PER_48M_FCLK	Functional

Table 3-116 lists the supported wake-up request generation capability for each module of the clock domain.

Table 3-116. CD_L4_PER Modules Wake-Up Request

Module	Wake-Up Feature
GPTIMER10	Slave wake-up request (MPU_A9 -IRQ)
GPTIMER11	Slave wake-up request (MPU_A9 -IRQ, MPU_M3 -IRQ)
GPTIMER2	Slave wake-up request (MPU_A9 -IRQ)
GPTIMER3	Slave wake-up request (MPU_A9 -IRQ, MPU_M3 -IRQ)
GPTIMER4	Slave wake-up request (MPU_A9 -IRQ, MPU_M3 -IRQ)
GPTIMER9	Slave wake-up request (MPU_A9 -IRQ, MPU_M3 -IRQ)
ELM	None
GPIO2	Slave wake-up request (MPU_A9 -IRQ, MPU_M3 -IRQ, DSP -IRQ)
GPIO3	Slave wake-up request (MPU_A9 -IRQ, DSP -IRQ)
GPIO4	Slave wake-up request (MPU_A9 -IRQ, DSP -IRQ)
GPIO5	Slave wake-up request (MPU_A9 -IRQ, DSP -IRQ)
GPIO6	Slave wake-up request (MPU_A9 -IRQ, DSP -IRQ)
HDQ	None
I2C1	Slave wake-up request (MPU_A9 -IRQ, MPU_M3 -IRQ, sDMA -DMA)
I2C2	Slave wake-up request (MPU_A9 -IRQ, MPU_M3 -IRQ, sDMA -DMA)
I2C3	Slave wake-up request (MPU_A9 -IRQ, MPU_M3 -IRQ, sDMA -DMA)
I2C4	Slave wake-up request (MPU_A9 -IRQ, MPU_M3 -IRQ, sDMA -DMA)
L4_PER interconnect	None
MCBSP4	Slave wake-up request (MPU_A9 -IRQ, DSP -IRQ and DMA, sDMA -DMA)
MCSPI1	Slave wake-up request (MPU_A9 -IRQ, MPU_M3 -IRQ, DSP -IRQ, sDMA -DMA)
MCSPI2	Slave wake-up request (MPU_A9 -IRQ, MPU_M3 -IRQ, sDMA -DMA)
MCSPI3	Slave wake-up request (MPU_A9 -IRQ, sDMA -DMA)
MCSPI4	Slave wake-up request (MPU_A9 -IRQ, sDMA -DMA)
HSMMC3	Slave wake-up request (MPU_A9 -IRQ, MPU_M3 -IRQ, sDMA -DMA)
HSMMC4	Slave wake-up request (MPU_A9 -IRQ, MPU_M3 -IRQ, sDMA -DMA)
HSMMC5	Slave wake-up request (MPU_A9 -IRQ, MPU_M3 -IRQ, sDMA -DMA)
SLIMBUS2	Slave wake-up request (MPU_A9 -IRQ, DSP -IRQ and DMA, sDMA -DMA)
UART1	Slave wake-up request (MPU_A9 -IRQ, sDMA -DMA)
UART2	Slave wake-up request (MPU_A9 -IRQ, sDMA -DMA)

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Table 3-116. CD_L4_PER Modules Wake-Up Request (continued)

Module	Wake-Up Feature
UART3	Slave wake-up request (MPU_A9 -IRQ, MPU_M3 -IRQ, DSP -IRQ and DMA, sDMA -DMA)
UART4	Slave wake-up request (MPU_A9 -IRQ, sDMA -DMA)

Table 3-117 lists the supported clock-management modes and associated software control bit fields for each module of the power domain.

Table 3-117. CD_L4_PER Modules Clock-Management Modes and Control

Module	Clock-Management Protocol	Status Bit Field	Role
GPTIMER10	Slave	CM_L4PER_GPTIMER10_CLKCTRL[17:16] IDLEST	Idle status
GPTIMER11	Slave	CM_L4PER_GPTIMER11_CLKCTRL[17:16] IDLEST	Idle status
GPTIMER2	Slave	CM_L4PER_GPTIMER2_CLKCTRL[17:16] IDLEST	Idle status
GPTIMER3	Slave	CM_L4PER_GPTIMER3_CLKCTRL[17:16] IDLEST	Idle status
GPTIMER4	Slave	CM_L4PER_GPTIMER4_CLKCTRL[17:16] IDLEST	Idle status
GPTIMER9	Slave	CM_L4PER_GPTIMER9_CLKCTRL[17:16] IDLEST	Idle status
ELM	Slave	CM_L4PER_ELM_CLKCTRL[17:16] IDLEST	Idle status
GPIO2	Slave	CM_L4PER_GPIO2_CLKCTRL[17:16] IDLEST	Idle status
GPIO3	Slave	CM_L4PER_GPIO3_CLKCTRL[17:16] IDLEST	Idle status
GPIO4	Slave	CM_L4PER_GPIO4_CLKCTRL[17:16] IDLEST	Idle status
GPIO5	Slave	CM_L4PER_GPIO5_CLKCTRL[17:16] IDLEST	Idle status
GPIO6	Slave	CM_L4PER_GPIO6_CLKCTRL[17:16] IDLEST	Idle status
HDQ	Slave	CM_L4PER_HDQ1W_CLKCTRL[17:16] IDLEST	Idle status
I2C1	Slave	CM_L4PER_I2C1_CLKCTRL[17:16] IDLEST	Idle status
I2C2	Slave	CM_L4PER_I2C2_CLKCTRL[17:16] IDLEST	Idle status
I2C3	Slave	CM_L4PER_I2C3_CLKCTRL[17:16] IDLEST	Idle status
I2C4	Slave	CM_L4PER_I2C4_CLKCTRL[17:16] IDLEST	Idle status
L4_PER interconnect	Slave	CM_L4PER_L4PER_CLKCTRL[17:16] IDLEST	Idle status
MCBSP4	Slave	CM_L4PER_MCBSP4_CLKCTRL[17:16] IDLEST	Idle status
MCSPI1	Slave	CM_L4PER_MCSPI1_CLKCTRL[17:16] IDLEST	Idle status
MCSPI2	Slave	CM_L4PER_MCSPI2_CLKCTRL[17:16] IDLEST	Idle status
MCSPI3	Slave	CM_L4PER_MCSPI3_CLKCTRL[17:16] IDLEST	Idle status
MCSPI4	Slave	CM_L4PER_MCSPI4_CLKCTRL[17:16] IDLEST	Idle status

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Table 3-117. CD_L4_PER Modules Clock-Management Modes and Control (continued)

Module	Clock-Management Protocol	Status Bit Field	Role
HSMMC3	Slave	CM_L4PER_MMCSD3_CLKCTRL[17:16] IDLEST	Idle status
HSMMC4	Slave	CM_L4PER_MMCSD4_CLKCTRL[17:16] IDLEST	Idle status
HSMMC5	Slave	CM_L4PER_MMCSD5_CLKCTRL[17:16] IDLEST	Idle status
SLIMBUS2	Slave	CM_L4PER_SLIMBUS2_CLKCTRL[17:16] IDLEST	Idle status
UART1	Slave	CM_L4PER_UART1_CLKCTRL[17:16] IDLEST	Idle status
UART2	Slave	CM_L4PER_UART2_CLKCTRL[17:16] IDLEST	Idle status
UART3	Slave	CM_L4PER_UART3_CLKCTRL[17:16] IDLEST	Idle status
UART4	Slave	CM_L4PER_UART4_CLKCTRL[17:16] IDLEST	Idle status

Table 3-118 lists the supported clock-management modes and associated software control bit fields for each module of the power domain.

Table 3-118. CD_L4_PER Modules Slave Clock-Management Modes and Control

Module	Disabled	Auto	Enabled	Control Bit Field	Access Type
GPTIMER10	Available	N/A	Available	CM_L4PER_GPTIMER10_CLKCTRL[1:0] MODULEMODE	Read/Write
GPTIMER11	Available	N/A	Available	CM_L4PER_GPTIMER11_CLKCTRL[1:0] MODULEMODE	Read/Write
GPTIMER2	Available	N/A	Available	CM_L4PER_GPTIMER2_CLKCTRL[1:0] MODULEMODE	Read/Write
GPTIMER3	Available	N/A	Available	CM_L4PER_GPTIMER3_CLKCTRL[1:0] MODULEMODE	Read/Write
GPTIMER4	Available	N/A	Available	CM_L4PER_GPTIMER4_CLKCTRL[1:0] MODULEMODE	Read/Write
GPTIMER9	Available	N/A	Available	CM_L4PER_GPTIMER9_CLKCTRL[1:0] MODULEMODE	Read/Write
ELM	N/A	Available	N/A	CM_L4PER_ELM_CLKCTRL[1:0] MODULEMODE	Read only
GPIO2	Available	Available	N/A	CM_L4PER_GPIO2_CLKCTRL[1:0] MODULEMODE	Read/Write
GPIO2	Available	Available	Available	CM_L4PER_GPIO2_CLKCTRL_RESTORE[1:0] MODULEMODE	Read/Write
GPIO3	Available	Available	N/A	CM_L4PER_GPIO3_CLKCTRL[1:0] MODULEMODE	Read/Write
GPIO3	Available	Available	Available	CM_L4PER_GPIO3_CLKCTRL_RESTORE[1:0] MODULEMODE	Read/Write

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Table 3-118. CD_L4_PER Modules Slave Clock-Management Modes and Control (continued)

Module	Disabled	Auto	Enabled	Control Bit Field	Access Type
GPIO4	Available	Available	N/A	CM_L4PER_GPIO4_CLKCTRL[1:0] MODULEMODE	Read/Write
GPIO4	Available	Available	Available	CM_L4PER_GPIO4_CLKCTRL_RESTORE[1:0] MODULEMODE	Read/Write
GPIO5	Available	Available	N/A	CM_L4PER_GPIO5_CLKCTRL[1:0] MODULEMODE	Read/Write
GPIO5	Available	Available	Available	CM_L4PER_GPIO5_CLKCTRL_RESTORE[1:0] MODULEMODE	Read/Write
GPIO6	Available	Available	N/A	CM_L4PER_GPIO6_CLKCTRL[1:0] MODULEMODE	Read/Write
GPIO6	Available	Available	Available	CM_L4PER_GPIO6_CLKCTRL_RESTORE[1:0] MODULEMODE	Read/Write
HDQ	Available	N/A	Available	CM_L4PER_HDQ1W_CLKCTRL[1:0] MODULEMODE	Read/Write
I2C1	Available	N/A	Available	CM_L4PER_I2C1_CLKCTRL[1:0] MODULEMODE	Read/Write
I2C2	Available	N/A	Available	CM_L4PER_I2C2_CLKCTRL[1:0] MODULEMODE	Read/Write
I2C3	Available	N/A	Available	CM_L4PER_I2C3_CLKCTRL[1:0] MODULEMODE	Read/Write
I2C4	Available	N/A	Available	CM_L4PER_I2C4_CLKCTRL[1:0] MODULEMODE	Read/Write
L4_PER interconnect	N/A	Available	N/A	CM_L4PER_L4PER_CLKCTRL[1:0] MODULEMODE	Read only
MCBSP4	Available	N/A	Available	CM_L4PER_MCBSP4_CLKCTRL[1:0] MODULEMODE	Read/Write
MCSPI1	Available	N/A	Available	CM_L4PER_MCSPI1_CLKCTRL[1:0] MODULEMODE	Read/Write
MCSPI2	Available	N/A	Available	CM_L4PER_MCSPI2_CLKCTRL[1:0] MODULEMODE	Read/Write
MCSPI3	Available	N/A	Available	CM_L4PER_MCSPI3_CLKCTRL[1:0] MODULEMODE	Read/Write
MCSPI4	Available	N/A	Available	CM_L4PER_MCSPI4_CLKCTRL[1:0] MODULEMODE	Read/Write
HSMMC3	Available	N/A	Available	CM_L4PER_MMCSD3_CLKCTRL[1:0] MODULEMODE	Read/Write
HSMMC4	Available	N/A	Available	CM_L4PER_MMCSD4_CLKCTRL[1:0] MODULEMODE	Read/Write

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Table 3-118. CD_L4_PER Modules Slave Clock-Management Modes and Control (continued)

Module	Disabled	Auto	Enabled	Control Bit Field	Access Type
HSMMC5	Available	N/A	Available	CM_L4PER_MMCSD5_CLKCTRL[1:0] MODULEMODE	Read/Write
SLIMBUS2	Available	N/A	Available	CM_L4PER_SLIMBUS2_CLKCTRL[1:0] MODULEMODE	Read/Write
UART1	Available	N/A	Available	CM_L4PER_UART1_CLKCTRL[1:0] MODULEMODE	Read/Write
UART2	Available	N/A	Available	CM_L4PER_UART2_CLKCTRL[1:0] MODULEMODE	Read/Write
UART3	Available	N/A	Available	CM_L4PER_UART3_CLKCTRL[1:0] MODULEMODE	Read/Write
UART4	Available	N/A	Available	CM_L4PER_UART4_CLKCTRL[1:0] MODULEMODE	Read/Write

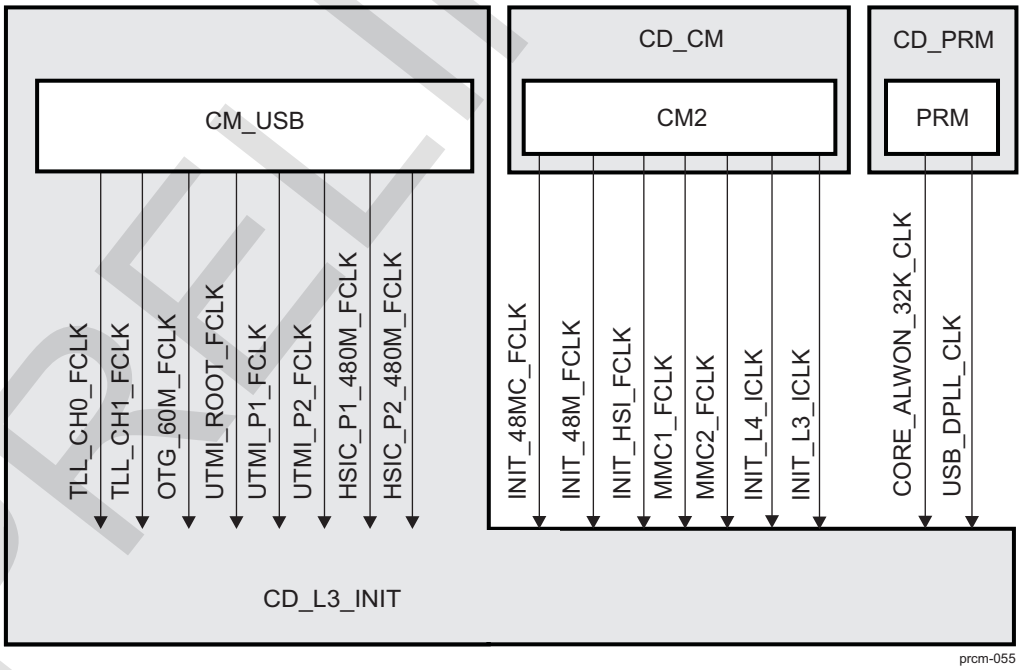
3.6.9 CD_L3_INIT Clock Domain

This section identifies the modes supported by the clock domain, the associated control and status bits. It also identifies its dependencies with other clock domains of the device.

3.6.9.1 Overview

Figure 3-59 shows the overview of the clock domain.

Figure 3-59. CD_L3_INIT Overview



3.6.9.2 Clock Domain Modes

Table 3-119 lists the clock domain modes supported by the clock domain.

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Table 3-119. CD_L3_INIT Clock Domain Modes

NO_SLEEP	SW_SLEEP	SW_WKUP	HW_AUTO
Available	Available	Available	Available

Table 3-120 lists the clock domain state transition control and status bits for the clock in this clock domain.

Table 3-120. CD_L3_INIT Control and Status Parameters

Parameter Name	Control/Status Bit Field
HSIC_P1_480M_FCLK clock status	CM_L3INIT_CLKSTCTRL[20] CLKACTIVITY_HSIC_P1_480M_FCLK
HSIC_P1_FCLK clock status	CM_L3INIT_CLKSTCTRL[26] CLKACTIVITY_HSIC_P1_FCLK
HSIC_P2_480M_FCLK clock status	CM_L3INIT_CLKSTCTRL[21] CLKACTIVITY_HSIC_P2_480M_FCLK
HSIC_P2_FCLK clock status	CM_L3INIT_CLKSTCTRL[27] CLKACTIVITY_HSIC_P2_FCLK
INIT_48MC_FCLK clock status	CM_L3INIT_CLKSTCTRL[12] CLKACTIVITY_INIT_48MC_FCLK
INIT_48M_FCLK clock status	CM_L3INIT_CLKSTCTRL[13] CLKACTIVITY_INIT_48M_FCLK
INIT_60M_P1_FCLK clock status	CM_L3INIT_CLKSTCTRL[28] CLKACTIVITY_INIT_60M_P1_FCLK
INIT_60M_P2_FCLK clock status	CM_L3INIT_CLKSTCTRL[29] CLKACTIVITY_INIT_60M_P2_FCLK
INIT_HSI_FCLK clock status	CM_L3INIT_CLKSTCTRL[16] CLKACTIVITY_INIT_HSI_FCLK
MMC1_FCLK clock status	CM_L3INIT_CLKSTCTRL[17] CLKACTIVITY_INIT_HSMMC1_FCLK
MMC2_FCLK clock status	CM_L3INIT_CLKSTCTRL[18] CLKACTIVITY_INIT_HSMMC2_FCLK
INIT_L3_ICLK clock status	CM_L3INIT_CLKSTCTRL[8] CLKACTIVITY_INIT_L3_ICLK
INIT_L4_ICLK clock status	CM_L3INIT_CLKSTCTRL[9] CLKACTIVITY_INIT_L4_ICLK
TLL_CH0_FCLK clock status	CM_L3INIT_CLKSTCTRL[22] CLKACTIVITY_TLL_CH0_FCLK
TLL_CH1_FCLK clock status	CM_L3INIT_CLKSTCTRL[23] CLKACTIVITY_TLL_CH1_FCLK
UTMI_ROOT_FCLK clock status	CM_L3INIT_CLKSTCTRL[25] CLKACTIVITY_UTMI_ROOT_FCLK
Clock Domain State Transition Control	CM_L3INIT_CLKSTCTRL[1:0] CLKTRCTRL

3.6.9.3 Clock Domain Dependency

3.6.9.3.1 Static Dependency

Table 3-121 lists the static dependency of the clock domain with respect to other clock domains of the device.

Table 3-121. CD_L3_INIT Static Dependency Association Parameters

Clock Domain Name	Default Setting	Control Bit Field	Access Type
CD_ABE	Disabled	CM_L3INIT_STATICDEP[3] ABE_STATDEP	Read/Write
CD_IVAHD	Disabled	CM_L3INIT_STATICDEP[2] IVAHD_STATDEP	Read/Write
CD_L3_1	Always enabled	CM_L3INIT_STATICDEP[5] L3_1_STATDEP	Read only
CD_L3_2	Always enabled	CM_L3INIT_STATICDEP[6] L3_2_STATDEP	Read only
CD_L4_CFG	Disabled	CM_L3INIT_STATICDEP[12] L4CFG_STATDEP	Read/Write
CD_L4_PER	Disabled	CM_L3INIT_STATICDEP[13] L4PER_STATDEP	Read/Write

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Table 3-121. CD_L3_INIT Static Dependency Association Parameters (continued)

Clock Domain Name	Default Setting	Control Bit Field	Access Type
CD_EMIF	Disabled	CM_L3INIT_STATICDEP[4] MEMIF_STATDEP	Read/Write

3.6.9.3.2 Dynamic Dependency

Table 3-122 lists the dynamic dependency of the clock domain with respect to other clock domains of the device.

Table 3-122. CD_L3_INIT Dynamic Dependency Association Parameters

Clock Domain Name	Default Setting	Control Bit Field	Access Type
CD_L3_1	Always disabled	CM_L3INIT_DYNAMICDEP[5] L3_1_DYNDEP	Read only
CD_L3_2	Always disabled	CM_L3INIT_DYNAMICDEP[6] L3_2_DYNDEP	Read only

3.6.9.3.3 Wake-Up Dependency

Table 3-123 lists the wake-up dependency settings for the modules of this clock clock domain.

Table 3-123. CD_L3_INIT Wake-Up Dependency Association Parameters

Originator Module	Originator Clock Domain	Servicing Clock Domain	Default Setting	Control Bit Field	Access Type
HSI	CD_L3_INIT	CD_CORTEXA9	Disabled	PM_L3INIT_HSI_WKDEP[8] WKUPDEP_WGM_HSI_WAKE_MPU	Read/Write
HSI	CD_L3_INIT	CD_DSP	Always enabled	PM_L3INIT_HSI_WKDEP[6] WKUPDEP_HSI_DSP_DSP	Read only
HSI	CD_L3_INIT	CD_CORTEXM3	Disabled	PM_L3INIT_HSI_WKDEP[1] WKUPDEP_HSI_MCU_MPU_M3	Read/Write
HSI	CD_L3_INIT	CD_CORTEXA9	Disabled	PM_L3INIT_HSI_WKDEP[0] WKUPDEP_HSI_MCU_MPU	Read/Write
HSMMC1	CD_L3_INIT	CD_DMA, CD_L3_1, CD_L3_2	Disabled	PM_L3INIT_MMC1_WKDEP[3] WKUPDEP_MMC1_SDMA	Read/Write
HSMMC1	CD_L3_INIT	CD_DSP	Disabled	PM_L3INIT_MMC1_WKDEP[2] WKUPDEP_MMC1_DSP	Read/Write
HSMMC1	CD_L3_INIT	CD_CORTEXM3	Disabled	PM_L3INIT_MMC1_WKDEP[1] WKUPDEP_MMC1_MPU_M3	Read/Write
HSMMC1	CD_L3_INIT	CD_CORTEXA9	Disabled	PM_L3INIT_MMC1_WKDEP[0] WKUPDEP_MMC1_MPU	Read/Write
HSMMC2	CD_L3_INIT	CD_DMA, CD_L3_1, CD_L3_2	Disabled	PM_L3INIT_MMC2_WKDEP[3] WKUPDEP_MMC2_SDMA	Read/Write

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Table 3-123. CD_L3_INIT Wake-Up Dependency Association Parameters (continued)

Originator Module	Originator Clock Domain	Servicing Clock Domain	Default Setting	Control Bit Field	Access Type
HSMMC2	CD_L3_INIT	CD_DSP	Disabled	PM_L3INIT_MMC2_WKDEP[2] WKUPDEP_MMC2_DSP	Read/Write
HSMMC2	CD_L3_INIT	CD_CORTEXM3	Disabled	PM_L3INIT_MMC2_WKDEP[1] WKUPDEP_MMC2_MPU_M3	Read/Write
HSMMC2	CD_L3_INIT	CD_CORTEXA9	Disabled	PM_L3INIT_MMC2_WKDEP[0] WKUPDEP_MMC2_MPU	Read/Write
FSUSB	CD_L3_INIT	CD_CORTEXM3	Disabled	PM_L3INIT_FSUSB_WKDEP[1] WKUPDEP_FSUSB_MPU_M3	Read/Write
FSUSB	CD_L3_INIT	CD_CORTEXA9	Disabled	PM_L3INIT_FSUSB_WKDEP[0] WKUPDEP_FSUSB_MPU	Read/Write
HSUSBHOST	CD_L3_INIT	CD_CORTEXM3	Disabled	PM_L3INIT_HSUSBHOST_WKDEP[1] WKUPDEP_HSUSBHOST_MPU_M3	Read/Write
HSUSBHOST	CD_L3_INIT	CD_CORTEXA9	Disabled	PM_L3INIT_HSUSBHOST_WKDEP[0] WKUPDEP_HSUSBHOST_MPU	Read/Write
HSUSBOTG	CD_L3_INIT	CD_CORTEXM3	Disabled	PM_L3INIT_HSUSBOTG_WKDEP[1] WKUPDEP_HSUSBOTG_MPU_M3	Read/Write
HSUSBOTG	CD_L3_INIT	CD_CORTEXA9	Disabled	PM_L3INIT_HSUSBOTG_WKDEP[0] WKUPDEP_HSUSBOTG_MPU	Read/Write
HSUSBTLL	CD_L3_INIT	CD_CORTEXM3	Disabled	PM_L3INIT_HSUSBTLL_WKDEP[1] WKUPDEP_HSUSBTLL_MPU_M3	Read/Write
HSUSBTLL	CD_L3_INIT	CD_CORTEXA9	Disabled	PM_L3INIT_HSUSBTLL_WKDEP[0] WKUPDEP_HSUSBTLL_MPU	Read/Write

3.6.9.4 Clock Domain Module Attributes

Table 3-124 lists for each module of the clock domain the clocks received by it and the role (that is, functional or interface clock).

Table 3-124. CD_L3_INIT Modules Clocks Association

Module	Clock	Clock Type
HSI	INIT_HSI_FCLK	Interface and functional
	INIT_L3_ICLK	Interface
	INIT_L4_ICLK	Interface
HSMMC1	MMC1_FCLK	Functional
	INIT_L3_ICLK	Interface

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Table 3-124. CD_L3_INIT Modules Clocks Association (continued)

Module	Clock	Clock Type
	INIT_L4_ICLK	Interface
HSMMC2	MMC2_FCLK	Functional
	INIT_L3_ICLK	Interface
	INIT_L4_ICLK	Interface
USBPHY	CORE_ALWON_32K_FCLK	Functional
	INIT_48M_FCLK	Functional
	INIT_L4_ICLK	Interface
	INIT_960M_FCLK	Functional
FSUSB	INIT_48MC_FCLK	Functional
	INIT_L3_ICLK	Interface
	INIT_L4_ICLK	Interface
HSUSBHOST	HSIC_P1_480M_FCLK	Functional
	HSIC_P1_FCLK	Functional
	HSIC_P2_480M_FCLK	Functional
	HSIC_P2_FCLK	Functional
	INIT_48MC_FCLK	Functional (mandatory)
	INIT_48MC_FCLK	Functional (optional)
	INIT_L3_ICLK	Interface
	INIT_L4_ICLK	Interface
	UTMI_P1_FCLK	Functional
	UTMI_P2_FCLK	Functional
	UTMI_ROOT_FCLK	Functional
HSUSBOTG	INIT_L3_ICLK	Interface
	INIT_L4_ICLK	Interface
	OTG_60M_FCLK	Functional
HSUSBTLL	INIT_L4_ICLK	Interface
	TLL_CH0_FCLK	Functional
	TLL_CH1_FCLK	Functional

Table 3-125 lists the supported wake-up request generation capability for each module of the clock domain.

Table 3-125. CD_L3_INIT Modules Wake-Up Request

Module	Wake-Up Feature
HSI	Slave wake-up request (MPU_A9 -IRQ, MPU_M3 -IRQ, DSP -IRQ)/Master wake-up request
HSMMC1	Slave wake-up request (MPU_A9 -IRQ, MPU_M3 -IRQ, DSP -IRQ, sDMA -DMA)
HSMMC2	Slave wake-up request (MPU_A9 -IRQ, MPU_M3 -IRQ, DSP -IRQ, sDMA -DMA)
USBPHY	None
FSUSB	Slave wake-up request (MPU_A9 -IRQ, MPU_M3 -IRQ)/Master wake-up request
HSUSBHOST	Slave wake-up request (MPU_A9 -IRQ, MPU_M3 -IRQ)
HSUSBOTG	Slave wake-up request (MPU_A9 -IRQ, MPU_M3 -IRQ)
HSUSBTLL	Slave wake-up request (MPU_A9 -IRQ, MPU_M3 -IRQ)

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Table 3-126 lists the supported clock-management modes and associated software control bit fields for each module of the power domain.

Table 3-126. CD_L3_INIT Modules Clock-Management Modes and Control

Module	Clock-Management Protocol	Status Bit Field	Role
HSI	Slave/Master	CM_L3INIT_HSI_CLKCTRL[18] STBYST	Standby status
		CM_L3INIT_HSI_CLKCTRL[17:16] IDLEST	Idle status
HSMMC1	Master/Slave	CM_L3INIT_HSMMC1_CLKCTRL[18] STBYST	Standby status
		CM_L3INIT_HSMMC1_CLKCTRL[17:16] IDLEST	Idle status
HSMMC2	Master/Slave	CM_L3INIT_HSMMC2_CLKCTRL[18] STBYST	Standby status
		CM_L3INIT_HSMMC2_CLKCTRL[17:16] IDLEST	Idle status
USBPHY	Slave	CM_L3INIT_USBPHY_CLKCTRL[17:16] IDLEST	Idle status
FSUSB	Slave/Master	CM_L3INIT_FSUSB_CLKCTRL[18] STBYST	Standby status
		CM_L3INIT_FSUSB_CLKCTRL[17:16] IDLEST	Idle status
HSUSBHOST	Slave/Master	CM_L3INIT_HSUSBHOST_CLKCTRL[18] STBYST	Standby status
		CM_L3INIT_HSUSBHOST_CLKCTRL[17:16] IDLEST	Idle status
		CM_L3INIT_HSUSBHOST_CLKCTRL_RESTORE[18] STBYST	Standby status
		CM_L3INIT_HSUSBHOST_CLKCTRL_RESTORE[17:16] IDLEST	Idle status
HSUSBOTG	Slave/Master	CM_L3INIT_HSUSBOTG_CLKCTRL[18] STBYST	Standby status
		CM_L3INIT_HSUSBOTG_CLKCTRL[17:16] IDLEST	Idle status
HSUSBTLL	Slave	CM_L3INIT_HSUSBTLL_CLKCTRL[17:16] IDLEST	Idle status
		CM_L3INIT_HSUSBTLL_CLKCTRL_RESTORE[17:16] IDLEST	Idle status

Table 3-127 lists the supported clock-management modes and associated software control bit fields for each module of the power domain.

Table 3-127. CD_L3_INIT Modules Slave Clock-Management Modes and Control

Module	Disabled	Auto	Enabled	Control Bit Field	Access Type
HSI	Available	Available	N/A	CM_L3INIT_HSI_CLKCTRL[1:0] MODULEMODE	Read/Write
HSMMC1	Available	N/A	Available	CM_L3INIT_HSMMC1_CLKCTRL[1:0] MODULEMODE	Read/Write
HSMMC2	Available	N/A	Available	CM_L3INIT_HSMMC2_CLKCTRL[1:0] MODULEMODE	Read/Write

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Table 3-127. CD_L3_INIT Modules Slave Clock-Management Modes and Control (continued)

Module	Disabled	Auto	Enabled	Control Bit Field	Access Type
USBPHY	Available	Available	N/A	CM_L3INIT_USBPHY_CLKCTRL[1:0] MODULEMODE	Read/Write
FSUSB	Available	N/A	Available	CM_L3INIT_FSUSB_CLKCTRL[1:0] MODULEMODE	Read/Write
HSUSBHOST	Available	N/A	Available	CM_L3INIT_HSUSBHOST_CLKCTRL[1:0] MODULEMODE	Read/Write
HSUSBOTG	Available	Available	N/A	CM_L3INIT_HSUSBOTG_CLKCTRL[1:0] MODULEMODE	Read/Write
HSUSBTLL	Available	Available	N/A	CM_L3INIT_HSUSBTLL_CLKCTRL[1:0] MODULEMODE	Read/Write

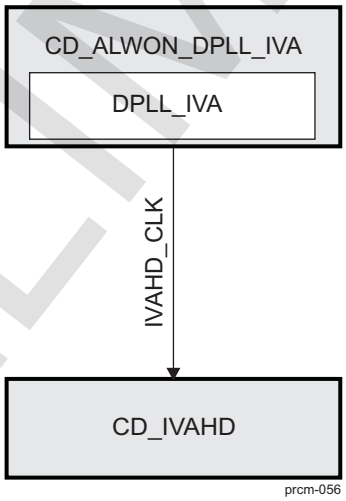
3.6.10 CD_IVAHD Clock Domain

This section identifies the modes supported by the clock domain, the associated control and status bits. It also identifies its dependencies with other clock domains of the device.

3.6.10.1 Overview

Figure 3-60 shows the overview of the clock domain.

Figure 3-60. CD_IVAHD Overview



3.6.10.2 Clock Domain Modes

Table 3-128 lists the clock domain modes supported by the clock domain.

Table 3-128. CD_IVAHD Clock Domain Modes

NO_SLEEP	SW_SLEEP	SW_WKUP	HW_AUTO
Available	Available	Available	Available

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Table 3-129 lists the clock domain state transition control and status bits for the clock in this clock domain.

Table 3-129. CD_IVAHD Control and Status Parameters

Parameter Name	Control/Status Bit Field
IVAHD_ROOT_CLK clock status	CM_IVAHD_CLKSTCTRL[8] CLKACTIVITY_IVAHD_CLK
Clock Domain State Transition Control	CM_IVAHD_CLKSTCTRL[1:0] CLKTRCTRL

3.6.10.3 Clock Domain Dependency

CD_IVAHD has no module wake-up dependency with any other clock domain of the device

3.6.10.3.1 Static Dependency

Table 3-130 lists the static dependency of the clock domain with respect to other clock domains of the device.

Table 3-130. CD_IVAHD Static Dependency Association Parameters

Clock Domain Name	Default Setting	Control Bit Field	Access Type
CD_L3_1	Disabled	CM_IVAHD_STATICDEP[5] L3_1_STATDEP	Read/Write
CD_L3_2	Always enabled	CM_IVAHD_STATICDEP[6] L3_2_STATDEP	Read only
CD_EMIF	Disabled	CM_IVAHD_STATICDEP[4] MEMIF_STATDEP	Read/Write

3.6.10.3.2 Dynamic Dependency

Table 3-131 lists the dynamic dependency of the clock domain with respect to other clock domains of the device.

Table 3-131. CD_IVAHD Dynamic Dependency Association Parameters

Clock Domain Name	Default Setting	Control Bit Field	Access Type
CD_L3_2	Always disabled	CM_IVAHD_DYNAMICDEP[6] L3_2_DYNDEP	Read only

3.6.10.4 Clock Domain Module Attributes

Table 3-132 lists for each module of the clock domain the clocks received by it and the role (that is, functional or interface clock).

Table 3-132. CD_IVAHD Modules Clocks Association

Module	Clock	Clock Type
IVAHD	IVAHD_ROOT_CLK	Interface and Functional
SL2	IVAHD_ROOT_CLK	Interface

Table 3-133 lists the supported wake-up request generation capability for each module of the clock domain.

Table 3-133. CD_IVAHD Modules Wake-Up Request

Module	Wake-Up Feature
IVAHD	None
SL2	None

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Table 3-134 lists the supported clock-management modes and associated software control bit fields for each module of the power domain.

Table 3-134. CD_IVAHD Modules Clock-Management Modes and Control

Module	Clock-Management Protocol	Status Bit Field	Role
IVAHD	Master/Slave	CM_IVAHD_IVAHD_CLKCTRL [18] STBYST	Standby status
		CM_IVAHD_IVAHD_CLKCTRL [17:16] IDLEST	Idle status
SL2	Slave	CM_IVAHD_SL2_CLKCTRL[17 :16] IDLEST	Idle status

Table 3-135 lists the supported clock-management modes and associated software control bit fields for each module of the power domain.

Table 3-135. CD_IVAHD Modules Slave Clock-Management Modes and Control

Module	Disabled	Auto	Enabled	Control Bit Field	Access Type
IVAHD	Available	Available	N/A	CM_IVAHD_IVAHD _CLKCTRL[1:0] MODULEMODE	Read/Write
SL2	Available	Available	N/A	CM_IVAHD_SL2_C LKCTRL[1:0] MODULEMODE	Read/Write

3.6.11 CD_SGX Clock Domain

This section identifies the modes supported by the clock domain, the associated control and status bits. It also identifies its dependencies with other clock domains of the device.

3.6.11.1 Overview

Figure 3-61 shows the overview of the clock domain.

Figure 3-61. CD_SGX Overview

3.6.11.2 Clock Domain Modes

Table 3-136 lists the clock domain modes supported by the clock domain.

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Table 3-136. CD_SGX Clock Domain Modes

NO_SLEEP	SW_SLEEP	SW_WKUP	HW_AUTO
Available	Available	Available	Available

Table 3-137 lists the clock domain state transition control and status bits for the clock in this clock domain.

Table 3-137. CD_SGX Control and Status Parameters

Parameter Name	Control/Status Bit Field
SGX_L3_ICLK clock status	CM_SGX_CLKSTCTRL[8] CLKACTIVITY_SGX_L3_ICLK
SGX_FCLK clock status	CM_SGX_CLKSTCTRL[9] CLKACTIVITY_SGX_FCLK
Clock Domain State Transition Control	CM_SGX_CLKSTCTRL[1:0] CLKTRCTRL

3.6.11.3 Clock Domain Dependency

CD_SGX has no module wake-up dependency with any other clock domain of the device.

3.6.11.3.1 Static Dependency

Table 3-138 lists the static dependency of the clock domain with respect to other clock domains of the device.

Table 3-138. CD_SGX Static Dependency Association Parameters

Clock Domain Name	Default Setting	Control Bit Field	Access Type
CD_IVAHD	Disabled	CM_SGX_STATICDEP[2] IVAHD_STATDEP	Read/Write
CD_L3_1	Disabled	CM_SGX_STATICDEP[5] L3_1_STATDEP	Read/Write
CD_L3_2	Always enabled	CM_SGX_STATICDEP[6] L3_2_STATDEP	Read only
CD_EMIF	Disabled	CM_SGX_STATICDEP[4] MEMIF_STATDEP	Read/Write

3.6.11.3.2 Dynamic Dependency

Table 3-139 lists the dynamic dependency of the clock domain with respect to other clock domains of the device.

Table 3-139. CD_SGX Dynamic Dependency Association Parameters

Clock Domain Name	Default Setting	Control Bit Field	Access Type
CD_L3_2	Always disabled	CM_SGX_DYNAMICDEP[6] L3_2_DYNDEP	Read only

3.6.11.4 Clock Domain Module Attributes

Table 3-140 identifies for each module of the clock domain the clocks received by it and the role (that is, functional or interface clock).

Table 3-140. CD_SGX Modules Clocks Association

Module	Clock	Clock Type
SGX	SGX_L3_ICLK	Interface
	SGX_FCLK	Functional

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Table 3-141 lists the supported wake-up request generation capability for each module of the clock domain.

Table 3-141. CD_SGX Modules Wake-Up Request

Module	Wake-Up Feature
SGX	None

Table 3-142 lists the supported clock-management modes and associated software control bit fields for each module of the power domain.

Table 3-142. CD_SGX Modules Clock-Management Modes and Control

Module	Clock-Management Protocol	Status Bit Field	Role
SGX	Master/Slave	CM_SGX_SGX_CLKCTRL[18] STBYST	Standby status
		CM_SGX_SGX_CLKCTRL[17:16] IDLEST	Idle status

Table 3-143 lists the supported clock-management modes and associated software control bit fields for each module of the power domain.

Table 3-143. CD_SGX Modules Slave Clock-Management Modes and Control

Module	Disabled	Auto	Enabled	Control Bit Field	Access Type
SGX	Available	N/A	Available	CM_SGX_SGX_CLKCTRL[1:0] MODULEMODE	Read/Write

3.6.12 CD_EMU Clock Domain

This section identifies the modes supported by the clock domain, the associated control and status bits. It also identifies its dependencies with other clock domains of the device.

3.6.12.1 Overview

Figure 3-62 shows the overview of the clock domain.

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Figure 3-62. CD_EMU Overview

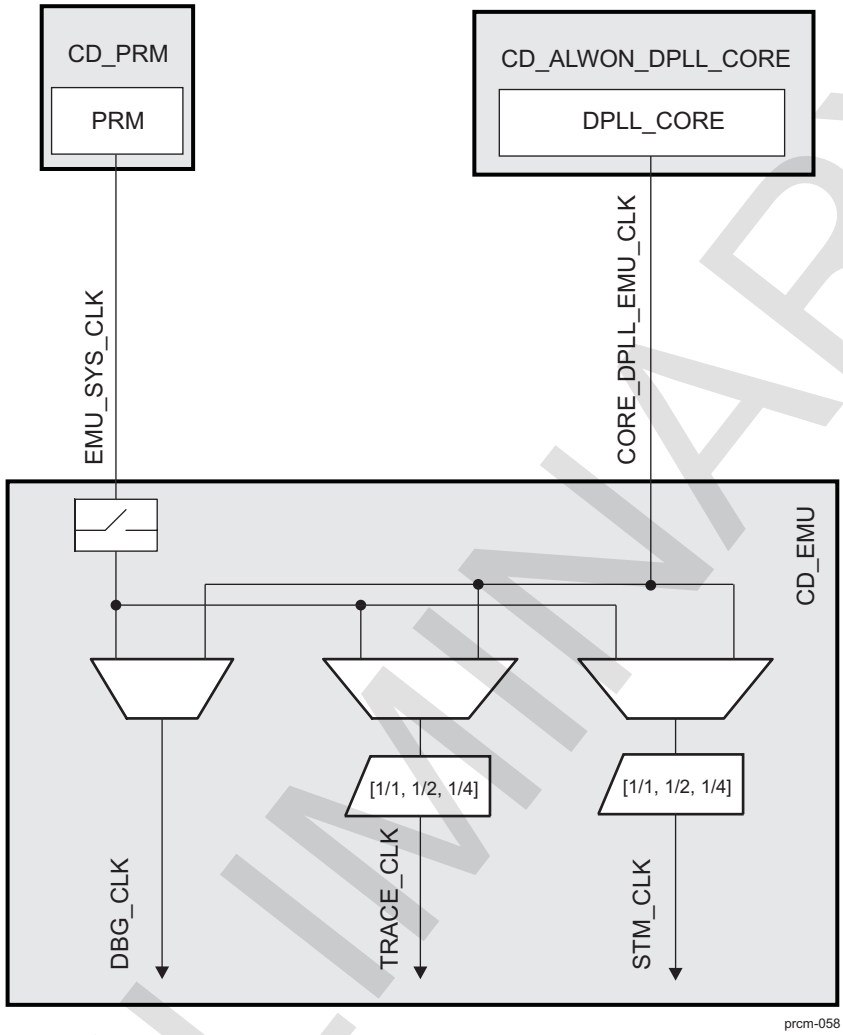

Table 3-144 lists controls for clock dividers or muxes in the clock domain.

Table 3-144. CD_EMU Clock Division and Muxing Control

Divider/Mux	Control Bit Field
Divider STM_CLK	CM_EMU_DEBUGSS_CLKCTRL[29:27] CLKSEL_PMD_STM_CLK
Divider TRACE_CLK	CM_EMU_DEBUGSS_CLKCTRL[26:24] CLKSEL_PMD_TRACE_CLK

3.6.12.2 Clock Domain Modes

Table 3-145 lists the clock domain modes supported by the clock domain.

Table 3-145. CD_EMU Clock Domain Modes

NO_SLEEP	SW_SLEEP	SW_WKUP	HW_AUTO
Not available	Not available	Available	Available

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Table 3-146 lists the clock domain state transition control and status bits for the clock in this clock domain.

Table 3-146. CD_EMU Control and Status Parameters

Parameter Name	Control/Status Bit Field
CORE_DPLL_EMU_CLK clock status	CM_EMU_CLKSTCTRL[9] CLKACTIVITY_CORE_DPLL_EMU_CLK
EMU_SYS_CLK clock status	CM_EMU_CLKSTCTRL[8] CLKACTIVITY_EMU_SYS_CLK
Clock Domain State Transition Control	CM_EMU_CLKSTCTRL[1:0] CLKTRCTRL

3.6.12.3 Clock Domain Dependency

CD_EMU has no static or module wake-up dependency with any other clock domain of the device.

3.6.12.3.1 Dynamic Dependency

Table 3-147 lists the dynamic dependency of the clock domain with respect to other clock domains of the device.

Table 3-147. CD_EMU Dynamic Dependency Association Parameters

Clock Domain Name	Default Setting	Control Bit Field	Access Type
CD_L3_2	Always enabled	CM_EMU_DYNAMICDEP[6] L3_2_DYNDEP	Read only

3.6.12.4 Clock Domain Module Attributes

Table 3-148 lists for each module of the clock domain the clocks received by it and the role (that is, functional or interface clock).

Table 3-148. CD_EMU Modules Clocks Association

Module	Clock	Clock Type
DEBUG	DBG_CLK	Interface
	EMU_SYS_CLK	Interface and Functional
	STM_CLK	Interface and Functional
	TRACE_CLK	Interface and Functional

Table 3-149 lists the supported wake-up request generation capability for each module of the clock domain.

Table 3-149. CD_EMU Modules Wake-Up Request

Module	Wake-Up Feature
DEBUG	Master wake-up request

3.6.13 CD_DSS Clock Domain

This section identifies the modes supported by the clock domain, the associated control and status bits. It also identifies its dependencies with other clock domains of the device.

3.6.13.1 Overview

Figure 3-63 shows the overview of the clock domain.

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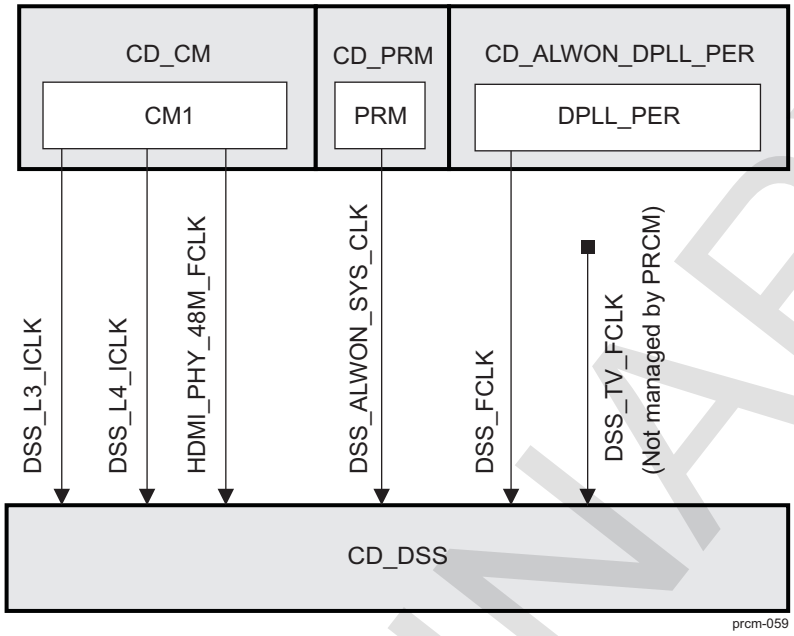
Figure 3-63. CD_DSS Overview



3.6.13.2 Clock Domain Modes

Table 3-150 lists the clock domain modes supported by the clock domain.

Table 3-150. CD_DSS Clock Domain Modes

NO_SLEEP	SW_SLEEP	SW_WKUP	HW_AUTO
Available	Available	Available	Available

Table 3-151 lists the clock domain state transition control and status bits for the clock in this clock domain.

Table 3-151. CD_DSS Control and Status Parameters

Parameter Name	Control/Status Bit Field
DSS_ALWON_SYS_CLK clock status	CM_DSS_CLKSTCTRL[10] CLKACTIVITY_DSS_ALWON_SYS_CLK
DSS_FCLK clock status	CM_DSS_CLKSTCTRL[9] CLKACTIVITY_DSS_FCLK
HDMI_PHY_48M_FCLK clock status	CM_DSS_CLKSTCTRL[11] CLKACTIVITY_HDMI_PHY_48M_FCLK
DSS_L3_ICLK clock status	CM_DSS_CLKSTCTRL[8] CLKACTIVITY_DSS_L3_ICLK(1)
Clock Domain State Transition Control	CM_DSS_CLKSTCTRL[1:0] CLKTRCTRL

(1) The VDAC function is not supported.

3.6.13.3 Clock Domain Dependency

3.6.13.3.1 Static Dependency

Table 3-152 lists the static dependency of the clock domain with respect to other clock domains of the device.

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Table 3-152. CD_DSS Static Dependency Association Parameters

Clock Domain Name	Default Setting	Control Bit Field	Access Type
CD_IVAHD	Disabled	CM_DSS_STATICDEP[2] IVAHD_STATDEP	Read/Write
CD_L3_1	Always enabled	CM_DSS_STATICDEP[5] L3_1_STATDEP	Read only
CD_L3_2	Disabled	CM_DSS_STATICDEP[6] L3_2_STATDEP	Read/Write
CD_EMIF	Disabled	CM_DSS_STATICDEP[4] MEMIF_STATDEP	Read/Write

3.6.13.3.2 Dynamic Dependency

Table 3-153 lists the dynamic dependency of the clock domain with respect to other clock domains of the device.

Table 3-153. CD_DSS Dynamic Dependency Association Parameters

Clock Domain Name	Default Setting	Control Bit Field	Access Type
CD_L3_1	Always disabled	CM_DSS_DYNAMICDEP[5] L3_1_DYNDEP	Read only

3.6.13.3.3 Wake-Up Dependency

Table 3-154 lists the wake-up dependency settings for the modules of this clock clock domain.

Table 3-154. CD_DSS Wake-Up Dependency Association Parameters

Originator Module	Originator Clock Domain	Servicing Clock Domain	Default Setting	Control Bit Field	Access Type
DSS-DSI1	CD_DSS	CD_DMA, CD_L3_1, CD_L3_2	Disabled	PM_DSS_DSS_WKDEP[7] WKUPDEP_DSI1_SDMA	Read/Write
DSS-DSI1	CD_DSS	CD_DSP	Disabled	PM_DSS_DSS_WKDEP[6] WKUPDEP_DSI1_DSP	Read/Write
DSS-DSI1	CD_DSS	CD_CORTEXM3	Disabled	PM_DSS_DSS_WKDEP[5] WKUPDEP_DSI1_MPU_M3	Read/Write
DSS-DSI1	CD_DSS	CD_CORTEXA9	Disabled	PM_DSS_DSS_WKDEP[4] WKUPDEP_DSI1_MPU	Read/Write
DSS-DSI2	CD_DSS	CD_CORTEXM3	Disabled	PM_DSS_DSS_WKDEP[9] WKUPDEP_DSI2_MPU_M3	Read/Write
DSS-DSI2	CD_DSS	CD_CORTEXA9	Disabled	PM_DSS_DSS_WKDEP[8] WKUPDEP_DSI2_MPU	Read/Write
DSS-DSI2	CD_DSS	CD_DMA, CD_L3_1, CD_L3_2	Disabled	PM_DSS_DSS_WKDEP[11] WKUPDEP_DSI2_SDMA	Read/Write
DSS-DSI2	CD_DSS	CD_DSP	Disabled	PM_DSS_DSS_WKDEP[10] WKUPDEP_DSI2_DSP	Read/Write

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Table 3-154. CD_DSS Wake-Up Dependency Association Parameters (continued)

Originator Module	Originator Clock Domain	Servicing Clock Domain	Default Setting	Control Bit Field	Access Type
DSS-HDMI	CD_DSS	CD_DMA, CD_L3_1, CD_L3_2	Enabled	PM_DSS_DSS_WKDEP[19] WKUPDEP_HDMIDMA_SDMA	Read/Write
DSS-HDMI	CD_DSS	CD_DSP	Disabled	PM_DSS_DSS_WKDEP[14] WKUPDEP_HDMIIRQ_DSP	Read/Write
DSS-HDMI	CD_DSS	CD_CORTEXM3	Disabled	PM_DSS_DSS_WKDEP[13] WKUPDEP_HDMIIRQ_MPU_M3	Read/Write
DSS-HDMI	CD_DSS	CD_CORTEXA9	Disabled	PM_DSS_DSS_WKDEP[12] WKUPDEP_HDMIIRQ_MPU	Read/Write
DSS-DISPC	CD_DSS	CD_CORTEXM3	Disabled	PM_DSS_DSS_WKDEP[1] WKUPDEP_DISPC_MPU_M3	Read/Write
DSS-DISPC	CD_DSS	CD_CORTEXA9	Disabled	PM_DSS_DSS_WKDEP[0] WKUPDEP_DISPC_MPU	Read/Write
DSS-DISPC	CD_DSS	CD_DSP	Disabled	PM_DSS_DSS_WKDEP[2] WKUPDEP_DISPC_DSP	Read/Write
DSS-DISPC	CD_DSS	CD_DMA, CD_L3_1, CD_L3_2	Disabled	PM_DSS_DSS_WKDEP[3] WKUPDEP_DISPC_SDMA	Read/Write

3.6.13.4 Clock Domain Module Attributes

Table 3-155 lists for each module of the clock domain the clocks received by it and the role (that is, functional or interface clock).

Table 3-155. CD_DSS Modules Clocks Association

Module	Clock	Clock Type
DSS	DSS_ALWON_SYS_CLK	Functional
	DSS_FCLK	Functional
	DSS_TV_FCLK	Functional
	HDMI_PHY_48M_FCLK	Functional
	DSS_L3_ICLK(1)	Interface
	DSS_L4_ICLK	Interface

(1) The VDAC function is not supported.

NOTE: DSS_TV_FCLK is sourced from fref_slicer_in input pin. To enable DSS_TV_FCLK it must be ungated in ALTCLKSRC[3] ENABLE_EXT and must be enabled in CM_DSS_DSS_CLKCTRL[11] OPTFCLKEN_TV_FCLK.

Table 3-156 lists the supported wake-up request generation capability for each module of the clock domain.

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Table 3-156. CD_DSS Modules Wake-Up Request

Module	Wake-Up Feature
DSS	Slave wake-up request (MPU_A9 -IRQ, MPU_M3 -IRQ, DSP -IRQ, sDMA -DMA)

Table 3-157 lists the supported clock-management modes and associated software control bit fields for each module of the power domain.

Table 3-157. CD_DSS Modules Clock-Management Modes and Control

Module	Clock-Management Protocol	Status Bit Field	Role
DSS	Master/Slave	CM_DSS_DSS_CLKCTRL[18] STBYST	Standby status
		CM_DSS_DSS_CLKCTRL[17:16] IDLEST	Idle status

Table 3-158 lists the supported clock-management modes and associated software control bit fields for each module of the power domain.

Table 3-158. CD_DSS Modules Slave Clock-Management Modes and Control

Module	Disabled	Auto	Enabled	Control Bit Field	Access Type
DSS	Available	N/A	Available	CM_DSS_DSS_CLKCTRL[1:0] MODULEMODE	Read/Write

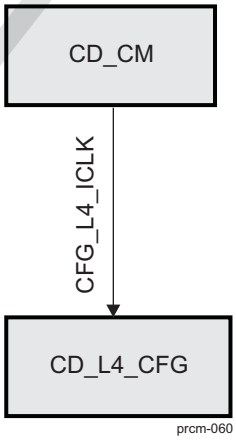
3.6.14 CD_L4_CFG Clock Domain

This section identifies the modes supported by the clock domain, the associated control and status bits. It also identifies its dependencies with other clock domains of the device.

3.6.14.1 Overview

Figure 3-64 shows the overview of the clock domain.

Figure 3-64. CD_L4_CFG Overview



3.6.14.2 Clock Domain Modes

Table 3-159 lists the clock domain modes supported by the clock domain.

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Table 3-159. CD_L4_CFG Clock Domain Modes

NO_SLEEP	SW_SLEEP	SW_WKUP	HW_AUTO
Available	Not available	Not available	Available

Table 3-160 lists the clock domain state transition control and status bits for the clock in this clock domain.

Table 3-160. CD_L4_CFG Control and Status Parameters

Parameter Name	Control/Status Bit Field
CFG_L4_ICLK clock status	CM_L4CFG_CLKSTCTRL[8] CLKACTIVITY_CFG_L4_ICLK
Clock Domain State Transition Control	CM_L4CFG_CLKSTCTRL[1:0] CLKTRCTRL

3.6.14.3 Clock Domain Dependency

CD_L4_CFG has no static or module wake-up dependency with any other clock domain of the device.

3.6.14.3.1 Dynamic Dependency

Table 3-161 lists the dynamic dependency of the clock domain with respect to other clock domains of the device.

Table 3-161. CD_L4_CFG Dynamic Dependency Association Parameters

Clock Domain Name	Default Setting	Control Bit Field	Access Type
CD_C2C	Always enabled	CM_L4CFG_DYNAMICDEP[18] C2C_DYNDEP	Read only
CD_DSS	Always enabled	CM_L4CFG_DYNAMICDEP[8] DSS_DYNDEP	Read only
CD_CAM	Always disabled	CM_L4CFG_DYNAMICDEP[9] ISS_DYNDEP	Read only
CD_L3_1	Always enabled	CM_L4CFG_DYNAMICDEP[5] L3_1_DYNDEP	Read only
CD_L3_2	Always enabled	CM_L4CFG_DYNAMICDEP[6] L3_2_DYNDEP	Read only
CD_L3_INIT	Always enabled	CM_L4CFG_DYNAMICDEP[7] L3INIT_DYNDEP	Read only
CD_EMIF	Always enabled	CM_L4CFG_DYNAMICDEP[4] MEMIF_DYNDEP	Read only
CD_DMA	Always enabled	CM_L4CFG_DYNAMICDEP[11] SDMA_DYNDEP	Read only
CD_DSP	Always enabled	CM_L4CFG_DYNAMICDEP[1] DSP_DYNDEP	Read only

3.6.14.4 Clock Domain Module Attributes

Table 3-162 lists for each module of the clock domain the clocks received by it and the role (that is, functional or interface clock).

Table 3-162. CD_L4_CFG Modules Clocks Association

Module	Clock	Clock Type
SYSCTRL_PADCONF_CORE	CFG_L4_ICLK	Functional
SYSCTRL_GENERAL_CORE	CFG_L4_ICLK	Functional
	CORE_TS_FCLK	Functional
SPINLOCK	CFG_L4_ICLK	Interface
L4_CFG interconnect	CFG_L4_ICLK	Interface
MAILBOX	CFG_L4_ICLK	Interface

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Table 3-162. CD_L4_CFG Modules Clocks Association (continued)

Module	Clock	Clock Type
SAR_ROM	CFG_L4_ICLK	Interface

Table 3-163 lists the supported wake-up request generation capability for each module of the clock domain.

Table 3-163. CD_L4_CFG Modules Wake-Up Request

Module	Wake-Up Feature
SYSCTRL_PADCONF_CORE	None
SYSCTRL_GENERAL_CORE	None
SPINLOCK	None
L4_CFG interconnect	None
MAILBOX	None
SAR_ROM	None

Table 3-164 lists the supported clock-management modes and associated software control bit fields for each module of the power domain.

Table 3-164. CD_L4_CFG Modules Clock-Management Modes and Control

Module	Clock-Management Protocol	Status Bit Field	Role
SPINLOCK	Slave	CM_L4CFG_SPINLOCK_CLKCTRL[17:16] IDLEST	Idle status
L4_CFG interconnect	Slave	CM_L4CFG_L4_CFG_CLKCTRL[17:16] IDLEST	Idle status
MAILBOX	Slave	CM_L4CFG_MAILBOX_CLKCTRL[17:16] IDLEST	Idle status
SAR_ROM	Slave	CM_L4CFG_SAR_ROM_CLKCTRL[17:16] IDLEST	Idle status

Table 3-165 lists the supported clock-management modes and associated software control bit fields for each module of the power domain.

Table 3-165. CD_L4_CFG Modules Slave Clock-Management Modes and Control

Module	Disabled	Auto	Enabled	Control Bit Field	Access Type
SPINLOCK	N/A	Available	N/A	CM_L4CFG_SPINLOCK_CLKCTRL[1:0] MODULEMODE	Read only
L4_CFG interconnect	N/A	Available	N/A	CM_L4CFG_L4_CFG_CLKCTRL[1:0] MODULEMODE	Read only
MAILBOX	N/A	Available	N/A	CM_L4CFG_MAILBOX_CLKCTRL[1:0] MODULEMODE	Read only
SAR_ROM	N/A	Available	N/A	CM_L4CFG_SAR_ROM_CLKCTRL[1:0] MODULEMODE	Read only

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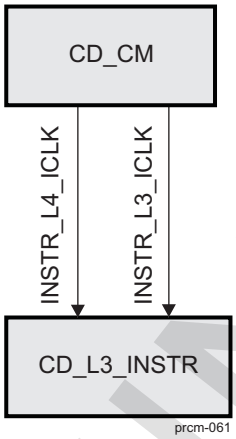
3.6.15 CD_L3_INSTR Clock Domain

This section identifies the modes supported by the clock domain, the associated control and status bits. It also identifies its dependencies with other clock domains of the device.

3.6.15.1 Overview

Figure 3-65 shows the overview of the clock domain.

Figure 3-65. CD_L3_INSTR Overview



3.6.15.2 Clock Domain Modes

Table 3-166 lists the clock domain modes supported by the clock domain.

Table 3-166. CD_L3_INSTR Clock Domain Modes

NO_SLEEP	SW_SLEEP	SW_WKUP	HW_AUTO
Not available	Not available	Not available	Available

Table 3-167 lists the clock domain state transition control and status bits for the clock in this clock domain.

Table 3-167. CD_L3_INSTR Control and Status Parameters

Parameter Name	Control/Status Bit Field
INSTR_L3_ICLK clock status	CM_L3INSTR_CLKSTCTRL[8] CLKACTIVITY_L3_INSTR_ICLK
Clock Domain State Transition Control	CM_L3INSTR_CLKSTCTRL[1:0] CLKTRCTRL

3.6.15.3 Clock Domain Dependency

CD_L3_INSTR has no static, dynamic, or module wake-up dependency with any other clock domain of the device

3.6.15.4 Clock Domain Module Attributes

Table 3-168 lists for each module of the clock domain the clocks received by it and the role (that is, functional or interface clock).

Table 3-168. CD_L3_INSTR Modules Clocks Association

Module	Clock	Clock Type
L3_3 interconnect	INSTR_L3_ICLK	Interface
	INSTR_L4_ICLK	Interface
L3_INSTR interconnect	INSTR_L3_ICLK	Interface

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Table 3-168. CD_L3_INSTR Modules Clocks Association (continued)

Module	Clock	Clock Type
OCP_WP1	INSTR_L3_ICLK	Interface
	INSTR_L4_ICLK	Interface

Table 3-169 lists the supported wake-up request generation capability for each module of the clock domain.

Table 3-169. CD_L3_INSTR Modules Wake-Up Request

Module	Wake-Up Feature
L3_3 interconnect	None
L3_INSTR interconnect	None

Table 3-170 lists the supported clock-management modes and associated software control bit fields for each module of the power domain.

Table 3-170. CD_L3_INSTR Modules Clock-Management Modes and Control

Module	Clock-Management Protocol	Status Bit Field	Role
L3_3 interconnect	Slave	CM_L3INSTR_L3_3_CLKCTRL[17:16] IDLEST	Idle status
		CM_L3INSTR_L3_3_CLKCTRL_RESTORE[17:16] IDLEST	Idle status
L3_INSTR interconnect	Slave	CM_L3INSTR_L3_INSTR_CLKCTRL[17:16] IDLEST	Idle status
		CM_L3INSTR_L3_INSTR_CLKCTRL_RESTORE[17:16] IDLEST	Idle status

Table 3-171 lists the supported clock-management modes and associated software control bit fields for each module of the power domain.

Table 3-171. CD_L3_INSTR Modules Slave Clock-Management Modes and Control

Module	Disabled	Auto	Enabled	Control Bit Field	Access Type
L3_3 interconnect	Available	Available	N/A	CM_L3INSTR_L3_3_CLKCTRL[1:0] MODULEMODE	Read/Write
L3_3 interconnect	Available	Available	N/A	CM_L3INSTR_L3_3_CLKCTRL_RESTORE[1:0] MODULEMODE	Read/Write
L3_INSTR interconnect	Available	Available	N/A	CM_L3INSTR_L3_INSTR_CLKCTRL[1:0] MODULEMODE	Read/Write
L3_INSTR interconnect	Available	Available	N/A	CM_L3INSTR_L3_INSTR_CLKCTRL_RESTORE[1:0] MODULEMODE	Read/Write

3.6.16 CD_L3_2 Clock Domain

This section identifies the modes supported by the clock domain, the associated control and status bits. It also identifies its dependencies with other clock domains of the device.

3.6.16.1 Overview

Figure 3-66 shows the overview of the clock domain.

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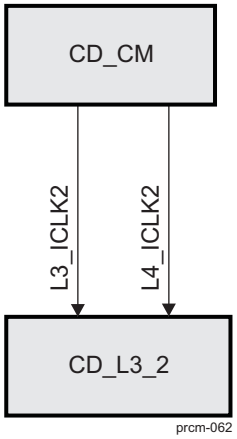
Figure 3-66. CD_L3_2 Overview



3.6.16.2 Clock Domain Modes

Table 3-172 lists the clock domain modes supported by the clock domain.

Table 3-172. CD_L3_2 Clock Domain Modes

NO_SLEEP	SW_SLEEP	SW_WKUP	HW_AUTO
Available	Not available	Not available	Available

Table 3-173 lists the clock domain state transition control and status bits for the clock in this clock domain.

Table 3-173. CD_L3_2 Control and Status Parameters

Parameter Name	Control/Status Bit Field
L3_ICLK2 clock status	CM_L3_2_CLKSTCTRL[8] CLKACTIVITY_L3_2_ICLK
Clock Domain State Transition Control	CM_L3_2_CLKSTCTRL[1:0] CLKTRCTRL

3.6.16.3 Clock Domain Dependency

CD_L3_2 has no static or module wake-up dependency with any other clock domain of the device.

3.6.16.3.1 Dynamic Dependency

Table 3-174 lists the dynamic dependency of the clock domain with respect to other clock domains of the device.

Table 3-174. CD_L3_2 Dynamic Dependency Association Parameters

Clock Domain Name	Default Setting	Control Bit Field	Access Type
CD_C2C	Always enabled	CM_L3_2_DYNAMICDEP[18] C2C_DYNDEP	Read only
CD_DSS	Always enabled	CM_L3_2_DYNAMICDEP[8] DSS_DYNDEP	Read only
CD_CORTEXM3	Always enabled	CM_L3_2_DYNAMICDEP[0] MPU_M3_DYNDEP	Read only
CD_SGX	Always enabled	CM_L3_2_DYNAMICDEP[10] SGX_DYNDEP	Read only
CD_CAM	Always disabled	CM_L3_2_DYNAMICDEP[9] ISS_DYNDEP	Read only
CD_IVAHD	Always enabled	CM_L3_2_DYNAMICDEP[2] IVAHD_DYNDEP	Read only

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Table 3-174. CD_L3_2 Dynamic Dependency Association Parameters (continued)

Clock Domain Name	Default Setting	Control Bit Field	Access Type
CD_L3_1	Always enabled	CM_L3_2_DYNAMICDEP[5] L3_1_DYNDEP	Read only
CD_L3_INIT	Always enabled	CM_L3_2_DYNAMICDEP[7] L3INIT_DYNDEP	Read only
CD_L4_PER	Always enabled	CM_L3_2_DYNAMICDEP[13] L4PER_DYNDEP	Read only

3.6.16.4 Clock Domain Module Attributes

Table 3-175 lists for each module of the clock domain the clocks received by it and the role (that is, functional or interface clock).

Table 3-175. CD_L3_2 Modules Clocks Association

Module	Clock	Clock Type
GPMC	L3_ICLK2	Interface
L3_2 interconnect	L3_ICLK2	Interface
	L4_ICLK2	Interface
OCMC_RAM	L3_ICLK2	Interface

Table 3-176 lists the supported wake-up request generation capability for each module of the clock domain.

Table 3-176. CD_L3_2 Modules Wake-Up Request

Module	Wake-Up Feature
GPMC	None
L3_2 interconnect	None
OCMC_RAM	None

Table 3-177 lists the supported clock-management modes and associated software control bit fields for each module of the power domain.

Table 3-177. CD_L3_2 Modules Clock-Management Modes and Control

Module	Clock-Management Protocol	Status Bit Field	Role
GPMC	Slave	CM_L3_2_GPMC_CLKCTRL[17:16] IDLEST	Idle status
L3_2 interconnect	Slave	CM_L3_2_L3_2_CLKCTRL[17:16] IDLEST	Idle status
OCMC_RAM	Slave	CM_L3_2_OCMC_RAM_CLKCTRL[17:16] IDLEST	Idle status

Table 3-178 lists the supported clock management modes and associated software control bit fields for each module of the power domain.

Table 3-178. CD_L3_2 Modules Slave Clock Management Modes and Control

Module	Disabled	Auto	Enabled	Control Bit Field	Access Type
GPMC	Available	Available	N/A	CM_L3_2_GPMC_CLKCTRL[1:0] MODULEMODE	Read/Write
L3_2 interconnect	N/A	Available	N/A	CM_L3_2_L3_2_CLKCTRL[1:0] MODULEMODE	Read only

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Table 3-178. CD_L3_2 Modules Slave Clock Management Modes and Control (continued)

Module	Disabled	Auto	Enabled	Control Bit Field	Access Type
OCMC_RAM	N/A	Available	N/A	CM_L3_2_OCMC_RAM_CLKCTRL[1:0] MODULEMODE	Read only

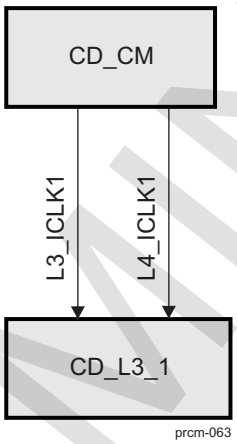
3.6.17 CD_L3_1 Clock Domain

This section identifies the modes supported by the clock domain, the associated control and status bits. It also identifies its dependencies with other clock domains of the device.

3.6.17.1 Overview

Figure 3-67 shows the overview of the clock domain.

Figure 3-67. CD_L3_1 Overview



3.6.17.2 Clock Domain Modes

Table 3-179 lists the clock domain modes supported by the clock domain.

Table 3-179. CD_L3_1 Clock Domain Modes

NO_SLEEP	SW_SLEEP	SW_WKUP	HW_AUTO
Available	Not available	Not available	Available

Table 3-180 lists the clock domain state transition control and status bits for the clock in this clock domain.

Table 3-180. CD_L3_1 Control and Status Parameters

Parameter Name	Control/Status Bit Field
L3_ICLK1 clock status	CM_L3_1_CLKSTCTRL[8] CLKACTIVITY_L3_1_ICLK
Clock Domain State Transition Control	CM_L3_1_CLKSTCTRL[1:0] CLKTRCTRL

3.6.17.3 Clock Domain Dependency

CD_L3_1 has no static or module wake-up dependency with any other clock domain of the device.

3.6.17.3.1 Dynamic Dependency

Table 3-181 lists the dynamic dependency of the clock domain with respect to other clock domains of the device.

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Table 3-181. CD_L3_1 Dynamic Dependency Association Parameters

Clock Domain Name	Default Setting	Control Bit Field	Access Type
CD_ABE	Always enabled	CM_L3_1_DYNAMICDEP[3] ABE_DYNDEP	Read only
CD_L3_2	Always enabled	CM_L3_1_DYNAMICDEP[6] L3_2_DYNDEP	Read only
CD_L4_CFG	Always enabled	CM_L3_1_DYNAMICDEP[12] L4CFG_DYNDEP	Read only
CD_EMIF	Always enabled	CM_L3_1_DYNAMICDEP[4] MEMIF_DYNDEP	Read only

3.6.17.4 Clock Domain Module Attributes

Table 3-182 lists for each module of the clock domain the clocks received by it and the role (that is, functional or interface clock).

Table 3-182. CD_L3_1 Modules Clocks Association

Module	Clock	Clock Type
L3_1 interconnect	L3_ICLK1	Interface
	L4_ICLK1	Interface

Table 3-183 lists the supported wake-up request generation capability for each module of the clock domain.

Table 3-183. CD_L3_1 Modules Wake-Up Request

Module	Wake-Up Feature
L3_1 interconnect	None

Table 3-184 lists the supported clock management modes and associated software control bit fields for each module of the power domain.

Table 3-184. CD_L3_1 Modules Clock Management Modes and Control

Module	Clock-Management Protocol	Status Bit Field	Role
L3_1 interconnect	Slave	CM_L3_1_L3_1_CLKCTRL[17:16] IDLEST	Idle status

Table 3-185 lists the supported clock management modes and associated software control bit fields for each module of the power domain.

Table 3-185. CD_L3_1 Modules Slave Clock Management Modes and Control

Module	Disabled	Auto	Enabled	Control Bit Field	Access Type
L3_1 interconnect	N/A	Available	N/A	CM_L3_1_L3_1_CLKCTRL[1:0] MODULEMODE	Read only

3.6.18 CD_EMIF Clock Domain

This section identifies the modes supported by the clock domain, the associated control and status bits. It also identifies its dependencies with other clock domains of the device.

3.6.18.1 Overview

Figure 3-68 shows the overview of the clock domain.

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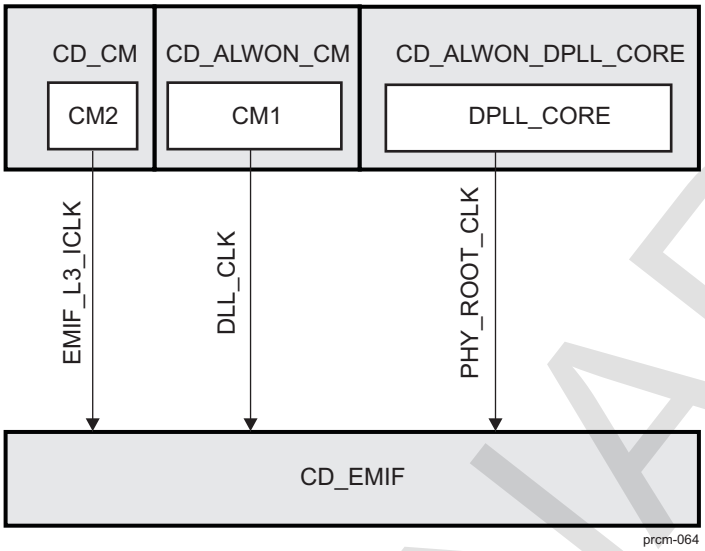
Figure 3-68. CD_EMIF Overview



3.6.18.2 Clock Domain Modes

Table 3-186 lists the clock domain modes supported by the clock domain.

Table 3-186. CD_EMIF Clock Domain Modes

NO_SLEEP	SW_SLEEP	SW_WKUP	HW_AUTO
Available	Not available	Available	Available

Table 3-187 lists the clock domain state transition control and status bits for the clock in this clock domain.

Table 3-187. CD_EMIF Control and Status Parameters

Parameter Name	Control/Status Bit Field
DLL_CLK clock status	CM_MEMIF_CLKSTCTRL[9] CLKACTIVITY_DLL_CLK
EMIF_L3_ICLK clock status	CM_MEMIF_CLKSTCTRL[8] CLKACTIVITY_L3_EMIF_ICLK
PHY_ROOT_CLK clock status	CM_MEMIF_CLKSTCTRL[10] CLKACTIVITY_PHY_ROOT_CLK
Clock Domain State Transition Control	CM_MEMIF_CLKSTCTRL[1:0] CLKTRCTRL

3.6.18.3 Clock Domain Dependency

CD_EMIF has no static, dynamic, or module wake-up dependency with any other clock domain of the device.

3.6.18.4 Clock Domain Module Attributes

Table 3-188 lists for each module of the clock domain the clocks received by it and the role (that is, functional or interface clock).

Table 3-188. CD_EMIF Modules Clocks Association

Module	Clock	Clock Type
DLL	DLL_CLK	Functional
DMM	EMIF_L3_ICLK	Interface
EMIF1	DLL_CLK	Interface
	EMIF_L3_ICLK	Interface

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Table 3-188. CD_EMIF Modules Clocks Association (continued)

Module	Clock	Clock Type
	EMIF_FCLK[1]	Functional
	EOCP_MA_ICLK[2]	Interface
	EOCP_L3_ICLK[2]	Interface
EMIF2	DLL_CLK	Interface
	EMIF_L3_ICLK	Interface
	EMIF_FCLK[1]	Functional
	EOCP_MA_ICLK[2]	Interface
	EOCP_L3_ICLK[2]	Interface
EMIF_FW	EMIF_L3_ICLK	Interface
	EMIF_L4_ICLK	Interface

(1) PHY_ROOT_CLK goes into DDRPHY. EMIF_FCLK comes out of DDRPHY and is PHY_ROOT_CLK divided by 4. DDR_PHY_CLK is PHY_ROOT_CLK divided by 2.

(2) EMIF modules are clocked by EOCP_MA_ICLK when MPU is active, otherwise EOCP_L3_ICLK clock is used.

Table 3-189 lists the supported wake-up request generation capability for each module of the clock domain.

Table 3-189. CD_EMIF Modules Wake-Up Request

Module	Wake-Up Feature
DDRPHY	None
DLL	None
DMM	None
EMIF1	None
EMIF2	None
EMIF_FW	None

Table 3-190 lists the supported clock-management modes and associated software control bit fields for each module of the power domain.

Table 3-190. CD_EMIF Modules Clock-Management Modes and Control

Module	Clock-Management Protocol	Status Bit Field	Role
DMM	Slave	CM_MEMIF_DMM_CLKCTRL[17:16] IDLEST	Idle status
EMIF1	Slave	CM_MEMIF_EMIF_1_CLKCTRL[17:16] IDLEST	Idle status
EMIF2	Slave	CM_MEMIF_EMIF_2_CLKCTRL[17:16] IDLEST	Idle status
EMIF_FW	Slave	CM_MEMIF_EMIF_FW_CLKCTRL[17:16] IDLEST	Idle status

Table 3-191 lists the supported clock-management modes and associated software control bit fields for each module of the power domain.

Table 3-191. CD_EMIF Modules Slave Clock-Management Modes and Control

Module	Disabled	Auto	Enabled	Control Bit Field	Access Type
DMM	N/A	Available	N/A	CM_MEMIF_DMM_CLKCTRL[1:0] MODULEMODE	Read only
EMIF1	Available	Available	N/A	CM_MEMIF_EMIF_1_CLKCTRL[1:0] MODULEMODE	Read/Write

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Table 3-191. CD_EMIF Modules Slave Clock-Management Modes and Control (continued)

Module	Disabled	Auto	Enabled	Control Bit Field	Access Type
EMIF2	Available	Available	N/A	CM_MEMIF_EMIF_2_CLKCTRL[1:0] MODULEMODE	Read/Write
EMIF_FW	N/A	Available	N/A	CM_MEMIF_EMIF_FW_CLKCTRL[1:0] MODULEMODE	Read only

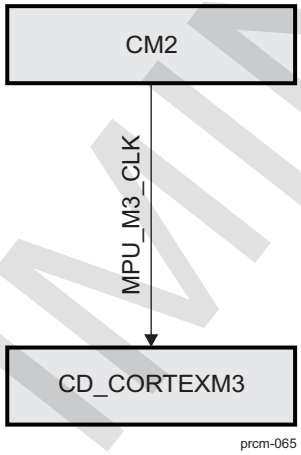
3.6.19 CD_CORTEXM3 Clock Domain

This section identifies the modes supported by the clock domain, the associated control and status bits. It also identifies its dependencies with other clock domains of the device.

3.6.19.1 Overview

Figure 3-69 shows the overview of the clock domain.

Figure 3-69. CD_CORTEXM3 Overview



3.6.19.2 Clock Domain Modes

Table 3-192 lists the clock domain modes supported by the clock domain.

Table 3-192. CD_CORTEXM3 Clock Domain Modes

NO_SLEEP	SW_SLEEP	SW_WKUP	HW_AUTO
Available	Available	Available	Available

Table 3-193 lists the clock domain state transition control and status bits for the clock in this clock domain.

Table 3-193. CD_CORTEXM3 Control and Status Parameters

Parameter Name	Control/Status Bit Field
MPU_M3_CLK clock status	CM_MPU_M3_CLKSTCTRL[8] CLKACTIVITY_MPU_M3_CLK
Clock Domain State Transition Control	CM_MPU_M3_CLKSTCTRL[1:0] CLKTRCTRL

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3.6.19.3 Clock Domain Dependency

CD_CORTEXM3 has no module wake-up dependency with any other clock domain of the device.

3.6.19.3.1 Static Dependency

Table 3-194 lists the static dependency of the clock domain with respect to other clock domains of the device.

Table 3-194. CD_CORTEXM3 Static Dependency Association Parameters

Clock Domain Name	Default Setting	Control Bit Field	Access Type
CD_ABE	Disabled	CM_MPU_M3_STATICDEP[3] ABE_STATDEP	Read/Write
CD_DSS	Disabled	CM_MPU_M3_STATICDEP[8] DSS_STATDEP	Read/Write
CD_SGX	Disabled	CM_MPU_M3_STATICDEP[10] SGX_STATDEP	Read/Write
CD_CAM	Always disabled	CM_MPU_M3_STATICDEP[9] ISS_STATDEP	Read only
CD_IVAHD	Disabled	CM_MPU_M3_STATICDEP[2] IVAHD_STATDEP	Read/Write
CD_L3_1	Enabled	CM_MPU_M3_STATICDEP[5] L3_1_STATDEP	Read/Write
CD_L3_2	Enabled	CM_MPU_M3_STATICDEP[6] L3_2_STATDEP	Read/Write
CD_L3_INIT	Disabled	CM_MPU_M3_STATICDEP[7] L3INIT_STATDEP	Read/Write
CD_L4_CFG	Enabled	CM_MPU_M3_STATICDEP[12] L4CFG_STATDEP	Read/Write
CD_L4_PER	Disabled	CM_MPU_M3_STATICDEP[13] L4PER_STATDEP	Read/Write
CD_EMIF	Enabled	CM_MPU_M3_STATICDEP[4] MEMIF_STATDEP	Read/Write
CD_DMA	Always disabled	CM_MPU_M3_STATICDEP[11] SDMA_STATDEP	Read only
CD_DSP	Disabled	CM_MPU_M3_STATICDEP[1] DSP_STATDEP	Read/Write

3.6.19.3.2 Dynamic Dependency

Table 3-195 lists the dynamic dependency of the clock domain with respect to other clock domains of the device.

Table 3-195. CD_CORTEXM3 Dynamic Dependency Association Parameters

Clock Domain Name	Default Setting	Control Bit Field	Access Type
CD_CAM	Always disabled	CM_MPU_M3_DYNAMICDEP[9] ISS_DYNDEP	Read only
CD_L3_2	Always enabled	CM_MPU_M3_DYNAMICDEP[6] L3_2_DYNDEP	Read only

3.6.19.4 Clock Domain Module Attributes

Table 3-196 lists for each module of the clock domain the clocks received by it and the role (that is, functional or interface clock).

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Table 3-196. CD_CORTEXM3 Modules Clocks Association

Module	Clock	Clock Type
CORTEXM3	MPU_M3_CLK	Interface and functional

Table 3-197 lists the supported wake-up request generation capability for each module of the clock domain.

Table 3-197. CD_CORTEXM3 Modules Wake-Up Request

Module	Wake-Up Feature
CORTEXM3	Master wake-up request

Table 3-198 lists the supported clock-management modes and associated software control bit fields for each module of the power domain.

Table 3-198. CD_CORTEXM3 Modules Clock-Management Modes and Control

Module	Clock-Management Protocol	Status Bit Field	Role
CORTEXM3	Master/Slave	CM_MPU_M3_MPU_M3_CLKCTRL[18] STBYST	Standby status
		CM_MPU_M3_MPU_M3_CLKCTRL[17:16] IDLEST	Idle status

Table 3-199 lists the supported clock-management modes and associated software control bit fields for each module of the power domain.

Table 3-199. CD_CORTEXM3 Modules Slave Clock-Management Modes and Control

Module	Disabled	Auto	Enabled	Control Bit Field	Access Type
CORTEXM3	Available	Available	N/A	CM_MPU_M3_MPU_M3_CLKCTRL[1:0] MODULEMODE	Read/Write

3.6.20 CD_DMA Clock Domain

This section identifies the modes supported by the clock domain, the associated control and status bits. It also identifies its dependencies with other clock domains of the device.

3.6.20.1 Overview

Figure 3-70 shows the overview of the clock domain.

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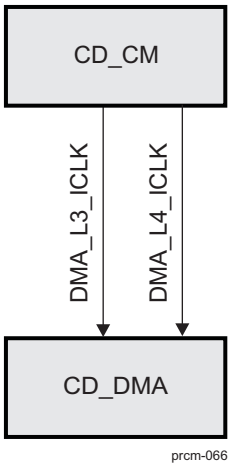
Figure 3-70. CD_DMA Overview



3.6.20.2 Clock Domain Modes

Table 3-200 lists the clock domain modes supported by the clock domain.

Table 3-200. CD_DMA Clock Domain Modes

NO_SLEEP	SW_SLEEP	SW_WKUP	HW_AUTO
Available	Not available	Available	Available

Table 3-201 lists the clock domain state transition control and status bits for the clock in this clock domain.

Table 3-201. CD_DMA Control and Status Parameters

Parameter Name	Control/Status Bit Field
DMA_L3_ICLK clock status	CM_SDMA_CLKSTCTRL[8] CLKACTIVITY_DMA_L3_ICLK
Clock Domain State Transition Control	CM_SDMA_CLKSTCTRL[1:0] CLKTRCTRL

3.6.20.3 Clock Domain Dependency

CD_DMA has a permanently enabled static dependency to the CD_L3_2 clock domain. It has no dynamic or module wake-up dependency with any other clock domain of the device.

3.6.20.4 Clock Domain Module Attributes

Table 3-202 lists for each module of the clock domain the clocks received by it and the role (that is, functional or interface clock).

Table 3-202. CD_DMA Modules Clocks Association

Module	Clock	Clock Type
sDMA	DMA_L3_ICLK	Interface and Functional
	DMA_L4_ICLK	Interface

Table 3-203 lists the supported wake-up request generation capability for each module of the clock domain.

Table 3-203. CD_DMA Modules Wake-Up Request

Module	Wake-Up Feature
sDMA	Master wake-up request

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Table 3-204 lists the supported clock-management modes and associated software control bit fields for each module of the power domain.

Table 3-204. CD_DMA Modules Clock-Management Modes and Control

Module	Clock-Management Protocol	Status Bit Field	Role
sDMA	Master/Slave	CM_SDMA_SDMA_CLKCTRL[18] STBYST	Standby status
		CM_SDMA_SDMA_CLKCTRL[17:16] IDLEST	Idle status

Table 3-205 lists the supported clock management modes and associated software control bit fields for each module of the power domain.

Table 3-205. CD_DMA Modules Slave Clock Management Modes and Control

Module	Disabled	Auto	Enabled	Control Bit Field	Access Type
sDMA	N/A	Available	N/A	CM_SDMA_SDMA_CLKCTRL[1:0] MODULEMODE	Read only

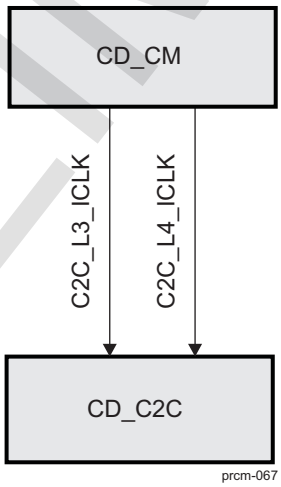
3.6.21 CD_C2C Clock Domain

This section identifies the modes supported by the clock domain, the associated control and status bits. It also identifies its dependencies with other clock domains of the device.

3.6.21.1 Overview

Figure 3-71 shows the overview of the clock domain.

Figure 3-71. CD_C2C Overview



3.6.21.2 Clock Domain Modes

Table 3-206 lists the clock domain modes supported by the clock domain.

Table 3-206. CD_C2C Clock Domain Modes

NO_SLEEP	SW_SLEEP	SW_WKUP	HW_AUTO
Available	Not available	Available	Available

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Table 3-207 lists the clock domain state transition control and status bits for the clock in this clock domain.

Table 3-207. CD_C2C Control and Status Parameters

Parameter Name	Control/Status Bit Field
C2C_L3_ICLK clock status	CM_C2C_CLKSTCTRL[8] CLKACTIVITY_L3_C2C_ICLK
C2C_L3X2_ICLK clock status	CM_C2C_CLKSTCTRL[10] CLKACTIVITY_L3X2_C2C_ICLK
C2C_L4_ICLK clock status	CM_C2C_CLKSTCTRL[9] CLKACTIVITY_L4_C2C_ICLK
Clock Domain State Transition Control	CM_C2C_CLKSTCTRL[1:0] CLKTRCTRL

3.6.21.3 Clock Domain Dependency

CD_C2C has no module wake-up dependency with any other clock domain of the device.

3.6.21.3.1 Static Dependency

Table 3-208 lists the static dependency of the clock domain with respect to other clock domains of the device.

Table 3-208. CD_C2C Static Dependency Association Parameters

Clock Domain Name	Default Setting	Control Bit Field	Access Type
CD_ABE	Disabled	CM_C2C_STATICDEP[3] ABE_STATDEP	Read/Write
CD_IVAHD	Disabled	CM_C2C_STATICDEP[2] IVAHD_STATDEP	Read/Write
CD_L3_1	Disabled	CM_C2C_STATICDEP[5] L3_1_STATDEP	Read/Write
CD_L3_2	Disabled	CM_C2C_STATICDEP[6] L3_2_STATDEP	Read/Write
CD_L3_INIT	Disabled	CM_C2C_STATICDEP[7] L3INIT_STATDEP	Read/Write
CD_L4_CFG	Disabled	CM_C2C_STATICDEP[12] L4CFG_STATDEP	Read/Write
CD_L4_PER	Disabled	CM_C2C_STATICDEP[13] L4PER_STATDEP	Read/Write
CD_EMIF	Enabled	CM_C2C_STATICDEP[4] MEMIF_STATDEP	Read/Write

3.6.21.3.2 Dynamic Dependency

Table 3-209 lists the dynamic dependency of the clock domain with respect to other clock domains of the device.

Table 3-209. CD_C2C Dynamic Dependency Association Parameters

Clock Domain Name	Default Setting	Control Bit Field	Access Type
CD_L3_2	Always enabled	CM_C2C_DYNAMICDEP[6] L3_2_DYNDEP	Read only
CD_EMIF	Always enabled	CM_C2C_DYNAMICDEP[4] MEMIF_DYNDEP	Read only

3.6.21.4 Clock Domain Module Attributes

Table 3-210 lists for each module of the clock domain the clocks received by it and the role (that is, functional or interface clock).

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Table 3-210. CD_C2C Modules Clocks Association

Module	Clock	Clock Type
C2C	C2C_L3X2_ICLK	Interface
	C2C_L3_ICLK	Interface
C2C_FW	C2C_L3_ICLK	Interface
	C2C_L4_ICLK	Interface

Table 3-211 lists the supported wake-up request generation capability for each module of the clock domain.

Table 3-211. CD_C2C Modules Wake-Up Request

Module	Wake-Up Feature
C2C	Master wake-up request
C2C_FW	None

Table 3-212 lists the supported clock-management modes and associated software control bit fields for each module of the power domain.

Table 3-212. CD_C2C Modules Clock-Management Modes and Control

Module	Clock-Management Protocol	Status Bit Field	Role
C2C	Master/Slave	CM_C2C_C2C_CLKCTRL[18] STBYST	Standby status
		CM_C2C_C2C_CLKCTRL[17:16] IDLEST	Idle status
C2C_FW	Slave	CM_C2C_C2C_FW_CLKCTRL [17:16] IDLEST	Idle status

Table 3-213 lists the supported clock-management modes and associated software control bit fields for each module of the power domain.

Table 3-213. CD_C2C Modules Slave Clock-Management Modes and Control

Module	Disabled	Auto	Enabled	Control Bit Field	Access Type
C2C	N/A	Available	N/A	CM_C2C_C2C_CLKCTRL[1:0] MODULEMODE	Read only
C2C_FW	N/A	Available	N/A	CM_C2C_C2C_FW_CLKCTRL[1:0] MODULEMODE	Read only

3.6.22 CD_CAM Clock Domain

This section identifies the modes supported by the clock domain, the associated control and status bits. It also identifies its dependencies with other clock domains of the device.

3.6.22.1 Overview

Figure 3-72 shows the overview of the clock domain.

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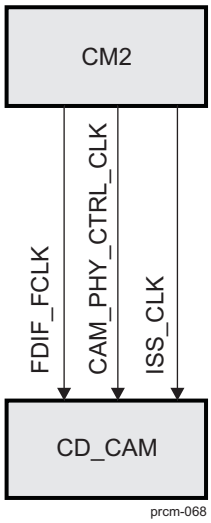
Figure 3-72. CD_CAM Overview



3.6.22.2 Clock Domain Modes

Table 3-214 lists the clock domain modes supported by the clock domain.

Table 3-214. CD_CAM Clock Domain Modes

NO_SLEEP	SW_SLEEP	SW_WKUP	HW_AUTO
Available	Available	Available	Available

Table 3-215 lists the clock domain state transition control and status bits for the clock in this clock domain.

Table 3-215. CD_CAM Control and Status Parameters

Parameter Name	Control/Status Bit Field
CAM_PHY_CTRL_CLK clock status	CM_CAM_CLKSTCTRL[9] CLKACTIVITY_CAM_PHY_CTRL_CLK
FDIF_FCLK clock status	CM_CAM_CLKSTCTRL[10] CLKACTIVITY_FDIF_FCLK
ISS_CLK clock status	CM_CAM_CLKSTCTRL[8] CLKACTIVITY_ISS_CLK
Clock Domain State Transition Control	CM_CAM_CLKSTCTRL[1:0] CLKTRCTRL

3.6.22.3 Clock Domain Dependency

CD_CAM has no module wake-up dependency with any other clock domain of the device.

3.6.22.3.1 Static Dependency

Table 3-216 lists the static dependency of the clock domain with respect to other clock domains of the device.

Table 3-216. CD_CAM Static Dependency Association Parameters

Clock Domain Name	Default Setting	Control Bit Field	Access Type
CD_IVAHD	Disabled	CM_CAM_STATICDEP[2] IVAHD_STATDEP	Read/Write
CD_L3_1	Disabled	CM_CAM_STATICDEP[5] L3_1_STATDEP	Read/Write
CD_L3_2	Always enabled	CM_CAM_STATICDEP[6] L3_2_STATDEP	Read only

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Table 3-216. CD_CAM Static Dependency Association Parameters (continued)

Clock Domain Name	Default Setting	Control Bit Field	Access Type
CD_EMIF	Disabled	CM_CAM_STATICDEP[4] MEMIF_STATDEP	Read/Write

3.6.22.3.2 Dynamic Dependency

Table 3-217 lists the dynamic dependency of the clock domain with respect to other clock domains of the device.

Table 3-217. CD_CAM Dynamic Dependency Association Parameters

Clock Domain Name	Default Setting	Control Bit Field	Access Type
CD_L3_2	Always disabled	CM_CAM_DYNAMICDEP[6] L3_2_DYNDEP	Read only

3.6.22.4 Clock Domain Module Attributes

Table 3-218 lists for each module of the clock domain the clocks received by it and the role (that is, functional or interface clock).

Table 3-218. CD_CAM Modules Clocks Association

Module	Clock	Clock Type
FACE DETECT	FDIF_FCLK	Interface and Functional
ISS	CAM_PHY_CTRL_CLK	Functional
	ISS_CLK	Interface and Functional

Table 3-219 lists the supported wake-up request generation capability for each module of the clock domain.

Table 3-219. CD_CAM Modules Wake-Up Request

Module	Wake-Up Feature
FACE DETECT	None
ISS	None

Table 3-220 lists the supported clock-management modes and associated software control bit fields for each module of the power domain.

Table 3-220. CD_CAM Modules Clock-Management Modes and Control

Module	Clock-Management Protocol	Status Bit Field	Role
FACE DETECT	Master/Slave	CM_CAM_FDIF_CLKCTRL[18] STBYST	Standby status
		CM_CAM_FDIF_CLKCTRL[17:16] IDLEST	Idle status
ISS	Master/Slave	CM_CAM_ISS_CLKCTRL[18] STBYST	Standby status
		CM_CAM_ISS_CLKCTRL[17:16] IDLEST	Idle status

Table 3-221 lists the supported clock-management modes and associated software control bit fields for each module of the power domain.

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Table 3-221. CD_CAM Modules Slave Clock-Management Modes and Control

Module	Disabled	Auto	Enabled	Control Bit Field	Access Type
FACE DETECT	Available	N/A	Available	CM_CAM_FDIF_CLKCTRL[1:0] MODULEMODE	Read/Write
ISS	Available	N/A	Available	CM_CAM_ISS_CLKCTRL[1:0] MODULEMODE	Read/Write

NOTE: To enable and access the ISS module, first the Cortex-M3 module must be enabled and the reset for Cortex-M3 CACHE and MMU must be cleared.

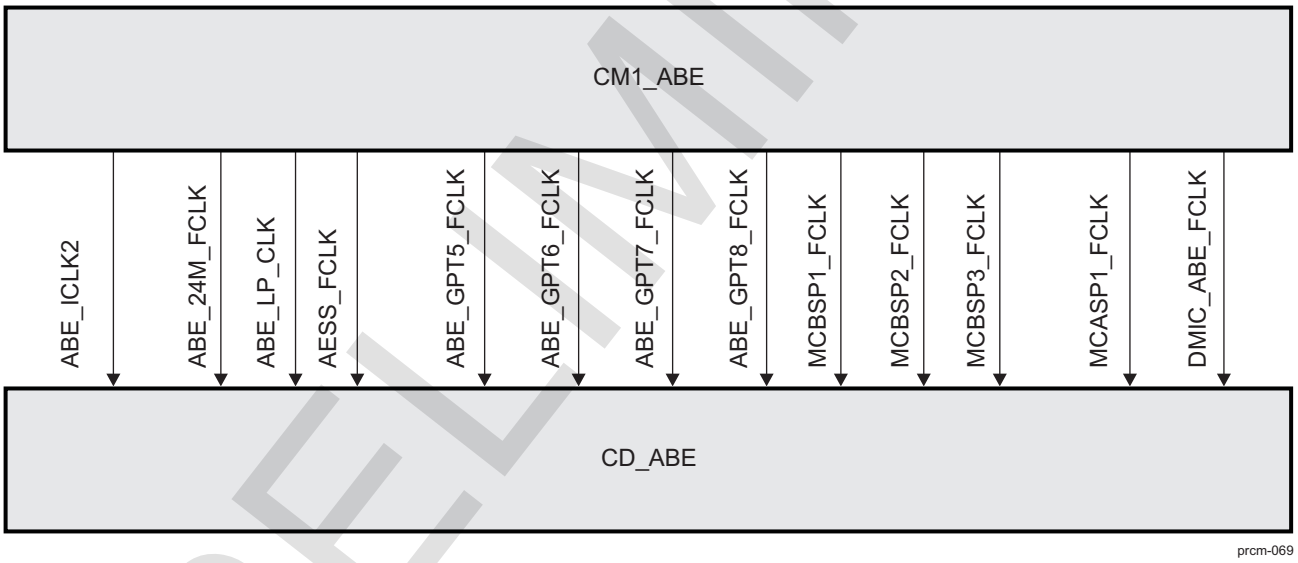
3.6.23 CD_ABE Clock Domain

This section identifies the modes supported by the clock domain, the associated control and status bits. It also identifies its dependencies with other clock domains of the device.

3.6.23.1 Overview

Figure 3-73 shows the overview of the clock domain.

Figure 3-73. CD_ABE Overview



3.6.23.2 Clock Domain Modes

Table 3-222 lists the clock domain modes supported by the clock domain.

Table 3-222. CD_ABE Clock Domain Modes

NO_SLEEP	SW_SLEEP	SW_WKUP	HW_AUTO
Available	Available	Available	Available

Table 3-223 lists the clock domain state transition control and status bits for the clock in this clock domain.

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Table 3-223. CD_ABE Control and Status Parameters

Parameter Name	Control/Status Bit Field
ABE_24M_FCLK clock status	CM1_ABE_CLKSTCTRL[13] CLKACTIVITY_ABE_24M_FCLK
ABE_ALWON_32K_CLK clock status	CM1_ABE_CLKSTCTRL[12] CLKACTIVITY_ABE_ALWON_32K_CLK
ABE_SYSCLK clock status	CM1_ABE_CLKSTCTRL[11] CLKACTIVITY_ABE_SYSCLK
ABE_X2_CLK clock status	CM1_ABE_CLKSTCTRL[8] CLKACTIVITY_ABE_X2_CLK
24M_FCLK clock status	CM1_ABE_CLKSTCTRL[10] CLKACTIVITY_24M_FCLK
ABE_ICLK2 clock status	CM1_ABE_CLKSTCTRL[9] CLKACTIVITY_ABE_ICLK2
Clock Domain State Transition Control	CM1_ABE_CLKSTCTRL[1:0] CLKTRCTRL

3.6.23.3 Clock Domain Dependency

CD_ABE has no static or dynamic dependency with any other clock domain of the device.

3.6.23.3.1 Wake-Up Dependency

Table 3-224 lists the wake-up dependency settings for the modules of this clock clock domain.

Table 3-224. CD_ABE Wake-Up Dependency Association Parameters

Originator Module	Originator Clock Domain	Servicing Clock Domain	Default Setting	Control Bit Field	Access Type
DMIC	CD_ABE	CD_DMA, CD_L3_1, CD_L3_2	Disabled	PM_ABE_DMIC_WKDEP[7] WKUPDEP_DMIC_DMA_SDMA	Read/Write
DMIC	CD_ABE	CD_DSP	Disabled	PM_ABE_DMIC_WKDEP[6] WKUPDEP_DMIC_DMA_DSP	Read/Write
DMIC	CD_ABE	CD_DSP	Disabled	PM_ABE_DMIC_WKDEP[2] WKUPDEP_DMIC_IRQ_DSP	Read/Write
DMIC	CD_ABE	CD_CORTEXA9	Disabled	PM_ABE_DMIC_WKDEP[0] WKUPDEP_DMIC_IRQ_MPU	Read/Write
MCASP1	CD_ABE	CD_DMA, CD_L3_1, CD_L3_2	Disabled	PM_ABE_MCASP_WKDEP[7] WKUPDEP_MCASP1_DMA_SDMA	Read/Write
MCASP1	CD_ABE	CD_DSP	Disabled	PM_ABE_MCASP_WKDEP[6] WKUPDEP_MCASP1_DMA_DSP	Read/Write
MCASP1	CD_ABE	CD_DSP	Disabled	PM_ABE_MCASP_WKDEP[2] WKUPDEP_MCASP1_IRQ_DSP	Read/Write
MCASP1	CD_ABE	CD_CORTEXA9	Disabled	PM_ABE_MCASP_WKDEP[0] WKUPDEP_MCASP1_IRQ_MPU	Read/Write
MCBSP1	CD_ABE	CD_DMA, CD_L3_1, CD_L3_2	Disabled	PM_ABE_MCBSP1_WKDEP[3] WKUPDEP_MCBSP1_SDMA	Read/Write

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Table 3-224. CD_ABE Wake-Up Dependency Association Parameters (continued)

Originator Module	Originator Clock Domain	Servicing Clock Domain	Default Setting	Control Bit Field	Access Type
MCBSP1	CD_ABE	CD_DSP	Disabled	PM_ABE_MCBSP1_WKDEP[2] WKUPDEP_MCBSP1_DSP	Read/Write
MCBSP1	CD_ABE	CD_CORTEXA9	Disabled	PM_ABE_MCBSP1_WKDEP[0] WKUPDEP_MCBSP1_MPU	Read/Write
MCBSP2	CD_ABE	CD_DMA, CD_L3_1, CD_L3_2	Disabled	PM_ABE_MCBSP2_WKDEP[3] WKUPDEP_MCBSP2_SDMA	Read/Write
MCBSP2	CD_ABE	CD_DSP	Disabled	PM_ABE_MCBSP2_WKDEP[2] WKUPDEP_MCBSP2_DSP	Read/Write
MCBSP2	CD_ABE	CD_CORTEXA9	Disabled	PM_ABE_MCBSP2_WKDEP[0] WKUPDEP_MCBSP2_MPU	Read/Write
MCBSP3	CD_ABE	CD_DMA, CD_L3_1, CD_L3_2	Disabled	PM_ABE_MCBSP3_WKDEP[3] WKUPDEP_MCBSP3_SDMA	Read/Write
MCBSP3	CD_ABE	CD_DSP	Disabled	PM_ABE_MCBSP3_WKDEP[2] WKUPDEP_MCBSP3_DSP	Read/Write
MCBSP3	CD_ABE	CD_CORTEXA9	Disabled	PM_ABE_MCBSP3_WKDEP[0] WKUPDEP_MCBSP3_MPU	Read/Write
MCPDM	CD_ABE	CD_DMA, CD_L3_1, CD_L3_2	Disabled	PM_ABE_PDM_WKDEP[7] WKUPDEP_PDM_DMA_SDMA	Read/Write
MCPDM	CD_ABE	CD_DSP	Disabled	PM_ABE_PDM_WKDEP[6] WKUPDEP_PDM_DMA_DSP	Read/Write
MCPDM	CD_ABE	CD_DSP	Disabled	PM_ABE_PDM_WKDEP[2] WKUPDEP_PDM_IRQ_DSP	Read/Write
MCPDM	CD_ABE	CD_CORTEXA9	Disabled	PM_ABE_PDM_WKDEP[0] WKUPDEP_PDM_IRQ_MPU	Read/Write
SLIMBUS1	CD_ABE	CD_DMA, CD_L3_1, CD_L3_2	Disabled	PM_ABE_SLIMBUS_WKDEP[7] WKUPDEP_SLIMBUS1_DMA_SDMA	Read/Write
SLIMBUS1	CD_ABE	CD_DSP	Disabled	PM_ABE_SLIMBUS_WKDEP[6] WKUPDEP_SLIMBUS1_DMA_DSP	Read/Write
SLIMBUS1	CD_ABE	CD_DSP	Disabled	PM_ABE_SLIMBUS_WKDEP[2] WKUPDEP_SLIMBUS1_IRQ_DSP	Read/Write

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Table 3-224. CD_ABE Wake-Up Dependency Association Parameters (continued)

Originator Module	Originator Clock Domain	Servicing Clock Domain	Default Setting	Control Bit Field	Access Type
SLIMBUS1	CD_ABE	CD_CORTEXA9	Disabled	PM_ABE_SLIMBUS_WKDEP[0] WKUPDEP_SLIMBUS1_IRQ_MPU	Read/Write
GPTIMER5	CD_ABE	CD_DSP	Disabled	PM_ABE_GPTIMER5_WKDEP[2] WKUPDEP_TIMER5_DSP	Read/Write
GPTIMER5	CD_ABE	CD_CORTEXA9	Disabled	PM_ABE_GPTIMER5_WKDEP[0] WKUPDEP_TIMER5_MPU	Read/Write
GPTIMER6	CD_ABE	CD_DSP	Disabled	PM_ABE_GPTIMER6_WKDEP[2] WKUPDEP_TIMER6_DSP	Read/Write
GPTIMER6	CD_ABE	CD_CORTEXA9	Disabled	PM_ABE_GPTIMER6_WKDEP[0] WKUPDEP_TIMER6_MPU	Read/Write
GPTIMER7	CD_ABE	CD_DSP	Disabled	PM_ABE_GPTIMER7_WKDEP[2] WKUPDEP_TIMER7_DSP	Read/Write
GPTIMER7	CD_ABE	CD_CORTEXA9	Disabled	PM_ABE_GPTIMER7_WKDEP[0] WKUPDEP_TIMER7_MPU	Read/Write
GPTIMER8	CD_ABE	CD_DSP	Disabled	PM_ABE_GPTIMER8_WKDEP[2] WKUPDEP_TIMER8_DSP	Read/Write
GPTIMER8	CD_ABE	CD_CORTEXA9	Disabled	PM_ABE_GPTIMER8_WKDEP[0] WKUPDEP_TIMER8_MPU	Read/Write
WDTIMER3	CD_ABE	CD_CORTEXA9	Always enabled	PM_ABE_WDTIMER3_WKDEP[0] WKUPDEP_WDT3_MPU	Read only

3.6.23.4 Clock Domain Module Attributes

Table 3-225 lists for each module of the clock domain the clocks received by it and the role (that is, functional or interface clock).

Table 3-225. CD_ABE Modules Clocks Association

Module	Clock	Clock Type
AUDIO ENGINE	AESS_FCLK	Functional
	ABE_ICLK2	Interface
DMIC	DMIC_ABE_FCLK	Functional
	ABE_ICLK2	Interface
L4_ABE interconnect	ABE_ICLK2	Interface
MCASP1	MCASP1_FCLK	Functional
	ABE_ICLK2	Interface and functional
MCBSP1	MCBSP1_FCLK	Functional

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Table 3-225. CD_ABE Modules Clocks Association (continued)

Module	Clock	Clock Type
	ABE_ICLK2	Interface
MCBSP2	MCBSP2_FCLK	Functional
	ABE_ICLK2	Interface
MCBSP3	MCBSP3_FCLK	Functional
	ABE_ICLK2	Interface
MCPDM	ABE_ICLK2	Interface
	PAD_CLKS	Functional
SLIMBUS1	ABE_24M_FCLK	Functional
	24M_FCLK	Functional
	ABE_ICLK2	Interface
	PAD_CLKS	Functional
	SLIMBUS_UCLKS	Functional
GPTIMER5	ABE_GPT5_FCLK	Functional
	ABE_ICLK2	Interface
GPTIMER6	ABE_GPT6_FCLK	Functional
	ABE_ICLK2	Interface
GPTIMER7	ABE_GPT7_FCLK	Functional
	ABE_ICLK2	Interface
GPTIMER8	ABE_GPT8_FCLK	Functional
	ABE_ICLK2	Interface
WDTIMER3	ABE_ALWON_32K_CLK	Functional
	ABE_ICLK2	Interface

Table 3-226 lists the supported wake-up request generation capability for each module of the clock domain.

Table 3-226. CD_ABE Modules Wake-Up Request

Module	Wake-Up Feature
AUDIO ENGINE	None
DMIC	Slave wake-up request (MPU_A9 -IRQ, DSP -IRQ and DMA, sDMA -DMA)
L4_ABE interconnect	None
MCASP1	Slave wake-up request (MPU_A9 -IRQ, DSP -IRQ and DMA, sDMA -DMA)
MCBSP1	Slave wake-up request (MPU_A9 -IRQ, DSP -IRQ and DMA, sDMA -DMA)
MCBSP2	Slave wake-up request (MPU_A9 -IRQ, DSP -IRQ and DMA, sDMA -DMA)
MCBSP3	Slave wake-up request (MPU_A9 -IRQ, DSP -IRQ and DMA, sDMA -DMA)
MCPDM	Slave wake-up request (MPU_A9 -IRQ, DSP -IRQ and DMA, sDMA -DMA)
SLIMBUS1	Slave wake-up request (MPU_A9 -IRQ, DSP -IRQ and DMA, sDMA -DMA)
GPTIMER5	Slave wake-up request (MPU_A9 -IRQ, DSP -IRQ)
GPTIMER6	Slave wake-up request (MPU_A9 -IRQ, DSP -IRQ)
GPTIMER7	Slave wake-up request (MPU_A9 -IRQ, DSP -IRQ)
GPTIMER8	Slave wake-up request (MPU_A9 -IRQ, DSP -IRQ)
WDTIMER3	Slave wake-up request (MPU_A9 -IRQ)

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Table 3-227 lists the supported clock-management modes and associated software control bit fields for each module of the power domain.

Table 3-227. CD_ABE Modules Clock-Management Modes and Control

Module	Clock-Management Protocol	Status Bit Field	Role
AUDIO ENGINE	Slave/Master	CM1_ABE_AESS_CLKCTRL[18] STBYST	Standby status
		CM1_ABE_AESS_CLKCTRL[17:16] IDLEST	Idle status
DMIC	Slave	CM1_ABE_DMIC_CLKCTRL[17:16] IDLEST	Idle status
L4_ABE interconnect	Slave	CM1_ABE_L4ABE_CLKCTRL[17:16] IDLEST	Idle status
MCASP1	Slave	CM1_ABE_MCASP_CLKCTRL[17:16] IDLEST	Idle status
MCBSP1	Slave	CM1_ABE_MCBSP1_CLKCTRL[17:16] IDLEST	Idle status
MCBSP2	Slave	CM1_ABE_MCBSP2_CLKCTRL[17:16] IDLEST	Idle status
MCBSP3	Slave	CM1_ABE_MCBSP3_CLKCTRL[17:16] IDLEST	Idle status
MCPDM	Slave	CM1_ABE_PDM_CLKCTRL[17:16] IDLEST	Idle status
SLIMBUS1	Slave	CM1_ABE_SLIMBUS_CLKCTRL[17:16] IDLEST	Idle status
GPTIMER5	Slave	CM1_ABE_GPTIMER5_CLKCTRL[17:16] IDLEST	Idle status
GPTIMER6	Slave	CM1_ABE_GPTIMER6_CLKCTRL[17:16] IDLEST	Idle status
GPTIMER7	Slave	CM1_ABE_GPTIMER7_CLKCTRL[17:16] IDLEST	Idle status
GPTIMER8	Slave	CM1_ABE_GPTIMER8_CLKCTRL[17:16] IDLEST	Idle status
WDTIMER3	Slave	CM1_ABE_WDTIMER3_CLKCTRL[17:16] IDLEST	Idle status

Table 3-228 lists the supported clock-management modes and associated software control bit fields for each module of the power domain.

Table 3-228. CD_ABE Modules Slave Clock-Management Modes and Control

Module	Disabled	Auto	Enabled	Control Bit Field	Access Type
AUDIO ENGINE	Available	N/A	Available	CM1_ABE_AESS_CLKCTRL[1:0] MODULEMODE	Read/Write
DMIC	Available	N/A	Available	CM1_ABE_DMIC_CLKCTRL[1:0] MODULEMODE	Read/Write
L4_ABE interconnect	N/A	Available	N/A	CM1_ABE_L4ABE_CLKCTRL[1:0] MODULEMODE	Read only
MCASP1	Available	N/A	Available	CM1_ABE_MCASP_CLKCTRL[1:0] MODULEMODE	Read/Write
MCBSP1	Available	N/A	Available	CM1_ABE_MCBSP1_CLKCTRL[1:0] MODULEMODE	Read/Write
MCBSP2	Available	N/A	Available	CM1_ABE_MCBSP2_CLKCTRL[1:0] MODULEMODE	Read/Write

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Table 3-228. CD_ABE Modules Slave Clock-Management Modes and Control (continued)

Module	Disabled	Auto	Enabled	Control Bit Field	Access Type
MCBSP3	Available	N/A	Available	CM1_ABE_MCBSP3_CLKCTRL[1:0] MODULEMODE	Read/Write
MCPDM	Available	N/A	Available	CM1_ABE_PDM_CLKCTRL[1:0] MODULEMODE	Read/Write
SLIMBUS1	Available	N/A	Available	CM1_ABE_SLIMBUS_CLKCTRL[1:0] MODULEMODE	Read/Write
GPTIMER5	Available	N/A	Available	CM1_ABE_GPTIMER5_CLKCTRL[1:0] MODULEMODE	Read/Write
GPTIMER6	Available	N/A	Available	CM1_ABE_GPTIMER6_CLKCTRL[1:0] MODULEMODE	Read/Write
GPTIMER7	Available	N/A	Available	CM1_ABE_GPTIMER7_CLKCTRL[1:0] MODULEMODE	Read/Write
GPTIMER8	Available	N/A	Available	CM1_ABE_GPTIMER8_CLKCTRL[1:0] MODULEMODE	Read/Write
WDTIMER3	Available	N/A	Available	CM1_ABE_WDTIMER3_CLKCTRL[1:0] MODULEMODE	Read/Write

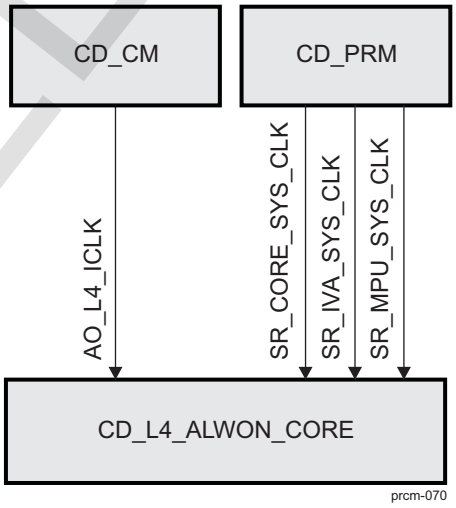
3.6.24 CD_L4_ALWON_CORE Clock Domain

This section identifies the modes supported by the clock domain, the associated control and status bits. It also identifies its dependencies with other clock domains of the device.

3.6.24.1 Overview

Figure 3-74 shows the overview of the clock domain.

Figure 3-74. CD_L4_ALWON_CORE Overview



3.6.24.2 Clock Domain Modes

CD_L4_ALWON_CORE is an always-on clock domain and has no software-controlled clock domain modes management associated.

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3.6.24.3 Clock Domain Dependency

CD_L4_ALWON_CORE has no static or dynamic dependency with any other clock domain of the device.

3.6.24.3.1 Wake-Up Dependency

Table 3-229 lists the wake-up dependency settings for the modules of this clock clock domain.

Table 3-229. CD_L4_ALWON_CORE Wake-Up Dependency Association Parameters

Originator Module	Originator Clock Domain	Servicing Clock Domain	Default Setting	Control Bit Field	Access Type
SR_CORE	CD_L4_ALWON_CORE	CD_CORTEXM3	Disabled	PM_ALWON_SR_CORE_WKDEP[1] WKUPDEP_SR_CORE_MPU_M3	Read/Write
	CD_L4_ALWON_CORE	CD_CORTEXA9	Disabled	PM_ALWON_SR_CORE_WKDEP[0] WKUPDEP_SR_CORE_MPU	Read/Write
SR_IVA	CD_L4_ALWON_CORE	CD_CORTEXM3	Disabled	PM_ALWON_SR_IVA_WKDEP[1] WKUPDEP_SR_IVA_MPU_M3	Read/Write
	CD_L4_ALWON_CORE	CD_CORTEXA9	Disabled	PM_ALWON_SR_IVA_WKDEP[0] WKUPDEP_SR_IVA_MPU	Read/Write
SR_MPU	CD_L4_ALWON_CORE	CD_CORTEXA9	Always enabled	PM_ALWON_SR_MPU_WKDEP[0] WKUPDEP_SR_MPU_MPU	Read only

3.6.24.4 Clock Domain Module Attributes

Table 3-230 lists for each module of the clock domain the clocks received by it and the role (that is, functional or interface clock).

Table 3-230. CD_L4_ALWON_CORE Modules Clocks Association

Module	Clock	Clock Type
SR_CORE	AO_L4_ICLK	Interface
	SR_CORE_SYS_CLK	Functional
SR_IVA	AO_L4_ICLK	Interface
	SR_IVA_SYS_CLK	Functional
SR_MPU	AO_L4_ICLK	Interface
	SR_MPU_SYS_CLK	Functional

Table 3-231 lists the supported wake-up request generation capability for each module of the clock domain.

Table 3-231. CD_L4_ALWON_CORE Modules Wake-Up Request

Module	Wake-Up Feature
SR_CORE	Slave wake-up request (MPU_A9 -IRQ, MPU_M3 -IRQ)
SR_IVA	Slave wake-up request (MPU_A9 -IRQ, MPU_M3 -IRQ)
SR_MPU	Slave wake-up request (MPU_A9 -IRQ)

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Table 3-232 lists the supported clock-management modes and associated software control bit fields for each module of the power domain.

Table 3-232. CD_L4_ALWON_CORE Modules Clock-Management Modes and Control

Module	Clock-Management Protocol	Status Bit Field	Role
SR_CORE	Slave	CM_ALWON_SR_CORE_CLKCTRL[17:16] IDLEST	Idle status
SR_IVA	Slave	CM_ALWON_SR_IVA_CLKCTRL[17:16] IDLEST	Idle status
SR_MPU	Slave	CM_ALWON_SR_MPU_CLKCTRL[17:16] IDLEST	Idle status

Table 3-233 lists the supported clock-management modes and associated software control bit fields for each module of the power domain.

Table 3-233. CD_L4_ALWON_CORE Modules Slave Clock-Management Modes and Control

Module	Disabled	Auto	Enabled	Control Bit Field	Access Type
SR_CORE	Available	N/A	Available	CM_ALWON_SR_CORE_CLKCTRL[1:0] MODULEMODE	Read/Write
SR_IVA	Available	N/A	Available	CM_ALWON_SR_IVA_CLKCTRL[1:0] MODULEMODE	Read/Write
SR_MPU	Available	N/A	Available	CM_ALWON_SR_MPU_CLKCTRL[1:0] MODULEMODE	Read/Write

3.7 Power Management Functional Description

This section highlights the functional concepts of power domain level power management in the device.

The following power domains support the DPS with switching times of less than 5 µs.

- PD_CORE
- PD_DSP
- PD_MPU

3.7.1 PD_WKUP Description

PD_WKUP contains the following reset domains:

- WKUP_PWRON_RST
- WKUP_RST
- WKUP_SYS_PWRON_RST

PD_WKUP contains CD_WKUP clock domain.

Table 3-234 lists the logic retention capability for each module of the power domain.

Table 3-234. PD_WKUP Modules Power Attributes

Module	Logic Retention	DFF Context Status	RFF Context Status
SYSCTRL_PADCONF_WKUP	No	None	None
BANDGAP	No	None	None
SYSCTRL_GENERAL_WKUP	No	None	None
GPIO1	No	RM_WKUP_GPIO1_CONTEXT[0] LOSTCONTEXT_DFF	None
KEYBOARD	No	RM_WKUP_KEYBOARD_CONTEXT[0] LOSTCONTEXT_DFF	None

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Table 3-234. PD_WKUP Modules Power Attributes (continued)

Module	Logic Retention	DFF Context Status	RFF Context Status
PRM	No	None	None
SAR_RAM	No	RM_WKUP_SARRAM_CONTEXT[0] LOSTCONTEXT_DFF	None
SCRM	No	None	None
32KTIMER	No	RM_WKUP_32KTIMER_CONTEXT[0] LOSTCONTEXT_DFF	None
GPTIMER1	No	RM_WKUP_GPTIMER1_CONTEXT[0] LOSTCONTEXT_DFF	None
WDTIMER2	No	RM_WKUP_WDTIMER2_CONTEXT[0] LOSTCONTEXT_DFF	None
L4_WKUP interconnect	No	RM_WKUP_L4WKUP_CONTEXT[0] LOSTCONTEXT_DFF	None

3.7.1.1 Power Domain Modes

The PD_WKUP power domain is an always-on power domain and does not switch to RETENTION state. There is no logic power state control or status bit field for this power domain.

The PD_WKUP power domain has no memory banks.

3.7.2 PD_DSP Description

PD_DSP contains the following reset domains:

- DSP_RST
- DSP_PWRON_RST
- DSP_RET_RST
- DSP_SYS_RST

PD_DSP contains the CD_DSP clock domain.

Table 3-235 lists the logic retention capability for each module of the power domain.

Table 3-235. PD_DSP Modules Power Attributes

Module	Logic Retention	DFF Context Status	RFF Context Status
DSP	Partial	RM_DSP_DSP_CONTEXT[0] LOSTCONTEXT_DFF	RM_DSP_DSP_CONTEXT[1] LOSTCONTEXT_RFF

3.7.2.1 Power Domain Modes

This section highlights the various power modes supported by the logic and memory areas of the power domain. It also identifies the software control and status bit fields associated. See Section 3.1.1.2.1, for a functional description of the power-management architecture of a generic power domain.

3.7.2.1.1 Logic and Memory Area Power Modes

Table 3-236 lists the power modes supported by the logic area of the power domain.

Table 3-236. PD_DSP Logic Area Power Modes

Off	Retention-OSWR	Retention-CSWR	On-Inactive	On-Active
Available	Available	Available	Available	Available

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Table 3-237 presents the power modes supported by the memory area of the power domain. A memory area power mode is identified with respect to a power state of the power domain. The Logic On, Logic Retention, and Logic Off columns identify the power states of the power domain. The values in these columns identify the supported power state of the memory area (identified in the Memory Bank column) or the module memory inside the memory area (identified in the Module - Memory column). The RTA Feature column identifies whether the memory supports the RTA feature.

Table 3-237. PD_DSP Memory Area Power Modes

Memory Bank	Module - Memory	Logic On	Logic Retention	Logic Off	RTA Feature
DSP_EDMA		ON	RETENTION	OFF	
	DSP - DSP_EDMA	always_on	always_retention		always_enabled
DSP_L1		ON	OFF, RETENTION	OFF	
	DSP - DSP_L1	always_on	software_control		None
DSP_L2		ON	OFF, RETENTION	OFF	
	DSP - DSP_L2	always_on	software_control		always_enabled

3.7.2.1.2 Logic and Memory Area Power Modes Control and Status

Table 3-238 lists the power modes controls for the power domain.

Table 3-238. PD_DSP Power Modes Control Parameters

Parameter Name	Memory Bank	Control Bit Field	Access Type
Memory Area - State Control (Logic in Retention state)	DSP_L2	PM_DSP_PWRSTCTRL[9] DSP_L2_RETSTATE	Read/Write
Memory Area - State Control (Logic in Retention state)	DSP_L1	PM_DSP_PWRSTCTRL[8] DSP_L1_RETSTATE	Read/Write
Power Domain - Low Power State Change Control		PM_DSP_PWRSTCTRL[4] LOWPOWERSTATECHANGE	Read/Write
Memory Area - State Control (Logic in On state)	DSP_EDMA	PM_DSP_PWRSTCTRL[21:20] DSP_EDMA_ONSTATE	Read only
Logic Area - Retention State Control		PM_DSP_PWRSTCTRL[2] LOGICRETSTATE	Read/Write
Memory Area - State Control (Logic in On state)	DSP_L2	PM_DSP_PWRSTCTRL[19:18] DSP_L2_ONSTATE	Read only
Memory Area - State Control (Logic in On state)	DSP_L1	PM_DSP_PWRSTCTRL[17:16] DSP_L1_ONSTATE	Read only
Memory Area - State Control (Logic in Retention state)	DSP_EDMA	PM_DSP_PWRSTCTRL[10] DSP_EDMA_RETSTATE	Read only
Power Domain - State Transition Control		PM_DSP_PWRSTCTRL[1:0] POWERSTATE	Read/Write

Table 3-239 lists the power modes status for the power domain.

Table 3-239. PD_DSP Power Modes Status Parameters

Parameter Name	Memory Bank	Status Bit Field
Power Domain - Last Power State Entered Status		PM_DSP_PWRSTST[25:24] LASTPOWERSTATEENTERED
Memory Area - State Status	DSP_EDMA	PM_DSP_PWRSTST[9:8] DSP_EDMA_STATEST
Memory Area - State Status	DSP_L2	PM_DSP_PWRSTST[7:6] DSP_L2_STATEST
Memory Area - State Status	DSP_L1	PM_DSP_PWRSTST[5:4] DSP_L1_STATEST
Power Domain - State Transition Status		PM_DSP_PWRSTST[20] INTRANSITION
Logic Area - State Status		PM_DSP_PWRSTST[2] LOGICSTATEST

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Table 3-239. PD_DSP Power Modes Status Parameters (continued)

Parameter Name	Memory Bank	Status Bit Field
Power Domain - State Status		PM_DSP_PWRSTST[1:0] POWERSTATEST

3.7.3 PD_STD_EFUSE Description

PD_STD_EFUSE contains the STD_EFUSE_PWRON_RST reset domain.

PD_STD_EFUSE contains the CD_STD_EFUSE clock domain.

Table 3-240 lists the logic retention capability for each module of the power domain.

Table 3-240. PD_STD_EFUSE Modules Power Attributes

Module	Logic Retention	DFF Context Status	RFF Context Status
STD_EFUSE	No	None	None

3.7.3.1 Power Domain Modes

The PD_STD_EFUSE power domain is hardware-controlled by the PRCM module and has no software control associated. It is switched to ON power state when the device is powered on and switched to OFF power state after the power-up sequence of the device.

The PD_STD_EFUSE power domain has no memory banks.

3.7.4 PD_MPU Description

PD_MPU contains the following reset domains:

- CORTEXA9_PWRON_RST
- CORTEXA9_RST

PD_MPU contains the CD_CORTEXA9 clock domain.

Table 3-241 lists the logic retention capability for each module of the power domain.

Table 3-241. PD_MPU Modules Power Attributes

Module	Logic Retention	DFF Context Status	RFF Context Status
CORTEXA9	No	RM_MPU_MPU_CONTEXT[0] LOSTCONTEXT_DFF	None

3.7.4.1 Power Domain Modes

This section highlights the various power modes supported by the logic and memory areas of the power domain. It also identifies the software control and status bit fields associated. See Section 3.1.1.2.1 for a functional description of the power-management architecture of a generic power domain.

3.7.4.1.1 Logic and Memory Area Power Modes

Table 3-242 lists the power modes supported by the logic area of the power domain.

Table 3-242. PD_MPU Logic Area Power Modes

Off	Retention-OSWR	Retention-CSWR	On-Inactive	On-Active
Available	Available	Available	Available	Available

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Table 3-243 presents the power modes supported by the memory area of the power domain. A memory area power mode is identified with respect to a power state of the power domain. The Logic On, Logic Retention, and Logic Off columns identify the power states of the power domain. The values in these columns identify the supported power state of the memory area (identified in the Memory Bank column) or the module memory inside the memory area (identified in the Module - Memory column). The RTA Feature column identifies whether the memory supports the RTA feature.

Table 3-243. PD_MPU Memory Area Power Modes

Memory Bank	Module - Memory	Logic On	Logic Retention	Logic Off	RTA Feature
MPU_L1		ON	OFF, RETENTION	OFF	
	CORTEXA9 - MPU_L1	always_on	software_control		None
MPU_L2		ON	OFF, RETENTION	OFF	
	CORTEXA9 - MPU_L2	always_on	software_control		always_enabled
MPU_RAM		ON	RETENTION	OFF	
	CORTEXA9 - MPU_RAM	always_on	always_retention		always_enabled

3.7.4.1.2 Logic and Memory Area Power Modes Control and Status

Table 3-244 lists the power modes controls for the power domain.

Table 3-244. PD_MPU Power Modes Control Parameters

Parameter Name	Memory Bank	Control Bit Field	Access Type
Memory Area - State Control (Logic in Retention state)	MPU_L2	PM_MPU_PWRSTCTRL[9] MPU_L2_RETSTATE	Read/Write
Memory Area - State Control (Logic in Retention state)	MPU_L1	PM_MPU_PWRSTCTRL[8] MPU_L1_RETSTATE	Read/Write
Power Domain - Low Power State Change Control		PM_MPU_PWRSTCTRL[4] LOWPOWERSTATECHANGE	Read only
Memory Area - State Control (Logic in On state)	MPU_RAM	PM_MPU_PWRSTCTRL[21:20] MPU_RAM_ONSTATE	Read only
Logic Area - Retention State Control		PM_MPU_PWRSTCTRL[2] LOGICRETSTATE	Read/Write
Memory Area - State Control (Logic in On state)	MPU_L2	PM_MPU_PWRSTCTRL[19:18] MPU_L2_ONSTATE	Read only
Memory Area - State Control (Logic in On state)	MPU_L1	PM_MPU_PWRSTCTRL[17:16] MPU_L1_ONSTATE	Read only
Memory Area - State Control (Logic in Retention state)	MPU_RAM	PM_MPU_PWRSTCTRL[10] MPU_RAM_RETSTATE	Read only
Power Domain - State Transition Control		PM_MPU_PWRSTCTRL[1:0] POWERSTATE	Read/Write

Table 3-245 lists the power modes status for the power domain.

Table 3-245. PD_MPU Power Modes Status Parameters

Parameter Name	Memory Bank	Status Bit Field
Power Domain - Last Power State Entered Status		PM_MPU_PWRSTST[25:24] LASTPOWERSTATEENTERED
Memory Area - State Status	MPU_RAM	PM_MPU_PWRSTST[9:8] MPU_RAM_STATEST
Memory Area - State Status	MPU_L2	PM_MPU_PWRSTST[7:6] MPU_L2_STATEST
Memory Area - State Status	MPU_L1	PM_MPU_PWRSTST[5:4] MPU_L1_STATEST

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Table 3-245. PD_MPU Power Modes Status Parameters (continued)

Parameter Name	Memory Bank	Status Bit Field
Power Domain - State Transition Status		PM_MPU_PWRSTST[20] INTRANSITION
Logic Area - State Status		PM_MPU_PWRSTST[2] LOGICSTATEST
Power Domain - State Status		PM_MPU_PWRSTST[1:0] POWERSTATEST

3.7.5 PD_L4_PER Description

PD_L4_PER contains the following reset domains:

- L4_PER_PWRON_RET_RST
- L4_PER_RET_RST
- L4_PER_RST

PD_L4_PER contains the CD_L4_PER clock domain.

•

Table 3-246 lists the logic retention capability for each module of the power domain.

Table 3-246. PD_L4_PER Modules Power Attributes

Module	Logic Retention	DFF Context Status	RFF Context Status
GPTIMER10	No	RM_L4PER_GPTIMER10_CONTEXT[0] LOSTCONTEXT_DFF	None
GPTIMER11	No	RM_L4PER_GPTIMER11_CONTEXT[0] LOSTCONTEXT_DFF	None
GPTIMER2	No	RM_L4PER_GPTIMER2_CONTEXT[0] LOSTCONTEXT_DFF	None
GPTIMER3	No	RM_L4PER_GPTIMER3_CONTEXT[0] LOSTCONTEXT_DFF	None
GPTIMER4	No	RM_L4PER_GPTIMER4_CONTEXT[0] LOSTCONTEXT_DFF	None
GPTIMER9	No	RM_L4PER_GPTIMER9_CONTEXT[0] LOSTCONTEXT_DFF	None
ELM	No	RM_L4PER_ELM_CONTEXT[0] LOSTCONTEXT_DFF	None
GPIO2	Full	None	RM_L4PER_GPIO2_CONTEXT[1] LOSTCONTEXT_RFF
GPIO3	Full	None	RM_L4PER_GPIO3_CONTEXT[1] LOSTCONTEXT_RFF
GPIO4	Full	None	RM_L4PER_GPIO4_CONTEXT[1] LOSTCONTEXT_RFF
GPIO5	Full	None	RM_L4PER_GPIO5_CONTEXT[1] LOSTCONTEXT_RFF
GPIO6	Full	None	RM_L4PER_GPIO6_CONTEXT[1] LOSTCONTEXT_RFF
HDQ	No	RM_L4PER_HDQ1W_CONTEXT[0] LOSTCONTEXT_DFF	None
I2C1	Full	None	RM_L4PER_I2C1_CONTEXT[1] LOSTCONTEXT_RFF
I2C2	No	RM_L4PER_I2C2_CONTEXT[0] LOSTCONTEXT_DFF	None
I2C3	No	RM_L4PER_I2C3_CONTEXT[0] LOSTCONTEXT_DFF	None
I2C4	No	RM_L4PER_I2C4_CONTEXT[0] LOSTCONTEXT_DFF	None

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Table 3-246. PD_L4_PER Modules Power Attributes (continued)

Module	Logic Retention	DFF Context Status	RFF Context Status
L4_PER interconnect	Partial	RM_L4PER_L4_PER_CONTEXT[0] LOSTCONTEXT_DFF	RM_L4PER_L4_PER_CONTEXT[1] LOSTCONTEXT_RFF
MCBSP4	No	RM_L4PER_MCBSP4_CONTEXT[0] LOSTCONTEXT_DFF	None
MCSPI1	No	RM_L4PER_MCSPI1_CONTEXT[0] LOSTCONTEXT_DFF	None
MCSPI2	No	RM_L4PER_MCSPI2_CONTEXT[0] LOSTCONTEXT_DFF	None
MCSPI3	No	RM_L4PER_MCSPI3_CONTEXT[0] LOSTCONTEXT_DFF	None
MCSPI4	No	RM_L4PER_MCSPI4_CONTEXT[0] LOSTCONTEXT_DFF	None
HSMMC3	No	RM_L4PER_MMCSD3_CONTEXT[0] LOSTCONTEXT_DFF	None
HSMMC4	No	RM_L4PER_MMCSD4_CONTEXT[0] LOSTCONTEXT_DFF	None
HSMMC5	No	RM_L4PER_MMCSD5_CONTEXT[0] LOSTCONTEXT_DFF	None
SLIMBUS2	No	RM_L4PER_SLIMBUS2_CONTEXT[0] LOSTCONTEXT_DFF	None
UART1	Full	None	RM_L4PER_UART1_CONTEXT[1] LOSTCONTEXT_RFF
UART2	Full	None	RM_L4PER_UART2_CONTEXT[1] LOSTCONTEXT_RFF
UART3	Full	None	RM_L4PER_UART3_CONTEXT[1] LOSTCONTEXT_RFF
UART4	Full	None	RM_L4PER_UART4_CONTEXT[1] LOSTCONTEXT_RFF

3.7.5.1 Power Domain Modes

This section highlights the various power modes supported by the logic and memory areas of the power domain. It also identifies the software control and status bit fields associated. See Section 3.1.1.2.1 for a functional description of the power-management architecture of a generic power domain.

3.7.5.1.1 Logic and Memory Area Power Modes

Table 3-247 lists the power modes supported by the logic area of the power domain.

Table 3-247. PD_L4_PER Logic Area Power Modes

Off	Retention-OSWR	Retention-CSWR	On-Inactive	On-Active
Available	Available	Available	Available	Available

Table 3-248 presents the power modes supported by the memory area of the power domain. A memory area power mode is identified with respect to a power state of the power domain. The Logic On, Logic Retention, and Logic Off columns identify the power states of the power domain. The values in these columns identify the supported power state of the memory area (identified in the Memory Bank column) or the module memory inside the memory area (identified in the Module - Memory column). The RTA Feature column identifies whether the memory supports the RTA feature.

Table 3-248. PD_L4_PER Memory Area Power Modes

Memory Bank	Module - Memory	Logic On	Logic Retention	Logic Off	RTA Feature
NONRETAINED_BANK		ON	OFF	OFF	

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Table 3-248. PD_L4_PER Memory Area Power Modes (continued)

Memory Bank	Module - Memory	Logic On	Logic Retention	Logic Off	RTA Feature
	MCBSP4 - MCBSP_BANK	always_on	always_off		None
	HSMMC3 - MMCHSSRAM	always_on	always_off		None
	SLIMBUS2 - SLIMBUS_BANK	always_on	always_off		None
RETAINED_BANK		ON	RETENTION	OFF	
	UART1 - UART_MEM	always_on	always_retention		None

3.7.5.1.2 Logic and Memory Area Power Modes Control and Status

Table 3-249 lists the power modes controls for the power domain.

Table 3-249. PD_L4_PER Power Modes Control Parameters

Parameter Name	Memory Bank	Control Bit Field	Access Type
Memory Area - State Control (Logic in Retention state)	NONRETAINED_BANK	PM_L4PER_PWRSTCTRL[9] NONRETAINED_BANK_RETSTATE	Read only
Memory Area - State Control (Logic in Retention state)	RETAINED_BANK	PM_L4PER_PWRSTCTRL[8] RETAINED_BANK_RETSTATE	Read only
Power Domain - Low Power State Change Control		PM_L4PER_PWRSTCTRL[4] LOWPOWERSTATECHANGE	Read/Write
Logic Area - Retention State Control		PM_L4PER_PWRSTCTRL[2] LOGICRETSTATE	Read/Write
Memory Area - State Control (Logic in On state)	NONRETAINED_BANK	PM_L4PER_PWRSTCTRL[19:18] NONRETAINED_BANK_ONSTATE	Read only
Memory Area - State Control (Logic in On state)	RETAINED_BANK	PM_L4PER_PWRSTCTRL[17:16] RETAINED_BANK_ONSTATE	Read only
Power Domain - State Transition Control		PM_L4PER_PWRSTCTRL[1:0] POWERSTATE	Read/Write

Table 3-250 lists the power modes status for the power domain.

Table 3-250. PD_L4_PER Power Modes Status Parameters

Parameter Name	Memory Bank	Status Bit Field
Power Domain - Last Power State Entered Status		PM_L4PER_PWRSTST[25:24] LASTPOWERSTATEENTERED
Memory Area - State Status	NONRETAINED_BANK	PM_L4PER_PWRSTST[7:6] NONRETAINED_BANK_STATEST
Memory Area - State Status	RETAINED_BANK	PM_L4PER_PWRSTST[5:4] RETAINED_BANK_STATEST
Power Domain - State Transition Status		PM_L4PER_PWRSTST[20] INTRANSITION
Logic Area - State Status		PM_L4PER_PWRSTST[2] LOGICSTATEST
Power Domain - State Status		PM_L4PER_PWRSTST[1:0] POWERSTATEST

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3.7.6 PD_L3_INIT Description

PD_L3_INIT contains the following reset domains:

- DPLL_L3_INIT_PWRON_RET_RST
- L3_INIT_PWRON_RST
- L3_INIT_RET_RST
- L3_INIT_RST

PD_L3_INIT contains the CD_L3_INIT clock domain.

Table 3-251 lists the logic retention capability for each module of the power domain.

Table 3-251. PD_L3_INIT Modules Power Attributes

Module	Logic Retention	DFF Context Status	RFF Context Status
CM1_USB	No	None	None
DPLL_USB	Full	None	None
HSI	Full	None	RM_L3INIT_HSI_CONTEXT[1] LOSTCONTEXT_RFF
HSMMC1	Full	None	RM_L3INIT_MMC1_CONTEXT [1] LOSTCONTEXT_RFF
HSMMC2	Full	None	RM_L3INIT_MMC2_CONTEXT [1] LOSTCONTEXT_RFF
USBPHY	No	RM_L3INIT_USBPHY_CONTEXT[0] LOSTCONTEXT_DFF	None
FSUSB	Full	None	RM_L3INIT_USB_HOST_FS_CONTEXT[1] LOSTCONTEXT_RFF
HSUSBHOST	Full	None	RM_L3INIT_USB_HOST_CONTEXT[1] LOSTCONTEXT_RFF
HSUSBOTG	Full	None	RM_L3INIT_USB_OTG_CONTEXT[1] LOSTCONTEXT_RFF
HSUSBTLL	Full	None	RM_L3INIT_HSUSBTLL_CONTEXT[1] LOSTCONTEXT_RFF

3.7.6.1 Power Domain Modes

This section highlights the various power modes supported by the logic and memory areas of the power domain. It also identifies the software control and status bit fields associated. See Section 3.1.1.2.1 for a functional description of the power-management architecture of a generic power domain.

3.7.6.1.1 Logic and Memory Area Power Modes

Table 3-252 lists the power modes supported by the logic area of the power domain.

Table 3-252. PD_L3_INIT Logic Area Power Modes

Off	Retention-OSWR	Retention-CSWR	On-Inactive	On-Active
Available	Available	Available	Available	Available

Table 3-253 presents the power modes supported by the memory area of the power domain. A memory area power mode is identified with respect to a power state of the power domain. The Logic On, Logic Retention, and Logic Off columns identify the power states of the power domain. The values in these columns identify the supported power state of the memory area (identified in the Memory Bank column) or the module memory inside the memory area (identified in the Module - Memory column). The RTA Feature column identifies whether the memory supports the RTA feature.

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Table 3-253. PD_L3_INIT Memory Area Power Modes

Memory Bank	Module - Memory	Logic On	Logic Retention	Logic Off	RTA Feature
L3INIT_BANK1		ON	OFF	OFF	
	HSI - HSI_DMAFIFO	always_on	always_off		None
	HSMMC1 - HSMMCSRAM	always_on	always_off		None
	HSUSBOTG - USBMEM	always_on	always_off		always_enabled

3.7.6.1.2 Logic and Memory Area Power Modes Control and Status

Table 3-254 lists the power modes controls for the power domain.

Table 3-254. PD_L3_INIT Power Modes Control Parameters

Parameter Name	Memory Bank	Control Bit Field	Access Type
Memory Area - State Control (Logic in Retention state)	L3INIT_BANK1	PM_L3INIT_PWRSTCTRL[8] L3INIT_BANK1_RETSTATE	Read only
Power Domain - Low Power State Change Control		PM_L3INIT_PWRSTCTRL[4] LOWPOWERSTATECHANGE	Read/Write
Logic Area - Retention State Control		PM_L3INIT_PWRSTCTRL[2] LOGICRETSTATE	Read/Write
Memory Area - State Control (Logic in On state)	L3INIT_BANK1	PM_L3INIT_PWRSTCTRL[17:16] L3INIT_BANK1_ONSTATE	Read only
Power Domain - State Transition Control		PM_L3INIT_PWRSTCTRL[1:0] POWERSTATE	Read/Write

Table 3-255 lists the power modes status for the power domain.

Table 3-255. PD_L3_INIT Power Modes Status Parameters

Parameter Name	Memory Bank	Status Bit Field
Power Domain - Last Power State Entered Status		PM_L3INIT_PWRSTST[25:24] LASTPOWERSTATEENTERED
Memory Area - State Status	L3INIT_BANK1	PM_L3INIT_PWRSTST[5:4] L3INIT_BANK1_STATEST
Power Domain - State Transition Status		PM_L3INIT_PWRSTST[20] INTRANSITION
Logic Area - State Status		PM_L3INIT_PWRSTST[2] LOGICSTATEST
Power Domain - State Status		PM_L3INIT_PWRSTST[1:0] POWERSTATEST

3.7.7 PD_IVAHD Description

PD_IVAHD contains the following reset domains:

- IVAHD_PWRON_RST
- IVAHD_RST
- IVAHD_SEQ1_RST
- IVAHD_SEQ2_RST

PD_IVAHD contains the CD_IVAHD clock domain.

Table 3-256 lists the logic retention capability for each module of the power domain.

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Table 3-256. PD_IVAHD Modules Power Attributes

Module	Logic Retention	DFF Context Status	RFF Context Status
IVAHD	No	RM_IVAHD_IVAHD_CONTEXT[0] LOSTCONTEXT_DFF	None
SL2	No	RM_IVAHD_SL2_CONTEXT[0] LOSTCONTEXT_DFF	None

3.7.7.1 Power Domain Modes

This section highlights the various power modes supported by the logic and memory areas of the power domain. It also identifies the software control and status bit fields associated. See Section 3.1.1.2.1 for a functional description of the power-management architecture of a generic power domain.

3.7.7.1.1 Logic and Memory Area Power Modes

Table 3-257 lists the power modes supported by the logic area of the power domain.

Table 3-257. PD_IVAHD Logic Area Power Modes

Off	Retention-OSWR	Retention-CSWR	On-Inactive	On-Active
Available	Available	Not available	Available	Available

Table 3-258 presents the power modes supported by the memory area of the power domain. A memory area power mode is identified with respect to a power state of the power domain. The Logic On, Logic Retention, and Logic Off columns identify the power states of the power domain. The values in these columns identify the supported power state of the memory area (identified in the Memory Bank column) or the module memory inside the memory area (identified in the Module - Memory column). The RTA Feature column identifies whether the memory supports the RTA feature.

Table 3-258. PD_IVAHD Memory Area Power Modes

Memory Bank	Module - Memory	Logic On	Logic Retention	Logic Off	RTA Feature
HWA_MEM		ON	OFF	OFF	
	IVAHD - HWA_MEM	always_on	always_off		always_enabled
SL2_MEM		ON	OFF, RETENTION	OFF	
	SL2 - SL2MEM	always_on	software_control		always_enabled
TCM1_MEM		ON	OFF, RETENTION	OFF	
	IVAHD - TCM_1	always_on	software_control		always_enabled
TCM2_MEM		ON	OFF, RETENTION	OFF	
	IVAHD - TCM_2	always_on	software_control		always_enabled

3.7.7.1.2 Logic and Memory Area Power Modes Control and Status

Table 3-259 lists the power modes controls for the power domain.

Table 3-259. PD_IVAHD Power Modes Control Parameters

Parameter Name	Memory Bank	Control Bit Field	Access Type
Memory Area - State Control (Logic in Retention state)	SL2_MEM	PM_IVAHD_PWRSTCTRL[9] SL2_MEM_RETSTATE	Read/Write
Memory Area - State Control (Logic in Retention state)	HWA_MEM	PM_IVAHD_PWRSTCTRL[8] HWA_MEM_RETSTATE	Read only
Power Domain - Low Power State Change Control		PM_IVAHD_PWRSTCTRL[4] LOWPOWERSTATECHANGE	Read/Write
Memory Area - State Control (Logic in On state)	TCM2_MEM	PM_IVAHD_PWRSTCTRL[23:22] TCM2_MEM_ONSTATE	Read only

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Table 3-259. PD_IVAHD Power Modes Control Parameters (continued)

Parameter Name	Memory Bank	Control Bit Field	Access Type
Memory Area - State Control (Logic in On state)	TCM1_MEM	PM_IVAHD_PWRSTCTRL[21:20] TCM1_MEM_ONSTATE	Read only
Logic Area - Retention State Control		PM_IVAHD_PWRSTCTRL[2] LOGICRETSTATE	Read only
Memory Area - State Control (Logic in On state)	SL2_MEM	PM_IVAHD_PWRSTCTRL[19:18] SL2_MEM_ONSTATE	Read only
Memory Area - State Control (Logic in On state)	HWA_MEM	PM_IVAHD_PWRSTCTRL[17:16] HWA_MEM_ONSTATE	Read only
Memory Area - State Control (Logic in Retention state)	TCM2_MEM	PM_IVAHD_PWRSTCTRL[11] TCM2_MEM_RETSTATE	Read/Write
Memory Area - State Control (Logic in Retention state)	TCM1_MEM	PM_IVAHD_PWRSTCTRL[10] TCM1_MEM_RETSTATE	Read/Write
Power Domain - State Transition Control		PM_IVAHD_PWRSTCTRL[1:0] POWERSTATE	Read/Write

Table 3-260 lists the power modes status for the power domain.

Table 3-260. PD_IVAHD Power Modes Status Parameters

Parameter Name	Memory Bank	Status Bit Field
Power Domain - Last Power State Entered Status		PM_IVAHD_PWRSTST[25:24] LASTPOWERSTATEENTERED
Memory Area - State Status	TCM1_MEM	PM_IVAHD_PWRSTST[9:8] TCM1_MEM_STATEST
Memory Area - State Status	SL2_MEM	PM_IVAHD_PWRSTST[7:6] SL2_MEM_STATEST
Memory Area - State Status	HWA_MEM	PM_IVAHD_PWRSTST[5:4] HWA_MEM_STATEST
Power Domain - State Transition Status		PM_IVAHD_PWRSTST[20] INTRANSITION
Logic Area - State Status		PM_IVAHD_PWRSTST[2] LOGICSTATEST
Memory Area - State Status	TCM2_MEM	PM_IVAHD_PWRSTST[11:10] TCM2_MEM_STATEST
Power Domain - State Status		PM_IVAHD_PWRSTST[1:0] POWERSTATEST

3.7.8 PD_SGX Description

PD_SGX contains the SGX_RST reset domain.

PD_SGX contains the CD_SGX clock domain.

Table 3-261 lists the logic retention capability for each module of the power domain.

Table 3-261. PD_SGX Modules Power Attributes

Module	Logic Retention	DFF Context Status	RFF Context Status
SGX	No	RM_SGX_SGX_CONTEXT[0] LOSTCONTEXT_DFF	None

3.7.8.1 Power Domain Modes

This section highlights the various power modes supported by the logic and memory areas of the power domain. It also identifies the software control and status bit fields associated. See Section 3.1.1.2.1 for a functional description of the power-management architecture of a generic power domain.

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3.7.8.1.1 Logic and Memory Area Power Modes

Table 3-262 lists the power modes supported by the logic area of the power domain.

Table 3-262. PD_SGX Logic Area Power Modes

Off	Retention-OSWR	Retention-CSWR	On-Inactive	On-Active
Available	Not available	Not available	Available	Available

Table 3-263 presents the power modes supported by the memory area of the power domain. A memory area power mode is identified with respect to a power state of the power domain. The Logic On, Logic Retention, and Logic Off columns identify the power states of the power domain. The values in these columns identify the supported power state of the memory area (identified in the Memory Bank column) or the module memory inside the memory area (identified in the Module - Memory column). The RTA Feature column identifies whether the memory supports the RTA feature.

Table 3-263. PD_SGX Memory Area Power Modes

Memory Bank	Module - Memory	Logic On	Logic Retention	Logic Off	RTA Feature
	SGX - SGX_MEM	always_on	always_off		always_enabled

3.7.8.1.2 Logic and Memory Area Power Modes Control and Status

Table 3-264 lists the power modes controls for the power domain.

Table 3-264. PD_SGX Power Modes Control Parameters

Parameter Name	Memory Bank	Control Bit Field	Access Type
Power Domain - Low Power State Change Control		PM_SGX_PWRSTCTRL[4] LOWPOWERSTATECHANGE	Read/Write
Memory Area - State Control (Logic in On state)	SGX_MEM	PM_SGX_PWRSTCTRL[17:16] SGX_MEM_ONSTATE	Read only
Power Domain - State Transition Control		PM_SGX_PWRSTCTRL[1:0] POWERSTATE	Read/Write

Table 3-265 lists the power modes status for the power domain.

Table 3-265. PD_SGX Power Modes Status Parameters

Parameter Name	Memory Bank	Status Bit Field
Memory Area - State Status	SGX_MEM	PM_SGX_PWRSTST[5:4] SGX_MEM_STATEST
Power Domain - State Transition Status		PM_SGX_PWRSTST[20] INTRANSITION
Logic Area - State Status		PM_SGX_PWRSTST[2] LOGICSTATEST
Power Domain - State Status		PM_SGX_PWRSTST[1:0] POWERSTATEST

3.7.9 PD_EMU Description

PD_EMU contains the following reset domains:

- EMU_EARLY_PWRON_RST
- EMU_PWRON_RST
- EMU_RST

PD_EMU contains the CD_EMU clock domain.

Table 3-266 lists the logic retention capability for each module of the power domain.

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Table 3-266. PD_EMU Modules Power Attributes

Module	Logic Retention	DFF Context Status	RFF Context Status
CM1_EMU	No	None	None
DEBUG	No	None	None

3.7.9.1 Power Domain Modes

This section highlights the various power modes supported by the logic and memory areas of the power domain. It also identifies the software control and status bit fields associated. See Section 3.1.1.2.1 for a functional description of the power-management architecture of a generic power domain.

3.7.9.1.1 Logic and Memory Area Power Modes

Table 3-267 lists the power modes supported by the logic area of the power domain.

Table 3-267. PD_EMU Logic Area Power Modes

Off	Retention-OSWR	Retention-CSWR	On-Inactive	On-Active
Available	Not available	Not available	Not available	Available

Table 3-268 presents the power modes supported by the memory area of the power domain. A memory area power mode is identified with respect to a power state of the power domain. The Logic On, Logic Retention, and Logic Off columns identify the power states of the power domain. The values in these columns identify the supported power state of the memory area (identified in the Memory Bank column) or the module memory inside the memory area (identified in the Module - Memory column). The RTA Feature column identifies whether the memory supports the RTA feature.

Table 3-268. PD_EMU Memory Area Power Modes

Memory Bank	Module - Memory	Logic On	Logic Retention	Logic Off	RTA Feature
	DEBUG - DebugSS_MEM	always_on	always_off		always_enabled

3.7.9.1.2 Logic and Memory Area Power Modes Control and Status

Table 3-269 lists the power modes controls for the power domain.

Table 3-269. PD_EMU Power Modes Control Parameters

Parameter Name	Memory Bank	Control Bit Field	Access Type
Memory Area - State Control (Logic in On state)	EMU_BANK	PM_EMU_PWRSTCTRL[17:16] EMU_BANK_ONSTATE	Read only
Power Domain - State Transition Control		PM_EMU_PWRSTCTRL[1:0] POWERSTATE	Read only

Table 3-270 lists the power modes status for the power domain.

Table 3-270. PD_EMU Power Modes Status Parameters

Parameter Name	Memory Bank	Status Bit Field
Memory Area - State Status	EMU_BANK	PM_EMU_PWRSTST[5:4] EMU_BANK_STATEST
Power Domain - State Transition Status		PM_EMU_PWRSTST[20] INTRANSITION
Logic Area - State Status		PM_EMU_PWRSTST[2] LOGICSTATEST
Power Domain - State Status		PM_EMU_PWRSTST[1:0] POWERSTATEST

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3.7.10 PD_DSS Description

PD_DSS contains the following reset domains:

- DSS_RET_RST
- DSS_RST

PD_DSS contains the CD_DSS clock domain.

Table 3-271 lists the logic retention capability for each module of the power domain.

Table 3-271. PD_DSS Modules Power Attributes

Module	Logic Retention	DFF Context Status	RFF Context Status
DSS	Partial	RM_DSS_DSS_CONTEXT[0] LOSTCONTEXT_DFF	RM_DSS_DSS_CONTEXT[1] LOSTCONTEXT_RFF

3.7.10.1 Power Domain Modes

This section highlights the various power modes supported by the logic and memory areas of the power domain. It also identifies the software control and status bit fields associated. See Section 3.1.1.2.1 for a functional description of the power-management architecture of a generic power domain.

3.7.10.1.1 Logic and Memory Area Power Modes

Table 3-272 lists the power modes supported by the logic area of the power domain.

Table 3-272. PD_DSS Logic Area Power Modes

Off	Retention-OSWR	Retention-CSWR	On-Inactive	On-Active
Available	Available	Available	Available	Available

Table 3-273 presents the power modes supported by the memory area of the power domain. A memory area power mode is identified with respect to a power state of the power domain. The Logic On, Logic Retention, and Logic Off columns identify the power states of the power domain. The values in these columns identify the supported power state of the memory area (identified in the Memory Bank column) or the module memory inside the memory area (identified in the Module - Memory column). The RTA Feature column identifies whether the memory supports the RTA feature.

Table 3-273. PD_DSS Memory Area Power Modes

Memory Bank	Module - Memory	Logic On	Logic Retention	Logic Off	RTA Feature
DSS_MEM		ON	OFF	OFF	
	DSS - DSSMEM	always_on	always_off		always_enabled

3.7.10.1.2 Logic and Memory Area Power Modes Control and Status

Table 3-274 lists the power modes controls for the power domain.

Table 3-274. PD_DSS Power Modes Control Parameters

Parameter Name	Memory Bank	Control Bit Field	Access Type
Memory Area - State Control (Logic in Retention state)	DSS_MEM	PM_DSS_PWRSTCTRL[8] DSS_MEM_RETSTATE	Read only
Power Domain - Low Power State Change Control		PM_DSS_PWRSTCTRL[4] LOWPOWERSTATECHANGE	Read/Write
Logic Area - Retention State Control		PM_DSS_PWRSTCTRL[2] LOGICRETSTATE	Read/Write
Memory Area - State Control (Logic in On state)	DSS_MEM	PM_DSS_PWRSTCTRL[17:16] DSS_MEM_ONSTATE	Read only

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Table 3-274. PD_DSS Power Modes Control Parameters (continued)

Parameter Name	Memory Bank	Control Bit Field	Access Type
Power Domain - State Transition Control		PM_DSS_PWRSTCTRL[1:0] POWERSTATE	Read/Write

Table 3-275 lists the power modes status for the power domain.

Table 3-275. PD_DSS Power Modes Status Parameters

Parameter Name	Memory Bank	Status Bit Field
Memory Area - State Status	DSS_MEM	PM_DSS_PWRSTST[5:4] DSS_MEM_STATEST
Power Domain - State Transition Status		PM_DSS_PWRSTST[20] INTRANSITION
Logic Area - State Status		PM_DSS_PWRSTST[2] LOGICSTATEST
Power Domain - State Status		PM_DSS_PWRSTST[1:0] POWERSTATEST

3.7.11 PD_CORE Description

PD_CORE contains the following reset domains:

- CM2_PWRON_RET_RST
- CM2_RET_RST
- CORE_PWRON_RET_RST
- CORE_RET_RST
- CORE_RST
- DLL_RST
- CORTEXM3_PWRON_RST
- CORTEXM3_RET_RST
- CORTEXM3_RST1
- CORTEXM3_RST2
- CORTEXM3_RST3
- EMIF_PWRON_RST
- SDMA_RET_RST

PD_CORE contains the following clock domains:

- CD_C2C
- CD_DMA
- CD_CORTEXM3
- CD_EMIF
- CD_L3_1
- CD_L3_2
- CD_L3_INSTR
- CD_L4_CFG

Table 3-276 lists the logic retention capability for each module of the power domain.

Table 3-276. PD_CORE Modules Power Attributes

Module	Logic Retention	DFF Context Status	RFF Context Status
SYSCTRL_PADCONF_CORE	Full	None	None
CM2	Full	None	None
DDRPHY	No	None	None

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Table 3-276. PD_CORE Modules Power Attributes (continued)

Module	Logic Retention	DFF Context Status	RFF Context Status
SYSCTRL_GENERAL_CORE	Full	None	None
DLL	No	None	None
DMM	Partial	RM_MEMIF_DMM_CONTEXT[0] LOSTCONTEXT_DFF	RM_MEMIF_DMM_CONTEXT[1] LOSTCONTEXT_RFF
CORTEXM3	Partial	RM_MPU_M3_MPU_M3_CONTEXT[0] LOSTCONTEXT_DFF	RM_MPU_M3_MPU_M3_CONTEXT[1] LOSTCONTEXT_RFF
EMIF1	Full	RM_MEMIF_EMIF_1_CONTEXT[0] LOSTCONTEXT_DFF	RM_MEMIF_EMIF_1_CONTEXT[1] LOSTCONTEXT_RFF
EMIF2	Full	RM_MEMIF_EMIF_2_CONTEXT[0] LOSTCONTEXT_DFF	RM_MEMIF_EMIF_2_CONTEXT[1] LOSTCONTEXT_RFF
EMIF_FW	Partial	RM_MEMIF_EMIF_FW_CONTEXT[0] LOSTCONTEXT_DFF	RM_MEMIF_EMIF_FW_CONTEXT[1] LOSTCONTEXT_RFF
GPMC	Full	None	RM_L3_2_GPMC_CONTEXT[1] LOSTCONTEXT_RFF
SPINLOCK	Full	None	RM_L4CFG_SPINLOCK_CONTEXT[1] LOSTCONTEXT_RFF
L3_2 interconnect	Partial	RM_L3_2_L3_2_CONTEXT[0] LOSTCONTEXT_DFF	RM_L3_2_L3_2_CONTEXT[1] LOSTCONTEXT_RFF
L3_3 interconnect	Partial	RM_L3INSTR_L3_3_CONTEXT[0] LOSTCONTEXT_DFF	RM_L3INSTR_L3_3_CONTEXT[1] LOSTCONTEXT_RFF
L3_1 interconnect	Partial	RM_L3_1_L3_1_CONTEXT[0] LOSTCONTEXT_DFF	RM_L3_1_L3_1_CONTEXT[1] LOSTCONTEXT_RFF
L3_INSTR interconnect	No	RM_L3INSTR_L3_INSTR_CONTEXT[0] LOSTCONTEXT_DFF	None
L4_CFG interconnect	Partial	RM_L4CFG_L4_CFG_CONTEXT[0] LOSTCONTEXT_DFF	RM_L4CFG_L4_CFG_CONTEXT[1] LOSTCONTEXT_RFF
Mailbox	Full	None	RM_L4CFG_MAILBOX_CONTEXT[1] LOSTCONTEXT_RFF
OCMC_RAM	No	RM_L3_2_OCMC_RAM_CONTEXT[0] LOSTCONTEXT_DFF	None
C2C	Partial	RM_C2C_C2C_CONTEXT[0] LOSTCONTEXT_DFF	RM_C2C_C2C_CONTEXT[1] LOSTCONTEXT_RFF
C2C_FW	Partial	RM_C2C_C2C_FW_CONTEXT[0] LOSTCONTEXT_DFF	RM_C2C_C2C_FW_CONTEXT[1] LOSTCONTEXT_RFF
SAR_ROM	No	RM_L4CFG_SAR_ROM_CONTEXT[0] LOSTCONTEXT_DFF	None
sDMA	Full	None	RM_SDMA_SDMA_CONTEXT[1] LOSTCONTEXT_RFF

3.7.11.1 Power Domain Modes

This section highlights the various power modes supported by the logic and memory areas of the power domain. It also identifies the software control and status bit fields associated. See Section 3.1.1.2.1 for a functional description of the power-management architecture of a generic power domain.

3.7.11.1.1 Logic and Memory Area Power Modes

Table 3-277 lists the power modes supported by the logic area of the power domain.

Table 3-277. PD_CORE Logic Area Power Modes

Off	Retention-OSWR	Retention-CSWR	On-Inactive	On-Active
Available	Available	Available	Available	Available

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Table 3-278 presents the power modes supported by the memory area of the power domain. A memory area power mode is identified with respect to a power state of the power domain. The Logic On, Logic Retention, and Logic Off columns identify the power states of the power domain. The values in these columns identify the supported power state of the memory area (identified in the Memory Bank column) or the module memory inside the memory area (identified in the Module - Memory column). The RTA Feature column identifies whether the memory supports the RTA feature.

Table 3-278. PD_CORE Memory Area Power Modes

Memory Bank	Module - Memory	Logic On	Logic Retention	logic off	RTA Feature
CORE_NRET_BANK		ON	OFF	OFF	
	DMM - DMM_MEMBANK2	always_on	always_off		None
CORE_OCMRAM		OFF, RETENTION, ON	OFF, RETENTION	OFF	
	OCMC_RAM - OCMC_RAM_Bank 1	software_control	software_control		always_enabled
CORE_OTHER_BANK		ON	RETENTION	OFF	
	sDMA - DMA_MEM	always_on	always_retention		None
	DMM - DMM_MEMBANK1	always_on	always_retention		always_enabled
MPU_M3_L2RAM		ON	OFF, RETENTION	OFF	
	CORTEXM3 - MPU_M3_L2RAM_MEM	always_on	software_control		always_enabled
MPU_M3_UNICACHE		ON	OFF, RETENTION	OFF	
	CORTEXM3 - MPU_M3_Unicache_mem	always_on	software_control		None

3.7.11.1.2 Logic and Memory Area Power Modes Control and Status

Table 3-279 lists the power modes controls for the power domain.

Table 3-279. PD_CORE Power Modes Control Parameters

Parameter Name	Memory Bank	Control Bit Field	Access Type
Memory Area - State Control (Logic in Retention state)	CORE_OCMRAM	PM_CORE_PWRSTCTRL[9] CORE_OCMRAM_RETSTATE	Read/Write
Memory Area - State Control (Logic in Retention state)	CORE_OTHER_BANK	PM_CORE_PWRSTCTRL[8] CORE_OTHER_BANK_RETSTATE	Read only
Memory Area - State Control (Logic in On state)	CORE_NRET_BANK	PM_CORE_PWRSTCTRL[25:24] INTRCONN_NRET_BANK_ONSTATE	Read only
Memory Area - State Control (Logic in On state)	MPU_M3_UNICACHE	PM_CORE_PWRSTCTRL[23:22] MPU_M3_UNICACHE_ONSTATE	Read only
Memory Area - State Control (Logic in On state)	MPU_M3_L2RAM	PM_CORE_PWRSTCTRL[21:20] MPU_M3_L2RAM_ONSTATE	Read only
Memory Area - State Control (Logic in On state)	CORE_OCMRAM	PM_CORE_PWRSTCTRL[19:18] CORE_OCMRAM_ONSTATE	Read/Write

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Table 3-279. PD_CORE Power Modes Control Parameters (continued)

Parameter Name	Memory Bank	Control Bit Field	Access Type
Memory Area - State Control (Logic in On state)	CORE_OTHER_BANK	PM_CORE_PWRSTCTRL[17:16] CORE_OTHER_BANK_ONSTATE	Read only
Memory Area - State Control (Logic in Retention state)	CORE_NRET_BANK	PM_CORE_PWRSTCTRL[12] INTRCONN_NRET_BANK_RETSTATE	Read only
Memory Area - State Control (Logic in Retention state)	MPU_M3_UNICACHE	PM_CORE_PWRSTCTRL[11] MPU_M3_UNICACHE_RETSTATE	Read/Write
Memory Area - State Control (Logic in Retention)	MPU_M3_L2RAM	PM_CORE_PWRSTCTRL[10] MPU_M3_L2RAM_RETSTATE	Read/Write
Logic Area - Retention State Control	N/A	PM_CORE_PWRSTCTRL[2] LOGICRETSTATE	Read/Write
Power Domain - Low Power State Change Control	N/A	PM_CORE_PWRSTCTRL[4] LOWPOWERSTATECHANGE	Read/Write
Power Domain - State Transition Control	N/A	PM_CORE_PWRSTCTRL[1:0] POWERSTATE	Read/Write

Table 3-280 lists the power modes status for the power domain.

Table 3-280. PD_CORE Power Modes Status Parameters

Parameter Name	Memory Bank	Status Bit Field
Power Domain - Last Power State Entered Status		PM_CORE_PWRSTST[25:24] LASTPOWERSTATEENTERED
Memory Area - State Status	MPU_M3_L2RAM	PM_CORE_PWRSTST[9:8] MPU_M3_L2RAM_STATEST
Memory Area - State Status	CORE_OCMRAM	PM_CORE_PWRSTST[7:6] CORE_OCMRAM_STATEST
Memory Area - State Status	CORE_OTHER_BANK	PM_CORE_PWRSTST[5:4] CORE_OTHER_BANK_STATEST
Memory Area - State Status	CORE_NRET_BANK	PM_CORE_PWRSTST[13:12] INTRCONN_NRET_BANK_STATEST
Memory Area - State Status	MPU_M3_UNICACHE	PM_CORE_PWRSTST[11:10] MPU_M3_UNICACHE_STATEST
Logic Area - State Status		PM_CORE_PWRSTST[2] LOGICSTATEST
Power Domain - State Transition Status		PM_CORE_PWRSTST[20] INTRANSITION
Power Domain - State Status		PM_CORE_PWRSTST[1:0] POWERSTATEST

3.7.12 PD_CAM Description

PD_CAM contains the CAM_RST reset domain.

PD_CAM contains the CD_CAM clock domain.

Table 3-281 lists the logic retention capability for each module of the power domain.

Table 3-281. PD_CAM Modules Power Attributes

Module	Logic Retention	DFF Context Status	RFF Context Status
FACE DETECT	No	RM_CAM_FDIF_CONTEXT[0] LOSTCONTEXT_DFF	None
ISS	No	RM_CAM_ISS_CONTEXT[0] LOSTCONTEXT_DFF	None

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3.7.12.1 Power Domain Modes

This section highlights the various power modes supported by the logic and memory areas of the power domain. It also identifies the software control and status bit fields associated. See Section 3.1.1.2.1 for functional description of the power-management architecture of a generic power domain.

3.7.12.1.1 Logic and Memory Area Power Modes

Table 3-282 lists the power modes supported by the logic area of the power domain.

Table 3-282. PD_CAM Logic Area Power Modes

Off	Retention-OSWR	Retention-CSWR	On-Inactive	On-Active
Available	Not available	Not available	Available	Available

Table 3-283 presents the power modes supported by the memory area of the power domain. A memory area power mode is identified with respect to a power state of the power domain. The Logic On, Logic Retention, and Logic Off columns identify the power states of the power domain. The values in these columns identify the supported power state of the memory area (identified in the Memory Bank column) or the module memory inside the memory area (identified in the Module - Memory column). The RTA Feature column identifies whether the memory supports the RTA feature.

Table 3-283. PD_CAM Memory Area Power Modes

Memory Bank	Module - Memory	Logic On	Logic Retention	Logic Off	RTA Feature
	FACE DETECT - FDIFMEM	always_on	always_off		always_enabled
	ISS - ISSMEM	always_on	always_off		always_enabled

3.7.12.1.2 Logic and Memory Area Power Modes Control and Status

Table 3-284 lists the power modes controls for the power domain.

Table 3-284. PD_CAM Power Modes Control Parameters

Parameter Name	Memory Bank	Control Bit Field	Access Type
Power Domain - Low Power State Change Control		PM_CAM_PWRSTCTRL[4] LOWPOWERSTATECHANGE	Read/Write
Memory Area - State Control (Logic in On state)	CAM_MEM	PM_CAM_PWRSTCTRL[17:16] CAM_MEM_ONSTATE	Read only
Power Domain - State Transition Control		PM_CAM_PWRSTCTRL[1:0] POWERSTATE	Read/Write

Table 3-285 lists the power modes status for the power domain.

Table 3-285. PD_CAM Power Modes Status Parameters

Parameter Name	Memory Bank	Status Bit Field
Memory Area - State Status	CAM_MEM	PM_CAM_PWRSTST[5:4] CAM_MEM_STATEST
Power Domain - State Transition Status		PM_CAM_PWRSTST[20] INTRANSITION
Logic Area - State Status		PM_CAM_PWRSTST[2] LOGICSTATEST
Power Domain - State Status		PM_CAM_PWRSTST[1:0] POWERSTATEST

3.7.13 PD_AUDIO Description

PD_AUDIO contains the following reset domains:

- AUDIO_PWRON_RST

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- AUDIO_RST

PD_AUDIO contains the CD_ABE clock domain.

Table 3-286 lists the logic retention capability for each module of the power domain.

Table 3-286. PD_AUDIO Modules Power Attributes

Module	Logic Retention	DFF Context Status	RFF Context Status
AUDIO ENGINE	No	RM_ABE_AESS_CONTEXT[0] LOSTCONTEXT_DFF	None
CM1_ABE	No	None	None
DMIC	No	RM_ABE_DMIC_CONTEXT[0] LOSTCONTEXT_DFF	None
L4_ABE interconnect	No	None	None
MCASP1	No	RM_ABE_MCASP_CONTEXT[0] LOSTCONTEXT_DFF	None
MCBSP1	No	RM_ABE_MCBSP1_CONTEXT[0] LOSTCONTEXT_DFF	None
MCBSP2	No	RM_ABE_MCBSP2_CONTEXT[0] LOSTCONTEXT_DFF	None
MCBSP3	No	RM_ABE_MCBSP3_CONTEXT[0] LOSTCONTEXT_DFF	None
MCPDM	No	RM_ABE_PDM_CONTEXT[0] LOSTCONTEXT_DFF	None
SLIMBUS1	No	RM_ABE_SLIMBUS_CONTEXT[0] LOSTCONTEXT_DFF	None
GPTIMER5	No	RM_ABE_GPTIMER5_CONTEXT[0] LOSTCONTEXT_DFF	None
GPTIMER6	No	RM_ABE_GPTIMER6_CONTEXT[0] LOSTCONTEXT_DFF	None
GPTIMER7	No	RM_ABE_GPTIMER7_CONTEXT[0] LOSTCONTEXT_DFF	None
GPTIMER8	No	RM_ABE_GPTIMER8_CONTEXT[0] LOSTCONTEXT_DFF	None
WDTIMER3	No	RM_ABE_WDTIMER3_CONTEXT[0] LOSTCONTEXT_DFF	None

3.7.13.1 Power Domain Modes

This section highlights the various power modes supported by the logic and memory areas of the power domain. It also identifies the software control and status bit fields associated. See Section 3.1.1.2.1 for a functional description of the power-management architecture of a generic power domain.

3.7.13.1.1 Logic and Memory Area Power Modes

Table 3-287 lists the power modes supported by the logic area of the power domain.

Table 3-287. PD_AUDIO Logic Area Power Modes

Off	Retention-OSWR	Retention-CSWR	On-Inactive	On-Active
Available	Available	Not available	Available	Available

Table 3-288 presents the power modes supported by the memory area of the power domain. A memory area power mode is identified with respect to a power state of the power domain. The Logic On, Logic Retention, and Logic Off columns identify the power states of the power domain. The values in these columns identify the supported power state of the memory area (identified in the Memory Bank column) or the module memory inside the memory area (identified in the Module - Memory column). The RTA Feature column identifies whether the memory supports the RTA feature.

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Table 3-288. PD_AUDIO Memory Area Power Modes

Memory Bank	Module - Memory	Logic On	Logic Retention	Logic Off	RTA Feature
AESSMEM		ON	RETENTION	OFF	
	AUDIO ENGINE - AESS_MemBank1	always_on	always_retention		always_enabled
PERIPHMEM		ON	OFF	OFF	
	DMIC - DMIC_BANK	always_on	always_off		None
	MCBSP1 - MCBSP_BANK	always_on	always_off		None
	MCPDM - MCPDM_BANK	always_on	always_off		None
	SLIMBUS1 - SLIMBUS_BANK	always_on	always_off		None

3.7.13.1.2 Logic and Memory Area Power Modes Control and Status

Table 3-289 lists the power modes controls for the power domain.

Table 3-289. PD_AUDIO Power Modes Control Parameters

Parameter Name	Memory Bank	Control Bit Field	Access Type
Memory Area - State Control (Logic in Retention state)	AESSMEM	PM_ABE_PWRSTCTRL[8] AESSMEM_RETSTATE	Read only
Memory Area - State Control (Logic in On state)	PERIPHMEM	PM_ABE_PWRSTCTRL[21:20] PERIPHMEM_ONSTATE	Read only
Memory Area - State Control (Logic in On state)	AESSMEM	PM_ABE_PWRSTCTRL[17:16] AESSMEM_ONSTATE	Read only
Memory Area - State Control (Logic in Retention state)	PERIPHMEM	PM_ABE_PWRSTCTRL[10] PERIPHMEM_RETSTATE	Read only
Logic Area - Retention State Control		PM_ABE_PWRSTCTRL[2] LOGICRETSTATE	Read only
Power Domain - Low Power State Change Control		PM_ABE_PWRSTCTRL[4] LOWPOWERSTATECHANGE	Read/Write
Power Domain - State Transition Control		PM_ABE_PWRSTCTRL[1:0] POWERSTATE	Read/Write

Table 3-290 lists the power modes status for the power domain.

Table 3-290. PD_AUDIO Power Modes Status Parameters

Parameter Name	Memory Bank	Status Bit Field
Power Domain - Last Power State Entered Status		PM_ABE_PWRSTST[25:24] LASTPOWERSTATEENTERED
Memory Area - State Status	PERIPHMEM	PM_ABE_PWRSTST[9:8] PERIPHMEM_STATEST
Memory Area - State Status	AESSMEM	PM_ABE_PWRSTST[5:4] AESSMEM_STATEST
Power Domain - State Transition Status		PM_ABE_PWRSTST[20] INTRANSITION
Logic Area - State Status		PM_ABE_PWRSTST[2] LOGICSTATEST
Power Domain - State Status		PM_ABE_PWRSTST[1:0] POWERSTATEST

3.7.14 PD_ALWON_MPU Description

PD_ALWON_MPU contains the following reset domains:

- ALWON_MPU_RST

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- DPLL_MPU_PWRON_RST

PD_ALWON_MPU has no associated clock domains.

Table 3-291 lists the logic retention capability for each module of the power domain.

Table 3-291. PD_ALWON_MPU Modules Power Attributes

Module	Logic Retention	DFF Context Status	RFF Context Status
DPLL_MPU	No	None	None
CORTEXA9_MPU_INTC	No	None	None

3.7.14.1 Power Domain Modes

The PD_ALWON_MPU power domain is an always-on power domain and does not switch to RETENTION state. There is no logic power state control or status bit field for this power domain.

The PD_ALWON_MPU power domain has no memory banks.

3.7.15 PD_ALWON_DSP Description

PD_ALWON_DSP contains the following reset domains:

- ALWON_IVA_RST
- DPLL_IVA_PWRON_RST

PD_ALWON_DSP has no clock domains associated.

Table 3-292 lists the logic retention capability for each module of the power domain.

Table 3-292. PD_ALWON_DSP Modules Power Attributes

Module	Logic Retention	DFF Context Status	RFF Context Status
DPLL_IVA	No	None	None
DSP_WKUPGEN	No	None	None

3.7.15.1 Power Domain Modes

The PD_ALWON_DSP power domain is an always-on power domain and does not switch to retention state. There is no logic power state control or status bit field for this power domain.

The PD_ALWON_DSP power domain has no memory banks.

3.7.16 PD_ALWON_CORE Description

PD_ALWON_CORE contains the following reset domains:

- ALWON_CM1_PWRON_RST
- ALWON_CM1_RST
- ALWON_CORE_PWRON_RST
- ALWON_CORE_RST

PD_ALWON_CORE contains the following clock domains:

- CD_ALWON_CM
- CD_L4_ALWON_CORE

Table 3-293 lists the logic retention capability for each module of the power domain.

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Table 3-293. PD_ALWON_CORE Modules Power Attributes

Module	Logic Retention	DFF Context Status	RFF Context Status
CM1	No	None	None
DPLL_ABE	No	None	None
DPLL_CORE	No	None	None
DPLL_PER	No	None	None
CORTEXM3_WKUPGEN	No	None	None
SDMA_WKUPGEN	No	None	None
SR_CORE	No	RM_ALWON_SR_CORE_CONTEXT[0] LOSTCONTEXT_DFF	None
SR_IVA	No	RM_ALWON_SR_IVA_CONTEXT[0] LOSTCONTEXT_DFF	None
SR_MPU	No	RM_ALWON_SR_MPU_CONTEXT[0] LOSTCONTEXT_DFF	None
SPINNER	No	None	None

3.7.16.1 Power Domain Modes

The PD_ALWON_CORE power domain is an always-on power domain and does not switch to RETENTION state. There is no logic power state control or status bit field for this power domain.

The PD_ALWON_CORE power domain has no memory banks.

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3.8 Voltage Management Functional Description

This section describes the voltage domains and voltage control architecture. It also explains the interactions between the device and the external power IC.

3.8.1 Overview

The voltage management architecture of the device is based on voltage sources managed by the PRCM module. They define the voltage domains within the device (see Section 3.1.1.3, *Voltage Management*). This partition of the voltage domains ensures independent voltage control of each voltage domain through dedicated SMPS or LDO. The following voltage domains are managed by the PRCM module:

- VDD_CORE_L
- VDD_MPU_L
- VDD_IVA_L
- LDO_CORE_M
- LDO_IVA_M
- LDO_MPU_M
- LDO_IVA_ABB
- LDO_MPU_ABB
- LDO_WAKEUP

NOTE: See Table 3-25 for device power supply pin association to the power domain.

The PRCM module supports the AVS technique on the VDD_MPU_L, VDD_CORE_L and VDD_IVA_L voltage domains, through automatic monitoring and adjustments of voltages by their dedicated SmartReflex modules. The VDD_MPU_L and VDD_IVA_L voltage domains support five DVFS OPPs. The VDD_CORE_L voltage domain supports three DVFS OPPs.

The PRCM module also supports ABB technique on the MPU and IVA voltage domains, through the LDO_MPU_ABB and LDO_IVA_ABB biasing voltages.

The PRCM module automatically scales down the LDO_MPU_M, LDO_CORE_M, and LDO_IVA_M to retention voltage level whenever all memory banks on these domain have transitioned to the RETENTION or OFF power state.

Table 3-294 lists the supported DVFS OPPs for each voltage domain. The exact values depend on the silicon; for more information, see the *Data Manual Operating Condition Addendum*.

Table 3-294. Supported DVFS OPPs Summary

Voltage Domain	Operating Point	Control
VDD_MPU_L (vdd_mpu)	OFF RETENTION OPP50 OPP100 OPP_TURBO OPP_NITRO OPP_NTSB	Hardware and software
VDD_IVA_L (vdd_iva)	OFF RETENTION OPP50 OPP100 OPP_TURBO OPP_NITRO OPP_NTSB	Hardware and software

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Table 3-294. Supported DVFS OPPs Summary (continued)

Voltage Domain	Operating Point	Control
VDD_CORE_L (vdd)	OFF RETENTION OPP50 OPP100 OPP119	Hardware and software

NOTE: For the supported OPPs for each device in the OMAP4460 family, see the *Data Manual Operating Condition Addendum*.

DVFS OPPs Dependencies

For detailed information about DVFS OPP dependencies, see the *Data Manual Operating Condition Addendum*.

For more information, see Section 3.8.6.4, *DVFS Voting Mechanism (VDD_CORE_L and VDD_IVA_L Voltage Domains)*.

3.8.2 Voltage-Control Architecture

The PRM is split over several blocks that manage the different voltage sources.

- Voltage processors for converting SmartReflex data to voltage values before sending to the voltage controller
- Voltage FSMs for hardware control of voltages. They either send commands to the voltage controller (I^2C mode).
- A voltage controller for gathering commands from the PRCM module register (direct access), voltage processors and voltage PRCMs. It then handles communication with the external power IC through the dedicated I^2C interface.
- A device PRCM for managing the voltage PRCMs and I/O wake-up control and system clock control sequencing during device sleep and wake-up transitions.
- LDO regulator controllers for ABB management, memory arrays voltage management and WAKEUP logic.
- Bandgap reference voltage sleep control

NOTE: The SmartReflex module allows dynamic voltage adjustments around an OPP voltage level to ensure target performance. It also allows switching from one OPP to another. However, it does not control voltage switching of the voltage domain to RETENTION or OFF level when all power domains within the power domain are in RETENTION or OFF power states. This is handled by the voltage PRCMs.

Figure 3-75 shows the architecture for PRM voltage control.

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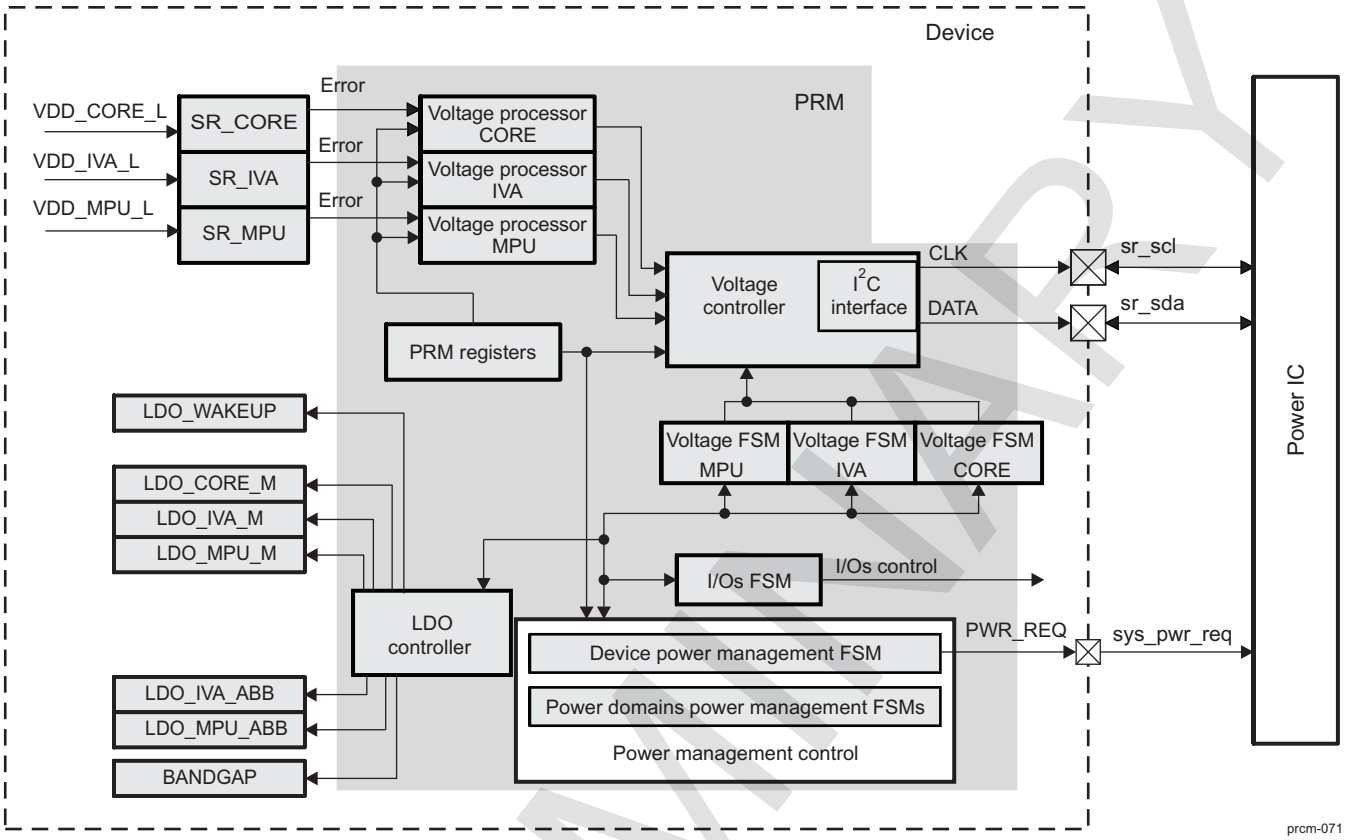
Figure 3-75. PRM Voltage Control Architecture



3.8.3 VDD_MPU_L, VDD_CORE_L, and VDD_IVA_L Control

These power supply sources can be controlled using PRM dedicated I²C control.

3.8.3.1 PRM Dedicated I²C Control

The PRM I²C interface is dedicated to SmartReflex voltage control. It enables the voltage controller to send voltage commands to the external power IC. To reduce latency of voltage changes, the voltage controller is configurable to run in HS I²C mode. The PRM I²C interface supports multimaster mode.

The voltage controller receives voltage control commands from following input ports:

- Voltage processors ports: Each voltage processor sends voltage change commands to the voltage controller depending on the information received from the associated SmartReflex module.
- Voltage PRCMs ports: Each voltage PRCM sends commands to the voltage controller when the device enters RETENTION or OFF power state, and also when the device wakes up.
- PRM register port: The PRM registers give direct software control over the voltage levels of the external voltage sources.

An arbitration scheme in the voltage controller manages concurrent requests on different ports.

Each internal port has a handshake to indicate when the I²C frame resulting from the request on that port has been acknowledged by the external Power IC.

The PRM can also send external voltage source sleep commands that can be used to activate power IC sleep mode, where the voltage regulator maintains output voltage but only a small load is supported. This lets the external power IC reduce its power consumption as well.

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NOTE: An I^2C interface not controlled by the PRM can be used to program voltage levels of the external power IC. Because it is not a hardware-controlled interface its use is restricted to move the voltage level from one OPP to another.

In this case, the control software must operate voltage transition when the device activity allows one.

3.8.3.2 Adaptive Voltage Scaling

As explained in Section 3.1.2.4, *Adaptive Voltage Scaling*, SmartReflex is a technology that uses adaptive power supply to achieve the goal of reducing active power consumption. With SmartReflex, the power supply voltage can be adapted to the silicon performance either statically (for example, adapted to the manufacturing process of a given device), or dynamically (for example, adapted to the temperature-induced current performance of the device).

SmartReflex voltage control in the device is based on the dedicated SmartReflex modules and the voltage processors, in addition to the voltage controller with dedicated I^2C interface, which are shared with the voltage PRCM modules and voltage control registers.

The SmartReflex modules allow a continuous real-time monitoring of voltage supply and device performance to do the following:

- Minimize the supply voltage to reduce the device power consumption.
- Maintain the desired device performance (by dynamically adjusting the device voltage) as the temperature of the device varies.

Because the SmartReflex modules and the voltage processors are dedicated to SmartReflex voltage control, they are described together in this section.

3.8.3.2.1 SmartReflex in the Device

Figure 3-76 shows the SmartReflex integration.

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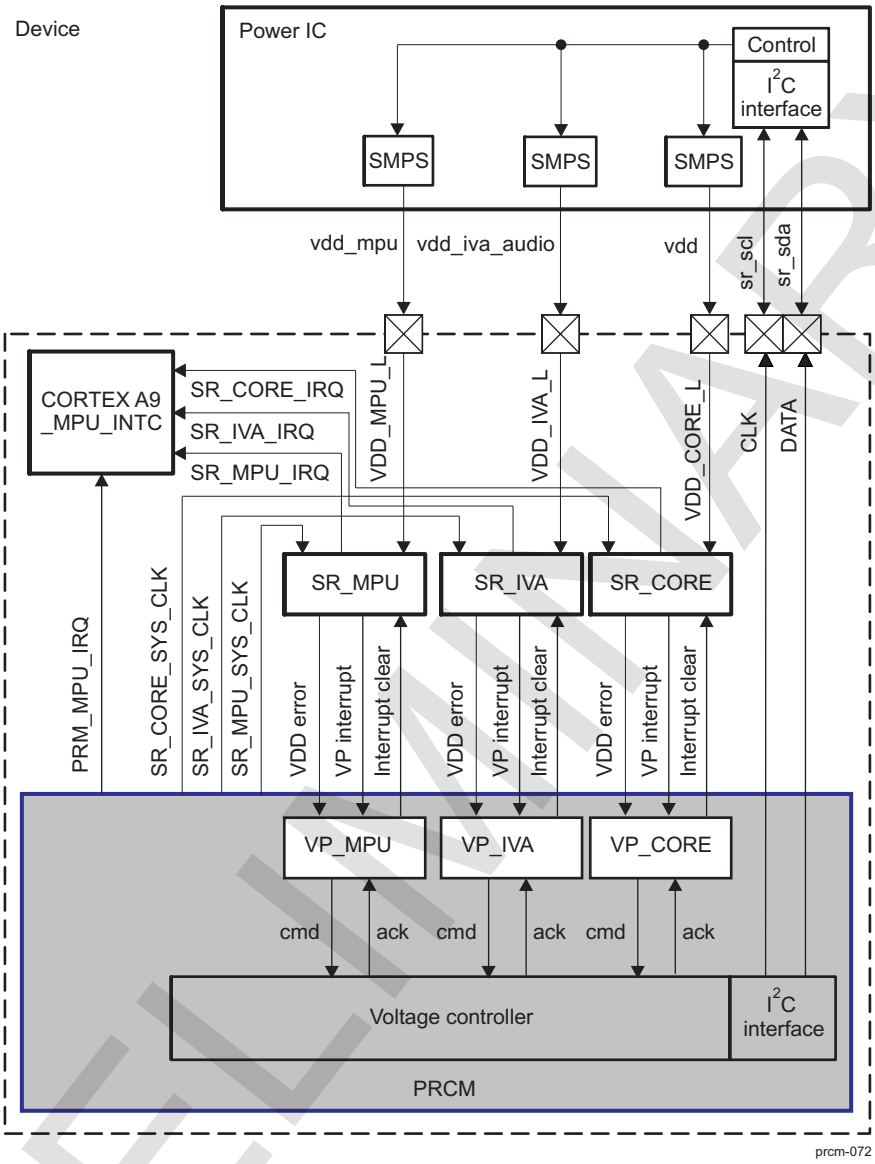
Figure 3-76. SmartReflex Integration



SmartReflex voltage control in the device is implemented for simultaneous control of three independent voltage sources. One SmartReflex module controls the VDD_CORE_L voltage, the second one is dedicated to VDD_IVA_L control, and the third controls the VDD_MPU_L voltage. Each SmartReflex module is connected to a voltage processor. Voltage commands from all voltage processors are passed to a voltage control, which sends them through a dedicated I^2C master interface to the power IC.

SmartReflex modules are in the PD_ALWON_CORE power domain and supplied by the VDD_CORE_L voltage domain. Each module senses its own voltage domain (VDD_CORE_L, VDD_IVA_L, or VDD_MPU_L).

3.8.3.2.2 SmartReflex Module

Figure 3-77 is a functional overview of the SmartReflex module.

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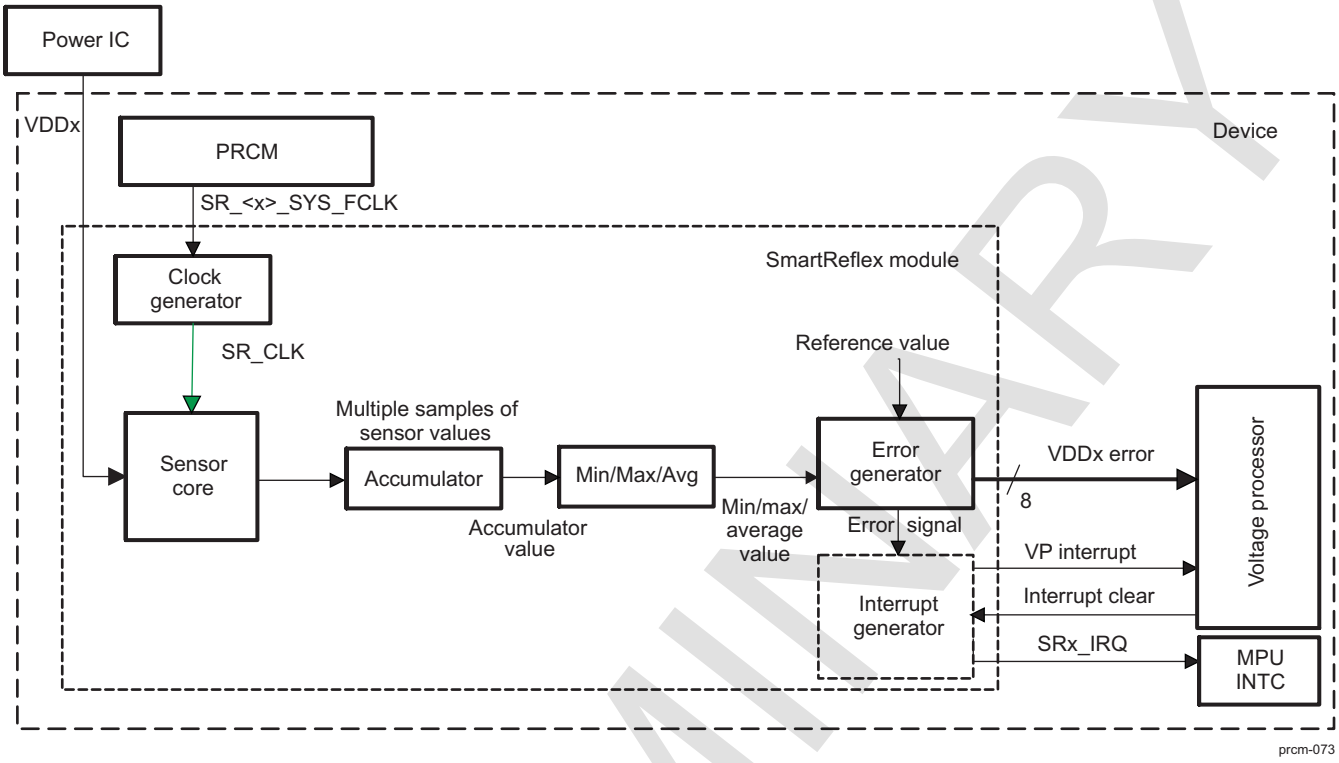
Figure 3-77. SmartReflex Module Functional Overview



3.8.3.2.3 SmartReflex Submodules

NOTE: In this and following section SRn refers to SR_IVA, SR_MPU, and SR_CORE SmartReflex modules.

The SmartReflex module is enabled by setting the SRn.SRCONFIG[11] SR_EN bit. The SmartReflex module is composed of six blocks:

- Clock generator
- Sensor core
- Accumulator
- Minimum/maximum/average
- Error generator
- Interrupt generator

Clock Generator

The clock generator provides the internal SR_CLK sampling clock to the sensor core of the module. The SRn.SRCONFIG[21:12] SRCLKLENGTH bit field allows the setting of the frequency divider ratio between the SRn_SYS_CLK and the SR_CLK. It is calculated using Equation 1:

$$SRn.SRCONFIG[21:12]\ SRCLKLENGTH = f_{SRn_SYS_CLK}/(2^* f_{SR_CLK}) \quad (1)$$

Where $f_{SRn_SYS_CLK}$ is the frequency of the SRn_SYS_CLK, and f_{SR_CLK} is the desired SR_CLK frequency.

To accurately use the target values programmed for SmartReflex modules in the device, the SRCLKLENGTH parameter must be set correctly. The target values for the SmartReflex modules are calculated with the SR_CLK frequency set at 100 kHz. It is thus mandatory that the value of the SRCLKLENGTH parameter is calculated from Equation 1-1 with f_{SR_CLK} set at 100 kHz.

For example, if the system clock has a frequency of 38.4 MHz, and the target SR_CLK frequency is 100 kHz, the SRn.SRCONFIG[21:12] SRCLKLENGTH bit field is 192 (0x0C0).

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Sensor Core

The sensor core receives the SR_CLK sampling clock and the voltage to be sensed. It generates sensor value samples proportional to the voltage sensed. For accuracy, a sensor core is composed of two sensors and generates two values per sample (one from each sensor).

The two sample values generated by the sensor core output can be read from the SRn.SENVAL[15:0] SENNVAL and SRn.SENVAL[31:16] SENPVAL bit fields.

The sensor core is enabled by the SRn.SRCONFIG[10] SENENABLE bit.

Accumulator

The accumulator consists of two stacks that store multiple samples of the two sensor values received from the sensor core.

The SRn.SRCONFIG[31:22] ACCUMDATA bit field defines the size of the accumulator in the number of samples to be stored. The allowable range is from 2 to 1023. The value of SRn.SRCONFIG[31:22] ACCUMDATA value is related to the desired sampling time window ($T_{TimeWindow}$) and the SR_CLK frequency (f_{SR_CLK}). It can be calculated using Equation 2:

$$\text{SRn.SRCONFIG[31:22] ACCUMDATA} = T_{TimeWindow} * f_{SR_CLK} \quad (2)$$

For example, for an accumulator time window of 10 ms and SR_CLK frequency of 32 kHz, the value of SRn.SRCONFIG[31:22] ACCUMDATA is 320 (0x140). The accumulation window must be large enough so that the minimum, maximum, and average counter values are accurate.

Minimum/Maximum/Average

The minimum/maximum/average block reads the samples stored in the accumulator and returns the minimum, maximum, and average values of the samples. Because the accumulator contains two separate groups of samples (one from each sensor of the sensor core), the minimum/maximum/average block also generates two sets of minimum, maximum, and average values.

The minimum, maximum, and average values of the samples of the first sensor can be read from the SRn.SENMIN[15:0] SENNMIN, SRn.SENMAX[15:0] SENNMAX, and SRn.SENAVG[15:0] SENNAVG bit fields.

For the sample values of the second sensor, the minimum, maximum, and average values can be read from the SRn.SENMIN[31:16] SENPMIN, SRn.SENMAX[31:16] SENPMAX, and SRn.SENAVG[31:16] SENPAVG bit fields.

The minimum/maximum/average block is enabled by the SRn.SRCONFIG[8] MINMAXAVGENABLE bit.

Error Generator

The error generator block reads the sample value generated by the sensor core and compares it with a reference value to calculate the error. This error is then passed to the voltage processor and the internal interrupt generator block.

The reference value for a given OPP of the device is configured by setting the SRn.NVALUERECIPROCAL[23:20] SENPGAIN, SRn.NVALUERECIPROCAL[19:16] SENNGAIN, SRn.NVALUERECIPROCAL[15:8] RNSENP, and SRn.NVALUERECIPROCAL[7:0] RNSENN bit fields by reading corresponding values from the eFuses (see Section 3.8.3.2.5, *SmartReflex Parameters Set After Silicon Characterization*).

The error generator sets the SRn.SRSTATUS[1] ERRGEN_VALID status bit when a valid error value is set in the SRn.SENERROR register.

The SRn.SENERROR register contains the average error (SRn.SENERROR[15:8] AVGERROR) and the percentage of error (SRn.SENERROR[7:0] SENERROR).

The error generator block is enabled by the SRn.SRCONFIG[9] ERRORGENERATORENABLE bit.

Interrupt Generator

The interrupt generator block generates interrupts to the MPU INTC and the voltage processor module (if the corresponding interrupts are enabled) to indicate errors.

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Table 3-295 and Table 3-296 list the interrupt events in the SmartReflex module and their enable and status bits.

Table 3-295. SmartReflex Interrupt Events

Interrupt Type	Description
Accumulator	The minimum/maximum/average module has completed computation over the accumulator data.
Valid	The average error is less than 2 percent of the true average error.
Disable acknowledge	The SmartReflex module is disabled and has cleared all MPU INTC and VP interrupts (internal registers are reset). This interrupt indicates to the software that the SmartReflex module is available for programming.
Bounds	The frequency error has crossed the maximum limit (ERRMAXLIMIT) or the minimum limit (ERRMINLIMIT). It is mapped to the voltage processor also.

The SRn_CORTEX_M3_IRQs from SR_IVA and SR_CORE are mapped to the MM_IRQ_47 interrupt line of the CORTEXM3_MPU_INTC.

Table 3-296. SmartReflex Interrupt Events Enable and Status Bits

Interrupt Type	Enable Bit	Status Bit
Accumulator	SRn.IRQENABLE_SET[3] MCUACCUMINTENSET	SRn.IRQSTATUS[3] MCUACCUMINTSTATENA
	SRn.IRQENABLE_CLR[3] MCUACCUMINTENCLR	
Valid	SRn.IRQENABLE_SET[2] MCUVALIDINTENSET	SRn.IRQSTATUS[2] MCUVALIDINTSTATENA
	SRn.IRQENABLE_CLR[2] MCUVALIDINTENCLR	
Disable acknowledge	SRn.IRQENABLE_SET[0] MCUDISABLEACKINTENSET	SRn.IRQSTATUS[0] MCUDISABLEACKINTSTATENA
	SRn.IRQENABLE_CLR[0] MCUDISABLEACKINTENCLR	
Bounds	SRn.IRQENABLE_SET[1] MCUBOUNDSINTENSET	SRn.IRQSTATUS[1] MCUBOUNDSINTSTATENA
	SRn.IRQENABLE_CLR[1] MCUBOUNDSINTENCLR	
	SRn.ERRCONFIG[22] VPBOUNDSINTENABLE	SRn.ERRCONFIG[23] VPBOUNDSINTSTATENA

The minimum and maximum error limits for the bounds interrupt are configured in the SRn.ERRCONFIG[15:8] ERRMAXLIMIT and SRn.ERRCONFIG[7:0] ERRMINLIMIT bit fields.

With automatic (also called hardware or Class-3) voltage control, the voltage processor interrupt (SRn.ERRCONFIG[31] VPBOUNDINTEN) is enabled and the SmartReflex module interrupts the voltage processor when the error crosses the error limits. In this case, the CORTEXM3 interrupts can also be enabled to allow software to monitor the behacior of the SmartReflex module.

With manual (also called software or Class-2) voltage control, the voltage processor interrupt remains disabled and only the CORTEXM3 interrupts are enabled. Thus, when an interrupt condition occurs, the CORTEXM3 is interrupted and software can then control the voltage by generating voltage commands.

Writing 1 to a bit in the IRQSTATUS register clears the interrupt pending status of each interrupt source whose corresponding bit is 1 in the value written. Other interrupt pending status bits are not affected (writing 0 to that bit does not affect the status).

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3.8.3.2.4 Status Register

The status register (SRSTATUS) indicates the validity of the minimum/maximum/average and error generator output values.

SRSTATUS has the following bits and bit fields:

- SRn.SRSTATUS[3] AVGERRVALID: Indicates the validity of the value in the SRn.SENERROR_REG[15:8] AVGERROR bit field. When the value is 0, the average error is not valid. When the value is 1, the average error is within 2 percent of the valid average error.
- SRn.SRSTATUS[2] MINMAXAVGVALID: Indicates the validity of the SRn.SENVAL, SRn.SENMIN, SRn.SENMAX, and SRn.SENAVG registers. When the value is 0, the registers are not valid. When the value is 1, the registers contain valid values, although the values are not necessarily fully accumulated.
- SRn.SRSTATUS[1] ERRGEN_VALID: Indicates the validity of the value in the SRn.SENERROR_REG[7:0] SENERROR bit field. When the value is 0, the error value is invalid. When the value is 1, the error value is valid.
- SRn.SRSTATUS[0] MINMAXAVGACCUMVALID: Indicates that the SRn.SENVAL, SRn.SENMIN, SRn.SENMAX, and SRn.SENAVG registers contain their final values accumulated over the defined sample time period.

3.8.3.2.5 SmartReflex Parameters Set After Silicon Characterization

Certain parameters of the SmartReflex module are characterized and calibrated after silicon testing. These values are then either set in the eFuse farm of the device or provided separately. Users must configure these parameters according to their given values to ensure correct functioning of the module.

The values for the following parameters (explained in Section 3.8.3.2.3, *SmartReflex Submodules*) are set in the device eFuse after device silicon characterization:

- SRn.SRCONFIG[6:5] SENNENABLE
- SRn.SRCONFIG[4:3] SENPENABLE
- SRn.NVALUERECIPROCAL[23:20] SENPGAIN
- SRn.NVALUERECIPROCAL[19:16] SENNGAIN
- SRn.NVALUERECIPROCAL[15:8] RNSENP
- SRn.NVALUERECIPROCAL[7:0] RNSENN

The eFuse values of these parameters must be read from the corresponding registers of the control module.

Information about the following parameters of the SmartReflex module is provided after silicon characterization:

- SRn.AVGWEIGHT[3:2] SENPAVGWEIGHT
- SRn.AVGWEIGHT[1:0] SENNAVGWEIGHT
- SRn.ERRCONFIG[18:16] ERRWEIGHT
- SRn.ERRCONFIG[15:8] ERRMAXLIMIT
- SRn.ERRCONFIG[7:0] ERRMINLIMIT

3.8.3.2.6 Voltage Processor Module

Figure 3-78 is a functional overview of the voltage processor.

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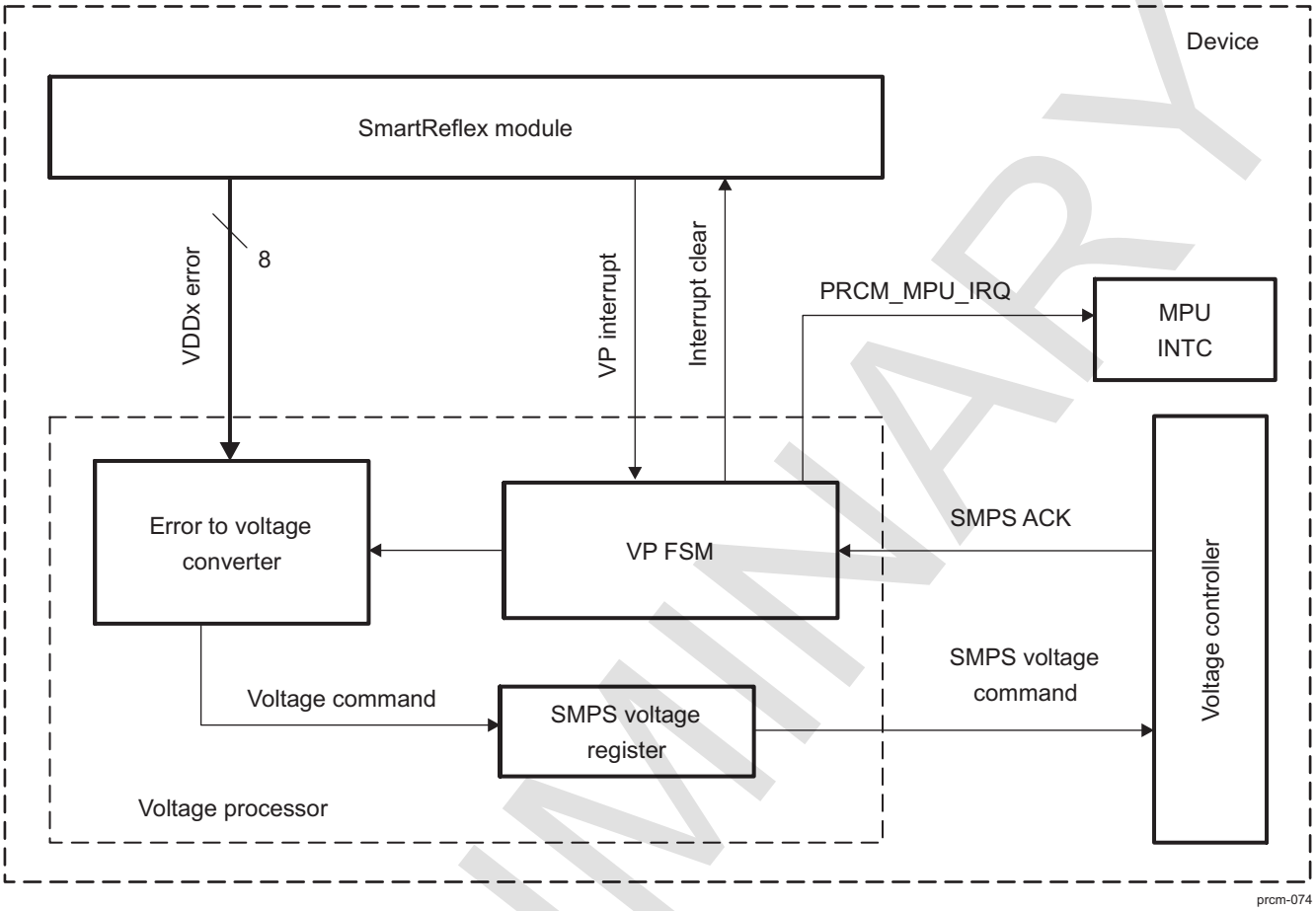
Figure 3-78. Voltage Processor Functional Overview



The voltage processor receives an error value and a VP interrupt signal from the SmartReflex module. Each time a new error value is sent, the SmartReflex module triggers an interrupt to inform the voltage processor. The voltage processor consists of an error-to-voltage command converter and a state controller. It processes an error and sends a voltage command to the voltage controller. It receives an acknowledge signal from the voltage controller when the SMPS receives the command. The voltage processor then acknowledges the SmartReflex module by clearing its interrupt.

The voltage processor is enabled by the PRM_VPn_CONFIG[0] VPENABLE bit.

Voltage Processor Interrupts

The voltage processor uses the PRCM_CORTEXM3_MPU_IRQ (MM_IRQ_46 of CORTEXM3_MPU_INTC) interrupt line of the CORTEXM3. Table 3-297 and Table 3-298 list the interrupt events in the voltage processor module and their enable and status bits.

Table 3-297. Voltage Processor Interrupt Events

Interrupt Type	Description
Transaction done	Voltage processor transaction is complete.
Equal value	Voltage requested in the new voltage command is the same as the current SMPS voltage.
No SMPS acknowledge	SMPS has not responded in a defined time interval to the transmitted voltage command.
Maximum VDD	New voltage requested in the voltage command is equal to or greater than maximum VDD.
Minimum VDD	New voltage requested in the voltage command is equal to or less than minimum VDD.
OPP change done	The average error is within the desired limit.

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NOTE: Transaction done and OPP change done interrupt events are generated under the same conditions (after voltage change).

Table 3-298. Voltage Processor Interrupt Event Enable and Status Bits

Interrupt Type	Enable Bit	Status Bit
Transaction done	PRM_IRQENABLE_MPU_M3[21] VP_CORE_TRANXDONE_EN	PRM_IRQSTATUS_MPU_M3[21] VP_CORE_TRANXDONE_ST
	PRM_IRQENABLE_MPU_M3[29] VP_IVA_TRANXDONE_EN	PRM_IRQSTATUS_MPU_M3[29] VP_IVA_TRANXDONE_ST
Equal value	PRM_IRQENABLE_MPU_M3[20] VP_CORE_EQVALUE_EN	PRM_IRQSTATUS_MPU_M3[20] VP_CORE_EQVALUE_ST
	PRM_IRQENABLE_MPU_M3[28] VP_CORE_EQVALUE_EN	PRM_IRQSTATUS_MPU_M3[28] VP_IVA_EQVALUE_ST
No SMPS acknowledge	PRM_IRQENABLE_MPU_M3[19] VP_CORE_NOSMPSACK_EN	PRM_IRQSTATUS_MPU_M3[19] VP_CORE_NOSMPSACK_ST
	PRM_IRQENABLE_MPU_M3[27] VP_IVA_NOSMPSACK_EN	PRM_IRQSTATUS_MPU_M3[27] VP_IVA_NOSMPSACK_ST
Maximum VDD	PRM_IRQENABLE_MPU_M3[18] VP_CORE_MAXVDD_EN	PRM_IRQSTATUS_MPU_M3[18] VP_CORE_MAXVDD_ST
	PRM_IRQENABLE_MPU_M3[26] VP_IVA_ MAXVDD_EN	PRM_IRQSTATUS_MPU_M3[26] VP_IVA_MAXVDD_ST
Minimum VDD	PRM_IRQENABLE_MPU_M3[17] VP_CORE_MINVDD_EN	PRM_IRQSTATUS_MPU_M3[17] VP_CORE_MINVDD_ST
	PRM_IRQENABLE_MPU_M3[25] VP_IVA_MINVDD_EN	PRM_IRQSTATUS_MPU_M3[25] VP_IVA_MINVDD_ST
OPP change done	PRM_IRQENABLE_MPU_M3[16] VP_CORE_OPPCHANGEDONE_EN	PRM_IRQSTATUS_MPU_M3[16] VP_CORE_OPPCHANGEDONE_ST
	PRM_IRQENABLE_MPU_M3 [24] VP_IVA_OPPCHANGEDONE_EN	PRM_IRQSTATUS_MPU_M3[24] VP_IVA_OPPCHANGEDONE_ST

Voltage Processor Status

The status of the voltage processor is represented by the following:

Bit/Bit Field	Parameter	Description
PRCM module.PRM_VPn_VOLTAGE[7:0] VPVOLTAGE	Current voltage for SMPS	Value of the current voltage level requested by the voltage processor
PRCM module.PRM_VPn_STATUS[0] VPINIDLE	Voltage processor in INACTIVE state	The voltage processor is in idle mode.

Voltage Processor Parameters

The following parameters of the voltage processor must be configured:

Bit/Bit Field	Parameter	Description
PRCM.PRM_VPn_CONFIG[31:24] ERROROFFSET	Error offset	Error in voltage offset value
PRCM.PRM_VPn_CONFIG[231:16] ERRORGAIN	Error gain	Error in voltage gain value
PRCM.PRM_VPn_CONFIG[3] TIMEOUTEN	Time-out enable	Enables/disables the time-out set by the time-out delay parameter
PRCM.PRM_VPn_VSTEPMIN[7:0] VSTEPMIN	Minimum step size	Minimum voltage step size
PRCM.PRM_VPn_VSTEPMAX[7:0] VSTEPMAX	Maximum step size	Maximum voltage step size
PRCM.PRM_VPn_VLIMITTO[31:24] VDDMAX	Maximum VDD limit	Maximum voltage limit of the VDD
PRCM.PRM_VPn_VLIMITTO[23:16] VDDMIN	Minimum VDD limit	Minimum voltage limit of the VDD
PRCM.PRM_VPn_VLIMITTO[15:0] TIMEOUT	Time-out delay	Maximum delay between a voltage change command and its acknowledge

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Bit/Bit Field	Parameter	Description
PRCM.PRM_VPn_CONFIG[15:8] INITVDD	Initial VDD voltage	Initial voltage set in the voltage processor
PRCM.PRM_VPn_CONFIG[2] INITVDD	Initialize VDD	Set initial voltage given in initial VDD voltage parameter in the voltage processor
PRCM.PRM_VPn_VSTEPMIN[23:8] SMPSWAITTIMEMIN	Minimum SMPS wait time	Slew rate for negative voltage steps
PRCM.PRM_VPn_VSTEPMAX[28:8] SMPSWAITTIMEMAX	Maximum SMPS wait time	Slew rate for positive voltage steps
PRCM.PRM_VPn_CONFIG[1] FORCEUPDATE	Force update	Sends the value of the VP current voltage parameter as the new voltage command to SMPS

3.8.3.2.7 SMPS-Dependent Parameter Configuration

The values of the following parameters of the voltage processor module depend on the characteristics of the SMPS used:

- PRCM.PRM_VPn_CONFIG[31:24] ERROROFFSET
- PRCM.PRM_VPn_CONFIG[23:16] ERRORGAIN
- PRCM.PRM_VPn_VSTEPMIN[7:0] VSTEPMIN
- PRCM.PRM_VPn_VSTEPMAX[7:0] VSTEPMAX
- PRCM.PRM_VPn_VLIMITTO[31:24] VDDMAX
- PRCM.PRM_VPn_VLIMITTO[23:16] VDDMIN
- PRCM.PRM_VPn_VLIMITTO[15:0] TIMEOUT
- PRCM.PRM_VPn_VSTEPMIN[23:8] SMPSWAITTIMEMIN
- PRCM.PRM_VPn_VSTEPMAX[28:8] SMPSWAITTIMEMAX

For information about the values of these parameters, see the specification document of the SMPS used.

3.8.3.2.8 Communication Between SmartReflex, Voltage Processor, Voltage Controller, and SMPS

The SmartReflex module, voltage processor, voltage controller, and SMPS implement a simple handshake protocol based on a request/acknowledge mechanism (see Figure 3-79):

1. The SmartReflex module generates a VP interrupt (clears to 0) when the average error crosses the minimum or maximum error bounds.
2. The average VDDx error is passed to the voltage processor when automatic voltage control is enabled.
3. The voltage processor reads the error and generates the voltage command for the SMPS. It then informs the voltage controller that a new voltage command is ready for the SMPS. The voltage controller sends the voltage command to the SMPS (external power IC) through the dedicated I^2C interface.
4. The SMPS responds to the reception of the voltage command with an acknowledgement to the voltage controller.
5. The voltage controller sends the acknowledgement to the voltage processor.
6. The voltage processor sends the interrupt-clear signal to the SmartReflex module.
7. The SmartReflex module clears the VP interrupt. It is now again ready to send a new frequency-error interrupt to the voltage processor.

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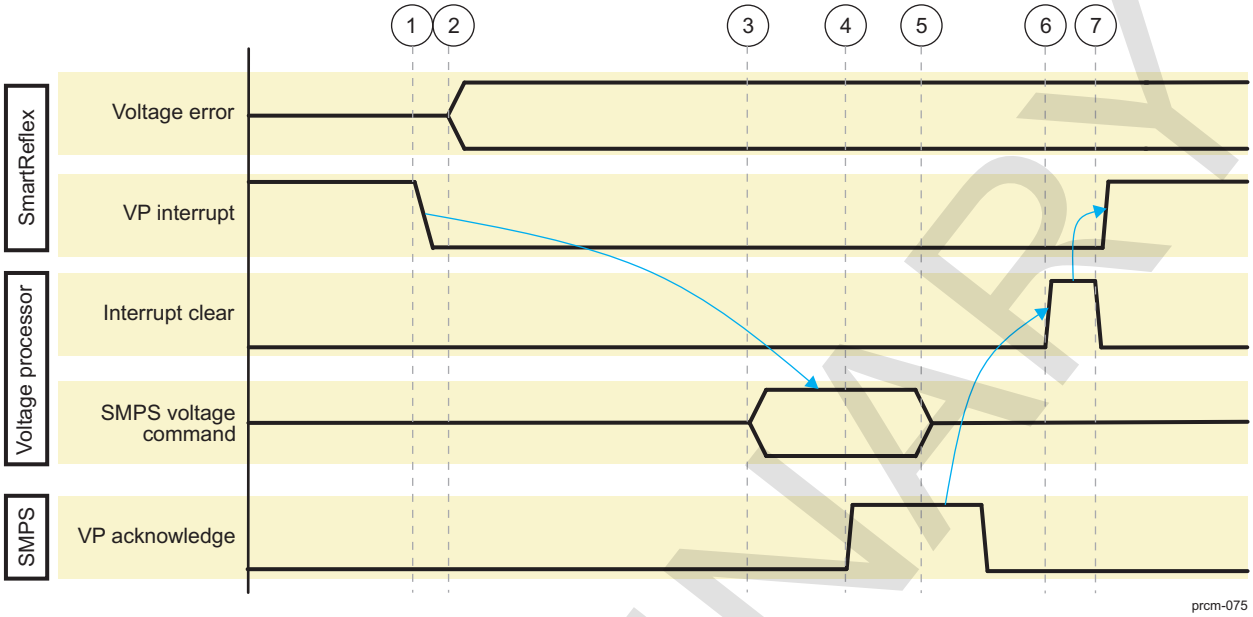
Figure 3-79. SmartReflex – SMPS Communication for Automatic Voltage Adjustments



3.8.4 Internal LDOs Control

3.8.4.1 Memory LDOs

Embedded SRAM LDOs (that is, LDO_CORE_M, LDO_IVA_M and LDO_MPU_M) are used to supply power to the split-rail memory arrays. The PRM generates the controls used to select LDO operating mode: on-active, on-retention, or off.

Split-rail type SRAMs are used in the device to implement the larger memories. These SRAMs feature memory array and periphery logic which are on separate supplies to allow independent power management. Proper memory operation, however, requires the SRAM array voltage to never be operated at a level lower than the SRAM periphery logic.

Memory LDO can switch to on, retention and off mode:

- On mode: 1.2 V is the normal voltage reference used through all functional OPPs, whenever memories must be functional. When logic voltage level VDD_x_L (where x can be MPU, CORE or IVA) becomes higher than the associated memory voltage level VDD_x_M, the LDO operates in the tracking mode and follows its respective the VDD_x_L voltage level.
- Retention mode: 0.6 V is set when software allows and when all memories banks belonging to the LDO memory voltage are in Retention or Off state. In this mode, the output voltage is generated from the corresponding VDD_x_L logic voltage source.
- Off mode: 0 V is set when the device switches to off mode.

Section 3.8.5.1, *Memory LDOs Transitions*, presents the state transition conditions and sequences for the memory LDOs.

NOTE: The voltage levels associated with the different modes may depend on the device characteristics.

3.8.4.2 LDO_WAKEUP

LDO_WAKEUP supports three voltage states depending on the PD_WKUP and PD_EMU activity:

- EMULATION overdrive: 1.2 V is voltage level and the LDO is set in bypass mode.
- ON: 1.06 V is the voltage reference (default state).

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- SLEEP: 0.83 V is the voltage reference. It is set when the device enters sleep mode.

Section 3.8.5.3, *LDO_WAKEUP Transitions,* presents the state transition conditions and sequences for the LDO_WKUP.

NOTE: The voltage levels associated with the different modes may depend on the device characteristics.

At boot time, the LDO_WAKEUP LDO is started in emulation mode. It is a software command (that is, from OS or ROM code) to set it to a different mode.

3.8.4.3 ABB LDOs Control

The ABB LDO supports two voltage modes:

- Bypass mode: In this mode the x_ABB LDO is bypassed and outputs the VDD_x_L voltages (x refers to MPU and IVA). This mode is activated when FBB is not required, or when voltage domain enters low-power mode.
- FBB mode is enabled when the device is a weak process device at highest OPP.

The information regarding the type of device silicon process (weak, nominal, strong) is stored in eFuse. The eFuse bits values are copied to the PRCM module registers during power-on sequence.

The PRCM module provides PRM_LDO_ABB_MPU_SETUP and PRM_LDO_ABB_IVA_SETUP registers for configuration with the following controls:

- SR2EN – To enable or bypass the ABB power management
- ACTIVE_FBB_SEL – To enable or bypass FBB mode
- SR2_WTCNT_VALUE – LDO settling delay on OPP change. The delay is in number of system clock cycles.

The PRCM module provides PRM_LDO_ABB_MPU_CTRL and PRM_LDO_ABB_IVA_CTRL register for control:

- OPP_SEL – Current operational OPP
- OPP_CHANGE – Initiate an OPP based ABB LDO setting change
- SR2_STATUS – Current mode of operation of ABB LDO
- SR2_IN_TRANSITION – ABB LDO is in transition.

For the ABB LDO state change programming sequence, see Section 3.10.4.2, *Changing OPP*.

3.8.4.4 Bandgap control

Bandgap provides voltage reference for internal LDOs. The PRCM module automatically controls the switching between ON and OFF states of the bandgap, based on the device power state. It is completely transparent to user software.

The PRM_LDO_BANDGAP_CTRL[0] OFF_ENABLE bit controls whether the bandgap remains on or is shut off when the device switches to OFF power state.

3.8.5 Voltage Domain State Transitions

In Section 3.1.1.3.1, *Voltage Domain*, the supported states of a voltage domain were presented. This section describes the trigger conditions to enable and perform sleep and wake-up transitions on PRCM module-controlled voltage domains:

- VDD_MPU_L
- VDD_IVA_L
- VDD_CORE_L
- LDO_MPU_M
- LDO_IVA_M

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- LDO_CORE_M

It also identifies state transition sequences for these voltage domains.

When the voltage domain state transition control is set to automatic, the PRCM module initiates the voltage domain state transition when the required hardware conditions are satisfied. These hardware conditions can be based on the power domain state conditions and/or system clock state conditions. The PRCM module prevents any transition when the associated conditions are not satisfied.

The LDO_MPU_M, LDO_IVA_M, or LDO_CORE_M memory voltage domain is automatically transitioned to the retention level whenever all memory arrays in the domain reach the RETENTION or OFF power state. Similarly, a transition back to the ON state is triggered upon one or more domain memory arrays requiring a transition back to the ON power state.

If a voltage command acknowledgement is not received within an allowed response time window (communications error over the I^2C interface), an error status is logged, a global warm reset is generated, and the transition is skipped.

3.8.5.1 VDD_x_L Transitions

Transition trigger conditions for sleep transition from ON to SLEEP or RETENTION state are:

- Software setting: PRM_VOLTCTRL[a:b] AUTO_CTRL_VDD_x_L = SLEEP (0x1) or RETENTION (0x2)
- Power states conditions:
  - For voltage domain SLEEP state transition – all power domains in the voltage domain must be in ON-INACTIVE, RETENTION, or OFF state.
  - For voltage domain Retention state transition – all power domains in the voltage domain must be in RETENTION or OFF state.
- Clock states conditions: No clock activity on voltage domain

NOTE:

- In case of VDD_CORE_L sleep transition from ON to SLEEP state, the PD_CORE can be either ON-INACTIVE or in RETENTION only.
- In case of VDD_MPU_L and VDD_IVAL sleep transition from ON to SLEEP state, the reference and bypass clocks to their respective DPLLs must also be gated.

Transition trigger conditions for wake-up transition from SLEEP or RETENTION state to ON state is:

- Any wake-up event occurs on the voltage domain.

The State transition sequence:

1. All transition trigger conditions are met.
2. The voltage controller sends an On, SLEEP, or Retention command sequence over the I^2C interface.
3. The PRCM module waits for I^2C command sequence acknowledge.
4. The PRCM module starts the voltage transition counter.
5. When the counter expires, a voltage transition completion state is reached.

3.8.5.2 Memory LDOs Transitions

The transition trigger conditions for on to retention mode are:

- At least one memory bank associated with the LDO is in RETENTION state and the rest of the memory banks may either be in RETENTION or OFF states.

The transition trigger conditions for on/retention mode to off mode transition:

- Device is switching to OFF state.

Transition sequence:

1. Transition trigger conditions are true (that is, satisfied).
2. Switch LDO reference to:

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- Retention mode value if on-to-retention mode transition
- Off mode value if on/retention-to-off mode transition

3. Start counter for LDO stabilization.
4. When counter expires voltage transition completion state is reached.

3.8.5.3 LDO_WAKEUP Transitions

The ON-to-SLEEP transition trigger conditions are:

- Power domain states: Device is in low-power state (STANDBY or OFF state) and PD_EMU power domain is off.
- Clock states: Only the 32K clock is active in CD_WKUP (and system clock is gated at SCRM level)

The SLEEP-to-ON transition trigger conditions are:

- Any device wake-up event other than emulation wake-up event

The EMULATION-to-ON transition trigger conditions are:

- Power domain states: PD_EMU is Off and device is in active mode OR
- Clock states: PD_EMU is Off and any clock other than 32K clock is active in PD_WKUP

The EMULATION-to-SLEEP transition trigger conditions are:

- Power domain states: Device is in low-power state (STANDBY or OFF state) and PD_EMU power domain is off.
- Clock states: Only the 32K clock is active in CD_WKUP (and system clock is gated at SCRM level)

The SLEEP or ON-to-EMULATION transition trigger condition is:

- Any wake-up event on PD_EMU

Transition sequence:

1. Transition trigger conditions are met.
2. LDO_WAKEUP initiates the transition.
3. Starts a counter for LDO_WAKEUP transition.
4. LDO_WAKEUP transition completes.

3.8.6 DVFS

Dynamic voltage and frequency scaling is a technique that can be used on the logic voltage domains (VDD_MPU_L, VDD_IVA-L, and VDD_CORE_L), independently of each other. Upon current or predictive performance request, determined by software according to ad hoc algorithms or heuristics, software can configure the PRCM module to change the OPP of a voltage domain. For an increase of performance, voltage is first raised, and then frequency is increased. For a decrease of performance, frequency is first decreased, and then voltage is dropped.

3.8.6.1 EMIF Clocks Frequency Scaling Constraints

CD_EMIF is inside the PD_CORE. The EMIF subsystem is getting several clocks:

- L3 interface clock
- DLL_CLK clock (that is, DLL clock): For the DLL only
- EMIF_FCLK clock: For external memory access and source of functional clock to EMIF. EMIF_FCLK frequency is DDR_PHY_CLK/2. DDR_PHY_CLK frequency is PHY_ROOT_CLK/2.

L3 interface clock frequency can be changed on the fly without affecting EMIF operations as long as DLL_CLK and PHY_ROOT_CLK clocks are not affected. EMIF has internal asynchronous bridge to handle different interface and functional clocks.

When DDR PHY clock frequency is to be changed, EMIF must be put into IDLE state. This ensures that external memory is in self-refresh mode.

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Similarly, DLL frequency change implies that DLL must relock. It can be done only when EMIF is in IDLE state. Relock time is 400 DLL clock cycles.

The EMIF clocking scheme allows for change of OPP without DLL relock (that is, DLL is clocked by a relatively low frequency supported in all OPPs). Then change of OPP consists only in changing the DDR PHY clock frequency (and eventually L3 interface clock frequency).

NOTE: Software must ensure that no master module tries to access the registers of the EMIF during this sequence.

EMIF clocks control requirements in the PRCM module:

- EMIF clock frequency setting should be done through shadow registers for DLL_CLK and DDR_PHY clocks.
- EMIF clock frequency update bit field should be used to copy shadow register value as current values.
- The PRCM module hardware manages automatic EMIF clock frequency update sequence:
  - Put the EMIF into IDLE state.
  - Upload shadow register values in corresponding current register and wait for new EMIF clocks to be stable.
  - Put the EMIF module back into ACTIVE state

NOTE: The PRCM module should not gate the DLL_CLK and DDR_PHY clocks during automatic EMIF frequency change.

Programming model to perform automatic EMIF frequency change as part or not of an OPP change (DVFS). The automatic EMIF frequency change must always be performed while CD_EMIF is under software-forced wakeup (SW_WKUP).

VDD_CORE_L voltage fixed and only clock frequency switching

Changing EMIF clock frequency without voltage change (example, change of SYS_CLK divider value while DPLL_CORE is in bypass, change of DPLL_CORE mode between bypass and lock)

- Software writes new EMIF timing parameters in shadow registers of the EMIF.
- It then configures the clock selection and frequency setting shadow registers in the PRCM module.
- The PRCM module sends an idle request to the EMIF (overriding the software settings of the MODULEMODE bit field for EMIF).
- EMIF stalls transactions on internal interconnect, completes all committed transaction to the external memory and then puts the external memory in self-refresh mode
- EMIF module then acknowledges the idle request of the PRCM module.
- The PRCM module uploads the values configured in the shadow register bit fields to the corresponding current register bit fields.
- The PRCM module waits for stabilization of the PHY_ROOT_CLK and DLL_CLK clocks through hardware monitoring, according to new settings.
- The PRCM module requests the EMIF to exit idle (stops the overriding of the software settings of the MODULEMODE bit field for EMIF).
- The PRCM module clears the frequency update field.
- The EMIF copies the timing parameter configured in the shadow register as the current values.
- The EMIF acknowledges that the PRCM module is functional, and starts accepting the transactions on the internal interconnect.
- If DLL clock was changed, EMIF waits for DLL to be relocked and transactions on internal interconnect, if required. The PRCM module is not aware of the DLL operations.
- Accesses to SDRAM are serviced again:

  Software execution can be stalled during the frequency change without harm as the critical hardware sequence is performed without software intervention. After having set the frequency update field, software should only poll for its clearing.

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Accesses to external SDRAM are stalled during following duration:

- 2 µs maximum due to EMIF entering and exiting idle
- + 400 DLL clock cycles in case DLL clock frequency has changed.
- + DPLL lock time in case DPLL has been locked.

VDD_CORE_L voltage change for OPP switching

It is assumed that DLL clock frequency is not changed and that the DPLL_CORE mode is not changed and stays locked. Only the DDR_PHY clock frequency is changed using the post divider. L3 clock is likely also changed, but it does not affect the EMIF.

Accesses to external SDRAM must be stalled at maximum during 2 µs due to this sequence.

Voltage scaling up consists of:

Software indicates to EMIF that voltage change operation has started to allow EMIF to ensure regular code updates from DLL masters.

Software disables SmartReflex for core voltage

Software performs direct VDD_CORE setting to new noncorrected value (for weak silicon) and wait for voltage stabilization.

Software configures SmartReflex for corresponding OPP.

Software re-enables SmartReflex for core voltage.

Software indicates to EMIF that voltage change operation is complete and it does not need to control the code update from DLL masters directly.

3.8.6.2 GPMC Clocks Frequency Scaling Constraints

CD_L3_2 is inside the PD_CORE. It supplies the L3_ICLK2 clock to the general-purpose memory controller (GPMC) module, which is used as interface and functional clock. GPMC timing parameters are supposed be programmed at boot for the nominal OPP. Theses timing parameters can be used for lower L3 frequency, at the downside of having slower access to external memory.

External memory connected to GPMC may not support on-the-fly L3 frequency changes. Following is the sequence to perform L3 frequency change as part or not of an OPP change (DVFS).

Hardware-controlled sequence

1. Software writes new L3 clock settings in the shadow register and sets the frequency update field.
2. The PRCM module requests idle to GPMC.
3. GPMC requests disconnection of its interconnect port and completes all outstanding transactions.
4. GPMC acknowledges idle. Any access to GPMC is then stalled.
5. The PRCM module uploads the values of the shadow register bit field in the corresponding current bit field.
6. The PRCM module waits for stabilization of the L3 clocks by monitoring the DPLL_CORE lock and/or divider acknowledge signals according to new settings.
7. The PRCM module clears the frequency update field.
8. The PRCM module requests the GPMC to exit idle.
9. GPMC re-allows interconnect connection and acknowledges it is functional.
10. Accesses to external memory are serviced again.

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NOTE:

- The frequency update field is the same as the one for EMIF clock change. The same hardware in the PRCM module handles the frequency change of L3, DDR_PHY, and DLL clocks.
- If the GPMC supports on-the-fly L3 frequency change, then the CM_SHADOW_FREQ_CONFIG2[0] GPMC_FREQ_UPDATE bit can allow bypassing of the sequence.

Software-controlled sequence

1. Software configures the PRCM module to disable GPMC.
2. The PRCM module requests idle to GPMC.
3. GPMC requests disconnection of its interconnect port and completes all outstanding transactions.
4. GPMC acknowledges idle. Any access to GPMC is then stalled.
5. Software programs the PRCM module to change L3 frequency and wait for L3 stabilization.
6. Software configures the PRCM module to re-enable GPMC.
7. GPMC re-allows interconnect connection and acknowledges it is functional.
8. Accesses to external memory are serviced again.

3.8.6.3 CORE DVFS Versus Subsystem Functionality

3.8.6.3.1 Display Subsystem

The display subsystem is part of the CORE voltage domain. It has internal FIFOs that are sized to sustain a change of OPP on the CORE voltage domain with no DPLL relock and no DLL frequency change. Accesses to external SDRAM are stalled at maximum during 2 µs in these conditions. DSS functional clock is not affected by the change of OPP on CORE voltage domain. Hence, DSS supports on the fly DVFS of the CORE voltage domain, assuming selected OPP remains compatible with the current DSS processing.

3.8.6.3.2 IVAHD

IVAHD is part of the IVA voltage domain. It can sustain a temporary stall of external SDRAM accesses because it is not real-time processing. IVAHD functional clock is not affected by the change of OPP on the CORE voltage domain; therefore, IVAHD supports on-the-fly DVFS of the CORE voltage domain.

3.8.6.3.3 Imaging Subsystem

The Imaging subsystem (ISS) is part of the CORE voltage domain. It is real-time processing (or data flow). It cannot support a 2-µs stall of external SDRAM access, due to the heavy data throughput (FIFO size increase is prohibitive). As a consequence, ISS does not support on-the-fly change of OPP on CORE voltage domain. However, the CORE DVFS can be synchronized to the interframe idle window of ISS. During this window, ISS does not initiate transaction to external SDRAM. Core OPP can be changed safely assuming selected OPP remains compatible with the current ISS processing. ISS functional clock frequency can either remain unchanged, or be scaled according to the OPP change, assuming is remains compatible with the current ISS processing. This is the responsibility of software.

Example: CORE OPP change OPP50→OPP100, with functional clock frequency unchanged – OPP is 50%, ISS functional clock is at 50 MHz, clock coming from CORE DPLL, ISS clock divider is set to 4

Software performs OPP change: OPP50→OPP100, – ISS is now at 100 MHz – SW sets the ISS clock divider to 8. - ISS functional clock is back at 50 MHz

3.8.6.4 DVFS Voting Mechanism (VDD_CORE_L and VDD_IVA_L Voltage Domains)

3.8.6.4.1 CORE OPP Voting Architecture

Core voltage domain operating point can be determined based on the following system masters:

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- APE DSP processor
- APE Cortex-M3 MPU processor
- Modem

The PRCM module provides:

- Four read/write voting registers (that is, CM_CORE_DVFS_PERFn, where n = 1 to 4). Software can use these, to specify the performance level of the CORE voltage domain as requested by each system master (likely EMIF bandwidth only). Software must encode the bit fields; encoding is not interpreted by hardware.
- One read/write register (that is, CM_CORE_DVFS_CURRENT) to identify the current CORE voltage domain OPP setting. Software must configure this register based on current OPP setting of the register. It is not managed by hardware.

See Section 3.8.6.4.3, *Voting Mechanism*, to understand the voting mechanism for DVFS on the voltage domain.

3.8.6.4.2 IVA OPP Voting Architecture

IVA voltage domain operating point can be determined based on the following subsystems performing different type of processing:

- DSP processor
- IVAHD accelerator
- ABE

The PRCM module provides:

- A read/write voting register (that is, CM_IVA_DVFS_PERF_Subsystem name) for each subsystem. Software can use these, to specify the performance level of the IVA voltage domain as requested by each subsystem. Software must encode the bit fields; encoding is not interpreted by hardware.
- One read/write register, that is, CM_IVA_DVFS_CURRENT, to identify the current IVA voltage domain OPP setting. It is again the software's responsibility to configure this register based on current OPP setting of the register. It is not managed by hardware.

See Section 3.8.6.4.3, *Voting Mechanism*, to understand the voting mechanism for DVFS on the voltage domain.

3.8.6.4.3 Voting Mechanism

The operating point change for the CORE and IVA voltage domains can be performed by the respective masters or subsystems by executing the following steps:

1. Obtain ownership of the voltage domain DVFS semaphore using the SPINLOCK module.
2. Write new performance requirement value in its voting register.
3. Read the current OPP and the voting registers.
4. Compute the result of the voting using ad hoc algorithm (for example, sum of performance requirements).
5. If the current OPP does not match the voting result (that is, either the OPP must be decreased in case of low performance demand, or the OPP must be increased in case of high performance demand) then the system master performs voltage domain OPP change to best match the voting result.
6. When change of OPP is completed, update the current voltage domain OPP register accordingly.
7. Release the voltage domain DVFS semaphore, using the SPINLOCK module.

3.9 Device Low-Power States

The device low-power states are the result of any valid combination of power domain states in which all the power domains are no longer in the ACTIVE state. In such a situation the PRCM module hardware can trigger events to further lower the consumption of the device and the system.

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Typically, the PRCM module can lower or even turn off the SMPS, shut down the system clock supplier, and allow the external power IC to turn off its internal resources.

These device low-power states are characterized by the system power consumption, the wake-up latency, and the required functionality.

The low-power states are:

- RETENTION: All the logic voltage domain (VDD_IVA_L and VDD_CORE_L) are in Retention state
- OFF: All the logic voltage domains are in Off state
- LOW POWER: Any combination of logic voltage domains states (ON, SLEEP, and RETENTION state), other than those identified above.

Once the PRCM module hardware detects any valid combination of power domain state and if a proper programming model of the PRCM module has been set, the PRCM module automatically triggers the transition into the device low-power mode.

3.9.1 Device Wake-Up Source Summary

Each power domain in the device may contain modules that can generate the wake-up events. However, when the device is in OFF power state and all the logic voltage domains are off, only the modules with wake-up capability and that are in the PD_WKUP power domain can generate the wake-up event. Modules in the other power domains require that their voltage domain be in RETENTION, SLEEP, or ON state to generate a wake-up event. Some modules may have a further constraint that their power domain should be ON-INACTIVE or in CSWR RETENTION state to generate the wake-up event.

The wake-up events can be asynchronous or synchronous. Synchronous wake-up events require the 32-kHz clock or the system clock to be active, while asynchronous wake-up events do not require any active clock.

The Modules Attributes subsection of each clock domain in Section 3.6, *Clock Management Functional Description*, presents the wake-up capability support for each module of the corresponding power domain.

3.9.2 Device RETENTION State Management

In Retention state, the voltages to the device are lowered to their minimum value to retain only the logic build with RFFs, while all DFF logic is lost. The memory area may be retained, depending on software configuration.

The device integrates enhanced device wake-up management while in Retention state. This allows:

- Triggering wake-up with limited capabilities from almost all programmed input pads all around the device.
- Triggering wake-up with full capabilities by using few GPIO inputs in the PD_WKUP power domain.

The logic voltages VDD_CORE_L, VDD_MPU_L, and VDD_IVA_L can transition to their retention value independently. Once the voltage domain state transition conditions are met in compliance with the software configuration, the PRCM module hardware initiates the transition into Retention state by sending an I^2C command for the corresponding SMPS.

When all the logic voltages are transitioned to their Retention state, the PRCM module hardware can, depending on a software configuration, toggle its system clock request and/or its power request to allow the SCRM to shut down the system clock source and to request the external power IC to shut down internal resources.

The PRCM module, SCRM, and the external power IC can also be programmed so that the voltage VDD_CORE_L is managed by the power request signal. This means the following:

- The power IC manages the ramp-down and ramp-up time of the VDD_CORE_L SMPS upon toggle of the power request.
- The SCRM accounts for the overall setup of the PMIC resources (internal PMIC resources and VDD_CORE_L SMPS).
- The PRCM module sends Retention and On commands through the I^2C interface. Indeed, the retention voltage value must be equal to the current voltage value and the value of the On voltage must be set to the expected voltage value following the wakeup. Also, the setup time periods corresponding to the

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SMPS ramp-up and ramp-down must be set to a zero value.

3.9.3 Device OFF State Management

The off mode is the device mode where all power domains except for PD_WKUP are in OFF state and the logic voltage domains (VDD_MPU_L, VDD_IVA_L and VDD_CORE_L) are shut down by the external power IC. Other power sources, such as the DPLL supplies, can be shut down by the external power IC during the off mode period.

The device integrates enhanced device wake-up management while in Retention state. This allows:

- Saving I/Os leakage by settings pads in the lowest power state compatible with the device environment.
- Triggering wake-up with limited capabilities from almost all programmed input pads all around the device.
- Triggering wake-up with full capabilities by using few GPIO inputs in the PD_WKUP power domain.

This section details the way the PRM manages and sequences the control of the various off mode contributors:

- LDO_WAKEUP
- Memory LDOs
- ABB LDOs
- Voltage controller
- Hardware save-and-restore mechanism
- Hardware power request signal

NOTE: For more information about the save-and-restore mechanism, see Section 16.4.21, *Auto-Restore Feature*, in Chapter 16.

Once the hardware conditions is met and according to the software configuration the PRCM module hardware initiates the transition into off mode by sending I^2C commands for each SMPS and by respecting required sequencing between the voltage domains.

When all the logic voltages are transitioned to their Retention state, the PRCM module hardware can, depending on a software configuration, toggle its system clock request and/or its power request to allow the SCRM to shut down the system clock source and to request the external power IC to shut down internal resources.

The PRCM module, SCRM and the external power IC can also be programmed so that the voltage VDD_CORE_L is managed by the power request signal. This means the following:

- The power IC manages the ramp-down and ramp-up time of the VDD_CORE_L SMPS upon toggle of the power request.
- The SCRM accounts for the overall setup of the PMIC resources (internal PMIC resources and VDD_CORE_L SMPS).
- The PRCM module sends Off and On commands through the I^2C interface. Indeed, the Off voltage value must be equal to the current voltage value and the value of the On voltage must be set to the expected voltage value following the wakeup. Also, the setup time periods corresponding to the SMPS ramp-up and ramp-down shall be set to a zero value.

3.9.3.1 Device Off Mode Sleep Sequence

This section describes the main steps of the device off mode sleep sequence. The Off command to shut down the voltages VDD_MPU_L, VDD_IVA_L, and VDD_CORE_L can be sent through the I^2C interface. The VDD_CORE_L may also be controlled independently using the power request signal.

NOTE: The power request signal can be used to turn off other resources of the power-management IC, even when it is not used for the VDD_CORE_L management.

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NOTE: LDOs in the power companion device (TWL60xx), which are turned off in ACTIVE state, are switched on when entering into SLEEP state with the default value.

After the first power on, all resources must be configured, especially the power resources that are not part of the power-up sequence. This must be done by sending a command through the I^2C interface.

1. Software has completed preliminary settings such as:
   - Settings in the external power IC
   - Voltage transition settling time settings in PRCM
   - Context save for the relevant modules
   - System control module is configured with valid I/O pads off mode configuration.
   - Enable/disable the wake-up feature for each pad by programming the system control module.
   - Enable/disable the automatic gating of the system clock (PRCM).
   - Enable the I/O wake-up scheme (PRCM).
   - Program a consistent power state for each power domain (that is, Off state for domains without hardware restored modules and OSWR state for domains with hardware restored modules build with RFF logic).
   - All modules in the PD_WKUP power domain must have their interrupts to Cortex-M3 and DSP, and their DMA requests to sDMA disabled.
   - Program automatic transition of the CD_WKUP clock domain.
   - Enable the off mode scheme (PRCM).
   - Configure the VDD_CORE_L management option:
     – Disable the option if power request signal is not used for VDD_CORE_L management.
     – Enable the option if power request signal is used for VDD_CORE_L management.
2. The PRCM module initiates the transition into off mode upon all following conditions:
   - All the programmable power domains have reached their targeted Low-Power state which can either be Off or OSWRET. It does not apply to always-on power domains and to the EMU power domain.
   - The CD_WKUP clock domain is idled.
   - The off mode has been enabled by software.

   At this stage the I/O wake-up scheme through the I/O pad daisy-chain is already enabled. The I/O isolation scheme is managed in parallel with the following sequence (see Section 3.9.4, *I/O Management*).
3. The PRCM module triggers in parallel:
   - Switch off all SRAM LDOs.
   - Bypass all ABB LDOs.
   - Isolate the analog area from digital supply removal.
4. The PRCM module then sends in a row the Off command for the voltages VDD_IVA_L and the VDD_MPU_L, once the following conditions are met:
   - I/O isolation scheme is complete.
   - SRAM LDOs have ramped down to 0 V.
   - ABB LDOs have switched in bypass.

   The order between the two Off commands is irrelevant and managed by the voltage controller.
5. Once the voltages VDD_IVA_L and VDD_MPU_L are ramped down to 0 V the PRCM module sends the Off command for the voltage VDD_CORE_L:
   - If power request signal is not used for VDD_CORE_L management then the VDD_CORE_L is ramped down to 0 V.
   - If power request signal is used for VDD_CORE_L management then the Off command for the voltage VDD_CORE_L, through the I^2C interface, has no effect and the voltage VDD_CORE_L

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remains unchanged.

6. Once the Off command for VDD_CORE_L is sent and acknowledged, the PRCM module gates locally its system clock.
7. The PRCM module then deassert the signal system clock request to the SCRM, if so configured by the software. Similarly, it deasserts the signal power request if configured by software.
   - If power request signal is used for VDD_CORE_L management, then VDD_CORE_L is ramped down to 0 V.
8. The SCRM then acknowledges the power request to the PRCM module. This acknowledge is required by the PRCM module before toggling again the signal power request.
9. The SCRM informs the PRCM module that all versions of the system clock have been gated; hence the PRCM module can transition the LDO_WAKEUP to SLEEP state if the PD_EMU power domain is in OFF state.
10. The DEVICE_OFFWKUP_CORERSTACTST signal intended for the core control module is asserted. The EMIF1_DEVICE_OFFWKUP_CORERSTACTST and EMIF2_DEVICE_OFFWKUP_CORERSTACTST signals intended for EMIF1 and EMIF2, respectively, are asserted according to their associated register bit fields, EMIF1_OFFWKUP_DISABLE and EMIF1_OFFWKUP_DISABLE.

3.9.3.2 Device Off Mode Wake-Up Sequences

The wake-up sequence includes a phase of hardware restore. Depending on the wake-up event source the restore sequence completes in one or two phases. The first phase always happens and is sufficient to serve some type of wake-up events; for other sources of event a second phase is required and occurs immediately after the first phase. Phase 2 is also split into two subphases (phase 2a and phase 2b). The device returns to off mode after the first phase completes.

Table 3-299 lists the device off wake-up and hardware restore phases.

Table 3-299. Device Off Wake-Up and Hardware Restore Phases

Wake-Up Event	Phase 1	Phase 2	Comment
Wake-up request from PD_WKUP	Yes	Yes	This event must wake up the PD_MPU power domain by dependency.
PRM interrupt toward MPU-A9 (includes I/O wake-up detection)	Yes	Yes	This event wakes up the PD_WKUP power domain. The PD_MPU power domain is woken up by broadcast of the wake-up event and the MPU-A9 boots up.
Global warm reset	Yes	No	After voltage stabilization, phase 1 restoration is performed. Then MPU-A9 reboots, because global warm reset is a source of PD_MPU power domain wakeup.

3.9.3.2.1 Wake Up From a Wake-Up Event

This section describes the main steps of the wake-up sequence to exit the device from off mode. The ON command to ramp-up the voltages VDD_MPU_L, VDD_IVA_L, and VDD_CORE_L can be sent through the I^2C interface. VDD_CORE_L can also be controlled independently using the power request signal.

NOTE: The power request signal can be used to turn on other resources of the power-management IC, even when it is not used for the VDD_CORE_L management.

Additionally it is assumed in this sequence that the wake-up source is not a global warm reset.

1. The PRCM module switches the LDO_WAKEUP from SLEEP to ON state and waits for the setup time of the LDO_WAKEUP (that is, four clock cycles of the 32-kHz clock).
2. The PRCM module asserts the system clock request signal to SCRM, which in turn sends the request to the external power IC. The SCRM accounts for the system clock stabilization time before enabling the clock to the PRCM module.
3. The PRCM module also asserts the power request signal to the SCRM. The PRCM module waits for the acknowledge of its power request signal and activation of the system clock before sending an I^2C

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command for the voltage ramp-up sequence.

- If power request signal is used for VDD_CORE_L management, then the power-management IC ramps up the voltage VDD_CORE_L.
- If power request signal is not used for VDD_CORE_L management, then the voltage VDD_CORE_L is unchanged.

4. The PRCM module sends the ON command for the VDD_CORE_L voltage ramp up, through the I^2C interface and waits for the setup time of the SMPS.
   - If power request signal is used for VDD_CORE_L management, then the voltage VDD_CORE_L is unchanged.
   - If power request signal is not used for VDD_CORE_L management, then the power-management IC ramps up the voltage VDD_CORE_L.
5. The PRCM module sends in a row the ON commands for the voltages VDD_MPU_L and VDD_IVA_L and waits for the setup time of the two SMPS.
6. The PRCM module enables the system clock to the eFuse controller and releases its reset line. It holds the other asserted resets until completion of the EFUSE bits sensing.
7. The PRCM module waits for the stabilization of the bandgap, memory LDOs and ABB LDOs stabilization.
8. Hardware restore phase 1 starts:

   (a) The PRCM module ensures that:
   - CORTEXA9, CORTEXM3, and DSP are held in reset.
   - C2C is kept in STANDBY state.
   - sDMA receives the restore request.
   - Phase 1 descriptor start address is sent to the sDMA.
   - MODULEMODE bit field of the L3_3 module is overridden to auto mode. This ensures the successful restoration of its firewalls during phase 1 of the restore.

   (b) The PRCM module generates a wake-up event on the CD_SDMA clock domain. As a result, the PD_CORE power domain and CD_SDMA wakeup. This causes the CD_L3_1, CD_L3_2, CD_L4_CFG, CD_MEMIF, CD_L4_PER, and CD_L3_INIT to wake up because of the wake-up broadcast due to static dependency and their respective reset are released once their clock is active. The clock domain L4_WKUP is woken up (due to a wake-up broadcast on static dependency).

   (c) The sDMA switches from STANDBY to ACTIVE state and performs phase 1 of the hardware restore:
   - Firewalls
   - System control module
   - EMIF
   - Part of the CM1 and part of the CM2 (core clock configuration, registers CLKTRCTRL of the CD_MPU, CD_L3_1, CD_L3_2, CD_L4_CFG, CD_MEMIF, CD_L4_PER, and CD_L3_INIT clock domains)

   The sDMA make the last write into the PRCM module end of phase 1 bit field. The PRCM module then switches it to STANDBY state and resets it.

   (d) The PRCM module releases I/O isolation of the EMIF. The other I/Os stay isolated.

   (e) The PRCM module checks and waits if necessary for the DPLL_CORE to be in a stable state.

   (f) In parallel the PRCM module does the following:
   - Release the condition preventing C2C to remain in STANDBY state
   - Release the override of the MODULEMODE bit field of the L3_3 module
9. Upon a need to perform phase 2 of the hardware automatic restore (according to the wake-up source), the following sequence occurs:

   (a) Phase 2a sequence.

   (i) The PRCM module drives the phase 2a descriptor start address to the sDMA.

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(ii) The PRCM module releases the sDMA from reset.

(iii) The PRCM module generates a wake-up event on the CD_SDMA clock domain (same as in Step 2 of phase 1).

(iv) The sDMA performs phase 2a of the hardware restore:

- The MODULEMODE bit field of each module to be restored during phase 2b is set to Enabled or Auto and the SARMODE bit field is enable if applicable. Only modules that have just interface clock(s) can be restored automatically.
- Register CM_SDMA_STATICDEP is set to enable all necessary static dependency To wake up all power domains having modules to be restored during phase 2b

The sDMA makes the last write into the PRCM module at the end of phase 2a bit field. The PRCM module then switches it to Standby state and resets it. This completes phase 2a.

(b) Phase 2b sequence.

(i) The PRCM module drives the phase 2b descriptor start address to the sDMA.

(ii) The PRCM module releases the sDMA from reset.

(iii) The PRCM module generates a wake-up event on the CD_SDMA clock domain (same as in Step 2 of phase 1).

(iv) The sDMA performs phase 2b of the hardware restore:

- Restore of the relevant modules

The sDMA makes the last write into the PRCM module at the end of the phase 2b bit field. The PRCM module then switches it to STANDBY state and resets it. This completes phase 2b.

10. The PRCM module releases I/O isolation of the remaining I/O, only if the PRM_IO_PMCTRL.ISOOVR_EXTEND bit field is not set.
11. The PRCM module releases the reset stall conditions holding CORTEXA9, CORTEXM3, and DSP in reset.
12. The PD_MPU power domain is woken up if required according to the wake-up source.

3.9.3.2.2 Wakeup Upon Global Warm Reset

When global warm reset is the source of the device wakeup, the sequence referred in Section 3.9.3.2.1, *Wake up From a Wake-Up Event*, is modified as follows:

Steps 4 and 5 are replaced by:

- The PRCM module waits for the three voltages VDD_MPU_L, VDD_IVA_L, and VDD_CORE_L stabilization time. It uses the PRM_VOLTSETUP_WARMRESET register for that purpose.

Step 6 is replaced by:

- The PRCM module enables the system clock to the eFuse controller and releases its reset line. In parallel, the device reset manager counts for global reset extension (setup by the PRM_RSTTIME[9:0] RSTTIME1 bit field). The PRCM module holds the other asserted resets until completion of the eFuse bits sensing and the global reset counter overflow.

Phase 2 of the hardware restore sequence is skipped.

The hardware blocks and modifies the FREQ_UPDATE bit field of CM_SHADOW_FREQ_CONFIG1 register during phase 1.

3.9.3.3 Global Warm Reset During a Device Wake-Up Sequence

If a global warm reset occurs before the PRCM module completes voltage stabilization count, the global warm reset is applied immediately. As a consequence, the sequence described in Section 3.9.3.2.2, *Wake up Upon Global Warm Reset*, is performed.

If the global warm reset occurs after the PRCM module completes voltage stabilization (during eFuse sensing or during phase 1 of automatic restore):

- Global warm reset is delayed and applied after of phase 1 restore completes.
- Phase 2 of restore is discarded.

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- MPU boots after the warm reset sequence completes.

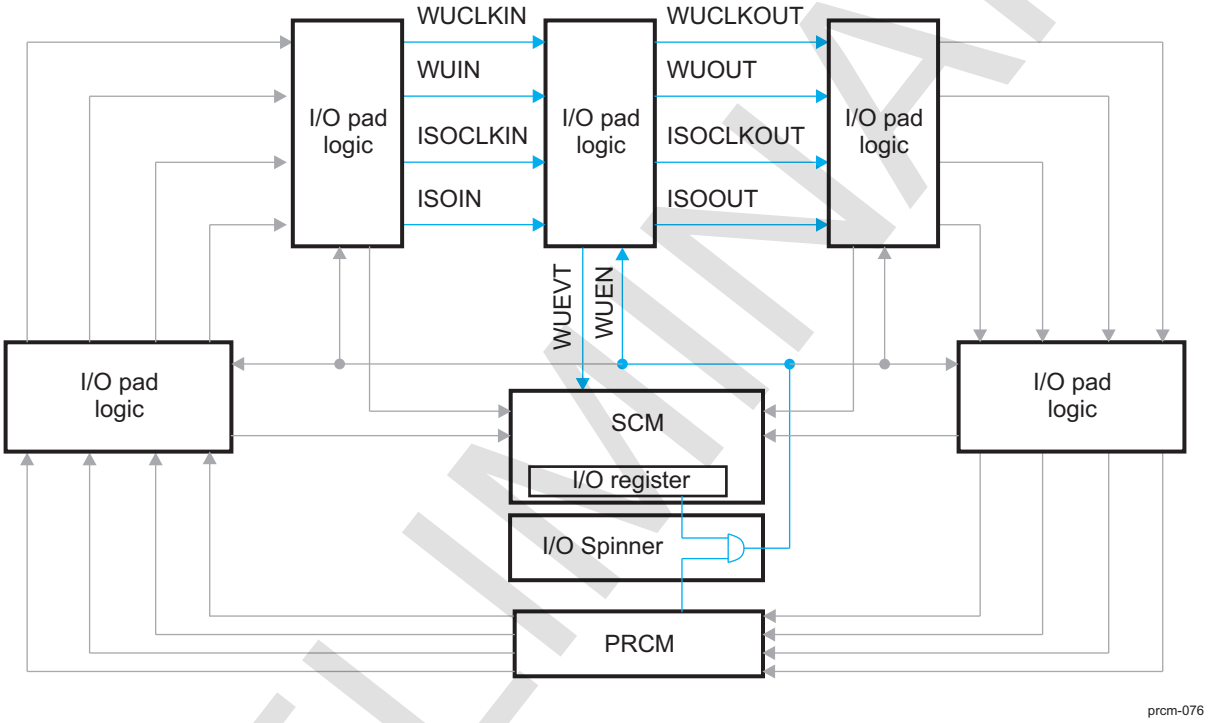
If the global warm reset occurs during phase 2 of automatic restore:

- Global warm reset is applied immediately.
- Phase 2 of restore is discarded.
- MPU boots after the warm reset sequence completes.

3.9.4 I/O Management

Figure 3-80 is an overview of the power-management modules and their internal connections with a generic power domain.

Figure 3-80. I/O Pads Daisy-Chain Configuration



Any I/O pad of the device can be configured to generate a wake-up event when the device is in off mode. This is managed by the configurations in the system control module and the PRM.

In the off mode, the I/O pads of the device form a daisy chain with the I/O pad logic output of one pad connected to the I/O pad logic input of the next one. The I/O pad logic at the two ends of the chain is connected to the PRM.

The I/O pad wake-up scheme must be enabled (WUEN signal) globally by setting the PRM_IO_PMCTRL[16] GLOBAL_WUEN bit and by also setting I/O pad wake-up enabled/disabled individually (WUEN signal) by writing to the following bit fields in the control module:

- CONTROL.CONTROL_(CORE/WKUP)_PAD0_X_PAD1_Y [14] WAKEUPENABLE
- CONTROL.CONTROL_(CORE/WKUP)_PAD0_X_PAD1_Y [30] WAKEUPENABLE

Once configured, the wake-up scheme within each I/O pad is enabled and disabled by triggering a control (WUCLKIN signal) of the I/O daisy chain. This is done thanks to a dedicated PRCM module register bit PRM_IO_PMCTRL[8] WUCLK_CTRL. The software must enable the I/O wakeup prior entering a low-power mode and disable it following a wake-up event.

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Writing the PRM_IO_PMCTRL[8] WUCLK_CTRL bit to 1 asserts signal WUCLKIN high to reset spurious wake-up event and to latch the current pad input value. PRCM module register PRM_IO_PMCTRL[9] WUCLK_STATUS logs the signal WUCLKOUT of the last pad of the I/O ring. Once this status is set to 1, the software may clear the PRM_IO_PMCTRL[8] WUCLK_CTRL bit to effectively enable or disable the wake-up feature within each pad.

Additionally, it is required that the WUCLKIN is forced to 1 during global power-on reset. The I/O wake-up feature is enabled or disabled depending on a control (WUEN) for each I/O pad. This control is generated by the Spinner logic resulting of the combination of a local enable/disable bit per pad located in the control module and a global enable/disable bit located in the PRCM module, that is, PRM_IO_PMCTRL[16] GLOBAL_WUEN.

When a wake-up event is detected by a wake-up enabled I/O pad in the daisy chain, it is logged within the I/O and is conveyed to the system control module (WUEVT signal). All the I/O wake-up event statuses are mapped on memory-mapped registers in the system control module.

When the device wakes up, the MPU can determine all sources of the current wake-up event logged into the corresponding bit fields in the control module.

- CONTROL.CONTROL_(CORE/WKUP)_PAD0_X_PAD1_Y [15] WAKEUPEVENT
- CONTROL.CONTROL_(CORE/WKUP)_PAD0_X_PAD1_Y [31] WAKEUPEVENT

For information about the control module, see Chapter 18, *Control Module*.

I/Os have two associated buffers, that is, 1.2 V and 1.8 V. A software configuration determines which one is used in normal operation. However, in the device off mode, the 1.2-V buffer is always disabled, and the 1.8-V buffer stays on but is powered by 1.2 V instead of 1.8 V to minimize leakage, if pad configure to drive the output.

3.9.4.1 Hardware-Controlled I/O Isolation Sequences

I/Os have two buffers: 1.2 V and 1.8 V.

The software configuration determines whether the 1.2-V buffer or the 1.8-V buffer is used. Regardless of the buffer used, in off mode the 1.2-V buffer is always disabled and the 1.8-V buffer stays on but is powered by 1.2 V instead of 1.8 V to minimize leakage (if the pad is configure to drive the output).

In addition to this, I/Os support the following features:

- Wake-up override: The PRCM module can control the I/Os that are wakened; that is, brought out of isolation from device off mode based on the source of wakeup. The primary application of this feature is to restore only the minimal context of the device for access to EMIF upon C2C request.
- Wakeup phased wakeup: The I/Os support a phased wake-up approach; that is, the I/Os can be brought out of off mode isolation in two phases without affecting the functional operation of the I/Os already out of isolation. This feature is used to wake up the I/Os still held in isolation without affecting the EMIF operations when a full device wakeup is requested.

The I/O transitions are:

- Full on to full isolation: Pad output controls are stable (A, GZ). Pad off mode configuration is activated.
- Full Isolation to EMIF on: EMIF I/O interface is brought out of isolation. Partial device context is restored.
- EMIF on to full on: EMIF I/O interface are already out of isolation and a new wake-up event requires a full device wakeup.
- EMIF on to full Isolation: EMIF I/O interface and some nonrestore sensitive I/Os are already out of isolation. The PRCM module puts the device back in off mode.

3.9.4.2 Software-Controlled I/O Isolation

In addition to the hardware-controlled I/O transitions, there is a dedicated PRCM module register bit, PRM_IO_PMCTRL[0] ISOCLK_OVERRIDE, that can be used by the software to force ISOCLKIN signal to the I/O pad. It is then propagated from one pad to the other in the wake-up enabled daisy chain of I/Os. The PRCM module register PRM_IO_PMCTR[1] ISOCLK_STATUS logs the signal ISOCLKOUT of the last pad of the I/O daisy chain.

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NOTE: Override is used at boot time only when software needs to change the mode of an I/O from 1.8-V default mode to 1.2-V mode. When not overridden, this signal is controlled only by hardware.

PRM_IO_PMCTRL[4] ISOOVR_EXTEND bit allows extending the non-EMIF I/O isolation. This feature can be used by software to restore modules driving output such as GPIO while non-EMIF I/Os are still isolated. Once software completes the relevant module restore, it clears the bit and hardware performs the full-isolation-to-EMIF transition on hardware-controlled I/O transition.

The PRM_IO_PMCTRL[5] IO_ON_STATUS status bit is available for software to check completion of the EMIF on transition.

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3.10 PRCM Module Programming Guide

3.10.1 DPLLs Low-Level Programming Models

This section covers the low-level hardware programming sequences for configuration and use of the module.

3.10.1.1 Global Initialization

3.10.1.1.1 Surrounding Module Global Initialization

This section identifies the requirements of initializing the surrounding modules when the module is to be used for the first time after a device reset. This initialization of surrounding modules is based on the integration and environment of the DPLLs.

Table 3-300 shows the global initialization of the surrounding modules.

Table 3-300. Global Initialization of Surrounding Modules

Surrounding Modules	Comments
PRCM	Ensure that the DPLL reference clock (gated version of system clock) is active.

3.10.1.1.2 DPLL Global Initialization

3.10.1.1.2.1 Main Sequence – DPLL Global Initialization

This procedure initializes the DPLL after a power-on or software reset and then locks it to the desired synthesized clock frequency.

Table 3-301. DPLL Global Initialization

Step	Register/Bit Field/Programming Model	Value
Configure SSC parameters	See Section 3.10.1.1.2.2.	
Configure Recalibration parameters	See Section 3.10.1.1.2.3.	
Set DPLL automatic idle mode	CM_AUTOIDLE_DPLL name[2:0] AUTO_DPLL_MODE	xx(1)
Configure synthesized clock parameters	See Section 3.10.1.1.2.4.	
Configure output clocks parameters	See Section 3.10.1.1.2.5.	
Lock DPLL	CM_CLKMODE_DPLL name[0] DPLL_EN	0x7

(1) It depends on the desired auto idle mode. See Section 3.6.3.3.3, *DPLL Power Modes*.

3.10.1.1.2.2 Subsequence – SSC Parameter Configuration

This procedure configures the SSC parameters for the DPLL and enables the SSC feature.

Table 3-302. DPLL SSC Parameter Configuration

Step	Register/Bit Field/Programming Model	Value
Configure M Step Size	CM_SSC_DELTAMSTEP_DPLL name[19:0] DELTAMSTEP	xx(1)
Configure modulation frequency divider exponent part	CM_SSC_MODFREQDIV_DPLL name[10:8] MODFREQDIV_EXPONENT	xx(1)
Configure modulation frequency divider mantissa part	CM_SSC_MODFREQDIV_DPLL name[6:0] MODFREQDIV_MANTISSA	xx(1)
Enable/disable frequency downspread	CM_CLKMODE_DPLL name[14] DPLL_SSC_DOWNSPREAD	xx(2)
Enable SSC feature	CM_CLKMODE_DPLL name[12] DPLL_SSC_EN	0x1

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Table 3-302. DPLL SSC Parameter Configuration (continued)

Step	Register/Bit Field/Programming Model	Value
Wait until SSC start acknowledge	CM_CLKMODE_DPLL name[13] DPLL_SSC_ACK	0x1

(1) See SSC description in Section 3.6.3.3.5, *DPLL Spread Spectrum Clocking*.

(2) The selected value depends on the desired SSC feature settings.

3.10.1.1.2.3 Subsequence – Recalibration Parameter Configuration

This procedure enables the recalibration feature and the associated processor interrupt flag.

Table 3-303. DPLL Recalibration Parameter Configuration

Step	Register/Bit Field/Programming Model	Value
Clear recalibration interrupt status	PRM_IRQSTATUS _Processor name[x] DPLL name_RECAL_ST	0x0
Unmask recalibration interrupt flag	PRM_IRQENABLE _Processor name[x] DPLL name_RECAL_EN	0x1
Enable recalibration feature	CM_CLKMODE_DPLL name[8] DPLL_DRIFTGUARD_EN	0x1

3.10.1.1.2.4 Subsequence – Synthesized Clock Parameter Configuration

This procedure configures the settings for the synthesized clock of the DPLL.

Table 3-304. DPLL Synthesized Clock Parameter Configuration

Step	Register/Bit Field/Programming Model	Value
Set DPLL clock synthesis multiplier	CM_CLKSEL_DPLL name[2:0] DPLL_MULT	xx(1)
Set DPLL clock synthesis divider	CM_CLKSEL_DPLL name[2:0] DPLL_DIV	xx(1)
IF : Low-power mode operation conditions satisfied?	Software test condition. See Section 3.6.3.3.2.	
Enable DPLL low-power operation mode	CM_CLKMODE_DPLL name[10] DPLL_LPMODE_EN	0x1
ENDIF		

(1) It depends on the desired synthesized clock frequency. See Section 3.6.3.3, *Generic DPLL Overview*.

3.10.1.1.2.5 Subsequence – Output Clock Parameter Configuration

This procedure configures the settings for the output clocks of the DPLL.

Table 3-305. DPLL Output Clock Parameter Configuration

Step	Register/Bit Field/Programming Model	Value
Set output clock dividers (that is, M2, M3 and Mn), where n is from 4 to 7. It depends on the available clock output of the DPLL.	CM_DIV_M2_DPLL name[4:0] DPLL_CLKOUT_DIV CM_DIV_M3_DPLL name[4:0] DPLL_CLKOUTHIF_DIV CM_DIV_Mn_DPLL name[4:0] HSDIVIDER_CLKOUTn-3_DIV	xx(1)
Wait until divider change acknowledged	CM_DIV_M2_DPLL name[5] DPLL_CLKOUT_DIVCHACK CM_DIV_M3_DPLL name[5] DPLL_CLKOUTHIF_DIVCHACK CM_DIV_Mn_DPLL name[5] HSDIVIDER_CLKOUTn-3_DIVCHACK	Bit toggled (2)

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Table 3-305. DPLL Output Clock Parameter Configuration (continued)

Step	Register/Bit Field/Programming Model	Value
Enable/disable output clock dividers auto power-down feature. It applies to M2, M3, and Mn dividers, where n is from 4 to 7. It depends on the available clock output dividers of the DPLL.	CM_DIV_M2_DPLL name[12] DPLL_M2_PWDN CM_DIV_M3_DPLL name[12] DPLL_CLKOUTHIF_PWDN CM_DIV_Mn_DPLL name[12] HSDIVIDER_CLKOUTn-3_PWDN	xx(3)
Enable/disable output clocks automatic gating feature. It applies to M2, M3, and Mn clock outputs, where n is from 4 to 7. It depends on the available clock output of the DPLL.	CM_DIV_M2_DPLL name[8] DPLL_CLKOUT_GATE_CTRL CM_DIV_M3_DPLL name[8] DPLL_CLKOUTHIF_GATE_CTRL CM_DIV_Mn_DPLL name[8] HSDIVIDER_CLKOUTn-3_GATE_CTRL	xx(4)

(1) It depends on the desired output clock frequency. See Section 3.6.3.3, *Generic DPLL Overview*.

(2) It is toggled only if the programmed divider value differs from the previous one.

(3) It depends on whether output clock divider automatic power down feature is to be enabled or not. See Section 3.6.3.3.6, *DPLL Output Power-Down*.

(4) It depends on whether output clock automatic gating feature is to be enabled or not.

3.10.1.2 DPLL Output Frequency Change

Figure 3-81 shows the DPLL output-frequency change.

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Figure 3-81. DPLL Output-Frequency Change

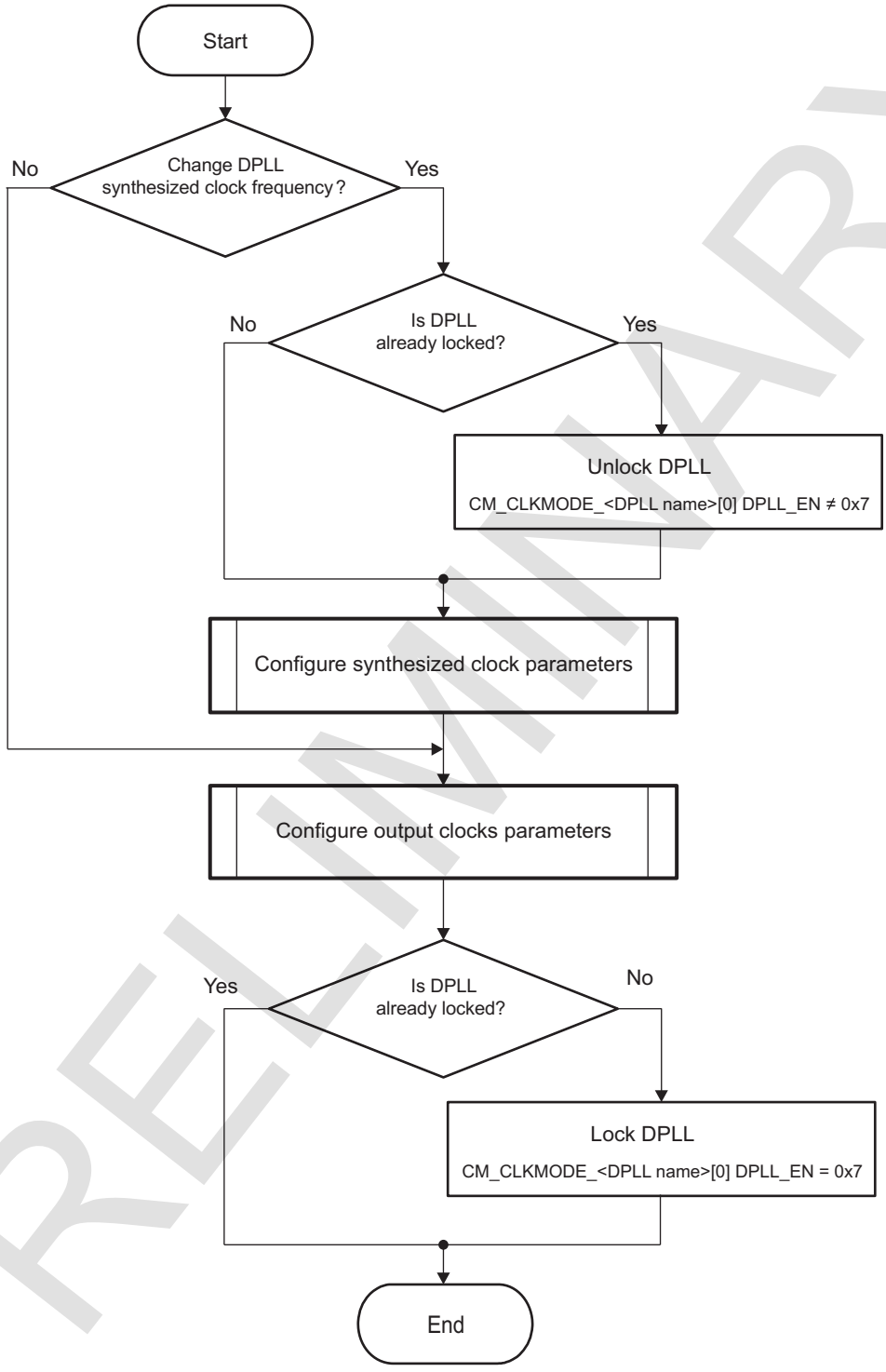

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Table 3-306. Register Call Summary for Sequence – DPLL Output Frequency Change

Register Name
CM_CLKMODE_DPLL name

Table 3-307. Subprocess Call Summary for Sequence – DPLL Output Frequency Change

Subprocess Name	Cross-reference
Configure synthesized clock parameters	See Section 3.10.1.1.2.4.
Configure output clocks parameters	See Section 3.10.1.1.2.5.

3.10.2 Clock Management Low-Level Programming Models

This section covers the low-level hardware programming sequences for configuration and use of the clocks in the device.

3.10.2.1 Global Initialization

3.10.2.1.1 Surrounding Module Global Initialization

This section identifies the requirements of initializing the surrounding modules when the module is to be used for the first time after a device reset. This initialization of surrounding modules is based on the integration and environment of the DPLLs.

Table 3-308 shows the global initialization of the surrounding modules.

Table 3-308. Global Initialization of Surrounding Modules

Surrounding Modules	Comments
PRCM DPLLs	Ensure that the DPLLS managed by the PRCM module are initialized.

3.10.2.1.2 Clock Management Global Initialization

3.10.2.1.2.1 Main Sequence – Clock Domain Global Initialization

This procedure initializes the clock domain of the device after a power-on or software reset.

Table 3-309. Clock Domain Global Initialization

Step	Register/Bit Field/Programming Model	Value
Configure module clock-management feature of master modules in the clock domain	Module name_SYSCONFIG[x] MIDLEMODE Module name_SYSCONFIG[x] STANDBYMODE	xx(1)
Configure module clock-management feature of slave modules in the clock domain	See Section 3.10.3.3.	
Enable/disable Static Sleep Dependency with other clock domains (that is, destination clock domains). Not all dependencies are configurable.	CM_Clock Domain name_STATICDEP [x] Destination Clock Domain name_STATDEP	0x0 to Disable 0x1 to Enable
Set Dynamic Dependency window size	CM_Clock Domain name_DYNAMICDEP[27:24] WINDOWSIZE	xx(2)
Enable/disable module wake-up dependency for the modules of the clock domain. It is available when the module can generate an interrupt or a DMA request to a service provider module (for example, a processor or DMA).	PM_Clock Domain name_Module name_WKDEP[x] WKUPDEP_Module name_DMA/IRQ request_DMA/Processor name	0x0 to disable 0x1 to enable
Set clock domain state transition feature	CM_Clock Domain name_CLKSTCTRL[1:0]11 CLKTRCTRL	xx(3)

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(1) See the module register for valid modes.

(2) It depends on the desired size of the window. See Section 3.1.1.1.7.2, *Clock Domain Dependency*.

(3) It depends on the desired state of the clock domain. See Table 3-11.

3.10.2.1.2.2 Subsequence – Slave Module Clock-Management Parameters Configuration

This procedure configures the SSC parameters for the DPLL and enables the SSC feature.

Table 3-310. Slave Module Clock-Management Parameter Configuration

Step	Register/Bit Field/Programming Model	Value
Configure module idle mode feature	Module name_SYSCONFIG[x] SIDLEMODE Module name_SYSCONFIG[x] IDLEMODE	xx(1)
IF : Smart-idle mode is selected	Module name_SYSCONFIG[x] SIDLEMODE Module name_SYSCONFIG[x] IDLEMODE	0x10
Configure module clock requirement feature	Module name_SYSCONFIG[x] CLOCKACTIVITY	x(1)
ENDIF		
Configure module management behavior on the PRCM module side	CM_Clock Domain name_Module name_CLKCTRL[1:0] MODULEMODE	xx(2)

(1) See the module register for valid settings.

(2) The selected value depends on the desired clock-management behavior.

3.10.2.2 Clock Domain Sleep Transition and Troubleshooting

This procedure initiates a sleep transition on a clock domain and allows to debug if the transition does not occur.

Table 3-311. Clock Domain Sleep Transition and Troubleshooting

Step	Register/Bit Field/Programming Model	Value
Set clock domain sleep transition state	CM_Clock Domain name_CLKSTCTRL[1:0]11 CLKTRCTRL	0x1: SW_SLEEP 0x3: HW_AUTO
IF : Clock domain sleep transition not initiated?		
Check all clock domain master modules are in standby mode	CM_Clock Domain name_Module name_CLKCTRL[18] STBYST	0x1: Module in standby
Check all clock domain slave modules are in idle mode	CM_Clock Domain name_Module name_CLKCTRL[17:16] IDLEST	0x1: In transition 0x2: Interface clock idled 0x3: Module idled
ENDIF		

3.10.2.3 Enable/Disable Software-Programmable Static Dependency

To change the setting of a software-programmable static dependency use the procedure described in Table 3-312.

Table 3-312. Enable/Disable Software-Programmable Static Dependency

Step	Register/Bit Field/Programming Model	Value
Force destination domain to be awake (SW_WKUP)	CM_Dest_CDname_CLKSTCTRL[1:0] CLKTRCTRL	0x2
Wait until power domain which encloses the destination domain is ON	PM_Dest_PDname_PWRSTST	=0x3
Change the static dependency	CM_Src_CDname_STATICDEP[x] Dest_CDname_STATDEP	0x1
Put destination domain back to automatic transition (HW_AUTO)	CM_Dest_CDname _CLKSTCTRL[1:0] CLKTRCTRL	0x3

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3.10.3 Power Management Low-Level Programming Models

This section covers the low-level hardware programming sequences for configuration and control of the power domain in the device.

3.10.3.1 Global Initialization

3.10.3.1.1 Surrounding Module Global Initialization

It does not require any initialization sequence of any surrounding modules within the device. The external power IC and the device clocks should be active.

3.10.3.1.2 Power Management Global Initialization

3.10.3.1.2.1 Main Sequence – Power Domain Global Initialization and Setting

This procedure initializes the power domain of the device after a power-on or software reset.

Table 3-313. Power Domain Global Initialization

Step	Register/Bit Field/Programming Model	Value
Configure memory area power state when the power domain is on. Not all memory area states are programmable.	PM_Power Domain name_PWRSTCTRL[x] Memory Bank name_ONSTATE	0x0: Off 0x1: RETAINED 0x3: On
Configure memory area power state when the power domain transitions to RETENTION state. Not all memory area states are programmable.	PM_Power Domain name_PWRSTCTRL[x] Memory Bank name_RETSTATE	0x0: Off 0x1: RETAINED
Configure logic area RETENTION power state when the power domain transitions to RETENTION state.	PM_Power Domain name_PWRSTCTRL[2] LOGICRETSTATE	0x0: OSWR 0x1: CSWR
Select target power state of the power domain. Not all states are programmable.	PM_Power Domain name_PWRSTCTRL[1:0] POWERSTATE	0x0: OFF 0x1: RETENTION 0x2: ON-INACTIVE 0x3: ON-ACTIVE
Wait until power state change is complete	PM_Power Domain name_PWRSTST[1:0] POWERSTATEST	0x0: OFF 0x1: RETENTION 0x2: ON-INACTIVE 0x3: ON-ACTIVE

3.10.3.2 Forced Memory Area State Change With Power Domain ON

This procedure initiates a forced memory area state change while the power domain is ON.

Table 3-314. Forced Memory Area State Change With Power Domain ON

Step	Register/Bit Field/Programming Model	Value
Configure memory area target power state. Not all memory area states are programmable.	PM_Power Domain name_PWRSTCTRL[x] Memory Bank name_ONSTATE	0x0: OFF 0x1: RETAINED 0x3: ON
Get memory area current state	PM_Power Domain name_PWRSTST[x] Memory Bank name_STATEST	0x0: OFF 0x1: RETAINED 0x3: ON

3.10.3.3 Forced Power Domain Low-Power State Transition

This procedure initiates a power state transition on a power domain from current low-power state (ON-INACTIVE or RETENTION) to a lower power state (RETENTION, OFF).

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Table 3-315. Forced Memory Area State Change With Power Domain On

Step	Register/Bit Field/Programming Model	Value
Select target low-power state of the power domain. Not all states are programmable.	PM_Power Domain name_PWRSTCTRL[1:0] POWERSTATE	0x0: Off 0x1: Retention
Force power domain low-power state transition.	PM_Power Domain name_PWRSTCTRL[4] LOWPOWERSTATECHANGE	0x1: Force change
Wait until state change is complete	PM_Power Domain name_PWRSTCTRL[4] LOWPOWERSTATECHANGE	0x0: Change complete
Get current power state.	PM_Power Domain name_PWRSTST[1:0] POWERSTATEST	0x0: Off 0x1: Retention

3.10.4 Voltage Management Low-Level Programming Models

This section covers the low-level hardware programming sequences for configuration and management of the voltage domains of the device.

3.10.4.1 Global Initialization

3.10.4.1.1 Surrounding Module Global Initialization

It does not require any initialization sequence of any surrounding modules within the device. The external power IC and the device clocks should be active.

3.10.4.1.2 Voltage Management Global Initialization

3.10.4.1.2.1 Main Sequence – Voltage Management Global Initialization and Setting

This procedure initializes the voltage management framework in the device.

Table 3-316. Power Domain Global Initialization

Step	Register/Bit Field/Programming Model	Value
Initialize SmartReflex modules	See Section 3.10.4.1.3.	
Initialize voltage processor modules	See Section 3.10.4.1.4.	
Initialize voltage controller module	See Section 3.10.4.1.5.	

3.10.4.1.3 SmartReflex Module Initialization

This procedure initializes the SmartReflex module.

Table 3-317. SmartReflex Module Configuration

Step	Register/Bit Field/Programming Model	Value
Configure clock	See Section 3.10.4.1.3.1.	
Configure sensor	See Section 3.10.4.1.3.2.	
Configure accumulator and min/max/avg	See Section 3.10.4.1.3.3.	
Configure error generator	See Section 3.10.4.1.3.4.	
Configure interrupt generator	See Section 3.10.4.1.3.5.	
Enable module	SRn.SRCONFIG[11] SR_EN	0x1

3.10.4.1.3.1 Subsequence – Clock Configuration

This procedure configures the clock for the SmartReflex module.

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Table 3-318. SmartReflex Module Clock Configuration

Step	Register/Bit Field/Programming Model	Value
Configure desired clock frequency	SRn.SRCONFIG[21:12] SRCLKLENGTH	xx(1)
Configure desired idle mode	SRn.ERRCONFIG[25:24] IDLEMODE	0x0: Forced-idle 0x1: No-idle 0x2: Smart-idle 0x3: Smart-idle Wakeup
Enable/disable wake-up feature	SRn.ERRCONFIG[26] WAKEUPENABLE	0x0: Disable 0x1: Enable
Enable clock	CM_ALWON_SR name_CLKCTRL[1:0] MODULEMODE	0x2: Enable

(1) See Equation 1 for clock frequency calculation.

3.10.4.1.3.2 Subsequence – Sensor Configuration

This procedure configures the sensor in the SmartReflex module.

Table 3-319. SmartReflex Module Sensor Configuration

Step	Register/Bit Field/Programming Model	Value
Enable sensor core A	SRn.SRCONFIG[1] SENNENABLE	0x1
Enable sensor core B	SRn.SRCONFIG[0] SENPENABLE	0x1
Enable sensor core	SRn.SRCONFIG[10] SENENABLE	0x1

3.10.4.1.3.3 Subsequence – Accumulator and Min/Max/Avg Configuration

This procedure configures the accumulator and min/max/avg part of the SmartReflex module.

Table 3-320. Accumulator and Min/Max/Avg Configuration

Step	Register/Bit Field/Programming Model	Value
Set size of the accumulator	SRn.SRCONFIG[31:22] ACCUMDATA	xxx(1)
Set average weight parameter for the sensor A	SRn.AVGWEIGHT[1:0] SENNAVGWEIGHT	x(1)
Set average weight parameter for the sensor B	SRn.AVGWEIGHT[3:2] SENPAVGWEIGHT	x(1)
Enable minimum/maximum/average	SRn.SRCONFIG[8] MINMAXAVGENABLE	0x1

(1) These parameters are calculated as given in Section 3.8.3.2.3, *SmartReflex Submodules*.

3.10.4.1.3.4 Subsequence – Error Generator Configuration

This procedure configures the error generator part of the SmartReflex module.

Table 3-321. Error Generator Configuration

Step	Register/Bit Field/Programming Model	Value
Configure four reference value parameters	SRn.NVALUERECIPROCAL[23:20] SENPGAIN	x(1)
	SRn.NVALUERECIPROCAL[19:16] SENNGAIN	x(1)
	SRn.NVALUERECIPROCAL[15:8] SENPRN	xx(1)
	SRn.NVALUERECIPROCAL[7:0] SENNRN	xx(1)
Enable the error generator	SRn.SRCONFIG[9] ERRORGENERATORENABLE	0x1

(1) Configured according to the values read for the current operating voltage level from the control module register in Section 3.8.3.2.3, *SmartReflex Submodules*.

3.10.4.1.3.5 Subsequence – Interrupt Generator Configuration

This procedure configures the interrupt generator part of the SmartReflex module.

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Table 3-322. Interrupt Generator Configuration

Step	Register/Bit Field/Programming Model	Value
Set the four reference value parameters	SRn.ERRCONFIG[18:16] ERRWEIGHT	x
	SRn.ERRCONFIG[15:8] ERRMAXLIMIT	xx
	SRn.ERRCONFIG[7:0] ERRMINLIMIT	xx
IF : Automatic voltage control using voltage processor	Software test condition	
Clear voltage processor bounds interrupt status	SRn.ERRCONFIG[23] VPBOUNDSINTSTATENA	0x1
Unmask voltage processor bounds interrupt	SRn.ERRCONFIG[22] VPBOUNDSINTENABLE	0x1
ELSE-IF : Software-controlled voltage management	Software test condition	
Unmask Processor interrupt events	SRn.IRQENABLE_SET[3] MCUACCUMINTENASET	0x1
	SRn.IRQENABLE_SET[2] MCUVALIDINTENASET	0x1
	SRn.IRQENABLE_SET[1] MCUBOUNDSINTENASET	0x1
ENDIF		

3.10.4.1.4 Voltage Processor Initialization

This procedure initializes the voltage processor.

Table 3-323. Voltage Processor Module Initialization

Step	Register/Bit Field/Programming Model	Value
Configure error-to-voltage converter	See Section 3.10.4.1.4.1.	
Configure PRCM	See Section 3.10.4.1.4.2.	
Mask/unmask interrupt events	PRCM.PRM_IRQENABLE_Processor name	
Enable module	PRCM.PRM_Voltage Processor name_CONFIG[0] VPENABLE	0x1

3.10.4.1.4.1 Subsequence – Error-to-Voltage Converter Configuration

This procedure configures the error-to-voltage converter of the voltage processor.

Table 3-324. Error-to-Voltage Converter Configuration

Step	Register/Bit Field/Programming Model	Value
Set error offset	PRCM.PRM_Voltage Processor name_CONFIG[31:24] ERROROFFSET	xx(1)
Set error gain	PRCM.PRM_Voltage Processor name_CONFIG[23:16] ERRORGAIN	xx(1)
Set SMPS negative voltage step slew rate	PRCM.PRM_Voltage Processor name_VSTEPMIN[23:8] SMPSWAITTIMEMIN	xx(1)
Set SMPS minimum voltage step size	PRCM.PRM_Voltage Processor name_VSTEPMIN[7:0] VSTEPMIN	xx(1)
Set SMPS positive voltage step slew rate	PRCM.PRM_Voltage Processor name_VSTEPMAX[23:8] SMPSWAITTIMEMAX	xx(1)
Set SMPS maximum voltage step size	PRCM.PRM_Voltage Processor name_VSTEPMAX[7:0] VSTEPMAX	xx(1)
Set SMPS minimum voltage limit	PRCM.PRM_Voltage Processor name_VLIMITTO[23:16] VDDMIN	xx(1)
Set SMPS maximum voltage limit	PRCM.PRM_Voltage Processor name_VLIMITTO[31:24] VDDMAX	xx(1)

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(1) Depend on the characteristics of the SMPS.

3.10.4.1.4.2 Subsequence – FSM Configuration

This procedure configures the FSM of the voltage processor.

Table 3-325. FSM Configuration

Step	Register/Bit Field/Programming Model	Value
Set maximum length of time to wait for the command acknowledge from the SMPS	PRCM.PRM_Voltage Processor name_VLIMITTO[15:0] TIMEOUT	xxxx(1)
Set target initial voltage level of the SMPS	PRCM.PRM_Voltage Processor name_CONFIG[15:8] INITVOLTAGE	xx
Assert the initial voltage into the voltage processor FSM	PRCM.PRM_Voltage Processor name_CONFIG[2] INITVDD	0x1

(1) Depend on the characteristics of the SMPS.

3.10.4.1.5 Voltage Controller Initialization

This procedure initializes the voltage controller.

Table 3-326. Voltage Controller Module Initialization

Step	Register/Bit Field/Programming Model	Value
Configure power IC slave addresses	PRCM.PRM_VC_SMPS_SA[x] SA_Voltage Domain name	xx(1)
Configure voltage configuration register addresses	PRCM.PRM_VC_VAL_SMPS_RA_VOL[x] VOLRA_Voltage Domain name	xx(1)
Configure command configuration register addresses	PRCM.PRM_VC_VAL_SMPS_RA_CMD[x] CMDRA_Voltage Domain name	xx(1)
Configure voltage domain command values	PRCM.PRM_VC_VAL_CMD_Voltage Domain name[x] Command name	xx(1)
Configure pointers for the VDD channels	See Section 3.10.4.1.5.1.	
Configure I^2C interface	See Section 3.10.4.1.5.2.	

(1) Depend on the characteristics of the SMPS.

3.10.4.1.5.1 Subsequence – VDD Channels Pointers Configuration

This procedure configures the FSM of the voltage processor.

Table 3-327. VDD Channel Pointer Configuration

Step	Register/Bit Field/Programming Model	Value
Set slave address pointer	PRCM.PRM_VC_CFG_CHANNEL[x] SA_Voltage Domain name	
Set voltage configuration register address pointer	PRCM.PRM_VC_CFG_CHANNEL[x] RAV_Voltage Domain name	
Set command configuration register address pointer	PRCM.PRM_VC_CFG_CHANNEL[x] RAC_Voltage Domain name	
Select voltage or command configuration register for FSM commands	PRCM.PRM_VC_CFG_CHANNEL[x] RACEN_Voltage Domain name	
Set command voltage level selection pointer	PRCM.PRM_VC_CFG_CHANNEL[x] CMD_Voltage Domain name	

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(1) Depend on the connectivity characteristics of the SMPS.

3.10.4.1.5.2 Subsequence – I²C Configuration

This procedure configures the I²C in the voltage controller.

Table 3-328. I²C Configuration

Step	Register/Bit Field/Programming Model	Value
Enable/disable I²C bus double digital filter	PRCM.PRM_VC_CFG_I2C_MODE[6] DFILTEREN	
Set master code value for I²C HS preamble	PRCM.PRM_VC_CFG_I2C_MODE[2:0] HSMCODE	
Enable/disable I²C HS mode	PRCM.PRM_VC_CFG_I2C_MODE[3] HSMODEEN	0x0: Disable 0x1: Enable
Enable/disable repeated start operation.	PRCM.PRM_VC_CFG_I2C_MODE[4] SRMODEEN	0x0: Disable 0x1: Enable

3.10.4.2 Changing OPP

This procedure allows changing of the voltage of the external SMPS from one OPP to the other. It also covers the programming sequence for ABB LDO if the OPP change requires a change in state of the ABB LDO.

NOTE: When switching from the current OPP to a target OPP, if the clock frequency of the target OPP is less than that of the current OPP, the clock frequency is first switched to the lower frequency of target OPP, and only then is the voltage scaling initiated. However, if the clock frequency of the target OPP is greater than that of the current OPP, voltage scaling is initiated before frequency scaling.

Table 3-329. Changing OPP Using Voltage-Processor Module

Step	Register/Bit Field/Programming Model	Value
Disable the SmartReflex module	SRn.SRCONFIG[11] SR_EN	0x0
Mask SmartReflex interrupts		
Disable the voltage processor module	PRCM.PRM_Voltage Processor name_CONFIG[0] VPENABLE	0x0
Configured according to the target OPP voltage value	PRCM.PRM_Voltage Processor name_CONFIG[15:8] INITVOLTAGE	
IF: ABB LDO state change is necessary	Software test (See Section 3.8.4.3)	
Set the desired state of the ABB LDO	PRCM.PRM_LDO_ABB_MPU or DSP_SETUP[x] ACTIVE_FBB_SEL	0x0/0x1
Enable/bypass the ABB power management of the ABB LDO	PRCM.PRM_LDO_ABB_MPU or DSP_SETUP[x] SR2EN	0x0/0x1
Select the next OPP for the ABB LDO	PRM_LDO_ABB_MPU or DSP_CTRL[1:0] OPP_SEL	
Initiate the state change for the ABB LDO	PRM_LDO_ABB_MPU or DSP_CTRL[2] OPP_CHANGE	0x1
Wait until ABB LDO state transition completes	PRM_LDO_ABB_MPU or DSP_CTRL[6] SR2_IN_TRANSITION	0x0
ENDIF		
Triggers a write of the value in the INITVOLTAGE into the voltage processor	PRCM.PRM_Voltage Processor name_CONFIG[2] INITVDD	0x1
Force update of the SMPS	PRCM.PRM_Voltage Processor name_CONFIG[1] FORCEUPDATE	0x1

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3.11 PRCM Register Manual

3.11.1 PRM Instance Summary

Table 3-330. PRM Instance Summary

Module Name	L4 Base Address	Size
INTRCONN_SOCKET_PRM	0x4A30 6000	256 bytes
CKGEN_PRM	0x4A30 6100	256 bytes
MPU_PRM	0x4A30 6300	256 bytes
DSP_PRM	0x4A30 6400	256 bytes
ABE_PRM	0x4A30 6500	256 bytes
ALWAYS_ON_PRM	0x4A30 6600	256 bytes
CORE_PRM	0x4A30 6700	2KB
IVAHD_PRM	0x4A30 6F00	256 bytes
CAM_PRM	0x4A30 7000	256 bytes
DSS_PRM	0x4A30 7100	256 bytes
SGX_PRM	0x4A30 7200	256 bytes
L3INIT_PRM	0x4A30 7300	256 bytes
L4PER_PRM	0x4A30 7400	512 bytes
WKUP_PRM	0x4A30 7700	256 bytes
WKUP_CM	0x4A30 7800	256 bytes
EMU_PRM	0x4A30 7900	256 bytes
EMU_CM	0x4A30 7A00	256 bytes
DEVICE_PRM	0x4A30 7B00	256 bytes
INSTR_PRM	0x4A30 7F00	256 bytes

3.11.2 INTRCONN_SOCKET_PRM Registers

3.11.2.1 INTRCONN_SOCKET_PRM Register Summary

Table 3-331. INTRCONN_SOCKET_PRM Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	INTRCONN_SOCKET_PRM L4 Base Address
REVISION_PRM	R	32	0x0000 0000	0x4A30 6000
PRM_IRQSTATUS_MPU_A9	RW	32	0x0000 0010	0x4A30 6010
PRM_IRQSTATUS_MPU_A9_2	RW	32	0x0000 0014	0x4A30 6014
PRM_IRQENABLE_MPU_A9	RW	32	0x0000 0018	0x4A30 6018
PRM_IRQENABLE_MPU_A9_2	RW	32	0x0000 001C	0x4A30 601C
PRM_IRQSTATUS_MPU_M3	RW	32	0x0000 0020	0x4A30 6020
PRM_IRQENABLE_MPU_M3	RW	32	0x0000 0028	0x4A30 6028
PRM_IRQSTATUS_DSP	RW	32	0x0000 0030	0x4A30 6030
PRM_IRQENABLE_DSP	RW	32	0x0000 0038	0x4A30 6038
CM_PRM_PROFILING_CLKCTRL	RW	32	0x0000 0040	0x4A30 6040
PRM_DEBUG_CFG	RW	32	0x0000 00F0	0x4A30 60F0

3.11.2.2 INTRCONN_SOCKET_PRM Register Description

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Table 3-332. REVISION_PRM

Address Offset	0x0000 0000		
Physical Address	0x4A30 6000	**Instance**	INTRCONN_SOCKET_PRM
Description	This register contains the IP revision code for the PRM part of the PRCM		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REV																															

Bits	Field Name	Description	Type	Reset
31:0	REV	Revision Number	R	0x- - TI Internal data

Table 3-333. Register Call Summary for Register REVISION_PRM

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- INTRCONN_SOCKET_PRM Register Summary: [0]

Table 3-334. PRM_IRQSTATUS_MPU_A9

Address Offset	0x0000 0010		
Physical Address	0x4A30 6010	**Instance**	INTRCONN_SOCKET_PRM
Description	This register provides status on MPU interrupt events. Any event is logged independently of the corresponding IRQENABLE value. Software is required to clear a set bit by writing a 1 into the bit-position to be cleared.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ABB_IVA_DONE_ST	VC_IVA_VPACK_ST	VP_IVA_TRANXDONE_ST	VP_IVA_EQVALUE_ST	VP_IVA_NOSMPSACK_ST	VP_IVA_MAXVDD_ST	VP_IVA_MINVDD_ST	VP_IVA_OPPCHANGEDONE_ST	RESERVED	VC_CORE_VPACK_ST	VP_CORE_TRANXDONE_ST	VP_CORE_EQVALUE_ST	VP_CORE_NOSMPSACK_ST	VP_CORE_MAXVDD_ST	VP_CORE_MINVDD_ST	VP_CORE_OPPCHANGEDONE_ST	RESERVED	VC_BYPASSACK_ST	VC_TOERR_ST	VC_RAERR_ST	VC_SAERR_ST	RESERVED	IO_ST	TRANSITION_ST	RESERVED			DPLL_ABE_RECAL_ST	DPLL_PER_RECAL_ST	DPLL_IVA_RECAL_ST	DPLL_MPU_RECAL_ST	DPLL_CORE_RECAL_ST

Bits	Field Name	Description	Type	Reset
31	ABB_IVA_DONE_ST	IVA ABB mode change done. This status is set when OPP_CHANGE bit is cleared by hardware in PRM_LDO_ABB_IVA_CRTL register. It is cleared by software. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
30	VC_IVA_VPACK_ST	Voltage Controller IVA voltage processor command acknowledge status. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
29	VP_IVA_TRANXDONE_ST	Voltage Processor IVA transaction completion status. This status is set when a transaction is completed in the voltage processor, including ABB mode change done if applicable (OPP_CHANGE bit cleared in PRM_LDO_ABB_IVA_CRTL). It is cleared by software. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
28	VP_IVA_EQVALUE_ST	Voltage Processor IVA voltage value change event. This status is set when an update has been requested but the new voltage value is the same as the current SMPS voltage value. It is cleared by software. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
27	VP_IVA_NOSMPSACK_ST	Voltage Processor IVA timeout event status. This status is set when the timeout occured before the SMPS acknowledge. It is cleared by software. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
26	VP_IVA_MAXVDD_ST	Voltage Processor IVA voltage higher limit event status. This status is set when the voltage higher limit is reached. It is cleared by software. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
25	VP_IVA_MINVDD_ST	Voltage Processor IVA voltage lower limit event status. This status is set when the voltage lower limit is reached. It is cleared by software. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
24	VP_IVA_OPPCHANGEDONE_ST	Voltage Processor IVA OPP change done status, including ABB mode change done if applicable (OPP_CHANGE bit cleared in PRM_LDO_ABB_IVA_CRTL). It is cleared by software. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
23	RESERVED		R	0
22	VC_CORE_VPACK_ST	Voltage Controller CORE voltage processor command acknowledge status 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
21	VP_CORE_TRANXDONE_ST	Voltage Processor CORE transaction completion status. This status is set when a transaction is completed in the voltage processor. It is cleared by software. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
20	VP_CORE_EQVALUE_ST	Voltage Processor CORE voltage value change event. This status is set when an update has been requested but the new voltage value is the same as the current SMPS voltage value. It is cleared by software. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
19	VP_CORE_NOSMPSACK_ST	Voltage Processor CORE timeout event status. This status is set when the timeout occured before the SMPS acknowledge. It is cleared by software. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
18	VP_CORE_MAXVDD_ST	Voltage Processor CORE voltage higher limit event status. This status is set when the voltage higher limit is reached. It is cleared by software. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
17	VP_CORE_MINVDD_ST	Voltage Processor CORE voltage lower limit event status. This status is set when the voltage lower limit is reached. It is cleared by software. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
16	VP_CORE_OPPCHANGEDONE_ST	Voltage Processor CORE OPP change done status. It is cleared by software. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
15	Reserved		R	0
14	VC_BYPASSACK_ST	Voltage Controller bypass command acknowledge status. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
13	VC_TOERR_ST	Voltage Controller timeout error event status. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
12	VC_RAERR_ST	Voltage Controller register address acknowledge error event status. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
11	VC_SAERR_ST	Voltage Controller slave address acknowledge error event status. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0x0
10	RESERVED		R	0
9	IO_ST	I/O pad event interrupt status. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
8	TRANSITION_ST	Software supervised transition completed event interrupt status (any domain). Asserted upon completion of any clock domain force wakeup transition or upon completion of any power domain sleep transition with at least one enclosed clock domain configured in forced-sleep. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
7:5	RESERVED		R	0x0
4	DPLL_ABE_RECAL_ST	ABE DPLL recalibration interrupt status. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
3	DPLL_PER_RECAL_ST	PER DPLL recalibration interrupt status. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
2	DPLL_IVA_RECAL_ST	IVA DPLL recalibration interrupt status. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
1	DPLL_MPU_RECAL_ST	MPU DPLL recalibration interrupt status. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
0	DPLL_CORE_RECAL_ST	CORE DPLL recalibration interrupt status. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0

Table 3-335. Register Call Summary for Register PRM_IRQSTATUS_MPU_A9

Clock Management Functional Description
- DPLL_PER Description: [0]
- DPLL_CORE Description: [1]
- DPLL_ABE Description: [2]
- DPLL_MPU Description: [3]
- DPLL_IVA Description: [4]

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- INTRCONN_SOCKET_PRM Register Summary: [5]

Table 3-336. PRM_IRQSTATUS_MPU_A9_2

Address Offset	0x0000 0014		
Physical Address	0x4A30 6014	**Instance**	INTRCONN_SOCKET_PRM
Description	This register provides status on MPU interrupt events. Any event is logged independently of the corresponding IRQENABLE value. Software is required to clear a set bit by writing a 1 into the bit-position to be cleared.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								ABB_MPU_DONE_ST	VC_MPU_VPACK_ST	VP_MPU_TRANXDONE_ST	VP_MPU_EQVALUE_ST	VP_MPU_NOSMPSACK_ST	VP_MPU_MAXVDD_ST	VP_MPU_MINVDD_ST	VP_MPU_OPPCHANGEDONE_ST

Bits	Field Name	Description	Type	Reset
31:8	RESERVED		R	0x000000
7	ABB_MPU_DONE_ST	MPU ABB mode change done. This status is set when OPP_CHANGE bit is cleared by hardware in PRM_LDO_ABB_MPU_CRTL register. It is cleared by software. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
6	VC_MPU_VPACK_ST	Voltage Controller MPU voltage processor command acknowledge status. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
5	VP_MPU_TRANXDONE_ST	Voltage Processor MPU transaction completion status. This status is set when a transaction is completed in the voltage processor, including ABB mode change done if applicable (OPP_CHANGE bit cleared in PRM_LDO_ABB_MPU_CRTL). It is cleared by software. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
4	VP_MPU_EQVALUE_ST	Voltage Processor MPU voltage value change event. This status is set when an update has been requested but the new voltage value is the same as the current SMPS voltage value. It is cleared by software. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
3	VP_MPU_NOSMPSACK_ST	Voltage Processor MPU timeout event status. This status is set when the timeout occured before the SMPS acknowledge. It is cleared by software. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
2	VP_MPU_MAXVDD_ST	Voltage Processor MPU voltage higher limit event status. This status is set when the voltage higher limit is reached. It is cleared by software. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
1	VP_MPU_MINVDD_ST	Voltage Processor MPU voltage lower limit event status. This status is set when the voltage lower limit is reached. It is cleared by software. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
0	VP_MPU_OPPCHANGEDONE_ST	Voltage Processor MPU OPP change done status, including ABB mode change done if applicable (OPP_CHANGE bit cleared in PRM_LDO_ABB_MPU_CRTL). It is cleared by software. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0

Table 3-337. Register Call Summary for Register PRM_IRQSTATUS_MPU_A9_2

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- INTRCONN_SOCKET_PRM Register Summary: [0]

Table 3-338. PRM_IRQENABLE_MPU_A9

Address Offset	0x0000 0018		
Physical Address	0x4A30 6018	**Instance**	INTRCONN_SOCKET_PRM
Description	This register is used to enable or disable MPU interrupt activation upon presence of corresponding IRQSTATUS bit.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ABB_IVA_DONE_EN	VC_IVA_VPACK_EN	VP_IVA_TRANXDONE_EN	VP_IVA_EQVALUE_EN	VP_IVA_NOSMPSACK_EN	VP_IVA_MAXVDD_EN	VP_IVA_MINVDD_EN	VP_IVA_OPPCHANGEDONE_EN	RESERVED	VC_CORE_VPACK_EN	VP_CORE_TRANXDONE_EN	VP_CORE_EQVALUE_EN	VP_CORE_NOSMPSACK_EN	VP_CORE_MAXVDD_EN	VP_CORE_MINVDD_EN	VP_CORE_OPPCHANGEDONE_EN	RESERVED	VC_BYPASSACK_EN	VC_TOERR_EN	VC_RAERR_EN	VC_SAERR_EN	RESERVED	IO_EN	TRANSITION_EN	RESERVED			DPLL_ABE_RECAL_EN	DPLL_PER_RECAL_EN	DPLL_IVA_RECAL_EN	DPLL_MPU_RECAL_EN	DPLL_CORE_RECAL_EN

Bits	Field Name	Description	Type	Reset
31	ABB_IVA_DONE_EN	IIVA ABB mode change done enable. 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
30	VC_IVA_VPACK_EN	Voltage Controller IVA voltage processor command acknowledge enable. 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
29	VP_IVA_TRANXDONE_EN	Voltage Processor IVA transaction completion enable. 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
28	VP_IVA_EQVALUE_EN	Voltage Processor IVA voltage value change event enable. 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
27	VP_IVA_NOSMPSACK_EN	Voltage Processor IVA timeout event enable. 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
26	VP_IVA_MAXVDD_EN	Voltage Processor IVA voltage higher limit event enable. 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
25	VP_IVA_MINVDD_EN	Voltage Processor IVA voltage lower limit event enable. 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
24	VP_IVA_OPPCHANGEDONE_EN	Voltage Processor IVA OPP change done enable. 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
23	RESERVED		R	0
22	VC_CORE_VPACK_EN	Voltage Controller CORE voltage processor command acknowledge enable 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
21	VP_CORE_TRANXDONE_EN	Voltage Processor CORE transaction completion enable. 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0

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Bits	Field Name	Description	Type	Reset
20	VP_CORE_EQVALUE_EN	Voltage Processor CORE voltage value change event enable. 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
19	VP_CORE_NOSMPSACK_EN	Voltage Processor CORE timeout event enable. 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
18	VP_CORE_MAXVDD_EN	Voltage Processor CORE voltage higher limit event enable. 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
17	VP_CORE_MINVDD_EN	Voltage Processor CORE voltage lower limit event enable. 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
16	VP_CORE_OPPCHANGEDONE_EN	Voltage Processor CORE OPP change done enable. 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
15	RESERVED		R	0
14	VC_BYPASSACK_EN	Voltage Controller bypass command acknowledge enable. 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
13	VC_TOERR_EN	Voltage Controller timeout error event enable. 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
12	VC_RAERR_EN	Voltage Controller register address acknowledge error event enable. 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
11	VC_SAERR_EN	Voltage Controller slave address acknowledge error event enable. 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0x0
10	RESERVED		R	0
9	IO_EN	I/O pad event interrupt enable. 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
8	TRANSITION_EN	Software supervised transition completed event interrupt enable (any domain). 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
7:5	RESERVED		R	0x0
4	DPLL_ABE_RECAL_EN	ABE DPLL recalibration interrupt enable. 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
3	DPLL_PER_RECAL_EN	PER DPLL recalibration interrupt enable. 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0

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Bits	Field Name	Description	Type	Reset
2	DPLL_IVA_RECAL_EN	IVA DPLL recalibration interrupt enable. 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
1	DPLL_MPU_RECAL_EN	MPU DPLL recalibration interrupt enable. 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
0	DPLL_CORE_RECAL_EN	CORE DPLL recalibration interrupt enable. 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0

Table 3-339. Register Call Summary for Register PRM_IRQENABLE_MPU_A9

Clock Management Functional Description
- DPLL_PER Description: [0]
- DPLL_CORE Description: [1]
- DPLL_ABE Description: [2]
- DPLL_MPU Description: [3]
- DPLL_IVA Description: [4]

PRCM Register Manual
- INTRCONN_SOCKET_PRM Register Summary: [5]

Table 3-340. PRM_IRQENABLE_MPU_A9_2

Address Offset	0x0000 001C		
Physical Address	0x4A30 601C	**Instance**	INTRCONN_SOCKET_PRM
Description	This register is used to enable or disable MPU interrupt activation upon presence of corresponding IRQSTATUS bit.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								ABB_MPU_DONE_EN	VC_MPU_VPACK_EB	VP_MPU_TRANXDONE_EN	VP_MPU_EQVALUE_EN	VP_MPU_NOSMPSACK_EN	VP_MPU_MAXVDD_EN	VP_MPU_MINVDD_EN	VP_MPU_OPPCHANGEDONE_EN

Bits	Field Name	Description	Type	Reset
31:8	RESERVED		R	0x0000000
7	ABB_MPU_DONE_EN	MPU ABB mode change done enable. 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
6	VC_MPU_VPACK_EB	Voltage Controller MPU voltage processor command acknowledge enable. 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0

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Bits	Field Name	Description	Type	Reset
5	VP_MPU_TRANXDONE_EN	Voltage Processor MPU transaction completion enable 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
4	VP_MPU_EQVALUE_EN	Voltage Processor MPU voltage value change event enable 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
3	VP_MPU_NOSMPSACK_EN	Voltage Processor MPU timeout event enable 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
2	VP_MPU_MAXVDD_EN	Voltage Processor MPU voltage higher limit event enable 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
1	VP_MPU_MINVDD_EN	Voltage Processor MPU voltage lower limit event enable 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
0	VP_MPU_OPPCHANGEDONE_EN	Voltage Processor MPU OPP change done enable 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0

Table 3-341. Register Call Summary for Register PRM_IRQENABLE_MPU_A9_2

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- INTRCONN_SOCKET_PRM Register Summary: [0]

Table 3-342. PRM_IRQSTATUS_MPU_M3

Address Offset	0x0000 0020		
Physical Address	0x4A30 6020	**Instance**	INTRCONN_SOCKET_PRM
Description	This register provides status on MPU_A3 interrupt events. Any event is logged independently of the corresponding IRQENABLE value. Software is required to clear a set bit by writing a 1 into the bit-position to be cleared.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ABB_IVA_DONE_ST	VC_IVA_VPACK_ST	VP_IVA_TRANXDONE_ST	VP_IVA_EQVALUE_ST	VP_IVA_NOSMPSACK_ST	VP_IVA_MAXVDD_ST	VP_IVA_MINVDD_ST	VP_IVA_OPPCHANGEDONE_ST	RESERVED	VC_CORE_VPACK_ST	VP_CORE_TRANXDONE_ST	VP_CORE_EQVALUE_ST	VP_CORE_NOSMPSACK_ST	VP_CORE_MAXVDD_ST	VP_CORE_MINVDD_ST	VP_CORE_OPPCHANGEDONE_ST	RESERVED	VC_BYPASSACK_ST	VC_TOERR_ST	VC_RAERR_ST	VC_SAERR_ST	FORCEWKUP_ST	IO_ST	TRANSITION_ST	RESERVED			DPLL_ABE_RECAL_ST	DPLL_PER_RECAL_ST	DPLL_IVA_RECAL_ST	RESERVED	DPLL_CORE_RECAL_ST

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Bits	Field Name	Description	Type	Reset
31	ABB_IVA_DONE_ST	IVA ABB mode change done. This status is set when OPP_CHANGE bit is cleared by hardware in PRM_LDO_ABB_IVA_CRTL register. It is cleared by software. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
30	VC_IVA_VPACK_ST	Voltage Controller IVA voltage processor command acknowledge status 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
29	VP_IVA_TRANXDONE_ST	Voltage Processor IVA transaction completion status. This status is set when a transaction is completed in the voltage processor, including ABB mode change done if applicable (OPP_CHANGE bit cleared in PRM_LDO_ABB_IVA_CRTL). It is cleared by software. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
28	VP_IVA_EQVALUE_ST	Voltage Processor IVA voltage value change event. This status is set when an update has been requested but the new voltage value is the same as the current SMPS voltage value. It is cleared by software. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
27	VP_IVA_NOSMPSACK_ST	Voltage Processor IVA timeout event status. This status is set when the timeout occured before the SMPS acknowledge. It is cleared by software. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
26	VP_IVA_MAXVDD_ST	Voltage Processor IVA voltage higher limit event status. This status is set when the voltage higher limit is reached. It is cleared by software. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
25	VP_IVA_MINVDD_ST	Voltage Processor IVA voltage lower limit event status. This status is set when the voltage lower limit is reached. It is cleared by software. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
24	VP_IVA_OPPCHANGEDONE_ST	Voltage Processor IVA OPP change done status, including ABB mode change done if applicable (OPP_CHANGE bit cleared in PRM_LDO_ABB_IVA_CRTL). It is cleared by software. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
23	RESERVED		R	0
22	VC_CORE_VPACK_ST	Voltage Controller CORE voltage processor command acknowledge status 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
21	VP_CORE_TRANXDONE_ST	Voltage Processor CORE transaction completion status. This status is set when a transaction is completed in the voltage processor. It is cleared by software. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
20	VP_CORE_EQVALUE_ST	Voltage Processor CORE voltage value change event. This status is set when an update has been requested but the new voltage value is the same as the current SMPS voltage value. It is cleared by software. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
19	VP_CORE_NOSMPSACK_ST	Voltage Processor CORE timeout event status. This status is set when the timeout occured before the SMPS acknowledge. It is cleared by software. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
18	VP_CORE_MAXVDD_ST	Voltage Processor CORE voltage higher limit event status. This status is set when the voltage higher limit is reached. It is cleared by software. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
17	VP_CORE_MINVDD_ST	Voltage Processor CORE voltage lower limit event status. This status is set when the voltage lower limit is reached. It is cleared by software. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
16	VP_CORE_OPPCHANGEDONE_ST	Voltage Processor CORE OPP change done status. It is cleared by software. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
15	RESERVED		R	0
14	VC_BYPASSACK_ST	Voltage Controller bypass command acknowledge status 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
13	VC_TOERR_ST	Voltage Controller timeout error event status 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
12	VC_RAERR_ST	Voltage Controller register address acknowledge error event status 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
11	VC_SAERR_ST	Voltage Controller slave address acknowledge error event status 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
10	FORCEWKUP_ST	CORTEXM3 domain software supervised wakeup transition completed event interrupt status. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
9	IO_ST	I/O pad event interrupt status. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
8	TRANSITION_ST	Software supervised transition completed event interrupt status (any domain). Asserted upon completion of any clock domain force wakeup transition or upon completion of any power domain sleep transition with at least one enclosed clock domain configured in forced-sleep. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
7:5	RESERVED		R	0x0
4	DPLL_ABE_RECAL_ST	ABE DPLL recalibration interrupt status. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
3	DPLL_PER_RECAL_ST	PER DPLL recalibration interrupt status. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
2	DPLL_IVA_RECAL_ST	IVA DPLL recalibration interrupt status. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
1	RESERVED		R	0
0	DPLL_CORE_RECAL_ST	CORE DPLL recalibration interrupt status. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0

Table 3-343. Register Call Summary for Register PRM_IRQSTATUS_MPU_M3

Clock Management Functional Description
- DPLL_PER Description: [0]
- DPLL_CORE Description: [1]
- DPLL_IVA Description: [2]

Voltage Management Functional Description
- Adaptive Voltage Scaling: [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14]

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- INTRCONN_SOCKET_PRM Register Summary: [15]

Table 3-344. PRM_IRQENABLE_MPU_M3

Address Offset	0x0000 0028		
Physical Address	0x4A30 6028	**Instance**	INTRCONN_SOCKET_PRM
Description	This register is used to enable or disable MPU_A3 interrupt activation upon presence of corresponding IRQSTATUS bit.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ABB_IVA_DONE_EN	VC_IVA_VPACK_EN	VP_IVA_TRANXDONE_EN	VP_IVA_EQVALUE_EN	VP_IVA_NOSMPSACK_EN	VP_IVA_MAXVDD_EN	VP_IVA_MINVDD_EN	VP_IVA_OPPCHANGEDONE_EN	RESERVED	VC_CORE_VPACK_EN	VP_CORE_TRANXDONE_EN	VP_CORE_EQVALUE_EN	VP_CORE_NOSMPSACK_EN	VP_CORE_MAXVDD_EN	VP_CORE_MINVDD_EN	VP_CORE_OPPCHANGEDONE_EN	RESERVED	VC_BYPASSACK_EN	VC_TOERR_EN	VC_RAERR_EN	VC_SAERR_EN	FORCEWKUP_EN	IO_EN	TRANSITION_EN	RESERVED			DPLL_ABE_RECAL_EN	DPLL_PER_RECAL_EN	DPLL_IVA_RECAL_EN	RESERVED	DPLL_CORE_RECAL_EN

Bits	Field Name	Description	Type	Reset
31	ABB_IVA_DONE_EN	IVA ABB mode change done enable 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0

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Bits	Field Name	Description	Type	Reset
30	VC_IVA_VPACK_EN	Voltage Controller IVA voltage processor command acknowledge enable 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
29	VP_IVA_TRANXDONE_EN	Voltage Processor IVA transaction completion enable 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
28	VP_IVA_EQVALUE_EN	Voltage Processor IVA voltage value change event enable 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
27	VP_IVA_NOSMPSACK_EN	Voltage Processor IVA timeout event enable 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
26	VP_IVA_MAXVDD_EN	Voltage Processor IVA voltage higher limit event enable 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
25	VP_IVA_MINVDD_EN	Voltage Processor IVA voltage lower limit event enable 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
24	VP_IVA_OPPCHANGEDONE_EN	Voltage Processor IVA OPP change done enable 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
23	RESERVED		R	0
22	VC_CORE_VPACK_EN	Voltage Controller CORE voltage processor command acknowledge enable 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
21	VP_CORE_TRANXDONE_EN	Voltage Processor CORE transaction completion enable 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
20	VP_CORE_EQVALUE_EN	Voltage Processor CORE voltage value change event enable 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
19	VP_CORE_NOSMPSACK_EN	Voltage Processor CORE timeout event enable 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
18	VP_CORE_MAXVDD_EN	Voltage Processor CORE voltage higher limit event enable 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
17	VP_CORE_MINVDD_EN	Voltage Processor CORE voltage lower limit event enable 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
16	VP_CORE_OPPCHANGEDONE_EN	Voltage Processor CORE OPP change done enable 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
15	RESERVED		R	0

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Bits	Field Name	Description	Type	Reset
14	VC_BYPASSACK_EN	Voltage Controller bypass command acknowledge enable 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
13	VC_TOERR_EN	Voltage Controller timeout error event enable 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
12	VC_RAERR_EN	Voltage Controller register address acknowledge error event enable 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
11	VC_SAERR_EN	Voltage Controller slave address acknowledge error event enable 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
10	FORCEWKUP_EN	CORTEXM3 domain software supervised wakeup transition completed event interrupt enable. 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
9	IO_EN	I/O pad event interrupt enable 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
8	TRANSITION_EN	Software supervised transition completed event interrupt enable (any domain) 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
7:5	RESERVED		R	0x0
4	DPLL_ABE_RECAL_EN	ABEDPLL recalibration interrupt enable 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
3	DPLL_PER_RECAL_EN	PER DPLL recalibration interrupt enable 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
2	DPLL_IVA_RECAL_EN	IVA DPLL recalibration interrupt enable 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
1	RESERVED		R	0
0	DPLL_CORE_RECAL_EN	CORE DPLL recalibration interrupt enable 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0

Table 3-345. Register Call Summary for Register PRM_IRQENABLE_MPU_M3

Clock Management Functional Description • DPLL_PER Description: [0] • DPLL_CORE Description: [1] • DPLL_IVA Description: [2]
Voltage Management Functional Description • Adaptive Voltage Scaling: [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14]
PRCM Register Manual • INTRCONN_SOCKET_PRM Register Summary: [15]

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Table 3-346. PRM_IRQSTATUS_DSP

Address Offset	0x0000 0030		
Physical Address	0x4A30 6030	**Instance**	INTRCONN_SOCKET_PRM
Description	This register provides status on DSP interrupt events. Any event is logged independently of the corresponding IRQENABLE value. Software is required to clear a set bit by writing a 1 into the bit-position to be cleared.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																					FORCEWKUP_ST	RESERVED					DPLL_ABE_RECAL_ST	RESERVED	DPLL_IVA_RECAL_ST	RESERVED	

Bits	Field Name	Description	Type	Reset
31:11	RESERVED		R	0x000000
10	FORCEWKUP_ST	DSP domain software supervised wakeup transition completed event interrupt status. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
9:5	RESERVED		R	0x00
4	DPLL_ABE_RECAL_ST	ABE DPLL recalibration interrupt status. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
3	RESERVED		R	0
2	DPLL_IVA_RECAL_ST	IVA DPLL recalibration interrupt status. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
1:0	RESERVED		R	0x0

Table 3-347. Register Call Summary for Register PRM_IRQSTATUS_DSP

PRCM Register Manual

- INTRCONN_SOCKET_PRM Register Summary: [0]

Table 3-348. PRM_IRQENABLE_DSP

Address Offset	0x0000 0038		
Physical Address	0x4A30 6038	**Instance**	INTRCONN_SOCKET_PRM
Description	This register is used to enable or disable DSP interrupt activation upon presence of corresponding IRQSTATUS bit.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																					FORCEWKUP_EN	RESERVED					DPLL_ABE_RECAL_EN	RESERVED	DPLL_IVA_RECAL_EN	RESERVED	

Bits	Field Name	Description	Type	Reset
31:11	RESERVED		R	0x000000
10	FORCEWKUP_EN	DSP domain software supervised wakeup transition completed event interrupt enable. 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
9:5	RESERVED		R	0x00
4	DPLL_ABE_RECAL_EN	ABEDPLL recalibration interrupt enable 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
3	RESERVED		R	0
2	DPLL_IVA_RECAL_EN	IVA DPLL recalibration interrupt enable 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
1:0	RESERVED		R	0x0

Table 3-349. Register Call Summary for Register PRM_IRQENABLE_DSP

PRCM Register Manual
- INTRCONN_SOCKET_PRM Register Summary: [0]

Table 3-350. CM_PRM_PROFILING_CLKCTRL

Address Offset	0x0000 0040		
Physical Address	0x4A30 6040	**Instance**	INTRCONN_SOCKET_PRM
Description	This register manages the PRM_PROFILING clock. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED														MODULEMODE	

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Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status Read 0x0: Module is fully functional Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in Idle Read 0x3: Module is disabled	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disabled by software. INTRCONN configuration port is not accessible. 0x1: Module is managed automatically by hardware along with EMU domain. INTRCONN configuration port is accessible only when EMU domain is on. Read 0x2: Reserved Read 0x3: Reserved	RW	0x0

Table 3-351. Register Call Summary for Register CM_PRM_PROFILING_CLKCTRL

PRCM Register Manual
- INTRCONN_SOCKET_PRM Register Summary: [0]

Table 3-352. PRM_DEBUG_CFG

Address Offset	0x0000 00F0		
Physical Address	0x4A30 60F0	**Instance**	INTRCONN_SOCKET_PRM
Description	This register is used to configure the PRM's 32-bit debug output. There is one 7-bit source select field for selecting from a shared set of 8-bit internal signal blocks per byte. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	SEL3							RESERVED	SEL2							RESERVED	SEL1							RESERVED	SEL0						

Bits	Field Name	Description	Type	Reset
31	RESERVED		R	0
30:24	SEL3	Internal signal block select for debug word byte-3	RW	0x03
23	RESERVED		R	0
22:16	SEL2	Internal signal block select for debug word byte-2	RW	0x02
15	RESERVED		R	0
14:8	SEL1	Internal signal block select for debug word byte-1	RW	0x01
7	RESERVED		R	0
6:0	SEL0	Internal signal block select for debug word byte-0	RW	0x00

Table 3-353. Register Call Summary for Register PRM_DEBUG_CFG

PRCM Register Manual
- INTRCONN_SOCKET_PRM Register Summary: [0]

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3.11.3 CKGEN_PRM Registers

3.11.3.1 CKGEN_PRM Register Summary

Table 3-354. CKGEN_PRM Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	CKGEN_PRM L4 Base Address
CM_ABE_DSS_SYS_CLKSEL	RW	32	0x0000 0000	0x4A30 6100
RESERVED	RW	32	0x0000 0004	0x4A30 6104
CM_L4_WKUP_CLKSEL	RW	32	0x0000 0008	0x4A30 6108
CM_ABE_PLL_REF_CLKSEL	RW	32	0x0000 000C	0x4A30 610C
CM_SYS_CLKSEL	RW	32	0x0000 0010	0x4A30 6110

3.11.3.2 CKGEN_PRM Register Description

Table 3-355. CM_ABE_DSS_SYS_CLKSEL

Address Offset	0x0000 0000		
Physical Address	0x4A30 6100	**Instance**	CKGEN_PRM
Description	Select the SYS CLK for ABE and DSS subsystems. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															CLKSEL

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	CLKSEL	Selects the divider value 0x0: Select SYS_CLK divided by 1 0x1: Select SYS_CLK divided by 2 Must be used for SYS_CLK > 26 MHz	RW	0

Table 3-356. Register Call Summary for Register CM_ABE_DSS_SYS_CLKSEL

PRCM Register Manual

- CKGEN_PRM Register Summary: [0]

Table 3-357. CM_L4_WKUP_CLKSEL

Address Offset	0x0000 0008		
Physical Address	0x4A30 6108	**Instance**	CKGEN_PRM
Description	Control the functional clock source of L4_WKUP, PRM and Smart Reflex functional clock.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															CLKSEL

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Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	CLKSEL	Select the clock source for L4WKUP_ICLK and for ABE_DPLL_BYPASS_CLK clocks. 0x0: Selects SYS_CLK for L4WKUP_ICLK Selects SYS_CLK for ABE_DPLL_BYPASS_CLK 0x1: Selects ABE_LP_CLK for L4WKUP_ICLK Selects 32K_FCLK for ABE_DPLL_BYPASS_CLK	RW	0

Table 3-358. Register Call Summary for Register CM_L4_WKUP_CLKSEL

Clock Management Functional Description • PRM Clock Source: [0] [1]
PRCM Register Manual • CKGEN_PRM Register Summary: [2]

Table 3-359. CM_ABE_PLL_REF_CLKSEL

Address Offset	0x0000 000C		
Physical Address	0x4A30 610C	**Instance**	CKGEN_PRM
Description	Control the source of the reference clock for DPLL_ABE		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															CLKSEL

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	CLKSEL	Select the source for the DPLL_ABE reference clock. 0x0: Selects SYS_CLK 0x1: Selects SYS_32K	RW	1

Table 3-360. Register Call Summary for Register CM_ABE_PLL_REF_CLKSEL

Clock Management Functional Description • PRM Clock Source: [0]
PRCM Register Manual • CKGEN_PRM Register Summary: [1]

Table 3-361. CM_SYS_CLKSEL

Address Offset	0x0000 0010		
Physical Address	0x4A30 6110	**Instance**	CKGEN_PRM
Description	Software sets the SYS_CLK configuration corresponding to the frequency of SYS_CLK. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														SYS_CLKSEL	

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Bits	Field Name	Description	Type	Reset
31:3	RESERVED		R	0x0000 0000
2:0	SYS_CLKSEL	System clock input selection. 0x0: Uninitialized 0x1: Input clock is 12 MHz 0x2: Reserved 0x3: Input clock is 16.8 MHz 0x4: Input clock is 19.2 MHz 0x5: Input clock is 26 MHz 0x6: Reserved 0x7: Input clock is 38.4 MHz	RW	0x0

Table 3-362. Register Call Summary for Register CM_SYS_CLKSEL

PRCM Register Manual
- CKGEN_PRM Register Summary: [0]

3.11.4 MPU_PRM Registers

3.11.4.1 MPU_PRM Register Summary

Table 3-363. MPU_PRM Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	MPU_PRM L4 Base Address
PM_MPU_PWRSTCTRL	RW	32	0x0000 0000	0x4A30 6300
PM_MPU_PWRSTST	R	32	0x0000 0004	0x4A30 6304
RM_MPU_RSTST	RW	32	0x0000 0014	0x4A30 6314
RM_MPU_MPU_CONTEXT	RW	32	0x0000 0024	0x4A30 6324

3.11.4.2 MPU_PRM Register Description

Table 3-364. PM_MPU_PWRSTCTRL

Address Offset	0x0000 0000		
Physical Address	0x4A30 6300	**Instance**	MPU_PRM
Description	This register controls the MPU domain power state to reach upon a domain sleep transition		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								MPU_RAM_ONSTATE		MPU_L2_ONSTATE		RESERVED									MPU_RAM_RETSTATE	MPU_L2_RETSTATE	RESERVED				LOWPOWERSTATECHANGE	RESERVED		LOGICRETSTATE	POWERSTATE		

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Bits	Field Name	Description	Type	Reset
31:22	RESERVED		R	0x000
21:20	MPU_RAM_ONSTATE	MPU_RAM memory state when domain is ON. Read 0x3: Memory bank is on when the domain is ON.	R R returns 1s	0x3
19:18	MPU_L2_ONSTATE	MPU_L2 memory state when domain is ON. Read 0x3: Memory bank is on when the domain is ON.	R R returns 1s	0x3
17:11	RESERVED		R	0x00
10	MPU_RAM_RETSTATE	MPU_RAM memory state when domain is RETENTION. Read 0x1: Memory bank is retained when domain is in RETENTION state.	RO R returns 1s	1
9	MPU_L2_RETSTATE	MPU_L2 memory state when domain is RETENTION. 0x0: Memory bank is off when the domain is in the RETENTION state. 0x1: Memory bank is retained when domain is in RETENTION state.	RW	1
8:5	RESERVED		R	0x0
4	LOWPOWERSTATECHANGE	Power state change request when domain has already performed a sleep transition. Allows going into deeper low power state without waking up the power domain. 0x0: Do not request a low power state change. 0x1: Request a low power state change. This bit is automatically cleared when the power state is effectively changed or when power state is ON.	RW WSpecial	0
3	RESERVED		R	0
2	LOGICRETSTATE	Logic state when power domain is RETENTION 0x0: Only retention registers are retained and remaing logic is off when the domain is in RETENTION state. 0x1: Whole logic is retained when domain is in RETENTION state.	RW	1
1:0	POWERSTATE	Power state control. 0x0: OFF state 0x1: RETENTION state 0x2: INACTIVE state 0x3: ON State	RW	0x3

Table 3-365. Register Call Summary for Register PM_MPU_PWRSTCTRL

Power Management Functional Description • Power Domain Modes: [0] [1] [2] [3] [4] [5] [6] [7] [8]
PRCM Register Manual • MPU_PRM Register Summary: [9]

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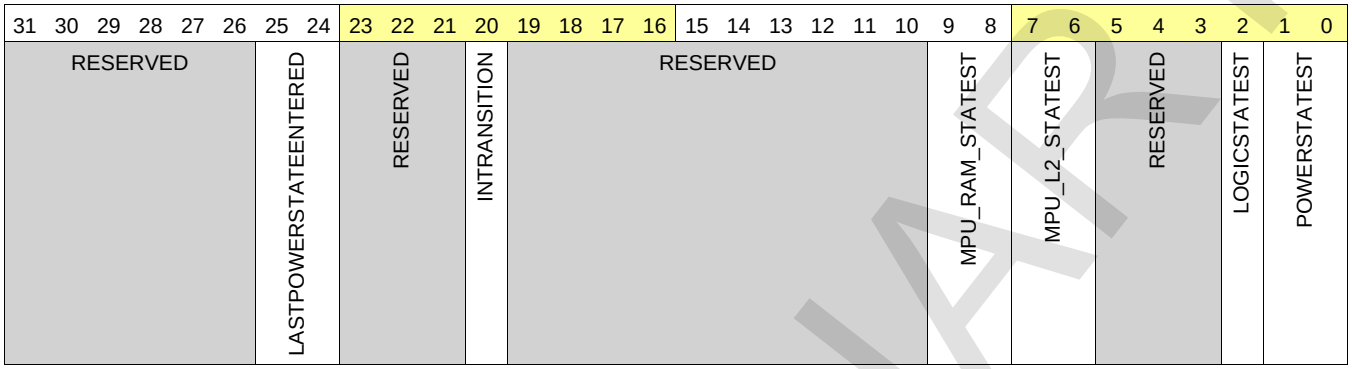
Table 3-366. PM_MPU_PWRSTST

Address Offset	0x0000 0004		
Physical Address	0x4A30 6304	**Instance**	MPU_PRM
Description	This register provides a status on the MPU domain current power state. [warm reset insensitive]		
Type	R		



Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x00
25:24	LASTPOWERSTATEENTERED	Last low power state entered. Set to 0x3 upon write of the same only. This register is intended for debug purpose only. Read 0x3: Power domain was previously ON-ACTIVE Read 0x2: Power domain was previously ON-INACTIVE Read 0x1: Power domain was previously in RETENTION Read 0x0: Power domain was previously OFF	RW W1toSet	0x0
23:21	RESERVED		R	0x0
20	INTRANSITION	Domain transition status Read 0x0: No ongoing transition on power domain Read 0x1: Power domain transition is in progress.	R	0
19:10	RESERVED		R	0x000
9:8	MPU_RAM_STATEST	MPU_RAM memory state status Read 0x0: Memory is OFF Read 0x1: Memory is RETENTION Read 0x2: Reserved Read 0x3: Memory is ON	R	0x3
7:6	MPU_L2_STATEST	MPU_L2 memory state status Read 0x0: Memory is OFF Read 0x1: Memory is RETENTION Read 0x2: Reserved Read 0x3: Memory is ON	R	0x3
5:3	RESERVED		R	0x0
2	LOGICSTATEST	Logic state status Read 0x0: Logic in domain is OFF Read 0x1: Logic in domain is ON	R	1
1:0	POWERSTATEST	Current power state status Read 0x0: Power domain is OFF Read 0x1: Power domain is in RETENTION Read 0x2: Power domain is ON-INACTIVE Read 0x3: Power domain is ON-ACTIVE	R	0x3

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Table 3-367. Register Call Summary for Register PM_MPU_PWRSTST

Power Management Functional Description • Power Domain Modes: [0] [1] [2] [3] [4] [5] [6]
PRCM Register Manual • MPU_PRM Register Summary: [7]

Table 3-368. RM_MPU_RSTST

Address Offset	0x0000 0014		
Physical Address	0x4A30 6314	**Instance**	MPU_PRM
Description	This register logs the different reset sources of the MPU domain. Each bit is set upon release of the domain reset signal. Must be cleared by software. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															EMULATION_RST

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	EMULATION_RST	MPU domain has been reset due to emulation reset source e.g. assert reset command initiated by the icepick module 0x0: No emulation reset 0x1: The domain has been reset upon emulation reset	RW W1toClr	0

Table 3-369. Register Call Summary for Register RM_MPU_RSTST

PRCM Register Manual • MPU_PRM Register Summary: [0]

Table 3-370. RM_MPU_MPU_CONTEXT

Address Offset	0x0000 0024		
Physical Address	0x4A30 6324	**Instance**	MPU_PRM
Description	This register contains dedicated MPU context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																					LOSTMEM_MPU_RAM	LOSTMEM_MPU_L2	RESERVED							LOSTCONTEXT_RFF	LOSTCONTEXT_DFF

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Bits	Field Name	Description	Type	Reset
31:11	RESERVED		R	0x000000
10	LOSTMEM_MPU_RAM	Specify if memory-based context in MPU_RAM memory bank has been lost due to a previous power transition or other reset source (not affected by a global warm reset). 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
9	LOSTMEM_MPU_L2	Specify if memory-based context in MPU_L2 memory bank has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
8:2	RESERVED		R	0x00
1	LOSTCONTEXT_RFF	Specify if RFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of MPU_MA_PWRON_RET_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of MPU_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-371. Register Call Summary for Register RM_MPU_MPU_CONTEXT

Power Management Functional Description • PD_MPU Description: [0]
PRCM Register Manual • MPU_PRM Register Summary: [1]

3.11.5 DSP_PRM Registers

3.11.5.1 DSP_PRM Register Summary

Table 3-372. DSP_PRM Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	DSP_PRM L4 Base Address
PM_DSP_PWRSTCTRL	RW	32	0x0000 0000	0x4A30 6400
PM_DSP_PWRSTST	R	32	0x0000 0004	0x4A30 6404
RM_DSP_RSTCTRL	RW	32	0x0000 0010	0x4A30 6410
RM_DSP_RSTST	RW	32	0x0000 0014	0x4A30 6414
RM_DSP_DSP_CONTEXT	RW	32	0x0000 0024	0x4A30 6424

3.11.5.2 DSP_PRM Register Description

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Table 3-373. PM_DSP_PWRSTCTRL

Address Offset	0x0000 0000		
Physical Address	0x4A30 6400	**Instance**	DSP_PRM
Description	This register controls the DSP power state to reach upon a domain sleep transition		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										DSP_EDMA_ONSTATE		DSP_L2_ONSTATE		DSP_L1_ONSTATE		RESERVED					DSP_EDMA_RETSTATE	DSP_L2_RETSTATE	DSP_L1_RETSTATE	RESERVED		LOWPOWERSTATECHANGE		RESERVED		LOGICRETSTATE		POWERSTATE	

Bits	Field Name	Description	Type	Reset
31:22	RESERVED		R	0x000
21:20	DSP_EDMA_ONSTATE	DSP_EDMA state when domain is ON. Read 0x3: Memory bank is on when the domain is ON.	R Rreturns 1s	0x3
19:18	DSP_L2_ONSTATE	DSP_L2 state when domain is ON. Read 0x3: Memory bank is on when the domain is ON.	R Rreturns 1s	0x3
17:16	DSP_L1_ONSTATE	DSP_L1 state when domain is ON. Read 0x3: Memory bank is on when the domain is ON.	R Rreturns 1s	0x3
15:11	RESERVED		R	0x00
10	DSP_EDMA_RETSTATE	DSP_EDMA state when domain is RETENTION. Read 0x1: Memory bank is retained when domain is in RETENTION state.	R Rreturns 1s	1
9	DSP_L2_RETSTATE	DSP_L2 state when domain is RETENTION. 0x0: Memory bank is off when the domain is in the RETENTION state. 0x1: Memory bank is retained when domain is in RETENTION state.	RW	1
8	DSP_L1_RETSTATE	DSP_L2 state when domain is RETENTION. 0x0: Memory bank is off when the domain is in the RETENTION state. 0x1: Memory bank is retained when domain is in RETENTION state.	RW	1
7:5	RESERVED		R	0x0
4	LOWPOWERSTATECHANGE	Power state change request when domain has already performed a sleep transition. Allows going into deeper low power state without waking up the power domain. 0x0: Do not request a low power state change. 0x1: Request a low power state change. This bit is automatically cleared when the power state is effectively changed or when power state is ON.	RW WSpecial	0
3	RESERVED		R	0

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Bits	Field Name	Description	Type	Reset
2	LOGICRETSTATE	Logic state when power domain is RETENTION 0x0: Only retention registers are retained and remaing logic is off when the domain is in RETENTION state. 0x1: Whole logic is retained when domain is in RETENTION state.	RW	1
1:0	POWERSTATE	Power state control 0x0: OFF state 0x1: RETENTION state 0x2: INACTIVE state 0x3: ON State	RW	0x3

Table 3-374. Register Call Summary for Register PM_DSP_PWRSTCTRL

Power Management Functional Description • Power Domain Modes: [0] [1] [2] [3] [4] [5] [6] [7] [8]
PRCM Register Manual • DSP_PRM Register Summary: [9]

Table 3-375. PM_DSP_PWRSTST

Address Offset	0x0000 0004		
Physical Address	0x4A30 6404	**Instance**	DSP_PRM
Description	This register provides a status on the DSP domain current power state. [warm reset insensitive]		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						LASTPOWERSTATEENTERED		RESERVED			INTRANSITION	RESERVED										DSP_EDMA_STATEST		DSP_L2_STATEST		DSP_L1_STATEST		RESERVED		LOGICSTATEST		POWERSTATEST	

Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x00
25:24	LASTPOWERSTATEENTERED	Last low power state entered. Set to 0x3 upon write of the same only. This register is intended for debug purpose only. Read 0x3: Power domain was previously ON-ACTIVE Read 0x2: Power domain was previously ON-INACTIVE Read 0x1: Power domain was previously in RETENTION Read 0x0: Power domain was previously OFF	RW W1toSet	0x0
23:21	RESERVED		R	0x0
20	INTRANSITION	Domain transition status Read 0x0: No ongoing transition on power domain Read 0x1: Power domain transition is in progress.	R	0
19:10	RESERVED		R	0x000

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Bits	Field Name	Description	Type	Reset
9:8	DSP_EDMA_STATEST	DSP_EDMA memory state status Read 0x0: Memory is OFF Read 0x1: Memory is RETENTION Read 0x2: Reserved Read 0x3: Memory is ON	R	0x3
7:6	DSP_L2_STATEST	DSP_L2 memory state status Read 0x0: Memory is OFF Read 0x1: Memory is RETENTION Read 0x2: Reserved Read 0x3: Memory is ON	R	0x3
5:4	DSP_L1_STATEST	DSP_L1 memory state status Read 0x0: Memory is OFF Read 0x1: Memory is RETENTION Read 0x2: Reserved Read 0x3: Memory is ON	R	0x3
3	RESERVED		R	0
2	LOGICSTATEST	Logic state status Read 0x0: Logic in domain is OFF Read 0x1: Logic in domain is ON	R	1
1:0	POWERSTATEST	Current power state status Read 0x0: Power domain is OFF Read 0x1: Power domain is in RETENTION Read 0x2: Power domain is ON-INACTIVE Read 0x3: Power domain is ON-ACTIVE	R	0x3

Table 3-376. Register Call Summary for Register PM_DSP_PWRSTST

Power Management Functional Description
- Power Domain Modes: [0] [1] [2] [3] [4] [5] [6]

PRCM Register Manual
- DSP_PRM Register Summary: [7]

Table 3-377. RM_DSP_RSTCTRL

Address Offset	0x0000 0010		
Physical Address	0x4A30 6410	**Instance**	DSP_PRM
Description	This register controls the release of the DSP sub-system resets.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														RST2	RST1

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	RST2	DSP - MMU, cache and slave interface reset control 0x0: Reset is cleared for the MMU, cache and slave interface 0x1: Reset is asserted for the MMU, cache and slave interface	RW	1

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Bits	Field Name	Description	Type	Reset
0	RST1	DSP - DSP reset control 0x0: Reset is cleared for the DSP - DSP 0x1: Reset is asserted for the DSP - DSP	RW	1

Table 3-378. Register Call Summary for Register RM_DSP_RSTCTRL

Reset Management Functional Description
- Reset Domains: [0]
- DSP Subsystem Power-On Reset Sequence: [1] [2]
- DSP Subsystem Software Warm Reset Sequence: [3] [4] [5] [6]

PRCM Register Manual
- DSP_PRM Register Summary: [7]

Table 3-379. RM_DSP_RSTST

Address Offset	0x0000 0014		
Physical Address	0x4A30 6414	**Instance**	DSP_PRM
Description	This register logs the different reset sources of the DSP domain. Each bit is set upon release of the domain reset signal. Must be cleared by software. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												DSP_DSP_EMU_REQ_RSTST	DSPSS_EMU_RSTST	RST2ST	RST1ST

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0000000
3	DSP_DSP_EMU_REQ_RSTST	DSP DSP processor has been reset due to DSP emulation reset request driven from DSPSS 0x0: No emulation reset 0x1: DSP DSP has been reset upon emulation reset request	RW W1toClr	0
2	DSPSS_EMU_RSTST	DSP domain has been reset due to emulation reset source e.g. assert reset command initiated by the icepick module 0x0: No emulation reset 0x1: DSP has been reset upon emulation reset	RW W1toClr	0
1	RST2ST	DSP MMU, cache and slave interface software reset status 0x0: No software reset occured 0x1: MMU, cache and slave interface has been reset upon software reset	RW W1toClr	0
0	RST1ST	DSP DSP software reset 0x0: No software reset occured 0x1: DSP has been reset upon software reset	RW W1toClr	0

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Table 3-380. Register Call Summary for Register RM_DSP_RSTST

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- DSP_PRM Register Summary: [0]

Table 3-381. RM_DSP_DSP_CONTEXT

Address Offset	0x0000 0024		
Physical Address	0x4A30 6424	**Instance**	DSP_PRM
Description	This register contains dedicated DSP context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																					LOSTMEM_DSP_EDMA	LOSTMEM_DSP_L2	LOSTMEM_DSP_L1	RESERVED						LOSTCONTEXT_RFF	LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:11	RESERVED		R	0x000000
10	LOSTMEM_DSP_EDMA	Specify if memory-based context in DSP_EDMA memory bank has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
9	LOSTMEM_DSP_L2	Specify if memory-based context in DSP_L2 memory bank has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
8	LOSTMEM_DSP_L1	Specify if memory-based context in DSP_L1 memory bank has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
7:2	RESERVED		R	0x00
1	LOSTCONTEXT_RFF	Specify if RFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of DSP_RET_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of DSP_SYS_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

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Table 3-382. Register Call Summary for Register RM_DSP_DSP_CONTEXT

Power Management Functional Description • PD_DSP Description: [0] [1]
PRCM Register Manual • DSP_PRM Register Summary: [2]

3.11.6 ABE_PRM Registers

3.11.6.1 ABE_PRM Register Summary

Table 3-383. ABE_PRM Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	ABE_PRM L4 Base Address
PM_ABE_PWRSTCTRL	RW	32	0x0000 0000	0x4A30 6500
PM_ABE_PWRSTST	R	32	0x0000 0004	0x4A30 6504
RM_ABE_AESS_CONTEXT	RW	32	0x0000 002C	0x4A30 652C
PM_ABE_PDM_WKDEP	RW	32	0x0000 0030	0x4A30 6530
RM_ABE_PDM_CONTEXT	RW	32	0x0000 0034	0x4A30 6534
PM_ABE_DMIC_WKDEP	RW	32	0x0000 0038	0x4A30 6538
RM_ABE_DMIC_CONTEXT	RW	32	0x0000 003C	0x4A30 653C
PM_ABE_MCASP_WKDEP	RW	32	0x0000 0040	0x4A30 6540
RM_ABE_MCASP_CONTEXT	RW	32	0x0000 0044	0x4A30 6544
PM_ABE_MCBSP1_WKDEP	RW	32	0x0000 0048	0x4A30 6548
RM_ABE_MCBSP1_CONTEXT	RW	32	0x0000 004C	0x4A30 654C
PM_ABE_MCBSP2_WKDEP	RW	32	0x0000 0050	0x4A30 6550
RM_ABE_MCBSP2_CONTEXT	RW	32	0x0000 0054	0x4A30 6554
PM_ABE_MCBSP3_WKDEP	RW	32	0x0000 0058	0x4A30 6558
RM_ABE_MCBSP3_CONTEXT	RW	32	0x0000 005C	0x4A30 655C
PM_ABE_SLIMBUS_WKDEP	RW	32	0x0000 0060	0x4A30 6560
RM_ABE_SLIMBUS_CONTEXT	RW	32	0x0000 0064	0x4A30 6564
PM_ABE_GPTIMER5_WKDEP	RW	32	0x0000 0068	0x4A30 6568
RM_ABE_GPTIMER5_CONTEXT	RW	32	0x0000 006C	0x4A30 656C
PM_ABE_GPTIMER6_WKDEP	RW	32	0x0000 0070	0x4A30 6570
RM_ABE_GPTIMER6_CONTEXT	RW	32	0x0000 0074	0x4A30 6574
PM_ABE_GPTIMER7_WKDEP	RW	32	0x0000 0078	0x4A30 6578
RM_ABE_GPTIMER7_CONTEXT	RW	32	0x0000 007C	0x4A30 657C
PM_ABE_GPTIMER8_WKDEP	RW	32	0x0000 0080	0x4A30 6580
RM_ABE_GPTIMER8_CONTEXT	RW	32	0x0000 0084	0x4A30 6584
PM_ABE_WDTIMER3_WKDEP	R	32	0x0000 0088	0x4A30 6588
RM_ABE_WDTIMER3_CONTEXT	RW	32	0x0000 008C	0x4A30 658C

3.11.6.2 ABE_PRM Register Description

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Table 3-384. PM_ABE_PWRSTCTRL

Address Offset	0x0000 0000		
Physical Address	0x4A30 6500	**Instance**	ABE_PRM
Description	This register controls the ABE domain power state to reach upon a domain sleep transition		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										PERIPHMEM_ONSTATE		RESERVED		AESSMEM_ONSTATE		RESERVED					PERIPHMEM_RETSTATE	RESERVED		AESSMEM_RETSTATE		RESERVED		LOWPOWERSTATECHANGE		RESERVED		LOGICRETSTATE		POWERSTATE	

Bits	Field Name	Description	Type	Reset
31:22	RESERVED		R	0x000
21:20	PERIPHMEM_ONSTATE	PERIPHMEM memory state when domain is ON. Read 0x3: Memory bank is on when the domain is ON.	R Rreturns 1s	0x3
19:18	RESERVED		R	0x0
17:16	AESSMEM_ONSTATE	AESSMEM memory state when domain is ON. Read 0x3: Memory bank is on when the domain is ON.	R Rreturns 1s	0x3
15:11	RESERVED		R	0x00
10	PERIPHMEM_RETSTATE	PERIPHMEM memory state when domain is RETENTION. Read 0x0: Memory bank is off when the domain is in the RETENTION state.	R	0
9	RESERVED		R	0
8	AESSMEM_RETSTATE	AESSMEM memory state when domain is RETENTION. Read 0x1: Memory bank is retained when domain is in RETENTION state.	R Rreturns 1s	1
7:5	RESERVED		R	0x0
4	LOWPOWERSTATECHANGE	Power state change request when domain has already performed a sleep transition. Allows going into deeper low power state without waking up the power domain. 0x0: Do not request a low power state change. 0x1: Request a low power state change. This bit is automatically cleared when the power state is effectively changed or when power state is ON.	RW WSpecial	0
3	RESERVED		R	0
2	LOGICRETSTATE	Logic state when power domain is RETENTION Read 0x0: Whole logic is off when the domain is in RETENTION state.	R	0
1:0	POWERSTATE	Power state control 0x0: OFF state 0x1: RETENTION state 0x2: INACTIVE state 0x3: ON State	RW	0x0

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Table 3-385. Register Call Summary for Register PM_ABE_PWRSTCTRL

Power Management Functional Description
- Power Domain Modes: [0] [1] [2] [3] [4] [5] [6]

PRCM Register Manual
- ABE_PRM Register Summary: [7]

Table 3-386. PM_ABE_PWRSTST

Address Offset	0x0000 0004		
Physical Address	0x4A30 6504	**Instance**	ABE_PRM
Description	This register provides a status on the ABE domain current power domain state. [warm reset insensitive]		
Type	R		

31 30 29 28 27 26	25 24	23 22 21	20	19 18 17 16	15 14 13 12 11 10	9 8	7 6	5 4	3	2	1 0
RESERVED	LASTPOWERSTATEENTERED	RESERVED	INTRANSITION	RESERVED		PERIPHMEM_STATEST	RESERVED	AESSMEM_STATEST	RESERVED	LOGICSTATEST	POWERSTATEST

Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x00
25:24	LASTPOWERSTATEENTERED	Last low power state entered. Set to 0x3 upon write of the same only. This register is intended for debug purpose only. Read 0x3: Power domain was previously ON-ACTIVE Read 0x2: Power domain was previously ON-INACTIVE Read 0x1: Power domain was previously in RETENTION Read 0x0: Power domain was previously OFF	RW W1toSet	0x0
23:21	RESERVED		R	0x0
20	INTRANSITION	Domain transition status Read 0x0: No ongoing transition on power domain Read 0x1: Power domain transition is in progress.	R	0
19:10	RESERVED		R	0x000
9:8	PERIPHMEM_STATEST	PERIPHMEM memory state status Read 0x0: Memory is OFF Read 0x1: Reserved Read 0x2: Reserved Read 0x3: Memory is ON	R	0x3
7:6	RESERVED		R	0x0
5:4	AESSMEM_STATEST	AESSMEM memory state status Read 0x0: Memory is OFF Read 0x1: Memory is RETENTION Read 0x2: Reserved Read 0x3: Memory is ON	R	0x3
3	RESERVED		R	0

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Bits	Field Name	Description	Type	Reset
2	LOGICSTATEST	Logic state status Read 0x0: Logic in domain is OFF Read 0x1: Logic in domain is ON	R	1
1:0	POWERSTATEST	Current power state status Read 0x0: Power domain is OFF Read 0x1: Power domain is in RETENTION Read 0x2: Power domain is ON-INACTIVE Read 0x3: Power domain is ON-ACTIVE	R	0x3

Table 3-387. Register Call Summary for Register PM_ABE_PWRSTST

Power Management Functional Description • Power Domain Modes: [0] [1] [2] [3] [4] [5]
PRCM Register Manual • ABE_PRM Register Summary: [6]

Table 3-388. RM_ABE_AESS_CONTEXT

Address Offset	0x0000 002C		
Physical Address	0x4A30 652C	**Instance**	ABE_PRM
Description	This register contains dedicated AESS context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							LOSTMEM_AESSMEM	RESERVED							LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	LOSTMEM_AESSMEM	Specify if memory-based context in AESSMEM memory bank has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
7:1	RESERVED		R	0x00
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of AUDIO_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-389. Register Call Summary for Register RM_ABE_AESS_CONTEXT

Power Management Functional Description • PD_AUDIO Description: [0]
PRCM Register Manual • ABE_PRM Register Summary: [1]

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Table 3-390. PM_ABE_PDM_WKDEP

Address Offset	0x0000 0030		
Physical Address	0x4A30 6530	**Instance**	ABE_PRM
Description	This register controls wakeup dependency based on PDM service requests.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								WKUPDEP_PDM_DMA_SDMA	WKUPDEP_PDM_DMA_DSP	RESERVED			WKUPDEP_PDM_IRQ_DSP	RESERVED	WKUPDEP_PDM_IRQ_MPU

Bits	Field Name	Description	Type	Reset
31:8	RESERVED		R	0x000000
7	WKUPDEP_PDM_DMA_SDMA	Wakeup dependency from PDM module (softwareakeup_dma signal) towards SDMA + L3_2 + L3_1 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
6	WKUPDEP_PDM_DMA_DSP	Wakeup dependency from PDM module (softwareakeup_dma signal) towards DSP domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
5:3	RESERVED		R	0x0
2	WKUPDEP_PDM_IRQ_DSP	Wakeup dependency from PDM module (softwareakeup_irq signal) towards DSP domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
1	RESERVED		R	0
0	WKUPDEP_PDM_IRQ_MPU	Wakeup dependency from PDM module (softwareakeup_irq signal) towards MPU domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-391. Register Call Summary for Register PM_ABE_PDM_WKDEP

Clock Management Functional Description
- Clock Domain Dependency: [0] [1] [2] [3]

PRCM Register Manual
- ABE_PRM Register Summary: [4]

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Table 3-392. RM_ABE_PDM_CONTEXT

Address Offset	0x0000 0034		
Physical Address	0x4A30 6534	**Instance**	ABE_PRM
Description	This register contains dedicated PDM context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							LOSTMEM_PERIHPMEM	RESERVED							LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	LOSTMEM_PERIHPMEM	Specify if memory-based context in PERIHPMEM memory bank has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
7:1	RESERVED		R	0x00
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of AUDIO_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-393. Register Call Summary for Register RM_ABE_PDM_CONTEXT

Power Management Functional Description • PD_AUDIO Description: [0]
PRCM Register Manual • ABE_PRM Register Summary: [1]

Table 3-394. PM_ABE_DMIC_WKDEP

Address Offset	0x0000 0038		
Physical Address	0x4A30 6538	**Instance**	ABE_PRM
Description	This register controls wakeup dependency based on DMIC service requests.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								WKUPDEP_DMIC_DMA_SDMA	WKUPDEP_DMIC_DMA_DSP	RESERVED			WKUPDEP_DMIC_IRQ_DSP	RESERVED	WKUPDEP_DMIC_IRQ_MPU

Bits	Field Name	Description	Type	Reset
31:8	RESERVED		R	0x000000
7	WKUPDEP_DMIC_DMA_SDMA	Wakeup dependency from DMIC module (softwareakeup_dma signal) towards SDMA + L3_2 + L3_1 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
6	WKUPDEP_DMIC_DMA_DSP	Wakeup dependency from DMIC module (softwareakeup_dma signal) towards DSP domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
5:3	RESERVED		R	0x0
2	WKUPDEP_DMIC_IRQ_DSP	Wakeup dependency from DMIC module (softwareakeup_irq signal) towards DSP domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
1	RESERVED		R	0
0	WKUPDEP_DMIC_IRQ_MPU	Wakeup dependency from DMIC module (softwareakeup_irq signal) towards MPU domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-395. Register Call Summary for Register PM_ABE_DMIC_WKDEP

Clock Management Functional Description • Clock Domain Dependency: [0] [1] [2] [3]
PRCM Register Manual • ABE_PRM Register Summary: [4]

Table 3-396. RM_ABE_DMIC_CONTEXT

Address Offset	0x0000 003C		
Physical Address	0x4A30 653C	**Instance**	ABE_PRM
Description	This register contains dedicated DMIC context statuses. [warm reset insensitive]		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								LOSTMEM_PERIHPMEM	RESERVED						LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	LOSTMEM_PERIHPMEM	Specify if memory-based context in PERIHPMEM memory bank has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
7:1	RESERVED		R	0x00
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of AUDIO_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-397. Register Call Summary for Register RM_ABE_DMIC_CONTEXT

Power Management Functional Description • PD_AUDIO Description: [0]
PRCM Register Manual • ABE_PRM Register Summary: [1]

Table 3-398. PM_ABE_MCASP_WKDEP

Address Offset	0x0000 0040		
Physical Address	0x4A30 6540	**Instance**	ABE_PRM
Description	This register controls wakeup dependency based on MCASP service requests.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								WKUPDEP_MCASP1_DMA_SDMA	WKUPDEP_MCASP1_DMA_DSP	RESERVED			WKUPDEP_MCASP1_IRQ_DSP	RESERVED	WKUPDEP_MCASP1_IRQ_MPU

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Bits	Field Name	Description	Type	Reset
31:8	RESERVED		R	0x000000
7	WKUPDEP_MCASP1_DMA_SDMA	Wakeup dependency from MCASP1 module (softwareakeup_dma signal) towards SDMA + L3_2 + L3_1 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
6	WKUPDEP_MCASP1_DMA_DSP	Wakeup dependency from MCASP1 module (softwareakeup_dma signal) towards DSP domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
5:3	RESERVED		R	0x0
2	WKUPDEP_MCASP1_IRQ_DSP	Wakeup dependency from MCASP1 module (softwareakeup_irq signal) towards DSP domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
1	RESERVED		R	0
0	WKUPDEP_MCASP1_IRQ_MPU	Wakeup dependency from MCASP1 module (softwareakeup_irq signal) towards MPU domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-399. Register Call Summary for Register PM_ABE_MCASP_WKDEP

Clock Management Functional Description
- Clock Domain Dependency: [0] [1] [2] [3]

PRCM Register Manual
- ABE_PRM Register Summary: [4]

Table 3-400. RM_ABE_MCASP_CONTEXT

Address Offset	0x0000 0044		
Physical Address	0x4A30 6544	**Instance**	ABE_PRM
Description	This register contains dedicated MCASP context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of AUDIO_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

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Table 3-401. Register Call Summary for Register RM_ABE_MCASP_CONTEXT

Power Management Functional Description • PD_AUDIO Description: [0]
PRCM Register Manual • ABE_PRM Register Summary: [1]

Table 3-402. PM_ABE_MCBSP1_WKDEP

Address Offset	0x0000 0048		
Physical Address	0x4A30 6548	**Instance**	ABE_PRM
Description	This register controls wakeup dependency based on MCBSP1 service requests.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												WKUPDEP_MCBSP1_SDMA	WKUPDEP_MCBSP1_DSP	RESERVED	WKUPDEP_MCBSP1_MPU

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0000000
3	WKUPDEP_MCBSP1_SDMA	Wakeup dependency from MCBSP1 module (softwareakeup signal) towards SDMA + L3_2 + L3_1 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
2	WKUPDEP_MCBSP1_DSP	Wakeup dependency from MCBSP1 module (softwareakeup signal) towards DSP domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
1	RESERVED		R	0
0	WKUPDEP_MCBSP1_MPU	Wakeup dependency from MCBSP1 module (softwareakeup signal) towards MPU domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-403. Register Call Summary for Register PM_ABE_MCBSP1_WKDEP

Clock Management Functional Description • Clock Domain Dependency: [0] [1] [2]
PRCM Register Manual • ABE_PRM Register Summary: [3]

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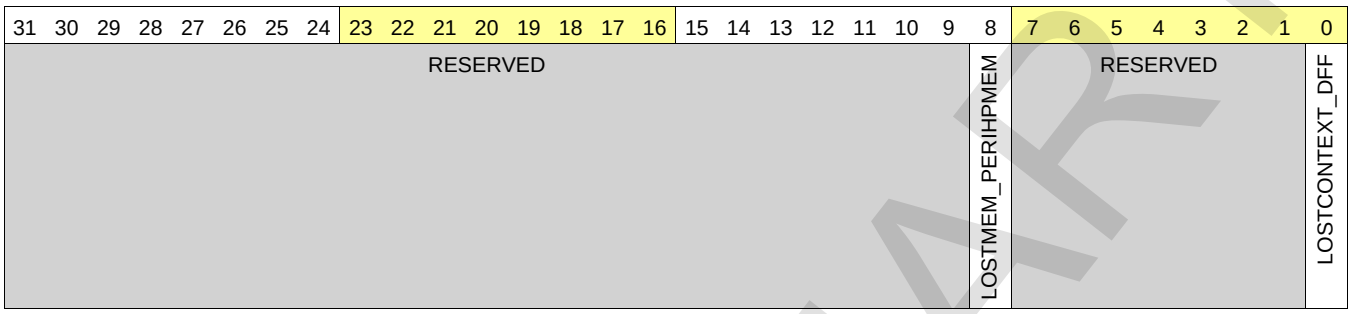
Table 3-404. RM_ABE_MCBSP1_CONTEXT

Address Offset	0x0000 004C		
Physical Address	0x4A30 654C	**Instance**	ABE_PRM
Description	This register contains dedicated MCBSP1 context statuses. [warm reset insensitive]		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	LOSTMEM_PERIHPMEM	Specify if memory-based context in PERIHPMEM memory bank has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
7:1	RESERVED		R	0x00
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of AUDIO_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-405. Register Call Summary for Register RM_ABE_MCBSP1_CONTEXT

Power Management Functional Description • PD_AUDIO Description: [0]
PRCM Register Manual • ABE_PRM Register Summary: [1]

Table 3-406. PM_ABE_MCBSP2_WKDEP

Address Offset	0x0000 0050		
Physical Address	0x4A30 6550	**Instance**	ABE_PRM
Description	This register controls wakeup dependency based on MCBSP2 service requests.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												WKUPDEP_MCBSP2_SDMA	WKUPDEP_MCBSP2_DSP	RESERVED	WKUPDEP_MCBSP2_MPU

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0000000
3	WKUPDEP_MCBSP2_SDMA	Wakeup dependency from MCBSP2 module (softwareakeup signal) towards SDMA + L3_2 + L3_1 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
2	WKUPDEP_MCBSP2_DSP	Wakeup dependency from MCBSP2 module (softwareakeup signal) towards DSP domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
1	RESERVED		R	0
0	WKUPDEP_MCBSP2_MPU	Wakeup dependency from MCBSP2 module (softwareakeup signal) towards MPU domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-407. Register Call Summary for Register PM_ABE_MCBSP2_WKDEP

Clock Management Functional Description • Clock Domain Dependency: [0] [1] [2]
PRCM Register Manual • ABE_PRM Register Summary: [3]

Table 3-408. RM_ABE_MCBSP2_CONTEXT

Address Offset	0x0000 0054		
Physical Address	0x4A30 6554	**Instance**	ABE_PRM
Description	This register contains dedicated MCBSP2 context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							LOSTMEM_PERIHPMEM	RESERVED							LOSTCONTEXT_DFF

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Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	LOSTMEM_PERIHPMEM	Specify if memory-based context in PERIHPMEM memory bank has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
7:1	RESERVED		R	0x00
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of AUDIO_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-409. Register Call Summary for Register RM_ABE_MCBSP2_CONTEXT

Power Management Functional Description • PD_AUDIO Description: [0]
PRCM Register Manual • ABE_PRM Register Summary: [1]

Table 3-410. PM_ABE_MCBSP3_WKDEP

Address Offset	0x0000 0058		
Physical Address	0x4A30 6558	**Instance**	ABE_PRM
Description	This register controls wakeup dependency based on MCBSP3 service requests.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												WKUPDEP_MCBSP3_SDMA	WKUPDEP_MCBSP3_DSP	RESERVED	WKUPDEP_MCBSP3_MPU

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0000000
3	WKUPDEP_MCBSP3_SDMA	Wakeup dependency from MCBSP3 module (softwareakeup signal) towards SDMA + L3_2 + L3_1 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
2	WKUPDEP_MCBSP3_DSP	Wakeup dependency from MCBSP3 module (softwareakeup signal) towards DSP domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
1	RESERVED		R	0

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Bits	Field Name	Description	Type	Reset
0	WKUPDEP_MCBSP3_MPU	Wakeup dependency from MCBSP3 module (softwareakeup signal) towards MPU domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-411. Register Call Summary for Register PM_ABE_MCBSP3_WKDEP

Clock Management Functional Description • Clock Domain Dependency: [0] [1] [2]
PRCM Register Manual • ABE_PRM Register Summary: [3]

Table 3-412. RM_ABE_MCBSP3_CONTEXT

Address Offset	0x0000 005C		
Physical Address	0x4A30 655C	**Instance**	ABE_PRM
Description	This register contains dedicated MCBSP3 context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							LOSTMEM_PERIHPMEM	RESERVED							LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	LOSTMEM_PERIHPMEM	Specify if memory-based context in PERIHPMEM memory bank has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
7:1	RESERVED		R	0x00
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of AUDIO_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-413. Register Call Summary for Register RM_ABE_MCBSP3_CONTEXT

Power Management Functional Description • PD_AUDIO Description: [0]
PRCM Register Manual • ABE_PRM Register Summary: [1]

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Table 3-414. PM_ABE_SLIMBUS_WKDEP

Address Offset	0x0000 0060		
Physical Address	0x4A30 6560	**Instance**	ABE_PRM
Description	This register controls wakeup dependency based on SLIMBUS service requests.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								WKUPDEP_SLIMBUS1_DMA_SDMA	WKUPDEP_SLIMBUS1_DMA_DSP	RESERVED			WKUPDEP_SLIMBUS1_IRQ_DSP	RESERVED	WKUPDEP_SLIMBUS1_IRQ_MPU

Bits	Field Name	Description	Type	Reset
31:8	RESERVED		R	0x000000
7	WKUPDEP_SLIMBUS1_DMA_SDMA	Wakeup dependency from SLIMBUS1 module (softwareakeup_dma signal) towards SDMA + L3_2 + L3_1 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
6	WKUPDEP_SLIMBUS1_DMA_DSP	Wakeup dependency from SLIMBUS1 module (softwareakeup_dma signal) towards DSP domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
5:3	RESERVED		R	0x0
2	WKUPDEP_SLIMBUS1_IRQ_DSP	Wakeup dependency from SLIMBUS1 module (softwareakeup_irq signal) towards DSP domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
1	RESERVED		R	0
0	WKUPDEP_SLIMBUS1_IRQ_MPU	Wakeup dependency from SLIMBUS1 module (softwareakeup_irq signal) towards MPU domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-415. Register Call Summary for Register PM_ABE_SLIMBUS_WKDEP

Clock Management Functional Description
- Clock Domain Dependency: [0] [1] [2] [3]

PRCM Register Manual
- ABE_PRM Register Summary: [4]

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Table 3-416. RM_ABE_SLIMBUS_CONTEXT

Address Offset	0x0000 0064		
Physical Address	0x4A30 6564	**Instance**	ABE_PRM
Description	This register contains dedicated SLIMBUS context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							LOSTMEM_PERIHPMEM	RESERVED							LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	LOSTMEM_PERIHPMEM	Specify if memory-based context in PERIHPMEM memory bank has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
7:1	RESERVED		R	0x00
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of AUDIO_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-417. Register Call Summary for Register RM_ABE_SLIMBUS_CONTEXT

Power Management Functional Description • PD_AUDIO Description: [0]
PRCM Register Manual • ABE_PRM Register Summary: [1]

Table 3-418. PM_ABE_GPTIMER5_WKDEP

Address Offset	0x0000 0068		
Physical Address	0x4A30 6568	**Instance**	ABE_PRM
Description	This register controls wakeup dependency based on TIMER5 service requests.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													WKUPDEP_TIMER5_DSP	RESERVED	WKUPDEP_TIMER5_MPU

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Bits	Field Name	Description	Type	Reset
31:3	RESERVED		R	0x0000 0000
2	WKUPDEP_TIMER5_DSP	Wakeup dependency from TIMER5 module (softwareakeup signal) towards DSP domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
1	RESERVED		R	0
0	WKUPDEP_TIMER5_MPU	Wakeup dependency from TIMER5 module (softwareakeup signal) towards MPU domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-419. Register Call Summary for Register PM_ABE_GPTIMER5_WKDEP

Clock Management Functional Description • Clock Domain Dependency: [0] [1]
PRCM Register Manual • ABE_PRM Register Summary: [2]

Table 3-420. RM_ABE_GPTIMER5_CONTEXT

Address Offset	0x0000 006C		
Physical Address	0x4A30 656C	**Instance**	ABE_PRM
Description	This register contains dedicated TIMER5 context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of AUDIO_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-421. Register Call Summary for Register RM_ABE_GPTIMER5_CONTEXT

Power Management Functional Description • PD_AUDIO Description: [0]
PRCM Register Manual • ABE_PRM Register Summary: [1]

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Table 3-422. PM_ABE_GPTIMER6_WKDEP

Address Offset	0x0000 0070		
Physical Address	0x4A30 6570	**Instance**	ABE_PRM
Description	This register controls wakeup dependency based on TIMER6 service requests.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													WKUPDEP_TIMER6_DSP	RESERVED	WKUPDEP_TIMER6_MPU

Bits	Field Name	Description	Type	Reset
31:3	RESERVED		R	0x0000 0000
2	WKUPDEP_TIMER6_DSP	Wakeup dependency from TIMER6 module (softwareakeup signal) towards DSP domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
1	RESERVED		R	0
0	WKUPDEP_TIMER6_MPU	Wakeup dependency from TIMER6 module (softwareakeup signal) towards MPU domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-423. Register Call Summary for Register PM_ABE_GPTIMER6_WKDEP

Clock Management Functional Description • Clock Domain Dependency: [0] [1]
PRCM Register Manual • ABE_PRM Register Summary: [2]

Table 3-424. RM_ABE_GPTIMER6_CONTEXT

Address Offset	0x0000 0074		
Physical Address	0x4A30 6574	**Instance**	ABE_PRM
Description	This register contains dedicated TIMER6 context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															LOSTCONTEXT_DFF

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Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of AUDIO_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-425. Register Call Summary for Register RM_ABE_GPTIMER6_CONTEXT

Power Management Functional Description • PD_AUDIO Description: [0]
PRCM Register Manual • ABE_PRM Register Summary: [1]

Table 3-426. PM_ABE_GPTIMER7_WKDEP

Address Offset	0x0000 0078		
Physical Address	0x4A30 6578	**Instance**	ABE_PRM
Description	This register controls wakeup dependency based on TIMER7 service requests.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													WKUPDEP_TIMER7_DSP	RESERVED	WKUPDEP_TIMER7_MPU

Bits	Field Name	Description	Type	Reset
31:3	RESERVED		R	0x0000 0000
2	WKUPDEP_TIMER7_DSP	Wakeup dependency from TIMER7 module (softwareakeup signal) towards DSP domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
1	RESERVED		R	0
0	WKUPDEP_TIMER7_MPU	Wakeup dependency from TIMER7 module (softwareakeup signal) towards MPU domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-427. Register Call Summary for Register PM_ABE_GPTIMER7_WKDEP

Clock Management Functional Description • Clock Domain Dependency: [0] [1]
PRCM Register Manual • ABE_PRM Register Summary: [2]

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Table 3-428. RM_ABE_GPTIMER7_CONTEXT

Address Offset	0x0000 007C		
Physical Address	0x4A30 657C	**Instance**	ABE_PRM
Description	This register contains dedicated TIMER7 context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of AUDIO_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-429. Register Call Summary for Register RM_ABE_GPTIMER7_CONTEXT

Power Management Functional Description • PD_AUDIO Description: [0]
PRCM Register Manual • ABE_PRM Register Summary: [1]

Table 3-430. PM_ABE_GPTIMER8_WKDEP

Address Offset	0x0000 0080		
Physical Address	0x4A30 6580	**Instance**	ABE_PRM
Description	This register controls wakeup dependency based on TIMER8 service requests.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													WKUPDEP_TIMER8_DSP	RESERVED	WKUPDEP_TIMER8_MPU

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Bits	Field Name	Description	Type	Reset
31:3	RESERVED		R	0x0000 0000
2	WKUPDEP_TIMER8_DSP	Wakeup dependency from TIMER8 module (softwareakeup signal) towards DSP domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
1	RESERVED		R	0
0	WKUPDEP_TIMER8_MPU	Wakeup dependency from TIMER8 module (softwareakeup signal) towards MPU domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-431. Register Call Summary for Register PM_ABE_GPTIMER8_WKDEP

Clock Management Functional Description • Clock Domain Dependency: [0] [1]
PRCM Register Manual • ABE_PRM Register Summary: [2]

Table 3-432. RM_ABE_GPTIMER8_CONTEXT

Address Offset	0x0000 0084		
Physical Address	0x4A30 6584	**Instance**	ABE_PRM
Description	This register contains dedicated TIMER8 context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of AUDIO_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-433. Register Call Summary for Register RM_ABE_GPTIMER8_CONTEXT

Power Management Functional Description • PD_AUDIO Description: [0]
PRCM Register Manual • ABE_PRM Register Summary: [1]

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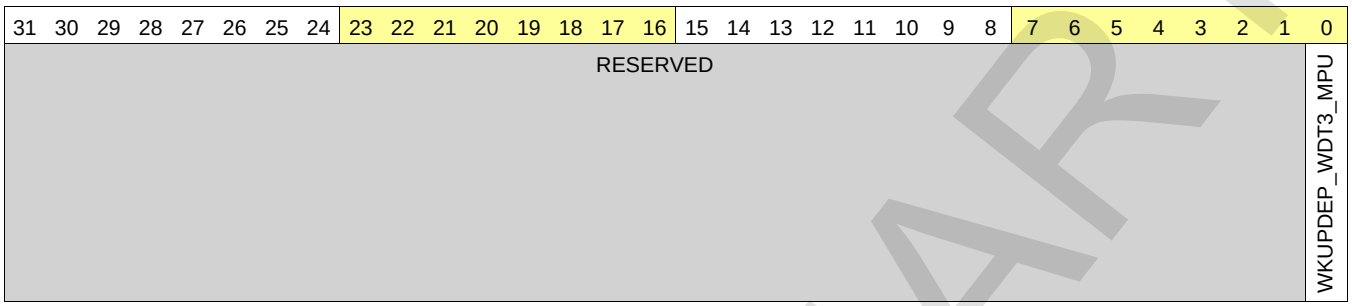
Table 3-434. PM_ABE_WDTIMER3_WKDEP

Address Offset	0x0000 0088		
Physical Address	0x4A30 6588	**Instance**	ABE_PRM
Description	This register controls wakeup dependency based on WDT3 service requests.		
Type	R		



Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	WKUPDEP_WDT3_MPU	Wakeup dependency from WDT3 module (softwareakeup signal) towards MPU domain Read 0x1: Dependency is enabled	R Rreturns 1s	1

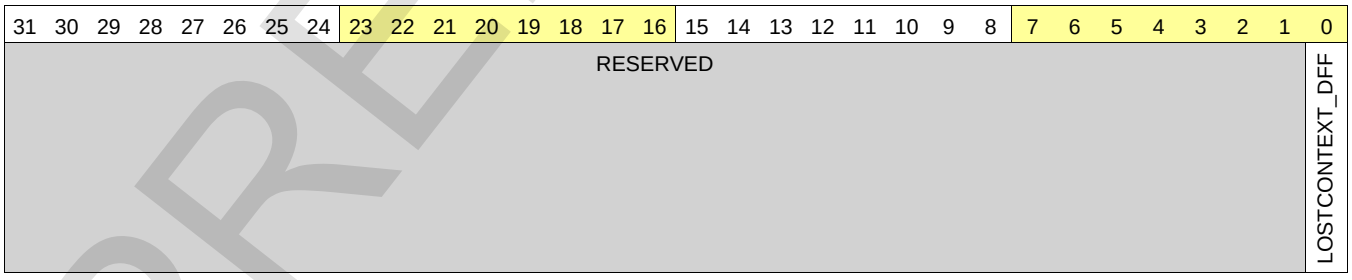
Table 3-435. Register Call Summary for Register PM_ABE_WDTIMER3_WKDEP

Clock Management Functional Description
- Clock Domain Dependency: [0]

PRCM Register Manual
- ABE_PRM Register Summary: [1]

Table 3-436. RM_ABE_WDTIMER3_CONTEXT

Address Offset	0x0000 008C		
Physical Address	0x4A30 658C	**Instance**	ABE_PRM
Description	This register contains dedicated WDT3 context statuses. [warm reset insensitive]		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of AUDIO_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

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Table 3-437. Register Call Summary for Register RM_ABE_WDTIMER3_CONTEXT

Power Management Functional Description • PD_AUDIO Description: [0]
PRCM Register Manual • ABE_PRM Register Summary: [1]

3.11.7 ALWAYS_ON_PRM Registers

3.11.7.1 ALWAYS_ON_PRM Register Summary

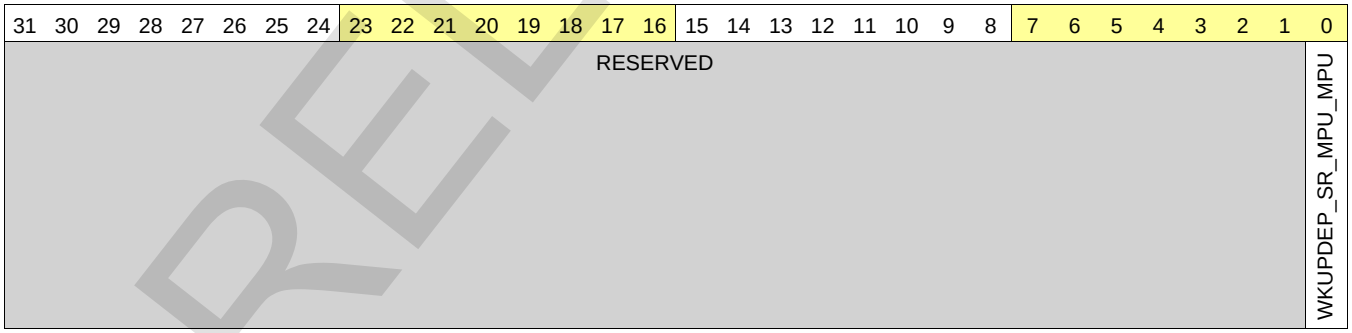
Table 3-438. ALWAYS_ON_PRM Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	ALWAYS_ON_PRM L4 Base Address
RESERVED	RW	32	0x0000 0024	0x4A30 6624
PM_ALWON_SR_MPU_WKDEP	R	32	0x0000 0028	0x4A30 6628
RM_ALWON_SR_MPU_CONTEXT	RW	32	0x0000 002C	0x4A30 662C
PM_ALWON_SR_IVA_WKDEP	RW	32	0x0000 0030	0x4A30 6630
RM_ALWON_SR_IVA_CONTEXT	RW	32	0x0000 0034	0x4A30 6634
PM_ALWON_SR_CORE_WKDEP	RW	32	0x0000 0038	0x4A30 6638
RM_ALWON_SR_CORE_CONTEXT	RW	32	0x0000 003C	0x4A30 663C

3.11.7.2 ALWAYS_ON_PRM Register Description

Table 3-439. PM_ALWON_SR_MPU_WKDEP

Address Offset	0x0000 0028		
Physical Address	0x4A30 6628	**Instance**	ALWAYS_ON_PRM
Description	This register controls wakeup dependency based on SR_MPU service requests.		
Type	R		



Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	WKUPDEP_SR_MPU_MPU	Wakeup dependency from SR_MPU module (softwareakeup signal) towards MPU + L3_1 + L4_CFG domains Read 0x1: Dependency is enabled	R Rreturns 1s	1

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Table 3-440. Register Call Summary for Register PM_ALWON_SR_MPU_WKDEP

Clock Management Functional Description • Clock Domain Dependency: [0]
PRCM Register Manual • ALWAYS_ON_PRM Register Summary: [1]

Table 3-441. RM_ALWON_SR_MPU_CONTEXT

Address Offset	0x0000 002C		
Physical Address	0x4A30 662C	**Instance**	ALWAYS_ON_PRM
Description	This register contains dedicated SR_MPU context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of Always_on_CORE_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-442. Register Call Summary for Register RM_ALWON_SR_MPU_CONTEXT

Power Management Functional Description • PD_ALWON_CORE Description: [0]
PRCM Register Manual • ALWAYS_ON_PRM Register Summary: [1]

Table 3-443. PM_ALWON_SR_IVA_WKDEP

Address Offset	0x0000 0030		
Physical Address	0x4A30 6630	**Instance**	ALWAYS_ON_PRM
Description	This register controls wakeup dependency based on SR_IVA service requests.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														WKUPDEP_SR_IVA_MPU_M3	WKUPDEP_SR_IVA_MPU

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	WKUPDEP_SR_IVA_MPU_M3	Wakeup dependency from SR_IVA module (softwareakeup signal) towards MPU_A3 + L3_2 + L3_1 + L4_CFG domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
0	WKUPDEP_SR_IVA_MPU	Wakeup dependency from SR_IVA module (softwareakeup signal) towards MPU + L3_1 + L4_CFG domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-444. Register Call Summary for Register PM_ALWON_SR_IVA_WKDEP

Clock Management Functional Description • Clock Domain Dependency: [0] [1]
PRCM Register Manual • ALWAYS_ON_PRM Register Summary: [2]

Table 3-445. RM_ALWON_SR_IVA_CONTEXT

Address Offset	0x0000 0034		
Physical Address	0x4A30 6634	**Instance**	ALWAYS_ON_PRM
Description	This register contains dedicated SR_IVA context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															LOSTCONTEXT_DFF

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Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of Always_on_CORE_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-446. Register Call Summary for Register RM_ALWON_SR_IVA_CONTEXT

Power Management Functional Description • PD_ALWON_CORE Description: [0]
PRCM Register Manual • ALWAYS_ON_PRM Register Summary: [1]

Table 3-447. PM_ALWON_SR_CORE_WKDEP

Address Offset	0x0000 0038		
Physical Address	0x4A30 6638	**Instance**	ALWAYS_ON_PRM
Description	This register controls wakeup dependency based on SR_CORE service requests.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														WKUPDEP_SR_CORE_MPU_M3	WKUPDEP_SR_CORE_MPU

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	WKUPDEP_SR_CORE_MPU_M3	Wakeup dependency from SR_CORE module (softwareakeup signal) towards MPU_A3 + L3_2 + L3_1 + L4_CFG domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
0	WKUPDEP_SR_CORE_MPU	Wakeup dependency from SR_CORE module (softwareakeup signal) towards MPU + L3_1 + L4_CFG domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-448. Register Call Summary for Register PM_ALWON_SR_CORE_WKDEP

Clock Management Functional Description • Clock Domain Dependency: [0] [1]
PRCM Register Manual • ALWAYS_ON_PRM Register Summary: [2]

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Table 3-449. RM_ALWON_SR_CORE_CONTEXT

Address Offset	0x0000 003C		
Physical Address	0x4A30 663C	**Instance**	ALWAYS_ON_PRM
Description	This register contains dedicated SR_CORE context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of Always_on_CORE_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-450. Register Call Summary for Register RM_ALWON_SR_CORE_CONTEXT

Power Management Functional Description • PD_ALWON_CORE Description: [0]
PRCM Register Manual • ALWAYS_ON_PRM Register Summary: [1]

3.11.8 CORE_PRM Registers

3.11.8.1 CORE_PRM Register Summary

Table 3-451. CORE_PRM Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	CORE_PRM L4 Base Address
PM_CORE_PWRSTCTRL	RW	32	0x0000 0000	0x4A30 6700
PM_CORE_PWRSTST	R	32	0x0000 0004	0x4A30 6704
RM_L3_1_L3_1_CONTEXT	RW	32	0x0000 0024	0x4A30 6724
RM_L3_2_L3_2_CONTEXT	RW	32	0x0000 0124	0x4A30 6824
RM_L3_2_GPMC_CONTEXT	RW	32	0x0000 012C	0x4A30 682C
RM_L3_2_OCMC_RAM_CONTEXT	RW	32	0x0000 0134	0x4A30 6834
RM_MPU_M3_RSTCTRL	RW	32	0x0000 0210	0x4A30 6910
RM_MPU_M3_RSTST	RW	32	0x0000 0214	0x4A30 6914
RM_MPU_M3_MPU_M3_CONTEXT	RW	32	0x0000 0224	0x4A30 6924
RM_SDMA_SDMA_CONTEXT	RW	32	0x0000 0324	0x4A30 6A24
RM_MEMIF_DMM_CONTEXT	RW	32	0x0000 0424	0x4A30 6B24
RM_MEMIF_EMIF_FW_CONTEXT	RW	32	0x0000 042C	0x4A30 6B2C
RM_MEMIF_EMIF_1_CONTEXT	RW	32	0x0000 0434	0x4A30 6B34

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Table 3-451. CORE_PRM Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	CORE_PRM L4 Base Address
RM_MEMIF_EMIF_2_CONTEXT	RW	32	0x0000 043C	0x4A30 6B3C
RM_MEMIF_DLL_CONTEXT	RW	32	0x0000 0444	0x4A30 6B44
RESERVED	RW	32	0x0000 0454	0x4A30 6B54
RESERVED	RW	32	0x0000 045C	0x4A30 6B5C
RESERVED	RW	32	0x0000 0464	0x4A30 6B64
RM_C2C_C2C_CONTEXT	RW	32	0x0000 0524	0x4A30 6C24
RESERVED	RW	32	0x0000 052C	0x4A30 6C2C
RM_C2C_C2C_FW_CONTEXT	RW	32	0x0000 0534	0x4A30 6C34
RM_L4CFG_L4_CFG_CONTEXT	RW	32	0x0000 0624	0x4A30 6D24
RM_L4CFG_SPINLOCK_CONTEXT	RW	32	0x0000 062C	0x4A30 6D2C
RM_L4CFG_MAILBOX_CONTEXT	RW	32	0x0000 0634	0x4A30 6D34
RM_L4CFG_SAR_ROM_CONTEXT	RW	32	0x0000 063C	0x4A30 6D3C
RM_L3INSTR_L3_3_CONTEXT	RW	32	0x0000 0724	0x4A30 6E24
RM_L3INSTR_L3_INSTR_CONTEXT	RW	32	0x0000 072C	0x4A30 6E2C
RM_L3INSTR_OCP_WP1_CONTEXT	RW	32	0x0000 0744	0x4A30 6E44

3.11.8.2 CORE_PRM Register Description

Table 3-452. PM_CORE_PWRSTCTRL

Address Offset	0x0000 0000		
Physical Address	0x4A30 6700	**Instance**	CORE_PRM
Description	This register controls the CORE power state to reach upon a domain sleep transition		
Type	RW		

31 30 29 28 27 26	25 24	23 22	21 20	19 18	17 16	15 14 13	12	11	10	9	8	7 6 5	4	3	2	1 0
RESERVED	INTRCONN_NRET_BANK_ONSTATE	MPU_M3_UNICACHE_ONSTATE	MPU_M3_L2RAM_ONSTATE	CORE_OCMRAM_ONSTATE	CORE_OTHER_BANK_ONSTATE	RESERVED	INTRCONN_NRET_BANK_RETSTATE	MPU_M3_UNICACHE_RETSTATE	MPU_M3_L2RAM_RETSTATE	CORE_OCMRAM_RETSTATE	CORE_OTHER_BANK_RETSTATE	RESERVED	LOWPOWERSTATECHANGE	RESERVED	LOGICRETSTATE	POWERSTATE

Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x00
25:24	INTRCONN_NRET_BANK_ONSTATE	INTRCONN_WP bank and DMM bank2 state when domain is ON. Read 0x3: Memory bank is on when the domain is ON.	R Rreturns 1s	0x3
23:22	MPU_M3_UNICACHE_ONSTATE	MPU_A3 UNICACHE bank state when domain is ON. Read 0x3: Memory bank is on when the domain is ON.	R Rreturns 1s	0x3

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Bits	Field Name	Description	Type	Reset
21:20	MPU_M3_L2RAM_ONSTATE	MPU_A3 L2 bank state when domain is ON. Read 0x3: Memory bank is on when the domain is ON.	R Rreturns 1s	0x3
19:18	CORE_OCMRAM_ONSTATE	OCMRAM bank state when domain is ON. Read 0x3: Memory bank is on when the domain is ON.	R Rreturns 1s	0x3
17:16	CORE_OTHER_BANK_ONSTATE	DMA/ICR bank and DMM bank1 state when domain is ON. Read 0x3: Memory bank is on when the domain is ON.	R Rreturns 1s	0x3
15:13	RESERVED		R	0x0
12	INTRCONN_NRET_BANK_RETSTATE	INTRCONN_WP bank and DMM bank2 state when domain is RETENTION. Read 0x0: Memory bank is off when the domain is in the RETENTION state.	R	0
11	MPU_M3_UNICACHE_RETSTATE	MPU_A3 UNICACHE bank state when domain is RETENTION. 0x0: Memory bank is off when the domain is in the RETENTION state. 0x1: Memory bank is retained when domain is in RETENTION state.	RW	1
10	MPU_M3_L2RAM_RETSTATE	MPU_A3 L2 bank state when domain is RETENTION. 0x0: Memory bank is off when the domain is in the RETENTION state. 0x1: Memory bank is retained when domain is in RETENTION state.	RW	1
9	CORE_OCMRAM_RETSTATE	OCMRAM bank state when domain is RETENTION. Read 0x1: Memory bank is retained when domain is in RETENTION state.	R Rreturns 1s	1
8	CORE_OTHER_BANK_RETSTATE	DMA/ICR bank and DMM bank1 state when domain is RETENTION. Read 0x1: Memory bank is retained when domain is in RETENTION state.	R Rreturns 1s	1
7:5	RESERVED		R	0x0
4	LOWPOWERSTATECHANGE	Power state change request when domain has already performed a sleep transition. Allows going into deeper low power state without waking up the power domain. 0x0: Do not request a low power state change. 0x1: Request a low power state change. This bit is automatically cleared when the power state is effectively changed or when power state is ON.	RW WSpecial	0
3	RESERVED		R	0
2	LOGICRETSTATE	Logic state when power domain is RETENTION 0x0: Only retention registers are retained and remaing logic is off when the domain is in RETENTION state. 0x1: Whole logic is retained when domain is in RETENTION state.	RW	1
1:0	POWERSTATE	Power state control Read 0x0: Reserved 0x1: RETENTION state 0x2: INACTIVE state 0x3: ON State	RW	0x3

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Table 3-453. Register Call Summary for Register PM_CORE_PWRSTCTRL

Power Management Functional Description
• Power Domain Modes: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12]
PRCM Register Manual
• CORE_PRM Register Summary: [13]

Table 3-454. PM_CORE_PWRSTST

Address Offset	0x0000 0004		
Physical Address	0x4A30 6704	**Instance**	CORE_PRM
Description	This register provides a status on the current CORE power domain state. [warm reset insensitive]		
Type	R		

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
RESERVED	RESERVED / INTRANSITION / RESERVED	INTRCONN_NRET_BANK_STATEST / MPU_M3_UNICACHE_STATEST / MPU_M3_L2RAM_STATEST	CORE_OCMRAM_STATEST / CORE_OTHER_BANK_STATEST / RESERVED / LOGICSTATEST / POWERSTATEST

Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x00
25:24	LASTPOWERSTATEENTERED	Last low power state entered. Set to 0x3 upon write of the same only. This register is intended for debug purpose only. Read 0x3: Power domain was previously ON-ACTIVE Read 0x2: Power domain was previously ON-INACTIVE Read 0x1: Power domain was previously in RETENTION Read 0x0: Power domain was previously OFF	RW W1toSet	0x0
23:21	RESERVED		R	0x0
20	INTRANSITION	Domain transition status Read 0x0: No ongoing transition on power domain Read 0x1: Power domain transition is in progress.	R	0
19:14	RESERVED		R	0x00
13:12	INTRCONN_NRET_BANK_STATEST	INTRCONN_WP bank and DMM bank2 state status Read 0x0: Memory is OFF Read 0x1: Reserved Read 0x2: Reserved Read 0x3: Memory is ON	R	0x3
11:10	MPU_M3_UNICACHE_STATEST	MPU_A3 UNICACHE bank state status Read 0x0: Memory is OFF Read 0x1: Memory is RETENTION Read 0x2: Reserved Read 0x3: Memory is ON	R	0x3

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Bits	Field Name	Description	Type	Reset
9:8	MPU_M3_L2RAM_STATEST	MPU_A3 L2 bank state status Read 0x0: Memory is OFF Read 0x1: Memory is RETENTION Read 0x2: Reserved Read 0x3: Memory is ON	R	0x3
7:6	CORE_OCMRAM_STATEST	OCMRAM bank state status Read 0x0: Memory is OFF Read 0x1: Memory is RETENTION Read 0x2: Reserved Read 0x3: Memory is ON	R	0x3
5:4	CORE_OTHER_BANK_STATEST	DMA/ICR bank and DMM bank1 state status Read 0x0: Memory is OFF Read 0x1: Memory is RETENTION Read 0x2: Reserved Read 0x3: Memory is ON	R	0x3
3	RESERVED		R	0
2	LOGICSTATEST	Logic state status Read 0x0: Logic in domain is OFF Read 0x1: Logic in domain is ON	R	1
1:0	POWERSTATEST	Current power state status Read 0x0: Reserved Read 0x1: Power domain is in RETENTION Read 0x2: Power domain is ON-INACTIVE Read 0x3: Power domain is ON-ACTIVE	R	0x3

Table 3-455. Register Call Summary for Register PM_CORE_PWRSTST

Power Management Functional Description • Power Domain Modes: [0] [1] [2] [3] [4] [5] [6] [7] [8]
PRCM Register Manual • CORE_PRM Register Summary: [9]

Table 3-456. RM_L3_1_L3_1_CONTEXT

Address Offset	0x0000 0024		
Physical Address	0x4A30 6724	**Instance**	CORE_PRM
Description	This register contains dedicated L3_1 context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														LOSTCONTEXT_RFF	LOSTCONTEXT_DFF

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Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	LOSTCONTEXT_RFF	Specify if RFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_PWRON_RET_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-457. Register Call Summary for Register RM_L3_1_L3_1_CONTEXT

Power Management Functional Description • PD_CORE Description: [0] [1]
PRCM Register Manual • CORE_PRM Register Summary: [2]

Table 3-458. RM_L3_2_L3_2_CONTEXT

Address Offset	0x0000 0124		
Physical Address	0x4A30 6824	**Instance**	CORE_PRM
Description	This register contains dedicated L3_2 context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														LOSTCONTEXT_RFF	LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	LOSTCONTEXT_RFF	Specify if RFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_PWRON_RET_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-459. Register Call Summary for Register RM_L3_2_L3_2_CONTEXT

Power Management Functional Description • PD_CORE Description: [0] [1]
PRCM Register Manual • CORE_PRM Register Summary: [2]

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Table 3-460. RM_L3_2_GPMC_CONTEXT

Address Offset	0x0000 012C		
Physical Address	0x4A30 682C	**Instance**	CORE_PRM
Description	This register contains dedicated GPMC context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														LOSTCONTEXT_RFF	RESERVED

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	LOSTCONTEXT_RFF	Specify if RFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_RET_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
0	RESERVED		R	0

Table 3-461. Register Call Summary for Register RM_L3_2_GPMC_CONTEXT

Power Management Functional Description
- PD_CORE Description: [0]

PRCM Register Manual
- CORE_PRM Register Summary: [1]

Table 3-462. RM_L3_2_OCMC_RAM_CONTEXT

Address Offset	0x0000 0134		
Physical Address	0x4A30 6834	**Instance**	CORE_PRM
Description	This register contains dedicated OCMC_RAM context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								LOSTMEM_CORE_OCMRAM	RESERVED						LOSTCONTEXT_DFF

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Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	LOSTMEM_CORE_OCMRAM	Specify if memory-based context in CORE_OCMRAM memory bank has been lost due to a previous power transition or other reset source (not affected by a global warm reset). 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
7:1	RESERVED		R	0x00
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-463. Register Call Summary for Register RM_L3_2_OCMC_RAM_CONTEXT

Power Management Functional Description • PD_CORE Description: [0]
PRCM Register Manual • CORE_PRM Register Summary: [1]

Table 3-464. RM_MPU_M3_RSTCTRL

Address Offset	0x0000 0210		
Physical Address	0x4A30 6910	**Instance**	CORE_PRM
Description	This register controls the release of the MPU_A3 sub-system resets.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													RST3	RST2	RST1

Bits	Field Name	Description	Type	Reset
31:3	RESERVED		R	0x0000 0000
2	RST3	MPU_A3 MMU and CACHE interface reset control. 0x0: Reset is cleared for MPU_A3 CACHE MMU 0x1: Reset is asserted for the MPU_A3 CACHE MMU	RW	1
1	RST2	MPU_A3 Cortex M3 CPU2 reset control. 0x0: Reset is cleared for the MPU_A3 Cortex M3 CPU2 0x1: Reset is asserted for the MPU_A3 Cortex M3 CPU2	RW	1
0	RST1	MPU_A3 Cortex M3 CPU1 reset control. 0x0: Reset is cleared for the MPU_A3 Cortex M3 CPU1 0x1: Reset is asserted for the MPU_A3 Cortex M3 CPU1	RW	1

Table 3-465. Register Call Summary for Register RM_MPU_M3_RSTCTRL

Reset Management Functional Description • Reset Domains: [0] • Cortex-M3 MPU Subsystem Power-On Reset Sequence: [1] [2] [3] • Cortex-M3 MPU Subsystem Software Warm Reset Sequence: [4] [5] [6] [7] [8]
PRCM Register Manual • CORE_PRM Register Summary: [9]

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Table 3-466. RM_MPU_M3_RSTST

Address Offset	0x0000 0214		
Physical Address	0x4A30 6914	**Instance**	CORE_PRM
Description	This register logs the different reset sources of the MPU_A3 SS. Each bit is set upon release of the domain reset signal. Must be cleared by software. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								ICECRUSHER_RST2ST	ICECRUSHER_RST1ST	EMULATION_RST2ST	EMULATION_RST1ST	RST3ST	RST2ST	RST1ST	

Bits	Field Name	Description	Type	Reset
31:7	RESERVED		R	0x0000000
6	ICECRUSHER_RST2ST	Cortex M3 CPU2 has been reset due to MPU_A3 ICECRUSHER2 reset source 0x0: No icecrusher reset 0x1: CPU2 has been reset upon icecrusher reset	RW W1toClr	0
5	ICECRUSHER_RST1ST	Cortex M3 CPU1 has been reset due to MPU_A3 ICECRUSHER1 reset source 0x0: No icecrusher reset 0x1: CPU1 has been reset upon icecrusher reset	RW W1toClr	0
4	EMULATION_RST2ST	Cortex M3 CPU2 has been reset due to emulation reset source e.g. assert reset command initiated by the icepick module 0x0: No emulation reset 0x1: CPU2 has been reset upon emulation reset	RW W1toClr	0
3	EMULATION_RST1ST	Cortex M3 CPU1 has been reset due to emulation reset source e.g. assert reset command initiated by the icepick module 0x0: No emulation reset 0x1: CPU1 has been reset upon emulation reset	RW W1toClr	0
2	RST3ST	MPU_A3 MMU and CACHE interface software reset status 0x0: No software reset occured 0x1: MPU_A3 MMU and CACHE interface has been reset upon software reset	RW W1toClr	0
1	RST2ST	MPU_A3 Cortex-M3 CPU2 software reset status 0x0: No software reset occured 0x1: Cortex M3 CPU2 has been reset upon software reset	RW W1toClr	0
0	RST1ST	MPU_A3 Cortex-M3 CPU1 software reset status 0x0: No software reset occured 0x1: Cortex M3 CPU1 has been reset upon software reset	RW W1toClr	0

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Table 3-467. Register Call Summary for Register RM_MPU_M3_RSTST

PRCM Register Manual
- CORE_PRM Register Summary: [0]

Table 3-468. RM_MPU_M3_MPU_M3_CONTEXT

Address Offset	0x0000 0224		
Physical Address	0x4A30 6924	**Instance**	CORE_PRM
Description	This register contains dedicated MPU_A3 context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						LOSTMEM_MPU_M3_L2RAM	LOSTMEM_MPU_M3_UNICACHE	RESERVED						LOSTCONTEXT_RFF	LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:10	RESERVED		R	0x000000
9	LOSTMEM_MPU_M3_L2RAM	Specify if memory-based context in MPU_A3_L2RAM memory bank has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
8	LOSTMEM_MPU_M3_UNICACHE	Specify if memory-based context in MPU_A3_UNICACHE memory bank has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
7:2	RESERVED		R	0x00
1	LOSTCONTEXT_RFF	Specify if RFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of MPU_A3_RET_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of MPU_A3_RST3 signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-469. Register Call Summary for Register RM_MPU_M3_MPU_M3_CONTEXT

Power Management Functional Description
- PD_CORE Description: [0] [1]

PRCM Register Manual
- CORE_PRM Register Summary: [2]

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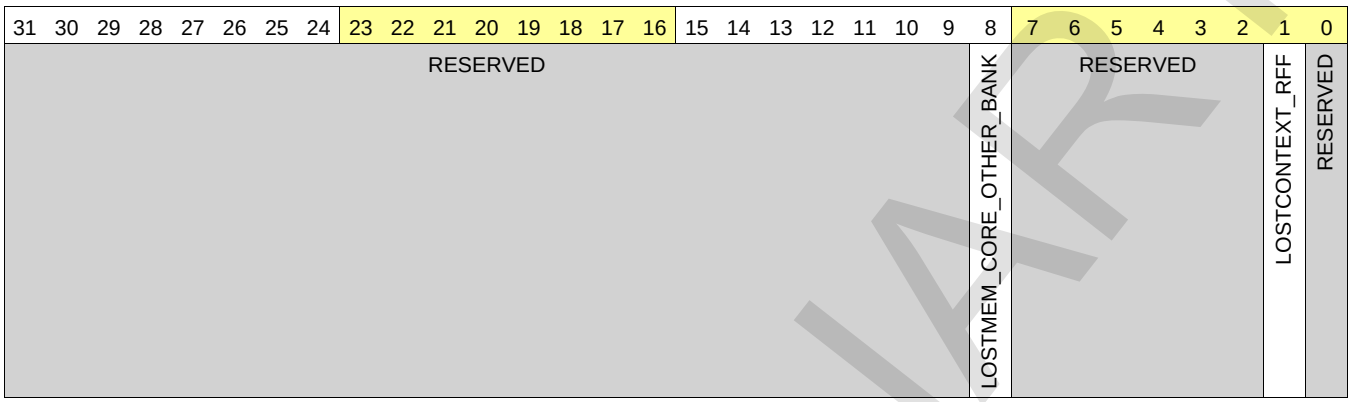
Table 3-470. RM_SDMA_SDMA_CONTEXT

Address Offset	0x0000 0324		
Physical Address	0x4A30 6A24	**Instance**	CORE_PRM
Description	This register contains dedicated SDMA context statuses. [warm reset insensitive]		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	LOSTMEM_CORE_OTHER_BANK	Specify if memory-based context in CORE_OTHER_BANK memory bank has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
7:2	RESERVED		R	0x00
1	LOSTCONTEXT_RFF	Specify if RFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of SDMA_RET_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
0	RESERVED		R	0

Table 3-471. Register Call Summary for Register RM_SDMA_SDMA_CONTEXT

Power Management Functional Description • PD_CORE Description: [0]
PRCM Register Manual • CORE_PRM Register Summary: [1]

Table 3-472. RM_MEMIF_DMM_CONTEXT

Address Offset	0x0000 0424		
Physical Address	0x4A30 6B24	**Instance**	CORE_PRM
Description	This register contains dedicated DMM context statuses. [warm reset insensitive]		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						LOSTMEM_CORE_NRET_BANK	LOSTMEM_CORE_OTHER_BANK	RESERVED						LOSTCONTEXT_RFF	LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:10	RESERVED		R	0x000000
9	LOSTMEM_CORE_NRET_BANK	Specify if memory-based context in CORE_NRET_BANK memory bank has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
8	LOSTMEM_CORE_OTHER_BANK	Specify if memory-based context in CORE_OTHER_BANK memory bank has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
7:2	RESERVED		R	0x00
1	LOSTCONTEXT_RFF	Specify if RFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_RET_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-473. Register Call Summary for Register RM_MEMIF_DMM_CONTEXT

Power Management Functional Description • PD_CORE Description: [0] [1]
PRCM Register Manual • CORE_PRM Register Summary: [2]

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Table 3-474. RM_MEMIF_EMIF_FW_CONTEXT

Address Offset	0x0000 042C		
Physical Address	0x4A30 6B2C	**Instance**	CORE_PRM
Description	This register contains dedicated EMIF_FW context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														LOSTCONTEXT_RFF	LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	LOSTCONTEXT_RFF	Specify if RFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_PWRON_RET_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-475. Register Call Summary for Register RM_MEMIF_EMIF_FW_CONTEXT

Power Management Functional Description
- PD_CORE Description: [0] [1]

PRCM Register Manual
- CORE_PRM Register Summary: [2]

Table 3-476. RM_MEMIF_EMIF_1_CONTEXT

Address Offset	0x0000 0434		
Physical Address	0x4A30 6B34	**Instance**	CORE_PRM
Description	This register contains dedicated EMIF_1 context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														LOSTCONTEXT_RFF	LOSTCONTEXT_DFF

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Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	LOSTCONTEXT_RFF	Specify if RFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_PWRON_RET_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_PWRON_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-477. Register Call Summary for Register RM_MEMIF_EMIF_1_CONTEXT

Power Management Functional Description • PD_CORE Description: [0] [1]
PRCM Register Manual • CORE_PRM Register Summary: [2]

Table 3-478. RM_MEMIF_EMIF_2_CONTEXT

Address Offset	0x0000 043C		
Physical Address	0x4A30 6B3C	**Instance**	CORE_PRM
Description	This register contains dedicated EMIF_2 context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														LOSTCONTEXT_RFF	LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	LOSTCONTEXT_RFF	Specify if RFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_PWRON_RET_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_PWRON_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-479. Register Call Summary for Register RM_MEMIF_EMIF_2_CONTEXT

Power Management Functional Description • PD_CORE Description: [0] [1]
PRCM Register Manual • CORE_PRM Register Summary: [2]

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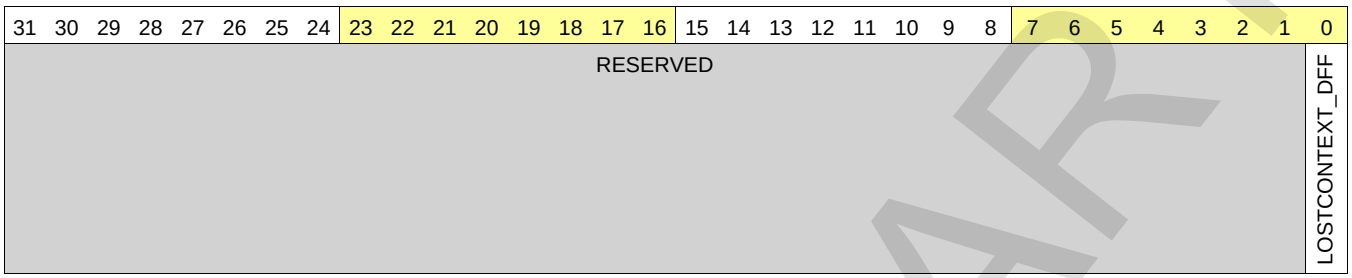
Table 3-480. RM_MEMIF_DLL_CONTEXT

Address Offset	0x0000 0444		
Physical Address	0x4A30 6B44	**Instance**	CORE_PRM
Description	This register contains dedicated DLL context statuses. [warm reset insensitive]		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of DLL_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

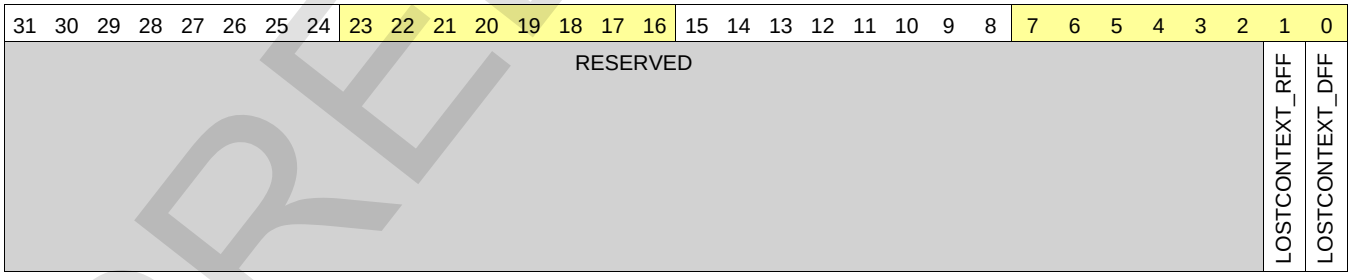
Table 3-481. Register Call Summary for Register RM_MEMIF_DLL_CONTEXT

PRCM Register Manual

- CORE_PRM Register Summary: [0]

Table 3-482. RM_C2C_C2C_CONTEXT

Address Offset	0x0000 0524		
Physical Address	0x4A30 6C24	**Instance**	CORE_PRM
Description	This register contains dedicated C2C context statuses. [warm reset insensitive]		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	LOSTCONTEXT_RFF	Specify if RFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

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Bits	Field Name	Description	Type	Reset
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-483. Register Call Summary for Register RM_C2C_C2C_CONTEXT

Power Management Functional Description • PD_CORE Description: [0] [1]
PRCM Register Manual • CORE_PRM Register Summary: [2]

Table 3-484. RM_C2C_C2C_FW_CONTEXT

Address Offset	0x0000 0534		
Physical Address	0x4A30 6C34	**Instance**	CORE_PRM
Description	This register contains dedicated C2C_FW context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														LOSTCONTEXT_RFF	LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	LOSTCONTEXT_RFF	Specify if RFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_PWRON_RET_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-485. Register Call Summary for Register RM_C2C_C2C_FW_CONTEXT

Power Management Functional Description • PD_CORE Description: [0] [1]
PRCM Register Manual • CORE_PRM Register Summary: [2]

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Table 3-486. RM_L4CFG_L4_CFG_CONTEXT

Address Offset	0x0000 0624		
Physical Address	0x4A30 6D24	**Instance**	CORE_PRM
Description	This register contains dedicated L4_CFG context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														LOSTCONTEXT_RFF	LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	LOSTCONTEXT_RFF	Specify if RFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_PWRON_RET_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-487. Register Call Summary for Register RM_L4CFG_L4_CFG_CONTEXT

Power Management Functional Description
- PD_CORE Description: [0] [1]

PRCM Register Manual
- CORE_PRM Register Summary: [2]

Table 3-488. RM_L4CFG_SPINLOCK_CONTEXT

Address Offset	0x0000 062C		
Physical Address	0x4A30 6D2C	**Instance**	CORE_PRM
Description	This register contains dedicated HW_SEM context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														LOSTCONTEXT_RFF	RESERVED

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Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	LOSTCONTEXT_RFF	Specify if RFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_RET_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
0	RESERVED		R	0

Table 3-489. Register Call Summary for Register RM_L4CFG_SPINLOCK_CONTEXT

Power Management Functional Description • PD_CORE Description: [0]
PRCM Register Manual • CORE_PRM Register Summary: [1]

Table 3-490. RM_L4CFG_MAILBOX_CONTEXT

Address Offset	0x0000 0634		
Physical Address	0x4A30 6D34	**Instance**	CORE_PRM
Description	This register contains dedicated MAILBOX context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														LOSTCONTEXT_RFF	RESERVED

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	LOSTCONTEXT_RFF	Specify if RFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_RET_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
0	RESERVED		R	0

Table 3-491. Register Call Summary for Register RM_L4CFG_MAILBOX_CONTEXT

Power Management Functional Description • PD_CORE Description: [0]
PRCM Register Manual • CORE_PRM Register Summary: [1]

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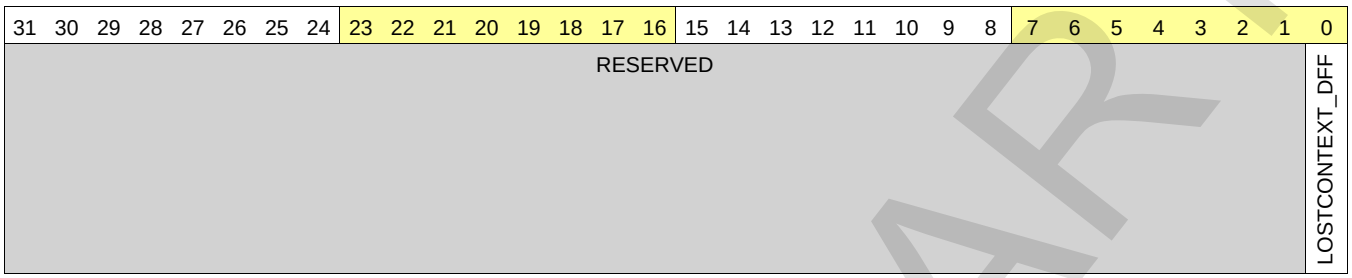
Table 3-492. RM_L4CFG_SAR_ROM_CONTEXT

Address Offset	0x0000 063C		
Physical Address	0x4A30 6D3C	**Instance**	CORE_PRM
Description	This register contains dedicated SAR_ROM context statuses. [warm reset insensitive]		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

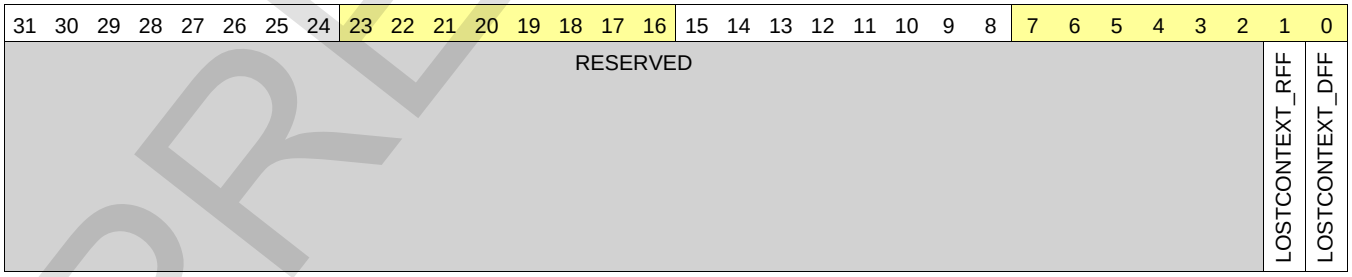
Table 3-493. Register Call Summary for Register RM_L4CFG_SAR_ROM_CONTEXT

Power Management Functional Description
- PD_CORE Description: [0]

PRCM Register Manual
- CORE_PRM Register Summary: [1]

Table 3-494. RM_L3INSTR_L3_3_CONTEXT

Address Offset	0x0000 0724		
Physical Address	0x4A30 6E24	**Instance**	CORE_PRM
Description	This register contains dedicated L3_3 context statuses. [warm reset insensitive]		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	LOSTCONTEXT_RFF	Specify if RFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_PWRON_RET_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

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Bits	Field Name	Description	Type	Reset
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-495. Register Call Summary for Register RM_L3INSTR_L3_3_CONTEXT

Power Management Functional Description • PD_CORE Description: [0] [1]
PRCM Register Manual • CORE_PRM Register Summary: [2]

Table 3-496. RM_L3INSTR_L3_INSTR_CONTEXT

Address Offset	0x0000 072C		
Physical Address	0x4A30 6E2C	**Instance**	CORE_PRM
Description	This register contains dedicated L3_INSTR context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-497. Register Call Summary for Register RM_L3INSTR_L3_INSTR_CONTEXT

Power Management Functional Description • PD_CORE Description: [0]
PRCM Register Manual • CORE_PRM Register Summary: [1]

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Table 3-498. RM_L3INSTR_OCP_WP1_CONTEXT

Address Offset	0x0000 0744		
Physical Address	0x4A30 6E44	**Instance**	CORE_PRM
Description	This register contains dedicated OCP_WP1 context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							LOSTMEM_CORE_NRET_BANK	RESERVED						LOSTCONTEXT_RFF	LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	LOSTMEM_CORE_NRET_BANK	Specify if memory-based context in CORE_NRET_BANK memory bank has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
7:2	RESERVED		R	0x00
1	LOSTCONTEXT_RFF	Specify if RFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_PWRON_RET_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-499. Register Call Summary for Register RM_L3INSTR_OCP_WP1_CONTEXT

PRCM Register Manual
- CORE_PRM Register Summary: [0]

3.11.9 IVAHD_PRM Registers

3.11.9.1 IVAHD_PRM Register Summary

Table 3-500. IVAHD_PRM Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	IVAHD_PRM L4 Base Address
PM_IVAHD_PWRSTCTRL	RW	32	0x0000 0000	0x4A30 6F00
PM_IVAHD_PWRSTST	R	32	0x0000 0004	0x4A30 6F04

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Table 3-500. IVAHD_PRM Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	IVAHD_PRM L4 Base Address
RM_IVAHD_RSTCTRL	RW	32	0x0000 0010	0x4A30 6F10
RM_IVAHD_RSTST	RW	32	0x0000 0014	0x4A30 6F14
RM_IVAHD_IVAHD_CONTEXT	RW	32	0x0000 0024	0x4A30 6F24
RM_IVAHD_SL2_CONTEXT	RW	32	0x0000 002C	0x4A30 6F2C

3.11.9.2 IVAHD_PRM Register Description

Table 3-501. PM_IVAHD_PWRSTCTRL

Address Offset	0x0000 0000		
Physical Address	0x4A30 6F00	**Instance**	IVAHD_PRM
Description	This register controls the IVAHD power state to reach upon a domain sleep transition		
Type	RW		

31 30 29 28 27 26 25 24	23 22	21 20	19 18	17 16	15 14 13 12	11	10	9	8	7 6 5	4	3	2	1 0
RESERVED	TCM2_MEM_ONSTATE	TCM1_MEM_ONSTATE	SL2_MEM_ONSTATE	HWA_MEM_ONSTATE	RESERVED	TCM2_MEM_RETSTATE	TCM1_MEM_RETSTATE	SL2_MEM_RETSTATE	HWA_MEM_RETSTATE	RESERVED	LOWPOWERSTATECHANGE	RESERVED	LOGICRETSTATE	POWERSTATE

Bits	Field Name	Description	Type	Reset
31:24	RESERVED		R	0x00
23:22	TCM2_MEM_ONSTATE	TCM2 memory state when domain is ON. Read 0x3: Memory bank is on when the domain is ON.	R Rreturns 1s	0x3
21:20	TCM1_MEM_ONSTATE	TCM1 memory state when domain is ON. Read 0x3: Memory bank is on when the domain is ON.	R Rreturns 1s	0x3
19:18	SL2_MEM_ONSTATE	SL2 memory state when domain is ON. Read 0x3: Memory bank is on when the domain is ON.	R Rreturns 1s	0x3
17:16	HWA_MEM_ONSTATE	HWA memory state when domain is ON. Read 0x3: Memory bank is on when the domain is ON.	R Rreturns 1s	0x3
15:12	RESERVED		R	0x0
11	TCM2_MEM_RETSTATE	TCM2 memory state when domain is RETENTION. 0x0: Memory bank is off when the domain is in the RETENTION state. 0x1: Memory bank is retained when domain is in RETENTION state.	RW	1
10	TCM1_MEM_RETSTATE	TCM1 memory state when domain is RETENTION. 0x0: Memory bank is off when the domain is in the RETENTION state. 0x1: Memory bank is retained when domain is in RETENTION state.	RW	1

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Bits	Field Name	Description	Type	Reset
9	SL2_MEM_RETSTATE	SL2 memory state when domain is RETENTION. 0x0: Memory bank is off when the domain is in the RETENTION state. 0x1: Memory bank is retained when domain is in RETENTION state.	RW	1
8	HWA_MEM_RETSTATE	HWA memory state when domain is RETENTION. Read 0x0: Memory bank is off when the domain is in the RETENTION state.	R	0
7:5	RESERVED		R	0x0
4	LOWPOWERSTATECHANGE	Power state change request when domain has already performed a sleep transition. Allows going into deeper low power state without waking up the power domain. 0x0: Do not request a low power state change. 0x1: Request a low power state change. This bit is automatically cleared when the power state is effectively changed or when power state is ON.	RW WSpecial	0
3	RESERVED		R	0
2	LOGICRETSTATE	Logic state when power domain is RETENTION Read 0x0: Whole logic is off when the domain is in RETENTION state.	R	0
1:0	POWERSTATE	Power state control 0x0: OFF state 0x1: RETENTION state 0x2: INACTIVE state 0x3: ON State	RW	0x3

Table 3-502. Register Call Summary for Register PM_IVAHD_PWRSTCTRL

Power Management Functional Description • Power Domain Modes: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10]
PRCM Register Manual • IVAHD_PRM Register Summary: [11]

Table 3-503. PM_IVAHD_PWRSTST

Address Offset	0x0000 0004		
Physical Address	0x4A30 6F04	**Instance**	IVAHD_PRM
Description	This register provides a status on the current IVAHD power domain state. [warm reset insensitive]		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												RESERVED																			
						LASTPOWERSTATEENTERED		RESERVED																									
											INTRANSITION																				
												RESERVED																			
																				TCM2_MEM_STATEST											
																						TCM1_MEM_STATEST									
																								SL2_MEM_STATEST							
																										HWA_MEM_STATEST					
																												RESERVED			
																													LOGICSTATEST		
																														POWERSTATEST	

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Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x00
25:24	LASTPOWERSTATEENTERED	Last low power state entered. Set to 0x3 upon write of the same only. This register is intended for debug purpose only. Read 0x3: Power domain was previously ON-ACTIVE Read 0x2: Power domain was previously ON-INACTIVE Read 0x1: Power domain was previously in RETENTION Read 0x0: Power domain was previously OFF	RW W1toSet	0x0
23:21	RESERVED		R	0x0
20	INTRANSITION	Domain transition status Read 0x0: No ongoing transition on power domain Read 0x1: Power domain transition is in progress.	R	0
19:12	RESERVED		R	0x00
11:10	TCM2_MEM_STATEST	TCM2 memory state status Read 0x0: Memory is OFF Read 0x1: Memory is RETENTION Read 0x2: Reserved Read 0x3: Memory is ON	R	0x3
9:8	TCM1_MEM_STATEST	TCM1 memory state status Read 0x0: Memory is OFF Read 0x1: Memory is RETENTION Read 0x2: Reserved Read 0x3: Memory is ON	R	0x3
7:6	SL2_MEM_STATEST	SL2 memory state status Read 0x0: Memory is OFF Read 0x1: Memory is RETENTION Read 0x2: Reserved Read 0x3: Memory is ON	R	0x3
5:4	HWA_MEM_STATEST	HWA memory state status Read 0x0: Memory is OFF Read 0x1: Memory is RETENTION Read 0x2: Reserved Read 0x3: Memory is ON	R	0x3
3	RESERVED		R	0
2	LOGICSTATEST	Logic state status Read 0x0: Logic in domain is OFF Read 0x1: Logic in domain is ON	R	1
1:0	POWERSTATEST	Current power state status Read 0x0: Power domain is OFF Read 0x1: Power domain is in RETENTION Read 0x2: Power domain is ON-INACTIVE Read 0x3: Power domain is ON-ACTIVE	R	0x3

Table 3-504. Register Call Summary for Register PM_IVAHD_PWRSTST

Power Management Functional Description
- Power Domain Modes: [0] [1] [2] [3] [4] [5] [6] [7]

PRCM Register Manual
- IVAHD_PRM Register Summary: [8]

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Table 3-505. RM_IVAHD_RSTCTRL

Address Offset	0x0000 0010		
Physical Address	0x4A30 6F10	**Instance**	IVAHD_PRM
Description	This register controls the release of the IVAHD sub-system resets.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													RST3	RST2	RST1

Bits	Field Name	Description	Type	Reset
31:3	RESERVED		R	0x0000 0000
2	RST3	IVAHD logic and SL2 reset control 0x0: Reset is cleared for the IVAHD logic and SL2 0x1: Reset is asserted for IVAHD logic and SL2	RW	1
1	RST2	IVAHD Sequencer2 reset control 0x0: Reset is cleared for IVAHD Sequencer CPU2 0x1: Reset is asserted for IVAHD Sequencer CPU2	RW	1
0	RST1	IVAHD sequencer1 reset control 0x0: Reset is cleared for the IVAHD Sequencer CPU1 0x1: Reset is asserted for the IVAHD sequencer CPU1	RW	1

Table 3-506. Register Call Summary for Register RM_IVAHD_RSTCTRL

Reset Management Functional Description
- Reset Domains: [0]
- IVAHD Subsystem Power-On Reset Sequence: [1] [2] [3]
- IVAHD Subsystem Software Warm Reset Sequence: [4] [5] [6] [7] [8] [9]

PRCM Register Manual
- IVAHD_PRM Register Summary: [10]

Table 3-507. RM_IVAHD_RSTST

Address Offset	0x0000 0014		
Physical Address	0x4A30 6F14	**Instance**	IVAHD_PRM
Description	This register logs the different reset sources of the IVAHD domain. Each bit is set upon release of the domain reset signal. Must be cleared by software. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																									ICECRUSHER_SEQ2_RST2ST	ICECRUSHER_SEQ1_RST1ST	EMULATION_SEQ2_RST2ST	EMULATION_SEQ1_RST1ST	RST3ST	RST2ST	RST1ST

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Bits	Field Name	Description	Type	Reset
31:7	RESERVED		R	0x0000000
6	ICECRUSHER_SEQ2_RST2ST	Sequencer2 CPU has been reset due to IVAHD ICECRUSHER2 reset event 0x0: No icecrusher reset 0x1: Sequencer2 has been reset upon icecrusher reset	RW W1toClr	0
5	ICECRUSHER_SEQ1_RST1ST	Sequencer1 CPU has been reset due to IVAHD ICECRUSHER1 reset event 0x0: No icecrusher reset 0x1: Sequencer1 has been reset upon icecrusher reset	RW W1toClr	0
4	EMULATION_SEQ2_RST2ST	0x0: No emulation reset 0x1: Sequencer2 has been reset upon emulation reset	RW W1toClr	0
3	EMULATION_SEQ1_RST1ST	Sequencer1 CPU has been reset due to emulation reset source e.g. assert reset command initiated by the icepick module 0x0: No emulation reset 0x1: Sequencer1 has been reset upon emulation reset	RW W1toClr	0
2	RST3ST	IVAHD logic and SL2 software reset 0x0: No software reset occured 0x1: IVAHD logic and SL2 has been reset upon software reset	RW W1toClr	0
1	RST2ST	IVAHD Sequencer2 CPU software reset 0x0: No software reset occured 0x1: Sequencer2 has been reset upon software reset	RW W1toClr	0
0	RST1ST	IVAHD Sequencer1 CPU software reset 0x0: No software reset occured 0x1: Sequencer1 has been reset upon software reset	RW W1toClr	0

Table 3-508. Register Call Summary for Register RM_IVAHD_RSTST

PRCM Register Manual
- IVAHD_PRM Register Summary: [0]

Table 3-509. RM_IVAHD_IVAHD_CONTEXT

Address Offset	0x0000 0024		
Physical Address	0x4A30 6F24	**Instance**	IVAHD_PRM
Description	This register contains dedicated IVAHD context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																					LOSTMEM_HWA_MEM	LOSTMEM_TCM2_MEM	LOSTMEM_TCM1_MEM	RESERVED							LOSTCONTEXT_DFF

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Bits	Field Name	Description	Type	Reset
31:11	RESERVED		R	0x000000
10	LOSTMEM_HWA_MEM	Specify if memory-based context in HWA_MEM memory bank has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
9	LOSTMEM_TCM2_MEM	Specify if memory-based context in TCM2_MEM memory bank has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
8	LOSTMEM_TCM1_MEM	Specify if memory-based context in TCM1_MEM memory bank has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
7:1	RESERVED		R	0x00
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of IVAHD_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-510. Register Call Summary for Register RM_IVAHD_IVAHD_CONTEXT

Power Management Functional Description • PD_IVAHD Description: [0]
PRCM Register Manual • IVAHD_PRM Register Summary: [1]

Table 3-511. RM_IVAHD_SL2_CONTEXT

Address Offset	0x0000 002C		
Physical Address	0x4A30 6F2C	**Instance**	IVAHD_PRM
Description	This register contains dedicated SL2 context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							LOSTMEM_SL2_MEM	RESERVED							LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	LOSTMEM_SL2_MEM	Specify if memory-based context in SL2_MEM memory bank has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
7:1	RESERVED		R	0x00

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Bits	Field Name	Description	Type	Reset
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of IVAHD_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-512. Register Call Summary for Register RM_IVAHD_SL2_CONTEXT

Power Management Functional Description • PD_IVAHD Description: [0]
PRCM Register Manual • IVAHD_PRM Register Summary: [1]

3.11.10 CAM_PRM Registers

3.11.10.1 CAM_PRM Register Summary

Table 3-513. CAM_PRM Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	CAM_PRM L4 Base Address
PM_CAM_PWRSTCTRL	RW	32	0x0000 0000	0x4A30 7000
PM_CAM_PWRSTST	RW	32	0x0000 0004	0x4A30 7004
RM_CAM_ISS_CONTEXT	RW	32	0x0000 0024	0x4A30 7024
RM_CAM_FDIF_CONTEXT	RW	32	0x0000 002C	0x4A30 702C

3.11.10.2 CAM_PRM Register Description

Table 3-514. PM_CAM_PWRSTCTRL

Address Offset	0x0000 0000		
Physical Address	0x4A30 7000	**Instance**	CAM_PRM
Description	This register controls the CAM power state to reach upon a domain sleep transition		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														CAM_MEM_ONSTATE		RESERVED											LOWPOWERSTATECHANGE	RESERVED			POWERSTATE

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	CAM_MEM_ONSTATE	CAM_MEM memory state when domain is ON. Read 0x3: Memory bank is on when the domain is ON.	R Rreturns 1s	0x3

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Bits	Field Name	Description	Type	Reset
15:5	RESERVED		R	0x000
4	LOWPOWERSTATECHANGE	Power state change request when domain has already performed a sleep transition. Allows going into deeper low power state without waking up the power domain. 0x0: Do not request a low power state change. 0x1: Request a low power state change. This bit is automatically cleared when the power state is effectively changed or when power state is ON.	RW WSpecial	0
3:2	RESERVED		R	0x0
1:0	POWERSTATE	Power state control 0x0: OFF state Read 0x1: Reserved 0x2: INACTIVE state 0x3: ON State	RW	0x0

Table 3-515. Register Call Summary for Register PM_CAM_PWRSTCTRL

Power Management Functional Description • Power Domain Modes: [0] [1] [2]
PRCM Register Manual • CAM_PRM Register Summary: [3]

Table 3-516. PM_CAM_PWRSTST

Address Offset	0x0000 0004		
Physical Address	0x4A30 7004	**Instance**	CAM_PRM
Description	This register provides a status on the current CAM power domain state. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								LASTPOWERSTATEENTERED		RESERVED			INTRANSITION		RESERVED											CAM_MEM_STATEST		RESERVED		LOGICSTATEST		POWERSTATEST	

Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x00
25:24	LASTPOWERSTATEENTERED	Last low power state entered. Set to 0x3 upon write of the same only. This register is intended for debug purpose only. Read 0x3: Power domain was previously ON-ACTIVE Read 0x2: Power domain was previously ON-INACTIVE Read 0x1: Power domain was previously in RETENTION Read 0x0: Power domain was previously OFF	RW W1toSet	0x0
23:21	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
20	INTRANSITION	Domain transition status Read 0x1: Power domain transition is in progress. Read 0x0: No on-going transition on power domain	R	0
19:6	RESERVED		R	0x0000
5:4	CAM_MEM_STATEST	CAM_MEM memory state status Read 0x3: Memory is ON Read 0x2: Reserved Read 0x1: Reserved Read 0x0: Memory is OFF	R	0x3
3	RESERVED		R	0
2	LOGICSTATEST	Logic state status Read 0x1: Logic in domain is ON Read 0x0: Logic in domain is OFF	R	1
1:0	POWERSTATEST	Current power state status Read 0x3: Power domain is ON-ACTIVE Read 0x2: Power domain is ON-INACTIVE Read 0x1: Power domain is in RETENTION Read 0x0: Power domain is OFF	R	0x3

Table 3-517. Register Call Summary for Register PM_CAM_PWRSTST

Power Management Functional Description • Power Domain Modes: [0] [1] [2] [3]
PRCM Register Manual • CAM_PRM Register Summary: [4]

Table 3-518. RM_CAM_ISS_CONTEXT

Address Offset	0x0000 0024		
Physical Address	0x4A30 7024	**Instance**	CAM_PRM
Description	This register contains dedicated ISS context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							LOSTMEM_CAM_MEM	RESERVED							LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	LOSTMEM_CAM_MEM	Specify if memory-based context in CAM_MEM memory bank has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
7:1	RESERVED		R	0x00

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Bits	Field Name	Description	Type	Reset
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CAM_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-519. Register Call Summary for Register RM_CAM_ISS_CONTEXT

Power Management Functional Description • PD_CAM Description: [0]
PRCM Register Manual • CAM_PRM Register Summary: [1]

Table 3-520. RM_CAM_FDIF_CONTEXT

Address Offset	0x0000 002C		
Physical Address	0x4A30 702C	**Instance**	CAM_PRM
Description	This register contains dedicated FDIF context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							LOSTMEM_CAM_MEM	RESERVED							LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	LOSTMEM_CAM_MEM	Specify if memory-based context in CAM_MEM memory bank has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
7:1	RESERVED		R	0x00
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CAM_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-521. Register Call Summary for Register RM_CAM_FDIF_CONTEXT

Power Management Functional Description • PD_CAM Description: [0]
PRCM Register Manual • CAM_PRM Register Summary: [1]

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3.11.11 DSS_PRM Registers

3.11.11.1 DSS_PRM Register Summary

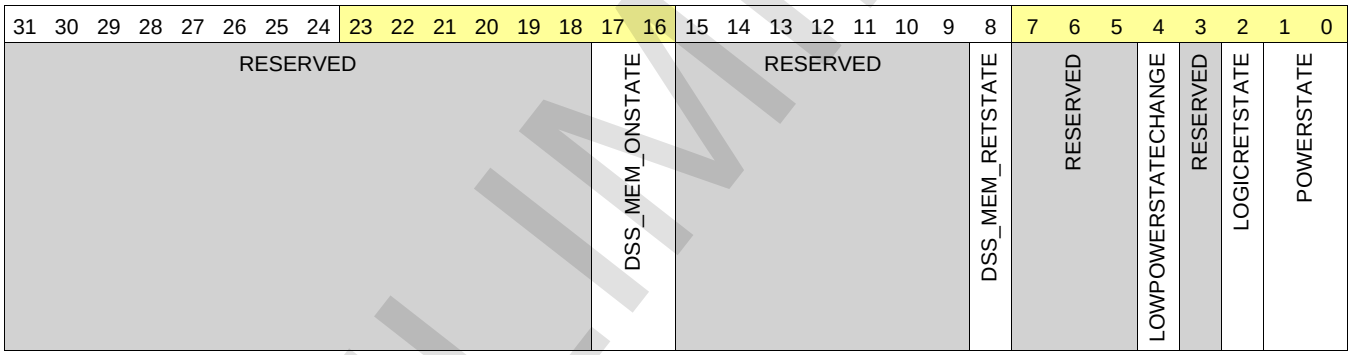
Table 3-522. DSS_PRM Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	DSS_PRM L4 Base Address
PM_DSS_PWRSTCTRL	RW	32	0x0000 0000	0x4A30 7100
PM_DSS_PWRSTST	R	32	0x0000 0004	0x4A30 7104
PM_DSS_DSS_WKDEP	RW	32	0x0000 0020	0x4A30 7120
RM_DSS_DSS_CONTEXT	RW	32	0x0000 0024	0x4A30 7124

3.11.11.2 DSS_PRM Register Description

Table 3-523. PM_DSS_PWRSTCTRL

Address Offset	0x0000 0000		
Physical Address	0x4A30 7100	**Instance**	DSS_PRM
Description	This register controls the DSS power state to reach upon a domain sleep transition		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	DSS_MEM_ONSTATE	DSS_MEM state when domain is ON. Read 0x3: Memory bank is on when the domain is ON.	R Rreturns 1s	0x3
15:9	RESERVED		R	0x00
8	DSS_MEM_RETSTATE	DSS_MEM state when domain is RETENTION. Read 0x0: Memory bank is off when the domain is in the RETENTION state.	R	0
7:5	RESERVED		R	0x0
4	LOWPOWERSTATECHANGE	Power state change request when domain has already performed a sleep transition. Allows going into deeper low power state without waking up the power domain. 0x0: Do not request a low power state change. 0x1: Request a low power state change. This bit is automatically cleared when the power state is effectively changed or when power state is ON.	RW WSpecial	0
3	RESERVED		R	0

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Bits	Field Name	Description	Type	Reset
2	LOGICRETSTATE	Logic state when power domain is RETENTION Read 0x0: Whole logic is off when the domain is in RETENTION state.	R	0
1:0	POWERSTATE	Power state control 0x0: OFF state 0x1: RETENTION state 0x2: INACTIVE state 0x3: ON State	RW	0x0

Table 3-524. Register Call Summary for Register PM_DSS_PWRSTCTRL

Power Management Functional Description • Power Domain Modes: [0] [1] [2] [3] [4]
PRCM Register Manual • DSS_PRM Register Summary: [5]

Table 3-525. PM_DSS_PWRSTST

Address Offset	0x0000 0004		
Physical Address	0x4A30 7104	**Instance**	DSS_PRM
Description	This register provides a status on the current DSS power domain state. [warm reset insensitive]		
Type	R		

31 30 29 28 27 26	25 24	23 22 21	20	19 18 17 16	15 14 13 12 11 10 9 8	7 6	5 4	3	2	1 0
RESERVED	LASTPOWERSTATEENTERED	RESERVED	INTRANSITION	RESERVED			DSS_MEM_STATEST	RESERVED	LOGICSTATEST	POWERSTATEST

Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x00
25:24	LASTPOWERSTATEENTERED	Last low power state entered. Set to 0x3 upon write of the same only. This register is intended for debug purpose only. Read 0x3: Power domain was previously OFF Read 0x2: Power domain was previously in RETENTION Read 0x1: Power domain was previously ON-INACTIVE Read 0x0: Power domain was previously ON-ACTIVE	RW W1toSet	0x0
23:21	RESERVED		R	0x0
20	INTRANSITION	Domain transition status Read 0x0: No ongoing transition on power domain Read 0x1: Power domain transition is in progress.	R	0
19:6	RESERVED		R	0x0000

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Bits	Field Name	Description	Type	Reset
5:4	DSS_MEM_STATEST	DSS_MEM state status Read 0x0: Memory is OFF Read 0x1: Reserved Read 0x2: Reserved Read 0x3: Memory is ON	R	0x3
3	RESERVED		R	0
2	LOGICSTATEST	Logic state status Read 0x0: Logic in domain is OFF Read 0x1: Logic in domain is ON	R	1
1:0	POWERSTATEST	Current power state status Read 0x0: Power domain is OFF Read 0x1: Power domain is in RETENTION Read 0x2: Power domain is ON-INACTIVE Read 0x3: Power domain is ON-ACTIVE	R	0x3

Table 3-526. Register Call Summary for Register PM_DSS_PWRSTST

Power Management Functional Description
- Power Domain Modes: [0] [1] [2] [3]

PRCM Register Manual
- DSS_PRM Register Summary: [4]

Table 3-527. PM_DSS_DSS_WKDEP

Address Offset	0x0000 0020		
Physical Address	0x4A30 7120	**Instance**	DSS_PRM
Description	This register controls wakeup dependency based on DSS service requests.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												WKUPDEP_HDMIDMA_SDMA	RESERVED			WKUPDEP_HDMIIRQ_DSP	WKUPDEP_HDMIIRQ_MPU_M3	WKUPDEP_HDMIIRQ_MPU	WKUPDEP_DSI2_SDMA	WKUPDEP_DSI2_DSP	WKUPDEP_DSI2_MPU_M3	WKUPDEP_DSI2_MPU	WKUPDEP_DSI1_SDMA	WKUPDEP_DSI1_DSP	WKUPDEP_DSI1_MPU_M3	WKUPDEP_DSI1_MPU	WKUPDEP_DISPC_SDMA	WKUPDEP_DISPC_DSP	WKUPDEP_DISPC_MPU_M3	WKUPDEP_DISPC_MPU

Bits	Field Name	Description	Type	Reset
31:20	RESERVED		R	0x000
19	WKUPDEP_HDMIDMA_SDMA	Wakeup dependency from HDMI module (SWakeup_HDMI_dma signal) towards SDMA + L3_2 domains Read 0x1: Dependency is enabled	R Rreturns 1s	1
18:15	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
14	WKUPDEP_HDMIIRQ_DSP	Wakeup dependency from HDMI module (softwareakeup_HDMI_irq signal) towards DSP + L3_1 + L3_2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
13	WKUPDEP_HDMIIRQ_MPU_M3	Wakeup dependency from HDMI module (softwareakeup_HDMI_irq signal) towards MPU_A3 + L3_2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
12	WKUPDEP_HDMIIRQ_MPU	Wakeup dependency from HDMI module (softwareakeup_HDMI_irq signal) towards MPU + L3_1 + L3_2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
11	WKUPDEP_DSI2_SDMA	Wakeup dependency from DSI2 module (softwareakeup_DSI2 signal) towards SDMA + L3_2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
10	WKUPDEP_DSI2_DSP	Wakeup dependency from DSI2 module (softwareakeup_DSI2 signal) towards DSP + L3_1 + L3_2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
9	WKUPDEP_DSI2_MPU_M3	Wakeup dependency from DSI2 module (softwareakeup_DSI2 signal) towards MPU_A3 + L3_2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
8	WKUPDEP_DSI2_MPU	Wakeup dependency from DSI2 module (softwareakeup_DSI2 signal) towards MPU + L3_1 + L3_2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
7	WKUPDEP_DSI1_SDMA	Wakeup dependency from DSI1 module (softwareakeup_DSI1 signal) towards SDMA + L3_2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
6	WKUPDEP_DSI1_DSP	Wakeup dependency from DSI1 module (softwareakeup_DSI1 signal) towards DSP + L3_1 + L3_2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
5	WKUPDEP_DSI1_MPU_M3	Wakeup dependency from DSI1 module (softwareakeup_DSI1 signal) towards MPU_A3 + L3_2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
4	WKUPDEP_DSI1_MPU	Wakeup dependency from DSI1 module (softwareakeup_DSI1 signal) towards MPU + L3_1 + L3_2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

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Bits	Field Name	Description	Type	Reset
3	WKUPDEP_DISPC_SDMA	Wakeup dependency from DISPC module (softwareakeup_DISPC signal) towards SDMA + L3_2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
2	WKUPDEP_DISPC_DSP	Wakeup dependency from DISPC module (softwareakeup_DISPC signal) towards DSP + L3_1 + L3_2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
1	WKUPDEP_DISPC_MPU_M3	Wakeup dependency from DISPC module (softwareakeup_DISPC signal) towards MPU_A3 + L3_2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
0	WKUPDEP_DISPC_MPU	Wakeup dependency from DISPC module (softwareakeup_DISPC signal) towards MPU + L3_1 + L3_2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-528. Register Call Summary for Register PM_DSS_DSS_WKDEP

Clock Management Functional Description
- Clock Domain Dependency: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15]

PRCM Register Manual
- DSS_PRM Register Summary: [16]

Table 3-529. RM_DSS_DSS_CONTEXT

Address Offset	0x0000 0024		
Physical Address	0x4A30 7124	**Instance**	DSS_PRM
Description	This register contains dedicated DSS context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							LOSTMEM_DSS_MEM	RESERVED						LOSTCONTEXT_RFF	LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	LOSTMEM_DSS_MEM	Specify if memory-based context in DSS_MEM memory bank has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
7:2	RESERVED		R	0x00

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Bits	Field Name	Description	Type	Reset
1	LOSTCONTEXT_RFF	Specify if RFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of DSS_RET_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of DSS_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-530. Register Call Summary for Register RM_DSS_DSS_CONTEXT

Power Management Functional Description • PD_DSS Description: [0] [1]
PRCM Register Manual • DSS_PRM Register Summary: [2]

3.11.12 SGX_PRM Registers

3.11.12.1 SGX_PRM Register Summary

Table 3-531. SGX_PRM Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	SGX_PRM L4 Base Address
PM_SGX_PWRSTCTRL	RW	32	0x0000 0000	0x4A30 7200
PM_SGX_PWRSTST	R	32	0x0000 0004	0x4A30 7204
RM_SGX_SGX_CONTEXT	RW	32	0x0000 0024	0x4A30 7224

3.11.12.2 SGX_PRM Register Description

Table 3-532. PM_SGX_PWRSTCTRL

Address Offset	0x0000 0000		
Physical Address	0x4A30 7200	**Instance**	SGX_PRM
Description	This register controls the SGX power state to reach upon a domain sleep transition		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														SGX_MEM_ONSTATE		RESERVED											LOWPOWERSTATECHANGE	RESERVED		POWERSTATE	

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Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	SGX_MEM_ONSTATE	SGX_MEM memory bank state when domain is ON. Read 0x3: Memory bank is on when the domain is ON.	R Rreturns 1s	0x3
15:5	RESERVED		R	0x000
4	LOWPOWERSTATECHANGE	Power state change request when domain has already performed a sleep transition. Allows going into deeper low power state without waking up the power domain. 0x0: Do not request a low power state change. 0x1: Request a low power state change. This bit is automatically cleared when the power state is effectively changed or when power state is ON.	RW WSpecial	0
3:2	RESERVED		R	0x0
1:0	POWERSTATE	Power state control 0x0: OFF state 0x1: Reserved 0x2: INACTIVE state 0x3: ON State	RW	0x0

Table 3-533. Register Call Summary for Register PM_SGX_PWRSTCTRL

Power Management Functional Description • Power Domain Modes: [0] [1] [2]
PRCM Register Manual • SGX_PRM Register Summary: [3]

Table 3-534. PM_SGX_PWRSTST

Address Offset	0x0000 0004		
Physical Address	0x4A30 7204	**Instance**	SGX_PRM
Description	This register provides a status on the current SGX power domain state. [warm reset insensitive]		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						LASTPOWERSTATEENTERED		RESERVED			INTRANSITION	RESERVED												SGX_MEM_STATEST		RESERVED		LOGICSTATEST		POWERSTATEST	

Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x00
25:24	LASTPOWERSTATEENTERED	Last low power state entered. Set to 0x3 upon write of the same only. This register is intended for debug purpose only. Read 0x0: Power domain was previously OFF Read 0x1: Power domain was previously in RETENTION Read 0x2: Power domain was previously ON-INACTIVE Read 0x3: Power domain was previously ON-ACTIVE	RW W1toSet	0x0

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Bits	Field Name	Description	Type	Reset
23:21	RESERVED		R	0x0
20	INTRANSITION	Domain transition status Read 0x0: No ongoing transition on power domain Read 0x1: Power domain transition is in progress.	R	0
19:6	RESERVED		R	0x0000
5:4	SGX_MEM_STATEST	SGX_MEM memory bank state status Read 0x0: Memory is OFF Read 0x1: Reserved Read 0x2: Reserved Read 0x3: Memory is ON	R	0x3
3	RESERVED		R	0
2	LOGICSTATEST	Logic state status Read 0x0: Logic in domain is OFF Read 0x1: Logic in domain is ON	R	1
1:0	POWERSTATEST	Current power state status Read 0x0: Power domain is OFF Read 0x1: Power domain is in RETENTION Read 0x2: Power domain is ON-INACTIVE Read 0x3: Power domain is ON-ACTIVE	R	0x3

Table 3-535. Register Call Summary for Register PM_SGX_PWRSTST

Power Management Functional Description
- Power Domain Modes: [0] [1] [2] [3]

PRCM Register Manual
- SGX_PRM Register Summary: [4]

Table 3-536. RM_SGX_SGX_CONTEXT

Address Offset	0x0000 0024		
Physical Address	0x4A30 7224	**Instance**	SGX_PRM
Description	This register contains dedicated SGX context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							LOSTMEM_SGX_MEM	RESERVED							LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	LOSTMEM_SGX_MEM	Specify if memory-based context in SGX_MEM memory bank has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
7:1	RESERVED		R	0x00

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Bits	Field Name	Description	Type	Reset
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of SGX_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-537. Register Call Summary for Register RM_SGX_SGX_CONTEXT

Power Management Functional Description • PD_SGX Description: [0]
PRCM Register Manual • SGX_PRM Register Summary: [1]

3.11.13 L3INIT_PRM Registers

3.11.13.1 L3INIT_PRM Register Summary

Table 3-538. L3INIT_PRM Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	L3INIT_PRM L4 Base Address
PM_L3INIT_PWRSTCTRL	RW	32	0x0000 0000	0x4A30 7300
PM_L3INIT_PWRSTST	R	32	0x0000 0004	0x4A30 7304
PM_L3INIT_MMC1_WKDEP	RW	32	0x0000 0028	0x4A30 7328
RM_L3INIT_MMC1_CONTEXT	RW	32	0x0000 002C	0x4A30 732C
PM_L3INIT_MMC2_WKDEP	RW	32	0x0000 0030	0x4A30 7330
RM_L3INIT_MMC2_CONTEXT	RW	32	0x0000 0034	0x4A30 7334
PM_L3INIT_HSI_WKDEP	RW	32	0x0000 0038	0x4A30 7338
RM_L3INIT_HSI_CONTEXT	RW	32	0x0000 003C	0x4A30 733C
RESERVED	RW	32	0x0000 0040	0x4A30 7340
RESERVED	RW	32	0x0000 0044	0x4A30 7344
PM_L3INIT_HSUSBHOST_WKDEP	RW	32	0x0000 0058	0x4A30 7358
RM_L3INIT_HSUSBHOST_CONTEXT	RW	32	0x0000 005C	0x4A30 735C
PM_L3INIT_HSUSBOTG_WKDEP	RW	32	0x0000 0060	0x4A30 7360
RM_L3INIT_HSUSBOTG_CONTEXT	RW	32	0x0000 0064	0x4A30 7364
PM_L3INIT_HSUSBTLL_WKDEP	RW	32	0x0000 0068	0x4A30 7368
RM_L3INIT_HSUSBTLL_CONTEXT	RW	32	0x0000 006C	0x4A30 736C
RESERVED	RW	32	0x0000 007C	0x4A30 737C
RESERVED	RW	32	0x0000 0084	0x4A30 7384
RESERVED	RW	32	0x0000 0088	0x4A30 7388
RESERVED	RW	32	0x0000 008C	0x4A30 738C
RESERVED	RW	32	0x0000 0094	0x4A30 7394
RESERVED	RW	32	0x0000 0098	0x4A30 7398
RESERVED	RW	32	0x0000 009C	0x4A30 739C
RESERVED	RW	32	0x0000 00AC	0x4A30 73AC
RESERVED	R	32	0x0000 00C0	0x4A30 73C0
RESERVED	RW	32	0x0000 00C4	0x4A30 73C4
RESERVED	RW	32	0x0000 00C8	0x4A30 73C8
RESERVED	RW	32	0x0000 00CC	0x4A30 73CC
PM_L3INIT_FSUSB_WKDEP	RW	32	0x0000 00D0	0x4A30 73D0

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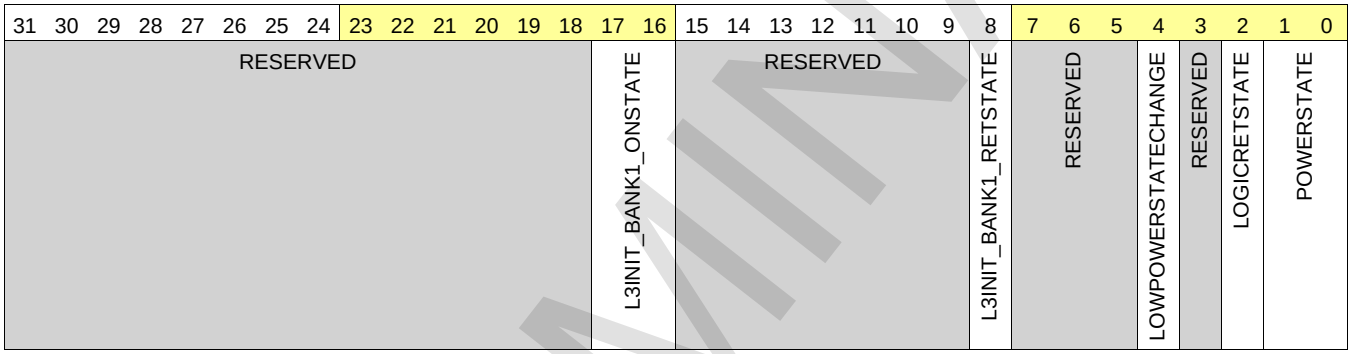
Table 3-538. L3INIT_PRM Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	L3INIT_PRM L4 Base Address
RM_L3INIT_FSUSB_CONTEXT	RW	32	0x0000 00D4	0x4A30 73D4
RM_L3INIT_USBPHY_CONTEXT	RW	32	0x0000 00E4	0x4A30 73E4

3.11.13.2 L3INIT_PRM Register Description

Table 3-539. PM_L3INIT_PWRSTCTRL

Address Offset	0x0000 0000		
Physical Address	0x4A30 7300	**Instance**	L3INIT_PRM
Description	This register controls the L3INIT power state to reach upon a domain sleep transition		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	L3INIT_BANK1_ONSTATE	L3INIT BANK state when domain is ON. Read 0x3: Memory bank is on when the domain is ON.	R Rreturns 1s	0x3
15:9	RESERVED		R	0x00
8	L3INIT_BANK1_RETSTATE	L3INIT BANK1 state when domain is RETENTION. Read 0x0: Memory bank is off when the domain is in the RETENTION state.	R	0
7:5	RESERVED		R	0x0
4	LOWPOWERSTATECHANGE	Power state change request when domain has already performed a sleep transition. Allows going into deeper low power state without waking up the power domain. 0x0: Do not request a low power state change. 0x1: Request a low power state change. This bit is automatically cleared when the power state is effectively changed or when power state is ON.	RW WSpecial	0
3	RESERVED		R	0
2	LOGICRETSTATE	Logic state when power domain is RETENTION 0x0: Only retention registers are retained and remaing logic is off when the domain is in RETENTION state. 0x1: Whole logic is retained when domain is in RETENTION state.	RW	1

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Bits	Field Name	Description	Type	Reset
1:0	POWERSTATE	Power state control 0x0: OFF state 0x1: RETENTION state 0x2: INACTIVE state 0x3: ON State	RW	0x0

Table 3-540. Register Call Summary for Register PM_L3INIT_PWRSTCTRL

Power Management Functional Description • Power Domain Modes: [0] [1] [2] [3] [4]
PRCM Register Manual • L3INIT_PRM Register Summary: [5]

Table 3-541. PM_L3INIT_PWRSTST

Address Offset	0x0000 0004		
Physical Address	0x4A30 7304	**Instance**	L3INIT_PRM
Description	This register provides a status on the current L3INIT power domain state. [warm reset insensitive]		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						LASTPOWERSTATEENTERED		RESERVED			INTRANSITION	RESERVED												L3INIT_BANK1_STATEST		RESERVED		LOGICSTATEST		POWERSTATEST	

Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x00
25:24	LASTPOWERSTATEENTERED	Last low power state entered. Set to 0x3 upon write of the same only. This register is intended for debug purpose only. Read 0x3: Power domain was previously ON-ACTIVE Read 0x2: Power domain was previously ON-INACTIVE Read 0x1: Power domain was previously in RETENTION Read 0x0: Power domain was previously OFF	RW W1toSet	0x0
23:21	RESERVED		R	0x0
20	INTRANSITION	Domain transition status Read 0x0: No ongoing transition on power domain Read 0x1: Power domain transition is in progress.	R	0
19:6	RESERVED		R	0x0000
5:4	L3INIT_BANK1_STATEST	L3INIT BANK1 state status Read 0x0: Memory is OFF Read 0x1: Reserved Read 0x2: Reserved Read 0x3: Memory is ON	R	0x3
3	RESERVED		R	0

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Bits	Field Name	Description	Type	Reset
2	LOGICSTATEST	Logic state status Read 0x0: Logic in domain is OFF Read 0x1: Logic in domain is ON	R	1
1:0	POWERSTATEST	Current power state status Read 0x0: Power domain is OFF Read 0x1: Power domain is in RETENTION Read 0x2: Power domain is ON-INACTIVE Read 0x3: Power domain is ON-ACTIVE	R	0x3

Table 3-542. Register Call Summary for Register PM_L3INIT_PWRSTST

Power Management Functional Description • Power Domain Modes: [0] [1] [2] [3] [4]
PRCM Register Manual • L3INIT_PRM Register Summary: [5]

Table 3-543. PM_L3INIT_MMC1_WKDEP

Address Offset	0x0000 0028		
Physical Address	0x4A30 7328	**Instance**	L3INIT_PRM
Description	This register controls wakeup dependency based on MMC1 service requests.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												WKUPDEP_MMC1_SDMA	WKUPDEP_MMC1_DSP	WKUPDEP_MMC1_MPU_M3	WKUPDEP_MMC1_MPU

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0000000
3	WKUPDEP_MMC1_SDMA	Wakeup dependency from MMC1 module (softwareakeup signal) towards SDMA + L3_2 + L4PER domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
2	WKUPDEP_MMC1_DSP	Wakeup dependency from MMC1 module (softwareakeup signal) towards DSP + L3_1 + L3_2 + L4_PER domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
1	WKUPDEP_MMC1_MPU_M3	Wakeup dependency from MMC1 module (softwareakeup signal) towards MPU_A3 + L3_2 + L4_PER domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
0	WKUPDEP_MMC1_MPU	Wakeup dependency from MMC1 module (softwareakeup signal) towards MPU + L3_1 + L3_2 + L4_PER domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

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Table 3-544. Register Call Summary for Register PM_L3INIT_MMC1_WKDEP

Clock Management Functional Description • Clock Domain Dependency: [0] [1] [2] [3]
PRCM Register Manual • L3INIT_PRM Register Summary: [4]

Table 3-545. RM_L3INIT_MMC1_CONTEXT

Address Offset	0x0000 002C		
Physical Address	0x4A30 732C	**Instance**	L3INIT_PRM
Description	This register contains dedicated MMC1 context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							LOSTMEM_L3INIT_BANK1	RESERVED						LOSTCONTEXT_RFF	RESERVED

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	LOSTMEM_L3INIT_BANK1	Specify if memory-based context in L3INIT_BANK1 memory bank has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
7:2	RESERVED		R	0x00
1	LOSTCONTEXT_RFF	Specify if RFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of L3_INIT_RET_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
0	RESERVED		R	0

Table 3-546. Register Call Summary for Register RM_L3INIT_MMC1_CONTEXT

Power Management Functional Description • PD_L3_INIT Description: [0]
PRCM Register Manual • L3INIT_PRM Register Summary: [1]

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Table 3-547. PM_L3INIT_MMC2_WKDEP

Address Offset	0x0000 0030		
Physical Address	0x4A30 7330	**Instance**	L3INIT_PRM
Description	This register controls wakeup dependency based on MMC2 service requests.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												WKUPDEP_MMC2_SDMA	WKUPDEP_MMC2_DSP	WKUPDEP_MMC2_MPU_M3	WKUPDEP_MMC2_MPU

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0000000
3	WKUPDEP_MMC2_SDMA	Wakeup dependency from MMC2 module (softwareakeup signal) towards SDMA + L3_2 + L4PER domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
2	WKUPDEP_MMC2_DSP	Wakeup dependency from MMC2 module (softwareakeup signal) towards DSP + L3_1 + L3_2 + L4_PER domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
1	WKUPDEP_MMC2_MPU_M3	Wakeup dependency from MMC2 module (softwareakeup signal) towards MPU_A3 + L3_2 + L4_PER domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
0	WKUPDEP_MMC2_MPU	Wakeup dependency from MMC2 module (softwareakeup signal) towards MPU + L3_1 + L3_2 + L4_PER domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-548. Register Call Summary for Register PM_L3INIT_MMC2_WKDEP

Clock Management Functional Description
- Clock Domain Dependency: [0] [1] [2] [3]

PRCM Register Manual
- L3INIT_PRM Register Summary: [4]

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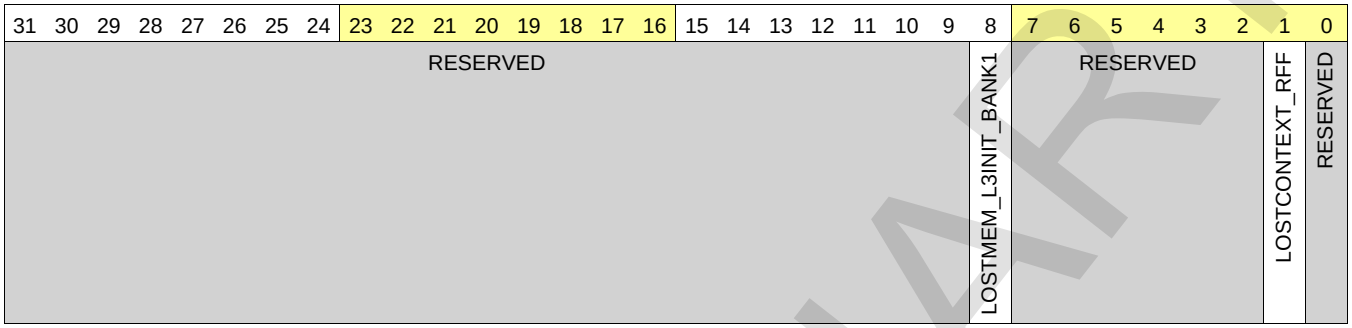
Table 3-549. RM_L3INIT_MMC2_CONTEXT

Address Offset	0x0000 0034		
Physical Address	0x4A30 7334	**Instance**	L3INIT_PRM
Description	This register contains dedicated MMC2 context statuses. [warm reset insensitive]		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	LOSTMEM_L3INIT_BANK1	Specify if memory-based context in L3INIT_BANK1 memory bank has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
7:2	RESERVED		R	0x00
1	LOSTCONTEXT_RFF	Specify if RFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of L3_INIT_RET_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
0	RESERVED		R	0

Table 3-550. Register Call Summary for Register RM_L3INIT_MMC2_CONTEXT

Power Management Functional Description
- PD_L3_INIT Description: [0]

PRCM Register Manual
- L3INIT_PRM Register Summary: [1]

Table 3-551. PM_L3INIT_HSI_WKDEP

Address Offset	0x0000 0038		
Physical Address	0x4A30 7338	**Instance**	L3INIT_PRM
Description	This register controls wakeup dependency based on HSI service requests.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							WKUPDEP_WGM_HSI_WAKE_MPU	RESERVED	WKUPDEP_HSI_DSP_DSP	RESERVED				WKUPDEP_HSI_MCU_MPU_M3	WKUPDEP_HSI_MCU_MPU

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	WKUPDEP_WGM_HSI_WAKE_MPU	Wakeup dependency from modem HSI_WAKE signal towards MPU + L3_1 + L4_CFG domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
7	RESERVED		R	0
6	WKUPDEP_HSI_DSP_DSP	Wakeup dependency from HSI module (softwareakeup_DSP signal) towards DSP + L3_1 + L4_CFG domains Read 0x1: Dependency is enabled	R Rreturns 1s	1
5:2	RESERVED		R	0x0
1	WKUPDEP_HSI_MCU_MPU_M3	Wakeup dependency from HSI module (softwareakeup_MPU signal) towards MPU_A3 + L3_2 + L3_1 + L4_CFG domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
0	WKUPDEP_HSI_MCU_MPU	Wakeup dependency from HSI module (softwareakeup_MPU signal) towards MPU + L3_1 + L4_CFG domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-552. Register Call Summary for Register PM_L3INIT_HSI_WKDEP

Clock Management Functional Description • Clock Domain Dependency: [0] [1] [2] [3]
PRCM Register Manual • L3INIT_PRM Register Summary: [4]

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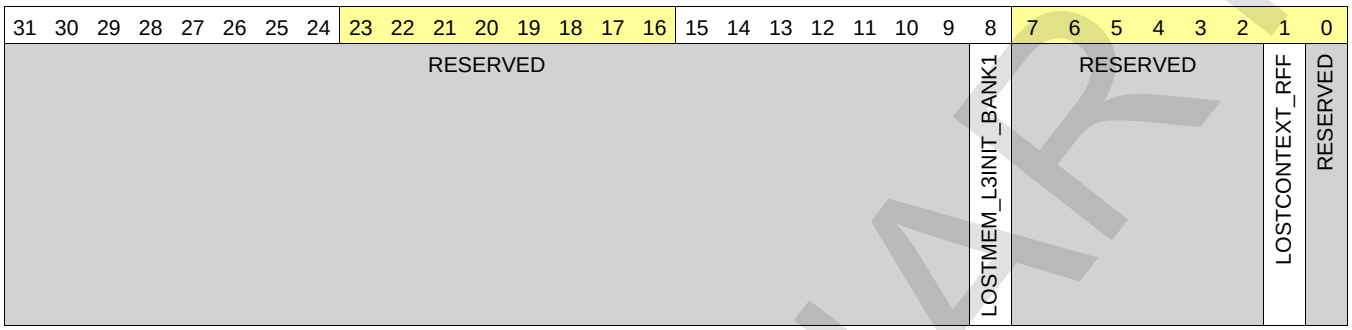
Table 3-553. RM_L3INIT_HSI_CONTEXT

Address Offset	0x0000 003C		
Physical Address	0x4A30 733C	**Instance**	L3INIT_PRM
Description	This register contains dedicated HSI context statuses. [warm reset insensitive]		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	LOSTMEM_L3INIT_BANK1	Specify if memory-based context in L3INIT_BANK1 memory bank has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
7:2	RESERVED		R	0x00
1	LOSTCONTEXT_RFF	Specify if RFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of L3_INIT_RET_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
0	RESERVED		R	0

Table 3-554. Register Call Summary for Register RM_L3INIT_HSI_CONTEXT

Power Management Functional Description
- PD_L3_INIT Description: [0]

PRCM Register Manual
- L3INIT_PRM Register Summary: [1]

Table 3-555. PM_L3INIT_HSUSBHOST_WKDEP

Address Offset	0x0000 0058		
Physical Address	0x4A30 7358	**Instance**	L3INIT_PRM
Description	This register controls wakeup dependency based on USB_HOST_HS service requests.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														WKUPDEP_HSUSBHOST_MPU_M3	WKUPDEP_HSUSBHOST_MPU

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	WKUPDEP_HSUSBHOST_MPU_M3	Wakeup dependency from USB_HOST_HS module (softwareakeup signal) towards MPU_A3 + L3_2 + L3_1 + L4_CFG domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
0	WKUPDEP_HSUSBHOST_MPU	Wakeup dependency from USB_HOST_HS module (softwareakeup signal) towards MPU + L3_1 + L4_CFG domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-556. Register Call Summary for Register PM_L3INIT_HSUSBHOST_WKDEP

Clock Management Functional Description • Clock Domain Dependency: [0] [1]
PRCM Register Manual • L3INIT_PRM Register Summary: [2]

Table 3-557. RM_L3INIT_HSUSBHOST_CONTEXT

Address Offset	0x0000 005C		
Physical Address	0x4A30 735C	**Instance**	L3INIT_PRM
Description	This register contains dedicated USB_HOST context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														LOSTCONTEXT_RFF	RESERVED

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Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	LOSTCONTEXT_RFF	Specify if RFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of L3_INIT_RET_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
0	RESERVED		R	0

Table 3-558. Register Call Summary for Register RM_L3INIT_HSUSBHOST_CONTEXT

PRCM Register Manual
- L3INIT_PRM Register Summary: [0]

Table 3-559. PM_L3INIT_HSUSBOTG_WKDEP

Address Offset	0x0000 0060		
Physical Address	0x4A30 7360	**Instance**	L3INIT_PRM
Description	This register controls wakeup dependency based on USB_OTG_HS service requests.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														WKUPDEP_HSUSBOTG_MPU_M3	WKUPDEP_HSUSBOTG_MPU

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	WKUPDEP_HSUSBOTG_MPU_M3	Wakeup dependency from USB_OTG_HS module (softwareakeup signal) towards MPU_A3 + L3_2 + L3_1 + L4_CFG domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
0	WKUPDEP_HSUSBOTG_MPU	Wakeup dependency from USB_OTG_HS module (softwareakeup signal) towards MPU + L3_1 + L4_CFG domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-560. Register Call Summary for Register PM_L3INIT_HSUSBOTG_WKDEP

Clock Management Functional Description
- Clock Domain Dependency: [0] [1]

PRCM Register Manual
- L3INIT_PRM Register Summary: [2]

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Table 3-561. RM_L3INIT_HSUSBOTG_CONTEXT

Address Offset	0x0000 0064		
Physical Address	0x4A30 7364	**Instance**	L3INIT_PRM
Description	This register contains dedicated USB_OTG_HS context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							LOSTMEM_L3INIT_BANK1	RESERVED						LOSTCONTEXT_RFF	RESERVED

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	LOSTMEM_L3INIT_BANK1	Specify if memory-based context in L3INIT_BANK1 memory bank has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
7:2	RESERVED		R	0x00
1	LOSTCONTEXT_RFF	Specify if RFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of L3_INIT_RET_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
0	RESERVED		R	0

Table 3-562. Register Call Summary for Register RM_L3INIT_HSUSBOTG_CONTEXT

PRCM Register Manual
- L3INIT_PRM Register Summary: [0]

Table 3-563. PM_L3INIT_HSUSBTLL_WKDEP

Address Offset	0x0000 0068		
Physical Address	0x4A30 7368	**Instance**	L3INIT_PRM
Description	This register controls wakeup dependency based on USB_TLL service requests.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														WKUPDEP_HSUSBTLL_MPU_M3	WKUPDEP_HSUSBTLL_MPU

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	WKUPDEP_HSUSBTLL_MPU_M3	Wakeup dependency from USB_TLL module (softwareakeup signal) towards MPU_A3 + L3_2 + L3_1 + L4_CFG domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
0	WKUPDEP_HSUSBTLL_MPU	Wakeup dependency from USB_TLL module (softwareakeup signal) towards MPU + L3_1 + L4_CFG domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-564. Register Call Summary for Register PM_L3INIT_HSUSBTLL_WKDEP

Clock Management Functional Description • Clock Domain Dependency: [0] [1]
PRCM Register Manual • L3INIT_PRM Register Summary: [2]

Table 3-565. RM_L3INIT_HSUSBTLL_CONTEXT

Address Offset	0x0000 006C		
Physical Address	0x4A30 736C	**Instance**	L3INIT_PRM
Description	This register contains dedicated USB_TLL context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														LOSTCONTEXT_RFF	RESERVED

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Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	LOSTCONTEXT_RFF	Specify if RFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of L3_INIT_RET_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
0	RESERVED		R	0

Table 3-566. Register Call Summary for Register RM_L3INIT_HSUSBTLL_CONTEXT

Power Management Functional Description • PD_L3_INIT Description: [0]
PRCM Register Manual • L3INIT_PRM Register Summary: [1]

Table 3-567. PM_L3INIT_FSUSB_WKDEP

Address Offset	0x0000 00D0		
Physical Address	0x4A30 73D0	**Instance**	L3INIT_PRM
Description	This register controls wakeup dependency based on USB_HOST_FS service requests.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														WKUPDEP_FSUSB_MPU_M3	WKUPDEP_FSUSB_MPU

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	WKUPDEP_FSUSB_MPU_M3	Wakeup dependency from USB_HOST_FS module (softwareakeup signal) towards MPU_A3 + L3_2 + L3_1 + L4_CFG domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
0	WKUPDEP_FSUSB_MPU	Wakeup dependency from USB_HOST_FS module (softwareakeup signal) towards MPU + L3_1 + L4_CFG domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-568. Register Call Summary for Register PM_L3INIT_FSUSB_WKDEP

Clock Management Functional Description • Clock Domain Dependency: [0] [1]
PRCM Register Manual • L3INIT_PRM Register Summary: [2]

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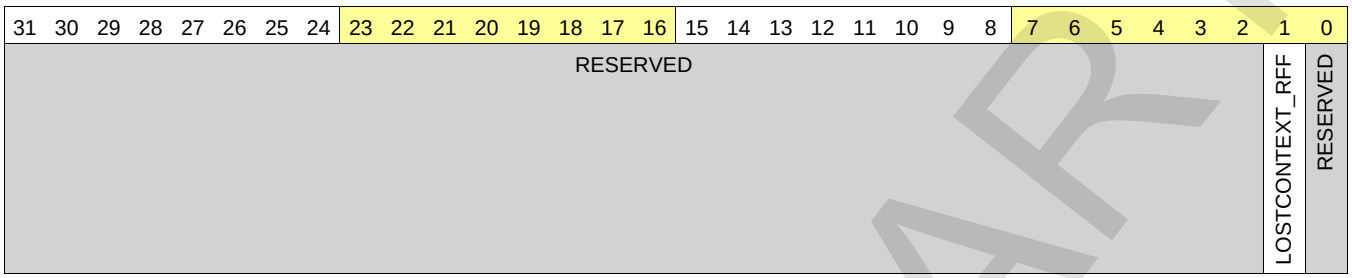
Table 3-569. RM_L3INIT_FSUSB_CONTEXT

Address Offset	0x0000 00D4		
Physical Address	0x4A30 73D4	**Instance**	L3INIT_PRM
Description	This register contains dedicated USB_HOST_FS context statuses. [warm reset insensitive]		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	LOSTCONTEXT_RFF	Specify if RFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of L3_INIT_RET_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
0	RESERVED		R	0

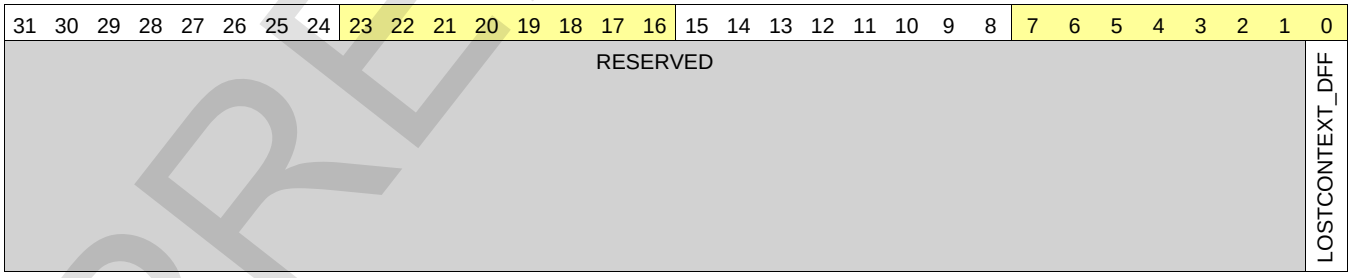
Table 3-570. Register Call Summary for Register RM_L3INIT_FSUSB_CONTEXT

PRCM Register Manual

- L3INIT_PRM Register Summary: [0]

Table 3-571. RM_L3INIT_USBPHY_CONTEXT

Address Offset	0x0000 00E4		
Physical Address	0x4A30 73E4	**Instance**	L3INIT_PRM
Description	This register contains dedicated USBPHY context statuses. [warm reset insensitive]		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of L3_INIT_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

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Table 3-572. Register Call Summary for Register RM_L3INIT_USBPHY_CONTEXT

Power Management Functional Description • PD_L3_INIT Description: [0]
PRCM Register Manual • L3INIT_PRM Register Summary: [1]

3.11.14 L4PER_PRM Registers

3.11.14.1 L4PER_PRM Register Summary

Table 3-573. L4PER_PRM Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	L4PER_PRM L4 Base Address
PM_L4PER_PWRSTCTRL	RW	32	0x0000 0000	0x4A30 7400
PM_L4PER_PWRSTST	R	32	0x0000 0004	0x4A30 7404
RESERVED	RW	32	0x0000 0024	0x4A30 7424
PM_L4PER_GPTIMER10_WKDEP	R	32	0x0000 0028	0x4A30 7428
RM_L4PER_GPTIMER10_CONTEXT	RW	32	0x0000 002C	0x4A30 742C
PM_L4PER_GPTIMER11_WKDEP	RW	32	0x0000 0030	0x4A30 7430
RM_L4PER_GPTIMER11_CONTEXT	RW	32	0x0000 0034	0x4A30 7434
PM_L4PER_GPTIMER2_WKDEP	R	32	0x0000 0038	0x4A30 7438
RM_L4PER_GPTIMER2_CONTEXT	RW	32	0x0000 003C	0x4A30 743C
PM_L4PER_GPTIMER3_WKDEP	RW	32	0x0000 0040	0x4A30 7440
RM_L4PER_GPTIMER3_CONTEXT	RW	32	0x0000 0044	0x4A30 7444
PM_L4PER_GPTIMER4_WKDEP	RW	32	0x0000 0048	0x4A30 7448
RM_L4PER_GPTIMER4_CONTEXT	RW	32	0x0000 004C	0x4A30 744C
PM_L4PER_GPTIMER9_WKDEP	RW	32	0x0000 0050	0x4A30 7450
RM_L4PER_GPTIMER9_CONTEXT	RW	32	0x0000 0054	0x4A30 7454
RM_L4PER_ELM_CONTEXT	RW	32	0x0000 005C	0x4A30 745C
PM_L4PER_GPIO2_WKDEP	RW	32	0x0000 0060	0x4A30 7460
RM_L4PER_GPIO2_CONTEXT	RW	32	0x0000 0064	0x4A30 7464
PM_L4PER_GPIO3_WKDEP	R	32	0x0000 0068	0x4A30 7468
RM_L4PER_GPIO3_CONTEXT	RW	32	0x0000 006C	0x4A30 746C
PM_L4PER_GPIO4_WKDEP	R	32	0x0000 0070	0x4A30 7470
RM_L4PER_GPIO4_CONTEXT	RW	32	0x0000 0074	0x4A30 7474
PM_L4PER_GPIO5_WKDEP	R	32	0x0000 0078	0x4A30 7478
RM_L4PER_GPIO5_CONTEXT	RW	32	0x0000 007C	0x4A30 747C
PM_L4PER_GPIO6_WKDEP	R	32	0x0000 0080	0x4A30 7480
RM_L4PER_GPIO6_CONTEXT	RW	32	0x0000 0084	0x4A30 7484
RM_L4PER_HDQ1W_CONTEXT	RW	32	0x0000 008C	0x4A30 748C
RESERVED	R	32	0x0000 0090	0x4A30 7490
RESERVED	RW	32	0x0000 0094	0x4A30 7494
RESERVED	R	32	0x0000 0098	0x4A30 7498
RESERVED	RW	32	0x0000 009C	0x4A30 749C
PM_L4PER_I2C1_WKDEP	RW	32	0x0000 00A0	0x4A30 74A0
RM_L4PER_I2C1_CONTEXT	RW	32	0x0000 00A4	0x4A30 74A4
PM_L4PER_I2C2_WKDEP	RW	32	0x0000 00A8	0x4A30 74A8
RM_L4PER_I2C2_CONTEXT	RW	32	0x0000 00AC	0x4A30 74AC
PM_L4PER_I2C3_WKDEP	RW	32	0x0000 00B0	0x4A30 74B0

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Table 3-573. L4PER_PRM Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	L4PER_PRM L4 Base Address
RM_L4PER_I2C3_CONTEXT	RW	32	0x0000 00B4	0x4A30 74B4
PM_L4PER_I2C4_WKDEP	RW	32	0x0000 00B8	0x4A30 74B8
RM_L4PER_I2C4_CONTEXT	RW	32	0x0000 00BC	0x4A30 74BC
RM_L4PER_L4_PER_CONTEXT	RW	32	0x0000 00C0	0x4A30 74C0
RESERVED	RW	32	0x0000 00D0	0x4A30 74D0
RESERVED	RW	32	0x0000 00D4	0x4A30 74D4
RESERVED	RW	32	0x0000 00D8	0x4A30 74D8
RESERVED	RW	32	0x0000 00DC	0x4A30 74DC
PM_L4PER_MCBSP4_WKDEP	RW	32	0x0000 00E0	0x4A30 74E0
RM_L4PER_MCBSP4_CONTEXT	RW	32	0x0000 00E4	0x4A30 74E4
RESERVED	RW	32	0x0000 00EC	0x4A30 74EC
PM_L4PER_MCSPI1_WKDEP	RW	32	0x0000 00F0	0x4A30 74F0
RM_L4PER_MCSPI1_CONTEXT	RW	32	0x0000 00F4	0x4A30 74F4
PM_L4PER_MCSPI2_WKDEP	RW	32	0x0000 00F8	0x4A30 74F8
RM_L4PER_MCSPI2_CONTEXT	RW	32	0x0000 00FC	0x4A30 74FC
PM_L4PER_MCSPI3_WKDEP	RW	32	0x0000 0100	0x4A30 7500
RM_L4PER_MCSPI3_CONTEXT	RW	32	0x0000 0104	0x4A30 7504
PM_L4PER_MCSPI4_WKDEP	RW	32	0x0000 0108	0x4A30 7508
RM_L4PER_MCSPI4_CONTEXT	RW	32	0x0000 010C	0x4A30 750C
PM_L4PER_MMCSD3_WKDEP	RW	32	0x0000 0120	0x4A30 7520
RM_L4PER_MMCSD3_CONTEXT	RW	32	0x0000 0124	0x4A30 7524
PM_L4PER_MMCSD4_WKDEP	RW	32	0x0000 0128	0x4A30 7528
RM_L4PER_MMCSD4_CONTEXT	RW	32	0x0000 012C	0x4A30 752C
RESERVED	RW	32	0x0000 0134	0x4A30 7534
PM_L4PER_SLIMBUS2_WKDEP	RW	32	0x0000 0138	0x4A30 7538
RM_L4PER_SLIMBUS2_CONTEXT	RW	32	0x0000 013C	0x4A30 753C
PM_L4PER_UART1_WKDEP	RW	32	0x0000 0140	0x4A30 7540
RM_L4PER_UART1_CONTEXT	RW	32	0x0000 0144	0x4A30 7544
PM_L4PER_UART2_WKDEP	RW	32	0x0000 0148	0x4A30 7548
RM_L4PER_UART2_CONTEXT	RW	32	0x0000 014C	0x4A30 754C
PM_L4PER_UART3_WKDEP	RW	32	0x0000 0150	0x4A30 7550
RM_L4PER_UART3_CONTEXT	RW	32	0x0000 0154	0x4A30 7554
PM_L4PER_UART4_WKDEP	RW	32	0x0000 0158	0x4A30 7558
RM_L4PER_UART4_CONTEXT	RW	32	0x0000 015C	0x4A30 755C
PM_L4PER_MMCSD5_WKDEP	RW	32	0x0000 0160	0x4A30 7560
RM_L4PER_MMCSD5_CONTEXT	RW	32	0x0000 0164	0x4A30 7564
RESERVED	R	32	0x0000 0168	0x4A30 7568
RESERVED	RW	32	0x0000 016C	0x4A30 756C
RESERVED	RW	32	0x0000 01A4	0x4A30 75A4
RESERVED	RW	32	0x0000 01AC	0x4A30 75AC
RESERVED	RW	32	0x0000 01B4	0x4A30 75B4
RESERVED	RW	32	0x0000 01BC	0x4A30 75BC
RESERVED	RW	32	0x0000 01C4	0x4A30 75C4
RESERVED	RW	32	0x0000 01CC	0x4A30 75CC
RESERVED	RW	32	0x0000 01DC	0x4A30 75DC

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3.11.14.2 L4PER_PRM Register Description

Table 3-574. PM_L4PER_PWRSTCTRL

Address Offset	0x0000 0000		
Physical Address	0x4A30 7400	**Instance**	L4PER_PRM
Description	This register controls the L4PER power state to reach upon a domain sleep transition		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												NONRETAINED_BANK_ONSTATE		RETAINED_BANK_ONSTATE		RESERVED							NONRETAINED_BANK_RETSTATE	RETAINED_BANK_RETSTATE	RESERVED			LOWPOWERSTATECHANGE	RESERVED	LOGICRETSTATE	POWERSTATE	

Bits	Field Name	Description	Type	Reset
31:20	RESERVED		R	0x000
19:18	NONRETAINED_BANK_ONSTATE	NONRETAINED_BANK state when domain is ON. Read 0x3: Memory bank is on when the domain is ON.	R Rreturns 1s	0x3
17:16	RETAINED_BANK_ONSTATE	RETAINED_BANK state when domain is ON. Read 0x3: Memory bank is on when the domain is ON.	R Rreturns 1s	0x3
15:10	RESERVED		R	0x00
9	NONRETAINED_BANK_RETSTATE	NONRETAINED_BANK state when domain is RETENTION. Read 0x0: Memory bank is off when the domain is in the RETENTION state.	R	0
8	RETAINED_BANK_RETSTATE	RETAINED_BANK state when domain is RETENTION. Read 0x1: Memory bank is retained when domain is in RETENTION state.	R Rreturns 1s	1
7:5	RESERVED		R	0x0
4	LOWPOWERSTATECHANGE	Power state change request when domain has already performed a sleep transition. Allows going into deeper low power state without waking up the power domain. 0x0: Do not request a low power state change. 0x1: Request a low power state change. This bit is automatically cleared when the power state is effectively changed or when power state is ON.	RW WSpecial	0
3	RESERVED		R	0
2	LOGICRETSTATE	Logic state when power domain is RETENTION 0x0: Only retention registers are retained and remaing logic is off when the domain is in RETENTION state. 0x1: Whole logic is retained when domain is in RETENTION state.	RW	1

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Bits	Field Name	Description	Type	Reset
1:0	POWERSTATE	Power state control 0x0: Reserved 0x1: RETENTION state 0x2: INACTIVE state 0x3: ON State	RW	0x3

Table 3-575. Register Call Summary for Register PM_L4PER_PWRSTCTRL

Power Management Functional Description • Power Domain Modes: [0] [1] [2] [3] [4] [5] [6]
PRCM Register Manual • L4PER_PRM Register Summary: [7]

Table 3-576. PM_L4PER_PWRSTST

Address Offset	0x0000 0004		
Physical Address	0x4A30 7404	**Instance**	L4PER_PRM
Description	This register provides a status on the current L4PER power domain state. [warm reset insensitive]		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						LASTPOWERSTATEENTERED		RESERVED			INTRANSITION	RESERVED												NONRETAINED_BANK_STATEST		RETAINED_BANK_STATEST		RESERVED	LOGICSTATEST	POWERSTATEST	

Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x00
25:24	LASTPOWERSTATEENTERED	Last low power state entered. Set to 0x3 upon write of the same only. This register is intended for debug purpose only. Read 0x3: Power domain was previously ON-ACTIVE Read 0x2: Power domain was previously ON-INACTIVE Read 0x1: Power domain was previously in RETENTION Read 0x0: Power domain was previously OFF	RW W1toSet	0x0
23:21	RESERVED		R	0x0
20	INTRANSITION	Domain transition status Read 0x0: No ongoing transition on power domain Read 0x1: Power domain transition is in progress.	R	0
19:8	RESERVED		R	0x000
7:6	NONRETAINED_BANK_STATEST	NONRETAINED_BANK state status Read 0x0: Memory is OFF Read 0x1: Reserved Read 0x2: Reserved Read 0x3: Memory is ON	R	0x3

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Bits	Field Name	Description	Type	Reset
5:4	RETAINED_BANK_STATEST	RETAINED_BANK state status Read 0x0: Memory is OFF Read 0x1: Memory is RETENTION Read 0x2: Reserved Read 0x3: Memory is ON	R	0x3
3	RESERVED		R	0
2	LOGICSTATEST	Logic state status Read 0x0: Logic in domain is OFF Read 0x1: Logic in domain is ON	R	1
1:0	POWERSTATEST	Current power state status Read 0x0: Reserved Read 0x1: Power domain is in RETENTION Read 0x2: Power domain is ON-INACTIVE Read 0x3: Power domain is ON-ACTIVE	R	0x3

Table 3-577. Register Call Summary for Register PM_L4PER_PWRSTST

Power Management Functional Description • Power Domain Modes: [0] [1] [2] [3] [4] [5]
PRCM Register Manual • L4PER_PRM Register Summary: [6]

Table 3-578. PM_L4PER_GPTIMER10_WKDEP

Address Offset	0x0000 0028		
Physical Address	0x4A30 7428	**Instance**	L4PER_PRM
Description	This register controls wakeup dependency based on DMTIMER10 service requests.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															WKUPDEP_DMTIMER10_MPU

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	WKUPDEP_DMTIMER10_MPU	Wakeup dependency from DMTIMER10 module (softwareakeup signal) towards MPU + L3_1 + L3_2 domains Read 0x1: Dependency is enabled	R Rreturns 1s	1

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Table 3-579. Register Call Summary for Register PM_L4PER_GPTIMER10_WKDEP

Clock Management Functional Description • Clock Domain Dependency: [0]
PRCM Register Manual • L4PER_PRM Register Summary: [1]

Table 3-580. RM_L4PER_GPTIMER10_CONTEXT

Address Offset	0x0000 002C		
Physical Address	0x4A30 742C	**Instance**	L4PER_PRM
Description	This register contains dedicated DMTIMER10 context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of L4_PER_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-581. Register Call Summary for Register RM_L4PER_GPTIMER10_CONTEXT

Power Management Functional Description • PD_L4_PER Description: [0]
PRCM Register Manual • L4PER_PRM Register Summary: [1]

Table 3-582. PM_L4PER_GPTIMER11_WKDEP

Address Offset	0x0000 0030		
Physical Address	0x4A30 7430	**Instance**	L4PER_PRM
Description	This register controls wakeup dependency based on DMTIMER11 service requests.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														WKUPDEP_DMTIMER11_MPU_M3	WKUPDEP_DMTIMER11_MPU

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	WKUPDEP_DMTIMER11_MPU_M3	Wakeup dependency from DMTIMER11 module (softwareakeup signal) towards MPU_A3 + L3_2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
0	WKUPDEP_DMTIMER11_MPU	Wakeup dependency from DMTIMER11 module (softwareakeup signal) towards MPU + L3_1 + L3_2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-583. Register Call Summary for Register PM_L4PER_GPTIMER11_WKDEP

Clock Management Functional Description • Clock Domain Dependency: [0] [1]
PRCM Register Manual • L4PER_PRM Register Summary: [2]

Table 3-584. RM_L4PER_GPTIMER11_CONTEXT

Address Offset	0x0000 0034		
Physical Address	0x4A30 7434	**Instance**	L4PER_PRM
Description	This register contains dedicated DMTIMER11 context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															LOSTCONTEXT_DFF

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Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of L4_PER_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-585. Register Call Summary for Register RM_L4PER_GPTIMER11_CONTEXT

Power Management Functional Description • PD_L4_PER Description: [0]
PRCM Register Manual • L4PER_PRM Register Summary: [1]

Table 3-586. PM_L4PER_GPTIMER2_WKDEP

Address Offset	0x0000 0038		
Physical Address	0x4A30 7438	**Instance**	L4PER_PRM
Description	This register controls wakeup dependency based on DMTIMER2 service requests.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															WKUPDEP_DMTIMER2_MPU

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	WKUPDEP_DMTIMER2_MPU	Wakeup dependency from DMTIMER2 module (softwareakeup signal) towards MPU + L3_1 + L3_2 domains Read 0x1: Dependency is enabled	R Rreturns 1s	1

Table 3-587. Register Call Summary for Register PM_L4PER_GPTIMER2_WKDEP

Clock Management Functional Description • Clock Domain Dependency: [0]
PRCM Register Manual • L4PER_PRM Register Summary: [1]

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Table 3-588. RM_L4PER_GPTIMER2_CONTEXT

Address Offset	0x0000 003C		
Physical Address	0x4A30 743C	**Instance**	L4PER_PRM
Description	This register contains dedicated DMTIMER2 context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of L4_PER_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-589. Register Call Summary for Register RM_L4PER_GPTIMER2_CONTEXT

Power Management Functional Description
- PD_L4_PER Description: [0]

PRCM Register Manual
- L4PER_PRM Register Summary: [1]

Table 3-590. PM_L4PER_GPTIMER3_WKDEP

Address Offset	0x0000 0040		
Physical Address	0x4A30 7440	**Instance**	L4PER_PRM
Description	This register controls wakeup dependency based on DMTIMER3 service requests.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														WKUPDEP_DMTIMER3_MPU_M3	WKUPDEP_DMTIMER3_MPU

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Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	WKUPDEP_DMTIMER3_MPU_M3	Wakeup dependency from DMTIMER3 module (softwareakeup signal) towards MPU_A3 + L3_2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
0	WKUPDEP_DMTIMER3_MPU	Wakeup dependency from DMTIMER3 module (softwareakeup signal) towards MPU + L3_1 + L3_2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-591. Register Call Summary for Register PM_L4PER_GPTIMER3_WKDEP

Clock Management Functional Description • Clock Domain Dependency: [0] [1]
PRCM Register Manual • L4PER_PRM Register Summary: [2]

Table 3-592. RM_L4PER_GPTIMER3_CONTEXT

Address Offset	0x0000 0044		
Physical Address	0x4A30 7444	**Instance**	L4PER_PRM
Description	This register contains dedicated DMTIMER3 context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of L4_PER_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-593. Register Call Summary for Register RM_L4PER_GPTIMER3_CONTEXT

Power Management Functional Description • PD_L4_PER Description: [0]
PRCM Register Manual • L4PER_PRM Register Summary: [1]

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Table 3-594. PM_L4PER_GPTIMER4_WKDEP

Address Offset	0x0000 0048		
Physical Address	0x4A30 7448	**Instance**	L4PER_PRM
Description	This register controls wakeup dependency based on DMTIMER4 service requests.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														WKUPDEP_DMTIMER4_MPU_M3	WKUPDEP_DMTIMER4_MPU

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	WKUPDEP_DMTIMER4_MPU_M3	Wakeup dependency from DMTIMER4 module (softwareakeup signal) towards MPU_A3 + L3_2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
0	WKUPDEP_DMTIMER4_MPU	Wakeup dependency from DMTIMER4 module (softwareakeup signal) towards MPU + L3_1 + L3_2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-595. Register Call Summary for Register PM_L4PER_GPTIMER4_WKDEP

Clock Management Functional Description
- Clock Domain Dependency: [0] [1]

PRCM Register Manual
- L4PER_PRM Register Summary: [2]

Table 3-596. RM_L4PER_GPTIMER4_CONTEXT

Address Offset	0x0000 004C		
Physical Address	0x4A30 744C	**Instance**	L4PER_PRM
Description	This register contains dedicated DMTIMER4 context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															LOSTCONTEXT_DFF

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Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of L4_PER_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-597. Register Call Summary for Register RM_L4PER_GPTIMER4_CONTEXT

Power Management Functional Description • PD_L4_PER Description: [0]
PRCM Register Manual • L4PER_PRM Register Summary: [1]

Table 3-598. PM_L4PER_GPTIMER9_WKDEP

Address Offset	0x0000 0050		
Physical Address	0x4A30 7450	**Instance**	L4PER_PRM
Description	This register controls wakeup dependency based on DMTIMER9 service requests.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														WKUPDEP_DMTIMER9_MPU_M3	WKUPDEP_DMTIMER9_MPU

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	WKUPDEP_DMTIMER9_MPU_M3	Wakeup dependency from DMTIMER9 module (softwareakeup signal) towards MPU_A3 + L3_2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
0	WKUPDEP_DMTIMER9_MPU	Wakeup dependency from DMTIMER9 module (softwareakeup signal) towards MPU + L3_1 + L3_2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-599. Register Call Summary for Register PM_L4PER_GPTIMER9_WKDEP

Clock Management Functional Description • Clock Domain Dependency: [0] [1]
PRCM Register Manual • L4PER_PRM Register Summary: [2]

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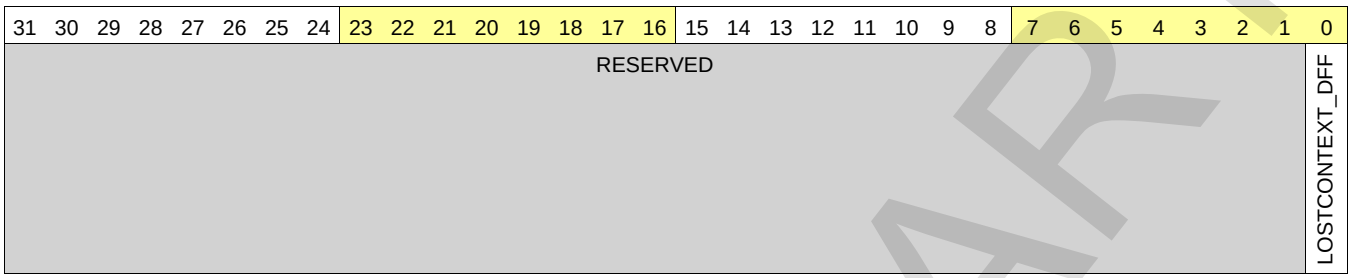
Table 3-600. RM_L4PER_GPTIMER9_CONTEXT

Address Offset	0x0000 0054		
Physical Address	0x4A30 7454	**Instance**	L4PER_PRM
Description	This register contains dedicated DMTIMER9 context statuses. [warm reset insensitive]		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of L4_PER_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

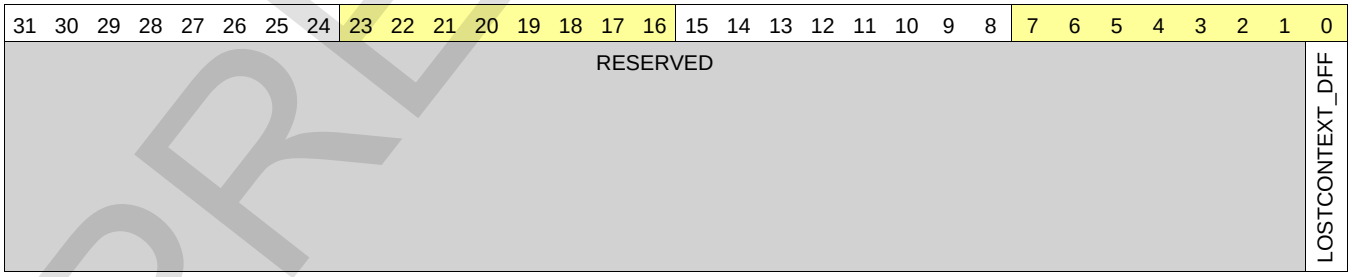
Table 3-601. Register Call Summary for Register RM_L4PER_GPTIMER9_CONTEXT

Power Management Functional Description
- PD_L4_PER Description: [0]

PRCM Register Manual
- L4PER_PRM Register Summary: [1]

Table 3-602. RM_L4PER_ELM_CONTEXT

Address Offset	0x0000 005C		
Physical Address	0x4A30 745C	**Instance**	L4PER_PRM
Description	This register contains dedicated ELM context statuses. [warm reset insensitive]		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of L4_PER_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

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Table 3-603. Register Call Summary for Register RM_L4PER_ELM_CONTEXT

Power Management Functional Description • PD_L4_PER Description: [0]
PRCM Register Manual • L4PER_PRM Register Summary: [1]

Table 3-604. PM_L4PER_GPIO2_WKDEP

Address Offset	0x0000 0060		
Physical Address	0x4A30 7460	**Instance**	L4PER_PRM
Description	This register controls wakeup dependency based on GPIO2 service requests.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																									WKUPDEP_GPIO2_IRQ2_DSP	RESERVED					WKUPDEP_GPIO2_IRQ1_MPU_M3	WKUPDEP_GPIO2_IRQ1_MPU

Bits	Field Name	Description	Type	Reset
31:7	RESERVED		R	0x0000000
6	WKUPDEP_GPIO2_IRQ2_DSP	Wakeup dependency from GPIO2 module (POINTRsoftwareAKEUP2 signal) towards DSP + L3_1 + L3_2 domains Read 0x1: Dependency is enabled	R Rreturns 1s	1
5:2	RESERVED		R	0x0
1	WKUPDEP_GPIO2_IRQ1_MPU_M3	Wakeup dependency from GPIO2 module (POINTRsoftwareAKEUP1 signal) module towards MPU_A3 + L3_2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
0	WKUPDEP_GPIO2_IRQ1_MPU	Wakeup dependency from GPIO2 module (POINTRsoftwareAKEUP1 signal) towards MPU + L3_1 + L3_2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-605. Register Call Summary for Register PM_L4PER_GPIO2_WKDEP

Clock Management Functional Description • Clock Domain Dependency: [0] [1] [2]
PRCM Register Manual • L4PER_PRM Register Summary: [3]

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Table 3-606. RM_L4PER_GPIO2_CONTEXT

Address Offset	0x0000 0064		
Physical Address	0x4A30 7464	**Instance**	L4PER_PRM
Description	This register contains dedicated GPIO2 context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														LOSTCONTEXT_RFF	RESERVED

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	LOSTCONTEXT_RFF	Specify if RFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of L4_PER_RET_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
0	RESERVED		R	0

Table 3-607. Register Call Summary for Register RM_L4PER_GPIO2_CONTEXT

Power Management Functional Description
- PD_L4_PER Description: [0]

PRCM Register Manual
- L4PER_PRM Register Summary: [1]

Table 3-608. PM_L4PER_GPIO3_WKDEP

Address Offset	0x0000 0068		
Physical Address	0x4A30 7468	**Instance**	L4PER_PRM
Description	This register controls wakeup dependency based on GPIO3 service requests.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																									WKUPDEP_GPIO3_IRQ2_DSP	RESERVED					WKUPDEP_GPIO3_IRQ1_MPU

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Bits	Field Name	Description	Type	Reset
31:7	RESERVED		R	0x0000000
6	WKUPDEP_GPIO3_IRQ2_DSP	Wakeup dependency from GPIO3 module (POINTRsoftwareAKEUP2 signal) towards DSP + L3_1 + L3_2 domains Read 0x1: Dependency is enabled	R Rreturns 1s	1
5:1	RESERVED		R	0x00
0	WKUPDEP_GPIO3_IRQ1_MPU	Wakeup dependency from GPIO3 module (POINTRsoftwareAKEUP1 signal) towards MPU + L3_1 + L3_2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-609. Register Call Summary for Register PM_L4PER_GPIO3_WKDEP

Clock Management Functional Description • Clock Domain Dependency: [0] [1]
PRCM Register Manual • L4PER_PRM Register Summary: [2]

Table 3-610. RM_L4PER_GPIO3_CONTEXT

Address Offset	0x0000 006C		
Physical Address	0x4A30 746C	**Instance**	L4PER_PRM
Description	This register contains dedicated GPIO3 context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														LOSTCONTEXT_RFF	RESERVED

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	LOSTCONTEXT_RFF	Specify if RFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of L4_PER_RET_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
0	RESERVED		R	0

Table 3-611. Register Call Summary for Register RM_L4PER_GPIO3_CONTEXT

Power Management Functional Description • PD_L4_PER Description: [0]
PRCM Register Manual • L4PER_PRM Register Summary: [1]

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Table 3-612. PM_L4PER_GPIO4_WKDEP

Address Offset	0x0000 0070		
Physical Address	0x4A30 7470	**Instance**	L4PER_PRM
Description	This register controls wakeup dependency based on GPIO4 service requests.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								WKUPDEP_GPIO4_IRQ2_DSP	RESERVED						WKUPDEP_GPIO4_IRQ1_MPU

Bits	Field Name	Description	Type	Reset
31:7	RESERVED		R	0x0000000
6	WKUPDEP_GPIO4_IRQ2_DSP	Wakeup dependency from GPIO4 module (POINTRsoftwareAKEUP2 signal) towards DSP + L3_1 + L3_2 domains Read 0x1: Dependency is enabled	R Rreturns 1s	1
5:1	RESERVED		R	0x00
0	WKUPDEP_GPIO4_IRQ1_MPU	Wakeup dependency from GPIO4 module (POINTRsoftwareAKEUP1 signal) towards MPU + L3_1 + L3_2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-613. Register Call Summary for Register PM_L4PER_GPIO4_WKDEP

Clock Management Functional Description • Clock Domain Dependency: [0] [1]
PRCM Register Manual • L4PER_PRM Register Summary: [2]

Table 3-614. RM_L4PER_GPIO4_CONTEXT

Address Offset	0x0000 0074		
Physical Address	0x4A30 7474	**Instance**	L4PER_PRM
Description	This register contains dedicated GPIO4 context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														LOSTCONTEXT_RFF	RESERVED

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Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	LOSTCONTEXT_RFF	Specify if RFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of L4_PER_RET_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
0	RESERVED		R	0

Table 3-615. Register Call Summary for Register RM_L4PER_GPIO4_CONTEXT

Power Management Functional Description • PD_L4_PER Description: [0]
PRCM Register Manual • L4PER_PRM Register Summary: [1]

Table 3-616. PM_L4PER_GPIO5_WKDEP

Address Offset	0x0000 0078		
Physical Address	0x4A30 7478	**Instance**	L4PER_PRM
Description	This register controls wakeup dependency based on GPIO5 service requests.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								WKUPDEP_GPIO5_IRQ2_DSP	RESERVED						WKUPDEP_GPIO5_IRQ1_MPU

Bits	Field Name	Description	Type	Reset
31:7	RESERVED		R	0x0000000
6	WKUPDEP_GPIO5_IRQ2_DSP	Wakeup dependency from GPIO5 module (POINTRsoftwareAKEUP2 signal) towards DSP + L3_1 + L3_2 domains Read 0x1: Dependency is enabled	R Rreturns 1s	1
5:1	RESERVED		R	0x00
0	WKUPDEP_GPIO5_IRQ1_MPU	Wakeup dependency from GPIO5 module (POINTRsoftwareAKEUP1 signal) towards MPU + L3_1 + L3_2 domains Read 0x1: Dependency is enabled	R Rreturns 1s	1

Table 3-617. Register Call Summary for Register PM_L4PER_GPIO5_WKDEP

Clock Management Functional Description • Clock Domain Dependency: [0] [1]
PRCM Register Manual • L4PER_PRM Register Summary: [2]

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Table 3-618. RM_L4PER_GPIO5_CONTEXT

Address Offset	0x0000 007C		
Physical Address	0x4A30 747C	**Instance**	L4PER_PRM
Description	This register contains dedicated GPIO5 context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														LOSTCONTEXT_RFF	RESERVED

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	LOSTCONTEXT_RFF	Specify if RFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of L4_PER_RET_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
0	RESERVED		R	0

Table 3-619. Register Call Summary for Register RM_L4PER_GPIO5_CONTEXT

Power Management Functional Description
- PD_L4_PER Description: [0]

PRCM Register Manual
- L4PER_PRM Register Summary: [1]

Table 3-620. PM_L4PER_GPIO6_WKDEP

Address Offset	0x0000 0080		
Physical Address	0x4A30 7480	**Instance**	L4PER_PRM
Description	This register controls wakeup dependency based on GPIO6 service requests.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																									WKUPDEP_GPIO6_IRQ2_DSP	RESERVED					WKUPDEP_GPIO6_IRQ1_MPU

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Bits	Field Name	Description	Type	Reset
31:7	RESERVED		R	0x0000000
6	WKUPDEP_GPIO6_IRQ2_DSP	Wakeup dependency from GPIO6 module (POINTRsoftwareAKEUP2 signal) towards DSP + L3_1 + L3_2 domains Read 0x1: Dependency is enabled	R Rreturns 1s	1
5:1	RESERVED		R	0x00
0	WKUPDEP_GPIO6_IRQ1_MPU	Wakeup dependency from GPIO6 module (POINTRsoftwareAKEUP1 signal) towards MPU + L3_1 + L3_2 domains Read 0x1: Dependency is enabled	R Rreturns 1s	1

Table 3-621. Register Call Summary for Register PM_L4PER_GPIO6_WKDEP

Clock Management Functional Description • Clock Domain Dependency: [0] [1]
PRCM Register Manual • L4PER_PRM Register Summary: [2]

Table 3-622. RM_L4PER_GPIO6_CONTEXT

Address Offset	0x0000 0084		
Physical Address	0x4A30 7484	**Instance**	L4PER_PRM
Description	This register contains dedicated GPIO6 context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														LOSTCONTEXT_RFF	RESERVED

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	LOSTCONTEXT_RFF	Specify if RFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of L4_PER_RET_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
0	RESERVED		R	0

Table 3-623. Register Call Summary for Register RM_L4PER_GPIO6_CONTEXT

Power Management Functional Description • PD_L4_PER Description: [0]
PRCM Register Manual • L4PER_PRM Register Summary: [1]

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Table 3-624. RM_L4PER_HDQ1W_CONTEXT

Address Offset	0x0000 008C		
Physical Address	0x4A30 748C	**Instance**	L4PER_PRM
Description	This register contains dedicated HDQ1W context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of L4_PER_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-625. Register Call Summary for Register RM_L4PER_HDQ1W_CONTEXT

Power Management Functional Description • PD_L4_PER Description: [0]
PRCM Register Manual • L4PER_PRM Register Summary: [1]

Table 3-626. PM_L4PER_I2C1_WKDEP

Address Offset	0x0000 00A0		
Physical Address	0x4A30 74A0	**Instance**	L4PER_PRM
Description	This register controls wakeup dependency based on I2C1 service requests.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								WKUPDEP_I2C1_DMA_SDMA	RESERVED					WKUPDEP_I2C1_IRQ_MPU_M3	WKUPDEP_I2C1_IRQ_MPU

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Bits	Field Name	Description	Type	Reset
31:8	RESERVED		R	0x000000
7	WKUPDEP_I2C1_DMA_SDMA	Wakeup dependency from I2C1 module (softwareakeup_dma signal) towards SDMA + L3_2 domains Read 0x1: Dependency is enabled	R Rreturns 1s	1
6:2	RESERVED		R	0x00
1	WKUPDEP_I2C1_IRQ_MPU_M3	Wakeup dependency from I2C1 module (softwareakeup_irq signal) towards MPU_A3 + L3_2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
0	WKUPDEP_I2C1_IRQ_MPU	Wakeup dependency from I2C1 module (softwareakeup_irq signal) towards MPU + L3_1 + L3_2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-627. Register Call Summary for Register PM_L4PER_I2C1_WKDEP

Clock Management Functional Description • Clock Domain Dependency: [0] [1] [2]
PRCM Register Manual • L4PER_PRM Register Summary: [3]

Table 3-628. RM_L4PER_I2C1_CONTEXT

Address Offset	0x0000 00A4		
Physical Address	0x4A30 74A4	**Instance**	L4PER_PRM
Description	This register contains dedicated I2C1 context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														LOSTCONTEXT_RFF	RESERVED

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	LOSTCONTEXT_RFF	Specify if RFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of L4_PER_RET_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
0	RESERVED		R	0

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Table 3-629. Register Call Summary for Register RM_L4PER_I2C1_CONTEXT

Power Management Functional Description • PD_L4_PER Description: [0]
PRCM Register Manual • L4PER_PRM Register Summary: [1]

Table 3-630. PM_L4PER_I2C2_WKDEP

Address Offset	0x0000 00A8		
Physical Address	0x4A30 74A8	**Instance**	L4PER_PRM
Description	This register controls wakeup dependency based on I2C2 service requests.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								WKUPDEP_I2C2_DMA_SDMA	RESERVED					WKUPDEP_I2C2_IRQ_MPU_M3	WKUPDEP_I2C2_IRQ_MPU

Bits	Field Name	Description	Type	Reset
31:8	RESERVED		R	0x000000
7	WKUPDEP_I2C2_DMA_SDMA	Wakeup dependency from I2C2 module (softwareakeup_dma signal) towards SDMA + L3_2 domains Read 0x1: Dependency is enabled	R Rreturns 1s	1
6:2	RESERVED		R	0x00
1	WKUPDEP_I2C2_IRQ_MPU_M3	Wakeup dependency from I2C2 module (softwareakeup_irq signal) towards MPU_A3 + L3_2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
0	WKUPDEP_I2C2_IRQ_MPU	Wakeup dependency from I2C2 module (softwareakeup_irq signal) towards MPU + L3_1 + L3_2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-631. Register Call Summary for Register PM_L4PER_I2C2_WKDEP

Clock Management Functional Description • Clock Domain Dependency: [0] [1] [2]
PRCM Register Manual • L4PER_PRM Register Summary: [3]

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Table 3-632. RM_L4PER_I2C2_CONTEXT

Address Offset	0x0000 00AC		
Physical Address	0x4A30 74AC	**Instance**	L4PER_PRM
Description	This register contains dedicated I2C2 context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of L4_PER_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-633. Register Call Summary for Register RM_L4PER_I2C2_CONTEXT

Power Management Functional Description
- PD_L4_PER Description: [0]

PRCM Register Manual
- L4PER_PRM Register Summary: [1]

Table 3-634. PM_L4PER_I2C3_WKDEP

Address Offset	0x0000 00B0		
Physical Address	0x4A30 74B0	**Instance**	L4PER_PRM
Description	This register controls wakeup dependency based on I2C3 service requests.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								WKUPDEP_I2C3_DMA_SDMA	RESERVED					WKUPDEP_I2C3_IRQ_MPU_M3	WKUPDEP_I2C3_IRQ_MPU

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Bits	Field Name	Description	Type	Reset
31:8	RESERVED		R	0x000000
7	WKUPDEP_I2C3_DMA_SDMA	Wakeup dependency from I2C3 module (softwareakeup_dma signal) towards SDMA + L3_2 domains Read 0x1: Dependency is enabled	R Rreturns 1s	1
6:2	RESERVED		R	0x00
1	WKUPDEP_I2C3_IRQ_MPU_M3	Wakeup dependency from I2C3 module (softwareakeup_irq signal) towards MPU_A3 + L3_2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
0	WKUPDEP_I2C3_IRQ_MPU	Wakeup dependency from I2C3 module (softwareakeup_irq signal) towards MPU + L3_1 + L3_2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-635. Register Call Summary for Register PM_L4PER_I2C3_WKDEP

Clock Management Functional Description • Clock Domain Dependency: [0] [1] [2]
PRCM Register Manual • L4PER_PRM Register Summary: [3]

Table 3-636. RM_L4PER_I2C3_CONTEXT

Address Offset	0x0000 00B4		
Physical Address	0x4A30 74B4	**Instance**	L4PER_PRM
Description	This register contains dedicated I2C3 context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of L4_PER_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-637. Register Call Summary for Register RM_L4PER_I2C3_CONTEXT

Power Management Functional Description • PD_L4_PER Description: [0]
PRCM Register Manual • L4PER_PRM Register Summary: [1]

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Table 3-638. PM_L4PER_I2C4_WKDEP

Address Offset	0x0000 00B8		
Physical Address	0x4A30 74B8	**Instance**	L4PER_PRM
Description	This register controls wakeup dependency based on I2C4 service requests.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								WKUPDEP_I2C4_DMA_SDMA	RESERVED					WKUPDEP_I2C4_IRQ_MPU_M3	WKUPDEP_I2C4_IRQ_MPU

Bits	Field Name	Description	Type	Reset
31:8	RESERVED		R	0x000000
7	WKUPDEP_I2C4_DMA_SDMA	Wakeup dependency from I2C4 module (softwareakeup_dma signal) towards SDMA + L3_2 domains Read 0x1: Dependency is enabled	R Rreturns 1s	1
6:2	RESERVED		R	0x00
1	WKUPDEP_I2C4_IRQ_MPU_M3	Wakeup dependency from I2C4 module (softwareakeup_irq signal) towards MPU_A3 + L3_2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
0	WKUPDEP_I2C4_IRQ_MPU	Wakeup dependency from I2C4 module (softwareakeup_irq signal) towards MPU + L3_1 + L3_2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-639. Register Call Summary for Register PM_L4PER_I2C4_WKDEP

Clock Management Functional Description
- Clock Domain Dependency: [0] [1] [2]

PRCM Register Manual
- L4PER_PRM Register Summary: [3]

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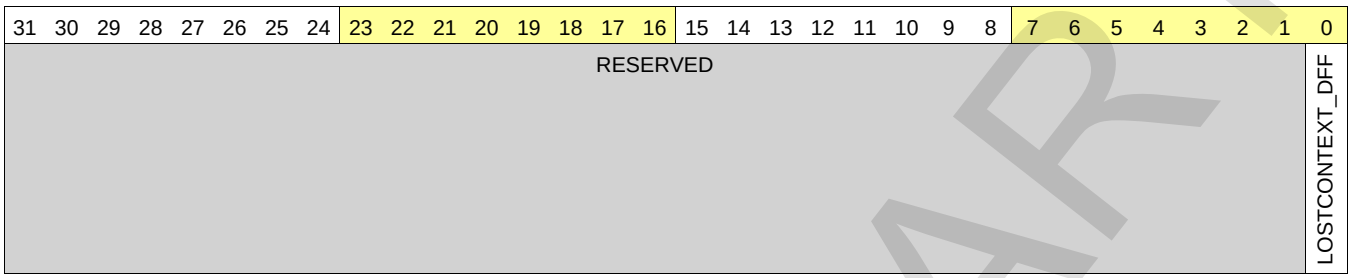
Table 3-640. RM_L4PER_I2C4_CONTEXT

Address Offset	0x0000 00BC		
Physical Address	0x4A30 74BC	**Instance**	L4PER_PRM
Description	This register contains dedicated I2C4 context statuses. [warm reset insensitive]		
Type	RW		



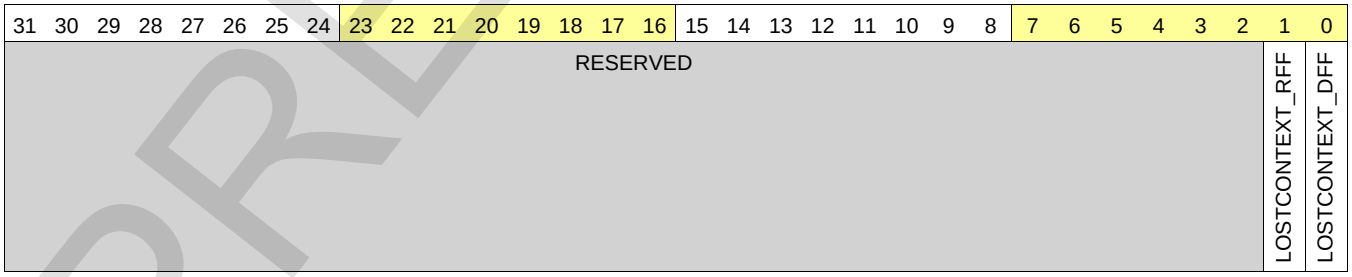
Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of L4_PER_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-641. Register Call Summary for Register RM_L4PER_I2C4_CONTEXT

Power Management Functional Description • PD_L4_PER Description: [0]
PRCM Register Manual • L4PER_PRM Register Summary: [1]

Table 3-642. RM_L4PER_L4_PER_CONTEXT

Address Offset	0x0000 00C0		
Physical Address	0x4A30 74C0	**Instance**	L4PER_PRM
Description	This register contains dedicated L4_PER context statuses. [warm reset insensitive]		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	LOSTCONTEXT_RFF	Specify if RFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of L4_PER_PWRON_RET_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

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Bits	Field Name	Description	Type	Reset
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of L4_PER_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-643. Register Call Summary for Register RM_L4PER_L4_PER_CONTEXT

Power Management Functional Description • PD_L4_PER Description: [0] [1]
PRCM Register Manual • L4PER_PRM Register Summary: [2]

Table 3-644. PM_L4PER_MCBSP4_WKDEP

Address Offset	0x0000 00E0		
Physical Address	0x4A30 74E0	**Instance**	L4PER_PRM
Description	This register controls wakeup dependency based on MCBSP4 service requests.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												WKUPDEP_MCBSP4_SDMA	WKUPDEP_MCBSP4_DSP	RESERVED	WKUPDEP_MCBSP4_MPU

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0000000
3	WKUPDEP_MCBSP4_SDMA	Wakeup dependency from MCBSP4 module (softwareakeup signal) towards SDMA + L3_2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
2	WKUPDEP_MCBSP4_DSP	Wakeup dependency from MCBSP4 module (softwareakeup signal) towards DSP + L3_1 + L3_2 domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
1	RESERVED		R	0
0	WKUPDEP_MCBSP4_MPU	Wakeup dependency from MCBSP4 module (softwareakeup signal) towards MPU + L3_1 + L3_2 domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

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Table 3-645. Register Call Summary for Register PM_L4PER_MCBSP4_WKDEP

Clock Management Functional Description • Clock Domain Dependency: [0] [1] [2]
PRCM Register Manual • L4PER_PRM Register Summary: [3]

Table 3-646. RM_L4PER_MCBSP4_CONTEXT

Address Offset	0x0000 00E4		
Physical Address	0x4A30 74E4	**Instance**	L4PER_PRM
Description	This register contains dedicated MCBSP4 context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							LOSTMEM_NONRETAINED_BANK	RESERVED							LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	LOSTMEM_NONRETAINED_BANK	Specify if memory-based context in NONRETAINED_BANK memory bank has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
7:1	RESERVED		R	0x00
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of L4_PER_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-647. Register Call Summary for Register RM_L4PER_MCBSP4_CONTEXT

Power Management Functional Description • PD_L4_PER Description: [0]
PRCM Register Manual • L4PER_PRM Register Summary: [1]

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Table 3-648. PM_L4PER_MCSPI1_WKDEP

Address Offset	0x0000 00F0		
Physical Address	0x4A30 74F0	**Instance**	L4PER_PRM
Description	This register controls wakeup dependency based on MCSPI1 service requests.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												WKUPDEP_MCSPI1_SDMA	WKUPDEP_MCSPI1_DSP	WKUPDEP_MCSPI1_MPU_M3	WKUPDEP_MCSPI1_MPU

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0000000
3	WKUPDEP_MCSPI1_SDMA	Wakeup dependency from MCSPI1 module (softwareakeup signal) towards SDMA + L3_2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
2	WKUPDEP_MCSPI1_DSP	Wakeup dependency from MCSPI1 module (softwareakeup signal) towards DSP + L3_1 + L3_2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
1	WKUPDEP_MCSPI1_MPU_M3	Wakeup dependency from MCSPI1 module (softwareakeup signal) towards MPU_A3 + L3_2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
0	WKUPDEP_MCSPI1_MPU	Wakeup dependency from MCSPI1 module (softwareakeup signal) towards MPU + L3_1 + L3_2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-649. Register Call Summary for Register PM_L4PER_MCSPI1_WKDEP

Clock Management Functional Description • Clock Domain Dependency: [0] [1] [2] [3]
PRCM Register Manual • L4PER_PRM Register Summary: [4]

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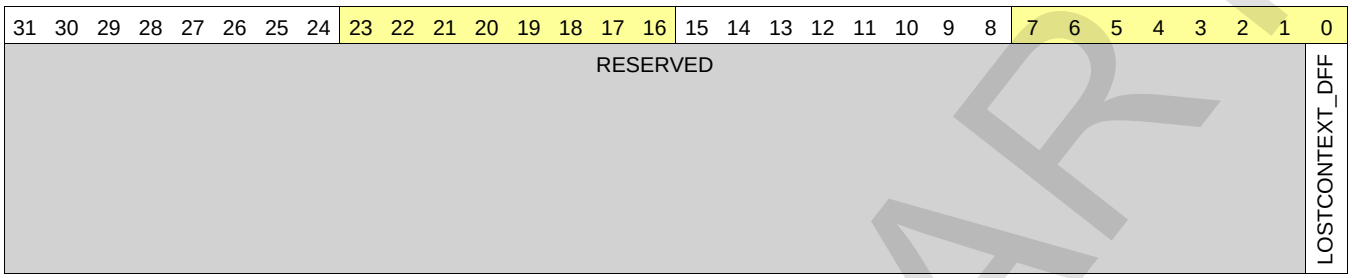
Table 3-650. RM_L4PER_MCSPI1_CONTEXT

Address Offset	0x0000 00F4		
Physical Address	0x4A30 74F4	**Instance**	L4PER_PRM
Description	This register contains dedicated MCSPI1 context statuses. [warm reset insensitive]		
Type	RW		



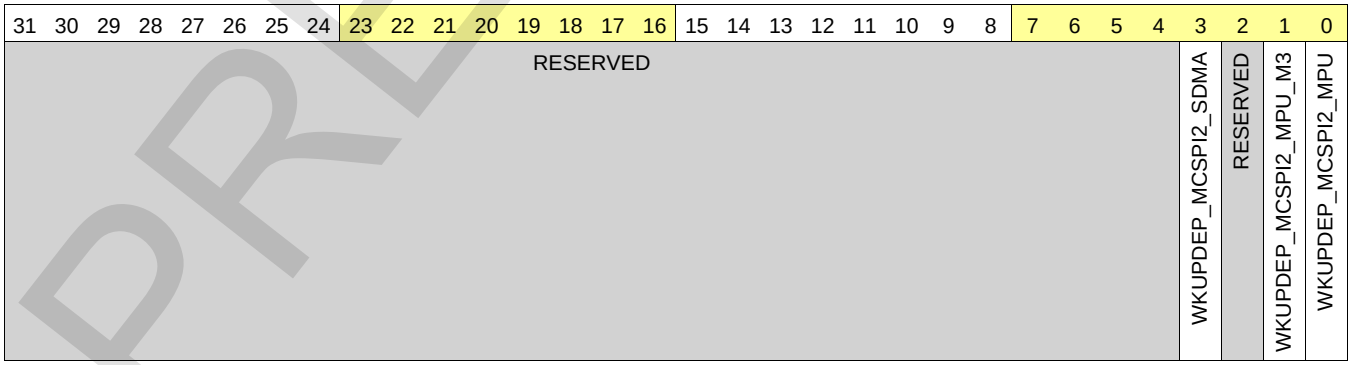
Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of L4_PER_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-651. Register Call Summary for Register RM_L4PER_MCSPI1_CONTEXT

Power Management Functional Description • PD_L4_PER Description: [0]
PRCM Register Manual • L4PER_PRM Register Summary: [1]

Table 3-652. PM_L4PER_MCSPI2_WKDEP

Address Offset	0x0000 00F8		
Physical Address	0x4A30 74F8	**Instance**	L4PER_PRM
Description	This register controls wakeup dependency based on MCSPI2 service requests.		
Type	RW		



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Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0000000
3	WKUPDEP_MCSPI2_SDMA	Wakeup dependency from MCSPI2 module (softwareakeup signal) towards SDMA + L3_2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
2	RESERVED		R	0
1	WKUPDEP_MCSPI2_MPU_M3	Wakeup dependency from MCSPI2 module (softwareakeup signal) towards MPU_A3 + L3_2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
0	WKUPDEP_MCSPI2_MPU	Wakeup dependency from MCSPI2 module (softwareakeup signal) towards MPU + L3_1 + L3_2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-653. Register Call Summary for Register PM_L4PER_MCSPI2_WKDEP

Clock Management Functional Description • Clock Domain Dependency: [0] [1] [2]
PRCM Register Manual • L4PER_PRM Register Summary: [3]

Table 3-654. RM_L4PER_MCSPI2_CONTEXT

Address Offset	0x0000 00FC		
Physical Address	0x4A30 74FC	**Instance**	L4PER_PRM
Description	This register contains dedicated MCSPI2 context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of L4_PER_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-655. Register Call Summary for Register RM_L4PER_MCSPI2_CONTEXT

Power Management Functional Description • PD_L4_PER Description: [0]
PRCM Register Manual • L4PER_PRM Register Summary: [1]

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Table 3-656. PM_L4PER_MCSPI3_WKDEP

Address Offset	0x0000 0100		
Physical Address	0x4A30 7500	**Instance**	L4PER_PRM
Description	This register controls wakeup dependency based on MCSPI3 service requests.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												WKUPDEP_MCSPI3_SDMA	RESERVED		WKUPDEP_MCSPI3_MPU

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0000000
3	WKUPDEP_MCSPI3_SDMA	Wakeup dependency from MCSPI3 module (softwareakeup signal) towards SDMA + L3_2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
2:1	RESERVED		R	0x0
0	WKUPDEP_MCSPI3_MPU	Wakeup dependency from MCSPI3 module (softwareakeup signal) towards MPU + L3_1 + L3_2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-657. Register Call Summary for Register PM_L4PER_MCSPI3_WKDEP

Clock Management Functional Description • Clock Domain Dependency: [0] [1]
PRCM Register Manual • L4PER_PRM Register Summary: [2]

Table 3-658. RM_L4PER_MCSPI3_CONTEXT

Address Offset	0x0000 0104		
Physical Address	0x4A30 7504	**Instance**	L4PER_PRM
Description	This register contains dedicated MCSPI3 context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															LOSTCONTEXT_DFF

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Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of L4_PER_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-659. Register Call Summary for Register RM_L4PER_MCSPI3_CONTEXT

Power Management Functional Description • PD_L4_PER Description: [0]
PRCM Register Manual • L4PER_PRM Register Summary: [1]

Table 3-660. PM_L4PER_MCSPI4_WKDEP

Address Offset	0x0000 0108		
Physical Address	0x4A30 7508	**Instance**	L4PER_PRM
Description	This register controls wakeup dependency based on MCSPI4 service requests.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												WKUPDEP_MCSPI4_SDMA	RESERVED		WKUPDEP_MCSPI4_MPU

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0000000
3	WKUPDEP_MCSPI4_SDMA	Wakeup dependency from MCSPI4 module (softwareakeup signal) towards SDMA + L3_2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
2:1	RESERVED		R	0x0
0	WKUPDEP_MCSPI4_MPU	Wakeup dependency from MCSPI4 module (softwareakeup signal) towards MPU + L3_1 + L3_2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-661. Register Call Summary for Register PM_L4PER_MCSPI4_WKDEP

Clock Management Functional Description • Clock Domain Dependency: [0] [1]
PRCM Register Manual • L4PER_PRM Register Summary: [2]

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Table 3-662. RM_L4PER_MCSPI4_CONTEXT

Address Offset	0x0000 010C		
Physical Address	0x4A30 750C	**Instance**	L4PER_PRM
Description	This register contains dedicated MCSPI4 context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of L4_PER_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-663. Register Call Summary for Register RM_L4PER_MCSPI4_CONTEXT

Power Management Functional Description • PD_L4_PER Description: [0]
PRCM Register Manual • L4PER_PRM Register Summary: [1]

Table 3-664. PM_L4PER_MMCSD3_WKDEP

Address Offset	0x0000 0120		
Physical Address	0x4A30 7520	**Instance**	L4PER_PRM
Description	This register controls wakeup dependency based on MMCSD3 service requests.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												WKUPDEP_MMCSD3_SDMA	RESERVED	WKUPDEP_MMCSD3_MPU_M3	WKUPDEP_MMCSD3_MPU

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Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0000000
3	WKUPDEP_MMCSD3_SDMA	Wakeup dependency from MMCSD3 module (softwareakeup signal) towards SDMA + L3_2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
2	RESERVED		R	0
1	WKUPDEP_MMCSD3_MPU_M3	Wakeup dependency from MMCSD3 module (softwareakeup signal) towards MPU_A3 + L3_2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
0	WKUPDEP_MMCSD3_MPU	Wakeup dependency from MMCSD3 module (softwareakeup signal) towards MPU + L3_1 + L3_2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-665. Register Call Summary for Register PM_L4PER_MMCSD3_WKDEP

Clock Management Functional Description • Clock Domain Dependency: [0] [1] [2]
PRCM Register Manual • L4PER_PRM Register Summary: [3]

Table 3-666. RM_L4PER_MMCSD3_CONTEXT

Address Offset	0x0000 0124		
Physical Address	0x4A30 7524	**Instance**	L4PER_PRM
Description	This register contains dedicated MMCSD3 context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							LOSTMEM_NONRETAINED_BANK	RESERVED							LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	LOSTMEM_NONRETAINED_BANK	Specify if memory-based context in NONRETAINED_BANK memory bank has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
7:1	RESERVED		R	0x00

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Bits	Field Name	Description	Type	Reset
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of L4_PER_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-667. Register Call Summary for Register RM_L4PER_MMCSD3_CONTEXT

Power Management Functional Description • PD_L4_PER Description: [0]
PRCM Register Manual • L4PER_PRM Register Summary: [1]

Table 3-668. PM_L4PER_MMCSD4_WKDEP

Address Offset	0x0000 0128		
Physical Address	0x4A30 7528	**Instance**	L4PER_PRM
Description	This register controls wakeup dependency based on MMCSD4 service requests.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												WKUPDEP_MMCSD4_SDMA	RESERVED	WKUPDEP_MMCSD4_MPU_M3	WKUPDEP_MMCSD4_MPU

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0000000
3	WKUPDEP_MMCSD4_SDMA	Wakeup dependency from MMCSD4 module (softwareakeup signal) towards SDMA + L3_2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
2	RESERVED		R	0
1	WKUPDEP_MMCSD4_MPU_M3	Wakeup dependency from MMCSD4 module (softwareakeup signal) towards MPU_A3 + L3_2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
0	WKUPDEP_MMCSD4_MPU	Wakeup dependency from MMCSD4 module (softwareakeup signal) towards MPU + L3_1 + L3_2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

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Table 3-669. Register Call Summary for Register PM_L4PER_MMCSD4_WKDEP

Clock Management Functional Description • Clock Domain Dependency: [0] [1] [2]
PRCM Register Manual • L4PER_PRM Register Summary: [3]

Table 3-670. RM_L4PER_MMCSD4_CONTEXT

Address Offset	0x0000 012C		
Physical Address	0x4A30 752C	**Instance**	L4PER_PRM
Description	This register contains dedicated MMCSD4 context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							LOSTMEM_NONRETAINED_BANK	RESERVED							LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	LOSTMEM_NONRETAINED_BANK	Specify if memory-based context in NONRETAINED_BANK memory bank has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
7:1	RESERVED		R	0x00
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of L4_PER_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-671. Register Call Summary for Register RM_L4PER_MMCSD4_CONTEXT

Power Management Functional Description • PD_L4_PER Description: [0]
PRCM Register Manual • L4PER_PRM Register Summary: [1]

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Table 3-672. PM_L4PER_SLIMBUS2_WKDEP

Address Offset	0x0000 0138		
Physical Address	0x4A30 7538	**Instance**	L4PER_PRM
Description	This register controls wakeup dependency based on SLIMBUS2 service requests.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								WKUPDEP_SLIMBUS2_DMA_SDMA	WKUPDEP_SLIMBUS2_DMA_DSP	RESERVED			WKUPDEP_SLIMBUS2_IRQ_DSP	RESERVED	WKUPDEP_SLIMBUS2_IRQ_MPU

Bits	Field Name	Description	Type	Reset
31:8	RESERVED		R	0x000000
7	WKUPDEP_SLIMBUS2_DMA_SDMA	Wakeup dependency from SLIMBUS2 module (softwareakeup_dma signal) towards SDMA + L3_2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
6	WKUPDEP_SLIMBUS2_DMA_DSP	Wakeup dependency from SLIMBUS2 module (softwareakeup_dma signal) towards DSP + L3_1 + L3_2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
5:3	RESERVED		R	0x0
2	WKUPDEP_SLIMBUS2_IRQ_DSP	Wakeup dependency from SLIMBUS2 module (softwareakeup_irq signal) towards DSP + L3_1 + L3_2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
1	RESERVED		R	0
0	WKUPDEP_SLIMBUS2_IRQ_MPU	Wakeup dependency from SLIMBUS2 module (softwareakeup_irq signal) towards MPU + L3_1 + L3_2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-673. Register Call Summary for Register PM_L4PER_SLIMBUS2_WKDEP

Clock Management Functional Description
- Clock Domain Dependency: [0] [1] [2] [3]

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- L4PER_PRM Register Summary: [4]

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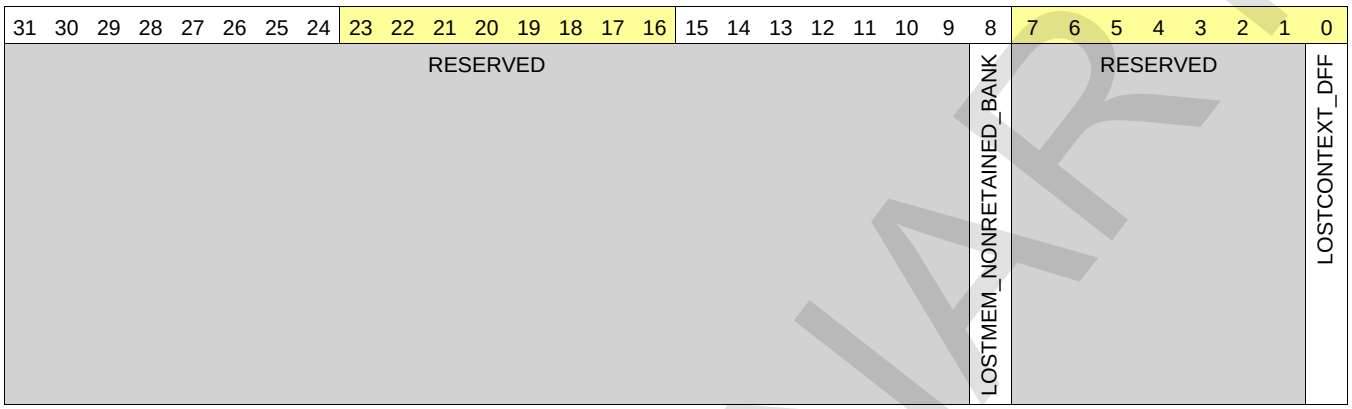
Table 3-674. RM_L4PER_SLIMBUS2_CONTEXT

Address Offset	0x0000 013C		
Physical Address	0x4A30 753C	**Instance**	L4PER_PRM
Description	This register contains dedicated SLIMBUS2 context statuses. [warm reset insensitive]		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	LOSTMEM_NONRETAINED_BANK	Specify if memory-based context in NONRETAINED_BANK memory bank has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
7:1	RESERVED		R	0x00
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of L4_PER_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-675. Register Call Summary for Register RM_L4PER_SLIMBUS2_CONTEXT

Power Management Functional Description • PD_L4_PER Description: [0]
PRCM Register Manual • L4PER_PRM Register Summary: [1]

Table 3-676. PM_L4PER_UART1_WKDEP

Address Offset	0x0000 0140		
Physical Address	0x4A30 7540	**Instance**	L4PER_PRM
Description	This register controls wakeup dependency based on UART1 service requests.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												WKUPDEP_UART1_SDMA	RESERVED		WKUPDEP_UART1_MPU

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0000000
3	WKUPDEP_UART1_SDMA	Wakeup dependency from UART1 module (softwareakeup signal) towards SDMA + L3_2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
2:1	RESERVED		R	0x0
0	WKUPDEP_UART1_MPU	Wakeup dependency from UART1 module (softwareakeup signal) towards MPU + L3_1 + L3_2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-677. Register Call Summary for Register PM_L4PER_UART1_WKDEP

Clock Management Functional Description • Clock Domain Dependency: [0] [1]
PRCM Register Manual • L4PER_PRM Register Summary: [2]

Table 3-678. RM_L4PER_UART1_CONTEXT

Address Offset	0x0000 0144		
Physical Address	0x4A30 7544	**Instance**	L4PER_PRM
Description	This register contains dedicated UART1 context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								LOSTMEM_RETAINED_BANK	RESERVED						LOSTCONTEXT_RFF	RESERVED

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Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	LOSTMEM_RETAINED_BANK	Specify if memory-based context in RETAINED_BANK memory bank has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
7:2	RESERVED		R	0x00
1	LOSTCONTEXT_RFF	Specify if RFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of L4_PER_RET_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
0	RESERVED		R	0

Table 3-679. Register Call Summary for Register RM_L4PER_UART1_CONTEXT

Power Management Functional Description • PD_L4_PER Description: [0]
PRCM Register Manual • L4PER_PRM Register Summary: [1]

Table 3-680. PM_L4PER_UART2_WKDEP

Address Offset	0x0000 0148		
Physical Address	0x4A30 7548	**Instance**	L4PER_PRM
Description	This register controls wakeup dependency based on UART2 service requests.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												WKUPDEP_UART2_SDMA	RESERVED		WKUPDEP_UART2_MPU

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0000000
3	WKUPDEP_UART2_SDMA	Wakeup dependency from UART2 module (softwareakeup signal) towards SDMA + L3_2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
2:1	RESERVED		R	0x0
0	WKUPDEP_UART2_MPU	Wakeup dependency from UART2 module (softwareakeup signal) towards MPU + L3_1 + L3_2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

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Table 3-681. Register Call Summary for Register PM_L4PER_UART2_WKDEP

Clock Management Functional Description • Clock Domain Dependency: [0] [1]
PRCM Register Manual • L4PER_PRM Register Summary: [2]

Table 3-682. RM_L4PER_UART2_CONTEXT

Address Offset	0x0000 014C		
Physical Address	0x4A30 754C	**Instance**	L4PER_PRM
Description	This register contains dedicated UART2 context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							LOSTMEM_RETAINED_BANK	RESERVED						LOSTCONTEXT_RFF	RESERVED

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	LOSTMEM_RETAINED_BANK	Specify if memory-based context in RETAINED_BANK memory bank has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
7:2	RESERVED		R	0x00
1	LOSTCONTEXT_RFF	Specify if RFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of L4_PER_RET_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
0	RESERVED		R	0

Table 3-683. Register Call Summary for Register RM_L4PER_UART2_CONTEXT

Power Management Functional Description • PD_L4_PER Description: [0]
PRCM Register Manual • L4PER_PRM Register Summary: [1]

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Table 3-684. PM_L4PER_UART3_WKDEP

Address Offset	0x0000 0150		
Physical Address	0x4A30 7550	**Instance**	L4PER_PRM
Description	This register controls wakeup dependency based on UART3 service requests.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												WKUPDEP_UART3_SDMA	WKUPDEP_UART3_DSP	WKUPDEP_UART3_MPU_M3	WKUPDEP_UART3_MPU

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0000000
3	WKUPDEP_UART3_SDMA	Wakeup dependency from UART3 module (softwareakeup signal) towards SDMA + L3_2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
2	WKUPDEP_UART3_DSP	Wakeup dependency from UART3 module (softwareakeup signal) towards DSP + L3_1 + L3_2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
1	WKUPDEP_UART3_MPU_M3	Wakeup dependency from UART3 module (softwareakeup signal) towards MPU_A3 + L3_2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
0	WKUPDEP_UART3_MPU	Wakeup dependency from UART3 module (softwareakeup signal) towards MPU + L3_1 + L3_2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-685. Register Call Summary for Register PM_L4PER_UART3_WKDEP

Clock Management Functional Description
- Clock Domain Dependency: [0] [1] [2] [3]

PRCM Register Manual
- L4PER_PRM Register Summary: [4]

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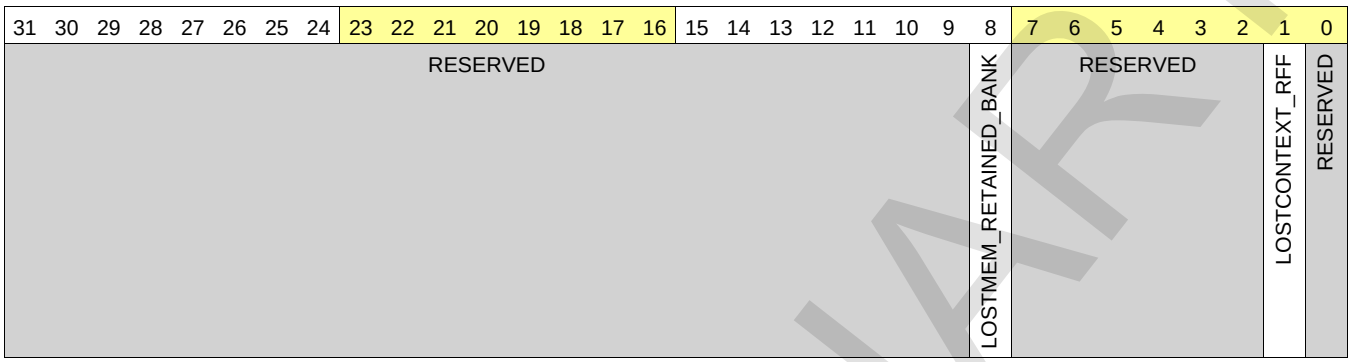
Table 3-686. RM_L4PER_UART3_CONTEXT

Address Offset	0x0000 0154		
Physical Address	0x4A30 7554	**Instance**	L4PER_PRM
Description	This register contains dedicated UART3 context statuses. [warm reset insensitive]		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	LOSTMEM_RETAINED_BANK	Specify if memory-based context in RETAINED_BANK memory bank has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
7:2	RESERVED		R	0x00
1	LOSTCONTEXT_RFF	Specify if RFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of L4_PER_RET_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
0	RESERVED		R	0

Table 3-687. Register Call Summary for Register RM_L4PER_UART3_CONTEXT

Power Management Functional Description • PD_L4_PER Description: [0]
PRCM Register Manual • L4PER_PRM Register Summary: [1]

Table 3-688. PM_L4PER_UART4_WKDEP

Address Offset	0x0000 0158		
Physical Address	0x4A30 7558	**Instance**	L4PER_PRM
Description	This register controls wakeup dependency based on UART4 service requests.		
Type	RW		

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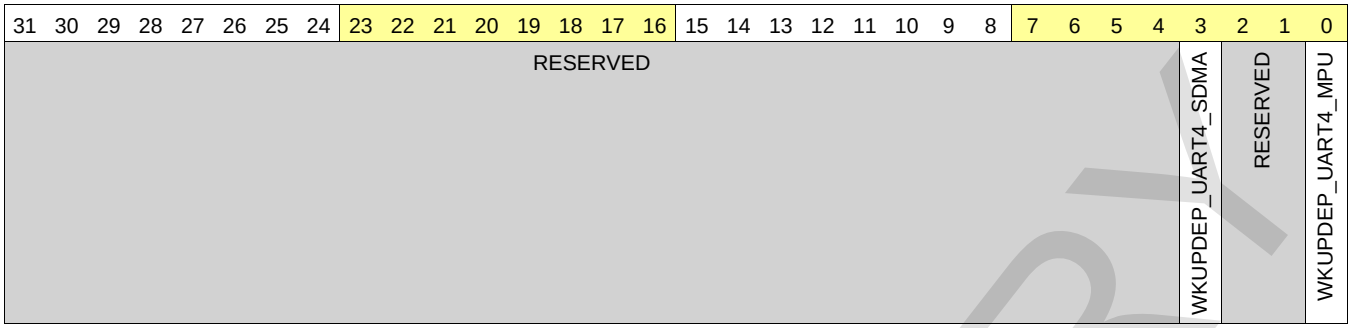


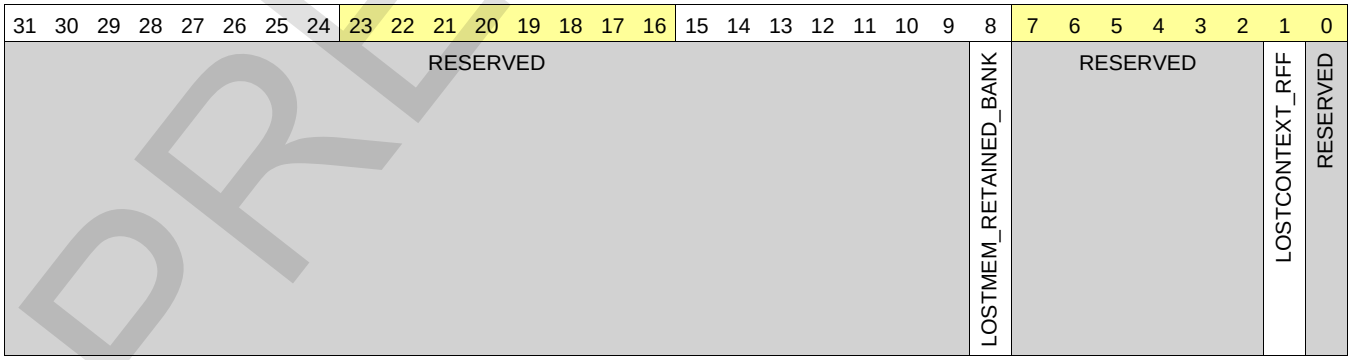
Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0000000
3	WKUPDEP_UART4_SDMA	Wakeup dependency from UART4 module (softwareakeup signal) towards SDMA + L3_2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
2:1	RESERVED		R	0x0
0	WKUPDEP_UART4_MPU	Wakeup dependency from UART4 module (softwareakeup signal) towards MPU + L3_1 + L3_2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-689. Register Call Summary for Register PM_L4PER_UART4_WKDEP

Clock Management Functional Description • Clock Domain Dependency: [0] [1]
PRCM Register Manual • L4PER_PRM Register Summary: [2]

Table 3-690. RM_L4PER_UART4_CONTEXT

Address Offset	0x0000 015C		
Physical Address	0x4A30 755C	**Instance**	L4PER_PRM
Description	This register contains dedicated UART4 context statuses. [warm reset insensitive]		
Type	RW		



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Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	LOSTMEM_RETAINED_BANK	Specify if memory-based context in RETAINED_BANK memory bank has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
7:2	RESERVED		R	0x00
1	LOSTCONTEXT_RFF	Specify if RFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of L4_PER_RET_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
0	RESERVED		R	0

Table 3-691. Register Call Summary for Register RM_L4PER_UART4_CONTEXT

Power Management Functional Description • PD_L4_PER Description: [0]
PRCM Register Manual • L4PER_PRM Register Summary: [1]

Table 3-692. PM_L4PER_MMCSD5_WKDEP

Address Offset	0x0000 0160		
Physical Address	0x4A30 7560	**Instance**	L4PER_PRM
Description	This register controls wakeup dependency based on MMCSD5 service requests.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												WKUPDEP_MMCSD5_SDMA	RESERVED	WKUPDEP_MMCSD5_MPU_M3	WKUPDEP_MMCSD5_MPU

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0000000
3	WKUPDEP_MMCSD5_SDMA	Wakeup dependency from MMCSD5 module (softwareakeup signal) towards SDMA + L3_2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
2	RESERVED		R	0
1	WKUPDEP_MMCSD5_MPU_M3	Wakeup dependency from MMCSD5 module (softwareakeup signal) towards MPU_A3 + L3_2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

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Bits	Field Name	Description	Type	Reset
0	WKUPDEP_MMCSD5_MPU	Wakeup dependency from MMCSD5 module (softwareakeup signal) towards MPU + L3_1 + L3_2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-693. Register Call Summary for Register PM_L4PER_MMCSD5_WKDEP

Clock Management Functional Description • Clock Domain Dependency: [0] [1] [2]
PRCM Register Manual • L4PER_PRM Register Summary: [3]

Table 3-694. RM_L4PER_MMCSD5_CONTEXT

Address Offset	0x0000 0164		
Physical Address	0x4A30 7564	**Instance**	L4PER_PRM
Description	This register contains dedicated MMCSD5 context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							LOSTMEM_NONRETAINED_BANK	RESERVED							LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	LOSTMEM_NONRETAINED_BANK	Specify if memory-based context in NONRETAINED_BANK memory bank has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
7:1	RESERVED		R	0x00
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of L4_PER_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-695. Register Call Summary for Register RM_L4PER_MMCSD5_CONTEXT

Power Management Functional Description • PD_L4_PER Description: [0]
PRCM Register Manual • L4PER_PRM Register Summary: [1]

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3.11.15 WKUP_PRM Registers

3.11.15.1 WKUP_PRM Register Summary

Table 3-696. WKUP_PRM Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	WKUP_PRM L4 Base Address
RM_WKUP_L4WKUP_CONTEXT	RW	32	0x0000 0024	0x4A30 7724
RESERVED	RW	32	0x0000 002C	0x4A30 772C
PM_WKUP_WDTIMER2_WKDEP	RW	32	0x0000 0030	0x4A30 7730
RM_WKUP_WDTIMER2_CONTEXT	RW	32	0x0000 0034	0x4A30 7734
PM_WKUP_GPIO1_WKDEP	RW	32	0x0000 0038	0x4A30 7738
RM_WKUP_GPIO1_CONTEXT	RW	32	0x0000 003C	0x4A30 773C
PM_WKUP_GPTIMER1_WKDEP	R	32	0x0000 0040	0x4A30 7740
RM_WKUP_GPTIMER1_CONTEXT	RW	32	0x0000 0044	0x4A30 7744
RESERVED	R	32	0x0000 0048	0x4A30 7748
RESERVED	RW	32	0x0000 004C	0x4A30 774C
RM_WKUP_32KTIMER_CONTEXT	RW	32	0x0000 0054	0x4A30 7754
RESERVED	RW	32	0x0000 0058	0x4A30 7758
RESERVED	RW	32	0x0000 005C	0x4A30 775C
RM_WKUP_SARRAM_CONTEXT	RW	32	0x0000 0064	0x4A30 7764
PM_WKUP_KEYBOARD_WKDEP	R	32	0x0000 0078	0x4A30 7778
RM_WKUP_KEYBOARD_CONTEXT	RW	32	0x0000 007C	0x4A30 777C
RESERVED	R	32	0x0000 0080	0x4A30 7780
RESERVED	RW	32	0x0000 0084	0x4A30 7784

3.11.15.2 WKUP_PRM Register Description

Table 3-697. RM_WKUP_L4WKUP_CONTEXT

Address Offset	0x0000 0024		
Physical Address	0x4A30 7724	**Instance**	WKUP_PRM
Description	This register contains dedicated L4WKUP context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of WKUP_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

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Table 3-698. Register Call Summary for Register RM_WKUP_L4WKUP_CONTEXT

Power Management Functional Description • PD_WKUP Description: [0]
PRCM Register Manual • WKUP_PRM Register Summary: [1]

Table 3-699. PM_WKUP_WDTIMER2_WKDEP

Address Offset	0x0000 0030		
Physical Address	0x4A30 7730	**Instance**	WKUP_PRM
Description	This register controls wakeup dependency based on WDT2 service requests.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														WKUPDEP_WDT2_MPU_M3	WKUPDEP_WDT2_MPU

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	WKUPDEP_WDT2_MPU_M3	Wakeup dependency from WDT2 module (softwareakeup signal) towards MPU_A3 + L3_2 + L3_1 + L4_CFG domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
0	WKUPDEP_WDT2_MPU	Wakeup dependency from WDT2 module (softwareakeup signal) towards MPU + L3_1 + L4_CFG domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-700. Register Call Summary for Register PM_WKUP_WDTIMER2_WKDEP

Clock Management Functional Description • Clock Domain Dependency: [0] [1]
PRCM Register Manual • WKUP_PRM Register Summary: [2]

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Table 3-701. RM_WKUP_WDTIMER2_CONTEXT

Address Offset	0x0000 0034		
Physical Address	0x4A30 7734	**Instance**	WKUP_PRM
Description	This register contains dedicated WDT2 context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of WKUP_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-702. Register Call Summary for Register RM_WKUP_WDTIMER2_CONTEXT

Power Management Functional Description • PD_WKUP Description: [0]
PRCM Register Manual • WKUP_PRM Register Summary: [1]

Table 3-703. PM_WKUP_GPIO1_WKDEP

Address Offset	0x0000 0038		
Physical Address	0x4A30 7738	**Instance**	WKUP_PRM
Description	This register controls wakeup dependency based on GPIO1 service requests.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																									WKUPDEP_GPIO1_IRQ2_DSP	RESERVED					WKUPDEP_GPIO1_IRQ1_MPU_M3	WKUPDEP_GPIO1_IRQ1_MPU

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Bits	Field Name	Description	Type	Reset
31:7	RESERVED		R	0x0000000
6	WKUPDEP_GPIO1_IRQ2_DSP	Wakeup dependency from GPIO1 module (POINTRsoftwareAKEUP2 signal) towards DSP + L3_1 + L4_CFG domains Read 0x1: Dependency is enabled	R Rreturns 1s	1
5:2	RESERVED		R	0x0
1	WKUPDEP_GPIO1_IRQ1_MPU_M3	Wakeup dependency from GPIO1 module (POINTRsoftwareAKEUP1 signal) module towards MPU_A3 + L3_2 + L3_1 + L4_CFG domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
0	WKUPDEP_GPIO1_IRQ1_MPU	Wakeup dependency from GPIO1 module (POINTRsoftwareAKEUP1 signal) towards MPU + L3_1 + L4_CFG domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-704. Register Call Summary for Register PM_WKUP_GPIO1_WKDEP

Clock Management Functional Description • Clock Domain Dependency: [0] [1] [2]
PRCM Register Manual • WKUP_PRM Register Summary: [3]

Table 3-705. RM_WKUP_GPIO1_CONTEXT

Address Offset	0x0000 003C		
Physical Address	0x4A30 773C	**Instance**	WKUP_PRM
Description	This register contains dedicated GPIO1 context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of WKUP_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-706. Register Call Summary for Register RM_WKUP_GPIO1_CONTEXT

Power Management Functional Description • PD_WKUP Description: [0]
PRCM Register Manual • WKUP_PRM Register Summary: [1]

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Table 3-707. PM_WKUP_GPTIMER1_WKDEP

Address Offset	0x0000 0040		
Physical Address	0x4A30 7740	**Instance**	WKUP_PRM
Description	This register controls wakeup dependency based on TIMER1 service requests.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															WKUPDEP_TIMER1_MPU

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	WKUPDEP_TIMER1_MPU	Wakeup dependency from TIMER1 module (softwareakeup signal) towards MPU + L3_1 + L4_CFG domains Read 0x1: Dependency is enabled	R Rreturns 1s	1

Table 3-708. Register Call Summary for Register PM_WKUP_GPTIMER1_WKDEP

Clock Management Functional Description
- Clock Domain Dependency: [0]

PRCM Register Manual
- WKUP_PRM Register Summary: [1]

Table 3-709. RM_WKUP_GPTIMER1_CONTEXT

Address Offset	0x0000 0044		
Physical Address	0x4A30 7744	**Instance**	WKUP_PRM
Description	This register contains dedicated TIMER1 context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of WKUP_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

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Table 3-710. Register Call Summary for Register RM_WKUP_GPTIMER1_CONTEXT

Power Management Functional Description • PD_WKUP Description: [0]
PRCM Register Manual • WKUP_PRM Register Summary: [1]

Table 3-711. RM_WKUP_32KTIMER_CONTEXT

Address Offset	0x0000 0054		
Physical Address	0x4A30 7754	**Instance**	WKUP_PRM
Description	This register contains dedicated SYNCTIMER context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of WKUP_SYS_PWRON_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-712. Register Call Summary for Register RM_WKUP_32KTIMER_CONTEXT

Power Management Functional Description • PD_WKUP Description: [0]
PRCM Register Manual • WKUP_PRM Register Summary: [1]

Table 3-713. RM_WKUP_SARRAM_CONTEXT

Address Offset	0x0000 0064		
Physical Address	0x4A30 7764	**Instance**	WKUP_PRM
Description	This register contains dedicated SARRAM context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								LOSTMEM_WKUP_BANK	RESERVED						LOSTCONTEXT_DFF

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Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	LOSTMEM_WKUP_BANK	Specify if memory-based context in WKUP_BANK memory bank has been lost due to a previous global cold reset. 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
7:1	RESERVED		R	0x00
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of WKUP_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-714. Register Call Summary for Register RM_WKUP_SARRAM_CONTEXT

Power Management Functional Description • PD_WKUP Description: [0]
PRCM Register Manual • WKUP_PRM Register Summary: [1]

Table 3-715. PM_WKUP_KEYBOARD_WKDEP

Address Offset	0x0000 0078		
Physical Address	0x4A30 7778	**Instance**	WKUP_PRM
Description	This register controls wakeup dependency based on KEYBOARD service requests.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															WKUPDEP_KEYBOARD_MPU

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	WKUPDEP_KEYBOARD_MPU	Wakeup dependency from KEYBOARD module (softwareakeup signal) towards MPU + L3_1 + L4_CFG domains Read 0x1: Dependency is enabled	R Rreturns 1s	1

Table 3-716. Register Call Summary for Register PM_WKUP_KEYBOARD_WKDEP

Clock Management Functional Description • Clock Domain Dependency: [0]
PRCM Register Manual • WKUP_PRM Register Summary: [1]

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Table 3-717. RM_WKUP_KEYBOARD_CONTEXT

Address Offset	0x0000 007C		
Physical Address	0x4A30 777C	**Instance**	WKUP_PRM
Description	This register contains dedicated KEYBOARD context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of WKUP_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-718. Register Call Summary for Register RM_WKUP_KEYBOARD_CONTEXT

Power Management Functional Description • PD_WKUP Description: [0]
PRCM Register Manual • WKUP_PRM Register Summary: [1]

3.11.16 WKUP_CM Registers

3.11.16.1 WKUP_CM Register Summary

Table 3-719. WKUP_CM Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	WKUP_CM L4 Base Address
CM_WKUP_CLKSTCTRL	RW	32	0x0000 0000	0x4A30 7800
CM_WKUP_L4WKUP_CLKCTRL	R	32	0x0000 0020	0x4A30 7820
RESERVED	R	32	0x0000 0028	0x4A30 7828
CM_WKUP_WDTIMER2_CLKCTRL	RW	32	0x0000 0030	0x4A30 7830
CM_WKUP_GPIO1_CLKCTRL	RW	32	0x0000 0038	0x4A30 7838
CM_WKUP_GPTIMER1_CLKCTRL	RW	32	0x0000 0040	0x4A30 7840
RESERVED	R	32	0x0000 0048	0x4A30 7848
CM_WKUP_32KTIMER_CLKCTRL	R	32	0x0000 0050	0x4A30 7850
RESERVED	RW	32	0x0000 0058	0x4A30 7858
CM_WKUP_SARRAM_CLKCTRL	R	32	0x0000 0060	0x4A30 7860
CM_WKUP_KEYBOARD_CLKCTRL	RW	32	0x0000 0078	0x4A30 7878
RESERVED	RW	32	0x0000 0080	0x4A30 7880
CM_WKUP_BANDGAP_CLKCTRL	RW	32	0x0000 0088	0x4A30 7888

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3.11.16.2 WKUP_CM Register Description

Table 3-720. CM_WKUP_CLKSTCTRL

Address Offset	0x0000 0000		
Physical Address	0x4A30 7800	**Instance**	WKUP_CM
Description	This register enables the domain power state transition. It controls the hardware supervised domain power state transition between ON-ACTIVE and ON-INACTIVE states. It also holds 1 status bit per clock input of the domain.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																		CLKACTIVITY_WKUP_TS_FCLK	CLKACTIVITY_L4_WKUP_ICLK	CLKACTIVITY_WKUP_32K_FCLK	RESERVED	CLKACTIVITY_ABE_LP_CLK	CLKACTIVITY_SYS_CLK	RESERVED						CLKTRCTRL	

Bits	Field Name	Description	Type	Reset
31:14	RESERVED		R	0x00000
13	CLKACTIVITY_WKUP_TS_FCLK	This field indicates the state of the WKUP_TS_FCLK clock in the domain. [warm reset insensitive] Read 0x1: Corresponding clock is running or gating/ungating transition is on-going Read 0x0: Corresponding clock is definitely gated	R	0
12	CLKACTIVITY_L4_WKUP_ICLK	This field indicates the state of the clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
11	CLKACTIVITY_WKUP_32K_FCLK	This field indicates the state of the clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
10	RESERVED		R	0
9	CLKACTIVITY_ABE_LP_CLK	This field indicates the state of the clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
8	CLKACTIVITY_SYS_CLK	This field indicates the state of the SYS_CLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
7:2	RESERVED		R	0x00

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Bits	Field Name	Description	Type	Reset
1:0	CLKTRCTRL	Controls the clock state transition of the WKUP clock domain. 0x0: NO_SLEEP: Sleep transition cannot be initiated. Wakeup transition may however occur. Read 0x1: Reserved Read 0x2: Reserved 0x3: HW_AUTO: Automatic transition is enabled. Sleep and wakeup transition are based upon hardware conditions.	RW	0x0

Table 3-721. Register Call Summary for Register CM_WKUP_CLKSTCTRL

Clock Management Functional Description • Clock Domain Modes: [0] [1] [2] [3] [4]
PRCM Register Manual • WKUP_CM Register Summary: [5]

Table 3-722. CM_WKUP_L4WKUP_CLKCTRL

Address Offset	0x0000 0020		
Physical Address	0x4A30 7820	**Instance**	WKUP_CM
Description	This register manages the L4WKUP clocks.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED								MODULEMODE							

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. Read 0x1: Module is managed automatically by hardware according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CLKTRCTRL=3, any INTRCONN access to module is always granted. Module clocks may be gated according to the clock domain state.	R Rreturns	0x1

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Table 3-723. Register Call Summary for Register CM_WKUP_L4WKUP_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • WKUP_CM Register Summary: [2]

Table 3-724. CM_WKUP_WDTIMER2_CLKCTRL

Address Offset	0x0000 0030		
Physical Address	0x4A30 7830	**Instance**	WKUP_CM
Description	This register manages the WDT2 clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED								MODULEMODE							

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by software. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen. Read 0x3: Reserved	RW	0x0

Table 3-725. Register Call Summary for Register CM_WKUP_WDTIMER2_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • WKUP_CM Register Summary: [2]

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Table 3-726. CM_WKUP_GPIO1_CLKCTRL

Address Offset	0x0000 0038		
Physical Address	0x4A30 7838	**Instance**	WKUP_CM
Description	This register manages the GPIO1 clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED							OPTFCLKEN_DBCLK	RESERVED						MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:9	RESERVED		R	0x00
8	OPTFCLKEN_DBCLK	Optional functional clock control. 0x0: Optional functional clock is disabled 0x1: Optional functional clock is enabled	RW	0
7:2	RESERVED		R	0x00
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by software. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). 0x1: Module is managed automatically by hardware according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CLKTRCTRL=3, any INTRCONN access to module is always granted. Module clocks may be gated according to the clock domain state. Read 0x2: Reserved Read 0x3: Reserved	RW	0x0

Table 3-727. Register Call Summary for Register CM_WKUP_GPIO1_CLKCTRL

Clock Management Functional Description
- Clock Domain Module Attributes: [0] [1]

PRCM Register Manual
- WKUP_CM Register Summary: [2]

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Table 3-728. CM_WKUP_GPTIMER1_CLKCTRL

Address Offset	0x0000 0040		
Physical Address	0x4A30 7840	**Instance**	WKUP_CM
Description	This register manages the TIMER1 clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							CLKSEL	RESERVED						IDLEST		RESERVED														MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:25	RESERVED		R	0x00
24	CLKSEL	Select the source of the functional clock 0x0: Selects the SYS_CLK as the source 0x1: Selects the 32KHz as the source	RW	0
23:18	RESERVED		R	0x00
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by software. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen. Read 0x3: Reserved	RW	0x0

Table 3-729. Register Call Summary for Register CM_WKUP_GPTIMER1_CLKCTRL

Clock Management Functional Description
- PRM Clock Source: [0]
- Clock Domain Module Attributes: [1] [2]

PRCM Register Manual
- WKUP_CM Register Summary: [3]

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Table 3-730. CM_WKUP_32KTIMER_CLKCTRL

Address Offset	0x0000 0050		
Physical Address	0x4A30 7850	**Instance**	WKUP_CM
Description	This register manages the SYNCTIMER clocks.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED														MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. Read 0x1: Module is managed automatically by hardware according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CLKTRCTRL=3, any INTRCONN access to module is always granted. Module clocks may be gated according to the clock domain state.	R Rreturns	0x1

Table 3-731. Register Call Summary for Register CM_WKUP_32KTIMER_CLKCTRL

Clock Management Functional Description
- Clock Domain Module Attributes: [0] [1]

PRCM Register Manual
- WKUP_CM Register Summary: [2]

Table 3-732. CM_WKUP_SARRAM_CLKCTRL

Address Offset	0x0000 0060		
Physical Address	0x4A30 7860	**Instance**	WKUP_CM
Description	This register manages the SARRAM clocks.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED														MODULEMODE	

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Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. Read 0x1: Module is managed automatically by hadware according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CLKTRCTRL=3, any INTRCONN access to module is always granted. Module clocks may be gated according to the clock domain state.	R Rreturns	0x1

Table 3-733. Register Call Summary for Register CM_WKUP_SARRAM_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • WKUP_CM Register Summary: [2]

Table 3-734. CM_WKUP_KEYBOARD_CLKCTRL

Address Offset	0x0000 0078		
Physical Address	0x4A30 7878	**Instance**	WKUP_CM
Description	This register manages the KEYBOARD clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED														MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000

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Bits	Field Name	Description	Type	Reset
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by software. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen. Read 0x3: Reserved	RW	0x0

Table 3-735. Register Call Summary for Register CM_WKUP_KEYBOARD_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • WKUP_CM Register Summary: [2]

Table 3-736. CM_WKUP_BANDGAP_CLKCTRL

Address Offset	0x0000 0088		
Physical Address	0x4A30 7888	**Instance**	WKUP_CM
Description	This register manages the clock delivered to the Bandgap and SYSCTRL_GENERAL_CORE modules for the Thermal Sensor feature. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						CLKSEL		RESERVED															OPTFCLKEN_TS_FCLK	RESERVED							

Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x00
25:24	CLKSEL	Selects the divider value for generating the Thermal Sensor clock from L4WKUP_ICLK source. The divider has to be selected so as to guarantee a frequency between 1MHz and 2MHz. 0x0: Divide by 8 0x1: Divide by 16 0x2: Divide by 32 0x3: Reserved	RW	0x2
23:9	RESERVED		R	0x0000
8	OPTFCLKEN_TS_FCLK	Optional functional clock control. 0x0: Optional functional clock is disabled 0x1: Optional functional clock is enabled	RW	0
7:0	RESERVED		R	0x00

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Table 3-737. Register Call Summary for Register CM_WKUP_BANDGAP_CLKCTRL

Clock Management Functional Description • PRM Clock Source: [0]
PRCM Register Manual • WKUP_CM Register Summary: [1]

3.11.17 EMU_PRM Registers

3.11.17.1 EMU_PRM Register Summary

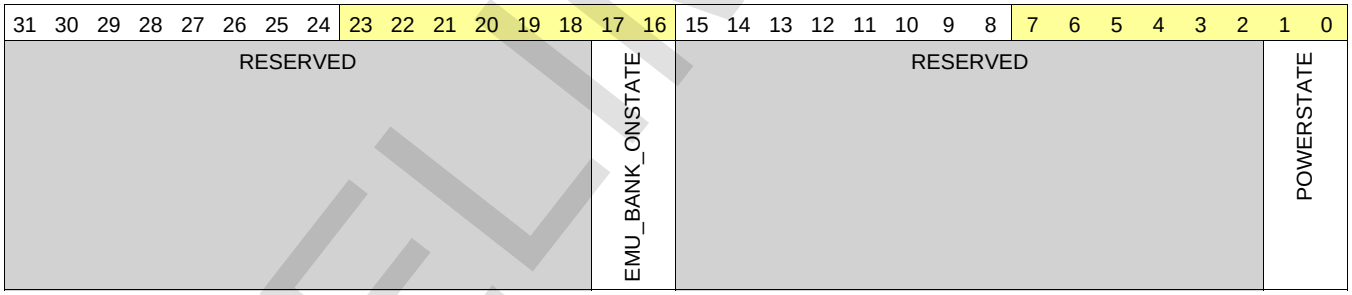
Table 3-738. EMU_PRM Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	EMU_PRM L4 Base Address
PM_EMU_PWRSTCTRL	R	32	0x0000 0000	0x4A30 7900
PM_EMU_PWRSTST	R	32	0x0000 0004	0x4A30 7904
RM_EMU_DEBUGSS_CONTEXT	RW	32	0x0000 0024	0x4A30 7924

3.11.17.2 EMU_PRM Register Description

Table 3-739. PM_EMU_PWRSTCTRL

Address Offset	0x0000 0000		
Physical Address	0x4A30 7900	**Instance**	EMU_PRM
Description	This register controls the EMU power state to reach upon a domain sleep transition		
Type	R		



Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	EMU_BANK_ONSTATE	EMU memory state when domain is ON. Read 0x3: Memory bank is on when the domain is ON.	R Rreturns 1s	0x3
15:2	RESERVED		R	0x0000
1:0	POWERSTATE	Power state control Read 0x0: OFF state	R	0x0

Table 3-740. Register Call Summary for Register PM_EMU_PWRSTCTRL

Power Management Functional Description • Power Domain Modes: [0] [1]
PRCM Register Manual • EMU_PRM Register Summary: [2]

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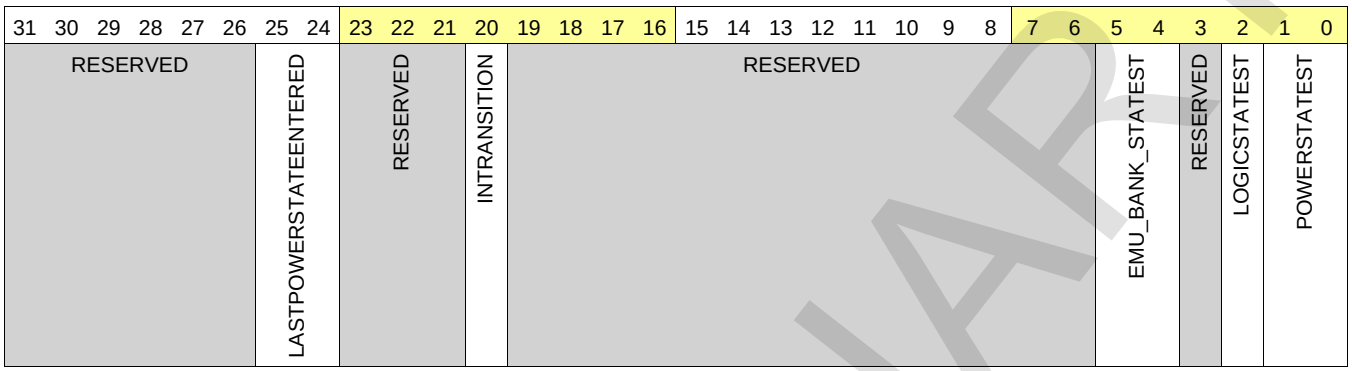
Table 3-741. PM_EMU_PWRSTST

Address Offset	0x0000 0004		
Physical Address	0x4A30 7904	**Instance**	EMU_PRM
Description	This register provides a status on the EMU domain current power state. [warm reset insensitive]		
Type	R		



Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x00
25:24	LASTPOWERSTATEENTERED	Last low power state entered. Set to 0x3 upon write of the same only. This register is intended for debug purpose only. Read 0x0: Power domain was previously OFF Read 0x1: Power domain was previously in RETENTION Read 0x2: Power domain was previously ON-INACTIVE Read 0x3: Power domain was previously ON-ACTIVE	RW W1toSet	0x0
23:21	RESERVED		R	0x0
20	INTRANSITION	Domain transition status Read 0x0: No ongoing transition on power domain Read 0x1: Power domain transition is in progress.	R	0
19:6	RESERVED		R	0x0000
5:4	EMU_BANK_STATEST	EMU memory bank state status Read 0x0: Memory is OFF Read 0x1: Reserved Read 0x2: Reserved Read 0x3: Memory is ON It is supplied by WKUP LDO	R	0x3
3	RESERVED		R	0
2	LOGICSTATEST	Logic state status Read 0x0: Logic in domain is OFF Read 0x1: Logic in domain is ON	R	1
1:0	POWERSTATEST	Current power state status Read 0x0: Power domain is OFF Read 0x3: Power domain is ON-ACTIVE	R	0x3

Table 3-742. Register Call Summary for Register PM_EMU_PWRSTST

Power Management Functional Description
- Power Domain Modes: [0] [1] [2] [3]

PRCM Register Manual
- EMU_PRM Register Summary: [4]

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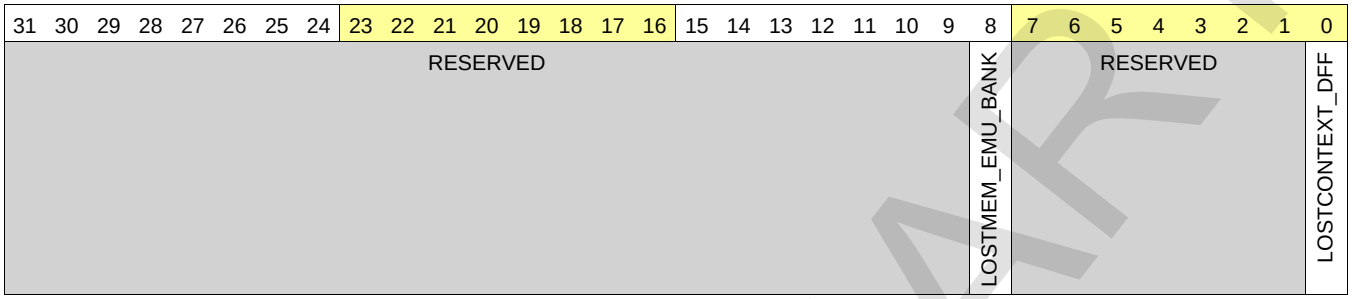
Table 3-743. RM_EMU_DEBUGSS_CONTEXT

Address Offset	0x0000 0024		
Physical Address	0x4A30 7924	**Instance**	EMU_PRM
Description	This register contains dedicated DEBUGSS context statuses. [warm reset insensitive]		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	LOSTMEM_EMU_BANK	Specify if memory-based context in EMU_BANK memory bank has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
7:1	RESERVED		R	0x00
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of EMU_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-744. Register Call Summary for Register RM_EMU_DEBUGSS_CONTEXT

PRCM Register Manual
- EMU_PRM Register Summary: [0]

3.11.18 EMU_CM Registers

3.11.18.1 EMU_CM Register Summary

Table 3-745. EMU_CM Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	EMU_CM L4 Base Address
CM_EMU_CLKSTCTRL	RW	32	0x0000 0000	0x4A30 7A00
CM_EMU_DYNAMICDEP	RW	32	0x0000 0008	0x4A30 7A08
CM_EMU_DEBUGSS_CLKCTRL	RW	32	0x0000 0020	0x4A30 7A20

3.11.18.2 EMU_CM Register Description

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Table 3-746. CM_EMU_CLKSTCTRL

Address Offset	0x0000 0000		
Physical Address	0x4A30 7A00	**Instance**	EMU_CM
Description	This register enables the EMU domain power state transition. It controls the hardware supervised domain power state transition between ON-ACTIVE and ON-INACTIVE states. It also holds 1 status bit per clock input of the domain. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						CLKACTIVITY_CORE_DPLL_EMU_CLK	CLKACTIVITY_EMU_SYS_CLK	RESERVED						CLKTRCTRL	

Bits	Field Name	Description	Type	Reset
31:10	RESERVED		R	0x0000000
9	CLKACTIVITY_CORE_DPLL_EMU_CLK	This field indicates the state of the CORE_DPLL_EMU_CLK clock in the domain. Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
8	CLKACTIVITY_EMU_SYS_CLK	This field indicates the state of the EMU_SYS_CLK clock in the domain. Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
7:2	RESERVED		R	0x00
1:0	CLKTRCTRL	Controls the clock state transition of the EMU clock domain. Read 0x0: Reserved Read 0x1: Reserved 0x2: SW_WKUP: Start a software forced wake-up transition on the domain. 0x3: HW_AUTO: Automatic transition is enabled. Sleep and wakeup transition are based upon hardware conditions.	RW	0x2

Table 3-747. Register Call Summary for Register CM_EMU_CLKSTCTRL

Clock Management Functional Description
- Clock Domain Modes: [0] [1] [2]

PRCM Register Manual
- EMU_CM Register Summary: [3]

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Table 3-748. CM_EMU_DYNAMICDEP

Address Offset	0x0000 0008		
Physical Address	0x4A30 7A08	**Instance**	EMU_CM
Description	This register controls the dynamic domain depedencies from EMU domain towards 'target' domains. It is relevant only for domain having INTRCONN master port(s).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				WINDOWSIZE				RESERVED																	L3_2_DYNDEP	RESERVED						

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:24	WINDOWSIZE	Size of sliding window used to monitor INTRCONN interface activity for determination of auto-sleep feature. Time unit defined by CM_DYN_DEP_PRESCAL register.	RW	0x4
23:7	RESERVED		R	0x00000
6	L3_2_DYNDEP	Dynamic dependency towards L3_2 clock domain Read 0x1: Dependency is enabled	R Rreturns 1s	1
5:0	RESERVED		R	0x00

Table 3-749. Register Call Summary for Register CM_EMU_DYNAMICDEP

Clock Management Functional Description
- Clock Domain Dependency: [0]

PRCM Register Manual
- EMU_CM Register Summary: [1]

Table 3-750. CM_EMU_DEBUGSS_CLKCTRL

Address Offset	0x0000 0020		
Physical Address	0x4A30 7A20	**Instance**	EMU_CM
Description	This register manages the DEBUGSS clocks. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			CLKSEL_PMD_STM_CLK			CLKSEL_PMD_TRACE_CLK			PMD_TRACE_MUX_CTRL		PMD_STM_MUX_CTRL		RESERVED	STBYST	IDLEST	RESERVED															MODULEMODE	

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Bits	Field Name	Description	Type	Reset
31:30	RESERVED		R	0x0
29:27	CLKSEL_PMD_STM_CLK	Selection of STM clock division Read 0x0: Reserved 0x1: STM_CLK is the selected STM source clock divided by 1 0x2: STM_CLK is the selected STM source clock divided by 2 Read 0x3: Reserved 0x4: STM_CLK is the selected STM source clock divided by 4 Read 0x5: Reserved Read 0x6: Reserved Read 0x7: Reserved	RW	0x1
26:24	CLKSEL_PMD_TRACE_CLK	Selection of TRACE clock division Read 0x0: Reserved 0x1: TRACE_CLK is the selected TRACE source clock divided by 1 0x2: TRACE_CLK is the selected TRACE source clock divided by 2 Read 0x3: Reserved 0x4: TRACE_CLK is the selected TRACE source clock divided by 4 Read 0x5: Reserved Read 0x6: Reserved Read 0x7: Reserved	RW	0x1
23:22	PMD_TRACE_MUX_CTRL	Selection of TRACE source clock 0x0: TRACE source clock is SYS_CLK 0x1: TRACE source clock is CORE_DPLL_EMU_CLK Read 0x2: Reserved Read 0x3: Reserved	RW	0x0
21:20	PMD_STM_MUX_CTRL	Selection of STM source clock 0x0: STM source clock is SYS_CLK 0x1: STM source clock is CORE_DPLL_EMU_CLK Read 0x2: Reserved Read 0x3: Reserved	RW	0x0
19	RESERVED		R	0
18	STBYST	Module standby status Read 0x0: Module is functional (not in standby) Read 0x1: Module is in standby	R	1
17:16	IDLEST	Module idle status Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000

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Bits	Field Name	Description	Type	Reset
1:0	MODULEMODE	Control the way mandatory clocks are managed. Read 0x1: Module is managed automatically by hardware according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CLKTRCTRL=3, any INTRCONN access to module is always granted. Module clocks may be gated according to the clock domain state.	R Rreturns	0x1

Table 3-751. Register Call Summary for Register CM_EMU_DEBUGSS_CLKCTRL

Clock Management Functional Description • Overview: [0] [1]
PRCM Register Manual • EMU_CM Register Summary: [2]

3.11.19 DEVICE_PRM Registers

3.11.19.1 DEVICE_PRM Register Summary

Table 3-752. DEVICE_PRM Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	DEVICE_PRM L4 Base Address
PRM_RSTCTRL	RW	32	0x0000 0000	0x4A30 7B00
PRM_RSTST	RW	32	0x0000 0004	0x4A30 7B04
PRM_RSTTIME	RW	32	0x0000 0008	0x4A30 7B08
PRM_CLKREQCTRL	RW	32	0x0000 000C	0x4A30 7B0C
PRM_VOLTCTRL	RW	32	0x0000 0010	0x4A30 7B10
PRM_PWRREQCTRL	RW	32	0x0000 0014	0x4A30 7B14
PRM_PSCON_COUNT	RW	32	0x0000 0018	0x4A30 7B18
PRM_IO_COUNT	RW	32	0x0000 001C	0x4A30 7B1C
PRM_IO_PMCTRL	RW	32	0x0000 0020	0x4A30 7B20
PRM_VOLTSETUP_WARMRESET	RW	32	0x0000 0024	0x4A30 7B24
PRM_VOLTSETUP_CORE_OFF	RW	32	0x0000 0028	0x4A30 7B28
PRM_VOLTSETUP_MPU_OFF	RW	32	0x0000 002C	0x4A30 7B2C
PRM_VOLTSETUP_IVA_OFF	RW	32	0x0000 0030	0x4A30 7B30
PRM_VOLTSETUP_CORE_RET_SLEEP	RW	32	0x0000 0034	0x4A30 7B34
PRM_VOLTSETUP_MPU_RET_SLEEP	RW	32	0x0000 0038	0x4A30 7B38
PRM_VOLTSETUP_IVA_RET_SLEEP	RW	32	0x0000 003C	0x4A30 7B3C
PRM_VP_CORE_CONFIG	RW	32	0x0000 0040	0x4A30 7B40
PRM_VP_CORE_STATUS	R	32	0x0000 0044	0x4A30 7B44
PRM_VP_CORE_VLIMITTO	RW	32	0x0000 0048	0x4A30 7B48
PRM_VP_CORE_VOLTAGE	R	32	0x0000 004C	0x4A30 7B4C
PRM_VP_CORE_VSTEPMAX	RW	32	0x0000 0050	0x4A30 7B50
PRM_VP_CORE_VSTEPMIN	RW	32	0x0000 0054	0x4A30 7B54
PRM_VP_MPU_CONFIG	RW	32	0x0000 0058	0x4A30 7B58
PRM_VP_MPU_STATUS	R	32	0x0000 005C	0x4A30 7B5C
PRM_VP_MPU_VLIMITTO	RW	32	0x0000 0060	0x4A30 7B60
PRM_VP_MPU_VOLTAGE	R	32	0x0000 0064	0x4A30 7B64
PRM_VP_MPU_VSTEPMAX	RW	32	0x0000 0068	0x4A30 7B68
PRM_VP_MPU_VSTEPMIN	RW	32	0x0000 006C	0x4A30 7B6C
PRM_VP_IVA_CONFIG	RW	32	0x0000 0070	0x4A30 7B70

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Table 3-752. DEVICE_PRM Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	DEVICE_PRM L4 Base Address
PRM_VP_IVA_STATUS	R	32	0x0000 0074	0x4A30 7B74
PRM_VP_IVA_VLIMITTO	RW	32	0x0000 0078	0x4A30 7B78
PRM_VP_IVA_VOLTAGE	R	32	0x0000 007C	0x4A30 7B7C
PRM_VP_IVA_VSTEPMAX	RW	32	0x0000 0080	0x4A30 7B80
PRM_VP_IVA_VSTEPMIN	RW	32	0x0000 0084	0x4A30 7B84
PRM_VC_SMPS_SA	RW	32	0x0000 0088	0x4A30 7B88
PRM_VC_VAL_SMPS_RA_VOL	RW	32	0x0000 008C	0x4A30 7B8C
PRM_VC_VAL_SMPS_RA_CMD	RW	32	0x0000 0090	0x4A30 7B90
PRM_VC_VAL_CMD_VDD_CORE_L	RW	32	0x0000 0094	0x4A30 7B94
PRM_VC_VAL_CMD_VDD_MPU_L	RW	32	0x0000 0098	0x4A30 7B98
PRM_VC_VAL_CMD_VDD_IVA_L	RW	32	0x0000 009C	0x4A30 7B9C
PRM_VC_VAL_BYPASS	RW	32	0x0000 00A0	0x4A30 7BA0
PRM_VC_CFG_CHANNEL	RW	32	0x0000 00A4	0x4A30 7BA4
PRM_VC_CFG_I2C_MODE	RW	32	0x0000 00A8	0x4A30 7BA8
PRM_VC_CFG_I2C_CLK	RW	32	0x0000 00AC	0x4A30 7BAC
PRM_SRAM_COUNT	RW	32	0x0000 00B0	0x4A30 7BB0
PRM_SRAM_WKUP_SETUP	RW	32	0x0000 00B4	0x4A30 7BB4
PRM_LDO_SRAM_CORE_SETUP	RW	32	0x0000 00B8	0x4A30 7BB8
PRM_LDO_SRAM_CORE_CTRL	RW	32	0x0000 00BC	0x4A30 7BBC
PRM_LDO_SRAM_MPU_SETUP	RW	32	0x0000 00C0	0x4A30 7BC0
PRM_LDO_SRAM_MPU_CTRL	RW	32	0x0000 00C4	0x4A30 7BC4
PRM_LDO_SRAM_IVA_SETUP	RW	32	0x0000 00C8	0x4A30 7BC8
PRM_LDO_SRAM_IVA_CTRL	RW	32	0x0000 00CC	0x4A30 7BCC
PRM_LDO_ABB_MPU_SETUP	RW	32	0x0000 00D0	0x4A30 7BD0
PRM_LDO_ABB_MPU_CTRL	RW	32	0x0000 00D4	0x4A30 7BD4
PRM_LDO_ABB_IVA_SETUP	RW	32	0x0000 00D8	0x4A30 7BD8
PRM_LDO_ABB_IVA_CTRL	RW	32	0x0000 00DC	0x4A30 7BDC
PRM_LDO_BANDGAP_SETUP	RW	32	0x0000 00E0	0x4A30 7BE0
PRM_DEVICE_OFF_CTRL	RW	32	0x0000 00E4	0x4A30 7BE4
PRM_PHASE1_CNDP	R	32	0x0000 00E8	0x4A30 7BE8
PRM_PHASE2A_CNDP	RW	32	0x0000 00EC	0x4A30 7BEC
PRM_PHASE2B_CNDP	RW	32	0x0000 00F0	0x4A30 7BF0
RESERVED	RW	32	0x0000 00F4	0x4A30 7BF4
PRM_VC_ERRST	RW	32	0x0000 00F8	0x4A30 7BF8

3.11.19.2 DEVICE_PRM Register Description

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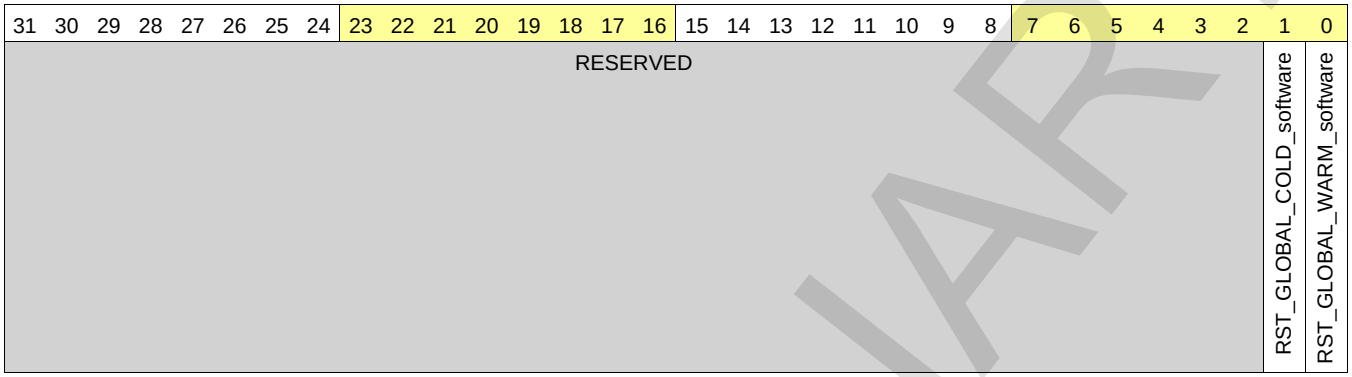
Table 3-753. PRM_RSTCTRL

Address Offset	0x0000 0000		
Physical Address	0x4A30 7B00	**Instance**	DEVICE_PRM
Description	Global software cold and warm reset control. This register is auto-cleared. Only write 1 is possible. A read returns 0 only.		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	RST_GLOBAL_COLD_software	Global COLD software reset control. This bit is reset only upon a global cold source of reset. 0x0: Global COLD software reset is cleared. 0x1: Triggers a global COLD software reset. The software must ensure the SDRAM is properly put in sef-refresh mode before applying this reset.	RW	0
0	RST_GLOBAL_WARM_software	Global WARM software reset control. This bit is reset upon any global source of reset (warm and cold). 0x0: Global warm software reset is cleared. 0x1: Triggers a global warm software reset.	RW	0

Table 3-754. Register Call Summary for Register PRM_RSTCTRL

Reset Management Functional Description • Global Reset Sources: [0] [1]
PRCM Register Manual • DEVICE_PRM Register Summary: [2]

Table 3-755. PRM_RSTST

Address Offset	0x0000 0004		
Physical Address	0x4A30 7B04	**Instance**	DEVICE_PRM
Description	This register logs the global reset sources. Each bit is set upon release of the domain reset signal. Must be cleared by software. [warm reset insensitive]		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																					C2C_RST	ICEPICK_RST	VDD_CORE_VOLT_MGR_RST	VDD_IVA_VOLT_MGR_RST	VDD_MPU_VOLT_MGR_RST	EXTERNAL_WARM_RST	RESERVED	MPU_WDT_RST	RESERVED	GLOBAL_WARM_SW_RST	GLOBAL_COLD_RST

Bits	Field Name	Description	Type	Reset
31:11	RESERVED		R	0x000000
10	C2C_RST	C2C warm reset event. This is a source of global warm reset. 0x0: No C2C warm reset. 0x1: C2C warm reset has occurred.	RW W1toClr	0
9	ICEPICK_RST	IcePick reset event. This is a source of global warm reset initiated by the emulation. 0x0: No ICEPICK reset. 0x1: IcePick reset has occurred.	RW W1toClr	0
8	VDD_CORE_VOLT_MGR_RST	VDD_CORE voltage manager reset event This is a source of global WARM reset. 0x0: No VDD_CORE voltage manager reset. 0x1: VDD_CORE voltage manager reset has occurred.	RW W1toClr	0
7	VDD_IVA_VOLT_MGR_RST	VDD_IVA voltage manager reset event This is a source of global WARM reset. 0x0: No VDD_IVA voltage manager reset. 0x1: VDD_IVA voltage manager reset has occurred.	RW W1toClr	0
6	VDD_MPU_VOLT_MGR_RST	VDD_MPU voltage manager reset event This is a source of global WARM reset. 0x0: No VDD_MPU voltage manager reset. 0x1: VDD_MPU voltage manager reset has occurred.	RW W1toClr	0
5	EXTERNAL_WARM_RST	External warm reset event 0x0: No global warm reset. 0x1: Global external warm reset has occurred.	RW W1toClr	0
4	RESERVED		RW W1toClr	0
3	MPU_WDT_RST	MPU Watchdog timer reset event. This is a source of global WARM reset. 0x0: No MPU watchdog reset. 0x1: MPU wachtdog reset has occurred.	RW W1toClr	0
2	RESERVED		RW W1toClr	0
1	GLOBAL_WARM_SW_RST	Global warm software reset event 0x0: No global warm software reset 0x1: Global warm software reset has occurred.	RW W1toClr	0
0	GLOBAL_COLD_RST	Power-on (cold) reset event 0x0: No power-on reset. 0x1: Power-on reset has occurred.	RW W1toClr	1

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Table 3-756. Register Call Summary for Register PRM_RSTST

PRCM Register Manual
- DEVICE_PRM Register Summary: [0]

Table 3-757. PRM_RSTTIME

Address Offset	0x0000 0008		
Physical Address	0x4A30 7B08	**Instance**	DEVICE_PRM
Description	Reset duration control. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RSTTIME2								RSTTIME1							

Bits	Field Name	Description	Type	Reset
31:15	RESERVED		R	0x00000
14:10	RSTTIME2	(Power domain) reset duration 2 (number of RM.SYSCLK clock cycles) 0x0: Reserved	RW	0x10
9:0	RSTTIME1	(Global) reset duration 1 (number of Func_32k.clk clock cycles) 0x0: Reserved	RW	0x06

Table 3-758. Register Call Summary for Register PRM_RSTTIME

Reset Management Functional Description
- Reset Domains: [0]
- DSP Subsystem Power-On Reset Sequence: [1] [2]
- DSP Subsystem Software Warm Reset Sequence: [3]
- DSP Subsystem Reset Sequence On Wake-Up Transitions From OSWR RETENTION State: [4]
- Cortex-M3 MPU Subsystem Power-On Reset Sequence: [5] [6]
- Cortex-M3 MPU Subsystem Software Warm Reset Sequence: [7]
- Global Warm Reset Sequence: [8]

Device Low-Power States
- Device Off Mode Wake-Up Sequences: [9]

PRCM Register Manual
- DEVICE_PRM Register Summary: [10]

Table 3-759. PRM_CLKREQCTRL

Address Offset	0x0000 000C		
Physical Address	0x4A30 7B0C	**Instance**	DEVICE_PRM
Description	This register allows controlling the CLKREQ signal towards SCRM.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															CLKREQ_COND

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Bits	Field Name	Description	Type	Reset
31:3	RESERVED		R	0x0000 0000
2:0	CLKREQ_COND	Control upon which condition CLKREQ signal is de-asserted. 0x0: CLKREQ is never de-asserted 0x1: CLKREQ is de-asserted when system clock is not required by any function in the device and if all voltage domains are in OFF state. 0x2: CLKREQ is de-asserted when system clock is not required by any function in the device and if all voltage domains are in RET or OFF state. 0x3: CLKREQ is de-asserted when system clock is not required by any function in the device and if all voltage domains are in SLEEP or RET or OFF state. 0x4: CLKREQ is de-asserted when system clock is not required by any function in the device. This is designed for low-power use-cases using the DPLL cascading scheme (ex: MP3) Read 0x5: Reserved Read 0x6: Reserved Read 0x7: Reserved	RW	0x0

Table 3-760. Register Call Summary for Register PRM_CLKREQCTRL

PRCM Register Manual
- DEVICE_PRM Register Summary: [0]

Table 3-761. PRM_VOLTCTRL

Address Offset	0x0000 0010		
Physical Address	0x4A30 7B10	**Instance**	DEVICE_PRM
Description	This register provides voltage domain management controls.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																VDD_IVA_I2C_DISABLE	VDD_MPU_I2C_DISABLE	VDD_CORE_I2C_DISABLE	RESERVED			VDD_IVA_PRESENCE	VDD_MPU_PRESENCE	RESERVED		AUTO_CTRL_VDD_IVA_L		AUTO_CTRL_VDD_MPU_L		AUTO_CTRL_VDD_CORE_L	

Bits	Field Name	Description	Type	Reset
31:15	RESERVED		R	0x000000
14	VDD_IVA_I2C_DISABLE	This bit allows disabling I2C interface with powerIC for IVA voltage (for debug purpose only). [warm reset insensitive] 0x0: Normal mode: I2C is enabled. 0x1: Debug mode: I2C is disabled.	RW	0

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Bits	Field Name	Description	Type	Reset
13	VDD_MPU_I2C_DISABLE	This bit allows disabling I2C interface with powerIC for MPU voltage (for debug purpose only). [warm reset insensitive] 0x0: Normal mode: I2C is enabled. 0x1: Debug mode: I2C is disabled.	RW	0
12	VDD_CORE_I2C_DISABLE	This bit allows disabling I2C interface with powerIC for CORE voltage (for debug purpose only). [warm reset insensitive] 0x0: Normal mode: I2C is enabled. 0x1: Debug mode: I2C is disabled.	RW	0
11:10	RESERVED		R	0x0
9	VDD_IVA_PRESENCE	This bit control the presence of IVA voltage in device. [warm reset insensitive] 0x0: IVA voltage is not present as an individual voltage: IVA voltage is merged with MPU voltage if VDD_MPU_presence=1. IVA voltage is merged with CORE voltage if VDD_MPU_presence=0. 0x1: IVA voltage is present on the device.	RW	1
8	VDD_MPU_PRESENCE	This bit control the presence of MPU voltage in device. [warm reset insensitive] 0x0: MPU voltage is not present as an individual voltage: MPU voltage is merged with IVA voltage if VDD_IVA_presence=1. MPU voltage is merged with CORE voltage if VDD_IVA_presence=0. 0x1: MPU voltage is present on the device.	RW	1
7:6	RESERVED		R	0x0
5:4	AUTO_CTRL_VDD_IVA_L	This bit field specifies the state to which the hardware can automatically transition the VDD_IVA_L voltage domain. 0x0: Voltage domain transitions are disabled. 0x1: Voltage domain transitions to SLEEP are enabled. 0x2: Voltage domain transitions to RET are enabled. Read 0x3: reserved	RW	0x0
3:2	AUTO_CTRL_VDD_MPU_L	This bit field specifies the state to which the hardware can automatically transition the VDD_MPU_L voltage domain. 0x0: Voltage domain transitions are disabled. 0x1: Voltage domain transitions to SLEEP are enabled. 0x2: Voltage domain transitions to RET are enabled. Read 0x3: reserved	RW	0x0
1:0	AUTO_CTRL_VDD_CORE_L	This bit field specifies the state to which the hardware can automatically transition the VDD_CORE_L voltage domain. 0x0: Voltage domain transitions are disabled. 0x1: Voltage domain transitions to SLEEP are enabled. 0x2: Voltage domain transitions to RET are enabled. Read 0x3: reserved	RW	0x0

Table 3-762. Register Call Summary for Register PRM_VOLTCTRL

Voltage Management Functional Description • VDD_x_L Transitions: [0]
PRCM Register Manual • DEVICE_PRM Register Summary: [1]

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Table 3-763. PRM_PWRREQCTRL

Address Offset	0x0000 0014		
Physical Address	0x4A30 7B14	**Instance**	DEVICE_PRM
Description	This register allows controlling the PWRREQ signal towards power IC.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														PWRREQ_COND	

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1:0	PWRREQ_COND	Control upon which condition from MPU, IVA and CORE voltage domains PWRREQ is de-asserted. 0x0: PWRREQ is never de-asserted 0x1: PWRREQ is de-asserted if all voltage domain are in SLEEP, RET or OFF state. Conversely, PWRREQ is asserted upon any voltage domain entering or staying in ON state. 0x2: PWRREQ is de-asserted if all voltage domain are in RET or OFF state. Conversely, PWRREQ is asserted upon any voltage domain entering or staying in ON or SLEEP state. 0x3: PWRREQ is de-asserted if all voltage domain are in OFF state. Conversely, PWRREQ is asserted upon any voltage domain entering or staying in ON or SLEEP or RET state.	RW	0x0

Table 3-764. Register Call Summary for Register PRM_PWRREQCTRL

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- DEVICE_PRM Register Summary: [0]

Table 3-765. PRM_PSCON_COUNT

Address Offset	0x0000 0018		
Physical Address	0x4A30 7B18	**Instance**	DEVICE_PRM
Description	This register allows controlling 2 parameters for power state controller. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PONOUT_2_PGOODIN_TIME								PCHARGE_TIME							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:8	PONOUT_2_PGOODIN_TIME	The value "NbCycles" set in this field determines the duration of the PONOUT to PGOODIN transition for power domain without DPS. The duration is computed as 8 x NbCycles of system clock cycles.	RW	0x9A
7:0	PCHARGE_TIME	Number of system clock cycles for the SRAM precharge duration.	RW	0x27

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Table 3-766. Register Call Summary for Register PRM_PSCON_COUNT

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- DEVICE_PRM Register Summary: [0]

Table 3-767. PRM_IO_COUNT

Address Offset	0x0000 001C		
Physical Address	0x4A30 7B1C	**Instance**	DEVICE_PRM
Description	This register allows controlling LPDDR2 I/O isolation removal setup. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								ISO_2_ON_TIME							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED		R	0x000000
7:0	ISO_2_ON_TIME	Determines the setup time of the LPDDR2 IOs going out of isolation. Counting on the system clock. Target is 1.5us.	RW	0x3A

Table 3-768. Register Call Summary for Register PRM_IO_COUNT

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- DEVICE_PRM Register Summary: [0]

Table 3-769. PRM_IO_PMCTRL

Address Offset	0x0000 0020		
Physical Address	0x4A30 7B20	**Instance**	DEVICE_PRM
Description	This register allows overriding ISOCLK signal towards I/O pad ring.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															GLOBAL_WUEN	RESERVED						WUCLK_STATUS	WUCLK_CTRL	RESERVED		IOON_STATUS	ISOOVR_EXTEND	RESERVED		ISOCLK_STATUS	ISOCLK_OVERRIDE

Bits	Field Name	Description	Type	Reset
31:17	RESERVED		R	0x0000
16	GLOBAL_WUEN	Global I/O wakeup enable. This is a gating condition to all individual I/O WUEN coming from control module. Gating is done in the Spinner logic. 0x0: All individual I/O WUEN are gated in the Spinner logic (overriden to 0). 0x1: All individual I/O WUEN from control module are going to IOs.	RW	0
15:10	RESERVED		R	0x00
9	WUCLK_STATUS	Gives value of WUCLKOUT signal coming back from I/O pad ring.	R	0

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Bits	Field Name	Description	Type	Reset
8	WUCLK_CTRL	Direct control on WUCLKIN signal to I/O pad ring. 0x0: WUCLKIN signal is driven to 0. I/O wakeup daisy chain is functional as well as I/O whose wakeup feature is enabled. 0x1: WUCLKIN signal is driven to 1. I/O wakeup daisy chain is reset and is latching current pad states and WUEN inputs.	RW	0
7:6	RESERVED		R	0x0
5	IOON_STATUS	Gives the functional status of the I/O ring. Read 0x0: Part or all of the IOs are not in the ON state, that is are in isolation state Read 0x1: All IOs are in the ON state	R	1
4	ISOOVR_EXTEND	Control non-EMIF I/O isolation extension upon a device wakeup from OFF mode. 0x0: Non-EMIF I/O isolation is not extended. "EMIF_ON" I/O transition happens as soon as automatic restore is completed 0x1: Non-EMIF I/O isolation is extended. "EMIF_ON" I/O transition is stalled	RW	0
3:2	RESERVED		R	0x0
1	ISOCLK_STATUS	Gives value of ISOCLKOUT signal coming back from I/O pad ring.	R	0
0	ISOCLK_OVERRIDE	Override control on ISOCLKIN signal to I/O pad ring. Override should be used at boot time only when it is needed to change the mode of an I/O from 1.8-V default mode to 1.2-V mode. When not overriden, this signal is controlled by hardware only. 0x0: ISOCLKIN signal is not overriden. 0x1: ISOCLKIN signal is overriden to active value (1).	RW	0

Table 3-770. Register Call Summary for Register PRM_IO_PMCTRL

Device Low-Power States
- Device Off Mode Wake-Up Sequences: [0]
- I/O Management: [1] [2] [3] [4] [5] [6]
- Software-Controlled I/O Isolation: [7] [8] [9]

PRCM Register Manual
- DEVICE_PRM Register Summary: [10]

Table 3-771. PRM_VOLTSETUP_WARMRESET

Address Offset	0x0000 0024		
Physical Address	0x4A30 7B24	**Instance**	DEVICE_PRM
Description	This register provides bit fields for specifying voltage ramp-up and ramp-down times for PRM managed external regulators. These values are used for VDD_CORE_L domain transitions with OFF state. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						STABLE_PRESCAL		RESERVED		STABLE_COUNT					

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Bits	Field Name	Description	Type	Reset
31:10	RESERVED		R	0x000000
9:8	STABLE_PRESCAL	Determines prescaler for stabilization duration counting. 0x0: Ramp-up counter is incremented every 32 system clock cycles 0x1: Ramp-up counter is incremented every 256 system clock cycles 0x2: Ramp-up counter is incremented every 2048 system clock cycles 0x3: Ramp-up counter is incremented every 16384 system clock cycles	RW	0x0
7:6	RESERVED		R	0x0
5:0	STABLE_COUNT	Determines the stabilization duration of all VDD_xxx_L regulators upon a global warm reset assertion. The duration is computed according to Stable_Prescal.	RW	0x00

Table 3-772. Register Call Summary for Register PRM_VOLTSETUP_WARMRESET

Device Low-Power States
- Device Off Mode Wake-Up Sequences: [0]

PRCM Register Manual
- DEVICE_PRM Register Summary: [1]

Table 3-773. PRM_VOLTSETUP_CORE_OFF

Address Offset	0x0000 0028		
Physical Address	0x4A30 7B28	**Instance**	DEVICE_PRM
Description	This register provides bit fields for specifying voltage ramp-up and ramp-down times for PRM managed external regulators. These values are used for VDD_CORE_L domain transitions with OFF state. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						RAMP_DOWN_PRESCAL		RESERVED		RAMP_DOWN_COUNT						RESERVED						RAMP_UP_PRESCAL		RESERVED		RAMP_UP_COUNT					

Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x00
25:24	RAMP_DOWN_PRESCAL	Determines prescaler for ramp-down duration counting. 0x0: Ramp-down counter is incremented every 64 system clock cycles 0x1: Ramp-down counter is incremented every 256 system clock cycles 0x2: Ramp-down counter is incremented every 512 system clock cycles 0x3: Ramp-down counter is incremented every 2048 system clock cycles	RW	0x0
23:22	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
21:16	RAMP_DOWN_COUNT	Determines the ramp-down duration of VDD_CORE_L regulators. The duration is computed according to Ramp_Down_Prescal.	RW	0x00
15:10	RESERVED		R	0x00
9:8	RAMP_UP_PRESCAL	Determines prescaler for ramp-up duration counting. 0x0: Ramp-up counter is incremented every 64 system clock cycles 0x1: Ramp-up counter is incremented every 256 system clock cycles 0x2: Ramp-up counter is incremented every 512 system clock cycles 0x3: Ramp-up counter is incremented every 2048 system clock cycles	RW	0x0
7:6	RESERVED		R	0x0
5:0	RAMP_UP_COUNT	Determines the ramp-up duration of VDD_CORE_L regulators. The duration is computed according to Ramp_Up_Prescal. At cold reset, PRCM assumes that VDD_CORE_L will be at a valid ON voltage before SYS_NRESPWRON is de-asserted.	RW	0x00

Table 3-774. Register Call Summary for Register PRM_VOLTSETUP_CORE_OFF

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- DEVICE_PRM Register Summary: [0]

Table 3-775. PRM_VOLTSETUP_MPU_OFF

Address Offset	0x0000 002C		
Physical Address	0x4A30 7B2C	**Instance**	DEVICE_PRM
Description	This register provides bit fields for specifying voltage ramp-up and ramp-down times for PRM managed external regulators. These values are used for VDD_MPU_L domain transitions to or from OFF state. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						RAMP_DOWN_PRESCAL		RESERVED		RAMP_DOWN_COUNT						RESERVED						RAMP_UP_PRESCAL		RESERVED		RAMP_UP_COUNT					

Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x00
25:24	RAMP_DOWN_PRESCAL	Determines prescaler for ramp-down duration counting. 0x0: Ramp-down counter is incremented every 64 system clock cycles 0x1: Ramp-down counter is incremented every 256 system clock cycles 0x2: Ramp-down counter is incremented every 512 system clock cycles 0x3: Ramp-down counter is incremented every 2048 system clock cycles	RW	0x0

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Bits	Field Name	Description	Type	Reset
23:22	RESERVED		R	0x0
21:16	RAMP_DOWN_COUNT	Determines the ramp-down duration of VDD_CORE_L regulators. The duration is computed according to Ramp_Down_Prescal.	RW	0x00
15:10	RESERVED		R	0x00
9:8	RAMP_UP_PRESCAL	Determines prescaler for ramp-up duration counting. 0x0: Ramp-up counter is incremented every 64 system clock cycles 0x1: Ramp-up counter is incremented every 256 system clock cycles 0x2: Ramp-up counter is incremented every 512 system clock cycles 0x3: Ramp-up counter is incremented every 2048 system clock cycles	RW	0x0
7:6	RESERVED		R	0x0
5:0	RAMP_UP_COUNT	Determines the ramp-up duration of VDD_CORE_L regulators. The duration is computed according to Ramp_Up_Prescal. At cold reset, PRCM assumes that VDD_CORE_L will be at a valid ON voltage before SYS_NRESPWRON is de-asserted.	RW	0x00

Table 3-776. Register Call Summary for Register PRM_VOLTSETUP_MPU_OFF

PRCM Register Manual
- DEVICE_PRM Register Summary: [0]

Table 3-777. PRM_VOLTSETUP_IVA_OFF

Address Offset	0x0000 0030		
Physical Address	0x4A30 7B30	**Instance**	DEVICE_PRM
Description	This register provides bit fields for specifying voltage ramp-up and ramp-down times for PRM managed external regulators. These values are used for VDD_IVA_L domain transitions to or from OFF state. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							RAMP_DOWN_PRESCAL	RESERVED		RAMP_DOWN_COUNT						RESERVED						RAMP_UP_PRESCAL		RESERVED		RAMP_UP_COUNT					

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Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x00
25:24	RAMP_DOWN_PRESCAL	Determines prescaler for ramp-down duration counting. 0x0: Ramp-down counter is incremented every 64 system clock cycles 0x1: Ramp-down counter is incremented every 256 system clock cycles 0x2: Ramp-down counter is incremented every 512 system clock cycles 0x3: Ramp-down counter is incremented every 2048 system clock cycles	RW	0x0
23:22	RESERVED		R	0x0
21:16	RAMP_DOWN_COUNT	Determines the ramp-down duration of VDD_CORE_L regulators. The duration is computed according to Ramp_Down_Prescal.	RW	0x00
15:10	RESERVED		R	0x00
9:8	RAMP_UP_PRESCAL	Determines prescaler for ramp-up duration counting. 0x0: Ramp-up counter is incremented every 64 system clock cycles 0x1: Ramp-up counter is incremented every 256 system clock cycles 0x2: Ramp-up counter is incremented every 512 system clock cycles 0x3: Ramp-up counter is incremented every 2048 system clock cycles	RW	0x0
7:6	RESERVED		R	0x0
5:0	RAMP_UP_COUNT	Determines the ramp-up duration of VDD_CORE_L regulators. The duration is computed according to Ramp_Up_Prescal. At cold reset, PRCM assumes that VDD_CORE_L will be at a valid ON voltage before SYS_NRESPWRON is de-asserted.	RW	0x00

Table 3-778. Register Call Summary for Register PRM_VOLTSETUP_IVA_OFF

PRCM Register Manual
- DEVICE_PRM Register Summary: [0]

Table 3-779. PRM_VOLTSETUP_CORE_RET_SLEEP

Address Offset	0x0000 0034		
Physical Address	0x4A30 7B34	**Instance**	DEVICE_PRM
Description	This register provides bit fields for specifying voltage ramp-up and ramp-down times for PRM managed external regulators. These values are used for VDD_CORE_L domain transitions between ON and RET or SLEEP state. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						RAMP_DOWN_PRESCAL		RESERVED		RAMP_DOWN_COUNT						RESERVED						RAMP_UP_PRESCAL		RESERVED		RAMP_UP_COUNT					

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Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x00
25:24	RAMP_DOWN_PRESCAL	Determines prescaler for ramp-down duration counting. 0x0: Ramp-down counter is incremented every 64 system clock cycles 0x1: Ramp-down counter is incremented every 256 system clock cycles 0x2: Ramp-down counter is incremented every 512 system clock cycles 0x3: Ramp-down counter is incremented every 2048 system clock cycles	RW	0x0
23:22	RESERVED		R	0x0
21:16	RAMP_DOWN_COUNT	Determines the ramp-down duration of VDD_CORE_L regulators. The duration is computed according to Ramp_Down_Prescal.	RW	0x00
15:10	RESERVED		R	0x00
9:8	RAMP_UP_PRESCAL	Determines prescaler for ramp-up duration counting. 0x0: Ramp-up counter is incremented every 64 system clock cycles 0x1: Ramp-up counter is incremented every 256 system clock cycles 0x2: Ramp-up counter is incremented every 512 system clock cycles 0x3: Ramp-up counter is incremented every 2048 system clock cycles	RW	0x0
7:6	RESERVED		R	0x0
5:0	RAMP_UP_COUNT	Determines the ramp-up duration of VDD_CORE_L regulators. The duration is computed according to Ramp_Up_Prescal.	RW	0x00

Table 3-780. Register Call Summary for Register PRM_VOLTSETUP_CORE_RET_SLEEP

PRCM Register Manual
- DEVICE_PRM Register Summary: [0]

Table 3-781. PRM_VOLTSETUP_MPU_RET_SLEEP

Address Offset	0x0000 0038		
Physical Address	0x4A30 7B38	**Instance**	DEVICE_PRM
Description	This register provides bit fields for specifying voltage ramp-up and ramp-down times for PRM managed external regulators. These values are used for VDD_MPU_L domain transitions between ON and RET or SLEEP state. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								RESERVED		RAMP_DOWN_COUNT						RESERVED								RESERVED		RAMP_UP_COUNT					
						RAMP_DOWN_PRESCAL																RAMP_UP_PRESCAL									

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Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x00
25:24	RAMP_DOWN_PRESCAL	Determines prescaler for ramp-down duration counting. 0x0: Ramp-down counter is incremented every 64 system clock cycles 0x1: Ramp-down counter is incremented every 256 system clock cycles 0x2: Ramp-down counter is incremented every 512 system clock cycles 0x3: Ramp-down counter is incremented every 2048 system clock cycles	RW	0x0
23:22	RESERVED		R	0x0
21:16	RAMP_DOWN_COUNT	Determines the ramp-down duration of VDD_MPU_L regulators. The duration is computed according to Ramp_Down_Prescal.	RW	0x00
15:10	RESERVED		R	0x00
9:8	RAMP_UP_PRESCAL	Determines prescaler for ramp-up duration counting. 0x0: Ramp-up counter is incremented every 64 system clock cycles 0x1: Ramp-up counter is incremented every256 system clock cycles 0x2: Ramp-up counter is incremented every 512 system clock cycles 0x3: Ramp-up counter is incremented every 2048 system clock cycles	RW	0x0
7:6	RESERVED		R	0x0
5:0	RAMP_UP_COUNT	Determines the ramp-up duration of VDD_MPU_L regulators. The duration is computed according to Ramp_Up_Prescal.	RW	0x00

Table 3-782. Register Call Summary for Register PRM_VOLTSETUP_MPU_RET_SLEEP

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- DEVICE_PRM Register Summary: [0]

Table 3-783. PRM_VOLTSETUP_IVA_RET_SLEEP

Address Offset	0x0000 003C		
Physical Address	0x4A30 7B3C	**Instance**	DEVICE_PRM
Description	This register provides bit fields for specifying voltage ramp-up and ramp-down times for PRM managed external regulators. These values are used for VDD_IVA_L domain transitions between ON and RET or SLEEP state. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								RAMP_DOWN_PRESCAL		RESERVED						RAMP_DOWN_COUNT						RESERVED								RAMP_UP_PRESCAL		RESERVED						RAMP_UP_COUNT			

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Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x00
25:24	RAMP_DOWN_PRESCAL	Determines prescaler for ramp-down duration counting. 0x0: Ramp-down counter is incremented every 64 system clock cycles 0x1: Ramp-down counter is incremented every 256 system clock cycles 0x2: Ramp-down counter is incremented every 512 system clock cycles 0x3: Ramp-down counter is incremented every 2048 system clock cycles	RW	0x0
23:22	RESERVED		R	0x0
21:16	RAMP_DOWN_COUNT	Determines the ramp-down duration of VDD_IVA_L regulators. The duration is computed according to Ramp_Down_Prescal.	RW	0x00
15:10	RESERVED		R	0x00
9:8	RAMP_UP_PRESCAL	Determines prescaler for ramp-up duration counting. 0x0: Ramp-up counter is incremented every 64 system clock cycles 0x1: Ramp-up counter is incremented every 256 system clock cycles 0x2: Ramp-up counter is incremented every 512 system clock cycles 0x3: Ramp-up counter is incremented every 2048 system clock cycles	RW	0x0
7:6	RESERVED		R	0x0
5:0	RAMP_UP_COUNT	Determines the ramp-up duration of VDD_IVA_L regulators. The duration is computed according to Ramp_Up_Prescal.	RW	0x00

Table 3-784. Register Call Summary for Register PRM_VOLTSETUP_IVA_RET_SLEEP

PRCM Register Manual
- DEVICE_PRM Register Summary: [0]

Table 3-785. PRM_VP_CORE_CONFIG

Address Offset	0x0000 0040
Physical Address	0x4A30 7B40 **Instance** DEVICE_PRM
Description	This register allows the configuration of the Voltage Processor dedicated to CORE Voltage Domain (VDD_CORE_L).
Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ERROROFFSET								ERRORGAIN								INITVOLTAGE								RESERVED				TIMEOUTEN	INITVDD	FORCEUPDATE	VPENABLE

Bits	Field Name	Description	Type	Reset
31:24	ERROROFFSET	Offset value in the Error to Voltage converter (two's complement number).	RW	0x00
23:16	ERRORGAIN	Gain value in the Error to Voltage converter (two's complement number).	RW	0x00

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Bits	Field Name	Description	Type	Reset
15:8	INITVOLTAGE	Set the initial voltage level of the SMPS. It must be reconfigured before enable the SmartReflex around a new OPP.	RW	0x00
7:4	RESERVED	Write 0's for future compatibility. Read is undefined.	R	0x0
3	TIMEOUTEN	Enable or disable the timeout capability of the Voltage Controller State Machine. 0x0: Timeout is disabled. Loop will wait indefinitely. 0x1: Timeout will occur when TIMEOUT cycles have elapsed.	RW	0
2	INITVDD	Initializes the voltage in the Voltage Processor. 0x0: Reset the initialization bit. 0x1: The positive edge of InitVdd triggers a write of the value in the InitVoltage into the Voltage Processor.	RW	0
1	FORCEUPDATE	Forces an update of the SMPS. 0x0: Reset the force bit. 0x1: The positive edge of ForceUpdate triggers an update of the voltage to the SMPS.	RW	0
0	VPENABLE	Enables or disables the Voltage Processor updates on SR_SInterruptz. 0x0: Disables the Voltage Processor. 0x1: Enables the Voltage Processor.	RW	0

Table 3-786. Register Call Summary for Register PRM_VP_CORE_CONFIG

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- DEVICE_PRM Register Summary: [0]

Table 3-787. PRM_VP_CORE_STATUS

Address Offset	0x0000 0044		
Physical Address	0x4A30 7B44	**Instance**	DEVICE_PRM
Description	This register reflects the idle state of the Voltage Processor dedicated to the CORE Voltage Domain (VDD_CORE_L. This register is read only and automatically updated.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															VPINIDLE

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Write 0's for future compatibility. Read is undefined.	R	0x0000 0000
0	VPINIDLE	CORE Voltage Processor idle status. Read 0x0: The Voltage Processor for CORE is processing. Warm reset sensitive Read 0x1: The Voltage Processor for CORE is in idle state.	R	1

Table 3-788. Register Call Summary for Register PRM_VP_CORE_STATUS

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Table 3-789. PRM_VP_CORE_VLIMITTO

Address Offset	0x0000 0048		
Physical Address	0x4A30 7B48	**Instance**	DEVICE_PRM
Description	This register allows the configuration of the voltage limits and timeout values of the Voltage Processor dedicated to the CORE Voltage Domain (VDD_CORE_L).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VDDMAX								VDDMIN								TIMEOUT															

Bits	Field Name	Description	Type	Reset
31:24	VDDMAX	Defines the maximum voltage supply level.	RW	0x00
23:16	VDDMIN	Defines the minimum voltage supply level.	RW	0x00
15:0	TIMEOUT	Defines Voltage Controller maximum wait time for responses, measured in sysclk cycles.	RW	0x0000

Table 3-790. Register Call Summary for Register PRM_VP_CORE_VLIMITTO

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- DEVICE_PRM Register Summary: [0]

Table 3-791. PRM_VP_CORE_VOLTAGE

Address Offset	0x0000 004C		
Physical Address	0x4A30 7B4C	**Instance**	DEVICE_PRM
Description	This register indicates the current value of the SMPS voltage for the Voltage Processor dedicated to the CORE Voltage Domain (VDD_CORE_L).		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FORCEUPDATEWAIT																								VPVOLTAGE							

Bits	Field Name	Description	Type	Reset
31:8	FORCEUPDATEWAIT	The time voltage processor needs to wait for SMPS to be settled after receiving SMPS acknowledge. This wait only be used during force_update operation.	RW	0x000111
7:0	VPVOLTAGE	Indicates the current SMPS programmed voltage.	R	0x00

Table 3-792. Register Call Summary for Register PRM_VP_CORE_VOLTAGE

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- DEVICE_PRM Register Summary: [0]

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Table 3-793. PRM_VP_CORE_VSTEPMAX

Address Offset	0x0000 0050		
Physical Address	0x4A30 7B50	**Instance**	DEVICE_PRM
Description	This register allows the programming of the maximum voltage step and waiting time of the Voltage Processor dedicated to CORE Voltage Domain (VDD_CORE_L).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								SMPsoftwareAITTIMEMAX																VSTEPMAX							

Bits	Field Name	Description	Type	Reset
31:24	RESERVED	Write 0's for future compatibility. Read is undefined.	R	0x00
23:8	SMPsoftwareAITTIMEMAX	Slew rate for positive voltage step (in number of cycles per step).	RW	0x0000
7:0	VSTEPMAX	Maximum voltage step	RW	0x00

Table 3-794. Register Call Summary for Register PRM_VP_CORE_VSTEPMAX

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- DEVICE_PRM Register Summary: [0]

Table 3-795. PRM_VP_CORE_VSTEPMIN

Address Offset	0x0000 0054		
Physical Address	0x4A30 7B54	**Instance**	DEVICE_PRM
Description	This register allows the programming of the minimum voltage step and waiting time of the Voltage Processor dedicated to the CORE Voltage Domain (VDD_CORE_L).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								SMPsoftwareAITTIMEMIN																VSTEPMIN							

Bits	Field Name	Description	Type	Reset
31:24	RESERVED	Write 0's for future compatibility. Read is undefined.	R	0x00
23:8	SMPsoftwareAITTIMEMIN	Slew rate for negative voltage step (in number of cycles per step).	RW	0x0000
7:0	VSTEPMIN	Minimum voltage step	RW	0x00

Table 3-796. Register Call Summary for Register PRM_VP_CORE_VSTEPMIN

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Table 3-797. PRM_VP_MPU_CONFIG

Address Offset	0x0000 0058		
Physical Address	0x4A30 7B58	**Instance**	DEVICE_PRM
Description	This register allows the configuration of the Voltage Processor dedicated to MPU Voltage Domain (VDD_MPU_L).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ERROROFFSET								ERRORGAIN								INITVOLTAGE								RESERVED				TIMEOUTEN	INITVDD	FORCEUPDATE	VPENABLE

Bits	Field Name	Description	Type	Reset
31:24	ERROROFFSET	Offset value in the Error to Voltage converter (two's complement number).	RW	0x00
23:16	ERRORGAIN	Gain value in the Error to Voltage converter (two's complement number).	RW	0x00
15:8	INITVOLTAGE	Set the initial voltage level of the SMPS. It must be reconfigured before enable the SmartReflex around a new OPP.	RW	0x00
7:4	RESERVED	Write 0's for future compatibility. Read is undefined.	R	0x0
3	TIMEOUTEN	Enable or disable the timeout capability of the Voltage Controller State Machine. 0x0: Timeout is disabled. Loop will wait indefinitely. 0x1: Timeout will occur when TIMEOUT cycles have elapsed.	RW	0
2	INITVDD	Initializes the voltage in the Voltage Processor. 0x0: Reset the initialization bit. 0x1: The positive edge of InitVdd triggers a write of the value in the InitVoltage into the Voltage Processor.	RW	0
1	FORCEUPDATE	Forces an update of the SMPS. 0x0: Reset the force bit. 0x1: The positive edge of ForceUpdate triggers an update of the voltage to the SMPS.	RW	0
0	VPENABLE	Enables or disables the Voltage Processor updates on SR_SInterruptz. 0x0: Disables the Voltage Processor. 0x1: Enables the Voltage Processor.	RW	0

Table 3-798. Register Call Summary for Register PRM_VP_MPU_CONFIG

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Table 3-799. PRM_VP_MPU_STATUS

Address Offset	0x0000 005C		
Physical Address	0x4A30 7B5C	**Instance**	DEVICE_PRM
Description	This register reflects the idle state of the Voltage Processor dedicated to the MPU Voltage Domain (VDD_MPU_L. This register is read only and automatically updated.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															VPINIDLE

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Write 0's for future compatibility. Read is undefined.	R	0x0000 0000
0	VPINIDLE	Voltage Processor 1 idle status. Read 0x0: The Voltage Processor 1 is processing. Read 0x1: The Voltage Processor 1 is in idle state.	R	1

Table 3-800. Register Call Summary for Register PRM_VP_MPU_STATUS

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- DEVICE_PRM Register Summary: [0]

Table 3-801. PRM_VP_MPU_VLIMITTO

Address Offset	0x0000 0060		
Physical Address	0x4A30 7B60	**Instance**	DEVICE_PRM
Description	This register allows the configuration of the voltage limits and timeout values of the Voltage Processor dedicated to the MPU Voltage Domain (VDD_MPU_L).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VDDMAX								VDDMIN								TIMEOUT															

Bits	Field Name	Description	Type	Reset
31:24	VDDMAX	Defines the maximum voltage supply level.	RW	0x00
23:16	VDDMIN	Defines the minimum voltage supply level.	RW	0x00
15:0	TIMEOUT	Defines Voltage Controller maximum wait time for responses, measured in sysclk cycles.	RW	0x0000

Table 3-802. Register Call Summary for Register PRM_VP_MPU_VLIMITTO

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Table 3-803. PRM_VP_MPU_VOLTAGE

Address Offset	0x0000 0064		
Physical Address	0x4A30 7B64	**Instance**	DEVICE_PRM
Description	This register indicates the current value of the SMPS voltage for the Voltage Processor dedicated to the MPU Voltage Domain (VDD_MPU_L).		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FORCEUPDATEWAIT																								VPVOLTAGE							

Bits	Field Name	Description	Type	Reset
31:8	FORCEUPDATEWAIT	The time voltage processor needs to wait for SMPS to be settled after receiving SMPS acknowledge. This wait only be used during force_update operation.	RW	0x000111
7:0	VPVOLTAGE	Indicates the current SMPS programmed voltage.	R	0x00

Table 3-804. Register Call Summary for Register PRM_VP_MPU_VOLTAGE

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- DEVICE_PRM Register Summary: [0]

Table 3-805. PRM_VP_MPU_VSTEPMAX

Address Offset	0x0000 0068		
Physical Address	0x4A30 7B68	**Instance**	DEVICE_PRM
Description	This register allows the programming of the maximum voltage step and waiting time of the Voltage Processor dedicated to MPU Voltage Domain (VDD_MPU_L).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								SMPsoftwareAITTIMEMAX																VSTEPMAX							

Bits	Field Name	Description	Type	Reset
31:24	RESERVED	Write 0's for future compatibility. Read is undefined.	R	0x00
23:8	SMPsoftwareAITTIMEMAX	Slew rate for positive voltage step (in number of cycles per step).	RW	0x0000
7:0	VSTEPMAX	Maximum voltage step	RW	0x00

Table 3-806. Register Call Summary for Register PRM_VP_MPU_VSTEPMAX

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- DEVICE_PRM Register Summary: [0]

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Table 3-807. PRM_VP_MPU_VSTEPMIN

Address Offset	0x0000 006C		
Physical Address	0x4A30 7B6C	**Instance**	DEVICE_PRM
Description	This register allows the programming of the minimum voltage step and waiting time of the Voltage Processor dedicated to the MPU Voltage Domain (VDD_MPU_L).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								SMPsoftwareAITTIMEMIN																VSTEPMIN							

Bits	Field Name	Description	Type	Reset
31:24	RESERVED	Write 0's for future compatibility. Read is undefined.	R	0x00
23:8	SMPsoftwareAITTIMEMIN	Slew rate for negative voltage step (in number of cycles per step).	RW	0x0000
7:0	VSTEPMIN	Minimum voltage step	RW	0x00

Table 3-808. Register Call Summary for Register PRM_VP_MPU_VSTEPMIN

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- DEVICE_PRM Register Summary: [0]

Table 3-809. PRM_VP_IVA_CONFIG

Address Offset	0x0000 0070		
Physical Address	0x4A30 7B70	**Instance**	DEVICE_PRM
Description	This register allows the configuration of the Voltage Processor dedicated to IVAVoltage Domain (VDD_IVA_L).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ERROROFFSET								ERRORGAIN								INITVOLTAGE								RESERVED				TIMEOUTEN	INITVDD	FORCEUPDATE	VPENABLE

Bits	Field Name	Description	Type	Reset
31:24	ERROROFFSET	Offset value in the Error to Voltage converter (two's complement number).	RW	0x00
23:16	ERRORGAIN	Gain value in the Error to Voltage converter (two's complement number).	RW	0x00
15:8	INITVOLTAGE	Set the initial voltage level of the SMPS. It must be reconfigured before enable the SmartReflex around a new OPP.	RW	0x00
7:4	RESERVED	Write 0's for future compatibility. Read is undefined.	R	0x0
3	TIMEOUTEN	Enable or disable the timeout capability of the Voltage Controller State Machine. 0x0: Timeout is disabled. Loop will wait indefinitely. 0x1: Timeout will occur when TIMEOUT cycles have elapsed.	RW	0
2	INITVDD	Initializes the voltage in the Voltage Processor. 0x0: Reset the initialization bit. 0x1: The positive edge of InitVdd triggers a write of the value in the InitVoltage into the Voltage Processor.	RW	0

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Bits	Field Name	Description	Type	Reset
1	FORCEUPDATE	Forces an update of the SMPS. 0x0: Reset the force bit. 0x1: The positive edge of ForceUpdate triggers an update of the voltage to the SMPS.	RW	0
0	VPENABLE	Enables or disables the Voltage Processor updates on SR_SInterruptz. 0x0: Disables the Voltage Processor. 0x1: Enables the Voltage Processor.	RW	0

Table 3-810. Register Call Summary for Register PRM_VP_IVA_CONFIG

PRCM Register Manual
- DEVICE_PRM Register Summary: [0]

Table 3-811. PRM_VP_IVA_STATUS

Address Offset	0x0000 0074		
Physical Address	0x4A30 7B74	**Instance**	DEVICE_PRM
Description	This register reflects the idle state of the Voltage Processor dedicated to the MPU Voltage Domain (VDD_IVA_L. This register is read only and automatically updated.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															VPINIDLE

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Write 0's for future compatibility. Read is undefined.	R	0x0000 0000
0	VPINIDLE	Voltage Processor 1 idle status. Read 0x0: The Voltage Processor 1 is processing. Read 0x1: The Voltage Processor 1 is in idle state.	R	1

Table 3-812. Register Call Summary for Register PRM_VP_IVA_STATUS

PRCM Register Manual
- DEVICE_PRM Register Summary: [0]

Table 3-813. PRM_VP_IVA_VLIMITTO

Address Offset	0x0000 0078		
Physical Address	0x4A30 7B78	**Instance**	DEVICE_PRM
Description	This register allows the configuration of the voltage limits and timeout values of the Voltage Processor dedicated to the IVA Voltage Domain (VDD_IVA_L).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VDDMAX								VDDMIN								TIMEOUT															

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Bits	Field Name	Description	Type	Reset
31:24	VDDMAX	Defines the maximum voltage supply level.	RW	0x00
23:16	VDDMIN	Defines the minimum voltage supply level.	RW	0x00
15:0	TIMEOUT	Defines Voltage Controller maximum wait time for responses, measured in sysclk cycles.	RW	0x0000

Table 3-814. Register Call Summary for Register PRM_VP_IVA_VLIMITTO

PRCM Register Manual
- DEVICE_PRM Register Summary: [0]

Table 3-815. PRM_VP_IVA_VOLTAGE

Address Offset	0x0000 007C		
Physical Address	0x4A30 7B7C	**Instance**	DEVICE_PRM
Description	This register indicates the current value of the SMPS voltage for the Voltage Processor dedicated to the IVA Voltage Domain (VDD_IVA_L).		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FORCEUPDATEWAIT																								VPVOLTAGE							

Bits	Field Name	Description	Type	Reset
31:8	FORCEUPDATEWAIT	The time voltage processor needs to wait for SMPS to be settled after receiving SMPS acknowledge. This wait only be used during force_update operation.	RW	0x000111
7:0	VPVOLTAGE	Indicates the current SMPS programmed voltage.	R	0x00

Table 3-816. Register Call Summary for Register PRM_VP_IVA_VOLTAGE

PRCM Register Manual
- DEVICE_PRM Register Summary: [0]

Table 3-817. PRM_VP_IVA_VSTEPMAX

Address Offset	0x0000 0080		
Physical Address	0x4A30 7B80	**Instance**	DEVICE_PRM
Description	This register allows the programming of the maximum voltage step and waiting time of the Voltage Processor dedicated to IVA Voltage Domain (VDD_IVA_L).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								SMPsoftwareAITTIMEMAX																VSTEPMAX							

Bits	Field Name	Description	Type	Reset
31:24	RESERVED	Write 0's for future compatibility. Read is undefined.	R	0x00
23:8	SMPsoftwareAITTIMEMAX	Slew rate for positive voltage step (in number of cycles per step).	RW	0x0000
7:0	VSTEPMAX	Maximum voltage step	RW	0x00

Table 3-818. Register Call Summary for Register PRM_VP_IVA_VSTEPMAX

PRCM Register Manual
- DEVICE_PRM Register Summary: [0]

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Table 3-819. PRM_VP_IVA_VSTEPMIN

Address Offset	0x0000 0084		
Physical Address	0x4A30 7B84	**Instance**	DEVICE_PRM
Description	This register allows the programming of the minimum voltage step and waiting time of the Voltage Processor dedicated to the IVA Voltage Domain (VDD_IVA_L).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								SMPsoftwareAITTIMEMIN																VSTEPMIN							

Bits	Field Name	Description	Type	Reset
31:24	RESERVED	Write 0's for future compatibility. Read is undefined.	R	0x00
23:8	SMPsoftwareAITTIMEMIN	Slew rate for negative voltage step (in number of cycles per step).	RW	0x0000
7:0	VSTEPMIN	Minimum voltage step	RW	0x00

Table 3-820. Register Call Summary for Register PRM_VP_IVA_VSTEPMIN

PRCM Register Manual
- DEVICE_PRM Register Summary: [0]

Table 3-821. PRM_VC_SMPS_SA

Address Offset	0x0000 0088		
Physical Address	0x4A30 7B88	**Instance**	DEVICE_PRM
Description	This register allows the setting of the I2C slave address of the Power IC device. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								SA_VDD_MPU_L								RESERVED	SA_VDD_IVA_L							RESERVED	SA_VDD_CORE_L						

Bits	Field Name	Description	Type	Reset
31:23	RESERVED		R	0x000
22:16	SA_VDD_MPU_L	Set the I2C slave address value for the third (if any) Power IC device.	RW	0x00
15	RESERVED		R	0
14:8	SA_VDD_IVA_L	Set the I2C slave address value for the second (if any) Power IC device.	RW	0x00
7	RESERVED	Write 0's for future compatibility. Read is undefined.	R	0
6:0	SA_VDD_CORE_L	Set the I2C slave address value for the first Power IC device.	RW	0x00

Table 3-822. Register Call Summary for Register PRM_VC_SMPS_SA

PRCM Module Programming Guide
- Global Initialization: [0]

PRCM Register Manual
- DEVICE_PRM Register Summary: [1]

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Table 3-823. PRM_VC_VAL_SMPS_RA_VOL

Address Offset	0x0000 008C		
Physical Address	0x4A30 7B8C	**Instance**	DEVICE_PRM
Description	This register allows the setting of the voltage configuration register address for the VDD channels. [warm reset insensitive]		
Type	RW		

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
RESERVED	VOLRA_VDD_MPU_L	VOLRA_VDD_IVA_L	VOLRA_VDD_CORE_L

Bits	Field Name	Description	Type	Reset
31:24	RESERVED	Write 0's for future compatibility. Read is undefined.	R	0x00
23:16	VOLRA_VDD_MPU_L	Voltage configuration register address value for VDD_MPU_L channel	RW	0x00
15:8	VOLRA_VDD_IVA_L	Voltage configuration register address value for VDD_IVA_L channel (if VDD_IVA_L source is placed in same chip as VDD_CORE_L source and have different voltage configuration register)	RW	0x00
7:0	VOLRA_VDD_CORE_L	Voltage configuration register address value for the VDD_CORE_L channel (if VDD_CORE_L source is placed in same chip as VDD_MPU_L source and has different voltage configuration register)	RW	0x00

Table 3-824. Register Call Summary for Register PRM_VC_VAL_SMPS_RA_VOL

PRCM Module Programming Guide
- Global Initialization: [0]

PRCM Register Manual
- DEVICE_PRM Register Summary: [1]

Table 3-825. PRM_VC_VAL_SMPS_RA_CMD

Address Offset	0x0000 0090		
Physical Address	0x4A30 7B90	**Instance**	DEVICE_PRM
Description	Command (ON/ON-Low-Power/Retention/OFF) configuration register address values for the VDD channels (if used SMPS chips have different command configuration register than voltage configuration register) [warm reset insensitive]		
Type	RW		

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
RESERVED	CMDRA_VDD_MPU_L	CMDRA_VDD_IVA_L	CMDRA_VDD_CORE_L

Bits	Field Name	Description	Type	Reset
31:24	RESERVED	Write 0's for future compatibility. Read is undefined.	R	0x00
23:16	CMDRA_VDD_MPU_L	Command (ON/ON-Low-Power /Retention/OFF) configuration register address value for VDD_MPU_L channel	RW	0x00
15:8	CMDRA_VDD_IVA_L	Command (ON/ON-Low-Power /Retention/OFF) configuration register address value for VDD_IVA_L channel (if VDD_IVA_L source has different command configuration register than voltage VDD_CORE_L)	RW	0x00
7:0	CMDRA_VDD_CORE_L	Command (ON/ON-Low-Power /Retention/OFF) configuration register address value for VDD_CORE_L channel (if VDD_CORE_L source has different command configuration register than voltage VDD_MPU_L)	RW	0x00

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Table 3-826. Register Call Summary for Register PRM_VC_VAL_SMPS_RA_CMD

PRCM Module Programming Guide
- Global Initialization: [0]

PRCM Register Manual
- DEVICE_PRM Register Summary: [1]

Table 3-827. PRM_VC_VAL_CMD_VDD_CORE_L

Address Offset	0x0000 0094
Physical Address	0x4A30 7B94 **Instance** DEVICE_PRM
Description	This register allows the setting of the ON/ON-Low-Power/Retention/OFF command values for VDD_CORE_L channel. [warm reset insensitive]
Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ON								ONLP								RET								OFF							

Bits	Field Name	Description	Type	Reset
31:24	ON	Set the ON command value.	RW	0x00
23:16	ONLP	Set the ON-Low-Power command value.	RW	0x00
15:8	RET	Set the RET command value.	RW	0x00
7:0	OFF	Set the OFF command value.	RW	0x00

Table 3-828. Register Call Summary for Register PRM_VC_VAL_CMD_VDD_CORE_L

PRCM Register Manual
- DEVICE_PRM Register Summary: [0]

Table 3-829. PRM_VC_VAL_CMD_VDD_MPU_L

Address Offset	0x0000 0098
Physical Address	0x4A30 7B98 **Instance** DEVICE_PRM
Description	This register allows the setting of the ON/ON-Low-Power/Retention/OFF command values for VDD_MPU_L channel. [warm reset insensitive]
Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ON								ONLP								RET								OFF							

Bits	Field Name	Description	Type	Reset
31:24	ON	Set the ON command value.	RW	0x00
23:16	ONLP	Set the ON-Low-Power command value.	RW	0x00
15:8	RET	Set the RET command value.	RW	0x00
7:0	OFF	Set the OFF command value.	RW	0x00

Table 3-830. Register Call Summary for Register PRM_VC_VAL_CMD_VDD_MPU_L

PRCM Register Manual
- DEVICE_PRM Register Summary: [0]

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Table 3-831. PRM_VC_VAL_CMD_VDD_IVA_L

Address Offset	0x0000 009C		
Physical Address	0x4A30 7B9C	**Instance**	DEVICE_PRM
Description	This register allows the setting of the ON/ON-Low-Power/Retention/OFF command values for VDD_IVA_L channel. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ON								ONLP								RET								OFF							

Bits	Field Name	Description	Type	Reset
31:24	ON	Set the ON command value.	RW	0x00
23:16	ONLP	Set the ON-Low-Power command value.	RW	0x00
15:8	RET	Set the RET command value.	RW	0x00
7:0	OFF	Set the OFF command value.	RW	0x00

Table 3-832. Register Call Summary for Register PRM_VC_VAL_CMD_VDD_IVA_L

PRCM Register Manual
- DEVICE_PRM Register Summary: [0]

Table 3-833. PRM_VC_VAL_BYPASS

Address Offset	0x0000 00A0		
Physical Address	0x4A30 7BA0	**Instance**	DEVICE_PRM
Description	Bypass data values register used for bypass command channel to send other configuration information (other then voltage configuration parameters) for SMPS chips which have no other configuration interface then this I2C interface. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							VALID	DATA								REGADDR								RESERVED	SLAVEADDR						

Bits	Field Name	Description	Type	Reset
31:25	RESERVED		R	0x00
24	VALID	This bit validates the bypass command. It is automatically cleared by hardware either after getting the acknowledge back from the SMPS or if an error occured. Read 0x0: The last command send has been acknowledged 0x1: Pending command is being process	RW WSpecial	0
23:16	DATA	Data to send to the Power IC device.	RW	0x00
15:8	REGADDR	Set the address of Power IC device register to configure.	RW	0x00
7	RESERVED		R	0
6:0	SLAVEADDR	Set the I2C slave address value.	RW	0x00

Table 3-834. Register Call Summary for Register PRM_VC_VAL_BYPASS

PRCM Register Manual
- DEVICE_PRM Register Summary: [0]

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Table 3-835. PRM_VC_CFG_CHANNEL

Address Offset	0x0000 00A4		
Physical Address	0x4A30 7BA4	**Instance**	DEVICE_PRM
Description	This register allows the configuration pointers for both VDD channels. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											RACEN_VDD_MPU_L	RAC_VDD_MPU_L	RAV_VDD_MPU_L	CMD_VDD_MPU_L	SA_VDD_MPU_L	RESERVED			CMD_VDD_IVA_L	RACEN_VDD_IVA_L	RAC_VDD_IVA_L	RAV_VDD_IVA_L	SA_VDD_IVA_L	RESERVED			CMD_VDD_CORE_L	RACEN_VDD_CORE_L	RAC_VDD_CORE_L	RAV_VDD_CORE_L	SA_VDD_CORE_L

Bits	Field Name	Description	Type	Reset
31:21	RESERVED		R	0x000
20	RACEN_VDD_MPU_L	Enable bit for usage of RAC_VDD_MPU_L 0x0: VDD_MPU_L channel uses VOLRA values for register address of VFSM-s commands. VFSM-s commands goes also to voltage configuration register. 0x1: VDD_MPU_L channel uses CMDRA values for register address of VFSM-s commands. VFSM-s commands goes to different command configuration register.	RW	0
19	RAC_VDD_MPU_L	Command (ON/ON-Low-Power/Retention/OFF) configuration register address pointer for VDD_MPU_L channel 0x0: Select CMDRA_VDD_CORE_L for VDD_MPU_L channel 0x1: Select CMDRA_VDD_MPU_L for VDD_MPU_L channel	RW	0
18	RAV_VDD_MPU_L	Voltage configuration register address pointer for VDD_MPU_L channel. 0x0: Select VOLRA_VDD_CORE_L for VDD_MPU_L channel 0x1: Select VOLRA_VDD_MPU_L for VDD_MPU_L channel	RW	0
17	CMD_VDD_MPU_L	Command values (ON/ON-Low-Power/Retention/OFF voltage values) set selection for VDD_MPU_L channel 0x0: VDD_MPU_L channel use VC_VAL_CMD_VDD_CORE_L set for command values 0x1: VDD_MPU_L channel use VC_VAL_CMD_VDD_MPU_L set for command values	RW	0
16	SA_VDD_MPU_L	Slave address pointer for VDD_MPU_L channel. 0x0: Select SA_VDD_CORE_L for VDD_MPU_L channel 0x1: Select SA_VDD_MPU_L for VDD_MPU_L channel	RW	0
15:13	RESERVED		R	0x0
12	CMD_VDD_IVA_L	Command values (ON/ON-Low-Power/Retention/OFF voltage values) set selection for VDD_IVA_L channel 0x0: VDD_IVA_L channel use VC_VAL_CMD_VDD_CORE_L set for command values 0x1: VDD_IVA_L channel use VC_VAL_CMD_VDD_IVA_L set for command values	RW	0

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Bits	Field Name	Description	Type	Reset
11	RACEN_VDD_IVA_L	Enable bit for usage of RAC_VDD_IVA_L 0x0: VDD_IVA_L channel uses VOLRA values for register address of VFSM-s commands. VFSM-s commands goes also to voltage configuration register. 0x1: VDD_IVA_L channel uses CMDRA values for register address of VFSM-s commands. VFSM-s commands goes to different command configuration register.	RW	0
10	RAC_VDD_IVA_L	Command (ON/ON-Low-Power/Retention/OFF) configuration register address pointer for VDD_IVA_L channel 0x0: Select CMDRA_VDD_CORE_L for VDD_IVA_L channel 0x1: Select CMDRA_VDD_IVA_L for VDD_IVA_L channel	RW	0
9	RAV_VDD_IVA_L	Voltage configuration register address pointer for VDD_IVA_L channel. 0x0: Select VOLRA_VDD_CORE_L for VDD_IVA_L channel 0x1: Select VOLRA_VDD_IVA_L for VDD_IVA_L channel	RW	0
8	SA_VDD_IVA_L	Slave address pointer for VDD_IVA_L channel. 0x0: Select SA_VDD_CORE_L for VDD_IVA_L channel 0x1: Select SA_VDD_IVA_L for VDD_IVA_L channel	RW	0
7:5	RESERVED		R	0x0
4	CMD_VDD_CORE_L	Command values (ON/ON-Low-Power/Retention/OFF voltage values) set selection for VDD_CORE_L channel (This bit has no influence on VDD_CORE_L channel)	RW	0
3	RACEN_VDD_CORE_L	Enable bit for usage of RAC_VDD_CORE_L. 0x0: VDD_CORE_L channel use VOLRA values for register address of VFSM-s commands. VFSM-s commands goes also to voltage configuration register. 0x1: VDD_CORE_L channel use CMDRA values for register address of VFSM-s commands. VFSM-s commands goes to different command configuration register.	RW	0
2	RAC_VDD_CORE_L	Command (ON/ON-Low-Power/Retention/OFF) configuration register address pointer for VDD_CORE_L channel. 0x0: Select CMDRA_VDD_MPU_L for the VDD_CORE_L channel. 0x1: Select CMDRA_VDD_CORE_L for the VDD_CORE_L channel.	RW	0
1	RAV_VDD_CORE_L	Voltage configuration register address pointer for VDD_CORE_L channel. 0x0: Select VOLRA_VDD_MPU_L for the VDD_CORE_L channel. 0x1: Select VOLRA_VDD_CORE_L for the VDD_CORE_L channel.	RW	0
0	SA_VDD_CORE_L	Slave address pointer for VDD_CORE_L channel. 0x0: Select SA_VDD_MPU_L for the VDD_CORE_L channel. 0x1: Select SA_VDD_CORE_L for the VDD_CORE_L channel.	RW	0

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Table 3-836. Register Call Summary for Register PRM_VC_CFG_CHANNEL

PRCM Module Programming Guide
- Global Initialization: [0] [1] [2] [3] [4]

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- DEVICE_PRM Register Summary: [5]

Table 3-837. PRM_VC_CFG_I2C_MODE

Address Offset	0x0000 00A8		
Physical Address	0x4A30 7BA8	**Instance**	DEVICE_PRM
Description	I^2C configuration register. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								DFILTEREN	RESERVED	SRMODEEN	HSMODEEN	HSMCODE			

Bits	Field Name	Description	Type	Reset
31:7	RESERVED		R	0x0000000
6	DFILTEREN	This field enables double filter procedure for I^2C input lines 0x0: I^2C bus digital filter rejects all glitches smaller than 1 sytem clock cycle 0x1: I^2C bus digital filter rejects all glitches smaller than 2 sytem clock cycles	RW	0
5	RESERVED		R	0
4	SRMODEEN	Enables the I^2C repeated start operation mode. (Effect of holding the SCL and SDA lines low, in effect blocking the I^2C bus from losing arbitration between repeated start points). Use of this feature results from a trade-off between speed and power consumption of I^2C interface. 0x0: Disables the repeated start operation mode 0x1: Enables the repeated start operation mode	RW	1
3	HSMODEEN	Enables I^2C bus high-speed mode. 0x0: Disables the I^2C high-speed mode 0x1: Enables the I^2C high-speed mode	RW	1
2:0	HSMCODE	Master code value for I^2C high-speed preamble transmission.	RW	0x0

Table 3-838. Register Call Summary for Register PRM_VC_CFG_I2C_MODE

PRCM Module Programming Guide
- Global Initialization: [0] [1] [2] [3]

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- DEVICE_PRM Register Summary: [4]

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Table 3-839. PRM_VC_CFG_I2C_CLK

Address Offset	0x0000 00AC		
Physical Address	0x4A30 7BAC	**Instance**	DEVICE_PRM
Description	I2C Interface clock configuration parameters. [warm reset insensitive]		
Type	RW		

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
HSSCLL	HSSCLH	SCLL	SCLH

Bits	Field Name	Description	Type	Reset
31:24	HSSCLL	Number of the system clock cycles, necessary to count the low period of the I2C clock signal, when the I2C interface runs in high-speed mode of operation. The value of the bit field is automatically increased by 7.	RW	0x00
23:16	HSSCLH	Number of the system clock cycles, necessary to count the high period of the I2C clock signal, when the I2C interface runs in high-speed mode of operation. The value of the bit field is automatically increased by 5.	RW	0x00
15:8	SCLL	Number of the system clock cycles, necessary to count the low period of the I2C clock signal, when the I2C interface runs in fast mode of operation. The value of the bit field is automatically increased by 7.	RW	0x00
7:0	SCLH	Number of the system clock cycles, necessary to count the high period of the I2C clock signal, when the I2C interface runs in fast mode of operation. The value of the bit field is automatically increased by 5.	RW	0x00

Table 3-840. Register Call Summary for Register PRM_VC_CFG_I2C_CLK

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- DEVICE_PRM Register Summary: [0]

Table 3-841. PRM_SRAM_COUNT

Address Offset	0x0000 00B0		
Physical Address	0x4A30 7BB0	**Instance**	DEVICE_PRM
Description	Common setup for SRAM LDO transition counters. Applies to all voltage domains. [warm reset insensitive]		
Type	RW		

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6	5 4 3 2 1 0
STARTUP_COUNT	SLPCNT_VALUE	VSETUPCNT_VALUE	RESERVED	PCHARGECNT_VALUE

Bits	Field Name	Description	Type	Reset
31:24	STARTUP_COUNT	Determines the start-up duration of SRAM and ABB LDO. The duration is computed as 16 x NbCycles of system clock cycles. Target is 50us.	RW	0x78
23:16	SLPCNT_VALUE	Delay between retention/off assertion of last SRAM bank and SRAMALLRET signal to LDO is driven high. Counting on system clock. Target is 2us.	RW	0x00
15:8	VSETUPCNT_VALUE	SRAM LDO rampup time from retention to active mode. The duration is computed as 8 x NbCycles of system clock cycles. Target is 30us.	RW	0x00
7:6	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
5:0	PCHARGECNT_VALUE	Delay between de-assertion of standby_rta_ret_on and standby_rta_ret_good. Counting on system clock. Target is 600ns.	RW	0x17

Table 3-842. Register Call Summary for Register PRM_SRAM_COUNT

PRCM Register Manual

- DEVICE_PRM Register Summary: [0]

Table 3-843. PRM_SRAM_WKUP_SETUP

Address Offset	0x0000 00B4		
Physical Address	0x4A30 7BB4	**Instance**	DEVICE_PRM
Description	Setup of memory in WKUP voltage domain. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															DISABLE_RTA_EXPORT

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	DISABLE_RTA_EXPORT	Control for HD memory RTA feature. After PowerOn reset and Efuse sensing, this bit field is automatically loaded with an Efuse value from control module. Bit field remains writable after this. 0x0: HD memory RTA feature is enabled 0x1: HD memory RTA feature is disabled	RW WSpecial	0

Table 3-844. Register Call Summary for Register PRM_SRAM_WKUP_SETUP

PRCM Register Manual

- DEVICE_PRM Register Summary: [0]

Table 3-845. PRM_LDO_SRAM_CORE_SETUP

Address Offset	0x0000 00B8		
Physical Address	0x4A30 7BB8	**Instance**	DEVICE_PRM
Description	Setup of the SRAM LDO for CORE voltage domain. [warm reset insensitive]		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							AIPOFF	ENFUNC5	ENFUNC4	ENFUNC3_EXPORT	ENFUNC2_EXPORT	ENFUNC1_EXPORT	ABBOFF_SLEEP_EXPORT	ABBOFF_ACT_EXPORT	DISABLE_RTA_EXPORT

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	AIPOFF	Override on AIPOFF input of SRAM LDO. 0x0: AIPOFF signal is not overriden 0x1: AIPOFF signal is overriden to 1. Corresponding SRAM LDO is disabled and in HZ mode.	RW	0
7	ENFUNC5	ENFUNC5 input of SRAM LDO. 0x0: Active to retention is a one step transfer 0x1: Active to retention is a two steps transfer	RW	0
6	ENFUNC4	ENFUNC4 input of SRAM LDO. 0x0: One external clock is supplied 0x1: No external clock is supplied	RW	0
5	ENFUNC3_EXPORT	ENFUNC3 input of SRAM LDO. After PowerOn reset and Efuse sensing, this bit field is automatically loaded with an Efuse value from control module. Bit field remains writable after this. 0x0: Sub regulation is disabled 0x1: Sub regulation is enabled	RW WSpecial	0
4	ENFUNC2_EXPORT	ENFUNC2 input of SRAM LDO. After PowerOn reset and Efuse sensing, this bit field is automatically loaded with an Efuse value from control module. Bit field remains writable after this. 0x0: External cap is used 0x1: External cap is not used	RW WSpecial	0
3	ENFUNC1_EXPORT	ENFUNC1 input of SRAM LDO. After PowerOn reset and Efuse sensing, this bit field is automatically loaded with an Efuse value from control module. Bit field remains writable after this. 0x0: Short circuit protection is disabled 0x1: Short circuit protection is enabled	RW WSpecial	0
2	ABBOFF_SLEEP_EXPORT	Determines whether SRAMNWA is supplied by VDDS or VDDAR during deep-sleep. After PowerOn reset and Efuse sensing, this bit field is automatically loaded with an Efuse value from control module. Bit field remains writable after this. 0x0: SRAMNWA supplied with VDDS 0x1: SRAMNWA supplied with VDDAR	RW WSpecial	0
1	ABBOFF_ACT_EXPORT	Determines whether SRAMNWA is supplied by VDDS or VDDAR during active mode. After PowerOn reset and Efuse sensing, this bit field is automatically loaded with an Efuse value from control module. Bit field remains writable after this. 0x0: SRAMNWA supplied with VDDS 0x1: SRAMNWA supplied with VDDAR	RW WSpecial	0

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Bits	Field Name	Description	Type	Reset
0	DISABLE_RTA_EXPORT	Control for HD memory RTA feature. After PowerOn reset and Efuse sensing, this bit field is automatically loaded with an Efuse value from control module. Bit field remains writable after this. 0x0: HD memory RTA feature is enabled 0x1: HD memory RTA feature is disabled	RW WSpecial	0

Table 3-846. Register Call Summary for Register PRM_LDO_SRAM_CORE_SETUP

PRCM Register Manual
- DEVICE_PRM Register Summary: [0]

Table 3-847. PRM_LDO_SRAM_CORE_CTRL

Address Offset	0x0000 00BC		
Physical Address	0x4A30 7BBC	**Instance**	DEVICE_PRM
Description	Control and status of the SRAM LDO for CORE voltage domain. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						SRAM_IN_TRANSITION	SRAMLDO_STATUS	RESERVED							RETMODE_ENABLE

Bits	Field Name	Description	Type	Reset
31:10	RESERVED		R	0x000000
9	SRAM_IN_TRANSITION	Status indicating SRAM LDO state machine state. Read 0x0: SRAM LDO state machine is stable Read 0x1: SRAM LDO state machine is in transition state	R	0
8	SRAMLDO_STATUS	SRAMLDO status Read 0x0: SRAMLDO is in ACTIVE mode. Read 0x1: SRAMLDO is on RETENTION mode.	R	0
7:1	RESERVED		R	0x00
0	RETMODE_ENABLE	Control if the SRAM LDO retention mode is used or not. 0x0: SRAM LDO is not allowed to go to RET mode 0x1: SRAM LDO go to RET mode when all memory of voltage domain are OFF or RET	RW	0

Table 3-848. Register Call Summary for Register PRM_LDO_SRAM_CORE_CTRL

PRCM Register Manual
- DEVICE_PRM Register Summary: [0]

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Table 3-849. PRM_LDO_SRAM_MPU_SETUP

Address Offset	0x0000 00C0		
Physical Address	0x4A30 7BC0	**Instance**	DEVICE_PRM
Description	Setup of the SRAM LDO for MPU voltage domain. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							AIPOFF	ENFUNC5	ENFUNC4	ENFUNC3_ECPORT	ENFUNC2_EXPORT	ENFUNC1_EXPORT	ABBOFF_SLEEP_EXPORT	ABBOFF_ACT_EXPORT	DISABLE_RTA_EXPORT

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	AIPOFF	Override on AIPOFF input of SRAM LDO. 0x0: AIPOFF signal is not overriden 0x1: AIPOFF signal is overriden to 1. Corresponding SRAM LDO is disabled and in HZ mode.	RW	0
7	ENFUNC5	ENFUNC5 input of SRAM LDO. 0x0: Active to retention is a one step transfer 0x1: Active to retention is a two steps transfer	RW	0
6	ENFUNC4	ENFUNC4 input of SRAM LDO. 0x0: One external clock is supplied 0x1: No external clock is supplied	RW	0
5	ENFUNC3_EXPORT	ENFUNC3 input of SRAM LDO. After PowerOn reset and Efuse sensing, this bit field is automatically loaded with an Efuse value from control module. Bit field remains writable after this. 0x0: Sub regulation is disabled 0x1: Sub regulation is enabled	RW	0
4	ENFUNC2_EXPORT	ENFUNC2 input of SRAM LDO. After PowerOn reset and Efuse sensing, this bit field is automatically loaded with an Efuse value from control module. Bit field remains writable after this. 0x0: External cap is used 0x1: External cap is not used	RW WSpecial	0
3	ENFUNC1_EXPORT	ENFUNC1 input of SRAM LDO. After PowerOn reset and Efuse sensing, this bit field is automatically loaded with an Efuse value from control module. Bit field remains writable after this. 0x0: Short circuit protection is disabled 0x1: Short circuit protection is enabled	RW	0
2	ABBOFF_SLEEP_EXPORT	Determines whether SRAMNWA is supplied by VDDS or VDDAR during deep-sleep. After PowerOn reset and Efuse sensing, this bit field is automatically loaded with an Efuse value from control module. Bit field remains writable after this. 0x0: SRAMNWA supplied with VDDS 0x1: SRAMNWA supplied with VDDAR	RW WSpecial	0

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Bits	Field Name	Description	Type	Reset
1	ABBOFF_ACT_EXPORT	Determines whether SRAMNWA is supplied by VDDS or VDDAR during active mode. After PowerOn reset and Efuse sensing, this bit field is automatically loaded with an Efuse value from control module. Bit field remains writable after this. 0x0: SRAMNWA supplied with VDDS 0x1: SRAMNWA supplied with VDDAR	RW WSpecial	0
0	DISABLE_RTA_EXPORT	Control for HD memory RTA feature. After PowerOn reset and Efuse sensing, this bit field is automatically loaded with an Efuse value from control module. Bit field remains writable after this. 0x0: HD memory RTA feature is enabled 0x1: HD memory RTA feature is disabled	RW WSpecial	0

Table 3-850. Register Call Summary for Register PRM_LDO_SRAM_MPU_SETUP

PRCM Register Manual
- DEVICE_PRM Register Summary: [0]

Table 3-851. PRM_LDO_SRAM_MPU_CTRL

Address Offset	0x0000 00C4		
Physical Address	0x4A30 7BC4	**Instance**	DEVICE_PRM
Description	Control and status of the SRAM LDO for MPU voltage domain. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						SRAM_IN_TRANSITION	SRAMLDO_STATUS	RESERVED							RETMODE_ENABLE

Bits	Field Name	Description	Type	Reset
31:10	RESERVED		R	0x000000
9	SRAM_IN_TRANSITION	Status indicating SRAM LDO state machine state. Read 0x0: SRAM LDO state machine is stable Read 0x1: SRAM LDO state machine is in transition state	R	0
8	SRAMLDO_STATUS	SRAMLDO status Read 0x0: SRAMLDO is in ACTIVE mode. Read 0x1: SRAMLDO is on RETENTION mode.	R	0
7:1	RESERVED		R	0x00
0	RETMODE_ENABLE	Control if the SRAM LDO retention mode is used or not. 0x0: SRAM LDO is not allowed to go to RET mode 0x1: SRAM LDO go to RET mode when all memory of voltage domain are OFF or RET	RW	0

Table 3-852. Register Call Summary for Register PRM_LDO_SRAM_MPU_CTRL

PRCM Register Manual
- DEVICE_PRM Register Summary: [0]

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Table 3-853. PRM_LDO_SRAM_IVA_SETUP

Address Offset	0x0000 00C8		
Physical Address	0x4A30 7BC8	**Instance**	DEVICE_PRM
Description	Setup of the SRAM LDO for IVA voltage domain. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							AIPOFF	ENFUNC5	ENFUNC4	ENFUNC3_EXPORT	ENFUNC2_EXPORT	ENFUNC1_EXPORT	ABBOFF_SLEEP_EXPORT	ABBOFF_ACT_EXPORT	DISABLE_RTA_EXPORT

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	AIPOFF	Override on AIPOFF input of SRAM LDO. 0x0: AIPOFF signal is not overriden 0x1: AIPOFF signal is overriden to 1. Corresponding SRAM LDO is disabled and in HZ mode.	RW	0
7	ENFUNC5	ENFUNC5 input of SRAM LDO. 0x0: Active to retention is a one step transfer 0x1: Active to retention is a two steps transfer	RW	0
6	ENFUNC4	ENFUNC4 input of SRAM LDO. 0x0: One external clock is supplied 0x1: No external clock is supplied	RW	0
5	ENFUNC3_EXPORT	ENFUNC3 input of SRAM LDO. After PowerOn reset and Efuse sensing, this bit field is automatically loaded with an Efuse value from control module. Bit field remains writable after this. 0x0: Sub regulation is disabled 0x1: Sub regulation is enabled	RW	0
4	ENFUNC2_EXPORT	ENFUNC2 input of SRAM LDO. After PowerOn reset and Efuse sensing, this bit field is automatically loaded with an Efuse value from control module. Bit field remains writable after this. 0x0: External cap is used 0x1: External cap is not used	RW WSpecial	0
3	ENFUNC1_EXPORT	ENFUNC1 input of SRAM LDO. After PowerOn reset and Efuse sensing, this bit field is automatically loaded with an Efuse value from control module. Bit field remains writable after this. 0x0: Short circuit protection is disabled 0x1: Short circuit protection is enabled	RW	0
2	ABBOFF_SLEEP_EXPORT	Determines whether SRAMNWA is supplied by VDDS or VDDAR during deep-sleep. After PowerOn reset and Efuse sensing, this bit field is automatically loaded with an Efuse value from control module. Bit field remains writable after this. 0x0: SRAMNWA supplied with VDDS 0x1: SRAMNWA supplied with VDDAR	RW WSpecial	0

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Bits	Field Name	Description	Type	Reset
1	ABBOFF_ACT_EXPORT	Determines whether SRAMNWA is supplied by VDDS or VDDAR during active mode. After PowerOn reset and Efuse sensing, this bit field is automatically loaded with an Efuse value from control module. Bit field remains writable after this. 0x0: SRAMNWA supplied with VDDS 0x1: SRAMNWA supplied with VDDAR	RW WSpecial	0
0	DISABLE_RTA_EXPORT	Control for HD memory RTA feature. After PowerOn reset and Efuse sensing, this bit field is automatically loaded with an Efuse value from control module. Bit field remains writable after this. 0x0: HD memory RTA feature is enabled 0x1: HD memory RTA feature is disabled	RW WSpecial	0

Table 3-854. Register Call Summary for Register PRM_LDO_SRAM_IVA_SETUP

PRCM Register Manual
- DEVICE_PRM Register Summary: [0]

Table 3-855. PRM_LDO_SRAM_IVA_CTRL

Address Offset	0x0000 00CC		
Physical Address	0x4A30 7BCC	**Instance**	DEVICE_PRM
Description	Control and status of the SRAM LDO for IVA voltage domain. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						SRAM_IN_TRANSITION	SRAMLDO_STATUS	RESERVED							RETMODE_ENABLE

Bits	Field Name	Description	Type	Reset
31:10	RESERVED		R	0x000000
9	SRAM_IN_TRANSITION	Status indicating SRAM LDO state machine state. Read 0x0: SRAM LDO state machine is stable Read 0x1: SRAM LDO state machine is in transition state	R	0
8	SRAMLDO_STATUS	SRAMLDO status Read 0x0: SRAMLDO is in ACTIVE mode. Read 0x1: SRAMLDO is on RETENTION mode.	R	0
7:1	RESERVED		R	0x00
0	RETMODE_ENABLE	Control if the SRAM LDO retention mode is used or not. 0x0: SRAM LDO is not allowed to go to RET mode 0x1: SRAM LDO go to RET mode when all memory of voltage domain are OFF or RET	RW	0

Table 3-856. Register Call Summary for Register PRM_LDO_SRAM_IVA_CTRL

PRCM Register Manual
- DEVICE_PRM Register Summary: [0]

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Table 3-857. PRM_LDO_ABB_MPU_SETUP

Address Offset	0x0000 00D0		
Physical Address	0x4A30 7BD0	**Instance**	DEVICE_PRM
Description	Selects the MPU_ABB LDO mode.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																SR2_WTCNT_VALUE								RESERVED				RESERVED	ACTIVE_FBB_SEL	RESERVED	SR2EN

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:8	SR2_WTCNT_VALUE	LDO settling time for active-mode OPP change. Counting at a 16 system clock cycles rate. Target is 50us. [warm reset insensitive]	RW	0x00
7:4	RESERVED		R	0x0
3	RESERVED	Reserved	RW	0
2	ACTIVE_FBB_SEL	Defines ABB LDO mode when voltage is in slow fast OPP. [warm reset insensitive] 0x0: ABB LDO is in bypass mode 0x1: ABB LDO is in FBB mode	RW	0
1	RESERVED	Reserved	RW	0
0	SR2EN	Enable ABB power management 0x0: ABB LDO is put in bypass mode 0x1: ABB LDO will operate accordingly to settings	RW	0

Table 3-858. Register Call Summary for Register PRM_LDO_ABB_MPU_SETUP

Voltage Management Functional Description
- ABB LDOs Control: [0]

PRCM Register Manual
- DEVICE_PRM Register Summary: [1]

Table 3-859. PRM_LDO_ABB_MPU_CTRL

Address Offset	0x0000 00D4		
Physical Address	0x4A30 7BD4	**Instance**	DEVICE_PRM
Description	Control and Status of ABB on MPU voltage domain. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								SR2_IN_TRANSITION	RESERVED	SR2_STATUS			OPP_CHANGE	OPP_SEL	

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Bits	Field Name	Description	Type	Reset
31:7	RESERVED		R	0x0000000
6	SR2_IN_TRANSITION	Indicates VBBLDO_CON is or is not in transition state. This output should be used by programming interface to clear OPP_CHANGE bit as an indication of OPP change completion. Read 0x0: Read 0x1: Indicates that VBBLDO_CON is in transition and SR2_STATUS bits are not stable to read.	R	0
5	RESERVED		R	0
4:3	SR2_STATUS	Indicate ABB LDO current operation status Read 0x0: ABB LDO is placed in bypass mode. Read 0x1: Reserved Read 0x2: ABB LDO is placed in FBB active mode. Read 0x3: Reserved	R	0x0
2	OPP_CHANGE	When OPP_CHANGE is set to 1, VBBLDO_CON samples OPP_SEL ACTIVE_FBB_SEL upon detecting rising edge. VBBLDO_CON asserts signal SR2_IN_TRANSITION in response to OPP_CHANGE. OPP_CHANGE should be cleared to 0 when SR2_IN_TRANSITION from VBBLDO_CON is de-asserted.	RW WSpecial	0
1:0	OPP_SEL	Selects the OPP at which the MPU voltage domain is operating 0x0: default : Nominal 0x1: Fast OPP 0x2: Nominal 0x3: Slow OPP	RW	0x0

Table 3-860. Register Call Summary for Register PRM_LDO_ABB_MPU_CTRL

Voltage Management Functional Description • ABB LDOs Control: [0]
PRCM Register Manual • DEVICE_PRM Register Summary: [1]

Table 3-861. PRM_LDO_ABB_IVA_SETUP

Address Offset	0x0000 00D8		
Physical Address	0x4A30 7BD8	**Instance**	DEVICE_PRM
Description	Selects the IVA_ABB LDO mode.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																SR2_WTCNT_VALUE								RESERVED				RESERVED	ACTIVE_FBB_SEL	RESERVED	SR2EN

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:8	SR2_WTCNT_VALUE	LDO settling time for active-mode OPP change. Counting at a 16 system clock cycles rate. Target is 50us. [warm reset insensitive]	RW	0x00

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Bits	Field Name	Description	Type	Reset
7:4	RESERVED		R	0x0
3	RESERVED	Reserved	RW	0
2	ACTIVE_FBB_SEL	Defines ABB LDO mode when voltage is in slow fast OPP. [warm reset insensitive] 0x0: ABB LDO is in bypass mode 0x1: ABB LDO is in FBB mode	RW	0
1	RESERVED	Reserved	RW	0
0	SR2EN	Enable ABB power management 0x0: ABB LDO is put in bypass mode 0x1: ABB LDO will operate accordingly to settings	RW	0

Table 3-862. Register Call Summary for Register PRM_LDO_ABB_IVA_SETUP

Voltage Management Functional Description • ABB LDOs Control: [0]
PRCM Register Manual • DEVICE_PRM Register Summary: [1]

Table 3-863. PRM_LDO_ABB_IVA_CTRL

Address Offset	0x0000 00DC		
Physical Address	0x4A30 7BDC	**Instance**	DEVICE_PRM
Description	Control and Status of ABB on IVA voltage domain. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								SR2_IN_TRANSITION	RESERVED	SR2_STATUS			OPP_CHANGE	OPP_SEL	

Bits	Field Name	Description	Type	Reset
31:7	RESERVED		R	0x0000000
6	SR2_IN_TRANSITION	Indicates VBBLDO_CON is or is not in transition state. This output should be used by programming interface to clear OPP_CHANGE bit as an indication of OPP change completion. Read 0x0: Read 0x1: Indicates that VBBLDO_CON is in transition and SR2_STATUS bits are not stable to read.	R	0
5	RESERVED		R	0
4:3	SR2_STATUS	Indicate ABB LDO current operation status Read 0x0: ABB LDO is placed in bypass mode. Read 0x1: Reserved Read 0x2: ABB LDO is placed in FBB active mode. Read 0x3: Reserved	R	0x0

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Bits	Field Name	Description	Type	Reset
2	OPP_CHANGE	When OPP_CHANGE is set to 1, VBBLDO_CON samples OPP_SEL ACTIVE_FBB_SEL upon detecting rising edge. VBBLDO_CON asserts signal SR2_IN_TRANSITION in response to OPP_CHANGE. OPP_CHANGE should be cleared to 0 when SR2_IN_TRANSITION from VBBLDO_CON is de-asserted.	RW WSpecial	0
1:0	OPP_SEL	Selects the OPP at which the IVA voltage domain is operating (Fast OPP, Nominal OPP or Slow OPP) 0x0: default : Nominal 0x1: Fast OPP 0x2: Nominal 0x3: Slow OPP	RW	0x0

Table 3-864. Register Call Summary for Register PRM_LDO_ABB_IVA_CTRL

Voltage Management Functional Description
- ABB LDOs Control: [0]

PRCM Register Manual
- DEVICE_PRM Register Summary: [1]

Table 3-865. PRM_LDO_BANDGAP_SETUP

Address Offset	0x0000 00E0		
Physical Address	0x4A30 7BE0	**Instance**	DEVICE_PRM
Description	Control of the bandgap. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								STARTUP_COUNT							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED		R	0x000000
7:0	STARTUP_COUNT	Determines the start-up duration of BANDGAP. The duration is computed as 32 x NbCycles of system clock cycles. Target is 100us.	RW	0x78

Table 3-866. Register Call Summary for Register PRM_LDO_BANDGAP_SETUP

PRCM Register Manual
- DEVICE_PRM Register Summary: [0]

Table 3-867. PRM_DEVICE_OFF_CTRL

Address Offset	0x0000 00E4		
Physical Address	0x4A30 7BE4	**Instance**	DEVICE_PRM
Description	This register is used to control device OFF transition.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						EMIF2_OFFWKUP_DISABLE	EMIF1_OFFWKUP_DISABLE	RESERVED							DEVICE_OFF_ENABLE

Bits	Field Name	Description	Type	Reset
31:10	RESERVED		R	0x0000 00
9	EMIF2_OFFWKUP_DISABLE	Controls the EMIF2_DEVICE_OFFWKUP_CORESRTACTST notifier sent to EMIF2 upon a device wakeup from off mode. (Warm reset insensitive) 0x0: Notifier is activated. 0x1: Notifier is not activated – stays low.	RW	0
8	EMIF1_OFFWKUP_DISABLE	Controls the EMIF1_DEVICE_OFFWKUP_CORESRTACTST notifier sent to EMIF1 upon a device wakeup from off mode. (Warm reset insensitive) 0x0: Notifier is activated. 0x1: Notifier is not activated – stays low.	RW	0
7:1	RESERVED		R	0x00
0	DEVICE_OFF_ENABLE	Controls transition to device OFF mode. 0x0: Device is not allowed to perform transition to off mode 0x1: Device is allowed to perform transition to off mode as soon as all power domains in MPU, IVA and CORE voltage are in OFF or OsoftwareRET state (open switch retention)	RW	0

Table 3-868. Register Call Summary for Register PRM_DEVICE_OFF_CTRL

PRCM Register Manual
- DEVICE_PRM Register Summary: [0]

Table 3-869. PRM_PHASE1_CNDP

Address Offset	0x0000 00E8		
Physical Address	0x4A30 7BE8	**Instance**	DEVICE_PRM
Description	This register stores the start descriptor address of automatic restore phase1. [warm reset insensitive]		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHASE1_CNDP																															

Bits	Field Name	Description	Type	Reset
31:0	PHASE1_CNDP	Start descriptor address of automatic restore phase1. Hard-coded to SAR_ROM base address.	R Rreturns	0x4A05 E000

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Table 3-870. Register Call Summary for Register PRM_PHASE1_CNDP

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- DEVICE_PRM Register Summary: [0]

Table 3-871. PRM_PHASE2A_CNDP

Address Offset	0x0000 00EC		
Physical Address	0x4A30 7BEC	**Instance**	DEVICE_PRM
Description	This register stores the start descriptor address of automatic restore phase2A. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHASE2A_CNDP																															

Bits	Field Name	Description	Type	Reset
31:0	PHASE2A_CNDP	Start descriptor address of automatic restore phase2A. Hard-coded to SAR_ROM base address + 0x30.	R Rreturns	0x4A05 E030

Table 3-872. Register Call Summary for Register PRM_PHASE2A_CNDP

PRCM Register Manual

- DEVICE_PRM Register Summary: [0]

Table 3-873. PRM_PHASE2B_CNDP

Address Offset	0x0000 00F0		
Physical Address	0x4A30 7BF0	**Instance**	DEVICE_PRM
Description	This register stores the start descriptor address of automatic restore phase2B. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHASE2B_CNDP																															

Bits	Field Name	Description	Type	Reset
31:0	PHASE2B_CNDP	Start descriptor address of automatic restore phase2B. Hard-coded to SAR_ROM base address + 0x60.	R Rreturns	0x4A05 E060

Table 3-874. Register Call Summary for Register PRM_PHASE2B_CNDP

PRCM Register Manual

- DEVICE_PRM Register Summary: [0]

Table 3-875. PRM_VC_ERRST

Address Offset	0x0000 00F8		
Physical Address	0x4A30 7BF8	**Instance**	DEVICE_PRM
Description	This debug register logs the error status coming from Voltage Controller. Must be cleared by software.		
Type	RW		

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31 30 29 28 27	26	25	24	23 22	21	20	19	18	17	16	15 14	13	12	11	10	9	8	7 6	5	4	3	2	1	0
RESERVED	BYPS_TIMEOUT_ERR	BYPS_RA_ERR	BYPS_SA_ERR	RESERVED	VFSM_TIMEOUT_ERR_MPU	VFSM_RA_ERR_MPU	VFSM_SA_ERR_MPU	SMPS_TIMEOUT_ERR_MPU	SMPS_RA_ERR_MPU	SMPS_SA_ERR_MPU	RESERVED	VFSM_TIMEOUT_ERR_IVA	VFSM_RA_ERR_IVA	VFSM_SA_ERR_IVA	SMPS_TIMEOUT_ERR_IVA	SMPS_RA_ERR_IVA	SMPS_SA_ERR_IVA	RESERVED	VFSM_TIMEOUT_ERR_CORE	VFSM_RA_ERR_CORE	VFSM_SA_ERR_CORE	SMPS_TIMEOUT_ERR_CORE	SMPS_RA_ERR_CORE	SMPS_SA_ERR_CORE

Bits	Field Name	Description	Type	Reset
31:27	RESERVED		R	0x00
26	BYPS_TIMEOUT_ERR	Bypass command frame is finished but is not acknowledged by the slave, or (I2C multimaster) arbitration lost. 0x0: No error 0x1: An error has been logged	RW W1toClr	0
25	BYPS_RA_ERR	Wrong register address error for bypass command 0x0: No error 0x1: An error has been logged	RW W1toClr	0
24	BYPS_SA_ERR	Wrong slave address error for bypass command 0x0: No error 0x1: An error has been logged	RW W1toClr	0
23:22	RESERVED		R	0x0
21	VFSM_TIMEOUT_ERR_MPU	MPU voltage FSM command frame is finished but is not acknowledged by the slave, or (I2C multimaster) arbitration lost. 0x0: No error 0x1: An error has been logged	RW W1toClr	0
20	VFSM_RA_ERR_MPU	Wrong register address error for MPU voltage FSM 0x0: No error 0x1: An error has been logged	RW W1toClr	0
19	VFSM_SA_ERR_MPU	Wrong slave address error for MPU voltage FSM 0x0: No error 0x1: An error has been logged	RW W1toClr	0
18	SMPS_TIMEOUT_ERR_MPU	MPU voltage processor command frame is finished but is not acknowledged by the slave, or (I2C multimaster) arbitration lost. 0x0: No error 0x1: An error has been logged	RW W1toClr	0
17	SMPS_RA_ERR_MPU	Wrong register address error for MPU voltage processor 0x0: No error 0x1: An error has been logged	RW W1toClr	0
16	SMPS_SA_ERR_MPU	Wrong slave address error for MPU voltage processor 0x0: No error 0x1: An error has been logged	RW W1toClr	0
15:14	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
13	VFSM_TIMEOUT_ERR_IVA	IVA voltage FSM command frame is finished but is not acknowledged by the slave, or (I2C multimaster) arbitration lost. 0x0: No error 0x1: An error has been logged	RW W1toClr	0
12	VFSM_RA_ERR_IVA	Wrong register address error for IVA voltage FSM 0x0: No error 0x1: An error has been logged	RW W1toClr	0
11	VFSM_SA_ERR_IVA	Wrong slave address error for IVA voltage FSM 0x0: No error 0x1: An error has been logged	RW W1toClr	0
10	SMPS_TIMEOUT_ERR_IVA	IVA voltage processor command frame is finished but is not acknowledged by the slave, or (I2C multimaster) arbitration lost. 0x0: No error 0x1: An error has been logged	RW W1toClr	0
9	SMPS_RA_ERR_IVA	Wrong register address error for IVA voltage processor 0x0: No error 0x1: An error has been logged	RW W1toClr	0
8	SMPS_SA_ERR_IVA	Wrong slave address error for IVA voltage processor 0x0: No error 0x1: An error has been logged	RW W1toClr	0
7:6	RESERVED		R	0x0
5	VFSM_TIMEOUT_ERR_CORE	CORE voltage FSM command frame is finished but is not acknowledged by the slave, or (I2C multimaster) arbitration lost. 0x0: No error 0x1: An error has been logged	RW W1toClr	0
4	VFSM_RA_ERR_CORE	Wrong register address error for CORE voltage FSM 0x0: No error 0x1: An error has been logged	RW W1toClr	0
3	VFSM_SA_ERR_CORE	Wrong slave address error for CORE voltage FSM 0x0: No error 0x1: An error has been logged	RW W1toClr	0
2	SMPS_TIMEOUT_ERR_CORE	CORE voltage processor command frame is finished but is not acknowledged by the slave, or (I2C multimaster) arbitration lost. 0x0: No error 0x1: An error has been logged	RW W1toClr	0
1	SMPS_RA_ERR_CORE	Wrong register address error for CORE voltage processor 0x0: No error 0x1: An error has been logged	RW W1toClr	0
0	SMPS_SA_ERR_CORE	Wrong slave address error for CORE voltage processor 0x0: No error 0x1: An error has been logged	RW W1toClr	0

Table 3-876. Register Call Summary for Register PRM_VC_ERRST

PRCM Register Manual

- DEVICE_PRM Register Summary: [0]

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3.11.20 INSTR_PRM Registers

3.11.20.1 INSTR_PRM Register Summary

Table 3-877. INSTR_PRM Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	INSTR_PRM Base Address
PMI_IDENTICATION	R	32	0x0000 0000	0x4A30 7F00
PMI_SYS_CONFIG	RW	32	0x0000 0010	0x4A30 7F10
PMI_STATUS	R	32	0x0000 0014	0x4A30 7F14
PMI_CONFIGURATION	RW	32	0x0000 0024	0x4A30 7F24
PMI_CLASS_FILTERING	RW	32	0x0000 0028	0x4A30 7F28
PMI_TRIGGERING	RW	32	0x0000 002C	0x4A30 7F2C
PMI_SAMPLING	RW	32	0x0000 0030	0x4A30 7F30

3.11.20.2 INSTR_PRM Register Description

Table 3-878. PMI_IDENTICATION

Address Offset	0x0000 0000		
Physical Address	0x4A30 7F00	**Instance**	INSTR_PRM
Description	PM profiling identification register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP revision	R	0x-- TI Internal data.

Table 3-879. Register Call Summary for Register PMI_IDENTICATION

PRCM Register Manual
- INSTR_PRM Register Summary: [0]

Table 3-880. PMI_SYS_CONFIG

Address Offset	0x0000 0010		
Physical Address	0x4A30 7F10	**Instance**	INSTR_PRM
Description	PM profiling system configuartion register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RESERVED		IDLEMODE		RESERVED		SOFTRESET	

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Bits	Field Name	Description	Type	Reset
31:6	RESERVED	Reserved	R	0x0000000
5:4	RESERVED	Reserved	R	0x0
3:2	IDLEMODE	Configuration of the local tartget state management mode	RW	0x2
1	RESERVED	Reserved	R	0
0	SOFTRESET	Software reset	RW	0

Table 3-881. Register Call Summary for Register PMI_SYS_CONFIG

PRCM Register Manual
- INSTR_PRM Register Summary: [0]

Table 3-882. PMI_STATUS

Address Offset	0x0000 0014		
Physical Address	0x4A30 7F14	**Instance**	INSTR_PRM
Description	PM profiling status register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							FIFOEMPTY	RESERVED							

Bits	Field Name	Description	Type	Reset
31:9	RESERVED	Reserved	R	0x000000
8	FIFOEMPTY	PM Profiling buffer empty	R	1
7:0	RESERVED	Reserved	R	0x00

Table 3-883. Register Call Summary for Register PMI_STATUS

PRCM Register Manual
- INSTR_PRM Register Summary: [0]

Table 3-884. PMI_CONFIGURATION

Address Offset	0x0000 0024		
Physical Address	0x4A30 7F24	**Instance**	INSTR_PRM
Description	PM profiling configuration register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLAIM_3		CLAIM_2	CLAIM_1	RESERVED				RESERVED								RESERVED								EVT_CAPT_EN	RESERVED						

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Bits	Field Name	Description	Type	Reset
31:30	CLAIM_3	Ownership	RW	0x0
29	CLAIM_2	Debugger override qualifier	RW	1
28	CLAIM_1	Current owner	R	0
27:24	RESERVED	Reserved	R	0x0
23	RESERVED	Reserved	R	0
22:16	RESERVED	Reserved	R	0x00
15	RESERVED	Reserved	R	0
14:8	RESERVED	Reserved	R	0x00
7	EVT_CAPT_EN	When HIGH the PM events capture is enabled	RW	0
6:0	RESERVED	Reserved	R	0x00

Table 3-885. Register Call Summary for Register PMI_CONFIGURATION

PRCM Register Manual
- INSTR_PRM Register Summary: [0]

Table 3-886. PMI_CLASS_FILTERING

Address Offset	0x0000 0028		
Physical Address	0x4A30 7F28	**Instance**	INSTR_PRM
Description	PM profiling class filtering register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												SNAP_CAPT_EN_03	SNAP_CAPT_EN_02	SNAP_CAPT_EN_01	SNAP_CAPT_EN_00

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved	R	0x0000000
3	SNAP_CAPT_EN_03	Snapshot capture enable - Class-ID = 0x03	RW	0
2	SNAP_CAPT_EN_02	Snapshot capture enable - Class-ID = 0x02	RW	0
1	SNAP_CAPT_EN_01	Snapshot capture enable - Class-ID = 0x01	RW	0
0	SNAP_CAPT_EN_00	Snapshot capture enable - Class-ID = 0x00	RW	0

Table 3-887. Register Call Summary for Register PMI_CLASS_FILTERING

PRCM Register Manual
- INSTR_PRM Register Summary: [0]

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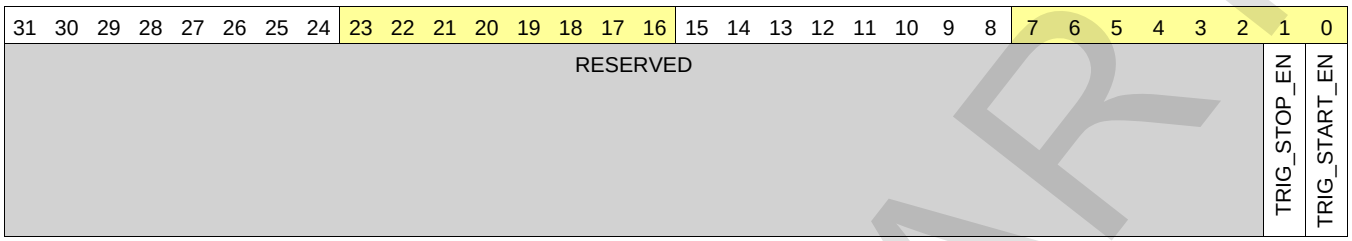
Table 3-888. PMI_TRIGGERING

Address Offset	0x0000 002C		
Physical Address	0x4A30 7F2C	**Instance**	INSTR_PRM
Description	PM profiling triggering control register		
Type	RW		



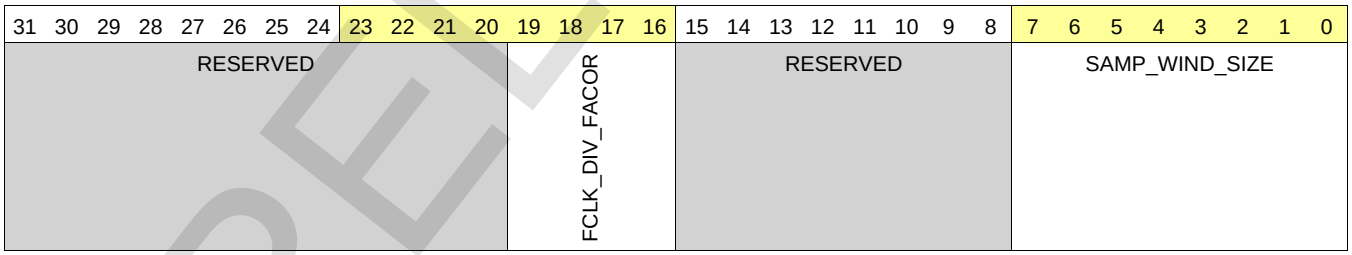
Bits	Field Name	Description	Type	Reset
31:2	RESERVED	Reserved	R	0x0000 0000
1	TRIG_STOP_EN	Enable stop capturing PM events from external trigger detection	RW	0
0	TRIG_START_EN	Enable start capturing PM events from external trigger detection	RW	0

Table 3-889. Register Call Summary for Register PMI_TRIGGERING

PRCM Register Manual
- INSTR_PRM Register Summary: [0]

Table 3-890. PMI_SAMPLING

Address Offset	0x0000 0030		
Physical Address	0x4A30 7F30	**Instance**	INSTR_PRM
Description	PM profiling sampling window register		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:20	RESERVED	Reserved	R	0x000
19:16	FCLK_DIV_FACOR	FunClk divide factor ranging from 1 to 16	RW	0x0
15:8	RESERVED	Reserved	R	0x00
7:0	SAMP_WIND_SIZE	PM events sampling window size	RW	0x00

Table 3-891. Register Call Summary for Register PMI_SAMPLING

PRCM Register Manual
- INSTR_PRM Register Summary: [0]

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3.11.21 CM1 Instance Summary

Table 3-892. CM1 Instance Summary

Module Name	L4 Base Address	Size
INTRCONN_SOCKET_CM1	0x4A00 4000	256Bytes
CKGEN_CM1	0x4A00 4100	512Bytes
MPU_CM1	0x4A00 4300	256Bytes
DSP_CM1	0x4A00 4400	256Bytes
ABE_CM1	0x4A00 4500	256Bytes
RESTORE_CM1	0x4A00 4E00	256Bytes
INSTR_CM1	0x4A00 4F00	256Bytes

3.11.22 INTRCONN_SOCKET_CM1 Registers

3.11.22.1 INTRCONN_SOCKET_CM1 Register Summary

Table 3-893. INTRCONN_SOCKET_CM1 Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	INTRCONN_SOCKET_CM1 L4 Base Address
REVISION_CM1	R	32	0x0000 0000	0x4A00 4000
CM_CM1_PROFILING_CLKCTRL	RW	32	0x0000 0040	0x4A00 4040
CM1_DEBUG_CFG	RW	32	0x0000 00F0	0x4A00 40F0

3.11.22.2 INTRCONN_SOCKET_CM1 Register Description

Table 3-894. REVISION_CM1

Address Offset	0x0000 0000		
Physical Address	0x4A00 4000	**Instance**	INTRCONN_SOCKET_CM1
Description	This register contains the IP revision code for the CM1 part of the PRCM		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	Revision Number	R	0x- - TI Internal data.

Table 3-895. Register Call Summary for Register REVISION_CM1

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- INTRCONN_SOCKET_CM1 Register Summary: [0]

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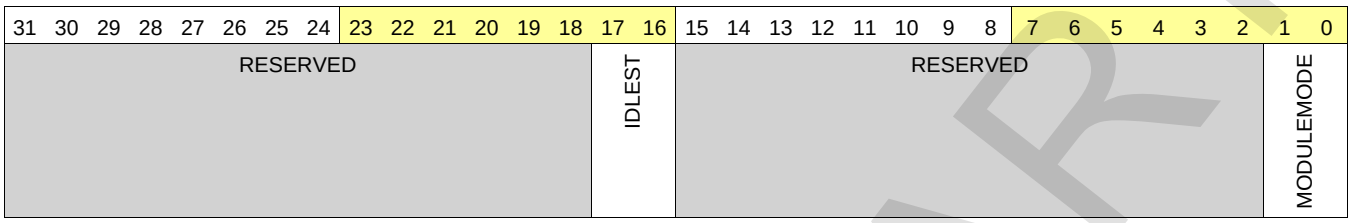
Table 3-896. CM_CM1_PROFILING_CLKCTRL

Address Offset	0x0000 0040		
Physical Address	0x4A00 4040	**Instance**	INTRCONN_SOCKET_CM1
Description	This register manages the CM1_PROFILING clock. [warm reset insensitive]		
Type	RW		



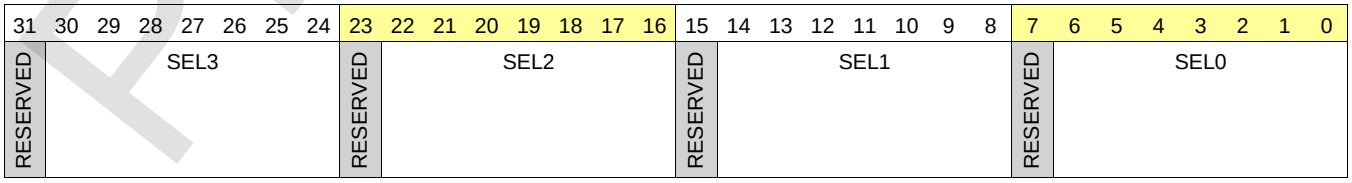
Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status Read 0x0: Module is fully functional Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in Idle Read 0x3: Module is disabled	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disabled by software. INTRCONN configuration port is not accessible. 0x1: Module is managed automatically by hardware along with CM1 and EMU domain. INTRCONN configuration port is accessible only when EMU domain is on. Read 0x2: Reserved Read 0x3: Reserved	RW	0x1

Table 3-897. Register Call Summary for Register CM_CM1_PROFILING_CLKCTRL

PRCM Register Manual
- INTRCONN_SOCKET_CM1 Register Summary: [0]
- RESTORE_CM1 Register Description: [1]

Table 3-898. CM1_DEBUG_CFG

Address Offset	0x0000 00F0		
Physical Address	0x4A00 40F0	**Instance**	INTRCONN_SOCKET_CM1
Description	This register is used to configure the CM1's 32-bit debug output. There is one 7-bit source select field for selecting from a shared set of 8-bit internal signal blocks per byte. [warm reset insensitive]		
Type	RW		



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Bits	Field Name	Description	Type	Reset
31	RESERVED		R	0
30:24	SEL3	Internal signal block select for debug word byte-3	RW	0x03
23	RESERVED		R	0
22:16	SEL2	Internal signal block select for debug word byte-2	RW	0x02
15	RESERVED		R	0
14:8	SEL1	Internal signal block select for debug word byte-1	RW	0x01
7	RESERVED		R	0
6:0	SEL0	Internal signal block select for debug word byte-0	RW	0x00

Table 3-899. Register Call Summary for Register CM1_DEBUG_CFG

PRCM Register Manual
- INTRCONN_SOCKET_CM1 Register Summary: [0]

3.11.23 CKGEN_CM1 Registers

3.11.23.1 CKGEN_CM1 Register Summary

Table 3-900. CKGEN_CM1 Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	CKGEN_CM1 L4 Base Address
CM_CLKSEL_CORE	RW	32	0x0000 0000	0x4A00 4100
CM_CLKSEL_ABE	RW	32	0x0000 0008	0x4A00 4108
CM_DLL_CTRL	RW	32	0x0000 0010	0x4A00 4110
CM_CLKMODE_DPLL_CORE	RW	32	0x0000 0020	0x4A00 4120
CM_IDLEST_DPLL_CORE	R	32	0x0000 0024	0x4A00 4124
CM_AUTOIDLE_DPLL_CORE	RW	32	0x0000 0028	0x4A00 4128
CM_CLKSEL_DPLL_CORE	RW	32	0x0000 002C	0x4A00 412C
CM_DIV_M2_DPLL_CORE	RW	32	0x0000 0030	0x4A00 4130
CM_DIV_M3_DPLL_CORE	RW	32	0x0000 0034	0x4A00 4134
CM_DIV_M4_DPLL_CORE	RW	32	0x0000 0038	0x4A00 4138
CM_DIV_M5_DPLL_CORE	RW	32	0x0000 003C	0x4A00 413C
CM_DIV_M6_DPLL_CORE	RW	32	0x0000 0040	0x4A00 4140
CM_DIV_M7_DPLL_CORE	RW	32	0x0000 0044	0x4A00 4144
CM_SSC_DELTAMSTEP_DPLL_CORE	RW	32	0x0000 0048	0x4A00 4148
CM_SSC_MODFREQDIV_DPLL_CORE	RW	32	0x0000 004C	0x4A00 414C
CM_EMU_OVERRIDE_DPLL_CORE	RW	32	0x0000 0050	0x4A00 4150
CM_CLKMODE_DPLL_MPU	RW	32	0x0000 0060	0x4A00 4160
CM_IDLEST_DPLL_MPU	R	32	0x0000 0064	0x4A00 4164
CM_AUTOIDLE_DPLL_MPU	RW	32	0x0000 0068	0x4A00 4168
CM_CLKSEL_DPLL_MPU	RW	32	0x0000 006C	0x4A00 416C
CM_DIV_M2_DPLL_MPU	RW	32	0x0000 0070	0x4A00 4170
CM_SSC_DELTAMSTEP_DPLL_MPU	RW	32	0x0000 0088	0x4A00 4188
CM_SSC_MODFREQDIV_DPLL_MPU	RW	32	0x0000 008C	0x4A00 418C
CM_BYPCLK_DPLL_MPU	RW	32	0x0000 009C	0x4A00 419C
CM_CLKMODE_DPLL_IVA	RW	32	0x0000 00A0	0x4A00 41A0
CM_IDLEST_DPLL_IVA	R	32	0x0000 00A4	0x4A00 41A4
CM_AUTOIDLE_DPLL_IVA	RW	32	0x0000 00A8	0x4A00 41A8
CM_CLKSEL_DPLL_IVA	RW	32	0x0000 00AC	0x4A00 41AC

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Table 3-900. CKGEN_CM1 Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	CKGEN_CM1 L4 Base Address
CM_DIV_M4_DPLL_IVA	RW	32	0x0000 00B8	0x4A00 41B8
CM_DIV_M5_DPLL_IVA	RW	32	0x0000 00BC	0x4A00 41BC
CM_SSC_DELTAMSTEP_DPLL_IVA	RW	32	0x0000 00C8	0x4A00 41C8
CM_SSC_MODFREQDIV_DPLL_IVA	RW	32	0x0000 00CC	0x4A00 41CC
CM_BYPCLK_DPLL_IVA	RW	32	0x0000 00DC	0x4A00 41DC
CM_CLKMODE_DPLL_ABE	RW	32	0x0000 00E0	0x4A00 41E0
CM_IDLEST_DPLL_ABE	R	32	0x0000 00E4	0x4A00 41E4
CM_AUTOIDLE_DPLL_ABE	RW	32	0x0000 00E8	0x4A00 41E8
CM_CLKSEL_DPLL_ABE	RW	32	0x0000 00EC	0x4A00 41EC
CM_DIV_M2_DPLL_ABE	RW	32	0x0000 00F0	0x4A00 41F0
CM_DIV_M3_DPLL_ABE	RW	32	0x0000 00F4	0x4A00 41F4
CM_SSC_DELTAMSTEP_DPLL_ABE	RW	32	0x0000 0108	0x4A00 4208
CM_SSC_MODFREQDIV_DPLL_ABE	RW	32	0x0000 010C	0x4A00 420C
RESERVED	RW	32	0x0000 0120	0x4A00 4220
RESERVED	R	32	0x0000 0124	0x4A00 4224
RESERVED	RW	32	0x0000 0128	0x4A00 4228
RESERVED	RW	32	0x0000 012C	0x4A00 422C
RESERVED	RW	32	0x0000 0130	0x4A00 4230
RESERVED	RW	32	0x0000 0138	0x4A00 4238
RESERVED	RW	32	0x0000 013C	0x4A00 423C
RESERVED	RW	32	0x0000 0140	0x4A00 4240
RESERVED	RW	32	0x0000 0148	0x4A00 4248
RESERVED	RW	32	0x0000 014C	0x4A00 424C
CM_SHADOW_FREQ_CONFIG1	RW	32	0x0000 0160	0x4A00 4260
CM_SHADOW_FREQ_CONFIG2	RW	32	0x0000 0164	0x4A00 4264
CM_DYN_DEP_PRESCAL	RW	32	0x0000 0170	0x4A00 4270
CM_RESTORE_ST	RW	32	0x0000 0180	0x4A00 4280

3.11.23.2 CKGEN_CM1 Register Description

Table 3-901. CM_CLKSEL_CORE

Address Offset	0x0000 0000		
Physical Address	0x4A00 4100	**Instance**	CKGEN_CM1
Description	CORE module clock selection.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							CLKSEL_L4	RESERVED			CLKSEL_L3	RESERVED			CLKSEL_CORE

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Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	CLKSEL_L4	Selects L4 interconnect clock (L4_clk) 0x0: L4_CLK is L3_CLK divided by 1 0x1: L4_CLK is L3_CLK divided by 2, to be used for OPP100 and OPP50	RW	0
7:5	RESERVED		R	0x0
4	CLKSEL_L3	Selects L3 interconnect clock (L3_clk) 0x0: L3_CLK is CORE_CLK divided by 1 0x1: L3_CLK is CORE_CLK divided by 2, to be used for OPP100 and OPP50	RW	0
3:1	RESERVED		R	0x0
0	CLKSEL_CORE	Selects CORE_CLK configuration 0x0: CORE_CLK is CORE_X2_CLK divided by 1, to be used for OPP100 and OPP50 0x1: CORE_CLK is CORE_X2_CLK divided by 2	RW	0

Table 3-902. Register Call Summary for Register CM_CLKSEL_CORE

Clock Management Functional Description
- CM Clock Source: [0] [1] [2]

PRCM Register Manual
- CKGEN_CM1 Register Summary: [3]
- CKGEN_CM1 Register Description: [4] [5]
- RESTORE_CM1 Register Description: [6] [7] [8]

Table 3-903. CM_CLKSEL_ABE

Address Offset	0x0000 0008		
Physical Address	0x4A00 4108	**Instance**	CKGEN_CM1
Description	ABE module clock selection.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																					SLIMBUS_CLK_GATE	RESERVED	PAD_CLKS_GATE	RESERVED							CLKSEL_OPP

Bits	Field Name	Description	Type	Reset
31:11	RESERVED		R	0x000000
10	SLIMBUS_CLK_GATE	Gating control for SLIMBUS_CLK clock tree in ABE. SLIMbus module always gets the ungated version. 0x0: The clock is gated 0x1: The clock is enabled	RW	0
9	RESERVED		R	0
8	PAD_CLKS_GATE	Gating control for PAD_CLKS clock tree in ABE 0x0: The clock is gated 0x1: The clock is enabled	RW	0
7:2	RESERVED		R	0x00

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Bits	Field Name	Description	Type	Reset
1:0	CLKSEL_OPP	Selects the OPP divider ABE domain 0x0: ABE_CLK is divide by 1 of DPLL_ABE_X2_CLK, to be used for OPP100 0x1: ABE_CLK is divide by 2 of DPLL_ABE_X2_CLK, to be used for OPP50 0x2: ABE_CLK is divide by 4 of DPLL_ABE_X2_CLK 0x3: Reserved	RW	0x0

Table 3-904. Register Call Summary for Register CM_CLKSEL_ABE

Clock Management Functional Description • CM Clock Source: [0] [1] [2] [3]
PRCM Register Manual • CKGEN_CM1 Register Summary: [4]

Table 3-905. CM_DLL_CTRL

Address Offset	0x0000 0010		
Physical Address	0x4A00 4110	**Instance**	CKGEN_CM1
Description	Special register for DLL control		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															DLL_OVERRIDE

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	DLL_OVERRIDE	Control if DLL lock and code outputs are overriden or not 0x0: Lock and code outputs are not overriden 0x1: Lock output is overriden to 1 and code output is overriden with a value coming from control module.	RW	1

Table 3-906. Register Call Summary for Register CM_DLL_CTRL

PRCM Register Manual • CKGEN_CM1 Register Summary: [0] • CKGEN_CM1 Register Description: [1] • RESTORE_CM1 Register Description: [2]

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Table 3-907. CM_CLKMODE_DPLL_CORE

Address Offset	0x0000 0020		
Physical Address	0x4A00 4120	**Instance**	CKGEN_CM1
Description	This register allows controlling the DPLL modes.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																DPLL_SSC_DOWNSPREAD	DPLL_SSC_ACK	DPLL_SSC_EN	DPLL_REGM4XEN	DPLL_LPMODE_EN	RESERVED	DPLL_DRIFTGUARD_EN	RESERVED							DPLL_EN	

Bits	Field Name	Description	Type	Reset
31:15	RESERVED		R	0x00000
14	DPLL_SSC_DOWNSPREAD	Control if only low frequency spread is required 0x0: When SSC is enabled, clock frequency is spread on both sides of the programmed frequency 0x1: When SSC is enabled, clock frequency is spread only on the lower side of the programmed frequency	RW	0
13	DPLL_SSC_ACK	Acknowledgement from the DPLL regarding start and stop of Spread Spectrum Clocking feature Read 0x0: SSC has been turned off on PLL o/ps Read 0x1: SSC has been turned on on PLL o/ps	R	0
12	DPLL_SSC_EN	Enable or disable Spread Spectrum Clocking 0x0: SSC disabled 0x1: SSC enabled	RW	0
11	DPLL_REGM4XEN	Enable the REGM4XEN mode of the DPLL. Please check the DPLL documentation to check when this mode can be enabled. Read 0x0: REGM4XEN mode of the DPLL is disabled	R	0
10	DPLL_LPMODE_EN	Set the DPLL in low-power mode. Check the DPLL documentation to see when this can be enabled. 0x0: Low-power mode of the DPLL is disabled 0x1: Low-power mode of the DPLL is enabled	RW	0
9	RESERVED		RW	0
8	DPLL_DRIFTGUARD_EN	This bit allows to enable or disable the automatic recalibration feature of the DPLL. The DPLL will automatically start a recalibration process upon assertion of the DPLL's RECAL flag if this bit is set. 0x0: DRIFTGUARD feature is disabled 0x1: DRIFTGUARD feature is enabled	RW	0
7:3	RESERVED		RW	0x00

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Bits	Field Name	Description	Type	Reset
2:0	DPLL_EN	DPLL control. Upon Warm Reset, the PRCM DPLL control state machine updates this register to reflect MN bypass mode. 0x0: Reserved 0x1: Reserved 0x2: Reserved 0x3: Reserved 0x4: Put the DPLL in MN bypass mode. The DPLL_MULT register bits are reset to 0 automatically by putting the DPLL in this mode. 0x5: Put the DPLL in Idle bypass low-power mode. 0x6: Put the DPLL in Idle bypass fast-relock mode. 0x7: Enables the DPLL in lock mode	RW	0x4

Table 3-908. Register Call Summary for Register CM_CLKMODE_DPLL_CORE

Clock Management Functional Description
- DPLL_CORE Description: [0] [1] [2] [5] [6] [7]

PRCM Register Manual
- CKGEN_CM1 Register Summary: [8]
- CKGEN_CM1 Register Description: [9]
- RESTORE_CM1 Register Description: [10] [11]

Table 3-909. CM_IDLEST_DPLL_CORE

Address Offset	0x0000 0024		
Physical Address	0x4A00 4124	**Instance**	CKGEN_CM1
Description	This register allows monitoring DPLL activity. This register is read only and automatically updated. [warm reset insensitive]		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							ST_MN_BYPASS	RESERVED							ST_DPLL_CLK

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	ST_MN_BYPASS	DPLL MN_BYPASS status Read 0x1: DPLL is in MN_Bypass Read 0x0: DPLL is not in MN_Bypass	R	0
7:1	RESERVED		R	0x00
0	ST_DPLL_CLK	DPLL lock status Read 0x1: DPLL is LOCKED Read 0x0: DPLL is either in bypass mode or in stop mode.	R	0

Table 3-910. Register Call Summary for Register CM_IDLEST_DPLL_CORE

PRCM Register Manual
- CKGEN_CM1 Register Summary: [0]

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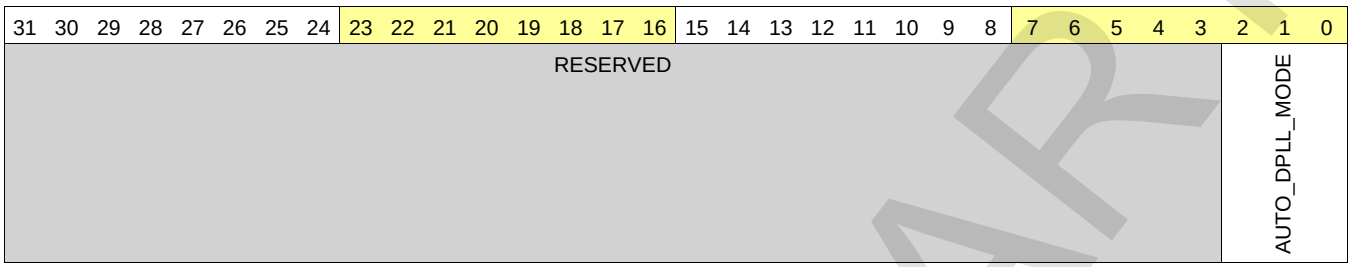
Table 3-911. CM_AUTOIDLE_DPLL_CORE

Address Offset	0x0000 0028		
Physical Address	0x4A00 4128	**Instance**	CKGEN_CM1
Description	This register provides automatic control over the DPLL activity.		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:3	RESERVED		R	0x0000000
2:0	AUTO_DPLL_MODE	DPLL automatic control. 0x0: DPLL auto control disabled 0x1: The DPLL is automatically put in low-power stop mode when its DPLL generated clocks are not required anymore. It is also restarted automatically. 0x2: The DPLL is automatically put in fast-relock stop mode when its DPLL generated clocks are not required anymore. It is also restarted automatically. 0x3: Reserved 0x4: Reserved 0x5: The DPLL is automatically put in idle bypass low-power mode when its DPLL generated clocks are not required anymore. It is also restarted automatically. 0x6: The DPLL is automatically put in idle bypass fast-relock mode when its DPLL generated clocks are not required anymore. It is also restarted automatically. 0x7: Reserved	RW	0x0

Table 3-912. Register Call Summary for Register CM_AUTOIDLE_DPLL_CORE

Clock Management Functional Description • DPLL_CORE Description: [0]
PRCM Register Manual • CKGEN_CM1 Register Summary: [1] • RESTORE_CM1 Register Description: [2]

Table 3-913. CM_CLKSEL_DPLL_CORE

Address Offset	0x0000 002C		
Physical Address	0x4A00 412C	**Instance**	CKGEN_CM1
Description	This register provides controls over the DPLL.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								DPLL_BYP_CLKSEL	RESERVED		DPLL_CLKOUTHIF_CLKSEL	RESERVED	DPLL_MULT											RESERVED	DPLL_DIV							

Bits	Field Name	Description	Type	Reset
31:24	RESERVED		R	0x00
23	DPLL_BYP_CLKSEL	Allows control of the BYPASS clock of the PLL and the associated HSDIVIDER. Same as ULOWCLKEN on DPLL. In DPLL locked mode, 0 - No impact 1 - No impact In DPLL bypass mode, 0 - CLKINP is selected as the BYPASS clock for CLKOUT/CLKOUTX2 1 - CLKINPULOW is selected as the BYPASS clock for CLKOUT/CLKOUTX2	RW	0
22:21	RESERVED		R	0x0
20	DPLL_CLKOUTHIF_CLKSEL	Selects the source of the DPLL CLKOUTHIF clock. Same as CLKINPHIFSEL pin on the DPLL 0x0: CLKOUTHIF is generated from the DPLL oscillator (DCO) 0x1: CLKOUTHIF is generated from CLKINPHIF	RW	0
19	RESERVED		R	0
18:8	DPLL_MULT	DPLL multiplier factor (2 to 2047). This register is automatically cleared to 0 when the DPLL_EN field in the *CLKMODE_DPLL* register is set to select MN bypass mode. (equal to input M of DPLL; M=2 to 2047 = DPLL multiplies by M). 0x0: Reserved 0x1: Reserved	RW	0x000
7	RESERVED		R	0
6:0	DPLL_DIV	DPLL divider factor (0 to 127) (equal to input N of DPLL; actual division factor is N+1).	RW	0x00

Table 3-914. Register Call Summary for Register CM_CLKSEL_DPLL_CORE

Clock Management Functional Description • CM Clock Source: [0] • DPLL_CORE Description: [1] [2]
PRCM Register Manual • CKGEN_CM1 Register Summary: [3] • RESTORE_CM1 Register Description: [4]

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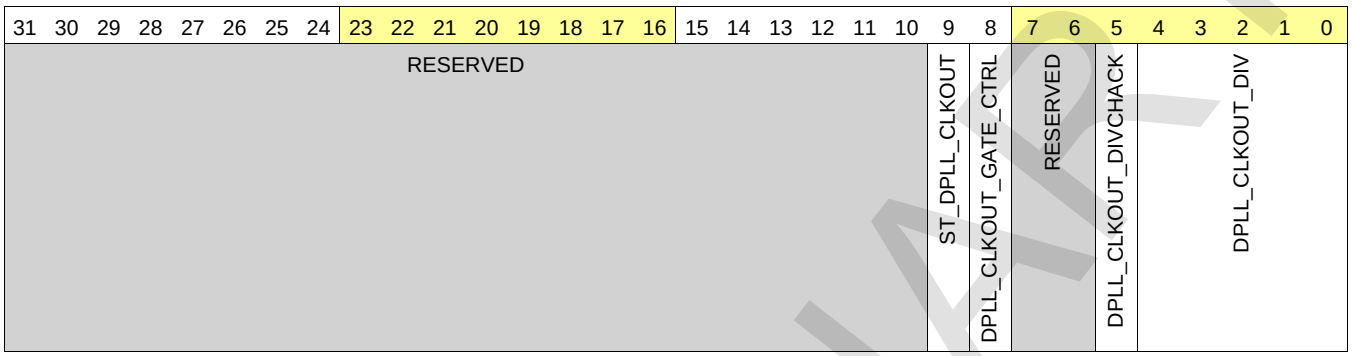
Table 3-915. CM_DIV_M2_DPLL_CORE

Address Offset	0x0000 0030		
Physical Address	0x4A00 4130	**Instance**	CKGEN_CM1
Description	This register provides controls over the M2 divider of the DPLL.		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:10	RESERVED		R	0x000000
9	ST_DPLL_CLKOUT	DPLL CLKOUT status Read 0x0: The clock output is gated Read 0x1: The clock output is enabled	R	0
8	DPLL_CLKOUT_GATE_CTRL	Control gating of DPLL CLKOUT 0x0: Automatically gate this clock when there is no dependency for it 0x1: Force this clock to stay enabled even if there is no request	RW	0
7:6	RESERVED		R	0x0
5	DPLL_CLKOUT_DIVCHACK	Toggle on this status bit after changing DPLL_CLKOUT_DIV indicates that the change in divider value has taken effect	R	0
4:0	DPLL_CLKOUT_DIV	DPLL post-divider factor, M2, for internal clock generation (1 to 31); Divide value from 1 to 31. 0x0: Reserved 0x1: 1, to be used for OPP100 0x2: 2, to be used for OPP50	RW	0x01

Table 3-916. Register Call Summary for Register CM_DIV_M2_DPLL_CORE

Clock Management Functional Description
- DPLL_CORE Description: [0] [1] [2] [3]

PRCM Register Manual
- CKGEN_CM1 Register Summary: [4]
- CKGEN_CM1 Register Description: [5]
- RESTORE_CM1 Register Description: [6] [7]

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Table 3-917. CM_DIV_M3_DPLL_CORE

Address Offset	0x0000 0034		
Physical Address	0x4A00 4134	**Instance**	CKGEN_CM1
Description	This register provides controls over the M3 divider of the DPLL.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						ST_DPLL_CLKOUTHIF	DPLL_CLKOUTHIF_GATE_CTRL	RESERVED		DPLL_CLKOUTHIF_DIVCHACK	DPLL_CLKOUTHIF_DIV				

Bits	Field Name	Description	Type	Reset
31:10	RESERVED		R	0x000000
9	ST_DPLL_CLKOUTHIF	DPLL CLKOUTHIF status Read 0x0: The clock output is gated Read 0x1: The clock output is enabled	R	0
8	DPLL_CLKOUTHIF_GATE_CTRL	Control gating of DPLL CLKOUTHIF 0x0: Gate unconditionally this clock and stop requesting it 0x1: Request this clock and un-gate it when available	RW	0
7:6	RESERVED		R	0x0
5	DPLL_CLKOUTHIF_DIVCHACK	Toggle on this status bit after changing DPLL_CLKOUTHIF_DIV indicates that the change in divider value has taken effect	R	0
4:0	DPLL_CLKOUTHIF_DIV	DPLL post-divider factor, M3, for internal clock generation (1 to 31). Divide value from 1 to 31 0x0: Reserved 0x5: 5, to be used for OPP100 0x8: 8, to be used for OPP50	RW	0x01

Table 3-918. Register Call Summary for Register CM_DIV_M3_DPLL_CORE

Clock Management Functional Description

- Generic DPLL Overview: [0]
- DPLL_CORE Description: [1] [2] [3] [4]

PRCM Register Manual

- CKGEN_CM1 Register Summary: [5]
- RESTORE_CM1 Register Description: [6]

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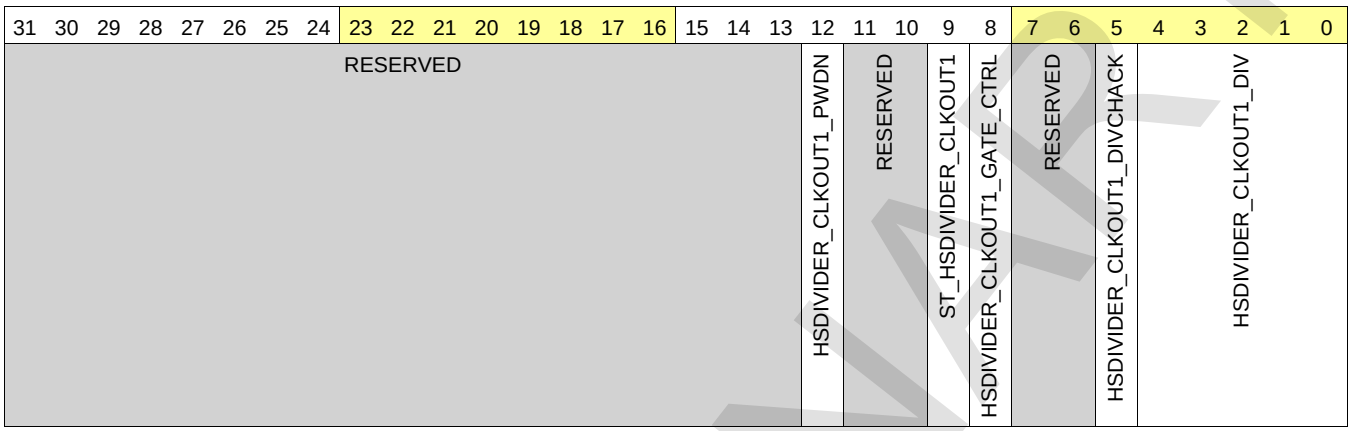
Table 3-919. CM_DIV_M4_DPLL_CORE

Address Offset	0x0000 0038		
Physical Address	0x4A00 4138	**Instance**	CKGEN_CM1
Description	This register provides controls over the CLKOUT1 o/p of the HSDIVIDER.		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000
12	HSDIVIDER_CLKOUT1_PWDN	Direct power down control for HSDIVIDER M4 divider and CLKOUT1 output. Power down should be enabled only when clock is first gated. 0x0: Divider is powered up 0x1: Divider is powered down	RW	0
11:10	RESERVED		R	0x0
9	ST_HSDIVIDER_CLKOUT1	HSDIVIDER CLKOUT1 status Read 0x0: The clock output is gated Read 0x1: The clock output is enabled	R	0
8	HSDIVIDER_CLKOUT1_GATE_CTRL	Control gating of HSDIVIDER CLKOUT1 0x0: Automatically gate this clock when there is no dependency for it 0x1: Force this clock to stay enabled even if there is no request	RW	0
7:6	RESERVED		R	0x0
5	HSDIVIDER_CLKOUT1_DIVCHACK	Toggle on this status bit after changing HSDIVIDER_CLKOUT1_DIV indicates that the change in divider value has taken effect	R	0
4:0	HSDIVIDER_CLKOUT1_DIV	DPLL M4 post-divider factor (1 to 31). 0x0: Reserved 0x8: 8, to be used for OPP100 and OPP50	RW	0x04

Table 3-920. Register Call Summary for Register CM_DIV_M4_DPLL_CORE

Clock Management Functional Description
- DPLL_CORE Description: [0] [1] [2] [3] [4]

PRCM Register Manual
- CKGEN_CM1 Register Summary: [5]
- RESTORE_CM1 Register Description: [6]

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Table 3-921. CM_DIV_M5_DPLL_CORE

Address Offset	0x0000 003C		
Physical Address	0x4A00 413C	**Instance**	CKGEN_CM1
Description	This register provides controls over the CLKOUT2 o/p of the HSDIVIDER.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																			HSDIVIDER_CLKOUT2_PWDN	RESERVED		ST_HSDIVIDER_CLKOUT2	HSDIVIDER_CLKOUT2_GATE_CTRL	RESERVED		HSDIVIDER_CLKOUT2_DIVCHACK	HSDIVIDER_CLKOUT2_DIV					

Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000
12	HSDIVIDER_CLKOUT2_PWDN	Direct power down control for HSDIVIDER M5 divider and CLKOUT2 output. Power down should be enabled only when clock is first gated. 0x0: Divider is powered up 0x1: Divider is powered down	RW	0
11:10	RESERVED		R	0x0
9	ST_HSDIVIDER_CLKOUT2	HSDIVIDER CLKOUT2 status Read 0x0: The clock output is gated Read 0x1: The clock output is enabled	R	0
8	HSDIVIDER_CLKOUT2_GATE_CTRL	Control gating of HSDIVIDER CLKOUT2 0x0: Automatically gate this clock when there is no dependency for it 0x1: Force this clock to stay enabled even if there is no request	RW	0
7:6	RESERVED		R	0x0
5	HSDIVIDER_CLKOUT2_DIVCHACK	Toggle on this status bit after changing HSDIVIDER_CLKOUT2_DIV indicates that the change in divider value has taken effect	R	0
4:0	HSDIVIDER_CLKOUT2_DIV	DPLL M5 post-divider factor (1 to 31) 0x0: Reserved 0x4: 4, to be used for OPP100 0x8: 8, to be used for OPP50	RW	0x04

Table 3-922. Register Call Summary for Register CM_DIV_M5_DPLL_CORE

Clock Management Functional Description
- DPLL_CORE Description: [0] [1] [2] [3] [4]

PRCM Register Manual
- CKGEN_CM1 Register Summary: [5]
- CKGEN_CM1 Register Description: [6]
- RESTORE_CM1 Register Description: [7] [8]

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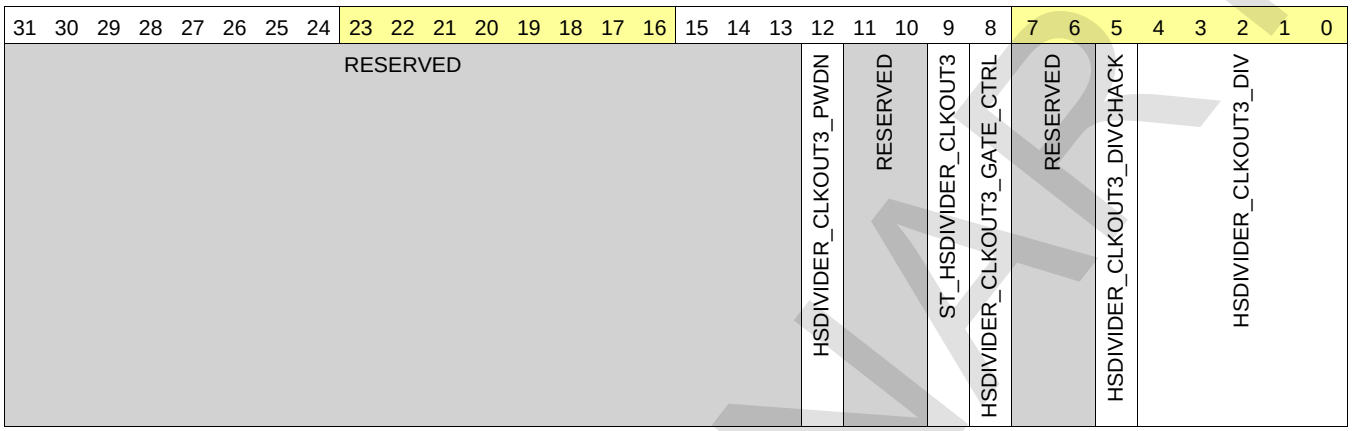
Table 3-923. CM_DIV_M6_DPLL_CORE

Address Offset	0x0000 0040		
Physical Address	0x4A00 4140	**Instance**	CKGEN_CM1
Description	This register provides controls over the CLKOUT3 o/p of the HSDIVIDER.		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000
12	HSDIVIDER_CLKOUT3_PWDN	Direct power down control for HSDIVIDER M6 divider and CLKOUT3 output. Power down should be enabled only when clock is first gated. 0x0: Divider is powered up 0x1: Divider is powered down	RW	0
11:10	RESERVED		R	0x0
9	ST_HSDIVIDER_CLKOUT3	HSDIVIDER CLKOUT3 status Read 0x0: The clock output is gated Read 0x1: The clock output is enabled	R	0
8	HSDIVIDER_CLKOUT3_GATE_CTRL	Control gating of HSDIVIDER CLKOUT3 0x0: Automatically gate this clock when there is no dependency for it 0x1: Force this clock to stay enabled even if there is no request	RW	0
7:6	RESERVED		R	0x0
5	HSDIVIDER_CLKOUT3_DIVCHACK	Toggle on this status bit after changing HSDIVIDER_CLKOUT3_DIV indicates that the change in divider value has taken effect	R	0
4:0	HSDIVIDER_CLKOUT3_DIV	DPLL M6 post-divider factor (1 to 31) 0x0: Reserved 0x6: 6, to be used for OPP100 0x8: 8, to be used for OPP50	RW	0x08

Table 3-924. Register Call Summary for Register CM_DIV_M6_DPLL_CORE

Clock Management Functional Description
- DPLL_CORE Description: [0] [1] [2] [3] [4]

PRCM Register Manual
- CKGEN_CM1 Register Summary: [5]
- RESTORE_CM1 Register Description: [6]

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Table 3-925. CM_DIV_M7_DPLL_CORE

Address Offset	0x0000 0044		
Physical Address	0x4A00 4144	**Instance**	CKGEN_CM1
Description	This register provides controls over the CLKOUT4 o/p of the HSDIVIDER.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																			HSDIVIDER_CLKOUT4_PWDN	RESERVED		ST_HSDIVIDER_CLKOUT4	HSDIVIDER_CLKOUT4_GATE_CTRL	RESERVED		HSDIVIDER_CLKOUT4_DIVCHACK	HSDIVIDER_CLKOUT4_DIV					

Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000
12	HSDIVIDER_CLKOUT4_PWDN	Direct power down control for HSDIVIDER M7 divider and CLKOUT4 output. Power down should be enabled only when clock is first gated. 0x0: Divider is powered up 0x1: Divider is powered down	RW	0
11:10	RESERVED		R	0x0
9	ST_HSDIVIDER_CLKOUT4	HSDIVIDER CLKOUT4 status Read 0x0: The clock output is gated Read 0x1: The clock output is enabled	R	0
8	HSDIVIDER_CLKOUT4_GATE_CTRL	Control gating of HSDIVIDER CLKOUT4 0x0: Automatically gate this clock when there is no dependency for it 0x1: Force this clock to stay enabled even if there is no request	RW	0
7:6	RESERVED		R	0x0
5	HSDIVIDER_CLKOUT4_DIVCHACK	Toggle on this status bit after changing HSDIVIDER_CLKOUT4_DIV indicates that the change in divider value has taken effect(1)	R	0
4:0	HSDIVIDER_CLKOUT4_DIV	DPLL M7 post-divider factor (1 to 31) 0x0: Reserved 0x6: 6, to be used for OPP100 for 266.7-MHz clock output 0x8: 8, to be used for OPP100 for 200-MHz clock output 0xC: 12, to be used for OPP50 for 133.3-MHz clock output 0x10: 16, to be used for OPP50 for 100-MHz clock output	RW	0x04

(1) It is toggled only if the programmed divider value differs from the previous one.

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Table 3-926. Register Call Summary for Register CM_DIV_M7_DPLL_CORE

Clock Management Functional Description • DPLL_CORE Description: [0] [1] [2] [3] [4]
PRCM Register Manual • CKGEN_CM1 Register Summary: [5] • RESTORE_CM1 Register Description: [6]

Table 3-927. CM_SSC_DELTAMSTEP_DPLL_CORE

Address Offset	0x0000 0048		
Physical Address	0x4A00 4148	**Instance**	CKGEN_CM1
Description	Control the DeltaMStep parameter for Spread Spectrum Clocking. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																DELTAMSTEP															

Bits	Field Name	Description	Type	Reset
31:20	RESERVED		R	0x000
19:0	DELTAMSTEP	DeltaMStep is split into fractional and integer part. For Triangular Spread Spectrum: [19:18] for integer part, [17:0] for fractional part For Square Wave Spread Spectrum [19:14] for integer part, [13:0] for fractional part	RW	0x00000

Table 3-928. Register Call Summary for Register CM_SSC_DELTAMSTEP_DPLL_CORE

Clock Management Functional Description • DPLL_CORE Description: [0]
PRCM Register Manual • CKGEN_CM1 Register Summary: [1] • RESTORE_CM1 Register Description: [2]

Table 3-929. CM_SSC_MODFREQDIV_DPLL_CORE

Address Offset	0x0000 004C		
Physical Address	0x4A00 414C	**Instance**	CKGEN_CM1
Description	Control the Modulation Frequency (Fm) for Spread Spectrum. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																					MODFREQDIV_EXPONENT			RESERVED	MODFREQDIV_MANTISSA						

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Bits	Field Name	Description	Type	Reset
31:11	RESERVED		R	0x000000
10:8	MODFREQDIV_EXPONENT	Set the Exponent component of MODFREQDIV factor	RW	0x0
7	RESERVED		R	0
6:0	MODFREQDIV_MANTISSA	Set the Mantissa component of MODFREQDIV factor	RW	0x00

Table 3-930. Register Call Summary for Register CM_SSC_MODFREQDIV_DPLL_CORE

Clock Management Functional Description
- DPLL_CORE Description: [0] [1]

PRCM Register Manual
- CKGEN_CM1 Register Summary: [2]
- RESTORE_CM1 Register Description: [3]

Table 3-931. CM_EMU_OVERRIDE_DPLL_CORE

Address Offset	0x0000 0050		
Physical Address	0x4A00 4150	**Instance**	CKGEN_CM1
Description	This register provides emulation override controls over the CORE DPLL.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												OVERRIDE_ENABLE	CORE_DPLL_EMU_MULT											RESERVED	CORE_DPLL_EMU_DIV						

Bits	Field Name	Description	Type	Reset
31:20	RESERVED		R	0x000
19	OVERRIDE_ENABLE	This bit allows to enable or disable the emulation override controls 0x0: The emulation override controls are disabled 0x1: The emulation override controls are enabled	RW	0
18:8	CORE_DPLL_EMU_MULT	DPLL multiplier factor (2 to 2047). (equal to input M of DPLL; M=2 to 2047 = DPLL multiplies by M) 0x0: Reserved 0x1: Reserved	RW	0x000
7	RESERVED		R	0
6:0	CORE_DPLL_EMU_DIV	CORE DPLL override divider factor (0 to 127) (equal to input N of DPLL; actual division factor is N+1).	RW	0x00

Table 3-932. Register Call Summary for Register CM_EMU_OVERRIDE_DPLL_CORE

PRCM Register Manual
- CKGEN_CM1 Register Summary: [0]

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Table 3-933. CM_CLKMODE_DPLL_MPU

Address Offset	0x0000 0060		
Physical Address	0x4A00 4160	**Instance**	CKGEN_CM1
Description	This register allows controlling the DPLL modes.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																DPLL_SSC_DOWNSPREAD	DPLL_SSC_ACK	DPLL_SSC_EN	DPLL_REGM4XEN	DPLL_LPMODE_EN	RESERVED	DPLL_DRIFTGUARD_EN	RESERVED						DPLL_EN		

Bits	Field Name	Description	Type	Reset
31:15	RESERVED		R	0x00000
14	DPLL_SSC_DOWNSPREAD	Control if only low frequency spread is required 0x0: When SSC is enabled, clock frequency is spread on both sides of the programmed frequency 0x1: When SSC is enabled, clock frequency is spread only on the lower side of the programmed frequency	RW	0
13	DPLL_SSC_ACK	Acknowledgement from the DPLL regarding start and stop of Spread Spectrum Clocking feature Read 0x0: SSC has been turned off on PLL o/ps Read 0x1: SSC has been turned on on PLL o/ps	R	0
12	DPLL_SSC_EN	Enable or disable Spread Spectrum Clocking 0x0: SSC disabled 0x1: SSC enabled	RW	0
11	DPLL_REGM4XEN	Enable the REGM4XEN mode of the DPLL. Please check the DPLL documentation to check when this mode can be enabled. Read 0x0: REGM4XEN mode of the DPLL is disabled	R	0
10	DPLL_LPMODE_EN	Set the DPLL in low-power mode. Check the DPLL documentation to see when this can be enabled. 0x0: Low-power mode of the DPLL is disabled 0x1: Low-power mode of the DPLL is enabled	RW	0
9	RESERVED		RW	0
8	DPLL_DRIFTGUARD_EN	This bit allows to enable or disable the automatic recalibration feature of the DPLL. The DPLL will automatically start a recalibration process upon assertion of the DPLL's RECAL flag if this bit is set. 0x0: DRIFTGUARD feature is disabled 0x1: DRIFTGUARD feature is enabled	RW	0
7:3	RESERVED		RW	0x00

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Bits	Field Name	Description	Type	Reset
2:0	DPLL_EN	DPLL control. Upon Warm Reset, the PRCM DPLL control state machine updates this register to reflect MN bypass mode. 0x0: Reserved 0x1: Reserved 0x2: Reserved 0x3: Reserved 0x4: Put the DPLL in MN bypass mode. The DPLL_MULT register bits are reset to 0 automatically by putting the DPLL in this mode. 0x5: Put the DPLL in idle bypass low-power mode. 0x6: Put the DPLL in idle bypass fast-relock mode. 0x7: Enables the DPLL in lock mode	RW	0x4

Table 3-934. Register Call Summary for Register CM_CLKMODE_DPLL_MPU

Clock Management Functional Description • DPLL_MPU Description: [0] [1] [2] [5] [6] [7]
PRCM Register Manual • CKGEN_CM1 Register Summary: [8]

Table 3-935. CM_IDLEST_DPLL_MPU

Address Offset	0x0000 0064		
Physical Address	0x4A00 4164	**Instance**	CKGEN_CM1
Description	This register allows monitoring DPLL activity. This register is read only and automatically updated. [warm reset insensitive]		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							ST_MN_BYPASS	RESERVED							ST_DPLL_CLK

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	ST_MN_BYPASS	DPLL MN_BYPASS status Read 0x1: DPLL is in MN_Bypass Read 0x0: DPLL is not in MN_Bypass	R	0
7:1	RESERVED		R	0x00
0	ST_DPLL_CLK	DPLL lock status Read 0x1: DPLL is LOCKED Read 0x0: DPLL is either in bypass mode or in stop mode.	R	0

Table 3-936. Register Call Summary for Register CM_IDLEST_DPLL_MPU

PRCM Register Manual • CKGEN_CM1 Register Summary: [0]

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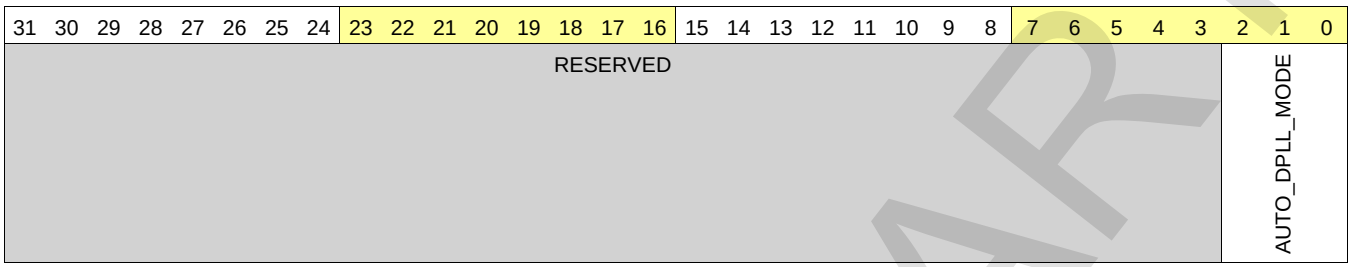
Table 3-937. CM_AUTOIDLE_DPLL_MPU

Address Offset	0x0000 0068		
Physical Address	0x4A00 4168	**Instance**	CKGEN_CM1
Description	This register provides automatic control over the DPLL activity.		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:3	RESERVED		R	0x0000 0000
2:0	AUTO_DPLL_MODE	DPLL automatic control; 0x0: DPLL auto control disabled 0x1: The DPLL is automatically put in low-power stop mode when its DPLL generated clocks are not required anymore. It is also restarted automatically. 0x2: The DPLL is automatically put in fast-relock stop mode when its DPLL generated clocks are not required anymore. It is also restarted automatically. 0x3: Reserved 0x4: Reserved 0x5: The DPLL is automatically put in idle bypass low-power mode when its DPLL generated clocks are not required anymore. It is also restarted automatically. 0x6: The DPLL is automatically put in idle bypass fast-relock mode when its DPLL generated clocks are not required anymore. It is also restarted automatically. 0x7: Reserved	RW	0x0

Table 3-938. Register Call Summary for Register CM_AUTOIDLE_DPLL_MPU

Clock Management Functional Description • DPLL_MPU Description: [0]
PRCM Register Manual • CKGEN_CM1 Register Summary: [1]

Table 3-939. CM_CLKSEL_DPLL_MPU

Address Offset	0x0000 006C		
Physical Address	0x4A00 416C	**Instance**	CKGEN_CM1
Description	This register provides controls over the DPLL.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DCC_COUNT_MAX								DPLL_BYP_CLKSEL	DCC_EN	RESERVED						DPLL_MULT								RESERVED	DPLL_DIV						

Bits	Field Name	Description	Type	Reset
31:24	DCC_COUNT_MAX	The value "NbCycles" set in this field determines the duration of the clock ramp step during which the output frequency is Fdpll/(2*M2). The duration is computed as 32 x NbCycles of L4 clock cycles (100 MHz). Duration should be 1.5 µs to allow enough time for DCC to lock. This bit field is relevant only when DCC_EN = 1.	RW	0x05
23	DPLL_BYP_CLKSEL	Only CLKINPULOW bypass clock supported for this PLL	R Returns 1s	1
22	DCC_EN	Enable or disable duty cycle correction. Must be enabled only for frequency 1 GHz. When enabled, the CLKOUTHIF output of the DPLL is used after duty cycle correction instead of CLKOUT. The M3 divider is hard-wired to 1 so the lock frequency Fdpll is directly provided to MPU. 0x0: DCC disabled 0x1: DCC enabled	RW	0
21:19	RESERVED		R	0x0
18:8	DPLL_MULT	DPLL multiplier factor (2 to 2047). This register is automatically cleared to 0 when the DPLL_EN field in the *CLKMODE_DPLL* register is set to select MN bypass mode. (equal to input M of DPLL; M=2 to 2047 = DPLL multiplies by M). 0x0: Reserved 0x1: Reserved	RW	0x000
7	RESERVED		R	0
6:0	DPLL_DIV	DPLL divider factor (0 to 127) (equal to input N of DPLL; actual division factor is N+1).	RW	0x00

Table 3-940. Register Call Summary for Register CM_CLKSEL_DPLL_MPU

Clock Management Functional Description • DPLL_MPU Description: [0] [1] [2] [3]
PRCM Register Manual • CKGEN_CM1 Register Summary: [4]

Table 3-941. CM_DIV_M2_DPLL_MPU

Address Offset	0x0000 0070		
Physical Address	0x4A00 4170	**Instance**	CKGEN_CM1
Description	This register provides controls over the M2 divider of the DPLL.		
Type	RW		

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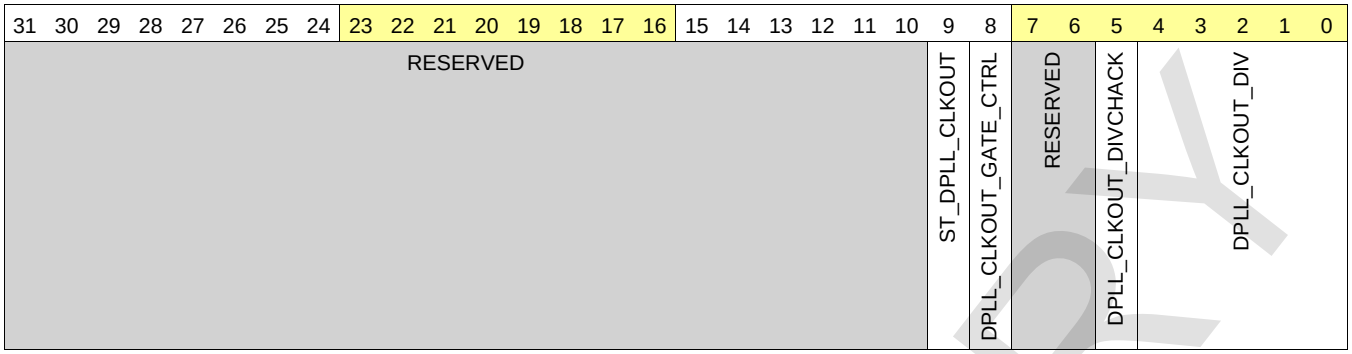


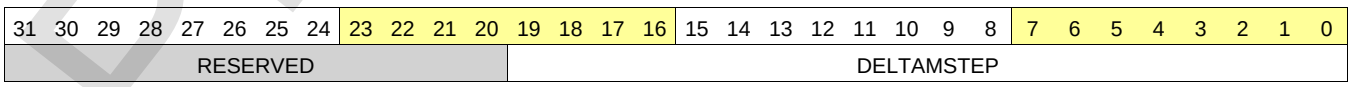
Bits	Field Name	Description	Type	Reset
31:10	RESERVED		R	0x000000
9	ST_DPLL_CLKOUT	DPLL CLKOUT status Read 0x0: The clock output is gated Read 0x1: The clock output is enabled	R	0
8	DPLL_CLKOUT_GATE_CTRL	Control gating of DPLL CLKOUT 0x0: Automatically gate this clock when there is no dependency for it 0x1: Force this clock to stay enabled even if there is no request	RW	0
7:6	RESERVED		R	0x0
5	DPLL_CLKOUT_DIVCHACK	Toggle on this status bit after changing DPLL_CLKOUT_DIV indicates that the change in divider value has taken effect	R	0
4:0	DPLL_CLKOUT_DIV	DPLL post-divider factor, M2, for internal clock generation (1 to 31);Divide value from 1 to 31 0x0: Reserved 0x1: 1, to be used for OPP100, OPP_TURBO, OPP_NITRO, and OPP_NITROSB 0x2: 2, to be used for OPP50	RW	0x01

Table 3-942. Register Call Summary for Register CM_DIV_M2_DPLL_MPU

Clock Management Functional Description • DPLL_MPU Description: [0] [1] [2] [3]
PRCM Register Manual • CKGEN_CM1 Register Summary: [4]

Table 3-943. CM_SSC_DELTAMSTEP_DPLL_MPU

Address Offset	0x0000 0088		
Physical Address	0x4A00 4188	**Instance**	CKGEN_CM1
Description	Control the DeltaMStep parameter for Spread Spectrum Clocking. [warm reset insensitive]		
Type	RW		



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Bits	Field Name	Description	Type	Reset
31:20	RESERVED		R	0x000
19:0	DELTAMSTEP	DeltaMStep is split into fractional and integer part. For Triangular Spread Spectrum: [19:18] for integer part, [17:0] for fractional part For Square Wave Spread Spectrum [19:14] for integer part, [13:0] for fractional part	RW	0x00000

Table 3-944. Register Call Summary for Register CM_SSC_DELTAMSTEP_DPLL_MPU

Clock Management Functional Description
- DPLL_MPU Description: [0]

PRCM Register Manual
- CKGEN_CM1 Register Summary: [1]

Table 3-945. CM_SSC_MODFREQDIV_DPLL_MPU

Address Offset	0x0000 008C		
Physical Address	0x4A00 418C	**Instance**	CKGEN_CM1
Description	Control the Modulation Frequency (Fm) for Spread Spectrum. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																					MODFREQDIV_EXPONENT			RESERVED	MODFREQDIV_MANTISSA						

Bits	Field Name	Description	Type	Reset
31:11	RESERVED		R	0x000000
10:8	MODFREQDIV_EXPONENT	Set the Exponent component of MODFREQDIV factor	RW	0x0
7	RESERVED		R	0
6:0	MODFREQDIV_MANTISSA	Set the Mantissa component of MODFREQDIV factor	RW	0x00

Table 3-946. Register Call Summary for Register CM_SSC_MODFREQDIV_DPLL_MPU

Clock Management Functional Description
- DPLL_MPU Description: [0] [1]

PRCM Register Manual
- CKGEN_CM1 Register Summary: [2]

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Table 3-947. CM_BYPCLK_DPLL_MPU

Address Offset	0x0000 009C		
Physical Address	0x4A00 419C	**Instance**	CKGEN_CM1
Description	Control MPU PLL BYPASS clock. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														CLKSEL	

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1:0	CLKSEL	Select the DPLL MPU bypass clock 0x0: DPLL_MPU bypass clock is CORE_X2_CLK divided by 1, to be used for OPP100 and OPP50 0x1: DPLL_MPU bypass clock is CORE_X2_CLK divided by 2 0x2: DPLL_MPU bypass clock is CORE_X2_CLK divided by 4 0x3: DPLL_MPU bypass clock is CORE_X2_CLK divided by 8	RW	0x0

Table 3-948. Register Call Summary for Register CM_BYPCLK_DPLL_MPU

Clock Management Functional Description
- CM Clock Source: [0]

PRCM Register Manual
- CKGEN_CM1 Register Summary: [1]

Table 3-949. CM_CLKMODE_DPLL_IVA

Address Offset	0x0000 00A0		
Physical Address	0x4A00 41A0	**Instance**	CKGEN_CM1
Description	This register allows controlling the DPLL modes.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																DPLL_SSC_DOWNSPREAD	DPLL_SSC_ACK	DPLL_SSC_EN	DPLL_REGM4XEN	DPLL_LPMODE_EN	RESERVED	DPLL_DRIFTGUARD_EN	RESERVED							DPLL_EN	

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Bits	Field Name	Description	Type	Reset
31:15	RESERVED		R	0x00000
14	DPLL_SSC_DOWNSPREAD	Control if only low frequency spread is required 0x0: When SSC is enabled, clock frequency is spread on both sides of the programmed frequency 0x1: When SSC is enabled, clock frequency is spread only on the lower side of the programmed frequency	RW	0
13	DPLL_SSC_ACK	Acknowledgement from the DPLL regarding start and stop of Spread Spectrum Clocking feature Read 0x0: SSC has been turned off on PLL o/ps Read 0x1: SSC has been turned on on PLL o/ps	R	0
12	DPLL_SSC_EN	Enable or disable Spread Spectrum Clocking 0x0: SSC disabled 0x1: SSC enabled	RW	0
11	DPLL_REGM4XEN	Enable the REGM4XEN mode of the DPLL. Please check the DPLL documentation to check when this mode can be enabled. Read 0x0: REGM4XEN mode of the DPLL is disabled	R	0
10	DPLL_LPMODE_EN	Set the DPLL in low-power mode. Check the DPLL documentation to see when this can be enabled. 0x0: Low-power mode of the DPLL is disabled 0x1: Low-power mode of the DPLL is enabled	RW	0
9	RESERVED		RW	0
8	DPLL_DRIFTGUARD_EN	This bit allows to enable or disable the automatic recalibration feature of the DPLL. The DPLL will automatically start a recalibration process upon assertion of the DPLL's RECAL flag if this bit is set. 0x0: DRIFTGUARD feature is disabled 0x1: DRIFTGUARD feature is enabled	RW	0
7:3	RESERVED		RW	0x00
2:0	DPLL_EN	DPLL control. Upon Warm Reset, the PRCM DPLL control state machine updates this register to reflect MN bypass mode. 0x0: Reserved 0x1: Reserved 0x2: Reserved 0x3: Reserved 0x4: Put the DPLL in MN bypass mode. The DPLL_MULT register bits are reset to 0 automatically by putting the DPLL in this mode. 0x5: Put the DPLL in idle bypass low-power mode. 0x6: Reserved 0x7: Enables the DPLL in lock mode	RW	0x4

Table 3-950. Register Call Summary for Register CM_CLKMODE_DPLL_IVA

Clock Management Functional Description • DPLL_IVA Description: [0] [1] [2] [5] [6] [7]
PRCM Register Manual • CKGEN_CM1 Register Summary: [8]

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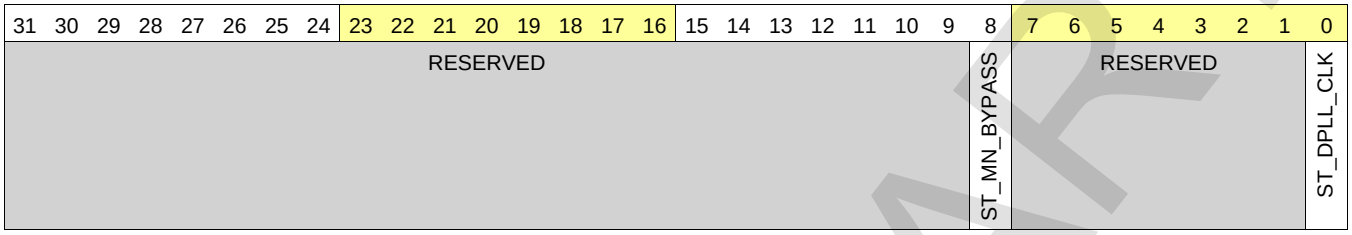
Table 3-951. CM_IDLEST_DPLL_IVA

Address Offset	0x0000 00A4		
Physical Address	0x4A00 41A4	**Instance**	CKGEN_CM1
Description	This register allows monitoring DPLL activity. This register is read only and automatically updated. [warm reset insensitive]		
Type	R		



Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	ST_MN_BYPASS	DPLL MN_BYPASS status Read 0x1: DPLL is in MN_Bypass Read 0x0: DPLL is not in MN_Bypass	R	0
7:1	RESERVED		R	0x00
0	ST_DPLL_CLK	DPLL lock status Read 0x1: DPLL is LOCKED Read 0x0: DPLL is either in bypass mode or in stop mode.	R	0

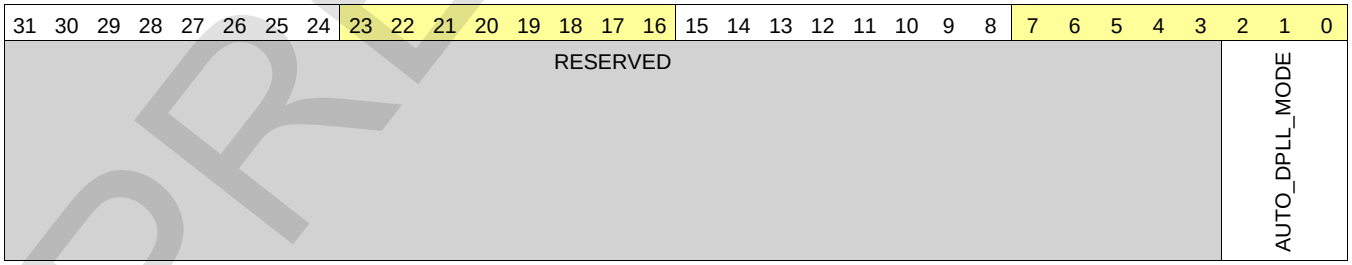
Table 3-952. Register Call Summary for Register CM_IDLEST_DPLL_IVA

PRCM Register Manual

- CKGEN_CM1 Register Summary: [0]

Table 3-953. CM_AUTOIDLE_DPLL_IVA

Address Offset	0x0000 00A8		
Physical Address	0x4A00 41A8	**Instance**	CKGEN_CM1
Description	This register provides automatic control over the DPLL activity.		
Type	RW		



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Bits	Field Name	Description	Type	Reset
31:3	RESERVED		R	0x0000000
2:0	AUTO_DPLL_MODE	DPLL automatic control; 0x0: DPLL auto control disabled 0x1: The DPLL is automatically put in low-power stop mode when its DPLL generated clocks are not required anymore. It is also restarted automatically. 0x2: The DPLL is automatically put in fast-relock stop mode when its DPLL generated clocks are not required anymore. It is also restarted automatically. 0x3: Reserved 0x4: Reserved 0x5: The DPLL is automatically put in idle bypass low-power mode when its DPLL generated clocks are not required anymore. It is also restarted automatically. 0x6: Reserved 0x7: Reserved	RW	0x0

Table 3-954. Register Call Summary for Register CM_AUTOIDLE_DPLL_IVA

Clock Management Functional Description • DPLL_IVA Description: [0]
PRCM Register Manual • CKGEN_CM1 Register Summary: [1]

Table 3-955. CM_CLKSEL_DPLL_IVA

Address Offset	0x0000 00AC		
Physical Address	0x4A00 41AC	**Instance**	CKGEN_CM1
Description	This register provides controls over the DPLL.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								DPLL_BYP_CLKSEL	RESERVED							DPLL_MULT								RESERVED	DPLL_DIV						

Bits	Field Name	Description	Type	Reset
31:24	RESERVED		R	0x00
23	DPLL_BYP_CLKSEL	Allows control of the BYPASS clock of the PLL and the associated HSDIVIDER. Same as ULOWCLKEN on DPLL. In DPLL locked mode, 0 - No impact 1 - No impact In DPLL bypass mode, 0 - CLKINP is selected as the BYPASS clock for CLKOUT/CLKOUTX2 1 - CLKINPULOW is selected as the BYPASS clock for CLKOUT/CLKOUTX2	RW	0
22:19	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
18:8	DPLL_MULT	DPLL multiplier factor (2 to 2047). This register is automatically cleared to 0 when the DPLL_EN field in the *CLKMODE_DPLL* register is set to select MN bypass mode. (equal to input M of DPLL; M=2 to 2047 = DPLL multiplies by M). 0x0: Reserved 0x1: Reserved	RW	0x000
7	RESERVED		R	0
6:0	DPLL_DIV	DPLL divider factor (0 to 127) (equal to input N of DPLL; actual division factor is N+1).	RW	0x00

Table 3-956. Register Call Summary for Register CM_CLKSEL_DPLL_IVA

Clock Management Functional Description • CM Clock Source: [0] • DPLL_IVA Description: [1] [2]
PRCM Register Manual • CKGEN_CM1 Register Summary: [3]

Table 3-957. CM_DIV_M4_DPLL_IVA

Address Offset	0x0000 00B8		
Physical Address	0x4A00 41B8	**Instance**	CKGEN_CM1
Description	This register provides controls over the CLKOUT1 o/p of the HSDIVIDER.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																			HSDIVIDER_CLKOUT1_PWDN	RESERVED		ST_HSDIVIDER_CLKOUT1	HSDIVIDER_CLKOUT1_GATE_CTRL	RESERVED		HSDIVIDER_CLKOUT1_DIVCHACK	HSDIVIDER_CLKOUT1_DIV							

Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000
12	HSDIVIDER_CLKOUT1_PWDN	Direct power down control for HSDIVIDER M4 divider and CLKOUT1 output. Power down should be enabled only when clock is first gated. 0x0: Divider is powered up 0x1: Divider is powered down	RW	0
11:10	RESERVED		R	0x0
9	ST_HSDIVIDER_CLKOUT1	HSDIVIDER CLKOUT1 status Read 0x0: The clock output is gated Read 0x1: The clock output is enabled	R	0

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Bits	Field Name	Description	Type	Reset
8	HSDIVIDER_CLKOUT1_GATE_CTRL	Control gating of HSDIVIDER CLKOUT1 0x0: Automatically gate this clock when there is no dependency for it 0x1: Force this clock to stay enabled even if there is no request	RW	0
7:6	RESERVED		R	0x0
5	HSDIVIDER_CLKOUT1_DIVCHACK	Toggle on this status bit after changing HSDIVIDER_CLKOUT1_DIV indicates that the change in divider value has taken effect	R	0
4:0	HSDIVIDER_CLKOUT1_DIV	DPLL M4 post-divider factor (1 to 31) 0x00: Reserved 0x2: 2, to be used for OPP_TURBO and OPP_NITRO 0x4: 4, to be used for OPP100 0x8: 8, to be used for OPP50	RW	0x04

Table 3-958. Register Call Summary for Register CM_DIV_M4_DPLL_IVA

Clock Management Functional Description • DPLL_IVA Description: [0] [1] [2] [3] [4]
PRCM Register Manual • CKGEN_CM1 Register Summary: [5]

Table 3-959. CM_DIV_M5_DPLL_IVA

Address Offset	0x0000 00BC		
Physical Address	0x4A00 41BC	**Instance**	CKGEN_CM1
Description	This register provides controls over the CLKOUT2 o/p of the HSDIVIDER.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																			HSDIVIDER_CLKOUT2_PWDN	RESERVED		ST_HSDIVIDER_CLKOUT2	HSDIVIDER_CLKOUT2_GATE_CTRL	RESERVED		HSDIVIDER_CLKOUT2_DIVCHACK	HSDIVIDER_CLKOUT2_DIV					

Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000
12	HSDIVIDER_CLKOUT2_PWDN	Direct power down control for HSDIVIDER M5 divider and CLKOUT2 output. Power down should be enabled only when clock is first gated. 0x0: Divider is powered up 0x1: Divider is powered down	RW	0
11:10	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
9	ST_HSDIVIDER_CLKOUT2	HSDIVIDER CLKOUT2 status Read 0x0: The clock output is gated Read 0x1: The clock output is enabled	R	0
8	HSDIVIDER_CLKOUT2_GATE_CTRL	Control gating of HSDIVIDER CLKOUT2 0x0: Automatically gate this clock when there is no dependency for it 0x1: Force this clock to stay enabled even if there is no request.	RW	0
7:6	RESERVED		R	0x0
5	HSDIVIDER_CLKOUT2_DIVCHACK	Toggle on this status bit after changing HSDIVIDER_CLKOUT2_DIV indicates that the change in divider value has taken effect.	R	0
4:0	HSDIVIDER_CLKOUT2_DIV	DPLL M5 post-divider factor (1 to 31) 0x00: Reserved 0x2: 2, to be used for OPP_NITRO 0x3: 3, to be used for OPP_TURBO 0x7: 7, to be used for OPP100 0xE: 14, to be used for OPP50	RW	0x04

Table 3-960. Register Call Summary for Register CM_DIV_M5_DPLL_IVA

Clock Management Functional Description • DPLL_IVA Description: [0] [1] [2] [3] [4]
PRCM Register Manual • CKGEN_CM1 Register Summary: [5]

Table 3-961. CM_SSC_DELTAMSTEP_DPLL_IVA

Address Offset	0x0000 00C8		
Physical Address	0x4A00 41C8	**Instance**	CKGEN_CM1
Description	Control the DeltaMStep parameter for Spread Spectrum Clocking. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																DELTAMSTEP															

Bits	Field Name	Description	Type	Reset
31:20	RESERVED		R	0x000
19:0	DELTAMSTEP	DeltaMStep is split into fractional and integer part. For Triangular Spread Spectrum: [19:18] for integer part, [17:0] for fractional part For Square Wave Spread Spectrum [19:14] for integer part, [13:0] for fractional part	RW	0x00000

Table 3-962. Register Call Summary for Register CM_SSC_DELTAMSTEP_DPLL_IVA

Clock Management Functional Description • DPLL_IVA Description: [0]
PRCM Register Manual • CKGEN_CM1 Register Summary: [1]

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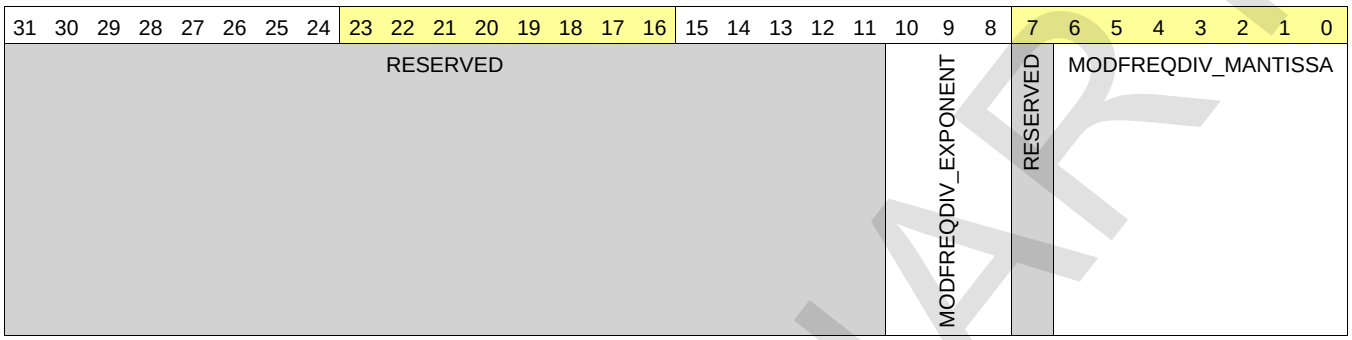
Table 3-963. CM_SSC_MODFREQDIV_DPLL_IVA

Address Offset	0x0000 00CC		
Physical Address	0x4A00 41CC	**Instance**	CKGEN_CM1
Description	Control the Modulation Frequency (Fm) for Spread Spectrum. [warm reset insensitive]		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:11	RESERVED		R	0x000000
10:8	MODFREQDIV_EXPONENT	Set the Exponent component of MODFREQDIV factor	RW	0x0
7	RESERVED		R	0
6:0	MODFREQDIV_MANTISSA	Set the Mantissa component of MODFREQDIV factor	RW	0x00

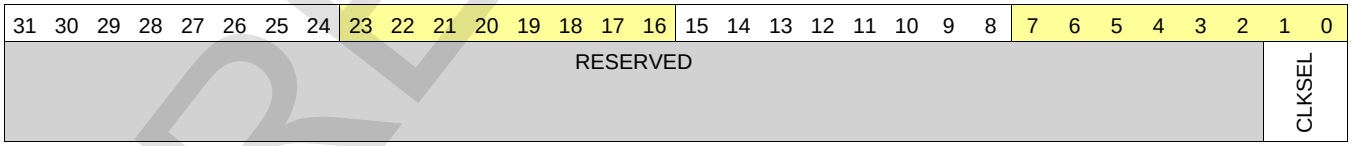
Table 3-964. Register Call Summary for Register CM_SSC_MODFREQDIV_DPLL_IVA

Clock Management Functional Description
- DPLL_IVA Description: [0] [1]

PRCM Register Manual
- CKGEN_CM1 Register Summary: [2]

Table 3-965. CM_BYPCLK_DPLL_IVA

Address Offset	0x0000 00DC		
Physical Address	0x4A00 41DC	**Instance**	CKGEN_CM1
Description	Control IVA PLL BYPASS clock. [warm reset insensitive]		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1:0	CLKSEL	Select the DPLL IVA bypass clock 0x0: DPLL_IVA bypass clock is CORE_X2_CLK divided by 1, to be used for OPP100 and OPP50 0x1: DPLL_IVA bypass clock is CORE_X2_CLK divided by 2 0x2: DPLL_IVA bypass clock is CORE_X2_CLK divided by 4 0x3: DPLL_IVA bypass clock is CORE_X2_CLK divided by 8	RW	0x0

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Table 3-966. Register Call Summary for Register CM_BYPCLK_DPLL_IVA

Clock Management Functional Description
- CM Clock Source: [0]

PRCM Register Manual
- CKGEN_CM1 Register Summary: [1]

Table 3-967. CM_CLKMODE_DPLL_ABE

Address Offset	0x0000 00E0		
Physical Address	0x4A00 41E0	**Instance**	CKGEN_CM1
Description	This register allows controlling the DPLL modes.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																DPLL_SSC_DOWNSPREAD	DPLL_SSC_ACK	DPLL_SSC_EN	DPLL_REGM4XEN	DPLL_LPMODE_EN	RESERVED	DPLL_DRIFTGUARD_EN	RESERVED							DPLL_EN	

Bits	Field Name	Description	Type	Reset
31:15	RESERVED		R	0x00000
14	DPLL_SSC_DOWNSPREAD	Control if only low frequency spread is required 0x0: When SSC is enabled, clock frequency is spread on both sides of the programmed frequency 0x1: When SSC is enabled, clock frequency is spread only on the lower side of the programmed frequency	RW	0
13	DPLL_SSC_ACK	Acknowledgement from the DPLL regarding start and stop of Spread Spectrum Clocking feature Read 0x0: SSC has been turned off on PLL o/ps Read 0x1: SSC has been turned on on PLL o/ps	R	0
12	DPLL_SSC_EN	Enable or disable Spread Spectrum Clocking 0x0: SSC disabled 0x1: SSC enabled	RW	0
11	DPLL_REGM4XEN	Enable the REGM4XEN mode of the DPLL. Please check the DPLL documentation to check when this mode can be enabled. Read 0x0: REGM4XEN mode of the DPLL is disabled	RW	0
10	DPLL_LPMODE_EN	Set the DPLL in low-power mode. Check the DPLL documentation to see when this can be enabled. 0x0: Low-power mode of the DPLL is disabled 0x1: Low-power mode of the DPLL is enabled	RW	0
9	RESERVED		RW	0
8	DPLL_DRIFTGUARD_EN	This bit allows to enable or disable the automatic recalibration feature of the DPLL. The DPLL will automatically start a recalibration process upon assertion of the DPLL's RECAL flag if this bit is set. 0x0: DRIFTGUARD feature is disabled 0x1: DRIFTGUARD feature is enabled	RW	0
7:3	RESERVED		RW	0x00

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Bits	Field Name	Description	Type	Reset
2:0	DPLL_EN	DPLL control. Upon Warm Reset, the PRCM DPLL control state machine updates this register to reflect MN bypass mode. 0x0: Reserved 0x1: Reserved 0x2: Reserved 0x3: Reserved 0x4: Put the DPLL in MN bypass mode. The DPLL_MULT register bits are reset to 0 automatically by putting the DPLL in this mode. 0x5: Put the DPLL in idle bypass low-power mode. 0x6: Put the DPLL in idle bypass fast-relock mode. 0x7: Enables the DPLL in lock mode	RW	0x4

Table 3-968. Register Call Summary for Register CM_CLKMODE_DPLL_ABE

Clock Management Functional Description • DPLL_ABE Description: [0] [1] [2] [5] [6] [7]
PRCM Register Manual • CKGEN_CM1 Register Summary: [8]

Table 3-969. CM_IDLEST_DPLL_ABE

Address Offset	0x0000 00E4		
Physical Address	0x4A00 41E4	**Instance**	CKGEN_CM1
Description	This register allows monitoring DPLL activity. This register is read only and automatically updated. [warm reset insensitive]		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							ST_MN_BYPASS	RESERVED							ST_DPLL_CLK

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	ST_MN_BYPASS	DPLL MN_BYPASS status Read 0x1: DPLL is in MN_Bypass Read 0x0: DPLL is not in MN_Bypass	R	0
7:1	RESERVED		R	0x00
0	ST_DPLL_CLK	DPLL lock status Read 0x1: DPLL is LOCKED Read 0x0: DPLL is either in bypass mode or in stop mode.	R	0

Table 3-970. Register Call Summary for Register CM_IDLEST_DPLL_ABE

PRCM Register Manual • CKGEN_CM1 Register Summary: [0]

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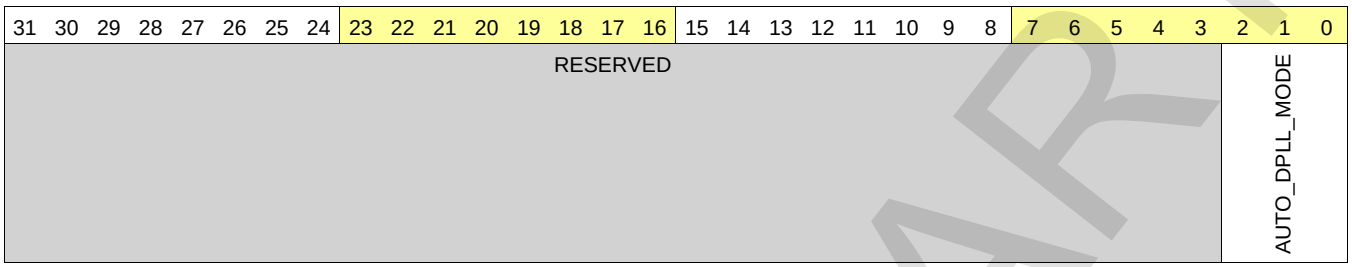
Table 3-971. CM_AUTOIDLE_DPLL_ABE

Address Offset	0x0000 00E8		
Physical Address	0x4A00 41E8	**Instance**	CKGEN_CM1
Description	This register provides automatic control over the DPLL activity.		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:3	RESERVED		R	0x0000 0000
2:0	AUTO_DPLL_MODE	DPLL automatic control; 0x0: DPLL auto control disabled 0x1: The DPLL is automatically put in low-power stop mode when its DPLL generated clocks are not required anymore. It is also restarted automatically. 0x2: The DPLL is automatically put in fast-relock stop mode when its DPLL generated clocks are not required anymore. It is also restarted automatically. 0x3: Reserved 0x4: Reserved 0x5: The DPLL is automatically put in idle bypass low-power mode when its DPLL generated clocks are not required anymore. It is also restarted automatically. 0x6: The DPLL is automatically put in idle bypass fast-relock mode when its DPLL generated clocks are not required anymore. It is also restarted automatically. 0x7: Reserved	RW	0x0

Table 3-972. Register Call Summary for Register CM_AUTOIDLE_DPLL_ABE

Clock Management Functional Description • DPLL_ABE Description: [0]
PRCM Register Manual • CKGEN_CM1 Register Summary: [1]

Table 3-973. CM_CLKSEL_DPLL_ABE

Address Offset	0x0000 00EC		
Physical Address	0x4A00 41EC	**Instance**	CKGEN_CM1
Description	This register provides controls over the DPLL.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								DPLL_BYP_CLKSEL	RESERVED							DPLL_MULT								RESERVED	DPLL_DIV						

Bits	Field Name	Description	Type	Reset
31:24	RESERVED		R	0x00
23	DPLL_BYP_CLKSEL	Only CLKINPULOW bypass clock supported for this PLL	R Rreturns 1s	1
22:19	RESERVED		R	0x0
18:8	DPLL_MULT	DPLL multiplier factor (2 to 2047). This register is automatically cleared to 0 when the DPLL_EN field in the *CLKMODE_DPLL* register is set to select MN bypass mode. (equal to input M of DPLL; M=2 to 2047 = DPLL multiplies by M). 0x0: Reserved 0x1: Reserved	RW	0x000
7	RESERVED		R	0
6:0	DPLL_DIV	DPLL divider factor (0 to 127) (equal to input N of DPLL; actual division factor is N+1).	RW	0x00

Table 3-974. Register Call Summary for Register CM_CLKSEL_DPLL_ABE

Clock Management Functional Description • DPLL_ABE Description: [0] [1]
PRCM Register Manual • CKGEN_CM1 Register Summary: [2]

Table 3-975. CM_DIV_M2_DPLL_ABE

Address Offset	0x0000 00F0		
Physical Address	0x4A00 41F0	**Instance**	CKGEN_CM1
Description	This register provides controls over the M2 divider of the DPLL.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				ST_DPLL_CLKOUTX2	DPLL_CLKOUTX2_GATE_CTRL	ST_DPLL_CLKOUT	DPLL_CLKOUT_GATE_CTRL	RESERVED	DPLL_CLKOUT_DIVCHACK	DPLL_CLKOUT_DIV						

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Bits	Field Name	Description	Type	Reset
31:12	RESERVED		R	0x00000
11	ST_DPLL_CLKOUTX2	DPLL CLKOUTX2 status Read 0x0: The clock output is gated Read 0x1: The clock output is enabled	R	0
10	DPLL_CLKOUTX2_GATE_CTRL	Control gating of DPLL CLKOUTX2 0x0: Automatically gate this clock when there is no dependency for it 0x1: Force this clock to stay enabled even if there is no request	RW	0
9	ST_DPLL_CLKOUT	DPLL CLKOUT status Read 0x0: The clock output is gated Read 0x1: The clock output is enabled	R	0
8	DPLL_CLKOUT_GATE_CTRL	Control gating of DPLL CLKOUT 0x0: Automatically gate this clock when there is no dependency for it 0x1: Force this clock to stay enabled even if there is no request.	RW	0
7:6	RESERVED		R	0x0
5	DPLL_CLKOUT_DIVCHACK	Toggle on this status bit after changing DPLL_CLKOUT_DIV indicates that the change in divider value has taken effect.	R	0
4:0	DPLL_CLKOUT_DIV	DPLL post-divider factor, M2, for internal clock generation (1 to 31). Divide value from 1 to 31 0x0: Reserved 0x1: 1, to be used for OPP100 and OPP50	RW	0x01

Table 3-976. Register Call Summary for Register CM_DIV_M2_DPLL_ABE

Clock Management Functional Description • DPLL_ABE Description: [0] [1] [2] [3] [4] [5]
PRCM Register Manual • CKGEN_CM1 Register Summary: [6]

Table 3-977. CM_DIV_M3_DPLL_ABE

Address Offset	0x0000 00F4		
Physical Address	0x4A00 41F4	**Instance**	CKGEN_CM1
Description	This register provides controls over the M3 divider of the DPLL.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						ST_DPLL_CLKOUTHIF	DPLL_CLKOUTHIF_GATE_CTRL	RESERVED		DPLL_CLKOUTHIF_DIVCHACK	DPLL_CLKOUTHIF_DIV				

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Bits	Field Name	Description	Type	Reset
31:10	RESERVED		R	0x000000
9	ST_DPLL_CLKOUTHIF	DPLL CLKOUTHIF status Read 0x0: The clock output is gated Read 0x1: The clock output is enabled	R	0
8	DPLL_CLKOUTHIF_GATE_CTRL	Control gating of DPLL CLKOUTHIF 0x0: Automatically gate this clock when there is no dependency for it 0x1: Force this clock to stay enabled even if there is no request.	RW	0
7:6	RESERVED		R	0x0
5	DPLL_CLKOUTHIF_DIVCHACK	Toggle on this status bit after changing DPLL_CLKOUTHIF_DIV indicates that the change in divider value has taken effect.	R	0
4:0	DPLL_CLKOUTHIF_DIV	DPLL post-divider factor, M3, for internal clock generation (1 to 31). Divide value from 1 to 31 0x0: Reserved 0x1: 1, to be used for OPP100 and OPP50	RW	0x01

Table 3-978. Register Call Summary for Register CM_DIV_M3_DPLL_ABE

Clock Management Functional Description • DPLL_ABE Description: [0] [1] [2] [3]
PRCM Register Manual • CKGEN_CM1 Register Summary: [4]

Table 3-979. CM_SSC_DELTAMSTEP_DPLL_ABE

Address Offset	0x0000 0108		
Physical Address	0x4A00 4208	**Instance**	CKGEN_CM1
Description	Control the DeltaMStep parameter for Spread Spectrum Clocking. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																DELTAMSTEP															

Bits	Field Name	Description	Type	Reset
31:20	RESERVED		R	0x000
19:0	DELTAMSTEP	DeltaMStep is split into fractional and integer part. For Triangular Spread Spectrum: [19:18] for integer part, [17:0] for fractional part For Square Wave Spread Spectrum [19:14] for integer part, [13:0] for fractional part	RW	0x00000

Table 3-980. Register Call Summary for Register CM_SSC_DELTAMSTEP_DPLL_ABE

Clock Management Functional Description • DPLL_ABE Description: [0]
PRCM Register Manual • CKGEN_CM1 Register Summary: [1]

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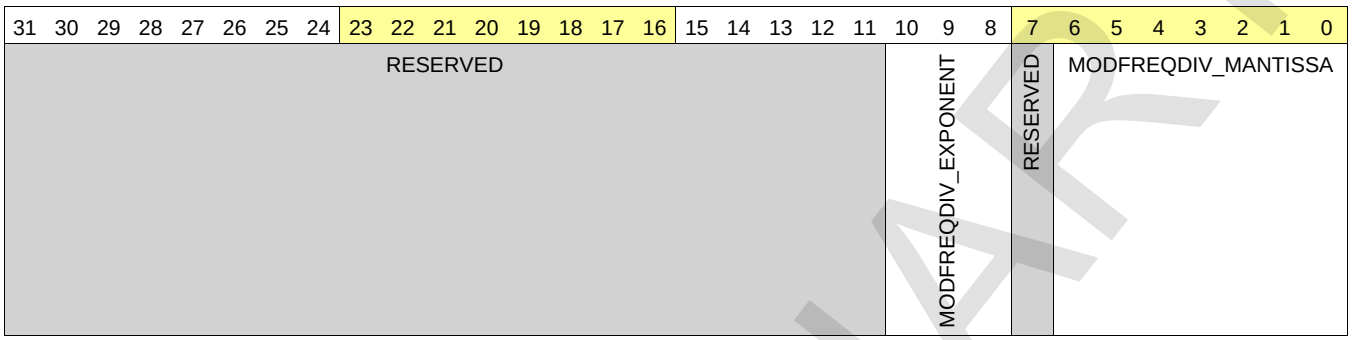
Table 3-981. CM_SSC_MODFREQDIV_DPLL_ABE

Address Offset	0x0000 010C		
Physical Address	0x4A00 420C	**Instance**	CKGEN_CM1
Description	Control the Modulation Frequency (Fm) for Spread Spectrum. [warm reset insensitive]		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:11	RESERVED		R	0x000000
10:8	MODFREQDIV_EXPONENT	Set the Exponent component of MODFREQDIV factor	RW	0x0
7	RESERVED		R	0
6:0	MODFREQDIV_MANTISSA	Set the Mantissa component of MODFREQDIV factor	RW	0x00

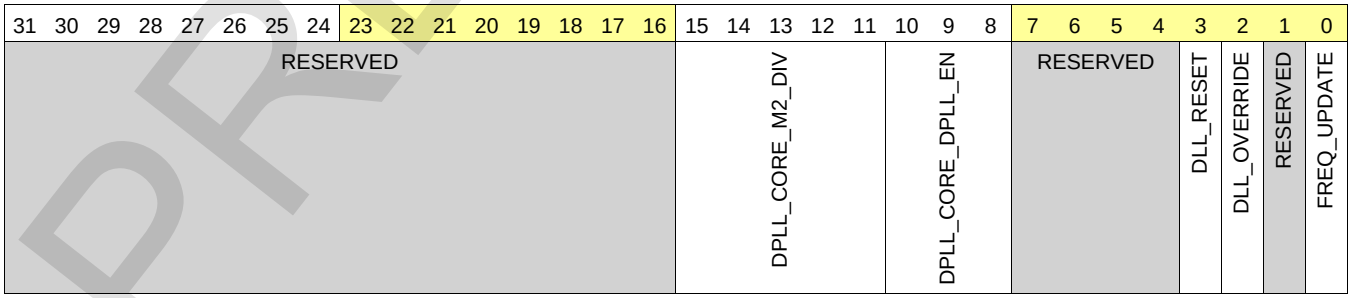
Table 3-982. Register Call Summary for Register CM_SSC_MODFREQDIV_DPLL_ABE

Clock Management Functional Description
- DPLL_ABE Description: [0] [1]

PRCM Register Manual
- CKGEN_CM1 Register Summary: [2]

Table 3-983. CM_SHADOW_FREQ_CONFIG1

Address Offset	0x0000 0160		
Physical Address	0x4A00 4260	**Instance**	CKGEN_CM1
Description	Shadow register to program new DPLL configuration affecting EMIF and GPMC (L3 clock) functional frequency during DVFS. The PRCM h/w automatically applies the new configuration after EMIF/GPMC have been put in idle state.		
Type	RW		



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Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x10D
15:11	DPLL_CORE_M2_DIV	Shadow register for CM_DIV_M2_DPLL_CORE.DPLL_CLKOUT_DIV. The main register is automatically loaded with the shadow register value after EMIF IDLE if the FREQ_UPDATE field is set to 1. Divide value from 1 to 31. 0x0: Reserved	RW	0x01
10:8	DPLL_CORE_DPLL_EN	Shadow register for CM_CLKMODE_DPLL_CORE.DPLL_EN. The main register is automatically loaded with the shadow register value after EMIF IDLE if the FREQ_UPDATE field is set to 1. 0x0: Reserved 0x1: Reserved 0x2: Reserved 0x3: Reserved 0x4: Put the DPLL in MN bypass mode. The DPLL_MULT register bits are reset to 0 automatically by putting the DPLL in this mode. 0x5: Put the DPLL in idle bypass low-power mode. 0x6: Put the DPLL in idle bypass fast-relock mode. 0x7: Enables the DPLL in lock mode	RW	0x5
7:4	RESERVED		R	0x0
3	DLL_RESET	Specify if DLL should be reset or not during the frequency change hardware sequence. 0x0: DLL is not reset during the frequency change hardware sequence 0x1: DLL is reset automatically during the frequency change hardware sequence	RW	1
2	DLL_OVERRIDE	Shadow register for CM_DLL_CTRL.DLL_OVERRIDE.The main register is automatically loaded with the shadow register value after EMIF IDLE if the FREQ_UPDATE field is set to 1. 0x0: Lock and code outputs are not overriden 0x1: Lock output is overriden to 1 and code output is overriden with a value coming from control module.	RW	1
1	RESERVED		RW	0
0	FREQ_UPDATE	Writing 1 indicates that a new configuration is available. It is automatically cleared by h/w after the configuration has been applied.	RW WSpecial	0

Table 3-984. Register Call Summary for Register CM_SHADOW_FREQ_CONFIG1

Clock Management Functional Description • DPLLs Cascading: [0] [1]
Device Low-Power States • Device Off Mode Wake-Up Sequences: [2]
PRCM Register Manual • CKGEN_CM1 Register Summary: [3] • CKGEN_CM1 Register Description: [4] [5] [6] • RESTORE_CM1 Register Description: [7] [8] [9] [10]

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Table 3-985. CM_SHADOW_FREQ_CONFIG2

Address Offset	0x0000 0164		
Physical Address	0x4A00 4264	**Instance**	CKGEN_CM1
Description	Shadow register to program new DPLL configuration affecting GPMC (L3 clock) functional frequency during DVFS. The PRCM h/w automatically applies the new configuration after EMIF/GPMC have been put in idle state.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								DPLL_CORE_M5_DIV					CLKSEL_L3	CLKSEL_CORE	GPMC_FREQ_UPDATE

Bits	Field Name	Description	Type	Reset
31:8	RESERVED		R	0x000000
7:3	DPLL_CORE_M5_DIV	Shadow register for CM_DIV_M5_DPLL_CORE.HSDIVIDER_CLKOUT2_DIV. The main register is automatically loaded with the shadow register value after GPMC IDLE if the CM_SHADOW_FREQ_CONFIG1.FREQ_UPDATE field is set to 1 and GPMC_FREQ_UPDATE is set to 1. Divide value from 1 to 31. 0x0: Reserved	RW	0x01
2	CLKSEL_L3	Shadow register for CM_CLKSEL_CORE.CLKSEL_L3. The main register is automatically loaded with the shadow register value after GPMC IDLE if the CM_SHADOW_FREQ_CONFIG1.FREQ_UPDATE field is set to 1 and GPMC_FREQ_UPDATE is set to 1. 0x0: L3_CLK is CORE_CLK divided by 1 0x1: L3_CLK is CORE_CLK divided by 2	RW	0
1	CLKSEL_CORE	Shadow register for CM_CLKSEL_CORE.CLKSEL_CORE. The main register is automatically loaded with the shadow register value after GPMC IDLE if the CM_SHADOW_FREQ_CONFIG1.FREQ_UPDATE field is set to 1 and GPMC_FREQ_UPDATE is set to 1. 0x0: CORE_CLK is CORE_X2_CLK divided by 1 0x1: CORE_CLK is CORE_X2_CLK divided by 2	RW	0
0	GPMC_FREQ_UPDATE	Controls whether or not GPMC has to be put automatically into idle during the frequency change operation. 0x0: GPMC is not put automatically into idle during frequency change operation. 0x1: GPMC is put automatically into idle during frequency change operation.	RW	0

Table 3-986. Register Call Summary for Register CM_SHADOW_FREQ_CONFIG2

Voltage Management Functional Description
- GPMC Clocks Frequency Scaling Constraints: [0]

PRCM Register Manual
- CKGEN_CM1 Register Summary: [1]
- RESTORE_CM1 Register Description: [2]

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Table 3-987. CM_DYN_DEP_PRESCAL

Address Offset	0x0000 0170		
Physical Address	0x4A00 4270	**Instance**	CKGEN_CM1
Description	Control the time unit of the sliding window for dynamic dependencies (auto-sleep feature).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								PRESCAL							

Bits	Field Name	Description	Type	Reset
31:6	RESERVED		R	0x0000000
5:0	PRESCAL	Time unit is equal to (PRESCAL + 1) L4 clock cycles.	RW	0x20

Table 3-988. Register Call Summary for Register CM_DYN_DEP_PRESCAL

Device Power Management Introduction

- Clock Management: [0]

PRCM Register Manual

- EMU_CM Register Description: [1]
- CKGEN_CM1 Register Summary: [2]
- MPU_CM1 Register Description: [3]
- DSP_CM1 Register Description: [4]
- RESTORE_CM1 Register Description: [5]
- CORE_CM2 Register Description: [6] [7] [8] [9] [10]
- L4PER_CM2 Register Description: [11]
- RESTORE_CM2 Register Description: [12] [13] [14] [15] [16]

Table 3-989. CM_RESTORE_ST

Address Offset	0x0000 0180		
Physical Address	0x4A00 4280	**Instance**	CKGEN_CM1
Description	Automatic restore status. This register is used by the system DMA to write a predefined value at the end of end automatic restore phase. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													PHASE2B_COMPLETED	PHASE2A_COMPLETED	PHASE1_COMPLETED

Bits	Field Name	Description	Type	Reset
31:3	RESERVED		R	0x0000 0000
2	PHASE2B_COMPLETED	Indicates if restore phase 2b is completed. Must be cleared by software before going to device OFF mode.	RW	0
1	PHASE2A_COMPLETED	Indicates if restore phase 2a is completed. Must be cleared by software before going to device OFF mode.	RW	0
0	PHASE1_COMPLETED	Indicates if restore phase 1 is completed. Must be cleared by software before going to device OFF mode.	RW	0

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Table 3-990. Register Call Summary for Register CM_RESTORE_ST

PRCM Register Manual
- CKGEN_CM1 Register Summary: [0]

3.11.24 MPU_CM1 Registers

3.11.24.1 MPU_CM1 Register Summary

Table 3-991. MPU_CM1 Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	MPU_CM1 L4 Base Address
CM_MPU_CLKSTCTRL	RW	32	0x0000 0000	0x4A00 4300
CM_MPU_STATICDEP	RW	32	0x0000 0004	0x4A00 4304
CM_MPU_DYNAMICDEP	RW	32	0x0000 0008	0x4A00 4308
CM_MPU_MPU_CLKCTRL	R	32	0x0000 0020	0x4A00 4320

3.11.24.2 MPU_CM1 Register Description

Table 3-992. CM_MPU_CLKSTCTRL

Address Offset	0x0000 0000		
Physical Address	0x4A00 4300	**Instance**	MPU_CM1
Description	This register enables the MPU domain power state transition. It controls the hardware supervised domain power state transition between ON-ACTIVE and ON-INACTIVE states. It also holds 1 status bit per clock input of the domain.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							CLKACTIVITY_MPU_DPLL_CLK	RESERVED						CLKTRCTRL	

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	CLKACTIVITY_MPU_DPLL_CLK	This field indicates the state of the MPU_DPLL_CLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
7:2	RESERVED		R	0x00

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Bits	Field Name	Description	Type	Reset
1:0	CLKTRCTRL	Controls the clock state transition of the MPU clock domain. 0x0: NO_SLEEP: Sleep transition cannot be initiated. Wakeup transition may however occur. Read 0x1: Reserved 0x2: SW_WKUP: Start a software forced wake-up transition on the domain. 0x3: HW_AUTO: Automatic transition is enabled. Sleep and wakeup transition are based upon hardware conditions.	RW	0x0

Table 3-993. Register Call Summary for Register CM_MPU_CLKSTCTRL

Clock Management Functional Description • Clock Domain Modes: [0] [1]
PRCM Register Manual • MPU_CM1 Register Summary: [2] • RESTORE_CM1 Register Description: [3]

Table 3-994. CM_MPU_STATICDEP

Address Offset	0x0000 0004		
Physical Address	0x4A00 4304	**Instance**	MPU_CM1
Description	This register controls the static domain depedencies from MPU domain towards 'target' domains. It is relevant only for domain having system initiator(s).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													C2C_STATDEP	RESERVED	ALWONCORE_STATDEP	L4WKUP_STATDEP	RESERVED	L4PER_STATDEP	L4CFG_STATDEP	SDMA_STATDEP	SGX_STATDEP	ISS_STATDEP	DSS_STATDEP	L3INIT_STATDEP	L3_2_STATDEP	L3_1_STATDEP	MEMIF_STATDEP	ABE_STATDEP	IVAHD_STATDEP	DSP_STATDEP	MPU_M3_STATDEP

Bits	Field Name	Description	Type	Reset
31:19	RESERVED		R	0x0000
18	C2C_STATDEP	Static dependency towards C2C clock domain Read 0x0: Dependency is disabled	R	0
17	RESERVED		R	0
16	ALWONCORE_STATDEP	Static dependency towards ALWONCORE clock domain Read 0x0: Dependency is disabled	R	0
15	L4WKUP_STATDEP	Static dependency towards L4WKUP clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	1
14	RESERVED		R	0
13	L4PER_STATDEP	Static dependency towards L4PER clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	1

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Bits	Field Name	Description	Type	Reset
12	L4CFG_STATDEP	Static dependency towards L4CFG clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	1
11	SDMA_STATDEP	Static dependency towards SDMA clock domain Read 0x0: Dependency is disabled	R	0
10	SGX_STATDEP	Static dependency towards SGX clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
9	ISS_STATDEP	Static dependency towards ISS clock domain Read 0x0: Dependency is disabled	R	0
8	DSS_STATDEP	Static dependency towards DSS clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
7	L3INIT_STATDEP	Static dependency towards L3INIT clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	1
6	L3_2_STATDEP	Static dependency towards L3_2 clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	1
5	L3_1_STATDEP	Static dependency towards L3_1 clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	1
4	MEMIF_STATDEP	Static dependency towards MEMIF clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	1
3	ABE_STATDEP	Static dependency towards ABE clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
2	IVAHD_STATDEP	Static dependency towards IVAHD clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
1	DSP_STATDEP	Static dependency towards DSP clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
0	MPU_M3_STATDEP	Static dependency towards MPU_A3 clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-995. Register Call Summary for Register CM_MPU_STATICDEP

Clock Management Functional Description • Clock Domain Dependency: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14]
PRCM Register Manual • MPU_CM1 Register Summary: [15]

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Table 3-996. CM_MPU_DYNAMICDEP

Address Offset	0x0000 0008		
Physical Address	0x4A00 4308	**Instance**	MPU_CM1
Description	This register controls the dynamic domain depedencies from MPU domain towards 'target' domains. It is relevant only for domain having INTRCONN master port(s).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				WINDOWSIZE				RESERVED																		L3_1_DYNDEP	MEMIF_DYNDEP	ABE_DYNDEP	RESERVED			

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:24	WINDOWSIZE	Size of sliding window used to monitor INTRCONN interface activity for determination of auto-sleep feature. Time unit defined by CM_DYN_DEP_PRESCAL register.	RW	0x4
23:6	RESERVED		R	0x00000
5	L3_1_DYNDEP	Dynamic dependency towards L3_1 clock domain Read 0x1: Dependency is enabled	R Rreturns 1s	1
4	MEMIF_DYNDEP	Dynamic dependency towards MEMIF clock domain Read 0x1: Dependency is enabled	R Rreturns 1s	1
3	ABE_DYNDEP	Dynamic dependency towards ABE clock domain Read 0x1: Dependency is enabled	R Rreturns 1s	1
2:0	RESERVED		R	0x0

Table 3-997. Register Call Summary for Register CM_MPU_DYNAMICDEP

Clock Management Functional Description • Clock Domain Dependency: [0] [1] [2]
PRCM Register Manual • MPU_CM1 Register Summary: [3]

Table 3-998. CM_MPU_MPU_CLKCTRL

Address Offset	0x0000 0020		
Physical Address	0x4A00 4320	**Instance**	MPU_CM1
Description	This register manages the MPU clocks.		
Type	R		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						CLKSEL_ABE_DIV_MODE	CLKSEL_EMIF_DIV_MODE	RESERVED					STBYST	IDLEST		RESERVED															MODULEMODE

Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x00
25	CLKSEL_ABE_DIV_MODE	Selects the ratio for MPU-ABE async bridge versus MPU DPLL clock. 0x0: MPU DPLL clock divided by 4 0x1: MPU DPLL clock divided by 8	RW	0
24	CLKSEL_EMIF_DIV_MODE	Selects the ratio for memory adapter clock (MA_EOCP_ICLK) versus MPU DPLL clock. 0x0: MPU DPLL clock divided by 2 0x1: MPU DPLL clock divided by 4	RW	0
23:19	RESERVED		R	0x00
18	STBYST	Module standby status. [warm reset insensitive] Read 0x0: Module is functional (not in standby) Read 0x1: Module is in standby	R	1
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in Idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. Read 0x1: Module is managed automatically by hardware according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. Module clocks may be gated according to the clock domain state.	R Rreturns	0x1

Table 3-999. Register Call Summary for Register CM_MPU_MPU_CLKCTRL

Clock Management Functional Description
- DPLL_MPU Description: [0] [1] [2]
- Clock Domain Module Attributes: [3] [4] [5]

PRCM Register Manual
- MPU_CM1 Register Summary: [6]

3.11.25 DSP_CM1 Registers

3.11.25.1 DSP_CM1 Register Summary

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Table 3-1000. DSP_CM1 Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	DSP_CM1 L4 Base Address
CM_DSP_CLKSTCTRL	RW	32	0x0000 0000	0x4A00 4400
CM_DSP_STATICDEP	RW	32	0x0000 0004	0x4A00 4404
CM_DSP_DYNAMICDEP	RW	32	0x0000 0008	0x4A00 4408
CM_DSP_DSP_CLKCTRL	RW	32	0x0000 0020	0x4A00 4420

3.11.25.2 DSP_CM1 Register Description

Table 3-1001. CM_DSP_CLKSTCTRL

Address Offset	0x0000 0000		
Physical Address	0x4A00 4400	**Instance**	DSP_CM1
Description	This register enables the DSP domain power state transition. It controls the hardware supervised domain power state transition between ON-ACTIVE and ON-INACTIVE states. It also holds 1 status bit per clock input of the domain.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							CLKACTIVITY_DSP_ROOT_CLK	RESERVED						CLKTRCTRL	

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	CLKACTIVITY_DSP_ROOT_CLK	This field indicates the state of the DSP_ROOT_CLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
7:2	RESERVED		R	0x00
1:0	CLKTRCTRL	Controls the clock state transition of the DSP clock domain. 0x0: NO_SLEEP: Sleep transition cannot be initiated. Wakeup transition may however occur. 0x1: SW_SLEEP: Start a software forced sleep transition on the domain. 0x2: SW_WKUP: Start a software forced wake-up transition on the domain. 0x3: HW_AUTO: Automatic transition is enabled. Sleep and wakeup transition are based upon hardware conditions.	RW	0x3

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Table 3-1002. Register Call Summary for Register CM_DSP_CLKSTCTRL

Reset Management Functional Description • DSP Subsystem Power-On Reset Sequence: [0]
Clock Management Functional Description • Clock Domain Modes: [1] [2]
PRCM Register Manual • DSP_CM1 Register Summary: [3]

Table 3-1003. CM_DSP_STATICDEP

Address Offset	0x0000 0004		
Physical Address	0x4A00 4404	**Instance**	DSP_CM1
Description	This register controls the static domain depedencies from DSP domain towards 'target' domains. It is relevant only for domain having system initiator(s).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															ALWONCORE_STATDEP	L4WKUP_STATDEP	RESERVED	L4PER_STATDEP	L4CFG_STATDEP	RESERVED		ISS_STATDEP	RESERVED	L3INIT_STATDEP	L3_2_STATDEP	L3_1_STATDEP	MEMIF_STATDEP	ABE_STATDEP	IVAHD_STATDEP	RESERVED	

Bits	Field Name	Description	Type	Reset
31:17	RESERVED		R	0x0000
16	ALWONCORE_STATDEP	Static dependency towards ALWONCORE clock domain Read 0x0: Dependency is disabled	R	0
15	L4WKUP_STATDEP	Static dependency towards L4WKUP clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
14	RESERVED		R	0
13	L4PER_STATDEP	Static dependency towards L4PER clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
12	L4CFG_STATDEP	Static dependency towards L4CFG clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
11:10	RESERVED		R	0x0
9	ISS_STATDEP	Static dependency towards ISS clock domain Read 0x0: Dependency is disabled	R	0
8	RESERVED		R	0
7	L3INIT_STATDEP	Static dependency towards L3INIT clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
6	L3_2_STATDEP	Static dependency towards L3_2 clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

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Bits	Field Name	Description	Type	Reset
5	L3_1_STATDEP	Static dependency towards L3_1 clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
4	MEMIF_STATDEP	Static dependency towards MEMIF clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
3	ABE_STATDEP	Static dependency towards ABE clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
2	IVAHD_STATDEP	Static dependency towards IVAHD clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
1:0	RESERVED		R	0x0

Table 3-1004. Register Call Summary for Register CM_DSP_STATICDEP

Clock Management Functional Description • Clock Domain Dependency: [0] [1] [2] [3] [4] [5] [6] [7] [8]
PRCM Register Manual • DSP_CM1 Register Summary: [9]

Table 3-1005. CM_DSP_DYNAMICDEP

Address Offset	0x0000 0008		
Physical Address	0x4A00 4408	**Instance**	DSP_CM1
Description	This register controls the dynamic domain depedencies from DSP domain towards 'target' domains. It is relevant only for domain having INTRCONN master port(s).		
Type	RW		

31 30 29 28	27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6	5	4	3	2	1 0
RESERVED	WINDOWSIZE	RESERVED			L3_1_DYNDEP	RESERVED	ABE_DYNDEP	IVAHD_DYNDEP	RESERVED

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:24	WINDOWSIZE	Size of sliding window used to monitor INTRCONN interface activity for determination of auto-sleep feature. Time unit defined by CM_DYN_DEP_PRESCAL register.	RW	0x4
23:6	RESERVED		R	0x00000
5	L3_1_DYNDEP	Dynamic dependency towards L3_1 clock domain Read 0x1: Dependency is enabled	R Rreturns 1s	1
4	RESERVED		R	0
3	ABE_DYNDEP	Dynamic dependency towards ABE clock domain Read 0x1: Dependency is enabled	R Rreturns 1s	1
2	IVAHD_DYNDEP	Dynamic dependency towards IVAHD clock domain Read 0x1: Dependency is enabled	R Rreturns 1s	1
1:0	RESERVED		R	0x0

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Table 3-1006. Register Call Summary for Register CM_DSP_DYNAMICDEP

Clock Management Functional Description • Clock Domain Dependency: [0] [1] [2]
PRCM Register Manual • DSP_CM1 Register Summary: [3]

Table 3-1007. CM_DSP_DSP_CLKCTRL

Address Offset	0x0000 0020		
Physical Address	0x4A00 4420	**Instance**	DSP_CM1
Description	This register manages the DSP clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													STBYST	IDLEST		RESERVED														MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:19	RESERVED		R	0x0000
18	STBYST	Module standby status. [warm reset insensitive] Read 0x0: Module is functional (not in standby) Read 0x1: Module is in standby	R	1
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in Idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by software. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). 0x1: Module is managed automatically by hardware according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CLKTRCTRL=3, any INTRCONN access to module is always granted. Module clocks may be gated according to the clock domain state. Read 0x2: Reserved Read 0x3: Reserved	RW	0x0

Table 3-1008. Register Call Summary for Register CM_DSP_DSP_CLKCTRL

Reset Management Functional Description • DSP Subsystem Power-On Reset Sequence: [0]
Clock Management Functional Description • Clock Domain Module Attributes: [1] [2] [3]
PRCM Register Manual • DSP_CM1 Register Summary: [4]

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3.11.26 ABE_CM1 Registers

3.11.26.1 ABE_CM1 Register Summary

Table 3-1009. ABE_CM1 Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	ABE_CM1 L4 Base Address
CM1_ABE_CLKSTCTRL	RW	32	0x0000 0000	0x4A00 4500
CM1_ABE_L4ABE_CLKCTRL	R	32	0x0000 0020	0x4A00 4520
CM1_ABE_AESS_CLKCTRL	RW	32	0x0000 0028	0x4A00 4528
CM1_ABE_PDM_CLKCTRL	RW	32	0x0000 0030	0x4A00 4530
CM1_ABE_DMIC_CLKCTRL	RW	32	0x0000 0038	0x4A00 4538
CM1_ABE_MCASP_CLKCTRL	RW	32	0x0000 0040	0x4A00 4540
CM1_ABE_MCBSP1_CLKCTRL	RW	32	0x0000 0048	0x4A00 4548
CM1_ABE_MCBSP2_CLKCTRL	RW	32	0x0000 0050	0x4A00 4550
CM1_ABE_MCBSP3_CLKCTRL	RW	32	0x0000 0058	0x4A00 4558
CM1_ABE_SLIMBUS_CLKCTRL	RW	32	0x0000 0060	0x4A00 4560
CM1_ABE_GPTIMER5_CLKCTRL	RW	32	0x0000 0068	0x4A00 4568
CM1_ABE_GPTIMER6_CLKCTRL	RW	32	0x0000 0070	0x4A00 4570
CM1_ABE_GPTIMER7_CLKCTRL	RW	32	0x0000 0078	0x4A00 4578
CM1_ABE_GPTIMER8_CLKCTRL	RW	32	0x0000 0080	0x4A00 4580
CM1_ABE_WDTIMER3_CLKCTRL	RW	32	0x0000 0088	0x4A00 4588

3.11.26.2 ABE_CM1 Register Description

Table 3-1010. CM1_ABE_CLKSTCTRL

Address Offset	0x0000 0000		
Physical Address	0x4A00 4500	**Instance**	ABE_CM1
Description	This register enables the ABE domain power state transition. It controls the hardware supervised domain power state transition between ON-ACTIVE and ON-INACTIVE states. It also holds 1 status bit per clock input of the domain.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																		CLKACTIVITY_ABE_24M_FCLK	CLKACTIVITY_ABE_ALWON_32K_CLK	CLKACTIVITY_ABE_SYSCLK	CLKACTIVITY_24M_FCLK	CLKACTIVITY_ABE_ICLK2	CLKACTIVITY_DPLL_ABE_X2_CLK	RESERVED						CLKTRCTRL	

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Bits	Field Name	Description	Type	Reset
31:14	RESERVED		R	0x00000
13	CLKACTIVITY_ABE_24M_FCLK	This field indicates the state of the ABE_24M_FCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
12	CLKACTIVITY_ABE_ALWON_32K_CLK	This field indicates the state of the ABE_ALWON_32K_CLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
11	CLKACTIVITY_ABE_SYSCLK	This field indicates the state of the ABE_SYSCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
10	CLKACTIVITY_24M_FCLK	This field indicates the state of the 24M_FCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
9	CLKACTIVITY_ABE_ICLK2	This field indicates the state of the ABE_ICLK2 interface clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
8	CLKACTIVITY_DPLL_ABE_X2_CLK	This field indicates the state of the DPLL_ABE_X2_CLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
7:2	RESERVED		R	0x00
1:0	CLKTRCTRL	Controls the clock state transition of the ABE clock domain. 0x0: NO_SLEEP: Sleep transition cannot be initiated. Wakeup transition may however occur. 0x1: SW_SLEEP: Start a software forced sleep transition on the domain. 0x2: SW_WKUP: Start a software forced wake-up transition on the domain. 0x3: HW_AUTO: Automatic transition is enabled. Sleep and wakeup transition are based upon hardware conditions.	RW	0x3

Table 3-1011. Register Call Summary for Register CM1_ABE_CLKSTCTRL

Clock Management Functional Description • Clock Domain Modes: [0] [1] [2] [3] [4] [5] [6]
PRCM Register Manual • ABE_CM1 Register Summary: [7]

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Table 3-1012. CM1_ABE_L4ABE_CLKCTRL

Address Offset	0x0000 0020		
Physical Address	0x4A00 4520	**Instance**	ABE_CM1
Description	This register manages the L4ABE clocks.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED														MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in Idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. Read 0x1: Module is managed automatically by hardware according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CLKTRCTRL=3, any INTRCONN access to module is always granted. Module clocks may be gated according to the clock domain state.	R Rreturns	0x1

Table 3-1013. Register Call Summary for Register CM1_ABE_L4ABE_CLKCTRL

Clock Management Functional Description
- Clock Domain Module Attributes: [0] [1]

PRCM Register Manual
- ABE_CM1 Register Summary: [2]

Table 3-1014. CM1_ABE_AESS_CLKCTRL

Address Offset	0x0000 0028		
Physical Address	0x4A00 4528	**Instance**	ABE_CM1
Description	This register manages the AESS clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							CLKSEL_AESS_FCLK	RESERVED					STBYST	IDLEST		RESERVED														MODULEMODE	

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Bits	Field Name	Description	Type	Reset
31:25	RESERVED		R	0x00
24	CLKSEL_AESS_FCLK	Selects the ratio of AESS_FCLK to ABE_CLK 0x0: AESS_FCLK is divide by 1 of ABE_CLK 0x1: AESS_FCLK is divide by 2 of ABE_CLK	RW	0
23:19	RESERVED		R	0x00
18	STBYST	Module standby status. [warm reset insensitive] Read 0x0: Module is functional (not in standby) Read 0x1: Module is in standby	R	1
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in Idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by software. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen. Read 0x3: Reserved	RW	0x0

Table 3-1015. Register Call Summary for Register CM1_ABE_AESS_CLKCTRL

Clock Management Functional Description • CM Clock Source: [0] [1] • Clock Domain Module Attributes: [2] [3] [4]
PRCM Register Manual • ABE_CM1 Register Summary: [5]

Table 3-1016. CM1_ABE_PDM_CLKCTRL

Address Offset	0x0000 0030		
Physical Address	0x4A00 4530	**Instance**	ABE_CM1
Description	This register manages the PDM clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED														MODULEMODE	

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Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in Idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by software. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen. Read 0x3: Reserved	RW	0x0

Table 3-1017. Register Call Summary for Register CM1_ABE_PDM_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • ABE_CM1 Register Summary: [2]

Table 3-1018. CM1_ABE_DMIC_CLKCTRL

Address Offset	0x0000 0038		
Physical Address	0x4A00 4538	**Instance**	ABE_CM1
Description	This register manages the DMIC clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CLKSEL_INTERNAL_SOURCE		CLKSEL_SOURCE		RESERVED						IDLEST		RESERVED														MODULEMODE	

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Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:26	CLKSEL_INTERNAL_SOURCE	Selects the internal clock to be used as the functional clock in case CLKSEL_SOURCE selects the internal clock source as the functional clock source. 0x0: 24MHz clock derived from DPLL_ABE is selected 0x1: ABE_SYSCLK is selected 0x2: 24MHz clock derived from DPLL_PER is selected 0x3: Reserved	RW	0x0
25:24	CLKSEL_SOURCE	Selects the source of the functional clock between, internal source, CLKS pad and Audio SLIMBUS_CLK pad. The switching between the clocks is not guaranteed to be glitchless. 0x0: Functional clock is sourced from an internal clock 0x1: Functional clock is sourced from CLKS pad 0x2: Functional clock is sourced from Audio SIMBUS pad 0x3: Reserved	RW	0x0
23:18	RESERVED		R	0x00
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in Idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by software. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen. Read 0x3: Reserved	RW	0x0

Table 3-1019. Register Call Summary for Register CM1_ABE_DMIC_CLKCTRL

Clock Management Functional Description • CM Clock Source: [0] [1] • Clock Domain Module Attributes: [2] [3]
PRCM Register Manual • ABE_CM1 Register Summary: [4]

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Table 3-1020. CM1_ABE_MCASP_CLKCTRL

Address Offset	0x0000 0040		
Physical Address	0x4A00 4540	**Instance**	ABE_CM1
Description	This register manages the MCASP clocks.		
Type	RW		

31 30 29 28	27 26	25 24	23 22 21 20 19 18	17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2	1 0
RESERVED	CLKSEL_INTERNAL_SOURCE	CLKSEL_SOURCE	RESERVED	IDLEST	RESERVED		MODULEMODE

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:26	CLKSEL_INTERNAL_SOURCE	Selects the internal clock to be used as the functional clock in case CLKSEL_SOURCE selects the internal clock source as the functional clock source. 0x0: 24MHz clock derived from DPLL_ABE is selected 0x1: ABE_SYSCLK is selected 0x2: 24MHz clock derived from DPLL_PER is selected 0x3: Reserved	RW	0x0
25:24	CLKSEL_SOURCE	Selects the source of the functional clock between, internal source, CLKS pad and Audio SLIMBUS_CLK pad. The switching between the clocks is not guaranteed to be glitchless. 0x0: Functional clock is sourced from an internal clock 0x1: Functional clock is sourced from CLKS pad 0x2: Functional clock is sourced from Audio SIMBUS pad 0x3: Reserved	RW	0x0
23:18	RESERVED		R	0x00
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in Idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000

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Bits	Field Name	Description	Type	Reset
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by software. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen. Read 0x3: Reserved	RW	0x0

Table 3-1021. Register Call Summary for Register CM1_ABE_MCASP_CLKCTRL

Clock Management Functional Description
- CM Clock Source: [0] [1]
- Clock Domain Module Attributes: [2] [3]

PRCM Register Manual
- ABE_CM1 Register Summary: [4]

Table 3-1022. CM1_ABE_MCBSP1_CLKCTRL

Address Offset	0x0000 0048		
Physical Address	0x4A00 4548	**Instance**	ABE_CM1
Description	This register manages the MCBSP1 clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CLKSEL_INTERNAL_SOURCE		CLKSEL_SOURCE		RESERVED						IDLEST		RESERVED														MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:26	CLKSEL_INTERNAL_SOURCE	Selects the internal clock to be used as the functional clock in case CLKSEL_SOURCE selects the internal clock source as the functional clock source. 0x0: 24MHz clock derived from DPLL_ABE is selected 0x1: ABE_SYSCLK is selected 0x2: 24MHz clock derived from DPLL_PER is selected 0x3: Reserved	RW	0x0

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Bits	Field Name	Description	Type	Reset
25:24	CLKSEL_SOURCE	Selects the source of the functional clock between, internal source, CLKS pad and Audio SLIMBUS_CLK pad. The switching between the clocks is not guaranteed to be glitchless. 0x0: Functional clock is sourced from an internal clock 0x1: Functional clock is sourced from CLKS pad 0x2: Functional clock is sourced from Audio SIMBUS pad 0x3: Reserved	RW	0x0
23:18	RESERVED		R	0x00
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in Idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by software. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen. Read 0x3: Reserved	RW	0x0

Table 3-1023. Register Call Summary for Register CM1_ABE_MCBSP1_CLKCTRL

Clock Management Functional Description • CM Clock Source: [0] [1] • Clock Domain Module Attributes: [2] [3]
PRCM Register Manual • ABE_CM1 Register Summary: [4]

Table 3-1024. CM1_ABE_MCBSP2_CLKCTRL

Address Offset	0x0000 0050		
Physical Address	0x4A00 4550	**Instance**	ABE_CM1
Description	This register manages the MCBSP2 clocks.		
Type	RW		

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31 30 29 28	27 26	25 24	23 22 21 20 19 18	17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2	1 0
RESERVED	CLKSEL_INTERNAL_SOURCE	CLKSEL_SOURCE	RESERVED	IDLEST	RESERVED		MODULEMODE

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:26	CLKSEL_INTERNAL_SOURCE	Selects the internal clock to be used as the functional clock in case CLKSEL_SOURCE selects the internal clock source as the functional clock source. 0x0: 24MHz clock derived from DPLL_ABE is selected 0x1: ABE_SYSCLK is selected 0x2: 24MHz clock derived from DPLL_PER is selected 0x3: Reserved	RW	0x0
25:24	CLKSEL_SOURCE	Selects the source of the functional clock between, internal source, CLKS pad and Audio SLIMBUS_CLK pad. The switching between the clocks is not guaranteed to be glitchless. 0x0: Functional clock is sourced from an internal clock 0x1: Functional clock is sourced from CLKS pad 0x2: Functional clock is sourced from Audio SIMBUS pad 0x3: Reserved	RW	0x0
23:18	RESERVED		R	0x00
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in Idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by software. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen. Read 0x3: Reserved	RW	0x0

Table 3-1025. Register Call Summary for Register CM1_ABE_MCBSP2_CLKCTRL

Clock Management Functional Description

- CM Clock Source: [0] [1]
- Clock Domain Module Attributes: [2] [3]

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Table 3-1025. Register Call Summary for Register CM1_ABE_MCBSP2_CLKCTRL (continued)

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- ABE_CM1 Register Summary: [4]

Table 3-1026. CM1_ABE_MCBSP3_CLKCTRL

Address Offset	0x0000 0058		
Physical Address	0x4A00 4558	**Instance**	ABE_CM1
Description	This register manages the MCBSP3 clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CLKSEL_INTERNAL_SOURCE		CLKSEL_SOURCE		RESERVED						IDLEST		RESERVED														MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:26	CLKSEL_INTERNAL_SOURCE	Selects the internal clock to be used as the functional clock in case CLKSEL_SOURCE selects the internal clock source as the functional clock source. 0x0: 24MHz clock derived from DPLL_ABE is selected 0x1: ABE_SYSCLK is selected 0x2: 24MHz clock derived from DPLL_PER is selected 0x3: Reserved	RW	0x0
25:24	CLKSEL_SOURCE	Selects the source of the functional clock between, internal source, CLKS pad and Audio SLIMBUS_CLK pad. The switching between the clocks is not guaranteed to be glitchless. 0x0: Functional clock is sourced from an internal clock 0x1: Functional clock is sourced from CLKS pad 0x2: Functional clock is sourced from Audio SIMBUS pad 0x3: Reserved	RW	0x0
23:18	RESERVED		R	0x00
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in Idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000

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Bits	Field Name	Description	Type	Reset
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by software. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen. Read 0x3: Reserved	RW	0x0

Table 3-1027. Register Call Summary for Register CM1_ABE_MCBSP3_CLKCTRL

Clock Management Functional Description
- CM Clock Source: [0] [1]
- Clock Domain Module Attributes: [2] [3]

PRCM Register Manual
- ABE_CM1 Register Summary: [4]

Table 3-1028. CM1_ABE_SLIMBUS_CLKCTRL

Address Offset	0x0000 0060		
Physical Address	0x4A00 4560	**Instance**	ABE_CM1
Description	This register manages the SLIMBUS clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED				OPTFCLKEN_SLIMBUS_CLK	OPTFCLKEN_FCLK2	OPTFCLKEN_FCLK1	OPTFCLKEN_FCLK0	RESERVED						MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in Idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:12	RESERVED		R	0x0
11	OPTFCLKEN_SLIMBUS_CLK	Optional functional clock control. 0x0: Optional functional clock is disabled 0x1: Optional functional clock is enabled	RW	0

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Bits	Field Name	Description	Type	Reset
10	OPTFCLKEN_FCLK2	Optional functional clock control. 0x0: Optional functional clock is disabled 0x1: Optional functional clock is enabled	RW	0
9	OPTFCLKEN_FCLK1	Optional functional clock control. 0x0: Optional functional clock is disabled 0x1: Optional functional clock is enabled	RW	0
8	OPTFCLKEN_FCLK0	Optional functional clock control. 0x0: Optional functional clock is disabled 0x1: Optional functional clock is enabled	RW	0
7:2	RESERVED		R	0x00
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by software. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen. Read 0x3: Reserved	RW	0x0

Table 3-1029. Register Call Summary for Register CM1_ABE_SLIMBUS_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • ABE_CM1 Register Summary: [2]

Table 3-1030. CM1_ABE_GPTIMER5_CLKCTRL

Address Offset	0x0000 0068		
Physical Address	0x4A00 4568	**Instance**	ABE_CM1
Description	This register manages the TIMER5 clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							CLKSEL	RESERVED						IDLEST		RESERVED															MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:25	RESERVED		R	0x00
24	CLKSEL	Selects between ABE_SYSCLK and ABE_ALWON_32K_CLK as the timer functional clock 0x0: Selects ABE_SYSCLK as the functional clock 0x1: Selects ABE_ALWON_32K_CLK as the functional clock	RW	0
23:18	RESERVED		R	0x00

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Bits	Field Name	Description	Type	Reset
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in Idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by software. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen. Read 0x3: Reserved	RW	0x0

Table 3-1031. Register Call Summary for Register CM1_ABE_GPTIMER5_CLKCTRL

Clock Management Functional Description • CM Clock Source: [0] • Clock Domain Module Attributes: [1] [2]
PRCM Register Manual • ABE_CM1 Register Summary: [3]

Table 3-1032. CM1_ABE_GPTIMER6_CLKCTRL

Address Offset	0x0000 0070		
Physical Address	0x4A00 4570	**Instance**	ABE_CM1
Description	This register manages the TIMER6 clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							CLKSEL	RESERVED						IDLEST		RESERVED								MODULEMODE							

Bits	Field Name	Description	Type	Reset
31:25	RESERVED		R	0x00
24	CLKSEL	Selects between ABE_SYSCLK and ABE_ALWON_32K_CLK as the timer functional clock 0x0: Selects ABE_SYSCLK as the functional clock 0x1: Selects ABE_ALWON_32K_CLK as the functional clock	RW	0
23:18	RESERVED		R	0x00

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Bits	Field Name	Description	Type	Reset
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in Idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by software. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen. Read 0x3: Reserved	RW	0x0

Table 3-1033. Register Call Summary for Register CM1_ABE_GPTIMER6_CLKCTRL

Clock Management Functional Description • CM Clock Source: [0] • Clock Domain Module Attributes: [1] [2]
PRCM Register Manual • ABE_CM1 Register Summary: [3]

Table 3-1034. CM1_ABE_GPTIMER7_CLKCTRL

Address Offset	0x0000 0078		
Physical Address	0x4A00 4578	**Instance**	ABE_CM1
Description	This register manages the TIMER7 clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							CLKSEL	RESERVED						IDLEST		RESERVED								MODULEMODE							

Bits	Field Name	Description	Type	Reset
31:25	RESERVED		R	0x00
24	CLKSEL	Selects between ABE_SYSCLK and ABE_ALWON_32K_CLK as the timer functional clock 0x0: Selects ABE_SYSCLK as the functional clock 0x1: Selects ABE_ALWON_32K_CLK as the functional clock	RW	0
23:18	RESERVED		R	0x00

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Bits	Field Name	Description	Type	Reset
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in Idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by software. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen. Read 0x3: Reserved	RW	0x0

Table 3-1035. Register Call Summary for Register CM1_ABE_GPTIMER7_CLKCTRL

Clock Management Functional Description • CM Clock Source: [0] • Clock Domain Module Attributes: [1] [2]
PRCM Register Manual • ABE_CM1 Register Summary: [3]

Table 3-1036. CM1_ABE_GPTIMER8_CLKCTRL

Address Offset	0x0000 0080		
Physical Address	0x4A00 4580	**Instance**	ABE_CM1
Description	This register manages the TIMER8 clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							CLKSEL	RESERVED						IDLEST		RESERVED								MODULEMODE							

Bits	Field Name	Description	Type	Reset
31:25	RESERVED		R	0x00
24	CLKSEL	Selects between ABE_SYSCLK and ABE_ALWON_32K_CLK as the timer functional clock 0x0: Selects ABE_SYSCLK as the functional clock 0x1: Selects ABE_ALWON_32K_CLK as the functional clock	RW	0
23:18	RESERVED		R	0x00

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Bits	Field Name	Description	Type	Reset
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in Idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by software. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen. Read 0x3: Reserved	RW	0x0

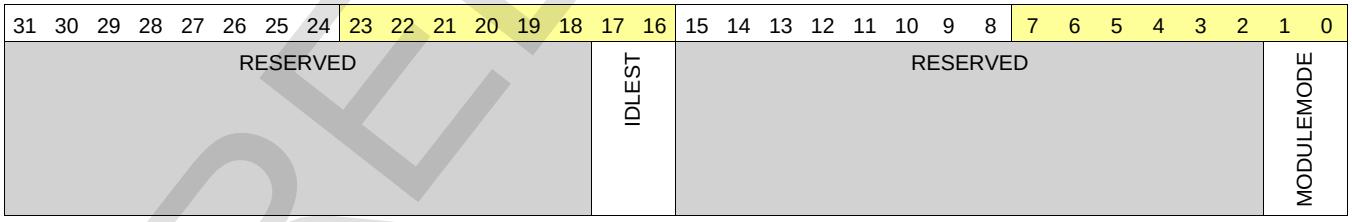
Table 3-1037. Register Call Summary for Register CM1_ABE_GPTIMER8_CLKCTRL

Clock Management Functional Description
- CM Clock Source: [0]
- Clock Domain Module Attributes: [1] [2]

PRCM Register Manual
- ABE_CM1 Register Summary: [3]

Table 3-1038. CM1_ABE_WDTIMER3_CLKCTRL

Address Offset	0x0000 0088		
Physical Address	0x4A00 4588	**Instance**	ABE_CM1
Description	This register manages the WDT3 clocks.		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in Idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000

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Bits	Field Name	Description	Type	Reset
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by software. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen. Read 0x3: Reserved	RW	0x0

Table 3-1039. Register Call Summary for Register CM1_ABE_WDTIMER3_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • ABE_CM1 Register Summary: [2]

3.11.27 RESTORE_CM1 Registers

3.11.27.1 RESTORE_CM1 Register Summary

Table 3-1040. RESTORE_CM1 Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	RESTORE_CM1 L4 Base Address
CM_CLKSEL_CORE_RESTORE	RW	32	0x0000 0000	0x4A00 4E00
CM_DIV_M2_DPLL_CORE_RESTORE	RW	32	0x0000 0004	0x4A00 4E04
CM_DIV_M3_DPLL_CORE_RESTORE	RW	32	0x0000 0008	0x4A00 4E08
CM_DIV_M4_DPLL_CORE_RESTORE	RW	32	0x0000 000C	0x4A00 4E0C
CM_DIV_M5_DPLL_CORE_RESTORE	RW	32	0x0000 0010	0x4A00 4E10
CM_DIV_M6_DPLL_CORE_RESTORE	RW	32	0x0000 0014	0x4A00 4E14
CM_DIV_M7_DPLL_CORE_RESTORE	RW	32	0x0000 0018	0x4A00 4E18
CM_CLKSEL_DPLL_CORE_RESTORE	RW	32	0x0000 001C	0x4A00 4E1C
CM_SSC_DELTAMSTEP_DPLL_CORE_RESTORE	RW	32	0x0000 0020	0x4A00 4E20
CM_SSC_MODFREQDIV_DPLL_CORE_RESTORE	RW	32	0x0000 0024	0x4A00 4E24
CM_CLKMODE_DPLL_CORE_RESTORE	RW	32	0x0000 0028	0x4A00 4E28
CM_SHADOW_FREQ_CONFIG2_RESTORE	RW	32	0x0000 002C	0x4A00 4E2C
CM_SHADOW_FREQ_CONFIG1_RESTORE	RW	32	0x0000 0030	0x4A00 4E30
CM_AUTOIDLE_DPLL_CORE_RESTORE	RW	32	0x0000 0034	0x4A00 4E34
CM_MPU_CLKSTCTRL_RESTORE	RW	32	0x0000 0038	0x4A00 4E38
CM_CM1_PROFILING_CLKCTRL_RESTORE	RW	32	0x0000 003C	0x4A00 4E3C
CM_DYN_DEP_PRESCAL_RESTORE	RW	32	0x0000 0040	0x4A00 4E40
RESERVED	RW	32	0x0000 0044	0x4A00 4E44
RESERVED	RW	32	0x0000 0048	0x4A00 4E48
RESERVED	RW	32	0x0000 004C	0x4A00 4E4C
RESERVED	RW	32	0x0000 0050	0x4A00 4E50
RESERVED	RW	32	0x0000 0054	0x4A00 4E54
RESERVED	RW	32	0x0000 0058	0x4A00 4E58

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3.11.27.2 RESTORE_CM1 Register Description

Table 3-1041. CM_CLKSEL_CORE_RESTORE

Address Offset	0x0000 0000		
Physical Address	0x4A00 4E00	**Instance**	RESTORE_CM1
Description	Second address map for register CM_CLKSEL_CORE. Used only by automatic restore upon wakeup from device OFF mode.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							CLKSEL_L4	RESERVED			CLKSEL_L3	RESERVED			CLKSEL_CORE

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	CLKSEL_L4	Selects L4 interconnect clock (L4_clk) 0x0: L4_CLK is L3_CLK divided by 1 0x1: L4_CLK is L3_CLK divided by 2	RW	0
7:5	RESERVED		R	0x0
4	CLKSEL_L3	Selects L3 interconnect clock (L3_clk) 0x0: L3_CLK is CORE_CLK divided by 1 0x1: L3_CLK is CORE_CLK divided by 2	RW	0
3:1	RESERVED		R	0x0
0	CLKSEL_CORE	Selects CORE_CLK configuration 0x0: CORE_CLK is CORE_X2_CLK divided by 1 0x1: CORE_CLK is CORE_X2_CLK divided by 2	RW	0

Table 3-1042. Register Call Summary for Register CM_CLKSEL_CORE_RESTORE

PRCM Register Manual
- RESTORE_CM1 Register Summary: [0]

Table 3-1043. CM_DIV_M2_DPLL_CORE_RESTORE

Address Offset	0x0000 0004		
Physical Address	0x4A00 4E04	**Instance**	RESTORE_CM1
Description	Second address map for register CM_DIV_M2_DPLL_CORE. Used only by automatic restore upon wakeup from device OFF mode.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						ST_DPLL_CLKOUT	DPLL_CLKOUT_GATE_CTRL	RESERVED		DPLL_CLKOUT_DIVCHACK	DPLL_CLKOUT_DIV				

Bits	Field Name	Description	Type	Reset
31:10	RESERVED		R	0x000000
9	ST_DPLL_CLKOUT	DPLL CLKOUT status Read 0x0: The clock output is enabled Read 0x1: The clock output is gated	R	0
8	DPLL_CLKOUT_GATE_CTRL	Control gating of DPLL CLKOUT 0x0: Automatically gate this clock when there is no dependency for it 0x1: Force this clock to stay enabled even if there is no request	RW	0
7:6	RESERVED		R	0x0
5	DPLL_CLKOUT_DIVCHACK	Toggle on this status bit after changing DPLL_CLKOUT_DIV indicates that the change in divider value has taken effect	R	0
4:0	DPLL_CLKOUT_DIV	DPLL post-divider factor, M2, for internal clock generation (1 to 31); Divide value from 1 to 31. 0x0: Reserved	RW	0x01

Table 3-1044. Register Call Summary for Register CM_DIV_M2_DPLL_CORE_RESTORE

PRCM Register Manual
- RESTORE_CM1 Register Summary: [0]

Table 3-1045. CM_DIV_M3_DPLL_CORE_RESTORE

Address Offset	0x0000 0008		
Physical Address	0x4A00 4E08	**Instance**	RESTORE_CM1
Description	Second address map for register CM_DIV_M3_DPLL_CORE. Used only by automatic restore upon wakeup from device OFF mode.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						ST_DPLL_CLKOUTHIF	DPLL_CLKOUTHIF_GATE_CTRL	RESERVED		DPLL_CLKOUTHIF_DIVCHACK	DPLL_CLKOUTHIF_DIV				

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Bits	Field Name	Description	Type	Reset
31:10	RESERVED		R	0x000000
9	ST_DPLL_CLKOUTHIF	DPLL CLKOUTHIF status Read 0x0: The clock output is enabled Read 0x1: The clock output is gated	R	0
8	DPLL_CLKOUTHIF_GATE_CTRL	Control gating of DPLL CLKOUTHIF 0x0: Automatically gate this clock when there is no dependency for it 0x1: Force this clock to stay enabled even if there is no request	RW	0
7:6	RESERVED		R	0x0
5	DPLL_CLKOUTHIF_DIVCHACK	Toggle on this status bit after changing DPLL_CLKOUTHIF_DIV indicates that the change in divider value has taken effect	R	0
4:0	DPLL_CLKOUTHIF_DIV	DPLL post-divider factor, M3, for internal clock generation (1 to 31);Divide value from 1 to 31. 0x0: Reserved	RW	0x01

Table 3-1046. Register Call Summary for Register CM_DIV_M3_DPLL_CORE_RESTORE

PRCM Register Manual
- RESTORE_CM1 Register Summary: [0]

Table 3-1047. CM_DIV_M4_DPLL_CORE_RESTORE

Address Offset	0x0000 000C		
Physical Address	0x4A00 4E0C	**Instance**	RESTORE_CM1
Description	Second address map for register CM_DIV_M4_DPLL_CORE. Used only by automatic restore upon wakeup from device OFF mode.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																			HSDIVIDER_CLKOUT1_PWDN	RESERVED		ST_HSDIVIDER_CLKOUT1	HSDIVIDER_CLKOUT1_GATE_CTRL	RESERVED		HSDIVIDER_CLKOUT1_DIVCHACK	HSDIVIDER_CLKOUT1_DIV							

Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000
12	HSDIVIDER_CLKOUT1_PWDN	Direct power down control for HSDIVIDER M4 divider and CLKOUT1 output. Power down should be enabled only when clock is first gated. 0x0: Divider is powered up 0x1: Divider is powered down	RW	0
11:10	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
9	ST_HSDIVIDER_CLKOUT1	HSDIVIDER CLKOUT1 status Read 0x0: The clock output is gated Read 0x1: The clock output is enabled	R	0
8	HSDIVIDER_CLKOUT1_GATE_CTRL	Control gating of HSDIVIDER CLKOUT1 0x0: Automatically gate this clock when there is no dependency for it 0x1: Force this clock to stay enabled even if there is no request	RW	0
7:6	RESERVED		R	0x0
5	HSDIVIDER_CLKOUT1_DIVCHACK	Toggle on this status bit after changing HSDIVIDER_CLKOUT1_DIV indicates that the change in divider value has taken effect	R	0
4:0	HSDIVIDER_CLKOUT1_DIV	DPLL M4 post-divider factor (1 to 31). 0x0: Reserved	RW	0x01

Table 3-1048. Register Call Summary for Register CM_DIV_M4_DPLL_CORE_RESTORE

Clock Management Functional Description
- DPLL_CORE Description: [0]

PRCM Register Manual
- RESTORE_CM1 Register Summary: [1]

Table 3-1049. CM_DIV_M5_DPLL_CORE_RESTORE

Address Offset	0x0000 0010		
Physical Address	0x4A00 4E10	**Instance**	RESTORE_CM1
Description	Second address map for register CM_DIV_M5_DPLL_CORE. Used only by automatic restore upon wakeup from device OFF mode.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																			HSDIVIDER_CLKOUT2_PWDN	RESERVED		ST_HSDIVIDER_CLKOUT2	HSDIVIDER_CLKOUT2_GATE_CTRL	RESERVED		HSDIVIDER_CLKOUT2_DIVCHACK	HSDIVIDER_CLKOUT2_DIV					

Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000
12	HSDIVIDER_CLKOUT2_PWDN	Direct power down control for HSDIVIDER M5 divider and CLKOUT2 output. Power down should be enabled only when clock is first gated. 0x0: Divider is powered up 0x1: Divider is powered down	RW	0
11:10	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
9	ST_HSDIVIDER_CLKOUT2	HSDIVIDER CLKOUT2 status Read 0x0: The clock output is gated Read 0x1: The clock output is enabled	R	0
8	HSDIVIDER_CLKOUT2_GATE_CTRL	Control gating of HSDIVIDER CLKOUT2 0x0: Automatically gate this clock when there is no dependency for it 0x1: Force this clock to stay enabled even if there is no request	RW	0
7:6	RESERVED		R	0x0
5	HSDIVIDER_CLKOUT2_DIVCHACK	Toggle on this status bit after changing HSDIVIDER_CLKOUT2_DIV indicates that the change in divider value has taken effect	R	0
4:0	HSDIVIDER_CLKOUT2_DIV	DPLL M5 post-divider factor (1 to 31). 0x0: Reserved	RW	0x01

Table 3-1050. Register Call Summary for Register CM_DIV_M5_DPLL_CORE_RESTORE

Clock Management Functional Description
- DPLL_CORE Description: [0]

PRCM Register Manual
- RESTORE_CM1 Register Summary: [1]

Table 3-1051. CM_DIV_M6_DPLL_CORE_RESTORE

Address Offset	0x0000 0014		
Physical Address	0x4A00 4E14	**Instance**	RESTORE_CM1
Description	Second address map for register CM_DIV_M6_DPLL_CORE. Used only by automatic restore upon wakeup from device OFF mode.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																			HSDIVIDER_CLKOUT3_PWDN	RESERVED		ST_HSDIVIDER_CLKOUT3	HSDIVIDER_CLKOUT3_GATE_CTRL	RESERVED		HSDIVIDER_CLKOUT3_DIVCHACK	HSDIVIDER_CLKOUT3_DIV					

Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000
12	HSDIVIDER_CLKOUT3_PWDN	Direct power down control for HSDIVIDER M6 divider and CLKOUT3 output. Power down should be enabled only when clock is first gated. 0x0: Divider is powered up 0x1: Divider is powered down	RW	0
11:10	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
9	ST_HSDIVIDER_CLKOUT3	HSDIVIDER CLKOUT3 status Read 0x0: The clock output is gated Read 0x1: The clock output is enabled	R	0
8	HSDIVIDER_CLKOUT3_GATE_CTRL	Control gating of HSDIVIDER CLKOUT3 0x0: Automatically gate this clock when there is no dependency for it 0x1: Force this clock to stay enabled even if there is no request	RW	0
7:6	RESERVED		R	0x0
5	HSDIVIDER_CLKOUT3_DIVCHACK	Toggle on this status bit after changing HSDIVIDER_CLKOUT3_DIV indicates that the change in divider value has taken effect	R	0
4:0	HSDIVIDER_CLKOUT3_DIV	DPLL M6 post-divider factor (1 to 31). 0x0: Reserved	RW	0x01

Table 3-1052. Register Call Summary for Register CM_DIV_M6_DPLL_CORE_RESTORE

Clock Management Functional Description
- DPLL_CORE Description: [0]

PRCM Register Manual
- RESTORE_CM1 Register Summary: [1]

Table 3-1053. CM_DIV_M7_DPLL_CORE_RESTORE

Address Offset	0x0000 0018		
Physical Address	0x4A00 4E18	**Instance**	RESTORE_CM1
Description	Second address map for register CM_DIV_M7_DPLL_CORE. Used only by automatic restore upon wakeup from device OFF mode.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																			HSDIVIDER_CLKOUT4_PWDN	RESERVED		ST_HSDIVIDER_CLKOUT4	HSDIVIDER_CLKOUT4_GATE_CTRL	RESERVED		HSDIVIDER_CLKOUT4_DIVCHACK	HSDIVIDER_CLKOUT4_DIV					

Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000
12	HSDIVIDER_CLKOUT4_PWDN	Direct power down control for HSDIVIDER M7 divider and CLKOUT4 output. Power down should be enabled only when clock is first gated. 0x0: Divider is powered up 0x1: Divider is powered down	RW	0
11:10	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
9	ST_HSDIVIDER_CLKOUT4	HSDIVIDER CLKOUT4 status Read 0x0: The clock output is gated Read 0x1: The clock output is enabled	R	0
8	HSDIVIDER_CLKOUT4_GATE_CTRL	Control gating of HSDIVIDER CLKOUT4 0x0: Automatically gate this clock when there is no dependency for it 0x1: Force this clock to stay enabled even if there is no request	RW	0
7:6	RESERVED		R	0x0
5	HSDIVIDER_CLKOUT4_DIVCHACK	Toggle on this status bit after changing HSDIVIDER_CLKOUT4_DIV indicates that the change in divider value has taken effect	R	0
4:0	HSDIVIDER_CLKOUT4_DIV	DPLL M7 post-divider factor (1 to 31). 0x0: Reserved	RW	0x01

Table 3-1054. Register Call Summary for Register CM_DIV_M7_DPLL_CORE_RESTORE

Clock Management Functional Description
- DPLL_CORE Description: [0]

PRCM Register Manual
- RESTORE_CM1 Register Summary: [1]

Table 3-1055. CM_CLKSEL_DPLL_CORE_RESTORE

Address Offset	0x0000 001C		
Physical Address	0x4A00 4E1C	**Instance**	RESTORE_CM1
Description	Second address map for register CM_CLKSEL_DPLL_CORE. Used only by automatic restore upon wakeup from device OFF mode.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								DPLL_BYP_CLKSEL	RESERVED		DPLL_CLKOUTHIF_CLKSEL	RESERVED				DPLL_MULT								RESERVED	DPLL_DIV						

Bits	Field Name	Description	Type	Reset
31:24	RESERVED		R	0x00
23	DPLL_BYP_CLKSEL	Allows control of the BYPASS clock of the PLL and the associated HSDIVIDER. Same as ULOWCLKEN on DPLL. In DPLL Locked mode, 0 - No impact 1 - No impact In DPLL Bypass mode, 0 - CLKINP is selected as the BYPASS clock for CLKOUT/CLKOUTX2 1 - CLKINPULOW is selected as the BYPASS clock for CLKOUT/CLKOUTX2	RW	0
22:21	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
20	DPLL_CLKOUTHIF_CLKSEL	Selects the source of the DPLL CLKOUTHIF clock. Same as CLKINPHIFSEL pin on the DPLL 0x0: CLKOUTHIF is generated from the DPLL oscillator (DCO) 0x1: CLKOUTHIF is generated from CLKINPHIF	RW	0
19	RESERVED		R	0
18:8	DPLL_MULT	DPLL multiplier factor (2 to 2047). This register is automatically cleared to 0 when the DPLL_EN field in the *CLKMODE_DPLL* register is set to select MN bypass mode. (equal to input M of DPLL; M=2 to 2047 = DPLL multiplies by M). 0x0: Reserved 0x1: Reserved	RW	0x000
7	RESERVED		R	0
6:0	DPLL_DIV	DPLL divider factor (0 to 127) (equal to input N of DPLL; actual division factor is N+1).	RW	0x00

Table 3-1056. Register Call Summary for Register CM_CLKSEL_DPLL_CORE_RESTORE

Clock Management Functional Description • DPLL_CORE Description: [0] [1]
PRCM Register Manual • RESTORE_CM1 Register Summary: [2]

Table 3-1057. CM_SSC_DELTAMSTEP_DPLL_CORE_RESTORE

Address Offset	0x0000 0020		
Physical Address	0x4A00 4E20	**Instance**	RESTORE_CM1
Description	Second address map for register CM_SSC_DELTAMSTEP_DPLL_CORE. Used only by automatic restore upon wakeup from device OFF mode. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								DELTAMSTEP																							

Bits	Field Name	Description	Type	Reset
31:20	RESERVED		R	0x000
19:0	DELTAMSTEP	DeltaMStep is split into fractional and integer part. For Triangular Spread Spectrum: [19:18] for integer part, [17:0] for fractional part For Square Wave Spread Spectrum [19:14] for integer part, [13:0] for fractional part	RW	0x00000

Table 3-1058. Register Call Summary for Register CM_SSC_DELTAMSTEP_DPLL_CORE_RESTORE

Clock Management Functional Description • DPLL_CORE Description: [0]
PRCM Register Manual • RESTORE_CM1 Register Summary: [1]

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Table 3-1059. CM_SSC_MODFREQDIV_DPLL_CORE_RESTORE

Address Offset	0x0000 0024		
Physical Address	0x4A00 4E24	**Instance**	RESTORE_CM1
Description	Second address map for register CM_SSC_MODFREQDIV_DPLL_CORE. Used only by automatic restore upon wakeup from device OFF mode. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																					MODFREQDIV_EXPONENT			RESERVED	MODFREQDIV_MANTISSA						

Bits	Field Name	Description	Type	Reset
31:11	RESERVED		R	0x000000
10:8	MODFREQDIV_EXPONENT	Set the Exponent component of MODFREQDIV factor	RW	0x0
7	RESERVED		R	0
6:0	MODFREQDIV_MANTISSA	Set the Mantissa component of MODFREQDIV factor	RW	0x00

Table 3-1060. Register Call Summary for Register CM_SSC_MODFREQDIV_DPLL_CORE_RESTORE

Clock Management Functional Description
- DPLL_CORE Description: [0] [1]

PRCM Register Manual
- RESTORE_CM1 Register Summary: [2]

Table 3-1061. CM_CLKMODE_DPLL_CORE_RESTORE

Address Offset	0x0000 0028		
Physical Address	0x4A00 4E28	**Instance**	RESTORE_CM1
Description	Second address map for register CM_CLKMODE_DPLL_CORE. Used only by automatic restore upon wakeup from device OFF mode.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																DPLL_SSC_DOWNSPREAD	DPLL_SSC_ACK	DPLL_SSC_EN	DPLL_REGM4XEN	DPLL_LPMODE_EN	RESERVED	DPLL_DRIFTGUARD_EN	RESERVED							DPLL_EN

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Bits	Field Name	Description	Type	Reset
31:15	RESERVED		R	0x00000
14	DPLL_SSC_DOWNSPREAD	Control if only low frequency spread is required 0x0: When SSC is enabled, clock frequency is spread on both sides of the programmed frequency 0x1: When SSC is enabled, clock frequency is spread only on the lower side of the programmed frequency	RW	0
13	DPLL_SSC_ACK	Acknowledgement from the DPLL regarding start and stop of Spread Spectrum Clocking feature Read 0x0: SSC has been turned off on PLL o/ps Read 0x1: SSC has been turned on on PLL o/ps	R	0
12	DPLL_SSC_EN	Enable or disable Spread Spectrum Clocking 0x0: SSC disabled 0x1: SSC enabled	RW	0
11	DPLL_REGM4XEN	Enable the REGM4XEN mode of the DPLL. Please check the DPLL documentation to check when this mode can be enabled. Read 0x0: REGM4XEN mode of the DPLL is disabled	R	0
10	DPLL_LPMODE_EN	Set the DPLL in low-power mode. Check the DPLL documentation to see when this can be enabled. 0x0: Low-power mode of the DPLL is disabled 0x1: Low-power mode of the DPLL is enabled	RW	0
9	RESERVED		RW	0
8	DPLL_DRIFTGUARD_EN	This bit allows to enable or disable the automatic recalibration feature of the DPLL. The DPLL will automatically start a recalibration process upon assertion of the DPLL's RECAL flag if this bit is set. 0x0: DRIFTGUARD feature is disabled 0x1: DRIFTGUARD feature is enabled	RW	0
7:3	RESERVED		RW	0x00
2:0	DPLL_EN	DPLL control. Upon Warm Reset, the PRCM DPLL control state machine updates this register to reflect MN bypass mode. 0x0: Reserved 0x1: Reserved 0x2: Reserved 0x3: Reserved 0x4: Put the DPLL in MN bypass mode. The DPLL_MULT register bits are reset to 0 automatically by putting the DPLL in this mode. 0x5: Put the DPLL in idle bypass low-power mode. 0x6: Put the DPLL in idle bypass fast-relock mode. 0x7: Enables the DPLL in lock mode	RW	0x4

Table 3-1062. Register Call Summary for Register CM_CLKMODE_DPLL_CORE_RESTORE

Clock Management Functional Description • DPLL_CORE Description: [0] [1] [2] [3] [4] [5]
PRCM Register Manual • RESTORE_CM1 Register Summary: [6]

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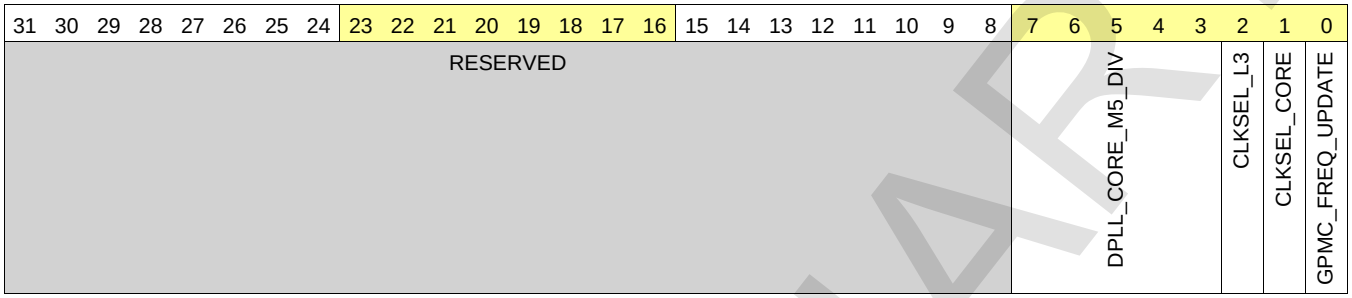
Table 3-1063. CM_SHADOW_FREQ_CONFIG2_RESTORE

Address Offset	0x0000 002C		
Physical Address	0x4A00 4E2C	**Instance**	RESTORE_CM1
Description	Second address map for register CM_SHADOW_FREQ_CONFIG2. Used only by automatic restore upon wakeup from device OFF mode.		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:8	RESERVED		R	0x000000
7:3	DPLL_CORE_M5_DIV	Shadow register for CM_DIV_M5_DPLL_CORE.HSDIVIDER_CLKOUT2_DIV. The main register is automatically loaded with the shadow register value after GPMC IDLE if the CM_SHADOW_FREQ_CONFIG1.FREQ_UPDATE field is set to 1 and GPMC_FREQ_UPDATE is set to 1. Divide value from 1 to 31. 0x0: Reserved	RW	0x04
2	CLKSEL_L3	Shadow register for CM_CLKSEL_CORE.CLKSEL_L3. The main register is automatically loaded with the shadow register value after GPMC IDLE if the CM_SHADOW_FREQ_CONFIG1.FREQ_UPDATE field is set to 1 and GPMC_FREQ_UPDATE is set to 1. 0x0: L3_CLK is CORE_CLK divided by 1 0x1: L3_CLK is CORE_CLK divided by 2	RW	0
1	CLKSEL_CORE	Shadow register for CM_CLKSEL_CORE.CLKSEL_CORE. The main register is automatically loaded with the shadow register value after GPMC IDLE if the CM_SHADOW_FREQ_CONFIG1.FREQ_UPDATE field is set to 1 and GPMC_FREQ_UPDATE is set to 1. 0x0: CORE_CLK is CORE_X2_CLK divided by 1 0x1: CORE_CLK is CORE_X2_CLK divided by 2	RW	0
0	GPMC_FREQ_UPDATE	Controls whether or not GPMC has to be put automatically into idle during the frequency change operation. 0x0: GPMC is not put automatically into idle during frequency change operation. 0x1: GPMC is put automatically into idle during frequency change operation.	RW	0

Table 3-1064. Register Call Summary for Register CM_SHADOW_FREQ_CONFIG2_RESTORE

PRCM Register Manual

- RESTORE_CM1 Register Summary: [0]

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Table 3-1065. CM_SHADOW_FREQ_CONFIG1_RESTORE

Address Offset	0x0000 0030		
Physical Address	0x4A00 4E30	**Instance**	RESTORE_CM1
Description	Second address map for register CM_SHADOW_FREQ_CONFIG1. Used only by automatic restore upon wakeup from device OFF mode.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																DPLL_CORE_M2_DIV					DPLL_CORE_DPLL_EN			RESERVED				DLL_RESET	DLL_OVERRIDE	RESERVED	FREQ_UPDATE

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x10D
15:11	DPLL_CORE_M2_DIV	Shadow register for CM_DIV_M2_DPLL_CORE.DPLL_CLKOUT_DIV. The main register is automatically loaded with the shadow register value after EMIF IDLE if the FREQ_UPDATE field is set to 1. Divide value from 1 to 31. 0x0: Reserved	RW	0x01
10:8	DPLL_CORE_DPLL_EN	Shadow register for CM_CLKMODE_DPLL_CORE.DPLL_EN. The main register is automatically loaded with the shadow register value after EMIF IDLE if the FREQ_UPDATE field is set to 1. 0x0: Reserved 0x1: Reserved 0x2: Reserved 0x3: Reserved 0x4: Put the DPLL in MN bypass mode. The DPLL_MULT register bits are reset to 0 automatically by putting the DPLL in this mode. 0x5: Put the DPLL in idle bypass low-power mode. 0x6: Put the DPLL in idle bypass fast-relock mode. 0x7: Enables the DPLL in lock mode	RW	0x5
7:4	RESERVED		R	0x0
3	DLL_RESET	Specify if DLL should be reset or not during the frequency change hardware sequence. 0x0: DLL is not reset during the frequency change hardware sequence 0x1: DLL is reset automatically during the frequency change hardware sequence	RW	1
2	DLL_OVERRIDE	Shadow register for CM_DLL_CTRL.DLL_OVERRIDE.The main register is automatically loaded with the shadow register value after EMIF IDLE if the FREQ_UPDATE field is set to 1. 0x0: Lock and code outputs are not overriden 0x1: Lock output is overriden to 1 and code output is overriden with a value coming from control module.	RW	1
1	RESERVED		RW	0

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Bits	Field Name	Description	Type	Reset
0	FREQ_UPDATE	Writing 1 indicates that a new configuration is available. It is automatically cleared by h/w after the configuration has been applied.	RW WSpecial	0

Table 3-1066. Register Call Summary for Register CM_SHADOW_FREQ_CONFIG1_RESTORE

PRCM Register Manual

- RESTORE_CM1 Register Summary: [0]

Table 3-1067. CM_AUTOIDLE_DPLL_CORE_RESTORE

Address Offset	0x0000 0034		
Physical Address	0x4A00 4E34	**Instance**	RESTORE_CM1
Description	Second address map for register CM_AUTOIDLE_DPLL_CORE. Used only by automatic restore upon wakeup from device OFF mode.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																											DPLL_DCOCLKLDO_PWDN	RESERVED		AUTO_DPLL_MODE		

Bits	Field Name	Description	Type	Reset
31:5	RESERVED		R	0x0000000
4	DPLL_DCOCLKLDO_PWDN	Allows powering down the DCOCLKLDO o/p of DPLL if all dividers in HSDIVIDER are powered down. PRCM takes care of reenabling this path for either restarting HSDIVIDER o/p or entering bypass mode. 0x0: Keep DCOCLKLDO powered even when all dividers in HSDIVIDER are powered down. 0x1: Automatically power down DCOCLKLDO when all o/ps of HSDIVIDER are powered down.	RW	0
3	RESERVED		R	0
2:0	AUTO_DPLL_MODE	DPLL automatic control. 0x0: DPLL auto control disabled 0x1: The DPLL is automatically put in low-power stop mode when its DPLL generated clocks are not required anymore. It is also restarted automatically. 0x2: The DPLL is automatically put in fast-relock stop mode when its DPLL generated clocks are not required anymore. It is also restarted automatically. 0x3: Reserved 0x4: Reserved 0x5: The DPLL is automatically put in idle bypass low-power mode when its DPLL generated clocks are not required anymore. It is also restarted automatically. 0x6: The DPLL is automatically put in idle bypass fast-relock mode when its DPLL generated clocks are not required anymore. It is also restarted automatically. 0x7: Reserved	RW	0x0

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Table 3-1068. Register Call Summary for Register CM_AUTOIDLE_DPLL_CORE_RESTORE

Clock Management Functional Description • DPLL_CORE Description: [0]
PRCM Register Manual • RESTORE_CM1 Register Summary: [1]

Table 3-1069. CM_MPU_CLKSTCTRL_RESTORE

Address Offset	0x0000 0038		
Physical Address	0x4A00 4E38	**Instance**	RESTORE_CM1
Description	Second address map for register CM_MPU_CLKSTCTRL. Used only by automatic restore upon wakeup from device OFF mode.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							CLKACTIVITY_MPU_DPLL_CLK	RESERVED						CLKTRCTRL	

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	CLKACTIVITY_MPU_DPLL_CLK	This field indicates the state of the MPU_DPLL_CLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
7:2	RESERVED		R	0x00
1:0	CLKTRCTRL	Controls the clock state transition of the MPU clock domain. 0x0: NO_SLEEP: Sleep transition cannot be initiated. Wakeup transition may however occur. Read 0x1: Reserved 0x2: SW_WKUP: Start a software forced wake-up transition on the domain. 0x3: HW_AUTO: Automatic transition is enabled. Sleep and wakeup transition are based upon hardware conditions.	RW	0x0

Table 3-1070. Register Call Summary for Register CM_MPU_CLKSTCTRL_RESTORE

PRCM Register Manual • RESTORE_CM1 Register Summary: [0]

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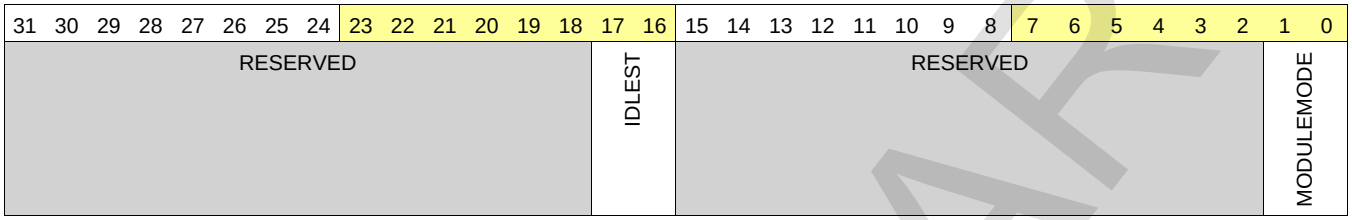
Table 3-1071. CM_CM1_PROFILING_CLKCTRL_RESTORE

Address Offset	0x0000 003C		
Physical Address	0x4A00 4E3C	**Instance**	RESTORE_CM1
Description	Second address map for register CM_CM1_PROFILING_CLKCTRL. Used only by automatic restore upon wakeup from device OFF mode. [warm reset insensitive]		
Type	RW		



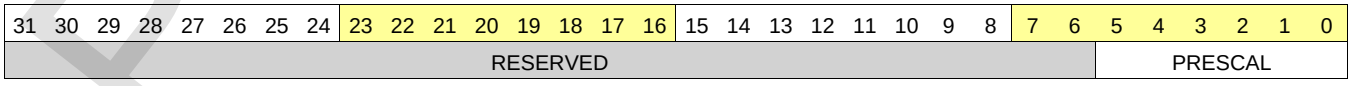
Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status Read 0x3: Module is disabled Read 0x2: Module is in Idle Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x0: Module is fully functional	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disabled by software. OCP configuration port is not accessible. 0x1: Module is managed automatically by hadware along with CM1 and EMU domain. OCP configuration port is accessible only when EMU domain is on. Read 0x2: Reserved Read 0x3: Reserved	RW	0x1

Table 3-1072. Register Call Summary for Register CM_CM1_PROFILING_CLKCTRL_RESTORE

PRCM Register Manual
- RESTORE_CM1 Register Summary: [0]

Table 3-1073. CM_DYN_DEP_PRESCAL_RESTORE

Address Offset	0x0000 0040		
Physical Address	0x4A00 4E40	**Instance**	RESTORE_CM1
Description	Second address map for register CM_DYN_DEP_PRESCAL. Used only by automatic restore upon wakeup from device OFF mode.		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:6	RESERVED		R	0x0000000
5:0	PRESCAL	Time unit is equal to (PRESCAL + 1) L4 clock cycles.	RW	0x20

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Table 3-1074. Register Call Summary for Register CM_DYN_DEP_PRESCAL_RESTORE

PRCM Register Manual • RESTORE_CM1 Register Summary: [0]

3.11.28 INSTR_CM1 Registers

3.11.28.1 INSTR_CM1 Register Summary

Table 3-1075. INSTR_CM1 Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	INSTR_CM1 Base Address
CMI1_IDENTICATION	R	32	0x0000 0000	0x4A00 4F00
CMI1_SYS_CONFIG	RW	32	0x0000 0010	0x4A00 4F10
CMI1_STATUS	R	32	0x0000 0014	0x4A00 4F14
CMI1_CONFIGURATION	RW	32	0x0000 0024	0x4A00 4F24
CMI1_CLASS_FILTERING	RW	32	0x0000 0028	0x4A00 4F28
CMI1_TRIGGERING	RW	32	0x0000 002C	0x4A00 4F2C
CMI1_SAMPLING	RW	32	0x0000 0030	0x4A00 4F30

3.11.28.2 INSTR_CM1 Register Description

Table 3-1076. CMI1_IDENTICATION

Address Offset	0x0000 0000		
Physical Address	0x4A00 4F00	**Instance**	INSTR_CM1
Description	CM profiling identification register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP revision	R	0x-- TI Internal data.

Table 3-1077. Register Call Summary for Register CMI1_IDENTICATION

PRCM Register Manual • INSTR_CM1 Register Summary: [0]

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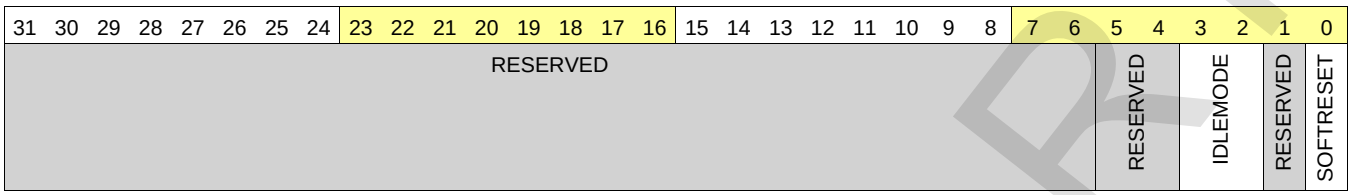
Table 3-1078. CMI1_SYS_CONFIG

Address Offset	0x0000 0010		
Physical Address	0x4A00 4F10	**Instance**	INSTR_CM1
Description	CM profiling system configuartion register		
Type	RW		



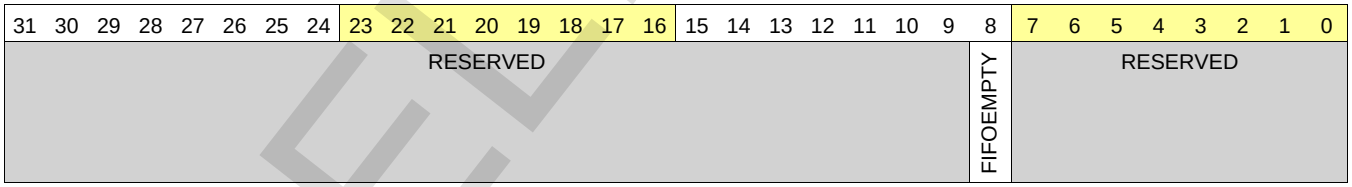
Bits	Field Name	Description	Type	Reset
31:6	RESERVED	Reserved	R	0x0000000
5:4	RESERVED	Reserved	R	0x0
3:2	IDLEMODE	Configuration of the local tartget state management mode	RW	0x2
1	RESERVED	Reserved	R	0
0	SOFTRESET	Software reset	RW	0

Table 3-1079. Register Call Summary for Register CMI1_SYS_CONFIG

PRCM Register Manual
- INSTR_CM1 Register Summary: [0]

Table 3-1080. CMI1_STATUS

Address Offset	0x0000 0014		
Physical Address	0x4A00 4F14	**Instance**	INSTR_CM1
Description	CM profiling status register		
Type	R		



Bits	Field Name	Description	Type	Reset
31:9	RESERVED	Reserved	R	0x000000
8	FIFOEMPTY	PM Profiling buffer empty	R	1
7:0	RESERVED	Reserved	R	0x00

Table 3-1081. Register Call Summary for Register CMI1_STATUS

PRCM Register Manual
- INSTR_CM1 Register Summary: [0]

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Table 3-1082. CMI1_CONFIGURATION

Address Offset	0x0000 0024		
Physical Address	0x4A00 4F24	**Instance**	INSTR_CM1
Description	CM profiling configuration register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLAIM_3		CLAIM_2	CLAIM_1	RESERVED				RESERVED								RESERVED								EVT_CAPT_EN							

Bits	Field Name	Description	Type	Reset
31:30	CLAIM_3	Ownership	RW	0x0
29	CLAIM_2	Debugger override qualifier	RW	1
28	CLAIM_1	Current owner	R	0
27:24	RESERVED	Reserved	R	0x0
23	RESERVED	Reserved	R	0
22:16	RESERVED	Reserved	R	0x00
15	RESERVED	Reserved	R	0
14:8	RESERVED	Reserved	R	0x00
7	EVT_CAPT_EN	When HIGH the PM events capture is enabled	RW	0
6:0	RESERVED	Reserved	R	0x00

Table 3-1083. Register Call Summary for Register CMI1_CONFIGURATION

PRCM Register Manual

- INSTR_CM1 Register Summary: [0]

Table 3-1084. CMI1_CLASS_FILTERING

Address Offset	0x0000 0028		
Physical Address	0x4A00 4F28	**Instance**	INSTR_CM1
Description	CM profiling class filtering register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												SNAP_CAPT_EN_03	SNAP_CAPT_EN_02	SNAP_CAPT_EN_01	SNAP_CAPT_EN_00

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved	R	0x0000000
3	SNAP_CAPT_EN_03	Snapshot capture enable - Class-ID = 0x03	RW	0
2	SNAP_CAPT_EN_02	Snapshot capture enable - Class-ID = 0x02	RW	0
1	SNAP_CAPT_EN_01	Snapshot capture enable - Class-ID = 0x01	RW	0

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Bits	Field Name	Description	Type	Reset
0	SNAP_CAPT_EN_00	Snapshot capture enable - Class-ID = 0x00	RW	0

Table 3-1085. Register Call Summary for Register CMI1_CLASS_FILTERING

PRCM Register Manual
- INSTR_CM1 Register Summary: [0]

Table 3-1086. CMI1_TRIGGERING

Address Offset	0x0000 002C		
Physical Address	0x4A00 4F2C	**Instance**	INSTR_CM1
Description	CM profiling triggering control register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														TRIG_STOP_EN	TRIG_START_EN

Bits	Field Name	Description	Type	Reset
31:2	RESERVED	Reserved	R	0x0000 0000
1	TRIG_STOP_EN	Enable stop capturing PM events from external trigger detection	RW	0
0	TRIG_START_EN	Enable start capturing PM events from external trigger detection	RW	0

Table 3-1087. Register Call Summary for Register CMI1_TRIGGERING

PRCM Register Manual
- INSTR_CM1 Register Summary: [0]

Table 3-1088. CMI1_SAMPLING

Address Offset	0x0000 0030		
Physical Address	0x4A00 4F30	**Instance**	INSTR_CM1
Description	CM profiling sampling window register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												FCLK_DIV_FACOR				RESERVED								SAMP_WIND_SIZE							

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Bits	Field Name	Description	Type	Reset
31:20	RESERVED	Reserved	R	0x000
19:16	FCLK_DIV_FACOR	FunClk divide factor ranging from 1 to 16	RW	0x0
15:8	RESERVED	Reserved	R	0x00
7:0	SAMP_WIND_SIZE	PM events sampling window size	RW	0x00

Table 3-1089. Register Call Summary for Register CMI1_SAMPLING

PRCM Register Manual
- INSTR_CM1 Register Summary: [0]

3.11.29 CM2 Instance Summary

Table 3-1090. CM2 Instance Summary

Module Name	L4 Base Address	Size
INTRCONN_SOCKET_CM2	0x4A00 8000	256Bytes
CKGEN_CM2	0x4A00 8100	256Bytes
ALWAYS_ON_CM2	0x4A00 8600	256Bytes
CORE_CM2	0x4A00 8700	2KBytes
IVAHD_CM2	0x4A00 8F00	256Bytes
CAM_CM2	0x4A00 9000	256Bytes
DSS_CM2	0x4A00 9100	256Bytes
SGX_CM2	0x4A00 9200	256Bytes
L3INIT_CM2	0x4A00 9300	256Bytes
L4PER_CM2	0x4A00 9400	512Bytes
RESTORE_CM2	0x4A00 9E00	256Bytes
INSTR_CM2	0x4A00 9F00	256Bytes

3.11.30 INTRCONN_SOCKET_CM2 Registers

3.11.30.1 INTRCONN_SOCKET_CM2 Register Summary

Table 3-1091. INTRCONN_SOCKET_CM2 Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	INTRCONN_SOCKET_CM2 L4 Base Address
REVISION_CM2	R	32	0x0000 0000	0x4A00 8000
CM_CM2_PROFILING_CLKCTRL	RW	32	0x0000 0040	0x4A00 8040
CM2_DEBUG_CFG	RW	32	0x0000 00F0	0x4A00 80F0

3.11.30.2 INTRCONN_SOCKET_CM2 Register Description

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Table 3-1092. REVISION_CM2

Address Offset	0x0000 0000		
Physical Address	0x4A00 8000	**Instance**	INTRCONN_SOCKET_CM2
Description	This register contains the IP revision code for the CM2 part of the PRCM		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	Revision Number	R	0x- - TI Internal data.

Table 3-1093. Register Call Summary for Register REVISION_CM2

PRCM Register Manual

- INTRCONN_SOCKET_CM2 Register Summary: [0]

Table 3-1094. CM_CM2_PROFILING_CLKCTRL

Address Offset	0x0000 0040		
Physical Address	0x4A00 8040	**Instance**	INTRCONN_SOCKET_CM2
Description	This register manages the CM2_PROFILING clocks. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED														MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status Read 0x0: Module is fully functional Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in Idle Read 0x3: Module is disabled	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disabled by software. INTRCONN configuration port is not accessible. 0x1: Module is managed automatically by hardware along with L3INSTR domain. Read 0x2: Reserved Read 0x3: Reserved	RW	0x1

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Table 3-1095. Register Call Summary for Register CM_CM2_PROFILING_CLKCTRL

PRCM Register Manual
- INTRCONN_SOCKET_CM2 Register Summary: [0]
- RESTORE_CM2 Register Description: [1]

Table 3-1096. CM2_DEBUG_CFG

Address Offset	0x0000 00F0		
Physical Address	0x4A00 80F0	**Instance**	INTRCONN_SOCKET_CM2
Description	This register is used to configure the CM2's 32-bit debug output. There is one 7-bit source select field for selecting from a shared set of 8-bit internal signal blocks per byte. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL3								SEL2								SEL1								SEL0							

Bits	Field Name	Description	Type	Reset
31:24	SEL3	Internal signal block select for debug word byte-3	RW	0x03
23:16	SEL2	Internal signal block select for debug word byte-2	RW	0x02
15:8	SEL1	Internal signal block select for debug word byte-1	RW	0x01
7:0	SEL0	Internal signal block select for debug word byte-0	RW	0x00

Table 3-1097. Register Call Summary for Register CM2_DEBUG_CFG

PRCM Register Manual
- INTRCONN_SOCKET_CM2 Register Summary: [0]

3.11.31 CKGEN_CM2 Registers

3.11.31.1 CKGEN_CM2 Register Summary

Table 3-1098. CKGEN_CM2 Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	CKGEN_CM2 L4 Base Address
CM_CLKSEL_MPU_M3_ISS_ROOT	RW	32	0x0000 0000	0x4A00 8100
CM_CLKSEL_USB_60MHZ	RW	32	0x0000 0004	0x4A00 8104
CM_SCALE_FCLK	RW	32	0x0000 0008	0x4A00 8108
CM_CORE_DVFS_PERF1	RW	32	0x0000 0010	0x4A00 8110
CM_CORE_DVFS_PERF2	RW	32	0x0000 0014	0x4A00 8114
CM_CORE_DVFS_PERF3	RW	32	0x0000 0018	0x4A00 8118
CM_CORE_DVFS_PERF4	RW	32	0x0000 001C	0x4A00 811C
CM_CORE_DVFS_CURRENT	RW	32	0x0000 0024	0x4A00 8124
CM_IVA_DVFS_PERF_DSP	RW	32	0x0000 0028	0x4A00 8128
CM_IVA_DVFS_PERF_IVAHD	RW	32	0x0000 002C	0x4A00 812C
CM_IVA_DVFS_PERF_ABE	RW	32	0x0000 0030	0x4A00 8130
CM_IVA_DVFS_CURRENT	RW	32	0x0000 0038	0x4A00 8138
CM_CLKMODE_DPLL_PER	RW	32	0x0000 0040	0x4A00 8140
CM_IDLEST_DPLL_PER	R	32	0x0000 0044	0x4A00 8144
CM_AUTOIDLE_DPLL_PER	RW	32	0x0000 0048	0x4A00 8148
CM_CLKSEL_DPLL_PER	RW	32	0x0000 004C	0x4A00 814C
CM_DIV_M2_DPLL_PER	RW	32	0x0000 0050	0x4A00 8150

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Table 3-1098. CKGEN_CM2 Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	CKGEN_CM2 L4 Base Address
CM_DIV_M3_DPLL_PER	RW	32	0x0000 0054	0x4A00 8154
CM_DIV_M4_DPLL_PER	RW	32	0x0000 0058	0x4A00 8158
CM_DIV_M5_DPLL_PER	RW	32	0x0000 005C	0x4A00 815C
CM_DIV_M6_DPLL_PER	RW	32	0x0000 0060	0x4A00 8160
CM_DIV_M7_DPLL_PER	RW	32	0x0000 0064	0x4A00 8164
CM_SSC_DELTAMSTEP_DPLL_PER	RW	32	0x0000 0068	0x4A00 8168
CM_SSC_MODFREQDIV_DPLL_PER	RW	32	0x0000 006C	0x4A00 816C
RESERVED	RW	32	0x0000 0070	0x4A00 8170
CM_CLKMODE_DPLL_USB	RW	32	0x0000 0080	0x4A00 8180
CM_IDLEST_DPLL_USB	R	32	0x0000 0084	0x4A00 8184
CM_AUTOIDLE_DPLL_USB	RW	32	0x0000 0088	0x4A00 8188
CM_CLKSEL_DPLL_USB	RW	32	0x0000 008C	0x4A00 818C
CM_DIV_M2_DPLL_USB	RW	32	0x0000 0090	0x4A00 8190
CM_SSC_DELTAMSTEP_DPLL_USB	RW	32	0x0000 00A8	0x4A00 81A8
CM_SSC_MODFREQDIV_DPLL_USB	RW	32	0x0000 00AC	0x4A00 81AC
CM_CLKDCOLDO_DPLL_USB	RW	32	0x0000 00B4	0x4A00 81B4
RESERVED	RW	32	0x0000 00C0	0x4A00 81C0
RESERVED	R	32	0x0000 00C4	0x4A00 81C4
RESERVED	RW	32	0x0000 00C8	0x4A00 81C8
RESERVED	RW	32	0x0000 00CC	0x4A00 81CC
RESERVED	RW	32	0x0000 00D0	0x4A00 81D0
RESERVED	RW	32	0x0000 00E8	0x4A00 81E8
RESERVED	RW	32	0x0000 00EC	0x4A00 81EC

3.11.31.2 CKGEN_CM2 Register Description

Table 3-1099. CM_CLKSEL_MPU_M3_ISS_ROOT

Address Offset	0x0000 0000		
Physical Address	0x4A00 8100	**Instance**	CKGEN_CM2
Description	MPU_A3/ISS root clock selection (MPU_A3_ISS_CLK).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															CLKSEL

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	CLKSEL	Select the source for the root clock of MPU_A3/ISS 0x0: Root clock is sourced from CORE_CLK 0x1: Functional clock is sourced from DPLL_PER	RW	0

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Table 3-1100. Register Call Summary for Register CM_CLKSEL_MPU_M3_ISS_ROOT

Clock Management Functional Description • CM Clock Source: [0]
PRCM Register Manual • CKGEN_CM2 Register Summary: [1]

Table 3-1101. CM_CLKSEL_USB_60MHZ

Address Offset	0x0000 0004		
Physical Address	0x4A00 8104	**Instance**	CKGEN_CM2
Description	Selects the configuration of the divider generating 60MHz clock for USB from the DPLL_USB o/p.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															CLKSEL

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	CLKSEL	Select the configuration of the divider 0x0: Set the divider in bypass mode to support bypass clock from DPLL_USB to pass through without division. 0x1: Set the divider to divide the DPLL o/p (480 MHz typical) by 8 to generate 60-MHz clock, to be used for OPP100 and OPP50.	RW	1

Table 3-1102. Register Call Summary for Register CM_CLKSEL_USB_60MHZ

Clock Management Functional Description • CM Clock Source: [0]
PRCM Register Manual • CKGEN_CM2 Register Summary: [1]

Table 3-1103. CM_SCALE_FCLK

Address Offset	0x0000 0008		
Physical Address	0x4A00 8108	**Instance**	CKGEN_CM2
Description	This register can be used to scale PER_ABE_NC_FCLK, 96M_FCLK, 48M_FCLK, and 64M_FCLK to half their respective typical frequencies.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															SCALE_FCLK

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Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	SCALE_FCLK	Enable or disable the functional clock scaling. 0x0: The functional clocks run at their default frequencies 0x1: The functional clocks run at half their typical frequencies	RW	0

Table 3-1104. Register Call Summary for Register CM_SCALE_FCLK

Clock Management Functional Description • CM Clock Source: [0]
PRCM Register Manual • CKGEN_CM2 Register Summary: [1]

Table 3-1105. CM_CORE_DVFS_PERF1

Address Offset	0x0000 0010		
Physical Address	0x4A00 8110	**Instance**	CKGEN_CM2
Description	This register allows to system master #1 to specify which level of performance is required from CORE domain (mainly external memory throughput?)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								PERF_REQ							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED		R	0x000000
7:0	PERF_REQ	Current performance request. Unit to be defined by user.	RW	0x00

Table 3-1106. Register Call Summary for Register CM_CORE_DVFS_PERF1

PRCM Register Manual • CKGEN_CM2 Register Summary: [0]

Table 3-1107. CM_CORE_DVFS_PERF2

Address Offset	0x0000 0014		
Physical Address	0x4A00 8114	**Instance**	CKGEN_CM2
Description	This register allows to system master #2 to specify which level of performance is require from CORE domain (mainly external memory throughput?)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								PERF_REQ							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED		R	0x000000
7:0	PERF_REQ	Current performance request. Unit to be defined by user.	RW	0x00

Table 3-1108. Register Call Summary for Register CM_CORE_DVFS_PERF2

PRCM Register Manual • CKGEN_CM2 Register Summary: [0]

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Table 3-1109. CM_CORE_DVFS_PERF3

Address Offset	0x0000 0018		
Physical Address	0x4A00 8118	**Instance**	CKGEN_CM2
Description	This register allows to system master #3 to specify which level of performance is require from CORE domain (mainly external memory throughput?)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								PERF_REQ							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED		R	0x000000
7:0	PERF_REQ	Current performance request. Unit to be defined by user.	RW	0x00

Table 3-1110. Register Call Summary for Register CM_CORE_DVFS_PERF3

PRCM Register Manual

- CKGEN_CM2 Register Summary: [0]

Table 3-1111. CM_CORE_DVFS_PERF4

Address Offset	0x0000 001C		
Physical Address	0x4A00 811C	**Instance**	CKGEN_CM2
Description	This register allows to system master #4 to specify which level of performance is require from CORE domain (mainly external memory throughput?)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								PERF_REQ							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED		R	0x000000
7:0	PERF_REQ	Current performance request. Unit to be defined by user.	RW	0x00

Table 3-1112. Register Call Summary for Register CM_CORE_DVFS_PERF4

PRCM Register Manual

- CKGEN_CM2 Register Summary: [0]

Table 3-1113. CM_CORE_DVFS_CURRENT

Address Offset	0x0000 0024		
Physical Address	0x4A00 8124	**Instance**	CKGEN_CM2
Description	This register hold the current level of performance achievable by the CORE domain, according to the current OPP setting		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								PERF_CURRENT							

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Bits	Field Name	Description	Type	Reset
31:8	RESERVED		R	0x000000
7:0	PERF_CURRENT	Current achievable performance level. Unit to be defined by user.	RW	0x00

Table 3-1114. Register Call Summary for Register CM_CORE_DVFS_CURRENT

Voltage Management Functional Description
- DVFS Voting Mechanism (VDD_CORE_L and VDD_IVA_L Voltage Domains): [0]

PRCM Register Manual
- CKGEN_CM2 Register Summary: [1]

Table 3-1115. CM_IVA_DVFS_PERF_DSP

Address Offset	0x0000 0028		
Physical Address	0x4A00 8128	**Instance**	CKGEN_CM2
Description	This register allows to specify which level of performance is required from IVA domain for DSP to operate.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								PERF_REQ							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED		R	0x000000
7:0	PERF_REQ	Current performance request. Unit to be defined by user.	RW	0x00

Table 3-1116. Register Call Summary for Register CM_IVA_DVFS_PERF_DSP

PRCM Register Manual
- CKGEN_CM2 Register Summary: [0]

Table 3-1117. CM_IVA_DVFS_PERF_IVAHD

Address Offset	0x0000 002C		
Physical Address	0x4A00 812C	**Instance**	CKGEN_CM2
Description	This register allows to specify which level of performance is required from IVA domain for IVAHD to operate.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								PERF_REQ							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED		R	0x000000
7:0	PERF_REQ	Current performance request. Unit to be defined by user.	RW	0x00

Table 3-1118. Register Call Summary for Register CM_IVA_DVFS_PERF_IVAHD

PRCM Register Manual
- CKGEN_CM2 Register Summary: [0]

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Table 3-1119. CM_IVA_DVFS_PERF_ABE

Address Offset	0x0000 0030		
Physical Address	0x4A00 8130	**Instance**	CKGEN_CM2
Description	This register allows to specify which level of performance is required from IVA domain for ABE to operate.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								PERF_REQ							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED		R	0x000000
7:0	PERF_REQ	Current performance request. Unit to be defined by user.	RW	0x00

Table 3-1120. Register Call Summary for Register CM_IVA_DVFS_PERF_ABE

PRCM Register Manual
- CKGEN_CM2 Register Summary: [0]

Table 3-1121. CM_IVA_DVFS_CURRENT

Address Offset	0x0000 0038		
Physical Address	0x4A00 8138	**Instance**	CKGEN_CM2
Description	This register hold the current level of performance achievable by the IVA domain, according to the current OPP setting		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								PERF_CURRENT							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED		R	0x000000
7:0	PERF_CURRENT	Current achievable performance level. Unit to be defined by user.	RW	0x00

Table 3-1122. Register Call Summary for Register CM_IVA_DVFS_CURRENT

Voltage Management Functional Description
- DVFS Voting Mechanism (VDD_CORE_L and VDD_IVA_L Voltage Domains): [0]

PRCM Register Manual
- CKGEN_CM2 Register Summary: [1]

Table 3-1123. CM_CLKMODE_DPLL_PER

Address Offset	0x0000 0040		
Physical Address	0x4A00 8140	**Instance**	CKGEN_CM2
Description	This register allows controlling the DPLL modes.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																DPLL_SSC_DOWNSPREAD	DPLL_SSC_ACK	DPLL_SSC_EN	DPLL_REGM4XEN	DPLL_LPMODE_EN	RESERVED	DPLL_DRIFTGUARD_EN	RESERVED					DPLL_EN		

Bits	Field Name	Description	Type	Reset
31:15	RESERVED		R	0x00000
14	DPLL_SSC_DOWNSPREAD	Control if only low frequency spread is required 0x0: When SSC is enabled, clock frequency is spread on both sides of the programmed frequency 0x1: When SSC is enabled, clock frequency is spread only on the lower side of the programmed frequency	RW	0
13	DPLL_SSC_ACK	Acknowledgement from the DPLL regarding start and stop of Spread Spectrum Clocking feature Read 0x0: SSC has been turned off on PLL o/ps Read 0x1: SSC has been turned on on PLL o/ps	R	0
12	DPLL_SSC_EN	Enable or disable Spread Spectrum Clocking 0x0: SSC disabled 0x1: SSC enabled	RW	0
11	DPLL_REGM4XEN	Enable the REGM4XEN mode of the DPLL. Please check the DPLL documentation to check when this mode can be enabled. Read 0x0: REGM4XEN mode of the DPLL is disabled	R	0
10	DPLL_LPMODE_EN	Set the DPLL in low-power mode. Check the DPLL documentation to see when this can be enabled. 0x0: Low-power mode of the DPLL is disabled 0x1: Low-power mode of the DPLL is enabled	RW	0
9	RESERVED		RW	0
8	DPLL_DRIFTGUARD_EN	This bit allows to enable or disable the automatic recalibration feature of the DPLL. The DPLL will automatically start a recalibration process upon assertion of the DPLL's RECAL flag if this bit is set. 0x0: DRIFTGUARD feature is disabled 0x1: DRIFTGUARD feature is enabled	RW	0
7:3	RESERVED		RW	0x00
2:0	DPLL_EN	DPLL control. Upon Warm Reset, the PRCM DPLL control state machine updates this register to reflect MN bypass mode. 0x0: Reserved 0x1: Reserved 0x2: Reserved 0x3: Reserved 0x4: Put the DPLL in MN bypass mode. The DPLL_MULT register bits are reset to 0 automatically by putting the DPLL in this mode. 0x5: Put the DPLL in idle bypass low-power mode. 0x6: Put the DPLL in idle bypass fast-relock mode. 0x7: Enables the DPLL in lock mode	RW	0x4

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Table 3-1124. Register Call Summary for Register CM_CLKMODE_DPLL_PER

Clock Management Functional Description • DPLL_PER Description: [0] [1] [2] [5] [6] [7]
PRCM Register Manual • CKGEN_CM2 Register Summary: [8]

Table 3-1125. CM_IDLEST_DPLL_PER

Address Offset	0x0000 0044		
Physical Address	0x4A00 8144	**Instance**	CKGEN_CM2
Description	This register allows monitoring DPLL activity. This register is read only and automatically updated. [warm reset insensitive]		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							ST_MN_BYPASS	RESERVED							ST_DPLL_CLK

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	ST_MN_BYPASS	DPLL MN_BYPASS status Read 0x1: DPLL is in MN_Bypass Read 0x0: DPLL is not in MN_Bypass	R	0
7:1	RESERVED		R	0x00
0	ST_DPLL_CLK	DPLL lock status Read 0x1: DPLL is LOCKED Read 0x0: DPLL is either in bypass mode or in stop mode.	R	0

Table 3-1126. Register Call Summary for Register CM_IDLEST_DPLL_PER

PRCM Register Manual • CKGEN_CM2 Register Summary: [0]

Table 3-1127. CM_AUTOIDLE_DPLL_PER

Address Offset	0x0000 0048		
Physical Address	0x4A00 8148	**Instance**	CKGEN_CM2
Description	This register provides automatic control over the DPLL activity.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														AUTO_DPLL_MODE	

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Bits	Field Name	Description	Type	Reset
31:3	RESERVED		R	0x0000000
2:0	AUTO_DPLL_MODE	DPLL automatic control; 0x0: DPLL auto control disabled 0x1: The DPLL is automatically put in low-power stop mode when its DPLL generated clocks are not required anymore. It is also restarted automatically. 0x2: The DPLL is automatically put in fast-relock stop mode when its DPLL generated clocks are not required anymore. It is also restarted automatically. 0x3: Reserved 0x4: Reserved 0x5: The DPLL is automatically put in idle bypass low-power mode when its DPLL generated clocks are not required anymore. It is also restarted automatically. 0x6: The DPLL is automatically put in idle bypass fast-relock mode when its DPLL generated clocks are not required anymore. It is also restarted automatically. 0x7: Reserved	RW	0x0

Table 3-1128. Register Call Summary for Register CM_AUTOIDLE_DPLL_PER

Clock Management Functional Description • DPLL_PER Description: [0]
PRCM Register Manual • CKGEN_CM2 Register Summary: [1]

Table 3-1129. CM_CLKSEL_DPLL_PER

Address Offset	0x0000 004C		
Physical Address	0x4A00 814C	**Instance**	CKGEN_CM2
Description	This register provides controls over the DPLL.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								DPLL_BYP_CLKSEL	RESERVED							DPLL_MULT								RESERVED	DPLL_DIV						

Bits	Field Name	Description	Type	Reset
31:24	RESERVED		R	0x00
23	DPLL_BYP_CLKSEL	Allows control of the BYPASS clock of the PLL and the associated HSDIVIDER. Same as ULOWCLKEN on DPLL. In DPLL Locked mode, 0 - No impact 1 - No impact In DPLL Bypass mode, 0 - CLKINP is selected as the BYPASS clock for CLKOUT/CLKOUTX2 1 - CLKINPULOW is selected as the BYPASS clock for CLKOUT/CLKOUTX2	RW	0
22:19	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
18:8	DPLL_MULT	DPLL multiplier factor (2 to 2047). This register is automatically cleared to 0 when the DPLL_EN field in the *CLKMODE_DPLL* register is set to select MN bypass mode. (equal to input M of DPLL; M=2 to 2047 = DPLL multiplies by M). 0x0: Reserved 0x1: Reserved	RW	0x000
7	RESERVED		R	0
6:0	DPLL_DIV	DPLL divider factor (0 to 127) (equal to input N of DPLL; actual division factor is N+1).	RW	0x00

Table 3-1130. Register Call Summary for Register CM_CLKSEL_DPLL_PER

Clock Management Functional Description
- CM Clock Source: [0]
- DPLL_PER Description: [1] [2]

PRCM Register Manual
- CKGEN_CM2 Register Summary: [3]

Table 3-1131. CM_DIV_M2_DPLL_PER

Address Offset	0x0000 0050		
Physical Address	0x4A00 8150	**Instance**	CKGEN_CM2
Description	This register provides controls over the M2 divider of the DPLL.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				ST_DPLL_CLKOUTX2	DPLL_CLKOUTX2_GATE_CTRL	ST_DPLL_CLKOUT	DPLL_CLKOUT_GATE_CTRL	RESERVED		DPLL_CLKOUT_DIVCHACK	DPLL_CLKOUT_DIV				

Bits	Field Name	Description	Type	Reset
31:12	RESERVED		R	0x00000
11	ST_DPLL_CLKOUTX2	DPLL CLKOUTX2 status Read 0x0: The clock output is gated Read 0x1: The clock output is enabled	R	0
10	DPLL_CLKOUTX2_GATE_CTRL	Control gating of DPLL CLKOUTX2 0x0: Automatically gate this clock when there is no dependency for it 0x1: Force this clock to stay enabled even if there is no request	RW	0
9	ST_DPLL_CLKOUT	DPLL CLKOUT status Read 0x0: The clock output is gated Read 0x1: The clock output is enabled	R	0

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Bits	Field Name	Description	Type	Reset
8	DPLL_CLKOUT_GATE_CTRL	Control gating of DPLL CLKOUT 0x0: Automatically gate this clock when there is no dependency for it 0x1: Force this clock to stay enabled even if there is no request.	RW	0
7:6	RESERVED		R	0x0
5	DPLL_CLKOUT_DIVCHACK	Toggle on this status bit after changing DPLL_CLKOUT_DIV indicates that the change in divider value has taken effect.	R	0
4:0	DPLL_CLKOUT_DIV	DPLL post-divider factor, M2, for internal clock generation (1 to 31) 0x0: Reserved 0x4: 4, to be used for OPP100 and OPP50 (when DPLL_PER is locked at 768 MHz) 0x8: 8, to be used for OPP100 and OPP50 (when DPLL_PER is locked at 1536 MHz)	RW	0x01

Table 3-1132. Register Call Summary for Register CM_DIV_M2_DPLL_PER

Clock Management Functional Description • DPLL_PER Description: [0] [1] [2] [3] [4] [5]
PRCM Register Manual • CKGEN_CM2 Register Summary: [6]

Table 3-1133. CM_DIV_M3_DPLL_PER

Address Offset	0x0000 0054		
Physical Address	0x4A00 8154	**Instance**	CKGEN_CM2
Description	This register provides controls over the M3 divider of the DPLL.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						ST_DPLL_CLKOUTHIF	DPLL_CLKOUTHIF_GATE_CTRL	RESERVED		DPLL_CLKOUTHIF_DIVCHACK	DPLL_CLKOUTHIF_DIV				

Bits	Field Name	Description	Type	Reset
31:10	RESERVED		R	0x000000
9	ST_DPLL_CLKOUTHIF	DPLL CLKOUTHIF status Read 0x0: The clock output is gated. Read 0x1: The clock output is enabled.	R	0
8	DPLL_CLKOUTHIF_GATE_CTRL	Control gating of DPLL CLKOUTHIF 0x0: Gate this clock unconditionally and stop requesting it. 0x1: Request this clock and un-gate it when available.	RW	0
7:6	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
5	DPLL_CLKOUTHIF_DIVCHACK	Toggle on this status bit after changing DPLL_CLKOUTHIF_DIV indicates that the change in divider value has taken effect.	R	0
4:0	DPLL_CLKOUTHIF_DIV	DPLL post-divider factor, M3, for internal clock generation (1 to 31) 0x0: Reserved 0x3: 3, to be used for OPP100 (when DPLL_PER is locked at 768 MHz) 0x4: 4, to be used for OPP50 (when DPLL_PER is locked at 768 MHz) 0x6: 6, to be used for OPP100 (when DPLL_PER is locked at 1536 MHz) 0x8: 8, to be used for OPP50 (when DPLL_PER is locked at 1536 MHz)	RW	0x01

Table 3-1134. Register Call Summary for Register CM_DIV_M3_DPLL_PER

Clock Management Functional Description
- Generic DPLL Overview: [0]
- DPLL_PER Description: [1] [2] [3] [4]

PRCM Register Manual
- CKGEN_CM2 Register Summary: [5]

Table 3-1135. CM_DIV_M4_DPLL_PER

Address Offset	0x0000 0058		
Physical Address	0x4A00 8158	**Instance**	CKGEN_CM2
Description	This register provides controls over the CLKOUT1 o/p of the HSDIVIDER.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																			HSDIVIDER_CLKOUT1_PWDN	RESERVED		ST_HSDIVIDER_CLKOUT1	HSDIVIDER_CLKOUT1_GATE_CTRL	RESERVED		HSDIVIDER_CLKOUT1_DIVCHACK	HSDIVIDER_CLKOUT1_DIV							

Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000
12	HSDIVIDER_CLKOUT1_PWDN	Direct power down control for HSDIVIDER M4 divider and CLKOUT1 output. Power down should be enabled only when clock is first gated. 0x0: Divider is powered up 0x1: Divider is powered down	RW	0
11:10	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
9	ST_HSDIVIDER_CLKOUT1	HSDIVIDER CLKOUT1 status Read 0x0: The clock output is gated. Read 0x1: The clock output is enabled.	R	0
8	HSDIVIDER_CLKOUT1_GATE_CTRL	Control gating of HSDIVIDER CLKOUT1 0x0: Automatically gate this clock when there is no dependency for it. 0x1: Force this clock to stay enabled even if there is no request.	RW	0
7:6	RESERVED		R	0x0
5	HSDIVIDER_CLKOUT1_DIVCHACK	Toggle on this status bit after changing HSDIVIDER_CLKOUT1_DIV indicates that the change in divider value has taken effect.	R	0
4:0	HSDIVIDER_CLKOUT1_DIV	DPLL M4 post-divider factor (1 to 31) 0x0: Reserved 0x6: 6, to be used for OPP100 and OPP50 (when DPLL_PER is locked at 768 MHz) 0xC: 12, to be used for OPP100 and OPP50 (when DPLL_PER is locked at 1536 MHz)	RW	0x04

Table 3-1136. Register Call Summary for Register CM_DIV_M4_DPLL_PER

Clock Management Functional Description • DPLL_PER Description: [0] [1] [2] [3] [4]
PRCM Register Manual • CKGEN_CM2 Register Summary: [5]

Table 3-1137. CM_DIV_M5_DPLL_PER

Address Offset	0x0000 005C		
Physical Address	0x4A00 815C	**Instance**	CKGEN_CM2
Description	This register provides controls over the CLKOUT2 o/p of the HSDIVIDER.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																			HSDIVIDER_CLKOUT2_PWDN	RESERVED		ST_HSDIVIDER_CLKOUT2	HSDIVIDER_CLKOUT2_GATE_CTRL	RESERVED		HSDIVIDER_CLKOUT2_DIVCHACK	HSDIVIDER_CLKOUT2_DIV							

Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000
12	HSDIVIDER_CLKOUT2_PWDN	Direct power down control for HSDIVIDER M5 divider and CLKOUT2 output. Power down should be enabled only when clock is first gated. 0x0: Divider is powered up. 0x1: Divider is powered down.	RW	0

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Bits	Field Name	Description	Type	Reset
11:10	RESERVED		R	0x0
9	ST_HSDIVIDER_CLKOUT2	HSDIVIDER CLKOUT2 status Read 0x0: The clock output is gated. Read 0x1: The clock output is enabled.	R	0
8	HSDIVIDER_CLKOUT2_GATE_CTRL	Control gating of HSDIVIDER CLKOUT2 0x0: Automatically gate this clock when there is no dependency for it. 0x1: Force this clock to stay enabled even if there is no request.	RW	0
7:6	RESERVED		R	0x0
5	HSDIVIDER_CLKOUT2_DIVCHACK	Toggle on this status bit after changing HSDIVIDER_CLKOUT2_DIV indicates that the change in divider value has taken effect.	R	0
4:0	HSDIVIDER_CLKOUT2_DIV	DPLL M5 post-divider factor (1 to 31) 0x0: Reserved 0x5: 5, to be used for OPP100 and OPP50 (when DPLL_PER is locked at 768 MHz) 0x9: 9, to be used for OPP100 and OPP50 (when DPLL_PER is locked at 1536 MHz)	RW	0x04

Table 3-1138. Register Call Summary for Register CM_DIV_M5_DPLL_PER

Clock Management Functional Description • DPLL_PER Description: [0] [1] [2] [3] [4]
PRCM Register Manual • CKGEN_CM2 Register Summary: [5]

Table 3-1139. CM_DIV_M6_DPLL_PER

Address Offset	0x0000 0060		
Physical Address	0x4A00 8160	**Instance**	CKGEN_CM2
Description	This register provides controls over the CLKOUT3 o/p of the HSDIVIDER.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																			HSDIVIDER_CLKOUT3_PWDN	RESERVED		ST_HSDIVIDER_CLKOUT3	HSDIVIDER_CLKOUT3_GATE_CTRL	RESERVED		HSDIVIDER_CLKOUT3_DIVCHACK	HSDIVIDER_CLKOUT3_DIV					

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Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000
12	HSDIVIDER_CLKOUT3_PWDN	Direct power down control for HSDIVIDER M6 divider and CLKOUT3 output. Power down should be enabled only when clock is first gated. 0x0: Divider is powered up. 0x1: Divider is powered down.	RW	0
11:10	RESERVED		R	0x0
9	ST_HSDIVIDER_CLKOUT3	HSDIVIDER CLKOUT3 status Read 0x0: The clock output is gated. Read 0x1: The clock output is enabled.	R	0
8	HSDIVIDER_CLKOUT3_GATE_CTRL	Control gating of HSDIVIDER CLKOUT3 0x0: Automatically gate this clock when there is no dependency for it. 0x1: Force this clock to stay enabled even if there is no request.	RW	0
7:6	RESERVED		R	0x0
5	HSDIVIDER_CLKOUT3_DIVCHACK	Toggle on this status bit after changing HSDIVIDER_CLKOUT3_DIV indicates that the change in divider value has taken effect.	R	0
4:0	HSDIVIDER_CLKOUT3_DIV	DPLL M6 post-divider factor (1 to 31) 0x0: Reserved 0x2: 2, to be used for OPP100 (when DPLL_PER is locked at 768 MHz) 0x4: 4, to be used for OPP100 (when DPLL_PER is locked at 1536 MHz) and for OPP50 (when DPLL_PER is locked at 768 MHz) 0x8: 8, to be used for OPP50 (when DPLL_PER is locked at 1536 MHz)	RW	0x04

Table 3-1140. Register Call Summary for Register CM_DIV_M6_DPLL_PER

Clock Management Functional Description • DPLL_PER Description: [0] [1] [2] [3] [4]
PRCM Register Manual • CKGEN_CM2 Register Summary: [5]

Table 3-1141. CM_DIV_M7_DPLL_PER

Address Offset	0x0000 0064		
Physical Address	0x4A00 8164	**Instance**	CKGEN_CM2
Description	This register provides controls over the CLKOUT4 o/p of the HSDIVIDER.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																			HSDIVIDER_CLKOUT4_PWDN	RESERVED		ST_HSDIVIDER_CLKOUT4	HSDIVIDER_CLKOUT4_GATE_CTRL	RESERVED		HSDIVIDER_CLKOUT4_DIVCHACK	HSDIVIDER_CLKOUT4_DIV					

Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000
12	HSDIVIDER_CLKOUT4_PWDN	Direct power down control for HSDIVIDER M7 divider and CLKOUT4 output. Power down should be enabled only when clock is first gated. 0x0: Divider is powered up. 0x1: Divider is powered down.	RW	0
11:10	RESERVED		R	0x0
9	ST_HSDIVIDER_CLKOUT4	HSDIVIDER CLKOUT4 status Read 0x0: The clock output is gated. Read 0x1: The clock output is enabled.	R	0
8	HSDIVIDER_CLKOUT4_GATE_CTRL	Control gating of HSDIVIDER CLKOUT4 0x0: Automatically gate this clock when there is no dependency for it. 0x1: Force this clock to stay enabled even if there is no request.	RW	0
7:6	RESERVED		R	0x0
5	HSDIVIDER_CLKOUT4_DIVCHACK	Toggle on this status bit after changing HSDIVIDER_CLKOUT4_DIV indicates that the change in divider value has taken effect.	R	0
4:0	HSDIVIDER_CLKOUT4_DIV	DPLL M7 post-divider factor (1 to 31) 0x0: Reserved 0x3: 3, to be used for OPP100 (when DPLL_PER is locked at 768 MHz) 0x5: 5, to be used for OPP100 (when DPLL_PER is locked at 1536 MHz) 0x6: 6, to be used for OPP50 (when DPLL_PER is locked at 768 MHz) 0xA: 10, to be used for OPP50 (when DPLL_PER is locked at 1536 MHz)	RW	0x04

Table 3-1142. Register Call Summary for Register CM_DIV_M7_DPLL_PER

Clock Management Functional Description
- DPLL_PER Description: [0] [1] [2] [3] [4]

PRCM Register Manual
- CKGEN_CM2 Register Summary: [5]

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Table 3-1143. CM_SSC_DELTAMSTEP_DPLL_PER

Address Offset	0x0000 0068		
Physical Address	0x4A00 8168	**Instance**	CKGEN_CM2
Description	Control the DeltaMStep parameter for Spread Spectrum Clocking. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								DELTAMSTEP																							

Bits	Field Name	Description	Type	Reset
31:20	RESERVED		R	0x000
19:0	DELTAMSTEP	DeltaMStep is split into fractional and integer part. For Triangular Spread Spectrum: [19:18] for integer part, [17:0] for fractional part For Square Wave Spread Spectrum [19:14] for integer part, [13:0] for fractional part	RW	0x00000

Table 3-1144. Register Call Summary for Register CM_SSC_DELTAMSTEP_DPLL_PER

Clock Management Functional Description
- DPLL_PER Description: [0]

PRCM Register Manual
- CKGEN_CM2 Register Summary: [1]

Table 3-1145. CM_SSC_MODFREQDIV_DPLL_PER

Address Offset	0x0000 006C		
Physical Address	0x4A00 816C	**Instance**	CKGEN_CM2
Description	Control the Modulation Frequency (Fm) for Spread Spectrum. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																					MODFREQDIV_EXPONENT			RESERVED	MODFREQDIV_MANTISSA						

Bits	Field Name	Description	Type	Reset
31:11	RESERVED		R	0x000000
10:8	MODFREQDIV_EXPONENT	Set the Exponent component of MODFREQDIV factor	RW	0x0
7	RESERVED		R	0
6:0	MODFREQDIV_MANTISSA	Set the Mantissa component of MODFREQDIV factor	RW	0x00

Table 3-1146. Register Call Summary for Register CM_SSC_MODFREQDIV_DPLL_PER

Clock Management Functional Description
- DPLL_PER Description: [0] [1]

PRCM Register Manual
- CKGEN_CM2 Register Summary: [2]

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Table 3-1147. CM_CLKMODE_DPLL_USB

Address Offset	0x0000 0080		
Physical Address	0x4A00 8180	**Instance**	CKGEN_CM2
Description	This register allows controlling the DPLL modes.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																	DPLL_SSC_DOWNSPREAD	DPLL_SSC_ACK	DPLL_SSC_EN	RESERVED										DPLL_EN	

Bits	Field Name	Description	Type	Reset
31:15	RESERVED		R	0x00000
14	DPLL_SSC_DOWNSPREAD	Control if only low frequency spread is required 0x0: When SSC is enabled, clock frequency is spread on both sides of the programmed frequency 0x1: When SSC is enabled, clock frequency is spread only on the lower side of the programmed frequency	RW	0
13	DPLL_SSC_ACK	Acknowledgement from the DPLL regarding start and stop of Spread Spectrum Clocking feature Read 0x0: SSC has been turned off on PLL o/ps Read 0x1: SSC has been turned on on PLL o/ps	R	0
12	DPLL_SSC_EN	Enable or disable Spread Spectrum Clocking 0x0: SSC disabled 0x1: SSC enabled	RW	0
11:3	RESERVED		R	0x000
2:0	DPLL_EN	DPLL control. Upon Warm Reset, the PRCM DPLL control state machine updates this register to reflect DPLL low-power stop mode. 0x0: Reserved 0x1: Put the DPLL in low-power stop mode 0x2: Reserved2 0x3: Reserved 0x4: Put the DPLL in MN bypass mode. The DPLL_MULT register bits are reset to 0 automatically by putting the DPLL in this mode. 0x5: Put the DPLL in idle bypass low-power mode. 0x6: Reserved 0x7: Enables the DPLL in lock mode	RW	0x4

Table 3-1148. Register Call Summary for Register CM_CLKMODE_DPLL_USB

Clock Management Functional Description
- DPLL_USB Description: [0] [1] [2] [3]

PRCM Register Manual
- CKGEN_CM2 Register Summary: [4]

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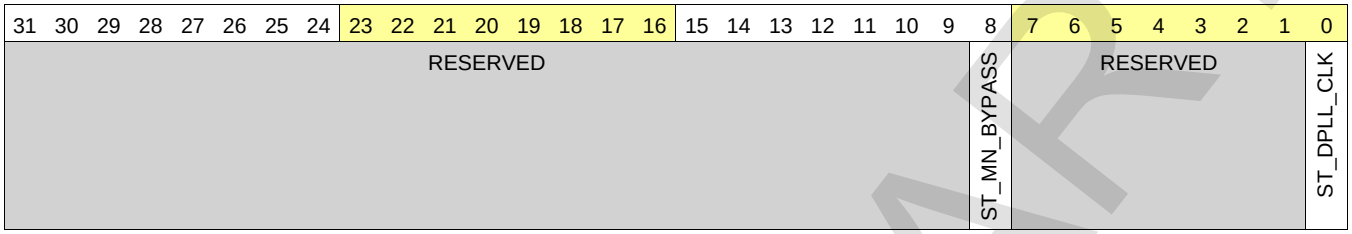
Table 3-1149. CM_IDLEST_DPLL_USB

Address Offset	0x0000 0084		
Physical Address	0x4A00 8184	**Instance**	CKGEN_CM2
Description	This register allows monitoring DPLL activity. This register is read only and automatically updated. [warm reset insensitive]		
Type	R		



Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	ST_MN_BYPASS	DPLL MN_BYPASS status Read 0x1: DPLL is in MN_Bypass Read 0x0: DPLL is not in MN_Bypass	R	0
7:1	RESERVED		R	0x00
0	ST_DPLL_CLK	DPLL lock status Read 0x1: DPLL is LOCKED Read 0x0: DPLL is either in bypass mode or in stop mode.	R	0

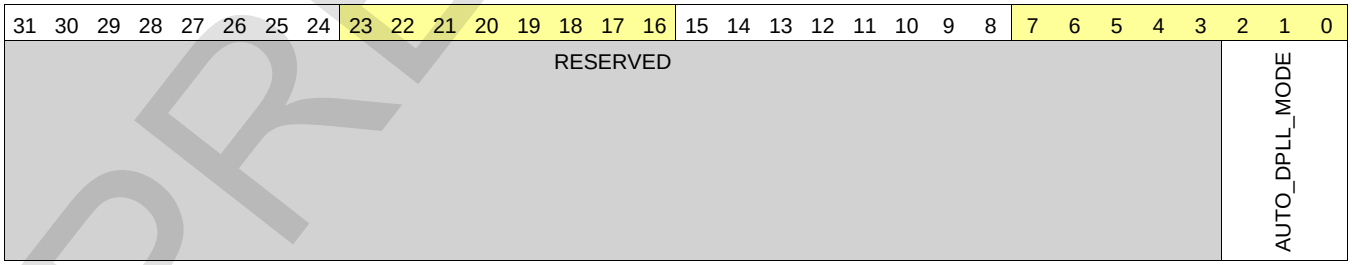
Table 3-1150. Register Call Summary for Register CM_IDLEST_DPLL_USB

PRCM Register Manual

- CKGEN_CM2 Register Summary: [0]

Table 3-1151. CM_AUTOIDLE_DPLL_USB

Address Offset	0x0000 0088		
Physical Address	0x4A00 8188	**Instance**	CKGEN_CM2
Description	This register provides automatic control over the DPLL activity.		
Type	RW		



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Bits	Field Name	Description	Type	Reset
31:3	RESERVED		R	0x0000 0000
2:0	AUTO_DPLL_MODE	DPLL automatic control; 0x0: DPLL auto control disabled 0x1: The DPLL is automatically put in low-power stop mode when its DPLL generated clocks are not required anymore. It is also restarted automatically. 0x2: Reserved 0x3: Reserved 0x4: Reserved 0x5: The DPLL is automatically put in idle bypass low-power mode when its DPLL generated clocks are not required anymore. It is also restarted automatically. 0x6: Reserved 0x7: Reserved	RW	0x0

Table 3-1152. Register Call Summary for Register CM_AUTOIDLE_DPLL_USB

Clock Management Functional Description • DPLL_USB Description: [0]
PRCM Register Manual • CKGEN_CM2 Register Summary: [1]

Table 3-1153. CM_CLKSEL_DPLL_USB

Address Offset	0x0000 008C		
Physical Address	0x4A00 818C	**Instance**	CKGEN_CM2
Description	This register provides controls over the DPLL.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DPLL_SD_DIV								DPLL_BYP_CLKSEL	RESERVED							DPLL_MULT								DPLL_DIV							

Bits	Field Name	Description	Type	Reset
31:24	DPLL_SD_DIV	Sigma-Delta divider select (2-255). This factor must be set by s/w to ensure optimum jitter performance. DPLL_SD_DIV = CEILING ([DPLL_MULT/(DPLL_DIV+1)] * CLKINP / 250), where CLKINP is the input clock of the DPLL in MHz). Must be set with M and N factors, and must not be changed once DPLL is locked. 0x0: Reserved 0x1: Reserved	RW	0x04
23	DPLL_BYP_CLKSEL	Allows control of the BYPASS clock of the PLL and the associated HSDIVIDER. Same as ULOWCLKEN on DPLL. In DPLL locked mode, 0 - No impact 1 - No impact In DPLL bypass mode, 0 - CLKINP is selected as the BYPASS clock for CLKOUT 1 - CLKINPULOW is selected as the BYPASS clock for CLKOUT	RW	0
22:20	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
19:8	DPLL_MULT	DPLL multiplier factor (2 to 4095). This register is automatically cleared to 0 when the DPLL_EN field in the *CLKMODE_DPLL* register is set to select MN bypass mode. (equal to input M of DPLL; M=2 to 4095 = DPLL multiplies by M). 0x0: Reserved 0x1: Reserved	RW	0x000
7:0	DPLL_DIV	DPLL divider factor (0 to 255) (equal to input N of DPLL; actual division factor is N+1).	RW	0x00

Table 3-1154. Register Call Summary for Register CM_CLKSEL_DPLL_USB

Clock Management Functional Description • DPLL_USB Description: [0] [1]
PRCM Register Manual • CKGEN_CM2 Register Summary: [2]

Table 3-1155. CM_DIV_M2_DPLL_USB

Address Offset	0x0000 0090		
Physical Address	0x4A00 8190	**Instance**	CKGEN_CM2
Description	This register provides controls over the M2 divider of the DPLL.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						ST_DPLL_CLKOUT	DPLL_CLKOUT_GATE_CTRL	DPLL_CLKOUT_DIVCHACK	DPLL_CLKOUT_DIV						

Bits	Field Name	Description	Type	Reset
31:10	RESERVED		R	0x00000
9	ST_DPLL_CLKOUT	DPLL CLKOUT status Read 0x0: The clock output is gated. Read 0x1: The clock output is enabled.	R	0
8	DPLL_CLKOUT_GATE_CTRL	Control gating of DPLL CLKOUT 0x0: Automatically gate this clock when there is no dependency for it. 0x1: Force this clock to stay enabled even if there is no request.	RW	0
7	DPLL_CLKOUT_DIVCHACK	Toggle on this status bit after changing DPLL_CLKOUT_DIV indicates that the change in divider value has taken effect.	R	0
6:0	DPLL_CLKOUT_DIV	DPLL post-divider factor, M2, for internal clock generation (1 to 127) 0x0: Reserved 0x2: 2, to be used for OPP100 and OPP50	RW	0x01

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Table 3-1156. Register Call Summary for Register CM_DIV_M2_DPLL_USB

Clock Management Functional Description • DPLL_USB Description: [0] [1] [2] [3]
PRCM Register Manual • CKGEN_CM2 Register Summary: [4]

Table 3-1157. CM_SSC_DELTAMSTEP_DPLL_USB

Address Offset	0x0000 00A8		
Physical Address	0x4A00 81A8	**Instance**	CKGEN_CM2
Description	Control the DeltaMStep parameter for Spread Spectrum Clocking. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								DELTAMSTEP																							

Bits	Field Name	Description	Type	Reset
31:21	RESERVED		R	0x000
20:0	DELTAMSTEP	DeltaMStep is split into fractional and integer part. For Triangular Spread Spectrum: [20:18] for integer part, [17:0] for fractional part For Square Wave Spread Spectrum [19:14] for integer part, [13:0] for fractional part	RW	0x00000

Table 3-1158. Register Call Summary for Register CM_SSC_DELTAMSTEP_DPLL_USB

Clock Management Functional Description • DPLL_USB Description: [0]
PRCM Register Manual • CKGEN_CM2 Register Summary: [1]

Table 3-1159. CM_SSC_MODFREQDIV_DPLL_USB

Address Offset	0x0000 00AC		
Physical Address	0x4A00 81AC	**Instance**	CKGEN_CM2
Description	Control the Modulation Frequency (Fm) for Spread Spectrum. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																					MODFREQDIV_EXPONENT			RESERVED	MODFREQDIV_MANTISSA						

Bits	Field Name	Description	Type	Reset
31:11	RESERVED		R	0x000000
10:8	MODFREQDIV_EXPONENT	Set the Exponent component of MODFREQDIV factor	RW	0x0
7	RESERVED		R	0
6:0	MODFREQDIV_MANTISSA	Set the Mantissa component of MODFREQDIV factor	RW	0x00

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Table 3-1160. Register Call Summary for Register CM_SSC_MODFREQDIV_DPLL_USB

Clock Management Functional Description • DPLL_USB Description: [0] [1]
PRCM Register Manual • CKGEN_CM2 Register Summary: [2]

Table 3-1161. CM_CLKDCOLDO_DPLL_USB

Address Offset	0x0000 00B4		
Physical Address	0x4A00 81B4	**Instance**	CKGEN_CM2
Description	This register provides controls over the CLKDCOLDO output of the DPLL.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						ST_DPLL_CLKDCOLDO	DPLL_CLKDCOLDO_GATE_CTRL	RESERVED							

Bits	Field Name	Description	Type	Reset
31:10	RESERVED		R	0x000000
9	ST_DPLL_CLKDCOLDO	DPLL CLKDCOLDO status Read 0x0: The clock output is gated Read 0x1: The clock output is enabled	R	0
8	DPLL_CLKDCOLDO_GATE_CTRL	Control gating of DPLL CLKDCOLDO 0x0: Automatically gate this clock when there is no request for it 0x1: Force this clock to stay enabled even if there is no request	RW	0
7:0	RESERVED		R	0x00

Table 3-1162. Register Call Summary for Register CM_CLKDCOLDO_DPLL_USB

PRCM Register Manual • CKGEN_CM2 Register Summary: [0]

3.11.32 ALWAYS_ON_CM2 Registers

3.11.32.1 ALWAYS_ON_CM2 Register Summary

Table 3-1163. ALWAYS_ON_CM2 Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	ALWAYS_ON_CM2 L4 Base Address
CM_ALWON_CLKSTCTRL	RW	32	0x0000 0000	0x4A00 8600
RESERVED	R	32	0x0000 0020	0x4A00 8620

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Table 3-1163. ALWAYS_ON_CM2 Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	ALWAYS_ON_CM2 L4 Base Address
CM_ALWON_SR_MPU_CLKCTRL	RW	32	0x0000 0028	0x4A00 8628
CM_ALWON_SR_IVA_CLKCTRL	RW	32	0x0000 0030	0x4A00 8630
CM_ALWON_SR_CORE_CLKCTRL	RW	32	0x0000 0038	0x4A00 8638
CM_ALWON_USBPHY_CLKCTRL	RW	32	0x0000 0040	0x4A00 8640

3.11.32.2 ALWAYS_ON_CM2 Register Description

Table 3-1164. CM_ALWON_CLKSTCTRL

Address Offset	0x0000 0000		
Physical Address	0x4A00 8600	**Instance**	ALWAYS_ON_CM2
Description	This register enables the domain power state transition. It controls the hardware supervised domain power state transition between ON-ACTIVE and ON-INACTIVE states. It also holds 1 status bit per clock input of the domain.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																			CLKACTIVITY_CORE_ALWON_32K_GFCLK	CLKACTIVITY_SR_CORE_SYSCLK	CLKACTIVITY_SR_IVA_SYSCLK	CLKACTIVITY_SR_MPU_SYSCLK	CLKACTIVITY_L4_AO_ICLK	RESERVED							CLKTRCTRL	

Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000
12	CLKACTIVITY_CORE_ALWON_32K_GFCLK	This field indicates the state of the CORE_ALWON_32K_GFCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated. Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing.	R	0
11	CLKACTIVITY_SR_CORE_SYSCLK	This field indicates the state of the SR_CORE_SYSCLK clock input of the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
10	CLKACTIVITY_SR_IVA_SYSCLK	This field indicates the state of the SR_IVA_SYSCLK clock input of the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0

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Bits	Field Name	Description	Type	Reset
9	CLKACTIVITY_SR_MPU_SYSCLK	This field indicates the state of the SR_MPU_SYSCLK clock input of the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
8	CLKACTIVITY_L4_AO_ICLK	This field indicates the state of the L4_AO_ICLK clock of the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
7:2	RESERVED		R	0x00
1:0	CLKTRCTRL	Controls the clock state transition of the ALWONCORE clock domain. 0x0: NO_SLEEP: Sleep transition cannot be initiated. Wakeup transition may however occur. Read 0x1: Reserved 0x2: SW_WKUP: Start a software forced wake-up transition on the domain. 0x3: HW_AUTO: Automatic transition is enabled. Sleep and wakeup transition are based upon hardware conditions.	RW	0x3

Table 3-1165. Register Call Summary for Register CM_ALWON_CLKSTCTRL

PRCM Register Manual
- ALWAYS_ON_CM2 Register Summary: [0]

Table 3-1166. CM_ALWON_SR_MPU_CLKCTRL

Address Offset	0x0000 0028		
Physical Address	0x4A00 8628	**Instance**	ALWAYS_ON_CM2
Description	This register manages the SR_MPU clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED								MODULEMODE							

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000

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Bits	Field Name	Description	Type	Reset
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by software. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen. Read 0x3: Reserved	RW	0x0

Table 3-1167. Register Call Summary for Register CM_ALWON_SR_MPU_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • ALWAYS_ON_CM2 Register Summary: [2]

Table 3-1168. CM_ALWON_SR_IVA_CLKCTRL

Address Offset	0x0000 0030		
Physical Address	0x4A00 8630	**Instance**	ALWAYS_ON_CM2
Description	This register manages the SR_IVA clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED								MODULEMODE							

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by software. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen. Read 0x3: Reserved	RW	0x0

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Table 3-1169. Register Call Summary for Register CM_ALWON_SR_IVA_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • ALWAYS_ON_CM2 Register Summary: [2]

Table 3-1170. CM_ALWON_SR_CORE_CLKCTRL

Address Offset	0x0000 0038		
Physical Address	0x4A00 8638	**Instance**	ALWAYS_ON_CM2
Description	This register manages the SR_CORE clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED								MODULEMODE							

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by software. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen. Read 0x3: Reserved	RW	0x0

Table 3-1171. Register Call Summary for Register CM_ALWON_SR_CORE_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • ALWAYS_ON_CM2 Register Summary: [2]

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Table 3-1172. CM_ALWON_USBPHY_CLKCTRL

Address Offset	0x0000 0040		
Physical Address	0x4A00 8640	**Instance**	ALWAYS_ON_CM2
Description	This register manages the USB PHY 32KHz clock.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							OPTFCLKEN_CLK32K	RESERVED							

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	OPTFCLKEN_CLK32K	Optional functional clock control. 0x0: Optional functional clock is disabled 0x1: Optional functional clock is enabled	RW	0
7:0	RESERVED		R	0x00

Table 3-1173. Register Call Summary for Register CM_ALWON_USBPHY_CLKCTRL

PRCM Register Manual
- ALWAYS_ON_CM2 Register Summary: [0]

3.11.33 CORE_CM2 Registers

3.11.33.1 CORE_CM2 Register Summary

Table 3-1174. CORE_CM2 Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	CORE_CM2 L4 Base Address
CM_L3_1_CLKSTCTRL	RW	32	0x0000 0000	0x4A00 8700
CM_L3_1_DYNAMICDEP	RW	32	0x0000 0008	0x4A00 8708
CM_L3_1_L3_1_CLKCTRL	R	32	0x0000 0020	0x4A00 8720
CM_L3_2_CLKSTCTRL	RW	32	0x0000 0100	0x4A00 8800
CM_L3_2_DYNAMICDEP	RW	32	0x0000 0108	0x4A00 8808
CM_L3_2_L3_2_CLKCTRL	R	32	0x0000 0120	0x4A00 8820
CM_L3_2_GPMC_CLKCTRL	RW	32	0x0000 0128	0x4A00 8828
CM_L3_2_OCMC_RAM_CLKCTRL	R	32	0x0000 0130	0x4A00 8830
CM_MPU_M3_CLKSTCTRL	RW	32	0x0000 0200	0x4A00 8900
CM_MPU_M3_STATICDEP	RW	32	0x0000 0204	0x4A00 8904
CM_MPU_M3_DYNAMICDEP	RW	32	0x0000 0208	0x4A00 8908
CM_MPU_M3_MPU_M3_CLKCTRL	RW	32	0x0000 0220	0x4A00 8920
CM_SDMA_CLKSTCTRL	RW	32	0x0000 0300	0x4A00 8A00
CM_SDMA_STATICDEP	RW	32	0x0000 0304	0x4A00 8A04
CM_SDMA_DYNAMICDEP	R	32	0x0000 0308	0x4A00 8A08
CM_SDMA_SDMA_CLKCTRL	R	32	0x0000 0320	0x4A00 8A20

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Table 3-1174. CORE_CM2 Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	CORE_CM2 L4 Base Address
CM_MEMIF_CLKSTCTRL	RW	32	0x0000 0400	0x4A00 8B00
CM_MEMIF_DMM_CLKCTRL	R	32	0x0000 0420	0x4A00 8B20
CM_MEMIF_EMIF_FW_CLKCTRL	R	32	0x0000 0428	0x4A00 8B28
CM_MEMIF_EMIF_1_CLKCTRL	RW	32	0x0000 0430	0x4A00 8B30
CM_MEMIF_EMIF_2_CLKCTRL	RW	32	0x0000 0438	0x4A00 8B38
CM_MEMIF_DLL_CLKCTRL	RW	32	0x0000 0440	0x4A00 8B40
RESERVED	RW	32	0x0000 0450	0x4A00 8B50
RESERVED	RW	32	0x0000 0458	0x4A00 8B58
RESERVED	RW	32	0x0000 0460	0x4A00 8B60
CM_C2C_CLKSTCTRL	RW	32	0x0000 0500	0x4A00 8C00
CM_C2C_STATICDEP	RW	32	0x0000 0504	0x4A00 8C04
CM_C2C_DYNAMICDEP	RW	32	0x0000 0508	0x4A00 8C08
CM_C2C_C2C_CLKCTRL	R	32	0x0000 0520	0x4A00 8C20
RESERVED	R	32	0x0000 0528	0x4A00 8C28
CM_C2C_C2C_FW_CLKCTRL	R	32	0x0000 0530	0x4A00 8C30
CM_L4CFG_CLKSTCTRL	RW	32	0x0000 0600	0x4A00 8D00
CM_L4CFG_DYNAMICDEP	RW	32	0x0000 0608	0x4A00 8D08
CM_L4CFG_L4_CFG_CLKCTRL	R	32	0x0000 0620	0x4A00 8D20
CM_L4CFG_SPINLOCK_CLKCTRL	R	32	0x0000 0628	0x4A00 8D28
CM_L4CFG_MAILBOX_CLKCTRL	R	32	0x0000 0630	0x4A00 8D30
CM_L4CFG_SAR_ROM_CLKCTRL	R	32	0x0000 0638	0x4A00 8D38
CM_L3INSTR_CLKSTCTRL	R	32	0x0000 0700	0x4A00 8E00
CM_L3INSTR_L3_3_CLKCTRL	RW	32	0x0000 0720	0x4A00 8E20
CM_L3INSTR_L3_INSTR_CLKCTRL	RW	32	0x0000 0728	0x4A00 8E28
CM_L3INSTR_OCP_WP1_CLKCTRL	RW	32	0x0000 0740	0x4A00 8E40

3.11.33.2 CORE_CM2 Register Description

Table 3-1175. CM_L3_1_CLKSTCTRL

Address Offset	0x0000 0000		
Physical Address	0x4A00 8700	**Instance**	CORE_CM2
Description	This register enables the domain power state transition. It controls the hardware supervised domain power state transition between ON-ACTIVE and ON-INACTIVE states. It also holds 1 status bit per clock input of the domain.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							CLKACTIVITY_L3_1_ICLK	RESERVED						CLKTRCTRL	

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Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	CLKACTIVITY_L3_1_ICLK	This field indicates the state of the L3_1_ICLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
7:2	RESERVED		R	0x00
1:0	CLKTRCTRL	Controls the clock state transition of the L3_1 clock domain. 0x0: NO_SLEEP: Sleep transition cannot be initiated. Wakeup transition may however occur. Read 0x1: Reserved Read 0x2: Reserved 0x3: HW_AUTO: Automatic transition is enabled. Sleep and wakeup transition are based upon hardware conditions.	RW	0x0

Table 3-1176. Register Call Summary for Register CM_L3_1_CLKSTCTRL

Clock Management Functional Description • Clock Domain Modes: [0] [1]
PRCM Register Manual • CORE_CM2 Register Summary: [2] • RESTORE_CM2 Register Description: [3]

Table 3-1177. CM_L3_1_DYNAMICDEP

Address Offset	0x0000 0008		
Physical Address	0x4A00 8708	**Instance**	CORE_CM2
Description	This register controls the dynamic domain depedencies from L3_1 domain towards 'target' domains. It is relevant only for domain having INTRCONN master port(s).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				WINDOWSIZE				RESERVED											L4CFG_DYNDEP	RESERVED						L3_2_DYNDEP	RESERVED	MEMIF_DYNDEP	ABE_DYNDEP	RESERVED		

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:24	WINDOWSIZE	Size of sliding window used to monitor INTRCONN interface activity for determination of auto-sleep feature. Time unit defined by CM_DYN_DEP_PRESCAL register.	RW	0x4
23:13	RESERVED		R	0x000
12	L4CFG_DYNDEP	Dynamic dependency towards L4CFG clock domain Read 0x1: Dependency is enabled	R Rreturns 1s	1
11:7	RESERVED		R	0x00
6	L3_2_DYNDEP	Dynamic dependency towards L3_2 clock domain Read 0x1: Dependency is enabled	R Rreturns 1s	1
5	RESERVED		R	0

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Bits	Field Name	Description	Type	Reset
4	MEMIF_DYNDEP	Dynamic dependency towards MEMIF clock domain Read 0x1: Dependency is enabled	R Rreturns 1s	1
3	ABE_DYNDEP	Dynamic dependency towards ABE clock domain Read 0x1: Dependency is enabled	R Rreturns 1s	1
2:0	RESERVED		R	0x0

Table 3-1178. Register Call Summary for Register CM_L3_1_DYNAMICDEP

Clock Management Functional Description • Clock Domain Dependency: [0] [1] [2] [3]
PRCM Register Manual • CORE_CM2 Register Summary: [4] • RESTORE_CM2 Register Description: [5]

Table 3-1179. CM_L3_1_L3_1_CLKCTRL

Address Offset	0x0000 0020		
Physical Address	0x4A00 8720	**Instance**	CORE_CM2
Description	This register manages the L3_1 clocks.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED								MODULEMODE							

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. Read 0x1: Module is managed automatically by hardware according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CLKTRCTRL=3, any INTRCONN access to module is always granted. Module clocks may be gated according to the clock domain state.	R Rreturns	0x1

Table 3-1180. Register Call Summary for Register CM_L3_1_L3_1_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • CORE_CM2 Register Summary: [2]

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Table 3-1181. CM_L3_2_CLKSTCTRL

Address Offset	0x0000 0100		
Physical Address	0x4A00 8800	**Instance**	CORE_CM2
Description	This register enables the domain power state transition. It controls the hardware supervised domain power state transition between ON-ACTIVE and ON-INACTIVE states. It also holds 1 status bit per clock input of the domain.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							CLKACTIVITY_L3_2_ICLK	RESERVED						CLKTRCTRL	

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	CLKACTIVITY_L3_2_ICLK	This field indicates the state of the L3_2_ICLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
7:2	RESERVED		R	0x00
1:0	CLKTRCTRL	Controls the clock state transition of the L3_2 clock domain. 0x0: NO_SLEEP: Sleep transition cannot be initiated. Wakeup transition may however occur. Read 0x1: Reserved Read 0x2: Reserved 0x3: HW_AUTO: Automatic transition is enabled. Sleep and wakeup transition are based upon hardware conditions.	RW	0x0

Table 3-1182. Register Call Summary for Register CM_L3_2_CLKSTCTRL

Clock Management Functional Description
- Clock Domain Modes: [0] [1]

PRCM Register Manual
- CORE_CM2 Register Summary: [2]
- RESTORE_CM2 Register Description: [3]

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Table 3-1183. CM_L3_2_DYNAMICDEP

Address Offset	0x0000 0108		
Physical Address	0x4A00 8808	**Instance**	CORE_CM2
Description	This register controls the dynamic domain depedencies from L3_2 domain towards 'target' domains. It is relevant only for domain having INTRCONN master port(s).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				WINDOWSIZE				RESERVED										L4PER_DYNDEP	RESERVED		SGX_DYNDEP	CAM_DYNDEP	DSS_DYNDEP	L3_INIT_DYNDEP	RESERVED	L3_1_DYNDEP	RESERVED			IVAHD_DYNDEP	RESERVED	MPU_M3_DYNDEP

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:24	WINDOWSIZE	Size of sliding window used to monitor INTRCONN interface activity for determination of auto-sleep feature. Time unit defined by CM_DYN_DEP_PRESCAL register.	RW	0x4
23:14	RESERVED		R	0x000
13	L4PER_DYNDEP	Dynamic dependency towards L4PER clock domain Read 0x1: Dependency is enabled	R Rreturns 1s	1
12:11	RESERVED		R	0x0
10	SGX_DYNDEP	Dynamic dependency towards SGX clock domain Read 0x1: Dependency is enabled	R Rreturns 1s	1
9	CAM_DYNDEP	Dynamic dependency towards ISS clock domain Read 0x0: Dependency is disabled	R	0
8	DSS_DYNDEP	Dynamic dependency towards DSS clock domain Read 0x1: Dependency is enabled	R Rreturns 1s	1
7	L3_INIT_DYNDEP	Dynamic dependency towards L3INIT clock domain Read 0x1: Dependency is enabled	R Rreturns 1s	1
6	RESERVED		R	0
5	L3_1_DYNDEP	Dynamic dependency towards L3_1 clock domain Read 0x1: Dependency is enabled	R Rreturns 1s	1
4:3	RESERVED		R	0x0
2	IVAHD_DYNDEP	Dynamic dependency towards IVAHD clock domain Read 0x1: Dependency is enabled	R Rreturns 1s	1
1	RESERVED		R	0
0	MPU_M3_DYNDEP	Dynamic dependency towards CORTEXM3 clock domain Read 0x1: Dependency is enabled	R Rreturns 1s	1

Table 3-1184. Register Call Summary for Register CM_L3_2_DYNAMICDEP

Clock Management Functional Description
- Clock Domain Dependency: [0] [1] [2] [3] [4] [5] [6] [7] [8]

PRCM Register Manual
- CORE_CM2 Register Summary: [9]
- RESTORE_CM2 Register Description: [10]

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Table 3-1185. CM_L3_2_L3_2_CLKCTRL

Address Offset	0x0000 0120		
Physical Address	0x4A00 8820	**Instance**	CORE_CM2
Description	This register manages the L3_2 clocks.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED														MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. Read 0x1: Module is managed automatically by hardware according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CLKTRCTRL=3, any INTRCONN access to module is always granted. Module clocks may be gated according to the clock domain state.	R Rreturns	0x1

Table 3-1186. Register Call Summary for Register CM_L3_2_L3_2_CLKCTRL

Clock Management Functional Description
- Clock Domain Module Attributes: [0] [1]

PRCM Register Manual
- CORE_CM2 Register Summary: [2]

Table 3-1187. CM_L3_2_GPMC_CLKCTRL

Address Offset	0x0000 0128		
Physical Address	0x4A00 8828	**Instance**	CORE_CM2
Description	This register manages the GPMC clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED														MODULEMODE	

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Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is temporarily disabled by software. Interconnect access to module are stalled. Can be used to change timing parameter of GPMC module. 0x1: Module is managed automatically by hardware according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CLKTRCTRL=3, any INTRCONN access to module is always granted. Module clocks may be gated according to the clock domain state. Read 0x2: Reserved Read 0x3: Reserved	RW	0x1

Table 3-1188. Register Call Summary for Register CM_L3_2_GPMC_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • CORE_CM2 Register Summary: [2]

Table 3-1189. CM_L3_2_OCMC_RAM_CLKCTRL

Address Offset	0x0000 0130		
Physical Address	0x4A00 8830	**Instance**	CORE_CM2
Description	This register manages the OCMC_RAM clocks.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED														MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3

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Bits	Field Name	Description	Type	Reset
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. Read 0x1: Module is managed automatically by hardware according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CLKTRCTRL=3, any INTRCONN access to module is always granted. Module clocks may be gated according to the clock domain state.	R Rreturns	0x1

Table 3-1190. Register Call Summary for Register CM_L3_2_OCMC_RAM_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • CORE_CM2 Register Summary: [2]

Table 3-1191. CM_MPU_M3_CLKSTCTRL

Address Offset	0x0000 0200		
Physical Address	0x4A00 8900	**Instance**	CORE_CM2
Description	This register enables the domain power state transition. It controls the hardware supervised domain power state transition between ON-ACTIVE and ON-INACTIVE states. It also holds 1 status bit per clock input of the domain.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							CLKACTIVITY_MPU_M3_CLK	RESERVED						CLKTRCTRL	

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	CLKACTIVITY_MPU_M3_CLK	This field indicates the state of the MPU_M3_CLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
7:2	RESERVED		R	0x00
1:0	CLKTRCTRL	Controls the clock state transition of the MPU_A3 clock domain. 0x0: NO_SLEEP: Sleep transition cannot be initiated. Wakeup transition may however occur. 0x1: SW_SLEEP: Start a software forced sleep transition on the domain. 0x2: SW_WKUP: Start a software forced wake-up transition on the domain. 0x3: HW_AUTO: Automatic transition is enabled. Sleep and wakeup transition are based upon hardware conditions.	RW	0x3

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Table 3-1192. Register Call Summary for Register CM_MPU_M3_CLKSTCTRL

Clock Management Functional Description
• Clock Domain Modes: [0] [1]
PRCM Register Manual
• CORE_CM2 Register Summary: [2]

Table 3-1193. CM_MPU_M3_STATICDEP

Address Offset	0x0000 0204		
Physical Address	0x4A00 8904	**Instance**	CORE_CM2
Description	This register controls the static domain depedencies from MPU_A3 domain towards 'target' domains. It is relevant only for domain having system initiator(s).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															ALWONCORE_STATDEP	L4WKUP_STATDEP	RESERVED	L4PER_STATDEP	L4CFG_STATDEP	SDMA_STATDEP	SGX_STATDEP	ISS_STATDEP	DSS_STATDEP	L3INIT_STATDEP	L3_2_STATDEP	L3_1_STATDEP	MEMIF_STATDEP	ABE_STATDEP	IVAHD_STATDEP	DSP_STATDEP	RESERVED

Bits	Field Name	Description	Type	Reset
31:17	RESERVED		R	0x0000
16	ALWONCORE_STATDEP	Static dependency towards ALWONCORE clock domain Read 0x0: Dependency is disabled	R	0
15	L4WKUP_STATDEP	Static dependency towards L4WKUP clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	1
14	RESERVED		RW	0
13	L4PER_STATDEP	Static dependency towards L4PER clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
12	L4CFG_STATDEP	Static dependency towards L4CFG clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	1
11	SDMA_STATDEP	Static dependency towards SDMA clock domain Read 0x0: Dependency is disabled	R	0
10	SGX_STATDEP	Static dependency towards SGX clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
9	ISS_STATDEP	Static dependency towards ISS clock domain Read 0x0: Dependency is disabled	R	0
8	DSS_STATDEP	Static dependency towards DSS clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
7	L3INIT_STATDEP	Static dependency towards L3INIT clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

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Bits	Field Name	Description	Type	Reset
6	L3_2_STATDEP	Static dependency towards L3_2 clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	1
5	L3_1_STATDEP	Static dependency towards L3_1 clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	1
4	MEMIF_STATDEP	Static dependency towards MEMIF clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	1
3	ABE_STATDEP	Static dependency towards ABE clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
2	IVAHD_STATDEP	Static dependency towards IVAHD clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
1	DSP_STATDEP	Static dependency towards DSP clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
0	RESERVED		R	0

Table 3-1194. Register Call Summary for Register CM_MPU_M3_STATICDEP

Clock Management Functional Description • Clock Domain Dependency: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12]
PRCM Register Manual • CORE_CM2 Register Summary: [13]

Table 3-1195. CM_MPU_M3_DYNAMICDEP

Address Offset	0x0000 0208		
Physical Address	0x4A00 8908	**Instance**	CORE_CM2
Description	This register controls the dynamic domain depedencies from MPU_A3 domain towards 'target' domains. It is relevant only for domain having INTRCONN master port(s).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				WINDOWSIZE				RESERVED														CAM_DYNDEP	RESERVED	L3_2_DYNDEP	RESERVED						

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:24	WINDOWSIZE	Size of sliding window used to monitor INTRCONN interface activity for determination of auto-sleep feature. Time unit defined by CM_DYN_DEP_PRESCAL register.	RW	0x4
23:10	RESERVED		R	0x0000
9	CAM_DYNDEP	Dynamic dependency towards ISS clock domain Read 0x0: Dependency is disabled	R	0
8:7	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
6	L3_2_DYNDEP	Dynamic dependency towards L3_2 clock domain Read 0x1: Dependency is enabled	R Rreturns 1s	1
5:0	RESERVED		R	0x00

Table 3-1196. Register Call Summary for Register CM_MPU_M3_DYNAMICDEP

Clock Management Functional Description • Clock Domain Dependency: [0] [1]
PRCM Register Manual • CORE_CM2 Register Summary: [2]

Table 3-1197. CM_MPU_M3_MPU_M3_CLKCTRL

Address Offset	0x0000 0220		
Physical Address	0x4A00 8920	**Instance**	CORE_CM2
Description	This register manages the MPU_A3 clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													STBYST	IDLEST		RESERVED														MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:19	RESERVED		R	0x0000
18	STBYST	Module standby status. [warm reset insensitive] Read 0x0: Module is functional (not in standby) Read 0x1: Module is in standby	R	1
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by software. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). 0x1: Module is managed automatically by hardware according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CLKTRCTRL=3, any INTRCONN access to module is always granted. Module clocks may be gated according to the clock domain state. Read 0x2: Reserved Read 0x3: Reserved	RW	0x0

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Table 3-1198. Register Call Summary for Register CM_MPU_M3_MPU_M3_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1] [2]
PRCM Register Manual • CORE_CM2 Register Summary: [3]

Table 3-1199. CM_SDMA_CLKSTCTRL

Address Offset	0x0000 0300		
Physical Address	0x4A00 8A00	**Instance**	CORE_CM2
Description	This register enables the domain power state transition. It controls the hardware supervised domain power state transition between ON-ACTIVE and ON-INACTIVE states. It also holds 1 status bit per clock input of the domain.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							CLKACTIVITY_DMA_L3_ICLK	RESERVED						CLKTRCTRL	

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	CLKACTIVITY_DMA_L3_ICLK	This field indicates the state of the DMA_L3_ICLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
7:2	RESERVED		R	0x00
1:0	CLKTRCTRL	Controls the clock state transition of the SDMA clock domain. 0x0: NO_SLEEP: Sleep transition cannot be initiated. Wakeup transition may however occur. Read 0x1: Reserved 0x2: SW_WKUP: Start a software forced wake-up transition on the domain. 0x3: HW_AUTO: Automatic transition is enabled. Sleep and wakeup transition are based upon hardware conditions.	RW	0x3

Table 3-1200. Register Call Summary for Register CM_SDMA_CLKSTCTRL

Clock Management Functional Description • Clock Domain Modes: [0] [1]
PRCM Register Manual • CORE_CM2 Register Summary: [2]

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Table 3-1201. CM_SDMA_STATICDEP

Address Offset	0x0000 0304		
Physical Address	0x4A00 8A04	**Instance**	CORE_CM2
Description	This register controls the static domain depedencies from SDMA domain towards 'target' domains. It is relevant only for domain having system initiator(s).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																L4WKUP_STATDEP	RESERVED	L4PER_STATDEP	L4CFG_STATDEP	RESERVED		ISS_STATDEP	DSS_STATDEP	L3INIT_STATDEP	L3_2_STATDEP	L3_1_STATDEP	MEMIF_STATDEP	ABE_STATDEP	IVAHD_STATDEP	RESERVED	MPU_M3_STATDEP

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15	L4WKUP_STATDEP	Static dependency towards L4WKUP clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	1
14	RESERVED		R	0
13	L4PER_STATDEP	Static dependency towards L4PER clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	1
12	L4CFG_STATDEP	Static dependency towards L4CFG clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	1
11:10	RESERVED		R	0x0
9	ISS_STATDEP	Static dependency towards ISS clock domain Read 0x0: Dependency is disabled	R	0
8	DSS_STATDEP	Static dependency towards DSS clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
7	L3INIT_STATDEP	Static dependency towards L3INIT clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	1
6	L3_2_STATDEP	Static dependency towards L3_2 clock domain Read 0x1: Dependency is enabled	R Rreturns 1s	1
5	L3_1_STATDEP	Static dependency towards L3_1 clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	1
4	MEMIF_STATDEP	Static dependency towards MEMIF clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	1
3	ABE_STATDEP	Static dependency towards ABE clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

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Bits	Field Name	Description	Type	Reset
2	IVAHD_STATDEP	Static dependency towards IVAHD clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
1	RESERVED		R	0
0	MPU_M3_STATDEP	Static dependency towards MPU_A3 clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-1202. Register Call Summary for Register CM_SDMA_STATICDEP

Device Low-Power States • Device Off Mode Wake-Up Sequences: [0]
PRCM Register Manual • CORE_CM2 Register Summary: [1] • RESTORE_CM2 Register Description: [2]

Table 3-1203. CM_SDMA_DYNAMICDEP

Address Offset	0x0000 0308		
Physical Address	0x4A00 8A08	**Instance**	CORE_CM2
Description	This register controls the dynamic domain depedencies from SDMA domain towards 'target' domains. It is relevant only for domain having INTRCONN master port(s).		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																									L3_2_DYNDEP	RESERVED					

Bits	Field Name	Description	Type	Reset
31:7	RESERVED		R	0x0000000
6	L3_2_DYNDEP	Dynamic dependency towards L3_2 clock domain Read 0x0: Dependency is disabled	R	0
5:0	RESERVED		R	0x00

Table 3-1204. Register Call Summary for Register CM_SDMA_DYNAMICDEP

PRCM Register Manual • CORE_CM2 Register Summary: [0]

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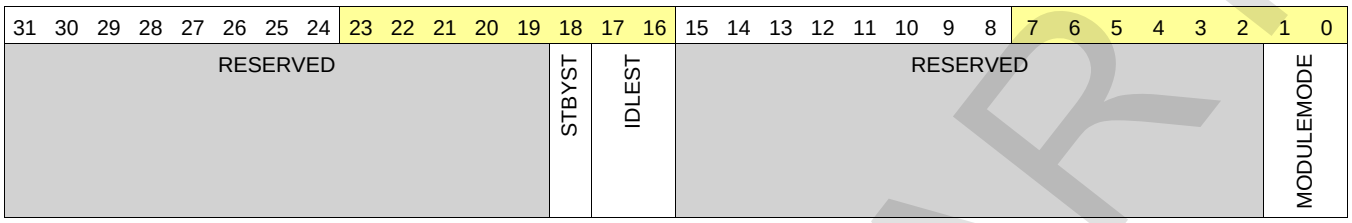
Table 3-1205. CM_SDMA_SDMA_CLKCTRL

Address Offset	0x0000 0320		
Physical Address	0x4A00 8A20	**Instance**	CORE_CM2
Description	This register manages the SDMA clocks.		
Type	R		



Bits	Field Name	Description	Type	Reset
31:19	RESERVED		R	0x0000
18	STBYST	Module standby status. [warm reset insensitive] Read 0x0: Module is functional (not in standby) Read 0x1: Module is in standby	R	1
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. Read 0x1: Module is managed automatically by hardware according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CLKTRCTRL=3, any INTRCONN access to module is always granted. Module clocks may be gated according to the clock domain state.	R Rreturns	0x1

Table 3-1206. Register Call Summary for Register CM_SDMA_SDMA_CLKCTRL

Clock Management Functional Description
- Clock Domain Module Attributes: [0] [1] [2]

PRCM Register Manual
- CORE_CM2 Register Summary: [3]

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Table 3-1207. CM_MEMIF_CLKSTCTRL

Address Offset	0x0000 0400		
Physical Address	0x4A00 8B00	**Instance**	CORE_CM2
Description	This register enables the domain power state transition. It controls the hardware supervised domain power state transition between ON-ACTIVE and ON-INACTIVE states. It also holds 1 status bit per clock input of the domain.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																					CLKACTIVITY_PHY_ROOT_CLK	CLKACTIVITY_DLL_CLK	CLKACTIVITY_L3_EMIF_ICLK	RESERVED						CLKTRCTRL	

Bits	Field Name	Description	Type	Reset
31:11	RESERVED		R	0x000000
10	CLKACTIVITY_PHY_ROOT_CLK	This field indicates the state of the PHY_ROOT_CLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
9	CLKACTIVITY_DLL_CLK	This field indicates the state of the DLL_CLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
8	CLKACTIVITY_L3_EMIF_ICLK	This field indicates the state of the L3_EMIF_ICLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
7:2	RESERVED		R	0x00
1:0	CLKTRCTRL	Controls the clock state transition of the MEMIF clock domain. 0x0: NO_SLEEP: Sleep transition cannot be initiated. Wakeup transition may however occur. Read 0x1: Reserved 0x2: SW_WKUP: Start a software forced wake-up transition on the domain. 0x3: HW_AUTO: Automatic transition is enabled. Sleep and wakeup transition are based upon hardware conditions.	RW	0x0

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Table 3-1208. Register Call Summary for Register CM_MEMIF_CLKSTCTRL

Clock Management Functional Description • Clock Domain Modes: [0] [1] [2] [3]
PRCM Register Manual • CORE_CM2 Register Summary: [4] • RESTORE_CM2 Register Description: [5]

Table 3-1209. CM_MEMIF_DMM_CLKCTRL

Address Offset	0x0000 0420		
Physical Address	0x4A00 8B20	**Instance**	CORE_CM2
Description	This register manages the DMM clocks.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED														MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. Read 0x1: Module is managed automatically by hardware according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CLKTRCTRL=3, any INTRCONN access to module is always granted. Module clocks may be gated according to the clock domain state.	R Rreturns	0x1

Table 3-1210. Register Call Summary for Register CM_MEMIF_DMM_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • CORE_CM2 Register Summary: [2]

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Table 3-1211. CM_MEMIF_EMIF_FW_CLKCTRL

Address Offset	0x0000 0428		
Physical Address	0x4A00 8B28	**Instance**	CORE_CM2
Description	This register manages the EMIF_FW clocks.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED														MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. Read 0x1: Module is managed automatically by hardware according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CLKTRCTRL=3, any INTRCONN access to module is always granted. Module clocks may be gated according to the clock domain state.	R Rreturns	0x1

Table 3-1212. Register Call Summary for Register CM_MEMIF_EMIF_FW_CLKCTRL

Clock Management Functional Description
- Clock Domain Module Attributes: [0] [1]

PRCM Register Manual
- CORE_CM2 Register Summary: [2]

Table 3-1213. CM_MEMIF_EMIF_1_CLKCTRL

Address Offset	0x0000 0430		
Physical Address	0x4A00 8B30	**Instance**	CORE_CM2
Description	This register manages the EMIF_1 clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED														MODULEMODE	

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Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is temporarily disabled by software. Interconnect access to module are stalled. Can be used to change timing parameter of EMIF1 module. 0x1: Module is managed automatically by hardware according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CLKTRCTRL=3, any INTRCONN access to module is always granted. Module clocks may be gated according to the clock domain state. Read 0x2: Reserved Read 0x3: Reserved	RW	0x1

Table 3-1214. Register Call Summary for Register CM_MEMIF_EMIF_1_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • CORE_CM2 Register Summary: [2]

Table 3-1215. CM_MEMIF_EMIF_2_CLKCTRL

Address Offset	0x0000 0438		
Physical Address	0x4A00 8B38	**Instance**	CORE_CM2
Description	This register manages the EMIF_2 clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED														MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3

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Bits	Field Name	Description	Type	Reset
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is temporarily disabled by software. Interconnect access to module are stalled. Can be used to change timing parameter of EMIF2 module. 0x1: Module is managed automatically by hardware according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CLKTRCTRL=3, any INTRCONN access to module is always granted. Module clocks may be gated according to the clock domain state. Read 0x2: Reserved Read 0x3: Reserved	RW	0x1

Table 3-1216. Register Call Summary for Register CM_MEMIF_EMIF_2_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • CORE_CM2 Register Summary: [2]

Table 3-1217. CM_MEMIF_DLL_CLKCTRL

Address Offset	0x0000 0440		
Physical Address	0x4A00 8B40	**Instance**	CORE_CM2
Description	This register manages the DLL clock.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							OPTFCLKEN_DLL_CLK	RESERVED							

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	OPTFCLKEN_DLL_CLK	Optional functional clock control. 0x0: Optional functional clock is disabled. DLL_CLK can be gated when MEMIF domain performs sleep transition 0x1: Optional functional clock is enabled. DLL_CLK is garantied to not be gated if already running.	RW	0
7:0	RESERVED		R	0x00

Table 3-1218. Register Call Summary for Register CM_MEMIF_DLL_CLKCTRL

PRCM Register Manual • CORE_CM2 Register Summary: [0]

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Table 3-1219. CM_C2C_CLKSTCTRL

Address Offset	0x0000 0500		
Physical Address	0x4A00 8C00	**Instance**	CORE_CM2
Description	This register enables the domain power state transition. It controls the hardware supervised domain power state transition between ON-ACTIVE and ON-INACTIVE states. It also holds 1 status bit per clock input of the domain.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																					CLKACTIVITY_L3X2_C2C_ICLK	CLKACTIVITY_L4_C2C_ICLK	CLKACTIVITY_L3_C2C_ICLK	RESERVED						CLKTRCTRL	

Bits	Field Name	Description	Type	Reset
31:11	RESERVED		R	0x000000
10	CLKACTIVITY_L3X2_C2C_ICLK	This field indicates the state of the C2C_L3X2_ICLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
9	CLKACTIVITY_L4_C2C_ICLK	This field indicates the state of the L4_C2C_ICLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
8	CLKACTIVITY_L3_C2C_ICLK	This field indicates the state of the L3_C2C_ICLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
7:2	RESERVED		R	0x00
1:0	CLKTRCTRL	Controls the clock state transition of the C2C clock domain. 0x0: NO_SLEEP: Sleep transition cannot be initiated. Wakeup transition may however occur. Read 0x1: Reserved 0x2: SW_WKUP: Start a software forced wake-up transition on the domain. 0x3: HW_AUTO: Automatic transition is enabled. Sleep and wakeup transition are based upon hardware conditions.	RW	0x3

Table 3-1220. Register Call Summary for Register CM_C2C_CLKSTCTRL

Clock Management Functional Description
- Clock Domain Modes: [0] [1] [2] [3]

PRCM Register Manual
- CORE_CM2 Register Summary: [4]

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Table 3-1221. CM_C2C_STATICDEP

Address Offset	0x0000 0504		
Physical Address	0x4A00 8C04	**Instance**	CORE_CM2
Description	This register controls the static domain depedencies from C2C domain towards 'target' domains. It is relevant only for domain having system initiator(s).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																		L4PER_STATDEP	L4CFG_STATDEP	RESERVED				L3INIT_STATDEP	L3_2_STATDEP	L3_1_STATDEP	MEMIF_STATDEP	ABE_STATDEP	IVAHD_STATDEP	RESERVED	

Bits	Field Name	Description	Type	Reset
31:14	RESERVED		R	0x00000
13	L4PER_STATDEP	Static dependency towards L4PER clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
12	L4CFG_STATDEP	Static dependency towards L4CFG clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
11:8	RESERVED		R	0x0
7	L3INIT_STATDEP	Static dependency towards L3INIT clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
6	L3_2_STATDEP	Static dependency towards L3_2 clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
5	L3_1_STATDEP	Static dependency towards L3_1 clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
4	MEMIF_STATDEP	Static dependency towards MEMIF clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	1
3	ABE_STATDEP	Static dependency towards ABE clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
2	IVAHD_STATDEP	Static dependency towards IVAHD clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
1:0	RESERVED		R	0x0

Table 3-1222. Register Call Summary for Register CM_C2C_STATICDEP

Clock Management Functional Description
- Clock Domain Dependency: [0] [1] [2] [3] [4] [5] [6] [7]

PRCM Register Manual
- CORE_CM2 Register Summary: [8]
- RESTORE_CM2 Register Description: [9]

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Table 3-1223. CM_C2C_DYNAMICDEP

Address Offset	0x0000 0508		
Physical Address	0x4A00 8C08	**Instance**	CORE_CM2
Description	This register controls the dynamic domain depedencies from C2C domain towards 'target' domains. It is relevant only for domain having INTRCONN master port(s).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				WINDOWSIZE				RESERVED																	L3_2_DYNDEP	RESERVED	MEMIF_DYNDEP	RESERVED			

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:24	WINDOWSIZE	Size of sliding window used to monitor INTRCONN interface activity for determination of auto-sleep feature. Time unit defined by CM_DYN_DEP_PRESCAL register.	RW	0x4
23:7	RESERVED		R	0x00000
6	L3_2_DYNDEP	Dynamic dependency towards L3_2 clock domain Read 0x1: Dependency is enabled	R Rreturns 1s	1
5	RESERVED		R	0
4	MEMIF_DYNDEP	Dynamic dependency towards MEMIF clock domain Read 0x1: Dependency is enabled	R Rreturns 1s	1
3:0	RESERVED		R	0x0

Table 3-1224. Register Call Summary for Register CM_C2C_DYNAMICDEP

Clock Management Functional Description
- Clock Domain Dependency: [0] [1]

PRCM Register Manual
- CORE_CM2 Register Summary: [2]
- RESTORE_CM2 Register Description: [3]

Table 3-1225. CM_C2C_C2C_CLKCTRL

Address Offset	0x0000 0520		
Physical Address	0x4A00 8C20	**Instance**	CORE_CM2
Description	This register manages the C2C clocks.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													STBYST	IDLEST		RESERVED														MODULEMODE	

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Bits	Field Name	Description	Type	Reset
31:19	RESERVED		R	0x0000
18	STBYST	C2C module standby status. [warm reset insensitive] Read 0x0: Module is functional (not in standby) Read 0x1: Module is in standby	R	1
17:16	IDLEST	C2C interface idle status. [warm reset insensitive] Read 0x0: C2C interface is in functional state Read 0x1: C2C interface is in a transitory state Read 0x2: C2C interface is in IDLE state	R	0x2
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. Read 0x1: Module is managed automatically by hardware according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CLKTRCTRL=3, any INTRCONN access to module is always granted. Module clocks may be gated according to the clock domain state.	R Rreturns	0x1

Table 3-1226. Register Call Summary for Register CM_C2C_C2C_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1] [2]
PRCM Register Manual • CORE_CM2 Register Summary: [3]

Table 3-1227. CM_C2C_C2C_FW_CLKCTRL

Address Offset	0x0000 0530		
Physical Address	0x4A00 8C30	**Instance**	CORE_CM2
Description	This register manages the C2C_FW clocks.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED								MODULEMODE							

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000

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Bits	Field Name	Description	Type	Reset
1:0	MODULEMODE	Control the way mandatory clocks are managed. Read 0x1: Module is managed automatically by hardware according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CLKTRCTRL=3, any INTRCONN access to module is always granted. Module clocks may be gated according to the clock domain state.	R Rreturns	0x1

Table 3-1228. Register Call Summary for Register CM_C2C_C2C_FW_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • CORE_CM2 Register Summary: [2]

Table 3-1229. CM_L4CFG_CLKSTCTRL

Address Offset	0x0000 0600		
Physical Address	0x4A00 8D00	**Instance**	CORE_CM2
Description	This register enables the domain power state transition. It controls the hardware supervised domain power state transition between ON-ACTIVE and ON-INACTIVE states. It also holds 1 status bit per clock input of the domain.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						CLKACTIVITY_CORE_TS_FCLK	CLKACTIVITY_CFG_L4_ICLK	RESERVED						CLKTRCTRL	

Bits	Field Name	Description	Type	Reset
31:10	RESERVED		R	0x000000
9	CLKACTIVITY_CORE_TS_FCLK	This field indicates the state of the CORE_TS_FCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is on-going	R	0
8	CLKACTIVITY_CFG_L4_ICLK	This field indicates the state of the CFG_L4_ICLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is gated. Read 0x1: Corresponding clock is running or gating/ungating; transition is ongoing.	R	0
7:2	RESERVED		R	0x00

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Bits	Field Name	Description	Type	Reset
1:0	CLKTRCTRL	Controls the clock state transition of the L4CFG clock domain. 0x0: NO_SLEEP: Sleep transition cannot be initiated. Wakeup transition may however occur. Read 0x1: Reserved Read 0x2: Reserved 0x3: HW_AUTO: Automatic transition is enabled. Sleep and wakeup transition are based upon hardware conditions.	RW	0x0

Table 3-1230. Register Call Summary for Register CM_L4CFG_CLKSTCTRL

Clock Management Functional Description • Clock Domain Modes: [0] [1]
PRCM Register Manual • CORE_CM2 Register Summary: [2] • RESTORE_CM2 Register Description: [3]

Table 3-1231. CM_L4CFG_DYNAMICDEP

Address Offset	0x0000 0608		
Physical Address	0x4A00 8D08	**Instance**	CORE_CM2
Description	This register controls the dynamic domain depedencies from L4_CFG domain towards 'target' domains. It is relevant only for domain having INTRCONN master port(s).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				WINDOWSIZE				RESERVED				MPU_DYNDEP	C2C_DYNDEP	RESERVED	ALWONCORE_DYNDEP	L4WKUP_DYNDEP	RESERVED			SDMA_DYNDEP	RESERVED	CAM_DYNDEP	DSS_DYNDEP	L3_INIT_DYNDEP	L3_2_DYNDEP	L3_1_DYNDEP	MEMIF_DYNDEP	RESERVED		DSP_DYNDEP	RESERVED

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:24	WINDOWSIZE	Size of sliding window used to monitor INTRCONN interface activity for determination of auto-sleep feature. Time unit defined by CM_DYN_DEP_PRESCAL register.	RW	0x4
23:20	RESERVED		R	0x00
19	MPU_DYNDEP	Dynamic dependency towards MPU clock domain Read 0x1: Dependency is enabled	R Rretunrs 1s	1
18	C2C_DYNDEP	Dynamic dependency towards C2C clock domain Read 0x1: Dependency is enabled	R Rreturns 1s	1
17	RESERVED		R	1
16	ALWONCORE_DYNDEP	Dynamic dependency towards ALWONCORE clock domain Read 0x1: Dependency is enabled	R Rreturns 1s	1
15	L4WKUP_DYNDEP	Dynamic dependency towards L4WKUP clock domain Read 0x1: Dependency is enabled	R Rreturns 1s	1

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Bits	Field Name	Description	Type	Reset
14:12	RESERVED		R	0x0
11	SDMA_DYNDEP	Dynamic dependency towards SDMA clock domain Read 0x1: Dependency is enabled	R Rreturns 1s	1
10	RESERVED		R	0
9	CAM_DYNDEP	Dynamic dependency towards ISS clock domain Read 0x0: Dependency is disabled	R	0
8	DSS_DYNDEP	Dynamic dependency towards DSS clock domain Read 0x1: Dependency is enabled	R Rreturns 1s	1
7	L3_INIT_DYNDEP	Dynamic dependency towards L3INIT clock domain Read 0x1: Dependency is enabled	R Rreturns 1s	1
6	L3_2_DYNDEP	Dynamic dependency towards L3_2 clock domain Read 0x1: Dependency is enabled	R Rreturns 1s	1
5	L3_1_DYNDEP	Dynamic dependency towards L3_1 clock domain Read 0x1: Dependency is enabled	R Rreturns 1s	1
4	MEMIF_DYNDEP	Dynamic dependency towards MEMIF clock domain Read 0x1: Dependency is enabled	R Rreturns 1s	1
3:2	RESERVED		R	0x0
1	DSP_DYNDEP	Dynamic dependency towards DSP clock domain Read 0x1: Dependency is enabled	R Rreturns 1s	1
0	RESERVED		R	0

Table 3-1232. Register Call Summary for Register CM_L4CFG_DYNAMICDEP

Clock Management Functional Description • Clock Domain Dependency: [0] [1] [2] [3] [4] [5] [6] [7] [8]
PRCM Register Manual • CORE_CM2 Register Summary: [9] • RESTORE_CM2 Register Description: [10]

Table 3-1233. CM_L4CFG_L4_CFG_CLKCTRL

Address Offset	0x0000 0620		
Physical Address	0x4A00 8D20	**Instance**	CORE_CM2
Description	This register manages the L4_CFG clocks.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED														MODULEMODE	

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Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. Read 0x1: Module is managed automatically by hardware according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CLKTRCTRL=3, any INTRCONN access to module is always granted. Module clocks may be gated according to the clock domain state.	R Rreturns	0x1

Table 3-1234. Register Call Summary for Register CM_L4CFG_L4_CFG_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • CORE_CM2 Register Summary: [2]

Table 3-1235. CM_L4CFG_SPINLOCK_CLKCTRL

Address Offset	0x0000 0628		
Physical Address	0x4A00 8D28	**Instance**	CORE_CM2
Description	This register manages the HW_SEM clocks.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED														MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000

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Bits	Field Name	Description	Type	Reset
1:0	MODULEMODE	Control the way mandatory clocks are managed. Read 0x1: Module is managed automatically by hardware according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CLKTRCTRL=3, any INTRCONN access to module is always granted. Module clocks may be gated according to the clock domain state.	R Rreturns	0x1

Table 3-1236. Register Call Summary for Register CM_L4CFG_SPINLOCK_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • CORE_CM2 Register Summary: [2]

Table 3-1237. CM_L4CFG_MAILBOX_CLKCTRL

Address Offset	0x0000 0630		
Physical Address	0x4A00 8D30	**Instance**	CORE_CM2
Description	This register manages the MAILBOX clocks.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED														MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. Read 0x1: Module is managed automatically by hardware according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CLKTRCTRL=3, any INTRCONN access to module is always granted. Module clocks may be gated according to the clock domain state.	R Rreturns	0x1

Table 3-1238. Register Call Summary for Register CM_L4CFG_MAILBOX_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • CORE_CM2 Register Summary: [2]

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Table 3-1239. CM_L4CFG_SAR_ROM_CLKCTRL

Address Offset	0x0000 0638		
Physical Address	0x4A00 8D38	**Instance**	CORE_CM2
Description	This register manages the SAR_ROM clocks.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED								MODULEMODE							

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. Read 0x1: Module is managed automatically by hardware according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CLKTRCTRL=3, any INTRCONN access to module is always granted. Module clocks may be gated according to the clock domain state.	R Rreturns	0x1

Table 3-1240. Register Call Summary for Register CM_L4CFG_SAR_ROM_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • CORE_CM2 Register Summary: [2]

Table 3-1241. CM_L3INSTR_CLKSTCTRL

Address Offset	0x0000 0700		
Physical Address	0x4A00 8E00	**Instance**	CORE_CM2
Description	This register enables the domain power state transition. It controls the hardware supervised domain power state transition between ON-ACTIVE and ON-INACTIVE states. It also holds 1 status bit per clock input of the domain.		
Type	R		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							CLKACTIVITY_L3_INSTR_ICLK	RESERVED						CLKTRCTRL	

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	CLKACTIVITY_L3_INSTR_ICLK	This field indicates the state of the L3_INSTR_GICLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
7:2	RESERVED		R	0x00
1:0	CLKTRCTRL	Controls the clock state transition of the L3INSTR clock domain. Read 0x3: HW_AUTO: Automatic transition is enabled. Sleep and wakeup transition are based upon hardware conditions.	R Rreturns 1s	0x3

Table 3-1242. Register Call Summary for Register CM_L3INSTR_CLKSTCTRL

Clock Management Functional Description • Clock Domain Modes: [0] [1]
PRCM Register Manual • CORE_CM2 Register Summary: [2]

Table 3-1243. CM_L3INSTR_L3_3_CLKCTRL

Address Offset	0x0000 0720		
Physical Address	0x4A00 8E20	**Instance**	CORE_CM2
Description	This register manages the L3_3 clocks. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED														MODULEMODE	

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Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by software. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). 0x1: Module is managed automatically by hardware according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CLKTRCTRL=3, any INTRCONN access to module is always granted. Module clocks may be gated according to the clock domain state. Read 0x2: Reserved Read 0x3: Reserved	RW	0x1

Table 3-1244. Register Call Summary for Register CM_L3INSTR_L3_3_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • CORE_CM2 Register Summary: [2] • RESTORE_CM2 Register Description: [3]

Table 3-1245. CM_L3INSTR_L3_INSTR_CLKCTRL

Address Offset	0x0000 0728		
Physical Address	0x4A00 8E28	**Instance**	CORE_CM2
Description	This register manages the L3 INSTRUMENTATION clocks. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED														MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3

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Bits	Field Name	Description	Type	Reset
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by software. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). 0x1: Module is managed automatically by hardware according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CLKTRCTRL=3, any INTRCONN access to module is always granted. Module clocks may be gated according to the clock domain state. Read 0x2: Reserved Read 0x3: Reserved	RW	0x1

Table 3-1246. Register Call Summary for Register CM_L3INSTR_L3_INSTR_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • CORE_CM2 Register Summary: [2] • RESTORE_CM2 Register Description: [3]

Table 3-1247. CM_L3INSTR_OCP_WP1_CLKCTRL

Address Offset	0x0000 0740		
Physical Address	0x4A00 8E40	**Instance**	CORE_CM2
Description	This register manages the OCP_WP1 clocks. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED														MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. Read 0x3: Module is disabled and cannot be accessed Read 0x2: Module is in idle mode (only Interconnect part). It is functional if using separate functional clock Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x0: Module is fully functional, including Interconnect	R	0x3
15:2	RESERVED		R	0x0000

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Bits	Field Name	Description	Type	Reset
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by software. Any Interconnect access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). 0x1: Module is managed automatically by hardware according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CLKTRCTRL=3, any Interconnect access to module is always granted. Module clocks may be gated according to the clock domain state. Read 0x2: Reserved Read 0x3: Reserved	RW	0x1

Table 3-1248. Register Call Summary for Register CM_L3INSTR_OCP_WP1_CLKCTRL

PRCM Register Manual
- CORE_CM2 Register Summary: [0]
- RESTORE_CM2 Register Description: [1]

3.11.34 IVAHD_CM2 Registers

3.11.34.1 IVAHD_CM2 Register Summary

Table 3-1249. IVAHD_CM2 Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	IVAHD_CM2 L4 Base Address
CM_IVAHD_CLKSTCTRL	RW	32	0x0000 0000	0x4A00 8F00
CM_IVAHD_STATICDEP	RW	32	0x0000 0004	0x4A00 8F04
CM_IVAHD_DYNAMICDEP	R	32	0x0000 0008	0x4A00 8F08
CM_IVAHD_IVAHD_CLKCTRL	RW	32	0x0000 0020	0x4A00 8F20
CM_IVAHD_SL2_CLKCTRL	RW	32	0x0000 0028	0x4A00 8F28

3.11.34.2 IVAHD_CM2 Register Description

Table 3-1250. CM_IVAHD_CLKSTCTRL

Address Offset	0x0000 0000		
Physical Address	0x4A00 8F00	**Instance**	IVAHD_CM2
Description	This register enables the IVAHD domain power state transition. It controls the hardware supervised domain power state transition between ON-ACTIVE and ON-INACTIVE states. It also holds 1 status bit per clock input of the domain.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							CLKACTIVITY_IVAHD_CLK	RESERVED						CLKTRCTRL	

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Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	CLKACTIVITY_IVAHD_CLK	This field indicates the state of the IVAHD_CLK clock input of the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
7:2	RESERVED		R	0x00
1:0	CLKTRCTRL	Controls the clock state transition of the IVAHD clock domain. 0x0: NO_SLEEP: Sleep transition cannot be initiated. Wakeup transition may however occur. 0x1: SW_SLEEP: Start a software forced sleep transition on the domain. 0x2: SW_WKUP: Start a software forced wake-up transition on the domain. 0x3: HW_AUTO: Automatic transition is enabled. Sleep and wakeup transition are based upon hardware conditions.	RW	0x3

Table 3-1251. Register Call Summary for Register CM_IVAHD_CLKSTCTRL

Reset Management Functional Description • IVAHD Subsystem Software Warm Reset Sequence: [0]
Clock Management Functional Description • Clock Domain Modes: [1] [2]
PRCM Register Manual • IVAHD_CM2 Register Summary: [3]

Table 3-1252. CM_IVAHD_STATICDEP

Address Offset	0x0000 0004		
Physical Address	0x4A00 8F04	**Instance**	IVAHD_CM2
Description	This register controls the static domain depedencies from IVAHD domain towards 'target' domains. It is relevant only for domain having system initiator(s).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								L3_2_STATDEP	L3_1_STATDEP	MEMIF_STATDEP	RESERVED				

Bits	Field Name	Description	Type	Reset
31:7	RESERVED		R	0x0000000
6	L3_2_STATDEP	Static dependency towards L3_2 clock domain Read 0x1: Dependency is enabled	R Rreturns 1s	1
5	L3_1_STATDEP	Static dependency towards L3_1 clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

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Bits	Field Name	Description	Type	Reset
4	MEMIF_STATDEP	Static dependency towards MEMIF clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
3:0	RESERVED		R	0x0

Table 3-1253. Register Call Summary for Register CM_IVAHD_STATICDEP

Clock Management Functional Description • Clock Domain Dependency: [0] [1] [2]
PRCM Register Manual • IVAHD_CM2 Register Summary: [3]

Table 3-1254. CM_IVAHD_DYNAMICDEP

Address Offset	0x0000 0008		
Physical Address	0x4A00 8F08	**Instance**	IVAHD_CM2
Description	This register controls the dynamic domain depedencies from IVAHD domain towards 'target' domains. It is relevant only for domain having INTRCONN master port(s).		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																									L3_2_DYNDEP	RESERVED					

Bits	Field Name	Description	Type	Reset
31:7	RESERVED		R	0x0000000
6	L3_2_DYNDEP	Dynamic dependency towards L3_2 clock domain Read 0x0: Dependency is disabled	R	0
5:0	RESERVED		R	0x00

Table 3-1255. Register Call Summary for Register CM_IVAHD_DYNAMICDEP

Clock Management Functional Description • Clock Domain Dependency: [0]
PRCM Register Manual • IVAHD_CM2 Register Summary: [1]

Table 3-1256. CM_IVAHD_IVAHD_CLKCTRL

Address Offset	0x0000 0020		
Physical Address	0x4A00 8F20	**Instance**	IVAHD_CM2
Description	This register manages the IVAHD clocks.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													STBYST	IDLEST		RESERVED														MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:19	RESERVED		R	0x0000
18	STBYST	Module standby status. [warm reset insensitive] Read 0x0: Module is functional (not in standby) Read 0x1: Module is in standby	R	1
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by software. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). 0x1: Module is managed automatically by hardware according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CLKTRCTRL=3, any INTRCONN access to module is always granted. Module clocks may be gated according to the clock domain state. Read 0x2: Reserved Read 0x3: Reserved	RW	0x0

Table 3-1257. Register Call Summary for Register CM_IVAHD_IVAHD_CLKCTRL

Reset Management Functional Description • IVAHD Subsystem Software Warm Reset Sequence: [0] [1]
Clock Management Functional Description • Clock Domain Module Attributes: [2] [3] [4]
PRCM Register Manual • IVAHD_CM2 Register Summary: [5]

Table 3-1258. CM_IVAHD_SL2_CLKCTRL

Address Offset	0x0000 0028		
Physical Address	0x4A00 8F28	**Instance**	IVAHD_CM2
Description	This register manages the SL2 clocks.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED														MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by software. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). 0x1: Module is managed automatically by hardware according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CLKTRCTRL=3, any INTRCONN access to module is always granted. Module clocks may be gated according to the clock domain state. Read 0x2: Reserved Read 0x3: Reserved	RW	0x0

Table 3-1259. Register Call Summary for Register CM_IVAHD_SL2_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • IVAHD_CM2 Register Summary: [2]

3.11.35 CAM_CM2 Registers

3.11.35.1 CAM_CM2 Register Summary

Table 3-1260. CAM_CM2 Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	CAM_CM2 L4 Base Address
CM_CAM_CLKSTCTRL	RW	32	0x0000 0000	0x4A00 9000
CM_CAM_STATICDEP	RW	32	0x0000 0004	0x4A00 9004
CM_CAM_DYNAMICDEP	R	32	0x0000 0008	0x4A00 9008
CM_CAM_ISS_CLKCTRL	RW	32	0x0000 0020	0x4A00 9020
CM_CAM_FDIF_CLKCTRL	RW	32	0x0000 0028	0x4A00 9028

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3.11.35.2 CAM_CM2 Register Description

Table 3-1261. CM_CAM_CLKSTCTRL

Address Offset	0x0000 0000		
Physical Address	0x4A00 9000	**Instance**	CAM_CM2
Description	This register enables the domain power state transition. It controls the hardware supervised domain power state transition between ON-ACTIVE and ON-INACTIVE states. It also holds 1 status bit per clock input of the domain.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																					CLKACTIVITY_FDIF_FCLK	CLKACTIVITY_CAM_PHY_CTRL_CLK	CLKACTIVITY_ISS_CLK	RESERVED						CLKTRCTRL	

Bits	Field Name	Description	Type	Reset
31:11	RESERVED		R	0x000000
10	CLKACTIVITY_FDIF_FCLK	This field indicates the state of the FDIF_FCLK clock input of the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
9	CLKACTIVITY_CAM_PHY_CTRL_CLK	This field indicates the state of the CAM_PHY_CTRL_CLK clock input of the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
8	CLKACTIVITY_ISS_CLK	This field indicates the state of the ISS_CLK clock input of the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
7:2	RESERVED		R	0x00
1:0	CLKTRCTRL	Controls the clock state transition of the CAM clock domain. 0x0: NO_SLEEP: Sleep transition cannot be initiated. Wakeup transition may however occur. 0x1: SW_SLEEP: Start a software forced sleep transition on the domain. 0x2: SW_WKUP: Start a software forced wake-up transition on the domain. 0x3: HW_AUTO: Automatic transition is enabled. Sleep and wakeup transition are based upon hardware conditions.	RW	0x3

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Table 3-1262. Register Call Summary for Register CM_CAM_CLKSTCTRL

Clock Management Functional Description • Clock Domain Modes: [0] [1] [2] [3]
PRCM Register Manual • CAM_CM2 Register Summary: [4]

Table 3-1263. CM_CAM_STATICDEP

Address Offset	0x0000 0004		
Physical Address	0x4A00 9004	**Instance**	CAM_CM2
Description	This register controls the static domain depedencies from CAM domain towards 'target' domains. It is relevant only for domain having system initiator(s).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								L3_2_STATDEP	L3_1_STATDEP	MEMIF_STATDEP	RESERVED	IVAHD_STATDEP	RESERVED		

Bits	Field Name	Description	Type	Reset
31:7	RESERVED		R	0x0000000
6	L3_2_STATDEP	Static dependency towards L3_2 clock domain Read 0x1: Dependency is enabled	R Rreturns 1s	1
5	L3_1_STATDEP	Static dependency towards L3_1 clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
4	MEMIF_STATDEP	Static dependency towards MEMIF clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
3	RESERVED		R	0
2	IVAHD_STATDEP	Static dependency towards IVAHD clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
1:0	RESERVED		R	0x0

Table 3-1264. Register Call Summary for Register CM_CAM_STATICDEP

Clock Management Functional Description • Clock Domain Dependency: [0] [1] [2] [3]
PRCM Register Manual • CAM_CM2 Register Summary: [4]

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Table 3-1265. CM_CAM_DYNAMICDEP

Address Offset	0x0000 0008		
Physical Address	0x4A00 9008	**Instance**	CAM_CM2
Description	This register controls the dynamic domain depedencies from CAM domain towards 'target' domains. It is relevant only for domain having INTRCONN master port(s).		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																									L3_2_DYNDEP	RESERVED					

Bits	Field Name	Description	Type	Reset
31:7	RESERVED		R	0x0000000
6	L3_2_DYNDEP	Dynamic dependency towards L3_2 clock domain Read 0x0: Dependency is disabled	R	0
5:0	RESERVED		R	0x00

Table 3-1266. Register Call Summary for Register CM_CAM_DYNAMICDEP

Clock Management Functional Description
- Clock Domain Dependency: [0]

PRCM Register Manual
- CAM_CM2 Register Summary: [1]

Table 3-1267. CM_CAM_ISS_CLKCTRL

Address Offset	0x0000 0020		
Physical Address	0x4A00 9020	**Instance**	CAM_CM2
Description	This register manages the ISS clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													STBYST	IDLEST		RESERVED							OPTFCLKEN_CTRLCLK	RESERVED							MODULEMODE

Bits	Field Name	Description	Type	Reset
31:19	RESERVED		R	0x0000
18	STBYST	Module standby status. [warm reset insensitive] Read 0x0: Module is functional (not in standby) Read 0x1: Module is in standby	R	1

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Bits	Field Name	Description	Type	Reset
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:9	RESERVED		R	0x00
8	OPTFCLKEN_CTRLCLK	Optional functional clock control for CAM_PHY_CTRL_GCLK 96Mhz clock. 0x0: Optional functional clock is disabled 0x1: Optional functional clock is enabled	RW	0
7:2	RESERVED		R	0x00
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by software. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen. Read 0x3: Reserved	RW	0x0

Table 3-1268. Register Call Summary for Register CM_CAM_ISS_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1] [2]
PRCM Register Manual • CAM_CM2 Register Summary: [3]

Table 3-1269. CM_CAM_FDIF_CLKCTRL

Address Offset	0x0000 0028		
Physical Address	0x4A00 9028	**Instance**	CAM_CM2
Description	This register manages the FDIF clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						CLKSEL_FCLK		RESERVED					STBYST	IDLEST		RESERVED														MODULEMODE	

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Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x00
25:24	CLKSEL_FCLK	Select the ration of FDIF_FCLK to FUNC_128M_CLK 0x0: FDIF_FCLK is divide by 1 of FUNC_128_CLK, to be used for OPP100 0x1: FDIF_FCLK is divide by 2 of FUNC_128_CLK, to be used for OPP50 0x2: FDIF_FCLK is divide by 4 of FUNC_128_CLK 0x3: Reserved	RW	0x0
23:19	RESERVED		R	0x00
18	STBYST	Module standby status. [warm reset insensitive] Read 0x0: Module is functional (not in standby) Read 0x1: Module is in standby	R	1
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by software. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen. Read 0x3: Reserved	RW	0x0

Table 3-1270. Register Call Summary for Register CM_CAM_FDIF_CLKCTRL

Clock Management Functional Description • CM Clock Source: [0] • Clock Domain Module Attributes: [1] [2] [3]
PRCM Register Manual • CAM_CM2 Register Summary: [4]

3.11.36 DSS_CM2 Registers

3.11.36.1 DSS_CM2 Register Summary

Table 3-1271. DSS_CM2 Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	DSS_CM2 L4 Base Address
CM_DSS_CLKSTCTRL	RW	32	0x0000 0000	0x4A00 9100
CM_DSS_STATICDEP	RW	32	0x0000 0004	0x4A00 9104
CM_DSS_DYNAMICDEP	R	32	0x0000 0008	0x4A00 9108
CM_DSS_DSS_CLKCTRL	RW	32	0x0000 0020	0x4A00 9120
RESERVED	RW	32	0x0000 0028	0x4A00 9128

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3.11.36.2 DSS_CM2 Register Description

Table 3-1272. CM_DSS_CLKSTCTRL

Address Offset	0x0000 0000		
Physical Address	0x4A00 9100	**Instance**	DSS_CM2
Description	This register enables the DSS domain power state transition. It controls the hardware supervised domain power state transition between ON-ACTIVE and ON-INACTIVE states. It also holds 1 status bit per clock input of the domain.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				CLKACTIVITY_HDMI_PHY_48M_FCLK	CLKACTIVITY_DSS_ALWON_SYS_CLK	CLKACTIVITY_DSS_FCLK	CLKACTIVITY_DSS_L3_ICLK	RESERVED						CLKTRCTRL	

Bits	Field Name	Description	Type	Reset
31:12	RESERVED		R	0x00000
11	CLKACTIVITY_HDMI_PHY_48M_FCLK	This field indicates the state of the HDMI_PHY_48MHz_FCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
10	CLKACTIVITY_DSS_ALWON_SYS_CLK	This field indicates the state of the DSS_ALWON_SYS_CLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
9	CLKACTIVITY_DSS_FCLK	This field indicates the state of the DSS_FCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
8	CLKACTIVITY_DSS_L3_ICLK	This field indicates the state of the DSS_L3_ICLK (and DSS_L4_ICLK) clock in the domain. [warm reset insensitive](1) Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
7:2	RESERVED		R	0x00

(1) The video DAC (VDAC) function is not supported.

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Bits	Field Name	Description	Type	Reset
1:0	CLKTRCTRL	Controls the clock state transition of the DSS clock domain. 0x0: NO_SLEEP: Sleep transition cannot be initiated. Wakeup transition may however occur. 0x1: SW_SLEEP: Start a software forced sleep transition on the domain. 0x2: SW_WKUP: Start a software forced wake-up transition on the domain. 0x3: HW_AUTO: Automatic transition is enabled. Sleep and wakeup transition are based upon hardware conditions.	RW	0x3

Table 3-1273. Register Call Summary for Register CM_DSS_CLKSTCTRL

Clock Management Functional Description • Clock Domain Modes: [0] [1] [2] [3] [4]
PRCM Register Manual • DSS_CM2 Register Summary: [5]

Table 3-1274. CM_DSS_STATICDEP

Address Offset	0x0000 0004		
Physical Address	0x4A00 9104	**Instance**	DSS_CM2
Description	This register controls the static domain depedencies from DSS domain towards 'target' domains. It is relevant only for domain having system initiator(s).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								L3_2_STATDEP	L3_1_STATDEP	MEMIF_STATDEP	RESERVED	IVAHD_STATDEP	RESERVED		

Bits	Field Name	Description	Type	Reset
31:7	RESERVED		R	0x0000000
6	L3_2_STATDEP	Static dependency towards L3_2 clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
5	L3_1_STATDEP	Static dependency towards L3_1 clock domain Read 0x1: Dependency is enabled	R Rreturns 1s	1
4	MEMIF_STATDEP	Static dependency towards MEMIF clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
3	RESERVED		R	0
2	IVAHD_STATDEP	Static dependency towards IVAHD clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
1:0	RESERVED		R	0x0

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Table 3-1275. Register Call Summary for Register CM_DSS_STATICDEP

Clock Management Functional Description • Clock Domain Dependency: [0] [1] [2] [3]
PRCM Register Manual • DSS_CM2 Register Summary: [4]

Table 3-1276. CM_DSS_DYNAMICDEP

Address Offset	0x0000 0008		
Physical Address	0x4A00 9108	**Instance**	DSS_CM2
Description	This register controls the dynamic domain depedencies from DSS domain towards 'target' domains. It is relevant only for domain having INTRCONN master port(s).		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																										L3_1_DYNDEP	RESERVED				

Bits	Field Name	Description	Type	Reset
31:6	RESERVED		R	0x0000000
5	L3_1_DYNDEP	Dynamic dependency towards L3_1 domain Read 0x0: Dependency is disabled	R	0
4:0	RESERVED		R	0x00

Table 3-1277. Register Call Summary for Register CM_DSS_DYNAMICDEP

Clock Management Functional Description • Clock Domain Dependency: [0]
PRCM Register Manual • DSS_CM2 Register Summary: [1]

Table 3-1278. CM_DSS_DSS_CLKCTRL

Address Offset	0x0000 0020		
Physical Address	0x4A00 9120	**Instance**	DSS_CM2
Description	This register manages the DSS clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													STBYST	IDLEST		RESERVED				OPTFCLKEN_TV_FCLK	OPTFCLKEN_SYS_CLK	OPTFCLKEN_48MHZ_CLK	OPTFCLKEN_DSSCLK	RESERVED							MODULEMODE	

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Bits	Field Name	Description	Type	Reset
31:19	RESERVED		R	0x0000
18	STBYST	Module standby status. [warm reset insensitive] Read 0x0: Module is functional (not in standby) Read 0x1: Module is in standby	R	1
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:12	RESERVED		R	0x0
11	OPTFCLKEN_TV_FCLK	Optional functional clock control. 0x0: Optional functional clock is disabled 0x1: Optional functional clock is enabled	RW	0
10	OPTFCLKEN_SYS_CLK	Optional functional clock control. 0x0: Optional functional clock is disabled 0x1: Optional functional clock is enabled	RW	0
9	OPTFCLKEN_48MHZ_CLK	Optional functional clock control. 0x0: Optional functional clock is disabled 0x1: Optional functional clock is enabled	RW	0
8	OPTFCLKEN_DSSCLK	Optional functional clock control. 0x0: Optional functional clock is disabled 0x1: Optional functional clock is enabled	RW	0
7:2	RESERVED		R	0x00
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by software. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen. Read 0x3: Reserved	RW	0x0

Table 3-1279. Register Call Summary for Register CM_DSS_DSS_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1] [2] [3]
PRCM Register Manual • DSS_CM2 Register Summary: [4]

3.11.37 SGX_CM2 Registers

3.11.37.1 SGX_CM2 Register Summary

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Table 3-1280. SGX_CM2 Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	SGX_CM2 L4 Base Address
CM_SGX_CLKSTCTRL	RW	32	0x0000 0000	0x4A00 9200
CM_SGX_STATICDEP	RW	32	0x0000 0004	0x4A00 9204
CM_SGX_DYNAMICDEP	R	32	0x0000 0008	0x4A00 9208
CM_SGX_SGX_CLKCTRL	RW	32	0x0000 0020	0x4A00 9220

3.11.37.2 SGX_CM2 Register Description

Table 3-1281. CM_SGX_CLKSTCTRL

Address Offset	0x0000 0000		
Physical Address	0x4A00 9200	**Instance**	SGX_CM2
Description	This register enables the SGX domain power state transition. It controls the hardware supervised domain power state transition between ON-ACTIVE and ON-INACTIVE states. It also holds 1 status bit per clock input of the domain.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						CLKACTIVITY_SGX_FCLK	CLKACTIVITY_SGX_L3_ICLK	RESERVED						CLKTRCTRL	

Bits	Field Name	Description	Type	Reset
31:10	RESERVED		R	0x000000
9	CLKACTIVITY_SGX_FCLK	This field indicates the state of the SGX_FCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
8	CLKACTIVITY_SGX_L3_ICLK	This field indicates the state of the SGX_L3_ICLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
7:2	RESERVED		R	0x00
1:0	CLKTRCTRL	Controls the clock state transition of the SGX clock domain. 0x0: NO_SLEEP: Sleep transition cannot be initiated. Wakeup transition may however occur. 0x1: SW_SLEEP: Start a software forced sleep transition on the domain. 0x2: SW_WKUP: Start a software forced wake-up transition on the domain. 0x3: HW_AUTO: Automatic transition is enabled. Sleep and wakeup transition are based upon hardware conditions.	RW	0x3

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Table 3-1282. Register Call Summary for Register CM_SGX_CLKSTCTRL

Clock Management Functional Description • Clock Domain Modes: [0] [1] [2]
PRCM Register Manual • SGX_CM2 Register Summary: [3]

Table 3-1283. CM_SGX_STATICDEP

Address Offset	0x0000 0004		
Physical Address	0x4A00 9204	**Instance**	SGX_CM2
Description	This register controls the static domain depedencies from SGX domain towards 'target' domains. It is relevant only for domain having system initiator(s).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								L3_2_STATDEP	L3_1_STATDEP	MEMIF_STATDEP	RESERVED	IVAHD_STATDEP	RESERVED		

Bits	Field Name	Description	Type	Reset
31:7	RESERVED		R	0x0000000
6	L3_2_STATDEP	Static dependency towards L3_2 clock domain Read 0x1: Dependency is enabled	R Rreturns 1s	1
5	L3_1_STATDEP	Static dependency towards L3_1 clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
4	MEMIF_STATDEP	Static dependency towards MEMIF clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
3	RESERVED		R	0
2	IVAHD_STATDEP	Static dependency towards IVAHD clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
1:0	RESERVED		R	0x0

Table 3-1284. Register Call Summary for Register CM_SGX_STATICDEP

Clock Management Functional Description • Clock Domain Dependency: [0] [1] [2] [3]
PRCM Register Manual • SGX_CM2 Register Summary: [4]

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Table 3-1285. CM_SGX_DYNAMICDEP

Address Offset	0x0000 0008		
Physical Address	0x4A00 9208	**Instance**	SGX_CM2
Description	This register controls the dynamic domain depedencies from SGX domain towards 'target' domains. It is relevant only for domain having INTRCONN master port(s).		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																									L3_2_DYNDEP	RESERVED					

Bits	Field Name	Description	Type	Reset
31:7	RESERVED		R	0x0000000
6	L3_2_DYNDEP	Dynamic dependency towards L3_2 clock domain Read 0x0: Dependency is disabled	R	0
5:0	RESERVED		R	0x00

Table 3-1286. Register Call Summary for Register CM_SGX_DYNAMICDEP

Clock Management Functional Description
- Clock Domain Dependency: [0]

PRCM Register Manual
- SGX_CM2 Register Summary: [1]

Table 3-1287. CM_SGX_SGX_CLKCTRL

Address Offset	0x0000 0020		
Physical Address	0x4A00 9220	**Instance**	SGX_CM2
Description	This register manages the SGX clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							CLKSEL_SGX_FCLK	RESERVED					STBYST	IDLEST		RESERVED															MODULEMODE		

Bits	Field Name	Description	Type	Reset
31:25	RESERVED		R	0x00
24	CLKSEL_SGX_FCLK	Select the source of SGX_FCLK 0x0: Functional clock is sourced from DPLL_CORE HSDIVIDER 0x1: Functional clock is sourced from DPLL_PER HSDIVIDER	RW	0
23:19	RESERVED		R	0x00

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Bits	Field Name	Description	Type	Reset
18	STBYST	Module standby status. [warm reset insensitive] Read 0x0: Module is functional (not in standby) Read 0x1: Module is in standby	R	1
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by software. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen. Read 0x3: Reserved	RW	0x0

Table 3-1288. Register Call Summary for Register CM_SGX_SGX_CLKCTRL

Clock Management Functional Description • CM Clock Source: [0] • Clock Domain Module Attributes: [1] [2] [3]
PRCM Register Manual • SGX_CM2 Register Summary: [4]

3.11.38 L3INIT_CM2 Registers

3.11.38.1 L3INIT_CM2 Register Summary

Table 3-1289. L3INIT_CM2 Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	L3INIT_CM2 L4 Base Address
CM_L3INIT_CLKSTCTRL	RW	32	0x0000 0000	0x4A00 9300
CM_L3INIT_STATICDEP	RW	32	0x0000 0004	0x4A00 9304
CM_L3INIT_DYNAMICDEP	R	32	0x0000 0008	0x4A00 9308
CM_L3INIT_HSMMC1_CLKCTRL	RW	32	0x0000 0028	0x4A00 9328
CM_L3INIT_HSMMC2_CLKCTRL	RW	32	0x0000 0030	0x4A00 9330
CM_L3INIT_HSI_CLKCTRL	RW	32	0x0000 0038	0x4A00 9338
RESERVED	RW	32	0x0000 0040	0x4A00 9340
CM_L3INIT_HSUSBHOST_CLKCTRL	RW	32	0x0000 0058	0x4A00 9358
CM_L3INIT_HSUSBOTG_CLKCTRL	RW	32	0x0000 0060	0x4A00 9360
CM_L3INIT_HSUSBTLL_CLKCTRL	RW	32	0x0000 0068	0x4A00 9368
RESERVED	R	32	0x0000 0078	0x4A00 9378
RESERVED	RW	32	0x0000 0080	0x4A00 9380
RESERVED	RW	32	0x0000 0088	0x4A00 9388
RESERVED	RW	32	0x0000 0090	0x4A00 9390

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Table 3-1289. L3INIT_CM2 Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	L3INIT_CM2 L4 Base Address
RESERVED	RW	32	0x0000 0098	0x4A00 9398
RESERVED	RW	32	0x0000 00A8	0x4A00 93A8
RESERVED	RW	32	0x0000 00C0	0x4A00 93C0
RESERVED	RW	32	0x0000 00C8	0x4A00 93C8
CM_L3INIT_FSUSB_CLKCTRL	RW	32	0x0000 00D0	0x4A00 93D0
CM_L3INIT_USBPHY_CLKCTRL	RW	32	0x0000 00E0	0x4A00 93E0

3.11.38.2 L3INIT_CM2 Register Description

Table 3-1290. CM_L3INIT_CLKSTCTRL

Address Offset	0x0000 0000		
Physical Address	0x4A00 9300	**Instance**	L3INIT_CM2
Description	This register enables the domain power state transition. It controls the hardware supervised domain power state transition between ON-ACTIVE and ON-INACTIVE states. It also holds 1 status bit per clock input of the domain.		
Type	RW		

31 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11 10	9	8	7 6 5 4 3 2	1	0
RESERVED	CLKACTIVITY_INIT_60M_P2_FCLK	CLKACTIVITY_INIT_60M_P1_FCLK	CLKACTIVITY_HSIC_P2_FCLK	CLKACTIVITY_HSIC_P1_FCLK	CLKACTIVITY_UTMI_ROOT_FCLK	RESERVED	CLKACTIVITY_TLL_CH1_FCLK	CLKACTIVITY_TLL_CH0_FCLK	CLKACTIVITY_HSIC_P2_480M_FCLK	CLKACTIVITY_HSIC_P1_480M_FCLK	RESERVED	CLKACTIVITY_INIT_HSMMC2_FCLK	CLKACTIVITY_INIT_HSMMC1_FCLK	CLKACTIVITY_INIT_HSI_FCLK	CLKACTIVITY_USB_DPLL_HS_CLK	CLKACTIVITY_USB_DPLL_CLK	CLKACTIVITY_INIT_48MC_FCLK	CLKACTIVITY_INIT_48M_FCLK	RESERVED	CLKACTIVITY_INIT_L4_ICLK	CLKACTIVITY_INIT_L3_ICLK	RESERVED	CLKTRCTRL

Bits	Field Name	Description	Type	Reset
31:30	RESERVED		R	0x0
29	CLKACTIVITY_INIT_60M_P2_FCLK	This field indicates the state of the INIT_60M_P2_FCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
28	CLKACTIVITY_INIT_60M_P1_FCLK	This field indicates the state of the INIT_60M_P1_FCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
27	CLKACTIVITY_HSIC_P2_FCLK	This field indicates the state of the HSIC_P2_FCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0

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Bits	Field Name	Description	Type	Reset
26	CLKACTIVITY_HSIC_P1_FCLK	This field indicates the state of the HSIC_P1_FCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
25	CLKACTIVITY_UTMI_ROOT_FCLK	This field indicates the state of the UTMI_ROOT_FCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
24	RESERVED		R	0
23	CLKACTIVITY_TLL_CH1_FCLK	This field indicates the state of the TLL_CH1_FCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
22	CLKACTIVITY_TLL_CH0_FCLK	This field indicates the state of the TLL_CH0_FCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
21	CLKACTIVITY_HSIC_P2_480M_FCLK	This field indicates the state of the HSIC_P2_480M_FCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
20	CLKACTIVITY_HSIC_P1_480M_FCLK	This field indicates the state of the HSIC_P1_480M_FCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
19	RESERVED	Reserved	R	0
18	CLKACTIVITY_INIT_HSMMC2_FCLK	This field indicates the state of the INIT_HSMMC2_FCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
17	CLKACTIVITY_INIT_HSMMC1_FCLK	This field indicates the state of the INIT_HSMMC1_FCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
16	CLKACTIVITY_INIT_HSI_FCLK	This field indicates the state of the INIT_HSI_FCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
15	CLKACTIVITY_USB_DPLL_HS_CLK	This field indicates the state of the USB_DPLL_HS_CLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0

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Bits	Field Name	Description	Type	Reset
14	CLKACTIVITY_USB_DPLL_CLK	This field indicates the state of the USB_DPLL_CLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
13	CLKACTIVITY_INIT_48MC_FCLK	This field indicates the state of the INIT_48MC_FCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
12	CLKACTIVITY_INIT_48M_FCLK	This field indicates the state of the INIT_48M_FCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
11:10	RESERVED	Reserved	R	0x0
9	CLKACTIVITY_INIT_L4_ICLK	This field indicates the state of the L4_INIT_ICLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
8	CLKACTIVITY_INIT_L3_ICLK	This field indicates the state of the L3_INIT_ICLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
7:2	RESERVED	Reserved	R	0x00
1:0	CLKTRCTRL	Controls the clock state transition of the L3INIT clock domain. 0x0: NO_SLEEP: Sleep transition cannot be initiated. Wakeup transition may however occur. 0x1: SW_SLEEP: Start a software forced sleep transition on the domain. 0x2: SW_WKUP: Start a software forced wake-up transition on the domain. 0x3: HW_AUTO: Automatic transition is enabled. Sleep and wakeup transition are based upon hardware conditions.	RW	0x0

Table 3-1291. Register Call Summary for Register CM_L3INIT_CLKSTCTRL

Clock Management Functional Description • Clock Domain Modes: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16]
PRCM Register Manual • L3INIT_CM2 Register Summary: [17] • RESTORE_CM2 Register Description: [18]

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Table 3-1292. CM_L3INIT_STATICDEP

Address Offset	0x0000 0004		
Physical Address	0x4A00 9304	**Instance**	L3INIT_CM2
Description	This register controls the static domain depedencies from L3INIT domain towards 'target' domains. It is relevant only for domain having system initiator(s).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																L4WKUP_STATDEP	RESERVED	L4PER_STATDEP	L4CFG_STATDEP	RESERVED				L3_2_STATDEP	L3_1_STATDEP	MEMIF_STATDEP	ABE_STATDEP	IVAHD_STATDEP	RESERVED		

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15	L4WKUP_STATDEP	Static dependency towards L4WKUP clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
14	RESERVED		R	0
13	L4PER_STATDEP	Static dependency towards L4PER clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
12	L4CFG_STATDEP	Static dependency towards L4CFG clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
11:7	RESERVED		R	0x00
6	L3_2_STATDEP	Static dependency towards L3_2 clock domain Read 0x1: Dependency is enabled	R Rreturns 1s	1
5	L3_1_STATDEP	Static dependency towards L3_1 clock domain Read 0x1: Dependency is enabled	R Rreturns 1s	1
4	MEMIF_STATDEP	Static dependency towards MEMIF clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
3	ABE_STATDEP	Static dependency towards ABE clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
2	IVAHD_STATDEP	Static dependency towards IVAHD clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
1:0	RESERVED		R	0x0

Table 3-1293. Register Call Summary for Register CM_L3INIT_STATICDEP

Clock Management Functional Description
- Clock Domain Dependency: [0] [1] [2] [3] [4] [5] [6]

PRCM Register Manual
- L3INIT_CM2 Register Summary: [7]

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Table 3-1294. CM_L3INIT_DYNAMICDEP

Address Offset	0x0000 0008		
Physical Address	0x4A00 9308	**Instance**	L3INIT_CM2
Description	This register controls the dynamic domain depedencies from L3INIT domain towards 'target' domains. It is relevant only for domain having INTRCONN master port(s).		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																									L3_2_DYNDEP	L3_1_DYNDEP	RESERVED					

Bits	Field Name	Description	Type	Reset
31:7	RESERVED		R	0x0000000
6	L3_2_DYNDEP	Dynamic dependency towards L3_2 clock domain Read 0x0: Dependency is disabled	R	0
5	L3_1_DYNDEP	Dynamic dependency towards L3_1 clock domain Read 0x0: Dependency is disabled	R	0
4:0	RESERVED		R	0x00

Table 3-1295. Register Call Summary for Register CM_L3INIT_DYNAMICDEP

Clock Management Functional Description
- Clock Domain Dependency: [0] [1]

PRCM Register Manual
- L3INIT_CM2 Register Summary: [2]

Table 3-1296. CM_L3INIT_HSMMC1_CLKCTRL

Address Offset	0x0000 0028		
Physical Address	0x4A00 9328	**Instance**	L3INIT_CM2
Description	This register manages the MMC1 clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							CLKSEL	RESERVED					STBYST	IDLEST		RESERVED															MODULEMODE

Bits	Field Name	Description	Type	Reset
31:25	RESERVED		R	0x00
24	CLKSEL	Selects the source of the functional clock. 0x0: 64MHz clock derived from DPLL_PER is selected 0x1: 96MHz clock derived from DPLL_PER is selected	RW	0
23:19	RESERVED		R	0x00

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Bits	Field Name	Description	Type	Reset
18	STBYST	Module standby status. [warm reset insensitive] Read 0x0: Module is functional (not in standby) Read 0x1: Module is in standby	R	1
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED	Reserved	R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by software. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen. Read 0x3: Reserved	RW	0x0

Table 3-1297. Register Call Summary for Register CM_L3INIT_HSMMC1_CLKCTRL

Clock Management Functional Description • CM Clock Source: [0] • Clock Domain Module Attributes: [1] [2] [3]
PRCM Register Manual • L3INIT_CM2 Register Summary: [4]

Table 3-1298. CM_L3INIT_HSMMC2_CLKCTRL

Address Offset	0x0000 0030		
Physical Address	0x4A00 9330	**Instance**	L3INIT_CM2
Description	This register manages the MMC2 clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							CLKSEL	RESERVED					STBYST	IDLEST		RESERVED														MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:25	RESERVED		R	0x00
24	CLKSEL	Selects the source of the functional clock. 0x0: 64MHz clock derived from DPLL_PER is selected 0x1: 96MHz clock derived from DPLL_PER is selected	RW	0
23:19	RESERVED		R	0x00

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Bits	Field Name	Description	Type	Reset
18	STBYST	Module standby status. [warm reset insensitive] Read 0x0: Module is functional (not in standby) Read 0x1: Module is in standby	R	1
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED	Reserved	R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by software. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen. Read 0x3: Reserved	RW	0x0

Table 3-1299. Register Call Summary for Register CM_L3INIT_HSMMC2_CLKCTRL

Clock Management Functional Description • CM Clock Source: [0] • Clock Domain Module Attributes: [1] [2] [3]
PRCM Register Manual • L3INIT_CM2 Register Summary: [4]

Table 3-1300. CM_L3INIT_HSI_CLKCTRL

Address Offset	0x0000 0038		
Physical Address	0x4A00 9338	**Instance**	L3INIT_CM2
Description	This register manages the HSI clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							CLKSEL	RESERVED					STBYST	IDLEST		RESERVED														MODULEMODE	

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Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x00
25:24	CLKSEL	Selects the functional clock source. 0x0: HSI_FCLK is divide by 1 of 192-MHz clock, to be used for OPP100 0x1: HSI_FCLK is divide by 2 of 192-MHz clock, to be used for OPP50 0x2: HSI_FCLK is divide by 4 of 192-MHz clock 0x3: Reserved	RW	0x0
23:19	RESERVED		R	0x00
18	STBYST	Module standby status. [warm reset insensitive] Read 0x0: Module is functional (not in standby) Read 0x1: Module is in standby	R	1
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED	Reserved	R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by software. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). 0x1: Module is managed automatically by hardware according to clock domain Read 0x: Reserved Read 0x3: Reserved	RW	0x0

Table 3-1301. Register Call Summary for Register CM_L3INIT_HSI_CLKCTRL

Clock Management Functional Description • CM Clock Source: [0] • Clock Domain Module Attributes: [1] [2] [3]
PRCM Register Manual • L3INIT_CM2 Register Summary: [4]

Table 3-1302. CM_L3INIT_HSUSBHOST_CLKCTRL

Address Offset	0x0000 0058		
Physical Address	0x4A00 9358	**Instance**	L3INIT_CM2
Description	This register manages the USB_HOST_HS clocks.		
Type	RW		

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31 30 29 28 27 26	25	24	23 22 21 20 19	18	17 16	15	14	13	12	11	10	9	8	7 6 5	4	3 2	1 0
RESERVED	CLKSEL_UTMI_P2	CLKSEL_UTMI_P1	RESERVED	STBYST	IDLEST	OPTFCLKEN_FUNC48MCLK	OPTFCLKEN_HSIC480M_P2_CLK	OPTFCLKEN_HSIC480M_P1_CLK	OPTFCLKEN_HSIC60M_P2_CLK	OPTFCLKEN_HSIC60M_P1_CLK	OPTFCLKEN_UTMI_P3_CLK	OPTFCLKEN_UTMI_P2_CLK	OPTFCLKEN_UTMI_P1_CLK	RESERVED	SAR_MODE	RESERVED	MODULEMODE

Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x00
25	CLKSEL_UTMI_P2	Selects the source of the functional clock for UTMI Port2 on USB Host 0x0: The functional clock is provided by the internal clock source 0x1: The functional clock is provided by an external PHY through an I/O pad.	RW	0
24	CLKSEL_UTMI_P1	Selects the source of the functional clock for UTMI Por1 on USB Host 0x0: The functional clock is provided by the internal clock source 0x1: The functional clock is provided by an external PHY through an I/O pad.	RW	0
23:19	RESERVED		R	0x00
18	STBYST	Module standby status. [warm reset insensitive] Read 0x0: Module is functional (not in standby) Read 0x1: Module is in standby	R	1
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15	OPTFCLKEN_FUNC48MCLK	USB-HOST optional clock control: FUNC48MCLK 0x0: Optional functional clock is disabled 0x1: Optional functional clock is enabled	RW	0
14	OPTFCLKEN_HSIC480M_P2_CLK	USB-HOST optional clock control: HSIC480M_P2_CLK 0x0: Optional functional clock is disabled 0x1: Optional functional clock is enabled	RW	0
13	OPTFCLKEN_HSIC480M_P1_CLK	USB-HOST optional clock control: HSIC480M_P1_CLK 0x0: Optional functional clock is disabled 0x1: Optional functional clock is enabled	RW	0
12	OPTFCLKEN_HSIC60M_P2_CLK	USB-HOST optional clock control: HSIC60M_P2_CLK 0x0: Optional functional clock is disabled 0x1: Optional functional clock is enabled	RW	0
11	OPTFCLKEN_HSIC60M_P1_CLK	USB-HOST optional clock control: HSIC60M_P1_CLK 0x0: Optional functional clock is disabled 0x1: Optional functional clock is enabled	RW	0

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Bits	Field Name	Description	Type	Reset
10	OPTFCLKEN_UTMI_P3_CLK	USB-HOST optional clock control: UTMI_P3_CLK 0x0: Optional functional clock is disabled 0x1: Optional functional clock is enabled	RW	0
9	OPTFCLKEN_UTMI_P2_CLK	USB-HOST optional clock control: UTMI_P2_CLK when CLKSEL_UTMI_P2 is 0 0x0: Optional functional clock is disabled 0x1: Optional functional clock is enabled	RW	0
8	OPTFCLKEN_UTMI_P1_CLK	USB-HOST optional clock control: UTMI_P1_CLK when CLKSEL_UTMI_P1 is 0 0x0: Optional functional clock is disabled 0x1: Optional functional clock is enabled	RW	0
7:5	RESERVED		R	0x0
4	SAR_MODE	SAR mode control for the module. Shall not be modify except if module is disabled. 0x0: SAR mode is disabled 0x1: SAR mode is enabled	RW	0
3:2	RESERVED		R	0x0
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by software. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen. Read 0x3: Reserved	RW	0x0

Table 3-1303. Register Call Summary for Register CM_L3INIT_HSUSBHOST_CLKCTRL

Clock Management Functional Description
- CM Clock Source: [0] [1]
- Clock Domain Module Attributes: [2] [3] [4]

PRCM Register Manual
- L3INIT_CM2 Register Summary: [5]

Table 3-1304. CM_L3INIT_HSUSBOTG_CLKCTRL

Address Offset	0x0000 0060		
Physical Address	0x4A00 9360	**Instance**	L3INIT_CM2
Description	This register manages the USB_OTG_HS clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							CLKSEL_60M	RESERVED					STBYST	IDLEST		RESERVED							OPTFCLKEN_XCLK	RESERVED						MODULEMODE	

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Bits	Field Name	Description	Type	Reset
31:25	RESERVED		R	0x00
24	CLKSEL_60M	Selects the source of the 60MHz functional clock. 0x0: The 60MHz clock is sourced from on die UTMI PHY 0x1: The 60MHz clock is sourced from the external ULPI PHY	RW	0
23:19	RESERVED		R	0x00
18	STBYST	Module standby status. [warm reset insensitive] Read 0x0: Module is functional (not in standby) Read 0x1: Module is in standby	R	1
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:9	RESERVED		R	0x00
8	OPTFCLKEN_XCLK	USB_OTG optional clock control: XCLK (60MHz clock) 0x0: Optional functional clock is disabled 0x1: Optional functional clock is enabled	RW	0
7:2	RESERVED		R	0x00
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by software. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). 0x1: Module is managed automatically by hardware according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CLKTRCTRL=3, any INTRCONN access to module is always granted. Module clocks may be gated according to the clock domain state. Read 0x2: Reserved Read 0x3: Reserved	RW	0x0

Table 3-1305. Register Call Summary for Register CM_L3INIT_HSUSBOTG_CLKCTRL

Clock Management Functional Description • CM Clock Source: [0] • Clock Domain Module Attributes: [1] [2] [3]
PRCM Register Manual • L3INIT_CM2 Register Summary: [4]

Table 3-1306. CM_L3INIT_HSUSBTLL_CLKCTRL

Address Offset	0x0000 0068		
Physical Address	0x4A00 9368	**Instance**	L3INIT_CM2
Description	This register manages the USB_TLL clocks.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED						OPTFCLKEN_USB_CH1_CLK	OPTFCLKEN_USB_CH0_CLK	RESERVED			SAR_MODE	RESERVED		MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:10	RESERVED		R	0x00
9	OPTFCLKEN_USB_CH1_CLK	USB-HOST optional clock control: USB_CH1_CLK 0x0: Optional functional clock is disabled 0x1: Optional functional clock is enabled	RW	0
8	OPTFCLKEN_USB_CH0_CLK	USB-HOST optional clock control: USB_CH0_CLK 0x0: Optional functional clock is disabled 0x1: Optional functional clock is enabled	RW	0
7:5	RESERVED		R	0x0
4	SAR_MODE	SAR mode control for the module. Shall not be modify except if module is disabled. 0x0: SAR mode is disabled 0x1: SAR mode is enabled	RW	0
3:2	RESERVED		R	0x0
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by software. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). 0x1: Module is managed automatically by hardware according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CLKTRCTRL=3, any INTRCONN access to module is always granted. Module clocks may be gated according to the clock domain state. Read 0x2: Reserved Read 0x3: Reserved	RW	0x0

Table 3-1307. Register Call Summary for Register CM_L3INIT_HSUSBTLL_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • L3INIT_CM2 Register Summary: [2] • RESTORE_CM2 Register Description: [3]

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Table 3-1308. CM_L3INIT_FSUSB_CLKCTRL

Address Offset	0x0000 00D0		
Physical Address	0x4A00 93D0	**Instance**	L3INIT_CM2
Description	This register manages the USB_HOST_FS clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													STBYST	IDLEST		RESERVED														MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:19	RESERVED		R	0x0000
18	STBYST	Module standby status. [warm reset insensitive] Read 0x0: Module is functional (not in standby) Read 0x1: Module is in standby	R	1
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by software. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen. Read 0x3: Reserved	RW	0x0

Table 3-1309. Register Call Summary for Register CM_L3INIT_FSUSB_CLKCTRL

Clock Management Functional Description
- Clock Domain Module Attributes: [0] [1] [2]

PRCM Register Manual
- L3INIT_CM2 Register Summary: [3]

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Table 3-1310. CM_L3INIT_USBPHY_CLKCTRL

Address Offset	0x0000 00E0		
Physical Address	0x4A00 93E0	**Instance**	L3INIT_CM2
Description	This register manages the USBPHY clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED							OPTFCLKEN_PHY_48M	RESERVED						MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:9	RESERVED		R	0x00
8	OPTFCLKEN_PHY_48M	USBPHY optional clock control: PHY_48M 0x0: Optional functional clock is disabled 0x1: Optional functional clock is enabled	RW	0
7:2	RESERVED		R	0x00
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by software. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). 0x1: Module is managed automatically by hardware according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CLKTRCTRL=3, any INTRCONN access to module is always granted. Module clocks may be gated according to the clock domain state. Read 0x2: Reserved Read 0x3: Reserved	RW	0x0

Table 3-1311. Register Call Summary for Register CM_L3INIT_USBPHY_CLKCTRL

Clock Management Functional Description
- Clock Domain Module Attributes: [0] [1]

PRCM Register Manual
- L3INIT_CM2 Register Summary: [2]

3.11.39 L4PER_CM2 Registers

3.11.39.1 L4PER_CM2 Register Summary

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Table 3-1312. L4PER_CM2 Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	L4PER_CM2 L4 Base Address
CM_L4PER_CLKSTCTRL	RW	32	0x0000 0000	0x4A00 9400
CM_L4PER_DYNAMICDEP	RW	32	0x0000 0008	0x4A00 9408
RESERVED	RW	32	0x0000 0020	0x4A00 9420
CM_L4PER_GPTIMER10_CLKCTRL	RW	32	0x0000 0028	0x4A00 9428
CM_L4PER_GPTIMER11_CLKCTRL	RW	32	0x0000 0030	0x4A00 9430
CM_L4PER_GPTIMER2_CLKCTRL	RW	32	0x0000 0038	0x4A00 9438
CM_L4PER_GPTIMER3_CLKCTRL	RW	32	0x0000 0040	0x4A00 9440
CM_L4PER_GPTIMER4_CLKCTRL	RW	32	0x0000 0048	0x4A00 9448
CM_L4PER_GPTIMER9_CLKCTRL	RW	32	0x0000 0050	0x4A00 9450
CM_L4PER_ELM_CLKCTRL	R	32	0x0000 0058	0x4A00 9458
CM_L4PER_GPIO2_CLKCTRL	RW	32	0x0000 0060	0x4A00 9460
CM_L4PER_GPIO3_CLKCTRL	RW	32	0x0000 0068	0x4A00 9468
CM_L4PER_GPIO4_CLKCTRL	RW	32	0x0000 0070	0x4A00 9470
CM_L4PER_GPIO5_CLKCTRL	RW	32	0x0000 0078	0x4A00 9478
CM_L4PER_GPIO6_CLKCTRL	RW	32	0x0000 0080	0x4A00 9480
CM_L4PER_HDQ1W_CLKCTRL	RW	32	0x0000 0088	0x4A00 9488
RESERVED	RW	32	0x0000 0090	0x4A00 9490
RESERVED	RW	32	0x0000 0098	0x4A00 9498
CM_L4PER_I2C1_CLKCTRL	RW	32	0x0000 00A0	0x4A00 94A0
CM_L4PER_I2C2_CLKCTRL	RW	32	0x0000 00A8	0x4A00 94A8
CM_L4PER_I2C3_CLKCTRL	RW	32	0x0000 00B0	0x4A00 94B0
CM_L4PER_I2C4_CLKCTRL	RW	32	0x0000 00B8	0x4A00 94B8
CM_L4PER_L4PER_CLKCTRL	R	32	0x0000 00C0	0x4A00 94C0
RESERVED	RW	32	0x0000 00D0	0x4A00 94D0
RESERVED	RW	32	0x0000 00D8	0x4A00 94D8
CM_L4PER_MCBSP4_CLKCTRL	RW	32	0x0000 00E0	0x4A00 94E0
RESERVED	RW	32	0x0000 00E8	0x4A00 94E8
CM_L4PER_MCSPI1_CLKCTRL	RW	32	0x0000 00F0	0x4A00 94F0
CM_L4PER_MCSPI2_CLKCTRL	RW	32	0x0000 00F8	0x4A00 94F8
CM_L4PER_MCSPI3_CLKCTRL	RW	32	0x0000 0100	0x4A00 9500
CM_L4PER_MCSPI4_CLKCTRL	RW	32	0x0000 0108	0x4A00 9508
CM_L4PER_MMCSD3_CLKCTRL	RW	32	0x0000 0120	0x4A00 9520
CM_L4PER_MMCSD4_CLKCTRL	RW	32	0x0000 0128	0x4A00 9528
RESERVED	RW	32	0x0000 0130	0x4A00 9530
CM_L4PER_SLIMBUS2_CLKCTRL	RW	32	0x0000 0138	0x4A00 9538
CM_L4PER_UART1_CLKCTRL	RW	32	0x0000 0140	0x4A00 9540
CM_L4PER_UART2_CLKCTRL	RW	32	0x0000 0148	0x4A00 9548
CM_L4PER_UART3_CLKCTRL	RW	32	0x0000 0150	0x4A00 9550
CM_L4PER_UART4_CLKCTRL	RW	32	0x0000 0158	0x4A00 9558
CM_L4PER_MMCSD5_CLKCTRL	RW	32	0x0000 0160	0x4A00 9560
RESERVED	RW	32	0x0000 0168	0x4A00 9568
RESERVED	RW	32	0x0000 0180	0x4A00 9580
RESERVED	RW	32	0x0000 0184	0x4A00 9584
RESERVED	R	32	0x0000 0188	0x4A00 9588
RESERVED	RW	32	0x0000 01A0	0x4A00 95A0
RESERVED	RW	32	0x0000 01A8	0x4A00 95A8
RESERVED	RW	32	0x0000 01B0	0x4A00 95B0

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Table 3-1312. L4PER_CM2 Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	L4PER_CM2 L4 Base Address
RESERVED	RW	32	0x0000 01B8	0x4A00 95B8
RESERVED	RW	32	0x0000 01C0	0x4A00 95C0
RESERVED	RW	32	0x0000 01C8	0x4A00 95C8
RESERVED	R	32	0x0000 01D8	0x4A00 95D8

3.11.39.2 L4PER_CM2 Register Description

Table 3-1313. CM_L4PER_CLKSTCTRL

Address Offset	0x0000 0000		
Physical Address	0x4A00 9400	**Instance**	L4PER_CM2
Description	This register enables the domain power state transition. It controls the hardware supervised domain power state transition between ON-ACTIVE and ON-INACTIVE states. It also holds 1 status bit per clock input of the domain.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						CLKACTIVITY_PER_ABE_24M_FCLK	RESERVED	RESERVED	CLKACTIVITY_PER_MCBSP4_FCLK	RESERVED		CLKACTIVITY_PER_96M_FCLK	CLKACTIVITY_PER_48M_FCLK	CLKACTIVITY_PER_32K_FCLK	CLKACTIVITY_PER_24MC_FCLK	CLKACTIVITY_12M_FCLK_FCLK	CLKACTIVITY_GPT9_FCLK	CLKACTIVITY_GPT4_FCLK	CLKACTIVITY_GPT3_FCLK	CLKACTIVITY_GPT2_FCLK	CLKACTIVITY_GPT11_FCLK	CLKACTIVITY_GPT10_FCLK	CLKACTIVITY_L4_PER_ICLK	RESERVED						CLKTRCTRL	

Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x00
25	CLKACTIVITY_PER_ABE_24M_FCLK	This field indicates the state of the PER_ABE_24M_FCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
24	RESERVED		R	0
23	RESERVED		R	0
22	CLKACTIVITY_PER_MCBSP4_FCLK	This field indicates the state of the PER_MCBSP4_FCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
21:20	RESERVED		R	0

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Bits	Field Name	Description	Type	Reset
19	CLKACTIVITY_PER_96M_FCLK	This field indicates the state of the PER_96M_FCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
18	CLKACTIVITY_PER_48M_FCLK	This field indicates the state of the PER_48M_FCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
17	CLKACTIVITY_PER_32K_FCLK	This field indicates the state of the PER_32K_FCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
16	CLKACTIVITY_PER_24MC_FCLK	This field indicates the state of the PER_24MC_FCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
15	CLKACTIVITY_12M_FCLK	This field indicates the state of the FUNC_12M_FCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
14	CLKACTIVITY_GPT9_FCLK	This field indicates the state of the DMT9_FCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
13	CLKACTIVITY_GPT4_FCLK	This field indicates the state of the DMT4_FCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
12	CLKACTIVITY_GPT3_FCLK	This field indicates the state of the DMT3_FCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
11	CLKACTIVITY_GPT2_FCLK	This field indicates the state of the DMT2_FCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
10	CLKACTIVITY_GPT11_FCLK	This field indicates the state of the DMT11_FCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
9	CLKACTIVITY_GPT10_FCLK	This field indicates the state of the DMT10_FCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0

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Bits	Field Name	Description	Type	Reset
8	CLKACTIVITY_L4_PER_ICLK	This field indicates the state of the L4_PER_GICLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
7:2	RESERVED		R	0x00
1:0	CLKTRCTRL	Controls the clock state transition of the L4PER clock domain. 0x0: NO_SLEEP: Sleep transition cannot be initiated. Wakeup transition may however occur. 0x1: SW_SLEEP: Start a software forced sleep transition on the domain. 0x2: SW_WKUP: Start a software forced wake-up transition on the domain. 0x3: HW_AUTO: Automatic transition is enabled. Sleep and wakeup transition are based upon hardware conditions.	RW	0x0

Table 3-1314. Register Call Summary for Register CM_L4PER_CLKSTCTRL

Clock Management Functional Description
- Clock Domain Modes: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14]

PRCM Register Manual
- L4PER_CM2 Register Summary: [15]
- RESTORE_CM2 Register Description: [16]

Table 3-1315. CM_L4PER_DYNAMICDEP

Address Offset	0x0000 0008		
Physical Address	0x4A00 9408	**Instance**	L4PER_CM2
Description	This register controls the dynamic domain depedencies from L4PER domain towards 'target' domains. It is relevant only for domain having INTRCONN master port(s).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				WINDOWSIZE				RESERVED															DSS_DYNDEP	L3_INIT_DYNDEP	RESERVED						

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:24	WINDOWSIZE	Size of sliding window used to monitor INTRCONN interface activity for determination of auto-sleep feature. Time unit defined by CM_DYN_DEP_PRESCAL register.	RW	0x4
23:9	RESERVED		R	0x020
8	DSS_DYNDEP	Dynamic dependency towards DSS clock domain Read 0x1: Dependency is enabled	R Rreturns 1s	1
7	L3_INIT_DYNDEP	Dynamic dependency towards L3INIT clock domain Read 0x1: Dependency is enabled	R Rreturns 1s	1
6:0	RESERVED		R	0x00

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Table 3-1316. Register Call Summary for Register CM_L4PER_DYNAMICDEP

Clock Management Functional Description • Clock Domain Dependency: [0] [1]
PRCM Register Manual • L4PER_CM2 Register Summary: [2] • RESTORE_CM2 Register Description: [3]

Table 3-1317. CM_L4PER_GPTIMER10_CLKCTRL

Address Offset	0x0000 0028		
Physical Address	0x4A00 9428	**Instance**	L4PER_CM2
Description	This register manages the DMTIMER10 clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							CLKSEL	RESERVED						IDLEST		RESERVED														MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:25	RESERVED		R	0x00
24	CLKSEL	Select the source of the functional clock 0x0: Selects the SYS_CLK as the source 0x1: Selects the 32KHz as the source	RW	0
23:18	RESERVED		R	0x00
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by software. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen. Read 0x3: Reserved	RW	0x0

Table 3-1318. Register Call Summary for Register CM_L4PER_GPTIMER10_CLKCTRL

Clock Management Functional Description • PRM Clock Source: [0] • Clock Domain Module Attributes: [1] [2]

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Table 3-1318. Register Call Summary for Register CM_L4PER_GPTIMER10_CLKCTRL (continued)

PRCM Register Manual
- L4PER_CM2 Register Summary: [3]

Table 3-1319. CM_L4PER_GPTIMER11_CLKCTRL

Address Offset	0x0000 0030		
Physical Address	0x4A00 9430	**Instance**	L4PER_CM2
Description	This register manages the DMTIMER11 clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							CLKSEL	RESERVED						IDLEST		RESERVED														MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:25	RESERVED		R	0x00
24	CLKSEL	Select the source of the functional clock 0x0: Selects the SYS_CLK as the source 0x1: Selects the 32KHz as the source	RW	0
23:18	RESERVED		R	0x00
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by software. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen. Read 0x3: Reserved	RW	0x0

Table 3-1320. Register Call Summary for Register CM_L4PER_GPTIMER11_CLKCTRL

Clock Management Functional Description
- PRM Clock Source: [0]
- Clock Domain Module Attributes: [1] [2]

PRCM Register Manual
- L4PER_CM2 Register Summary: [3]

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Table 3-1321. CM_L4PER_GPTIMER2_CLKCTRL

Address Offset	0x0000 0038		
Physical Address	0x4A00 9438	**Instance**	L4PER_CM2
Description	This register manages the DMTIMER2 clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							CLKSEL	RESERVED						IDLEST		RESERVED														MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:25	RESERVED		R	0x00
24	CLKSEL	Select the source of the functional clock 0x0: Selects the SYS_CLK as the source 0x1: Selects the 32KHz as the source	RW	0
23:18	RESERVED		R	0x00
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by software. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen. Read 0x3: Reserved	RW	0x0

Table 3-1322. Register Call Summary for Register CM_L4PER_GPTIMER2_CLKCTRL

Clock Management Functional Description
- PRM Clock Source: [0]
- Clock Domain Module Attributes: [1] [2]

PRCM Register Manual
- L4PER_CM2 Register Summary: [3]

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Table 3-1323. CM_L4PER_GPTIMER3_CLKCTRL

Address Offset	0x0000 0040		
Physical Address	0x4A00 9440	**Instance**	L4PER_CM2
Description	This register manages the DMTIMER3 clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							CLKSEL	RESERVED						IDLEST		RESERVED														MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:25	RESERVED		R	0x00
24	CLKSEL	Select the source of the functional clock 0x0: Selects the SYS_CLK as the source 0x1: Selects the 32KHz as the source	RW	0
23:18	RESERVED		R	0x00
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by software. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen. Read 0x3: Reserved	RW	0x0

Table 3-1324. Register Call Summary for Register CM_L4PER_GPTIMER3_CLKCTRL

Clock Management Functional Description
- PRM Clock Source: [0]
- Clock Domain Module Attributes: [1] [2]

PRCM Register Manual
- L4PER_CM2 Register Summary: [3]

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Table 3-1325. CM_L4PER_GPTIMER4_CLKCTRL

Address Offset	0x0000 0048		
Physical Address	0x4A00 9448	**Instance**	L4PER_CM2
Description	This register manages the DMTIMER4 clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							CLKSEL	RESERVED						IDLEST		RESERVED														MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:25	RESERVED		R	0x00
24	CLKSEL	Select the source of the functional clock 0x0: Selects the SYS_CLK as the source 0x1: Selects the 32KHz as the source	RW	0
23:18	RESERVED		R	0x00
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by software. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen. Read 0x3: Reserved	RW	0x0

Table 3-1326. Register Call Summary for Register CM_L4PER_GPTIMER4_CLKCTRL

Clock Management Functional Description
- PRM Clock Source: [0]
- Clock Domain Module Attributes: [1] [2]

PRCM Register Manual
- L4PER_CM2 Register Summary: [3]

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Table 3-1327. CM_L4PER_GPTIMER9_CLKCTRL

Address Offset	0x0000 0050		
Physical Address	0x4A00 9450	**Instance**	L4PER_CM2
Description	This register manages the DMTIMER9 clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							CLKSEL	RESERVED						IDLEST		RESERVED														MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:25	RESERVED		R	0x00
24	CLKSEL	Select the source of the functional clock 0x0: Selects the SYS_CLK as the source 0x1: Selects the 32KHz as the source	RW	0
23:18	RESERVED		R	0x00
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by software. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen. Read 0x3: Reserved	RW	0x0

Table 3-1328. Register Call Summary for Register CM_L4PER_GPTIMER9_CLKCTRL

Clock Management Functional Description
- PRM Clock Source: [0]
- Clock Domain Module Attributes: [1] [2]

PRCM Register Manual
- L4PER_CM2 Register Summary: [3]

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Table 3-1329. CM_L4PER_ELM_CLKCTRL

Address Offset	0x0000 0058		
Physical Address	0x4A00 9458	**Instance**	L4PER_CM2
Description	This register manages the ELM clocks.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED								MODULEMODE							

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. Read 0x1: Module is managed automatically by hardware according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CLKTRCTRL=3, any INTRCONN access to module is always granted. Module clocks may be gated according to the clock domain state.	R Rreturns	0x1

Table 3-1330. Register Call Summary for Register CM_L4PER_ELM_CLKCTRL

Clock Management Functional Description
- Clock Domain Module Attributes: [0] [1]

PRCM Register Manual
- L4PER_CM2 Register Summary: [2]

Table 3-1331. CM_L4PER_GPIO2_CLKCTRL

Address Offset	0x0000 0060		
Physical Address	0x4A00 9460	**Instance**	L4PER_CM2
Description	This register manages the GPIO2 clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED							OPTFCLKEN_DBCLK	RESERVED						MODULEMODE	

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Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:9	RESERVED		R	0x00
8	OPTFCLKEN_DBCLK	Optional functional clock control. 0x0: Optional functional clock is disabled 0x1: Optional functional clock is enabled	RW	0
7:2	RESERVED		R	0x00
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by software. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). 0x1: Module is managed automatically by hardware according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CLKTRCTRL=3, any INTRCONN access to module is always granted. Module clocks may be gated according to the clock domain state. Read 0x2: Reserved Read 0x3: Reserved	RW	0x0

Table 3-1332. Register Call Summary for Register CM_L4PER_GPIO2_CLKCTRL

Clock Management Functional Description
- Clock Domain Module Attributes: [0] [1]

PRCM Register Manual
- L4PER_CM2 Register Summary: [2]
- RESTORE_CM2 Register Description: [3]

Table 3-1333. CM_L4PER_GPIO3_CLKCTRL

Address Offset	0x0000 0068		
Physical Address	0x4A00 9468	**Instance**	L4PER_CM2
Description	This register manages the GPIO3 clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED							OPTFCLKEN_DBCLK	RESERVED						MODULEMODE	

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Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:9	RESERVED		R	0x00
8	OPTFCLKEN_DBCLK	Optional functional clock control. 0x0: Optional functional clock is disabled 0x1: Optional functional clock is enabled	RW	0
7:2	RESERVED		R	0x00
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by software. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). 0x1: Module is managed automatically by hardware according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CLKTRCTRL=3, any INTRCONN access to module is always granted. Module clocks may be gated according to the clock domain state. Read 0x2: Reserved Read 0x3: Reserved	RW	0x0

Table 3-1334. Register Call Summary for Register CM_L4PER_GPIO3_CLKCTRL

Clock Management Functional Description
- Clock Domain Module Attributes: [0] [1]

PRCM Register Manual
- L4PER_CM2 Register Summary: [2]
- RESTORE_CM2 Register Description: [3]

Table 3-1335. CM_L4PER_GPIO4_CLKCTRL

Address Offset	0x0000 0070		
Physical Address	0x4A00 9470	**Instance**	L4PER_CM2
Description	This register manages the GPIO4 clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED							OPTFCLKEN_DBCLK	RESERVED						MODULEMODE	

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Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:9	RESERVED		R	0x00
8	OPTFCLKEN_DBCLK	Optional functional clock control. 0x0: Optional functional clock is disabled 0x1: Optional functional clock is enabled	RW	0
7:2	RESERVED		R	0x00
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by software. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). 0x1: Module is managed automatically by hardware according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CLKTRCTRL=3, any INTRCONN access to module is always granted. Module clocks may be gated according to the clock domain state. Read 0x2: Reserved Read 0x3: Reserved	RW	0x0

Table 3-1336. Register Call Summary for Register CM_L4PER_GPIO4_CLKCTRL

Clock Management Functional Description
- Clock Domain Module Attributes: [0] [1]

PRCM Register Manual
- L4PER_CM2 Register Summary: [2]
- RESTORE_CM2 Register Description: [3]

Table 3-1337. CM_L4PER_GPIO5_CLKCTRL

Address Offset	0x0000 0078		
Physical Address	0x4A00 9478	**Instance**	L4PER_CM2
Description	This register manages the GPIO5 clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED							OPTFCLKEN_DBCLK	RESERVED						MODULEMODE	

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Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:9	RESERVED		R	0x00
8	OPTFCLKEN_DBCLK	Optional functional clock control. 0x0: Optional functional clock is disabled 0x1: Optional functional clock is enabled	RW	0
7:2	RESERVED		R	0x00
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by software. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). 0x1: Module is managed automatically by hardware according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CLKTRCTRL=3, any INTRCONN access to module is always granted. Module clocks may be gated according to the clock domain state. Read 0x2: Reserved Read 0x3: Reserved	RW	0x0

Table 3-1338. Register Call Summary for Register CM_L4PER_GPIO5_CLKCTRL

Clock Management Functional Description
- Clock Domain Module Attributes: [0] [1]

PRCM Register Manual
- L4PER_CM2 Register Summary: [2]
- RESTORE_CM2 Register Description: [3]

Table 3-1339. CM_L4PER_GPIO6_CLKCTRL

Address Offset	0x0000 0080		
Physical Address	0x4A00 9480	**Instance**	L4PER_CM2
Description	This register manages the GPIO6 clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED							OPTFCLKEN_DBCLK	RESERVED						MODULEMODE	

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Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:9	RESERVED		R	0x00
8	OPTFCLKEN_DBCLK	Optional functional clock control. 0x0: Optional functional clock is disabled 0x1: Optional functional clock is enabled	RW	0
7:2	RESERVED		R	0x00
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by software. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). 0x1: Module is managed automatically by hardware according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CLKTRCTRL=3, any INTRCONN access to module is always granted. Module clocks may be gated according to the clock domain state. Read 0x2: Reserved Read 0x3: Reserved	RW	0x0

Table 3-1340. Register Call Summary for Register CM_L4PER_GPIO6_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • L4PER_CM2 Register Summary: [2] • RESTORE_CM2 Register Description: [3]

Table 3-1341. CM_L4PER_HDQ1W_CLKCTRL

Address Offset	0x0000 0088		
Physical Address	0x4A00 9488	**Instance**	L4PER_CM2
Description	This register manages the HDQ1W clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED														MODULEMODE	

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Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by software. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen. Read 0x3: Reserved	RW	0x0

Table 3-1342. Register Call Summary for Register CM_L4PER_HDQ1W_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • L4PER_CM2 Register Summary: [2]

Table 3-1343. CM_L4PER_I2C1_CLKCTRL

Address Offset	0x0000 00A0		
Physical Address	0x4A00 94A0	**Instance**	L4PER_CM2
Description	This register manages the I2C1 clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED														MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000

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Bits	Field Name	Description	Type	Reset
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by software. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen. Read 0x3: Reserved	RW	0x0

Table 3-1344. Register Call Summary for Register CM_L4PER_I2C1_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • L4PER_CM2 Register Summary: [2]

Table 3-1345. CM_L4PER_I2C2_CLKCTRL

Address Offset	0x0000 00A8		
Physical Address	0x4A00 94A8	**Instance**	L4PER_CM2
Description	This register manages the I2C2 clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED														MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by software. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen. Read 0x3: Reserved	RW	0x0

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Table 3-1346. Register Call Summary for Register CM_L4PER_I2C2_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • L4PER_CM2 Register Summary: [2]

Table 3-1347. CM_L4PER_I2C3_CLKCTRL

Address Offset	0x0000 00B0		
Physical Address	0x4A00 94B0	**Instance**	L4PER_CM2
Description	This register manages the I2C3 clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED								MODULEMODE							

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by software. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen. Read 0x3: Reserved	RW	0x0

Table 3-1348. Register Call Summary for Register CM_L4PER_I2C3_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • L4PER_CM2 Register Summary: [2]

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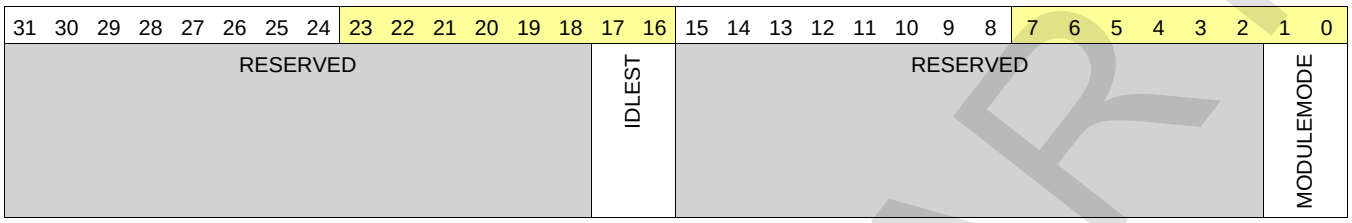
Table 3-1349. CM_L4PER_I2C4_CLKCTRL

Address Offset	0x0000 00B8		
Physical Address	0x4A00 94B8	**Instance**	L4PER_CM2
Description	This register manages the I2C4 clocks.		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by software. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen. Read 0x3: Reserved	RW	0x0

Table 3-1350. Register Call Summary for Register CM_L4PER_I2C4_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • L4PER_CM2 Register Summary: [2]

Table 3-1351. CM_L4PER_L4PER_CLKCTRL

Address Offset	0x0000 00C0		
Physical Address	0x4A00 94C0	**Instance**	L4PER_CM2
Description	This register manages the L4PER clocks.		
Type	R		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED								MODULEMODE							

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. Read 0x1: Module is managed automatically by hardware according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CLKTRCTRL=3, any INTRCONN access to module is always granted. Module clocks may be gated according to the clock domain state.	R Rreturns	0x1

Table 3-1352. Register Call Summary for Register CM_L4PER_L4PER_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • L4PER_CM2 Register Summary: [2]

Table 3-1353. CM_L4PER_MCBSP4_CLKCTRL

Address Offset	0x0000 00E0		
Physical Address	0x4A00 94E0	**Instance**	L4PER_CM2
Description	This register manages the MCBSP4 clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						CLKSEL_INTERNAL_SOURCE	CLKSEL_SOURCE	RESERVED						IDLEST		RESERVED														MODULEMODE	

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Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x00
25	CLKSEL_INTERNAL_SOURCE	Selects the internal clock to be used as the functional clock in case CLKSEL_SOURCE selects the internal clock source as the functional clock source. 0x0: 96MHz clock derived from DPLL_PER is selected 0x1: 98MHz clock derived from DPLL_ABE is selected	RW	0
24	CLKSEL_SOURCE	Selects the source of the functional clock between, internal source and CLKS pad. The switching between the clocks is not guaranteed to be glitchless. 0x0: Functional clock is sourced from an internal clock 0x1: Functional clock is sourced from CLKS pad	RW	0
23:18	RESERVED		R	0x00
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by software. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen. Read 0x3: Reserved	RW	0x0

Table 3-1354. Register Call Summary for Register CM_L4PER_MCBSP4_CLKCTRL

Clock Management Functional Description
- CM Clock Source: [0] [1]
- Clock Domain Module Attributes: [2] [3]

PRCM Register Manual
- L4PER_CM2 Register Summary: [4]

Table 3-1355. CM_L4PER_MCSPI1_CLKCTRL

Address Offset	0x0000 00F0		
Physical Address	0x4A00 94F0	**Instance**	L4PER_CM2
Description	This register manages the MCSPI1 clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED														MODULEMODE	

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Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by software. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen. Read 0x3: Reserved	RW	0x0

Table 3-1356. Register Call Summary for Register CM_L4PER_MCSPI1_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • L4PER_CM2 Register Summary: [2]

Table 3-1357. CM_L4PER_MCSPI2_CLKCTRL

Address Offset	0x0000 00F8		
Physical Address	0x4A00 94F8	**Instance**	L4PER_CM2
Description	This register manages the MCSPI2 clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED														MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000

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Bits	Field Name	Description	Type	Reset
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by software. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen. Read 0x3: Reserved	RW	0x0

Table 3-1358. Register Call Summary for Register CM_L4PER_MCSPI2_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • L4PER_CM2 Register Summary: [2]

Table 3-1359. CM_L4PER_MCSPI3_CLKCTRL

Address Offset	0x0000 0100		
Physical Address	0x4A00 9500	**Instance**	L4PER_CM2
Description	This register manages the MCSPI3 clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED								MODULEMODE							

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by software. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen. Read 0x3: Reserved	RW	0x0

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Table 3-1360. Register Call Summary for Register CM_L4PER_MCSPI3_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • L4PER_CM2 Register Summary: [2]

Table 3-1361. CM_L4PER_MCSPI4_CLKCTRL

Address Offset	0x0000 0108		
Physical Address	0x4A00 9508	**Instance**	L4PER_CM2
Description	This register manages the MCSPI4 clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED								MODULEMODE							

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by software. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen. Read 0x3: Reserved	RW	0x0

Table 3-1362. Register Call Summary for Register CM_L4PER_MCSPI4_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • L4PER_CM2 Register Summary: [2]

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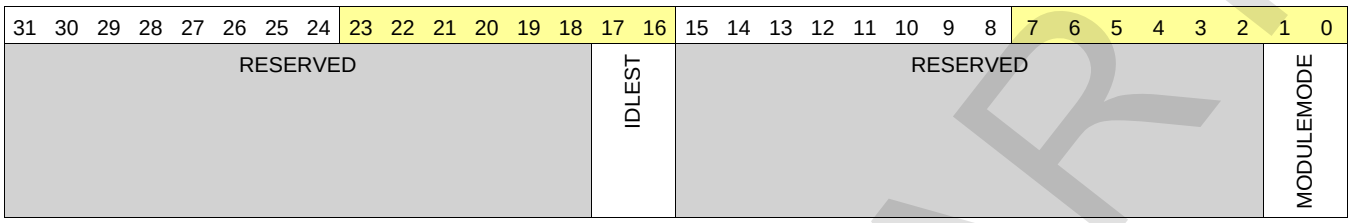
Table 3-1363. CM_L4PER_MMCSD3_CLKCTRL

Address Offset	0x0000 0120		
Physical Address	0x4A00 9520	**Instance**	L4PER_CM2
Description	This register manages the MMCSD3 clocks.		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by software. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen. Read 0x3: Reserved	RW	0x0

Table 3-1364. Register Call Summary for Register CM_L4PER_MMCSD3_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • L4PER_CM2 Register Summary: [2]

Table 3-1365. CM_L4PER_MMCSD4_CLKCTRL

Address Offset	0x0000 0128		
Physical Address	0x4A00 9528	**Instance**	L4PER_CM2
Description	This register manages the MMCSD4 clocks.		
Type	RW		

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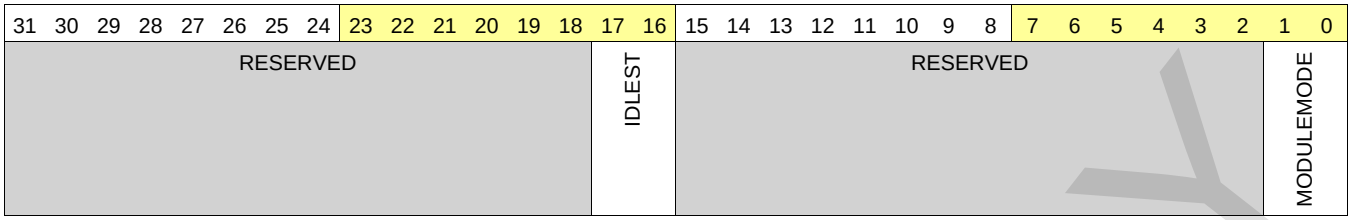

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by software. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen. Read 0x3: Reserved	RW	0x0

Table 3-1366. Register Call Summary for Register CM_L4PER_MMCSD4_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • L4PER_CM2 Register Summary: [2]

Table 3-1367. CM_L4PER_SLIMBUS2_CLKCTRL

Address Offset	0x0000 0138		
Physical Address	0x4A00 9538	**Instance**	L4PER_CM2
Description	This register manages the SLIMBUS2 clocks.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED					OPTFCLKEN_SLIMBUS_CLK	OPTFCLKEN_PERABE24M_FCLK	OPTFCLKEN_PER24MC_FCLK	RESERVED						MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:11	RESERVED		R	0x00
10	OPTFCLKEN_SLIMBUS_CLK	Optional functional clock control. 0x0: Optional functional clock is disabled 0x1: Optional functional clock is enabled	RW	0
9	OPTFCLKEN_PERABE24M_FCLK	Optional functional clock control for PER_ABE_24M_FCLK clock. 0x0: Optional functional clock is disabled 0x1: Optional functional clock is enabled	RW	0
8	OPTFCLKEN_PER24MC_FCLK	Optional functional clock control for PER_24MC_FCLK clock. 0x0: Optional functional clock is disabled 0x1: Optional functional clock is enabled	RW	0
7:2	RESERVED		R	0x00
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by software. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen. Read 0x3: Reserved	RW	0x0

Table 3-1368. Register Call Summary for Register CM_L4PER_SLIMBUS2_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • L4PER_CM2 Register Summary: [2]

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Table 3-1369. CM_L4PER_UART1_CLKCTRL

Address Offset	0x0000 0140		
Physical Address	0x4A00 9540	**Instance**	L4PER_CM2
Description	This register manages the UART1 clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED														MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by software. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen. Read 0x3: Reserved	RW	0x0

Table 3-1370. Register Call Summary for Register CM_L4PER_UART1_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • L4PER_CM2 Register Summary: [2]

Table 3-1371. CM_L4PER_UART2_CLKCTRL

Address Offset	0x0000 0148		
Physical Address	0x4A00 9548	**Instance**	L4PER_CM2
Description	This register manages the UART2 clocks.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED								MODULEMODE							

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by software. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen. Read 0x3: Reserved	RW	0x0

Table 3-1372. Register Call Summary for Register CM_L4PER_UART2_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • L4PER_CM2 Register Summary: [2]

Table 3-1373. CM_L4PER_UART3_CLKCTRL

Address Offset	0x0000 0150		
Physical Address	0x4A00 9550	**Instance**	L4PER_CM2
Description	This register manages the UART3 clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED								MODULEMODE							

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Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by software. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen. Read 0x3: Reserved	RW	0x0

Table 3-1374. Register Call Summary for Register CM_L4PER_UART3_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • L4PER_CM2 Register Summary: [2]

Table 3-1375. CM_L4PER_UART4_CLKCTRL

Address Offset	0x0000 0158		
Physical Address	0x4A00 9558	**Instance**	L4PER_CM2
Description	This register manages the UART4 clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED														MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000

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Bits	Field Name	Description	Type	Reset
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by software. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen. Read 0x3: Reserved	RW	0x0

Table 3-1376. Register Call Summary for Register CM_L4PER_UART4_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • L4PER_CM2 Register Summary: [2]

Table 3-1377. CM_L4PER_MMCSD5_CLKCTRL

Address Offset	0x0000 0160		
Physical Address	0x4A00 9560	**Instance**	L4PER_CM2
Description	This register manages the MMCSD5 clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED														MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by software. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen. Read 0x3: Reserved	RW	0x0

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Table 3-1378. Register Call Summary for Register CM_L4PER_MMCSD5_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • L4PER_CM2 Register Summary: [2]

3.11.40 RESTORE_CM2 Registers

3.11.40.1 RESTORE_CM2 Register Summary

Table 3-1379. RESTORE_CM2 Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	RESTORE_CM2 L4 Base Address
CM_L3_1_CLKSTCTRL_RESTORE	RW	32	0x0000 0000	0x4A00 9E00
CM_L3_2_CLKSTCTRL_RESTORE	RW	32	0x0000 0004	0x4A00 9E04
CM_L4CFG_CLKSTCTRL_RESTORE	RW	32	0x0000 0008	0x4A00 9E08
CM_MEMIF_CLKSTCTRL_RESTORE	RW	32	0x0000 000C	0x4A00 9E0C
CM_L4PER_CLKSTCTRL_RESTORE	RW	32	0x0000 0010	0x4A00 9E10
CM_L3INIT_CLKSTCTRL_RESTORE	RW	32	0x0000 0014	0x4A00 9E14
CM_L3INSTR_L3_3_CLKCTRL_RESTORE	RW	32	0x0000 0018	0x4A00 9E18
CM_L3INSTR_L3_INSTR_CLKCTRL_RESTORE	RW	32	0x0000 001C	0x4A00 9E1C
CM_L3INSTR_OCP_WP1_CLKCTRL_RESTORE	RW	32	0x0000 0020	0x4A00 9E20
CM_CM2_PROFILING_CLKCTRL_RESTORE	RW	32	0x0000 0024	0x4A00 9E24
CM_C2C_STATICDEP_RESTORE	RW	32	0x0000 0028	0x4A00 9E28
CM_L3_1_DYNAMICDEP_RESTORE	RW	32	0x0000 002C	0x4A00 9E2C
CM_L3_2_DYNAMICDEP_RESTORE	RW	32	0x0000 0030	0x4A00 9E30
CM_C2C_DYNAMICDEP_RESTORE	RW	32	0x0000 0034	0x4A00 9E34
CM_L4CFG_DYNAMICDEP_RESTORE	RW	32	0x0000 0038	0x4A00 9E38
CM_L4PER_DYNAMICDEP_RESTORE	RW	32	0x0000 003C	0x4A00 9E3C
CM_L4PER_GPIO2_CLKCTRL_RESTORE	RW	32	0x0000 0040	0x4A00 9E40
CM_L4PER_GPIO3_CLKCTRL_RESTORE	RW	32	0x0000 0044	0x4A00 9E44
CM_L4PER_GPIO4_CLKCTRL_RESTORE	RW	32	0x0000 0048	0x4A00 9E48
CM_L4PER_GPIO5_CLKCTRL_RESTORE	RW	32	0x0000 004C	0x4A00 9E4C
CM_L4PER_GPIO6_CLKCTRL_RESTORE	RW	32	0x0000 0050	0x4A00 9E50
CM_L3INIT_HSUSBHOST_CLKCTRL_RESTORE	RW	32	0x0000 0054	0x4A00 9E54
CM_L3INIT_HSUSBTLL_CLKCTRL_RESTORE	RW	32	0x0000 0058	0x4A00 9E58
CM_SDMA_STATICDEP_RESTORE	RW	32	0x0000 005C	0x4A00 9E5C

3.11.40.2 RESTORE_CM2 Register Description

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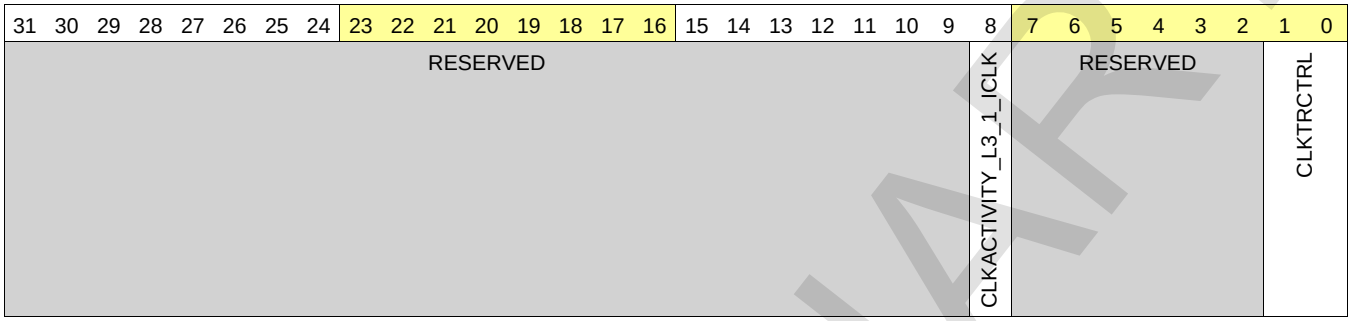
Table 3-1380. CM_L3_1_CLKSTCTRL_RESTORE

Address Offset	0x0000 0000		
Physical Address	0x4A00 9E00	**Instance**	RESTORE_CM2
Description	Second address map for register CM_L3_1_CLKSTCTRL. Used only by automatic restore upon wakeup from device OFF mode.		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	CLKACTIVITY_L3_1_ICLK	This field indicates the state of the L3_1_GICLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
7:2	RESERVED		R	0x00
1:0	CLKTRCTRL	Controls the clock state transition of the L3_1 clock domain. 0x0: NO_SLEEP: Sleep transition cannot be initiated. Wakeup transition may however occur. Read 0x1: Reserved Read 0x2: Reserved 0x3: HW_AUTO: Automatic transition is enabled. Sleep and wakeup transition are based upon hardware conditions.	RW	0x0

Table 3-1381. Register Call Summary for Register CM_L3_1_CLKSTCTRL_RESTORE

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- RESTORE_CM2 Register Summary: [0]

Table 3-1382. CM_L3_2_CLKSTCTRL_RESTORE

Address Offset	0x0000 0004		
Physical Address	0x4A00 9E04	**Instance**	RESTORE_CM2
Description	Second address map for register CM_L3_2_CLKSTCTRL. Used only by automatic restore upon wakeup from device OFF mode.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							CLKACTIVITY_L3_2_ICLK	RESERVED						CLKTRCTRL	

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	CLKACTIVITY_L3_2_ICLK	This field indicates the state of the L3_2_GICLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
7:2	RESERVED		R	0x00
1:0	CLKTRCTRL	Controls the clock state transition of the L3_2 clock domain. 0x0: NO_SLEEP: Sleep transition cannot be initiated. Wakeup transition may however occur. Read 0x1: Reserved Read 0x2: Reserved 0x3: HW_AUTO: Automatic transition is enabled. Sleep and wakeup transition are based upon hardware conditions.	RW	0x0

Table 3-1383. Register Call Summary for Register CM_L3_2_CLKSTCTRL_RESTORE

PRCM Register Manual
- RESTORE_CM2 Register Summary: [0]

Table 3-1384. CM_L4CFG_CLKSTCTRL_RESTORE

Address Offset	0x0000 0008		
Physical Address	0x4A00 9E08	**Instance**	RESTORE_CM2
Description	Second address map for register CM_L4CFG_CLKSTCTRL. Used only by automatic restore upon wakeup from device OFF mode.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							CLKACTIVITY_CFG_L4_ICLK	RESERVED						CLKTRCTRL	

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Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	CLKACTIVITY_CFG_L4_ICLK	This field indicates the state of the L4_CFG_GICLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
7:2	RESERVED		R	0x00
1:0	CLKTRCTRL	Controls the clock state transition of the L4CFG clock domain. 0x0: NO_SLEEP: Sleep transition cannot be initiated. Wakeup transition may however occur. Read 0x1: Reserved Read 0x2: Reserved 0x3: HW_AUTO: Automatic transition is enabled. Sleep and wakeup transition are based upon hardware conditions.	RW	0x0

Table 3-1385. Register Call Summary for Register CM_L4CFG_CLKSTCTRL_RESTORE

PRCM Register Manual
- RESTORE_CM2 Register Summary: [0]

Table 3-1386. CM_MEMIF_CLKSTCTRL_RESTORE

Address Offset	0x0000 000C		
Physical Address	0x4A00 9E0C	**Instance**	RESTORE_CM2
Description	Second address map for register CM_MEMIF_CLKSTCTRL. Used only by automatic restore upon wakeup from device OFF mode.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																		CLKACTIVITY_ASYNC_PHY2_CLK	CLKACTIVITY_ASYNC_PHY1_CLK	CLKACTIVITY_ASYNC_DLL_CLK	CLKACTIVITY_PHY_ROOT_CLK	CLKACTIVITY_DLL_CLK	CLKACTIVITY_L3_EMIF_ICLK	RESERVED						CLKTRCTRL	

Bits	Field Name	Description	Type	Reset
31:14	RESERVED		R	0x00000
13	CLKACTIVITY_ASYNC_PHY2_CLK	This field indicates the state of the ASYNC_PHY2_CLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0

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Bits	Field Name	Description	Type	Reset
12	CLKACTIVITY_ASYNC_PHY1_CLK	This field indicates the state of the ASYNC_PHY1_CLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
11	CLKACTIVITY_ASYNC_DLL_CLK	This field indicates the state of the ASYNC_DLL_CLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
10	CLKACTIVITY_PHY_ROOT_CLK	This field indicates the state of the PHY_ROOT_CLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
9	CLKACTIVITY_DLL_CLK	This field indicates the state of the DLL_CLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
8	CLKACTIVITY_L3_EMIF_ICLK	This field indicates the state of the L3_EMIF_GICLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
7:2	RESERVED		R	0x00
1:0	CLKTRCTRL	Controls the clock state transition of the MEMIF clock domain. 0x0: NO_SLEEP: Sleep transition cannot be initiated. Wakeup transition may however occur. Read 0x1: Reserved 0x2: SW_WKUP: Start a software forced wake-up transition on the domain. 0x3: HW_AUTO: Automatic transition is enabled. Sleep and wakeup transition are based upon hardware conditions.	RW	0x0

Table 3-1387. Register Call Summary for Register CM_MEMIF_CLKSTCTRL_RESTORE

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- RESTORE_CM2 Register Summary: [0]

Table 3-1388. CM_L4PER_CLKSTCTRL_RESTORE

Address Offset	0x0000 0010		
Physical Address	0x4A00 9E10	**Instance**	RESTORE_CM2
Description	Second address map for register CM_L4PER_CLKSTCTRL. Used only by automatic restore upon wakeup from device OFF mode.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						CLKACTIVITY_PER_ABE_24M_FCLK	RESERVED	RESERVED	CLKACTIVITY_PER_MCBSP4_FCLK	RESERVED		CLKACTIVITY_PER_96M_FCLK	CLKACTIVITY_PER_48M_FCLK	CLKACTIVITY_PER_32K_FCLK	CLKACTIVITY_PER_24MC_FCLK	CLKACTIVITY_12M_FCLK_FCLK	CLKACTIVITY_GPT9_FCLK	CLKACTIVITY_GPT4_FCLK	CLKACTIVITY_GPT3_FCLK	CLKACTIVITY_GPT2_FCLK	CLKACTIVITY_GPT11_FCLK	CLKACTIVITY_GPT10_FCLK	CLKACTIVITY_L4_PER_ICLK	RESERVED						CLKTRCTRL	

Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x00
25	CLKACTIVITY_PER_ABE_24M_FCLK	This field indicates the state of the PER_ABE_24M_FCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
24	RESERVED		R	0
23	RESERVED		R	0
22	CLKACTIVITY_PER_MCBSP4_FCLK	This field indicates the state of the PER_MCBSP4_FCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
21:20	RESERVED		R	0
19	CLKACTIVITY_PER_96M_FCLK	This field indicates the state of the PER_96M_FCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
18	CLKACTIVITY_PER_48M_FCLK	This field indicates the state of the PER_48M_FCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
17	CLKACTIVITY_PER_32K_FCLK	This field indicates the state of the PER_32K_FCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
16	CLKACTIVITY_PER_24MC_FCLK	This field indicates the state of the PER_24MC_FCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
15	CLKACTIVITY_12M_FCLK_FCLK	This field indicates the state of the FUNC_12M_FCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0

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Bits	Field Name	Description	Type	Reset
14	CLKACTIVITY_GPT9_FCLK	This field indicates the state of the DMT9_FCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
13	CLKACTIVITY_GPT4_FCLK	This field indicates the state of the DMT4_FCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
12	CLKACTIVITY_GPT3_FCLK	This field indicates the state of the DMT3_FCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
11	CLKACTIVITY_GPT2_FCLK	This field indicates the state of the DMT2_FCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
10	CLKACTIVITY_GPT11_FCLK	This field indicates the state of the DMT11_FCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
9	CLKACTIVITY_GPT10_FCLK	This field indicates the state of the DMT10_FCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
8	CLKACTIVITY_L4_PER_ICLK	This field indicates the state of the L4_PER_GICLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
7:2	RESERVED		R	0x00
1:0	CLKTRCTRL	Controls the clock state transition of the L4PER clock domain. 0x0: NO_SLEEP: Sleep transition cannot be initiated. Wakeup transition may however occur. 0x1: SW_SLEEP: Start a software forced sleep transition on the domain. 0x2: SW_WKUP: Start a software forced wake-up transition on the domain. 0x3: HW_AUTO: Automatic transition is enabled. Sleep and wakeup transition are based upon hardware conditions.	RW	0x0

Table 3-1389. Register Call Summary for Register CM_L4PER_CLKSTCTRL_RESTORE

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- RESTORE_CM2 Register Summary: [0]

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Table 3-1390. CM_L3INIT_CLKSTCTRL_RESTORE

Address Offset	0x0000 0014		
Physical Address	0x4A00 9E14	**Instance**	RESTORE_CM2
Description	Second address map for register CM_L3INIT_CLKSTCTRL. Used only by automatic restore upon wakeup from device OFF mode.		
Type	RW		

31 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11 10	9	8	7 6 5 4 3 2	1 0
RESERVED	CLKACTIVITY_INIT_60M_P2_FCLK	CLKACTIVITY_INIT_60M_P1_FCLK	CLKACTIVITY_HSIC_P2_FCLK	CLKACTIVITY_HSIC_P1_FCLK	CLKACTIVITY_UTMI_ROOT_FCLK	RESERVED	CLKACTIVITY_TLL_CH1_FCLK	CLKACTIVITY_TLL_CH0_FCLK	CLKACTIVITY_HSIC_P2_480M_FCLK	CLKACTIVITY_HSIC_P1_480M_FCLK	CLKACTIVITY_INIT_HSMMC6_FCLK	CLKACTIVITY_INIT_HSMMC2_FCLK	CLKACTIVITY_INIT_HSMMC1_FCLK	CLKACTIVITY_INIT_HSI_FCLK	CLKACTIVITY_USB_DPLL_HS_CLK	CLKACTIVITY_USB_DPLL_CLK	CLKACTIVITY_INIT_48MC_FCLK	CLKACTIVITY_INIT_48M_FCLK	RESERVED	CLKACTIVITY_INIT_L4_ICLK	CLKACTIVITY_INIT_L3_ICLK	RESERVED	CLKTRCTRL

Bits	Field Name	Description	Type	Reset
31:30	RESERVED		R	0x0
29	CLKACTIVITY_INIT_60M_P2_FCLK	This field indicates the state of the INIT_60M_P2_FCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
28	CLKACTIVITY_INIT_60M_P1_FCLK	This field indicates the state of the INIT_60M_P1_FCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
27	CLKACTIVITY_HSIC_P2_FCLK	This field indicates the state of the HSIC_P2_FCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
26	CLKACTIVITY_HSIC_P1_FCLK	This field indicates the state of the HSIC_P1_FCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
25	CLKACTIVITY_UTMI_ROOT_FCLK	This field indicates the state of the UTMI_ROOT_FCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
24	RESERVED		R	0
23	CLKACTIVITY_TLL_CH1_FCLK	This field indicates the state of the TLL_CH1_FCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0

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Bits	Field Name	Description	Type	Reset
22	CLKACTIVITY_TLL_CH0_FCLK	This field indicates the state of the TLL_CH0_FCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
21	CLKACTIVITY_HSIC_P2_480M_FCLK	This field indicates the state of the HSIC_P2_480M_FCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
20	CLKACTIVITY_HSIC_P1_480M_FCLK	This field indicates the state of the HSIC_P1_480M_FCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
19	CLKACTIVITY_INIT_HSMMC6_FCLK	This field indicates the state of the INIT_HSMMC6_FCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
18	CLKACTIVITY_INIT_HSMMC2_FCLK	This field indicates the state of the INIT_HSMMC2_FCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
17	CLKACTIVITY_INIT_HSMMC1_FCLK	This field indicates the state of the INIT_HSMMC1_FCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
16	CLKACTIVITY_INIT_HSI_FCLK	This field indicates the state of the INIT_HSI_FCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
15	CLKACTIVITY_USB_DPLL_HS_CLK	This field indicates the state of the USB_DPLL_HS_CLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
14	CLKACTIVITY_USB_DPLL_CLK	This field indicates the state of the USB_DPLL_CLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
13	CLKACTIVITY_INIT_48MC_FCLK	This field indicates the state of the INIT_48MC_FCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
12	CLKACTIVITY_INIT_48M_FCLK	This field indicates the state of the INIT_48M_FCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0

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Bits	Field Name	Description	Type	Reset
11:10	RESERVED	Reserved	R	0x0
9	CLKACTIVITY_INIT_L4_ICLK	This field indicates the state of the L4_INIT_GICLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
8	CLKACTIVITY_INIT_L3_ICLK	This field indicates the state of the L3_INIT_GICLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing	R	0
7:2	RESERVED	Reserved	R	0x00
1:0	CLKTRCTRL	Controls the clock state transition of the L3INIT clock domain. 0x0: NO_SLEEP: Sleep transition cannot be initiated. Wakeup transition may however occur. 0x1: SW_SLEEP: Start a software forced sleep transition on the domain. 0x2: SW_WKUP: Start a software forced wake-up transition on the domain. 0x3: HW_AUTO: Automatic transition is enabled. Sleep and wakeup transition are based upon hardware conditions.	RW	0x0

Table 3-1391. Register Call Summary for Register CM_L3INIT_CLKSTCTRL_RESTORE

PRCM Register Manual
- RESTORE_CM2 Register Summary: [0]

Table 3-1392. CM_L3INSTR_L3_3_CLKCTRL_RESTORE

Address Offset	0x0000 0018		
Physical Address	0x4A00 9E18	**Instance**	RESTORE_CM2
Description	Second address map for register CM_L3INSTR_L3_3_CLKCTRL. Used only by automatic restore upon wakeup from device OFF mode.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED								MODULEMODE							

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000

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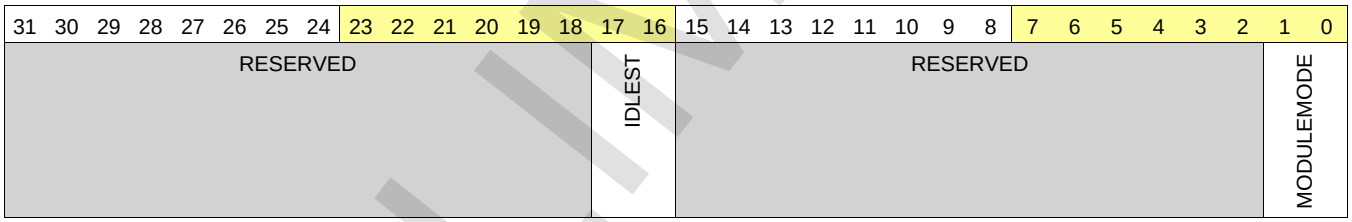
Bits	Field Name	Description	Type	Reset
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by software. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). 0x1: Module is managed automatically by hardware according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CLKTRCTRL=3, any INTRCONN access to module is always granted. Module clocks may be gated according to the clock domain state. Read 0x2: Reserved Read 0x3: Reserved	RW	0x1

Table 3-1393. Register Call Summary for Register CM_L3INSTR_L3_3_CLKCTRL_RESTORE

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • RESTORE_CM2 Register Summary: [2]

Table 3-1394. CM_L3INSTR_L3_INSTR_CLKCTRL_RESTORE

Address Offset	0x0000 001C		
Physical Address	0x4A00 9E1C	**Instance**	RESTORE_CM2
Description	Second address map for register CM_L3INSTR_L3_INSTR_CLKCTRL. Used only by automatic restore upon wakeup from device OFF mode.		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000

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Bits	Field Name	Description	Type	Reset
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by software. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). 0x1: Module is managed automatically by hardware according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CLKTRCTRL=3, any INTRCONN access to module is always granted. Module clocks may be gated according to the clock domain state. Read 0x2: Reserved Read 0x3: Reserved	RW	0x1

Table 3-1395. Register Call Summary for Register CM_L3INSTR_L3_INSTR_CLKCTRL_RESTORE

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • RESTORE_CM2 Register Summary: [2]

Table 3-1396. CM_L3INSTR_OCP_WP1_CLKCTRL_RESTORE

Address Offset	0x0000 0020		
Physical Address	0x4A00 9E20	**Instance**	RESTORE_CM2
Description	Second address map for register CM_L3INSTR_OCP_WP1_CLKCTRL. Used only by automatic restore upon wakeup from device OFF mode.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED														MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x3: Module is disabled and cannot be accessed Read 0x2: Module is in idle mode (only Interconnect part). It is functional if using separate functional clock Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x0: Module is fully functional, including Interconnect	R	0x3
15:2	RESERVED		R	0x0000

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Bits	Field Name	Description	Type	Reset
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by software. Any Interconnect access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). 0x1: Module is managed automatically by hardware according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CLKTRCTRL=3, any Interconnect access to module is always granted. Module clocks may be gated according to the clock domain state. Read 0x2: Reserved Read 0x3: Reserved	RW	0x1

Table 3-1397. Register Call Summary for Register CM_L3INSTR_OCP_WP1_CLKCTRL_RESTORE

PRCM Register Manual
- RESTORE_CM2 Register Summary: [0]

Table 3-1398. CM_CM2_PROFILING_CLKCTRL_RESTORE

Address Offset	0x0000 0024		
Physical Address	0x4A00 9E24	**Instance**	RESTORE_CM2
Description	Second address map for register CM_CM2_PROFILING_CLKCTRL. Used only by automatic restore upon wakeup from device OFF mode. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED														MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status Read 0x3: Module is disabled Read 0x2: Module is in Idle Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x0: Module is fully functional	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disabled by software. OCP configuration port is not accessible. 0x1: Module is managed automatically by hardware along with L3INSTR domain. Read 0x2: Reserved Read 0x3: Reserved	RW	0x1

Table 3-1399. Register Call Summary for Register CM_CM2_PROFILING_CLKCTRL_RESTORE

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- RESTORE_CM2 Register Summary: [0]

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Table 3-1400. CM_C2C_STATICDEP_RESTORE

Address Offset	0x0000 0028		
Physical Address	0x4A00 9E28	**Instance**	RESTORE_CM2
Description	Second address map for register CM_C2C_STATICDEP. Used only by automatic restore upon wakeup from device OFF mode.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																		L4PER_STATDEP	L4CFG_STATDEP	RESERVED				L3INIT_STATDEP	L3_2_STATDEP	L3_1_STATDEP	MEMIF_STATDEP	ABE_STATDEP	IVAHD_STATDEP	RESERVED	

Bits	Field Name	Description	Type	Reset
31:14	RESERVED		R	0x00000
13	L4PER_STATDEP	Static dependency towards L4PER clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
12	L4CFG_STATDEP	Static dependency towards L4CFG clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
11:8	RESERVED		R	0x0
7	L3INIT_STATDEP	Static dependency towards L3INIT clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
6	L3_2_STATDEP	Static dependency towards L3_2 clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
5	L3_1_STATDEP	Static dependency towards L3_1 clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
4	MEMIF_STATDEP	Static dependency towards MEMIF clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	1
3	ABE_STATDEP	Static dependency towards ABE clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
2	IVAHD_STATDEP	Static dependency towards IVAHD clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
1:0	RESERVED		R	0x0

Table 3-1401. Register Call Summary for Register CM_C2C_STATICDEP_RESTORE

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- RESTORE_CM2 Register Summary: [0]

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Table 3-1402. CM_L3_1_DYNAMICDEP_RESTORE

Address Offset	0x0000 002C		
Physical Address	0x4A00 9E2C	**Instance**	RESTORE_CM2
Description	Second address map for register CM_L3_1_DYNAMICDEP. Used only by automatic restore upon wakeup from device OFF mode.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				WINDOWSIZE				RESERVED											L4CFG_DYNDEP	RESERVED						L3_2_DYNDEP	RESERVED	MEMIF_DYNDEP	ABE_DYNDEP	RESERVED		

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:24	WINDOWSIZE	Size of sliding window used to monitor OCP interface activity for determination of auto-sleep feature. Time unit defined by CM_DYN_DEP_PRESCAL register.	RW	0x4
23:13	RESERVED		R	0x000
12	L4CFG_DYNDEP	Dynamic dependency towards L4CFG clock domain Read 0x1: Dependency is enabled	R Rreturns 1s	1
11:7	RESERVED		R	0x00
6	L3_2_DYNDEP	Dynamic dependency towards L3_2 clock domain Read 0x1: Dependency is enabled	R Rreturns 1s	1
5	RESERVED		R	0
4	MEMIF_DYNDEP	Dynamic dependency towards MEMIF clock domain Read 0x1: Dependency is enabled	R Rreturns 1s	1
3	ABE_DYNDEP	Dynamic dependency towards ABE clock domain Read 0x1: Dependency is enabled	R Rreturns 1s	1
2:0	RESERVED		R	0x0

Table 3-1403. Register Call Summary for Register CM_L3_1_DYNAMICDEP_RESTORE

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- RESTORE_CM2 Register Summary: [0]

Table 3-1404. CM_L3_2_DYNAMICDEP_RESTORE

Address Offset	0x0000 0030		
Physical Address	0x4A00 9E30	**Instance**	RESTORE_CM2
Description	Second address map for register CM_L3_2_DYNAMICDEP. Used only by automatic restore upon wakeup from device OFF mode.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				WINDOWSIZE				RESERVED					C2C_DYNDEP	RESERVED		L4SEC_DYNDEP	L4PER_DYNDEP	RESERVED			GFX_DYNDEP	ISS_DYNDEP	DSS_DYNDEP	L3INIT_DYNDEP	RESERVED	L3_1_DYNDEP	RESERVED		IVAHD_DYNDEP	RESERVED	MPU_M3_DYNDEP

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:24	WINDOWSIZE	Size of sliding window used to monitor OCP interface activity for determination of auto-sleep feature. Time unit defined by CM_DYN_DEP_PRESCAL register.	RW	0x4
23:19	RESERVED		R	0x00
18	C2C_DYNDEP	Dynamic dependency towards D2D clock domain Read 0x1: Dependency is enabled	R Rreturns 1s	1
17:15	RESERVED		R	0x0
14	L4SEC_DYNDEP	Dynamic dependency towards L4SEC clock domain Read 0x1: Dependency is enabled	R Rreturns 1s	1
13	L4PER_DYNDEP	Dynamic dependency towards L4PER clock domain Read 0x1: Dependency is enabled	R Rreturns 1s	1
12:11	RESERVED		R	0x0
10	GFX_DYNDEP	Dynamic dependency towards GFX clock domain Read 0x1: Dependency is enabled	R Rreturns 1s	1
9	ISS_DYNDEP	Dynamic dependency towards ISS clock domain Read 0x0: Dependency is disabled	R	0
8	DSS_DYNDEP	Dynamic dependency towards DSS clock domain Read 0x1: Dependency is enabled	R Rreturns 1s	1
7	L3INIT_DYNDEP	Dynamic dependency towards L3INIT clock domain Read 0x1: Dependency is enabled	R Rreturns 1s	1
6	RESERVED		R	0
5	L3_1_DYNDEP	Dynamic dependency towards L3_1 clock domain Read 0x1: Dependency is enabled	R Rreturns 1s	1
4:3	RESERVED		R	0x0
2	IVAHD_DYNDEP	Dynamic dependency towards IVAHD clock domain Read 0x1: Dependency is enabled	R Rreturns 1s	1
1	RESERVED		R	0
0	MPU_M3_DYNDEP	Dynamic dependency towards CORTEXM3 clock domain Read 0x1: Dependency is enabled	R Rreturns 1s	1

Table 3-1405. Register Call Summary for Register CM_L3_2_DYNAMICDEP_RESTORE

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- RESTORE_CM2 Register Summary: [0]

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Table 3-1406. CM_C2C_DYNAMICDEP_RESTORE

Address Offset	0x0000 0034		
Physical Address	0x4A00 9E34	**Instance**	RESTORE_CM2
Description	Second address map for register CM_C2C_DYNAMICDEP. Used only by automatic restore upon wakeup from device OFF mode.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				WINDOWSIZE				RESERVED																	L3_2_DYNDEP	RESERVED	MEMIF_DYNDEP	RESERVED			

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:24	WINDOWSIZE	Size of sliding window used to monitor OCP interface activity for determination of auto-sleep feature. Time unit defined by CM_DYN_DEP_PRESCAL register.	RW	0x4
23:7	RESERVED		R	0x00000
6	L3_2_DYNDEP	Dynamic dependency towards L3_2 clock domain Read 0x1: Dependency is enabled	R Rreturns 1s	1
5	RESERVED		R	0
4	MEMIF_DYNDEP	Dynamic dependency towards MEMIF clock domain Read 0x1: Dependency is enabled	R Rreturns 1s	1
3:0	RESERVED		R	0x0

Table 3-1407. Register Call Summary for Register CM_C2C_DYNAMICDEP_RESTORE

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- RESTORE_CM2 Register Summary: [0]

Table 3-1408. CM_L4CFG_DYNAMICDEP_RESTORE

Address Offset	0x0000 0038		
Physical Address	0x4A00 9E38	**Instance**	RESTORE_CM2
Description	Second address map for register CM_L4CFG_DYNAMICDEP. Used only by automatic restore upon wakeup from device OFF mode.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				WINDOWSIZE				RESERVED				MPU_DYNDEP	C2C_DYNDEP	RESERVED	ALWONCORE_DYNDEP	L4WKUP_DYNDEP	RESERVED			SDMA_DYNDEP	RESERVED	ISS_DYNDEP	DSS_DYNDEP	L3INIT_DYNDEP	L3_2_DYNDEP	L3_1_DYNDEP	MEMIF_DYNDEP	RESERVED		DSP_DYNDEP	RESERVED

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Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:24	WINDOWSIZE	Size of sliding window used to monitor OCP interface activity for determination of auto-sleep feature. Time unit defined by CM_DYN_DEP_PRESCAL register.	RW	0x4
23:20	RESERVED		R	0x0
19	MPU_DYNDEP	Dynamic dependency towards MPU clock domain Read 0x1: Dependency is enabled	R Rreturns 1s	1
18	C2C_DYNDEP	Dynamic dependency towards D2D clock domain Read 0x1: Dependency is enabled	R Rreturns 1s	1
17	RESERVED		R	1
16	ALWONCORE_DYNDEP	Dynamic dependency towards ALWONCORE clock domain Read 0x1: Dependency is enabled	R Rreturns 1s	1
15	L4WKUP_DYNDEP	Dynamic dependency towards L4WKUP clock domain Read 0x1: Dependency is enabled	R Rreturns 1s	1
14:12	RESERVED		R	0x0
11	SDMA_DYNDEP	Dynamic dependency towards SDMA clock domain Read 0x1: Dependency is enabled	R Rreturns 1s	1
10	RESERVED		R	0
9	ISS_DYNDEP	Dynamic dependency towards ISS clock domain Read 0x0: Dependency is disabled	R	0
8	DSS_DYNDEP	Dynamic dependency towards DSS clock domain Read 0x1: Dependency is enabled	R Rreturns 1s	1
7	L3INIT_DYNDEP	Dynamic dependency towards L3INIT clock domain Read 0x1: Dependency is enabled	R Rreturns 1s	1
6	L3_2_DYNDEP	Dynamic dependency towards L3_2 clock domain Read 0x1: Dependency is enabled	R Rreturns 1s	1
5	L3_1_DYNDEP	Dynamic dependency towards L3_1 clock domain Read 0x1: Dependency is enabled	R Rreturns 1s	1
4	MEMIF_DYNDEP	Dynamic dependency towards MEMIF clock domain Read 0x1: Dependency is enabled	R Rreturns 1s	1
3:2	RESERVED		R	0x0
1	DSP_DYNDEP	Dynamic dependency towards DSP clock domain Read 0x1: Dependency is enabled	R Rreturns 1s	1
0	RESERVED		R	0

Table 3-1409. Register Call Summary for Register CM_L4CFG_DYNAMICDEP_RESTORE

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Table 3-1410. CM_L4PER_DYNAMICDEP_RESTORE

Address Offset	0x0000 003C		
Physical Address	0x4A00 9E3C	**Instance**	RESTORE_CM2
Description	Second address map for register CM_L4PER_DYNAMICDEP. Used only by automatic restore upon wakeup from device OFF mode.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				WINDOWSIZE				RESERVED									L4SEC_DYNDEP	RESERVED					DSS_DYNDEP	L3INIT_DYNDEP	RESERVED						

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:24	WINDOWSIZE	Size of sliding window used to monitor OCP interface activity for determination of auto-sleep feature. Time unit defined by CM_DYN_DEP_PRESCAL register.	RW	0x4
23:15	RESERVED		R	0x000
14	L4SEC_DYNDEP	Dynamic dependency towards L4SEC clock domain Read 0x1: Dependency is enabled	R Rreturns 1s	1
13:9	RESERVED		R	0x00
8	DSS_DYNDEP	Dynamic dependency towards DSS clock domain Read 0x1: Dependency is enabled	R Rreturns 1s	1
7	L3INIT_DYNDEP	Dynamic dependency towards L3INIT clock domain Read 0x1: Dependency is enabled	R Rreturns 1s	1
6:0	RESERVED		R	0x00

Table 3-1411. Register Call Summary for Register CM_L4PER_DYNAMICDEP_RESTORE

PRCM Register Manual

- RESTORE_CM2 Register Summary: [0]

Table 3-1412. CM_L4PER_GPIO2_CLKCTRL_RESTORE

Address Offset	0x0000 0040		
Physical Address	0x4A00 9E40	**Instance**	RESTORE_CM2
Description	Second address map for register CM_L4PER_GPIO2_CLKCTRL. Used only by automatic restore upon wakeup from device OFF mode.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED							OPTFCLKEN_DBCLK	RESERVED						MODULEMODE	

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Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:9	RESERVED		R	0x00
8	OPTFCLKEN_DBCLK	Optional functional clock control. 0x0: Optional functional clock is disabled 0x1: Optional functional clock is enabled	RW	0
7:2	RESERVED		R	0x00
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by software. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). 0x1: Module is managed automatically by hardware according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CLKTRCTRL=3, any INTRCONN access to module is always granted. Module clocks may be gated according to the clock domain state. Read 0x2: Reserved Read 0x3: Reserved	RW	0x0

Table 3-1413. Register Call Summary for Register CM_L4PER_GPIO2_CLKCTRL_RESTORE

Clock Management Functional Description • Clock Domain Module Attributes: [0]
PRCM Register Manual • RESTORE_CM2 Register Summary: [1]

Table 3-1414. CM_L4PER_GPIO3_CLKCTRL_RESTORE

Address Offset	0x0000 0044		
Physical Address	0x4A00 9E44	**Instance**	RESTORE_CM2
Description	Second address map for register CM_L4PER_GPIO3_CLKCTRL. Used only by automatic restore upon wakeup from device OFF mode.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED							OPTFCLKEN_DBCLK	RESERVED						MODULEMODE	

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Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:9	RESERVED		R	0x00
8	OPTFCLKEN_DBCLK	Optional functional clock control. 0x0: Optional functional clock is disabled 0x1: Optional functional clock is enabled	RW	0
7:2	RESERVED		R	0x00
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by software. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). 0x1: Module is managed automatically by hardware according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CLKTRCTRL=3, any INTRCONN access to module is always granted. Module clocks may be gated according to the clock domain state. Read 0x2: Reserved Read 0x3: Reserved	RW	0x0

Table 3-1415. Register Call Summary for Register CM_L4PER_GPIO3_CLKCTRL_RESTORE

Clock Management Functional Description • Clock Domain Module Attributes: [0]
PRCM Register Manual • RESTORE_CM2 Register Summary: [1]

Table 3-1416. CM_L4PER_GPIO4_CLKCTRL_RESTORE

Address Offset	0x0000 0048		
Physical Address	0x4A00 9E48	**Instance**	RESTORE_CM2
Description	Second address map for register CM_L4PER_GPIO4_CLKCTRL. Used only by automatic restore upon wakeup from device OFF mode.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED							OPTFCLKEN_DBCLK	RESERVED						MODULEMODE	

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Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:9	RESERVED		R	0x00
8	OPTFCLKEN_DBCLK	Optional functional clock control. 0x0: Optional functional clock is disabled 0x1: Optional functional clock is enabled	RW	0
7:2	RESERVED		R	0x00
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by software. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). 0x1: Module is managed automatically by hardware according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CLKTRCTRL=3, any INTRCONN access to module is always granted. Module clocks may be gated according to the clock domain state. Read 0x2: Reserved Read 0x3: Reserved	RW	0x0

Table 3-1417. Register Call Summary for Register CM_L4PER_GPIO4_CLKCTRL_RESTORE

Clock Management Functional Description • Clock Domain Module Attributes: [0]
PRCM Register Manual • RESTORE_CM2 Register Summary: [1]

Table 3-1418. CM_L4PER_GPIO5_CLKCTRL_RESTORE

Address Offset	0x0000 004C		
Physical Address	0x4A00 9E4C	**Instance**	RESTORE_CM2
Description	Second address map for register CM_L4PER_GPIO5_CLKCTRL. Used only by automatic restore upon wakeup from device OFF mode.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED							OPTFCLKEN_DBCLK	RESERVED						MODULEMODE	

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Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:9	RESERVED		R	0x00
8	OPTFCLKEN_DBCLK	Optional functional clock control. 0x0: Optional functional clock is disabled 0x1: Optional functional clock is enabled	RW	0
7:2	RESERVED		R	0x00
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by software. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). 0x1: Module is managed automatically by hardware according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CLKTRCTRL=3, any INTRCONN access to module is always granted. Module clocks may be gated according to the clock domain state. Read 0x2: Reserved Read 0x3: Reserved	RW	0x0

Table 3-1419. Register Call Summary for Register CM_L4PER_GPIO5_CLKCTRL_RESTORE

Clock Management Functional Description • Clock Domain Module Attributes: [0]
PRCM Register Manual • RESTORE_CM2 Register Summary: [1]

Table 3-1420. CM_L4PER_GPIO6_CLKCTRL_RESTORE

Address Offset	0x0000 0050		
Physical Address	0x4A00 9E50	**Instance**	RESTORE_CM2
Description	Second address map for register CM_L4PER_GPIO6_CLKCTRL. Used only by automatic restore upon wakeup from device OFF mode.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED							OPTFCLKEN_DBCLK	RESERVED						MODULEMODE	

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Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:9	RESERVED		R	0x00
8	OPTFCLKEN_DBCLK	Optional functional clock control. 0x0: Optional functional clock is disabled 0x1: Optional functional clock is enabled	RW	0
7:2	RESERVED		R	0x00
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by software. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). 0x1: Module is managed automatically by hardware according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CLKTRCTRL=3, any INTRCONN access to module is always granted. Module clocks may be gated according to the clock domain state. Read 0x2: Reserved Read 0x3: Reserved	RW	0x0

Table 3-1421. Register Call Summary for Register CM_L4PER_GPIO6_CLKCTRL_RESTORE

Clock Management Functional Description • Clock Domain Module Attributes: [0]
PRCM Register Manual • RESTORE_CM2 Register Summary: [1]

Table 3-1422. CM_L3INIT_HSUSBHOST_CLKCTRL_RESTORE

Address Offset	0x0000 0054		
Physical Address	0x4A00 9E54	**Instance**	RESTORE_CM2
Description	Second address map for register CM_L3INIT_USB_HOST_CLKCTRL. Used only by automatic restore upon wakeup from device OFF mode.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						CLKSEL_UTMI_P2	CLKSEL_UTMI_P1	RESERVED					STBYST	IDLEST		OPTFCLKEN_FUNC48MCLK	OPTFCLKEN_HSIC480M_P2_CLK	OPTFCLKEN_HSIC480M_P1_CLK	OPTFCLKEN_HSIC60M_P2_CLK	OPTFCLKEN_HSIC60M_P1_CLK	OPTFCLKEN_UTMI_P3_CLK	OPTFCLKEN_UTMI_P2_CLK	OPTFCLKEN_UTMI_P1_CLK	RESERVED			SAR_MODE	RESERVED		MODULEMODE	

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Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x00
25	CLKSEL_UTMI_P2	Selects the source of the functional clock for UTMI Port2 on USB Host 0x0: The functional clock is provided by the internal clock source 0x1: The functional clock is provided by an external PHY through an I/O pad.	RW	0
24	CLKSEL_UTMI_P1	Selects the source of the functional clock for UTMI Por1 on USB Host 0x0: The functional clock is provided by the internal clock source 0x1: The functional clock is provided by an external PHY through an I/O pad.	RW	0
23:19	RESERVED		R	0x00
18	STBYST	Module standby status. [warm reset insensitive] Read 0x0: Module is functional (not in standby) Read 0x1: Module is in standby	R	1
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15	OPTFCLKEN_FUNC48MCLK	USB-HOST optional clock control: FUNC48MCLK 0x0: Optional functional clock is disabled 0x1: Optional functional clock is enabled	RW	0
14	OPTFCLKEN_HSIC480M_P2_CLK	USB-HOST optional clock control: HSIC480M_P2_CLK 0x0: Optional functional clock is disabled 0x1: Optional functional clock is enabled	RW	0
13	OPTFCLKEN_HSIC480M_P1_CLK	USB-HOST optional clock control: HSIC480M_P1_CLK 0x0: Optional functional clock is disabled 0x1: Optional functional clock is enabled	RW	0
12	OPTFCLKEN_HSIC60M_P2_CLK	USB-HOST optional clock control: HSIC60M_P2_CLK 0x0: Optional functional clock is disabled 0x1: Optional functional clock is enabled	RW	0
11	OPTFCLKEN_HSIC60M_P1_CLK	USB-HOST optional clock control: HSIC60M_P1_CLK 0x0: Optional functional clock is disabled 0x1: Optional functional clock is enabled	RW	0
10	OPTFCLKEN_UTMI_P3_CLK	USB-HOST optional clock control: UTMI_P3_CLK 0x0: Optional functional clock is disabled 0x1: Optional functional clock is enabled	RW	0
9	OPTFCLKEN_UTMI_P2_CLK	USB-HOST optional clock control: UTMI_P2_CLK when CLKSEL_UTMI_P2 is 0 0x0: Optional functional clock is disabled 0x1: Optional functional clock is enabled	RW	0
8	OPTFCLKEN_UTMI_P1_CLK	USB-HOST optional clock control: UTMI_P1_CLK when CLKSEL_UTMI_P1 is 0 0x0: Optional functional clock is disabled 0x1: Optional functional clock is enabled	RW	0
7:5	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
4	SAR_MODE	SAR mode control for the module. Shall not be modify except if module is disabled. 0x0: SAR mode is disabled 0x1: SAR mode is enabled	RW	0
3:2	RESERVED		R	0x0
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by software. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen. Read 0x3: Reserved	RW	0x0

Table 3-1423. Register Call Summary for Register CM_L3INIT_HSUSBHOST_CLKCTRL_RESTORE

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • RESTORE_CM2 Register Summary: [2]

Table 3-1424. CM_L3INIT_HSUSBTLL_CLKCTRL_RESTORE

Address Offset	0x0000 0058		
Physical Address	0x4A00 9E58	**Instance**	RESTORE_CM2
Description	Second address map for register CM_L3INIT_HSUSBTLL_CLKCTRL. Used only by automatic restore upon wakeup from device OFF mode.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED						OPTFCLKEN_USB_CH1_CLK	OPTFCLKEN_USB_CH0_CLK	RESERVED			SAR_MODE	RESERVED		MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:10	RESERVED		R	0x00

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Bits	Field Name	Description	Type	Reset
9	OPTFCLKEN_USB_CH1_CLK	USB-HOST optional clock control: USB_CH1_CLK 0x0: Optional functional clock is disabled 0x1: Optional functional clock is enabled	RW	0
8	OPTFCLKEN_USB_CH0_CLK	USB-HOST optional clock control: USB_CH0_CLK 0x0: Optional functional clock is disabled 0x1: Optional functional clock is enabled	RW	0
7:5	RESERVED		R	0x0
4	SAR_MODE	SAR mode control for the module. Shall not be modify except if module is disabled. 0x0: SAR mode is disabled 0x1: SAR mode is enabled	RW	0
3:2	RESERVED		R	0x0
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by software. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). 0x1: Module is managed automatically by hardware according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CLKTRCTRL=3, any INTRCONN access to module is always granted. Module clocks may be gated according to the clock domain state. Read 0x2: Reserved Read 0x3: Reserved	RW	0x0

Table 3-1425. Register Call Summary for Register CM_L3INIT_HSUSBTLL_CLKCTRL_RESTORE

Clock Management Functional Description • Clock Domain Module Attributes: [0]
PRCM Register Manual • RESTORE_CM2 Register Summary: [1]

Table 3-1426. CM_SDMA_STATICDEP_RESTORE

Address Offset	0x0000 005C		
Physical Address	0x4A00 9E5C	**Instance**	RESTORE_CM2
Description	Second address map for register CM_SDMA_STATICDEP. Used only by automatic restore upon wakeup from device OFF mode.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																L4WKUP_STATDEP	RESERVED	L4PER_STATDEP	L4CFG_STATDEP	RESERVED		ISS_STATDEP	DSS_STATDEP	L3INIT_STATDEP	L3_2_STATDEP	L3_1_STATDEP	MEMIF_STATDEP	ABE_STATDEP	IVAHD_STATDEP	RESERVED	MPU_M3_STATDEP

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15	L4WKUP_STATDEP	Static dependency towards L4WKUP clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	1

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Bits	Field Name	Description	Type	Reset
14	RESERVED		RW	0
13	L4PER_STATDEP	Static dependency towards L4PER clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
12	L4CFG_STATDEP	Static dependency towards L4CFG clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	1
11:10	RESERVED		R	0x0
9	ISS_STATDEP	Static dependency towards ISS clock domain Read 0x0: Dependency is disabled	R	0
8	DSS_STATDEP	Static dependency towards DSS clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
7	L3INIT_STATDEP	Static dependency towards L3INIT clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
6	L3_2_STATDEP	Static dependency towards L3_2 clock domain Read 0x1: Dependency is enabled	R Rreturns 1s	1
5	L3_1_STATDEP	Static dependency towards L3_1 clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	1
4	MEMIF_STATDEP	Static dependency towards MEMIF clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	1
3	ABE_STATDEP	Static dependency towards ABE clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
2	IVAHD_STATDEP	Static dependency towards IVAHD clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
1	RESERVED		R	0
0	MPU_M3_STATDEP	Static dependency towards MPU_A3 clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-1427. Register Call Summary for Register CM_SDMA_STATICDEP_RESTORE

PRCM Register Manual
- RESTORE_CM2 Register Summary: [0]

3.11.41 INSTR_CM2 Registers

3.11.41.1 INSTR_CM2 Register Summary

Table 3-1428. INSTR_CM2 Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	INSTR_CM2 Base Address
CMI2_IDENTICATION	R	32	0x0000 0000	0x4A00 9F00

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Table 3-1428. INSTR_CM2 Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	INSTR_CM2 Base Address
CMI2_SYS_CONFIG	RW	32	0x0000 0010	0x4A00 9F10
CMI2_STATUS	R	32	0x0000 0014	0x4A00 9F14
CMI2_CONFIGURATION	RW	32	0x0000 0024	0x4A00 9F24
CMI2_CLASS_FILTERING	RW	32	0x0000 0028	0x4A00 9F28
CMI2_TRIGGERING	RW	32	0x0000 002C	0x4A00 9F2C
CMI2_SAMPLING	RW	32	0x0000 0030	0x4A00 9F30

3.11.41.2 INSTR_CM2 Register Description

Table 3-1429. CMI2_IDENTICATION

Address Offset	0x0000 0000		
Physical Address	0x4A00 9F00	**Instance**	INSTR_CM2
Description	CM profiling identification register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP revision	R	0x-- TI Internal data.

Table 3-1430. Register Call Summary for Register CMI2_IDENTICATION

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- INSTR_CM2 Register Summary: [0]

Table 3-1431. CMI2_SYS_CONFIG

Address Offset	0x0000 0010		
Physical Address	0x4A00 9F10	**Instance**	INSTR_CM2
Description	CM profiling system configuartion register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RESERVED				IDLEMODE		RESERVED	SOFTRESET

Bits	Field Name	Description	Type	Reset
31:6	RESERVED	Reserved	R	0x0000000
5:4	RESERVED	Reserved	R	0x0
3:2	IDLEMODE	Configuration of the local tartget state management mode	RW	0x2
1	RESERVED	Reserved	R	0
0	SOFTRESET	Software reset	RW	0

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Table 3-1432. Register Call Summary for Register CMI2_SYS_CONFIG

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- INSTR_CM2 Register Summary: [0]

Table 3-1433. CMI2_STATUS

Address Offset	0x0000 0014		
Physical Address	0x4A00 9F14	**Instance**	INSTR_CM2
Description	CM profiling status register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							FIFOEMPTY	RESERVED							

Bits	Field Name	Description	Type	Reset
31:9	RESERVED	Reserved	R	0x000000
8	FIFOEMPTY	PM Profiling buffer empty	R	1
7:0	RESERVED	Reserved	R	0x00

Table 3-1434. Register Call Summary for Register CMI2_STATUS

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- INSTR_CM2 Register Summary: [0]

Table 3-1435. CMI2_CONFIGURATION

Address Offset	0x0000 0024		
Physical Address	0x4A00 9F24	**Instance**	INSTR_CM2
Description	CM profiling configuration register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLAIM_3		CLAIM_2	CLAIM_1	RESERVED				RESERVED	RESERVED							RESERVED	RESERVED							EVT_CAPT_EN	RESERVED						

Bits	Field Name	Description	Type	Reset
31:30	CLAIM_3	Ownership	RW	0x0
29	CLAIM_2	Debugger override qualifier	RW	1
28	CLAIM_1	Current owner	R	0
27:24	RESERVED	Reserved	R	0x0
23	RESERVED	Reserved	R	0
22:16	RESERVED	Reserved	R	0x00
15	RESERVED	Reserved	R	0
14:8	RESERVED	Reserved	R	0x00
7	EVT_CAPT_EN	When HIGH the PM events capture is enabled	RW	0

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Bits	Field Name	Description	Type	Reset
6:0	RESERVED	Reserved	R	0x00

Table 3-1436. Register Call Summary for Register CMI2_CONFIGURATION

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- INSTR_CM2 Register Summary: [0]

Table 3-1437. CMI2_CLASS_FILTERING

Address Offset	0x0000 0028		
Physical Address	0x4A00 9F28	**Instance**	INSTR_CM2
Description	CM profiling class filtering register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												SNAP_CAPT_EN_03	SNAP_CAPT_EN_02	SNAP_CAPT_EN_01	SNAP_CAPT_EN_00

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved	R	0x0000000
3	SNAP_CAPT_EN_03	Snapshot capture enable - Class-ID = 0x03	RW	0
2	SNAP_CAPT_EN_02	Snapshot capture enable - Class-ID = 0x02	RW	0
1	SNAP_CAPT_EN_01	Snapshot capture enable - Class-ID = 0x01	RW	0
0	SNAP_CAPT_EN_00	Snapshot capture enable - Class-ID = 0x00	RW	0

Table 3-1438. Register Call Summary for Register CMI2_CLASS_FILTERING

PRCM Register Manual
- INSTR_CM2 Register Summary: [0]

Table 3-1439. CMI2_TRIGGERING

Address Offset	0x0000 002C		
Physical Address	0x4A00 9F2C	**Instance**	INSTR_CM2
Description	CM profiling triggering control register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														TRIG_STOP_EN	TRIG_START_EN

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Bits	Field Name	Description	Type	Reset
31:2	RESERVED	Reserved	R	0x0000 0000
1	TRIG_STOP_EN	Enable stop capturing PM events from external trigger detection	RW	0
0	TRIG_START_EN	Enable start capturing PM events from external trigger detection	RW	0

Table 3-1440. Register Call Summary for Register CMI2_TRIGGERING

PRCM Register Manual
- INSTR_CM2 Register Summary: [0]

Table 3-1441. CMI2_SAMPLING

Address Offset	0x0000 0030		
Physical Address	0x4A00 9F30	**Instance**	INSTR_CM2
Description	CM profiling sampling window register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												FCLK_DIV_FACOR				RESERVED								SAMP_WIND_SIZE							

Bits	Field Name	Description	Type	Reset
31:20	RESERVED	Reserved	R	0x000
19:16	FCLK_DIV_FACOR	FunClk divide factor ranging from 1 to 16	RW	0x0
15:8	RESERVED	Reserved	R	0x00
7:0	SAMP_WIND_SIZE	PM events sampling window size	RW	0x00

Table 3-1442. Register Call Summary for Register CMI2_SAMPLING

PRCM Register Manual
- INSTR_CM2 Register Summary: [0]

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3.12 SCRM Register Manual

3.12.1 SCRM Instance Summary

Table 3-1443. SCRM Instance Summary

Module Name	L4 Base Address	Size
SCRM	0x4A30 A000	256Bytes

3.12.2 SCRM Registers

3.12.2.1 SCRM Register Summary

Table 3-1444. SCRM Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	SCRM L4 Base Address
REVISION_SCRM	R	32	0x0000 0000	0x4A30 A000
CLKSETUPTIME	RW	32	0x0000 0100	0x4A30 A100
PMICSETUPTIME	RW	32	0x0000 0104	0x4A30 A104
ALTCLKSRC	RW	32	0x0000 0110	0x4A30 A110
RESERVED	RW	32	0x0000 0118	0x4A30 A118
C2CCLKM	RW	32	0x0000 011C	0x4A30 A11C
EXTCLKREQ	RW	32	0x0000 0200	0x4A30 A200
ACCCLKREQ	RW	32	0x0000 0204	0x4A30 A204
PWRREQ	RW	32	0x0000 0208	0x4A30 A208
AUXCLKREQ0	RW	32	0x0000 0210	0x4A30 A210
AUXCLKREQ1	RW	32	0x0000 0214	0x4A30 A214
AUXCLKREQ2	RW	32	0x0000 0218	0x4A30 A218
AUXCLKREQ3	RW	32	0x0000 021C	0x4A30 A21C
AUXCLKREQ4	RW	32	0x0000 0220	0x4A30 A220
AUXCLKREQ5	RW	32	0x0000 0224	0x4A30 A224
C2CCLKREQ	RW	32	0x0000 0234	0x4A30 A234
AUXCLK0	RW	32	0x0000 0310	0x4A30 A310
AUXCLK1	RW	32	0x0000 0314	0x4A30 A314
AUXCLK2	RW	32	0x0000 0318	0x4A30 A318
AUXCLK3	RW	32	0x0000 031C	0x4A30 A31C
AUXCLK4	RW	32	0x0000 0320	0x4A30 A320
AUXCLK5	RW	32	0x0000 0324	0x4A30 A324
RSTTIME_REG	RW	32	0x0000 0400	0x4A30 A400
RESERVED	RW	32	0x0000 0418	0x4A30 A418
C2CRSTCTRL	RW	32	0x0000 041C	0x4A30 A41C
EXTPWRONRSTCTRL	RW	32	0x0000 0420	0x4A30 A420
RESERVED	RW	32	0x0000 0500	0x4A30 A500
RESERVED	RW	32	0x0000 0504	0x4A30 A504
RESERVED	RW	32	0x0000 0508	0x4A30 A508
RESERVED	RW	32	0x0000 050C	0x4A30 A50C
EXTWARMRSTST_REG	RW	32	0x0000 0510	0x4A30 A510
APEWARMRSTST_REG	RW	32	0x0000 0514	0x4A30 A514
RESERVED	RW	32	0x0000 0518	0x4A30 A518
C2CWARMRSTST_REG	RW	32	0x0000 051C	0x4A30 A51C

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3.12.2.2 SCRM Register Description

Table 3-1445. REVISION_SCRM

Address Offset	0x0000 0000		
Physical Address	0x4A30 A000	**Instance**	SCRM
Description	This register contains the IP revision code for the SCRM.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								REV							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Reads returns 0.	R	0x000000
7:0	REV	Revision Number	R	0x- - TI Internal data.

Table 3-1446. Register Call Summary for Register REVISION_SCRM

SCRM Register Manual

- SCRM Register Summary: [0]

Table 3-1447. CLKSETUPTIME

Address Offset	0x0000 0100		
Physical Address	0x4A30 A100	**Instance**	SCRM
Description	This register holds the clock setup time counters of the system clock source supplier.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								DOWNTIME								RESERVED				SETUPTIME											

Bits	Field Name	Description	Type	Reset
31:22	RESERVED	Reads returns 0.	R	0x000
21:16	DOWNTIME	Holds the number of 32 kHz clock cycles it takes to gate the clock source supplier.	RW	0x00
15:12	RESERVED	Reads returns 0.	R	0x0
11:0	SETUPTIME	Holds the number of 32 kHz clock cycles it takes to stabilize the clock source supplier.	RW	0x000

Table 3-1448. Register Call Summary for Register CLKSETUPTIME

SCRM Register Manual

- SCRM Register Summary: [0]

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Table 3-1449. PMICSETUPTIME

Address Offset	0x0000 0104		
Physical Address	0x4A30 A104	**Instance**	SCRM
Description	This register holds the setup time counters for the sleep mode of the PMIC.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								WAKEUPTIME								RESERVED								SLEEPTIME							

Bits	Field Name	Description	Type	Reset
31:22	RESERVED	Reads returns 0.	R	0x000
21:16	WAKEUPTIME	Holds the number of 32 kHz clock cycles it takes to exit the PMIC from sleep mode.	RW	0x00
15:6	RESERVED	Reads returns 0.	R	0x000
5:0	SLEEPTIME	Holds the number of 32 kHz clock cycles it takes to enter the PMIC in sleep mode.	RW	0x00

Table 3-1450. Register Call Summary for Register PMICSETUPTIME

SCRM Register Manual

- SCRM Register Summary: [0]

Table 3-1451. ALTCLKSRC

Address Offset	0x0000 0110		
Physical Address	0x4A30 A110	**Instance**	SCRM
Description	This register controls the alternate system clock source supplier.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												ENABLE_EXT	ENABLE_INT	MODE	

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reads returns 0.	R	0x0000000
3	ENABLE_EXT	This bit allows to enable and disable the output alternate system clock version. This bit is intended to be used in order to gate this clock path while the source is stabilizing. 0x0: The alternate system clock version is disabled. 0x1: The alternate system clock version is enabled.	RW	0
2	ENABLE_INT	This bit allows to enable and disable the alternate system clock version used to generate the auxiliary clocks. This bit is intended to be used in order to gate this clock path while the source is stabilizing and also to gate this clock path while switching the auxiliary clock paths on / from this possible source. 0x0: The alternate system clock version is disabled. 0x1: The alternate system clock version is enabled.	RW	0

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Bits	Field Name	Description	Type	Reset
1:0	MODE	This bit field defines the functional mode of the alternate system clock supplier. 0x0: The alternate system clock source supplier is powered-down. 0x1: The alternate system clock source supplier is active. 0x2: The alternate system clock source supplier is bypassed. 0x3: Reserved	RW	0x0

Table 3-1452. Register Call Summary for Register ALTCLKSRC

Clock Management Functional Description • Clock Domain Module Attributes: [0]
SCRM Register Manual • SCRM Register Summary: [1]

Table 3-1453. C2CCLKM

Address Offset	0x0000 011C		
Physical Address	0x4A30 A11C	**Instance**	SCRM
Description	This register controls the clocks of the external C2C interface.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														SYSCLK	CLK_32KHZ

Bits	Field Name	Description	Type	Reset
31:2	RESERVED	Reads returns 0.	R	0x0000 0000
1	SYSCLK	This bit allows to enable and disable the system clock version of the external C2C interface. 0x0: The system clock version for the external C2C interface is disabled. 0x1: The system clock version for the external C2C interface is enabled.	RW	0
0	CLK_32KHZ	This bit allows to enable and disable the 32 kHz clock version of the external C2C interface. 0x0: The 32 kHz clock version for the external C2C interface is disabled. 0x1: The 32 kHz clock version for the external C2C interface is enabled.	RW	0

Table 3-1454. Register Call Summary for Register C2CCLKM

SCRM Register Manual • SCRM Register Summary: [0]

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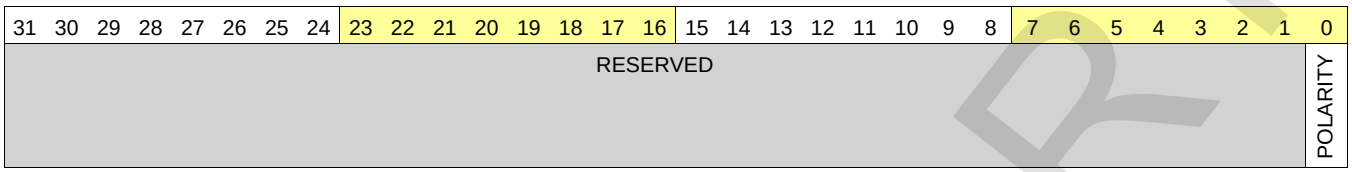
Table 3-1455. EXTCLKREQ

Address Offset	0x0000 0200		
Physical Address	0x4A30 A200	**Instance**	SCRM
Description	This register holds qualifiers for the external clock request.		
Type	RW		



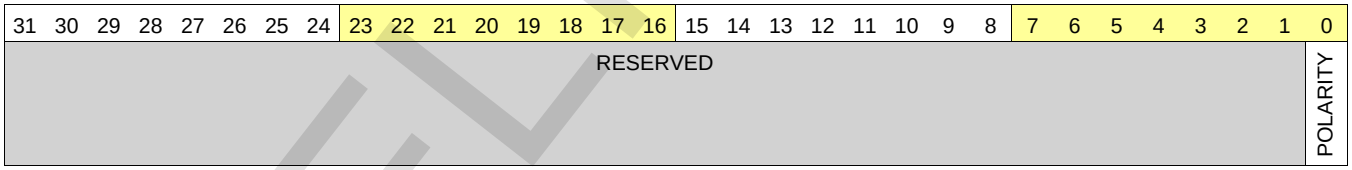
Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reads returns 0.	R	0x0000 0000
0	POLARITY	This bit defines the active level of the external clock request. 0x0: The external clock request is active low. 0x1: The external clock request is active high.	RW	1

Table 3-1456. Register Call Summary for Register EXTCLKREQ

SCRM Register Manual
- SCRM Register Summary: [0]

Table 3-1457. ACCCLKREQ

Address Offset	0x0000 0204		
Physical Address	0x4A30 A204	**Instance**	SCRM
Description	This register holds qualifiers for the accurate clock request.		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reads returns 0.	R	0x0000 0000
0	POLARITY	This bit defines the active level of the accurate clock request. 0x0: The accurate clock request is active low. 0x1: The accurate clock request is active high.	RW	1

Table 3-1458. Register Call Summary for Register ACCCLKREQ

SCRM Register Manual
- SCRM Register Summary: [0]

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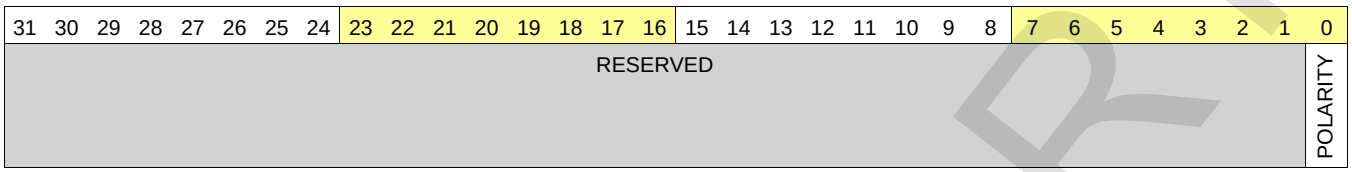
Table 3-1459. PWRREQ

Address Offset	0x0000 0208		
Physical Address	0x4A30 A208	**Instance**	SCRM
Description	This register holds qualifiers for the external power request.		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reads returns 0.	R	0x0000 0000
0	POLARITY	This bit defines the active level of the external power request. 0x0: The external power request is active low. 0x1: The external power request is active high.	RW	1

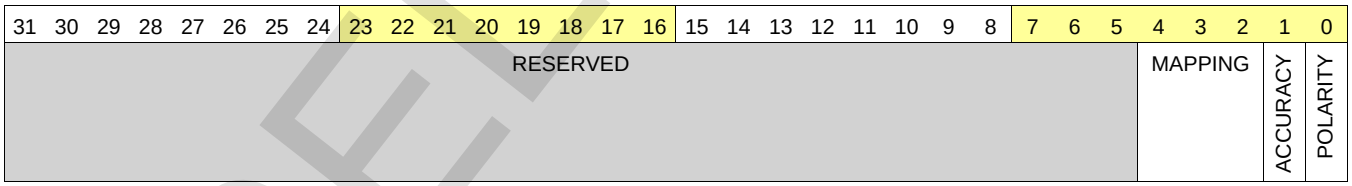
Table 3-1460. Register Call Summary for Register PWRREQ

PRCM Register Manual
- DEVICE_PRM Register Description: [0] [1] [2] [3] [4] [5] [6] [7] [8]

SCRM Register Manual
- SCRM Register Summary: [9]

Table 3-1461. AUXCLKREQ0

Address Offset	0x0000 0210		
Physical Address	0x4A30 A210	**Instance**	SCRM
Description	This register holds qualifiers for the auxiliary clock request #0.		
Type	RW		



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Bits	Field Name	Description	Type	Reset
31:5	RESERVED		R	0x0000000
4:2	MAPPING	This field allows re-mapping the auxiliary clock request #0 on another auxiliary clock output than auxiliary clock #0. 0x0: The auxiliary clock request #0 is mapped on the auxiliary clock #0. 0x1: The auxiliary clock request #0 is mapped on the auxiliary clock #1. 0x2: The auxiliary clock request #0 is mapped on the auxiliary clock #2. 0x3: The auxiliary clock request #0 is mapped on the auxiliary clock #3. 0x4: The auxiliary clock request #0 is mapped on the auxiliary clock #4. 0x5: The auxiliary clock request #0 is mapped on the auxiliary clock #5. 0x6: Reserved 0x7: Reserved	RW	0x0
1	ACCURACY	This bit qualifies the auxiliary clock request #0 as an accurate clock request. 0x0: An active auxiliary clock request #0 doesn't generate an accurate clock request. 0x1: An active auxiliary clock request #0 generates an accurate clock request.	RW	0
0	POLARITY	This bit defines the active level of the auxiliary clock request #0. 0x0: The auxiliary clock request #0 is active low. 0x1: The auxiliary clock request #0 is active high.	RW	1

Table 3-1462. Register Call Summary for Register AUXCLKREQ0

PRCM Subsystem Environment • External Clock Signals: [0]
SCRM Register Manual • SCRM Register Summary: [1]

Table 3-1463. AUXCLKREQ1

Address Offset	0x0000 0214		
Physical Address	0x4A30 A214	**Instance**	SCRM
Description	This register holds qualifiers for the auxiliary clock request #1.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																											MAPPING			ACCURACY	POLARITY

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Bits	Field Name	Description	Type	Reset
31:5	RESERVED	Reads returns 0.	R	0x0000000
4:2	MAPPING	This field allows re-mapping the auxiliary clock request #1 on another auxiliary clock output than auxiliary clock #1. 0x0: The auxiliary clock request #1 is mapped on the auxiliary clock #0. 0x1: The auxiliary clock request #1 is mapped on the auxiliary clock #1. 0x2: The auxiliary clock request #1 is mapped on the auxiliary clock #2. 0x3: The auxiliary clock request #1 is mapped on the auxiliary clock #3. 0x4: The auxiliary clock request #1 is mapped on the auxiliary clock #4. 0x5: The auxiliary clock request #1 is mapped on the auxiliary clock #5. 0x6: Reserved 0x7: Reserved	RW	0x1
1	ACCURACY	This bit qualifies the auxiliary clock request #1 as an accurate clock request. 0x0: An active auxiliary clock request #1 doesn't generate an accurate clock request. 0x1: An active auxiliary clock request #1 generates an accurate clock request.	RW	0
0	POLARITY	This bit defines the active level of the auxiliary clock request #1. 0x0: The auxiliary clock request #1 is active low. 0x1: The auxiliary clock request #1 is active high.	RW	1

Table 3-1464. Register Call Summary for Register AUXCLKREQ1

SCRM Register Manual
- SCRM Register Summary: [0]

Table 3-1465. AUXCLKREQ2

Address Offset	0x0000 0218		
Physical Address	0x4A30 A218	**Instance**	SCRM
Description	This register holds qualifiers for the auxiliary clock request #2.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																											MAPPING			ACCURACY	POLARITY

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Bits	Field Name	Description	Type	Reset
31:5	RESERVED	Reads returns 0.	R	0x0000000
4:2	MAPPING	This field allows re-mapping the auxiliary clock request #2 on another auxiliary clock output than auxiliary clock #2. 0x0: The auxiliary clock request #2 is mapped on the auxiliary clock #0. 0x1: The auxiliary clock request #2 is mapped on the auxiliary clock #1. 0x2: The auxiliary clock request #2 is mapped on the auxiliary clock #2. 0x3: The auxiliary clock request #2 is mapped on the auxiliary clock #3. 0x4: The auxiliary clock request #2 is mapped on the auxiliary clock #4. 0x5: The auxiliary clock request #2 is mapped on the auxiliary clock #5. 0x6: Reserved 0x7: Reserved	RW	0x2
1	ACCURACY	This bit qualifies the auxiliary clock request #2 as an accurate clock request. 0x0: An active auxiliary clock request #2 doesn't generate an accurate clock request. 0x1: An active auxiliary clock request #2 generates an accurate clock request.	RW	0
0	POLARITY	This bit defines the active level of the auxiliary clock request #2. 0x0: The auxiliary clock request #2 is active low. 0x1: The auxiliary clock request #2 is active high.	RW	1

Table 3-1466. Register Call Summary for Register AUXCLKREQ2

SCRM Register Manual
- SCRM Register Summary: [0]

Table 3-1467. AUXCLKREQ3

Address Offset	0x0000 021C		
Physical Address	0x4A30 A21C	**Instance**	SCRM
Description	This register holds qualifiers for the auxiliary clock request #3.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																											MAPPING			ACCURACY	POLARITY

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Bits	Field Name	Description	Type	Reset
31:5	RESERVED	Reads returns 0.	R	0x0000000
4:2	MAPPING	This field allows re-mapping the auxiliary clock request #3 on another auxiliary clock output than auxiliary clock #3. 0x0: The auxiliary clock request #3 is mapped on the auxiliary clock #0. 0x1: The auxiliary clock request #3 is mapped on the auxiliary clock #1. 0x2: The auxiliary clock request #3 is mapped on the auxiliary clock #2. 0x3: The auxiliary clock request #3 is mapped on the auxiliary clock #3. 0x4: The auxiliary clock request #3 is mapped on the auxiliary clock #4. 0x5: The auxiliary clock request #3 is mapped on the auxiliary clock #5. 0x6: Reserved 0x7: Reserved	RW	0x3
1	ACCURACY	This bit qualifies the auxiliary clock request #3 as an accurate clock request. 0x0: An active auxiliary clock request #3 doesn't generate an accurate clock request. 0x1: An active auxiliary clock request #3 generates an accurate clock request.	RW	0
0	POLARITY	This bit defines the active level of the auxiliary clock request #3. 0x0: The auxiliary clock request #3 is active low. 0x1: The auxiliary clock request #3 is active high.	RW	1

Table 3-1468. Register Call Summary for Register AUXCLKREQ3

SCRM Register Manual
- SCRM Register Summary: [0]

Table 3-1469. AUXCLKREQ4

Address Offset	0x0000 0220		
Physical Address	0x4A30 A220	**Instance**	SCRM
Description	This register holds qualifiers for the auxiliary clock request #4.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																											MAPPING			ACCURACY	POLARITY

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Bits	Field Name	Description	Type	Reset
31:5	RESERVED	Reads returns 0.	R	0x0000000
4:2	MAPPING	This field allows re-mapping the auxiliary clock request #4 on another auxiliary clock output than auxiliary clock #4. 0x0: The auxiliary clock request #4 is mapped on the auxiliary clock #0. 0x1: The auxiliary clock request #4 is mapped on the auxiliary clock #1. 0x2: The auxiliary clock request #4 is mapped on the auxiliary clock #2. 0x3: The auxiliary clock request #4 is mapped on the auxiliary clock #3. 0x4: The auxiliary clock request #4 is mapped on the auxiliary clock #4. 0x5: The auxiliary clock request #4 is mapped on the auxiliary clock #5. 0x6: Reserved 0x7: Reserved	RW	0x4
1	ACCURACY	This bit qualifies the auxiliary clock request #4 as an accurate clock request. 0x0: An active auxiliary clock request #4 doesn't generate an accurate clock request. 0x1: An active auxiliary clock request #4 generates an accurate clock request.	RW	0
0	POLARITY	This bit defines the active level of the auxiliary clock request #4. 0x0: The auxiliary clock request #4 is active low. 0x1: The auxiliary clock request #4 is active high.	RW	1

Table 3-1470. Register Call Summary for Register AUXCLKREQ4

SCRM Register Manual
- SCRM Register Summary: [0]

Table 3-1471. AUXCLKREQ5

Address Offset	0x0000 0224		
Physical Address	0x4A30 A224	**Instance**	SCRM
Description	This register holds qualifiers for the auxiliary clock request #5.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																											MAPPING			ACCURACY	POLARITY

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Bits	Field Name	Description	Type	Reset
31:5	RESERVED	Reads returns 0.	R	0x0000000
4:2	MAPPING	This field allows re-mapping the auxiliary clock request #5 on another auxiliary clock output than auxiliary clock #5. 0x0: The auxiliary clock request #5 is mapped on the auxiliary clock #0. 0x1: The auxiliary clock request #5 is mapped on the auxiliary clock #1. 0x2: The auxiliary clock request #5 is mapped on the auxiliary clock #2. 0x3: The auxiliary clock request #5 is mapped on the auxiliary clock #3. 0x4: The auxiliary clock request #5 is mapped on the auxiliary clock #4. 0x5: The auxiliary clock request #5 is mapped on the auxiliary clock #5. 0x6: Reserved 0x7: Reserved	RW	0x5
1	ACCURACY	This bit qualifies the auxiliary clock request #5 as an accurate clock request. 0x0: An active auxiliary clock request #5 doesn't generate an accurate clock request. 0x1: An active auxiliary clock request #5 generates an accurate clock request.	RW	0
0	POLARITY	This bit defines the active level of the auxiliary clock request #5. 0x0: The auxiliary clock request #5 is active low. 0x1: The auxiliary clock request #5 is active high.	RW	1

Table 3-1472. Register Call Summary for Register AUXCLKREQ5

SCRM Register Manual
- SCRM Register Summary: [0]

Table 3-1473. C2CCLKREQ

Address Offset	0x0000 0234		
Physical Address	0x4A30 A234	**Instance**	SCRM
Description	This register holds qualifiers for the external C2C interface clock request.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														ACCURACY	POLARITY

Bits	Field Name	Description	Type	Reset
31:2	RESERVED	Reads returns 0.	R	0x0000 0000
1	ACCURACY	This bit qualifies the external C2C interface clock request as an accurate clock request. 0x0: An active external C2C interface clock request doesn't generate an accurate clock request. 0x1: An active external C2C interface clock request generates an accurate clock request.	RW	0

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Bits	Field Name	Description	Type	Reset
0	POLARITY	This bit defines the active level of the external C2C interface clock request. 0x0: The external C2C interface clock request is active low. 0x1: The external C2C interface clock request is active high.	RW	1

Table 3-1474. Register Call Summary for Register C2CCLKREQ

SCRM Register Manual

- SCRM Register Summary: [0]

Table 3-1475. AUXCLK0

Address Offset	0x0000 0310		
Physical Address	0x4A30 A310	**Instance**	SCRM
Description	This register holds qualifiers for the auxiliary clock #0.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								CLKDIV								RESERVED						DISABLECLK	ENABLE	RESERVED					SRCSELECT		POLARITY

Bits	Field Name	Description	Type	Reset
31:20	RESERVED	Reads returns 0.	R	0x000
19:16	CLKDIV	This field holds the divider value for the auxiliary clock #0. 0x0: The auxiliary clock #0 is divided by 1. 0x1: The auxiliary clock #0 is divided by 2. 0x2: The auxiliary clock #0 is divided by 3. 0x3: The auxiliary clock #0 is divided by 4. 0x4: The auxiliary clock #0 is divided by 5. 0x5: The auxiliary clock #0 is divided by 6. 0x6: The auxiliary clock #0 is divided by 7. 0x7: The auxiliary clock #0 is divided by 8. 0x8: The auxiliary clock #0 is divided by 9. 0x9: The auxiliary clock #0 is divided by 10. 0xA: The auxiliary clock #0 is divided by 11. 0xB: The auxiliary clock #0 is divided by 12. 0xC: The auxiliary clock #0 is divided by 13. 0xD: The auxiliary clock #0 is divided by 14. 0xE: The auxiliary clock #0 is divided by 15. 0xF: The auxiliary clock #0 is divided by 16.	RW	0x0
15:10	RESERVED	Reads returns 0.	R	0x00

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Bits	Field Name	Description	Type	Reset
9	DISABLECLK	This bit allows to gate the auxiliary clock #0 without condition. This is bit is intended to be used only when the SOC is not clock provider. 0x0: The auxiliary clock #0 is gated upon normal condition: auxiliary clock requests mapped on this path or ENABLE bit set. 0x1: The auxiliary clock #0 is gated wihout conditon.	RW	0
8	ENABLE	This bit allows to request the auxiliary clock #0 by software. 0x0: The auxiliary clock #0 is not requested by software. 0x1: The auxiliary clock #0 is requested by software.	RW	0
7:3	RESERVED	Reads returns 0.	R	0x00
2:1	SRCSELECT	This field allows selecting the clock source of the auxiliary clock #0. 0x0: The clock source is the system clock. 0x1: The clock source is the version from the CORE DPLL. 0x2: The clock source is the version from the PER DPLL. 0x3: The clock source is the alternate clock.	RW	0x0
0	POLARITY	This bit defines the output level when the auxiliary clock #0 is gated. 0x0: The auxiliary clock #0 is gated low. 0x1: The auxiliary clock #0 is gated high.	RW	0

Table 3-1476. Register Call Summary for Register AUXCLK0

PRCM Subsystem Environment • External Clock Signals: [0] [1]
SCRM Register Manual • SCRM Register Summary: [2]

Table 3-1477. AUXCLK1

Address Offset	0x0000 0314		
Physical Address	0x4A30 A314	**Instance**	SCRM
Description	This register holds qualifiers for the auxiliary clock #1.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								CLKDIV				RESERVED											ENABLE	RESERVED					SRCSELECT		POLARITY

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Bits	Field Name	Description	Type	Reset
31:20	RESERVED	Reads returns 0.	R	0x000
19:16	CLKDIV	This field holds the divider value for the auxiliary clock #1. 0x0: The auxiliary clock #1 is divided by 1. 0x1: The auxiliary clock #1 is divided by 2. 0x2: The auxiliary clock #1 is divided by 3. 0x3: The auxiliary clock #1 is divided by 4. 0x4: The auxiliary clock #1 is divided by 5. 0x5: The auxiliary clock #1 is divided by 6. 0x6: The auxiliary clock #1 is divided by 7. 0x7: The auxiliary clock #1 is divided by 8. 0x8: The auxiliary clock #1 is divided by 9. 0x9: The auxiliary clock #1 is divided by 10. 0xA: The auxiliary clock #1 is divided by 11. 0xB: The auxiliary clock #1 is divided by 12. 0xC: The auxiliary clock #1 is divided by 13. 0xD: The auxiliary clock #1 is divided by 14. 0xE: The auxiliary clock #1 is divided by 15. 0xF: The auxiliary clock #1 is divided by 16.	RW	0x0
15:9	RESERVED	Reads returns 0.	R	0x00
8	ENABLE	This bit allows to request the auxiliary clock #1 by software. 0x0: The auxiliary clock #1 is not requested by software. 0x1: The auxiliary clock #1 is requested by software.	RW	0
7:3	RESERVED	Reads returns 0.	R	0x00
2:1	SRCSELECT	This field allows selecting the clock source of the auxiliary clock #1. 0x0: The clock source is the system clock. 0x1: The clock source is the version from the CORE DPLL. 0x2: The clock source is the version from the PER DPLL. 0x3: The clock source is the alternate clock.	RW	0x0
0	POLARITY	This bit defines the output level when the auxiliary clock #1 is gated. 0x0: The auxiliary clock #1 is gated low. 0x1: The auxiliary clock #1 is gated high.	RW	0

Table 3-1478. Register Call Summary for Register AUXCLK1

SCRM Register Manual
- SCRM Register Summary: [0]

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Table 3-1479. AUXCLK2

Address Offset	0x0000 0318		
Physical Address	0x4A30 A318	**Instance**	SCRM
Description	This register holds qualifiers for the auxiliary clock #2.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												CLKDIV				RESERVED								ENABLE	RESERVED					SRCSELECT	POLARITY

Bits	Field Name	Description	Type	Reset
31:20	RESERVED	Reads returns 0.	R	0x000
19:16	CLKDIV	This field holds the divider value for the auxiliary clock #2. 0x0: The auxiliary clock #2 is divided by 1. 0x1: The auxiliary clock #2 is divided by 2. 0x2: The auxiliary clock #2 is divided by 3. 0x3: The auxiliary clock #2 is divided by 4. 0x4: The auxiliary clock #2 is divided by 5. 0x5: The auxiliary clock #2 is divided by 6. 0x6: The auxiliary clock #2 is divided by 7. 0x7: The auxiliary clock #2 is divided by 8. 0x8: The auxiliary clock #2 is divided by 9. 0x9: The auxiliary clock #2 is divided by 10. 0xA: The auxiliary clock #2 is divided by 11. 0xB: The auxiliary clock #2 is divided by 12. 0xC: The auxiliary clock #2 is divided by 13. 0xD: The auxiliary clock #2 is divided by 14. 0xE: The auxiliary clock #2 is divided by 15. 0xF: The auxiliary clock #2 is divided by 16.	RW	0x0
15:9	RESERVED	Reads returns 0.	R	0x00
8	ENABLE	This bit allows to request the auxiliary clock #2 by software. 0x0: The auxiliary clock #2 is not requested by software. 0x1: The auxiliary clock #2 is requested by software.	RW	0
7:3	RESERVED	Reads returns 0.	R	0x00
2:1	SRCSELECT	This field allows selecting the clock source of the auxiliary clock #2. 0x0: The clock source is the system clock. 0x1: The clock source is the version from the CORE DPLL. 0x2: The clock source is the version from the PER DPLL. 0x3: The clock source is the alternate clock.	RW	0x0
0	POLARITY	This bit defines the output level when the auxiliary clock #2 is gated. 0x0: The auxiliary clock #2 is gated low. 0x1: The auxiliary clock #2 is gated high.	RW	0

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Table 3-1480. Register Call Summary for Register AUXCLK2

SCRM Register Manual

- SCRM Register Summary: [0]

Table 3-1481. AUXCLK3

Address Offset	0x0000 031C		
Physical Address	0x4A30 A31C	**Instance**	SCRM
Description	This register holds qualifiers for the auxiliary clock #3.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												CLKDIV				RESERVED							ENABLE	RESERVED					SRCSELECT		POLARITY

Bits	Field Name	Description	Type	Reset
31:20	RESERVED	Reads returns 0.	R	0x000
19:16	CLKDIV	This field holds the divider value for the auxiliary clock #3. 0x0: The auxiliary clock #3 is divided by 1. 0x1: The auxiliary clock #3 is divided by 2. 0x2: The auxiliary clock #3 is divided by 3. 0x3: The auxiliary clock #3 is divided by 4. 0x4: The auxiliary clock #3 is divided by 5. 0x5: The auxiliary clock #3 is divided by 6. 0x6: The auxiliary clock #3 is divided by 7. 0x7: The auxiliary clock #3 is divided by 8. 0x8: The auxiliary clock #3 is divided by 9. 0x9: The auxiliary clock #3 is divided by 10. 0xA: The auxiliary clock #3 is divided by 11. 0xB: The auxiliary clock #3 is divided by 12. 0xC: The auxiliary clock #3 is divided by 13. 0xD: The auxiliary clock #3 is divided by 14. 0xE: The auxiliary clock #3 is divided by 15. 0xF: The auxiliary clock #3 is divided by 16.	RW	0x0
15:9	RESERVED	Reads returns 0.	R	0x00
8	ENABLE	This bit allows to request the auxiliary clock #3 by software. 0x0: The auxiliary clock #3 is disabled by software. 0x1: The auxiliary clock #3 is requested by software.	RW	0
7:3	RESERVED	Reads returns 0.	R	0x00
2:1	SRCSELECT	This field allows selecting the clock source of the auxiliary clock #3. 0x0: The clock source is the system clock. 0x1: The clock source is the version from the CORE DPLL. 0x2: The clock source is the version from the PER DPLL. 0x3: The clock source is the alternate clock.	RW	0x0

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Bits	Field Name	Description	Type	Reset
0	POLARITY	This bit defines the output level when the auxiliary clock #3 is gated. 0x0: The auxiliary clock #3 is gated low. 0x1: The auxiliary clock #3 is gated high.	RW	0

Table 3-1482. Register Call Summary for Register AUXCLK3

SCRM Register Manual
- SCRM Register Summary: [0]

Table 3-1483. AUXCLK4

Address Offset	0x0000 0320		
Physical Address	0x4A30 A320	**Instance**	SCRM
Description	This register holds qualifiers for the auxiliary clock #4.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												CLKDIV				RESERVED							ENABLE	RESERVED					SRCSELECT	POLARITY	

Bits	Field Name	Description	Type	Reset
31:20	RESERVED	Reads returns 0.	R	0x000
19:16	CLKDIV	This field holds the divider value for the auxiliary clock #4. 0x0: The auxiliary clock #4 is divided by 1. 0x1: The auxiliary clock #4 is divided by 2. 0x2: The auxiliary clock #4 is divided by 3. 0x3: The auxiliary clock #4 is divided by 4. 0x4: The auxiliary clock #4 is divided by 5. 0x5: The auxiliary clock #4 is divided by 6. 0x6: The auxiliary clock #4 is divided by 7. 0x7: The auxiliary clock #4 is divided by 8. 0x8: The auxiliary clock #4 is divided by 9. 0x9: The auxiliary clock #4 is divided by 10. 0xA: The auxiliary clock #4 is divided by 11. 0xB: The auxiliary clock #4 is divided by 12. 0xC: The auxiliary clock #4 is divided by 13. 0xD: The auxiliary clock #4 is divided by 14. 0xE: The auxiliary clock #4 is divided by 15. 0xF: The auxiliary clock #4 is divided by 16.	RW	0x1
15:9	RESERVED	Reads returns 0.	R	0x00
8	ENABLE	This bit allows to request the auxiliary clock #4 by software. 0x0: The auxiliary clock #4 is not requested by software. 0x1: The auxiliary clock #4 is requested by software.	RW	1
7:3	RESERVED	Reads returns 0.	R	0x00

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Bits	Field Name	Description	Type	Reset
2:1	SRCSELECT	This field allows selecting the clock source of the auxiliary clock #4. 0x0: The clock source is the system clock. 0x1: The clock source is the version from the CORE DPLL. 0x2: The clock source is the version from the PER DPLL. 0x3: The clock source is the alternate clock.	RW	0x0
0	POLARITY	This bit defines the output level when the auxiliary clock #4 is gated. 0x0: The auxiliary clock #4 is gated low. 0x1: The auxiliary clock #4 is gated high.	RW	0

Table 3-1484. Register Call Summary for Register AUXCLK4

SCRM Register Manual
- SCRM Register Summary: [0]

Table 3-1485. AUXCLK5

Address Offset	0x0000 0324		
Physical Address	0x4A30 A324	**Instance**	SCRM
Description	This register holds qualifiers for the auxiliary clock #5.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												CLKDIV				RESERVED							ENABLE	RESERVED					SRCSELECT		POLARITY

Bits	Field Name	Description	Type	Reset
31:20	RESERVED	Reads returns 0.	R	0x000
19:16	CLKDIV	This field holds the divider value for the auxiliary clock #5. 0x0: The auxiliary clock #5 is divided by 1. 0x1: The auxiliary clock #5 is divided by 2. 0x2: The auxiliary clock #5 is divided by 3. 0x3: The auxiliary clock #5 is divided by 4. 0x4: The auxiliary clock #5 is divided by 5. 0x5: The auxiliary clock #5 is divided by 6. 0x6: The auxiliary clock #5 is divided by 7. 0x7: The auxiliary clock #5 is divided by 8. 0x8: The auxiliary clock #5 is divided by 9. 0x9: The auxiliary clock #5 is divided by 10. 0xA: The auxiliary clock #5 is divided by 11. 0xB: The auxiliary clock #5 is divided by 12. 0xC: The auxiliary clock #5 is divided by 13. 0xD: The auxiliary clock #5 is divided by 14. 0xE: The auxiliary clock #5 is divided by 15. 0xF: The auxiliary clock #5 is divided by 16.	RW	0x0
15:9	RESERVED	Reads returns 0.	R	0x00

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Bits	Field Name	Description	Type	Reset
8	ENABLE	This bit allows to request the auxiliary clock #5 by software. 0x0: The auxiliary clock #5 is not requested by software. 0x1: The auxiliary clock #5 is requested by software.	RW	0
7:3	RESERVED	Reads returns 0.	R	0x00
2:1	SRCSELECT	This field allows selecting the clock source of the auxiliary clock #5. 0x0: The clock source is the system clock. 0x1: The clock source is the version from the CORE DPLL. 0x2: The clock source is the version from the PER DPLL. 0x3: The clock source is the alternate clock.	RW	0x0
0	POLARITY	This bit defines the output level when the auxiliary clock #5 is gated. 0x0: The auxiliary clock #5 is gated low. 0x1: The auxiliary clock #5 is gated high.	RW	0

Table 3-1486. Register Call Summary for Register AUXCLK5

SCRM Register Manual
- SCRM Register Summary: [0]

Table 3-1487. RSTTIME_REG

Address Offset	0x0000 0400		
Physical Address	0x4A30 A400	**Instance**	SCRM
Description	This register holds the reset time counter which is used to extend the reset lines beyond the release of the pad reset.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												RSTTIME			

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reads returns 0.	R	0x0000000
3:0	RSTTIME	Holds the number of 32 kHz clock cycles for which the reset duration is extended. Values 0,1 and 2 are not allowed. 0x0: Reserved. 0x1: Reserved. 0x2: Reserved.	RW	0x4

Table 3-1488. Register Call Summary for Register RSTTIME_REG

SCRM Register Manual
- SCRM Register Summary: [0]

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Table 3-1489. C2CRSTCTRL

Address Offset	0x0000 041C		
Physical Address	0x4A30 A41C	**Instance**	SCRM
Description	This register controls the release of the external C2C interface reset lines.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														WARMRST	COLDRST

Bits	Field Name	Description	Type	Reset
31:2	RESERVED	Reads returns 0.	R	0x0000 0000
1	WARMRST	This bit allows to release the warm reset line of the external C2C interface. [warm reset sensitive] 0x0: Clearing this bit has for effect to release the warm reset line of the external C2C interface. 0x1: Writing this bit has for effect to assert the warm reset line of the external C2C interface.	RW	1
0	COLDRST	This bit allows to release the cold reset line of the external C2C interface. 0x0: Clearing this bit has for effect to release the cold reset line of the external C2C interface. 0x1: Writing this bit has for effect to assert the cold reset line of the external C2C interface.	RW	1

Table 3-1490. Register Call Summary for Register C2CRSTCTRL

SCRM Register Manual
- SCRM Register Summary: [0]

Table 3-1491. EXTPWRONRSTCTRL

Address Offset	0x0000 0420		
Physical Address	0x4A30 A420	**Instance**	SCRM
Description	This register allows the software to perform an external power-on reset.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														PWRONRST	ENABLE

Bits	Field Name	Description	Type	Reset
31:2	RESERVED	Reads returns 0.	R	0x0000 0000
1	PWRONRST	This bit controls the assertion and the de-assertion of the external power-on reset. 0x0: De-asserts the external power-on reset. 0x1: Asserts the external power-on reset.	RW WSpecial	0

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Bits	Field Name	Description	Type	Reset
0	ENABLE	This bit must be set to 1 to allow the software to assert the external power-on reset. 0x0: Prevents the software to assert the external power-on reset. 0x1: Allows the software to assert the external power-on reset.	RW WSpecial	0

Table 3-1492. Register Call Summary for Register EXTPWRONRSTCTRL

Reset Management Functional Description • SCRM Reset Management Functional Description: [0] [1]
SCRM Register Manual • SCRM Register Summary: [2]

Table 3-1493. EXTWARMRSTST_REG

Address Offset	0x0000 0510		
Physical Address	0x4A30 A510	**Instance**	SCRM
Description	This register logs the source of warm reset output. Each bit is set upon release of the warm reset output and must be cleared by software.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															EXTWARMRSTST

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reads returns 0.	R	0x0000 0000
0	EXTWARMRSTST	This bit logs the external warm reset source. 0x0: No external warm reset occurred. 0x1: An external warm reset occurred.	RW W1toClr	0

Table 3-1494. Register Call Summary for Register EXTWARMRSTST_REG

Reset Management Functional Description • SCRM Reset Management Functional Description: [0]
SCRM Register Manual • SCRM Register Summary: [1]

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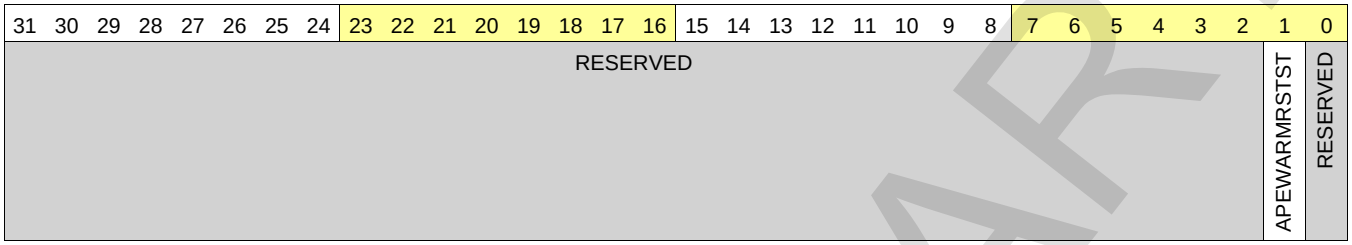
Table 3-1495. APEWARMRSTST_REG

Address Offset	0x0000 0514		
Physical Address	0x4A30 A514	**Instance**	SCRM
Description	This register logs the source of warm reset on the APE. Each bit is set upon release of the APE warm reset and must be cleared by software.		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:2	RESERVED	Reads returns 0.	R	0x0000 0000
1	APEWARMRSTST	This bit logs the APE warm reset source. 0x0: No APE warm reset occurred. 0x1: An APE warm reset occurred.	RW W1toClr	0
0	RESERVED	Reads returns 0.	R	0

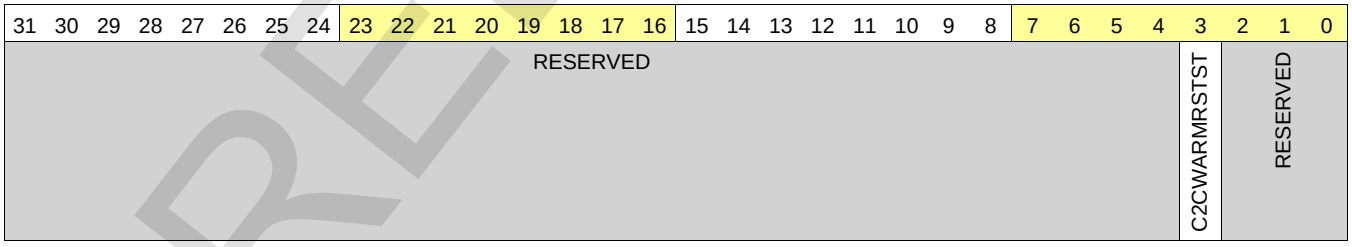
Table 3-1496. Register Call Summary for Register APEWARMRSTST_REG

SCRM Register Manual

- SCRM Register Summary: [0]

Table 3-1497. C2CWARMRSTST_REG

Address Offset	0x0000 051C		
Physical Address	0x4A30 A51C	**Instance**	SCRM
Description	This register logs the source of warm reset on the external C2C interface. Each bit is set upon release of the external C2C interface warm reset and must be cleared by software.		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reads returns 0.	R	0x0000000
3	C2CWARMRSTST	This bit logs the C2C warm reset source. 0x0: No C2C warm reset occurred. 0x1: A C2C warm reset occurred.	RW W1toClr	0
2:0	RESERVED	Reads returns 0.	R	0x0

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Table 3-1498. Register Call Summary for Register C2CWARMRSTST_REG

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• SCRM Register Summary: [0]

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3.13 SR Register Manual

3.13.1 SR Instance Summary

Table 3-1499. SR Instance Summary

Module Name	L4 Base Address	Size
SR_MPU	0x4A0D 9000	256Bytes
SR_IVA	0x4A0D B000	256Bytes
SR_CORE	0x4A0D D000	256Bytes

3.13.2 SR Registers

3.13.2.1 SR Register Summary

Table 3-1500. SR Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	SR_MPU L4 Base Address	SR_IVA L4 Base Address	SR_CORE L4 Base Address
SRCONFIG	RW	32	0x0000 0000	0x4A0D 9000	0x4A0D B000	0x4A0D D000
SRSTATUS	R	32	0x0000 0004	0x4A0D 9004	0x4A0D B004	0x4A0D D004
SENVAL	R	32	0x0000 0008	0x4A0D 9008	0x4A0D B008	0x4A0D D008
SENMIN	R	32	0x0000 000C	0x4A0D 900C	0x4A0D B00C	0x4A0D D00C
SENMAX	R	32	0x0000 0010	0x4A0D 9010	0x4A0D B010	0x4A0D D010
SENAVG	R	32	0x0000 0014	0x4A0D 9014	0x4A0D B014	0x4A0D D014
AVGWEIGHT	RW	32	0x0000 0018	0x4A0D 9018	0x4A0D B018	0x4A0D D018
NVALUERECIPROCAL	RW	32	0x0000 001C	0x4A0D 901C	0x4A0D B01C	0x4A0D D01C
RESERVED	W	32	0x0000 0020	0x4A0D 9020	0x4A0D B020	0x4A0D D020
IRQSTATUS_RAW	RW	32	0x0000 0024	0x4A0D 9024	0x4A0D B024	0x4A0D D024
IRQSTATUS	RW	32	0x0000 0028	0x4A0D 9028	0x4A0D B028	0x4A0D D028
IRQENABLE_SET	RW	32	0x0000 002C	0x4A0D 902C	0x4A0D B02C	0x4A0D D02C
IRQENABLE_CLR	RW	32	0x0000 0030	0x4A0D 9030	0x4A0D B030	0x4A0D D030
SENERROR	R	32	0x0000 0034	0x4A0D 9034	0x4A0D B034	0x4A0D D034
ERRCONFIG	RW	32	0x0000 0038	0x4A0D 9038	0x4A0D B038	0x4A0D D038

3.13.2.2 SR Register Description

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Table 3-1501. SRCONFIG

Address Offset	0x0000 0000
Physical Address	0x4A0D 9000 0x4A0D B000 0x4A0D D000
Description	Configuration bits for the Sensor Core and the Digital Processing.
Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ACCUMDATA								SRCLKLENGTH												SRENABLE	SENENABLE	ERRORGENERATORENABLE	MINMAXAVGENABLE	RESERVED						SENNENABLE	SENPENABLE

Bits	Field Name	Description	Type	Reset
31:22	ACCUMDATA	Number of Values to Accumulate	RW	0x080
21:12	SRCLKLENGTH	Determines frequency of SRClk	RW	0x200
11	SRENABLE	0: Asynchronously resets MinMaxAvgAccumValid, MinMaxAvgValid, ErrorGeneratorValid, AccumData sensor, SRClk counter, and MinMaxAvg registers. Also gates the clock for power savings and disables all the digital logic. , 1: Enables the module	RW	0
10	SENENABLE	0: All sensors disabled, 1: Sensors enabled per SenNEnable SenPEnable	RW	1
9	ERRORGENERATORENABLE	0: Error Generator Module disabled, 1: Error Generator Module enabled	RW	0
8	MINMAXAVGENABLE	0: MinMaxAvg Detector Module disabled, 1: MinMaxAvg Detector Module enabled	RW	0
7:2	RESERVED	Reserved	RW	0x00
1	SENNENABLE	0: Disable SenN sensor, 1: Enable SenN sensor	RW	1
0	SENPENABLE	0: Disable SenP sensor, 1: Enable SenP sensor	RW	0

Table 3-1502. Register Call Summary for Register SRCONFIG

Voltage Management Functional Description • Adaptive Voltage Scaling: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10]
PRCM Module Programming Guide • Global Initialization: [11] [12] [13] [14] [15] [16] [17] [18] • Changing OPP: [19]
SR Register Manual • SR Register Summary: [20]

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Table 3-1503. SRSTATUS

Address Offset	0x0000 0004
Physical Address	0x4A0D 9004 0x4A0D B004 0x4A0D D004
Description	Status bits that indicate that the values in the register are valid or events have occurred.
Type	R

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												AVGERRVALID	MINMAXAVGVALID	ERRORGENERATORVALID	MINMAXAVGACCUMVALID

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved	R	0x0000000
3	AVGERRVALID	0: AvgError registers are not valid, 1: AvgError registers are valid.	R	0
2	MINMAXAVGVALID	0: SenVal, SenMin, SenMax, SenAvg registers are not valid, 1: SenVal, SenMin, SenMax, SenAvg registers are valid, but not necessarily fully accumulated	R	0
1	ERRORGENERATORVALID	0: SenError register do not have valid data, 1: SenError registers have valid data.	R	0
0	MINMAXAVGACCUMVALID	0: SenVal, SenMin, SenMax, SenAvg registers are not valid, 1: SenVal, SenMin, SenMax, SenAvg registers have valid, final data	R	0

Table 3-1504. Register Call Summary for Register SRSTATUS

Voltage Management Functional Description
- Adaptive Voltage Scaling: [0] [1] [2] [3] [4] [5] [6]

SR Register Manual
- SR Register Summary: [7]

Table 3-1505. SENVAL

Address Offset	0x0000 0008
Physical Address	0x4A0D 9008 0x4A0D B008 0x4A0D D008
Description	The current sensor values from the Sensor Core.
Type	R

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SENPVAL																SENNVAL															

Bits	Field Name	Description	Type	Reset
31:16	SENPVAL	The latest value of the SenPVal from the sensor core.	R	0x0000
15:0	SENNVAL	The latest value of the SenNVal from the sensor core.	R	0x0000

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Table 3-1506. Register Call Summary for Register SENVAL

Voltage Management Functional Description • Adaptive Voltage Scaling: [0] [1] [2] [3]
SR Register Manual • SR Register Summary: [4]

Table 3-1507. SENMIN

Address Offset	0x0000 000C
Physical Address	0x4A0D 900C 0x4A0D B00C 0x4A0D D00C
Description	The minimum sensor values.
Type	R

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SENPMIN																SENNMIN															

Bits	Field Name	Description	Type	Reset
31:16	SENPMIN	The minimum value of the SenPVal from the sensor core since the last restat operation.	R	0xFFFF
15:0	SENNMIN	The minimum value of the SenNVal from the sensor core since the last restat operation.	R	0xFFFF

Table 3-1508. Register Call Summary for Register SENMIN

Voltage Management Functional Description • Adaptive Voltage Scaling: [0] [1] [2] [3]
SR Register Manual • SR Register Summary: [4]

Table 3-1509. SENMAX

Address Offset	0x0000 0010
Physical Address	0x4A0D 9010 0x4A0D B010 0x4A0D D010
Description	The maximum sensor values.
Type	R

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SENPMAX																SENNMAX															

Bits	Field Name	Description	Type	Reset
31:16	SENPMAX	The maximum value of the SenPVal from the sensor core since the last restat operation.	R	0x0000
15:0	SENNMAX	The maximum value of the SenNVal from the sensor core since the last restat operation.	R	0x0000

Table 3-1510. Register Call Summary for Register SENMAX

Voltage Management Functional Description • Adaptive Voltage Scaling: [0] [1] [2] [3]
SR Register Manual • SR Register Summary: [4]

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Table 3-1511. SENAVG

Address Offset	0x0000 0014
Physical Address	0x4A0D 9014 0x4A0D B014 0x4A0D D014
Description	The average sensor values.
Type	R

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SENPAVG																SENNAVG															

Bits	Field Name	Description	Type	Reset
31:16	SENPAVG	The running average of the SenPVal from the sensor core since the last restat operation.	R	0x0000
15:0	SENNAVG	The running average of the SenNVal from the sensor core since the last restat operation.	R	0x0000

Table 3-1512. Register Call Summary for Register SENAVG

Voltage Management Functional Description • Adaptive Voltage Scaling: [0] [1] [2] [3]
SR Register Manual • SR Register Summary: [4]

Table 3-1513. AVGWEIGHT

Address Offset	0x0000 0018
Physical Address	0x4A0D 9018 0x4A0D B018 0x4A0D D018
Description	The weighting factor in the average computation.
Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												SENPAVGWEIGHT		SENNAVGWEIGHT	

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved bits.	R	0x0000000
3:2	SENPAVGWEIGHT	The weighting factor for the SenP averager.	RW	0x0
1:0	SENNAVGWEIGHT	The weighting factor for the SenN averager.	RW	0x0

Table 3-1514. Register Call Summary for Register AVGWEIGHT

Voltage Management Functional Description • Adaptive Voltage Scaling: [0] [1] [2] [3]
PRCM Module Programming Guide • Global Initialization: [4] [5] [6] [7]
SR Register Manual • SR Register Summary: [8]

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Table 3-1515. NVALUERECIPROCAL

Address Offset	0x0000 001C
Physical Address	0x4A0D 901C 0x4A0D B01C 0x4A0D D01C
Description	The reciprocal of the SenN and SenP values used in error generation.
Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								SENPGAIN				SENNGAIN				SENPRN								SENNRN							

Bits	Field Name	Description	Type	Reset
31:24	RESERVED	Reserved bits.	R	0x00
23:20	SENPGAIN	The gain value for the SenP reciprocal.	RW	0x0
19:16	SENNGAIN	The gain value for the SenN reciprocal.	RW	0x0
15:8	SENPRN	The scale value for the SenP reciprocal.	RW	0x00
7:0	SENNRN	The scale value for the SenN reciprocal.	RW	0x00

Table 3-1516. Register Call Summary for Register NVALUERECIPROCAL

Voltage Management Functional Description • Adaptive Voltage Scaling: [0] [1] [2] [3] [4] [5] [6] [7]
PRCM Module Programming Guide • Global Initialization: [8] [9] [10] [11]
SR Register Manual • SR Register Summary: [12]

Table 3-1517. IRQSTATUS_RAW

Address Offset	0x0000 0024
Physical Address	0x4A0D 9024 0x4A0D B024 0x4A0D D024
Description	MCU raw interrup status and set.
Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												MCUACCUMINTSTATRAW	MCUVALIDINTSTATRAW	MCUBOUNDSINTSTATRAW	MCUDISABLEACKINTSTATRAW

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved bits.	R	0x0000000
3	MCUACCUMINTSTATRAW	0: Accum interrupt status is unchanged 1: Accum interrupt status is set	RW	0

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Bits	Field Name	Description	Type	Reset
2	MCUVALIDINTSTATRAW	0: Valid interrupt status is unchanged 1: Valid interrupt status is set	RW	0
1	MCUBOUNDSINTSTATRAW	0: Bounds interrupt status is unchanged 1: Bounds interrupt status is set	RW	0
0	MCUDISABLEACKINTSTATRAW	0: MCUDisable acknowledge status is unchanged 1: MCUDisable acknowledge status is set	RW	0

Table 3-1518. Register Call Summary for Register IRQSTATUS_RAW

SR Register Manual

- SR Register Summary: [0]

Table 3-1519. IRQSTATUS

Address Offset	0x0000 0028
Physical Address	0x4A0D 9028 0x4A0D B028 0x4A0D D028
Description	MCU masked interrupt status and clear.
Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												MCUACCUMINTSTATENA	MCUVALIDINTSTATENA	MCUBOUNDSINTSTATENA	MCUDISABLEACKINTSTATENA

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved bits	R	0x0000000
3	MCUACCUMINTSTATENA	Read 0: Accum interrupt status is unchanged. Read 1: Accum interrupt status is set. Write 0: Accum interrupt status is unchanged. Write 1: Accum interrupt status is cleared.	RW	0
2	MCUVALIDINTSTATENA	Read 0: Valid interrupt status is unchanged. Read 1: Valid interrupt status is set. Write 0: Valid interrupt status is unchanged. Write 1: Valid interrupt status is cleared.	RW	0
1	MCUBOUNDSINTSTATENA	Read 0: Bounds interrupt status is unchanged. Read 1: Bounds interrupt status is set. Write 0: Bounds interrupt status is unchanged. Write 1: Bounds interrupt status is cleared.	RW	0
0	MCUDISABLEACKINTSTATENA	Read 0: MCUDisable acknowledge status is unchanged. Read 1: MCUDisable acknowledge status is set. Write 0: MCUDisable interrupt status is unchanged. Write 1: MCUDisable interrupt status is cleared.	RW	0

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Table 3-1520. Register Call Summary for Register IRQSTATUS

Voltage Management Functional Description • Adaptive Voltage Scaling: [0] [1] [2] [3] [4]
PRCM Register Manual • INTRCONN_SOCKET_PRM Register Description: [5] [6] [7] [8]
SR Register Manual • SR Register Summary: [9]

Table 3-1521. IRQENABLE_SET

Address Offset	0x0000 002C
Physical Address	0x4A0D 902C 0x4A0D B02C 0x4A0D D02C
Description	MCU interrupt enable flag and set.
Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												MCUACCUMINTENASET	MCUVALIDINTENASET	MCUBOUNDSINTENASET	MCUDISABLEACTINTENASET

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved bits.	R	0x0000000
3	MCUACCUMINTENASET	Read mode: 0: Accum interrupt generation is disabled/masked, 1: Accum interrupt generation is enabled; Write mode: 0: No change to Accum interrupt enable, 1: Enable Accum interrupt generation.	RW	0
2	MCUVALIDINTENASET	Read mode: 0: Valid interrupt generation is disabled/masked, 1: Valid interrupt generation is enabled; Write mode: 0: No change to Valid interrupt enable, 1: Enable Valid interrupt generation.	RW	0
1	MCUBOUNDSINTENASET	Read mode: 0: Bounds interrupt generation is disabled/masked, 1: Bounds interrupt generation is enabled; Write mode: 0: No change to Bounds interrupt enable, 1: Enable Bounds interrupt generation.	RW	0
0	MCUDISABLEACTINTENASET	Read mode: 0: MCUDisableAck interrupt generation is disabled/masked, 1: MCUDisableAck interrupt generation is enabled; Write mode: 0: No change to MCUDisAck interrupt enable, 1: Enable MCUDisableAck interrupt generation.	RW	0

Table 3-1522. Register Call Summary for Register IRQENABLE_SET

Voltage Management Functional Description • Adaptive Voltage Scaling: [0] [1] [2] [3]
PRCM Module Programming Guide • Global Initialization: [4] [5] [6]
SR Register Manual • SR Register Summary: [7]

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Table 3-1523. IRQENABLE_CLR

Address Offset	0x0000 0030
Physical Address	0x4A0D 9030 0x4A0D B030 0x4A0D D030
Description	MCU interrup enable flag and clear.
Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												MCUACCUMINTENACLR	MCUVALIDINTENACLR	MCUBOUNDSINTENACLR	MCUDISABLEACKINTENACLR

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved bits.	R	0x0000000
3	MCUACCUMINTENACLR	Read mode: 0: Accum interrupt generation is disabled/masked, 1: Accum interrupt generation is enabled; Write mode: 0: No change to Accum interrupt enable, 1: Enable Accum interrupt generation.	RW	0
2	MCUVALIDINTENACLR	Read mode: 0: Valid interrupt generation is disabled/masked, 1: Valid interrupt generation is enabled; Write mode: 0: No change to Valid interrupt enable, 1: Enable Valid interrupt generation.	RW	0
1	MCUBOUNDSINTENACLR	Read mode: 0: Bounds interrupt generation is disabled/masked, 1: Bounds interrupt generation is enabled; Write mode: 0: No change to Bounds interrupt enable, 1: Enable Bounds interrupt generation.	RW	0
0	MCUDISABLEACKINTENACLR	Read mode: 0: MCUDisableAck interrupt generation is disabled/masked, 1: MCUDisableAck interrupt generation is enabled; Write mode: 0: No change to MCUDisAck interrupt enable, 1: Enable MCUDisableAck interrupt generation.	RW	0

Table 3-1524. Register Call Summary for Register IRQENABLE_CLR

Voltage Management Functional Description
- Adaptive Voltage Scaling: [0] [1] [2] [3]

SR Register Manual
- SR Register Summary: [4]

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Table 3-1525. SENERROR

Address Offset	0x0000 0034
Physical Address	0x4A0D 9034 0x4A0D B034 0x4A0D D034
Description	The sensor error from the error generator.
Type	R

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																AVGERROR								SENERROR							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved bits.	R	0x0000
15:8	AVGERROR	The average sensor error.	R	0x00
7:0	SENERROR	The percentage of sensor error.	R	0x00

Table 3-1526. Register Call Summary for Register SENERROR

Voltage Management Functional Description
- Adaptive Voltage Scaling: [0] [1] [2] [3] [4] [5] [6]

SR Register Manual
- SR Register Summary: [7]
- SR Register Description: [8]

Table 3-1527. ERRCONFIG

Address Offset	0x0000 0038
Physical Address	0x4A0D 9038 0x4A0D B038 0x4A0D D038
Description	The sensor error configuration.
Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					WAKEUPENABLE	IDLEMODE		VPBOUNDSINTSTATENA	VPBOUNDSINTENABLE	RESERVED			ERRWEIGHT			ERRMAXLIMIT								ERRMINLIMIT							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Reserved bits.	R	0x00
26	WAKEUPENABLE	Wakeup from MCU Interrupts enable.	RW	0
25:24	IDLEMODE	0b00: Force-Idle Mode, 0b01: No Idle Mode, 0b10: Smart-Idle Mode #2, 0b11: Smart-Idle-Wkup mode	RW	0x2
23	VPBOUNDSINTSTATENA	0: Bounds interrupt status is unchanged, 1: Bounds interrupt status is cleared.	RW	0
22	VPBOUNDSINTENABLE	0: Bounds interrupt disabled, 1: Bounds interrupt enabled.	RW	0
21:19	RESERVED	Reserved bits.	R	0x0

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Bits	Field Name	Description	Type	Reset
18:16	ERRWEIGHT	The AvgSenError weight.	RW	0x0
15:8	ERRMAXLIMIT	The upper limit of SenError for interrupt generation.	RW	0x7F
7:0	ERRMINLIMIT	The lower limit of SenError for interrupt generation.	RW	0x80

Table 3-1528. Register Call Summary for Register ERRCONFIG

Voltage Management Functional Description • Adaptive Voltage Scaling: [0] [1] [2] [3] [4] [5] [6] [7]
PRCM Module Programming Guide • Global Initialization: [8] [9] [10] [11] [12] [13] [14]
SR Register Manual • SR Register Summary: [15]

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Dual Cortex-A9 MPU Subsystem

This chapter describes the dual Cortex™-A9 MPU subsystem.

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4.1 Dual Cortex-A9 MPU Subsystem Overview

4.1.1 Introduction

The dual Cortex™-A9 microprocessor unit (MPU) subsystem of the device is based on the symmetric multiprocessor (SMP) architecture. Thus, the dual Cortex-A9 MPU subsystem delivers higher performance, optimal power management, and debug and emulation capabilities.

The dual Cortex-A9 MPU subsystem incorporates two Cortex-A9 central processing units (CPUs), level 2 (L2) cache shared between the two CPUs, and uses PL310 as an L2 cache controller. Each CPU has 32KB of level 1 (L1) instruction cache, 32KB of L1 data cache, separate dedicated power domain, and includes one Neon™ and Vector Floating Point Unit (VFPv3) coprocessors. The dual Cortex-A9 MPU subsystem also includes standard CoreSight™ components to support SMP debug and emulation, snoop control unit (SCU), interrupt controller (GIC), clock and reset manager, Memory Adapter (MA) and Cache Management Unit (CMU).

The MPU subsystem handles transactions among the ARM® core, L3 interconnect, EMIF controller (through the MA), L4-ABE, and interrupt controller (INTC).

Hereafter in this chapter, references to the dual Cortex-A9 MPU subsystem, Cortex-A9 MPU subsystem, and MPU subsystem are equivalent.

Figure 4-1 shows a high-level block diagram of the MPU subsystem.

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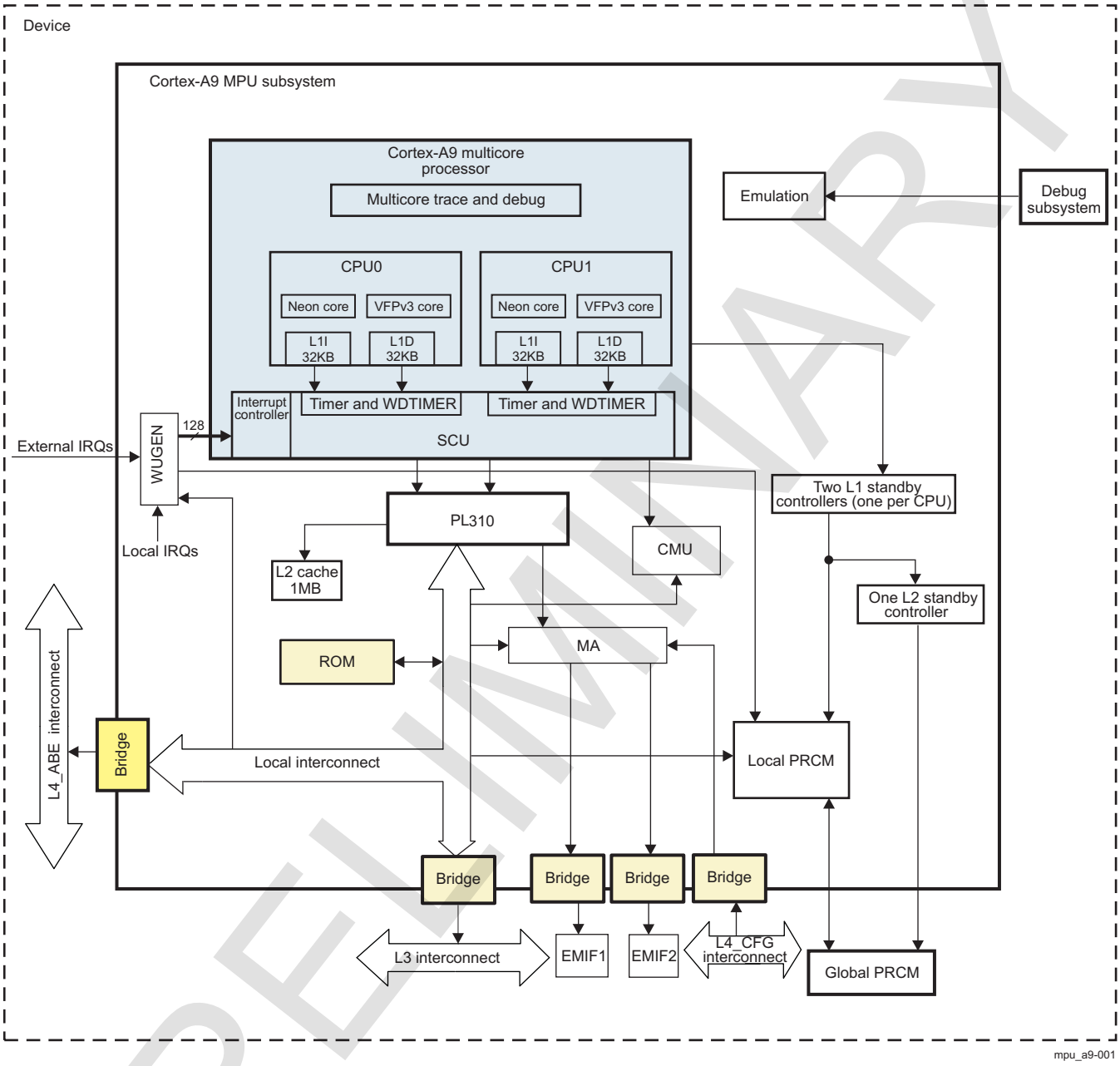
Figure 4-1. Cortex-A9 MPU Subsystem Overview



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4.1.2 Features

The Cortex-A9 MPU subsystem integrates the following:

- ARM subchip
  - Cortex-A9 core revision r2p10
  - SMP architecture
  - Superscalar, dynamic multiple issue technology with an efficient 8-stage pipeline
  - Out-of-order (OoO) instruction dispatch and completion
  - ARM Neon™ Advanced SIMD (single instruction, multiple data) support for accelerated media and signal processing computation.
  - Include VFPv3 hardware to support single and double-precision add, subtract, divide, multiply and accumulate, and square root operations
  - 32KB L1 instruction and 32-KB L1 data cache – 32-byte line size, 4-way set associative
  - Memory management unit (MMU)
    - Two-level translation lookaside buffer (TLB) organization
    - First level is an 32-entry, fully associative micro-TLB implemented on the Instruction and Data side.
    - Second level is a unified, 2-way associative, 128-entry main TLB
    - Supports hardware TLB table-walk
  - SCU ensures memory coherency between the two CPUs
  - Integrated timer and watchdog timer per CPU
  - Interrupt controller with 128 hardware interrupt inputs
- PL310 L2 cache controller (revision r3p1-50rel0) with 1-MB cache size
  - 16-way set associative
  - 32-byte line size
  - PL310 address filtering function used to split accesses between MA and Local interconnect
  - Two slave ports and two master ports
  - Includes four 256-bit line-fill-buffers (LFBs) shared by the master ports
  - Each slave port includes two 256-bit line-read-buffers (LRBs)
  - Includes four 256-bit store buffers with merge capability
  - Support for 64-byte line fills issued to L3
- Program trace macrocell (PTM)
- Emulation logic (cross-triggers)
- AMBA advanced trace bus (ATB) trace port
- Advanced peripheral bus (APB) port
- ROM memory
- Wake-up generator (WUGEN) module: Responsible for waking up the CPUs
- Standby controllers: The Cortex-A9 MPU implements a two-level standby controller consisting of two L1 standby controllers (one per CPU) and one L2 standby controller. The standby controllers handle the power transitions inside the Cortex-A9 MPU subsystem.
- Interface to audio back-end (ABE) subsystem: Enables direct connection between the Cortex-A9 multicore processor and the ABE module to reduce power consumption during long audio playback
- Power, clock, and reset manager: The Cortex-A9 MPU subsystem implements a local PRCM module to handle CPU power domains.
- MA
- CMU

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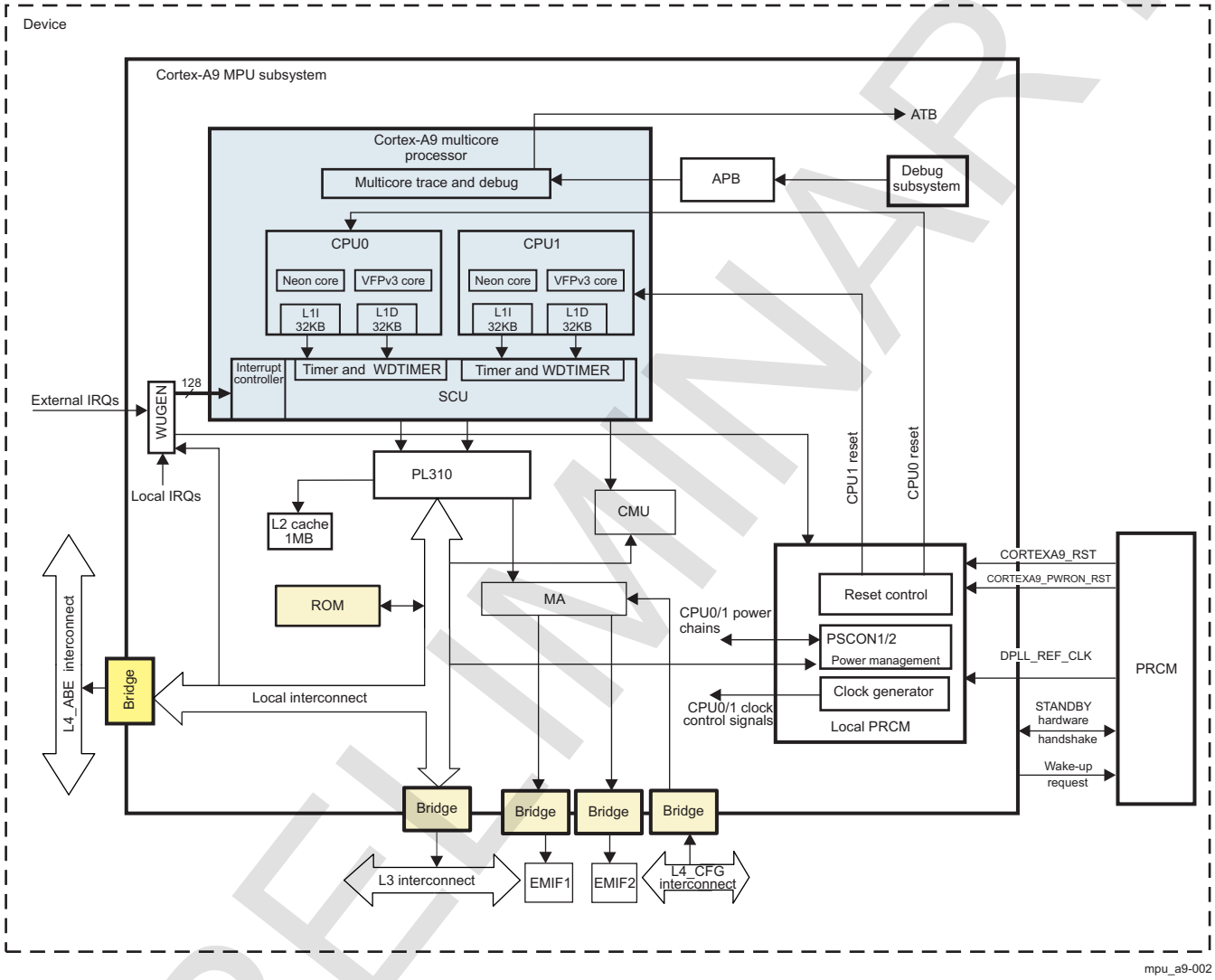
4.2 Dual Cortex-A9 MPU Subsystem Integration

This section describes the integration of the module in the device, including information about clocks, resets, and hardware requests.

Figure 4-2 shows the Cortex-A9 MPU integration.

Figure 4-2. Cortex-A9 MPU Subsystem Integration



NOTE: For more information about the STANDBY hardware handshake and the wake-up request, see Section 3.1.1.1, *Clock Management*, in Chapter 3, *Power, Reset, and Clock Management*.

Table 4-1 and Table 4-2 summarize the integration of the module in the device.

Table 4-1. Integration Attributes

Module Instance	Attributes	
	Power Domain	Interconnect
CORTEXA9	PD_MPU	L3

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Table 4-2. Clocks and Resets

Clocks				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
CORTEXA9	MPU_DPLL_CLK	MPU_DPLL_CLK	PRCM	Interface and functional clock
Resets				
CORTEXA9	CORTEXA9_PWRON_RSTN	CORTEXA9_PWRON_RSTN	PRCM	Power-on reset (POR) for all the modules inside the MPU system power domain; nonretention
	CORTEXA9_RSTN	CORTEXA9_RSTN	PRCM	Warm reset for all the modules inside the MPU system power domain; nonretention

4.2.1 Clock Distribution

The Cortex-A9 MPU clock generator is fed by the MPU digital phase-locked loop (DPLL), which can be gated off by the global power, reset, and clock management (PRCM) module when system power domain is in a low-power state. There is a global clock gating for each CPU. Because of the MPU DPLL, the Cortex-A9 MPU subsystem is asynchronous from the rest of the device.

The clock generator generates the following clocks from the MPU DPLL output clock:

- ARM_FCLK: ARM Cortex-A9 MPCore functional clock
- LOCAL_INTCNT_FCLK: Local interconnect functional clock
- CACHE_CTRL_FCLK: PL310 cache controller functional clock
- CMU_CLK1 and CMU_CLK2: CMU functional clocks
- MA_CLK1, MA_CLK2 and MA_CLK3: MA functional clocks

The following clocks have the same frequency:

- ARM_FCLK
- CACHE_CTRL_FCLK
- CMU_CLK1
- MA_CLK1

The frequency of the following clocks is half of ARM_FCLK:

- LOCAL_INTCNT_FCLK
- CMU_CLK2
- MA_CLK2

The frequency of MA_CLK3 is software-configurable (through the CM_MPU_MPU_CLKCTRL[24] CLKSEL_EMIF_DIV_MODE bit) and can be half of the ARM_FCLK and one fourth of the ARM_FCLK frequency.

NOTE: For more information about setting the CM_MPU_MPU_CLKCTRL[24] CLKSEL_EMIF_DIV_MODE and CM_MPU_MPU_CLKCTRL[25] CLKSEL_ABE_DIV_MODE bits, see the *Data Manual Operating Condition Addendum*.

Figure 4-3 shows the MPU subsystem clocking scheme.

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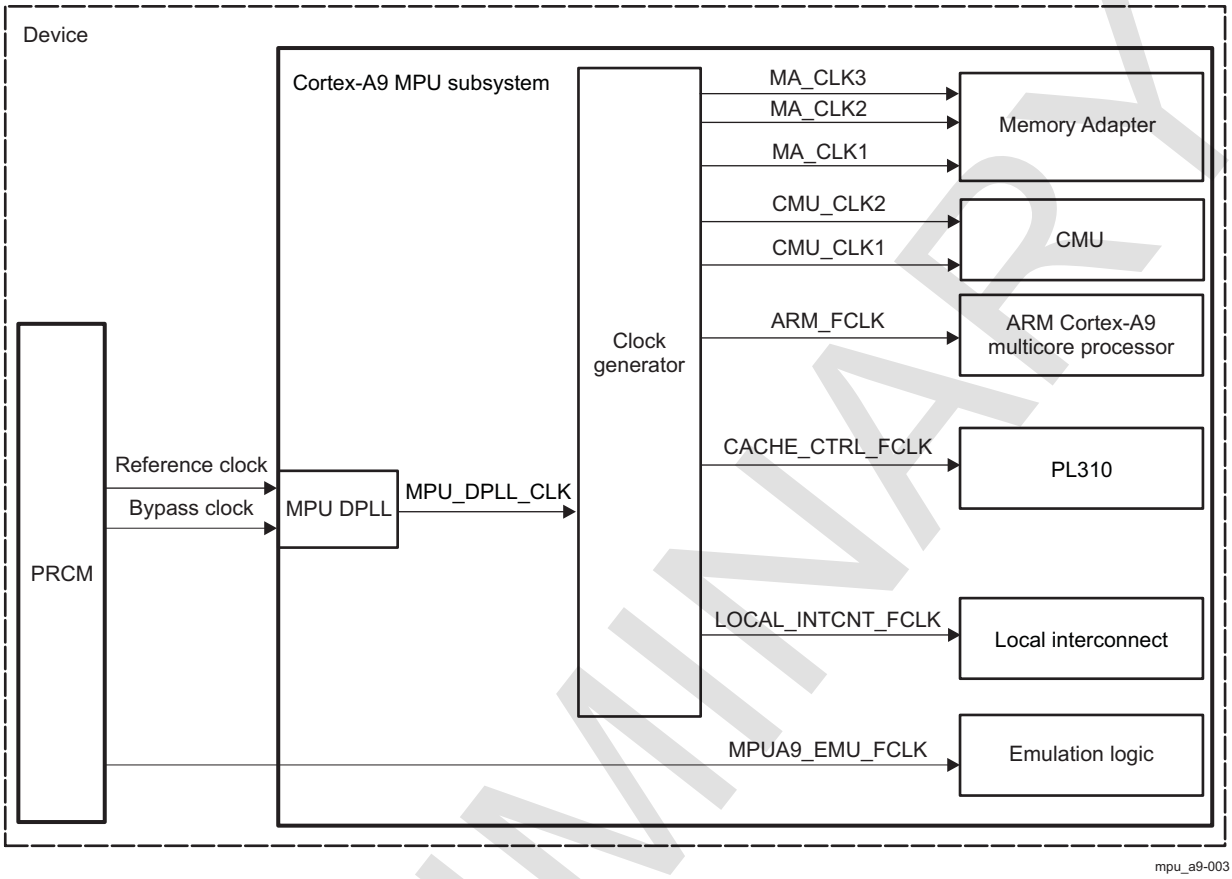
Figure 4-3. Cortex-A9 MPU Subsystem Clocking Scheme



NOTE: For more information about the MPU DPLL, see Section 3.6.3.3, *Generic DPLL Overview*, in Chapter 3, *Power, Reset, and Clock Management*.

The reference clock in Figure 4-3 is relevant to the DPLL_REF_CLK clock signal. The ARM Cortex-A9 multicore processor has no wake-up capabilities.

If only one Cortex-A9 CPU is needed, the ARM_FCLK can be gated independently for each CPU. For more information about how to gate this clock, see Section 4.3.6.2, *Power States of CPU0 and CPU1*.

The two Cortex-A9 CPUs cannot be clocked at different frequencies.

4.2.2 Reset Distribution

Resets to the MPU subsystem are provided by the global PRCM module and controlled by the local PRCM module.

For more information about the power domains in the Cortex-A9 MPU subsystem, see Section 4.3.6.1, *Power Domains*. Figure 4-4 shows the reset scheme of the MPU subsystem.

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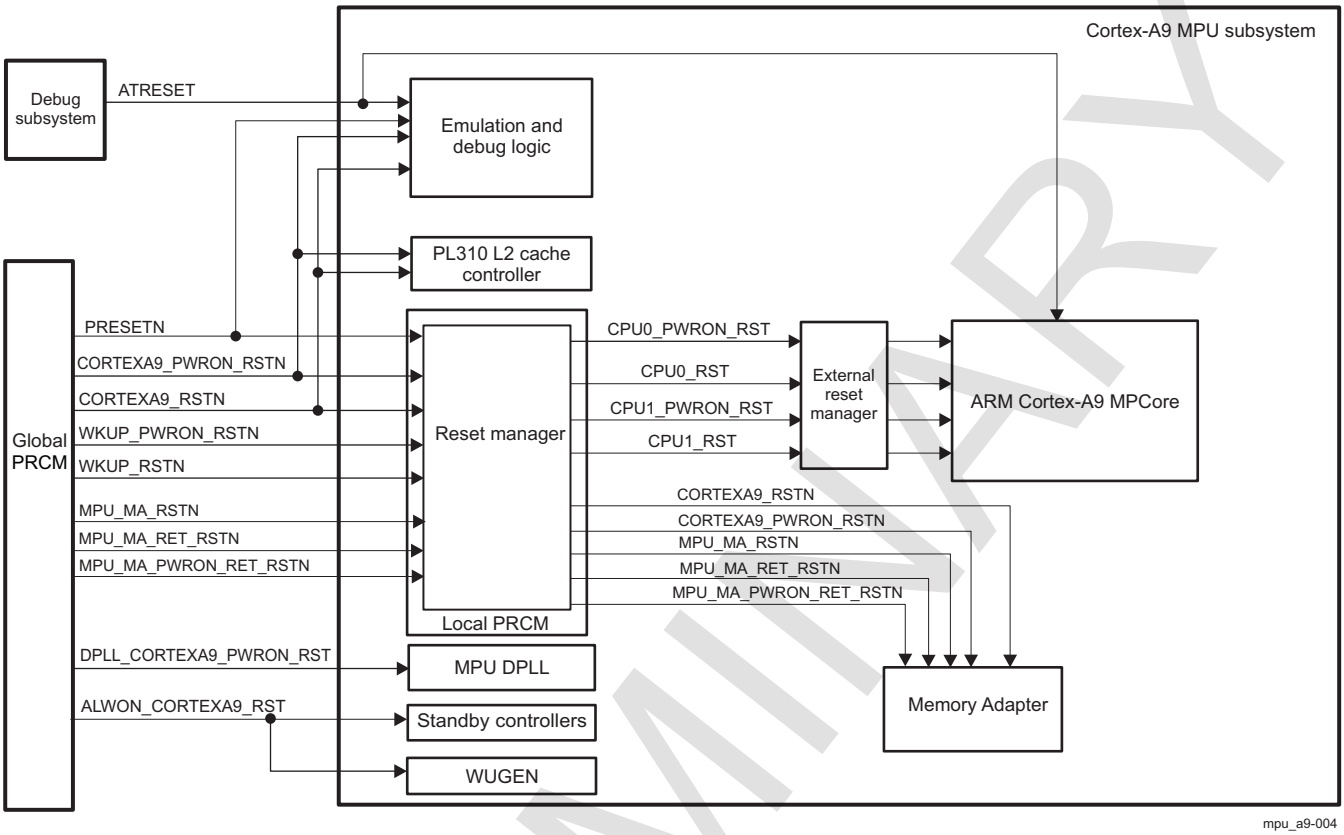
Figure 4-4. Cortex-A9 MPU Subsystem Reset Scheme



All eight external resets that are input to the local PRCM signals are active low. All eleven external reset input signals are driven by the global PRCM, except the ATRESETN reset signal, which is driven by the device debug subsystem. There are four internal reset signals that are generated by the local PRCM module.

ATRESETN is asserted at initial device power up and resets the debug and trace modules. ATRESETN affects the debug logic of the Cortex-A9 MPU and ARM CPUs.

The PRESETN reset signal resets the debug logic in the Cortex-A9 MPU (CTI0/1, trace funnel, DAP_PC) and ARM CPUs.

The WKUP_PWRON_RSTN reset signal is a global cold reset for the wake-up logic and resets the wake-up domain logic (the PSCON modules) in the local PRCM module. A cold reset is typically asserted when power is initially applied to the system. The user can check whether this reset event has occurred by reading the PRM_RSTST[0] GLOBAL_COLD_RESET bit.

The WKUP_RSTN reset signal is a global warm reset that resets the wake-up domain logic (the PSCON modules) in the local PRCM module. Warm reset is typically used for resetting a system that has been operating for some time. The user can check whether this reset event has occurred by reading the PRM_RSTST[1] GLOBAL_WARM_RST bit.

The DPLL_CORTEXA9_PWRON_RST reset signal resets the MPU_DPLL.

The ALWON_CORTEXA9_RST reset signal resets the MPU always-on domain: The standby controllers and the WUGEN. The user can check whether the reset has occurred by reading the WKG_CONTROL_0[15] DOMAIN_RST bit for CPU0 and the WKG_CONTROL_1[15] DOMAIN_RST bit for CPU1.

The MA has five incoming reset signals:

- CORTEXA9_RSTN
- CORTEXA9_PWRON_RSTN

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- MPU_MA_RSTN
- MPU_MA_RET_RSTN
- MPU_MA_PWRON_RET_RSTN

These five reset signals are driven by the Cortex-A9 MPU local reset manager and are active low.

The local PRCM module provides two reset signals for each CPU:

- The CPU0_RST and CPU1_RST reset signals are warm reset events. These reset signals initialize most of the ARM CPUs, except the debug logic (breakpoints and watchpoints are retained during this reset). The user can check whether these reset events have occurred by reading the RM_PDA_CPUi_RSTCTRL[0] RST bit.
- The CPU0_PWRON_RST and CPU1_PWRON_RST reset signals are cold and debug reset events.

For more information about clocks, resets, and power domains, and the CORTEXA9_PWRON_RSTN and CORTEXA9_RSTN reset signals, see Chapter 3, *Power, Reset, and Clock Management*.

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4.3 Dual Cortex-A9 MPU Subsystem Functional Description

4.3.1 Cortex-A9 MPU Subsystem Block Diagram

The Cortex-A9 MPU subsystem integrates the following group of submodules:

- Two ARM Cortex-A9 CPUs. Each CPU contains:
  - ARM version 7 ISA™: Standard ARM instruction set plus Thumb®-2 , Jazelle® RCT, and Jazelle DBX Java™ accelerator
  - Neon SIMD coprocessor and VFPv3
- INTC: Handles module interrupts (for more information, see Chapter 17, *Interrupt Controller*)
- PL310 L2 cache controller (revision r3p1-50rel0) with 1-MB cache and two 64-bit slave and two 64-bit master ports (for more information about the L2 cache controller, see the *ARM PL310 Cache Controller* TRM)
- Local interconnect: Connects the ARM Cortex-A9 multicore processor to:
  - Level 3 (L3) interconnect
  - ABE interconnect
  - Local PRCM module
  - PL310 L2 cache controller
  - On-chip ROM
  - WUGEN
  - CMU
  - MA
- Power, clock, and reset manager
- On-chip ROM: CPU0 (the master CPU) can boot from this memory. The ROM size is 48KB, and the address range is from 0x4003 0000 to 0x4003 BFFF. For more information, see Chapter 27, *Initialization*.
- WUGEN: Responsible for waking up the CPUs, used by the ROM code and OS during SMP boot. Two internal memory-mapped registers (AUX_CORE_BOOT_0 and AUX_CORE_BOOT_1) are available to the OS for communicating start-up information. For more information, see Chapter 27, *Initialization*.
- Standby controllers: Handle the power transitions inside the Cortex-A9 MPU subsystem
- SCU for L1 cache coherency
- One timer and one watchdog unit per core
- Caches memories:
  - 32-KB L1 instruction and 32-KB data caches: 4-way associative on each core
  - 1-MB L2 unified cache: 16-way associative
- MA
- CMU

Figure 4-5 is the Cortex-A9 MPU block diagram.

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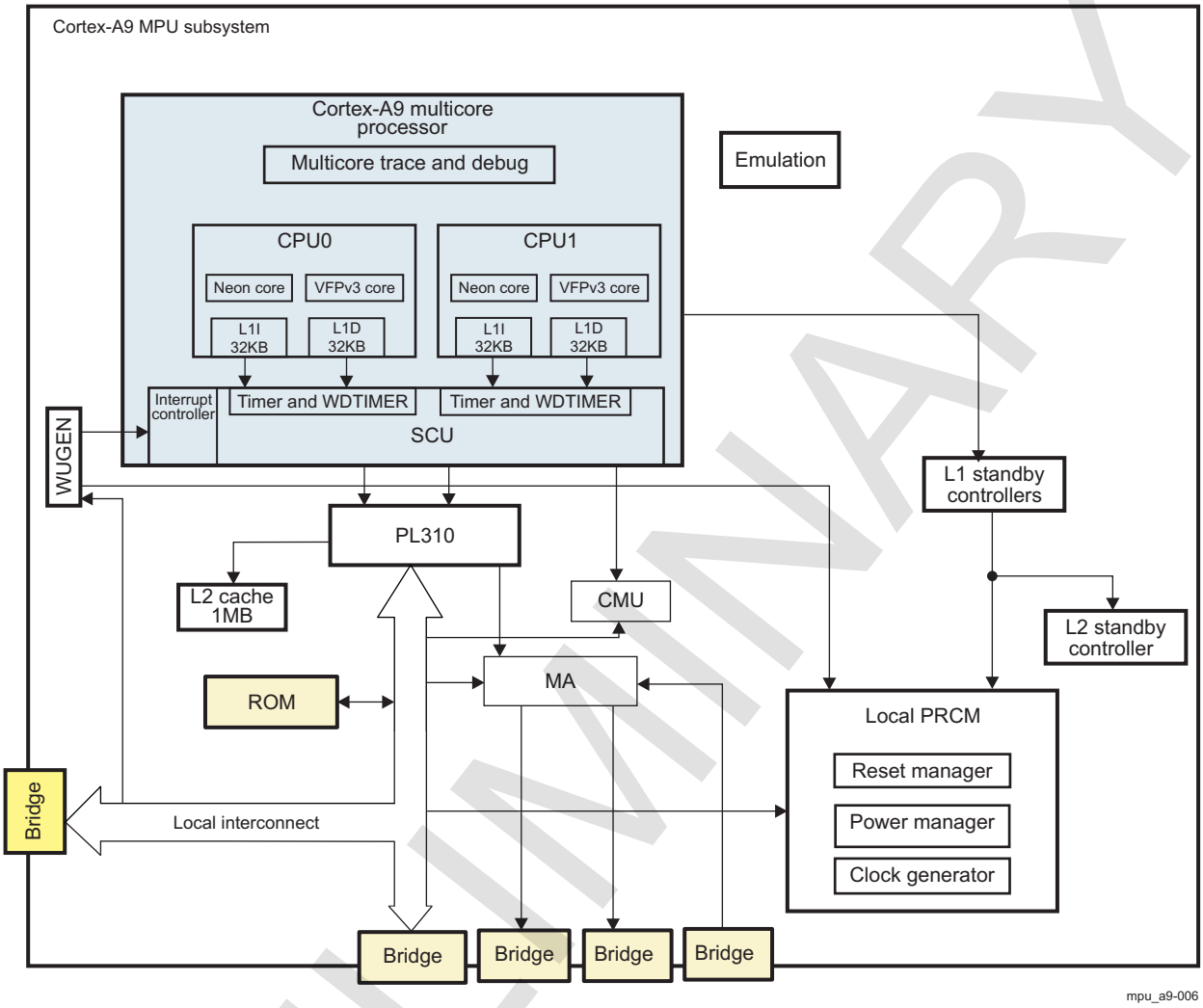
Figure 4-5. Cortex-A9 MPU Block Diagram



4.3.2 ARM Core

The Cortex-A9 MPU subsystem implements ARM version 7 ISA. Table 4-3 lists the main functions of the Cortex-A9 core.

Table 4-3. ARM Core Key Features

Feature	Comment
ARM version 7 ISA	Standard ARM instruction set + Thumb-2, Jazelle RCT/DBX Java accelerator, and media extensions. Backward-compatible with previous ARM ISA versions.
L1 Icache and Dcache	32KB each

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Table 4-3. ARM Core Key Features (continued)

Feature	Comment
L2 cache (PL310)	Main characteristics are: • Physically addressed and physically tagged • 16-way associative • 32-byte line length • Critical word first transactions • Prefetching capability • Pseudo-random victim selection policy • Two 256-bit LFBs in each master port • Two 256-bit LRBs in each slave port • Three 256-bit write buffers (merging capable) • Three 256-bit eviction buffers • Two 64-bit slave ports from SCU • Two master ports, one 64-bit port to L3 (through the Local interconnect) and one 128-bit port to EMIF (through the MA) • PL310 address filtering function used to split accesses between MA and Local interconnect • Support for 64-byte line fills issued to L3
SCU	The SCU controls by hardware the coherency of the two Cortex-A9 MPCores L1 data caches. The SCU supports up to four outstanding reads for each CPU. The SCU can be given an address range that redirects all memory transactions within this range to the second master ports (to L2 cache controller).
TLB	Two levels: Micro TLB (32 entries on each of instruction and data sides) + main TLB (instruction/data unified) implemented as a combination of a fully associative array of 4 elements (lockable) + a low-associative, 128 entries, 2-way
Trace interface	One program trace macrocell (PTM) per core
Branch prediction	512 entries per core + global history buffer (GHB) of 4096 2-bit predictors + 8-entry return stack
Enhanced MMU	Mapping sizes are 4KB, 64KB, 1MB, and 16MB.
Neon	Includes advanced SIMD instructions and the ARM VFPv3 instructions

4.3.3 Local Interconnect

The local interconnect is used in the device design to connect one of the 64-bit buses of the PL310 L2 cache controller to the L3 interconnect (64-bit width), MA, ABE interconnect port (32-bit width), and local power manager. The local interconnect must do some minimal address decoding to decide where to forward the requests.

Main features:

- Connects to the L3 interconnect through a 64-bit port. The interface frequency is configurable between one half (default value) and one fourth of the MPU_DPLL_CLK clock signal frequency. This is programmable in the CM_MPU_MPU_CLKCTRL[24] CLKSEL_EMIF_DIV_MODE bit.
- Connects to the ABE through a 32-bit port. The interface frequency is configurable between one fourth (default value) and one eighth of the MPU_DPLL_CLK clock signal frequency. This is programmable in the CM_MPU_MPU_CLKCTRL[25] CLKSEL_ABE_DIV_MODE bit.

NOTE: For more information about setting the CM_MPU_MPU_CLKCTRL[24] CLKSEL_EMIF_DIV_MODE and CM_MPU_MPU_CLKCTRL[25] CLKSEL_ABE_DIV_MODE bits, see the *Data Manual Operating Condition Addendum*.

- Connection to the CMU for register configuration
- Connection to the MA for register configuration
- Contains internal configuration register related to the MA function
- Supports single-request-multiple-data (data handshaking) burst mode to pipeline requests
- Supports multiple outstanding requests

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- Supports posted and nonposted write transactions, based on the attributes of the transactions coming from the ARM Cortex-A9 processor. Software can override all writes from the local interconnect to the L3 interconnect to be nonposted, regardless of the attributes of the transactions coming from the ARM Cortex-A9 processor, by setting the FORCEWRNP[0] MPUFORCEWRNP bit to 0x1. For the register description, see Chapter 18, *Control Module*.

NOTE: For the register description of the CM_MPU_MPU_CLKCTRL, see Chapter 3, *Power, Reset, and Clock Management*.

4.3.4 Memory Adapter

The purpose of the MA is to improve the missed latency of the L2 cache between the ARM Cortex-A9 processor and external memory. One of the PL310 master ports is connected to the MA and is used for all accesses to SCRAM. The PL310 address filtering mechanism is used to split incoming addresses between the MA connected to one of the PL310 master ports and the local interconnect connected to the other PL310 master port.

Requests from the MA to the EMIF typically run at half the CPU frequency. In high-speed (turbo) mode, when the CPU runs at higher frequency, these requests can be run at one fourth of the CPU frequency. The MA matches the bandwidth of the PL310 port on burst accesses by packing the write data to 128-bit-wide words and unpacking the 128-bit read data at full processor speed. Because the MA duplicates some of the logic in the local interconnect and DMM module, the MA has similar functionality.

The main features of the MA are:

- Connected to the PL310 slave port
- Direct 128-bit interface each to EMIF1 and EMIF2
  - Single request multiple data
  - No write response on posted writes
- Full-speed interface to the PL310 L2 cache controller
- Programmable half-speed (default is one half) or one-fourth speed interface to the EMIF (EMIF1 and EMIF2). This is selected by the CM_MPU_MPU_CLKCTRL[24] CLKSEL_EMIF_DIV_MODE bit.

NOTE: For more information about setting the CM_MPU_MPU_CLKCTRL[24] CLKSEL_EMIF_DIV_MODE and CM_MPU_MPU_CLKCTRL[25] CLKSEL_ABE_DIV_MODE bits, see the *Data Manual Operating Condition Addendum*.

- Performs interleaving functions to optimize the bandwidth of the EMIF
- Uses firewall logic to check access rights of incoming addresses. The firewall on both EMIF supports:
  - Configurable number of regions with fixed priority
  - Access support for up to eight execution domains
  - Busy indicator during reconfiguration
- Blocked read and write access to the EMIF for all accesses failing authorization checks
- Parallel processing of reads and writes
- Packing of burst write data into 128-bit words at full processor clock speeds
- Unpacking of burst read data into 64-bit words at full processor clock speeds
- Support for narrow bursts
- Burst wrap for single and double cache line fills.
- Supports the CMU by squelching dummy accesses (single thread operation only)
- Supports boot from EMIF space
- MA section manager (SM) supports:
  - Programmable multi-zone DRAM mapping and interleaving configuration
  - Supports 4 prioritized sections for defining configuration regions within the external memory

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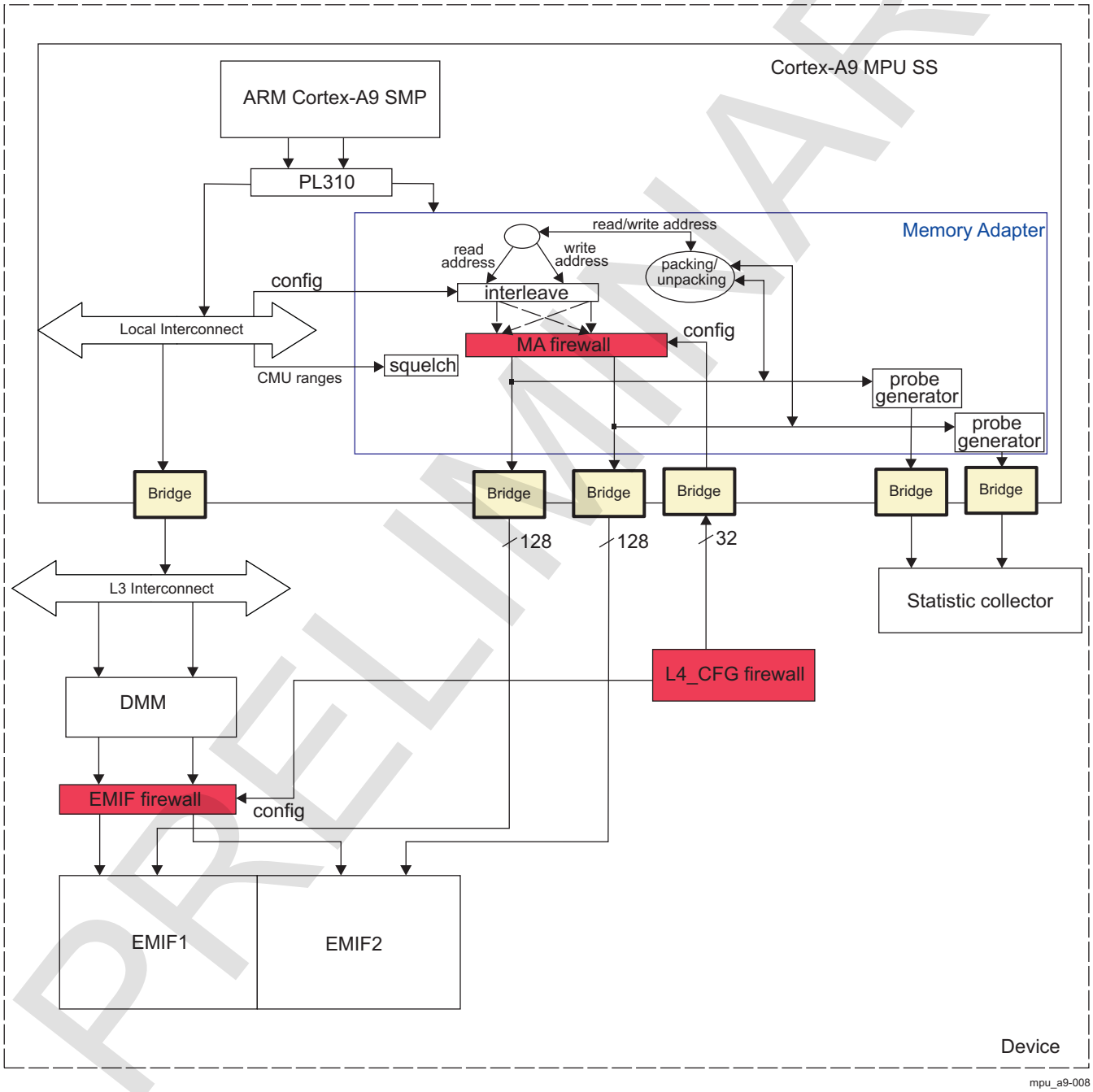
– Supports interleaving at 128-, 256-, and 512-byte boundaries

- Supports standard disconnect and idle protocols for independent powering down of the MA and both EMIFs (the EMIF must be powered down or up as a pair).
- Probe interface for performance monitoring of the EMIF ports
- Splits all read bursts that cross 1-KB boundaries

Figure 4-6 shows the integration of the MA in the device.

Figure 4-6. MA Block Diagram



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4.3.4.1 MA Functional Description

4.3.4.1.1 Input Interface

The input is driven from one of the PL310 master ports. Only accesses that target EMIF external space appear on this interface. All accesses to the configuration registers of the EMIF, firewall, and MA SM appear on the other master port of the PL310 and are routed through the local interconnect.

4.3.4.1.2 Interleaving

To optimize the bandwidth of the two EMIFs and their associated DDR memories, an interleaving scheme can be enabled. This interleaving is programmable and supports interleaving on 128-, 256-, and 512-byte boundaries. The programming can be performed in the MA_LISA_MAP_i[19:18] SDRC_INTL (where i = 0 to 3) bit fields. Some address translation is also part of this interleaving function. Because the EMIF memories are accessible by the Cortex-A9 MPU through the MA and the L3 interconnect through the DMM, the same interleaving scheme must be used. To ensure compatibility, the interleaving function is implemented by a scaled-down version of the MA SM, which implements the interleaving function in the DMM. For more information about the interleaving scheme of the MA SM, see Section 15.2.3.5.1.1, *Dynamic Mapping*, and Section 15.2.3.5.1.2, *Address Mapping*, in Section 15.2, *Dynamic Memory Manager*. When reading, replace DMM with MA SM.

4.3.4.1.2.1 Section Manager

The SM module in the MA contains one set of registers and three ports. Each port can handle one address translation, provide the interface size, and determine the EMIF mapping. Two of the ports process read and write addresses simultaneously. The third port processes the address of a split read burst. The MA SM supports four sections.

4.3.4.1.2.2 Memory Adapter Registers

Table 4-4 lists the DMM registers that are duplicated locally in the MA. These registers have the same names except that DMM is replaced by MA. Software must keep the content of these registers equal to the content of their counterparts in the DMM module.

Table 4-4. MA Registers Duplicated From the DMM Register Map

Register	Type	Width (Bits)	Base Address
MA_LISA_LOCK	RW	32	0x482A F01C
MA_LISA_MAP_i (where i = 0 to 3)	RW	32	From 0x482A F040 to 0x482A F04C

For descriptions of the registers, see *Section 15.2.6.2.2, DMM Register Description*, in Section 15.2, *Dynamic Memory Manager*. The only differences are the following reset values of the MA_LISA_MAP_0 register:

- MA_LISA_MAP_0[22:20] SYS_SIZE = 0x1(32-MB section)
- MA_LISA_MAP_0[17:16] SDRC_ADDRSPC = 0x1
- MA_LISA_MAP_0[9:8] SDRC_MAP = 0x1

The configuration of the MA must be programmed by the Cortex-A9 MPU to match the configuration of the DMM during boot. The registers must be locked after initial programming to avoid corruption by application software. When the SM configuration registers are being programmed there are no interlocks or safeguards to prevent accesses from being processed at the same time. The MA_LISA_LOCK and MA_LISA_MAP_i registers are retained during power down of retention mode.

If an access is made to a region marked as having unused address space or an unmapped SDRC map, no access is made to the EMIF and an error is returned. If an access is made to a region marked as accesses-SDRC-internal-registers, no access occurs to the EMIF and an error is returned. This is because the internal registers are not accessible from this port.

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4.3.4.1.2.3 Posted and Nonposted Writes

On posted writes, a response is returned after all write data is accepted by the MA and one of the follow occurs:

- The request is canceled, because of an interleaving error or is stopped by the CMU logic.
- The request is pushed into the firewall FIFO.

On nonposted writes, a response is not returned until after all write data is accepted by the MA and one of the follow occurs:

- The request is canceled, because of an interleaving error or is stopped by the CMU logic.
- The request has a firewall violation.
- The associated response is received from the EMIF (access is completed in the EMIF).

When the FORCEWRNP[0] MPUFORCEWRNP bit is set to 0x1, all writes are forced to be converted to nonposted writes (prevents posted writes).

4.3.4.1.2.4 Errors

If the region is marked as unmapped, targets EMIF internal registers or reserved space, access is blocked and an error response is returned. Such an error occurs on the first half of a potential split access and aborts the entire access at that time.

To avoid undefined results, the following program rules must be followed:

- A section cannot be mapped as interleaving (MA_LISA_MAP_i[9:8] SDRC_MAP = 0x3), and the MA_LISA_MAP_i[19:18] SDRC_INTL bit field must be equal to 0x0.
- If the section maps to a single EMIF (MA_LISA_MAP_i[9:8] SDRC_MAP = 0x1 or 0x2) , the MA_LISA_MAP_i[7:0] SDRC_ADDR bit field must be aligned to the MA_LISA_MAP_i[22:20] SYS_SIZE bit field (that is, the lower SDRC_ADDR bits must be 0).
- If the section maps to both EMIFs (MA_LISA_MAP_i[9:8] SDRC_MAP = 0x3), the MA_LISA_MAP_i[7:0] SDRC_ADDR bit field must be aligned to MA_LISA_MAP_i[22:20] SYS_SIZE – 1, because the addressable space for each EMIF is half.
- If the section maps to both EMIFs (MA_LISA_MAP_i[9:8] SDRC_MAP = 0x3), the MA_LISA_MAP_i[22:20] SYS_SIZE bit field cannot be 0.

4.3.4.1.3 CMU Access Squelching

The CMU allows blocks of memory space to be flushed from the cache in the background while the Cortex-A9 MPU runs other user code. The CMU accomplishes this by generating dummy read and write accesses through the PL310 accelerator coherency port (ACP), which evicts or invalidates the required lines. If these dummy accesses reach the MA, they must be killed and the appropriate response returned. For more information about the CMU, see Section 4.3.5, *Cache Management Unit*.

4.3.4.1.3.1 Statistics Collector Probe Ports

To enable performance monitoring by the debug subsystem, a subset of interconnect signals must be monitored and sent to a statistics collector in the CORE domain. For more information about the statistics collector, see Chapter 28, *On-Chip Debug Support*.

4.3.4.1.4 MA Firewall

A firewall exists between the interleaving logic and each of the EMIF ports. The firewall checks the address and access qualifiers against the permission attributes for the highest priority region to which the address belongs. If the access fails to get permission, a violation occurs and the fw_func_error or fw_debug_error outputs are asserted. The failing access is blocked and a slave error response is returned on the MA port for read and nonposted accesses. For more information about the MA firewall, see Chapter 13, *Interconnect*.

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4.3.4.1.5 MA Power and Reset Management

The MA supports a power-down state where the MA SM and FW configurations are retained. It also supports a save-and-restore operation where external logic saves the configuration state of the firewall (does not include the MA SM) and reloads it before the Cortex-A9 MPU is brought out of reset state. For more information about the save-and-restore operation, see , *sDMA*.

The MA SM supports only smart-idle mode.

4.3.5 Cache Management Unit

4.3.5.1 Overview

The CMU provides the ability to perform maintenance operations on Cortex-A9 MPU caches by physical address range. This reduces the execution time required by the Cortex-A9 CPUs to perform cache maintenance operations, while improving the overall throughput of maintenance operations. This frees the CPUs for other useful work. The registers inside the CMU are configured using the 32-bit interconnect configuration port from the local interconnect. The CMU operates at half the clock speed of the CPU core.

The main features of the CMU are:

- Autonomous cache invalidate and clean-and-invalidate operations on physical address ranges
- Multiprocessor and multiprogramming supported through built-in atomic range set allocation
- Independent programming of parameters in 64 range programming sets (RangeSets)
- Poll for status or interrupt on completion or error
- Handshake with power-management logic to ensure the CMU is idle before power management

The CMU indicates the idle status to the Cortex-A9 MPU subsystem, which implies all pending operations in the CMU are complete and is used by the local power-management logic to signal to the global PRCM module to shut down the domain clock and power of the Cortex-A9 MPU subsystem. The local power-management logic uses a handshake approach to ensure that the CMU completes all outstanding cache maintenance operations and enters IDLE state.

4.3.5.1.1 Integration in the Cortex-A9 MPU Subsystem

Figure 4-6 shows the integration of the CMU into the Cortex-A9 MPU subsystem. The CMU is connected to the ACP of the SCU. The ACP is a 64-bit slave port over which the CMU can perform ACP reads and writes, coherent and noncoherent. The registers inside the CMU are configured using the 32-bit interconnect configuration port from the local interconnect.

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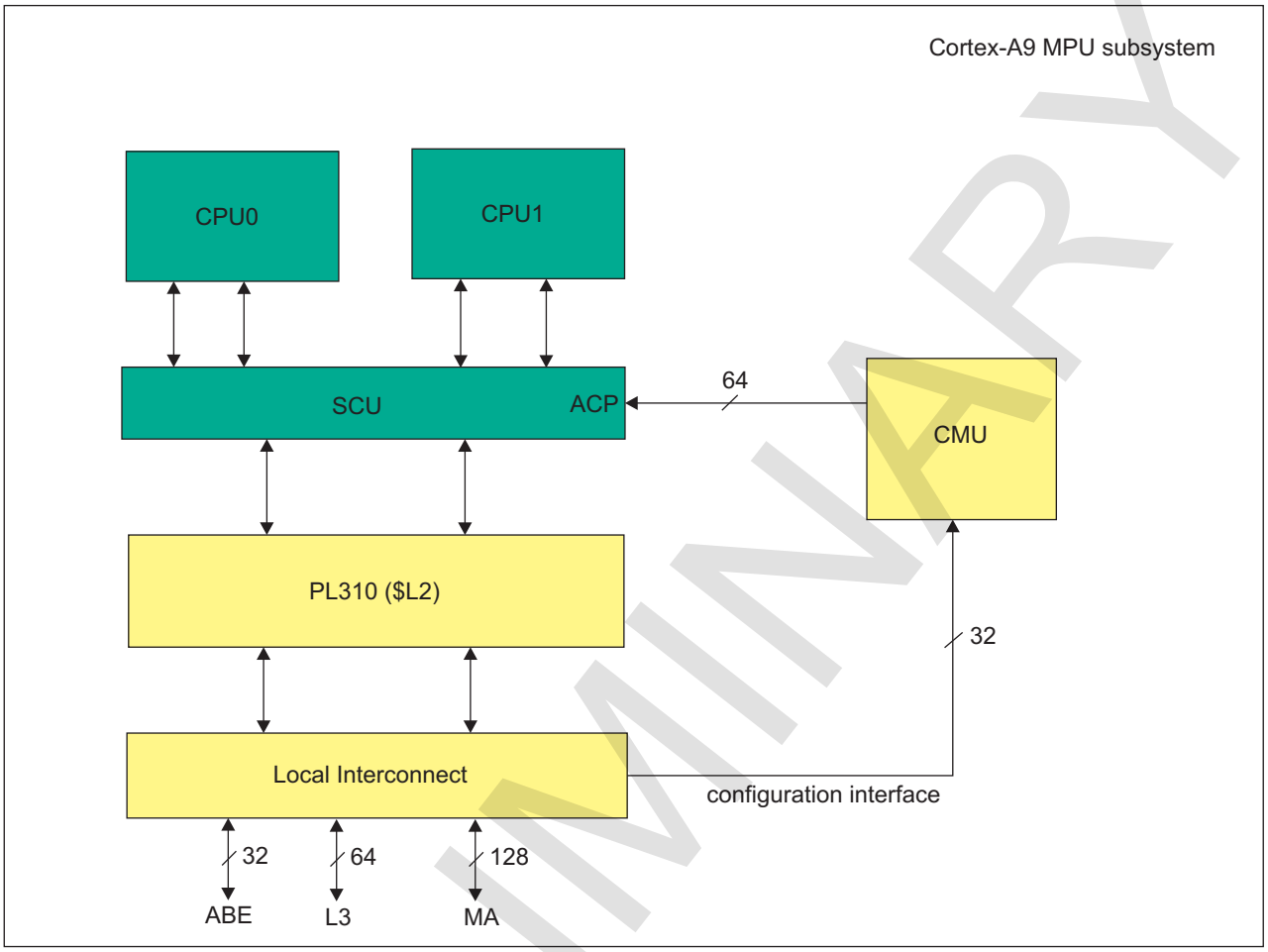
Figure 4-7. Integration of CMU in Cortex-A9 MPU Subsystem



4.3.5.1.2 Functionality

The CMU is programmed with:

- Starting physical address: CMUSTARTPA_i[31:0] STARTPA. It is a byte granular address and has no alignment restrictions.
- Length of region to be operated on: CMULENGTH_i[11:0] LEN. The maximum length can be as large as 4KB or as small as 1 byte. CMU operates on "line step" granularity, and the default value for line step is 32 bytes, which is the line size of the Cortex-A9 MPU. The line step can be programmed in the CMUCONFIGREG[2:0] LINESTEP bit field.
- Type of operation to be performed (clean/clean-invalidate/invalidate): CMUOPERATION_i[3:0] OPNSEL

This information is programmed in a structure called a range set.

The CMU performs the appropriate operation (clean/clean-invalidate/invalidate) on the address range in all cache levels on a line step basis and can be programmed to interrupt the processor when the operation completes, or to poll for the status. The CMU can generate an interrupt request (CMU_IRQ_P) to the Cortex-A9 MPU interrupt controller (mapped as MA_IRQ_6) when it finishes operating.

The CMU has 64 range sets. Allocation and deallocation of the 64 range sets is done as an explicit step in software. Allocation is performed by reading the CMUALLOCATE register. Deallocation is performed by writing in the CMUDEALLOCATE register. Two groups of registers can check the status of operations: CMUOPERATION_i and CMURANGESTATE_i.

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4.3.5.1.3 Clean/Clean-Invalidate/Invalidate Flow

For all flows, the following bits must be set in PL310 so that the L2 line is invalidated on a write if it hits in the L2 cache:

- Shared Attribute Override Enable = 0; bit 22 of the Auxiliary Control Register. This is the default behavior and transforms normal memory noncacheable transactions into:
  - Cacheable no allocate for reads: L2 is looked up.
  - Write Through (WT) and No Write Allocate (NWA) for writes: L2 is updated on a hit and write is sent to L3. These writes are done as part of the clean/clean-invalidate flow.
- Shared Attribute Invalidate Enable = 1; bit 13 of the Auxiliary Control Register. When this bit is set, the L2 line is invalidated in the L2 cache and a write is sent to L3.

4.3.5.1.3.1 Clean/Clean-Invalidate Flow

For a clean/clean-invalidate operation:

1. The CMU performs an ACP read of the first line in the address range:
   (a) If the address hit in L1 or L2, get data from L1 or L2. The CMU does not know where it came from.
   (b) Else if the address missed in L1 and L2:
      (i) PL310 sends a read request to L3.
      (ii) The local interconnect returns a slave error to the CMU if the local interconnect sees a read request from the CMU/ACP and the CMU ends the operation on that line.
2. If the ACP read did not abort, the CMU performs an ACP write of data returned from the ACP read (all bytes valid). This is called as an optimized transfer.
   (a) ACP write of all bytes invalidates the line in L1: Cortex-A9 behavior
   (b) ACP write goes to PL310 where if the address hits, the PL310 line is invalidated. To optimize CMU flows, some auxiliary control bits must be set to make use of the "invalidate L2 line if it hits" feature.
   (c) ACP writes the data to L3 through the local interconnect: The line has been cleaned/clean-invalidated. Clean invalidates the line.
3. Return to Step 1 for the next line in the range if the address of the next line is less than the starting physical address + length.

NOTE: There is no difference between the clean and clean-invalidate flows.

NOTE: The PL310 auxiliary control register cannot be changed dynamically. L2 must be disabled, which requires flushing the buffers, etc. and then changing the register.

4.3.5.1.3.2 Invalidate Flow

For an invalidate operation:

1. The CMU does an ACP write of all bytes. Data is set to 0.
2. This invalidates lines in L1 and L2; if it hit in L1 or L2, the write is sent to L3 by PL310. The local interconnect drops the write request and sends an OKAY response to the CMU.
3. If the address misses in L1 and L2, the PL310 sends the address to the local interconnect, which drops the write request and sends an OKAY response to the CMU.

4.3.5.2 Architecture

Figure 4-8 shows the major blocks of the CMU.

- Range Operations Queue: Queue of activated range sets
- RangeSet Register Array: Sets of registers holding the range sets
- Range Walker: Block that performs the operation
- Index Queue: Holds a queue of indices of the range set that needs to interrupt the CPUs

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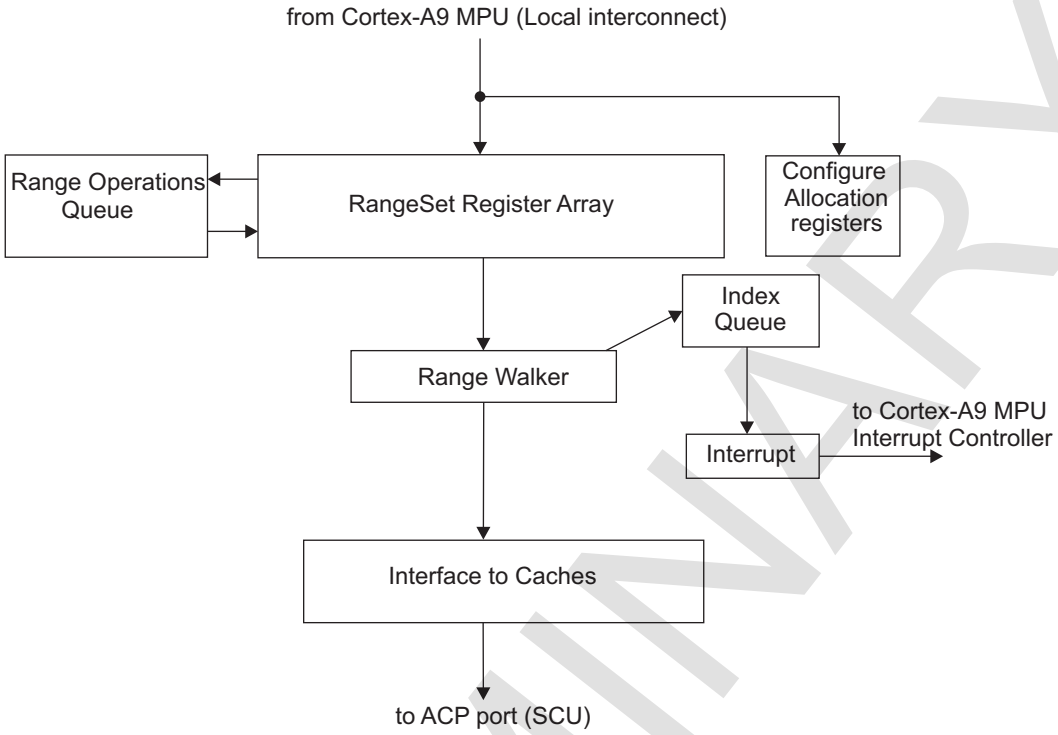
Figure 4-8. Cache Maintenance Unit Blocks



The Interface to Caches (see Figure 4-8) issues a request to no more than one cache line at a time.

4.3.5.2.1 Range Sets

Each range operation is programmed into a set of range operation registers called a range set. The CMU has 64 range sets.

The CMU supports queuing of cache maintenance range operations. By enqueuing range sets, the programming interface is freed to allow programming of the next range set.

A range set has three registers that must be programmed to define the range set operation:

- The CMU Starting Address Register contains a 32-bit physical address (CMUSTARTPA_i[31:0] STARTPA).
- The CMU Length Register programs the length of a range in bytes (CMULENGTH_i[11:0] LEN). The value in this register must be the length of the data buffer minus 1 so that CMUSTARTPA + CMULENGTH is the address of the last byte within the range. Cache lines containing the starting address and every physical address up to and including CMUSTARTPA + CMULENGTH have the particular cache management operation (CMO) performed on them.
- The CMU Operation Register controls the operation performed and several other properties of the range set (CMUOPERATION_i[3:0] OPNSEL). The operations supported are clean, clean/invalidate, and invalidate. The write to set the operation register activates the range set. Once the range set is activated, software must not attempt to change any range set register.

Figure 4-9 shows the relationship between the starting address and the length.

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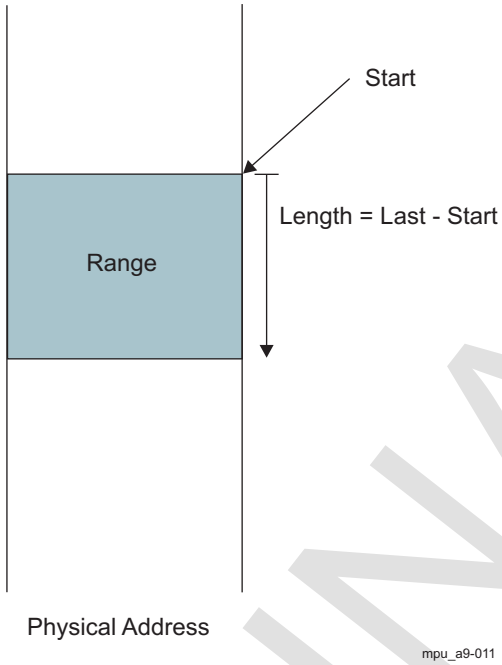
Figure 4-9. Start and Length of Range Set



Multiple range set may be programmed and will queue to execute. The programmer should not wait for previous range sets to complete before activating new range sets.

4.3.5.2.2 Parallelism and Pipelining

The CMU can pipeline requests, thus achieving faster throughput on the execution of a range set operation.

The CMUCONFIGREG[10] DISABLEPIPELINING bit forces the interface to the caches to issue a request to no more than one cache line at a time. Depending on the particular interface to the caches, operations can normally be pipelined several cache lines deep by issuing operations against additional cache lines before earlier cache line requests are complete. The disable pipelining feature causes the CMU to perform the operations serially. When disable pipelining is enabled, the accesses are sent as strongly ordered accesses; this ensures that accesses are not pipelined. This feature detects bad addresses that have been programmed in the CMU, because this address goes to the local interconnect block, which then detects the bad addresses. Setting disable pipelining makes the CMU ineffective. Therefore, disable pipelining must be used only for debug purposes when bad address programming is suspected.

In addition, the CMU can process more than one range-set operation in parallel. Multithreading can occur through time-multiplexing or pipelining the operation of more than one range operation so that they occur at least partially in parallel. The CMUOPERATION_i[8] WAIT bit indicates that this range operation must not be started until all previously activated operations complete (wait does not affect allocated operations, only activated operations). Thus, the WAIT bit prevents a range operation from being threaded in parallel with any range operation activated earlier.

4.3.5.2.3 Completion Handling

Completion of the handling of a range-set operation leaves it in completed state or error state. The completion handling option for a range set is programmed in th CMUOPERATION_i[10:9] COMPLETION bit field. No interrupt is sent if the CMUCONFIGREG[8] INTEN is set to 0.

Anytime a normal or error completion generates an interrupt (or would, but INTEN = 0), the INDEX, ERROR, and VALID bits of the CMUINTRACK register of the range set is put into the interrupt index queue of the CMU FIFO. If the FIFO is already full and INTEN = 1, the CMU suspends the processing of range sets until the completion can be recorded in the range set. If the FIFO is already full and INTEN = 0, the newest completion is lost and not recorded in the FIFO.

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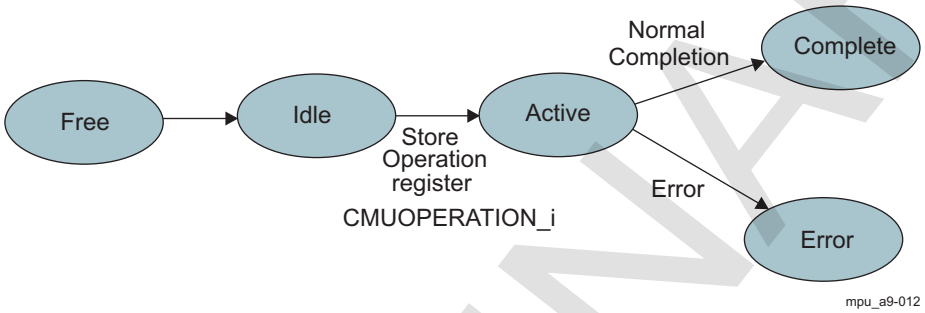
Normal completion is not signaled until any writes generated by clean operations have reached the point where they can be seen by all masters in the device, usually the main memory.

Figure 4-10 shows the states a range set can take:

- Free: Range set is available.
- Idle: Range set has been allocated or reserved by software, but not yet activated.
- Active: Range set has been activated.
- Complete: Range set completed normally.
- Error: Range set completed with an error.

Figure 4-10. Range Set States



4.3.5.2.4 Allocation

To allocate a range set, software reads the allocation register (CMUALLOCATE). This register returns the index of a free range set (in free state). If there are no free range sets, the register returns with the NONE bit set (CMUALLOCATE[31] NONE = 0x1). The range set that is allocated is moved to idle state and is not available for allocation.

To return a range set to free state, software that has processed the completion must write the range set index to the deallocation register (CMUDEALLOCATE[7:0] INDEX). If software does not deallocate range sets, the pool of free range sets is exhausted and allocation fails.

This allocation and deallocation scheme places all mutual exclusion into the allocation hardware where it can be made atomic.

The number of allocations is the total number of range sets minus 8.

4.3.5.3 Address Sequence Generation

The CMU generates a sequence of addresses according to the programmed quantities in a range set. The addresses generated are always aligned to the LINESTEP size.

Because the length register (CMULENGTH_i) encodes the range length (1 byte), the minimum length that can be encoded is 1 byte (encoded as 0 in the length field: CMULENGTH_i[11:0] LEN = 0x0).

The first address issued is always the StartingPA (CMUSTARTPA_i[31:0] STARTPA) aligned to the beginning of the cache line.

After each cache line step, the working address is incremented by the LINESTEP size (32 bytes). If the new working address is greater than CMUSTARTPA_i + CMULENGTH_i, the operation is complete. Otherwise, the operation is performed using the new working address and execution loops to perform the next cache line step.

4.3.5.4 Using the CMU

To use the CMU:

1. Allocate a range set.
2. Store StartPA and length.
3. Activate by storing the operation register.

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4. Monitor for completion through an interrupt (preferred) or polling.
5. Free range set.

Section 4.3.5.4.6 explains how to use the CMU with paged memory so that a single buffer can span the divide between pages and large buffers that are more than 4KB in length.

NOTE: It is important to follow the previous sequence. Otherwise, interconnect response errors can occur. For example, trying to free a range set before it completes (with or without error) can lead to an interconnect response error. Writing to a range that is not free (which is really IDLE, because free goes to IDLE after successful allocation) also leads to interconnect response errors.

It is not necessary to enable interrupts on all range sets. For example, if five ranges are enabled, then interrupt can be enabled for only the last range set (assuming range sets 0, 1, 2, 3, and 4 were activated in that order [0 first, 1 next, etc.]). Then, when interrupt is enabled for range set 4, range sets 0, 1, 2 ,and 3 are assured to be complete. However, it is still recommended to read the status of range sets 0, 1, 2, and 3 to ensure they are complete and without errors, before concluding that range sets 0 to 4 are complete.

4.3.5.4.1 Allocating a Range Set

Software may attempt to allocate a range set by reading from the CMU allocation register (CMUALLOCATE). If the returned value is positive, it is the index of a range set that has been allocated by this read. The allocated range set is not eligible for allocation again until it is freed. The allocation register makes mutual exclusion unnecessary for choosing and programming a range set.

If the value returned by the allocation register is 1 (the CMUALLOCATE[31] NONE bit), no range set can be allocated. Software must wait to allow processing that can free a range set to complete before retrying the allocation.

The number of allocations is 56.

4.3.5.4.2 Storing Starting Physical Address and Length

The first store into a range set must be to the CMUSTARTPA_i[31:0] STARTPA bit field.

The STARTPA is the lowest physical address in the range (the smallest value in unsigned arithmetic). It is a 32-bit byte address. There are no address alignment constraints because the range walker masks the generated addresses so that each cache operation is performed to the lowest address in a cache line.

The CMULENGTH_i[11:0] LEN bit field is defined to be the difference between the STARTPA and the byte of the range with the highest value (using unsigned arithmetic). This is the size of the range minus 1. The byte addressed by STARTPA + LEN is within the range. The largest range size is 4KB.

4.3.5.4.3 Activate the Range Set by Storing the Operation Register

A range set is activated when its operation register is stored. This register is programmed with the cache operation (CMUOPERATION_i), whether to interrupt on completion, and other controls.

The registers of a range set are not writable unless they are in IDLE state. This must be enforced in software; otherwise, an interconnect response error occurs.

A range set cannot be deallocated unless it is in COMPLETE or ERROR state. This also must be enforced in software; otherwise, an interconnect response error occurs.

4.3.5.4.4 Monitoring Completion

Two ways to monitor for completion are:

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- Polling: To monitor for completion with polling, the status register CMUSTATUSREG[0] BUSY can be read to determine whether any range sets are still in operation, if wanting to wait for all range sets to complete, or poll the CMURANGESTATE_i[31:29] STATE bit field to watch for a particular range set to move to COMPLETE or ERROR state. These states indicate that the range operation completed normally or stopped because of an error, respectively.
- Interrupt: To monitor for completion with interrupt, the CMUOPERATION_i[10:9] COMPLETION bit field must be set to interrupt on completion. The interrupt handler must read the CMUINTRACK_NS[11:0] INDEX bit field to get the range set index of the interrupt-generating cache operation. The status of the completed operation can be read from the range set, particularly the CMURANGESTATE_i[31:29] STATE bit field.

4.3.5.4.5 Freeing a Range Set

When a range set operation completes and software is done examining the completion information, the range set must be freed to allow it to be reallocated. To free a range set, write its index to the CMUDEALLOCATE[7:0] INDEX bit field.

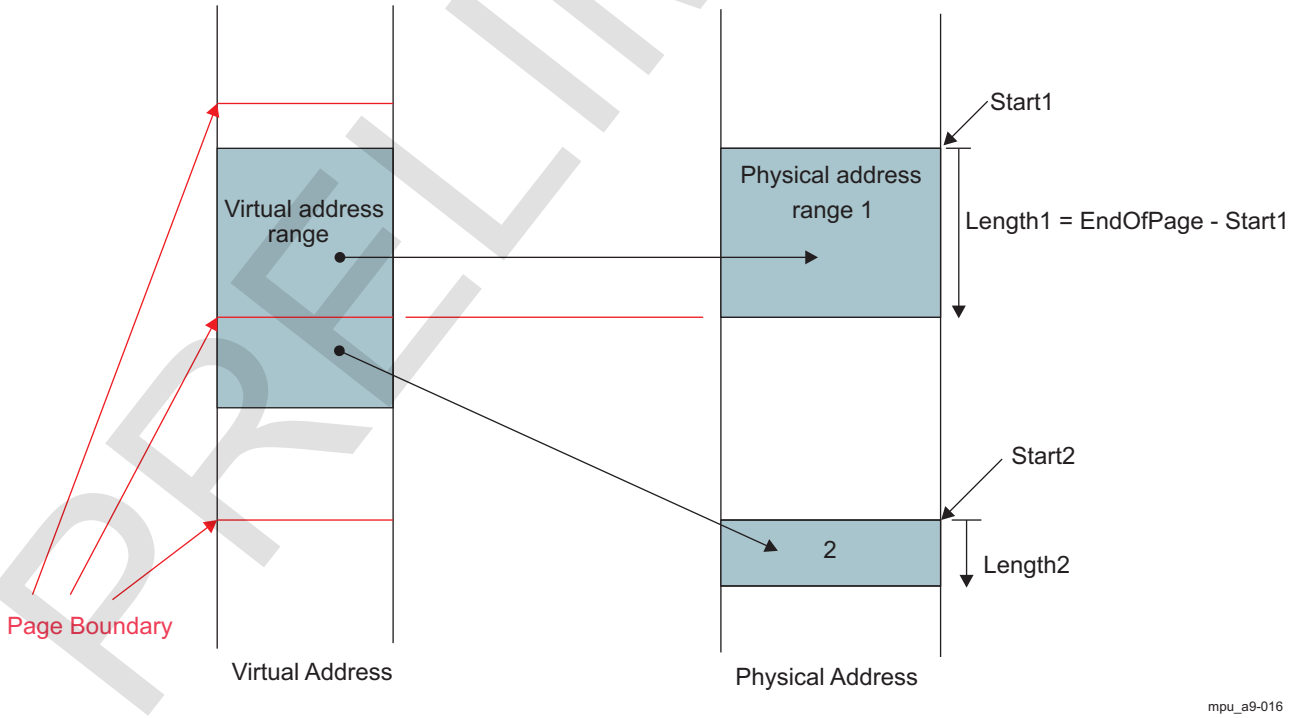
4.3.5.4.6 Paged Memory

Any range more than 1-byte long may span a page boundary. The page mappings for contiguous virtual memory pages may not be contiguous in physical memory. Ranges must end when a page boundary is encountered so each page of the range can be translated separately to physical memory. The software must perform the page mapping (possibly using ARM CP15 operations for that purpose) to produce the physical address needed to program the CMU.

In a paged environment, even a small buffer may cross a page boundary and require two range operations to cover the two parts of the buffer. Two range sets must be used to program the two ranges, each wholly contained within a page.

Figure 4-11 shows this scenario.

Figure 4-11. Range in Paged Virtual Memory



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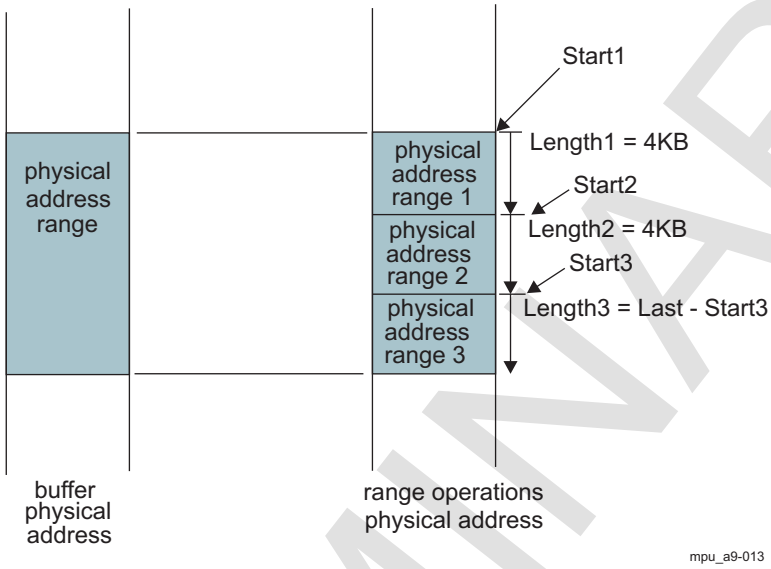
4.3.5.4.7 Large Buffers

Even when a buffer is contiguous in physical memory it may be large enough that it cannot be contained within a range set, because the length is restricted to 4KB.

Figure 4-12 shows the large buffer in physical memory.

Figure 4-12. Large Buffer in Physical Memory



4.3.5.5 Micro-Architecture of CMU

Different range sets can be activated by different masters; therefore, no assumptions must be made regarding the atomicity of range set register programming. The Start PA, length, and operation registers from multiple masters can be interleaved. Multiple range sets can be allocated to different masters and activation of them can be out of order.

Figure 4-13 shows the CMU micro-architecture.

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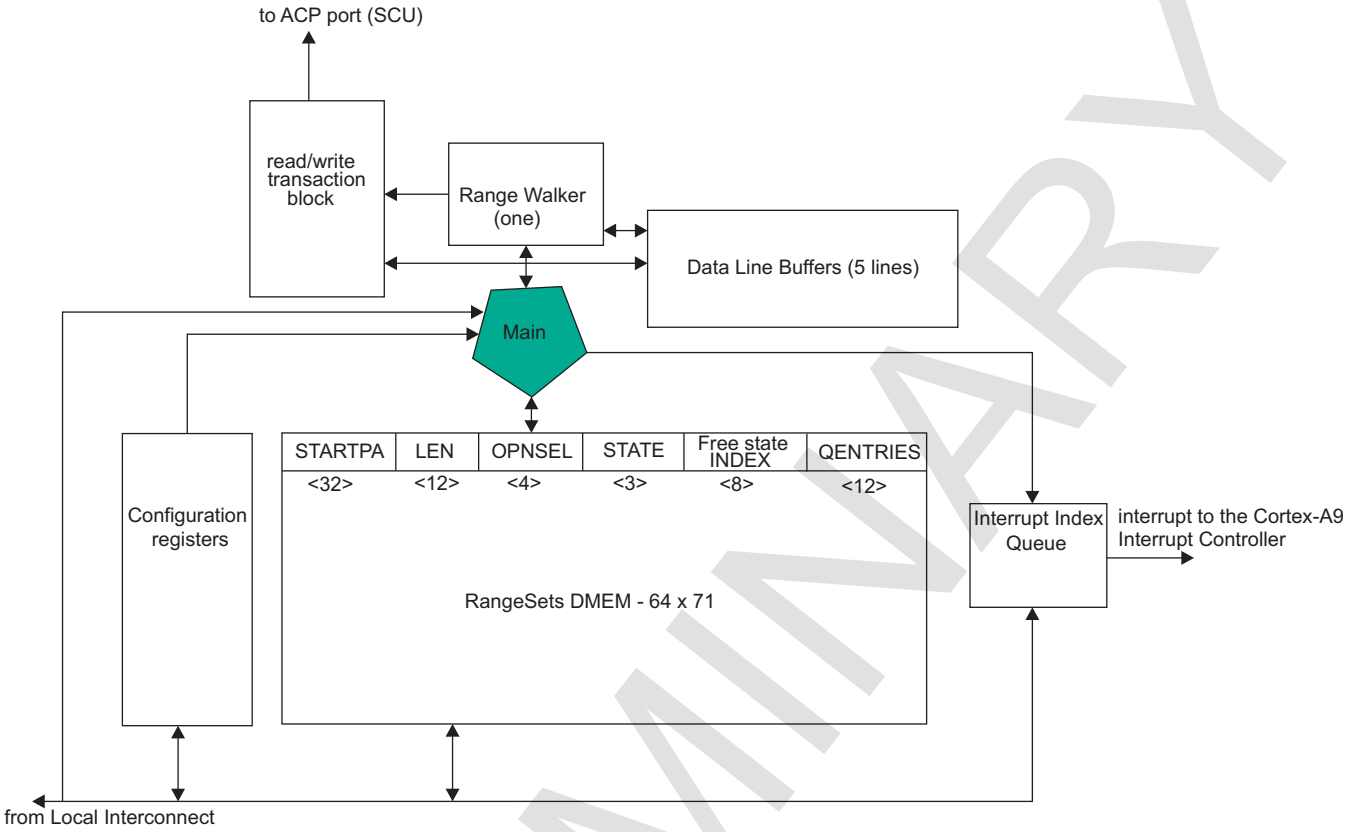
Figure 4-13. CMU Micro-Architecture



4.3.5.5.1 Range Set DMEM

This memory has 64 rows and each row is 71 bits wide.

4.3.5.5.2 Data Line Buffers

The data line buffers hold the read data for the ACP reads that hit in L1 or L2 for clean/clean-invalidate operations. Each line is 32 bytes with a 64-bit interface from ACP. To maintain an optimal throughput, the Cortex-A9 MPU, which has a single range walker, needs at least four line buffers (five line buffers are available).

4.3.5.5.3 Range Walker

The range walker is the block that steps through line steps using STARTPA until reaching STARTPA + LEN. The range walker gets two indices from main control that it uses to access range sets DMEM to get STARTPA, LEN, etc., and then interacts with the read/write transaction block. This block issues ACP reads, ACP writes, etc. for the range.

4.3.5.5.4 Main Control

This is the main controller that coordinates between the various blocks and resolves arbitration conflicts for access to the DMEMs and maintains the free state indices and operation queue pointers.

4.3.5.5.5 Interrupt Index Queue

The Interrupt index queue holds the index of the range set whose operation register CMUOPERATION_i indicates "interrupt on completion." The size is constant and is four entries.

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4.3.5.5.6 Configuration Registers

This block holds all the common configuration registers, such as CMUALLOCATE, CMUDEALLOCATE, and others.

4.3.5.5.7 Read/Write Transaction Block

This is the block that creates the read/write transactions from the range walker into SCU-compatible protocol.

4.3.5.6 Free Set Management, Operation Queue Functionality, and Main Control

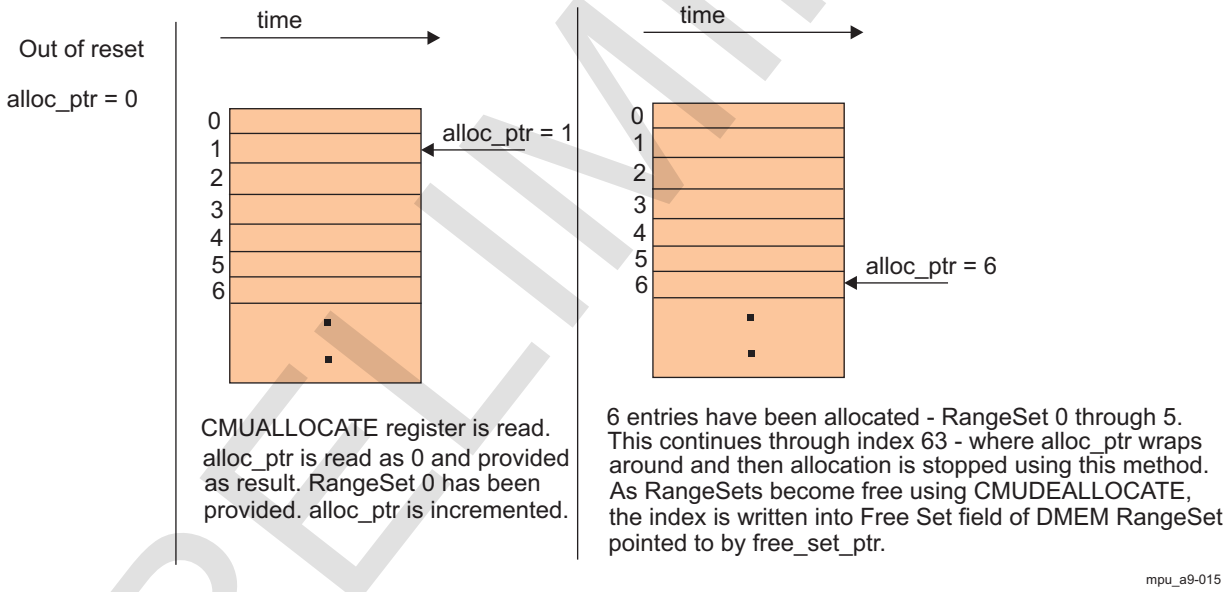
4.3.5.6.1 Allocation and Free Set Management

Using the CMU, the first step to enabling a range set is to read the CMUALLOCATE register. This returns the index of a range set that is in free state. Detecting a free range set is done in the following two ways.

4.3.5.6.1.1 Out of Reset

Two pointers are maintained in main control, alloc_ptr and active_ptr. Both are 0 out of reset. When the CMUALLOCATE register is read, the value of alloc_ptr is returned and then incremented. This continues until alloc_ptr wraps around, which happens when all 64 range sets have been allocated (see Figure 4-14).

Figure 4-14. Free Set Allocation out of Reset



4.3.5.6.1.2 Steady State – Once alloc_ptr Has Wrapped Around

Once alloc_ptr has wrapped around, allocation cannot be based on the out-of-reset way. Allocations must be based on range sets that are free. Range sets can be activated in an order that differs from what was allocated. Software can program activations out of order with respect to allocations. This can happen naturally when there are multiple masters. When the CMUDEALLOCATE register is written, the index pointed to by the register contents is freed. This index is written into the free state INDEX field of the range set DMEM, as pointed to by free_set_ptr, which is then incremented (see Figure 4-15).

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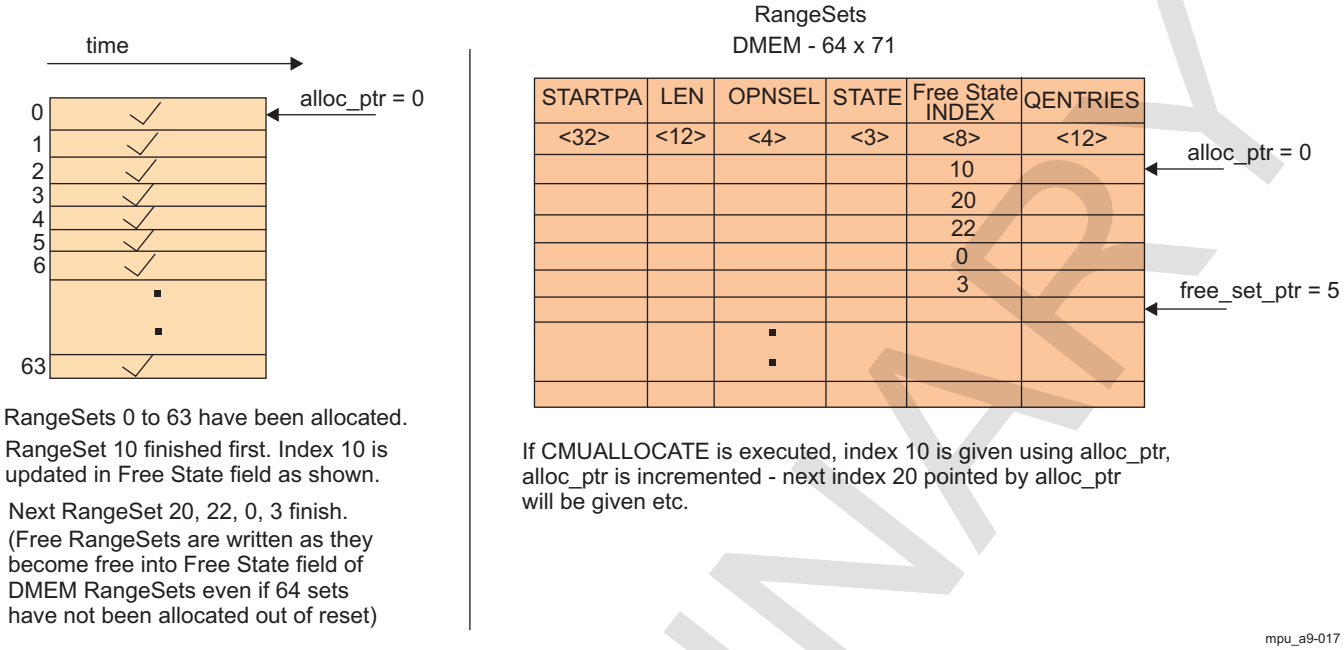
Figure 4-15. Allocation in Steady State



The check mark in each index indicates that the index has been allocated. Figure 4-15 shows a state where all 64 range sets have been allocated. Assume various range sets have been activated. Now, assume that range set 10 becomes free first when software writes to the CMUDEALLOCATE register with index 10. Index 10 is written into the Free State field as pointed to by free_set_ptr, which is 0 out of reset. Next, range sets 20, 22, 0, and 3 are freed. free_set_ptr points to entry 5 as the next entry to be updated when the CMUDEALLOCATE register is written. When a CMUALLOCATE register is read, the DMEM entry pointed to by alloc_ptr is read. The contents of the Free Set field are read (10 is returned to CMUALLOCATE register read). alloc_ptr is then incremented.

4.3.5.6.2 Activation and Operation Queue Functionality

The operation queue stores the indices of the range sets that have been activated. When CMUOPERATION is stored that particular index is activated. The activated index is written into the operation queue (QENTRIES) field of DMEM RangeSets to the address pointed to by active_ptr, which is 0 out of reset (see Figure 4-16).

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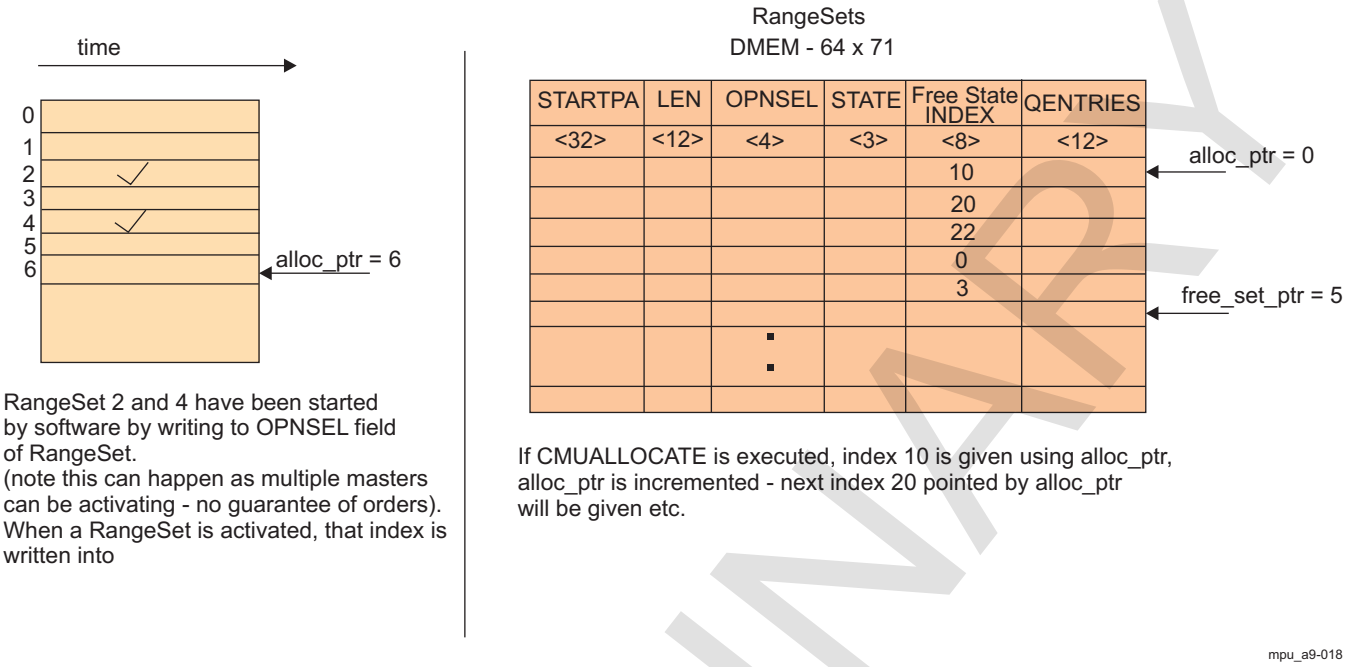
Figure 4-16. Operation Queue Functionality



4.3.5.6.3 Main Control

These pointers are maintained in main control, which is made aware of the range walker. The main control block distributes active_ptr to the range walker. The range walker needs two active_ptr pointers for optimal throughput.

4.3.5.7 Priority of Range Set DMEM Accesses

The following must be the priority of DMEM accesses, from highest to lowest:

1. Interconnect configuration accesses to range sets: Programming range sets, CMUALLOCATE, CMUDEALLOCATE, etc.
2. Range walker access to read range sets and update range set state

Range walker access to read range sets and update states should be less frequent than configuration access. Once the range set is activated, all information necessary for performing operations is kept in local registers.

4.3.5.8 Interrupt Index Queue

When the CMUCONFIGREG_i[8] INTEN bit is set to 1, and if the CMUOPERATION_i[10:9] COMPLETION bit field is configured for interrupt, the index for the completed range set is placed in the interrupt index queue and the CMUINTRACK register is prepared before the interrupt is raised.

Software can read the CMUINTRACK[31] VALID bit and execute the ISR. Once software reads the CMUINTRACK register, the next valid index in the interrupt index queue is updated in the CMUINTRACK register, which software reads after it performs the ISR for the first index. If the VALID bit is 0, because no more entries are in the interrupt index queue, software exits the ISR processing. Hardware also disables the interrupt.

Thus, using one interrupt, ISR for multiple indices can be handled at one time.

The interrupt index queue has only the index and is maintained by pointers.

4.3.5.9 Important Programming Notes for Users of CMU

For optimal performance, software must do the following:

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- The CMUCONFIGREG_i[10] DISABLEPIPELINING and CMUCONFIGREG_i[9] DISABLEPARALLEL bits must be set to 0. These come out of reset as 1, and if not set to 0, they serialize the operation of the CMU and reduce throughput significantly. Disable pipelining must be set to 0 for proper operation and should be used only when bad address programming is suspected; if this bit is set to 1, the CMU will not work.
- The CMUCONFIGREG_i register must be programmed at the beginning or when the CMU is idle. The CMUCONFIGREG_i[3] ENNSWR bit (enable NS write) must be set appropriately so that non-safe programs can write or not write to this register.
- All CMU writes must be done as device writes; otherwise, they are combined in the Cortex-A9 MPU and can become a burst write access, which the local interconnect does not have the logic to split.

NOTE: All interconnect write response errors are imprecise errors when writes are device writes, because they are a bufferable type in PL310. If precise errors are required, writes must be done as strongly ordered writes; however, these are slow and thus should be avoided. Because writes that encounter errors do not occur in the CMU, the effect of imprecise errors is that later instructions to the CMU that depend on earlier writes (that may have encountered an error) would have occurred. Because no such sequences are in the CMU, it should be okay to use device stores. Sequences do exist, however, where CMUALLOCATE read is done and if the read is successful, then a write to RangeSet occurs. However, CMUALLOCATE is a read followed by writes and read errors are always precise. CMUDELLOACTE is a write that may not happen (because of a software error, such as trying to deallocate something that is not complete or if the NS = 1 program is trying to deallocate an NS = 0 RangeSet). Subsequent writes to range sets, however, are protected by a read in between by CMUALLOCATE.

- All CMU reads must be done as device reads.
- Writes to range sets must be done only when CMUALLOCATE read returns a valid range set (CMUALLOCATE); otherwise, an interconnect response error results.
- Writes to free a range set by a DEALLOCATE write must be done only after the status is examined to ensure that the range set is complete (with or without error); otherwise, an interconnect response error (CMUDEALLOCATE) results.
- It is preferable to use interrupt processing rather than polling to determine whether a range set is complete.

4.3.5.10 Notes on Corner Cases – Hardware and Software Notes

- When the ACP performs a read of a line, for example in L1, it uses that data to perform an ACP write for clean/clean-invalidate. If the CPU modifies the data between the ACP read and ACP write, the CPU write is lost. The ACP/CMU has no way to detect this. Semaphores must be used to ensure that the CMU clean/clean-invalidate is started only after the CPU updates the buffer.
- The Cortex-A9 CPUs support prefetching and speculative caching of data into L1 and L2 caches. While CMU operations are in progress, Cortex-A9 may prefetch the data back into L1 and L2 after it has been invalidated; this may be because addresses close to the invalidated range were touched by the CPU. An external master may have updated the address that has been invalidated and for the CPU to see the updated state, the speculatively filled address must be invalidated out of L1/L2. This can be done as an invalidation of the L1/L2 address range just before fetching the updated buffer. Care should be taken to ensure that the CPU is not working on addresses being operated on the CMU.
- CMU data is always dirty; therefore, when data is clean in L1/L2, it still is written to external memory because the CMU data looks like the most recent write to dirty the clean data in L1/L2. Therefore, software must not attempt to start the consumer to consume the data until after the CMU operation has completed a clean or clean-invalidate range.
- Because all of the bytes of the cache lines at the beginning and end of a range are affected by cache maintenance, software must insure that this does not cause unintended effects. The most general solution is to allocate buffers that may be subject to cache maintenance so that they are aligned to a cache line boundary (32 bytes on this device, but for compatibility with old and future devices, 64-byte alignment is suggested). This will prevent unrelated data from sharing a cache line with the beginning of the buffer. In addition, the end of the buffer allocation should also be padded to a cache line

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boundary so that no unrelated data shares the final cache line of the buffer.

- The CMU does not handle wrap-around from a high physical address to a low physical address. Software must not program a CMU range set with a starting address and length that exceeds $2^{32} - 1$. Such a range must be broken into parts so that no single range set is programmed to cross this boundary.

4.3.6 Power Management

- The Cortex-A9 MPU subsystem implemented a local PRCM module to handle the local CPU power domain.
- Support cache retention
- The Cortex-A9 MPU subsystem has six power domains.
- The local PRCM module handles the power management in conjunction with the global PRCM. The local PRCM module has its own registers and is clocked by the system clock, which is the same as the global PRCM.

4.3.6.1 Power Domains

The Cortex-A9 MPU subsystem is divided into six power domains controlled by the local or global PRCM module, as shown in Figure 4-17.

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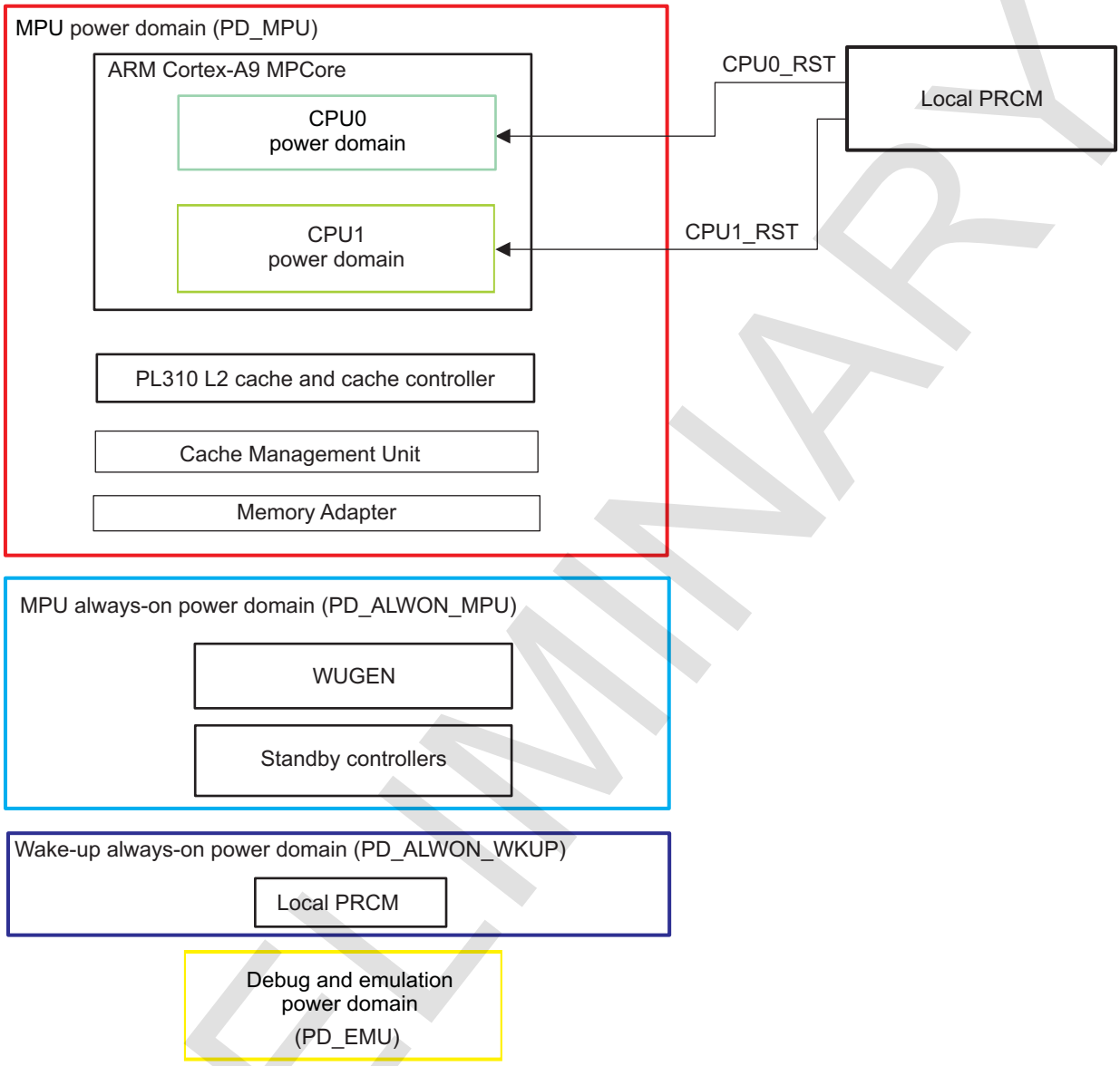
Figure 4-17. Cortex-A9 MPU Subsystem Power Domain Overview



The CPU power domains (CPU0 and CPU1) and L1 cache are controlled by the local PRCM module. The system and emulation power domains (PD_MPU and PD_EMU) are controlled by the global PRCM. The power-management support for debug and emulation is distributed between the local and global PRCM modules.

The Cortex-A9 local PRCM module includes two PSCON modules to control the power chains for CPU0 and CPU1. The PRM_PSCON_COUNT register is used for that control purpose.

To maximize performance and SMP scalability, both CPUs must run at the same frequency. Do not lower the frequency of one CPU as a power-saving option.

The device-level power domains are directly aligned with voltage domains and thus can be represented as a cross-reference to the different voltage domains.

For information about the physical power domains (PD_MPU, PD_EMU, and PD_ALWON_MPU) and the related voltage domains, see Chapter 3, *Power, Reset, and Clock Management.*

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4.3.6.2 Power States of CPU0 and CPU1

CPUx (where x = 0 or 1) changes power states only when the StandbyWFI signal is asserted. The user can check this in the WKG_CONTROL_0/WKG_CONTROL_1[8] STANDBYWFI bit. In conjunction with StandbyWFI, the CPU power state transition is also based on the SCU CPU Power Status register, which software must program before executing the wait for interrupt (WFI) instruction.

Each CPU clock can be gated independently. This clock gating is controlled by several hardware and software conditions.

Clock transition depends on the StandbyWFI assertion + the value of 3 bit fields:

- PWRCTLO from the SCU power status register (internal to ARM)
- CLKTRCTRL from the CM_PDA_CPUi_CLKSTCTRL register (local PRCM module)
- POWERSTATE from the PM_PDA_CPUi_PWRSTCTRL register (local PRCM module)

The power states of both CPUs do not have to be the same. The power state of CPUx can be:

- Normal (run) mode
- Dormant mode
- Power-off mode

Table 4-5 gives details of the power state of the supported CPUx and the corresponding values of the local PRCM register.

Table 4-5. CPUx Supported Power States

Hardware Conditions		CPUx Programming Model				Resulting CPUx State			
StandbyWFI StandbyWFE	**SCU CPUx Power Status**	**Local PRCM Power State PM_PDA_CPUi_PWRSTCTRL[1:0] POWERSTATE**	**Local PRCM Logic Retention State PM_PDA_CPUi_PWRSTCTRL[2] LOGICRETSTATE**	**Local PRCM L1 Cache Memory Retention State PM_PDA_CPUi_PWRSTCTRL[8] L1_BANK_RETSTATE**	**Local PRCM Clock Transition Control CM_PDA_CPUi_CLKSTCTRL[1:0] CLKTRCTRL**	**Logic**	**L1 Cache**	**ARM Cortex-A9 Internal Clock Gating**	**Power State at Local PRCM**
CPUx running[1]	Any	Any	Any	Any	Any	ON	ON	ON	ON
CPUx in WFE[2]	Any	Any	Any	Any	Any	ON	ON	OFF	ON
CPUx in WFI	Normal	Any	Any	Any	NO_SLEEP/SW_WKUP	ON	ON	OFF	ON
		ON	Any	Any	HW_AUTO				
CPUx in WFI	Dormant	RETENTION	Open switch retention (OSW)	RETENTION	HW_AUTO	OFF	RET	OFF	Open switch retention
CPUx in WFI	Power off	OFF	Any	Any	HW_AUTO	OFF	OFF	OFF	OFF

(1) When CPUx is running, no power transition is possible.
(2) When CPUx is in WFE mode, no power transition is possible.

The PM_PDA_CPUi_PWRSTCTRL register is static over any power transition. That is, software programs it before executing the WFI instruction and does not change it until CPUx is again in running mode. In other words, when CPUx reaches a low-power state (DORMANT, POWER OFF), it cannot move to another low-power state. It must be woken up to reach another low-power state. To wake up CPUx, the user must:

1. Execute a forced wake-up transition to the CPUx: CM_PDA_CPUx_CLKSTCTRL[1:0] CLKTRCTRL = 0x2.
2. The CPUx interrupt handler must set back the automatic hardware transition CM_PDA_CPUx_CLKSTCTRL[1:0] CLKTRCTRL = 0x3.

The MPU subsystem power domain (PD_MPU) must be at a higher or equal power state (state that

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consumes more power) than the higher of the two CPUs. For example, it is illegal for the MPU subsystem power state to be OFF, while the power state of one or both of the CPUs is DORMANT. Software must ensure that only legal power states are programmed. When an illegal state is entered, the behavior of the hardware is unpredictable. Do not program the Cortex-A9 MPU in CSWRET, L2$ in OFF, or either or both CPUs in CSWRET.

Table 4-6 lists the MPU power states handled by the local and global PRCM.

Table 4-6. MPU Power States Handled by the Local and Global (Device) PRCM Modules

CPU State at Local PRCM	PRCM Power State	Logic Retention State	L2 Cache Memory Retention State	PRCM Clock Control	Logic Resulting State	L2 Cache Memory Resulting State	DPLL Clock	MPU Power State at PRCM
At least one is ON	**Any**	**Any**	**Any**	**Any**	**ON**	**ON**	**ON**	**ON**
Power state of both CPUs is less than or equal to OSWRET	Any	Any	Any	No sleep/software wakeup	ON	ON	ON	ON
	ON	Any	Any	Hardware auto	ON	ON	ON	ON
	INACTIVE	Any	Any	Hardware auto	ON	ON	OFF	INACTIVE
	RETENTION	CSW	RETENTION	Hardware auto	ON	RETENTION	OFF	CSWRET
Power state of both CPUs is less than or equal to OSWRET	RETENTION	OSW	RETENTION	Hardware auto	OFF	RETENTION	OFF	OSWRET
	RETENTION	OSW	OFF	Hardware auto	OFF	OFF	OFF	OSWRET
Power state of both CPUs is OFF	OFF	Any	Any	Hardware auto	OFF	OFF	OFF	OFF

WFI: State where logic is closed switch, memory is ON, and clock is gated off

DORMANT (for CPU0 or CPU1): State where logic is in opened or closed switch (depending on programming value), memory is in RETENTION, and clock is gated off

ON/OFF (for system logic): State where logic is in opened or closed switch, depending on whether the higher of the two CPU power states is opened or closed switch. For example, if CPU0 is in opened switch dormant mode and CPU1 is in closed switch dormant mode, system logic must be closed switch.

When the Cortex-A9 MPU reaches a low-power state (INACT, CSWRET, OSWRET, OFF), it cannot move to another low-power state. It must be woken up to reach another low-power state.

For the CPU0 and CPU1 power states and power state transitions, see the ARM Cortex-A9 MPCore TRM.

4.3.6.3 WUGEN

The WUGEN belongs to the MPU always-on power domain (PD_ALWON_MPU) and is responsible for generating wake-up events from the incoming interrupts (external and local) according to the enabled bits in the WUGEN registers.

The WUGEN unit has a 128-bit enable field (from WKG_ENB_A_0 to WKG_ENB_D_0 for CPU0 and from WKG_ENB_A_1 to WKG_ENB_D_1 for CPU1) which defines the interrupt that wakes up the corresponding CPU. The enable bits are reset to 0 and can be set to 1 to enable the interrupt to wake up the CPU. All interrupts are enabled after reset, except MA_IRQ_8 (which is not supported by the GP device). The Cortex-A9 MPU can access the WUGEN internal configuration registers through the local interconnect.

Software must program interrupt enabling and disabling coherently in the INTC and in the WUGEN enable registers. That is, a given interrupt for a given CPU is either enabled at both INTC and WUGEN, or disabled at both; no combination is allowed.

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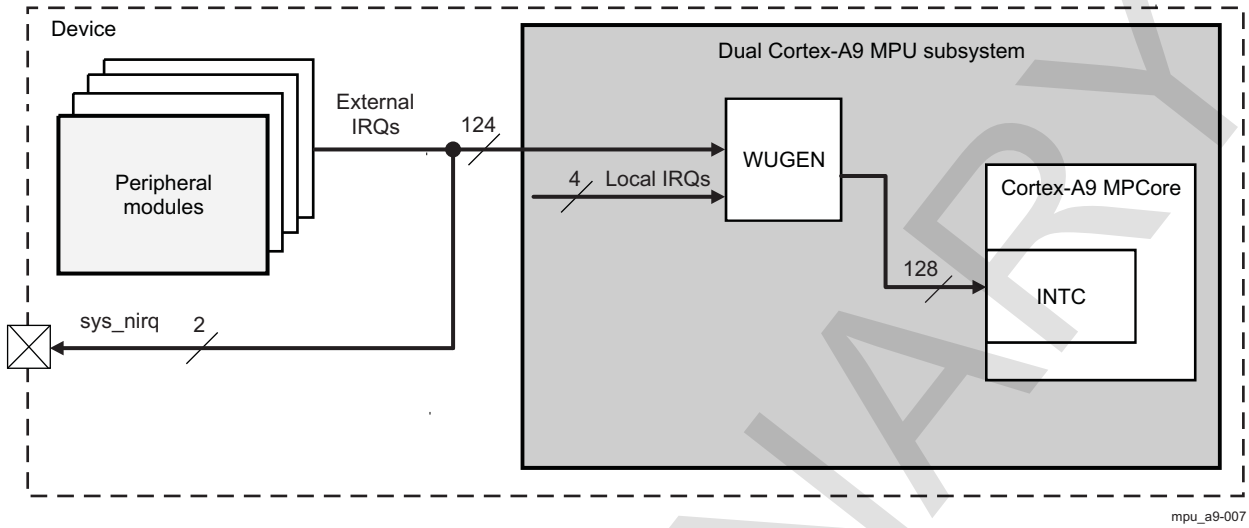
Figure 4-18 is a functional overview of the WUGEN in the Cortex-A9 MPU subsystem.

Figure 4-18. Cortex-A9 MPU Subsystem WUGEN



4.3.6.4 Power Transition Sequence

The three types of power transition sequences are:

- Power transitions that do not involve the local or global PRCM module

  When the CPU enters WFI state, provided the CPU power is not shut down or the DPLL is not gated off, the Cortex-A9 internally gates off the CPU clock and no action is required by local or global PRCM module. When an (enabled) interrupt is received, the Cortex-A9 exits WFI state.

- Power transitions handled by the local PRCM module

  When the CPU enters DORMANT or OFF states, the local PRCM module must participate to perform the power sequencing. If the system power domain remains ON and the DPLL is not gated off, the global PRCM module is not needed. To enable and control the CPU domain power mode transitions, write in the CM_PDA_CPUi_CLKCTRL[1:0] CLKTRCTRL bit field.

- Power transitions handled by the local and global PRCM modules

  When the CPU enters a power state that causes the system power domain to go into WFI, DORMANT, or OFF state, the local and global PRCM modules must be involved in the power transition.

4.3.6.5 CPU0 and CPU1 Power Domains Description

The PD_CPUx (where x = 1 or 2) contains the following reset domains:

- CPU0_RST
- CPU0_PWRON_RST
- CPU1_RST
- CPU1_PWRON_RST

The PD_CPUx contains the following clock domains:

- CD_CPU0
- CD_CPU1

Table 4-7 lists the logic retention capability for each module of the PD_CPUx.

Table 4-7. PD_CPUx Modules Power Attributes

Module	Logic Retention	DFF Context Status	RFF Context Status
CPUx	No	RM_PDA_CPUi_CONTEXT[0] LOSTCONTEXT_DFF	None

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The DFF-based logic is nonretention flip flop. For more information, see Chapter 3, *Power, Reset, and Clock Management*.

4.3.6.5.1 Power Domain Modes

This section describes the various power modes supported by the logic and memory areas of the power domain. It also identifies the software control and associated status bit fields. For a functional description of the power-management architecture of a generic power domain, see , *Power Domain*, in Chapter 3, *Power, Reset, and Clock Management*.

4.3.6.5.1.1 Logic and Memory Area Power Modes

Table 4-8 lists the power modes supported by the logic area of the power domain.

Table 4-8. PD_CPUx Logic Area Power Modes

OFF	RETENTION-OSWR	RETENTION-CSWR	ON-INACTIVE	ON-ACTIVE
Available	Available	Available	Available	Available

Table 4-9 lists the power modes supported by the memory area of the power domain. A memory area power mode is identified with respect to a power state of the power domain. The Logic ON, Logic RETENTION, and Logic OFF columns identify the power states of the power domain. The values in these columns identify the supported power state of the memory area (see the Memory Bank column) or the module memory inside the memory area (see the Module – Memory column).

Table 4-9. PD_CPUx Memory Area Power Modes

Memory Bank	Module – Memory	Logic ON	Logic RETENTION	Logic OFF
CPU0_L1		ON	OFF, RETENTION	OFF
	CPU0–CPU0_L1	always_on	software_control	
CPU1_L1		ON	OFF, RETENTION	OFF
	CPU1–CPU1_L1	always_on	software_control	

4.3.6.5.1.2 Logic and Memory Area Power Modes Control and Status

Table 4-10 lists the power mode controls for the power domain.

Table 4-10. PD_CPUx Power Mode Control Parameters

Parameter Name	Memory Bank	Control Bit Field	Access Type
Memory Area – State Control (Logic in RETENTION state)	CPUx_L1	PM_PDA_CPUi_PWRSTCTRL[8] L1_BANK_RETSTATE	Read only
Memory Area – State Control (Logic in ON state)	CPUx_L1	PM_PDA_CPUi_PWRSTCTRL[17:16] L1_BANK_ONSTATE	Read only
Logic Area – Retention State Control		PM_PDA_CPUi_PWRSTCTRL[2] LOGICRETSTATE	Read/write
Power Domain – State Transition Control		PM_PDA_CPUi_PWRSTCTRL[1:0] POWERSTATE	Read/write

Table 4-11 lists the status of the power modes for the power domain.

Table 4-11. PD_CPUx Power Mode Status Parameters

Parameter Name	Memory Bank	Status Bit Field
Memory Area – State Status	CPUx_L1	PM_PDA_CPUi_PWRSTST[5:4] L1_BANK_STATEST
Power Domain – State Transition Status		PM_PDA_CPUi_PWRSTST[20] INTRANSITION

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Table 4-11. PD_CPUx Power Mode Status Parameters (continued)

Parameter Name	Memory Bank	Status Bit Field
Logic Area – State Status		PM_PDA_CPUi_PWRSTST[2] LOGICSTATEST
Power Domain – State Status		PM_PDA_CPUi_PWRSTST[1:0] POWERSTATEST

Table 4-12 lists the supported clock-management modes and the associated software control bit fields for each module of the power domain.

Table 4-12. Module Clock Management Modes and Control

Module	Clock Management Protocol	Status Bit Field	Role
CPUx	Master/Slave	CM_PDA_CPUi_CLKCTRL[0] STBYST	Standby status

Table 4-13 lists the supported clock-management modes and associated software control bit fields for each module of the power domain.

Table 4-13. Module Slave Clock Management Modes and Control

Module	Disabled	Auto	Enabled	Control Bit Field	Access Type
CPUx	n/a	Available	n/a	CM_PDA_CPUi_CLKSTCTRL[1:0] MODULEMODE	Read/write

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4.4 Dual Cortex-A9 MPU Subsystem Register Manual

4.4.1 Cortex-A9 MPU Subsystem Instance Summary

Table 4-14. Cortex-A9 MPU Instance Summary

Module Name	Base Address	Size
SCU	0x4824 0000	128 bytes
GIC_Proc_Interface[1]	0x4824 0100	256 bytes
Timer	0x4824 0600	256 bytes
GIC_Intr_Distributor[2]	0x4824 1000	4KB
PL310	0x4824 2000	4KB
CORTEXA9_SOCKET_PRCM	0x4824 3000	512 bytes
CORTEXA9_PRM	0x4824 3200	512 bytes
CORTEXA9_CPU0	0x4824 3400	1KB
CORTEXA9_CPU1	0x4824 3800	1KB
CORTEXA9_WUGEN	0x4828 1000	4KB
CMU	0x4829 0000	64KB
Local interconnect	0x482A 0000	4KB
MA	0x482A F000	4KB

(1) Processor interfaces: Handles interrupt acknowledgment, interrupt masking, and interrupt completion acknowledgment
(2) Interrupt distributor: Handles interrupt detection, interrupt prioritization, and distribution of interrupts to the CPUs

4.4.2 SCU Registers

For information about the SCU registers and their description, see the ARM® Cortex™-A9 MPCore Technical Reference Manual .

4.4.3 Interrupt Controller Registers

For information about the GIC registers and their description, see the ARM® Cortex™-A9 MPCore Technical Reference Manual .

4.4.4 Timer Registers

For information about the timer registers and their description, see the ARM® Cortex™-A9 MPCore Technical Reference Manual .

4.4.5 PL310 Registers

For information about the PL310 registers and their description, see the ARM® PL310 Cache Controller Technical Reference Manual .

4.4.6 Local PRCM Revision Register

4.4.6.1 Local PRCM Revision Register Summary

Table 4-15. Local PRCM Revision Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	CORTEXA9_SOCKET_PRCM Base Address
CORTEXA9_PRCM_REVISION	R	32	0x0	0x4824 3000

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4.4.6.2 Local PRCM Revision Register Description

Table 4-16. CORTEXA9_PRCM_REVISION

Address Offset	0x0000 0000		
Physical Address	0x4824 3000	**Instance**	CORTEXA9_SOCKET_PRCM
Description	IP Revision register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP revision	R	TI internal data

Table 4-17. Register Call Summary for Register CORTEXA9_PRCM_REVISION

Dual Cortex-A9 MPU Subsystem Register Manual
- Local PRCM Revision Register Summary: [0]

4.4.7 Local PRCM Registers

4.4.7.1 Local PRCM Register Summary

Table 4-18. Local PRCM Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	CORTEXA9_PRM Base Address
PRM_RSTST	RW	32	0x0000 0000	0x4824 3200
PRM_PSCON_COUNT	RW	32	0x0000 0004	0x4824 3204

4.4.7.2 Local PRCM Log Register Description

Table 4-19. PRM_RSTST

Address Offset	0x0000 0000		
Physical Address	0x4824 3200	**Instance**	CORTEXA9_PRM
Description	This register logs the global reset sources, thus contains information regarding the cold/warm reset events generated by global PRCM. Each bit is set upon release of the domain reset signal. Must be cleared by software.		
Type	RW (W1toClr - write 0x1 to clear the bit)		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														GLOBAL_WARM_RST	GLOBAL_COLD_RST

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Bits	Field Name	Description	Type	Reset
31:2	RESERVED	Reserved	R	0x0000 0000
1	GLOBAL_WARM_RST	Global warm reset event generated by Global PRCM 0x0: No global warm reset. 0x1: Global external warm reset has occurred.	RW W1toClr	0
0	GLOBAL_COLD_RST	Power-on (cold) reset event generated by global PRCM 0x0: No power-on reset. 0x1: Power-on reset has occurred.	RW W1toClr	1

Table 4-20. Register Call Summary for Register PRM_RSTST

Dual Cortex-A9 MPU Subsystem Integration • Reset Distribution: [0] [1]
Dual Cortex-A9 MPU Subsystem Register Manual • Local PRCM Register Summary: [2]

Table 4-21. PRM_PSCON_COUNT

Address Offset	0x0000 0004		
Physical Address	0x4824 3204	**Instance**	CORTEXA9_PRM
Description	Programmable Precharge count for L1Cache. This register is useful to ensure the correct delay between toggles of pscon lines and therefore to avoid Any problem of power switch transitions. The register corresponds to the number of device system clock cycles for the SRAM precharge duration. It means that the local PRCM module waits for PCHARGE_TIME cycles of system clock. The pscon modules belongs to the local PRCM modules and are used to control the power of the CPUx.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPAREUSED				SPARE																				PCHARGE_TIME							

Bits	Field Name	Description	Type	Reset
31:28	SPAREUSED	4 bits consumed for Last Power State Entered	R	0x0
27:8	SPARE	Spare programmable bits	RW	0x00000
7:0	PCHARGE_TIME	Programmable Precharge count during retention	RW	0x17

Table 4-22. Register Call Summary for Register PRM_PSCON_COUNT

Dual Cortex-A9 MPU Subsystem Functional Description • Power Domains: [0]
Dual Cortex-A9 MPU Subsystem Register Manual • Local PRCM Register Summary: [1]

4.4.8 Local PRCM CPU0 and CPU1 Registers

4.4.8.1 Local PRCM CPU0 and CPU1 Register Summary

Table 4-23. Local PRCM CPU0 and CPU1 Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	CORTEXA9_CPU0 Base Address	CORTEXA9_CPU1 Base Address
PM_PDA_CPUi_PWRSTCTRL (1)	RW	32	0x0000 0000	0x4824 3400	0x4824 3800
PM_PDA_CPUi_PWRSTST (1)	RW	32	0x0000 0004	0x4824 3404	0x4824 3804

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Table 4-23. Local PRCM CPU0 and CPU1 Register Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	CORTEXA9_CPU0 Base Address	CORTEXA9_CPU1 Base Address
RM_PDA_CPUi_CONTEXT (1)	RW	32	0x0000 0008	0x4824 3408	0x4824 3808
RM_PDA_CPUi_RSTCTRL (1)	RW	32	0x0000 000C	0x4824 340C	0x4824 380C
RESERVED	R	32	0x0000 0010	0x4824 3410	0x4824 3810
CM_PDA_CPUi_CLKCTRL (1)	R	32	0x0000 0014	0x4824 3414	0x4824 3814
CM_PDA_CPUi_CLKSTCTRL (1)	RW	32	0x0000 0018	0x4824 3418	0x4824 3818

(1) I = 0 or 1

4.4.8.2 Local PRCM CPU0 Register Description

Table 4-24. PM_PDA_CPUi_PWRSTCTRL

Address Offset	0x0000 0000	**Index**	I = 0 to 1
Physical Address	0x4824 3400 0x4824 3800	**Instance**	CORTEXA9_CPU0 CORTEXA9_CPU1
Description	This register controls the CPU domain power state to reach upon a domain sleep transition		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														L1_BANK_ONSTATE		RESERVED							L1_BANK_RETSTATE	RESERVED					LOGICRETSTATE	POWERSTATE	

Bits	Field Name	Description	Type	Reset
31:18	RESERVED	Reserved	R	0x0000
17:16	L1_BANK_ONSTATE	CPU_L1 memory state when domain is ON. Read 0x3: Memory bank is on when the domain is ON.	R	0x3
15:9	RESERVED	Reserved	R	0x00
8	L1_BANK_RETSTATE	CPU L1 memory state when domain is RETENTION state. Read 0x1: Memory bank is retained when domain is in RETENTION state.	R	1
7:3	RESERVED	Reserved	R	0x0
2	LOGICRETSTATE	Logic state control when power domain is RETENTION 0x0: All CPU logic is off when the domain is in RETENTION state. 0x1: Whole logic is retained when domain is in RETENTION state.	RW	1
1:0	POWERSTATE	Power state control 0x0: OFF state 0x1: RETENTION state 0x2: INACTIVE state 0x3: ON State	RW	0x2

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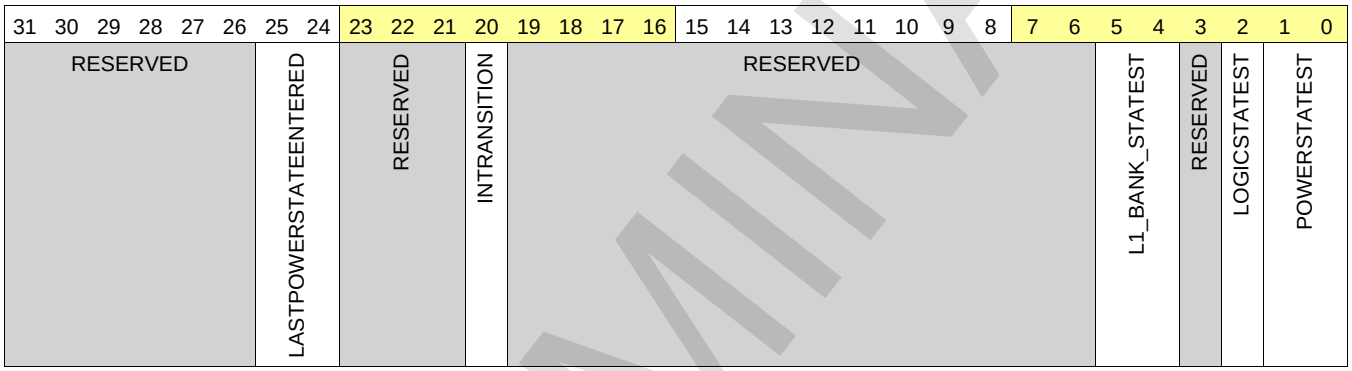
Table 4-25. Register Call Summary for Register PM_PDA_CPUi_PWRSTCTRL

Dual Cortex-A9 MPU Subsystem Functional Description
- Power States of CPU0 and CPU1: [0] [1] [2] [3] [4]
- Power Domain Modes: [5] [6] [7] [8]

Dual Cortex-A9 MPU Subsystem Register Manual
- Local PRCM CPU0 and CPU1 Register Summary: [9]
- Local PRCM CPU0 Register Description: [10]

Table 4-26. PM_PDA_CPUi_PWRSTST

Address Offset	0x0000 0004	**Index**	I = 0 to 1
Physical Address	0x4824 3404 0x4824 3804	**Instance**	CORTEXA9_CPU0 CORTEXA9_CPU1
Description	This register provides a status on the CPU domain current power state. [warm reset insensitive]		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:26	RESERVED	Reserved	R	0x000
25:24	LASTPOWERSTATEENTERED	Last low power state entered. The software has to write 0x3 in this field to update this register. 0x0: Power domain was previously in OFF 0x1: Power domain was previously in RETENTION 0x2: Power domain was previously INACTIVE 0x3: Power domain was previously ON	RW W1toSet	0x0
23:21	RESERVED	Reserved	R	0x0
20	INTRANSITION	Domain transition status Read 0x0: No ongoing transition on power domain Read 0x1: Power domain transition is in progress.	R	0
19:6	RESERVED	Reserved	R	0x0000
5:4	L1_BANK_STATEST	CPU_L1 memory state status Read 0x0: Memory is OFF Read 0x1: Memory is RET Read 0x2: Reserved Read 0x3: Memory is ON	R	0x3
3	RESERVED	Reserved	R	0
2	LOGICSTATEST	Logic state status Read 0x0: Logic in domain is OFF Read 0x1: Logic in domain is ON	R	1

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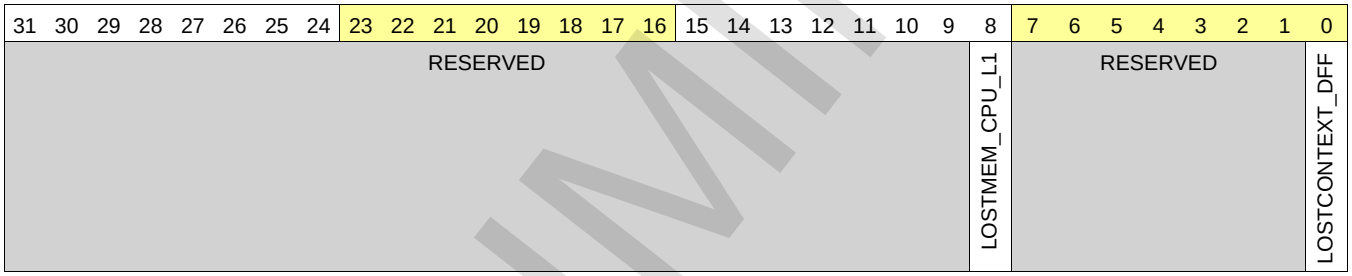
Bits	Field Name	Description	Type	Reset
1:0	POWERSTATEST	Current power state status Read 0x0: Power domain is OFF Read 0x1: Power domain is in RETENTION Read 0x2: Power domain is ON-INACTIVE Read 0x3: Power domain is ON-ACTIVE	R	0x3

Table 4-27. Register Call Summary for Register PM_PDA_CPUi_PWRSTST

Dual Cortex-A9 MPU Subsystem Functional Description • Power Domain Modes: [0] [1] [2] [3]
Dual Cortex-A9 MPU Subsystem Register Manual • Local PRCM CPU0 and CPU1 Register Summary: [4]

Table 4-28. RM_PDA_CPUi_CONTEXT

Address Offset	0x0000 0008	**Index**	I = 0 to 1
Physical Address	0x4824 3408 0x4824 3808	**Instance**	CORTEXA9_CPU0 CORTEXA9_CPU1
Description	This register contains dedicated CPU context statuses. [warm reset insensitive]		
Type	RW (W1toClr - write 0x1 to clear the bit)		



Bits	Field Name	Description	Type	Reset
31:9	RESERVED	Reserved	R	0x000000
8	LOSTMEM_CPU_L1	Specify if memory-based context in CPU_L1 memory bank has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
7:1	RESERVED	Reserved	R	0x00
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 4-29. Register Call Summary for Register RM_PDA_CPUi_CONTEXT

Dual Cortex-A9 MPU Subsystem Functional Description • CPU0 and CPU1 Power Domains Description: [0]
Dual Cortex-A9 MPU Subsystem Register Manual • Local PRCM CPU0 and CPU1 Register Summary: [1]

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Table 4-30. RM_PDA_CPUi_RSTCTRL

Address Offset	0x0000 000C	**Index**	I = 0 to 1
Physical Address	0x4824 340C 0x4824 380C	**Instance**	CORTEXA9_CPU0 CORTEXA9_CPU1
Description	This register controls the assertion/release of the CPU CORE reset. This is basically a software warm reset (that asserts CPUx_RST) per CPU. One CPU can set this bit to reset the other CPU. Actually the CPU can set this bit to reset itself as well (and it will be kept in reset until the other active CPU clears this bit).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															RST

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	RST	CPU warm local reset control 0x0: Reset is cleared 0x1: Reset is asserted	RW	0

Table 4-31. Register Call Summary for Register RM_PDA_CPUi_RSTCTRL

Dual Cortex-A9 MPU Subsystem Integration
- Reset Distribution: [0]

Dual Cortex-A9 MPU Subsystem Register Manual
- Local PRCM CPU0 and CPU1 Register Summary: [1]

Table 4-32. CM_PDA_CPUi_CLKCTRL

Address Offset	0x0000 0014	**Index**	I = 0 to 1
Physical Address	0x4824 3414 0x4824 3814	**Instance**	CORTEXA9_CPU0 CORTEXA9_CPU1
Description	This register manages the CPU clocks.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															STBYST

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	STBYST	Module standby status. [warm reset insensitive] Read 0x0: Module is functional (not in standby) Read 0x1: Module is in standby	R	1

Table 4-33. Register Call Summary for Register CM_PDA_CPUi_CLKCTRL

Dual Cortex-A9 MPU Subsystem Functional Description
- Power Transition Sequence: [0]
- Power Domain Modes: [1]

Dual Cortex-A9 MPU Subsystem Register Manual
- Local PRCM CPU0 and CPU1 Register Summary: [2]

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Table 4-34. CM_PDA_CPUi_CLKSTCTRL

Address Offset	0x0000 0018	**Index**	I = 0 to 1
Physical Address	0x4824 3418 0x4824 3818	**Instance**	CORTEXA9_CPU0 CORTEXA9_CPU1
Description	This register enables the CPU domain power state transition. It controls the hardware-supervised domain power state transition between ON-ACTIVE and ON-INACTIVE states. It also holds 1 status bit per clock input of the domain.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														CLKTRCTRL	

Bits	Field Name	Description	Type	Reset
31:2	RESERVED	Reserved	R	0x0000 0000
1:0	CLKTRCTRL	Controls the full domain transition of the CPU domain. 0x0: NO_SLEEP: Sleep transition cannot be initiated. Wake-up transition may however occur. Read 0x1: Reserved 0x2: Start a software forced wake-up transition on the domain. The software forced wake-up transition allows the software to wakeup a powered-down CPU by a method other than an externally triggered interrupt. 0x3: HW_AUTO: Automatic transition is enabled. Sleep and wake-up transition are based upon hardware conditions. WFI triggers the sleep transition based on settings in CM_PDA_CPUi_CLKSTCTRL and PM_PDA_CPUi_PWRSTCTRL registers.	RW	0x0

Table 4-35. Register Call Summary for Register CM_PDA_CPUi_CLKSTCTRL

Dual Cortex-A9 MPU Subsystem Functional Description
- Power States of CPU0 and CPU1: [0] [1]
- Power Domain Modes: [2]

Dual Cortex-A9 MPU Subsystem Register Manual
- Local PRCM CPU0 and CPU1 Register Summary: [3]
- Local PRCM CPU0 Register Description: [4]

4.4.9 Wake-Up Generator Registers

4.4.9.1 CORTEXA9_WUGEN Register Summary

Table 4-36. CORTEXA9_WUGEN Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	Base Address
WKG_CONTROL_0	R	32	0x0000 0000	0x4828 1000
WKG_ENB_A_0	RW	32	0x0000 0010	0x4828 1010
WKG_ENB_B_0	RW	32	0x0000 0014	0x4828 1014
WKG_ENB_C_0	RW	32	0x0000 0018	0x4828 1018
WKG_ENB_D_0	RW	32	0x0000 001C	0x4828 101C
RESERVED	R	32	0x0000 0020	0x4828 1020
RESERVED	R	32	0x0000 0024	0x4828 1024

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Table 4-36. CORTEXA9_WUGEN Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	Base Address
RESERVED	R	32	0x0000 0028	0x4828 1028
RESERVED	R	32	0x0000 002C	0x4828 102C
WKG_CONTROL_1	R	32	0x0000 0400	0x4828 1400
WKG_ENB_A_1	RW	32	0x0000 0410	0x4828 1410
WKG_ENB_B_1	RW	32	0x0000 0414	0x4828 1414
WKG_ENB_C_1	RW	32	0x0000 0418	0x4828 1418
WKG_ENB_D_1	RW	32	0x0000 041C	0x4828 141C
RESERVED	R	32	0x0000 0420	0x4828 1420
RESERVED	R	32	0x0000 0424	0x4828 1424
RESERVED	R	32	0x0000 0428	0x4828 1428
RESERVED	R	32	0x0000 042C	0x4828 142C
AUX_CORE_BOOT_0	RW	32	0x0000 0800	0x4828 1800
AUX_CORE_BOOT_1	RW	32	0x0000 0804	0x4828 1804
RESERVED	R	32	0x0000 0C00	0x4828 1C00
RESERVED	R	32	0x0000 0C04	0x4828 1C04
RESERVED	R	32	0x0000 0C08	0x4828 1C08
RESERVED	R	32	0x0000 0C0C	0x4828 1C0C

4.4.9.2 CORTEXA9_WUGEN Register Description

Table 4-37. WKG_CONTROL_0

Address Offset	0x0000 0000		
Physical Address	0x4828 1000	**Instance**	CORTEXA9_WUGEN
Description	Wake-up generator status register for CPU0		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																DOMAIN_RST	CORTEXA9_WARM_RST	CORTEXA9_COLD_RST	WDT_RST	RESERVED	EVENTO	STANDBYWFE	STANDBYWFI	RESERVED							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x00000
15	DOMAIN_RST	MPU always-on power domain (PD_ALWON_MPU) reset status bit. It shows if the reset occurred previously. 0x0: no reset occur 0x1: reset occur	R	0
14	CORTEXA9_WARM_RST	This bit is set when the CORTEXA9_RSTN signal is asserted. 0x0: CORTEXA9_RSTN reset signal has not been asserted 0x1: CORTEXA9_RSTN reset request has been asserted	R	0

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Bits	Field Name	Description	Type	Reset
13	CORTEXA9_COLD_RST	This bit is set when the CORTEXA9_PWRON_RSTN signal is asserted. 0x0: CORTEXA9_PWRON_RSTN reset signal has not been asserted 0x1: CORTEXA9_PWRON_RSTN reset request has been asserted	R	0
12	WDT_RST	This bit is set when the WD timer Reset Request signal from the SCU is asserted. 0x0: WDT reset request has not been asserted 0x1: WDT reset request has been asserted	R	0
11	RESERVED	Reserved	R	0
10	EVENTO	EVENTO status bit. The event output signal is active, when one SEV instruction is executed. This bit is set when a rising edge of EVENTO from CPU is detected. 0x0: Rising edge of EVENTO is not detected 0x1: Rising edge of EVENTO is detected	R	0
9	STANDBYWFE	This bit gives software the visibility to track whether WFE mode have been entered. 0x0: WFE mode has not been entered 0x1: WFE mode has been entered	R	0
8	STANDBYWFI	This bit gives software the visibility to track whether WFI mode have been entered. 0x0: WFI mode has not been entered 0x1: WFI mode has been entered	R	0
7:0	RESERVED	Reserved	R	0

Table 4-38. Register Call Summary for Register WKG_CONTROL_0

Dual Cortex-A9 MPU Subsystem Integration • Reset Distribution: [0]
Dual Cortex-A9 MPU Subsystem Functional Description • Power States of CPU0 and CPU1: [1]
Dual Cortex-A9 MPU Subsystem Register Manual • CORTEXA9_WUGEN Register Summary: [2]

Table 4-39. WKG_ENB_A_0

Address Offset	0x0000 0010		
Physical Address	0x4828 1010	**Instance**	CORTEXA9_WUGEN
Description	This register enables the interrupts (for CPU0) from MA_IRQ_0 to MA_IRQ_31 write 0x0: disable interrupt write 0x1: enable interrupt		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WKG_ENB_FOR_INTR31	WKG_ENB_FOR_INTR30	WKG_ENB_FOR_INTR29	WKG_ENB_FOR_INTR28	WKG_ENB_FOR_INTR27	WKG_ENB_FOR_INTR26	WKG_ENB_FOR_INTR25	WKG_ENB_FOR_INTR24	WKG_ENB_FOR_INTR23	WKG_ENB_FOR_INTR22	WKG_ENB_FOR_INTR21	WKG_ENB_FOR_INTR20	WKG_ENB_FOR_INTR19	WKG_ENB_FOR_INTR18	WKG_ENB_FOR_INTR17	WKG_ENB_FOR_INTR16	WKG_ENB_FOR_INTR15	WKG_ENB_FOR_INTR14	WKG_ENB_FOR_INTR13	WKG_ENB_FOR_INTR12	WKG_ENB_FOR_INTR11	WKG_ENB_FOR_INTR10	WKG_ENB_FOR_INTR9	RESERVED	WKG_ENB_FOR_INTR7	WKG_ENB_FOR_INTR6	RESERVED	WKG_ENB_FOR_INTR4	RESERVED	WKG_ENB_FOR_INTR2	WKG_ENB_FOR_INTR1	WKG_ENB_FOR_INTR0

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Bits	Field Name	Description	Type	Reset
31	WKG_ENB_FOR_INTR31		RW	1
30	WKG_ENB_FOR_INTR30		RW	1
29	WKG_ENB_FOR_INTR29		RW	1
28	WKG_ENB_FOR_INTR28		RW	1
27	WKG_ENB_FOR_INTR27		RW	1
26	WKG_ENB_FOR_INTR26		RW	1
25	WKG_ENB_FOR_INTR25		RW	1
24	WKG_ENB_FOR_INTR24		RW	1
23	WKG_ENB_FOR_INTR23		RW	1
22	WKG_ENB_FOR_INTR22		RW	1
21	WKG_ENB_FOR_INTR21		RW	1
20	WKG_ENB_FOR_INTR20		RW	1
19	WKG_ENB_FOR_INTR19		RW	1
18	WKG_ENB_FOR_INTR18		RW	1
17	WKG_ENB_FOR_INTR17		RW	1
16	WKG_ENB_FOR_INTR16		RW	1
15	WKG_ENB_FOR_INTR15		RW	1
14	WKG_ENB_FOR_INTR14		RW	1
13	WKG_ENB_FOR_INTR13		RW	1
12	WKG_ENB_FOR_INTR12		RW	1
11	WKG_ENB_FOR_INTR11		RW	1
10	WKG_ENB_FOR_INTR10		RW	1
9	WKG_ENB_FOR_INTR9		RW	1
8	RESERVED		R	0[(1)]
7	WKG_ENB_FOR_INTR7		RW	1
6	WKG_ENB_FOR_INTR6		RW	1
5	RESERVED		R	1
4	WKG_ENB_FOR_INTR4		RW	1
3	RESERVED		R	1
2	WKG_ENB_FOR_INTR2		RW	1
1	WKG_ENB_FOR_INTR1		RW	1
0	WKG_ENB_FOR_INTR0		RW	1

(1) The reset value is 0x0 by safety reasons.

Table 4-40. Register Call Summary for Register WKG_ENB_A_0

Dual Cortex-A9 MPU Subsystem Functional Description • WUGEN: [0]
Dual Cortex-A9 MPU Subsystem Register Manual • CORTEXA9_WUGEN Register Summary: [1]

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Table 4-41. WKG_ENB_B_0

Address Offset	0x0000 0014		
Physical Address	0x4828 1014	**Instance**	CORTEXA9_WUGEN
Description	This register enables the interrupts (for CPU0) from MA_IRQ_32 to MA_IRQ_63 write 0x0: disable interrupt write 0x1: enable interrupt		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	WKG_ENB_FOR_INTR62	WKG_ENB_FOR_INTR61	RESERVED	WKG_ENB_FOR_INTR59	WKG_ENB_FOR_INTR58	WKG_ENB_FOR_INTR57	WKG_ENB_FOR_INTR56	RESERVED	RESERVED	WKG_ENB_FOR_INTR53	RESERVED	RESERVED	RESERVED	RESERVED	WKG_ENB_FOR_INTR48	WKG_ENB_FOR_INTR47	WKG_ENB_FOR_INTR46	WKG_ENB_FOR_INTR45	WKG_ENB_FOR_INTR44	WKG_ENB_FOR_INTR43	WKG_ENB_FOR_INTR42	WKG_ENB_FOR_INTR41	WKG_ENB_FOR_INTR40	WKG_ENB_FOR_INTR39	WKG_ENB_FOR_INTR38	WKG_ENB_FOR_INTR37	WKG_ENB_FOR_INTR36	RESERVED	WKG_ENB_FOR_INTR34	WKG_ENB_FOR_INTR33	WKG_ENB_FOR_INTR32

Bits	Field Name	Description	Type	Reset
31	RESERVED		R	1
30	WKG_ENB_FOR_INTR62		RW	1
29	WKG_ENB_FOR_INTR61		RW	1
28	RESERVED		R	1
27	WKG_ENB_FOR_INTR59		RW	1
26	WKG_ENB_FOR_INTR58		RW	1
25	WKG_ENB_FOR_INTR57		RW	1
24	WKG_ENB_FOR_INTR56		RW	1
23	RESERVED		R	1
22	RESERVED		R	1
21	WKG_ENB_FOR_INTR53		RW	1
20	RESERVED		R	1
19	RESERVED		R	1
18	RESERVED		R	1
17	RESERVED		R	1
16	WKG_ENB_FOR_INTR48		RW	1
15	WKG_ENB_FOR_INTR47		RW	1
14	WKG_ENB_FOR_INTR46		RW	1
13	WKG_ENB_FOR_INTR45		RW	1
12	WKG_ENB_FOR_INTR44		RW	1
11	WKG_ENB_FOR_INTR43		RW	1
10	WKG_ENB_FOR_INTR42		RW	1
9	WKG_ENB_FOR_INTR41		RW	1
8	WKG_ENB_FOR_INTR40		RW	1
7	WKG_ENB_FOR_INTR39		RW	1
6	WKG_ENB_FOR_INTR38		RW	1
5	WKG_ENB_FOR_INTR37		RW	1
4	WKG_ENB_FOR_INTR36		RW	1
3	RESERVED		R	1
2	WKG_ENB_FOR_INTR34		RW	1
1	WKG_ENB_FOR_INTR33		RW	1
0	WKG_ENB_FOR_INTR32		RW	1

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Table 4-42. Register Call Summary for Register WKG_ENB_B_0

Dual Cortex-A9 MPU Subsystem Register Manual

- CORTEXA9_WUGEN Register Summary: [0]

Table 4-43. WKG_ENB_C_0

Address Offset	0x0000 0018		
Physical Address	0x4828 1018	**Instance**	CORTEXA9_WUGEN
Description	This register enables the interrupts (for CPU0) from MA_IRQ_64 to MA_IRQ_95 write 0x0: disable interrupt write 0x1: enable interrupt		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	WKG_ENB_FOR_INTR94	WKG_ENB_FOR_INTR93	WKG_ENB_FOR_INTR92	WKG_ENB_FOR_INTR91	WKG_ENB_FOR_INTR90	WKG_ENB_FOR_INTR89	WKG_ENB_FOR_INTR88	WKG_ENB_FOR_INTR87	WKG_ENB_FOR_INTR86	RESERVED	WKG_ENB_FOR_INTR84	WKG_ENB_FOR_INTR83	RESERVED	RESERVED	WKG_ENB_FOR_INTR80	RESERVED	WKG_ENB_FOR_INTR78	WKG_ENB_FOR_INTR77	WKG_ENB_FOR_INTR76	WKG_ENB_FOR_INTR75	WKG_ENB_FOR_INTR74	WKG_ENB_FOR_INTR73	WKG_ENB_FOR_INTR72	WKG_ENB_FOR_INTR71	WKG_ENB_FOR_INTR70	WKG_ENB_FOR_INTR69	WKG_ENB_FOR_INTR68	WKG_ENB_FOR_INTR67	WKG_ENB_FOR_INTR66	WKG_ENB_FOR_INTR65	RESERVED

Bits	Field Name	Description	Type	Reset
31	RESERVED		R	1
30	WKG_ENB_FOR_INTR94		RW	1
29	WKG_ENB_FOR_INTR93		RW	1
28	WKG_ENB_FOR_INTR92		RW	1
27	WKG_ENB_FOR_INTR91		RW	1
26	WKG_ENB_FOR_INTR90		RW	1
25	WKG_ENB_FOR_INTR89		RW	1
24	WKG_ENB_FOR_INTR88		RW	1
23	WKG_ENB_FOR_INTR87		RW	1
22	WKG_ENB_FOR_INTR86		RW	1
21	RESERVED		R	1
20	WKG_ENB_FOR_INTR84		RW	1
19	WKG_ENB_FOR_INTR83		RW	1
18	RESERVED		R	1
17	RESERVED		R	1
16	WKG_ENB_FOR_INTR80		RW	1
15	RESERVED		R	1
14	WKG_ENB_FOR_INTR78		RW	1
13	WKG_ENB_FOR_INTR77		RW	1
12	WKG_ENB_FOR_INTR76		RW	1
11	WKG_ENB_FOR_INTR75		RW	1
10	WKG_ENB_FOR_INTR74		RW	1
9	WKG_ENB_FOR_INTR73		RW	1
8	WKG_ENB_FOR_INTR72		RW	1
7	WKG_ENB_FOR_INTR71		RW	1
6	WKG_ENB_FOR_INTR70		RW	1
5	WKG_ENB_FOR_INTR69		RW	1

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Bits	Field Name	Description	Type	Reset
4	WKG_ENB_FOR_INTR68		RW	1
3	WKG_ENB_FOR_INTR67		RW	1
2	WKG_ENB_FOR_INTR66		RW	1
1	WKG_ENB_FOR_INTR65		RW	1
0	RESERVED		R	1

Table 4-44. Register Call Summary for Register WKG_ENB_C_0

Dual Cortex-A9 MPU Subsystem Register Manual
- CORTEXA9_WUGEN Register Summary: [0]

Table 4-45. WKG_ENB_D_0

Address Offset	0x0000 001C		
Physical Address	0x4828 101C	**Instance**	CORTEXA9_WUGEN
Description	This register enables the interrupts (for CPU0) from MA_IRQ_96 to MA_IRQ_127 write 0x0: disable interrupt write 0x1: enable interrupt		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	WKG_ENB_FOR_INTR120	WKG_ENB_FOR_INTR119	RESERVED	RESERVED	RESERVED	RESERVED	WKG_ENB_FOR_INTR114	WKG_ENB_FOR_INTR113	WKG_ENB_FOR_INTR112	WKG_ENB_FOR_INTR111	WKG_ENB_FOR_INTR110	WKG_ENB_FOR_INTR109	RESERVED	WKG_ENB_FOR_INTR107	RESERVED	RESERVED	WKG_ENB_FOR_INTR104	WKG_ENB_FOR_INTR103	WKG_ENB_FOR_INTR102	WKG_ENB_FOR_INTR101	WKG_ENB_FOR_INTR100	WKG_ENB_FOR_INTR99	WKG_ENB_FOR_INTR98	WKG_ENB_FOR_INTR97	WKG_ENB_FOR_INTR96

Bits	Field Name	Description	Type	Reset
31	RESERVED		R	1
30	RESERVED		R	1
29	RESERVED		R	1
28	RESERVED		R	1
27	RESERVED		R	1
26	RESERVED		R	1
25	RESERVED		R	1
24	WKG_ENB_FOR_INTR120		RW	1
23	WKG_ENB_FOR_INTR119		RW	1
22	RESERVED		R	1
21	RESERVED		R	1
20	RESERVED		R	1
19	RESERVED		R	1
18	WKG_ENB_FOR_INTR114		RW	1
17	WKG_ENB_FOR_INTR113		RW	1
16	WKG_ENB_FOR_INTR112		RW	1
15	WKG_ENB_FOR_INTR111		RW	1
14	WKG_ENB_FOR_INTR110		RW	1
13	WKG_ENB_FOR_INTR109		RW	1
12	RESERVED		R	1

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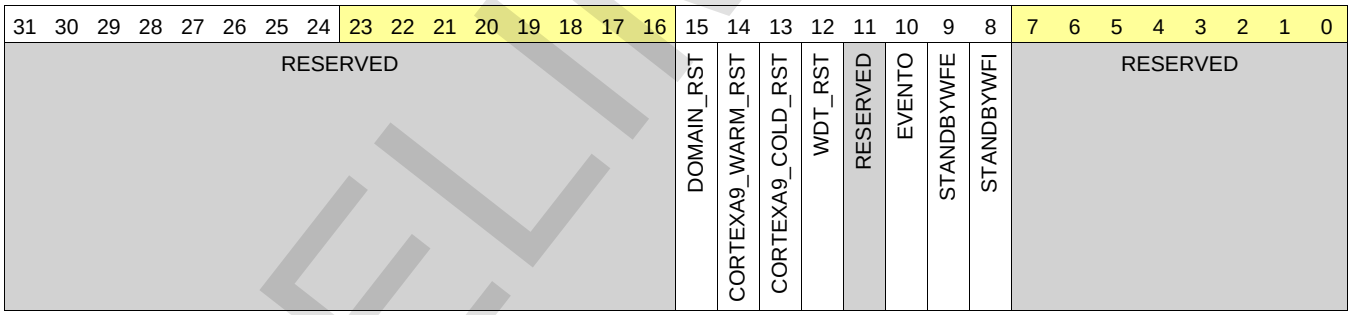
Bits	Field Name	Description	Type	Reset
11	WKG_ENB_FOR_INTR107		RW	1
10	RESERVED		R	1
9	RESERVED		R	1
8	WKG_ENB_FOR_INTR104		RW	1
7	WKG_ENB_FOR_INTR103		RW	1
6	WKG_ENB_FOR_INTR102		RW	1
5	WKG_ENB_FOR_INTR101		RW	1
4	WKG_ENB_FOR_INTR100		RW	1
3	WKG_ENB_FOR_INTR99		RW	1
2	WKG_ENB_FOR_INTR98		RW	1
1	WKG_ENB_FOR_INTR97		RW	1
0	WKG_ENB_FOR_INTR96		RW	1

Table 4-46. Register Call Summary for Register WKG_ENB_D_0

Dual Cortex-A9 MPU Subsystem Functional Description • WUGEN: [0]
Dual Cortex-A9 MPU Subsystem Register Manual • CORTEXA9_WUGEN Register Summary: [1]

Table 4-47. WKG_CONTROL_1

Address Offset	0x0000 0400		
Physical Address	0x4828 1400	**Instance**	CORTEXA9_WUGEN
Description	Wake-up generator status register for CPU1		
Type	R		



Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x00000
15	DOMAIN_RST	MPU always-on power domain (PD_ALWON_MPU) reset status bit. It shows if the reset occurred previously. 0x0: no reset occur 0x1: reset occur	R	0
14	CORTEXA9_WARM_RST	This bit is set when the CORTEXA9_RSTN signal is asserted. 0x0: CORTEXA9_RSTN reset signal has not been asserted 0x1: CORTEXA9_RSTN reset request has been asserted	R	0
13	CORTEXA9_COLD_RST	This bit is set when the CORTEXA9_PWRON_RSTN signal is asserted. 0x0: CORTEXA9_PWRON_RSTN reset signal has not been asserted 0x1: CORTEXA9_PWRON_RSTN reset request has been asserted	R	0

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Bits	Field Name	Description	Type	Reset
12	WDT_RST	This bit is set when the WD timer Reset Request signal from the SCU is asserted. 0x0: WDT reset request has not been asserted 0x1: WDT reset request has been asserted	R	0
11	RESERVED	Reserved	R	0
10	EVENTO	EVENTO status bit. The event output signal is active, when one SEV instruction is executed. This bit is set when a rising edge of EVENTO from CPU is detected. 0x0: Rising edge of EVENTO is not detected 0x1: Rising edge of EVENTO is detected	R	0
9	STANDBYWFE	This bit gives software the visibility to track whether WFE mode have been entered. 0x0: WFE mode has not been entered 0x1: WFE mode has been entered	R	0
8	STANDBYWFI	This bit gives software the visibility to track whether WFI mode have been entered. 0x0: WFI mode has not been entered 0x1: WFI mode has been entered	R	0
7:0	RESERVED	Reserved	R	0

Table 4-48. Register Call Summary for Register WKG_CONTROL_1

Dual Cortex-A9 MPU Subsystem Integration • Reset Distribution: [0]
Dual Cortex-A9 MPU Subsystem Functional Description • Power States of CPU0 and CPU1: [1]
Dual Cortex-A9 MPU Subsystem Register Manual • CORTEXA9_WUGEN Register Summary: [2]

Table 4-49. WKG_ENB_A_1

Address Offset	0x0000 0410		
Physical Address	0x4828 1410	**Instance**	CORTEXA9_WUGEN
Description	This register enables the interrupts (for CPU1) from MA_IRQ_0 to MA_IRQ_31 write 0x0: disable interrupt write 0x1: enable interrupt		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WKG_ENB_FOR_INTR31	WKG_ENB_FOR_INTR30	WKG_ENB_FOR_INTR29	WKG_ENB_FOR_INTR28	WKG_ENB_FOR_INTR27	WKG_ENB_FOR_INTR26	WKG_ENB_FOR_INTR25	WKG_ENB_FOR_INTR24	WKG_ENB_FOR_INTR23	WKG_ENB_FOR_INTR22	WKG_ENB_FOR_INTR21	WKG_ENB_FOR_INTR20	WKG_ENB_FOR_INTR19	WKG_ENB_FOR_INTR18	WKG_ENB_FOR_INTR17	WKG_ENB_FOR_INTR16	WKG_ENB_FOR_INTR15	WKG_ENB_FOR_INTR14	WKG_ENB_FOR_INTR13	WKG_ENB_FOR_INTR12	WKG_ENB_FOR_INTR11	WKG_ENB_FOR_INTR10	WKG_ENB_FOR_INTR9	RESERVED	WKG_ENB_FOR_INTR7	WKG_ENB_FOR_INTR6	RESERVED	WKG_ENB_FOR_INTR4	RESERVED	WKG_ENB_FOR_INTR2	WKG_ENB_FOR_INTR1	WKG_ENB_FOR_INTR0

Bits	Field Name	Description	Type	Reset
31	WKG_ENB_FOR_INTR31		RW	1
30	WKG_ENB_FOR_INTR30		RW	1
29	WKG_ENB_FOR_INTR29		RW	1
28	WKG_ENB_FOR_INTR28		RW	1
27	WKG_ENB_FOR_INTR27		RW	1
26	WKG_ENB_FOR_INTR26		RW	1
25	WKG_ENB_FOR_INTR25		RW	1

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Bits	Field Name	Description	Type	Reset
24	WKG_ENB_FOR_INTR24		RW	1
23	WKG_ENB_FOR_INTR23		RW	1
22	WKG_ENB_FOR_INTR22		RW	1
21	WKG_ENB_FOR_INTR21		RW	1
20	WKG_ENB_FOR_INTR20		RW	1
19	WKG_ENB_FOR_INTR19		RW	1
18	WKG_ENB_FOR_INTR18		RW	1
17	WKG_ENB_FOR_INTR17		RW	1
16	WKG_ENB_FOR_INTR16		RW	1
15	WKG_ENB_FOR_INTR15		RW	1
14	WKG_ENB_FOR_INTR14		RW	1
13	WKG_ENB_FOR_INTR13		RW	1
12	WKG_ENB_FOR_INTR12		RW	1
11	WKG_ENB_FOR_INTR11		RW	1
10	WKG_ENB_FOR_INTR10		RW	1
9	WKG_ENB_FOR_INTR9		RW	1
8	RESERVED		R	0(1)
7	WKG_ENB_FOR_INTR7		RW	1
6	WKG_ENB_FOR_INTR6		RW	1
5	RESERVED		R	1
4	WKG_ENB_FOR_INTR4		RW	1
3	RESERVED		R	1
2	WKG_ENB_FOR_INTR2		RW	1
1	WKG_ENB_FOR_INTR1		RW	1
0	WKG_ENB_FOR_INTR0		RW	1

(1) The reset value is 0x0 by safety reasons.

Table 4-50. Register Call Summary for Register WKG_ENB_A_1

Dual Cortex-A9 MPU Subsystem Functional Description • WUGEN: [0]
Dual Cortex-A9 MPU Subsystem Register Manual • CORTEXA9_WUGEN Register Summary: [1]

Table 4-51. WKG_ENB_B_1

Address Offset	0x0000 0414		
Physical Address	0x4828 1414	**Instance**	CORTEXA9_WUGEN
Description	This register enables the interrupts (for CPU1) from MA_IRQ_32 to MA_IRQ_63 write 0x0: disable interrupt write 0x1: enable interrupt		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	WKG_ENB_FOR_INTR62	WKG_ENB_FOR_INTR61	RESERVED	WKG_ENB_FOR_INTR59	WKG_ENB_FOR_INTR58	WKG_ENB_FOR_INTR57	WKG_ENB_FOR_INTR56	RESERVED	RESERVED	WKG_ENB_FOR_INTR53	RESERVED	RESERVED	RESERVED	RESERVED	WKG_ENB_FOR_INTR48	WKG_ENB_FOR_INTR47	WKG_ENB_FOR_INTR46	WKG_ENB_FOR_INTR45	WKG_ENB_FOR_INTR44	WKG_ENB_FOR_INTR43	WKG_ENB_FOR_INTR42	WKG_ENB_FOR_INTR41	WKG_ENB_FOR_INTR40	WKG_ENB_FOR_INTR39	WKG_ENB_FOR_INTR38	WKG_ENB_FOR_INTR37	WKG_ENB_FOR_INTR36	RESERVED	WKG_ENB_FOR_INTR34	WKG_ENB_FOR_INTR33	WKG_ENB_FOR_INTR32

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Bits	Field Name	Description	Type	Reset
31	RESERVED		R	1
30	WKG_ENB_FOR_INTR62		RW	1
29	WKG_ENB_FOR_INTR61		RW	1
28	RESERVED		R	1
27	WKG_ENB_FOR_INTR59		RW	1
26	WKG_ENB_FOR_INTR58		RW	1
25	WKG_ENB_FOR_INTR57		RW	1
24	WKG_ENB_FOR_INTR56		RW	1
23	RESERVED		R	1
22	RESERVED		R	1
21	WKG_ENB_FOR_INTR53		RW	1
20	RESERVED		R	1
19	RESERVED		R	1
18	RESERVED		R	1
17	RESERVED		R	1
16	WKG_ENB_FOR_INTR48		RW	1
15	WKG_ENB_FOR_INTR47		RW	1
14	WKG_ENB_FOR_INTR46		RW	1
13	WKG_ENB_FOR_INTR45		RW	1
12	WKG_ENB_FOR_INTR44		RW	1
11	WKG_ENB_FOR_INTR43		RW	1
10	WKG_ENB_FOR_INTR42		RW	1
9	WKG_ENB_FOR_INTR41		RW	1
8	WKG_ENB_FOR_INTR40		RW	1
7	WKG_ENB_FOR_INTR39		RW	1
6	WKG_ENB_FOR_INTR38		RW	1
5	WKG_ENB_FOR_INTR37		RW	1
4	WKG_ENB_FOR_INTR36		RW	1
3	RESERVED		R	1
2	WKG_ENB_FOR_INTR34		RW	1
1	WKG_ENB_FOR_INTR33		RW	1
0	WKG_ENB_FOR_INTR32		RW	1

Table 4-52. Register Call Summary for Register WKG_ENB_B_1

Dual Cortex-A9 MPU Subsystem Register Manual

- CORTEXA9_WUGEN Register Summary: [0]

Table 4-53. WKG_ENB_C_1

Address Offset	0x0000 0418		
Physical Address	0x4828 1418	**Instance**	CORTEXA9_WUGEN
Description	This register enables the interrupts (for CPU1) from MA_IRQ_64 to MA_IRQ_95 write 0x0: disable interrupt write 0x1: enable interrupt		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	WKG_ENB_FOR_INTR94	WKG_ENB_FOR_INTR93	WKG_ENB_FOR_INTR92	WKG_ENB_FOR_INTR91	WKG_ENB_FOR_INTR90	WKG_ENB_FOR_INTR89	WKG_ENB_FOR_INTR88	WKG_ENB_FOR_INTR87	WKG_ENB_FOR_INTR86	RESERVED	WKG_ENB_FOR_INTR84	WKG_ENB_FOR_INTR83	RESERVED	RESERVED	WKG_ENB_FOR_INTR80	RESERVED	WKG_ENB_FOR_INTR78	WKG_ENB_FOR_INTR77	WKG_ENB_FOR_INTR76	WKG_ENB_FOR_INTR75	WKG_ENB_FOR_INTR74	WKG_ENB_FOR_INTR73	WKG_ENB_FOR_INTR72	WKG_ENB_FOR_INTR71	WKG_ENB_FOR_INTR70	WKG_ENB_FOR_INTR69	WKG_ENB_FOR_INTR68	WKG_ENB_FOR_INTR67	WKG_ENB_FOR_INTR66	WKG_ENB_FOR_INTR65	RESERVED

Bits	Field Name	Description	Type	Reset
31	RESERVED		R	1
30	WKG_ENB_FOR_INTR94		RW	1
29	WKG_ENB_FOR_INTR93		RW	1
28	WKG_ENB_FOR_INTR92		RW	1
27	WKG_ENB_FOR_INTR91		RW	1
26	WKG_ENB_FOR_INTR90		RW	1
25	WKG_ENB_FOR_INTR89		RW	1
24	WKG_ENB_FOR_INTR88		RW	1
23	WKG_ENB_FOR_INTR87		RW	1
22	WKG_ENB_FOR_INTR86		RW	1
21	RESERVED		R	1
20	WKG_ENB_FOR_INTR84		RW	1
19	WKG_ENB_FOR_INTR83		RW	1
18	RESERVED		R	1
17	RESERVED		R	1
16	WKG_ENB_FOR_INTR80		RW	1
15	RESERVED		R	1
14	WKG_ENB_FOR_INTR78		RW	1
13	WKG_ENB_FOR_INTR77		RW	1
12	WKG_ENB_FOR_INTR76		RW	1
11	WKG_ENB_FOR_INTR75		RW	1
10	WKG_ENB_FOR_INTR74		RW	1
9	WKG_ENB_FOR_INTR73		RW	1
8	WKG_ENB_FOR_INTR72		RW	1
7	WKG_ENB_FOR_INTR71		RW	1
6	WKG_ENB_FOR_INTR70		RW	1
5	WKG_ENB_FOR_INTR69		RW	1
4	WKG_ENB_FOR_INTR68		RW	1
3	WKG_ENB_FOR_INTR67		RW	1
2	WKG_ENB_FOR_INTR66		RW	1
1	WKG_ENB_FOR_INTR65		RW	1
0	RESERVED		R	1

Table 4-54. Register Call Summary for Register WKG_ENB_C_1

Dual Cortex-A9 MPU Subsystem Register Manual

- CORTEXA9_WUGEN Register Summary: [0]

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Table 4-55. WKG_ENB_D_1

Address Offset	0x0000 041C		
Physical Address	0x4828 141C	**Instance**	CORTEXA9_WUGEN
Description	This register enables the interrupts (for CPU1) from MA_IRQ_96 to MA_IRQ_127 write 0x0: disable interrupt write 0x1: enable interrupt		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	WKG_ENB_FOR_INTR120	WKG_ENB_FOR_INTR119	RESERVED	RESERVED	RESERVED	RESERVED	WKG_ENB_FOR_INTR114	WKG_ENB_FOR_INTR113	WKG_ENB_FOR_INTR112	WKG_ENB_FOR_INTR111	WKG_ENB_FOR_INTR110	WKG_ENB_FOR_INTR109	RESERVED	WKG_ENB_FOR_INTR107	RESERVED	RESERVED	WKG_ENB_FOR_INTR104	WKG_ENB_FOR_INTR103	WKG_ENB_FOR_INTR102	WKG_ENB_FOR_INTR101	WKG_ENB_FOR_INTR100	WKG_ENB_FOR_INTR99	WKG_ENB_FOR_INTR98	WKG_ENB_FOR_INTR97	WKG_ENB_FOR_INTR96

Bits	Field Name	Description	Type	Reset
31	RESERVED		R	1
30	RESERVED		R	1
29	RESERVED		R	1
28	RESERVED		R	1
27	RESERVED		R	1
26	RESERVED		R	1
25	RESERVED		R	1
24	WKG_ENB_FOR_INTR120		RW	1
23	WKG_ENB_FOR_INTR119		RW	1
22	RESERVED		R	1
21	RESERVED		R	1
20	RESERVED		R	1
19	RESERVED		R	1
18	WKG_ENB_FOR_INTR114		RW	1
17	WKG_ENB_FOR_INTR113		RW	1
16	WKG_ENB_FOR_INTR112		RW	1
15	WKG_ENB_FOR_INTR111		RW	1
14	WKG_ENB_FOR_INTR110		RW	1
13	WKG_ENB_FOR_INTR109		RW	1
12	RESERVED		R	1
11	WKG_ENB_FOR_INTR107		RW	1
10	RESERVED		R	1
9	RESERVED		R	1
8	WKG_ENB_FOR_INTR104		RW	1
7	WKG_ENB_FOR_INTR103		RW	1
6	WKG_ENB_FOR_INTR102		RW	1
5	WKG_ENB_FOR_INTR101		RW	1
4	WKG_ENB_FOR_INTR100		RW	1
3	WKG_ENB_FOR_INTR99		RW	1
2	WKG_ENB_FOR_INTR98		RW	1
1	WKG_ENB_FOR_INTR97		RW	1

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Bits	Field Name	Description	Type	Reset
0	WKG_ENB_FOR_INTR96		RW	1

Table 4-56. Register Call Summary for Register WKG_ENB_D_1

Dual Cortex-A9 MPU Subsystem Functional Description • WUGEN: [0]
Dual Cortex-A9 MPU Subsystem Register Manual • CORTEXA9_WUGEN Register Summary: [1]

Table 4-57. AUX_CORE_BOOT_0

Address Offset	0x800		
Physical Address	0x4828 1800	**Instance**	CORTEXA9_WUGEN
Description	This register is used by the ROM code and OS during SMP boot, it is intended to store execution start address of CPU1. When needed, the SMP OS (executing on the CPU0) wakes up CPU1 by executing a SEV command. CPU0 needs to communicate some start-up information (e.g. starting address) to CPU1.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AUX_CORE_BOOT_0																															

Bits	Field Name	Description	Type	Reset
31:0	AUX_CORE_BOOT_0	SMP boot register	RW	0x00000000

Table 4-58. Register Call Summary for Register AUX_CORE_BOOT_0

Dual Cortex-A9 MPU Subsystem Functional Description • Cortex-A9 MPU Subsystem Block Diagram: [0]
Dual Cortex-A9 MPU Subsystem Register Manual • CORTEXA9_WUGEN Register Summary: [1] • CORTEXA9_WUGEN Register Description: [2]

Table 4-59. AUX_CORE_BOOT_1

Address Offset	0x804		
Physical Address	0x4828 1804	**Instance**	CORTEXA9_WUGEN
Description	This register is used by the ROM code and OS during SMP boot, used to indicate boot status to either CPUs. When CPU1 received an event (caused by the SEV command), it continues execution in the ROM which set up the code to branch to the address signaled by CPU0.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AUX_CORE_BOOT_1																															

Bits	Field Name	Description	Type	Reset
31:0	AUX_CORE_BOOT_1	SMP boot register	RW	0x00000000

Table 4-60. Register Call Summary for Register AUX_CORE_BOOT_1

Dual Cortex-A9 MPU Subsystem Functional Description • Cortex-A9 MPU Subsystem Block Diagram: [0]
Dual Cortex-A9 MPU Subsystem Register Manual • CORTEXA9_WUGEN Register Summary: [1] • CORTEXA9_WUGEN Register Description: [2]

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4.4.10 CMU Registers

4.4.10.1 CMU Register Summary

Table 4-61. CMU Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	CMU Base Address
CMUCONFIGREG	RW	32	0x0000 0000	0x4829 0000
CMUSTATUSREG	R	32	0x0000 0004	0x4829 0004
RESERVED	R	32	0x0000 0008	0x4829 0008
CMUINTRACK	R	32	0x0000 000C	0x4829 000C
CMUALLOCATE	R	32	0x0000 0010	0x4829 0010
CMUDEALLOCATE	RW	32	0x0000 0014	0x4829 0014
RESERVED	R	32	0x0000 0018	0x4829 0018
CMUDEBUG	RW	32	0x0000 001C	0x4829 001C
CMUOPERATION_i (1)	RW	32	0x0000 1000 + (0x10 * I)	0x4829 1000 + (0x10 * I)
CMUSTARTPA_i (1)	RW	32	0x0000 1004 + (0x10 * I)	0x4829 1004 + (0x10 * I)
CMULENGTH_i (1)	RW	32	0x0000 1008 + (0x10 * I)	0x4829 1008 + (0x10 * I)
CMURANGESTATE_i (1)	R	32	0x0000 100C + (0x10 * I)	0x4829 100C + (0x10 * I)

(1) I = 0 to 63

4.4.10.2 CMU Register Description

Table 4-62. CMUCONFIGREG

Address Offset	0x0000 0000		
Physical Address	0x4829 0000	**Instance**	CMU
Description	CMU Configuration Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
THREADS				QENTRIES												RESERVED					DISABLEPIPELINING	DISABLEPARALLEL	INTEN	RESERVED				ENNSWR	LINESTEP		

Bits	Field Name	Description	Type	Reset
31:28	THREADS	Number of parallel CMO threads that can be simultaneously processed.	R	0x1
27:16	QENTRIES	Number of Queue Entries Configured	R	0x040
15:11	RESERVED	Reserved.	R	0x00
10	DISABLEPIPELINING	Disable pipelining of requests.	RW	1
9	DISABLEPARALLEL	Force sequential operation by disabling any parallelism between RangeSets.	RW	1
8	INTEN	Enable Interrupt on Set Completion. 0b0 = Don't interrupt. 0b1 = Interrupt on Completion.	RW	0
7:4	RESERVED	Reserved	R	0x0

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Bits	Field Name	Description	Type	Reset
3	ENNSWR	This enables Non-Safe programs to write this register. Out of reset - this bit is 0 which will prevent Non-Safe programs from writing it. Reading is always allowed. This bit can be set to 0x1 only through a Special Safe Monitor API. For more information about the API, see the Initialization chapter. The ROM Code will set this bit to 1 at boot time. The API can be used at runtime by the NS SW to enable/disable when necessary.	RW	0
2:0	LINESTEP	Size of smallest cache line size, log2 - 2. 0x0: Line Step = 4 bytes. 0x1: Line Step = 8 bytes. 0x2: Line Step = 16 bytes. 0x3: Line Step = 32 bytes. 0x4: Line Step = 64 bytes. 0x5: Line Step = 128 bytes. 0x6: Line Step = 256 bytes. 0x7: Line Step = 512 bytes.	R	0x3

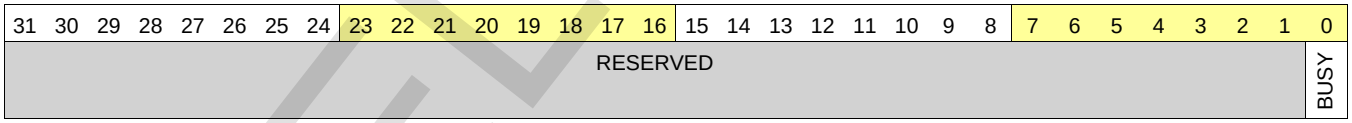
Table 4-63. Register Call Summary for Register CMUCONFIGREG

Dual Cortex-A9 MPU Subsystem Functional Description
- Functionality: [0]
- Parallelism and Pipelining: [1]
- Completion Handling: [2]

Dual Cortex-A9 MPU Subsystem Register Manual
- CMU Register Summary: [3]

Table 4-64. CMUSTATUSREG

Address Offset	0x0000 0004		
Physical Address	0x4829 0004	**Instance**	CMU
Description	CMU Status.		
Type	R		



Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved.	R	0x0000 0000
0	BUSY	Indicates that at least one set is active. 0b0 = CMU is idle. 0b1 = At least one set is active.	R	0

Table 4-65. Register Call Summary for Register CMUSTATUSREG

Dual Cortex-A9 MPU Subsystem Functional Description
- Monitoring Completion: [0]

Dual Cortex-A9 MPU Subsystem Register Manual
- CMU Register Summary: [1]

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Table 4-66. CMUINTRACK

Address Offset	0x0000 000C		
Physical Address	0x4829 000C	**Instance**	CMU
Description	Interrupt Acknowledgment Register. Returns the index of the RangeSet that caused the interrupt. An error bit indicates an error completion. Since there is a queue of interrupt acknowledgments, there is also a valid bit that indicates that there were no more interrupts on the queue.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALID	RESERVED															ERROR	RESERVED							INDEX							
R	R															R	R							R							
0	0															-	0							0x—							

Bits	Field Name	Description	Type	Reset
31	VALID	Indicates that the label field is valid. Can read the entire queue of entries by reading until get Valid = 0.	R	0
30:16	RESERVED	Reserved	R	0x0000
15	ERROR	Indicates that the RangeSet operation completed with an error.	R	-
14:12	RESERVED	Reserved	R	0x0
11:0	INDEX	The index of the RangeSet that caused the interrupt.	R	0x—

Table 4-67. Register Call Summary for Register CMUINTRACK

Dual Cortex-A9 MPU Subsystem Functional Description

- Completion Handling: [0]
- Interrupt Index Queue: [1] [2] [3] [4]

Dual Cortex-A9 MPU Subsystem Register Manual

- CMU Register Summary: [5]

Table 4-68. CMUALLOCATE

Address Offset	0x0000 0010		
Physical Address	0x4829 0010	**Instance**	CMU
Description	Returns the index of a RangeSet in the Free state.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NONE	RESERVED																							INDEX							
R	R																							R							
0	0																							0x00							

Bits	Field Name	Description	Type	Reset
31	NONE	Returns 0b0 if Index is valid or 0b1 if no RangeSets available for allocation	R	0
30:8	RESERVED	Reserved.	R	0x000000
7:0	INDEX	Returns the Index of a RangeSet if one is available or zero.	R	0x00

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Table 4-69. Register Call Summary for Register CMUALLOCATE

Dual Cortex-A9 MPU Subsystem Functional Description

- Functionality: [0]
- Allocation: [1] [2]
- Allocating a Range Set: [3] [4]
- Configuration Registers: [5]
- Allocation and Free Set Management: [6] [7] [8] [9]
- Priority of Range Set DMEM Accesses: [10]
- Important Programming Notes for Users of CMU: [11] [12] [13] [14] [15]

Dual Cortex-A9 MPU Subsystem Register Manual

- CMU Register Summary: [16]

Table 4-70. CMUDEALLOCATE

Address Offset	0x0000 0014		
Physical Address	0x4829 0014	**Instance**	CMU
Description	An index stored to this register frees the RangeSet with that index.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								INDEX							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Reserved	R	0x000000
7:0	INDEX	RangeSet Index written here is deallocated (set to the Free state).	RW	0x00

Table 4-71. Register Call Summary for Register CMUDEALLOCATE

Dual Cortex-A9 MPU Subsystem Functional Description

- Functionality: [0]
- Allocation: [1]
- Freeing a Range Set: [2]
- Configuration Registers: [3]
- Allocation and Free Set Management: [4] [5] [6]
- Priority of Range Set DMEM Accesses: [7]
- Important Programming Notes for Users of CMU: [8]

Dual Cortex-A9 MPU Subsystem Register Manual

- CMU Register Summary: [9]

Table 4-72. CMUDEBUG

Address Offset	0x0000 001C		
Physical Address	0x4829 001C	**Instance**	CMU
Description	Debug register to configure how MSuspend from the various CPUs need to be looked at by CMU to either send or not send traffic during debug session.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																											AND_MSUSPEND	OR_MSUSPEND	SPEC_MSUSPEND	CPU_MSUSPEND		

Bits	Field Name	Description	Type	Reset
31:5	RESERVED		R	0x0000000
4	AND_MSUSPEND	This bit can be set so that only if all the MSuspends of all the CPUs present are enabled, CMU will suspend activity to ACP. Bits 3 and 2 need to be set to 0.	RW	0
3	OR_MSUSPEND	This bit can be set so that if any of the MSuspends of CPUs present are enabled, then CMU will suspend activity to ACP. Bits 4 and 2 need to be 0.	RW	0
2	SPEC_MSUSPEND	This bit enables CMU to look at the MSuspend of a specific CPU to suspend CMU activity to ACP. Bits 4, 3 need to be 0 when bit 2 is 1.	RW	0
1:0	CPU_MSUSPEND	This field allows CMU to look at the MSuspend of a specific CPU to suspend traffic to ACP. When bit 4:2 = 3'b001, bits 1:0 indicates which CPU's MSuspend needs to be looked at. If the appropriate CPU's MSuspend is 1, then CMU will not generate any more activity to ACP and rest of system to have a non-intrusive debug session. When Bit 2 = 0, specific CPU's MSuspend cannot be used to control CMU's activity.	RW	0x0

Table 4-73. Register Call Summary for Register CMUDEBUG

Dual Cortex-A9 MPU Subsystem Register Manual

- CMU Register Summary: [0]

Table 4-74. CMUOPERATION_i

Address Offset	0x0000 1000 + (0x10 * I)	**Index**	I = 0 to 63
Physical Address	0x4829 1000 + (0x10 * I)	**Instance**	CMU
Description	Controls the operation of one RangeSet of the CMU. Storing this register enqueues or activates the RangeSet. Note: must not write to any of the rangeset registers if State != 0b00. That indicates that previous values have not yet been transferred to the queue!		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NS	RESERVED																				COMPLETION	WAIT	RESERVED					OPNSEL			

Bits	Field Name	Description	Type	Reset
31	NS	Not Safe. Set to NS used to access StartPA register. Writing one to this bit will perform the operation as non-safe. The software can not clear this bit to 0x0 after.	RW W1toSet	0
30:11	RESERVED	Reserved.	R	0x00000

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Bits	Field Name	Description	Type	Reset
10:9	COMPLETION	Completion Signaling Options: 0x0: No notification of normal or error completion. 0x1: Interrupt on normal or error completion. 0x2: Interrupt on error but not normal completion. 0x3: Reserved.	RW	0x0
8	WAIT	Wait to start. 0b1 = Wait until all previous requests are complete. 0b0 = may proceed in parallel with previous requests.	RW	0
7:4	RESERVED	Reserved.	R	0x0
3:0	OPNSEL	Selects the Cache Management Operation. If an operation is started with a reserved OpnSel, the RangeSet is immediately moved to the Error state. 0x0: No operation is performed. A RangeSet activated with this OpnSel is immediately moved to the completed state. 0x1: Invalidate. 0x2: Clean. 0x3: Clean and Invalidate. 0x4: Reserved. 0x5: Reserved. 0x6: Reserved. 0x7: Reserved. 0x8: Reserved 0x9: Reserved. 0xA: Reserved. 0xB: Reserved. 0xC: Reserved. 0xD: Reserved. 0xE: Reserved. 0xF: Always moves the RangeSet to the Error State.	RW	0x0

Table 4-75. Register Call Summary for Register CMUOPERATION_i

Dual Cortex-A9 MPU Subsystem Functional Description

- Functionality: [0] [1]
- Range Sets: [2]
- Parallelism and Pipelining: [3]
- Completion Handling: [4]
- Activate the Range Set by Storing the Operation Register: [5]
- Monitoring Completion: [6]
- Interrupt Index Queue: [7]
- Interrupt Index Queue: [8]

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- CMU Register Summary: [9]

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Table 4-76. CMUSTARTPA_i

Address Offset	0x0000 1004 + (0x10 * I)	**Index**	I = 0 to 63
Physical Address	0x4829 1004 + (0x10 * I)	**Instance**	CMU
Description	Starting (lower, inclusive) 32-bit physical address.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STARTPA																															

Bits	Field Name	Description	Type	Reset
31:0	STARTPA	Start of range for cache operations.	RW	0x0000 0000

Table 4-77. Register Call Summary for Register CMUSTARTPA_i

Dual Cortex-A9 MPU Subsystem Functional Description
- Functionality: [0]
- Range Sets: [1]
- Address Sequence Generation: [2] [3]
- Storing Starting Physical Address and Length: [4]

Dual Cortex-A9 MPU Subsystem Register Manual
- CMU Register Summary: [5]

Table 4-78. CMULENGTH_i

Address Offset	0x0000 1008 + (0x10 * I)	**Index**	I = 0 to 63
Physical Address	0x4829 1008 + (0x10 * I)	**Instance**	CMU
Description	Length in bytes of the range - 1, giving a representable range of 1 byte to 4k bytes.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				LEN											

Bits	Field Name	Description	Type	Reset
31:12	RESERVED	Reserved	R	0x000
11:0	LEN	Length of range minus 1.	RW	0x000

Table 4-79. Register Call Summary for Register CMULENGTH_i

Dual Cortex-A9 MPU Subsystem Functional Description
- Functionality: [0]
- Range Sets: [1]
- Address Sequence Generation: [2] [3] [4]
- Storing Starting Physical Address and Length: [5]

Dual Cortex-A9 MPU Subsystem Register Manual
- CMU Register Summary: [6]

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Table 4-80. CMURANGESTATE_i

Address Offset	0x0000 100C + (0x10 * I)	**Index**	I = 0 to 63
Physical Address	0x4829 100C + (0x10 * I)	**Instance**	CMU
Description	State of the Range Operation. Used to poll RangeSet for error or completion.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STATE								RESERVED																							

Bits	Field Name	Description	Type	Reset
31:29	STATE	State of the RangeSet Request. Read 0x0: RangeSet is unallocated. Read 0x1: RangeSet allocated but not yet activated. Read 0x2: Reserved Read 0x3: RangeSet is active, either sequencing through cache lines, awaiting completion of earlier RangeSets or awaiting processing resources. Read 0x4: Reserved Read 0x5: Reserved Read 0x6: RangeSet operation completed without errors. Read 0x7: RangeSet encountered an error. Processing of the RangeSet stops with the first error. It is reported as complete with error.	R	0x0
28:0	RESERVED	Reserved	R	0x0000 0000

Table 4-81. Register Call Summary for Register CMURANGESTATE_i

Dual Cortex-A9 MPU Subsystem Functional Description
- Functionality: [0]
- Monitoring Completion: [1] [2]

Dual Cortex-A9 MPU Subsystem Register Manual
- CMU Register Summary: [3]

4.4.11 Local Interconnect Registers

4.4.11.1 Local Interconnect Register Summary

Table 4-82. Local interconnect Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	Local interconnect Base Address
MA_PRIORITY	RW	32	0x0	0x482A 2000

4.4.11.2 Local Interconnect Register Description

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Table 4-83. MA_PRIORITY

Address Offset	0x0000 0000		
Physical Address	0x482A 2000	**Instance**	Local interconnect
Description	Memory Adapter Priority Register. This register indicates the priority of memory access from MA to EMIF. This priority is used by EMIF in scheduling MA access to EMIF. 0x0 is lowest priority and 0x7 highest priority.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													PRIORITY		

Bits	Field Name	Description	Type	Reset
31:3	RESERVED	Reserved	RW	0x0000 0000
2:0	PRIORITY	MA priority value	RW	0x0

Table 4-84. Register Call Summary for Register MA_PRIORITY

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- Local Interconnect Register Summary: [0]

4.4.12 MA Registers

4.4.12.1 MA Register Summary

Table 4-85. MA Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	MA Base Address
RESERVED	R	32	0x0000 0010	0x482A F010
MA_LISA_LOCK	RW	32	0x0000 001C	0x482A F01C
MA_LISA_MAP_i [(1)]	RW	32	0x0000 0040 + (0x4 * I)	0x482A F040 + (0x4 * I)

(1) I = 0 to 63

4.4.12.2 MA Register Description

For the description of the MA registers, see Section 15.2.6, *DMM Register Manual*, in Section 15.2, *Dynamic Memory Manager*, where MA_LISA_LOCK corresponds to the DMM_LISA_LOCK register description, and MA_LISA_MAP_i corresponds to the DMM_LISA_MAP_i register description.

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DSP Subsystem

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IVA-HD Subsystem

This chapter describes the IVA-HD subsystem in the multimedia device.

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6.1 IVA-HD Overview **1130**

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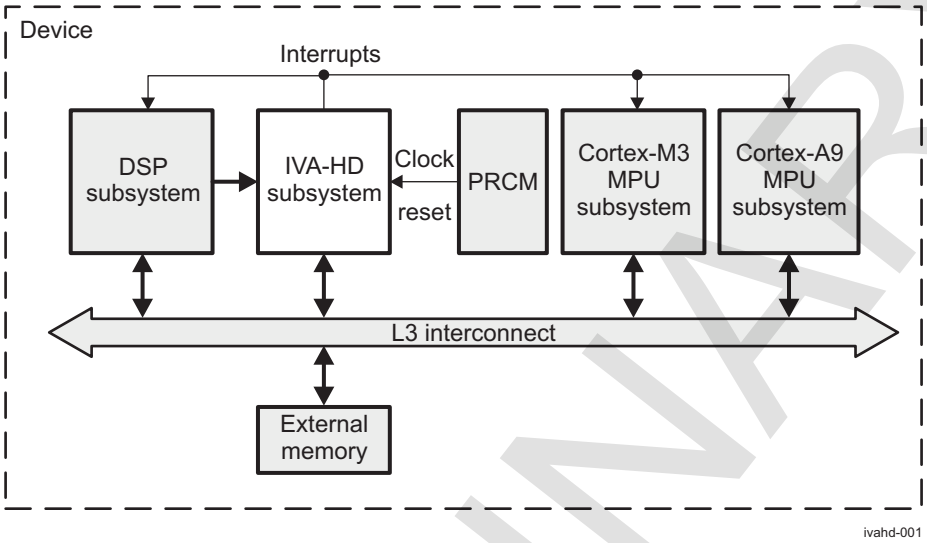
6.1 IVA-HD Overview

The IVA-HD is the image and video imaging hardware accelerator subsystem. Figure 6-1 shows the IVA-HD subsystem in the device.

Figure 6-1. IVA-HD in the Device



The IVA-HD supports resolutions up to 1080 p/i with full performance of 30 fps (or 60 fields). The IVA-HD subsystem supports the following codec standards natively; that is, all functions of standards are accelerated (without any intervention of the digital signal processor [DSP]):

- H.264: BP/MP/HP Encode and Decode
- H.264: Fast Profile/RCDO Encode and Decode
- MPEG-4: SP/ASP Encode/Decode (No support for GMC)
- DivX 5.x and higher Encode/Decode (No lower version; for example, 3.11 and 4.x)
- H.263: Profile 0 and 3 for Decode, Profile 0 for Encode
- Sorenson Spark: V0 and V1 Decode (No encode support)
- MPEG-2 SP/MP Encode/Decode
- MPEG-1 Encode/Decode
- VC-1/WMV9/RTV : SP/MP/AP Encode and Decode
- On2® VP6/VP7 Decode
- RealVideo® 8/9/10 Decode
- AVS 1.0 Encode and Decode
- JPEG (also MJPEG) Baseline Encode/Decode
- H.264 Annex G (SVC) Scalable Baseline Profile to 480p – 720p30
- H.264 Annex H (MVC) up to 720p30

The IVA-HD subsystem is composed of:

- A primary sequencer, including its memories and an interrupt controller: iCONT1
- A video direct memory access (DMA) processor, which can be used as a secondary sequencer: iCONT2
- A video DMA engine: vDMA
- An entropy coder/decoder: ECD3
- A motion compensation engine: MC3
- A transform and quantization calculation engine: CALC3
- A loop filter acceleration engine: iLF3

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- A motion estimation acceleration engine: iME3
- An intraprediction estimation engine: iPE3
- Shared level 2 (L2) interface and memory
- Local interconnect
- A message interface for communication between SyncBoxes
- Mailbox
- A debug module for trace event and software instrumentation: SMSET

IVA-HD 1.0 will use eXpressDSP Digital Media (xDM) standard as the principle software interface. The xDM standard defines application programming interfaces (APIs) through which an application invokes a particular class of codec, such as video decode or audio encode.

xDM developers kit, technical documentation and full compliant codecs can be downloaded from http://focus.ti.com/docs/toolsw/folders/print/tmdxdaisxdm.html.

Software released on IVA-HD 1.0 will be xDM-compliant and will be available during 2010.

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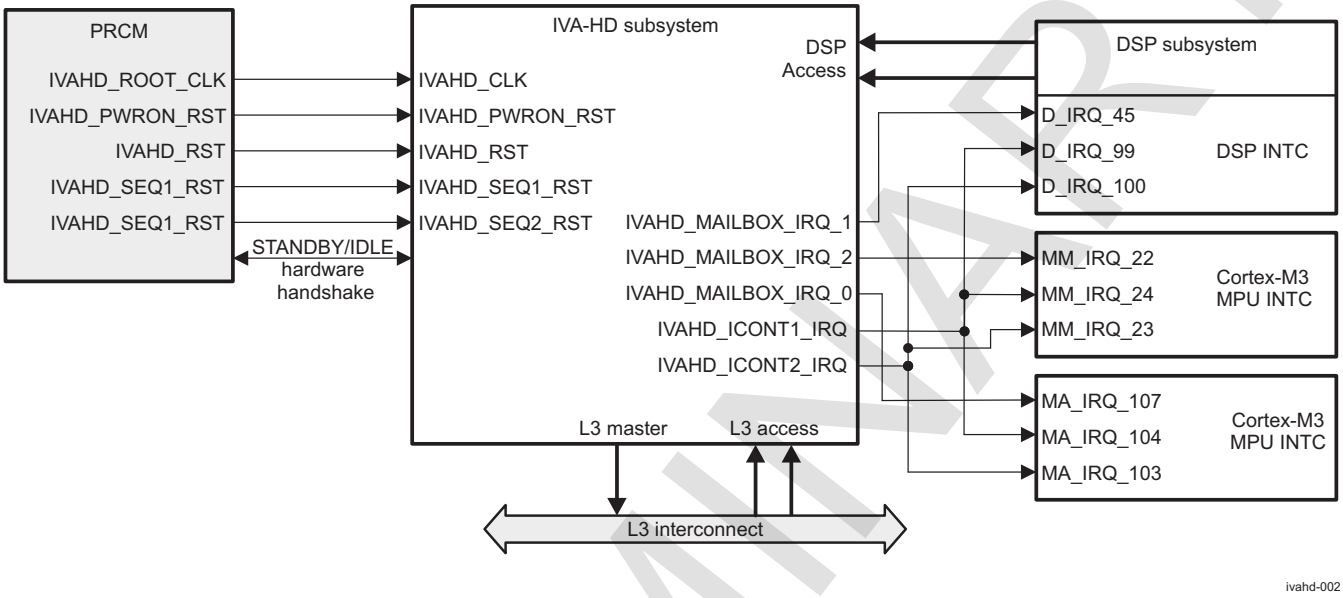
6.1.1 IVA-HD Integration

This section describes IVA-HD in the device, including information about clocks, resets, and hardware requests.

Figure 6-2 shows IVA-HD integration.

Figure 6-2. IVA-HD Integration



NOTE: For more information about the STANDBY/IDLE hardware handshake and the wake-up request, see Section 3.1.1.1.2, *Module-Level Clock Management*, in Chapter 3 *Power, Reset and Clock Management*.

Table 6-1 through Table 6-3 summarize the integration of the module in the device.

Table 6-1. IVA-HD Integration Attributes

Module Instance	Attributes	
	Power Domain	Interconnect
IVA-HD	PD_IVAHD	L3

Table 6-2. IVA-HD Clocks and Resets

Clocks				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
IVA-HD	IVAHD_CLK	IVAHD_ROOT_CLK	CM	IVA-HD clock (functional and interface)
Resets				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
IVA-HD	IVAHD_PWRON_RST	IVAHD_PWRON_RST	PRM	IVA-HD power-on reset
IVA-HD	IVAHD_RST	IVAHD_RST	PRM	IVA-HD global reset (all logic is reset)
IVA-HD	IVAHD_SEQ1_RST	IVAHD_SEQ1_RST	PRM	iCONT1 reset
IVA-HD	IVAHD_SEQ2_RST	IVAHD_SEQ2_RST	PRM	iCONT2 reset

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Table 6-3. Hardware Requests

Interrupt Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
IVA-HD	IVAHD_MAILBOX_IRQ_0	MA_IRQ_107	Cortex™-A9 MPU INTC	IVA-HD mailbox user 0 interrupt
IVA-HD	IVAHD_ICONT1_IRQ	MA_IRQ_104	Cortex-A9 MPU INTC	Sync interrupt from iCONT1
IVA-HD	IVAHD_ICONT2_IRQ	MA_IRQ_103	Cortex-A9 MPU INTC	Sync interrupt from iCONT2
IVA-HD	IVAHD_MAILBOX_IRQ_1	D_IRQ_45	DSP INTC	IVA-HD mailbox user 1 interrupt
IVA-HD	IVAHD_ICONT1_IRQ	D_IRQ_99	DSP INTC	Sync interrupt from iCONT1
IVA-HD	IVAHD_ICONT2_IRQ	D_IRQ_100	DSP INTC	Sync interrupt from iCONT2
IVA-HD	IVAHD_MAILBOX_IRQ_2	MM_IRQ_22	Cortex™-M3 MPU INTC	IVA-HD mailbox user 2 interrupt
IVA-HD	IVAHD_ICONT1_IRQ	MM_IRQ_24	Cortex-M3 MPU INTC	Sync interrupt from iCONT1
IVA-HD	IVAHD_ICONT2_IRQ	MM_IRQ_23	Cortex-M3 MPU INTC	Sync interrupt from iCONT2

NOTE:

- For more information about the mailbox interrupt, see Section 19.3.4.

6.1.2 IVA-HD Functional Description

6.1.2.1 IVA-HD Block Diagram

Figure 6-3 shows a block diagram of the IVA-HD subsystem.

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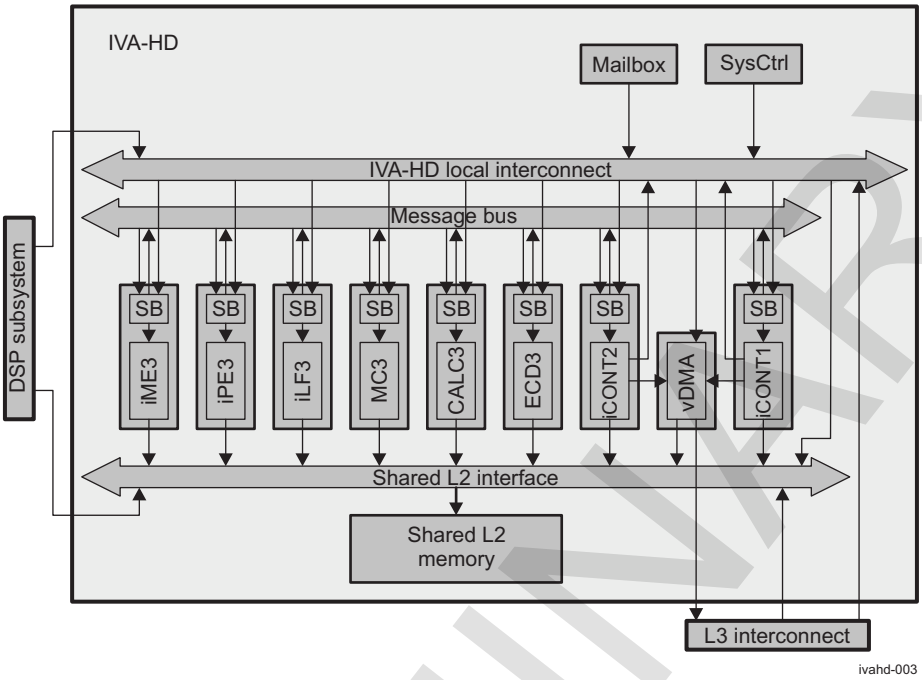
Figure 6-3. IVA-HD Block Diagram



NOTE: SB stands for SyncBox.

NOTE: iPE3, MC3, CALC3, and ECD3 include a load and store engine (LSE), which is the same in each of these modules.

6.1.2.1.1 SyncBox

The SyncBox is a configurable module that is responsible for scheduling all embedded hardware module within IVA-HD subsystem. It handles all aspects of synchronization, data sharing, and parameters passing between accelerators. It also offers the possibilities to use asynchronous messages.

6.1.2.1.2 iCONTs

The iCONT module is an ARM968E-S™ based microcontroller with 32KB of instruction tightly coupled memory and 16KB of data tightly coupled memory. It includes an interrupt controller (INTC), a local data mover, its own SyncBox module for synchronizing tasks with other modules and its associated SyncBox handler.

Two identical instances of iCONT, iCONT1, and iCONT2, are present in the IVA-HD subsystem. They can typically be used to perform high-level processing (at frame and slice level), control at macroblock-level bounding box computation and other vDMA processing tasks.

Software can map process equally on either iCONT.

6.1.2.1.3 vDMA

The vDMA is a DMA engine to perform data transfer between external memories and shared L2 memory and also memory copies inside SL2 and inside external memory.

6.1.2.1.4 iME3

The iME3 accelerator is used to perform motion estimation in encode processing. iME3 embeds its own SyncBox module for synchronizing tasks with other modules.

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It compares a current macroblock to reference area and provides area in reference region (in terms of offsets) which is least different to the current macroblock. It can also interpolate a block with half or quarter pixel precision, thus producing 4 (half pixel) or 16 (quarter pixel) interpolated blocks from the original block. Additionally, it supports searching of the best matching block within the interpolated planes.

6.1.2.1.5 iPE3

The iPE3 accelerator is used to perform the intraprediction estimation in encode. The iPE3 embeds its own SyncBox module for synchronizing tasks with other modules and an LSE to transfer data from internal memories to shared L2 memory.

It supports two modes, depending on video standard:

- Spatial intraprediction estimation for H.264 and AVS. It creates intraprediction macroblocks with given intramodes from original macroblock and provides cost estimation between the original macroblock and each pseudo intraprediction macroblock, and then chooses a mode with the smallest cost to recommend it as an optimal intraprediction mode.
- Spatial activity for MPEG-1/2/4 and VC-1. It calculates the spatial activity of the original luminance samples with the specified block size. This mode intends to provide information of the original Luma pixels. The values can be used to decide the coding parameters of the macroblock such as the coding mode and the quantization parameter.

6.1.2.1.6 MC3

The MC3 accelerator is used to perform the motion compensation. MC3 embeds its own SyncBox module for synchronizing tasks with other HWAs and an LSE to transfer data from internal memories to shared L2 memory.

It creates an interprediction macroblock with given motion vectors and modes from the reference data.

6.1.2.1.7 CALC3

The CALC3 accelerator is used to perform forward and inverse transform and quantization calculation. CALC3 embeds its own SyncBox module for synchronizing tasks with other HWAs and an LSE to transfer data from internal memories to shared L2 memory.

It can perform transform/inverse transform, Q/iQ and DC/AC prediction.

6.1.2.1.8 iLF3

The iLF3 accelerator is used to perform deblocking filtering and boundary strength computation. The iLF3 embeds its own SyncBox module for synchronizing tasks with other HWAs.

6.1.2.1.9 ECD3

The ECD3 accelerator is designed to encode and decode the stream. ECD3 embeds its own SyncBox module for synchronizing tasks with other HWAs and an LSE to transfer data from internal memories to shared L2 memory.

It supports Huffman codes and arithmetic codes.

For encode, the ECD3 encodes the macroblock information and residual data into bitstream. For decode, the ECD3 decodes the bitstream and recovers the macroblock information and residual data.

6.1.2.1.10 SL2 Interface

The shared L2 interface, SL2IF, is an arbitrator that allows 18 initiators to access to an interleaved set of eight memory banks.

The SL2IF has two sets of interfaces:

- Eighteen 128-bit interfaces for accesses from module's to shared L2 memories.
- Eight 128-bit memory interfaces for direct accesses to memory bank

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6.1.2.1.11 Message Bus

The message bus, is an arbitrator that allows eight initiators to access eight targets. It is used to dispatch messages generated by the SyncBox of the different IPs.

6.1.2.1.12 IVA-HD Local Interconnect

The IVA-HD local interconnect provides connectivity between two external host interconnects (DSP and L3), two local sequencers (iCONT1 and iCONT2) and video hardware accelerators (iME3, iLF3, ECD3, CALC3, MC3, iPE3), video DMA engine (vDMA), and local modules (mailbox and sysctrl).

6.1.2.1.13 MailBox

The function of the mailbox is to support a 2-way communication between two hosts through interrupt. It allows the software to establish a communication channel between processors through a set of registers and associated interrupt signals by sending and receiving messages.

The mailbox embedded inside the IVA-HD subsystem implements a 2-way communication between three external users and one internal user. This communication is ensured through three pairs of mailboxes and four-message FIFO depth for each message queue.

NOTE: The internal user is one of the two iCONTs. iCONT1 and iCONT2 are connected on a shared interrupt line. The choice between iCONT1 and iCONT2 is done by masking mailbox interrupt on iCONT1 or iCONT2. iCONT1 and iCONT2 can access the mailbox through the IVA-HD local interconnect.

For a detailed description of the mailbox, including IVA-HD mailbox interrupt mapping, see , *IVA-HD Imaging Controller*.

6.1.2.1.14 IVA-HD System Control

The SYSCTRL module of IVA-HD is in charge of:

- Controlling clocks to module's, upon software control and power handshaking state
- Controlling power, reset, and clock management (PRCM) module power handshaking
- Providing status of the above operation
- Supporting synchronization through external event

6.1.2.2 IVA-HD Power Management

Table 6-4 describes power-management features available for the IVA-HD module.

NOTE: For descriptions of IdleMode and StandbyMode features, see Section 3.1.1.1.2, *Module-Level Clock Management*, in Chapter 3, *Power, Reset, and Clock Management*.

Table 6-4. Local Power-Management Features

Feature	Registers	Description
Slave idle modes	IVAHD_SYSCONFIG[3:2] IDLEMODE	No-idle and smart-idle modes are available.
Master standby modes	IVAHD_SYSCONFIG[5:4] STANDBYMODE	No-standby and smart-standby modes are available.

6.1.2.3 IVA-HD Memory Mapping

ARM968E-S (of each iCONT) can address a 4-GB memory space. The lower address range (8MB) is allocated to its level 1 (L1) memories (ITCM and DTCM). The higher address range is allocated to L2 memories. Access to L2 memories can be buffered or nonbuffered, depending on the selected address range. For more information, see the ARM968E-STM Technical Reference Manual.

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In Table 6-5, the address spaces of buffered regions are shown as EXT_BUF, and the address spaces of nonbuffered regions are shown as EXT_NBUF.

Table 6-5. iCONT Memory Mapping Regions

Region Name	Address		Size	Description
	Start	Stop	(KB)	
ITCM	0x0000 0000	0x0000 7FFF	32	ITCM memory aliased 128 times
	...	...	...	
ITCM (alias 127)	0x003F 8000	0x003F FFFF	32	
DTCM	0x0040 0000	0x0040 3FFF	16	DTCM memory aliased 256 times
	...	...	...	
DTCM (alias 255)	0x007F C000	0x007F FFFF	16	
EXT_BUF	0x0080 0000	0x008F FFFF	1024	External buffered region
	...	...	...	
EXT_BUF (alias 247)	0x0FF0 0000	0x0FFF FFFF	1024	External buffered region
EXT_NBUF (alias)	0x1000 0000	0x100F 0000	1024	External nonbuffered region
	...	...	...	
EXT_NBUF (alias)	0x1FF0 00000	0x1FFF FFFF	1024	External nonbuffered region
	...	...	...	
EXT_BUF (alias)	0xM000 0000	0xM0FF FFFF	1024	External buffered region
	...	...	...	
EXT_NBUF (alias)	0xFFF0 0000	0xFFFF FFFF	1024	External nonbuffered region

Each of these regions (EXT_BUF and EXT_NBUF) has the same memory map, aliased throughout the address range of the region. Table 6-6 lists iCONT1 memory mapping, and Table 6-7 lists iCONT2 memory mapping. Offsets shown are from the start of the region.

Table 6-6. iCONT1 Memory Mapping

Module	Offset in Region		Size
	Begin	End	KB
SL2 - Mem	0x0000 0000	0x0003 FFFF	256
Reserved	0x0004 0000	0x0007 FFFF	256
iCONT1 - DMem	0x0008 0000	0x0008 3FFF	16
Reserved	0x0008 4000	0x0008 7FFF	16
iCONT1 - IMem	0x0008 8000	0x0008 FFFF	32
iCONT2 - DMem	0x0009 0000	0x0009 3FFF	16
Reserved	0x0009 4000	0x0009 7FFF	16
iCONT2 - IMem	0x0009 8000	0x0009 FFFF	32
ECD3 - Mem	0x000A 0000	0x000A 7FFF	32
CALC3 - Mem	0x000A 8000	0x000A BFFF	16
Reserved	0x000A C000	0x000A FFFF	16
MC3 - Mem	0x000B 0000	0x000B 7FFF	32
iPE3 - Mem	0x000B 8000	0x000B 8FFF	4
Reserved	0x000B 9000	0x000C 0FFF	32
SMSET - Reg	0x000C 1000	0x000C 1FFF	4
SMSET - SWI	0x000C 2000	0x000C 27FF	2
Reserved	0x000C 2800	0x000C FFFF	54
vDMA - Reg	0x000D 0000	0x000D 1FFF	8
iLF3 - Reg	0x000D 2000	0x000D 2FFF	4
Reserved	0x000D 3000	0x000D 3FFF	4

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Table 6-6. iCONT1 Memory Mapping (continued)

Module	Offset in Region		Size
	Begin	End	KB
iME3 - Reg	0x000D 4000	0x000D 7FFF	16
CALC3 - Reg	0x000D 8000	0x000D 87FF	2
iPE3 - Reg	0x000D 8800	0x000D 8FFF	2
MC3 - Reg	0x000D 9000	0x000D 97FF	2
ECD3 - Reg	0x000D 9800	0x000D 9FFF	2
Reserved	0x000D A000	0x000D A3FF	1
SysControl	0x000D A400	0x000D A7FF	1
Mailbox	0x000D A800	0x000D ABFF	1
Reserved	0x000D AC00	0x000D FFFF	21
iCONT1 - SyncBox	0x000E 0000	0x000E 07FF	2
iCONT2 - SyncBox	0x000E 0800	0x000E 0FFF	2
iLF3 - SyncBox	0x000E 1000	0x000E 17FF	2
iME3 - SyncBox	0x000E 1800	0x000E 1FFF	2
CALC3 - SyncBox	0x000E 2000	0x000E 27FF	2
iPE3 - SyncBox	0x000E 2800	0x000E 2FFF	2
MC3 - SyncBox	0x000E 3000	0x000E 37FF	2
ECD3 - SyncBox	0x000E 3800	0x000E 3FFF	2
Reserved	0x000E 4000	0x000E FFFF	48
iCONT1 - Reg(1)	0x000F 0000	0x000F 0FFF	4
iCONT2 - Reg	0x000F 1000	0x000F 1FFF	4
iCONT1 - Reg (2)	0x000F 2000	0x000F 2FFF	4
Reserved	0x000F 3000	0x000F FFFF	52

(1) iCONT1 private access to its own registers

(2) iCONT1 self-access to its own registers

Table 6-7. iCONT2 Memory Mapping

Module	Offset in Region		Size
	Begin	End	KB
SL2 - Mem	0x0000 0000	0x0003 FFFF	256
Reserved	0x0004 0000	0x0007 FFFF	256
iCONT1 - DMem	0x0008 0000	0x0008 3FFF	16
Reserved	0x0008 4000	0x0008 7FFF	16
iCONT1 - IMem	0x0008 8000	0x0008 FFFF	32
iCONT2 - DMem	0x0009 0000	0x0009 3FFF	16
Reserved	0x0009 4000	0x0009 7FFF	16
iCONT2 - IMem	0x0009 8000	0x0009 FFFF	32
ECD3 - Mem	0x000A 0000	0x000A 7FFF	32
CALC3 - Mem	0x000A 8000	0x000A BFFF	16
Reserved	0x000A C000	0x000A FFFF	16
MC3 - Mem	0x000B 0000	0x000B 7FFF	32
iPE3 - Mem	0x000B 8000	0x000B 8FFF	4
Reserved	0x000B 9000	0x000C 0FFF	32
SMSET - Reg	0x000C 1000	0x000C 1FFF	4
SMSET - SWI	0x000C 2000	0x000C 27FF	2
Reserved	0x000C 2800	0x000C FFFF	54

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Table 6-7. iCONT2 Memory Mapping (continued)

Module	Offset in Region		Size
vDMA - Reg	0x000D 0000	0x000D 1FFF	8
iLF3 - Reg	0x000D 2000	0x000D 2FFF	4
Reserved	0x000D 3000	0x000D 3FFF	4
iME3 - Reg	0x000D 4000	0x000D 7FFF	16
CALC3 - Reg	0x000D 8000	0x000D 87FF	2
iPE3 - Reg	0x000D 8800	0x000D 8FFF	2
MC3 - Reg	0x000D 9000	0x000D 97FF	2
ECD3 - Reg	0x000D 9800	0x000D 9FFF	2
Reserved	0x000D A000	0x000D A3FF	1
SysControl	0x000D A400	0x000D A7FF	1
Mailbox	0x000D A800	0x000D ABFF	1
Reserved	0x000D AC00	0x000D FFFF	21
iCONT1 - SyncBox	0x000E 0000	0x000E 07FF	2
iCONT2 - SyncBox	0x000E 0800	0x000E 0FFF	2
iLF3 - SyncBox	0x000E 1000	0x000E 17FF	2
iME3 - SyncBox	0x000E 1800	0x000E 1FFF	2
CALC3 - SyncBox	0x000E 2000	0x000E 27FF	2
iPE3 - SyncBox	0x000E 2800	0x000E 2FFF	2
MC3 - SyncBox	0x000E 3000	0x000E 37FF	2
ECD3 - SyncBox	0x000E 3800	0x000E 3FFF	2
Reserved	0x000E 4000	0x000E FFFF	48
iCONT1 - Reg	0x000F 0000	0x000F 0FFF	4
iCONT2 - Reg	0x000F 1000	0x000F 1FFF	4
Reserved	0x000F 2000	0x000F 2FFF	4
iCONT2 - Reg	0x000F 3000	0x000F 3FFF	4
Reserved	0x000F 4000	0x000F FFFF	48

1. iCONT2 private access to its own registers
2. iCONT2 self-access to its own registers

NOTE: Definition of iCONT self-access and private access:

- Self-access: Direct access of iCONT to its own memory-mapped registers (MMRs) (reduced latency); that is, without using the IVA-HD local interconnect. Internal iCONT configuration (CFG) registers are not visible. Only IRQ, DM, and SBH registers can be accessed.
- Private access: Access through IVA-HD local interconnect. By default, all iCONT accesses described in Table 6-6 and Table 6-7 are private, except for corresponding self-access. In case of iCONT private access to its own registers, internal iCONT CFG registers are visible (on top of IRQ, DM, and SBH).

NOTE: Examples of start address:

- Buffered region: 0x0080 0000, 0x0090 0000, 0x00A0 0000, 0x0FF0 0000, 0x2000 0000, etc.
- Nonbuffered region: 0x1000 0000, 0x1010 0000, 0x1020 0000, 0x1FF0 0000, 0x3000 0000, etc.

Table 6-8 shows IVA-HD modules and memory addresses forthe DSP processor and L3 access.

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Table 6-8. DSP and L3 Interconnect Memory Mapping

Module	Begin Offset	DSP Private Address		L3 Interconnect Address		Size
		Begin	End	Begin	End	(KB)
iCONT1 - DMem	0x0000 0000	0x01E0 0000	0x01E0 3FFF	0x5A00 0000	0x5A00 3FFF	16
Reserved	0x0000 4000	0x01E0 4000	0x01E0 7FFF	0x5A00 4000	0x5A00 7FFF	16
iCONT1 - IMem	0x0000 8000	0x01E0 8000	0x01E0 FFFF	0x5A00 8000	0x5A00 FFFF	32
iCONT2 - DMem	0x0001 0000	0x01E1 0000	0x01E1 3FFF	0x5A01 0000	0x5A01 3FFF	16
Reserved	0x0001 4000	0x01E1 4000	0x01E1 7FFF	0x5A01 4000	0x5A01 7FFF	16
iCONT2 - IMem	0x0001 8000	0x01E1 8000	0x01E1 FFFF	0x5A01 8000	0x5A01 FFFF	32
ECD3 - Mem	0x0002 0000	0x01E2 0000	0x01E2 7FFF	0x5A02 0000	0x5A02 7FFF	32
CALC3 - Mem	0x0002 8000	0x01E2 8000	0x01E2 BFFF	0x5A02 8000	0x5A02 BFFF	16
Reserved	0x0002 C000	0x01E2 C000	0x01E2 FFFF	0x5A02 C000	0x5A02 FFFF	16
MC3 - Mem	0x0003 0000	0x01E3 0000	0x01E3 7FFF	0x5A03 0000	0x5A03 7FFF	32
iPE3 - Mem	0x0003 8000	0x01E3 8000	0x01E3 8FFF	0x5A03 8000	0x5A03 8FFF	4
Reserved	0x0003 9000	0x01E3 9000	0x01E4 FFFF	0x5A03 9000	0x5A04 FFFF	92
vDMA - Reg	0x0005 0000	0x01E5 0000	0x01E5 1FFF	0x5A05 0000	0x5A05 1FFF	8
iLF3 - Reg	0x0005 2000	0x01E5 2000	0x01E5 2FFF	0x5A05 2000	0x5A05 2FFF	4
Reserved	0x0005 3000	0x01E5 3000	0x01E5 3FFF	0x5A05 3000	0x5A05 3FFF	4
iME3 - Reg	0x0005 4000	0x01E5 4000	0x01E5 7FFF	0x5A05 4000	0x5A05 7FFF	16
CALC3 - Reg	0x0005 8000	0x01E5 8000	0x01E5 87FF	0x5A05 8000	0x5A05 87FF	2
iPE3 - Reg	0x0005 8800	0x01E5 8800	0x01E5 8FFF	0x5A05 8800	0x5A05 8FFF	2
MC3 - Reg	0x0005 9000	0x01E5 9000	0x01E5 97FF	0x5A05 9000	0x5A05 97FF	2
ECD3 - Reg	0x0005 9800	0x01E5 9800	0x01E5 9FFF	0x5A05 9800	0x5A05 9FFF	2
Reserved	0x0005 A000	0x01E5 A000	0x01E5 A3FF	0x5A05 A000	0x5A05 A3FF	1
SysControl	0x0005 A400	0x01E5 A400	0x01E5 A7FF	0x5A05 A400	0x5A05 A7FF	1
Mailbox	0x0005 A800	0x01E5 A800	0x01E5 ABFF	0x5A05 A800	0x5A05 ABFF	1
Reserved	0x0005 AC00	0x01E5 AC00	0x01E5 FFFF	0x5A05 AC00	0x5A05 FFFF	21
iCONT1 - SBox	0x0006 0000	0x01E6 0000	0x01E6 07FF	0x5A06 0000	0x5A06 07FF	2
iCONT2 - SBox	0x0006 0800	0x01E6 0800	0x01E6 0FFF	0x5A06 0800	0x5A06 0FFF	2
iLF3 - SyncBox	0x0006 1000	0x01E6 1000	0x01E6 17FF	0x5A06 1000	0x5A06 17FF	2
iME3 - SyncBox	0x0006 1800	0x01E6 1800	0x01E6 1FFF	0x5A06 1800	0x5A06 1FFF	2
CALC3 - SyncBox	0x0006 2000	0x01E6 2000	0x01E6 27FF	0x5A06 2000	0x5A06 27FF	2
iPE3 - SyncBox	0x0006 2800	0x01E6 2800	0x01E6 2FFF	0x5A06 2800	0x5A06 2FFF	2
MC3 - SyncBox	0x0006 3000	0x01E6 3000	0x01E6 37FF	0x5A06 3000	0x5A06 37FF	2
ECD3 - SyncBox	0x0006 3800	0x01E6 3800	0x01E6 3FFF	0x5A06 3800	0x5A06 3FFF	2
Reserved	0x0006 4000	0x01E6 4000	0x01E6 FFFF	0x5A06 4000	0x5A06 FFFF	48
iCONT1 - Reg	0x0007 0000	0x01E7 0000	0x01E7 0FFF	0x5A07 0000	0x5A07 0FFF	4
iCONT2 - Reg	0x0007 1000	0x01E7 1000	0x01E7 1FFF	0x5A07 1000	0x5A07 1FFF	4
Reserved	0x0007 2000	0x01E7 2000	0x01E7 FFFF	0x5A07 2000	0x5A07 FFFF	56

6.1.3 IVA-HD Register Manual

CAUTION

This section provides information about iCONT memory mapping (private access). This information represents only the address offsets from the start of relevant buffered (EXT_BUF) or nonbuffered (EXT_NBUF) regions. For more information, see Section 6.1.2.3, *IVA-HD Memory Mapping*.

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6.1.3.1 IVA-HD Instance Summary

Table 6-9 shows the IVA-HD instance summary.

Table 6-9. IVA-HD Instance Summary

Module Name	Base Address (L3 Interconnect)	Base Address (DSP Private Access)	Base Address (iCONT Private Access)	Size
SYSCTRL	0x5A05 A400	0x01E5 A400	0x000D A400	1KB

NOTE: Private access is an access through the IVA-HD local interconnect without using the L3 interconnect.

6.1.3.2 SYSCTRL Registers

6.1.3.2.1 SYSCTRL Register Summary

Table 6-10 lists the mapping summary for the SYSCTRL registers.

CAUTION

SYSCTRL registers are limited to 32-bit access; 16-bit and 8-bit accesses are not allowed and can corrupt register content.

Table 6-10. SYSCTRL Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	Physical Address (L3 Interconnect)	Physical Address (DSP Private Access)	Physical Address (iCONT Private Access)
IVAHD_REVISION	R	32	0x0000 0000	0x5A05 A400	0x01E5 A400	0x000D A400
IVAHD_HWINFO	R	32	0x0000 0004	0x5A05 A404	0x01E5 A404	0x000D A404
IVAHD_SYSCONFIG	RW	32	0x0000 0010	0x5A05 A410	0x01E5 A410	0x000D A410
RESERVED	RW	32	0x0000 0020	0x5A05 A420	0x01E5 A420	0x000D A420
IVAHD_IRQSTATUS_RAW	RW	32	0x0000 0024	0x5A05 A424	0x01E5 A424	0x000D A424
IVAHD_IRQSTATUS	RW	32	0x0000 0028	0x5A05 A428	0x01E5 A428	0x000D A428
IVAHD_IRQENABLE_SET	RW	32	0x0000 002C	0x5A05 A42C	0x01E5 A42C	0x000D A42C
IVAHD_IRQENABLE_CLR	RW	32	0x0000 0030	0x5A05 A430	0x01E5 A430	0x000D A430
IVAHD_SYNC_IRQSTATUS_RAW	RW	32	0x0000 0034	0x5A05 A434	0x01E5 A434	0x000D A434
IVAHD_SYNC_IRQSTATUS	RW	32	0x0000 0038	0x5A05 A438	0x01E5 A438	0x000D A438
IVAHD_SYNC_IRQENABLE_SET	RW	32	0x0000 003C	0x5A05 A43C	0x01E5 A43C	0x000D A43C
IVAHD_SYNC_IRQENABLE_CLR	RW	32	0x0000 0040	0x5A05 A440	0x01E5 A440	0x000D A440
IVAHD_CLKCTRL	RW	32	0x0000 0050	0x5A05 A450	0x01E5 A450	0x000D A450
IVAHD_CLKST	R	32	0x0000 0054	0x5A05 A454	0x01E5 A454	0x000D A454
IVAHD_STDBYST	R	32	0x0000 0058	0x5A05 A458	0x01E5 A458	0x000D A458

6.1.3.2.2 SYSCTRL Register Description

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Table 6-11. IVAHD_REVISION

Address Offset	0x0000 0000		
Physical Address	0x5A05 A400 0x01E5 A400 0x000D A400	**Instance**	SYSCTRL_L3 SYSCTRL_DSP SYSCTRL_ICONT
Description	IP revision identifier (X.Y.R). Used by software to track features, bugs, and compatibility		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP revision	R	TI Internal Data

Table 6-12. Register Call Summary for Register IVAHD_REVISION

IVA-HD Overview

- SYSCTRL Register Summary: [0]

Table 6-13. IVAHD_HWINFO

Address Offset	0x0000 0004		
Physical Address	0x5A05 A404 0x01E5 A404 0x000D A404	**Instance**	SYSCTRL_L3 SYSCTRL_DSP SYSCTRL_ICONT
Description	Information about the IP module's hardware configuration.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																ECD3	MC3	IPE3	CALC3	IME3	ILF3	VDMA	ICONT2	ICONT1	SL2BANK	SL2SIZE					

Bits	Field Name	Description	Type	Reset
31:15	RESERVED	Reserved	R	0x00000
14	ECD3	ECD3 available 0: ECD3 not present 1: ECD3 present	R	1
13	MC3	MC3 available 0: MC3 not present 1: MC3 present	R	1
12	IPE3	iPE3 available 0: iPE3 not present 1: iPE3 present	R	1
11	CALC3	CALC3 available 0: CALC3 not present 1: CALC3 present	R	1
10	IME3	iME3 available 0: iME3 not present 1: iME3 present	R	1
9	ILF3	iLF3 available 0: iLF3 not present 1: iLF3 present	R	1
8	VDMA	vDMA available 0: vDMA not present 1: vDMA present	R	1

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Bits	Field Name	Description	Type	Reset
7	ICONT2	iCONT2 available 0: iCONT2 not present 1: iCONT2 present	R	1
6	ICONT1	iCONT1 available 0: iCONT1 not present 1: iCONT1 present	R	1
5:4	SL2BANK	Read 0x0: 1 memory bank Read 0x1: 2 memory bank Read 0x2: 4 memory bank Read 0x3: 8 memory bank	R	0x3
3:0	SL2SIZE	Size of SL2 memory Read 0x1: 16KB Read 0x2: 32KB Read 0x3: 48KB Read 0x4: 64KB Read 0x5: 96KB Read 0x6: 128KB Read 0x7: 160KB Read 0x8: 192KB Read 0x9: 224KB Read 0xA: 256KB Read 0xB: 320KB Read 0xC: 384KB Read 0xD: 448KB Read 0xE: 512KB	R	0xA

Table 6-14. Register Call Summary for Register IVAHD_HWINFO

IVA-HD Overview

- SYSCTRL Register Summary: [0]

Table 6-15. IVAHD_SYSCONFIG

Address Offset	0x0000 0010		
Physical Address	0x5A05 A410 0x01E5 A410 0x000D A410	**Instance**	SYSCTRL_L3 SYSCTRL_DSP SYSCTRL_ICONT
Description	Clock management configuration		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																										STANDBYMODE		IDLEMODE		RESERVED	

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Bits	Field Name	Description	Type	Reset
31:6	RESERVED	Reserved	R	0x0000000
5:4	STANDBYMODE	Configuration of the local initiator state management mode. By definition, initiator may generate read/write transaction as long as it is out of STANDBY state. 0x0 and 0x3: Reserved 0x1: No-standby mode: local initiator is unconditionally placed out of standby state. Backup mode, for debug only. 0x2: Smart-standby mode: local initiator standby status depends on local conditions, that is, the module's functional requirement from the initiator. IP module shall not generate (initiator-related) wakeup events.	RW	0x2
3:2	IDLEMODE	Configuration of the local target state management mode. By definition, target can handle read/write transaction as long as it is out of IDLE state. 0x0 and 0x3: Reserved 0x1: No-idle mode: local target never enters idle state. Backup mode, for debug only. 0x2: Smart-idle mode: local target's idle state eventually follows (acknowledges) the system's idle requests, depending on the IP module's internal requirements. IP module shall not generate (IRQ- or DMA-request-related) wakeup events.	RW	0x2
1:0	RESERVED	Reserved	R	0x0

Table 6-16. Register Call Summary for Register IVAHD_SYSCONFIG

IVA-HD Overview
- IVA-HD Power Management: [0] [1]
- SYSCTRL Register Summary: [2]

Table 6-17. IVAHD_IRQSTATUS_RAW

Address Offset	0x0000 0024		
Physical Address	0x5A05 A424 0x01E5 A424 0x000D A424	**Instance**	SYSCTRL_L3 SYSCTRL_DSP SYSCTRL_ICONT
Description	Per-event raw interrupt status vector. Raw status is set even if event is not enabled. Write 1 to set the (raw) status, mostly for debug.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															SYSCTRL_CLKERR

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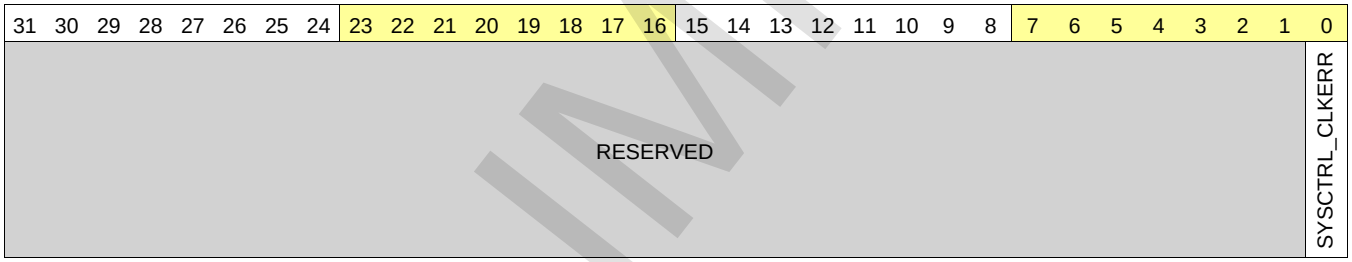
Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	SYSCTRL_CLKERR	Settable raw status for Clock Programming Error event Write 0x0: No action Read 0x0: No event pending Read 0x1: Event pending Write 0x1: Set event (debug)	RW	0

Table 6-18. Register Call Summary for Register IVAHD_IRQSTATUS_RAW

IVA-HD Overview
- SYSCTRL Register Summary: [1]

Table 6-19. IVAHD_IRQSTATUS

Address Offset	0x0000 0028		
Physical Address	0x5A05 A428 0x01E5 A428 0x000D A428	**Instance**	SYSCTRL_L3 SYSCTRL_DSP SYSCTRL_ICONT
Description	Per-event "enabled" interrupt status vector, line 0. Enabled status is not set unless event is enabled. Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, that is, even if not enabled).		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	SYSCTRL_CLKERR	Clearable, enabled status for Clock Programming Error event Write 0x0: No action Read 0x0: No (enabled) event pending Read 0x1: Event pending Write 0x1: Clear (raw) event	RW	0

Table 6-20. Register Call Summary for Register IVAHD_IRQSTATUS

IVA-HD Overview
- SYSCTRL Register Summary: [3]

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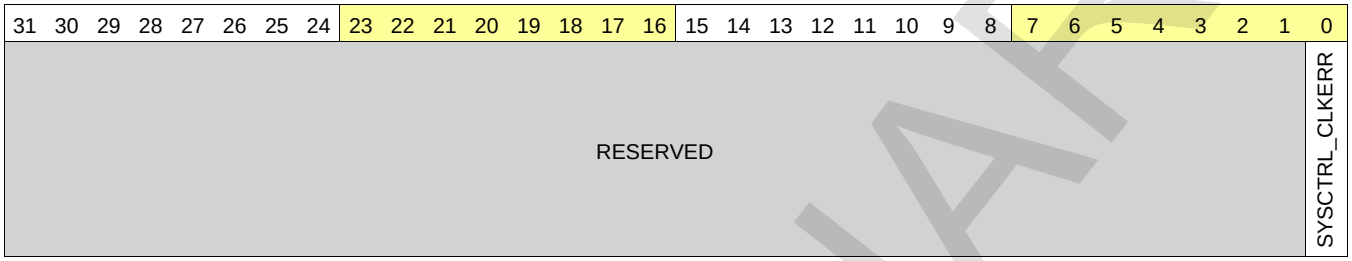
Table 6-21. IVAHD_IRQENABLE_SET

Address Offset	0x0000 002C		
Physical Address	0x5A05 A42C 0x01E5 A42C 0x000D A42C	**Instance**	SYSCTRL_L3 SYSCTRL_DSP SYSCTRL_ICONT
Description	Per-event interrupt enable bit vector. Write 1 to set (enable interrupt). Readout equal to corresponding _CLR register.		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	SYSCTRL_CLKERR	Clock Programing Error Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW W1toSet	0

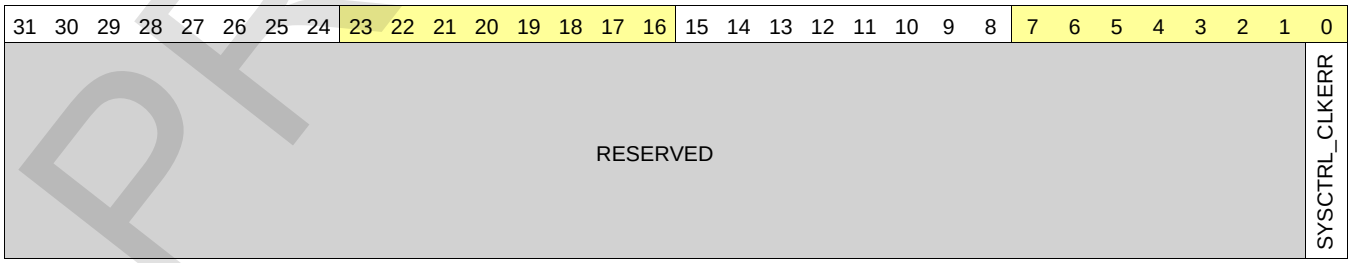
Table 6-22. Register Call Summary for Register IVAHD_IRQENABLE_SET

IVA-HD Overview

- SYSCTRL Register Summary: [3]

Table 6-23. IVAHD_IRQENABLE_CLR

Address Offset	0x0000 0030		
Physical Address	0x5A05 A430 0x01E5 A430 0x000D A430	**Instance**	SYSCTRL_L3 SYSCTRL_DSP SYSCTRL_ICONT
Description	Per-event interrupt enable bit vector. Write 1 to clear (disable interrupt). Readout equal to corresponding _SET register.		
Type	RW		



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Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	SYSCTRL_CLKERR	Clock Programing Error Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW	0

Table 6-24. Register Call Summary for Register IVAHD_IRQENABLE_CLR

IVA-HD Overview
- SYSCTRL Register Summary: [1]

Table 6-25. IVAHD_SYNC_IRQSTATUS_RAW

Address Offset	0x0000 0034		
Physical Address	0x5A05 A434 0x01E5 A434 0x000D A434	**Instance**	SYSCTRL_L3 SYSCTRL_DSP SYSCTRL_ICONT
Description	Per-event raw interrupt status vector. Raw status is set even if event is not enabled. Write 1 to set the (raw) status, mostly for debug.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								SYNC_INPUT7_0							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Reserved	R	0x000000
7:0	SYNC_INPUT7_0	Settable raw status for SYNC INPUT event. For each bit of the bit field: Read 0: No event pending Read 1: Event pending Write 0: No action Write 1: Set event (debug)	RW	0x00

Table 6-26. Register Call Summary for Register IVAHD_SYNC_IRQSTATUS_RAW

IVA-HD Overview
- SYSCTRL Register Summary: [1]

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Table 6-27. IVAHD_SYNC_IRQSTATUS

Address Offset	0x0000 0038		
Physical Address	0x5A05 A438 0x01E5 A438 0x000D A438	**Instance**	SYSCTRL_L3 SYSCTRL_DSP SYSCTRL_ICONT
Description	Per-event "enabled" interrupt status vector, line 0. Enabled status is not set unless event is enabled. Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, that is, even if not enabled).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								SYNC_INPUT7_0							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Reserved	R	0x000000
7:0	SYNC_INPUT7_0	Clearable, enabled status for SYNC INPUT event. For each bit of the bit field: Read 0: No (enabled) event pending Read 1: Event pending Write 0: No action Write 1: Clear (raw) event	RW	0x00

Table 6-28. Register Call Summary for Register IVAHD_SYNC_IRQSTATUS

IVA-HD Overview

- SYSCTRL Register Summary: [1]

Table 6-29. IVAHD_SYNC_IRQENABLE_SET

Address Offset	0x0000 003C		
Physical Address	0x5A05 A43C 0x01E5 A43C 0x000D A43C	**Instance**	SYSCTRL_L3 SYSCTRL_DSP SYSCTRL_ICONT
Description	Per-event interrupt enable bit vector. Write 1 to set (enable interrupt). Readout equal to corresponding _CLR register.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								SYNC_INPUT7_0							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Reserved	R	0x000000
7:0	SYNC_INPUT7_0	Enable for interrupt event. For each bit of the bit field: Read 0: Interrupt disabled (masked) Read 1: Interrupt enabled Write 0: No action Write 1: Enable interrupt	RW	0x00

Table 6-30. Register Call Summary for Register IVAHD_SYNC_IRQENABLE_SET

IVA-HD Overview

- SYSCTRL Register Summary: [1]

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Table 6-31. IVAHD_SYNC_IRQENABLE_CLR

Address Offset	0x0000 0040		
Physical Address	0x5A05 A440 0x01E5 A440 0x000D A440	**Instance**	SYSCTRL_L3 SYSCTRL_DSP SYSCTRL_ICONT
Description	Per-event interrupt enable bit vector. Write 1 to clear (disable interrupt). Readout equal to corresponding _SET register.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								SYNC_INPUT7_0							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Reserved	R	0x000000
7:0	SYNC_INPUT7_0	Enable for interrupt event. For each bit of the bitfiled: Read 0: Interrupt disabled (masked) Read 1: Interrupt enabled Write 0: No action Write 1: Disable interrupt	RW	0x00

Table 6-32. Register Call Summary for Register IVAHD_SYNC_IRQENABLE_CLR

IVA-HD Overview

- SYSCTRL Register Summary: [1]

Table 6-33. IVAHD_CLKCTRL

Address Offset	0x0000 0050		
Physical Address	0x5A05 A450 0x01E5 A450 0x000D A450	**Instance**	SYSCTRL_L3 SYSCTRL_DSP SYSCTRL_ICONT
Description	IVA-HD clock control register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																					SMSET	MSGIF	ECD3	MC3	IPE3	CALC3	ILF3	IME3	VDMA	ICONT2	ICONT1

Bits	Field Name	Description	Type	Reset
31:11	RESERVED	Reserved	R	0x000000
10	SMSET	Clock control of SMSET 0: Exit idle state and start SMSET clock 1: Request SMSET to go to idle state and stop SMSET clock Note: Shutting down SMSET clock may hang system if software performs software instrumentation and/or access to its configuration port.	RW	0
9	MSGIF	Clock control of MSGIF 0: Exit idle state and start MSGIF clock 1: Request MSGIF to go to idle state and stop MSGIF clock	RW	0
8	ECD3	Clock control of ECD3 0: Exit idle state and start ECD3 clock 1: Request ECD3 to go to idle state and stop ECD3 clock	RW	0

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Bits	Field Name	Description	Type	Reset
7	MC3	Clock control of MC3 0: Exit idle state and start MC3 clock 1: Request MC3 to go to idle state and stop MC3 clock	RW	0
6	IPE3	Clock control of iPE3 0: Exit idle state and start iPE3 clock 1: Request iME3 to go to idle state and stop iPE3 clock	RW	0
5	CALC3	Clock control of CALC3 0: Exit idle state and start CALC3 clock 1: Request CALC3 to go to idle state and stop CALC3 clock	RW	0
4	ILF3	Clock control of iLF3 0: Exit idle state and start iLF3 clock 1: Request iLF3 to go to idle state and stop iLF3 clock	RW	0
3	IME3	Clock control of iME3 0: Exit idle state and start iME3 clock 1: Request iME3 to go to idle state and stop iME3 clock	RW	0
2	VDMA	Clock control of vDMA 0: Exit idle state and start vDMA clock 1: Request vDMA to go to idle state and stop vDMA clock	RW	0
1	ICONT2	Clock control of iCONT2 0: Exit idle state and start iCONT2 clock 1: Request iCONT2 to go to idle state and stop iCONT2 clock	RW	0
0	ICONT1	Clock control of iCONT1 0: Exit idle state and start iCONT1 clock 1: Request iCONT1 to go to idle state and stop iCONT1 clock	RW	0

Table 6-34. Register Call Summary for Register IVAHD_CLKCTRL

IVA-HD Overview

- SYSCTRL Register Summary: [4]

Table 6-35. IVAHD_CLKST

Address Offset	0x0000 0054		
Physical Address	0x5A05 A454 0x01E5 A454 0x000D A454	**Instance**	SYSCTRL_L3 SYSCTRL_DSP SYSCTRL_ICONT
Description	IVA-HD clock status register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																					SMSET	MSGIF	ECD3	MC3	IPE3	CALC3	ILF3	IME3	VDMA	ICONT2	ICONT1

Bits	Field Name	Description	Type	Reset
31:11	RESERVED	Reserved	R	0x000000
10	SMSET	Clock status of SMSET 1: SMSET clock is active 0: SMSET clock is idled	R	0
9	MSGIF	Clock status of MSGIF 1: MSGIF clock is active 0: MSGIF clock is idled	R	0
8	ECD3	Clock status of ECD3 1: ECD3 clock is active 0: ECD3 clock is idled	R	0

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Bits	Field Name	Description	Type	Reset
7	MC3	Clock status of MC3 1: MC3 clock is active 0: MC3 clock is idled	R	0
6	IPE3	Clock status of iPE3 1: iPE3 clock is active 0: iPE3 clock is idled	R	0
5	CALC3	Clock status of CALC3 1: CALC3 clock is active 0: CALC3 clock is idled	R	0
4	ILF3	Clock status of iLF3 1: iLF3 clock is active 0: iLF3 clock is idled	R	0
3	IME3	Clock status of iME3 1: iME3 clock is active 0: iME3 clock is idled	R	0
2	VDMA	Clock status of vDMA 1: vDMA clock is active 0: vDMA clock is idled	R	0
1	ICONT2	Clock status of iCONT2 1: iCONT2 clock is active 0: iCONT2 clock is idled	R	0
0	ICONT1	Clock status of iCONT1 1: iCONT1 clock is active 0: iCONT1 clock is idled	R	0

Table 6-36. Register Call Summary for Register IVAHD_CLKST

IVA-HD Overview

- SYSCTRL Register Summary: [1]

Table 6-37. IVAHD_STDBYST

Address Offset	0x0000 0058		
Physical Address	0x5A05 A458 0x01E5 A458 0x000D A458	**Instance**	SYSCTRL_L3 SYSCTRL_DSP SYSCTRL_ICONT
Description	IVA-HD STANDBY status		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													vDMA	ICONT2	ICONT1

Bits	Field Name	Description	Type	Reset
31:3	RESERVED	Reserved	R	0x0000 0000
2	vDMA	vDMA Standby status 0: module is not in Standby 1: module is in Standby	R	1
1	ICONT2	iCONT2 Standby status 0: module is not in Standby 1: module is in Standby	R	1
0	ICONT1	iCONT1 Standby status 0: module is not in Standby 1: module is in Standby	R	1

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Table 6-38. Register Call Summary for Register IVAHD_STDBYST

IVA-HD Overview
• SYSCTRL Register Summary: [2]

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Dual Cortex-M3 MPU Subsystem

This chapter describes the dual Cortex-M3 microprocessor unit (MPU) subsystem.

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7.2 Dual Cortex-M3 MPU Subsystem Integration 1156
7.3 Dual Cortex-M3 MPU Subsystem Functional Description 1160
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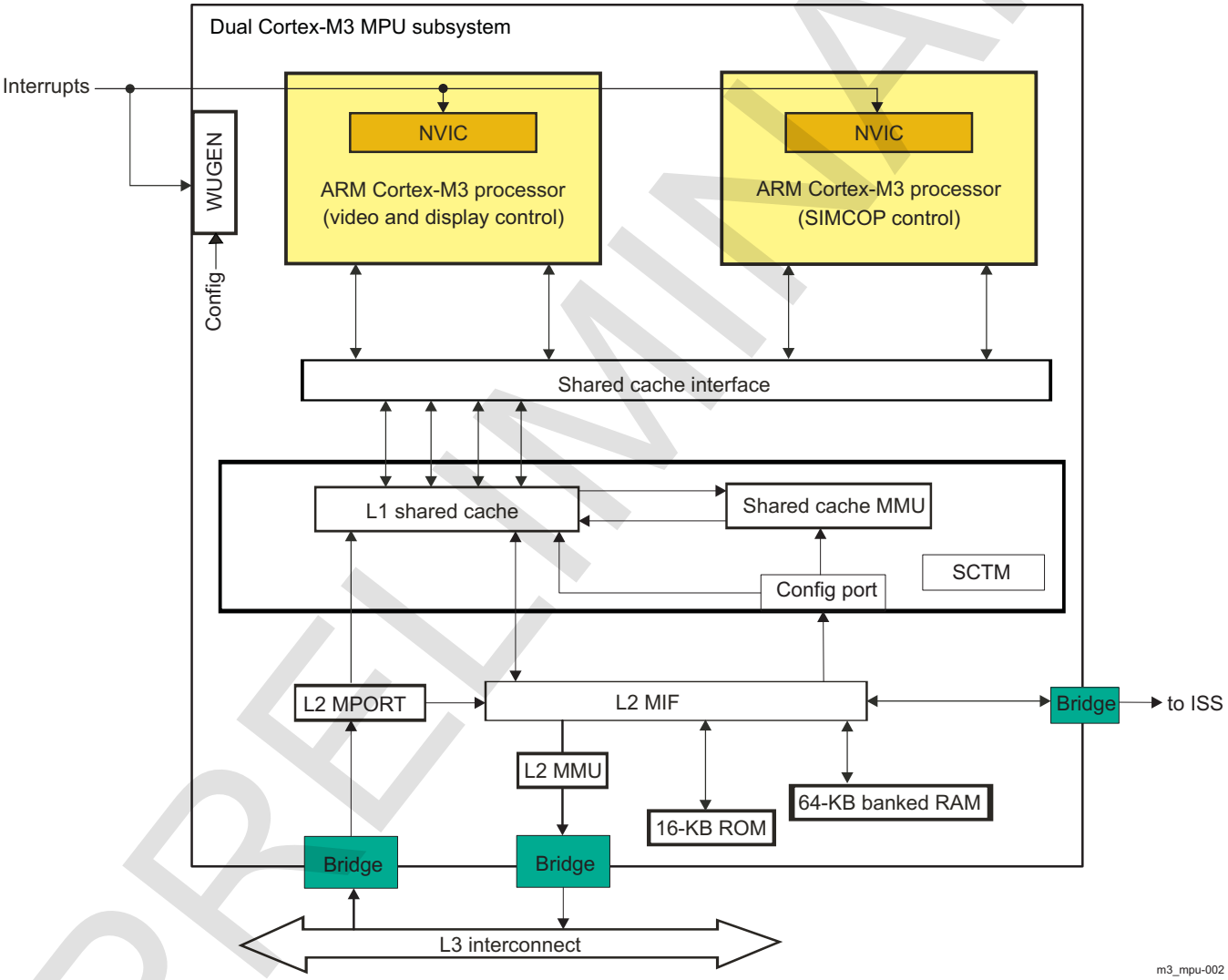
7.1 Dual Cortex-M3 MPU Subsystem Overview

7.1.1 Introduction

The dual Cortex™-M3 microprocessor (MPU) subsystem controls the imaging subsystem (ISS) and manages some controls of the video and display subsystem. It contains two ARM® Cortex-M3 processors (CPUs) that share a common level 1 (L1) cache (shared cache). One of the CPUs is dedicated to sequencing still image coprocessor (SIMCOP) accelerators, and the other CPU is dedicated to the ISS and display subsystem control. A single image real-time operating system (RTOS) runs on both cores, thereby minimizing the code size. The integrated interrupt handling of the dual Cortex-M3 MPU allows efficient control of the ISS. Figure 7-1 is a high-level block diagram of the dual Cortex-M3 MPU subsystem.

Figure 7-1. Dual Cortex-M3 MPU Subsystem Overview



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7.1.2 Features

The dual Cortex-M3 MPU subsystem integrates the following:

- Two ARM Cortex-M3 microprocessors:
  - ARMv7-M and Thumb®-2 instruction set architecture
  - Hardware division and single-cycle multiplication computational acceleration
  - Integrated nested vector interrupt controller (NVIC)
  - Integrated bus matrix
  - Registers:
    - Thirteen general-purpose 32-bit registers
    - Link register (LR)
    - Program counter (PC)
    - Program status register, xPSR
    - Two banked SP registers
  - Integrated power management
  - Extensive debug capabilities
- Shared cache interface:
  - Instruction and data interface
  - Supports paralleled accesses
- Level 2 (L2) MIF (master interface) splitter for access to memory or configuration port
- Configuration port: Used for shared cache maintance and shared cache memory management unit (MMU) configuration
- Shared cache:
  - 32KB divided into 16 banks
  - 4-way
  - Cache configuration lock/freeze/preload
  - Internal MMU:
    - 16-entry region-based address translation
    - Read/write control and access type control
    - Execute Never (XN) MMU protection policy
    - Little-endian format
- Subsystem counter timer module (SCTM)
- On-chip ROM and banked RAM memory
- Emulation/debug: Emulation feature embedded in Cortex-M3
- L2 MMU: 32 entries with walking table logic
- Wake-up generator (WUGEN): Generates wake-up request from external interrupts
- Power management:
  - Local power-management control: Configurable through the WUGEN registers.
  - Three sleep modes supported, controlled by the local power-management module.
  - Dual Cortex-M3 MPU is clock-gated in all sleep modes.
  - NVIC interrupt interface stays awake.

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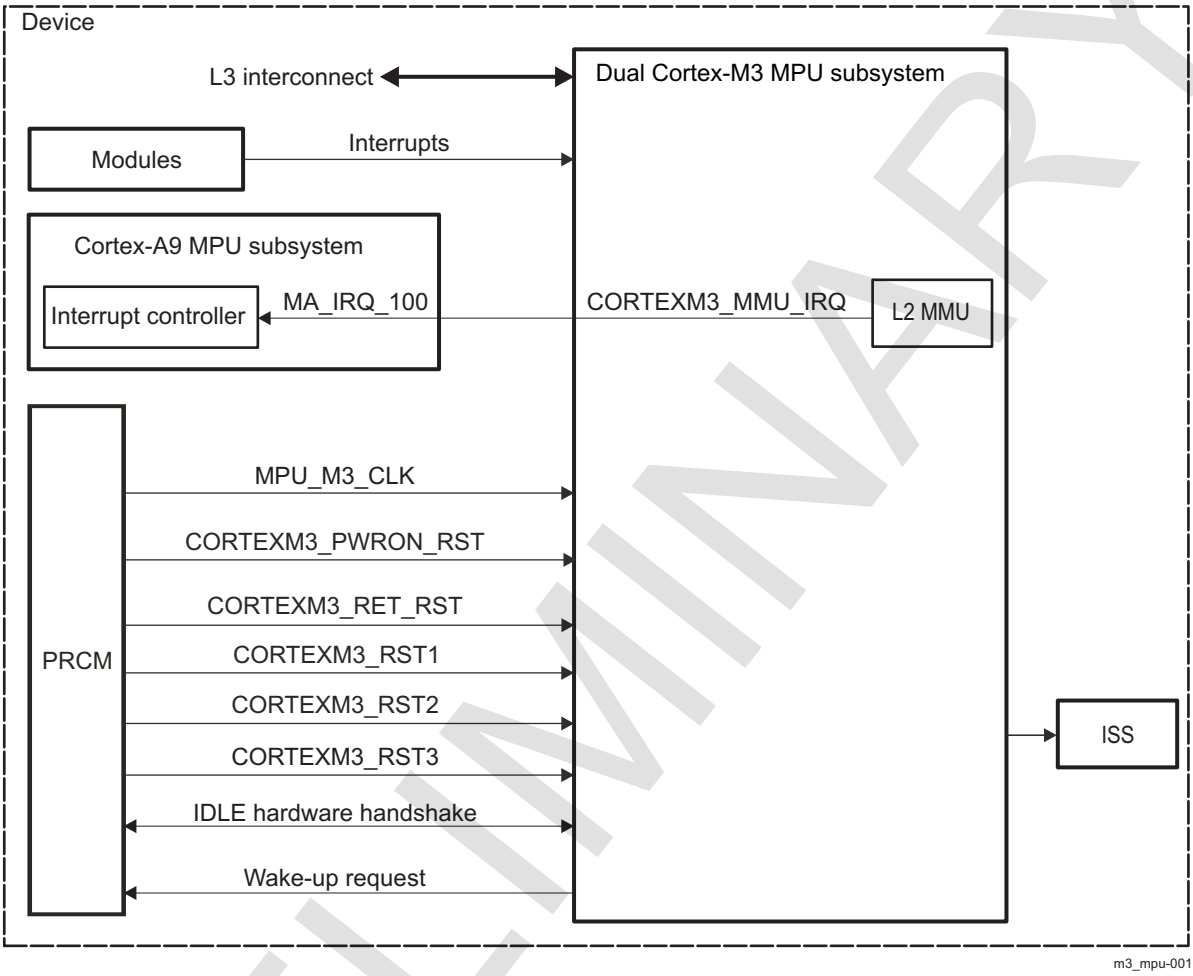
7.2 Dual Cortex-M3 MPU Subsystem Integration

Figure 7-2 shows the signals that interface with other modules.

Figure 7-2. Dual Cortex-M3 MPU Subsystem Integration Overview



NOTE: Some debug, trace, and emulation features are implemented in the MPU subsystem. This chapter includes only the clock/reset inputs and power-management aspects for these features.

Table 7-1 through Table 7-3 summarize the integration of the module in the device.

Table 7-1. Integration Attributes

Module Instance	Attributes	
	Power Domain	Interconnect
CORTEXM3	PD_CORE	L3

Table 7-2. Hardware Requests

Interrupt Requests				
Module Instance	Source Signal Name	Destination Signal Name	Destination	Description
L2_MMU	CORTEXM3_MMU_IRQ	MA_IRQ_100	Cortex-A9 MPU INTC	L2 MMU fault interrupt

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Table 7-3. Clocks and Resets

Clocks				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
CORTEXM3	MPU_M3_CLK	MPU_M3_CLK	PRCM module	Interface and functional clock
Resets				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
CORTEXM3	CORTEXM3_PWRON_RST	CORTEXM3_PWRON_RST	PRCM module	Power-on reset, used to reset the whole dual Cortex-M3 subsystem
	CORTEXM3_RET_RST	CORTEXM3_RET_RST	PRCM module	Retention reset to few retention logic inside the shared cache
	CORTEXM3_RST1	CORTEXM3_RST1	PRCM module	Reset signal to the video and display control CPU
	CORTEXM3_RST2	CORTEXM3_RST2	PRCM module	Reset signal to the SIMCOP CPU
	CORTEXM3_RST3	CORTEXM3_RST3	PRCM module	Reset signal to the shared cache and the L2 MMU

For more information about clocks, resets, and power domains, see Chapter 3, *Power, Reset, and Clock Management.*

7.2.1 Dual Cortex-M3 MPU Subsystem Clock and Reset Distribution

7.2.1.1 Clock Distribution

The dual Cortex-M3 subsystem receives only one clock, MPU_M3_CLK, which is divided in two for each ARM Cortex-M3 processor, ROM and RAM memory and the L2 MMU. The shared cache and the L2 MIF are directly clocked by the MPU_M3_CLK, without any division. For more information, see Chapter 3, *Power, Reset, and Clock Management*.

Figure 7-3 shows the clocking scheme of the MPU subsystem.

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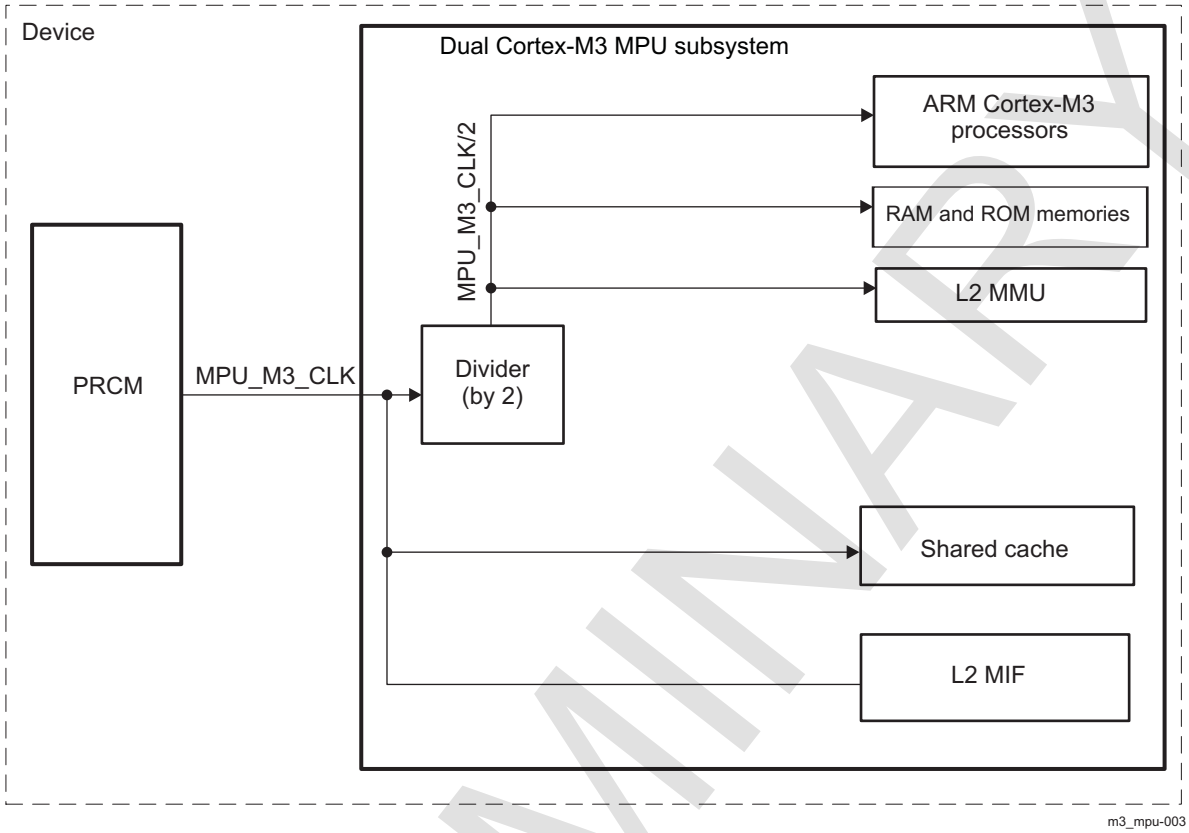
Figure 7-3. Dual Cortex-M3 MPU Subsystem Clocking Scheme



7.2.1.2 Reset Distribution

Three reset signals controlled by the power, reset, and clock management (PRCM) module let the two ARM Cortex-M3 processors and the rest of the dual Cortex-M3 MPU subsystem be reset independently. These three reset signals are: CORTEXM3_RST1, CORTEXM3_RST2, and CORTEXM3_RST3. The ARM Cortex-M3 processors must come out of reset one at a time:

- At CORTEXM3_RST1, the video and display control ARM Cortex-M3 processor comes out of reset, but the SIMCOP ARM Cortex-M3 processor is held in reset.
- The video and display control ARM Cortex-M3 controls the reset for the SIMCOP Cortex-M3 (through the PRCM register - RM_MPU_M3_RSTCTRL[1] RST2).

As the video and display control ARM Cortex-M3 controls the reset for the SIMCOP Cortex-M3 (through the PRCM registers), the code running on the video and display control ARM Cortex-M3 decides the mode of operation, whether it is:

- Mode 1: One ARM Cortex-M3 processor is running, and the other processor is held on reset.
- Mode 2: The two ARM Cortex-M3 processors are running.

This decision of which mode to use is driven by the use case. If the software partitioning and performance requirement for a use case requires two Cortex-M3 processor to run simultaneously, the user must go to mode 2. If SIMCOP Cortex-M3 is not required for a particular use case, the user can remain in mode 1.

Figure 7-4 shows the reset scheme of the MPU subsystem.

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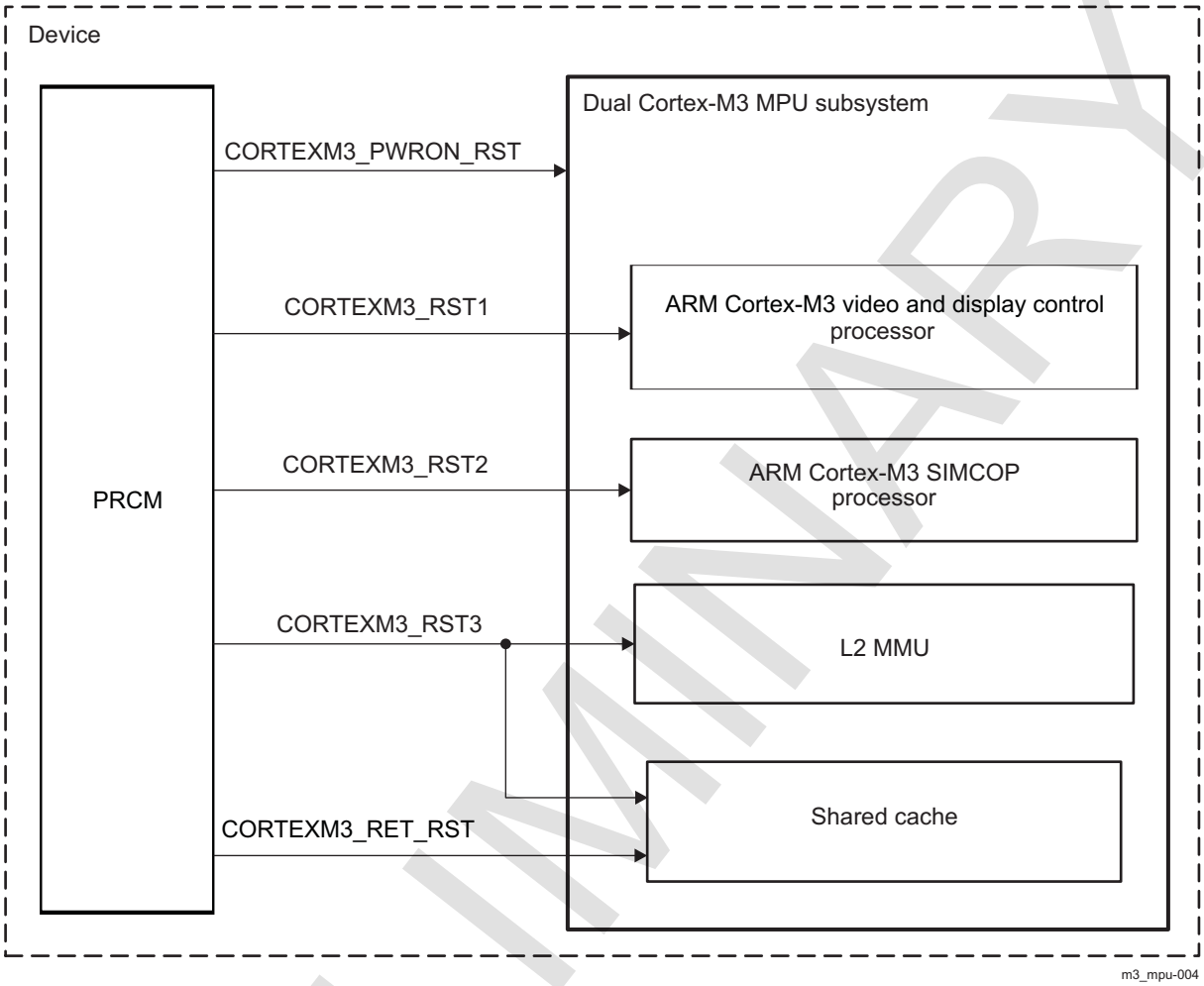
Figure 7-4. Dual Cortex-M3 MPU Subsystem Reset Scheme



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7.3 Dual Cortex-M3 MPU Subsystem Functional Description

7.3.1 Dual Cortex-M3 MPU Subsystem Block Diagram

The dual Cortex-M3 MPU subsystem integrates the following group of submodules:

- Two ARM Cortex-M3 processors: Two cores (r2p0 revision), one dedicated to sequencing SIMCOP accelerators and the other dedicated for video and display subsystem control. For a description of the ARM Cortex-M3 processor, see the *ARM Cortex-M3 Technical Reference Manual* .
- Interrupt controller (NVIC): To facilitate parallel processing, the interrupt mapping is the same for the two cores. Each Cortex-M3 processor receives the same interrupts, except for a few internal interrupts. Every IRQ line is shared between the two ARM processors. By properly configuring the NVIC registers inside each ARM processor, it can be ensured that the shared IRQ is taken by only one of the ARM processors (for more information, see Chapter 17, *Interrupt Controller*).
- Shared cache interface: The cache interface converts the data between the different protocols in the subsystem. Four ports are required to support the four buses from the ARM Cortex-M3 processors (two for each processor).The instruction and data connections from each ARM Cortex-M3 are multiplexed, but the ARM Cortex-M3 prevents conflicts on this connection. Default cache policies are provided through the sideband signals and are not used to access the cache. Cacheability is provided through the MMU inside the cache.
- Shared cache: Allows basic maintenance operations, which are performed through a dedicated interface: preload, lock, clean (write out dirty lines, but do not invalidate directly), and invalidate.
- Shared cache MMU: Provides the multiple access cache with region-based address translation, read/write control, access type control, and multilevel cache maintenance. Access to the shared cache MMU is done only under privilege mode. The shared cache MMU can be programmed by the Cortex-A9 MPU subsystem through the Cortex-M3 slave port.
- SCTM: Embedded in the shared cache
- Interconnect configuration port: Cache maintenance and MMU configuration are done through an interconnect slave port. Accesses must be performed to a noncacheable area that must be defined within the shared cache MMU. Interconnect accesses are generated from the L2 MIF.
- L2 MMU: Provides address translation for all the accesses done from the Cortex-M3 to the level 3 (L3) interconnect. The L2 MMU can be programmed by the Cortex-A9 MPU subsystem through the Cortex-M3 slave port.
- L3 interconnect port: Allows access to the system memories and peripherals. For the address mapping of the modules in the dual Cortex-M3 MPU subsystem, see Chapter 2, *Memory Mapping*.
- On-chip ROM and banked RAM memory. The ROM memory is used for boot/initialization purposes. For more information about the initialization of the device, see Chapter 27, *Initialization*. The address range of the ROM memory is from 0x5500_0000 to 0x5500_3FFF. The address range of the on-chip banked RAM memory is from 0x5502_0000 to 0x5502_FFFF.

Figure 7-5 is the block diagram of the dual Cortex-M3 MPU subsystem.

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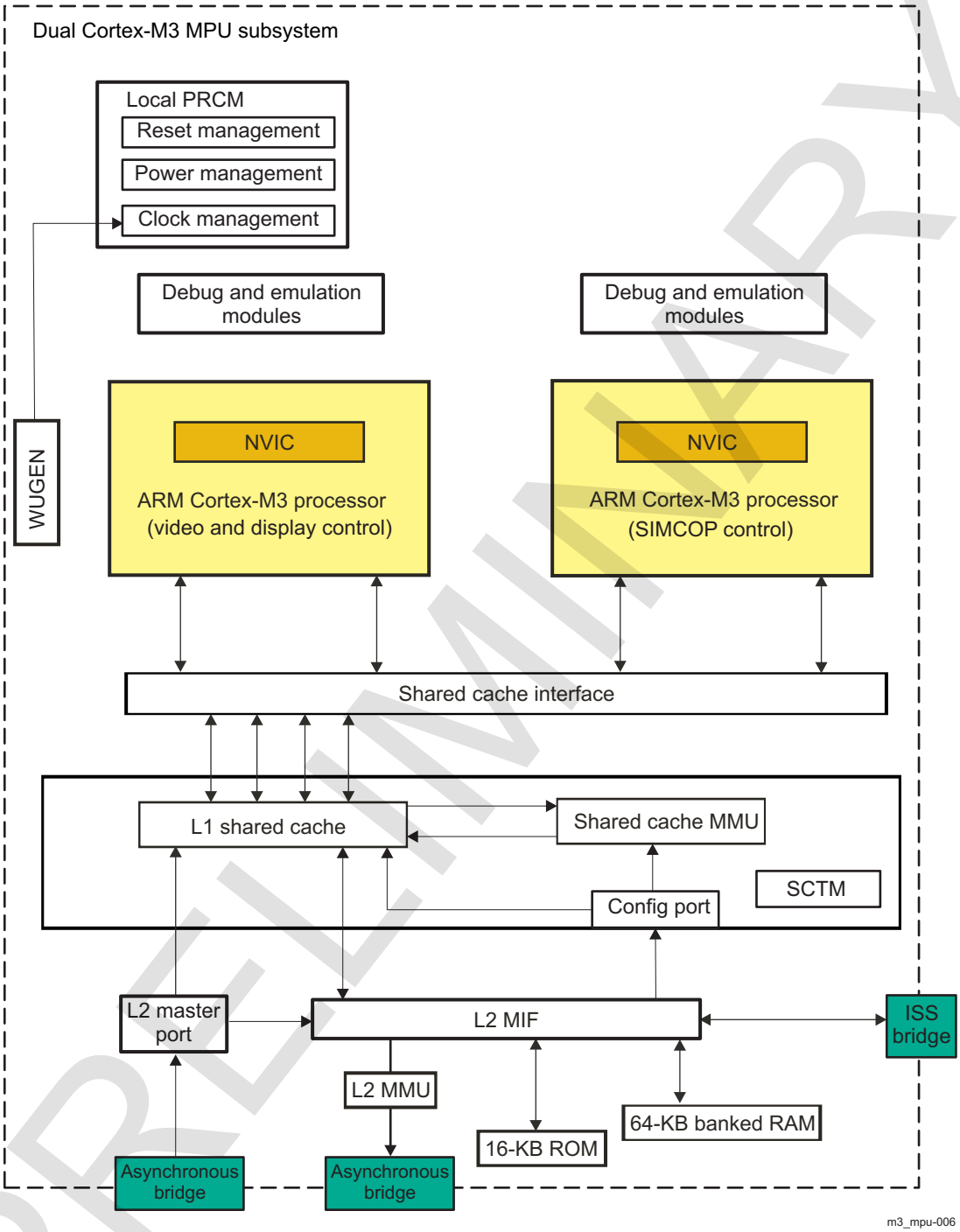
Figure 7-5. Dual Cortex-M3 MPU Block Diagram



7.3.2 Power Management

NOTE: For information about source clock gating and for a description of the sleep/wake-up transitions, see Section 3.1.1.1, *Clock Management*, in Chapter 3, *Power, Reset, and Clock Management*.

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7.3.2.1 Local Power Management

The user can configure the local power management through the STANDBY_CORE_SYSCONFIG, IDLE_CORE_SYSCONFIG, and WUGEN_IRQ_EN registers. The user can:

- Configure the different standby modes (the default is smart wake-up standby mode) through the STANDBY_CORE_SYSCONFIG[1:0] STANDBYMODE bit field
- Configure the different idle modes (the default is smart wake-up idle mode) through the IDLE_CORE_SYSCONFIG[1:0] IDLEMODE bit field
- Control which interrupts will cause a wakeup by appropriately configuring the WUGEN_MEVT0 and WUGEN_MEVT1 registers (the default is ALL_MASKED)

The Cortex-M3 provides three sleep modes:

- On mode: Sleep on exit (wait for the interrupt service routine [ISR] to complete)
- Sleep mode: Wait for interrupt to wake up the processor
- Deep-sleep mode: Long duration sleep; phase-locked loop (PLL) can be stopped

During sleep mode, the system clock can be stopped, but the free-running clock input must still be running to allow the processor to be wakened by an interrupt or an event. The sleep modes are invoked by wait for interrupt (WFI) or wait for event (WFE) instructions. The processor clock is automatically stopped, waiting for an interrupt or an event. Deep-sleep mode also stops the processor clock, but this can also be supported by the PRCM module. A combined signal is generated from the two Cortex-M3 processors in deep-sleep mode to initiate another power state and let the PRCM module handle the next power states. At this time, software must ensure that all shared cache background operations (for example, maintenance) are complete.

Table 7-4 describes local clock gating.

Table 7-4. Local Clock Gating

Cortex-M3 CPU Mode	CPU2 On	CPU2 Sleep	CPU2 Deep Sleep
CPU1 On	On	Functional clock 2 stopped locally	Functional clock 2 stopped locally
CPU1 Sleep	Functional clock 1 stopped locally	Functional clock 1 and clock 2 stopped locally	Functional clock 1 and clock 2 stopped locally
CPU1 Deep Sleep	Functional clock 1 stopped locally	Functional clock 1 and clock 2 stopped locally	Standby request to power-management module

7.3.2.2 Power Domains

The dual Cortex-M3 MPU subsystem is divided into two power domains (CORE and WKUP), which are controlled by the PRCM module (see Section 7.3.2.3).

The CORE power domain is the main power domain and includes all the Cortex-M3 components (two ARM Cortex-M3 processors, shared cache, ROM and RAM memories, and emulation\debug modules) except the WUGEN.

The AWLON_CORE power domain is an always-on power domain. The AWLON_CORE power domain contains the WUGEN, which generates a wake-up request from external interrupts. By this separate AWLON_CORE power domain, the wake-up request can be generated even when the CORE power domain is in OFF or RET state.

For information about the CORE and ALWON_CORE power domains, see Chapter 3, *Power, Reset, and Clock Management.*

7.3.2.3 Voltage Domain

The dual Cortex-M3 MPU subsystem is composed of two voltage domains. Each voltage domain can control individual voltage levels:

- VDD1: Cortex-M3, shared cache/MMU, WUGEN
- VDD_array: All memories array

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The AWLON_CORE and CORE power domains are in the same voltage domain – the CORE voltage domain (CORE_VD).

For information about the physical power domains, see Chapter 3, *Power, Reset, and Clock Management.*

7.3.2.4 Power States and Modes

Table 7-5 lists the different power modes and the expected states for each power domain.

Table 7-5. Dual Cortex-M3 MPU Power Modes

		Activity			Power Status	
	Functional Domain	Core		Dual Cortex-M3 MPU Subsystem	CORE Power Domain	ALWON_CORE Power Domain
	Modules included	Cortex-M3 processor 1	Cortex-M3 processor 2	WUGEN		
Power modes	Active	Active	Active	Active	ON	ON
	Processor 1 idle	Idle	Active	Active	ON	ON
	Processor 2 idle	Active	Idle	Active	ON	ON
	Core standby	Idle	Idle	Active	ON	ON
	Full idle	Idle	Idle	Idle	ON	ON
	Retention	Idle	Idle	Idle	RET	ON
	Power off	Idle	Idle	Idle	OFF	OFF

Table 7-6 lists the power mode transitions in the dual Cortex-M3 MPU subsystem.

Table 7-6. Power Mode Transitions

	Active	Processor 1 Idle	Processor 2 Idle	Standby	Full-Idle	Retention	Power Off
Active		WFE/WFI instruction	WFE/WFI instruction				
Processor 1 idle	Events/ interrupts			Deep sleep			
Processor 2 idle	Events/ interrupts			Deep sleep			
Standby	Wake-up IRQ				L1/L2/ WUGEN functional domain idle		
Full idle	Wake-up IRQ			Wake-up (through interconnect)		PRCM module	PRCM module
Retention					PRCM module or wakeup		PRCM module
Power off					PRCM module or wakeup	PRCM module	

The different power modes and their features are:

- Active mode: All function domains are operable.
- Core 1 and Core 2 idle mode:
  - Only the CPU core is idled (when running WFE/WFI instructions).
  - Only one Cortex-M3 core can be in this mode. Interrupts or events can waken the core.
  - Can go into sleep or deep-sleep mode. Potentially, both cores can be in sleep mode.
  - When both cores are in deep-sleep mode, a standby request is sent to the PRCM module.
  - Software must ensure that all shared cache background operations (for example, maintenance) are complete before the PRCM module asserts an IdleReq. For more information, see Chapter 5, *DSP*, , *Direct Maintenance of Caches*.

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- Core standby mode
  - Both cores in the CORE functional domain are in idle mode (an interrupt cannot wake up either of the cores).
  - The PRCM module must have acknowledged its acceptance by an MWait signal.
  - After this handshake, all power management is under the control of the PRCM module.
- Full-idle mode:
  - The dual Cortex-M3 MPU subsystem functional domain is also idled.
  - After coming to this mode, power states can be moved deeper.
- Retention mode:
  - The voltage of the logic supply is lowered to reduce static power consumption by leakage current. The logic power switch in the CORE power domain is still closed (ON); thus, all logic states are retained.
  - L1 and/or L2 memories can go independently into retention depending on the settings done at the PRCM level.
- Power off mode:
  - The voltage source is shut down. The logic states, including the retention logic, are lost.
  - The WUGEN is not operating and only the PRCM module can trigger the Cortex-M3 wakeup.
  - Reset must be applied to the dual Cortex-M3 MPU subsystem to restart the two ARM Cortex-M3 processors and the memory subsystem.

7.3.2.5 Wake-Up Generator

The WUGEN in the dual Cortex-M3 MPU subsystem enables efficient power management. The WUGEN generates a wake-up signal to the PRCM module to enable the dual Cortex-M3 MPU subsystem to recover its functional clocks, which are gated by the PRCM module when at least one request is active. The WUGEN can be configured in standby mode or idle mode through the STANDBY_CORE_SYSCONFIG[1:0] STANDBYMODE and IDLE_CORE_SYSCONFIG[1:0] IDLEMODE bit fields.

7.3.2.5.1 WUGEN Main Features

The WUGEN allows:

- Gating of the Cortex-M3 MPU clock dynamically, thus reducing power consumption
- Simplifying of dependencies in the PRCM module

Figure 7-6 is an overview of the WUGEN.

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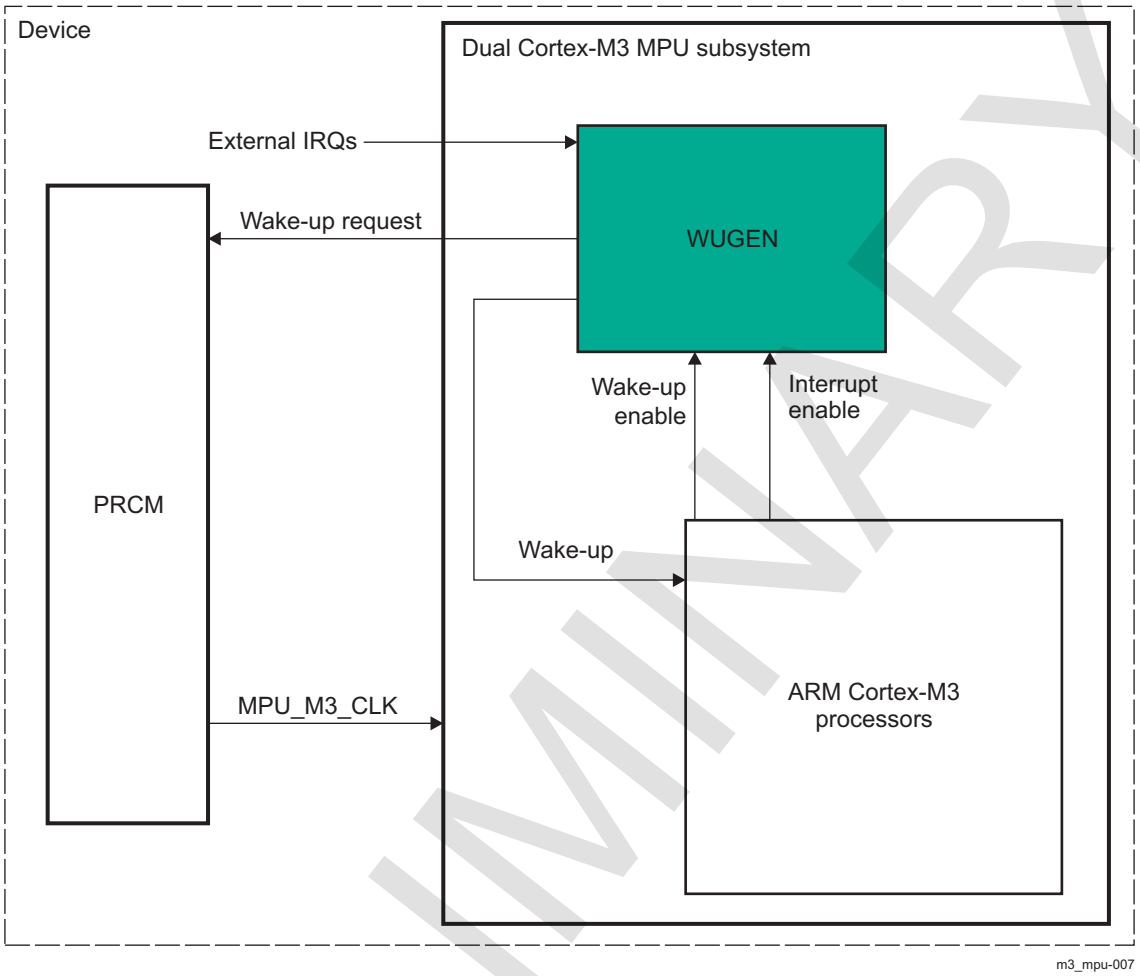
Figure 7-6. WUGEN Overview



The wake-up signal to the PRCM module requests the Cortex-M3 functional clock (MPU_M3_CLK). The wake-up signal to the ARM Cortex-M3 procesors indicates to them that at least one enabled request is active.

Two retention registers WUGEN_MEVT0 (for CPU1) and WUGEN_MEVT1 (for CPU2), enable the WUGEN requests to the NVICs.

7.3.3 Shared Cache

Table 7-7 describes the shared cache configuration in the dual Cortex-M3 MPU subsystem platform.

Table 7-7. Shared Cache Configuration

Parameter	Value
Way	4
Size	32KB
Bank elements	32 bits
Bank number	16
Slave interface data size	32 bits
Master interface data size	64 bits
Line size	256 bits
MMU lookup	Included
Number of slaves	4

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Table 7-7. Shared Cache Configuration (continued)

Parameter	Value
Number of masters	1
Number of fill/prefetch buffers	Four prefetch buffers
Slave types	Shared cache interface

Shared cache allows basic maintenance operations, which are performed through a dedicated interface:

1. Preload
2. Lock
3. Clean
4. Invalidate

Maintenance of the cache is performed between the start and end addresses. This allows for direct control of memory regions. All maintenance operations occur in the background and can generate an interrupt when they complete. Such operations are protected by software semaphore, because only one operation at a time can be performed. The maintenance operations can also be performed using MMU small entries.

The shared cache is the same as the one in the DSP subsystem. For more information about the shared cache, see Chapter 5, *DSP Subsystem*.

7.3.4 Shared Cache MMU

The MMU for the shared cache provides the multi-access cache with region-based address translation, read/write control, access type control, and multilevel cache maintenance. Table 7-8 describes the MMU configuration in the dual Cortex-M3 MPU subsystem.

Table 7-8. Shared Cache MMU Configuration

Parameter	Values
Number of large pages	Four entries
Size of large pages	512MB or 32MB (configurable)
Number of medium pages	Two entries
Size of medium pages	256KB or 128MB (configurable)
Number of small pages	10 entries
Size of small pages	16KB or 4KB (configurable)
Number of patch pages	Not included
Size of line pages	256-bit
Number of comparison interfaces	4
Number of comparator sets	1
Write pipeline data comparison	Disabled
Number of shared cache maintenance interfaces	3
Size of entry address	32-bit

The size of the pages is configurable in the shared cache MMU registers. The different MMU page sizes can be used to create smaller policies within a larger region. The shared cache MMU is the same as the one in the DSP subsystem. For more information, see Chapter 5, *DSP Subsystem*.

7.3.5 L2 MMU

An additional MMU provides address translation for the accesses done from the dual Cortex-M3 MPU subsystem to the L3 interconnect. The main characteristics of this MMU are:

- 32 entries
- Compatible with ARMv6 architecture MMU translation tables (protection bits not used)
- Page-based or access-based endianness conversion

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- Two-level descriptor hierarchy
- One intermediate page table
- Four page sizes (16MB, 1MB, 64KB, 4KB)
- Page table alignment on 128-byte boundary for ARM11® compatibility

The configuration of the MMU can be done from one of the Cortex-M3 cores or from the L3 interconnect slave port. The accesses done to configure the MMU cannot be part of a burst access.

For more information about the L2 MMU, see Chapter 20, *Memory Management Unit*.

7.3.5.1 L2 MMU Behavior on Page-Fault in Dual Cortex-M3 MPU

Table 7-9. L2 MMU Behavior on Page-Fault

Application		Debug	
Table-Walker Enabled	**Table-Walker Disabled**	**Table-Walker Enabled**	**Table-Walker Disabled**
Use Table-Walker to find translation. Update TLB cache if successful, set TRANSLATIONFAULT bit and interrupt if not. The following bits are used for the purpose: MMU_IRQENABLE[1] TRANSLATIONFAULT and MMU_IRQSTATUS[1] TRANSLATIONFAULT.	Set TLBMISS bit and interrupt and stall. The following registers are used for the purpose: MMU_IRQENABLE[0] TLBMISS and MMU_IRQSTATUS[0] TLBMISS.	Use Table-Walker to find translation. Update TLB cache if successful (only if MMU_CNTL[3] EMUTLBUPDATE is set), generate in-band bus error if not.	Set EMUMISS bit and interrupt and stall. The following bits are used for the purpose: MMU_IRQENABLE[2] EMUMISS and MMU_IRQSTATUS[2] EMUMISS.

The MMU fault interrupt line is connected to both Cortex-M3 cores and also propagated outside of Cortex-M3 and connected to the Cortex-A9 MPU (MA_IRQ_100). The Cortex-A9 MPU receives the MMU fault and must clean up the fault to resume the execution of the code (or reset Cortex-M3). It is not possible for one of the Cortex-M3 CPUs to clean up the fault caused by the other Cortex-M3 CPU. This is because both the slave port of L2 MMU (which is stalled) and the configuration port of L2 MMU is connected (through a splitter) to the same shared cache master port.

The above default behavior of the L2 MMU can be overridden by setting the MMU_GP_REG[0] BUS_ERR_BACK_EN bit to 1. Once this bit is set, all MMU faults (including TLB miss) return a bus error to the Cortex-M3 (interrupt event XLATE_MMU_FAULT). This allows the end user to quickly establish the cause of the MMU fault by having appropriate code in the ISR.

7.3.6 Interprocessor Communication (IPC)

7.3.6.1 Use of WFE and SEV

The dual Cortex-M3 MPU subsystem provides multiprocessor communication interface for synchronizing tasks. The ARM processors have one output signal, TXEV (transmit event), for sending events and one input signal, RXEV (receive event), for receiving events. Figure 7-7 shows how TXEV and RXEV are connected in the dual Cortex-M3 MPU subsystem.

When a WFE instruction is executed, the processor enters into sleep mode waiting for an event and continues instruction execution when an external event is received. With an SEV (send event) instruction, one processor can wake up the other processor, which is in sleep mode.

The WFE and SEV instructions can help reduce the number of iterations around a lock acquire loop (a spinlock), and thereby reduce power consumption. The basic mechanism involves an observer that is in a spinlock executing a WFE instruction, which suspends execution on that observer until an asynchronous exception or an explicit event (sent by an observer using the SEV instruction) is seen by that observer. The observer that holds the lock uses the SEV instruction to send an event after a lock is released.

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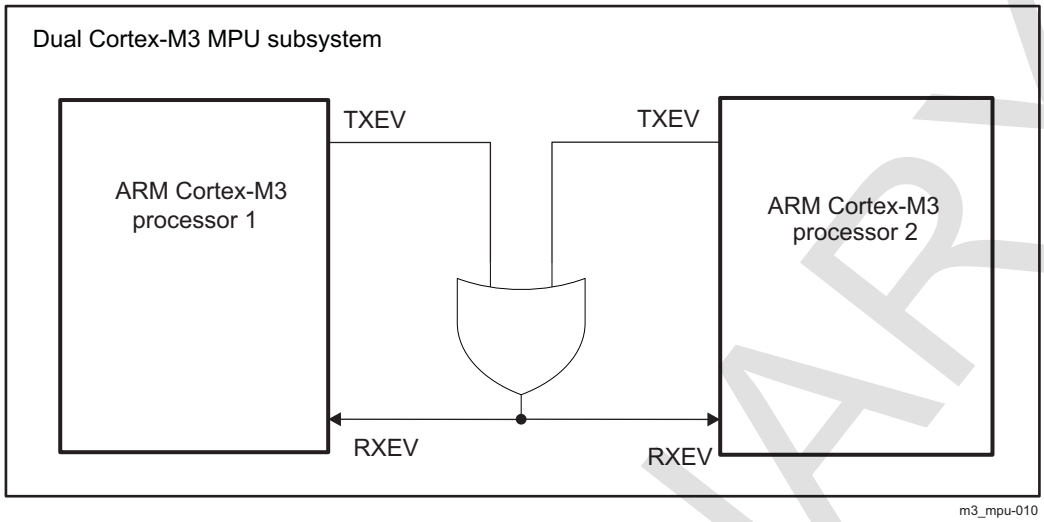
Figure 7-7. Event Communication Connection in Dual Cortex-M3 MPU Subsystem



7.3.6.2 Use of Interrupt for IPC

Each Cortex-M3 can interrupt the other Cortex-M3 by setting up an interrupt register (CORTEXM3_CTRL_REG). Because the priority level for that interrupt can be defined, it is possible to choose the task level at which the interrupt will run. For example, if CPU1 was active and CPU2 was idle (WFI state), when CPU1 completes its task it sets the bit for CPU2 in the control register (CORTEXM3_CTRL_REG[16] INT_CORTEX_2) and goes into sleep mode. CPU2 wakes up seeing this interrupt, and starts running its task. After the completion of its task, CPU2 sets the interrupt for CPU1 (CORTEXM3_CTRL_REG[0] INT_CORTEX_1), and then goes into WFI state. This kind of handshake ensures that if CPU1 and CPU2 are accessing the same resources (memory, registers etc.), only one of the CPUs at a time is active.

7.3.6.3 Use of the Bit-Band Feature for Semaphore Operations

The two Cortex-M3 cores share the same memory system, and it is possible to use the bit-band feature to carry semaphore operations. Because the bit-band alias writes are locked read-modify-write transfers, provided that all tasks changed only the lock bit representing themselves, the lock bits of other tasks are not lost, even if two tasks try to write to the same memory location at the same time.

Each Cortex-M3 core supports two bit-band regions.

Bit-band 1 applies to the virtual address space 0x2000 0000 – 0x200F FFFF (1MB). This virtual address space can be mapped to any physical address and bit-banding will apply to that region. It is recommended that the user map the L2 RAM (64KB) to this virtual space and use it only for bit-banding operations. If required, the user can define other available small and medium pages over and above the L2 RAM virtual space and further extend the use of the bit-band feature.

Bit-band 2 applies to the virtual address space 0x4000 0000 – 0x400F FFFF (1MB). The first 16KB of this space (0x4000 0000 – 0x4000 3FFF) are already reserved for small (one page) pages and cannot be remapped by software. The bit-band alias that corresponds to this 16-KB region (0x4200 0000 – 0x4207 FFFF) must also be treated as reserved and no access should be made. The rest of bit-band 2 can be used by appropriately defining the available small and medium pages. In this device, because it is likely that during normal AMMU programming all of L3 is mapped to this region, it is highly recommended that the user use only bit-band 1 for all purposes and bit-band 2 only if it is necessary.

7.3.6.4 Private Memory Space

Each ARM Cortex-M3 processor has its own memory space, unaccessible by the other processor. In the private memory space are the NVICs and RW table registers: CORTEXM3_RW_PID1 and

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CORTEXM3_RW_PID2. CORTEXM3_RW_PID1 and CORTEXM3_RW_PID2 are only accessible by the respective Cortex-M3 cores (CORTEXM3_RW_PID1 is accessible only to the video and display control ARM processor, while CORTEXM3_RW_PID2 is only accessible by the SIMCOP processor) . These registers are not accessible from the Cortex-A9 MPU. Because they are not shared, they do not require bit-band feature (semaphore) to read and write to them.

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7.4 Dual Cortex-M3 MPU Subsystem Register Manual

7.4.1 Dual Cortex-M3 Subsystem Instance Summary

Table 7-10 summarizes the dual Cortex-M3 MPU instance.

Table 7-10. Dual Cortex-M3 MPU Subsystem Instance Summary

Module Name	Base Address	Size
SCACHE_CFG	0x5508 0000	4KB
SCACHE_SCTM	0x5508 0400	4KB
SCACHE_MMU	0x5508 0800	4KB
CORTEXM3_WKUP	0x5508 1000	4KB
CORTEXM3_MMU	0x5508 2000	4KB
CM3_NVIC_CPU1(1)	0xE000 E000	4KB
CM3_NVIC_CPU2(2)	0xE000 E000	4KB
CM3_RW_Table(3)	0xE00F E000	4KB

(1) Private memory space for CPU1
(2) Private memory space for CPU2
(3) Private memory space for each CPU

7.4.2 Shared Cache Configuration Registers

For information about the shared cache configuration registers and their description, see Chapter 5, *DSP Subsystem*.

7.4.3 Shared Cache SCTM Registers

For information about the shared cache SCTM registers and their description, see Chapter 5, *DSP Subsystem*.

The SCTM registers in the Cortex-M3 MPU differ from the registers listed in Chapter 5, *DSP Subsystem*, in the following ways:

- Counters with indexes from i = 2 to 5 can be chained and shadowing is enabled.
- The reset value of the SCACHE_SCTM_CTCR_WOT_j[7] CHNSDW bit is 1.
- The option to write 1 in the SCACHE_SCTM_CTCR_WOT_j[4] CHAIN bit is not reserved and when the bit is write 1, the counter is chained.

7.4.4 Shared Cache MMU Registers

For information about the shared cache MMU registers and their description, see Chapter 5, *DSP Subsystem*.

The shared cache MMU in Cortex-M3 has four large pages, two medium pages, and ten small pages. Because of the different page sizes, there are differences with the registers described in Chapter 5, DSP Subsystem, in the enumerated indexes below the register mapping, which are the following: (i = 0 to 3), (j = 0 to 1), (k = 0 to 9). There are also differences in the reset value of the following registers:

- SCACHE_MMU_SMALL_ADDR_0 with reset value 0x00000000
- SCACHE_MMU_SMALL_ADDR_1 with reset value 0x40000000
- SCACHE_MMU_SMALL_POLICY_k with reset value 0x0000000 (k = 0 to 9)
- SCACHE_MMU_SMALL_XLTE_0 with reset value 0x55020000
- SCACHE_MMU_SMALL_XLTE_1 with reset value 0x55080000
- SCACHE_MMU_SMALL_XLTE_k with reset value 0x00000000 (k = 2 to 9)

The page sizes for the 16 entries are:

- Large pages (four): The page size supported are 32MB and 512MB.

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- Medium pages (two): The page sizes supported are 128KB and 256KB.
- Small pages (ten): The page sizes supported are 4KB and 16KB.

7.4.5 Cortex-M3 L2 MMU Registers

For information about the L2 MMU registers and their description, see Chapter 20, *Memory Management Unit*.

7.4.6 Cortex-M3 NVIC Registers

For information about the Cortex-M3 MPU NVIC registers and their description, see the ARM Cortex-M3 Technical Reference Manual .

7.4.7 Cortex-M3 Wake-Up Generator Registers

7.4.7.1 CORTEXM3_WKUP Register Summary

Table 7-11 summarizes the dual Cortex-M3 MPU register mapping.

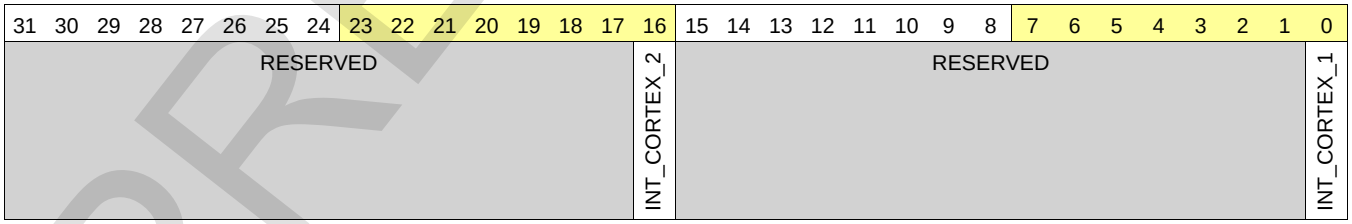
Table 7-11. CORTEXM3_WKUP Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	Cortex-M3 Base Address
CORTEXM3_CTRL_REG	RW	32	0x0000 0000	0x5508 1000
STANDBY_CORE_SYSCONFIG	RW	32	0x0000 0004	0x5508 1004
IDLE_CORE_SYSCONFIG	RW	32	0x0000 0008	0x5508 1008
WUGEN_MEVT0	RW	32	0x0000 000C	0x5508 100C
WUGEN_MEVT1	RW	32	0x0000 0010	0x5508 1010
RESERVED	R	32	0x0000 0014	0x5508 1014

7.4.7.2 Dual Cortex-M3 MPU Wake-Up Generator Register Description

Table 7-12. CORTEXM3_CTRL_REG

Address Offset	0x0000 0000		
Physical Address	0x5508 1000	**Instance**	CORTEXM3_WKUP
Description	The register is used by one CPU to interrupt the other, thus used as a handshake between the two CPUs 0x0: Interrupt is cleared; 0x1: Interrupt is set.		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:17	RESERVED		RW	0x0000 0000
16	INT_CORTEX_2	Interrupt to ARM Cortex-M3 CPU2	RW	0
15:1	RESERVED		RW	0x0000 0000
0	INT_CORTEX_1	Interrupt to ARM Cortex-M3 CPU1	RW	0

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Table 7-13. Register Call Summary for Register CORTEXM3_CTRL_REG

Dual Cortex-M3 MPU Subsystem Functional Description • Use of Interrupt for IPC: [0] [1] [2]
Dual Cortex-M3 MPU Subsystem Register Manual • CORTEXM3_WKUP Register Summary: [3]

Table 7-14. STANDBY_CORE_SYSCONFIG

Address Offset	0x0000 0004		
Physical Address	0x5508 1004	**Instance**	CORTEXM3_WKUP
Description	Standby protocol		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														STANDBYMODE	

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		RW	0x0000 0000
1:0	STANDBYMODE	0x0: Force-standby mode 0x1: No-standby mode 0x2: Smart-standby mode 0x3: Smart-standby wakeup mode - normal mode to be used	RW	0x3

Table 7-15. Register Call Summary for Register STANDBY_CORE_SYSCONFIG

Dual Cortex-M3 MPU Subsystem Functional Description • Local Power Management: [0] [1] • Wake-Up Generator: [2]
Dual Cortex-M3 MPU Subsystem Register Manual • CORTEXM3_WKUP Register Summary: [3]

Table 7-16. IDLE_CORE_SYSCONFIG

Address Offset	0x0000 0008		
Physical Address	0x5508 1008	**Instance**	CORTEXM3_WKUP
Description	Idle protocol		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														IDLEMODE	

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Bits	Field Name	Description	Type	Reset
31:2	RESERVED		RW	0x0000 0000
1:0	IDLEMODE	0x0: Force-idle mode 0x1: No-idle mode 0x2: Smart-idle mode 0x3: Smart-idle wakeup mode - normal mode to be used	RW	0x3

Table 7-17. Register Call Summary for Register IDLE_CORE_SYSCONFIG

Dual Cortex-M3 MPU Subsystem Functional Description
- Local Power Management: [0] [1]
- Wake-Up Generator: [2]

Dual Cortex-M3 MPU Subsystem Register Manual
- CORTEXM3_WKUP Register Summary: [3]

Table 7-18. WUGEN_MEVT0

Address Offset	0x0000 000C		
Physical Address	0x5508 100C	**Instance**	CORTEXM3_WKUP
Description	This register contains the interrupt mask (LSB) wake-up enable bit per interrupt request 0x0: Interrupt is disabled; 0x1: Interrupt is enabled.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MIRQ31	RESERVED	MIRQ29	MIRQ28	MIRQ27	MIRQ26	MIRQ25	MIRQ24	MIRQ23	MIRQ22	MIRQ21	MIRQ20	MIRQ19	MIRQ18	MIRQ17	MIRQ16	MIRQ15	MIRQ14	MIRQ13	MIRQ12	MIRQ11	MIRQ10	MIRQ9	MIRQ8	MIRQ7	RESERVED							

Bits	Field Name	Description	Type	Reset
31	MIRQ31	Interrupt Mask bit 31	RW	0
30	RESERVED	Reserved	R	0
29	MIRQ29	Interrupt Mask bit 29	RW	0
28	MIRQ28	Interrupt Mask bit 28	RW	0
27	MIRQ27	Interrupt Mask bit 27	RW	0
26	MIRQ26	Interrupt Mask bit 26	RW	0
25	MIRQ25	Interrupt Mask bit 25	RW	0
24	MIRQ24	Interrupt Mask bit 24	RW	0
23	MIRQ23	Interrupt Mask bit 23	RW	0
22	MIRQ22	Interrupt Mask bit 22	RW	0
21	MIRQ21	Interrupt Mask bit 21	RW	0
20	MIRQ20	Interrupt Mask bit 20	RW	0
19	MIRQ19	Interrupt Mask bit 19	RW	0
18	MIRQ18	Interrupt Mask bit 18	RW	0
17	MIRQ17	Interrupt Mask bit 17	RW	0
16	MIRQ16	Interrupt Mask bit 16	RW	0
15	MIRQ15	Interrupt Mask bit 15	RW	0
14	MIRQ14	Interrupt Mask bit 14	RW	0
13	MIRQ13	Interrupt Mask bit 13	RW	0
12	MIRQ12	Interrupt Mask bit 12	RW	0
11	MIRQ11	Interrupt Mask bit 11	RW	0
10	MIRQ10	Interrupt Mask bit 10	RW	0

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Bits	Field Name	Description	Type	Reset
9	MIRQ9	Interrupt Mask bit 9	RW	0
8	MIRQ8	Interrupt Mask bit 8	RW	0
7	MIRQ7	Interrupt Mask bit 7	RW	0
6:0	RESERVED	Reserved	R	0

Table 7-19. Register Call Summary for Register WUGEN_MEVT0

Dual Cortex-M3 MPU Subsystem Functional Description

- Local Power Management: [0]
- WUGEN Main Features: [1]

Dual Cortex-M3 MPU Subsystem Register Manual

- CORTEXM3_WKUP Register Summary: [2]

Table 7-20. WUGEN_MEVT1

Address Offset	0x0000 0010		
Physical Address	0x5508 1010	**Instance**	CORTEXM3_WKUP
Description	This register contains the interrupt mask (MSB) wake-up enable bit per interrupt request 0x0: Interrupt is disabled; 0x1: Interrupt is enabled.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MIRQ63	MIRQ62	MIRQ61	MIRQ60	MIRQ59	MIRQ58	MIRQ57	MIRQ56	RESERVED	MIRQ54	MIRQ53	MIRQ52	MIRQ51	MIRQ50	RESERVED	MIRQ48	MIRQ47	MIRQ46	RESERVED			MIRQ42	MIRQ41	MIRQ40	MIRQ39	MIRQ38	MIRQ37	MIRQ36	MIRQ35	MIRQ34	MIRQ33	RESERVED

Bits	Field Name	Description	Type	Reset
31	MIRQ63	Interrupt Mask bit 63	RW	0
30	MIRQ62	Interrupt Mask bit 62	RW	0
29	MIRQ61	Interrupt Mask bit 61	RW	0
28	MIRQ60	Interrupt Mask bit 60	RW	0
27	MIRQ59	Interrupt Mask bit 59	RW	0
26	MIRQ58	Interrupt Mask bit 58	RW	0
25	MIRQ57	Interrupt Mask bit 57	RW	0
24	MIRQ56	Interrupt Mask bit 56	RW	0
23	RESERVED	Reserved	R	0
22	MIRQ54	Interrupt Mask bit 54	RW	0
21	MIRQ53	Interrupt Mask bit 53	RW	0
20	MIRQ52	Interrupt Mask bit 52	RW	0
19	MIRQ51	Interrupt Mask bit 51	RW	0
18	MIRQ50	Interrupt Mask bit 50	RW	0
17	RESERVED	Reserved	R	0
16	MIRQ48	Interrupt Mask bit 48	RW	0
15	MIRQ47	Interrupt Mask bit 47	RW	0
14	MIRQ46	Interrupt Mask bit 46	RW	0
13:11	RESERVED	Reserved	R	0
10	MIRQ42	Interrupt Mask bit 42	RW	0
9	MIRQ41	Interrupt Mask bit 41	RW	0
8	MIRQ40	Interrupt Mask bit 40	RW	0
7	MIRQ39	Interrupt Mask bit 39	RW	0

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Bits	Field Name	Description	Type	Reset
6	MIRQ38	Interrupt Mask bit 38	RW	0
5	MIRQ37	Interrupt Mask bit 37	RW	0
4	MIRQ36	Interrupt Mask bit 36	RW	0
3	MIRQ35	Interrupt Mask bit 35	RW	0
2	MIRQ34	Interrupt Mask bit 34	RW	0
1	MIRQ33	Interrupt Mask bit 33	RW	0
0	RESERVED	Reserved	R	0

Table 7-21. Register Call Summary for Register WUGEN_MEVT1

Dual Cortex-M3 MPU Subsystem Functional Description • Local Power Management: [0] • WUGEN Main Features: [1]
Dual Cortex-M3 MPU Subsystem Register Manual • CORTEXM3_WKUP Register Summary: [2]

7.4.8 Cortex-M3 RW Table Registers

7.4.8.1 CM3_RW_Table Register Summary

Table 7-22. CM3_RW_Table Register Summary

Register Name	Type	Register Width (Bits)	Address Offset	Cortex-M3 Base Address
CORTEXM3_RW_PID1	RW	32	0x0000 0000	0xE00F E000
CORTEXM3_RW_PID2	RW	32	0x0000 0004	0xE00F E004
RESERVED	R	32	0x0000 0008	0xE00F E008

7.4.8.2 Cortex-M3 RW Table Register Description

Table 7-23. CORTEXM3_RW_PID1

Address Offset	0x0000 0000		
Physical Address	0xE00F E000	**Instance**	CM3_RW_Table
Description	Peripheral Identification register - allows the user software to differentiate between the two ARM Cortex-M3 processors (two CPUs). The same piece of code running on the two CPUs can result in different execution (in example branch to different location) depending on what address is stored in the register. The address is stored by the BIOS code. The register cannot be accessed when the BIOS code is running (used).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BASEADD1																															

Bits	Field Name	Description	Type	Reset
31:0	BASEADD1	ROM memory address	RW	0x0000 0000

Table 7-24. Register Call Summary for Register CORTEXM3_RW_PID1

Dual Cortex-M3 MPU Subsystem Functional Description • Private Memory Space: [0] [1] [2]
Dual Cortex-M3 MPU Subsystem Register Manual • CM3_RW_Table Register Summary: [3]

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Table 7-25. CORTEXM3_RW_PID2

Address Offset	0x0000 0004		
Physical Address	0xE00F E004	**Instance**	CM3_RW_Table
Description	Peripheral Identification register - allows the user software to differentiate between the two ARM Cortex-M3 processors (two CPUs). The same piece of code running on the two CPUs can result in different execution (in example branch to different location) depending on what address is stored in the register. The address is stored by the BIOS code. The register cannot be accessed when the BIOS code is running (used).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BASEADD2																															

Bits	Field Name	Description	Type	Reset
31:0	BASEADD2	ROM memory address	RW	0x0000 0000

Table 7-26. Register Call Summary for Register CORTEXM3_RW_PID2

Dual Cortex-M3 MPU Subsystem Functional Description • Private Memory Space: [0] [1] [2]
Dual Cortex-M3 MPU Subsystem Register Manual • CM3_RW_Table Register Summary: [3]

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Imaging Subsystem

This chapter gives a top-level overview of the imaging subsystem (ISS) in the device.

Topic **Page**

8.1 ISS Overview **1178**
8.2 ISS Interfaces **1216**
8.3 ISS ISP **1488**
8.4 ISS Still Image Coprocessor **1943**

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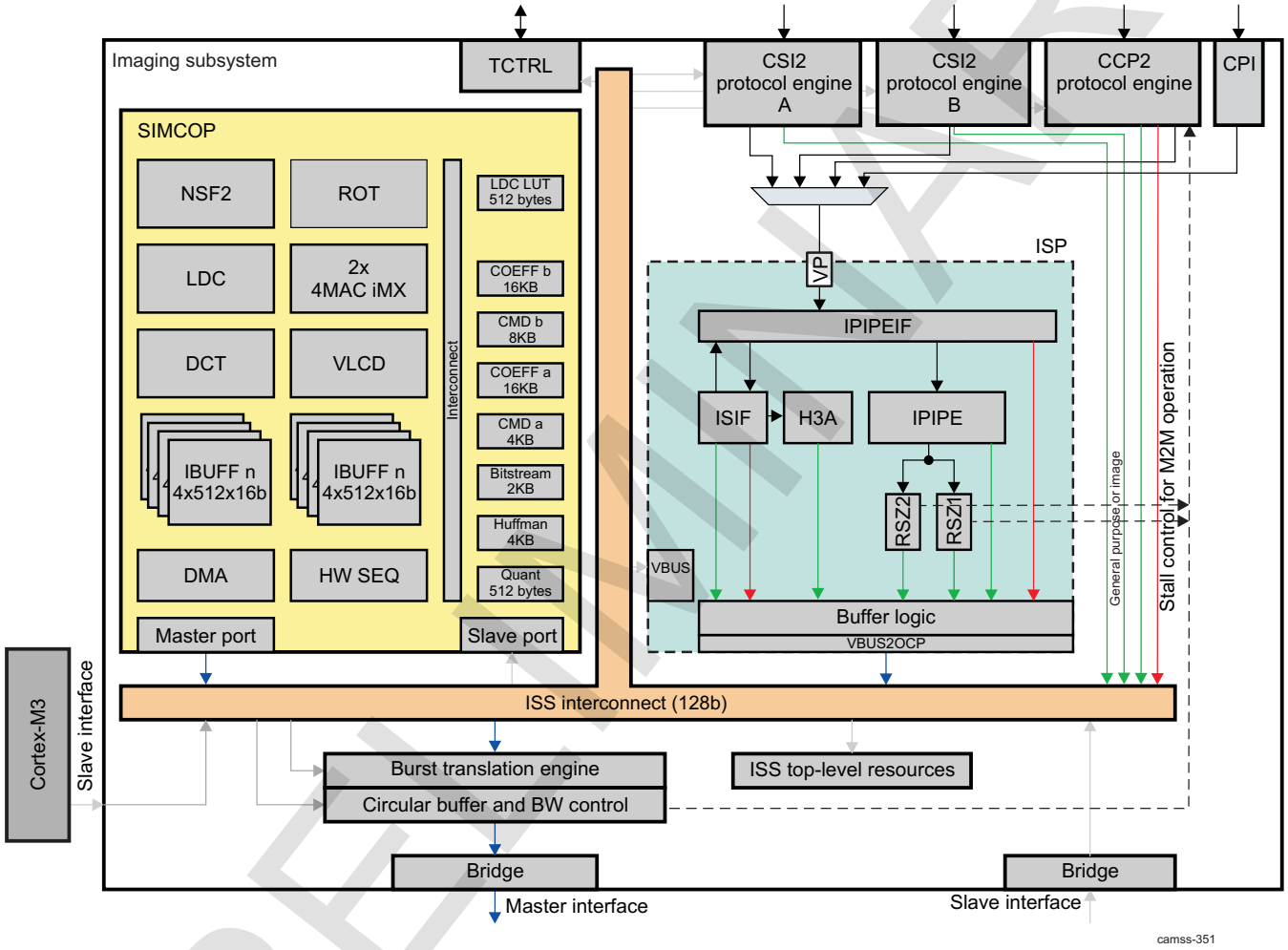
8.1 ISS Overview

The imaging subsystem (ISS) deals with the processing of the pixel data coming from an external image sensor, data from memory (image format encoding and decoding can be done to and from memory), or data from SL2 in IVA-HD for hardware encoding. With its subparts, such as interfaces and interconnects, image signal processor (ISP), and still image coprocessor (SIMCOP), the ISS is a key component for the following multimedia applications: camera viewfinder, video record, and still image capture. Figure 8-1 shows an overview of the ISS.

Figure 8-1. ISS Overview



The direction of the arrows shows the command flow direction from the master (initiator) to the slave (target). The following color conventions are used for the connections:

- Blue: Bidirectional, 128-bit-wide interface data connection
- Green: Write (ISS → system memory) data connection. Either 64-bit interface, 128-bit interface, or 32-bit MTC (inside ISP5).
- Red: Read (system memory to ISS) data connection. 128-bit interface port or 32-bit MTC (inside ISP5).
- Gray: 32-bit interface configuration connection
- Solid black: Video port and camera interface related signals
- Dotted black: Data flow stall control signal. Used to slow down ISP for memory-to-memory operation.

The ISS is mainly composed of CCP2 and CSI2-A, CSI2-B camera interfaces, a parallel interface (CPI), an ISP, and a block-based imaging accelerator (SIMCOP).

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The ISS is designed to reach high throughput and low latency with large image sensors. In high-performance mode, the ISS supports a pixel throughput of 200 MPix/s.

Two programmable image processors (iMX4) are included in the SIMCOP subsystem to add further flexibility to implement new algorithms or where new issues are encountered with the image sensors. The iMX4 processors are also open to third-party algorithms.

The ISS is tightly coupled with a low-interrupt latency microprocessor unit (MPU) subsystem (Cortex™-M3 MPU) that runs a real-time operating system (OS) to reach optimal performance. Mainly, the Cortex-M3 MPU can quickly change the ISS configuration during frame blanking periods and run some sequencing tasks.

The ISS targets the following major use cases:

- Viewfinder with digital zoom, video stabilization, and rotations
- Up to 1080p video record at 30 fps with digital zoom, video stabilization, and rotation
- Up to 16 MPix still image capture with digital zoom and rotation
  - High performance mode: Up to 200 MPix/s throughput
  - High quality and low light modes: Up to 50 MPix/s throughput
- Still image capture during video record

NOTE: The ISS is not limited to 16 Mpix. Higher resolution can be achieved through multiple passes.

NOTE: For a detailed list of features of a certain submodule, see the related subsection.

The ISS offers the following features:

- SIMCOP:
  - Memory-to-memory operation
  - JPEG encode and decode hardware acceleration
  - High-ISO noise filtering (NSF 2.0) with up to 120 MPix/s throughput
  - Rotation accelerator
  - Warping accelerator
  - Lens distortion correction (YUV space) with up to 200 MPix/s throughput
  - General-purpose (GP) imaging accelerator (2x iMX4) with up to 400-MHz clock speed
  - Direct memory access (DMA) controller
  - Hardware sequencer
- ISP:
  - On-the-fly or memory-to-memory processing
  - Up to 200-MHz pixel throughput
  - Statistic data collection
  - Image pipe interface front-end raw data processing
  - RGB and YUV data processing through ISIF and IPIPE
  - Hardware 3A (H3A) statistics block for real-time auto focus (AF), auto exposure (AE), and auto white balance (AWB)
  - Two image continuous real-time resizers
  - Video port (VP) for interfacing with the receivers and directing data to the ISP
- ISS interfaces:
  - 128-bit-wide data interface to the level 3 (L3) interconnect
  - Burst translation engine (BTE) tightly coupled with the TILER to support efficient rotation
  - Circular buffer for linear space, physically located in memory

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- The ISS relies on the centralized memory management unit (MMU). See Chapter 20, *Memory Management Unit*.
- Two CSI2 camera interfaces: CSI2-A (primary) and CSI2-B (secondary)
- CCP2 camera interface (secondary). Compatible with the *SMIA CCP2 Specification v1.0* and the *MIPI CSI1 Specification*.
- Parallel interface (CPI) (16 bit wide, with up to 148.5 MPix/s throughput, and supporting BT656, SYNC modes)
- System memory data read-back port (supported by the CCP2 protocol engine module)

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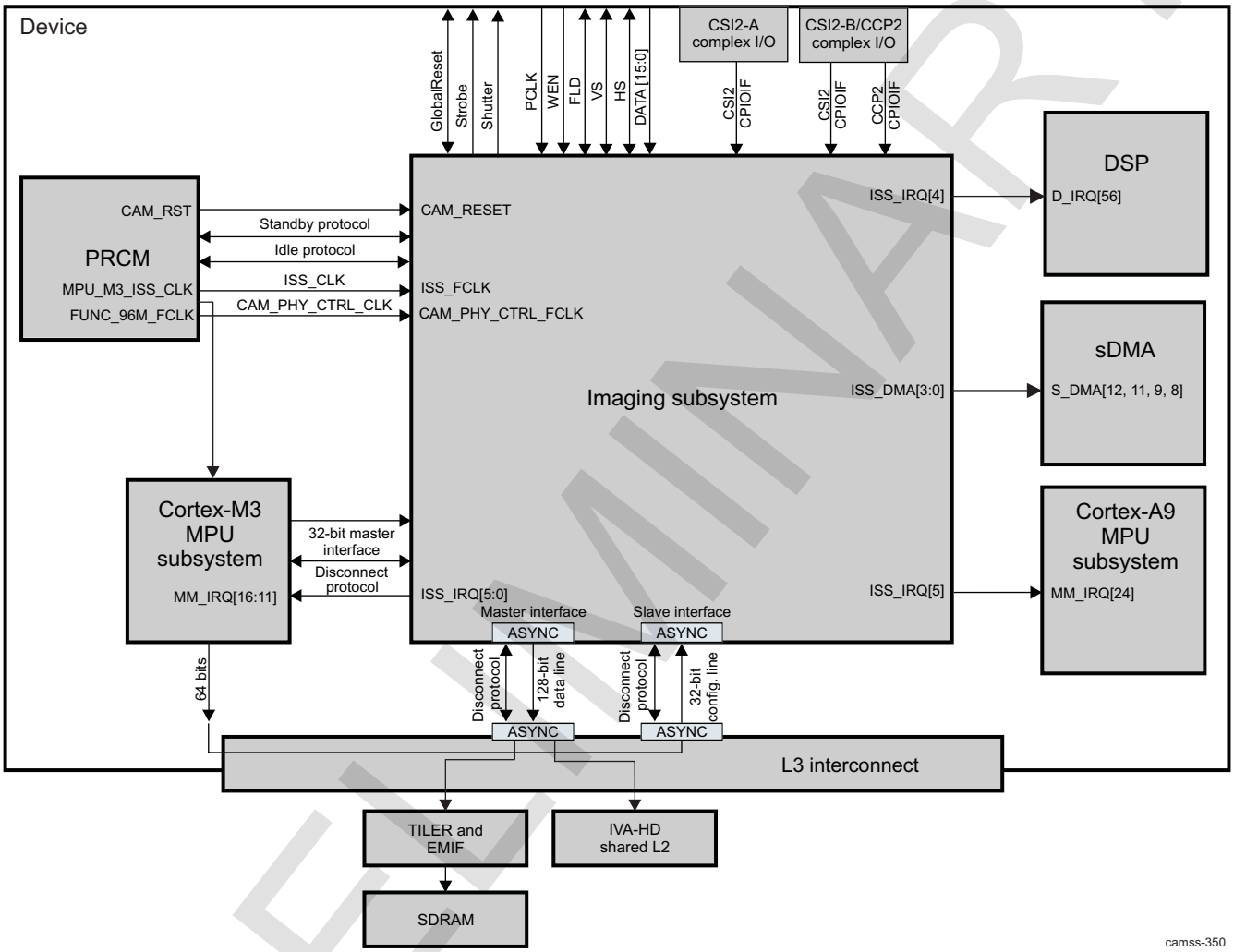
8.1.1 ISS Integration

This section describes the integration of the module in the device, including information about clocks, resets, and hardware requests.

Figure 8-2 shows the ISS integration.

Figure 8-2. ISS Integration



NOTE: For more information about the IDLE hardware handshake and wake-up request, see Section 3.1.1.1, *Clock Management*, in Chapter 3, *Power, Reset, and Clock Management*.

This section gives an overview of typical uses of the module. For more information about the relationship of the power, reset, and clock management (PRCM) module to the ISS clocks and the reset settings, see the detailed functional description in Chapter 3, *Power, Reset, and Clock Management*.

The ISS is part of ISS hardware and power management, which comprises the Cortex-M3 MPU, ISS, and a clock generator. These are all independent power domains. The ISS is part of the CAM power domain.

The PRCM module provides a single clock (MPU_M3_ISS_CLK) to ISS power management. This clock generates the clocks for the Cortex-M3 MPU, ISS, and the bridges to L3.

The ISS also supports software reset. A software reset has the same function as a hardware reset except that it does not reset the power-management protocols.

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When enabled, MPU_M3_ISS_CLK is gated to provide ISS_CLK, which, after entering the ISS boundary, is named ISS_FCLK. MPU_M3_ISS_CLK is provided as long as the Cortex-M3 MPU or ISS modules within the ISS require it.

CAM_PHY_CTRL_CLK is gated from FUNC_96M_FCLK, which comes from the PRCM module. When enabled and inside the ISS boundary, it is called CAM_PHY_CTRL_FCLK.

NOTE: For more information about the device clocks and how they are handled by the PRCM module before going into the ISS, see, *CM2 Clock Generator*, in Chapter 3, *Power, Reset, and Clock Management.*

Table 8-1 through Table 8-3 summarize the integration of the module in the device.

Table 8-1. ISS Integration Attributes

Module Instance	Attributes		
	Power Domain	Wake-Up Capability	Interconnect
ISS	PD_CAM	No	

Table 8-2. ISS Clocks and Resets

Clocks				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
ISS	ISS_FLCK	ISS_CLK	PRCM	ISS global functional clock from the PRCM module
	CAM_PHY_CTRL_FCLK	CAM_PHY_CTRL_CLK	PRCM	Physical layer functional clock from the PRCM module
Resets				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
ISS	CAM_RESET	CAM_RST	PRCM	ISS global reset

Table 8-3. ISS Hardware Requests

Interrupt Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
ISS	ISS_IRQ4	D_IRQ_56	DSP INTC	Interrupt generated by ISS to DSP
	ISS_IRQ5	MM_IRQ_24	Cortex-A9 INTC	Interrupt generated by ISS to Cortex-M9
	ISS_IRQ0	MM_IRQ_11	Cortex-M3 INTC	Interrupt generated by ISS to Cortex-M3
	ISS_IRQ1	MM_IRQ_12	Cortex-M3 INTC	Interrupt generated by ISS to Cortex-M3
	ISS_IRQ2	MM_IRQ_13	Cortex-M3 INTC	Interrupt generated by ISS to Cortex-M3
	ISS_IRQ3	MM_IRQ_14	Cortex-M3 INTC	Interrupt generated by ISS to Cortex-M3
	ISS_IRQ4	MM_IRQ_15	Cortex-M3 INTC	Interrupt generated by ISS to Cortex-M3
	ISS_IRQ5	MM_IRQ_16	Cortex-M3 INTC	Interrupt generated by ISS to Cortex-M3
DMA Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
ISS	ISS_DMA0	S_DMA_8	sDMA	Signal connected to the sDMA directly provided by ISP.
	ISS_DMA1	S_DMA_9	sDMA	Signal connected to the sDMA directly provided by ISP
	ISS_DMA2	S_DMA_11	sDMA	Signal connected to the sDMA directly provided by ISP
	ISS_DMA3	S_DMA_12	sDMA	Signal connected to the sDMA directly provided by ISP

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8.1.1.1 ISS PRCM Interface Integration

8.1.1.1.1 ISS Clock Domains

The ISS has five asynchronous clock domains. Most of the logic uses ISS_FCLK; the other clock domains are used for interfaces.

Table 8-4 provides a high-level view of clocks. The frequencies provided are maximum values.

Table 8-4. ISS Local Clock Domains

Name	Description
PCLK	Parallel interface (CPI) pixel clock provided by the camera external sensor. The CSI2-A, CSI2-B, and CCP2 modules also have video port outputs, each having its own pixel clock. These pixel clocks are generated from the functional clock (ISS_FCLK). Then all four pixel clock sources are multiplexed into one clock provided to the ISP.
CSI2_A_BC	Byte clock provided by the CSI2-A complex I/O. Used by the CSI2-A receiver.
CSI2_B_BC	Byte clock provided by the CSI2-B/CCP2 complex I/O. Used by the CSI2-B receiver.
CCP2_BC	Clock provided by the CCP2 complex I/O. Used by the CCP2 protocol engine.
ISS_FCLK	Functional clock provided by ISS_CLK from the PRCM module. It is used by all ISS submodules and ISS top-level resources.
CAM_PHY_CTRL_FCLK	Functional clock provided by the PRCM module. It is used by the CSI2-A and CSI2-B/CCP2 complex I/Os.

To save power, the ISS can divide the received functional clock (ISS_CLK) by 2 or 4 from ISS_CTRL[4:5] ISS_CLK_DIV. The configuration clock is always half the functional clock.

The functional clock of some submodules can be cut by software to reduce power consumption by cutting off or turning on the modules from the ISS_CLKCTRL register. Also, the pixel clocks sent by submodules to ISP can be cut off from ISS_CLKCTRL VPORT*x*_CLK.

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8.1.2 ISS Functional Description

This section provides only a top-level overview of the ISS. The ISS submodules are described in: Section 8.4, *ISS:SIMCOP*, Section 8.2, *ISS:interfaces*, and Section 8.3, *ISS:ISP*.

Section 8.1.2.1, *ISS Interrupts*, describes the ISS power-management mechanisms and gives an introduction to and a functional description of the ISP submodules.

8.1.2.1 ISS Interrupts

Table 8-5 lists the events generated by the submodules and the top level of the ISS.

Each event that generates an interrupt can be individually enabled by setting the appropriate bit in the ISS_HL_IRQENABLE_SET_i register. The interrupt is disabled by setting the appropriate bit in the ISS_HL_IRQENABLE_CLR_i register.

When an event occurs, the corresponding bit in the ISS_HL_IRQSTATUS_RAW_i register is set regardless of whether or not the event is enabled. Bits in the ISS_HL_IRQSTATUS_i registers are set only when an enabled event occurs.

Software can clear a pending HS_VS_IRQ event by setting the ISS_HL_IRQSTATUS_i[17] HS_VS_IRQ bit. Events generated by submodules are automatically cleared at the ISS level when they are cleared at the submodule level.

8.1.2.1.1 ISS Interrupt Merger

The ISS merges the following eight interrupt sources into six physical interrupt lines. All six lines support level and pulse modes.

Table 8-5. ISS Interrupts

Interrupt	Source	Description
ISP_IRQ[3:0]	ISP	Interrupt generated by the ISP (1)
CSIA_IRQ	CSI2-A	Interrupt generated by the CSI2-A receiver(1)
CSIB_IRQ	CSI2-B	Interrupt generated by the CSI2-B receiver (1)
CCP2_IRQ[3:0]	CCP2	Interrupt generated by the CCP2 receiver(1)
CCP2_IRQ[8]	CCP2	Interrupt generated by the CCP2 receiver(1)
CBUFF_IRQ	CBUFF	Interrupt generated by the circular buffer(1)
BTE_IRQ	BTE	Interrupt generated by the BTE (1)
SIMCOP_IRQ[3:0]	SIMCOP	Interrupt generated by SIMCOP
HS_VS_IRQ	ISS	HS or VS synchronization event. This event is triggered if a rising or falling edge is detected on the HS or VS signal. The rising or falling edge and the HS or VS signal selection are chosen using the ISP_CTRL[0:1] SYNC_DETECT bit field.

(1) For more information, see Section 8.1.2.1.2, *ISS Submodule Interrupts*.

Software can select which interrupt sources are routed to each output line (ISS_IRQ[0:5]). All six physical interrupt outputs have equivalent functions. Software can use different interrupt lines to group events together by type and therefore reduce interrupt latencies. Typically, one interrupt line is used for low-priority events (errors), and the other interrupt lines are used for high-priority events (for example, SIMCOP sequencing and end-of-frame events to trigger configuration load). The ISS internal interrupt request (IRQ) merger (see Figure 8-3) relies only on level interrupts provided by submodules. Pulse interrupts provided by submodules are ignored. Typically, all of the interrupts are routed to the Cortex-M3 running the camera driver. In addition, one interrupt is routed to Cortex-A9, which may run the imaging software. Software does not need to clear events from submodules at the ISS level: it clears only the events at the submodule level; the IRQ merger automatically clears the IRQ at this level.

NOTE: Only the HS_VS_IRQ top-level event is cleared at the ISS level.

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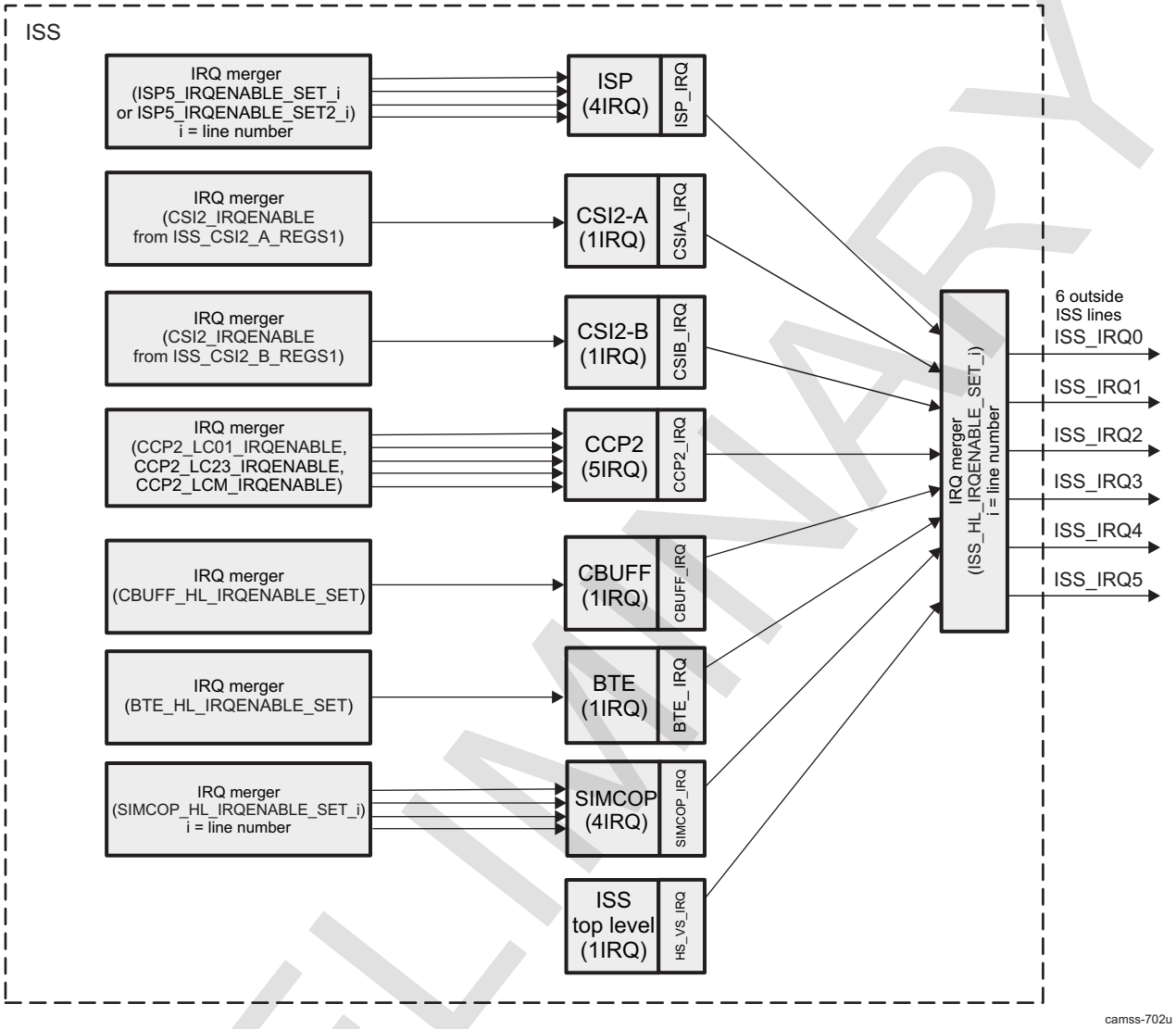
Figure 8-3. ISS Interrupt Merger



NOTE: For more information about mapping the six lines to the outside ISS device modules, see Table 8-3.

Only the ISP, SIMCOP, and HL ISS merger IRQ lines are configurable. Each interrupt can be mapped to the required line. This is not the case with CCP2 where, for example, LC01 is hardwired to line0 and line1.

8.1.2.1.2 ISS Submodule Interrupts

The ISS shown in Figure 8-3 and listed in Table 8-3 can generate six interrupts.

8.1.2.1.2.1 ISS ISP Interrupts

Table 8-6 summarizes events that cause ISP interrupts.

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Table 8-6. ISS ISP Interrupts

Event and Register [(1)]	Description
ISP5_IRQENABLE_SET_i[[31] OCP_ERR_IRQ	An interface port error has been received on the ISP master port.
ISP5_IRQENABLE_SET_i[29] IPIPE_INT_DPC_RNEW1	HD interrupt signal to indicate the need to renew the defect pixel correction (DPC) table with new entries. The second 128 entries in the DPC table must be updated when this event triggers. This event is triggered when the 255th entry in the look-up table (LUT) is used. This interrupt is not synchronous to the HD signal.
ISP5_IRQENABLE_SET_i[28] IPIPE_INT_DPC_RNEW0	VD interrupt signal to indicate the need to renew the DPC table with new entries. The first 128 entries in the DPC table must be updated when the event triggers. This event is triggered when the 127th entry in the LUT is used. This interrupt is not synchronous to the HD signal.
ISP5_IRQENABLE_SET_i[27] IPIPE_INT_DPC_INI	Interrupt to signal the need to initialize the DPC table. The DPC table contains two tables of 128 entries. When this signal is used, software must ensure that the 256 table entries are updated with the DPC information.
ISP5_IRQENABLE_SET_i[25] IPIPE_INT_EOF	End of frame interrupt signal
ISP5_IRQENABLE_SET_i[24] H3A_INT_EOF	End of frame interrupt signal
ISP5_IRQENABLE_SET_i[22] RSZ_INT_EOF1	See Section 8.1.3, *ISS Register Manual*, and Section 8.3.5, *ISS ISP Register Manual*.
ISP5_IRQENABLE_SET_i[23] RSZ_INT_EOF0	See Section 8.1.3, *ISS Register Manual*, and Section 8.3.5, *ISS ISP Register Manual*.
ISP5_IRQENABLE_SET_i[19] RSZ_FIFO_IN_BLK_ERR	See Section 8.1.3, *ISS Register Manual*, and Section 8.3.5, *ISS ISP Register Manual*.
ISP5_IRQENABLE_SET_i[18] RSZ_FIFO_IN_OVF	See Section 8.1.3, *ISS Register Manual*, and Section 8.3.5, *ISS ISP Register Manual*.
ISP5_IRQENABLE_SET_i[17] RSZ_INT_CYC_RZB	See Section 8.1.3, *ISS Register Manual*, and Section 8.3.5, *ISS ISP Register Manual*.
ISP5_IRQENABLE_SET_i[16] RSZ_INT_CYC_RZA	See Section 8.1.3, *ISS Register Manual*, and Section 8.3.5, *ISS ISP Register Manual*.
ISP5_IRQENABLE_SET_i[15] RSZ_INT_DMA	See Section 8.1.3, *ISS Register Manual*, and Section 8.3.5, *ISS ISP Register Manual*.
ISP5_IRQENABLE_SET_i[14] RSZ_INT_LAST_PIX	See Section 8.1.3, *ISS Register Manual*, and Section 8.3.5, *ISS ISP Register Manual*.
ISP5_IRQENABLE_SET_i[13] RSZ_INT_REG	See Section 8.1.3, *ISS Register Manual*, and Section 8.3.5, *ISS ISP Register Manual*.
ISP5_IRQENABLE_SET_i[12] H3A_INT	Interrupt generated by the AF and AE/AWB blocks inside the H3A module. It indicates the end of processing a frame and is active high for one configuration bus clock cycle.
ISP5_IRQENABLE_SET_i[11] AF_INT	AF inside generates an interrupt at the end of processing frame; a third interrupt is generated at the same time as the last process to finish.
ISP5_IRQENABLE_SET_i[10] AEW_INT	AEW inside generates an interrupt at the end of processing frame; a third interrupt is generated at the same time as the last process to finish.
ISP5_IRQENABLE_SET_i[9] IPIPEIF_IRQ	IPIPEIF module interrupt is generated at the start position of a frame and is active high for one configuration bus clock cycle.
ISP5_IRQENABLE_SET_i[8] IPIPE_INT_HST	IPIPE module interrupt is generated when histogram is done.
ISP5_IRQENABLE_SET_i[7] IPIPE_INT_BSC	IPIPE module interrupt is generated when boundary signal calculation is done.
ISP5_IRQENABLE_SET_i[6] IPIPE_INT_DMA	IPIPE module interrupt is issued when the SDRAM transfer of boxcar is done. At this time, IPIPE EOF is sent to buffer logic.
ISP5_IRQENABLE_SET_i[5] IPIPE_INT_LAST_PIX	IPIPE module interrupt is issued when the last pixel of a frame comes into IPIPE.
ISP5_IRQENABLE_SET_i[4] IPIPE_INT_REG	IPIPE module interrupt is issued when the register update of the module is allowed.
ISP5_IRQENABLE_SET_i[3] ISIF_INT_3	See Section 8.1.3, *ISS Register Manual*, and Section 8.3.5, *ISS ISP Register Manual*.
ISP5_IRQENABLE_SET_i[2] ISIF_INT_2	See Section 8.1.3, *ISS Register Manual*, and Section 8.3.5, *ISS ISP Register Manual*.

(1) i = 0 to 3

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Table 8-6. ISS ISP Interrupts (continued)

Event and Register [(1)]	Description
ISP5_IRQENABLE_SET_i[1] ISIF_INT_1	See Section 8.1.3, *ISS Register Manual*, and Section 8.3.5, *ISS ISP Register Manual*.
ISP5_IRQENABLE_SET_i[0] ISIF_INT_0	See Section 8.1.3, *ISS Register Manual*, and Section 8.3.5, *ISS ISP Register Manual*.
ISP5_IRQENABLE_SET2_i[0] H3A_OVF	See Section 8.1.3, *ISS Register Manual*, and Section 8.3.5, *ISS ISP Register Manual*.
ISP5_IRQENABLE_SET2_i[1] IPIPEIF_UDF	See Section 8.1.3, *ISS Register Manual*, and Section 8.3.5, *ISS ISP Register Manual*.
ISP5_IRQENABLE_SET2_i[2] IPIPE_BOXCAR_OVF	See Section 8.1.3, *ISS Register Manual*, and Section 8.3.5, *ISS ISP Register Manual*.
ISP5_IRQENABLE_SET2_i[3] ISIF_OVF	See Section 8.1.3, *ISS Register Manual*, and Section 8.3.5, *ISS ISP Register Manual*.
ISP5_IRQENABLE_SET2_i[4] IPIPE_HST_ERR	See Section 8.1.3, *ISS Register Manual*, and Section 8.3.5, *ISS ISP Register Manual*.

8.1.2.1.2.2 ISS CSI2-A and CSI2-B Complex I/O Interrupts

Table 8-7 lists the event generation of the CSI2-A and CSI2-B receivers through the CSI2 interrupt status and interrupt enable registers. The events are checked for status using the CSI2_IRQSTATUS and CSI2_IRQENABLE registers.

Table 8-7. ISS CSI2-A and CSI2-B Interrupts

Event and Register	Description
CSI2_IRQENABLE[14] OCP_ERR_IRQ	Interface port error
CSI2_IRQENABLE[13] SHORT_PACKET_IRQ	Short packet reception (other than sync events: line start, line end, frame start, and frame end; only data types from 0x8 to 0xF are considered)
CSI2_IRQENABLE[12] ECC_CORRECTION_IRQ	ECC was used to correct a 1-bit error (short packet only).
CSI2_IRQENABLE[11] ECC_NO_CORRECTION_IRQ	ECC was not used to correct the header because the error is larger than 1 bit (short and long packets).
CSI2_IRQENABLE[9] COMPLEXIO_ERR_IRQ	Error signaling from complex I/O: This interrupt is triggered when any error is received from the complex I/O (events are defined in CSI2_COMPLEXIO_IRQSTATUS [see Table 8-8]).
CSI2_IRQENABLE[8] FIFO_OVF_IRQ	FIFO overflow error: This interrupt is triggered when a FIFO overflow is detected. An overflow can occur if there is a mismatch between the data input and output rates. A reset of the module is required to restart correctly.
CSI2_IRQENABLE[7] CONTEXT7	At least one interrupt event enabled from Context 7 occurred (see Table 8-9).
CSI2_IRQENABLE[6] CONTEXT6	At least one interrupt event enabled from Context 6 occurred (see Table 8-9).
CSI2_IRQENABLE[5] CONTEXT5	At least one interrupt event enabled from Context 5 occurred (see Table 8-9).
CSI2_IRQENABLE[4] CONTEXT4	At least one interrupt event enabled from Context 4 occurred (see Table 8-9).
CSI2_IRQENABLE[3] CONTEXT3	At least one interrupt event enabled from Context 3 occurred (see Table 8-9).
CSI2_IRQENABLE[2] CONTEXT2	At least one interrupt event enabled from Context 2 occurred (see Table 8-9).
CSI2_IRQENABLE[1] CONTEXT1	At least one interrupt event enabled from Context 1 occurred (see Table 8-9).
CSI2_IRQENABLE[0] CONTEXT0	At least one interrupt event enabled from Context 0 occurred (see Table 8-9).

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Table 8-8 lists CSI2 receiver event generation through the CSI2-A/CSI2-B complex I/O interrupt status and interrupt enable registers. The events are checked and controlled from the CSI2_COMPLEXIO_IRQSTATUS and CSI2_COMPLEXIO_IRQENABLE registers.

Table 8-8. ISS CSI2-A and CSI2-B Receivers Complex I/O Interrupts

Event and Register	Description
CSI2_COMPLEXIO_IRQENABLE[0] ERRSOTHS1	Start of transmission error for lane 1
CSI2_COMPLEXIO_IRQENABLE[1] ERRSOTHS2	Start of transmission error for lane 2
CSI2_COMPLEXIO_IRQENABLE[2] ERRSOTHS3	Start of transmission error for lane 3
CSI2_COMPLEXIO_IRQENABLE[5] ERRSOTSYNCHS1	Start of transmission sync error for lane 1
CSI2_COMPLEXIO_IRQENABLE[6] ERRSOTSYNCHS2	Start of transmission sync error for lane 2
CSI2_COMPLEXIO_IRQENABLE[7] ERRSOTSYNCHS3	Start of transmission sync error for lane 3
CSI2_COMPLEXIO_IRQENABLE[10] ERRESC1	Escape entry error for lane 1
CSI2_COMPLEXIO_IRQENABLE[11] ERRESC2	Escape entry error for lane 2
CSI2_COMPLEXIO_IRQENABLE[12] ERRESC3	Escape entry error for lane 3
CSI2_COMPLEXIO_IRQENABLE[15] ERRCONTROL1	Control error for lane 1
CSI2_COMPLEXIO_IRQENABLE[16] ERRCONTROL2	Control error for lane 2
CSI2_COMPLEXIO_IRQENABLE[17] ERRCONTROL3	Control error for lane 3
CSI2_COMPLEXIO_IRQENABLE[20] STATEULPM1	Lane 1 in ULPM
CSI2_COMPLEXIO_IRQENABLE[21] STATEULPM2	Lane 2 in ULPM
CSI2_COMPLEXIO_IRQENABLE[22] STATEULPM3	Lane 3 in ULPM
CSI2_COMPLEXIO_IRQENABLE[25] STATEALLULPMENTER	All active lanes are entering the ULPM.
CSI2_COMPLEXIO_IRQENABLE[26] STATEALLULPMEXIT	At least one active lane exited the ULPM.

Because the CSI2-A/CSI2-B receivers support eight contexts, the CSI2_CTX_IRQSTATUS_i and CSI2_CTX_IRQENABLE_i registers are present eight times (one time per context).

The events are generated only for the enabled context(s). Table 8-9 describes the generation of the CS12 receiver event through the CSI2_CTX_IRQSTATUS_i and CSI2_CTX_IRQENABLE_i registers.

Table 8-9. ISS CSI2-A/CSI2-B Receivers CONTEXT Interrupts

Event [(1)]	Description
CSI2_CTX_IRQENABLE_i[0] FS_IRQ	Frame start: This interrupt is triggered when a frame-start synchronization code is detected in the CSI2 data stream.
CSI2_CTX_IRQENABLE_i[1] FE_IRQ	Frame end: This interrupt is triggered when a frame-end synchronization code is detected in the CSI2 data stream.
CSI2_CTX_IRQENABLE_i[2] LS_IRQ	Line start: This interrupt is triggered when a line-start synchronization code is detected in the CSI2 data stream.
CSI2_CTX_IRQENABLE_i[3] LE_IRQ	Line end: This interrupt is triggered when a line-end synchronization code is detected in the CSI2 data stream.
CSI2_CTX_IRQENABLE_i[5] CS_IRQ	CS error: This interrupt is triggered when a mismatch between the transmitter and receiver checksums (payload) is detected.
CSI2_CTX_IRQENABLE_i[6] FRAME_NUMBER_IRQ	Frame counter reached: This interrupt is triggered when the frame counter reaches its programmable target value.
CSI2_CTX_IRQENABLE_i[7] LINE_NUMBER_IRQ	Line number reached: The programmable line number is received. The modulo feature can be selected (CSI2_CTX_CTRL1_i.LINE_MODULO). When selected, the interrupt is generated for each line number multiple of the programmed line number (CSI2_CTX_CTRL3_i.LINE_NUMBER); otherwise, the interrupt is generated only for the line number.
CSI2_CTX_IRQENABLE_i[8] ECC_CORRECTION_IRQ	ECC was used to correct a 1-bit error (long packets only).

(1) i = 0 to 7

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8.1.2.1.2.3 ISS CCP2 Interrupts

Table 8-10 summarizes the CCP2 receiver interrupts.

Table 8-10. ISS CCP2 Receiver Interrupts

Event and Register	Description
CCP2_LC01_IRQENABLE[31] LC1_OCPERROR_IRQ	CCP2 write master interface port error on logical channel 1
CCP2_LC01_IRQENABLE[27] LC1_FS_IRQ	CCP2 frame-start synchronization code detection on logical channel 1. This interrupt is triggered when a frame-start synchronization code is detected in the CCP2 data stream.
CCP2_LC01_IRQENABLE[26] LC1_LE_IRQ	CCP2 line-end synchronization code detection on logical channel 1. This interrupt is triggered when a line-end synchronization code is detected in the CCP2 data stream.
CCP2_LC01_IRQENABLE[25] LC1_LS_IRQ	CCP2 line-start synchronization code detection on logical channel 1. This interrupt is triggered when a line-start synchronization code is detected in the CCP2 data stream.
CCP2_LC01_IRQENABLE[24] LC1_FE_IRQ	CCP2 frame-end synchronization code detection on logical channel 1. This interrupt is triggered when a frame-end synchronization code is detected in the CCP2 data stream.
CCP2_LC01_IRQENABLE[23] LC1_COUNT_IRQ	CCP2 frame counter reached on logical channel 1. This interrupt is triggered when the frame counter reaches its programmable target value.
CCP2_LC01_IRQENABLE[21] LC1_FIFO_OVF_IRQ	CCP2 FIFO overflow error for logical channel 1. An overflow can occur if there is a mismatch between the data input and output rates.
CCP2_LC01_IRQENABLE[20] LC1_CRC_IRQ	CCP2 CRC error for logical channel 1. This interrupt is triggered when a mismatch between the transmitter and receiver checksums is detected.
CCP2_LC01_IRQENABLE[19] LC1_FSP_IRQ	CCP2 false-synchronization protection code error for logical channel 1. This interrupt is triggered by the FSP decoder if an illegal combination is detected, but 0xA5 is not present in the bitstream.
CCP2_LC01_IRQENABLE[18] LC1_FW_IRQ	CCP2 frame-width error for logical channel 1. This interrupt is generated if the frame width constraints associated with the current data type are not respected.
CCP2_LC01_IRQENABLE[17] LC1_FSC_IRQ	CCP2 false-synchronization code error for logical channel 1. This interrupt is triggered if the synchronization code order is not respected. This state is shown in the CCP2 receiver finite state-machine (FSM).
CCP2_LC01_IRQENABLE[15] LC0_OCPERROR_IRQ	CCP2 write master interface port error on logical channel 1
CCP2_LC01_IRQENABLE[11] LC0_FS_IRQ	CCP2 frame-start synchronization code detection on logical channel 0. This interrupt is triggered when a frame-start synchronization code is detected in the CCP2 data stream.
CCP2_LC01_IRQENABLE[10] LC0_LE_IRQ	CCP2 line-end synchronization code detection on logical channel 0. This interrupt is triggered when a line-end synchronization code is detected in the CCP2 data stream.
CCP2_LC01_IRQENABLE[9] LC0_LS_IRQ	CCP2 line-start synchronization code detection on logical channel 0. This interrupt is triggered when a line-start synchronization code is detected in the CCP2 data stream.
CCP2_LC01_IRQENABLE[8] LC0_FE_IRQ	CCP2 frame-end synchronization code detection on logical channel 0. This interrupt is triggered when a frame-end synchronization code is detected in the CCP2 data stream.
CCP2_LC01_IRQENABLE[7] LC0_COUNT_IRQ	CCP2 frame counter reached on logical channel 0. This interrupt is triggered when the frame counter reaches its programmable target value.
CCP2_LC01_IRQENABLE[5] LC0_FIFO_OVF_IRQ	CCP2 FIFO overflow error for logical channel 0. An overflow can occur if there is a mismatch between the data input and output rates.
CCP2_LC01_IRQENABLE[4] LC0_CRC_IRQ	CCP2 CRC error for logical channel 0. This interrupt is triggered when a mismatch between the transmitter and receiver checksums is detected.
CCP2_LC01_IRQENABLE[3] LC0_FSP_IRQ	CCP2 false-synchronization code error for logical channel 0. This interrupt is triggered if the synchronization code order is not respected. This state is shown in the CCP2 receiver FSM.
CCP2_LC01_IRQENABLE[2] LC0_FW_IRQ	CCP2 frame-width error for logical channel 0. This interrupt is generated if the frame-width constraints associated with the current data type are not respected.

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Table 8-10. ISS CCP2 Receiver Interrupts (continued)

Event and Register	Description
CCP2_LC01_IRQENABLE[1] LC0_FSC_IRQ	CCP2 false-synchronization code error for logical channel 0. This interrupt is triggered if the synchronization code order is not respected. This state is shown in the CCP2 receiver FSM.
CCP2_LC23_IRQENABLE[31] LC3_OCPERROR_IRQ	CCP2 write master interface port error on logical channel 3
CCP2_LC23_IRQENABLE[27] LC3_FS_IRQ	CCP2 frame-start synchronization code detection on logical channel 3. This interrupt is triggered when a frame-start synchronization code is detected in the CCP2 data stream.
CCP2_LC23_IRQENABLE[26] LC3_LE_IRQ	CCP2 line-end synchronization code detection on logical channel 3. This interrupt is triggered when a line-end synchronization code is detected in the CCP2 data stream.
CCP2_LC23_IRQENABLE[25] LC3_LS_IRQ	CCP2 line-start synchronization code detection on logical channel 3. This interrupt is triggered when a line-start synchronization code is detected in the CCP2 data stream.
CCP2_LC23_IRQENABLE[24] LC3_FE_IRQ	CCP2 frame-end synchronization code detection on logical channel 3. This interrupt is triggered when a frame-end synchronization code is detected in the CCP2 data stream.
CCP2_LC23_IRQENABLE[23] LC3_COUNT_IRQ	CCP2 frame counter reached on logical channel 3. This interrupt is triggered when the frame counter reaches its programmable target value.
CCP2_LC23_IRQENABLE[21] LC3_FIFO_OVF_IRQ	CCP2 FIFO overflow error for logical channel 3. An overflow can occur if there is a mismatch between the data input and output rates.
CCP2_LC23_IRQENABLE[20] LC3_CRC_IRQ	CCP2 CRC error for logical channel 3. This interrupt is triggered when a mismatch between the transmitter and receiver checksums is detected.
CCP2_LC23_IRQENABLE[19] LC3_FSP_IRQ	CCP2 false-synchronization code error for logical channel 3. This interrupt is triggered if the synchronization code order is not respected. This state is shown in the CCP2 receiver FSM.
CCP2_LC23_IRQENABLE[18] LC3_FW_IRQ	CCP2 frame-width error for logical channel 3. This interrupt is generated if the frame-width constraints associated with the current data type are not respected.
CCP2_LC23_IRQENABLE[17] LC3_FSC_IRQ	CCP2 false-synchronization code error for logical channel 3. This interrupt is triggered if the synchronization code order is not respected. This state is shown in the CCP2 receiver FSM.
CCP2_LC23_IRQENABLE[11] LC2_FS_IRQ	CCP2 frame-start synchronization code detection on logical channel 2. This interrupt is triggered on the detection of a frame-start synchronization code into the CCP2 data stream.
CCP2_LC23_IRQENABLE[10] LC2_LE_IRQ	CCP2 line-end synchronization code detection on logical channel 2. This interrupt is triggered on the detection of a line-end synchronization code into the CCP2 data stream.
CCP2_LC23_IRQENABLE[9] LC2_LS_IRQ	CCP2 line-start synchronization code detection on logical channel 2. This interrupt is triggered when a line-start synchronization code is detected in the CCP2 data stream.
CCP2_LC23_IRQENABLE[8] LC2_FE_IRQ	CCP2 frame-end synchronization code detection on logical channel 2. This interrupt is triggered when a frame-end synchronization code is detected in the CCP2 data stream.
CCP2_LC23_IRQENABLE[7] LC2_COUNT_IRQ	CCP2 frame counter reached on logical channel 2. This interrupt is triggered when the frame counter reaches its programmable target value.
CCP2_LC23_IRQENABLE[5] LC2_FIFO_OVF_IRQ	CCP2 FIFO overflow error for logical channel 2. An overflow can occur if there is a mismatch between the data input and output rates.
CCP2_LC23_IRQENABLE[4] LC2_CRC_IRQ	CCP2 CRC error for logical channel 2. This interrupt is triggered when a mismatch is detected between the transmitter and receiver checksums.
CCP2_LC23_IRQENABLE[3] LC2_FSP_IRQ	CCP2 false-synchronization code error for logical channel 2. This interrupt is triggered if the synchronization code order is not respected. This state is shown in the CCP2 receiver FSM.
CCP2_LC23_IRQENABLE[2] LC2_FW_IRQ	CCP2 frame-width error for logical channel 2. This interrupt is generated if the frame-width constraints associated with the current data type are not respected.
CCP2_LC23_IRQENABLE[1] LC2_FSC_IRQ	CCP2 false-synchronization code error for logical channel 2. This interrupt is triggered if the synchronization code order is not respected. This state is shown in the CCP2 receiver FSM.

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Table 8-10. ISS CCP2 Receiver Interrupts (continued)

Event and Register	Description
CCP2_LCM_IRQENABLE[1] LCM_OCPERROR	CCP2 an interface error occurred on the master read port. This interrupt is triggered when an OCP error is detected on the master read port.
CCP2_LCM_IRQENABLE[0] LCM_EOF	Memory read channel – end of frame: This interrupt is triggered when a frame is read completely from memory.

8.1.2.1.2.4 ISS CBUFF Interrupts

Table 8-11 summarizes the CBUFF interrupts.

Table 8-11. ISS CBUFF Interrupts

Event and Register	Description
CBUFF_HL_IRQENABLE_SET[31] IRQ_CTX7_OVR	CBUFF overflow
CBUFF_HL_IRQENABLE_SET[30] IRQ_CTX6_OVR	CBUFF overflow
CBUFF_HL_IRQENABLE_SET[29] IRQ_CTX5_OVR	CBUFF overflow
CBUFF_HL_IRQENABLE_SET[28] IRQ_CTX4_OVR	CBUFF overflow
CBUFF_HL_IRQENABLE_SET[27] IRQ_CTX3_OVR	CBUFF overflow
CBUFF_HL_IRQENABLE_SET[26] IRQ_CTX2_OVR	CBUFF overflow
CBUFF_HL_IRQENABLE_SET[25] IRQ_CTX1_OVR	CBUFF overflow
CBUFF_HL_IRQENABLE_SET[24] IRQ_CTX0_OVR	CBUFF overflow
CBUFF_HL_IRQENABLE_SET[23] IRQ_CTX7_INVALID	CBUFF invalid access
CBUFF_HL_IRQENABLE_SET[22] IRQ_CTX6_INVALID	CBUFF invalid access
CBUFF_HL_IRQENABLE_SET[21] IRQ_CTX5_INVALID	CBUFF invalid access
CBUFF_HL_IRQENABLE_SET[20] IRQ_CTX4_INVALID	CBUFF invalid access
CBUFF_HL_IRQENABLE_SET[19] IRQ_CTX3_INVALID	CBUFF invalid access
CBUFF_HL_IRQENABLE_SET[18] IRQ_CTX2_INVALID	CBUFF invalid access
CBUFF_HL_IRQENABLE_SET[17] IRQ_CTX1_INVALID	CBUFF invalid access
CBUFF_HL_IRQENABLE_SET[16] IRQ_CTX0_INVALID	CBUFF invalid access
CBUFF_HL_IRQENABLE_SET[15] IRQ_CTX7_READY	CBUFF WB physical window ready for access by the CPU
CBUFF_HL_IRQENABLE_SET[14] IRQ_CTX6_READY	CBUFF WB physical window ready for access by the CPU
CBUFF_HL_IRQENABLE_SET[13] IRQ_CTX5_READY	CBUFF WB physical window ready for access by the CPU
CBUFF_HL_IRQENABLE_SET[12] IRQ_CTX4_READY	CBUFF WB physical window ready for access by the CPU
CBUFF_HL_IRQENABLE_SET[11] IRQ_CTX3_READY	CBUFF WB physical window ready for access by the CPU
CBUFF_HL_IRQENABLE_SET[10] IRQ_CTX2_READY	CBUFF WB physical window ready for access by the CPU
CBUFF_HL_IRQENABLE_SET[9] IRQ_CTX1_READY	CBUFF WB physical window ready for access by the CPU
CBUFF_HL_IRQENABLE_SET[8] IRQ_CTX0_READY	CBUFF WB physical window ready for access by the CPU
CBUFF_HL_IRQENABLE_SET[0] IRQ_OCP_ERR	CBUFF master interface port error

8.1.2.1.2.5 ISS BTE Interrupts

Table 8-12 summarizes the BTE interrupts.

Table 8-12. ISS BTE Interrupts

Event and Register	Description
BTE_HL_IRQENABLE_SET[31] IRQ_CTX7_ERR	Writes enable notification for read request before enough data is prefetched. Reads notify when a read request that requires translation on Context 7 is received, but not enough frame lines have been prefetched in the buffer. See Section 8.2.7.3.2.4.3, *iSS BTE Buffer Prefetch*.

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Table 8-12. ISS BTE Interrupts (continued)

Event and Register	Description
BTE_HL_IRQENABLE_SET[30] IRQ_CTX6_ERR	Writes enable notification for read request before enough data is prefetched. Reads notify when a read request that requires translation on Context 6 is received, but not enough frame lines have been prefetched in the buffer. See Section 8.2.7.3.2.4.3, *ISS BTE Buffer Prefetch*.
BTE_HL_IRQENABLE_SET[29] IRQ_CTX5_ERR	Writes enable notification for read request before enough data is prefetched. Reads notify when a read request that requires translation on Context 5 is received, but not enough frame lines have been prefetched in the buffer. See Section 8.2.7.3.2.4.3, *ISS BTE Buffer Prefetch*.
BTE_HL_IRQENABLE_SET[28] IRQ_CTX4_ERR	Writes enable notification for read request before enough data is prefetched. Reads notify when a read request that requires translation on Context 4 is received, but not enough frame lines have been prefetched in the buffer. See Section 8.2.7.3.2.4.3, *ISS BTE Buffer Prefetch*.
BTE_HL_IRQENABLE_SET[27] IRQ_CTX3_ERR	Writes enable notification for read request before enough data is prefetched. Reads notify when a read request that requires translation on Context 3 is received, but not enough frame lines have been prefetched in the buffer. See Section 8.2.7.3.2.4.3, *ISS BTE Buffer Prefetch*.
BTE_HL_IRQENABLE_SET[26] IRQ_CTX2_ERR	Writes enable notification for read request before enough data is prefetched. Reads notify when a read request that requires translation on Context 2 is received, but not enough frame lines have been prefetched in the buffer. See Section 8.2.7.3.2.4.3, *ISS BTE Buffer Prefetch*.
BTE_HL_IRQENABLE_SET[25] IRQ_CTX1_ERR	Writes enable notification for read request before enough data is prefetched. Reads notify when a read request that requires translation on Context 1 is received, but not enough frame lines have been prefetched in the buffer. See Section 8.2.7.3.2.4.3, *ISS BTE Buffer Prefetch*.
BTE_HL_IRQENABLE_SET[24] IRQ_CTX0_ERR	Writes enable notification for read request before enough data is prefetched. Reads notify when a read request that requires translation on Context 0 is received, but not enough frame lines have been prefetched in the buffer. See Section 8.2.7.3.2.4.3, *ISS BTE Buffer Prefetch*.
BTE_HL_IRQENABLE_SET[23] IRQ_CTX7_INVALID	Writes enable invalid access to Context 7. Reads notify when access to an unexpected location in Context 7 is requested, or the start context location access is valid, but the burst length exceeds the Context 7 end. See Section 8.2.7.3.2.2, *ISS BTE Virtual Address Space and Context Mapping*.
BTE_HL_IRQENABLE_SET[22] IRQ_CTX6_INVALID	Writes enable invalid access to Context 6. Reads notify when access to an unexpected location in Context 6 is requested, or the start context location access is valid, but the burst length exceeds the Context 6 end. See Section 8.2.7.3.2.2, *ISS BTE Virtual Address Space and Context Mapping*.
BTE_HL_IRQENABLE_SET[21] IRQ_CTX5_INVALID	Writes enable invalid access to Context 5. Reads notify when access to an unexpected location in Context 5 is requested, or the start context location access is valid, but the burst length exceeds the Context 5 end. See Section 8.2.7.3.2.2, *ISS BTE Virtual Address Space and Context Mapping*.
BTE_HL_IRQENABLE_SET[20] IRQ_CTX4_INVALID	Writes enable invalid access to Context 4. Reads notify when access to an unexpected location in Context 4 is requested, or the start context location access is valid, but the burst length exceeds the Context 4 end. See Section 8.2.7.3.2.2, *ISS BTE Virtual Address Space and Context Mapping*.
BTE_HL_IRQENABLE_SET[19] IRQ_CTX3_INVALID	Writes enable invalid access to Context 3. Reads notify when access to an unexpected location in Context 3 is requested, or the start context location access is valid, but the burst length exceeds the Context 3 end. See Section 8.2.7.3.2.2, *ISS BTE Virtual Address Space and Context Mapping*.

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Table 8-12. ISS BTE Interrupts (continued)

Event and Register	Description
BTE_HL_IRQENABLE_SET[18] IRQ_CTX2_INVALID	Writes enable invalid access to Context 2. Reads notify when access to an unexpected location in Context 2 is requested, or the start context location access is valid, but the burst length exceeds the Context 2 end. See Section 8.2.7.3.2.2, *ISS BTE Virtual Address Space and Context Mapping*.
BTE_HL_IRQENABLE_SET[17] IRQ_CTX1_INVALID	Writes enable invalid access to Context 1. Reads notify when access to an unexpected location in Context 1 is requested, or the start context location access is valid, but the burst length exceeds the Context 1 end. See Section 8.2.7.3.2.2, *ISS BTE Virtual Address Space and Context Mapping*.
BTE_HL_IRQENABLE_SET[16] IRQ_CTX0_INVALID	Writes enable invalid access to Context 0. Reads notify when access to an unexpected location in Context 0 is requested, or the start context location access is valid, but the burst length exceeds the Context 0 end. See Section 8.2.7.3.2.2, *ISS BTE Virtual Address Space and Context Mapping*.
BTE_HL_IRQENABLE_SET[15] IRQ_CTX7_DONE	Writes enable notification for context that has been fully and successfully transferred to TILER. Reads notify when enough frame lines have been prefetched into the buffer and Context 7 is translated to TILER. This interrupt is triggered when flushing completes (if enabled) in one-shot mode. It is triggered once per frame in continuous mode. See Section 8.2.7.3.2.4.3, *ISS BTE Buffer Prefetch*.
BTE_HL_IRQENABLE_SET[14] IRQ_CTX6_DONE	Writes enable notification for context that has been fully and successfully transferred to TILER. Reads notify when enough frame lines have been prefetched into the buffer and Context 6 is translated to TILER. This interrupt is triggered when flushing completes (if enabled) in one-shot mode. It is triggered once per frame in continuous mode. See Section 8.2.7.3.2.4.3, *ISS BTE Buffer Prefetch*.
BTE_HL_IRQENABLE_SET[13] IRQ_CTX5_DONE	Writes enable notification for context that has been fully and successfully transferred to TILER. Reads notify when enough frame lines have been prefetched into the buffer and Context 5 is translated to TILER. This interrupt is triggered when flushing completes (if enabled) in one-shot mode. It is triggered once per frame in continuous mode. See Section 8.2.7.3.2.4.3, *ISS BTE Buffer Prefetch*.
BTE_HL_IRQENABLE_SET[12] IRQ_CTX4_DONE	Writes enable notification for context that has been fully and successfully transferred to TILER. Reads notify when enough frame lines have been prefetched into the buffer and Context 4 is translated to TILER. This interrupt is triggered when flushing completes (if enabled) in one-shot mode. It is triggered once per frame in continuous mode. See Section 8.2.7.3.2.4.3, *ISS BTE Buffer Prefetch*.
BTE_HL_IRQENABLE_SET[11] IRQ_CTX3_DONE	Writes enable notification for context that has been fully and successfully transferred to TILER. Reads notify when enough frame lines have been prefetched into the buffer and Context 3 is translated to TILER. This interrupt is triggered when flushing completes (if enabled) in one-shot mode. It is triggered once per frame in continuous mode. See Section 8.2.7.3.2.4.3, *ISS BTE Buffer Prefetch*.
BTE_HL_IRQENABLE_SET[10] IRQ_CTX2_DONE	Writes enable notification for context that has been fully and successfully transferred to TILER. Reads notify when enough frame lines have been prefetched into the buffer and Context 2 is translated to TILER. This interrupt is triggered when flushing completes (if enabled) in one-shot mode. It is triggered once per frame in continuous mode. See Section 8.2.7.3.2.4.3, *ISS BTE Buffer Prefetch*.
BTE_HL_IRQENABLE_SET[9] IRQ_CTX1_DONE	Writes enable notification for context that has been fully and successfully transferred to TILER. Reads notify when enough frame lines have been prefetched into the buffer and Context 1 is translated to TILER. This interrupt is triggered when flushing completes (if enabled) in one-shot mode. It is triggered once per frame in continuous mode. See Section 8.2.7.3.2.4.3, *ISS BTE Buffer Prefetch*.

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Table 8-12. ISS BTE Interrupts (continued)

Event and Register	Description
BTE_HL_IRQENABLE_SET[8] IRQ_CTX0_DONE	Writes enable notification for context that has been fully and successfully transferred to TILER. Reads notify when enough frame lines have been prefetched into the buffer and Context 0 is translated to TILER. This interrupt is triggered when flushing completes (if enabled) in one-shot mode. It is triggered once per frame in continuous mode. See Section 8.2.7.3.2.4.3, *ISS BTE Buffer Prefetch*.
BTE_HL_IRQENABLE_SET[1] IRQ_INVALID	Writes enable Invalid virtual space access notification. Reads notify when access falls into a translated from the BTE region, but it is 2D access or it does not map to an active context. See Section 8.2.7.3.2.4.3, *ISS BTE Virtual Address Space and Context Mapping*.
BTE_HL_IRQENABLE_SET[1] IRQ_OCP_ERR	Writes enable notification for error on the master output interface. Reads notify when an error has occurred on the master output interface.

8.1.2.1.2.6 ISS SIMCOP Interrupts

Table 8-13 summarizes the SIMCOP high-level interrupts mapped to the outer boundaries of the SIMCOP. For more information about interrupts generated from inside the SIMCOP modules, see the SIMCOP section.

Table 8-13. ISS SIMCOP High-Level Interrupts

Event and Register	Description
SIMCOP_HL_IRQENABLE_SET_i[19] CPU_PROC_START_IRQ	Interrupt used when CPU data processing is used in a macroblock processing pipeline. When the CPU receives this IRQ, data is ready to be processed. When the CPU finishes processing the data, it acknowledges by setting the SIMCOP_HWSEQ_CTRL.CPU_PROC_DONE bit.
SIMCOP_HL_IRQENABLE_SET_i[18] SIMCOP_DMA_IRQ1	Interrupt triggered by SIMCOP DMA
SIMCOP_HL_IRQENABLE_SET_i[16] OCP_ERR_IRQ	SIMCOP master port interface error
SIMCOP_HL_IRQENABLE_SET_i[15] VLCDJ_DECODE_ERR_IRQ	A decode error has been signaled by the VLCDJ module.
SIMCOP_HL_IRQENABLE_SET_i[14] DONE_IRQ	Event triggered when hardware sequencer finishes the sequence: • The sequence step counter has reached the limit. • All accelerator and DMA events for the last sequence step have been received.
SIMCOP_HL_IRQENABLE_SET_i[13] STEP3_IRQ	Event triggered when a SIMCOP Context 3 is activated by the hardware sequencer.
SIMCOP_HL_IRQENABLE_SET_i[12] STEP2_IRQ	Event triggered when a SIMCOP Context 2 is activated by the hardware sequencer.
SIMCOP_HL_IRQENABLE_SET_i[11] STEP1_IRQ	Event triggered when a SIMCOP Context 1 is activated by the hardware sequencer.
SIMCOP_HL_IRQENABLE_SET_i[10] STEP0_IRQ	Event triggered when a SIMCOP Context 0 is activated by the hardware sequencer.
SIMCOP_HL_IRQENABLE_SET_i[9] LDC_BLOCK_IRQ	A macroblock has been processed.
SIMCOP_HL_IRQENABLE_SET_i[7] ROT_A	Rotational engine interrupt
SIMCOP_HL_IRQENABLE_SET_i[6] IMX_B_IRQ	Event triggered when iMX has executed a SLEEP instruction
SIMCOP_HL_IRQENABLE_SET_i[5] IMX_A_IRQ	Event triggered when iMX has executed a SLEEP instruction
SIMCOP_HL_IRQENABLE_SET_i[4] NSF_IRQ	Event triggered by the NSD2 imaging accelerator when processing of a block is done
SIMCOP_HL_IRQENABLE_SET_i[3] VLCDJ_BLOC_IRQ	A macroblock has been processed (that is, encode and decode).
SIMCOP_HL_IRQENABLE_SET_i[2] DCT_IRQ	DCT operating is complete (configured number of MCUs for YUV4:2:0/4:2:2 mode, or number of blocks for sequential block mode).
SIMCOP_HL_IRQENABLE_SET_i[1] LDC_FRAME_IRQ	A full frame has been processed.

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Table 8-13. ISS SIMCOP High-Level Interrupts (continued)

Event and Register	Description
SIMCOP_HL_IRQENABLE_SET_i[0] SIMCOP_DMA_IRQ0	Interrupt triggered by SIMCOP DMA

8.1.2.2 ISS Clocks

The clocks of ISS submodules can be cut individually using the ISS_CLKCTRL register. Software can poll the module status reading the appropriate bit in the ISS_CLKSTAT register.

When software wants to enable a submodule:

- Software sets the appropriate bit in the ISS_CLKCTRL register.
- Hardware enables the submodule functional and interface clocks (expected to take a few cycles).
- Hardware sets the appropriate bit in the ISS_CLKSTAT register.

Software must enable the modules in the correct order. The hardware imposes no particular constraint. For example, when data must be provided by the CSI2-A/CSI2-B receiver and processed by the ISP, both modules must be enabled and correctly configured before data arrives. An example of configuration order is: enabling the CSI2-A receiver powers up the complex I/O connected to the external sensor. Additionally, the ISP must be configured and the source interface must be selected. For details and the order of configuration, see the programming module of the particular submodule.

When software wants to shut down a submodule:

- Software ensures that the submodule is idle. Mainly:
  - The submodule must not generate new events.
  - The submodule must not have any pending events.
  - For initiators: The submodule must stop the generation of an interface bridge transaction.
- Software clears the appropriate bit in the ISS_CLKCTRL register.
- For modules having only a master port: Hardware waits until the submodule to be disconnected asserts the MStandBy signal on its master port. It asserts MWait of the submodule.

NOTE: The ISS does not assert the MWait signal when a shutdown of the module is not requested by software.

- Hardware cuts the submodule clocks.
- Hardware clears the appropriate bit in the ISS_CLKSTAT register.

Table 8-14 describes the clock gating of the ISS submodule.

Table 8-14. ISS Submodule Clock Gating

ISS Resource	Feature On/Off Control
ISS top-level resources	Not applicable. ISS top-level resources cannot be cut. However, top-level resources support the autogating feature.
SIMCOP	ISS_CLKCTRL[0] SIMCOP
ISP	ISS_CLKCTRL[1] ISP
CSI2-A	ISS_CLKCTRL[2] CSI2_A
CSI2-B	ISS_CLKCTRL[3] CSI2_B
CCP2	ISS_CLKCTRL[4] CCP2
ISS interconnect BTE CBUFF TCTRL	These modules cannot be switched off individually. They are required for any processing performed by SIMCOP because they are on the main data path. However, they support autogating to reduce power consumption when activity is low.

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When the clock of a submodule is cut and an interface bridge request for this module is received from the ISS configuration interconnect, the ISS clock manager temporarily enables the module clock to handle the access properly.

All ISS submodules are off after reset; software must enable them before they can be used.

8.1.2.3 ISS Reset

The ISS can accept a general software reset, propagated through all the hierarchy. This reset can be done to initialize the module and has the same effect as the hardware reset.

1. Set the ISS_HL_SYSCONFIG[0] SOFTRESET bit to 1.
2. Read the ISS_HL_SYSCONFIG[0] SOFTRESET bit to check whether it equals 0, which means the reset occurred.

If after five reads, ISS_HL_SYSCONFIG[0] SOFTRESET still returns 1, it can be assumed that an error occurred during the reset stage.

A software reset must not reset the power manager protocols (must not reset the IDLE and STANDBY generic IPs).

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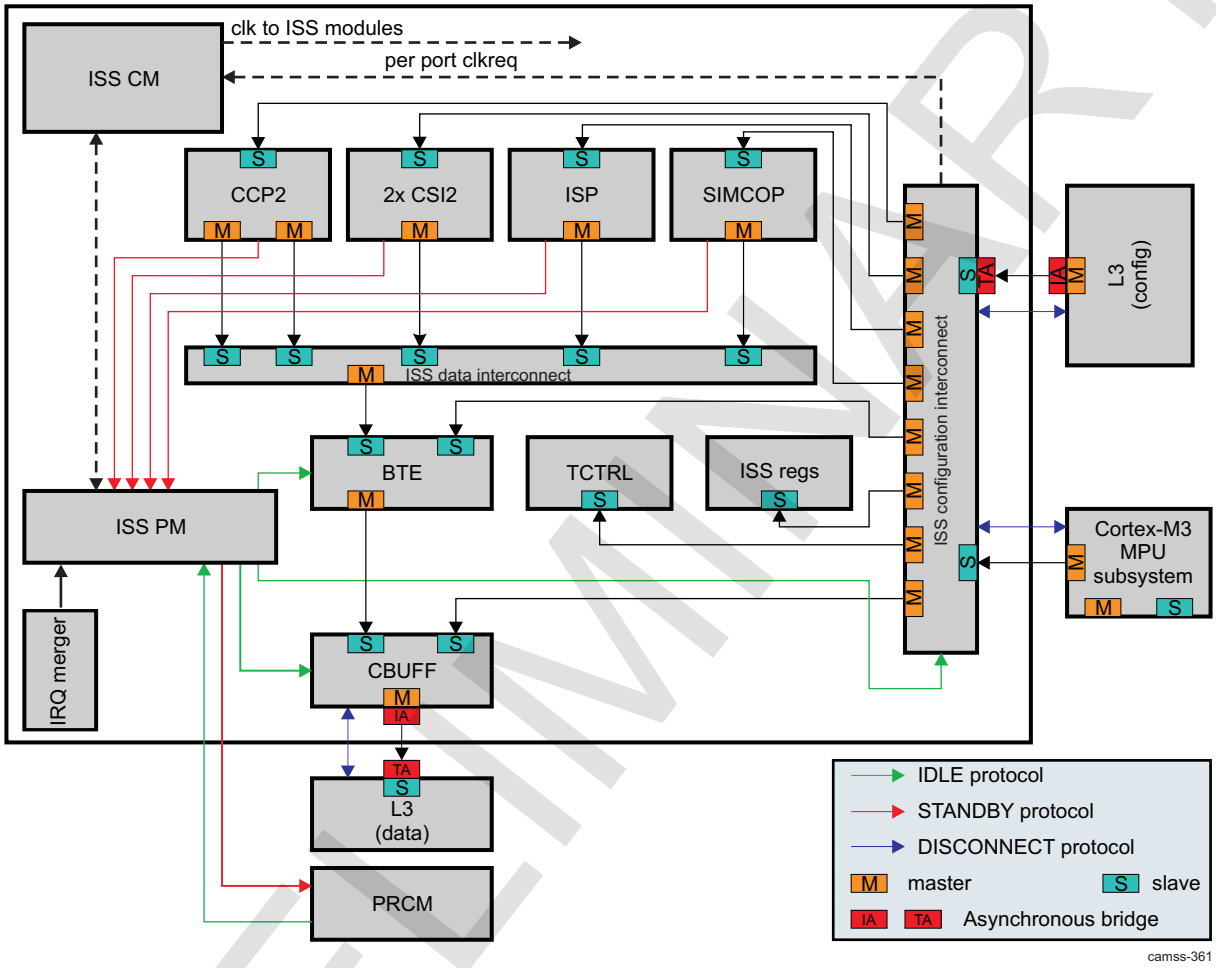
8.1.2.4 ISS Power Management

8.1.2.4.1 ISS Power-Management Infrastructure Overview

Figure 8-4 is an overview of the ISS power management.

Figure 8-4. ISS Power Management



NOTE: For power savings, the PRCM module can request idle mode from the ISS. When the ISS is not functional, software must decide when the PRCM module can send the request. For more information, see Section 3.1.1.1.2, *Module Level Clock Management*, in Chapter 3, *Power, Reset, and Clock Management.*

8.1.2.4.2 ISS STANDBY Mechanism

The power manager receives STANDBY information from the CCP2, CSI2-A, CSI2-B, ISP, and SIMCOP modules. These modules assert a standby signal when they have no more transactions to perform. The ISS power manager acknowledges by asserting a wait signal.

When those five modules are in standby mode, the ISS power manager initiates a STANDBY sequence for the ISS:

1. The ISS waits while the CCP2, CSI2-A, CSI2-B, ISP, and SIMCOP MStandby is asserted.
2. The ISS power manager acknowledges by asserting the CCP2, CSI2-A, CSI2-B, ISP, and SIMCOP MWait signal.
3. The ISS initiators assert only the MStandBy signal when they receive responses to all sent requests.

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Therefore, when all initiators have asserted MStandBy, the ISS interconnect has no more pending traffic (although configurable, only nonposted writes must be used for error reporting).

4. The ISS power manager sends an IDLE request to the BTE. This IDLE request is used to drain BTE data. It does not affect the configuration port.
5. The BTE drains all transactions.
6. The BTE acknowledges the IDLE request.
7. The ISS power manager sends an IDLE request to the CBUFF. This IDLE request is used to drain CBUFF data. It does not affect the configuration port.
8. CBUFF drains all transactions.
9. CBUFF disconnects the interface master port connected to the L3 interconnect.
10. CBUFF acknowledges the IDLE request.
11. The ISS power manager asserts the MStandBy signals connected to the system PRCM module.
12. The PRCM module acknowledges by asserting the MWait signal.

A functional standby transition can be aborted when one of the CCP2, CSI2-A, CSI2-B, ISP, or SIMCOP modules deasserts the MStandBy signal. The corresponding MWait signal is deasserted only when the ISS interconnect, BTE, CBUFF, and ISS interface master port are ready to receive requests.

When one of the CCP2, CSI2-A, CSI2-B, ISP, or SIMCOP modules must perform accesses to the ISS interface master port, it deasserts the MStandBy signal. The ISS power manager executes the following sequence to leave the STANDBY state:

1. The ISS power manager deasserts the MStandby signal.
2. The ISS waits until the PRCM module deasserts the MWait signal.
3. The ISS power manager requests CBUFF to go into functional mode.
4. CBUFF connects the interface port.
5. The ISS power manager requests the BTE to go into functional mode.
6. The ISS power manager waits until CBUFF and BTE acknowledge functional mode.
7. The ISS deasserts the MWait signal of the module requesting access.

Abort of the standby-to-functional mode transition is not supported. The ISS power manager completes the standby-to-functional transition and then allows a new functional-to-standby transition.

Typically, the MStandby signal is used for two purposes. Software chooses one of the following behaviors through PRCM configuration:

- During blanking periods: The ISS asserts the MStandBy signal between frames when it has no more data to send. The PRCM module can use this information to switch off the L3 interconnect and save some dynamic power. However, the PRCM module is not allowed to cut the ISS functional clock in that case, because it is needed to receive the next frame.
- For ISS shutdown: The ISS asserts MStandBy when it has no more transactions to perform. The PRCM module then initiates an IDLE sequence. Once the ISS acknowledges the transition into idle mode, the PRCM module can cut the ISS clock and power.

The internal standby mode can be reached only when CCP2, CSI2-A, CSI2-B, SIMCOP, ISP, ISS data interconnect, BTE, and CBUFF are in IDLE or STANDBY state. Choosing no-idle or no-standby mode for any of these modules prevents the ISS from going into STANDBY state.

Four modes for standby control are supported:

- Smart-standby-wakeup mode: This is the mode normally used. When in this mode, the ISS asserts the MStandBy signal when the MStandBy of all ISS internal initiators is asserted and the ISS data interconnect, BTE, and CBUFF are in IDLE state.
- Smart-standby mode: The ISS has no wake-up event. This mode is equivalent to smart-standby-wakeup mode.
- Force-standby mode: This is a backup mode intended to be used only if smart-standby mode is bugged. When in this mode, the ISS asserts MStandBy unconditionally. Software must ensure that the ISS is in a correct quiet state before programming this mode.
- No-standby mode: This is a backup mode intended to be used only if smart-standby mode is bugged.

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When in this mode, the ISS never asserts the MStandBy signal.

8.1.2.4.3 ISS IDLE Mechanism

The PRCM module can request the ISS to go into IDLE state when the ISS has asserted its MStandBy output.

In a normal case, software must ensure that the ISS is in a quiet state before allowing the PRCM module to send an IDLE request to the ISS:

- The ISS has no more traffic to generate.
- The ISS cannot generate any new interrupts.
- The ISS has no pending interrupts.

When an IDLE request is received from the PRCM module, the ISS power manager verifies that the ISS MWait input has been asserted and that all ISS interrupt outputs are deasserted. It then starts the STANDBY-to-IDLE transition:

1. Send IDLE request to the ISS configuration interconnect.
2. The ISS configuration interconnect requests disconnection of both ISS interface slave ports. Disconnection is done by the master:
   - It stops accepting new requests and drains currently ongoing ones.
   - It waits for completion of all ongoing transactions.
3. The ISS configuration interconnect acknowledges the IDLE transition.
4. The ISS power manager acknowledges the IDLE request from the PRCM module.
5. The PRCM module can cut the ISS clock and power.

The PRCM module first enables the ISS power and clock before requesting the ISS to go into functional state by deasserting the SIdleReq signal. The ISS power manager then executes the wake-up sequence:

1. Request the ISS interconnect to go into functional state.
2. The ISS interconnect connects the ISS slave ports.
3. The ISS interconnect acknowledges transition into functional mode.
4. The ISS power manager acknowledges transition into functional mode (ISS output SIdleAck = 00).

Four modes for IDLE control are supported:

- Smart-idle-wakeup mode [b11]: This is the mode normally used. When in this mode, the ISS acknowledges a request to go idle from the power manager after having performed all hardware operations necessary for the IAF to be in a correct quiet state.
- Smart-idle mode [b10]: This is equivalent to smart-idle-wakeup mode.
- Force-idle mode [b00]: This is a backup mode intended to be used only if smart-idle mode is bugged. When in this mode, the ISS acknowledges a request to go idle from the power manager with no hardware condition. Software must ensure that the ISS is in a correct quiet state before requesting a force-idle transition.
- No-idle mode [b01]: When in this mode, the ISS disregards any request to go idle from the power manager.

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8.1.3 ISS Register Manual

8.1.3.1 ISS Instance Summary

Table 8-15 is the ISS instance.

Table 8-15. ISS Instance Summary

Module Name	Module Base Address	Size
ISS_TOP	0x5200 0000	256 bytes

NOTE: This section contains the ISS TOP registers only. For submodule register details, see the register manual of the particular submodule.

8.1.3.2 ISS Registers

8.1.3.2.1 ISS TOP Register Summary

Table 8-16 summarizes the ISS TOP register mapping.

Table 8-16. ISS TOP Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	ISS_TOP Base Address
ISS_HL_REVISION	R	32	0x0000 0000	0x5200 0000
RESERVED	R	32	0x0000 0004	0x5200 0004
ISS_HL_SYSCONFIG	RW	32	0x0000 0010	0x5200 0010
RESERVED	RW	32	0x0000 001C	0x5200 001C
ISS_HL_IRQSTATUS_RAW_i (1)	RW	32	0x0000 0020 + (0x10 * i)	0x5200 0020 + (0x10 * i)
ISS_HL_IRQSTATUS_i (1)	RW	32	0x0000 0024 + (0x10 * i)	0x5200 0024 + (0x10 * i)
ISS_HL_IRQENABLE_SET_i (1)	RW	32	0x0000 0028 + (0x10 * i)	0x5200 0028 + (0x10 * i)
ISS_HL_IRQENABLE_CLR_i (1)	RW	32	0x0000 002C + (0x10 * i)	0x5200 002C + (0x10 * i)
ISS_CTRL	RW	32	0x0000 0080	0x5200 0080
ISS_CLKCTRL	W	32	0x0000 0084	0x5200 0084
ISS_CLKSTAT	R	32	0x0000 0088	0x5200 0088
ISS_PM_STATUS	R	32	0x0000 008C	0x5200 008C

(1) i = 0 to 5

8.1.3.2.2 ISS TOP Register Description

through describe the ISS TOP registers.

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Table 8-17. ISS_HL_REVISION

Address Offset	0x0000 0000		
Physical Address	0x5200 0000	**Instance**	ISS_TOP
Description	IP Revision Identifier (X.Y.R) Used by software to track features, bugs, and compatibility		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP Revision	R	See(1)

(1) TI internal data

Table 8-18. Register Call Summary for Register ISS_HL_REVISION

ISS Overview

- ISS TOP Register Summary: [0]

Table 8-19. ISS_HL_SYSCONFIG

Address Offset	0x0000 0010		
Physical Address	0x5200 0010	**Instance**	ISS_TOP
Description	Clock management configuration		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																										STANDBYMODE		IDLEMODE		RESERVED	SOFTRESET

Bits	Field Name	Description	Type	Reset
31:6	RESERVED		R	0x0000000
5:4	STANDBYMODE	Master interface power management, standby/Wait control 0x0: Force-standby. MStandby is asserted unconditionally. 0x1: No-standby. MStandby is never asserted. 0x3: Smart-standby 0x2: Smart-standby	RW	0x2
3:2	IDLEMODE	IDLE protocol configuration 0x0: Force-idle 0x1: No-idle 0x3: Smart-idle 0x2: Smart-idle	RW	0x2
1	RESERVED		R	0

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Bits	Field Name	Description	Type	Reset
0	SOFTRESET	Software reset. Write 0x0: No action Write 0x1: Initiate software reset Read 0x1: Reset (software or other) ongoing Read 0x0: Reset done, no pending action	RW	0

Table 8-20. Register Call Summary for Register ISS_HL_SYSCONFIG

ISS Overview
- ISS Reset: [0] [1] [2]
- ISS TOP Register Summary: [3]

Table 8-21. ISS_HL_IRQSTATUS_RAW_i

Address Offset	0x0000 0020 + (0x10 * i)	**Index**	i = 0 to 5
Physical Address	0x5200 0020 + (0x10 * i)	**Instance**	ISS_TOP
Description	Per-event raw interrupt status vector, line 0. Raw status is set even if event is not enabled by setting the ISS_HL_IRQENABLE_SET_i register.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														HS_VS_IRQ	CCP2_IRQ8	SIMCOP_IRQ3	SIMCOP_IRQ2	SIMCOP_IRQ1	SIMCOP_IRQ0	BTE_IRQ	CBUFF_IRQ	CCP2_IRQ3	CCP2_IRQ2	CCP2_IRQ1	CCP2_IRQ0	CSIB_IRQ	CSIA_IRQ	ISP_IRQ3	ISP_IRQ2	ISP_IRQ1	ISP_IRQ0

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17	HS_VS_IRQ	HS or VS synchronization event. This event is triggered if a rising or falling edge is detected on the HS or VS signal (after the video port mux). The rising or falling edge and the HS or VS signal selection is chosen with the ISS_CTRL.SYNC_DETECT bit field. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW	0
16	CCP2_IRQ8	Event generated by the CCP2 receiver Read 0x1: Event pending Read 0x0: No event pending	R	0
15	SIMCOP_IRQ3	Event generated by SIMCOP Read 0x1: Event pending Read 0x0: No event pending	R	0
14	SIMCOP_IRQ2	Event generated by SIMCOP Read 0x1: Event pending Read 0x0: No event pending	R	0
13	SIMCOP_IRQ1	Event generated by SIMCOP Read 0x1: Event pending Read 0x0: No event pending	R	0

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Bits	Field Name	Description	Type	Reset
12	SIMCOP_IRQ0	Event generated by SIMCOP Read 0x1: Event pending Read 0x0: No event pending	R	0
11	BTE_IRQ	Event generated by the burst translation engine Read 0x1: Event pending Read 0x0: No event pending	R	0
10	CBUFF_IRQ	Event generated by the circular buffer Read 0x1: Event pending Read 0x0: No event pending	R	0
9	CCP2_IRQ3	Event generated by the CCP2 receiver Read 0x1: Event pending Read 0x0: No event pending	R	0
8	CCP2_IRQ2	Event generated by the CCP2 receiver Read 0x1: Event pending Read 0x0: No event pending	R	0
7	CCP2_IRQ1	Event generated by the CCP2 receiver Read 0x1: Event pending Read 0x0: No event pending	R	0
6	CCP2_IRQ0	Event generated by the CCP2 receiver Read 0x1: Event pending Read 0x0: No event pending	R	0
5	CSIB_IRQ	Event generated by the CSI2 receiver #b Read 0x1: Event pending Read 0x0: No event pending	R	0
4	CSIA_IRQ	Event generated by the CSI2 receiver #a Read 0x1: Event pending Read 0x0: No event pending	R	0
3	ISP_IRQ3	Combined interrupt event provided by the ISP. Read 0x1: Event pending Read 0x0: No event pending	R	0
2	ISP_IRQ2	Combined interrupt event provided by the ISP. Read 0x1: Event pending Read 0x0: No event pending	R	0
1	ISP_IRQ1	Combined interrupt event provided by the ISP. Read 0x1: Event pending Read 0x0: No event pending	R	0
0	ISP_IRQ0	Combined interrupt event provided by the ISP. Read 0x1: Event pending Read 0x0: No event pending	R	0

Table 8-22. Register Call Summary for Register ISS_HL_IRQSTATUS_RAW_i

ISS Overview

- ISS Interrupts: [0]
- ISS TOP Register Summary: [1]

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Table 8-23. ISS_HL_IRQSTATUS_i

Address Offset	0x0000 0024 + (0x10 * i)	**Index**	i = 0 to 5
Physical Address	0x5200 0024 + (0x10 * i)	**Instance**	ISS_TOP
Description	Per-event "enabled" interrupt status vector, line 0. Enabled status is not set unless event is enabled by setting the ISS_HL_IRQENABLE_SET_i register.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														HS_VS_IRQ	CCP2_IRQ8	SIMCOP_IRQ3	SIMCOP_IRQ2	SIMCOP_IRQ1	SIMCOP_IRQ0	BTE_IRQ	CBUFF_IRQ	CCP2_IRQ3	CCP2_IRQ2	CCP2_IRQ1	CCP2_IRQ0	CSIB_IRQ	CSIA_IRQ	ISP_IRQ3	ISP_IRQ2	ISP_IRQ1	ISP_IRQ0

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17	HS_VS_IRQ	HS or VS synchronization event. This event is triggered if a rising or falling edge is detected on the HS or VS signal (after the video port mux). The rising or falling edge and the HS or VS signal selection is chosen with the ISS_CTRL.SYNC_DETECT bit field. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toSet	0
16	CCP2_IRQ8	Event generated by the CCP2 receiver Read 0x1: Event pending Read 0x0: No (enabled) event pending	R	0
15	SIMCOP_IRQ3	Event generated by SIMCOP Read 0x1: Event pending Read 0x0: No (enabled) event pending	R	0
14	SIMCOP_IRQ2	Event generated by SIMCOP Read 0x1: Event pending Read 0x0: No (enabled) event pending	R	0
13	SIMCOP_IRQ1	Event generated by SIMCOP Read 0x1: Event pending Read 0x0: No (enabled) event pending	R	0
12	SIMCOP_IRQ0	Event generated by SIMCOP Read 0x1: Event pending Read 0x0: No (enabled) event pending	R	0
11	BTE_IRQ	Event generated by the burst translation engine Read 0x1: Event pending Read 0x0: No (enabled) event pending	R	0
10	CBUFF_IRQ	Event generated by the circular buffer Read 0x1: Event pending Read 0x0: No (enabled) event pending	R	0
9	CCP2_IRQ3	Event generated by the CCP2 receiver Read 0x1: Event pending Read 0x0: No (enabled) event pending	R	0

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Bits	Field Name	Description	Type	Reset
8	CCP2_IRQ2	Event generated by the CCP2 receiver Read 0x1: Event pending Read 0x0: No (enabled) event pending	R	0
7	CCP2_IRQ1	Event generated by the CCP2 receiver Read 0x1: Event pending Read 0x0: No (enabled) event pending	R	0
6	CCP2_IRQ0	Event generated by the CCP2 receiver Read 0x1: Event pending Read 0x0: No (enabled) event pending	R	0
5	CSIB_IRQ	Event generated by the CSI2 receiver #b Read 0x1: Event pending Read 0x0: No (enabled) event pending	R	0
4	CSIA_IRQ	Event generated by the CSI2 receiver #a Read 0x1: Event pending Read 0x0: No (enabled) event pending	R	0
3	ISP_IRQ3	Combined interrupt event provided by the ISP. Read 0x1: Event pending Read 0x0: No (enabled) event pending	R	0
2	ISP_IRQ2	Combined interrupt event provided by the ISP. Read 0x1: Event pending Read 0x0: No (enabled) event pending	R	0
1	ISP_IRQ1	Combined interrupt event provided by the ISP. Read 0x1: Event pending Read 0x0: No (enabled) event pending	R	0
0	ISP_IRQ0	Combined interrupt event provided by the ISP. Read 0x1: Event pending Read 0x0: No (enabled) event pending	R	0

Table 8-24. Register Call Summary for Register ISS_HL_IRQSTATUS_i

ISS Overview
- ISS Interrupts: [0] [1]
- ISS TOP Register Summary: [2]

Table 8-25. ISS_HL_IRQENABLE_SET_i

Address Offset	0x0000 0028 + (0x10 * i)	**Index**	i = 0 to 5
Physical Address	0x5200 0028 + (0x10 * i)	**Instance**	ISS_TOP
Description	Per-event interrupt enable bit vector Write 1 to set (enable interrupt). Readout equal to corresponding _CLR register.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														HS_VS_IRQ	CCP2_IRQ8	SIMCOP_IRQ3	SIMCOP_IRQ2	SIMCOP_IRQ1	SIMCOP_IRQ0	BTE_IRQ	CBUFF_IRQ	CCP2_IRQ3	CCP2_IRQ2	CCP2_IRQ1	CCP2_IRQ0	CSIB_IRQ	CSIA_IRQ	ISP_IRQ3	ISP_IRQ2	ISP_IRQ1	ISP_IRQ0

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Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17	HS_VS_IRQ	HS or VS synchronization event. This event is triggered if a rising or falling edge is detected on the HS or VS signal (after the video port mux). The rising or falling edge and the HS or VS signal selection is chosen with the ISS_CTRL.SYNC_DETECT bit field. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
16	CCP2_IRQ8	Event generated by the CCP2 receiver Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
15	SIMCOP_IRQ3	Event generated by SIMCOP Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
14	SIMCOP_IRQ2	Event generated by SIMCOP Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
13	SIMCOP_IRQ1	Event generated by SIMCOP Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
12	SIMCOP_IRQ0	Event generated by SIMCOP Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
11	BTE_IRQ	Event generated by the burst translation engine Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
10	CBUFF_IRQ	Event generated by the circular buffer Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
9	CCP2_IRQ3	Event generated by the CCP2 receiver Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0

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Bits	Field Name	Description	Type	Reset
8	CCP2_IRQ2	Event generated by the CCP2 receiver Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
7	CCP2_IRQ1	Event generated by the CCP2 receiver Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
6	CCP2_IRQ0	Event generated by the CCP2 receiver Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
5	CSIB_IRQ	Event generated by the CSI2 receiver #b Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
4	CSIA_IRQ	Event generated by the CSI2 receiver #a Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
3	ISP_IRQ3	Combined interrupt event provided by the ISP. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
2	ISP_IRQ2	Combined interrupt event provided by the ISP. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
1	ISP_IRQ1	Combined interrupt event provided by the ISP. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
0	ISP_IRQ0	Combined interrupt event provided by the ISP. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0

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Table 8-26. Register Call Summary for Register ISS_HL_IRQENABLE_SET_i

ISS Overview

- ISS Interrupts: [0]
- ISS TOP Register Summary: [1]
- ISS TOP Register Description: [2] [3]

Table 8-27. ISS_HL_IRQENABLE_CLR_i

Address Offset	0x0000 002C + (0x10 * i)	**Index**	i = 0 to 5
Physical Address	0x5200 002C + (0x10 * i)	**Instance**	ISS_TOP
Description	Per-event interrupt enable bit vector Write 1 to clear (disable interrupt). Readout equal to corresponding _SET register.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														HS_VS_IRQ	CCP2_IRQ8	SIMCOP_IRQ3	SIMCOP_IRQ2	SIMCOP_IRQ1	SIMCOP_IRQ0	BTE_IRQ	CBUFF_IRQ	CCP2_IRQ3	CCP2_IRQ2	CCP2_IRQ1	CCP2_IRQ0	CSIB_IRQ	CSIA_IRQ	ISP_IRQ3	ISP_IRQ2	ISP_IRQ1	ISP_IRQ0

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17	HS_VS_IRQ	HS or VS synchronization event. This event is triggered if a rising or falling edge is detected on the HS or VS signal (after the video port mux). The rising or falling edge and the HS or VS signal selection is chosen with the ISS_CTRL.SYNC_DETECT bit field. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
16	CCP2_IRQ8	Event generated by the CCP2 receiver Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
15	SIMCOP_IRQ3	Event generated by SIMCOP Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
14	SIMCOP_IRQ2	Event generated by SIMCOP Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
13	SIMCOP_IRQ1	Event generated by SIMCOP Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
12	SIMCOP_IRQ0	Event generated by SIMCOP Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
11	BTE_IRQ	Event generated by the BTE Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
10	CBUFF_IRQ	Event generated by the CBUFF Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
9	CCP2_IRQ3	Event generated by the CCP2 receiver Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
8	CCP2_IRQ2	Event generated by the CCP2 receiver Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
7	CCP2_IRQ1	Event generated by the CCP2 receiver Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
6	CCP2_IRQ0	Event generated by the CCP2 receiver Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
5	CSIB_IRQ	Event generated by the CSI2 receiver b Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
4	CSIA_IRQ	Event generated by the CSI2 receiver a Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
3	ISP_IRQ3	Combined interrupt event provided by the ISP. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
2	ISP_IRQ2	Combined interrupt event provided by the ISP. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
1	ISP_IRQ1	Combined interrupt event provided by the ISP. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
0	ISP_IRQ0	Combined interrupt event provided by the ISP. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0

Table 8-28. Register Call Summary for Register ISS_HL_IRQENABLE_CLR_i

ISS Overview

- ISS Interrupts: [0]
- ISS TOP Register Summary: [1]

Table 8-29. ISS_CTRL

Address Offset	0x0000 0080		
Physical Address	0x5200 0080	**Instance**	ISS_TOP
Description	ISS control register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CSI2_B_TAG_CNT								CSI2_A_TAG_CNT								CCP2W_TAG_CNT								CCP2R_TAG_CNT							
RESERVED																										ISS_CLK_DIV		INPUT_SEL		SYNC_DETECT	

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Bits	Field Name	Description	Type	Reset
31:28	CSI2_B_TAG_CNT	Defines the maximum number of tags that could be used by the CSI2 b write bridge. Note: Tag count must be set to 16 for best performance.	RW	0x0
27:24	CSI2_A_TAG_CNT	Defines the maximum number of tags that could be used by the CSI2 a write bridge. Note: Tag count must be set to 16 for best performance.	RW	0x0
23:20	CCP2W_TAG_CNT	Defines the maximum number of tags that could be used by the CCP2 write bridge Note: Tag count must be set to 16 for best performance.	RW	0x0
19:16	CCP2R_TAG_CNT	Defines the maximum number of tags that could be used by the CCP2 read bridge Note: Tag count must be set to 16 for best performance.	RW	0x0
15:6	RESERVED		R	0x000
5:4	ISS_CLK_DIV	ISS functional clock division CLK refers to the input clock provided to the ISS. FCLK is the functional clock provided to ISS top level and submodules. CFGCLK is the clock used for the configuration network. 0x0: FCLK=CLK CFGCLK=CLK/2 0x1: FCLK=CLK/2 CFGCLK=CLK/4 0x3: Reserved 0x2: FCLK=CLK/4 CFGCLK=CLK/8	RW	0x0
3:2	INPUT_SEL	Selects ISP input 0x0: CSI2-A 0x1: CSI2-B 0x2: CCP2 0x3: Parallel interface	RW	0x0
1:0	SYNC_DETECT	Chooses among rising and falling edge for the HS_VS_IRQ synchronization event 0x0: HS falling edge 0x1: HS raising edge 0x3: VS raising edge 0x2: VS falling edge	RW	0x0

Table 8-30. Register Call Summary for Register ISS_CTRL

ISS Overview

- ISS Clock Domains: [0]
- ISS TOP Register Summary: [2]
- ISS TOP Register Description: [3] [4] [5] [6]

Table 8-31. ISS_CLKCTRL

Address Offset	0x0000 0084		
Physical Address	0x5200 0084	**Instance**	ISS_TOP
Description	ISS clock control register. Use to enable/disable the interface and functional clock of ISS submodules.		
Type	W		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VPORT3_CLK	VPORT2_CLK	VPORT1_CLK	VPORT0_CLK	RESERVED																							CCP2	CSI2_B	CSI2_A	ISP	SIMCOP

Bits	Field Name	Description	Type	Reset
31	VPORT3_CLK	Enables the pixel clock from the parallel interface 0x0: Disabled 0x1: Enabled	RW	1
30	VPORT2_CLK	Enables the pixel clock from the CCP2 protocol engine 0x0: Disabled 0x1: Enabled	RW	1
29	VPORT1_CLK	Enables the pixel clock from the CSI2_B protocol engine 0x0: Disabled 0x1: Enabled	RW	1
28	VPORT0_CLK	Enables the pixel clock from the CSI2_A protocol engine 0x0: Disabled 0x1: Enabled	RW	1
27:5	RESERVED		R	0x000000
4	CCP2	CCP2 Write 0x0: Request shutdown of the submodule. No effect if the submodule clock is already off. Write 0x1: Request enable of the submodule. No effect if the submodule clock is already off.	W	0
3	CSI2_B	CSI2_B Write 0x0: Request shutdown of the submodule. No effect if the submodule clock is already off. Write 0x1: Request enable of the submodule. No effect if the submodule clock is already off.	W	0
2	CSI2_A	CSI2_A Write 0x0: Request shutdown of the submodule. No effect if the submodule clock is already off. Write 0x1: Request enable of the submodule. No effect if the submodule clock is already off.	W	0
1	ISP	ISP Write 0x0: Request shutdown of the submodule. No effect if the submodule clock is already off. Write 0x1: Request enable of the submodule. No effect if the submodule clock is already off.	W	0
0	SIMCOP	SIMCOP Write 0x0: Request shutdown of the submodule. No effect if the submodule clock is already off. Write 0x1: Request enable of the submodule. No effect if the submodule clock is already off.	W	0

Table 8-32. Register Call Summary for Register ISS_CLKCTRL

ISS Overview

- ISS Clock Domains: [0] [1]
- ISS Clocks: [2] [3] [4] [5] [6] [7] [8] [9]
- ISS TOP Register Summary: [10]

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Table 8-33. ISS_CLKSTAT

Address Offset	0x0000 0088		
Physical Address	0x5200 0088	**Instance**	ISS_TOP
Description	ISS clock status register.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VPORT3_CLK	VPORT2_CLK	VPORT1_CLK	VPORT0_CLK	RESERVED																							CCP2	CSI2_B	CSI2_A	ISP	SIMCOP

Bits	Field Name	Description	Type	Reset
31	VPORT3_CLK	Status of the pixel clock from the parallel interface Read 0x1: Enabled Read 0x0: Disabled	R	1
30	VPORT2_CLK	Status of the pixel clock from the CCP2 protocol engine Read 0x1: Enabled Read 0x0: Disabled	R	1
29	VPORT1_CLK	Status of the pixel clock from the CSI2_B protocol engine Read 0x1: Enabled Read 0x0: Disabled	R	1
28	VPORT0_CLK	Status of the pixel clock from the CSI2_A protocol engine Read 0x1: Enabled Read 0x0: Disabled	R	1
27:5	RESERVED		R	0x000000
4	CCP2	CCP2 Read 0x1: The submodule is on. Read 0x0: The submodule is off.	R	0
3	CSI2_B	CSI2_B Read 0x1: The submodule is on. Read 0x0: The submodule is off.	R	0
2	CSI2_A	CSI2_A Read 0x1: The submodule is on. Read 0x0: The submodule is off.	R	0
1	ISP	ISP Read 0x1: The submodule is on. Read 0x0: The submodule is off.	R	0
0	SIMCOP	SIMCOP Read 0x1: The submodule is on. Read 0x0: The submodule is off.	R	0

Table 8-34. Register Call Summary for Register ISS_CLKSTAT

ISS Overview

- ISS Clocks: [0] [1] [2]
- ISS TOP Register Summary: [3]

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Table 8-35. ISS_PM_STATUS

Address Offset	0x0000 008C		
Physical Address	0x5200 008C	**Instance**	ISS_TOP
Description	ISS power manager status register. Software could know what modules are in functional or STANDBY/IDLE state. This feature could be particularly useful to debug when ISS does not go into STANDBY mode		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																		CBUFF_PM		BTE_PM		SIMCOP_PM		ISP_PM		CCP2_PM		CSI2_B_PM		CSI2_A_PM	

Bits	Field Name	Description	Type	Reset
31:14	RESERVED		R	0x00000
13:12	CBUFF_PM	Power status of the CBUFF. Read 0x2: Functional Read 0x1: Transition Read 0x0: Idle	R	0x0
11:10	BTE_PM	Power status of the BTE. Read 0x2: Functional Read 0x1: Transition Read 0x0: Idle	R	0x0
9:8	SIMCOP_PM	Power status of the SIMCOP. Read 0x2: Functional Read 0x1: Transition Read 0x0: Standby	R	0x0
7:6	ISP_PM	Power status of the ISP. Read 0x2: Functional Read 0x1: Transition Read 0x0: Standby	R	0x0
5:4	CCP2_PM	Power status of the CCP2. Read 0x2: Functional Read 0x1: Transition Read 0x0: Standby	R	0x0
3:2	CSI2_B_PM	Power status of the CSI2 module b Read 0x2: Functional Read 0x1: Transition Read 0x0: Standby	R	0x0
1:0	CSI2_A_PM	Power status of the CSI2 module a Read 0x2: Functional Read 0x1: Transition Read 0x0: Standby	R	0x0

Table 8-36. Register Call Summary for Register ISS_PM_STATUS

ISS Overview

- ISS TOP Register Summary: [0]

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8.2 ISS Interfaces

8.2.1 ISS Interfaces Overview

Along with the submodules, the ISS has two serial camera interfaces (primary and secondary) and a parallel interface. The primary serial interface (CSI2-A) supports MIPI® CSI2 protocol with four data lanes, and the secondary serial interface (CSI2-B/CCP2) supports CSI2 protocol with two data lanes or CCP2 protocol. The parallel interface (CPI) supports up to 16 data lanes. All interfaces can use the image signal processor (ISP), but not concurrently. When one interface uses the ISP, the other must send data to memory. However, the ISP can still be used to process this data in memory-to-memory. Time multiplex processing is also possible.

Figure 8-5 shows the ISS interfaces and interconnects.

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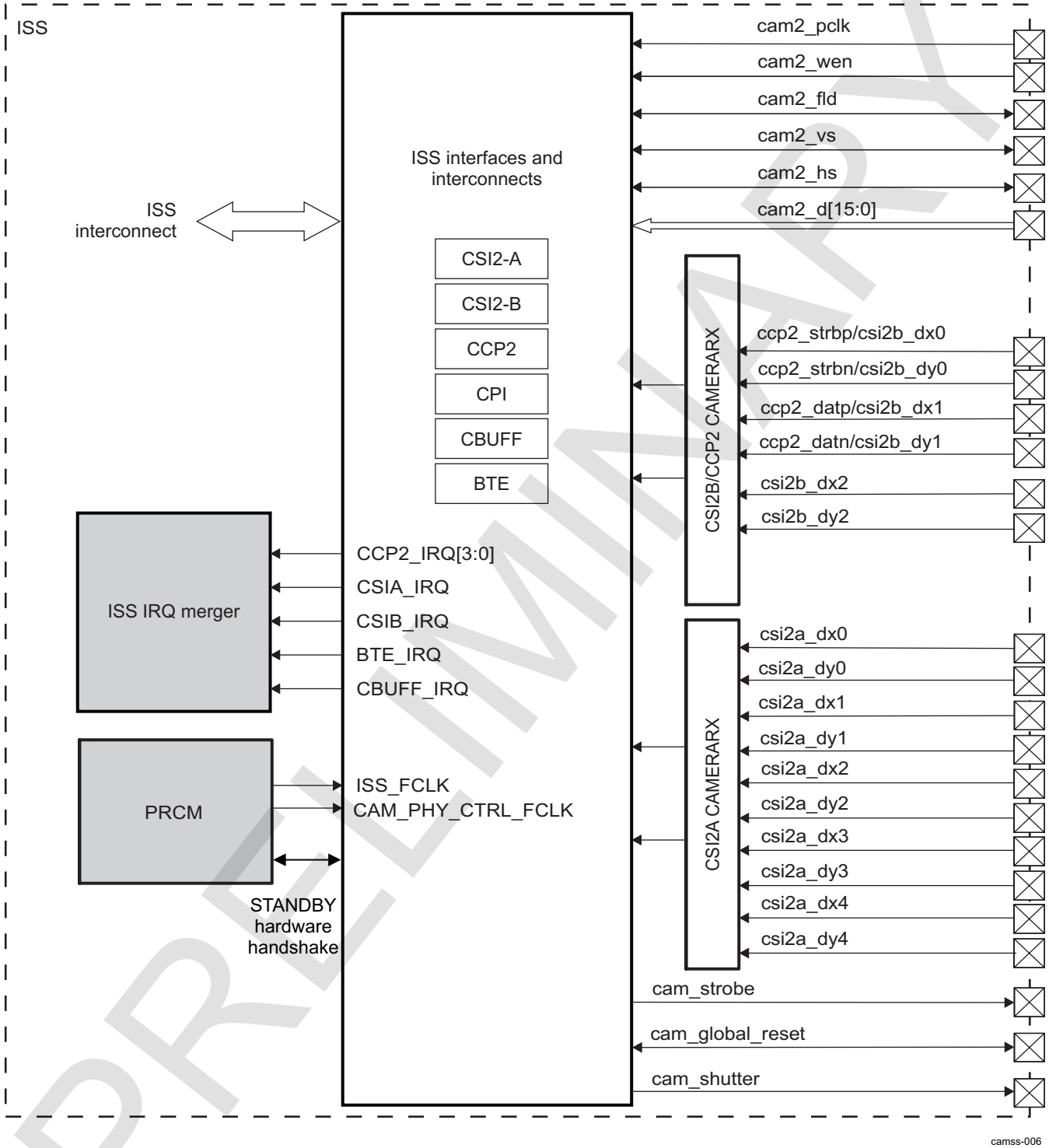
Figure 8-5. ISS Interfaces and Interconnects Highlight



NOTE: In the device, the number 2 in the cam2 interface name does not mean there are two camera parallel interfaces available in the device. The cam2 interface name defines the camera parallel interface available in the device versus the legacy device.

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8.2.1.1 ISS Interface Features

The camera subsystem supports the following features:

- System interfaces and interconnects:
  - Two 32-bit-wide configuration interfaces:
    - Interface to Cortex™-M3 microprocessor unit (MPU): Synchronous to the functional clock
    - Interface to Cortex™-A9 MPU and system direct memory access (sDMA): Asynchronous from the functional clock
  - 128-bit-wide data interface to level 3 (L3) interconnect: Asynchronous from the functional clock
    - Shared interface level 2 (L2) in IVA-HD module for hardware encoding
    - Outside connection using the L3 interconnect through the TILER to the synchronous dynamic random access memory (SDRAM) controller (SDRC), which acts as the primary interface between the SDRAM and the ISS functional block
  - The ISS has a local interconnect that connects all modules inside the ISS.
  - BTE:
    - Tightly coupled with the TILER to support efficient rotation
  - CBUFF:
    - Maps a linear space into a circular buffer
    - The buffer is physically located in system memory.
  - TCTRL:
    - Control signal generation for flash prestrobe and strobe
    - Camera global reset control
- Camera interfaces:
  - Two CSI2 camera interfaces: CSI2-A (primary) and CSI2-B (secondary)
    - Transfer pixels and data received by the CSI2 digital physical layer receiver to the system memory or to the ISP
    - Use unidirectional data link
    - CSI2-A supports four configurable data links in addition to the clock signaling.
    - CSI2-B supports two configurable data links in addition to the clock signaling.
    - Maximum data rate of 1 Gbps per data lane
    - Data merger for 2-, 3-, or 4-data lane configuration
    - Maximum data rate of 1 Gbps per data lane, possible configurations are:
      - One data lane: 1000 Mbps (824 Mbps if lane 4 is used)
      - Two data lanes: 2 × 1000 Mbps (2 × 824 Mbps if lane 4 is used
      - Three data lanes: 3 × 1000 Mbps (3 × 824 Mbps if lane 4 is used)
      - Four data lanes: 4 × 824 Mbps
    - Error detection and correction by the protocol engine
    - Direct memory access (DMA) engine integrated with dedicated first in first out (FIFO)
    - One-dimensional (1D) and two-dimensional (2D) addressing mode
    - Burst support
    - Streaming burst support (64- or 32-bit)
    - Eight contexts to support eight dedicated configurations of virtual channel ID and data types
    - Ping-pong mechanism for double-buffering
    - All primary and secondary MIPI-defined formats are supported.
    - Conversion of the RGB formats
    - On-the-fly differential pulse code modulation (DPCM) decompression
    - On-the-fly image cropping and A-law/DPCM compression

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- Configuration of the complex input/output (I/O) physical layer (PHY) (MIPI D-PHY-compliant receiver PHY solution [D-PHY mode]/CCP2-compatible receiver PHY solution (CCP2 mode)

– CCP2 camera interface (secondary)
  - Four logical channels
  - Transfer pixels and data received by the complex I/O PHY (CCP2 D-PHY RX to the system memory or the ISP)
  - Use unidirectional data link
  - Maximum data rate of 650 Mbps
  - DMA engine integrated with dedicated FIFO
  - 1D and 2D addressing mode
  - False synchronization code protection
  - Ping-pong mechanism for double-buffering
  - RGB, RAW, YUV, and JPEG formats supported
  - On-the-fly DPCM decompression
  - On-the-fly image cropping and A-Law/DPCM compression
– Parallel interface (CPI)
  - 16 bits wide
  - up to 148.5 MPix/s
  - BT656 and SYNC mode (HS, VS, FIELD, WEN)
– System memory data read back port (supported by the CCP2 protocol engine)
  - RAW 6, 7, 8, 10, 12, 14, 16 formats supported
  - DPCM and A-law decompression
  - Supports image cropping for compressed or uncompressed data

NOTE: Rotated DPCM data is not supported.

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8.2.2 ISS Interfaces Environment

8.2.2.1 ISS Interfaces Signal Descriptions

Table 8-37 summarizes the I/O signals.

Table 8-37. ISS I/O Description

Signal Name	I/O [1]	Description	Serial Mode CCP2	Serial Mode CSI2	Parallel Mode CPI
cam_strobe	O	Flash strobe control signal	x	x	
cam_shutter	O	Mechanical shutter control signal	x	x	
cam_global_reset	I/O	Global reset release shutter signal	x	x	
csi2a_dx0	I	Serial CSI2-A mode: Differential clock positive input		x	
csi2a_dy0	I	Serial CSI2-A mode: Differential clock negative input		x	
csi2a_dx1	I	Serial CSI2-A mode: Differential data lane positive input		x	
csi2a_dy1	I	Serial CSI2-A mode: Differential data lane negative input		x	
csi2a_dx2	I	Serial CSI2-A mode: Differential data lane positive input		x	
csi2a_dy2	I	Serial CSI2-A mode: Differential data lane negative input		x	
csi2a_dx3	I	Serial CSI2-A mode: Differential data lane positive input		x	
csi2a_dy3	I	Serial CSI2-A mode: Differential data lane negative input		x	
csi2a_dx4	I	Serial CSI2-A mode: Differential data lane positive input		x	
csi2a_dy4	I	Serial CSI2-A mode: Differential data lane negative input		x	
csi2b_dx0	I	Serial CSI2-B mode: Differential clock lane positive input		x	
csi2b_dy0	I	Serial CSI2-B mode: Differential clock lane negative input		x	
csi2b_dx1	I	Serial CSI2-B mode: Differential data lane positive input		x	
csi2b_dy1	I	Serial CSI2-B mode: Differential data lane negative input		x	
csi2b_dx2	I	Serial CSI2-B mode: Differential data lane positive input		x	

[1] I = Input; O = Output

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Table 8-37. ISS I/O Description (continued)

Signal Name	I/O [1]	Description	Serial Mode CCP2	Serial Mode CSI2	Parallel Mode CPI
csi2b_dy2	I	Serial CSI2-B mode: Differential data lane negative input		x	
ccp2_strbp	I	Serial CCP2 mode: Differential clock positive input	x		
ccp2_strbn	I	Serial CCP2 mode: Differential clock negative input	x		
ccp2_datp	I	Serial CCP2 mode: Differential data positive input	x		
ccp2_datn	I	Serial CCP2 mode: Differential data negative input	x		
cam2_pclk	I	Parallel mode pixel clock input			x
cam2_wen	I	Parallel mode write enable signal input			x
cam2_fld	I/O	Parallel mode pixel clock field signal			x
cam2_vs	I/O	Parallel mode vertical frame synchronization			x
cam2_hs	I/O	Parallel mode horizontal frame synchronization			x
cam2_d[15:0]	I	Parallel mode data lanes (16 signals)			x

NOTE: Lane polarity can be changed in complex I/O. For more information, see Section 8.2.2.2, *ISS Interface Modes*.

NOTE: At least one data lane must be configured for using the CSI2-A and CSI2-B interfaces. The signals are also configurable from the control module. Thus, they are not required to be at a certain location to act as clock or data; this can be configured.

NOTE: The Parallel interface (CPI), CCP2, and CSI2-B share pins. Their modes are not supported as a pin configuration mux option. The modes are configured from the CSI2-B/CCP2 CAMERARX configured from the system control module (see Chapter 18, *Control Module*).

8.2.2.2 ISS Interfaces Modes

The camera subsystem can manage a parallel interface and two serial image sensors. Depending on the configuration of the shared pins, two of the interfaces can be active at the same time. However, only one data flow can use the ISP. Moreover, if the parallel interface is used data from it goes to ISP and the other used interface must send it to memory. Figure 8-6 shows an example block diagram of the interface configuration. Each serial port clock lane is configurable. The MIPI CSI2 protocol requires only a clock lane setup. The data lane configuration is optional. For more information, see Section 8.2.5.1.1, *ISS CSI2 Protocol and Data Format*.

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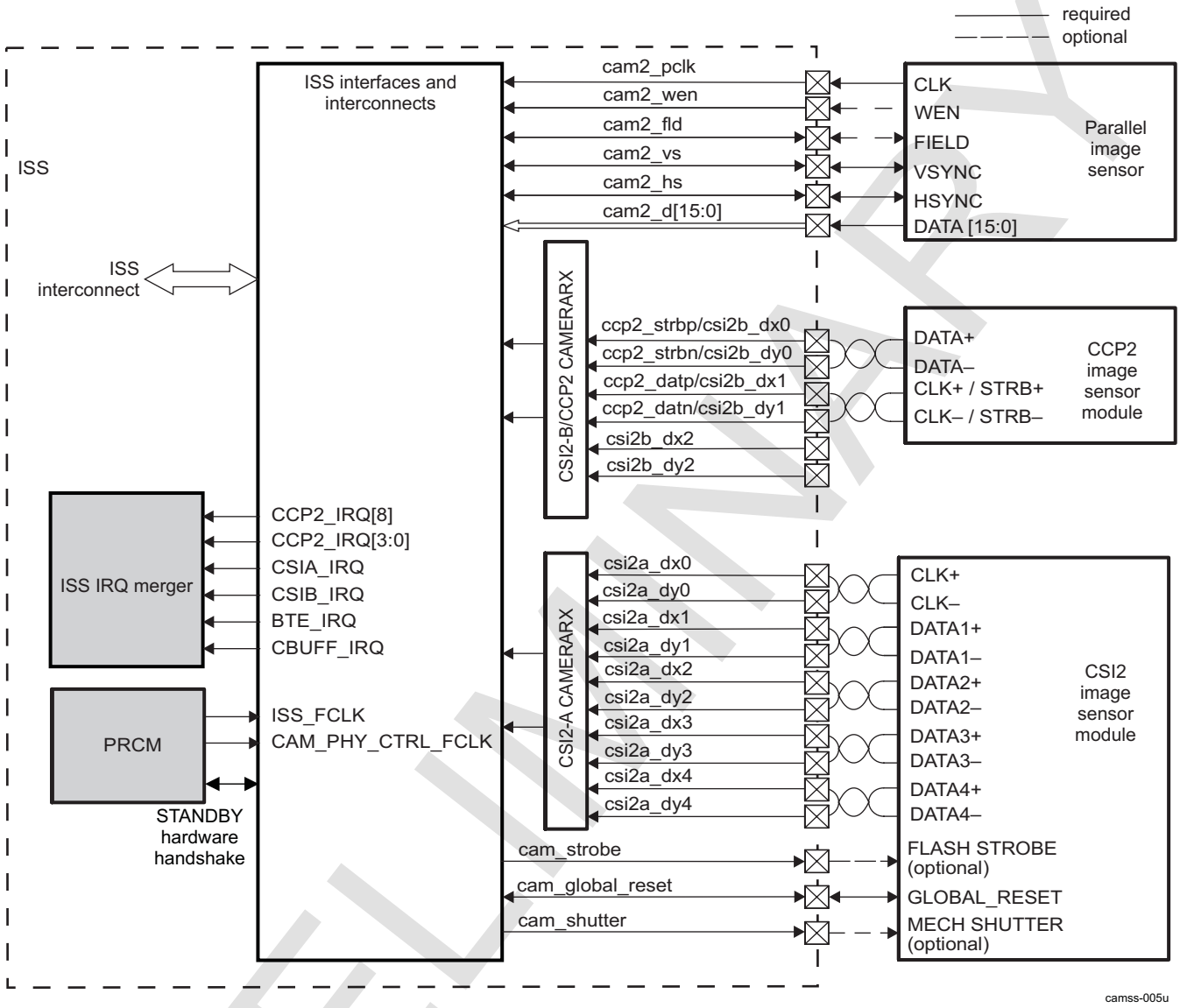
Figure 8-6. ISS CSI2-A, CSI2-B/CCP2 Serial Interface Configuration



NOTE: Depending on the needs, cam_strobe, cam_global_reset, and cam_shutter can be connected to the image sensor module rather than the CSI2 image sensor module.

NOTE: Dedicated power, reset, and clock management (PRCM) module pins for power and ground are provided for external sensors: vdda_csi2a, vdda_csi2b, vssa_csi2a, and vssa_csi2b.

A graphical representation of the pins for connecting external sensors to the ISS shows a variety of connectivity configurations that are possible by setting the PHY immediately before the receivers, and a variety of output paths, including some sensor data through the receivers to memory or the ISP. Table 8-38 lists some of the connectivity possibilities; the ISP can take only one input lane at a time. For more information about the operating properties and configuration of the CAMERARX PHY, see Section 8.2.3, *ISS CSI2 PHY*.

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Table 8-38. ISS Interfaces Connectivity Scheme Example Scenarios

CSI2-A	On, 4DL CSI2-A(1) to ISP	On, 2DL CSI2-A(2) to Memory	Off	On, 2DL CSI2-A(2) to memory	On, 3DL CSI2-A(2) to ISP/memory	Off	Off
CCP2	Off	Off	On, 1DL CCP2(1) to Memory	On, 1DL CCP2(1) to ISP	Off	On, 1DL CCP2(1) to memory	Off
CSI2-B	On, 2DL CSI2-B (1) to memory	Off	Off	Off	On, 2DL CSI2-B(1) to memory/ISP	Off	On, 2DL CSI2-B(1) to memory
Parallel interface (CPI) up to 16 lanes	Off	On, 16 data lanes(1) to ISP	On, 12 data lanes(2) to ISP	Off	Off	Off	Off
Signal	Simultaneous	Simultaneous	Simultaneous	Simultaneous	Simultaneous	Simultaneous	Simultaneous
cam_strobe	x	x	x	x	x	x	x
cam_global_reset	x	x	x	x	x	x	x
cam_shutter	x	x	x	x	x	x	x
csi2a_dx0	x	x		x	x		
csi2a_dy0	x	x		x	x		
csi2a_dx1	x	x		x	x		
csi2a_dy1	x	x		x	x		
csi2a_dx2	x	x		x	x		
csi2a_dy2	x	x		x	x		
csi2a_dx3	x				x		
csi2a_dy3	x				x		
csi2a_dx4	x						
csi2a_dy4	x						
csi2b_dx0/ccp2_strbp	x		x	x	x	x	x
csi2b_dy0/ccp2_strbn	x		x	x	x	x	x
csi2b_dx1/ccp2_datp	x		x	x	x	x	x
csi2b_dy1/ccp2_datn	x		x	x	x	x	x
csi2b_dx2	x				x		x
csi2b_dy2	x				x		x
cam2_pclk		x	x				
cam2_wen		x	x				
cam2_fld		x	x				
cam2_vs		x	x				
cam2_hs		x	x				
cam2_d[15:0]		x	x				

(1) Full: All data/clock lanes are connected.
(2) Limited: Some data/clock lanes are connected.

NOTE: The ISP can take only one input at a time. The other inputs must go to memory and then be processed after the ISP processes the input that was received first.

In looking at the sample connections between the ISS through the receivers and external sensors, it is

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apparent that the lanes of the input can be adjusted for certain needs. For example, it is not necessary that the CSI2-A has four data lanes connected at the same time. The restriction is that CSI2-B is limited to two data lanes. Because CSI2-B and CCP2 share pins, they cannot be used simultaneously. CSI2-A and CSI2-B/CCP2 can function at the same time by sending data to memory. In this manner, external sensors can be connected any way possible for best performance and results.

8.2.2.3 ISS Interfaces CPI Data Formats

8.2.2.3.1 ISS Interfaces CPI Generic Configuration Protocol and Data Format (8, 10, 12, 16 Bits)

The SYNC mode implements a generic parallel interface with the image sensor. The SYNC mode supports 8- to 16-bit-wide data signals.

In this configuration, no assumptions are made about the data format of pixels, but the dynamic range is limited to 8, 10, 12, and 16 bits (data can be pure Luminance for black and white sensor, RGB444, Bayer RGB, etc.). The pixel data is presented on cam2_d, where 1 pixel is sampled for every cam2_pclk rising edge (or falling edge, depending on the configuration of cam2_pclk polarity).

Additional pixel times between rows represent blanking periods. Active pixels are identified by a combination of two additional timing signals: horizontal synchronization (cam2_hs) and vertical synchronization (cam2_vs). During the image-sensor readout, these signals define when a row of valid data begins and ends, and when a frame starts and ends.

NOTE: For correct operation, the clock cam2_pclk must run during blanking periods (cam2_hs and cam2_vs inactive). cam2_pclk must start before sending cam2_d and start cam2_vs and cam2_hs.

Figure 8-7 and Figure 8-8 show the frame and data timing, based on synchronization signals in the parallel No BT configuration.

Figure 8-7. ISS Interfaces CPI Synchronization Signals and Frame Timing in SYNC Mode

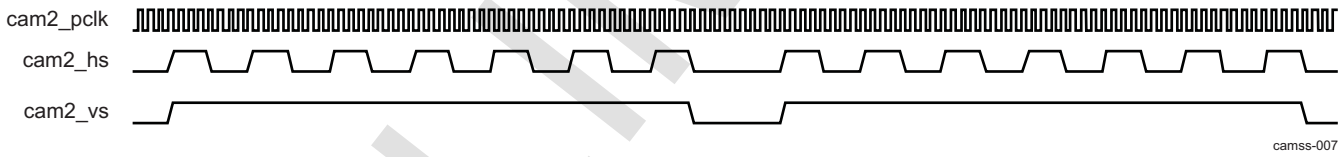
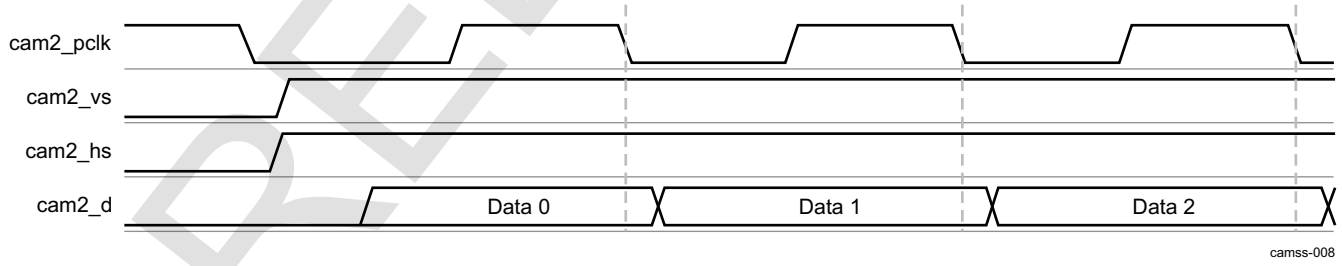


Figure 8-8. ISS Interfaces CPI Synchronization Signals and Data Timing in SYNC Mode



NOTE: The pixel clock can be gated to qualify valid pixels. It can also be gated during blanking periods to reduce power consumption. However, at least four clock pulses are required before sending active image data and synchronization information; eight clock pulses are required after the end of active video. Extra-clock pulses are allowed but not required during the line blanking periods.

Figure 8-9 shows the timing diagram of the SYNC move clock gating.

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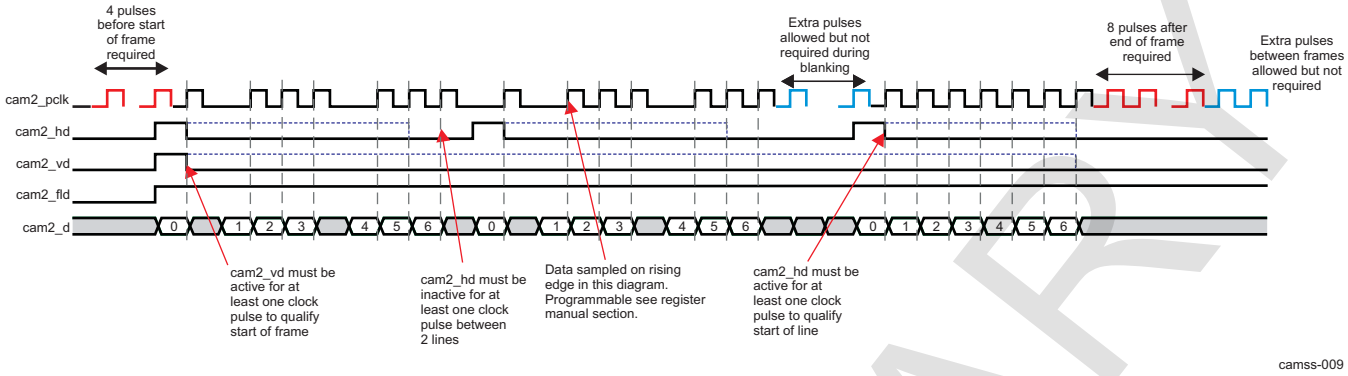
Figure 8-9. ISS Interfaces CPI SYNC Mode Clock Gating

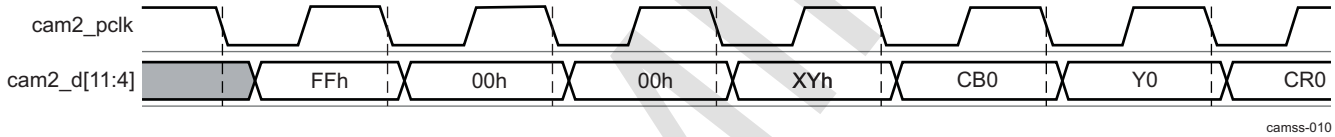


8.2.2.3.2 ISS Interfaces CPI ITU-R BT.656/1120 422 Protocol and Data Formats (8, 10 Bits)

The ISS CPI supports data in ITU-R BT.656 format. The ITU-R BT.656 standard specifies a method of transferring YUV4:2:2 data over an 8- or 10-bit video interface.

Figure 8-10 shows the data timing diagram with embedded synchronization signals.

Figure 8-10. ISS Interfaces CPI Data Timing With Embedded Synchronization Signals (8-Bit Case)



In BT.656, the data words (8- or 10-bit) in which the 8 most-significant bits (MSBs) are all set to 1, or all set to 0, are reserved.

NOTE: The ITU-R BT.656 specification is for 525-line and 625-line, digital component video signals in compliance with ITU-R BT.601. See the CCIR document Rec. 656-1 for detailed information about the interface.

The data is multiplexed in the following order: Cb0 Y0 Cr0 Y1 Cb2 Y2 Cr2 Y3, etc., where the byte sequence Cb2n Y2n Cr2n refers to interleaved Luminance and Chroma samples and the following byte Y2n + 1 corresponds to the next Luminance sample.

The BT.656 protocol uses unique timing reference signals embedded in the video stream. The synchronization signals cam2_hs and cam2_vs are not needed. This reduces the number of wires required for a BT.656 video interface.

There are two timing reference codes: The start of active video (SAV) reference code precedes each video data block, and the end of active video (EAV) follows each video data block. Each timing reference signal consists of a 4-byte sequence in the following hexadecimal format: FF 00 00 XY. The first 3 bytes are a fixed preamble (see the ITU-R BT.656 specification). The fourth byte (XY) contains information defining field identification (F), blanking (V), and SAV/EAV information (H), and 4 parity bits calculated as a function of F, V, and H (see the ITU-R BT.656 specification).

Table 8-39 lists the video timing reference codes for SAV and EAV.

Table 8-39. ISS Interfaces CPI Video Timing Reference Codes for SAV and EAV

Data Bit Number	First Word (FF)	Second Word (00)	Third Word (00)	Fourth Word (XY)
9 (MSB)	1	0	0	1
8	1	0	0	F
7	1	0	0	V
6	1	0	0	H

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Table 8-39. ISS Interfaces CPI Video Timing Reference Codes for SAV and EAV (continued)

Data Bit Number	First Word (FF)	Second Word (00)	Third Word (00)	Fourth Word (XY)
5	1	0	0	P3
4	1	0	0	P2
3	1	0	0	P1
2	1	0	0	P0
1	1	0	0	0
0	1	0	0	0

Table 8-40 describes the F, V, and H signals.

Table 8-40. ISS Interfaces CPI F, V, H Signal Descriptions

Signal	Value	Command
F	0	Field 1
	1	Field 2
V	0	0
	1	Vertical blank
H	0	SAV
	1	EAV

The resulting Hamming distance between any two code words is four, allowing two error detections and one error correction. To enable or disable the error-correcting capability, configure the ISIF_REC656IF[0] ECCFVH bit.

NOTE: The 2-bit errors are detected, but not flagged or corrected. Errors of more than 2 bits are not corrected or flagged.

Table 8-41 lists the F, V, and H protection (error-correction) bits.

Table 8-41. ISS Interfaces CPI F, V, H Protection (Error-Correction) Bits

F	V	H	P3	P2	P1	P0
0	0	0	0	0	0	0
0	0	1	1	1	0	1
0	1	0	1	0	1	1
0	1	1	0	1	1	0
1	0	0	0	1	1	1
1	0	1	1	0	1	0
1	1	0	1	1	0	0
1	1	1	0	0	0	1

When operating in ITU-R BT.656 mode, data is stored in SDRAM according to the format listed in Table 8-42 when the ISIF_REC656IF[1] R656ON bit is enabled.

Table 8-42. ISS Interfaces CPI ITU-R BT.656 Mode Data Format in SDRAM

b31			b0
Pixel3 (Y1)	Pixel2 (Cr0)	Pixel1 (Y0)	Pixel0 (Cb0)

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8.2.3 ISS CSI2 PHY

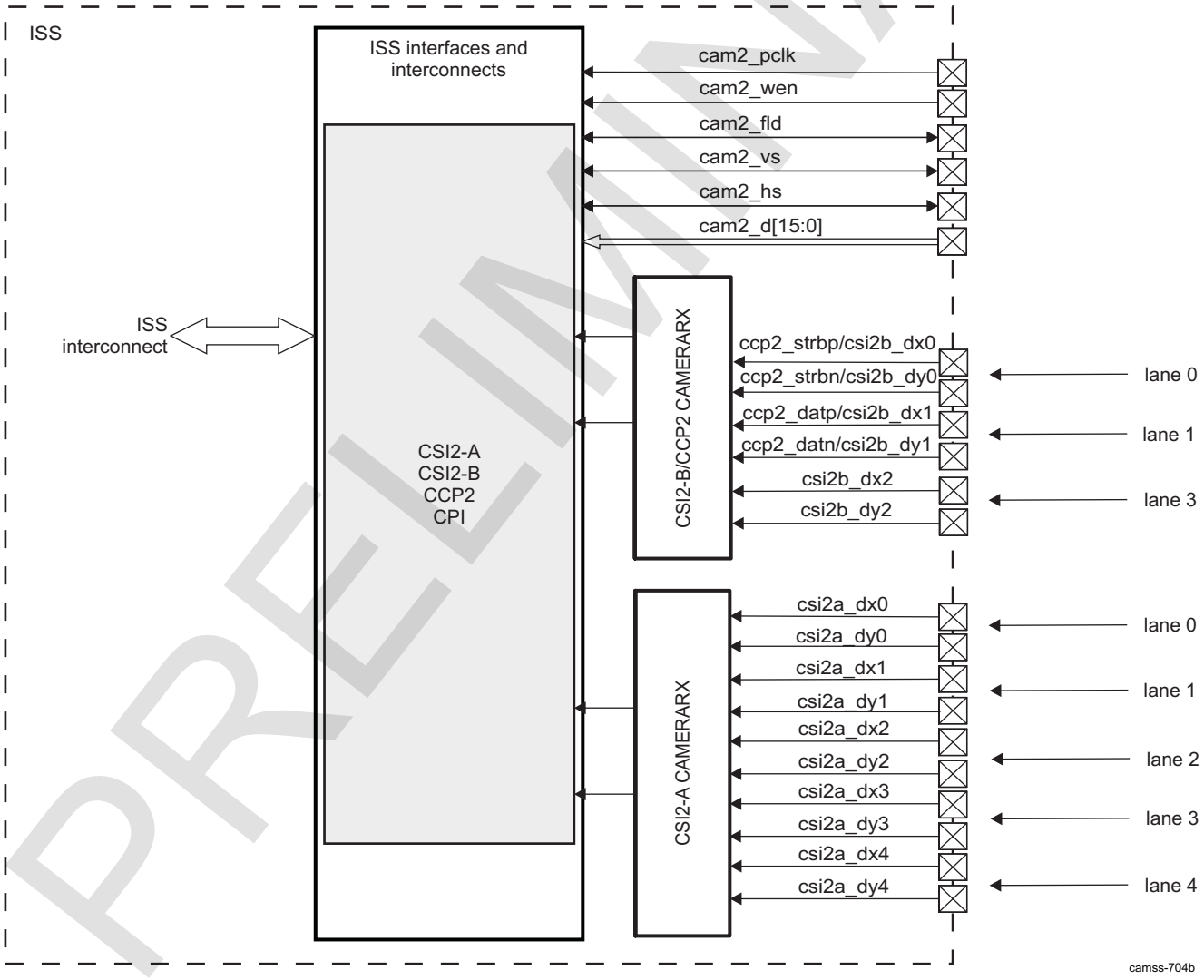
8.2.3.1 ISS CSI2 PHY Overview

Two MIPI D-PHY-compliant CAMERARX PHY receivers immediately before the ISS interfaces act as a physical connection and configuration of clock/data lanes with external sensors. CAMERARX PHY supports up to four configurations, depending on the required number of D-PHY data lane external sensors. The receivers are compatible with the *MIPI D-PHY Specification v0.92*. The selection of CAMERARX in D-PHY mode, parallel mode, or CCP2 mode must be done before reset and not on the fly.

The PHY is controlled and must be configured first from the control module for pad configuration. The differential data/clock lanes coming into the CSI2-A and CSI2-B CAMERARX are configured from registers explained inSection 18.4.8.4 (see register CONTROL_CAMERA_RX).

As mentioned previously, two PHYs are integrated in the device. The CSI2-A CAMERARX contains four data lanes, as shown in Figure 8-11; CSI2-B is the same except that it has two data lanes plus a clock/strobe lane. The figure also shows case CSI2-A, with four data lanes and one clock, listed in Table 8-38.

Figure 8-11. ISS Interfaces CSI2-A PHY Diagram Four D-PHY Data Lane Configuration



NOTE: If CCP2 mode is chosen for use in the CSI2-B/CCP2 CAMERARX, then LANE 0 and LANE 1 are used only as datp/datn and strbp/strbn.

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NOTE: LANE 4 can be used only as a data lane, never as a clock lane. All other configurations are possible. Also, a speed restriction is present when lane 4 is used; then all data lanes perform at up to 824 Mbps instead of 1000 Mbps.

NOTE: Depending on the selected mux mode form the Control Module, the Parralel interface (CPI) signals can also be going through one of the CAMERARXs

CSI2-A and CSI2-B/CCP2 CAMERARX represent the overall PHY solution for connecting external sensors to feed the ISS. The MIPI D-PHY function can support up to four data lane modules and one clock lane module. Reverse direction escape mode is not supported. The lane module polarity and positions are configurable; that is, any lane module can be chosen as the clock lane module, and the DX/DY data pad for each lane module can be configured as DP or DN pins defined. The configuration and the selection of D-PHY mode, data/clock, or data/strobes are done through the control module (see Chapter 18, *Control Module*). The only exception is the four-data-lane use case, in which one corner lane is allowed to be only a data lane. For the CCP2 function, the CAMERARX PHY solution supports one data/strobe or data/clock lane module. The data lane module and strobe lane module must be physically adjacent. CAMERARX supports serial configuration protocol for the configuration interface.

8.2.3.2 ISS CSI2 PHY Functional Description

8.2.3.2.1 ISS CSI2 PHY Functional Configuration

The CSI2 PHY converts the bitstream, divided into 1 to 4 serial data lanes, into a bitstream compatible with the CSI2 receiver and one clock lane.

The CSI2_COMPLEXIO_IRQSTATUS register logs complex I/O events of the following types:

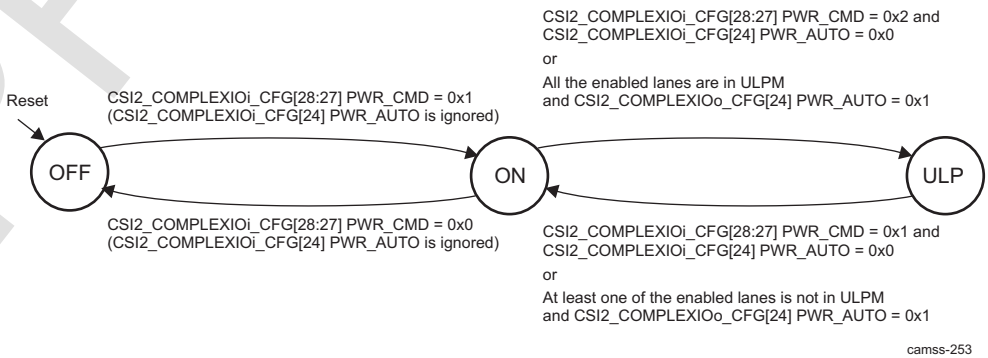
- Line power-state change (all lanes in ultralow-power mode [ULPM], at least one lane exits ULPM, etc.)
- Error on one lane

The CSI2 receiver embeds two registers to configure/read some complex I/O parameters:

- The REGISTER0 register detects clock miss with respect to the *MIPI D-PHY Specification v0.92* and control timing.
- The REGISTER0 register reports completion of reset on the different parts of the module and configures the timing parameters.
- The CSI2_COMPLEXIO_CFG registers contain the PWR_AUTO and PWR_CMD bit fields, which affect the power management of the two complex I/Os.

The complex I/O has three power modes: on, off, and ultralow power (ULP). These modes can reflect the ON or ULP states of the five differential lines if the CSI2_COMPLEXIO_CFG[24] PWR_AUTO bit is set to 1. If the PWR_AUTO bit is at reset value (0), the complex I/O power state is controlled by the CSI2_COMPLEXIO_CFG[28:27] PWR_CMD bit field, which directly defines the power state. Figure 8-12 shows the complex I/O power finite state-machine (FSM).

Figure 8-12. ISS CSI2 Complex I/O Power FSM



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Another register, CSI2_TIMING, is used to control the power state of the complex I/O modules with regard to the differential line state. This register controls the mode of the two complex I/Os (RxMode and NoRxMode) and the delay between the differential lanes in STOP state and the complex I/O on NoRxMode. The CSI2_TIMING[15] FORCE_RX_MODE_IO1 bit sets the complex I/O in RxMode or NoRxMode (stopped mode). The FORCE_RX_MODE_IO bit is automatically reset to 0 by hardware when the counter ends and the FSM returns to NoRxMode. Three bits (CSI2_TIMING[14] STOP_STATE_X16_IO1, CSI2_TIMING[13] STOP_STATE_X4_IO1, and the CSI2_TIMING[12:0] STOP_STATE_COUNTER_IO1 bit field) configure the delay between line stop mode and complex I/O stop mode. The delay represents the number of functional clock (ISS_FCLK) cycles and can be calculated as follows:

Total delay in ISS_FCLK cycle = CSI2_TIMING.STOP_STATE_COUNTER_IO x (1+CSI2_TIMING.STOP_STATE_X16_IO x 15) x (1+CSI2_TIMING.STOP_STATE_X4_IO x 3).

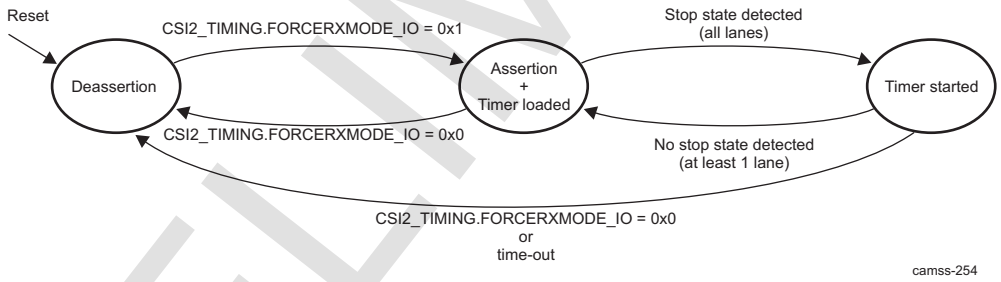
Table 8-43 lists the possible values of the delay, in terms of the ISS_FCLK cycles, depending on the values of the STOP_STATE_X16_IO and STOP_STATE_X4_IO bits.

Table 8-43. ISS CSI2 Possible Time-Out Value for RxMode Counter

STOP_STATE_X16_IO	STOP_STATE_X4_IO	Possible Delay Value (in Functional Clock Cycles)
0x0	0x0	8191 (with step of 1)
0x0	0x1	32764 (with step of 4)
0x1	0x0	131056 (with step of 16)
0x1	0x1	524224 (with step of 64)

The FORCERXMODE signal is used at initialization time (complex I/O). Figure 8-13 describes the ForceRxMode and StopState FSM to assert and deassert the FORCERXMODE signal and to monitor STOPSTATE from the complex I/O.

Figure 8-13. ISS CSI2 RxMode and StopState FSM



8.2.3.2.2 ISS CSI2 PHY and Link Initialization Sequence

The MIPI D-PHY initialization sequence is not implemented within CAMERARX. The CSI2-A receiver is expected to coordinate the PHY initialization. The controller must ensure that the PHY is held in RESET/WAIT for RX mode until the D-PHY transmitter is powered up and the link comes to the defined state. The controller can use the STOPSTATE and FORCERXMODE signals of CAMERARX for this purpose. STOPSTATE indicates the line states, while FORCERXMODE forces the receiver state-machine into "wait for stop state." One possible initialization sequence is:

To fully initialize the CSIPHY, perform the following steps:

1. Configure all CSI2 receiver registers to be ready to receive signals/data from the CSIPHY:
   (a) Configure all needed CSI2 registers:
      (i) Set CSI2_COMPLEXIO_CFG[18:16] DATA4_POSITION.
      (ii) Set CSI2_COMPLEXIO_CFG[14:12] DATA3_POSITION.
      (iii) Set CSI2_COMPLEXIO_CFG[10:8] DATA2_POSITION.
      (iv) Set CSI2_COMPLEXIO_CFG[6:4] DATA1_POSITION.
      (v) Set CSI2_COMPLEXIO_CFG[2:0] CLOCK_POSITION.

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(vi) Set the CONTROL_CAMERA_RX[20:19] CAMERARX_CSI22_CAMMODE or CONTROL_CAMERA_RX[17:16] CAMERARX_CSI21_CAMMODE.

CAUTION

This must be done before the CSIPHY is active.

2. CSIPHY and link initialization sequence:

(a) Deassert the CSIPHY reset.

(i) Set CSI2_COMPLEXIO_CFG[30] RESET_CTRL to 0x1.

CAUTION

For the CSI2_COMPLEXIO_CFG[29] RESET_DONE bit to be set to 0x1 (reset completed), the external sensor must to be active and sending the MIPI HS BYTECLK.

The following registers can be set only after deasserting the CSIPHY reset and before asserting the FORCERXMODE signal:

- REGISTER0
- REGISTER1
- REGISTER2

(b) Assert the FORCERXMODE signal:

(i) Set CSI2_TIMING[15] FORCE_RX_MODE_IO1 to 0x1.

(c) Connect pulldown on link (DP/DN) by asserting the respective PIPD* signals (PIPD* = 0):

For CSI2-A CAMERARX pulldown on signals through padconf registers:

- csi21_dx4:
  - CONTROL_CORE_PAD0_CSI21_DX4_PAD1_CSI21_DY4[8] CSI21_DX4_INPUTENABLE = 0x1
  - CONTROL_CORE_PAD0_CSI21_DX4_PAD1_CSI21_DY4[4] CSI21_DX4_PULLTYPESELECT = 0x0
  - CONTROL_CORE_PAD0_CSI21_DX4_PAD1_CSI21_DY4[3] CSI21_DX4_PULLUDENABLE = 0x1
- csi21_dy4:
  - CONTROL_CORE_PAD0_CSI21_DX4_PAD1_CSI21_DY4[24] CSI21_DY4_INPUTENABLE = 0x1
  - CONTROL_CORE_PAD0_CSI21_DX4_PAD1_CSI21_DY4[20] CSI21_DY4_PULLTYPESELECT = 0x0
  - CONTROL_CORE_PAD0_CSI21_DX4_PAD1_CSI21_DY4[19] CSI21_DY4_PULLUDENABLE = 0x1
- csi21_dx3:
  - CONTROL_CORE_PAD0_CSI21_DX3_PAD1_CSI21_DY3[8] CSI21_DX3_INPUTENABLE = 0x1
  - CONTROL_CORE_PAD0_CSI21_DX3_PAD1_CSI21_DY3[4] CSI21_DX3_PULLTYPESELECT= 0x0
  - CONTROL_CORE_PAD0_CSI21_DX3_PAD1_CSI21_DY3[3] CSI21_DX3_PULLUDENABLE = 0x1
- csi21_dy3:
  - CONTROL_CORE_PAD0_CSI21_DX3_PAD1_CSI21_DY3[24] CSI21_DY3_INPUTENABLE = 0x1

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  - CONTROL_CORE_PAD0_CSI21_DX3_PAD1_CSI21_DY3[20] CSI21_DY3_PULLTYPESELECT= 0x0
  - CONTROL_CORE_PAD0_CSI21_DX3_PAD1_CSI21_DY3[19] CSI21_DY3_PULLUDENABLE = 0x1
- csi21_dx2:
  - CONTROL_CORE_PAD0_CSI21_DX2_PAD1_CSI21_DY2[8] CSI21_DX2_INPUTENABLE = 0x1
  - CONTROL_CORE_PAD0_CSI21_DX2_PAD1_CSI21_DY2[4] CSI21_DX2_PULLTYPESELECT= 0x0
  - CONTROL_CORE_PAD0_CSI21_DX2_PAD1_CSI21_DY2[3] CSI21_DX2_PULLUDENABLE = 0x1
- csi21_dy2:
  - CONTROL_CORE_PAD0_CSI21_DX2_PAD1_CSI21_DY2[24] CSI21_DY2_INPUTENABLE = 0x1
  - CONTROL_CORE_PAD0_CSI21_DX2_PAD1_CSI21_DY2[20] CSI21_DY2_PULLTYPESELECT= 0x0
  - CONTROL_CORE_PAD0_CSI21_DX2_PAD1_CSI21_DY3[19] CSI21_DY2_PULLUDENABLE = 0x1
- csi21_dx1:
  - CONTROL_CORE_PAD0_CSI21_DX1_PAD1_CSI21_DY1[8] CSI21_DX1_INPUTENABLE = 0x1
  - CONTROL_CORE_PAD0_CSI21_DX1_PAD1_CSI21_DY1[4] CSI21_DX1_PULLTYPESELECT= 0x0
  - CONTROL_CORE_PAD0_CSI21_DX1_PAD1_CSI21_DY1[3] CSI21_DX1_PULLUDENABLE = 0x1
- csi21_dy1:
  - CONTROL_CORE_PAD0_CSI21_DX1_PAD1_CSI21_DY1[24] CSI21_DY1_INPUTENABLE = 0x1
  - CONTROL_CORE_PAD0_CSI21_DX1_PAD1_CSI21_DY1[20] CSI21_DY1_PULLTYPESELECT= 0x0
  - CONTROL_CORE_PAD0_CSI21_DX1_PAD1_CSI21_DY1[19] CSI21_DY1_PULLUDENABLE = 0x1
- csi21_dx0:
  - CONTROL_CORE_PAD0_CSI21_DX0_PAD1_CSI21_DY0[8] CSI21_DX0_INPUTENABLE = 0x1
  - CONTROL_CORE_PAD0_CSI21_DX0_PAD1_CSI21_DY0[4] CSI21_DX0_PULLTYPESELECT= 0x0
  - CONTROL_CORE_PAD0_CSI21_DX0_PAD1_CSI21_DY0[3] CSI21_DX0_PULLUDENABLE = 0x1
- csi21_dy0:
  - CONTROL_CORE_PAD0_CSI21_DX0_PAD1_CSI21_DY0[24] CSI21_DY0_INPUTENABLE = 0x1
  - CONTROL_CORE_PAD0_CSI21_DX0_PAD1_CSI21_DY0[20] CSI21_DY0_PULLTYPESELECT= 0x0
  - CONTROL_CORE_PAD0_CSI21_DX0_PAD1_CSI21_DY0[19] CSI21_DY0_PULLUDENABLE = 0x1

For CSI2-B/CCP2 CAMERARX pulldown on signals through padconf registers:

- csi22_dx2:
  - CONTROL_CORE_PAD0_DPM_EMU19_PAD1_CSI22_DX2[24] CSI22_DX1_INPUTENABLE = 0x1
  - CONTROL_CORE_PAD0_DPM_EMU19_PAD1_CSI22_DX2[20]

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CSI22_DX1_PULLTYPESELECT = 0x0

– CONTROL_CORE_PAD0_DPM_EMU19_PAD1_CSI22_DX2[19] CSI22_DX1_PULLUDENABLE = 0x1

- csi22_dy2:
  - CONTROL_CORE_PAD0_CSI22_DY2[8] CSI22_DY1_INPUTENABLE = 0x1
  - CONTROL_CORE_PAD0_CSI22_DY2[4] CSI22_DY1_PULLTYPESELECT = 0x0
  - CONTROL_CORE_PAD0_CSI22_DY2[3] CSI22_DY1_PULLUDENABLE = 0x1
- csi22_dx1:
  - CONTROL_CORE_PAD0_CSI22_DX1_PAD1_CSI22_DY1[8] CSI22_DX1_INPUTENABLE = 0x1
  - CONTROL_CORE_PAD0_CSI22_DX1_PAD1_CSI22_DY1[4] CSI22_DX1_PULLTYPESELECT = 0x0
  - CONTROL_CORE_PAD0_CSI22_DX1_PAD1_CSI22_DY1[3] CSI22_DX1_PULLUDENABLE = 0x1
- csi22_dy1:
  - CONTROL_CORE_PAD0_CSI22_DX1_PAD1_CSI22_DY1[24] CSI22_DY1_INPUTENABLE = 0x1
  - CONTROL_CORE_PAD0_CSI22_DX1_PAD1_CSI22_DY1[20] CSI22_DY1_PULLTYPESELECT = 0x0
  - CONTROL_CORE_PAD0_CSI22_DX1_PAD1_CSI22_DY1[19] CSI22_DY1_PULLUDENABLE = 0x1
- csi22_dx0:
  - CONTROL_CORE_PAD0_CSI22_DX0_PAD1_CSI22_DY0[8] CSI22_DX0_INPUTENABLE = 0x1
  - CONTROL_CORE_PAD0_CSI22_DX0_PAD1_CSI22_DY0[4] CSI22_DX0_PULLTYPESELECT = 0x0
  - CONTROL_CORE_PAD0_CSI22_DX0_PAD1_CSI22_DY0[3] CSI22_DX0_PULLUDENABLE = 0x1
- csi22_dy0:
  - CONTROL_CORE_PAD0_CSI22_DX0_PAD1_CSI22_DY0[24] CSI22_DY0_INPUTENABLE = 0x1
  - CONTROL_CORE_PAD0_CSI22_DX0_PAD1_CSI22_DY0[20] CSI22_DY0_PULLTYPESELECT = 0x0
  - CONTROL_CORE_PAD0_CSI22_DX0_PAD1_CSI22_DY0[19] CSI22_DY0_PULLUDENABLE = 0x1

(d) Power up the CSIPHY:

(i) Set CSI2_COMPLEXIO_CFG[28:27] PWR_CMD to 0x1.

(e) Check whether the state status reaches the ON state:

- CSI2_COMPLEXIO_CFG[26:25] PWR_STATUS = 0x1

(f) Wait for STOPSTATE = 1 (for all enabled lane modules):

(i) The timer is set through the CSI2_TIMING[14:0] bit field. The reset value can be kept.

(ii) Wait until CSI2_TIMING[15] FORCE_RX_MODE_IO1 = 0x0. It is automatically put at 0 when all enabled lanes are in STOPSTATE and the timer is finished.

(g) Release PIPD* (= 1).

For CSI2-A CAMERARX pullup on signals through padconf registers:

- csi21_dx4:
  - CONTROL_CORE_PAD0_CSI21_DX4_PAD1_CSI21_DY4[4] CSI21_DX4_PULLTYPESELECT = 0x1
- csi21_dy4:

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  - CONTROL_CORE_PAD0_CSI21_DX4_PAD1_CSI21_DY4[20] CSI21_DY4_PULLTYPESELECT = 0x1
- csi21_dx3:
  - CONTROL_CORE_PAD0_CSI21_DX3_PAD1_CSI21_DY3[4] CSI21_DX3_PULLTYPESELECT = 0x1
- csi21_dy3:
  - CONTROL_CORE_PAD0_CSI21_DX3_PAD1_CSI21_DY3[20] CSI21_DY3_PULLTYPESELECT = 0x1
- csi21_dx2:
  - CONTROL_CORE_PAD0_CSI21_DX2_PAD1_CSI21_DY2[4] CSI21_DX2_PULLTYPESELECT = 0x1
- csi21_dy2:
  - CONTROL_CORE_PAD0_CSI21_DX2_PAD1_CSI21_DY2[20] CSI21_DY2_PULLTYPESELECT = 0x1
- csi21_dx1:
  - CONTROL_CORE_PAD0_CSI21_DX1_PAD1_CSI21_DY1[4] CSI21_DX1_PULLTYPESELECT = 0x1
- csi21_dy1:
  - CONTROL_CORE_PAD0_CSI21_DX1_PAD1_CSI21_DY1[20] CSI21_DY1_PULLTYPESELECT = 0x1
- csi21_dx0:
  - CONTROL_CORE_PAD0_CSI21_DX0_PAD1_CSI21_DY0[4] CSI21_DX0_PULLTYPESELECT = 0x1
- csi21_dy0:
  - CONTROL_CORE_PAD0_CSI21_DX0_PAD1_CSI21_DY0[20] CSI21_DY0_PULLTYPESELECT = 0x1

3. The CSIPHY is initialized and ready/active in CSI2 mode.

8.2.3.2.3 ISS CCP2 and Link Initialization Sequence

The CSI2-B interface is expected to coordinate the PHY initialization. The controller must ensure that the PHY is held in RESET state until the CCP transmitter is powered up and the link comes to the defined state. The controller can use the FORCERXMODE signals of CAMERARX for this purpose. FORCERXMODE forces the receiver state-machine into RESET state, while the rest of common logic is powered up and functional. One possible initialization sequence is:

To fully initialize the CSIPHY, perform the following steps:

1. Configure all CSI2-B receiver registers to be ready to receive signals/data from the CSIPHY:
   (a) Configure all CCP2 registers:
      (i) Set CSI2_COMPLEXIO_CFG[2:0] CLOCK_POSITION.
      (ii) Set CSI2_COMPLEXIO_CFG[6:4] DATA1_POSITION.
   (b) Set CONTROL_CAMERA_RX[20:19] CAMERARX_CSI22_CAMMODE or CONTROL_CAMERA_RX[17:16] CAMERARX_CSI21_CAMMODE.

> **CAUTION**
>
> This must be done before the CSIPHY is active.

2. CSIPHY and link initialization sequence:
   (a) Deassert the CSIPHY reset:
      (i) Set CSI2_COMPLEXIO_CFG[30] RESET_CTRL to 0x1.

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(b) Assert the FORCERXMODE signal:

(i) Set CSI2_TIMING[15] FORCE_RX_MODE_IO1 to 0x1.

(c) Power up the CSIPHY:

(i) Set CSI2_COMPLEXIO_CFG[28:27] PWR_CMD to 0x1.

(d) Check that the state status reaches the ON state:

- CSI2_COMPLEXIO_CFG[26:25] PWR_STATUS = 0x1

(e) Release the FORCERXMODE signal:

(i) Set CSI2_TIMING[15] FORCE_RX_MODE_IO1 to 0x0.

3. The CSIPHY is initialized and ready/active in CSI1/CCP2B mode.

8.2.3.2.4 ISS CSI PHY Error Signals

In D-PHY mode, the CSIPHY supports the following error detection and signaling to the associated receiver:

- ERRSOTHS: Flags 1-bit errors in the HS start of transmission synchronization pattern. In this error scenario, the CSIPHY continues to receive the data and pass it to the receiver, but confidence in the data may be low, because of the 1-bit error seen in sync. This signal, if asserted, is high for one cycle of RXBYTECLKHS.
- ERRSOTSYNCHS: Flags multiple bit errors in the HS start of transmission synchronization pattern. In this case, the CSIPHY cannot achieve proper synchronization and does not pass the received data to the receiver. This signal, if asserted, is high for one cycle of RXBYTECLKHS.
- ERRCONTROL: Flags the control sequence error; that is, when the LP sequence observed on line is not recognized as a valid control sequence. This signal, if asserted, is high until the next change in the state of the LP line.
- ERRESC: Flags the escape entry error; that is, when the escape entry sequence is unrecognized. This signal, if asserted, is high until the next change in the state of the LP line.
- ERRSYNCESC: Flags the low-power data transmission synchronization error. This error is flagged if the number of bits received during a low-power data transmission is not a multiple of 8 bits. This signal, if asserted, is high until the next change in the state of the LP line. In case the number of received bits is 1 less than a multiple of 8, RXVALIDESC is also asserted together with ERRSYNCESC, and an erroneous data byte is output on RXDATAESC. In other cases of this error, RXVALIDESC is not asserted and an erroneous data byte is not sent out.

In CCP2 mode, the CSIPHY supports the following error detection and signaling to the associated receiver:

- CCPERRRESYNC output is an error indicator to the receiver to flag the shifted synchronization error, if the new synchronization sequence is not aligned with a 32-bit word boundary compared to the previously received synchronization sequence. This error flag is asserted for 32 cycles (4 bytes/32 bits).

8.2.3.3 ISS CSI2 PHY Register Manual

8.2.3.3.1 ISS CSI2 PHY Instance Summary

Table 8-44 lists the ISS CSI2 PHY instance.

Table 8-44. ISS CSI2 PHY Instance Summary

Module Name	L3 Base Address	Size
ISS_CAMERARX_CORE1	0x5200 1170	32 bytes
ISS_CAMERARX_CORE2	0x5200 1570	32 bytes

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NOTE: ISS_CAMERARX_CORE1 is for CSI2-A CAMERARX.

ISS_CAMERARX_CORE2 is for CSI2-B/CCP2 CAMERARX.

8.2.3.3.2 ISS CSI2 PHY Registers

8.2.3.3.2.1 ISS CSI2 PHY Register Summary

Table 8-45 summarizes the ISS CSI2 register mapping.

Table 8-45. ISS CSI2 PHY Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	ISS_CAMERARX_ CORE1 Base Address	ISS_CAMERARX_ CORE2 Base Address
REGISTER0	RW	32	0x0000 0000	0x5200 1170	0x5200 1570
REGISTER1	RW	32	0x0000 0004	0x5200 1174	0x5200 1574
REGISTER2	RW	32	0x0000 0008	0x5200 1178	0x5200 1578

8.2.3.3.2.2 ISS CSI2 PHY Register Description

through describe the ISS CSI2 PHY register bits.

Table 8-46. REGISTER0

Address Offset	0x0000 0000
Physical Address	0x5200 1170 0x5200 1570
Description	First register
Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							HSCLOCKCONFIG	RESERVED								THS_TERM								THS_SETTLE							

Bits	Field Name	Description	Type	Reset
31:25	RESERVED	Reserved fields	NA	0x00
24	HSCLOCKCONFIG	Disable clock missing detector	RW	0
23:16	RESERVED	Read returns zero	R	0x00
15:8	THS_TERM	THS_TERM timing parameter in multiples of DDR clock Effective time for enabling of termination = synchronizer delay + timer delay + LPRX delay + combinational routing delay ~ (1–2)* DDRCLK + THS-TERM + ~ (1 –15) ns Programmed value = ceil(12.5 / DDR clock period) –1	RW	0x04
7:0	THS_SETTLE	THS_SETTLE timing parameter in multiples of DDR clock frequency Effective THS_SETTLE seen on line (starting to look for sync pattern) = synchronizer delay + timer delay + LPRX delay + combinational routing delay – pipeline delay in HS data path. ~ (1–2)* DDRCLK + THS-SETTLE + ~ (1–15) ns –1*DDRCLK Programmed value = ceil(90 ns / DDR clock period) + 3	RW	0x27

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Table 8-47. Register Call Summary for Register REGISTER0

ISS Interfaces

- ISS CSI2 PHY Functional Configuration: [0] [1]
- ISS CSI2 PHY and Link Initialization Sequence: [2]
- ISS CSI2 PHY Registers: [3]

Table 8-48. REGISTER1

Address Offset	0x0000 0004
Physical Address	0x5200 1174 0x5200 1574
Description	Second register
Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESVD_READ_BIT		RESET_DONE_STATUS		RESERVED		CLOCK_MISS_DETECTOR_STATUS		TCLK_TERM								DPHY_HS_SYNC_PATTERN						CTRLCLK_DIV_FACTOR		TCLK_SETTLE							

Bits	Field Name	Description	Type	Reset
31:30	RESVD_READ_BIT	Reserved bit	NA	0x0
29:28	RESET_DONE_STATUS	Reset done read bits. 28: RESETDONERXBYTECLK **Note:** BYTECLK is provided to the ISS CSI2-A, CSI2-B, and CCP2 interfaces 29: RESETDONECTRLCLK **Note:** This is the CAM_PHY_CTRL_FCLK provided to the PHY from the PRCM module.	R	0x0
27:26	RESERVED	Write 0 for future compatibility.	RW	0x0
25	CLOCK_MISS_DETECTOR_STATUS	1: Error in clock missing detector. 0: Clock missing detector successful	R	0
24:18	TCLK_TERM	TCLK_TERM timing parameter in multiples of CTRLCLK Effective time for enabling of termination = synchronizer delay + timer delay + LPRX delay + combinational routing delay ~ (1–2)* CTRLCLK + TCLK_TERM + ~ (1–15) ns Programmed value = ceil(9.5 / CTRLCLK period) – 1	RW	0x00
17:10	DPHY_HS_SYNC_PATTERN	DPHY mode HS sync pattern in byte order (reverse of received order) See Section 8.2.3.2.4, *ISS CSI PHY Error Signals.*	RW	0xB8
9:8	CTRLCLK_DIV_FACTOR	Divide factor for CTRLCLK for CLKMISS detector	RW	0x1
7:0	TCLK_SETTLE	TCLK_SETTLE timing parameter in multiples of CTRLCLK Clock Effective TCLK_SETTLE = synchronizer delay + timer delay + LPRX delay + combinational routing delay ~ (1–2)* CTRLCLK + Tclk-settle + ~ (1 –15) ns Programmed value = max[3, ceil(155 ns/CTRLCLK period) –1]	RW	0x0E

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Table 8-49. Register Call Summary for Register REGISTER1

ISS Interfaces
• ISS CSI2 PHY and Link Initialization Sequence: [0]
• ISS CSI2 PHY Registers: [1]

Table 8-50. REGISTER2

Address Offset	0x0000 0008
Physical Address	0x5200 1178 0x5200 1578
Description	Third register
Type	RW

31 30	29 28	27 26	25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
TRIGGER_CMD_RXTRIGESC0	TRIGGER_CMD_RXTRIGESC1	TRIGGER_CMD_RXTRIGESC2	TRIGGER_CMD_RXTRIGESC3	CCP2_SYNC_PATTERN		

Bits	Field Name	Description	Type	Reset
31:30	TRIGGER_CMD_RXTRIGESC0	Mapping of Trigger escape entry command to PPI output RXTRIGGERESC0	RW	0x0
29:28	TRIGGER_CMD_RXTRIGESC1	Mapping of Trigger escape entry command to PPI output RXTRIGGERESC1	RW	0x0
27:26	TRIGGER_CMD_RXTRIGESC2	Mapping of Trigger escape entry command to PPI output RXTRIGGERESC2	RW	0x0
25:24	TRIGGER_CMD_RXTRIGESC3	Mapping of Trigger escape entry command to PPI output RXTRIGGERESC3	RW	0x0
23:0	CCP2_SYNC_PATTERN	CCP2 mode sync pattern in byte order See Section 8.2.3.2.4, *ISS CSI PHY Error Signals.*	R	0x0000FF

Table 8-51. Register Call Summary for Register REGISTER2

ISS Interfaces
• ISS CSI2 PHY and Link Initialization Sequence: [0]
• ISS CSI2 PHY Registers: [1]

8.2.4 ISS CCP2

8.2.4.1 ISS CCP2 Environment

8.2.4.1.1 ISS CCP2 Protocol and Data Formats

This section describes the CCP2 protocol and data formats. The CCP2 receiver is compatible with the *SMIA CCP2 Specification v1.0* and the *MIPI CSI1 Specification*. Table 8-52 describes the I/O for serial interface CCP2.

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Table 8-52. I/O Description for Serial Interface CCP2

Signal Name		I/O [1]	Description
ccp2_datp	CAM_S_DATA	I	Serial data input. Configurable.
ccp2_datn			
ccp2_strbp	CAM_S_CLK	I	Serial clock or strobe input. Configurable.
ccp2_strbn			

(1) I = Input; O = Output

From the device point of view, the CCP2 interface comprises four differential inputs representing two effective signals: the serial data and the clock.

The CCP2 receiver is a serial interface to an image sensor. Signals from the camera are serial input data (CAM_S_DATA) and a clock/strobe signal (CAM_S_CLK).

8.2.4.1.1.1 ISS CCP2 Synchronization Codes

Each frame is clearly identified by four unique 32-bit synchronization codes: frame start, frame end, line start, and line end, which are embedded in the serial bitstream. The logical channel identification number is also encoded in the synchronization codes.

- Frame-start code (FSC): Identifies the start of a new frame
- Line-start code (LSC): Identifies the start of a new line and is received for every line, except the first line, that starts with an FSC
- Line-end code (LEC): Identifies the end of a line and is received for every line, except the last line, that ends with an FEC
- Frame-end code (FEC): Identifies the end of the last line and the end of the current frame

8.2.4.1.1.2 ISS CCP2 False Synchronization Code Protection

CCP2 supports false synchronization protection (FSP). Additional bytes after the JPEG stream can be written to the SDRAM. They do not prevent JPEG encode and there is no need to preserve them.

8.2.4.1.1.3 ISS CCP2 Image Data Operating Modes and Alignment Constraints

The CCP2 receiver interface has several image data operating modes (see Table 8-53). The EXPx formats (where x = 8, 16, or 32) are used to expand data up to 8, 16, or 32 bits by padding data with zeros. The Data Size Increase in Memory column indicates memory overhead versus format without data expansion and/or DPCM compression.

Table 8-53. ISS CCP2 Image Data Operating Modes and Alignment Constraints

CCP2_LCx_CTRL[7:2] Format	CCP2 Data Format	Bits per Pixel (bpp) (When sending data to memory, N/A when sending to VP)	Data Size Increase in Memory. (When negative, data compression present)	2D Mode Availability [1]	Comments
0x0	YUV4:2:2 big endian	16	0%	Yes	
0x1	YUV4:2:2 little endian	16	0%	Yes	
0x2	YUV4:2:0	12	0%	Yes	
0x3	YUV4:2:2 + VP	N/A, data are sent to VP, YUV4:2:2 + VP = RAW8 + VP	N/A	Yes	
0x3	RAW8 + VP	N/A, data are sent to VP, YUV4:2:2 + VP must be used to output RAW8 + VP to memory	N/A	Yes	

(1) If 2D mode is available, there are no supplementary constraints on data width. 2D mode does not apply when sending to the video port (VP).

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Table 8-53. ISS CCP2 Image Data Operating Modes and Alignment Constraints (continued)

CCP2_LCx_CTRL[7:2] Format	CCP2 Data Format	Bits per Pixel (bpp) (When sending data to memory, N/A when sending to VP)	Data Size Increase in Memory. (When negative, data compression present)	2D Mode Availability (1)	Comments
0x4	RGB444 + EXP16	16	50%	Yes	
0x5	RGB565	16	0%	Yes	
0x6	RGB888	24	0%	Yes	
0x7	RGB888 + EXP32	32	33%	Yes	
0x8	RAW6 + EXP8	8	33%	Yes	
0x9	RAW6 + DPCM10 + EXP16	16	167%	Yes	DPCM decompression
0xA	RAW6 + DPCM10 + VP	N/A, data are sent to VP	N/A	Yes	DPCM decompression
0xB	RAW10 - RAW6 DPCM	6	40%	Yes	DPCM compression
0xC	RAW7 + EXP8	8	14%	Yes	
0xD	RAW7 + DPCM10 + EXP16	16	128%	Yes	DPCM decompression
0xE	RAW7 + DPCM10 + VP	N/A, data are sent to VP	N/A	Yes	DPCM decompression
0xF	RAW10 - RAW6 DPCM + EXP8	8	25%	Yes	DPCM compression
0x10	RAW8, this mode can be used to output RAW6 and RAW7	8	0%	Yes	
0x11	RAW8 + DPCM10 + EXP16	16	100%	Yes	DPCM decompression
0x12	RAW8 + DPCM10 + VP	N/A, data are sent to VP	N/A	Yes	DPCM decompression
0x13	RAW10 - RAW7 DPCM	7	30%	Yes	DPCM compression
0x14	RAW10	10	0%	Yes	
0x15	RAW10 + EXP16	16	60%	Yes	
0x16	RAW10 + VP	N/A, data are sent to VP	N/A	Yes	
0x17	RAW10 - RAW7 DPCM + EXP8	8	20%	Yes	
0x18	RAW12	12	0%	Yes	
0x19	RAW12 + EXP16	16	33%	Yes	
0x1A	RAW12 + VP	N/A, data are sent to VP	N/A	Yes	
0x1B	RAW10 - RAW8 DPCM	8	20%	Yes	DPCM decompression
0x1C	JPEG, 8-bit data	N/A	0%	Yes	
0x1D	JPEG, 8-bit data + FSP	N/A	0%	Yes	
0x1E	RAW10 - RAW8 DPCM	8	20%	Yes	Data right shift
0x1F	RAW8 DPCM12-RAW12 + VP	N/A, data are sent to VP	N/A	Yes	
0x20	RAW10 - RAW8 ALAW	8	20%	Yes	
0x21	RAW8 DPCM10 - ALAW	8	20%	Yes	

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NOTE:

- Padding data of a 32-bit pixel data stream is handled the same way regardless of the programmed format. Therefore, there is no increase or decrease in storage because it is not compressed or decompressed.
- EXP8 = Data expansion to 8 bits, padding with zeros
- EXP16 = Data expansion to 16 bits, padding with alpha or zeros

  CCP2_LCx_CTRL[15:8] ALPHA can be used to set an alpha value.

  For RGB444 + EXP16:

  – data_out[31:28] = ALPHA [3:0]
  – data_out[15:12] = ALPHA [3:0]
- EXP32 = Data expansion to 32 bits, padding with alpha

  CCP2_LCx_CTRL[15:8] ALPHA can be used to set an alpha value.

  For RGB888 + EXP32: data_out[31:24] = ALPHA [7:0]
- FSP = False synchronization code protection decoding. Applies only to JPEG8 data format.
- VP = Output to the video-preprocessing hardware is enabled. Programmers must ensure that only one logical channel is enabled to the video preprocessing hardware. The behavior of the hardware is unpredictable if several logical channels to the video preprocessing hardware are enabled simultaneously.
- DPCM10 = Data decompression to 10 bits. Applies only to RAW6, RAW7, and RAW8 data formats; disabled if CCP2_CTRL[4] MODE = 0.
- Padding is handled the same way regardless of the programmed format.

NOTE: Data written by CSI2 can be read back by the CCP2 read channel. Some constrains apply (see Table 8-56).

8.2.4.1.1.4 ISS CCP2 Pixel Data Format

This section summarizes how the CCP2 pixel data formats are transmitted over the serial interface and how the pixels are reconstructed, stored in memory, or passed to the video port.

The CCP2 receiver can cope with all data formats if the data line length sent through the CS1/CCP2 physical protocol is a multiple of 32 bits. This condition is required for the CCP2 receiver to work correctly.

However, some data formats impose stronger line-length constraints to finish pixel reconstruction correctly at the end of the lines. This is imposed by CCP2 protocol-specific requirements, and not the CCP2 receiver. If CCP2 protocol constraints are not respected:

- Only the pixels reconstructed last in every line are erroneous. The missing bits are replaced with zeros to perform pixel reconstruction.
- The FW_IRQ interrupt is triggered.

8.2.4.1.1.4.1 ISS CCP2 YUV Operating Modes

NOTE: Although there are different possibilities of endianness in the bitstream, the device as a whole typically works in little-endian format. Therefore, the use of little-endian format is recommended.

8.2.4.1.1.4.1.1 ISS CCP2 YUV4:2:2

The YUV4:2:2 data format can be stored to memory in little- or big-endian format. The line length sent through the CCP2 receiver protocol must be a multiple of 32 bits.

YUV4:2:2 data format can also be sent to the video port.

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YUV4:2:2 + VP is used to output RAW8 data to the video port: YUV4:2:2 + VP is equivalent to RAW8 + VP. Figure 8-14 and Figure 8-15 show big-endian and little-endian YUV4:2:2 format, respectively. Set CCP2_LCx_CTRL[7:2] FORMAT to 0x0 to select YUV4:2:2 big-endian mode and to 0x1 for YUV4:2:2 little-endian mode.

Figure 8-14. ISS CCP2 YUV4:2:2 Big Endian

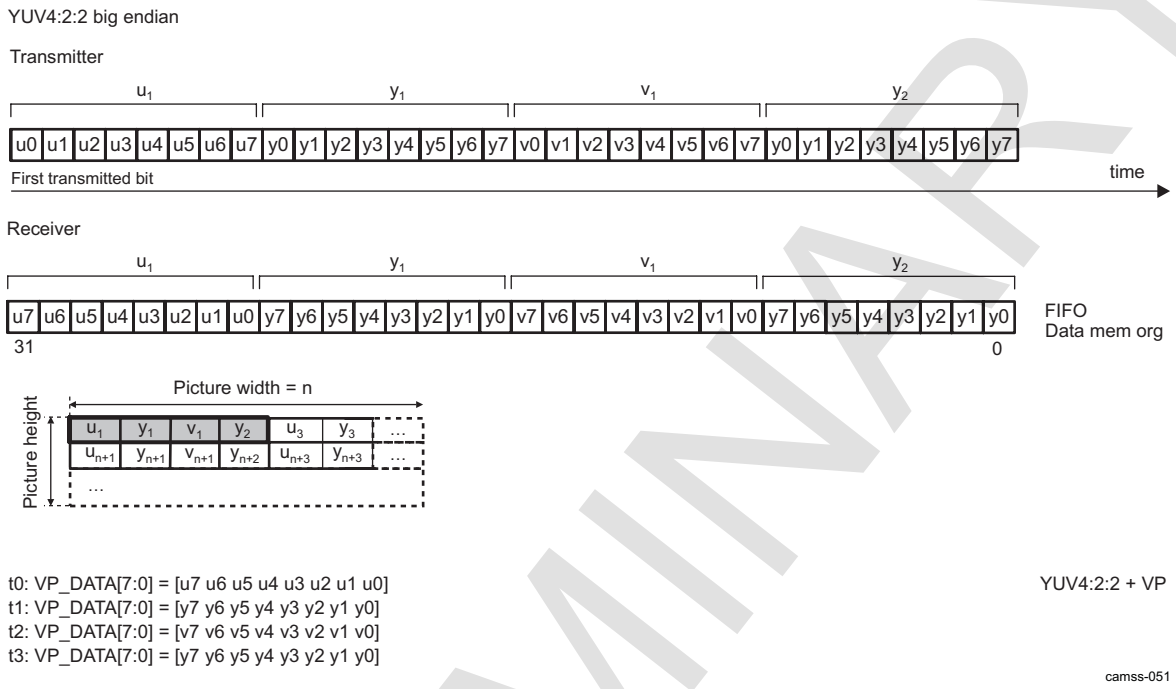
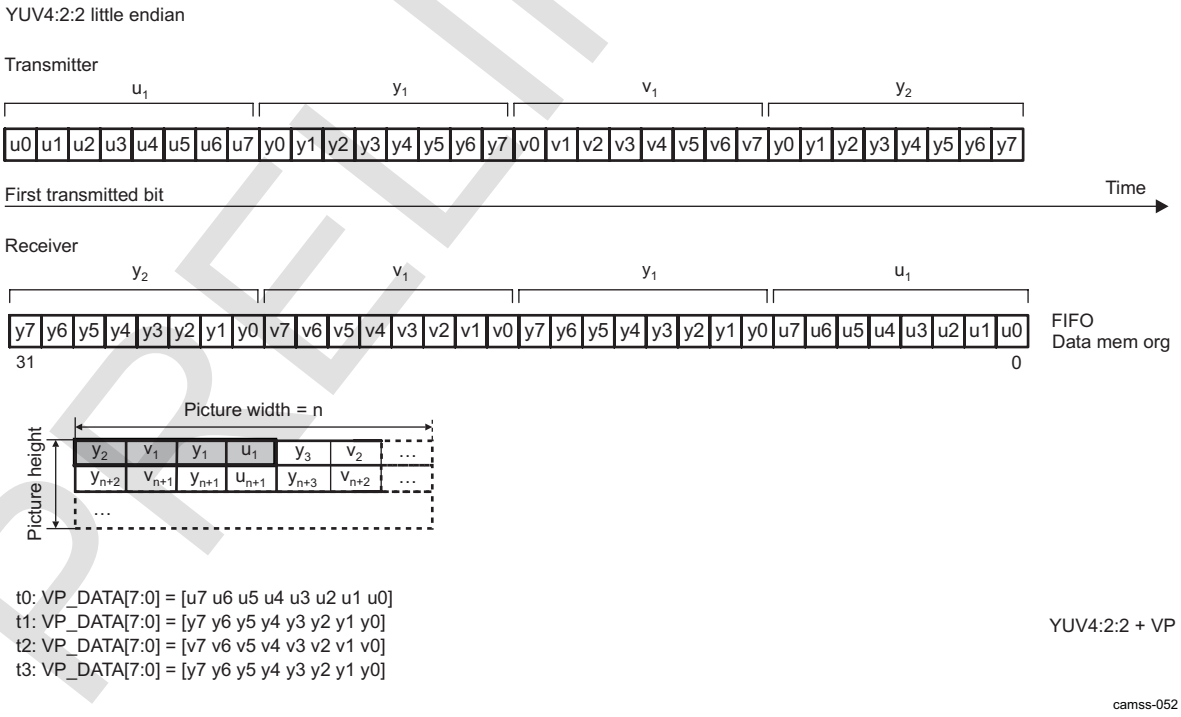


Figure 8-15. ISS CCP2 YUV4:2:2 Little Endian



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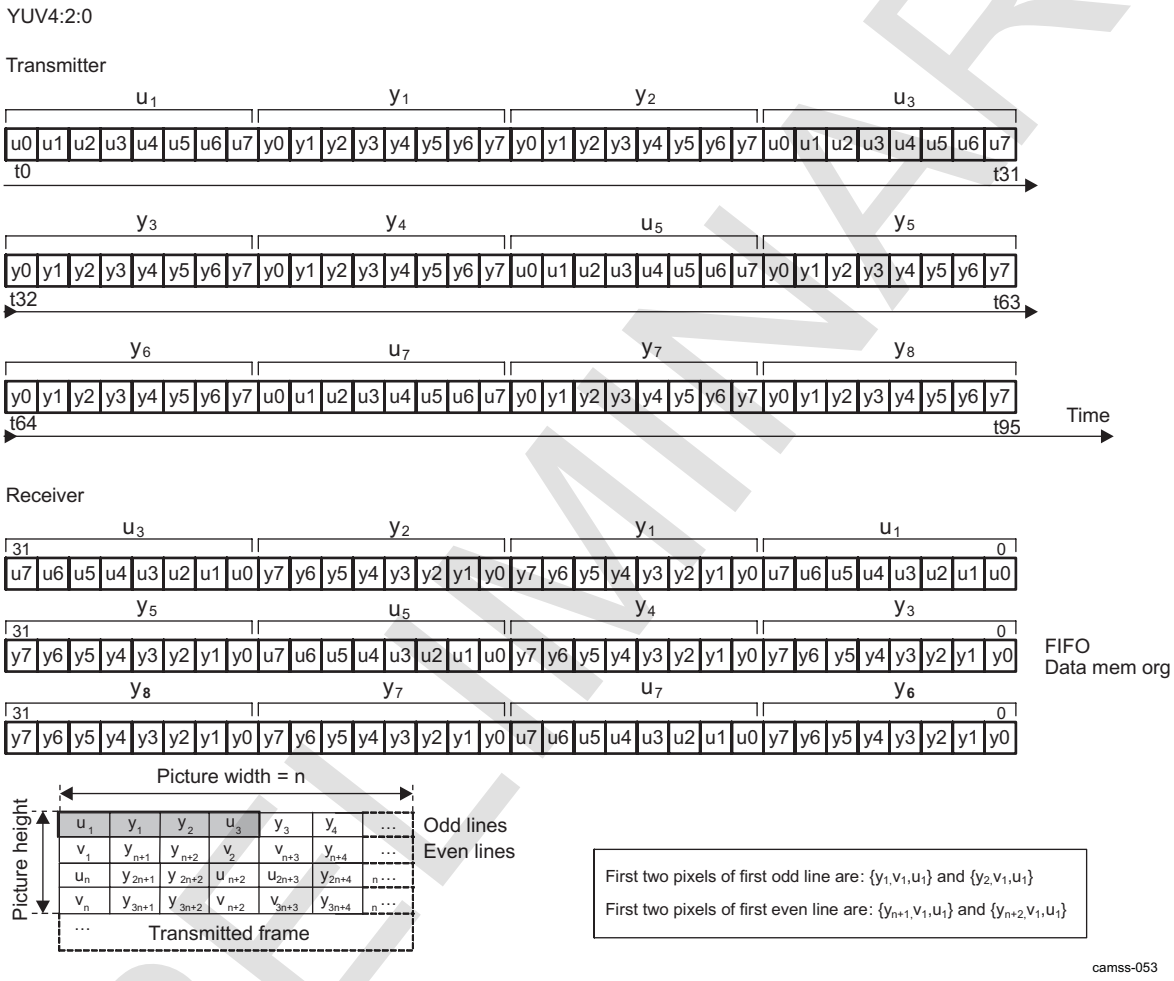
8.2.4.1.1.4.1.2 ISS CCP2 YUV4:2:0

The line length sent through the CCP2 receiver protocol is a multiple of 32 bits. Furthermore, the line length all together sent by the CCP2 receiver is a multiple of 3 x 32 bits and the number of lines is even to correctly finish the pixel reconstruction.

The line structure is different for odd and even lines. Odd lines transport the U component, while even lines contain the V component. This is shown in Figure 8-16. Set CCP2_LCx_CTRL[7:2] FORMAT to 0x3 to select YUV4:2:0 mode.

Figure 8-16. ISS CCP2 YUV4:2:0



8.2.4.1.1.4.2 ISS CCP2 RGB Operating Modes

8.2.4.1.1.4.2.1 ISS CCP2 RGB888

RGB888 data format can be output to memory in two formats: without data expansion and with data expansion.

If data expansion is used, the value of the 8 upper bits is programmable and can be set with an alpha value for computer graphics applications. The line length sent through the CCP2 receiver protocol is a multiple of 32 bits. The line length all together sent by the CCP2 receiver is a multiple of 3 x 32 bits to finish pixel reconstruction correctly.

Figure 8-17 is an example of RGB888 format. Set CCP2_LCx_CTRL[7:2] FORMAT to 0x6 to select RGB888 mode (24 bits) or to 0x7 to expand RGB888 over 32 bits.

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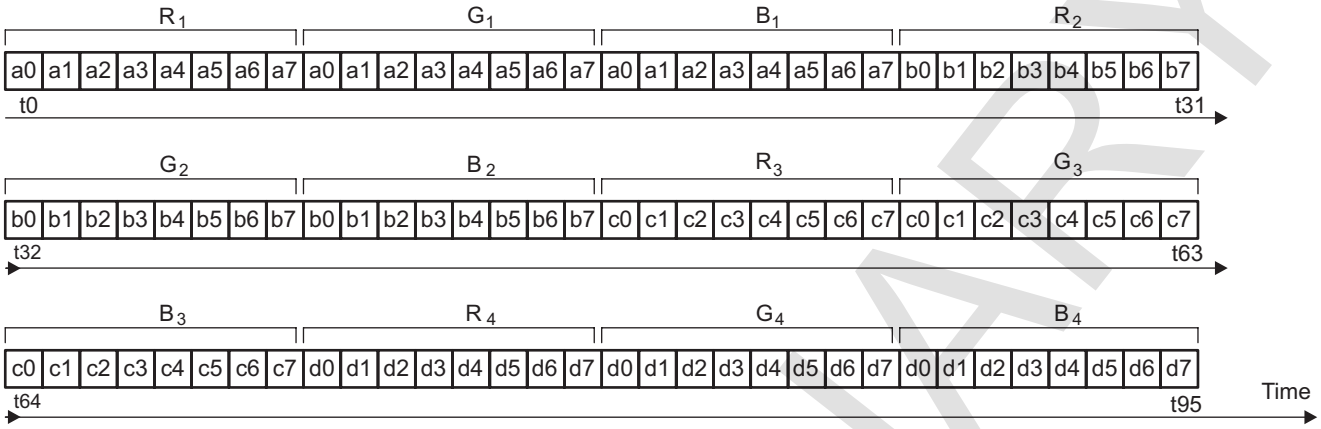
Figure 8-17. ISS CCP2 RGB888

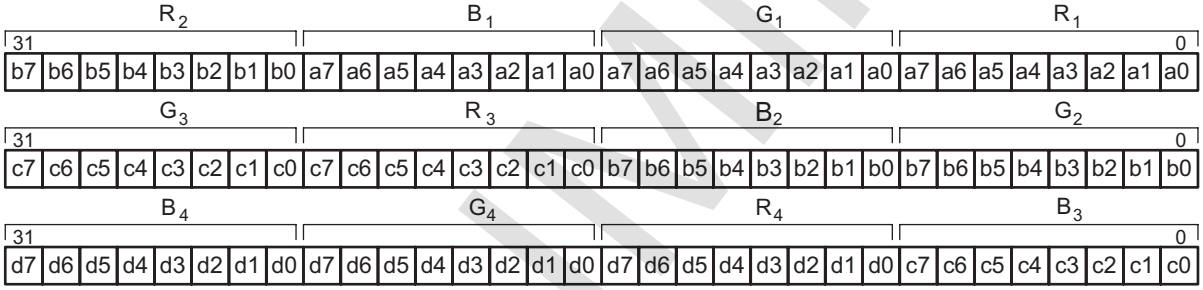
RGB888 Line width must be a multiple of three 32-bit words.

Transmitter

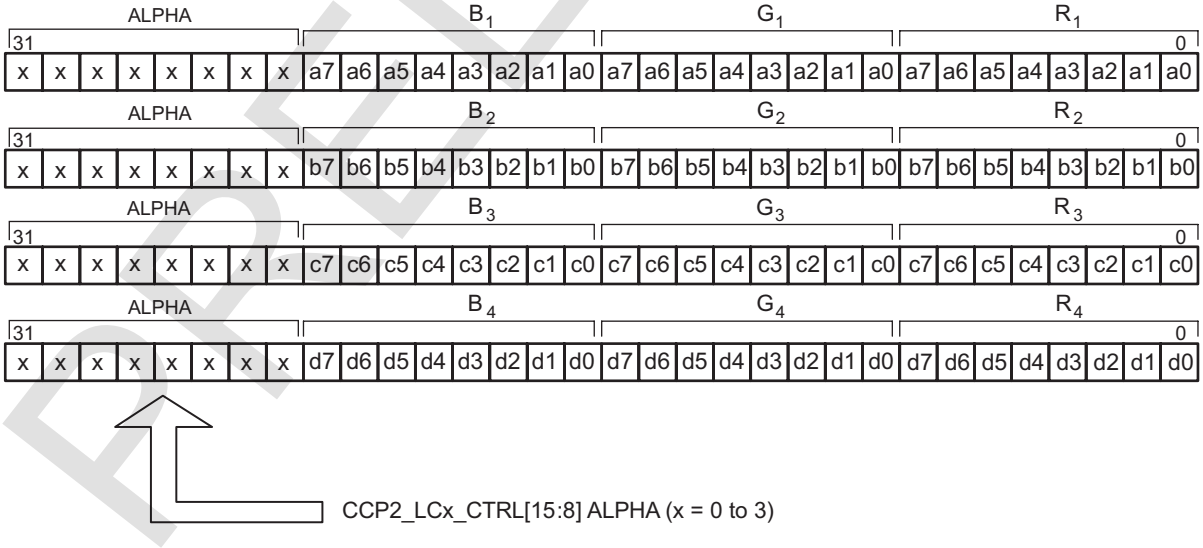


Receiver

Without data expansion



With data expansion



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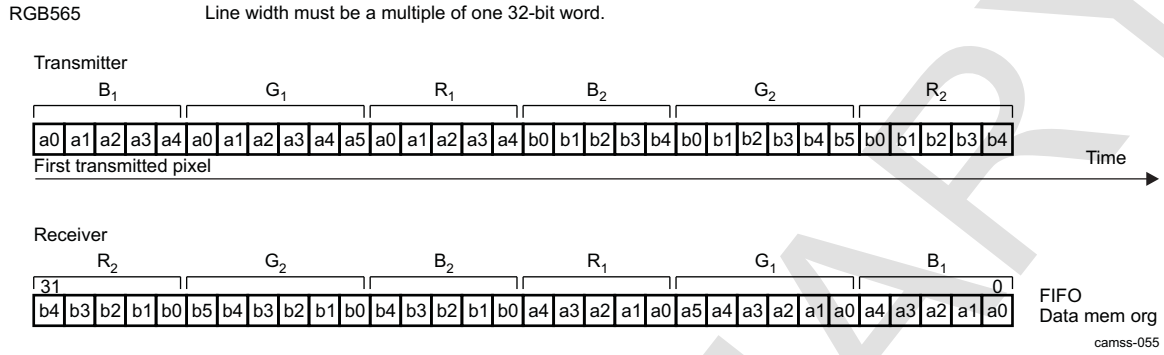
8.2.4.1.1.4.2.2 ISS CCP2 RGB565

For RGB565, the line length sent through the CCP2 receiver protocol is a multiple of 32 bits (see Figure 8-18). Set CCP2_LCx_CTRL[7:2] FORMAT to 0x6 to select RGB565 mode.

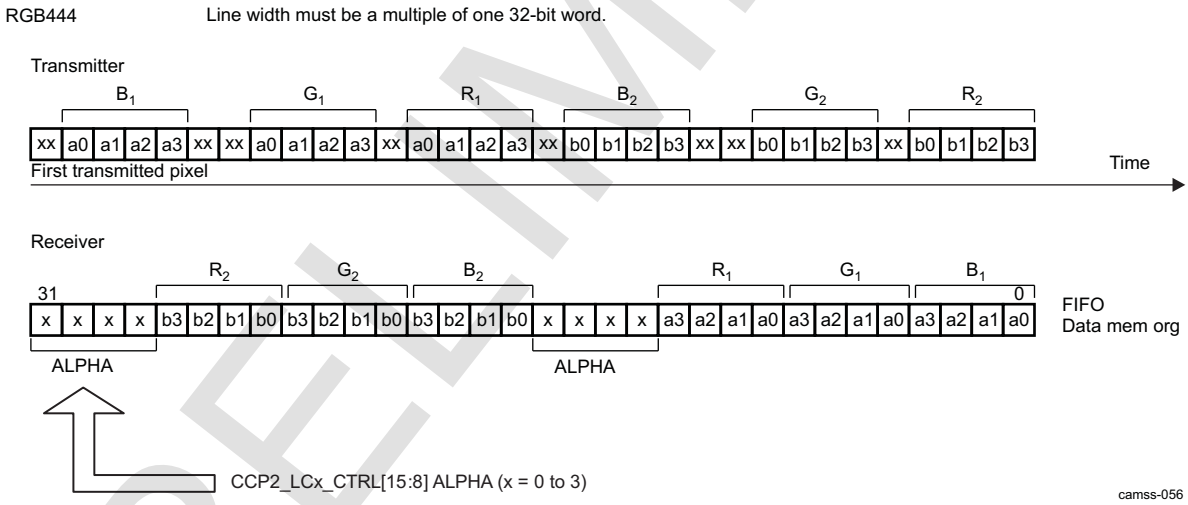
Figure 8-18. ISS CCP2 RGB565



8.2.4.1.1.4.2.3 ISS CCP2 RGB444

RGB444 data format is output to memory with data expansion. If data expansion is used, the value of the 4 upper bits is programmable and can be set with an alpha value for computer graphics applications. The line length sent through the CCP2 receiver protocol is a multiple of 32 bits (see Figure 8-19). Set CCP2_LCx_CTRL[7:2] FORMAT to 0x4 to select RGB444 mode (12 bits expanded to 16).

Figure 8-19. ISS CCP2 RGB444



8.2.4.1.1.4.3 ISS CCP2 RAW Bayer Operating Modes

NOTE: For more information about packed RAW data, see Section 8.2.4.3.5.1, *ISS CCP2 Read Data From Memory*.

8.2.4.1.1.4.3.1 ISS CCP2 RAW6

RAW6 data format can be output to memory in two formats: without data expansion and with data expansion. The line length sent through the CSI receiver protocol is a multiple of 32 bits. The line all together sent by the CCP2 receiver is a multiple of 3 x 32 bits to finish pixel reconstruction correctly (the lowest common multiple of 32 and 6 is 96; that is, 3 x 32 bits).

Figure 8-20 shows the RAW6 format. Set CCP2_LCx_CTRL[7:2] FORMAT to:

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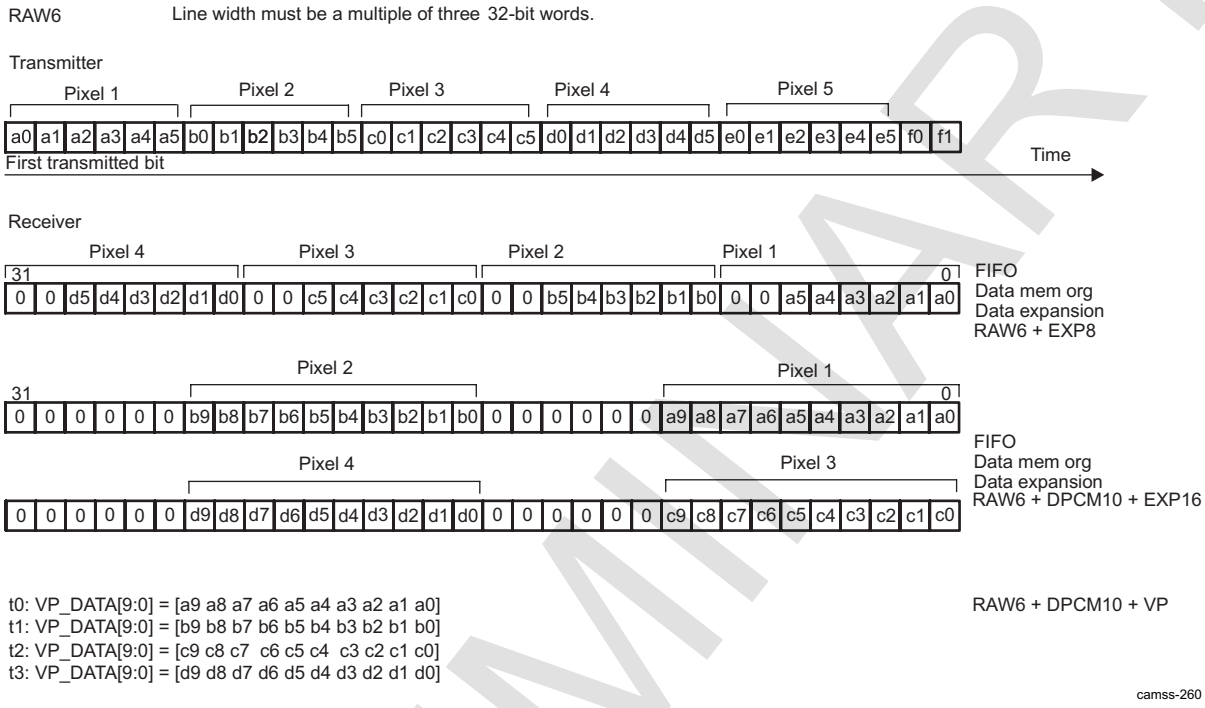
- 0x8 to select RAW6 mode expanded to 8-bit
- 0x9 to select RAW6 mode with DPCM decompression
- 10-bit and expansion to 16-bit
- 0xA to select RAW6 mode with DPCM decompression to 10-bit to video port

Figure 8-20. ISS CCP2 RAW6



NOTE: Use RAW8 data format to output RAW6 data format to memory.

8.2.4.1.1.4.3.2 ISS CCP2 RAW7

RAW7 data format can be output to memory in two formats: without data expansion and with data expansion. The line length sent through the CCP2 receiver protocol is a multiple of 32 bits. The line length all together sent by the CCP2 receiver is a multiple of 7 x 32 bits to finish the pixel reconstruction correctly (the lowest common multiple of 32 and 7 is 224; that is, 7 x 32 bits).

Figure 8-21 shows the RAW7 format. Set CCP2_LCx_CTRL[7:2] FORMAT to:

- 0xC to select RAW7 mode expanded to 8-bit
- 0xD to select RAW7 mode with DPCM decompression to 10-bit and expansion to 16-bit
- 0xE to select RAW7 mode with DPCM decompression to 10-bit to video port

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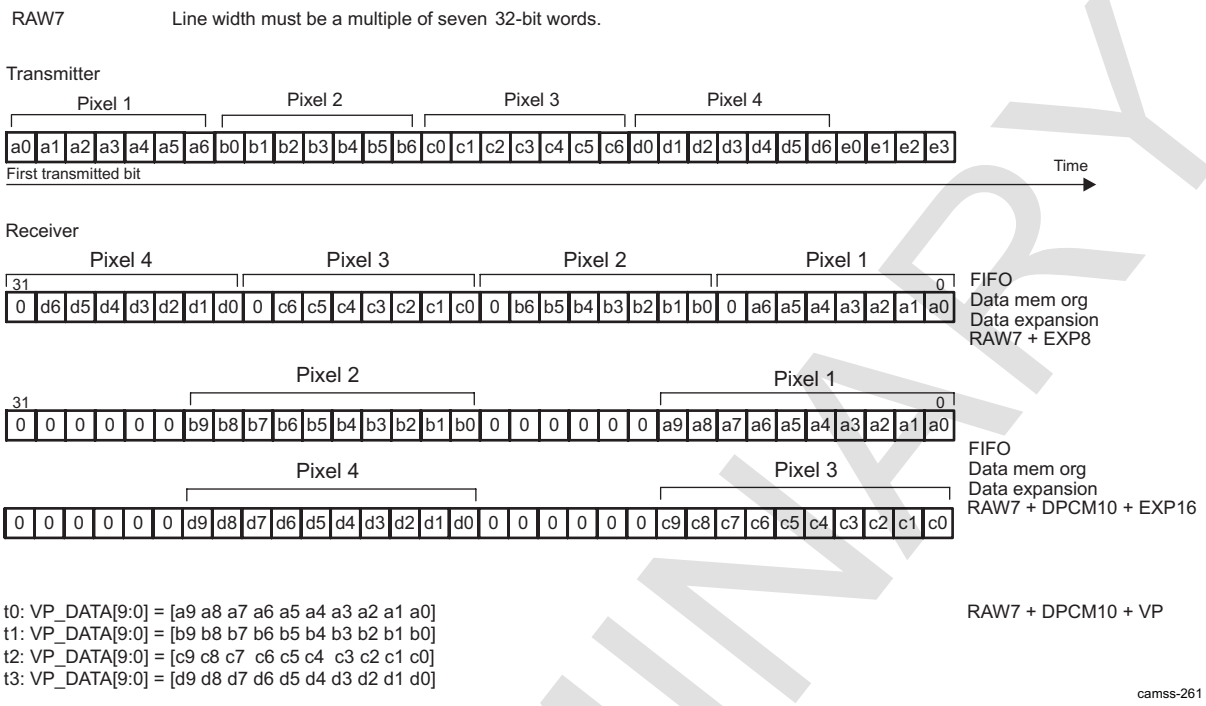
Figure 8-21. ISS CCP2 RAW7



NOTE: Use RAW8 data format to output RAW7 data format to memory.

8.2.4.1.1.4.3.3 ISS CCP2 RAW8

RAW8 data format can be output to memory. The line length sent through the CCP2 receiver protocol is a multiple of 32 bits.

Figure 8-22 shows RAW8 format. Set CCP2_LCx_CTRL[7:2] FORMAT to:

- 0x10 to select RAW8
- 0x11 to select RAW8 mode with DPCM decompression to 10-bit and expansion to 16-bit
- 0x12 to select RAW8 mode with DPCM decompression to 10-bit to video port
- 0x20 to select RAW8 with A-Law decompression to RAW10

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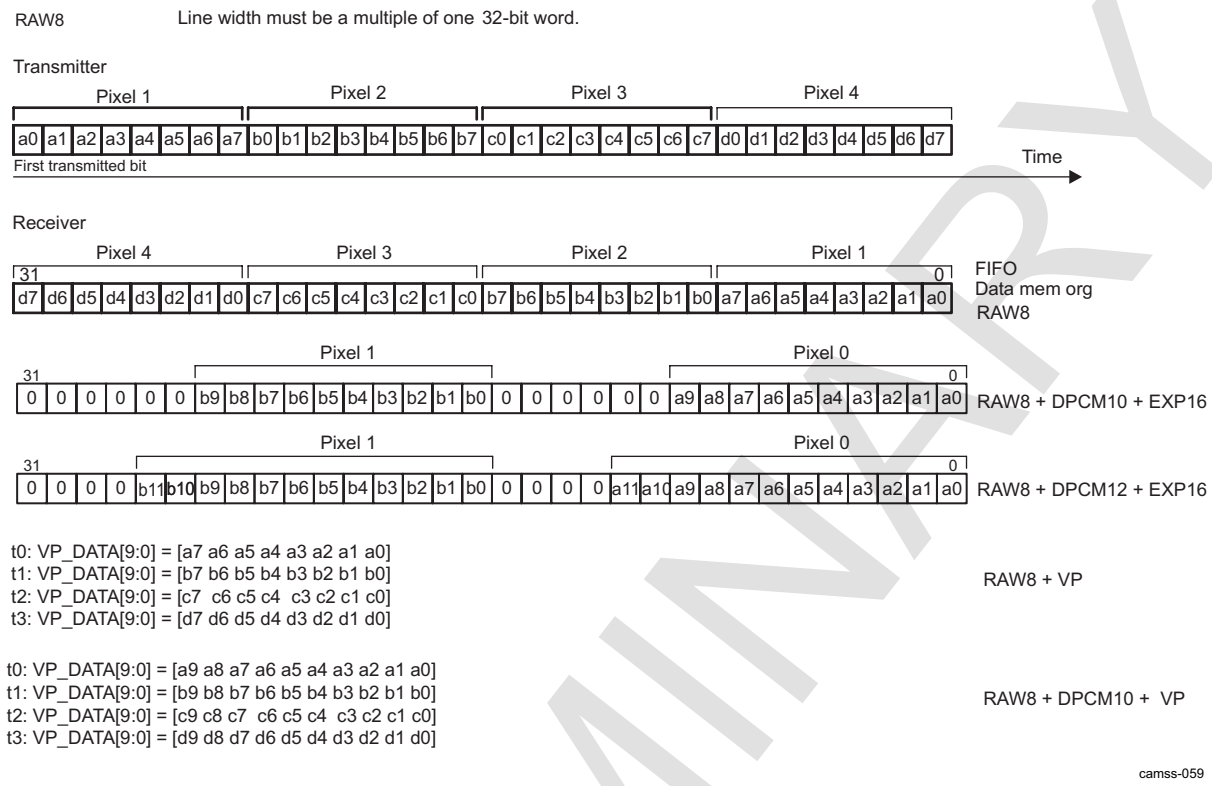
Figure 8-22. ISS CCP2 RAW8



NOTE: Use YUV4:2:2 + VP to output RAW8 data to the video port: YUV4:2:2 + VP is equivalent to RAW8 + VP.

8.2.4.1.1.4.3.4 ISS CCP2 RAW10

RAW10 data format can be output to memory in two formats: without data expansion and with data expansion. If data expansion is used, the 10-bit data are padded with 0s on a 16-bit word. The line length sent through the CCP2 receiver protocol is a multiple of 32 bits. Furthermore, the line length all together sent by the CCP2 receiver is a multiple of 5 x 32 bits to finish pixel reconstruction correctly (the lowest common multiple of 32 and 10 is 320; that is, 10 x 32 bits).

RAW10 data format can be sent to the video port. Figure 8-23 shows the RAW10 format. Set CCP2_LCx_CTRL[7:2] FORMAT to:

- 0x14 to select RAW10
- 0x13 to select RAW10 mode with DPCM compression to 7-bit
- 0x16 to select RAW10 mode to video port
- 0x17 with DPCM compression to 7-bit with expansion to 8-bit
- 0x1B to select RAW10 compressed to 8-bit
- 0xB with DPCM compression to 6-bit
- 0xF to select RAW10 compressed to 6-bit with expansion to 8-bit
- 0x1E to select RAW10 compressed to 8-bit
- 0x20 to select RAW10 with A-Law compression to RAW8

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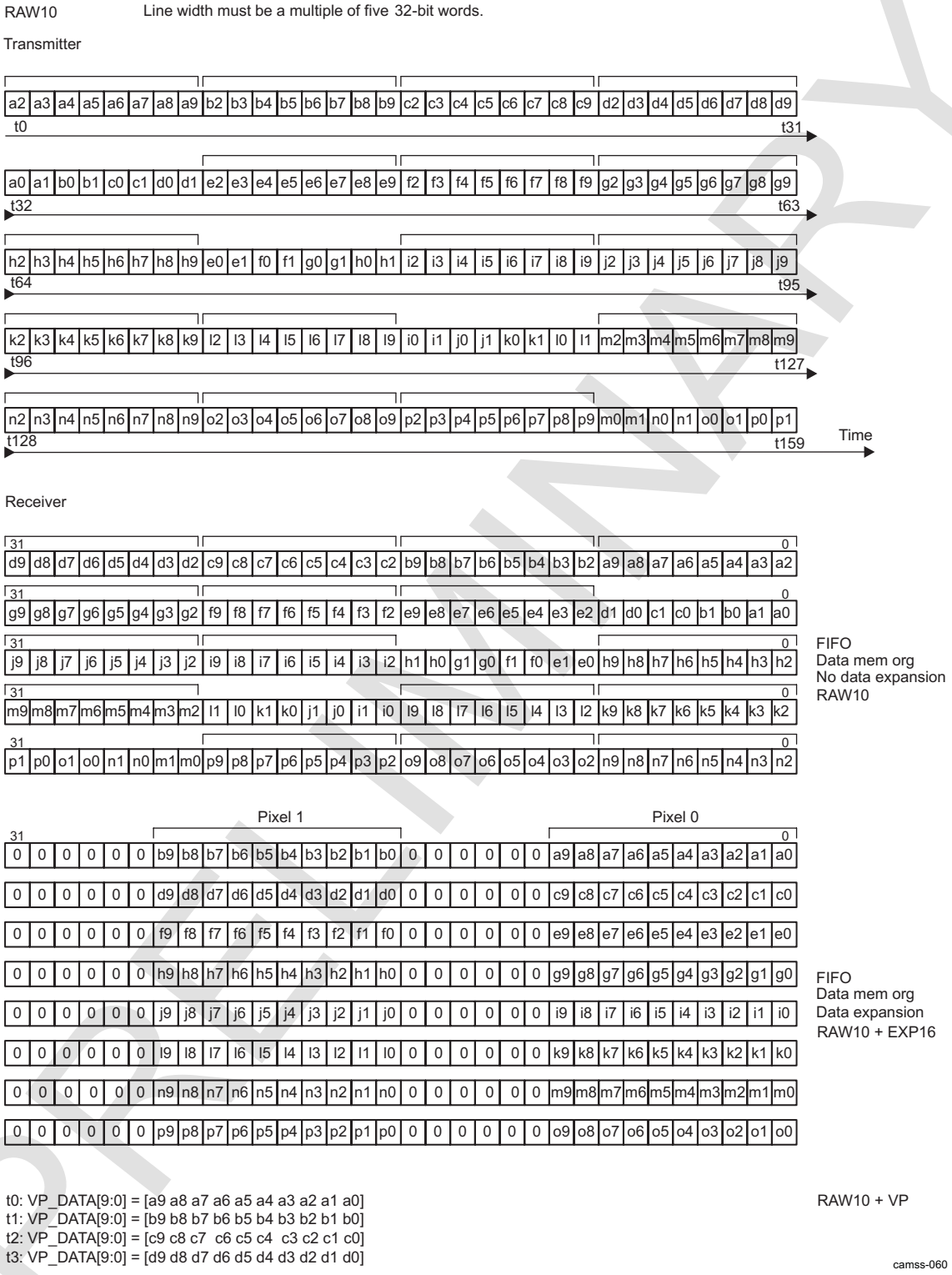
Figure 8-23. ISS CCP2 RAW10



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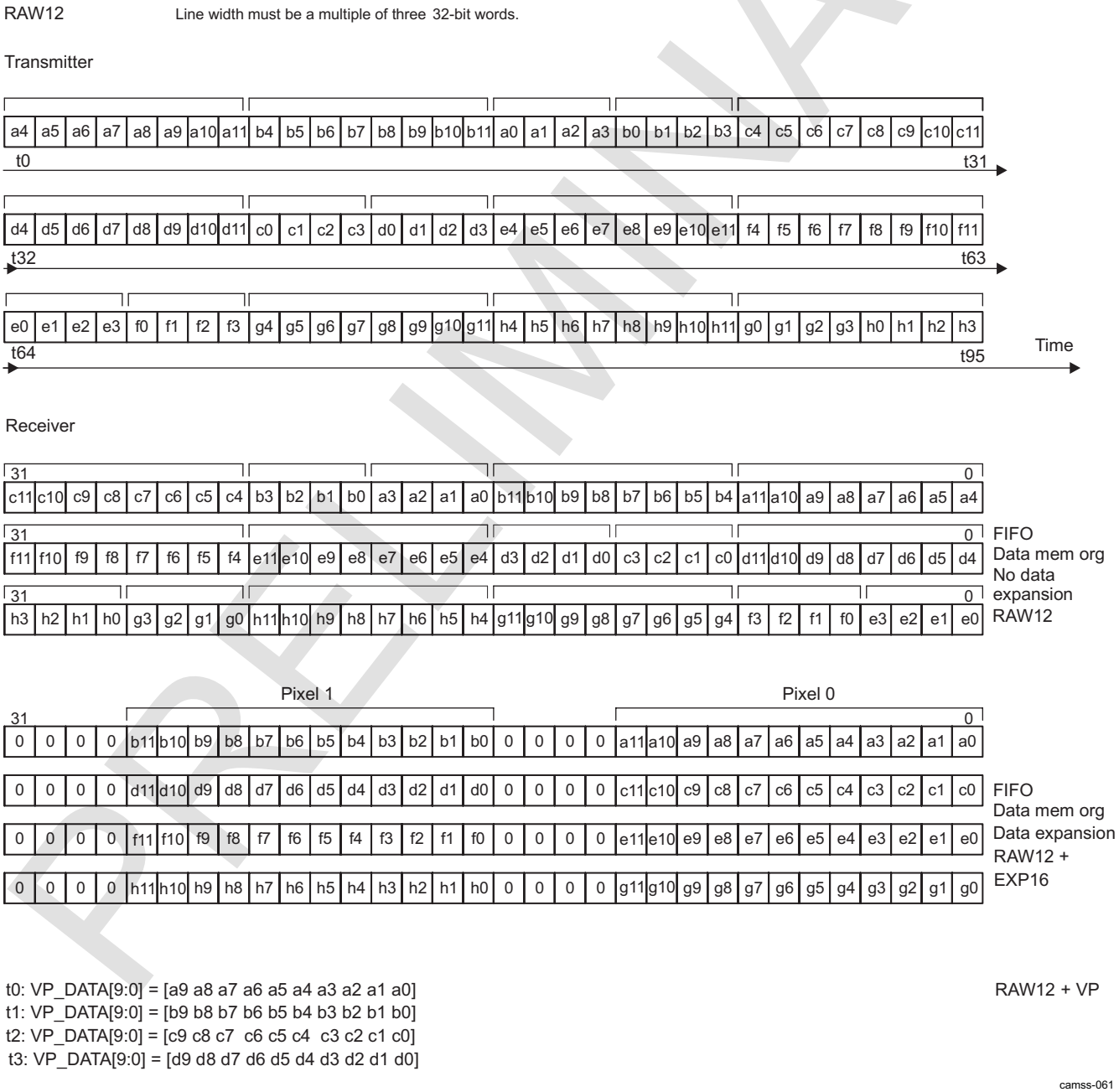
8.2.4.1.1.4.3.5 ISS CCP2 RAW12

RAW12 data format can be output to memory in two formats: without data expansion and with data expansion. If data expansion is used, the 12-bit data are padded with 0s on a 16-bit word. The line length sent through the CCP2 PHY is a multiple of 32 bits. The line length is a multiple of 3 x 32 bits to finish pixel reconstruction correctly (the lowest common multiple of 32 and 12 is 96; that is, 3 x 32 bits).

RAW12 data format can be sent to the video port. Figure 8-24 shows RAW12 format. Set CCP2_LCx_CTRL[7:2] FORMAT to:

- 0x18 to select RAW12
- 0x19 to select RAW12 mode with expansion to 16-bit
- 0x1A to select RAW12 mode to video port
- 0x17 with DPCM compression to 7-bit with expansion to 8-bit

Figure 8-24. ISS CCP2 RAW12



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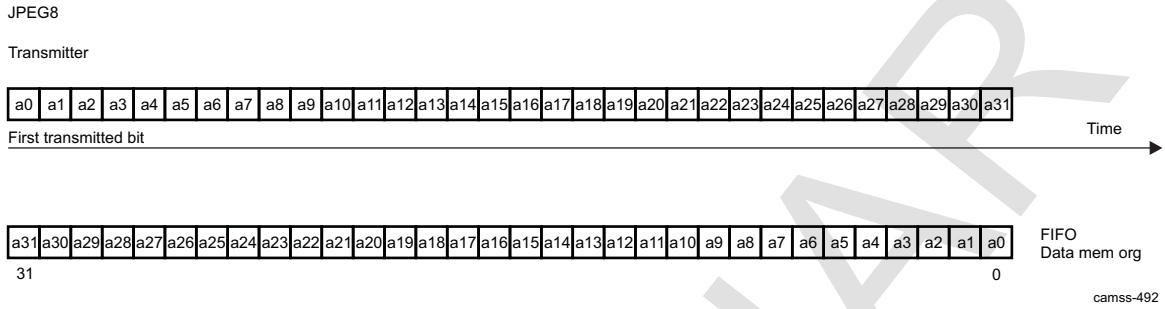
8.2.4.1.1.4.4 ISS CCP2 JPEG8 Operating Modes

The line length sent through the CCP2 receiver protocol is a multiple of 32 bits. The FSP code insertion on the transmitter side automatically ensures this line length. It is impossible to know in advance the size of a compressed stream. Figure 8-25 shows the JPEG8 and JPEG8 FSP format. Set CCP2_LCx_CTRL[7:2] FORMAT to 0x1C to select JPEG8 format, or to 0x1D to select JPEG8 format with FSP.

Figure 8-25. ISS CCP2 JPEG8 and JPEG8 FSP



In JPEG8 mode, the JPEG encoder on the sensor side must avoid generating data equal to the synchronization code and must deliver a synchronization-code-free bitstream for line-start and line-end before and after the transmitted data. For more information, see Section 8.2.4.1.1.2, *ISS CCP2 False Synchronization Protection Code*.

8.2.4.1.1.5 ISS CCP2 Data Transfer Through Write Master Port

The CCP2 receiver module uses its 64-bit master interface to transfer the data stored in the FIFO. The system can set the burst size to be used in the CCP2_CTRL BURST register. The recommended burst size is 128 bytes (0x4: 16 x 64-bit bursts are the most efficient for memory output); other sizes should be used only when issues are faced. The module tries to burst data whenever possible to increase system performance and save power. The module uses the appropriate register-selected burst size when the conditions (address is properly aligned, there is enough data in the FIFO to finish the line) are met; otherwise, it uses single requests.

For example, if the line consists of 50 pixels of 64-bit data and BURST = 0x4 (16 × 64-bit bursts), the module generates four times 16 x 64-bit bursts to transmit the whole line. The FIFO can have information about only two different lines.

The CCP2 engine supports tag count. The count is configurable through a register at the top level of the ISS (see Section 8.1.3, *ISS Register Manual*).

8.2.4.2 ISS CCP2 Integration

Figure 8-26 is an overview of the integration of the CCP2 interface in the device. The figure shows the CCP2 receiver top-level block diagram. The CCP2 receiver receives serial data from a CCP2-compatible image sensor, converts it to parallel data, extracts the logical channels, detects and extracts the synchronization codes, reformats the data, and outputs it through the VP interface (which is connected to the video preprocessing hardware [ISP]) or the ISS interconnect. The CCP2 can also get its data from memory using a dedicated interface read master port when this feature is enabled at compile time.

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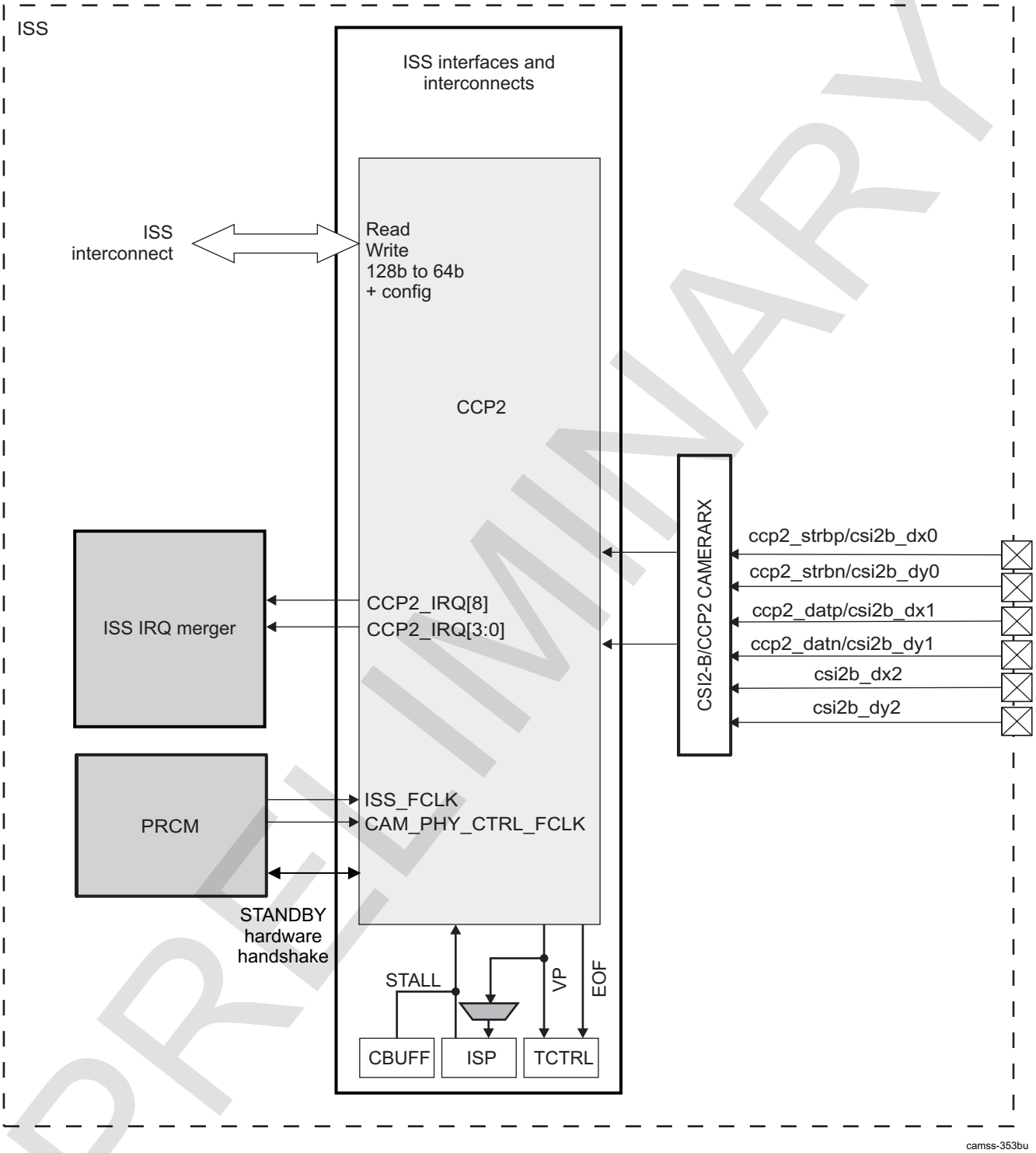
Figure 8-26. ISS CCP2 Integration



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NOTE: Because CCP2 and CSI2-B share pins, they cannot be used simultaneously. For ISP source select, see Section 8.1.1, *ISS Integration*, for ISP registers input selection and for top-level input select settings.

For power domain, clocks, reset, and hardware requests, see Section 8.1.2.4, *ISS Power Management*.

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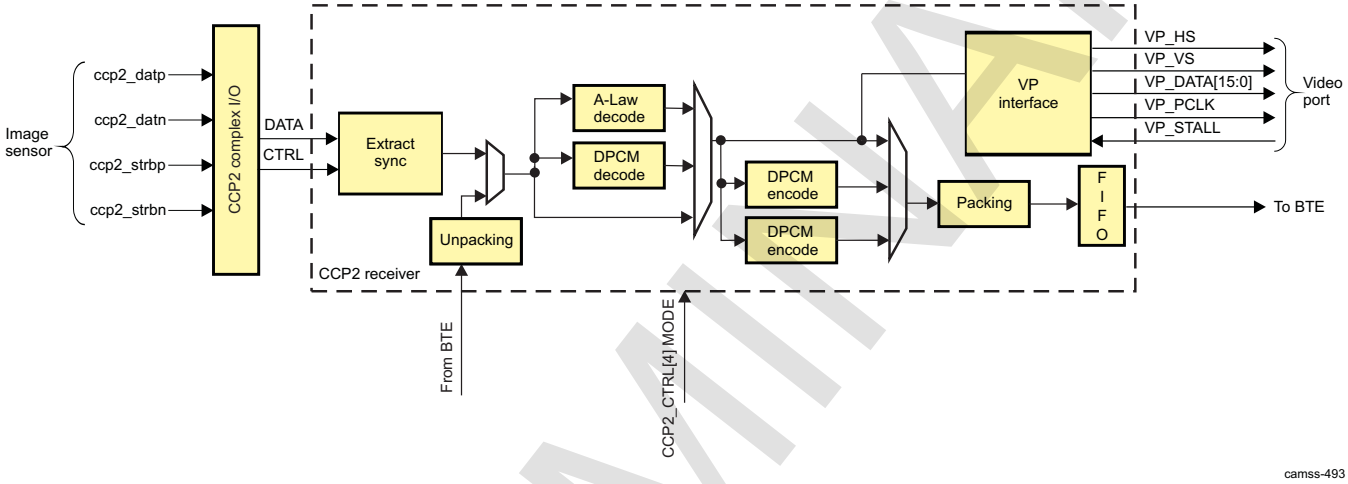
8.2.4.3 ISS CCP2 Functional Description

8.2.4.3.1 ISS CCP2 Overview

Figure 8-27 is the top-level block diagram of the CCP2 receiver. The CCP2 receiver receives serial data from a CCP2-compatible image sensor, converts it to parallel data, extracts the logical channels, detects and extracts the synchronization codes, reformats the data, and outputs it through the VP interface (which is connected to the video preprocessing hardware [ISP]) or the ISS interconnect. The CCP2 can also read data from memory getting burst packets from the BTE when this feature has been enabled at compile time. For read data from memory, see Section 8.2.4.3.5, *ISS CCP2 Memory Read Channel*.

The CCP2 receiver video port interface is connected to the video preprocessing hardware.

Figure 8-27. ISS CCP2 Receiver Block Diagram



8.2.4.3.2 ISS CCP2 PHY

The CCP2 receiver does not connect directly to a sensor (see Section 8.2.3, *ISS CSI2 PHY*). It uses a complex I/O physical layer. The CCP2 complex I/O is shared with the CSI2-B receiver. The CSI2-B/CCP2 PHY is powered up by configuring the CSI2 receiver configuration register. For more information about the configuration of the PHY, see Section 8.2.3.2.1, *ISS CSI2 PHY Functional Configuration*. The CCP2 serial interface is a unidirectional differential serial interface with two options for the PHY: data/clock or data/strobe signals. After the PHY is configured and initialization is done, the CCP2 mode can be selected and controlled by the CCP2_CTRL[1] MODE bit.

8.2.4.3.2.1 ISS CCP2 Data/Clock Signaling

Data/clock signaling consists of two parallel signals: data and data clock.

- The data signal carries bit serial data. The CCP2 transmitter writes the data on each falling edge of the clock. The data are usually transmitted bytewise, least-significant bit (LSB) first.
- The data clock signal carries the clock signal. The CCP2 transmitter writes the data on each falling edge of the clock. The CCP2 receiver reads the data on the rising edge of the clock.

8.2.4.3.2.2 ISS CCP2 Data/Strobe Signaling (CCP2 Only)

Data/strobe signaling consists of two parallel signals: data and data strobe.

- The data signal carries bit serial data.
- The data strobe signal carries the strobe signal. It toggles when the data signal does not change state.

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The data signal or the strobe signal changes between 2 data bits. The data and strobe signals must not change simultaneously. The data and strobe signals are used in the receiver to reconstruct the transmission clock. Both fronts of the reconstructed clock are used to sample the data. Set the CCP2_CTRL[4] MODE bit and see Section 8.2.3, *ISS CSI2 PHY*, to set the data/clock or data/strobe function.

8.2.4.3.3 ISS CCP2 VP Interface

Table 8-54 summarizes the video interface signals. The video interface connects the CCP2 receiver module to the video preprocessing hardware (ISP). The interface is connected to a 16-bit video port. On the other side of the video port is the ISIF inside the ISP. The ISIF also uses the signals listed in Table 8-54 to synchronize pixel data sent to it by the CCP2 receiver.

Table 8-54. ISS CCP2 Video interface Signals

Pin	Type (1)	Description
VP_HS	O	Line trigger output signal
VP_VS	O	Frame trigger output signal
VP_DATA[15:0]	O	Parallel output data: bits 0 to 15
VP_PCLK	O	Video port pixel clock. The frequency can be configured.
VP_STALL	I	Stalls data flow when data is read from memory

(1) I = Input; O = Output

When data is read from memory and sent to the video port, the data flow can be stalled by asserting the VP_STALL signal. Doing so does not overflow internal FIFOs: the CCP2 module adapts its read rate automatically.

The response time to the VP_STALL signal must not exceed two cycles: when VP_STALL is asserted, the CCP2 module can send 0, 1, or 2 pixels to the video port.

VP_STALL is asserted and deasserted synchronous to the functional clock.

NOTE: Stalling the video port for data received from the sensor may lead to internal overflows; VP_STALL must not be used for this purpose.

The pixel clock is generated from the functional clock. Clock pulses are gated based on the selected clock division factor and pixel availability. In other words, software must set the CCP2 receiver to ensure that the pixel clock:

- Never exceeds what the ISP can support: the top value set in the CCP2_CTRL[31:15] FRACDIV bit field
- Is sent only when valid pixels or blanking data must be sent

Also, software must set the number of clock pulses during horizontal blanking periods using the CCP2_CTRL1[1:0] BLANKING bit field.

- The CCP2 receiver stops generating horizontal blanking clock pulses when the number of pulses defined in the CCP2_CTRL1[1:0] BLANKING bit field are generated or when data for the next line arrives from the sensor.
- Free-running horizontal blanking can be selected only when data comes from the sensor.
- When data comes from memory, the CCP2 receiver ensures that the number of horizontal blanking pulses defined in the CCP2_CTRL1[1:0] BLANKING bit field is received. The CCP2 receiver stops generating horizontal blanking clock pulses when then number of pulses defined in the CCP2_CTRL1[1:0] BLANKING bit field is generated or when data for the next line arrives from the sensor.

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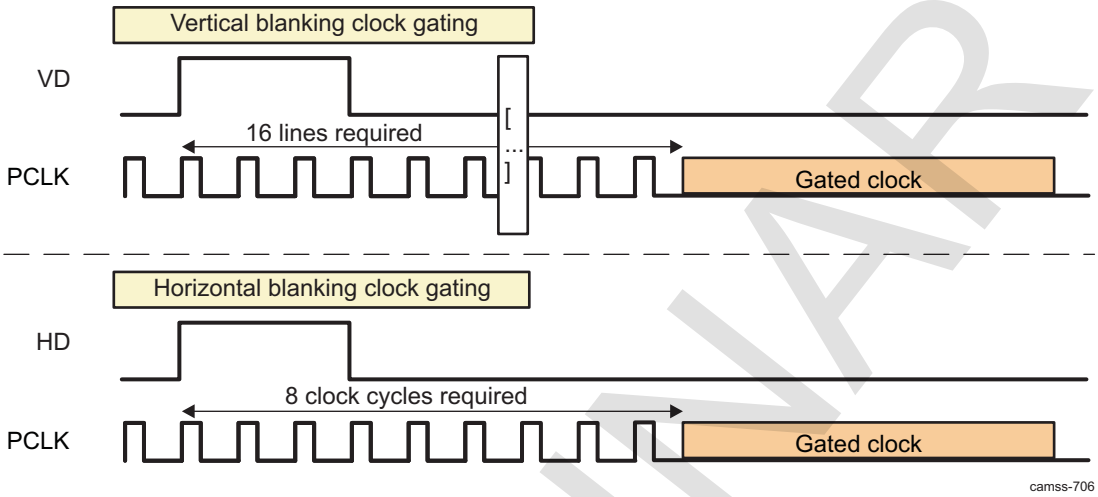
NOTE: To work properly, the ISP requires a minimum of eight clock cycles in the horizontal blanking period and a minimum of 16 lines in the vertical blanking period. The pixel clock can be gated only when these intervals are respected. This is required to flush the pipeline of the different ISP modules. Figure 8-28 shows VP_PCLK gating during blanking periods.

Figure 8-28. ISS CCP2 VP_PCLK Gating During Blanking Periods



Vertical blanking generation is controlled through the CCP2_CTRL[9] VP_CLK_FORCE_ON bit. The VP_PCLK clock is enabled during vertical blanking periods when this bit is set. This pushes pixels through the ISP processing pipe. It is needed, for example, when the ISP resizer uses the averager. Otherwise, hardware ensures only that at least four clock pulses are generated before the first pixel of each frame. It may be necessary for the clock to keep running after the frame end to flush internal pipelines. In that case, an interrupt request (IRQ) or status bit is typically present in the attached hardware that indicates when the VP_PCLK clock is no longer needed (for example, an end of processing interrupt). The module leaves the vertical blanking state when new data is received from the sensor or the memory read channel.

The configured pixel clock is used for active and blanking periods.

Table 8-55 shows how RAW and YUV data is sent over the video port. The data is sent to the ISIF if ISP is used. For the ISIF details about video port data, see Section 8.3 *ISS: ISP*.

Table 8-55. ISS CCP2 Video Port Data Mapping

Format	Video Port DATA[15:0]															
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RAW6	0	0	0	0	0	0	0	0	0	0	R5	R4	R3	R2	R1	R0
RAW7	0	0	0	0	0	0	0	0	0	R6	R5	R4	R3	R2	R1	R0
RAW8	0	0	0	0	0	0	0	0	R7	R6	R5	R4	R3	R2	R1	R0
RAW10	0	0	0	0	0	0	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0
RAW12	0	0	0	0	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0
RAW14	0	0	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0
RAW16	R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0
YUV4:2:2	0	0	0	0	0	0	0	0	U7	U6	U5	U4	U3	U2	U1	U0
	0	0	0	0	0	0	0	0	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0
	0	0	0	0	0	0	0	0	V7	V6	V5	V4	V3	V2	V1	V0
	0	0	0	0	0	0	0	0	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0

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8.2.4.3.4 ISS CCP2 Data Compression

The data compression technique used is DPCM and pulse code modulation (PCM).

The CCP2 receiver performs on-the-fly compression and decompression. The compressed/decompressed data is passed to the video preprocessing hardware or stored in memory.

The data compression method is lossy and does not require any information outside the current encoded/decoded line. This means that all the image lines can be encoded and decoded separately.

Two different predictors are used:

- The simple predictor

  This predictor uses only the previous same color component value as a prediction value. Therefore, only 2-pixel memory is required.
- The advanced predictor

  This predictor uses four previous pixel values, when the prediction value is evaluated. This means that also the other color component values are used, when the prediction value is defined.

The preferable use is that the simple predictor is used with 10 bits to 8 bits or 12 bits to 8 bits conversion (10810 or 12812) and the advanced predictor is used with 10 bits to 7 bits and 10 bits to 6 bits conversions (10710 and 10610). The advanced predictor gives slightly better prediction for pixel value; thus, the image quality can be improved with it. Because the simple predictor is very simple, the processing power and memory requirements are reduced with it, when the image quality is already high enough.

Select the predictor with the CCP2_LCx_CTRL[10] DPCM_PRED bit.

8.2.4.3.5 ISS CCP2 Memory Read Channel

The memory channel can perform the following operations:

- Reads data from memory. It is unpacked and DPCM or A-Law decompressed if necessary.
- Sends data to the video preprocessing hardware
- Sends data back to memory. It can be DPCM or A-Law compressed and packed before it is sent to memory.

It cannot receive its input data directly from the sensor, and the logical channels are disabled when the memory channel is enabled.

Table 8-56 summarizes supported modes for memory-to-memory operations.

NOTE: Video port and memory destinations are mutually exclusive.

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Table 8-56. ISS CCP2 Memory-to-Memory Supported Operations

Memory Input	Memory Output																					
	RAW 6	RAW 6+PACK	RAW 6+DPCM	RAW 6+PACK+DPCM	RAW 6+DPCM_ADV	RAW 6+PACK+DPCM_ADV	RAW 7	RAW 7+PACK	RAW 7+DPCM	RAW 7+PACK+DPCM	RAW 7+DPCM_ADV	RAW 7+PACK+DPCM_ADV	RAW 8	RAW 8+DPCM	RAW 8+DPCM12	RAW 8+ALAW10	RAW 10	RAW 10+PACK	RAW 12	RAW 12+PACK	RAW 14	RAW 16
RAW6																						
RAW6 + PACK																						
RAW6 + DPCM																	X	X				
RAW6 + PACK + DPCM																	X	X				
RAW6 + DPCM_ADV																	X	X				
RAW6 + PACK + DPMC_ADV																	X	X				
RAW7																						
RAW7 + PACK																						
RAW7 + DPCM																	X	X				
RAW7 + PACK + DPCM																	X	X				
RAW7 + DPCM_ADV																	X	X				
RAW7 + PACK + DPMC_ADV																	X	X				
RAW8																						
RAW8 + DPCM																	X	X				
RAW8 + DPCM12																			X	X		

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Table 8-56. ISS CCP2 Memory-to-Memory Supported Operations (continued)

Memory Input	Memory Output																					
	RAW 6	RAW 6+PACK	RAW 6+DPCM	RAW 6+PACK+DPCM	RAW 6+DPCM_ADV	RAW 6+PACK+DPCM_ADV	RAW 7	RAW 7+PACK	RAW 7+DPCM	RAW 7+PACK+DPCM	RAW 7+DPCM_ADV	RAW 7+PACK+DPCM_ADV	RAW 8	RAW 8+DPCM	RAW 8+DPCM12	RAW 8+ALAW10	RAW 10	RAW 10+PACK	RAW 12	RAW 12+PACK	RAW 14	RAW 16
RAW8 + ALAW10																	X	X				
RAW10			X	X	X	X			X	X	X	X		X								
RAW10 + PACK			X	X	X	X			X	X	X	X		X								
RAW12																						
RAW12 + PACK																						
RAW14																						
RAW16																						

Table 8-57 summarizes supported modes for memory-to-video port operations.

Table 8-57. ISS CCP2 Memory-to-Video Port Supported Formats

Memory Input	Video Port Output						
	RAW6	RAW7	RAW8	RAW10	RAW12	RAW14	RAW16
RAW6				X			
RAW6 + PACK				X			
RAW6 +DPCM				X			
RAW6 + PACK + DPCM				X			
RAW6 + DPCM_ADV				X			
RAW6 + DPCM_ADV + PACK				X			
RAW7				X			
RAW7 + PACK				X			
RAW7 + DPCM				X			
RAW7 + PACK + DPCM				X			
RAW7 + DPCM_ADV				X			
RAW7 + DPCM_ADV + PACK				X			

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Table 8-57. ISS CCP2 Memory-to-Video Port Supported Formats (continued)

Memory Input	Video Port Output						
	RAW6	RAW7	RAW8	RAW10	RAW12	RAW14	RAW16
RAW8				X			
RAW8 + DPCM				X			
RAW8 + DPCM12					X		
RAW10				X			
RAW10 + PACK				X			
RAW12					X		
RAW12 + PACK					X		
RAW14						X	
RAW16							X

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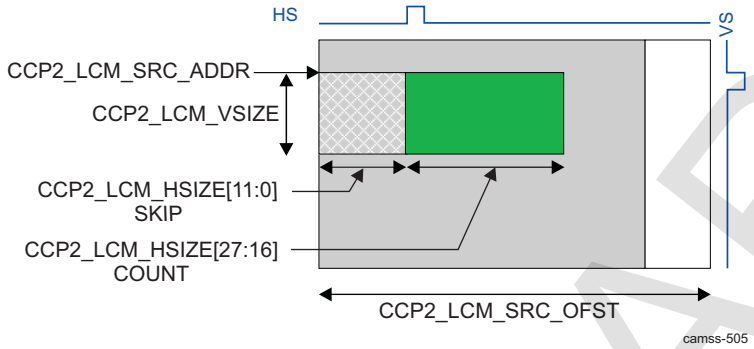
8.2.4.3.5.1 ISS CCP2 Read Data From Memory

Figure 8-29 shows the data organization in memory.

Figure 8-29. ISS CCP2 Data Organization in Memory



The user chooses the start address and the line length using the CCP2_LCM_SRC_ADDR and CCP2_LCM_SRC_OFST registers. The image start address normally must point to the beginning of a line because of packing constraints. However, it does not necessarily point to the first line of the frame in memory. The CCP2_LCM_VSIZE[27:16] COUNT bit field specifies the total line count to be read from memory.

It is also possible to skip a certain pixel count (CCP2_LCM_HSIZE[11:0] SKIP) from the start of the line. Thus, they are not sent to the video port or back to memory. The CCP2_LCM_HSIZE[27:16] COUNT bit field specifies the horizontal size of the image. The pixels after the right boundary of the image are not read from memory.

When data are sent to the video port, throughput is imposed by the selected VP_PCLK. Otherwise, it is imposed by the selected interconnect read port clock. The interconnect read rate can be throttled (limiting the maximum data read speed for memory-to-memory operation) using the CCP2_LCM_CTRL[4:3] READ_THROTTLE bit field. Therefore, it is possible to read the unused data at a higher rate than the used video port data rate. This provides better performance than framing the image in the video preprocessing hardware.

The data storage format in memory is defined by the CCP2_LCM_CTRL[18:16] SRC_FORMAT and CCP2_LCM_CTRL[23] SRC_PACK bit fields.

Not all I/O format combinations are valid. For more information, see Table 8-56 and Table 8-57.

Figure 8-30 shows how data are packed in memory. Pixel order (left to right in the image) is alphabetical (a, b, c). Therefore, data storage is little endian.

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Figure 8-30. ISS CCP2 Data Organization Packing in Memory

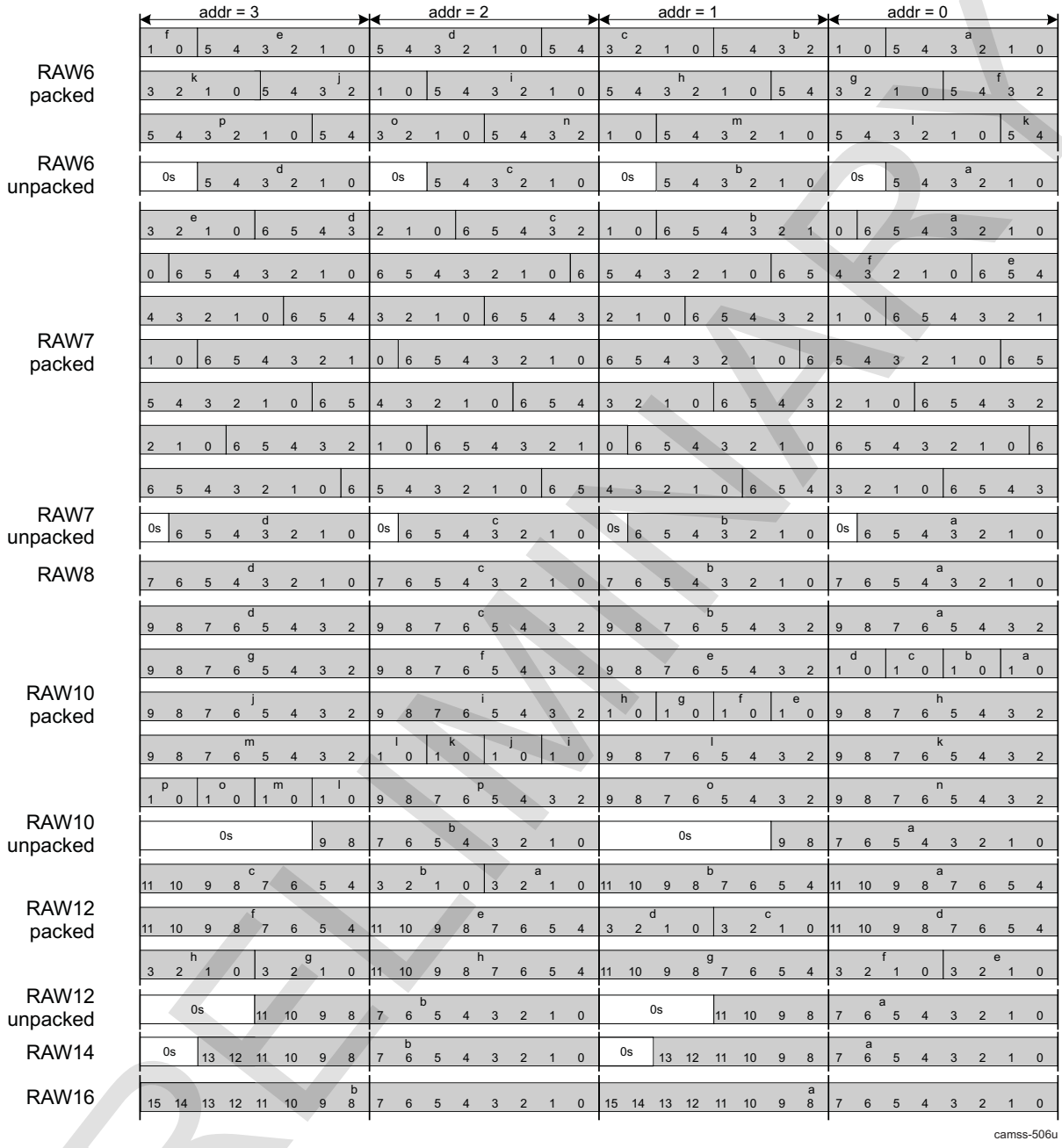

Table 8-58 summarizes the storage reduction versus unpacked format and image width restrictions when data packing is used. The image width applies to the data width multiple in pixels that must be stored to have storage reduction. Moreover, because each address is 8 bits long, the percentage shows how many bits out of 8 are to be packed in the empty space from another pixel address. A pixel is selected and split. One of the parts is put into another pixel address empty space. When unpacked, each pixel bit is stored continuously again.

Table 8-58. ISS CCP2 Data Packing Benefit and Constraints

	Bits Per Pixel		Storage Reduction	Width Multiple (Pixels)
	Packed	Unpacked		
RAW6	6	8	25%	16
RAW7	7	8	13%	3

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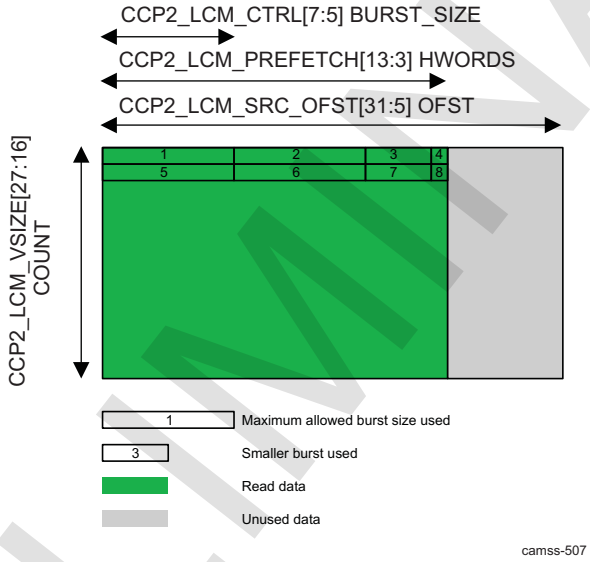
Table 8-58. ISS CCP2 Data Packing Benefit and Constraints (continued)

	Bits Per Pixel		Storage Reduction	Width Multiple (Pixels)
	Packed	Unpacked		
RAW8	8	8	0%	4
RAW10	10	16	38%	16
RAW12	12	16	25%	8

8.2.4.3.5.2 ISS CCP2 Memory Read Port Burst Generation

Hardware always uses the largest possible burst size according to the setup. The amount of data read from memory can be higher than what is actually used by the CCP2 receiver. Only full 64-bit burst words are read back from memory. Figure 8-31 shows the data organization and the relationship between the different parameters controlling the burst generation.

Figure 8-31. ISS CCP2 Data Organization in Memory



NOTE:

- A minimum burst size of 2 must be selected for correct operation.
- The HWORDS bit field must be even for correct operation.

The CCP2_LCM_SRC_ADDR register address of the first data to read is aligned to a 32-byte boundary. The read port fetches CCP2_LCM_PREFETCH[13:3] HWORDS of 64-bit words per line using the longest possible burst computed from the CCP2_LCM_CTRL[7:5] BURST_SIZE bit field and the remaining data to be fetched. Burst size of 128 bytes is preferred. When the CCP2 receiver is configured to fetch more data than required, extra data are dropped internally.

8.2.4.3.5.3 ISS CCP2 Video Port

The video port always receives unpacked data. It can be enabled using the CCP2_LCM_CTRL[2] DST_PORT bit. Its clock can be selected with the CCP2_CTRL[31:15] FRACDIV bit field and gated or not during frame blanking periods using the CCP2_CTRL[9] VP_CLK_FORCE_ON bit.

The data format used by the video port is defined by the CCP2_LCM_CTRL[26:24] DST_FORMAT bit field. For a list of supported modes, see Table 8-57.

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8.2.4.3.5.4 ISS CCP2 Encode, Pack, and Store Data

This stage is used only when data are sent to memory. Memory destination is selected using the CCP2_LCM_CTRL[2] DST_PORT bit. The output data format is defined by the CCP2_LCM_CTRL[26:24] DST_FORMAT bit field and the CCP2_LCM_CTRL[31] DST_PACK bit. Not all possible combinations are supported; see Table 8-56 for details.

The destination address and offset for the output data of the memory channel are set by the CCP2_LCM_DST_ADDR and CCP2_LCM_DST_OFST registers.

Because of alignment constraints on the interconnect port, the output image width restrictions in Table 8-59 apply.

Table 8-59. ISS CCP2 Output Width Restrictions in Memory-to-Memory Operation

Format	Bits per Pixel	Width Multiple of (1)	Note
RAW6	8	1	Full 32-bit words are written at the end of the line. This last word can eventually include 0s.
RAW6 packed	6	1	
RAW7	8	1	
RAW7 packed	7	1	
RAW8	8	1	
RAW10	16	1	
RAW10 packed	10	16	
RAW12	16	1	Same constraints as RAW8
RAW12 packed	12	8	

(1) In continuous mode, lines must be multiples of 128 bits. In 2D mode, lines must start on 128-bit boundaries.

For example, when RAW6 packed data are written to memory, any output width is allowed. However, only full 32-bit words are written to memory. This eventually overwrites some data in memory at the end of a line.

The supported output width is restricted for packed RAW10 and RAW12 data because of the particular bit ordering in those formats (see Figure 8-30).

When the DST_OFST bit is set to 0, start of lines are aligned on 4-byte boundaries. When DST_OFST is not set to 0, data are aligned on 32-byte boundaries.

NOTE: The RAW6, RAW7, and DPCM data formats do not apply to the MIPI CSI1-compatible mode.

8.2.4.3.5.5 ISS CCP2 DPCM Decompression History

The DPCM compression algorithm can encode the difference between consecutive samples in a line instead of the actual samples value to reduce the amount of data to store. The drawback is that lines must always be decoded from the beginning (the first samples of a line are always encoded as PCM).

The CCP2 receiver has a mechanism to preserve the DPCM decode history for each line to avoid decoding the same samples multiple times when vertical frame division mode is used.

The typical use case (also known as vertical frame division mode) is when an image is wider than the ISP can process on the fly, but the image must be processed. Therefore, the image is cut into multiple vertical slices that are processed sequentially by the ISP. The slices are stitched together in the SDRAM through proper address generation in the ISP. Because of various alignment constraints in the ISP, the slices must overlap. Without preserving the DPCM history, all lines from the beginning of the second (and other consecutive) vertical slice would have to be recoded, which would lead to performance degradation.

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Writing DPCM history information into the system memory is enabled by setting the CCP2_LCM_HISTORY[16] EN_HIST_WR bit. The CCP2_LCM_HISTORY[15:0] HIST_EXPORT bit field defines the position at which history data is written to memory. The position is counted from the beginning line. The first decoded pixel has position 0. The last decoded pixel has position CCP2_LCM_HSIZE[14:0] SKIP + CCP2_LCM_HSIZE[30:16] COUNT. The CCP2_LCM_HISTORY[15:0] HIST_EXPORT bit field is used to choose the resume position and allows support of overlapping vertical slices. History data is written to the SDRAM at ADDR = CCP2_LCM_DST_ADDR[31:5] ADDR + Y × 8 bytes (where Y is the line number). The CCP2 receiver always writes 8 bytes of history data per line to the SDRAM regardless of the chosen DPCM format. The CCP2 receiver uses the interface bursts to send history data to memory.

DPCM history data holds the decoded value of four samples. The CCP2 receiver exports samples of positions:

- CCP2_LCM_HISTORY[15:0] HIST_EXPORT – 3
- CCP2_LCM_HISTORY[15:0] HIST_EXPORT – 2
- CCP2_LCM_HISTORY[15:0] HIST_EXPORT – 1
- CCP2_LCM_HISTORY[15:0] HIST_EXPORT

Every sample is coded on 16 bits, and several MSBs are unused. The valid range for CCP2_LCM_HISTORY[15:0] HIST_EXPORT is [3.. CCP2_LCM_HSIZE[14:0] SKIP + CCP2_LCM_HSIZE[30:16] COUNT – 1]. History data can be exported even when data is not sent to the video port (CCP2_LCM_HISTORY[15:0] HIST_EXPORT CCP2_LCM_HSIZE[14:0] SKIP is valid).

8.2.4.4 ISS CCP2 Programming Model

This section describes the programming model of the CCP2 receiver.

8.2.4.4.1 ISS CCP2 Programming Hardware Setup/Initialization

This section discusses the configuration of the CCP2 receiver required before image capture can begin. Before using the receiver, a CSIPHY initialization in CCP2 mode must be made for CSI2-B/CCP2 CAMERARX, which is associated with the CCP2 receiver. See Section 8.2.3.2.3, *ISS CCP2 and Link Initialization Sequence.*

NOTE: The setup/initialization previously explained is valid only when the external sensor is used. If the user plans to use the logical memory channel (LCM) or debug mode (CCP2_CTRL[13] DBG_EN = 0x1) instead of the external sensor, this setup/initialization is not necessary.

8.2.4.4.1.1 ISS CCP2 Reset Behavior

On hardware or software reset of the ISS, all registers in the CCP2 receiver are reset to their reset values.

The two sources for CCP2 software reset are:

- Global reset for the whole ISS – ISS_HL_SYSCONFIG[0] SOFTRESET bit
- Local reset, affecting only the CCP2 module. The reset is initiated by writing 0x1 in the CCP2_SYSCONFIG[1] SOFT_RESET bit. The reset done status can be check by reading the CCP2_SYSSTATUS[0] RESET_DONE bit.

8.2.4.4.2 ISS CCP2 Programming Event and Status Checking

When an event occurs, the corresponding bit in the CCP2_LC01_IRQSTATUS, CCP2_LC23_IRQSTATUS, or CCP2_LCM_IRQSTATUS register is set. Each event can be individually masked using the CCP2_LC01_IRQENABLE, CCP2_LC23_IRQENABLE, or CCP2_LCM_IRQENABLE register. Masked events are not transmitted to the interrupt line, but the CCP2_LC01_IRQSTATUS, CCP2_LC23_IRQSTATUS, or CCP2_LCM_IRQSTATUS register is updated.

Events transmitted to the ISS interrupt merger can be mapped to the Cortex-A9 or Cortex-M3 MPU

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subsystem or DSP by unmasking ISS_HL_IRQENABLE_SET_i[] CCP2_IRQj (where i = 0 to 5, j = 0, 1, 2, 3, and 8). Only the ISS_HL_IRQENABLE_SET_5 output line is connected to the Cortex-A9 MPU interrupt controller, and only the ISS_HL_IRQENABLE_SET_4 output line is connected to the DSP interrupt controller. The Cortex-M3 interrupt controller, however, is connected to all six output lines of ISS_HL_IRQENABLE_SET_i (where i = 0 to 5). To clear an event, the following actions are required:

- Clear the event at the CCP2 receiver level by writing 1 to the corresponding bit in the CCP2_LC01_IRQSTATUS, CCP2_LC23_IRQSTATUS or CCP2_LCM_IRQSTATUS register.
- Events generated by the submodules and ISS top level clear it. Each event that generates an interrupt can be individually enabled by setting the appropriate bit in the ISS_HL_IRQENABLE_SET_i register. It is disabled by setting the appropriate bit in the ISS_HL_IRQENABLE_CLR_i register. When an event occurs, the corresponding bit in the ISS_HL_IRQSTATUS_i register is set, regardless of whether or not the event is enabled. Bits in the ISS_HL_IRQSTATUS_i registers are set only when an enabled event occurs. Software can clear a pending HS_VS_IRQ event by setting the appropriate bit ISS_HL_IRQSTATUS[17] HS_VS_IRQ. Events generated by submodules are automatically cleared at ISS top level when they are cleared at submodule level.

8.2.4.4.3 ISS CCP2 Programming Register Accessibility During Frame Processing

There are two types of register accesses in the CCP2 receiver:

- Shadowed registers:
  - These registers/fields can be read and written (if the field is writable) at any time. However, written values take effect only at the start of a frame. Reads return the most-recent write, even though the settings are not used until the next start of frame.
  - The shadowed registers are:
    - CCP2_LCx_CTRL
    - CCP2_LCx_CODE
    - CCP2_LCx_STAT_START
    - CCP2_LCx_STAT_SIZE
    - CCP2_LCx_SOF_ADDR
    - CCP2_LCx_EOF_ADDR
    - CCP2_LCx_DAT_SIZE
    - CCP2_LCx_DAT_PING_ADDR
    - CCP2_LCx_DAT_PONG_ADDR
    - CCP2_LCx_DAT_OFST
- Busy-locked registers:
  - These registers/fields must not be written if the module is busy.
  - All register fields not listed as shadowed are busy-writable registers.

8.2.4.4.4 ISS CCP2 Programming Enable/Disable the Hardware

The CCP2 receiver is globally controlled by the CCP2_CTRL register. The bit fields in this register must not be modified when the CCP2 interface is active (except CCP2_CTRL[0] IF_EN).

Table 8-60 and Table 8-61 list the procedures to enable and disable, respectively, the interface.

Table 8-60. ISS CCP2 Interface Enable

Step	Bit Field	Value
Clear the interface. Data acquisition starts on the following FSC synchronization code.	CCP2_CTRL[0] IF_EN	0x1
Reset the output FIFO of the module; the reset is caused by the 0-to-1 edge transition.	CCP2_CTRL[0] IF_EN	0x1

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Table 8-61. ISS CCP2 Interface Disable

Step	Bit Field	Value
Disable interface. • The interface is disabled immediately if CCP2_CTRL[3] FRAME = 0x0. • If CCP2_CTRL[3] FRAME = 0x1 and CCP2_LCx_CTRL[2] CRC_EN = 0x0, the interface is disabled after the FEC synchronization code is received. • If CCP2_CTRL[3] FRAME = 0x1 and CCP2_LCx_CTRL[2] CRC_EN = 0x1, the interface is disabled only after the 16-bit CRC checksum and 16-bit pad data is received. • Before disabling the interface (IF_EN = 0), it is advised to disable all active channels by writing CCP2_LCx_CTRL[0] CHAN_EN = 0x0. Otherwise, if IF_EN = 0 is set during a vertical blanking period, the reception continues until the FEC synchronization code is received for all active channels.	CCP2_CTRL[0] IF_EN	0x0

8.2.4.4.5 ISS CCP2 Programming Select the Signaling Scheme

Table 8-62 lists the procedure to select the signaling scheme.

Table 8-62. ISS CCP2 Select the Signaling Scheme

Step	Bit Field	Value
Selects whether the data/strobe or data/clock signaling scheme is used. For the correct settings as a function of the image sensor class, see Section 8.2.3, *ISS CSI2 PHY*. This setting must also be configured in the control module.	See Section 8.2.3, *ISS CSI2 PHY*. For the register and bit field, see Chapter 18, *Control Module* (CONTROL_CAMERA_RX register).	0x0: Data/clock 0x1: Data/strobe

8.2.4.4.6 ISS CCP2 Programming Select the Mode: MIPI CSI1 or CCP2

Table 8-63 lists the procedure to select MIPI CSI1 or CCP2 mode.

Table 8-63. ISS CCP2 Select MIPI CSI1 or CCP2 Mode

Step	Bit Field	Value
Selects whether the CCP2 module works in MIPI CSI1 or CCP2-compatible mode	CCP2_CTRL[4] MODE	0x0: Disables the CCP2-specific features (data/strobe, CRC, logical channels, RAW6, RAW7, and DPCM data formats) 0x1: CCP2 mode

8.2.4.4.7 ISS CCP2 Programming Burst Settings

Table 8-64 lists the procedure to configure the burst settings.

Table 8-64. ISS CCP2 Configure Burst Settings

Step	Bit Field	Value
The module can be forced to perform single 64-bit requests or bursts of 2x, 4x, 8x, and 16 x 64 bits. The module must always use 16 x 64. The FIFO size is 64 x 64 bits.	CCP2_CTRL[6:5] BURST CSI2_CTRL[16] BURST_SIZE_EXPAND	0x0: Single request. 0x1: 2 x 64-bit bursts 0x2: 4 x 64-bit bursts 0x3: 8 x 64-bit bursts 0x4: 16 x 64-bit bursts (with burst expand)

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Table 8-64. ISS CCP2 Configure Burst Settings (continued)

Step	Bit Field	Value
Enable 128 bytes (recommended setting) of the DMA CSI2/CCP DMA engine to burst 128 bytes over the L3 interconnect.	CSI2_CTRL[16] BURST_SIZE_EXPAND	0x0: Use the burst size defined in the BURST_SIZE bit field. 0x1: Allow generation of 16 x 64-bit bursts.

8.2.4.4.8 ISS CCP2 Programming Debug Mode

Table 8-65 lists the procedure to enable debug mode.

Table 8-65. ISS CCP2 Enable Debug Mode

Step	Bit Field	Value
Enable debug mode.	CCP2_CTRL[13] DBG_EN	0x1

- During debug mode, the input comes from the CCP2_DBG register, not from the CCP2 physical interface. The full CCP2 receiver function can be debugged in debug mode. Full 32-bit values must always be written to the CCP2_DBG register.
- The following bit has no effect during debug mode:
  - CCP2_CTRL[0] IF_EN
- The following examples apply to the CCP2_DBG register:
  - Synchronization codes: CCP2_DBG = 0xFF000000 (LSC) or 0xFF00001 (LEC) or 0xFF00002 (FSC) or 0xFF000003 (FEC)
  - To send the RAW12 pixels 0x673, 0x452, 0x01d, 0xefc, 0xab0, 0x891, 0x326, and 0x547, write CCP2_DBG = 0x01234567 followed by CCP2_DBG = 0x89abcdef and CCP2_DBG = 0x76543210.

NOTE: Each write to the CCP2_DBG register sends a full 32-bit word through the CCP2 receiver hardware. When 8- or 16-bit writes are performed to the register, the previous 32-bit value is merged with the newly written one. When the driver writes, for example, 0x01234567 followed by 0x0000 00FF the MPU subsystem informs that only 8 bits are written), the CCP2 receiver pipeline gets 0x01234567 followed by 0x012345FF.

8.2.4.4.9 ISS CCP2 Programming Video Port

Table 8-66 lists the procedure to configure the video port.

Table 8-66. ISS CCP2 Configure Video Port

Step	Bit Field	Value
Set the video port output frequency. It varies from ISS_FLCK down to ISS_FLCK/65,536 MHz.	CCP2_CTRL[31:15] FRACDIV	From 1 to 65,536
Enable video port clock during vertical blanking periods or not.	CCP2_CTRL[9] VP_CLK_FORCE_ON	0x0: The video port clock is gated during vertical blanking periods. 0x1: The video port clock is free-running during vertical blanking periods.

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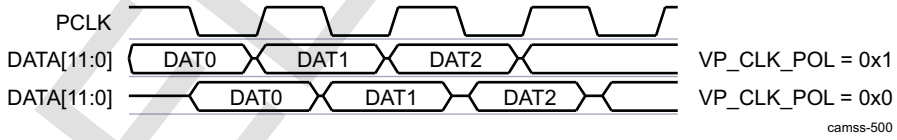
Table 8-66. ISS CCP2 Configure Video Port (continued)

Step	Bit Field	Value
Controls whether the video-port output is the only output interface enabled and applies for all channels. When CCP2_CTRL[11] VP_ONLY_EN = 0x1, the data are output only to the video port; the interface master port is not used. The two parts of the frame (embedded data and pixel data) are output to the video port (instead of pixel data to the video port and embedded data to the interconnect). • The video port outputs the embedded data defined by the CCP2_LCx_STAT_START and CCP2_LCx_STAT_SIZE registers without decompression. • The video port outputs the pixel data defined by the CCP2_LCx_DAT_START and CCP2_LCx_DAT_SIZE registers.	CCP2_CTRL[11] VP_ONLY_EN	
Control the video port pixel clock polarity: (Recommended setting: rising edge)	CCP2_CTRL[12] VP_CLK_POL	0x0: The CCP2 receiver writes the data on the video port on the pixel-clock falling edge. The module connected to the video port samples the data on the pixel clock rising edge. 0x1: The CCP2 receiver writes the data on the video port on the pixel-clock rising edge. The module connected to the video port samples the data on the pixel clock falling edge. Figure 8-32 shows the settings for CCP2_CTRL.VP_CLK_POL.

Figure 8-32 shows the settings for CCP2_CTRL.VP_CLK_POL.

Figure 8-32. CCP2_CTRL.VP_CLK_POL Settings



8.2.4.4.10 ISS CCP2 Programming Logical Channels

The CCP2 receiver supports simultaneous logical channels. Each logical channel is controlled independently with its own set of registers. The four sets of registers are identical, but some reset values are different.

The same description applies to all four logical channels (LCx, where x = 0 to 3).

All the registers in this section can be modified at any time. However, the modifications apply only from the start of the following frame.

8.2.4.4.11 ISS CCP2 Programming Controls

Table 8-67 lists the procedure to enable the logical channels.

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Table 8-67. ISS CCP2 Enable Logical Channels

Step	Bit Field	Value
Enable logical channels. It has no effect if CCP2_CTRL[4] MODE = 0x0. By default, all logical channels except logical channel 0 are disabled. Only the pixel data of one logical channel can go to the video preprocessing hardware; the SOF and EOF lines are always sent to memory through the interconnect interface.	CCP2_LCx_CTRL[0] CHAN_EN	0x1

8.2.4.4.12 ISS CCP2 Programming Region-of-Interest

Table 8-68 lists the procedure to enable the region-of-interest.

Table 8-68. ISS CCP2 Enable Region-of-Interest

Step	Bit Field	Value
Enables the region-of-interest feature (SOF lines, pixel data, and EOF lines): • If enabled, register settings set the position and size of each region; all data not in a region of interest are ignored. • If disabled, all data in the frame are output. CCP2_LCx_CTRL[1] REGION_EN is set to 0x0 for a JPEG bitstream.	CCP2_LCx_CTRL[1] REGION_EN	0x1

8.2.4.4.13 ISS CCP2 Programming CRC

Table 8-69 lists the procedure to enable the CRC.

Table 8-69. ISS CCP2 Enable the CRC

Step	Bit Field	Value
Enable the CRC. If the received checksum and the computed checksum do not match, an interrupt is triggered: the corresponding event is LCx_CRC_IRQ. Setting CCP2_LCx_CTRL[2] CRC_EN = 0x1 has no effect if CCP2_CTRL[4] MODE = 0x0.	CCP2_LCx_CTRL[2] CRC_EN	0x1

8.2.4.4.14 ISS CCP2 Programming Destination Format

Control the destination format:

- The CCP2 receiver reformats received data to store it in memory or to send it to the video preprocessing.
- The CCP2_LCx_CTRL[7:3] FORMAT bit field controls the destination-data format:
  - EXP8 = Data expansion to 8 bits, padding with zeros
  - EXP16 = Data expansion to 16 bits, padding with alpha or zeros. The CCP2_CTRL[15:8] ALPHA bit field can be used to set an alpha value. For RGB444 + EXP16:
    - data_out [31:28] = ALPHA [3:0]
    - data_out [15:12] = ALPHA [3:0]
  - EXP32 = Data expansion to 32 bits, padding with alpha. The CCP2_CTRL[15:8] ALPHA bit field can be used to set an alpha value. For RGB888 + EXP32: data_out [31:24] = ALPHA [7:0]
  - FSP = False synchronization protection code decoding. Applies only to JPEG8 data format.
  - VP = Output to video preprocessing is enabled.

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8.2.4.4.15 ISS CCP2 Programming Frame Acquisition

Table 8-70 lists the procedure to acquire frames.

Table 8-70. ISS CCP2 Frame Acquisition

Step	Bit Field	Value
Program the number of frames that the CCP2 receiver acquires. The value of COUNT is decremented after each frame received.	CCP2_LCx_CTRL[31:24] COUNT	0: The counter is free-running (default value). 1255: Remaining frames to be acquired
Writes to the COUNT bit field are controlled by the COUNT_UNLOCK bit.	CCP2_LCx_CTRL[16] COUNT_UNLOCK	
Configures PING and PONG addresses	CCP2_LCx_DAT_PING_ADDR and CCP2_LCx_DAT_PONG_ADDR	
Indicates whether the PING address or PONG address was used to store the pixel data of the last frame. After reset or after a 0-to-1 edge transition in CCP2_CTRL[0] IF_EN, the pixel data are written in the PING buffer and CCP2_LCx_CTRL[17] PING_PONG = 0x1 (PONG). After the first FEC synchronization code is received, the pixel data are written in the PONG buffer and CCP2_LCx_CTRL[17] PING_PONG = 0x0 (PING). CCP2_LCx_CTRL[17] PING_PONG toggles after every FEC synchronization code.	CCP2_LCx_CTRL[17] PING_PONG	

After the correct number of frames is received, acquisition is automatically disabled (CCP2_LCx_CTRL[0] CHAN_EN = 0x0) and the COUNT_IRQ interrupt is triggered. The programmer can re-enable the acquisition by resetting the CCP2_LCx_CTRL[0] CHAN_EN bit to 0x1.

8.2.4.4.16 ISS CCP2 Programming Synchronization Codes

The FSC, FEC, LSC, and LEC synchronization codes have default values given by the *SMIA CCP2 Specification v1.0*. Also, each logical channel is identified by a default identifier.

The CCP2_LCx_CODE register enables overwriting of the default values: CCP2_LCx_CODE[11:8] FSC, CCP2_LCx_CODE[15:12] FEC, CCP2_LCx_CODE[3:0] LSC, and CCP2_LCx_CODE[7:4] LEC overwrite the 4 LSBs of the 32-bit synchronization codes. The default values must not be modified.

8.2.4.4.17 ISS CCP2 Programming Status Data

The SOF and EOF status lines can be output to memory.

The SOF and EOF status lines always cover full lines. No register settings enable the setting of width.

The CCP2_LCx_STAT_START register enables the setting of the vertical start position of the SOF and EOF status lines. Because the SOF status line comes first in the CCP2 frame, CCP2_LCx_STAT_START[11:0] SOF = 0x0.

The CCP2_LCx_STAT_SIZE register enables the setting of the numbers of SOF and EOF status lines. If CCP2_LCx_STAT_SIZE[11:0] SOF = 0x0 and CCP2_LCx_STAT_SIZE[27:16] EOF = 0x0, no status data are output.

Figure 8-33 shows the SOF and EOF region settings. The SOF and EOF status lines and the pixel data must not overlap, but can be consecutive.

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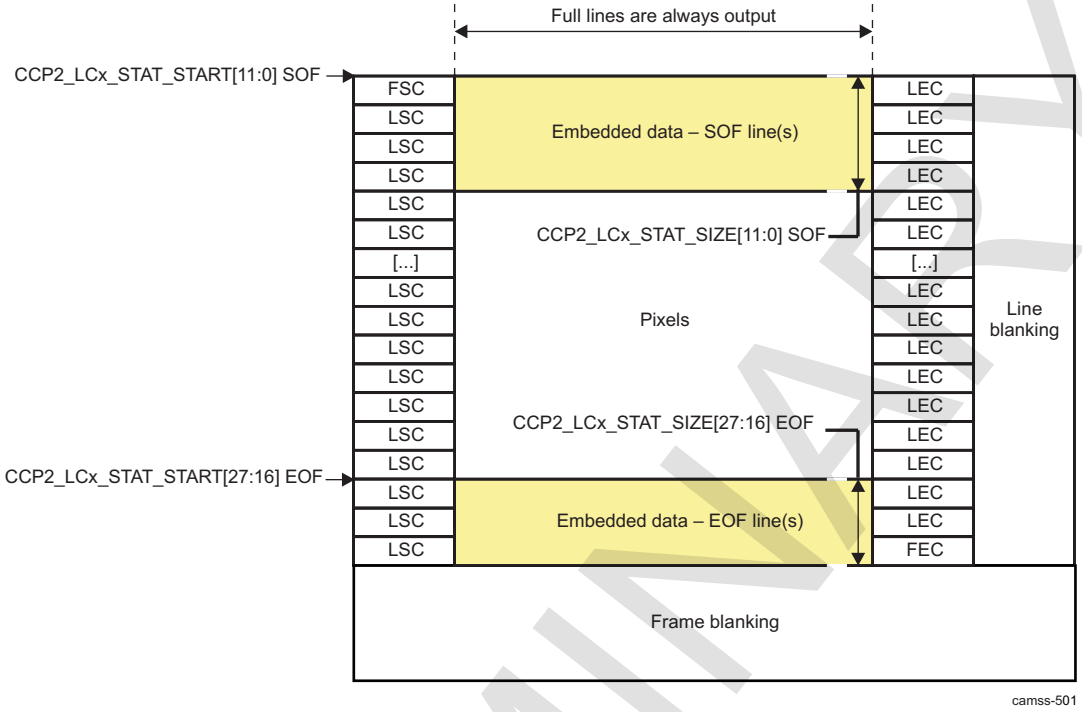
Figure 8-33. ISS CCP2 SOF and EOF Region Settings



The 32-bit destination addresses of the SOF status lines are set by the CCP2_LCx_SOF_ADDR register.

NOTE: The destination addresses of the SOF status lines must be aligned on a 32-byte boundary; the 5 LSBs of the address are ignored. The SOF lines are packed together at the destination address.

The 32-bit destination addresses of the EOF status lines are set by the CCP2_LCx_EOF_ADDR register.

NOTE: The destination addresses of the EOF status lines must be aligned on a 32-byte boundary; the 5 LSBs of the address are ignored. The EOF lines are packed together at the destination address.

NOTE: The CCP2 receiver does not modify the data in the SOF and EOF status lines. The data are received and written with no modifications.

8.2.4.4.18 ISS CCP2 Programming Pixel Data Region

Pixel data can be output to memory or to the video-preprocessing hardware.

The pixel data region covers full lines. The CCP2_LCx_DAT_SIZE register sets the horizontal size of the pixel region. The vertical size is expressed in lines.

The CCP2_LCx_DAT_START register enables the setting of the vertical start position of the pixel data. The vertical start position is expressed in lines.

Figure 8-34 shows the pixel region settings.

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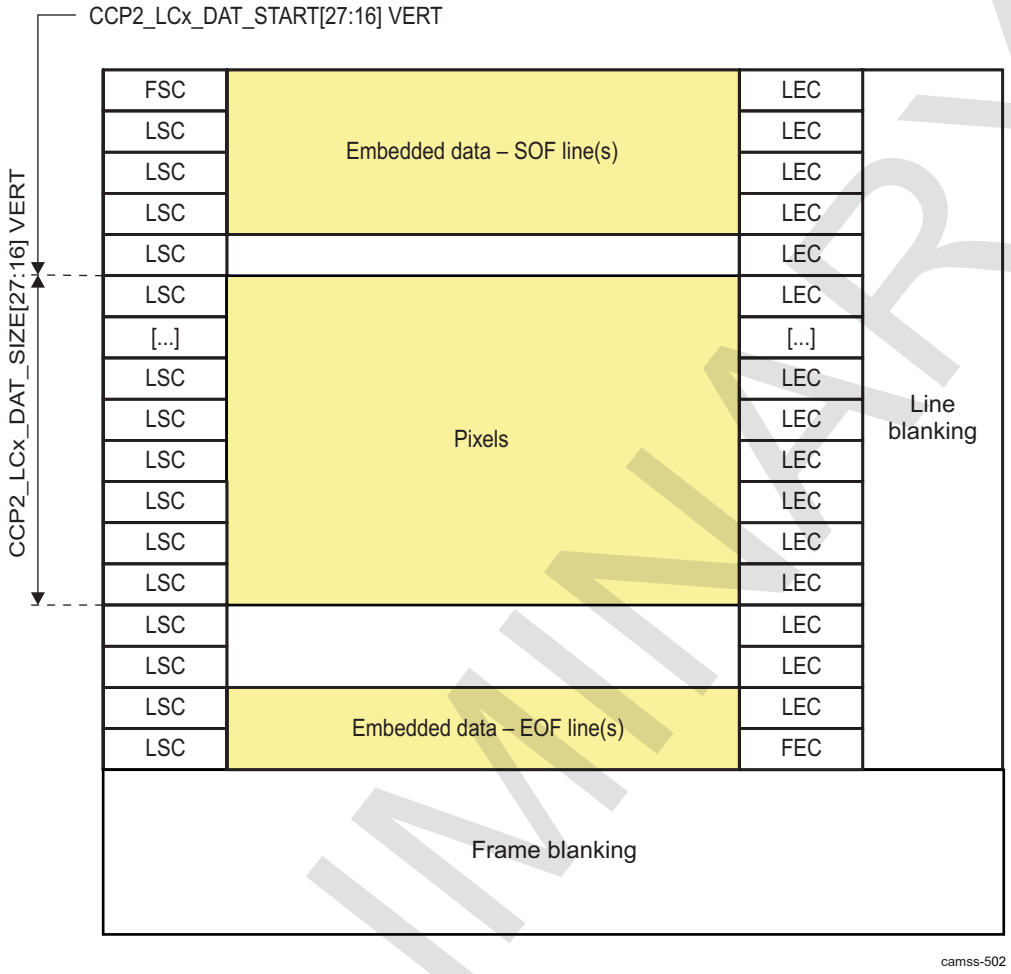
Figure 8-34. ISS CCP2 Pixel Data Region Settings



The 32-bit destination addresses of the pixel data are set by the CCP2_LCx_DAT_PING_ADDR and CCP2_LCx_DAT_PONG_ADDR registers.

NOTE: The destination address must be aligned on a 32-byte boundary; the 5 LSBs of the address are ignored. The pixel data lines are packed together at the destination address.

It is possible to perform double-buffering (ping-ponging) at the destination by setting different addresses in the CCP2_LCx_DAT_PING_ADDR and CCP2_LCx_DAT_PONG_ADDR registers. It is possible to disable double-buffering by setting up the same address in both registers. The CCP2_LCx_CTRL[17] PING_PONG bit must be used by software to determine which address contains the latest frame.

A destination pitch controls the address jump between the address of the first pixel of the previous line and the address of the first pixel of the current line. The destination pitch is set in bytes with the CCP2_LCx_DAT_OFST register. It applies for CCP2_LCx_DAT_PING_ADDR and CCP2_LCx_DAT_PONG_ADDR.

NOTE: The destination pitch must be a multiple of 32 bytes; the 5 LSBs of the address are ignored.

The destination data format is set with the CCP2_LCx_CTRL[7:2] FORMAT bit field.

For the PING frame:

- @Line0 = CCP2_LCx_DAT_PING_ADDR
- @Line1 = @Line0 + CCP2_LCx_DAT_OFST

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- @Line2 = @Line1 + CCP2_LCx_DAT_OFST

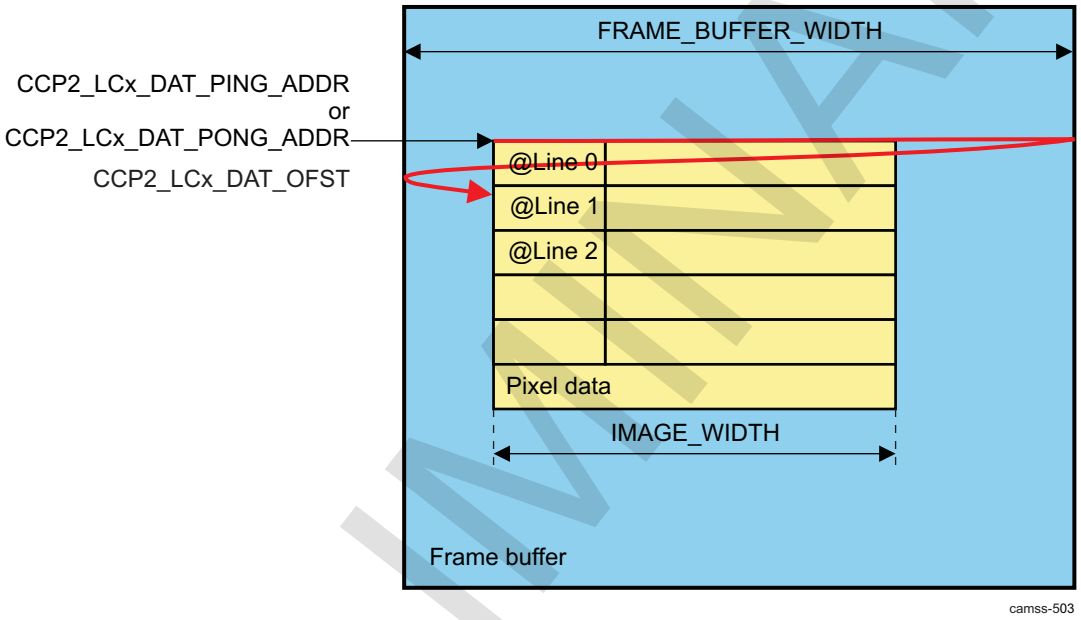
For the PONG frame:

- @Line0 = CCP2_LCx_DAT_PONG_ADDR
- @Line1 = @Line0 + CCP2_LCx_DAT_OFST
- @Line2 = @Line1 + CCP2_LCx_DAT_OFST

When CCP2_LCx_DAT_OFST = 0x0, the lines are written contiguously in memory. The destination pitch enables 2D transfers; it is required to write the pixel data directly in the frame buffer, for instance.

In such cases, CCP2_LCx_DAT_OFST = FRAME_BUFFER_WIDTH. Figure 8-35 shows the pixel data destination settings.

Figure 8-35. ISS CCP2 Pixel Data Destination Settings



8.2.4.4.19 ISS CCP2 Programming Memory Read Channel

8.2.4.4.19.1 ISS CCP2 Write Data From Sensor to Memory

Data can be captured from the sensor using any logical channel. To keep the native data format, the channel format must be set to YUV4:2:2 little-endian format.

8.2.4.4.19.2 ISS CCP2 Read Data From Memory

Table 8-71 lists the procedure to configure read data from memory.

Table 8-71. ISS CCP2 Configure Read Data From Memory

Step	Bit Field	Value
Disable all logical channels.	CCP2_CTRL[0] IF_EN	0x0
Wait until disabling of the physical interface is effective before enabling the memory read channel.	CCP2_CTRL[3] FRAME	0x1
Configure the burst siz .The recommended value for best performance is 0x4 (16 × 64-bit burst).	CCP2_LCM_CTRL[7:5] BURST_SIZE	–

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Table 8-71. ISS CCP2 Configure Read Data From Memory (continued)

Step	Bit Field	Value
Configure the source data format, location, and framing. In addition to the CCP2_LCM_HSIZE[11:0] SKIP and CCP2_LCM_HSIZE[27:16] COUNT bit fields, firmware must specify the amount of data to be fetched from memory. This value is set in 64-bit word steps and must be a multiple of 32 bytes (four words of 64 bits). The value is computed with the following formula: HWORDS = 4 × ceil(((SKIP + COUNT) x bits_per_pixel)/(8 × 32)) (3) The CCP2_LCM_SRC_ADDR and CCP2_LCM_SRC_OFST registers must be aligned on 32-byte boundaries for correct operation. For best performance, both registers must be aligned on 256-byte boundaries. See the example following this table.	CCP2_LCM_CTRL, CCP2_LCM_HSIZE, CCP2_LCM_VSIZE, CCP2_LCM_PREFETCH, CCP2_LCM_SRC_ADDR, CCP2_LCM_SRC_OFST	
Select destination.	CCP2_LCM_CTRL[2] DST_PORT	0x0: Video port 0x1: Memory
If destination = video port, configure clock frequency and its gating during frame blanking periods.	CCP2_CTRL[31:15] FRACDIV, CCP2_CTRL[9] VP_CLK_FORCE_ON	
If needed, configure READ_THROTTLE to reduce the bandwidth in memory-to-memory operation to prevent system overload. It has no effect when data are sent to the video port (controlled by video port clock in this case).	CCP2_LCM_CTRL[4:3] READ_THROTTLE	
If the memory write port is used, the destination format and address must be configured.	CCP2_LCM_DST_ADDR, CCP2_LCM_DST_OFST	
Enable memory read channel. After processing a full frame, this bit is automatically cleared by hardware and an EOF event is triggered.	CCP2_LCM_CTRL[0] CHAN_EN	0x1

Example:

- CCP2_LCM_CTRL[7:5] BURST_SIZE is set to 16 × 64 bits
- CCP2_LCM_HSIZE[11:0] SKIP = 0
- CCP2_LCM_HSIZE[27:16] COUNT = 1000
- CCP2_LCM_CTRL[23] SRC_PACK = YES
- CCP2_LCM_CTRL[18:16] SRC_FORMAT = RAW6
- CCP2_LCM_PREFETCH[13:3] HWORDS = 96 (=94)
  Setting the size to 94 produces the following burst sequence: 16, 16, 16, 16, 16, 8, and 4 (7 interconnect requests). However, when it is set to 96, the burst sequence is 6 × 16 (6 interconnect requests).

8.2.4.5 ISS CCP2 Register Manual

8.2.4.5.1 ISS CCP2 Instance Summary

Table 8-72 summarizes the CCP2 instance.

Table 8-72. ISS CCP2 Instance Summary

Module Name	L3 Base Address	Size
ISS_CCP2	0x5200 1C00	512 bytes

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8.2.4.5.2 ISS CCP2 Registers

8.2.4.5.2.1 ISS CCP2 Register Summary

Table 8-73 lists the CCP2 registers.

Table 8-73. ISS CCP2 Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	ISS_CCP2 Base Address
CCP2_REVISION	R	32	0x0000 0000	0x5200 1C00
CCP2_SYSCONFIG	RW	32	0x0000 0004	0x5200 1C04
CCP2_SYSSTATUS	R	32	0x0000 0008	0x5200 1C08
CCP2_LC01_IRQENABLE	RW	32	0x0000 000C	0x5200 1C0C
CCP2_LC01_IRQSTATUS	RW	32	0x0000 0010	0x5200 1C10
CCP2_LC23_IRQENABLE	RW	32	0x0000 0014	0x5200 1C14
CCP2_LC23_IRQSTATUS	RW	32	0x0000 0018	0x5200 1C18
CCP2_LCM_IRQENABLE	RW	32	0x0000 002C	0x5200 1C2C
CCP2_LCM_IRQSTATUS	RW	32	0x0000 0030	0x5200 1C30
CCP2_CTRL	RW	32	0x0000 0040	0x5200 1C40
CCP2_DBG	W	32	0x0000 0044	0x5200 1C44
CCP2_GNQ	R	32	0x0000 0048	0x5200 1C48
CCP2_CTRL1	RW	32	0x0000 004C	0x5200 1C4C
CCP2_LCx_CTRL (1)	RW	32	0x0000 0050 + (x * 0x30)	0x5200 1C50 + (x * 0x30)
CCP2_LCx_CODE (1)	RW	32	0x0000 0054 + (x * 0x30)	0x5200 1C54 + (x * 0x30)
CCP2_LCx_STAT_START (1)	RW	32	0x0000 0058 + (x * 0x30)	0x5200 1C58 + (x * 0x30)
CCP2_LCx_STAT_SIZE (1)	RW	32	0x0000 005C + (x * 0x30)	0x5200 1C5C + (x * 0x30)
CCP2_LCx_SOF_ADDR (1)	RW	32	0x0000 0060 + (x * 0x30)	0x5200 1C60 + (x * 0x30)
CCP2_LCx_EOF_ADDR (1)	RW	32	0x0000 0064 + (x * 0x30)	0x5200 1C64 + (x * 0x30)
CCP2_LCx_DAT_START (1)	RW	32	0x0000 0068 + (x * 0x30)	0x5200 1C68 + (x * 0x30)
CCP2_LCx_DAT_SIZE (1)	RW	32	0x0000 006C + (x * 0x30)	0x5200 1C6C + (x * 0x30)
CCP2_LCx_DAT_PING_ADDR (1)	RW	32	0x0000 0070 + (x * 0x30)	0x5200 1C70 + (x * 0x30)
CCP2_LCx_DAT_PONG_ADDR (1)	RW	32	0x0000 0074 + (x * 0x30)	0x5200 1C74 + (x * 0x30)
CCP2_LCx_DAT_OFST (1)	RW	32	0x0000 0078 + (x * 0x30)	0x5200 1C78 + (x * 0x30)
CCP2_LCM_CTRL	RW	32	0x0000 01D0	0x5200 1DD0
CCP2_LCM_VSIZE	RW	32	0x0000 01D4	0x5200 1DD4
CCP2_LCM_HSIZE	RW	32	0x0000 01D8	0x5200 1DD8
CCP2_LCM_PREFETCH	RW	32	0x0000 01DC	0x5200 1DDC
CCP2_LCM_SRC_ADDR	RW	32	0x0000 01E0	0x5200 1DE0
CCP2_LCM_SRC_OFST	RW	32	0x0000 01E4	0x5200 1DE4
CCP2_LCM_DST_ADDR	RW	32	0x0000 01E8	0x5200 1DE8
CCP2_LCM_DST_OFST	RW	32	0x0000 01EC	0x5200 1DEC
CCP2_LCM_HISTORY	RW	32	0x0000 01F0	0x5200 1DF0

(1) x = 0 to 3

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8.2.4.5.2.2 ISS CCP2 Register Description

Table 8-74 through Table 8-139 describe the CCP2 registers.

Table 8-74. CCP2_REVISION

Address Offset	0x0000 0000		
Physical Address	0x5200 1C00	**Instance**	ISS_CCP2
Description	IP Revision Identifier (X.Y.R) Used by software to track features, bugs, and compatibility		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP revision	R	See(1)

(1) TI internal data

Table 8-75. Register Call Summary for Register CCP2_REVISION

ISS Interfaces
- ISS CCP2 Registers: [0]

Table 8-76. CCP2_SYSCONFIG

Address Offset	0x0000 0004		
Physical Address	0x5200 1C04	**Instance**	ISS_CCP2
Description	SYSTEM CONFIGURATION REGISTER This register is the OCP-socket system configuration register.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																		MSTANDBY_MODE		RESERVED										SOFT_RESET	AUTO_IDLE

Bits	Field Name	Description	Type	Reset
31:14	RESERVED		R	0x00000
13:12	MSTANDBY_MODE	Sets the behavior of the master port power management signals. 0x0: Force-standby. MStandby is only asserted when the module is disabled. 0x1: No-standby. MStandby is never asserted. 0x2: Smart-standby: MStandby is asserted based on the activity of the module. The module will try to go to standby during the vertical blanking period.	RW	0x0
11:2	RESERVED		R	0x000

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Bits	Field Name	Description	Type	Reset
1	SOFT_RESET	Software reset. Set the bit to 1 to trigger a module reset. The bit is automatically reset by the hardware. During reads return 0. 0x0: Normal mode. 0x1: The module is reset	RW	0
0	AUTO_IDLE	Internal OCP clock gating strategy. 0x0: OCP clock is free-running. 0x1: Automatic OCP clock gating strategy is applied based on the OCP interface activity.	RW	1

Table 8-77. Register Call Summary for Register CCP2_SYSCONFIG

ISS Interfaces
- ISS CCP2 Programming Hardware Setup/Initialization: [0]
- ISS CCP2 Registers: [1]

Table 8-78. CCP2_SYSSTATUS

Address Offset	0x0000 0008		
Physical Address	0x5200 1C08	**Instance**	ISS_CCP2
Description	SYSTEM STATUS REGISTER This register provides status information about the module, excluding the interrupt status register.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															RESET_DONE

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Write 0's for future compatibility. Reads returns 0.	R	0x0000 0000
0	RESET_DONE	Internal reset monitoring Read 0x1: Reset completed. Read 0x0: Internal module reset is on going.	R	1

Table 8-79. Register Call Summary for Register CCP2_SYSSTATUS

ISS Interfaces
- ISS CCP2 Programming Hardware Setup/Initialization: [0]
- ISS CCP2 Registers: [1]

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Table 8-80. CCP2_LC01_IRQENABLE

Address Offset	0x0000 000C
Physical Address	0x5200 1C0C **Instance** ISS_CCP2
Description	INTERRUPT ENABLE REGISTER - LOG CHAN 0 1 This register regroups all the events related to logical channel 0 and logical channel 1. The events related to logical channel 0 trigger SINTERRUPTN[0]. The events related to logical channel 1 trigger SINTERRUPTN[1]. The channel shall be enabled for events to be generated on that channel.
Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LC1_OCPERROR_IRQ	RESERVED			LC1_FS_IRQ	LC1_LE_IRQ	LC1_LS_IRQ	LC1_FE_IRQ	LC1_COUNT_IRQ	RESERVED	LC1_FIFO_OVF_IRQ	LC1_CRC_IRQ	LC1_FSP_IRQ	LC1_FW_IRQ	LC1_FSC_IRQ	RESERVED	LC0_OCPERROR_IRQ	RESERVED			LC0_FS_IRQ	LC0_LE_IRQ	LC0_LS_IRQ	LC0_FE_IRQ	LC0_COUNT_IRQ	RESERVED	LC0_FIFO_OVF_IRQ	LC0_CRC_IRQ	LC0_FSP_IRQ	LC0_FW_IRQ	LC0_FSC_IRQ	RESERVED

Bits	Field Name	Description	Type	Reset
31	LC1_OCPERROR_IRQ	An OCP error occurred on the master write port. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
30:28	RESERVED		R	0x0
27	LC1_FS_IRQ	Logical channel 1 - Frame start sync code detection. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
26	LC1_LE_IRQ	Logical channel 1 - Line end sync code detection. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
25	LC1_LS_IRQ	Logical channel 1 - Line start sync code detection. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
24	LC1_FE_IRQ	Logical channel 1 - Frame end sync code detection. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
23	LC1_COUNT_IRQ	Logical channel 1 - Frame counter reached. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
22	RESERVED		R	0
21	LC1_FIFO_OVF_IRQ	Logical channel 1 - FIFO overflow error. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
20	LC1_CRC_IRQ	Logical channel 1 - CRC error. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
19	LC1_FSP_IRQ	Logical channel 1 - FSP error. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
18	LC1_FW_IRQ	Logical channel 1 - Frame width error. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0

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Bits	Field Name	Description	Type	Reset
17	LC1_FSC_IRQ	Logical channel 1 - False sync code error. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
16	RESERVED	Reserved	RW	0
15	LC0_OCPERROR_IRQ	An OCP error occurred on the master write port. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
14:12	RESERVED		R	0x0
11	LC0_FS_IRQ	Logical channel 0 - Frame start sync code detection. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
10	LC0_LE_IRQ	Logical channel 0 - Line end sync code detection. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
9	LC0_LS_IRQ	Logical channel 0 - Line start sync code detection. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
8	LC0_FE_IRQ	Logical channel 0 - Frame end sync code detection. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
7	LC0_COUNT_IRQ	Logical channel 0 - Frame counter reached. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
6	RESERVED		R	0
5	LC0_FIFO_OVF_IRQ	Logical channel 0 - FIFO overflow error. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
4	LC0_CRC_IRQ	Logical channel 0 - CRC error. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
3	LC0_FSP_IRQ	Logical channel 0 - FSP error. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
2	LC0_FW_IRQ	Logical channel 0 - Frame width error. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
1	LC0_FSC_IRQ	Logical channel 0 - False sync code error. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
0	RESERVED	Reserved	RW	0

Table 8-81. Register Call Summary for Register CCP2_LC01_IRQENABLE

ISS Interfaces

- ISS CCP2 Programming Event and Status Checking: [0]
- ISS CCP2 Registers: [1]

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Table 8-82. CCP2_LC01_IRQSTATUS

Address Offset	0x0000 0010		
Physical Address	0x5200 1C10	**Instance**	ISS_CCP2
Description	INTERRUPT STATUS REGISTER - LOG CHAN 0 1 This register regroups all the events related to logical channel 0 and logical channel 1. The events related to logical channel 0 trigger SINTERRUPTN[0]. The events related to logical channel 1 trigger SINTERRUPTN[1]. The channel shall be enabled for events to be generated on that channel.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LC1_OCPERROR_IRQ	RESERVED			LC1_FS_IRQ	LC1_LE_IRQ	LC1_LS_IRQ	LC1_FE_IRQ	LC1_COUNT_IRQ	RESERVED	LC1_FIFO_OVF_IRQ	LC1_CRC_IRQ	LC1_FSP_IRQ	LC1_FW_IRQ	LC1_FSC_IRQ	RESERVED	LC0_OCPERROR_IRQ	RESERVED			LC0_FS_IRQ	LC0_LE_IRQ	LC0_LS_IRQ	LC0_FE_IRQ	LC0_COUNT_IRQ	RESERVED	LC0_FIFO_OVF_IRQ	LC0_CRC_IRQ	LC0_FSP_IRQ	LC0_FW_IRQ	LC0_FSC_IRQ	RESERVED

Bits	Field Name	Description	Type	Reset
31	LC1_OCPERROR_IRQ	An OCP error occurred on the master write port. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
30:28	RESERVED		R	0x0
27	LC1_FS_IRQ	Logical channel 1 - Frame start sync code detection status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
26	LC1_LE_IRQ	Logical channel 1 - Line end sync code detection status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
25	LC1_LS_IRQ	Logical channel 1 - Line start sync code detection status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
24	LC1_FE_IRQ	Logical channel 1 - Frame end sync code detection status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
23	LC1_COUNT_IRQ	Logical channel 1 - Frame counter reached status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
22	RESERVED		R	0

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Bits	Field Name	Description	Type	Reset
21	LC1_FIFO_OVF_IRQ	Logical channel 1 - FIFO overflow error status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
20	LC1_CRC_IRQ	Logical channel 1 - CRC error status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
19	LC1_FSP_IRQ	Logical channel 1 - FSP error status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
18	LC1_FW_IRQ	Logical channel 1 - Frame width error status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
17	LC1_FSC_IRQ	Logical channel 1 - False sync code error status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
16	RESERVED	Reserved	RW	0
15	LC0_OCPERROR_IRQ	An OCP error occurred on the master write port. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
14:12	RESERVED		R	0x0
11	LC0_FS_IRQ	Logical channel 0 - Frame start sync code detection status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
10	LC0_LE_IRQ	Logical channel 0 - Line end sync code detection status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
9	LC0_LS_IRQ	Logical channel 0 - Line start sync code detection status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
8	LC0_FE_IRQ	Logical channel 0 - Frame end sync code detection status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
7	LC0_COUNT_IRQ	Logical channel 0 - Frame counter reached status 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
6	RESERVED		R	0
5	LC0_FIFO_OVF_IRQ	Logical channel 0 - FIFO overflow error status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
4	LC0_CRC_IRQ	Logical channel 0 - CRC error status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
3	LC0_FSP_IRQ	Logical channel 0 - FSP error status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
2	LC0_FW_IRQ	Logical channel 0 - Frame width error status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
1	LC0_FSC_IRQ	Logical channel 0 - False sync code error status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
0	RESERVED	Reserved	RW	0

Table 8-83. Register Call Summary for Register CCP2_LC01_IRQSTATUS

ISS Interfaces

- ISS CCP2 Programming Event and Status Checking: [0] [1] [2]
- ISS CCP2 Registers: [3]

Table 8-84. CCP2_LC23_IRQENABLE

Address Offset	0x0000 0014		
Physical Address	0x5200 1C14	**Instance**	ISS_CCP2
Description	INTERRUPT ENABLE REGISTER - LOG CHAN 2 3 This register regroups all the events related to logical channel 2 and logical channel 3. The events related to logical channel 2 trigger SINTERRUPTN[2]. The events related to logical channel 3 trigger SINTERRUPTN[3]. The channel shall be enabled for events to be generated on that channel.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LC3_OCPERROR_IRQ	RESERVED			LC3_FS_IRQ	LC3_LE_IRQ	LC3_LS_IRQ	LC3_FE_IRQ	LC3_COUNT_IRQ	RESERVED	LC3_FIFO_OVF_IRQ	LC3_CRC_IRQ	LC3_FSP_IRQ	LC3_FW_IRQ	LC3_FSC_IRQ	RESERVED	LC2_OCPERROR_IRQ	RESERVED			LC2_FS_IRQ	LC2_LE_IRQ	LC2_LS_IRQ	LC2_FE_IRQ	LC2_COUNT_IRQ	RESERVED	LC2_FIFO_OVF_IRQ	LC2_CRC_IRQ	LC2_FSP_IRQ	LC2_FW_IRQ	LC2_FSC_IRQ	RESERVED

Bits	Field Name	Description	Type	Reset
31	LC3_OCPERROR_IRQ	An OCP error occurred on the master write port. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
30:28	RESERVED		R	0x0
27	LC3_FS_IRQ	Logical channel 3 - Frame start sync code detection. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
26	LC3_LE_IRQ	Logical channel 3 - Line end sync code detection. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
25	LC3_LS_IRQ	Logical channel 3 - Line start sync code detection. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
24	LC3_FE_IRQ	Logical channel 3 - Frame end sync code detection. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
23	LC3_COUNT_IRQ	Logical channel 3 - Frame counter reached. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
22	RESERVED		R	0
21	LC3_FIFO_OVF_IRQ	Logical channel 3 - FIFO overflow error. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
20	LC3_CRC_IRQ	Logical channel 3 - CRC error. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
19	LC3_FSP_IRQ	Logical channel 3 - FSP error. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
18	LC3_FW_IRQ	Logical channel 3 - Frame width error. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
17	LC3_FSC_IRQ	Logical channel 3 - False sync code error. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
16	RESERVED	Reserved	RW	0
15	LC2_OCPERROR_IRQ	An OCP error occurred on the master write port. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0

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Bits	Field Name	Description	Type	Reset
14:12	RESERVED		R	0x0
11	LC2_FS_IRQ	Logical channel 2 - Frame start sync code detection. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
10	LC2_LE_IRQ	Logical channel 2 - Line end sync code detection. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
9	LC2_LS_IRQ	Logical channel 2 - Line start sync code detection. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
8	LC2_FE_IRQ	Logical channel 2 - Frame end sync code detection. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
7	LC2_COUNT_IRQ	Logical channel 2 - Frame counter reached. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
6	RESERVED		R	0
5	LC2_FIFO_OVF_IRQ	Logical channel 2 - FIFO overflow error. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
4	LC2_CRC_IRQ	Logical channel 2 - CRC error. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
3	LC2_FSP_IRQ	Logical channel 2 - FSP error. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
2	LC2_FW_IRQ	Logical channel 2 - Frame width error. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
1	LC2_FSC_IRQ	Logical channel 2 - False sync code error. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
0	RESERVED	Reserved	RW	0

Table 8-85. Register Call Summary for Register CCP2_LC23_IRQENABLE

ISS Interfaces

- ISS CCP2 Programming Event and Status Checking: [0]
- ISS CCP2 Registers: [1]

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Table 8-86. CCP2_LC23_IRQSTATUS

Address Offset	0x0000 0018		
Physical Address	0x5200 1C18	**Instance**	ISS_CCP2
Description	INTERRUPT STATUS REGISTER - LOG CHAN 2 3 This register regroups all the events related to logical channel 2 and logical channel 3. The events related to logical channel 2 trigger SINTERRUPTN[2]. The events related to logical channel 3 trigger SINTERRUPTN[3]. The channel shall be enabled for events to be generated on that channel.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LC3_OCPERROR_IRQ	RESERVED			LC3_FS_IRQ	LC3_LE_IRQ	LC3_LS_IRQ	LC3_FE_IRQ	LC3_COUNT_IRQ	RESERVED	LC3_FIFO_OVF_IRQ	LC3_CRC_IRQ	LC3_FSP_IRQ	LC3_FW_IRQ	LC3_FSC_IRQ	RESERVED	LC2_OCPERROR_IRQ	RESERVED			LC2_FS_IRQ	LC2_LE_IRQ	LC2_LS_IRQ	LC2_FE_IRQ	LC2_COUNT_IRQ	RESERVED	LC2_FIFO_OVF_IRQ	LC2_CRC_IRQ	LC2_FSP_IRQ	LC2_FW_IRQ	LC2_FSC_IRQ	RESERVED

Bits	Field Name	Description	Type	Reset
31	LC3_OCPERROR_IRQ	An OCP error occurred on the master write port. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
30:28	RESERVED		R	0x0
27	LC3_FS_IRQ	Logical channel 3 - Frame start sync code detection status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
26	LC3_LE_IRQ	Logical channel 3 - Line end sync code detection status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
25	LC3_LS_IRQ	Logical channel 3 - Line start sync code detection status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
24	LC3_FE_IRQ	Logical channel 3 - Frame end sync code detection status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
23	LC3_COUNT_IRQ	Logical channel 3 - Frame counter reached status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
22	RESERVED		R	0

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Bits	Field Name	Description	Type	Reset
21	LC3_FIFO_OVF_IRQ	Logical channel 3 - FIFO overflow error status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
20	LC3_CRC_IRQ	Logical channel 3 - CRC error status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
19	LC3_FSP_IRQ	Logical channel 3 - FSP error status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
18	LC3_FW_IRQ	Logical channel 3 - Frame width error status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
17	LC3_FSC_IRQ	Logical channel 3 - False sync code error status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
16	RESERVED	Reserved	RW	0
15	LC2_OCPERROR_IRQ	An OCP error occurred on the master write port. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
14:12	RESERVED		R	0x0
11	LC2_FS_IRQ	Logical channel 2 - Frame start sync code detection status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
10	LC2_LE_IRQ	Logical channel 2 - Line end sync code detection status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
9	LC2_LS_IRQ	Logical channel 2 - Line start sync code detection status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
8	LC2_FE_IRQ	Logical channel 2 - Frame end sync code detection status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
7	LC2_COUNT_IRQ	Logical channel 2 - Frame counter reached status 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
6	RESERVED		R	0
5	LC2_FIFO_OVF_IRQ	Logical channel 2 - FIFO overflow error status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
4	LC2_CRC_IRQ	Logical channel 2 - CRC error status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
3	LC2_FSP_IRQ	Logical channel 2 - FSP error status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
2	LC2_FW_IRQ	Logical channel 2 - Frame width error status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
1	LC2_FSC_IRQ	Logical channel 2 - False sync code error status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
0	RESERVED	Reserved	RW	0

Table 8-87. Register Call Summary for Register CCP2_LC23_IRQSTATUS

ISS Interfaces

- ISS CCP2 Programming Event and Status Checking: [0] [1] [2]
- ISS CCP2 Registers: [3]

Table 8-88. CCP2_LCM_IRQENABLE

Address Offset	0x0000 002C		
Physical Address	0x5200 1C2C	**Instance**	ISS_CCP2
Description	INTERRUPT ENABLE REGISTER - Memory channel This register regroups all the events related to the memory channel 2. The events related to memory channel trigger SINTERRUPTN[8]. The channel shall be enabled for events to be generated on that channel.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														LCM_OCPERROR	LCM_EOF

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	LCM_OCPERROR	An interconnect error has been returned for a read (interconnect read master) or write (interconnect write master) transaction related to LCM operation 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
0	LCM_EOF	Memory read channel - End of frame 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0

Table 8-89. Register Call Summary for Register CCP2_LCM_IRQENABLE

ISS Interfaces

- ISS CCP2 Programming Event and Status Checking: [0]
- ISS CCP2 Registers: [1]

Table 8-90. CCP2_LCM_IRQSTATUS

Address Offset	0x0000 0030		
Physical Address	0x5200 1C30	**Instance**	ISS_CCP2
Description	INTERRUPT STATUS REGISTER - Memory channel This register regroups all the events related to memory channel. The events related to memory channel trigger SINTERRUPTN[8]. The channel shall be enabled for events to be generated on that channel.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														LCM_OCPERROR	LCM_EOF

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	LCM_OCPERROR	An interconnect error has been returned for a read (interconnect read master) or write (interconnect write master) transaction related to LCM operation 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
0	LCM_EOF	Memory read channel - End of frame 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0

Table 8-91. Register Call Summary for Register CCP2_LCM_IRQSTATUS

ISS Interfaces

- ISS CCP2 Programming Event and Status Checking: [0] [1] [2]
- ISS CCP2 Registers: [3]

Table 8-92. CCP2_CTRL

Address Offset	0x0000 0040		
Physical Address	0x5200 1C40	**Instance**	ISS_CCP2
Description	GLOBAL CONTROL REGISTER This register controls the CCP2 receiver. This register shall not be modified dynamically (except IF_EN bit field).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FRACDIV																POSTED	DBG_EN	VP_CLK_POL	VP_ONLY_EN	RESERVED	VP_CLK_FORCE_ON	RESERVED	BURST			MODE	FRAME	RESERVED	RESERVED	IF_EN	

Bits	Field Name	Description	Type	Reset
31:15	FRACDIV	Fractional clock divider control for the video port. The mean video port clock is VPBASECLOCK * FRACDIV/65536. Valid range: 1-65536	RW	0x10000
14	POSTED	Selects between posted and non posted writes. 0x0: Non posted 0x1: Posted	RW	0
13	DBG_EN	Enables the debug mode. 0x0: Disable 0x1: Enable	RW	0
12	VP_CLK_POL	VP clock polarity 0x0: The CCP2 receiver writes the data on the VP on the L3 falling edge before the next falling PCLK edge. 0x1: The CCP2 receiver writes the data on the VP on the L3 rising edge before the next rising PCLK edge.	RW	0
11	VP_ONLY_EN	VP only enable. 0x0: The VP is enabled and the OCP master port are enabled. 0x1: The VP is enabled and the OCP master port is disabled. The embedded data and pixel data are output on the VP.	RW	0
10	RESERVED	Read returns reset value	RW	0

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Bits	Field Name	Description	Type	Reset
9	VP_CLK_FORCE_ON	Controls VP_PCLK gating during frame blanking periods. 0x0: The VP_PCLK is gated during vertical blanking periods. 0x1: The VP_PCLK is free-running during vertical blanking periods.	RW	0
8	RESERVED		R	0
7:5	BURST	Forces the write burst size used by the module. The write burst size shall never exceed the output FIFO size. The output FIFO size can be read with the CCP2_GNQ.FIFODEPTH bit field. 0x0: 1x 64-bit burst = single request. 0x1: 2x 64-bit bursts. 0x3: 8x 64-bit bursts. 0x4: 16x 64-bit bursts. 0x2: 4x 64-bit bursts.	RW	0x0
4	MODE	Selects the receiver operating mode. This bit is only writable when the CCP2MODE input is 1. 0x0: MIPI CSI1 compatible mode. When this bit is set all CCP2 settings are ignored. If the settings are not set correctly to MIPI CSI1 values, the behavior of the receiver is unpredictable. 0x1: CCP2 compatible mode	RW	0
3	FRAME	Set the modality in which IF_EN works. 0x0: When software writes IF_EN = 0 the interface is disabled immediately. 0x1: When software writes IF_EN = 0 the interface is disabled after the next FEC sync code.	RW	0
2	RESERVED	Read returns reset value	RW	0
1	RESERVED	Read returns reset value	RW	0
0	IF_EN	Enables the physical interface to the module. 0x0: The interface is disabled. If FRAME = 0, it is disabled immediately. If FRAME = 1, it is disabled on the next FEC sync code. If FRAME=1, it is advised to disable the logical channels first (CCP2_LCX_CTRL.CHAN_EN=0) before writing IF_EN=0. 0x1: The interface is enabled immediately, the data acquisition starts on the next FSC sync code. Writing 1 to this register when the current value is 0 has the effect to clear the output FIFO. The pixel data of the following frame will be written in the PING buffer, that is, the CCP2_LCX_CTRL.PING_PONG bits are reset to 1 as well.	RW	0

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Table 8-93. Register Call Summary for Register CCP2_CTRL

ISS Interfaces

- ISS CCP2 Protocol and Data Formats: [0] [1]
- ISS CCP2 PHY: [2] [3]
- ISS CCP2 VP Interface: [4] [5]
- ISS CCP2 Memory Read Channel: [6] [7]
- ISS CCP2 Programming Hardware Setup/Initialization: [8]
- ISS CCP2 Programming Enable/Disable the Hardware: [9] [10] [11] [12] [13] [14] [15] [16]
- ISS CCP2 Programming Select the Mode: MIPI CSI1 or CCP2: [17]
- ISS CCP2 Programming Burst Settings: [18]
- ISS CCP2 Programming Debug Mode: [19] [20]
- ISS CCP2 Programming Video Port: [21] [22] [23] [24] [25] [26] [27]
- ISS CCP2 Programming Controls: [28]
- ISS CCP2 Programming CRC: [29]
- ISS CCP2 Programming Destination Format: [30] [31]
- ISS CCP2 Programming Frame Acquisition: [32]
- ISS CCP2 Programming Memory Read Channel: [33] [34] [35] [36]
- ISS CCP2 Registers: [37] [38]
- ISS CSI2 REGS1 Registers: [39]

Table 8-94. CCP2_DBG

Address Offset	0x0000 0044		
Physical Address	0x5200 1C44	**Instance**	ISS_CCP2
Description	DEBUG REGISTER This register provides a way to debug the CCP2 receiver with no image sensor connected to the module. The debug mode is enabled by CCP2_CTRL.DBG_EN. Each write to this register provides a full 32bit word to the CCP2 receiver, even when only 8 or 16 bits are written. The newly written value is merged with the previous value (check the example in the programming model section).		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DBG																															

Bits	Field Name	Description	Type	Reset
31:0	DBG	32-bit input value. Write only register. Reads return 0.	W	0x0000 0000

Table 8-95. Register Call Summary for Register CCP2_DBG

ISS Interfaces

- ISS CCP2 Programming Debug Mode: [0] [1] [2] [3] [4] [5] [6] [7]
- ISS CCP2 Registers: [8]

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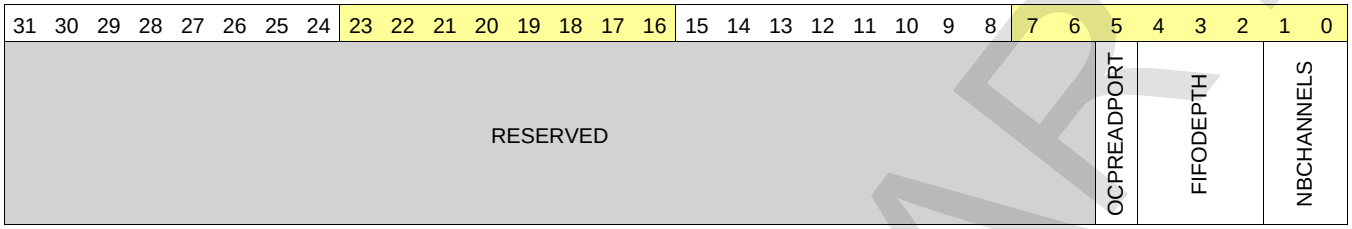
Table 8-96. CCP2_GNQ

Address Offset	0x0000 0048		
Physical Address	0x5200 1C48	**Instance**	ISS_CCP2
Description	GENERIC PARAMETER REGISTER This register provide a way to read the generic parameters used in the design.		
Type	R		



Bits	Field Name	Description	Type	Reset
31:6	RESERVED		R	0x0000000
5	OCPREADPORT	The OCP master read port, the DPCM encoder and ALAW decompression are only present when this bit is set.	R	1
4:2	FIFODEPTH	Output FIFO size in multiple of 64 bits. Read 0x3: 16 x 64 bits Read 0x4: 32 x 64 bits Read 0x2: 8 x 64 bits Read 0x0: 2 x 64 bits Read 0x1: 4 x 64 bits Read 0x5: 64 x 64 bits	R	0x5
1:0	NBCHANNELS	Number of logical channels supported by the module. Read 0x3: 8 logical channels Read 0x2: 4 logical channels Read 0x1: 2 logical channels Read 0x0: 1 logical channel	R	0x2

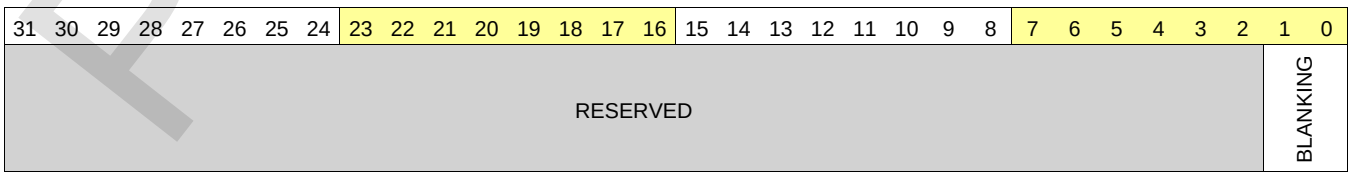
Table 8-97. Register Call Summary for Register CCP2_GNQ

ISS Interfaces

- ISS CCP2 Registers: [0] [1]

Table 8-98. CCP2_CTRL1

Address Offset	0x0000 004C		
Physical Address	0x5200 1C4C	**Instance**	ISS_CCP2
Description	GLOBAL CONTROL REGISTER (2) This register controls the CCP2 receiver.		
Type	RW		



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Bits	Field Name	Description	Type	Reset
31:2	RESERVED	Reserved	RO Rreturns 0s	0
1:0	BLANKING	Controls the number of clock pulses provided during vertical and horizontal clock periods. When the blanking period provided by the camera is lower than the value set here, the blanking period is shortened by the CCP2 to prevent internal FIFO overflow. Software must increase the sensor blanking period in that case. 0x0: 4 video port clock cycles 0x1: 16 video port clock cycles 0x2: 64 video port clock cycles 0x3: Free running	RW	0x0

Table 8-99. Register Call Summary for Register CCP2_CTRL1

ISS Interfaces

- ISS CCP2 VP Interface: [0] [1] [2] [3]
- ISS CCP2 Registers: [4]

Table 8-100. CCP2_LCx_CTRL

Address Offset	0x0000 0050 + (x * 0x30)	**Index**	x = 0 to 3
Physical Address	0x5200 1C50 + (x * 0x30)	**Instance**	ISS_CCP2
Description	CONTROL REGISTER - LOG CHAN 0 This register controls the logical channel 0. This register is shadowed: modifications are taken into account after the next FSC sync code.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT								RESERVED				CRC_EN	DPCM_PRED	PING_PONG	COUNT_UNLOCK	ALPHA								FORMAT						REGION_EN	CHAN_EN

Bits	Field Name	Description	Type	Reset
31:24	COUNT	Sets the number of frame to acquire. Once the frame acquisition starts, the COUNT value is decremented after every frame. When COUNT reaches 0, the COUNT_IRQ interrupt is triggered and CHAN_EN is set to 0. Writes to this bit field are controlled by the COUNT_UNLOCK bit. COUNT can be overwritten dynamically with a new count value. 0: Infinite number of frames (no count). 1: 1 frame to acquire ... 255: 255 frames to acquire.	RW	0x00
23:20	RESERVED		R	0x0
19	CRC_EN	Enables the cyclic redundancy check. 0x0: Disabled 0x1: Enabled	RW	0

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Bits	Field Name	Description	Type	Reset
18	DPCM_PRED	Selects the DPCM predictor to be used for the RAW6+DPCM10, RAW7+DPCM10 and RAW8+DPCM12 data formats. The RAW8+DPCM10 data format always use the simple predictor. 0x0: The advanced predictor is used 0x1: The simple predictor is used.	RW	0
17	PING_PONG	Indicates whether the PING or PONG destination address (CCP2_LC0_DAT_PING_ADDR or CCP2_LC0_DAT_PONG_ADDR) was used to write the last frame. This bit field toggles after every FEC sync code. Read 0x1: PONG buffer Read 0x0: PING buffer	R	1
16	COUNT_UNLOCK	Unlock writes to the COUNT bit field. Write 0x0: COUNT bit field is locked. Writes have no effect Write 0x1: COUNT bit field is unlocked. Writes are possible.	W	0
15:8	ALPHA	Alpha value for RGB888 and RBG444.	RW	0x00

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Bits	Field Name	Description	Type	Reset
7:2	FORMAT	Data format selection. 0xD: RAW7 + DPCM10 + EXP16 0x15: RAW10 + EXP16 0x1E: RAW10 - RAW8 RAW10 data from sensor is right shifted to produce RAW8 before it is send to memory 0x8: RAW6 + EXP8 0x5: RGB565 0x1B: RAW10 - RAW8 DPCM RAW10 data from sensor is DPCM compressed into RAW8 before it is send to memory. 0x2: YUV4:2:0 0x4: RGB444 + EXP16 0x6: RGB888 0x1: YUV4:2:2 LITTLE ENDIAN 0x1D: JPEG8 0x0: YUV4:2:2 BIG ENDIAN 0xB: RAW10 - RAW6 DPCM RAW10 data from sensor is DPCM compressed into RAW6 before it is send to memory. Used predictor is selected by the DPCM_PRED bit. 0x20: RAW10 - RAW8 ALAW 0x3: YUV4:2:2 + VP or RAW8 + VP 0x17: RAW10 - RAW7 DPCM + EXP8 RAW10 data from sensor is DPCM compressed into RAW7 and expanded to 8 bits before it is send to memory. Used predictor is selected by the DPCM_PRED bit. 0x11: RAW8 + DPCM10 + EXP16 0xA: RAW6 + DPCM10 + VP 0x9: RAW6 + DPCM10 + EXP16 0x10: RAW8 This mode can be used to output RAW6 and RAW7 as well. 0x21: RAW8 DPCM10 - ALAW 0x12: RAW8 + DPCM10 + VP 0x13: RAW10 - RAW7 DPCM RAW10 data from sensor is DPCM compressed into RAW7 before it is send to memory. Used predictor is selected by the DPCM_PRED bit. 0x18: RAW12 0x14: RAW10 0xE: RAW7 + DPCM10 + VP 0x16: RAW10 + VP 0x1C: JPEG8 + FSP 0x7: RGB888 + EXP32 0x19: RAW12 + EXP16 0x1F: RAW8 DPCM12 - RAW12 + VP Used predictor is selected by the DPCM_PRED bit. 0x1A: RAW12 + VP 0xF: RAW10 - RAW6 DPCM + EXP8 RAW10 data from sensor is DPCM compressed into RAW6 and expanded to 8 bits before it is send to memory. Used predictor is selected by the DPCM_PRED bit. 0xC: RAW7 + EXP8	RW	0x00

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Bits	Field Name	Description	Type	Reset
1	REGION_EN	Enables the setting of regions of interest in the frame: SOF region, EOF region and DAT region. 0x0: Disabled 0x1: Enabled	RW	0
0	CHAN_EN	Enables the logical channel 0x0: Disabled 0x1: Enabled	RW	0x1 for LC0 0x0 for LC1 0x0 for LC2 0x0 for LC3

Table 8-101. Register Call Summary for Register CCP2_LCx_CTRL

ISS Interfaces

- ISS CCP2 Protocol and Data Formats: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13]
- ISS CCP2 Data Compression: [16]
- ISS CCP2 Programming Register Accessibility During Frame Processing: [17]
- ISS CCP2 Programming Enable/Disable the Hardware: [18] [19] [20]
- ISS CCP2 Programming Controls: [21]
- ISS CCP2 Programming Region-of-Interest: [22] [23]
- ISS CCP2 Programming CRC: [24] [25]
- ISS CCP2 Programming Destination Format: [26]
- ISS CCP2 Programming Frame Acquisition: [27] [28] [29] [30] [31] [32] [33] [34]
- ISS CCP2 Programming Pixel Data Region: [35] [36]
- ISS CCP2 Registers: [37]

Table 8-102. CCP2_LCx_CODE

Address Offset	0x0000 0054 + (x * 0x30)	**Index**	x = 0 to 3
Physical Address	0x5200 1C54 + (x * 0x30)	**Instance**	ISS_CCP2
Description	CODE REGISTER - LOG CHAN 0 This register sets the codes that are used in the 32-bit synchronization codes to recognize the logical channel, frame start, frame end, line start and line end codes. This register applies for logical channel 0 only. The default values are usually not supposed to be modified. Updating this register with new codes under a flowing serial transmission on that channel will cause unexpected result.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								CHAN_ID				FEC				FSC				LEC				LSC							

Bits	Field Name	Description	Type	Reset
31:20	RESERVED		R	0x000
19:16	CHAN_ID	Log chan 0 identifier. The channel identifier is located between bits 4 to 7 in the 32-bit synchronization codes.	RW	0x0
15:12	FEC	Log chan 0 frame end sync code identifier. The sync code identifier is located between bits 0 to 3 in the 32-bit synchronization codes.	RW	0x3
11:8	FSC	Log chan 0 frame start sync code identifier. The sync code identifier is located between bits 0 to 3 in the 32-bit synchronization codes.	RW	0x2
7:4	LEC	Log chan 0 line end sync code identifier. The sync code identifier is located between bits 0 to 3 in the 32-bit synchronization codes.	RW	0x1
3:0	LSC	Log chan 0 line start sync code identifier. The sync code identifier is located between bits 0 to 3 in the 32-bit synchronization codes.	RW	0x0

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Table 8-103. Register Call Summary for Register CCP2_LCx_CODE

ISS Interfaces

- ISS CCP2 Programming Register Accessibility During Frame Processing: [0]
- ISS CCP2 Programming Synchronization Codes: [1] [2] [3] [4] [5]
- ISS CCP2 Registers: [6]

Table 8-104. CCP2_LCx_STAT_START

Address Offset	0x0000 0058 + (x * 0x30)	**Index**	x = 0 to 3
Physical Address	0x5200 1C58 + (x * 0x30)	**Instance**	ISS_CCP2
Description	STATUS LINE START REGISTER - LOG CHAN 0 This register is shadowed: modifications are taken into account after the next FSC sync code.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				EOF												RESERVED				SOF											

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:16	EOF	Sets the vertical position of the EOF status lines in regards of the FSC sync code. From 0 to 4095.	RW	0x000
15:12	RESERVED		R	0x0
11:0	SOF	Sets the vertical position of the EOF status lines in regards of the FSC sync code. Should always be 0.	RW	0x000

Table 8-105. Register Call Summary for Register CCP2_LCx_STAT_START

ISS Interfaces

- ISS CCP2 Programming Register Accessibility During Frame Processing: [0]
- ISS CCP2 Programming Video Port: [1]
- ISS CCP2 Programming Status Data: [2] [3]
- ISS CCP2 Registers: [4]

Table 8-106. CCP2_LCx_STAT_SIZE

Address Offset	0x0000 005C + (x * 0x30)	**Index**	x = 0 to 3
Physical Address	0x5200 1C5C + (x * 0x30)	**Instance**	ISS_CCP2
Description	STATUS LINE SIZE REGISTER - LOG CHAN 0 This register is shadowed: modifications are taken into account after the next FSC sync code.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				EOF												RESERVED				SOF											

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:16	EOF	Sets the number of EOF status lines From 0 to 4095	RW	0x000
15:12	RESERVED		R	0x0
11:0	SOF	Sets the number of SOF status line(s) From 0 to 4095	RW	0x000

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Table 8-107. Register Call Summary for Register CCP2_LCx_STAT_SIZE

ISS Interfaces

- ISS CCP2 Programming Register Accessibility During Frame Processing: [0]
- ISS CCP2 Programming Video Port: [1]
- ISS CCP2 Programming Status Data: [2] [3] [4]
- ISS CCP2 Registers: [5]

Table 8-108. CCP2_LCx_SOF_ADDR

Address Offset	0x0000 0060 + (x * 0x30)	**Index**	x = 0 to 3
Physical Address	0x5200 1C60 + (x * 0x30)	**Instance**	ISS_CCP2
Description	SOF STATUS LINE MEM ADDRESS REGISTER - LOG CHAN 0 This register sets the 32-bit memory address where the SOF data are stored. The 5 LSBs are ignored: the address shall be aligned on a 32-byte boundary. This register is shadowed: modifications are taken into account after the next FSC sync code.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR																								RESERVED							

Bits	Field Name	Description	Type	Reset
31:5	ADDR	27 most significant bits of the 32-bit address.	RW	0x0000000
4:0	RESERVED		R	0x00

Table 8-109. Register Call Summary for Register CCP2_LCx_SOF_ADDR

ISS Interfaces

- ISS CCP2 Programming Register Accessibility During Frame Processing: [0]
- ISS CCP2 Programming Status Data: [1]
- ISS CCP2 Registers: [2]

Table 8-110. CCP2_LCx_EOF_ADDR

Address Offset	0x0000 0064 + (x * 0x30)	**Index**	x = 0 to 3
Physical Address	0x5200 1C64 + (x * 0x30)	**Instance**	ISS_CCP2
Description	EOF STATUS LINE MEM ADDRESS REGISTER - LOG CHAN 0 This register sets the 32-bit memory address where the EOF data are stored. The 5 LSBs are ignored: the address shall be aligned on a 32-byte boundary. This register is shadowed: modifications are taken into account after the next FSC sync code.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR																								RESERVED							

Bits	Field Name	Description	Type	Reset
31:5	ADDR	27 most significant bits of the 32-bit address.	RW	0x0000000
4:0	RESERVED		R	0x00

Table 8-111. Register Call Summary for Register CCP2_LCx_EOF_ADDR

ISS Interfaces

- ISS CCP2 Programming Register Accessibility During Frame Processing: [0]
- ISS CCP2 Programming Status Data: [1]
- ISS CCP2 Registers: [2]

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Table 8-112. CCP2_LCx_DAT_START

Address Offset	0x0000 0068 + (x * 0x30)	**Index**	x = 0 to 3
Physical Address	0x5200 1C68 + (x * 0x30)	**Instance**	ISS_CCP2
Description	DATA START REGISTER - LOG CHAN 0 This register is shadowed: modifications are taken into account after the next FSC sync code.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								VERT								RESERVED															

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:16	VERT	Sets the vertical position of the data in regards of the FSC sync code. From 0 to 4095 lines.	RW	0x000
15:0	RESERVED		R	0x0000

Table 8-113. Register Call Summary for Register CCP2_LCx_DAT_START

ISS Interfaces

- ISS CCP2 Programming Video Port: [0]
- ISS CCP2 Programming Pixel Data Region: [1]
- ISS CCP2 Registers: [2]

Table 8-114. CCP2_LCx_DAT_SIZE

Address Offset	0x0000 006C + (x * 0x30)	**Index**	x = 0 to 3
Physical Address	0x5200 1C6C + (x * 0x30)	**Instance**	ISS_CCP2
Description	DATA SIZE REGISTER - LOG CHAN 0 This register is shadowed: modifications are taken into account after the next FSC sync code.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								VERT								RESERVED															

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:16	VERT	Sets the vertical size of the data window. From 0 to 4095 lines. If VERT = "0", no data is output.	RW	0x000
15:0	RESERVED		R	0x0000

Table 8-115. Register Call Summary for Register CCP2_LCx_DAT_SIZE

ISS Interfaces

- ISS CCP2 Programming Register Accessibility During Frame Processing: [0]
- ISS CCP2 Programming Video Port: [1]
- ISS CCP2 Programming Pixel Data Region: [2]
- ISS CCP2 Registers: [3]

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Table 8-116. CCP2_LCx_DAT_PING_ADDR

Address Offset	0x0000 0070 + (x * 0x30)	**Index**	x = 0 to 3
Physical Address	0x5200 1C70 + (x * 0x30)	**Instance**	ISS_CCP2
Description	DATA MEM PING ADDRESS REGISTER - LOG CHAN 0 This register sets the 32-bit memory address where the pixel data are stored. The destination is double buffered: this register sets the PING address. Double buffering is enabled when the addresses CCP2_LC0_DAT_PING_ADDR and CCP2_LC0_DAT_PONG_ADDR are different. The 5 LSBs are ignored: the address shall be aligned on a 32-byte boundary. This register is shadowed: modifications are taken into account after the next FSC sync code.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR																								RESERVED							

Bits	Field Name	Description	Type	Reset
31:5	ADDR	27 most significant bits of the 32-bit address.	RW	0x0000000
4:0	RESERVED		R	0x00

Table 8-117. Register Call Summary for Register CCP2_LCx_DAT_PING_ADDR

ISS Interfaces

- ISS CCP2 Programming Register Accessibility During Frame Processing: [0]
- ISS CCP2 Programming Frame Acquisition: [1]
- ISS CCP2 Programming Pixel Data Region: [2] [3] [4] [5]
- ISS CCP2 Registers: [6]

Table 8-118. CCP2_LCx_DAT_PONG_ADDR

Address Offset	0x0000 0074 + (x * 0x30)	**Index**	x = 0 to 3
Physical Address	0x5200 1C74 + (x * 0x30)	**Instance**	ISS_CCP2
Description	DATA MEM PONG ADDRESS REGISTER - LOG CHAN 0 This register sets the 32-bit memory address where the pixel data are stored. The destination is double buffered: this register sets the PONG address. Double buffering is enabled when the addresses CCP2_LC0_DAT_PING_ADDR and CCP2_LC0_DAT_PONG_ADDR are different. The 5 LSBs are ignored: the address shall be aligned on a 32-byte boundary. This register is shadowed: modifications are taken into account after the next FSC sync code.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR																								RESERVED							

Bits	Field Name	Description	Type	Reset
31:5	ADDR	27 most significant bits of the 32-bit address.	RW	0x0000000
4:0	RESERVED		R	0x00

Table 8-119. Register Call Summary for Register CCP2_LCx_DAT_PONG_ADDR

ISS Interfaces

- ISS CCP2 Programming Register Accessibility During Frame Processing: [0]
- ISS CCP2 Programming Frame Acquisition: [1]
- ISS CCP2 Programming Pixel Data Region: [2] [3] [4] [5]
- ISS CCP2 Registers: [6]

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Table 8-120. CCP2_LCx_DAT_OFST

Address Offset	0x0000 0078 + (x * 0x30)	**Index**	x = 0 to 3
Physical Address	0x5200 1C78 + (x * 0x30)	**Instance**	ISS_CCP2
Description	DATA MEM ADDRESS OFFSET REGISTER - LOG CHAN 0 This register sets the offset, which is applied on the destination address after each line is written to memory. This register applies for both CCP2_LC0_DAT_PING_ADDR and CCP2_LC0_DAT_PONG_ADDR. For example, it enables to perform 2D data transfers of the pixel data into a frame buffer. In such case, the pixel data and frame buffer data shall have the same data format. The 5 LSBs are ignored: the offset shall be a multiple of 32 bytes. Only full 64-bits words are written to memory at the end of lines. This register is shadowed: modifications are taken into account after the next FSC sync code.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OFST																											RESERVED					

Bits	Field Name	Description	Type	Reset
31:5	OFST	Line offset programmed in bytes. If OFST = 0, the data is written contiguously in memory. Otherwise, OFST sets the destination offset between the first pixel of the previous line and the first pixel of the current line. NOTE: An OCP access (read/write) is required to properly update the CCP2_LCx_DAT_OFST register	RW	0x0000000
4:0	RESERVED		R	0x00

Table 8-121. Register Call Summary for Register CCP2_LCx_DAT_OFST

ISS Interfaces

- ISS CCP2 Programming Register Accessibility During Frame Processing: [0]
- ISS CCP2 Programming Pixel Data Region: [1] [2] [3] [4] [5] [6] [7]
- ISS CCP2 Registers: [8] [9]

Table 8-122. CCP2_LCM_CTRL

Address Offset	0x0000 01D0		
Physical Address	0x5200 1DD0	**Instance**	ISS_CCP2
Description	Control register for the memory channel. It defines the data format of the source frame stored in memory and how this frame is processed.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DST_PACK	DST_DPCM_PRED	DST_COMPR		RESERVED		DST_FORMAT		SRC_PACK	SRC_DPCM_PRED	SRC_DECOMPR		SRC_FORMAT				RESERVED								BURST_SIZE			READ_THROTTLE			DST_PORT	RESERVED	CHAN_EN

Bits	Field Name	Description	Type	Reset
31	DST_PACK	Data is packed before it is send to memory. Applies to RAW6, RAW7, RAW10, and RAW12 only. 0x0: Disabled 0x1: Enabled	RW	0

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Bits	Field Name	Description	Type	Reset
30	DST_DPCM_PRED	Selects the DPCM predictor to be used for the RAW6+DPCM10 and RAW7+DPCM10 data formats. The RAW8+DPCM10 data format always use the simple predictor. 0x0: The advanced predictor is used 0x1: The simple predictor is used.	RW	0
29:28	DST_COMPR	Enables data compression of data sent to memory 0x0: No compression 0x1: A-Law compression RAW10 - RAW8 A-Law when DST_FORMAT=RAW8 other destination formats are invalid. 0x2: DPCM compression RAW10 - RAW6 DPCM when DST_FORMAT=RAW6 RAW10 - RAW7 DPCM when DST_FORMAT=RAW7 RAW10 - RAW8 DPCM when DST_FORMAT=RAW8 other destination formats are invalid.	RW	0x0
27	RESERVED		R	0
26:24	DST_FORMAT	Output format selection. Not every combination between input and output formats are possible. 0x6: RAW16 0x1: RAW7 0x0: RAW6 0x2: RAW8 0x4: RAW12 0x5: RAW14 0x3: RAW10	RW	0x0
23	SRC_PACK	Data stored in memory is packed and must be unpacked. 0x0: Disabled 0x1: Enabled	RW	0
22	SRC_DPCM_PRED	Selects the DPCM predictor to be used for the RAW6+DPCM10, RAW7+DPCM10 and RAW8+DPCM12 data formats. The RAW8+DPCM10 and RAW6 + DPCM12 data format always use the simple predictor. 0x0: The advanced predictor is used 0x1: The simple predictor is used.	RW	0
21:20	SRC_DECOMPR	Enable decompression of incoming data 0x0: No decompression 0x1: A-Law decompression RAW8 A-Law - RAW10 when SRC_FORMAT=RAW8 other source formats are invalid. 0x3: DPCM decompression RAW6 DPCM - RAW12 when SRC_FORMAT=RAW6 RAW8 DPCM - RAW12 when SRC_FORMAT=RAW8 other source formats are invalid. 0x2: DPCM decompression RAW6 DPCM - RAW10 when SRC_FORMAT=RAW6 RAW7 DPCM - RAW10 when SRC_FORMAT=RAW7 RAW8 DPCM - RAW10 when SRC_FORMAT=RAW8 other source formats are invalid.	RW	0x0

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Bits	Field Name	Description	Type	Reset
19:16	SRC_FORMAT	Data format of the data stored in memory. As there is no header embedded in the data sent to memory the user is responsible of choosing the adequate format. 0x6: RAW16 0x1: RAW7 0xA: Reserved 0x7: Reserved 0xD: Reserved 0x0: RAW6 0x2: RAW8 0x8: Reserved 0x9: Reserved 0xB: Reserved 0x4: RAW12 0x5: RAW14 0xF: Reserved 0xC: Reserved 0x3: RAW10 0xE: Reserved	RW	0x0
15:8	RESERVED		R	0x00
7:5	BURST_SIZE	Defines the burst size of the master read port 0x0: 1x 64-bit burst = single request. 0x1: 2x 64-bit bursts. 0x3: 8x 64-bit bursts. 0x4: 16x 64-bit bursts. 0x2: 4x 64-bit bursts.	RW	0x0
4:3	READ_THROTTLE	Limit maximum data read speed for memory to memory operation 0x0: Full speed. Throughput is limited by internal processing capabilities. 0x1: 1/2 speed 0x3: 1/8 speed 0x2: 1/4 speed	RW	0x0
2	DST_PORT	Select the destination port 0x0: Data is send to video port, it is always send without compression or packing. The DST_COMPR, DST_DPCM_PRED, DST_PACK, CCP2_LCM_DST_WRITE, and CCP2_LCM_DST_OFST registers have no effect. 0x1: Data is send to memory.	RW	0
1	RESERVED		R	0
0	CHAN_EN	Enables the read from memory channel. Before enabling the memory read channel software shall: - disable the physical interface using the IF_EN bit - wait until disabling of the physical interface is effective (depends on the FRAME bit) Read from memory starts as soon as this bit is set, therefore all CCP2_LCM_x registers must be configured correctly before. This bit is cleared by hardware at the end of the frame. 0x0: Disabled 0x1: Enabled	RW	0

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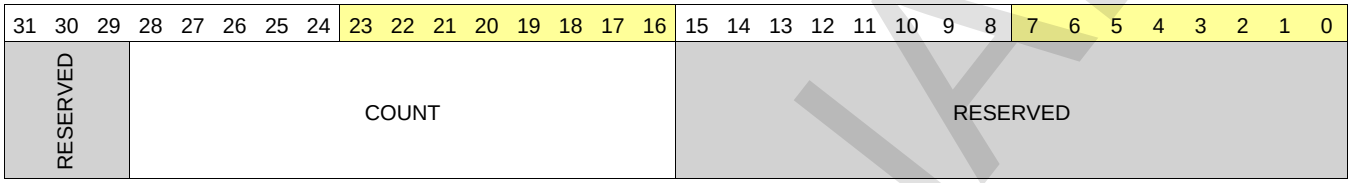
Table 8-123. Register Call Summary for Register CCP2_LCM_CTRL

ISS Interfaces
- ISS CCP2 Memory Read Channel: [0] [1] [2] [3] [4] [5] [6] [7] [8]
- ISS CCP2 Programming Memory Read Channel: [9] [10] [11] [12] [13] [14] [15] [16]
- ISS CCP2 Registers: [17]

Table 8-124. CCP2_LCM_VSIZE

Address Offset	0x0000 01D4		
Physical Address	0x5200 1DD4	**Instance**	ISS_CCP2
Description	Memory channel vertical framing register		
Type	RW		



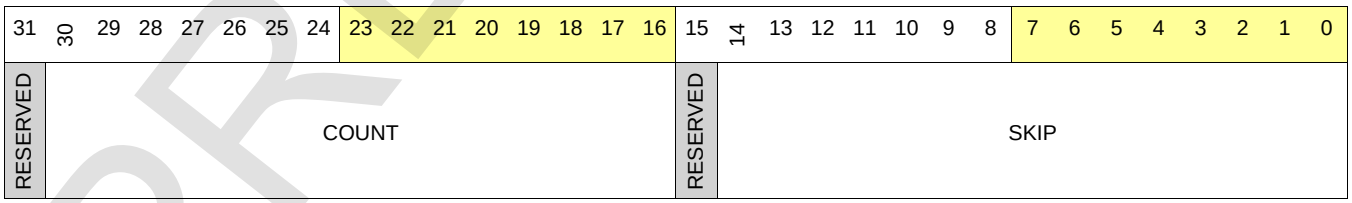
Bits	Field Name	Description	Type	Reset
31:29	RESERVED		R	0x0
28:16	COUNT	Defines the line count to be read from memory. From 1 to 8191 lines.	RW	0x0001
15:0	RESERVED		R	0x0000

Table 8-125. Register Call Summary for Register CCP2_LCM_VSIZE

ISS Interfaces
- ISS CCP2 Memory Read Channel: [0]
- ISS CCP2 Programming Memory Read Channel: [1]
- ISS CCP2 Registers: [2]

Table 8-126. CCP2_LCM_HSIZE

Address Offset	0x0000 01D8		
Physical Address	0x5200 1DD8	**Instance**	ISS_CCP2
Description	Memory read channel horizontal framing register.		
Type	RW		



Bits	Field Name	Description	Type	Reset
31	RESERVED		R	0x0
30:16	COUNT	Horizontal count of samples to output after the skipped pixels. Valid values: 1 to 32767.	RW	0x0001
15	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
14:0	SKIP	Horizontal count of samples to skip after the start of the line. When DPCM compressed data is read from memory using this feature is the only valid way to set a horizontal starting position. Valid values: 0 to 32767. 0 disables pixel skipping	RW	0x0000

Table 8-127. Register Call Summary for Register CCP2_LCM_HSIZE

ISS Interfaces
- ISS CCP2 Memory Read Channel: [0] [1] [2] [3] [4] [5] [6]
- ISS CCP2 Programming Memory Read Channel: [7] [8] [9] [10] [11]
- ISS CCP2 Registers: [12] [13]

Table 8-128. CCP2_LCM_PREFETCH

Address Offset	0x0000 01DC		
Physical Address	0x5200 1DDC	**Instance**	ISS_CCP2
Description	This register defines the amount of data to be fetched from memory. It must be consistent with the CCP2_LCM_HSIZE register (check programming model).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															HWORDS														RESERVED	

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:3	HWORDS	64 bit words to read from memory for each line of the image. Possible values 1..8191	RW	0x0001
2:0	RESERVED		R	0x0

Table 8-129. Register Call Summary for Register CCP2_LCM_PREFETCH

ISS Interfaces
- ISS CCP2 Memory Read Channel: [0]
- ISS CCP2 Programming Memory Read Channel: [1] [2]
- ISS CCP2 Registers: [3]

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Table 8-130. CCP2_LCM_SRC_ADDR

Address Offset	0x0000 01E0		
Physical Address	0x5200 1DE0	**Instance**	ISS_CCP2
Description	Memory channel source address register This register sets the 32-bit memory address where the pixel data are stored. The 5 LSBs are ignored: the address shall be aligned on a 32-byte boundary.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR																								RESERVED							

Bits	Field Name	Description	Type	Reset
31:5	ADDR	27 most-significant bits of the 32-bit address	RW	0x0000000
4:0	RESERVED		R	0x00

Table 8-131. Register Call Summary for Register CCP2_LCM_SRC_ADDR

ISS Interfaces

- ISS CCP2 Memory Read Channel: [0] [1]
- ISS CCP2 Programming Memory Read Channel: [2] [3]
- ISS CCP2 Registers: [4]

Table 8-132. CCP2_LCM_SRC_OFST

Address Offset	0x0000 01E4		
Physical Address	0x5200 1DE4	**Instance**	ISS_CCP2
Description	Memory channel source offset register. This register sets the offset, which is applied on the source address after each line is read from memory. For example, it enables to perform 2D data transfers of the pixel data from a frame buffer. In such case, the pixel data and frame buffer data shall have the same data format. The 5 LSBs are ignored: the offset shall be a multiple of 32 bytes.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OFST																								RESERVED							

Bits	Field Name	Description	Type	Reset
31:5	OFST	Line offset programmed in bytes. If OFST = 0, the data is read contiguously from memory. Otherwise, OFST sets the source offset between the first pixel of the previous line and the first pixel of the current line.	RW	0x0000000
4:0	RESERVED		R	0x00

Table 8-133. Register Call Summary for Register CCP2_LCM_SRC_OFST

ISS Interfaces

- ISS CCP2 Memory Read Channel: [0]
- ISS CCP2 Programming Memory Read Channel: [1] [2]
- ISS CCP2 Registers: [3]

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Table 8-134. CCP2_LCM_DST_ADDR

Address Offset	0x0000 01E8		
Physical Address	0x5200 1DE8	**Instance**	ISS_CCP2
Description	Memory channel destination address. This register sets the 32-bit memory address where the pixel data are stored. The 5 LSBs are ignored: the address shall be aligned on a 32-byte boundary.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR																											RESERVED			

Bits	Field Name	Description	Type	Reset
31:5	ADDR	27 most significant bits of the 32-bit address.	RW	0x0000000
4:0	RESERVED		R	0x00

Table 8-135. Register Call Summary for Register CCP2_LCM_DST_ADDR

ISS Interfaces

- ISS CCP2 Memory Read Channel: [0] [1]
- ISS CCP2 Programming Memory Read Channel: [2]
- ISS CCP2 Registers: [3]

Table 8-136. CCP2_LCM_DST_OFST

Address Offset	0x0000 01EC		
Physical Address	0x5200 1DEC	**Instance**	ISS_CCP2
Description	Memory channel destination offset register. This register sets the offset, which is applied on the destination address after each line is written to memory. For example, it enables to perform 2D data transfers of the pixel data into a frame buffer. In such case, the pixel data and frame buffer data shall have the same data format. The 5 LSBs are ignored: the offset shall be a multiple of 32 bytes.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OFST																											RESERVED			

Bits	Field Name	Description	Type	Reset
31:5	OFST	Line offset programmed in bytes. If OFST = 0, the data is written contiguously to memory if possible. At the end of a line only full 32 bit words will be written, creating eventually gaps at the end of lines. Otherwise, OFST sets the destination offset between the first pixel of the previous line and the first pixel of the current line.	RW	0x0000000
4:0	RESERVED		R	0x00

Table 8-137. Register Call Summary for Register CCP2_LCM_DST_OFST

ISS Interfaces

- ISS CCP2 Memory Read Channel: [0]
- ISS CCP2 Programming Memory Read Channel: [1]
- ISS CCP2 Registers: [2] [3]

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Table 8-138. CCP2_LCM_HISTORY

Address Offset	0x0000 01F0		
Physical Address	0x5200 1DF0	**Instance**	ISS_CCP2
Description	Controls operation of the DPCM history read/write feature		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														EN_HIST_RD	EN_HIST_WR	HIST_EXPORT															

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17	EN_HIST_RD	Enable DPCM history read 0x0: Disable 0x1: Enable	RW	0
16	EN_HIST_WR	Enable DPCM history write 0x0: Disable 0x1: Enable	RW	0
15:0	HIST_EXPORT	Defines the horizontal position at which DPCM history information is written. The first decoded sample of a line has position 0 The last decoded sample has position SKIP+COUNT–1 Valid range [3..SKIP+COUNT–1]	RW	0x0000

Table 8-139. Register Call Summary for Register CCP2_LCM_HISTORY

ISS Interfaces

- ISS CCP2 Memory Read Channel: [0] [1] [2] [3] [4] [5] [6] [7] [8]
- ISS CCP2 Registers: [9]

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8.2.5 ISS CSI2

8.2.5.1 ISS CSI2 Environment

8.2.5.1.1 ISS CSI2 Protocol and Data Format

The CSI2 supports MIPI CSI2 multiple data type formats. This section describes MIPI CSI2 protocol and data formats. The CSI2 is compatible with the *MIPI CSI2 Specification v1.0-01-00 r0.03*. Table 8-140 lists the MIPI CSI2 supported by CSI2 formats in addition to JPEG8. Shading in the primary and secondary MIPI CSI2-defined formats indicates special format extensions of the CSI2 receiver.

Table 8-140 summarizes the pixel formats supported by the CSI2 receiver interface.

Table 8-140. ISS CSI2 Pixel Format Modes

CSI2_CTX_CTRL2_i[9:0] Format	CSI2 Data Format	Bits per Pixel (BPP)	Data Size Increases in Memory	2D Mode Availability (1)	Comments
0x18	YUV4:2:0 8 bit	12	0%	Yes	
0x19	YUV4:2:0 10 bit	12	0%	Yes	
0x1E	YUV4:2:2 8 bit	16	0%	Yes	
0x1F	YUV4:2:2 10 bit	16	0%	Yes	
0x22	RGB565	16	0%	Yes	
0x24	RGB888	24	0%	Yes	
0x29	RAW7	7	0%	Yes	
0x2A	RAW8	8	8%	Yes	
0x2B	RAW10	10	0%	Yes	
0x2C	RAW12	12	0%	Yes	
0x2D	RAW14	14	0%	Yes	
0xA3	RGB666 + EXP32	32	77%	Yes	
0x68	RAW6 + EXP8	8	33%	Yes	
0x69	RAW7 + EXP8	8	14%	Yes	
0xA0	RGB444 + EXP16	16	33%	Yes	
0xA1	RGB555 + EXP16	16	6%	Yes	
0xAB	RAW10 + EXP16	16	60%	Yes	
0xAC	RAW12 + EXP16	16	33%	Yes	
0xAD	RAW14 + EXP16	16	14%	Yes	
0xE3	RGB666 + EXP32	32	77%	Yes	
0xE4	RGB888 + EXP32	32	33%	Yes	
0x2A8	RAW6 + DPCM10 + EXP16	16	166%	Yes	DPCM decompression
0x229	RAW7 + DPCM10 + EXP16	16	128%	Yes	DPCM decompression
0x2AA	RAW8 + DPCM10 + EXP16	16	100%	Yes	DPCM decompression
0x369	RAW7 + DPCM12 + EXP16	16	128%	Yes	DPCM decompression
0x36A	RAW8 + DPCM12 + EXP16	16	100%	Yes	DPCM decompression
0x3A8	RAW6 + DPCM12 + EXP16	16	166%	Yes	DPCM decompression
0x12	JPEG8	8	0%		

(1) If 2D mode is available, there are no supplementary constraints on data width. 2D mode does not apply when sending to the video port (VP).

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For more information about how the data formats are transmitted and how the data are stored in memory, see Section 8.2.5.1.1.4, *CSI2 Operating Modes*.

NOTE: The VP formats are not included in Table 8-140, because they are not sent to memory; instead they are sent to the ISP for further processing.

NOTE: Data written by CSI2 can be read back by the CCP2 read channel. CCP2 can get data from a sensor or memory. For more information about supported memory operations, see Table 8-56.

8.2.5.1.1.1 ISS CSI2 Physical Layer

The CSI2-A/CSI2-B receivers are tightly connected to a PHY layer (for more information about the PHY, see Section 8.2.3, *ISS CSI2 PHY*). Table 8-141 lists the CSI2-A receiver I/O, and Table 8-142 lists the CSI2-B I/O. The CSI2_RECEIVER provides access to the complex I/O register through a serial configuration port interface. Accesses performed to the CSI2_PHY_CFG_i register are forwarded to the complex I/O register at address i. The CSI2_RECEIVER can access up to eight 32-bit registers in each complex I/O (up to two complex I/Os supported).

Table 8-141. ISS CSI2-A I/O Description

Signal Name		I/O[1]	Description
csi2a_dx0	lane 0 (position 1)	I	Serial data/clock input
csi2a_dy0			
csi2a_dx1	lane 1 (position 2)	I	Serial data/clock input
csi2a_dy1			
csi2a_dx2	lane 2 (position 3)	I	Serial data/clock input
csi2a_dy2			
csi2a_dx3	lane 3 (position 4)	I	Serial data/clock input
csi2a_dy3			
csi2a_dx4	lane 4 (position 5)	I	Serial data input only
csi2a_dy4			

(1) I = Input

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Table 8-142. ISS CSI2-B I/O Description

Signal Name		I/O[1]	Description
csi2b_dx0	line 0 (position 1)	I	Serial data/clock input
csi2b_dy0			
csi2b_dx1	line 1 (position 2)	I	Serial data/clock input
csi2b_dy1			
csi2b_dx2	line 2 (position 3)	I	Serial data/clock input
csi2b_dy2			

(1) I = Input

NOTE: The serial lane can be used as clock lane or data lane (excluding lane 4 on the CSI2-A I/O). The MIPI CSI2 protocol requires one clock lane (others are data lane or unused lane).

Lanes support the two operating modes:

- HS mode: High-speed transmit mode
- Off mode: Lane is off.

8.2.5.1.1.2 ISS CSI2 Lane Merger

The layer consists of lane merger logic to merge the incoming serial stream into a byte stream. The lane merger can merge up to four lanes (CSI2-A) into a single byte stream. The bits are sent with the LSB first. The order of the lanes at the CSI2-A, CSI2-B receiver core depends on the lane configuration. The merger is not used for a single lane.

The number of lanes and their configuration can be changed only in ULPM or when all data lanes are in off mode.

Figure 8-36 to Figure 8-39 show the byte position into each serial link for one to four data lane configurations. The byte stream always starts from lane 1. It finishes on one of the lanes, depending on the number of bytes to receive and the number of lanes.

Figure 8-36. ISS CSI2 One Data-Lane Configuration

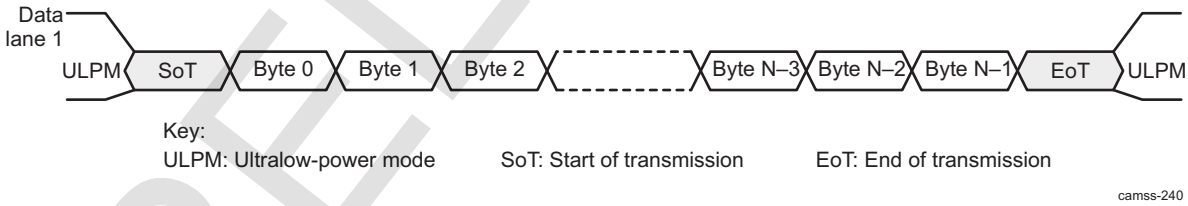

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Figure 8-37. ISS CSI2 Two Data-Lane Merger Configuration

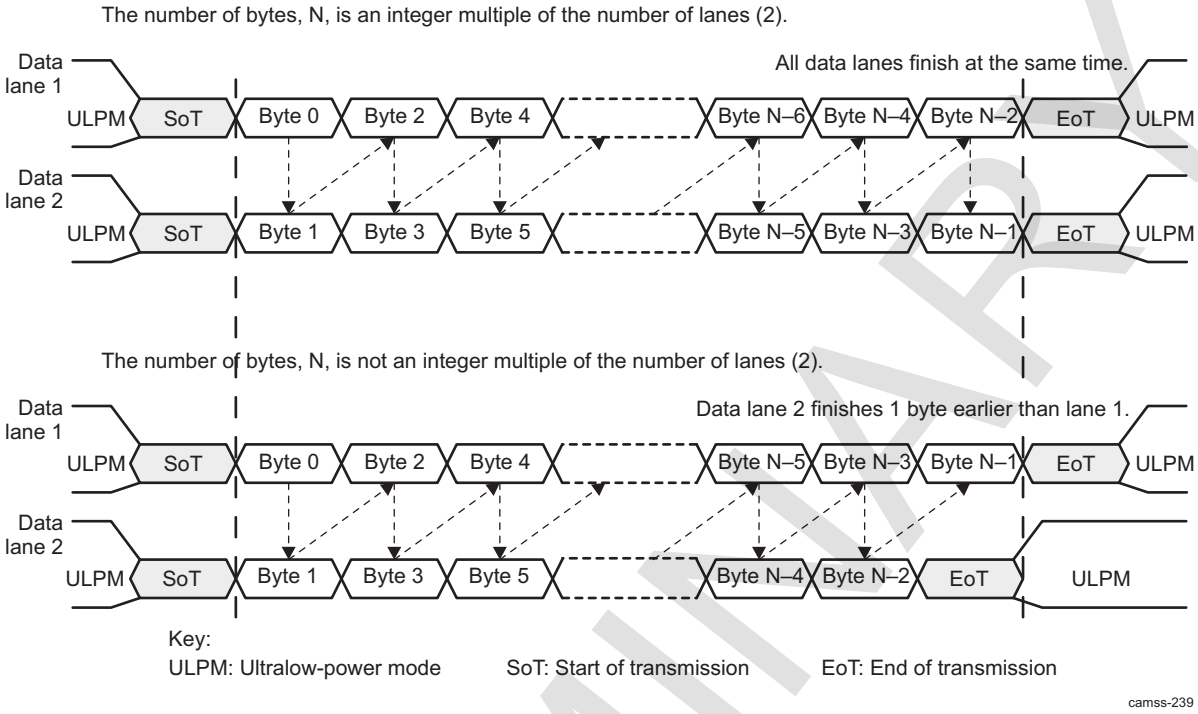

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Figure 8-38. ISS CSI2 Three Data-Lane Merger Configuration

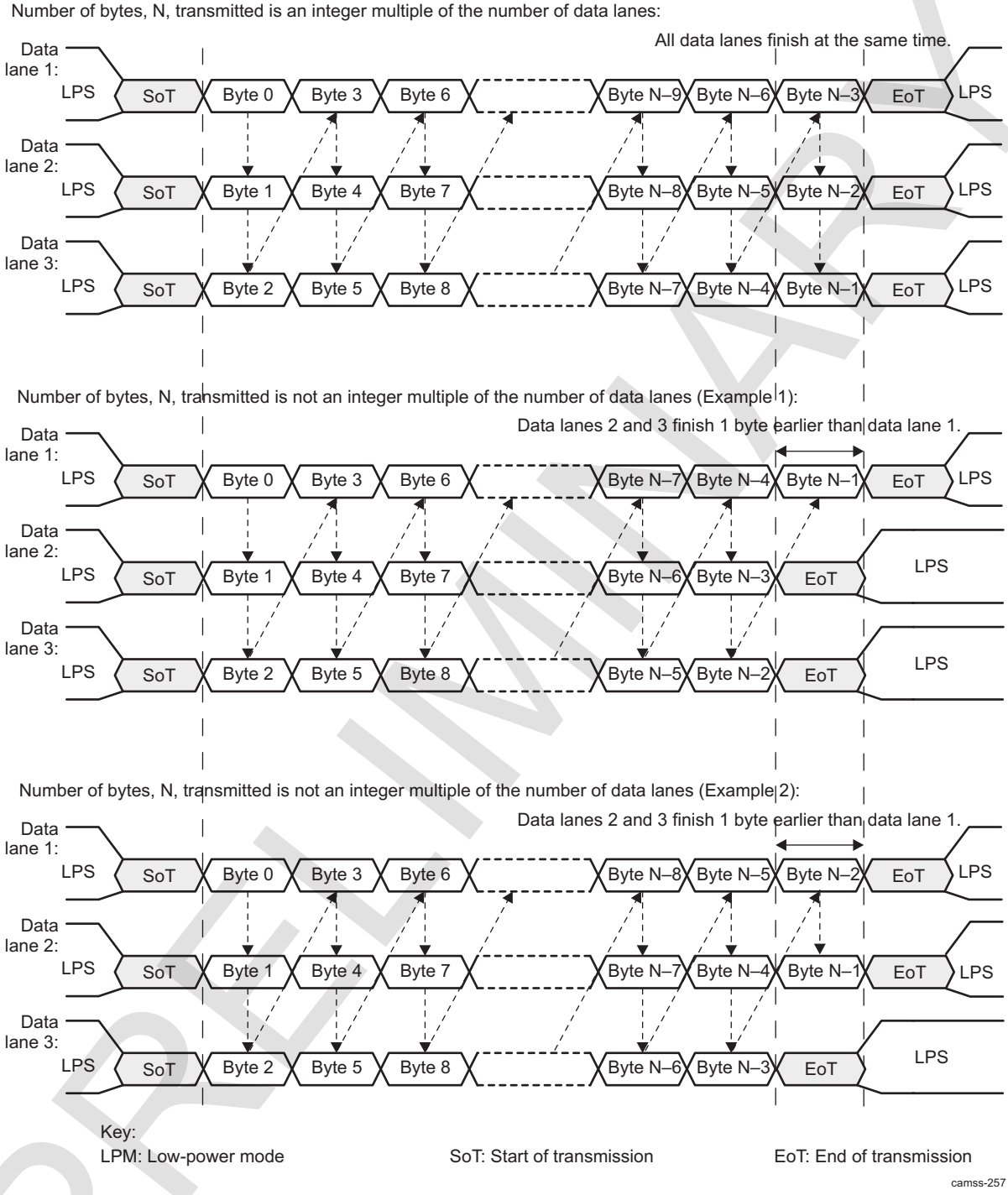

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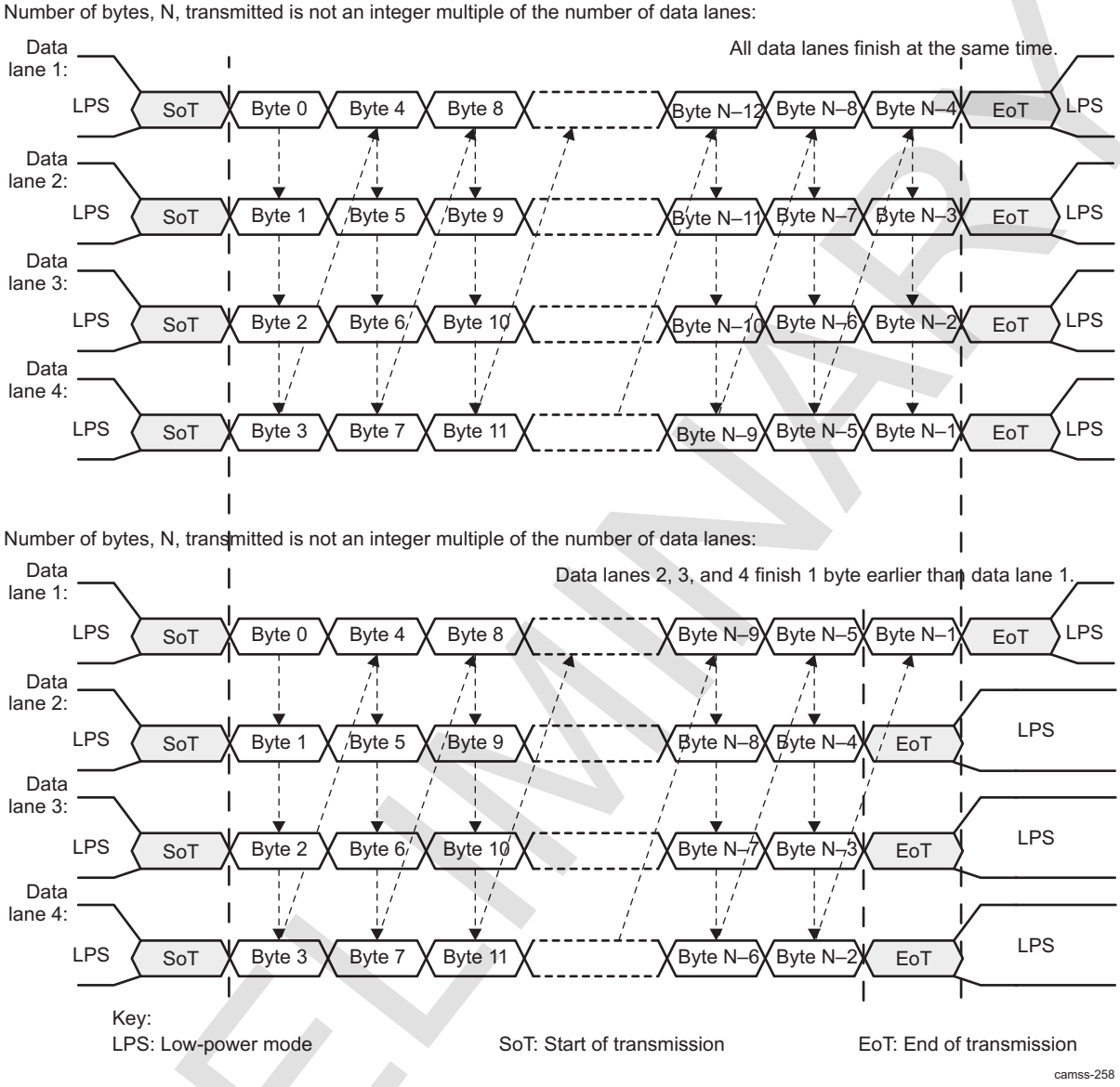
Figure 8-39. ISS CSI2 Four Data-Lane Merger Configuration



8.2.5.1.1.3 ISS CSI2 Protocol Layer

The low-level protocol (LLP) is a byte-oriented protocol from the lane merger layer. It supports short and long packet formats.

The CSI2 protocol layer defines how image-sensor data is transported onto the physical layer.

The feature set of the protocol layer implemented by the CSI2 receiver is:

- Transport of arbitrary data (payload-independent)
- 8-bit word size
- Support for up to four interleaved virtual channels on the same link
- Special packets for frame-start, frame-end, line-start, and line-end information
- Descriptor for the type, pixel depth, and format of application-specific payload data
- Error-correction code (ECC) for 1-bit error correction or 2-bit error detection in the header
- 16-bit checksum code for payload error detection

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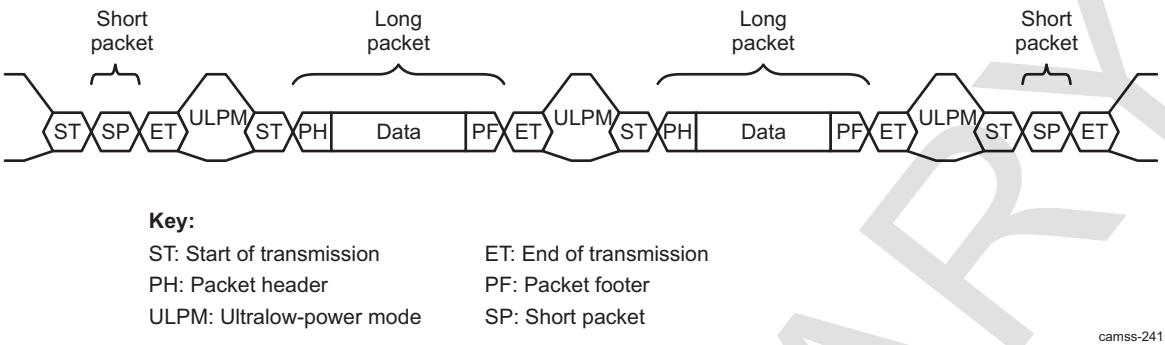
Figure 8-40 shows the CSI2 protocol layer with short and long packets.

Figure 8-40. ISS CSI2 Protocol Layer With Short and Long Packets

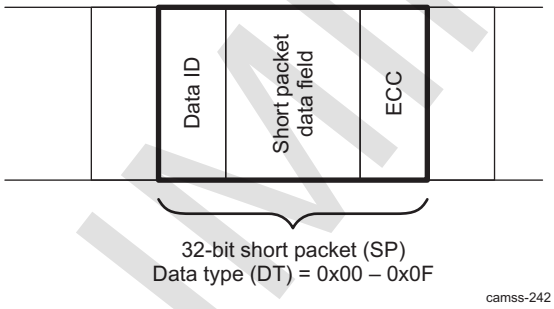


Two packets are always separated from each other with a sequence of ET, ULPM, and ST.

8.2.5.1.1.3.1 ISS CSI2 Short Packet

A short packet is identified by data types 0x00 to 0x0F. A short packet can be used for frame or line synchronization or for generic data. Figure 8-41 shows the structure of a short packet.

Figure 8-41. ISS CSI2 Short Packet Structure



For frame-synchronization data types, the short packet data field is the frame number. For line-synchronization data types, the short packet data field is the line number. For generic short packet data types, the content of the short packet data field is user-defined.

The 16-bit frame number, when used, is always nonzero to distinguish it from the use case where the frame number is inoperative and remains set to 0. The behavior of the 16-bit frame number is one of the following:

- The frame number is always 0 and is inoperative.
- The frame number increments by 1 for every FS packet within the same virtual channel and is periodically reset to 1 (1, 2, 1, 2, 1, 2, 1, 2 or 1, 2, 3, 4, 1, 2, 3, 4).

For LSC and LEC synchronization packets, the short packet data field contains a 16-bit line number. This line number is the same for the LS and LE packets corresponding to a given line. Line numbers are logical line numbers and do not necessarily equal physical line numbers. The 16-bit line number, when used, is always nonzero to distinguish it from the use case where the line number is inoperative and remains set to 0.

The behavior of the 16-bit line number is one of the following:

- The line number is always 0 and is inoperative.
- The line number increments by 1 for every LS packet within the same virtual channel and the same data type. The line number is periodically reset to 1 for the first LS packet after an FS packet. The intended use is for progressive scan (noninterlaced) video data streams. The line number must be a nonzero value.
- The line number increments by the same arbitrary step value greater than 1 for every LS packet within the same virtual channel and the same data type. The line number is periodically reset to a nonzero

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arbitrary start value for the first LS packet after an FS packet. The arbitrary start value can be different between successive frames. The intended use is for interlaced video data streams.

The ECC byte allows single-bit errors to be corrected and 2-bit errors to be detected in the short packet.

Short packets apply to all contexts using the same virtual channel ID (up to eight contexts support eight dedicated configurations of virtual channel ID and data types). The data type associated with the context is not used to distinguish which context is used when receiving short packets.

8.2.5.1.1.3.2 ISS CSI2 Long Packet

A long packet is identified by data types 0x10 to 0x37. A long packet consists of three elements:

- A 32-bit packet header (PH)
- An application-specific data payload with a variable number of 8-bit data words
- A 16-bit packet footer (PF)

The packet header is composed of three elements:

- An 8-bit data identifier
- A 16-bit word count field
- An 8-bit ECC

The packet footer has one element, a 16-bit checksum.

Figure 8-42 and Table 8-143 show the structure of a long packet.

Figure 8-42. ISS CSI2 Long Packet Structure

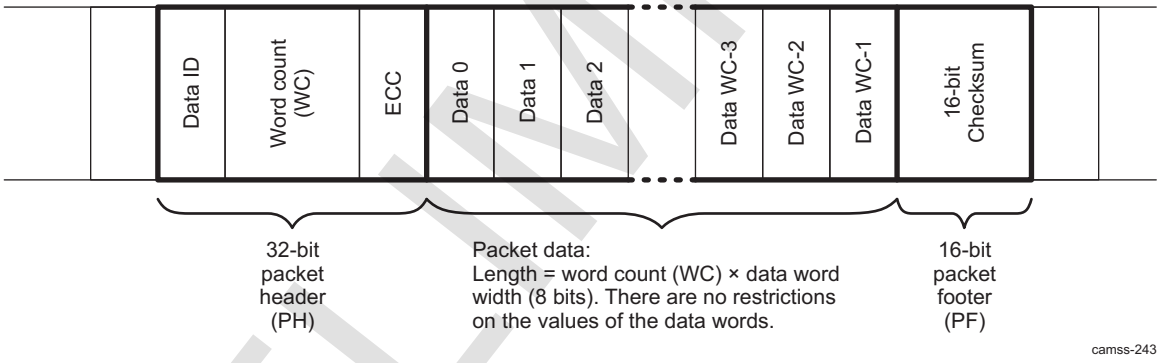

Table 8-143. ISS CSI2 Long Packet Structure Description

Packet Part	Field Name	Size (Bits)	Description
Header	Data ID	8	Contains the virtual channel identifier and the data-type information
	Word count	16	Number of data words in the packet data. A word is 8 bits.
	ECC	8	ECC for data ID and WC field. Allows 1-bit error recovery and 2-bit error detection.
Data	Data	WC-8	Application-specific payload (WC words of 8 bits)
Footer	Checksum	16	16-bit CRC for packet data

There are no restrictions on the size of the packet data, but each data format can impose additional restrictions on the length of the payload data (for example, a multiple of 4 bytes).

8.2.5.1.1.3.3 ISS CSI2 Data Identifier

The data identifier byte contains the virtual channel (VC) value and the data-type (DT) value, as shown in Figure 8-43. The VC value is in the 2 MSBs of the data identifier byte. The DT value is in the 6 LSBs of the data identifier byte.

Figure 8-43 shows the data identifier structure.

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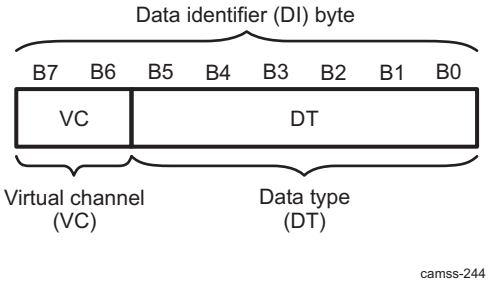
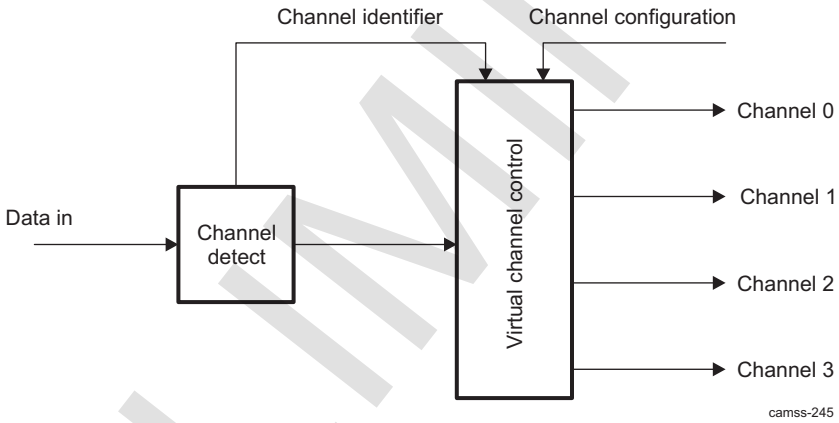
Figure 8-43. ISS CSI2 Data Identifier Structure



Virtual Channel

The CSI2 protocol layer transports virtual channels. Virtual channels are built of frames. A frame can comprise embedded data and image-sensor data. Two contexts are used to send the two types of data separately. Each frame is identified by unique mandatory synchronization codes: frame start and frame end. Line start and line end synchronization codes are optional for the transmitter. A set of registers is associated with each context defined by the virtual channel ID and the data type. Figure 8-44 shows a virtual channel.

Figure 8-44. ISS CSI2 Virtual Channel



Pixel Formats

8.2.5.1.1.3.4 ISS CSI2 Synchronization Codes

Data reception from the image-sensor module uses four synchronization codes embedded in the serial bitstream:

- FSC: Identifies the start of a new frame
- LSC: Identifies the start of a new line; received for every line
- LEC: Identifies the end of a line; received for every line
- FEC: Identifies the end of the last line and the end of the current frame

Table 8-144 summarizes the synchronization code values.

Table 8-144. ISS CSI2 Synchronization Codes

Synchronization Code	Value	Comments
FSC	0x0	Mandatory
FEC	0x1	Mandatory
LSC	0x2	Optional
LEC	0x3	Optional
Reserved	0x4 to 0x7	Not used

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8.2.5.1.1.3.5 ISS CSI2 Generic Short Packet Codes

When the synchronization code value is from 0x8 to 0xF, the short packet is called a generic short packet. Short packets are not processed by the camera interface hardware. A generic short packet is stored in a register without the ECC and an interrupt can be generated. Therefore, generic short packets must be handled by software.

8.2.5.1.1.3.6 ISS CSI2 Generic Long Packet Codes

The code value 0x10 indicates null packets, which can be received at any time. They are discarded by the protocol engine.

The code value 0x11 indicates blanking packets, which can be received at any time. They are discarded by the protocol engine.

The code value 0x12 indicates embedded 8-bit nonimage data typically used for JPEG.

Code values from 0x13 to 0x17 are reserved.

8.2.5.1.1.3.7 ISS CSI2 Frame Structure

Each frame consists of short packets to indicate SOF and EOF. Optional short packets for start of line and end of line can be sent by the image sensor.

Some information before and after the picture data can be sent as SOF and EOF information by the image sensor to the memory through the L3 port.

For each frame, the pixel data (arbitrary data or user-defined byte data) are valid only after an SOF short packet. If the data are invalid, they are discarded by the protocol engine.

A frame contains embedded data and image-sensor data. Figure 8-45 shows where the embedded data and image-sensor data are in the frame. The frame is scanned in raster order starting from the top-left corner, as shown in Figure 8-45 and Figure 8-46. The following definitions for a frame apply:

- Zero or more SOF status lines (SOF lines) can be embedded at the beginning of a CSI2 frame.
- The image embedded data is carried using separate data types and virtual channels (see Section 8.2.4.1.1, *ISS CCP2 Protocol and Data Formats*, and Section 8.2.5.3.3.4, *ISS CSI2 Virtual Channel and Context*).
- Zero or more EOF status lines (EOF lines) can be embedded at the end of a CSI2 frame.
- The SOF lines, pixel data, and EOF lines do not overlap.

The CSI2 receiver does not use the information in the status lines. However, it extracts it and stores it in memory for use by software.

Because the data types are different, the data is carried using separate data types called virtual channels. Those must be mapped to the adequate context. The CSI2 receiver uses a different context for embedded data and image-sensor data. See Section 8.2.5.3.3.4, *ISS CSI2 Virtual Channel and Context*.

Embedded data is supported as a context by the CSI2 receiver; therefore, there is no specific hardware support for embedded data.

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Figure 8-45. ISS CSI2 General Frame Structure (Informative)

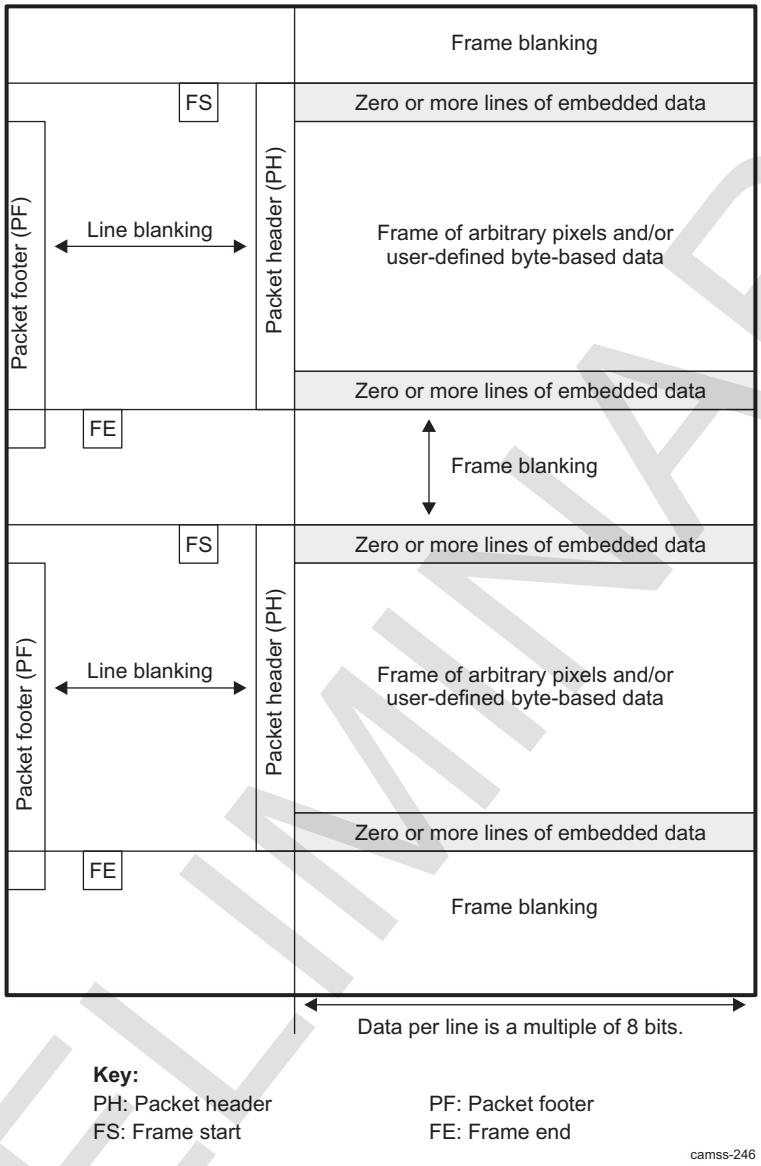

Figure 8-46 shows the frame structure of a YUV4:2:2 interlaced video frame without embedded data.

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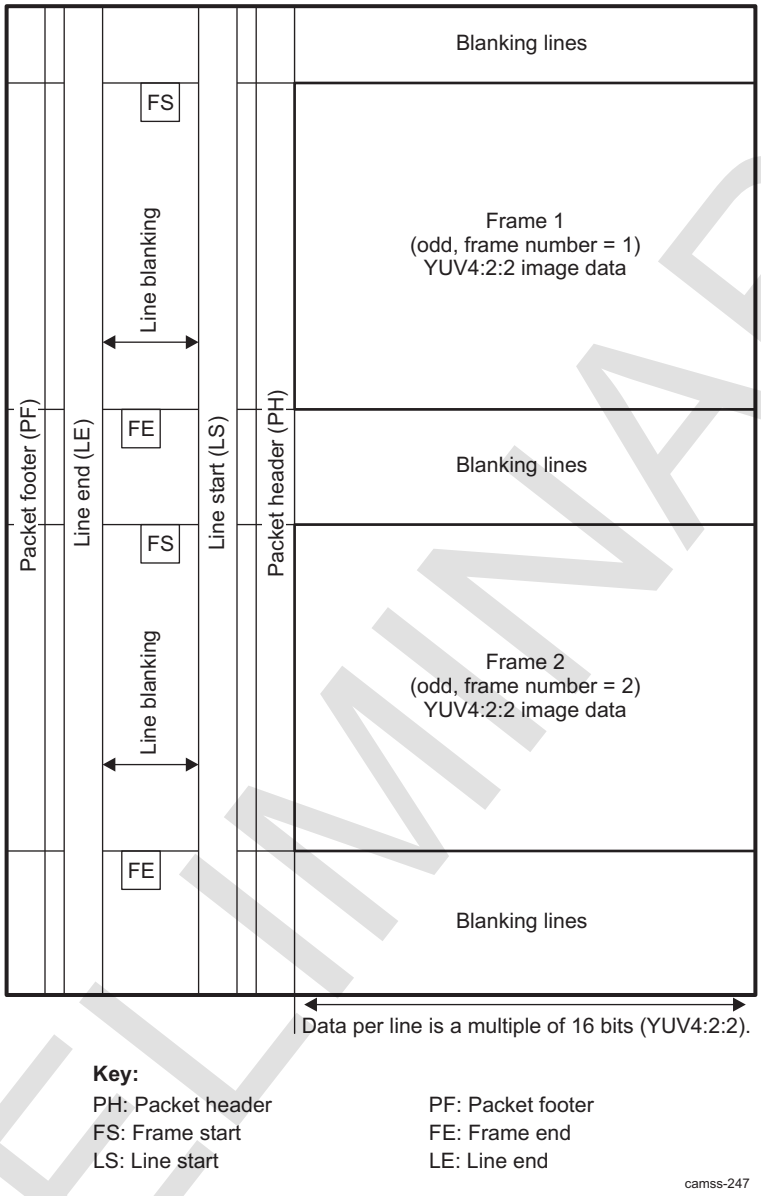
Figure 8-46. ISS CSI2 Digital Interlaced Video Frame (Informative)



The period between the LEC and the new LSC is the line blanking period. The time between the FEC and the new FSC is the frame blanking period. The receiver works with the line blanking period set to 0. The image data is stored in memory by selecting one of the various operating modes. Section 8.2.5.1.1.4, *ISS CSI2 Operating Modes*, explains storing image data frames into memory.

8.2.5.1.1.4 ISS CSI2 Operating Modes

8.2.5.1.1.4.1 ISS CSI2 YUV Operating Modes

8.2.5.1.1.4.1.1 ISS CSI2 YUV4:2:0 8-Bit

YUV4:2:0 8-bit data can be stored to memory in little-endian and big-endian format. To set the endianness for YUV4:2:0 use the CSI2_CTRL[4] ENDIANNESS bit. The line length sent through the CSI2 physical protocol is a multiple of 16 bits for odd lines and 32 bits for even lines.

For correct pixel reconstruction, the line length must be a multiple of 32 bits and the number of lines must

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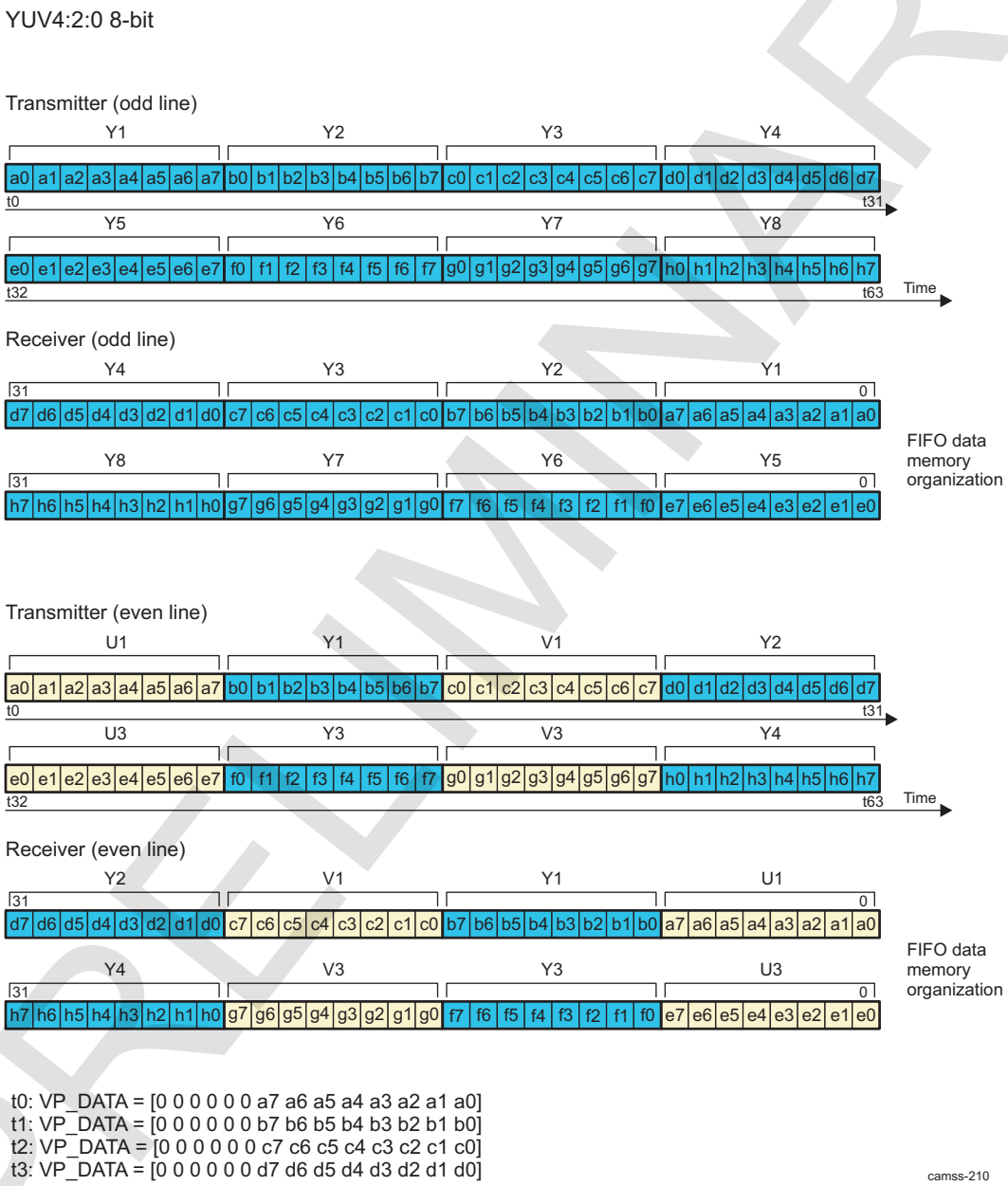
be even. Figure 8-47 shows the storage format for YUV4:2:0 8-bit data. It is shown as little endian. If the data format is big endian, the figure changes accordingly. Set the CSI2_CTX_CTRL2_i[9:0] FORMAT bit field to 0x18 to select YUV4:2:0 8-bit mode. Even and odd lines do not have the same length. Offset must be set accordingly with the CSI2_CTX_DAT_OFST_i[16:5] OFST bit field; for example, if the offset is 0, the data is written in a contiguous way (bit-to-bit of odd and even lines). If the data has an offset, set the destination offset between the first pixel of the previous line and the first pixel of the current line being written to memory.

Figure 8-47. ISS CSI2 YUV4:2:0 8-Bit



8.2.5.1.1.4.1.2 ISS CSI2 YUV4:2:0 10-Bit

YUV4:2:0 10-bit data can be stored to memory in little-endian and big-endian format. The line length sent through the CSI2 physical protocol is a multiple of 40 bits for odd lines and 80 bits for even lines. Figure 8-48 shows the storage format for YUV4:2:0 10-bit data. Set the CSI2_CTX_CTRL2_i[9:0] FORMAT bit field to 0x19 to select YUV4:2:0 10-bit mode. Even and odd lines do not have the same length. Offset must be set accordingly with the CSI2_CTX_DAT_OFST_i[16:5] OFST bit field.

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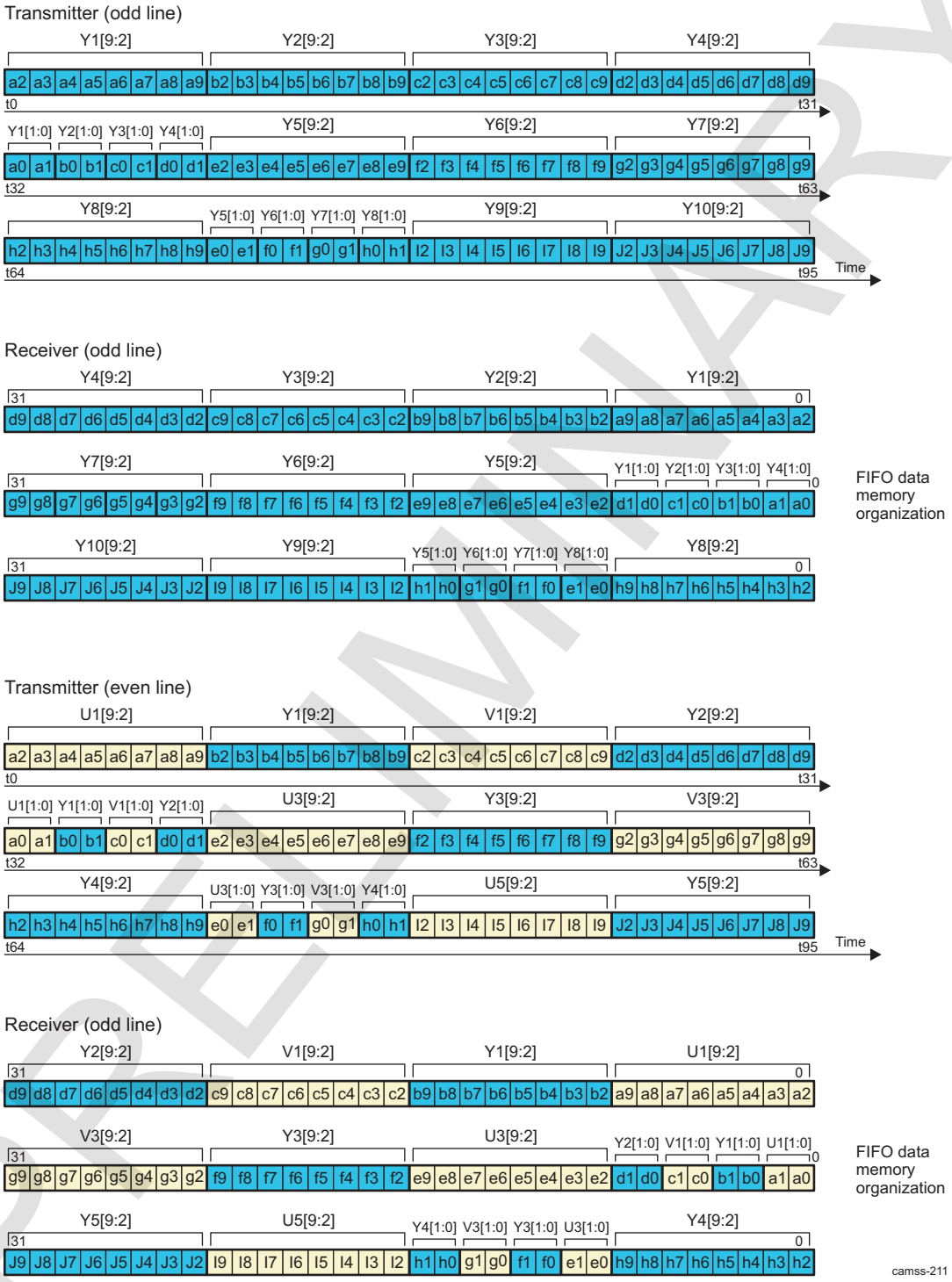
Figure 8-48. ISS CSI2 YUV4:2:0 10-Bit



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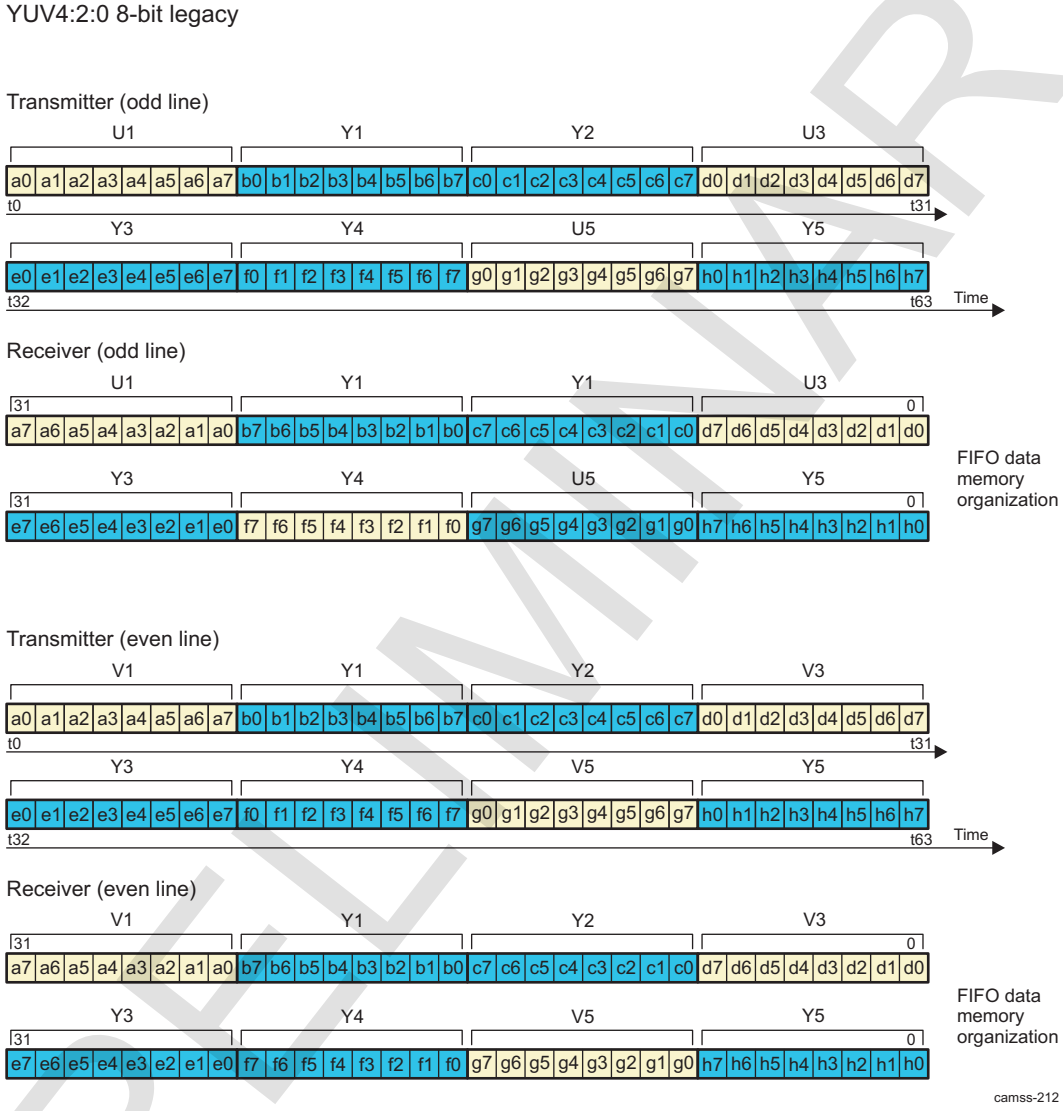
8.2.5.1.1.4.1.3 CSI2 YUV4:2:0 8-Bit Legacy

YUV4:2:0 8-bit legacy data can be stored to memory in little-endian and big-endian format. The line length sent through the CSI2 physical protocol is a multiple of 4 bytes. Figure 8-49 shows the storage format for YUV4:2:0 8-bit legacy data. Set the CSI2_CTX_CTRL2_i[9:0] FORMAT bit field to 0x1A to select YUV4:2:0 8-bit legacy mode.

Figure 8-49. ISS CSI2 YUV4:2:0 8-Bit Legacy



8.2.5.1.1.4.1.4 ISS CSI2 YUV4:2:0 8-Bit + CSPS

YUV4:2:0 8-bit CSPS data can be stored to memory in little-endian and big-endian format. The line length sent through the CSI2 physical protocol is a multiple of 16 bits for odd lines and 32 bits for even lines.

For correct pixel reconstruction, the line length must be a multiple of 3 32 bits and the number of lines must be even. Figure 8-50 shows the storage format for YUV4:2:0 8-bit + CSPS data. Set the CSI2_CTX_CTRL2_i[9:0] FORMAT bit field to 0x1C to select YUV4:2:0 8-bit + CSPS mode.

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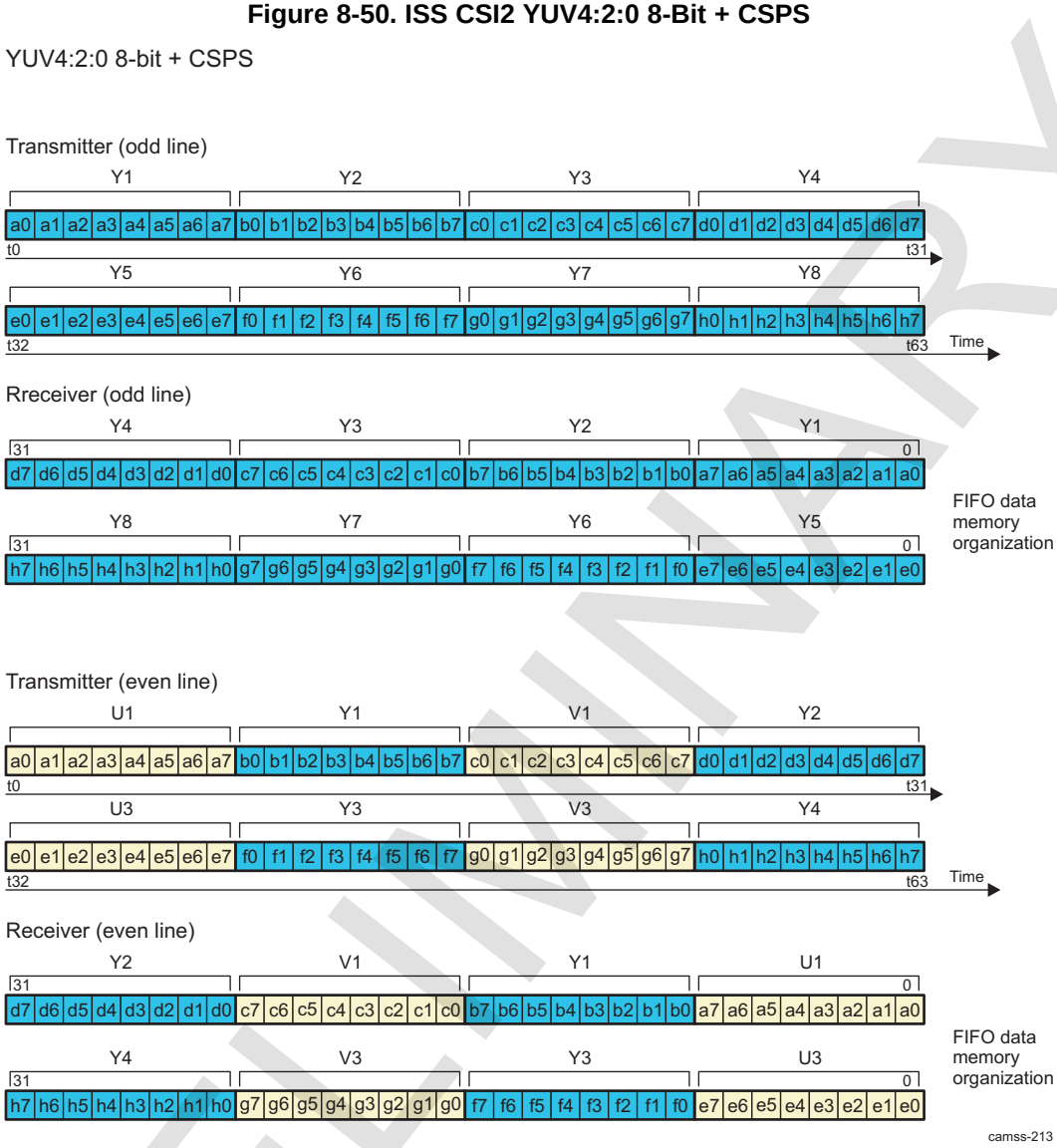
Figure 8-50. ISS CSI2 YUV4:2:0 8-Bit + CSPS



8.2.5.1.1.4.1.5 Camera ISP CSI2 Byte Swap

The CSI2 receiver incorporates a byte-swapping function. Software can optionally enable byte-swapping of the payload data by setting the CSI2_CTx_CTRL1[31] BYTESWAP bit. This feature must be used only when the amount of payload data per packet is a multiple of 16 bits. The byte-swapping is performed before pixel reconstruction.

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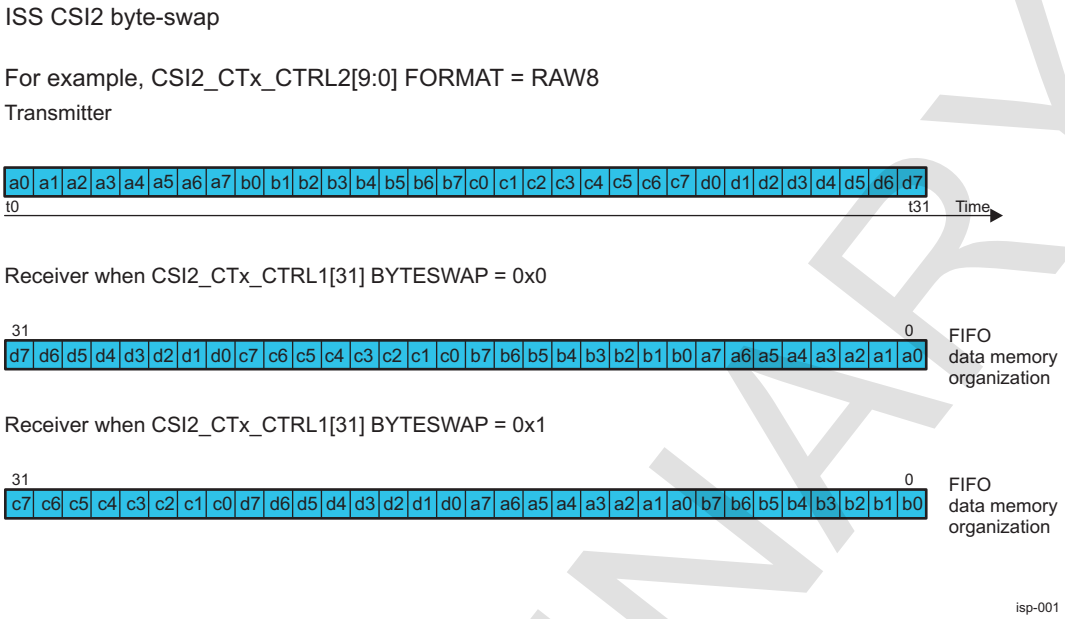
Figure 8-51. Camera ISP CSI2 Byte Swap



8.2.5.1.1.4.1.6 ISS CSI2 YUV4:2:0 10-Bit + CSPS

YUV4:2:0 10-bit CSPS data can be stored to memory in little-endian and big-endian format. The line length sent through the CSI2 physical protocol is a multiple of 40 bits for odd lines and 80 bits for even lines.

For correct pixel reconstruction, the line length must be a multiple of 3 32 bits and the number of lines must be even. Figure 8-52 shows the storage format for YUV4:2:0 10-bit + CSPS data. Set the CSI2_CTX_CTRL2_i[9:0] FORMAT bit field to 0x1D to select YUV4:2:0 10-bit + CSPS mode.

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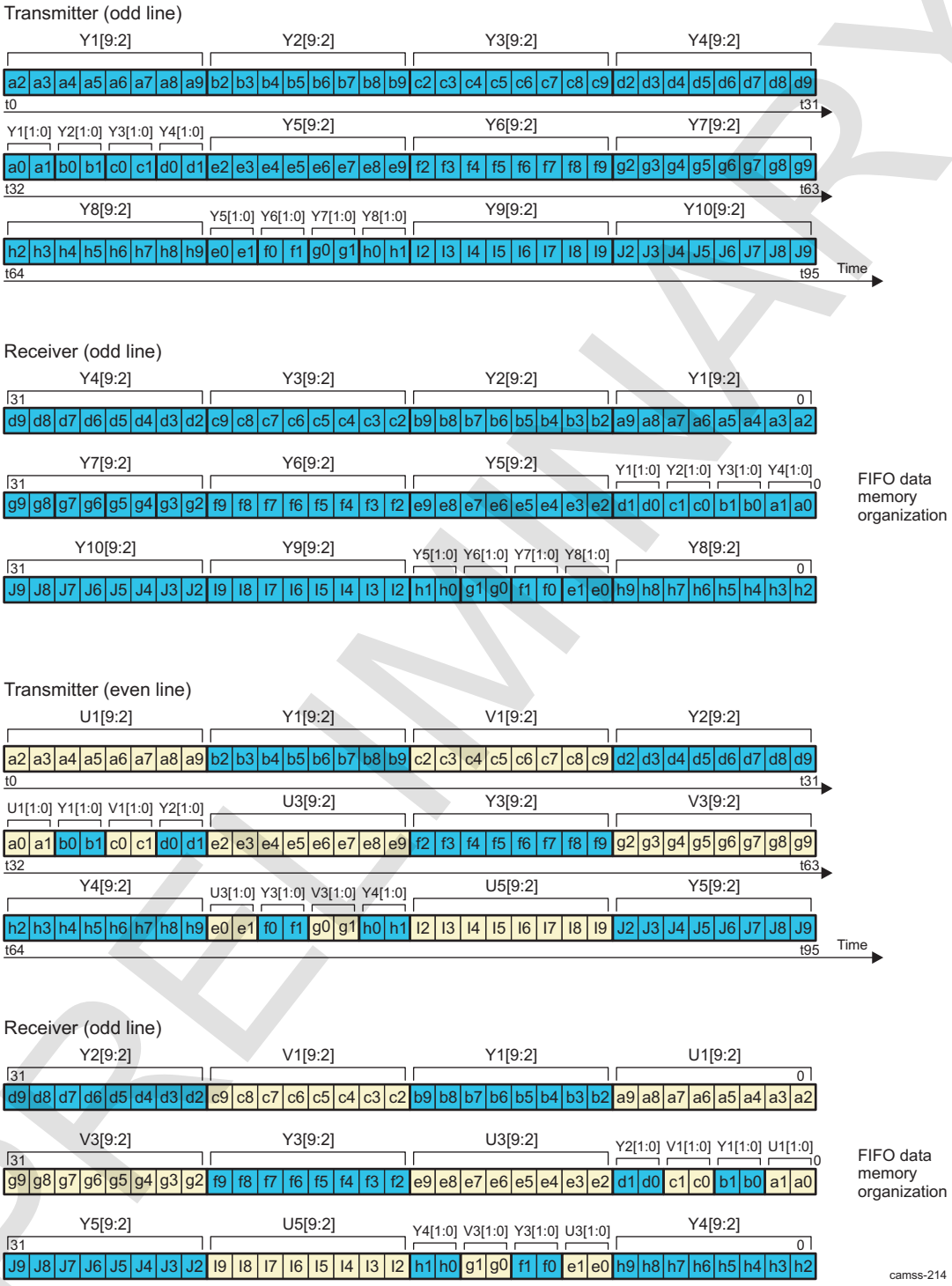
Figure 8-52. ISS CSI2 YUV4:2:0 10-Bit + CSPS



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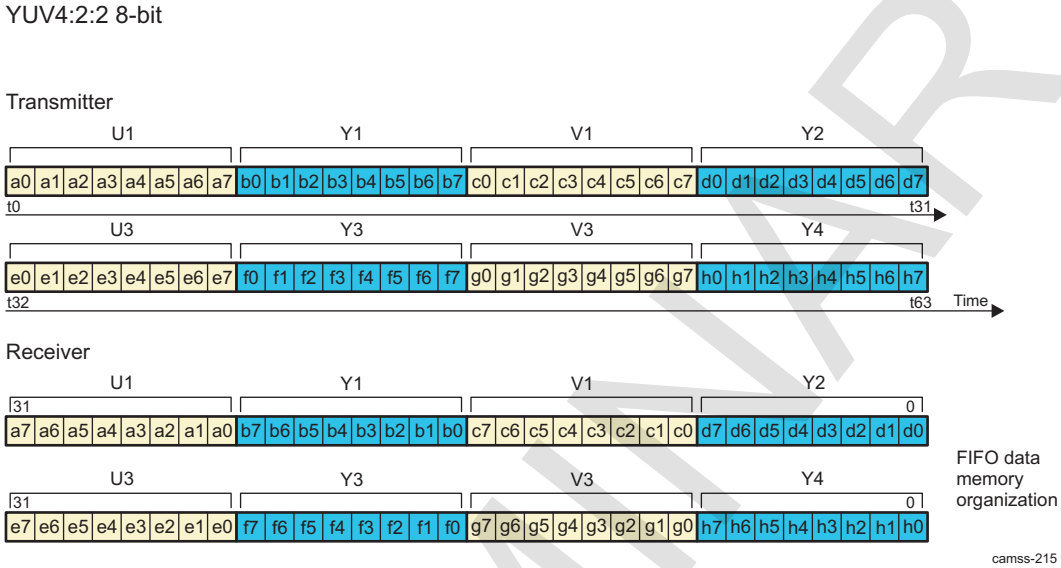
8.2.5.1.1.4.1.7 ISS CSI2 YUV4:2:2 8-Bit

YUV4:2:2 data can be stored to memory in little-endian and big-endian format. To set the endianness for YUV4:2:2 use the CSI2_CTRL[4] ENDIANNESS bit. The line length sent through the CSI2 physical protocol is a multiple of 32 bits. Figure 8-53 shows the storage format for YUV4:2:2 8-bit data. Set the CSI2_CTX_CTRL2_i[9:0] FORMAT bit field to 0x1E to select YUV4:2:2 8-bit mode.

Figure 8-53. ISS CSI2 YUV4:2:2 8-Bit



8.2.5.1.1.4.1.8 CSI2 YUV4:2:2 10-Bit

YUV4:2:2 data can be stored to memory in little-endian and big-endian format. The line length sent through the CSI2 physical protocol is a multiple of 40 bits. Figure 8-54 shows the storage format for YUV4:2:2 10-bit data. Set the CSI2_CTX_CTRL2_i[9:0] FORMAT bit field to 0x1F to select YUV4:2:2 10-bit mode.

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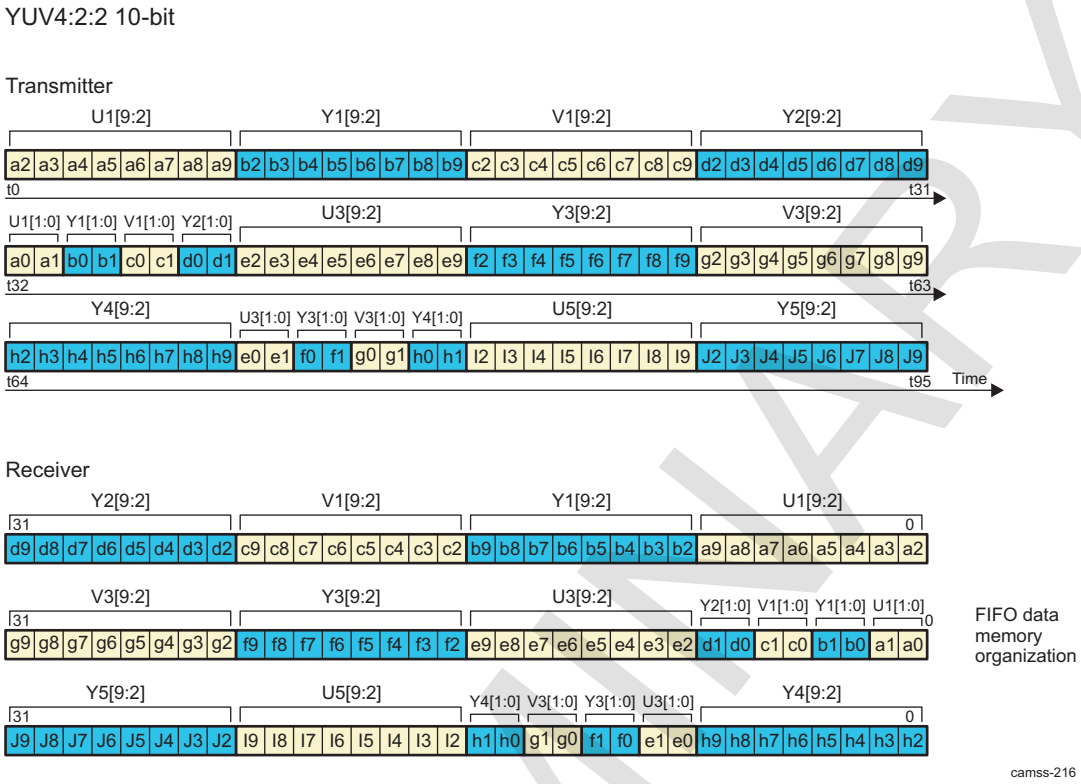
Figure 8-54. ISS CSI2 YUV4:2:2 10-Bit

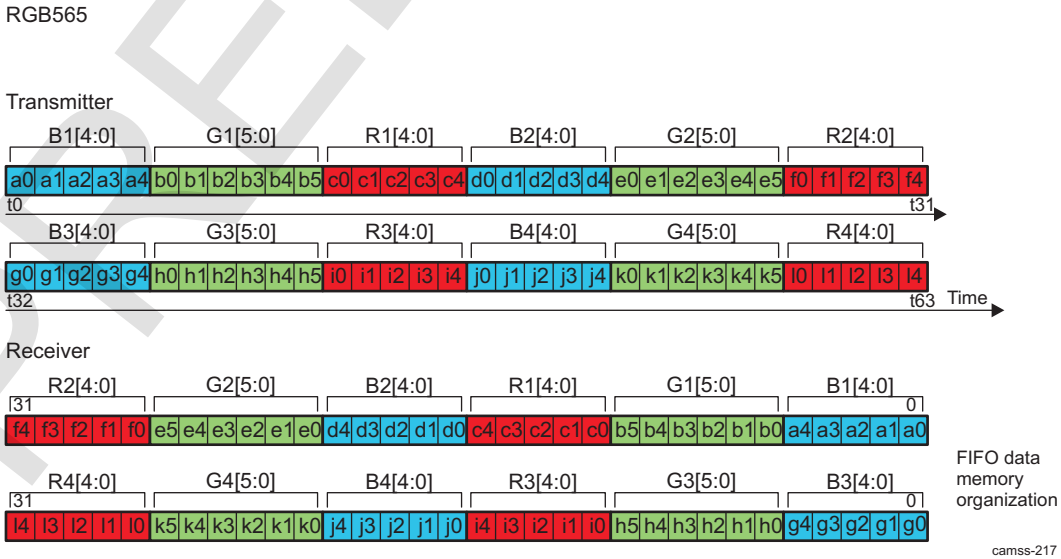


8.2.5.1.1.4.2 ISS CSI2 RGB Operating Modes

8.2.5.1.1.4.2.1 ISS CSI2 RGB565

RGB565 data is output to memory without data expansion. The line length sent through the CSI2 physical layer is always a multiple of 16 bits. Figure 8-55 shows the storage format for RGB565 data. Set the CSI2_CTX_CTRL2_i[9:0] FORMAT bit field to 0x22 to select RGB565 mode.

Figure 8-55. ISS CSI2 RGB565



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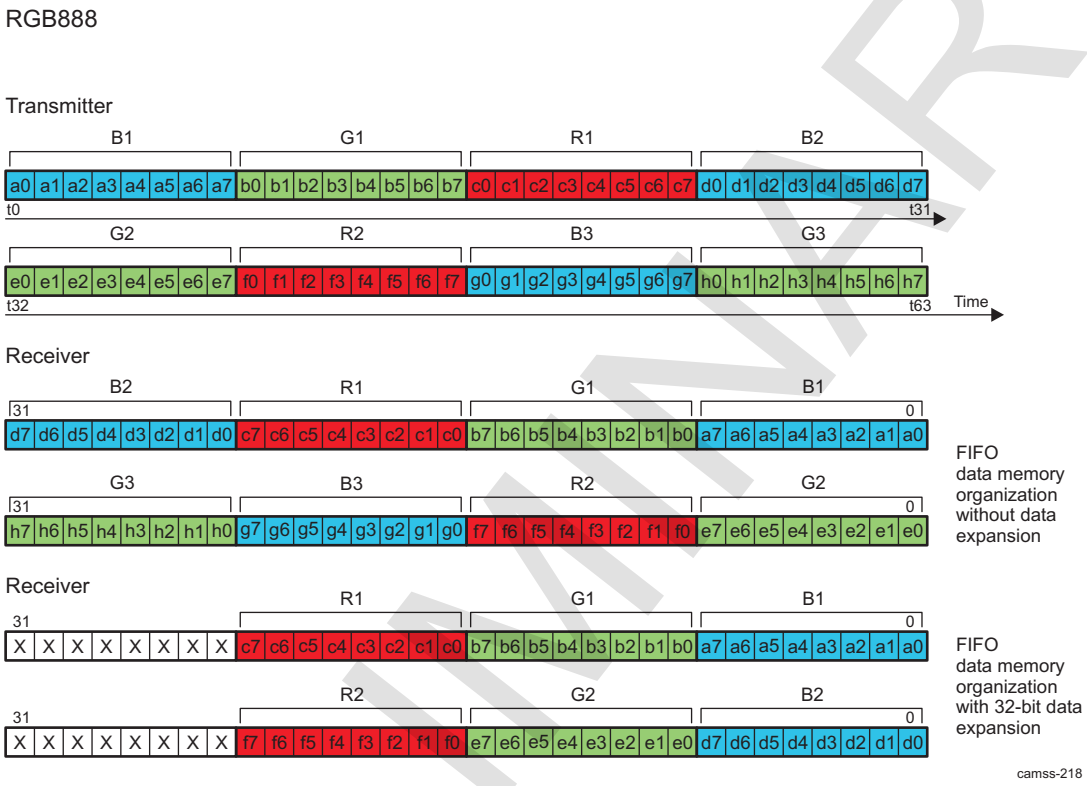
8.2.5.1.1.4.2.2 ISS CSI2 RGB888

RGB888 data can be output to memory in two formats: with or without data expansion. If data expansion is used, the value of the 8 upper bits is programmable and can be set with an alpha value for computer graphics applications (the CSI2_CTX_CTRL3_i[29:16] ALPHA bit field). Figure 8-56 shows the storage format for RGB888 data. Set the CSI2_CTX_CTRL2_i[9:0] FORMAT bit field to 0x24 to select RGB888 mode.

Figure 8-56. ISS CSI2 RGB888



8.2.5.1.1.4.2.3 ISS CSI2 RGB666

RGB666 data is always output to memory with data expansion. The value of the 14 upper bits is programmable and can be set with an alpha value for computer graphics applications (the CSI2_CTX_CTRL3_i[29:16] ALPHA bit field). The line length sent through the CSI2 physical protocol is a multiple of 8 bits. Furthermore, the line length is a multiple of 9 × 8 bits to finish the pixel reconstruction correctly. Figure 8-57 shows the storage format for RGB666 data. Set the CSI2_CTX_CTRL2_i[9:0] FORMAT bit field to 0x33 to select RGB666 mode.

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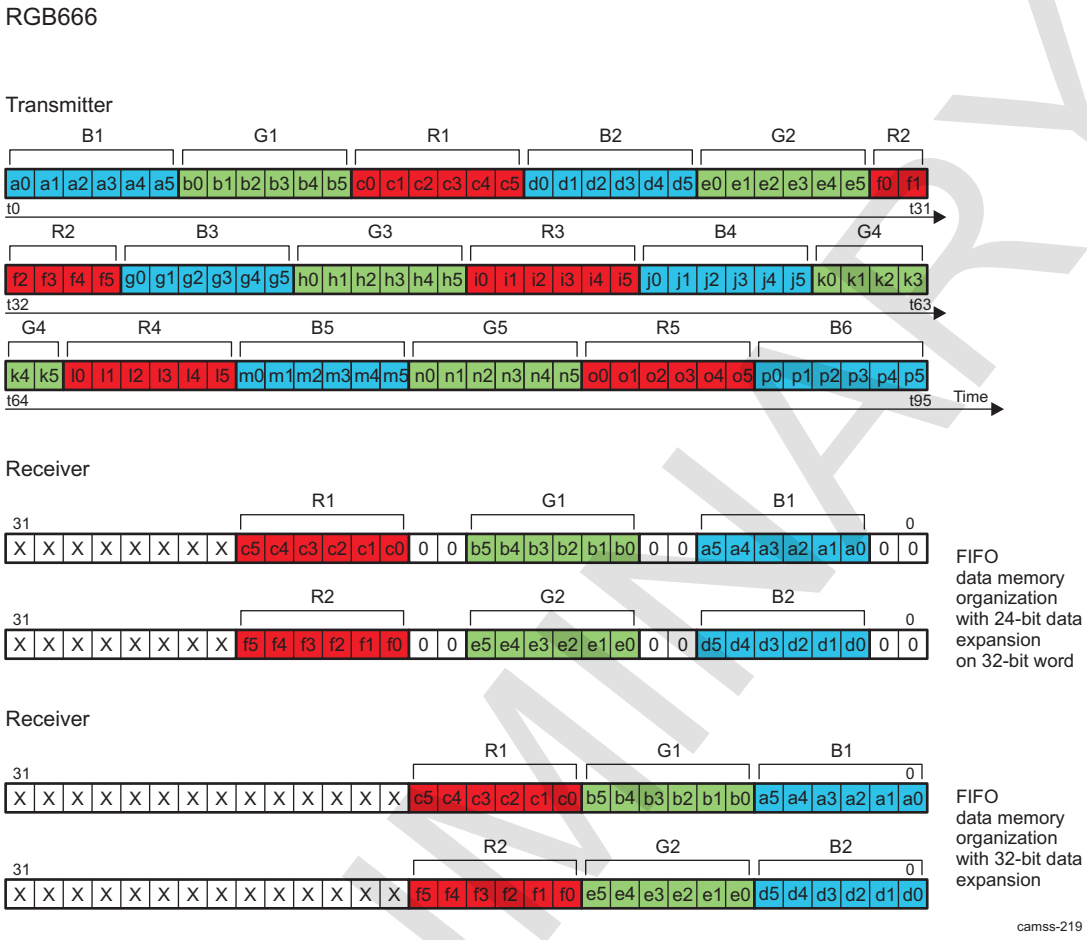
Figure 8-57. ISS CSI2 RGB666



8.2.5.1.1.4.2.4 ISS CSI2 RGB444

RGB444 data is output to memory with data expansion. When data expansion is used, the value of the 4 upper bits is programmable and can be set with an alpha value for computer graphics applications (the CSI2_CTX_CTRL3_i[29:16] ALPHA bit field). Figure 8-58 shows the storage format for RGB444 data. Set the CSI2_CTX_CTRL2_i[9:0] FORMAT bit field to 0xA0 to select RGB444 mode.

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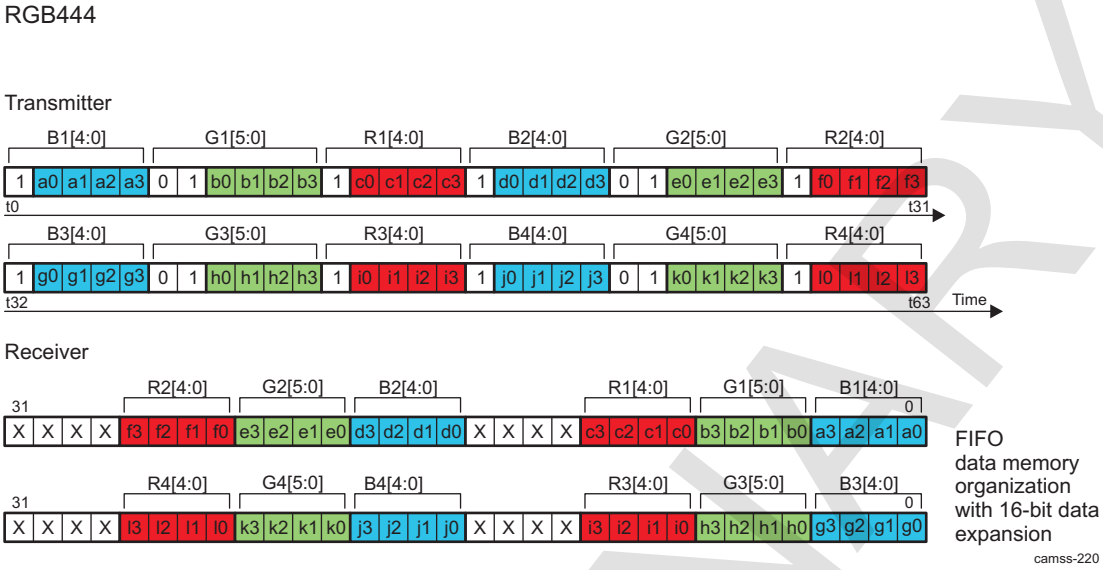
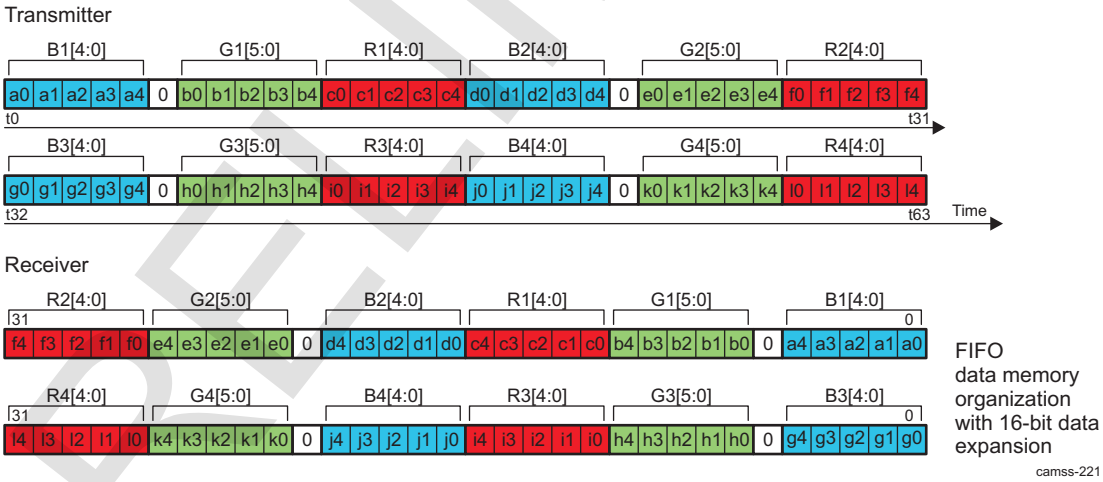
Figure 8-58. ISS CSI2 RGB444



8.2.5.1.1.4.2.5 ISS CSI2 RGB555

RGB555 data is output to memory with data expansion. Figure 8-59 shows the storage format for RGB555 data. Set the CSI2_CTX_CTRL2_i[9:0] FORMAT bit field to 0xA1 to select RGB555 mode.

Figure 8-59. ISS CSI2 RGB555



8.2.5.1.1.4.3 ISS CSI2 RAW Bayer RGB Operating Modes

8.2.5.1.1.4.3.1 ISS CSI2 RAW6

RAW6 data can be output to memory with or without data expansion. The line length sent through the CSI2 physical layer is a multiple of 8 bits (6-bit image data + 2-bit expansion). Furthermore, the line length is a multiple of 3 × 8 bits to complete the pixel reconstruction correctly (the lowest common multiple of 8 and 6 is 24, so 3 × 8 bits). Figure 8-60 shows the storage format for RAW6 data. Set the CSI2_CTX_CTRL2_i[9:0] FORMAT bit field as follows:

- To 0x28 to select RAW6 mode

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- To 0x68 for RAW6 + 8-bit expansion
- To 0xE8 for RAW6 + DPCM decompression to 10-bit to video port
- To 0x2A8 for RAW6 + DPCM decompression to 10-bit expanded to 16-bit
- To 0x3A8 for RAW6 + DPCM decompression to 12-bit expanded to 16-bit
- To 0x368 for RAW6 + DPCM decompression to 12-bit to video port

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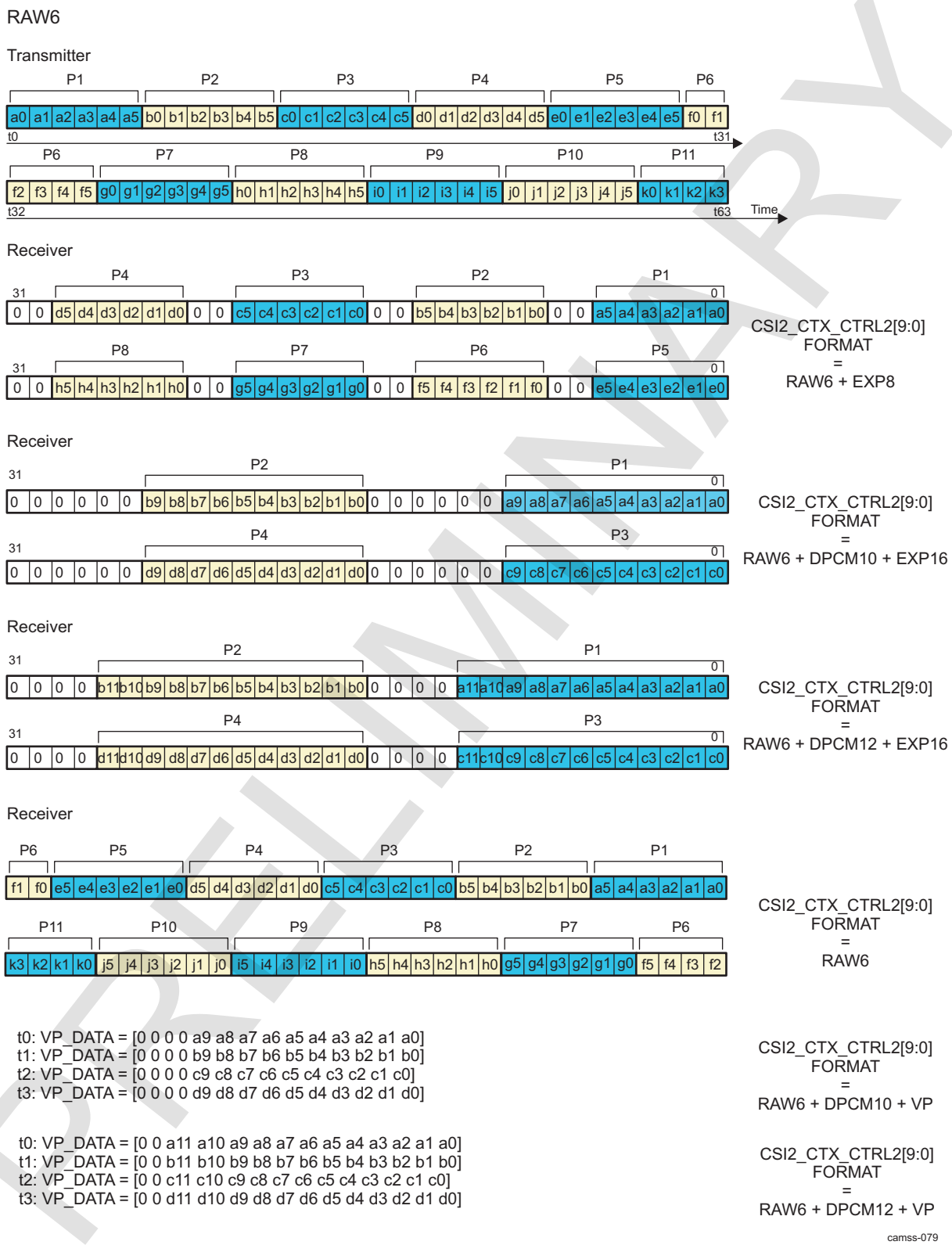
Figure 8-60. ISS CSI2 RAW6



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8.2.5.1.1.4.3.2 ISS CSI2 RAW7

RAW7 data can be output to memory with or without data expansion. The line length sent through the CSI2 physical layer is a multiple of 8 bits. Furthermore, the line length is a multiple of 7 × 8 bits to complete the pixel reconstruction correctly (the lowest common multiple of 8 and 7 is 56, so 7 × 8 bits). Figure 8-61 shows the storage format for RAW7 data. Set the CSI2_CTX_CTRL2_i[9:0] FORMAT bit field as follows:

- To 0x29 to select RAW7 mode
- To 0x69 for RAW7 + 8-bit expansion
- To 0x329 for RAW7 + DPCM decompression to 10-bit to video port
- To 0x229 for RAW7 + DPCM decompression to 10-bit expanded to 16-bit
- To 0x369 for RAW7 + DPCM decompression to 12-bit expanded to 16-bit
- To 0x3A9 for RAW7 + DPCM decompression to 12-bit to video port

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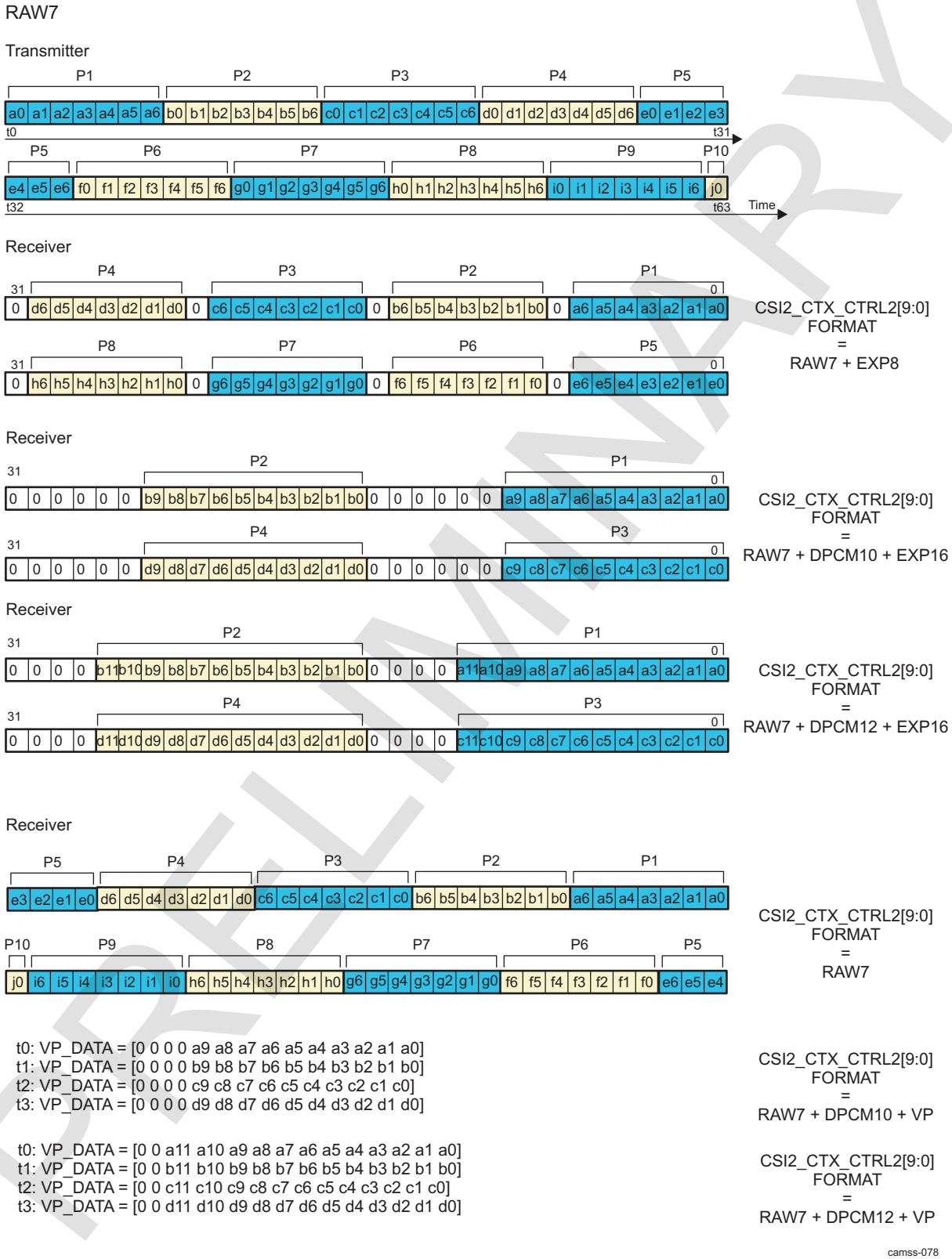
Figure 8-61. ISS CSI2 RAW7



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8.2.5.1.1.4.3.3 ISS CSI2 RAW8

RAW8 data can be output to memory with or without data expansion. The line length sent through the CSI2 physical layer is always a multiple of 8 bits. Figure 8-62 shows the storage format for RAW8 data. Set the CSI2_CTX_CTRL2_i[9:0] FORMAT bit field as follows:

- To 0x2A to select RAW8 mode
- To 0x12A for RAW8 to video port
- To 0x32A for RAW8 + DPCM decompression to 10-bit to video port
- To 0x2AA for RAW8 + DPCM decompression to 10-bit expanded to 16-bit
- To 0x36A for RAW8 + DPCM decompression to 12-bit expanded to 16-bit
- To 0x3AA for RAW8 + DPCM decompression to 12-bit to video port

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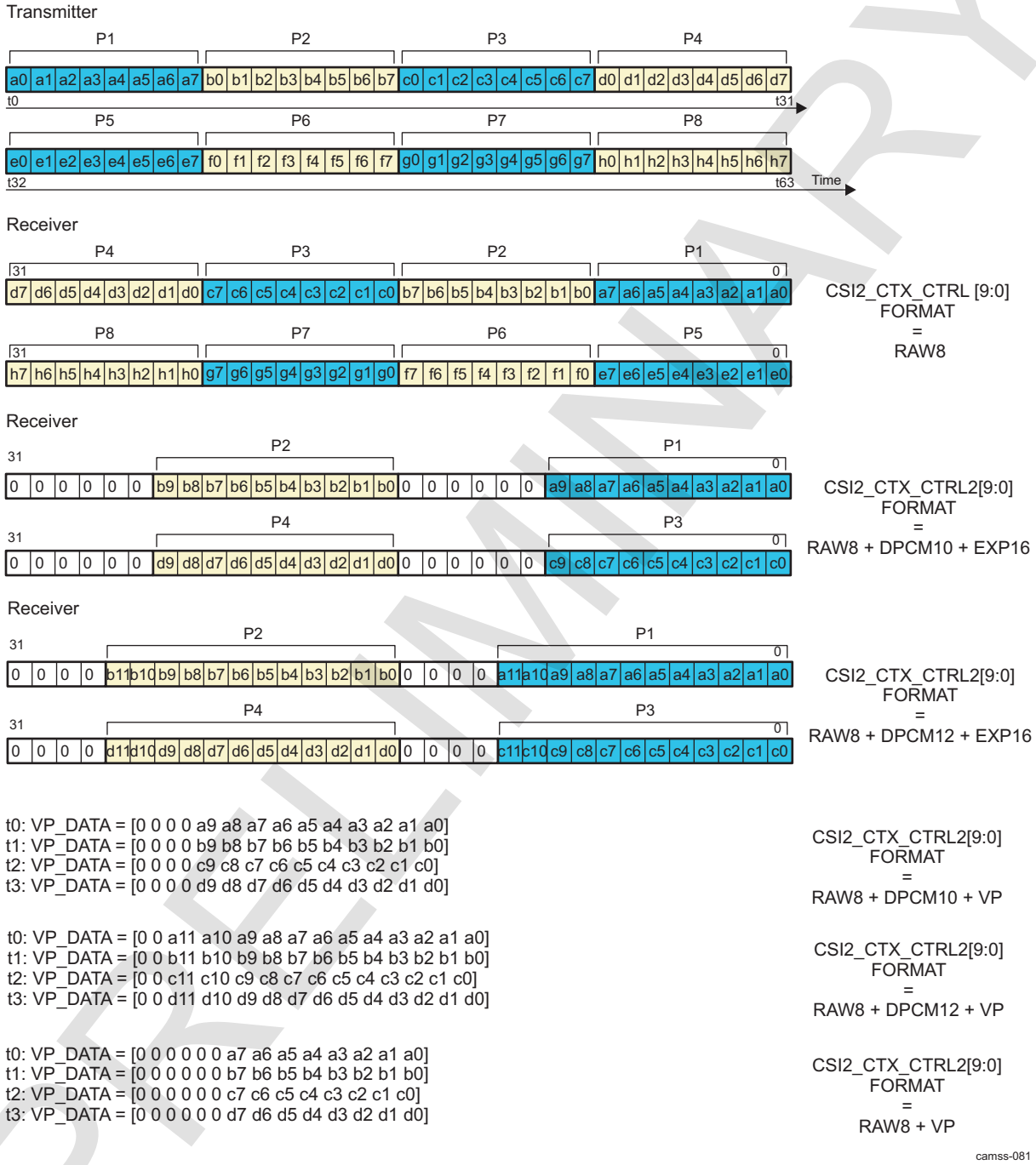
Figure 8-62. ISS CSI2 RAW8



8.2.5.1.1.4.3.4 ISS CSI2 RAW10

RAW10 data can be output memory in two formats: with or without data expansion. It can also be sent to

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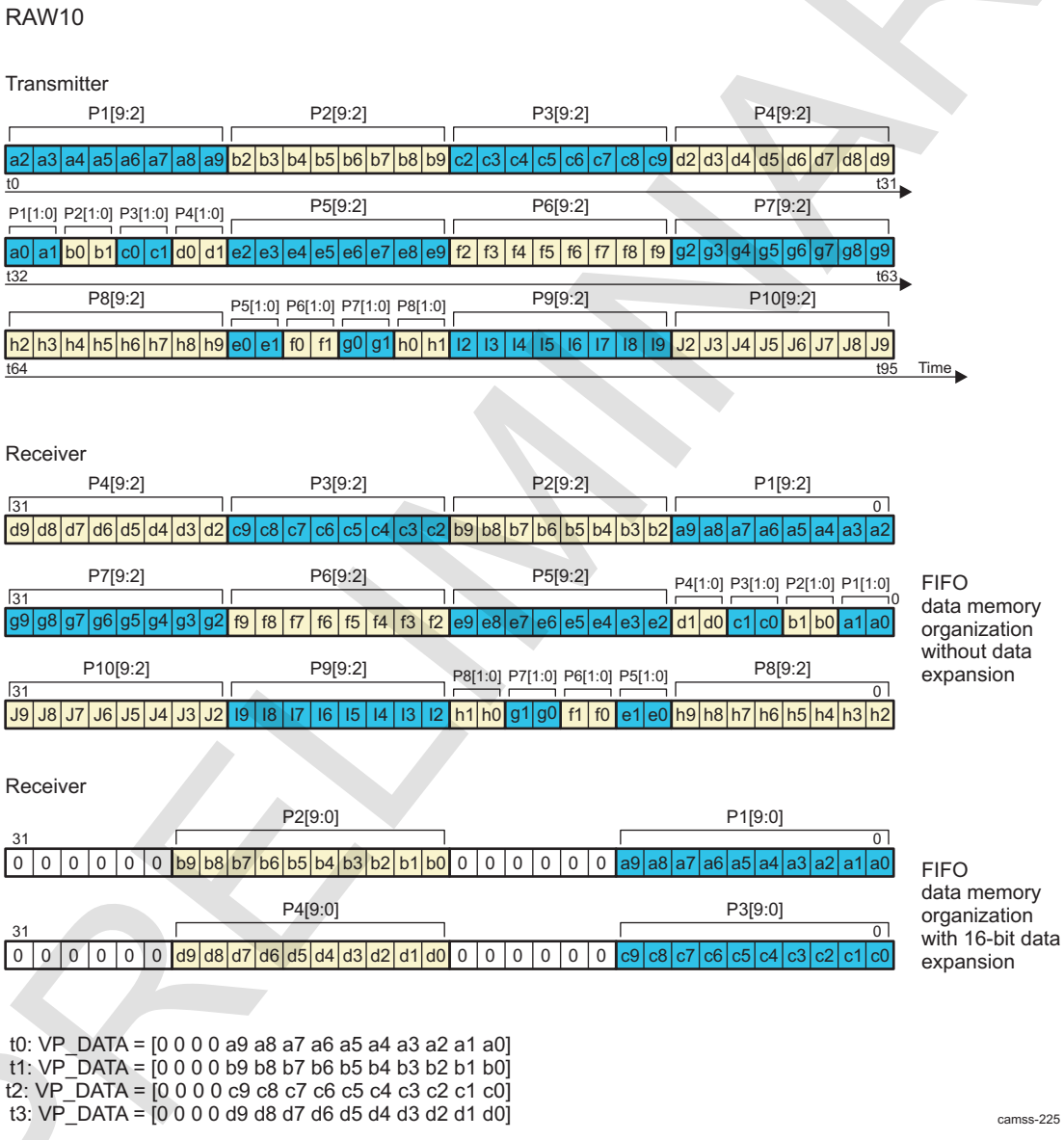
the video port. If data expansion is used, the 10-bit data are padded with 0s on a 16-bit word. The line length sent through the CSI2 physical layer is a multiple of 8 bits. Furthermore, the line length is a multiple of 5 × 8 bits to complete the pixel reconstruction correctly (the lowest common multiple of 8 and 10 is 40, so 5 × 8 bits). Figure 8-63 shows the storage format for RAW10 data. Set the CSI2_CTX_CTRL2_i[9:0] FORMAT bit field as follows:

- To 0x2B to select RAW10 mode
- To 0xAB for RAW10 + 16-bit expansion
- To 0x12F for RAW10 to video port

Figure 8-63. ISS CSI2 RAW10



8.2.5.1.1.4.3.5 ISS CSI2 RAW12

RAW12 data can be output to memory in two formats: with or without data expansion. It can also be sent to the video port. If data expansion is used, the 12-bit data are padded with 0s on a 16-bit word. The line length sent through the CSI2 physical layer is a multiple of 8 bits. Furthermore, the line length is a multiple of 3 × 8 bits to complete the pixel reconstruction correctly (the lowest common multiple of 8 and 12 is 24, so 3 × 8 bits). Figure 8-64 shows the storage format for RAW12 data. Set the CSI2_CTX_CTRL2_i[9:0] FORMAT bit field as follows:

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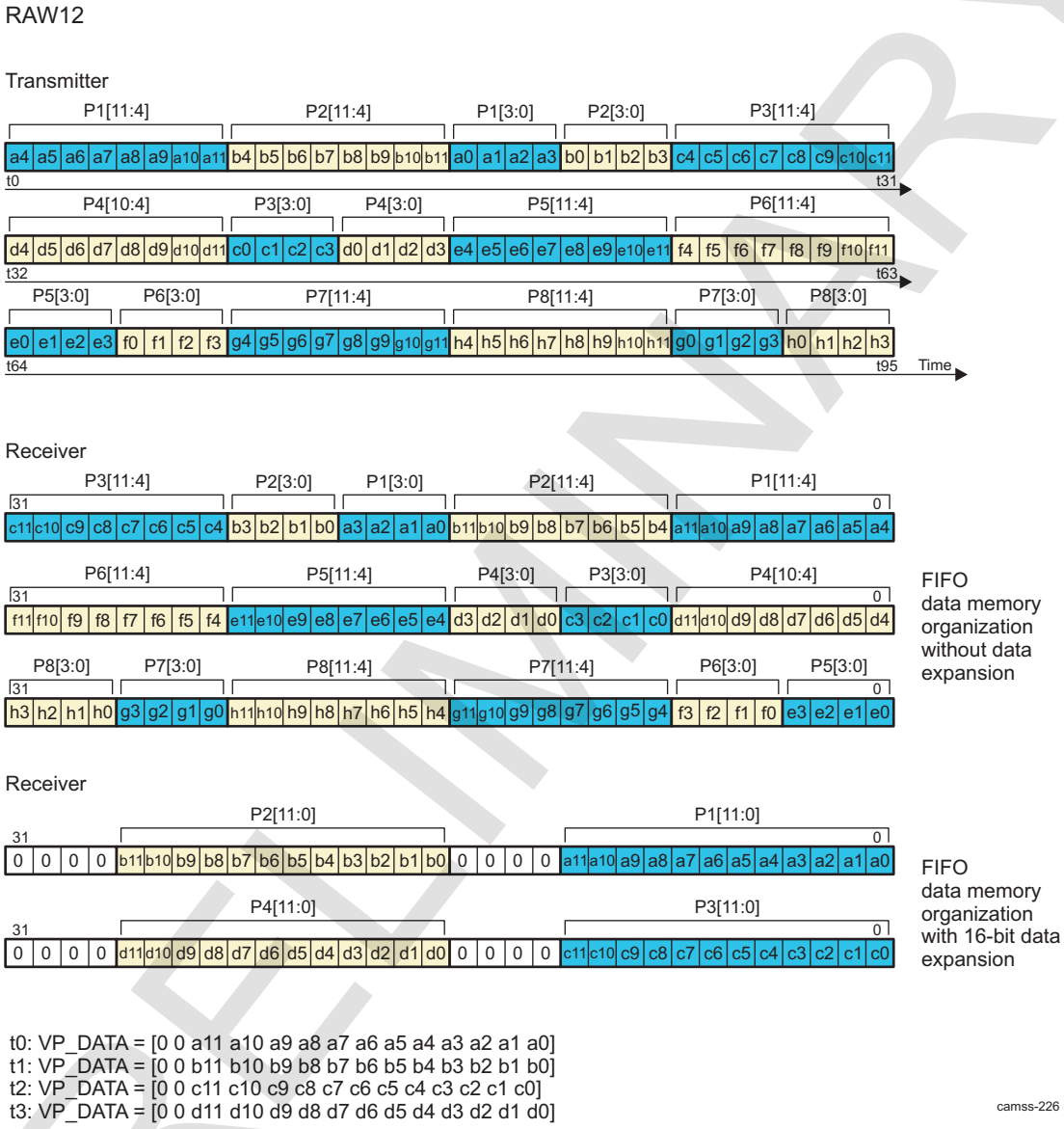
- To 0x2C to select RAW12 mode
- To 0xAC for RAW12 + 16-bit expansion
- To 0x12C for RAW12 to video port

Figure 8-64. ISS CSI2 RAW12



8.2.5.1.1.4.3.6 ISS CSI2 RAW14

RAW14 data can be output to memory in two formats: with or without data expansion. It can also be sent to the video port. If data expansion is used, the 14-bit data are padded with 0s on a 16-bit word. The line length sent through the CSI2 physical layer is a multiple of 8 bits. Furthermore, the line length is a multiple of 7 × 8 bits to complete the pixel reconstruction correctly (the lowest common multiple of 8 and 14 is 56, so 7 × 8 bits). Figure 8-65 shows the storage format for RAW14 data. Set the CSI2_CTX_CTRL2_i[9:0] FORMAT bit field as follows:

- To 0x2D to select RAW14 mode
- To 0xAD for RAW14 + 16-bit expansion
- To 0x12D for RAW12 to video port

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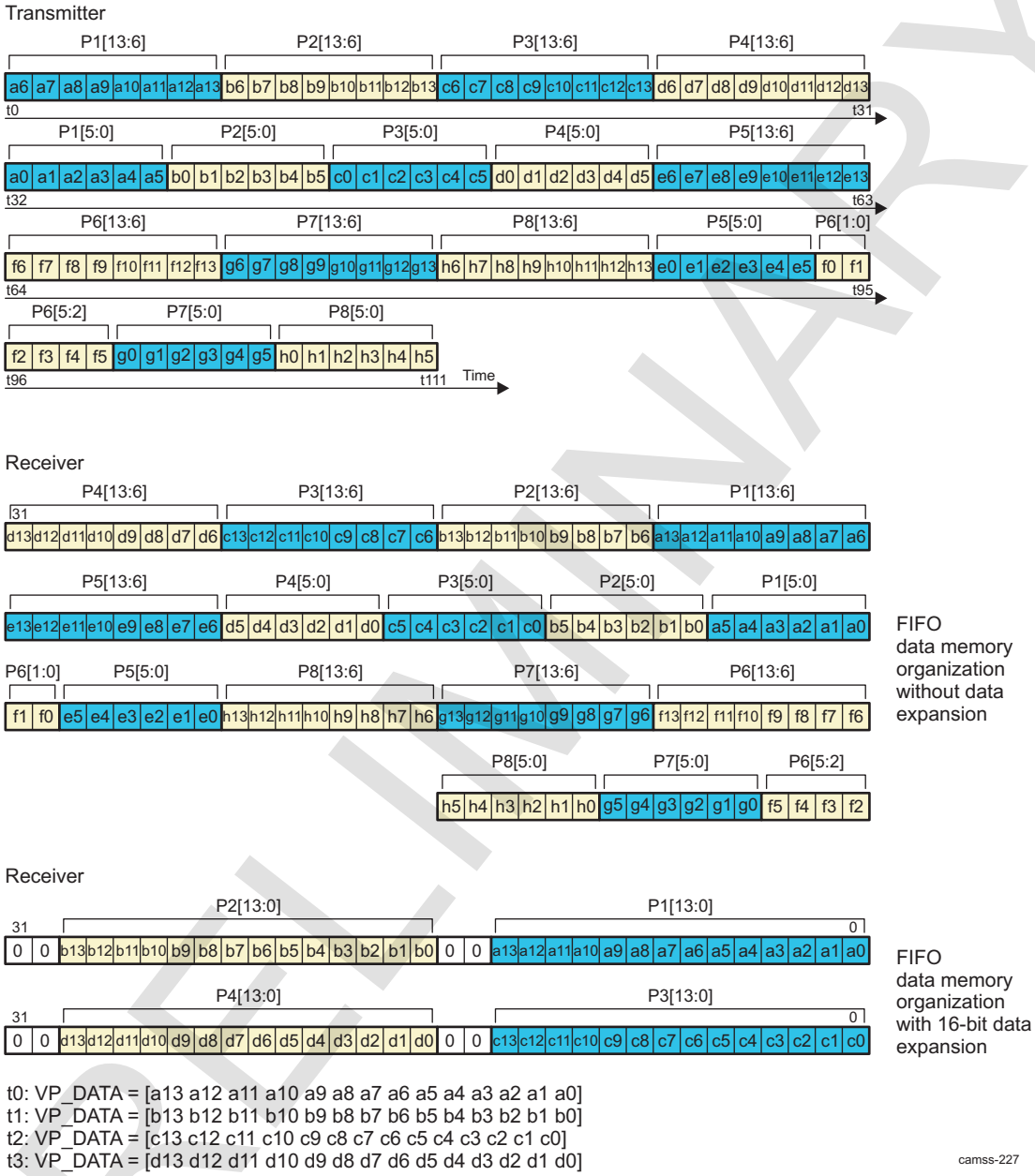
Figure 8-65. ISS CSI2 RAW14



8.2.5.1.1.4.4 ISS CSI2 JPEG8 Operating Modes

The size of a compressed stream can be known in advance. Figure 8-66 shows the format for storing JPEG8 data.

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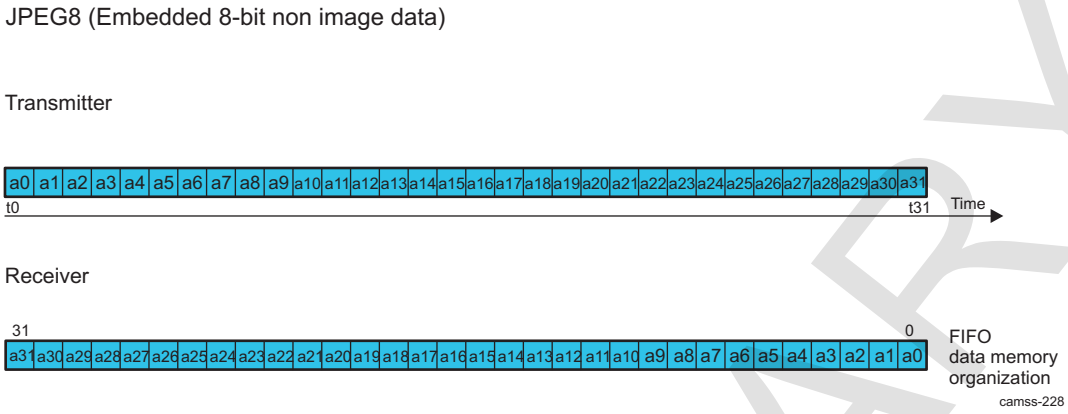
Figure 8-66. ISS CSI2 JPEG8

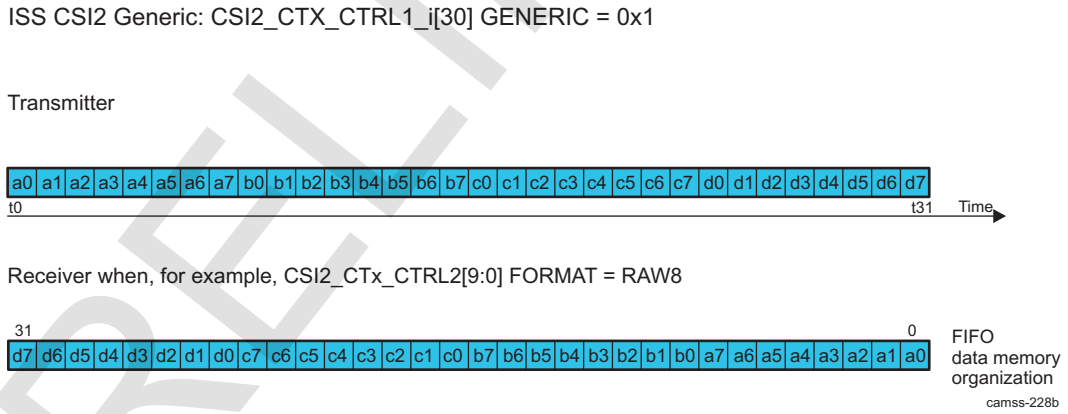


8.2.5.1.1.4.5 ISS CSI2 Generic Format

The CSI2 receiver supports a generic format to send data to memory and/or the video port. The generic mode is entered by setting the CSI2_CTX_CTRL1_i[30] GENERIC bit. The CSI2_CTX_CTRL2_i[9:0] FORMAT bit field defines how the data stream is decoded. When generic mode is enabled (GENERIC = 1), the MIPI data type code is ignored and data is decoded using the FORMAT bit. Whatever the MIPI data type code, it is ignored (the data stream is processed even if the FORMAT bit does not match the MIPI data type code.) When generic mode is not used (GENERIC = 0), the data stream is processed only when the MIPI data type code matches the FORMAT setting of the enabled context. If not matched, the data stream is not processed by the CSI2 engine. Only the virtual channel information is used to map a received data stream to a context. Software must ensure that a MIPI virtual channel used in generic mode is mapped only to a single context.

Figure 8-67 shows the ISS CSI2 generic format.

Figure 8-67. ISS CSI2 Generic Format



8.2.5.1.1.4.6 ISS CSI2 MIPI Format Supported Summary

Table 8-145 summarizes the CSI2 MIPI-supported formats and their output category. By setting the CSI2_CTX_CTRL2_i register format, the CSI2 outputs certain types of pixel packet data.

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Table 8-145. ISS CSI2 MIPI Format Supported by the Protocol Engine

MIPI			CSI2 Protocol Engine Support
Category	**Abbreviation**	**Register Setting Format Description**	**Configuration Value for CSI2_CTX_CTRL2_i[9:0] FORMAT**
Sync short packet data types(1)	Short packet sync code	Mandatory FSC	0x000
	Short packet sync code	Mandatory FEC	0x001
	Short packet sync code	Optional LSC	0x002
	Short packet sync code	Optional LEC	0x003
			0x004
			0x005
			0x006
			0x007
Generic short packet data types(1)	Short packet	32-bit without ECC is stored in a register with code value 0x008.	0x008
	Short packet	32-bit without ECC is stored in a register with code value 0x009.	0x009
	Short packet	32-bit without ECC is stored in a register with code value 0x00A.	0x00A
	Short packet	32-bit without ECC is stored in a register with code value 0x00B.	0x00B
	Short packet	32-bit without ECC is stored in a register with code value 0x00C.	0x00C
	Short packet	32-bit without ECC is stored in a register with code value 0x00D.	0x00D
	Short packet	32-bit without ECC is stored in a register with code value 0x00E.	0x00E
	Short packet	32-bit without ECC is stored in a register with code value 0x00.	0x00F
Generic Long packet data types(2)	Null	Discarded	0x010
	Blanking data	Discarded	0x011
	Embedded 8-bit nonimage data (for example, JPEG)	0x12: Embedded 8-bit nonimage data (for example, JPEG)	0x012
		Send to memory when FORMAT = 0	0x013
		Send to memory when FORMAT = 0	0x014
		Send to memory when FORMAT = 0	0x015
		Send to memory when FORMAT = 0	0x016
		Send to memory when FORMAT = 0	0x017
YUV data	YUV4:2:0 8-bit	YUV4:2:0 8-bit	0x018
	YUV4:2:0 10-bit	YUV4:2:0 10-bit	0x019
	YUV4:2:0 8-bit legacy	YUV4:2:0 8-bit legacy	0x01A
	Reserved	Send to memory when FORMAT = 0	0x01B
	YUV4:2:0 8-bit + CSPS	YUV4:2:0 8 bit + CSPS	0x01C
	YUV4:2:0 10-bit + CSPS	YUV4:2:0 10 bit + CSPS	0x01D
	YUV4:2:2 8-bit	YUV4:2:2 8-bit	0x01E
		YUV4:2:2 8-bit + VP	0x09E

(1) To understand ISS synchronization codes and short packets, see Section 8.2.5.3.3.3, *ISS CSI2 Short Packet*.
(2) To understand ISS synchronization codes and long packets, see Section 8.2.5.1.1.3.2, *ISS CSI2 Long Packet*.

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Table 8-145. ISS CSI2 MIPI Format Supported by the Protocol Engine (continued)

MIPI			CSI2 Protocol Engine Support
Category	**Abbreviation**	**Register Setting Format Description**	**Configuration Value for CSI2_CTX_CTRL2_i[9:0] FORMAT**
		YUV4:2:2 8-bit + VP16	0x0DE
	YUV4:2:2 10-bit	YUV4:2:2 10-bit	0x01F
RGB data	RGB444	RGB444 + EXP16	0x0A0
	RGB555	RGB555 + EXP16	0x0A1
	RGB565	RGB565	0x022
	RGB666	RGB666 + EXP32	0x0E3
		RGB666 + EXP32_24	0x033
	RGB888	RGB888	0x024
		RGB888 + EXP32	0x0E4
	Reserved	Send to memory when FORMAT = 0	0x025
	Reserved	Send to memory when FORMAT = 0	0x026
	Reserved	Send to memory when FORMAT = 0	0x027
RAW data	RAW6	RAW6	0x028
		RAW6 + EXP8	0x068
		RAW6 + DPCM10 + VP	0x0E8
		RAW6 + DPCM10 + EXP16	0x2A8
		RAW6 + DPCM12 + VP	0x368
		RAW6 + DPCM12 + EXP16	0x3A8
	RAW7	RAW7	0x029
		RAW7 + EXP8	0x069
		RAW7 + DPCM10 + EXP16	0x229
		RAW7 + DPCM10 + VP	0x329
		RAW7 + DPCM12 + EXP16	0x369
		RAW7 + DPCM12 + VP	0x3A9
	RAW8	RAW8	0x02A
		RAW8 + VP	0x12A
		RAW8 + DPCM10 + EXP16	0x2AA
		RAW8 + DPCM10 + VP	0x32A
		RAW8 + DPCM12 + EXP16	0x36A
		RAW8 + DPCM12 + VP	0x3AA
	RAW10	RAW10	0x02B
		RAW10 + EXP16	0x0AB
		RAW10 + VP	0x12F
	RAW12	RAW12	0x02C
		RAW12 + EXP16	0x0AC
		RAW12 + VP	0x12C
	RAW14	RAW14	0x02D
		RAW14 + EXP16	0x0AD
		RAW14 + VP	0x12D
	Reserved	Send to memory when FORMAT = 0	0x02E
	Reserved	Send to memory when FORMAT = 0	0x02F
User-defined byte-based data		USER_DEFINED_BYTE_DATA	0x040
		USER_DEFINED_BYTE_DATA + EXP8	0x080
		USER_DEFINED_BYTE_DATA + DPCM10 + EXP16	0x2C0

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Table 8-145. ISS CSI2 MIPI Format Supported by the Protocol Engine (continued)

MIPI			CSI2 Protocol Engine Support
Category	Abbreviation	Register Setting Format Description	Configuration Value for CSI2_CTX_CTRL2_i[9:0] FORMAT
		USER_DEFINED_BYTE_DATA + DPCM10 + VP	0x340
		USER_DEFINED_BYTE_DATA + DPCM12 + EXP16	0x1C0
		USER_DEFINED_BYTE_DATA + DPCM12 + VP	0x140
		USER_DEFINED_BYTE_DATA	0x041
		USER_DEFINED_BYTE_DATA + EXP8	0x081
		USER_DEFINED_BYTE_DATA + DPCM10 + EXP16	0x2C1
		USER_DEFINED_BYTE_DATA + DPCM10 + VP	0x341
		USER_DEFINED_BYTE_DATA + DPCM12 + EXP16	0x1C1
		USER_DEFINED_BYTE_DATA + DPCM12 + VP	0x141
		USER_DEFINED_BYTE_DATA	0x042
		USER_DEFINED_BYTE_DATA + EXP8	0x082
		USER_DEFINED_BYTE_DATA + DPCM10 + EXP16	0x2C2
		USER_DEFINED_BYTE_DATA + DPCM10 + VP	0x342
		USER_DEFINED_BYTE_DATA + DPCM12 + EXP16	0x1C2
		USER_DEFINED_BYTE_DATA + DPCM12 + VP	0x142
		USER_DEFINED_BYTE_DATA	0x043
		USER_DEFINED_BYTE_DATA + EXP8	0x083
		USER_DEFINED_BYTE_DATA + DPCM10 + EXP16	0x2C3
		USER_DEFINED_BYTE_DATA + DPCM10 + VP	0x343
		USER_DEFINED_BYTE_DATA + DPCM12 + EXP16	0x1C3
		USER_DEFINED_BYTE_DATA + DPCM12 + VP	0x143
		USER_DEFINED_BYTE_DATA	0x044
		USER_DEFINED_BYTE_DATA + EXP8	0x084
		USER_DEFINED_BYTE_DATA + DPCM10 + EXP16	0x2C4
		USER_DEFINED_BYTE_DATA + DPCM10 + VP	0x344
		USER_DEFINED_BYTE_DATA + DPCM12 + EXP16	0x1C4
		USER_DEFINED_BYTE_DATA + DPCM12 + VP	0x144
		USER_DEFINED_BYTE_DATA	0x045
		USER_DEFINED_BYTE_DATA + EXP8	0x085
		USER_DEFINED_BYTE_DATA + DPCM10 + EXP16	0x2C5
		USER_DEFINED_BYTE_DATA + DPCM10 + VP	0x345

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Table 8-145. ISS CSI2 MIPI Format Supported by the Protocol Engine (continued)

MIPI			CSI2 Protocol Engine Support
Category	**Abbreviation**	**Register Setting Format Description**	**Configuration Value for CSI2_CTX_CTRL2_i[9:0] FORMAT**
		USER_DEFINED_BYTE_DATA + DPCM12 + EXP16	0x1C5
		USER_DEFINED_BYTE_DATA + DPCM12 + VP	0x145
		USER_DEFINED_BYTE_DATA	0x046
		USER_DEFINED_BYTE_DATA + EXP8	0x086
		USER_DEFINED_BYTE_DATA + DPCM10 + EXP16	0x2C6
		USER_DEFINED_BYTE_DATA + DPCM10 + VP	0x346
		USER_DEFINED_BYTE_DATA + DPCM12 + EXP16	0x1C6
		USER_DEFINED_BYTE_DATA + DPCM12 + VP	0x146
		USER_DEFINED_BYTE_DATA	0x047
		USER_DEFINED_BYTE_DATA + EXP8	0x087
		USER_DEFINED_BYTE_DATA + DPCM10 + EXP16	0x2C7
		USER_DEFINED_BYTE_DATA + DPCM10 + VP	0x347
		USER_DEFINED_BYTE_DATA + DPCM12 + EXP16	0x1C7
		USER_DEFINED_BYTE_DATA + DPCM12 + VP	0x147
Reserved		Send to memory when FORMAT = 0	0x038
		Send to memory when FORMAT = 0	0x039
		Send to memory when FORMAT = 0	0x03A
		Send to memory when FORMAT = 0	0x03B
		Send to memory when FORMAT = 0	0x03C
		Send to memory when FORMAT = 0	0x03D
		Send to memory when FORMAT = 0	0x03E
		Send to memory when FORMAT = 0	0x03F

8.2.5.2 ISS CSI2 Integration

Figure 8-68 is an overview of the integration of the CSI2-A/CSI2-B interface in the device. The figure is the top-level block diagram of the CSI2-A/CSI2-B receiver. The CSI2-A/CSI2-B receiver receives the serial data coming from a CSI2 compatible image sensor, converts it to parallel data, extracts the logical channels, detects and extracts the synchronization codes, reformats the data, and outputs it through the video port or the ISS interconnect interface.

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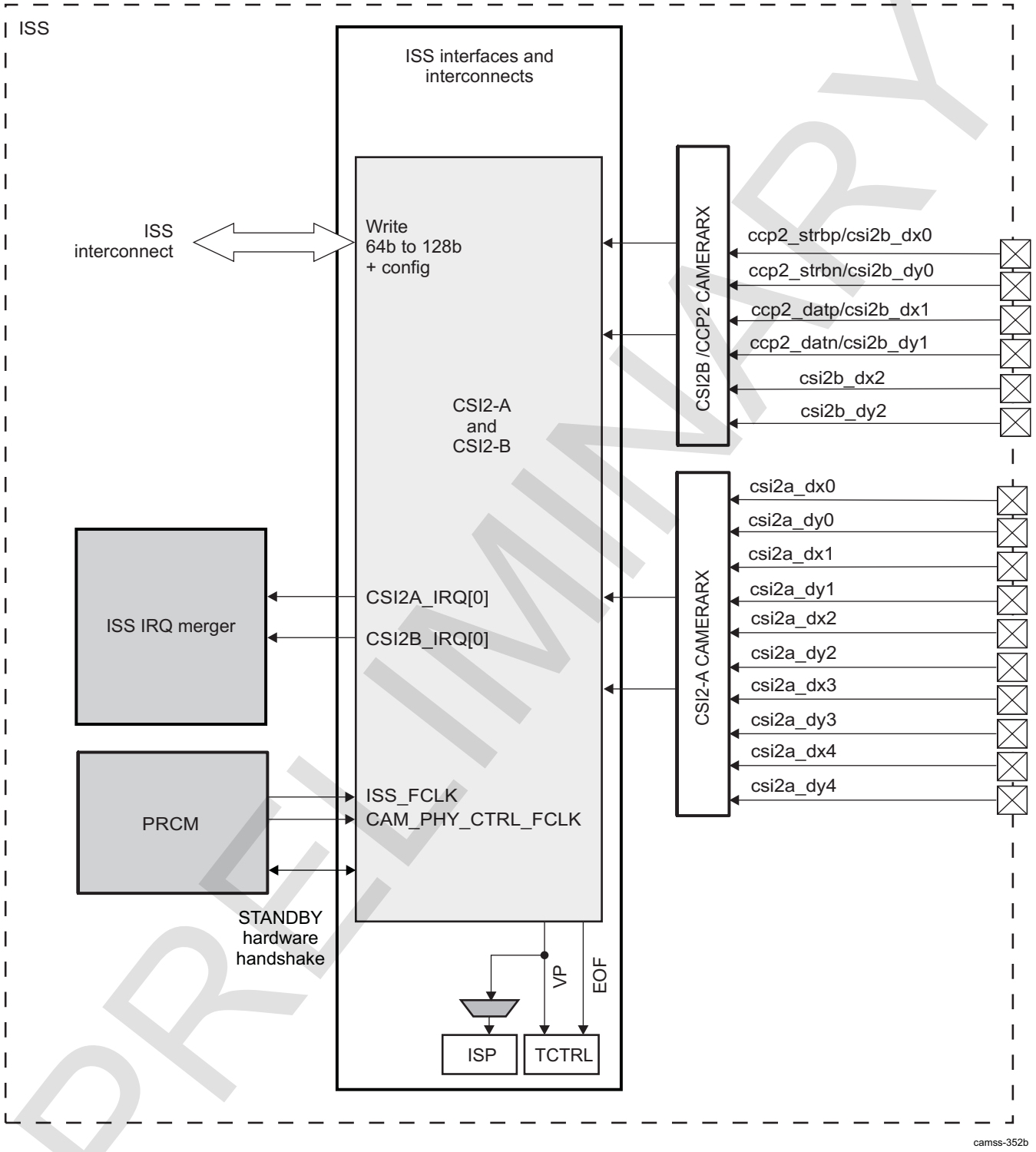
Figure 8-68. ISS CSI2-A/CSI2-B Integration



The CSI2-A/CSI2-B receiver can send data directly to system memory using the master port or send it to the camera ISP using the video port.

For power domain, clocks, reset, and hardware requests, see Section 8.1.2.4, *ISS Power Management*.

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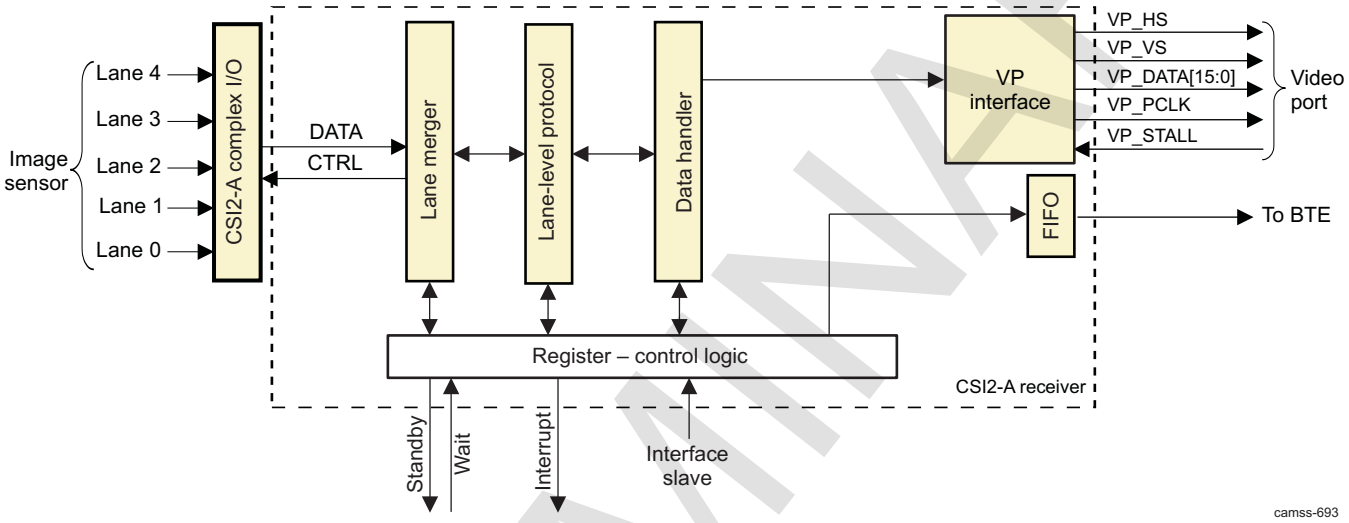
8.2.5.3 ISS CSI2 Functional Description

8.2.5.3.1 ISS CSI2 Overview

Figure 8-69 is the CSI2-A receiver block diagram (it assumes there are four CSI2 image sensor data lines). The only difference for CSI2-B is the number of lanes coming into the complex I/O. The CSI2 receiver receives the byte data coming from a CSI2 D-PHY receiver (up to four data pairs), converts it to byte stream, detects and corrects errors, extracts the virtual channel ID, detects and extracts the synchronization codes, reformats the data, and outputs it through the video port or the ISS interconnect interface. Data communication between CSI2 and ISP is done through the video port.

Figure 8-69. ISS CSI2-A Receiver Block Diagram



8.2.5.3.2 ISS CSI2 Features

The CSI2 receiver is a master on the L3 interconnect for storing data in memory and a slave on the level 4 (L4) interconnect for register access.

The main features of the CSI2 receiver are:

- Transfer pixels and data received by the CSI2 PHY to the system memory or video processor
- Unidirectional data link
- Supports up to four data-configurable links in addition to the clock signaling (minimum of one data link and maximum of four depending on the speed)
- Data merger for two, three, or four data lane configurations
- Error detection and correction by the protocol engine
- DMA engine integrated with dedicated FIFO
- 1D and 2D addressing modes
- Up to eight contexts to support eight dedicated configurations of virtual channel ID and data types
- Ping-pong mechanism for double-buffering
- JPEG support for unknown length transfer (no extraction of the thumbnail)
- Supports all primary and secondary MIPI-defined formats (RGB, RAW, and YUV)
- Storage in progressive mode for interlaced stream (using line numbering)
- Conversion to the RGB formats
- Decompressions of the RAW formats
- RAW frame transcoding, including DPCM and A-Law compression
- Fully configurable interface of the complex PHY I/O: position of the clock and data and order of ± differential signals for each pair

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8.2.5.3.3 ISS CSI2 Functional Description

8.2.5.3.3.1 ISS CSI2 Physical Layer Lane Configuration

The CSI2 serial interface is a unidirectional differential serial interface with data/clock for the physical layer.

The maximum CSI2 receiver data transfer capacity is 1000 Mbps per data lane.

Data-clock signaling consists of two to five differential signal pairs: from one to four data lanes and one clock lane:

- The data signal carries the bit-serial data. The CSI2 transmitter in the image sensor sends the data in-quadrature with the dual-data rate (DDR) clock in HS mode; otherwise, the clock is extracted from the received data in LS mode. Data is transmitted byte-wise, LSB first. The CSI2 complex I/O receives the data and sends the byte stream to the CSI2 receiver.
- The clock signal carries the DDR clock signal.

Each physical lane can be a data or clock lane with a restriction to the fourth line, which can only be data (see Section 8.2.3.1, *ISS CSI2 PHY Overview*). The clock/data lane must be configured before transmission to indicate the byte order, while merging the received bytes into a byte stream shows the reachable speed per data lane function of data lane numbers.

Lanes are configured through the CSI2_COMPLEXIO_CFG registers for CSI2-A and CSI2-B PHY, respectively. The CSI2_COMPLEXIO_CFG[2:0] CLOCK_POSITION bit field and the CSI2_COMPLEXIO_CFG[3] CLOCK_POL bit configure which lane transmits the clock and define its polarity. DATAl_POSITION and DATAl_POL configure the data lanes and their polarity, where l is the number of the data lane (l = 1 to 4). When the DATAl_POSITION field is set to 0, data lane l is not used.

CAUTION

Lane 4 (position 5) supports only data. The CLOCK_POSITION must not be set at position 5.

8.2.5.3.3.2 ISS CSI2 ECC and Checksum Generation

The CSI2 receiver includes an ECC in the packet header and a checksum in the packet footer for long-packet transmission. These two fields can be used to detect and/or correct errors in the received packet.

8.2.5.3.3.2.1 ISS CSI2 ECC

To detect and correct transmission errors of the header of short and long packets, an 8-bit ECC is included in the header of packets (short and long packet).

The ECC concerns all the fields for a short packet (data ID and short-packet data field) and the packet header for a long packet (data ID and word count). The ECC can only correct one error. Additional errors cannot be repaired, but they are flagged.

The CSI2 receiver ECC is compared against the CSI2 transmitter ECC embedded in the bitstream. If the ECC does not match, an interrupt is triggered to the host central processing unit (CPU).

For long and short packets, the correction is always done if there is only one error per packet header.

An ECC error with or without correction can be reported at two levels, depending on the type of packet. Table 8-146 describes the field in which events are logged. Logging cannot be disabled, but users can set the corresponding bit in the CSI2_IRQENABLE and CSI2_CTX_IRQENABLE_i registers to prevent event generation at a higher level.

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Table 8-146. ISS CSI2 ECC Event Logging

	Short Packet	Long Packet
With correction	Global CSI2_IRQSTATUS[12] ECC_CORRECTION_IRQ	Context CSI2_CTX_IRQSTATUS_i[8] ECC_CORRECTION_IRQ
Without correction	Global CSI2_IRQSTATUS[11] ECC_NO_CORRECTION_IRQ	Global CSI2_IRQSTATUS[11] ECC_NO_CORRECTION_IRQ

The ECC check can be disabled (short and long packet) by setting the CSI2_CTRL[2] ECC_EN bit to 0. Setting the bit to 1 enables the ECC check.

8.2.5.3.3.2.2 ISS CSI2 Checksum

To detect errors in transmission of the payload of long packets, a 16-bit CRC checksum is computed on the payload of the long packets in the transmitter. This CRC is stored in the packet footer. A CRC is also computed in the CSI2 receiver. If the checksums do not match, an interrupt is triggered to the host CPU.

CRC errors are logged in the CS_IRQ field of the corresponding context register, CSI2_CTX_IRQSTATUS_i. Logging cannot be disabled, but users can set the corresponding bit in the CSI2_CTX_IRQENABLE_i register to prevent event generation at a higher level.

The CRC can be disabled for a specific context by setting the CSI2_CTRL[5] CS_EN bit to 0. Seeting the bit to 1 enables the CRC.

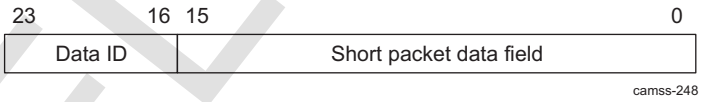
8.2.5.3.3.3 ISS CSI2 Short Packet

There are two types of short packets in the CSI2 receiver:

- Synchronization short packet: Used by the protocol engine to synchronize frame and line (data ID from 0x0 to 0x7)
- Generic short packet: User-dependent; not treated by the protocol engine (data ID from 0x8 to 0xF)

When a generic short packet is received by the CSI2 receiver, the ECC check is performed if it is enabled. Then, the short packet is written in the CSI2_SHORT_PACKET[23:0] SHORT_PACKET bit field. The ECC field is deleted from the short packet. Figure 8-70 shows the SHORT_PACKET bit field format.

Figure 8-70. ISS CSI2 SHORT_PACKET Bit Field Format



When a short packet is stored, an event is logged in the CSI2_IRQSTATUS[13] SHORT_PACKET_IRQ bit. Logging cannot be disabled, but users can set the corresponding bit in the CSI2_IRQENABLE register to prevent event generation at a higher level.

The application reads the CSI2_SHORT_PACKET register before the next short packet with a code from 0x8 to 0xF. There is a single register for capturing the generic short packet, because no data type in it is associated with context.

8.2.5.3.3.4 ISS CSI2 Virtual Channel and Context

The CSI2 protocol layer transports virtual channels. The virtual channels separate different data flows interleaved in the same data stream. Each virtual channel is identified by a unique channel identification number in the packet header. This channel identification number is encoded in the 2-bit code.

The CSI2 receiver monitors the channel identifier number and demultiplexes the interleaved data streams. The CSI2 receiver supports up to four concurrent virtual channels.

The CSI2 receiver supports eight contexts with their events to control the four possible virtual channels and the different data transmitted through them. A context is linked to a specific data type transported by a given virtual channel. The following bit fields permit configuration of a context:

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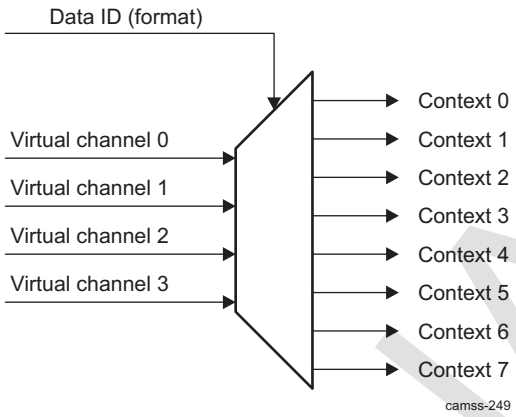
- CSI2_CTX_CTRL2_i[12:11] VIRTUAL_ID: Configures the virtual ID linked to the current context
- CSI2_CTX_CTRL2_i[9:0] FORMAT: Configures the data format linked to the current context

Figure 8-71 shows the relationships between virtual channels and contexts.

Figure 8-71. ISS CSI2 Virtual Channel to Context



Each context consists of eight registers: six registers to control the corresponding context and two to log and enable events from the context. All registers in a context can be modified at any time; however, modifications apply only from the start of the following frame.

A context can be enabled independently by setting the CSI2_CTX_CTRL1_i[0] CTX_EN bit to 1; setting this bit to 0 disables the corresponding context.

When acquiring frames on a context, users can write the number of frames to capture in the CSI2_CTX_CTRL1_i[15:8] COUNT bit field. Acceptable values are 0 to 255; 0 stands for infinite capture (no count). After each frame is acquired, the count value is decremented by 1. When the count value reaches 0, the CSI2_CTX_IRQSTATUS_i[6] FRAME_NUMBER_IRQ event is set and the CTX_EN bit is set to 0. To write a value in the COUNT bit field, the CSI2_CTX_CTRL1_i[4] COUNT_UNLOCK bit must be set to 1. If the value of the COUNT_UNLOCK bit is 0, a write in the COUNT bit field has no effect.

The CSI2_CTX_CTRL3_i[15:0] LINE_NUMBER bit field configures the generation of the CSI2_CTX_IRQSTATUS_i[7] LINE_NUMBER_IRQ event. The CSI2_CTX_CTRL1_i[1] LINE_MODULO bit configures how the LINE_NUMBER event is generated:

- 0: The event is generated one time by frame.
- 1: The event is generated modulo LINE_NUMBER (the event can be generated more than once in a frame).

During a frame capture, the CSI2_CTX_CTRL2_i[31:16] FRAME_NUMBER bit field shows the number that identifies the frame received.

8.2.5.3.3.5 ISS CSI2 DMA Engine

The CSI2 receiver integrates its own DMA engine with dedicated FIFO.

Global DMA configuration is common to the eight channels and is defined in the CSI2_CTRL register. Configuration of the ping-pong address and the offset between lines is specific for a given context; therefore, each context has its own DMA configuration registers.

The DMA engine supports:

- 1D addressing mode (no address line offset, CSI2_CTX_DAT_OFST_i = 0)
- 2D addressing mode (address line offset different than 0, CSI2_CTX_DAT_OFST_i = 0)

The burst size is defined in the CSI2_CTRL[6:5] BURST_SIZE bit field and the CSI2_CTRL[16]

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BURST_SIZE_EXPAND bit. The DMA uses the burst size or smaller sizes down to single open-core protocol (OCP) writes depending on the alignment at the end of lines. The DMA engine can handle burst requests. When the burst requests can be used, as soon as one burst of data is present in the FIFO, the DMA engine initiates a burst write. The burst size is defined in the CSI2_CTRL[6:5] BURST_SIZE bit field and the CSI2_CTRL[16] BURST_SIZE_EXPAND bit.

NOTE: Unless there are specific requirements, CSI2 (also applies to all other ISS initiators) must be configured to use only a burst size of 128 bytes and nonposted writes.

When single requests must be used, as soon as one element (the size depends on the data type and the post-processing: DPCM, EXT, etc.) is present in the FIFO, the DMA engine initiates a single write.

Interleave mode is dedicated by the CSI2 receiver only when the line numbers are received (short packets). The line number is used to calculate the start address of the line.

The DMA starts to write in memory using the CSI2_CTX_DAT_PING_ADDR_i[31:5] ADDR bit field for the first frame to be transferred, and then uses the CSI2_CTX_DAT_PONG_ADDR_i[31:5] ADDR bit field and the ping address alternately. Thus, the first frame uses the ping address, the second frame uses the pong address, the third frame uses the ping address, and so on.

The CSI2_CTX_CTRL1_i[3] PING_PONG status bit indicates whether the ping address (CSI2_CTX_DAT_PING_ADDR_i) or the pong address (CSI2_CTX_DAT_PONG_ADDR_i) was used to store the pixel data of the last frame. After reset or after a 0-to-1 edge transition in the CSI2_CTRL[0] IF_EN bit, the pixel data is written in the ping buffer and the CSI2_CTX_CTRL1_i[3] PING_PONG bit = PONG. When the number of FECs received equals the value programmed in the CSI2_CTX_CTRL1_i[23:16] FEC_NUMBER bit field, the pixel data are written in the pong buffer and CSI2_CTX_CTRL1_i[3] PING_PONG = PING. CSI2_CTX_CTRL1_i[3] PING_PONG toggles after the CSI2_CTX_CTRL1_i[23:16] FEC_NUMBER FEC sync code with the virtual channel ID defined is received in the CSI2_CTX_CTRL2_i[12:11] VIRTUAL_ID bit field.

The CSI2_CTX_CTRL1_i[23:16] FEC_NUMBER bit field must be set as follows:

- In progressive mode, set to 1.
- In interlaced mode, set to the number of interlaced frames to recreate a progressive image in the PING_PONG buffer.

8.2.5.3.3.5.1 ISS CSI2 Progressive Frame to Progressive Storage

After each line, a new start line address is computed, depending on the value of the CSI2_CTX_DAT_OFST_i[31:5] OFST bit field:

- If OFST = 0, the new line starts immediately after the last pixel (data are written contiguously in memory).
- Otherwise, the value of OFST sets the offset between the first pixel of the previous line and the first pixel of the current line in memory.

For the ping frame:

```
@Line0 = CSI2_CTX_DAT_PING_ADDR_i@Line1 = @Line0 + CSI2_CTX_DAT_OFST_i@Line2 = @Line1 +
CSI2_CTX_DAT_OFST_i
```

For the pong frame:

```
@Line0 = CSI2_CTX_DAT_PONG_ADDR_i@Line1 = @Line0 + CSI2_CTX_DAT_OFST_i@Line2 = @Line1 +
CSI2_CTX_DAT_OFST_i
```

8.2.5.3.3.5.2 ISS CSI2 Interlaced Frame to Progressive Storage

The mode is functional only when the line numbers are transmitted. It is automatically enabled without setting.

For the ping frame:

```
@LineX = CSI2_CTX_DAT_PING_ADDR_i + CSI2_CTX_DAT_OFST_i * Line_Number
```

For the pong frame:

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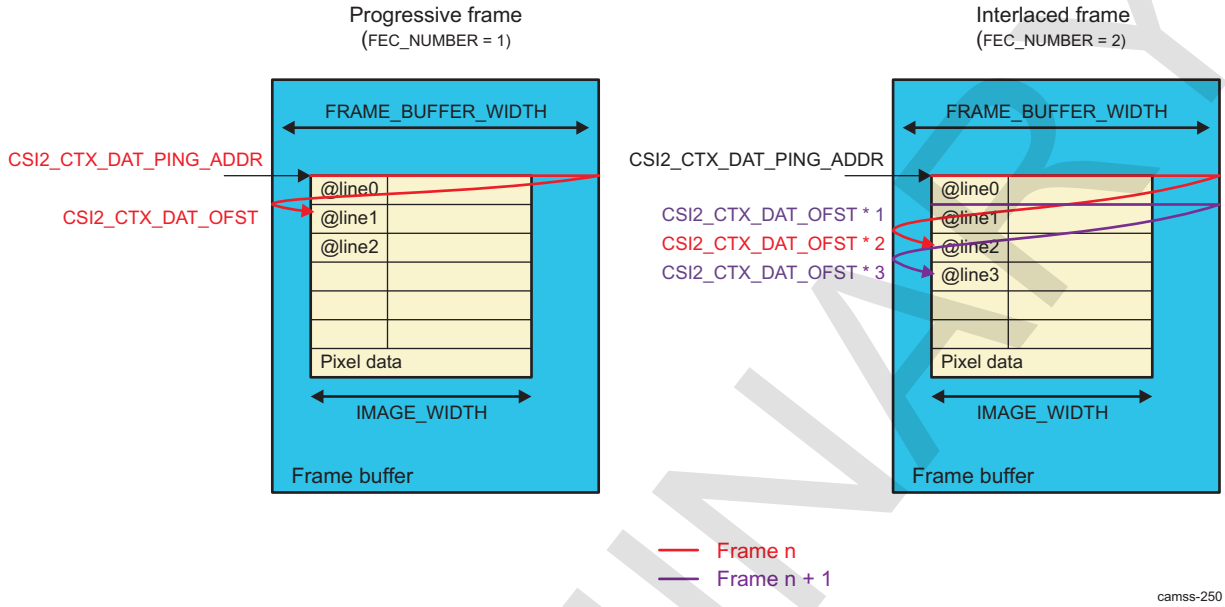
```
@LineX = CSI2_CTX_DAT_PONG_ADDR_i + CSI2_CTX_DAT_OFST_i * Line_Number
```

Figure 8-72 shows how data are stored in memory regarding the DMA configuration.

Figure 8-72. ISS CSI2 Pixel Data Destination Setting in Progressive and Interlaced Mode



The burst size is defined in the CSI2_CTRL[6:5] BURST_SIZE bit field for bursts up to 16 × 64 bits or the CSI2_CTRL[16] BURST_SIZE_EXPAND bit for 16 × 128-bit bursts. It can be changed only while the CSI2_CTRL[0] IF_EN bit is reset to 0. The recommended value is the CSI2_CTRL[16] BURST_SIZE_EXPAND bit set to 1, which defines a burst of 16 × 64 bits (the maximum value); otherwise, by default it is set to 8 × 64 bits. When the BURST_SIZE_EXPAND bit is set, the BURST_SIZE setting has no effect. The DMA uses nonposted writes by default. The CSI2_CTRL[13] NON_POSTED_WRITE bit must be set to 1 to match DMA default configuration. It can be changed only while the CSI2_CTRL[0] IF_EN bit is reset to 0.

8.2.5.3.3.6 ISS CSI2 Transcoding

Image transcoding is used mainly to reduce memory footprint and bandwidth when:

- The sensor does not support DPCM compression. In fact, A-Law and DPCM compressed pixels occupy only 6, 7, or 8 BPP of storage.
- Digital zoom is used
  - Data that is not going to be used by further processing does not need to the stored in system memory.
  - Pixels cannot be accessed from random locations in a DPCM-compressed frame. Transcoding avoids memory-to-memory processing of unused pixels.

Figure 8-73 shows the logical representation of the image transcoding operation.

- Data is extracted from the CSI2 stream by the protocol engine.
- It is DPCM decompressed if necessary. That is the case when the received stream is DPCM-compressed and transcoding has been enabled using the CSI2_CTX_CTRL1_i[27:24] TRANSCODE bit field.
- Data sent to the video port cannot be compressed: it is intended to be processed by the ISS ISP. Data sent to system memory can be optionally compressed.
- Internal data are aligned on MSB when they enter the cropping stage. For example:
  - 4 LSBs are 0s when RAW10 data are handled.
  - 2 LSBs are 0s when RAW12 data are handled.

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Figure 8-73. ISS CSI2 Frame Processing

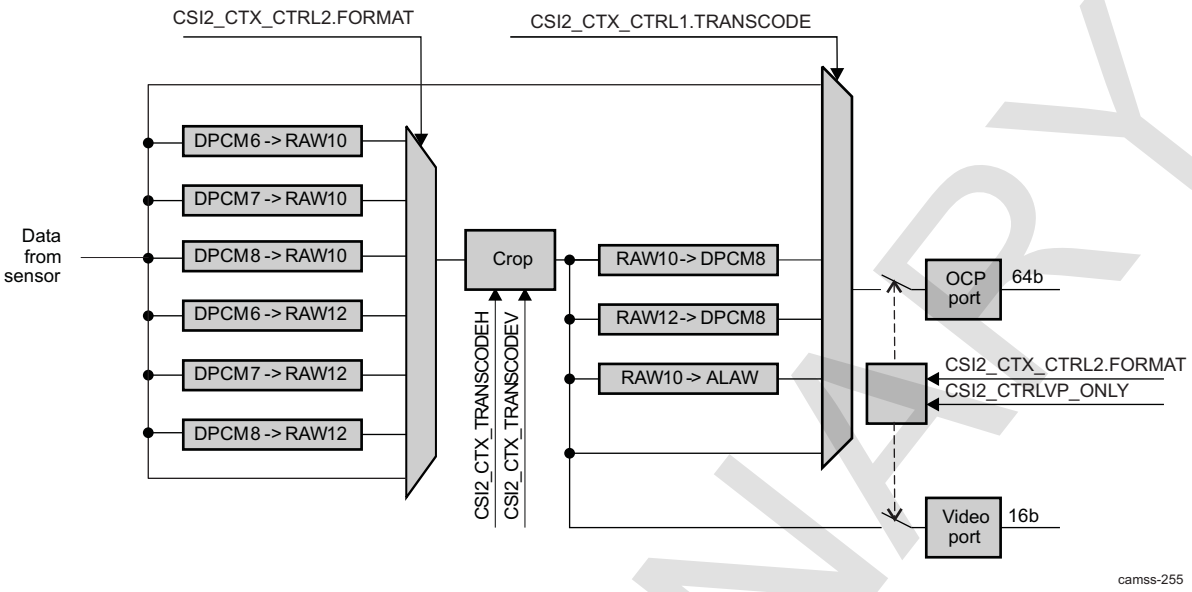

Table 8-147 shows the input format provided to the cropping engine for a given pixel format provided by the sensor. Formats not listed in the table are not supported for transcoding. The FORMAT and Corresponding Setting Value column corresponds to the value set in the CSI2_CTX_CTRL2_i[9:0] FORMAT register.

Table 8-147. ISS CSI2 Supported Transcoding Input Formats

CSI2_CTX_CTRL2_i[9:0] FORMAT and Corresponding Setting Value		Cropping Engine Input Format	DPCM Decomposition Enabled	Video Port Enabled
0x028	RAW6	RAW6		
0x058	RAW6 + EXP8			
0x029	RAW7	RAW7		
0x059	RAW7 + EXP8			
0x02A	RAW8	RAW8		
0x12A	RAW8 + VP			Yes
0x02B	RAW10	RAW10		
0x0AB	RAW10 + EXP16			
0x0E8	RAW6 + DPCM10 + VP		Yes	Yes
0x12F	RAW10 + VP			Yes
0x229	RAW7 + DPCM10 + EXP16		Yes	
0x2A8	RAW6 + DPCM10 + EXP16		Yes	
0x2AA	RAW8 + DPCM10 + EXP16		Yes	
0x329	RAW7 + DPCM10 + VP		Yes	Yes
0x32A	RAW8 + DPCM10 + VP		Yes	Yes
0x2Cn	USER_DEFINED_BYTE_DATA + DPCM10 + EXP16		Yes	
0x34n	USER_DEFINED_BYTE_DATA + DPCM10 + VP		Yes	Yes
0x02C	RAW12	RAW12		
0x0AC	RAW12 + EXP16			
0x12C	RAW12 + VP			Yes
0x35A	RAW8 DPCM12 + EXP16		Yes	
0x3AA	RAW8 DPCM12 + VP		Yes	Yes
0x1Cn	USER_DEFINED_BYTE_DATA + DPCM12 + EXP16		Yes	

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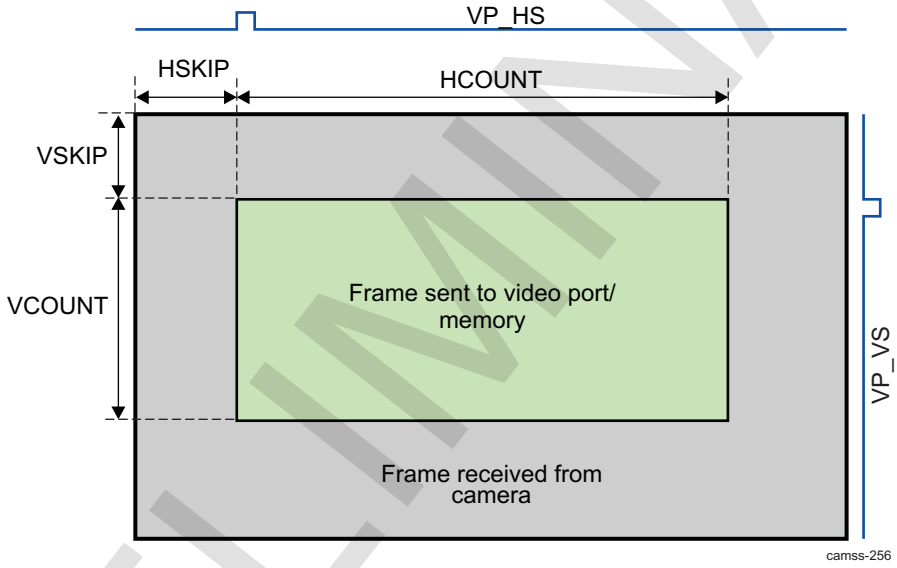
Table 8-147. ISS CSI2 Supported Transcoding Input Formats (continued)

CSI2_CTX_CTRL2_i[9:0] FORMAT and Corresponding Setting Value		Cropping Engine Input Format	DPCM Decomposition Enabled	Video Port Enabled
0x14n	USER_DEFINED_BYTE_DATA + DPCM12 + VP		Yes	Yes
0x3A8	RAW6 + DPCM12 + EXP16		Yes	
0x358	RAW6 + DPCM12 + VP		Yes	Yes
0x359	RAW7 + DPCM12 + EXP16		Yes	
0x3A9	RAW7 + DPCM12 + VP		Yes	Yes
0x02D	RAW14	RAW14		
0x0AD	RAW14 + EXP16			
0x12D	RAW14 + VP			Yes

Image cropping parameters are controlled by software. Figure 8-74 shows the cropping operation.

Figure 8-74. ISS CSI2 Frame Cropping



CAUTION

Hardware does not check for validity of the settings. The following rules must be respected:

- CSI2_CTX_TRANSCODEH_i[12:0] HSKIP + CSI2_CTX_TRANSCODEH_i[28:16] HCOUNT = image width
- CSI2_CTX_TRANSCODEV_i[12:0] VSKIP + CSI2_CTX_TRANSCODEV_i[28:16] VCOUNT = image height

Furthermore, the CSI2_CTX_TRANSCODEH_i[28:16] HCOUNT bit field must comply with the following alignment constraints; otherwise, undefined behavior occurs. Table 8-148 shows the transcode alignment constraints

Table 8-148. ISS CSI2 Transcode Alignment Constraints

CSI2_CTX_CTRLi[27:24] TRANSCODE Value	Transcode	HCOUNT Must Be Multiple of
0x0	Disabled	1
0x1	DPCM10 RAW8	1

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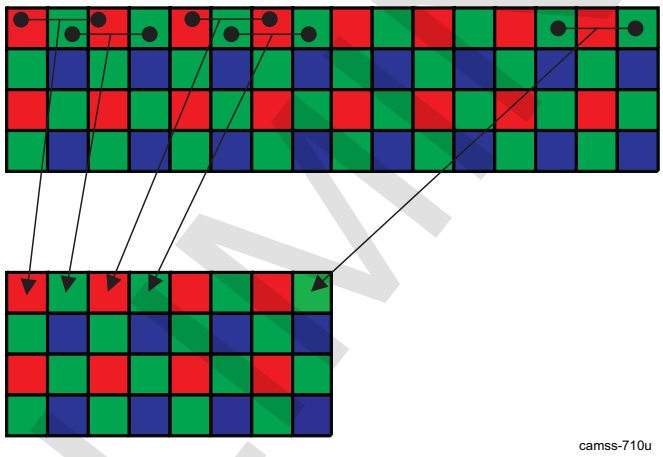
Table 8-148. ISS CSI2 Transcode Alignment Constraints (continued)

CSI2_CTX_CTRLi[27:24] TRANSCODE Value	Transcode	HCOUNT Must Be Multiple of
0x2	DPCM12 RAW8	1
0x3	ALAW10 RAW8	1
0x4	RAW8	1
0x5	RAW10 + EXP16	1
0x6	RAW10	4
0x7	RAW12 + EXP16	1
0x8	RAW12	2
0x9	RAW10 + EXP16	4

The CSI2_CTX_CTRL1_i[28] HSCALE configuration register enables horizontal downscaling of RAW data. It reduces the horizontal size and pixel clock by a factor of 2. The scaler uses a 2-tap horizontal filter operating on samples of the same color plane. The coefficients are: [1/2 ; 0 ; 1/2]

Figure 8-75 shows the scaler operation.

Figure 8-75. ISS CSI2 Horizontal Scaler



The scaler can send data to the video port or the interface port. When data goes to the video port, no additional alignment constraints apply. But when data goes to the interface port, HCOUNT/2 must comply with the constraints from Table 8-148 (for example, for RAW10, HCOUNT must be a multiple of 8).

Table 8-149 lists possible combinations of input and output formats supported by the transcoding engine. The Transcode column corresponds to the CSI2_CTX_CTRL1_i[27:24] TRANSCODE bit field of a context.

Table 8-149. ISS CSI2-Supported Transcoding Output Formats

Cropping Engine Output	Transcode		Supported	Cropping Engine Output	Transcode		Supported
RAW6	0	Disabled	Yes	RAW10	0	Disabled	Yes
	1	DPCM10 RAW8			1	DPCM10 RAW8	Yes
	2	DPCM12 RAW8			2	DPCM12 RAW8	
	3	ALAW10 RAW8			3	ALAW10 RAW8	Yes
	4	RAW8			4	RAW8	
	5	RAW10 + EXP16			5	RAW10 + EXP16	Yes
	6	RAW10			6	RAW10	Yes
	7	RAW12 + EXP16			7	RAW12 + EXP16	
	8	RAW12			8	RAW12	

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Table 8-149. ISS CSI2-Supported Transcoding Output Formats (continued)

Cropping Engine Output	Transcode		Supported	Cropping Engine Output	Transcode		Supported
	9	RAW14			9	RAW14	
RAW7	0	Disabled	Yes	RAW12	0	Disabled	Yes
	1	DPCM10 RAW8			1	DPCM10 RAW8	
	2	DPCM12 RAW8			2	DPCM12 RAW8	Yes
	3	ALAW10 RAW8			3	ALAW10 RAW8	
	4	RAW8			4	RAW8	
	5	RAW10 + EXP16			5	RAW10 + EXP16	
	6	RAW10			6	RAW10	
	7	RAW12 + EXP16			7	RAW12 + EXP16	Yes
	8	RAW12			8	RAW12	Yes
	9	RAW14			9	RAW14	
RAW8	0	Disabled	Yes	RAW14	0	Disabled	Yes
	1	DPCM10 RAW8			1	DPCM10 RAW8	
	2	DPCM12 RAW8			2	DPCM12 RAW8	
	3	ALAW10 RAW8			3	ALAW10 RAW8	
	4	RAW8	Yes		4	RAW8	
	5	RAW10 + EXP16			5	RAW10 + EXP16	
	6	RAW10			6	RAW10	
	7	RAW12 + EXP16			7	RAW12 + EXP16	
	8	RAW12			8	RAW12	
	9	RAW14			9	RAW14	Yes

RAW pixels are packed into 64-bit words sent to the OCP master port, as defined in:

- Section 8.2.5.1.1.4.3.3, *ISS CSI2 RAW8*
- Section 8.2.5.1.1.4.3.4, *ISS CSI2 RAW10*
- Section 8.2.5.1.1.4.3.5, *ISS CSI2 RAW12*
- Section 8.2.5.1.1.4.3.6, *ISS CSI2 RAW14*

For RAW10 and RAW12, software can choose among packed and nonpacked storage. A-Law and DPCM-compressed pixels are stored as RAW8 data: each RAW8 container holds a compressed data point.

Similarly, RAW data is sent over the video port, as described in:

- Section 8.2.5.1.1.4.3.3, *ISS CSI2 RAW8*
- Section 8.2.5.1.1.4.3.4, *ISS CSI2 RAW10*
- Section 8.2.5.1.1.4.3.5, *ISS CSI2 RAW12*
- Section 8.2.5.1.1.4.3.6, *ISS CSI2 RAW14*

Enabling of the OCP/video port is controlled by the CSI2_CTX_CTRL2_i[9:0] FORMAT bit field and the CSI2_CTRL[11] VP_ONLY_EN and CSI2_CTX_CTRL1_i[2] VPFORCE bits.

To enable transcoding, software configures the context normally and also configures the framing using the CSI2_CTX_TRANSCODEV_i and CSI2_CTX_TRANSCODEH_i registers. Software defines the after transcoding with the CSI2_CTX_CTRL1_i[27:24] TRANSCODE bit field.

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8.2.5.3.3.7 ISS CSI2 EndOfFrame and EndOfLine (EOF and EOL) Pulses

The CSI2 receiver generates two signals to qualify the last pixel of a frame and the last pixel of a line to the TCTRL. It is active during or after the adequate interface bridge transaction and becomes inactive before the first transaction of the next line. Software can enable/disable generation of those signals for each context using the CSI2_CTX_CTRL1_i[7] EOF_EN and CSI2_CTX_CTRL1_i[6] EOL_EN bits. When data is sent to both OCP and video ports, the EOL/EOF timing defined for the OCP port is used.

8.2.5.3.3.8 ISS CSI2 Data Decompression

The data compression technique used is DPCM and PCM.

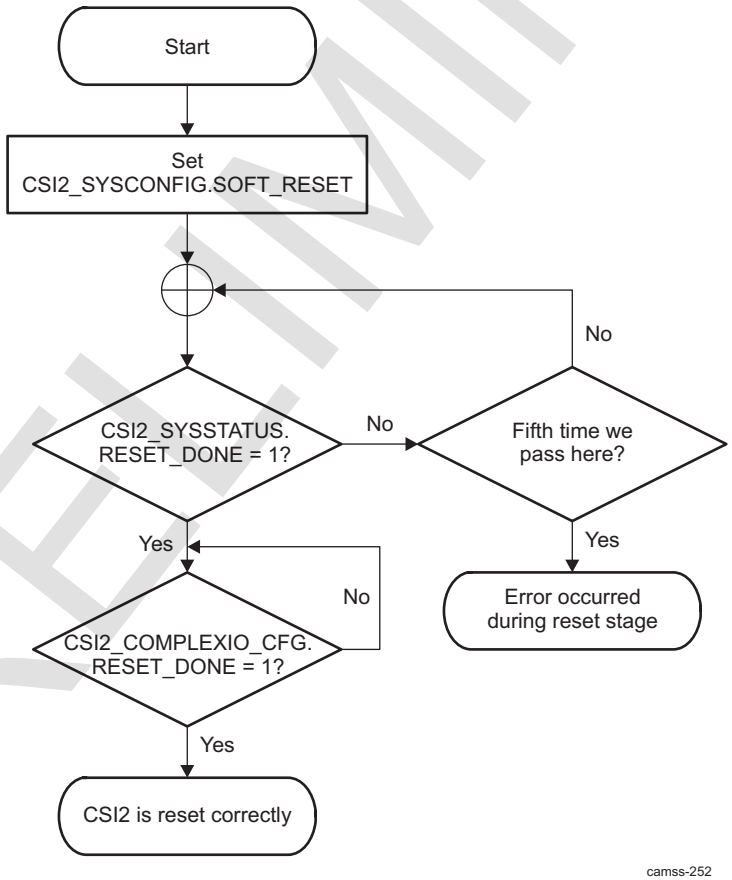
To select the DPCM decompression predictor for the CSI2 Interface, set the CSI2_CTX_CTRL2_i[10] DPCM_PRED bit to 1 for simple predictor or to 0 for advanced predictor.

8.2.5.4 ISS CSI2 Programming Model

8.2.5.4.1 ISS CSI2 Programming Reset Management

The CSI2 receiver accepts a general software reset, propagated throughout the hierarchy. This reset can be done to initialize the CSI2 receiver and the complex I/O (A or B) and has the same effect as a hardware reset. Figure 8-76 shows how to reset CSI2 globally.

Figure 8-76. ISS CSI2 Receiver Global Reset Flow Chart



NOTE: Before setting the software reset bit to 1 in the CSI2_SYSCONFIG register, the user must have access to a CSI2 receiver register.

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NOTE: The CSI2_COMPLEXIO_CFG[29] RESET_DONE bit is set to 1 only after the initialization of the CSI2 receiver, CSI2 complex I/O, and external camera completes.

8.2.5.4.2 ISS CSI2 Programming Enable Video/Picture Acquisition

Before using the receiver, a CSIPHY initialization in CSI2 mode must be made for CSI2-A CAMERARX, which is associated with the CSI2 receiver. See Section 8.2.3.2.2, *ISS CSI2 PHY and Link Initialization Sequence.* To start a video/picture acquisition, perform the steps listed in Table 8-150.

Table 8-150. ISS CSI2 Global Initialization

Step	Register/Bit Field/Programming Model	Value
Reset the CSI2 receiver.	See Section 8.2.5.4.1, *Reset Management.*	
Configure the module power management. The module tries to enter smart-standby mode during the vertical blanking period. The CSI2_SYSCONFIG[0] AUTO_IDLE bit keeps its reset value; by default, an automatic port clock gating strategy is applied based on port interface activity.	CSI2_SYSCONFIG[13:12] MSTANDBY_MODE	0x2
Configure the interrupt generation as required. To enable context and/or complex I/O event reporting, enable the corresponding bit field in the CSI2_IRQENABLE register. If the enable bit is at 0, logging is still effective if an event occurs, but is not reported to a higher level.	CSI2_IRQSTATUS and CSI2_IRQENABLE	
Configure the complex I/O interrupt generation as required. If the enable bit is at 0, logging is still effective if an event occurs, but is not reported to a higher level.	CSI2_COMPLEXIO_IRQSTATUS and CSI2_COMPLEXIO_IRQENABLE)	
Start complex I/O: Set the CSI2_COMPLEXIO_CFG[28:27] PWR_CMD bit field to 0x1 to pass the complex I/O to the ON state, and then check that the state status reaches the ON state (CSI2_COMPLEXIO_CFG[26:25] PWR_STATUS = 0x1) (for complex I/O A).	CSI2_COMPLEXIO_CFG[28:27] PWR_CMD	0x1
Configure the complex I/O: • The complex I/O is fully functional with CSI2_COMPLEX_CFG set at its reset value. • CSI2_COMPLEX_CFG must be changed according to the data rate being used.	CSI2_COMPLEXIO_CFG	
Set RXMODE and STOPSTATE FSM to RXMODE state. Users can also configure the delay for the FSM to return from RXMODE to NORXMODE when all lines reach STOPSTATE.	CSI2_TIMING[15] FORCE_RX_MODE_IO1	0x1
Activate ECC correction and error detection on short packets and packet headers. The ECC check corrects the packet if there is one error and generates an error if there is more than one error (unrecoverable error).	CSI2_CTRL[2] ECC_EN	0x1
Start the CSI2 receiver.	CSI2_CTRL[0] IF_EN	0x1
Configure the different contexts to be used.		
Link the context to a virtual channel and a data type.	See Section 8.2.5.4.6, *Linking a Context to a Virtual Channel and a Data Type.*	
Set the FEC_NUMBER bit field to 0x1 for a progressive video and to 0x2 for an interlaced video. For more information, see Section 8.2.5.3.3.5, *DMA Engine.*	CSI2_CTX_CTRL1_i[26:23] FEC_NUMBER	0x1 or 0x2
Capture an infinite number of frames (until the interface or the context is disabled).	CSI2_CTX_CTRL1_i[15:8] COUNT and CSI2_CTX_CTRL1_i[4] COUNT_UNLOCK	0x0

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Table 8-150. ISS CSI2 Global Initialization (continued)

Step	Register/Bit Field/Programming Model	Value
Enable the CRC checksum on long packet payload. This allows detection of errors, but cannot correct errors like the ECC for header and short packet. On error detection, an event is triggered (the CSI2_CTX_IRQSTATUS_i[5] CS_IRQ bit).	CSI2_CTX_CTRL1_i[5] CS_EN	
Configure the DMA engine for the current channel: Configure the ping and pong addresses.	CSI2_CTX_DAT_PING_ADDR_i[31:5] ADDR and CSI2_CTX_DAT_PING_ADDR_i[31:5] ADDR	
Set the CSI2_CTx_DAT_OFST_i[15:5] OFST bit field to 0x0 so consecutive lines are stored consecutively in memory (image width and frame-buffer width are equal).	CSI2_CTX_DAT_OFST_i[15:5] OFST	
Keep the ALPHA setting at its reset value (0x0) for RGB padding.	CSI2_CTX_CTRL3_i[29:16] ALPHA	
Enable the contexts.	CSI2_CTX_CTRL1_i[0] CTX_EN	0x1

8.2.5.4.3 ISS CSI2 Programming Disable Video/Picture Acquisition

There are two ways to end picture acquisition:

- Disable the corresponding context by setting the CSI2_CTX_CTRL1_i[0] CTX_EN bit to 0. This stops the acquisition for the current context. Other enabled contexts are still capturing frames and writing them in memory.
- Disable the CSI2 receiver interface by setting the CSI2_CTRL[0] IF_EN bit to 0. This can have an immediate effect if the CSI2_CTRL[3] FRAME bit is set to 0, or it can be effective after all the enabled contexts receive the FEC if the CSI2_CTRL[3] FRAME bit is set to 1.

8.2.5.4.4 ISS CSI2 Programming Capture a Finite Number of Frames

The CSI2 receiver can be configured to capture a finite number of frames. To configure the CSI2 receiver in this mode, perform the steps listed in Table 8-151.

Table 8-151. ISS CSI2 Capture a Finite Number of Frames

Step	Bit Field	Value
Enable a write to the COUNT bit field.	CSI2_CTX_CTRL1_i[4] COUNT_UNLOCK	0x1
Set the bit field to the number of frames the CSI2 receiver must capture.	CSI2_CTX_CTRL1_i[15:8] COUNT	Valid values are 0 to 255; 0 is infinite capture and 1 to 255 defines the number of frames to capture.
Disable a write to the COUNT bit field.	CSI2_CTX_CTRL1_i[4] COUNT_UNLOCK	0x0

During frame capture, the COUNT bit field is decremented by 1 at each frame capture. Software reads the COUNT bit field to know how many frames must still be captured.

The COUNT bit can be updated during capture if the COUNT_UNLOCK bit is set to 1.

8.2.5.4.5 ISS CSI2 Programming a Periodic Event During Frame Acquisition

The CSI2 receiver can generate a periodic event. This line number is defined in the CSI2_CTX_CTRL3_i[15:0] LINE_NUMBER bit field. The event can be generated once or multiple times per frame, depending on the value of the CSI2_CTX_CTRL1_i[1] LINE_MODULO bit:

- If the LINE_MODULO bit = 0, the event is generated when the line number corresponding to the LINE_NUMBER bit field is received.
- If the LINE_MODULO bit = 1, the event is generated when the line number received corresponds to a multiple of the LINE_NUMBER value (LINE_NUMBER is used as a modulo).

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8.2.5.4.6 ISS CSI2 Programming a Context to a Virtual Channel and a Data Type

The CSI2 receiver supports eight contexts and the CSI2 protocol defines four virtual channels. Therefore, a CSI2 receiver context can be associated with a virtual channel and a data type. Virtual channels are defined by a 2-bit field. Valid data types for the CSI2 receiver with their associated values are described in the CSI2_CTX_CTRL2_i[9:0] FORMAT bit field.

For each context, a CSI2_CTX_CTRL2_i register defines with which channel and data type the context is associated:

- The VIRTUAL_ID bit field defines the associated virtual ID transported by the CSI2 protocol from the camera sensor.
- The FORMAT bit field defines the associated data type. The data type is a combination of the data type transported by the CSI2 protocol and the type of storage in memory. A given data type (RGB888) can be stored in memory in different ways (RGB888 or RGB888 + EXP32). Therefore, the FORMAT bit field also defines how DMA stores data in memory.

For example, for the current context to capture a frame from virtual channel 2 and data type RAW12 with data expansion (RAW12 + EXP16), write the value 0x10AC (0x2 11 + 0xAC) in the 16 LSBs of the CSI2_CTX_CTRL2_i register.

8.2.5.4.7 ISS CSI2 Programming Progressive and Interleaved Frame Configuration

The CSI2 receiver can treat progressive and interlaced frames. There is no progressive or interleaved mode, but the CSI2_CTX_CTRL1_i[23:16] FEC_NUMBER bit field controls the number of FECs before swapping to the other (ping or pong) buffer. Therefore, two modes are possible:

- FEC_NUMBER = 1: This is equivalent to progressive mode. After a FEC on the context, the current buffer is switched (ping to pong or pong to ping). The image in the memory buffer consists of one transmitted frame.
- FEC_NUMBER 1: The current buffer is switched (ping to pong or pong to ping) after the FEC_NUMBER FEC is received for the context. The image in the memory buffer consists of the FEC_NUMBER transmitted frame.

For more information about how data is stored in memory through the DMA, see Section 8.2.5.3.3.5, *DMA Engine*.

NOTE: If FEC_NUMBER 1, the camera sensor must send the line number information with the current line. Otherwise, the CSI2 receiver cannot calculate each line address.

8.2.5.4.8 ISS CSI2 Programming Progressive and Interleaved Frame Configuration

Table 8-152 lists the procedure to enable debug mode.

Table 8-152. ISS CSI2 Enable Debug Mode

Step	Bit	Value
Enable debug mode.	CSI2_CTRL[7] DBG_EN	0x1

- During debug mode the input does not come from the CSI2 receiver interface but from the CSI2_DBG_H and CSI2_DBG_P registers. The full CSI2 receiver function can be debugged in debug mode. Full 32-bit values must always be written to the CSI2_DBG_H register. The CSI2_CTRL[0] IF_EN bit has no affect during debug mode. To reset the FIFO in case of overflow, the CSI2_CTRL[7] DBG_EN bit must be reset to 0, and the interface must be enabled by setting the CSI2_CTRL[0] IF_EN bit to 0x1.
- The CSI2_DBG_H register is used to provide short packet and long packet headers.
- The CSI2_DBG_P register is used to provide long packet payload.

The following examples apply to the CSI2_DBG_H register:

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- The sync codes for virtual channel 0 are written as CSI2_DBG_H = 0xFF00 0000 or 0xFF00 0001, or 0xFF00 0002 or 0xFF00 0003. To send the RAW12 pixels 0x673, 0x452, 0x01d, 0xefc, 0xab0, 0x891, 0x326, 0x547, write CSI2_DBG_H = 0x0123 4567, followed by CSI2_DBG_H = 0x89abcdef, and CSI2_DBG_H = 0x7654 3210.

8.2.5.5 ISS CSI2 Register Manual

8.2.5.5.1 ISS CSI2 Instance Summary

Table 8-153 summarizes the CSI2 instance.

Table 8-153. ISS CSI2 Instance Summary

Module Name	L3 Base Address	Size
ISS_CSI2_A_REGS1	0x5200 1000	368 bytes
ISS_CSI2_A_REGS2	0x5200 11C0	64 bytes
ISS_CSI2_B_REGS1	0x5200 1400	368 bytes
ISS_CSI2_B_REGS2	0x5200 15C0	64 bytes

8.2.5.5.2 ISS CSI2 REGS1 Registers

8.2.5.5.2.1 ISS CSI2 REGS1 Register Summary

Table 8-154 summarizes the CSI2 REGS1 registers.

Table 8-154. ISS CSI2 REGS1 Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	ISS_CSI2_A_REGS 1 Base Address	ISS_CSI2_B_REGS 1 Base Address
CSI2_REVISION	R	32	0x0000 0000	0x5200 1000	0x5200 1400
CSI2_SYSCONFIG	RW	32	0x0000 0010	0x5200 1010	0x5200 1410
CSI2_SYSSTATUS	R	32	0x0000 0014	0x5200 1014	0x5200 1414
CSI2_IRQSTATUS	RW	32	0x0000 0018	0x5200 1018	0x5200 1418
CSI2_IRQENABLE	RW	32	0x0000 001C	0x5200 101C	0x5200 141C
CSI2_CTRL	RW	32	0x0000 0040	0x5200 1040	0x5200 1440
CSI2_DBG_H	W	32	0x0000 0044	0x5200 1044	0x5200 1444
RESERVED	R	32	0x0000 0048	0x5200 1048	0x5200 1448
RESERVED	RW	32	0x0000 004C	0x5200 104C	0x5200 144C
CSI2_COMPLEXIO_CFG	RW	32	0x0000 0050	0x5200 1050	0x5200 1450
CSI2_COMPLEXIO_IRQSTATUS	RW	32	0x0000 0054	0x5200 1054	0x5200 1454
RESERVED	RW	32	0x0000 0058	0x5200 1058	0x5200 1458
CSI2_SHORT_PACKET	R	32	0x0000 005C	0x5200 105C	0x5200 145C
CSI2_COMPLEXIO_IRQENABLE	RW	32	0x0000 0060	0x5200 1060	0x5200 1460
RESERVED	RW	32	0x0000 0064	0x5200 1064	0x5200 1464
CSI2_DBG_P	W	32	0x0000 0068	0x5200 1068	0x5200 1468
CSI2_TIMING	RW	32	0x0000 006C	0x5200 106C	0x5200 146C
CSI2_CTX_CTRL1_i (1)	RW	32	0x0000 0070 + (0x20 * i)	0x5200 1070 + (0x20 * i)	0x5200 1470 + (0x20 * i)
CSI2_CTX_CTRL2_i (1)	RW	32	0x0000 0074 + (0x20 * i)	0x5200 1074 + (0x20 * i)	0x5200 1474 + (0x20 * i)

(1) i = 0 to 7

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Table 8-154. ISS CSI2 REGS1 Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	ISS_CSI2_A_REGS 1 Base Address	ISS_CSI2_B_REGS 1 Base Address
CSI2_CTX_DAT_OFST_i [1]	RW	32	0x0000 0078 + (0x20 * i)	0x5200 1078 + (0x20 * i)	0x5200 1478 + (0x20 * i)
CSI2_CTX_DAT_PING_ADDR_i [1]	RW	32	0x0000 007C + (0x20 * i)	0x5200 107C + (0x20 * i)	0x5200 147C + (0x20 * i)
CSI2_CTX_DAT_PONG_ADDR_i [1]	RW	32	0x0000 0080 + (0x20 * i)	0x5200 1080 + (0x20 * i)	0x5200 1480 + (0x20 * i)
CSI2_CTX_IRQENABLE_i [1]	RW	32	0x0000 0084 + (0x20 * i)	0x5200 1084 + (0x20 * i)	0x5200 1484 + (0x20 * i)
CSI2_CTX_IRQSTATUS_i [1]	RW	32	0x0000 0088 + (0x20 * i)	0x5200 1088 + (0x20 * i)	0x5200 1488 + (0x20 * i)
CSI2_CTX_CTRL3_i [1]	RW	32	0x0000 008C + (0x20 * i)	0x5200 108C + (0x20 * i)	0x5200 148C + (0x20 * i)

8.2.5.5.2.2 ISS CSI2 REGS1 Register Description

Table 8-155 through Table 8-157 describe the CSI2 REGS1 registers.

Table 8-155. CSI2_REVISION

Address Offset	0x0000 0000
Physical Address	0x5200 1000 0x5200 1400
Description	IP Revision Identifier (X.Y.R) Used by software to track features, bugs, and compatibility
Type	R

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP Revision	R	See [1]

[1] TI internal data

Table 8-156. Register Call Summary for Register CSI2_REVISION

ISS Interfaces

- ISS CSI2 REGS1 Registers: [0]

Table 8-157. CSI2_SYSCONFIG

Address Offset	0x0000 0010
Physical Address	0x5200 1010 0x5200 1410
Description	SYSTEM CONFIGURATION REGISTER This register is the OCP-socket system configuration register.
Type	RW

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																		MSTANDBY_MODE		RESERVED										SOFT_RESET	AUTO_IDLE

Bits	Field Name	Description	Type	Reset
31:14	RESERVED		R	0x00000
13:12	MSTANDBY_MODE	Sets the behavior of the master port power management signals. 0x0: Force-standby. MStandby is only asserted when the module is disabled. 0x1: No-standby. MStandby is never asserted. 0x2: Smart-standby: MStandby is asserted based on the activity of the module. The module will try to go to standby during the vertical blanking period.	RW	0x0
11:2	RESERVED		R	0x000
1	SOFT_RESET	Software reset. Set the bit to 1 to trigger a module reset. The bit is automatically reset by the hardware. During reads return 0. 0x0: Normal mode. 0x1: The module is reset Note: Before setting the software reset bit to 1 in CSI2_SYSCONFIG register, the user must have access to a CSI2 receiver register.	RW	0
0	AUTO_IDLE	Internal OCP gating strategy 0x0: OCP clock is free-running. 0x1: Automatic OCP clock gating strategy is applied based on the OCP interface activity.	RW	1

Table 8-158. Register Call Summary for Register CSI2_SYSCONFIG

ISS Interfaces
- ISS CSI2 Programming Reset Management: [0]
- ISS CSI2 Programming Enable Video/Picture Acquisition: [1] [2]
- ISS CSI2 REGS1 Registers: [3] [4]

Table 8-159. CSI2_SYSSTATUS

Address Offset	0x0000 0014
Physical Address	0x5200 1014 0x5200 1414
Description	SYSTEM STATUS REGISTER This register provides status information about the module, excluding the interrupt status register.
Type	R

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															RESET_DONE

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Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reads returns 0.	R	0x0000 0000
0	RESET_DONE	Internal reset monitoring Read 0x1: Reset completed. Read 0x0: Internal module reset is on going.	R	1

Table 8-160. Register Call Summary for Register CSI2_SYSSTATUS

ISS Interfaces
- ISS CSI2 REGS1 Registers: [0]

Table 8-161. CSI2_IRQSTATUS

Address Offset	0x0000 0018
Physical Address	0x5200 1018 0x5200 1418
Description	INTERRUPT STATUS REGISTER - All contexts This register associates one bit for each context in order to determine which context has generated the interrupt. The context shall be enabled for events to be generated on that context. If the context is disabled, the interrupt is not generated.
Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																OCP_ERR_IRQ	SHORT_PACKET_IRQ	ECC_CORRECTION_IRQ	ECC_NO_CORRECTION_IRQ	RESERVED	COMPLEXIO_ERR_IRQ	FIFO_OVF_IRQ	CONTEXT7	CONTEXT6	CONTEXT5	CONTEXT4	CONTEXT3	CONTEXT2	CONTEXT1	CONTEXT0	

Bits	Field Name	Description	Type	Reset
31:15	RESERVED		R	0x00000
14	OCP_ERR_IRQ	OCP Error Interrupt 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
13	SHORT_PACKET_IRQ	Short packet reception status (other than synch events: Line Start, Line End, Frame Start, and Frame End: data type between 0x8 and x0F only shall be considered). 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
12	ECC_CORRECTION_IRQ	ECC has been used to do the correction of the only 1-bit error status (short packet only). 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
11	ECC_NO_CORRECTION_IRQ	ECC error status (short and long packets). No correction of the header because of more than 1-bit error. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
10	RESERVED	Reserved	R	0
9	COMPLEXIO_ERR_IRQ	Error signaling from complex I/O: status of the PHY errors received from the complex I/O (events are defined in CSI2_COMPLEXIO_IRQSTATUS for the complex I/O). Read 0x1: READS: Event is true (pending). Read 0x0: READS: Event is false.	R	0
8	FIFO_OVF_IRQ	FIFO overflow error status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
7	CONTEXT7	Context 7 Read 0x1: READS: Event is true (pending). Read 0x0: READS: Event is false.	R	0
6	CONTEXT6	Context 6 Read 0x1: READS: Event is true (pending). Read 0x0: READS: Event is false.	R	0
5	CONTEXT5	Context 5 Read 0x1: READS: Event is true (pending). Read 0x0: READS: Event is false.	R	0
4	CONTEXT4	Context 4 Read 0x1: READS: Event is true (pending). Read 0x0: READS: Event is false.	R	0
3	CONTEXT3	Context 3 Read 0x1: READS: Event is true (pending). Read 0x0: READS: Event is false.	R	0
2	CONTEXT2	Context 2 Read 0x1: READS: Event is true (pending). Read 0x0: READS: Event is false.	R	0
1	CONTEXT1	Context 1 Read 0x1: READS: Event is true (pending). Read 0x0: READS: Event is false.	R	0
0	CONTEXT0	Context 0 Read 0x1: READS: Event is true (pending). Read 0x0: READS: Event is false.	R	0

Table 8-162. Register Call Summary for Register CSI2_IRQSTATUS

ISS Interfaces

- ISS CSI2 Functional Description: [0] [1] [2] [3]
- ISS CSI2 Programming Enable Video/Picture Acquisition: [4]
- ISS CSI2 REGS1 Registers: [5]

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Table 8-163. CSI2_IRQENABLE

Address Offset	0x0000 001C
Physical Address	0x5200 101C 0x5200 141C
Description	INTERRUPT ENABLE REGISTER - All contexts This register associates one bit for each context in order to enable/disable each context individually.
Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																OCP_ERR_IRQ	SHORT_PACKET_IRQ	ECC_CORRECTION_IRQ	ECC_NO_CORRECTION_IRQ	RESERVED	COMPLEXIO_ERR_IRQ	FIFO_OVF_IRQ	CONTEXT7	CONTEXT6	CONTEXT5	CONTEXT4	CONTEXT3	CONTEXT2	CONTEXT1	CONTEXT0	

Bits	Field Name	Description	Type	Reset
31:15	RESERVED		R	0x00000
14	OCP_ERR_IRQ	OCP Error Interrupt 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
13	SHORT_PACKET_IRQ	Short packet reception (other than synch events: Line Start, Line End, Frame Start, and Frame End: data type between 0x8 and x0F only shall be considered). 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
12	ECC_CORRECTION_IRQ	ECC has been used to correct the only 1-bit error (short packet only). 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
11	ECC_NO_CORRECTION_IRQ	ECC error (short and long packets). No correction of the header because of more than 1-bit error. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
10	RESERVED	Reserved	RW	0
9	COMPLEXIO_ERR_IRQ	Error signaling from complex I/O: the interrupt is triggered when any error is received from the complex I/O (events are defined in CSI2_COMPLEXIO_IRQSTATUS for the complex I/O). 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
8	FIFO_OVF_IRQ	FIFO overflow enable 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
7	CONTEXT7	Context 7 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0

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Bits	Field Name	Description	Type	Reset
6	CONTEXT6	Context 6 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
5	CONTEXT5	Context 5 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
4	CONTEXT4	Context 4 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
3	CONTEXT3	Context 3 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
2	CONTEXT2	Context 2 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
1	CONTEXT1	Context 1 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
0	CONTEXT0	Context 0 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0

Table 8-164. Register Call Summary for Register CSI2_IRQENABLE

ISS Interfaces

- ISS CSI2 Functional Description: [0] [1]
- ISS CSI2 Programming Enable Video/Picture Acquisition: [2] [3]
- ISS CSI2 REGS1 Registers: [4]

Table 8-165. CSI2_CTRL

Address Offset	0x0000 0040
Physical Address	0x5200 1040 0x5200 1440
Description	GLOBAL CONTROL REGISTER This register controls the CSI2 RECEIVER module. This register shall not be modified dynamically (except IF_EN bit field).
Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															BURST_SIZE_EXPAND	VP_CLK_EN	RESERVED	NON_POSTED_WRITE	RESERVED	VP_ONLY_EN	STREAMING_32_BIT	VP_OUT_CTRL		DBG_EN	BURST_SIZE		ENDIANNESS	FRAME	ECC_EN	RESERVED	IF_EN

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Bits	Field Name	Description	Type	Reset
31:17	RESERVED	Reserved	R	0x0000
16	BURST_SIZE_EXPAND	Sets the DMA burst size on the L3 interconnect. 0x0: Use the burst size defined in the BURST_SIZE register 0x1: Allow generation of 16x64-bit bursts	RW	0
15	VP_CLK_EN	VP clock enable. 0x0: The VP clock is disabled. 0x1: The VP clock is enabled.	RW	0
14	RESERVED	Read returns reset value	RW	0
13	NON_POSTED_WRITE	Not posted writes 0x0: Disable 0x1: Enable	RW	0
12	RESERVED		R	0
11	VP_ONLY_EN	VP only enable. 0x0: The VP is enabled and the OCP master port is enabled. 0x1: The VP is enabled and the OCP master port is disabled.	RW	0
10	STREAMING_32_BIT	Indicates if 64-bit or 32-bit streaming burst is used. Valid only if CSI2_CTRL.STREAMING=1 0x0: 64-bit streaming burst is used; byte enable pattern is 0xFF 0x1: 32-bit streaming burst is used; byte enable pattern is 0x0F	RW	0
9:8	VP_OUT_CTRL	VP_PCLK control. Sets the VP_PCLK as a function of the ISS interconnect interface clock (OCPCLK). 0x0: No division: VP_PCLK = OCPCLK. 0x1: Division by 2: VP_PCLK = OCPCLK / 2. 0x3: Division by 4: VP_PCLK = OCPCLK / 4. 0x2: Division by 3: VP_PCLK = OCPCLK / 3. Example scenarios: - Low VP_PCLK, Memory - VP: Same as typical memory - VP, but VP_PCLK = OCPCLK/2 - Typical sensor - VP: Autoidle enabled, FCLK at optimal rate, sensor provides DPCM compressed RAW12 data at 650 Mbps. Image timings VP_PCLK = (OCPCLK/2) and CCP2_CTRL[31:15] FRACDIV = 0xD000 2600 active pixels/line, 128 blanking pixels, no vertical blanking. (This scenario corresponds to the OTF operation at maximum CCP2 speed.)	RW	0x0
7	DBG_EN	Enables the debug mode. 0x0: Disable 0x1: Enable	RW	0
6:5	BURST_SIZE	Sets the DMA burst size on the L3 interconnect. 0x0: 1x64 OCP writes 0x1: 2x64 OCP writes 0x3: 8x64 OCP writes 0x2: 4x64 OCP writes	RW	0x0
4	ENDIANNESS	Select endianness for YUV4:2:2 8 bit and YUV4:2:0 legacy formats. 0x0: Use native MIPI CSI2 endianness: Little endian for all formats except for YUV4:2:2 8b and YUV4:2:0 Legacy which a big endian. 0x1: Store all pixel formats little endian.	RW	0

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Bits	Field Name	Description	Type	Reset
3	FRAME	Set the modality in which IF_EN works. 0x0: If IF_EN = 0 the interface is disabled immediately. 0x1: If IF_EN = 1 the interface is disabled after all FEC sync code have been received for the active contexts.	RW	0
2	ECC_EN	Enables the Error Correction Code check for the received header (short and long packets for all virtual channel ids). 0x0: Disabled 0x1: Enabled	RW	0
1	RESERVED	Read returns reset value	RW	0
0	IF_EN	Enables the physical interface to the module. 0x0: The interface is disabled. If FRAME = 0, it is disabled immediately. If FRAME = 1, it is disabled when each context has received the FEC sync code. 0x1: The interface is enabled immediately, the data acquisition starts on the next FSC sync code. Writing 1 to this register when the current value is 0 has the effect to clear the output FIFO. The pixel data of the following frame will be written in the PING buffer, that is, the CSI2_CTX_CTRL.PING_PONG bits are reset to 0 as well.	RW	0

Table 8-166. Register Call Summary for Register CSI2_CTRL

ISS Interfaces

- ISS CCP2 Programming Burst Settings: [0] [1]
- ISS CSI2 Protocol and Data Format: [2] [3]
- ISS CSI2 Functional Description: [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18]
- ISS CSI2 Programming Enable Video/Picture Acquisition: [19] [20]
- ISS CSI2 Programming Disable Video/Picture Acquisition: [21] [22] [23]
- ISS CSI2 Programming Progressive and Interleaved Frame Configuration: [24] [25] [26] [27]
- ISS CSI2 REGS1 Registers: [28] [29] [30] [31] [32]

Table 8-167. CSI2_DBG_H

Address Offset	0x0000 0044
Physical Address	0x5200 1044 0x5200 1444
Description	DEBUG REGISTER (Header) This register provides a way to debug the CSI2 RECEIVER module with no image sensor connected to the module. The debug mode is enabled by CSI2_CTRL.DBG_EN. Only full 32-bit values shall be written. The register is used to write short packets and header of long packets.
Type	W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DBG																															

Bits	Field Name	Description	Type	Reset
31:0	DBG	32-bit input value.	W	0x0000 0000

Table 8-168. Register Call Summary for Register CSI2_DBG_H

ISS Interfaces

- ISS CSI2 Programming Progressive and Interleaved Frame Configuration: [0] [1] [2] [3] [4] [5] [6] [7]
- ISS CSI2 REGS1 Registers: [8]

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Table 8-169. CSI2_COMPLEXIO_CFG

Address Offset	0x0000 0050
Physical Address	0x5200 1050 0x5200 1450
Description	COMPLEXIO CONFIGURATION REGISTER for the complex I/O This register contains the lane configuration for the order and position of the lanes (clock and data) and the polarity order for the control of the PHY differential signals in addition to the control bit for the power FSM.
Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	RESET_CTRL	RESET_DONE	PWR_CMD		PWR_STATUS		PWR_AUTO	RESERVED				DATA4_POL	DATA4_POSITION			DATA3_POL	DATA3_POSITION			DATA2_POL	DATA2_POSITION			DATA1_POL	DATA1_POSITION			CLOCK_POL	CLOCK_POSITION		

Bits	Field Name	Description	Type	Reset
31	RESERVED		R	0
30	RESET_CTRL	Controls the reset of the complex I/O 0x0: Complex I/O reset active. 0x1: Complex I/O reset deasserted.	RW	0
29	RESET_DONE	Internal reset monitoring of the power domain using the byte clock provided by the associated CSIPHY (see Section 8.1.1, *ISS Clock Domains*. **Caution:** For the CSI2_COMPLEXIO_CFG[29] RESET_DONE bit to be set to 0x1 (reset completed), the external sensor must to be active and sending the MIPI HS BYTECLK. Read 0x1: Reset completed. Read 0x0: Internal module reset is ongoing.	R	0
28:27	PWR_CMD	Command for power control of the complex I/O 0x0: Command to change to OFF state 0x1: Command to change to ON state 0x2: Command to change to Ultralow-Power state	RW	0x0
26:25	PWR_STATUS	Status of the power control of the complex I/O Read 0x2: Complex I/O in Ultralow-Power state Read 0x1: Complex I/O in ON state Read 0x0: Complex I/O in OFF state	R	0x0
24	PWR_AUTO	Automatic switch between ULP and ON states based on ULPM signals from complex I/O 0x0: Disable 0x1: Enable	RW	0
23:20	RESERVED		R	0x0
19	DATA4_POL	+/- differential pin order of data lane 4. 0x0: +/- pin order 0x1: -/+ pin order	RW	0

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Bits	Field Name	Description	Type	Reset
18:16	DATA4_POSITION	Position and order of the data lane 4. The values 6 and 7 are reserved. This lane is not available for CSI2-B receiver. 0x0: This data lane is not used. 0x1: Data lane 4 is at position 1. This position is not available to the CSI2-B receiver. 0x2: Data lane 4 is at position 2. This position is not available to the CSI2-B receiver. 0x3: Data lane 4 is at position 3. This position is not available to the CSI2-B receiver. 0x4: Data lane 4 is at position 4. This position is not available to the CSI2-B receiver. 0x5: Data lane 4 is at position 5. This position is not available to the CSI2-B receiver. 0x6: Reserved 0x7: Reserved	RW	0x0
15	DATA3_POL	+/- differential pin order of data lane 3. 0x0: +/- pin order 0x1: -/+ pin order	RW	0
14:12	DATA3_POSITION	Position and order of the data lane 3. The values 6 and 7 are reserved. This lane is not available for CSI2-B receiver. 0x0: This data lane is not used. 0x1: Data lane 3 is at position 1. This position is not available to the CSI2-B receiver. 0x2: Data lane 3 is at position 2. This position is not available to the CSI2-B receiver. 0x3: Data lane 3 is at position 3. This position is not available to the CSI2-B receiver. 0x4: Data lane 3 is at position 4. This position is not available to the CSI2-B receiver. 0x5: Data lane 3 is at position 5. This position is not available to the CSI2-B receiver. 0x6: Reserved 0x7: Reserved	RW	0x0
11	DATA2_POL	+/- differential pin order of DATA lane 2. 0x0: +/- pin order (csi2_dx=+ and csi2_dy=-) 0x1: -/+ pin order (csi2_dx=- and csi2_dy=+)	RW	0
10:8	DATA2_POSITION	Position and order of the data lane 2. The values 6 and 7 are reserved. 0x0: This data lane is not used. 0x1: Data lane 2 is at position 1. 0x2: Data lane 2 is at position 2. 0x3: Data lane 2 is at position 3. 0x4: Data lane 2 is at position 4. This position is not available to the CSI2-B receiver. 0x5: Data lane 2 is at position 5. This position is not available to the CSI2-B receiver. 0x6: Reserved 0x7: Reserved	RW	0x0
7	DATA1_POL	+/- differential pin order of data lane 1. 0x0: +/- pin order (csi2_dx=+ and csi2_dy=-) 0x1: -/+ pin order (csi2_dx=- and csi2_dy=+)	RW	0

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Bits	Field Name	Description	Type	Reset
6:4	DATA1_POSITION	Position and order of the DATA lane 1. The values 6 and 7 are reserved. When CSI2 is used, the data lane 1 position must be different from 0, 6, or 7. 0x0: This data lane is not used. 0x1: Data lane 1 is at position 1. x2: Data lane 1 is at position 2. 0x3: Data lane 1 is at position 3. 0x4: Data lane 1 is at position 4. This position is not available to the CSI2-B receiver. 0x5: Data lane 1 is at position 5. This position is not available to the CSI2-B receiver. 0x6: Reserved 0x7: Reserved	RW	0x0
3	CLOCK_POL	+/- differential pin order of clock lane. 0x0: +/- pin order (csi2_dx=+ and csi2_dy=-) 0x1: -/+ pin order (csi2_dx=- and csi2_dy=+)	RW	0
2:0	CLOCK_POSITION	Position and order of the clock lane. The values 5, 6, and 7 are reserved. When CSI2 is used, the clock lane position must be different from 0, 5, 6, or 7. 0x0: This data lane is not used. 0x1: Clock lane is at position 1. 0x2: Clock lane is at position 2. 0x3: Clock lane is at position 3. 0x4: Clock lane is at position 4. This position is not available to the CSI2-B receiver. 0x5: Reserved 0x6: Reserved 0x7: Reserved	RW	0x0

Table 8-170. Register Call Summary for Register CSI2_COMPLEXIO_CFG

ISS Interfaces

- ISS CSI2 PHY Functional Configuration: [0] [1] [2]
- ISS CSI2 PHY and Link Initialization Sequence: [3] [4] [5] [6] [7] [8] [9] [10] [11]
- ISS CCP2 and Link Initialization Sequence: [12] [13] [14] [15] [16]
- ISS CSI2 Functional Description: [17] [18] [19]
- ISS CSI2 Programming Reset Management: [20]
- ISS CSI2 Programming Enable Video/Picture Acquisition: [21] [22] [23] [24]
- ISS CSI2 REGS1 Registers: [25] [26]

Table 8-171. CSI2_COMPLEXIO_IRQSTATUS

Address Offset	0x0000 0054
Physical Address	0x5200 1054 0x5200 1454
Description	INTERRUPT STATUS REGISTER - All errors from complex I/O #1
Type	RW

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					STATEALLULPMEXIT	STATEALLULPMENTER	STATEULPM5	STATEULPM4	STATEULPM3	STATEULPM2	STATEULPM1	ERRCONTROL5	ERRCONTROL4	ERRCONTROL3	ERRCONTROL2	ERRCONTROL1	ERRESC5	ERRESC4	ERRESC3	ERRESC2	ERRESC1	ERRSOTSYNCHS5	ERRSOTSYNCHS4	ERRSOTSYNCHS3	ERRSOTSYNCHS2	ERRSOTSYNCHS1	ERRSOTHS5	ERRSOTHS4	ERRSOTHS3	ERRSOTHS2	ERRSOTHS1

Bits	Field Name	Description	Type	Reset
31:27	RESERVED		R	0x00
26	STATEALLULPMEXIT	At least one of the active lanes has exit the ULPM 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
25	STATEALLULPMENTER	All active lanes are entering in ULPM. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
24	STATEULPM5	Lane 5 in ULPM 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
23	STATEULPM4	Lane 4 in ULPM 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
22	STATEULPM3	Lane 3 in ULPM 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
21	STATEULPM2	Lane 2 in ULPM 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
20	STATEULPM1	Lane 1 in ULPM 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
19	ERRCONTROL5	Control error for lane 5 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
18	ERRCONTROL4	Control error for lane 4 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
17	ERRCONTROL3	Control error for lane 3 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
16	ERRCONTROL2	Control error for lane 2 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
15	ERRCONTROL1	Control error for lane 1 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
14	ERRESC5	Escape entry error for lane 5 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
13	ERRESC4	Escape entry error for lane 4 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
12	ERRESC3	Escape entry error for lane 3 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
11	ERRESC2	Escape entry error for lane 2 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
10	ERRESC1	Escape entry error for lane 1 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
9	ERRSOTSYNCHS5	Start of transmission sync error for lane 5 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
8	ERRSOTSYNCHS4	Start of transmission sync error for lane 4 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
7	ERRSOTSYNCHS3	Start of transmission sync error for lane 3 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
6	ERRSOTSYNCHS2	Start of transmission sync error for lane 2 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
5	ERRSOTSYNCHS1	Start of transmission sync error for lane 1 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
4	ERRSOTHS5	Start of transmission error for lane 5 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
3	ERRSOTHS4	Start of transmission error for lane 4 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
2	ERRSOTHS3	Start of transmission error for lane 3 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
1	ERRSOTHS2	Start of transmission error for lane 2 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
0	ERRSOTHS1	Start of transmission error for lane 1 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0

Table 8-172. Register Call Summary for Register CSI2_COMPLEXIO_IRQSTATUS

ISS Interfaces

- ISS CSI2 PHY Functional Configuration: [0]
- ISS CSI2 Programming Enable Video/Picture Acquisition: [1]
- ISS CSI2 REGS1 Registers: [2] [3] [4]

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Table 8-173. CSI2_SHORT_PACKET

Address Offset	0x0000 005C
Physical Address	0x5200 105C 0x5200 145C
Description	SHORT PACKET INFORMATION - This register sets the 24-bit DATA_ID + Short Packet Data Field when the data type is between 0x8 and x0F
Type	R

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								SHORT_PACKET																							

Bits	Field Name	Description	Type	Reset
31:24	RESERVED	Reads returns 0.	R	0x00
23:0	SHORT_PACKET	Short Packet information: DATA ID + DATA FIELD	R	0x000000

Table 8-174. Register Call Summary for Register CSI2_SHORT_PACKET

ISS Interfaces

- ISS CSI2 Functional Description: [0] [1]
- ISS CSI2 REGS1 Registers: [2]

Table 8-175. CSI2_COMPLEXIO_IRQENABLE

Address Offset	0x0000 0060
Physical Address	0x5200 1060 0x5200 1460
Description	INTERRUPT ENABLE REGISTER - All errors from complex I/O
Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					STATEALLULPMEXIT	STATEALLULPMENTER	STATEULPM5	STATEULPM4	STATEULPM3	STATEULPM2	STATEULPM1	ERRCONTROL5	ERRCONTROL4	ERRCONTROL3	ERRCONTROL2	ERRCONTROL1	ERRESC5	ERRESC4	ERRESC3	ERRESC2	ERRESC1	ERRSOTSYNCHS5	ERRSOTSYNCHS4	ERRSOTSYNCHS3	ERRSOTSYNCHS2	ERRSOTSYNCHS1	ERRSOTHS5	ERRSOTHS4	ERRSOTHS3	ERRSOTHS2	ERRSOTHS1

Bits	Field Name	Description	Type	Reset
31:27	RESERVED		R	0x00
26	STATEALLULPMEXIT	At least one of the active lanes has exit the ULPM 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
25	STATEALLULPMENTER	All active lanes are entering in ULPM. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
24	STATEULPM5	Lane 5 in ULPM 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0

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Bits	Field Name	Description	Type	Reset
23	STATEULPM4	Lane 4 in ULPM 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
22	STATEULPM3	Lane 3 in ULPM 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
21	STATEULPM2	Lane 2 in ULPM 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
20	STATEULPM1	Lane 1 in ULPM 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
19	ERRCONTROL5	Control error for lane 5 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
18	ERRCONTROL4	Control error for lane 4 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
17	ERRCONTROL3	Control error for lane 3 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
16	ERRCONTROL2	Control error for lane 2 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
15	ERRCONTROL1	Control error for lane 1 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
14	ERRESC5	Escape entry error for lane 5 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
13	ERRESC4	Escape entry error for lane 4 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
12	ERRESC3	Escape entry error for lane 3 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
11	ERRESC2	Escape entry error for lane 2 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
10	ERRESC1	Escape entry error for lane 1 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
9	ERRSOTSYNCHS5	Start of transmission sync error for lane 5 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
8	ERRSOTSYNCHS4	Start of transmission sync error for lane 4 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0

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Bits	Field Name	Description	Type	Reset
7	ERRSOTSYNCHS3	Start of transmission sync error for lane 3 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
6	ERRSOTSYNCHS2	Start of transmission sync error for lane 2 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
5	ERRSOTSYNCHS1	Start of transmission sync error for lane 1 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
4	ERRSOTHS5	Start of transmission error for lane 5 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
3	ERRSOTHS4	Start of transmission error for lane 4 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
2	ERRSOTHS3	Start of transmission error for lane 3 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
1	ERRSOTHS2	Start of transmission error for lane 2 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
0	ERRSOTHS1	Start of transmission error for lane 1 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0

Table 8-176. Register Call Summary for Register CSI2_COMPLEXIO_IRQENABLE

ISS Interfaces

- ISS CSI2 Programming Enable Video/Picture Acquisition: [0]
- ISS CSI2 REGS1 Registers: [1]

Table 8-177. CSI2_DBG_P

Address Offset 0x0000 0068

Physical Address 0x5200 1068
0x5200 1468

Description DEBUG REGISTER (Payload)
This register provides a way to debug the CSI2 RECEIVER module with no image sensor connected to the module. The debug mode is enabled by CSI2_CTRL.DBG_EN. Only full 32-bit values shall be written. The register is used to write payload of long packets.

Type W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DBG																															

Bits	Field Name	Description	Type	Reset
31:0	DBG	32-bit input value.	W	0x0000 0000

Table 8-178. Register Call Summary for Register CSI2_DBG_P

ISS Interfaces

- ISS CSI2 Programming Progressive and Interleaved Frame Configuration: [0] [1]
- ISS CSI2 REGS1 Registers: [2]

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Table 8-179. CSI2_TIMING

Address Offset	0x0000 006C
Physical Address	0x5200 106C 0x5200 146C
Description	TIMING REGISTER This register controls the CSI2 RECEIVER module. This register shall not be modified while CSI2_CTRL.IF_EN is set to 1. It is used to indicate the number of L3 cycles for the Stop State monitoring.
Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			RESERVED													FORCE_RX_MODE_IO1			STOP_STATE_X16_IO1					STOP_STATE_X4_IO1							
RESERVED			RESERVED																					STOP_STATE_COUNTER_IO1							
RESERVED			RESERVED																												

Bits	Field Name	Description	Type	Reset
31	RESERVED	Read returns reset value	RW	0
30	RESERVED	Read returns reset value	RW	1
29	RESERVED	Read returns reset value	RW	1
28:16	RESERVED	Read returns reset value	RW	0x1FFF
15	FORCE_RX_MODE_IO1	Control of ForceRxMode signal 0x0: Deassertion of ForceRxMode. The hardware reset the bit at the end of the Force RX Mode assertion. The software can reset the bit in order to stop the assertion of the ForceRXMode signal prior to the completion of the period. 0x1: Assertion of ForceRxMode	RW	0
14	STOP_STATE_X16_IO1	Multiplication factor for the number of L3 cycles defined in STOP_STATE_COUNTER bit field 0x0: The number of L3 cycles defined in STOP_STATE _COUNTER is multiplied by 1x 0x1: The number of L3 cycles defined in STOP_STATE _COUNTER is multiplied by 16x	RW	1
13	STOP_STATE_X4_IO1	Multiplication factor for the number of L3 cycles defined in STOP_STATE_COUNTER bit field 0x0: The number of L3 cycles defined in STOP_STATE _COUNTER is multiplied by 1x 0x1: The number of L3 cycles defined in STOP_STATE _COUNTER is multiplied by 4x	RW	1
12:0	STOP_STATE_COUNTER_IO1	Stop State counter for monitoring. It indicates the number of L3 to monitor for Stop State before deasserting ForceRxMode (complex I/O 1). The value is from 0 to 8191.	RW	0x1FFF

Table 8-180. Register Call Summary for Register CSI2_TIMING

ISS Interfaces

- ISS CSI2 PHY Functional Configuration: [0] [1] [2] [3] [4] [5] [6] [7]
- ISS CSI2 PHY and Link Initialization Sequence: [8] [9] [10]
- ISS CCP2 and Link Initialization Sequence: [11] [12]
- ISS CSI2 Programming Enable Video/Picture Acquisition: [13]
- ISS CSI2 REGS1 Registers: [14]

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Table 8-181. CSI2_CTX_CTRL1_i

Address Offset	0x0000 0070 + (0x20 * i)	**Index**	i = 0 to 7
Physical Address	0x5200 1070 + (0x20 * i) 0x5200 1470 + (0x20 * i)		
Description	CONTROL REGISTER - Context This register controls the Context. This register is shadowed: modifications are taken into account after the next FSC sync code.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BYTESWAP	GENERIC	RESERVED	HSCALE	TRANSCODE				FEC_NUMBER								COUNT								EOF_EN	EOL_EN	CS_EN	COUNT_UNLOCK	PING_PONG	VP_FORCE	LINE_MODULO	CTX_EN

Bits	Field Name	Description	Type	Reset
31	BYTESWAP	Allows swapping bytes two by two in the payload data. It does not affect: - short packets - long packet header or footers - CRC calculation The purpose is to by swap data send to the OCP port and/or video port 0x0: Disabled 0x1: Enabled	RW	0
30	GENERIC	Enables the generic mode. 0x0: Disabled. Data is received according to CSI2_CTX_CTRL1.FORMAT and the long packet code transmitted in the MIPI stream is used. 0x1: Enabled. Data is received according to CSI2_CTX_CTRL1.FORMAT and the long packet code transmitted in the MIPI stream is ignored.	RW	0
29	RESERVED		R	0x0
28	HSCALE	Enable horizontal downscaling by a factor of two. Applies to RAW data when transcoding is enabled. 0x0: Disable 0x1: Enable	RW	0x0

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Bits	Field Name	Description	Type	Reset
27:24	TRANSCODE	Enables image transcoding. When this features is enabled: - the data format from the camera is defined by the FORMAT register - the format after transcode is defined by the TRANSCODE register. The memory storage / video port formats is defined by the TRANSCODE register 0x6: Outputs uncompressed RAW10 data. Data in memory is organized as regular packed RAW10 data 0x1: Outputs DPCM compressed RAW10 data. After compression, pixels are coded on 8 bits. Data in memory is organized as regular RAW8 data 0x7: Outputs uncompressed RAW12 data. Data in memory is organized as regular RAW12+EXP16 data 0x0: Feature disabled. 0x2: Outputs DPCM compressed RAW12 data. After compression, pixels are coded on 8 bits. Data in memory is organized as regular RAW8 data 0x8: Outputs uncompressed RAW12 data. Data in memory is organized as regular packed RAW12 data 0x9: Outputs uncompressed RAW14 data. 0x4: Outputs uncompressed RAW8 data. Data in memory is organized as regular RAW8 data 0x5: Outputs uncompressed RAW10 data. Data in memory is organized as regular RAW10+EXP16 data 0x3: Outputs A-Law compressed RAW10 data. After compression, pixels are coded on 8 bits. Data in memory is organized as regular RAW8 data.	RW	0x0
23:16	FEC_NUMBER	Number of FEC to receive between using swap of CSI2_CTX_DAT_PING_ADDR and CSI2_CTX_DAT_PONG_ADDR for the calculation of the address in memory (must be used only in interlace mode, otherwise set to 1).	RW	0x01
15:8	COUNT	Sets the number of frame to acquire. Once the frame acquisition starts, the COUNT value is decremented after every frame. When COUNT reaches 0, the FRAME_NUMBER_IRQ interrupt is triggered and CTX_EN is set to 0. Writes to this bit field are controlled by the COUNT_UNLOCK bit. During the same OCP write access, the bit field COUNT_UNLOCK shall be written in addition to COUNT bit field in order to change the COUNT value. COUNT can be overwritten dynamically with a new count value. 0: Infinite number of frames (no count). 1: 1 frame to acquire ... 255: 255 frames to acquire	RW	0x00
7	EOF_EN	Indicates if the end of frame signal shall be asserted at the end of the line. Read 0x1: The end of frame signal is asserted at the end of each frame. Read 0x0: The end of frame signal is not asserted at the end of each frame.	RW	0

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Bits	Field Name	Description	Type	Reset
6	EOL_EN	Indicates if the end of line signal shall be asserted at the end of the line. Read 0x1: The end of line signal is asserted at the end of each frame. Read 0x0: The end of line signal is not asserted at the end of each frame.	RW	0
5	CS_EN	Enables the checksum check for the received payload (long packet only). 0x0: Disabled 0x1: Enabled	RW	0
4	COUNT_UNLOCK	Unlock writes to the COUNT bit field. Write 0x0: COUNT bit field is locked. Writes have no effect Write 0x1: COUNT bit field is unlocked. Writes are possible.	W	0
3	PING_PONG	Indicates whether the PING or PONG destination address (CSI2_CTX_DAT_PING_ADDR or CSI2_CTX_DAT_PONG_ADDR) was used to write the last frame. This bit field toggles after every FEC_NUMBER FEC sync code received for the current context. Read 0x1: PONG buffer Read 0x0: PING buffer	R	1
2	VP_FORCE	Forces sending of the data to both VPORT and OCP. Only applies to formats that existing in two versions: - One sending data to OCP port only - One sending data to VPORT only (tagged with the +VP extension) The format version sending data only to OCP should be chosen. 0x0: Disabled 0x1: Enabled	RW	0
1	LINE_MODULO	Line modulo configuration 0x0: CSI2_CTX_CTRL3.LINE_NUMBER is used once per frame for the generation of the LINE_NUMBER_IRQ. 0x1: CSI2_CTX_CTRL3.LINE_NUMBER is used as a modulo number for the generation of the LINE_NUMBER_IRQ (multiple times the interrupt can be generated for each frame)	RW	0
0	CTX_EN	Enables the context 0x0: Disabled 0x1: Enabled	RW	0

Table 8-182. Register Call Summary for Register CSI2_CTX_CTRL1_i

ISS Interfaces

- ISS CSI2 Protocol and Data Format: [0]
- ISS CSI2 Functional Description: [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18]
- ISS CSI2 Programming Enable Video/Picture Acquisition: [19] [20] [21] [22] [23]
- ISS CSI2 Programming Disable Video/Picture Acquisition: [24]
- ISS CSI2 Programming Capture a Finite Number of Frames: [25] [26] [27]
- ISS CSI2 Programming a Periodic Event During Frame Acquisition: [28]
- ISS CSI2 Programming Progressive and Interleaved Frame Configuration: [29]
- ISS CSI2 REGS1 Registers: [30]

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Table 8-183. CSI2_CTX_CTRL2_i

Address Offset	0x0000 0074 + (0x20 * i)	**Index**	i = 0 to 7
Physical Address	0x5200 1074 + (0x20 * i) 0x5200 1474 + (0x20 * i)		
Description	CONTROL REGISTER - Context This register controls the Context. This register is shadowed: modifications are taken into account after the next FSC sync code (except for VIRTUAL_ID and FORMAT fields). The change of VIRTUIAL_ID and FORMAT has to occur only when the context is disabled (CSI2_CTX_CTRL1.CTX_EN).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FRAME																RESERVED	USER_DEF_MAPPING		VIRTUAL_ID		DPCM_PRED		FORMAT							

Bits	Field Name	Description	Type	Reset
31:16	FRAME	Frame number received	R	0x0000
15	RESERVED		R	0
14:13	USER_DEF_MAPPING	Selects the pixel format of USER_DEFINED in FORMAT 0x0: RAW6 0x1: RAW7 0x2: RAW8 (not valid if FORMAT is USER_DEFINED_8_BIT_DATA_TYPE_x_EXP8 with x from 1 to 8)	RW	0x0
12:11	VIRTUAL_ID	Virtual channel ID 0x0: Virtual Channel ID 0 0x1: Virtual Channel ID 1 0x3: Virtual Channel ID 3 0x2: Virtual Channel ID 2	RW	0x0
10	DPCM_PRED	Selects the DPCM predictor. 0x0: The advanced predictor is used. Not supported for 10- 8- 10 algorithm. Performance limited to 1 pixel/cycle. 0x1: The simple predictor is used.	RW	0
9:0	FORMAT	Data format selection. 0x3A9: RAW7 DPCM12 + VP 0x80: USER_DEFINED_8_BIT_DATA_TYPE_1 + EXP8 0x84: USER_DEFINED_8_BIT_DATA_TYPE_5 + EXP8 0x346: USER_DEFINED_8_BIT_DATA_TYPE_7 + DPCM10 + VP 0x1D: YUV4:2:0 10bit + CSPS 0x2C6: USER_DEFINED_8_BIT_DATA_TYPE_7 + DPCM10 + EXP16 0x41: USER_DEFINED_8_BIT_DATA_TYPE_2 0x1C5: USER_DEFINED_8_BIT_DATA_TYPE_6_DPCM12_EXP16 0xAC: RAW12 + EXP16 0x145: USER_DEFINED_8_BIT_DATA_TYPE_6_DPCM12_VP	RW	0x000

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Bits	Field Name	Description	Type	Reset
		0x12: Embedded 8-bit nonimage data (that is, JPEG)		
		0x46: USER_DEFINED_8_BIT_DATA_TYPE_7		
		0x83: USER_DEFINED_8_BIT_DATA_TYPE_4 + EXP8		
		0x2B: RAW10		
		0x9E: YUV4:2:2 8bit + VP		
		0x1C0: USER_DEFINED_8_BIT_DATA_TYPE_1_DPCM12_EXP16		
		0x140: USER_DEFINED_8_BIT_DATA_TYPE_1_DPCM12_VP		
		0x329: RAW7 + DPCM10 + VP		
		0x22: RGB565		
		0x68: RAW6 + EXP8		
		0x43: USER_DEFINED_8_BIT_DATA_TYPE_4		
		0xE3: RGB666 + EXP32		
		0x1C7: USER_DEFINED_8_BIT_DATA_TYPE_8_DPCM12_EXP16		
		0x143: USER_DEFINED_8_BIT_DATA_TYPE_4_DPCM12_VP		
		0xA0: RGB444 + EXP16		
		0x87: USER_DEFINED_8_BIT_DATA_TYPE_8 + EXP8		
		0x85: USER_DEFINED_8_BIT_DATA_TYPE_6 + EXP8		
		0x0: OTHERS (except NULL and BLANKING packets)		
		0x341: USER_DEFINED_8_BIT_DATA_TYPE_2 + DPCM10 + VP		
		0xAD: RAW14 + EXP16		
		0x2C3: USER_DEFINED_8_BIT_DATA_TYPE_4 + DPCM10 + EXP16		
		0xE4: RGB888 + EXP32		
		0x343: USER_DEFINED_8_BIT_DATA_TYPE_4 + DPCM10 + VP		
		0x368: RAW6 DPCM12 + VP		
		0x12C: RAW12 + VP		
		0x42: USER_DEFINED_8_BIT_DATA_TYPE_3		
		0xA1: RGB555 + EXP16		
		0x12D: RAW14 + VP		
		0x144: USER_DEFINED_8_BIT_DATA_TYPE_5_DPCM12_VP		
		0x1C4: USER_DEFINED_8_BIT_DATA_TYPE_5_DPCM12_EXP16		
		0x2A: RAW8		
		0x3AA: RAW8 DPCM12 + VP		
		0x2C1: USER_DEFINED_8_BIT_DATA_TYPE_2 + DPCM10 + EXP16		
		0x1C3: USER_DEFINED_8_BIT_DATA_TYPE_4_DPCM12_EXP16		
		0x342: USER_DEFINED_8_BIT_DATA_TYPE_3 + DPCM10 + VP		
		0x142: USER_DEFINED_8_BIT_DATA_TYPE_3_DPCM12_VP		
		0x1A: YUV4:2:0 8bit legacy		

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Bits	Field Name	Description	Type	Reset
		0x36A: RAW8 DPCM12 + EXP16		
		0x32A: RAW8 + DPCM10 + VP		
		0x229: RAW7 + DPCM10 + EXP16		
		0x12A: RAW8 + VP		
		0x28: RAW6		
		0x1C1: USER_DEFINED_8_BIT_DATA_TYPE_2_DPCM12_EXP16		
		0x2A8: RAW6 + DPCM10 + EXP16		
		0x45: USER_DEFINED_8_BIT_DATA_TYPE_6		
		0xDE: Same as YUV4:2:2 8bit + VP but data is send as 16-bit wide words to video port. Could be used together with the GENERIC and BYTESWAP features.		
		0x340: USER_DEFINED_8_BIT_DATA_TYPE_1 + DPCM10 + VP		
		0x40: USER_DEFINED_8_BIT_DATA_TYPE_1		
		0x19: YUV4:2:0 10 bit		
		0x344: USER_DEFINED_8_BIT_DATA_TYPE_5 + DPCM10 + VP		
		0x2C2: USER_DEFINED_8_BIT_DATA_TYPE_3 + DPCM10 + EXP16		
		0x141: USER_DEFINED_8_BIT_DATA_TYPE_2_DPCM12_VP		
		0x369: RAW7 DPCM12 + EXP16		
		0x69: RAW7 + EXP8		
		0x2C4: USER_DEFINED_8_BIT_DATA_TYPE_5 + DPCM10 + EXP16		
		0x1C: YUV4:2:0 8 bit + CSPS		
		0x347: USER_DEFINED_8_BIT_DATA_TYPE_8 + DPCM10 + VP		
		0x146: USER_DEFINED_8_BIT_DATA_TYPE_7_DPCM12_VP		
		0x82: USER_DEFINED_8_BIT_DATA_TYPE_3 + EXP8		
		0x47: USER_DEFINED_8_BIT_DATA_TYPE_8		
		0x2AA: RAW8 + DPCM10 + EXP16		
		0x1E: YUV4:2:2 8 bit		
		0x33: RGB666 + EXP32_24		
		0x2C: RAW12		
		0x2C7: USER_DEFINED_8_BIT_DATA_TYPE_8 + DPCM10 + EXP16		
		0x147: USER_DEFINED_8_BIT_DATA_TYPE_8_DPCM12_VP		
		0x81: USER_DEFINED_8_BIT_DATA_TYPE_2 + EXP8		
		0x24: RGB888		
		0x2D: RAW14		
		0x345: USER_DEFINED_8_BIT_DATA_TYPE_6 + DPCM10 + VP		
		0xAB: RAW10 + EXP16		
		0x3A8: RAW6 DPCM12 + EXP16		
		0x44: USER_DEFINED_8_BIT_DATA_TYPE_5		
		0x2C0: USER_DEFINED_8_BIT_DATA_TYPE_1 + DPCM10 + EXP16		
		0x18: YUV4:2:0 8 bit		

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Bits	Field Name	Description	Type	Reset
		0x12F: RAW10 + VP 0xE8: RAW6 + DPCM10 + VP 0x1F: YUV4:2:2 10 bit 0x2C5: USER_DEFINED_8_BIT_DATA_TYPE_6 + DPCM10 + EXP16 0x1C2: USER_DEFINED_8_BIT_DATA_TYPE_3_DPCM12_EXP16 0x1C6: USER_DEFINED_8_BIT_DATA_TYPE_7_DPCM12_EXP16 0x29: RAW7 0x86: USER_DEFINED_8_BIT_DATA_TYPE_7 + EXP8		

Table 8-184. Register Call Summary for Register CSI2_CTX_CTRL2_i

ISS Interfaces

- ISS CSI2 Protocol and Data Format: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21]
- ISS CSI2 Functional Description: [22] [23] [24] [25] [26] [27] [28] [29]
- ISS CSI2 Programming a Context to a Virtual Channel and a Data Type: [30] [31] [32]
- ISS CSI2 REGS1 Registers: [33]

Table 8-185. CSI2_CTX_DAT_OFST_i

Address Offset	0x0000 0078 + (0x20 * i)	**Index**	i = 0 to 7
Physical Address	0x5200 1078 + (0x20 * i) 0x5200 1478 + (0x20 * i)		
Description	DATA MEM ADDRESS OFFSET REGISTER - Context This register sets the offset, which is applied on the destination address after each line is written to memory. This register applies for both CSI2_CTX_DAT_PING_ADDR and CSI2_CTX_DAT_PONG_ADDR. For example, it enables to perform 2D data transfers of the pixel data into a frame buffer. In such case, the pixel data and frame buffer data shall have the same data format. The 5 LSBs are ignored: the offset shall be a multiple of 32 bytes. This register is shadowed: modifications are taken into account after the next FSC sync code. Only full 32-bit values shall be written.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								OFST																RESERVED							

Bits	Field Name	Description	Type	Reset
31:17	RESERVED		R	0x0000
16:5	OFST	Line offset programmed in bytes (signed value 2s complement). If OFST = 0, the data is written contiguously in memory. Otherwise, OFST sets the destination offset between the first pixel of the previous line and the first pixel of the current line.	RW	0x000
4:0	RESERVED		R	0x00

Table 8-186. Register Call Summary for Register CSI2_CTX_DAT_OFST_i

ISS Interfaces

- ISS CSI2 Protocol and Data Format: [0] [1]
- ISS CSI2 Functional Description: [2] [3] [4]
- ISS CSI2 Programming Enable Video/Picture Acquisition: [5]
- ISS CSI2 REGS1 Registers: [6]

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Table 8-187. CSI2_CTX_DAT_PING_ADDR_i

Address Offset	0x0000 007C + (0x20 * i)	**Index**	i = 0 to 7
Physical Address	0x5200 107C + (0x20 * i) 0x5200 147C + (0x20 * i)		
Description	DATA MEM PING ADDRESS REGISTER - Context This register sets the 32-bit memory address where the pixel data are stored. The destination is double buffered: this register sets the PING address. Double buffering is enabled when the addresses CSI2_CTX_DAT_PING_ADDR and CSI2_CTX_DAT_PONG_ADDR are different. The 5 LSBs are ignored: the address shall be aligned on a 32-byte boundary. This register is shadowed: modifications are taken into account after the next FSC sync code. Only full 32-bit values shall be written.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR																											RESERVED					

Bits	Field Name	Description	Type	Reset
31:5	ADDR	27 most-significant bits of the 32-bit address.	RW	0x0000000
4:0	RESERVED		R	0x00

Table 8-188. Register Call Summary for Register CSI2_CTX_DAT_PING_ADDR_i

ISS Interfaces

- ISS CSI2 Functional Description: [0] [1]
- ISS CSI2 Programming Enable Video/Picture Acquisition: [2] [3]
- ISS CSI2 REGS1 Registers: [4]

Table 8-189. CSI2_CTX_DAT_PONG_ADDR_i

Address Offset	0x0000 0080 + (0x20 * i)	**Index**	i = 0 to 7
Physical Address	0x5200 1080 + (0x20 * i) 0x5200 1480 + (0x20 * i)		
Description	DATA MEM PONG ADDRESS REGISTER - Context This register sets the 32-bit memory address where the pixel data are stored. The destination is double-buffered: this register sets the PONG address. Double-buffering is enabled when the addresses CSI2_CTX_DAT_PING_ADDR and CSI2_CTX_DAT_PONG_ADDR are different. The 5 LSBs are ignored: the address shall be aligned on a 32-byte boundary. This register is shadowed: modifications are taken into account after the next FSC sync code. Only full 32-bit values shall be written.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR																											RESERVED					

Bits	Field Name	Description	Type	Reset
31:5	ADDR	27 most-significant bits of the 32-bit address.	RW	0x0000000
4:0	RESERVED		R	0x00

Table 8-190. Register Call Summary for Register CSI2_CTX_DAT_PONG_ADDR_i

ISS Interfaces

- ISS CSI2 Functional Description: [0] [1]
- ISS CSI2 REGS1 Registers: [2]

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Table 8-191. CSI2_CTX_IRQENABLE_i

Address Offset	0x0000 0084 + (0x20 * i)	**Index**	i = 0 to 7
Physical Address	0x5200 1084 + (0x20 * i) 0x5200 1484 + (0x20 * i)		
Description	INTERRUPT ENABLE REGISTER - Context This register regroups all the events related to context.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							ECC_CORRECTION_IRQ	LINE_NUMBER_IRQ	FRAME_NUMBER_IRQ	CS_IRQ	RESERVED	LE_IRQ	LS_IRQ	FE_IRQ	FS_IRQ

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	ECC_CORRECTION_IRQ	Context - ECC has been used to correct the only 1-bit error (long packet only). 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
7	LINE_NUMBER_IRQ	Context - Line number is reached. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
6	FRAME_NUMBER_IRQ	Context - Frame counter reached. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
5	CS_IRQ	Context - Check-Sum of the payload mismatch detection 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
4	RESERVED		R	0
3	LE_IRQ	Context - Line end sync code detection. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
2	LS_IRQ	Context - Line start sync code detection. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
1	FE_IRQ	Context - Frame end sync code detection. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
0	FS_IRQ	Context - Frame start sync code detection. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0

Table 8-192. Register Call Summary for Register CSI2_CTX_IRQENABLE_i

ISS Interfaces

- ISS CSI2 Functional Description: [0] [1]
- ISS CSI2 REGS1 Registers: [2]

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Table 8-193. CSI2_CTX_IRQSTATUS_i

Address Offset	0x0000 0088 + (0x20 * i)	**Index**	i = 0 to 7
Physical Address	0x5200 1088 + (0x20 * i) 0x5200 1488 + (0x20 * i)		
Description	INTERRUPT STATUS REGISTER - Context This register regroups all the events related to Context.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							ECC_CORRECTION_IRQ	LINE_NUMBER_IRQ	FRAME_NUMBER_IRQ	CS_IRQ	RESERVED	LE_IRQ	LS_IRQ	FE_IRQ	FS_IRQ

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	ECC_CORRECTION_IRQ	Context - ECC has been used to do the correction of the only 1-bit error status (long packet only). 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
7	LINE_NUMBER_IRQ	Context - Line number reached status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
6	FRAME_NUMBER_IRQ	Context - Frame counter reached status 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
5	CS_IRQ	Context - Check-Sum mismatch status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
4	RESERVED		R	0
3	LE_IRQ	Context - Line end sync code detection status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
2	LS_IRQ	Context - Line start sync code detection status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
1	FE_IRQ	Context - Frame end sync code detection status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
0	FS_IRQ	Context - Frame start sync code detection status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0

Table 8-194. Register Call Summary for Register CSI2_CTX_IRQSTATUS_i

ISS Interfaces
- ISS CSI2 Functional Description: [0] [1] [2] [3]
- ISS CSI2 Programming Enable Video/Picture Acquisition: [4]
- ISS CSI2 REGS1 Registers: [5]

Table 8-195. CSI2_CTX_CTRL3_i

Address Offset	0x0000 008C + (0x20 * i)	**Index**	i = 0 to 7
Physical Address	0x5200 108C + (0x20 * i) 0x5200 148C + (0x20 * i)		
Description	CONTROL REGISTER - Context This register controls the Context. This register is shadowed: modifications are taken into account after the next FSC sync code.		
Type	RW		

31 30	29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
RESERVED		ALPHA	LINE_NUMBER	

Bits	Field Name	Description	Type	Reset
31:30	RESERVED		R	0x0
29:16	ALPHA	Alpha value for RGB888, RGB666 and RBG444.	RW	0x0000
15:0	LINE_NUMBER	Line number for the interrupt generation	RW	0x0000

Table 8-196. Register Call Summary for Register CSI2_CTX_CTRL3_i

ISS Interfaces
- ISS CSI2 Protocol and Data Format: [0] [1] [2]
- ISS CSI2 Functional Description: [3]
- ISS CSI2 Programming Enable Video/Picture Acquisition: [4]
- ISS CSI2 Programming a Periodic Event During Frame Acquisition: [5]
- ISS CSI2 REGS1 Registers: [6]

8.2.5.5.3 ISS CSI2 REGS2 Registers

8.2.5.5.3.1 ISS CSI2 REGS2 Register Summary

Table 8-197 summarizes the CSI2 REGS2 registers.

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Table 8-197. ISS CSI2 REGS2 Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	ISS_CSI2_A_REGS2 Base Address	ISS_CSI2_B_REGS2 Base Address
CSI2_CTX_TRANSCODEH_i [1]	RW	32	0x0000 0000 + (0x8 * i)	0x5200 11C0 + (0x8 * i)	0x5200 15C0 + (0x8 * i)
CSI2_CTX_TRANSCODEV_i [1]	RW	32	0x0000 0004 + (0x8 * i)	0x5200 11C4 + (0x8 * i)	0x5200 15C4 + (0x8 * i)

(1) i = 0 to 7

8.2.5.5.3.2 ISS CSI2 REGS2 Register Description

and describe the CSI2 REGS2 registers.

Table 8-198. CSI2_CTX_TRANSCODEH_i

Address Offset	0x0000 0000 + (0x8 * i)	**Index**	i = 0 to 7
Physical Address	0x5200 11C0 + (0x8 * i) 0x5200 15C0 + (0x8 * i)		
Description	Transcode configuration register: defines horizontal frame cropping		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								HCOUNT								RESERVED								HSKIP							

Bits	Field Name	Description	Type	Reset
31:29	RESERVED		R	0x0
28:16	HCOUNT	Pixels to output per line when the values is between 1 and 8191. Pixels HSKIP-WIDTH pixels are output when HCOUNT=0. WIDTH corresponds to the image width provided by the sensor.	RW	0x0000
15:13	RESERVED		R	0x0
12:0	HSKIP	Pixel to skip horizontally. Valid values: 0-8191	RW	0x0000

Table 8-199. Register Call Summary for Register CSI2_CTX_TRANSCODEH_i

ISS Interfaces

- ISS CSI2 Functional Description: [0] [1] [2] [3]
- ISS CSI2 REGS2 Registers: [4]

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Table 8-200. CSI2_CTX_TRANSCODEV_i

Address Offset	0x0000 0004 + (0x8 * i)	**Index**	i = 0 to 7
Physical Address	0x5200 11C4 + (0x8 * i) 0x5200 15C4 + (0x8 * i)		
Description	Transcode configuration register: defines vertical frame cropping		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								VCOUNT								RESERVED								VSKIP							

Bits	Field Name	Description	Type	Reset
31:29	RESERVED		R	0x0
28:16	VCOUNT	Lines to output per frame when the values is between 1 and 8191. Pixels VSKIP-HEIGHT pixels are output when VCOUNT=0. HEIGHT corresponds to the image height provided by the sensor.	RW	0x0000
15:13	RESERVED		R	0x0
12:0	VSKIP	Pixel to skip vertically Valid values: 0-8191	RW	0x0000

Table 8-201. Register Call Summary for Register CSI2_CTX_TRANSCODEV_i

ISS Interfaces

- ISS CSI2 Functional Description: [0] [1] [2]
- ISS CSI2 REGS2 Registers: [3]

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8.2.6 ISS TCTRL

8.2.6.1 ISS TCTRL Environment

There are no particular environment attributes. See Section 8.2.2, *ISS Interfaces Environment*.

8.2.6.2 ISS TCTRL Integration

Figure 8-77 shows the integration of the TCTRL.

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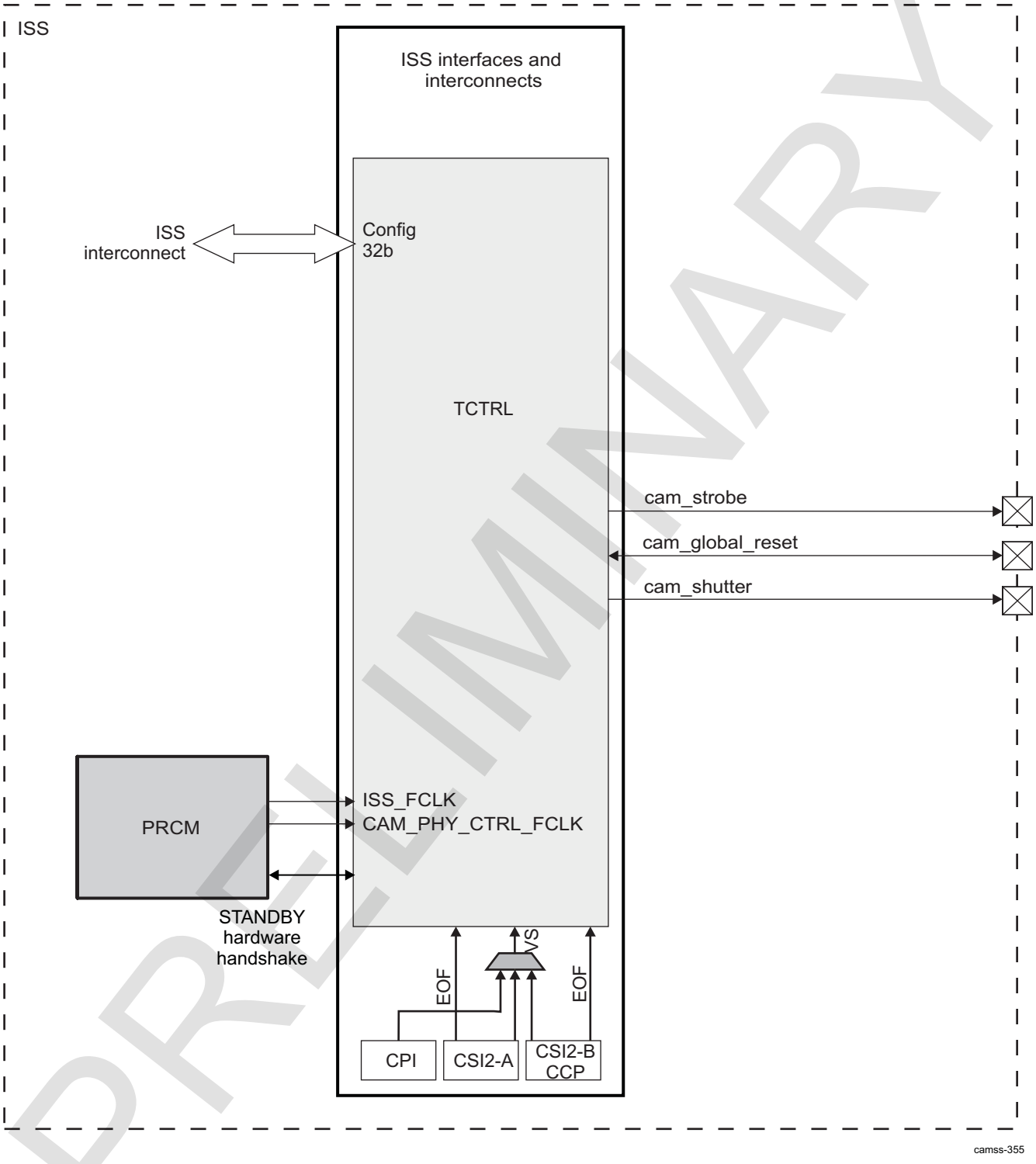
Figure 8-77. ISS TCTRL Integration



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For information about the power domain, clocks, reset, and hardware requests, see Section 8.1.2.4, *ISS Power Management*.

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8.2.6.3 ISS TCTRL Functional Description

8.2.6.3.1 ISS TCTRL Features

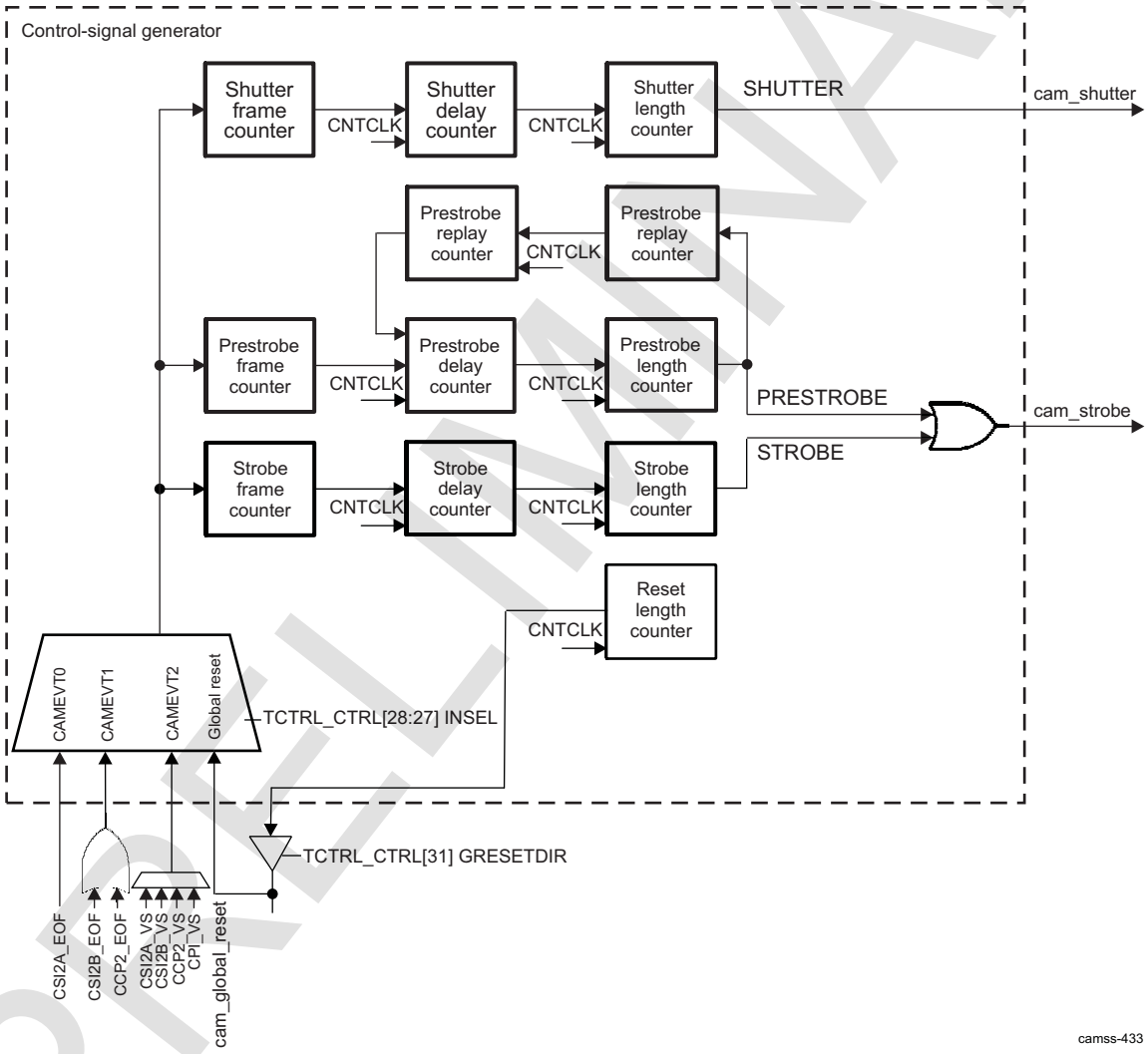
The TCTRL generates the control signals (cam_strobe and cam_shutter) for the flash prestrobe, flash strobe, and mechanical shutters.

The TCTRL includes a timing generator and a control-signal generator.

8.2.6.3.2 ISS TCTRL Control-Signal Generator

The control-signal generator generates the prestrobe, strobe, and shutter signals: cam_strobe and cam_shutter. Figure 8-78 shows the principle of control-signal generation.

Figure 8-78. TCTRL Control-Signal Generation



The control-signal generator gathers precise timings for the cam_strobe and cam_shutter signals, to assert and deassert the signals at known times. The timing control-signal generator can be synchronized on the vertical synchronization signal coming from the CSI2-A, CSI2-B, CCP2, Parallel interface (CPI), or on an externally generated cam_global_reset signal.

A multiplexer controls which of the CSI2-A, CSI2-B, CCP2, or Parallel interfaces drives control-signal generation. This multiplexer can also select the externally generated cam_global_reset signal as the trigger event. The TCTRL_CTRL[31] GRESETDIR bit defines the direction of cam_global_reset.

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- The externally generated cam_global_reset is used as a trigger when TCTRL_CTRL[31] GRESETDIR = 0 and TCTRL_CTRL[28:27] INSEL = 3.
- The internally generated cam_global_reset is used as a trigger when TCTRL_CTRL[31] GRESETDIR = 1 and TCTRL_CTRL[28:27] INSEL = 3.

The cam_global_reset signal can also be generated internally by the control-signal generator under software control. In this case, the prestrobe and shutter signals are synchronized on internally generated cam_global_reset . The multiplexer controls whether control-signal generation must be triggered by the internal or external cam_global_reset.

The prestrobe-, strobe-, and shutter-control signals can be individually enabled at any time. These signals must not be disabled by software.

The clock divider generates the CNTCLK clock based on the functional clock. The clock divider is programmable. Table 8-202 lists the possible frequencies as a function of the divisor values.

Table 8-202. ISS TCTRL Control-Signal Generator: CNTCLK Frequencies

Divisor Value TCTRL_CTRL[18:10] DIVC	CNTCLK Clock	CNTCLK Precision (ns)
0 (default)	Clock gated. No clock.	N/A
1	200 MHz	5
2	100 MHz	10
3	66,667 MHz	15
4	50 MHz	20
...	...	...
510	0.392 MHz	2550
511	0.391 MHz	2555

There are three counters per control signal, for a total of nine counters. Each counter is programmable.

- The frame counter is decreased each time a full new frame is received.
  - A new frame is detected by the TCTRL module when CAMEVTx is received.
  - The frame counter determines how many whole frames must be ignored before the delay counter is triggered. The frame counters can be set to 0 to bypass the frame counters.
- The delay counter determines the control-signal activation delay. The counter is decreased at every CNTCLK clock cycle. When the counter reaches 0, the control signal is asserted. If the delay counter is set to 0, the control signal is asserted immediately.
- The activation-length counter determines the length of control-signal assertion. The counter is decreased at every CNTCLK clock cycle. When the counter reaches 0, the signal is deasserted and the control-signal enable bit is disabled. If the activation length is set to 0, the control signal is not asserted and the control-signal enable bit is disabled.

The polarity of the following signals can be individually selected:

- TCTRL_CTRL[26] STRBPSTRBPOL for the prestrobe and strobe signals
- TCTRL_CTRL[24] SHUTPOL for the shutter signal
- TCTRL_CTRL[30] GRESETPOL for cam_global_reset

Software can trigger the generation of cam_global_reset to the camera module. The length of signal-activation is programmable. The counter is decreased at every CNTCLK clock cycle. When the counter reaches 0, the signal is deasserted and the global reset enable bit is disabled (the TCTRL_CTRL[29] GRESETEN bit). If the activation length is set to 0, the control signal is not asserted and the control-signal enable bit is disabled. The polarity of cam_global_reset can be selected (the TCTRL_CTRL[30] GRESETPOL bit).

Figure 8-79 shows the use of cam_global_reset set as an input or output signal. cam_global_reset is asynchronous, edge-sensitive, and asserted for at least one interconnect clock cycle.

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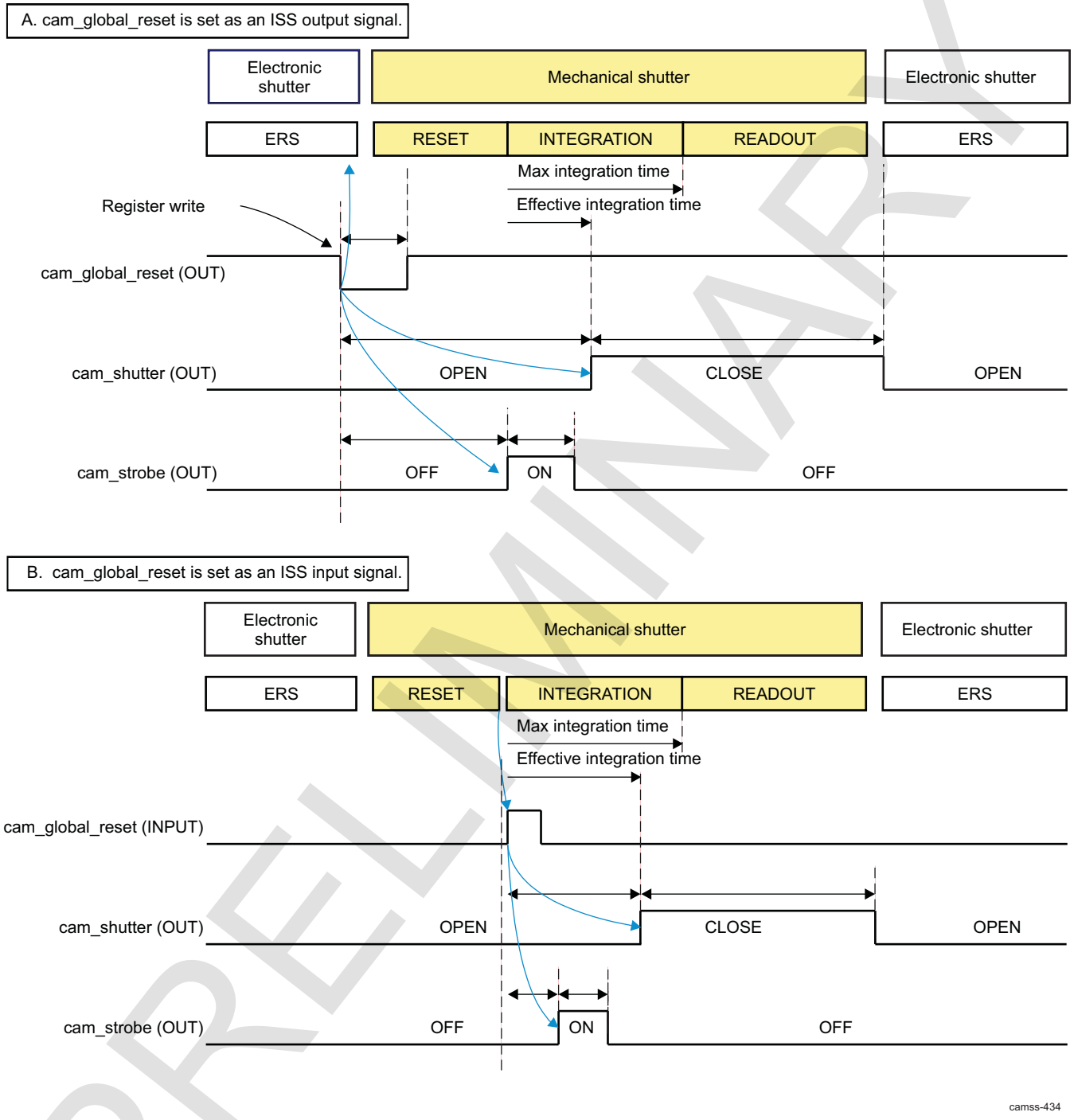
Figure 8-79. ISS TCTRL Use of cam_global_reset With Global Reset Release Camera Modules



There are two types of shutter mechanisms: mechanical and electronic. A mechanical shutter is used only for high-resolution sensors. The three control signals (cam_global_reset, cam_shutter, and cam_strobe) are useful with a mechanical shutter. High frame rates can be achieved only with an electronic shutter. When an electronic shutter is used, none of the three control signals is used.

- Mechanical shutter mechanism:
  - Reset: All pixels of the sensor are reset to their black value. When the sensor has a global reset feature, the mechanical shutter can be open during reset.
  - Integration: The light received by the sensor is transformed into electrical charges that are stored inside pixels. At the end of the integration time, the shutter must be closed. Exposure time is

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defined by the time between reset release and shutter close.

– Readout: The charges accumulated in pixels are converted to digital values that are sent to the camera receiver.

- Electronic rolling shutter (ERS) mechanism:
  – Each line of the sensor is reset separately and read after a fixed amount of time. Exposure time is defined by the time between reset and read.

8.2.6.4 ISS TCTRL Programming Model

The following settings must be done before enabling the TCTRL.

8.2.6.4.1 ISS TCTRL Camera-Control Signal Generator

Two configurations apply:

- First configuration: The control signals are based on the vertical synchronization information coming from the camera module or from externally generated cam_global_reset.
- Second configuration: The control signals are based on internally generated cam_global_reset.

8.2.6.4.1.1 ISS TCTRL Vertical Sync-Based Control-Signal Generation or Externally Generated cam_global_reset

To enable control-signal generation in the first configuration, follow the procedure listed in Table 8-203.

Table 8-203. ISS TCTRL Enabling the Control-Signal Generation in First Configuration

Step	Bit Field	Value
Select the input that triggers the control signals. The trigger signal can come from the CSI2-A, CSI2-B/CCP2 interface, Parallel interface (CPI) or the externally generated cam_global_reset signal.	TCTRL_CTRL[28:27] INSEL	0x0: CSI2A 0x1: CSI2B or CCP2 0x2: VS signal 0x3: Global reset
Set the global reset as input signal. Writes to the TCTRL_CTRL[29] GRESETEN bit do not trigger the CAM_STROBE and CAM_SHUTTER signals and do not generate the CAM_GLOBAL_RESET signal.	TCTRL_CTRL[31] GRESETDIR	0x0
The following bits are cleared automatically to 0 after the signal assertion:	• TCTRL_CTRL[21] SHUTEN • TCTRL_CTRL[22] PSTRBEN • TCTRL_CTRL[23] STRBEN	
Set the polarity of the SHUTTER, STROBE/PRESTROBE, and cam_global_reset signals.	• TCTRL_CTRL[24] SHUTPOL • TCTRL_CTRL[26] STRBPSTRBPOL • TCTRL_CTRL[30] GRESETPOL	
Set the clock divisor value, which generates the CNTCLK clock The clock is set by CNTCLK = ISS_FCLK/TCTRL_CTRL[18:10] DIVC.	TCTRL_CTRL[18:10] DIVC	0x0: Disable CNTCLK 0 to 511: Divider
Set the frame counters.	• TCTRL_FRAME[5:0] SHUT • TCTRL_FRAME[11:6] PSTRB • TCTRL_FRAME[17:12] STRB	0: TCTRL does not delay any frame in input. 1 to 63
Set the delay counters.	• TCTRL_SHUT_DELAY • TCTRL_PSTRB_DELAY • TCTRL_STRB_DELAY	The possible values are 0 to 2^{25} 1 cycles. The cycles are at the CNTCLK clock frequency. The maximum signal duration is (2^{25} 1) x 511/200 MHz = 85.73157376 s (TCTRL_CTRL[18:10] DIVC = 511).

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Table 8-203. ISS TCTRL Enabling the Control-Signal Generation in First Configuration (continued)

Step	Bit Field	Value
Set the signal durations.	• TCTRL_SHUT_LENGTH • TCTRL_PSTRB_LENGTH • TCTRL_STRB_LENGTH	The possible values are 0 to 2^{24} 1 cycles. The cycles are at the CNTCLK clock frequency. The maximum signal duration for a 200 MHz input clock is (2^{24} 1) x 511/200 MHz = 42.865784325 s (TCTRL_CTRL.DIVC = 511).
Enable the SHUTTER signal.	TCTRL_CTRL[21] SHUTEN	0x1
Enable the PRESTROBE signal.	TCTRL_CTRL[22] PSTRBEN	0x1
Enable the STROBE signal.	TCTRL_CTRL[23] STRBEN	0x1

8.2.6.4.1.2 ISS TCTRL Internally Generated cam_global_reset-Based Control-Signal Generation

To enable control-signal generation in the second configuration, follow the procedure listed in Table 8-204.

Table 8-204. ISS TCTRL Enabling the Control-Signal Generation in Second Configuration

Step	Bit Field	Value
Select the input to global reset, to loop back the internally generated GLOBAL_RESET. Vertical synchronization events do not trigger the CAM_STROBE and CAM_SHUTTER signals.	TCTRL_CTRL[28:27] INSEL	0x3: Global reset
Set the global reset as output signal.	TCTRL_CTRL[31] GRESETDIR	0x1
The following bits are cleared automatically to 0 after the signal assertion:	• TCTRL_CTRL[21] SHUTEN • TCTRL_CTRL[22] PSTRBEN • TCTRL_CTRL[23] STRBEN • TCTRL_CTRL[29] GRESETEN	0x0
Set the polarity of the SHUTTER, STROBE/PRESTROBE, and cam_global_reset signals.	• TCTRL_CTRL[24] SHUTPOL • TCTRL_CTRL[26] STRBPSTRBPOL • TCTRL_CTRL[30] GRESETPOL	
Set the clock divisor value, which generates the CNTCLK clock The clock is set by CNTCLK = ISS_FCLK/TCTRL_CTRL[18:10] DIVC.	TCTRL_CTRL[18:10] DIVC	0x0: Disable CNTCLK 0 to 511: Divider
Set the frame counters.	• TCTRL_FRAME[5:0] SHUT • TCTRL_FRAME[11:6] PSTRB • TCTRL_FRAME[17:12] STRB	0: TCTRL does not delay any frame in input. 1 to 63
Set the delay counters.	• TCTRL_SHUT_DELAY • TCTRL_PSTRB_DELAY • TCTRL_STRB_DELAY	The possible values are 0 to 2^{25} 1 cycles. The cycles are at the CNTCLK clock frequency. The maximum signal duration is (2^{25} 1) x 511/200 MHz = 85.73157376 s (TCTRL_CTRL[18:10] DIVC = 511).

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Table 8-204. ISS TCTRL Enabling the Control-Signal Generation in Second Configuration (continued)

Step	Bit Field	Value
Set the signal durations.	• TCTRL_SHUT_LENGTH • TCTRL_PSTRB_LENGTH • TCTRL_STRB_LENGTH	The possible values are 0 to 2^{24} 1 cycles. The cycles are at the CNTCLK clock frequency. The maximum signal duration for a 200 MHz input clock is (2^{24} 1) x 511/200 MHz = 42.865784325 s (TCTRL_CTRL.DIVC = 511).
Set the cam_global_reset assertion time.	TCTRL_GRESET_LENGTH	The possible values are 0 to 2^{24} 1 cycles. The cycles are at the CNTCLK clock frequency. The maximum signal duration for a 200 MHz input clock is (2^{24} 1) x 511/200 MHz = 42.865784325 s (TCTRL_CTRL.DIVC = 511).
Enable the SHUTTER signal.	TCTRL_CTRL[21] SHUTEN	0x1
Enable the PRESTROBE signal.	TCTRL_CTRL[22] PSTRBEN	0x1
Enable the STROBE signal.	TCTRL_CTRL[23] STRBEN	0x1
Enable the cam_global_reset control-signal generation.	TCTRL_CTRL[29] GRESETEN	0x1

NOTE: Setting the following bits to 1 simultaneously leads to unpredictable behavior:

- TCTRL_CTRL[21] SHUTEN
- TCTRL_CTRL[22] PSTRBEN
- TCTRL_CTRL[23] STRBEN
- TCTRL_CTRL [29] GRESETEN

The following bits must be set before TCTRL_CTRL[29] GRESETEN is enabled:

- TCTRL_CTRL[21] SHUTEN
- TCTRL_CTRL[22] PSTRBEN
- TCTRL_CTRL[23] STRBEN

8.2.6.4.1.3 ISS TCTRL STROBE and PRESTROBE Signal Generation for Red-Eye Removal

The STROBE and PRESTROBE signal generation enables a strobe flash for red-eye removal. The process is shown in Figure 8-80. The dotted line corresponds to known timings from which the delay counters start decreasing: cam_global_reset event.

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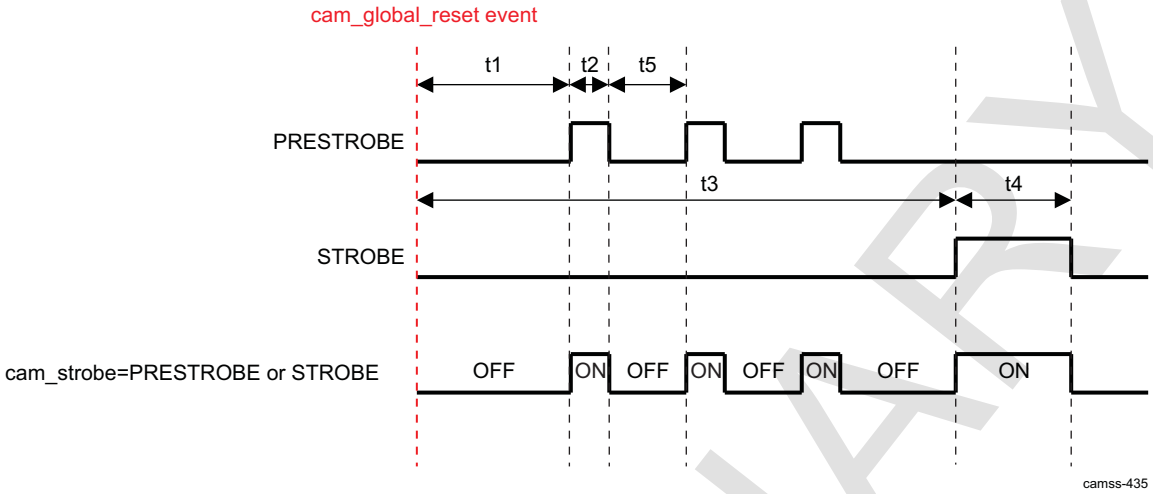
Figure 8-80. cam_strobe Signal-Generation for Red-Eye Removal



- t1: Set by the TCTRL_PSTRB_DELAY register
- t2: Set by the TCTRL_PSTRB_LENGTH register
- t5: Set by the TCTRL_PSTRB_REPLAY[24:0] DELAY bit field. The number of times the pulse is repeated is controlled by the TCTRL_PSTRB_REPLAY[31:25] COUNTER bit field.

  In the previous example, TCTRL_PSTRB_REPLAY[31:25] COUNTER = 2.
  - The possible delay values are 0 to 2^{25} 1 cycle. The cycles are at the CNTCLK clock frequency. The maximum signal duration is (2^{25} 1) x 511/200 MHz = 85.73157376 s (TCTRL_CTRL[18:11] DIVC = 511).
  - The possible count values are 0 to 127 additional pulses.
- t3: Set by the TCTRL_STRB_DELAY register
- t4: Set by the TCTRL_STRB_LENGTH register

8.2.6.5 ISS TCTRL Register Manual

8.2.6.5.1 ISS TCTRL Instance Summary

Table 8-205 summarizes the TCTRL instance.

Table 8-205. ISS TCTRL Instance Summary

Module Name	L3 Base Address	Size
ISS_TCTRL	0x5200 0400	256 bytes

8.2.6.5.2 ISS TCTRL Registers

8.2.6.5.2.1 ISS TCTRL Register Summary

Table 8-206 summarizes the TCTRL registers.

Table 8-206. ISS TCTRL Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	ISS_TCTRL Base Address
TCTRL_REVISION	R	32	0x0000 0000	0x5200 0400
TCTRL_SYSCONFIG	RW	32	0x0000 0004	0x5200 0404
TCTRL_SYSSTATUS	R	32	0x0000 0008	0x5200 0408
TCTRL_STRB_LENGTH	RW	32	0x0000 0010	0x5200 0410

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Table 8-206. ISS TCTRL Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	ISS_TCTRL Base Address
TCTRL_PSTRB_LENGTH	RW	32	0x0000 0014	0x5200 0414
TCTRL_SHUT_LENGTH	RW	32	0x0000 0018	0x5200 0418
TCTRL_GRESET_LENGTH	RW	32	0x0000 001C	0x5200 041C
TCTRL_STRB_DELAY	RW	32	0x0000 0020	0x5200 0420
TCTRL_PSTRB_DELAY	RW	32	0x0000 0024	0x5200 0424
TCTRL_SHUT_DELAY	RW	32	0x0000 0028	0x5200 0428
TCTRL_CTRL	RW	32	0x0000 0030	0x5200 0430
TCTRL_PSTRB_REPLAY	RW	32	0x0000 0034	0x5200 0434
TCTRL_FRAME	RW	32	0x0000 0038	0x5200 0438

8.2.6.5.2.2 ISS TCTRL Register Description

Table 8-207 through Table 8-232 describe the TCTRL registers.

Table 8-207. TCTRL_REVISION

Address Offset	0x0000 0000		
Physical Address	0x5200 0400	**Instance**	ISS_TCTRL
Description	IP Revision Identifier (X.Y.R) Used by software to track features, bugs, and compatibility		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP revision	R	See(1)

(1) TI internal data

Table 8-208. Register Call Summary for Register TCTRL_REVISION

ISS Interfaces

- ISS TCTRL Registers: [0]

Table 8-209. TCTRL_SYSCONFIG

Address Offset	0x0000 0004		
Physical Address	0x5200 0404	**Instance**	ISS_TCTRL
Description	OCP-SOCKET SYSTEM CONFIGURATION REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														SOFT_RESET	AUTO_IDLE

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Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	SOFT_RESET	Software reset. Set the bit to 1 to trigger the module reset. The bit is automatically reset be the hardware. During reads return 0. 0x0: Normal mode. 0x1: The module is reset.	RW	0
0	AUTO_IDLE	Internal OCP and functional clock gating strategy 0x0: OCP and functional clocks are free-running 0x1: Automatic clock gating strategy is applied, based on the OCP interface activity for interface clock and on the functional activity for functional clocks.	RW	1

Table 8-210. Register Call Summary for Register TCTRL_SYSCONFIG

ISS Interfaces
- ISS TCTRL Registers: [0]

Table 8-211. TCTRL_SYSSTATUS

Address Offset	0x0000 0008		
Physical Address	0x5200 0408	**Instance**	ISS_TCTRL
Description	OCP-SOCKET SYSTEM STATUS REGISTER		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															RESET_DONE

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	RESET_DONE	Internal reset monitoring Read 0x1: Reset completed. Read 0x0: Internal module reset is ongoing.	R	0

Table 8-212. Register Call Summary for Register TCTRL_SYSSTATUS

ISS Interfaces
- ISS TCTRL Registers: [0]

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Table 8-213. TCTRL_STRB_LENGTH

Address Offset	0x0000 0010		
Physical Address	0x5200 0410	**Instance**	ISS_TCTRL
Description	TIMING CONTROL - STROBE LENGTH REGISTER This register is used by the TIMING CTRL module to generate the STROBE signal.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								LENGTH																							

Bits	Field Name	Description	Type	Reset
31:24	RESERVED		R	0x00
23:0	LENGTH	Sets the length of the CAM_STROBE signal assertion in cycles of the CNTCLK clock. The CNTCLK frequency is generated with the TCTRL_CTRL.DIVC bit field. After signal assertion, the TCTRL_CTRL.STRBEN bit is automatically cleared. The possible values are 0 to 2^{24}-1 cycles.	RW	0x000000

Table 8-214. Register Call Summary for Register TCTRL_STRB_LENGTH

ISS Interfaces

- ISS TCTRL Camera-Control Signal Generator: [0] [1] [2]
- ISS TCTRL Registers: [3] [4]

Table 8-215. TCTRL_PSTRB_LENGTH

Address Offset	0x0000 0014		
Physical Address	0x5200 0414	**Instance**	ISS_TCTRL
Description	TIMING CONTROL - PRESTROBE LENGTH REGISTER This register is used by the TIMING CTRL module to generate the PRESTROBE signal.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								LENGTH																							

Bits	Field Name	Description	Type	Reset
31:24	RESERVED		R	0x00
23:0	LENGTH	Sets the length of the CAM_PRESTROBE signal assertion in cycles of the CNTCLK clock. The CNTCLK frequency is generated with the TCTRL_CTRL.DIVC bit field. After signal assertion, the TCTRL_CTRL.PSTRBEN bit is automatically cleared. The possible values are 0 to 2^{24}-1 cycles.	RW	0x000000

Table 8-216. Register Call Summary for Register TCTRL_PSTRB_LENGTH

ISS Interfaces

- ISS TCTRL Camera-Control Signal Generator: [0] [1] [2]
- ISS TCTRL Registers: [3] [4] [5] [6] [7]

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Table 8-217. TCTRL_SHUT_LENGTH

Address Offset	0x0000 0018		
Physical Address	0x5200 0418	**Instance**	ISS_TCTRL
Description	TIMING CONTROL - SHUTTER LENGTH REGISTER This register is used by the TIMING CTRL module to generate the SHUTTER signal.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								LENGTH																							

Bits	Field Name	Description	Type	Reset
31:24	RESERVED		R	0x00
23:0	LENGTH	Sets the length of the CAM_SHUTTER signal assertion in cycles of the CNTCLK clock. The CNTCLK frequency is generated with the TCTRL_CTRL.DIVC bit field. After signal assertion, the TCTRL_CTRL.SHUTEN bit is automatically cleared. The possible values are 0 to 2^{24}-1 cycles.	RW	0x000000

Table 8-218. Register Call Summary for Register TCTRL_SHUT_LENGTH

ISS Interfaces

- ISS TCTRL Camera-Control Signal Generator: [0] [1]
- ISS TCTRL Registers: [2] [3]

Table 8-219. TCTRL_GRESET_LENGTH

Address Offset	0x0000 001C		
Physical Address	0x5200 041C	**Instance**	ISS_TCTRL
Description	TIMING CONTROL - GLOBAL SHUTTER LENGTH REGISTER This register is used by the TIMING CTRL module to generate the CAM.GRESET signal.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								LENGTH																							

Bits	Field Name	Description	Type	Reset
31:24	RESERVED		R	0x00
23:0	LENGTH	Sets the length of the CAM_GLOBAL_RESET signal assertion in cycles of the CNTCLK clock. The CNTCLK frequency is generated with the TCTRL_CTRL.DIVC bit field. After signal assertion, the TCTRL_CTRL.GRESETEN bit is automatically cleared. The possible values are 0 to 2^{24}-1 cycles. The polarity of the CAM_GLOBAL_RESET signal is set by the TCTRL_CTRL.GRESETPOL bit.	RW	0x000000

Table 8-220. Register Call Summary for Register TCTRL_GRESET_LENGTH

ISS Interfaces

- ISS TCTRL Camera-Control Signal Generator: [0]
- ISS TCTRL Registers: [1] [2]

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Table 8-221. TCTRL_STRB_DELAY

Address Offset	0x0000 0020		
Physical Address	0x5200 0420	**Instance**	ISS_TCTRL
Description	TIMING CONTROL - STROBE DELAY REGISTER This register is used by the TIMING CTRL module to generate the STROBE signal.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								DELAY																							

Bits	Field Name	Description	Type	Reset
31:25	RESERVED		R	0x00
24:0	DELAY	Sets the delay for the CAM_STROBE signal assertion in cycles of the CNTCLK clock. The CNTCLK frequency is generated with the TCTRL_CTRL.DIVC bit field. The possible values are 0 to 2^{25}-1 cycles.	RW	0x0000000

Table 8-222. Register Call Summary for Register TCTRL_STRB_DELAY

ISS Interfaces

- ISS TCTRL Camera-Control Signal Generator: [0] [1] [2]
- ISS TCTRL Registers: [3] [4]

Table 8-223. TCTRL_PSTRB_DELAY

Address Offset	0x0000 0024		
Physical Address	0x5200 0424	**Instance**	ISS_TCTRL
Description	TIMING CONTROL - PRE STROBE DELAY REGISTER This register is used by the TIMING CTRL module to generate the PRESTROBE signal.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								DELAY																							

Bits	Field Name	Description	Type	Reset
31:25	RESERVED		R	0x00
24:0	DELAY	Sets the delay for the CAM_PSTROBE signal assertion in cycles of the CNTCLK clock. The CNTCLK frequency is generated with the TCTRL_CTRL.DIVC bit field. The possible values are 0 to 2^{25}-1 cycles.	RW	0x0000000

Table 8-224. Register Call Summary for Register TCTRL_PSTRB_DELAY

ISS Interfaces

- ISS TCTRL Camera-Control Signal Generator: [0] [1] [2]
- ISS TCTRL Registers: [3] [4] [5]

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Table 8-225. TCTRL_SHUT_DELAY

Address Offset	0x0000 0028		
Physical Address	0x5200 0428	**Instance**	ISS_TCTRL
Description	TIMING CONTROL - SHUTTER DELAY REGISTER This register is used by the TIMING CTRL module to generate the SHUTTER signal.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								DELAY																							

Bits	Field Name	Description	Type	Reset
31:25	RESERVED		R	0x00
24:0	DELAY	Sets the delay for the CAM_SHUTTER signal assertion in cycles of the CNTCLK clock. The CNTCLK frequency is generated with the TCTRL_CTRL.DIVC bit field. The possible values are 0 to 2^{25}-1 cycles.	RW	0x0000000

Table 8-226. Register Call Summary for Register TCTRL_SHUT_DELAY

ISS Interfaces

- ISS TCTRL Camera-Control Signal Generator: [0] [1]
- ISS TCTRL Registers: [2] [3]

Table 8-227. TCTRL_CTRL

Address Offset	0x0000 0030		
Physical Address	0x5200 0430	**Instance**	ISS_TCTRL
Description	TIMING CONTROL - CONTROL REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GRESETDIR	GRESETPOL	GRESETEN	INSEL		STRBPSTRBPOL	RESERVED	SHUTPOL	STRBEN	PSTRBEN	SHUTEN	RESERVED	DIVC												RESERVED							

Bits	Field Name	Description	Type	Reset
31	GRESETDIR	Sets the direction of the GLOBAL_RESET signal. 0x0: INPUT – GLOBAL_RESET is an input to the TIMING CONTROL module. GLOBAL_RESET is externally generated. 0x1: OUTPUT – GLOBAL_RESET is an output of the TIMING CONTROL module. GLOBAL_RESET is internally generated. If GRESETEN is set to 1, the internally generated GLOBAL_RESET will trigger the generation of the PRESTROBE, STROBE and SHUTTER signals. The frame counters are ignored.	RW	0
30	GRESETPOL	Sets the polarity of the global reset signal: CAM_GLOBAL_RESET. It applies whatever the direction of the GLOBAL_RESET signal: input or output. 0x0: active high 0x1: active low	RW	0

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Bits	Field Name	Description	Type	Reset
29	GRESETEN	Triggers the generation of the CAM_GLOBAL_RESET signal. The signal is asserted immediately. If enabled, the CAM_GLOBAL_RESET signal will be asserted for TCTRL_GRESET_LENGTH cycles. After the signal assertion, the enable bit is automatically cleared to 0. The polarity of the GLOBAL_RESET signal is set with TCTRL_CTRL.GRESETPOL. Enabling this bit triggers the generation of the CAM_SHUTTER and CAM_STROBE signals (if previously enabled). The frame counters shall be set to 0 when this bit is set to 1 and GRESETDIR is set a OUTPUT.	RW	0
28:27	INSEL	Sets the mode that will trigger the SHUTTER, PRESTROBE and STROBE signals. 0x0: Synchronization event from camera 0 0x1: Synchronization event from camera 1 0x3: GRESET – The CAM_GLOBAL_RESET input signal will trigger the SHUTTER, PRESTROBE and STROBE signals. In this mode, there are no frame counters. The delay counters start decrementing as soon as the GLOBAL_RESET signal is asserted. The polarity of the GLOBAL_RESET signal is set with TCTRL_CTRL.GRESETPOL. 0x2: Synchronization event from camera 2 (serial interfaces muxed with the camera Parallel interface (CPI))	RW	0x0
26	STRBPSTRBPOL	Sets the polarity of the strobe and prestrobe signals. 0x0: Active high 0x1: Active low	RW	0
25	RESERVED		R	0
24	SHUTPOL	Sets the polarity of the mechanical shutter signal: CAM_SHUTTER 0x0: Active high 0x1: Active low	RW	0
23	STRBEN	Flash strobe signal enable. If enabled, the STROBE signal will be asserted after TCTRL_FRAME.STRB frames have been received and a delay of TCTRL_STRB_DELAY cycles have passed. The STROBE signal is asserted for TCTRL_STRB_LENGTH cycles. After the signal assertion, the enable bit is automatically cleared to 0. This signal shall not be disabled by software.	RW	0
22	PSTRBEN	Flash prestrobe signal enable. If enabled, the PRESTROBE signal will be asserted after TCTRL_FRAME.PSTRB frames have been received and a delay of TCTRL_PSTRB_DELAY cycles have passed. The PRESTROBE signal is asserted for TCTRL_PSTRB_LENGTH cycles. After the signal assertion, the enable bit is automatically cleared to 0. This signal shall not be disabled by software.	RW	0
21	SHUTEN	Mechanical shutter signal enable. If enabled, the SHUTTER signal will be asserted after TCTRL_FRAME.SHUT frames have been received and a delay of TCTRL_SHUT_DELAY cycles have passed. The SHUTTER signal is asserted for TCTRL_SHUT_LENGTH cycles. After the signal assertion, the enable bit is automatically cleared to 0. This signal shall not be disabled by software.	RW	0
20:19	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
18:10	DIVC	Sets the clock divisor value for the CNTCLK clock generation based on the CLK input clock. CNTCLK is an internal clock used by the TIMING CTRL module counters. Usually, CNTCLK = CLK / DIVC, except for some particular values shown hereafter. 0x0: No clock. CNTCLK is gated.	RW	0x000
9:0	RESERVED		R	0x000

Table 8-228. Register Call Summary for Register TCTRL_CTRL

ISS Interfaces

- ISS TCTRL Control-Signal Generator: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10]
- ISS TCTRL Camera-Control Signal Generator: [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23] [24] [25] [26] [27] [28] [29] [30] [31] [32] [33] [34] [35] [36] [37] [38] [39] [40] [41] [42] [43] [44] [45] [46] [47] [48] [49] [50] [51] [52] [53]
- ISS TCTRL Registers: [54] [55] [56] [57] [58] [59] [60] [61] [62] [63] [64] [65] [66] [67] [68] [69]

Table 8-229. TCTRL_PSTRB_REPLAY

Address Offset	0x0000 0034		
Physical Address	0x5200 0434	**Instance**	ISS_TCTRL
Description	TIMING CONTROL - PRESTROBE REPLAY REGISTER This register is used by the TIMING CTRL module to generate the prestrobe signal.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNTER								DELAY																							

Bits	Field Name	Description	Type	Reset
31:25	COUNTER	Sets the number of PRESTROBE pulses after the original pulse. If this bit is set to 0, the PRESTROBE signal behavior is only controlled by TCTRL_FRAME.STRB, TCTRL_PSTRB_DELAY, and TCTRL_PSTRB_LENGTH. If TCTRL_PSTRB_LENGTH=0, there is no replay. This bit is useful when one wants to enable red-eye removal.	RW	0x00
24:0	DELAY	Sets the delay for the PRESTROBE signal reassertion in cycles of the CNTCLK clock. The CNTCLK frequency is generated with the TCTRL_CTRL.DIVC bit field. The possible values are 0 to 2^{25}-1 cycles. If TCTRL_PSTRB_LENGTH=0, there is no replay. This bit field shall not be set to 0 if the COUNTER is set to a value different of 0. This bit is useful when one wants to enable red-eye removal.	RW	0x0000000

Table 8-230. Register Call Summary for Register TCTRL_PSTRB_REPLAY

ISS Interfaces

- ISS TCTRL Camera-Control Signal Generator: [0] [1] [2]
- ISS TCTRL Registers: [3]

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Table 8-231. TCTRL_FRAME

Address Offset	0x0000 0038		
Physical Address	0x5200 0438	**Instance**	ISS_TCTRL
Description	TIMING CONTROL - FRAME REGISTER This register is used by the TIMING CTRL module to generate the SHUTTER, PRESTROBE, and STROBE signals.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																STRB								PSTRB							
																										SHUT					

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:12	STRB	Frame counter for the STROBE signal generation. From 0 to 63 frames. This bit field is ignored if TCTRL.INSEL=GRESET.	RW	0x00
11:6	PSTRB	Frame counter for the PRESTROBE signal generation. From 0 to 63 frames. This bit field is ignored if TCTRL.INSEL=GRESET.	RW	0x00
5:0	SHUT	Frame counter for the SHUTTER signal generation. From 0 to 63 frames. This bit field is ignored if TCTRL.INSEL=GRESET.	RW	0x00

Table 8-232. Register Call Summary for Register TCTRL_FRAME

ISS Interfaces

- ISS TCTRL Camera-Control Signal Generator: [0] [1] [2] [3] [4] [5]
- ISS TCTRL Registers: [6] [7] [8] [9] [10]

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8.2.7 ISS BTE

8.2.7.1 ISS BTE Environment

There are no particular environment attributes (see Section 8.2.2, *ISS Interfaces Environment*).

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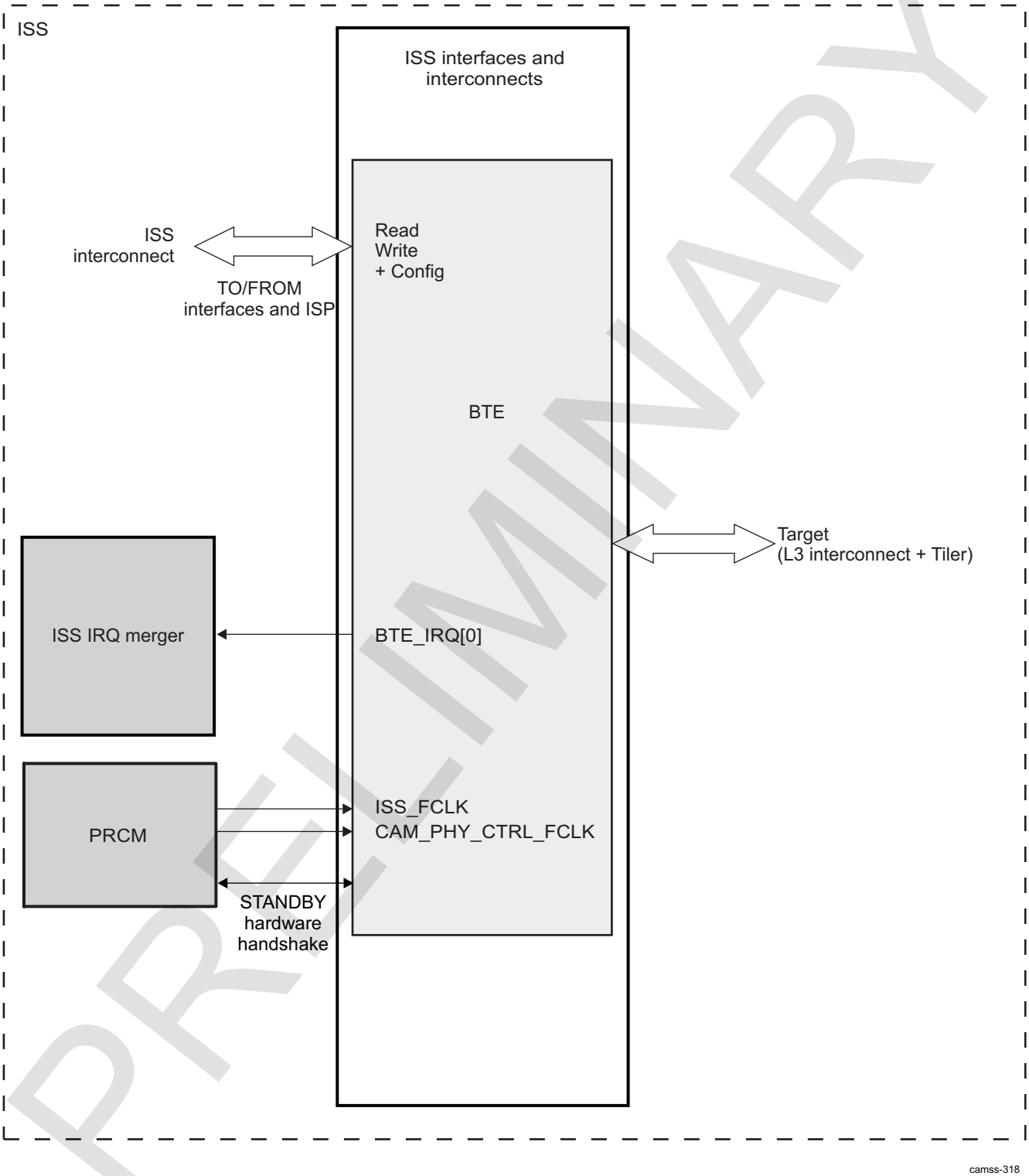
8.2.7.2 ISS BTE Integration

Figure 8-81. ISS BTE Integration



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For power domain, clocks, reset, and hardware requests, see Section 8.1.2.4, *ISS Power Management*.

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8.2.7.2.1 ISS BTE PRCM Interface

8.2.7.2.1.1 ISS BTE Power Management

8.2.7.2.1.1.1 ISS BTE PRCM Handshake

The BTE supports the IDLE protocol to flush outstanding transactions. When an IDLE request is received, the BTE:

- Completes ongoing requests on OCPI (request, data and response phases) and stalls the port (SCmdAccept = 0)
- Flushes all contexts (same behavior than when the BTE_CONTEXT_CTRL_i[2] FLUSH bit is set by software) when the BTE_CONTEXT_CTRL_i[11] AUTOFLUSH bit is set. Otherwise, no context flushing is triggered by an IDLE request.
- Completes ongoing requests on OCPO (request, data and response phases)
- Acknowledges the IDLE request.

8.2.7.3 ISS BTE Functional Description

8.2.7.3.1 ISS BTE Features

The BTE increases access efficiency of raster initiators to tiled SDRAM. In fact, the TILER expects 2D-bursts corresponding to a row or column of subtiles for maximal efficiency. For more information about SDRAM and TILER, see Section 15.2, *Dynamic Memory Manager*.

The BTE is connected between one or multiple raster initiators. It can translate reads and writes. For reads, BTE prefetches sufficient data from tiled memory to translate raster requests. For writes, BTE buffers raster requests until is has sufficient data to generate requests to tiled memory. The features of the BTE are:

- Interfaces:
  - 32-bit-wide configuration interface (OCPC)
  - 128-bit-wide slave data port (OCPI)
  - 128-bit-wide master data port (OCPO)
- Incrementing to 2D burst translation for read and writes:
  - Four contexts. A context is a virtual frame buffer attached to a data flow requiring translation.
  - One-shot and continuous mode
- Local memories for temporal storage:
  - Cannot use external memories for temporal data storage
- Transparent for accesses that do not require translation. Requests are forwarded from OCPI to OCPO without modification.
- Local buffer

8.2.7.3.2 ISS BTE Functional Description Details

The main tasks and capabilities of the BTE are:

- Forward OCP transactions that do not need translation.
- For OCP writes requiring translation:
  - Store data received from OCPI to local buffers.
  - Read data from local buffers and send it to OCPO.
- For OCP read requiring translation:
  - Store data received from OCPO to local buffers.
  - Read data from local buffers and send it to OCPI.
- BTE DMA capability

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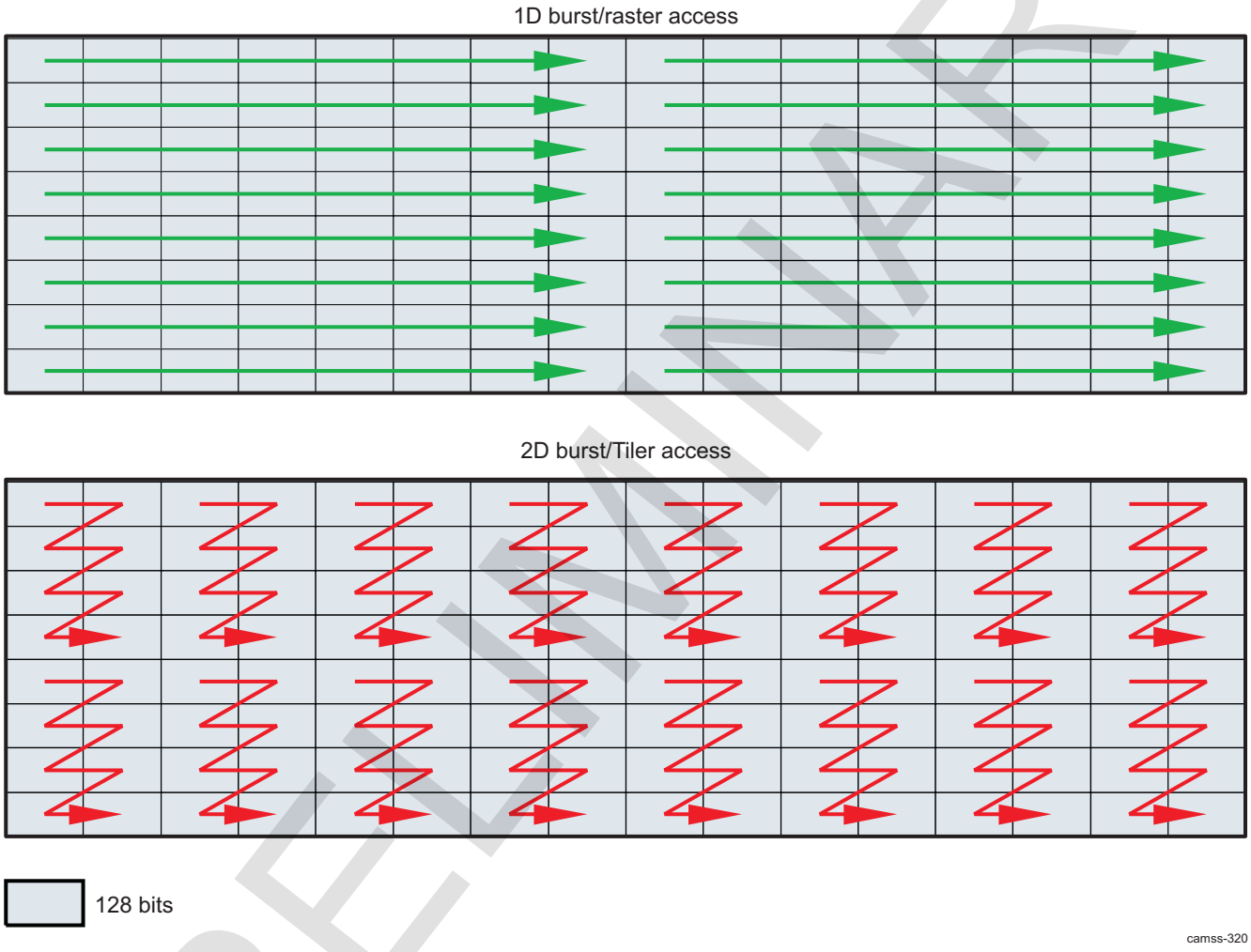
8.2.7.3.2.1 ISS BTE Burst Translation Principle

The BTE receives raster accesses from the OCPI port and generates TILER accesses on OCPO.

The BTE keeps track of the amount of data written into the local memories. For translated writes, 2D bursts are sent to OCPO when there is sufficient data in the local memory to generate TILER accesses. For translated reads, 2D burst are generated to fill the local memory with data that is returned when raster accesses are received on OCPI. Figure 8-82 shows the BTE burst translation principle.

Figure 8-82. ISS BTE Burst Translation Principle



In the following sections, three address spaces are described:

- Virtual: Corresponds to the translated address region on OCPI. Accesses performed to this address space are translated by the BTE. It can be seen as a 64KB x 8 k lines frame buffer. Locations in this space are expressed as byte addresses for OCP compliance. However, the access granularity is 128-bit (4 LSBs expected to be zeros). For more information about this space, see Section 8.2.7.3.2.2, *ISS BTE Virtual Address Space and Context Mapping*.
- Physical: Corresponds to the addresses used to access the physical buffer of the BTE. The physical space is addressed in 128-bit-wide words. However, this document refers to byte addresses to preserve homogeneity.
- Tiler: Corresponds to addresses used by translated accesses. Locations in this space are expressed as byte addresses for OCP compliance. However, the access granularity is 128-bit (4 LSBs expected to be zeros). For more information about this space, see Section 8.2.7.3.2.5, *ISS BTE TILER Space Accesses: 2D Burst Generation*.

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8.2.7.3.2.2 ISS BTE Virtual Address Space and Context Mapping

The location of the virtual space in the address map of OCPI is set by the BTE_CTRL[11:8] BASE bit field. It always occupies 64KB × 8k lines = 512MB. Software must map a virtual space into an unused region (a region, for example, that the ISS top level cannot access).

The virtual space is decomposed into contexts. A context corresponds to a 2D region in the virtual space that requires burst translation. It can also be seen as a virtual frame buffer.

Accesses to different contexts can be interleaved at OCP transaction level. OCP transactions spanning multiple contexts are not allowed.

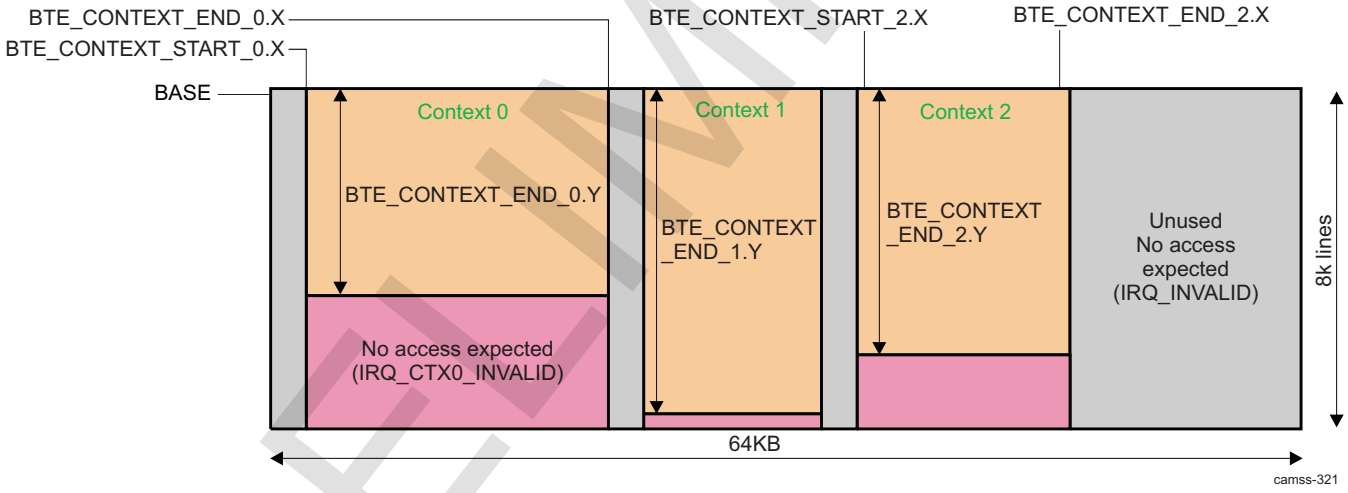
When the BTE receives an access from the OCPI port, it performs the following checks:

- If the access address is not between BASE 512MB and (BASE + 1) 512MB 1, it is handled as a transparent: request and data phases are simply forwarded to the OCPO without modification.
- If the access falls into the translated region:
  - If the access is a 2D burst, an IRQ_INVALID event is generated.
  - If the access does not map to an active context, an IRQ_INVALID event is generated. The BTE ignores bits [28:16] for this test.
  - Otherwise, context mapping is performed (see Figure 8-83).

Invalid requests are not forwarded to the OCPO.

Software must ensure that contexts do not overlap. The BTE hardware does not check for this condition. Wrong setup is likely to lead to corrupted data.

Figure 8-83. ISS BTE Context Mapping



The BTE internally keeps track of every context where the next access is expected. It internally maintains a 2D pointer, referred to as (SX_i, SY_i) in the remainder of this document. The expected byte address for an access into context x is:

ADDR = BTE_CTRL[11:8] BASE 512MB +
SX_i 16 bytes + SY_i 64KB

If an access to an unexpected location in a given context is received from OCPI, the BTE generates an IRQ_CTXx_INVALID event. The BTE provides a valid response on OCPI but does not store any data into the internal buffer. Subsequent accesses are handled normally: in other words, the BTE does not enter any specific error mode. When this happens, typically an initiator configuration is not aligned with the BTE context configuration.

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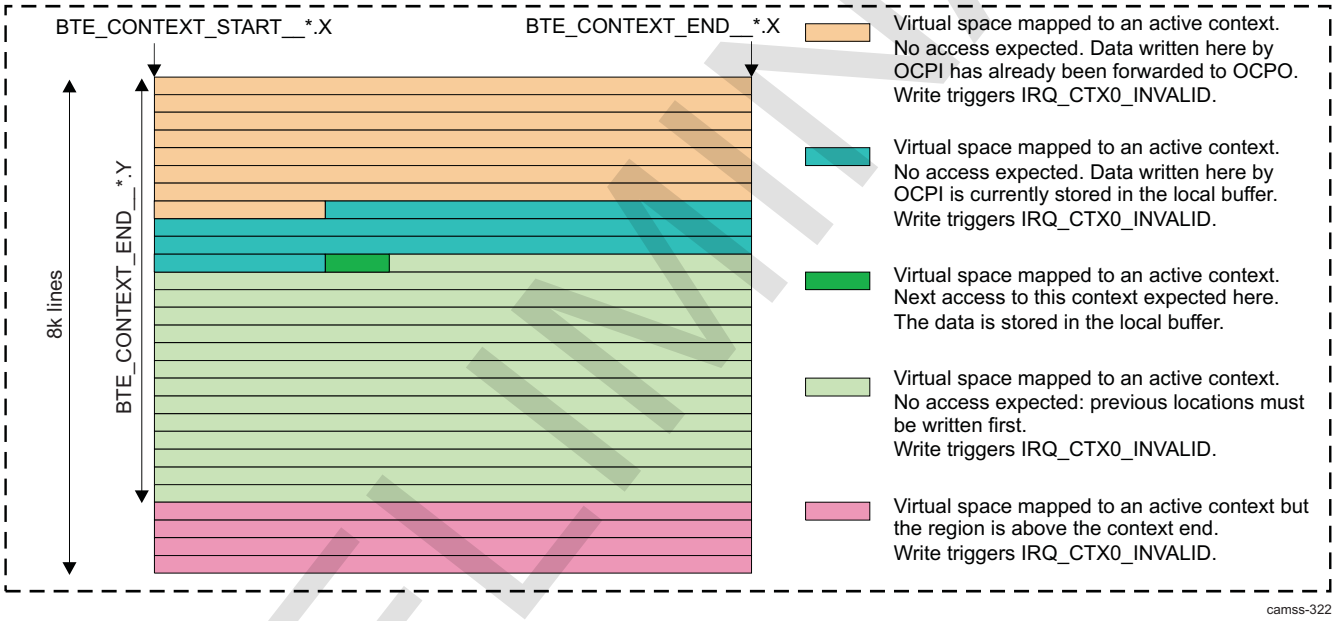
The (SX_i, SY_i) pointer of a context is updated on every access to this context. It is reset to SX_i = BTE_CONTEXT_START_i[15:7] X and SY_x = 0 when a context is enabled. SX_i is incremented by 1 for every received 16-byte word, except when it equals BTE_CONTEXT_END_i[15:4] X. In that case it is reset to BTE_CONTEXT_START_i[15:7] X and SY_i is incremented. SY_i is reset when it reaches the bottom-right corner of the context.

Therefore, the BTE can only translate raster accesses:

- Image data must be provided line by line, starting from the top-left corner of the context.
- A line stride of 64KB is expected.
- The maximum supported image height is 8k lines.

Figure 8-84 is an example of an active context. There is only one location in an active context where an access from OCPI is expected (green). Accesses to any other location trigger an IRQ_CTXx_INVALID event. Reads to contexts in write mode (BTE_CONTEXT_CTRL_i[7:6] MODE = 0) or writes to contexts in read mode (BTE_CONTEXT_CTRL_i[7:6] MODE = 1) trigger an IRQ_CTXx_INVALID event. When an access to an expected location is received but the burst length exceeds the context end, an IRQ_CTXx_INVALID event is triggered.

Figure 8-84. ISS BTE Expected Access Locations in the Virtual Space



Some alignment constraints are summarized as follows and are shown in Figure 8-85. They apply only to translated accesses.

- The context start addresses are aligned on 16-byte boundaries.
- The context width is aligned on 16-byte boundaries.
- The OCPI initiator must not use BYTEEN to qualify subwords in the middle of lines. The BTE interprets each BYTEEN as 0xFFFF. Access of partial words triggers an IRQ_CTXx_INVALID error.
- The line length sent by the initiator can be 1-byte aligned. The initiator can use BYTEEN to qualify valid data for the last access of the line. The BTE treats those accesses as full 16-byte writes and writes 0 data into its local buffers to complete the access. Those 0s are forwarded to OCPO when burst translation is performed. Software must ensure this data is discarded when the buffer is read back.
- The BTE does not impose any specific constraint on vertical alignment on the TILER tile and subtile grids. However, it is strongly recommended to configure the burst generation in such a way the requests performed to the TILER do not cross tile or subtile boundaries. For more information, see Section 8.2.7.3.2.5, *ISS BTE TILER Space Accesses: 2D Burst Generation*.
- The BTE accepts only one outstanding transaction per OCP tag on the OCPI port. When an initiator

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tries to generate an OCP request on a tag ID that is already used (no response has been returned on OCPI), the OCPI port is stalled.

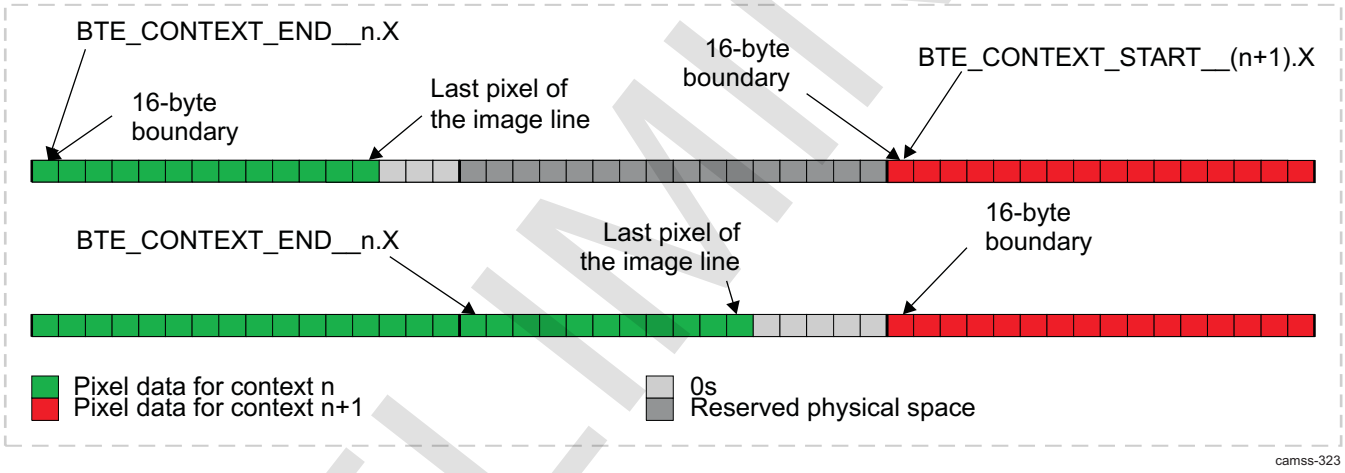
- The amount of memory allocated for each context must be a multiple of 512 bytes. Software must leave mod(BTE_CONTEXT_END_i BTE_CONTEXT_START_i + 1, 8) unused locations between the end of the context and the start of the next one. No accesses to this space from OCPI are allowed, but the BTE can use it to store data.
- While programming a BTE context, the BTE context End X value of all contexts must be less than MEMORY/64 in 128-bit address (equals MEMORY/4 in byte address)

NOTE: The generic BTE MEMORY size can be found by reading the BTE_HL_HWINFO[18:0] MEMORY bit field.

- While reading from a BTE-translated location, the CCP2 read burst size must be greater than or equal to (=) 16 bytes (128 bits) for correct operation. Bus width translation is performed in the ISS. Therefore, 64-bit accesses lead to 128-bit accesses with BYTEEN = 0x00FF. On the BTE side, BYTEEN is always processed as 0xFFFF; thus, access to a BTE-translated 128-bit location is not correct if software uses 64-bit access.

Figure 8-85 shows the BTE context alignment constraints.

Figure 8-85. ISS BTE Context Alignment Constraints



8.2.7.3.2.3 ISS BTE TILER Context Configuration Example

Global configuration and context configuration must be done before traffic from the master can be enabled.

This section provides a configuration example used to write YUV4:2:0 data into a 90-degree rotated buffer (S = 1,/Y = 1,/X = 0). The YUV frame is made up of two objects: Y data (8 bits) and UV data (16 bits).

The BTE provides data orientation and format information to the TILER using a 33-bit address. It can be controlled by software using the BTE_CONTEXT_BASE_i and BTE_CONTEXT_CTRL_i[12] ADDR32 bits. ADDR32 must be set to 1. Bits [31:27] of the address control the accessed view format. Table 8-233 is an example of a BTE TILER context configuration.

Figure 8-86 shows BTE TILER mode addressing in 90- or 270-degree orientation.

Table 8-233. ISS BTE TILER Context Configuration Example

32	31	30	29	28	27	26 ... 4	3 ... 0
T	Orientation			Mode		Virtual Address	
1	S	/Y	/X	M1	M0	A26 ... A4	0

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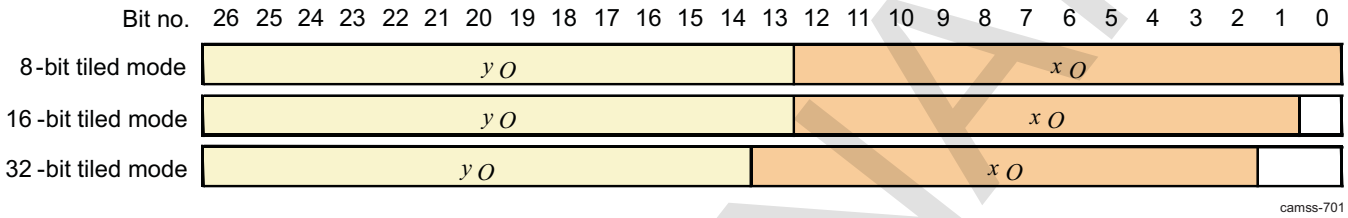
For the example described here, the following settings are used:

90-degree view, 8-bit data	ADDR[32:27] = 0b1 110 00
90-degree view, 16-bit data	ADDR[32:27] = 0b1 110 01

Software must also configure the BTE_CONTEXT_CTRL_i[9:8] GRID bit field to match the view and format set by the base address:

90-degree view, 8-bit data	GRID = 1	Stride = 8k
90-degree view, 16-bit data	GRID = 1	Stride = 8k

Figure 8-86. ISS BTE TILER Mode Addressing in 90- or 270-Degree Orientation



Bits [26:0] of the BTE_CONTEXT_BASE_i register are used to address a pixel in the virtual space of TILER. It must point to the top-left corner of the 2D object.

Software must also configure the other context register before it can start it by setting the BTE_CONTEXT_CTRL_i[0] START bit.

8.2.7.3.2.4 ISS BTE Local Memory Management

8.2.7.3.2.4.1 ISS BTE Introduction

The amount of data buffered is defined by the BTE_CONTEXT_CTRL_i[29:16] TRIGGER bit field. In write mode, translated 2D writes to OCPO are issued when the buffer fill level is greater than or equal to the value of the BTE_CONTEXT_CTRL_i[29:16] TRIGGER bit field. In read mode, translated 2D reads are sent to OCPO when the buffer level is less than the value of the BTE_CONTEXT_CTRL_i[29:16] TRIGGER bit field.

8.2.7.3.2.4.2 ISS BTE Buffer Flushing

8.2.7.3.2.4.2.1 ISS BTE One-Shot Mode

One-shot mode is enabled by setting the BTE_CONTEXT_CTRL_i[10] ONESHOT bit.

During normal operation, a data transfer from local memory to the TILER is automatically triggered when sufficient data is available in the buffer.

Three lines of data remain in the buffer once the OCPI initiator stops sending data into the context.

The BTE supports two ways to flush data remaining in the buffer:

- The last data (bottom-right corner) in a context is written. The last data is defined by the BTE_CONTEXT_END_i[15:4] X and BTE_CONTEXT_END_i[28:16] Y bit fields.
- Software writes the BTE_CONTEXT_CTRL_i[2] FLUSH bit. This is typically done when the context has been stopped before the full frame has been written.

An autoflush mode controls automatic context flushing when an IDLE request is received. It can be activated by setting the BTE_CONTEXT_CTRL_i[11] AUTOFLUSH bit to 1.

During a context flush, all remaining data in the buffer are written to the TILER.

Buffer flushing has lower priority than burst translation active contexts or forwarding transparent accesses. This prevents performance degradation.

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If software wants to abort context operation at a random location, it must disable the context.

8.2.7.3.2.4.2.2 ISS BTE Continuous Mode

When continuous mode is selected (the BTE_CONTEXT_CTRL_i[10] ONESHOT bit set to 0), reception of frame n pushes the data remaining from frame 1 out of the memory to OCPO. This mode is particularly useful when vertical blanking periods are too short to perform a buffer flush at the end of the frame. Also, it avoids creating traffic peaks due to buffer flushing.

The frame height must be a multiple of eight lines and the BTE_CONTEXT_CTRL_i[14:13] INITSY bit field must be 0x0 in continuous mode.

8.2.7.3.2.4.3 ISS BTE Buffer Prefetch

The buffer must be prefilled before read requests requiring translation can be accepted. Buffer prefetch starts with the top-left corner of the frame when a context is enabled by setting the BTE_CONTEXT_CTRL_i[0] START bit. When enough lines have been prefetched, an IRQ_CTXx_DONE event is triggered to inform software that the context is ready to perform request translation. Typically, software enables the data flow requiring translation in response to this event. Context ready for transaction and last transaction can be controlled by BTE_CONTEXT_START and BTE_CONTEXT_END, respectively.

When a read request requiring translation is received while prefetch is ongoing, an IRQ_CTXx_ERR event is triggered. It informs software that the read traffic was enabled too early. The BTE returns 0s to OCPI for the failing request (it does not hold the response until real data is available).

After prefetch completion, when a request requiring translation is received but the required data is missing (the BTE is waiting for a response from OCPO), the BTE delays the response on OCPI until the missing data is received on OCPI.

This behavior avoids stalling the OCPI port for too long (that is, a prefetch of up to 3.25 lines of data). However, it avoids getting errors because of slow OCPI responses.

8.2.7.3.2.4.4 ISS BTE Bandwidth Limiter

Translated and transparent traffic has higher priority than prefetch and flushing traffic. However, overall system bandwidth is limited. Requesting too much bandwidth for prefetch and flushing traffic may increase latencies for higher priority traffic. That could affect higher priority traffic.

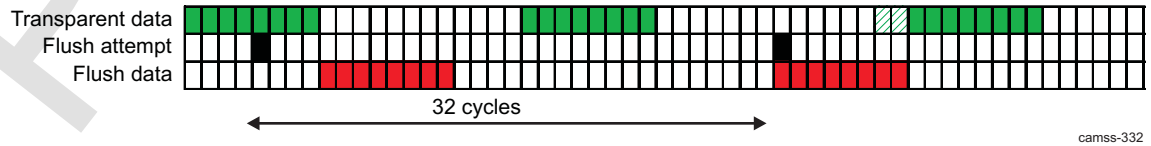
Software can limit the speed of prefetching and buffer flushing by using the BTE_CTRL[31:22] BW_LIMITER bit field. Typically, this register is used to avoid the buffer prefetch and flush traffic using all the available system bandwidth. This register does not slow down the translated or transparent traffic.

The example in Figure 8-87 assumes:

- 200-MHz functional clock
- 800 Mbps of transparent traffic = one 8 × 128-bit burst every 32 cycles

Without the bandwidth limiter, prefetch and flush traffic may use up to 3.2 0.8 = 2.4Gbps. Using BTE_CTRL[31:22] BW_LIMITER = 24 ensures that at a maximum one flush/prefetch request is issued every 32 cycles. A prefetch/flush request may be delayed by higher priority traffic of OCP port stalls. To avoid excessive traffic slowdown, the BTE tries to catch up by requesting the next flush/prefetch transaction earlier.

Figure 8-87. BTE Bandwidth Limiter Example



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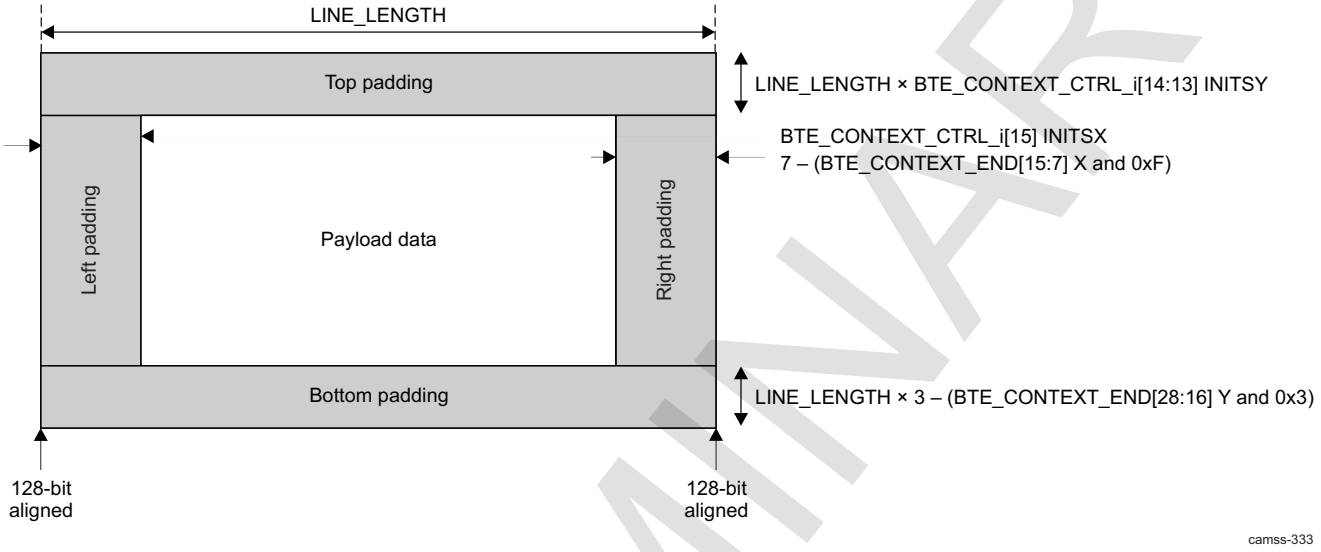
8.2.7.3.2.5 ISS BTE TILER Space Accesses: 2D Burst Generation

8.2.7.3.2.5.1 ISS BTE Buffer Fill Level

The BTE maintains an internal counter to keep track of the buffer fill level. This internal counter is used to detect when a translated OCP request is sent to the OCPO port. The counter also accounts for padding data. Figure 8-88 shows the BTE buffer fill-level padding.

Figure 8-88. ISS BTE Buffer Fill-Level Padding



In BTE context, the preferred parameter to be used is128-bit word as unit. The BTE_CONTEXT_START_i and BTE_CONTEXT_END_i registers are usually written as byte-aligned; however, the BTE_CONTEXT_START_i.X and BTE_CONTEXT_END_i.X bit fields are more readily understood (nominally) as (128 bytes = 8 x 128 bits = 8 words).

The (lower half) BTE_CONTEXT_END_i register must be written as byte-aligned, but the BTE_CONTEXT_END_i.X bit field is understood (nominally) as (128 bits = 1 word).

The BTE TRIGGER is based on word size (128 bits), but the related register (upper half) BTE_BTE_CONTEXT_CTRL_i register is not byte-aligned; it is word-aligned (128-bits).

LINE_LENGTH = ((BTE_CONTEXT_END_i[15:4] X) – BTE_CONTEXT_START_i[15:7] X) 4) 0xFF8 + 8

NOTE: LINE_LENGTH is measured as a 128-bit word and can be used directly for TRIGGER calculation (3 * LINE_LENGTH + x)

Example 1: 64 x 15 pixels line = 64 x 15 Nb bytes in a line

(Nb bytes in a line – 16(128-bit word)) 4 = 0x3B

LINE_LENGTH = (0x3B 0xFF8) + 8 = 0x40

TRIGGER = 0x40 * 3 + 2 = 0xC2

Example 2: 64 x 11 pixel line = 64 x 11 Nb bytes in a line

(Nb bytes in a line – 16(128-bit word)) 4 = 0x2B

LINE_LENGTH = (0x2B 0xFF8) + 8 = 0x30

TRIGGER = 0x30 * 3 + 2 = 0x92

Figure 8-88 is a visual representation of the following explanation about how read or write events are triggered determined by the internal buffer size.

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When context is started, the buffer fill level is initialized to LINE_LENGTH × BTE_CONTEXT_CTRL_i[14:13] INITSY + BTE_CONTEXT_CTRL_i[15] INITSX (see the previous equation for the LINE_LENGTH calculation). If the BTE reads or writes, the level of the internal buffer is incremented or decremented, respectively, by the burst size. Here, only full 16-byte accesses are performed. Other OCP BYTEEN patterns are forced to 0xFF.

The BTE_CONTEXT_CTRL_i [29:16] TRIGGER bit field triggers a buffer level read or write even. In write mode, if flushing, the data level is greater than 0; if not flushing, the BTE translates to OCPO when the level is greater than or equal to the value set by the register. If the level is smaller than the BTE_CONTEXT_CTRL_i[29:16] TRIGGER software setup, then the BTE reads data.

8.2.7.3.2.5.2 ISS BTE OCP Request Generation

Except on borders:

- TILER bursts are 32 bytes × 4 lines of data blocks.
- Bursts are aligned on subtile boundaries.

The BTE maintains an internal 2D pointer (DX_i, DY_i) that corresponds to the top-left corner of the next access to be issued to the TILER. It is initialized to (0, 0) when a context is enabled or wraps around. It is updated each time an access to the TILER is performed.

Table 8-234 lists all supported TILER formats and views.

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Table 8-234. ISS BTE Supported TILER Formats and Views

Modes	View			Description	OFST	Subtile Grid		1KB Tile Grid		X		Y		GRID	Subtile Aligned		Tile Aligned	
	S	/Y	/X			X	Y	X	Y	LSB	MSB	LSB	MSB		X	Y	X	Y
8-bit	0	0	0	0-degree view	16384	4	4	32	32	0	13	14	26	0	[1:0]	[15:14]	[4:0]	[18:14]
	0	0	1	0-degree view with vertical mirror														
	0	1	0	0-degree view with horizontal mirror														
	0	1	1	180-degree view														
	1	0	0	90-degree view with vertical mirror	8192	4	4	32	32	0	12	13	26	1	[1:0]	[14:13]	[4:0]	[17:13]
	1	0	1	270-degree view														
	1	1	0	90-degree view														
	1	1	1	90-degree view with horizontal mirror														
16-bit	0	0	0	0-degree view	32768	8	2	64	16	0	14	15	26	2	[2:0]	[15]	[5:0]	[18:15]
	0	0	1	0-degree view with vertical mirror														
	0	1	0	0-degree view with horizontal mirror														
	0	1	1	180-degree view														
	1	0	0	90-degree view with vertical mirror	8192	4	4	32	32	0	12	13	26	1	[1:0]	[14:13]	[4:0]	[17:13]
	1	0	1	270-degree view														
	1	1	0	90-degree view														
	1	1	1	90-degree view with horizontal mirror														
32-bit	0	0	0	0-degree view	32768	8	2	64	16	0	14	15	26	2	[2:0]	[15]	[5:0]	[18:15]
	0	0	1	0-degree view with vertical mirror														
	0	1	0	0-degree view with horizontal mirror														
	0	1	1	180-degree view														
	1	0	0	90-degree view with vertical mirror	16384	8	2	64	16	0	13	14	26	3	[2:0]	[14]	[5:0]	[17:14]
	1	0	1	270-degree view														
	1	1	0	90-degree view														
	1	1	1	90-degree view with horizontal mirror														

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The BTE_CONTEXT_BASE_i and BTE_CONTEXT_CTRL_i[9:8] GRID registers must the configured by software to choose the format and view. The format must match the data stored into the virtual space. The choice of the view depends on the desired behavior.

The GRID bit field controls the used OCP stride and OCP address generation. The OCP address is generated using the following formula:

OCP_ADDR = BTE_CONTEXT_BASE_n + DX_x + DY_x Y_LSB

Y_LSB corresponds to the Y LSB column of Table 8-234.

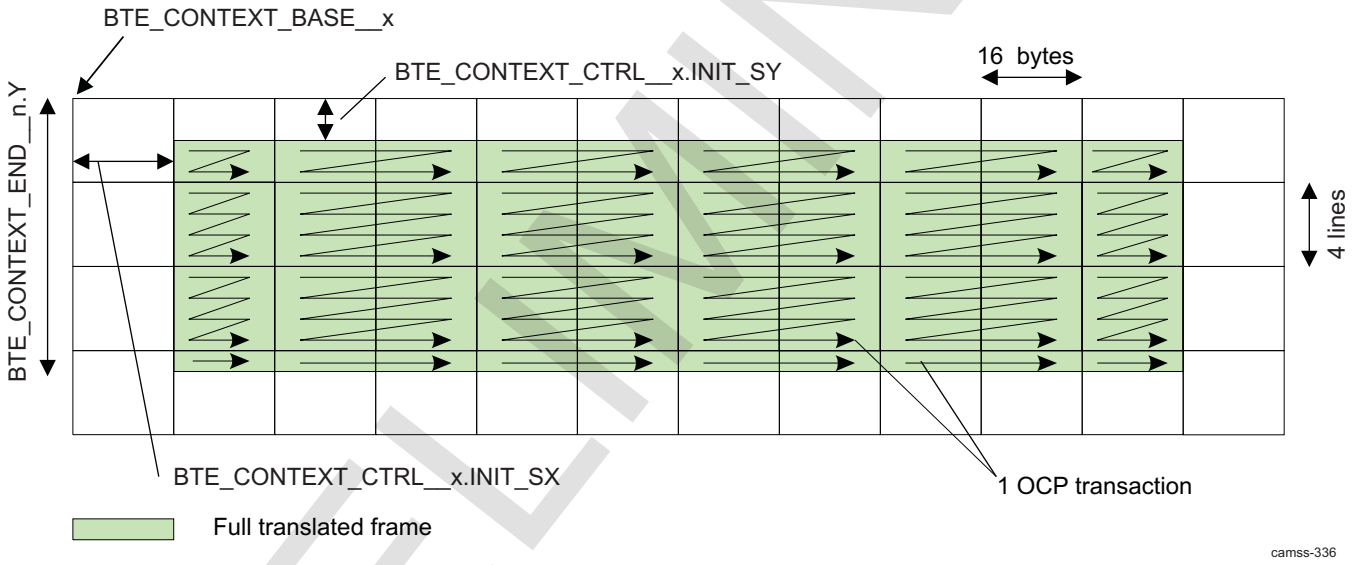
The OCP stride corresponds to the OFST column of Table 8-234. The tile and subtile grid information is currently not used by hardware.

The BTE does not automatically realign 2D bursts on tile or subtile boundaries. However, software can force the (SX_i, SY_i) (see Section 8.2.7.3.2.4, *ISS BTE Local Memory Management*, for the definition of SY_i) reset value to be used. It is set through the BTE_CONTEXT_CTRL_i[15] INITSX bit and the BTE_CONTEXT_CTRL_i[14:13] INITSY bit field.

The length and height of the 2D burst is adapted by the BTE to avoid sending dummy data to the TILER.

Figure 8-89 is an example of BTE 2D burst generation. The vertical start and end of the full 2D frame are not vertically aligned on the grid.

Figure 8-89. ISS BTE 2D Burst Generation



8.2.7.3.2.6 ISS BTE Posted and Nonposted Write Support

The BTE can handle posted and nonposted writes received on OCPI. Normally, only nonposted writes should be used.

For transparent accesses, posted and nonposted writes are forwarded to OCPO. The response provided by OCPO is returned to OCPI.

For translated accesses, the response to posted and nonposted writes is provided by the BTE. It does not wait for the response of the translated request that is sent to the TILER. In other words, the BTE has no true nonposted write support for translated accesses. The BTE does not ensure that the data has effectively been written to the destination memory when it returns the response to a nonposted translated write.

True nonposted write support is ensured for transparent accesses. Only nonposted writes must be used. Select nonposted write mode through the BTE_CTRL[5] POSTED bit.

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8.2.7.3.2.7 ISS BTE Error Reporting

Unexpected accesses are flagged using interrupts. Also, when an SResp = ERR is received on OCPO, an interrupt is triggered. If the response corresponds to a transparent access, it is forwarded to OCPI.

The BTE is not an OCP checker: It expects only valid and supported transactions from the external world.

Also, it is not intended to detect all types of software errors; few cases are detected. Those cases are described in the functional description sections.

8.2.7.3.2.8 ISS BTE Interrupts

All events generated by the module are merged into a single event at ISS level. This event can be enabled from ISS level by the ISS_HL_IRQENABLE_SET_i[11] BTE_IRQ bit. Table 8-235 lists the BTE interrupt events.

Table 8-235. ISS BTE Interrupt Events

Event	Description
IRQ_OCP_ERR	OCP error received from OCPO master port
IRQ_INVALID	An access to a location that is not mapped to any context has been performed. For more information, see Section 8.2.7.3.2.2, *ISS BTE Virtual Address Space and Context Mapping*.
IRQ_CTXx_DONE	Context has been fully transferred to the TILER. This interrupt is triggered when flushing completes in one-shot mode. It is triggered once per frame in continuous mode.
IRQ_CTXx_INVALID	Unexpected address sequence or access direction (read of a context in write mode or write of a context in read mode). For more information, see Section 8.2.7.3.2.2, *ISS BTE Virtual Address Space and Context Mapping*.
IRQ_CTXx_ERR	Can occur only when a context is configured in read mode. This request triggers when a read request is received but insufficient data is buffered to perform the translation. For more information, see Section 8.2.7.3.2.4.3, *ISS BTE Buffer Prefetch*.

8.2.7.3.2.9 ISS BTE Debug Support

The BTE has no specific debug support.

8.2.7.4 ISS BTE Programming Model

8.2.7.4.1 ISS BTE Reset

The BTE can accept a general software reset, propagated through all the hierarchy. This reset can be done to initialize the module and has the same effect as the hardware reset.

1. Set the BTE_HL_SYSCONFIG[0] SOFTRESET bit to 1.
2. Read the BTE_HL_SYSCONFIG[0] SOFTRESET bit to check whether it is set to 1, which means the reset occurred.

If after five reads, the BTE_HL_SYSCONFIG[0] SOFTRESET bit still returns 0, assume that an error occurred during the reset stage.

Programmers must not set the BTE_HL_SYSCONFIG[0] SOFTRESET bit to 1 if the BTE is integrated in a subsystem; it is safer to use the software reset at subsystem level.

NOTE: A software reset does not reset the IDLE protocol signals.

8.2.7.4.2 ISS BTE Interrupts

All events are mapped to a single interrupt output, BTE_IRQ. Table 8-236 lists the procedure to configure or manage the BTE interrupts.

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Table 8-236. ISS BTE Configure/Manage Interrupts

Step	Bit Field	Value
Each event that generates an interrupt can be individually enabled by setting the appropriate bit.	BTE_HL_IRQENABLE_SET	
Each event that generates an interrupt can be individually disabled by setting the adequate bit.	BTE_HL_IRQENABLE_CLR	
When an event occurs, the corresponding bit in the BTE_HL_IRQSTATUS_RAW register is set, regardless of whether or not the event is enabled. Bits in the BTE_HL_IRQSTATUS registers are set only when an enabled event occurs.	BTE_HL_IRQSTATUS_RAW and BTE_HL_IRQSTATUS	
Software can clear a pending event by setting the adequate bit in the BTE_HL_IRQSTATUS register.	BTE_HL_IRQSTATUS	

8.2.7.4.3 ISS BTE Context Configuration

Global configuration and context configuration must be done before traffic from the master can be enabled.

This section provides a configuration example used to write YUV4:2:0 data into a 90-degree rotated buffer (S = 1,/Y = 1,/X = 0). The YUV frame consists of two objects: Y data (8 bits) and UV data (16 bits).

The BTE provides data orientation and format information to the TILER using a 33-bit address. It can be controlled by software using the BTE_CONTEXT_BASE_i and BTE_CONTEXT_CTRL_i[12] ADDR32 registers.

ADDR32 must be set to 1. Bits [31:27] of the address control the accessed view and data format. Table 8-237 gives the format of the TILER address. Figure 8-90 shows BTE tiled mode addressing in 90- or 270-degree orientation.

Table 8-. TILER Address Format

32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
T	Orientation			Mode		Virtual Address																										
1	S	Y	X	M1	M0	A26 ... A4																			0							

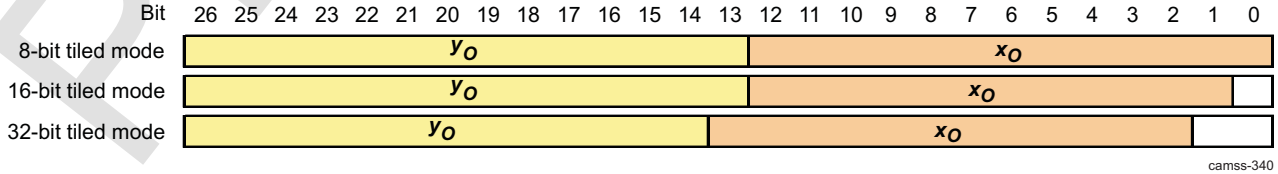
For the example described here, the following settings are used.

90-degree view, 8-bit data ADDR[32:27] = 0b1 110 00
90-degree view, 16-bit data ADDR[32:27] = 0b1 110 01

Software must also configure the BTE_CONTEXT_CTRL_i[9:8] GRID bit field to match the view and format set by the base address:

90-degree view, 8-bit data GRID = 1 Stride = 8k
90-degree view, 16-bit data GRID = 1 Stride = 8k

Figure 8-90. ISS BTE Tiled Mode Addressing in 90- or 270-Degree Orientation (S = 1)



Bits [26:0] of the BTE_CONTEXT_BASE_i register are used to address a pixel in the virtual space of the TILER. It must point to the top-left corner of the 2D object.

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Software must also configure the other context registers before it can start it by setting the BTE_CONTEXT_CTRL_i[0] START bit.

8.2.7.4.4 ISS BTE Change Context Configuration

All contexts operate independently. Software can change the configuration of an inactive context while other contexts are active and perform request translation.

When software must change the configuration of an active context, it must follow the sequence in Table 8-238.

Table 8-238. ISS BTE Change Context Configuration

Step	Bit Field	Value
Ensure that the initiator does not send any more data to this context until it is re-enabled.		
Disable the context. • The STOP condition is considered on a valid OCP boundary. • It preserves the internal states so that buffer flushing can be done. • The BTE no longer translates requests received for this context. Any transactions received for an inactive context trigger error interrupts. • The BTE completes all outstanding transactions on OCPO.	BTE_CONTEXT_CTRL_i[1] STOP	0x1
Flush all remaining data for the context, if needed. If software simply wants to abort the transfer to recover from some error condition, flushing is not needed. The context is automatically reset when it is enabled again.	BTE_CONTEXT_CTRL_i[2] FLUSH	0x1
Wait until the context completes pending OCP transaction and buffer flush (if enabled). It sets the IRQ_CTXx_DONE when it becomes idle.	BTE_HL_IRQSTATUS. IRQ_CTXx_DONE	Read 0x0
Change the context configuration.		
Enable the context by setting the BTE_CONTEXT_CTRL_i[0] START bit. Setting the START bit resets the internal state-machine of the context.	BTE_CONTEXT_CTRL_i[0] START	0x1

Alternatively, software can change the context mode to one-shot and wait until the CTXx_DONE_IRQ is triggered.

NOTE: Once a context is disabled it cannot be resumed simply by writing the START bit. In fact, doing so resets the internal FSM. If data is lost in the buffer, it will be lost.

8.2.7.5 ISS BTE Register Manual

8.2.7.5.1 ISS BTE Instance Summary

Table 8-239 lists the BTE instance.

Table 8-239. ISS BTE Instance Summary

Module Name	L3 Base Address	Size
ISS_BTE	0x5200 2000	512 bytes

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8.2.7.5.2 ISS BTE Registers

8.2.7.5.2.1 ISS BTE Register Summary

Table 8-240 summarizes the BTE registers.

Table 8-240. ISS BTE Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	ISS_BTE Base Address
BTE_HL_REVISION	R	32	0x0000 0000	0x5200 2000
BTE_HL_HWINFO	R	32	0x0000 0004	0x5200 2004
BTE_HL_SYSCONFIG	RW	32	0x0000 0010	0x5200 2010
RESERVED	RW	32	0x0000 001C	0x5200 201C
BTE_HL_IRQSTATUS_RAW	RW	32	0x0000 0020	0x5200 2020
BTE_HL_IRQSTATUS	RW	32	0x0000 0024	0x5200 2024
BTE_HL_IRQENABLE_SET	RW	32	0x0000 0028	0x5200 2028
BTE_HL_IRQENABLE_CLR	RW	32	0x0000 002C	0x5200 202C
BTE_CTRL	RW	32	0x0000 0030	0x5200 2030
BTE_CTRL1	RW	32	0x0000 0034	0x5200 2034
BTE_CONTEXT_CTRL_i (1)	RW	32	0x0000 0040 + (0x20 * i)	0x5200 2040 + (0x20 * i)
BTE_CONTEXT_BASE_i (1)	RW	32	0x0000 0044 + (0x20 * i)	0x5200 2044 + (0x20 * i)
BTE_CONTEXT_START_i (1)	RW	32	0x0000 0048 + (0x20 * i)	0x5200 2048 + (0x20 * i)
BTE_CONTEXT_END_i (1)	RW	32	0x0000 004C + (0x20 * i)	0x5200 204C + (0x20 * i)

(1) i = 0 to 7

8.2.7.5.2.2 ISS BTE Register Description

Table 8-241 through Table 8-266 describe the BTE registers.

Table 8-241. BTE_HL_REVISION

Address Offset	0x0000 0000		
Physical Address	0x5200 2000	**Instance**	ISS_BTE
Description	IP revision identifier (X.Y.R) Used by software to track features, bugs, and compatibility		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP revision	R	See (1)

(1) TI internal data

Table 8-242. Register Call Summary for Register BTE_HL_REVISION

ISS Interfaces
- ISS BTE Registers: [0]

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Table 8-243. BTE_HL_HWINFO

Address Offset	0x0000 0004		
Physical Address	0x5200 2004	**Instance**	ISS_BTE
Description	Information about the hardware configuration of the IP module; that is, typically, the HDL generics (if any) of the module.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								RESPFIFO			CONTEXTS					RESERVED															

Bits	Field Name	Description	Type	Reset
31:24	RESERVED	Reserved	R	0x00
23:21	RESPFIFO	Response FIFO size Read 0x3: 64 x 128 bits Read 0x4: 128 x 128 bits Read 0x2: 32 x 128 bits Read 0x0: Reserved Read 0x6: Reserved Read 0x1: 16 x 128 bits Read 0x7: Reserved Read 0x5: Reserved	R	0x2
20:19	CONTEXTS	Number of contexts Read 0x3: Reserved Read 0x2: 8 contexts Read 0x1: 4 contexts Read 0x0: 2 contexts	R	0x1
18:0	RESERVED	Reserved	R	0x056A0

Table 8-244. Register Call Summary for Register BTE_HL_HWINFO

ISS Interfaces

- ISS BTE Functional Description Details: [0]
- ISS BTE Registers: [1]

Table 8-245. BTE_HL_SYSCONFIG

Address Offset	0x0000 0010		
Physical Address	0x5200 2010	**Instance**	ISS_BTE
Description	Clock management configuration		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												IDLEMODE		RESERVED	SOFTRESET

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Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0000000
3:2	IDLEMODE	Configuration of the local target state management mode. By definition, target can handle read/write transaction as long as it is out of IDLE state. 0x0: An IDLE request is acknowledged unconditionally 0x1: An IDLE request is never acknowledged 0x3: Reserved. Do not use 0x2: Smart-idle mode. Acknowledgment to an IDLE request is given based on the internal activity of the module.	RW	0x2
1	RESERVED		R	0
0	SOFTRESET	Software reset. Write 0x0: No action Write 0x1: Initiate software reset Read 0x1: Reset (software or other) ongoing Read 0x0: Reset done, no pending action	RW	0

Table 8-246. Register Call Summary for Register BTE_HL_SYSCONFIG

ISS Interfaces
- ISS BTE Reset: [0] [1] [2] [3]
- ISS BTE Registers: [4]

Table 8-247. BTE_HL_IRQSTATUS_RAW

Address Offset	0x0000 0020		
Physical Address	0x5200 2020	**Instance**	ISS_BTE
Description	Per-event raw interrupt status vector Raw status is set even if event is not enabled. Write 1 to set the (raw) status, mostly for debug.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IRQ_CTX7_ERR	IRQ_CTX6_ERR	IRQ_CTX5_ERR	IRQ_CTX4_ERR	IRQ_CTX3_ERR	IRQ_CTX2_ERR	IRQ_CTX1_ERR	IRQ_CTX0_ERR	IRQ_CTX7_INVALID	IRQ_CTX6_INVALID	IRQ_CTX5_INVALID	IRQ_CTX4_INVALID	IRQ_CTX3_INVALID	IRQ_CTX2_INVALID	IRQ_CTX1_INVALID	IRQ_CTX0_INVALID	IRQ_CTX7_DONE	IRQ_CTX6_DONE	IRQ_CTX5_DONE	IRQ_CTX4_DONE	IRQ_CTX3_DONE	IRQ_CTX2_DONE	IRQ_CTX1_DONE	IRQ_CTX0_DONE	RESERVED						IRQ_INVALID	IRQ_OCP_ERR

Bits	Field Name	Description	Type	Reset
31	IRQ_CTX7_ERR	Read request received before sufficient data has been prefetched. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
30	IRQ_CTX6_ERR	Read request received before sufficient data has been prefetched. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0

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Bits	Field Name	Description	Type	Reset
29	IRQ_CTX5_ERR	Read request received before sufficient data has been prefetched. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
28	IRQ_CTX4_ERR	Read request received before sufficient data has been prefetched. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
27	IRQ_CTX3_ERR	Read request received before sufficient data has been prefetched. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
26	IRQ_CTX2_ERR	Read request received before sufficient data has been prefetched. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
25	IRQ_CTX1_ERR	Read request received before sufficient data has been prefetched. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
24	IRQ_CTX0_ERR	Read request received before sufficient data has been prefetched. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
23	IRQ_CTX7_INVALID	Invalid access. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
22	IRQ_CTX6_INVALID	Invalid access. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
21	IRQ_CTX5_INVALID	Invalid access. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0

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Bits	Field Name	Description	Type	Reset
20	IRQ_CTX4_INVALID	Invalid access. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
19	IRQ_CTX3_INVALID	Invalid access. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
18	IRQ_CTX2_INVALID	Invalid access. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
17	IRQ_CTX1_INVALID	Invalid access. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
16	IRQ_CTX0_INVALID	Invalid access. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
15	IRQ_CTX7_DONE	Context has been fully transferred to the TILER Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
14	IRQ_CTX6_DONE	Context has been fully transferred to the TILER Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
13	IRQ_CTX5_DONE	Context has been fully transferred to the TILER Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
12	IRQ_CTX4_DONE	Context has been fully transferred to the TILER Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0

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Bits	Field Name	Description	Type	Reset
11	IRQ_CTX3_DONE	Context has been fully transferred to the TILER Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
10	IRQ_CTX2_DONE	Context has been fully transferred to the TILER Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
9	IRQ_CTX1_DONE	Context has been fully transferred to the TILER Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
8	IRQ_CTX0_DONE	Write mode: Context has been fully transferred to the TILER Read mode: Context prefetch has completed. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
7:2	RESERVED		R	0x00
1	IRQ_INVALID	Invalid access to the virtual space Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
0	IRQ_OCP_ERR	OCP error received from OCP master port. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0

Table 8-248. Register Call Summary for Register BTE_HL_IRQSTATUS_RAW

ISS Interfaces

- ISS BTE Interrupts: [0] [1]
- ISS BTE Registers: [2]

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Table 8-249. BTE_HL_IRQSTATUS

Address Offset	0x0000 0024		
Physical Address	0x5200 2024	**Instance**	ISS_BTE
Description	Per-event "enabled" interrupt status vector. Enabled status is not set unless event is enabled. Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, that is, even if not enabled).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IRQ_CTX7_ERR	IRQ_CTX6_ERR	IRQ_CTX5_ERR	IRQ_CTX4_ERR	IRQ_CTX3_ERR	IRQ_CTX2_ERR	IRQ_CTX1_ERR	IRQ_CTX0_ERR	IRQ_CTX7_INVALID	IRQ_CTX6_INVALID	IRQ_CTX5_INVALID	IRQ_CTX4_INVALID	IRQ_CTX3_INVALID	IRQ_CTX2_INVALID	IRQ_CTX1_INVALID	IRQ_CTX0_INVALID	IRQ_CTX7_DONE	IRQ_CTX6_DONE	IRQ_CTX5_DONE	IRQ_CTX4_DONE	IRQ_CTX3_DONE	IRQ_CTX2_DONE	IRQ_CTX1_DONE	IRQ_CTX0_DONE	RESERVED						IRQ_INVALID	IRQ_OCP_ERR

Bits	Field Name	Description	Type	Reset
31	IRQ_CTX7_ERR	Read request received before sufficient data has been prefetched. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
30	IRQ_CTX6_ERR	Read request received before sufficient data has been prefetched. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
29	IRQ_CTX5_ERR	Read request received before sufficient data has been prefetched. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
28	IRQ_CTX4_ERR	Read request received before sufficient data has been prefetched. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
27	IRQ_CTX3_ERR	Read request received before sufficient data has been prefetched. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
26	IRQ_CTX2_ERR	Read request received before sufficient data has been prefetched. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
25	IRQ_CTX1_ERR	Read request received before sufficient data has been prefetched. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
24	IRQ_CTX0_ERR	Read request received before sufficient data has been prefetched. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
23	IRQ_CTX7_INVALID	Invalid access. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
22	IRQ_CTX6_INVALID	Invalid access. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
21	IRQ_CTX5_INVALID	Invalid access. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
20	IRQ_CTX4_INVALID	Invalid access. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
19	IRQ_CTX3_INVALID	Invalid access. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
18	IRQ_CTX2_INVALID	Invalid access. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
17	IRQ_CTX1_INVALID	Invalid access. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
16	IRQ_CTX0_INVALID	Invalid access. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
15	IRQ_CTX7_DONE	Context has been fully transferred to the TILER Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
14	IRQ_CTX6_DONE	Context has been fully transferred to the TILER Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
13	IRQ_CTX5_DONE	Context has been fully transferred to the TILER Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
12	IRQ_CTX4_DONE	Context has been fully transferred to the TILER Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
11	IRQ_CTX3_DONE	Context has been fully transferred to the TILER Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
10	IRQ_CTX2_DONE	Context has been fully transferred to the TILER Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
9	IRQ_CTX1_DONE	Context has been fully transferred to the TILER Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
8	IRQ_CTX0_DONE	Write mode: Context has been fully transferred to the TILER Read mode: Context prefetch has completed. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
7:2	RESERVED		R	0x00
1	IRQ_INVALID	Invalid access to the virtual space Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
0	IRQ_OCP_ERR	OCP error received from OCP master port. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0

Table 8-250. Register Call Summary for Register BTE_HL_IRQSTATUS

ISS Interfaces

- ISS BTE Interrupts: [0] [1] [2] [3]
- ISS BTE Change Context Configuration: [4]
- ISS BTE Registers: [5]

Table 8-251. BTE_HL_IRQENABLE_SET

Address Offset	0x0000 0028		
Physical Address	0x5200 2028	**Instance**	ISS_BTE
Description	Per-event interrupt enable bit vector Write 1 to set (enable interrupt). Readout equal to corresponding _CLR register.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IRQ_CTX7_ERR	IRQ_CTX6_ERR	IRQ_CTX5_ERR	IRQ_CTX4_ERR	IRQ_CTX3_ERR	IRQ_CTX2_ERR	IRQ_CTX1_ERR	IRQ_CTX0_ERR	IRQ_CTX7_INVALID	IRQ_CTX6_INVALID	IRQ_CTX5_INVALID	IRQ_CTX4_INVALID	IRQ_CTX3_INVALID	IRQ_CTX2_INVALID	IRQ_CTX1_INVALID	IRQ_CTX0_INVALID	IRQ_CTX7_DONE	IRQ_CTX6_DONE	IRQ_CTX5_DONE	IRQ_CTX4_DONE	IRQ_CTX3_DONE	IRQ_CTX2_DONE	IRQ_CTX1_DONE	IRQ_CTX0_DONE	RESERVED						IRQ_INVALID	IRQ_OCP_ERR

Bits	Field Name	Description	Type	Reset
31	IRQ_CTX7_ERR	Read request received before sufficient data has been prefetched. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0

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Bits	Field Name	Description	Type	Reset
30	IRQ_CTX6_ERR	Read request received before sufficient data has been prefetched. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
29	IRQ_CTX5_ERR	Read request received before sufficient data has been prefetched. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
28	IRQ_CTX4_ERR	Read request received before sufficient data has been prefetched. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
27	IRQ_CTX3_ERR	Read request received before sufficient data has been prefetched. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
26	IRQ_CTX2_ERR	Read request received before sufficient data has been prefetched. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
25	IRQ_CTX1_ERR	Read request received before sufficient data has been prefetched. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
24	IRQ_CTX0_ERR	Read request received before sufficient data has been prefetched. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
23	IRQ_CTX7_INVALID	Invalid access. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0

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Bits	Field Name	Description	Type	Reset
22	IRQ_CTX6_INVALID	Invalid access. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
21	IRQ_CTX5_INVALID	Invalid access. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
20	IRQ_CTX4_INVALID	Invalid access. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
19	IRQ_CTX3_INVALID	Invalid access. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
18	IRQ_CTX2_INVALID	Invalid access. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
17	IRQ_CTX1_INVALID	Invalid access. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
16	IRQ_CTX0_INVALID	Invalid access. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
15	IRQ_CTX7_DONE	Context has been fully transferred to the TILER Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
14	IRQ_CTX6_DONE	Context has been fully transferred to the TILER Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0

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Bits	Field Name	Description	Type	Reset
13	IRQ_CTX5_DONE	Context has been fully transferred to the TILER Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
12	IRQ_CTX4_DONE	Context has been fully transferred to the TILER Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
11	IRQ_CTX3_DONE	Context has been fully transferred to the TILER Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
10	IRQ_CTX2_DONE	Context has been fully transferred to the TILER Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
9	IRQ_CTX1_DONE	Context has been fully transferred to the TILER Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
8	IRQ_CTX0_DONE	Write mode: Context has been fully transferred to the TILER Read mode: Context prefetch has completed. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
7:2	RESERVED		R	0x00
1	IRQ_INVALID	Invalid access to the virtual space Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
0	IRQ_OCP_ERR	OCP error received from OCP master port. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0

Table 8-252. Register Call Summary for Register BTE_HL_IRQENABLE_SET

ISS Interfaces

- ISS BTE Interrupts: [0]
- ISS BTE Registers: [1]

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Table 8-253. BTE_HL_IRQENABLE_CLR

Address Offset	0x0000 002C
Physical Address	0x5200 202C **Instance** ISS_BTE
Description	Per-event interrupt enable bit vector Write 1 to clear (disable interrupt). Readout equal to corresponding _SET register.
Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IRQ_CTX7_ERR	IRQ_CTX6_ERR	IRQ_CTX5_ERR	IRQ_CTX4_ERR	IRQ_CTX3_ERR	IRQ_CTX2_ERR	IRQ_CTX1_ERR	IRQ_CTX0_ERR	IRQ_CTX7_INVALID	IRQ_CTX6_INVALID	IRQ_CTX5_INVALID	IRQ_CTX4_INVALID	IRQ_CTX3_INVALID	IRQ_CTX2_INVALID	IRQ_CTX1_INVALID	IRQ_CTX0_INVALID	IRQ_CTX7_DONE	IRQ_CTX6_DONE	IRQ_CTX5_DONE	IRQ_CTX4_DONE	IRQ_CTX3_DONE	IRQ_CTX2_DONE	IRQ_CTX1_DONE	IRQ_CTX0_DONE	RESERVED						IRQ_INVALID	IRQ_OCP_ERR

Bits	Field Name	Description	Type	Reset
31	IRQ_CTX7_ERR	Read request received before sufficient data has been prefetched. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
30	IRQ_CTX6_ERR	Read request received before sufficient data has been prefetched. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
29	IRQ_CTX5_ERR	Read request received before sufficient data has been prefetched. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
28	IRQ_CTX4_ERR	Read request received before sufficient data has been prefetched. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
27	IRQ_CTX3_ERR	Read request received before sufficient data has been prefetched. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
26	IRQ_CTX2_ERR	Read request received before sufficient data has been prefetched. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
25	IRQ_CTX1_ERR	Read request received before sufficient data has been prefetched. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
24	IRQ_CTX0_ERR	Read request received before sufficient data has been prefetched. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
23	IRQ_CTX7_INVALID	Invalid access. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
22	IRQ_CTX6_INVALID	Invalid access. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
21	IRQ_CTX5_INVALID	Invalid access. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
20	IRQ_CTX4_INVALID	Invalid access. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
19	IRQ_CTX3_INVALID	Invalid access. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
18	IRQ_CTX2_INVALID	Invalid access. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
17	IRQ_CTX1_INVALID	Invalid access. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
16	IRQ_CTX0_INVALID	Invalid access. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
15	IRQ_CTX7_DONE	Context has been fully transferred to the TILER Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
14	IRQ_CTX6_DONE	Context has been fully transferred to the TILER Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
13	IRQ_CTX5_DONE	Context has been fully transferred to the TILER Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
12	IRQ_CTX4_DONE	Context has been fully transferred to the TILER Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
11	IRQ_CTX3_DONE	Context has been fully transferred to the TILER Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
10	IRQ_CTX2_DONE	Context has been fully transferred to the TILER Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
9	IRQ_CTX1_DONE	Context has been fully transferred to the TILER Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
8	IRQ_CTX0_DONE	Write mode: Context has been fully transferred to the TILER Read mode: Context prefetch has completed. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
7:2	RESERVED		R	0x00
1	IRQ_INVALID	Invalid access to the virtual space Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
0	IRQ_OCP_ERR	OCP error received from OCP master port. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0

Table 8-254. Register Call Summary for Register BTE_HL_IRQENABLE_CLR

ISS Interfaces

- ISS BTE Interrupts: [0]
- ISS BTE Registers: [1]

Table 8-255. BTE_CTRL

Address Offset	0x0000 0030		
Physical Address	0x5200 2030	**Instance**	ISS_BTE
Description	BTE control register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BW_LIMITER								RESERVED								BASE								RESERVED		POSTED	RESERVED	TAG_CNT			

Bits	Field Name	Description	Type	Reset
31:22	BW_LIMITER	Minimum number of OCP cycles between two consecutive buffer flushing or prefetch requests. Used to limit the bandwidth used to fill/empty buffers. 0: Maximum speed. Up to 1 request every 8 cycles (3.2GB @ 200 MHz) 1: Up to 1 request every 9 cycles. 1023: Minimum speed. Up to 1 request every 1031 cycles (24MB @ 200 MHz)	RW	0x000
21:12	RESERVED		R	0x000
11:8	BASE	Base address of the virtual space translated by the BTE. Start address = BASE*512MB End address = (BASE+1)*512MB 1 For example: BASE=3 = 0x 0 6000 0000 - 0x 0 7FFF FFFF	RW	0x0
7:6	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
5	POSTED	Select among posted and nonposted writes for translated requests. 0x0: Use non posted writes 0x1: Use posted writes	RW	0
4	RESERVED		R	0
3:0	TAG_CNT	BTE could use up to TAG_CNT+1 tags on OCPO. There could only be one outstanding request per tag. TAG_CNT does not control the number of requests it could handle on OCPI. This register is internally shadowed. Modifications are taken into account when there are no outstanding transactions on OCPO. TAG ID 0 to TAG_CNT are used on OCPO.	RW	0xF

Table 8-256. Register Call Summary for Register BTE_CTRL

ISS Interfaces
- ISS BTE Functional Description Details: [0] [1] [2] [3] [4]
- ISS BTE Registers: [5]

Table 8-257. BTE_CTRL1

Address Offset	0x0000 0034		
Physical Address	0x5200 2034	**Instance**	ISS_BTE
Description	BTE control register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RESP_FIFO_THR							

Bits	Field Name	Description	Type	Reset
31:7	RESERVED		R	0x0000000
6:0	RESP_FIFO_THR	The BTE stops accepting new requests from OCPI (on a clean burst boundary) when the response FIFO contains more than RESP_FIFO_THR words. The reset value is FIFO_SIZE - 16 - 1. FIFO_SIZE = 8 * $2^{\overline{RESPFIFO}}$	RW	0x0F

Table 8-258. Register Call Summary for Register BTE_CTRL1

ISS Interfaces
- ISS BTE Registers: [0]

Table 8-259. BTE_CONTEXT_CTRL_i

Address Offset	0x0000 0040 + (0x20 * i)	**Index**	i = 0 to 7
Physical Address	0x5200 2040 + (0x20 * i)	**Instance**	ISS_BTE
Description	Context control register		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TRIGGER								INITSX	INITSY		ADDR32	AUTOFLUSH	ONESHOT	GRID		MODE		RESERVED			FLUSH	STOP	START

Bits	Field Name	Description	Type	Reset
31:30	RESERVED		R	0x0
29:16	TRIGGER	Threshold used to trigger translated requests to OCPO. Unit: words or 16 bytes Valid range: 3 lines + 2 ... 4 lines WRITE: a 2D write is issued to OCPO when the internal buffer level (including masked accesses) is superior or equal to TRIGGER READ: a 2D read is issued to OCPO when the internal buffer level (including masked accesses) is inferior to TRIGGER.	RW	0x0000
15	INITSX	Reset value to be used for SX__x. Check the section describing the local buffer management for details.	RW	0
14:13	INITSY	Reset value to be used for SY__x. Check the section describing the local buffer management for details.	RW	0x0
12	ADDR32	Controls the value of the OCP address bit 32 to be used for translated accesses	RW	1
11	AUTOFLUSH	Controls automatic context flushing when an IDLE request is received 0x0: Disabled 0x1: Enabled	RW	0
10	ONESHOT	Selects one-shot or continuous mode 0x0: The context is automatically re-enabled when its end is reached. 0x1: The context is disabled when the end of a frame has been reached.	RW	0
9:8	GRID	Grid used to access the TILER 0x0: Stride = 16k Subtile = 4x4 bytes Tile = 32x32 bytes 0x1: Stride = 8k Subtile = 4x4 bytes Tile = 32x32 bytes 0x3: Stride = 16k Subtile = 8x2 bytes Tile = 64x16 bytes 0x2: Stride = 32k Subtile = 8x2 bytes Tile = 64x16 bytes	RW	0x0
7:6	MODE	Select the translation mode for the context 0x0: Write translation 0x1: Read translation 0x3: reserved 0x2: Direct access to local buffer	RW	0x0
5:3	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
2	FLUSH	Flushes all remaining data of the context to the TILER. Write 0x0: No effect Write 0x1: Flush	W	0
1	STOP	Stops the context on a clean OCP transaction boundary. Write 0x0: No effect Write 0x1: Stop the context	W	0
0	START	Resets the contexts internal state and enables the context on a clean OCP transaction boundary. Write 0x0: No effect Write 0x1: Reset + Enable	W	0

Table 8-260. Register Call Summary for Register BTE_CONTEXT_CTRL_i

ISS Interfaces

- ISS BTE PRCM Interface: [0] [1]
- ISS BTE Functional Description Details: [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [17] [18] [19] [20] [21] [22] [23]
- ISS BTE Context Configuration: [24] [25] [26]
- ISS BTE Change Context Configuration: [27] [28] [29] [30]
- ISS BTE Registers: [31]

Table 8-261. BTE_CONTEXT_BASE_i

Address Offset	0x0000 0044 + (0x20 * i)	**Index**	i = 0 to 7
Physical Address	0x5200 2044 + (0x20 * i)	**Instance**	ISS_BTE
Description	Address of the frame buffer in the TILER address space.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR																														RESERVED	

Bits	Field Name	Description	Type	Reset
31:5	ADDR	Address	RW	0x0000000
4:0	RESERVED		R	0x00

Table 8-262. Register Call Summary for Register BTE_CONTEXT_BASE_i

ISS Interfaces

- ISS BTE Functional Description Details: [0] [1] [2]
- ISS BTE Context Configuration: [3] [4]
- ISS BTE Registers: [5]

Table 8-263. BTE_CONTEXT_START_i

Address Offset	0x0000 0048 + (0x20 * i)	**Index**	i = 0 to 7
Physical Address	0x5200 2048 + (0x20 * i)	**Instance**	ISS_BTE
Description	Top-left corner of the context.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																X								RESERVED							

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Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:7	X	Address, in 128-byte words	RW	0x000
6:0	RESERVED		R	0x00

Table 8-264. Register Call Summary for Register BTE_CONTEXT_START_i

ISS Interfaces
- ISS BTE Functional Description Details: [0] [1] [2] [3] [4] [5]
- ISS BTE Registers: [6]

Table 8-265. BTE_CONTEXT_END_i

Address Offset	0x0000 004C + (0x20 * i)	**Index**	i = 0 to 7
Physical Address	0x5200 204C + (0x20 * i)	**Instance**	ISS_BTE
Description	Bottom-right corner of the context.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								Y								X												RESERVED			

Bits	Field Name	Description	Type	Reset
31:29	RESERVED		R	0x0
28:16	Y	Last line number for the context (0 corresponds to a context of 1 line)	RW	0x0000
15:4	X	Address, in 128-bit words, of the last column of the context	RW	0x000
3:0	RESERVED		R	0x0

Table 8-266. Register Call Summary for Register BTE_CONTEXT_END_i

ISS Interfaces
- ISS BTE Functional Description Details: [0] [1] [2] [3] [4] [5] [6] [7] [8]
- ISS BTE Registers: [9]

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8.2.8 ISS CBUFF

8.2.8.1 ISS CBUFF Environment

There are no particular environment attributes. See Section 8.2.2, *ISS Interfaces Environment*.

8.2.8.2 ISS CBUFF Integration

Figure 8-91 shows the integration of the CBUFF in the ISS. Because the CBUFF maps a virtual memory space from the physical memory, it therefore communicates with the ISS ISP and ISS interface modules for data to and from memory. This figure shows the normal data flow for further processing by the ISP and/or still-image coprocessor (SIMCOP) (in green) and the stall functionality of CBUFF (in red), which stall the data for a certain amount of time. An example of stalling is when the ISP processes the data faster than the input from CCP2 to memory. The CBUFF then must stall the data flow until a sufficient amount of data can be read from memory by the ISP.

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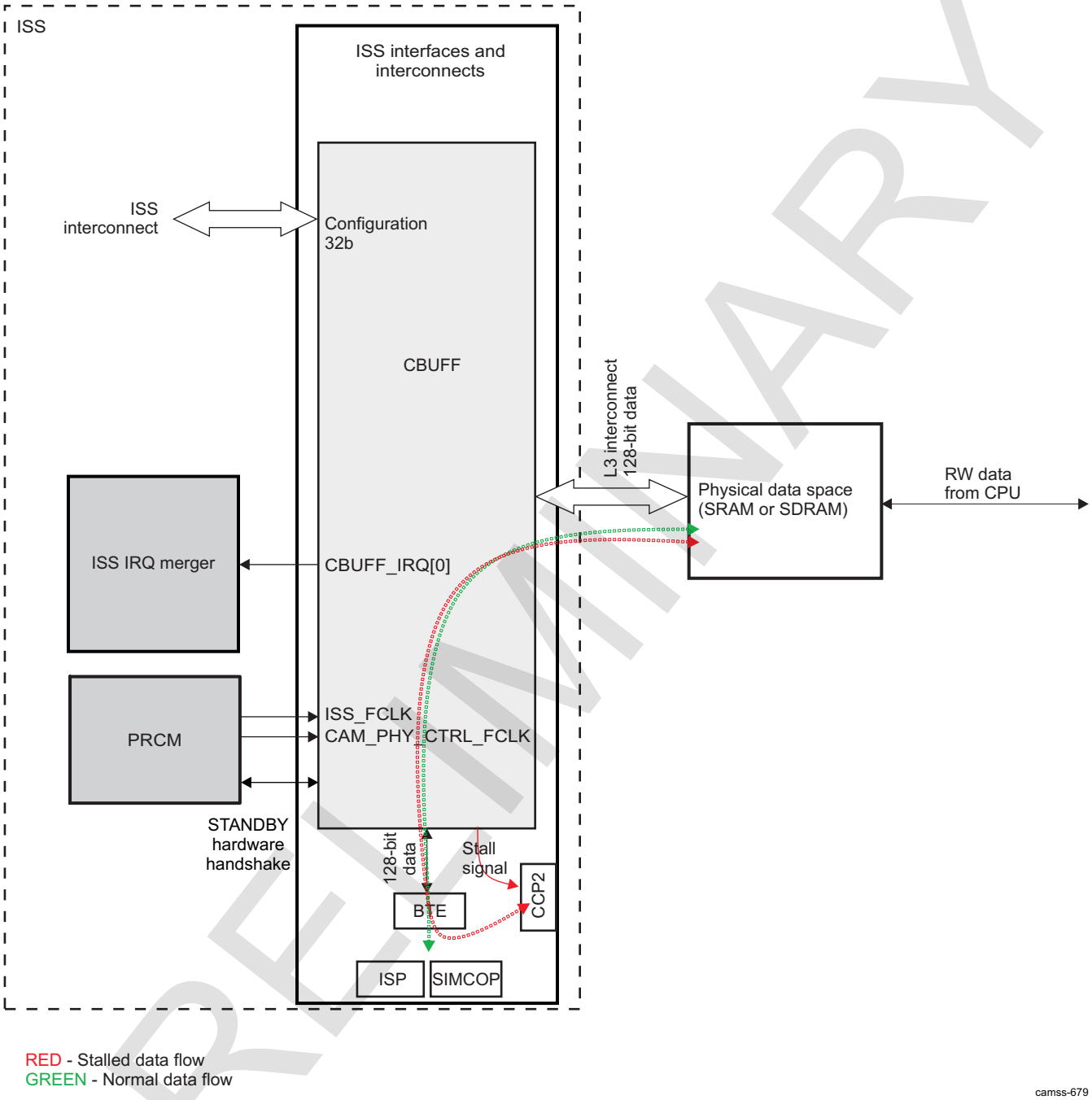
Figure 8-91. ISS CBUFF Integration



For power domain, clocks, reset, and hardware requests, see Section 8.1.2.4, *ISS Power Management*.

8.2.8.2.1 ISS CBUFF PRCM Interface

8.2.8.2.1.1 ISS CBUFF Reset and Idle Mechanism

A reset signal is provided by the PRCM module to the top-level ISS power and clock-management module.

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For standby, when none of the ISS modules require CBUFF execution actions, ISS PM executes the standby sequence, which reaches the CBUFF. When an IDLE request arrives, the CBUFF data is drained. After all transactions are drained, the CBUFF acknowledges the IDLE request to the ISS PM/CM. The IDLE request/acknowledge steps are:

When an IDLE request is received in smart-idle mode:

1. CBUFF stops accepting any new OCP requests on a clean OCP transaction boundary.
2. Waits until the interrupt output becomes inactive (no more enabled event pending)
3. Waits until all outstanding OCP transactions are complete on OCPO and OCPI. CBUFF keeps track of issued requests, data phases, and responses for that purpose.
4. CBUFF disconnects the OCPO port.
5. CBUFF acknowledges the IDLE request.

When a wake-up request is received in smart-idle mode:

1. CBUFF connects the OCPO port.
2. Starts accepting new requests from OCPI
3. Acknowledges the functional state

Idle mode is controlled through the CBUFF_HL_SYSCONFIG[3:2] IDLEMODE bit field. For software reset, it is recommended to use the global ISS reset; if a reset is required, it can be set from the CBUFF_HL_SYSCONFIG[0] SOFTRESET bit.

8.2.8.2.2 ISS CBUFF Interrupts

All events generated by the module are merged into a single event at ISS level. This event can be mapped to the MPU subsystem by enabling the ISS_HL_IRQENABLE_SET_i[10] CBUFF_IRQ bit. Table 8-267 lists the procedure to manage CBUFF interrupts.

Table 8-267. ISS CBUFF Interrupt Management

Description	Bit Field	Value
Each event that generates an interrupt can be individually enabled by setting the appropriate bit.	CBUFF_HL_IRQENABLE_SET	
Each event that generates an interrupt can be individually disabled by setting the appropriate bit.	CBUFF_HL_IRQENABLE_CLR	
When an event occurs, the corresponding bit in the CBUFF_HL_IRQSTATUS_RAW register is set regardless of whether or not the event is enabled. Bits in the CBUFF_HL_IRQSTATUS registers are only set only when an enabled event occurs	CBUFF_HL_IRQSTATUS_RAW and CBUFF_HL_IRQSTATUS	
Software can clear a pending event by setting the appropriate bit in the CBUFF_HL_IRQSTATUS register.	CBUFF_HL_IRQSTATUS	

The CBUFF can generate three events per context and one global event. All events are merged into one physical interrupt line. Table 8-268 describes the CBUFF-generated events.

Table 8-268. ISS CBUFF-Generated Events

Event	Description
IRQ_CTXx_READY	Read mode: CPU can write data to the physical window pointed by CBUFF_CTX_STATUS_i[3:0] WB.
	Write mode: CPU can read data from the physical window pointed by CBUFF_CTX_STATUS_i[3:0] WB.
	Read/write mode: The OCPI initiator has completed writing a physical window.
IRQ_CTXx_INVALID	Invalid access
	OCPI writes the virtual space of context i in read mode.
	OCPI reads the virtual space of context i in write mode.
	OCPI writes the virtual space of context i outside the CBUFF_CTX_STATUS_i[11:8] WA window in write or read/write mode.

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Table 8-268. ISS CBUFF-Generated Events (continued)

Event	Description
	OCPI reads the virtual space of context i outside the CBUFF_CTX_STATUS_i[11:8] WA window in read mode.
	OCPI reads the virtual space of context i outside the CBUFF_CTX_STATUS_i[3:0] WB window in read/write mode.
	CPU writes the DONE bit when physical windows are not ready for the CPU.
	This event indicates a wrong configuration of the CBUFF, the OCPI initiator or bogus software. When it happens, context i goes into an error state. In this state all accesses to the virtual space of context i are cancelled: they are not forwarded to the physical space. The purpose is to prevent corruption of the physical memory. Of course, the CBUFF still returns OCP responses to OCPI to ensure the integrity of the OCP.
	The error state can be left by disabling the context i and re-enabling it. Before doing so, software must ensure that there are no more outstanding requests to the virtual space of context i.
IRQ_CTXx_OVR	Physical space overflow or underflow event This event indicates a bandwidth mismatch between data producer and data consumer. When it happens, context i does not go into error state. However, the data in the physical space is likely to be corrupted.
IRQ_OCP_ERR	OCP error received in the OCPO master port. The OCP response is forwarded to OCPI normally.

8.2.8.3 ISS CBUFF Functional Description

The CBUFF maps a virtual space to a physical space by address translation. It does not change the data or store it locally.

8.2.8.3.1 ISS CBUFF Features

The ISS CBUFF features are:

- Fully transparent for accesses out of the configured virtual space
- Three functional modes:
  - Read mode: Read requests received from OCPI and forwarded after translation to OCPO. Writes are handled by an external process and acknowledged by the CPU.
  - Write mode: Write request received from OCPI and forwarded after translation to OCPO. Reads are handled by an external process and acknowledged by the CPU.
  - Read/write mode: Read and write requests received from OCPI and forwarded after translation to OCPO
- Four independent contexts
- Virtual address space (linear) mapped into a physical space (circular)
- Maximum physical buffer size of 16 × 16MB:
  - Physical space consists of 2, 4, 8, or 16 windows.
  - Maximum allowed window size is 16MB.
- Support of 2D addressing modes
- Strong error detection mechanisms to prevent data corruption caused by bogus configuration
- Addresses are 128-bit aligned, but window fill level managing is byte accurate
- Bandwidth control feedback loop to stall in initiator connected to OCPI

8.2.8.3.2 ISS CBUFF Functional Description

The CBUFF maps a virtual address space to a physical space also called circular buffer.

The CBUFF can handle up to eight contexts. For most data formats, primarily four contexts are used. In cases where YUV4:2:0 data is exchanged, two contexts are consumed by the SIMCOP (JPEG encode) coming from the resizer module, which is the ISP output module. Moreover, a context is a virtual full-frame buffer that maps to a configurable number of physical windows.

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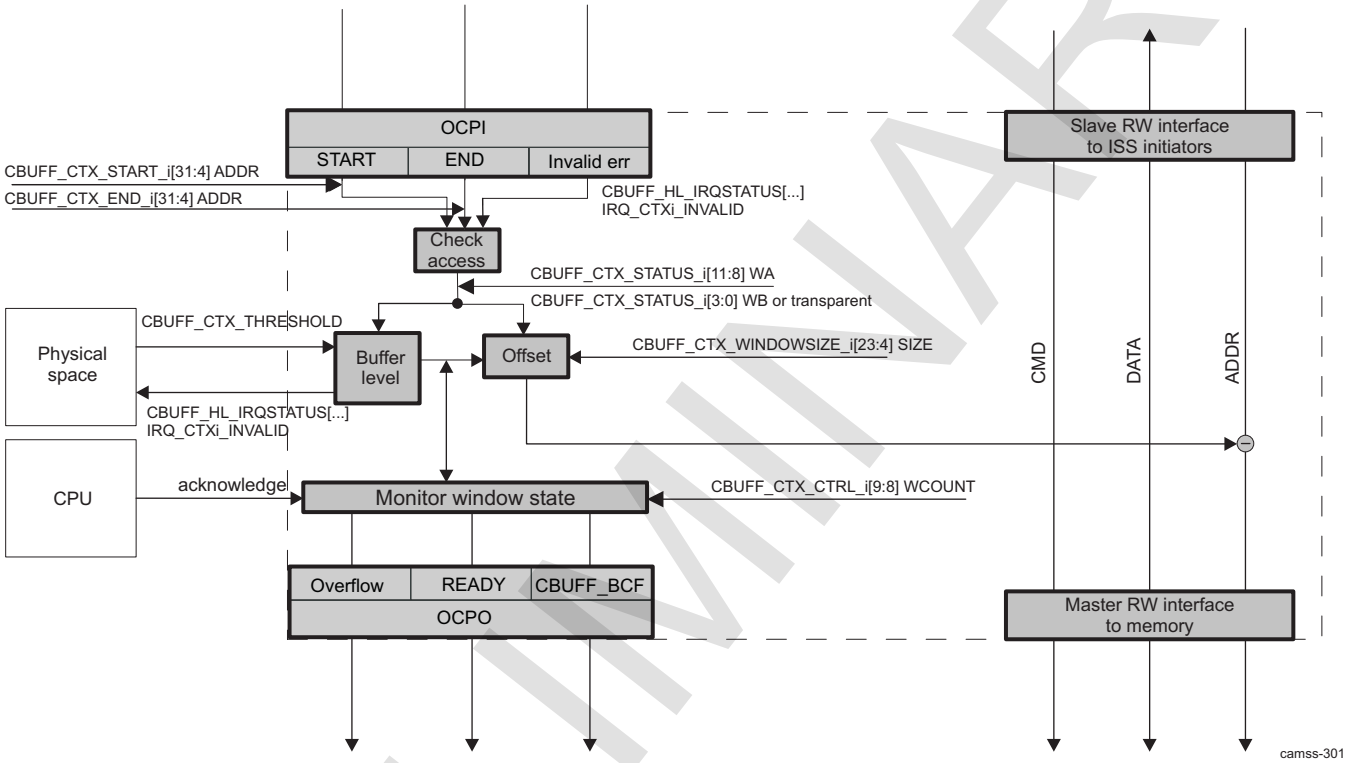
This section gives an overview of typical uses of the CBUFF.

8.2.8.3.2.1 ISS CBUFF Top-Level Diagram

Figure 8-92 shows the functional principle diagram. It does not include an exhaustive list of the interface signals or internal status registers.

A more detailed functional description is provided in the following sections.

Figure 8-92. ISS CBUFF Top-Level Diagram



8.2.8.3.2.2 ISS CBUFF Functional Modes

The CBUFF supports three functional modes (see Table 8-269).

Table 8-269. ISS CBUFF Functional Modes

Mode	Data Written by	Data Read by
Write mode	ISS initiator	CPU-controlled process
Read mode	CPU-controlled process	ISS initiator
Read/write mode	ISS initiator	ISS initiator

8.2.8.3.2.2.1 ISS CBUFF Write Mode

In write mode, the physical space is written by the CBUFF and it is read by the CPU. An IRQ_CTXx_READY event is set each time a physical window is available to be read by the CPU. This happens when the CBUFF_CTX_STATUS_i[11:8] WA pointer is moved by the CBUFF.

The CBUFF sets an IRQ_CTXx_READY event to inform the CPU that it can access the CBUFF_CTX_STATUS_i[3:0] WB physical window. The CBUFF cannot monitor CPU accesses to the physical window. The CPU must indicate when it has completed the processing of the CBUFF_CTX_STATUS_i[3:0] WB window by setting the CBUFF_CTX_CTRL_i[2:1] DONE bit field. This increments the window index CBUFF_CTX_STATUS_i[3:0] WB by one modulo the window count (defined by the CBUFF_CTX_CTRL_i[9:8] WCOUNT bit field).

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The CBUFF ensures that one IRQ_CTXx_READY event is sent to the CPU per physical window to be read. In other words, when a new IRQ_CTXx_READY event occurs before the previous one(s) is acknowledged by the CPU, it is not lost. The CBUFF memorizes the event and triggers the interrupt line again when the CPU clears it.

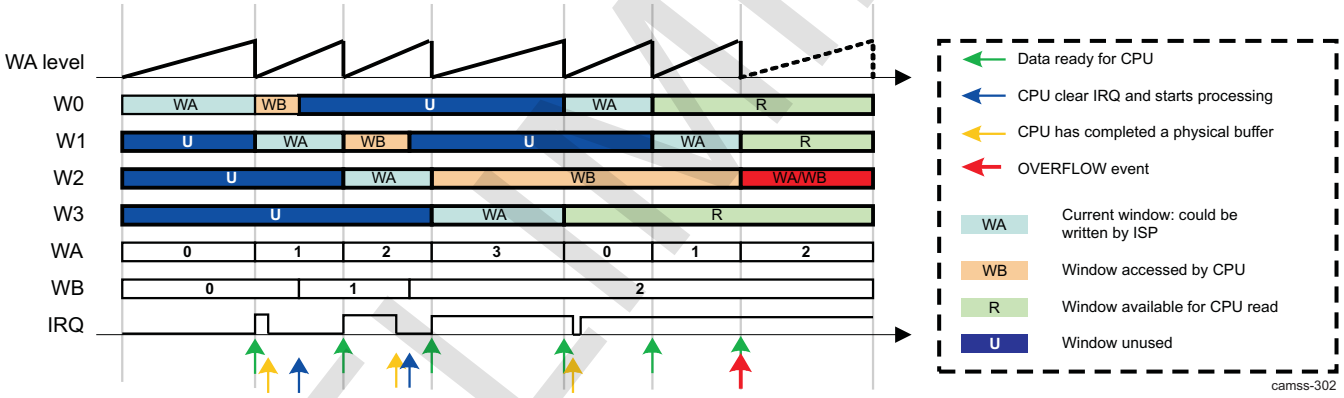
When the CPU reads the physical space too slowly, the CBUFF_CTX_STATUS_i[11:8] WA window pointer falls into the CBUFF_CTX_STATUS_i[3:0] WB window. This generates an IRQ_CTXx_OVR event when the OCPI initiator performs an access to that window. The CPU receives the IRQ_CTXx_READY event only if it is allowed to access a physical window. Therefore, it cannot generate an IRQ_CTXx_OVR event in a normal case. The OCPI initiator accesses are tracked based on activity on the OCP port.

When an IRQ_CTXx_OVR event occurs, the buffer content is likely to be corrupted. However, the CBUFF context continues processing data normally; it does not go into error state. Software must reset data generation and the CBUFF in a clean manner.

Figure 8-93 shows an example scenario with CBUFF_CTX_CTRL_i[9:8] WCOUNT = 1 (four windows). In normal operation, the CPU processes data at least at the same speed as it is written to the physical space. When this is not true, the number of windows to be read by the CPU increases. When no more physical windows are available for OCPI writes, an overflow occurs.

In the previous example, the CPU takes more time than expected to read the third buffer. Therefore, physical windows are not freed up. The OPCI initiator continues to write data into the physical window. That leads to an overflow when the OCPI initiator writes into the physical window that is read by the CPU (CBUFF_CTX_STATUS_i[11:8] WA = CBUFF_CTX_STATUS_i[3:0] WB and writes into CBUFF_CTX_STATUS_i[11:8] WA detected).

Figure 8-93. ISS CBUFF Write Mode CPU Interaction Example



(1) When there is no physical window available to be read by the CPU and the CPU writes the DONE bit, an IRQ_CTXx_INVALID event occurs.

(2) The bandwidth control feedback (BCF) feature can be used to prevent overflow. It must be supported by the module writing data into the virtual space (typically, an ISS).

8.2.8.3.2.2.2 ISS CBUFF Read Mode

In read mode, the physical space is read by the CBUFF and it is written by the CPU. An IRQ_CTXx_READY event is set each time a physical window is available to be written by the CPU. This is true until all free buffers are used.

The CBUFF sets an IRQ_CTXx_READY event to inform the CPU that it can write the CBUFF_CTX_STATUS_i[3:0] WB window. The CBUFF cannot monitor CPU accesses to the physical space. It must indicate when it completes writing the CBUFF_CTX_STATUS_i[3:0] WB window by setting the CBUFF_CTX_CTRL_i[2:1] DONE bit field. This increments the CPU window index CBUFF_CTX_STATUS_i[3:0] WB by one modulo the window count (defined by the CBUFF_CTX_CTRL_i[9:8] WCOUNT bit field).

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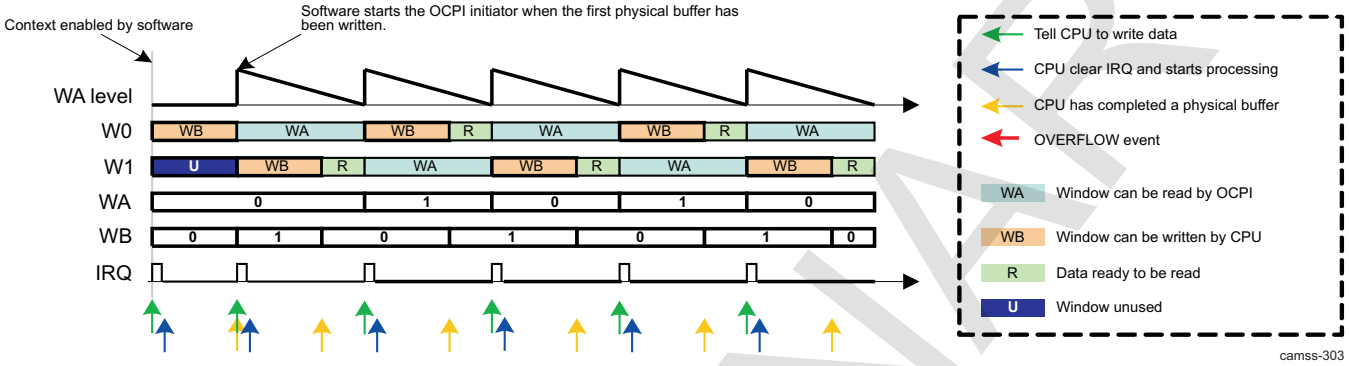
The CBUFF ensures that one IRQ_CTXx_READY event is sent to the CPU per physical window to be written. In other words, when a new IRQ_CTXx_READY event occurs before the previous one(s) is acknowledged by the CPU, it is not lost. The CBUFF memorizes the event and triggers the interrupt line again when the CPU clears it.

The following is an example of a normal operation in which the CPU writes data faster than it is read by the OCPI initiator. Figure 8-94 uses two physical windows (CBUFF_CTX_CTRL_i[9:8] WCOUNT = 0).

Figure 8-94. ISS CBUFF CPU Writes Data Faster Than it Is Read by the OCPI Initiator



Software must enable the ISS initiator only when at least one window is written by the CPU. Otherwise, an OVERFLOW event occurs when BCF is not used.

The CPU receives an interrupt each time a physical window is available to receive data. It clears the interrupt and then starts filling the physical window. When the buffer is completely written, it sets the CBUFF_CTX_CTRL_i[2:1] DONE bit field. This happens before the OCPI initiator has read all data from the previous physical window: the CPU must wait until the next IRQ_CTXx_READY event is received before it can write again to the physical space.

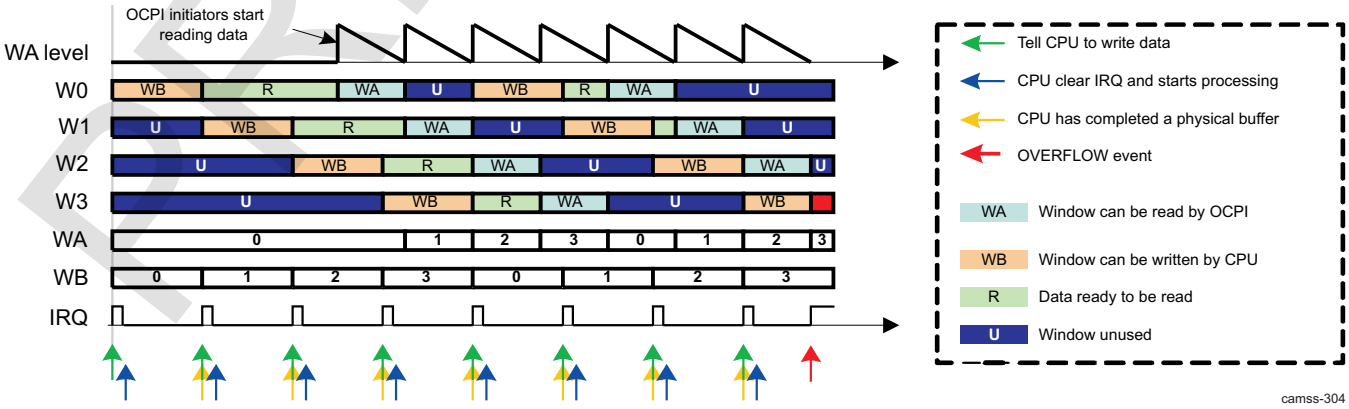
When the CPU writes buffers too slowly, the CBUFF_CTX_STATUS_i[11:8] WA window falls into the CBUFF_CTX_STATUS_i[3:0] WB window. This generates an IRQ_CTXx_OVR event only when the OCPI initiator performs reads to that window. The CPU receives the IRQ_CTXx_READY event only if it is allowed to access a physical window. Therefore, it does not generate an IRQ_CTXx_OVR event in a normal case. ISS accesses are tracked based on activity on the OCPI port.

When no buffer is available to be written by the CPU and the CPU writes the DONE bit, an IRQ_CTXx_INVALID event occurs.

When an IRQ_CTXx_OVR event occurs, the OPCI initiator reading the virtual space is likely to receive dummy data. However, the CBUFF context continues to process data normally; it does not go into error state. Software must reset the data consumer (OCPI initiator) and CBUFF context in a clean manner.

Figure 8-95 is an example of CBUFF read mode CPU interaction.

Figure 8-95. CBUFF Read Mode CPU Interaction Example



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The BCF feature can be used to prevent overflow. It must be supported by the module reading data from the virtual space (typically, an ISS).

8.2.8.3.2.2.3 ISS CBUFF Read/Write Mode

Reads and writes are performed by OCPI initiators such as a camera interface, ISP, or SIMCOP. Address translation is performed for read and write data flows. The WA pointer is used for the write data flow, and the WB pointer is used for the read data flow. Therefore, address translation for the write data flow is the same as for write mode.

In this mode, the OCPI read data flow is stalled when there is not enough data to read in the physical space. A typical application is to store data from the camera in a CBUFF and to read it back by the ISP. When the camera is slower than the ISP, the ISP stalls.

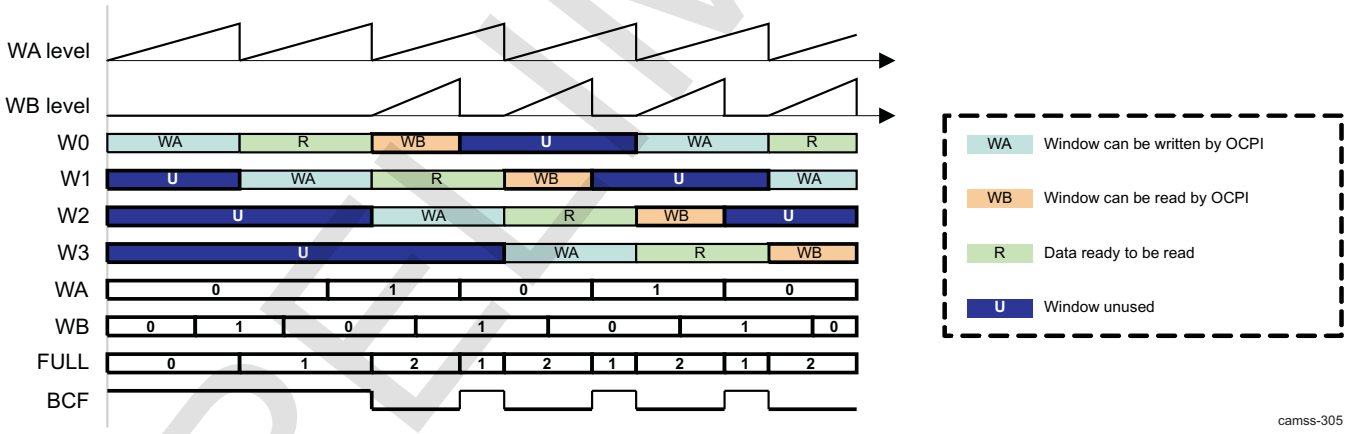
This mode does not rely on CPU synchronization. Synchronization is always performed using the BCF hardware mechanism. IRQ_CTXx_READY events are triggered in this mode when the OPCI write initiator has filled a physical window. Software can use this event for debug or performance bench marking purposes. Writes to the CBUFF_CTX_CTRL_i[2:1] DONE bit field are ignored in this mode.

The IRQ_CTXx_OVR event is triggered when an underflow occurs. In a normal case this should not occur, because the BCF signal is used to stall the read data flow when insufficient data is available in the physical space.

Figure 8-96 assumes:

- Read/write mode
- Four physical windows
- CBUFF_CTX_THRESHOLD_S_i = CBUFF_CTX_THRESHOLD_F_i
- The OCPI read initiator is faster than the OCPI write initiator. The BCF feature is used to stall the read initiator. CBUFF_CTX_CTRL_i[7:4] BCF = 2

Figure 8-96. ISS CBUFF Read/Write Mode Example



8.2.8.3.2.3 ISS CBUFF Events and Status Checking

8.2.8.3.2.3.1 ISS CBUFF Operations

A CBUFFx_READY_IRQ event is generated each time the CPU can read data from the CBUFF. The CPU can clear the event when it starts processing the data to avoid masking other events. The CPU can keep track of the location on the data internally or use the CBUFF registers to compute it.

The formula used is: ADDR = CBUFF_CTX_STATUS_i[3:0] WB CBUFF_CTX_WINDOWSIZE_i + CBUFF_CTX_PHY_i

When the CPU is done with processing, it must free the buffer by setting the CBUFF_CTX_CTRL_i[10] DONE bit. Otherwise, an overflow event may occur.

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The CBUFF does not keep track of EOF events. They must be managed by the CPU using the EOF event of the module that writes into the CBUFF. At the EOF, data may remain in the current write windows. For example, when the window size is set to 8 lines and the image size is 20 lines, only two window-ready events are generated for a linear addressing scheme. The remaining four lines can be read after the EOF event.

No automatic reset of the CBUFF FSM occurs at the end of the image frame. Software must reset the context by clearing the CBUFF_CTX_CTRL_i[0] ENABLEABLE bit when the frame is completely processed. A new frame can start only when the CBUFF_CTX_CTRL_i[0] ENABLEABLE bit is set.

8.2.8.3.2.3.2 ISS CBUFF Status Checking

The CBUFF provides read-only access to the CBUFF_CTX_STATUS_i[11:8] WA and CBUFF_CTX_STATUS_i[3:0] WB pointers through the CBUFF_CTX_STATUS_i register. For example, the CBUFF_CTX_STATUS_i[3:0] WB index can be used by the CPU to compute the address of a physical window. Those indexes can also be used to evaluate latency margins.

8.2.8.3.2.3.3 ISS CBUFF Register Accessibility During Frame Processing

All registers are busy-writeable registers. These registers/fields can be read or written even if the module is busy. Changes to the underlying settings occur instantly. However, module behavior is unpredictable when registers are changed during processing.

For correct operation, software must:

1. Disable all accesses to the virtual space managed by the context.
2. Disable the context by clearing the CBUFF_CTX_CTRL_i[0] ENABLEABLE bit.
3. Change the configuration.
4. Re-enable CBUFFx by setting the CBUFF_CTX_CTRL_i[0] ENABLEABLE bit.

8.2.8.3.2.4 ISS CBUFF Memory-to-Memory Operation BCF

The BCF mechanism matches the bandwidth between two processes.

The BCF feature can be used in all three CBUFF modes:

- Read mode: A CPU-controlled process writes data into physical space. The BCF signal is deasserted when the physical space contains enough data to start the read initiator connected to OCPI.
- Write mode: The BCF signal controls the write initiator connected to OCPI. When the CPU-controlled process does not read the data fast enough from the physical space, the BCF signal is asserted to stall filling of the buffer. It is deasserted when enough space is available in the physical space.
- Read/write mode: The BCF signal controls the read initiator connected to OCPI. Another initiator connected to OCPI fills the physical space. The BCF signal is deasserted when the physical space contains data that can be read by the read initiator. It is deasserted when insufficient data is available in the physical space.

The CBUFF_BCF output is controlled based on two factors:

- The window count available for the OCPI initiator to read/write
- The amount of data in the last available window (pretrigger)

The CBUFF_BCF signal is enabled by the CBUFF_CTX_CTRL_i[7:4] BCF bit field. It defines:

- Write mode: The amount of required free windows to allow writing from the ISS. In other words, when less than the required amount of BCF windows is available for ISS writes, the stall mechanism is triggered. The number of free windows is initialized to the total window count of the context. It is decreased by 1 each time the OCPI initiator finishes writing a window. It is increased by 1 each time the CPU finishes reading a window.
- Read and read/write modes: The minimum amount of required full windows to allow reading from the OCPI. When fewer than CBUFF_CTX_CTRL_i[7:4] BCF windows are available for ISS read, the stall mechanism is triggered. The number of full windows is initialized to 0. It is decreased by 1 each time the OCPI initiator completes reading a window. It is increased by 1 each time the CPU/OCPI initiator finishes writing a window.

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Figure 8-97 is an example of BCF use. It assumes:

- Write mode: OCPI writes data into physical space and the CPU reads it.
- Two physical windows
- CBUFF_CTX_THRESHOLD_S_i = CBUFF_CTX_THRESHOLD_F_i
- The OCPI write initiator is faster than the CPU.
- CBUFF_CTX_CTRL_i[7:4] BCF = 1

Figure 8-97. ISS CBUFF Write Mode CPU Interaction Example BCF Used

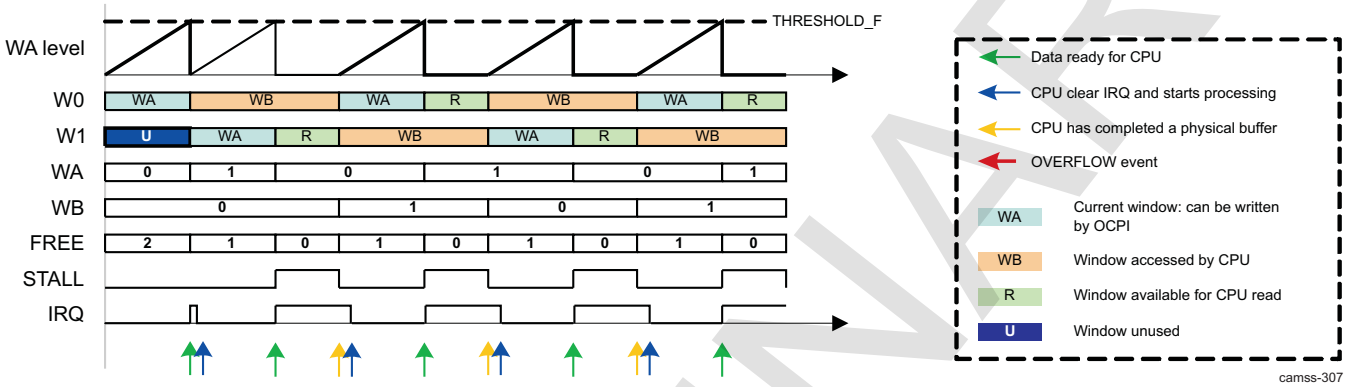

Figure 8-98 is another example. It assumes:

- Read mode: The CPU writes data into physical space and the OCPI reads it.
- Four physical windows
- CBUFF_CTX_THRESHOLD_S_i = CBUFF_CTX_THRESHOLD_F_i
- The OCPI read initiator is faster than the CPU. It starts after the CPU.
- CBUFF_CTX_CTRL_i[7:4] BCF = 2

Figure 8-98. ISS CBUFF Read Mode CPU Interaction Example (1)

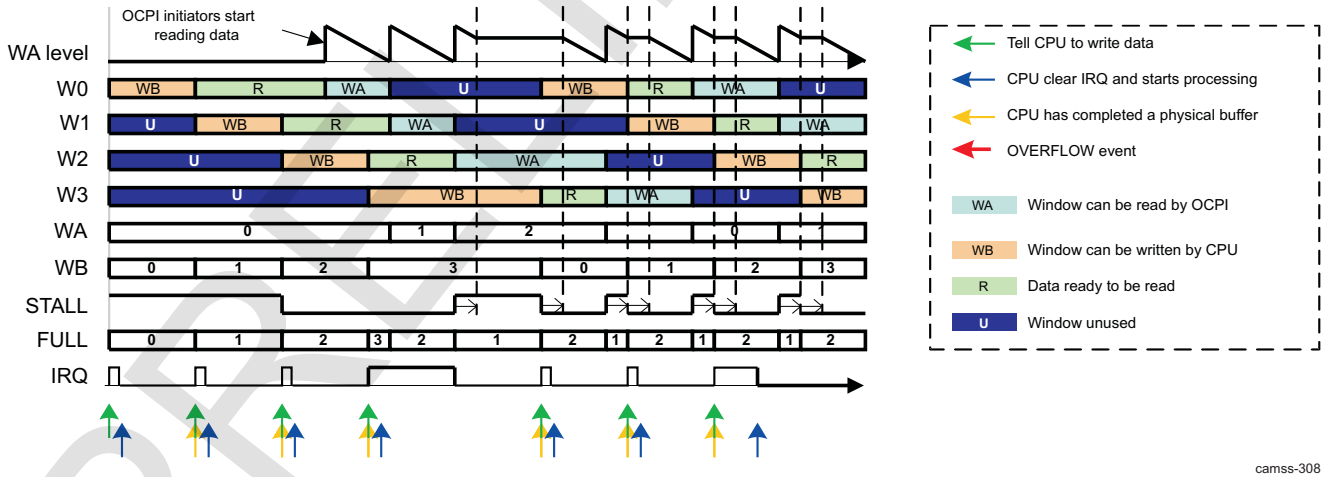

Figure 8-99 is another example. It assumes:

- Read mode: The CPU writes data into physical space and the OCPI reads it.
- Two physical windows
- CBUFF_CTX_THRESHOLD_S_i = CBUFF_CTX_THRESHOLD_F_i
- The OCPI read initiator is faster than the CPU. It starts after the CPU.
- CBUFF_CTX_CTRL_i[7:4] BCF = 1

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Figure 8-99. ISS CBUFF Read Mode CPU Interaction Example (2)

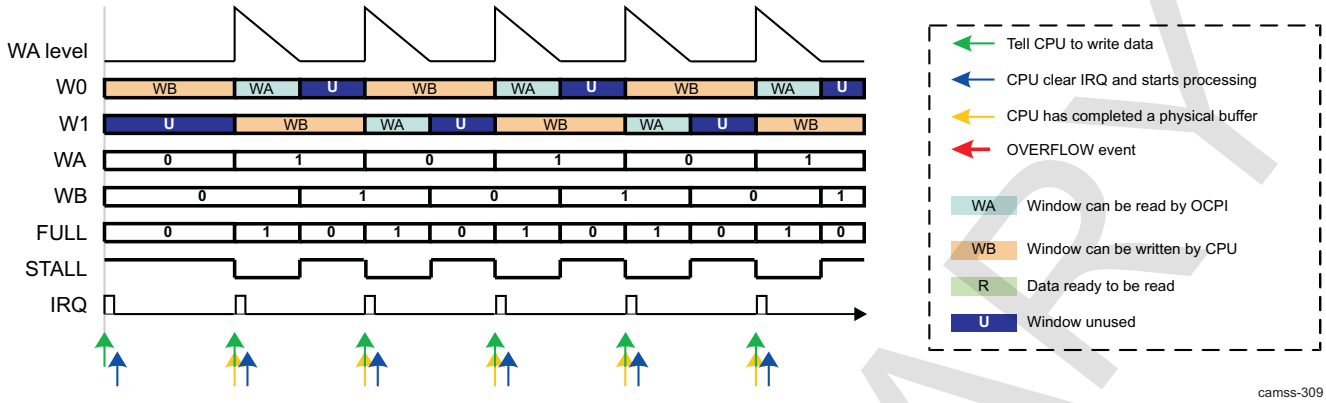

Figure 8-100 is another example. It assumes:

- Read mode: The CPU writes data into physical space and the OCPI reads it.
- Four physical windows
- CBUFF_CTX_THRESHOLD_S_i = CBUFF_CTX_THRESHOLD_F_i
- The OCPI read initiator is faster than the CPU. It starts after the CPU.
- CBUFF_CTX_CTRL_i[7:4] BCF = 1

CBUFF supports pretriggering the BCF signal for finer latency compensation control. This mechanism is active only for the last window available for OCPI access. It typically improves the physical space use, which is particularly useful when on-chip SRAM is used as a ping-pong buffer.

Pretriggering is controlled through the CBUFF_CTX_THRESHOLD_S_i register. It defines:

- Write mode: When the fill level of the last window available for ISS writes is greater than or equal to CBUFF_CTX_THRESHOLD_S_i, the CBUFF_BCF signal is asserted.
- Read mode: When the amount of data in the last window available for ISS reads is less than CBUFF_CTX_THRESHOLD_F_i/CBUFF_CTX_THRESHOLD_S_i, the CBUFF_BCF signal is asserted.

BCF pretriggering is disabled by setting CBUFF_CTX_THRESHOLD_S_i = CBUFF_CTX_THRESHOLD_F_i.

Figure 8-100 is an example of BCF pretriggering, assuming the following:

- Write mode: The CPU reads data from the physical space and the OCPI writes it.
- Two physical windows
- CBUFF_CTX_THRESHOLD_S_i = 1/3 CBUFF_CTX_THRESHOLD_F_i
- CBUFF_CTX_CTRL_i[7:4] BCF = 1

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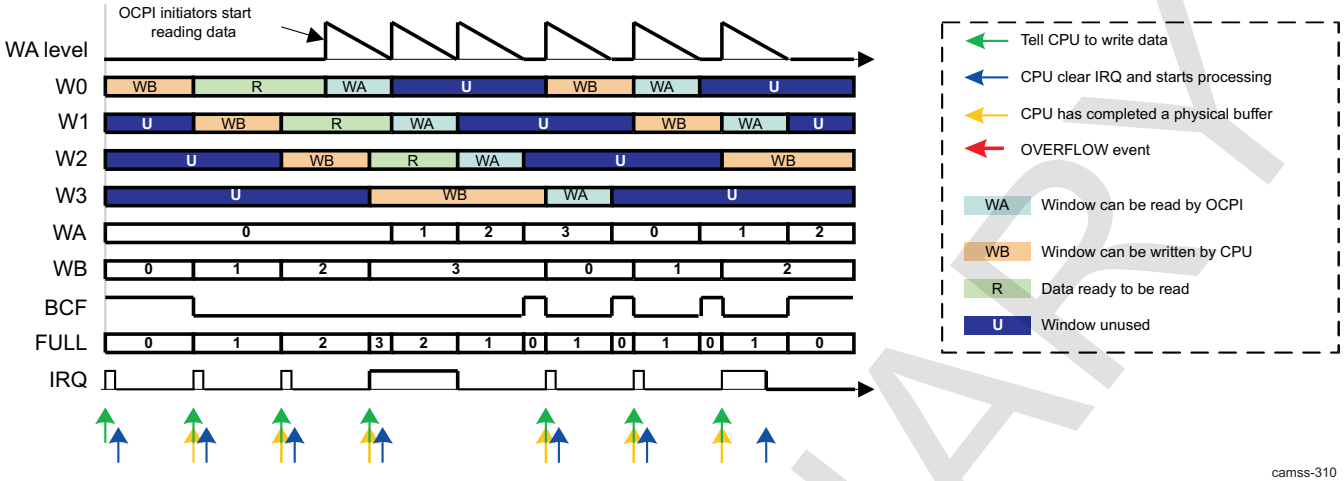
Figure 8-100. ISS CBUFF BCF Pretrigger Example: Write Mode

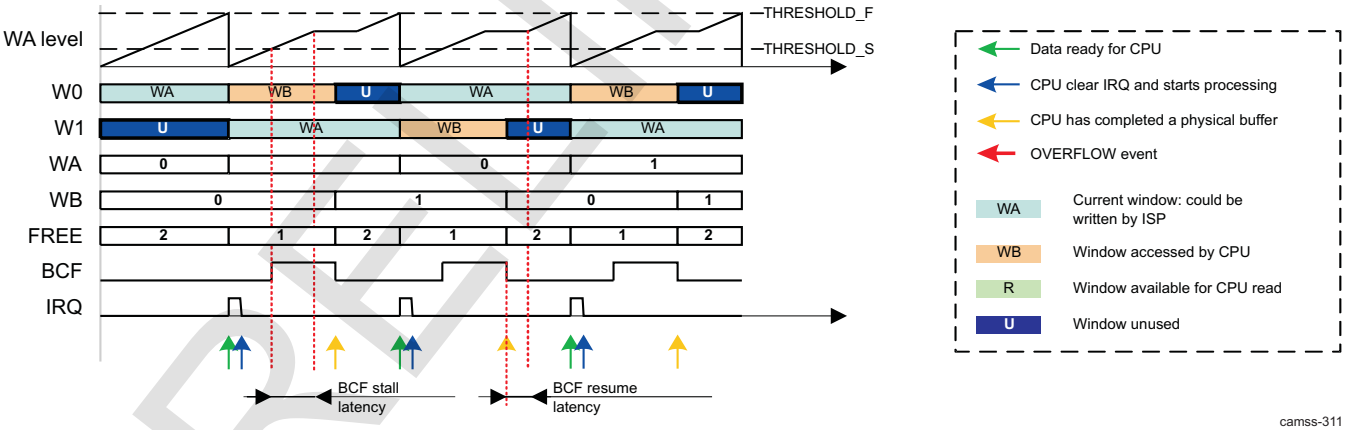


The CBUFF_BCF output signal is a logical OR of all internal BCF signals of CBUFF contexts. For example, when contexts 0 and 1 have enabled the BCF feature, both contexts can request a data flow stall.

Figure 8-101 is an example of pretriggering in read mode:

- Read mode: CPU writes data into the physical space and the OCPI reads it.
- Four physical windows
- CBUFF_CTX_THRESHOLD_S_i = 2/3 CBUFF_CTX_THRESHOLD_F_i
- The OCPI read initiator is faster than the CPU. It starts after the CPU.
- CBUFF_CTX_CTRL_i[7:4] BCF = 2

Figure 8-101. ISS CBUFF BCF Pretrigger Example: Read Mode



8.2.8.3.2.5 ISS CBUFF TILER Support

The CBUFF can translate 2D (BLOCK) bursts intended for the TILER. However, software must ensure that a given burst fits in a window.

The expected value for ADDR[32] is defined by the CBUFF_CTX_CTRL_i[11] TILERMODE bit.

- When ADDR[32] = CBUFF_CTX_CTRL_i[11] TILERMODE, the access is processed normally. ADDR[32] is not used for further processing.
- Otherwise, the access is treated as transparent.

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8.2.8.3.2.6 ISS CBUFF Window Management and Address Remapping Details

This section explains the internal address remapping and windows management algorithm. Internally, the module maintains some variables in addition to the configuration registers. The module manages multiple contexts in parallel. Table 8-270 lists the CBUFF internal variables.

Table 8-270. ISS CBUFF Internal Variables

Variable	Description
WAx	Current window index for context x. Possible values are 0 to allowed window count. The current value can be read using the CBUFF_CTX_STATUS_i[11:8] WA bit field.
WBx	Window in the physical space that can be accessed by the CPU in read/write modes. Window that is read from OCPI in read/write mode. Possible values are 0 to allowed window count. The current value can be read using the CBUFF_CTX_STATUS_i[3:0] WB bit field.
VPAx	Start address, in the virtual space, of the CBUFF_CTX_STATUS_i[11:8] WA window
	Used as a base pointer for the read (read mode) or write data flow (write, read/write modes)
	This is an internal quantity that cannot be accessed by software.
VPBx	Start address, in the virtual space, of the CBUFF_CTX_STATUS_i[3:0] WB window
	Used as a base pointer for the read data flow.
	This is an internal quantity that cannot be accessed by software.
OFFSETAx	This is an internal quantity that cannot be accessed by software.
OFFSETBx	Address offset used when WAx or WBx is accessed
LEVELAx	This is an internal quantity that cannot be accessed by software.
LEVELBx	Address offset used when WAx or WBx is accessed

8.2.8.3.2.6.1 ISS CBUFF Startup

The status of a CBUFF context is reset when it is disabled. This does not affect the configuration registers or the CBUFF_IRQSTATUS register. Table 8-271 lists the internal state after reset.

Table 8-271. ISS CBUFF Internal State After Reset

Variable	Description
WAx	0
WBx	0
VPAx VPBx	CBUFF_CTX_START_i
OFFSETAx OFFSETBx	CBUFF_CTX_START_i – CBUFF_CTX_PHY_i
LEVELAx LEVELBx	0

8.2.8.3.2.6.2 ISS CBUFF Access Identification

For each access to the virtual space (OCPI slave port), the CBUFF first checks the address to classify the transaction into one of the categories listed in Table 8-272.

Table 8-272. ISS CBUFF Address identification

Address ID	Variable	Condition
0+2*x	WA_CBUFFx	CBUFF_CTX_CTRL_i[0] ENABLE = 1 and ADDR = VPAx and ADDR VPAx + CBUFF_CTX_WINDOWSIZE_i and ADDR = CBUFF_CTX_END_i and Access type = write when read/write mode is selected
1+2*x	WB_CBUFFx	CBUFF_CTX_CTRL_i[0] ENABLE = 1 and CBUFF_CTX_CTRL_i[2:1] MODE = 2 and

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Table 8-272. ISS CBUFF Address identification (continued)

Address ID	Variable	Condition
		Access type = read and ADDR=VPBx and ADDRVPBx + CBUFF_CTX_WINDOWSIZE_i and ADDR= CBUFF_CTX_END_i
16+x	ERR_CBUFFx	CBUFF_CTX_CTRL_i[0] ENABLE = 1 and ADDR= CBUFF_CTX_START_i and ADDR= CBUFF_CTX_END_i
24	TRANSPARENT	Always true

Lower IDs correspond to higher priorities if multiple conditions are true. For example, when the current virtual window of CBUFF 0 is accessed, at least the tests for categories WA_CBUFFx and ERR_CBUFFx are true. The final category is WA_CBUFFx, because it has a higher priority.

NOTE: Tests must be performed in parallel to match the desired performance.

Further processing depends on the category:

- TRANSPARENT: Accesses flow though the module without changing its internal state or any translation.
- ERR_CBUFFx: The module goes into error state for the concerned context and sets the CBUFF_HL_IRQSTATUS.IRQ_CTXx_INVALID bit. When the module is in error state for CBUFFx, all accesses to that buffer are cancelled. In other words, any access that has an address between CBUFF_CTX_START_i and CBUFF_CTX_END_i is not transmitted to the OCPO master port. There are two ways to leave the error state:
  - Hardware reset
  - Disable and re-enable the context in error state.

    Accesses outside of the virtual space from the context in error state are not affected.
- WA_CBUFFx and WB_CBUFFx: The internal state is updated and address translation is performed when the performed access type (read or write) is compatible with the current mode (read, write, or read/write mode). Otherwise, a CBUFF_HL_IRQSTATUS.IRQ_CTXx_INVALID event is set and CBUFFx goes into the error state.

8.2.8.3.2.6.3 ISS CBUFF Address Translation

An offset is selected depending on the access category (see Section 8.2.8.3.2.6.1, *ISS CBUFF Startup*) and the internal state of the accessed buffer. Table 8-273 lists possible cases.

Table 8-273. ISS CBUFF Address Translation

Condition	Address Translation
CBUFF_CTX_CTRL_i[0] ENABLE = 1 and ADDR = CBUFF_CTX_START_i and ADDR = CBUFF_CTX_END_i and CBUFFx in error state	Access cancelled
Category = WA_CBUFFx	ADDROUT = ADDRIN-OFFSETAx
Category = WB_CBUFFx	Read/write mode only ADDROUT = ADDRIN-OFFSETBx
Category = ERR_CBUFFx	Access cancelled
Category = TRANSPARENT	ADDROUT = ADDRIN

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8.2.8.3.2.6.4 ISS CBUFF Window Fill Level

Each time an access is performed into an active window (WA_CBUFFx when context x is enabled) the window level is updated. The corresponding LEVELy is incremented according to the BYTEEN input of the OCPI slave port. All possible BYTEEN patterns, including nonaligned ones, are supported. Table 8-274 shows some examples. The basic idea is to count the number of 1s in the BYTEEN input for each 128-bit word and to sum the values.

Table 8-274. ISS CBUFF Window-Level Increment

BYTEEN	LEVELy Increment	Comment
0x0000	0	No access
0x0001	1	8-bit access
0x0002	1	8-bit access
0x0003	2	16-bit access
...	...	...
0x0007	3	24-bit access
...	...	...
0x000F	4	32-bit access
...	...	...
0x00F0	4	32-bit access
...	...	...
0xFFFF	16	128-bit access

The window level is compared to CBUFFx_THRESHOLD. Table 8-275 lists the situations that may occur:

Table 8-275. ISS CBUFF Window-Level Comparison(1)

Condition	Description
LEVELAx = CBUFF_CTX_THRESHOLD_F_i	The CBUFF_CTX_STATUS_i[11:8] WA bit field of context x is full (write mode) or empty (read mode). Internal window indexes, levels, and offsets are updated.
LEVELBx = CBUFF_CTX_THRESHOLD_F_i	Read/write mode only Window used to handle the read flow of context x is empty. Internal window indexes, levels, and offsets are updated.

(1) All situations described in Table 8-275 are mutually exclusive because only one level is updated each cycle.

8.2.8.3.2.6.5 ISS CBUFF Window Pointer and Offset Update

The following description refers to the update of WA in write mode:

When the current window of a context is full:

- A new window is opened. The update is done in a circular manner: the first physical window in is reused after the last one.
  - WA (WA + 1) modulo the number defined by CBUFF_CTX_CTRL_i[9:8] WCOUNT
  - LEVELA - 0
  - VPA - VPA + CBUFF_CTX_WINDOWSIZE_i
- When the window is moved from the last buffer to the first:
  - OFFSETA - OFFSETA + CBUFF_CTX_WINDOWSIZE_i (CBUFF_CTX_CTRL_i[9:8] WCOUNT + 1)
- Otherwise, OFFSETA does not change.

The algorithm used to update WA in read mode is the same, except that *full* refers to *all data of the window has been read* or *window empty*.

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For read/write mode, the same algorithm is used to translate reads to the WBx window. Make the following changes:

- Replace WA with WB.
- Replace LEVELA with LEVELB.
- Replace VPA with VPB.
- Replace OFFSETA with OFFSETB.

8.2.8.3.2.7 ISS CBUFF Error State

Contexts may go into error state when they receive unexpected accesses. In that case, the CBUFF does not send dummy transactions to the OCPO port. It does not forward the failing transactions to OCPO and returns valid responses (SResp = DVA) on OCPI to preserve the integrity of the OCP.

Responses may be received on OCPO while the CBUFF responds to failing transactions on OCPI. The OCPO response phase is stalled (MRespAccept = 0) during that time to prevent corruption. OCPO cannot be stalled longer than one full OCP transaction. Responses received on OCPO are handled before another internally generated response can be sent back to the OCPI. In that case, command and data phases are eventually stalled. Not stalling OCPO for too long is required to avoid affecting system performance.

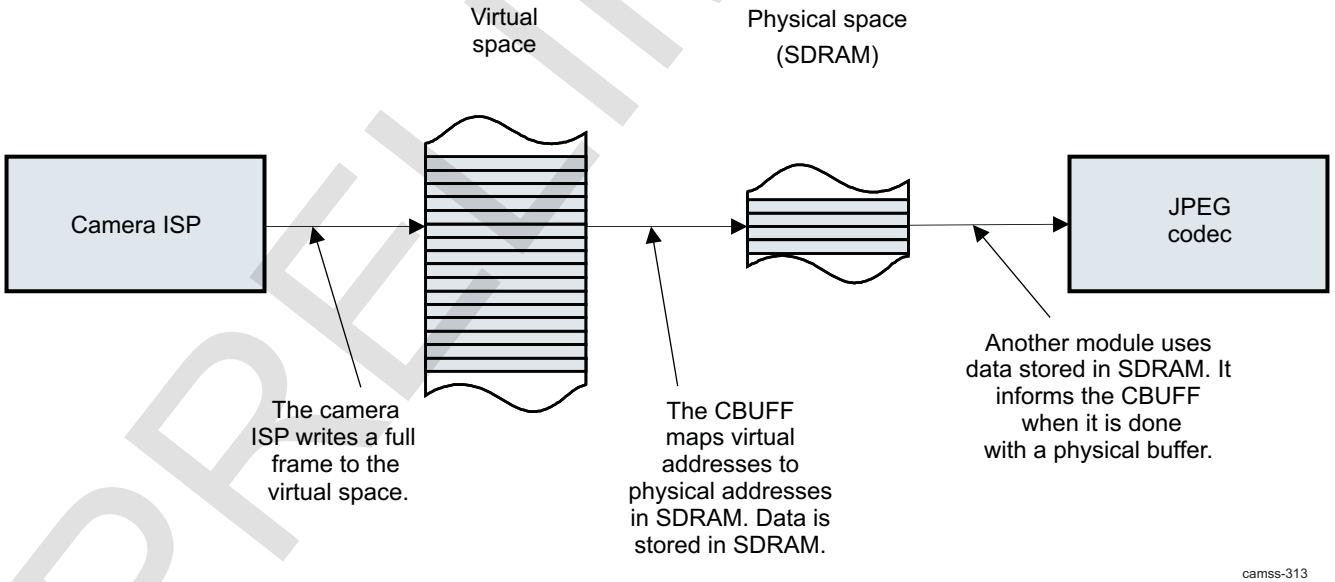
During normal operation (that is, no context is in error state), the OCPO response phase is never stalled.

8.2.8.3.2.8 ISS CBUFF Typical Configurations

8.2.8.3.2.8.1 ISS CBUFF Single-Slice Buffer

An OCP master (typically, the ISS) writes data with an incremental addressing scheme to the virtual space. The physical space is smaller than the virtual space. Therefore, physical space locations are read and written multiple times. Figure 8-102 shows the CBUFF single-slice buffer in write mode.

Figure 8-102. ISS CBUFF Single-Slice Buffer (Write Mode)



Physically, this CBUFF is in on-chip SRAM or SDRAM. The virtual space is defined by a start and end addresses. The physical space is defined by a start address, a window size, and a window count. It is contiguous in memory. When the CPU accesses physical memory for processing, it must know if the SDRAM is available for it to access and if the CBUFF is not using it. The CPU and CBUFF cannot track each other. For example, an interrupt must be triggered from the SIMCOP to the CBUFF to notify it when the processor is done working with SDRAM. For more information about the software configuration for these interrupts, see Section 8.2.8.3.2.2.1, *ISS CBUFF Write Mode*.

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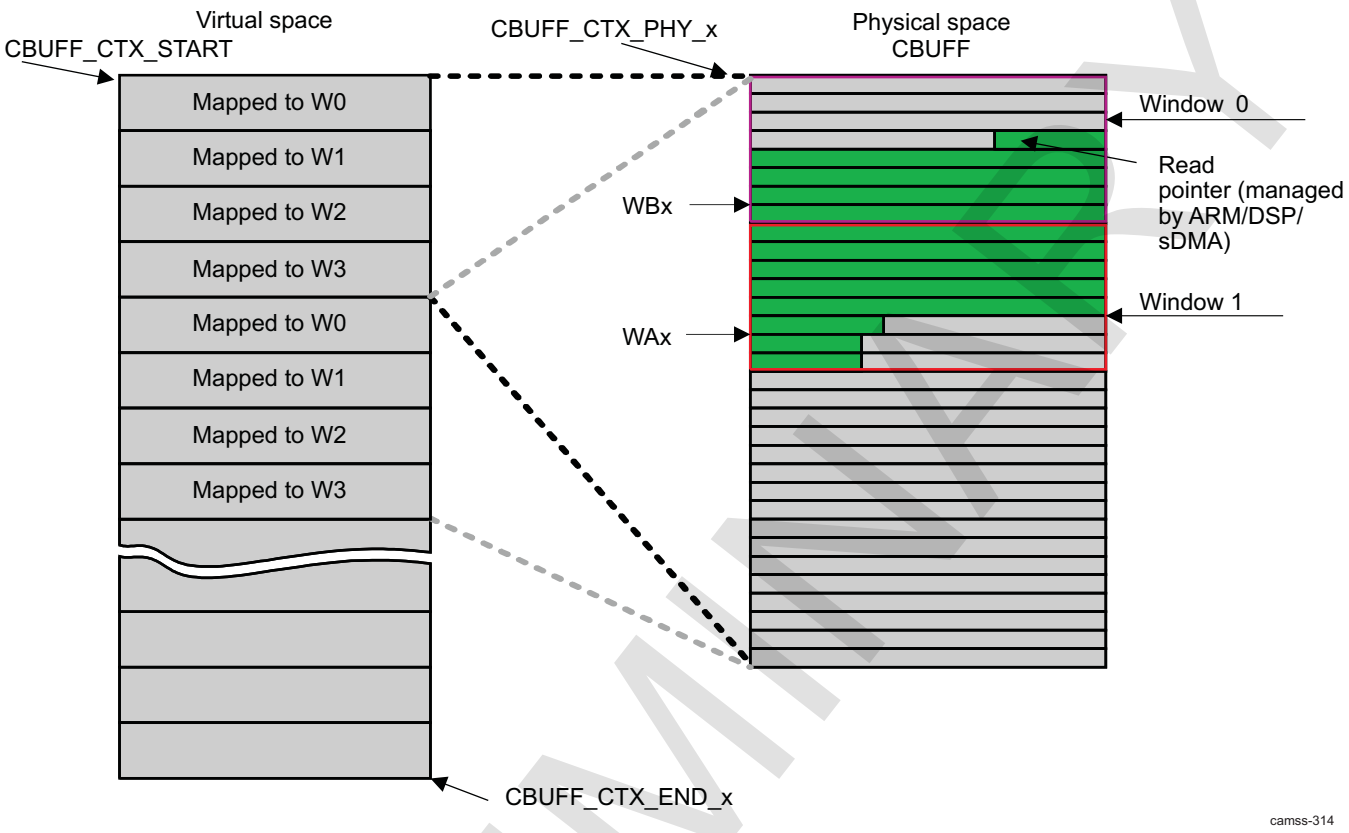
Figure 8-103 shows the buffer organization for a 4-window buffer.

Figure 8-103. ISS CBUFF Single-Slice Buffer Example (Write Mode)

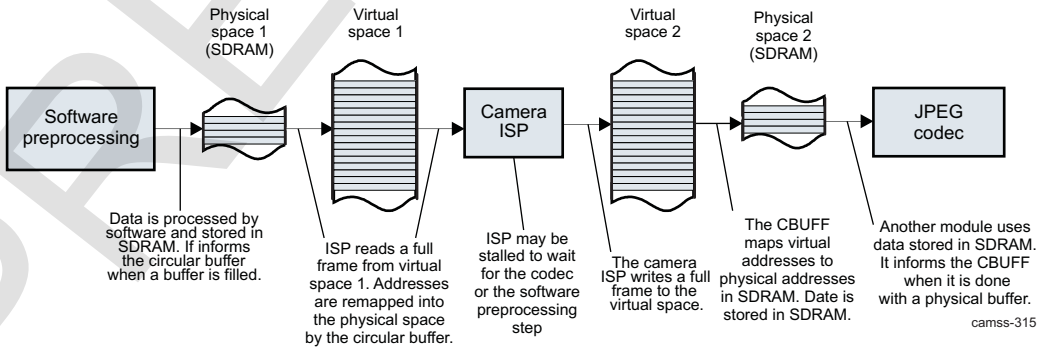


The CBUFF can manage multiple contexts in single-slice mode.

8.2.8.3.2.8.2 ISS CBUFF Extended-Slice Buffer

In extended-slice mode, at least two contexts managed by the CBUFF are used together. The two contexts provide address translation, one for the read data flow and the other for a write data flow. Figure 8-104 is an example of the CBUFF extended-slice buffer.

Figure 8-104. ISS CBUFF Extended-Slice Buffer Example



8.2.8.3.2.9 ISS CBUFF FIFO Mode

The CBUFF can behave like a FIFO to buffer data between two initiators connected to the OCPI. A typical use case is a camera interface writing data to the FIFO and an ISP reading data from the FIFO. Figure 8-105 shows the CBUFF FIFO mode.

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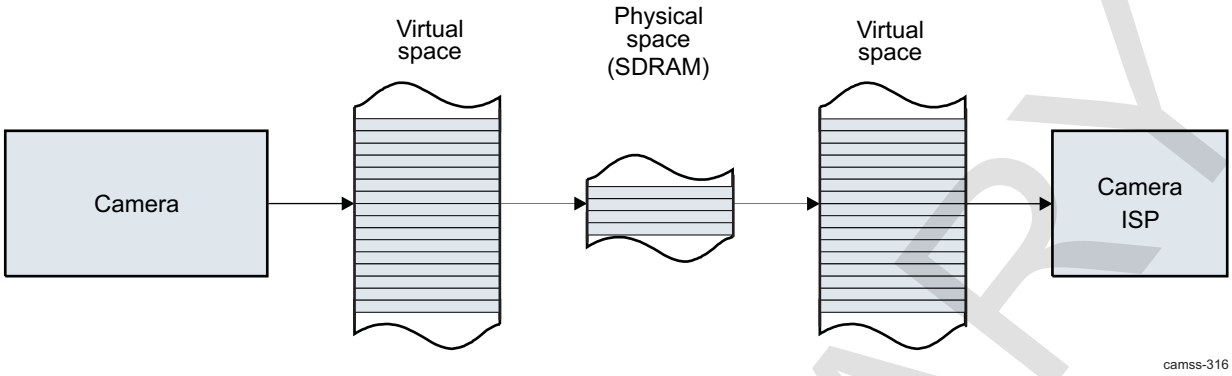
Figure 8-105. ISS CBUFF FIFO Mode

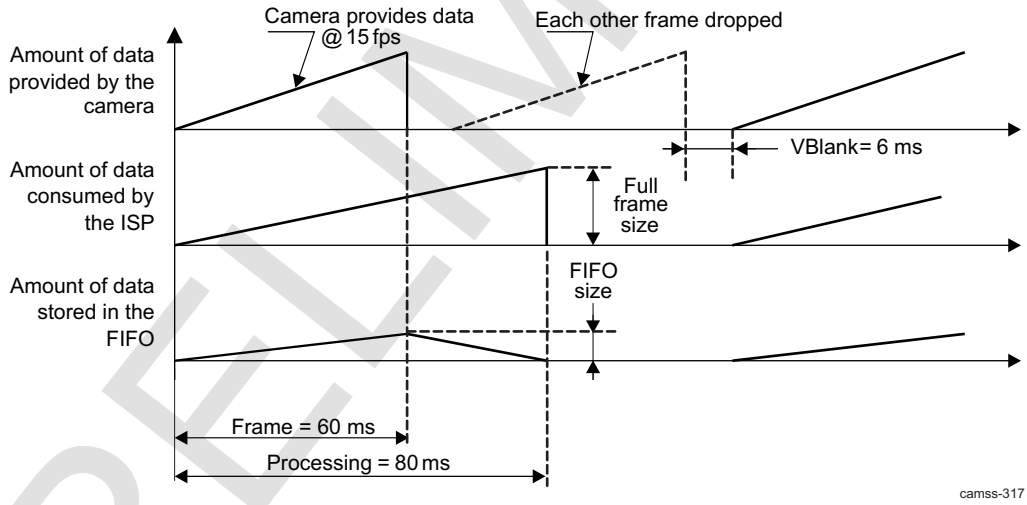


The CBUFF is used as a FIFO when the camera provides data at a higher rate than the ISP can process. To avoid storing one or multiple full-frame buffers, a FIFO buffer is used to store the data that cannot be processed immediately.

For this example, assume that the camera provides 16 MPix at 15 frames per second. A new frame is provided every 66 ms. The ISP needs 80 ms to process this frame. Therefore, the processing cannot be done on the fly, and each other frame must be dropped.

Figure 8-106 shows the accumulated amount of data provided by the camera since the start of the frame; the amount of data consumed by the ISP since it has started processing the frame; and the difference between the two, which must be stored in the FIFO.

Figure 8-106. ISS CBUFF FIFO Use Example



The FIFO is emulated as 16 windows (CBUFF_CTX_CTRL_i[9:8] WCOUNT = 0x3). The ISP is started by software when a few kilobytes of data are written to the physical space. Alternatively, the BCF mechanism can be used, but the minimum FIFO size is more complex to calculate.

The FIFO level reaches its maximum when the camera performs the last write of the frame. The camera provides the data at 1 byte/pixel 16 MPix/60 ms = 266 Mbps. The ISP reads data at 1 byte/pixel × 16 MPix/80 ms = 200 Mbps. Therefore, the minimum FIFO size is 60 ms × (266 Mbps – 200 Mbps) = 3.96 Mbps, which is four times less than a full-frame buffer.

Each window holds 256KB of data. The camera starts writing to a new physical window every 256KB/266 Mbps = 962 µs. The ISP starts reading from a new physical window every 1280 µs.

The FIFO mode can also be used when the ISP is slower than the camera. In that case, the ISP is stalled when insufficient data is available in the physical space.

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8.2.8.4 ISS CBUFF Programming Model

8.2.8.4.1 ISS CBUFF Reset Behavior

Upon hardware or software reset of the CBUFF, all registers in the CBUFF are reset to their reset values

This software reset has the same effect as a hardware reset. ISS high-level software reset ensures that traffic is stopped on clear boundary because the CBUFF is sending data to and from other modules. ISS top-level reset is preferred. For more information about ISS software reset, see Section 8.1.2.3, *ISS Reset*. Submodule reset is not preferred but is available through the following registers:

1. Set the CBUFF_HL_SYSCONFIG[0] SOFTRESET bit to 1.
2. Read the CBUFF_HL_SYSCONFIG[0] SOFTRESET bit to check whether it is set to 1, which means the reset occurred.

The reset is performed without waiting until all OCP traffic stops. To avoid OCP corruption, software must ensure there is no more ongoing traffic before performing a reset.

8.2.8.4.2 ISS CBUFF Register Setup

All registers of the context to be used must be initialized for correct operation. Table 8-276 lists the procedure for the CBUFF register setup.

Table 8-276. ISS CBUFF Setup Register

Step	Bit Field	Value
Set operation mode.	CBUFF_CTX_CTRL_i[2:1] MODE	0x0: Write mode 0x1: Read mode 0x2: Read/write mode 0x3: Reserved
Define the virtual address range managed by the CBUFF. It usually corresponds to the address region where one image frame is written by the OCPI initiator.	CBUFF_CTX_START_i and CBUFF_CTX_END_i	
Define the start address of the physical buffer.	CBUFF_CTX_PHY_i	
Set the window count and size. The window size usually depends on the use of the buffer. Eight or 16 video lines correspond to a current size for JPEG video compression. A higher window count provides better latency-related overflow protection.	CBUFF_CTX_CTRL_i[9:8] WCOUNT and CBUFF_CTX_WINDOWSIZE_i	
When the 2D addressing capability is not used, set to the window size in CBUFF_CTX_THRESHOLD_F_i. Otherwise, it is set to a smaller value depending on the buffer organization. For example, when each window corresponds to lines by 4096 pixels, but the ISP sends lines of only 2560 pixels, CBUFF_CTX_WINDOWSIZE_i = 8 4096 and CBUFF_CTX_THRESHOLD_F_i = 8 2560.	CBUFF_CTX_THRESHOLD_F_i	
BCF signal-generation configuration is optional.	CBUFF_CTX_THRESHOLD_S_i and CBUFF_CTX_CTRL_i[7:4] BCF	
Enable the module. It can be disabled by clearing the ENABLE bit. This must be done only when there are no more outstanding requests to the virtual space managed by CBUFFx. All internal FSMs and counters of the CBUFF are reset when it is disabled. Pending interrupts are not affected.	CBUFF_CTX_CTRL_i[0] ENABLE	

8.2.8.5 ISS CBUFF Register Manual

8.2.8.5.1 ISS CBUFF Instance Summary

Table 8-277 lists the CBUFF instance.

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Table 8-277. ISS CBUFF Instance Summary

Module Name	L3 Base Address	Size
ISS_CBUFF	0x5200 1800	512 bytes

8.2.8.5.2 ISS CBUFF Registers

8.2.8.5.2.1 ISS CBUFF Register Summary

Table 8-278 summarizes the CBUFF registers.

Table 8-278. ISS CBUFF Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	ISS_CBUFF Base Address
CBUFF_HL_REVISION	R	32	0x0000 0000	0x5200 1800
CBUFF_HL_HWINFO	R	32	0x0000 0004	0x5200 1804
CBUFF_HL_SYSCONFIG	RW	32	0x0000 0010	0x5200 1810
RESERVED	RW	32	0x0000 001C	0x5200 181C
CBUFF_HL_IRQSTATUS_RAW	RW	32	0x0000 0020	0x5200 1820
CBUFF_HL_IRQSTATUS	RW	32	0x0000 0024	0x5200 1824
CBUFF_HL_IRQENABLE_SET	RW	32	0x0000 0028	0x5200 1828
CBUFF_HL_IRQENABLE_CLR	RW	32	0x0000 002C	0x5200 182C
CBUFF_FRAG_ADDR_j (1)	RW	32	0x0000 0080 + (0x4 * j)	0x5200 1880 + (0x4 * j)
CBUFF_CTX_CTRL_i (2)	RW	32	0x0000 0100 + (0x20 * i)	0x5200 1900 + (0x20 * i)
CBUFF_CTX_START_i (2)	RW	32	0x0000 0104 + (0x20 * i)	0x5200 1904 + (0x20 * i)
CBUFF_CTX_END_i (2)	RW	32	0x0000 0108 + (0x20 * i)	0x5200 1908 + (0x20 * i)
CBUFF_CTX_WINDOWSIZE_i (2)	RW	32	0x0000 010C + (0x20 * i)	0x5200 190C + (0x20 * i)
CBUFF_CTX_THRESHOLD_F_i (2)	RW	32	0x0000 0110 + (0x20 * i)	0x5200 1910 + (0x20 * i)
CBUFF_CTX_THRESHOLD_S_i (2)	RW	32	0x0000 0114 + (0x20 * i)	0x5200 1914 + (0x20 * i)
CBUFF_CTX_STATUS_i (2)	R	32	0x0000 0118 + (0x20 * i)	0x5200 1918 + (0x20 * i)
CBUFF_CTX_PHY_i (2)	RW	32	0x0000 011C + (0x20 * i)	0x5200 191C + (0x20 * i)

(1) j = 0 to 15
(2) i = 0 to 7

8.2.8.5.2.2 ISS CBUFF Register Description

Table 8-279 through Table 8-310 describe the CBUFF registers.

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Table 8-279. CBUFF_HL_REVISION

Address Offset	0x0000 0000		
Physical Address	0x5200 1800	**Instance**	ISS_CBUFF
Description	IP revision identifier (X.Y.R) Used by software to track features, bugs, and compatibility		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP Revision	R	See(1)

(1) TI internal data

Table 8-280. Register Call Summary for Register CBUFF_HL_REVISION

ISS Interfaces
- ISS CBUFF Registers: [0]

Table 8-281. CBUFF_HL_HWINFO

Address Offset	0x0000 0004		
Physical Address	0x5200 1804	**Instance**	ISS_CBUFF
Description	Information about the IP module's hardware configuration.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													CONTEXTS		ENABLE_FRAGMENTATION

Bits	Field Name	Description	Type	Reset
31:3	RESERVED		R	0x0000 0000
2:1	CONTEXTS	Number of contexts	R	0x1
		Read 0x3: Reserved		
		Read 0x2: 8 contexts		
		Read 0x1: 4 contexts		
		Read 0x0: 2 contexts		
0	ENABLE_FRAGMENTATION	Provides information to software if fragmentation support is available	R	0
		Read 0x1: Yes		
		Read 0x0: No		

Table 8-282. Register Call Summary for Register CBUFF_HL_HWINFO

ISS Interfaces
- ISS CBUFF Registers: [0]

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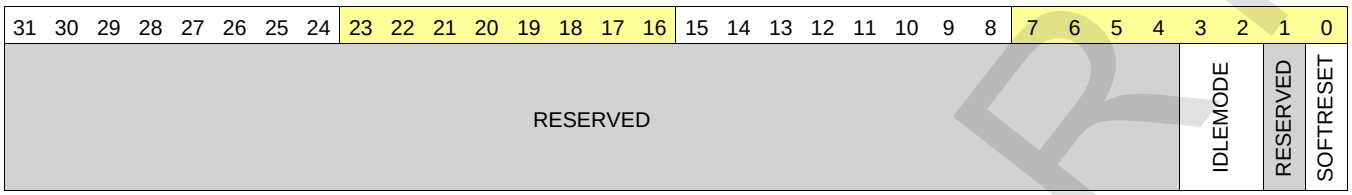
Table 8-283. CBUFF_HL_SYSCONFIG

Address Offset	0x0000 0010		
Physical Address	0x5200 1810	**Instance**	ISS_CBUFF
Description	Clock management configuration		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0000000
3:2	IDLEMODE	Configuration of the local target state management mode. By definition, target can handle read/write transaction as long as it is out of IDLE state. 0x0: Force-idle mode: local target's idle state follows (acknowledges) the system's idle requests unconditionally, that is, regardless of the IP module's internal requirements. Backup mode, for debug only. 0x1: No-idle mode: local target never enters IDLE state. Backup mode, for debug only. 0x3: Reserved 0x2: Smart-idle mode: local target's IDLE state eventually follows (acknowledges) the system's IDLE requests, depending on the IP module's internal requirements. IP module shall not generate (IRQ- or DMA-request-related) wake-up events.	RW	0x2
1	RESERVED		R	0
0	SOFTRESET	Software reset Write 0x0: No action Write 0x1: Initiate software reset Read 0x1: Reset (software or other) ongoing Read 0x0: Reset done, no pending action	RW	0

Table 8-284. Register Call Summary for Register CBUFF_HL_SYSCONFIG

ISS Interfaces

- ISS CBUFF PRCM Interface: [0] [1]
- ISS CBUFF Reset Behavior: [2] [3]
- ISS CBUFF Registers: [4]

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Table 8-285. CBUFF_HL_IRQSTATUS_RAW

Address Offset	0x0000 0020		
Physical Address	0x5200 1820	**Instance**	ISS_CBUFF
Description	Per-event raw interrupt status vector. Raw status is set even if event is not enabled. Write 1 to set the (raw) status, mostly for debug.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IRQ_CTX7_OVR	IRQ_CTX6_OVR	IRQ_CTX5_OVR	IRQ_CTX4_OVR	IRQ_CTX3_OVR	IRQ_CTX2_OVR	IRQ_CTX1_OVR	IRQ_CTX0_OVR	IRQ_CTX7_INVALID	IRQ_CTX6_INVALID	IRQ_CTX5_INVALID	IRQ_CTX4_INVALID	IRQ_CTX3_INVALID	IRQ_CTX2_INVALID	IRQ_CTX1_INVALID	IRQ_CTX0_INVALID	IRQ_CTX7_READY	IRQ_CTX6_READY	IRQ_CTX5_READY	IRQ_CTX4_READY	IRQ_CTX3_READY	IRQ_CTX2_READY	IRQ_CTX1_READY	IRQ_CTX0_READY	RESERVED							IRQ_OCP_ERR

Bits	Field Name	Description	Type	Reset
31	IRQ_CTX7_OVR	Buffer overflow event. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
30	IRQ_CTX6_OVR	Buffer overflow event. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
29	IRQ_CTX5_OVR	Buffer overflow event. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
28	IRQ_CTX4_OVR	Buffer overflow event. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
27	IRQ_CTX3_OVR	Buffer overflow event. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
26	IRQ_CTX2_OVR	Buffer overflow event. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0

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Bits	Field Name	Description	Type	Reset
25	IRQ_CTX1_OVR	Buffer overflow event. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
24	IRQ_CTX0_OVR	Buffer overflow event. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
23	IRQ_CTX7_INVALID	Invalid access. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
22	IRQ_CTX6_INVALID	Invalid access. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
21	IRQ_CTX5_INVALID	Invalid access. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
20	IRQ_CTX4_INVALID	Invalid access. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
19	IRQ_CTX3_INVALID	Invalid access. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
18	IRQ_CTX2_INVALID	Invalid access. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
17	IRQ_CTX1_INVALID	Invalid access. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0

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Bits	Field Name	Description	Type	Reset
16	IRQ_CTX0_INVALID	Invalid access. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
15	IRQ_CTX7_READY	The WB physical window is ready to be accessed by the CPU. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
14	IRQ_CTX6_READY	The WB physical window is ready to be accessed by the CPU. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
13	IRQ_CTX5_READY	The WB physical window is ready to be accessed by the CPU. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
12	IRQ_CTX4_READY	The WB physical window is ready to be accessed by the CPU. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
11	IRQ_CTX3_READY	The WB physical window is ready to be accessed by the CPU. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
10	IRQ_CTX2_READY	The WB physical window is ready to be accessed by the CPU. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
9	IRQ_CTX1_READY	The WB physical window is ready to be accessed by the CPU. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0

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Bits	Field Name	Description	Type	Reset
8	IRQ_CTX0_READY	The WB physical window is ready to be accessed by the CPU. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
7:1	RESERVED		R	0x00
0	IRQ_OCP_ERR	OCP error received in the master port. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0

Table 8-286. Register Call Summary for Register CBUFF_HL_IRQSTATUS_RAW

ISS Interfaces
- ISS CBUFF Interrupts: [0] [1]
- ISS CBUFF Registers: [2]

Table 8-287. CBUFF_HL_IRQSTATUS

Address Offset	0x0000 0024		
Physical Address	0x5200 1824	**Instance**	ISS_CBUFF
Description	Per-event "enabled" interrupt status vector. Enabled status is not set unless event is enabled. Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, that is, even if not enabled).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IRQ_CTX7_OVR	IRQ_CTX6_OVR	IRQ_CTX5_OVR	IRQ_CTX4_OVR	IRQ_CTX3_OVR	IRQ_CTX2_OVR	IRQ_CTX1_OVR	IRQ_CTX0_OVR	IRQ_CTX7_INVALID	IRQ_CTX6_INVALID	IRQ_CTX5_INVALID	IRQ_CTX4_INVALID	IRQ_CTX3_INVALID	IRQ_CTX2_INVALID	IRQ_CTX1_INVALID	IRQ_CTX0_INVALID	IRQ_CTX7_READY	IRQ_CTX6_READY	IRQ_CTX5_READY	IRQ_CTX4_READY	IRQ_CTX3_READY	IRQ_CTX2_READY	IRQ_CTX1_READY	IRQ_CTX0_READY	RESERVED							IRQ_OCP_ERR

Bits	Field Name	Description	Type	Reset
31	IRQ_CTX7_OVR	Buffer overflow event. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
30	IRQ_CTX6_OVR	Buffer overflow event. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
29	IRQ_CTX5_OVR	Buffer overflow event. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
28	IRQ_CTX4_OVR	Buffer overflow event. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
27	IRQ_CTX3_OVR	Buffer overflow event. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
26	IRQ_CTX2_OVR	Buffer overflow event. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
25	IRQ_CTX1_OVR	Buffer overflow event. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
24	IRQ_CTX0_OVR	Buffer overflow event. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
23	IRQ_CTX7_INVALID	Invalid access. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
22	IRQ_CTX6_INVALID	Invalid access. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
21	IRQ_CTX5_INVALID	Invalid access. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
20	IRQ_CTX4_INVALID	Invalid access. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
19	IRQ_CTX3_INVALID	Invalid access. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
18	IRQ_CTX2_INVALID	Invalid access. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
17	IRQ_CTX1_INVALID	Invalid access. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
16	IRQ_CTX0_INVALID	Invalid access. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
15	IRQ_CTX7_READY	The WB physical window is ready to be accessed by the CPU. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
14	IRQ_CTX6_READY	The WB physical window is ready to be accessed by the CPU. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
13	IRQ_CTX5_READY	The WB physical window is ready to be accessed by the CPU. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
12	IRQ_CTX4_READY	The WB physical window is ready to be accessed by the CPU. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
11	IRQ_CTX3_READY	The WB physical window is ready to be accessed by the CPU. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
10	IRQ_CTX2_READY	The WB physical window is ready to be accessed by the CPU. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
9	IRQ_CTX1_READY	The WB physical window is ready to be accessed by the CPU. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
8	IRQ_CTX0_READY	The WB physical window is ready to be accessed by the CPU. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
7:1	RESERVED		R	0x00
0	IRQ_OCP_ERR	OCP error received in the master port. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0

Table 8-288. Register Call Summary for Register CBUFF_HL_IRQSTATUS

ISS Interfaces

- ISS CBUFF Interrupts: [0] [1] [2] [3]
- ISS CBUFF Functional Description: [4] [5]
- ISS CBUFF Registers: [6]

Table 8-289. CBUFF_HL_IRQENABLE_SET

Address Offset	0x0000 0028		
Physical Address	0x5200 1828	**Instance**	ISS_CBUFF
Description	Per-event interrupt enable bit vector. Write 1 to set (enable interrupt). Readout equal to corresponding _CLR register.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IRQ_CTX7_OVR	IRQ_CTX6_OVR	IRQ_CTX5_OVR	IRQ_CTX4_OVR	IRQ_CTX3_OVR	IRQ_CTX2_OVR	IRQ_CTX1_OVR	IRQ_CTX0_OVR	IRQ_CTX7_INVALID	IRQ_CTX6_INVALID	IRQ_CTX5_INVALID	IRQ_CTX4_INVALID	IRQ_CTX3_INVALID	IRQ_CTX2_INVALID	IRQ_CTX1_INVALID	IRQ_CTX0_INVALID	IRQ_CTX7_READY	IRQ_CTX6_READY	IRQ_CTX5_READY	IRQ_CTX4_READY	IRQ_CTX3_READY	IRQ_CTX2_READY	IRQ_CTX1_READY	IRQ_CTX0_READY	RESERVED							IRQ_OCP_ERR

Bits	Field Name	Description	Type	Reset
31	IRQ_CTX7_OVR	Buffer overflow event. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
30	IRQ_CTX6_OVR	Buffer overflow event. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
29	IRQ_CTX5_OVR	Buffer overflow event. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
28	IRQ_CTX4_OVR	Buffer overflow event. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
27	IRQ_CTX3_OVR	Buffer overflow event. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
26	IRQ_CTX2_OVR	Buffer overflow event. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
25	IRQ_CTX1_OVR	Buffer overflow event. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
24	IRQ_CTX0_OVR	Buffer overflow event. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0

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Bits	Field Name	Description	Type	Reset
23	IRQ_CTX7_INVALID	Invalid access. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
22	IRQ_CTX6_INVALID	Invalid access. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
21	IRQ_CTX5_INVALID	Invalid access. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
20	IRQ_CTX4_INVALID	Invalid access. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
19	IRQ_CTX3_INVALID	Invalid access. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
18	IRQ_CTX2_INVALID	Invalid access. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
17	IRQ_CTX1_INVALID	Invalid access. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
16	IRQ_CTX0_INVALID	Invalid access. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
15	IRQ_CTX7_READY	The WB physical window is ready to be accessed by the CPU. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0

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Bits	Field Name	Description	Type	Reset
14	IRQ_CTX6_READY	The WB physical window is ready to be accessed by the CPU. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
13	IRQ_CTX5_READY	The WB physical window is ready to be accessed by the CPU. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
12	IRQ_CTX4_READY	The WB physical window is ready to be accessed by the CPU. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
11	IRQ_CTX3_READY	The WB physical window is ready to be accessed by the CPU. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
10	IRQ_CTX2_READY	The WB physical window is ready to be accessed by the CPU. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
9	IRQ_CTX1_READY	The WB physical window is ready to be accessed by the CPU. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
8	IRQ_CTX0_READY	The WB physical window is ready to be accessed by the CPU. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
7:1	RESERVED		R	0x00
0	IRQ_OCP_ERR	OCP error received in the master port. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0

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Table 8-290. Register Call Summary for Register CBUFF_HL_IRQENABLE_SET

ISS Interfaces

- ISS CBUFF Interrupts: [0]
- ISS CBUFF Registers: [1]

Table 8-291. CBUFF_HL_IRQENABLE_CLR

Address Offset	0x0000 002C		
Physical Address	0x5200 182C	**Instance**	ISS_CBUFF
Description	Per-event interrupt enable bit vector, line 0. Write 1 to clear (disable interrupt). Readout equal to corresponding _SET register.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IRQ_CTX7_OVR	IRQ_CTX6_OVR	IRQ_CTX5_OVR	IRQ_CTX4_OVR	IRQ_CTX3_OVR	IRQ_CTX2_OVR	IRQ_CTX1_OVR	IRQ_CTX0_OVR	IRQ_CTX7_INVALID	IRQ_CTX6_INVALID	IRQ_CTX5_INVALID	IRQ_CTX4_INVALID	IRQ_CTX3_INVALID	IRQ_CTX2_INVALID	IRQ_CTX1_INVALID	IRQ_CTX0_INVALID	IRQ_CTX7_READY	IRQ_CTX6_READY	IRQ_CTX5_READY	IRQ_CTX4_READY	IRQ_CTX3_READY	IRQ_CTX2_READY	IRQ_CTX1_READY	IRQ_CTX0_READY	RESERVED							IRQ_OCP_ERR

Bits	Field Name	Description	Type	Reset
31	IRQ_CTX7_OVR	Buffer overflow event. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
30	IRQ_CTX6_OVR	Buffer overflow event. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
29	IRQ_CTX5_OVR	Buffer overflow event. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
28	IRQ_CTX4_OVR	Buffer overflow event. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
27	IRQ_CTX3_OVR	Buffer overflow event. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
26	IRQ_CTX2_OVR	Buffer overflow event. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
25	IRQ_CTX1_OVR	Buffer overflow event. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
24	IRQ_CTX0_OVR	Buffer overflow event. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
23	IRQ_CTX7_INVALID	Invalid access. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
22	IRQ_CTX6_INVALID	Invalid access. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
21	IRQ_CTX5_INVALID	Invalid access. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
20	IRQ_CTX4_INVALID	Invalid access. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
19	IRQ_CTX3_INVALID	Invalid access. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
18	IRQ_CTX2_INVALID	Invalid access. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
17	IRQ_CTX1_INVALID	Invalid access. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
16	IRQ_CTX0_INVALID	Invalid access. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
15	IRQ_CTX7_READY	The WB physical window is ready to be accessed by the CPU. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
14	IRQ_CTX6_READY	The WB physical window is ready to be accessed by the CPU. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
13	IRQ_CTX5_READY	The WB physical window is ready to be accessed by the CPU. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
12	IRQ_CTX4_READY	The WB physical window is ready to be accessed by the CPU. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
11	IRQ_CTX3_READY	The WB physical window is ready to be accessed by the CPU. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
10	IRQ_CTX2_READY	The WB physical window is ready to be accessed by the CPU. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
9	IRQ_CTX1_READY	The WB physical window is ready to be accessed by the CPU. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
8	IRQ_CTX0_READY	The WB physical window is ready to be accessed by the CPU. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
7:1	RESERVED		R	0x00
0	IRQ_OCP_ERR	OCP error received in the master port. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0

Table 8-292. Register Call Summary for Register CBUFF_HL_IRQENABLE_CLR

ISS Interfaces
- ISS CBUFF Interrupts: [0]
- ISS CBUFF Registers: [1]

Table 8-293. CBUFF_FRAG_ADDR_j

Address Offset	0x0000 0080 + (0x4 * j) See Table 8-278.	**Index** **Instance**	j = 0 to 15 ISS_CBUFF
Description	Start address of the physical buffer of the CBUFF context 0. This register only exists when fragmentation support is enabled.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR																												RESERVED			

Bits	Field Name	Description	Type	Reset
31:4	ADDR	Address, in 128-bit words	RW	0x0000000
3:0	RESERVED		R	0x0

Table 8-294. Register Call Summary for Register CBUFF_FRAG_ADDR_j

ISS Interfaces
- ISS CBUFF Registers: [0]

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Table 8-295. CBUFF_CTX_CTRL_i

Address Offset	0x0000 0100 + (0x20 * i)	**Index**	i = 0 to 7
Physical Address	0x5200 1900 + (0x20 * i)	**Instance**	ISS_CBUFF
Description	Context control register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				TILERMODE	DONE	WCOUNT		BCF				RESERVED	MODE		ENABLE

Bits	Field Name	Description	Type	Reset
31:12	RESERVED		R	0x00000
11	TILERMODE	Sets the expected value for ADDR[32]. If ADDR[32]=TILERMODE, ADDR[31:4] is processed and eventually translated. Otherwise, the access is handled as transparent, regardless of the other address bits.	RW	0
10	DONE	Write this bit to 1 to indicate the CPU has finished processing its physical buffer. This bit is automatically cleared by hardware, reads always return 0. This bit has no effect when MODE=2 (read/write) Write 0x0: No effect. Write 0x1: The CPU has completely processed the WB physical buffer.	W	0
9:8	WCOUNT	Window count 0x0: 2 windows 0x1: 4 windows 0x3: 16 windows 0x2: 8 windows	RW	0x0
7:4	BCF	This register controls the bandwidth control feedback loop output. 0: Control loop disabled. 1-15: The control feedback loop enabled. Behavior depends on functional mode, see Section 8.2.8.3.2.4, *ISS CBUFF Memory-to-Memory Operation BCF*.	RW	0x0
3	RESERVED		R	0
2:1	MODE	Selects the functional mode of this context 0x0: Write mode. ISS writes and CPU reads the physical space. CPU accesses are out of the scope of the CBUFF module; therefore, only writes are permitted between CBUFF_CTX_START__x and CBUFF_CTX_END__x. 0x1: Read mode. Hardware reads and CPU writes the physical space. CPU accesses are out of the scope of the CBUFF module; therefore, only reads are permitted between CBUFF_CTX_START__x and CBUFF_CTX_END__x. 0x2: Read/Write mode. Read and writes are monitored by the CBUFF. WB is used to track current read positions WA is used to track current write position.	RW	0x0

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Bits	Field Name	Description	Type	Reset
0	ENABLE	Enable/disable 0x0: Disables the context. This resets the internal state of the context. All accesses received on OCPI are transmitted to OCPO without modification. Disabling the context takes effect immediately. Software must ensure that no more accesses to the context are outstanding before disabling it. Otherwise memory corruption may occur. 0x1: Enable the context. All accesses between CBUFF_CTX_START__x and CBUFF_CTX_END__x are processed by the CBUFF.	RW	0

Table 8-296. Register Call Summary for Register CBUFF_CTX_CTRL_i

ISS Interfaces

- ISS CBUFF Functional Description: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23] [24] [25] [26] [27] [28] [29] [30] [31]
- ISS CBUFF Register Setup: [32] [33] [34] [35]
- ISS CBUFF Registers: [36]

Table 8-297. CBUFF_CTX_START_i

Address Offset	0x0000 0104 + (0x20 * i)	**Index**	i = 0 to 7
Physical Address	0x5200 1904 + (0x20 * i)	**Instance**	ISS_CBUFF
Description	Start address of the virtual space managed by the context		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR																												RESERVED			

Bits	Field Name	Description	Type	Reset
31:4	ADDR	Address, in 128-bit words	RW	0x0000000
3:0	RESERVED		R	0x0

Table 8-298. Register Call Summary for Register CBUFF_CTX_START_i

ISS Interfaces

- ISS CBUFF Functional Description: [0] [1] [2] [3] [4]
- ISS CBUFF Register Setup: [5]
- ISS CBUFF Registers: [6]

Table 8-299. CBUFF_CTX_END_i

Address Offset	0x0000 0108 + (0x20 * i)	**Index**	i = 0 to 7
Physical Address	0x5200 1908 + (0x20 * i)	**Instance**	ISS_CBUFF
Description	End address of the virtual space managed by the context		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR																												RESERVED			

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Bits	Field Name	Description	Type	Reset
31:4	ADDR	Address, in 128-bit words	RW	0x0000000
3:0	RESERVED		R	0x0

Table 8-300. Register Call Summary for Register CBUFF_CTX_END_i

ISS Interfaces
- ISS CBUFF Functional Description: [0] [1] [2] [3] [4]
- ISS CBUFF Register Setup: [5]
- ISS CBUFF Registers: [6]

Table 8-301. CBUFF_CTX_WINDOWSIZE_i

Address Offset	0x0000 010C + (0x20 * i)	**Index**	i = 0 to 7
Physical Address	0x5200 190C + (0x20 * i)	**Instance**	ISS_CBUFF
Description	Defines the size of a window		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								SIZE																				RESERVED			

Bits	Field Name	Description	Type	Reset
31:24	RESERVED		R	0x00
23:4	SIZE	Size, in 128-bit words	RW	0x00000
3:0	RESERVED		R	0x0

Table 8-302. Register Call Summary for Register CBUFF_CTX_WINDOWSIZE_i

ISS Interfaces
- ISS CBUFF Functional Description: [0] [1] [2] [3] [4]
- ISS CBUFF Register Setup: [5] [6]
- ISS CBUFF Registers: [7]

Table 8-303. CBUFF_CTX_THRESHOLD_F_i

Address Offset	0x0000 0110 + (0x20 * i)	**Index**	i = 0 to 7
Physical Address	0x5200 1910 + (0x20 * i)	**Instance**	ISS_CBUFF
Description	Threshold value used to check if a write window is full		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								THRESHOLD																							

Bits	Field Name	Description	Type	Reset
31:24	RESERVED		R	0x00
23:0	THRESHOLD	Threshold value, in bytes	RW	0x000000

Table 8-304. Register Call Summary for Register CBUFF_CTX_THRESHOLD_F_i

ISS Interfaces
- ISS CBUFF Functional Description: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10]
- ISS CBUFF Register Setup: [11] [12] [13]
- ISS CBUFF Registers: [14]

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Table 8-305. CBUFF_CTX_THRESHOLD_S_i

Address Offset	0x0000 0114 + (0x20 * i)	**Index**	i = 0 to 7
Physical Address	0x5200 1914 + (0x20 * i)	**Instance**	ISS_CBUFF
Description	Threshold value used to control the BCF synchronization mechanism		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								THRESHOLD																							

Bits	Field Name	Description	Type	Reset
31:24	RESERVED		R	0x00
23:0	THRESHOLD	Threshold value, in bytes	RW	0x000000

Table 8-306. Register Call Summary for Register CBUFF_CTX_THRESHOLD_S_i

ISS Interfaces

- ISS CBUFF Functional Description: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10]
- ISS CBUFF Register Setup: [11]
- ISS CBUFF Registers: [12]

Table 8-307. CBUFF_CTX_STATUS_i

Address Offset	0x0000 0118 + (0x20 * i)	**Index**	i = 0 to 7
Physical Address	0x5200 1918 + (0x20 * i)	**Instance**	ISS_CBUFF
Description	Status register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				WA				RESERVED				WB			

Bits	Field Name	Description	Type	Reset
31:12	RESERVED		R	0x00000
11:8	WA	Valid values depend on the CBUFF_CTX_CTRL__x.WCOUNT register.	R	0x0
7:4	RESERVED		R	0x0
3:0	WB	Valid values depend on the CBUFF_CTX_CTRL__x.WCOUNT register.	R	0x0

Table 8-308. Register Call Summary for Register CBUFF_CTX_STATUS_i

ISS Interfaces

- ISS CBUFF Interrupts: [0] [1] [2] [3] [4]
- ISS CBUFF Functional Description: [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23] [24] [25] [26] [27] [28]
- ISS CBUFF Registers: [29]

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Table 8-309. CBUFF_CTX_PHY_i

Address Offset	0x0000 011C + (0x20 * i)	**Index**	i = 0 to 7
Physical Address	0x5200 191C + (0x20 * i)	**Instance**	ISS_CBUFF
Description	Start address of the first physical buffer managed by the context when fragmentation support is disabled.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR																												RESERVED			

Bits	Field Name	Description	Type	Reset
31:4	ADDR	Address, in 128 bit words.	RW	0x0000000
3:0	RESERVED		R	0x0

Table 8-310. Register Call Summary for Register CBUFF_CTX_PHY_i

ISS Interfaces

- ISS CBUFF Functional Description: [0] [1]
- ISS CBUFF Register Setup: [2]
- ISS CBUFF Registers: [3]

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8.3 ISS ISP

This section describes the image signal processor.

8.3.1 ISS ISP Overview

The image signal processor (ISP) is part of the image subsystem (ISS) of the device and is a key component for imaging and video applications. It describes all ISP modules in the multimedia device; that is, the video port (VP), pattern generator (PG), image pipe interface (IPIPEIF), image pipe module (IPIPE), resizer (RSZ), hardware 3A (H3A), image sensor interface (ISIF), and buffer logic (BL).For better understanding, see the first top-level ISS diagram and feature list in Section 8.1, *ISS Overview*.

8.3.1.1 ISS ISP Features

The video-processing hardware removes the need for expensive camera modules to perform processing functions. The ISS can support the following features:

- On-the-fly or memory-to-memory processing
- Up to 200-MHz pixel throughput.
- Statistic data collection:
  - On-the-fly or memory-to-memory operation
  - Data collection for auto exposure
  - Data collection for auto white balance
  - Data collection for auto focus
  - Boundary signal calculation for video stabilization
- IPIPE front end: RAW data processing:
  - On-the-fly or memory-to-memory processing
  - 16-bit-wide RAW BAYER data path between image and sensor linearization module
  - 12-bit-wide RAW BAYER data path between sensor linearization module and gamma correction module. Gamma correction module outputs 10-bit data.
  - Programmable Bayer RGB positions
  - Sensor data linearization for dynamic range extension
  - Programmable 2D lens shading compensation (LSC) correction
  - Per-pixel gain and offset control
  - Black level compensation
  - Boxcar filter
  - Data collection for histogram generation
  - Defect pixel correction (LUT_DPC) with look-up table (LUT)
  - Defect pixel correction (OTF_DPC) with on-the-fly detection and correction
  - 2D noise filtering
  - Green imbalance correction (GIC)
  - Digital gains and offset
  - 8- to 10-bit A-law decompression and 10- to 8-bit A-law compression
- IPIPE back end: RGB and YUV data processing:
  - RGB-to-RGB color correction
  - Gamma correction (GC).
  - RGB - YUV4:2:2: Color conversion, cosited chroma filtering and downsampling
  - 2D edge enhancement (EE)
  - 3D LUT for color correction
  - False chroma suppression (FCS)
- Two resizers:

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- Performance: input and output rates up to 200 MPix/s
- YUV4:2:2 to RGB56, ARGB888, YUV4:2:2, and YUV4:2:0 data output
- YUV4:2:0 to YUV4:2:0 data output
- RAW to RAW data output
- Range from x1/4096 to x20. Supports memory-to-memory rescaling.

The ISP comprises the following modules:

- Pattern generator (PG)
- IPIPE interface (IPIPEIF)
- Image sensor interface (ISIF) accelerator
- Auto exposure, auto white balance, and auto focus engine (H3A)
- Image pipe accelerator (IPIPE)
- Two resizer (RSZ) accelerators
- Buffer logic (BL): Receives module requests, performs arbitration, and creates read/write bursts to the memory subsystem

8.3.1.2 ISS ISP Block Diagram

Figure 8-107 is the ISP top-level block diagram. The ISS supports four simultaneous pixel flows (CCP2, CSI2 A, CSI2 B, and parallel interface [CPI]), but only one of them at a time can use the video-processing hardware; the others can go directly to memory (CPI must always use ISP).

The ISP master port is connected to the level 3 (L3) interconnect, and the slave port is connected to the level 4 (L4) interconnect.

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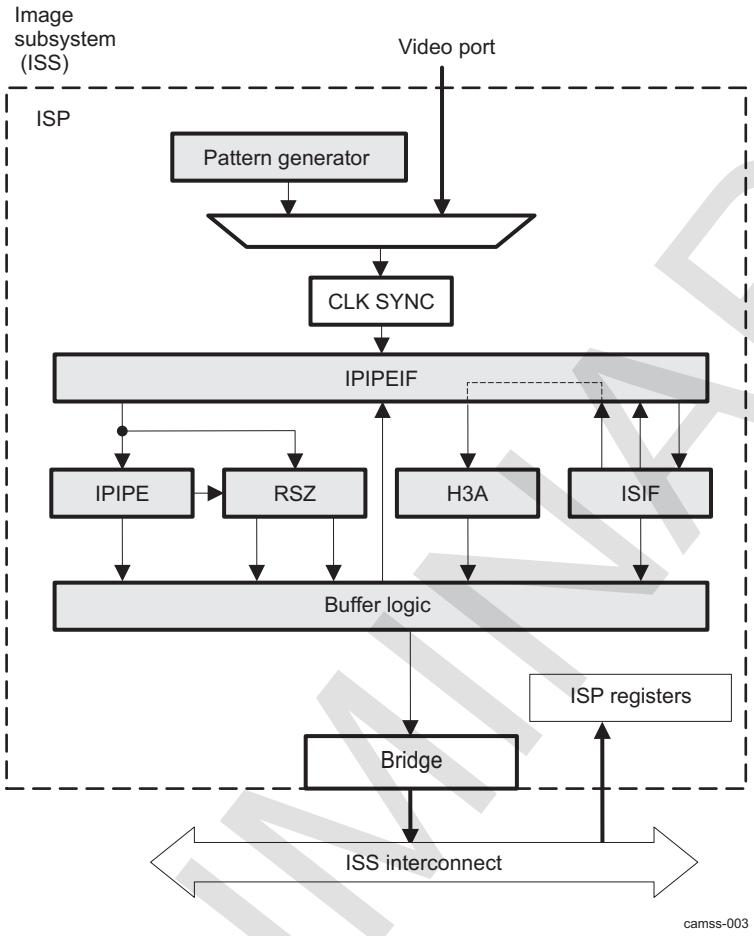
Figure 8-107. ISS ISP Block Diagram



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8.3.2 ISS ISP Integration

This section describes the integration of the ISP modules in the ISP and includes information about clocks, resets, and hardware requests.

The ISP is part of the ISS of the device and is a key component for imaging and video applications such as camera viewfinder, video record, and still image capture.

ISS is coupled with a low interrupt latency ISS microprocessor unit (MPU) subsystem running a real-time operating system to reach optimal performance. Primarily, the ISS MPU subsystem can quickly change the ISS configuration during frame blanking periods and run some sequencing tasks.

8.3.2.1 ISS ISP PRCM Interface

The ISP and its internal modules, as integrated in the ISS, use the same power and clock management details. See Section 8.1.2, *ISS Functional Description*, for the ISP top-level power, reset, and clock management (PRCM) Interface.

8.3.2.1.1 ISS ISP Clocks

The PRCM module, through the local power and clock management inside the ISS, provides a unique PCLK that can be enabled from the ISP5_CTRL register.

The modules inside the ISP require three clocks:

- PCLK: This clock is asynchronous to the other clocks. It is provided by the module sending the data to the IPIPEIF module on the VP.
- ISS_ FCLK: This clock is synchronous with the configuration clock domain. This is the clock used for the MTC interface.
- GCK_MMR: This is the clock for the configuration bus. It is created from the ISS_FCLK and runs at half the speed of the ISS_FCLK.

8.3.2.1.2 ISS ISP Reset

The ISP supports global software reset along with internal hardware reset, if needed.

Software reset is done through the ISP5_SYSCONFIG[1] SOFTRESET bit. Before issuing a software reset, the ISP must be in standby mode. The following must be done:

1. Ensure that the interfaces are stopped from sending data and/or the ISP modules are disabled. Before reset, the last interrupt triggered by the ISP when the frame processing completes is RSZ_INT_DMA. RSZ_INT_DMA must be used to enable clean termination of the processing. Software must wait a few hundred cycles to trigger a soft reset after RSZ_INT_DMA is asserted; this is to ensure that the BL is completely drained.
2. Ensure that ISP5_SYSCONFIG[5:4] STANDBYMODE = 2 (smart standby). Write the ISP5_CTRL[24] MSTANDBY bit to 1 and poll for ISP5_CTRL[20] MSTANDBY_WAIT = 1. Then, the soft reset can be applied (ISP5_SYSCONFIG[1] SOFTRESET = 1).

In case an ISP overflow or underflow event happens (for example, RSZ_FIFO_OVF, ISIF_OVF, etc.), it is not sufficient to reset the ISP. In that case a reset must take place at the ISS level.

8.3.2.2 ISS ISP Interrupt Tree

Table 8-311 summarizes the submodule interrupts that can be mapped to the four ISP interrupt output lines. After this, these output lines are mapped to the ISS top interrupt request (IRQ) merger (for more information, see Section 8.1.2). Software enables the explained before merger from the top-level ISS resources registers in Section 8.1.2.

Table 8-311. ISS ISP Interrupt Tree Table

Register	Module	Destination	Comments
ISP5_IRQENABLE_SET_i[9] IPIPEIF_IRQ	IPIPEIF	ISP to ISS merger four IRQ lines	See Section 8.3.2.4.1.

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Table 8-311. ISS ISP Interrupt Tree Table (continued)

Register	Module	Destination	Comments
ISP5_IRQENABLE_SET2_i[1] IPIPEIF_UDF			
ISP5_IRQENABLE_SET_i[29] IPIPE_INT_DPC_RNEW1	IPIPE		See Section 8.3.2.5.1.
ISP5_IRQENABLE_SET_i[28] IPIPE_INT_DPC_RNEW0			
ISP5_IRQENABLE_SET_i[27] IPIPE_INT_DPC_INI			
ISP5_IRQENABLE_SET_i[8] IPIPE_INT_HST			
ISP5_IRQENABLE_SET_i[7] IPIPE_INT_BSC			
ISP5_IRQENABLE_SET_i[6] IPIPE_INT_DMA			
ISP5_IRQENABLE_SET_i[5] IPIPE_INT_LAST_PIX			
ISP5_IRQENABLE_SET_i[4] IPIPE_INT_REG			
ISP5_IRQENABLE_SET_i[25] IPIPE_INT_EOF			
ISP5_IRQENABLE_SET2_i[4] IPIPE_HST_ERR			
ISP5_IRQENABLE_SET2_i[2] IPIPE_BOXCAR_OVF			
ISP5_IRQENABLE_SET_i[12] H3A_INT	H3A		See Section 8.3.2.7.
ISP5_IRQENABLE_SET_i[24] H3A_INT_EOF			
ISP5_IRQENABLE_SET2_i[0] H3A_OVF			
ISP5_IRQENABLE_SET_i[23] RSZ_INT_EOF1	RSZ		See Section 8.3.2.6.2.
ISP5_IRQENABLE_SET_i[22] RSZ_INT_EOF0			
ISP5_IRQENABLE_SET_i[19] RSZ_FIFO_IN_BLK_ERR			
ISP5_IRQENABLE_SET_i[18] RSZ_FIFO_OVF			
ISP5_IRQENABLE_SET_i[17] RSZ_INT_CYC_RZB			
ISP5_IRQENABLE_SET_i[16] RSZ_INT_CYC_RZA			
ISP5_IRQENABLE_SET_i[15] RSZ_INT_DMA			
ISP5_IRQENABLE_SET_i[14] RSZ_INT_LAST_PIX			
ISP5_IRQENABLE_SET_i[13] RSZ_INT_REG			
ISP5_IRQENABLE_SET_i[3] ISIF_INT_3	ISIF		See Section 8.3.2.8.1.
ISP5_IRQENABLE_SET_i[2] ISIF_INT_2			
ISP5_IRQENABLE_SET_i[1] ISIF_INT_1			
ISP5_IRQENABLE_SET_i[0] ISIF_INT_0			
ISP5_IRQENABLE_SET2_i[3] ISIF_OVF			

8.3.2.3 ISS ISP PG Integration

See Section 8.3.2, *ISS ISP Integration*.

8.3.2.4 ISS ISP IPIPEIF Integration

8.3.2.4.1 ISS ISP IPIPEIF Interrupts

The IPIPEIF module generates two interrupts, one generic and one:

- IPIPEIF_IRQ: This event is triggered to the BL module when a new frame starts (VS signal). The interrupt is active low and is asserted for one GCK_MMR clock cycle.
- IPIPEIF_UDF: Interrupt generated when an underflow happens in the IPIPEIF module. Underflow events are nonrecoverable at the ISP level and a soft reset is required at the ISS level.

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The interrupts are enabled from the ISP5_IRQENABLE_SET_i[9] IPIPEIF_IRQ and ISP5_IRQENABLE_SET2_i[1] IPIPEIF_UDF bits (where i = 0 to 3 for the line that will be mapped to the four lines of the ISP). Then, each line from the ISP is sent to the ISS top level, where it is muxed with other ISS modules for a total output of six interrupt lines. See Section 8.1.2, *ISP Top -Level Integration.*

8.3.2.5 ISS ISP IPIPE Integration

8.3.2.5.1 ISS ISP IPIPE Interrupts

IPIPE can generate several interrupts:

- IPIPE_INT_DPC_RNEW: This event is triggered when there is permission to initialize LUT-DPC table lines 0 and 1.
- IPIPE_INT_DPC_INI: This event is triggered when the defect pixel correction (DPC) table is initialized.
- IPIPE_INT_HST: This event is triggered when the histogram is done.
- IPIPE_INT_BSC: This event is triggered when boundary signal calculation is done.
- IPIPE_INT_DMA: This event is triggered when the boxcar SDRAM transfer is done. On this timing, IPIPE_INT_EOF is sent to the BL. This event is active high for one GCK_MMR clock cycle.
- IPIPE_INT_LAST_PIX: This event is triggered when the last pixel of a frame comes into IPIPE. This event is active high for one GCK_MMR clock cycle.
- IPIPE_INT_EOF: This event is triggered for end of frame.
- IPIPE_BOXCAR_OVF: This event is generated when an overflow happens in the IPIPE-BOXCAR output buffer. The interrupt avoids polling the IPIPE_SRC_STA[0] VAL0 bit for errors. Overflow events are nonrecoverable at the ISP level and a soft reset is required at the ISS level.
- IPIPE_HST_ERR: This event is triggered when the MPU or system direct memory access (sDMA) is still reading the memory that is being used by the module. This is an indication that the read operation was not fast enough.

The interrupts are enabled from the ISP5_IRQENABLE_SET_i and ISP5_IRQENABLE_SET2_i registers (where i = 0 to 3 for the line that will be mapped to the four lines of the ISP). Then, each line from the ISP is sent to the ISS top level, where it is muxed with other ISS modules for a total output of six interrupt lines. See Section 8.1.2, *ISP Top-Level Integration.*

8.3.2.5.2 ISS ISP DMA Requests

The ISP generally outputs four direct memory access (DMA) requests, which can be used to read or write memories inside the IPIPE module. These memories are:

- BSC memory: This memory must be read during a vertical blanking period. It is used by the video stabilization application.
- HIST memory: This memory must be read during a vertical blanking period. It is used by the 3A application. The HIST data is double-buffered from frame-to-frame. Software must select the memory that is to be used by setting the IPIPE_HST_TBL[0] SEL bit.
- GAMMA memory: This memory must be set during a vertical blanking period. The imaging application typically uses multiple gamma tables.
- DPC memory: This memory must be set during a frame acquisition. The memory is not big enough to store all faulty pixels for a given frame.

To generate the DMA requests, the following events must be used:

- The IPIPE_INT_BSC event is used to generate the DMA request for the BSC memory. It maps on DMA line 0, ISS_DMA0.
- The IPIPE_INT_HST event is used to generate the DMA request for the HIST memory. It maps on DMA line 1, ISS_DMA1. The HIST data is double-buffered from frame-to-frame. Software must select the memory that is to be used by setting the IPIPE_HST_TBL[0] SEL bit. When the DMA request is set, it is required to read 4KB from the ping buffer address (0x2000) or the pong buffer address (0x3000). Software must ensure that when one buffer is selected no other accesses (for example, MPU) take place in the other buffer.
- The IPIPE_INT_LAST_PIX event is used to generate the DMA request for the GAMMA memory. This

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same event can also be used to initialize the DPC LUT (not the preferred method; it is better to use IPIPE_INT_DPC_INI). Basically, when the last pixel is output from the IPIPE module, it is safe to modify the IPIPE memories. It maps on DMA line 3, ISS_DMA3.

- The IPIPE_INT_DPC_INI event signals that DPC table memory initialization can take place. IPIPE_INT_DPC_INI is used to generate two back-to-back DMA requests, the first one mapping on IPIPE_INT_DPC_RNEW0 and the second one mapping on IPIPE_INT_DPC_RNEW1. After initialization (steady state), the IPIPE_INT_DPC_RNEW0 and IPIPE_INT_DPC_RNEW1 events are used to generate the DMA request for the DPC LUT renewal. It maps on DMA line 2, ISS_DMA2. To select which event is used to initialize the DPC (IPIPE_INT_LAST_PIX or IPIPE_INT_DPC_INI), set the ISP5_CTRL[25] DPC_EVT_INI bit.

NOTE: The size of the DPC table in SDRAM must be a multiple of the number of DMA requests. It ensures that during burst capture mode the DMA always loads the correct data from frame-to-frame. The DMA automatically warps back to the start of the table after all expected DMA requests are received. There is a total of ceil(nb_faulty_pixel/128) + 2 DMA requests per frame when the IPIPE_INT_DPC_INI EVENT is used. Hence, the size of the DPC table in the SDRAM is (ceil(nb_faulty_pixel/128) + 2) × 128 × 32 bits.

NOTE: If DMA channels are not used but the MPU is used, an error check must be performed for IPIPE HST. See ISP5_CTRL[26] HST_RD_CHK for details.

The DMA request assertion and deassertion to the sDMA is automatic and no software intervention is needed. The ISP contains two registers (ISP5_DMAENABLE_SET and ISP5_DMAENABLE_CLR) that must be used to enable or disable generation of the DMA requests.

The DMA request deassertion is based on late deassertion; that is, the DMA request is disabled only when all the data corresponding to the transfer size have been read or written. To deassert the DMA request and generate the hw_eoi signal, hardware counts the number of 32-bit accesses that are done in the memory range of the corresponding DMA request through the ISP slave port. When the number of accesses corresponding to the DMA request is done, the DMA request is cleared. Multiple DMA requests can be active simultaneously.

Software must not attempt to read or write in the memory range of the DMA requests that are enabled because CPU accesses, instead of sDMA accesses, will be counted. Software can freely access ISP memories for which the DMA request is disabled, and can access registers while the sDMA performs the transfers.

8.3.2.6 ISS ISP RSZ Integration

8.3.2.6.1 ISS ISP RSZ PRCM Interface

8.3.2.6.1.1 ISS ISP RSZ Reset

The resizer module has no standalone software reset. RSZ must be reset at the ISP level. See Section 8.3.2.1.2, *ISS ISP Reset*.

8.3.2.6.2 ISS ISP RSZ Interrupts

RSZ can generate several interrupts:

- RSZ_INT_EOF0: This event is triggered for end of frame.
- RSZ_INT_EOF1: This event is triggered for end of frame.
- RSZ_FIFO_IN_BLK_ERR: This event is triggered when the minimum vertical blanking period has not been respected, thus causing errors in the input data buffering submodule. This event is triggered when the RSZ_INT_REG event of frame N is triggered before RSZ_INT_DMA of frame N + 1. This event typically happens at the transition between two frames because there is not enough vertical blanking between frames. Hardware cannot recover from this error. It requires a reset. It is a requirement that despite the error the RSZ module must finish correctly: ongoing requests are

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completed and further requests are blocked.

- RSZ_FIFO_OVF: This event is triggered when overflow happens in the input data buffering submodule. It typically occurs while processing a frame, because the VP pixel clock is too high. Because hardware cannot recover from this error, a reset is required. It is a requirement that despite the error the RSZ module must finish correctly: ongoing requests are completed and further requests are blocked.

  This event can be also triggered at the master write interface (MTC), where an MTC stall signal is generated.
- RSZ_INT_CYC_RZA/RSZ_INT_CYC_RZB: This event is triggered as circular interrupt every time that RSZ_IRQ_RZA/RSZ_IRQ_RZB output lines are written out to the RZA_SDR_Y/RZB_SDR_Y buffer. The range can go from 1 to 8192 lines. Usually, this value must be such that the circular buffer vertical size (set by the RZBA_SDR_Y_PTR_E/RZBB_SDR_Y_PTR_E register) is a multiple of RSZ_IRQ_RZA/RSZ_IRQ_RZA.
- RSZ_INT_DMA: This event is triggered when the last EOF (of the two MTC interfaces) is sent out to the BL and the RSZ core returns to idle. This event is active high for one GCK_MMR clock cycle.
- RSZ_INT_LAST_PIX: This event is triggered when the last pixel of the valid area is received. This event is active high for one GCK_MMR clock cycle.
- RSZ_INT_REG: This event is triggered when the new value of the shadowed registers, if updated, takes effect on the next RSZ_INT_REG event. Then again, shadowed registers can be updated for the next frame after the RSZ_INT_REG event is triggered. This event is active high for one GCK_MMR clock cycle.

The interrupts are enabled from the ISP5_IRQENABLE_SET_i register (where i = 0 to 3 for the line that will be mapped to the four lines of the ISP). Then, each line from the ISP is sent to the ISS top level, where it is muxed with other ISS modules for a total output of six interrupt lines. See Section 8.1.2, *ISP Top-Level Integration.*

8.3.2.7 ISS ISP H3A Integration

8.3.2.7.1 ISS ISP H3A Interrupts

H3A can generate the following interrupts:

- H3A_INT: This event is triggered at the end of the last window or last paxel, whichever completes last. This always triggers at the same time as H3A_INT_EOF.
- H3A_INT_EOF: This event is triggered and generated at the end of the last window. This event is active high for one GCK_MMR clock cycle.
- H3A_OVF: This interrupt is generated when an overflow happens in the H3A output buffer. The interrupt avoids polling the H3A_PCR[21] OVF bit for errors. Overflow events are nonrecoverable at the ISP level and a soft reset is required at the ISS level. The event is active high for one GCK_MMR clock cycle.

The interrupts are enabled from ISP5_IRQENABLE_SET_i and ISP5_IRQENABLE_SET2_i (where i = 0 to 3 for the line that will be mapped to the four lines of the ISP). Then, each line from the ISP is sent to the ISS top level, where it is muxed with other ISS modules for a total output of six interrupt lines. See Section 8.1.2*, ISP Top-Level Integration.*

8.3.2.8 ISS ISP ISIF Integration

8.3.2.8.1 ISS ISP ISIF Interrupts

The ISIF can generate several interrupts:

- ISIF_INT_0: This event is triggered when the VD0 interrupt on line 0 is configured. The VD0 interrupt can be configured based on the VD position. It is asserted after receiving the number of horizontal lines (horizontal pulse signals) set in VDINT0. See Section 8.3.3.7.19.1 for more information.
- ISIF_INT_1: This event is triggered when the VD1 interrupt on line 1 is configured. The VD1 interrupt can be configured based on the VD position. It is asserted after receiving the number of horizontal lines (horizontal pulse signals) set in VDINT1. See Section 8.3.3.7.19.1 for more information.

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- ISIF_INT_2: This event is triggered when the VD2 interrupt on line 2 is configured. The VD2 interrupt can be configured based on the VD position. It is asserted after receiving the number of horizontal lines (horizontal pulse signals) set in VDINT2. See Section 8.3.3.7.19.1 for more information.
- ISIF_INT_3: This event is triggered LSC interrupt is an interrupt issued by the 2D-LSC block. See Section 8.3.3.7.10.1.5 for more information.
- ISIF_OVF: This Interrupt is generated when an underflow happens in the ISIF module. The interrupt avoids polling the ISIF_MODESET[11] OVF bit for errors.

The interrupts are enabled from the ISP5_IRQENABLE_SET_i and ISP5_IRQENABLE_SET2_i registers (where i = 0 to 3 for the line that will be mapped to the four lines of the ISP). Then, each line from ISP is sent to the ISS top level where it is muxed with other ISS modules for a total output of six interrupt lines. See Section 8.1.2*, ISP Top-Level integration.*

8.3.2.9 ISS ISP BL Integration

See Section 8.3.2, *ISS ISP Integration*.

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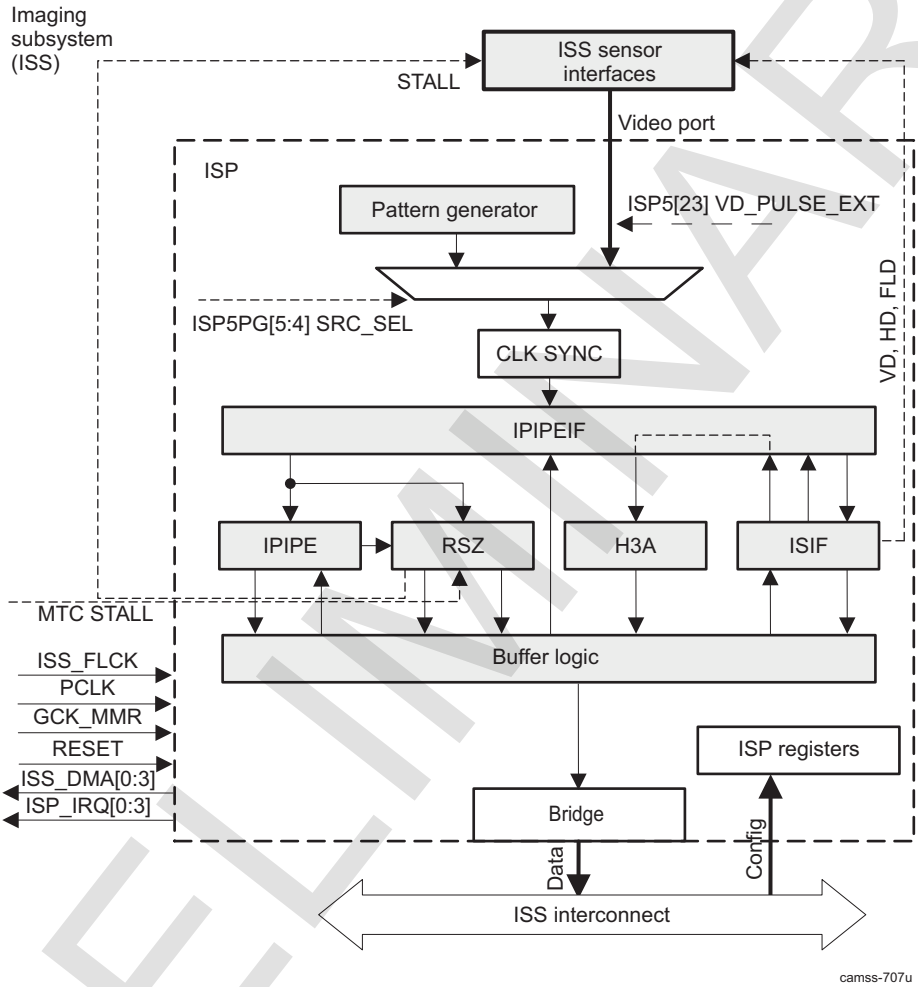
8.3.3 ISS ISP Functional Description

The functionality of the ISP is part of the overall performance of the ISS. For the top-level ISS diagram with ISP inside and for a features list, see Section 8.1, *ISS Overview*. Figure 8-108 is an overview of the ISP module. It outputs DMA and interrupt requests, has clocks coming in, and a stall signal to the CCP2 interface receiver from the resizer. It also shows the top-level configuration for input to IPIPEIF. For the scaled-in functional details of each submodule inside the ISP, see its functional description section.

Figure 8-108. ISS ISP High-Level Diagram



8.3.3.1 ISS ISP VP Functional Description

8.3.3.1.1 ISS ISP VP Overview

The VP supports a parallel interface that is used for interfacing with image sensors. The ISP VP can transport 8- to 16-bit RAW data and 8-/16-bit YCbCr data.

Figure 8-109 shows the VP module connections to other submodules of the ISP.

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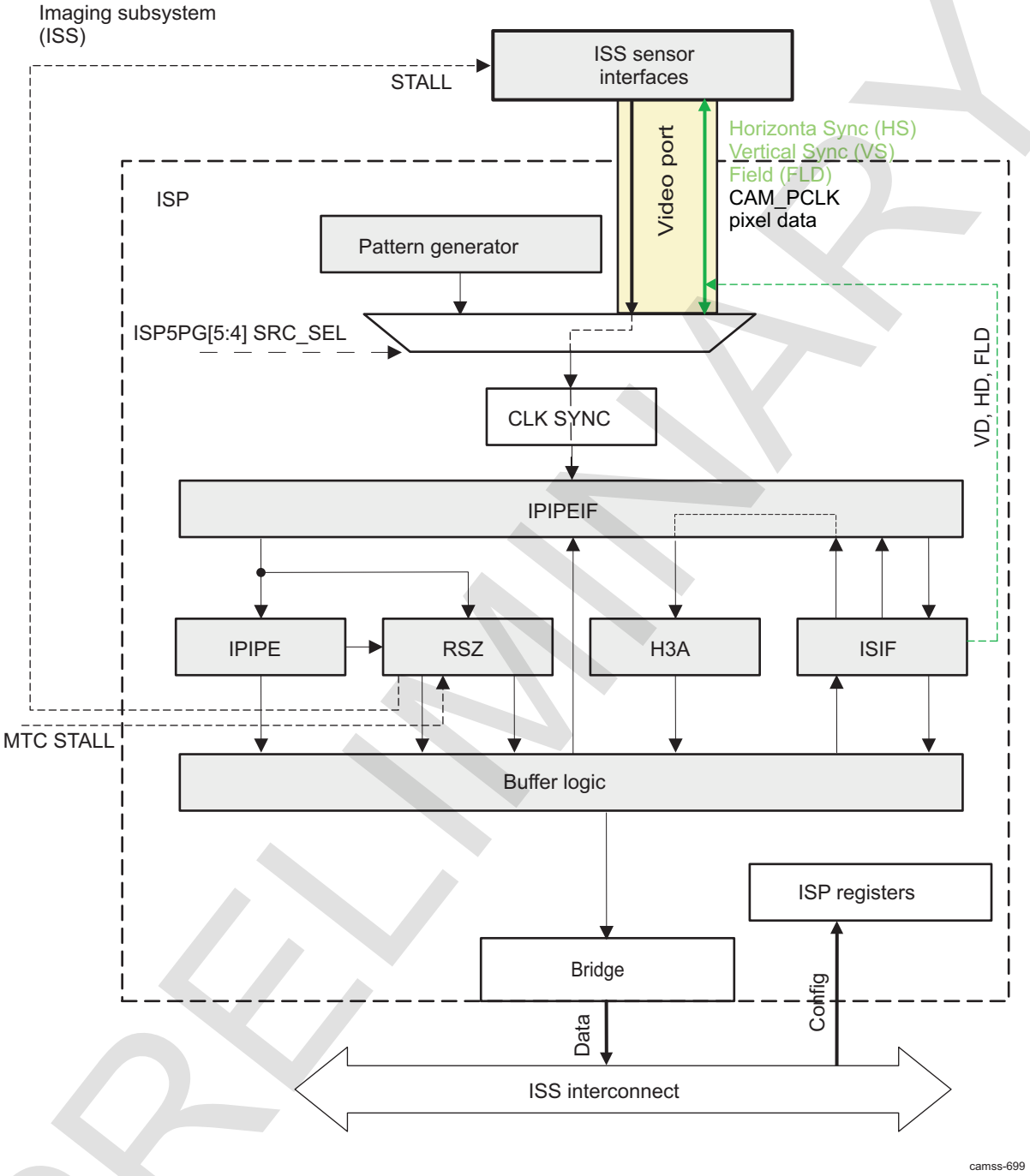
Figure 8-109. ISS ISP VP High-Level Diagram



8.3.3.1.2 ISS ISP VP Data Formats

The VP can be used to connect external camera receivers to the ISS. Data paths inside the ISP hardware depend on the image format sourced by the sensor (RAW RGB, YUV4:2:2, JPEG, etc.). Table 8-312 shows how the CCP2/CSI2 modules are connected to the VP in function of the image format.

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Table 8-312. ISS ISP VP Format Mapping

Source		Format	Connected to																ISIF	Data Provided to ISIF Linearization Engine																	
CCP2	CSI2		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	GWDI	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	RAW16	R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0	R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0
X	X	RAW14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0	0	0	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0	0
			0	0	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	1	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0	0
X	X	RAW12	0	0	0	0	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0	0	0	0
			0	0	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0	0	1	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0	0	0	0
			R11	R10	R9	R8	R7	R5	R5	R4	R3	R2	R1	R0	0	0	0	0	2	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0	0	0	0
X	X	RAW10	0	0	0	0	0	0	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0	0	0	0	0	0
			0	0	0	0	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0	0	1	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0	0	0	0	0	0
			0	0	R9	R8	R7	R5	R5	R4	R3	R2	R1	R0	0	0	0	0	2	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0	0	0	0	0	0
			R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0	0	0	0	0	0	3	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0	0	0	0	0	0
X	X	RAW8								R8	R7	R6	R5	R4	R3	R2	R1	R0	0	R7	R6	R5	R4	R3	R2	R1	R0	0	0	0	0	0	0	0	0
									R7	R6	R5	R4	R3	R2	R1	R0			1	R7	R6	R5	R4	R3	R2	R1	R0	0	0	0	0	0	0	0	0
							R7	R6	R5	R4	R3	R2	R1	R0					2	R7	R6	R5	R4	R3	R2	R1	R0	0	0	0	0	0	0	0	0
					R7	R6	R5	R4	R3	R2	R1	R0							3	R7	R6	R5	R4	R3	R2	R1	R0	0	0	0	0	0	0	0	0
			R7	R5	R5	R4	R3	R2	R1	R0									4	R7	R6	R5	R4	R3	R2	R1	R0	0	0	0	0	0	0	0	0
		YUV16-bit	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	C7	C6	C5	C4	C3	C2	C1	C0	0																	
		YUV8-bit									YC7	YC6	YC5	YC4	YC3	YC2	YC1	YC0	0																	

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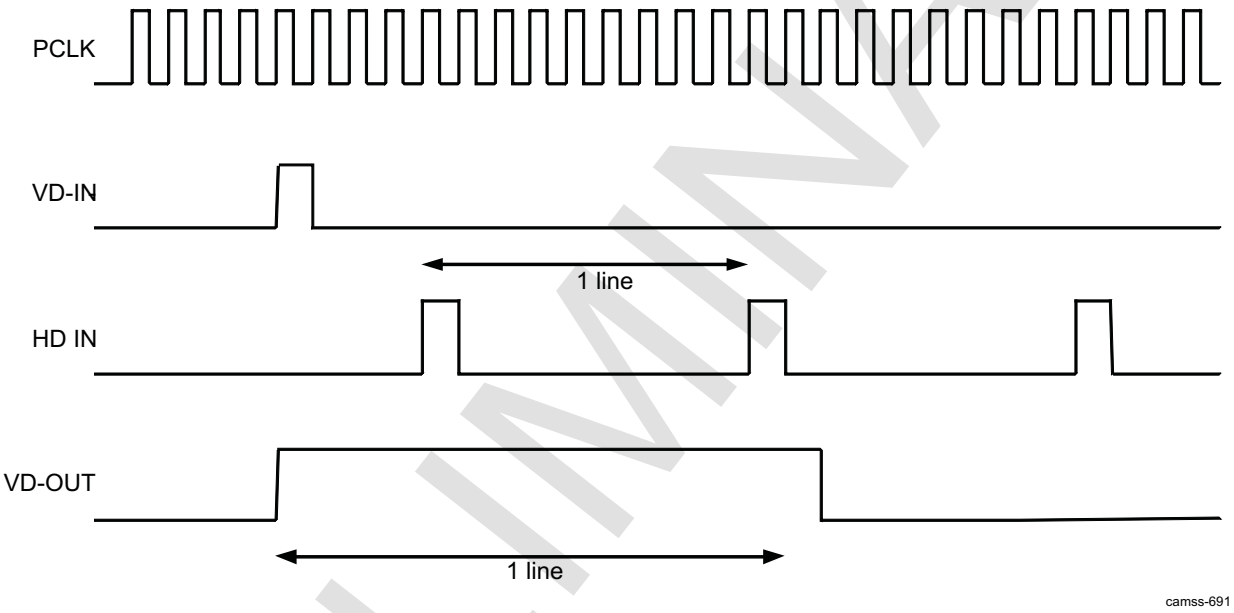
8.3.3.1.3 ISS ISP VP Top-Level Communication With CCP2 RX and CSI2 RX

At the ISS level, the VP is connected to the VP of the CCP2 RX and CSI2 RX modules. VP implementation differences force the introduction of a bridge between the CCP2 RX/CIS2 RX modules and the VP. The role of the bridge is to perform VD pulse extension. The CCP2 RX module assumes that the VD signal is active for at least one pixel clock cycle, and the CSI2 RX module assumes that the VD signal is asserted for four pixel clock cycles. However, the ISP assumes that the VD pulse is active on at least one line.

Figure 8-110 shows how the VD pulse extension works. Assume that VD-IN is the VD signal at the input of the pulse extension bridge, and VD-OUT is the VD signal at the output of the pulse extension bridge.

The VD-OUT signal is asserted at the same time as VD-IN. The VD-OUT signal is kept high until one full line is received. A line is delimited by two rising edges of the HD signal. The VD-OUT pulse is deasserted on the next cycle after the falling edge of the HD signal.

Figure 8-110. ISS ISP VP VD Pulse



The ISP5_CTRL[23] VD_PULSE_EXT bit controls whether the VD extension bridge is enabled or disabled. By default, the bridge is enabled. When the bridge is disabled, the VD pulse must be unmodified: VD-OUT = VD-IN. At the ISS level, it is expected that ISP5_CTRL [23] VD_PULSE_EXT = 1 when the VP gets data from the CSI2 RX modules and ISP5_CTRL[23] VD_PULSE_EXT = 0 when the VP gets data from the parallel interface or CCP2 RX module.

CAUTION

A minimum of four lines per frame is required on the VP when the VD pulse extension bridge is enabled; therefore, the VD extension bridge is not functional if a 1-/2-/3-line frame is sent to the VP.

8.3.3.1.4 ISS ISP VP Pixel Clock Inversion

The ISP always uses the rising edge of the pixel clock to sample the pixel data. The ISP provides the capability to invert the pixel clock so it can shift the resampling of a pixel clock period by half. This is controlled by the ISP5_CTRL[22] PCLK_INV bit. By default, the inversion is disabled. The 5 bits in Table 8-313 are resynchronized from the GCK_MMR clock domain to the PCLK clock domain. There must be at least three clock cycles between the time these bits are modified and the HD/VD pulse for start of frame comes.

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Table 8-313. ISS ISP VP GCK_MMR to PCLK Clock Resynchronization

Module	Register	Bit Field
ISP	ISP5_CTRL	VD_PULSE_EXT
ISIF	ISIF_MODESET	HDVDD
ISIF	ISIF_MODESET	FIDD
ISP	ISP5_CTRL	ISIF_CLK_ENABLE

8.3.3.2 ISS ISP PG Functional Description

8.3.3.2.1 ISS ISP PG Overview

The PG implements an internal data generation mechanism to test the external pins and can generate RAW data (to the IPIPEIF, ISIF, and other ISP modules) without the need for an external image sensor.

Figure 8-111 show the PG module connections to other submodules of the ISP.

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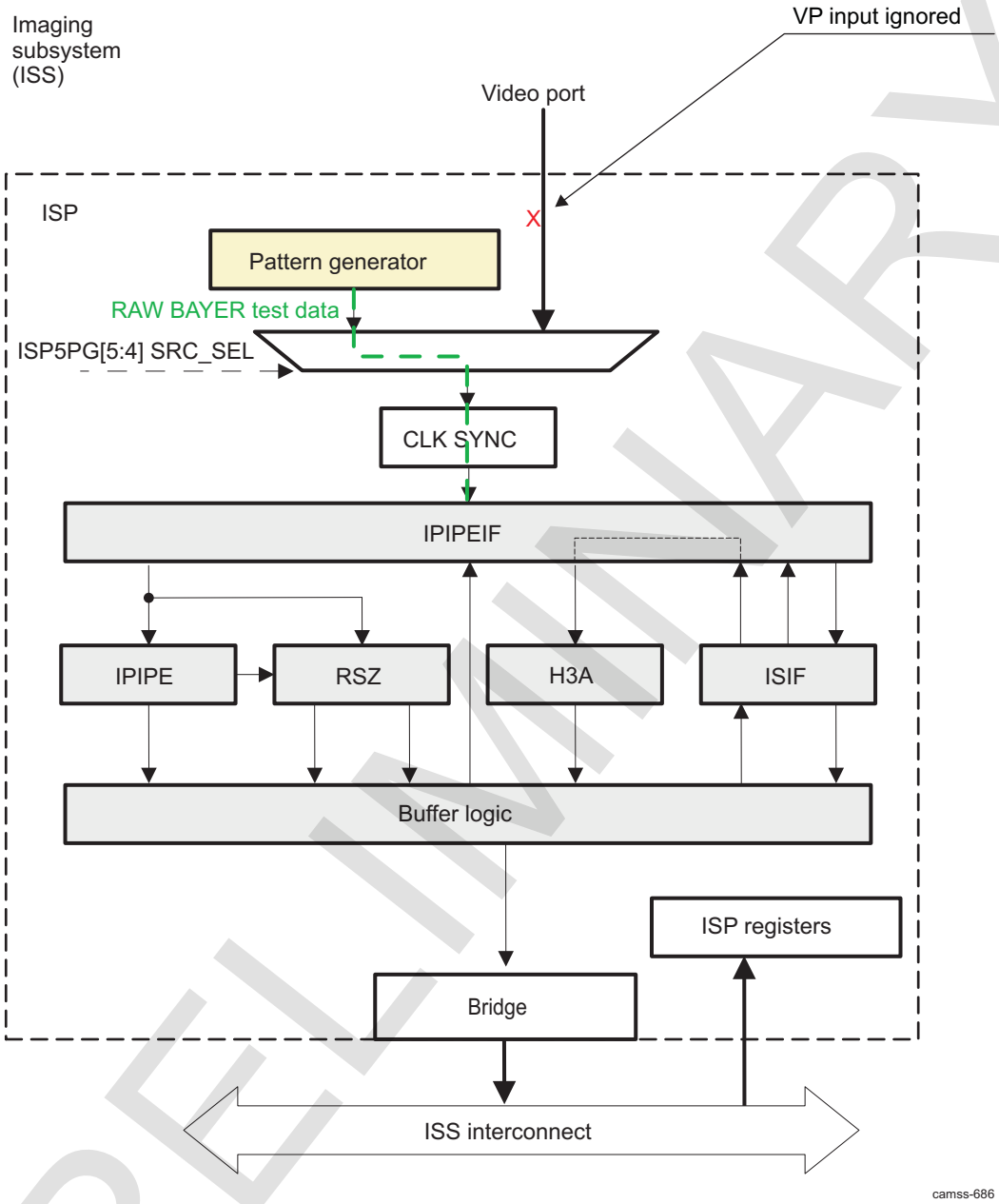
Figure 8-111. ISS ISP PG High-Level Diagram



8.3.3.2.2 ISS ISP PG Functional Description

The data pattern is as follows:

- Data remain unchanged from frame to frame.
- Data are always generated as a BAYER pattern with RED (only on even/even pixel/line; other locations are RED = 0), GREEN (only on odd/even pixel/line and even/odd pixel/line; other locations are GREEN = 0) and BLUE (only on odd/odd pixel/line; other locations are BLUE = 0) colors.
- The frame is divided into four equal horizontal sections:
  - 1st horizontal section is further divided into eight equal vertical sections
    - 1st vertical section is RED only with maximum value (depending on number of bits programmed).
    - 2nd vertical section is RED and GREEN with maximum value.

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- 3rd vertical section is RED, GREEN, and BLUE with maximum value.
- 4th vertical section RED and BLUE with maximum value.
- 5th vertical section is all zeros.
- 6th vertical section is GREEN and BLUE with maximum value.
- 7th vertical section is GREEN with maximum value.
- 8th vertical section is BLUE with maximum value.

– 2nd horizontal section is all RED with the pixel value linearly incrementing (reset to zero for each line) from zero onward.
– 3rd horizontal section is all GREEN with the pixel value linearly incrementing (reset to zero for each line) from zero onward.
– 4th horizontal section is all BLUE with the pixel value linearly incrementing (reset to zero for each line) from zero onward.

By default, the ISP source is the VP. To select PG as the source for the ISP, set the ISP5_PG[5:4] SRC_SEL bit field to 0x3.

The ISP5_PG[2] WEN bit controls write-enable signal generation for the PG module. There are two modes: the write enable signal is enabled all the time or it is enabled and disabled every eight clock cycles. The ISP5_PG[1] HDPOL and ISP5_PG[0] VDPOL bits control the polarity of the horizontal and vertical synchronization signals generated by the PG module. These signals can be active high or active low.

The ISP5_PG_PULSE_CTRL register controls the HS and VS signal widths for the PG module.

- The ISP5_PG_PULSE_CTRL[12:0] HDW bit field sets the duration of the HD signal in terms of pixel clock cycles. The actual duration of the signal is ISP5_PG_PULSE_CTRL[12:0] HDW + 1 cycle. The minimum signal duration is one cycle, and the maximum signal duration is 4096 cycles.
- The ISP5_PG_PULSE_CTRL[27:16] VDW bit field sets the duration of the VD signal in terms of lines. The actual duration of the signal is ISP5_PG_PULSE_CTRL[27:16] VDW + 1 line. The minimum signal duration is one line, and the maximum signal duration is 4096 lines.

The ISP5_PG_FRAME_SIZE register controls the PG module horizontal and vertical frame sizes.

- The ISP5_PG_FRAME_SIZE[31:16] PPLN bit field sets the number of pixels per line a frame generated by the PG module. The actual number of pixels in a line is set by ISP5_PG_FRAME_SIZE[31:16] FRAME_PPLN + 1. The minimum number of pixels is 1.
- ISP5_PG_FRAME_SIZE[15:0] HLPFR sets the number of lines per frame generated by the PG module. The actual number lines is set by ISP5_PG_FRAME_SIZE[15:0] HLPFR + 1. The minimum number of lines is one.

The ISP5_PG[3] EN bit enables or disables the PG module.

8.3.3.3 ISS ISP IPIPEIF Functional Description

8.3.3.3.1 ISS ISP IPIPEIF Overview

The IPIPEIF module provides data and synchronization signals (HD, VD) for the ISIF, IPIPE, RSZ, and H3A modules. The data source of this module is the VP, ISIF, or SDRAM using BL, and the selected data is output to ISIF, IPIPE, H3A, and RSZ. This module supports:

- Up to 16-bpp data on the VP
- Up to 200-MHz pixel clock on the VP, up to 8K × 8K imaging resolution
- RAW and YUV data formats on the VP and BL ports
- Dark-frame subtract of 8-bit RAW image stored in SDRAM from image from VP
- Dark-frame subtract of 8-bit RAW image stored in SDRAM from image from ISIF
- Dark-frame subtract of 8-bit RAW image from VP from image read from SDRAM through the BL
- Simple defect correction to prevent the subtraction of defect pixels
- 8-10, 8-12 DPCM of 10-8, 12-8 DPCM compressed data in SDRAM

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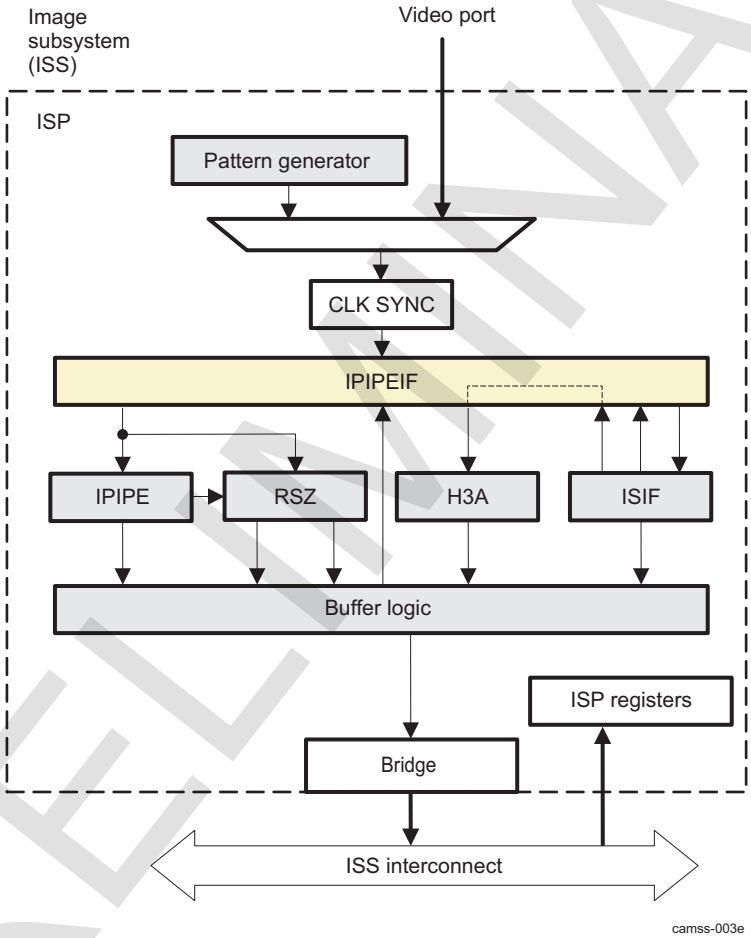
- Simple and advanced DPCM predictor
- Inverse A-Law decompression of RAW data 10-8 A-Law compressed from SDRAM
- 8-bit, 12-bit unpacking of 8-bit,12-bit packed SDRAM data
- Gain multiply for output data to IPIPE module
- Horizontal Bayer rescaler in the data paths to the IPIPE and H3A modules: Supports (1, 2, 1) averager filter and supports horizontal pixel decimation
- Data rate control when reading data from SDRAM: Fraction clock divider
- (1, 2, 1) averager filter and supports horizontal pixel decimation in the data path to the IPIPE for YUV data.

Figure 8-112 show the IPIPEIF module connections to other submodules of the ISP.

Figure 8-112. ISS ISP IPIPEIF High-Level Diagram



8.3.3.3.2 ISS ISP IPIPEIF Top-Level Block Diagram

The following sections describe the function of each subblock in the IPIPEIF, as shown in Figure 8-113.

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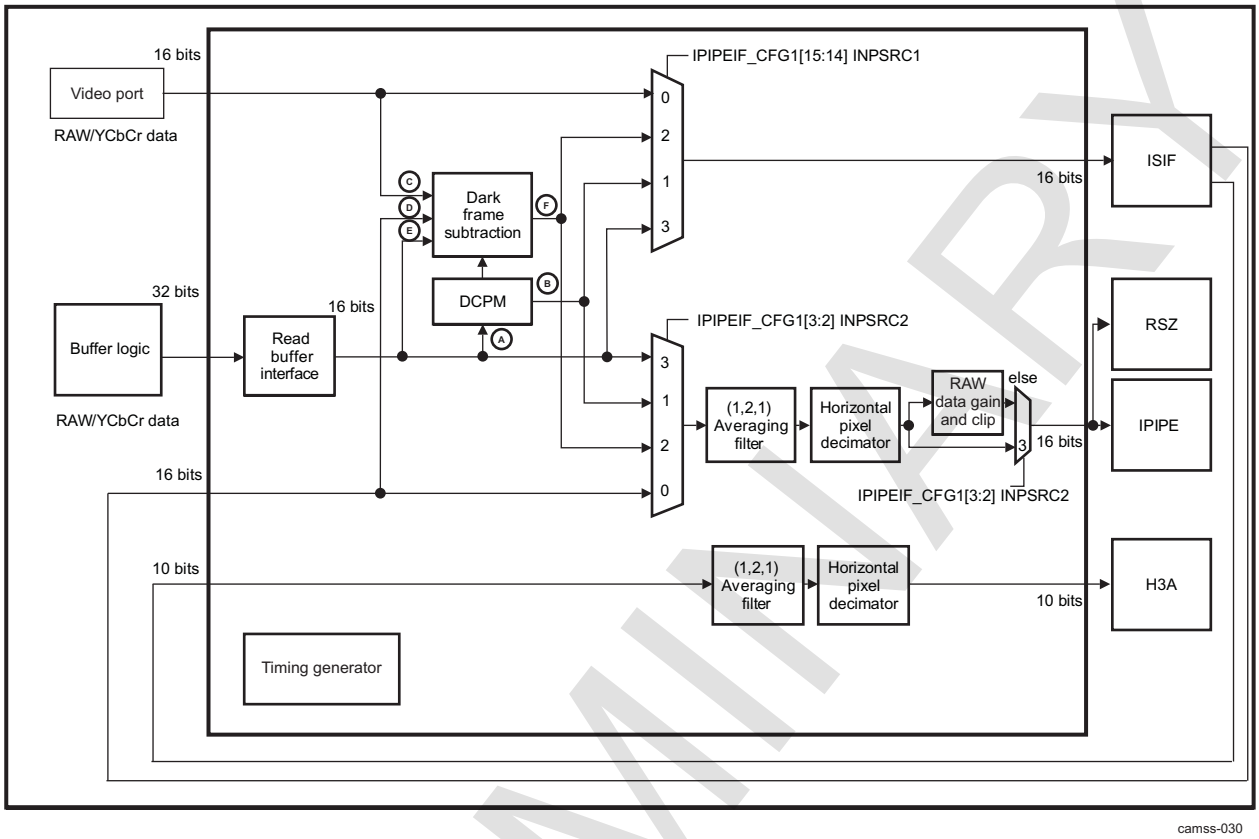
Figure 8-113. ISS ISP IPIPEIF Top-Level Block Diagram



NOTE: When the IPIPEIF receives data from the VP, the timing generator must be configured for HD, VD, and WEN. For more information, see Section 8.3.3.3.5, *ISS ISP IPIPEIF Timing Generation.*

8.3.3.3.3 ISS ISP IPIPEIF Input Interface

The IPIPEIF module comprises two major interface blocks: VP and BL. The data types can be RAW or YUV.

8.3.3.3.3.1 ISS ISP IPIPEIF Input From VP

The VP typically receives data from the image sensor. At the ISS level, it is connected to the serial interface receivers.

8.3.3.3.3.2 ISS ISP IPIPEIF Input From BL

The BL is the interface with the memory (SDRAM). In that case, the SDRAM address and line offset registers must be programmed in units of 32 bytes.

- SDRAM start address (byte) = (IPIPEIF_ADDRU[10:0] ADDRU)16 + (IPIPEIF_ADDRL[15:0] ADDRL)
- SDRAM address offset (byte) = IPIPEIF_ADOFS[11:0] ADOFS

Two types of data can be stored in memory: pixel data and dark frame data.

For pixel data, the HD and VD signals are reconstructed with:

- IPIPEIF_HNUM
- IPIPEIF_VNUM

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- IPIPEIF_LPFR
- IPIPEIF_PPLN

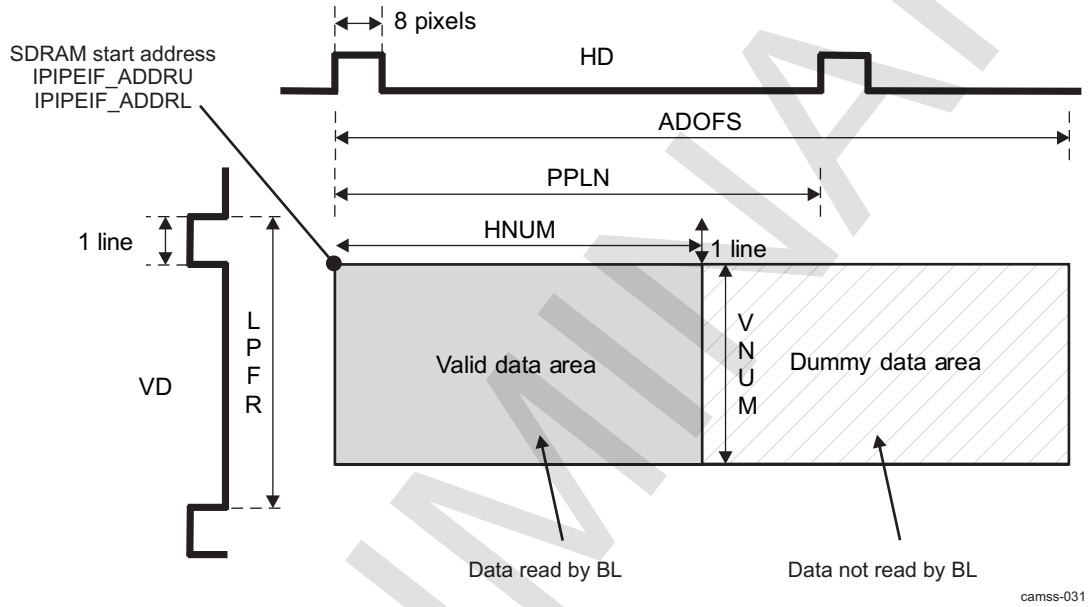
The IPIPEIF_HNUM and IPIPEIF_VNUM registers define the number of pixels per line and lines per frame to read from the SDRAM, and the IPIPEIF_LPFR and IPIPEIF_PPLN registers define the interval of VD and HD, respectively.

Vertical blanking for the frame is defined with the following equation: IPIPEIF_LPFR IPIPEIF_VNUM 1.

Horizontal blanking for the frame is defined with the following equation: IPIPEIF_PPLN IPIPEIF_HNUM.

Figure 8-114 shows the global frame definition for all SDRAM input modes, except for dark frame subtract.

Figure 8-114. ISS ISP IPIPEIF Global Frame Definition in SDRAM Input Modes (Except Dark Frame)



For dark frame data, the HD and VD signals come from the VP through the ISIF. The IPIPEIF_PPLN and IPIPEIF_LPFR registers must be used to indicate the horizontal and vertical start position of the subtraction from the ISIF data, as shown in Figure 8-115. The value of the IPIPEIF_LPFR [12:0] LPFR bit field must be greater than 0 because the first line from the VP or ISIF cannot be subtracted from. The IPIPEIF_HNUM and IPIPEIF_VNUM registers must be used to set the number of valid pixels horizontally and the number of valid lines vertically.

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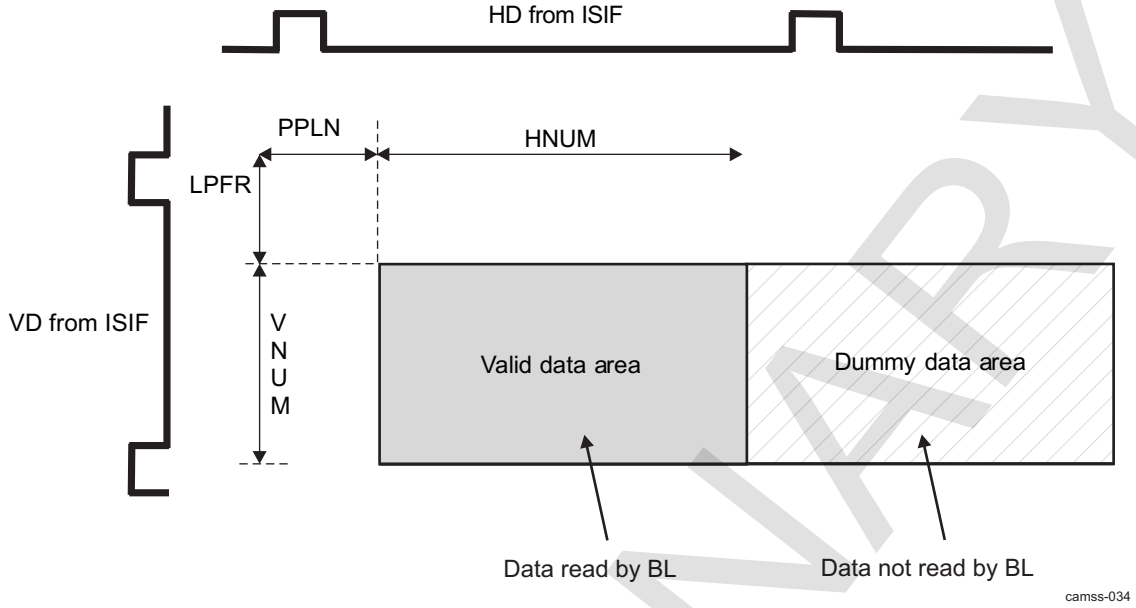
Figure 8-115. ISS ISP IPIPEIF Global Frame Definition in Dark Frame Subtract Mode



8.3.3.3.3.2.1 ISS ISP IPIPEIF Double-Buffer Input Function When Reading From BL

The IPIPEIF module supports a double-buffer input function. This feature is most useful when SDRAM space is limited, because it enables to read continuously from two buffers and to push data to the rest of the ISP (ISIF, H3A, etc.) for further processing.

Consider the following configuration where data are read from two buffers, A and B. The intent is not only to read continuously from these buffers but also to ensure that the ISP modules consider the data as being from the same frame; that is, VD is generated the first time buffer A is read, but it must not toggle until all the frames are read.

The IPIPEIF module can mask the VD sync signal by writing the IPIPEIF_ENABLE[1] SYNCOFF bit but such that the IPIPEIF module drives the data to the ISP modules as if it is a continuous frame data.

In the following example, there are 16 lines per trigger and input circular addressing. VNUM = 16 (see Figure 8-114), and the VD signal is generated only for the first frame (see Figure 8-116).

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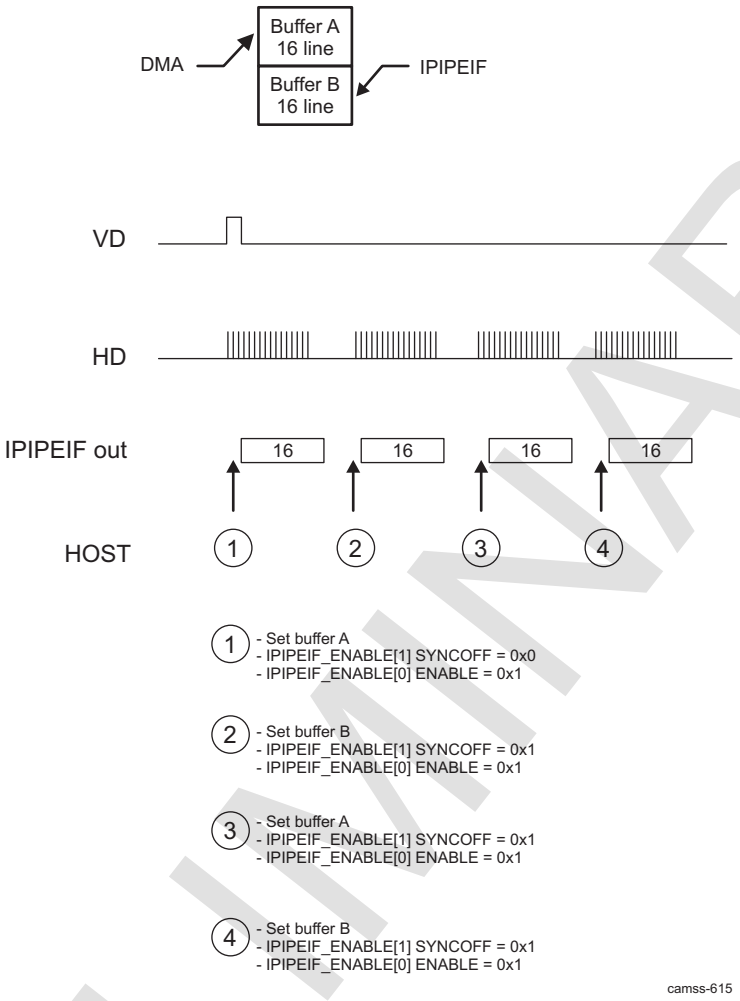
Figure 8-116. ISS ISP IPIPEIF Double-Buffer Functionality



8.3.3.3.4 ISS ISP IPIPEIF Data Path Selection

The data path configuration through the IPIPEIF module is set with the IPIPEIF_CFG1[15:14] INPSRC1 and IPIPEIF_CFG1[3:2] INPSRC2 bit fields. Table 8-314 lists the possible combinations for these two bit fields.

Table 8-314. ISS ISP IPIPEIF IPIPEIF_CFG1[15:14] INPSRC1 and IPIPEIF_CFG1[3:2] INPSRC2 Possible Combinations

IPIPEIF_CFG1[15:14] INPSRC1	IPIPEIF_CFG1[3:2] INPSRC2	Description	Common Use
0	0	This data path is described in Section 8.3.3.3.4.1, *ISS ISP IPIPEIF INPSRC1 = 0 and INPSRC2 = 0* .	Video record, view finder, on-the-fly still image capture applications
0	1	This data path is described in Section 8.3.3.3.4.2, *ISS ISP IPIPEIF INPSRC1 = 0 and INPSRC2 = 1*.	Memory-to IPIPE-to memory
0	2	This data path is described in Section 8.3.3.3.4.3, *ISS ISP IPIPEIF INPSRC1 = 0 and INPSRC2 = 2*.	Image capture with on-the-fly dark frame subtraction

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Table 8-314. ISS ISP IPIPEIF IPIPEIF_CFG1[15:14] INPSRC1 and IPIPEIF_CFG1[3:2] INPSRC2 Possible Combinations (continued)

IPIPEIF_CFG1[15:14] INPSRC1	IPIPEIF_CFG1[3:2] INPSRC2	Description	Common Use
0	3	This data path is described in Section 8.3.3.3.4.4, *ISS ISP IPIPEIF INPSRC1 = 0 and INPSRC2 = 3*.	On-the-fly data acquisition done in VP, forwarded to the ISIF, and then to the H3A through IPIPEIF while data from memory is processed and forwarded to the IPIPE module and then stored in memory YUV4:2:2 or RAW data processing with the IPIPE and RESIZER modules from memory to memory fetched by IPIPEIF
1	0	This data path is described in Section 8.3.3.3.4.5, *ISS ISP IPIPEIF INPSRC1 = 1 and INPSRC2 = 0*.	Memory-to-ISIF- to memory operation
1	1	This data path is possible but there is no use case associated.	N/A
1	2	This data path is not supported.	N/A
1	3	This data path is not supported.	N/A
2	0	This data path is described in Section 8.3.3.3.4.6, *ISS ISP IPIPEIF INPSRC1 = 2 and INPSRC2 = 0*.	Dark frame subtraction is performed and data sent to the ISIF module for further processing, back to IPIPEIF, and then to IPIPE and RSZ.
2	1	This data path is not supported.	N/A
2	2	This data path is not supported.	N/A
2	3	This data path is not supported.	N/A
3	0	This data path is described in Section 8.3.3.3.4.7, *ISS ISP IPIPEIF INPSRC1 = 3 and INPSRC2 = 0*.	Memory-to-ISIF-to memory operation
3	1	This data path is not supported.	N/A
3	2	This data path is not supported.	N/A
3	3	This data path is possible but there is no use case associated.	N/A

8.3.3.3.4.1 ISS ISP IPIPEIF INPSRC1 = 0 and INPSRC2 = 0

Set the IPIPEIF_CFG1[15:14] INPSRC1 bit field to 0 and the IPIPEIF_CFG1[3:2] INPSRC2 bit field to 0.

This configuration can be used for the video record, viewfinder, and on-the-fly still image capture applications. The full ISP processing capability is used in a single pass.

Figure 8-117 shows the data path.

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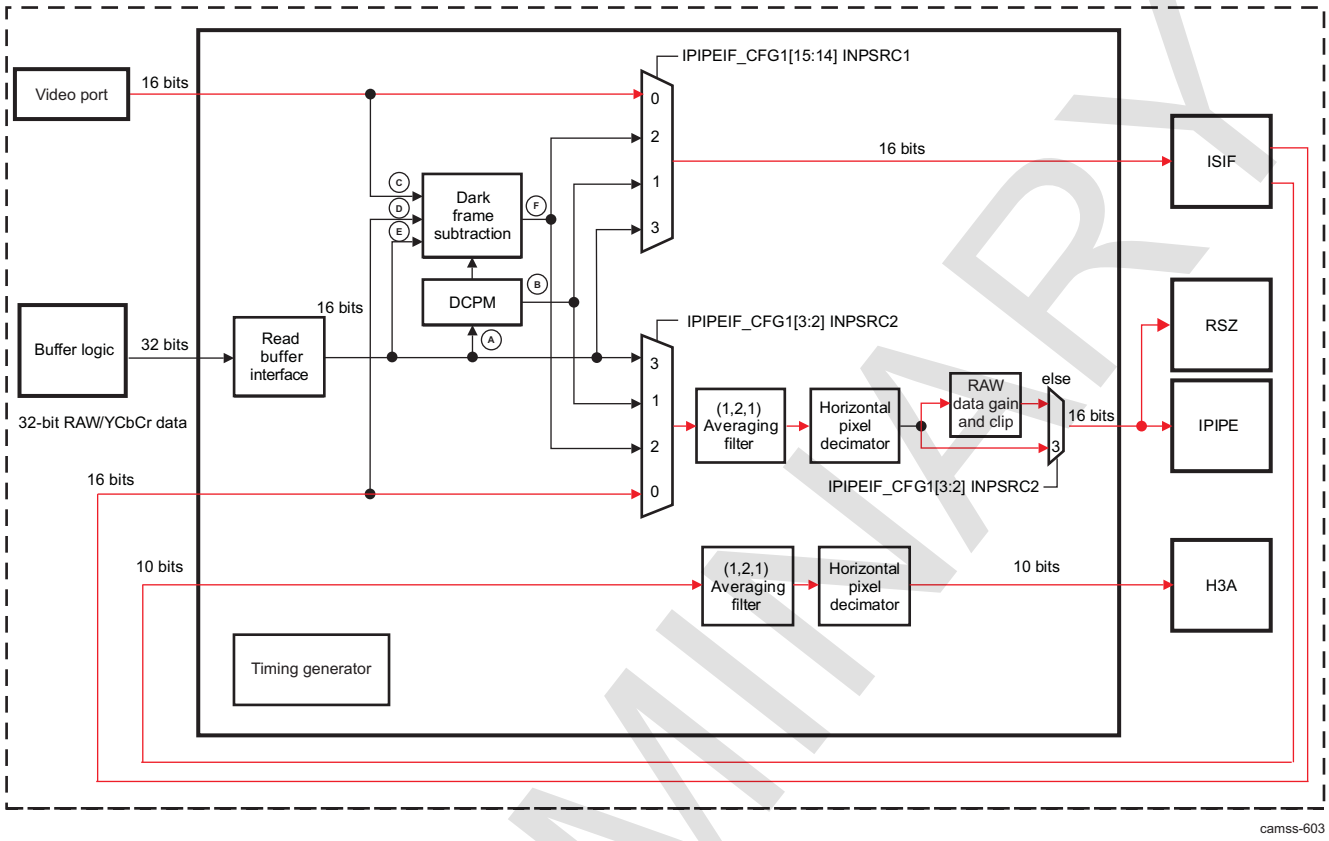
Figure 8-117. ISS ISP IPIPEIF INPSRC1 = 0 and INPSRC2 = 0 Data Path



8.3.3.3.4.2 ISS ISP IPIPEIF INPSRC1 = 0 and INPSRC2 = 1

Set the IPIPEIF_CFG1[15:14] INPSRC1 bit field to 0 and the IPIPEIF_CFG1[3:2] INPSRC2 bit field to 1.

This configuration can be used to process data with the IPIPE module from memory to memory. The data stored in SDRAM can be decompressed (A-law or DPCM) before being forwarded to the IPIPE module.

NOTE: In this configuration, the ISIF and H3A modules are assumed to be disabled.

Figure 8-118 shows the data path.

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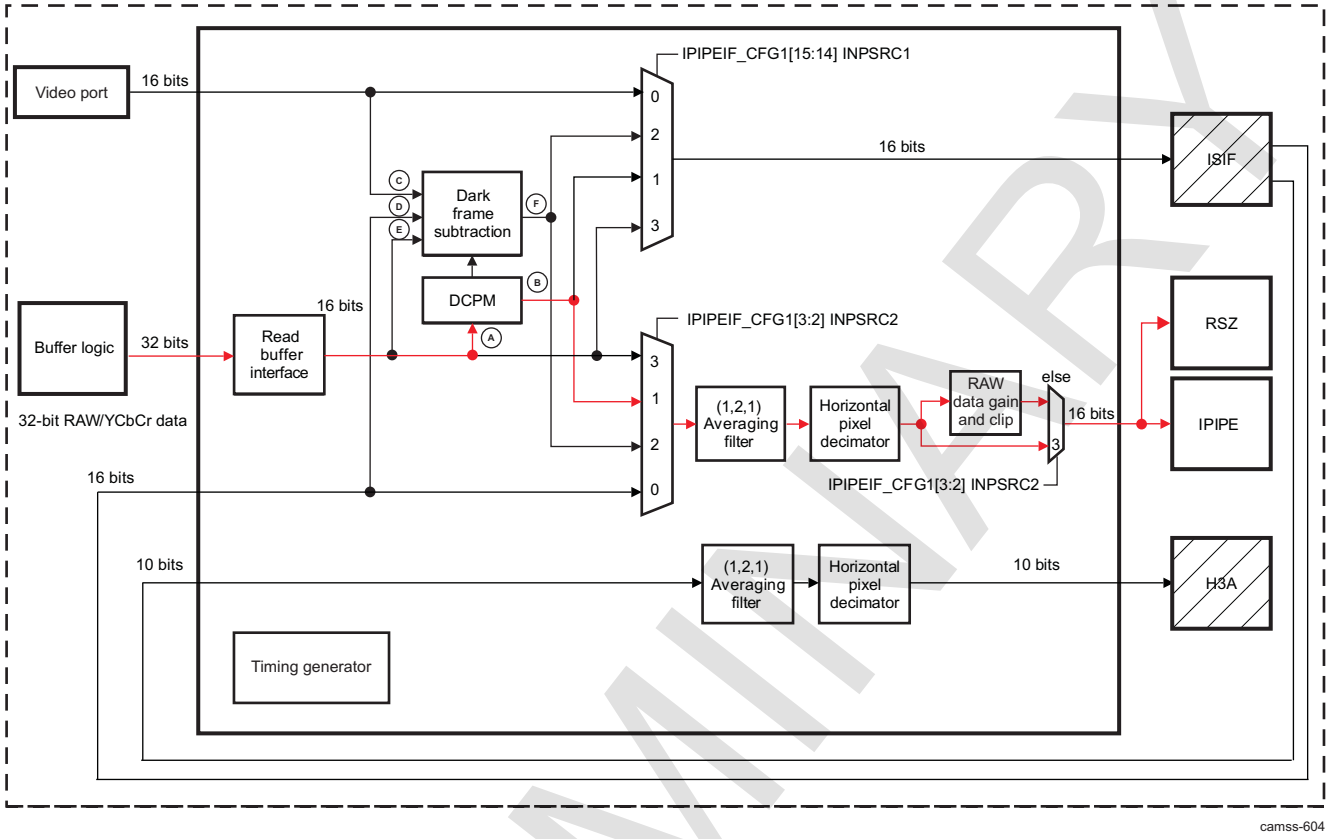
Figure 8-118. ISS ISP IPIPEIF INPSRC1 = 0 and INPSRC2 = 1 Data Path



8.3.3.3.4.3 ISS ISP IPIPEIF INPSRC1 = 0 and INPSRC2 = 2

Set IPIPEIF_CFG1[15:14] INPSRC1 to 0 and IPIPEIF_CFG1[3:2] INPSRC2 to 2.

This configuration can be used for image capture with on-the-fly dark-frame subtraction. In the first case, the dark frame can come from BL and data from the ISIF. In the second case, the dark frame can come from the VP and data from BL.

Figure 8-119 shows the data path.

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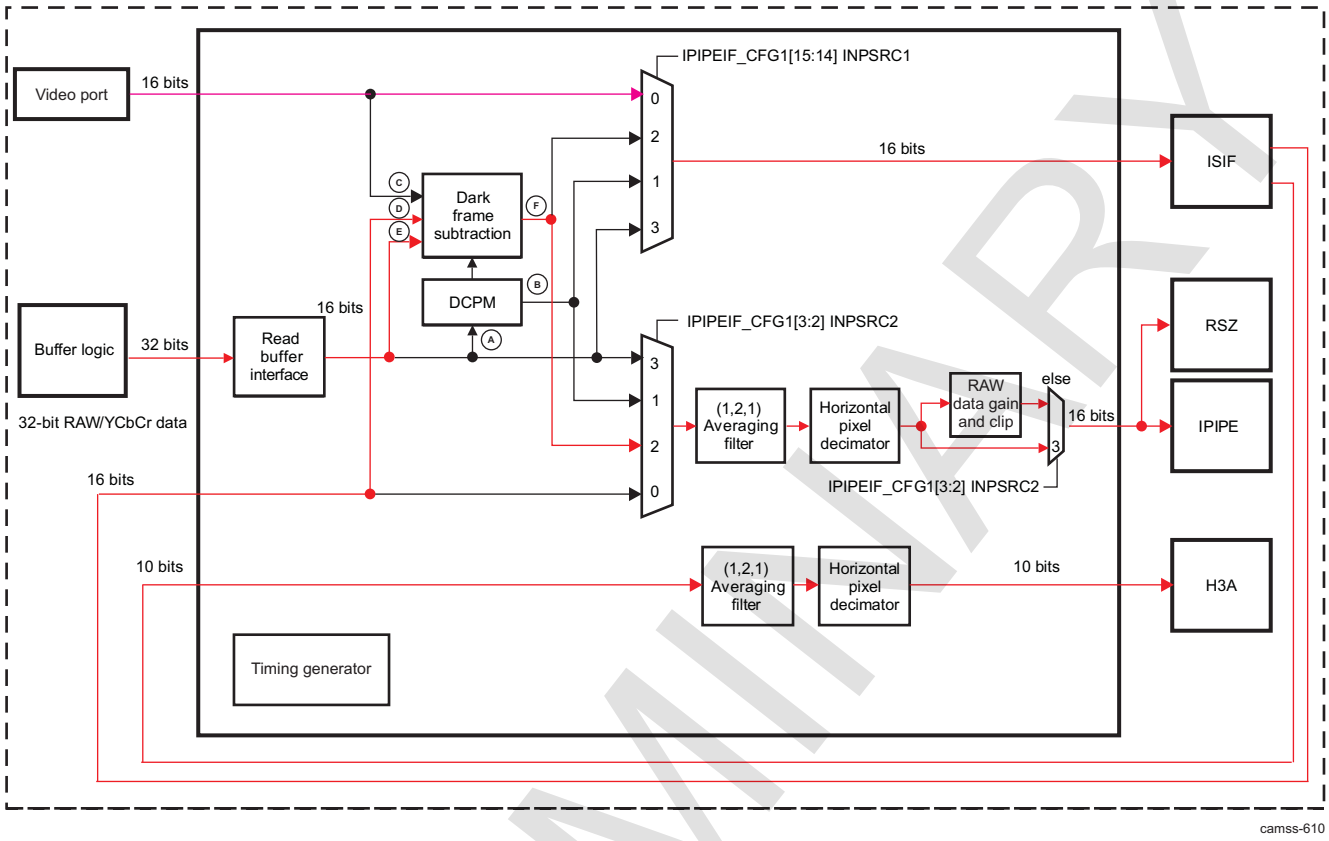
Figure 8-119. ISS ISP IPIPEIF INPSRC1 = 0 and INPSRC2 = 2 Data Paths



8.3.3.3.4.4 ISS ISP IPIPEIF INPSRC1 = 0 and INPSRC2 = 3

Set the IPIPEIF_CFG1[15:14] INPSRC1 bit field to 0 and the IPIPEIF_CFG1[3:2] INPSRC2 bit field to 3.

In the first case, on-the-fly data acquisition is done with the VP, forwarded to the ISIF, and then sent to the H3A through the IPIPEIF while data from memory is processed and forwarded to the IPIPE module and then stored in memory.

In the second case, the configuration can be used to process YUV4:2:2 or RAW data with the IPIPE and RESIZER modules from memory-to-memory. The YUV4:2:2 or RAW data stored in the SDRAM is fetched and forwarded to the IPIPE and RSZ modules. ISIF and H3A are assumed to be disabled in this configuration.

Figure 8-120 and Figure 8-121 show the two possible data paths.

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Figure 8-120. ISS ISP IPIPEIF INPSRC1 = 0 and INPSRC2 = 3 Data Paths: First Case

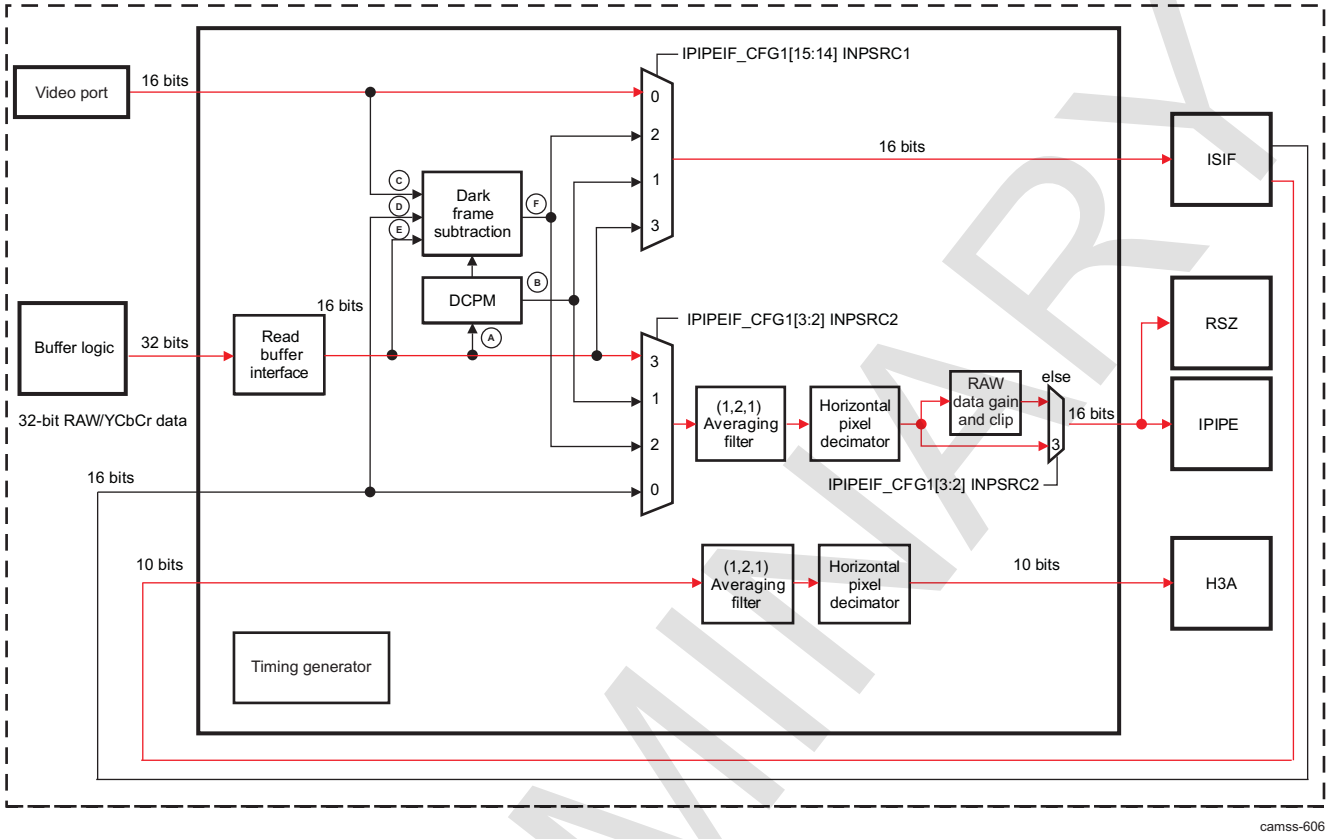

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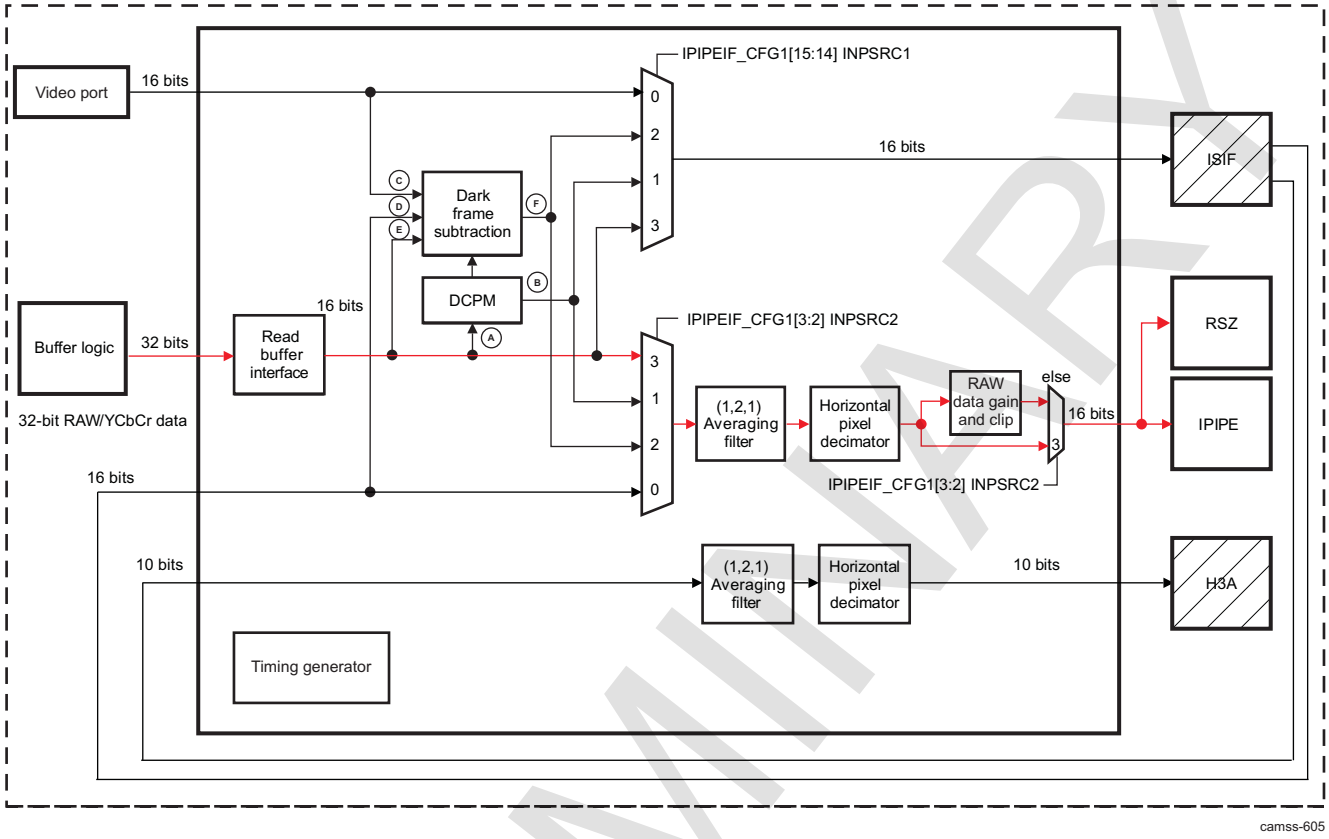
Figure 8-121. ISS ISP IPIPEIF INPSRC1 = 0 and INPSRC2 = 3 Data Paths: Second Case



8.3.3.3.4.5 ISS ISP IPIPEIF INPSRC1 = 1 and INPSRC2 = 0

Set the IPIPEIF_CFG1[15:14] INPSRC1 bit field to 1 and the IPIPEIF_CFG1[3:2] INPSRC2 bit field to 0.

This configuration is a memory-to-memory operation. RAW data is read by the BL interface, decompressed, and pushed to the ISIF. The ISIF processes the data and sends it back to the IPIPEIF module before the data is pushed to the IPIPE and H3A modules.

Figure 8-122 shows the data path.

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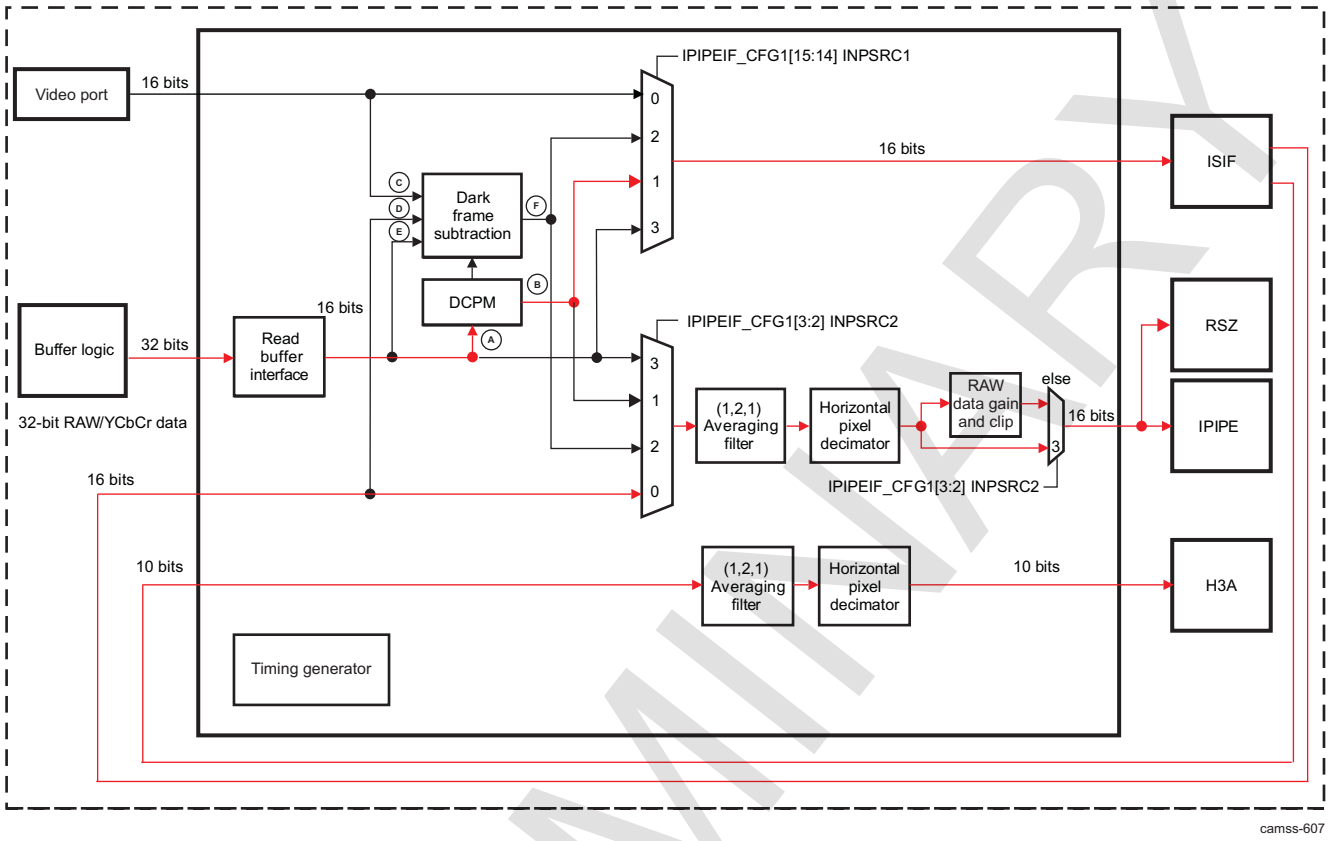
Figure 8-122. ISS ISP IPIPEIF INPSRC1 = 1 and INPSRC2 = 0 Data Path



8.3.3.3.4.6 ISS ISP IPIPEIF INPSRC1 = 2 and INPSRC2 = 0

Set the IPIPEIF_CFG1[15:14] INPSRC1 bit field to 2 and the IPIPEIF_CFG1[3:2] INPSRC2 bit field to 0.

In this configuration, dark frame subtraction is performed and data is sent to the ISIF module. The ISIF processes the data and sends it back to the IPIPEIF module before the data is pushed to the IPIPE or RSZ modules. There are two possible dark frame subtractions: the first is with data coming from the VP and the dark frame coming from BL; the second is with data coming from BL and the dark frame coming from the VP.

Figure 8-123 shows the data path.

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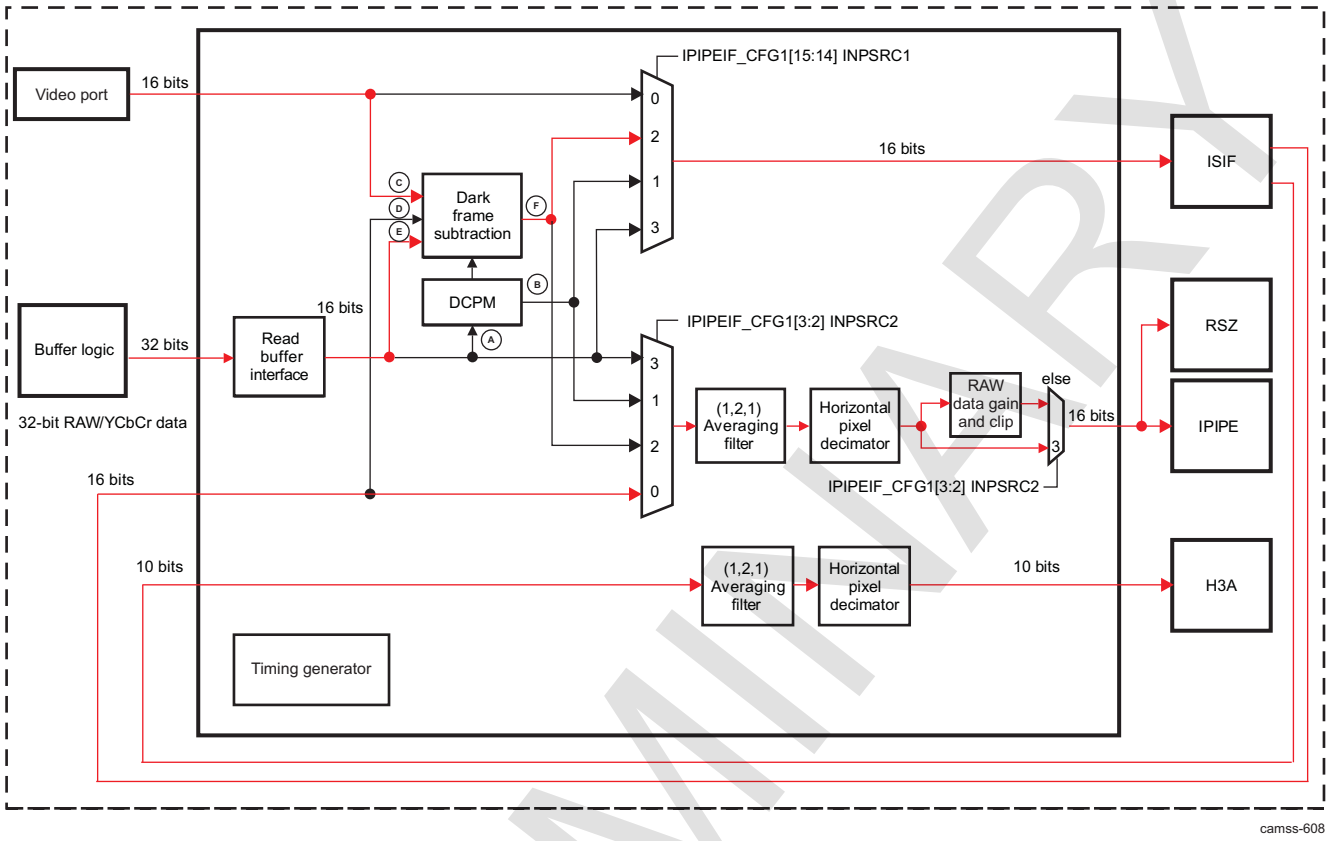
Figure 8-123. ISS ISP IPIPEIF INPSRC1 = 2 and INPSRC2 = 0 Data Path



8.3.3.3.4.7 ISS ISP IPIPEIF INPSRC1 = 3 and INPSRC2 = 0

Set the IPIPEIF_CFG1[15:14] INPSRC1 bit field to 3 and the IPIPEIF_CFG1[3:2] INPSRC2 bit field to 0.

This configuration is a memory-to-memory operation. Data is loaded from the SDRAM. Input data is expected as 16 bpp. The ISIF processes the data and sends it back to the IPIPEIF module before the data is pushed to the IPIPE or RSZ module.

In this configuration data is assumed to be YUV only, and H3A and RAW data gain are assumed to be disabled.

Figure 8-124 shows the data path.

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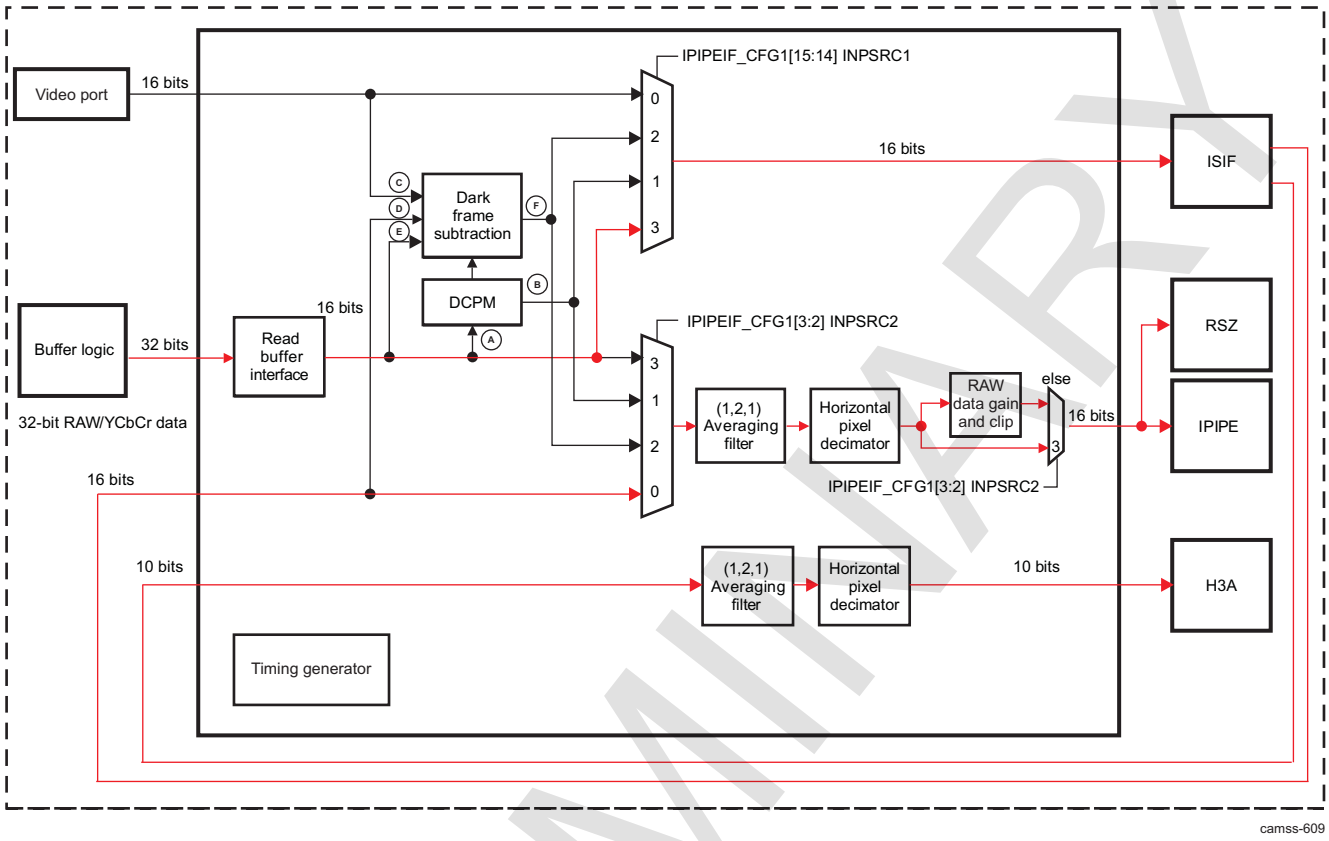
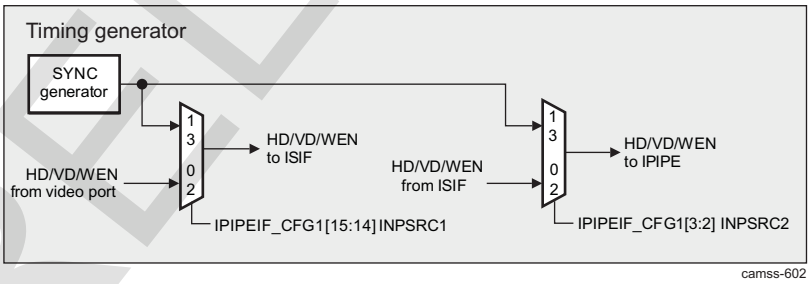
Figure 8-124. ISS ISP IPIPEIF INPSRC1 = 3 and INPSRC2 = 0 Data Path



8.3.3.3.5 ISS ISP IPIPEIF Timing Generation

Figure 8-125 shows the ISS ISP IPIPEIF timing generator submodule.

Figure 8-125. ISS ISP IPIPEIF Timing Generator Submodule



When the IPIPEIF module input source is from the VP (IPIPEIF_CFG1[15:14] INPSRC1 = 0 or 2) or the ISIF (IPIPEIF_CFG1[3:2] INPSRC2 = 0 or 2) , the IPIPEIF_CFG1[10] CLKSEL bit must be set to 0 so that data is latched using the PCLK, HD, and VD signals from the VP.

When the IPIPEIF module input source is not from the VP (IPIPEIF_CFG1[15:14] INPSRC1 = 1 or 3), the IPIPEIF_CFG1[10] CLKSEL bit must be set to 1 so that the IPIPEIF module generates its proper PCLK, HD, and VD signals (through the use of the SYNC generator). The IPIPEIF_CLKDIV register is then used to select a divide ratio of the SDRAM (DMA) clock for the pixel clock frequency, which is used to clock the data into the PCLK. See Section 8.3.3.3.5.1, *ISS ISP IPIPEIF Fractional Clock Divider*.

When the IPIPEIF_CFG1[15:14] INPSRC1 or IPIPEIF_CFG1[3:2] INPSRC2 bit field is not set to 0, the IPIPEIF SDRAM data reading and timing generation can be enabled (IPIPEIF_ENABLE[0] ENABLE) in one-shot mode or continuous mode (IPIPEIF_CFG1[0] ONESHOT).

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8.3.3.3.5.1 ISS ISP IPIPEIF Fractional Clock Divider

When the input data of the IPIPEIF module does not come from the VP but from memory, it is useful to have control of the rate at which the data is fetched from memory to avoid overflow conditions or to avoid peak bandwidth requirements. The IPIPEIF_CFG1[10] CLKSEL bit is equal to 1 for fractional divider use.

The ISP clock ISS_FCLK is divided to generate the pixel clock, which goes to the ISIF and IPIPE modules when data is read from memory (IPIPEIF_CFG1[15:14] INPSRC1 = IPIPEIF_CFG1[3:2] INPSRC2 = 1 or 3). The IPIPEIF_CLKDIV register selects the divider ratio: M and N values in the IPIPEIF_CLKDIV[15:0] CLKDIV bit field.

Given an input clock of clock rate ISS_FCLK, the fractional clock divider generates an output clock with average clock rate f_out.

Where f_out = ISS_FCLK x M/N, and M = 1 through 256, and N = 1 through 256.

The fractional clock divider logic is synchronous and uses only the positive clock edge of the input clock.

8.3.3.3.6 ISS ISP IPIPEIF Decompression (DCPM) Subblock: Unpack and Decompression Function

The IPIPEIF module can read RAW data from memory. The RAW data can be previously packed/compressed into memory. Unpack, A-Law decompression, and DPCM decompression are available in the IPIPEIF module.

Figure 8-126 shows the DCPM subblock.

Figure 8-126. ISS ISP IPIPEIF DCPM Subblock

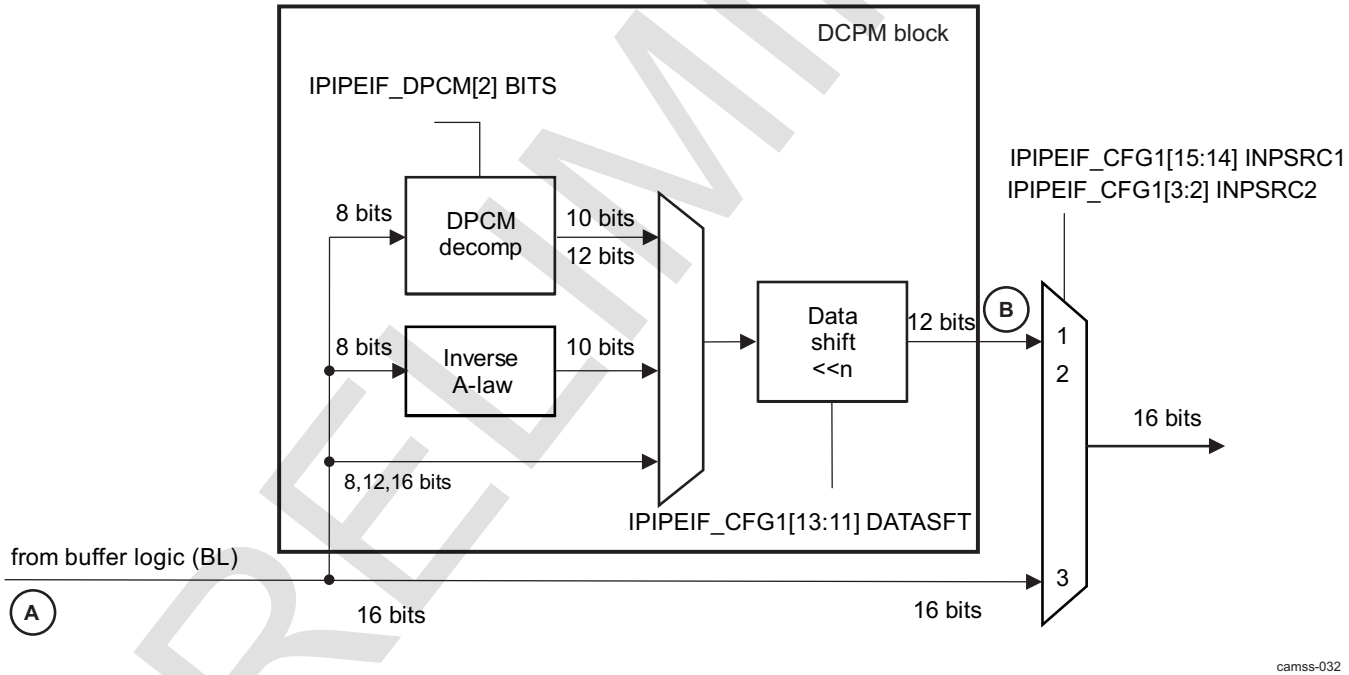

Table 8-315 provides the possible configuration of the DCPM block.

Table 8-315. ISS ISP IPIPEIF DCPM Block Possible Configuration

Number of Bits per Pixel at DCPM Block Input	Number of Bits per Pixel at DCPM Block Output	Description	Registers
16	16	It can correspond to YUV4:2:2 or RAW16 data.	IPIPEIF_CFG1[9:8] UNPACK = 0x0 In this configuration, IPIPEIF_CFG1[3:2] INPSRC2 = 0x3. In this configuration data bypasses the DCPM block.

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Table 8-315. ISS ISP IPIPEIF DCPM Block Possible Configuration (continued)

Number of Bits per Pixel at DCPM Block Input	Number of Bits per Pixel at DCPM Block Output	Description	Registers
8	8	PACK8: YUV	IPIPEIF_CFG1[9:8] UNPACK = 0x1 IPIPEIF_DPCM[0] ENA = 0x0 IPIPEIF_CFG1[13:11] DATASFT = 0x01. In this configuration an 8-bit packed RAW data is used in DFS mode or YUV4:2:0 pass through. (See Section 8.3.3.3.13, *ISS ISP IPIPEIF YUV4:2:2 8-bits Packed Data Input Coming From ISIF Module*.)
8	10	DPCM10: The 8-bit input data are DPCM-decompressed in 10 bits.	IPIPEIF_CFG1[9:8] UNPACK = 0x1 IPIPEIF_DPCM[0] ENA = 0x1 IPIPEIF_DPCM[2] BITS= 0x0 Set the IPIPEIF_DPCM[1] PRED(1) (2) IPIPEIF_CFG1[13:11] DATASFT = 0x2
8	12	DPCM12: The 8-bit input data are DPCM-decompressed in 12 bits.	IPIPEIF_CFG1[9:8] UNPACK = 0x1 IPIPEIF_DPCM[0] ENA = 0x1 IPIPEIF_DPCM[2] = 0x1 Set the IPIPEIF_DPCM[1] PRED(1) (2) IPIPEIF_CFG1[13:11] DATASFT = 0x0
8	10	ALAW10: The 8-bit input data were previously A-law compressed. The 8 bits are A-law decompressed and padded with 0.	IPIPEIF_CFG1[9:8] UNPACK = 0x2 IPIPEIF_CFG1[13:11] DATASFT = 0x2
12	12	PACK12: The input is coded on 12 bits and is packed in the SDRAM. This mode is compatible with the ISIF module packing capability. If inverse A-law and DPCM decompression are not enabled, the data read from the SDRAM can be shifted by the IPIPEIF_CFG1[13:11] DATASFT bit field to select which 12 bits to use. MSB input data bit must be shifted such that it corresponds to bit 11 after the shift.	IPIPEIF_CFG1[9:8] UNPACK = 0x3 Set the IPIPEIF_CFG1[13:11] DATASFT

(1) The simple predictor uses only the value of the previous same color component as a prediction value. Therefore, only 2-pixel memory is required. It is typically used for 10–8–10 or 12–8–12 bit conversions.

(2) The advanced predictor uses four previous pixel values, when the prediction value is evaluated. This means that the values of the other color components are also used, when the prediction value is defined. Therefore, the advanced predictor is slightly better than the simple predictor but consumes more power and memory. It can, however, improve image quality. It is typically used for 10–7–10 and 10–6–10 bit conversions.

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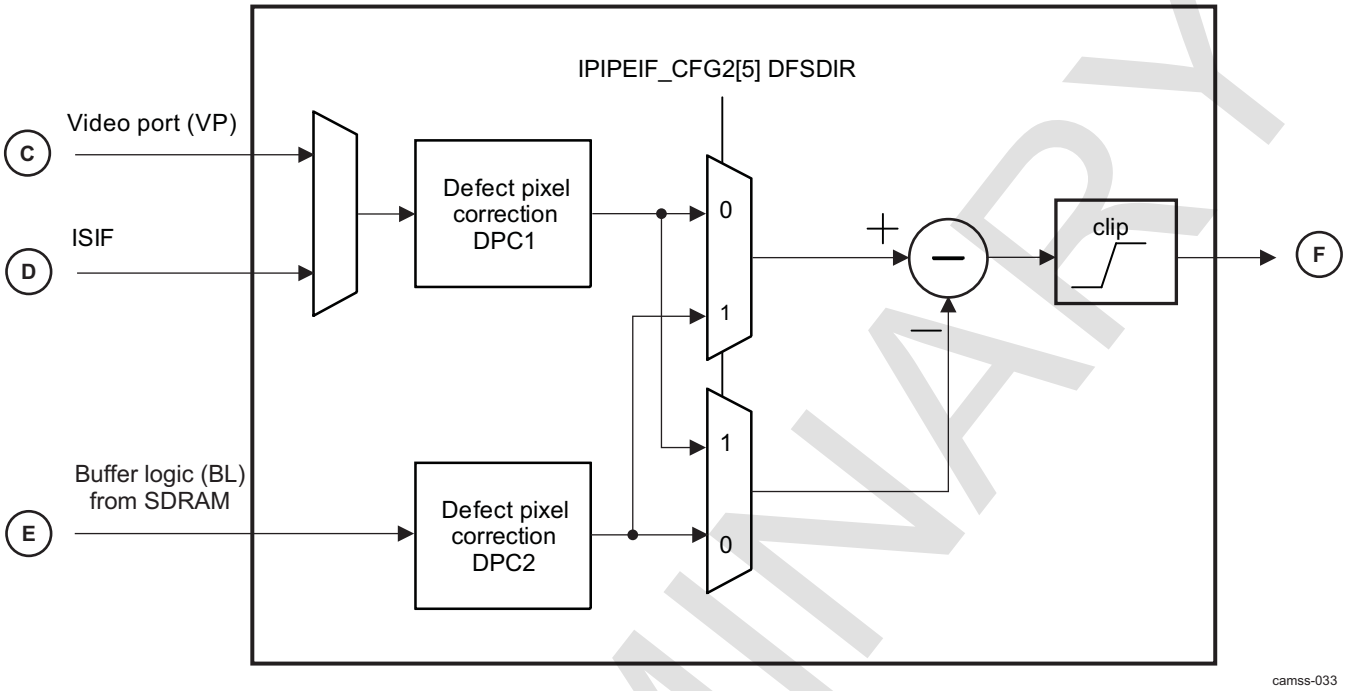
8.3.3.3.7 ISS ISP IPIPEIF Dark-Frame Subtraction Functionality

Figure 8-127. ISS ISP IPIPEIF Dark-Frame Subtraction Subblock



The dark-frame subtract function is used to remove noise from the sensor. Typically, the ISIF module previously writes a dark frame (frame captured when the shutter is closed) to SDRAM using 8 bits of linear data packed into 2 pixels per 16 bits.

In this mode, RAW data from the ISIF and SDRAM is used. Data can also be read from SDRAM with the IPIPEIF_CFG1[9:8] UNPACK bit field set to 1. Each pixel read from SDRAM is subtracted from each pixel sent from the VP or ISIF.

The mux at the input of the dark-frame subtraction subblock is implicitly controlled by the selection of the IPIPEIF_CFG1[15:14] INPSRC1 and IPIPEIF_CFG1[3:2] INPSRC2 bit fields:

- When IPIPEIF_CFG1[15:14] INPSRC1 = 0x2, the selected input ports are VP and BL. Therefore, the dark frame operation can be:
  - Dark frame = VP – BL
  - Dark frame = BL – VP
- When IPIPEIF_CFG1[3:2] INPSRC2 = 0x2, the selected input ports are ISIF and BL. Therefore, the dark frame operation can be:
  - Dark frame = ISIF – BL
  - Dark frame = BL – ISIF

The output of the dark frame subtract operation is 12-bits wide (U12Q0). There must be adequate SDRAM bandwidth if this feature is enabled. If the data fetched from memory arrives late, an underflow bit (IPIPEIF_DTUF) must be triggered to know it .

8.3.3.3.7.1 ISS ISP IPIPEIF Defect Pixel Correction

NOTE: For DPC memory access locations, see Section 8.3.3.9.

A simple DPC can be applied to the ISIF or VP input data path and SDRAM input data path, respectively. This DPC algorithm is intended to correct hot pixels during RAW dark frame acquisition or dark frame readout from SDRAM before dark frame subtraction.

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The following code describes DPC algorithm:

```
If (image(n)  TH) || ((image(2)  TH) (image(n+2) TH)
 image(n) = image(n)
Else if image(2)  TH
 image(n) = image(n+2)
Else if image(n+2)  TH
 image(n) = image(2)
Else
 image(n) = (image(2)+ image(n+2))/2
// Where TH is equal to IPIPEIF_DPC1[11:0] TH for DPC1
// Where TH is equal to IPIPEIF_DPC2[11:0] TH for DPC2
```

The IPIPEIF_DPC1[12] ENA bit enables DPC for the VP/ISIF input path, and the IPIPEIF_DPC2[12] ENA bit enables DPC for the SDRAM input path. The algorithm requires a threshold value that is set by the IPIPEIF_DPC1[11:0] TH or IPIPEIF_DPC2[11:0] TH bit field that is a 12-bit unsigned value.

8.3.3.3.7.2 ISS ISP IPIPEIF DFS Subtraction Direction

The IPIPEIF_CFG2[5] DFSDIR bit selects how the DFS subtraction is performed.

- Set theIPIPEIF_CFG2[5] DFSDIR bit to 0 when the RAW data is coming from the VP/ISIF and the dark frame is stored in SDRAM.
- Set the IPIPEIF_CFG2[5] DFSDIR bit to 1 when the RAW data is coming from SDRAM and the dark frame is coming from the VP/ISIF.

After subtraction, a clip ensures that the value is not negative.

Table 8-316 lists the different modes supported in DFS.

Table 8-316. ISS ISP IPIPEIF DFS Modes Supported

Description	DFDIR Value
Dark frame subtract of 8-bit RAW image stored in SDRAM from image from VP	IPIPEIF_CFG2[5] DFSDIR = 0x0
Dark frame subtract of 8-bit RAW image stored in SDRAM from image from ISIF	IPIPEIF_CFG2[5] DFSDIR = 0x0
Dark frame subtract of 8-bit RAW image from VP from image read from SDRAM through the BL	IPIPEIF_CFG2[5] DFSDIR = 0x1

NOTE: DFS input depends on the INPSRC1 and INPSRC2 settings.

8.3.3.3.8 ISS ISP IPIPEIF (1, 2, 1) Averaging Filter for IPIPE Data Path

The averaging filter acts as an anti-aliasing low-pass filter for the horizontal pixel decimator. Usually, when horizontal pixel decimation is enabled (IPIPEIF_CFG1[1] DECIM), the averaging filter must also be enabled to avoid aliasing artifacts. The averaging filter can be enabled by setting the IPIPEIF_CFG1[7] AVGFILT bit. It operates on every other pixel (same color) in RAW Bayer input or every Y component in YCbCr data in the following equation:

output = (input[i – 1] + 2 * input[i] + input[i + 1]) 2

The averaging filter operates on every other pixel (same color) in RAW Bayer input or YUV data.

If the data is YUV4:2:2, the option to average and decimate is given under the conditions listed in Table 8-317.

Table 8-317. ISS ISP IPIPEIF Averaging Filter Conditions for YUV4:2:2 Data

IPIPEIF_CFG1[3:2] INPSRC2	IPIPEIF_CFG2[3] YUV16	Comments
0	1	YUV4:2:2 data is coming from the ISIF module. Averager and decimation is possible on the data path to the IPIPE module.

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Table 8-317. ISS ISP IPIPEIF Averaging Filter Conditions for YUV4:2:2 Data (continued)

IPIPEIF_CFG1[3:2] INPSRC2	IPIPEIF_CFG2[3] YUV16	Comments
1	1	YUV4:2:2 data is read from SDRAM. Averager and decimation is possible on the data path to the IPIPE module.
3		YUV4:2:2 data is read from SDRAM. Averager and decimation is possible on the data path to the IPIPE module.
Other value	Other value	For YUV4:2:2 data, averager and decimation is not possible on the data path to the IPIPE module.

The averager implements a (1, 2, 1) FIR filter on Luma and Chroma. The following registers have a part in the behavior of the YUV data averaging and decimation:

- IPIPEIF_INIRSZ[12:0] INIRSZ
- IPIPEIF_CFG1[7] AVGFILT
- IPIPEIF_CFG1[1] DECIM

8.3.3.3.9 ISS ISP IPIPEIF Horizontal Pixel Decimator (Downsizer) for IPIPE Data Path

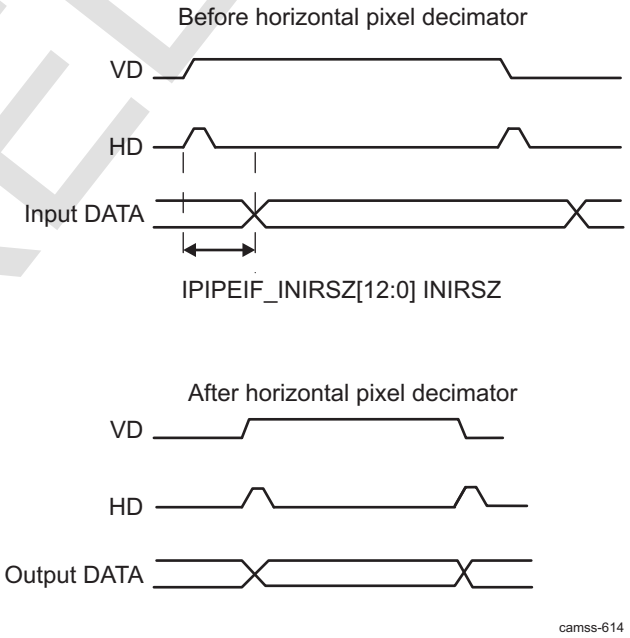
The IPIPE input is limited to 5376 pixels per horizontal line due to restrictions in the line memory width in the IPIPE.

To process image sensor resolutions with more than 5376 pixels per line with no resolution loss, vertical frame division mode (FDM) must be used; that is, the image must be divided into vertical chunks of less than 5376 pixels, and each chunk must be processed sequentially by the ISP. FDM is memory-to-memory processing and is not supported on the fly.

Alternatively, if a loss in resolution is acceptable, the line width decimator (the IPIPEIF_CFG1[1] DECIM bit) can be enabled to downsample the input lines to a width equal to or less than the 5376 pixel maximum. The resize ratio (16/RSZ) can be configured by programming the IPIPEIF_RSZ[6:0] RSZ bit field to be within the range from 16 to 112 to give a resampling range from 1x to 1/7x.

When ALNSYNC is enabled (IPIPEIF_INIRSZ[13] ALNSYNC = 0x1), the IPIPEIF_INIRSZ[12:0] INIRSZ pixels are skipped (from the HD position) before the horizontal pixel decimator, as shown in Figure 8-128.

Figure 8-128. ISS ISP IPIPEIF Resizer Offset Definition



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8.3.3.3.10 ISS ISP IPIPEIF RAW Data Gain for IPIPE Data Path

A gain factor ranging from 0.00195(1/512) to 1.99805(1023/512) is multiplied to the RAW output of the IPIPEIF. The gain is not applied if the input data is YCbCr. The gain constant is set in the IPIPEIF_GAIN[9:0] GAIN bit field using U10Q9 format.

The output value is clipped after gain control through the value of the IPIPEIF_OCLIP[11:0] OCLIP bit field.

8.3.3.3.11 ISS ISP IPIPEIF (1, 2 ,1) Averaging Filter for H3A Data Path

The averaging filter acts as an anti-aliasing low-pass filter for the horizontal pixel decimator. Usually, when horizontal pixel decimation is enabled (the IPIPEIF_RSZ3A[9] DECIM bit), the averaging filter must also be enabled to avoid aliasing artifacts. The averaging filter can also be used to reduce noise before H3A statistics generation. It operates on every other pixel (the same color) in a RAW Bayer input or every Y component in YCbCr data. The averaging filter can be enabled by setting the IPIPEIF_RSZ3A[8] AVGFILT bit, and it operates with the following equation:

output = (input[i – 1] + 2 * input[i] + input[i + 1]) 2

8.3.3.3.12 ISS ISP IPIPEIF Horizontal Pixel Decimator (Downsizer) for H3A Data Path

The H3A input is limited to 3008 pixels per horizontal line due to restrictions in the line memory width in the H3A.

To process image-sensor resolutions with more than 3008 pixels per line with no resolution loss, vertical frame division mode (FDM must be used); that is, the image must be divided into vertical chunks of less than 3008 pixels, and each chunk must be processed sequentially by the ISP. FDM is memory-to-memory processing and is not supported on the fly.

Alternatively, if loss of resolution is acceptable, the line width decimator (the IPIPEIF_RSZ3A[9] DECIM bit) can be enabled to downsample the input lines to a width equal to or less than the 3008 pixel maximum. The resize ratio (16/RSZ) can be configured by programming the IPIPEIF_RSZ3A[6:0] RSZ bit field to be within the range from 16 to 112 to give a resampling range from 1x to 1/7x.

When ALNSYNC is enabled (IPIPEIF_INIRSZ3A[13] ALNSYNC = 0x1), the IPIPEIF_INIRSZ3A[12:0] INIRSZ pixels are skipped (from the HD position) before the horizontal pixel decimator (see Figure 8-128).

8.3.3.3.13 ISS ISP IPIPEIF YUV4:2:2 8-bits Packed Data Input Coming From ISIF Module

This section applies when data coming from the ISIF is 8 bits (IPIPEIF_CFG2[6] YUV8 = 0x1). When IPIPEIF_CFG1[3:2] INPSRC2 = 0 and IPIPEIF_CFG2[3] YUV16 = 1, the 8-bit YUV data are transformed into 16-bit YUV data. The way the data are unpacked from 8 bits to 16 bits is controlled by the IPIPEIF_CFG2[7] YUV8P bit. See Figure 8-129.

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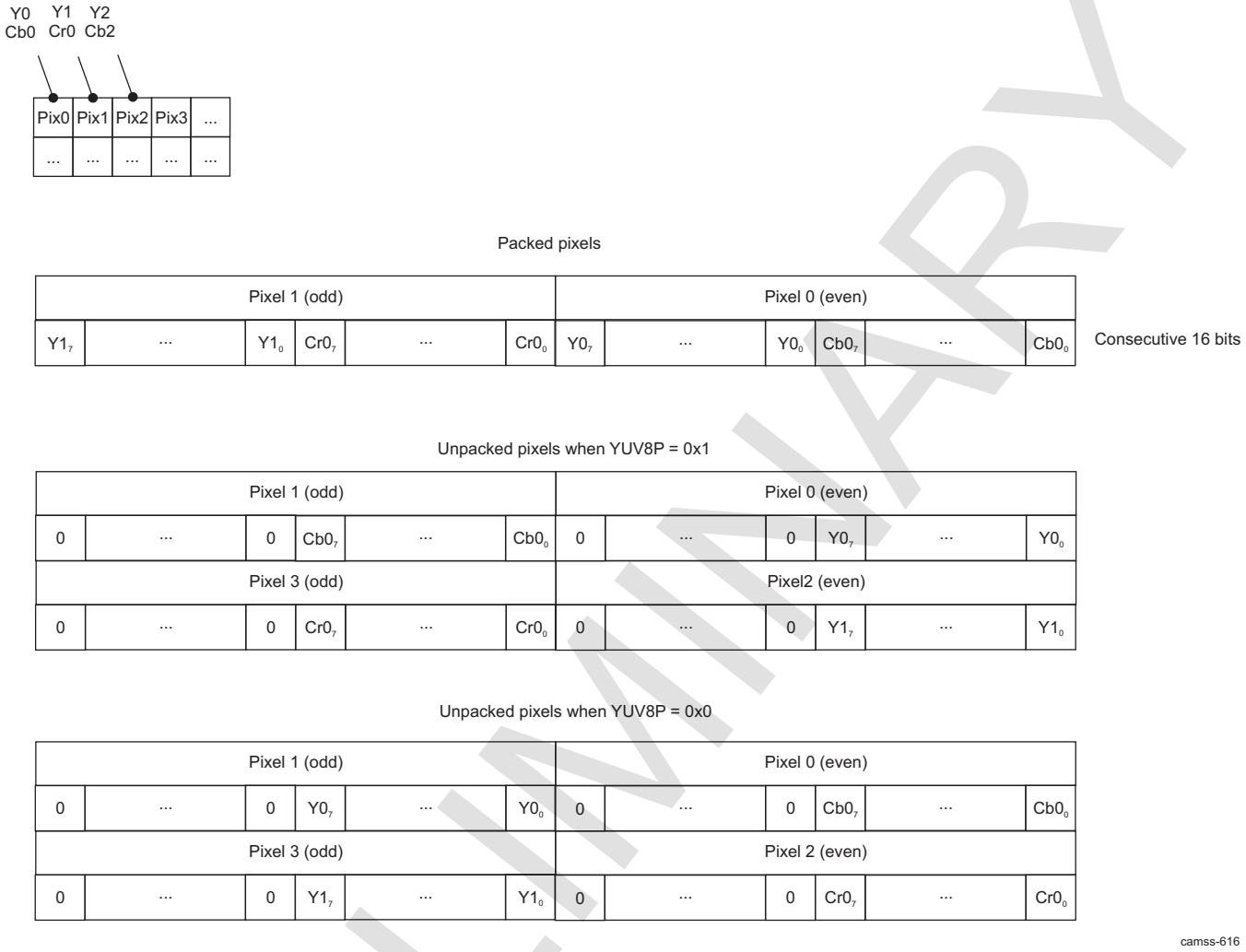
Figure 8-129. ISS ISP IPIPEIF YUV8P Settings



8.3.3.3.14 ISS ISP IPIPEIF YUV4:2:0 Data Input for Memory-to-Memory Resize Operations

The ISP RSZ module can resize YUV4:2:0 data. The YUV4:2:0 data can come from the memory (through BL) or from the VP through the CCP2 RX module, which reads data from SDRAM and pushes it to the IPIPEIF module VP. The possible data paths are:

- SDRAM - IPIPEIF (BL) - RESIZER - SDRAM
- SDRAM - CCP2 RX - IPIPEIF (VP) - RESIZER - SDRAM
- SDRAM - IPIPEIF (BL) - IPIPE - RESIZER - SDRAM
- SDRAM - CCP2 RX - IPIPEIF (BL) - IPIPE - RESIZER - SDRAM

When the data comes from BL, the IPIPEIF module must be set up to process the luminance data first, and then the chrominance data.

- For 420Y (first pass):
  - IPIPEIF_CFG1[15:14] INPSRC1 = 0x1 (SDRAM data input)
  - IPIPEIF_CFG1[3:2] INPSRC2 = 0x1 (SDRAM data input)
  - IPIPEIF_CFG1[13:11] DATASFT = 0x0 (no data shift)
  - IPIPEIF_CFG1[9:8] UNPACK = 0x1 (data packed on 8 bits)
  - IPIPEIF_CFG2[3] YUV16 = 0x1 (data_input [7:0] = 0 and data_input [15:8] = valid)
- For 420C (second pass):

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- IPIPEIF_CFG1[15:14] INPSRC1 = 0x1 (SDRAM data input)
- IPIPEIF_CFG1[3:2] INPSRC2 = 0x1 (SDRAM data input)
- IPIPEIF_CFG1[13:11] DATASFT = 0x0 (no data shift)
- IPIPEIF_CFG1[9:8] UNPACK = 0x1 (data packed on 8 bits)
- IPIPEIF_CFG2[3] YUV16 = 0x0 (data_input[7:0] = valid and data_input [15:8] = 0)

8.3.3.3.15 ISS ISP IPIPEIF Module Events and Status Checking

The IPIPEIF module generates an IPIPEIF event through the IPIPEIF_IRQ interrupt at the end of each frame. This interrupt is set through the ISP5_IRQENABLE_SET_i[9] IPIPEIF_IRQ bit. The input interrupt source generation is selected through the IPIPEIF_CFG2[0] INTSW bit in a certain configuration. The following pseudo code describes INTSW.

```
if (IPIPEIF_CFG2[0] INTSW==0) // Interrupt source from VP
 if (IPIPEIF_CFG1[15:14] INPSRC1==1,2 or 3)
 if (CFG1.ONESHOT==1) // In one shot mode
 Interrupt happens at the end of frame
 else // In continuous mode
 Interrupt is the start position of VD which is generated by IPIPEIF timing generator
 else // IPIPEIF_CFG1[15:14] INPSRC1==0, data is from VP
 Interrupt is the start position of VD from VP
else // Interrupt source from ISIF: IPIPEIF_CFG2[0] INTSW==1
 if (IPIPEIF_CFG1[3:2] INPSRC2==1,2 or 3)
 if (CFG1.ONESHOT==1) // In one shot mode
 Interrupt happens at the end of frame
 else
 Interrupt is the start position of VD which is generated by IPIPEIF timing generator
 else // IPIPEIF_CFG1[3:2] INPSRC2==0, data is from ISIF
 Interrupt is the start position of VD from ISIF
```

In addition to this interrupt, the host must check the IPIPEIF_DTUF status flag of the ISP5_IRQSTATUS_RAW2_i[1] IPIPEIF_UDF bit (if this is enabled and mapped to the ISP IRQ lines) to see if an underflow occurred. For more information, see Section 8.3.4.3.4.

8.3.3.4 ISS ISP IPIPE Functional Description

8.3.3.4.1 ISS ISP IPIPE Overview

- The input interface extracts the valid region from the Bayer RAW data:
  - Up to 12-bit input pixel resolution
  - Requires at least 8 pixels for horizontal blanking and four lines for vertical blanking. In one-shot mode; 16 blanking lines after processing area are required.
  - The maximum horizontal and vertical offset of IPIPE processing area from synchronous signal is 65534.
  - Supports RGB Bayer pattern for input
- The DPC module fixes defect pixels using two methods: LUT-based and on-the-fly adaptive.
- The 2D noise-filter module reduces noise in RAW data.
- The green-imbalance-correction (GIC) module reduces Gb/Gr difference to remove line crawl noise.
- The white balance module applies offset and gain adjustments to each color.
- The Color filter array (CFA) interpolation module implements CFA interpolation. The output from the CFA interpolation module is RGB-4:4:4 formatted data. CFA also reduces aliasing caused by undersampling by digital anti-aliasing (DAA).
- The RGB2RGB blending module applies a 3 × 3 matrix transform to the RGB data generated by the CFA interpolation module.
- The gamma correction module independently applies gamma correction to each RGB component. Gamma is implemented using a piece-wise linear interpolation approach with a 512-entry LUT for each color.

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- The 2nd RGB2RGB blending module applies a 3 × 3 matrix transform to the RGB data after gamma correction.
- 3D-LUT converts RGB data to RGB data using 9 × 9 × 9 table and tetrahedral interpolation.
- The RGB2YCbCr conversion module applies 3 × 3 matrix transformation to the RGB data to convert it to YCbCr data. This module also implements offset. The global brightness and contrast enhancement module fixes brightness and contrast tone.
- The 4:2:2 conversion module applies the chroma low pass filter and downsampling to Cb and Cr to convert 4:4:4 data to 4:2:2 data.
- The 2D edge-enhancer module improves image clarity with a luminance nonlinear filter.
- The chroma artifact reduction module reduces color artifacts using gain control and a 2D median filter.
- The output interface module transfers data from IPIPE to SDRAM in the form of one YCbCr (4:2:2 or 4:2:0), RGB (32/16 bits), or Bayer data.
- The histogram function can record histograms of up to four distinct areas into up to 256 bins.
- The boxcar function makes 1/8 or 1/16 size (1/64 or 1/256 in area) images.
- The boundary signal calculator (BSC) makes vectors of row and column summations.

IPIPE has four different processing paths:

- Case 1: IPIPE reads CCD RAW data and applies all IPIPE functions and stores the YCbCr (or RGB) data to SDRAM.
- Case 2: IPIPE reads CCD RAW data and stores the Bayer data after white balance to SDRAM.
- Case 3: IPIPE reads YCbCr-4:2:2 data and applies edge enhance, chroma suppression, and resize to output YCbCr data to SDRAM.
- Case 4: IPIPE reads YCbCr-4:2:0 data and applies resize to output YCbCr data to SDRAM.

Figure 8-130 shows the connections from the IPIPE module to other submodules of the ISP.

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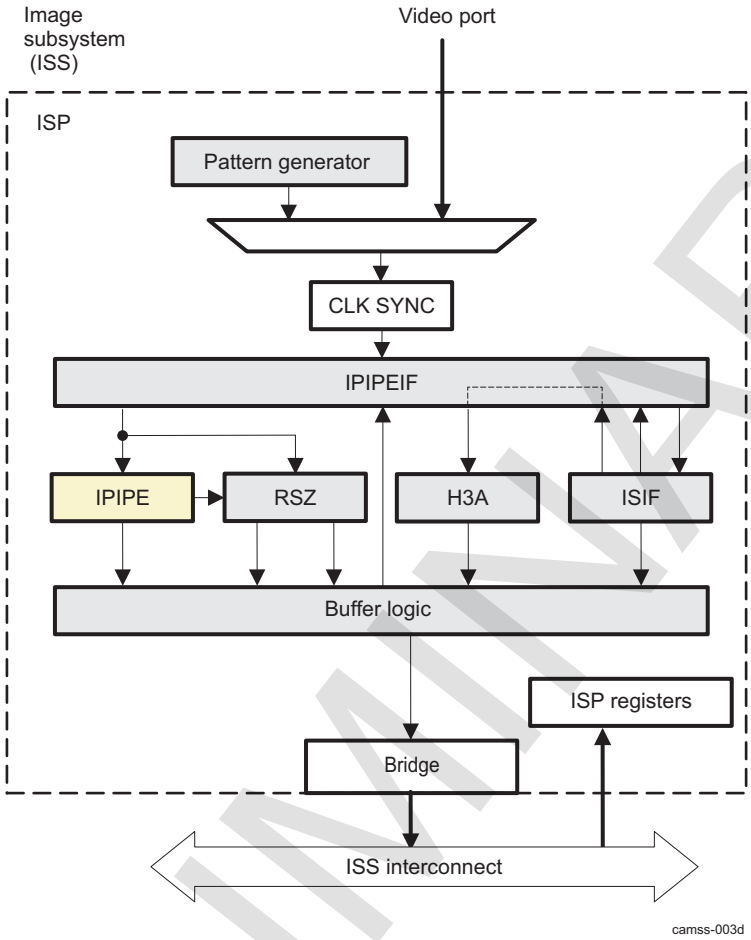
Figure 8-130. ISS ISP IPIPE High-Level Diagram

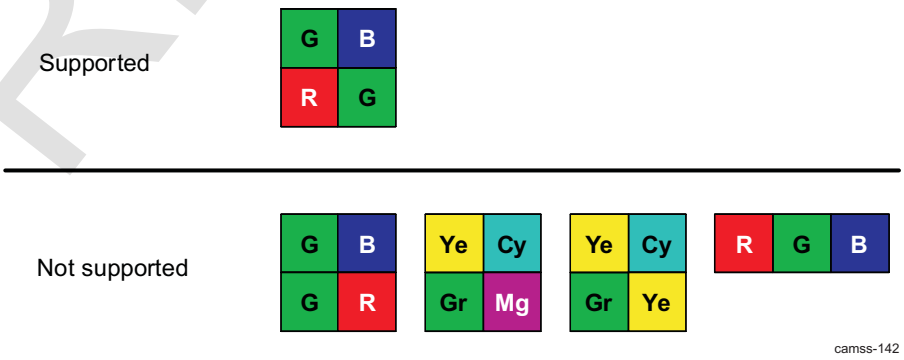


8.3.3.4.2 ISS ISP IPIPE Top-Level Block Diagram

The IPIPE is a programmable hardware image-processing module that generates image data in YCbCr-4:2:2 or YCbCr-4:2:0 format from RAW CCD/CMOS data. The IPIPE module supports output of Bayer data.

The IPIPE module supports RAW data in Bayer format, as shown in Figure 8-131. Other RGB formats or complimentary color formats are not supported.

Figure 8-131. ISS ISP IPIPE Supported CFA Format



As shown in Figure 8-132, many internal modules are used to process Bayer data into YCbCr data

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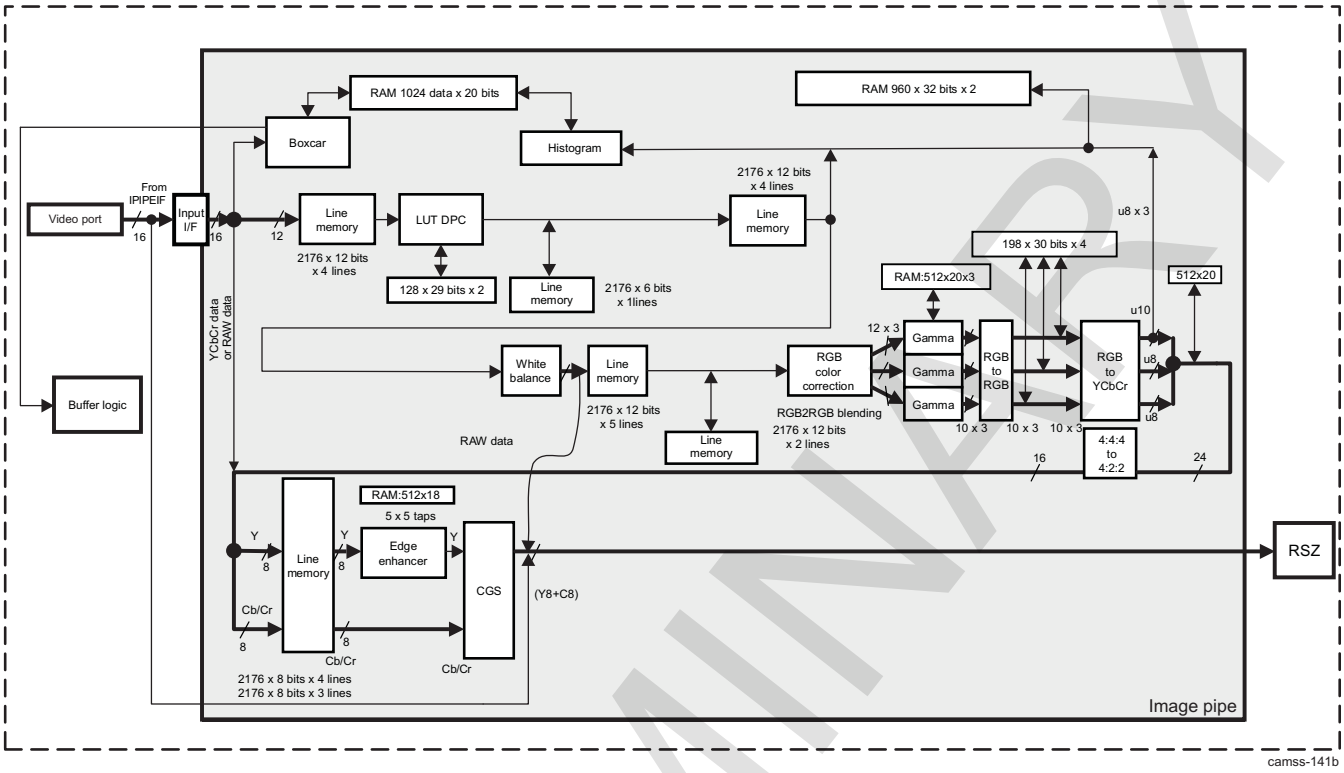
Figure 8-132. ISS ISP IPIPE Module Block Diagram



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8.3.3.4.3 ISS ISP IPIPE Input Interface

The IPIPE module receives 12-bit RAW image data or 16-bit YCbCr data through the IPIPEIF module. The IPIPE module can work with up to 5376 pixels in each horizontal line, except in RAW pass-through mode. If the image width is larger than 5376, the image must be scaled down at the IPIPEIF module level. Otherwise, the input image must be split into several blocks.

If the input data is YCbCr, all RGB processing modules are skipped, and only edge enhancer and chroma suppression are applied to the input data.

If the input data is YCbCr-4:2:0, only Y or C can be processed at a time, and only the resizer process can be applied. Because the resizer is outside the ISIF module, the data is passed to it directly by skipping the RGB and YCbCr processing modules.

In RAW pass-through mode, images up to 8190 pixels per line can be processed. In RAW pass-through mode, the input data is written out directly to SDRAM.

The IPIPE module is enabled through the IPIPE_SRC_EN[0] EN bit.

The IPIPEIF module must be selected as the IPIPE module source with the IPIPE_SRC_MODE[1] WRT bit set to 1 from the input port of the IPIPEIF. This is required to enable and transfer data properly from the interface to the IPIPE.

The IPIPE module has two processing modes, which can be selected through the IPIPE_SRC_MODE[0] OST bit:

- One-shot mode: IPIPE_SRC_MODE[0] OST = 0x1
- Free-run mode: IPIPE_SRC_MODE[0] OST = 0x0

The input and output formats are selected in the IPIPE_SRC_FMT[1:0] FMT bit field (see Table 8-318).

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Table 8-318. ISS ISP IPIPE Input and Output Selections

IPIPE_SRC_FMT[1:0] FMT	IPIPE Module Input	IPIPE Module Output
0x0	RAW Bayer	YCbCr or RGB
0x1	RAW Bayer	RAW Bayer
0x2	RAW Bayer	Disabled
0x3	YCbCr 16 bits	YCbCr

The input to the IPIPE module is in the formats (YCbCr-8bit is not allowed) shown in Figure 8-133.

Figure 8-133. ISS ISP IPIPE Module Input Format

IPIPE input	RAW	LOW	LOW	LOW	LOW	RAW11	RAW10	RAW9	RAW8	RAW7	RAW6	RAW5	RAW4	RAW3	RAW2	RAW1	RAW0
	YCbCr 16b	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	Cb/Cr7	Cb/Cr6	Cb/Cr5	Cb/Cr4	Cb/Cr3	Cb/Cr2	Cb/Cr1	Cb/Cr0
	Y 8bit	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW
	CbCr 8bit	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	Cb/Cr7	Cb/Cr6	Cb/Cr5	Cb/Cr4	Cb/Cr3	Cb/Cr2	Cb/Cr1	Cb/Cr0

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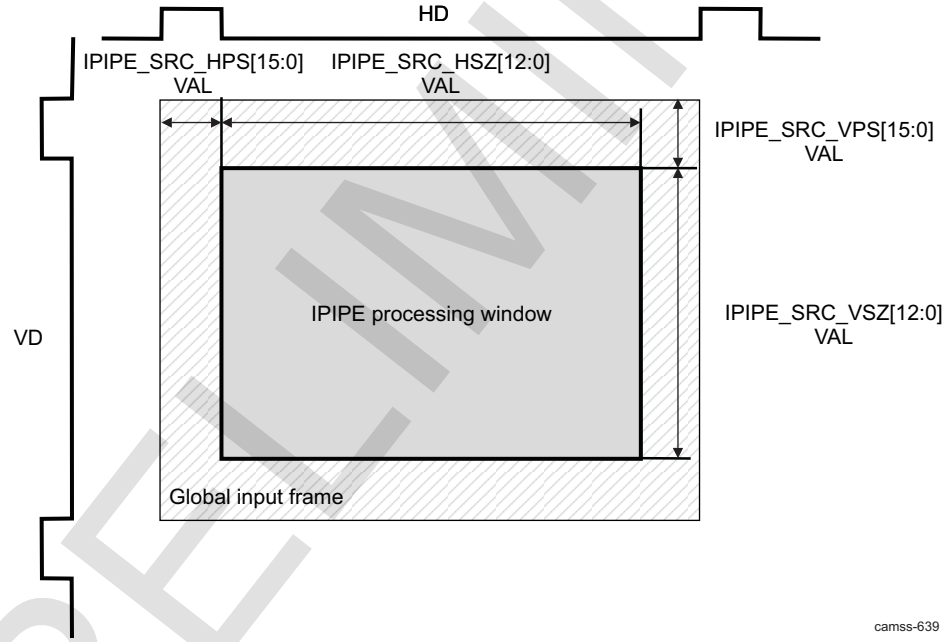
The window to process can be defined by its vertical and horizontal start position (IPIPE_SRC_VPS and IPIPE_SRC_HPS) and vertical and horizontal size (IPIPE_SRC_VSZ and IPIPE_SRC_HSZ). Figure 8-134 shows the window settings for processing.

Figure 8-134. ISS ISP IPIPE Module Processing Window Settings



8.3.3.4.4 ISS ISP IPIPE Defect Pixel Correction

The DPC module corrects defect pixels using two methods: look-up-table-based method (LUT DPC) and on-the-fly adaptive method (OTF DPC). Figure 8-135 shows defect pixel correction.

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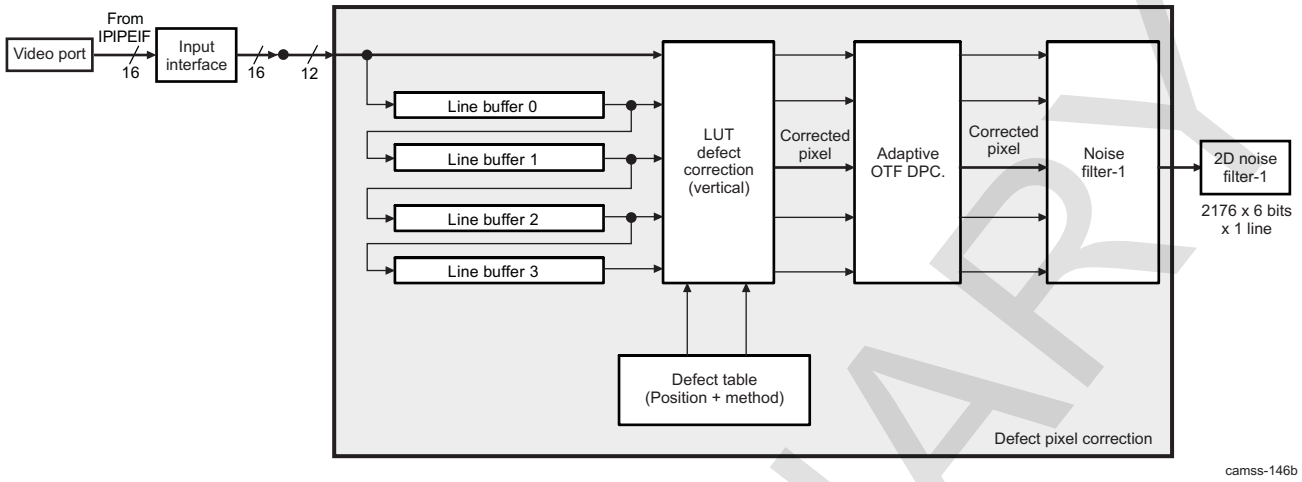
Figure 8-135. ISS ISP IPIPE Defect Pixel Correction



8.3.3.4.4.1 ISS ISP IPIPE LUT Defect Pixel Correction (LUT DPC)

LUT DPC is the first stage of the IPIPE image-processing pipeline. The LUT DPC module corrects defects in input data. It supports up to a 256-defect point table. However, the table can be renewed as required during image processing. Therefore, the maximum amount of defect information is limited only by system-level performance.

The module uses two sets of 128 × 29 memories to hold defect information. The table contains the information of horizontal position (13 bits), vertical position (13 bits), and correction method (3 bits), as shown in Table 8-319. The LUT DPC is enabled through the IPIPE_DPC_LUT_EN[0] EN bit.

Table 8-319. ISS ISP IPIPE Defect Information Packing

Correction Method	Vertical Position	Horizontal Position
28…26	25…13	12…0

The information must be listed in the order of "from left to right" and "from the top to bottom." The first position in the defect information table and the number of defects that are used can be specified. The address of the table must be programmed in the IPIPE_DPC_LUT_ADR[9:0] ADR bit field. Thus, the address of the first valid data is stated.

The LUT type can be:

- With a finite number of entries:
  - IPIPE_DPC_LUT_SEL[1] TBL = 0x0
  - The size of the LUT is set in the IPIPE_DPC_LUT_SIZ[9:0] SIZ bit field.
- With an infinite number of entries:
  - IPIPE_DPC_LUT_SEL[1] TBL = 0x1

The correction methods, set in Table 8-319, are described in Table 8-320.

Table 8-320. ISS ISP IPIPE Correction Method Description

Correction Method	d0 =	Comment
0	Black or white dot	Replace with a black (or white) dot to force OTF-DPC to work on the pixel. White or black dot replacement can be selected through the IPIPE_DPC_LUT_SEL[0] DOT field.
1	d4	Copy from left
2	d5	Copy from right

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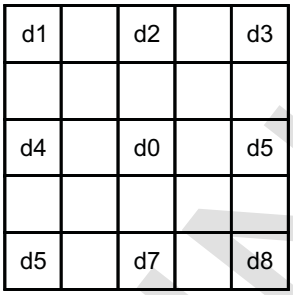
Table 8-320. ISS ISP IPIPE Correction Method Description (continued)

Correction Method	d0 =	Comment
3	(d4 + d5)/2	Horizontal interpolation
4	(d2 + d7)/2	Vertical interpolation
5	d2	Copy from top
6	d7	Copy from bottom
7	(d2 + d4 + d5 + d7)/2	2D interpolation

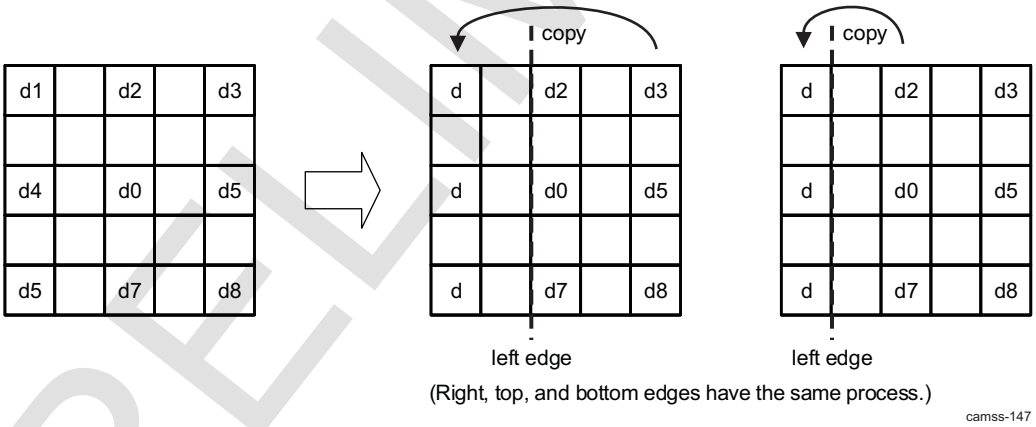
The pixels in the defect correction algorithm are numbered as shown in Figure 8-136.

Figure 8-136. ISS ISP IPIPE Pixel Numbering in Defect Correction Algorithm



The pixels at the edges are mirrored in the way described in Figure 8-137. The figure shows the typical correction by overwriting far-edge pixels and mirroring them with other edge pixels. The example shows how by using a noise filter the correct-by-definition pixels are copied over bad pixels.

Figure 8-137. ISS ISP IPIPE Mirroring in Defect Correction and Noise Filter



8.3.3.4.5 ISS ISP IPIPE White Balance

The white balance module executes white balance to each color component. White balance gain adjusts the ratio of each color existing in a CFA pattern. An offset can be applied before white balance correction (IPIPE_WB2_OFT_R, GR, Gb, or B registers).

Figure 8-138 is a block diagram of the white balance module. In the white balance gain adjuster, the RAW data is multiplied by a selected gain (IPIPE_WB2_WGN_R, Gr, Gb, or B registers) corresponding to the color. The white balance gain can be selected from four 13-bit values. Firmware can assign any combination of 4 pixels in horizontal and vertical directions. The precision of each gain is shown in the figure.

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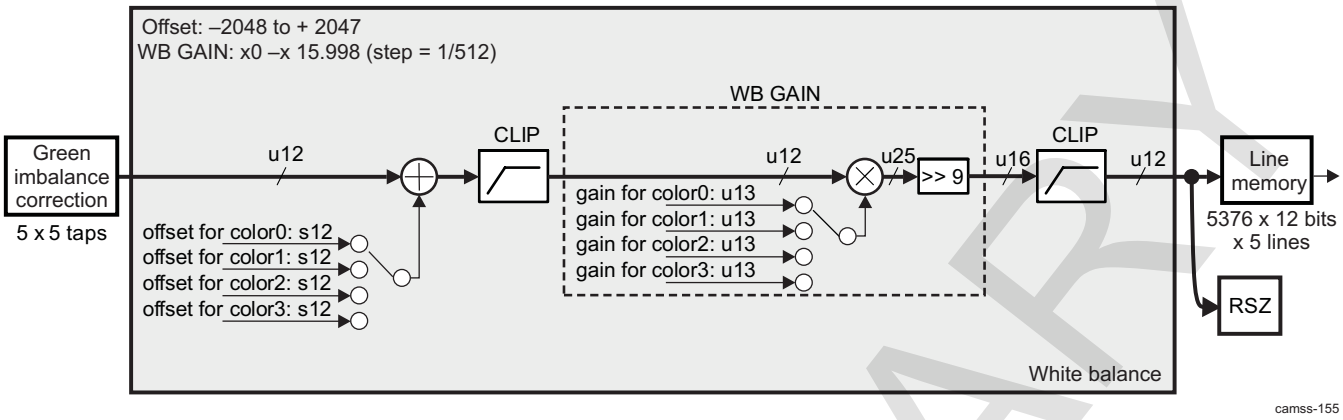
Figure 8-138. ISS ISP IPIPE White Balance



8.3.3.4.6 ISS ISP IPIPE RGB2RGB Blending Module

The RGB2RGB blending module transforms the RGB data generated by the CFA interpolation module using a 3 × 3 square matrix transformation in combination with an added offset. The RGB-to-RGB blending is calculated using the formula shown in Figure 8-139. Each gain range is from –8 to +7.996 with step 1/256 = 0.004, and is set in the IPIPE_RGB1_MUL_RR to IPIPE_RGB1_MUL_BB registers. The offset range for each component is from –4096 to 4095, and is set in the IPIPE_RGB1_OFT_OR to IPIPE_RGB1_OFT_OB registers.

Figure 8-139. ISS ISP IPIPE RGB2RGB Conversion Formula

$$\begin{pmatrix} R_out \\ G_out \\ B_out \end{pmatrix} = \begin{pmatrix} gain_RR & gain_GR & gain_BR \\ gain_RG & gain_GG & gain_BG \\ gain_RB & gain_GB & gain_BB \end{pmatrix} \begin{pmatrix} R_in \\ G_in \\ B_in \end{pmatrix} + \begin{pmatrix} offset_r \\ offset_G \\ offset_B \end{pmatrix}$$

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8.3.3.4.7 ISS ISP IPIPE Gamma Correction Module

NOTE: For the memory access locations of the gamma correction module, see Section 8.3.3.9.

The gamma correction module performs gamma correction independently for each color in the RGB color space by using a piece-wise linear interpolation. ROM tables and RAM tables are selectable through the IPIPE_GMM_CFG[4] TBL bit. Each ROM table and RAM table has 512-entries, and each entry accommodates a 10-bit offset and 10-bit slope. The range of slope value is from –512 to +511. The ROM table has 1024 entries and an output 8-bit value.

Figure 8-140 is a block diagram of the gamma correction module. It is composed of two tables and one selector. When the BYPASS bit is asserted, the input data is divided by 16 (the IPIPE_GMM_CFG[0] BYPR ,IPIPE_GMM_CFG[1] BYPG, and IPIPE_GMM_CFG[2] BYPB bits).

Figure 8-141 shows an example of the gamma curve. Figure 8-142 shows offset and slope packing.

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Figure 8-140. ISS ISP IPIPE Gamma Correction Module Block Diagram

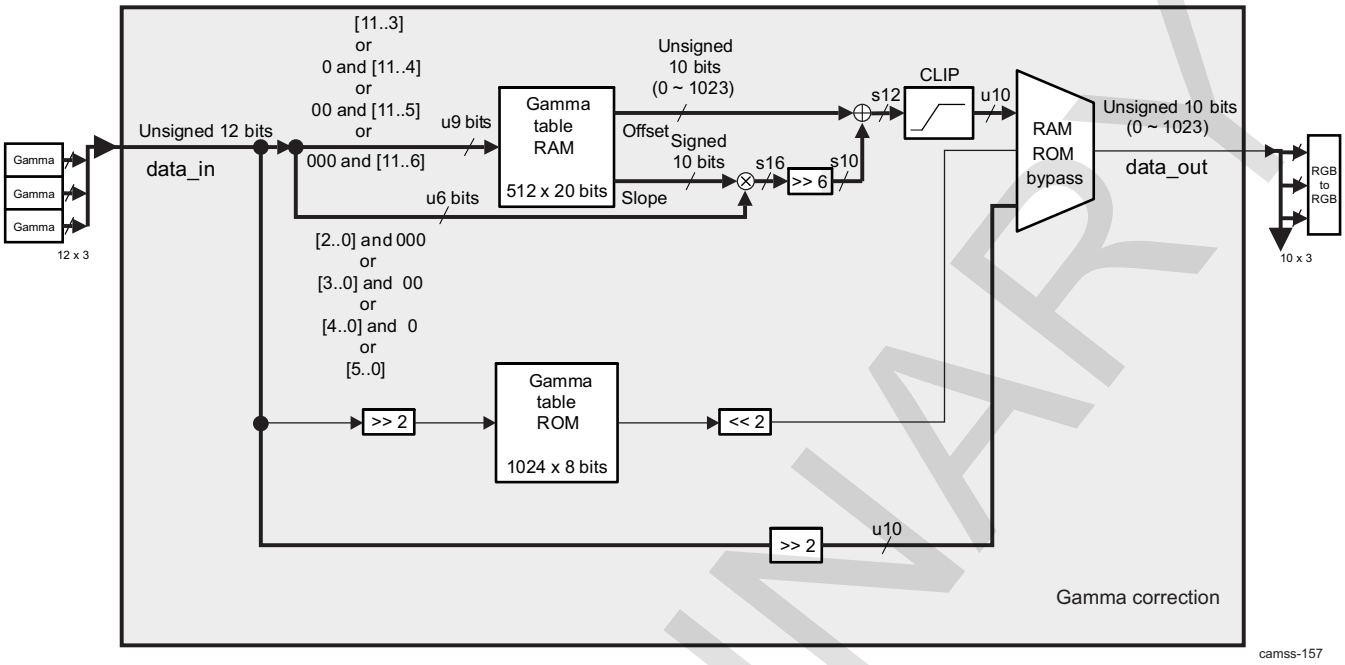


Figure 8-141. ISS ISP IPIPE Gamma Curve Example

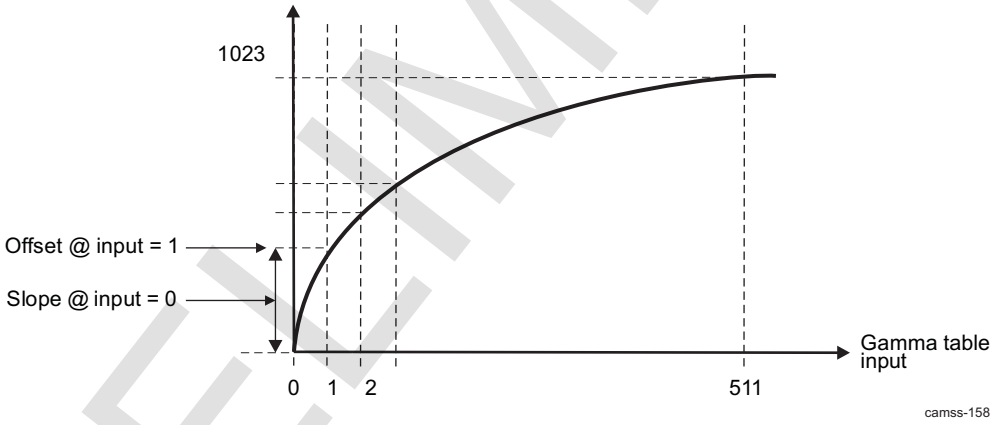
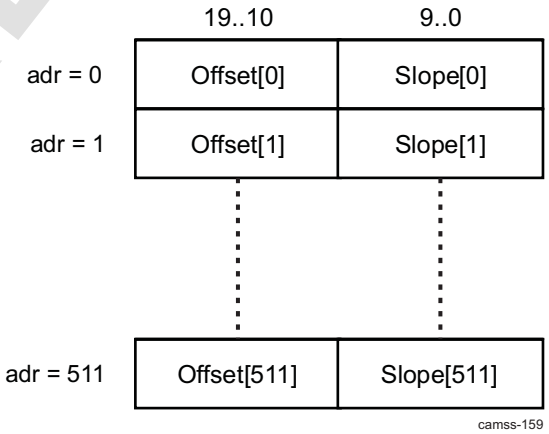


Figure 8-142. ISS ISP IPIPE Gamma Table Offset/Slope Packing



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8.3.3.4.8 ISS ISP IPIPE 2nd RGB2RGB Conversion Matrix

The second RGB2RGB blending module transforms the RGB data after gamma correction using the 3 × 3 square matrix transformation in combination with an added offset. The RGB-to-RGB blending is calculated using the formula shown in Figure 8-143. Each gain range is from –4 to +3.996 with step 1/256 = 0.004 (s3.8), and is set in the IPIPE_RGB2_MUL_RR to IPIPE_RGB2_MUL_BB registers. The offset is –1024 to 1023 (s11), and is set in the IPIPE_RGB2_OFT_OR to IPIPE_RGB2_OFT_OB registers.

Figure 8-143. ISS ISP IPIPE RGB2RGB 2nd Conversion Formula

$$\begin{pmatrix} R_out \\ G_out \\ B_out \end{pmatrix} = \begin{pmatrix} gain_RR & gain_GR & gain_BR \\ gain_RG & gain_GG & gain_BG \\ gain_RB & gain_GB & gain_BB \end{pmatrix} \begin{pmatrix} R_in \\ G_in \\ B_in \end{pmatrix} + \begin{pmatrix} offset_r \\ offset_G \\ offset_B \end{pmatrix}$$

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8.3.3.4.9 ISS ISP IPIPE RGB2YCbCr Conversion Matrix

This module transforms the RGB data to YCbCr data format using a 3 × 3 matrix transformation in combination with an added offset. While transferring, the brightness control and contrast control can be adjusted using the IPIPE_YUV_ADJ[8:15] BRT and IPIPE_YUV_ADJ[8:15] CRT bit fields, respectively. Then, the transform is calculated using the formula shown in Figure 8-144. Each gain range is from –8 to +7.996 with step 1/256 = 0.004, configured in the IPIPE_YUV_MUL_RY to IPIPE_YUV_MUL_BCr registers. The offset is –1024 to 1023 for Y, Cb, and Cr, configured in the IPIPE_YUV_OFT_Y to IPIPE_YUV_OFT_Cr registers. Figure 8-145 is the block diagram of the RGB to RGB blending module. The output is calculated by the equation.

Figure 8-144. ISS ISP IPIPE RGB2RGB 2nd Conversion Formula

$$\begin{pmatrix} Y_out \\ Cb_out \\ Cr_out \end{pmatrix} = \begin{pmatrix} gain_RY & gain_GY & gain_BY \\ gain_RCb & gain_GCb & gain_BCb \\ gain_RCr & gain_GCr & gain_BCr \end{pmatrix} \begin{pmatrix} R_in \\ G_in \\ B_in \end{pmatrix} + \begin{pmatrix} offset_Y \\ offset_Cb \\ offset_Cr \end{pmatrix}$$

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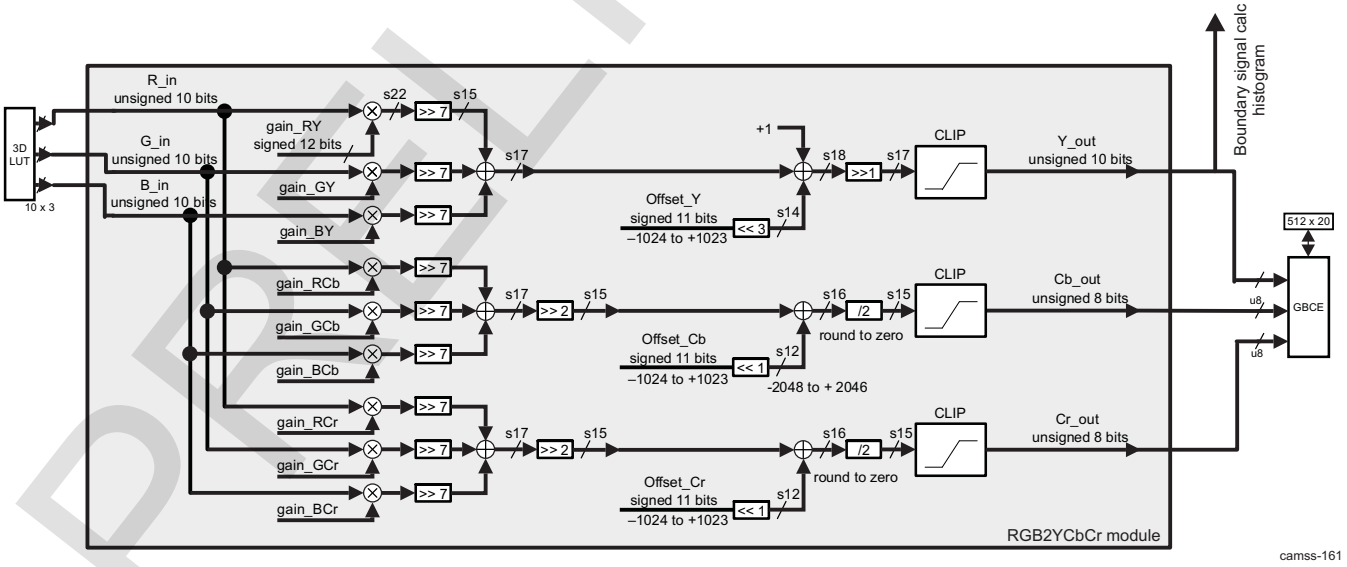
Figure 8-145. ISS ISP IPIPE RGB2YCbCr Module Block Diagram



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8.3.3.4.10 ISS ISP IPIPE 4:2:2 Conversion Module

The 4:2:2 conversion module converts the image data to YCbCr-4:2:2 format by taking the average of every two Cb and Cr components. Y and Cb/Cr sampling point of spatial cosited or spatial centering are selectable using the IPIPE_YUV_PHS[0] POS register. Horizontal 3 taps and 4- or 2-tap filters are used for spatial cosited and spatial centering, respectively. The module is enabled from the IPIPE_YUV_PHS[1] PLF bit.

Figure 8-146. ISS ISP IPIPE Chroma Subsampling Position

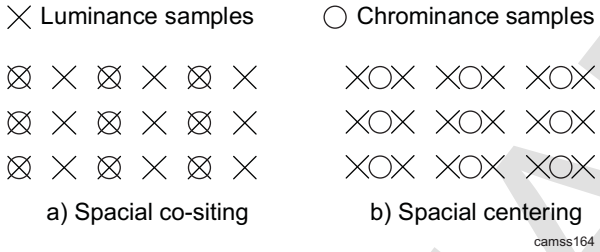
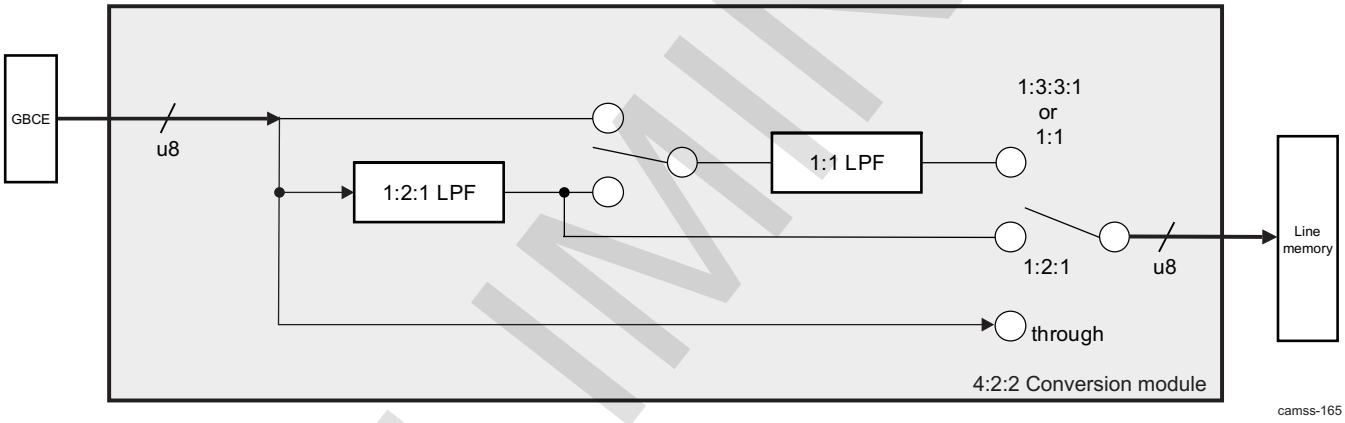


Figure 8-147 is a block diagram of the 4:2:2 conversion module.

Figure 8-147. ISS ISP IPIPE 4:2:2 Conversion Module Block Diagram



8.3.3.4.11 ISS ISP IPIPE 2D Edge Enhancer

NOTE: For the location of 2D edge-enhancer memory accesses, see Section 8.3.3.9.

The edge-enhancer module operates on the luminance (Y data) component of images to improve the image quality and can be enabled from the IPIPE_YEE_EN[0] EN bit. Edges in input images are detected by a 2D high-pass filter, and its sharpness is increased by the value from a non-linear table. Figure 8-148 shows a block diagram of the luminance non-linear edge-enhancer. Entry for the non-linear table is 10-bit and the output is in signed 9-bit.

In edge-enhancer mode when IPIPE_YEE_TYP[0] SEL is set to 0, linear filter with programmable coefficient is applied to the Y input. Here, M is a 5 × 5 matrix with programmable coefficients (IPIPE_YEE_MUL_xx, where x = 00, 01, 02, 10, 11, 12, 20, 21, 22). A down shift of high pass filter is applied to the edge enhancer from the IPIPE_YEE_SHF[3:0] SHF bit field (shgHPF in the formula).

Then, the HPF value is shrunk by a threshold value (u6) specified by the IPIPE_YEE_THR register (thresholdHPF in the formula), and clipped to signed 10 bits to get the index for the LUT.

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Figure 8-148. ISS ISP IPIPE 2D Edge-Enhancer Indexing

$$index = clip\left(shrink\left(HPF, threshold_{HPF}\right), -512, 511\right)$$

$$shrink\left(x, threshold\right) = \begin{cases} x + threshold & x < -threshold \\ 0 & -threshold \le x \le threshold \\ x - threshold & threshold < x \end{cases}$$

$$clip\left(x, limit_{LOW}, limit_{HIGH}\right) = \begin{cases} -limit_{LOW} & x < -limit_{LOW} \\ x & -limit_{LOW} \le x \le limit_{HIGH} \\ limit_{HIGH} & limit_{HIGH} < x \end{cases}$$

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Moreover, the edge-enhancement intensity is looked up from the LUT through the formula shown in Figure 8-149 and in Table 8-321.

Figure 8-149. ISS ISP IPIPE 2D Edge Intensity LUT Formula

$$E_{int} = LUT\left[index\right]$$

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Table 8-321. ISS ISP IPIPE Edge-Enhancer LUT Mapping

Address (32-bit Word Address)	Bit Position	LUT Index
0x00000h	8 .. 0	1
	17 ..9	2
0x00001h	8 .. 0	2
	17 .. 9	3
0x00002h	8 .. 0	4
	17 .. 9	5
0x00003h	8 .. 0	6
	17 .. 9	7
. . .	. . .	. . .
0x000FFh	8 .. 0	510
	17 .. 9	511
0x00100h	8 .. 0	–512
	17 .. 0	–511
0x00101h	8 .. 0	–510
	17 .. 9	–509
. . .	. . .	. . .
0x001FD	8 .. 0	–6
	17 .. 9	–5
0x001FE	8 .. 0	-4
	17 .. 9	-3
0x001FFh	8 .. 0	-2
	17 .. 9	-1

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Figure 8-150 shows the LUT packing, and Figure 8-151 shows the 2D edge-enhancer block diagram.

Figure 8-150. ISS ISP IPIPE 2D Edge-Enhancer LUT Packing

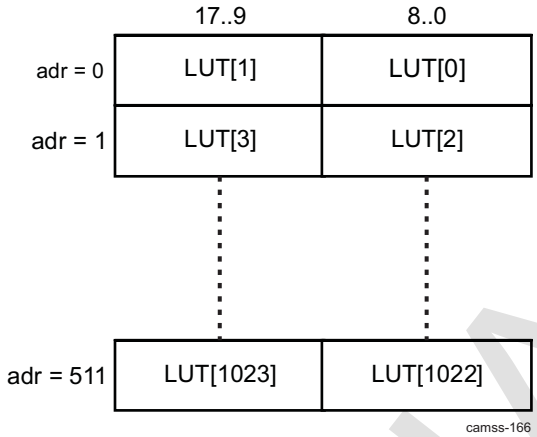
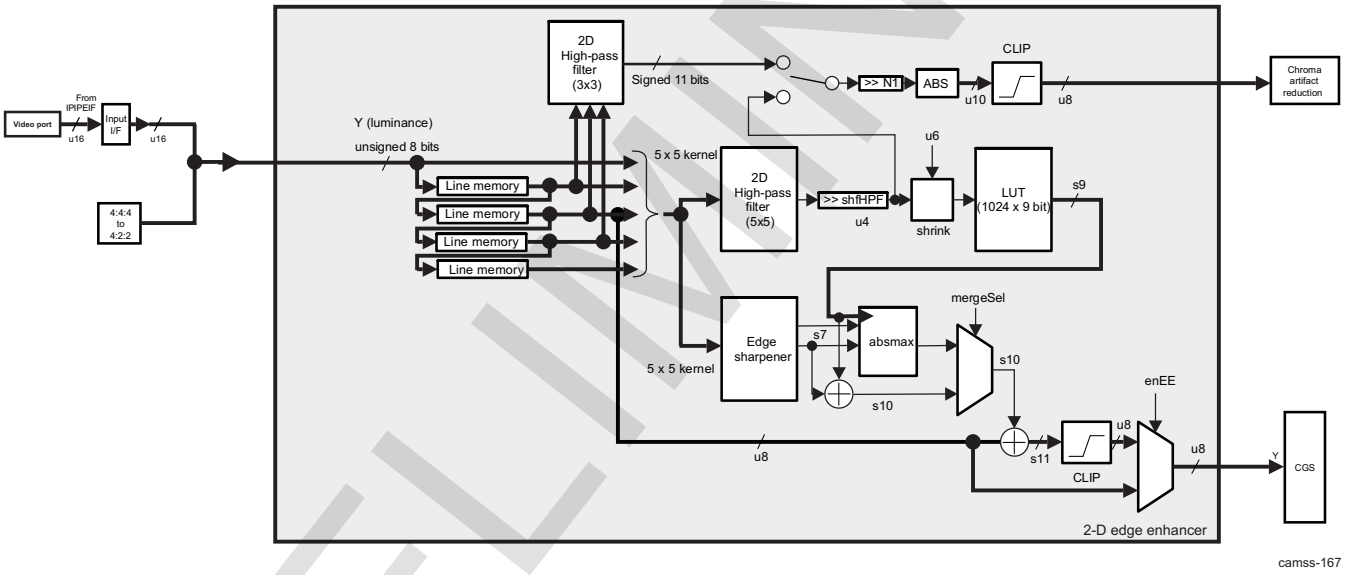


Figure 8-151. ISS ISP IPIPE 2D Edge-Enhancer Block Diagram



In edge sharpener mode, enabled when IPIPE_YEE_TYP[0] SEL = 1, edge clarity is enhanced without producing a Halo artifact. In this module, edge intensity is derived by the 2D linear filter with fixed coefficients shown in Figure 8-152.

Figure 8-152. ISS ISP IPIPE Edge Sharpener Details

$$S_{i,j} = \begin{pmatrix} 0 & -1 & -2 & -1 & 0 \\ -1 & 0 & 2 & 0 & -1 \\ -2 & 2 & 8 & 2 & -2 \\ -1 & 0 & 2 & 0 & -1 \\ 0 & -1 & -2 & -1 & 0 \end{pmatrix}$$

$$sharpness(h,v) = clip\left(shrink\left(g \sum_{j=-2}^{2} \sum_{i=-2}^{2} S_{i,j} Y(h+i, v+j), -threshold_{LOW}, threshold_{LOW} \right) >> 6, threshold_{HIGH} \right)$$

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The gain (g) and threshold values for the shrink/clip function ($threshold_{LOW}$, $threshold_{HIGH}$) are determined by the IPIPE_YEE_E_GAN, IPIPE_YEE_THR_1 and IPIPE_YEE_THR_2 registers. The bit width of g and $threshold_{HIGH}$ is in U6, and $threshold_{LOW}$ is in U12Q6.

This edge intensity is then clipped by a threshold value in the formula shown in Figure 8-153.

Figure 8-153. ISS ISP IPIPE 2D Edge-Intensity Clipping Formula

$$S_{int} = \begin{cases} clip(sharpness, grad) & \text{Halo reduction on} \\ sharpness & \text{Halo reduction off} \end{cases}$$

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The threshold value (grad) is a function of the activity around the target pixel, which is derived from gradient values. Gain and offset are specified by IPIPE_YEE_G_GAN and IPIPE_YEE_G_OFT

Capping with gradient value prevents overly enhancing edges, and suppresses halo artifacts around edges.

The output from edge enhancer and edge sharpener are merged with the function shown in Figure 8-154.

Figure 8-154. ISS ISP IPIPE 2D Edge Enhancer and Sharpener Merger Formula

$$E_{merge} = \begin{cases} E_{int} + S_{int} & mergedsel = 1 \\ absmax(E_{int}, S_{int}) & mergedsel = 0 \end{cases}$$

$$absmax(x, y) = \begin{cases} x & abs(y) \le abs(x) \\ y & otherwise \end{cases}.$$

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The E_{merge} value is added to the Y input value to make the final output.

For chroma suppression, another 2D high pass filter (HPF) is implemented. One of the four coefficient sets shown in Figure 8-155 is selectable.

Figure 8-155. ISS ISP IPIPE 2D Edge Chroma-Suppression Coefficient Sets

$$\begin{pmatrix} 0 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 0 \end{pmatrix}, \begin{pmatrix} 0 & 0 & 0 \\ 1 & -2 & 1 \\ 0 & 0 & 0 \end{pmatrix}, \begin{pmatrix} 0 & 1 & 0 \\ 0 & -2 & 0 \\ 0 & 1 & 0 \end{pmatrix}, \quad or \quad \begin{pmatrix} 0 & 1 & 0 \\ 1 & -4 & 1 \\ 0 & 1 & 0 \end{pmatrix}$$

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At the end of the edge enhancer process, brightness and contrast adjustment are applied to the Y signal. The formula shown in Figure 8-156 describes the process.

Figure 8-156. ISS ISP IPIPE 2D Edge-Brightness and Contrast Adjustments Formula

$$Y_{ctr_brt} = clip8(clip8((Y_{EE} \times CTR) >> 4) + BRT)$$

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8.3.3.4.12 ISS ISP IPIPE Histogram

NOTE: The boxcar function can be used simultaneously with the histogram function if needed.

NOTE: For the locations of histogram memory access, see Section 8.3.3.9.

The histogram module counts the number of pixels that have a value in a region and can be enabled from the IPIPE_HST_EN[0] EN bit. Moreover, if enabled, the IPIPE_HST_MODE register can be set to work constantly or one time. If the IPIPE_HST_MODE[0] OST bit is set to 1, the histogram is disabled by clearing the IPIPE_HST_EN[0] EN bit to 0 after one run (one-shot mode).

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After enabling the module, the following features are available:

- The data to be summed is taken from the DPC memory or RGB2YCbCr module. The choice is made in the IPIPE_HST_SEL[2] SEL bit.
- When data are collected from the DPC memory, the sampled colors are R/G/B/Y. Y is derived in the following method:

Y = (HST_MUL_R*R + HST_MUL_GR*Gr + HST_MUL_GB*Gb + HST_MUL_B*B) (4)

For the G histogram, Gb, Gr, or the average is used, through the IPIPE_HST_SEL[1:0] TYP bit field.

- Two sets of 512 × 20-bit memory are used.
- The number of bins can be set from 32 to 256 in the IPIPE_HST_PARA[13:12] BIN bit field.
- The number of regions (areas) from 1 to 4; each region can be enabled through IPIPE_HST_PARA[x] RGNx (where x = 0 to 3). The positions of the regions are defined in IPIPE_HST_x_VPS and IPIPE_HST_x_HPS, and the vertical and horizontal size are defined by IPIPE_HST_x_VSZ and IPIPE_HST_x_HSZ, respectively (where x = 0 to 3).
- The number of regions × the number of bins = 256.
- Each region can be turned on/off counting.
- The regions have priority orders.
- Each region has its own start coordinate X/Y (12 bits) and horizontal/vertical sizes (12 bits)
- When regions are overlapped, the value in the overlapped region is accumulated only in the region with the highest priority.
- The number of colors to be counted is from 1 to 4. Each color in all regions can be turned off counting (the IPIPE_HST_PARA[7:4] bit field).
- The value of each pixel is down-shifted (0 ~ 11) before counting using the IPIPE_HST_PARA[11:8] SHF bit field.
- When the value of a bin reaches (2^{20} – 1), the value is saturated until the memory is cleared.
- Number of bins: 32, 64, 128, or 256

The histogram memory can be cleared at the VD signal. When the memory is cleared, the first line of each frame cannot be sampled by the histogram if the width of the frame is larger than 512. If the width of the frame is smaller than 512, the first ceil (512/width) lines cannot be collected, where ceil(x) is the smallest integer value above x. If the clearing function is not enabled, the histogram bins are accumulated over the previous values.

The histogram has two banks of memories, which can be switched alternatively. The two memory banks are slipped into four histogram memory tables. Only two tables cam be used at a time: output memory tables 0 and 1, or tables 2 and 3. To initialize tables, the IPIPE_HST_TBL[1] CLR bit is set to 1, and to select which set of tables is to be used the IPIPE_HST_TBL[0] SEL bit can be switched between 0 and 1.

A gain for each color can be applied using the IPIPE_HST_MUL_x registers, where x = R, GR, GB, or B.

8.3.3.4.13 ISS ISP IPIPE Boxcar

The boxcar module generates a boxcar by taking mosaic image data and averaging the red, green, and blue pixels in an (8 × 8) or (16 × 16) block to produce one red, green, and blue output, as shown in Figure 8-157 and in Figure 8-158. Here, similar to the histogram module, the boxcar is enabled from the IPIPE_BOX_EN[0] EN bit, and if the mode is set to run once (one shot) (IPIPE_BOX_MODE[0] OST = 1), the enable bit is cleared after the run. The size of the blocks is determined from the IPIPE_BOX_SHF[0] SEL bit, where if set to 0 = 8 × 8, and 1 = 16 × 16.

The result of this operation is a full-color image with (1/64) or (1/256) area of the original image. The maximum input horizontal width is 8190 pixels when a 16 ×16 block is used; the width is 4096 when an 8 × 8 block is used. Also, the image size (width and height) must be multiple of 16 for a 16 × 16 block, and multiple of 8 for an 8 × 8 block. Boxcar operation works on 12-bit Bayer data and outputs 16-bit data. The output data is 48-bit RGB data for each 8 × 8 or 16 × 16 block. The 48-bit data is aligned in 64-bit format

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in SDRAM as shown in Section 8.3.3.4.13. The first address of SDRAM access is specified by the IPIPE_BOX_SDR_SAD_H and IPIPE_BOX_SDR_SAD_L registers. The output data are written to SDRAM continuously line by line; there is no address offset between lines. After the image transfer of each frame completes, the ipipe_eof signal is sent to buffer logic. This signal is issued at the same timing as ipipe_int_dma.

Figure 8-157. ISS ISP IPIPE Boxcar Operation (8 × 8 Block)

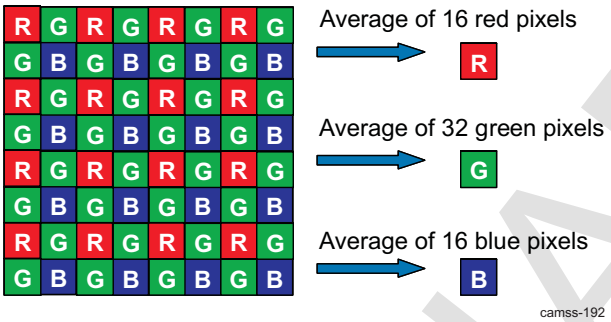


Figure 8-158. ISS ISP IPIPE Boxcar Operation (16 × 16 Block)

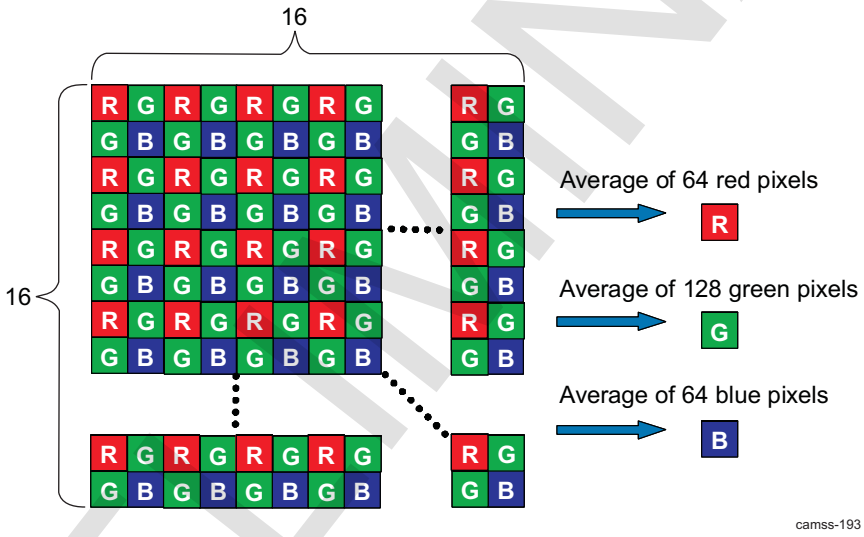
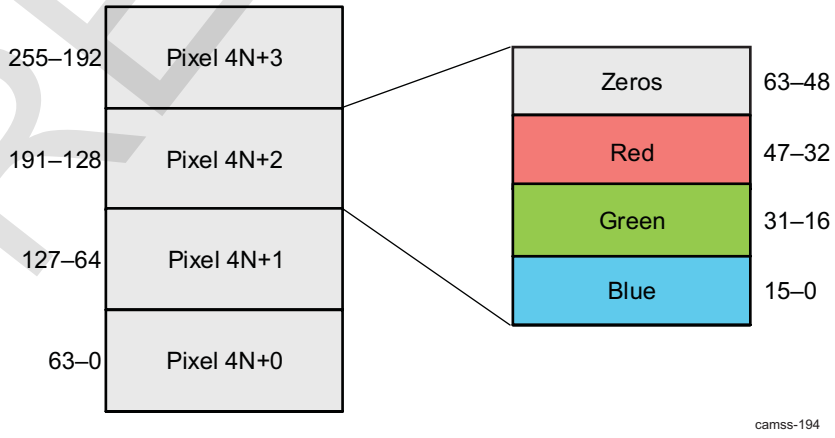


Figure 8-159. ISS ISP IPIPE Boxcar Data Packing in SDRAM



The right shift value is specified by the IPIPE_BOX_SHF register, which has a range of 0 to 4. (The shift down is performed to fit the 20-bit accumulated value into 16-bit output.) For green signal processing, a divide-by-two operation rounds off the least-significant bit (LSB).

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8.3.3.5 ISS ISP RSZ Functional Description

8.3.3.5.1 ISS ISP RSZ Overview

The RSZ module rescales images into various sizes ranging from x1/4096 scale-down to x16 scale-up. It also works in conjunction with the rotational engine (ROT) in SIMCOP for rotating images. The RSZ data slave interfaces support a parallel video port (VP). The RSZ module can produce two output images simultaneously, because there are two independent resizer engines. The input data used by the two resizer engines is the same.

The RSZ module has the following capabilities:

- Input/output data formats:
  - Common input data for the two resizers
  - Independent output data formats for the two resizers
  - Supports YUV4:2:2 input and then supports YUV4:2:2/YUV4:2:0 or RGB5:6:5/ARGB32 output.
    - Output rates up to 200 MPix/s for YUV4:2:2/YUV4:2:0 or RGB5:6:5 output
    - Output rates up to 160 MPix/s for ARGB32 output
  - Supports YUV4:2:0 input data and then supports only YUV4:2:0
    - YUV4:2:0 input format not supported natively
      - Two passes required: luma followed by chroma or vice versa
        - Input and output rates up to 100 MPix/s in this configuration (YUV4:2:0)
      - Only supported from memory to memory
  - Supports RAW Bayer input and RAW Bayer output
    - RAW format invariant. Takes whichever RAW format at the input and writes it out unmodified: 16 bits are read, 16 bits are written out.
    - No resizing can take place on RAW data.
- Resizer capabilities:
  - Input image cropping
    - Common for the two resizer engines: Same input data before and after cropping
    - Supported on YUV4:2:2 and RAW data formats
    - Supported on pass-through mode data path
    - Supported on bypass mode data path
  - Dual resizer engines: RSZ-A and RSZ-B
    - Up to x20 upsampling and x1/4096 downsampling on both engines
    - Up to 200-MHz pixel throughput on both resizer engines
    - Programmable data rate control to smooth the peak memory bandwidth
  - RSZ-A
    - Horizontal resolution of up to 8K pixels on RSZ-A.
  - RSZ-B
    - Horizontal resolution of up to 8K pixels on resizer RSZ-B
  - Independent Y and Cb/Cr phases on horizontal and vertical axis
    - Enables to take care of different YUV4:2:0 phases used in different video formats
    - Enables frame division mode: Images can be stitched together with the right phase.
  - Rescaling: two modes supported
    - Normal mode for upscale and downscale: Higher flexibility but lower downscale quality
    - Downscale mode for downscale only: Lower flexibility but higher downscale quality
  - Filtering: two modes supported
    - Independent settings for the horizontal and vertical directions
    - 3-tap low pass filter with 2-tap linear interpolation

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    - 4-tap cubic interpolation
  - Flip support of the output image
    - Horizontal flip
    - Vertical flip
  - Pixel duplication on the top/bottom, left/right sides
    - Avoids losing pixels at the image boundaries because of the filtering
  - Support pass-through and bypass modes: Resizer engines bypassed
    - Pass-through mode
      - RAW and YUV4:2:2 data support
      - Lower power consumption mode to transfer data to memory
      - Can transfer images larger than 8K pixels to memory
    - Bypass mode
    - RAW and YUV4:2:2 data support
    - Input buffer used. Can benefit from additional buffering in case the BL module memory is not big enough and back pressure occurs.
- Slave data interface: VP interface
  - Two VP interfaces: The programming model selects which VP is used to input data to the RSZ module. Both VPs cannot be active simultaneously.
    - VP 1: Typically connected to the IPIPE module.
    - VP 2: Typically connected to the IPIPEIF module.
  - Up to 200-MHz pixel clock
- Master data interface:
  - Two interfaces to the BL module
    - Up to 200 MHz
    - 32-bit wide, 32-byte long requests
    - Accesses are aligned on 32-byte boundaries
    - Used to transfer data to memory
    - Each interface is dedicated to a single output image.
  - Addressing modes
    - Linear
    - Circular
- Configuration interface:
  - Up to 100 MHz
  - 32-bit wide
  - Used to configure the resizer registers
- Power management:
  - Independent clock domains for the two resizers
    - Each resizer engine can be gated off separately
- Error management:
  - FIFO overflow detection on the input buffers

Figure 8-160 show the RSZ module connections to other submodules of the ISP.

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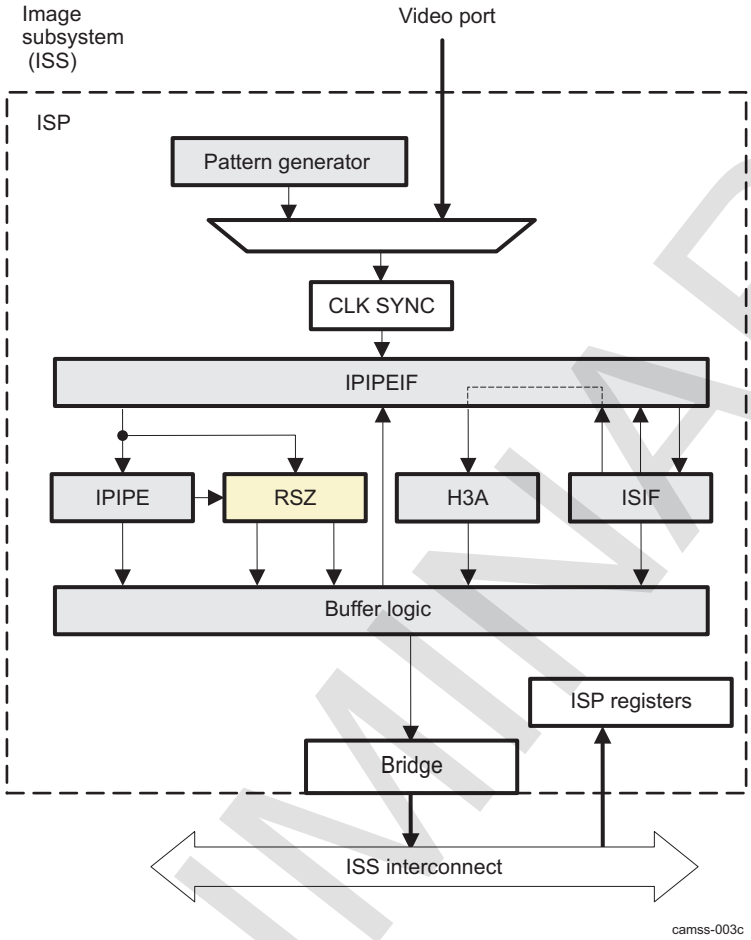
Figure 8-160. ISS ISP RSZ High-Level Diagram



8.3.3.5.2 ISS ISP RSZ Top-Level Block Diagram

Figure 8-161 is the top-level block diagram of the RSZ module. The RSZ module comprises the following submodules: cropping, input data buffering, data requestor, averager, data saturation, and resizer Interpolation (comprised of horizontal rescaler, vertical rescaler, color conversion, and output interface) (see the following sections for more information).

The RSZ module comprises two independent resizer engines with the same capabilities (except for the memory line size). The input data can come from VP 1 or VP 2. Software must determine and control which interface is selected.

The RSZ module includes one VBUSP slave port, which is used to control the RSZ registers. It also includes two MTC master ports, which are used to pass the pixels to the BL. The BL in turn creates the burst requests to the memory subsystem (see Section 8.3.3.5.3, *ISS ISP RSZ Interfaces*).

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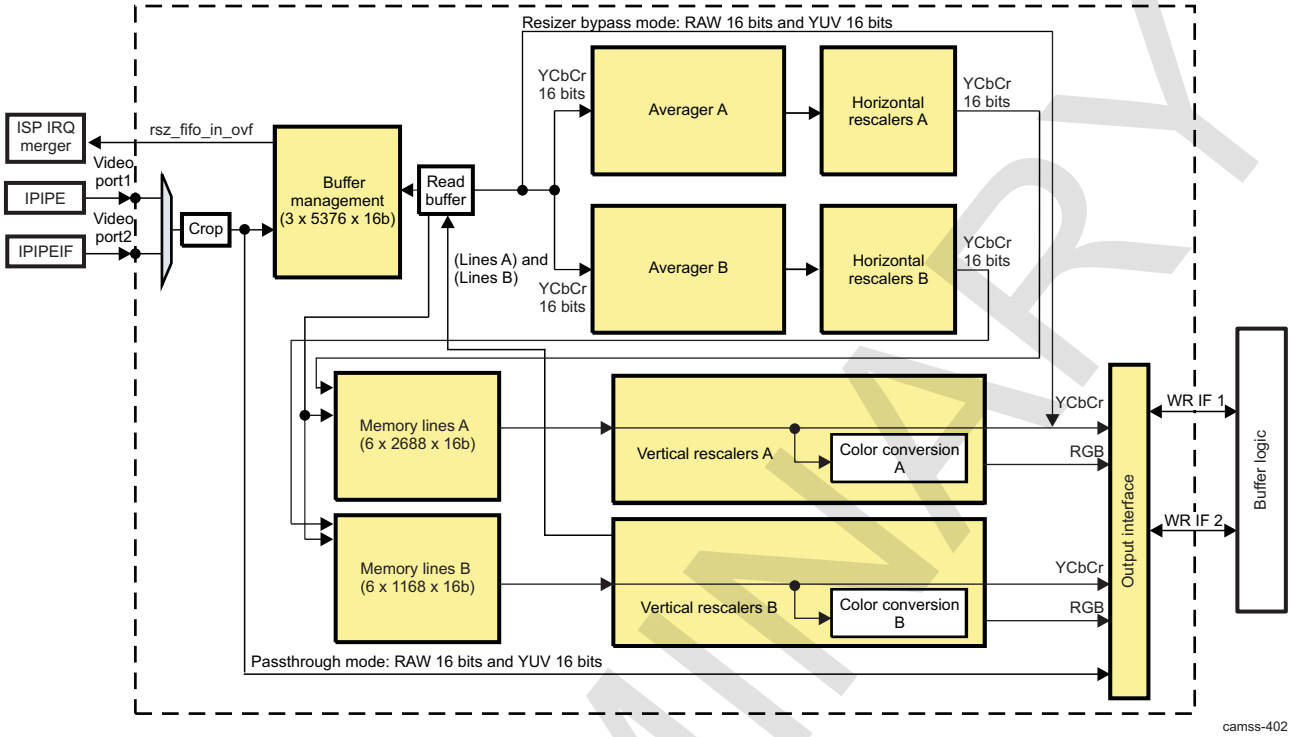
Figure 8-161. ISS ISP RSZ Top-Level Block Diagram



8.3.3.5.3 ISS ISP RSZ Interfaces

The RSZ module has the following data interfaces:

- One 32-bit read/write point-to-point pending VBUSP interface
- Two slave VP interfaces for transport YUV and RAW data
- TWO MTC interfaces to BL for RZA A and RZA B, with only write capabilities

8.3.3.5.3.1 ISS ISP RSZ VBUSP interface

The VBUSP interface is a 32-bit read/write capable interface. The VBUSP interface must be programmed in a way that back-to-back requests are possible for read and write. The RSZ_GCK_MMR[0] MMR bit enables the memory register access from the VBUSP interface to enable transfer and signal such as MMR request, direction, enable write/read data can be enabled.

8.3.3.5.3.2 ISS ISP RSZ Video Port Interfaces

The VP interfaces are slave interfaces; one is connected to IPIPE, and the other to IPIPEIF. These interfaces are for data transfer. Table 8-322 lists the format supported across IPIPE/IPIPEIF and RSZ. Signals coming from IPIPE and IPIPEIF can be write-enable signals. The RSZ_SRC_MODE[1] WRT bit is set whether or not the write enable signals are considered. This is a line-valid qualifier. This signal is sampled on the rising edge of HD, and the value is used for the full line.

Table 8-322. ISS ISP RSZ VP Supported Formats

	VP Signals: From IPIPE and IPIPEIF Modules (dat[15:0] Register)															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RAW16	R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0
YUV4:2:2 16 bits	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	Cb7 Cr7	Cb6 Cr6	Cb5 Cr5	Cb4 Cr4	Cb3 Cr3	Cb2 Cr2	Cb1 Cr1	Cb0 Cr0

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Table 8-322. ISS ISP RSZ VP Supported Formats (continued)

YUV4:2:0 Y data	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	Low	Low	Low	Low	Low	Low	Low	Low
YUV4:2:0 Cb/Cr data	Low	Low	Low	Low	Low	Low	Low	Low	Cb7 Cr7	Cb6 Cr6	Cb5 Cr5	Cb4 Cr4	Cb3 Cr3	Cb2 Cr2	Cb1 Cr1	Cb0 Cr0

NOTE: The formats are set from the IPIPE and IPIPEIF registers. For more information, see Section 8.3.3.4 and Section 8.3.3.3.

8.3.3.5.3.3 ISS ISP RSZ MTC interfaces

The RSZ module includes two write-only MTC interfaces. Their implementation enables passing a maximum of eight 32-byte requests in ten clock cycles. The RSZ must be programmed to obtain smooth and average bandwidth to buffer logic module by setting a minimum interval between two successive requests (set the RSZ_DMA_RZA[15:0] RZA and RSZ_DMA_RZB[15:0] RZB bit fields for the A and B resizers as appropriate). This setting is not expected to be dynamic. It can be fixed setting from request to request and frame to frame. When the bandwidth is set appropriately, between the first valid translated pixel and the EOF signal sent to buffer logic, the RSZ_DMA_STA[0] STATUS bit can be seen, and it is high if the transfer over the MTC interfaces is active. Figure 8-162 shows how RSZ_DMA_RZx for resizers A and B affects the MTC data request generator.

Figure 8-162. ISS ISP RSZ MTC DMA Bandwidth Control

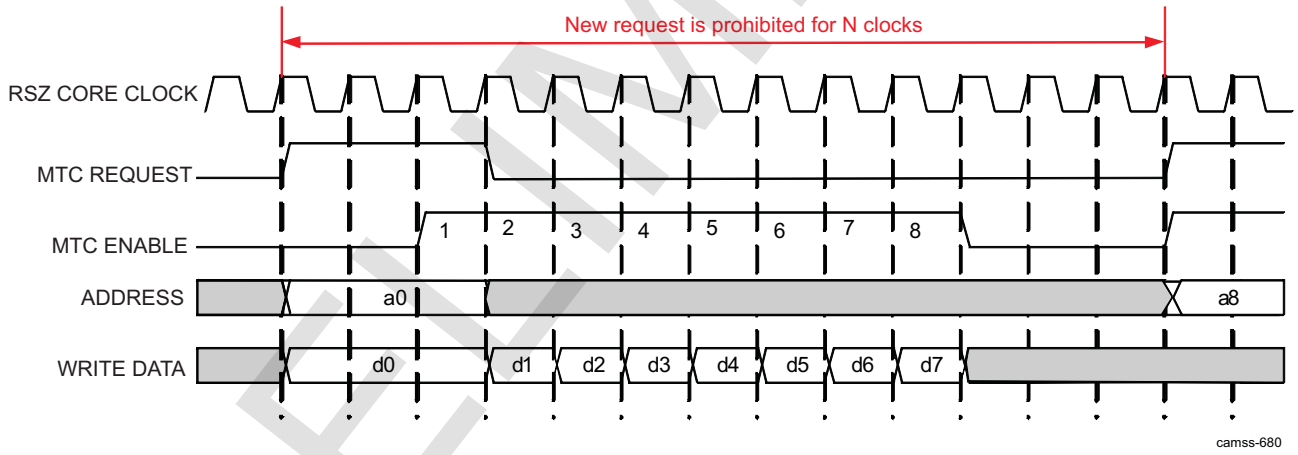

Figure 8-163 shows the pixel order in memory written by the MTC. The arrows do not represent the order in which data is written. Data are always written from left to right, whether horizontal reversal is enabled or not.

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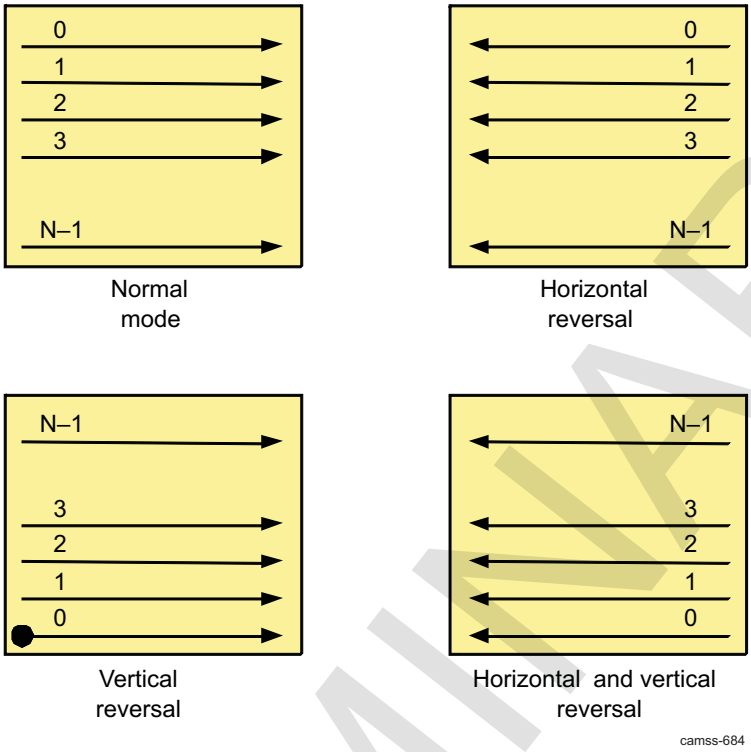
Figure 8-163. ISS ISP RSZ MTC Image Data Storage Pixel Order



8.3.3.5.4 ISS ISP RSZ Integration

Figure 8-164 shows how the VP and interfaces of the RSZ module are connected to surrounding modules at the ISP level. The RSZ module gets data from the IPIPEIF module or IPIPE module.

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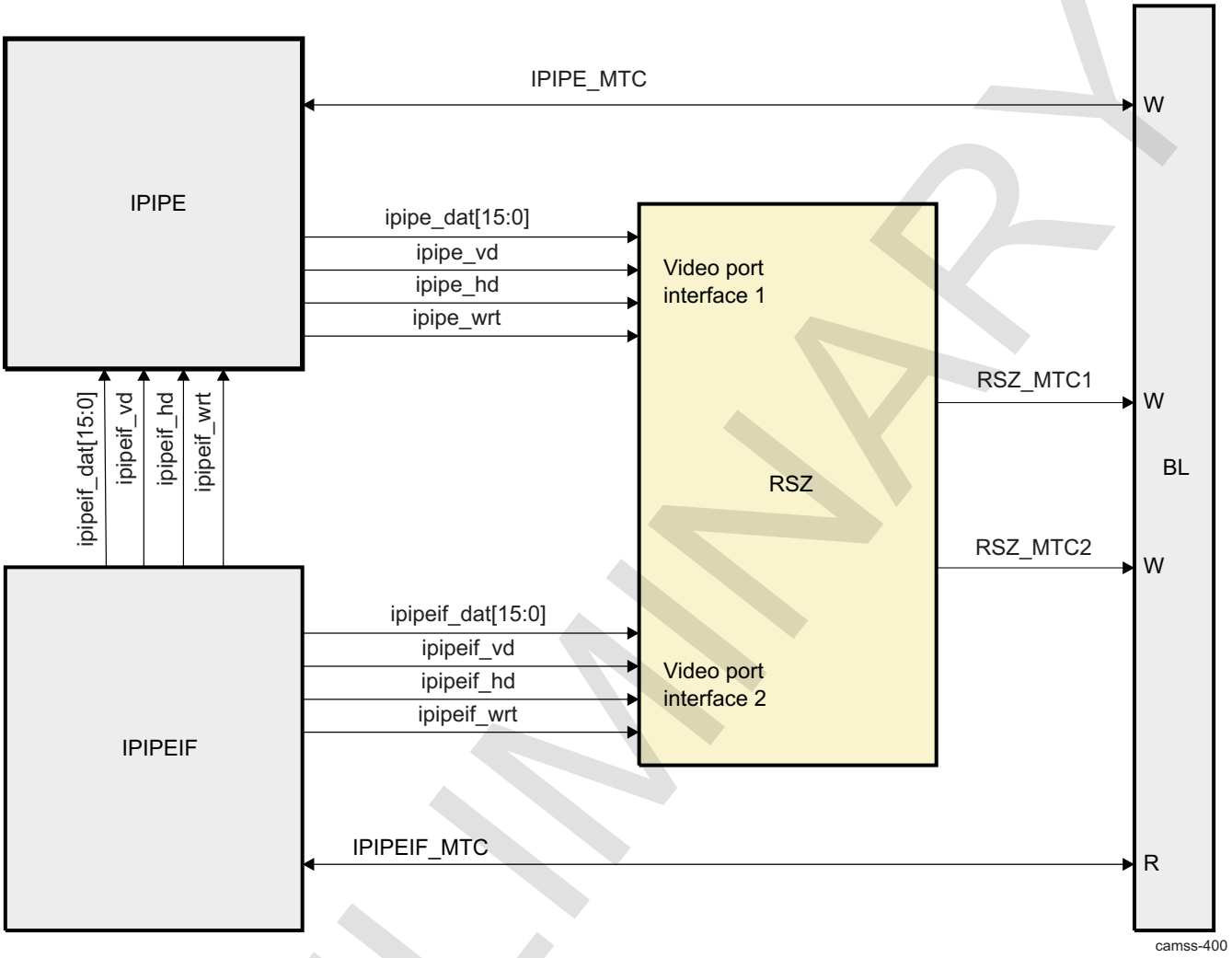
Figure 8-164. ISS ISP RSZ Typical Module Integration: High-Level Summary



The following constraints apply to the RSZ module:

- The data coming from the IPIPEIF module can be RAW or YUV4:2:2 data. Because the RSZ module can rescale only YUV4:2:2 data, the RSZ module must be configured in pass-through mode when RAW data is received on VP 2. It is possible to bypass the RSZ engine if YUV4:2:2 data is sent but rescaling is not needed (bypass mode).
- The data coming from the IPIPE module can be RAW or YUV4:2:2 data. Eventually, YUV4:2:0 data can be sent through this path, but the data must be sent in two passes. Because the RSZ module can rescale only YUV4:2:2 data, the RSZ module must be configured in pass-through mode when RAW data is received on VP 1. It is possible to bypass the RSZ engine if YUV4:2:2 data is sent but rescaling is not needed (bypass mode).

VP 2 provides a way to bypass the IPIPE module when YUV4:2:2 data is received from the images sensor or when YUV4:2:2 is read back from memory with the CCP2 RX or ISIF module.

Table 8-323 summarizes the different RSZ configuration possibilities as a function of the input data format.

Table 8-323. ISS ISP RSZ Data Flow vs. Input Data Format Constraints

VP 1 Data Format	VP 2 Data Format	RSZ-A Configuration	RSZ-B Configuration	Comments
RAW	N/A	Disabled	Disabled	RSZ module in pass-though mode

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Table 8-323. ISS ISP RSZ Data Flow vs. Input Data Format Constraints (continued)

VP 1 Data Format	VP 2 Data Format	RSZ-A Configuration	RSZ-B Configuration	Comments
N/A	RAW	Disabled	Disabled	RSZ module in pass-though mode
YUV4:2:2	N/A	Disabled	Disabled	RSZ module in pass-though mode or bypass mode
YUV4:2:2	N/A	Enabled	Disabled	One output image
YUV4:2:2	N/A	Disabled	Enabled	One output image
YUV4:2:2	N/A	Enabled	Enabled	Two output images
N/A	YUV4:2:2	Disabled	Disabled	RSZ module in pass-though mode or bypass mode
N/A	YUV4:2:2	Enabled	Disabled	One output image
N/A	YUV4:2:2	Disabled	Enabled	One output image
N/A	YUV4:2:2	Enabled	Enabled	Two output images

8.3.3.5.5 ISS ISP RSZ Functional Description

To start up, the RSZ configuration can be set from the RSZ_SYSCONFIG register, which provides enabling the RSZ-A and RSZ-B clocks. The RSZ module does not have standalone reset and status check. Software reset must be done at the ISP level. Moreover, when enabled, the RSZ module can control the input data buffer, and when the rsz_stall_input signals are set from the RSZ_IN_FIFO_CTRL register, the RSZ module generates a stall signal that can be used by the master module sending data to the RSZ module when the data threshold is too high.

The RSZ_SRC_EN[0] EN bit starts the resizer processing. If the processing mode is set to one shot (one run and then turn off) from the RSZ_SRC_MODE[0] OST bit, the EN bit is cleared to 0.

The resizer can be configured to be bypassed in certain cases (see Figure 8-164 for the module constraints) from the RSZ_SRC_FMT0[1] BYPASS bit. The data can be sent directly from here to the output interface (bypass mode) or imported to the module buffer, but not manipulated and sent to the output interface (pass-through mode). The master device sending data to the resizer can be switched between IPIPEIF and IPIPE using the RSZ_SRC_FMT0[0] SEL bit. The resizer understanding of the data input is set from the RSZ_SRC_FMT1 register (for more information, see Table 8-325). The RSZ_SEQ.VRVX and RSZ_SEQ.HRVX registers can be set to flip the image horizontally or vertically, respectively (see Figure 8-163).

Depending on the mode to which the resizer is set, the core clock can be enabled from the RSZ_GCK_SDR register. Table 8-324 summarizes the behavior of the module for the different settings.

Table 8-324. ISS ISP RSZ Module Modes: Register Settings

Configuration Number	RSZ_SRC_EN	RZA_EN	RZA_CLK_EN	RZB_EN	RZB_CLK_EN	RSZ_GCK_SDR.CORE	RSZ_SRC_FMT0.BYPASS	Comments
0	0	X	X	X	X	X	X	Data cannot go through the RSZ module.
								Interrupts are not issued.
1	1	0	X	0	X	1	0	Resizer A is disabled.
								Resizer B is disabled.
								It is best to have RZA_EN = RZB_EN = 0 to save power, but RZA_EN = RZB_EN = 1 is also supported.
								This configuration is supported but does not make sense because data cannot go through the module.
2	1	1	1	0	X	1	0	Resizer A is enabled.
								Resizer B is disabled.

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Table 8-324. ISS ISP RSZ Module Modes: Register Settings (continued)

								It is best to have RZB_EN = 0 to save power, but RZB_EN=1 is supported as well.
3	1	0	X	1	1	1	0	Resizer A is disabled.
								Resizer B is enabled.
								It is best to have RZA_EN = 0 to save power, but RZA_EN = 1 is also supported.
4	1	1	1	1	1	1	0	Resizer A is enabled.
								Resizer B is enabled.
5	1	X	X	X	X	0	0	Bypass mode is enabled.
								Resizer core functional clock is disabled.
6	1	X	X	X	X	0	1	Pass-through mode enabled.
								Resizer core functional clock is disabled.
7	1	X	X	X	X	1	1	Pass-through mode is enabled.
								Resizer core functional clock is enabled.
								Not a preferred configuration. Configuration (6) saves power.

Table 8-325. ISS ISP RSZ Module Input Control: Register Settings

RSZ_SRC_FMT1.IN420	RSZ_SRC_FMT1.COL	Comments
0	X	YUV4:2:2 input. Chrominance is cosited.
1	0	YUV4:2:0 input. Valid data is Y, C is dummy. On the VP, YUV4:2:2 data is always assumed.
1	1	YUV4:2:0 input. Valid data is C, Y is dummy. On the VP, YUV4:2:2 data is always assumed.

The RSZ_YUV_PHS[0] POS bit sets the chrominance output. The RSZ module does not change the relative position of the chroma samples versus the luma samples between the input and output, and the chroma position at the output of the IPIPE module and at the output of the RSZ module must be identical. In other words, RSZ_YUV_PHS.POS = IPIPE_YUV_PHS.POS.

Settings are common for both resizer engines inside the RSZ module. Each engine (RZA or RZB) can be enabled from the RZx_EN register: select the mode from RZx_MODE, and select the input and output in the YUV color scheme from the RZx_420 register (valid only if YUV 4:2:2 is the input set from RSZ_SRC_FMT1.IN420). Table 8-326 summarizes the combination of settings available in the RZx_420 register.

Table 8-326. ISS ISP RSZ-A/RSZ-B Output Format Selection

RZx_420.YEN	RZx_420.CEN	Comments
0	0	Input is YUV4:2:2. Output is YUV4:2:2 if RZX_RGB_EN = 0 and RGB if RZB_RGB_EN = 1.
0	1	Input is YUV4:2:2. Output is the chroma of YUV4:2:0. RZX_RGB_EN is ignored. Must be used to rescale YUV4:2:0 data: 1st/2nd pass
1	0	Input is YUV4:2:2 .Output is the luma of YUV4:2:0. RZX_RGB_EN is ignored. Must be used to rescale YUV4:2:0 data: 2nd/1st pass
1	1	Input is YUV4:2:2 .Output is YUV4:2:0. RZX_RGB_EN is ignored.

8.3.3.5.5.1 ISS ISP RSZ Operating Modes

The RSZ module offers two basic rescaling modes. These modes are not built-in but are particular configurations, which means that other hybrid modes can be programmed. The normal mode provides more flexibility (the rescale ratio granularity is smaller) than downscale mode, but downscale mode produces better image quality (averager performs anti-aliasing):

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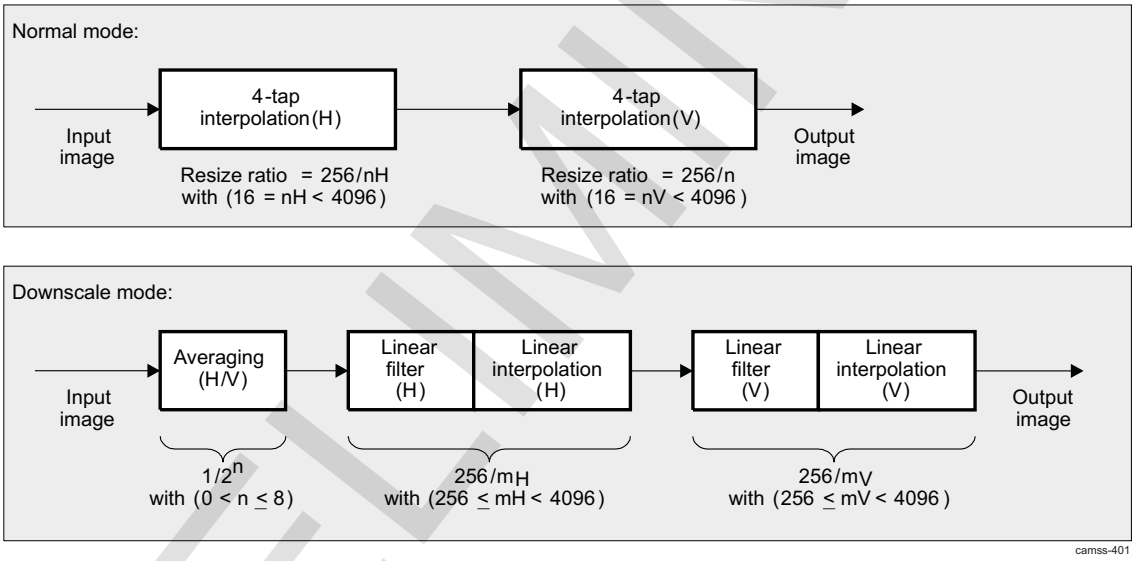
- Normal mode: The scaling process is carried out using interpolation with a 4-tap filter. The interpolation method is a 4-tap cubic convolution or a 3-tap linear filter + 2-tap linear interpolation. The user controls the type of interpolation that is used. The possible rescale ratios range from 1/16x to 20x.
- Downscale mode: The scaling process is the same as for normal mode, but an averaging function is placed before. It enables reaching much higher reduction factors while avoiding anti-aliasing artifacts. The interpolation method is a 4-tap cubic convolution or a 3-tap linear filter + 2-tap linear interpolation. The possible rescale ratios range from 1/4096x to 1x.

NOTE: The selection of the mode is independent for each resizer engine. One resizer engine can be configured in normal mode, while another is configured in downscale mode.

The RSZ module can produce two output images simultaneously, because there are two independent resizer engines. The input data used by the two resizer engines is the same. The RSZ output image sizes are limited to RSZ_GNC[0:12] RSZA_MEM_LINE_SIZE pixels/line for RSZ-A (5376 pixels/line) and RSZB_MEM_LINE_SIZE[16:28] for RSZ-B (2336 pixels/line).

Figure 8-165 shows the RSZ operating modes. Nothing prevents the use of linear interpolation in normal mode or bicubic interpolation in downscale mode; similarly, it is possible to mix the interpolation modes for horizontal and vertical filtering. This is fully programmable.

Figure 8-165. ISS ISP RSZ Operating Modes



8.3.3.5.5.1.1 ISS ISP RSZ Operating Modes and Maximum Input Clock

The maximum output pixel clock on both resizers is 200 MHz (100 percent optimal power performance [OPP]); that is, a pixel throughput of 200 MPix/s. Moreover, hardware takes care of the following constraints:

- When both resizer engines are configured to perform downscaling, there is no particular constraint on the VP pixel clock. The VP pixel clock can be as high as 200 MHz.
- When one resizer engine is configured to perform upscaling and the second resizer engine is configured to perform downscaling, the VP pixel clock must be limited. The VP must be lower than:

clk_pix = (200 MHz/(Vertical Upscale Ratio * Horizontal Upscale Ratio)) (5)

For example, if a 4x upscale ratio happens horizontally and vertically, then the input pixel clock must be lower than 200/(4*4) = 12.5 MHz.

It is the reason why it is not possible to perform digital zoom upscaling on the fly. It is necessary to acquire the pixels to memory first and to read them back at a pace that does not exceed the previously discussed constraints. At the ISS level, data can be read back from memory from the CCP2 RX or ISIF module.

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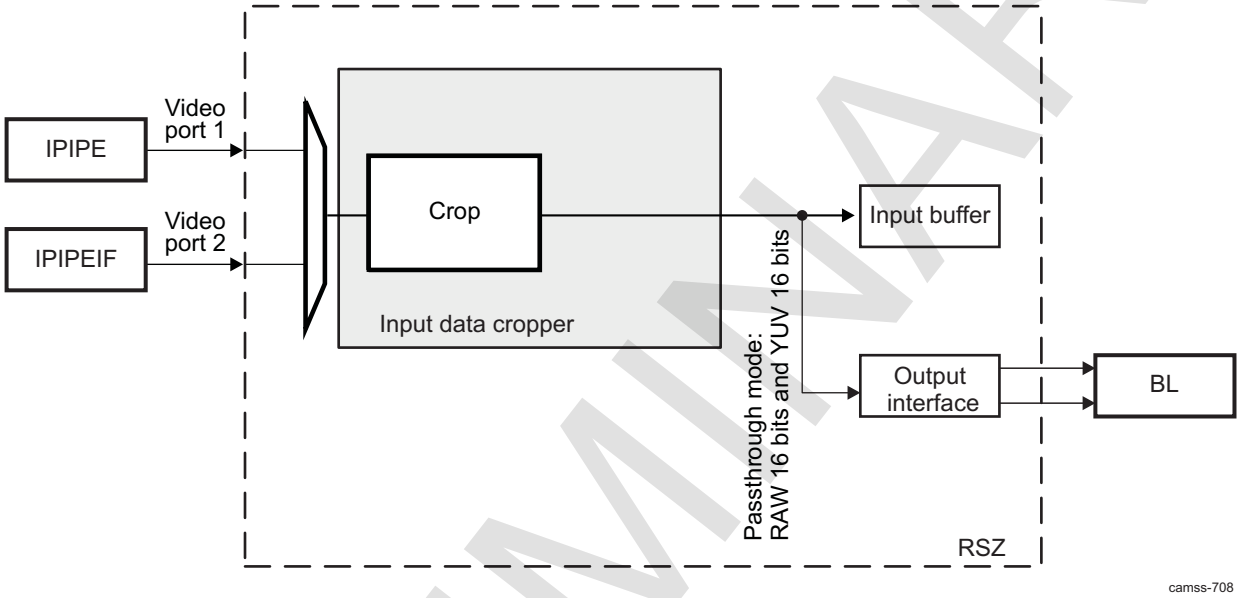
- When the two resizer engines are configured to perform upscaling, the VP pixel clock must be limited. In that case, the VP frequency is limited by the resizer engine having the larger rescale ratios.

8.3.3.5.5.2 ISS ISP RSZ Input Data Cropper

The data coming from the VPs into the RSZ module can be cropped: this applies to RAW and YUV4:2:2 data. It is mandatory to crop the data as early as possible in the RSZ processing pipeline to reduce power consumption. It is mandatory to crop the data before storing it in the input data buffer. Figure 8-166 is the block diagram of the RSZ input data cropper.

Figure 8-166. ISS ISP RSZ Input Data Cropper Block Diagram



The input data are in YUV4:2:2 interleaved format or RAW format.

For YUV4:2:2 format, the data come as Cb0, Y0, Cr0, Y1, Cb2, Y2, Cr2, Y3, etc. Y denotes the luma component value and Cb/Cr denotes the chroma component values. There are as many Y components as Cb/Cr components per line.

Figure 8-167 shows input data cropping. Only the cropped data is stored in the input data buffer. The names used in the figure correspond to the register names. If no cropping is desired, the RSZ_SRC_HPS and RSZ_SRC_VPS registers, which set the horizontal and vertical positions, must be set to 0; the start size from the RSZ_SRC_HSZ register must be set to the input image width minus 1, and the RSZ_SRC_VSZ register must be set to the input image height minus 1. These are typical settings for both resize engines inside the RESIZER. After setting, more flexibility is present through RZx_i_VPS and RZx_i_HPS for vertical and horizontal positioning, respectively, of the input/output (where x = A or B, i = I or O).

Depending on the input data format, different constraints apply to the registers that set the cropping parameters:

- For YUV4:2:2 format, the vertical start positions of the cropped frame can be even or odd. However, the horizontal start position must be even: the reason is to always start with the same pattern: Cb_{2n}, Y_{2n}, Cr_{2n}, Y_{2n+1},.. For the same reason, the horizontal size of the cropped frame (RSZ_SRC_HSZ + 1) must be an even number. Finally, the vertical size of the cropped frame can be odd or even.
- For RAW format, the vertical start position of the cropped frame can be even or odd. The vertical size can be even or odd. The horizontal resolution must be even.

These features and constraints are common for both resizer engines inside the resizer module. Figure 8-167 shows the input data cropping.

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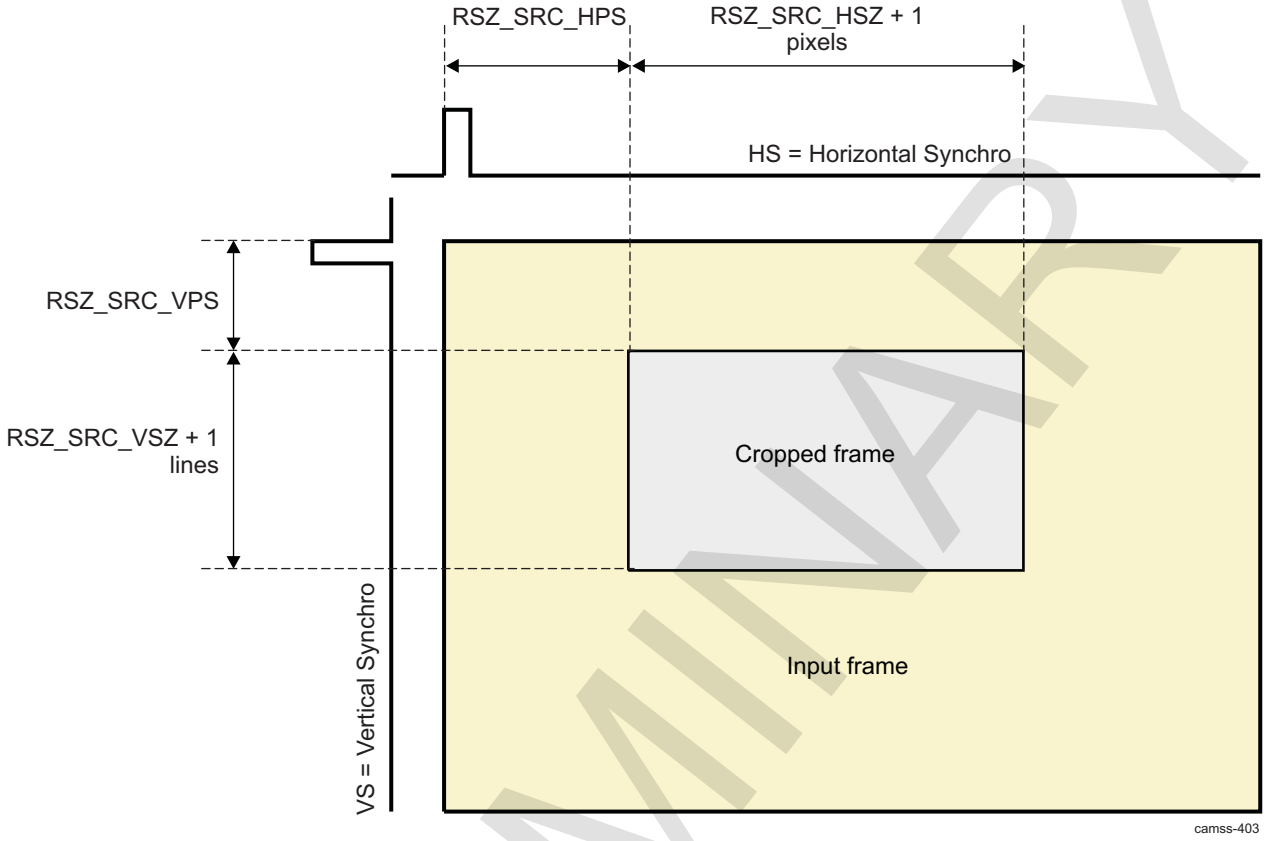
Figure 8-167. ISS ISP RSZ Input Data Cropping



8.3.3.5.5.3 ISS ISP RSZ Averager

8.3.3.5.5.3.1 ISS ISP RSZ Use Cases

The two RSZ engines can have independent averager settings:

- Both resizers can use it.
- One resizer can bypass it and the other can use it.
- Both resizers can bypass it.

8.3.3.5.5.3.2 ISS ISP RSZ Memory Utilization

Vertical averaging requires memory to perform pixel data accumulation. It shares the vertical memory lines that are used for vertical filtering: this is the reason why the vertical memory lines are organized as two banks of half lines.

- The averagers output lines that are at most half the size of the input image in one memory bank.
- The horizontal resizers write their output data in the second memory banks.

Figure 8-168 shows the use of memory when the averager is enabled or disabled.

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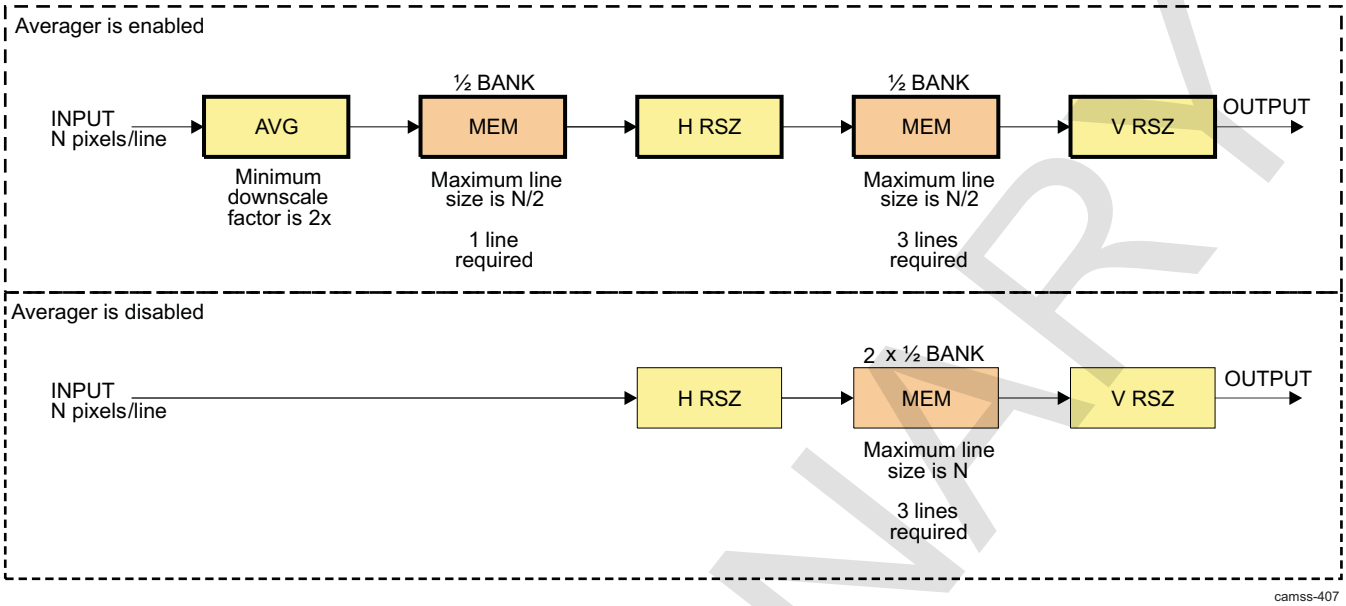
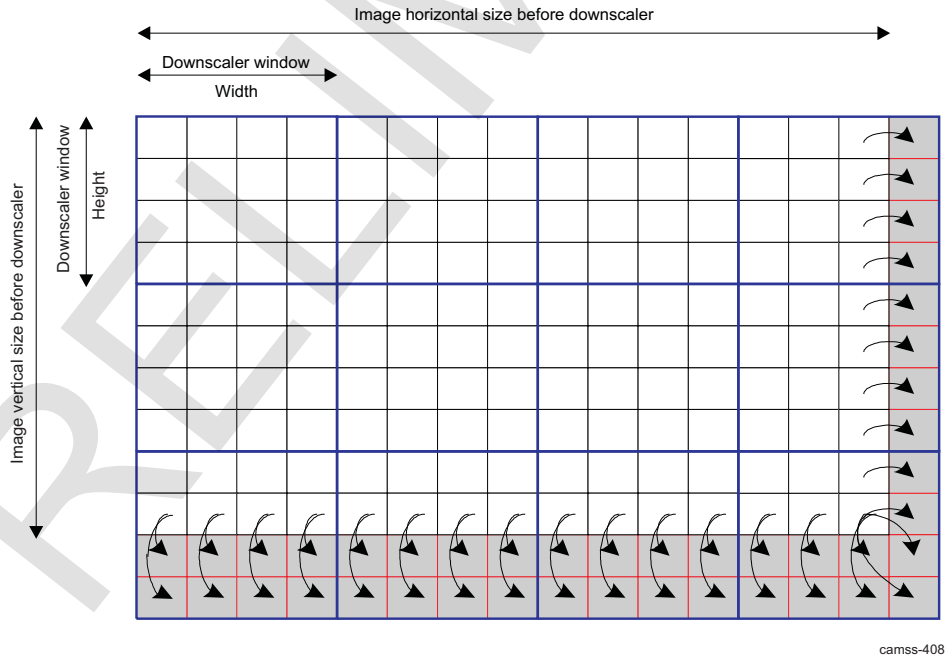
Figure 8-168. ISS ISP RSZ Averager Memory Utilization



8.3.3.5.5.3.3 ISS ISP RSZ Border Conditions

Figure 8-169 shows the averager behavior for border conditions. If the input image is not big enough, border duplication must occur.

Figure 8-169. ISS ISP RSZ Averager Border Conditions



Downscaling is enabled from the RZi_DWN_EN register. Moreover, the vertical averaging size is set by the RZA_DWN_AV[3:5] V bit field. The actual downscale ratio is given by $1/2^{(RZA_DWN_AV[3:5]\ V\ +1)}$. The range is from 1/2 to 1/256 in power of two. The horizontal averaging size is set by the RZA_DWN_AV[0:2] H bit field. The actual downscale ratio is given by $1/2^{(RZA_DWN_AV[3:5]\ H\ +1)}$. The equations are the same for RSZ-B. The range goes from 1/2 to 1/256 in power of 2.

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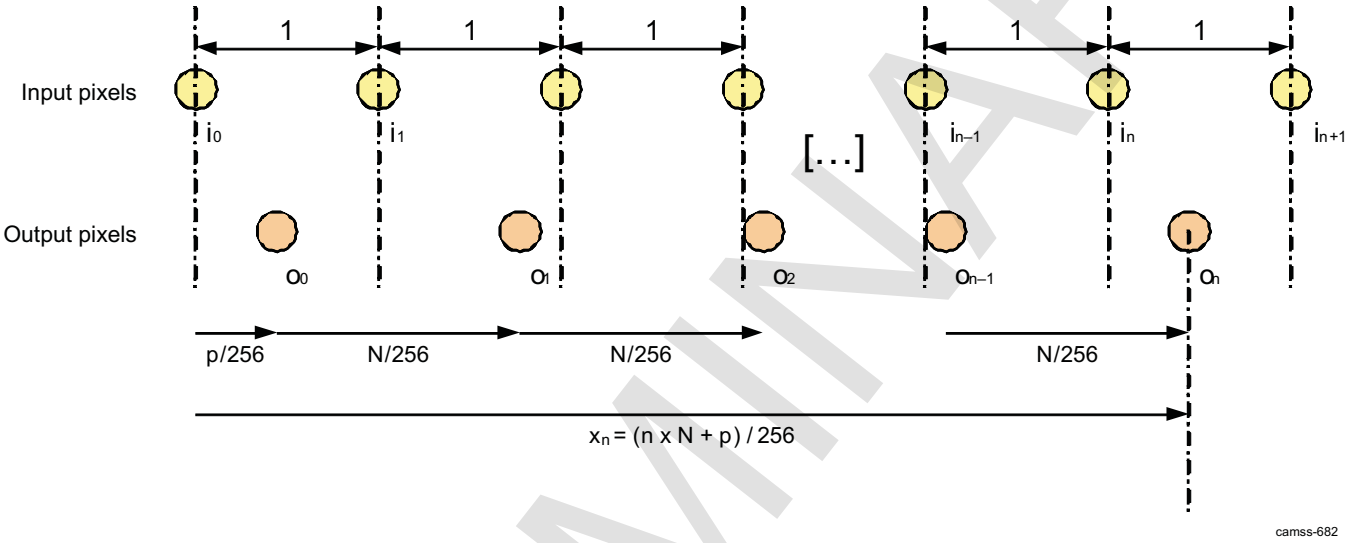
8.3.3.5.5.4 ISS ISP RSZ Interpolation

Figure 8-170 shows the basic interpolation method used in the RESIZER module. The following assumptions are made:

- The distance between each input pixel is 1.
- The magnification ration is given by 256/N and p/256 is the initial phase of the output data.

The output pixels are also evenly spaced. The distance between each output pixel is given by N/256. In the example in Figure 8-170, N is greater than 256. The position of the n^{th} output pixel is given by (n x N + p) / 256.

Figure 8-170. ISS ISP RSZ Basic Interpolation Method



Assuming the intensity of input pixels is i_0, i_1, i_2, etc. and the resized (output) pixels are o_0, o_1, o_2, etc., the n^{th} output pixel (o_n) is determined using the nearest 4 input pixels as follows:

$o_n = h(1+d) \times i_1 + h(d) \times i_m + h(d-1) \times i_{m+1} + h(d-2) \times i_{m+2}$

In the previous equation h(x) is the interpolation main function. The RESIZER module supports linear and bicubic convolution interpolation functions.

Figure 8-171 shows the interpolation principle at the n^{th} output pixel (on) at position xn. Furthermore, the m and d parameters are as follows:

m = floor((n x N + p) / 256) and d = ((n x N + p) / 256) – m

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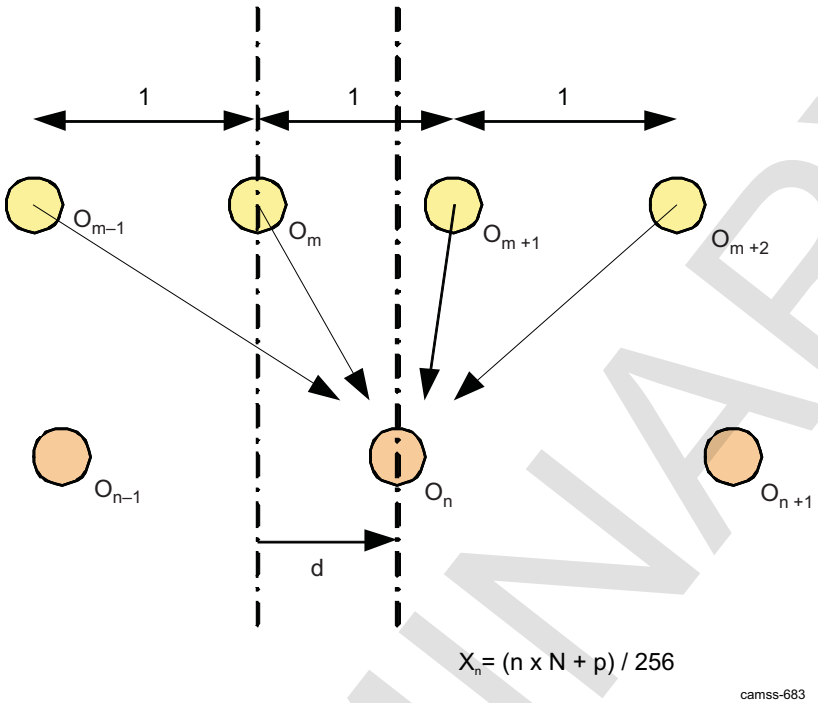
Figure 8-171. ISS ISP RSZ Interpolation Filtering



For each resizer (RSZ-A or RSZ-B), and for chrominance and luminance, the interpolation method for vertical interpolation can be a 2-tap linear interpolation or a 4-tap cubic convolution (default) method. The choice is made in RZi_V_TYP[0] Y for luminance and RZi_V_TYP[1] C for chrominance, where i = A or B and is the resizer number. It is similar for horizontal interpolation from RZi_H_TYP[0] Y for luminance and RZi_H_TYP[1] C for chrominance, where i = A or B and is the resizer number.

8.3.3.5.5.4.1 ISS ISP RSZ Liner Interpolation Input Data

Before data interpolation, a low pass filtering (LPF) operation is required on the input data. The following equation gives the LPF function. The equation is evaluated at pixel position d_i but neighbor pixels d_{i-1} and d_{i+1} are required. The gain value g is set up by the register RZi_V_LPF and RZi_H_LPF. Different gains are possible horizontally and vertically as well as for Luma and Chroma.

$LPF_g (d_{i-1}, d_i, d_{i+1}) = d_i + g \times (d_{i-1} - 2d_{i+1} + d_{i+2})/128$

8.3.3.5.5.4.1.1 ISS ISP RSZ Cubic Convolution Mode

The input data is not modified in bicubic mode. Basically, the input is equal to the output.

8.3.3.5.5.4.1.2 ISS ISP RSZ Phase Settings

The initial value for the phase value for vertical resizing is set by the RZi_V_PHS_Y for luminance and RZi_V_PHS_C for chrominance. These values are in the U14Q8 fractional format (values in the range [0 – 63.996]). When YUV4:2:2 data are output, the phase value for Luma and Chroma must be aligned; that is, RZi_V_PHS_Y = RZi_V_PHS_C.

The following constraint equation applies: | RZi_V_PHS_Y - RZx_V_PHS_C | = RZi_V_DIF . This constraint means that at most the distance between the initial phases for luminance and chrominance is not expected to exceed the distance between two Luma pixels. The absolute value is used; therefore, the initial Luma phase can be greater than the initial Chroma phase or vice versa. As a reminder, the distance between two output pixels for Luma is given by RZi_V_DIF.

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The initial value for the phase value for horizontal resizing is set by the RZi_H_PHS bit field. The RZi_H_PHS_ADJ register enables adjusting the horizontal phase for the Luma component when averaging is enabled (the averager disrupts the relative sampling point between luminance and chrominance when YUV4:2:2 cosited data is input). The relative phase between Luma and Chroma is different before and after the horizontal averager. The vertical phase is not affected by the averager. Figure 8-172 shows the effect of the averager on the phases. RZi_H_PHS_ADJ is expected to be equal to zero if the averager is disabled.

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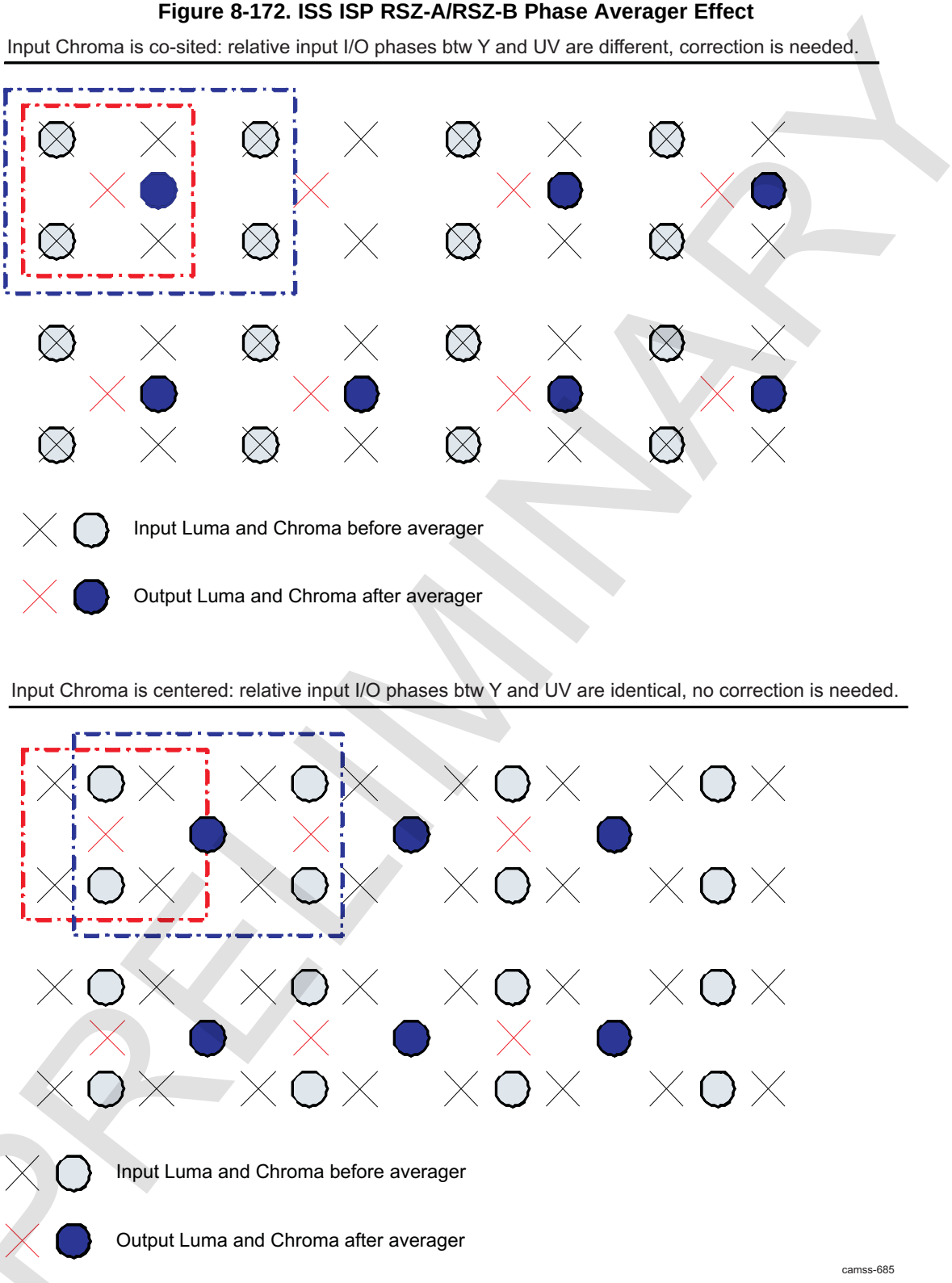
Figure 8-172. ISS ISP RSZ-A/RSZ-B Phase Averager Effect



8.3.3.5.5.5 ISS ISP RSZ Data Saturator

After vertical rescaling and before color conversion, the output data is saturated (clipped) to programmable values that are given by the following registers:

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- RSZ_YUV_Y_MIN
- RSZ_YUV_Y_MAX
- RSZ_YUV_C_MIN
- RSZ_YUV_C_MAX

The maximum Y value is set up with the RSZ_YUV_Y_MAX register. If the Input Y value is greater than the MAX value, it is clipped to MAX.

The minimum Y value is set up with the RSZ_YUV_Y_MIN register. If the Input Y value is smaller than the MIN value, it is clipped to MIN.

The maximum Cb/Cr value is set up with the RSZ_YUV_C_MAX register. If the Input Cb/Cr value is greater than the MAX value, it is clipped to MAX.

The minimum Cb/Cr value is set up with the RSZ_YUV_C_MIN register . If the Input Cb/Cr value is smaller than the MIN value, it is clipped to MIN.

8.3.3.5.5.6 ISS ISP RSZ Color Convertor

As mentioned previously, the resizer can support RAW, YUV4:2:0, and YUV4:2:2 formats. The resizer engines can also support RGB output: RGB5:6:5 and ARGB32.

The RGB5:6:5 data is 16 bits wide and consists of 5 bits for red, 6 bits for green, and 5 bits for blue.

The following table shows the way RGB5:6:5 is stored to memory. This data format is compatible with the display controller. Only the little-endian memory representation is supported.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R1					G1						B1					R0					G0							B0				

The ARGB32 data is 32 bits wide and consists of 8 bits for alpha, 8 bits for red, 8 bits for green, and 8 bits for blue. The alpha value is global and is set for the entire frame; registers control the alpha value: the RZx_RGB_BLD register controls the alpha values of resizer A and resizer B.

The following table shows the way ARGB32 is stored to memory. This data format is compatible with the display controller. This representation is endiannism invariant: it is the same for little endian and big endian.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
A								R								G								B							

The RGB output is enabled by setting the RZx_RGB_EN[0] RGB_EN bit to 1.

The RGB format is set by the RZx_RGB_TYP[0] TYP bit (0 for ARGB32 format and 1 for RGB5:6:5).

To handle the horizontal border conditions, the leftmost Chroma sample or the right-most Chroma sample is duplicated on the left or the right.

Software must make it possible to remove 2 pixels on the left and/or right to take care of the issues that Chroma duplication introduces on the borders. The RZx_RGB_TYP[1] MSK0 and RZx_RGB_TYP[2] MSK1 bits control this feature.

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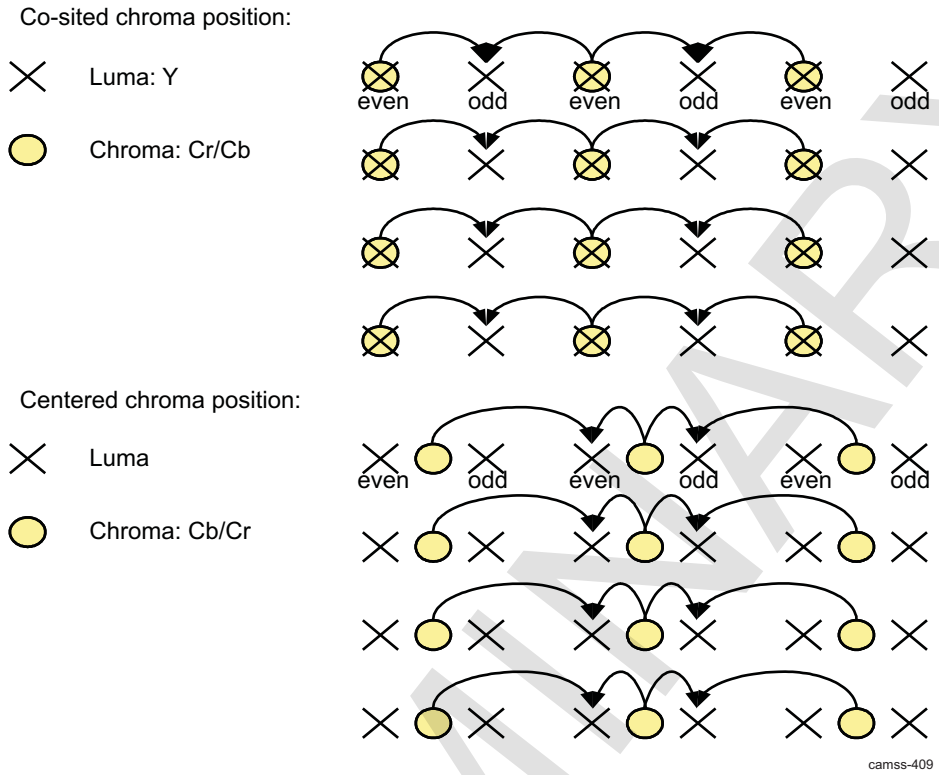
Figure 8-173. ISS ISP RSZ Chroma Position and Upsampling



8.3.3.5.5.7 ISS ISP RSZ Output Interface

The output interface receives the data generated by the two resizer engines and generates the addresses and the port requests to the BL module.

- The port 1 interface is dedicated to the RSZ-A module. If the RSZ module is set up in pass-through mode, then the data is output on the port 1 interface. This interface can transfer RAW, YUV4:2:2, YUV4:2:0 and RGB data
- The port 2 interface is dedicated to the RSZ-B module. This interface can transfer RAW, YUV4:2:2, YUV4:2:0 and RGB data.

The YUV4:2:0 data format is handled differently from the other formats because the output data are written at two different memory locations: luminance in one buffer and chrominance in a second buffer. For all other formats the data are written in the same buffer.

Each data format must be stored in memory in a dedicated manner, which is summarized in Table 8-327.

Table 8-327. ISS ISP RSZ Output Interface: Data Formats

Output Format	Bytes per Pixel	Output Buffers per Image	Interface Supporting the Data Format
RAW	2	1	MTC port 1
YUV4:2:2	2 average	1	MTC port 1 port 2
YUV4:2:0	1.5 average	2	MTC port 1 port 2
RGB16	2	1	MTC port 1 port 2
ARGB32	4	1	MTC port 1 port 2

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8.3.3.5.5.7.1 ISS ISP RSZ Circular Buffer

Figure 8-174 shows the parameters that are required to set up the circular buffers. As mentioned previously, there can be up to four circular buffers in case the two resizer engines are outputting YUV4:2:0 data.

The circular buffer management requires the following parameters (REZ-A or RSZ-B A or B ,chrominance or luminance Y or C, low or high part of the address, L or H. Sets the base address of the circular buffer):

- Baseline address (BAD, in registers, where x is the resizer A or B, and i is Y or C)
- Start address (SAD, in RZx_SDR_i_SAD_j registers)
- Start pointer (PTR_S, in RZx_SDR_i_PTR_S registers)
- End pointer (PTR_E, in RZx_SDR_i_PTR_E registers)
- Line offset (OFT, in RZx_SDR_i_OFT registers)

Circular Buffer Parameter	Register (for RSZ-A and RSZ-B)	Description
Baseline address	RZA_SDR_Y_BAD_H RZA_SDR_Y_BAD_L RZA_SDR_C_BAD_H RZA_SDR_C_BAD_L RZB_SDR_Y_BAD_H RZB_SDR_Y_BAD_L RZB_SDR_C_BAD_H RZB_SDR_C_BAD_L	Sets the base address of the circular buffer
Start address	RZA_SDR_Y_SAD_H RZA_SDR_Y_SAD_L RZA_SDR_C_SAD_H RZA_SDR_C_SAD_L RZB_SDR_Y_SAD_H RZB_SDR_Y_SAD_L RZB_SDR_C_SAD_H RZB_SDR_C_SAD_L	Sets the start address of the circular buffer. The first data output is written to this address. If the first line of a frame must be written at the beginning of the circular buffer memory, then SAD = BAD and PTR_S = 0.
Start pointer	RZA_SDR_Y_PTR_S RZA_SDR_C_PTR_S RZB_SDR_Y_PTR_S RZB_SDR_C_PTR_S	Sets the initial value of the circular buffer internal counter. It must be set up as PTR_S = (SAD - BAD)/OFT. PTR_S is expressed in the number of lines.
End pointer	RZA_SDR_Y_PTR_E RZA_SDR_C_PTR_E RZB_SDR_Y_PTR_E RZB_SDR_C_PTR_E	Sets the size of the circular buffer. PTR_E is expressed in the number of lines. The circular buffer can contain up to PTR_E lines.
Line offset	RZA_SDR_Y_OFT RZA_SDR_C_OFT RZB_SDR_Y_OFT RZB_SDR_C_OFT	This is the offset expressed in bytes between two lines in the circular buffer. Here: Line 0 = SAD, Line 1 = SAD + 1 x OFT, Line 2 = SAD + 2 x OFT, etc. OFT does not necessarily correspond to the size of a line in a frame; it can be bigger.

More generally, the following equations hold:

- SAD = BAD + (PTR_S x OFT) and PTR_S PTR_E

Interrupts can be triggered every time a certain number of lines are written to the circular buffer. There are independent settings for each resizer and for each possible output of each resizer.

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Figure 8-174. ISS ISP RSZ and Circular Buffer Settings

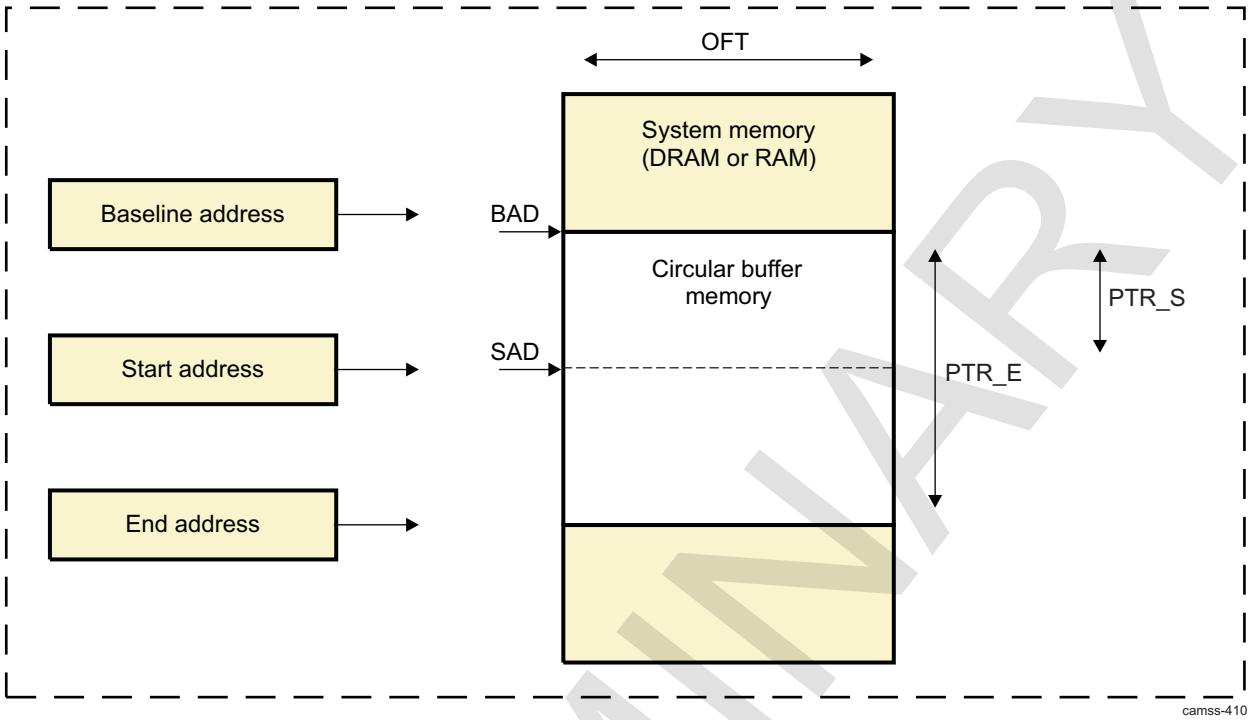

Figure 8-175 shows how the data are stored in the circular buffer over time when vertical flip is disabled. In this example, PTR_S = 5 and PTR_E = 7. There can be up to PTR_E = 7 lines in the circular buffer.

Figure 8-175. ISS ISP RSZ and Circular Buffer Settings – Example 1

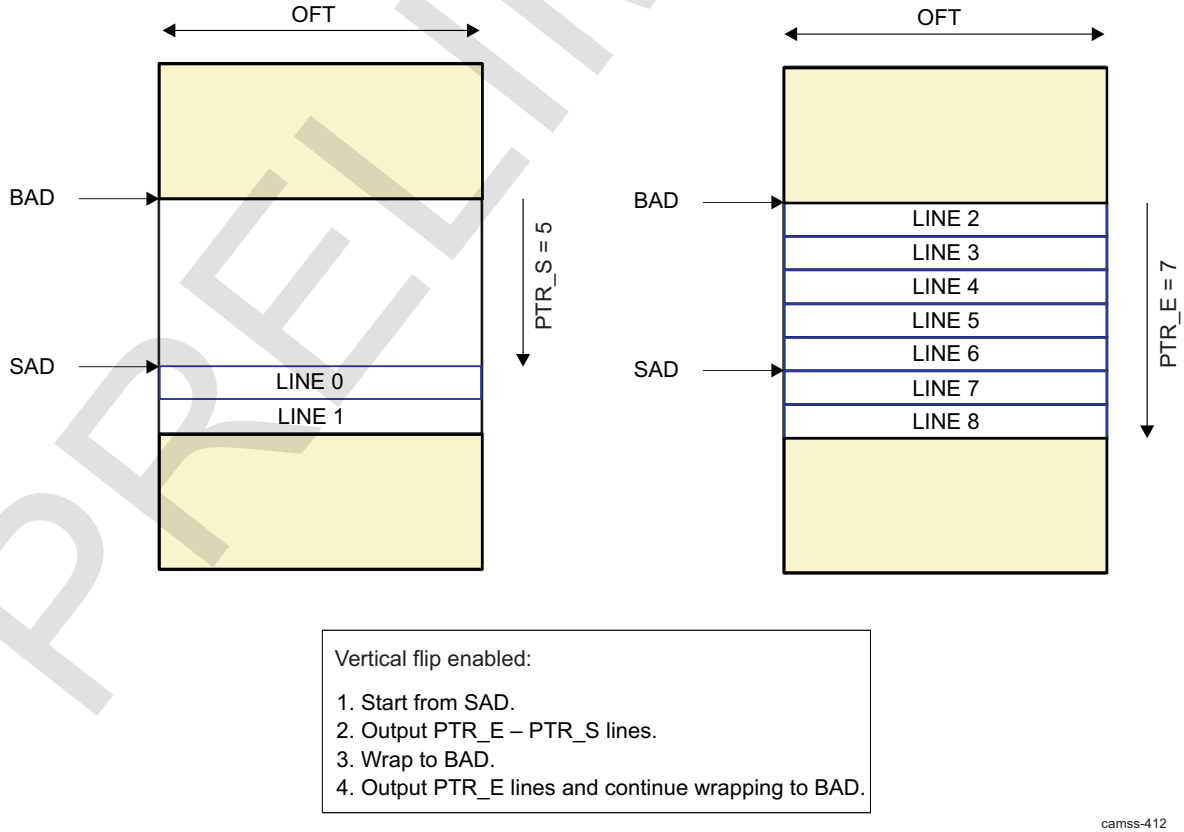

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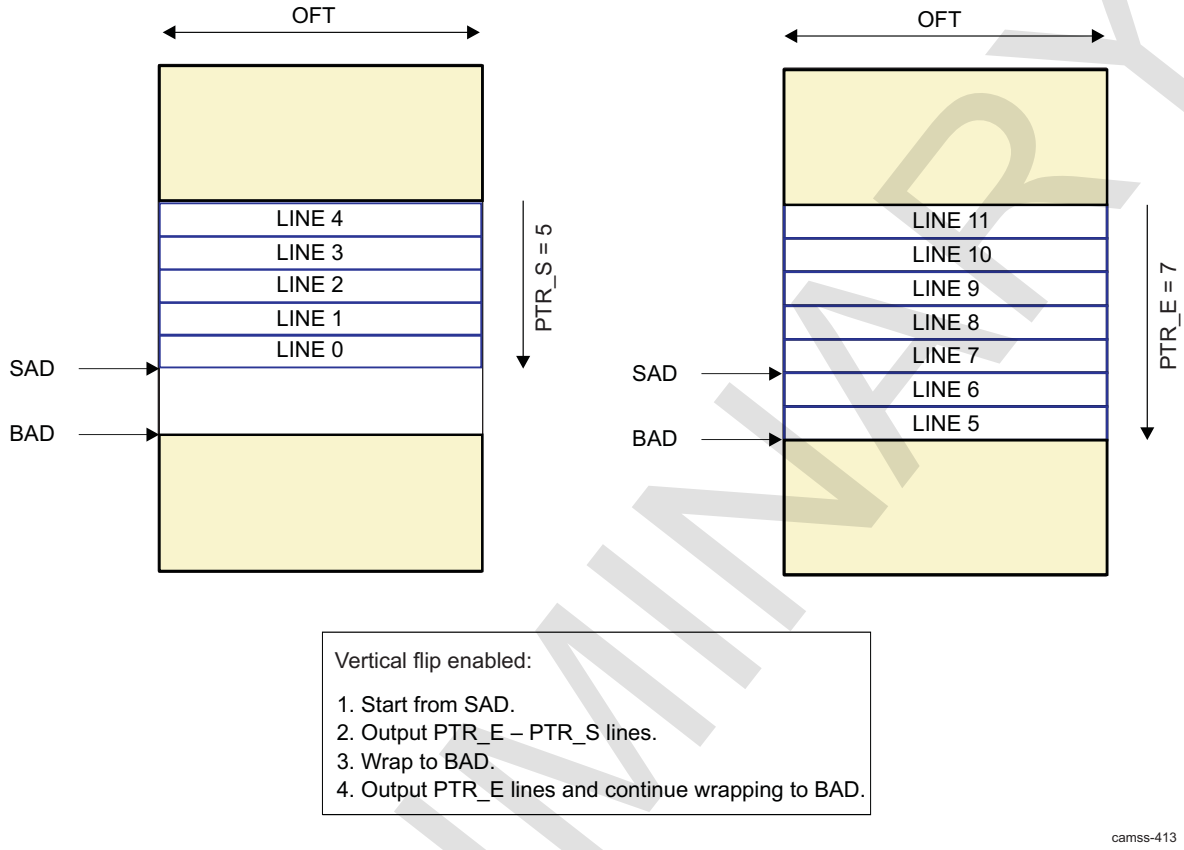
Figure 8-176 shows how the data are stored in the circular buffer over time when vertical flip is enabled. In this example, PTR_S = 5 and PTR_E = 7. There can be up to PTR_E = 7 lines in the circular buffer.

Figure 8-176. ISS ISP RSZ and Circular Buffer Settings – Example 2



8.3.3.6 ISS ISP H3A Functional Description

8.3.3.6.1 ISS ISP H3A Overview

The H3A module supports the control loops for autofocus, auto white balance, and auto exposure by collecting metrics about the imaging/video data. The metrics are used to adjust parameters for processing the imaging/video data. There are two main blocks in the H3A module:

- Autofocus (AF) engine:

  The AF submodule extracts and filters the red, green, and blue data from input image data and provides the accumulation or peaks of the data in a specified region. The specified region is a 2D block of data referred to as a paxel. The AF engine supports the following features:

  – Peak mode in a paxel
    - Accumulation of the maximum focus value (FV) of each line in a paxel
  – Accumulation mode in a paxel
  – Accumulation of horizontal and vertical focus value in a paxel
  – Up to 12 paxels in the horizontal direction and up to 12 paxels in the vertical direction with vertical focus
  – Up to 36 paxels in the horizontal direction and up to 128 paxels in the vertical direction with horizontal focus only
  – Programmable width and height for the paxel/window
  – Programmable red, green, and blue position within a 2 × 2 matrix
  – Separate horizontal start for paxel and filtering

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  - Programmable vertical and horizontal line increments within a paxel
  - Horizontal FV uses parallel infinite impulse response (IIR) filters configured in a dual-biquad configuration with individual coefficients (two filters with 11 coefficients each). The filters are intended to compute the sharpness/peaks in the frame to focus on.
  - Vertical FV uses a 5-tap FIR filter with 8-bit coefficients. With horizontal steps each paxel has up to 32 columns to be maintained for vertical FV calculation.
- Auto exposure and auto white balance (AE/AWB) engine:

  The AE/AWB engine accumulates values and checks for saturated values in a subsampling of the video data. In the case of the AE/AWB, the 2D block of data is referred to as a window. Thus, other than having different names, paxels and windows are essentially the same. However, the numbers, dimensions, and starting positions of AF paxels and AE/AWB windows are programmable separately. AE/AWB supports the following features:
  - Accumulate clipped pixels along with all nonsaturated pixels in each window per color
  - Accumulate the sum of squared pixels in each window per color
  - Minimum and maximum pixel values in each window per color
  - Supports for up to 36 horizontal windows with sum + { sum_sq or min+max} output
  - Support for up to 56 horizontal windows with sum output
  - Support for up to 128 vertical windows
  - Programmable width and height for the windows. All windows in the frame are the same size.
  - Separate vertical start coordinate and height for a black row of paxels that is different than the remaining color paxels
  - Programmable horizontal sampling points in a window
  - Programmable vertical sampling points in a window
- Maximum pixel throughput of 200 MPix/s
- Double-buffer for paxel/window accumulation
- H3A data path is 10 bits.
- Maximum input size is 3008 pixels.

Figure 8-177 shows the H3A module connections to other submodules of the ISP.

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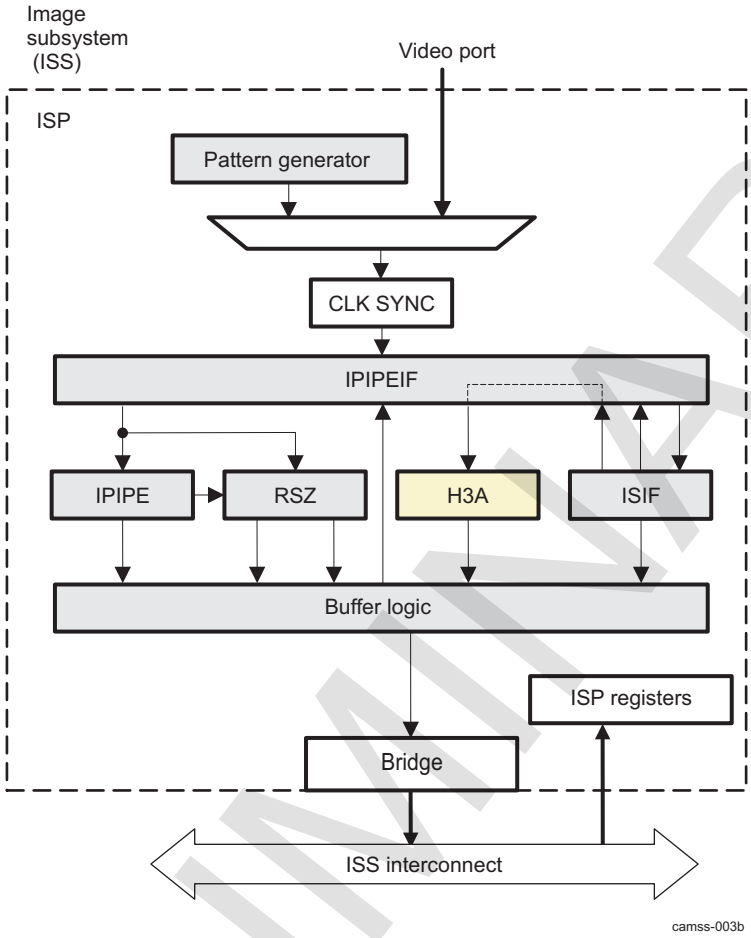
Figure 8-177. ISS ISP H3A High-Level Diagram



8.3.3.6.2 ISS ISP H3A Top-Level Block Diagram

The block diagram in Figure 8-178 shows the process of the AF and AE/AWB data paths through the H3A module.

The data flow before H3A is:

1. Data comes from the VP (VP) or BL.
2. The data is processed by the ISIF.
3. The data is processed by the IPIPEIF.
4. The data is 10 bits from the IPIPEIF at H3A input.

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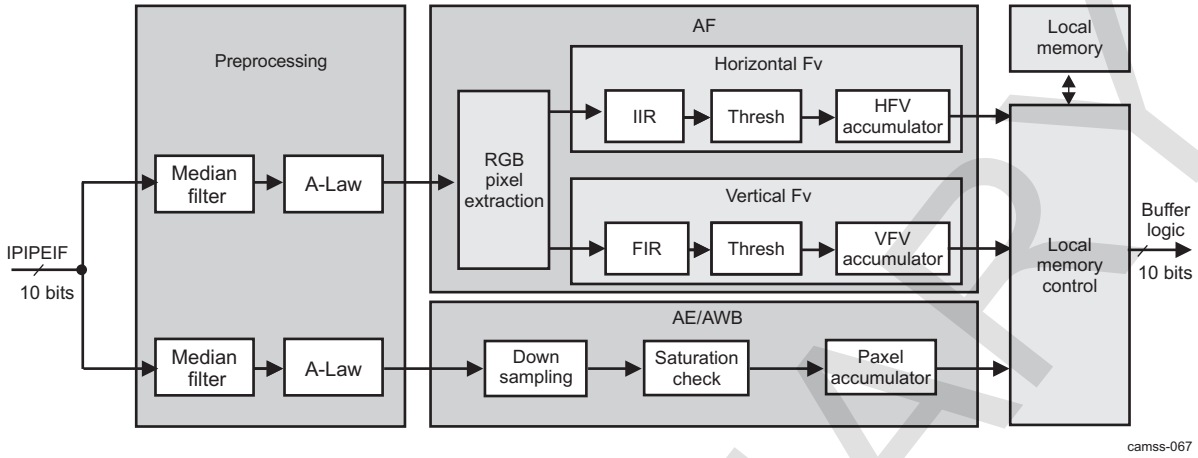
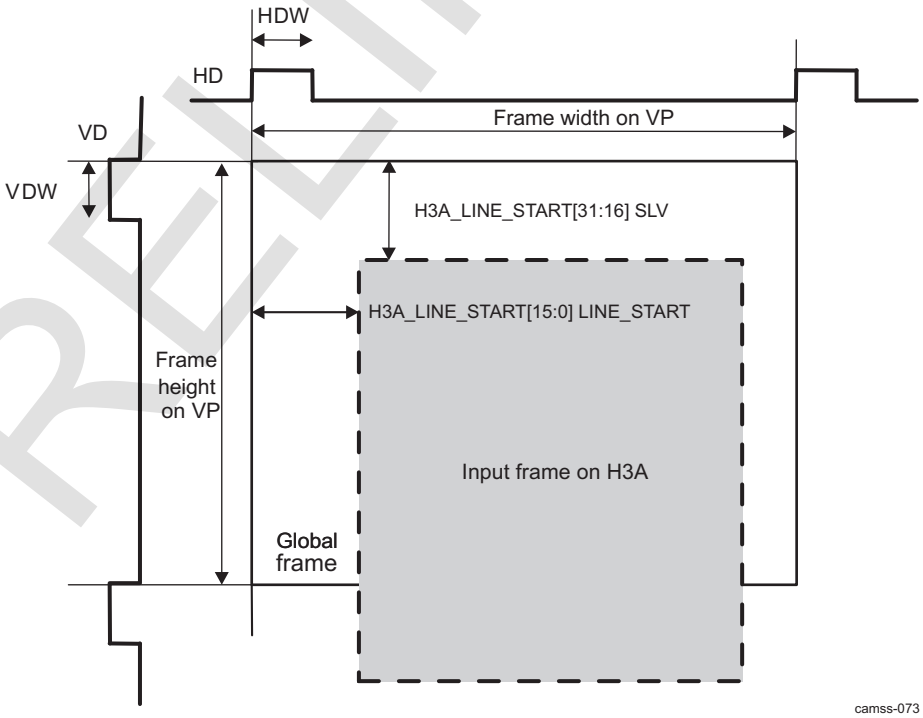
Figure 8-178. ISS ISP H3A Top-Level Block Diagram



8.3.3.6.3 ISS ISP H3A Line Framing Logic

In certain cases the number of clock cycles between HD pulses is greater than the line buffer included in the H3A. To solve this problem a framing module was added before the line buffer. The framing module uses the H3A_LINE_START register to find the position of the first pixel to place into the line buffer. All other registers reference this point as the 0 pixel for their start positions. The line size is 3008 pixels. After 3008 clock cycles the framing logic disables the line buffer and waits until the next HD. If the next HD comes before 3008 clock cycles, then the active region ends immediately and the counter waits for the H3A_LINE_START register count to be reached again. For the vertical position the H3A_LINE_START[31:16] SLV bit field can be used to determine where the start point of the frame is relative to the rising edge of VD. This logic allows for an active frame to cross VD boundaries and remain in the same frame.

Figure 8-179. ISS ISP H3A Frame Format Settings



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NOTE: (Frame width on VP) - (H3A_LINE_START[15:0] LINE_START) must be less than or equal to 3008, because the H3A memory lines are limited to 3008 pixels.

8.3.3.6.4 ISS ISP H3A Optional Preprocessing

The input to the H3A module is 10-bit RAW data from the IPIPEIF. A 10-bit to 8-bit A-Law compression step can be enabled and disabled separately for the AF engine (the H3A_PCR[1] AF_ALAW_EN bit) and the AE/AWB engine (the H3A_PCR[17] AEW_ALAW_EN bit). A-Law compression offers added protection against overflowing the accumulators.

If the A-Law table is enabled, the output is 10 bits, with the upper two bits filled with 0.

For the AF process, a horizontal median filter can be enabled and disabled (the H3A_PCR[2] AF_MED_EN bit) before A-Law compression. This filter is useful for reducing temperature-induced noise. The horizontal median filter calculates the absolute difference between the current pixel (i) and pixel (i – 2), and between the current pixel (i) and pixel (i + 2). If the absolute difference exceeds a threshold, and the sign of the differences is the same, the average of pixel (i – 2) and pixel (i + 2) replaces pixel (i). The threshold of the horizontal median filter can be set in the H3A_PCR[10:3] MED_TH bit field.

8.3.3.6.5 ISS ISP H3A Autofocus Engine

The AF engine works by extracting each green (Gr or Gb) pixel from the video stream and subtracts a fixed offset of 128 or 512 (depending of whether A-Law is enabled or disabled) from the pixel value. The offset value is then passed through an IIR filter and the absolute value of the filter output is the focus value (FV). Both FV and FV^2 are produced. The FV and FV^2 values can be accumulated or the maximum for each line/column can be accumulated. The following sections describe this process in more detail.

8.3.3.6.5.1 ISS ISP H3A Paxel Extraction

From the paxel starting coordinate (the H3A_AFPAXSTART[27:16] PAXSH and H3A_AFPAXSTART[11:0] PAXSV bit fields) specifies the starting point of the paxel grid, with respect to first pixel of th input image frame.

The paxel starting coordinate also indicates which color pixels are extracted if VF is enabled (that is, if H3A_PCR[20] AF_VF_EN = 1). Normally, either Gr or Gb is used for AF, but it is not important to the hardware whether it is red, green, or blue. If VF is not enabled, then the red, green, and blue pixel extraction is controlled by the H3A_PCR [13:11] RGBPOS bit field to extract the correct colors from the input stream. Figure 8-181 shows the available options for this bit field. The red and blue pixel positions are interchangeable. For each 2 × 2 grid, the green pixels are summed to create a single value. Because of this, the amplitude of the green output contains 2 pixels, while the red and blue outputs each contain 1 pixel.

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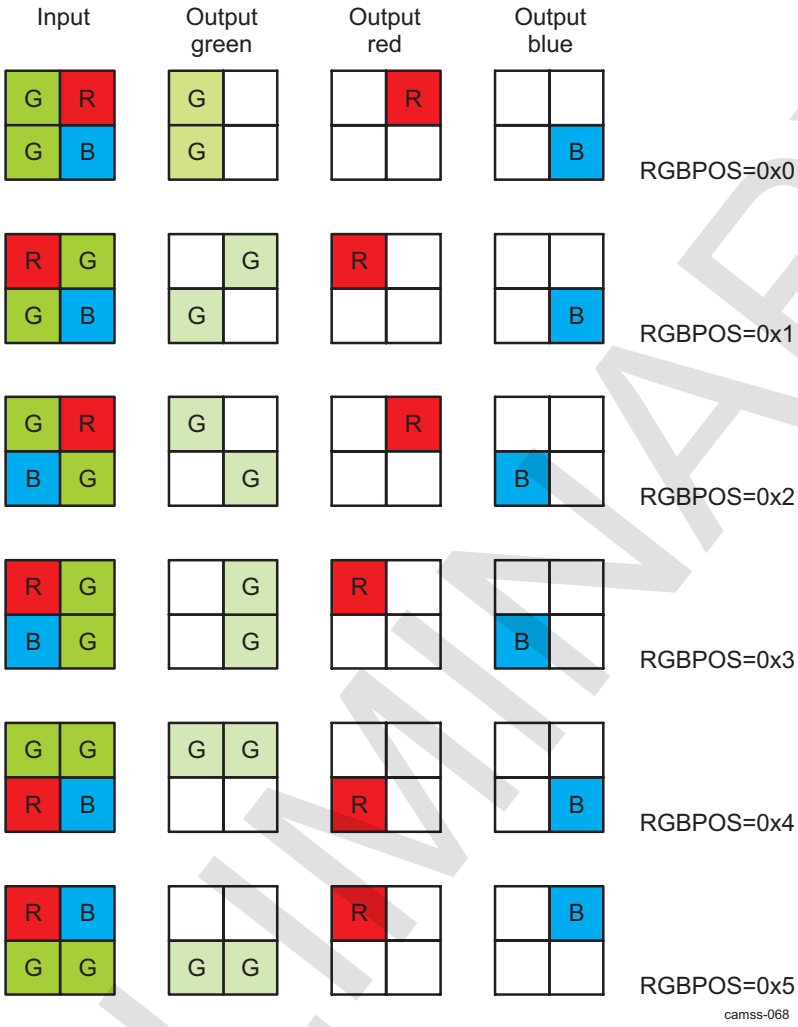
Figure 8-180. ISS ISP H3A Red, Green, and Blue Pixel Extraction Examples



Each paxel is H3A_AFPAX1[23:16] PAXW × H3A_AFPAX1[7:0] PAXH (width × height) pixels. Inside each paxel, horizontal FV can skip lines, operating on one every H3A_AFPAX2[16:13] AFINCV lines. Vertical FV can skip columns, operating on one every H3A_AFPAX2[20:17] AFINCH columns. Up to 32 columns are supported for each paxel. If floor (PAXW/AFINCH) = 32, only the first 32 designated columns are operated on. Because PAXW, PAXH, AFINCV, and AFINCH are all even numbers, AF always operates on the same green color, Gr or Gb. IIR filters for the horizontal FVs start operation at column H3A_AFIIRSH[11:0] IIRSH.

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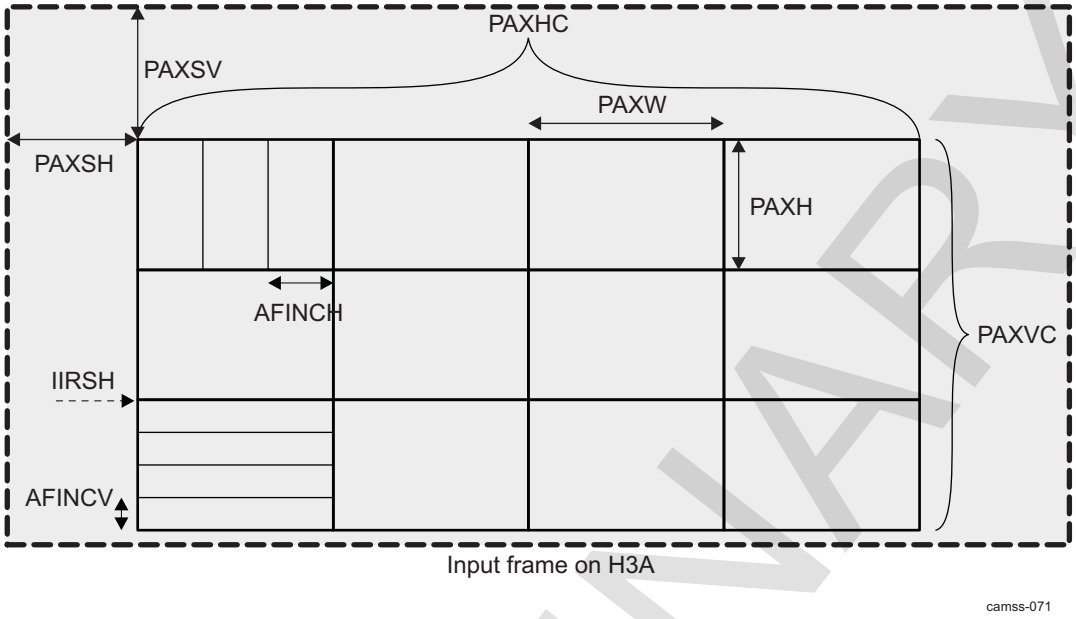
Figure 8-181. ISS ISP H3A Horizontal/Vertical FV Paxel Configuration



NOTE: (H3A_AFPAXSTART [27:16] PAXSH) + (H3A_AFPAX2 [5:0] PAXHC) × (H3A_AFPAX1[23:16] PAXW) = [(Frame width on VP) – (H3A_LINE_START[15:0] LINE_START)] = 3008

Table 8-328 lists the register fields that configure the size and number of paxels.

Table 8-328. ISS ISP H3A Paxel Register Field Descriptions

Register Field	Bit Width	Description
H3A_AFPAX1[23:16] PAXW	8	Paxel width (in pixels)
H3A_AFPAX1[7:0] PAXH	8	Paxel height (in lines)
H3A_AFPAX2[5:0] PAXHC	6	Paxel count for horizontal direction
H3A_AFPAX2[12:6] PAXVC	7	Paxel count for vertical direction
H3A_AFPAX2[16:13] AFINCV	4	Line increments in a paxel
H3A_AFPAX2[20:17] AFINCH	4	Column increments in a paxel
H3A_AFPAXSTART[27:16] PAXSH	12	Paxel start position H
H3A_AFPAXSTART[11:0] PAXSV	12	Paxel start position V
H3A_AFIIRSH[11:0] IIRSH	12	IIR filter start position

The H3A AF engine also has an option for an advanced or normal stats collection mode. When 0xCA00 is written to the H3A_ADVANCED[31:15] ID bit field, then H3A_ADVANCED[0] AF_MODE can be used to toggle between normal and advanced AF stats collection mode. When the advanced AF stats collection mode is enabled, the ZEROS section of the AF paxel packet is filled with the sum of the maximum FVs, regardless of the color, from HFV_1 and HFV_2.

8.3.3.6.5.2 ISS ISP H3A Horizontal FV Calculator

The FV calculator takes the unsigned red/green/blue extracted data and subtracts 128 or 512 (depending on whether A-Law is enabled) to place the data in the range [–128:127] or [–512:511].

After removing the offset, the data is sent through two parallel IIR filters configured in a dual-biquad configuration. Each filter uses a unique set of 11 programmable coefficients. Each coefficient is 12-bits-wide with 6 bits of decimal, S12Q6 (H3A_AFCOEF010 to H3A_AFCOEF0010 for SET0, and H3A_AFCOEF110 to H3A_AFCOEF1010 for SET1). The filter-shift registers are cleared on each

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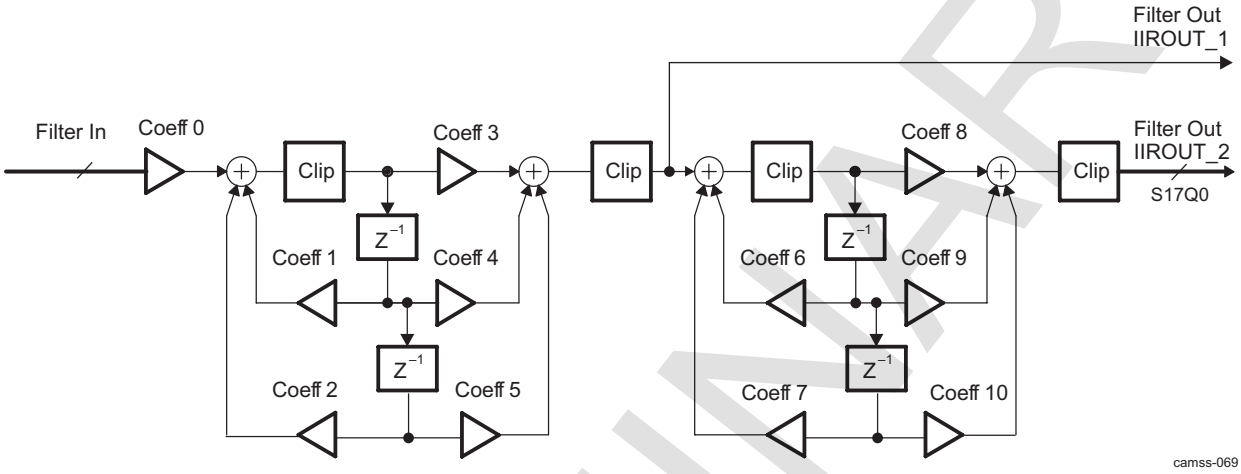
horizontal line at the position set by the register IIR horizontal start register (the H3A_AFIIRSH [11:0] IIRSH bit field). The absolute values of the output (16-bits-wide with 4 bits of decimal, U16Q4) of both filters are then sent to the AF accumulator module. Signed clipping is performed during the FV calculation. If the input value is m bits (signed) and the required output value is n bits, clipping transforms the input to between -2^1 and 2^1. Values lower than -2^1 are set to -2^1, and values higher than 2^1 are set to 2^1.

Figure 8-182 shows the IIR filter model.

Figure 8-182. ISS ISP H3A IIR Filter Model



8.3.3.6.5.3 ISS ISP H3A HFV Accumulator

The horizontal focus value (HFV) accumulator takes the output of the horizontal IIR filter and accumulates values for each paxel. The size and number of paxels is configurable by registers.

Table 8-328 lists the register fields that configure the size and number of paxels:

- In peak mode (H3A_PCR[14] FVMODE = 0x1), the maximum value is accumulated.
- In sum mode (H3A_PCR[14] FVMODE = 0x0), all HFV_n are accumulated in a paxel.

The following equations detail the calculation for:

- Sum of pixel values used in HFV: The pixel values that are used for filtering and accumulation of HFV are also accumulated in this sum of pixel values.
- HFV_n (HFV_n_peak for peak mode or HFV_n_sum for sum mode)
- HFV_count_n
- HFV_sq_n (HFV_sq_n_peak for peak mode or HFV_sq_n_sum for sum mode)

n = 1 or 2 for IIR1 and IIR2, respectively.

For each paxel, these six values are available for each R, G, and B component.

```
for (k=0; k PAXH) // Loop on paxel rows
{
 rowpeak_n = 0;
 for (l=0; lPAXW; l++) // Loop on values within a row
 {
 aIIRout_n = ABS(IIRout_n);
 if (aIIRout_n = threshold_n)
 {
 hfval = aIIRout_n - threshold_n;
 HFV_count_n++;
 }
 else hfval = 0;
 if (hfval  rowpeak_n)
 {
 rowpeak_n = HFV_n;
 }
```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```
 HFV_n_sum += hfval;
 HFV_sq_n_sum += (hfval* hfval + RNDADD)  RNDSHIFT;
 } // Finished looping on values in a row
 HFV_n_peak += rowpeak_n;
 HFV_sq_n_peak += (rowpeak_n * rowpeak_n + RNDADD)  RNDSHIFT;
}
```

- threshold_n is H3A_HVF_THR[15:0] HTHR1and H3A_HVF_THR[31:16] HTHR2, respectively.
- IIRout_n is the IIRout_1 and IIRout_2 outputs, respectively.
- HFV_count_n and HFV_sq_n are not sent to the DMA interface if VF is disabled.
- RNDADD and RNDSHIFT depend on whether input pixels are 8-bit or 10-bit, and achieves rounding. This is automatically performed by the module.
- If VF is enabled, only the green color channel values are output to the DMA interface.
- In sum mode:
  - HFV_n = HFV_n_sum
  - HFV_sq_n = HFV_sq_n_sum
- In peak mode:
  - HFV_n = HFV_n_peak
  - HFV_sq_n = HFV_sq_n_peak

8.3.3.6.5.4 ISS ISP H3A VFV Calculator

The VFV calculator takes the unsigned extracted data through two FIR filters, each with a set of five coefficients (VCOEF1_x, where x = 0..4, in the H3A_VFV_CFG1 and H3A_VFV_CFG2 registers for FIR 1, and VCOEF2_x, where x = 0..4, in H3A_VFV_CFG3 and H3A_VFV_CFG4 registers). Each coefficient is 8 bits wide with 4 bits of decimal (S8Q4). The filter outcome is downshifted by 4 bits and taken absolute value to produce a 16-bit unsigned value. This is then sent to threshold H3A_VFV_CFG2[31:16] VTHR1 for FIR 1, and H3A_VFV_CFG4[31:16] VTHR2 for FIR 2, and square logic to produce VFV_n and VFV_sq_n.

8.3.3.6.5.5 ISS ISP H3A VFV Accumulator

The VFV accumulator takes the output of the vertical FIR filters and accumulates values for each paxel. The size and number of paxels is configurable by registers.

Table 8-328 lists the register fields that configure the size and number of paxels.

The following equations detail the calculation for:

- VFV_n
- VFV_count_n
- VFV_sq_n

n = 1 or 2 for FIR1 and FIR2, respectively.

For each paxel, these six values are available for each R, G, and B component.

```
FIR_coef_n = [VCOEFn_0, VCOEFn_1, VCOEFn_2, VCOEFn_3, VCOEFn_4]; /* coefficient values in S8.4
format */
aFIRout_n = (ABS(inner_product(extracted_G, FIR_coef_n)) + 8)  4;
if (aFIRout_n = threshold_n)
{
 VFV_n = aFIRout_n - threshold_n
 VFV_count_n++;
}
else VFV_n = 0;
VFV_sq_n = (VFV_n * VFV_n + RNDADD)  RNDSHIFT;
```

- threshold_n is H3A_VFV_CFG2[31:16] VTHR1 and H3A_VFV_CFG4[31:16] VTHR2, respectively.
- FIRout_n is the FIRout_1 and FIRout_2 outputs, respectively.
- RNDADD and RNDSHIFT depend on whether the input pixels are 8-bit or 10-bit, and achieves rounding. This is automatically performed by the module.

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8.3.3.6.6 ISS ISP H3A AE/AWB Engine

The AE/AWB engine starts by dividing the frames into windows, and then subsamples each window into 2 × 2 blocks. For each subsampled 2 × 2 block, each pixel is accumulated. Also, each pixel is compared to a limit set in a register. If any pixels in a 2 × 2 block are greater than or equal to the limit, the block is not counted in the unsaturated block counter. Pixels greater than the limit are replaced by the limit, and the value of the pixel is accumulated.

The AE/AWB module has three output format modes, which are set through the H3A_AEWCFG[9:8] AEFMT bit field:

- Sum of square mode: H3A_AEWCFG[9:8] AEFMT = 0x0
- Min/max mode: H3A_AEWCFG[9:8] AEFMT = 0x1
- Sum-only mode: H3A_AEWCFG[9:8] AEFMT = 0x2

8.3.3.6.6.1 ISS ISP H3A Subsampler

The subsampler partitions the frame into windows using the size, count, and starting location parameters shown on the left in Figure 8-179. Each window is further sampled down to a set of 2 × 2 blocks. The horizontal and vertical distances between the start of blocks within a window is programmable using the parameters shown on the right in Figure 8-179.

Figure 8-183. ISS ISP H3A AE/AWB Window Configurations

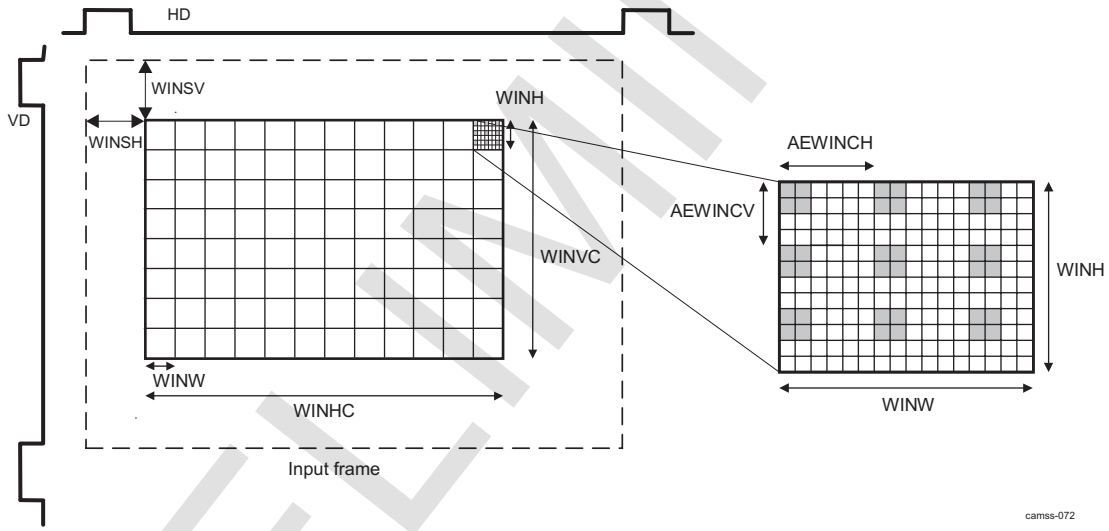

Table 8-329 lists the register fields that configure the window and block sizes, counts, and starting positions.

Table 8-329. ISS ISP H3A AE/AWB Window Register Field Descriptions

Register Field	Bit Width	Description
H3A_AEWWIN1[20:13] WINW	7	Window width (in pixels)
H3A_AEWWIN1[31:24] WINH	7	Window height (in lines)
H3A_AEWWIN1[5:0] WINHC	6	Window count for horizontal direction
H3A_AEWWIN1[12:6] WINVC	7	Window count for vertical direction
H3A_AEWINSTART[11:0] WINSH	12	Window start position H
H3A_AEWINSTART[27:16] WINSV	12	Window start position V
H3A_AEWSUBWIN[3:0] AEWINCH	4	Horizontal distance between subsamples
H3A_AEWSUBWIN[11:8] AEWINCV	4	Vertical distance between subsamples

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8.3.3.6.6.2 ISS ISP H3A Additional Black Row of AE/AWB Windows

In addition to the 128 rows of windows, the AE/AWB module provides support for an additional row of windows for black data. This data may be useful in determining the DC offset noise of the rest of the data. The black row of windows can be before or after the regular rows of windows. The vertical start line for the black row of windows is specified in the H3A_AEWINBLK[27:16] WINSV bit field, and the height is specified in the H3A_AEWINBLK[6:0] WINH bit field. The horizontal starting pixel and horizontal width of the black row of windows are the same as for the regular rows of windows.

Figure 8-184 shows a black row of windows before rows of windows.

Figure 8-184. ISS ISP H3A Black Row of Windows Before Regular Rows of Windows

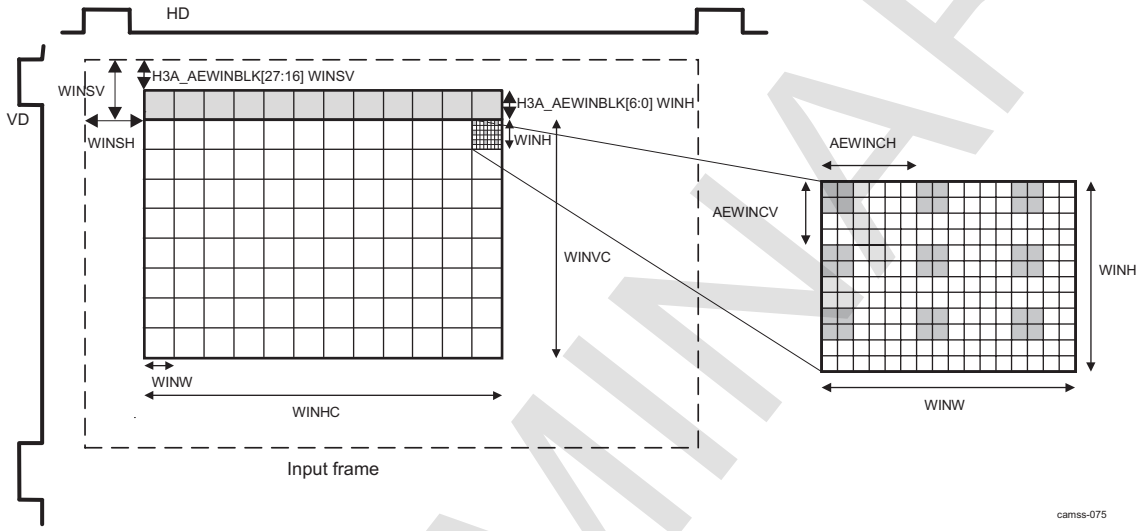

Table 8-330. ISS ISP H3A AE/AWB Window with Additional Black Row Register Field Descriptions

Register Field	Bit Width	Description
H3A_AEWWIN1[20:13] WINW	7	Window width (in pixels)
H3A_AEWWIN1[31:24] WINH	7	Window height (in lines)
H3A_AEWWIN1[5:0] WINHC	6	Window count for horizontal direction
H3A_AEWWIN1[12:6] WINVC	7	Window count for vertical direction
H3A_AEWINSTART[11:0] WINSH	12	Window start position H
H3A_AEWINSTART[27:16] WINSV	12	Window start position V
H3A_AEWSUBWIN[3:0] AEWINCH	4	Horizontal distance between subsamples
H3A_AEWSUBWIN[11:8] AEWINCV	4	Vertical distance between subsamples
H3A_AEWINBLK[27:16] WINSV	12	Window start position H for single black line
H3A_AEWINBLK[6:0] WINH	7	Window height (in lines) for single black line

8.3.3.6.6.3 ISS ISP H3A Saturation Check

The saturation check module compares the data from the subsampler to the value programmed in the H3A_PCR [31:22] AVE2LMT bit field. This value is the maximum clipping value. If all 4 pixels in the 2 × 2 block are less than the AVE2LMT value, the value of the unsaturated block counter is incremented. There is one unsaturated block counter per window. The unsaturated block counters are later written to memory.

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8.3.3.6.6.4 ISS ISP H3A AE/AWB Accumulators

The output from the saturation check module and the subsampler module are separately accumulated for each pixel in every 2 × 2 pixel block for each window. Therefore, there are eight accumulators per window (one accumulator for each pixel in a 2 × 2 pixel block, times two sets of accumulators: clipped/saturated data and presaturated data). Each of the 4 pixels in the 2 × 2 pixel grid is associated with a color (R, Gr, B, Gb); however, the output of these accumulators is referenced by position in the grid, not color.

The accumulators are 16 bits wide, and the accumulated data is 10 bits wide. Therefore, when a window contains more than 64 pixels of the same color, an overflow risk exists. This risk can be reduced by enabling the A-Law conversion in the preprocessing stage. See Section 8.3.3.6.4 for details.

The AE/AWB module has a shift value for the accumulation of pixel values that is set in the H3A_AEWCFG[3:0] SUMSHFT bit field.

8.3.3.6.7 ISS ISP H3A DMA Interface

The DMA interface module takes the data from the AF engine and AE/AWB engine and builds packets to be sent out to the memory through the BL module.

The data interface has separate start pointers for the AF and AE/AWB engines.

- The starting address for the AF engine is the H3A_AFBUFST[31:5] AFBUFST bit field.
- The starting address for the AE/AWB engine is the H3A_AEWBUFST[31:5] AEWBUFST bit field.

The DMA interface module continuously loops through this data as it builds the packets. To optimize the transfer sizes, the DMA interface sends out an AF or AE transfer for each row of paxels or windows. This requires that each horizontal row of paxels or windows starts and ends on a 32-byte boundary. If a horizontal row of paxels or windows ends on a non-32 byte boundary, the hardware packs zeroes. The counts for the AEW that occur every eight windows is sent in the row with the 8th consecutive window.

Table 8-331 lists the packet formats for AF with vertical AF disabled.

Table 8-331. ISS ISP H3A AF Packet Format With Vertical AF Disabled

Buffer Start Address (Byte Address) H3A_AFBUFST	31 16	15 0
	Sum of pixel values used in HFV	(Paxel 0)
	HFV_1 (peak or sum)	(Paxel 0)
	HFV_2 (peak or sum)	(Paxel 0)
	ZEROES	(Paxel 0)
	Sum of pixel values used in HFV	(Paxel 0)
	HFV_1 (peak or sum)	(Paxel 0)
	HFV_2 (peak or sum)	(Paxel 0)
	ZEROES	(Paxel 0)
	Sum of pixel values used in HFV	(Paxel 0)
	HFV_1 (peak or sum)	(Paxel 0)
	HFV_2 (peak or sum)	(Paxel 0)
	ZEROES	(Paxel 0)
	Sum of pixel values used in HFV	(Paxel 1)
	HFV_1 (peak or sum)	(Paxel 1)
	HFV_2 (peak or sum)	(Paxel 1)
	ZEROES	(Paxel 1)
	...	

Table 8-332 shows the packet formats for AF with vertical AF enabled.

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Table 8-332. ISS ISP H3A AF Packet Format With Vertical AF Enabled

Buffer Start Address (Byte Address) H3A_AFBUFST	31 16	15 0
	Sum of pixel values used in HFV	(Paxel 0)
	HFV_1 (peak or sum)	(Paxel 0)
	HFV_sq_1 (peak or sum)	(Paxel 0)
	HFV_count_1	(Paxel 0)
	HFV_2 (peak or sum)	(Paxel 0)
	HFV_sq_2 (peak or sum)	(Paxel 0)
	HFV_count_2	(Paxel 0)
	ZEROES	(Paxel 0)
	VFV_1	(Paxel 0)
	VFV_sq_1	(Paxel 0)
	VFV_count_1	(Paxel 0)
	ZEROES	(Paxel 0)
	VFV_2	(Paxel 0)
	VFV_sq_2	(Paxel 0)
	VFV_count_2	(Paxel 0)
	ZEROES	(Paxel 0)
	Sum of pixel values used in HFV	(Paxel 1)
	HFV_1 (peak or sum)	(Paxel 1)
	HFV_sq_1 (peak or sum)	(Paxel 1)
	HFV_count_1	(Paxel 1)
	...	

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Figure 8-185 shows the windows and subsample definition used in tables.

Figure 8-185. ISS ISP H3A AE/AWB Window and Subsample Definition

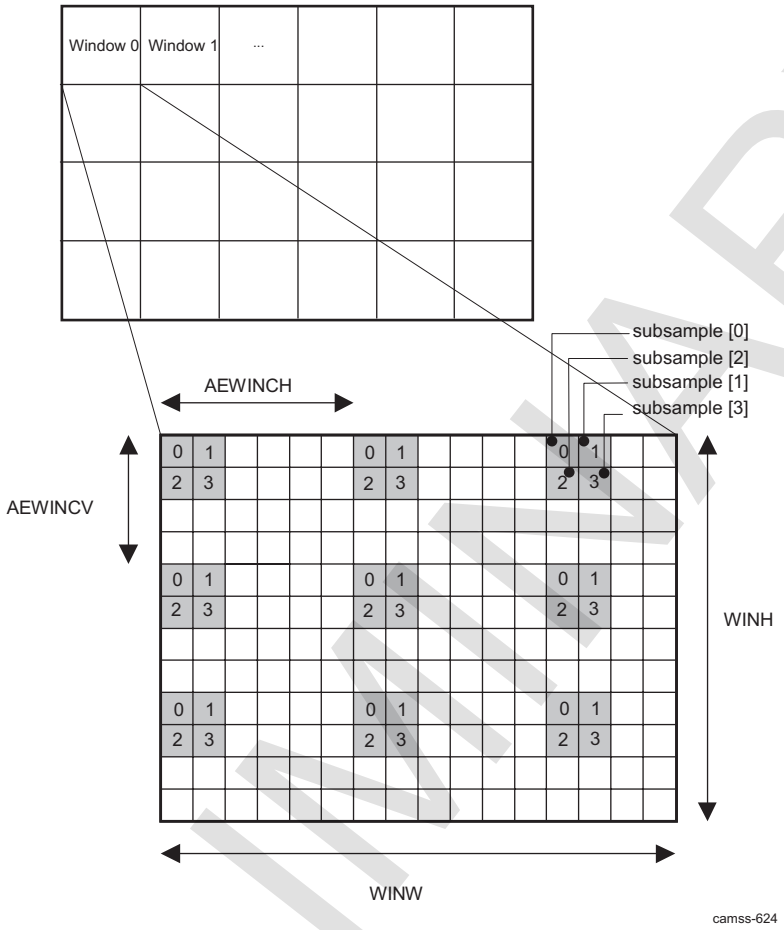

Table 8-333 lists the packet formats for AE/AWB for sum of square mode (H3A_AEWCFG[9:8] AEFMT = 0x0) .

Table 8-333. ISS ISP H3A AE/AWB Packet Format for Sum of Square Mode

	31 16	15 0	
Buffer address (byte address) H3A_AEWBUFST	Subsample Accum[1]	Subsample Accum[0]	Window 0 data
	Subsample Accum[3]	Subsample Accum[2]	
	Saturator Accum[1]	Saturator Accum[0]	
	Saturator Accum [3]	Saturator Accum[2]	
	Sum of squares[0]		
	Sum of squares[1]		
	Sum of squares[2]		
	Sum of squares[3]		
H3A_AEWBUFST + 32 bytes	Subsample Accum[1]	Subsample Accum[0]	Window 1 data
	Subsample Accum[3]	Subsample Accum[2]	
	Saturator Accum[1]	Saturator Accum[0]	
	Saturator Accum [3]	Saturator Accum[2]	

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Table 8-333. ISS ISP H3A AE/AWB Packet Format for Sum of Square Mode (continued)

	31 16	15 0	
	Sum of squares[0]		
	Sum of squares[1]		
	Sum of squares[2]		
	Sum of squares[3]		
H3A_AEWBUFST + 64 bytes	Subsample Accum[1]	Subsample Accum[0]	Window 2 data
	Subsample Accum[3]	Subsample Accum[2]	
	Saturator Accum[1]	Saturator Accum[0]	
	Saturator Accum [3]	Saturator Accum[2]	
	Sum of squares[0]		
	Sum of squares[1]		
	Sum of squares[2]		
	Sum of squares[3]		
H3A_AEWBUFST + 96 bytes	Subsample Accum[1]	Subsample Accum[0]	Window 3 data
	Subsample Accum[3]	Subsample Accum[2]	
	Saturator Accum[1]	Saturator Accum[0]	
	Saturator Accum [3]	Saturator Accum[2]	
	Sum of squares[0]		
	Sum of squares[1]		
	Sum of squares[2]		
	Sum of squares[3]		
H3A_AEWBUFST + 128 bytes	Subsample Accum[1]	Subsample Accum[0]	Window 4 data
	Subsample Accum[3]	Subsample Accum[2]	
	Saturator Accum[1]	Saturator Accum[0]	
	Saturator Accum [3]	Saturator Accum[2]	
	Sum of squares[0]		
	Sum of squares[1]		
	Sum of squares[2]		
	Sum of squares[3]		
H3A_AEWBUFST + 160 bytes	Subsample Accum[1]	Subsample Accum[0]	Window 5 data
	Subsample Accum[3]	Subsample Accum[2]	
	Saturator Accum[1]	Saturator Accum[0]	
	Saturator Accum [3]	Saturator Accum[2]	
	Sum of squares[0]		
	Sum of squares[1]		
	Sum of squares[2]		
	Sum of squares[3]		
H3A_AEWBUFST + 192 bytes	Subsample Accum[1]	Subsample Accum[0]	Window 6 data
	Subsample Accum[3]	Subsample Accum[2]	
	Saturator Accum[1]	Saturator Accum[0]	
	Saturator Accum [3]	Saturator Accum[2]	
	Sum of squares[0]		
	Sum of squares[1]		
	Sum of squares[2]		
	Sum of squares[3]		

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Table 8-333. ISS ISP H3A AE/AWB Packet Format for Sum of Square Mode (continued)

	31 16	15 0	
H3A_AEWBUFST + 224 bytes	Subsample Accum[1]	Subsample Accum[0]	Window 7 data
	Subsample Accum[3]	Subsample Accum[2]	
	Saturator Accum[1]	Saturator Accum[0]	
	Saturator Accum [3]	Saturator Accum[2]	
	Sum of squares[0]		
	Sum of squares[1]		
	Sum of squares[2]		
	Sum of squares[3]		
H3A_AEWBUFST + 256 bytes	Unsaturated count, win 1	Unsaturated count, win 0	Unsaturated block count for the above 8 windows
	Unsaturated count, win 3	Unsaturated count, win 2	
	Unsaturated count, win 5	Unsaturated count, win 4	
	Unsaturated count, win 7	Unsaturated count, win 6	
	Data for next eight windows, and so on. If the total number of windows is not a multiple of 8, the unsaturated counters are written immediately following the last window data. For example, if the total number of windows (including the black row) are 43, the first 40 windows are written out as per the 272-byte boundary above. Then the remaining three windows are written at +0, +32, and +64 bytes. The counts are written out at +96 instead of +256-byte boundary.		

Table 8-334 lists the packet formats for AE/AWB in minimum-maximum mode (H3A_AEWCFG[9:8] AEFMT = 0x1).

Table 8-334. ISS ISP H3A AE/AWB Packet Format for Minimum-Maximum Mode

	31 16	15 0	
Buffer address (byte address) H3A_AEWBUFST	Subsample Accum[1]	Subsample Accum[0]	Window 0 data
	Subsample Accum[3]	Subsample Accum[2]	
	Saturator Accum[1]	Saturator Accum[0]	
	Saturator Accum [3]	Saturator Accum[2]	
	Minimum[1]	Minimum[0]	
	Minimum[3]	Minimum[2]	
	Maximum[1]	Maximum[0]	
	Maximum[3]	Maximum[2]	
H3A_AEWBUFST + 32 bytes	Subsample Accum[1]	Subsample Accum[0]	Window 1 data
	Subsample Accum[3]	Subsample Accum[2]	
	Saturator Accum[1]	Saturator Accum[0]	
	Saturator Accum [3]	Saturator Accum[2]	
	Minimum[1]	Minimum[0]	
	Minimum[3]	Minimum[2]	
	Maximum[1]	Maximum[0]	
	Maximum[3]	Maximum[2]	
H3A_AEWBUFST + 64 bytes	Subsample Accum[1]	Subsample Accum[0]	Window 2 data

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Table 8-334. ISS ISP H3A AE/AWB Packet Format for Minimum-Maximum Mode (continued)

	31 16	15 0	
	Subsample Accum[3]	Subsample Accum[2]	
	Saturator Accum[1]	Saturator Accum[0]	
	Saturator Accum [3]	Saturator Accum[2]	
	Minimum[1]	Minimum[0]	
	Minimum[3]	Minimum[2]	
	Maximum[1]	Maximum[0]	
	Maximum[3]	Maximum[2]	
H3A_AEWBUFST + 96 bytes	Subsample Accum[1]	Subsample Accum[0]	Window 3 data
	Subsample Accum[3]	Subsample Accum[2]	
	Saturator Accum[1]	Saturator Accum[0]	
	Saturator Accum [3]	Saturator Accum[2]	
	Minimum[1]	Minimum[0]	
	Minimum[3]	Minimum[2]	
	Maximum[1]	Maximum[0]	
	Maximum[3]	Maximum[2]	
H3A_AEWBUFST + 128 bytes	Subsample Accum[1]	Subsample Accum[0]	Window 4 data
	Subsample Accum[3]	Subsample Accum[2]	
	Saturator Accum[1]	Saturator Accum[0]	
	Saturator Accum [3]	Saturator Accum[2]	
	Minimum[1]	Minimum[0]	
	Minimum[3]	Minimum[2]	
	Maximum[1]	Maximum[0]	
	Maximum[3]	Maximum[2]	
H3A_AEWBUFST + 160 bytes	Subsample Accum[1]	Subsample Accum[0]	Window 5 data
	Subsample Accum[3]	Subsample Accum[2]	
	Saturator Accum[1]	Saturator Accum[0]	
	Saturator Accum [3]	Saturator Accum[2]	
	Minimum[1]	Minimum[0]	
	Minimum[3]	Minimum[2]	
	Maximum[1]	Maximum[0]	
	Maximum[3]	Maximum[2]	
H3A_AEWBUFST + 192 bytes	Subsample Accum[1]	Subsample Accum[0]	Window 6 data
	Subsample Accum[3]	Subsample Accum[2]	
	Saturator Accum[1]	Saturator Accum[0]	
	Saturator Accum [3]	Saturator Accum[2]	
	Minimum[1]	Minimum[0]	
	Minimum[3]	Minimum[2]	
	Maximum[1]	Maximum[0]	
	Maximum[3]	Maximum[2]	
H3A_AEWBUFST + 224 bytes	Subsample Accum[1]	Subsample Accum[0]	Window 7 data
	Subsample Accum[3]	Subsample Accum[2]	
	Saturator Accum[1]	Saturator Accum[0]	
	Saturator Accum [3]	Saturator Accum[2]	
	Minimum[1]	Minimum[0]	

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Table 8-334. ISS ISP H3A AE/AWB Packet Format for Minimum-Maximum Mode (continued)

	31 16	15 0	
	Minimum[3]	Minimum[2]	
	Maximum[1]	Maximum[0]	
	Maximum[3]	Maximum[2]	
H3A_AEWBUFST + 256 bytes	Unsaturated count, win 1	Unsaturated count, win 0	Unsaturated block count for the above 8 windows
	Unsaturated count, win 3	Unsaturated count, win 2	
	Unsaturated count, win 5	Unsaturated count, win 4	
	Unsaturated count, win 7	Unsaturated count, win 6	
	Data for next eight windows, and so on. If the total number of windows is not a multiple of 8, the unsaturated counters are written immediately following the last window data. For example, if the total number of windows (including the black row) are 43, the first 40 windows are written out as per the 272-byte boundary above. Then the remaining three windows are written at +0, +32, and +64 bytes. The counts are written out at +96 instead of +256-byte boundary.		

Table 8-335 lists the packet formats for AE/AWB in sum-only mode (H3A_AEWCFG[9:8] AEFMT = 0x2).

Table 8-335. ISS ISP H3A AE/AWB Packet Format for Sum-Only Mode

	31 16	15 0	
Buffer address (byte address) H3A_AEWBUFST	Subsample Accum[1]	Subsample Accum[0]	Window 0 data
	Subsample Accum[3]	Subsample Accum[2]	
	Saturator Accum[1]	Saturator Accum[0]	
	Saturator Accum [3]	Saturator Accum[2]	
H3A_AEWBUFST + 32 bytes	Subsample Accum[1]	Subsample Accum[0]	Window 1 data
	Subsample Accum[3]	Subsample Accum[2]	
	Saturator Accum[1]	Saturator Accum[0]	
	Saturator Accum [3]	Saturator Accum[2]	
H3A_AEWBUFST + 64 bytes	Subsample Accum[1]	Subsample Accum[0]	Window 2 data
	Subsample Accum[3]	Subsample Accum[2]	
	Saturator Accum[1]	Saturator Accum[0]	
	Saturator Accum [3]	Saturator Accum[2]	
H3A_AEWBUFST + 96 bytes	Subsample Accum[1]	Subsample Accum[0]	Window 3 data
	Subsample Accum[3]	Subsample Accum[2]	
	Saturator Accum[1]	Saturator Accum[0]	
	Saturator Accum [3]	Saturator Accum[2]	
H3A_AEWBUFST + 128 bytes	Subsample Accum[1]	Subsample Accum[0]	Window 4 data
	Subsample Accum[3]	Subsample Accum[2]	
	Saturator Accum[1]	Saturator Accum[0]	
	Saturator Accum [3]	Saturator Accum[2]	

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Table 8-335. ISS ISP H3A AE/AWB Packet Format for Sum-Only Mode (continued)

	31 16	15 0	
H3A_AEWBUFST + 160 bytes	Subsample Accum[1]	Subsample Accum[0]	Window 5 data
	Subsample Accum[3]	Subsample Accum[2]	
	Saturator Accum[1]	Saturator Accum[0]	
	Saturator Accum [3]	Saturator Accum[2]	
H3A_AEWBUFST + 192 bytes	Subsample Accum[1]	Subsample Accum[0]	Window 6 data
	Subsample Accum[3]	Subsample Accum[2]	
	Saturator Accum[1]	Saturator Accum[0]	
	Saturator Accum [3]	Saturator Accum[2]	
H3A_AEWBUFST + 224 bytes	Subsample Accum[1]	Subsample Accum[0]	Window 7 data
	Subsample Accum[3]	Subsample Accum[2]	
	Saturator Accum[1]	Saturator Accum[0]	
	Saturator Accum [3]	Saturator Accum[2]	
H3A_AEWBUFST + 256 bytes	Unsaturated count, win 1	Unsaturated count, win 0	Unsaturated block count for the above 8 windows
	Unsaturated count, win 3	Unsaturated count, win 2	
	Unsaturated count, win 5	Unsaturated count, win 4	
	Unsaturated count, win 7	Unsaturated count, win 6	
	Data for next eight windows, and so on. If the total number of windows is not a multiple of 8, the unsaturated counters are written immediately following the last window data. For example, if the total number of windows (including black row) are 43, the first 40 windows are written out as per the 272-byte boundary above. Then the remaining three windows are written at +0, +32, and +64 bytes. The counts are written out at +96 instead of +256-byte boundary.		

8.3.3.6.8 ISS ISP H3A Events and Status Checking

The AF and AEW engines generate an interrupt event at the end of processing each frame. However, these two interrupts are internally tied together so that only one H3A interrupt signal is generated. If the AF engine and AEW engine do not process the same frame concurrently, this should not be an issue. However, if they do run concurrently, one of two outcomes may occur:

- The H3A interrupt may seem to trigger only once for each frame. This can happen when the processing for the AF and AEW engines finishes at or near the same time. The interrupt service routine does not have enough time to clear the interrupt flag for the first interrupt before the second interrupt occurs.
- The H3A interrupt may trigger twice for each frame. This can happen when the AF engine or the AEW engine finishes processing the frame much earlier than the other engine. In this case, the interrupt service routine does have enough time to clear the interrupt flag for the first interrupt by the time the second interrupt occurs.

The outcome depends on the difference in location of the last paxel/window in the frame (determines when processing is finished), the frequency of the relative clocks in the system, the occurrence and triggering of other interrupts in the system, and the latencies of the context switching and interrupt service routine execution.

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The H3A_PCR[15] BUSYAF and/or H3A_PCR[18] BUSYAEAWB status bits are set when the start of frame occurs (if the H3A_PCR[0] AF_EN and/or H3A_PCR[16] AEW_EN bits are 1 at that time). They are automatically reset to 0 at the end of processing a frame. The H3A_PCR[15] BUSYAF and/or H3A_PCR[18] BUSYAEAWB status bits may be polled to determine the end of frame status.

8.3.3.7 ISS ISP ISIF Functional Description

8.3.3.7.1 ISS ISP ISIF Overview

The image sensor interface (ISIF) module receives RAW or YUV4:2:2 data from the IPIPEIF module. The module outputs data back to the IPIPEIF module and can also output data to memory though the BL module. The ISIF module can process the incoming data and supports the following functions:

- Maximum supported image size is 32,768 × 32,768
- Supports up to 16-bit analog front end
- Sensor data linearization
- Supports Bayer and Foveon® input data format (RGB and CMYG color support)
- Supports VGA read out mode
- Supports various image data format
- Color space conversion
- Digital clamp with horizontal/vertical offset drift compensation
- Vertical line defect correction
- Programmable 2D-matrix LSC
- Gain and offset control
- Programmable horizontal/vertical culling pattern
- Maximum pixel rate clock of 200 MPix/s on the VP interface.
- 10-to-8-bit A-Law compression table inside
- 12-bit pack supported when written to memory

Figure 8-186 show the ISIF module connections to other submodules of the ISP.

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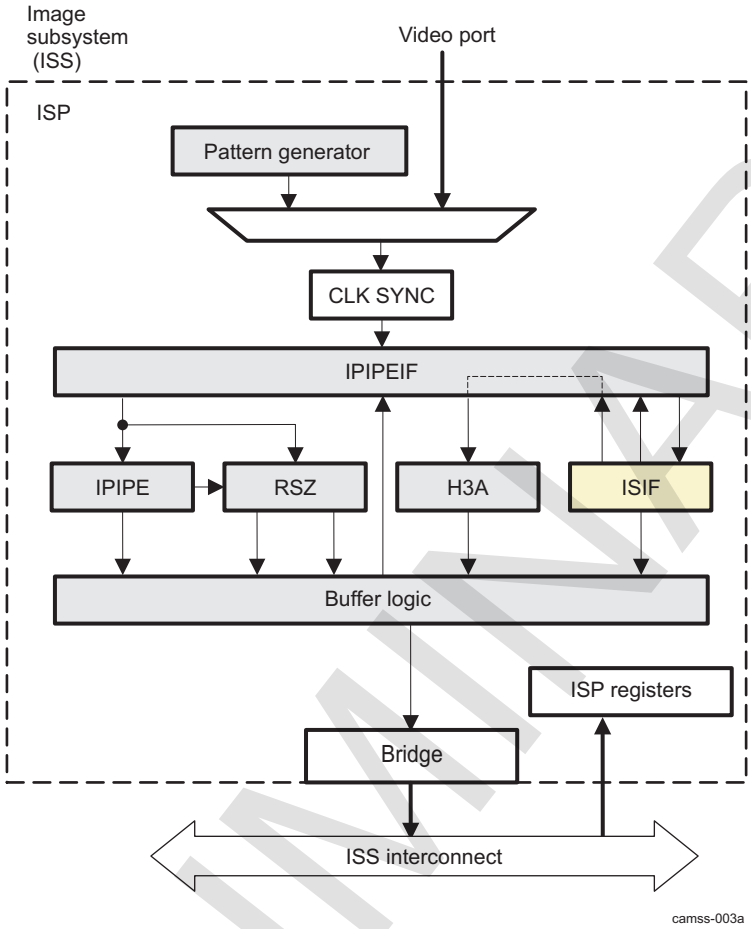
Figure 8-186. ISS ISP ISIF High-Level Diagram



8.3.3.7.2 ISS ISP ISIF Top-Level Block Diagram

Figure 8-187 shows the different blocks of the ISIF module.

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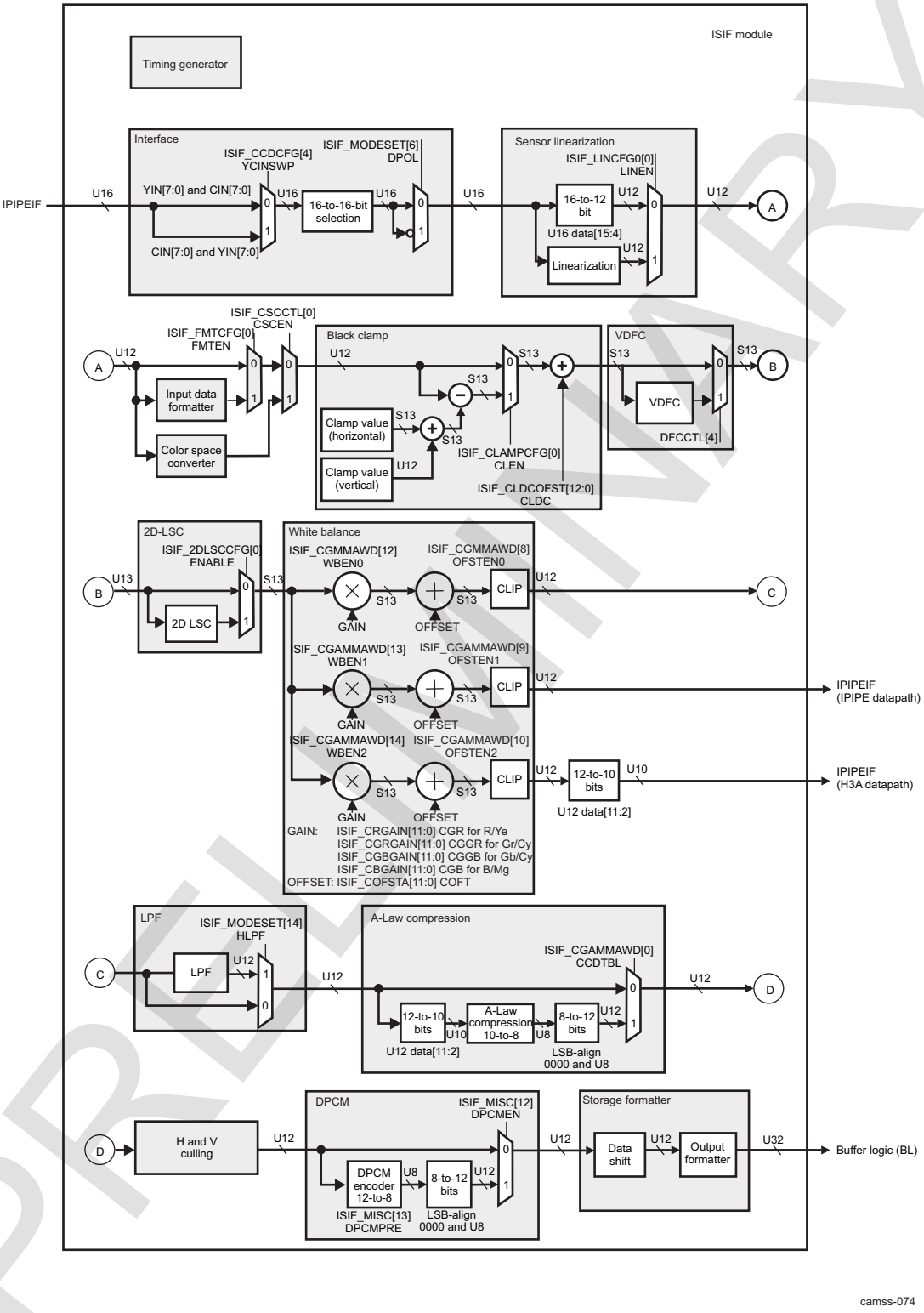
Figure 8-187. ISS ISP ISIF Top-Level Block Diagram



camss-074

The following sections describe the blocks in the ISIF module.

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8.3.3.7.3 ISS ISP ISIF Input Interface

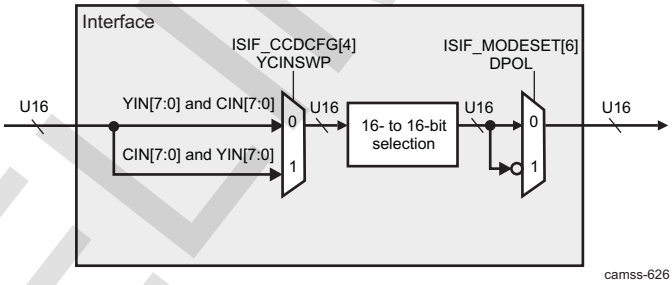
The input interface is a video interface. It comprises the horizontal(HD)l and vertical(VD) synchronization signal, pixel clock (PCLK), and data(DATA). Table 8-336 gives more information about these different signals. The ISIF uses the HD and VD signals provided by the sensor through the VP and IPIPEIF. The pixel clock clocks data into the ISIF at a maximum rate of 200 MHz.

Table 8-336. ISS ISP ISIF Input Interface Signals

Name	I/O	Function
VD	I	Vertical sync signal
HD	I	Horizontal sync signal
PCLK	I	Pixel clock. This signal is the pixel clock used to load image data into the ISIF. The clock controller can configure to trigger on the rising or falling edge of the PCLK signal.
DATA	I	Data. The data interface is a 16-bit interface. When the ISIF is configured to write data to SDRAM, the write enable signal allows an external device to control which data is to be written to SDRAM. The data input can be configured from the ISIF_MODESET.INPMOD register where it can be set to RAW, YCbCr (16 bits and 8 bits). The polarity of the data can be changed from the ISIF_MODESET.DPOL as shown in Figure 8-188.

8.3.3.7.4 ISS ISP ISIF Interface

Figure 8-188. ISS ISP ISIF Interface Block Diagram



The ISIF supports 8- to 16-bit-wide RAW data signals and 8-/16-bit YCbCr signals, as described in Table 8-337. The interface can be set in the three different modes from the ISIF_MODESET[13:12] INPMOD bit field. The ISIF_CCDCFG[11] Y8POS bit selects the y signal positioning whenever YUV4:2:2 is input. Moreover, if CCIR656 input is used the width of selected bit can be set through the ISIF_CCDCFG[5] BT656 bit.

Table 8-337. ISS ISP ISIF Data Input Formats

ISIF Input Port Name	RAW Data	16-bit YCbCr	8-bit YCbCr
YI7	C_DATA15	Y7	
YI6	C_DATA14	Y6	
YI5	C_DATA13	Y5	
YI4	C_DATA12	Y4	
YI3	C_DATA11	Y3	
YI2	C_DATA10	Y2	
YI1	C_DATA9	Y1	

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Table 8-337. ISS ISP ISIF Data Input Formats (continued)

ISIF Input Port Name	RAW Data	16-bit YCbCr	8-bit YCbCr
YI0	C_DATA8	Y0	
CI7	C_DATA7	Cb7,Cr7	Y7,Cb7,Cr7
CI6	C_DATA6	Cb6,Cr6	Y6,Cb6,Cr6
CI5	C_DATA5	Cb5,Cr5	Y5,Cb5,Cr5
CI4	C_DATA4	Cb4,Cr4	Y4,Cb4,Cr4
CI3	C_DATA3	Cb3,Cr3	Y3,Cb3,Cr3
CI2	C_DATA2	Cb2,Cr2	Y2,Cb2,Cr2
CI1	C_DATA1	Cb1,Cr1	Y1,Cb1,Cr1
CI0	C_DATA0	Cb0,Cr0	Y0,Cb0,Cr0

Y and C input signals can be swapped through the ISIF_CCDCFG[4] YCINSWP bit.

In case of RAW data at ISIF input, a 16- to-16-bit selection can be done: when the number of RAW data lines is less than 16, data can be connected to the upper or lower lines of C_DATA[15:0]. Lines not connected must be tied low. As shown in Table 8-338, the ISIF_CGAMMAWD[4:1] GWDI bit field must be configured correctly so that the MSB of the input is connected to the MSB of the 16-bit data bus in ISIF.

Table 8-338. ISS ISP ISIF Raw Data Connection: Selects MSB Position of Input Data

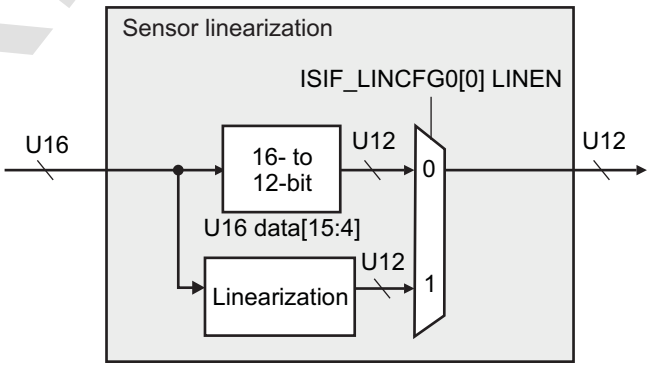
ISIF_CGAMMAWD[4:1] GWDI	16-to-16-bit Selection
0	C_DATA [15:0] = C_DATA[15:0]
1	C_DATA [15:0] = C_DATA[14:0] 0
2	C_DATA [15:0] = C_DATA[13:0] 00
3	C_DATA [15:0] = C_DATA[12:0] 000
4	C_DATA [15:0] = C_DATA[11:0] 0000
5	C_DATA [15:0] = C_DATA[10:0] 00000
6	C_DATA [15:0] = C_DATA[9:0] 000000
7	C_DATA [15:0] = C_DATA[8:0] 0000000
8	C_DATA [15:0] = C_DATA[7:0] 00000000

The polarity of the input image data can be switched through the ISIF_MODESET[6] DPOL bit.

8.3.3.7.5 ISS ISP ISIF Sensor Linearization

NOTE: For the memory access locations of the sensor linearization table, see Section 8.3.3.9.

Figure 8-189. ISS ISP ISIF Sensor Linearization Block Diagram



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The sensor linearization module can correct for the non-linear response of image sensors. A LUT is programmed with an offset value to add to the original pixel value based on the original pixel value.

The LUT is a sampling of the linearization correction curve based on calibration of the image sensor. Intermediate values between sampling points are computed using linear interpolation. The entire correction curve is divided into seven regions, as shown in Table 8-339. The regions for the darkest part and the brightest part of the response curve have dense sampling. The linearization mode can be a uniform or a non-uniform sampling and can be set through the ISIF_LINCFG0[1] LINMD bit.

Table 8-339. ISS ISP ISIF Linearization LUT

Region	Number of Sample Points	LUT Address
table_in[15:11] == 00000	32	table_in[10:6]
table_in[15:11] == 00001	4	table_in[10:9] + 32
table_in[15:12] == 0001	4	table_in[11:10] + 36
table_in[15:13] == 001	4	table_in[12:11] + 40
table_in[15:14] == 01	4	table_in[13:12] + 44
table_in[15:14] == 10	16	table_in[13:10] + 48
table_in[15:14] == 01	128	table_in[13:7] + 64

The LUT has 192 entries and is split into two 96 × 10-bit memories, as shown in Figure 8-190. The table is mapped in the memory map. The LUT entries are interleaved between memory 0 and memory 1.

Figure 8-190. ISS ISP ISIF Linearization LUT Memories

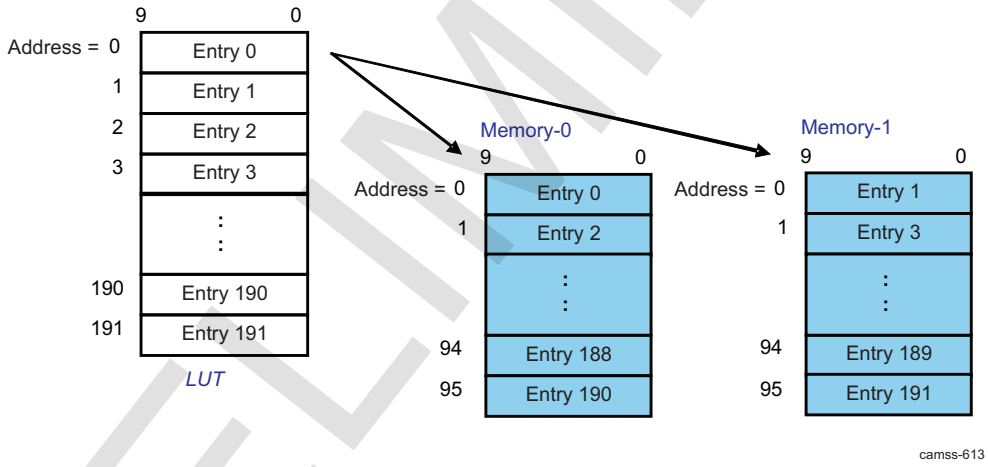

Table 8-340. ISS ISP ISIF LUT Memory Region

Memory Region	Address Range	Description
Memory 0	0xC000 – 0xC17F	ISIF linearity compensation LUT 0
Memory 1	0xC400 – C57F	ISIF linearity compensation LUT 1

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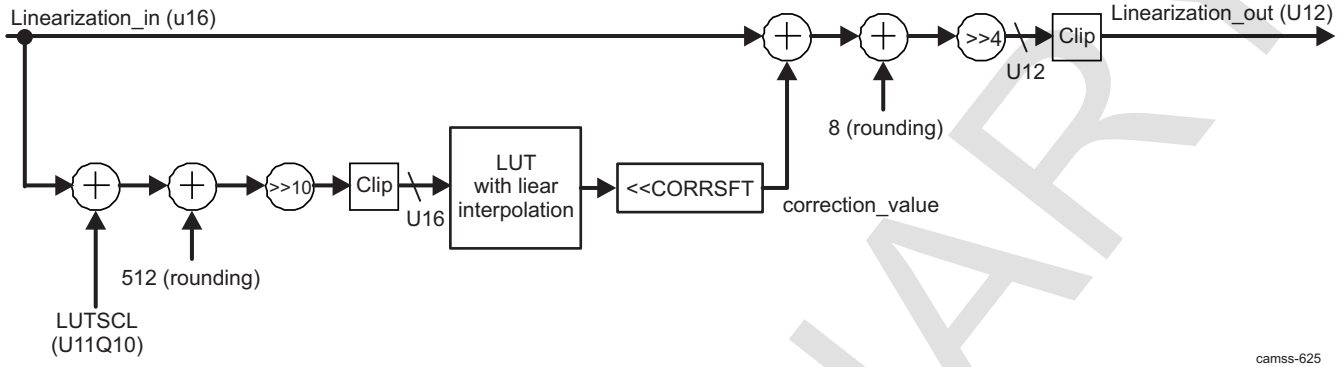
A scale factor is applied to the input before lookup through the ISIF_LINCFG1[10:0] LUTSCL bit field. The LUT entries are signed 10-bit data (u16). After linear interpolation, the correction value is left-shifted by a programmable amount (the ISIF_LINCFG0[6:4] CORRSFT bit field), and then added to the input. This is then converted to unsigned 12-bit by right shift, followed by clipping.

Figure 8-191. ISS ISP ISIF Linearization Block Diagram

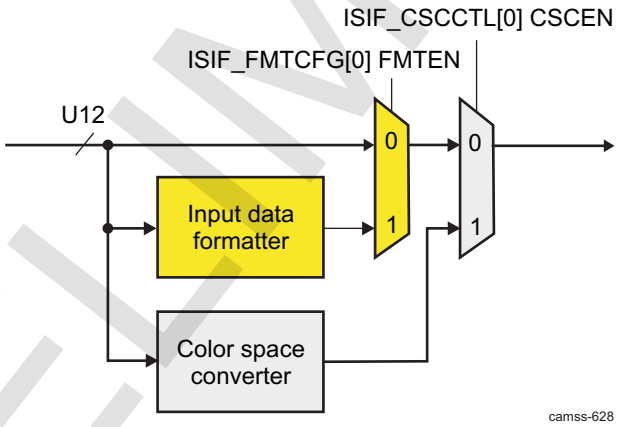


To enable the linearization module, set the ISIF_LINCFG0[0] LINEN bit to 1.

If the linearization module is disabled (ISIF_LINCFG0[0] LINEN = 0x0), a 16- to-12-bit transformation is done, and the upper 12-bits of U16 input are sent to the next block.

8.3.3.7.6 ISS ISP ISIF Input Data Formatter

Figure 8-192. ISS ISP ISIF Input Data Formatter Block Diagram



There are two functional blocks: input data formatter and color space converter, which use two 5376 × 12-bit memories (corresponds to one line of maximum 5376 pixels with each pixel equal to 12 bits). Only one of the function blocks can be enabled.

The input data formatter block allows the ISIF to handle a wide variety of current and future readout schemes other than Bayer format. Two line memories and a programmable address generator are used to translate those patterns into a standard Bayer pattern (or any other pattern). This allows the back-end processing (noise filters, interpolation, histogram, 3A statistics) to remain unchanged.

The input data formatter block also supports divided input lines. In case an input line is divided into multiple lines and fed to the ISIF, the formatter gathers the divided lines and organizes a single line. Up to four divided lines can be supported.

The input data formatter is enabled through the ISIF_FMTCFG[0] FMTEN bit.

The input data formatter can split an input line into 1, 2, 3, or 4 output lines, or can combine the divided 1, 2, 3, or 4 input lines into a single line.

- Set the ISIF_FMTCFG[1] FMTCBL bit to 0 for split mode.

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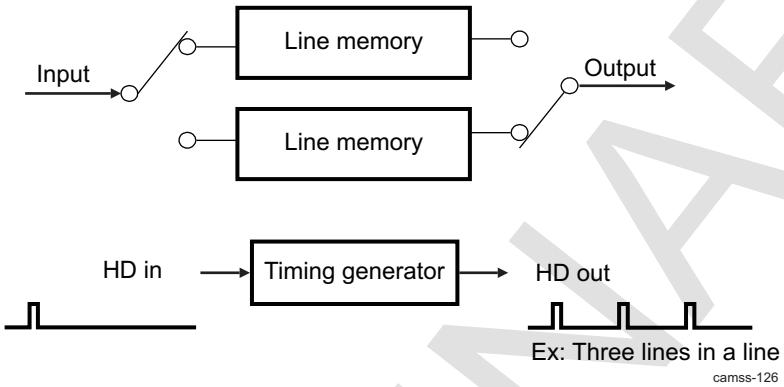
- Set the ISIF_FMTCFG[1] FMTCBL bit to 1 for combine mode.
- Select the number of lines in the ISIF_FMTCFG[5:4] LNUM bit field.

The Input data formatter can work in normal or line alternative mode. The choice is done through the ISIF_FMTCFG[2] LNALT bit.

Figure 8-193 shows an example of generating three output lines from an input line with a new, internally generated HD signal.

Figure 8-193. ISS ISP ISIF Splits an Input Line Into Three Output Lines



This HD signal then gates the downstream processing rather than the original sensor HD signal. Descriptions of how to configure the formatter are provided in the following sections.

Because the size of the line memories is 5376 × 12 bits, the following restrictions apply for the data formatter:

- Split mode:
  - The maximum number of pixels that can be supported in an output line if the input line is transformed into 1 output line is 5376.
  - The maximum number of pixels that can be supported in an output line if the input line is transformed into 2 output lines is 2688.
  - The maximum number of pixels that can be supported in an output line if the input line is transformed into 3 output lines is 1792.
  - The maximum number of pixels that can be supported in an output line if the input line is transformed into 4 output lines is 1344.
- Combine mode:
  - The maximum number of pixels that can be supported in an input line if 1 input line is transformed into an output line is 5376.
  - The maximum number of pixels that can be supported in an input line if 2 input lines are transformed into an output line is 2368.
  - The maximum number of pixels that can be supported in an input line if 3 input lines are transformed into an output line is 1792.
  - The maximum number of pixels that can be supported in an input line if 4 input lines are transformed into an output line is 1344.

8.3.3.7.6.1 ISS ISP ISIF Formatter Area Settings

As shown in Figure 8-194, the following registers are used to set the formatter area:

- ISIF_FMTSPH
- ISIF_FMTLNH
- ISIF_FMTLSV
- ISIF_FMTLNV

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Table 8-341 describes these registers. The input line is input to the formatter, and the output line is output from the formatter.

Figure 8-194. ISS ISP ISIF Input Data Formatter Area Settings

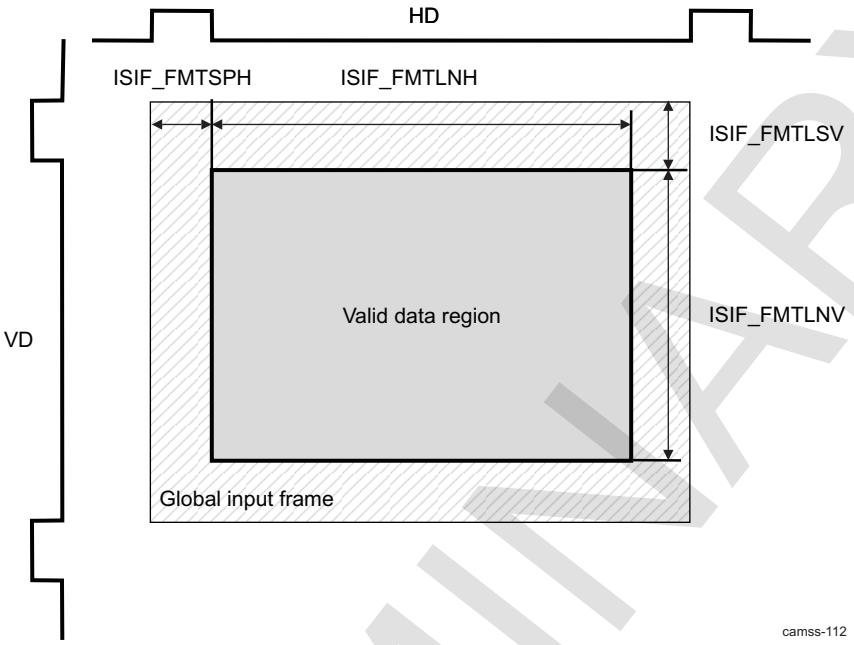

Table 8-341. ISS ISP ISIF Input Data Formatter Area Setting Registers

Register	Description
ISIF_FMTSPH	The first valid pixel of an input line
ISIF_FMTLNH	Valid length of a input line = FMTLNH + 1
ISIF_FMTLSV	The first valid input line
ISIF_FMTLNV	The number of the valid input lines = FMTLNV + 1

Table 8-342. ISS ISP ISIF Output Data Formatter Area Setting Registers

Register	Description
ISIF_FMTRLEN	The length of an output line
ISIF_FMTHCNT	HD interval for output lines
ISIF_SPH	The first pixel in an output line to be stored to SDRAM
ISIF_LNH	Number of pixels in an output line to be stored to SDRAM = LNH + 1
ISIF_LNV	The number of the output lines to be stored to SDRAM = LNV + 1

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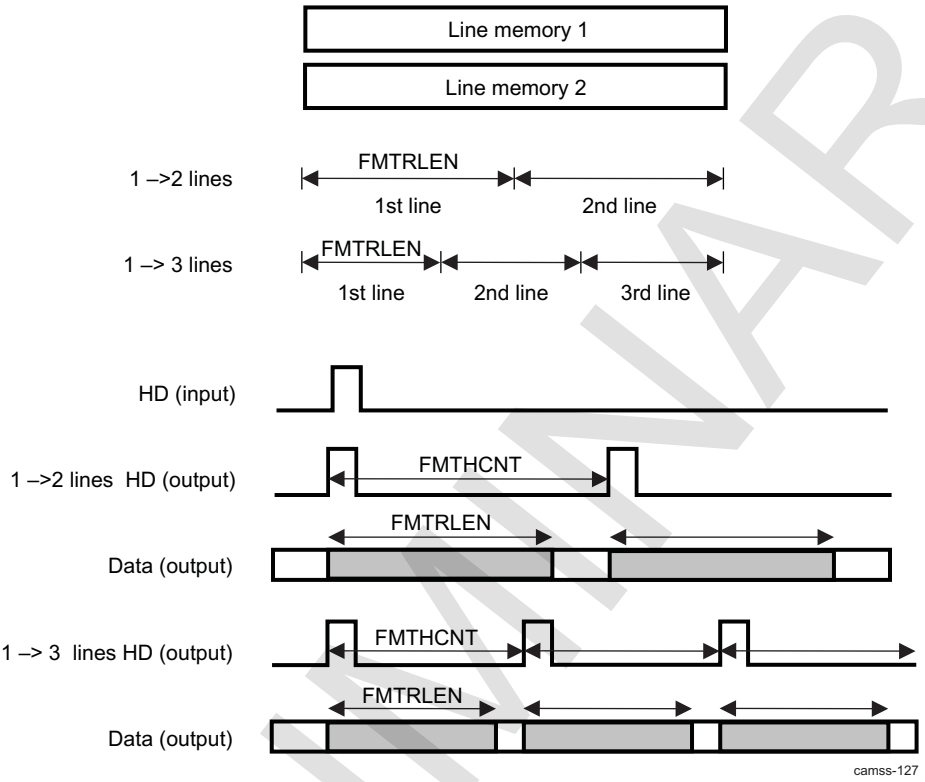
The number of pixels in an output line must be set to the ISIF_FMTRLEN register, and the HD output interval must be set to the ISIF_FMTHCNT register. It is not necessary to set the ISIF_FMTHCNT register if multiple input lines are combined into a single line.

Figure 8-195 shows an example of splitting an input line into two or three output lines.

Figure 8-195. ISS ISP ISIF Data Formatter Output Control Example



8.3.3.7.6.2 ISS ISP ISIF Formatter Programming

The data formatter derives its flexibility by supporting up to 16 different addresses and a program that can contain up to 32 entries.

Address pointer

There are 16 address pointer registers (ISIF_FMTAPTR0 to ISIF_FMTAPTR15), which contain:

- The ISIF_FMTAPTRx[14:13] LINE bit field: 2-bit line number to specify the output line to which it belongs: 0, 1, 2, or 3. It is valid only for the line splitting.
- The ISIF_FMTAPTRx[12:0] INIT bit field: 13-bit initial address for pointer x (where x = 0 to 15)

Each of the address values is auto-incremented or auto-decremented by a programmable value (the ISIF_FMTCFG[11:8] FMTAINC bit field).

Program

There are 32 program entry registers, which contain:

- In the ISIF_FMTPGMVF0 and ISIF_FMTPGMVF1 registers: The PGMxxEN fields (where xx = 00 to 31) set the program entry valid flag.
- In the ISIF_FMTPGMAPS0 to ISIF_FMTPGMAPS7 registers: The PGMxxAPTR fields specify the program xx address pointer (where xx = 00 to 31).
- In the ISIF_FMTPGMAPU0 and ISIF_FMTPGMAPU1 registers: The PGMxxUPDT fields (where xx = 00 to 31) set the program xx address update (increment or decrement).

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Because each of the program entries has a valid flag, the formatter can also support images larger than the memory limit (length: 4480) by not choosing some of the entries.

The total program memory of 32 entries is divided into two or four SETs:

- Program memory of 16 entries each for odd and even lines to split the line:
  - SET0 for even input line: Program entry 015
  - SET1 for odd input line: Program entry 1631
- Program memory of eight entries for up to four input lines to combine the lines:
  - SET0 for first input line: Program entry 07
  - SET1 for second input line: Program entry 815
  - SET2 for third input line: Program entry 1623
  - SET3 for fourth input line: Program entry 2431

The number of program entries per SET must be specified by the ISIF_FMTPLEN register as follows:

- Number of program entries for SET0: ISIF_FMTPLEN[3:0] FMTPLEN0
- Number of program entries for SET1: ISIF_FMTPLEN[7:4] FMTPLEN1
- Number of program entries for SET2: ISIF_FMTPLEN[10:8] FMTPLEN2
- Number of program entries for SET3: ISIF_FMTPLEN[14:12] FMTPLEN3

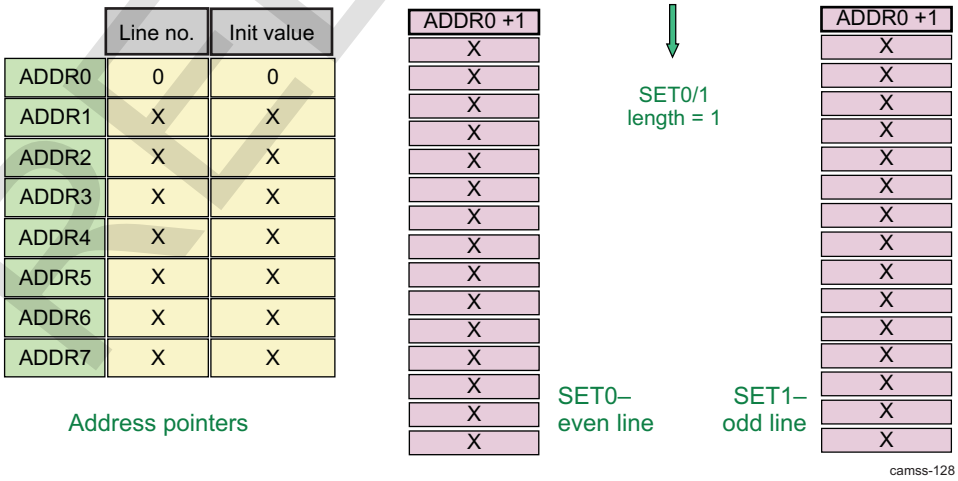
The program entry must be set from the lower registers within a SET. For instance, start from program entry 16 for odd input lines.

The following examples show the programmability of the data formatter:

- Register settings:
  - ISIF_FMTCFG[0] FMTEN = 0x1
  - ISIF_FMTCFG[1] FMTCBL = 0x0
  - ISIF_FMTCFG[11:8] FMTAINC = 0x0 (add or subtract 1)
- 1 input line - 1 output line

NOTE: ADDR0 is set to an example value. Addresses with no value in the following example are marked with X.

Figure 8-196. ISS ISP ISIF Conventional Read-Out Pattern



The following examples show the programmability of the data formatter with a 2-tap analog front end (AFE):

- Register settings:
  - ISIF_FMTCFG[0] FMTEN = 0x1

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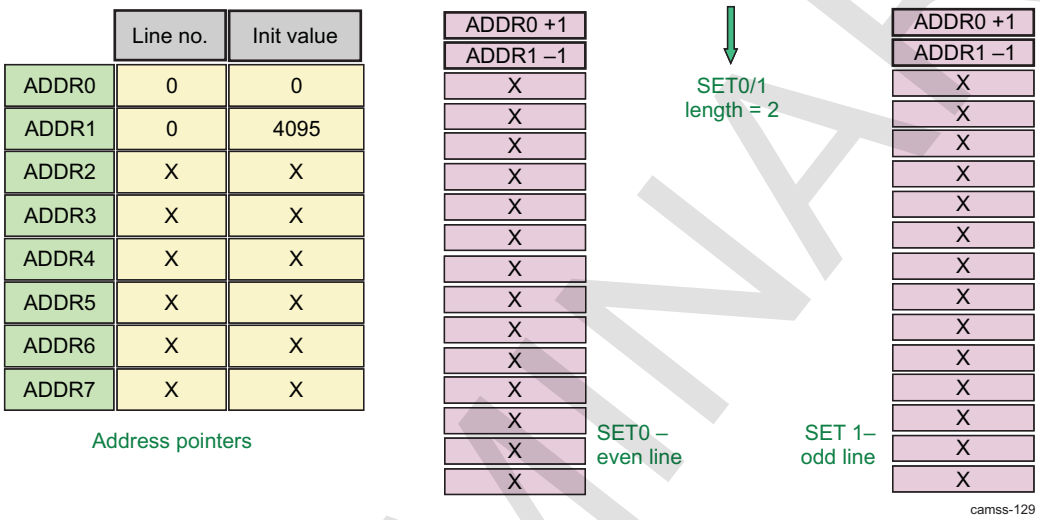
  - ISIF_FMTCFG[1] FMTCBL = 0x0
  - ISIF_FMTCFG[11:8] FMTAINC = 0x0 (add or subtract 1)
  - ISIF_FMTCFG[5:4] LNUM = 0x0
- One input line (4096) - one output line with left and right read-out
- Input - First pixel, last pixel, first pixel + 1, last pixel – 1, and so on
- Input - 0, 4095, 1, 4094, 2, 4093, 3, 4092, ..., 2047 and 2048
- Output - 0, 1, 2, 3, ..., 4094 and 4095

Figure 8-197. ISS ISP ISIF Conventional Read-Out Pattern With 2-tap AFE



8.3.3.7.6.3 ISS ISP ISIF Combine the Divided Input Lines

The formatter can gather the divided input lines and organize a single line. Figure 8-198 shows an example generating a single output line from three input lines and masking two out of three HD input pulses.

Figure 8-198. ISS ISP ISIF Combine Three Input Lines Into Single Line

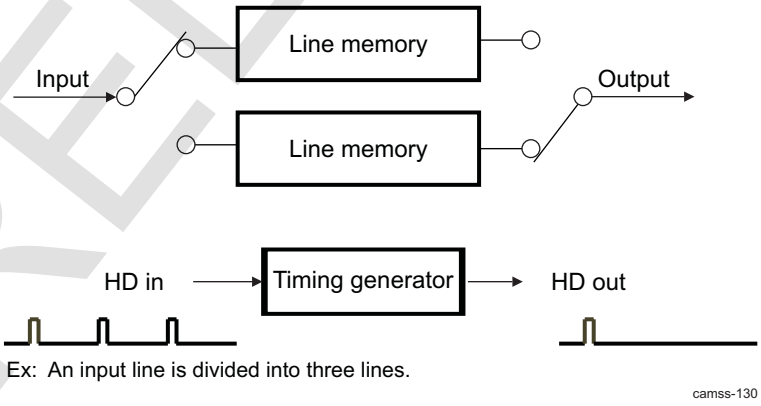


Figure 8-199 is an example that shows the register setting.

- Multiple input lines combined into one output line (use three input lines to one output line in this example)
- Input - 4, 5, 10, 11, ..., 2, 3, 8, 9, ..., 0, 1, 6, 7, ... (three lines read from sensor)
- Output - 0, 1, 2, 3, ... (1 line output)
- Register settings:

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- ISIF_FMTCFG[0] FMTEN = 0x1
- ISIF_FMTCFG[1] FMTCBL = 0x1
- ISIF_FMTCFG[11:8] FMTAINC = 0x5 (add or subtract 6)
- ISIF_FMTCFG[5:4] LNUM = 0x2
- SETs recycled based on LNUM

Figure 8-199. ISS ISP ISIF Example of Combining Three Input Lines Into a Single Line

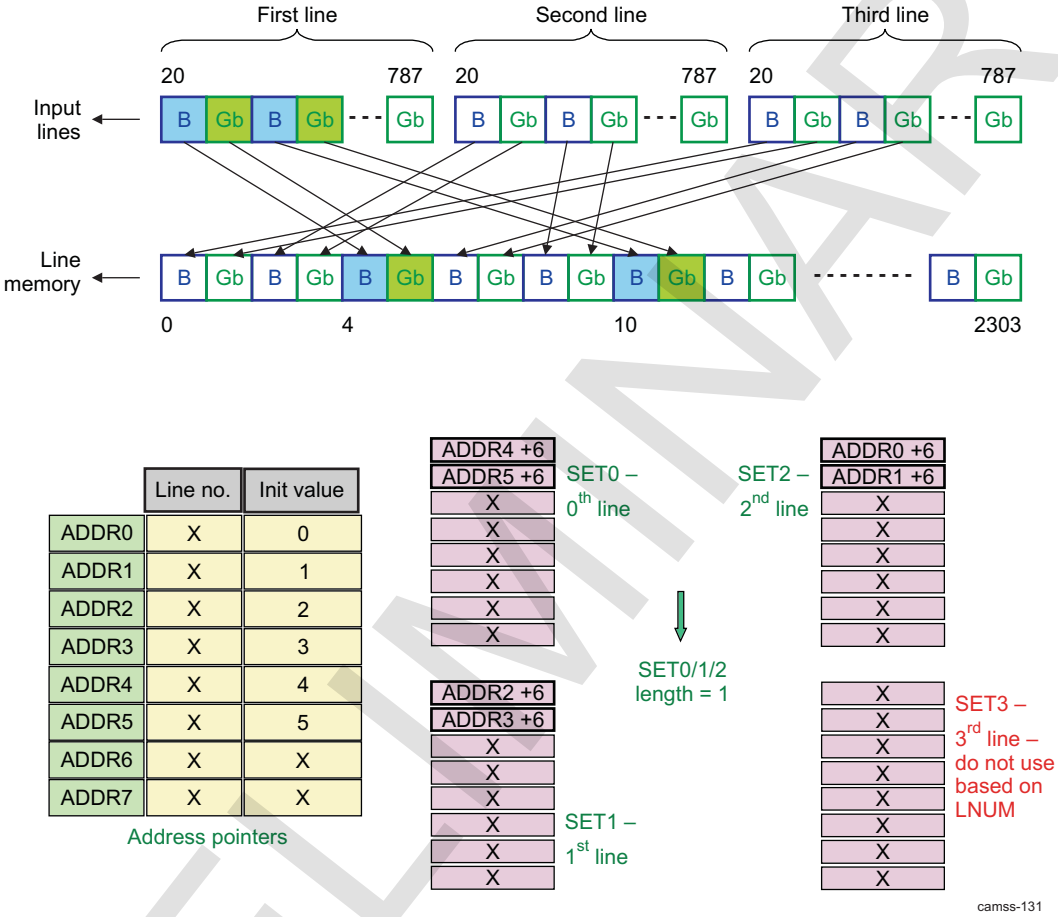

Table 8-343. ISS ISP ISIF Example of Combining Three Input Lines Into a Single Line: Register Setting Example

Step	Configuration Required	Size
Formatter enable	ISIF_FMTCFG[0] FMTEN	1
Combine input lines.	ISIF_FMTCFG[1] FMTCBL	1
Address increment = FMTAINC + 1 = 6	ISIF_FMTCFG[11:8] FMTAINC	5
The first valid pixel of a divided line	ISIF_FMTSPH[12:0] FMTSPH	20
Valid length of a divided line = FMTLNH + 1 = 768	ISIF_FMTLNH[12:0] FMTLNH	767
The first valid divided line	ISIF_FMTLSV[12:0] FMTSLV	16
The number of the valid divided lines = FMTLNV + 1 = 4590	ISIF_FMTLNV[14:0] FMTLNV	4589
The length of an organized line = (FMTLNH + 1) x (LNUM + 1) = 2304	ISIF_FMTRLEN[12:0] FMTRLEN	2304
Split/combine line number = LNUM + 1 = 3.	ISIF_FMTCFG[5:4] LNUM	2
Number of PGM entries for SET0 = FMTPLEN0 + 1 = 2	ISIF_FMTPLEN[3:0] FMTPLEN0	1
Number of PGM entries for SET1 = FMTPLEN1 + 1 = 2	ISIF_FMTPLEN[7:4] FMTPLEN1	1

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Table 8-343. ISS ISP ISIF Example of Combining Three Input Lines Into a Single Line: Register Setting Example (continued)

Step	Configuration Required	Size
Number of PGM entries for SET2 = FMTPLEN2 + 1 = 2	ISIF_FMTPLEN[10:8] FMTPLEN2	1
Address Pointer 0, INIT = 0	ISIF_FMTAPTR0[12:0] INIT	0
Address Pointer 1, INIT = 1	ISIF_FMTAPTR1[12:0] INIT	1
Address Pointer 2, INIT = 2	ISIF_FMTAPTR2[12:0] INIT	2
Address Pointer 3, INIT = 3	ISIF_FMTAPTR3[12:0] INIT	3
Address Pointer 4, INIT = 4	ISIF_FMTAPTR4[12:0] INIT	4
Address Pointer 5, INIT = 5	ISIF_FMTAPTR5[12:0] INIT	5
Program 0 Valid flag	ISIF_FMTPGMVF0[0] PGM00EN	1
Program 1 Valid flag	ISIF_FMTPGMVF0[1] PGM01EN	1
Program 8 Valid flag	ISIF_FMTPGMVF0[8] PGM08EN	1
Program 9 Valid flag	ISIF_FMTPGMVF0[9] PGM09EN	1
Program 16 Valid flag	ISIF_FMTPGMVF1[0] PGM16EN	1
Program 17 Valid flag	ISIF_FMTPGMVF1[1] PGM17EN	1
Increment Address pointer = 0x0 Program 0 Address pointer = ADDR4 + 6	ISIF_FMTPGMAPU0[0] PGM0UPDT ISIF_FMTPGMAPS0[3:0] PGM0APTR	4
Increment Address pointer = 0x0 Program 1 Address pointer = ADDR5 + 6	ISIF_FMTPGMAPU0[1] PGM1UPDT ISIF_FMTPGMAPS0[7:4] PGM1APTR	5
Increment Address pointer = 0x0 Program 8 Address pointer = ADDR2 + 6	ISIF_FMTPGMAPU0[8] PGM8UPDT ISIF_FMTPGMAPS2[3:0] PGM8APTR	2
Increment Address pointer = 0x0 Program 9 Address pointer = ADDR3 + 6	ISIF_FMTPGMAPU0[9] PGM9UPDT ISIF_FMTPGMAPS2[7:4] PGM9APTR	3
Increment Address pointer = 0x0 Program 16 Address pointer = ADDR0 + 6	ISIF_FMTPGMAPU1[1] PGM17UPDT ISIF_FMTPGMAPS4[3:0] PGM16APTR	0
Increment Address pointer = 0x0 Program 17 Address pointer = ADDR1 + 6	ISIF_FMTPGMAPU1[0] PGM16UPDT ISIF_FMTPGMAPS4[7:4] PGM17APTR	1

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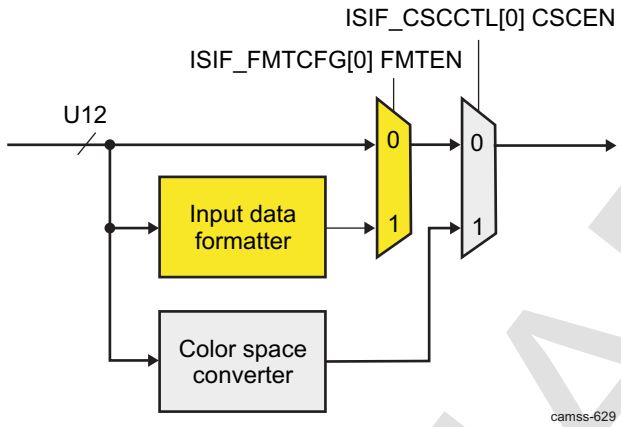
8.3.3.7.7 ISS ISP ISIF Color Space Converter

Figure 8-200. ISS ISP ISIF Color Space Converter Block Diagram

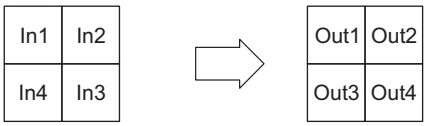


The color space converter (CSC) includes four 8-bit × 12-bit multipliers and one adder for the color space conversion. These multiplier/adder units are used for the operation described in Figure 8-201. Data are taken from two input lines during the operation.

Coefficients are signed 8-bit (decimal is 5 bits). Coefficients are set through the following registers:

- Coefficient M00: ISIF_CSCM0[7:0] CSCM00
- Coefficient M01: ISIF_CSCM0[15:8] CSCM01
- Coefficient M02: ISIF_CSCM1[7:0] CSCM02
- Coefficient M03: ISIF_CSCM1[15:8] CSCM03
- Coefficient M10: ISIF_CSCM2[7:0] CSCM10
- Coefficient M11: ISIF_CSCM2[15:8] CSCM11
- Coefficient M12: ISIF_CSCM3[7:0] CSCM12
- Coefficient M13: ISIF_CSCM3[15:8] CSCM13
- Coefficient M20: ISIF_CSCM4[7:0] CSCM20
- Coefficient M21: ISIF_CSCM4[15:8] CSCM21
- Coefficient M22: ISIF_CSCM5[7:0] CSCM22
- Coefficient M23: ISIF_CSCM5[15:8] CSCM23
- Coefficient M30: ISIF_CSCM6[7:0] CSCM30
- Coefficient M31: ISIF_CSCM6[15:8] CSCM31
- Coefficient M32: ISIF_CSCM7[7:0] CSCM32
- Coefficient M33: ISIF_CSCM7[15:8] CSCM33

Figure 8-201. ISS ISP ISIF Color Space Converter Operation



$$\begin{pmatrix} Out1 \\ Out2 \\ Out3 \\ Out4 \end{pmatrix} = \begin{pmatrix} M00 & M01 & M02 & M03 \\ M10 & M11 & M12 & M13 \\ M20 & M21 & M22 & M23 \\ M30 & M31 & M32 & M33 \end{pmatrix} \begin{pmatrix} In1 \\ In2 \\ In3 \\ In4 \end{pmatrix}$$

M00–M33: Signed 8-bit data with 5-bit decimal
the value range –4=< Mxx<4

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The CSC can convert CMYG filtered CCD data to Bayer matrix (RGBG) data, as shown in Figure 8-202.

Figure 8-202. ISS ISP ISIF Color Space Converter Operation: CMYG to RGBG

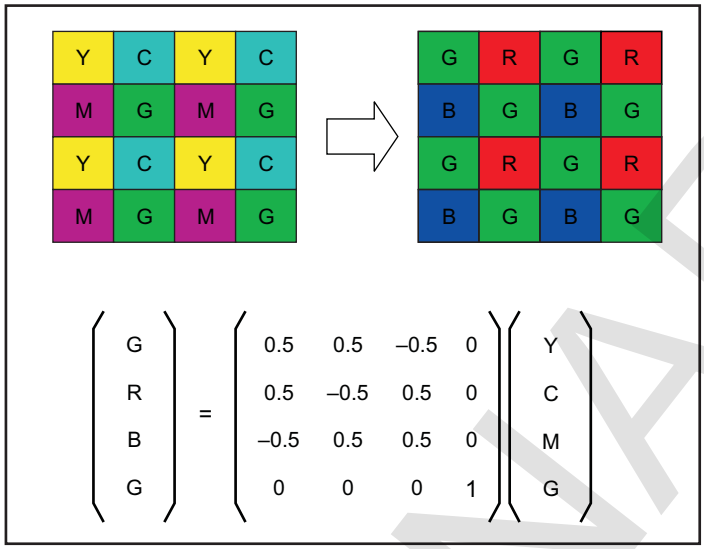

Figure 8-203 through Figure 8-205 show which input pixels are used for the operation. There is one-line latency between the input and the output.

Figure 8-203. ISS ISP ISIF Color Space Conversion Example

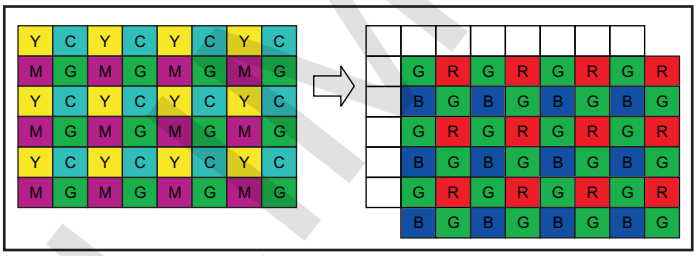

Figure 8-204. ISS ISP ISIF 1st Pixel/1st Line Generation

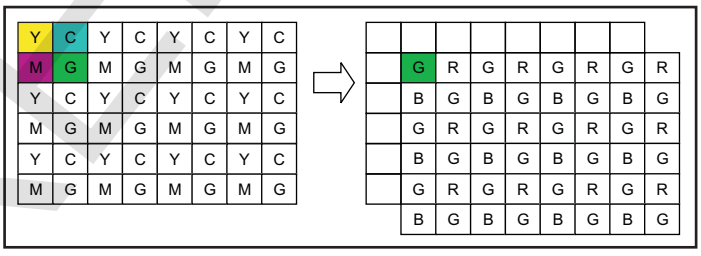

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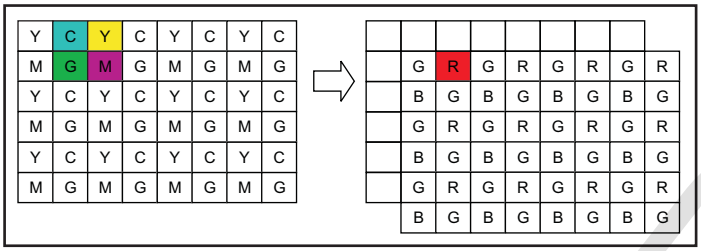
Figure 8-205. ISS ISP ISIF 2nd Pixel/1st Line Generation



As shown inFigure 8-206 through Figure 8-209, the operation for the last pixel and the second last pixel uses the same input data.

Figure 8-206. ISS ISP ISIF 2nd Last Pixel/1st Line Generation

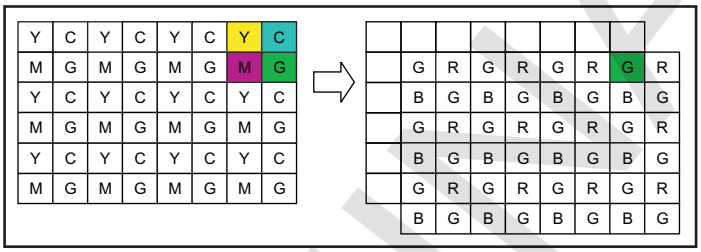


Figure 8-207. ISS ISP ISIF Last Pixel/1st Line Generation

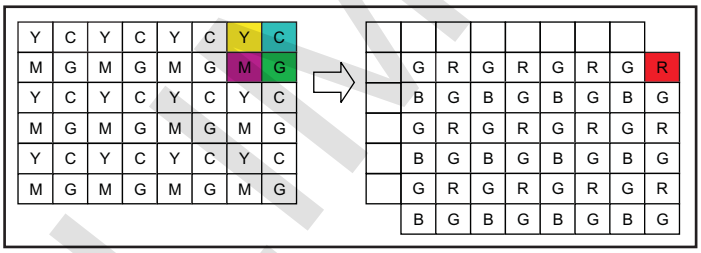


Figure 8-208. ISS ISP ISIF 1st Pixel/Last Line Generation

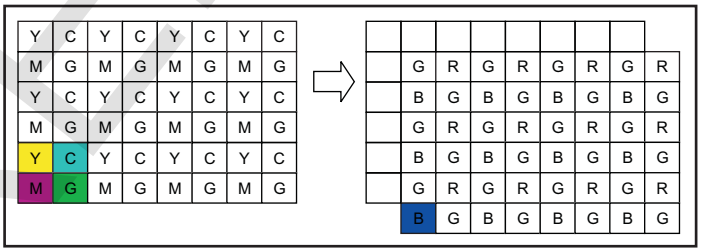


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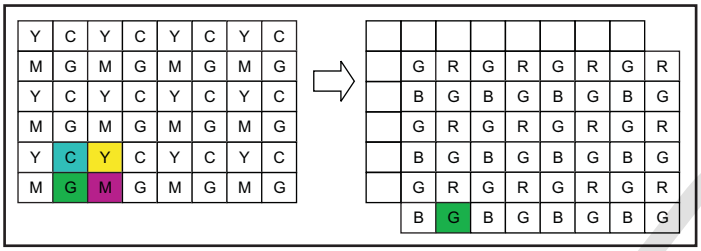
Figure 8-209. ISS ISP ISIF 2nd Pixel/Last Line Generation



Also, the operation for the last line and the second last line uses the same input data (see Figure 8-210 and Figure 8-211).

Figure 8-210. ISS ISP ISIF 2nd Last Pixel/Last Line Generation

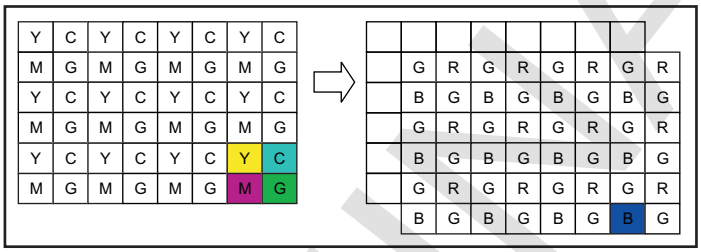
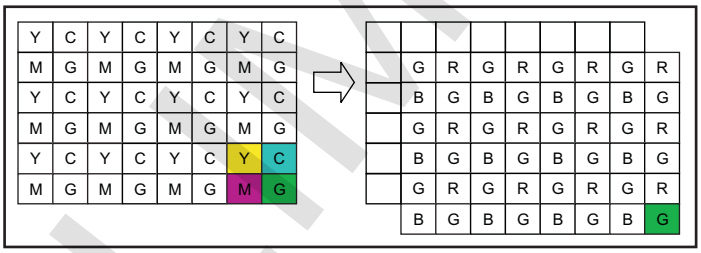


Figure 8-211. ISS ISP ISIF Last Pixel/Last Line Generation



In addition to the registers specific to the color space converter, some of the registers are shared with the input data formatter to configure the valid area:

- ISIF_FMTSPH
- ISIF_FMTLNH
- ISIF_FMTLSV
- ISIF_FMTLNV

There must be at least 1 invalid pixel at the end of the line and one invalid line at the end of the frame.

To enable the color space conversion, set the ISIF_CSCCTL[0] CSCEN bit to 1.

8.3.3.7.8 ISS ISP ISIF Black Clamp

NOTE: For the memory access locations of the ISIF clamp, see Section 8.3.3.9.

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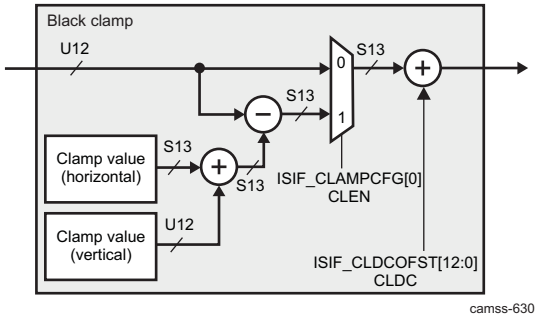
Figure 8-212. ISS ISP ISIF Black Clamp Block Diagram



The clamp value is calculated based on the pixel value of the OB region of the sensor. The clamp value is calculated separately for horizontal and vertical directions to compensate the offset drift in both horizontal and vertical directions. The sum of the horizontal and vertical clamp values is subtracted from the image data, and then the additional DC offset is added (the ISIF_CLDCOFST[12:0] CLDC bit field, an S13Q0 value). This value is added whether the black clamp module is enabled or not.

The horizontal clamp is disabled through the ISIF_CLAMPCFG[2:1] CLHMD bit field.

To enable the black clamp module, set the ISIF_CLAMPCFG[0] CLEN bit to 1. The ISIF_PPLN[15:0] PPLN bit field sets the pixel per line, and the number of pixel clock periods in one line HD period equals PPLN + 1 pixel clock. The ISIF_PPLN[15:0] bit field is not used when the input is are already HD/VD.

8.3.3.7.8.1 ISS ISP ISIF Clamp Value for Horizontal Direction

The clamp value for horizontal direction is calculated using the pixel values at the upper OB region.

The maximum pixel value to be used for the clamp value calculation can be limited to 1023 if the pixel value limitation is enabled (ISIF_CLHWIN0[6] CLHLMT = 1).

Clamp value calculation for horizontal direction can be disabled in case there is no upper OB region. The operating modes are:

- Horizontal clamp value calculation is enabled. The calculated horizontal clamp value is subtracted from the image data along with the vertical clamp value (ISIF_CLAMPCFG[2:1] CLHMD = 0x1).
- Horizontal clamp value is not updated. The horizontal clamp value used for the previous image is subtracted from the image data along with the vertical clamp value (ISIF_CLAMPCFG[2:1] CLHMD = 0x2).
- Horizontal clamp value is not updated. Only the vertical clamp value is subtracted from the image data (ISIF_CLAMPCFG[2:1] CLHMD = 0x0).

The number of windows in a row is set with the ISIF_CLHWIN0[4:0] CLHWC bit field.

Up to 32 windows in a row can be set for clamp value calculation. All the windows have the same size in a format [$2^{(ISIF_CLHWIN0[9:8]\ CLHWM+5)}$] pixels by [$2^{(ISIF_CLHWIN0[13:12]\ CLHWN+1)}$] lines.

The ISIF_CLHWIN2[12:0] CLHSV and ISIF_CLHWIN1[12:0] CLHSH bit fields enable setting the position of the first optical black clamp window in the frame. The pixel and line offset are in a range [0:8191]. The ISIF_HDW register sets the width of the HD.

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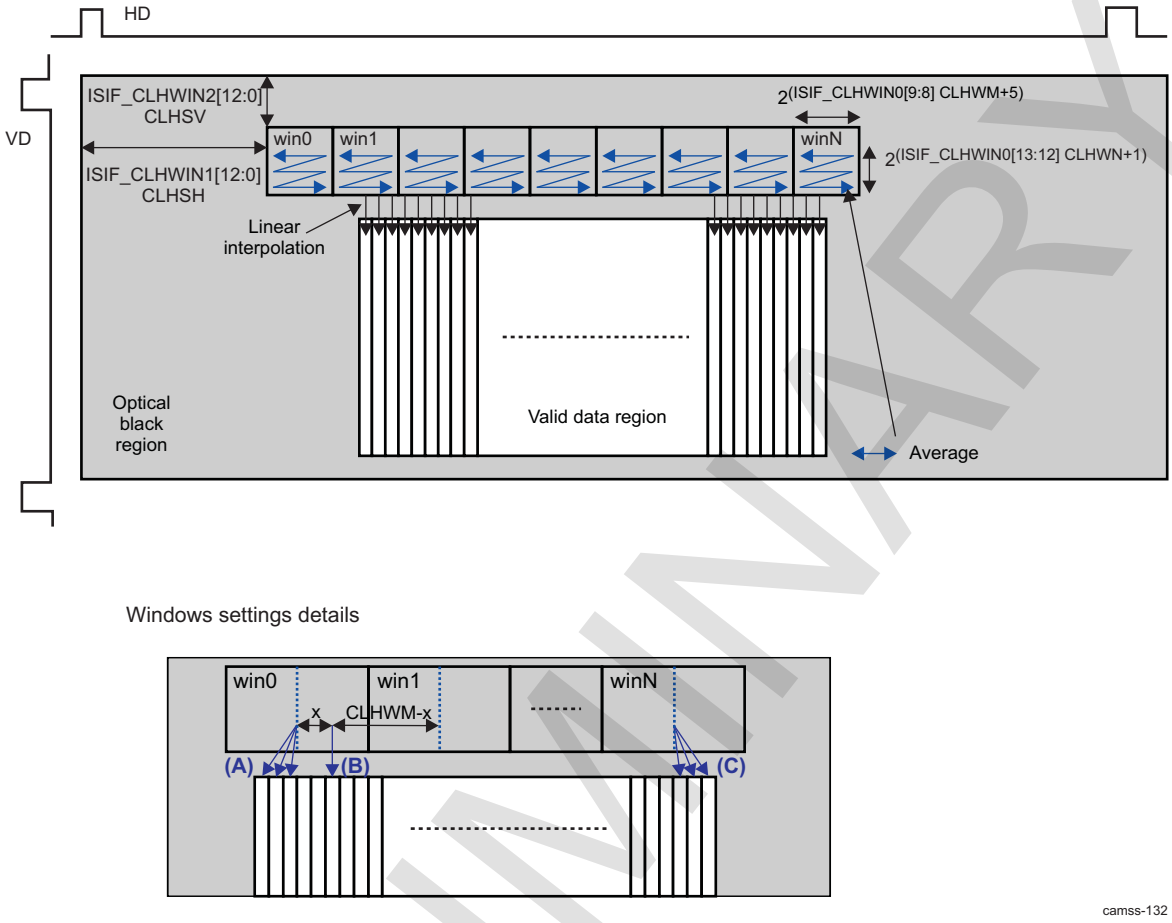
Figure 8-213. ISS ISP ISIF Clamp Value for Horizontal Direction



The clamp value for horizontal direction calculation steps is:

1. Calculate the average of the pixel value in each window (ave_win_0 to ave_win_N).

Calculation Steps	win0	win1	win2	...	wini	wini + 1	...	winN
Average of the pixel value	ave_win_0	ave_win_1	ave_win_2		ave_win_i	ave_win_{i+1}		ave_win_N

2. Set the average of the left-most window or the right-most window as the base value B_V:
   - B_V = ave_win_0 (if ISIF_CLHWIN0[5] CLHWBS = 0x0, case 1)
   - B_V = ave_win_N (if ISIF_CLHWIN0[5] CLHWBS = 0x1, case 2)
3. Subtract the base value from the average of each window. Use this value as a clamp value for each window.

Calculation Steps	win0	...	wini	wini+1	...	winN
Clamp value for each window	$clamp_win_0$ = ave_win_0- B_V		$clamp_win_i$ = ave_win_i-B_V	$clamp_win_{i+1}$ = ave_win_{i+1}-B_V		$clamp_win_N$ = ave_win_N-B_V

4. Acquire the horizontal distance (X and CLHWM – X) from the valid pixel to be processed to the center of the closest two windows.
5. Calculate the clamp value of the valid pixel by linear interpolation, using the clamp value of the closest two windows (i and i + 1).
   - Case 1: interpolated_clamp_win$_X$ = ($clamp_win_{i+1}$ – $clamp_win_i$) * X / CLHWM
   - Case 2: interpolated_clamp_win$_X$ = ($clamp_win_i$ – $clamp_win_N$) * (CLHWM - X) / CLHWM +

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($clamp_win_{i+1}$ – $clamp_win_N$) * X / CLHWM

6. If the valid pixel is on the left of the center of the left-most window, the clamp value of the left-most window is applied. If the valid pixel is on the right of the center of the right-most window, the clamp value of the right-most window is applied.

The clamp values calculated (A), (B) and (C) are:

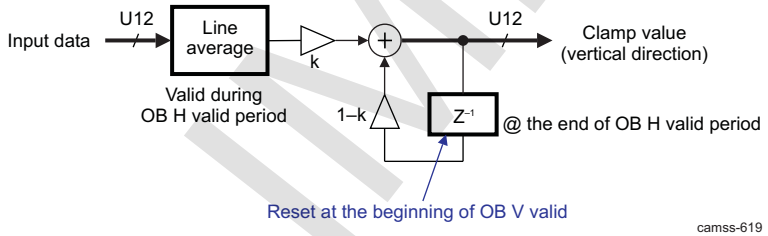
- Case1: Base is win0 (Left-most window: ISIF_CLHWIN0[5] CLHWBS = 0x0)
  - (A): zero
  - (B): ($clamp_win_{i+1}$ – $clamp_win_i$) * X / CLHWM
  - (C): ($clamp_win_N$ – $clamp_win_0$)
- Case2: Base is winN (Right-most window: ISIF_CLHWIN0[5] CLHWBS = 0x1)
  - (A): ($clamp_win_0$ – $clamp_win_N$)
  - (B): ($clamp_win_i$ – $clamp_win_N$) * (CLHWM – X) / CLHWM + ($clamp_win_{i+1}$ – $clamp_win_N$) * X / CLHWM
  - (C): zero

Each interpolated value $interpolated_clamp_win_X$ is then subtracted to the associated column.

8.3.3.7.8.2 ISS ISP ISIF Clamp Value for Vertical Direction

The clamp value for vertical direction is calculated using the pixel values at the left or right OB region. Line average is calculated for the OB H valid period ($2^{(ISIF_CLVWIN0[2:0]\ CLVOBH\ +\ 1)}$). The averages for the previous lines are also added back to reduce the difference between the lines, as shown in Figure 8-214.

Figure 8-214. ISS ISP ISIF Clamp Value for Vertical Direction Calculation



- Clamp Value (V_n) = Line Average (V_n) * k + Clamp Value (V_1) * (1-k)
- k = ISIF_CLVWIN0[15:8] CLVCOEF

The position of the first vertical black clamp window is set with the ISIF_CLVWIN2[12:0] CLVSV and ISIF_CLVWIN1[12:0] CLVSH bit fields. The number of vertical windows is set with the ISIF_CLVWIN3[12:0] CLVOBV bit field. ISIF_VDW sets the width of the VD.

The accumulator, which holds the vertical clamp value for the previous line, is reset at the beginning of the OB V valid. The reset value can be selected through the ISIF_CLVWIN0[5:4] CLVRVSL bit field:

- ISIF_CLVWIN0[5:4] CLVRVSL = 0x0: The base value is calculated for horizontal direction (left-most window win0 or right-most winn set with ISIF_CLHWIN0[5] CLHWBS).
- ISIF_CLVWIN0[5:4] CLVRVSL = 0x1: The base value is set through the configuration register (ISIF_CLVRV[11:0] CLVRV).
- ISIF_CLVWIN0[5:4] CLVRVSL = 0x2: No update (same as the previous image)

The following figures show the OB valid settings and associated vertical clamp value calculation when OB region is at the left (seeFigure 8-215) and when OB region is at the right (see Figure 8-216). Each line average value is subtracted from the associated line valid region data.

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Figure 8-215. ISS ISP ISIF Clamp Value for Vertical Direction With OB Region at the Left

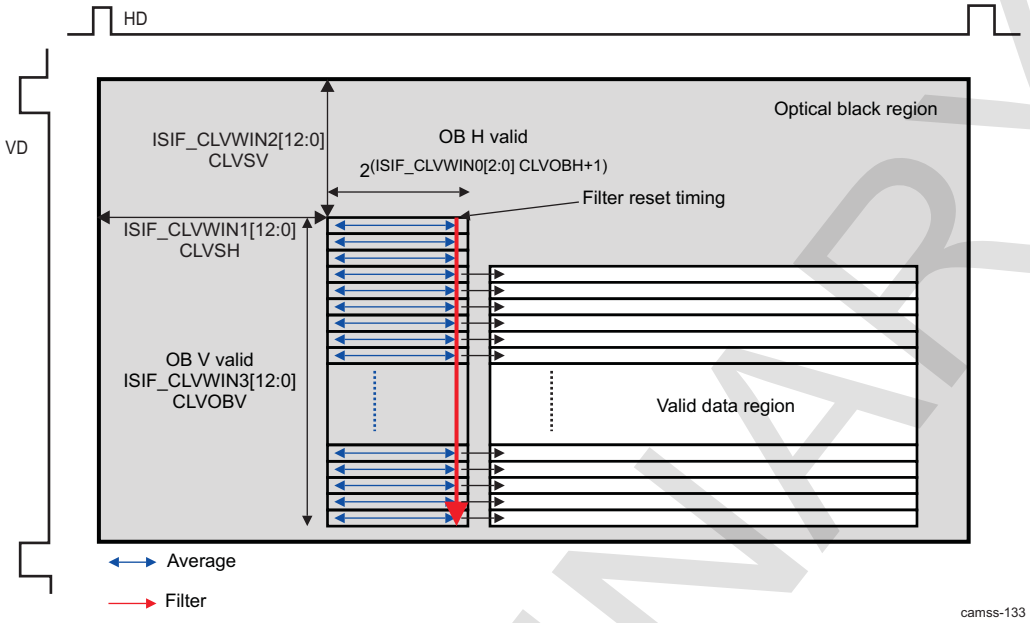
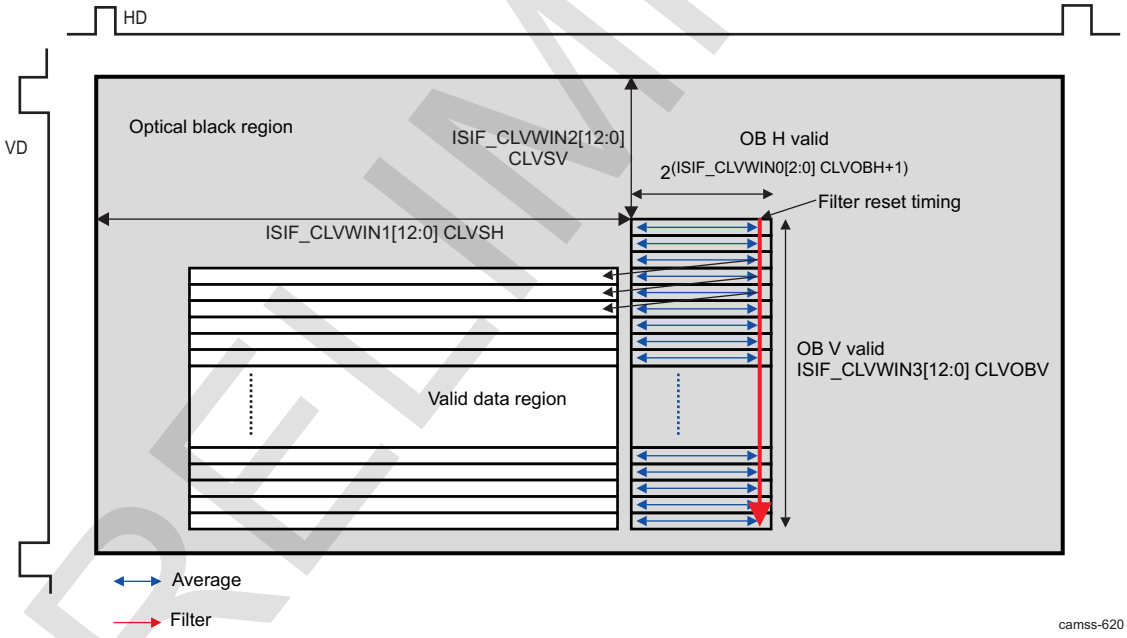


Figure 8-216. ISS ISP ISIF Clamp Value for Vertical Direction With OB Region at the Right



8.3.3.7.9 ISS ISP ISIF Vertical Line Defect Correction (VDFC)

Figure 8-217 shows the block diagram of the vertical line defect (VDFC) correction.

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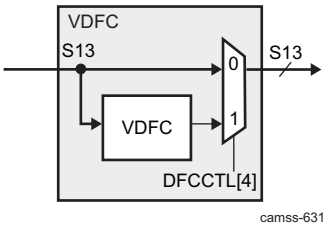
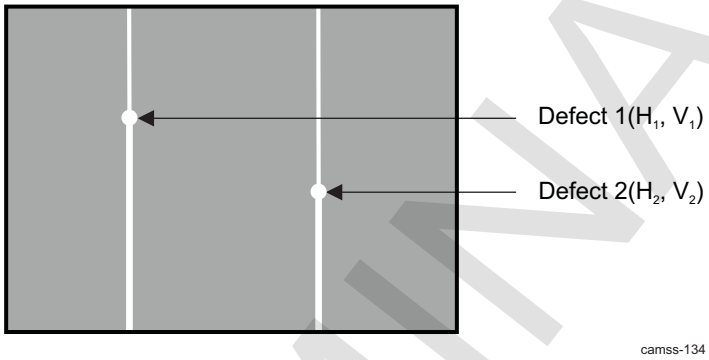
Figure 8-217. ISS ISP ISIF Vertical Line Defect Correction Block Diagram



The VDFC block can correct up to eight vertical line defects (see Figure 8-218).

Figure 8-218. ISS ISP ISIF Vertical Line Defects



The correction method is common to all the defects and can be selected through the ISIF_DFCCTL[6:5] VDFCSL bit field.

There are two different methods to correct vertical line defects (ISIF_DFCCTL[6:5] VDFCSL):

- Method 1: Data is replaced by an average (ISIF_DFCCTL[6:5] VDFCSL = 0x2):
  - The defect is replaced by the average of pixel (i – 2) and pixel (i + 2)
- Method 2: Data is subtracted by a defect level (ISIF_DFCCTL[6:5] VDFCSL = 0x0 or 0x1):
  - A saturation level is defined in the ISIF_VDFSATLV[11:0] VDFSLV bit field.
  - The coordinates of the defect:
    - Are defined in the ISIF_DFCMEM0[12:0] DFCMEM0 and ISIF_DFCMEM1[12:0] DFCMEM1 bit fields
    - Are 13 bits wide for horizontal and vertical direction, so an image size up to 8192 × 8192 is supported
  - If the data is not saturated (data VDFSLV):
    - The defect is corrected by subtracting the defect level. A different defect level is defined for:
      - The point of the defect (V = Vdefect): SUB1 defect level is defined in the ISIF_DFCMEM2[7:0] DFCMEM2 bit field.
      - The pixels lower than the defect (V Vdefect): SUB2 defect level is defined in the ISIF_DFCMEM3[7:0] DFCMEM3 bit field.
      - The pixels upper than the defect (V Vdefect): Defect level is defined in the ISIF_DFCMEM4[7:0] DFCMEM4 bit field.
    - Each defect level (value to be subtracted from the data) described previously can be up-shifted through the ISIF_DFCCTL[10:8] VDFLSFT bit field.
    - Vertical line defect correction for upper pixels can be disabled through the ISIF_DFCCTL[7] VDFCUDA bit.
  - If the data is saturated (VDFSLV), there are two possibilities:
    - ISIF_DFCCTL[6:5] VDFCSL = 0x0: Data is simply fed through (not subtracted).
    - ISIF_DFCCTL[6:5] VDFCSL = 0x1: Horizontal interpolation ((i 2) + (i + 2))/2 (data is replaced by

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interpolation or data is subtracted with interpolation)

The ISIF_LPFR register sets the number of half lines per frame or field: VD period = (L PFR+ 1)/2 lines. LPFR is not used when HD and VD are inputs.

The following paragraphs concern only method 2 correction.

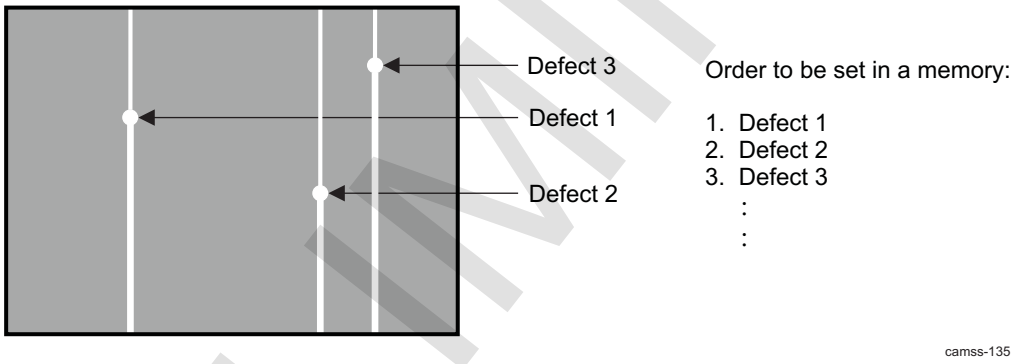
The coordinates of the defects and the defect levels to be subtracted from the data must be set to the processing shown in Table 8-344.

Table 8-344. ISS ISP ISIF Vertical Line Defect Table in Memory

Bit	Defect Information
12:0	Vertical position of the defects
25:13	Horizontal position of the defects
33:26	Defect level of the vertical line defect position (V = Vdefect)
41:34	Defect level of the pixels upper than the vertical line defect (V Vdefect)
49:42	Defect level of the pixels lower than the vertical line defect (V Vdefect)

The defect must be set from left to right, as shown in Figure 8-219.

Figure 8-219. ISS ISP ISIF Vertical Line Defects



Vertical line defect correction is enable by setting the ISIF_DFCCTL[4] VDFCEN bit to 1, but the procedure explained in Section 8.3.3.7.9.1, *ISS ISP ISIF Vertical Line Defect Table Update Procedure*, must be respected.

8.3.3.7.9.1 ISS ISP ISIF Vertical Line Defect Table Update Procedure

The following procedure must be respected to write the vertical line defect table in memory.

1. ISIF_DFCMEMCTL[4] DFCMCLR = 0x1
2. Ensure that ISIF_DFCCTL[4] VDFCEN is disabled (0x0).
3. Write the V coordinate of the first defect to the ISIF_DFCMEM0[12:0] DFCMEM0 bit field.
4. Write the H coordinate of the first defect to the ISIF_DFCMEM1[12:0] DFCMEM1 bit field.
5. Set the defect level to:
   - ISIF_DFCMEM2[7:0] DFCMEM2
   - ISIF_DFCMEM3[7:0] DFCMEM3
   - ISIF_DFCMEM4[7:0] DFCMEM4
6. Set the ISIF_DFCMEMCTL[0] DFCMWR bit to 1 with the ISIF_DFCMEMCTL[2] DFCMARST bit set to 1.
7. Wait until the ISIF_DFCMEMCTL[0] DFCMWR bit is cleared.
8. Write the next data to:
   - ISIF_DFCMEM0[12:0] DFCMEM0

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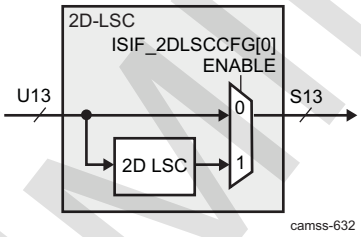
- ISIF_DFCMEM1[12:0] DFCMEM1
- ISIF_DFCMEM2[7:0] DFCMEM2
- ISIF_DFCMEM3[7:0] DFCMEM3
- ISIF_DFCMEM4[7:0] DFCMEM4

9. Set the ISIF_DFCMEMCTL[0] DFCMWR bit to 1 with the ISIF_DFCMEMCTL[2] DFCMARST bit cleared.
10. Repeat 4~5 times until all entries (up to 8) are written to the vertical line defect table.
11. In case the defect entry is less than 8, an extra write cycle is required to fill the next table location with a certain value.
12. Clear the ISIF_DFCMEM0[12:0] DFCMEM0 bit field to all 0, set the ISIF_DFCMEM1[12:0] DFCMEM1 to all 1, and set the ISIF_DFCMEMCTL[0] DFCMWR bit to 1 with the ISIF_DFCMEMCTL[2] DFCMARST bit cleared.
13. Enable VDFC by setting the ISIF_DFCCTL[1] VDFCEN bit.

8.3.3.7.10 ISS ISP ISIF Lens Shading Correction (2D-LSC)

NOTE: For the memory access locations of the 2D-LSC table, see Section 8.3.3.9.

Figure 8-220. ISS ISP ISIF 2D-LSC Block Diagram



LSC is useful for correcting optical artifacts that cause image brightness to decrease starting from the center of the image and going out to the edges.

The LSC module implements a per pixel offset and gain adjustment in the RAW Bayer domain (2 × 2 color pattern). The offset is applied before gain multiplication.

The offset and gains are stored in a LUT, which is stored in SDRAM and is loaded in real time. The submodule prefetches the data from SDRAM such that no underflow occurs. Underflow occurs when the offset and gain data required for the current pixel are not available.

The data stored in the LUT is downsampled; that is, there is no gain or offset per pixel. The downsampling factor is programmable. High downsampling ratios lead to a smaller LUT, lower accuracy, and lower memory bandwidth. A low downsampling ratio leads to a bigger LUT, higher accuracy, and higher memory bandwidth.

When the offset and gain values are loaded, they are upscaled to the incoming image resolution. The missing table values are computed through bilinear interpolation.

To enable the 2D-LSC module, set the ISIF_2DLSCCFG[0] ENABLE bit to 1.

8.3.3.7.10.1 ISS ISP ISIF 2D-LSC Active Region Settings

The gain and offset maps are internally up-sampled to full resolution before being applied to the image. In order to account for all the possible cropping schemes and zoom ratios, the 2D-LSC can be configured such that a single gain map can be stored in memory that maps to sensor lens. The 2D-LSC active region is defined by Figure 8-221.

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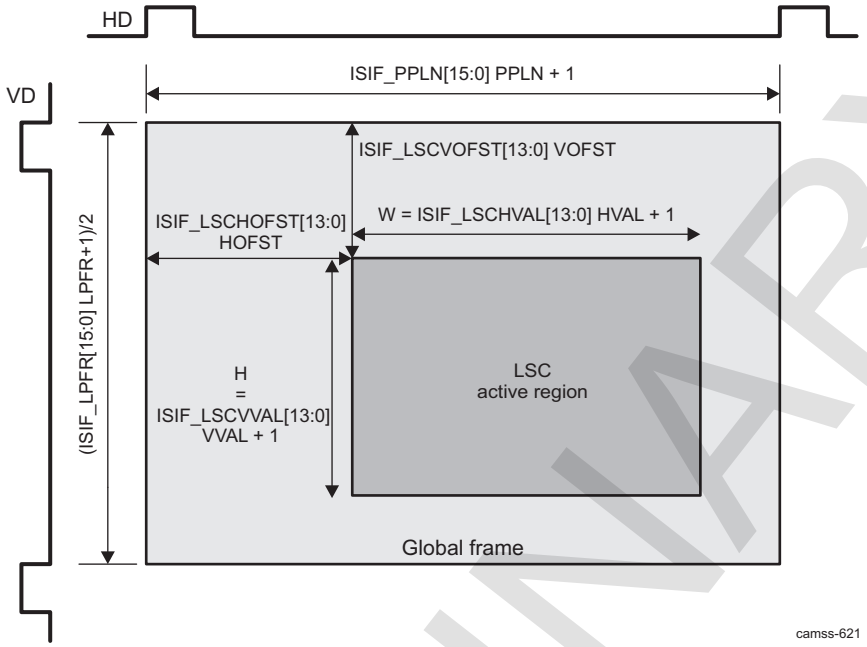
Figure 8-221. ISS ISP ISIF 2D-LSC Active Region for ISIF Input Frame



8.3.3.7.10.1.1 ISS ISP ISIF 2D-LSC Gain and Offset Tables

The gain and offset map are MxN downsampled:

- M is the horizontal sampling factor.
- N is the vertical sampling factor.
- M and N are {8, 16, 32, 64, 128} independently.
- N = M. M is set in the ISIF_2DLSCCFG[14:12] GAIN_MODE_M bit field.
- N is set in the ISIF_2DLSCCFG[10:8] GAIN_MODE_N bit field.

The starting point of the preconfigured lens shading map can be modified in software to align with the ISIF input image frame. The location of the gain and offset mask data in memory is specified by :

- For gain map:
  - Table base address: ISIF_2DLSCGRBU[15:0] BASE31_16 and ISIF_2DLSCGRBL[15:0] BASE15_0
- For offset map:
  - Table base address: ISIF_2DLSCORBU[15:0] BASE and ISIF_2DLSCORBL[15:0] BASE

The input address must be aligned to a 4-byte boundary.

In the full resolution case, the address is set to the beginning of the map. When the LSC active region is defined over a cropped region of the full image, the SDRAM input address can be set to the upper-left corner of the grid closest to the beginning of the active region, and the ISIF_2DLSCINI[6:0] X and ISIF_2DLSCINI[14:8] Y bit fields mark the offset into the upsampled gain and offset map where the active region begins. Figure 8-222 shows the LSC active region with respect to the gain and offset map grid. Because (X, Y) deals with the pixel phase inside a gain and offset map grid, X and Y must each be less than M and N, respectively.

Before applying the gain or offset table, the table is internally upsampled and interpolated back to full resolution via bilinear interpolation.

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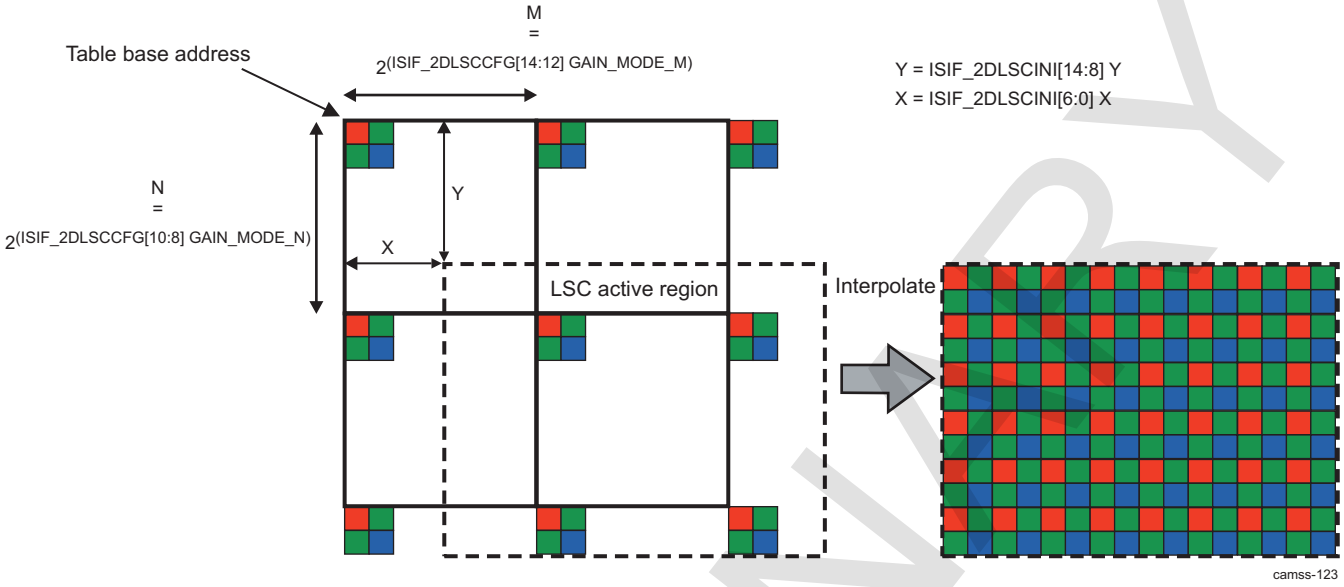
Figure 8-222. ISS ISP ISIF Gain and Offset Mask Upsampling via Bilinear Interpolation



The gain table format is set in the ISIF_2DLSCCFG[3:1] GAIN_FORMAT bit field. 8-bit entries are supported in the gain map (in U8Q8, U8Q7, U8Q6, and U8Q5 format with optional base of 1.0 to shift the range up).

8-bit entries are supported in the offset map (in S8Q0 format). An optional shifting up for offsets is possible. The shift up value is selected through the ISIF_2DLSCOFST[6:4] OFSTSFT bit field. A scaling factor for offsets is defined in the ISIF_2DLSCOFST[15:8] OFSTSF bit field.

The offset control in the 2D-LSC module can be enabled or disabled through the ISIF_2DLSCOFST[0] OFSTEN bit.

For an LSC active region size of W × H (the output and input are the same size), and the gain and offset maps are MxN downsampled, a table with the following values is needed:

- (ceil[(X + W) / M] + 1) x (ceil[(Y + H) / N] + 1) × 4 bytes data in external memory organized as:
  - (ceil[(InitX + W) / M] +1) lines of data
  - Each line having at least (ceil[(InitY + H) / N] + 1) × 4 data points

  Extra data at end of each line can be skipped by the line offset register parameter:
  - For gain map:
    - Line offset: ISIF_2DLSCGROF[15:0] OFFSET
  - For offset map:
    - Line offset: ISIF_2DLSCOROF[15:0] OFFSET
  - Each line offset must start at a 32-bit aligned boundary.

8.3.3.7.10.1.2 ISS ISP ISIF 2D-LSC Gain and Offset Table Upsampling

Upsampling of the pixel-by-pixel gains is performed by locating the four same-color anchors for each destination gain value and applying bilinear interpolation.

The gain and offset mask function is neutral to color pattern. The starting color of the gain and offset mask must be consistent with the starting color of the image, and can be any color. To align starting colors, the X and Y values must be even. The 2D-LSC engine upsamples each phase of the mask data as a separate plane and applies the upsampled mask to the image with the same color phasing. In other words, the red

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gains are interpolated with red gains, and applied to the red input pixels. The same is done for each of the other three colors in the color pattern. The 2D-LSC module is designed to work with Bayer CFA data, having the R/Gr/Gb/B color pattern. For the purpose of functional description, assume red is the starting color, but any other starting color or other 2 × 2 pattern can be used by placing color gains in the appropriate order.

8.3.3.7.10.1.3 ISS ISP ISIF Application of Gain and Offset to Image Pixels

The gain value interpolated for each pixel is multiplied with a corresponding input pixel. An offset is applied before the gain. The product is rounded to the nearest integer and then clipped or saturated to the valid range of 13 bits.

The following equation describes the operation of the LSC in terms of offset and gain:

out[x,y] = (in[x,y] + a*(ofst[x,y] T)) * gain[x,y] (6)

- in[x, y] are the input pixels, 13 bits signed.
- ofst[x, y] are the upsampled offset points.
- T is the upshift value applied to the result of the offset interpolation points (0 – 5) set through the ISIF_2DLSCOFST[6:4] OFSTSFT bit field.
- a is the offset gain value in U8Q7 format set through the ISIF_2DLSCOFST[15:8] OFSTSF bit field.
- gain[x, y] are the upsampled gain points.
- out[x, y] are the resulting output pixels, 13 bits signed.

8.3.3.7.10.1.4 ISS ISP ISIF Enabling/ Disabling the 2D-LSC Module

LSC operates on a single frame or continuously, depending on the firmware programming.

Upon power-on reset (POR), the 2D-LSC module is disabled and input pixels are copied to the output, bypassing any shading operation.

When enabling or disabling the 2D-LSC, caution must be taken on the timing of register modifications. To avoid causing a prefetch error or other unexpected behavior, the following safeguards must be implemented:

1. While configuring the 2D-LSC registers, the input clock into the ISIF should be toggling.
2. All of the 2D-LSC registers must be configured appropriately before enabling the ISIF_2DLSCCFG[0] ENABLE bit.
3. After setting the ENABLE bit to 1, the hardware immediately begins fetching the first two rows of gain and offset data entries from external memory. When this is complete, the ISIF_2DLSCIRQST[2] PREFETCH_COMPETED status flag is set.

NOTE: If the ENABLE bit is disabled before the ISIF_2DLSCIRQST[3] SOF status flag is set, the ISIF_2DLSCIRQST[1] PREFETCH_ERROR flag is set and the state of the 2D-LSC submodule may lead to unexpected errors. Therefore, the ENABLE bit must not be disabled until after the ISIF_2DLSCIRQST[3] SOF status flag is set.

4. Appropriate gains and offsets are applied to the image pixels. Pixels outside the LSC active region are passed through unaltered. When the 2D-LSC operation on the active region completes, the ISIF_2DLSCIRQST[0] DONE status flag is set.
5. At this point:
   - If the ENABLE bit is still set to 1, the hardware immediately begins to prefetch the gain and offset data entries for the next frame and waits for the active region of the next frame to arrive.
   - If the ENABLE bit is set to 0, it stops LSC operation once the active region is passed, and goes into idle until the ENABLE bit is written to 1 again.

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NOTE: To provide a mechanism for firmware to recover from the LSC module waiting indefinitely for the input image, if LSC_ENABLE is written to 0 after it has started gain/offset map prefetching, but before the LSC gets to the next active region, the LSC operation is aborted and turned idle, and any prefetched gain/offset entries are discarded. This can happen before or after the next start-of-frame.

NOTE: Therefore, because of the constraints set in point 3, the ENABLE register bit must be disabled only after the ISIF_2DLSCIRQST[3] SOF status flag is set and before the ISIF_2DLSCIRQST[0] DONE status flag is set for that same frame.

It is suggested that when the 2D-LSC or the whole ISIF needs to be disabled for switching modes, the ISIF_2DLSCIRQST[3] SOF interrupt be enabled so that software knows when it is safe to disable the 2D-LSC. Then the ISIF can be disabled after the ISIF_2DLSCIRQST[0] DONE status signal is set for that frame.

NOTE: The LSC_ENABLE bit, once written to 1, must not be cleared until at least one vpi_clk clock cycle after start-of-frame, to ensure correct processing.

8.3.3.7.10.1.5 ISS ISP ISIF 2D-LSC Events and Status Checking

The 2D-LSC submodule can generate events on a single interrupt line. These events are further remapped at the ISP level in ISP5_IRQENABLE_SET__0.ISIF_INT_3 - ISP5_IRQENABLE_SET__3.ISIF_INT3.

Four 2D-LSC events can be generated:

- DONE: LSC done. This event triggers when the LSC submodules transition from ACTIVE state to IDLE state.
- PREFETCH_ERROR: Gain table prefetch error. This event triggers when the tables stored in SDRAM are read too slowly. After this event is asserted, the LSC disables the LSC computation until the beginning of the next frame.
- PREFETCH_COMPLETE: Gain table prefetch complete. This event triggers when data prefetching from SDRAM completes. Data prefetching must complete by the time the first pixel of a frame comes. The event triggers when the buffer contains three full rows of data.
- SOF: This event signals the start of the LSC valid region. The LSC configuration registers for the next frame can be updated after the LSC SOF triggers.

The ISIF_2DLSCIRQEN register can be configured to select which events are masked and which are propagated to the LSC interrupt signal. The ISIF_2DLSCIRQST register can be read and cleared to identify which events have occurred.

In addition, the 2D-LSC module provides the following status bit:

- BUSY: This indicates that LSC has entered the active region vertically. This bit remains on during horizontal blanking, and turns off only after the entire active region of the current frame is processed.

8.3.3.7.10.1.6 ISS ISP ISIF Supported On-the-Fly 2D-LSC Configurations

The 2D-LSC prefetch memory is equal to 2 × 1536 × 32 bits. This memory is sized to fetch three lines of 8-bit gain and 8-bit offset × four color components per paxel. Given an image sensor of horizontal resolution H, there are floor [(H / ISIF_2DLSCCFG[14:12] GAIN_MODE_M) + 1] paxels per line, where M is the horizontal LSC paxel size.

Table 8-345 shows the LSC horizontal paxel size, which can be supported for different image sensor resolutions. When M = 8, some resolutions cannot be supported on the fly (orange-shaded cells in the table); the way to process such large images is to use vertical frame division.

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Table 8-345. ISS ISP ISIF Supported On-the-Fly LSC Configurations

MPix	Aspect Ratio		Line Size	Horizontal LSC Paxel Size: M = 2[ISIF_2DLSCCFG[14:12] GAIN_MODE_M]				
				8	16	32	64	128
Maximum	–	–	5376	2019	1011	507	255	129
16	16	9	5333	2003	1003	503	253	128
16	4	3	4619	1735	869	436	220	111
16	3	2	4899	1840	922	462	233	118
12	16	9	4619	1735	869	436	220	111
12	4	3	4000	1503	753	378	191	97
12	3	2	4243	1594	798	401	202	102
10	16	9	4216	1584	794	398	201	102
10	4	3	3651	1372	688	345	174	89
10	3	2	3873	1455	729	366	185	94
8	16	9	3771	1417	710	357	180	91
8	4	3	3266	1228	615	309	156	80
8	3	2	3464	1302	653	328	165	84

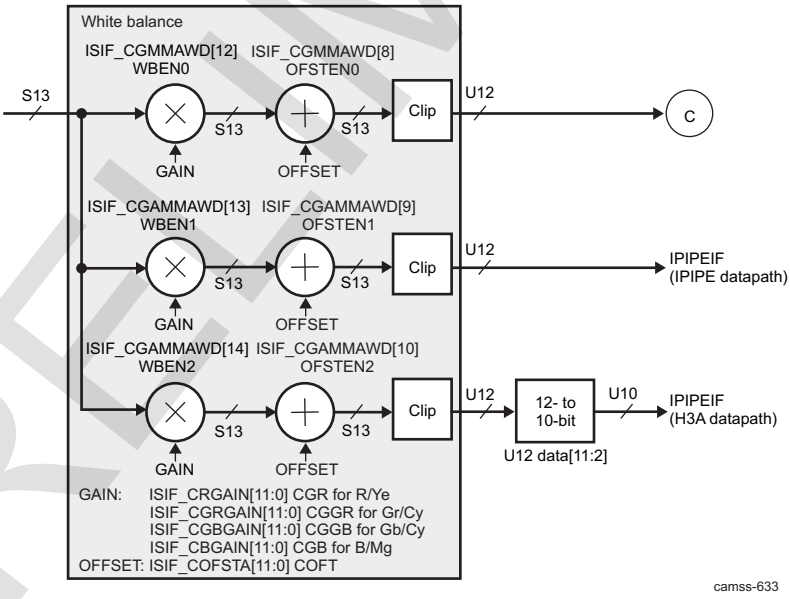
8.3.3.7.10.1.7 ISS ISP ISIF Bandwidth Requirements on BL Read Port

See Section 8.3.3.7.18.2 for details.

8.3.3.7.11 ISS ISP ISIF White Balance

Figure 8-223 shows the white balance block diagram.

Figure 8-223. ISS ISP ISIF White Balance Block Diagram



Color pattern settings are set through the ISIF_CCOLP register. Moreover, through this register the pixel position from 0 to 3 can be set to the needed Bayer universal camera filter color pattern (RGB/CYGM).

The CFA pattern can be in two modes, stripe or mosaic, and is set through the ISIF_CGAMMAWD[5] CFAP bit.

There are color-dependent gain controls for the three outputs: BL output, IPIPEIF (IPIPE path) output, and IPIPEIF (H3A path) output. Gain applied to each data is selected according to the pixel position and the color pattern settings. Gain factors are common for the three data paths. Gain is in U11Q9 format, which ranges from 0 to 3 + 511/512. The gain factor is set through the following registers:

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- R/Ye gain: ISIF_CRGAIN[11:0] CGR
- Gr/Cy gain: ISIF_CGRGAIN[11:0] CGGR
- Gb/Cy gain: ISIF_CGBGAIN[11:0] CGGB
- B/Mg gain: ISIF_CBGAIN[11:0] CGB

Gain control can be enabled or disabled individually for each path.

- Enable or disable gain for the BL path: ISIF_CGAMMAWD[12] WBEN0.
- Enable or disable gain for the IPIPEIF (IPIPE) path: ISIF_CGAMMAWD[13] WBEN1.
- Enable or disable gain for the IPIPEIF (H3A) path: ISIF_CGAMMAWD[14] WBEN2.

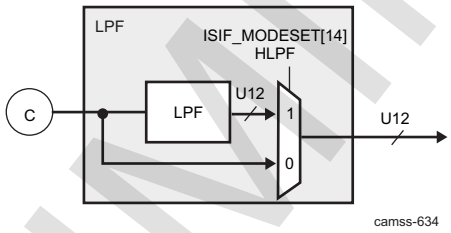
After the gain control, a single offset value can be added to each path individually. This offset is common for the three paths and is set through the ISIF_COFSTA[11:0] COFT bit field. The offset value is U12, which ranges from 0 to 4095. Data (S13) are then truncated to U12.

- Enable or disable offset for the BL path: ISIF_CGAMMAWD[8] OFSTEN0.
- Enable or disable offset for the IPIPEIF (IPIPE) path: ISIF_CGAMMAWD[9] OFSTEN1.
- Enable or disable offset for the IPIPEIF (H3A) path: ISIF_CGAMMAWD[10] OFSTEN2.

8.3.3.7.12 ISS ISP ISIF Low-Pass Filter (LPF)

Figure 8-224 shows the low-pass filter block diagram.

Figure 8-224. ISS ISP ISIF Low-Pass Filter Block Diagram



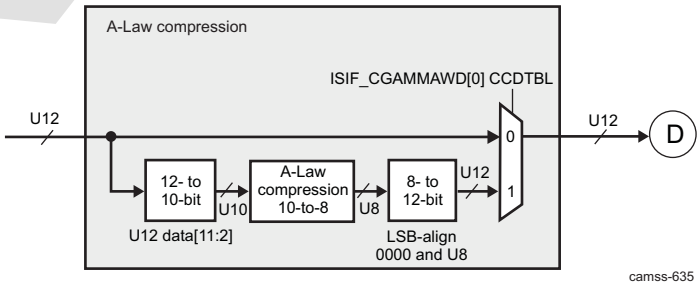
An optional horizontal low-pass anti-aliasing filter (LPF) can be applied (the ISIF_MODESET[14] HLPF bit) after reframing. The low-pass filter consists of a simple 3-tap (1/4, 1/2, and 1/4) filter. Two pixels on the left and two pixels on the right of each line are cropped if the filter is enabled. Use of the LPF is intended for bandwidth reduction if culling is enabled.

NOTE: For YUV data, the LPF must be disabled (ISIF_MODESET[14] HLPF = 0x0).

8.3.3.7.13 ISS ISP ISIF A-Law Compression

Figure 8-225shows the A-Law compression block diagram.

Figure 8-225. ISS ISP ISIF A-Law Compression Block Diagram



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An optional 10-to-8-bit A-Law compression using a fixed A-Law table can be applied (ISIF_CGAMMAWD[0] CCDTBL) as the final processing stage. Using this compression causes the data width to be reduced to 8 bits and allows packing to 8 bits/pixel when saving to memory. Because data resolution can be greater than 10 bits at this stage, the 10 bits for input to the A-Law operation must be selected (ISIF_CGAMMAWD[4:1] GWDI).

The IPIPEIF module has an inverse A-Law table (A-Law decompression) option so that this nonlinear operation can be reversed if this saved data is to be read back in for further processing.

NOTE: Do not use A-Law compression (ISIF_CGAMMAWD[0] CCDTBL = 0) with YUV data.

Figure 8-226 shows the A-Law table diagram, and Figure 8-227 shows the A-Law table values.

Figure 8-226. ISS ISP ISIF A-Law Table Diagram

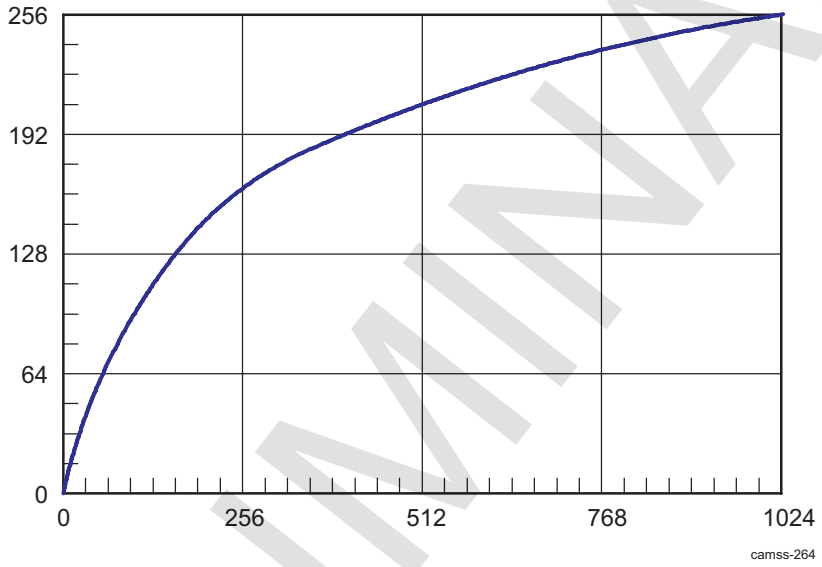

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Figure 8-227. ISS ISP ISIF A-Law Table Values

Input	A-Law	Input	A-Law	Input	A-Law	Input	A-Law	Input	A-Law	Input	A-Law	Input	A-Law	Input	A-Law
0	0	64	64	128	112	192	140	256	161	320	176	384	189	448	200
1	1	65	65	129	113	193	141	257	161	321	176	385	189	449	200
2	2	66	66	130	113	194	141	258	161	322	177	386	189	450	200
3	3	67	67	131	114	195	142	259	161	323	177	387	189	451	200
4	4	68	68	132	114	196	142	260	162	324	177	388	190	452	200
5	5	69	69	133	115	197	142	261	162	325	177	389	190	453	200
6	6	70	70	134	115	198	143	262	162	326	177	390	190	454	201
7	7	71	71	135	116	199	143	263	162	327	178	391	190	455	201
8	8	72	72	136	116	200	143	264	163	328	178	392	190	456	201
9	9	73	73	137	117	201	144	265	163	329	178	393	190	457	201
10	10	74	74	138	117	202	144	266	163	330	178	394	191	458	201
11	11	75	75	139	118	203	144	267	163	331	178	395	191	459	201
12	12	76	76	140	118	204	145	268	164	332	179	396	191	460	201
13	13	77	77	141	119	205	145	269	164	333	179	397	191	461	202
14	14	78	78	142	119	206	145	270	164	334	179	398	191	462	202
15	15	79	78	143	120	207	146	271	164	335	179	399	191	463	202
16	16	80	79	144	120	208	146	272	165	336	179	400	192	464	202
17	17	81	80	145	121	209	146	273	165	337	180	401	192	465	202
18	18	82	81	146	121	210	147	274	165	338	180	402	192	466	202
19	19	83	82	147	122	211	147	275	166	339	180	403	192	467	202
20	20	84	83	148	122	212	147	276	166	340	180	404	192	468	203
21	21	85	84	149	123	213	148	277	166	341	181	405	193	469	203
22	22	86	84	150	123	214	148	278	166	342	181	406	193	470	203
23	23	87	85	151	124	215	148	279	167	343	181	407	193	471	203
24	24	88	86	152	124	216	149	280	167	344	181	408	193	472	203
25	25	89	87	153	125	217	149	281	167	345	181	409	193	473	203
26	26	90	88	154	125	218	149	282	167	346	182	410	193	474	204
27	27	91	88	155	125	219	150	283	168	347	182	411	194	475	204
28	28	92	89	156	126	220	150	284	168	348	182	412	194	476	204
29	29	93	90	157	126	221	150	285	168	349	182	413	194	477	204
30	30	94	91	158	127	222	151	286	168	350	182	414	194	478	204
31	31	95	91	159	127	223	151	287	168	351	183	415	194	479	204
32	32	96	92	160	128	224	151	288	169	352	183	416	194	480	204
33	33	97	93	161	128	225	152	289	169	353	183	417	195	481	205
34	34	98	93	162	129	226	152	290	169	354	183	418	195	482	205
35	35	99	94	163	129	227	152	291	169	355	183	419	195	483	205
36	36	100	95	164	129	228	152	292	170	356	184	420	195	484	205
37	37	101	96	165	130	229	153	293	170	357	184	421	195	485	205
38	38	102	96	166	130	230	153	294	170	358	184	422	195	486	205
39	39	103	97	167	131	231	153	295	170	359	184	423	196	487	205
40	40	104	98	168	131	232	154	296	171	360	184	424	196	488	206
41	41	105	98	169	132	233	154	297	171	361	185	425	196	489	206
42	42	106	99	170	132	234	154	298	171	362	185	426	196	490	206
43	43	107	100	171	132	235	155	299	171	363	185	427	196	491	206
44	44	108	100	172	133	236	155	300	172	364	185	428	196	492	206
45	45	109	101	173	133	237	155	301	172	365	185	429	197	493	206
46	46	110	102	174	134	238	155	302	172	366	185	430	197	494	206
47	47	111	102	175	134	239	156	303	172	367	186	431	197	495	207
48	48	112	103	176	134	240	156	304	173	368	186	432	197	496	207
49	49	113	103	177	135	241	156	305	173	369	186	433	197	497	207
50	50	114	104	178	135	242	157	306	173	370	186	434	197	498	207
51	51	115	105	179	136	243	157	307	173	371	186	435	198	499	207
52	52	116	105	180	136	244	157	308	173	372	187	436	198	500	207
53	53	117	106	181	136	245	157	309	174	373	187	437	198	501	207
54	54	118	106	182	137	246	158	310	174	374	187	438	198	502	208
55	55	119	107	183	137	247	158	311	174	375	187	439	198	503	208
56	56	120	108	184	137	248	158	312	174	376	187	440	198	504	208
57	57	121	108	185	138	249	159	313	175	377	188	441	198	505	208
58	58	122	109	186	138	250	159	314	175	378	188	442	199	506	208
59	59	123	109	187	139	251	159	315	175	379	188	443	199	507	208
60	60	124	110	188	139	252	159	316	175	380	188	444	199	508	208
61	61	125	110	189	139	253	160	317	175	381	188	445	199	509	208
62	62	126	111	190	140	254	160	318	176	382	188	446	199	510	209
63	63	127	112	191	140	255	160	319	176	383	189	447	199	511	209

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Input	A-Law	Input	A-Law	Input	A-Law	Input	A-Law	Input	A-Law	Input	A-Law	Input	A-Law	Input	A-Law
512	209	576	217	640	224	704	231	768	237	832	243	896	248	960	253
513	209	577	217	641	225	705	231	769	237	833	243	897	248	961	253
514	209	578	217	642	225	706	231	770	237	834	243	898	248	962	253
515	209	579	217	643	225	707	231	771	237	835	243	899	248	963	253
516	209	580	218	644	225	708	232	772	238	836	243	900	248	964	253
517	210	581	218	645	225	709	232	773	238	837	243	901	248	965	253
518	210	582	218	646	225	710	232	774	238	838	243	902	248	966	253
519	210	583	218	647	225	711	232	775	238	839	243	903	249	967	253
520	210	584	218	648	225	712	232	776	238	840	243	904	249	968	253
521	210	585	218	649	225	713	232	777	238	841	244	905	249	969	253
522	210	586	218	650	226	714	232	778	238	842	244	906	249	970	254
523	210	587	218	651	226	715	232	779	238	843	244	907	249	971	254
524	211	588	219	652	226	716	232	780	238	844	244	908	249	972	254
525	211	589	219	653	226	717	232	781	238	845	244	909	249	973	254
526	211	590	219	654	226	718	233	782	238	846	244	910	249	974	254
527	211	591	219	655	226	719	233	783	239	847	244	911	249	975	254
528	211	592	219	656	226	720	233	784	239	848	244	912	249	976	254
529	211	593	219	657	226	721	233	785	239	849	244	913	249	977	254
530	211	594	219	658	226	722	233	786	239	850	244	914	249	978	254
531	211	595	219	659	227	723	233	787	239	851	244	915	249	979	254
532	212	596	220	660	227	724	233	788	239	852	244	916	250	980	254
533	212	597	220	661	227	725	233	789	239	853	245	917	250	981	254
534	212	598	220	662	227	726	233	790	239	854	245	918	250	982	254
535	212	599	220	663	227	727	233	791	239	855	245	919	250	983	254
536	212	600	220	664	227	728	233	792	239	856	245	920	250	984	255
537	212	601	220	665	227	729	234	793	239	857	245	921	250	985	255
538	212	602	220	666	227	730	234	794	240	858	245	922	250	986	255
539	212	603	220	667	227	731	234	795	240	859	245	923	250	987	255
540	213	604	220	668	227	732	234	796	240	860	245	924	250	988	255
541	213	605	221	669	228	733	234	797	240	861	245	925	250	989	255
542	213	606	221	670	228	734	234	798	240	862	245	926	250	990	255
543	213	607	221	671	228	735	234	799	240	863	245	927	250	991	255
544	213	608	221	672	228	736	234	800	240	864	245	928	250	992	255
545	213	609	221	673	228	737	234	801	240	865	246	929	250	993	255
546	213	610	221	674	228	738	234	802	240	866	246	930	251	994	255
547	214	611	221	675	228	739	235	803	240	867	246	931	251	995	255
548	214	612	221	676	228	740	235	804	240	868	246	932	251	996	255
549	214	613	221	677	228	741	235	805	240	869	246	933	251	997	255
550	214	614	222	678	229	742	235	806	241	870	246	934	251	998	255
551	214	615	222	679	229	743	235	807	241	871	246	935	251	999	255
552	214	616	222	680	229	744	235	808	241	872	246	936	251	1000	255
553	214	617	222	681	229	745	235	809	241	873	246	937	251	1001	255
554	214	618	222	682	229	746	235	810	241	874	246	938	251	1002	255
555	215	619	222	683	229	747	235	811	241	875	246	939	251	1003	255
556	215	620	222	684	229	748	235	812	241	876	246	940	251	1004	255
557	215	621	222	685	229	749	235	813	241	877	246	941	251	1005	255
558	215	622	222	686	229	750	236	814	241	878	247	942	251	1006	255
559	215	623	223	687	229	751	236	815	241	879	247	943	252	1007	255
560	215	624	223	688	230	752	236	816	241	880	247	944	252	1008	255
561	215	625	223	689	230	753	236	817	242	881	247	945	252	1009	255
562	215	626	223	690	230	754	236	818	242	882	247	946	252	1010	255
563	216	627	223	691	230	755	236	819	242	883	247	947	252	1011	255
564	216	628	223	692	230	756	236	820	242	884	247	948	252	1012	255
565	216	629	223	693	230	757	236	821	242	885	247	949	252	1013	255
566	216	630	223	694	230	758	236	822	242	886	247	950	252	1014	255
567	216	631	223	695	230	759	236	823	242	887	247	951	252	1015	255
568	216	632	224	696	230	760	236	824	242	888	247	952	252	1016	255
569	216	633	224	697	230	761	237	825	242	889	247	953	252	1017	255
570	216	634	224	698	231	762	237	826	242	890	247	954	252	1018	255
571	217	635	224	699	231	763	237	827	242	891	248	955	252	1019	255
572	217	636	224	700	231	764	237	828	242	892	248	956	252	1020	255
573	217	637	224	701	231	765	237	829	243	893	248	957	253	1021	255
574	217	638	224	702	231	766	237	830	243	894	248	958	253	1022	255
575	217	639	224	703	231	767	237	831	243	895	248	959	253	1023	255

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8.3.3.7.14 ISS ISP ISIF Culling

Figure 8-228 shows the culling block diagram.

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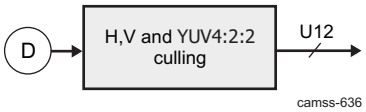
Figure 8-228. ISS ISP ISIF Culling Block Diagram



The culling block performs a programmable decimation function for horizontal, vertical, and YUV4:2:2 data directions. The horizontal and vertical decimation of image data can be controlled by two registers.

The horizontal culling operation allows selected pixel data to be culled (deleted) from a line. The ISIF_CULH register specifies the horizontal culling pattern for even and odd lines:

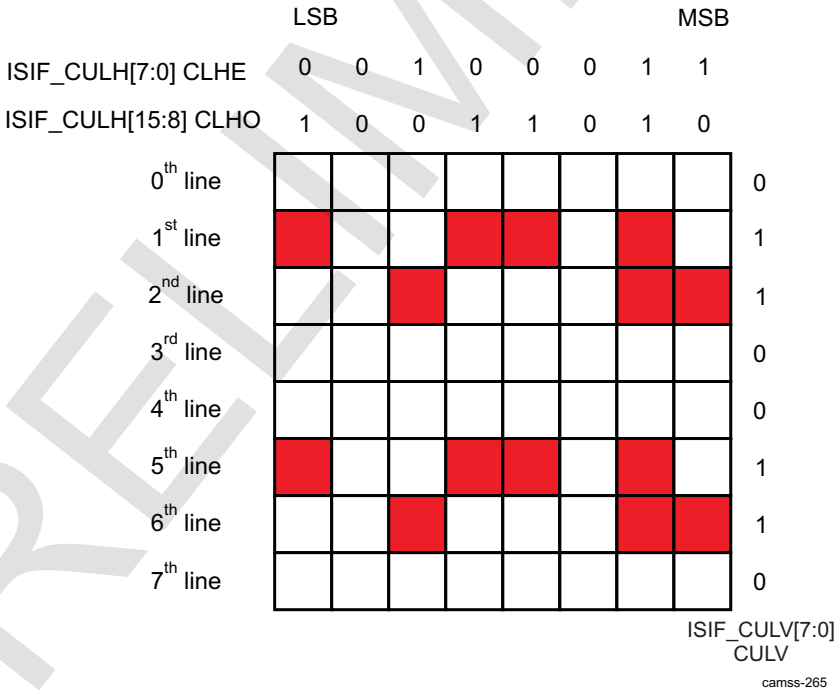
- Even lines: ISIF_CULH[15:8] CLHE
- Odd lines: ISIF_CULH[16:0] CLHO

The vertical culling operation allows selected lines to be culled from a frame. The ISIF_CULV register specifies the pattern for the vertical direction. The LSBs of CULV represent the top line of the CCD; the MSB is the seventh line.

Figure 8-229 is an example of how register values apply the decimation pattern to the data. The red pixels are saved to memory and the white pixels are discarded. In this example, CULH = 0x59C4 and CULV = 0x0066.

NOTE: Culling can be used with YUV data, but care must be taken to preserve the YUV4:2:2 output format.

Figure 8-229. ISS ISP ISIF Example for Decimation Pattern



8.3.3.7.15 ISS ISP ISIF 12-to-8 bit DCPM Compression Block

In ISIF, there is a DPCM compression block, which is between the culling module and the storage formatter module. This block can compress 12-bit image data to 8 bits for bandwidth reduction in transmission between the ISIF and SDRAM. An 8- to-12-bit DPCM decoder at the IPIPEIF decompresses data for IPIPE processing.

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Two different predictors are used for the compression system. The first predictor is simple (simple predictor), and the second predictor is slightly more complex (advanced predictor). Because the advanced predictor gives a slightly better prediction for the pixel value, the image quality can be improved using it. Because the simple predictor is very simple, the processing power and memory requirements are reduced using it, when the image quality is already sufficiently high.

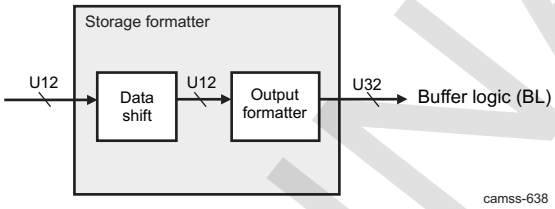
- Advanced predictor: This predictor uses only the previous same color component value as a prediction value. Therefore, only 2-pixel memory is required.
- This predictor uses four previous pixel values when the prediction value is evaluated. This means that the other color component values are also used when the prediction value has been defined.

The function is controlled from the ISIF_MISC[12] DPCMEN and ISIF_MISC[13] DPCMPRE bits.

8.3.3.7.16 ISP ISIF Storage Formatter

Figure 8-230 shows the storage formatter block diagram.

Figure 8-230. ISS ISP ISIF Storage Formatter Block Diagram



Data are stored to the lower bits of a 16-bit SDRAM word, or can be 8- or 12-bit packed. The ISIF_HSIZE[11:0] HSIZE bit field can specify the memory address offsets between lines of memory (offset in 32-byte units). If set, the ISIF_HSIZE[12] ADCR bit can decrement the memory address line and the line can be horizontally flipped in memory.

In case of RAW data, a data shift module is used: data to be stored can be right-shifted according to the value set at the ISIF_MODESET[10:8] CCDW bit field, as described in Table 8-346.

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Table 8-346. ISS ISP ISIF RAW Data Shifting

ISIF_MODESET[10:8] CCDW	Output Format	
	MSB	LSB
000	0000 U12 data[11:0]	
001	00000 U12 data[11:1]	
010	000000 U12 data[11:2]	
011	0000000 U12 data[11:3]	
100	00000000 U12 data[11:4]	

Table 8-347 shows the format where data are stored to the lower bits of a 16-bit word and the format where data are packed to 8 bits. The unused bits are filled with zeros.

Table 8-347. ISS ISP ISIF SDRAM Data Format

	Upper Word		Lower Word	
	MSB(31)	LSB(16)	MSB(15)	LSB(0)
12 bit	0	Pixel 1	0	Pixel 0
11 bit	0	Pixel 1	0	Pixel 0
10 bit	0	Pixel 1	0	Pixel 0
9 bit	0	Pixel 1	0	Pixel 0
8 bit	0	Pixel 1	0	Pixel 0
8-bit packed	Pixel 3	Pixel 2	Pixel 1	Pixel 0

Table 8-348 shows the format where data are packed to 12 bits.

Table 8-348. ISS ISP ISIF SDRAM Data Format for 12-bit Packed

	Upper Word		Lower Word	
	MSB(31)	LSB(16)	MSB(15)	LSB(0)
12 bit	Pixel2[7:0]	Pixel1	Pixel 0	
	Pixel5[3:0]	Pixel4	Pixel3	Pixel2[11:8]
	Pixel7	Pixel6	Pixel5[11:4]	

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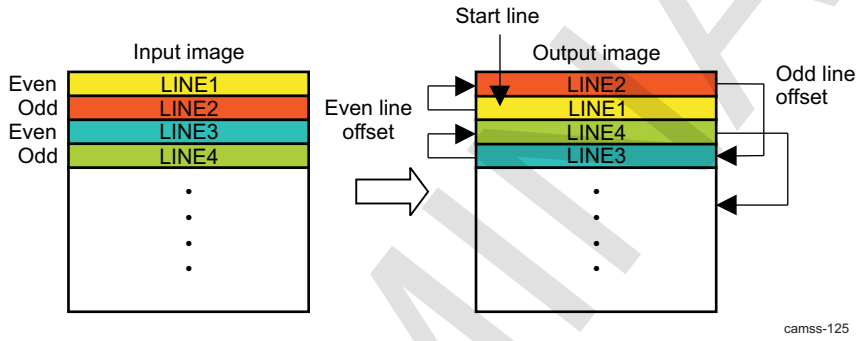
In case of YUV, YUV data is stored in memory in packed YUV4:2:2 mode, using 2 pixels per 32 bits, as shown in Table 8-349.

The output formatter can configure to any image format by using the SDRAM line offset register and offset control registers. Figure 8-231 shows how to construct a frame format in SDRAM. The ISIF_CADU[10:0] CADU bit field specifies the memory destination (upper 11 bits) to SDRAM (the address is the value of the set bit multiplied by 32 bytes). On the other hand, the ISIF_CADL[15:0] CADL bit field sets the memory destination to SDRAM (lower 16 bits) (the address is the value of the set bit multiplied by 32 bytes).

- ISIF_SPH
- ISIF_LNH
- ISIF_SLV0
- ISIF_SLV1
- ISIF_LNV

Figure 8-231. ISS ISP ISIF Frame Image Format Conversion



8.3.3.7.17 ISS ISP ISIF YCbCr signal Processing

The ISIF accepts 4:2:2 sampled YCbCr input data. The luminance and color difference signals are 8 bits each, scaled 0 to 255. The color difference signals are multiplexed into one 8-bit bus beginning with a Cb sample. The Y and CbCr buses can be input parallel (16-bit mode) or be time-multiplexed and input as a single bus (8-bit mode).

The 16- or 8-bit YCbCr data is stored in SDRAM as 4:2:2 format. Table 8-349 lists the data format in SDRAM. Y data typically has a range of 16 to 235; however, it is possible to subtract a DC value from the Y signal.

Table 8-349. ISS ISP ISIF Memory Output Format for YUV Data

Memory Address	Upper Word		Lower Word	
	MSB(31)	LSB(16)	MSB(15)	LSB(0)
N	Y1	Cr0	Y0	Cb0
N + 1	Y3	Cr1	Y2	Cb1
N + 2	Y5	Cr2	Y4	Cb2

8.3.3.7.18 ISS ISP ISIF Expected Bandwidth on BL Ports

The ISIF module has a write port and a read port connected to the BL. This section summarizes the expected bandwidth on these ports.

8.3.3.7.18.1 ISS ISP ISIF Write Port

The write port is used to write pixels to memory after the data have passed through the storage formatter. Data storage to SDRAM is controlled by the ISIF_SYNCEN[1] DWEN bit. The module allows writing the data as 16, 12, and 8 bits per pixel. The bit width is controlled by the ISIF_CCDCFG[1:0] SDRPACK bit field.

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The write port generates a burst of 32 bytes on the MTC interface. The delay between consecutive bursts is proportional to the input pixel clock. Hence, the write port does not request peak bandwidth traffic.

Table 8-350 lists the estimated delay between 32-byte MTC requests for different pixel clock frequencies and assumes the L3 clock is 200 MHz.

Table 8-350. ISP ISIF ISIF Module: Write Port Bandwidth

Pixel Clock	Maximum Bandwidth 2 bytes/s pixel MB/s	Expected Delay Between MTC Requests
200	400	16 cycles = 80 ns
100	200	32 cycles = 160 ns
10	20	320 cycles = 1600 ns

8.3.3.7.18.2 ISS ISP ISIF Read Port

The read port is used to read gain and offset data from SDRAM required for the LSC computation. When LSC is enabled, 8-bit gain values are read and 8-bit offset values can optionally also be read. The LSC gain computation can be enabled or disabled by setting the ISIF_2DLSCCFG[0] ENABLE bit. The LSC offset computation can be enabled by setting the ISIF_2DLSCOFST[0] OFSTEN bit.

The LSC submodule fetches four 8-bit gain values per paxel and optionally four 8-bit offset values per paxel. This is a maximum 8 bytes per paxel.

The bandwidth that is generated by the LSC module is also proportional to the paxel size. The paxel size is set up by the ISIF_2DLSCCFG[14:12] GAIN_MODE_M and ISIF_2DLSCCFG[10:8] GAIN_MODE_N bit fields. The possible values are 8, 16, 32, 64 and 128. Smaller values lead to higher memory bandwidth requirements. Hence, the worst case is achieved by setting an 8 × 8 paxel size.

When the LSC submodule is enabled it automatically prefetches two lines of gain values and two lines of offset values (if this is enabled). When the first VD comes, it again requests one line of gain values and one line of offset values (if this is enabled). Then, it again fetches one line of gain values and one line of offset values (if this is enabled) after ISIF_2DLSCCFG[10:8] GAIN_MODE_N lines. It continues to do so until the last row of paxels. For the last row of paxels, it fetch two lines of gain values and two lines of offset values (if this is enabled), which are used for the following frame.

By default, the LSC submodule creates peak bandwidth requirements. To avoid this, the MTC bandwidth limiter must be used to space the request over time.

The MTC bandwidth limiter must be used to smooth the bandwidth requirements of the LSC module. The MTC bandwidth limiter can be set with the ISP5_BL_MTC_1.ISIF_R register.

The principle is that instead of reading the gain and offset data as fast as possible, use the time that it takes for ISIF_2DLSCCFG[10:8] GAIN_MODE_N lines to pass through the ISP to read the data.

Table 8-351 gives the estimated delay between 32-byte MTC requests for different pixel clock frequencies and assumes the L3 clock at 200 MHz.

Table 8-351. ISS ISP ISIF Read Port Bandwidth

Pixel Clock	Max Bandwidth MB/s	Expected Delay Between MTC Requests
200	25.07	255 cycles = 1275 ns
100	12.5	510 cycles = 2550 ns
10	1.25	5103 cycles = 2515 ns

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When the bandwidth limiter is used, ensure that there is enough time for the data prefetching.

- The LSC submodule must be enabled at least 2 × ISIF_2DLSCCFG[10:8] GAIN_MODE_N lines before the first VD.
- There must be at least ISIF_2DLSCCFG[10:8] GAIN_MODE_N lines of blanking. If there is not enough blanking, multiply the bandwidth requirement by 2 (that is, ensure two lines of gain and offset data can be fetched within the time of ISIF_2DLSCCFG[10:8] GAIN_MODE_N lines.

8.3.3.7.19 ISS ISP ISIF Events and Status Checking

The ISIF module can generate four different interrupts: VDINT0, VDINT1, VDINT2, and 2DLSCINT. The ISIF_SYNCEN[0] SYEN bit must be enabled to receive any of the ISIF interrupts.

8.3.3.7.19.1 ISS ISP ISIF VDINT0, VDINT1, and VDINT2 Interrupts

As shown in Figure 8-232, the VDINT0, VDINT1, and VDINT2 interrupts occur relative to the VD pulse. The trigger timing is selected by using the ISIF_MODESET[2] VDPOL bit setting. VDINT0, VDINT1, and VDINT2 occur after receiving the number of horizontal lines (HD pulse signals) set in the ISIF_VDINT0[14:0] CDV0, ISIF_VDINT1[14:0] CDV1, and ISIF_VDINT2[14:0] CDV2 register fields, respectively.

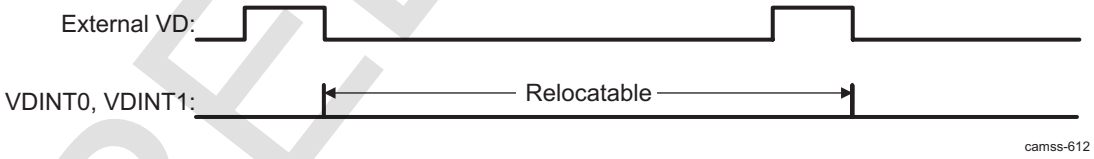
NOTE: In the case of BT.656 input mode, there is a VD at the beginning of each field. Therefore, there are two interrupts for each frame (that is, one for each field).

If the ISIF_MODESET[2] VDPOL bit is set to 0, the VDINT0, VDINT1, and VDINT2 HD counters begin counting HD pulses from the rising edge of the external VD.

Figure 8-232. ISS ISP ISIF VDINT0/VDINT1/VDINT2 Interrupt Behavior When VDPOL = 0

If the ISIF_MODESET[2] VDPOL bit is set to 1, the VDINT0, VDINT1, and VDINT2 HD counters begin counting HD pulses from the falling edge of the external VD.

Figure 8-233. ISS ISP ISIF VDINT0/VDINT1/VDINT2 Interrupt Behavior When VDPOL = 1



8.3.3.7.19.2 ISS ISP ISIF 2DLSCINT Interrupt

See Section 8.3.3.7.10.1.5 for more information.

8.3.3.7.19.3 ISS ISP ISIF Status Checking

The ISIF_MODESET[15] MDFS bit is set when the field status is on an even field, and it is cleared when the field status is on an odd field.

The 2D-LSC has a register that monitors the status of the LSC. See Section 8.3.3.7.10.1.5 for more information.

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8.3.3.8 ISS ISP BL Functional Description

8.3.3.8.1 ISS ISP BL Overview

The BL module arbitrates and merges the memory requests of the ISP master module. The BL module also generates interrupts upon frame completion for the following modules. The interrupt generation is delayed until the transfer completes (ack is returned). The following interrupts are delayed by the BL module:

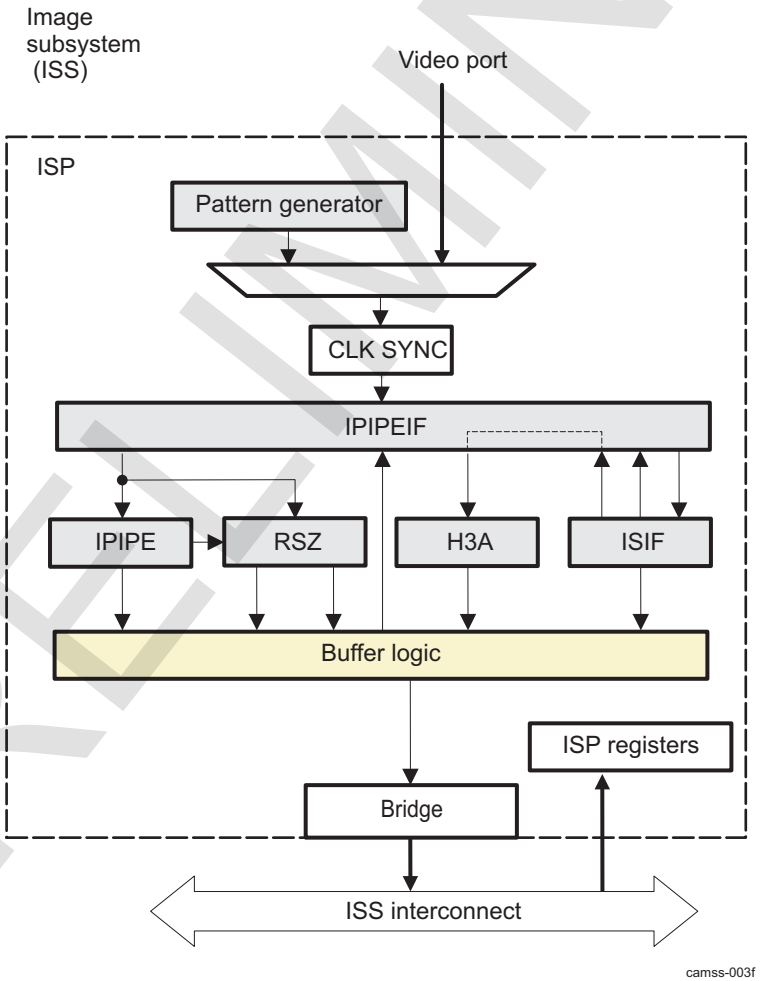
- RSZ module RSZ-A EOF
- RSZ module resizer RSZ-B EOF
- H3A module EOF
- IPIPE module EOF

The BL uses two different types of interfaces:

- MTC protocol is used between the ISP modules and the BL.
- VBUSM is use on the BL master port interface.

Figure 8-234 show the BL module connections to other submodules of the ISP.

Figure 8-234. ISS ISP BL High-Level Diagram



8.3.3.8.2 ISS ISP BL Functional Description

The BL merges the memory requests of the ISP master module to memory (read/write). The BL interfaces with all the ISP modules through a 32-bit-wide bus following.

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The ISP modules make memory requests of 32 bytes. Additional signals, SOF for read and EOF for write, are included to deal with boundary conditions in frame transitions.

The BL arbitration is divided into two parts: a bus hog and a fixed priority arbitration. Bus hog refers to the property of the buffer logic that gives higher priority to the module that last sent or received data. RESIZER module MTC write port 0 and RESIZER module MTC write port 1 are excluded from the bus hog.

The buffer logic is to be programmed to maximize the memory bandwidth: it makes maximum burst requests of 128 bytes (8 × 128 bits) for reads and writes. The BL can generate burst sizes of 2 × 128, 4 × 128, 6 × 128, and 8 × 128 bits.

NOTE: The ISP interface supports burst sizes of only 1, 2, 4, and 8 × 128 bits. If the BL generates a 6 × 128-bit request, it is broken into a 4 × 128-bit request, followed by another 2 × 128-bit request.

To use the memory bandwidth efficiently, the BL interfaces with the memory through a high-bandwidth bus (128 bits wide).

The BL handles memory requests for the following modules:

- IPIPEIF module read port
- ISIF-LSC module read port
- ISIF module write port
- IPIPE-BOXCAR module write port
- H3A module write port
- RESIZER module write port 0
- RESIZER module write port 1

From a use case point of view, the following sharing and priority arrangement is used. All reads have higher priority than writes; for reads: IPIPEIF ISIF-LSC, and for writes: ISIF IPIPE-BOXCAR RESIZER 0 RESIZER 1 H3A.

NOTE: BL can generate a static or a dynamic MFlag signal. The MFlag signal is used by the ISS arbitration to consider the urgency of the requests coming from the ISP. The dynamic MFlag feature is enabled from the ISP5_CTRL[21] MFLAG bit.

Figure 8-235 shows the BL top-level block diagram. The figure highlights the two clock domains that are used.

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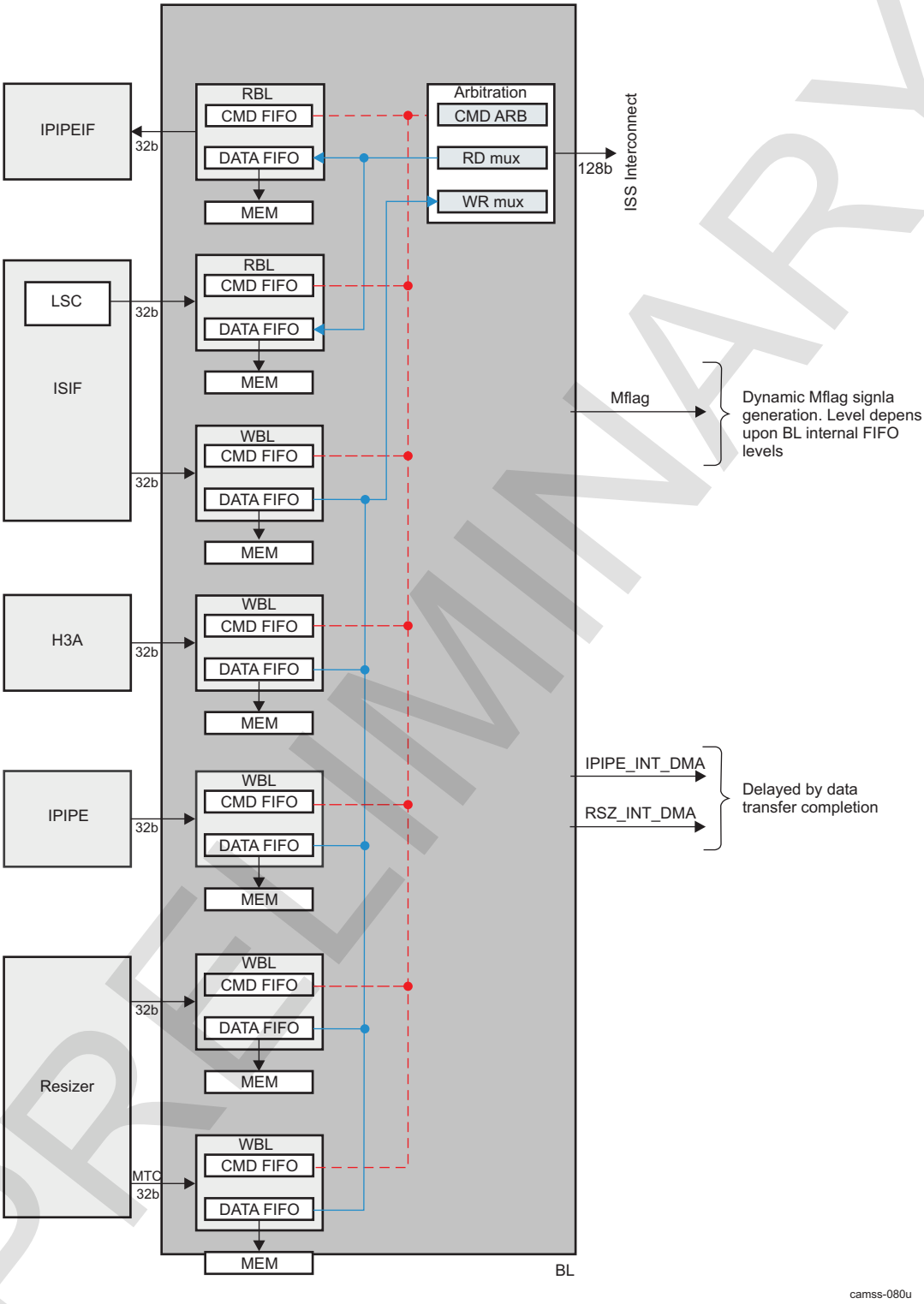
Figure 8-235. ISS ISP BL Block Diagram



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NOTE: The BL module has no registers. The configurations come from the top level of the ISP. See Table 8-393 for register details.

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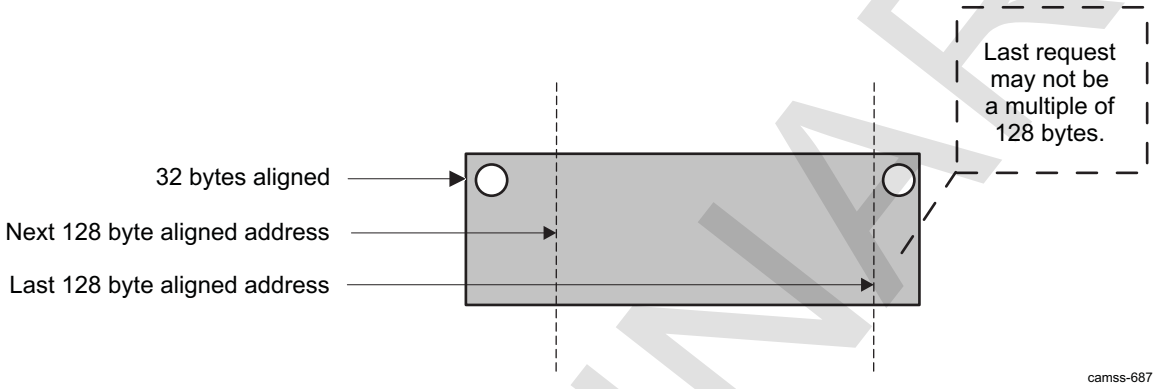
8.3.3.8.3 ISS ISP BL Address Alignment

The BL module ensures maximum memory efficiency by realigning data to a 128-byte address boundary. In all cases, the BL accesses are 32-byte-aligned: address [4:0] is always 0.

This is required when the input address is a multiple of 32 bytes, not 128 bytes. The BL issues a non-aligned burst until it reaches a 128-byte boundary, and then keeps making a 128-byte request until the end of the line. Eventually, although the last burst in a line may not be a multiple of 128 bytes, it will always be a multiple of 32 bytes, as shown in Figure 8-236.

Figure 8-236. ISS ISP BL Address Alignment



8.3.3.8.4 ISS ISP BL Out-of-Order Responses

BL supports out-of-order responses. The out-of-order response is handled by having up to 16 outstanding CIDs (reads + writes). The maximum number of outstanding CIDs is set up by the ISP5_CTRL[7:4] VBUSM_CIDS bit field. There is one outstanding request per CID.

If any of the CIDs are not outstanding, a command is accepted from the highest prioritized buffer with a request. The CID availability is cleared when status complete is received. The outstanding commands can be all reads or all writes or any combination. The CID that is allocated is the lowest number of the 16 that are available when the command is accepted. As soon as a CID is released it is used if a command is available.

The VBUSM2OCP module transforms the VBUMS CIDs into OCP MFlag signals. Note that there can be only one outstanding per tag. It is not authorized to make a new request on a tag which is already waiting for a response.

8.3.3.8.5 ISS ISP BL Stalling

The BL can stall the requests from the initiator modules for reads and writes

8.3.3.8.5.1 ISS ISP BL Stalling Write Requests

One reason for the BL to stall write requests is that there is usually back pressure on the system memory and requests cannot be issued as fast as required. In that case the BL must stall requests from the initiator modules. The BL module cannot know whether stalling the request will lead to an initiator overflow or not. The RESIZER module can support back pressure from the BL module when it is configured in bypass mode. The input buffer memory can be used to store data from the IPIPE and IPIPEIF modules. If the RESIZER input buffer overflows, an interrupt is issued.

8.3.3.8.5.2 ISS ISP BL Stalling Read Requests

The BL may also stall read requests from the ISIF-LSC and IPIPEIF modules. When data comes from an image sensor there is no way to stop the sensor. If the read request is stalled too long, the LSC module may eventually underflow. When the IPIPEIF module reads all its data from memory, the IPIPEIF stalls transfers to successive modules by masking the clock.

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8.3.3.8.6 ISS ISP BL Dynamic and Static MFlag Generation

NOTE: The following applies when ISP5_CTRL[21] MFLAG = 1. The MFlag value is static.

The BL outputs cpriority[2:0] and cepriority[2:0] signals on its VBUS master port interface. On the VBUSM side, these signals are aligned with the request (creq). Both values are actually repeating register input signals. The lower value (0) corresponds to the higher priority.

The MFlag signal does not need to be aligned with the request. The signal can change value anytime.

In the ISP VBUSM2 interface bridge, the cepriority signal is ignored and only the cpriority signal is used. Because the priority value is set up by a register setting, the value is not going to be dynamically modified obviously. Table 8-352 shows how the cpriority values are mapped to the interface MFlag signal, which is present on the ISP master interface and set in the ISP5_CTRL[3:1] VBUSM_CPRIORITY bit field.

Table 8-352. ISS ISP BL cpriority to MFlag With ISP5_CTRL[21] MFLAG = 1

MFlag[1:0]	Description
00	Normal priority cpriority[2:0] = 4, 5, 6, 7
01	Medium priority cpriority[2:0] = 2, 3
10	Reserved
11	High priority cpriority[2:0] = 0, 1

NOTE: The following applies when the ISP5_CTRL[21] MFLAG = 0. The MFlag value is dynamic.

This feature is enabled at reset. The general idea for dynamic MFlag generation is to monitor the FIFO levels. Thresholds are used to increase or decrease the MFlag values. There are different implementations for read and write requestors.

An individual MFlag value is generated for each FIFO and then ORed altogether and exported at the BL boundary. The MFlag signal generation does not affect the BL arbitration scheme.

- Writes: To prevent overflows in the BL, dynamic MFlag signal generation gives higher priority to FIFOs that are almost full:
  - Low FIFO level = 50 percent
  - High FIFO level = 75 percent
  - FIFOs with more than 75 percent fill level have high priority: MFlag = 11
  - FIFOs between 50 and 75 percent fill level have medium priority: MFlag = 01
  - FIFOs below 50 percent fill level have normal priority: MFlag = 00

Table 8-353 gives the low- and high-level priority thresholds for write initiators.

Table 8-353. ISS ISP BL MFlag Write Low- and High-Level Priority Thresholds

	ISIF	H3A	IPIPE	RSZ
Access type	Write	Write	Write	Write
Buffer size	64 × 128	64 × 128	48 × 128	64 × 136
50% low level	32 × 128	32 × 128	24 × 128	32 × 136
75% high level	48 × 128	48 × 128	36 × 128	48 × 128

- Reads: The dynamic MFlag signal generation depends on the reserved data units in the initiator data FIFO. The reserved data units correspond to read commands waiting to be sent on the interface bus, plus the read commands that have been sent on the interface bus and for which data responses have not yet arrived.
- The total FIFO size in bytes can be expressed as reserved data units (bytes) + data bytes stored (bytes) + empty space (bytes). By definition, empty space is lower than a burst size (128 bytes).
  - Low FIFO level = 25 percent

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– High FIFO level = 50 percent
– Data bytes stored + empty space (bytes) = 50 percent of FIFO size: MFlag = 00
– Data bytes stored + empty space (bytes) 50 percent of FIFO size: MFlag = 01
– Data bytes stored + empty space (bytes) 25 percent of FIFO size: MFlag = 11

Table 8-354 gives the low- and high-level priority thresholds for read initiators

Table 8-354. ISS ISP BL MFlag Read Low- and High-Level Priority Thresholds

	IPIPEIF	ISIF-LSC
Access type	Read	Read
Buffer size	64 × 128	32 × 128
25% buffer size	16 × 128	8 × 128
50% buffer size	32 × 128	16 × 128

8.3.3.8.7 ISS ISP BL VBUSM2OCP Last Beat Command Delay

The VBUSM2OCP module bridge implements the following function to work around a limitation of the BL module, which does not send back-to-back requests to the ISS, thereby leading to possible situations where the ISP loses arbitration at the ISS level.

To fully benefit from dynamic MFlag generation (see Section 8.3.3.8.6), the following function is present in the VBUSM2OCP module bridge:

- The delay occurs only if BL MFflag = ISP5_BL_VBUSM[5] MFLAG_THRES.
- The MFlag value used is whatever is available when the last beat comes on the interface bus.
- The last beat of the interface request (read or write) is held until one cycle before a new command (read or write). This is achieved by masking the last beat of the interface command at the ISP interface.

  The last beat is unmasked on the first event of one cycle before a new interface command, or the delay counter that uses the ISP5_BL_VBUSM[4:0] LASTCMD_DLY value counter expires (has decremented to zero). The ISP5_BL_VBUSM[4:0] LASTCMD_DLY bit field must be set before the request on the BL starts. If the value of the ISP5_BL_VBUSM[4:0] LASTCMD_DLY bit field is changed during the pending requests, the delay counter is not updated.

8.3.3.8.8 ISS ISP BL Peak Memory Bandwidth Reduction

To limit the peak memory bandwidth generated by the IPIPEIF (read port), ISIF (read port), and H3A (write port) modules, a bandwidth limiter is placed between the modules and the BL. The resizer module has this function built in and therefore does not need a bandwidth limiter.

The bandwidth limiter enables control of the minimum interval between two consecutive memory requests.

This function is controlled by the ISP5_BL_MTC_1 and ISP5_BL_MTC_2 registers. When the registers are set to 0, the function is not modified (that is, the bandwidth limiter is disabled). For the resizer module, it is controlled by the following registers: RSZ_DMA_RZA and RSZ_DMA_RZB.

8.3.3.9 ISS ISP Memory Mapping

A total of 64KB is reserved for the ISP registers and memories. Table 8-355 describes the memory map.

Table 8-355. ISS ISP Memory Mapping

Memory Mapping	Start	End	Size	Comments
ISS ISP5 SYS1	0x5201 0000	0x5201 009F	160	ISP5 configuration registers (set 1)
ISS ISP5 SYS2	0x5201 00A0	0x5201 03FF	864	ISP5 configuration registers (set 2)
ISS RESIZER registers	0x5201 0400	0x5201 07FF	1024	RESIZER configuration registers

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Table 8-355. ISS ISP Memory Mapping (continued)

Memory Mapping	Start	End	Size	Comments
ISS IPIPE registers	0x5201 0800	0x5201 0FFF	2048	IPIPE configuration registers
ISS ISIF registers	0x52011000	0x5201 11FF	512	ISIF configuration registers
ISS IPIPEIF registers	0x5201 1200	0x5201 13FF	512	IPIPEIF configuration registers
ISS H3A registers	0x5201 1400	0x5201 15FF	512	H3A configuration registers
Reserved	0x5201 1600	0x5201 17FF	512	Reserved
Reserved	0x5201 1800	0x5201 1BFF	1024	Reserved
Reserved	0x5201 1C00	0x5201 1DFF	512	Reserved
Reserved	0x5201 1E00	0x5201 1FFF	512	Reserved
HST memory 0	0x5201 2000	0x5201 27FF	2048	IPIPE histogram
HST memory 1	0x5201 2800	0x5201 2FFF	2048	IPIPE histogram
HST memory 2	0x5201 3000	0x5201 37FF	2048	IPIPE histogram
HST memory 3	0x5201 3800	0x5201 3FFF	2048	IPIPE histogram
Reserved	0x5201 4000	0x5201 6EFF	16384	Reserved
DPC table 0	0x5201 8000	0x5201 81FF	1024	IPIPE Defect(Fault) Pixel Correction address table
DPC table 1	0x5201 8400	0x5201 85FF	1024	IPIPE Defect(Fault) Pixel Correction address table
YEE table	0x5201 8800	0x5201 8FFF	2048	IPIPE Y-data Edge Enhance table
Reserved	0x5201 9000	0x5201 A6FF	6144	Reserved
GAMR table	0x5201 A800	0x5201 AFFF	2048	IPIPE Gamma correction table (R)
GAMG table	0x5201 B000	0x5201 B7FF	2048	IPIPE Gamma correction table (G)
GAMB table	0x5201 B800	0x5201 BFFF	2048	IPIPE Gamma correction table (B)
LIN table0	0x5201 C000	0x5201 C17F	1024	ISIF Linearization table
LIN table1	0x5201 C400	0x5201 C57F	1024	ISIF Linearization table
DCCLAMP	0x5201 C800	0x5201 C9FF	2048	ISIF Digital Clamp
LSC table0	0x5201 D000	0x5201 E7FF	6144	ISIF Lens Shading gain table
LSC table1	0x5201 E800	0x5201 FFFF	6144	ISIF Lens Shading gain table

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8.3.4 ISS ISP Programming Model

NOTE: The preferred way to perform memory-to-memory processing with ISP is to use the CCP2 receiver module at the ISS level (see Section 8.2, *ISS Interfaces*.). It is possible to use the IPIPEIF read port for memory-to-memory processing, but it is not the preferred way because it does not provide enough granularity on the fractional clock divider for up to 20x digital zoom.

8.3.4.1 ISS ISP PG Programming Model

The procedure in Table 8-356 initializes the pattern generator.

Table 8-356. ISS ISP PG Settings

Step	Register/Bit Field/Programming Model	Value
Select the PG as the ISP source.	ISP5_PG[5:4] SRC_SEL	0x3
Select the mode for write-enable signal generation.	ISP5_PG[2] WEN	
Select the polarity of the horizontal sync signal.	ISP5_PG[1] HDPOL	
Select the polarity of the vertical sync signal.	ISP5_PG[0] VDPOL	
Sets the duration of the HD signal	ISP5_PG_PULSE_CTRL[12:0] HDW	
Sets the duration of the VD signal	ISP5_PG_PULSE_CTRL[27:16] VDW	
Sets the number of pixels per line	ISP5_PG_FRAME_SIZE[31:16] PPLN	
Sets the number of lines per frame	ISP5_PG_FRAME_SIZE[15:0] HLPFR	
Enables the pattern generator	ISP5_PG[3] EN	0x1

8.3.4.2 ISS ISP ISIF Programming Model

This section discusses issues related to the software control of the ISIF. It lists the registers that are required to be programmed in different modes, describes how to enable and disable the ISIF and how to check the status of the ISIF, discusses the different register access types, and enumerates several programming constraints.

8.3.4.2.1 ISS ISP ISIF Hardware Setup/Initialization

This section discusses the configuration of the ISIF required before image processing can begin.

8.3.4.2.1.1 ISS ISP ISIF Reset Behavior

Upon hardware reset of the ISP, all of the registers in the ISIF, except the defect table registers, are reset to their reset values. Because the defect table registers are stored in internal RAM, they do not have reset values. If the reset is a chip-level POR (reset after power is applied), the values of the defect table register are unknown. If the reset is an ISP module reset (when power remains active), the contents of this memory remain the same as before the reset.

8.3.4.2.1.2 ISS ISP ISIF Register Setup

Before enabling the ISIF, the hardware must be properly configured through register writes. Figure 8-237 and Figure 8-238 show the sequence to be used for RAW and YUV data before enabling the ISIF. The register settings for each process in the following sequence are described in Table 8-357.

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Figure 8-237. ISS ISP ISIF Initialization Flow Chart – Part One

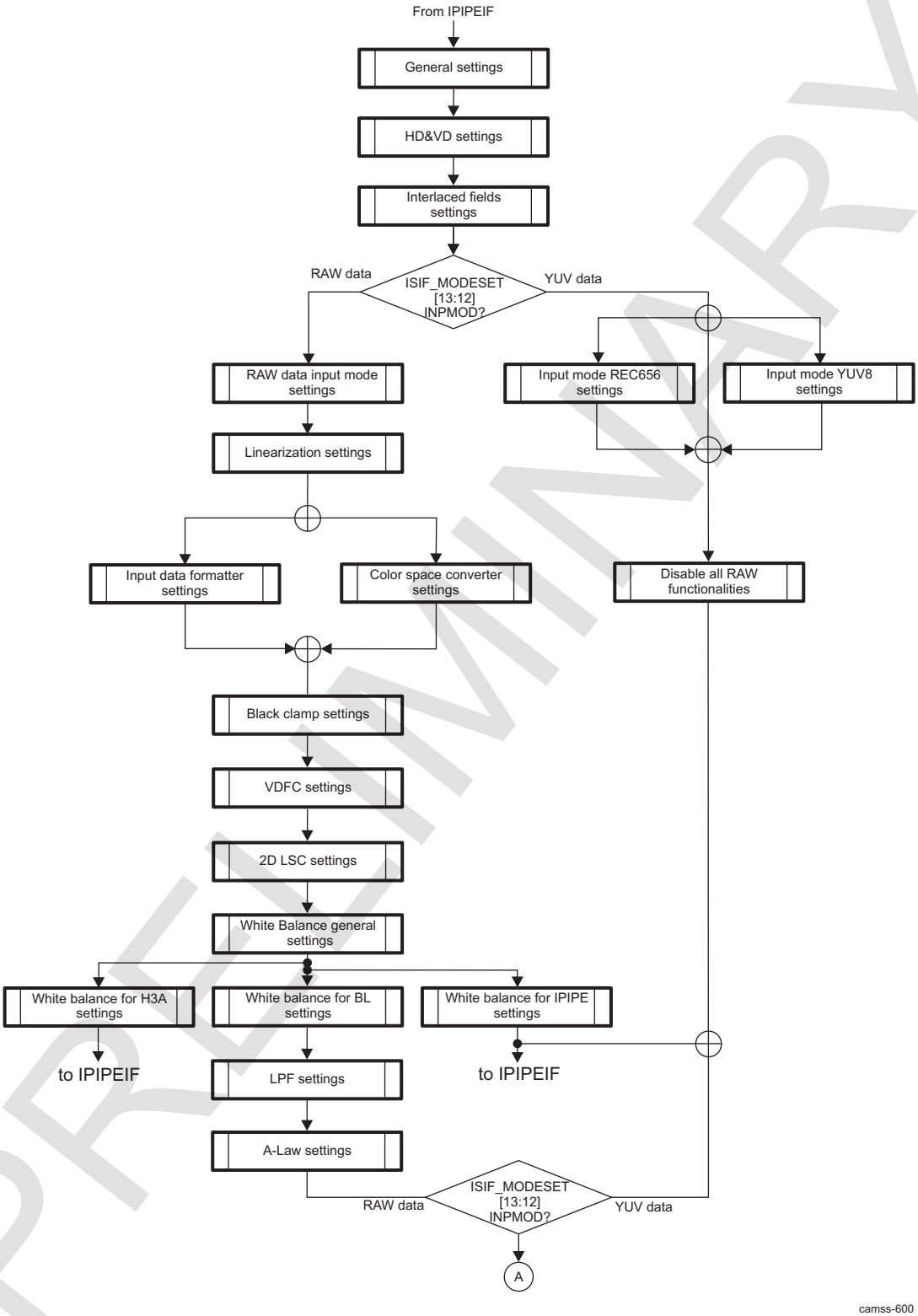

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Figure 8-238. ISS ISP ISIF Initialization Flow Chart – Part Two

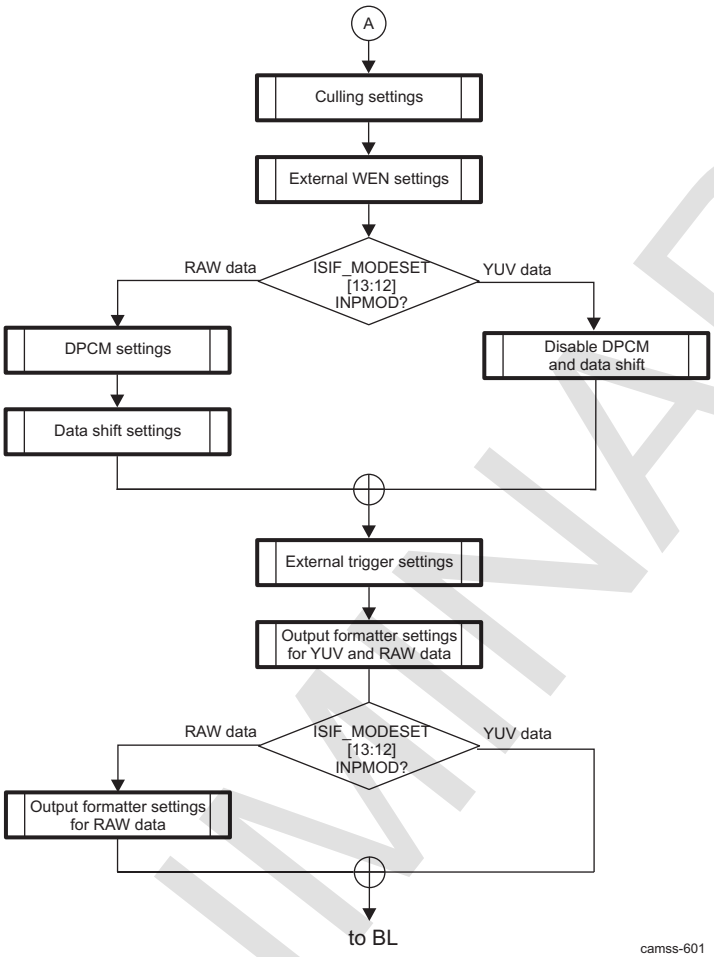

Table 8-357. ISS ISP ISIF Required Configuration Parameters

Step	Configuration Required	Value
General settings		
Set the Field Indicator signal direction.	ISIF_MODESET[1] FIDD	
Set the VD signal polarity.	ISIF_MODESET[2] VDPOL	
Set the HD signal polarity.	ISIF_MODESET[3] HDPOL	
Set the Field Indicator signal polarity.	ISIF_MODESET[4] FIPOL	
HD and VD settings		
Set the HD and VD signal directions.	ISIF_MODESET[0] HDVDD	
If: HD and VD are set as output (HDVDD = 0x1):		
Set the HD width.	ISIF_HDW[11:0] HDW	
Set the VD width.	ISIF_VDW[11:0] VDW	
Set the HD period.	ISIF_PPLN[15:0] PPLN	
Set the VD period.	ISIF_LPFR[15:0] LPFR	
End		
Interlaced fields settings		
Select the type of image sensor (progressive or interlaced)	ISIF_MODESET[7] CCDMD	
Input mode settings		
Set the data input mode.	ISIF_MODESET[13:12] INPMOD	

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Table 8-357. ISS ISP ISIF Required Configuration Parameters (continued)

Step	Configuration Required	Value
Input mode settings for REC656 data		
Select CCIR Rec.656 interface or not.	ISIF_REC656IF[1] R656ON	
If: input is REC656 (R656ON = 0x1)		
Set error correction of FVH code.	ISIF_REC656IF[0] ECCFVH	
Selects bit width of CCIR656.	ISIF_CCDCFG[5] BT656	
e End		
Input mode settings for YCC 8 bit data (if INPMOD = 0x2)		
Selects Y position signal	ISIF_CCDCFG[11] Y8POS	
RAW data processing: input settings		
Enable or disable MSB inverse of CIN port (YUV format).	ISIF_CCDCFG[13] MSBINVI	
Select Y and C swapping.	ISIF_CCDCFG[4] YCINSWP	
Selects MSB position of input data (16 bits-to-16 bits)	ISIF_CGAMMAWD[4:1] GWDI	
Set the image sensor data polarity.	ISIF_MODESET[6] DPOL	
Select the CFA pattern mode.	ISIF_CGAMMAWD[5] CFAP	
Specifies the color pattern	ISIF_CCOLP[7:6] CP0_F0	
	ISIF_CCOLP[5:4] CP1_F0	
	ISIF_CCOLP[3:2] CP2_F0	
	ISIF_CCOLP[1:0] CP3_F0	
Linearization settings		
Enable linearization or not.	ISIF_LINCFG0[0] LINEN	
If: Linearization enabled (LINEN = 0x1)		
Select linearization mode.	ISIF_LINCFG0[1] LINMD	
Select the shift value.	ISIF_LINCFG0[6:4] CORRSFT	
Set the scale factor for LUT.	ISIF_LINCFG1[10:0] LUTSCL	
Set up linearization LUT.		
End		
Input data formatter settings		
Enable data formatter or not.	ISIF_FMTCFG[0] FMTEN	
If: Data formatter is enabled (FMTEN = 0x1)		
Select the combine input lines.	ISIF_FMTCFG[1] FMTCBL	
Select the mode normal or alternative.	ISIF_FMTCFG[2] LNALT	
Select the split/combine number of lines.	ISIF_FMTCFG[5:4] LNUM	
Set the address increment.	ISIF_FMTCFG[11:8] FMTAINC	
Set the number of program entries per SET.	ISIF_FMTPLEN[3:0] FMTPLEN0	
	ISIF_FMTPLEN[7:4] FMTPLEN1	
	ISIF_FMTPLEN[10:8] FMTPLEN2	
	ISIF_FMTPLEN[14:12] FMTPLEN3	
Set the first pixel in a line.	ISIF_FMTSPH[12:0] FMTSPH	
Set the number of pixels in a line.	ISIF_FMTLNH[12:0] FMTLNH	
Set the start line vertical.	ISIF_FMTLSV[12:0] FMTSLV	
Set the number of lines in a vertical.	ISIF_FMTLNV[14:0] FMTLNV	
Set the number of pixels in an output line.	ISIF_FMTRLEN[12:0] FMTRLEN	
Set the HD interval for output lines.	ISIF_FMTHCNT[12:0] FMTHCNT	
Set up to 16 address pointers.	ISIF_FMTAPTRx[14:13] LINE (x = 0 to 15)	
	ISIF_FMTAPTRx[12:0] INIT (x = 0 to 15)	

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Table 8-357. ISS ISP ISIF Required Configuration Parameters (continued)

Step	Configuration Required	Value
Set the 32 possible program entry valid flag.	ISIF_FMTPGMVF0	
	ISIF_FMTPGMVF1	
Set the 32 possible address pointers.	ISIF_FMTPGMAPS0	
	ISIF_FMTPGMAPS1	
	ISIF_FMTPGMAPS2	
	ISIF_FMTPGMAPS3	
	ISIF_FMTPGMAPS4	
	ISIF_FMTPGMAPS5	
	ISIF_FMTPGMAPS6	
	ISIF_FMTPGMAPS7	
Set the 32 possible address update (increment or decrement).	ISIF_FMTPGMAPU0	
	ISIF_FMTPGMAPU1	E
End		
Color space converter settings		
Enable or disable color space converter.	ISIF_CSCCTL[0] CSCEN	
If: Color space converter is enabled (CSCEN = 0x1)		
Set the color space converter coefficients.	ISIF_CSCM0	
	ISIF_CSCM1	
	ISIF_CSCM2	
	ISIF_CSCM3	
	ISIF_CSCM4	
	ISIF_CSCM5	
	ISIF_CSCM6	
	ISIF_CSCM7	
End		
Black Clamp settings		
Enable or disable black clamp.	ISIF_CLAMPCFG[0] CLEN	
If: Black clamp is enabled (CLEN = 0x1)		
Set the DC offset for black clamp.	ISIF_CLDCOFST[12:0] CLDC	
[Horizontal Black Clamp]		
Set the horizontal clamp mode.	ISIF_CLAMPCFG[2:1] CLHMD	
Set the vertical dimension of a window.	ISIF_CLHWIN0[13:12] CLHWN	
Set the horizontal dimension of a window.	ISIF_CLHWIN0[9:8] CLHWM	
Enable or disable limitation for horizontal.	ISIF_CLHWIN0[6] CLHLMT	
Select base window.	ISIF_CLHWIN0[5] CLHWBS	
Set the window count per color.	ISIF_CLHWIN0[4:0] CLHWC	
Set window start position (H).	ISIF_CLHWIN1[12:0] CLHSH	
Set the window start position (V).	ISIF_CLHWIN2[12:0] CLHSV	
[Vertical Black Clamp]		
Set the black clamp start position.	ISIF_CLSV[12:0] CLSV	
Set the vertical black clamp reset value.	ISIF_CLVRV[11:0] CLVRV	
Set the line average coefficient.	ISIF_CLVWIN0[15:8] CLVCOEF	
Select the reset value for the clamp value of the previous line.	ISIF_CLVWIN0[5:4] CLVRVSL	
Select the optical black H valid.	ISIF_CLVWIN0[2:0] CLVOBH	
Set the window start position (H).	ISIF_CLVWIN1[12:0] CLVSH	
Set the window start position (V).	ISIF_CLVWIN2[12:0] CLVSV	
Select the optical black V valid.	ISIF_CLVWIN3[12:0] CLVOBV	

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Table 8-357. ISS ISP ISIF Required Configuration Parameters (continued)

Step	Configuration Required	Value
End		
Set the DC offset for black clamp (RAW data only).	ISIF_CLDCOFST[12:0] CLDC	DC offset available for YUV
Vertical line defect correction (VDFC) settings		
Disable vertical line defect correction.	ISIF_DFCCTL[4] VDFCEN	0x0
If: Vertical line defect correction will be enabled (VDFCEN = 0x1)		
Select the mode.	ISIF_DFCCTL[6:5] VDFCSL	
Select upper pixels correction enable or disable.	ISIF_DFCCTL[7] VDFCUDA	
Set the shift value.	ISIF_DFCCTL[10:8] VDFLSFT	
Set the saturation level.	ISIF_VDFSATLV[11:0] VDFSLV	
Clear memories.	ISIF_DFCMEMCTL[4] DFCMCLR	0x1
Vertical line defect table update procedure.	See Section 8.3.3.7.9.1 for details.	
	Use the following registers:	
	ISIF_DFCMEMCTL[2] DFCMARST	
	ISIF_DFCMEMCTL[0] DFCMWR	
	ISIF_DFCMEM0	
	ISIF_DFCMEM1	
	ISIF_DFCMEM2	
	ISIF_DFCMEM3	
	ISIF_DFCMEM4	
Rnd		
Enable vertical line defect correction.	ISIF_DFCCTL[4] VDFCEN	0x1
2D Lens Shading Compensation (LSC) settings		
Disable lens shading compensation.	ISIF_2DLSCCFG[0] ENABLE	0x0
If: 2D-LSC will be enabled (ENABLE = 0x1)		
Set the H direction data offset.	ISIF_LSCHOFST[13:0] HOFST	
Set the V direction data offset.	ISIF_LSCVOFST[13:0] VOFST	
Set the number of valid pixels in H direction.	ISIF_LSCHVAL[13:0] HVAL	
Set the number of valid lines in V direction.	ISIF_LSCVVAL[13:0] VVAL	
Define the horizontal dimension of a paxel.	ISIF_2DLSCCFG[14:12] GAIN_MODE_M	
Define the vertical dimension of a paxel.	ISIF_2DLSCCFG[10:8] GAIN_MODE_N	
Set gain format table.	ISIF_2DLSCCFG[3:1] GAIN_FORMAT	
Enable or disable offset control.	ISIF_2DLSCOFST[0] OFSTEN	
Select shift up value for offsets.	ISIF_2DLSCOFST[6:4] OFSTSFT	
Set scaling factor for offset.	ISIF_2DLSCOFST[15:8] OFSTSF	
Set the initial Y position.	ISIF_2DLSCINI[14:8] Y	
Set the initial X position.	ISIF_2DLSCINI[6:0] X	
Set the gain table base address.	ISIF_2DLSCGRBU[15:0] BASE31_16	
	ISIF_2DLSCGRBL[15:0] BASE15_0	
Set the gain table offset (length of one row).	ISIF_2DLSCGROF[15:0] OFFSET	
Set the offset table base address.	ISIF_2DLSCORBU[15:0] BASE	
	ISIF_2DLSCORBL[15:0] BASE	
Set the offset table offset (length of one row).	ISIF_2DLSCOROF	

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Table 8-357. ISS ISP ISIF Required Configuration Parameters (continued)

Step	Configuration Required	Value
Enable useful interrupts	ISIF_2DLSCIRQEN[3] SOF	
	ISIF_2DLSCIRQEN[2] PREFETCH_COMPLETED	
	ISIF_2DLSCIRQEN[1] PREFETCH_ERROR	
	ISIF_2DLSCIRQEN[0] DONE	
Set up LSC gain table and offset table in SDRAM. See Figure 8-224 for details.		
Wait seven clock periods before enabling LSC.		
Enable lens shading compensation.	ISIF_2DLSCCFG[0] ENABLE	0x1
End		
White balance color settings		
Set R/Ye gain.	ISIF_CRGAIN[11:0] CGR	
Set Gr/Cy gain.	ISIF_CGRGAIN[11:0] CGGR	
Set Gr/Cy gain.	ISIF_CGBGAIN[11:0] CGGB	
Set B/Mg gain.	ISIF_CBGAIN[11:0] CGB	
Set offset.	ISIF_COFSTA[11:0] COFT	
[For BL output]		
Enable or disable white balance for BL path.	ISIF_CGAMMAWD[12] WBNEN0	
Enable or disable offset control for BL path.	ISIF_CGAMMAWD[8] OFSTEN0	
[For IPIPE (through IPIPEIF) output]		
Enable or disable white balance for IPIPE path.	ISIF_CGAMMAWD[13] WBEN1	
Enable or disable offset control for IPIPE path.	ISIF_CGAMMAWD[9] OFSTEN1	
[For H3A (through IPIPEIF) output]		
Enable or disable white balance for H3A path.	ISIF_CGAMMAWD[14] WBEN2	
Enable or disable offset control for H3A path.	ISIF_CGAMMAWD[10] OFSTEN2	
LPF settings (for BL output only) (RAW data only)		
Enable or disable low pass filter.	ISIF_MODESET[14] HLPF	
A-Law compression settings (for BL output only) (RAW data only)		
Enable or disable A-Law compression.	ISIF_CGAMMAWD[0] CCDTBL	
Culling settings (for BL output only) (RAW or YUV data)		
Set the culling pattern in odd lines.	ISIF_CULH[15:8] CLHO	
Set the culling pattern in even lines.	ISIF_CULH[7:0] CLHE	
Set the culling pattern in vertical lines.	ISIF_CULV[7:0] CULV	
External WEN settings (for BL output only)		
Select external WEN use or not.	ISIF_MODESET[5] SWEN	
If: External WEN is used (SWEN = 0x1):		
Specifies the CCD valid area	ISIF_CCDCFG[8] WENLOG	
End		
DPCM settings (for BL output only) RAW data only		
Select the predictor for DPCM encoder.	ISIF_MISC[13] DPCMPRE	
Enable or disable DPCM encoding.	ISIF_MISC[12] DPCMEN	
Data shift settings (for BL output only) (RAW data only)		
Select the data shift value when image is written to memory	ISIF_MODESET[10:8] CCDW	

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Table 8-357. ISS ISP ISIF Required Configuration Parameters (continued)

Step	Configuration Required	Value
External trigger settings (for BL output only)		
If: External trigger is selected (EXTRG = 0x1):		
Select the trigger source signal.	ISIF_CCDCFG[9] TRGSEL	
End		
Output formatter (for BL output only) RAW and YUV		
Set the memory address decrement.	ISIF_HSIZE[12] ADCR	
Set the memory address offset between lines.	ISIF_HSIZE[11:0] HSIZE	
Set the first pixel in a line to be stored in memory.	ISIF_SPH[14:0] SPH	
Set the number of pixels in a line to be stored in memory.	ISIF_LNH[14:0] LNH	
Set the start line vertical for field 0.	ISIF_SLV0[14:0] SLV0	
Set the start line vertical for field 1.	ISIF_SLV1[14:0] SLV1	
Set the number of lines to be stored in memory.	ISIF_LNV[14:0] LNV	
Enable or disable the storage of image in memory.	ISIF_SYNCEN[1] DWEN	
Set the memory destination address.	ISIF_CADU[10:0] CADU	
	ISIF_CADL[10:0] CADL	
Enable or disable MSB inverse of COUT port.	ISIF_CCDCFG[14] MSBINVO	
Enable or disable byte swap when SDRAM capturing.	ISIF_CCDCFG[12] BSWD	
Select Y and C swapping.	ISIF_CCDCFG[2] YCOUNTSWP	
Select SDRAM pack mode.	ISIF_CCDCFG[1:0] SDRPACK	
Enable or disable VD/HD output.	ISIF_SYNCEN[0] SYEN	

8.3.4.2.2 ISS ISP ISIF Enable/Disable Hardware

The ISIF is enabled by setting the ISIF_SYNCEN[0] SYEN bit. This is done after all the required registers discussed in the previous section are programmed.

With respect to the write enable bit and output address, the following procedure must be followed:

1. Set the data output address (ISIF_CADU and ISIF_CADL).
2. Enable HD/VD and WEN at the same time (ISIF_MODESET[1] DWEN and ISIF_SYNCEN[0] SYEN).

If the ISIF_SYNCEN[0] SYEN bit is written before the output address and the SDRAM write enable bit (not recommended but may be required for a particular mode), data begins to be written to the old address value and not the one recently programmed. The desired response can be achieved if the following procedure is followed:

1. Enable HD/VD (ISIF_SYNCEN[0] SYEN).
2. Set the output address (ISIF_CADU and ISIF_CADL).
3. Wait for the next VD.
4. Enable WEN (ISIF_MODESET[1] DWEN).

The ISIF always operates in continuous mode. In other words, after enabling the ISIF, it continues to process sequential frames until the ISIF_SYNCEN[0] SYEN bit is cleared by software. When this happens, the frame being processed is disabled immediately and does not continue to process the current frame.

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When the HD/VD signals are set to outputs (ISIF_MODESET[0] HDVDD = 0x1), fetching and processing of the frame begin immediately upon setting the ISIF_SYNCEN[0] SYEN bit.

When the HD/VD signals are set to inputs (ISIF_MODESET[0] HDVDD = 0x0), processing of the frame is dependent on the input timing of the external sensor/decoder. To ensure that data from the external device is not missed, the ISIF must be enabled before data transmission from the external device. In this way, the ISIF waits for data from the external device.

8.3.4.2.3 ISS ISP ISIF Register Accessibility During Frame Processing

There are two types of register access in the ISIF:

- Shadowed registers (event latched registers)

  Shadowed registers are those that can be read and written at any time, but the written values take effect (are latched) only at certain times based on some event. Reads still return the most recent write even though the settings are not used until the specific event occurs.
- Busy-writable registers

  These registers/fields can be read or written even if the module is busy. Changes to the underlying settings takes place instantly.

The following registers/fields can be set as shadow registers, or optionally set as busy-writable registers. When the ISIF_CCDCFG[15] VDLC bit is set to 0, these registers are shadowed; when the ISIF_CCDCFG[15] VDLC bit is set to 1, these registers are busy-writable. All other ISIF registers not included in this list are always busy-writable.

ISIF_SYNCEN[1] DWEN	ISIF_SLV1	ISIF_CGRGAIN	ISIF_FMTLSV
ISIF_MODESET[14] HLPF	ISIF_CULH	ISIF_CGBGAIN	ISIF_FMTLNV
ISIF_HDW	ISIF_CULV	ISIF_CBGAIN	ISIF_LSCHOFST
ISIF_VDW	ISIF_HSIZE	ISIF_COFSTA	ISIF_LSCVOFST
ISIF_PPLN	ISIF_SDOFST	ISIF_CLAMPCFG[0] CLEN	ISIF_DFCCTL
ISIF_LPFR	ISIF_CADU	ISIF_MISC	ISIF_VDFSATLV
ISIF_SPH	ISIF_CADL	ISIF_CGAMMAWD	
ISIF_LNH	ISIF_CCOLP	ISIF_FMTSPH	
ISIF_SLV0	ISIF_CRGAIN	ISIF_FMTLNH	

8.3.4.2.4 ISS ISP ISIF Interframe Operations

Between frames, it may be necessary to enable or disable functions or to modify the memory pointers. Because the ISIF_SYNCEN[1] DWEN bit and the memory pointer registers are shadowed, these modifications can occur any time before the end of the frame and the data will be latched in for the next frame. Likewise, the 2D-LSC registers can be changed after receiving the LSC SOF interrupt but before it starts to prefetch the gain values for the next frame (the end of the LSC active region is reached). The host controller can perform these changes upon receiving an interrupt.

8.3.4.2.5 ISS ISP ISIF Summary of Constraints

The following is a list of register configuration constraints to adhere to when programming the ISIF. It can be used as a quick checklist. More detailed register setting constraints can be found in the individual register descriptions.

- PCLK cannot be higher than 200 MHz.
- If SDRAM output port is enabled:
  - The memory output line offset and address must be on 32-byte boundaries.
  - ISIF_LNH[14:0] LNH –1 must be a multiple of 32 bytes.
  - ISIF_SPH, ISIF_LNH, ISIF_SLV0, ISIF_SLV1, and ISIF_LNV must be cleared to 0 within the same VD period that the ISIF_SYNCEN[1] DWEN bit is cleared to 0.

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- ISIF_SPH, ISIF_LNH, ISIF_SLV0, ISIF_SLV1, and ISIF_LNV must be set from 0 to the appropriate values within the same VD period that the ISIF_SYNCEN[1] DWEN bit is set to 1.

- In RAW input mode:
  - ISIF_CCDCFG[4] YCINSWP must be set to 0.
- If DPCM compression is enabled:
  - Horizontal culling must not be used. Use the input formatter instead.
- For 2D-LSC:
  - N=M (where M = horizontal downsampling factor, N = vertical downsampling factor)
  - The ISIF_2DLSCINI register values must be even numbers.
  - Maximum widths with respect to selected M value (see Table 8-358)

Table 8-358. ISS ISP ISIF Maximum Line Width Versus M Value

M	Maximum Line Width
8	2040
16	4080
32	8160
64	16,320
128	16,384

8.3.4.3 ISS ISP IPIPEIF Programming Model

This section discusses issues related to the software control of the IPIPEIF module. It lists the registers that are required to be programmed in different modes, describes how to enable and disable the IPIPEIF module and how to check the status of the IPIPEIF module, discusses the different register access types, and enumerates several programming constraints.

8.3.4.3.1 ISS ISP IPIPEIF Hardware Setup/Initialization

This section discusses the configuration of the IPIPEIF module required before image processing can begin.

8.3.4.3.1.1 ISS ISP IPIPEIF Reset Behavior

Upon hardware reset of the ISP (ISP5_SYSCONFIG[1] SOFTRESET = 0x1), all the registers in the IPIPEIF are reset to their reset values.

8.3.4.3.1.2 ISS ISP IPIPEIF Register Setup

Before enabling the IPIPEIF, the hardware must be properly configured through register writes. Table 8-359 identifies the register parameters that must be programmed before enabling the IPIPEIF module (depending on the functions needed).

Table 8-359. ISS ISP IPIPEIF Required Configuration Parameters

Step	Configuration Required	Value
General settings		
Select the input sources for IPIPEIF.	IPIPEIF_CFG1[15:14] INPSRC1	
	IPIPEIF_CFG1[3:2] INPSRC2	
Select VD sync polarity.	IPIPEIF_CFG2[2] VDPOL	
Select HD sync polarity.	IPIPEIF_CFG2[1] HDPOL	
Select the interrupt source.	IPIPEIF_CFG2[0] INTSW	
Select the input clock source.	IPIPEIF_CFG1[10] CLKSEL	
Set the clock divider value.	IPIPEIF_CLKDIV[15:0] CLKDIV	
Set the data type: YUV or RAW.	IPIPEIF_CFG2[3] YUV16	

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Table 8-359. ISS ISP IPIPEIF Required Configuration Parameters (continued)

Step	Configuration Required	Value
Settings to perform if data is from BL		
Set HD setting.	IPIPEIF_PPLN[12:0] PPLN	
Set VD setting.	IPIPEIF_LPFR[12:0] LPFR	
Set the number of valid pixels in a line.	IPIPEIF_HNUM[12:0] HNUM	
Set the number of valid lines.	IPIPEIF_VNUM[12:0] VNUM	
Set memory address information.	IPIPEIF_ADDRU[10:0] ADDRU	
	IPIPEIF_ADDRL[15:0] ADDRL	
	IPIPEIF_ADOFS[11:0] ADOFS	
Set one-shot mode, if needed.	IPIPEIF_CFG1[0] ONESHOT	
Use SYNCOFF function only for double-buffering. See Section 8.3.3.3.3.2.1 for details.	IPIPEIF_ENABLE[1] SYNCOFF	
Settings to perform for RAW data from ISIF or BL		
Select the unpack function.	IPIPEIF_CFG1[9:8] UNPACK	
Settings to perform for YUV for data from ISIF		
Set the data type to YUV.	IPIPEIF_CFG2[3] YUV16	
If YUV16 = 0x1, enables or not the conversion from 8 bits to 16 bits	IPIPEIF_CFG2[6] YUV8	
If YUV16 = 0x1, set the way the data is unpacked.	IPIPEIF_CFG2[7] YUV8P	
DCPM function	RAW data from Buffer Logic (BL)	
Enable or disable DPCM decompression.	IPIPEIF_DPCM[0] ENA	
Select DPCM prediction mode.	IPIPEIF_DPCM[1] PRED	
Select DPCM bit mode.	IPIPEIF_DPCM[2] BITS	
Select inverse A-Law function.	IPIPEIF_CFG1[9:8] UNPACK	
Select SDRAM read data shift. - For RAW data - DPCM enabled and A- Law disabled - or DPCM disabled	IPIPEIF_CFG1[13:11] DATASFT	
Dark frame subtraction (DFS) function	RAW data from VP (video port), BL(buffer logic, SDRAM) or ISIF	
Set defect pixel correction (DPC1) for VP or ISIF inputs.	IPIPEIF_DPC1[12] ENA	
Set the associated threshold for DPC1.	IPIPEIF_DPC1[11:0] TH	
Set defect pixel correction (DPC2) for BL inputs.	IPIPEIF_DPC2[12] ENA	
Set the associated threshold for DPC1.	IPIPEIF_DPC2[11:0] TH	
Set the direction of subtraction.	IPIPEIF_CFG2[5] DFSDIR	
Set the averaging filter, horizontal pixel decimator, and gain function for IPIPE data path.		
Enable averaging filter function.	IPIPEIF_CFG1[7] AVGFILT	
Enable horizontal pixel decimation function.	IPIPEIF_CFG1[1] DECIM	
Set horizontal resizing value.	IPIPEIF_RSZ[6:0] RSZ	
Set the resizer initial position.	IPIPEIF_INIRSZ[13] ALNSYNC	
	IPIPEIF_INIRSZ[12:0] INIRSZ	
Set the data gain (only for RAW data).	IPIPEIF_GAIN[9:0] GAIN	
Set the output clipping value.	IPIPEIF_OCLIP[11:0] OCLIP	

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Table 8-359. ISS ISP IPIPEIF Required Configuration Parameters (continued)

Step	Configuration Required	Value
Set the averaging filter and horizontal pixel decimator function for H3A data path.		
Enable averaging filter function.	IPIPEIF_RSZ3A[8] AVGFILT	
Enable horizontal pixel decimation function.	IPIPEIF_RSZ3A[9] DECIM	
Set horizontal resizing value.	IPIPEIF_RSZ3A[6:0] RSZ	
Set the resizer initial position.	IPIPEIF_RSZ3A[13] ALNSYNC	
	IPIPEIF_RSZ3A[12:0] INIRSZ	

For information about YUV data coming and unpacking from the ISIF module, see Section 8.3.3.3.13.

8.3.4.3.2 ISS ISP IPIPEIF Enable/Disable Hardware

When IPIPEIF_CFG1[15:14] INPSRC1 or IPIPEIF_CFG1[3:2] INPSRC2 = 0, the IPIPEIF does not need to be enabled: it receives data from the VP and pushes it to the ISIF, H3A, IPIPE, and RESIZER modules.

If IPIPEIF_CFG1[15:14] INPSRC1 or IPIPEIF_CFG1[3:2] INPSRC2 ≠ 0, the IPIPEIF module begins to fetch data from the BL by setting the IPIPEIF_ENABLE[0] ENABLE bit. Writing the enable bit must be the last step of the configuration.

When the input source is the BL, the IPIPEIF can optionally operate in one-shot mode or continuous mode by setting the IPIPEIF_CFG1[0] ONESHOT parameter. If one-shot mode is enabled, then after enabling the IPIPEIF, the IPIPEIF_ENABLE[0] ENABLE bit is automatically turned off (set to 0) and only a single frame is processed from memory. In this mode, fetching and processing of the frame begins immediately upon setting the IPIPEIF_ENABLE[0] ENABLE bit.

When the input source is the ISIF, processing of the frame is dependent on the timing of the ISIF. To ensure that data from the ISIF is not missed, the IPIPEIF must be enabled before the ISIF. In this way, the IPIPEIF waits for data from the ISIF.

When the IPIPEIF is in continuous mode, it can be disabled by clearing the IPIPEIF_ENABLE[0] ENABLE bit after processing of the last frame. The disable takes place immediately because it is a busy-writable register.

An EOF interrupt can indicate to other modules that the frame treatment is finished. See Section 8.3.3.3.15 for more information.

8.3.4.3.3 ISS ISP IPIPEIF Register Accessibility During Frame Processing

There are two types of register access in the IPIPEIF:

- Shadow registers

  These registers/fields can be read and written (if the field is writable) at any time. However, the written values take effect only at the start of a frame (VD rising edge). Reads still return the most recent write even though the settings are not used until the next start of frame. The following are the shadowed registers in the IPIPEIF:

IPIPEIF_PPLN
IPIPEIF_HNUM
IPIPEIF_VNUM
IPIPEIF_GAIN
IPIPEIF_RSZ3A[6:0] RSZ
IPIPEIF_ADDRU
IPIPEIF_ADOFS
IPIPEIF_ENABLE[1] SYNCOFF
IPIPEIF_RSZ3A[9] DECIM
IPIPEIF_CFG1[1] DECIM
IPIPEIF_CFG1[7] AVGFILT
IPIPEIF_RSZ
IPIPEIF_RSZ3A[8] AVGFILT

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- Busy-writable registers

  These registers/fields can be read or written even if the module is busy. Changes to the underlying settings takes place instantaneously. Registers that are not shadowed are busy-writable.

Only for busy-writable registers, the ideal procedure for changing the IPIPEIF registers is IF (PCR.BUSY == 0) OR IF (EOF interrupt occurs):

- Disable IPIPEIF (IPIPEIF_ENABLE[0] ENABLE = 0x0).
- Change registers.
- Enable IPIPEIF (IPIPEIF_ENABLE[0] ENABLE = 0x1).

8.3.4.3.4 ISS ISP IPIPEIF Interframe Operations

Between frames, it may be necessary to enable or disable functions or to modify the memory pointers. Because several of the registers are shadowed, these modifications can take place any time before the end of the frame, and the data is latched in for the next frame. The host controller can perform these changes upon receiving an interrupt.

When reading input data from the BL, the host must check IPIPEIF_DTUF or the ISP5_IRQSTATUS_RAW2_i[1] IPIPEIF_UDF register (if this event is enabled and mapped to the ISP IRQ lines) during vertical blanking to see if an underflow occurred.

If an underflow occurs it means the system is congested because too much bandwidth is being generated. It is most likely that the scenario being passed is too memory bandwidth-intensive. If the bit is set, software must clear the bit. If the process is taking place from memory-to-memory, the software may try to re-initiate the data flow. Software must decide the sequence to execute after an underflow.

8.3.4.3.5 ISS ISP IPIPEIF Summary of Constraints

The following is a list of register configuration constraints to adhere to when programming the IPIPEIF module. It can be used as a quick checklist. More detailed register setting constraints can be found in the individual register descriptions.

- If BL is the source for the IPIPEIF:
  - The memory output line offset and address must be on 32-byte boundaries.
  - In DFS block, IPIPEIF_LPFR must be 0, because the first line cannot be fetched.
  - IPIPEIF_PPLN IPIPEIF_HNUM
  - IPIPEIF_LPFR IPIPEIF_VNUM + 1
- There are restrictions on IPIPEIF_CFG1[15:14] INPSRC1 and IPIPEIF_CFG1[3:2] INPSRC2 combinations. See Table 8-314 for details.

8.3.4.4 ISS ISP IPIPE Programming Model

This section describes the low-level hardware programming sequences for the configuration and use of the ISS PIPE module.

8.3.4.4.1 Global Initialization

8.3.4.4.1.1 Surrounding Modules Global Initialization

This initialization of surrounding modules is based on the integration of the ISS ISP.

8.3.4.4.1.2 ISS IPIPE Global Initialization

8.3.4.4.1.2.1 Main Sequence – ISS ISP IPIPE Global Initialization

This procedure initializes the ISS ISP PIPE modules after a POR or software reset.

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Table 8-360. ISS Global Initialization

Step	Register/Bit Field/Programming Model	Value
Set the IPIPE processing modes.	IPIPE_SRC_MODE[0] OST	0x-
Select the IPIPEIF module as a source.	IPIPE_SRC_MODE[1] WRT	0x1
Set the vertical start position of the window to process.	IPIPE_SRC_VPS[15:0] VAL	0x-
Set the horizontal start position of the window to process.	IPIPE_SRC_HPS[15:0] VAL	0x-
Set the vertical size of the processing area.	IPIPE_SRC_VSZ[12:0] VAL	0X-
Set the horizontal size of the processing area.	IPIPE_SRC_HSZ[12:1] VAL	0x-
Enable clk_arm_g0.	IPIPE_GCK_MMR[0] REG	0x-
Enable the clk_pix_g3.	IPIPE_GCK_PIX[3] G3	0x-
Enable the clk_pix_g2.	IPIPE_GCK_PIX[2] G2	0x-
Enable the clk_pix_g1.	IPIPE_GCK_PIX[1] G1	0x-
Enable the clk_pix_g0.	IPIPE_GCK_PIX[0] G0	0x-
Enable IPIPE module.	IPIPE_SRC_EN[0] EN	0x1

8.3.4.4.1.2.2 Subsequence – ISS ISP IPIPE Defect Pixel Correction Initialization

8.3.4.4.1.2.2.1 Subsequence – ISS ISP IPIPE LUT Defect Pixel Correction (LUT DPC)

Table 8-361. ISS ISP IPIPE LUT Defect Pixel Correction (LUT DPC)

Step	Register/Bit Field/Programming Model	Value
Set the address of the first valid data in the LUT.	IPIPE_DPC_LUT_ADR[9:0] ADR	0x-
Set the LUT type.	IPIPE_DPC_LUT_SEL[1] TBL	0x-
Set the size of the LUT.	IPIPE_DPC_LUT_SIZ[9:0] SIZ	0x-
Set the dot replacement correction method .	IPIPE_DPC_LUT_SEL[0] DOT	0x-
Enable LUT DPC.	IPIPE_DPC_LUT_EN[0] EN	0x1

8.3.4.4.1.2.3 Subsequence – ISS ISP IPIPE White Balance Initialization

Table 8-362. ISS ISP IPIPE White Balance Initialization

Step	Register/Bit Field/Programming Model	Value
Set the offset before white balance.	IPIPE_WB2_OFT_R[11:0] VAL IPIPE_WB2_OFT_GR[11:0] VAL IPIPE_WB2_OFT_GB[11:0] VAL IPIPE_WB2_OFT_B[11:0] VAL	0x-
Set the white balance gain.	IPIPE_WB2_WGN_R[12:0] VAL IPIPE_WB2_WGN_GR[12:0] VAL IPIPE_WB2_WGN_GB[12:0] VAL IPIPE_WB2_WGN_B[12:0] VAL	0x-

8.3.4.4.1.2.4 Subsequence – ISS ISP IPIPE RGB2RGB Blending Module Initialization

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Table 8-363. ISS ISP IPIPE RGB2RGB Blending Module Initialization

Step	Register/Bit Field/Programming Model	Value
Set gain range.	IPIPE_RGB1_MUL_RR[11:0] VAL IPIPE_RGB1_MUL_GR[11:0] VAL IPIPE_RGB1_MUL_BR[11:0] VAL IPIPE_RGB1_MUL_RG[11:0] VAL IPIPE_RGB1_MUL_GG[11:0] VAL IPIPE_RGB1_MUL_BG[11:0] VAL IPIPE_RGB1_MUL_RB[11:0] VAL IPIPE_RGB1_MUL_GB[11:0] VAL IPIPE_RGB1_MUL_BB[11:0] VAL	0x-
Se the offset range for each component.	IPIPE_RGB1_OFT_OR[12:0] VAL IPIPE_RGB1_OFT_OG[12:0] VAL IPIPE_RGB1_OFT_OB[12:0] VAL	0x-

8.3.4.4.1.2.5 Subsequence – ISS ISP IPIPE Gamma Correction Module Initialization

Table 8-364. ISS ISP IPIPE Gamma Correction Module Initialization

Step	Register/Bit Field/Programming Model	Value
Select the gamma table.	IPIPE_GMM_CFG[4] TBL	0x-
Set the size of the gamma table.	IPIPE_GMM_CFG[6:5]SIZ	0x-
(optional) Insert bypass bit for each color.	IPIPE_GMM_CFG[0] BYPR IPIPE_GMM_CFG[1] BYPG IPIPE_GMM_CFG[2] BYPB	0x1

8.3.4.4.1.2.6 Subsequence – ISS ISP IPIPE 2nd RGB2RGB Conversion Matrix Initialization

Table 8-365. ISS ISP IPIPE 2nd RGB2RGB Conversion Matrix Initialization

Step	Register/Bit Field/Programming Model	Value
Set the gain range.	IPIPE_RGB2_MUL_RR[10:0] VAL IPIPE_RGB2_MUL_GR[10:0] VAL IPIPE_RGB2_MUL_BR[10:0] VAL IPIPE_RGB2_MUL_RG[10:0] VAL IPIPE_RGB2_MUL_GG[10:0] VAL IPIPE_RGB2_MUL_BG[10:0] VAL IPIPE_RGB2_MUL_RB[10:0] VAL IPIPE_RGB2_MUL_GB[10:0] VAL IPIPE_RGB2_MUL_BB[10:0] VAL	0x-
Set the offset.	IPIPE_RGB2_OFT_OR[10:0] VAL IPIPE_RGB2_OFT_OG[10:0] VAL IPIPE_RGB2_OFT_OB[10:0] VAL	0x-

8.3.4.4.1.2.7 Subsequence – ISS ISP IPIPE RGB2YCbCr Conversion Matrix Initialization

Table 8-366. ISS ISP IPIPE RGB2YCbCr Conversion Matrix Initialization

Step	Register/Bit Field/Programming Model	Value
Set the brightness control.	IPIPE_YUV_ADJ[15:8] BRT	0x-
Set the contrast control.	IPIPE_YUV_ADJ[7:0] CRT	0x-
Configure the gain range.	IPIPE_YUV_MUL_RY[11:0]VAL IPIPE_YUV_MUL_GY[11:0]VAL IPIPE_YUV_MUL_BY[11:0]VAL IPIPE_YUV_MUL_RCB[11:0]VAL IPIPE_YUV_MUL_GCB[11:0]VAL IPIPE_YUV_MUL_BCB[11:0]VAL IPIPE_YUV_MUL_RCR[11:0]VAL IPIPE_YUV_MUL_GCR[11:0]VAL IPIPE_YUV_MUL_BCR[11:0]VAL	0x-

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Table 8-366. ISS ISP IPIPE RGB2YCbCr Conversion Matrix Initialization (continued)

Step	Register/Bit Field/Programming Model	Value
Set the output offset value for Y.	IPIPE_YUV_OFT_Y[10:0] VAL	0x-
Set the output offset value for Cr.	IPIPE_YUV_OFT_CR[10:0] VAL	0x-
Set the output offset value for Cb.	IPIPE_YUV_OFT_CB[10:0] VAL	0x-

8.3.4.4.1.2.8 Subsequence – ISS ISP IPIPE 4:2:2 Conversion Module Initialization

Table 8-367. ISS ISP IPIPE 4:2:2 Conversion Module Initialization

Step	Register/Bit Field/Programming Model	Value
If: RAW BAYER data set as an input?	IPIPE_SRC_FMT.[1:0] FMT	= 0x0
Select the Y and Cb/Cr sampling point.	IPIPE_YUV_PHS[0] POS	0x-
Enable 4:2:2 conversion module.	IPIPE_YUV_PHS[1] PLF	0x-
ELSE		

8.3.4.4.1.2.9 Subsequence – ISS ISP IPIPE 2D Edge Enhancer Initialization

Table 8-368. ISS ISP IPIPE 2D Edge Enhancer Initialization

Step	Register/Bit Field/Programming Model	Value
Set the merging method.	IPIPE_YEE_TYP[0] SEL	0x-
Set the downshift length of HPF in the edge enhancer.	IPIPE_YEE_SHF[3:0] SHF	0x-
Set the edge enhancer lower threshold before referring to the LUT.	IPIPE_YEE_THR[5:0] VAL	0x-
Set the multiplier coefficient in the HPF.	IPIPE_YEE_MUL_00[9:0] VAL IPIPE_YEE_MUL_01[9:0] VAL IPIPE_YEE_MUL_02[9:0] VAL IPIPE_YEE_MUL_10[9:0] VAL IPIPE_YEE_MUL_11[9:0] VAL IPIPE_YEE_MUL_12[9:0] VAL IPIPE_YEE_MUL_20[9:0] VAL IPIPE_YEE_MUL_21[9:0] VAL IPIPE_YEE_MUL_22[9:0] VAL	0x-
Set the edge sharpener HPF value lower limit.	IPIPE_YEE_E_THR_1[11:0] VAL	0x-
Set the edge sharpener HPF value upper limit.	IPIPE_YEE_E_THR_2[5:0] VAL	0x-
Set the edge sharpener gain value on gradient.	IPIPE_YEE_G_GAN[7:0] VAL	0x-
Set the edge sharpener gain value.	IPIPE_YEE_E_GAN[7:0] VAL	0x-
Set the edge sharpener offset value on gradient.	IPIPE_YEE_G_OFT[5:0] VAL	0x-
Enable the 2D edge enhancer.	IPIPE_YEE_EN[0] EN	0x1

8.3.4.4.1.2.10 Subsequence – ISS ISP IPIPE Histogram Initialization

Table 8-369. ISS ISP IPIPE Histogram Initialization

Step	Register/Bit Field/Programming Model	Value
Select input source.	IPIPE_HST_SEL[2] SEL	0x-
Select the Bayer mode.	IPIPE_HST_SEL[1:0] TYP	0x-
Set the number of bins.	IPIPE_HST_PARA[13:12] BIN	0x-
Enable region(area) 0.	IPIPE_HST_PARA[0] RGN0	0x-
Enable region(area) 1.	IPIPE_HST_PARA[1] RGN1	0x-
Enable region(area) 2.	IPIPE_HST_PARA[2] RGN2	0x-

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Table 8-369. ISS ISP IPIPE Histogram Initialization (continued)

Step	Register/Bit Field/Programming Model	Value
Enable region(area) 3.	IPIPE_HST_PARA[3] RGN3	0x-
Set the vertical position of region 0.	IPIPE_HST_0_VPS[12:1] VAL	0x-
Set the vertical position of region 1.	IPIPE_HST_1_VPS[12:1] VAL	0x-
Set the vertical position of region 2.	IPIPE_HST_2_VPS[12:1] VAL	0x-
Set the vertical position of region 3.	IPIPE_HST_3_VPS[12:1] VAL	0x-
Set the horizontal position of region 0.	IPIPE_HST_0_HPS[12:1] VAL	0x-
Set the horizontal position of region 1.	IPIPE_HST_0_HPS[12:1] VAL	0x-
Set the horizontal position of region 2.	IPIPE_HST_0_HPS[12:1] VAL	0x-
Set the horizontal position of region 3.	IPIPE_HST_0_HPS[12:1] VAL	0x-
Set the vertical size of region 0.	IPIPE_HST_0_VSZ[12:1] VAL	0x-
Set the vertical size of region 1.	IPIPE_HST_1_VSZ[12:1] VAL	0x-
Set the vertical size of region 2.	IPIPE_HST_2_VSZ[12:1] VAL	0x-
Set the vertical size of region 3.	IPIPE_HST_3_VSZ[12:1] VAL	0x-
Set the horizontal size of region 0.	IPIPE_HST_0_HSZ[12:1] VAL	0x-
Set the horizontal size of region 1.	IPIPE_HST_1_HSZ[12:1] VAL	0x-
Set the horizontal size of region 2.	IPIPE_HST_2_HSZ[12:1] VAL	0x-
Set the horizontal size of region 3.	IPIPE_HST_3_HSZ[12:1] VAL	0x-
Enable selection of the color pattern 0 (R).	IPIPE_HST_PARA[4] COL0	0x-
Enable selection of the color pattern 1 (G).	IPIPE_HST_PARA[5] COL1	0x-
Enable selection of the color pattern 2 (B).	IPIPE_HST_PARA[6] COL2	0x-
Enable selection of the color pattern 3 (Y).	IPIPE_HST_PARA[7] COL3	0x-
Set the shift length of the input data.	IPIPE_HST_PARA[11:8] SHF	0x-
Enable/disable histogram memory clear.	IPIPE_HST_TBL[1] CLR	0x-
Select table for store the histogram data.	IPIPE_HST_TBL[1] CLR	0x-
IF: Is input from noise filter?	IPIPE_HST_SEL[2] SEl	0x0
Gain for color for R.	IPIPE_HST_MUL_R[7:0]GAIN	0x-
Gain for color for GR.	IPIPE_HST_MUL_GR[7:0]GAIN	0x-
Gain for color for GB.	IPIPE_HST_MUL_GB[7:0]GAIN	0x-
Gain for color for B.	IPIPE_HST_MUL_B[7:0]GAIN	0x-
ENDIF		
Select processing mode.	IPIPE_HST_MODE[0]OST	0x-
Enable histogram.	IPIPE_HST_EN[0] EN	0x1

8.3.4.4.1.2.11 Subsequence – ISS ISP IPIPE Boxcar Initialization

Table 8-370. ISS ISP IPIPE Boxcar Initialization

Step	Register/Bit Field/Programming Model	Value
Select the processing mode.	IPIPE_BOX_MODE[0] OST	0x-
Set the size of blocks.	IPIPE_BOX_TYP[0] SEL	0x-
Set the higher 16 bits of the first address of output in memory.	IPIPE_BOX_SDR_SAD_H[15:0] VAL	0x-
Set the lower 16 bits of the first address of output in memory.	IPIPE_BOX_SDR_SAD_L[15:5] VAL	0x-
Set the downshift value.	IPIPE_BOX_SHF[2:0] VAL	0x-
Enable boxcar.	IPIPE_BOX_EN[0] EN	0x1

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8.3.4.4.2 ISS ISP IPIPE Operational Modes Configuration

8.3.4.4.2.1 ISS ISP IPIPE Processing Path: Case 1 Configuration

Table 8-371. ISS ISP IPIPE Processing Path: Case 1 Configuration

Step	Register/Bit Field/Programming Model	Value
Select processing path: Case 1	IPIPE_SRC_FMT[1:0] FMT	0x0
Configure IPIPE DPC.	See Section 8.3.4.4.1.2.2, *Subsequence – ISS ISP IPIPE Defect Pixel Correction Initialization*.	
Configure IPIPE white balance.	See Section 8.3.4.4.1.2.3, *Subsequence – ISS ISP IPIPE White Balance Initialization*.	
Configure IPIPE RGB2RGB blending module.	See Section 8.3.4.4.1.2.4, *Subsequence – ISS ISP IPIPE RGB2RGB Blending Module Initialization*.	
Configure IPIPE gamma correction module.	See Section 8.3.4.4.1.2.5, *Subsequence – ISS ISP IPIPE Gamma Correction Module Initialization*.	
Configure IPIPE 2nd RGB2RGB conversion matrix.	See Section 8.3.4.4.1.2.6, *Subsequence – ISS ISP IPIPE 2nd RGB2RGB Conversion Matrix Initialization*.	
Configure IPIPE RGB2YCbCr conversion matrix.	See Section 8.3.4.4.1.2.7, *Subsequence – ISS ISP IPIPE RGB2YCbCr Conversion Matrix Initialization*.	
Configure IPIPE 2D edge enhancer.	See Section 8.3.4.4.1.2.9, *Subsequence – ISS ISP IPIPE 2D Edge Enhancer Initialization*.	
Enable IPIPE module.	IPIPE_SRC_EN[0] EN	0x1

8.3.4.4.2.2 ISS ISP IPIPE Processing Path: Case 2 Configuration

Table 8-372. ISS ISP IPIPE Processing Path: Case 2 Configuration

Step	Register/Bit Field/Programming Model	Value
Select processing path: Case 2.	IPIPE_SRC_FMT[1:0] FMT	0x1
Configure IPIPE DPC.	See Section 8.3.4.4.1.2.2, *Subsequence – ISS ISP IPIPE Defect Pixel Correction Initialization*.	
Configure IPIPE white balance.	See Section 8.3.4.4.1.2.3, *Subsequence – ISS ISP IPIPE White Balance Initialization*.	
Enable IPIPE module.	IPIPE_SRC_EN[0] EN	0x1

8.3.4.4.2.3 ISS ISP IPIPE Processing Path: Case 3 Configuration

Table 8-373. ISS ISP IPIPE Processing Path: Case 3 Configuration

Step	Register/Bit Field/Programming Model	Value
Select processing path: Case 3.	IPIPE_SRC_FMT[1:0] FMT	0x3
Configure IPIPE 2D edge enhancer.	See Section 8.3.4.4.1.2.9, *Subsequence - ISS ISP IPIPE 2D Edge Enhancer Initialization*.	
Enable IPIPE module.	IPIPE_SRC_EN[0] EN	0x1

8.3.4.4.2.4 ISS ISP IPIPE Processing Path: Case 4 Configuration

Table 8-374. ISS ISP IPIPE Processing Path: Case 4 Configuration

Step	Register/Bit Field/Programming Model	Value
Select processing path: Case 4.	IPIPE_SRC_FMT[1:0] FMT	0x2
Configure IPIPE boxcar.	See Section 8.3.4.4.1.2.11, *Subsequence – ISS ISP IPIPE Boxcar Initialization*.	

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Table 8-374. ISS ISP IPIPE Processing Path: Case 4 Configuration (continued)

Step	Register/Bit Field/Programming Model	Value
Configure IPIEE histogram.	See Section 8.3.4.4.1.2.10, *Subsequence – ISS ISP IPIPE Histogram Initialization*.	
Enable IPIPE module.	IPIPE_SRC_EN[0] EN	0x1

8.3.4.5 ISS ISP RSZ Programming Model

This section discusses programming configuration steps related to software control of the RSZ. It lists the registers that must be programmed in different modes, describes how to enable and disable the RSZ and how to check the status of the image resizing procedure, and discusses the different register access types and several programming constraints.

8.3.4.5.1 ISS ISP RSZ Hardware Setup/Initialization

This section discusses the configuration of the RSZ required before image processing can begin.

8.3.4.5.1.1 ISS ISP RSZ Surrounding Modules Global Initialization

This section identifies the requirements for initializing the surrounding modules when the RSZ module is to be used for the first time after a device reset. This initialization of surrounding modules is based on the integration and environment of the RSZ. For more information, see Section 8.3.3.5.4, *ISS ISP RSZ Integration.*.

Table 8-375. ISS ISP RSZ Surrounding Modules Global Initialization

Surrounding Modules	Comments
PRCM	Module interface and functional clocks must be enabled. RSZ is part of ISP, which is part of ISS. To enable the clocks for ISS, see Chapter 3, *Power, Reset, and Clock Management*. Also see Section 8.3.2.1.1, *ISS ISP Clocks*.
(optional) MPU INTC	The MPU INTC must be configured to enable interrupts from the RSZ. For information about how to configure the local ISS interrupt channels, see Section 8.3.2.2, *ISS ISP Interrupt Tree* , and Section 8.1.2.1.1, *ISS Interrupt Merger*. Then, to configure the outside ISS boundary channels, see Chapter 17, *Interrupt Controllers*.
(optional) IPIPE	Configure the IPIPE module to process and pass data to the RSZ module. See Section 8.3.4.4, *ISS ISP IPIPE Programming Model* .
(optional) IPIPEIF	Configure the IPIPEIF module to process and pass data to the RSZ module. See Section 8.3.4.3, *ISS ISP IPIPEIF Programming Model* .
(optional) BL	Configure the BL for reading back data from memory. See Section 8.3.4.7, *ISS ISP BL Programming Model* .
(optional) CSI2	If the data comes from the sensor, configure the CSI2-A interface. See Section 8.2.5.4, *ISS CSI2 Programming Model*.
(optional) CCP2	If the data comes from the sensor, configure the CCP2 interface. See Section 8.2.4.4, *ISS CCP2 Programming Model*.

NOTE: The MPU INTC configurations are necessary if the interrupt-based communication modes are used. The IPIPE or IPIPEIF configuration is also necessary for putting data into the RSZ. Moreover, if data comes from memory, the BL must be configured. If data comes from the image sensor CSI2 or CCP2, the interface must be configured.

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8.3.4.5.1.2 ISS ISP RSZ Initial Register Setup

Before enabling the RSZ, the hardware must be properly configured through register writes. Table 8-376 identifies the sequence to be used before enabling the hardware.

Table 8-376. ISS ISP RSZ Initial Register Setup

Step	Register/Bit Field/Programming Model	Value
Set the MMR clock to enable RSZ register read/write access.	RSZ_GCK_MMR[0] MMR	0x1
Determine whether or not a bypass mode will be used and set the RSZ core functional clock accordingly.	RSZ_GCK_SDR[0] CORE	0x-
IF: Is the core clock enabled?	RSZ_GCK_SDR[0] CORE	= 0x1
Enable RSZ engine clocks.	RSZ_SYSCONFIG[8] RSZA_CLK_EN RSZ_SYSCONFIG[9] RSZB_CLK_EN	0x1
ELSE: The input data buffer in not used?	RSZ_GCK_SDR[0] CORE	= 0x0
Set the bypass mode accordingly.	RSZ_SRC_FMT0[1] BYPASS	0x-
ENDIF		
Enable the RSZ core clock.	RSZ_GCK_SDR[0] CORE	0x1
Determine the upscale ratio and functional clock, and adjust the fractional clock divider as appropriate.	RSZ_FRACDIV[15:0] RSZ_FRACDIV	0x-
Set the low threshold of the RSZ input data buffer as appropriate.	RSZ_IN_FIFO_CTRL[28:16] THRLD_LOW	0x-
Set the high threshold of the RSZ input data buffer as appropriate.	RSZ_IN_FIFO_CTRL[12:0] THRLD_HIGH	0x-
Determine whether IPIPE or IPEPIF will be the source of input and set this bit accordingly.	RSZ_SRC_FMT0[0] SEL	0x-
Determine whether the RSZ will process as long as data is present in the input buffer, or whether it will wait for a WEN signal from the input source (IPIPE or IPIPEIF) to process lines arrived only during WEN high state.	RSZ_SRC_MODE[1] WRT	0x-
Select the processing mode (one shot or free running). This bit controls the RSZ module. There are also additional mode settings for the two RSZ engines within. After RSZ reset, the mode is automatically set to free running.	RSZ_SRC_MODE[0] OST	0x-
Configure the number of interrupt intervals for writing lines into CBUFF for the two RSZ engines.	RSZ_IRQ_RZA[12:0] RZA RSZ_IRQ_RZB[12:0] RZB	0x-
Enable the RSZ module.	RSZ_SRC_EN[0] EN	0x1
Enable the RSZ engine A.	RZA_EN[0] EN	0x1
Enable the RSZ engine B.	RZB_EN[0] EN	0x1

NOTE: RSZ engine A or RSZ engine B must be enabled after setting all needed configuration parameters.

8.3.4.5.1.3 ISS ISP RSZ Reset Behavior

Because the RSZ module has no software reset, software can issue one at the ISP level. Moreover, upon hardware reset, all the registers in the RSZ are reset to their reset values. Table 8-377 identifies the proper software sequence before and after RSZ reset issues at the ISP level.

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Table 8-377. ISS ISP RSZ Reset Behavior

Step	Register/Bit Field/Programming Model	Value
ELSE IF: Is FIFO overflow or blanking error present?	ISP5_IRQSTATUS_i[18] RSZ_FIFO_IN_OVF or ISP5_IRQSTATUS_[19] RSZ_FIFO_IN_BLK_ERR	= 0x1
Clear the FIFO blanking event.	ISP5_IRQENABLE_CLR_i[19] RSZ_FIFO_IN_BLK_ERR	0x1
Clear the overflow event.	SP5_IRQENABLE_CLR_i[18] RSZ_FIFO_IN_OVF	0x1
ELSE: No FIFO overflow or blanking error is present?		
Wait until there is no DMA process and the module ready for reset.	ISP5_SYSCONFIG[1] SOFTRESET and ISP5_IRQSTATUS_i[15] RSZ_INT_DMA	= 0x0
ENDIF		
Disable the source data.	RSZ_SRC_EN[0] EN	0x0
Reset the RSZ at the ISP level.	ISP5_SYSCONFIG[1] SOFTRESET	0x1
Check whether the RSZ has been reset properly.	ISP5_SYSCONFIG[1] SOFTRESET	0x-

8.3.4.5.2 ISS ISP RSZ Global Image Processing Settings

This section discusses the configuration of the RSZ global settings before/during image frame processing. Table 8-378 identifies the global RSZ functional sequence, which includes global control, frame settings, bandwidth control, and reversal output image frames.

Table 8-378. ISS ISP RSZ Global Image Processing Settings

Step	Register/Bit Field/Programming Model	Value
Initialize the RSZ module.	See Section 8.3.4.5.1.	
Determine input data type and configure the source parameters.	See Section 8.3.4.5.2.1.	
Determine if vertical flip of the output image will be performed by the two RSZ engines and set accordingly.	RSZ_SEQ[1] VRVA RSZ_SEQ[3] VRVB	0x-
Determine if horizontal flip of the output image will be performed by the two RSZ engines and set accordingly.	RSZ_SEQ[0] HRVA RSZ_SEQ[2] HRVB	0x-
Set the baseline address of the RSZ output to CBUFF. Best performance can be achieved by assigning address on a 128-byte boundary.	RZA_SDR_Y_BAD_H[15:0] Y_BAD_H RZA_SDR_Y_BAD_L[15:0] Y_BAD_L RZB_SDR_Y_BAD_H[15:0] Y_BAD_H RZB_SDR_Y_BAD_L[15:0] Y_BAD_L RZA_SDR_C_BAD_H[15:0] C_BAD_H RZA_SDR_C_BAD_L[15:0] C_BAD_L RZB_SDR_C_BAD_H[15:0] C_BAD_H RZB_SDR_C_BAD_L[15:0] C_BAD_L	0x-

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Table 8-378. ISS ISP RSZ Global Image Processing Settings (continued)

Step	Register/Bit Field/Programming Model	Value
Set the start address of the RSZ output to CBUFF. The first data output will be written to this address. If the first line of a frame is written at the beginning of the CBUFF memory, then SAD = BAD and PTR_S = 0. It is strongly advised to set up this address on a 128-byte boundary, which will lead to the best performance.	RZA_SDR_Y_SAD_H[15:0] Y_SAD_H	0x-
	RZA_SDR_Y_SAD_L[15:0] Y_SAD_L	
	RZB_SDR_Y_SAD_H[15:0] Y_SAD_H	
	RZB_SDR_Y_SAD_L[15:0] Y_SAD_L	
	RZA_SDR_C_SAD_H[15:0] C_SAD_H	
	RZA_SDR_C_SAD_L [15:0] C_SAD_L	
	RZB_SDR_C_SAD_H[15:0] C_SAD_H	
	RZB_SDR_C_SAD_L[15:0] C_SAD_L	
Set the start pointer of the CBUFF internal counter. It must be set up as PTR_S = (SAD – BAD) / OFT. PTR_S is expressed in number of lines.	RZA_SDR_Y_PTR_S[12:0] Y_PTR_S	0x-
	RZB_SDR_Y_PTR_S[12:0] Y_PTR_S	
	RZA_SDR_C_PTR_S[12:0] C_PTR_S	
	RZB_SDR_C_PTR_S[12:0] C_PTR_S	
Set the end pointer of the CBUFF internal counter. PTR_E is expressed in number of lines. The CBUFF can contain up to PTR_E lines.	RZA_SDR_Y_PTR_E[12:0] Y_PTR_E	0x-
	RZB_SDR_Y_PTR_E[12:0] Y_PTR_E	
	RZA_SDR_C_PTR_E[12:0] C_PTR_E	
	RZB_SDR_C_PTR_E[12:0] C_PTR_E	
Set the line of offset expressed in bytes between two lines in the CBUFF (Line 0 = SAD, Line 1 = SAD + 1 x OFT, Line 2 = SAD + 2 x OFT). PTR_E is expressed in number of lines. The CBUFF can contain up to PTR_E lines. Note: OFT does not necessarily correspond to the size of a line in a frame; it can be much bigger. The line offset must be a multiple of 128 bytes.	RZA_SDR_Y_OFT[16:0] Y_OFT	0x-
	RZB_SDR_Y_OFT[16:0] Y_OFT	
	RZA_SDR_C_OFT[16:0] C_OFT	
	RZB_SDR_C_OFT[16:0] C_OFT	
Determine output data type, whether it will be flipped, and configure the output memory addresses.	See Section 8.3.4.5.2.2.	

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NOTE: When data output is 4:2:2 or 4:2:0-Y only, the following values are not needed:

- RZx_SDR_C_BAD_x
- RZx_SDR_C_SAD_x
- RZx_SDR_C_PTR_S
- RZx_SDR_C_PTR_E
- RZx_SDR_C_OFT

When output is 4:2:0-C only, the following values are not needed:

- RZx_SDR_Y_BAD_x
- RZx_SDR_Y_SAD_x
- RZx_SDR_Y_PTR_S
- RZx_SDR_Y_PTR_E
- RZx_SDR_Y_OFT

8.3.4.5.2.1 ISS ISP RSZ Global Image Processing Settings – Subsequence 1

The procedure shown in Figure 8-239 determines which of the RSZ engines is enabled and the type of input data, and configures the source data parameters.

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Figure 8-239. ISS ISP RSZ Global Image Processing Settings – Subsequence 1

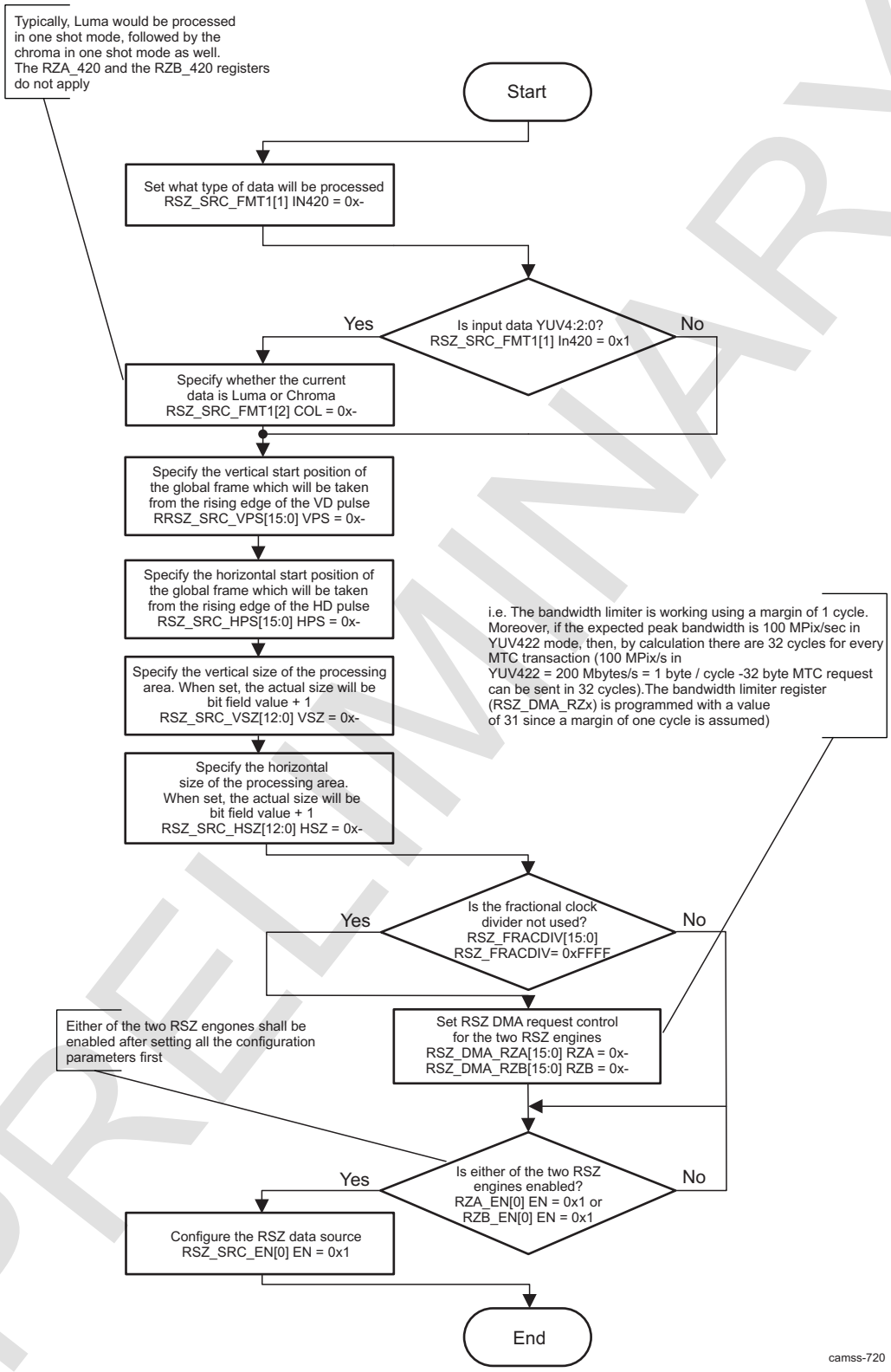

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Table 8-379. Register Call Summary for ISS ISP RSZ Global Image Processing Settings – Subsequence 1

Register Name	Register Name	Register Name
RZA_420[1] CEN	RZA_420[0] YEN	RSZ_SRC_FMT1[1] IN420
RZB_420[0] CEN	RZB_420[1] YEN	RSZ_SRC_FMT1[2] COL
RSZ_SRC_EN[0] EN	RSZ_SRC_VPS[15:0] VPS	RSZ_SRC_HPS[15:0] HPS
RSZ_SRC_VSZ[12:0] VSZ	RSZ_SRC_HSZ[12:0] HSZ	RSZ_FRACDIV[15:0] RSZ_FRACDIV
RSZ_DMA_RZA[15:0] RZA	RSZ_DMA_RZB[15:0] RZB	

8.3.4.5.2.2 ISS ISP RSZ Global Image Processing Settings – Subsequence 2

The procedure shown in Figure 8-240 determines the type of output data and whether it will be flipped. Then it configures the RSZ engines accordingly.

Figure 8-240. ISS ISP RSZ Global Image Processing Settings – Subsequence 2

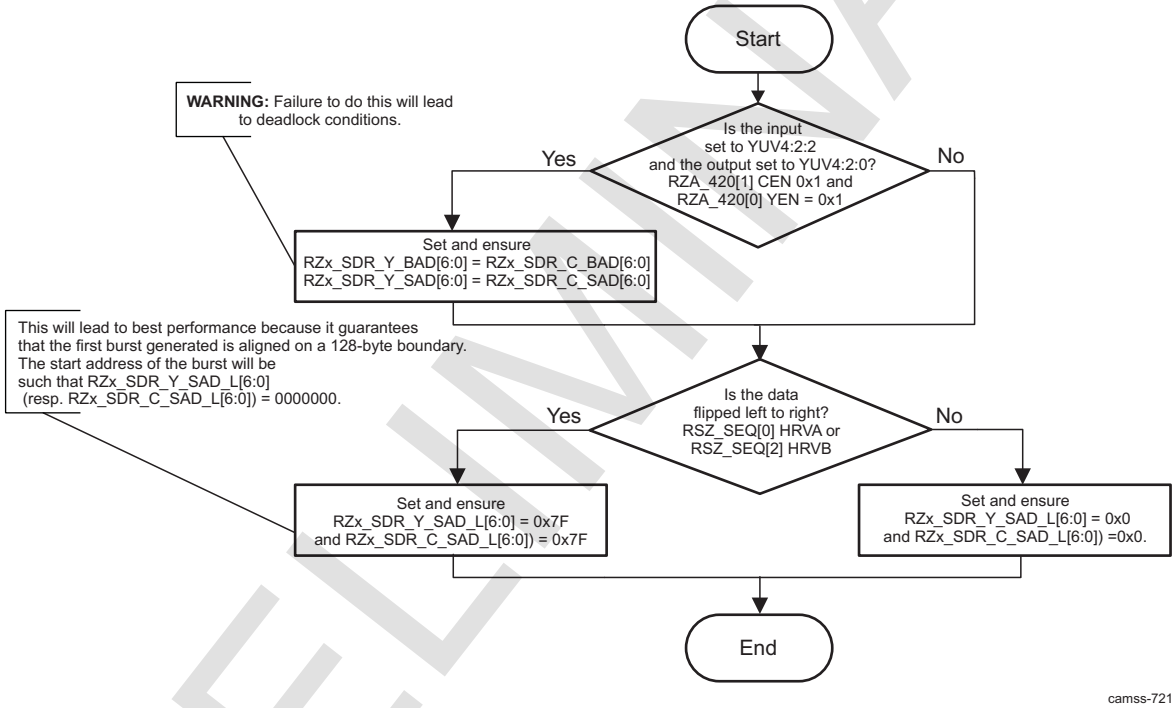

Table 8-380. Register Call Summary for ISS ISP RSZ Global Image Processing Settings – Subsequence 2

Register Name	Register Name	Register Name
RZA_420[1] CEN	RZA_420[0] YEN	RZB_420[1] CEN
RZB_420[0] YEN	RZA_SDR_Y_SAD_L	RZA_SDR_C_SAD_L
RZB_SDR_Y_SAD_L	RZB_SDR_C_SAD_L	RSZ_SEQ[0] HRVA
RSZ_SEQ[2] HRVB		

8.3.4.5.3 ISS ISP RSZ Engines Interframe Image Processing Settings

This section discusses the configuration of the RSZ interframe image processing. Table 8-381 identifies the setup sequence for the two different engines within the RSZ module.

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Table 8-381. ISS ISP RSZ Engines Interframe Image Processing Settings

Step	Register/Bit Field/Programming Model	Value
IF: Is the resizer module set to free-running mode?	RSZ_SRC_MODE[0] OST	= 0x0
Set either of the engines to free-running mode to keep popping data out of the internal buffer. Otherwise, it will lead to an overflow event after the first frame.	RZA_MODE[0] MODE RZB_MODE[0] MODE	0x0
ELSE: Is the resizer module set to one-shot mode?		
Set both RSZ engines to one-shot mode.	RZA_MODE[0] MODE RZB_MODE[0] MODE	0x1
ENDIF		
Set the output format. See Table 8-326.	RZA_420[0] YEN RZA_420[1] CEN RZB_420[0] YEN RZB_420[1] CEN	0x-
On the side of the RSZ_SRC_VPS, RSZ_SRC_HPS, RSZ_SRC_VSZ, and RSZ_SRC_HSZ registers, set the engine complementary function to crop within the global frame and assign proper vertical start position of the input frame.	RZA_I_VPS[12:0] VPS RZB_I_VPS[12:0] VPS	0x-
Assign proper horizontal start position of the input frame.	RZA_I_HPS[12:0] HPS RZB_I_HPS[12:0] HPS	0x-
Assign proper vertical size of the output frame.	RZA_O_VSZ[12:0] VPS RZB_O_VSZ[12:0] VPS	0x-
Assign proper horizontal size of the output frame.	RZA_O_HSZ[12:1] HPS RZB_O_HSZ[12:1] HPS	0x-
Set the phase position for the Chroma and Luma element and configure the averager.	See Section 8.3.4.5.3.1	
Set the vertical resize value for the two engines. (vertical resize ration = 256 / RZx_V_DIF).	RZA_V_DIF[13:0] V RZB_V_DIF[13:0] V	0x-
Set the horizontal resize value for the two engines. (horizontal resize ration = 256 / RZx_H_DIF).	RZA_H_DIF[13:0] H RZB_H_DIF[13:0] H	0x-
Select vertical method of resizing filtering (linear or cubic interpolation) for the Luma and Chroma elements.	RZA_V_TYP[0] Y RZB_V_TYP[0] Y RZA_V_TYP[1] C RZB_V_TYP[1] C	0x-
Select horizontal method of resizing filtering (linear or cubic interpolation) for the Luma and Chroma elements.	RZA_H_TYP[0] Y RZB_H_TYP[0] Y RZA_H_TYP[1] C RZB_H_TYP[1] C	0x-
IF: Is the interpolation method linear?	RZx_V_TYP[0] Y **AND** RZx_V_TYP[1] C RZx_H_TYP[0] Y **AND** RZx_H_TYP[1] C	= 0x1
Set the needed vertical LPF intensity for the Luma and Chroma elements.	RZA_V_LPF[5:0] Y RZA_V_LPF[11:6] C RZB_V_LPF[5:0] Y RZB_V_LPF[11:6] C	0x-
Set the needed horizontal LPF intensity for the Luma and Chroma elements.	RZA_H_LPF[5:0] Y RZA_H_LPF[11:6] C RZB_H_LPF[5:0] Y RZB_H_LPF[11:6] C	0x-
ENDIF		
Set the Chroma saturation MAX and MIN values.	RSZ_YUV_C_MAX[7:0] MAX RSZ_YUV_C_MIN[7:0] MIN	0x-
Set the Luma saturation MAX and MIN values.	RSZ_YUV_Y_MAX[7:0] MAX RSZ_YUV_Y_MIN[7:0] MIN	0x-

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Table 8-381. ISS ISP RSZ Engines Interframe Image Processing Settings (continued)

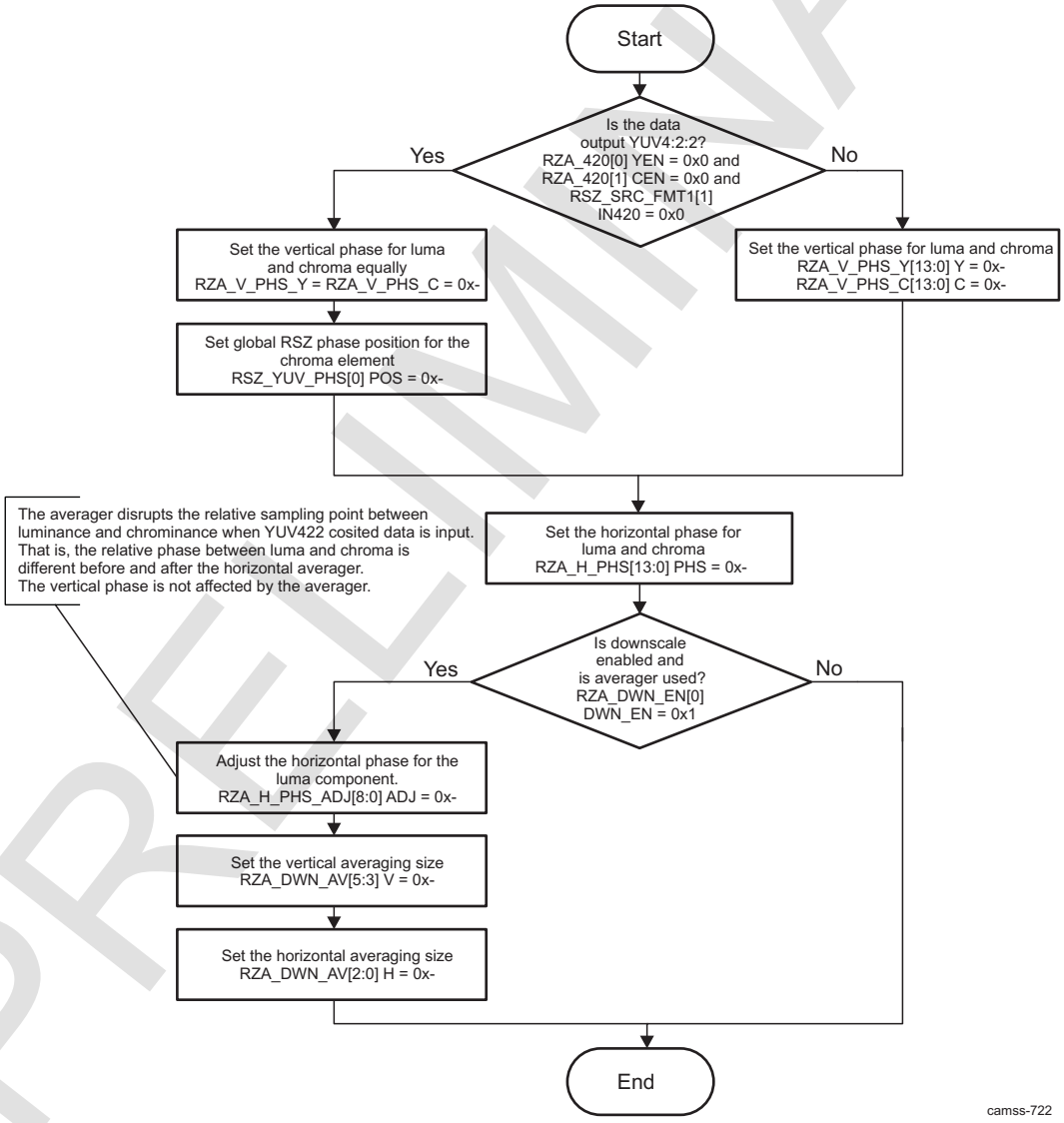
Step	Register/Bit Field/Programming Model	Value
(optional)Set the mode to RGB conversion, configure the alpha value and set additional pixel masking.	See Section 8.3.4.5.3.2.	

8.3.4.5.3.1 ISS ISP RSZ Engines Interframe Image Processing Settings – Subsequence 1

The procedure shown in Figure 8-241 sets the phase position for the Chroma and Luma elements and configures the averager.

NOTE: This procedure configures RSZ engine A. The procedure for RSZ engine B is identical.

Figure 8-241. ISS ISP RSZ Engines Interframe Image Processing Settings – Subsequence 1



NOTE: When masking is used, boundaries affect the leftmost/rightmost 2 pixels in up-conversion.

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Table 8-382. Register Call Summary for ISS ISP RSZ Engines Interframe Image Processing Settings – Subsequence 1

Register Name	Register Name	Register Name
RZA_420[0] YEN	RZA_420[1] CEN	RSZ_SRC_FMT1[1] IN420
RZA_V_PHS_Y	RZA_V_PHS_C	RSZ_YUV_PHS[0] POS
RZA_V_PHS_Y[13:0] Y	RZA_V_PHS_C[13:0] C	RZA_H_PHS [13:0] PHS
RZA_DWN_EN[0] DWN_EN	RZA_H_PHS_ADJ[8:0] ADJ	RZA_DWN_AV[5:3] V
RZA_DWN_AV[2:0] H		

8.3.4.5.3.2 ISS ISP RSZ Engines Interframe Image Processing Settings – Subsequence 2

The procedure shown in Figure 8-242 sets the mode to RGB conversion, configures the alpha value, and sets additional pixel masking.

NOTE: This procedure configures RSZ engine A. The procedure for RSZ engine B is identical.

Figure 8-242. ISS ISP RSZ Engines Interframe Image Processing Settings – Subsequence 2

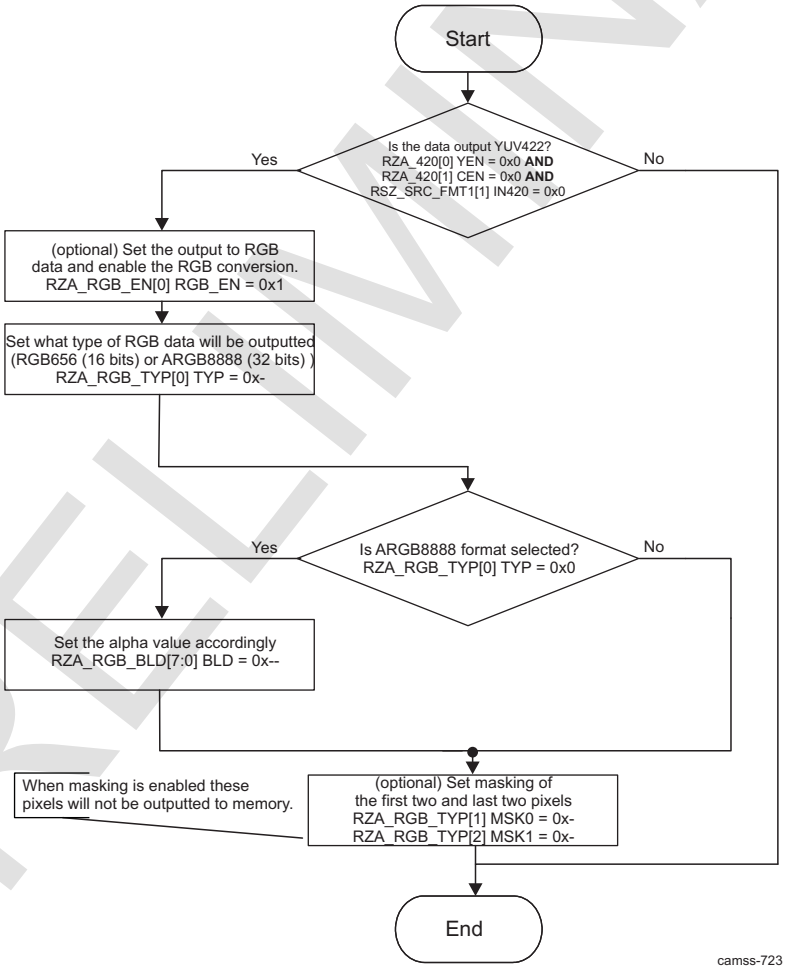

Table 8-383. Register Call Summary for ISS ISP RSZ Engines Interframe Image Processing Settings – Subsequence 2

Register Name	Register Name	Register Name
RZA_420[0] YEN	RZA_420[1] CEN	RSZ_SRC_FMT1[1] IN420

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Table 8-383. Register Call Summary for ISS ISP RSZ Engines Interframe Image Processing Settings – Subsequence 2 (continued)

Register Name	Register Name	Register Name
RZA_RGB_EN[0] RGB_EN	RZA_RGB_TYP[0] TYP	RZA_RGB_BLD[7:0] BLD
RZA_RGB_TYP[1] MSK0	RZA_RGB_TYP[2] MSK1	

8.3.4.5.4 ISS ISP RSZ Programming Constraints

The RSZ module contains shadowed and nonshadowed registers. Shadowed registers can be updated anytime during the resizing operation, but the new setting does not take effect until the next rsz_int_reg event. Shadowed registers can be updated for the next frame after the rsz_int_reg event triggers.

Nonshadowed registers must be programmed before enabling the RSZ module or between frames (that is, after the rsz_int_dma and the entire frame have come on the VPORT IF, and before the VD of the next frame). Table 8-384 list the nonshadowed registers.

Table 8-384. ISS ISP RSZ Nonshadowed Registers

Nonshadowed Registers
RSZ_SYSCONFIG
RSZ_IN_FIFO_CTRL
RSZ_GCK_MMR
RSZ_GCK_SDR
RSZ_SRC_MODE
RSZ_SRC_FMT0
RSZ_SRC_VPS
RSZ_SRC_HPS
RSZ_SRC_EN

8.3.4.6 ISS ISP H3A Programming Model

This section discusses issues related to the software control of the H3A module. It lists which registers are required to be programmed in different modes, how to enable and disable the H3A, how to check the status of the H3A, discusses the different register access types, and enumerates several programming constraints.

8.3.4.6.1 ISS ISP H3A Hardware Setup/Initialization

This section discusses the configuration of the H3A required before image processing can begin.

8.3.4.6.1.1 ISS ISP H3A Reset Behavior

Upon hardware reset of the ISP, all the registers in the H3A are reset to their reset values.

8.3.4.6.1.2 ISS ISP H3A Register Setup

For register configuration purposes, the AF and AEW engines of the H3A can be configured independently. Because there are separate enable bits for each engine, this section is divided into the AF engine and the AEW engine.

8.3.4.6.1.2.1 ISS ISP H3A AF Engine

Before enabling the AF engine, the hardware must be properly configured through register writes. Table 8-385 lists the register parameters that must be programmed before enabling the AF engine of the H3A.

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Table 8-385. ISS ISP H3A AF Engine Required Configuration Parameters

Step	Configuration Required	Value
AF optional preprocessing settings		
Note: A suggestion is to use the averaging filter in the IPIPEIF to reduce noise before generating AF statistics.		
Enable or disable the median filter.	H3A_PCR[2] AF_MED_EN	
Set the median filter threshold, if the filter is enabled.	H3A_PCR[10:3] MED_TH	
Enable or disable A-Law compression.	H3A_PCR[1] AF_ALAW_EN	
Set AF general settings.		
Set the focus value accumulation mode.	H3A_PCR[14] FVMODE	
Set the input start information.	H3A_LINE_START[31:16] SLV H3A_LINE_START[15:0] LINE_START	
Set the output SDRAM destination start address.	H3A_AFBUFST[31:5] AFBUFST	
RGB pixel extraction and paxel settings		
Set the RGB positions in the pixel.	H3A_PCR[13:11] RGBPOS	
Set the paxel width.	H3A_AFPAX1[23:16] PAXW	
Set the paxel height.	H3A_AFPAX1[7:0] PAXH	
Set the paxel horizontal start position.	H3A_AFPAXSTART[27:16] PAXSH	
Set the paxel vertical start position.	H3A_AFPAXSTART[11:0] PAXSV	
Set the column increment.	H3A_AFPAX2[20:17] AFINCH	
Set the line increment.	H3A_AFPAX2[16:13] AFINCV	
Set the vertical paxel count.	H3A_AFPAX2[12:6] PAXVC	
Set the horizontal paxel count.	H3A_AFPAX2[5:0] PAXHC	
Horizontal focus value calculator settings		
Set the horizontal threshold for the two IIR.	H3A_HVF_THR[31:16] HTHR2 H3A_HVF_THR[15:0] HTHR1	
Set the IIR horizontal start position.	H3A_AFIIRSH[11:0] IIRSH	
Set the coefficients for the SET 0 IIR.	H3A_AFCOEF010 H3A_AFCOEF032 H3A_AFCOEF054 H3A_AFCOEF076 H3A_AFCOEF098 H3A_AFCOEF0010	
Set the coefficients for the SET 1 IIR.	H3A_AFCOEF110 H3A_AFCOEF132 H3A_AFCOEF154 H3A_AFCOEF176 H3A_AFCOEF198 H3A_AFCOEF1010	
Vertical focus value calculator settings		
Enable or disable vertical AF focus value calculation.	H3A_PCR[20] AF_VF_EN	
Set the vertical FIR 1 coefficients and threshold.	H3A_VFV_CFG1 H3A_VFV_CFG2	
Set the vertical FIR 2 coefficients and threshold.	H3A_VFV_CFG3 H3A_VFV_CFG4	

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The following references offer guidelines on how to program the filter coefficients and make use of the H3A output.

- V. Peddigari, M. Gamadia, and N. Kehtarnavaz, *Real-time implementation issues in passive automatic focusing for digital still cameras*, Journal of Imaging Science and Technology, vol. 49, no. 2, pp. 114-123, Mar/Apr 2005.
- M. Gamadia and N. Kehtarnavaz, *A real-time continuous automatic focus algorithm for digital cameras*, in Proceedings of IEEE Southwest Symposium on Image Analysis and Interpretation 2006, pp. 163 - 167, Mar. 2006.
- M. Gamadia, N. Kehtarnavaz, and K. Roberts-Hoffman, *Low-light auto-focus enhancement for digital and cell-phone camera image pipelines*, IEEE Transactions on Consumer Electronics, vol. 53, no. 2, pp. 249-257, May 2007.

8.3.4.6.1.2.2 ISS ISP H3A AEW Engine

Before enabling the AEW engine, the hardware must be properly configured through register writes. Table 8-386 lists the register parameters that must be programmed before enabling the AEW engine of the H3A.

Table 8-386. ISS ISP H3A AEW Engine Required Configuration Parameters

Step	Configuration Required	Value
AEW optional preprocessing settings		
Enable or disable the median filter.	H3A_PCR[19] AEW_MED_EN	
Set the median filter threshold.	H3A_PCR[10:3] MED_TH	
Enable or disable A-Law compression.	H3A_PCR[17] AEW_ALAW_EN	
Set AEW general settings.		
Set the saturation limit.	H3A_PCR[31:22] AVE2LMT	
Set the AE/AWB output format.	H3A_AEWCFG[9:8] AEFMT	
Set the AE/AWB shift value for sum of pixels.	H3A_AEWCFG[3:0] SUMFST	
Set the input start information.	H3A_LINE_START[31:16] SLV H3A_LINE_START[15:0] LINE_START	
Set the output SDRAM destination start address.	H3A_AEWBUFST[31:5] AEWBUFST	
Set the AE/AWB window configuration settings.		
Set the window width (in pixels).	H3A_AEWWIN1[20:13] WINW	
Set the window height (in lines).	H3A_AEWWIN1[31:24] WINH	
Set the window count for horizontal direction.	H3A_AEWWIN1[5:0] WINHC	
Set the window count for vertical direction.	H3A_AEWWIN1[12:6] WINVC	
Set the window start position H.	H3A_AEWINSTART[11:0] WINSH	
Set the window start position V.	H3A_AEWINSTART[27:16] WINSV	
Set the horizontal distance between subsamples.	H3A_AEWSUBWIN[3:0] AEWINCH	
Set the vertical distance between subsamples.	H3A_AEWSUBWIN[11:8] AEWINCV	
Set the vertical start position for single black line of windows.	H3A_AEWINBLK[27:16] WINSV	
Set the height for the single black line of windows.	H3A_AEWINBLK[6:0] WINH	

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8.3.4.6.2 ISS ISP H3A Enable/Disable Hardware

Setting the H3A_PCR[0] AF_EN bit enables the AF engine, and setting the H3A_PCR[16] AEW_EN bit enables the AEW engine. This is done after all of the required registers discussed in the previous section are programmed.

The H3A operates in continuous mode. Processing of the frame is dependent on the timing of the IPIPEIF. To ensure that data from the IPIPEIF is not missed, the H3A must be enabled before the IPIPEIF. In this way, the H3A waits for data from the IPIPEIF. The AF engine or the AEW engine can be disabled by clearing the H3A_PCR[0] AF_EN or H3A_PCR[16] AEW_EN bit, respectively, during the processing of the last frame. The disable is latched in at the end of the frame in which it was written.

8.3.4.6.3 ISS ISP H3A Register Accessibility During Frame Processing

There are two types of register access in the H3A module:

- Shadow registers

  These registers/fields can be read and written (if the field is writable) at any time. However, the written values take effect only at the start of a frame. Reads still return the most recent write even though the settings are not used until the next start of frame.

  The only shadowed registers in the H3A module are:

  – H3A_AFPAX1
  – H3A_AFPAX2
  – H3A_AFPAXSTART
  – H3A_AFIIRSH
  – H3A_AEWWIN1
  – H3A_AEWINSTART
  – H3A_AEWINBLK
  – H3A_AEWSUBWIN
  – H3A_AEWCFG
  – H3A_AEWBUFST

- Busy-lock registers

  All other registers, except those described previously, belong to this category.

  Busy-lock registers cannot be written when the module is busy (H3A_PCR[15] BUSYAF == 1 OR H3A_PCR[18] BUSYAEAWB == 1). Writes are allowed to occur, but no change occurs in the registers (blocked writes from the hardware perspective, but allowed write from the software perspective). Once the busy bit in the H3A_PCR register (H3A_PCR[15] BUSYAF or H3A_PCR[18] BUSYAEAWB bit) is reset to 0, the busy-lock registers can be written.

The ideal procedure for changing the H3A registers if (H3A_PCR[15] BUSYAF == 0 or H3A_PCR[18] BUSYAEAWB == 0) or if (EOF interrupt occurs) is:

1. Disable AF or AE/AWB.
2. Change registers.
3. Enable AF or AE/AWB.

8.3.4.6.4 ISS ISP H3A Interframe Operations

Between frames, it may be necessary to modify the memory pointers before processing the next frame. Because the H3A_PCR register and memory pointer registers are shadowed, these modifications can take place any time before the end of the frame, and the data will be latched in for the next frame. The host controller can perform these changes upon receiving an interrupt.

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8.3.4.6.5 ISS ISP H3A Summary of Constraints

The following is a list of register configuration constraints to adhere to when programming the H3A. It can be used as a quick checklist. More detailed register setting constraints can be found in the individual register descriptions.

- The output addresses (H3A_AFBUFST[31:5] AFBUFST and) must be on 64-byte boundaries.
- Each horizontal row of paxels () or windows () starts on a 32-byte boundary.
- If the pixel clock frequency ISP_FCLK/2 and vertical focus is enabled, the constraints listed in Table 8-387 apply.

Table 8-387. ISS ISP H3A Constraints When PCLK ISP_FCLK/2 and Vertical Focus Enabled

Field	Constraint
H3A_AEWWIN1[20:13] WINW	7
H3A_AFPAX1[23:16] PAXW	7
H3A_AFIIRSH[11:0] IIRSH	None
H3A_AFPAXSTART[27:16] PAXSH	= H3A_AFIIRSH[11:0] IIRSH + 2
H3A_AFPAX2[20:17] AFINCH	None
H3A_AFPAX2[5:0] PAXHC	=11

- If the pixel clock frequency ISP_FCLK/2 and vertical focus is disabled, the constraints listed in Table 8-388 apply.

Table 8-388. ISS ISP H3A Constraints When PCLK ISP_FCLK/2 and Vertical Focus Disabled

Field	Constraint
H3A_AEWWIN1[20:13] WINW	7
H3A_AFPAX1[23:16] PAXW	7
H3A_AFIIRSH[11:0] IIRSH	Must be even
H3A_AFPAXSTART[27:16] PAXSH	= H3A_AFIIRSH[11:0] IIRSH + 2 and must be even
H3A_AFPAX2[20:17] AFINCH	(1+ H3A_AFPAX1[23:16] PAXW / H3A_AFPAX2[20:17] AFINCH) * H3A_AFPAX2[5:0] PAXHC must be between 4 and 384
H3A_AFPAX2[5:0] PAXHC	=35

- If the pixel clock frequency = ISP_FCLK/2 and vertical focus is enabled, the constraints listed in Table 8-389 apply.

Table 8-389. ISS ISP H3A Constraints When PCLK = ISP_FCLK/2 and Vertical Focus Enabled

Field	Constraint
H3A_AEWWIN1[20:13] WINW	15
H3A_AFPAX1[23:16] PAXW	15
H3A_AFIIRSH[11:0] IIRSH	None
H3A_AFPAXSTART[27:16] PAXSH	= H3A_AFIIRSH[11:0] IIRSH + 2
H3A_AFPAX2[20:17] AFINCH	None
H3A_AFPAX2[5:0] PAXHC	=11

- If the pixel clock frequency = ISP_FCLK/2 and vertical focus is disabled, the constraints in Table 8-390 apply.

Table 8-390. ISS ISP H3A Constraints When PCLK = ISP_FCLK/2 and Vertical Focus Disabled

Field	Constraint
H3A_AEWWIN1[20:13] WINW	15
H3A_AFPAX1[23:16] PAXW	15
H3A_AFIIRSH[11:0] IIRSH	Must be even
H3A_AFPAXSTART[27:16] PAXSH	= H3A_AFIIRSH[11:0] IIRSH + 2 and must be even

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Table 8-390. ISS ISP H3A Constraints When PCLK = ISP_FCLK/2 and Vertical Focus Disabled (continued)

Field	Constraint
H3A_AFPAX2[20:17] AFINCH	(1+ H3A_AFPAX1[23:16] PAXW / H3A_AFPAX2[20:17] AFINCH) * H3A_AFPAX2[5:0] PAXHC must be between 4 and 384 and H3A_AFPAX2[20:17] AFINCH modulo H3A_AFPAX1[23:16] PAXW !=1
H3A_AFPAX2[5:0] PAXHC	=35

AF engine

- The paxel horizontal start value must be greater than or equal to the IIR horizontal start position.
- The paxel start/end and IIR filter start positions must not be set within the first 2 and the last 2 pixels (to check).
- The width (H3A_AFPAX1[23:16] PAXW) and height (H3A_AFPAX1[7:0] PAXH) of the paxels must be an even number.
- The minimum width of the paxel (H3A_AFPAX1[23:16] PAXW) must be 8 pixels.
- The number of columns to increment in a paxel (H3A_AFPAX2[20:17] AFINCH) must be even and is restricted to 2 to 32.
- The number of lines to increment in a paxel (H3A_AFPAX2[16:13] AFINCV) must be even and is restricted to 0 to 30.
- The maximum number of vertical paxels in a frame (H3A_AFPAX2[12:6] PAXVC) must not exceed 128.
- The number of paxels in the horizontal direction (H3A_AFPAX2[5:0] PAXHC) has a valid range from 1 to 35.
- If vertical mode is enabled:
  - The paxel horizontal start position (H3A_AFPAXSTART[27:16] PAXSH) must be even.
  - The lower bit of the H3A_AFPAXSTART[27:16] PAXSH bit field and the lower bit of the H3A_AFIIRSH[11:0 IIRSH] bit field must be equal.
  - The H3A_AFPAXSTART[11:0] PAXSV bit field must be = 8.
- If vertical mode is not enabled, the H3A_AFIIRSH[11:0] IIRSH bit field must be even.
- Paxels cannot overlap the last pixel in a line.
- Paxels must be adjacent to one another.

AEW engine

- The width (H3A_AEWWIN1[20:13] WINW) and height (H3A_AEWWIN1[31:24] WINH) of the windows must be an even number.
- The minimum width of the window (H3A_AEWWIN1[20:13] WINW) must be 8 pixels.
- The window height (H3A_AEWWIN1[31:24] WINH) has a valid range from 2 to 512.
- The maximum number of vertical windows in a frame (H3A_AEWWIN1[12:6] WINVC) must not exceed 128.
- The number of horizontal windows (H3A_AEWWIN1[5:0] WINHC) has a valid range from 1 to 35.
- The vertical and horizontal window start position (H3A_AEWWINSTART) has a valid range from 0 to 4095.
- The vertical window start position for single black lines (H3A_AEWINBLK[27:16] WINSV) has a valid range from 0 to 4095.
- The horizontal window start position for single black lines (H3A_AEWINBLK[6:0] WINH) must be even and has a valid range from 2 to 256
- The subsampling windows can start only on even numbers.
- The vertical and horizontal sampling point increment (H3A_AEWSUBWIN) has a valid range from 2 to 32.

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8.3.4.7 ISS ISP BL Programming Model

The procedure listed in Table 8-391 initializes the buffer logic.

Table 8-391. ISS ISP BL Settings

Step	Register/Bit Field/Programming Model	Value
Sets the memory access priority registers	ISP5_MPSR	
Sets the minimum interval between two memory requests for ISIF read port	ISP5_BL_MTC_1[31:16] ISIF_R	
Sets the minimum interval between two memory requests for IPIPEIF read port	ISP5_BL_MTC_1[15:0] IPIPEIF_R	
Sets the minimum interval between two memory requests for H3A write port	ISP5_BL_MTC_1[31:16] H3A_W	
Set the maximum number of CIDs/tags that the BL can use.	ISP5_CTRL[7:4] VBUSM_CIDS	
Set the BL VBUSM priority setting.	ISP5_CTRL[3:1] VBUSM_CPRIORITY	
Set write posted/nonposted.	ISP5_CTRL[0] OCP_WRNP	
Enable the BL clock.	ISP5_CTRL[15] BL_CLK_ENABLE	0x1

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8.3.5 ISS ISP Register Manual

8.3.5.1 ISS ISP Instance Summary

Table 8-392. ISS ISP Instance Summary

Module Name	Module Base Address	Size
ISS_ISP5_SYS1	0x5201 0000	160 bytes
ISS_ISP5_SYS2	0x5201 00A0	864 bytes
ISS_RESIZER	0x5201 0400	1KB
ISS_IPIPE	0x5201 0800	2KB
ISS_ISIF	0x5201 1000	512 bytes
ISS_IPIPEIF	0x5201 1200	128 bytes
ISS_H3A	0x5201 1400	512 bytes

8.3.5.2 ISS ISP5 SYS1 Registers

8.3.5.2.1 ISS ISP5 SYS1 Register Summary

Table 8-393. ISS ISP5 SYS1 Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	ISS_ISP5_SYS1 Base Address
ISP5_REVISION	R	32	0x0000 0000	0x5201 0000
ISP5_HWINFO1	R	32	0x0000 0004	0x5201 0004
ISP5_HWINFO2	R	32	0x0000 0008	0x5201 0008
ISP5_SYSCONFIG	RW	32	0x0000 0010	0x5201 0010
RESERVED	RW	32	0x0000 0020	0x5201 0020
ISP5_IRQSTATUS_RAW_i (1)	RW	32	0x0000 0024 + (0x10 * i)	0x5201 0024 + (0x10 * i)
ISP5_IRQSTATUS_i (1)	RW	32	0x0000 0028 + (0x10 * i)	0x5201 0028 + (0x10 * i)
ISP5_IRQENABLE_SET_i (1)	RW	32	0x0000 002C + (0x10 * i)	0x5201 002C + (0x10 * i)
ISP5_IRQENABLE_CLR_i (1)	RW	32	0x0000 0030 + (0x10 * i)	0x5201 0030 + (0x10 * i)
ISP5_DMAENABLE_SET	RW	32	0x0000 0064	0x5201 0064
ISP5_DMAENABLE_CLR	RW	32	0x0000 0068	0x5201 0068
ISP5_CTRL	RW	32	0x0000 006C	0x5201 006C
ISP5_PG	RW	32	0x0000 0070	0x5201 0070
ISP5_PG_PULSE_CTRL	RW	32	0x0000 0074	0x5201 0074
ISP5_PG_FRAME_SIZE	RW	32	0x0000 0078	0x5201 0078
ISP5_MPSR	RW	32	0x0000 007C	0x5201 007C
ISP5_BL_MTC_1	RW	32	0x0000 0080	0x5201 0080
ISP5_BL_MTC_2	RW	32	0x0000 0084	0x5201 0084
ISP5_BL_VBUSM	RW	32	0x0000 0088	0x5201 0088

(1) i = 0 to 3

8.3.5.2.2 ISS ISP5 SYS1 Register Description

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Table 8-394. ISP5_REVISION

Address Offset	0x0000 0000		
Physical Address	0x5201 0000	**Instance**	ISS_ISP5_SYS1
Description	IP Revision Identifier (X.Y.R) Used by software to track features, bugs, and compatibility		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP Revision	R	See(1)

(1) TI internal data

Table 8-395. Register Call Summary for Register ISP5_REVISION

ISS ISP

- ISS ISP5 SYS1 Register Summary: [0]

Table 8-396. ISP5_HWINFO1

Address Offset	0x0000 0004		
Physical Address	0x5201 0004	**Instance**	ISS_ISP5_SYS1
Description	GENERIC PARAMETER REGISTER Information about the hardware configuration of the IP module.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			ISIF_RFM_LINE_SIZE													RESERVED			IPIPE_LINE_SIZE												

Bits	Field Name	Description	Type	Reset
31:29	RESERVED		R	0x0
28:16	ISIF_RFM_LINE_SIZE	Memory line size for the data reformatter in the ISIF module.	R	0x1500
15:13	RESERVED		R	0x0
12:0	IPIPE_LINE_SIZE	Memory line size for the IPIPE module	R	0x1500

Table 8-397. Register Call Summary for Register ISP5_HWINFO1

ISS ISP

- ISS ISP5 SYS1 Register Summary: [0]

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Table 8-398. ISP5_HWINFO2

Address Offset	0x0000 0008		
Physical Address	0x5201 0008	**Instance**	ISS_ISP5_SYS1
Description	GENERIC PARAMETER REGISTER Information about the hardware configuration of the IP module.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								H3A_LINE_SIZE							

Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000
12:0	H3A_LINE_SIZE	Memory line size for the H3A module	R	0x0BC0

Table 8-399. Register Call Summary for Register ISP5_HWINFO2

ISS ISP

- ISS ISP5 SYS1 Register Summary: [0]

Table 8-400. ISP5_SYSCONFIG

Address Offset	0x0000 0010		
Physical Address	0x5201 0010	**Instance**	ISS_ISP5_SYS1
Description	Clock management configuration		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																										STANDBYMODE		RESERVED		SOFTRESET	AUTO_IDLE

Bits	Field Name	Description	Type	Reset
31:6	RESERVED		R	0x0000000
5:4	STANDBYMODE	Configuration of the local initiator state management mode. By definition, initiator may generate read/write transaction as long as it is out of STANDBY state. 0x0: Force-standby mode: local initiator is unconditionally placed in standby state. Backup mode, for debug only. 0x1: No-standby mode: local initiator is unconditionally placed out of standby state. Backup mode, for debug only. 0x3: Reserved 0x2: Smart-standby mode: local initiator standby status depends on local conditions, that is, the module's functional requirement from the initiator. IP module must not generate (initiator-related) wake-up events. Generation of the MStandby signal must be initiated by the firmware by writing ISP5_CTRL.MSTANDBY = 1.	RW	0x2
3:2	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
1	SOFTRESET	Software reset. The soft reset will cause the MStandby to be asserted as the reset value of the ISP5_CTRL.MSTANDBY bit is 1. After a soft reset, the software must ensure not to perform any access for 16 clock cycles (OCP-slave port frequency) after writing this bit. The OCP slave port is running at half the frequency of the functional clock. Before issuing a soft reset, the software must ensure that no more traffic is being generated by the ISP. Basically, it means that the camera module must be stopped from sending data and/or that the ISP modules are disabled. The last interrupt triggered by the ISP design upon completion of the frame processing is rsz_int_dma. This rsz_int_dma event must be used to enable clean termination of the processing. The software must wait a few hundred cycles to trigger the soft reset after upon assertion of the rsz_int_dma, this is to ensure that the BL is completely drained. Software must set the ISP in standby mode before issuing the soft reset: Set ISP5_SYSCONFIG.STANDBYMODE = 2 (smart standby). Set ISP5_CTRL.MSTANDBY to 1. Poll for ISP5_CTRL.MSTANDBY_WAIT = 1. Then, the soft reset can be applied (ISP5_SYSCONFIG.SOFTRESET = 1). Write 0x0: No action Write 0x1: Initiate software reset Read 0x1: Reset (software or other) ongoing Read 0x0: Reset done, no pending action	RW	0
0	AUTO_IDLE	Auto clock gating. Always enabled.	R	1

Table 8-401. Register Call Summary for Register ISP5_SYSCONFIG

ISS ISP

- ISS ISP Reset: [0] [1] [2]
- ISS ISP IPIPEIF Hardware Setup/Initialization: [3]
- ISS ISP RSZ Hardware Setup/Initialization: [4] [5] [6]
- ISS ISP5 SYS1 Register Summary: [7]
- ISS ISP5 SYS1 Register Description: [8] [9]

Table 8-402. ISP5_IRQSTATUS_RAW_i

Address Offset	0x0000 0024 + (0x10 * i)	**Index**	i = 0 to 3
Physical Address	0x5201 0024 + (0x10 * i)	**Instance**	ISS_ISP5_SYS1
Description	Per-event raw interrupt status vector. Raw status is set even if event is not enabled. Write 1 to set the (raw) status, mostly for debug. The ISP outputs four interrupt lines, ISP_IRQ0 to ISP_IRQ3. Any internal ISP event can be merged on the four lines. A same event must be enabled on only one interrupt line.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OCP_ERR_IRQ	RESERVED	IPIPE_INT_DPC_RNEW1	IPIPE_INT_DPC_RNEW0	IPIPE_INT_DPC_INI	RESERVED	IPIPE_INT_EOF	H3A_INT_EOF	RSZ_INT_EOF1	RSZ_INT_EOF0	RESERVED		RSZ_FIFO_IN_BLK_ERR	RSZ_FIFO_OVF	RSZ_INT_CYC_RZB	RSZ_INT_CYC_RZA	RSZ_INT_DMA	RSZ_INT_LAST_PIX	RSZ_INT_REG	H3A_INT	AF_INT	AEW_INT	IPIPEIF_IRQ	IPIPE_INT_HST	IPIPE_INT_BSC	IPIPE_INT_DMA	IPIPE_INT_LAST_PIX	IPIPE_INT_REG	ISIF_INT_3	ISIF_INT_2	ISIF_INT_1	ISIF_INT_0

Bits	Field Name	Description	Type	Reset
31	OCP_ERR_IRQ	An OCP error has been received on the ISP master port. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
30	RESERVED		R	0
29	IPIPE_INT_DPC_RNEW1	Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
28	IPIPE_INT_DPC_RNEW0	Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
27	IPIPE_INT_DPC_INI	Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
26	RESERVED		R	0
25	IPIPE_INT_EOF	Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
24	H3A_INT_EOF	Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
23	RSZ_INT_EOF1	RESIZER module event: This event signals that the BL has received the EOF signal from the resizer B engine which happens one the last transfer in the frame has happened. Note that because the BL has FIFOs it may take some additional time before true data transfer completion to memory. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0

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Bits	Field Name	Description	Type	Reset
22	RSZ_INT_EOF0	RESIZER module event: This event signals that the BL has received the EOF signal from the resizer A engine which happens one the last transfer in the frame has happened. Note that because the BL has FIFOs it may take some additional time before true data transfer completion to memory. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
21:20	RESERVED		R	0x0
19	RSZ_FIFO_IN_BLK_ERR	This event signals that the minimum vertical blanking period has not been respected causing errors in the input data buffering submodule. This event will be triggered when the rsz_int_reg event of frame N is triggered before the rsz_int_dma of frame N + 1. This event would typically happen at the transition between two frames because there is not enough vertical blanking between frames: the firmware must take care to ensure enough vertical blanking. The hardware cannot recover from this error. It will be required to perform a reset of the IP. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
18	RSZ_FIFO_OVF	This event signals that overflow happened in the input data buffering submodule. This event would typically happen while processing a frame because the video port pixel clock is too high: the firmware must take care to use a lower pixel clock at the input of the resizer module. Depending on the mode being used, the overflow can happen at different places: 1. Bypass mode: overflow happened in the input circular buffer. 2. Pass through mode: overflow happened on the module output interface (MTC) 3. Normal resize mode: overflow happened in the input circular buffer. The hardware cannot recover from this error. It will be required to perform a reset of the IP. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0

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Bits	Field Name	Description	Type	Reset
17	RSZ_INT_CYC_RZB	RESIZER module event: This event is the circular interrupt for RESIZER #B. An event can be triggered every time that RSZ_IRQ_RZB output lines have been written out to the RZB_SDR_Y buffer. The range can go from 1 to 8192 lines. Usually, this value should be such that the circular buffer vertical size (set by the RZB_SDR_Y_PTR_E register) is a multiple of RSZ_IRQ_RZB. Note that at the time the interrupt is triggered, the actual data write has not taken place. It may take a few hundred of cycles to complete the data write into system memory. This is not an issue since the start of the buffer is read first. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
16	RSZ_INT_CYC_RZA	RESIZER module event: This event is the circular interrupt for RESIZER #A. An event can be triggered every time that RSZ_IRQ_RZA output lines have been written out to the RZA_SDR_Y buffer. The range can go from 1 to 8192 lines. Usually, the circular buffer vertical size (set by the RZA_SDR_Y_PTR_E register) should be a multiple of RSZ_IRQ_RZA. Note that at the time the interrupt is triggered, the actual data write has not taken place. It may take a few hundred of cycles to complete the data write into system memory. This is not an issue since the start of the buffer is read first. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
15	RSZ_INT_DMA	This event is triggered when the last EOF (of the two MTC interfaces) is sent out to the BL and that the resizer core has returned to idle. rsz_int_dma is a true indication that all processing is finished for the particular frame on both resizer engines. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
14	RSZ_INT_LAST_PIX	This event is triggered when the last pixel of the valid area is received. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
13	RSZ_INT_REG	This event is triggered when the first pixel of the valid area is received. Shadowed registers can be updated at any time but the new value will take effect on the next rsz_int_reg event. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0

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Bits	Field Name	Description	Type	Reset
12	H3A_INT	Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
11	AF_INT	Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
10	AEW_INT	Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
9	IPIPEIF_IRQ	IPIPEIF module interrupt Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
8	IPIPE_INT_HST	Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
7	IPIPE_INT_BSC	Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
6	IPIPE_INT_DMA	Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
5	IPIPE_INT_LAST_PIX	Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
4	IPIPE_INT_REG	Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
3	ISIF_INT_3	Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
2	ISIF_INT_2	Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0

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Bits	Field Name	Description	Type	Reset
1	ISIF_INT_1	Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
0	ISIF_INT_0	Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0

Table 8-403. Register Call Summary for Register ISP5_IRQSTATUS_RAW_i

ISS ISP
- ISS ISP5 SYS1 Register Summary: [0]

Table 8-404. ISP5_IRQSTATUS_i

Address Offset	0x0000 0028 + (0x10 * i)	**Index**	i = 0 to 3
Physical Address	0x5201 0028 + (0x10 * i)	**Instance**	ISS_ISP5_SYS1
Description	Per-event "enabled" interrupt status vector. Enabled status is not set unless event is enabled. Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, that is, even if not enabled). The ISP outputs four interrupt lines, ISP_IRQ0 to ISP_IRQ3. Any internal ISP event can be merged on the four lines. A same event must be enabled on only one interrupt line.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OCP_ERR_IRQ	RESERVED	IPIPE_INT_DPC_RNEW1	IPIPE_INT_DPC_RNEW0	IPIPE_INT_DPC_INI	RESERVED	IPIPE_INT_EOF	H3A_INT_EOF	RSZ_INT_EOF1	RSZ_INT_EOF0	RESERVED		RSZ_FIFO_IN_BLK_ERR	RSZ_FIFO_OVF	RSZ_INT_CYC_RZB	RSZ_INT_CYC_RZA	RSZ_INT_DMA	RSZ_INT_LAST_PIX	RSZ_INT_REG	H3A_INT	AF_INT	AEW_INT	IPIPEIF_IRQ	IPIPE_INT_HST	IPIPE_INT_BSC	IPIPE_INT_DMA	IPIPE_INT_LAST_PIX	IPIPE_INT_REG	ISIF_INT_3	ISIF_INT_2	ISIF_INT_1	ISIF_INT_0

Bits	Field Name	Description	Type	Reset
31	OCP_ERR_IRQ	An OCP error has been received on the ISP master port. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
30	RESERVED		R	0
29	IPIPE_INT_DPC_RNEW1	Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
28	IPIPE_INT_DPC_RNEW0	Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
27	IPIPE_INT_DPC_INI	Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
26	RESERVED		R	0
25	IPIPE_INT_EOF	Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
24	H3A_INT_EOF	Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
23	RSZ_INT_EOF1	RESIZER module event: This event signals that the BL has received the EOF signal from the resizer B engine which happens one the last transfer in the frame has happened. Note that because the BL has FIFOs it may take some additional time before true data transfer completion to memory. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
22	RSZ_INT_EOF0	RESIZER module event: This event signals that the BL has received the EOF signal from the resizer A engine which happens one the last transfer in the frame has happened. Note that because the BL has FIFOs it may take some additional time before true data transfer completion to memory. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
21:20	RESERVED		R	0x0
19	RSZ_FIFO_IN_BLK_ERR	This event signals that the minimum vertical blanking period has not been respected causing errors in the input data buffering submodule. This event will be triggered when the rsz_int_reg event of frame N is triggered before the rsz_int_dma of frame N + 1. This event would typically happen at the transition between two frames because there is not enough vertical blanking between frames: the firmware must take care to ensure enough vertical blanking. The hardware cannot recover from this error. It will be required to perform a reset of the IP. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
18	RSZ_FIFO_OVF	This event signals that overflow happened in the input data buffering submodule or in the RSZ output interface. This event would typically happen while processing a frame because the video port pixel clock is too high: the firmware must take care to use a lower pixel clock at the input of the resizer module. The hardware cannot recover from this error. It will be required to perform a reset of the IP. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
17	RSZ_INT_CYC_RZB	RESIZER module event: This event is the circular interrupt for RESIZER #B. An event can be triggered every time that RSZ_IRQ_RZB output lines have been written out to the RZB_SDR_Y buffer. The range can go from 1 to 8192 lines. Usually, this value should be such that the circular buffer vertical size (set by the RZB_SDR_Y_PTR_E register) is a multiple of RSZ_IRQ_RZB. Note that at the time the interrupt is triggered, the actual data write has not taken place. It may take a few hundred of cycles to complete the data write into system memory. This is not an issue since the start of the buffer is read first. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
16	RSZ_INT_CYC_RZA	RESIZER module event: This event is the circular interrupt for RESIZER #A. An event can be triggered every time that RSZ_IRQ_RZA output lines have been written out to the RZA_SDR_Y buffer. The range can go from 1 to 8192 lines. Usually, the circular buffer vertical size (set by the RZA_SDR_Y_PTR_E register) should be a multiple of RSZ_IRQ_RZA. Note that at the time the interrupt is triggered, the actual data write has not taken place. It may take a few hundred of cycles to complete the data write into system memory. This is not an issue since the start of the buffer is read first. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
15	RSZ_INT_DMA	This event is triggered when the last EOF (of the two MTC interfaces) is sent out to the BL and that the resizer core has returned to idle. rsz_int_dma is a true indication that all processing is finished for the particular frame on both resizer engines. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
14	RSZ_INT_LAST_PIX	This event is triggered when the last pixel of the valid area is received. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
13	RSZ_INT_REG	This event is triggered when the first pixel of the valid area is received. Shadowed registers can be updated at any time but the new value will take effect on the next rsz_int_reg event. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
12	H3A_INT	Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
11	AF_INT	Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
10	AEW_INT	Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
9	IPIPEIF_IRQ	IPIPEIF module interrupt Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
8	IPIPE_INT_HST	Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
7	IPIPE_INT_BSC	Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
6	IPIPE_INT_DMA	Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
5	IPIPE_INT_LAST_PIX	Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
4	IPIPE_INT_REG	Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
3	ISIF_INT_3	LSC interrupt issued by 2D-LSC block. Four types of 2D-LSC can be generated and mapped to the INT_3 line. For more information, see Section 8.3.3.7.10.1.5, *ISS ISP ISIF 2D-LSC Events and Status Checking.* Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
2	ISIF_INT_2	VD interrupt 2 event. Read this bit to check the interrupt mapped to the INT_2 line. This interrupt is also set based on the VD pulse position after receiving a configured number of horizontal pulse signals. For more information, see Section 8.3.3.7.19.1, *ISS ISP ISIF VDINT0, VDINT1 and VDINT2 Interrupts.* Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
1	ISIF_INT_1	VD interrupt 1 event. Read this bit to check the interrupt mapped to the INT_1 line. This interrupt is also set based on the VD pulse position after receiving a configured number of horizontal pulse signals. For more information, see Section 8.3.3.7.19.1, *ISS ISP ISIF VDINT0, VDINT1 and VDINT2 Interrupts.* Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
0	ISIF_INT_0	VD interrupt 0 event. Read this bit to check the interrupt mapped to the INT_0 line. This interrupt is also set based on the VD pulse position after receiving a configured number of horizontal pulse signals. For more information, see Section 8.3.3.7.19.1, *ISS ISP ISIF VDINT0, VDINT1 and VDINT2 Interrupts.* Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0

Table 8-405. Register Call Summary for Register ISP5_IRQSTATUS_i

ISS ISP

- ISS ISP RSZ Hardware Setup/Initialization: [0] [1]
- ISS ISP5 SYS1 Register Summary: [2]

NOTE: ISP submodule interrupts are mapped to ISP top-level lines. Moreover, ISP top-level lines are mapped to the ISS top interrupt merger level. For information about how IRQ lines are handled at the ISP level, see Table 8-311. For information about how IRQs are handled at the ISS top-level before the signals leave ISS boundaries, see Section 8.1.2.1.1, *ISS Interrupt Merger.*

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Table 8-406. ISP5_IRQENABLE_SET_i

Address Offset	0x0000 002C + (0x10 * i)	**Index**	i = 0 to 3
Physical Address	0x5201 002C + (0x10 * i)	**Instance**	ISS_ISP5_SYS1
Description	Per-event interrupt enable bit vector. Write 1 to set (enable interrupt). Readout equal to corresponding _CLR register. The ISP outputs four interrupt lines, ISP_IRQ0 to ISP_IRQ3. Any internal ISP event can be merged on the four lines. A same event must be enabled on only one interrupt line.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OCP_ERR_IRQ	RESERVED	IPIPE_INT_DPC_RNEW1	IPIPE_INT_DPC_RNEW0	IPIPE_INT_DPC_INI	RESERVED	IPIPE_INT_EOF	H3A_INT_EOF	RSZ_INT_EOF1	RSZ_INT_EOF0	RESERVED		RSZ_FIFO_IN_BLK_ERR	RSZ_FIFO_OVF	RSZ_INT_CYC_RZB	RSZ_INT_CYC_RZA	RSZ_INT_DMA	RSZ_INT_LAST_PIX	RSZ_INT_REG	H3A_INT	AF_INT	AEW_INT	IPIPEIF_IRQ	IPIPE_INT_HST	IPIPE_INT_BSC	IPIPE_INT_DMA	IPIPE_INT_LAST_PIX	IPIPE_INT_REG	ISIF_INT_3	ISIF_INT_2	ISIF_INT_1	ISIF_INT_0

Bits	Field Name	Description	Type	Reset
31	OCP_ERR_IRQ	An OCP error has been received on the ISP master port. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
30	RESERVED		R	0
29	IPIPE_INT_DPC_RNEW1	Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
28	IPIPE_INT_DPC_RNEW0	Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
27	IPIPE_INT_DPC_INI	Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
26	RESERVED		R	0
25	IPIPE_INT_EOF	Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
24	H3A_INT_EOF	Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0

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Bits	Field Name	Description	Type	Reset
23	RSZ_INT_EOF1	RESIZER module event: This event signals that the BL has received the EOF signal from the resizer B engine which happens one the last transfer in the frame has happened. Note that because the BL has FIFOs it may take some additional time before true data transfer completion to memory. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
22	RSZ_INT_EOF0	RESIZER module event: This event signals that the BL has received the EOF signal from the resizer A engine which happens one the last transfer in the frame has happened. Note that because the BL has FIFOs it may take some additional time before true data transfer completion to memory. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
21:20	RESERVED		R	0x0
19	RSZ_FIFO_IN_BLK_ERR	This event signals that the minimum vertical blanking period has not been respected causing errors in the input data buffering submodule. This event will be triggered when the rsz_int_reg event of frame N is triggered before the rsz_int_dma of frame N + 1. This event would typically happen at the transition between two frames because there is not enough vertical blanking between frames: the firmware must take care to ensure enough vertical blanking. The hardware cannot recover from this error. It will be required to perform a reset of the IP. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
18	RSZ_FIFO_OVF	This event signals that overflow happened in the input data buffering submodule or in the RSZ output interface. This event would typically happen while processing a frame because the video port pixel clock is too high: the firmware must take care to use a lower pixel clock at the input of the resizer module. The hardware cannot recover from this error. It will be required to perform a reset of the IP. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0

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Bits	Field Name	Description	Type	Reset
17	RSZ_INT_CYC_RZB	RESIZER module event: This event is the circular interrupt for RESIZER #B. An event can be triggered every time that RSZ_IRQ_RZB output lines have been written out to the RZB_SDR_Y buffer. The range can go from 1 to 8192 lines. Usually, this value should be such that the circular buffer vertical size (set by the RZB_SDR_Y_PTR_E register) is a multiple of RSZ_IRQ_RZB. Note that at the time the interrupt is triggered, the actual data write has not taken place. It may take a few hundred of cycles to complete the data write into system memory. This is not an issue since the start of the buffer is read first. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
16	RSZ_INT_CYC_RZA	RESIZER module event: This event is the circular interrupt for RESIZER #A. An event can be triggered every time that RSZ_IRQ_RZA output lines have been written out to the RZA_SDR_Y buffer. The range can go from 1 to 8192 lines. Usually, the circular buffer vertical size (set by the RZA_SDR_Y_PTR_E register) should be a multiple of RSZ_IRQ_RZA. Note that at the time the interrupt is triggered, the actual data write has not taken place. It may take a few hundred of cycles to complete the data write into system memory. This is not an issue since the start of the buffer is read first. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
15	RSZ_INT_DMA	This event is triggered when the last EOF (of the two MTC interfaces) is sent out to the BL and that the resizer core has returned to idle. rsz_int_dma is a true indication that all processing is finished for the particular frame on both resizer engines. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
14	RSZ_INT_LAST_PIX	This event is triggered when the last pixel of the valid area is received. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
13	RSZ_INT_REG	This event is triggered when the first pixel of the valid area is received. Shadowed registers can be updated at any time but the new value will take effect on the next rsz_int_reg event. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0

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Bits	Field Name	Description	Type	Reset
12	H3A_INT	Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
11	AF_INT	Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
10	AEW_INT	Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
9	IPIPEIF_IRQ	IPIPEIF module interrupt Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
8	IPIPE_INT_HST	Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
7	IPIPE_INT_BSC	Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
6	IPIPE_INT_DMA	Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
5	IPIPE_INT_LAST_PIX	Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
4	IPIPE_INT_REG	Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
3	ISIF_INT_3	LSC interrupt issued by the 2D-LSC block. Four types of 2D-LSC can be generated and mapped to the INT_3 line. For more information, see Section 8.3.3.7.10.1.5, *ISS ISP ISIF 2D-LSC Events and Status Checking.* Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0

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Bits	Field Name	Description	Type	Reset
2	ISIF_INT_2	VD interrupt 2 event. Set this bit to enable the interrupt and map it to the INT_2 line. This interrupt is set based on the VD pulse position after receiving a configured number of horizontal pulse signals. For more information, see Section 8.3.3.7.19.1, *ISS ISP ISIF VDINT0, VDINT1 and VDINT2 Interrupts.* Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
1	ISIF_INT_1	VD interrupt 1 event. Set this bit to enable the interrupt and map it to the INT_1 line. This interrupt is set based on the VD pulse position after receiving a configured number of horizontal pulse signals. For more information, see Section 8.3.3.7.19.1, *ISS ISP ISIF VDINT0, VDINT1 and VDINT2 Interrupts.* Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
0	ISIF_INT_0	VD interrupt 0 event. Set this bit to enable the interrupt mapped to INT_0 line. This interrupt is set based on the VD pulse position after receiving a configured number of horizontal pulse signals. For more information, see Section 8.3.3.7.19.1, *ISS ISP ISIF VDINT0, VDINT1 and VDINT2 Interrupts.* Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0

Table 8-407. Register Call Summary for Register ISP5_IRQENABLE_SET_i

ISS ISP

- ISS ISP Interrupt Tree: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23] [24]
- ISS ISP IPIPEIF Interrupts: [25]
- ISS ISP IPIPE Interrupts: [26]
- ISS ISP RSZ Interrupts: [27]
- ISS ISP H3A Interrupts: [28]
- ISS ISP ISIF Interrupts: [29]
- ISS ISP IPIPEIF Module Events and Status Checking: [30]
- ISS ISP5 SYS1 Register Summary: [31]

NOTE: Setting the ISP submodule interrupts and mapping them to the ISP lines requires a configuration to receive the IRQ events at a higher ISS interrupt merger level. For information about how IRQ lines are handled at the ISP level, see Table 8-311. For information about how IRQs are handled at the ISS top-level before the signals leave ISS boundaries, see Section 8.1.2.1.1, *ISS Interrupt Merger.*

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Table 8-408. ISP5_IRQENABLE_CLR_i

Address Offset	0x0000 0030 + (0x10 * i)	**Index**	i = 0 to 3
Physical Address	0x5201 0030 + (0x10 * i)	**Instance**	ISS_ISP5_SYS1
Description	Per-event interrupt enable bit vector. Write 1 to clear (disable interrupt). Readout equal to corresponding _SET register. The ISP outputs four interrupt lines, ISP_IRQ0 to ISP_IRQ3. Any internal ISP event can be merged on the four lines. A same event must be enabled on only one interrupt line.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OCP_ERR_IRQ	RESERVED	IPIPE_INT_DPC_RNEW1	IPIPE_INT_DPC_RNEW0	IPIPE_INT_DPC_INI	RESERVED	IPIPE_INT_EOF	H3A_INT_EOF	RSZ_INT_EOF1	RSZ_INT_EOF0	RESERVED		RSZ_FIFO_IN_BLK_ERR	RSZ_FIFO_OVF	RSZ_INT_CYC_RZB	RSZ_INT_CYC_RZA	RSZ_INT_DMA	RSZ_INT_LAST_PIX	RSZ_INT_REG	H3A_INT	AF_INT	AEW_INT	IPIPEIF_IRQ	IPIPE_INT_HST	IPIPE_INT_BSC	IPIPE_INT_DMA	IPIPE_INT_LAST_PIX	IPIPE_INT_REG	ISIF_INT_3	ISIF_INT_2	ISIF_INT_1	ISIF_INT_0

Bits	Field Name	Description	Type	Reset
31	OCP_ERR_IRQ	An OCP error has been received on the ISP master port. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
30	RESERVED		R	0
29	IPIPE_INT_DPC_RNEW1	Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
28	IPIPE_INT_DPC_RNEW0	Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
27	IPIPE_INT_DPC_INI	Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
26	RESERVED		R	0
25	IPIPE_INT_EOF	Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW	0
24	H3A_INT_EOF	Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW	0

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Bits	Field Name	Description	Type	Reset
23	RSZ_INT_EOF1	RESIZER module event: This event signals that the BL has received the EOF signal from the resizer B engine which happens one the last transfer in the frame has happened. Note that because the BL has FIFOs it may take some additional time before true data transfer completion to memory. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW	0
22	RSZ_INT_EOF0	RESIZER module event: This event signals that the BL has received the EOF signal from the resizer A engine which happens one the last transfer in the frame has happened. Note that because the BL has FIFOs it may take some additional time before true data transfer completion to memory. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW	0
21:20	RESERVED		R	0x0
19	RSZ_FIFO_IN_BLK_ERR	This event signals that the minimum vertical blanking period has not been respected causing errors in the input data buffering submodule. This event will be triggered when the rsz_int_reg event of frame N is triggered before the rsz_int_dma of frame N + 1. This event would typically happen at the transition between two frames because there is not enough vertical blanking between frames: the firmware must take care to ensure enough vertical blanking. The hardware cannot recover from this error. It will be required to perform a reset of the IP. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
18	RSZ_FIFO_OVF	RESIZER module event: This event signals that overflow happened in the input data buffering submodule or in the RSZ output interface.. This event would typically happen because the video port pixel clock is too high. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
17	RSZ_INT_CYC_RZB	RESIZER module event: This event is the circular interrupt for RESIZER #B. An event can be triggered every time that RSZ_IRQ_RZB output lines have been written out to the RZB_SDR_Y buffer. The range can go from 1 to 8192 lines. Usually, this value should be such that the circular buffer vertical size (set by the RZB_SDR_Y_PTR_E register) is a multiple of RSZ_IRQ_RZB. Note that at the time the interrupt is triggered, the actual data write has not taken place. It may take a few hundred of cycles to complete the data write into system memory. This is not an issue since the start of the buffer is read first. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
16	RSZ_INT_CYC_RZA	RESIZER module event: This event is the circular interrupt for RESIZER #A. An event can be triggered every time that RSZ_IRQ_RZA output lines have been written out to the RZA_SDR_Y buffer. The range can go from 1 to 8192 lines. Usually, the circular buffer vertical size (set by the RZA_SDR_Y_PTR_E register) should be a multiple of RSZ_IRQ_RZA. Note that at the time the interrupt is triggered, the actual data write has not taken place. It may take a few hundred of cycles to complete the data write into system memory. This is not an issue since the start of the buffer is read first. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
15	RSZ_INT_DMA	RESIZER module event: This event is triggered when the last EOF (of the two MTC interfaces) is sent out to the BL and that the resizer core has returned to idle. rsz_int_dma is a true indication that all processing is finished for the particular frame on both resizer engines. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
14	RSZ_INT_LAST_PIX	RESIZER module event: This event is triggered when the last pixel of the valid area is received. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
13	RSZ_INT_REG	RESIZER module event: This event is triggered when the first pixel of the valid area is received. Shadowed registers can be updated at any time but the new value will take effect on the next rsz_int_reg event. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
12	H3A_INT	Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
11	AF_INT	Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
10	AEW_INT	Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
9	IPIPEIF_IRQ	IPIPEIF module interrupt Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
8	IPIPE_INT_HST	Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
7	IPIPE_INT_BSC	Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
6	IPIPE_INT_DMA	Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
5	IPIPE_INT_LAST_PIX	Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
4	IPIPE_INT_REG	Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
3	ISIF_INT_3	Set this bit to disable the LSC interrupt issued by the 2D-LSC block. Four types of 2D-LSC can be generated and mapped to the INT_3 line. For more information, see Section 8.3.3.7.10.1.5, *ISS ISP ISIF 2D-LSC Events and Status Checking.* Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
2	ISIF_INT_2	VD interrupt 2 event. Set this bit to disable the interrupt mapped to the INT_2 line. This interrupt is set based on the VD pulse position after receiving a configured number of horizontal pulse signals. For more information, see Section 8.3.3.7.19.1, *ISS ISP ISIF VDINT0, VDINT1 and VDINT2 Interrupts.* Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
1	ISIF_INT_1	VD interrupt 1 event. Set this bit to disable the interrupt mapped to the INT_1 line. This interrupt is set based on the VD pulse position after receiving a configured number of horizontal pulse signals. For more information, see Section 8.3.3.7.19.1, *ISS ISP ISIF VDINT0, VDINT1 and VDINT2 Interrupts.* Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
0	ISIF_INT_0	VD interrupt 0 event. Set this bit to disable the interrupt mapped to the INT_0 line. This interrupt is set based on the VD pulse position after receiving a configured number of horizontal pulse signals. For more information, see Section 8.3.3.7.19.1, *ISS ISP ISIF VDINT0, VDINT1 and VDINT2 Interrupts.* Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0

Table 8-409. Register Call Summary for Register ISP5_IRQENABLE_CLR_i

ISS ISP

- ISS ISP RSZ Hardware Setup/Initialization: [0]
- ISS ISP5 SYS1 Register Summary: [1]

NOTE: Setting or disabling the ISP submodule interrupts mapped to the ISP lines requires a configuration to receive or disable the IRQ events at a higher ISS interrupt merger level. For information about how IRQ lines are handled at the ISP level, see Table 8-311. For information about how IRQs are handled at the ISS top-level before the signals leave ISS boundaries, see Section 8.1.2.1.1, *ISS Interrupt Merger.*

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Table 8-410. ISP5_DMAENABLE_SET

Address Offset	0x0000 0064		
Physical Address	0x5201 0064	**Instance**	ISS_ISP5_SYS1
Description	Per-line DMA enable bit vector Write 1 to set (enable DMA request generation). Readout equal to corresponding _CLR register.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																											IPIPE_INT_DPC_RNEW1	IPIPE_INT_LAST_PIX	IPIPE_INT_DPC_RNEW0	IPIPE_INT_HST	IPIPE_INT_BSC	

Bits	Field Name	Description	Type	Reset
31:5	RESERVED		R	0x0000000
4	IPIPE_INT_DPC_RNEW1	Enable for ISP DMA request generation on line #2 This DMA request must be set to transfer the DPC data from memory to the IPIPE internal RAM. Write 0x0: No action Write 0x1: Enable DMA Read 0x1: DMA enabled Read 0x0: DMA disabled	RW W1toSet	0
3	IPIPE_INT_LAST_PIX	Enable for ISP DMA request generation on line #3 This DMA request must be set to transfer the GAMMA data from memory to the IPIPE internal RAM or to initialize the DPC table. One must set the ISP5_CTRL.DMA3_CFG register before enabling this DMA request. Write 0x0: No action Write 0x1: Enable DMA Read 0x1: DMA enabled Read 0x0: DMA disabled	RW W1toSet	0
2	IPIPE_INT_DPC_RNEW0	Enable for ISP DMA request generation on line #2 This DMA request must be set to transfer the DPC data from memory to the IPIPE internal RAM. Write 0x0: No action Write 0x1: Enable DMA Read 0x1: DMA enabled Read 0x0: DMA disabled	RW W1toSet	0
1	IPIPE_INT_HST	Enable for ISP DMA request generation on line #1 This DMA request must be set to transfer the HIST data from the IPIPE internal RAM to memory. Write 0x0: No action Write 0x1: Enable DMA Read 0x1: DMA enabled Read 0x0: DMA disabled	RW W1toSet	0

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Bits	Field Name	Description	Type	Reset
0	IPIPE_INT_BSC	Enable for ISP DMA request generation on line #0 This DMA request must be set to transfer the BSC data from the IPIPE internal RAM to memory. Write 0x0: No action Write 0x1: Enable DMA Read 0x1: DMA enabled Read 0x0: DMA disabled	RW W1toSet	0

Table 8-411. Register Call Summary for Register ISP5_DMAENABLE_SET

ISS ISP

- ISS ISP DMA Requests: [0]
- ISS ISP5 SYS1 Register Summary: [1]

Table 8-412. ISP5_DMAENABLE_CLR

Address Offset	0x0000 0068		
Physical Address	0x5201 0068	**Instance**	ISS_ISP5_SYS1
Description	Per-line DMA clear bit vector Write 1 to clear (disable DMA request generation). Readout equal to corresponding _SET register.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																											IPIPE_INT_DPC_RNEW1	IPIPE_INT_LAST_PIX	IPIPE_INT_DPC_RNEW0	IPIPE_INT_HST	IPIPE_INT_BSC

Bits	Field Name	Description	Type	Reset
31:5	RESERVED		R	0x0000000
4	IPIPE_INT_DPC_RNEW1	Clear for ISP DMA request generation on line ISS_DMA2. This DMA request must be set to transfer the DPC data from memory to the IPIPE internal RAM. Write 0x0: No action Write 0x1: Disable DMA Read 0x1: DMA enabled Read 0x0: DMA disabled	RW W1toClr	0
3	IPIPE_INT_LAST_PIX	Clear for ISP DMA request generation on ISS_DMA3. This DMA request must be set to transfer the GAMMA data from memory to the IPIPE internal RAM. Write 0x0: No action Write 0x1: Disable DMA Read 0x1: DMA enabled Read 0x0: DMA disabled	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
2	IPIPE_INT_DPC_RNEW0	Clear for ISP DMA request generation on ISS_DMA2. This DMA request must be set to transfer the DPC data from memory to the IPIPE internal RAM. Write 0x0: No action Write 0x1: Disable DMA Read 0x1: DMA enabled Read 0x0: DMA disabled	RW W1toClr	0
1	IPIPE_INT_HST	Clear for ISP DMA request generation on ISS_DMA1. This DMA request must be set to transfer the HIST data from the IPIPE internal RAM to memory. Write 0x0: No action Write 0x1: Disable DMA Read 0x1: DMA enabled Read 0x0: DMA disabled	RW W1toClr	0
0	IPIPE_INT_BSC	Clear for ISP DMA request generation on ISS_DMA0. This DMA request must be set to transfer the BSC data from the IPIPE internal RAM to memory. Write 0x0: No action Write 0x1: Disable DMA Read 0x1: DMA enabled Read 0x0: DMA disabled	RW W1toClr	0

Table 8-413. Register Call Summary for Register ISP5_DMAENABLE_CLR

ISS ISP

- ISS ISP DMA Requests: [0]
- ISS ISP5 SYS1 Register Summary: [1]

Table 8-414. ISP5_CTRL

Address Offset	0x0000 006C		
Physical Address	0x5201 006C	**Instance**	ISS_ISP5_SYS1
Description	ISP5 CONTROL REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMA3_CFG		RESERVED		RESERVED	HST_RD_CHK	DPC_EVT_INI	MSTANDBY	VD_PULSE_EXT	PCLK_INV	MFLAG	MSTANDDBY_WAIT	RESERVED				BL_CLK_ENABLE	ISIF_CLK_ENABLE	H3A_CLK_ENABLE	RSZ_CLK_ENABLE	IPIPE_CLK_ENABLE	IPIPEIF_CLK_ENABLE	SYNC_ENABLE	PSYNC_CLK_SEL	VBUSM_CIDS				VBUSM_CPRIORITY			OCP_WRNP

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Bits	Field Name	Description	Type	Reset
31:30	DMA3_CFG	This bit field selects the DMA transfer configuration which is used with the ISS_DMA3 DMA request signal. This DMA request is generated from IPIPE_INT_LAST_PIXEL event. One can choose to use this DMA request to transfer the DPC initialization data, the gamma table, or both. 0x0: No DMA request associated with ISS_DMA3. 0x1: DPC DMA request associated with ISS_DMA3. Expected DMA transfer size is 2KB in the range 0x8000-0x87FF. DPC_EVT_INI must be set to 0. 0x3: DPC + GAMMA DMA request associated with ISS_DMA3. Expected DMA transfer size is 8KB in the range 0x8000-0x87FF and 0xA800-0xBFFF. DPC_EVT_INI must be set to 0. 0x2: GAMMA DMA request associated with ISS_DMA3. Expected DMA transfer size is 6KB in the range 0xA800-0xBFFF.	RW	0x0
29:28	RESERVED		R	0x0
27	RESERVED		R	0x0
26	HST_RD_CHK	When the HISTOGRAM computation is enabled and the HST DMA request is not used to read out the data, this register ensures that the data is read fast enough, else an interrupt ISP5_IRQSTATUS2_i[5] IPIPE_HST_ERR is triggered. The hardware sets automatically this bit to 1 when software can start reading the memory. **CAUTION** It is the software responsibility to set this bit to 0 after reading the data. Once the MPU has read the histogram data, it must clear this register, else the ISP5_IRQSTATUS2_i[5] IPIPE_HST_ERR will occur. Write 0x0: Clears the signal to avoid error generation. The software must write this bit to 0 after the last data read. Write 0x1: Reserved Read 0x1: The MPU can read the data from the memory. Needs to complete fast enough to avoid the interrupt generation. Read 0x0: No interrupt generation can happen	RW	0
25	DPC_EVT_INI	Select the IPIPE module event to be used to generate the DMA requests for the DPC submodule. 0x0: IPIPE_INT_LAST_PIX event is selected. 0x1: IPIPE_INT_DPC_INI event is selected.	RW	0

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Bits	Field Name	Description	Type	Reset
24	MSTANDBY	MStandby signal assertion and de-assertion control for power management transitions. After software reset, this bit is asserted. Write "1" to transition from normal mode to idle mode. The firmware needs to ensure that no more ISP processing is ongoing before setting up this bit. Write "0" to transition from idle mode to normal mode. The software should poll ISP5_CTRL.MSTANDBY_WAIT = 0 after writing ISP5_CTRL.MSTANDBY = 0 in a transition from idle to normal mode. 0x0: De-assert MStandby signal. May not be immediate due to power management handshaking btw the MStandby and Wait signals. 0x1: Assert MStandby signal	RW	1
23	VD_PULSE_EXT	VD pulse extension enable This bit enables or disables the VD extension bridge. By default, the bridge is enabled. At ISS level, it is expected that ISP5_CTRL.VD_PULSE_EXT = 1 when the VPORT gets data from the CSI2 RX module and ISP5_CTRL.VD_PULSE_EXT = 0 when the VPORT gets data from the parallel interface or the CCP2 RX module. There must be at least three clock cycles between the time this bit is modified and the HD/VD pulse for start of frame comes. 0x0: Disabled 0x1: Enabled	RW	1
22	PCLK_INV	Pixel clock inversion This bit enables or disables pixel clock inversion. The ISP always samples the data on the rising edge of the pixel clock. Enabling the inversion shifts the resampling period by 1/2 a pixel clock period. 0x0: Normal 0x1: Inversed	RW	0
21	MFLAG	MFlag signal generation control This bit controls how the OCP MFlag signal is generated on the ISS NOC. 0x0: The MFlag value is dynamic. 0x1: The MFlag value is static. The value is set with the ISP5_CTRL[3:1] VBUSM_CPRIORITY.	RW	0
20	MSTANDDBY_WAIT	MStandby / Wait power management status bit. The power management framework of the ISP is based on the handshaking of the MStandby and Wait signals. The software is not supposed to write inside the ISP slave port and initiate traffic when ISP5_CTRL.MSTANDBY bit is written. The software can poll this bit to know when Wait signal is deasserted. Read 0x1: MStandby signal is asserted. Read 0x0: MStandby signal is deasserted.	R	-
19:16	RESERVED		R	0x0
15	BL_CLK_ENABLE	BL clock enable 0x0: Disable 0x1: Enable	RW	0
14	ISIF_CLK_ENABLE	ISIF clock enable The ISP will return OCP_ERROR if one tries to program the module MMR or memory when the clock is disabled. There must be at least three clock cycles between the time this bit is modified and the HD/VD pulse for start of frame comes. 0x0: Disable 0x1: Enable	RW	0

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Bits	Field Name	Description	Type	Reset
13	H3A_CLK_ENABLE	H3A clock enable The ISP will return OCP_ERROR if one tries to program the module MMR or memory when the clock is disabled. 0x0: Disable 0x1: Enable	RW	0
12	RSZ_CLK_ENABLE	RESIZER clock enable The ISP will return OCP_ERROR if one tries to program the module MMR or memory when the clock is disabled. 0x0: Disable 0x1: Enable	RW	0
11	IPIPE_CLK_ENABLE	IPIPE clock enable The ISP will return OCP_ERROR if one tries to program the module MMR or memory when the clock is disabled. 0x0: Disable 0x1: Enable	RW	0
10	IPIPEIF_CLK_ENABLE	IPIPEIF clock enable The ISP will return OCP_ERROR if one tries to program the module MMR or memory when the clock is disabled. 0x0: Disable 0x1: Enable	RW	0
9	SYNC_ENABLE	PCLK Sync module enable 0x0: Disable. must be used only when the video port is not receiving data; for example, data is read from the IPIPEIF module memory read port. 0x1: Enable. must only be used when the video port is not receiving data.	RW	0
8	PSYNC_CLK_SEL	PCLK Sync clock select. This bit selects the clock which is used to resynchronize the input pixel clock. 0x0: MMR_CLK. Can be used if the input pixel clock is always lower than 100 MHz. 0x1: DMA_CLK. must be used if the pixel clock is higher than 100 MHz.	RW	0
7:4	VBUSM_CIDS	BL MAX VBUSM CIDs The BL module supports up to 16 CIDs/tags. This bit field sets up the maximum number of CISs/tags that the BL can use. The actual number of CIDs/tags is setup by VBUSM_CIDS + 1. Tag number 0 to VBUSM_CIDS are used.	RW	0xF
3:1	VBUSM_CPRIORITY	BL VBUSM priority setting 0x6: Normal Priority VBUSM cpriority[2:0] = 6 0x1: High Priority VBUSM cpriority[2:0] = 1 0x7: Normal Priority VBUSM cpriority[2:0] = 7 0x0: High Priority VBUSM cpriority[2:0] = 0 0x2: Medium Priority VBUSM cpriority[2:0] = 2 0x4: Normal Priority VBUSM cpriority[2:0] = 4 0x5: Normal Priority VBUSM cpriority[2:0] = 5 0x3: Medium Priority VBUSM cpriority[2:0] = 3	RW	0x4

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Bits	Field Name	Description	Type	Reset
0	OCP_WRNP	ISP OCP master port non-posted write control. 0x0: All writes are non posted. 0x1: All writes are posted.	RW	0

Table 8-415. Register Call Summary for Register ISP5_CTRL

ISS ISP

- ISS ISP Clocks: [0]
- ISS ISP Reset: [1] [2]
- ISS ISP DMA Requests: [3] [4]
- ISS ISP VP Top-Level Communication With CCP2 RX and CSI2 RX: [6] [7] [8]
- ISS ISP VP Pixel Clock Inversion: [9] [10] [11]
- ISS ISP BL Functional Description: [12]
- ISS ISP BL Out-of-Order Responses: [13]
- ISS ISP BL Dynamic and Static MFlag Generation: [14] [15] [16]
- ISS ISP BL Programming Model: [17] [18] [19] [20]
- ISS ISP5 SYS1 Register Summary: [21]
- ISS ISP5 SYS1 Register Description: [22] [23] [24] [25] [26] [27] [28] [29] [30] [31] [32]
- ISS ISP5 SYS2 Register Description: [34]

Table 8-416. ISP5_PG

Address Offset	0x0000 0070		
Physical Address	0x5201 0070	**Instance**	ISS_ISP5_SYS1
Description	PATTERN GENERATOR REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																										SRC_SEL		EN		WEN		HDPOL		VDPOL	

Bits	Field Name	Description	Type	Reset
31:6	RESERVED		R	0x0000000
5:4	SRC_SEL	Input mux selection 0x0: ISP video port is selected. 0x1: Reserved 0x3: Pattern generator is selected. 0x2: Reserved	RW	0x0
3	EN	0x0: Pattern generator off 0x1: Enable pattern generator	RW	0
2	WEN	0x0: WEN is always activated 0x1: WEN is on 8 cycles and off 8 cycles	RW	0
1	HDPOL	0x0: Active high 0x1: Active low	RW	0
0	VDPOL	0x0: Active high 0x1: Active low	RW	0

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Table 8-417. Register Call Summary for Register ISP5_PG

ISS ISP

- ISS ISP PG Functional Description: [0] [1] [2] [3] [4]
- ISS ISP PG Programming Model: [5] [6] [7] [8] [9]
- ISS ISP5 SYS1 Register Summary: [10]

Table 8-418. ISP5_PG_PULSE_CTRL

Address Offset	0x0000 0074		
Physical Address	0x5201 0074	**Instance**	ISS_ISP5_SYS1
Description	PATTERN GENERATOR REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				VDW												RESERVED	HDW														

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:16	VDW	Pattern generator VD width Width = VDW+1	RW	0x000
15:13	RESERVED		R	0x0
12:0	HDW	Pattern generator HD width Width = HDW+1	RW	0x0000

Table 8-419. Register Call Summary for Register ISP5_PG_PULSE_CTRL

ISS ISP

- ISS ISP PG Functional Description: [0] [1] [2] [3] [4]
- ISS ISP PG Programming Model: [5] [6]
- ISS ISP5 SYS1 Register Summary: [7]

Table 8-420. ISP5_PG_FRAME_SIZE

Address Offset	0x0000 0078		
Physical Address	0x5201 0078	**Instance**	ISS_ISP5_SYS1
Description	PATTERN GENERATOR REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PPLN																HLPFR															

Bits	Field Name	Description	Type	Reset
31:16	PPLN	Pattern Generator: pixels per line, PPLN+1	RW	0x0000
15:0	HLPFR	Pattern Generator: half lines per frame, HLPFR+1	RW	0x0000

Table 8-421. Register Call Summary for Register ISP5_PG_FRAME_SIZE

ISS ISP

- ISS ISP PG Functional Description: [0] [1] [2] [3] [4]
- ISS ISP PG Programming Model: [5] [6]
- ISS ISP5 SYS1 Register Summary: [7]

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Table 8-422. ISP5_MPSR

Address Offset	0x0000 007C		
Physical Address	0x5201 007C	**Instance**	ISS_ISP5_SYS1
Description	ISP memory access register. One need to pay attention when setting the bit fields in this register such that there is no conflict between the CPU and module accesses. Usually, the ISP modules must have access to the memories and it is only when the ISP is idle (vertical blanking period or module disabled that the CPU can access the memories.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							IPIPE_GAMMA_RGB_COPY	RESERVED			IPIPE_BSC_TB1	IPIPE_BSC_TB0	IPIPE_HST_TB3	IPIPE_HST_TB2	IPIPE_HST_TB1	IPIPE_HST_TB0	IPIPE_D3L_TB3	IPIPE_D3L_TB2	IPIPE_D3L_TB1	IPIPE_D3L_TB0	IPIPE_GBC_TB	IPIPE_YEE_TB	IPIPE_GMM_TBR	IPIPE_GMM_TBG	IPIPE_GMM_TBB	IPIPE_DPC_TB	ISIF_DCLAMP	ISIF_LSC_TB1	ISIF_LSC_TB0	ISIF_LIN_TB	RESERVED

Bits	Field Name	Description	Type	Reset
31:25	RESERVED		R	0x00
24	IPIPE_GAMMA_RGB_COPY	GAMMA table RGB Copy This bit must be enable when one wants to use the same Gamma table for the R, G and B color components. When the CPU writes the R table, it is automatically copied to the G and B tables if this bit is set. 0x0: Copy disable Independent RGB gamma table 0x1: Copy enable Common RGB Gamma table	RW	0
23:21	RESERVED		R	0x0
20	IPIPE_BSC_TB1	IPIPE BSC TB1 memory access priority This memory is expected to be read by the CPU or the DMA to get BSC information during vertical blanking period. 0x0: MODULE access has higher priority 0x1: CPU access has higher priority.	RW	0
19	IPIPE_BSC_TB0	IPIPE BSC TB0 memory access priority This memory is expected to be read by the CPU or the DMA to get BSC information during vertical blanking period. 0x0: MODULE access has higher priority 0x1: CPU access has higher priority.	RW	0
18	IPIPE_HST_TB3	IPIPE histogram memory #3 access priority This memory is expected to be read by the CPU or the DMA to get HST information during vertical blanking period. 0x0: MODULE access has higher priority 0x1: CPU access has higher priority.	RW	0
17	IPIPE_HST_TB2	IPIPE histogram memory #2 access priority This memory is expected to be read by the CPU or the DMA to get HST information during vertical blanking period. 0x0: MODULE access has higher priority 0x1: CPU access has higher priority.	RW	0

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Bits	Field Name	Description	Type	Reset
16	IPIPE_HST_TB1	IPIPE histogram memory #1 access priority This memory is expected to be read by the CPU or the DMA to get HST information during vertical blanking period. 0x0: MODULE access has higher priority 0x1: CPU access has higher priority.	RW	0
15	IPIPE_HST_TB0	IPIPE histogram memory #0 access priority This memory is expected to be read by the CPU or the DMA to get HST information during vertical blanking period. 0x0: MODULE access has higher priority 0x1: CPU access has higher priority.	RW	0
14	IPIPE_D3L_TB3	D3L TB3 memory access priority This memory is expected to be written during ISP initialization and potentially updated during vertical blanking periods. 0x0: MODULE access has higher priority 0x1: CPU access has higher priority.	RW	0
13	IPIPE_D3L_TB2	D3L TB2 memory access priority This memory is expected to be written during ISP initialization and potentially updated during vertical blanking periods. 0x0: MODULE access has higher priority 0x1: CPU access has higher priority.	RW	0
12	IPIPE_D3L_TB1	D3L TB1 memory access priority This memory is expected to be written during ISP initialization and potentially updated during vertical blanking periods. 0x0: MODULE access has higher priority 0x1: CPU access has higher priority.	RW	0
11	IPIPE_D3L_TB0	D3L TB0 memory access priority This memory is expected to be written during ISP initialization and potentially updated during vertical blanking periods. 0x0: MODULE access has higher priority 0x1: CPU access has higher priority.	RW	0
10	IPIPE_GBC_TB	IPIPE GBC TB memory access priority This memory is expected to be written during ISP initialization and potentially updated during vertical blanking periods. 0x0: MODULE access has higher priority 0x1: CPU access has higher priority.	RW	0
9	IPIPE_YEE_TB	YEE TB memory access priority This memory is expected to be written during ISP initialization and potentially updated during vertical blanking periods. 0x0: MODULE access has higher priority 0x1: CPU access has higher priority.	RW	0
8	IPIPE_GMM_TBR	IPIPE Gamma LUT R memory arbitration This memory is expected to be written during ISP initialization and potentially updated during vertical blanking periods. 0x0: MODULE access has higher priority 0x1: CPU access has higher priority.	RW	0

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Bits	Field Name	Description	Type	Reset
7	IPIPE_GMM_TBG	IPIPE Gamma LUT G memory arbitration This memory is expected to be written during ISP initialization and potentially updated during vertical blanking periods. 0x0: MODULE access has higher priority 0x1: CPU access has higher priority.	RW	0
6	IPIPE_GMM_TBB	IPIPE Gamma LUT B memory arbitration This memory is expected to be written during ISP initialization and potentially updated during vertical blanking periods. 0x0: MODULE access has higher priority 0x1: CPU access has higher priority.	RW	0
5	IPIPE_DPC_TB	IPIPE defect pixel memory arbitration This memory is expected to be written during ISP initialization and potentially updated during vertical blanking periods. 0x0: MODULE access has higher priority 0x1: CPU access has higher priority.	RW	0
4	ISIF_DCLAMP	ISIF DC accumulation memory arbitration This memory is expected to be written during ISP initialization and potentially updated during vertical blanking periods. 0x0: MODULE access has higher priority 0x1: CPU access has higher priority.	RW	0
3	ISIF_LSC_TB1	ISIF LSC memory 1 access This memory is expected to be written during ISP initialization and potentially updated during vertical blanking periods. 0x0: MODULE has memory access When the module has memory access, the potential concurrent CPU accesses (on the ISP memory map) to read the memory are stalled. The CPU will eventually get back the data during the horizontal or vertical blanking periods when the module is not making access anymore. 0x1: CPU has memory access When the CPU has memory access (read or write), it will cause data corruption if the module tries to perform concurrent memory accesses. The module cannot know that the read or write access has not taken place because of CPU accesses.	RW	0
2	ISIF_LSC_TB0	ISIF LSC memory 0 access This memory is expected to be written during ISP initialization and potentially updated during vertical blanking periods. 0x0: MODULE has memory access. When the module has memory access, the potential concurrent CPU accesses (on the ISP memory map) to read the memory are stalled. The CPU will eventually get back the data during the horizontal or vertical blanking periods when the module is not making access anymore. 0x1: CPU has memory access When the CPU has memory access (read or write), it will cause data corruption if the module tries to perform concurrent memory accesses. The module cannot know that the read or write access has not taken place because of CPU accesses.	RW	0
1	ISIF_LIN_TB	ISIF linearity compensation memory arbitration This memory is expected to be written during ISP initialization and potentially updated during vertical blanking periods. 0x0: MODULE access has higher priority 0x1: CPU access has higher priority.	RW	0

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Bits	Field Name	Description	Type	Reset
0	RESERVED		R	0

Table 8-423. Register Call Summary for Register ISP5_MPSR

ISS ISP
- ISS ISP BL Programming Model: [0]
- ISS ISP5 SYS1 Register Summary: [1]

Table 8-424. ISP5_BL_MTC_1

Address Offset	0x0000 0080		
Physical Address	0x5201 0080	**Instance**	ISS_ISP5_SYS1
Description	MEMORY REQUEST MINIMUM INTERVAL REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ISIF_R																IPIPEIF_R															

Bits	Field Name	Description	Type	Reset
31:16	ISIF_R	Sets the minimum interval btw two consecutive memory requests for the ISIF-Read port. Specified in number of interface clock cycles.	RW	0x0000
15:0	IPIPEIF_R	Sets the minimum interval btw two consecutive memory requests for the IPIPEIF-Read port. Specified in number of interface clock cycles.	RW	0x0000

Table 8-425. Register Call Summary for Register ISP5_BL_MTC_1

ISS ISP
- ISS ISP ISIF Expected Bandwidth on BL Ports: [0]
- ISS ISP BL Peak Memory Bandwidth Reduction: [1]
- ISS ISP BL Programming Model: [2] [3] [4]
- ISS ISP5 SYS1 Register Summary: [5]

Table 8-426. ISP5_BL_MTC_2

Address Offset	0x0000 0084		
Physical Address	0x5201 0084	**Instance**	ISS_ISP5_SYS1
Description	MEMORY REQUEST MINIMUM INTERVAL REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
H3A_W																RESERVED															

Bits	Field Name	Description	Type	Reset
31:16	H3A_W	Sets the minimum interval btw two consecutive memory requests for the H3A-Write port. Specified in number of interface clock cycles.	RW	0x0000
15:0	RESERVED		R	0x0000

Table 8-427. Register Call Summary for Register ISP5_BL_MTC_2

ISS ISP
- ISS ISP BL Peak Memory Bandwidth Reduction: [0]
- ISS ISP5 SYS1 Register Summary: [1]

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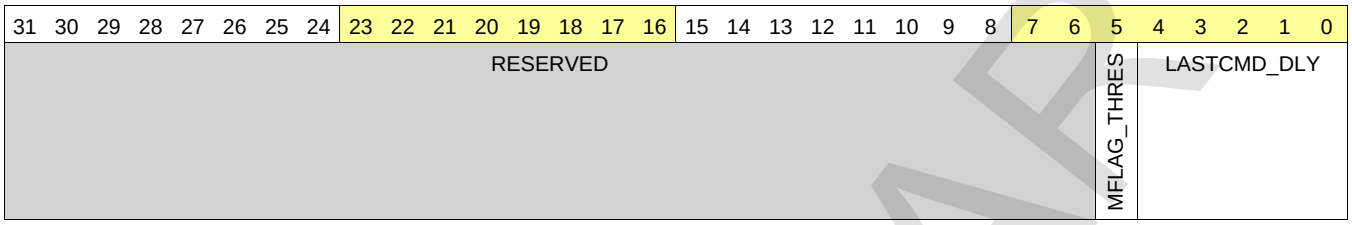
Table 8-428. ISP5_BL_VBUSM

Address Offset	0x0000 0088		
Physical Address	0x5201 0088	**Instance**	ISS_ISP5_SYS1
Description	BL VBUSM TUNING REGISTER The settings in the register are static and not expected to be modified dynamically.		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:6	RESERVED		R	0x0000000
5	MFLAG_THRES	MFLAG Threshold value The value of this bit field is a threshold which is compared to the MFlag output of the ISP5. If the BL MFlag signal is greater or equal to this threshold the last beat of the VBUSM command is delayed by ISP5_BL_VBUSM[4:0] LASTCMD_DLY cycles. Only values 0, 1 are valid, the least significant bit is tied off to 1 to make a 2-bit field. 0x0: Thres = 1 0x1: Thres = 3	RW	1
4:0	LASTCMD_DLY	The value of this bit field represents a delay expressed in cycles (L3 clock). This value is used to delay the last beat of the VBUSM command such that the ISP does not loose arbitration at the ISS level because the BL does not generate back to back requests by default. The last beat is delayed until the counter expires or the new request is accepted. This delay is used when the MFlag output of the ISP is greater or equal to ISP5_BL_VBUSM[5] MFLAG_THRES. One can set this value to 0 to disable the last command beat delay.	RW	0x04

Table 8-429. Register Call Summary for Register ISP5_BL_VBUSM

ISS ISP

- ISS ISP BL VBUSM2OCP Last Beat Command Delay: [0] [1] [2] [3]
- ISS ISP5 SYS1 Register Summary: [4]
- ISS ISP5 SYS1 Register Description: [5] [6]

8.3.5.3 ISS ISP5 SYS2 Registers

CAUTION

The ISS ISP5 SYS2 registers are limited to 32 bit and 16 bit data accesses; 8bit data access is not allowed and can corrupt register content.

8.3.5.3.1 ISS ISP5 SYS2 Register Summary

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Table 8-430. ISS ISP5 SYS2 Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	ISS_ISP5_SYS2 Base Address
ISP5_KEY_EN1	R	32	0x0000 0000	0x5201 00A0
ISP5_KEY_EN2	R	32	0x0000 0004	0x5201 00A4
ISP5_KEY_EN3	R	32	0x0000 0008	0x5201 00A8
ISP5_KEY_EN4	R	32	0x0000 000C	0x5201 00AC
ISP5_KEY_EN5	R	32	0x0000 0010	0x5201 00B0
ISP5_KEY_EN6	R	32	0x0000 0014	0x5201 00B4
ISP5_IRQSTATUS_RAW2_i (1)	RW	32	0x0000 0018 + (0x10 * i)	0x5201 00B8 + (0x10 * i)
ISP5_IRQSTATUS2_i (1)	RW	32	0x0000 001C + (0x10 * i)	0x5201 00BC + (0x10 * i)
ISP5_IRQENABLE_SET2_i (1)	RW	32	0x0000 0020 + (0x10 * i)	0x5201 00C0 + (0x10 * i)
ISP5_IRQENABLE_CLR2_i (1)	RW	32	0x0000 0024 + (0x10 * i)	0x5201 00C4 + (0x10 * i)

(1) i = 0 to 3

8.3.5.3.2 ISS ISP5 SYS2 Register Description

Table 8-431. ISP5_KEY_EN1

Address Offset	0x0000 0000		
Physical Address	0x5201 00A0	**Instance**	ISS_ISP5_SYS2
Description	IPIPE eFuse enable.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															KEY1_EN

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	KEY1_EN	eFuse enable Equals 1 when ISP5_EFUSE3_EN = 1 or 0 otherwise. Read 0x1: Enable Read 0x0: Disable	R	0

Table 8-432. Register Call Summary for Register ISP5_KEY_EN1

ISS ISP

- ISS ISP5 SYS2 Register Summary: [0]

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Table 8-433. ISP5_KEY_EN2

Address Offset	0x0000 0004		
Physical Address	0x5201 00A4	**Instance**	ISS_ISP5_SYS2
Description	ISIF eFuse enable.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															KEY1_EN

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	KEY1_EN	eFuse enable Equals 1 when ISP5_EFUSE1_EN = 1 or 0 otherwise. Read 0x1: Enable Read 0x0: Disable	R	1

Table 8-434. Register Call Summary for Register ISP5_KEY_EN2

ISS ISP

- ISS ISP5 SYS2 Register Summary: [0]

Table 8-435. ISP5_KEY_EN3

Address Offset	0x0000 0008		
Physical Address	0x5201 00A8	**Instance**	ISS_ISP5_SYS2
Description	ISIF eFuse enable.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															KEY_EN

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	KEY_EN	eFuse enable Equals 1 when ISP5_EFUSE3_EN = 1 or 0 otherwise. Read 0x1: Enable Read 0x0: Disable	R	0

Table 8-436. Register Call Summary for Register ISP5_KEY_EN3

ISS ISP

- ISS ISP5 SYS2 Register Summary: [0]

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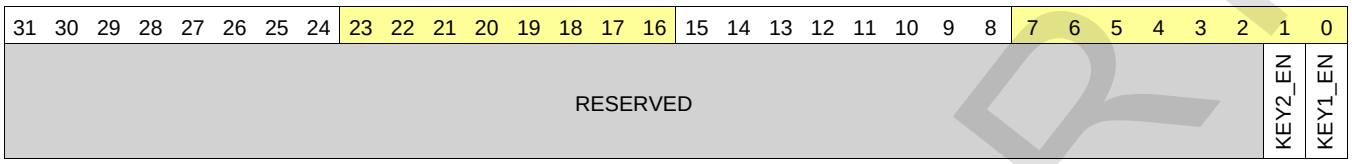
Table 8-437. ISP5_KEY_EN4

Address Offset	0x0000 000C		
Physical Address	0x5201 00AC	**Instance**	ISS_ISP5_SYS2
Description	IPIPEIF eFuse enable.		
Type	R		



Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	KEY2_EN	eFuse enable Equals 1 when ISP5_EFUSE4_EN = 1 or 0 otherwise. Read 0x1: Enable Read 0x0: Disable	R	0
0	KEY1_EN	eFuse enable Equals 1 when ISP5_EFUSE1_EN = 1 or 0 otherwise. Read 0x1: Enable Read 0x0: Disable	R	1

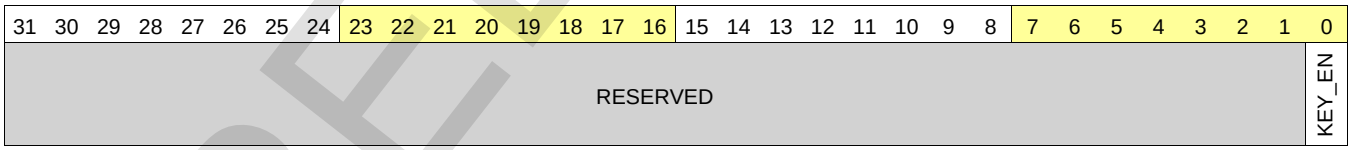
Table 8-438. Register Call Summary for Register ISP5_KEY_EN4

ISS ISP

- ISS ISP5 SYS2 Register Summary: [0]

Table 8-439. ISP5_KEY_EN5

Address Offset	0x0000 0010		
Physical Address	0x5201 00B0	**Instance**	ISS_ISP5_SYS2
Description	H3A eFuse enable.		
Type	R		



Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	KEY_EN	eFuse enable Equals 1 when ISP5_EFUSE2_EN = 1 or 0 otherwise. Read 0x1: Enable Read 0x0: Disable	R	0

Table 8-440. Register Call Summary for Register ISP5_KEY_EN5

ISS ISP

- ISS ISP5 SYS2 Register Summary: [0]

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Table 8-441. ISP5_KEY_EN6

Address Offset	0x0000 0014		
Physical Address	0x5201 00B4	**Instance**	ISS_ISP5_SYS2
Description	H3A eFuse enable.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															KEY_EN

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	KEY_EN	eFuse enable Equals 1 when ISP5_EFUSE3_EN = 1 or 0 otherwise. Read 0x1: Enable Read 0x0: Disable	R	0

Table 8-442. Register Call Summary for Register ISP5_KEY_EN6

ISS ISP

- ISS ISP5 SYS2 Register Summary: [0]

Table 8-443. ISP5_IRQSTATUS_RAW2_i

Address Offset	0x0000 0018 + (0x10 * i)	**Index**	i = 0 to 3
Physical Address	0x5201 00B8 + (0x10 * i)	**Instance**	ISS_ISP5_SYS2
Description	Per-event raw interrupt status vector. Raw status is set even if event is not enabled. Write 1 to set the (raw) status, mostly for debug. Overflow / underflow errors are not recoverable at ISP level, a software reset is required at ISS level. The ISP outputs 4 interrupt lines ISP5_IRQ0 to ISP5_IRQ3. Any internal ISP event can be merged on the 4 lines. A same event must be enabled on only one interrupt line.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																										RESERVED	IPIPE_HST_ERR	ISIF_OVF	IPIPE_BOXCAR_OVF	IPIPEIF_UDF	H3A_OVF

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Bits	Field Name	Description	Type	Reset
31:6	RESERVED		R	0x0000000
5	RESERVED		R	0x0
4	IPIPE_HST_ERR	IPIPE HISTOGRAM memory read error This error will happen when the histogram data is not read fast enough by the MPU or the DMA. When the data is read with the MPU, one need to pay attention to clear the ISP5_CTRL[26] HST_RD_CHK bit immediately after reading the last data, else this event will be set. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
3	ISIF_OVF	ISIF module overflow Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
2	IPIPE_BOXCAR_OVF	IPIPE BOXCAR module overflow Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
1	IPIPEIF_UDF	IPIPEIF module underflow interrupt Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
0	H3A_OVF	H3A module overflow interrupt. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0

Table 8-444. Register Call Summary for Register ISP5_IRQSTATUS_RAW2_i

ISS ISP

- ISS ISP IPIPEIF Module Events and Status Checking: [0]
- ISS ISP IPIPEIF Interframe Operations: [1]
- ISS ISP5 SYS2 Register Summary: [2]

Table 8-445. ISP5_IRQSTATUS2_i

Address Offset	0x0000 001C + (0x10 * i)	**Index**	i = 0 to 3
Physical Address	0x5201 00BC + (0x10 * i)	**Instance**	ISS_ISP5_SYS2
Description	Per-event "enabled" interrupt status vector. Enabled status is not set unless event is enabled. Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, that is, even if not enabled). Overflow / underflow errors are not recoverable at ISP level, a software reset is required at ISS level. The ISP outputs 4 interrupt lines ISP5_IRQ0 to ISP5_IRQ3. Any internal ISP event can be merged on the 4 lines. A same event must be enabled on only one interrupt line.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																										RESERVED	IPIPE_HST_ERR	ISIF_OVF	IPIPE_BOXCAR_OVF	IPIPEIF_UDF	H3A_OVF

Bits	Field Name	Description	Type	Reset
31:6	RESERVED		R	0x0000000
5	RESERVED		R	0x0
4	IPIPE_HST_ERR	IPIPE HISTOGRAM memory read error This error will happen when the histogram data is not read fast enough by either the MPU or the DMA. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
3	ISIF_OVF	ISIF module overflow Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
2	IPIPE_BOXCAR_OVF	IPIPE BOXCAR module overflow Overflow errors are not recoverable at ISP level, a software reset is required at ISS level. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
1	IPIPEIF_UDF	IPIPEIF module underflow interrupt Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
0	H3A_OVF	H3A module overflow interrupt. Overflow errors are not recoverable at ISP level, a software reset is required at ISS level. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0

Table 8-446. Register Call Summary for Register ISP5_IRQSTATUS2_i

ISS ISP

- ISS ISP DMA Requests:
- ISS ISP5 SYS1 Register Description: [4] [5]
- ISS ISP5 SYS2 Register Summary: [6]

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Table 8-447. ISP5_IRQENABLE_SET2_i

Address Offset	0x0000 0020 + (0x10 * i)	**Index**	i = 0 to 3
Physical Address	0x5201 00C0 + (0x10 * i)	**Instance**	ISS_ISP5_SYS2
Description	Per-event interrupt enable bit vector. Write 1 to set (enable interrupt). Readout equal to corresponding _CLR register. Overflow / underflow errors are not recoverable at ISP level, a software reset is required at ISS level. The ISP outputs 4 interrupt lines ISP5_IRQ0 to ISP5_IRQ3. Any internal ISP event can be merged on the 4 lines. A same event must be enabled on only one interrupt line.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																										RESERVED	IPIPE_HST_ERR	ISIF_OVF	IPIPE_BOXCAR_OVF	IPIPEIF_UDF	H3A_OVF

Bits	Field Name	Description	Type	Reset
31:6	RESERVED		R	0x0000000
5	RESERVED		R	0x0
4	IPIPE_HST_ERR	IPIPE HISTOGRAM memory read error This error will happen when the histogram data is not read fast enough by either the MPU or the DMA.	RW W1toSet	0
3	ISIF_OVF	ISIF module overflow	RW W1toSet	0
2	IPIPE_BOXCAR_OVF	IPIPE BOXCAR module overflow	RW W1toSet	0
1	IPIPEIF_UDF	IPIPEIF module underflow interrupt	RW W1toSet	0
0	H3A_OVF	H3A module overflow interrupt. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled	RW W1toSet	0

Table 8-448. Register Call Summary for Register ISP5_IRQENABLE_SET2_i

ISS ISP

- ISS ISP Interrupt Tree: [0] [2] [3] [4] [5]
- ISS ISP IPIPEIF Interrupts: [6]
- ISS ISP IPIPE Interrupts: [7]
- ISS ISP H3A Interrupts: [8]
- ISS ISP ISIF Interrupts: [9]
- ISS ISP5 SYS2 Register Summary: [10]

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Table 8-449. ISP5_IRQENABLE_CLR2_i

Address Offset	0x0000 0024 + (0x10 * i)	**Index**	i = 0 to 3
Physical Address	0x5201 00C4 + (0x10 * i)	**Instance**	ISS_ISP5_SYS2
Description	Per-event interrupt enable bit vector. Write 1 to clear (disable interrupt). Readout equal to corresponding _SET register. Overflow / underflow errors are not recoverable at ISP level, a software reset is required at ISS level. The ISP outputs 4 interrupt lines ISP5_IRQ0 to ISP5_IRQ3. Any internal ISP event can be merged on the 4 lines. A same event must be enabled on only one interrupt line.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																										RESERVED	IPIPE_HST_ERR	ISIF_OVF	IPIPE_BOXCAR_OVF	IPIPEIF_UDF	H3A_OVF

Bits	Field Name	Description	Type	Reset
31:6	RESERVED		R	0x0000000
5	RESERVED		R	0x0
4	IPIPE_HST_ERR	IPIPE HISTOGRAM memory read error This error will happen when the histogram data is not read fast enough by either the MPU or the DMA. Write 0x0: No action Write 0x1: Disable Interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled	RW W1toClr	0
3	ISIF_OVF	ISIF module overflow Write 0x0: No action Write 0x1: Disable Interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled	RW W1toClr	0
2	IPIPE_BOXCAR_OVF	IPIPE BOXCAR module overflow Write 0x0: No action Write 0x1: Disable Interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled	RW W1toClr	0
1	IPIPEIF_UDF	IPIPEIF module underflow interrupt Write 0x0: No action Write 0x1: Disable Interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled	RW W1toClr	0
0	H3A_OVF	H3A module overflow interrupt. Write 0x0: No action Write 0x1: Disable Interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled	RW W1toClr	0

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Table 8-450. Register Call Summary for Register ISP5_IRQENABLE_CLR2_i

ISS ISP
- ISS ISP5 SYS2 Register Summary: [0]

8.3.5.4 ISS RESIZER Registers

8.3.5.4.1 ISS RESIZER Register Summary

Table 8-451. ISS RESIZER Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	ISS_RESIZER Base Address
RSZ_REVISION	R	32	0x0000 0000	0x5201 0400
RSZ_SYSCONFIG	RW	32	0x0000 0004	0x5201 0404
RESERVED	R	32	0x0000 0008	0x5201 0408
RSZ_IN_FIFO_CTRL	RW	32	0x0000 000C	0x5201 040C
RSZ_GNC	R	32	0x0000 0010	0x5201 0410
RSZ_FRACDIV	RW	32	0x0000 0014	0x5201 0414
RSZ_SRC_EN	RW	32	0x0000 0020	0x5201 0420
RSZ_SRC_MODE	RW	32	0x0000 0024	0x5201 0424
RSZ_SRC_FMT0	RW	32	0x0000 0028	0x5201 0428
RSZ_SRC_FMT1	RW	32	0x0000 002C	0x5201 042C
RSZ_SRC_VPS	RW	32	0x0000 0030	0x5201 0430
RSZ_SRC_VSZ	RW	32	0x0000 0034	0x5201 0434
RSZ_SRC_HPS	RW	32	0x0000 0038	0x5201 0438
RSZ_SRC_HSZ	RW	32	0x0000 003C	0x5201 043C
RSZ_DMA_RZA	RW	32	0x0000 0040	0x5201 0440
RSZ_DMA_RZB	RW	32	0x0000 0044	0x5201 0444
RSZ_DMA_STA	R	32	0x0000 0048	0x5201 0448
RSZ_GCK_MMR	RW	32	0x0000 004C	0x5201 044C
RESERVED	R	32	0x0000 0050	0x5201 0450
RSZ_GCK_SDR	RW	32	0x0000 0054	0x5201 0454
RSZ_IRQ_RZA	RW	32	0x0000 0058	0x5201 0458
RSZ_IRQ_RZB	RW	32	0x0000 005C	0x5201 045C
RSZ_YUV_Y_MIN	RW	32	0x0000 0060	0x5201 0460
RSZ_YUV_Y_MAX	RW	32	0x0000 0064	0x5201 0464
RSZ_YUV_C_MIN	RW	32	0x0000 0068	0x5201 0468
RSZ_YUV_C_MAX	RW	32	0x0000 006C	0x5201 046C
RSZ_YUV_PHS	RW	32	0x0000 0070	0x5201 0470
RSZ_SEQ	RW	32	0x0000 0074	0x5201 0474
RZA_EN	RW	32	0x0000 0078	0x5201 0478
RZA_MODE	RW	32	0x0000 007C	0x5201 047C
RZA_420	RW	32	0x0000 0080	0x5201 0480
RZA_I_VPS	RW	32	0x0000 0084	0x5201 0484
RZA_I_HPS	RW	32	0x0000 0088	0x5201 0488
RZA_O_VSZ	RW	32	0x0000 008C	0x5201 048C
RZA_O_HSZ	RW	32	0x0000 0090	0x5201 0490
RZA_V_PHS_Y	RW	32	0x0000 0094	0x5201 0494
RZA_V_PHS_C	RW	32	0x0000 0098	0x5201 0498
RZA_V_DIF	RW	32	0x0000 009C	0x5201 049C

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Table 8-451. ISS RESIZER Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	ISS_RESIZER Base Address
RZA_V_TYP	RW	32	0x0000 00A0	0x5201 04A0
RZA_V_LPF	RW	32	0x0000 00A4	0x5201 04A4
RZA_H_PHS	RW	32	0x0000 00A8	0x5201 04A8
RZA_H_PHS_ADJ	RW	32	0x0000 00AC	0x5201 04AC
RZA_H_DIF	RW	32	0x0000 00B0	0x5201 04B0
RZA_H_TYP	RW	32	0x0000 00B4	0x5201 04B4
RZA_H_LPF	RW	32	0x0000 00B8	0x5201 04B8
RZA_DWN_EN	RW	32	0x0000 00BC	0x5201 04BC
RZA_DWN_AV	RW	32	0x0000 00C0	0x5201 04C0
RZA_RGB_EN	RW	32	0x0000 00C4	0x5201 04C4
RZA_RGB_TYP	RW	32	0x0000 00C8	0x5201 04C8
RZA_RGB_BLD	RW	32	0x0000 00CC	0x5201 04CC
RZA_SDR_Y_BAD_H	RW	32	0x0000 00D0	0x5201 04D0
RZA_SDR_Y_BAD_L	RW	32	0x0000 00D4	0x5201 04D4
RZA_SDR_Y_SAD_H	RW	32	0x0000 00D8	0x5201 04D8
RZA_SDR_Y_SAD_L	RW	32	0x0000 00DC	0x5201 04DC
RZA_SDR_Y_OFT	RW	32	0x0000 00E0	0x5201 04E0
RZA_SDR_Y_PTR_S	RW	32	0x0000 00E4	0x5201 04E4
RZA_SDR_Y_PTR_E	RW	32	0x0000 00E8	0x5201 04E8
RZA_SDR_C_BAD_H	RW	32	0x0000 00EC	0x5201 04EC
RZA_SDR_C_BAD_L	RW	32	0x0000 00F0	0x5201 04F0
RZA_SDR_C_SAD_H	RW	32	0x0000 00F4	0x5201 04F4
RZA_SDR_C_SAD_L	RW	32	0x0000 00F8	0x5201 04F8
RZA_SDR_C_OFT	RW	32	0x0000 00FC	0x5201 04FC
RZA_SDR_C_PTR_S	RW	32	0x0000 0100	0x5201 0500
RZA_SDR_C_PTR_E	RW	32	0x0000 0104	0x5201 0504
RZB_EN	RW	32	0x0000 0108	0x5201 0508
RZB_MODE	RW	32	0x0000 010C	0x5201 050C
RZB_420	RW	32	0x0000 0110	0x5201 0510
RZB_I_VPS	RW	32	0x0000 0114	0x5201 0514
RZB_I_HPS	RW	32	0x0000 0118	0x5201 0518
RZB_O_VSZ	RW	32	0x0000 011C	0x5201 051C
RZB_O_HSZ	RW	32	0x0000 0120	0x5201 0520
RZB_V_PHS_Y	RW	32	0x0000 0124	0x5201 0524
RZB_V_PHS_C	RW	32	0x0000 0128	0x5201 0528
RZB_V_DIF	RW	32	0x0000 012C	0x5201 052C
RZB_V_TYP	RW	32	0x0000 0130	0x5201 0530
RZB_V_LPF	RW	32	0x0000 0134	0x5201 0534
RZB_H_PHS	RW	32	0x0000 0138	0x5201 0538
RZB_H_PHS_ADJ	RW	32	0x0000 013C	0x5201 053C
RZB_H_DIF	RW	32	0x0000 0140	0x5201 0540
RZB_H_TYP	RW	32	0x0000 0144	0x5201 0544
RZB_H_LPF	RW	32	0x0000 0148	0x5201 0548
RZB_DWN_EN	RW	32	0x0000 014C	0x5201 054C
RZB_DWN_AV	RW	32	0x0000 0150	0x5201 0550
RZB_RGB_EN	RW	32	0x0000 0154	0x5201 0554
RZB_RGB_TYP	RW	32	0x0000 0158	0x5201 0558

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Table 8-451. ISS RESIZER Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	ISS_RESIZER Base Address
RZB_RGB_BLD	RW	32	0x0000 015C	0x5201 055C
RZB_SDR_Y_BAD_H	RW	32	0x0000 0160	0x5201 0560
RZB_SDR_Y_BAD_L	RW	32	0x0000 0164	0x5201 0564
RZB_SDR_Y_SAD_H	RW	32	0x0000 0168	0x5201 0568
RZB_SDR_Y_SAD_L	RW	32	0x0000 016C	0x5201 056C
RZB_SDR_Y_OFT	RW	32	0x0000 0170	0x5201 0570
RZB_SDR_Y_PTR_S	RW	32	0x0000 0174	0x5201 0574
RZB_SDR_Y_PTR_E	RW	32	0x0000 0178	0x5201 0578
RZB_SDR_C_BAD_H	RW	32	0x0000 017C	0x5201 057C
RZB_SDR_C_BAD_L	RW	32	0x0000 0180	0x5201 0580
RZB_SDR_C_SAD_H	RW	32	0x0000 0184	0x5201 0584
RZB_SDR_C_SAD_L	RW	32	0x0000 0188	0x5201 0588
RZB_SDR_C_OFT	RW	32	0x0000 018C	0x5201 058C
RZB_SDR_C_PTR_S	RW	32	0x0000 0190	0x5201 0590
RZB_SDR_C_PTR_E	RW	32	0x0000 0194	0x5201 0594

8.3.5.4.2 ISS RESIZER Register Description

Table 8-452. RSZ_REVISION

Address Offset	0x0000 0000		
Physical Address	0x5201 0400	**Instance**	ISS_RESIZER
Description	IP Revision Identifier (X.Y.R) Used by software to track features, bugs, and compatibility		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP Revision	R	See(1)

(1) TI internal data

Table 8-453. Register Call Summary for Register RSZ_REVISION

ISS ISP

- ISS RESIZER Register Summary: [0]

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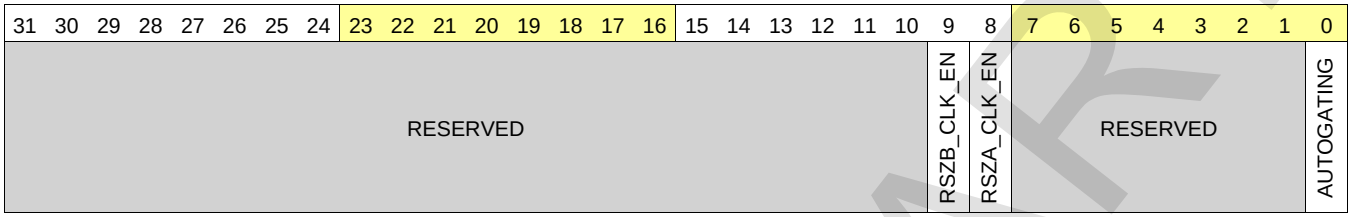
Table 8-454. RSZ_SYSCONFIG

Address Offset	0x0000 0004		
Physical Address	0x5201 0404	**Instance**	ISS_RESIZER
Description	SYSTEM CONFIGURATION REGISTER This register is not shadowed. There is no standalone software reset for the resizer module.		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:10	RESERVED		R	0x000000
9	RSZB_CLK_EN	Resizer B clock enable This bit enable to enable / disable the RESIZER B clock. Note that it is a second level clock enable. This bit has effect only if RSZ_GCK_SDR is set to 1. 0x0: off 0x1: on	RW	0
8	RSZA_CLK_EN	Resizer A clock enable This bit enable to enable / disable the RESIZER A clock. Note that it is a second level clock enable. This bit has effect only if RSZ_GCK_SDR is set to 1. 0x0: off 0x1: on	RW	0
7:1	RESERVED		R	0x00
0	AUTOGATING	Internal Clock Gating Strategy Enables or disables auto clock gating. **NOTE:** This is only for debug purposes. When this bit is set to "0" autogating is not performed on any of the clocks, thus the clocks stay free running. Though, they are still controlled by the clock enable bit fields RSZA_CLK_EN and RSZB_CLK_EN. 0x0: Clocks are free running 0x1: Automatic clock gating strategy.	RW	1

Table 8-455. Register Call Summary for Register RSZ_SYSCONFIG

ISS ISP

- ISS ISP RSZ Functional Description: [0]
- ISS ISP RSZ Hardware Setup/Initialization: [1] [2]
- ISS ISP RSZ Programming Constraints: [3]
- ISS RESIZER Register Summary: [4]

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Table 8-456. RSZ_IN_FIFO_CTRL

Address Offset	0x0000 000C		
Physical Address	0x5201 040C	**Instance**	ISS_RESIZER
Description	INPUT DATA BUFFER CONTROL REGISTER This register is not shadowed		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								THRLD_LOW								RESERVED								THRLD_HIGH							

Bits	Field Name	Description	Type	Reset
31:29	RESERVED		R	0x0
28:16	THRLD_LOW	When RSZ_IN_FIFO_CTRL.THRLD_HIGH = RSZ_IN_FIFO_CTRL.THRLD_LOW, the rsz_stall_input is not asserted. The only purpose of the RSZ_IN_FIFO_CTRL.THRLD_LOW register is to prevent rsz_stall_input signal assertion.	RW	0x0000
15:13	RESERVED		R	0x0
12:0	THRLD_HIGH	High threshold value. The rsz_stall_input signal is asserted if 2 lines of circular buffer are full and the third line has more pixels than RSZ_IN_FIFO_CTRL.THRLD_HIGH. The rsz_stall_input signal stays high as long as one full line is not free for receiving further data. THRLD_HIGH is in terms of line size and can at max be programmed equal to the input line size (RSZ_SRC_HSZ).	RW	0x0000

Table 8-457. Register Call Summary for Register RSZ_IN_FIFO_CTRL

ISS ISP

- ISS ISP RSZ Functional Description: [0]
- ISS ISP RSZ Hardware Setup/Initialization: [3] [4]
- ISS ISP RSZ Programming Constraints: [5]
- ISS RESIZER Register Summary: [6]
- ISS RESIZER Register Description: [7] [8] [9] [10]

Table 8-458. RSZ_GNC

Address Offset	0x0000 0010		
Physical Address	0x5201 0410	**Instance**	ISS_RESIZER
Description	GENERIC PARAMETER REGISTER		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								RSZB_MEM_LINE_SIZE								RESERVED								RSZA_MEM_LINE_SIZE							

Bits	Field Name	Description	Type	Reset
31:29	RESERVED		R	0x0
28:16	RSZB_MEM_LINE_SIZE	Resizer #B memory line size (pixels). The output image cannot exceed this size.	R	0x0920

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Bits	Field Name	Description	Type	Reset
15:13	RESERVED		R	0x0
12:0	RSZA_MEM_LINE_SIZE	Resizer #A memory line size (pixels). The output image cannot exceed this size.	R	0x1500

Table 8-459. Register Call Summary for Register RSZ_GNC

ISS ISP

- ISS ISP RSZ Functional Description: [0]
- ISS RESIZER Register Summary: [3]

Table 8-460. RSZ_FRACDIV

Address Offset	0x0000 0014		
Physical Address	0x5201 0414	**Instance**	ISS_RESIZER
Description	Fractional clock divider settings		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:0	RSZ_FRACDIV	Fractional clock divider value. The fractional clock divider gates the read requests made to the input data buffer such that the input data buffer is read at an average frequency equal to FFCLK instead of FCLK. The value of FFCLK depends upon the upscaling ratios as well as the input pixel clock: see the functional spec. We have FFCLK = FCLK / FRACDIV MHz and RSZ_FRACDIV = 65536 / FRACDIV. When RSZ_ FRACDIV = 65536, we have: FFCLK = FCLK.	RW	0xFFFF

Table 8-461. Register Call Summary for Register RSZ_FRACDIV

ISS ISP

- ISS ISP RSZ Hardware Setup/Initialization: [0] [1]
- ISS ISP RSZ Global Image Processing Settings: [2] [3]
- ISS RESIZER Register Summary: [4]
- ISS RESIZER Register Description: [5] [6]

Table 8-462. RSZ_SRC_EN

Address Offset	0x0000 0020		
Physical Address	0x5201 0420	**Instance**	ISS_RESIZER
Description	RESIZER ENABLE REGISTER This register is not shadowed		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															EN

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Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	EN	Resizer module enable The start flag of the RESIZER module. When EN is set to 1, the RESIZER module starts the processing from the next rising edge of the VD pulse. If the processing mode of the RESIZER module is set to "one shot", the EN bit is cleared to 0 after the end of the processing. One has to pay attention that when this bit is enabled and 0x0: Disable 0x1: Enable	RW	0

Table 8-463. Register Call Summary for Register RSZ_SRC_EN

ISS ISP

- ISS ISP RSZ Functional Description: [0]
- ISS ISP RSZ Hardware Setup/Initialization: [1] [2]
- ISS ISP RSZ Global Image Processing Settings: [3]
- ISS ISP RSZ Programming Constraints: [4]
- ISS RESIZER Register Summary: [5]

Table 8-464. RSZ_SRC_MODE

Address Offset	0x0000 0024		
Physical Address	0x5201 0424	**Instance**	ISS_RESIZER
Description	This register is not shadowed		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														WRT	OST

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	WRT	Video port WEN signal selection This bit selects whether the WEN signal which is present on the IPIPE and IPIPEIF video port is used or not to select the input data. If WRT is 0, the RESIZER module ignores the WEN signal and processes all image frame while RESIZER is enabled. If WRT is 1, the RESIZER module only processes the lines that arrived while the WEN is high. HD is used to sample the WEN signal. 0x0: Disable 0x1: Enable	RW	0
0	OST	The processing mode selection of the RESIZER module. Value 0 indicates the mode of free run, value 1 indicates the mode of one shot. 0x0: Free running 0x1: One shot	RW	0

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Table 8-465. Register Call Summary for Register RSZ_SRC_MODE

ISS ISP

- ISS ISP RSZ Interfaces: [0]
- ISS ISP RSZ Functional Description: [1]
- ISS ISP RSZ Hardware Setup/Initialization: [2] [3]
- ISS ISP RSZ Engines Interframe Image Processing Settings: [4]
- ISS ISP RSZ Programming Constraints: [5]
- ISS RESIZER Register Summary: [6]

Table 8-466. RSZ_SRC_FMT0

Address Offset	0x0000 0028		
Physical Address	0x5201 0428	**Instance**	ISS_RESIZER
Description	This register is not shadowed		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														BYPASS	SEL

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	BYPASS	Pass Through This bit enables or disables the RESIZER module pass through mode. The pass through mode can transfer images which are 8K pixel wide. When it is enabled, the input data buffer and the resizer engines are bypassed. 0x0: Pass through off = normal output mode, the input data buffer is used. 0x1: Pass through on = normal output mode, the input data buffer is bypassed.	RW	0
0	SEL	Input selection This bit selects which of the two video port is selected to push data through the RESIZER module. 0x0: IPIPE 0x1: IPIPEIF	RW	0

Table 8-467. Register Call Summary for Register RSZ_SRC_FMT0

ISS ISP

- ISS ISP RSZ Functional Description: [0] [1] [2]
- ISS ISP RSZ Hardware Setup/Initialization: [3] [4]
- ISS ISP RSZ Programming Constraints: [5]
- ISS RESIZER Register Summary: [6]
- ISS RESIZER Register Description: [7] [8] [9] [10] [11]

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Table 8-468. RSZ_SRC_FMT1

Address Offset	0x0000 002C		
Physical Address	0x5201 042C	**Instance**	ISS_RESIZER
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													COL	IN420	RAW

Bits	Field Name	Description	Type	Reset
31:3	RESERVED		R	0x0000 0000
2	COL	Y/C selection This bit is valid only if the input data is YUV4:2:0 (IN420 = 1). It enables to specify where the data which is input to the RESIZER module is luma or chroma data. 0x0: Y data is input 0x1: Chroma data is input	RW	0
1	IN420	Chroma Format Selection This bit sets the chroma undersampling when YUV data is input to the RESIZER module. 0x0: YUV4:2:2 is input 0x1: YUV4:2:0 is input	RW	0
0	RAW	Pass-through mode input data format selection This bit affects the horizontal reversal (flipping) process. 0x0: Flipping preserves YCbCr format 0x1: Flipping preserves RAW format	RW	0

Table 8-469. Register Call Summary for Register RSZ_SRC_FMT1

ISS ISP

- ISS ISP RSZ Functional Description: [0] [1] [2] [3]
- ISS ISP RSZ Global Image Processing Settings: [4] [5]
- ISS ISP RSZ Engines Interframe Image Processing Settings: [6] [7]
- ISS RESIZER Register Summary: [8]

Table 8-470. RSZ_SRC_VPS

Address Offset	0x0000 0030		
Physical Address	0x5201 0430	**Instance**	ISS_RESIZER
Description	VERTICAL POSITION REGISTER This register is not shadowed		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																VPS															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:0	VPS	Vertical Start Position Sets the vertical position of the global frame from the rising edge of the VD. The RSZ module will start the image processing from the VPS'th line. This value can be odd or even whatever the input data format.	RW	0x0000

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Table 8-471. Register Call Summary for Register RSZ_SRC_VPS

ISS ISP

- ISS ISP RSZ Functional Description: [0]
- ISS ISP RSZ Global Image Processing Settings: [1]
- ISS ISP RSZ Engines Interframe Image Processing Settings: [2]
- ISS ISP RSZ Programming Constraints: [3]
- ISS RESIZER Register Summary: [4]

Table 8-472. RSZ_SRC_VSZ

Address Offset	0x0000 0034		
Physical Address	0x5201 0434	**Instance**	ISS_RESIZER
Description	VERTICAL SIZER REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								VSZ							

Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000
12:0	VSZ	Vertical Processing Size Sets the vertical size of the processing area. The RSZ module will process (VSZ+1) lines. This value can be odd or even whatever the input data format.	RW	0x0000

Table 8-473. Register Call Summary for Register RSZ_SRC_VSZ

ISS ISP

- ISS ISP RSZ Functional Description: [0]
- ISS ISP RSZ Global Image Processing Settings: [1]
- ISS ISP RSZ Engines Interframe Image Processing Settings: [2]
- ISS RESIZER Register Summary: [3]

Table 8-474. RSZ_SRC_HPS

Address Offset	0x0000 0038		
Physical Address	0x5201 0438	**Instance**	ISS_RESIZER
Description	HORIZONTAL POSITION REGISTER This register is not shadowed		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																HPS															

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Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:0	HPS	Horizontal Start Position The RSZ_SRC_HPS register has two functions: The first function is to compensate for possible delay between the HD pulse and the first valid data. It is possible for this delay to be different than 0 when the RESIZER module gets its input data from the VP connected to the IPIPEIF module (the offset value can be odd or even). When data are coming from the IPIPE module, it is not required to resynchronize HD and the first valid data. The second function is to crop the data in the horizontal direction. When used for cropping, only RSZ_SRC_HPS must be even or null.	RW	0x0000

Table 8-475. Register Call Summary for Register RSZ_SRC_HPS

ISS ISP

- ISS ISP RSZ Functional Description: [0]
- ISS ISP RSZ Global Image Processing Settings: [1]
- ISS ISP RSZ Engines Interframe Image Processing Settings: [2]
- ISS ISP RSZ Programming Constraints: [3]
- ISS RESIZER Register Summary: [4]
- ISS RESIZER Register Description: [5] [6]

Table 8-476. RSZ_SRC_HSZ

Address Offset	0x0000 003C		
Physical Address	0x5201 043C	**Instance**	ISS_RESIZER
Description	HORIZONTAL SIZE REGISTER The HSZ value is given by HSZ concatenated with HSZ_LSB		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								HSZ							

Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000
12:0	HSZ	Horizontal size Sets the horizontal size of the processing area. The RSZ module processes (HSZ+1) pixels. (HSZ+1) must be even for YUV4:2:2 and RAW data. The valid available values for HSZ are 1~xxxx.	RW	0x0000

Table 8-477. Register Call Summary for Register RSZ_SRC_HSZ

ISS ISP

- ISS ISP RSZ Functional Description: [0] [1]
- ISS ISP RSZ Global Image Processing Settings: [2]
- ISS ISP RSZ Engines Interframe Image Processing Settings: [3]
- ISS RESIZER Register Summary: [4]
- ISS RESIZER Register Description: [5]

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Table 8-478. RSZ_DMA_RZA

Address Offset	0x0000 0040		
Physical Address	0x5201 0440	**Instance**	ISS_RESIZER
Description	RESIZER A - MEMORY REQUEST MINIMUM INTERVAL REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RZA															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:0	RZA	Sets the minimum interval btw two consecutive memory request for resizer #A. Specified in number of interface clock cycles. Values of 0, 1, and 2 are used as a condition to keep the bandwidth limiter off. When this function is enabled, this value must be greater than 10 cycles.	RW	0x0000

Table 8-479. Register Call Summary for Register RSZ_DMA_RZA

ISS ISP

- ISS ISP RSZ Interfaces: [0]
- ISS ISP BL Peak Memory Bandwidth Reduction: [1]
- ISS ISP RSZ Global Image Processing Settings: [2]
- ISS RESIZER Register Summary: [3]

Table 8-480. RSZ_DMA_RZB

Address Offset	0x0000 0044		
Physical Address	0x5201 0444	**Instance**	ISS_RESIZER
Description	RESIZER B - MEMORY REQUEST MINIMUM INTERVAL REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RZB															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:0	RZB	Sets the minimum interval btw two consecutive memory request for resizer #B. Specified in number of interface clock cycles. Values of 0, 1, and 2 are used as a condition to keep the bandwidth limiter off. When this function is enabled, this value must be greater than 10 cycles.	RW	0x0000

Table 8-481. Register Call Summary for Register RSZ_DMA_RZB

ISS ISP

- ISS ISP RSZ Interfaces: [0]
- ISS ISP BL Peak Memory Bandwidth Reduction: [1]
- ISS ISP RSZ Global Image Processing Settings: [2]
- ISS RESIZER Register Summary: [3]

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Table 8-482. RSZ_DMA_STA

Address Offset	0x0000 0048		
Physical Address	0x5201 0448	**Instance**	ISS_RESIZER
Description	RESIZER STATUS REGISTER		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															STATUS

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	STATUS	Resizer process status This bit is set in the time window from rsz_int_reg to rsz_int_dma. Read 0x1: Active Read 0x0: Not active	R	0

Table 8-483. Register Call Summary for Register RSZ_DMA_STA

ISS ISP

- ISS ISP RSZ Interfaces: [0]
- ISS RESIZER Register Summary: [1]

Table 8-484. RSZ_GCK_MMR

Address Offset	0x0000 004C		
Physical Address	0x5201 044C	**Instance**	ISS_RESIZER
Description	MMR CLOCK CONTROL REGISTER This register is not shadowed		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															MMR

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	MMR	The on/off selection of the MMR interface clock which is used for MMR register access. 0x0: Off 0x1: On	RW	0

Table 8-485. Register Call Summary for Register RSZ_GCK_MMR

ISS ISP

- ISS ISP RSZ Interfaces: [0]
- ISS ISP RSZ Hardware Setup/Initialization: [1]
- ISS ISP RSZ Programming Constraints: [2]
- ISS RESIZER Register Summary: [3]

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Table 8-486. RSZ_GCK_SDR

Address Offset	0x0000 0054		
Physical Address	0x5201 0454	**Instance**	ISS_RESIZER
Description	CORE CLOCK CONTROL REGISTER This register is not shadowed		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															CORE

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	CORE	RSZ Core Clock Enable. This bit enables or disables the resizer core functional clock. When this bit is off, the resizer core (interpolator) is automatically bypassed (resizer-bypass mode of pass-through mode is selected depending on RSZ_SRC_FMT0 value). In resizer-bypass mode or pass-through mode, no up-scaling or downscaling process is operated. 0x0: Resizer core clock disabled. Resizer in bypass mode if RSZ_SRC_FMT0.BYPASS = 0 Resizer in pass-through if RSZ_SRC_FMT0.BYPASS = 1 0x1: Resizer core clock enabled. Resizer in rescaling mode if RSZ_SRC_FMT0.BYPASS = 0 Resizer in pass-through if RSZ_SRC_FMT0.BYPASS = 1	RW	0

Table 8-487. Register Call Summary for Register RSZ_GCK_SDR

ISS ISP

- ISS ISP RSZ Functional Description: [0] [1]
- ISS ISP RSZ Hardware Setup/Initialization: [2] [3] [4] [5]
- ISS ISP RSZ Programming Constraints: [6]
- ISS RESIZER Register Summary: [7]
- ISS RESIZER Register Description: [8] [9]

Table 8-488. RSZ_IRQ_RZA

Address Offset	0x0000 0058		
Physical Address	0x5201 0458	**Instance**	ISS_RESIZER
Description	RESIZER A - CIRCULAR BUFFER INTERRUPT INTERVAL REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RZA							

Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000
12:0	RZA	Resizer A circular buffer interval Sets the circular buffer interval for Resizer A. The interrupt is triggered every time (RZA+1) lines are written to the circular buffer (Y buffer). The range goes from 1 to 8192 lines. Usually, the circular buffer vertical size should be a multiple of RZA.	RW	0x0000

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Table 8-489. Register Call Summary for Register RSZ_IRQ_RZA

ISS ISP

- ISS ISP RSZ Interrupts: [0] [1] [2]
- ISS ISP RSZ Hardware Setup/Initialization: [3]
- ISS ISP5 SYS1 Register Description: [4] [5] [6] [7] [8] [9] [10] [11]
- ISS RESIZER Register Summary: [12]

Table 8-490. RSZ_IRQ_RZB

Address Offset	0x0000 005C		
Physical Address	0x5201 045C	**Instance**	ISS_RESIZER
Description	RESIZER B - CIRCULAR BUFFER INTERRUPT INTERVAL REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RZB							

Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000
12:0	RZB	Resizer B circular buffer interval Sets the circular buffer interval for Resizer B. The interrupt is triggered every time (RZB+1) lines are written to the circular buffer (Y buffer). The range goes from 1 to 8192 lines. Usually, the circular buffer vertical size should be a multiple of RZB.	RW	0x0000

Table 8-491. Register Call Summary for Register RSZ_IRQ_RZB

ISS ISP

- ISS ISP RSZ Interrupts: [0]
- ISS ISP RSZ Hardware Setup/Initialization: [1]
- ISS ISP5 SYS1 Register Description: [2] [3] [4] [5] [6] [7] [8] [9]
- ISS RESIZER Register Summary: [10]

Table 8-492. RSZ_YUV_Y_MIN

Address Offset	0x0000 0060		
Physical Address	0x5201 0460	**Instance**	ISS_RESIZER
Description	LUMINANCE SATURATION REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								MIN							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED		R	0x000000
7:0	MIN	The minimum value of Luminance (8bits unsigned). If the value of the Luminance is smaller than VAL, it will be clipped to VAL. This bit field must be set to its default values when the resizer is set in pass-though mode.	RW	0x00

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Table 8-493. Register Call Summary for Register RSZ_YUV_Y_MIN

ISS ISP
- ISS ISP RSZ Functional Description: [0] [1]
- ISS ISP RSZ Engines Interframe Image Processing Settings: [2]
- ISS RESIZER Register Summary: [3]

Table 8-494. RSZ_YUV_Y_MAX

Address Offset	0x0000 0064		
Physical Address	0x5201 0464	**Instance**	ISS_RESIZER
Description	LUMINANCE SATURATION REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								MAX							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED		R	0x000000
7:0	MAX	The maximum value of Luminance (8bits unsigned). If the value of the Luminance is larger than VAL, it will be clipped to VAL. This bit field must be set to its default values when the resizer is set in pass-through mode.	RW	0xFF

Table 8-495. Register Call Summary for Register RSZ_YUV_Y_MAX

ISS ISP
- ISS ISP RSZ Functional Description: [0] [1]
- ISS ISP RSZ Engines Interframe Image Processing Settings: [2]
- ISS RESIZER Register Summary: [3]

Table 8-496. RSZ_YUV_C_MIN

Address Offset	0x0000 0068		
Physical Address	0x5201 0468	**Instance**	ISS_RESIZER
Description	CHROMINANCE SATURATION REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								MIN							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED		R	0x000000
7:0	MIN	The minimum value of Chrominance (8bits unsigned). If the value of the Chrominance is smaller than VAL, it will be clipped to VAL. This bit field must be set to its default values when the resizer is set in pass-though mode.	RW	0x00

Table 8-497. Register Call Summary for Register RSZ_YUV_C_MIN

ISS ISP
- ISS ISP RSZ Functional Description: [0] [1]
- ISS ISP RSZ Engines Interframe Image Processing Settings: [2]
- ISS RESIZER Register Summary: [3]

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Table 8-498. RSZ_YUV_C_MAX

Address Offset	0x0000 006C		
Physical Address	0x5201 046C	**Instance**	ISS_RESIZER
Description	CHROMINANCE SATURATION REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								MAX							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED		R	0x000000
7:0	MAX	The maximum value of Chrominance (8bits unsigned). If the value of the Chrominance is larger than VAL, it will be clipped to VAL. This bit field must be set to its default values when the resizer is set in pass-through mode.	RW	0xFF

Table 8-499. Register Call Summary for Register RSZ_YUV_C_MAX

ISS ISP

- ISS ISP RSZ Functional Description: [0] [1]
- ISS ISP RSZ Engines Interframe Image Processing Settings: [2]
- ISS RESIZER Register Summary: [3]

Table 8-500. RSZ_YUV_PHS

Address Offset	0x0000 0070		
Physical Address	0x5201 0470	**Instance**	ISS_RESIZER
Description	The phase position of the output of the Chrominance		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															POS

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	POS	The phase position of the output of the chrominance. The RESIZER module does not change the relative position of the chroma samples vs. the luma samples between the input and output and the chroma position at the output of the IPIPE module and at the output of the RESIZER module must be identical. In other words, we must have RSZ_YUV_PHS.POS = IPIPE_YUV_PHS.POS. 0x0: Same position with Luminance: cosited 0x1: The middle of the luminance: centered	RW	0

Table 8-501. Register Call Summary for Register RSZ_YUV_PHS

ISS ISP

- ISS ISP RSZ Functional Description: [0] [1]
- ISS ISP RSZ Engines Interframe Image Processing Settings: [2]
- ISS RESIZER Register Summary: [3]
- ISS RESIZER Register Description: [4]
- ISS IPIPE Register Description: [5]

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Table 8-502. RSZ_SEQ

Address Offset	0x0000 0074		
Physical Address	0x5201 0474	**Instance**	ISS_RESIZER
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																											CRV	VRVB	HRVB	VRVA	HRVA

Bits	Field Name	Description	Type	Reset
31:5	RESERVED		R	0x0000000
4	CRV	Chroma sampling point change 0x0: Chroma sampling point is not changed 0x1: Chroma sampling point is changed from odd-numbered pixels to even-number pixels. The pixel at the left end is removed and the pixel at the right end is duplicated.	RW	0
3	VRVB	Resizer B - Vertical reversal of output image 0x0: Processed pixels are output in the order of input (normal operation) in vertical direction. 0x1: The order of output data is flipped top to bottom.	RW	0
2	HRVB	Resizer B -Horizontal reversal of output image 0x0: Processed pixels are output in the order of input (normal operation) in horizontal direction. 0x1: The order of output data is flipped left to right.	RW	0
1	VRVA	Resizer A - Vertical reversal of output image 0x0: Processed pixels are output in the order of input (normal operation) in vertical direction. 0x1: The order of output data is flipped top to bottom.	RW	0
0	HRVA	Resizer A - Horizontal reversal of output image 0x0: Processed pixels are output in the order of input (normal operation) in horizontal direction. 0x1: The order of output data is flipped left to right.	RW	0

Table 8-503. Register Call Summary for Register RSZ_SEQ

ISS ISP

- ISS ISP RSZ Functional Description: [0] [1]
- ISS ISP RSZ Global Image Processing Settings: [2] [3] [4] [5] [6] [7]
- ISS RESIZER Register Summary: [8]

Table 8-504. RZA_EN

Address Offset	0x0000 0078		
Physical Address	0x5201 0478	**Instance**	ISS_RESIZER
Description	RESIZER A - ENABLE REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															EN

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Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	EN	Enable resizer #A This bit is latched on video port VD input. The reason is that the resizer must only starts the processing on a clean frame boundary. In one-shot mode, this bit is negated on VD. 0x0: Disable 0x1: Enable	RW	0

Table 8-505. Register Call Summary for Register RZA_EN

ISS ISP

- ISS ISP RSZ Functional Description: [0] [1] [2] [3] [4]
- ISS ISP RSZ Hardware Setup/Initialization: [5]
- ISS RESIZER Register Summary: [6]

Table 8-506. RZA_MODE

Address Offset	0x0000 007C		
Physical Address	0x5201 047C	**Instance**	ISS_RESIZER
Description	RESIZER #A MODE REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															MODE

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	MODE	Select "Free Run mode" or "One Shot Mode" 0x0: Free run 0x1: One shot	RW	0

Table 8-507. Register Call Summary for Register RZA_MODE

ISS ISP

- ISS ISP RSZ Engines Interframe Image Processing Settings: [0] [1]
- ISS RESIZER Register Summary: [2]

Table 8-508. RZA_420

Address Offset	0x0000 0080		
Physical Address	0x5201 0480	**Instance**	ISS_RESIZER
Description	YEN/CEN: 0/0: in = YUV4:2:2 input, out = YUV4:2:2 output 0/1: in = YUV4:2:2 input, out = Chrominance of YUV4:2:0 output 1/0: in = YUV4:2:2 input, out = Luminance of YUV4:2:0 output 1/1: in = YUV4:2:2 input, out = YUV4:2:0 output		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														CEN	YEN

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Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	CEN	Output Enable for Chrominance This bit is valid in 422 input mode. When CEN=0 and YEN=0, output is 422 0x0: C output disable 0x1: C output enable and 422to420 conversion enabled	RW	0
0	YEN	Output Enable for Luminance. This bit is valid in 422 input mode. When CEN=0 and YEN=0, output is 422 0x0: Y output disable 0x1: Y output enable and 422to420 conversion enabled	RW	0

Table 8-509. Register Call Summary for Register RZA_420

ISS ISP

- ISS ISP RSZ Global Image Processing Settings: [0] [1] [2] [3]
- ISS ISP RSZ Engines Interframe Image Processing Settings: [4] [5] [6] [7] [8] [9]
- ISS RESIZER Register Summary: [10]
- ISS RESIZER Register Description: [11] [12]

Table 8-510. RZA_I_VPS

Address Offset	0x0000 0084		
Physical Address	0x5201 0484	**Instance**	ISS_RESIZER
Description	RESIZER A - INPUT VERTICAL START REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																VPS															

Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000
12:0	VPS	Input Vertical Position Sets the vertical start position of the input image within the global frame. It enables to crop data into the global frame. After SRC_VPS, the Vps'th line is processed as the first line in each image.	RW	0x0000

Table 8-511. Register Call Summary for Register RZA_I_VPS

ISS ISP

- ISS ISP RSZ Engines Interframe Image Processing Settings: [0]
- ISS RESIZER Register Summary: [1]

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Table 8-512. RZA_I_HPS

Address Offset	0x0000 0088		
Physical Address	0x5201 0488	**Instance**	ISS_RESIZER
Description	RESIZER A - INPUT HORIZONTAL START REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								HPS							

Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000
12:0	HPS	Input Horizontal Position Sets the horizontal position of the first pixel for each line within the global frame. After SRC_HPS, the pixel at the VAL'th position is processed as the first pixel. This value must be even.	RW	0x0000

Table 8-513. Register Call Summary for Register RZA_I_HPS

ISS ISP

- ISS ISP RSZ Engines Interframe Image Processing Settings: [0]
- ISS RESIZER Register Summary: [1]

Table 8-514. RZA_O_VSZ

Address Offset	0x0000 008C		
Physical Address	0x5201 048C	**Instance**	ISS_RESIZER
Description	RESIZER A - OUTPUT VERTICAL SIZER REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								VSZ							

Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000
12:0	VSZ	The target output size of the resized image. The number of output lines is (VSZ+1). Set 479, when 480 lines of output is required.	RW	0x0000

Table 8-515. Register Call Summary for Register RZA_O_VSZ

ISS ISP

- ISS ISP RSZ Engines Interframe Image Processing Settings: [0]
- ISS RESIZER Register Summary: [1]

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Table 8-516. RZA_O_HSZ

Address Offset	0x0000 0090		
Physical Address	0x5201 0490	**Instance**	ISS_RESIZER
Description	RESIZER A - OUTPUT HORIZONTAL SIZE REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								HSZ							HSZ_LSB

Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000
12:1	HSZ	The horizontal size of output image. The number of pixel in each line is (HSZ+1). Set 479, when 480 pixels are required. This value must be lower than the max memory line size supported by the resizer engine, except in RAW pass through mode. Note that the LSB of the 13-bit HSZ value is fixed to 1 such that the horizontal size is always even.	RW	0x000
0	HSZ_LSB	The least significant bit of HSZ is forced to 1.	R	1

Table 8-517. Register Call Summary for Register RZA_O_HSZ

ISS ISP

- ISS ISP RSZ Engines Interframe Image Processing Settings: [0]
- ISS RESIZER Register Summary: [1]

Table 8-518. RZA_V_PHS_Y

Address Offset	0x0000 0094		
Physical Address	0x5201 0494	**Instance**	ISS_RESIZER
Description	RESIZER A - INITIAL LUMINANCE PHASE OF VERTICAL RESIZING PROCESS When YUV4:2:2 data are output, the phase values for luma and chroma should typically be equal, that is, RZX_V_PHS_Y= RZX_V_PHS_C. The following constraints apply when setting the initial vertical phases ABS(RZX_V_PHS_Y - RZX_V_PHS_C) RZX_V_DIF. This constraint means that at most the distance between the initial phases for luminance and chrominance is not expected to exceed the distance between two luma pixels. Note that the absolute value is used, hence, the initial luma phase can be greater than the initial chroma phase or the other way around. As a reminder, the distance between two output pixels for luma is given by RZX_V_DIF.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																Y															

Bits	Field Name	Description	Type	Reset
31:14	RESERVED		R	0x00000
13:0	Y	The initial value for the luma phase in vertical resizing process. This value is in U14Q8 fractional format.	RW	0x0000

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Table 8-519. Register Call Summary for Register RZA_V_PHS_Y

ISS ISP

- ISS ISP RSZ Engines Interframe Image Processing Settings: [0] [1]
- ISS RESIZER Register Summary: [2]

Table 8-520. RZA_V_PHS_C

Address Offset	0x0000 0098		
Physical Address	0x5201 0498	**Instance**	ISS_RESIZER
Description	RESIZER A - INITIAL CHROMINANCE PHASE OF VERTICAL RESIZING PROCESS When YUV4:2:2 data are output, the phase values for luma and chroma should typically be equal, that is, RZX_V_PHS_Y= RZX_V_PHS_C. The following constraints apply when setting the initial vertical phases ABS(RZX_V_PHS_Y - RZX_V_PHS_C) RZX_V_DIF. This constraint means that at most the distance between the initial phases for luminance and chrominance is not expected to exceed the distance between two luma pixels. Note that the absolute value is used, hence, the initial luma phase can be greater than the initial chroma phase or the other way around. As a reminder, the distance between two output pixels for luma is given by RZX_V_DIF.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								C							

Bits	Field Name	Description	Type	Reset
31:14	RESERVED		R	0x00000
13:0	C	The initial value for the chroma phase in vertical resizing process. This value is in U14Q8 fractional format.	RW	0x0000

Table 8-521. Register Call Summary for Register RZA_V_PHS_C

ISS ISP

- ISS ISP RSZ Engines Interframe Image Processing Settings: [0] [1]
- ISS RESIZER Register Summary: [2]

Table 8-522. RZA_V_DIF

Address Offset	0x0000 009C		
Physical Address	0x5201 049C	**Instance**	ISS_RESIZER
Description	RESIZER A - VERTICAL RESIZER REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								V							

Bits	Field Name	Description	Type	Reset
31:14	RESERVED		R	0x00000
13:0	V	The parameter for vertical resize. The actual resizing ratio is 256/RZA_V_DIF. In normal mode: 16 = RZA_V_DIF = 4096. In down-scale mode: 256 = RZA_V_DIF = 4096.	RW	0x0000

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Table 8-523. Register Call Summary for Register RZA_V_DIF

ISS ISP

- ISS ISP RSZ Engines Interframe Image Processing Settings: [0]
- ISS RESIZER Register Summary: [1]
- ISS RESIZER Register Description: [2] [3] [4]

Table 8-524. RZA_V_TYP

Address Offset	0x0000 00A0		
Physical Address	0x5201 04A0	**Instance**	ISS_RESIZER
Description	RESIZER A - INTERPOLATION METHOD FOR VERTICAL RESIZING		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														C	Y

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	C	Selection of resizing method for chrominance: vertical 0x0: 4-tap cubic convolution (default) 0x1: 2-tap linear interpolation	RW	0
0	Y	Selection of resizing method for luminance: vertical 0x0: 4-tap cubic convolution (default) 0x1: 2-tap linear interpolation	RW	0

Table 8-525. Register Call Summary for Register RZA_V_TYP

ISS ISP

- ISS ISP RSZ Engines Interframe Image Processing Settings: [0] [1]
- ISS RESIZER Register Summary: [2]

Table 8-526. RZA_V_LPF

Address Offset	0x0000 00A4		
Physical Address	0x5201 04A4	**Instance**	ISS_RESIZER
Description	RESIZER A - VERTICAL LPF INTENSITY REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				C								Y			

Bits	Field Name	Description	Type	Reset
31:12	RESERVED		R	0x00000
11:6	C	The intensity parameter for chroma vertical low pass filtering.	RW	0x00
5:0	Y	The intensity parameter for luma vertical low pass filtering.	RW	0x00

Table 8-527. Register Call Summary for Register RZA_V_LPF

ISS ISP

- ISS ISP RSZ Engines Interframe Image Processing Settings: [0] [1]
- ISS RESIZER Register Summary: [2]

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Table 8-528. RZA_H_PHS

Address Offset	0x0000 00A8		
Physical Address	0x5201 04A8	**Instance**	ISS_RESIZER
Description	RESIZER A - INITIAL PHASE OF HORIZONTAL RESIZING PROCESS		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								PHS							

Bits	Field Name	Description	Type	Reset
31:14	RESERVED		R	0x00000
13:0	PHS	Initial value for the phase in horizontal resizing process, that is, the sampling position is shifted. This value is in U14Q8 fractional format. Example: If RZX_H_PHS = 128, the first output pixel is sampled at the center of the first two valid input pixels. If RZX_I_HPS=100 and RZX_H_PHS=128, the first output pixel is resampled at the center of the 100-th and the 101-st input pixels.	RW	0x0000

Table 8-529. Register Call Summary for Register RZA_H_PHS

ISS ISP

- ISS ISP RSZ Engines Interframe Image Processing Settings: [0]
- ISS RESIZER Register Summary: [1]

Table 8-530. RZA_H_PHS_ADJ

Address Offset	0x0000 00AC		
Physical Address	0x5201 04AC	**Instance**	ISS_RESIZER
Description	RESIZER A - LUMINANCE HORIZONTAL PHASE ADJUSTMENT The RZA_H_PHS_ADJ register enables to adjust the horizontal phase for the luma component when averaging is enabled (the horizontal averaging disrupts the relative sampling point between luminance and chrominance when YUV4:2:2 cosited data is input), that is, the relative phase between luma and chroma is different before and after the horizontal averager.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								ADJ							

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8:0	ADJ	Horizontal phase adjustment value. This value is in U9Q8 fractional format. This value is expected to be equal to zero if the averager is disabled or if input chroma is centered.	RW	0x000

Table 8-531. Register Call Summary for Register RZA_H_PHS_ADJ

ISS ISP

- ISS ISP RSZ Engines Interframe Image Processing Settings: [0]
- ISS RESIZER Register Summary: [1]
- ISS RESIZER Register Description: [2] [3]
- ISS IPIPE Register Description: [4]

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Table 8-532. RZA_H_DIF

Address Offset	0x0000 00B0		
Physical Address	0x5201 04B0	**Instance**	ISS_RESIZER
Description	RESIZER A - HORIZONTAL RESIZER REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								H							

Bits	Field Name	Description	Type	Reset
31:14	RESERVED		R	0x00000
13:0	H	The parameter for horizontal resizing process. The actual resizing ratio is 256/VAL. In normal mode 16= RSZ_RZA_H_DIF=4096 In down-scale mode 256=RSZ_RZA_H_DIF=4096	RW	0x0000

Table 8-533. Register Call Summary for Register RZA_H_DIF

ISS ISP

- ISS ISP RSZ Engines Interframe Image Processing Settings: [0]
- ISS RESIZER Register Summary: [1]
- ISS RESIZER Register Description: [2] [3] [4] [5]

Table 8-534. RZA_H_TYP

Address Offset	0x0000 00B4		
Physical Address	0x5201 04B4	**Instance**	ISS_RESIZER
Description	Resize-A		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														C	Y

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	C	Selection of resizing method for chrominance: horizontal 0x0: 4-tap cubic convolution (default) 0x1: 2-tap linear interpolation	RW	0
0	Y	Selection of resizing method for luminance: horizontal 0x0: 4-tap cubic convolution (default) 0x1: 2-tap linear interpolation	RW	0

Table 8-535. Register Call Summary for Register RZA_H_TYP

ISS ISP

- ISS ISP RSZ Engines Interframe Image Processing Settings: [0] [1]
- ISS RESIZER Register Summary: [2]

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Table 8-536. RZA_H_LPF

Address Offset	0x0000 00B8		
Physical Address	0x5201 04B8	**Instance**	ISS_RESIZER
Description	RESIZER A - HORIZONTAL LPF INTENSITY REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				C				Y							

Bits	Field Name	Description	Type	Reset
31:12	RESERVED		R	0x00000
11:6	C	Horizontal LPF Intensity for Chrominance	RW	0x00
5:0	Y	Selection of resizing method for Luminance in horizontal direction	RW	0x00

Table 8-537. Register Call Summary for Register RZA_H_LPF

ISS ISP

- ISS ISP RSZ Engines Interframe Image Processing Settings: [0] [1]
- ISS RESIZER Register Summary: [2]

Table 8-538. RZA_DWN_EN

Address Offset	0x0000 00BC		
Physical Address	0x5201 04BC	**Instance**	ISS_RESIZER
Description	RESIZER #A - DOWNSCALE ENABLE REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															DWN_EN

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	DWN_EN	Resizer downscale enable 0x0: Off. Normal operation: upscale and downscale are allowed. 0x1: On. Downscale mode.	RW	0

Table 8-539. Register Call Summary for Register RZA_DWN_EN

ISS ISP

- ISS ISP RSZ Engines Interframe Image Processing Settings: [0]
- ISS RESIZER Register Summary: [1]

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Table 8-540. RZA_DWN_AV

Address Offset	0x0000 00C0		
Physical Address	0x5201 04C0	**Instance**	ISS_RESIZER
Description	Resize-A		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																										V			H		

Bits	Field Name	Description	Type	Reset
31:6	RESERVED		R	0x0000000
5:3	V	Vertical averaging size : $1/2^{(VWT+1)}$ The range goes from 1/2 to 1/256 in power of two. 0:_DIV2 1/2 down scale 1:_DIV4 1/4 down scale 2:_DIV8 1/8 down scale 3:_DIV16 1/16 down scale 4:_DIV32 1/32 down scale 5:_DIV64 1/64 down scale 6:_DIV128 1/128 down scale 7:_DIV256 1/256 down scale	RW	0x0
2:0	H	Horizontal averaging size : $1/2^{(HWT+1)}$ The range goes from 1/2 to 1/256 in power of two. 0:_DIV2 1/2 down scale 1:_DIV4 1/4 down scale 2:_DIV8 1/8 down scale 3:_DIV16 1/16 down scale 4:_DIV32 1/32 down scale 5:_DIV64 1/64 down scale 6:_DIV128 1/128 down scale 7:_DIV256 1/256 down scale	RW	0x0

Table 8-541. Register Call Summary for Register RZA_DWN_AV

ISS ISP

- ISS ISP RSZ Functional Description: [0] [1]
- ISS ISP RSZ Engines Interframe Image Processing Settings: [2] [3]
- ISS RESIZER Register Summary: [4]

Table 8-542. RZA_RGB_EN

Address Offset	0x0000 00C4		
Physical Address	0x5201 04C4	**Instance**	ISS_RESIZER
Description	RESIZER #A - RGB OUTPUT ENABLE		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															RGB_EN

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Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	RGB_EN	Enable of RGB output In pass through mode, this register must be 0. This bit can only be set to 1 when YUV4:2:2 data are output. YUV4:2:2 data output is selected when SRC_FMT1.IN420 = 0 and RZA_420.YEN = RZA_420.CEN = 0 0x0: Off (YCbCr output) 0x1: On (RGB output)	RW	0

Table 8-543. Register Call Summary for Register RZA_RGB_EN

ISS ISP

- ISS ISP RSZ Engines Interframe Image Processing Settings: [0]
- ISS RESIZER Register Summary: [1]

Table 8-544. RZA_RGB_TYP

Address Offset	0x0000 00C8		
Physical Address	0x5201 04C8	**Instance**	ISS_RESIZER
Description	RESIZER A - RGB OUTPUT CONTROL REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													MSK1	MSK0	TYP

Bits	Field Name	Description	Type	Reset
31:3	RESERVED		R	0x0000 0000
2	MSK1	Enables masking of the last 2 pixels This bit is used to mask the 2 last pixels at the image boundary which are affected by the YUV4:2:2 to YUV4:4:4 conversion. 0x0: output the last 2 pixels 0x1: mask the last 2 pixels (Resizer do not output them.)	RW	0
1	MSK0	Enables masking of the first 2 pixels This bit is used to mask the 2 first pixels at the image boundary which are affected by the YUV4:2:2 to YUV4:4:4 conversion. 0x0: output the first 2 pixels 0x1: mask the first 2 pixels (Resizer do not output them.)	RW	0
0	TYP	16bit/32bit output selection 0x0: 32-bit output: alpha + R + G + B (8 bit each) This mode comes with performance degradation. The maximum input frequency in this mode is 160 MHz. This due to the fact that the output is 4 bytes / pixel. 0x1: 16-bit output: R(5 bit) + G (6 bit) + B (5 bit)	RW	0

Table 8-545. Register Call Summary for Register RZA_RGB_TYP

ISS ISP

- ISS ISP RSZ Engines Interframe Image Processing Settings: [0] [1] [2]
- ISS RESIZER Register Summary: [3]

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Table 8-546. RZA_RGB_BLD

Address Offset	0x0000 00CC		
Physical Address	0x5201 04CC	**Instance**	ISS_RESIZER
Description	RESIZER A - RGB BLEND REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								BLD							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED		R	0x000000
7:0	BLD	The alpha value used in 32-bit RGBA output mode	RW	0x00

Table 8-547. Register Call Summary for Register RZA_RGB_BLD

ISS ISP

- ISS ISP RSZ Engines Interframe Image Processing Settings: [0]
- ISS RESIZER Register Summary: [1]

Table 8-548. RZA_SDR_Y_BAD_H

Address Offset	0x0000 00D0		
Physical Address	0x5201 04D0	**Instance**	ISS_RESIZER
Description	RESIZER A - OUTPUT MEMORY BASE ADDRESS REGISTER (HIGH) This register is used if the output data format is one of the following: RAW, YUV4:2:2, YUV4:2:0, RGB5:6:5, RGBA. RAW: RAW data is written to this address YUV4:2:2: YUV data is written to this address YUV4:2:0: Y data is written to this address RGB5:6:5: 16-bit RGB data is written to this address RGBA: 32-bit RGBA data is written to this address		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																Y_BAD_H															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:0	Y_BAD_H	Memory Base Address Sets the 16 upper bits of the 32-bit base address of the circular buffer in memory.	RW	0x0000

Table 8-549. Register Call Summary for Register RZA_SDR_Y_BAD_H

ISS ISP

- ISS ISP RSZ Functional Description: [0]
- ISS ISP RSZ Global Image Processing Settings: [1]
- ISS RESIZER Register Summary: [2]

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Table 8-550. RZA_SDR_Y_BAD_L

Address Offset	0x0000 00D4		
Physical Address	0x5201 04D4	**Instance**	ISS_RESIZER
Description	RESIZER A - OUTPUT MEMORY BASE ADDRESS REGISTER (LOW) This register is used if the output data format is one of the following: RAW, YUV4:2:2, YUV4:2:0, RGB5:6:5, RGBA. RAW: RAW data is written to this address YUV4:2:2: YUV data is written to this address YUV4:2:0: Y data is written to this address RGB5:6:5: 16-bit RGB data is written to this address RGBA: 32-bit RGBA data is written to this address		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																Y_BAD_L															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:0	Y_BAD_L	Memory Base Address Sets the 16 lower bits of the 32-bit base address of the circular buffer in memory. It is a byte address. YUV4:2:0 format (output data on 8 bits): The two least significant bits must be set to 00 when horizontal reversal mode is off. The two least significant bits must be set to 11 when horizontal reversal mode is on. RAW, RGB5:6:5 and YUV4:2:2 formats (output data on 16 bits): The two least significant bits must be set to 00 when horizontal reversal mode is off. The two least significant bits must be set to 11 when horizontal reversal mode is on. RGBA format (output data on 32 bits): The three least significant bits must be set to "000" when horizontal reversal mode is off. The three least significant bits must be set to "111" when horizontal reversal mode is on.	RW	0x0000

Table 8-551. Register Call Summary for Register RZA_SDR_Y_BAD_L

ISS ISP

- ISS ISP RSZ Functional Description: [0]
- ISS ISP RSZ Global Image Processing Settings: [1]
- ISS RESIZER Register Summary: [2]

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Table 8-552. RZA_SDR_Y_SAD_H

Address Offset	0x0000 00D8		
Physical Address	0x5201 04D8	**Instance**	ISS_RESIZER
Description	RESIZER A - OUTPUT MEMORY START ADDRESS REGISTER (HIGH) This register is used if the output data format is one of the following: RAW, YUV4:2:2, YUV4:2:0, RGB5:6:5, RGBA. RAW: RAW data is written to this address YUV4:2:2: YUV data is written to this address YUV4:2:0: Y data is written to this address RGB5:6:5: 16-bit RGB data is written to this address RGBA: 32-bit RGBA data is written to this address		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																Y_SAD_H															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:0	Y_SAD_H	Memory Start Address Sets the 16 upper bits of the 32-bit start address in memory.	RW	0x0000

Table 8-553. Register Call Summary for Register RZA_SDR_Y_SAD_H

ISS ISP

- ISS ISP RSZ Functional Description: [0]
- ISS ISP RSZ Global Image Processing Settings: [1]
- ISS RESIZER Register Summary: [2]

Table 8-554. RZA_SDR_Y_SAD_L

Address Offset	0x0000 00DC		
Physical Address	0x5201 04DC	**Instance**	ISS_RESIZER
Description	RESIZER A - OUTPUT MEMORY START ADDRESS REGISTER (LOW) This register is used if the output data format is one of the following: RAW, YUV4:2:2, YUV4:2:0, RGB5:6:5, RGBA. RAW: RAW data is written to this address YUV4:2:2: YUV data is written to this address YUV4:2:0: Y data is written to this address RGB5:6:5: 16-bit RGB data is written to this address RGBA: 32-bit RGBA data is written to this address		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																Y_SAD_L															

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Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:0	Y_SAD_L	Memory Start Address Sets 16 lower bits of the 32-bit start address in memory. It is a byte address. For every frame, the first line of data will be written to this address. We have: SAD = BAD + (PTR_S x OFT) and PTR_S PTR_E If the first line must be written at the beginning of the circular buffer memory then SAD = BAD and PTR_S = 0. YUV4:2:0 format (output data on 8 bits): The two least significant bits must be set to 00 when horizontal reversal mode is off. The two least significant bits must be set to 11 when horizontal reversal mode is on. RAW, RGB5:6:5 and YUV4:2:2 formats (output data on 16 bits): The two least significant bits must be set to 00 when horizontal reversal mode is off. The two least significant bits must be set to 11 when horizontal reversal mode is on. RGBA format (output data on 32 bits): The three least significant bits must be set to "000" when horizontal reversal mode is off. The three least significant bits must be set to "111" when horizontal reversal mode is on.	RW	0x0000

Table 8-555. Register Call Summary for Register RZA_SDR_Y_SAD_L

ISS ISP

- ISS ISP RSZ Functional Description: [0]
- ISS ISP RSZ Global Image Processing Settings: [1] [2]
- ISS RESIZER Register Summary: [3]

Table 8-556. RZA_SDR_Y_OFT

Address Offset	0x0000 00E0		
Physical Address	0x5201 04E0	**Instance**	ISS_RESIZER
Description	RESIZER A - OUTPUT MEMORY OFFSET REGISTER This register is used if the output data format is one of the following: RAW, YUV4:2:2, YUV4:2:0 or RGBA.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																Y_OFT															

Bits	Field Name	Description	Type	Reset
31:17	RESERVED		R	0x0000
16:0	Y_OFT	Memory Line Offset Sets the size of each line in the circular buffer. It is expressed in bytes and unsigned. Note that OFT does not necessary corresponds to the size of a line in a frame, it can be much bigger. The line offset must be a multiple of 128 bytes (bits [6:0] of RZX_SDR_Y_OFT and RZX_SDR_C_OFT must be set to 0). Example: line 0 address = SAD line 1 address = SAD + 1 x OFT line 2 address = SAD + 2 x OFT	RW	0x00000

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Table 8-557. Register Call Summary for Register RZA_SDR_Y_OFT

ISS ISP

- ISS ISP RSZ Functional Description: [0]
- ISS ISP RSZ Global Image Processing Settings: [1]
- ISS RESIZER Register Summary: [2]

Table 8-558. RZA_SDR_Y_PTR_S

Address Offset	0x0000 00E4		
Physical Address	0x5201 04E4	**Instance**	ISS_RESIZER
Description	RESIZER A - OUTPUT MEMORY START ADDRESS REGISTER This register is used if the output data format is one of the following: RAW, YUV4:2:2, YUV4:2:0 or RGBA.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								Y_PTR_S							

Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000
12:0	Y_PTR_S	Start Line of Memory Pointer Sets the vertical position of the first output line in the output memory space. This value is expressed in number of lines. The hardware uses it to set up the initial value of the circular buffer. It must be set up such as PTR_S = (SAD - BAD) / OFT. This value must be set to 0 when RSZ_RZA_SDR_Y_BAD = RSZ_RZA_SDR_Y_SAD.	RW	0x0000

Table 8-559. Register Call Summary for Register RZA_SDR_Y_PTR_S

ISS ISP

- ISS ISP RSZ Functional Description: [0]
- ISS ISP RSZ Global Image Processing Settings: [1]
- ISS RESIZER Register Summary: [2]

Table 8-560. RZA_SDR_Y_PTR_E

Address Offset	0x0000 00E8		
Physical Address	0x5201 04E8	**Instance**	ISS_RESIZER
Description	RESIZER A - OUTPUT MEMORY END ADDRESS REGISTER This register is used if the output data format is one of the following: RAW, YUV4:2:2, YUV4:2:0 or RGBA.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								Y_PTR_E							

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Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000
12:0	Y_PTR_E	End Line of Memory Pointer Sets the maximum number of lines to be stored in the output memory space. This value is expressed in number of lines. When the number of output lines exceeds this value, the address restarts from the first address in the output memory space (BAD).	RW	0x0000

Table 8-561. Register Call Summary for Register RZA_SDR_Y_PTR_E

ISS ISP

- ISS ISP RSZ Functional Description: [0]
- ISS ISP RSZ Global Image Processing Settings: [1]
- ISS ISP5 SYS1 Register Description: [2] [3] [4] [5]
- ISS RESIZER Register Summary: [6]

Table 8-562. RZA_SDR_C_BAD_H

Address Offset	0x0000 00EC		
Physical Address	0x5201 04EC	**Instance**	ISS_RESIZER
Description	RESIZER A - OUTPUT MEMORY BASE ADDRESS REGISTER FOR CHROMA DATA (YUV4:2:0) This register is used if the output data format is YUV4:2:0. U and V data are written into this buffer.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																C_BAD_H															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:0	C_BAD_H	Memory Base Address Sets the 16 higher bits of the 32-bit base address of the circular buffer in memory.	RW	0x0000

Table 8-563. Register Call Summary for Register RZA_SDR_C_BAD_H

ISS ISP

- ISS ISP RSZ Functional Description: [0]
- ISS ISP RSZ Global Image Processing Settings: [1]
- ISS RESIZER Register Summary: [2]

Table 8-564. RZA_SDR_C_BAD_L

Address Offset	0x0000 00F0		
Physical Address	0x5201 04F0	**Instance**	ISS_RESIZER
Description	RESIZER A - OUTPUT MEMORY BASE ADDRESS REGISTER FOR CHROMA DATA (YUV4:2:0) This register is used if the output data format is YUV4:2:0. U and V data are written into this buffer.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																C_BAD_L															

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Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:0	C_BAD_L	Memory Base Address Sets the 16 lower bits of the 32-bit base address of the circular buffer in memory. It is a byte address. YUV4:2:0 format (output data on 8 bits): The two least significant bits must be set to 00 when horizontal reversal mode is off. The two least significant bits must be set to 11 when horizontal reversal mode is on.	RW	0x0000

Table 8-565. Register Call Summary for Register RZA_SDR_C_BAD_L

ISS ISP

- ISS ISP RSZ Functional Description: [0]
- ISS ISP RSZ Global Image Processing Settings: [1]
- ISS RESIZER Register Summary: [2]

Table 8-566. RZA_SDR_C_SAD_H

Address Offset	0x0000 00F4		
Physical Address	0x5201 04F4	**Instance**	ISS_RESIZER
Description	RESIZER A - OUTPUT MEMORY START ADDRESS REGISTER FOR CHROMA DATA (YUV4:2:0) This register is used if the output data format is YUV4:2:0. U and V data are written into this buffer.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																C_SAD_H															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:0	C_SAD_H	Memory Base Address Sets the 16 higher bits of the 32-bit start address in memory.	RW	0x0000

Table 8-567. Register Call Summary for Register RZA_SDR_C_SAD_H

ISS ISP

- ISS ISP RSZ Functional Description: [0]
- ISS ISP RSZ Global Image Processing Settings: [1]
- ISS RESIZER Register Summary: [2]

Table 8-568. RZA_SDR_C_SAD_L

Address Offset	0x0000 00F8		
Physical Address	0x5201 04F8	**Instance**	ISS_RESIZER
Description	RESIZER A - OUTPUT MEMORY START ADDRESS REGISTER FOR CHROMA DATA (YUV4:2:0) This register is used if the output data format is YUV4:2:0. U and V data are written into this buffer.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																C_SAD_L															

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Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:0	C_SAD_L	Memory Base Address Sets the 16 lower bits of the 32-bit start address in memory. It is a byte address. For every frame, the first line of data will be written to this address. We have: SAD = BAD + (PTR_S x OFT) and PTR_S PTR_E If the first line must be written at the beginning of the circular buffer memory then SAD = BAD and PTR_S = 0. YUV4:2:0 format (output data on 8 bits): The two least significant bits must be set to 00 when horizontal reversal mode is off. The two least significant bits must be set to 11 when horizontal reversal mode is on.	RW	0x0000

Table 8-569. Register Call Summary for Register RZA_SDR_C_SAD_L

ISS ISP

- ISS ISP RSZ Functional Description: [0]
- ISS ISP RSZ Global Image Processing Settings: [1] [2]
- ISS RESIZER Register Summary: [3]

Table 8-570. RZA_SDR_C_OFT

Address Offset	0x0000 00FC		
Physical Address	0x5201 04FC	**Instance**	ISS_RESIZER
Description	RESIZER A - OUTPUT MEMORY OFFSET REGISTER FOR CHROMA DATA (YUV4:2:0) This register is used if the output data format is YUV4:2:0		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																C_OFT															

Bits	Field Name	Description	Type	Reset
31:17	RESERVED		R	0x0000
16:0	C_OFT	Memory Line Offset Sets the size of each line in the circular buffer. It is expressed in bytes and unsigned. Note that OFT does not necessary corresponds to the size of a line in a frame, it can be much bigger. The line offset must be a multiple of 128 bytes (bits [6:0] of RZX_SDR_Y_OFT and RZX_SDR_C_OFT must be set to 0). Example: line 0 address = SAD line 1 address = SAD + 1 x OFT line 2 address = SAD + 2 x OFT	RW	0x00000

Table 8-571. Register Call Summary for Register RZA_SDR_C_OFT

ISS ISP

- ISS ISP RSZ Functional Description: [0]
- ISS ISP RSZ Global Image Processing Settings: [1]
- ISS RESIZER Register Summary: [2]

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Table 8-572. RZA_SDR_C_PTR_S

Address Offset	0x0000 0100		
Physical Address	0x5201 0500	**Instance**	ISS_RESIZER
Description	RESIZER A - OUTPUT MEMORY START ADDRESS REGISTER FOR CHROMA DATA (YUV4:2:0) This register is used if the output data format is YUV4:2:0		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								C_PTR_S							

Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000
12:0	C_PTR_S	Start Line of Memory Pointer Sets the vertical position of the first output line in the output memory space. This value is expressed in number of lines. The hardware uses it to set up the initial value of the circular buffer. It must be set up such as PTR_S = (SAD - BAD) / OFT. This value must be set to 0 when RSZ_RZA_SDR_C_BAD = RSZ_RZA_SDR_C_SAD.	RW	0x0000

Table 8-573. Register Call Summary for Register RZA_SDR_C_PTR_S

ISS ISP

- ISS ISP RSZ Functional Description: [0]
- ISS ISP RSZ Global Image Processing Settings: [1]
- ISS RESIZER Register Summary: [2]

Table 8-574. RZA_SDR_C_PTR_E

Address Offset	0x0000 0104		
Physical Address	0x5201 0504	**Instance**	ISS_RESIZER
Description	RESIZER A - OUTPUT MEMORY END ADDRESS REGISTER FOR CHROMA DATA (YUV4:2:0) This register is used if the output data format is YUV4:2:0		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								C_PTR_E							

Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000
12:0	C_PTR_E	End Line of Memory Pointer Sets the maximum number of lines to be stored in the output memory space. This value is expressed in number of lines. When the number of output lines exceeds this value, the address restarts from the first address in the output memory space (BAD).	RW	0x0000

Table 8-575. Register Call Summary for Register RZA_SDR_C_PTR_E

ISS ISP

- ISS ISP RSZ Functional Description: [0]
- ISS ISP RSZ Global Image Processing Settings: [1]
- ISS RESIZER Register Summary: [2]

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Table 8-576. RZB_EN

Address Offset	0x0000 0108		
Physical Address	0x5201 0508	**Instance**	ISS_RESIZER
Description	RESIZER B - ENABLE REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															EN

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	EN	Enable resizer #A This bit is latched on the video port VD input signal. The reason is that the resizer must only starts the processing on a clean frame boundary. In one-shot mode, this bit is negated on VD. 0x0: Disable 0x1: Enable	RW	0

Table 8-577. Register Call Summary for Register RZB_EN

ISS ISP

- ISS ISP RSZ Functional Description: [0] [1] [2] [3] [4]
- ISS ISP RSZ Hardware Setup/Initialization: [5]
- ISS RESIZER Register Summary: [6]

Table 8-578. RZB_MODE

Address Offset	0x0000 010C		
Physical Address	0x5201 050C	**Instance**	ISS_RESIZER
Description	RESIZER B MODE REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															MODE

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	MODE	Select "Free Run mode" or "One Shot Mode" 0x0: Free run 0x1: One shot	RW	0

Table 8-579. Register Call Summary for Register RZB_MODE

ISS ISP

- ISS ISP RSZ Engines Interframe Image Processing Settings: [0] [1]
- ISS RESIZER Register Summary: [2]

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Table 8-580. RZB_420

Address Offset	0x0000 0110		
Physical Address	0x5201 0510	**Instance**	ISS_RESIZER
Description	YEN/CEN: 0/0: in = YUV4:2:2 input, out = YUV4:2:2 output 0/1: in = YUV4:2:2 input, out = Chrominance of YUV4:2:0 output 1/0: in = YUV4:2:2 input, out = Luminance of YUV4:2:0 output 1/1: in = YUV4:2:2 input, out = YUV4:2:0 output		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														CEN	YEN

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	CEN	Output Enable for Chrominance This bit is valid in 422 input mode. When CEN=0 and YEN=0, output is 422 0x0: C output disable 0x1: C output enable and 422to420 conversion enabled	RW	0
0	YEN	Output Enable for Luminance. This bit is valid in 422 input mode. When CEN=0 and YEN=0, output is 422 0x0: Y output disable 0x1: Y output enable and 422to420 conversion enabled	RW	0

Table 8-581. Register Call Summary for Register RZB_420

ISS ISP

- ISS ISP RSZ Global Image Processing Settings: [0] [1] [2] [3]
- ISS ISP RSZ Engines Interframe Image Processing Settings: [4] [5]
- ISS RESIZER Register Summary: [6]
- ISS RESIZER Register Description: [7] [8]

Table 8-582. RZB_I_VPS

Address Offset	0x0000 0114		
Physical Address	0x5201 0514	**Instance**	ISS_RESIZER
Description	RESIZER B - INPUT VERTICAL START REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																VPS															

Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000
12:0	VPS	Input Vertical Position Sets the vertical start position of the input image within the global frame. It enables to crop data into the global frame. After SRC_VPS, the Vps'th line is processed as the first line in each image.	RW	0x0000

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Table 8-583. Register Call Summary for Register RZB_I_VPS

ISS ISP

- ISS ISP RSZ Engines Interframe Image Processing Settings: [0]
- ISS RESIZER Register Summary: [1]

Table 8-584. RZB_I_HPS

Address Offset	0x0000 0118		
Physical Address	0x5201 0518	**Instance**	ISS_RESIZER
Description	RESIZER B - INPUT HORIZONTAL START REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								HPS							

Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000
12:0	HPS	Input Horizontal Position Sets the horizontal position of the first pixel for each line within the global frame. After SRC_HPS, the pixel at the VAL'th position is processed as the first pixel. This value must be even.	RW	0x0000

Table 8-585. Register Call Summary for Register RZB_I_HPS

ISS ISP

- ISS ISP RSZ Engines Interframe Image Processing Settings: [0]
- ISS RESIZER Register Summary: [1]

Table 8-586. RZB_O_VSZ

Address Offset	0x0000 011C		
Physical Address	0x5201 051C	**Instance**	ISS_RESIZER
Description	RESIZER B - OUTPUT VERTICAL SIZER REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								VSZ							

Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000
12:0	VSZ	The target output size of the resized image. The number of output lines is (VSZ+1). Set 479, when 480 lines of output is required.	RW	0x0000

Table 8-587. Register Call Summary for Register RZB_O_VSZ

ISS ISP

- ISS ISP RSZ Engines Interframe Image Processing Settings: [0]
- ISS RESIZER Register Summary: [1]

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Table 8-588. RZB_O_HSZ

Address Offset	0x0000 0120		
Physical Address	0x5201 0520	**Instance**	ISS_RESIZER
Description	RESIZER B - OUTPUT HORIZONTAL SIZE REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																HSZ															HSZ_LSB

Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000
12:1	HSZ	The horizontal size of output image. The number of pixel in each line is (HSZ+1). Set 479, when 480 pixels are required. This value must be lower than the max memory line size supported by the resizer engine, except in RAW pass through mode. Note that the LSB of the 13-bit HSZ value is fixed to 1 such that the horizontal size is always even.	RW	0x000
0	HSZ_LSB	The least significant bit of HSZ is forced to 1.	R	1

Table 8-589. Register Call Summary for Register RZB_O_HSZ

ISS ISP

- ISS ISP RSZ Engines Interframe Image Processing Settings: [0]
- ISS RESIZER Register Summary: [1]

Table 8-590. RZB_V_PHS_Y

Address Offset	0x0000 0124		
Physical Address	0x5201 0524	**Instance**	ISS_RESIZER
Description	RESIZER B - INITIAL LUMINANCE PHASE OF VERTICAL RESIZING PROCESS When YUV4:2:2 data are output, the phase values for luma and chroma should typically be equal, that is, RZX_V_PHS_Y= RZX_V_PHS_C. The following constraints apply when setting the initial vertical phases ABS(RZX_V_PHS_Y - RZX_V_PHS_C) RZX_V_DIF. This constraint means that at most the distance between the initial phases for luminance and chrominance is not expected to exceed the distance between two luma pixels. Note that the absolute value is used, hence, the initial luma phase can be greater than the initial chroma phase or the other way around. As a reminder, the distance between two output pixels for luma is given by RZX_V_DIF.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																Y															

Bits	Field Name	Description	Type	Reset
31:14	RESERVED		R	0x00000
13:0	Y	The initial value for the luma phase in vertical resizing process. This value is in U14Q8 fractional format.	RW	0x0000

Table 8-591. Register Call Summary for Register RZB_V_PHS_Y

ISS ISP

- ISS RESIZER Register Summary: [0]

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Table 8-592. RZB_V_PHS_C

Address Offset	0x0000 0128		
Physical Address	0x5201 0528	**Instance**	ISS_RESIZER
Description	RESIZER B - INITIAL CHROMINANCE PHASE OF VERTICAL RESIZING PROCESS When YUV4:2:2 data are output, the phase values for luma and chroma should typically be equal, that is, RZX_V_PHS_Y= RZX_V_PHS_C. The following constraints apply when setting the initial vertical phases ABS(RZX_V_PHS_Y - RZX_V_PHS_C) RZX_V_DIF. This constraint means that at most the distance between the initial phases for luminance and chrominance is not expected to exceed the distance between two luma pixels. Note that the absolute value is used, hence, the initial luma phase can be greater than the initial chroma phase or the other way around. As a reminder, the distance between two output pixels for luma is given by RZX_V_DIF.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								C							

Bits	Field Name	Description	Type	Reset
31:14	RESERVED		R	0x00000
13:0	C	The initial value for the chroma phase in vertical resizing process. This value is in U14Q8 fractional format.	RW	0x0000

Table 8-593. Register Call Summary for Register RZB_V_PHS_C

ISS ISP

- ISS RESIZER Register Summary: [0]

Table 8-594. RZB_V_DIF

Address Offset	0x0000 012C		
Physical Address	0x5201 052C	**Instance**	ISS_RESIZER
Description	RESIZER B - VERTICAL RESIZER REGISTERR		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								V							

Bits	Field Name	Description	Type	Reset
31:14	RESERVED		R	0x00000
13:0	V	The parameter for vertical resize. The actual resizing ratio is 256/RZB_V_DIF. In normal mode: 16 = RZB_V_DIF = 4096. In down-scale mode: 256 = RZB_V_DIF = 4096.	RW	0x0000

Table 8-595. Register Call Summary for Register RZB_V_DIF

ISS ISP

- ISS ISP RSZ Engines Interframe Image Processing Settings: [0]
- ISS RESIZER Register Summary: [1]
- ISS RESIZER Register Description: [2] [3] [4]

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Table 8-596. RZB_V_TYP

Address Offset	0x0000 0130		
Physical Address	0x5201 0530	**Instance**	ISS_RESIZER
Description	RESIZER B - INTERPOLATION METHOD FOR VERTICAL RESIZING		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														C	Y

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	C	Selection of resizing method for chrominance: vertical 0x0: 4-tap cubic convolution (default) 0x1: 2-tap linear interpolation	RW	0
0	Y	Selection of resizing method for luminance: vertical 0x0: 4-tap cubic convolution (default) 0x1: 2-tap linear interpolation	RW	0

Table 8-597. Register Call Summary for Register RZB_V_TYP

ISS ISP

- ISS ISP RSZ Engines Interframe Image Processing Settings: [0] [1]
- ISS RESIZER Register Summary: [2]

Table 8-598. RZB_V_LPF

Address Offset	0x0000 0134		
Physical Address	0x5201 0534	**Instance**	ISS_RESIZER
Description	RESIZER B - VERTICAL LPF INTENSITY REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				C				Y							

Bits	Field Name	Description	Type	Reset
31:12	RESERVED		R	0x00000
11:6	C	The intensity parameter for chroma vertical low pass filtering.	RW	0x00
5:0	Y	The intensity parameter for luma vertical low pass filtering.	RW	0x00

Table 8-599. Register Call Summary for Register RZB_V_LPF

ISS ISP

- ISS ISP RSZ Engines Interframe Image Processing Settings: [0] [1]
- ISS RESIZER Register Summary: [2]

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Table 8-600. RZB_H_PHS

Address Offset	0x0000 0138		
Physical Address	0x5201 0538	**Instance**	ISS_RESIZER
Description	RESIZER B - INITIAL PHASE OF HORIZONTAL RESIZING PROCESS		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								PHS							

Bits	Field Name	Description	Type	Reset
31:14	RESERVED		R	0x00000
13:0	PHS	Initial value for the phase in horizontal resizing process, that is, the sampling position is shifted. This value is in U14Q8 fractional format. Example: If RZX_H_PHS = 128, the first output pixel is sampled at the center of the first two valid input pixels. If RZX_I_HPS=100 and RZX_H_PHS=128, the first output pixel is resampled at the center of the 100-th and the 101-st input pixels.	RW	0x0000

Table 8-601. Register Call Summary for Register RZB_H_PHS

ISS ISP

- ISS RESIZER Register Summary: [0]

Table 8-602. RZB_H_PHS_ADJ

Address Offset	0x0000 013C		
Physical Address	0x5201 053C	**Instance**	ISS_RESIZER
Description	RESIZER B - LUMINANCE HORIZONTAL PHASE ADJUSTMENT The RZA_H_PHS_ADJ register enables to adjust the horizontal phase for the luma component when averaging is enabled (the horizontal averaging disrupts the relative sampling point between luminance and chrominance when YUV4:2:2 cosited data is input), that is, the relative phase between luma and chroma is different before and after the horizontal averager.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								ADJ							

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8:0	ADJ	Horizontal phase adjustment value. This value is in U9Q8 fractional format. This value is expected to be equal to zero if the averager is disabled or if input chroma is centered.	RW	0x000

Table 8-603. Register Call Summary for Register RZB_H_PHS_ADJ

ISS ISP

- ISS RESIZER Register Summary: [0]
- ISS IPIPE Register Description: [1]

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Table 8-604. RZB_H_DIF

Address Offset	0x0000 0140		
Physical Address	0x5201 0540	**Instance**	ISS_RESIZER
Description	RESIZER B - HORIZONTAL RESIZER REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								H							

Bits	Field Name	Description	Type	Reset
31:14	RESERVED		R	0x00000
13:0	H	The parameter for horizontal resizing process. The actual resizing ratio is 256/VAL. In normal mode 16= RSZ_RZA_H_DIF=4096 In down-scale mode 256=RSZ_RZA_H_DIF=4096	RW	0x0000

Table 8-605. Register Call Summary for Register RZB_H_DIF

ISS ISP

- ISS ISP RSZ Engines Interframe Image Processing Settings: [0]
- ISS RESIZER Register Summary: [1]

Table 8-606. RZB_H_TYP

Address Offset	0x0000 0144		
Physical Address	0x5201 0544	**Instance**	ISS_RESIZER
Description	RESIZER B		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														C	Y

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	C	Selection of resizing method for chrominance: horizontal 0x0: 4-tap cubic convolution (default) 0x1: 2-tap linear interpolation	RW	0
0	Y	Selection of resizing method for luminance: horizontal 0x0: 4-tap cubic convolution (default) 0x1: 2-tap linear interpolation	RW	0

Table 8-607. Register Call Summary for Register RZB_H_TYP

ISS ISP

- ISS ISP RSZ Engines Interframe Image Processing Settings: [0] [1]
- ISS RESIZER Register Summary: [2]

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Table 8-608. RZB_H_LPF

Address Offset	0x0000 0148		
Physical Address	0x5201 0548	**Instance**	ISS_RESIZER
Description	RESIZER B - HORIZONTAL LPF INTENSITY REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				C				Y							

Bits	Field Name	Description	Type	Reset
31:12	RESERVED		R	0x00000
11:6	C	Horizontal LPF Intensity for Chrominance	RW	0x00
5:0	Y	Selection of resizing method for Luminance in horizontal direction	RW	0x00

Table 8-609. Register Call Summary for Register RZB_H_LPF

ISS ISP

- ISS ISP RSZ Engines Interframe Image Processing Settings: [0] [1]
- ISS RESIZER Register Summary: [2]

Table 8-610. RZB_DWN_EN

Address Offset	0x0000 014C		
Physical Address	0x5201 054C	**Instance**	ISS_RESIZER
Description	RESIZER B - DOWNSCALE ENABLE REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															DWN_EN

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	DWN_EN	Resizer downscale enable 0x0: Off. Normal operation: upscale and downscale are allowed. 0x1: On. Downscale mode.	RW	0

Table 8-611. Register Call Summary for Register RZB_DWN_EN

ISS ISP

- ISS RESIZER Register Summary: [0]

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Table 8-612. RZB_DWN_AV

Address Offset	0x0000 0150		
Physical Address	0x5201 0550	**Instance**	ISS_RESIZER
Description	RESIZER B		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																											V			H	

Bits	Field Name	Description	Type	Reset
31:6	RESERVED		R	0x0000000
5:3	V	Vertical averaging size : $1/2^{(VWT+1)}$ The range goes from 1/2 to 1/256 in power of two. 0:_DIV2 1/2 down scale 1:_DIV4 1/4 down scale 2:_DIV8 1/8 down scale 3:_DIV16 1/16 down scale 4:_DIV32 1/32 down scale 5:_DIV64 1/64 down scale 6:_DIV128 1/128 down scale 7:_DIV256 1/256 down scale	RW	0x0
2:0	H	Horizontal averaging size : $1/2^{(HWT+1)}$ The range goes from 1/2 to 1/256 in power of two. 0:_DIV2 1/2 down scale 1:_DIV4 1/4 down scale 2:_DIV8 1/8 down scale 3:_DIV16 1/16 down scale 4:_DIV32 1/32 down scale 5:_DIV64 1/64 down scale 6:_DIV128 1/128 down scale 7:_DIV256 1/256 down scale	RW	0x0

Table 8-613. Register Call Summary for Register RZB_DWN_AV

ISS ISP

- ISS RESIZER Register Summary: [0]

Table 8-614. RZB_RGB_EN

Address Offset	0x0000 0154		
Physical Address	0x5201 0554	**Instance**	ISS_RESIZER
Description	RESIZER B - RGB OUTPUT ENABLE		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															RGB_EN

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Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	RGB_EN	Enable of RGB output In pass through mode, this register must be 0. This bit can only be set to 1 when YUV4:2:2 data are output. YUV4:2:2 data output is selected when SRC_FMT1.IN420 = 0 and RZB_420.YEN = RZB_420.CEN = 0 0x0: Off (YCbCr output) 0x1: On (RGB output)	RW	0

Table 8-615. Register Call Summary for Register RZB_RGB_EN

ISS ISP

- ISS ISP RSZ Functional Description: [0]
- ISS RESIZER Register Summary: [1]

Table 8-616. RZB_RGB_TYP

Address Offset	0x0000 0158		
Physical Address	0x5201 0558	**Instance**	ISS_RESIZER
Description	RESIZER B - RGB OUTPUT CONTROL REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													MSK1	MSK0	TYP

Bits	Field Name	Description	Type	Reset
31:3	RESERVED		R	0x0000 0000
2	MSK1	Enables masking of the last 2 pixels This bit is used to mask the 2 last pixels at the image boundary which are affected by the YUV4:2:2 to YUV4:4:4 conversion. 0x0: output the last 2 pixels 0x1: mask the last 2 pixels (Resizer do not output them.)	RW	0
1	MSK0	Enables masking of the first 2 pixels This bit is used to mask the 2 first pixels at the image boundary which are affected by the YUV4:2:2 to YUV4:4:4 conversion. 0x0: output the first 2 pixels 0x1: mask the first 2 pixels (Resizer do not output them.)	RW	0
0	TYP	16bit/32bit output selection 0x0: 32-bit output: alpha + R + G + B (8 bit each) This mode comes with performance degradation. The maximum input frequency in this mode is 160 MHz. This due to the fact that the output is 4 bytes / pixel. 0x1: 16-bit output: R(5 bit) + G (6 bit) + B (5 bit)	RW	0

Table 8-617. Register Call Summary for Register RZB_RGB_TYP

ISS ISP

- ISS RESIZER Register Summary: [0]

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Table 8-618. RZB_RGB_BLD

Address Offset	0x0000 015C		
Physical Address	0x5201 055C	**Instance**	ISS_RESIZER
Description	RESIZER B - RGB BLEND REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								BLD							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED		R	0x000000
7:0	BLD	The alpha value used in 32-bit RGBA output mode	RW	0x00

Table 8-619. Register Call Summary for Register RZB_RGB_BLD

ISS ISP

- ISS RESIZER Register Summary: [0]

Table 8-620. RZB_SDR_Y_BAD_H

Address Offset	0x0000 0160		
Physical Address	0x5201 0560	**Instance**	ISS_RESIZER
Description	RESIZER B - OUTPUT MEMORY BASE ADDRESS REGISTER This register is used if the output data format is one of the following: RAW, YUV4:2:2, YUV4:2:0, RGB5:6:5, RGBA. RAW: RAW data is written to this address YUV4:2:2: YUV data is written to this address YUV4:2:0: Y data is written to this address RGB5:6:5: 16-bit RGB data is written to this address RGBA: 32-bit RGBA data is written to this address		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																Y_BAD_H															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:0	Y_BAD_H	Memory Base Address Sets 16 upper bits of the 32-bit base address of the circular buffer in memory.	RW	0x0000

Table 8-621. Register Call Summary for Register RZB_SDR_Y_BAD_H

ISS ISP

- ISS ISP RSZ Functional Description: [0]
- ISS ISP RSZ Global Image Processing Settings: [1]
- ISS RESIZER Register Summary: [2]

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Table 8-622. RZB_SDR_Y_BAD_L

Address Offset	0x0000 0164		
Physical Address	0x5201 0564	**Instance**	ISS_RESIZER
Description	RESIZER B - OUTPUT MEMORY BASE ADDRESS REGISTER This register is used if the output data format is one of the following: RAW, YUV4:2:2, YUV4:2:0, RGB5:6:5, RGBA. RAW: RAW data is written to this address YUV4:2:2: YUV data is written to this address YUV4:2:0: Y data is written to this address RGB5:6:5: 16-bit RGB data is written to this address RGBA: 32-bit RGBA data is written to this address		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																Y_BAD_L															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:0	Y_BAD_L	Memory Base Address Sets the 16 lower bits of the 32-bit base address of the circular buffer in memory. It is a byte address. YUV4:2:0 format (output data on 8 bits): The two least significant bits must be set to 00 when horizontal reversal mode is off. The two least significant bits must be set to 11 when horizontal reversal mode is on. RAW, RGB5:6:5 and YUV4:2:2 formats (output data on 16 bits): The two least significant bits must be set to 00 when horizontal reversal mode is off. The two least significant bits must be set to 11 when horizontal reversal mode is on. RGBA format (output data on 32 bits): The three least significant bits must be set to "000" when horizontal reversal mode is off. The three least significant bits must be set to "111" when horizontal reversal mode is on.	RW	0x0000

Table 8-623. Register Call Summary for Register RZB_SDR_Y_BAD_L

ISS ISP

- ISS ISP RSZ Functional Description: [0]
- ISS ISP RSZ Global Image Processing Settings: [1]
- ISS RESIZER Register Summary: [2]

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Table 8-624. RZB_SDR_Y_SAD_H

Address Offset	0x0000 0168		
Physical Address	0x5201 0568	**Instance**	ISS_RESIZER
Description	RESIZER B - OUTPUT MEMORY START ADDRESS REGISTER This register is used if the output data format is one of the following: RAW, YUV4:2:2, YUV4:2:0, RGB5:6:5, RGBA. RAW: RAW data is written to this address YUV4:2:2: YUV data is written to this address YUV4:2:0: Y data is written to this address RGB5:6:5: 16-bit RGB data is written to this address RGBA: 32-bit RGBA data is written to this address		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																Y_SAD_H															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:0	Y_SAD_H	Memory Start Address Sets 16 upper bits of the 32-bit start address in memory.	RW	0x0000

Table 8-625. Register Call Summary for Register RZB_SDR_Y_SAD_H

ISS ISP

- ISS ISP RSZ Functional Description: [0]
- ISS ISP RSZ Global Image Processing Settings: [1]
- ISS RESIZER Register Summary: [2]

Table 8-626. RZB_SDR_Y_SAD_L

Address Offset	0x0000 016C		
Physical Address	0x5201 056C	**Instance**	ISS_RESIZER
Description	RESIZER B - OUTPUT MEMORY START ADDRESS REGISTER This register is used if the output data format is one of the following: RAW, YUV4:2:2, YUV4:2:0, RGB5:6:5, RGBA. RAW: RAW data is written to this address YUV4:2:2: YUV data is written to this address YUV4:2:0: Y data is written to this address RGB5:6:5: 16-bit RGB data is written to this address RGBA: 32-bit RGBA data is written to this address		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																Y_SAD_L															

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Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:0	Y_SAD_L	Memory Start Address Sets the 16 lower bits of the 32-bit start address in memory. It is a byte address. For every frame, the first line of data will be written to this address. We have: SAD = BAD + (PTR_S x OFT) and PTR_S PTR_E If the first line must be written at the beginning of the circular buffer memory then SAD = BAD and PTR_S = 0. YUV4:2:0 format (output data on 8 bits): The two least significant bits must be set to 00 when horizontal reversal mode is off. The two least significant bits must be set to 11 when horizontal reversal mode is on. RAW, RGB5:6:5 and YUV4:2:2 formats (output data on 16 bits): The two least significant bits must be set to 00 when horizontal reversal mode is off. The two least significant bits must be set to 11 when horizontal reversal mode is on. RGBA format (output data on 32 bits): The three least significant bits must be set to "000" when horizontal reversal mode is off. The three least significant bits must be set to "111" when horizontal reversal mode is on.	RW	0x0000

Table 8-627. Register Call Summary for Register RZB_SDR_Y_SAD_L

ISS ISP

- ISS ISP RSZ Functional Description: [0]
- ISS ISP RSZ Global Image Processing Settings: [1] [2]
- ISS RESIZER Register Summary: [3]

Table 8-628. RZB_SDR_Y_OFT

Address Offset	0x0000 0170		
Physical Address	0x5201 0570	**Instance**	ISS_RESIZER
Description	RESIZER B - OUTPUT MEMORY OFFSET REGISTER This register is used if the output data format is one of the following: RAW, YUV4:2:2, YUV4:2:0 or RGBA.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																Y_OFT															

Bits	Field Name	Description	Type	Reset
31:17	RESERVED		R	0x0000
16:0	Y_OFT	Memory Line Offset Sets the size of each line in the circular buffer. It is expressed in bytes and unsigned. Note that OFT does not necessary corresponds to the size of a line in a frame, it can be much bigger. The line offset must be a multiple of 128 bytes (bits [6:0] of RZX_SDR_Y_OFT and RZX_SDR_C_OFT must be set to 0). Example: line 0 address = SAD line 1 address = SAD + 1 x OFT line 2 address = SAD + 2 x OFT	RW	0x00000

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Table 8-629. Register Call Summary for Register RZB_SDR_Y_OFT

ISS ISP

- ISS ISP RSZ Functional Description: [0]
- ISS ISP RSZ Global Image Processing Settings: [1]
- ISS RESIZER Register Summary: [2]

Table 8-630. RZB_SDR_Y_PTR_S

Address Offset	0x0000 0174		
Physical Address	0x5201 0574	**Instance**	ISS_RESIZER
Description	RESIZER B - OUTPUT MEMORY START ADDRESS REGISTER This register is used if the output data format is one of the following: RAW, YUV4;2:2, YUV4:2:0 or RGBA.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								Y_PTR_S							

Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000
12:0	Y_PTR_S	Start Line of Memory Pointer Sets the vertical position of the first output line in the output memory space. This value is expressed in number of lines. The hardware uses it to set up the initial value of the circular buffer. It must be set up such as PTR_S = (SAD - BAD) / OFT. This value must be set to 0 when RSZ_RZA_SDR_Y_BAD = RSZ_RZA_SDR_Y_SAD.	RW	0x0000

Table 8-631. Register Call Summary for Register RZB_SDR_Y_PTR_S

ISS ISP

- ISS ISP RSZ Functional Description: [0]
- ISS ISP RSZ Global Image Processing Settings: [1]
- ISS RESIZER Register Summary: [2]

Table 8-632. RZB_SDR_Y_PTR_E

Address Offset	0x0000 0178		
Physical Address	0x5201 0578	**Instance**	ISS_RESIZER
Description	RESIZER B - OUTPUT MEMORY END ADDRESS REGISTER This register is used if the output data format is one of the following: RAW, YUV4:2:2, YUV4:2:0 or RGBA.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								Y_PTR_E							

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Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000
12:0	Y_PTR_E	End Line of Memory Pointer Sets the maximum number of lines to be stored in the output memory space. This value is expressed in number of lines. When the number of output lines exceeds this value, the address restarts from the first address in the output memory space (BAD).	RW	0x0000

Table 8-633. Register Call Summary for Register RZB_SDR_Y_PTR_E

ISS ISP

- ISS ISP RSZ Functional Description: [0]
- ISS ISP RSZ Global Image Processing Settings: [1]
- ISS ISP5 SYS1 Register Description: [2] [3] [4] [5]
- ISS RESIZER Register Summary: [6]

Table 8-634. RZB_SDR_C_BAD_H

Address Offset	0x0000 017C		
Physical Address	0x5201 057C	**Instance**	ISS_RESIZER
Description	RESIZER B - OUTPUT MEMORY BASE ADDRESS REGISTER FOR CHROMA DATA (YUV4:2:0) This register is used if the output data format is YUV4:2:0. U and V data are written into this buffer.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																C_BAD_H															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:0	C_BAD_H	Memory Base Address Sets the 16 upper bits of the 32-bit base address of the circular buffer in memory.	RW	0x0000

Table 8-635. Register Call Summary for Register RZB_SDR_C_BAD_H

ISS ISP

- ISS ISP RSZ Functional Description: [0]
- ISS ISP RSZ Global Image Processing Settings: [1]
- ISS RESIZER Register Summary: [2]

Table 8-636. RZB_SDR_C_BAD_L

Address Offset	0x0000 0180		
Physical Address	0x5201 0580	**Instance**	ISS_RESIZER
Description	RESIZER B - OUTPUT MEMORY BASE ADDRESS REGISTER FOR CHROMA DATA (YUV4:2:0) This register is used if the output data format is YUV4:2:0. U and V data are written into this buffer.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																C_BAD_L															

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Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:0	C_BAD_L	Memory Base Address Sets the 16 lower bits of the 32-bit base address of the circular buffer in memory. It is a byte address. YUV4:2:0 format (output data on 8 bits): The two least significant bits must be set to 00 when horizontal reversal mode is off. The two least significant bits must be set to 11 when horizontal reversal mode is on.	RW	0x0000

Table 8-637. Register Call Summary for Register RZB_SDR_C_BAD_L

ISS ISP

- ISS ISP RSZ Functional Description: [0]
- ISS ISP RSZ Global Image Processing Settings: [1]
- ISS RESIZER Register Summary: [2]

Table 8-638. RZB_SDR_C_SAD_H

Address Offset	0x0000 0184		
Physical Address	0x5201 0584	**Instance**	ISS_RESIZER
Description	RESIZER B - OUTPUT MEMORY START ADDRESS REGISTER FOR CHROMA DATA (YUV4:2:0) This register is used if the output data format is YUV4:2:0. U and V data are written into this buffer.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																C_SAD_H															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:0	C_SAD_H	Memory Base Address Sets the 16 upper bits of the 32-bit start address in memory.	RW	0x0000

Table 8-639. Register Call Summary for Register RZB_SDR_C_SAD_H

ISS ISP

- ISS ISP RSZ Functional Description: [0]
- ISS ISP RSZ Global Image Processing Settings: [1]
- ISS RESIZER Register Summary: [2]

Table 8-640. RZB_SDR_C_SAD_L

Address Offset	0x0000 0188		
Physical Address	0x5201 0588	**Instance**	ISS_RESIZER
Description	RESIZER B - OUTPUT MEMORY START ADDRESS REGISTER FOR CHROMA DATA (YUV4:2:0) This register is used if the output data format is YUV4:2:0. U and V data are written into this buffer.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																C_SAD_L															

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Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:0	C_SAD_L	Memory Base Address Sets the 16 lower bits of the 32-bit start address in memory. It is a byte address. For every frame, the first line of data will be written to this address (C_SAD_H/C_SAD_L). We have: SAD = BAD + (PTR_S x OFT) and PTR_S PTR_E If the first line must be written at the beginning of the circular buffer memory then SAD = BAD and PTR_S = 0. YUV4:2:0 format (output data on 8 bits): The two least significant bits must be set to 00 when horizontal reversal mode is off. The two least significant bits must be set to 11 when horizontal reversal mode is on.	RW	0x0000

Table 8-641. Register Call Summary for Register RZB_SDR_C_SAD_L

ISS ISP

- ISS ISP RSZ Functional Description: [0]
- ISS ISP RSZ Global Image Processing Settings: [1] [2]
- ISS RESIZER Register Summary: [3]

Table 8-642. RZB_SDR_C_OFT

Address Offset	0x0000 018C		
Physical Address	0x5201 058C	**Instance**	ISS_RESIZER
Description	RESIZER B - OUTPUT MEMORY OFFSET REGISTER FOR CHROMA DATA (YUV4:2:0) This register is used if the output data format is YUV4:2:0		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																C_OFT															

Bits	Field Name	Description	Type	Reset
31:17	RESERVED		R	0x0000
16:0	C_OFT	Memory Line Offset Sets the size of each line in the circular buffer. It is expressed in bytes and unsigned. Note that OFT does not necessary corresponds to the size of a line in a frame, it can be much bigger. The line offset must be a multiple of 128 bytes (bits [6:0] of RZX_SDR_Y_OFT and RZX_SDR_C_OFT must be set to 0). Example: line 0 address = SAD line 1 address = SAD + 1 x OFT line 2 address = SAD + 2 x OFT	RW	0x00000

Table 8-643. Register Call Summary for Register RZB_SDR_C_OFT

ISS ISP

- ISS ISP RSZ Functional Description: [0]
- ISS ISP RSZ Global Image Processing Settings: [1]
- ISS RESIZER Register Summary: [2]

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Table 8-644. RZB_SDR_C_PTR_S

Address Offset	0x0000 0190		
Physical Address	0x5201 0590	**Instance**	ISS_RESIZER
Description	RESIZER B - OUTPUT MEMORY START ADDRESS REGISTER FOR CHROMA DATA (YUV4:2:0) This register is used if the output data format is YUV4:2:0		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								C_PTR_S							

Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000
12:0	C_PTR_S	Start Line of Memory Pointer Sets the vertical position of the first output line in the output memory space. This value is expressed in number of lines. The hardware uses it to set up the initial value of the circular buffer. It must be set up such as PTR_S = (SAD - BAD) / OFT. This value must be set to 0 when RSZ_RZA_SDR_C_BAD = RSZ_RZA_SDR_C_SAD.	RW	0x0000

Table 8-645. Register Call Summary for Register RZB_SDR_C_PTR_S

ISS ISP

- ISS ISP RSZ Functional Description: [0]
- ISS ISP RSZ Global Image Processing Settings: [1]
- ISS RESIZER Register Summary: [2]

Table 8-646. RZB_SDR_C_PTR_E

Address Offset	0x0000 0194		
Physical Address	0x5201 0594	**Instance**	ISS_RESIZER
Description	RESIZER B - OUTPUT MEMORY END ADDRESS REGISTER FOR CHROMA DATA (YUV4:2:0) This register is used if the output data format is YUV4:2:0		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								C_PTR_E							

Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000
12:0	C_PTR_E	End Line of Memory Pointer Sets the maximum number of lines to be stored in the output memory space. This value is expressed in number of lines. When the number of output lines exceeds this value, the address restarts from the first address in the output memory space (BAD).	RW	0x0000

Table 8-647. Register Call Summary for Register RZB_SDR_C_PTR_E

ISS ISP

- ISS ISP RSZ Functional Description: [0]
- ISS ISP RSZ Global Image Processing Settings: [1]
- ISS RESIZER Register Summary: [2]

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8.3.5.5 ISS IPIPE registers

8.3.5.5.1 ISS IPIPE Register Summary

Table 8-648. ISS IPIPE Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	ISS_IPIPE Base Address
IPIPE_SRC_EN	RW	32	0x0000 0000	0x5201 0800
IPIPE_SRC_MODE	RW	32	0x0000 0004	0x5201 0804
IPIPE_SRC_FMT	RW	32	0x0000 0008	0x5201 0808
IPIPE_SRC_COL	RW	32	0x0000 000C	0x5201 080C
IPIPE_SRC_VPS	RW	32	0x0000 0010	0x5201 0810
IPIPE_SRC_VSZ	RW	32	0x0000 0014	0x5201 0814
IPIPE_SRC_HPS	RW	32	0x0000 0018	0x5201 0818
IPIPE_SRC_HSZ	RW	32	0x0000 001C	0x5201 081C
IPIPE_SEL_SBU	RW	32	0x0000 0020	0x5201 0820
IPIPE_SRC_STA	R	32	0x0000 0024	0x5201 0824
IPIPE_GCK_MMR	RW	32	0x0000 0028	0x5201 0828
IPIPE_GCK_PIX	RW	32	0x0000 002C	0x5201 082C
RESERVED	R	32	0x0000 0030	0x5201 0830
IPIPE_DPC_LUT_EN	RW	32	0x0000 0034	0x5201 0834
IPIPE_DPC_LUT_SEL	RW	32	0x0000 0038	0x5201 0838
IPIPE_DPC_LUT_ADR	RW	32	0x0000 003C	0x5201 083C
IPIPE_DPC_LUT_SIZ	RW	32	0x0000 0040	0x5201 0840
RESERVEDa[1]	RW	32	0x0000 0044 + (b * 4)	0x5201 0844 + (b * 4)
IPIPE_LSC_VOFT	RW	32	0x0000 0090	0x5201 0890
IPIPE_LSC_VA2	RW	32	0x0000 0094	0x5201 0894
IPIPE_LSC_VA1	RW	32	0x0000 0098	0x5201 0898
IPIPE_LSC_VS	RW	32	0x0000 009C	0x5201 089C
IPIPE_LSC_HOFT	RW	32	0x0000 00A0	0x5201 08A0
IPIPE_LSC_HA2	RW	32	0x0000 00A4	0x5201 08A4
IPIPE_LSC_HA1	RW	32	0x0000 00A8	0x5201 08A8
IPIPE_LSC_HS	RW	32	0x0000 00AC	0x5201 08AC
IPIPE_LSC_GAN_R	RW	32	0x0000 00B0	0x5201 08B0
IPIPE_LSC_GAN_GR	RW	32	0x0000 00B4	0x5201 08B4
IPIPE_LSC_GAN_GB	RW	32	0x0000 00B8	0x5201 08B8
IPIPE_LSC_GAN_B	RW	32	0x0000 00BC	0x5201 08BC
IPIPE_LSC_OFT_R	RW	32	0x0000 00C0	0x5201 08C0
IPIPE_LSC_OFT_GR	RW	32	0x0000 00C4	0x5201 08C4
IPIPE_LSC_OFT_GB	RW	32	0x0000 00C8	0x5201 08C8
IPIPE_LSC_OFT_B	RW	32	0x0000 00CC	0x5201 08CC
IPIPE_LSC_SHF	RW	32	0x0000 00D0	0x5201 08D0
IPIPE_LSC_MAX	RW	32	0x0000 00D4	0x5201 08D4
RESERVEDb[1]	RW	32	0x0000 00D8 + (b * 0x4)	0x5201 08D8 + (b * 0x4)
RESERVEDc[1]	RW	32	0x0000 01B8 + (c * 0x4)	0x5201 09B8 + (c * 0x4)

(1) a = 0 to 18
b = 0 to 55
c = 0 to 5
d = 0 to 14
e = 0 to 1
f = 0 to 24
g = 0 to 18

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Table 8-648. ISS IPIPE Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	ISS_IPIPE Base Address
IPIPE_WB2_OFT_R	RW	32	0x0000 01D0	0x5201 09D0
IPIPE_WB2_OFT_GR	RW	32	0x0000 01D4	0x5201 09D4
IPIPE_WB2_OFT_GB	RW	32	0x0000 01D8	0x5201 09D8
IPIPE_WB2_OFT_B	RW	32	0x0000 01DC	0x5201 09DC
IPIPE_WB2_WGN_R	RW	32	0x0000 01E0	0x5201 09E0
IPIPE_WB2_WGN_GR	RW	32	0x0000 01E4	0x5201 09E4
IPIPE_WB2_WGN_GB	RW	32	0x0000 01E8	0x5201 09E8
IPIPE_WB2_WGN_B	RW	32	0x0000 01EC	0x5201 09EC
RESERVEDd[1]	RW	32	0x0000 01F0 + (d * 0x4)	0x5201 09F0 + (d * 0x4)
IPIPE_RGB1_MUL_RR	RW	32	0x0000 022C	0x5201 0A2C
IPIPE_RGB1_MUL_GR	RW	32	0x0000 0230	0x5201 0A30
IPIPE_RGB1_MUL_BR	RW	32	0x0000 0234	0x5201 0A34
IPIPE_RGB1_MUL_RG	RW	32	0x0000 0238	0x5201 0A38
IPIPE_RGB1_MUL_GG	RW	32	0x0000 023C	0x5201 0A3C
IPIPE_RGB1_MUL_BG	RW	32	0x0000 0240	0x5201 0A40
IPIPE_RGB1_MUL_RB	RW	32	0x0000 0244	0x5201 0A44
IPIPE_RGB1_MUL_GB	RW	32	0x0000 0248	0x5201 0A48
IPIPE_RGB1_MUL_BB	RW	32	0x0000 024C	0x5201 0A4C
IPIPE_RGB1_OFT_OR	RW	32	0x0000 0250	0x5201 0A50
IPIPE_RGB1_OFT_OG	RW	32	0x0000 0254	0x5201 0A54
IPIPE_RGB1_OFT_OB	RW	32	0x0000 0258	0x5201 0A58
IPIPE_GMM_CFG	RW	32	0x0000 025C	0x5201 0A5C
IPIPE_RGB2_MUL_RR	RW	32	0x0000 0260	0x5201 0A60
IPIPE_RGB2_MUL_GR	RW	32	0x0000 0264	0x5201 0A64
IPIPE_RGB2_MUL_BR	RW	32	0x0000 0268	0x5201 0A68
IPIPE_RGB2_MUL_RG	RW	32	0x0000 026C	0x5201 0A6C
IPIPE_RGB2_MUL_GG	RW	32	0x0000 0270	0x5201 0A70
IPIPE_RGB2_MUL_BG	RW	32	0x0000 0274	0x5201 0A74
IPIPE_RGB2_MUL_RB	RW	32	0x0000 0278	0x5201 0A78
IPIPE_RGB2_MUL_GB	RW	32	0x0000 027C	0x5201 0A7C
IPIPE_RGB2_MUL_BB	RW	32	0x0000 0280	0x5201 0A80
IPIPE_RGB2_OFT_OR	RW	32	0x0000 0284	0x5201 0A84
IPIPE_RGB2_OFT_OG	RW	32	0x0000 0288	0x5201 0A88
IPIPE_RGB2_OFT_OB	RW	32	0x0000 028C	0x5201 0A8C
RESERVED	RW	32	0x0000 0290	0x5201 0A90
IPIPE_YUV_ADJ	RW	32	0x0000 0294	0x5201 0A94
IPIPE_YUV_MUL_RY	RW	32	0x0000 0298	0x5201 0A98
IPIPE_YUV_MUL_GY	RW	32	0x0000 029C	0x5201 0A9C
IPIPE_YUV_MUL_BY	RW	32	0x0000 02A0	0x5201 0AA0
IPIPE_YUV_MUL_RCB	RW	32	0x0000 02A4	0x5201 0AA4
IPIPE_YUV_MUL_GCB	RW	32	0x0000 02A8	0x5201 0AA8
IPIPE_YUV_MUL_BCB	RW	32	0x0000 02AC	0x5201 0AAC
IPIPE_YUV_MUL_RCR	RW	32	0x0000 02B0	0x5201 0AB0
IPIPE_YUV_MUL_GCR	RW	32	0x0000 02B4	0x5201 0AB4
IPIPE_YUV_MUL_BCR	RW	32	0x0000 02B8	0x5201 0AB8
IPIPE_YUV_OFT_Y	RW	32	0x0000 02BC	0x5201 0ABC
IPIPE_YUV_OFT_CB	RW	32	0x0000 02C0	0x5201 0AC0

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Table 8-648. ISS IPIPE Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	ISS_IPIPE Base Address
IPIPE_YUV_OFT_CR	RW	32	0x0000 02C4	0x5201 0AC4
IPIPE_YUV_PHS	RW	32	0x0000 02C8	0x5201 0AC8
RESERVEDe[2]	RW	32	0x0000 02CC + (e * 0x4)	0x5201 0ACC + (e * 0x4)
IPIPE_YEE_EN	RW	32	0x0000 02D4	0x5201 0AD4
IPIPE_YEE_TYP	RW	32	0x0000 02D8	0x5201 0AD8
IPIPE_YEE_SHF	RW	32	0x0000 02DC	0x5201 0ADC
IPIPE_YEE_MUL_00	RW	32	0x0000 02E0	0x5201 0AE0
IPIPE_YEE_MUL_01	RW	32	0x0000 02E4	0x5201 0AE4
IPIPE_YEE_MUL_02	RW	32	0x0000 02E8	0x5201 0AE8
IPIPE_YEE_MUL_10	RW	32	0x0000 02EC	0x5201 0AEC
IPIPE_YEE_MUL_11	RW	32	0x0000 02F0	0x5201 0AF0
IPIPE_YEE_MUL_12	RW	32	0x0000 02F4	0x5201 0AF4
IPIPE_YEE_MUL_20	RW	32	0x0000 02F8	0x5201 0AF8
IPIPE_YEE_MUL_21	RW	32	0x0000 02FC	0x5201 0AFC
IPIPE_YEE_MUL_22	RW	32	0x0000 0300	0x5201 0B00
IPIPE_YEE_THR	RW	32	0x0000 0304	0x5201 0B04
IPIPE_YEE_E_GAN	RW	32	0x0000 0308	0x5201 0B08
IPIPE_YEE_E_THR_1	RW	32	0x0000 030C	0x5201 0B0C
IPIPE_YEE_E_THR_2	RW	32	0x0000 0310	0x5201 0B10
IPIPE_YEE_G_GAN	RW	32	0x0000 0314	0x5201 0B14
IPIPE_YEE_G_OFT	RW	32	0x0000 0318	0x5201 0B18
RESERVEDf[3]	RW	32	0x0000 031C + (f * 0x4)	0x5201 0B1C + (f * 0x4)
IPIPE_BOX_EN	RW	32	0x0000 0380	0x5201 0B80
IPIPE_BOX_MODE	RW	32	0x0000 0384	0x5201 0B84
IPIPE_BOX_TYP	RW	32	0x0000 0388	0x5201 0B88
IPIPE_BOX_SHF	RW	32	0x0000 038C	0x5201 0B8C
IPIPE_BOX_SDR_SAD_H	RW	32	0x0000 0390	0x5201 0B90
IPIPE_BOX_SDR_SAD_L	RW	32	0x0000 0394	0x5201 0B94
RESERVED	R	32	0x0000 0398	0x5201 0B98
IPIPE_HST_EN	RW	32	0x0000 039C	0x5201 0B9C
IPIPE_HST_MODE	RW	32	0x0000 03A0	0x5201 0BA0
IPIPE_HST_SEL	RW	32	0x0000 03A4	0x5201 0BA4
IPIPE_HST_PARA	RW	32	0x0000 03A8	0x5201 0BA8
IPIPE_HST_0_VPS	RW	32	0x0000 03AC	0x5201 0BAC
IPIPE_HST_0_VSZ	RW	32	0x0000 03B0	0x5201 0BB0

(2) a = 0 to 18
b = 0 to 55
c = 0 to 5
d = 0 to 14
e = 0 to 1
f = 0 to 24
g = 0 to 18

(3) a = 0 to 18
b = 0 to 55
c = 0 to 5
d = 0 to 14
e = 0 to 1
f = 0 to 24
g = 0 to 18

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Table 8-648. ISS IPIPE Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	ISS_IPIPE Base Address
IPIPE_HST_0_HPS	RW	32	0x0000 03B4	0x5201 0BB4
IPIPE_HST_0_HSZ	RW	32	0x0000 03B8	0x5201 0BB8
IPIPE_HST_1_VPS	RW	32	0x0000 03BC	0x5201 0BBC
IPIPE_HST_1_VSZ	RW	32	0x0000 03C0	0x5201 0BC0
IPIPE_HST_1_HPS	RW	32	0x0000 03C4	0x5201 0BC4
IPIPE_HST_1_HSZ	RW	32	0x0000 03C8	0x5201 0BC8
IPIPE_HST_2_VPS	RW	32	0x0000 03CC	0x5201 0BCC
IPIPE_HST_2_VSZ	RW	32	0x0000 03D0	0x5201 0BD0
IPIPE_HST_2_HPS	RW	32	0x0000 03D4	0x5201 0BD4
IPIPE_HST_2_HSZ	RW	32	0x0000 03D8	0x5201 0BD8
IPIPE_HST_3_VPS	RW	32	0x0000 03DC	0x5201 0BDC
IPIPE_HST_3_VSZ	RW	32	0x0000 03E0	0x5201 0BE0
IPIPE_HST_3_HPS	RW	32	0x0000 03E4	0x5201 0BE4
IPIPE_HST_3_HSZ	RW	32	0x0000 03E8	0x5201 0BE8
IPIPE_HST_TBL	RW	32	0x0000 03EC	0x5201 0BEC
IPIPE_HST_MUL_R	RW	32	0x0000 03F0	0x5201 0BF0
IPIPE_HST_MUL_GR	RW	32	0x0000 03F4	0x5201 0BF4
IPIPE_HST_MUL_GB	RW	32	0x0000 03F8	0x5201 0BF8
IPIPE_HST_MUL_B	RW	32	0x0000 03FC	0x5201 0BFC
RESERVEDg[3]	RW	32	0x0000 0400 + (g * 0x4)	0x5201 0C00 + (g * 0x4)

8.3.5.5.2 ISS IPIPE Register Description

Table 8-649. IPIPE_SRC_EN

Address Offset	0x0000 0000		
Physical Address	0x5201 0800	**Instance**	ISS_IPIPE
Description	This register is not shadowed		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED															EN

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:1	RESERVED		R	0x0000
0	EN	The start flag of the IPIPE module. When EN is 1, the IPIPE module starts a processing from the next rising edge of the VD. If the processing mode of the IPIPE module is one shot, the EN is cleared to 0 immediately after the processing has started. 0x0: waiting 0x1: start/busy	RW	0

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Table 8-650. Register Call Summary for Register IPIPE_SRC_EN

ISS ISP

- ISS ISP IPIPE Input Interface: [0]
- Global Initialization: [1]
- ISS ISP IPIPE Operational Modes Configuration: [2] [3] [4] [5]
- ISS IPIPE Register Summary: [6]

Table 8-651. IPIPE_SRC_MODE

Address Offset	0x0000 0004		
Physical Address	0x5201 0804	**Instance**	ISS_IPIPE
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED														WRT	OST

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:2	RESERVED		R	0x0000
1	WRT	The mode selection of the ipipeif_wrt which is an input port of the IPIPE module. If WRT is 0, the IPIPE module does not use the ipipeif_wrt. Else the IPIPE module uses it. 0x0: Disable 0x1: Enable	RW	0
0	OST	The processing mode selection of the IPIPE module. Value 0 indicates the mode of free run, value 1 indicates the mode of one shot. 0x0: Free run 0x1: One shot	RW	0

Table 8-652. Register Call Summary for Register IPIPE_SRC_MODE

ISS ISP

- ISS ISP IPIPE Input Interface: [0] [1] [2] [3]
- Global Initialization: [4] [5]
- ISS IPIPE Register Summary: [6]

Table 8-653. IPIPE_SRC_FMT

Address Offset	0x0000 0008		
Physical Address	0x5201 0808	**Instance**	ISS_IPIPE
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED															FMT

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Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:2	RESERVED		R	0x0000
1:0	FMT	IPIPE module data path selection 0x0: IN: RAW BAYER OUT: YUV4:2:2 Note that the IPIPE YUV4:2:2 output goes to the RESIZER module where it can be further be converted in YUV4:2:0 or RGB format. 0x1: IN: RAW BAYER OUT: RAW BAYER The data are output after the White Balance module. It enables to bypass a large part of the IPIPE module. 0x3: IN: YUV4:2:2 OUT: YUV4:2:2 Note that the IPIPE YUV4:2:2 output goes to the RESIZER module where it can be further be converted in YUV4:2:0 or RGB format. 0x2: IN: RAW BAYER OUT: DISABLED The data are only going to BOXCAR and HISTOGRAM modules.	RW	0x0

Table 8-654. Register Call Summary for Register IPIPE_SRC_FMT

ISS ISP

- ISS ISP IPIPE Input Interface: [0] [1]
- Global Initialization: [2]
- ISS ISP IPIPE Operational Modes Configuration: [3] [4] [5] [6]
- ISS IPIPE Register Summary: [7]
- ISS IPIPE Register Description: [8] [9] [10]

Table 8-655. IPIPE_SRC_COL

Address Offset	0x0000 000C		
Physical Address	0x5201 080C	**Instance**	ISS_IPIPE
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								OO		OE		EO		EE	

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:8	RESERVED		R	0x00
7:6	OO	The color pattern of the odd line and odd pixel. This parameter is valid when IPIPE_SRC[FMT] is 0,1,2. 0x0: R 0x1: Gr 0x3: B 0x2: Gb	RW	0x3
5:4	OE	The color pattern of the odd line and even pixel. This parameter is valid when IPIPE_SRC[FMT] is 0,1,2. 0x0: R 0x1: Gr 0x3: B 0x2: Gb	RW	0x2

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Bits	Field Name	Description	Type	Reset
3:2	EO	The color pattern of the even line and odd pixel. This parameter is valid when IPIPE_SRC[FMT] is 0,1,2. 0x0: R 0x1: Gr 0x3: B 0x2: Gb	RW	0x1
1:0	EE	The color pattern of the even line and even pixel. This parameter is valid when IPIPE_SRC[FMT] is 0,1,2. 0x0: R 0x1: Gr 0x3: B 0x2: Gb	RW	0x0

Table 8-656. Register Call Summary for Register IPIPE_SRC_COL

ISS ISP
- ISS IPIPE Register Summary: [0]

Table 8-657. IPIPE_SRC_VPS

Address Offset	0x0000 0010		
Physical Address	0x5201 0810	**Instance**	ISS_IPIPE
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																VAL															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:0	VAL	The vertical position of the global frame from the rising edge of the VD. The IPIPE module will start an image processing from VAL line.	RW	0x0000

Table 8-658. Register Call Summary for Register IPIPE_SRC_VPS

ISS ISP
- ISS ISP IPIPE Input Interface: [0]
- Global Initialization: [1]
- ISS IPIPE Register Summary: [2]
- ISS IPIPE Register Description: [3] [4] [5] [6] [7] [8] [9] [10]

Table 8-659. IPIPE_SRC_VSZ

Address Offset	0x0000 0014		
Physical Address	0x5201 0814	**Instance**	ISS_IPIPE
Description			
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12:0	VAL	The vertical size of the processing area. The VAL0 can not be written. The IPIPE module will process (VAL+1) lines.	RW	0x0000

Table 8-660. Register Call Summary for Register IPIPE_SRC_VSZ

ISS ISP

- ISS ISP IPIPE Input Interface: [0]
- Global Initialization: [1]
- ISS IPIPE Register Summary: [2]

Table 8-661. IPIPE_SRC_HPS

Address Offset	0x0000 0018		
Physical Address	0x5201 0818	**Instance**	ISS_IPIPE
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																VAL															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:0	VAL	The horizontal position of the global frame from the rising edge of the HD. The IPIPE module will start an image processing from VAL clock.	RW	0x0000

Table 8-662. Register Call Summary for Register IPIPE_SRC_HPS

ISS ISP

- ISS ISP IPIPE Input Interface: [0]
- Global Initialization: [1]
- ISS IPIPE Register Summary: [2]
- ISS IPIPE Register Description: [3] [4] [5] [6] [7] [8] [9] [10]

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Table 8-663. IPIPE_SRC_HSZ

Address Offset	0x0000 001C		
Physical Address	0x5201 081C	**Instance**	ISS_IPIPE
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																VAL															VAL_0

Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000
12:1	VAL	The horizontal size of the processing area. The VAL0 is fixed. The IPIPE module processes (VAL+1) clocks.	RW	0x000
0	VAL_0	This is the LSB of the VAL[12:0]. This bit is read only.	R	1

Table 8-664. Register Call Summary for Register IPIPE_SRC_HSZ

ISS ISP

- ISS ISP IPIPE Input Interface: [0]
- Global Initialization: [1]
- ISS IPIPE Register Summary: [2]

Table 8-665. IPIPE_SEL_SBU

Address Offset	0x0000 0020		
Physical Address	0x5201 0820	**Instance**	ISS_IPIPE
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED															EDOF

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:1	RESERVED		R	0x0000
0	EDOF	EDOF port selection This bit must not be enabled since the EDOF module is not implemented. This is a provision for a future revision of the IP. 0x0: Not used 0x1: Used	RW	0

Table 8-666. Register Call Summary for Register IPIPE_SEL_SBU

ISS ISP

- ISS IPIPE Register Summary: [0]

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Table 8-667. IPIPE_SRC_STA

Address Offset	0x0000 0024		
Physical Address	0x5201 0824	**Instance**	ISS_IPIPE
Description	IPIPE STATUS REGISTER		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED											VAL4	VAL3	VAL2	VAL1	VAL0

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:5	RESERVED		R	0x000
4	VAL4	Status of Histogram Process (busy status).	R	0
3	VAL3	Status of Histogram bank select.	R	0
2	VAL2	Status of BSC process (busy status).	R	0
1	VAL1	Status of Boxcar process (busy status).	R	0
0	VAL0	Status of Boxcar process (error status). This bit will be triggered when an overflow happens while transferring the boxcar data to memory. Instead of polling for this register, it is preferable to use the IPIPE_BOXCAR_OVF interrupt. Overflow errors are non recoverable at ISP level and require a software reset at ISS level.	R	0

Table 8-668. Register Call Summary for Register IPIPE_SRC_STA

ISS ISP

- ISS ISP IPIPE Interrupts: [0]
- ISS IPIPE Register Summary: [1]

Table 8-669. IPIPE_GCK_MMR

Address Offset	0x0000 0028		
Physical Address	0x5201 0828	**Instance**	ISS_IPIPE
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED															REG

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:1	RESERVED		R	0x0000
0	REG	The on/off selection of the clk_arm_g0 which is used for some ARM register access. 0x0: Off 0x1: On	RW	0

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Table 8-670. Register Call Summary for Register IPIPE_GCK_MMR

ISS ISP
- Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-671. IPIPE_GCK_PIX

Address Offset	0x0000 002C		
Physical Address	0x5201 082C	**Instance**	ISS_IPIPE
Description	This register is not shadowed		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED												G3	G2	G1	G0

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:4	RESERVED		R	0x000
3	G3	The on/off selection of the clk_pix_g3 which is use for the IPIPE processes of EE and "CAR". 0x0: Disable 0x1: Enable	RW	0
2	G2	The on/off selection of the clk_pix_g2 which is use for the IPIPE processes of CFA to "422", "Histogram(YCbCr input)", and "Boundary Signal Calculator". 0x0: Disable 0x1: Enable	RW	0
1	G1	The on/off selection of the clk_pix_g1 which is used for the IPIPE processes of "DefectCorrection" to "WhiteBalance", and "Histogram(RAW input)". 0x0: Disable 0x1: Enable	RW	0
0	G0	The on/off selection of the clk_pix_g0 which is used for the IPIPE processing of "Boxcar". 0x0: Disable 0x1: Enable	RW	0

Table 8-672. Register Call Summary for Register IPIPE_GCK_PIX

ISS ISP
- Global Initialization: [0] [1] [2] [3]
- ISS IPIPE Register Summary: [4]

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Table 8-673. IPIPE_DPC_LUT_EN

Address Offset	0x0000 0034		
Physical Address	0x5201 0834	**Instance**	ISS_IPIPE
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED															EN

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:1	RESERVED		R	0x0000
0	EN	Enable of LUT defect pixel correction. 0x0: Off 0x1: On	RW	0

Table 8-674. Register Call Summary for Register IPIPE_DPC_LUT_EN

ISS ISP

- ISS ISP IPIPE Defect Pixel Correction: [0]
- Global Initialization: [1]
- ISS IPIPE Register Summary: [2]

Table 8-675. IPIPE_DPC_LUT_SEL

Address Offset	0x0000 0038		
Physical Address	0x5201 0838	**Instance**	ISS_IPIPE
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED														TBL	DOT

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:2	RESERVED		R	0x0000
1	TBL	LUT table type selection. 0x0: Up to 1024 entries. (use IPIPE_DPC_LUT_SIZ) 0x1: infinity number of entries. (not use IPIPE_DPC_LUT_SIZ)	RW	0
0	DOT	Replace dot selection on processing method 0. 0x0: Replace with black dot 0x1: Replace with white dot	RW	0

Table 8-676. Register Call Summary for Register IPIPE_DPC_LUT_SEL

ISS ISP

- ISS ISP IPIPE Defect Pixel Correction: [0] [1] [2]
- Global Initialization: [3] [4]
- ISS IPIPE Register Summary: [5]

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Table 8-677. IPIPE_DPC_LUT_ADR

Address Offset	0x0000 003C		
Physical Address	0x5201 083C	**Instance**	ISS_IPIPE
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								ADR							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:10	RESERVED		R	0x00
9:0	ADR	The address of the first valid data in look-up-table	RW	0x000

Table 8-678. Register Call Summary for Register IPIPE_DPC_LUT_ADR

ISS ISP

- ISS ISP IPIPE Defect Pixel Correction: [0]
- Global Initialization: [1]
- ISS IPIPE Register Summary: [2]

Table 8-679. IPIPE_DPC_LUT_SIZ

Address Offset	0x0000 0040		
Physical Address	0x5201 0840	**Instance**	ISS_IPIPE
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								SIZ							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:10	RESERVED		R	0x00
9:0	SIZ	The number of valid data in look-up-table. (SIZ+1)	RW	0x000

Table 8-680. Register Call Summary for Register IPIPE_DPC_LUT_SIZ

ISS ISP

- ISS ISP IPIPE Defect Pixel Correction: [0]
- Global Initialization: [1]
- ISS IPIPE Register Summary: [2]
- ISS IPIPE Register Description: [3] [4]

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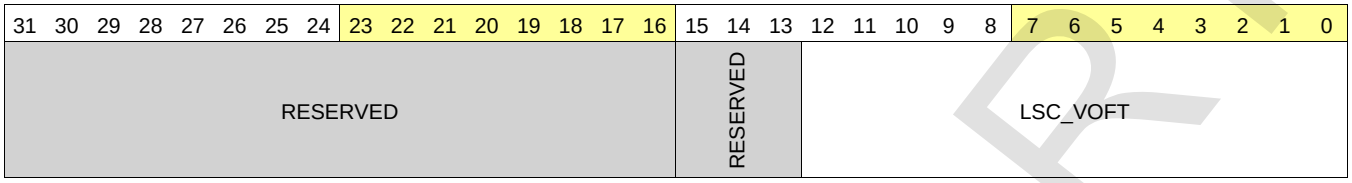
Table 8-681. IPIPE_LSC_VOFT

Address Offset	0x0000 0090		
Physical Address	0x5201 0890	**Instance**	ISS_IPIPE
Description	LSC VOFT		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12:0	LSC_VOFT		RW	0x0000

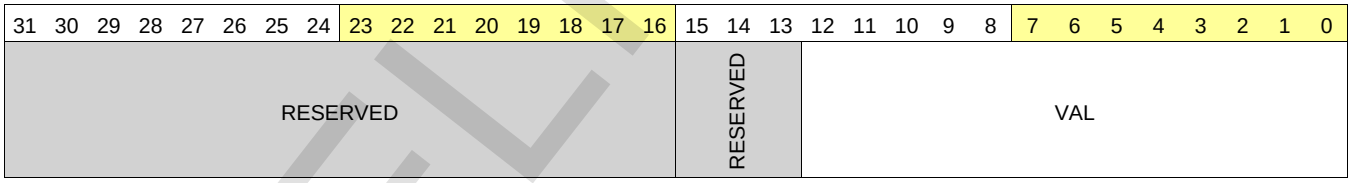
Table 8-682. Register Call Summary for Register IPIPE_LSC_VOFT

ISS ISP

- Global Initialization:
- ISS IPIPE Register Summary: [2]

Table 8-683. IPIPE_LSC_VA2

Address Offset	0x0000 0094		
Physical Address	0x5201 0894	**Instance**	ISS_IPIPE
Description			
Type	RW		



Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12:0	VAL	LSC VA2	RW	0x0000

Table 8-684. Register Call Summary for Register IPIPE_LSC_VA2

ISS ISP

- Global Initialization:
- ISS IPIPE Register Summary: [2]

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Table 8-685. IPIPE_LSC_VA1

Address Offset	0x0000 0098		
Physical Address	0x5201 0898	**Instance**	ISS_IPIPE
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12:0	VAL	LSC VA1	RW	0x0000

Table 8-686. Register Call Summary for Register IPIPE_LSC_VA1

ISS ISP

- Global Initialization:
- ISS IPIPE Register Summary: [2]

Table 8-687. IPIPE_LSC_VS

Address Offset	0x0000 009C		
Physical Address	0x5201 089C	**Instance**	ISS_IPIPE
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VS2				VS1			

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:8	RESERVED		R	0x00
7:4	VS2	LSC VS1	RW	0x0
3:0	VS1	LSC VS1	RW	0x0

Table 8-688. Register Call Summary for Register IPIPE_LSC_VS

ISS ISP

- Global Initialization:
- ISS IPIPE Register Summary: [3]

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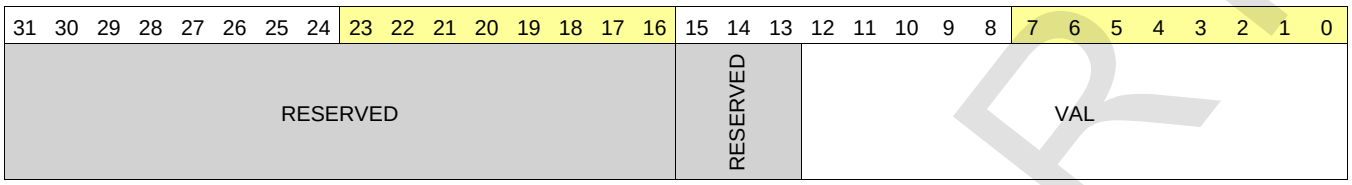
Table 8-689. IPIPE_LSC_HOFT

Address Offset	0x0000 00A0		
Physical Address	0x5201 08A0	**Instance**	ISS_IPIPE
Description			
Type	RW		



Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12:0	VAL	LSC HOFT	RW	0x0000

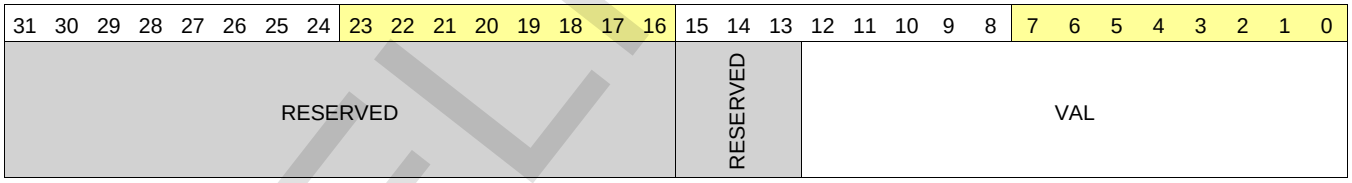
Table 8-690. Register Call Summary for Register IPIPE_LSC_HOFT

ISS ISP

- Global Initialization:
- ISS IPIPE Register Summary: [2]

Table 8-691. IPIPE_LSC_HA2

Address Offset	0x0000 00A4		
Physical Address	0x5201 08A4	**Instance**	ISS_IPIPE
Description			
Type	RW		



Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12:0	VAL	LSC HA2	RW	0x0000

Table 8-692. Register Call Summary for Register IPIPE_LSC_HA2

ISS ISP

- Global Initialization:
- ISS IPIPE Register Summary: [2]

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Table 8-693. IPIPE_LSC_HA1

Address Offset	0x0000 00A8		
Physical Address	0x5201 08A8	**Instance**	ISS_IPIPE
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12:0	VAL	LSC HA1	RW	0x0000

Table 8-694. Register Call Summary for Register IPIPE_LSC_HA1

ISS ISP

- Global Initialization:
- ISS IPIPE Register Summary: [2]

Table 8-695. IPIPE_LSC_HS

Address Offset	0x0000 00AC		
Physical Address	0x5201 08AC	**Instance**	ISS_IPIPE
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								HS2				HS1			

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:8	RESERVED		R	0x00
7:4	HS2	LSC HS1	RW	0x0
3:0	HS1	LSC HS1	RW	0x0

Table 8-696. Register Call Summary for Register IPIPE_LSC_HS

ISS ISP

- Global Initialization:
- ISS IPIPE Register Summary: [3]

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Table 8-697. IPIPE_LSC_GAN_R

Address Offset	0x0000 00B0		
Physical Address	0x5201 08B0	**Instance**	ISS_IPIPE
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:8	RESERVED		R	0x00
7:0	VAL	GAN R	RW	0x00

Table 8-698. Register Call Summary for Register IPIPE_LSC_GAN_R

ISS ISP

- Global Initialization:
- ISS IPIPE Register Summary: [1]

Table 8-699. IPIPE_LSC_GAN_GR

Address Offset	0x0000 00B4		
Physical Address	0x5201 08B4	**Instance**	ISS_IPIPE
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:8	RESERVED		R	0x00
7:0	VAL	GAN GR	RW	0x00

Table 8-700. Register Call Summary for Register IPIPE_LSC_GAN_GR

ISS ISP

- Global Initialization:
- ISS IPIPE Register Summary: [1]

Table 8-701. IPIPE_LSC_GAN_GB

Address Offset	0x0000 00B8		
Physical Address	0x5201 08B8	**Instance**	ISS_IPIPE
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

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Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:8	RESERVED		R	0x00
7:0	VAL	GAN GB	RW	0x00

Table 8-702. Register Call Summary for Register IPIPE_LSC_GAN_GB

ISS ISP
- Global Initialization:
- ISS IPIPE Register Summary: [1]

Table 8-703. IPIPE_LSC_GAN_B

Address Offset	0x0000 00BC		
Physical Address	0x5201 08BC	**Instance**	ISS_IPIPE
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:8	RESERVED		R	0x00
7:0	VAL	GAN B	RW	0x00

Table 8-704. Register Call Summary for Register IPIPE_LSC_GAN_B

ISS ISP
- Global Initialization:
- ISS IPIPE Register Summary: [1]

Table 8-705. IPIPE_LSC_OFT_R

Address Offset	0x0000 00C0		
Physical Address	0x5201 08C0	**Instance**	ISS_IPIPE
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:8	RESERVED		R	0x00
7:0	VAL	LSC OFT R	RW	0x00

Table 8-706. Register Call Summary for Register IPIPE_LSC_OFT_R

ISS ISP
- Global Initialization:
- ISS IPIPE Register Summary: [1]

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Table 8-707. IPIPE_LSC_OFT_GR

Address Offset	0x0000 00C4		
Physical Address	0x5201 08C4	**Instance**	ISS_IPIPE
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:8	RESERVED		R	0x00
7:0	VAL	LSC OFT GR	RW	0x00

Table 8-708. Register Call Summary for Register IPIPE_LSC_OFT_GR

ISS ISP

- Global Initialization:
- ISS IPIPE Register Summary: [1]

Table 8-709. IPIPE_LSC_OFT_GB

Address Offset	0x0000 00C8		
Physical Address	0x5201 08C8	**Instance**	ISS_IPIPE
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:8	RESERVED		R	0x00
7:0	VAL	LSC OFT GB	RW	0x00

Table 8-710. Register Call Summary for Register IPIPE_LSC_OFT_GB

ISS ISP

- Global Initialization:
- ISS IPIPE Register Summary: [1]

Table 8-711. IPIPE_LSC_OFT_B

Address Offset	0x0000 00CC		
Physical Address	0x5201 08CC	**Instance**	ISS_IPIPE
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

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Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:8	RESERVED		R	0x00
7:0	VAL	LSC OFT B	RW	0x00

Table 8-712. Register Call Summary for Register IPIPE_LSC_OFT_B

ISS ISP
- Global Initialization:
- ISS IPIPE Register Summary: [1]

Table 8-713. IPIPE_LSC_SHF

Address Offset	0x0000 00D0		
Physical Address	0x5201 08D0	**Instance**	ISS_IPIPE
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:4	RESERVED		R	0x000
3:0	VAL	LSC SHV	RW	0x0

Table 8-714. Register Call Summary for Register IPIPE_LSC_SHF

ISS ISP
- Global Initialization:
- ISS IPIPE Register Summary: [2]

Table 8-715. IPIPE_LSC_MAX

Address Offset	0x0000 00D4		
Physical Address	0x5201 08D4	**Instance**	ISS_IPIPE
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:9	RESERVED		R	0x00
8:0	VAL	LSC MAX	RW	0x000

Table 8-716. Register Call Summary for Register IPIPE_LSC_MAX

ISS ISP
- Global Initialization:
- ISS IPIPE Register Summary: [2]

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Table 8-717. IPIPE_WB2_OFT_R

Address Offset	0x0000 01D0		
Physical Address	0x5201 09D0	**Instance**	ISS_IPIPE
Description	White Balance Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED				VAL											

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	RESERVED		R	0x0
11:0	VAL	Offset before white balance (S12) -2048 to +2047	RW	0x000

Table 8-718. Register Call Summary for Register IPIPE_WB2_OFT_R

ISS ISP

- ISS ISP IPIPE White Balance: [0]
- Global Initialization: [1]
- ISS IPIPE Register Summary: [2]

Table 8-719. IPIPE_WB2_OFT_GR

Address Offset	0x0000 01D4		
Physical Address	0x5201 09D4	**Instance**	ISS_IPIPE
Description	White Balance Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED				VAL											

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	RESERVED		R	0x0
11:0	VAL	Offset before white balance (S12) -2048 to +2047	RW	0x000

Table 8-720. Register Call Summary for Register IPIPE_WB2_OFT_GR

ISS ISP

- Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

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Table 8-721. IPIPE_WB2_OFT_GB

Address Offset	0x0000 01D8		
Physical Address	0x5201 09D8	**Instance**	ISS_IPIPE
Description	White Balance Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED				VAL											

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	RESERVED		R	0x0
11:0	VAL	Offset before white balance (S12) -2048 to +2047	RW	0x000

Table 8-722. Register Call Summary for Register IPIPE_WB2_OFT_GB

ISS ISP

- Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-723. IPIPE_WB2_OFT_B

Address Offset	0x0000 01DC		
Physical Address	0x5201 09DC	**Instance**	ISS_IPIPE
Description	White Balance Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED				VAL											

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	RESERVED		R	0x0
11:0	VAL	Offset before white balance (S12) -2048 to +2047	RW	0x000

Table 8-724. Register Call Summary for Register IPIPE_WB2_OFT_B

ISS ISP

- Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

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Table 8-725. IPIPE_WB2_WGN_R

Address Offset	0x0000 01E0		
Physical Address	0x5201 09E0	**Instance**	ISS_IPIPE
Description	White Balance Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12:0	VAL	White balance gain for R in U4.9 format 0 to +15.998	RW	0x0200

Table 8-726. Register Call Summary for Register IPIPE_WB2_WGN_R

ISS ISP

- ISS ISP IPIPE White Balance: [0]
- Global Initialization: [1]
- ISS IPIPE Register Summary: [2]

Table 8-727. IPIPE_WB2_WGN_GR

Address Offset	0x0000 01E4		
Physical Address	0x5201 09E4	**Instance**	ISS_IPIPE
Description	White Balance Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12:0	VAL	White balance gain for Gr in U4.9 format 0 to +15.998	RW	0x0200

Table 8-728. Register Call Summary for Register IPIPE_WB2_WGN_GR

ISS ISP

- Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

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Table 8-729. IPIPE_WB2_WGN_GB

Address Offset	0x0000 01E8		
Physical Address	0x5201 09E8	**Instance**	ISS_IPIPE
Description	White Balance Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12:0	VAL	White balance gain for Gb in U4.9 format 0 to +15.998	RW	0x0200

Table 8-730. Register Call Summary for Register IPIPE_WB2_WGN_GB

ISS ISP

- Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-731. IPIPE_WB2_WGN_B

Address Offset	0x0000 01EC		
Physical Address	0x5201 09EC	**Instance**	ISS_IPIPE
Description	White Balance Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12:0	VAL	White balance gain for B in U4.9 format 0 to +15.998	RW	0x0200

Table 8-732. Register Call Summary for Register IPIPE_WB2_WGN_B

ISS ISP

- Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

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Table 8-733. IPIPE_RGB1_MUL_RR

Address Offset	0x0000 022C		
Physical Address	0x5201 0A2C	**Instance**	ISS_IPIPE
Description	RGB to RGB Conversion Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED				VAL											

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	RESERVED		R	0x0
11:0	VAL	The matrix coefficient. 011111111111 = 2047/256 = 7.99609375 011111111110 = 2046/256 [...] 000011111111 = 255/256 000100000000 = 256/256 = 1 000100000001 = 257/256 [...] 000000000001 = 1/256 000000000000 = 0/256 = 0 111111111111 = -1/256 = -0.00390625 111111111110 = -2/256 [...] 100000000001 = -2047/256 100000000000 = -2048/256 = -8.	RW	0x100

Table 8-734. Register Call Summary for Register IPIPE_RGB1_MUL_RR

ISS ISP

- ISS ISP IPIPE RGB2RGB Blending Module: [0]
- Global Initialization: [1]
- ISS IPIPE Register Summary: [2]

Table 8-735. IPIPE_RGB1_MUL_GR

Address Offset	0x0000 0230		
Physical Address	0x5201 0A30	**Instance**	ISS_IPIPE
Description	RGB to RGB Conversion Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED				VAL											

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	RESERVED		R	0x0
11:0	VAL	The matrix coefficient.	RW	0x000

Table 8-736. Register Call Summary for Register IPIPE_RGB1_MUL_GR

ISS ISP

- Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

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Table 8-737. IPIPE_RGB1_MUL_BR

Address Offset	0x0000 0234		
Physical Address	0x5201 0A34	**Instance**	ISS_IPIPE
Description	RGB to RGB Conversion Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED				VAL											

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	RESERVED		R	0x0
11:0	VAL	The matrix coefficient.	RW	0x000

Table 8-738. Register Call Summary for Register IPIPE_RGB1_MUL_BR

ISS ISP

- Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-739. IPIPE_RGB1_MUL_RG

Address Offset	0x0000 0238		
Physical Address	0x5201 0A38	**Instance**	ISS_IPIPE
Description	RGB to RGB Conversion Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED				VAL											

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	RESERVED		R	0x0
11:0	VAL	The matrix coefficient.	RW	0x000

Table 8-740. Register Call Summary for Register IPIPE_RGB1_MUL_RG

ISS ISP

- Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-741. IPIPE_RGB1_MUL_GG

Address Offset	0x0000 023C		
Physical Address	0x5201 0A3C	**Instance**	ISS_IPIPE
Description	RGB to RGB Conversion Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED				VAL											

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Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	RESERVED		R	0x0
11:0	VAL	The matrix coefficient.	RW	0x100

Table 8-742. Register Call Summary for Register IPIPE_RGB1_MUL_GG

ISS ISP
- Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-743. IPIPE_RGB1_MUL_BG

Address Offset	0x0000 0240		
Physical Address	0x5201 0A40	**Instance**	ISS_IPIPE
Description	RGB to RGB Conversion Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	RESERVED		R	0x0
11:0	VAL	The matrix coefficient.	RW	0x000

Table 8-744. Register Call Summary for Register IPIPE_RGB1_MUL_BG

ISS ISP
- Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-745. IPIPE_RGB1_MUL_RB

Address Offset	0x0000 0244		
Physical Address	0x5201 0A44	**Instance**	ISS_IPIPE
Description	RGB to RGB Conversion Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	RESERVED		R	0x0
11:0	VAL	The matrix coefficient.	RW	0x000

Table 8-746. Register Call Summary for Register IPIPE_RGB1_MUL_RB

ISS ISP
- Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

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Table 8-747. IPIPE_RGB1_MUL_GB

Address Offset	0x0000 0248		
Physical Address	0x5201 0A48	**Instance**	ISS_IPIPE
Description	RGB to RGB Conversion Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED				VAL											

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	RESERVED		R	0x0
11:0	VAL	The matrix coefficient.	RW	0x000

Table 8-748. Register Call Summary for Register IPIPE_RGB1_MUL_GB

ISS ISP

- Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-749. IPIPE_RGB1_MUL_BB

Address Offset	0x0000 024C		
Physical Address	0x5201 0A4C	**Instance**	ISS_IPIPE
Description	RGB to RGB Conversion Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED				VAL											

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	RESERVED		R	0x0
11:0	VAL	The matrix coefficient.	RW	0x100

Table 8-750. Register Call Summary for Register IPIPE_RGB1_MUL_BB

ISS ISP

- ISS ISP IPIPE RGB2RGB Blending Module: [0]
- Global Initialization: [1]
- ISS IPIPE Register Summary: [2]

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Table 8-751. IPIPE_RGB1_OFT_OR

Address Offset	0x0000 0250		
Physical Address	0x5201 0A50	**Instance**	ISS_IPIPE
Description	RGB to RGB Conversion Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12:0	VAL	The output offset value for R. (s13) -4096 to +4095	RW	0x0000

Table 8-752. Register Call Summary for Register IPIPE_RGB1_OFT_OR

ISS ISP

- ISS ISP IPIPE RGB2RGB Blending Module: [0]
- Global Initialization: [1]
- ISS IPIPE Register Summary: [2]

Table 8-753. IPIPE_RGB1_OFT_OG

Address Offset	0x0000 0254		
Physical Address	0x5201 0A54	**Instance**	ISS_IPIPE
Description	RGB to RGB Conversion Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12:0	VAL	The output offset value for G. (s13) -4096 to +4095	RW	0x0000

Table 8-754. Register Call Summary for Register IPIPE_RGB1_OFT_OG

ISS ISP

- Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

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Table 8-755. IPIPE_RGB1_OFT_OB

Address Offset	0x0000 0258		
Physical Address	0x5201 0A58	**Instance**	ISS_IPIPE
Description	RGB to RGB Conversion Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12:0	VAL	The output offset value for B. (s13) -4096 to +4095	RW	0x0000

Table 8-756. Register Call Summary for Register IPIPE_RGB1_OFT_OB

ISS ISP

- ISS ISP IPIPE RGB2RGB Blending Module: [0]
- Global Initialization: [1]
- ISS IPIPE Register Summary: [2]

Table 8-757. IPIPE_GMM_CFG

Address Offset	0x0000 025C		
Physical Address	0x5201 0A5C	**Instance**	ISS_IPIPE
Description	RGB to RGB Conversion Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								SIZ		TBL	RESERVED	BYPB	BYPG	BYPR	

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:7	RESERVED		R	0x000
6:5	SIZ	The size of the gamma table. 0x0: 64 words 0x1: 128 words 0x3: 512 words 0x2: 256 words	RW	0x3
4	TBL	Selection of Gamma table. 0x0: RAM 0x1: ROM	RW	0
3	RESERVED		RW	0

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Bits	Field Name	Description	Type	Reset
2	BYPB	Gamma correction mode for B 0x0: Not bypassed 0x1: Bypassed	RW	1
1	BYPG	Gamma correction mode for G 0x0: Not bypassed 0x1: Bypassed	RW	1
0	BYPR	Gamma correction mode for R 0x0: Not bypassed 0x1: Bypassed	RW	1

Table 8-758. Register Call Summary for Register IPIPE_GMM_CFG

ISS ISP
- ISS ISP IPIPE Gamma Correction Module: [0] [1] [2] [3]
- Global Initialization: [4] [5] [6] [7] [8]
- ISS IPIPE Register Summary: [9]

Table 8-759. IPIPE_RGB2_MUL_RR

Address Offset	0x0000 0260		
Physical Address	0x5201 0A60	**Instance**	ISS_IPIPE
Description	RGB to RGB conversion after gamma		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED					VAL										

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:11	RESERVED		R	0x00
10:0	VAL	The matrix coefficient. 011111111111 = 2047/256 = 7.99609375 011111111110 = 2046/256 000011111111 = 255/256 000100000000 = 256/256 = 1 000100000001 = 257/256 000000000001 = 1/256 000000000000 = 0/256 = 0 111111111111 = -1/256 = -0.00390625 111111111110 = -2/256 100000000001 = -2047/256 100000000000 = -2048/256 = -8.	RW	0x100

Table 8-760. Register Call Summary for Register IPIPE_RGB2_MUL_RR

ISS ISP
- ISS ISP IPIPE 2nd RGB2RGB Conversion Matrix: [0]
- Global Initialization: [1]
- ISS IPIPE Register Summary: [2]

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Table 8-761. IPIPE_RGB2_MUL_GR

Address Offset	0x0000 0264		
Physical Address	0x5201 0A64	**Instance**	ISS_IPIPE
Description	RGB to RGB conversion after gamma		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:11	RESERVED		R	0x00
10:0	VAL	The matrix coefficient.	RW	0x000

Table 8-762. Register Call Summary for Register IPIPE_RGB2_MUL_GR

ISS ISP

- Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-763. IPIPE_RGB2_MUL_BR

Address Offset	0x0000 0268		
Physical Address	0x5201 0A68	**Instance**	ISS_IPIPE
Description	RGB to RGB conversion after gamma		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:11	RESERVED		R	0x00
10:0	VAL	The matrix coefficient.	RW	0x000

Table 8-764. Register Call Summary for Register IPIPE_RGB2_MUL_BR

ISS ISP

- Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-765. IPIPE_RGB2_MUL_RG

Address Offset	0x0000 026C		
Physical Address	0x5201 0A6C	**Instance**	ISS_IPIPE
Description	RGB to RGB conversion after gamma		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

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Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:11	RESERVED		R	0x00
10:0	VAL	The matrix coefficient.	RW	0x000

Table 8-766. Register Call Summary for Register IPIPE_RGB2_MUL_RG

ISS ISP
- Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-767. IPIPE_RGB2_MUL_GG

Address Offset	0x0000 0270		
Physical Address	0x5201 0A70	**Instance**	ISS_IPIPE
Description	RGB to RGB conversion after gamma		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:11	RESERVED		R	0x00
10:0	VAL	The matrix coefficient.	RW	0x100

Table 8-768. Register Call Summary for Register IPIPE_RGB2_MUL_GG

ISS ISP
- Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-769. IPIPE_RGB2_MUL_BG

Address Offset	0x0000 0274		
Physical Address	0x5201 0A74	**Instance**	ISS_IPIPE
Description	RGB to RGB conversion after gamma		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:11	RESERVED		R	0x00
10:0	VAL	The matrix coefficient.	RW	0x000

Table 8-770. Register Call Summary for Register IPIPE_RGB2_MUL_BG

ISS ISP
- Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

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Table 8-771. IPIPE_RGB2_MUL_RB

Address Offset	0x0000 0278		
Physical Address	0x5201 0A78	**Instance**	ISS_IPIPE
Description	RGB to RGB conversion after gamma		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:11	RESERVED		R	0x00
10:0	VAL	The matrix coefficient.	RW	0x000

Table 8-772. Register Call Summary for Register IPIPE_RGB2_MUL_RB

ISS ISP

- Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-773. IPIPE_RGB2_MUL_GB

Address Offset	0x0000 027C		
Physical Address	0x5201 0A7C	**Instance**	ISS_IPIPE
Description	RGB to RGB conversion after gamma		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:11	RESERVED		R	0x00
10:0	VAL	The matrix coefficient.	RW	0x000

Table 8-774. Register Call Summary for Register IPIPE_RGB2_MUL_GB

ISS ISP

- Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-775. IPIPE_RGB2_MUL_BB

Address Offset	0x0000 0280		
Physical Address	0x5201 0A80	**Instance**	ISS_IPIPE
Description	RGB to RGB conversion after gamma		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

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Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:11	RESERVED		R	0x00
10:0	VAL	The matrix coefficient.	RW	0x100

Table 8-776. Register Call Summary for Register IPIPE_RGB2_MUL_BB

ISS ISP

- ISS ISP IPIPE 2nd RGB2RGB Conversion Matrix: [0]
- Global Initialization: [1]
- ISS IPIPE Register Summary: [2]

Table 8-777. IPIPE_RGB2_OFT_OR

Address Offset	0x0000 0284		
Physical Address	0x5201 0A84	**Instance**	ISS_IPIPE
Description	RGB to RGB conversion after gamma		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:11	RESERVED		R	0x00
10:0	VAL	The output offset value for R S10 number: -1024 to + 1023	RW	0x000

Table 8-778. Register Call Summary for Register IPIPE_RGB2_OFT_OR

ISS ISP

- ISS ISP IPIPE 2nd RGB2RGB Conversion Matrix: [0]
- Global Initialization: [1]
- ISS IPIPE Register Summary: [2]

Table 8-779. IPIPE_RGB2_OFT_OG

Address Offset	0x0000 0288		
Physical Address	0x5201 0A88	**Instance**	ISS_IPIPE
Description	RGB to RGB conversion after gamma		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:11	RESERVED		R	0x00
10:0	VAL	The output offset value for G S10 number: -1024 to + 1023	RW	0x000

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Table 8-780. Register Call Summary for Register IPIPE_RGB2_OFT_OG

ISS ISP

- Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-781. IPIPE_RGB2_OFT_OB

Address Offset	0x0000 028C		
Physical Address	0x5201 0A8C	**Instance**	ISS_IPIPE
Description	RGB to RGB conversion after gamma		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED					VAL										

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:11	RESERVED		R	0x00
10:0	VAL	The output offset value for B S10 number: -1024 to + 1023	RW	0x000

Table 8-782. Register Call Summary for Register IPIPE_RGB2_OFT_OB

ISS ISP

- ISS ISP IPIPE 2nd RGB2RGB Conversion Matrix: [0]
- Global Initialization: [1]
- ISS IPIPE Register Summary: [2]

Table 8-783. IPIPE_YUV_ADJ

Address Offset	0x0000 0294		
Physical Address	0x5201 0A94	**Instance**	ISS_IPIPE
Description	RGB to YUV Conversion Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																BRT								CRT							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:8	BRT	The offset value for brightness control.	RW	0x00
7:0	CRT	The multiplier coefficient value for contrast control. 00000000 = 0/16 = 0 00000001 = 1/16 00001111 = 15/16 00010000 = 16/16 = 1 00010001 = 17/16 11111110 = 254/16 11111111 = 255/16 = 15.9375	RW	0x10

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Table 8-784. Register Call Summary for Register IPIPE_YUV_ADJ

ISS ISP

- ISS ISP IPIPE RGB2YCbCr Conversion Matrix: [0] [1]
- Global Initialization: [2] [3]
- ISS IPIPE Register Summary: [4]

Table 8-785. IPIPE_YUV_MUL_RY

Address Offset	0x0000 0298		
Physical Address	0x5201 0A98	**Instance**	ISS_IPIPE
Description	RGB to YUV Conversion Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED				VAL											

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	RESERVED		R	0x0
11:0	VAL	Matrix Coefficient for RY (S4.8 = -8 - +7.996)	RW	0x04D

Table 8-786. Register Call Summary for Register IPIPE_YUV_MUL_RY

ISS ISP

- ISS ISP IPIPE RGB2YCbCr Conversion Matrix: [0]
- Global Initialization: [1]
- ISS IPIPE Register Summary: [2]

Table 8-787. IPIPE_YUV_MUL_GY

Address Offset	0x0000 029C		
Physical Address	0x5201 0A9C	**Instance**	ISS_IPIPE
Description	RGB to YUV Conversion Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED				VAL											

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	RESERVED		R	0x0
11:0	VAL	Matrix Coefficient for GY (S4.8 = -8 - +7.996)	RW	0x096

Table 8-788. Register Call Summary for Register IPIPE_YUV_MUL_GY

ISS ISP

- Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

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Table 8-789. IPIPE_YUV_MUL_BY

Address Offset	0x0000 02A0		
Physical Address	0x5201 0AA0	**Instance**	ISS_IPIPE
Description	RGB to YUV Conversion Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED				VAL											

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	RESERVED		R	0x0
11:0	VAL	Matrix Coefficient for BY (S4.8 = -8 - +7.996)	RW	0x01D

Table 8-790. Register Call Summary for Register IPIPE_YUV_MUL_BY

ISS ISP

- Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-791. IPIPE_YUV_MUL_RCB

Address Offset	0x0000 02A4		
Physical Address	0x5201 0AA4	**Instance**	ISS_IPIPE
Description	RGB to YUV Conversion Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED				VAL											

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	RESERVED		R	0x0
11:0	VAL	The matrix coefficient.	RW	0xFD5

Table 8-792. Register Call Summary for Register IPIPE_YUV_MUL_RCB

ISS ISP

- Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

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Table 8-793. IPIPE_YUV_MUL_GCB

Address Offset	0x0000 02A8		
Physical Address	0x5201 0AA8	**Instance**	ISS_IPIPE
Description	RGB to YUV Conversion Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED				VAL											

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	RESERVED		R	0x0
11:0	VAL	The matrix coefficient.	RW	0xFAB

Table 8-794. Register Call Summary for Register IPIPE_YUV_MUL_GCB

ISS ISP

- Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-795. IPIPE_YUV_MUL_BCB

Address Offset	0x0000 02AC		
Physical Address	0x5201 0AAC	**Instance**	ISS_IPIPE
Description	RGB to YUV Conversion Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED				VAL											

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	RESERVED		R	0x0
11:0	VAL	The matrix coefficient.	RW	0x080

Table 8-796. Register Call Summary for Register IPIPE_YUV_MUL_BCB

ISS ISP

- Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-797. IPIPE_YUV_MUL_RCR

Address Offset	0x0000 02B0		
Physical Address	0x5201 0AB0	**Instance**	ISS_IPIPE
Description	RGB to YUV Conversion Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED				VAL											

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Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	RESERVED		R	0x0
11:0	VAL	The matrix coefficient.	RW	0x080

Table 8-798. Register Call Summary for Register IPIPE_YUV_MUL_RCR

ISS ISP
- Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-799. IPIPE_YUV_MUL_GCR

Address Offset	0x0000 02B4		
Physical Address	0x5201 0AB4	**Instance**	ISS_IPIPE
Description	RGB to YUV Conversion Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	RESERVED		R	0x0
11:0	VAL	The matrix coefficient.	RW	0xF95

Table 8-800. Register Call Summary for Register IPIPE_YUV_MUL_GCR

ISS ISP
- Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-801. IPIPE_YUV_MUL_BCR

Address Offset	0x0000 02B8		
Physical Address	0x5201 0AB8	**Instance**	ISS_IPIPE
Description	RGB to YUV Conversion Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	RESERVED		R	0x0
11:0	VAL	The matrix coefficient.	RW	0xFEB

Table 8-802. Register Call Summary for Register IPIPE_YUV_MUL_BCR

ISS ISP
- Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

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Table 8-803. IPIPE_YUV_OFT_Y

Address Offset	0x0000 02BC		
Physical Address	0x5201 0ABC	**Instance**	ISS_IPIPE
Description	RGB to YUV Conversion Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:11	RESERVED		R	0x00
10:0	VAL	The output offset value for Y	RW	0x000

Table 8-804. Register Call Summary for Register IPIPE_YUV_OFT_Y

ISS ISP

- ISS ISP IPIPE RGB2YCbCr Conversion Matrix: [0]
- Global Initialization: [1]
- ISS IPIPE Register Summary: [2]

Table 8-805. IPIPE_YUV_OFT_CB

Address Offset	0x0000 02C0		
Physical Address	0x5201 0AC0	**Instance**	ISS_IPIPE
Description	RGB to YUV Conversion Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:11	RESERVED		R	0x00
10:0	VAL	The output offset value for Cb For Cb/Cr, set (0x80 + offset value) here. (0x80 for zero offset.)	RW	0x080

Table 8-806. Register Call Summary for Register IPIPE_YUV_OFT_CB

ISS ISP

- Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

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Table 8-807. IPIPE_YUV_OFT_CR

Address Offset	0x0000 02C4		
Physical Address	0x5201 0AC4	**Instance**	ISS_IPIPE
Description	RGB to YUV Conversion Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:11	RESERVED		R	0x00
10:0	VAL	The output offset value for Cr For Cb/Cr, set (0x80 + offset value) here. (0x80 for zero offset.)	RW	0x080

Table 8-808. Register Call Summary for Register IPIPE_YUV_OFT_CR

ISS ISP

- Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-809. IPIPE_YUV_PHS

Address Offset	0x0000 02C8		
Physical Address	0x5201 0AC8	**Instance**	ISS_IPIPE
Description	YUV4:2:2 down sampling register. This register controls the YUV4:4:4 to YUV4:2:2 chroma downsampling. This register is valid if IPIPE_SRC_FMT.FMT = 0 (RAW input and YUV output). IPIPE_YUV_PHS = 0 leads to pure subsampling, no filtering, cosited chroma output. IPIPE_YUV_PHS = 1 leads to (1, 1) 1 filtering, centered chroma output. IPIPE_YUV_PHS = 2 leads to (1, 2, 1) 1 filtering, cosited chroma output. IPIPE_YUV_PHS = 3 leads to (1, 3, 3, 1) 3 filtering, centered chroma output. When the chroma output is cosited, and that downsampling is enabled in the RESIZER module, one need to take care that the averager disrupts the relative phase for luma and chroma color components. The RZA_H_PHS_ADJ and RZB_H_PHS_ADJ registers need to be used to fix the disruption.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED														LPF	POS

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:2	RESERVED		R	0x0000
1	LPF	121-LPF enable for chrominance samples. This register is valid if IPIPE_SRC_FMT.FMT = 0 (RAW input and YUV output). 0x0: off 0x1: on	RW	0

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Bits	Field Name	Description	Type	Reset
0	POS	This bit sets the output position of the chrominance sample with regards to the luma sample positions. One can choose between centered and cosited. This register is valid if IPIPE_SRC_FMT.FMT = 0 (RAW input and YUV output). The RESIZER module does not change the relative position of the chroma samples vs. the luma samples between the input and output and the chroma position at the output of the IPIPE module and at the output of the RESIZER module must be identical. In other words, we must have RSZ_YUV_PHS.POS = IPIPE_YUV_PHS.POS. 0x0: Cosited = same position with luminance 0x1: Centered = middle of the luminance	RW	0

Table 8-810. Register Call Summary for Register IPIPE_YUV_PHS

ISS ISP

- ISS ISP IPIPE 4:2:2 Conversion Module: [0] [1]
- ISS ISP RSZ Functional Description: [2]
- Global Initialization: [3] [4]
- ISS RESIZER Register Description: [5]
- ISS IPIPE Register Summary: [6]
- ISS IPIPE Register Description: [7] [8] [9] [10] [11]

Table 8-811. IPIPE_YEE_EN

Address Offset	0x0000 02D4		
Physical Address	0x5201 0AD4	**Instance**	ISS_IPIPE
Description	Edge Enhancer Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED															EN

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:1	RESERVED		R	0x0000
0	EN	The on/off selection of the Edge enhancer. 0x0: Disable 0x1: Enable	RW	0

Table 8-812. Register Call Summary for Register IPIPE_YEE_EN

ISS ISP

- ISS ISP IPIPE 2D Edge Enhancer: [0]
- Global Initialization: [1]
- ISS IPIPE Register Summary: [2]

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Table 8-813. IPIPE_YEE_TYP

Address Offset	0x0000 02D8		
Physical Address	0x5201 0AD8	**Instance**	ISS_IPIPE
Description	Edge Enhancer Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED														HAL	SEL

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:2	RESERVED		R	0x0000
1	HAL	Halo reduction in Edge Sharpener module	RW	0
0	SEL	Merging method between Edge Enhancer and Edge Sharpener 0x0: EE + ES 0x1: Maximum (EE, ES)	RW	0

Table 8-814. Register Call Summary for Register IPIPE_YEE_TYP

ISS ISP

- ISS ISP IPIPE 2D Edge Enhancer: [0] [1]
- Global Initialization: [2]
- ISS IPIPE Register Summary: [3]

Table 8-815. IPIPE_YEE_SHF

Address Offset	0x0000 02DC		
Physical Address	0x5201 0ADC	**Instance**	ISS_IPIPE
Description	Edge Enhancer Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED												SHF			

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:4	RESERVED		R	0x000
3:0	SHF	Down shift length of high pass filter (HPF) in edge enhancer.	RW	0x0

Table 8-816. Register Call Summary for Register IPIPE_YEE_SHF

ISS ISP

- ISS ISP IPIPE 2D Edge Enhancer: [0]
- Global Initialization: [1]
- ISS IPIPE Register Summary: [2]

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Table 8-817. IPIPE_YEE_MUL_00

Address Offset	0x0000 02E0		
Physical Address	0x5201 0AE0	**Instance**	ISS_IPIPE
Description	Edge Enhancer Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:10	RESERVED		R	0x00
9:0	VAL	Multiplier coefficient in HPF. 0111111111 = 511 0111111110 = 510 0000000001 = 1 0000000000 = 0 1111111111 = -1 1000000001 = -511 1000000000 = -512	RW	0x000

Table 8-818. Register Call Summary for Register IPIPE_YEE_MUL_00

ISS ISP

- Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-819. IPIPE_YEE_MUL_01

Address Offset	0x0000 02E4		
Physical Address	0x5201 0AE4	**Instance**	ISS_IPIPE
Description	Edge Enhancer Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:10	RESERVED		R	0x00
9:0	VAL	Multiplier coefficient in HPF.	RW	0x000

Table 8-820. Register Call Summary for Register IPIPE_YEE_MUL_01

ISS ISP

- Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

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Table 8-821. IPIPE_YEE_MUL_02

Address Offset	0x0000 02E8		
Physical Address	0x5201 0AE8	**Instance**	ISS_IPIPE
Description	Edge Enhancer Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:10	RESERVED		R	0x00
9:0	VAL	Multiplier coefficient in HPF.	RW	0x000

Table 8-822. Register Call Summary for Register IPIPE_YEE_MUL_02

ISS ISP

- Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-823. IPIPE_YEE_MUL_10

Address Offset	0x0000 02EC		
Physical Address	0x5201 0AEC	**Instance**	ISS_IPIPE
Description	Edge Enhancer Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:10	RESERVED		R	0x00
9:0	VAL	Multiplier coefficient in HPF.	RW	0x000

Table 8-824. Register Call Summary for Register IPIPE_YEE_MUL_10

ISS ISP

- Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-825. IPIPE_YEE_MUL_11

Address Offset	0x0000 02F0		
Physical Address	0x5201 0AF0	**Instance**	ISS_IPIPE
Description	Edge Enhancer Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

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Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:10	RESERVED		R	0x00
9:0	VAL	Multiplier coefficient in HPF.	RW	0x000

Table 8-826. Register Call Summary for Register IPIPE_YEE_MUL_11

ISS ISP
- Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-827. IPIPE_YEE_MUL_12

Address Offset	0x0000 02F4		
Physical Address	0x5201 0AF4	**Instance**	ISS_IPIPE
Description	Edge Enhancer Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:10	RESERVED		R	0x00
9:0	VAL	Multiplier coefficient in HPF.	RW	0x000

Table 8-828. Register Call Summary for Register IPIPE_YEE_MUL_12

ISS ISP
- Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-829. IPIPE_YEE_MUL_20

Address Offset	0x0000 02F8		
Physical Address	0x5201 0AF8	**Instance**	ISS_IPIPE
Description	Edge Enhancer Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:10	RESERVED		R	0x00
9:0	VAL	Multiplier coefficient in HPF.	RW	0x000

Table 8-830. Register Call Summary for Register IPIPE_YEE_MUL_20

ISS ISP
- Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

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Table 8-831. IPIPE_YEE_MUL_21

Address Offset	0x0000 02FC		
Physical Address	0x5201 0AFC	**Instance**	ISS_IPIPE
Description	Edge Enhancer Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:10	RESERVED		R	0x00
9:0	VAL	Multiplier coefficient in HPF.	RW	0x000

Table 8-832. Register Call Summary for Register IPIPE_YEE_MUL_21

ISS ISP

- Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-833. IPIPE_YEE_MUL_22

Address Offset	0x0000 0300		
Physical Address	0x5201 0B00	**Instance**	ISS_IPIPE
Description	Edge Enhancer Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:10	RESERVED		R	0x00
9:0	VAL	Multiplier coefficient in HPF.	RW	0x000

Table 8-834. Register Call Summary for Register IPIPE_YEE_MUL_22

ISS ISP

- Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-835. IPIPE_YEE_THR

Address Offset	0x0000 0304		
Physical Address	0x5201 0B04	**Instance**	ISS_IPIPE
Description	Edge Enhancer Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED														VAL	

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Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:6	RESERVED		R	0x000
5:0	VAL	Edge Enhancer lower threshold before referring to LUT. If HPF -IPIPE_YEE_THR - output is HPF + IPIPE_YEE_THR If HPF IPIPE_YEE_THR - output is HPF - IPIPE_YEE_THR Otherwise, output is zero.	RW	0x00

Table 8-836. Register Call Summary for Register IPIPE_YEE_THR

ISS ISP
- ISS ISP IPIPE 2D Edge Enhancer: [0]
- Global Initialization: [1]
- ISS IPIPE Register Summary: [2]
- ISS IPIPE Register Description: [3] [4] [5] [6]

Table 8-837. IPIPE_YEE_E_GAN

Address Offset	0x0000 0308		
Physical Address	0x5201 0B08	**Instance**	ISS_IPIPE
Description	Edge Enhancer Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED				VAL											

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	RESERVED		R	0x0
11:0	VAL	Edge sharpener gain	RW	0x000

Table 8-838. Register Call Summary for Register IPIPE_YEE_E_GAN

ISS ISP
- ISS ISP IPIPE 2D Edge Enhancer: [0]
- Global Initialization: [1]
- ISS IPIPE Register Summary: [2]

Table 8-839. IPIPE_YEE_E_THR_1

Address Offset	0x0000 030C		
Physical Address	0x5201 0B0C	**Instance**	ISS_IPIPE
Description	Edge Enhancer Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED				VAL											

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	RESERVED		R	0x0
11:0	VAL	Edge sharpener HPF value lower limit	RW	0x000

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Table 8-840. Register Call Summary for Register IPIPE_YEE_E_THR_1

ISS ISP
- Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-841. IPIPE_YEE_E_THR_2

Address Offset	0x0000 0310		
Physical Address	0x5201 0B10	**Instance**	ISS_IPIPE
Description	Edge Enhancer Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:6	RESERVED		R	0x000
5:0	VAL	Edge sharpener HPF value upper limit (after 6 bit right shift)	RW	0x00

Table 8-842. Register Call Summary for Register IPIPE_YEE_E_THR_2

ISS ISP
- Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-843. IPIPE_YEE_G_GAN

Address Offset	0x0000 0314		
Physical Address	0x5201 0B14	**Instance**	ISS_IPIPE
Description	Edge Enhancer Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:8	RESERVED		R	0x00
7:0	VAL	Edge sharpener, gain value on gradient	RW	0x00

Table 8-844. Register Call Summary for Register IPIPE_YEE_G_GAN

ISS ISP
- ISS ISP IPIPE 2D Edge Enhancer: [0]
- Global Initialization: [1]
- ISS IPIPE Register Summary: [2]

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Table 8-845. IPIPE_YEE_G_OFT

Address Offset	0x0000 0318		
Physical Address	0x5201 0B18	**Instance**	ISS_IPIPE
Description	Edge Enhancer Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:6	RESERVED		R	0x000
5:0	VAL	Edge sharpener, offset value on gradient	RW	0x00

Table 8-846. Register Call Summary for Register IPIPE_YEE_G_OFT

ISS ISP

- ISS ISP IPIPE 2D Edge Enhancer: [0]
- Global Initialization: [1]
- ISS IPIPE Register Summary: [2]

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:8	RESERVED		R	0x00
7:0	VAL	The threshold of the gain function for HPF value	RW	0x00

Table 8-847. IPIPE_BOX_EN

Address Offset	0x0000 0380		
Physical Address	0x5201 0B80	**Instance**	ISS_IPIPE
Description	Boxcar Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED															EN

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:1	RESERVED		R	0x0000
0	EN	This bit enables or disables the BOXCAR functionality. The BOXCAR output is written to SDRAM. One need to set the IPIPE_BOX_SDR_SAD_H and IPIPE_BOX_SDR_SAD_L registers with the appropriate address. 0x0: Disable 0x1: Enable	RW	0

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Table 8-848. Register Call Summary for Register IPIPE_BOX_EN

ISS ISP

- ISS ISP IPIPE Boxcar: [0]
- Global Initialization: [1]
- ISS IPIPE Register Summary: [2]

Table 8-849. IPIPE_BOX_MODE

Address Offset	0x0000 0384		
Physical Address	0x5201 0B84	**Instance**	ISS_IPIPE
Description	Boxcar Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED															OST

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:1	RESERVED		R	0x0000
0	OST	The processing mode selection of the Boxcar function. A 0 indicates the mode of the free run, a 1 indicates the mode of the one shot. 0x0: Free run 0x1: One shot	RW	0

Table 8-850. Register Call Summary for Register IPIPE_BOX_MODE

ISS ISP

- ISS ISP IPIPE Boxcar: [0]
- Global Initialization: [1]
- ISS IPIPE Register Summary: [2]

Table 8-851. IPIPE_BOX_TYP

Address Offset	0x0000 0388		
Physical Address	0x5201 0B88	**Instance**	ISS_IPIPE
Description	Boxcar Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED															SEL

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:1	RESERVED		R	0x0000
0	SEL	Block size in boxcar sampling 0x0: 8x8 0x1: 16x16	RW	0

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Table 8-852. Register Call Summary for Register IPIPE_BOX_TYP

ISS ISP
- Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-853. IPIPE_BOX_SHF

Address Offset	0x0000 038C		
Physical Address	0x5201 0B8C	**Instance**	ISS_IPIPE
Description	Boxcar Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED														VAL	

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:3	RESERVED		R	0x0000
2:0	VAL	The down shift value applied to the boxcar computation result. R out = SUM (Rij) SHF G out = (SUM (Gr ij)/2 + SUM (Gr ij)/2) SHF B out = SUM (Gij) SHF	RW	0x0

Table 8-854. Register Call Summary for Register IPIPE_BOX_SHF

ISS ISP
- ISS ISP IPIPE Boxcar: [0] [1]
- Global Initialization: [2]
- ISS IPIPE Register Summary: [3]

Table 8-855. IPIPE_BOX_SDR_SAD_H

Address Offset	0x0000 0390		
Physical Address	0x5201 0B90	**Instance**	ISS_IPIPE
Description	Boxcar Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																VAL															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:0	VAL	The higher 11 bits of the first address of output in memory.	RW	0x0000

Table 8-856. Register Call Summary for Register IPIPE_BOX_SDR_SAD_H

ISS ISP
- ISS ISP IPIPE Boxcar: [0]
- Global Initialization: [1]
- ISS IPIPE Register Summary: [2]
- ISS IPIPE Register Description: [3]

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Table 8-857. IPIPE_BOX_SDR_SAD_L

Address Offset	0x0000 0394		
Physical Address	0x5201 0B94	**Instance**	ISS_IPIPE
Description	Boxcar Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																VAL														VAL_RESERVED	

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:5	VAL	The lower 16 bits of the first address of output in memory.	RW	0x000
4:0	VAL_RESERVED	Ensures 32-byte alignment.	R	0x00

Table 8-858. Register Call Summary for Register IPIPE_BOX_SDR_SAD_L

ISS ISP

- ISS ISP IPIPE Boxcar: [0]
- Global Initialization: [1]
- ISS IPIPE Register Summary: [2]
- ISS IPIPE Register Description: [3]

Table 8-859. IPIPE_HST_EN

Address Offset	0x0000 039C		
Physical Address	0x5201 0B9C	**Instance**	ISS_IPIPE
Description	Histogram		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED															EN

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:1	RESERVED		R	0x0000
0	EN	This bit enables or disables the HISTOGRAM functionality. When enabled, the HISTOGRAM computation will start the processing from the next rising edge of the VD pulse. If the processing mode of the HISTOGRAM is one shot, the enable bit will be cleared to 0 immediately after the processing has started. 0x0: disable 0x1: start/busy	RW	0

Table 8-860. Register Call Summary for Register IPIPE_HST_EN

ISS ISP

- ISS ISP IPIPE Histogram: [0] [1]
- Global Initialization: [2]
- ISS IPIPE Register Summary: [3]

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Table 8-861. IPIPE_HST_MODE

Address Offset	0x0000 03A0		
Physical Address	0x5201 0BA0	**Instance**	ISS_IPIPE
Description	Histogram		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED															OST

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:1	RESERVED		R	0x0000
0	OST	The processing mode selection of the Histogram module. A 0 indicates the mode of the free run, a 1 indicates the mode of the one shot. 0x0: Free run 0x1: One shot	RW	0

Table 8-862. Register Call Summary for Register IPIPE_HST_MODE

ISS ISP

- ISS ISP IPIPE Histogram: [0] [1]
- Global Initialization: [2]
- ISS IPIPE Register Summary: [3]

Table 8-863. IPIPE_HST_SEL

Address Offset	0x0000 03A4		
Physical Address	0x5201 0BA4	**Instance**	ISS_IPIPE
Description	Histogram		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED														SEL	TYP

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:3	RESERVED		R	0x0000
2	SEL	Input selection. When SEL0=0, RGBY are sampled from the output of the line buffer in noise filter-2. When SEL0=1, YCbCr are sampled at the output of RGB2YCbCr module. Y is sampled twice. 0x0: From noise filter input 0x1: From RGBtoYUV	RW	0
1:0	TYP	G selection in Bayer mode (SEL0=0) 0x0: Gb 0x1: Gr 0x3: Reserved 0x2: (Gb+Gr)/2	RW	0x0

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Table 8-864. Register Call Summary for Register IPIPE_HST_SEL

ISS ISP

- ISS ISP IPIPE Histogram: [0] [1]
- Global Initialization: [2] [3] [4]
- ISS IPIPE Register Summary: [5]

Table 8-865. IPIPE_HST_PARA

Address Offset	0x0000 03A8		
Physical Address	0x5201 0BA8	**Instance**	ISS_IPIPE
Description	Histogram COL0, COL1, COL2, and COL3 should be set to 1.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED		BIN		SHF				COL3	COL2	COL1	COL0	RGN3	RGN2	RGN1	RGN0

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:14	RESERVED		R	0x0
13:12	BIN	The number of the bins. 0x0: 32 0x1: 64 0x3: 256 0x2: 128	RW	0x0
11:8	SHF	The shift length of the input data. data = (INPUT SHF)	RW	0x0
7	COL3	The on/off selection of the color pattern 3 (Y). 0x0: Disable 0x1: Enable	RW	0
6	COL2	The on/off selection of the color pattern 2 (B). 0x0: Disable 0x1: Enable	RW	0
5	COL1	The on/off selection of the color pattern 1 (G). 0x0: Disable 0x1: Enable	RW	0
4	COL0	The on/off selection of the color pattern 0 (R). 0x0: Disable 0x1: Enable	RW	0
3	RGN3	The on/off selection of the region 3. 0x0: Disable 0x1: Enable	RW	0
2	RGN2	The on/off selection of the region 2. 0x0: Disable 0x1: Enable	RW	0
1	RGN1	The on/off selection of the region 1. 0x0: Disable 0x1: Enable	RW	0

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Bits	Field Name	Description	Type	Reset
0	RGN0	The on/off selection of the region 0. 0x0: Disable 0x1: Enable	RW	0

Table 8-866. Register Call Summary for Register IPIPE_HST_PARA

ISS ISP
- ISS ISP IPIPE Histogram: [0] [1] [2] [3]
- Global Initialization: [4] [5] [6] [7] [8] [9] [10] [11] [12] [13]
- ISS IPIPE Register Summary: [14]

Table 8-867. IPIPE_HST_0_VPS

Address Offset	0x0000 03AC		
Physical Address	0x5201 0BAC	**Instance**	ISS_IPIPE
Description	Histogram		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							VAL_RESERVED

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12:1	VAL	The vertical position of the region 0 from the IPIPE_SRC_VPS. The region 0 will start the Histogram processing from VAL line. VAL[0] can not be written.	RW	0x000
0	VAL_RESERVED	The vertical position of the region 0 from the IPIPE_SRC_VPS. The region 0 will start the Histogram processing from VAL line. VAL[0] can not be written.	R	0

Table 8-868. Register Call Summary for Register IPIPE_HST_0_VPS

ISS ISP
- Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

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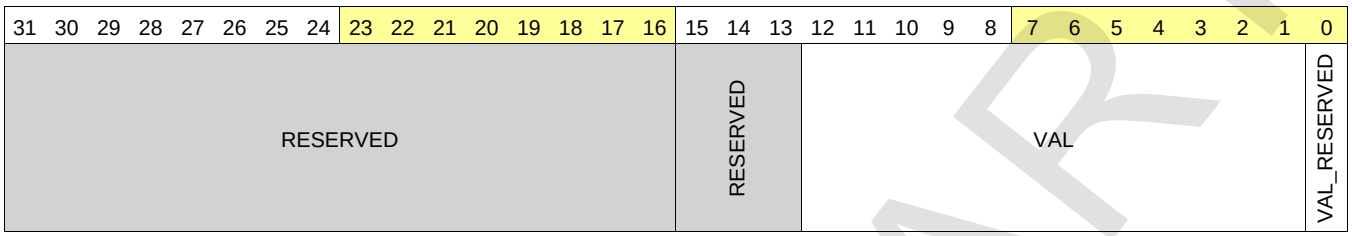
Table 8-869. IPIPE_HST_0_VSZ

Address Offset	0x0000 03B0		
Physical Address	0x5201 0BB0	**Instance**	ISS_IPIPE
Description	Histogram		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12:1	VAL	The vertical size of the region 0. The Histogram processing of the region 0 will process (VAL+1) lines.	RW	0x000
0	VAL_RESERVED	The vertical size of the region 0. The Histogram processing of the region 0 will process (VAL+1) lines. VAL[0] cannot be written.	R Rreturns 1s	1

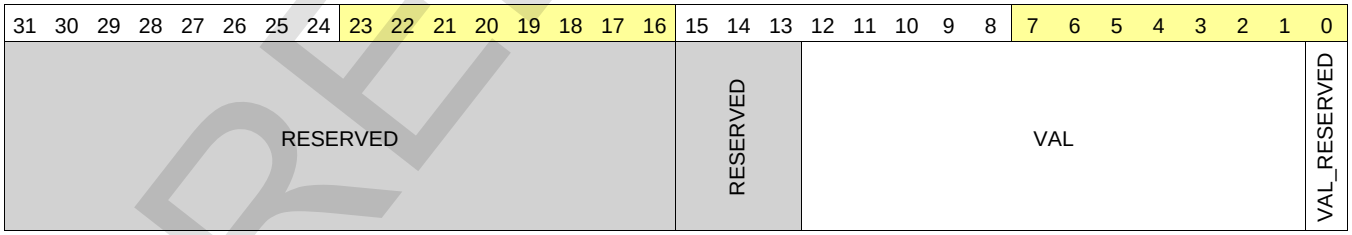
Table 8-870. Register Call Summary for Register IPIPE_HST_0_VSZ

ISS ISP

- Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-871. IPIPE_HST_0_HPS

Address Offset	0x0000 03B4		
Physical Address	0x5201 0BB4	**Instance**	ISS_IPIPE
Description	Histogram		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12:1	VAL	The horizontal position of the region 0 from the IPIPE_SRC_HPS. The region 0 will start the Histogram processing from VAL clocks. VAL[0] can not be written.	RW	0x000

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Bits	Field Name	Description	Type	Reset
0	VAL_RESERVED	The horizontal position of the region 0 from the IPIPE_SRC_HPS. The region 0 will start the Histogram processing from VAL clocks. VAL[0] can not be written.	R	0

Table 8-872. Register Call Summary for Register IPIPE_HST_0_HPS

ISS ISP
- Global Initialization: [0] [1] [2] [3]
- ISS IPIPE Register Summary: [4]

Table 8-873. IPIPE_HST_0_HSZ

Address Offset	0x0000 03B8		
Physical Address	0x5201 0BB8	**Instance**	ISS_IPIPE
Description	Histogram		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							VAL_RESERVED

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12:1	VAL	The horizontal size of the region 0. The Histogram processing of the region 0 will process (VAL+1) clocks. VAL[0] cannot be written.	RW	0x000
0	VAL_RESERVED	The horizontal size of the region 0. The Histogram processing of the region 0 will process (VAL+1) clocks. VAL[0] cannot be written.	R Rreturns 1s	1

Table 8-874. Register Call Summary for Register IPIPE_HST_0_HSZ

ISS ISP
- Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-875. IPIPE_HST_1_VPS

Address Offset	0x0000 03BC		
Physical Address	0x5201 0BBC	**Instance**	ISS_IPIPE
Description	Histogram		
Type	RW		

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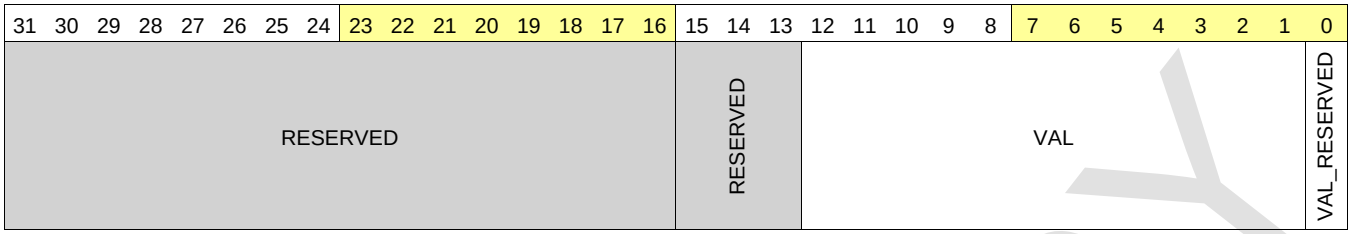


Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12:1	VAL	The vertical position of the region 0 from the IPIPE_SRC_VPS. The region 1 will start the Histogram processing from VAL line. VAL[0] can not be written.	RW	0x000
0	VAL_RESERVED	The vertical position of the region 0 from the IPIPE_SRC_VPS. The region 1 will start the Histogram processing from VAL line. VAL[0] can not be written.	R	0

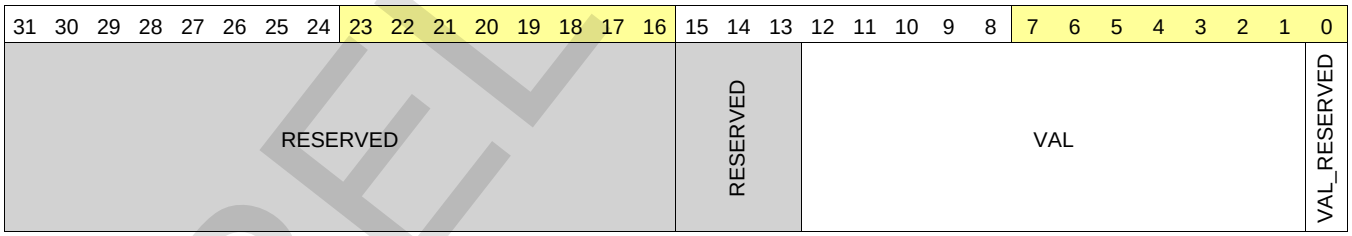
Table 8-876. Register Call Summary for Register IPIPE_HST_1_VPS

ISS ISP

- Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-877. IPIPE_HST_1_VSZ

Address Offset	0x0000 03C0		
Physical Address	0x5201 0BC0	**Instance**	ISS_IPIPE
Description	Histogram		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12:1	VAL	The vertical size of the region 1. The Histogram processing of the region 1 will process (VAL+1) lines. VAL[0] cannot be written.	RW	0x000
0	VAL_RESERVED	The vertical size of the region 1. The Histogram processing of the region 1 will process (VAL+1) lines. VAL[0] cannot be written.	R Rreturns 1s	1

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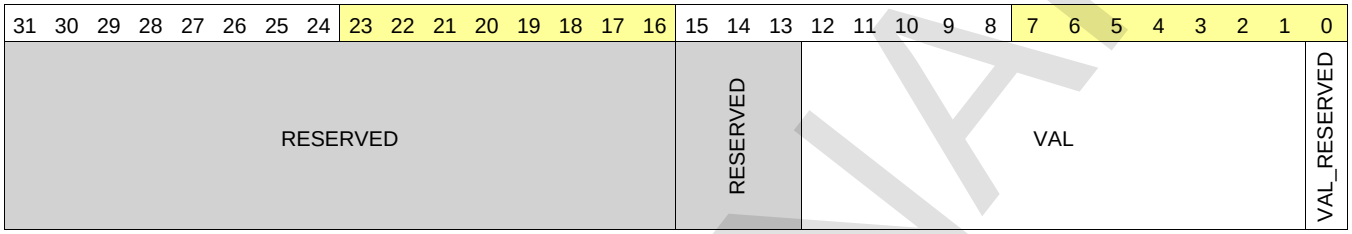
Table 8-878. Register Call Summary for Register IPIPE_HST_1_VSZ

ISS ISP

- Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-879. IPIPE_HST_1_HPS

Address Offset	0x0000 03C4		
Physical Address	0x5201 0BC4	**Instance**	ISS_IPIPE
Description	Histogram		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12:1	VAL	The horizontal position of the region 0 from the IPIPE_SRC_HPS. The region 1 will start the Histogram processing from VAL clocks. VAL[0] can not be written.	RW	0x000
0	VAL_RESERVED	The horizontal position of the region 0 from the IPIPE_SRC_HPS. The region 1 will start the Histogram processing from VAL clocks. VAL[0] can not be written.	R	0

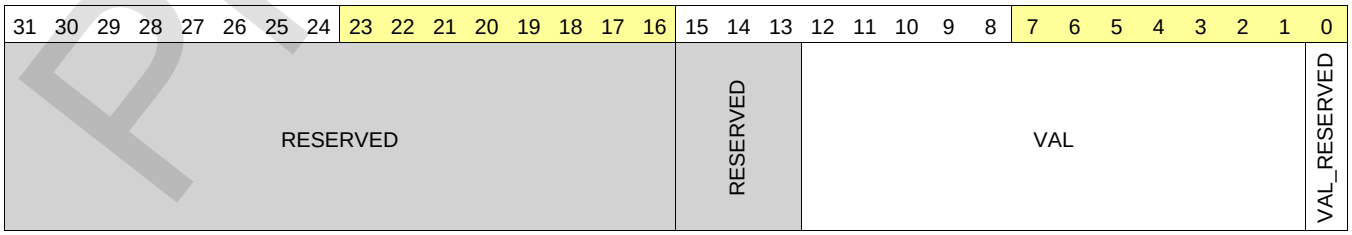
Table 8-880. Register Call Summary for Register IPIPE_HST_1_HPS

ISS ISP

- ISS IPIPE Register Summary: [0]

Table 8-881. IPIPE_HST_1_HSZ

Address Offset	0x0000 03C8		
Physical Address	0x5201 0BC8	**Instance**	ISS_IPIPE
Description	Histogram		
Type	RW		



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Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12:1	VAL	The horizontal size of the region 1. The Histogram processing of the region 1 will process (VAL+1) clocks. VAL[0] cannot be written.	RW	0x000
0	VAL_RESERVED	The horizontal size of the region 1. The Histogram processing of the region 1 will process (VAL+1) clocks. VAL[0] cannot be written.	R Rreturns 1s	1

Table 8-882. Register Call Summary for Register IPIPE_HST_1_HSZ

ISS ISP

- Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-883. IPIPE_HST_2_VPS

Address Offset	0x0000 03CC		
Physical Address	0x5201 0BCC	**Instance**	ISS_IPIPE
Description	Histogram		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED				VAL											VAL_RESERVED

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12:1	VAL	The vertical position of the region 0 from the IPIPE_SRC_VPS. The region 2 will start the Histogram processing from VAL line. VAL[0] can not be written.	RW	0x000
0	VAL_RESERVED	The vertical position of the region 0 from the IPIPE_SRC_VPS. The region 2 will start the Histogram processing from VAL line. VAL[0] can not be written.	R	0

Table 8-884. Register Call Summary for Register IPIPE_HST_2_VPS

ISS ISP

- Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

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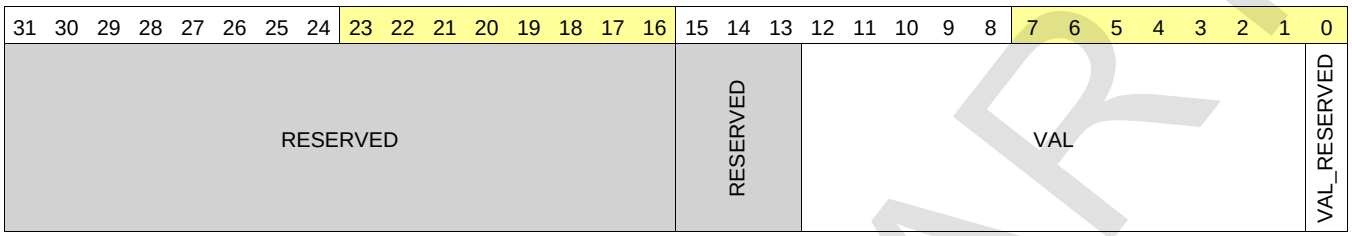
Table 8-885. IPIPE_HST_2_VSZ

Address Offset	0x0000 03D0		
Physical Address	0x5201 0BD0	**Instance**	ISS_IPIPE
Description	Histogram		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12:1	VAL	The vertical size of the region 2. The Histogram processing of the region 2 will process (VAL+1) lines. VAL[0] cannot be written.	RW	0x000
0	VAL_RESERVED	The vertical size of the region 2. The Histogram processing of the region 2 will process (VAL+1) lines. VAL[0] cannot be written.	R Rreturns 1s	1

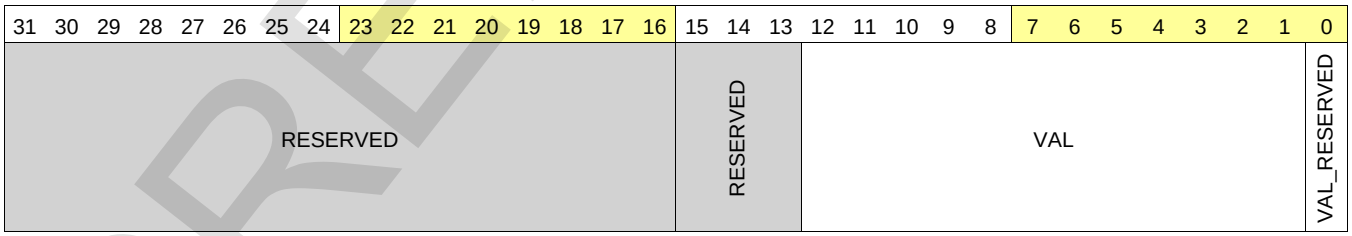
Table 8-886. Register Call Summary for Register IPIPE_HST_2_VSZ

ISS ISP

- Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-887. IPIPE_HST_2_HPS

Address Offset	0x0000 03D4		
Physical Address	0x5201 0BD4	**Instance**	ISS_IPIPE
Description	Histogram		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12:1	VAL	The horizontal position of the region 0 from the IPIPE_SRC_HPS. The region 2 will start the Histogram processing from VAL clocks. VAL[0] can not be written.	RW	0x000

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Bits	Field Name	Description	Type	Reset
0	VAL_RESERVED	The horizontal position of the region 0 from the IPIPE_SRC_HPS. The region 2 will start the Histogram processing from VAL clocks. VAL[0] can not be written.	R	0

Table 8-888. Register Call Summary for Register IPIPE_HST_2_HPS

ISS ISP
- ISS IPIPE Register Summary: [0]

Table 8-889. IPIPE_HST_2_HSZ

Address Offset	0x0000 03D8		
Physical Address	0x5201 0BD8	**Instance**	ISS_IPIPE
Description	Histogram		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED			VAL												VAL_RESERVED

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12:1	VAL	The horizontal size of the region 2. The Histogram processing of the region 2 will process (VAL+1) clocks. VAL[0] cannot be written.	RW	0x000
0	VAL_RESERVED	The horizontal size of the region 2. The Histogram processing of the region 2 will process (VAL+1) clocks. VAL[0] cannot be written.	R Rreturns 1s	1

Table 8-890. Register Call Summary for Register IPIPE_HST_2_HSZ

ISS ISP
- Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-891. IPIPE_HST_3_VPS

Address Offset	0x0000 03DC		
Physical Address	0x5201 0BDC	**Instance**	ISS_IPIPE
Description	Histogram		
Type	RW		

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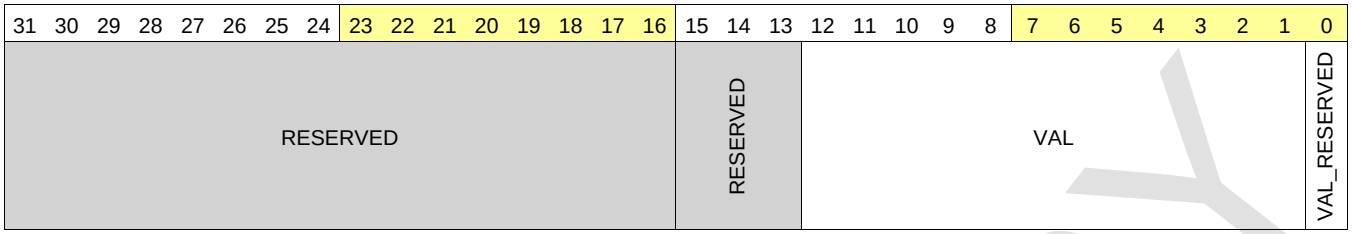


Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12:1	VAL	The vertical position of the region 0 from the IPIPE_SRC_VPS. The region 3 will start the Histogram processing from VAL line. VAL[0] can not be written.	RW	0x000
0	VAL_RESERVED	The vertical position of the region 0 from the IPIPE_SRC_VPS. The region 3 will start the Histogram processing from VAL line. VAL[0] can not be written.	R	0

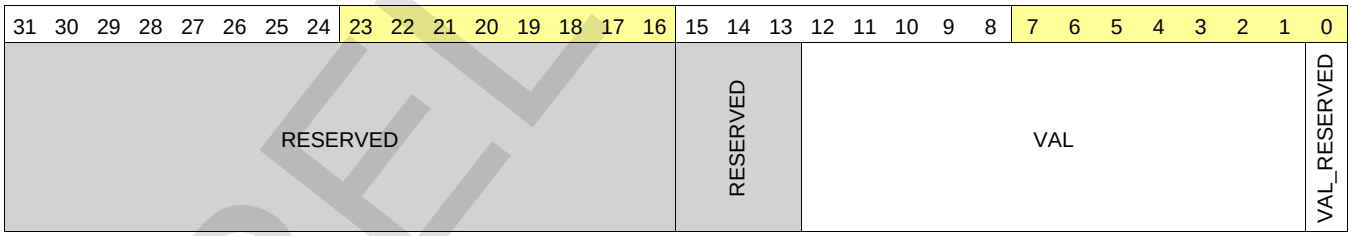
Table 8-892. Register Call Summary for Register IPIPE_HST_3_VPS

ISS ISP

- Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-893. IPIPE_HST_3_VSZ

Address Offset	0x0000 03E0		
Physical Address	0x5201 0BE0	**Instance**	ISS_IPIPE
Description	Histogram		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12:1	VAL	The vertical size of the region 3. The Histogram processing of the region 3 will process (VAL+1) lines. VAL[0] cannot be written.	RW	0x000
0	VAL_RESERVED	The vertical size of the region 3. The Histogram processing of the region 3 will process (VAL+1) lines. VAL[0] cannot be written.	R Rreturns 1s	1

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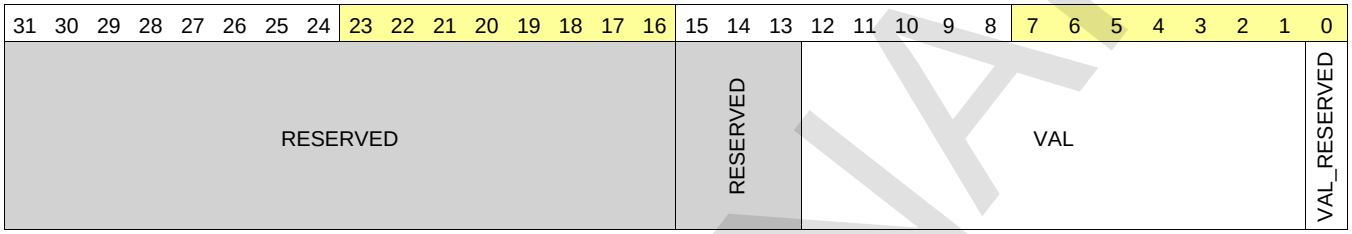
Table 8-894. Register Call Summary for Register IPIPE_HST_3_VSZ

ISS ISP

- Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-895. IPIPE_HST_3_HPS

Address Offset	0x0000 03E4		
Physical Address	0x5201 0BE4	**Instance**	ISS_IPIPE
Description	Histogram		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12:1	VAL	The horizontal position of the region 0 from the IPIPE_SRC_HPS. The region 3 will start the Histogram processing from VAL clocks. VAL[0] can not be written.	RW	0x000
0	VAL_RESERVED	The horizontal position of the region 0 from the IPIPE_SRC_HPS. The region 3 will start the Histogram processing from VAL clocks. VAL[0] can not be written.	R	0

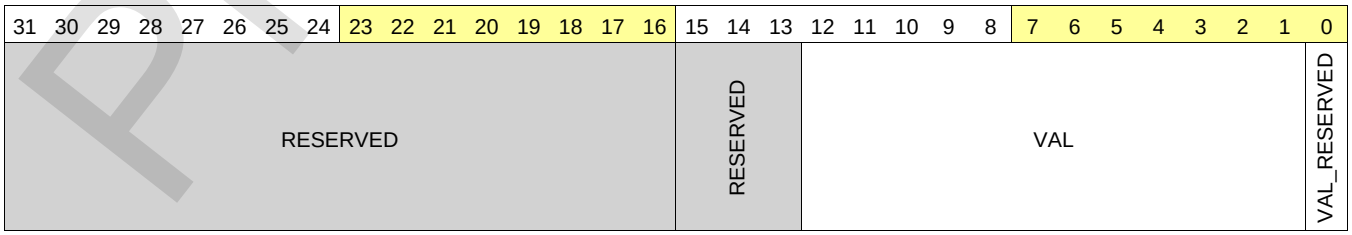
Table 8-896. Register Call Summary for Register IPIPE_HST_3_HPS

ISS ISP

- ISS IPIPE Register Summary: [0]

Table 8-897. IPIPE_HST_3_HSZ

Address Offset	0x0000 03E8		
Physical Address	0x5201 0BE8	**Instance**	ISS_IPIPE
Description	Histogram		
Type	RW		



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Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12:1	VAL	The horizontal size of the region 3. The Histogram processing of the region 3 will process (VAL+1) clocks. VAL[0] cannot be written.	RW	0x000
0	VAL_RESERVED	The horizontal size of the region 3. The Histogram processing of the region 3 will process (VAL+1) clocks. VAL[0] cannot be written.	R Rreturns 1s	1

Table 8-898. Register Call Summary for Register IPIPE_HST_3_HSZ

ISS ISP

- Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-899. IPIPE_HST_TBL

Address Offset	0x0000 03EC		
Physical Address	0x5201 0BEC	**Instance**	ISS_IPIPE
Description	Histogram		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED														CLR	SEL

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:2	RESERVED		R	0x0000
1	CLR	Histogram memory clear. The histogram can be cleared before the start of operations. However, the clear takes 512 cycles and therefore: + if line size 512, the first line must not be used for histogram computation. + if line size 512, ceil (512/line size) lines must not be used for histogram computation. It's the programmer's responsibility to set the histogram computation area outside the "clear" area. 0x0: Disable 0x1: Enable	RW	0
0	SEL	This bit must be used to select which memory is used to store the histogram data. By selecting alternatively one or the other bit, one can double buffer the histogram output buffer. The 4 KB memory can either be read by the CPU or a DMA request. 0x0: Use Table 0 and 1 = 4KB in the memory ISP map. 0x1: Use Table 2 and 3 = 4KB in the memory ISP map.	RW	0

Table 8-900. Register Call Summary for Register IPIPE_HST_TBL

ISS ISP

- ISS ISP DMA Requests: [0] [1]
- ISS ISP IPIPE Histogram: [2] [3]
- Global Initialization: [4] [5]
- ISS IPIPE Register Summary: [6]

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Table 8-901. IPIPE_HST_MUL_R

Address Offset	0x0000 03F0		
Physical Address	0x5201 0BF0	**Instance**	ISS_IPIPE
Description	Histogram		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								GAIN							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:8	RESERVED		R	0x00
7:0	GAIN	Gain	RW	0x00

Table 8-902. Register Call Summary for Register IPIPE_HST_MUL_R

ISS ISP

- Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-903. IPIPE_HST_MUL_GR

Address Offset	0x0000 03F4		
Physical Address	0x5201 0BF4	**Instance**	ISS_IPIPE
Description	Histogram		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								GAIN							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:8	RESERVED		R	0x00
7:0	GAIN	Gain	RW	0x00

Table 8-904. Register Call Summary for Register IPIPE_HST_MUL_GR

ISS ISP

- Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-905. IPIPE_HST_MUL_GB

Address Offset	0x0000 03F8		
Physical Address	0x5201 0BF8	**Instance**	ISS_IPIPE
Description	Histogram		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								GAIN							

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Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:8	RESERVED		R	0x00
7:0	GAIN	Gain	RW	0x00

Table 8-906. Register Call Summary for Register IPIPE_HST_MUL_GB

ISS ISP
- Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-907. IPIPE_HST_MUL_B

Address Offset	0x0000 03FC		
Physical Address	0x5201 0BFC	**Instance**	ISS_IPIPE
Description	Histogram		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								GAIN							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:8	RESERVED		R	0x00
7:0	GAIN	Gain	RW	0x00

Table 8-908. Register Call Summary for Register IPIPE_HST_MUL_B

ISS ISP
- Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

8.3.5.6 ISS ISIF Registers

CAUTION

The ISS ISIF registers are limited to 32 bit and 16 bit data accesses; 8bit data access is not allowed and can corrupt register content.

8.3.5.6.1 ISS ISIF Register Summary

Table 8-909. ISS ISIF Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	ISS_ISIF Base Address
ISIF_SYNCEN	RW	32	0x0000 0000	0x5201 1000
ISIF_MODESET	RW	32	0x0000 0004	0x5201 1004
ISIF_HDW	RW	32	0x0000 0008	0x5201 1008
ISIF_VDW	RW	32	0x0000 000C	0x5201 100C
ISIF_PPLN	RW	32	0x0000 0010	0x5201 1010
ISIF_LPFR	RW	32	0x0000 0014	0x5201 1014
ISIF_SPH	RW	32	0x0000 0018	0x5201 1018
ISIF_LNH	RW	32	0x0000 001C	0x5201 101C

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Table 8-909. ISS ISIF Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	ISS_ISIF Base Address
RESERVED	RW	32	0x0000 0020	0x5201 1020
RESERVED	RW	32	0x0000 0024	0x5201 1024
ISIF_LNV	RW	32	0x0000 0028	0x5201 1028
ISIF_CULH	RW	32	0x0000 002C	0x5201 102C
ISIF_CULV	RW	32	0x0000 0030	0x5201 1030
ISIF_HSIZE	RW	32	0x0000 0034	0x5201 1034
RESERVED	RW	32	0x0000 0038	0x5201 1038
ISIF_CADU	RW	32	0x0000 003C	0x5201 103C
ISIF_CADL	RW	32	0x0000 0040	0x5201 1040
ISIF_LINCFG0	RW	32	0x0000 0044	0x5201 1044
ISIF_LINCFG1	RW	32	0x0000 0048	0x5201 1048
ISIF_CCOLP	RW	32	0x0000 004C	0x5201 104C
ISIF_CRGAIN	RW	32	0x0000 0050	0x5201 1050
ISIF_CGRGAIN	RW	32	0x0000 0054	0x5201 1054
ISIF_CGBGAIN	RW	32	0x0000 0058	0x5201 1058
ISIF_CBGAIN	RW	32	0x0000 005C	0x5201 105C
ISIF_COFSTA	RW	32	0x0000 0060	0x5201 1060
ISIF_VDINT0	RW	32	0x0000 0070	0x5201 1070
ISIF_VDINT1	RW	32	0x0000 0074	0x5201 1074
ISIF_VDINT2	RW	32	0x0000 0078	0x5201 1078
ISIF_MISC	RW	32	0x0000 007C	0x5201 107C
ISIF_CGAMMAWD	RW	32	0x0000 0080	0x5201 1080
ISIF_REC656IF	RW	32	0x0000 0084	0x5201 1084
ISIF_CCDCFG	RW	32	0x0000 0088	0x5201 1088
ISIF_DFCCTL	RW	32	0x0000 008C	0x5201 108C
ISIF_VDFSATLV	RW	32	0x0000 0090	0x5201 1090
ISIF_DFCMEMCTL	RW	32	0x0000 0094	0x5201 1094
ISIF_DFCMEM0	RW	32	0x0000 0098	0x5201 1098
ISIF_DFCMEM1	RW	32	0x0000 009C	0x5201 109C
ISIF_DFCMEM2	RW	32	0x0000 00A0	0x5201 10A0
ISIF_DFCMEM3	RW	32	0x0000 00A4	0x5201 10A4
ISIF_DFCMEM4	RW	32	0x0000 00A8	0x5201 10A8
ISIF_CLAMPCFG	RW	32	0x0000 00AC	0x5201 10AC
ISIF_CLDCOFST	RW	32	0x0000 00B0	0x5201 10B0
ISIF_CLSV	RW	32	0x0000 00B4	0x5201 10B4
ISIF_CLHWIN0	RW	32	0x0000 00B8	0x5201 10B8
ISIF_CLHWIN1	RW	32	0x0000 00BC	0x5201 10BC
ISIF_CLHWIN2	RW	32	0x0000 00C0	0x5201 10C0
ISIF_CLVRV	RW	32	0x0000 00C4	0x5201 10C4
ISIF_CLVWIN0	RW	32	0x0000 00C8	0x5201 10C8
ISIF_CLVWIN1	RW	32	0x0000 00CC	0x5201 10CC
ISIF_CLVWIN2	RW	32	0x0000 00D0	0x5201 10D0
ISIF_CLVWIN3	RW	32	0x0000 00D4	0x5201 10D4
ISIF_LSCHOFST	RW	32	0x0000 00D8	0x5201 10D8
ISIF_LSCVOFST	RW	32	0x0000 00DC	0x5201 10DC
ISIF_LSCHVAL	RW	32	0x0000 00E0	0x5201 10E0
ISIF_LSCVVAL	RW	32	0x0000 00E4	0x5201 10E4

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Table 8-909. ISS ISIF Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	ISS_ISIF Base Address
ISIF_2DLSCCFG	RW	32	0x0000 00E8	0x5201 10E8
ISIF_2DLSCOFST	RW	32	0x0000 00EC	0x5201 10EC
ISIF_2DLSCINI	RW	32	0x0000 00F0	0x5201 10F0
ISIF_2DLSCGRBU	RW	32	0x0000 00F4	0x5201 10F4
ISIF_2DLSCGRBL	RW	32	0x0000 00F8	0x5201 10F8
ISIF_2DLSCGROF	RW	32	0x0000 00FC	0x5201 10FC
ISIF_2DLSCORBU	RW	32	0x0000 0100	0x5201 1100
ISIF_2DLSCORBL	RW	32	0x0000 0104	0x5201 1104
ISIF_2DLSCOROF	RW	32	0x0000 0108	0x5201 1108
ISIF_2DLSCIRQEN	RW	32	0x0000 010C	0x5201 110C
ISIF_2DLSCIRQST	RW	32	0x0000 0110	0x5201 1110
ISIF_FMTCFG	RW	32	0x0000 0114	0x5201 1114
ISIF_FMTPLEN	RW	32	0x0000 0118	0x5201 1118
ISIF_FMTSPH	RW	32	0x0000 011C	0x5201 111C
ISIF_FMTLNH	RW	32	0x0000 0120	0x5201 1120
ISIF_FMTLSV	RW	32	0x0000 0124	0x5201 1124
ISIF_FMTLNV	RW	32	0x0000 0128	0x5201 1128
ISIF_FMTRLEN	RW	32	0x0000 012C	0x5201 112C
ISIF_FMTHCNT	RW	32	0x0000 0130	0x5201 1130
ISIF_FMTAPTR0	RW	32	0x0000 0134	0x5201 1134
ISIF_FMTAPTR1	RW	32	0x0000 0138	0x5201 1138
ISIF_FMTAPTR2	RW	32	0x0000 013C	0x5201 113C
ISIF_FMTAPTR3	RW	32	0x0000 0140	0x5201 1140
ISIF_FMTAPTR4	RW	32	0x0000 0144	0x5201 1144
ISIF_FMTAPTR5	RW	32	0x0000 0148	0x5201 1148
ISIF_FMTAPTR6	RW	32	0x0000 014C	0x5201 114C
ISIF_FMTAPTR7	RW	32	0x0000 0150	0x5201 1150
ISIF_FMTAPTR8	RW	32	0x0000 0154	0x5201 1154
ISIF_FMTAPTR9	RW	32	0x0000 0158	0x5201 1158
ISIF_FMTAPTR10	RW	32	0x0000 015C	0x5201 115C
ISIF_FMTAPTR11	RW	32	0x0000 0160	0x5201 1160
ISIF_FMTAPTR12	RW	32	0x0000 0164	0x5201 1164
ISIF_FMTAPTR13	RW	32	0x0000 0168	0x5201 1168
ISIF_FMTAPTR14	RW	32	0x0000 016C	0x5201 116C
ISIF_FMTAPTR15	RW	32	0x0000 0170	0x5201 1170
ISIF_FMTPGMVF0	RW	32	0x0000 0174	0x5201 1174
ISIF_FMTPGMVF1	RW	32	0x0000 0178	0x5201 1178
ISIF_FMTPGMAPU0	RW	32	0x0000 017C	0x5201 117C
ISIF_FMTPGMAPU1	RW	32	0x0000 0180	0x5201 1180
ISIF_FMTPGMAPS0	RW	32	0x0000 0184	0x5201 1184
ISIF_FMTPGMAPS1	RW	32	0x0000 0188	0x5201 1188
ISIF_FMTPGMAPS2	RW	32	0x0000 018C	0x5201 118C
ISIF_FMTPGMAPS3	RW	32	0x0000 0190	0x5201 1190
ISIF_FMTPGMAPS4	RW	32	0x0000 0194	0x5201 1194
ISIF_FMTPGMAPS5	RW	32	0x0000 0198	0x5201 1198
ISIF_FMTPGMAPS6	RW	32	0x0000 019C	0x5201 119C
ISIF_FMTPGMAPS7	RW	32	0x0000 01A0	0x5201 11A0

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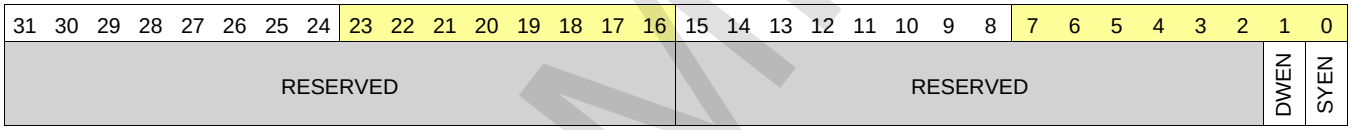
Table 8-909. ISS ISIF Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	ISS_ISIF Base Address
ISIF_CSCCTL	RW	32	0x0000 01A4	0x5201 11A4
ISIF_CSCM0	RW	32	0x0000 01A8	0x5201 11A8
ISIF_CSCM1	RW	32	0x0000 01AC	0x5201 11AC
ISIF_CSCM2	RW	32	0x0000 01B0	0x5201 11B0
ISIF_CSCM3	RW	32	0x0000 01B4	0x5201 11B4
ISIF_CSCM4	RW	32	0x0000 01B8	0x5201 11B8
ISIF_CSCM5	RW	32	0x0000 01BC	0x5201 11BC
ISIF_CSCM6	RW	32	0x0000 01C0	0x5201 11C0
ISIF_CSCM7	RW	32	0x0000 01C4	0x5201 11C4
ISIF_CLKCTL	RW	32	0x0000 01F8	0x5201 11F8

8.3.5.6.2 ISS ISIF Register Description

Table 8-910. ISIF_SYNCEN

Address Offset	0x0000 0000		
Physical Address	0x5201 1000	**Instance**	ISS_ISIF
Description			
Type	RW		



Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:2	RESERVED		R	0x0000
1	DWEN	Controls the storage of image sensor RAW data in memory. This bit is loaded with the timing of the internal VD signal: it becomes active starting at the lead of the VD signal that comes after 1 is written in this bit. 0x0: Disable 0x1: Enable	RW	0
0	SYEN	Controls ON/OFF of VD/HD output. Internal timing generator becomes active and VD/HD output starts when 1 is written in this bit. In case of input, VD/HD loading begins. 0: Disable 1: Enable	RW	0

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Table 8-911. Register Call Summary for Register ISIF_SYNCEN

ISS ISP

- ISS ISP ISIF Expected Bandwidth on BL Ports: [0]
- ISS ISP ISIF Events and Status Checking: [1]
- ISS ISP ISIF Hardware Setup/Initialization: [2] [3]
- ISS ISP ISIF Enable/Disable Hardware: [4] [5] [6] [7] [8] [9]
- ISS ISP ISIF Register Accessibility During Frame Processing: [10]
- ISS ISP ISIF Interframe Operations: [11]
- ISS ISP ISIF Summary of Constraints: [12] [13]
- ISS ISIF Register Summary: [14]

Table 8-912. ISIF_MODESET

Address Offset	0x0000 0004		
Physical Address	0x5201 1004	**Instance**	ISS_ISIF
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED	HLPF	INPMOD		OVF	CCDW			CCDMD	DPOL	SWEN	RESERVED	HDPOL	VDPOL	FIDD	HDVDD

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15	RESERVED	Read returns reset value	R	0
14	HLPF	Low pass filter enable. When this bit is enabled, a 3-tap (1/4 + 1/2 Z^{-2} + 1/4 Z^{4}) filtering process is performed on the sensor data. 0x0: Disable 0x1: Enable	RW	0
13:12	INPMOD	Data input mode: 0x0: RAW data 0x1: YCbCr 16bit 0x3: Reserved 0x2: YCbCr 8bit	RW	0x2
11	OVF	ISIF module write port overflow status bit If the write port of the ISIF module overflows when writing data to SDRAM, this bit will toggle. 0x0: No overflow pending (r) No action (w) 0x1: Overflow pending (r) Clear overflow (w)	RW	0

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Bits	Field Name	Description	Type	Reset
10:8	CCDW	This bit enables to shift right (divide) the up-to-12-bit RAW data value when writing out to SDRAM. The effect is that the dynamic of the output signal is decreased. The ISIF_MODESET.CCDW, ISIF_HSIZE.ADCR, ISIF_HSIZE.HSIZE, ISIF_CCDCFG.BSWD, ISIF_CCDCFG.MSBINV, ISIF_CCDCFG.SDRPACK bit fields control how pixel data are stored to SDRAM. 0x6: Reserved 0x1: 1-bit right shift out[15:0] = 00000 data[11:1] 0x7: Reserved 0x0: No shift out[15:0] = 0000 data[11:0] 0x2: 2-bit right shift out[15:0] = 000000 data[11:2] 0x4: 4-bit right shift out[15:0] = 00000000 data[11:4] 0x5: Reserved 0x3: 3-bit right shift out[15:0] = 0000000 data[11:3]	RW	0x0
7	CCDMD	Field mode: This bit selects the type of image sensor: interlaced or progressive 0x0: Progressive image sensor 0x1: Interlaced image sensor	RW	0
6	DPOL	Image sensor input data polarity 0x0: No change 0x1: One's complement	RW	0
5	SWEN	External WEN selection In case this bit and SYNCEN.DWEN are set to 1, the external WEN signal is used to store image sensor data to memory. 0x0: WEN not used 0x1: Use external WEN	RW	0
4	RESERVED	Read returns reset value	RW	0
3	HDPOL	HD Sync Signal Polarity 0x0: Positive 0x1: Negative	RW	0
2	VDPOL	VD Sync Signal Polarity 0x0: Positive 0x1: Negative	RW	0
1	FIDD	FLD Signal Direction. There must be at least three clock cycles between the time this bit is modified and the HD/VD pulse for the start of frame comes. 0x0: Input 0x1: Output	RW	0
0	HDVDD	VD,HD Sync Signal Direction. There must be at least three clock cycles between the time this bit is modified and the HD/VD pulse for the start of frame comes. 0x0: Input 0x1: Output	RW	0

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Table 8-913. Register Call Summary for Register ISIF_MODESET

ISS ISP

- ISS ISP ISIF Interrupts: [0]
- ISS ISP VP Pixel Clock Inversion: [1] [2]
- ISS ISP ISIF Input Interface: [3] [4]
- ISS ISP ISIF Interface: [5] [6]
- ISS ISP ISIF Low-Pass Filter (LPF): [7] [8]
- ISP ISIF Storage Formatter: [9] [10]
- ISS ISP ISIF Events and Status Checking: [11] [12] [13] [14]
- ISS ISP ISIF Hardware Setup/Initialization: [15] [16] [17] [18] [19] [20] [21] [22] [23] [24] [25]
- ISS ISP ISIF Enable/Disable Hardware: [26] [27] [28] [29]
- ISS ISP ISIF Register Accessibility During Frame Processing: [30]
- ISS ISIF Register Summary: [31]
- ISS ISIF Register Description: [32] [33] [34] [35] [36]

Table 8-914. ISIF_HDW

Address Offset	0x0000 0008		
Physical Address	0x5201 1008	**Instance**	ISS_ISIF
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED				HDW											

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	RESERVED		R	0x0
11:0	HDW	HD width: Sets width of HD. HD width = HDW + 1 clock	RW	0x000

Table 8-915. Register Call Summary for Register ISIF_HDW

ISS ISP

- ISS ISP ISIF Black Clamp: [0]
- ISS ISP ISIF Hardware Setup/Initialization: [1]
- ISS ISP ISIF Register Accessibility During Frame Processing: [2]
- ISS ISIF Register Summary: [3]

Table 8-916. ISIF_VDW

Address Offset	0x0000 000C		
Physical Address	0x5201 100C	**Instance**	ISS_ISIF
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED				VDW											

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	RESERVED		R	0x0
11:0	VDW	VD width : Sets width of VD. VD width = VDW + 1 line	RW	0x000

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Table 8-917. Register Call Summary for Register ISIF_VDW

ISS ISP

- ISS ISP ISIF Black Clamp: [0]
- ISS ISP ISIF Hardware Setup/Initialization: [1]
- ISS ISP ISIF Register Accessibility During Frame Processing: [2]
- ISS ISIF Register Summary: [3]

Table 8-918. ISIF_PPLN

Address Offset	0x0000 0010		
Physical Address	0x5201 1010	**Instance**	ISS_ISIF
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PPLN															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:0	PPLN	Pixels per line Number of pixel clock periods in one line HD period = PPLN+1 pixel clocks. PPLN is not used when HD and VD are inputs, that is, when VDHDOUT in MODESET is cleared to 0. *This bit field is latched by VD.	RW	0x0000

Table 8-919. Register Call Summary for Register ISIF_PPLN

ISS ISP

- ISS ISP ISIF Black Clamp: [0] [1]
- ISS ISP ISIF Hardware Setup/Initialization: [2]
- ISS ISP ISIF Register Accessibility During Frame Processing: [3]
- ISS ISIF Register Summary: [4]

Table 8-920. ISIF_LPFR

Address Offset	0x0000 0014		
Physical Address	0x5201 1014	**Instance**	ISS_ISIF
Description	Line per Frame/Field		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																LPFR															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:0	LPFR	Half lines per filed or frame Sets number of half lines per frame or field. VD period = (LPFR+1)/2 lines. LPFR is not used when HD and are inputs, that is, when VDHDOUT in MODESET is cleared to 0. *This bit field is latched by VD.	RW	0x0000

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Table 8-921. Register Call Summary for Register ISIF_LPFR

ISS ISP

- ISS ISP ISIF Vertical Line Defect Correction (VDFC): [0]
- ISS ISP ISIF Hardware Setup/Initialization: [1]
- ISS ISP ISIF Register Accessibility During Frame Processing: [2]
- ISS ISIF Register Summary: [3]

Table 8-922. ISIF_SPH

Address Offset	0x0000 0018		
Physical Address	0x5201 1018	**Instance**	ISS_ISIF
Description	Start Pixel Horizontal		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								SPH							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15	RESERVED		R	0
14:0	SPH	The first pixel in a line to be stored to memory.	RW	0x0000

Table 8-923. Register Call Summary for Register ISIF_SPH

ISS ISP

- ISS ISP ISIF Input Data Formatter: [0]
- ISP ISIF Storage Formatter: [1]
- ISS ISP ISIF Hardware Setup/Initialization: [2]
- ISS ISP ISIF Register Accessibility During Frame Processing: [3]
- ISS ISP ISIF Summary of Constraints: [4] [5]
- ISS ISIF Register Summary: [6]

Table 8-924. ISIF_LNH

Address Offset	0x0000 001C		
Physical Address	0x5201 101C	**Instance**	ISS_ISIF
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								LNH							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15	RESERVED		R	0
14:0	LNH	Number of pixels in an line to be stored to memory. Number of pixels = LNH + 1.	RW	0x0000

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Table 8-925. Register Call Summary for Register ISIF_LNH

ISS ISP

- ISS ISP ISIF Input Data Formatter: [0]
- ISP ISIF Storage Formatter: [1]
- ISS ISP ISIF Hardware Setup/Initialization: [2]
- ISS ISP ISIF Register Accessibility During Frame Processing: [3]
- ISS ISP ISIF Summary of Constraints: [4] [5] [6]
- ISS ISIF Register Summary: [7]

Table 8-926. ISIF_LNV

Address Offset	0x0000 0028		
Physical Address	0x5201 1028	**Instance**	ISS_ISIF
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED	LNV														

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15	RESERVED	The number of lines to be stored to SDRAM.	R	0
14:0	LNV	The number of lines to be stored to memory. Number of lines = LNV + 1	RW	0x0000

Table 8-927. Register Call Summary for Register ISIF_LNV

ISS ISP

- ISS ISP ISIF Input Data Formatter: [0]
- ISP ISIF Storage Formatter: [1]
- ISS ISP ISIF Hardware Setup/Initialization: [2]
- ISS ISP ISIF Summary of Constraints: [3] [4]
- ISS ISIF Register Summary: [5]

Table 8-928. ISIF_CULH

Address Offset	0x0000 002C		
Physical Address	0x5201 102C	**Instance**	ISS_ISIF
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																CLHO								CLHE							

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Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:8	CLHO	Culling Pattern in ODD Line: Sets culling pattern when data is loaded into memory (odd lines). Example: 0xAA: 1 / 2 horizontal direction culling. LSB becomes left side on screen. 0x0: Pixel invalid 0x1: Pixel valid	RW	0xFF
7:0	CLHE	Culling Pattern in Even Line: Sets culling pattern when data is loaded into memory (even lines). 0x0: Pixel invalid 0x1: Pixel valid	RW	0xFF

Table 8-929. Register Call Summary for Register ISIF_CULH

ISS ISP
- ISS ISP ISIF Culling: [0] [1] [2]
- ISS ISP ISIF Hardware Setup/Initialization: [3] [4]
- ISS ISP ISIF Register Accessibility During Frame Processing: [5]
- ISS ISIF Register Summary: [6]

Table 8-930. ISIF_CULV

Address Offset	0x0000 0030		
Physical Address	0x5201 1030	**Instance**	ISS_ISIF
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								CULV							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:8	RESERVED		R	0x00
7:0	CULV	Culling Pattern in Vertical Line Example: 0x88: 1/4 vertical direction culling. LSB becomes top side on screen. 0x0: Pixel invalid 0x1: Pixel valid	RW	0xFF

Table 8-931. Register Call Summary for Register ISIF_CULV

ISS ISP
- ISS ISP ISIF Culling: [0]
- ISS ISP ISIF Hardware Setup/Initialization: [1]
- ISS ISP ISIF Register Accessibility During Frame Processing: [2]
- ISS ISIF Register Summary: [3]

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Table 8-932. ISIF_HSIZE

Address Offset	0x0000 0034		
Physical Address	0x5201 1034	**Instance**	ISS_ISIF
Description	SDRAM OUTPUT CTRL REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED			ADCR	HSIZE											

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12	ADCR	SDRAM address decrement. By setting this bit, memory address in a line is automatically decreased so that a line can be Horizontally flipped in memory. The ISIF_MODESET.CCDW, ISIF_HSIZE.ADCR, ISIF_HSIZE.HSIZE, ISIF_CCDCFG.BSWD, ISIF_CCDCFG.MSBINV, ISIF_CCDCFG.SDRPACK bit fields control how pixel data are stored to SDRAM. 0x0: Address increment. 0x1: Address decrement.	RW	0
11:0	HSIZE	Memory address offset between the lines. Specify the offset in 32-byte units.	RW	0x000

Table 8-933. Register Call Summary for Register ISIF_HSIZE

ISS ISP

- ISP ISIF Storage Formatter: [0] [1]
- ISS ISP ISIF Hardware Setup/Initialization: [2] [3]
- ISS ISP ISIF Register Accessibility During Frame Processing: [4]
- ISS ISIF Register Summary: [5]
- ISS ISIF Register Description: [6] [7] [8] [9] [10] [11] [12] [13] [14] [15]

Table 8-934. ISIF_CADU

Address Offset	0x0000 003C		
Physical Address	0x5201 103C	**Instance**	ISS_ISIF
Description	SDRAM OUTPUT CTRL REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED					CADU										

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:11	RESERVED		R	0x00
10:0	CADU	Memory Address (Upper 11-bits): Specifies the memory destination address. The actual address is the value set here multiplied by 32bytes.	RW	0x000

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Table 8-935. Register Call Summary for Register ISIF_CADU

ISS ISP

- ISP ISIF Storage Formatter: [0]
- ISS ISP ISIF Hardware Setup/Initialization: [1]
- ISS ISP ISIF Enable/Disable Hardware: [2] [3]
- ISS ISP ISIF Register Accessibility During Frame Processing: [4]
- ISS ISIF Register Summary: [5]

Table 8-936. ISIF_CADL

Address Offset	0x0000 0040		
Physical Address	0x5201 1040	**Instance**	ISS_ISIF
Description	SDRAM OUTPUT CTRL REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																CADL															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:0	CADL	Memory Address (Lower 16-bits): Specifies the memory destination address. The actual address is the value set here multiplied by 32bytes.	RW	0x0000

Table 8-937. Register Call Summary for Register ISIF_CADL

ISS ISP

- ISP ISIF Storage Formatter: [0]
- ISS ISP ISIF Hardware Setup/Initialization: [1]
- ISS ISP ISIF Enable/Disable Hardware: [2] [3]
- ISS ISP ISIF Register Accessibility During Frame Processing: [4]
- ISS ISIF Register Summary: [5]

Table 8-938. ISIF_LINCFG0

Address Offset	0x0000 0044		
Physical Address	0x5201 1044	**Instance**	ISS_ISIF
Description	INPUT LINEARIZATION CTRL REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								CORRSFT				RESERVED		LINMD	LINEN

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Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:7	RESERVED		R	0x000
6:4	CORRSFT	Shift up value for the correction value (S10). 0x6: 6-bit left shift 0x1: 1-bit left shift 0x7: Reserved 0x0: No shift 0x2: 2-bit left shift 0x4: 4-bit left shift 0x5: 5-bit left shift 0x3: 3-bit left shift	RW	0x0
3:2	RESERVED		R	0x0
1	LINMD	Linearization Mode: 0x0: Uniform sampling 0x1: Non-uniform sampling	RW	0
0	LINEN	Linearization Enable: 0x0: Disable 0x1: Enable	RW	0

Table 8-939. Register Call Summary for Register ISIF_LINCFG0

ISS ISP

- ISS ISP ISIF Sensor Linearization: [0] [1] [2] [3]
- ISS ISP ISIF Hardware Setup/Initialization: [4] [5] [6]
- ISS ISIF Register Summary: [7]

Table 8-940. ISIF_LINCFG1

Address Offset	0x0000 0048		
Physical Address	0x5201 1048	**Instance**	ISS_ISIF
Description	INPUT LINEARIZATION CTRL REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED					LUTSCL										

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:11	RESERVED		R	0x00
10:0	LUTSCL	Scale factor (U11Q10) for LUT input. Range: 0 - 1+1023/1024 It is applied to the Input Data before looking up the correction factor. The scale factor is only applied to the table input. It is not applied when using the input value to compute the output.	RW	0x400

Table 8-941. Register Call Summary for Register ISIF_LINCFG1

ISS ISP

- ISS ISP ISIF Sensor Linearization: [0]
- ISS ISP ISIF Hardware Setup/Initialization: [1]
- ISS ISIF Register Summary: [2]

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Table 8-942. ISIF_CCOLP

Address Offset	0x0000 004C		
Physical Address	0x5201 104C	**Instance**	ISS_ISIF
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																CP0_F1		CP1_F1		CP2_F1		CP3_F1		CP0_F0		CP1_F0		CP2_F0		CP3_F0	

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:14	CP0_F1	Specifies color pattern for pixel position 0 (Field 1) Pixel position 0 corresponds to pixel count=0 at even line in case of CFAP= 0, and to pixel count=0 in case of CFAP= 1. 0x0: R / Ye 0x1: Gr / Cy 0x3: B / Mg 0x2: Gb / G	RW	0x0
13:12	CP1_F1	Specifies color pattern for pixel position 1 (Field 1) Pixel position 1 corresponds to pixel count=1 at even line in case of CFAP= 0, and to pixel count=1 in case of CFAP= 1. 0x0: R / Ye 0x1: Gr / Cy 0x3: B / Mg 0x2: Gb / G	RW	0x0
11:10	CP2_F1	Specifies color pattern for pixel position 2 (Field 1) Pixel position 2 corresponds to pixel count=0 at odd line in case of CFAP= 0, and to pixel count=2 in case of CFAP= 1. 0x0: R / Ye 0x1: Gr / Cy 0x3: B / Mg 0x2: Gb / G	RW	0x0
9:8	CP3_F1	Specifies color pattern for pixel position 3 (Field 1) Pixel position 3 corresponds to pixel count=1 at odd line in case of CFAP= 0. Not applicable for CFAP= 1. 0x0: R / Ye 0x1: Gr / Cy 0x3: B / Mg 0x2: Gb / G	RW	0x0
7:6	CP0_F0	Specifies color pattern for pixel position 0 (Field 0) Pixel position 0 corresponds to pixel count=0 at even line in case of CFAP= 0, and to pixel count=0 in case of CFAP= 1. 0x0: R / Ye 0x1: Gr / Cy 0x3: B / Mg 0x2: Gb / G	RW	0x0

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Bits	Field Name	Description	Type	Reset
5:4	CP1_F0	Specifies color pattern for pixel position 1 (Field 0) Pixel position 1 corresponds to pixel count=1 at even line in case of CFAP= 0, and to pixel count=1 in case of CFAP= 1. 0x0: R / Ye 0x1: Gr / Cy 0x3: B / Mg 0x2: Gb / G	RW	0x0
3:2	CP2_F0	Specifies color pattern for pixel position 2 (Field 0) Pixel position 2 corresponds to pixel count=0 at odd line in case of CFAP= 0, and to pixel count=2 in case of CFAP= 1. 0x0: R / Ye 0x1: Gr / Cy 0x3: B / Mg 0x2: Gb / G	RW	0x0
1:0	CP3_F0	Specifies color pattern for pixel position 3 (Field 0) Pixel position 3 corresponds to pixel count=1 at odd line in case of CFAP= 0. Not applicable for CFAP= 1. 0x0: R / Ye 0x1: Gr / Cy 0x3: B / Mg 0x2: Gb / G	RW	0x0

Table 8-943. Register Call Summary for Register ISIF_CCOLP

ISS ISP

- ISS ISP ISIF White Balance: [0]
- ISS ISP ISIF Hardware Setup/Initialization: [1] [2] [3] [4]
- ISS ISP ISIF Register Accessibility During Frame Processing: [5]
- ISS ISIF Register Summary: [6]

Table 8-944. ISIF_CRGAIN

Address Offset	0x0000 0050		
Physical Address	0x5201 1050	**Instance**	ISS_ISIF
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED				CGR											

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	RESERVED		R	0x0
11:0	CGR	R/Ye gain: Performs gain adjustment on image sensor data. U12Q9. Range: 0 - 7+511/512	RW	0x200

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Table 8-945. Register Call Summary for Register ISIF_CRGAIN

ISS ISP

- ISS ISP ISIF White Balance: [0]
- ISS ISP ISIF Hardware Setup/Initialization: [1]
- ISS ISP ISIF Register Accessibility During Frame Processing: [2]
- ISS ISIF Register Summary: [3]

Table 8-946. ISIF_CGRGAIN

Address Offset	0x0000 0054		
Physical Address	0x5201 1054	**Instance**	ISS_ISIF
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED				CGGR											

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	RESERVED		R	0x0
11:0	CGGR	Gr/Cy gain: Performs gain adjustment on image sensor data. U12Q9. Range: 0 - 7+511/512	RW	0x200

Table 8-947. Register Call Summary for Register ISIF_CGRGAIN

ISS ISP

- ISS ISP ISIF White Balance: [0]
- ISS ISP ISIF Hardware Setup/Initialization: [1]
- ISS ISP ISIF Register Accessibility During Frame Processing: [2]
- ISS ISIF Register Summary: [3]

Table 8-948. ISIF_CGBGAIN

Address Offset	0x0000 0058		
Physical Address	0x5201 1058	**Instance**	ISS_ISIF
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED				CGGB											

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	RESERVED		R	0x0
11:0	CGGB	Gb/Cy gain: Performs gain adjustment on image sensor data. U12Q9. Range: 0 - 7+511/512	RW	0x200

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Table 8-949. Register Call Summary for Register ISIF_CGBGAIN

ISS ISP
- ISS ISP ISIF White Balance: [0]
- ISS ISP ISIF Hardware Setup/Initialization: [1]
- ISS ISP ISIF Register Accessibility During Frame Processing: [2]
- ISS ISIF Register Summary: [3]

Table 8-950. ISIF_CBGAIN

Address Offset	0x0000 005C		
Physical Address	0x5201 105C	**Instance**	ISS_ISIF
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED				CGB											

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	RESERVED		R	0x0
11:0	CGB	B/Mg gain: Performs gain adjustment on image sensor data. U12Q9. Range: 0 - 7+511/512	RW	0x200

Table 8-951. Register Call Summary for Register ISIF_CBGAIN

ISS ISP
- ISS ISP ISIF White Balance: [0]
- ISS ISP ISIF Hardware Setup/Initialization: [1]
- ISS ISP ISIF Register Accessibility During Frame Processing: [2]
- ISS ISIF Register Summary: [3]

Table 8-952. ISIF_COFSTA

Address Offset	0x0000 0060		
Physical Address	0x5201 1060	**Instance**	ISS_ISIF
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED				COFT											

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	RESERVED		R	0x0
11:0	COFT	Image sensor offset: Performs offset value adjustment on image sensor data (0~4095).	RW	0x000

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Table 8-953. Register Call Summary for Register ISIF_COFSTA

ISS ISP

- ISS ISP ISIF White Balance: [0]
- ISS ISP ISIF Hardware Setup/Initialization: [1]
- ISS ISP ISIF Register Accessibility During Frame Processing: [2]
- ISS ISIF Register Summary: [3]

Table 8-954. ISIF_VDINT0

Address Offset	0x0000 0070		
Physical Address	0x5201 1070	**Instance**	ISS_ISIF
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								CVD0							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15	RESERVED		R	0
14:0	CVD0	VD0 Interrupt timing in a field (line number).	RW	0x0000

Table 8-955. Register Call Summary for Register ISIF_VDINT0

ISS ISP

- ISS ISP ISIF Events and Status Checking: [0]
- ISS ISIF Register Summary: [1]

Table 8-956. ISIF_VDINT1

Address Offset	0x0000 0074		
Physical Address	0x5201 1074	**Instance**	ISS_ISIF
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								CVD1							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15	RESERVED		R	0
14:0	CVD1	VD1 Interrupt timing in a field (line number).	RW	0x0000

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Table 8-957. Register Call Summary for Register ISIF_VDINT1

ISS ISP

- ISS ISP ISIF Events and Status Checking: [0]
- ISS ISIF Register Summary: [1]

Table 8-958. ISIF_VDINT2

Address Offset	0x0000 0078		
Physical Address	0x5201 1078	**Instance**	ISS_ISIF
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED	CVD2														

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15	RESERVED		R	0
14:0	CVD2	VD2 Interrupt timing in a field (line number).	RW	0x0000

Table 8-959. Register Call Summary for Register ISIF_VDINT2

ISS ISP

- ISS ISP ISIF Events and Status Checking: [0]
- ISS ISIF Register Summary: [1]

Table 8-960. ISIF_MISC

Address Offset	0x0000 007C		
Physical Address	0x5201 107C	**Instance**	ISS_ISIF
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED		DPCMPRE	DPCMEN	RESERVED										RESERVED	

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:14	RESERVED		R	0x0
13	DPCMPRE	Selects Predictor for DPCM Encoder (12-8) 0x0: Predictor 1 0x1: Predictor 2	RW	0
12	DPCMEN	Enables DPCM Encoding (12-8) 0x0: Disable 0x1: Enable	RW	0
11:1	RESERVED		R	0x000

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Bits	Field Name	Description	Type	Reset
0	RESERVED		RW	0

Table 8-961. Register Call Summary for Register ISIF_MISC

ISS ISP

- ISS ISP ISIF 12-to-8 bit DCPM Compression Block: [0] [1]
- ISS ISP ISIF Hardware Setup/Initialization: [2] [3]
- ISS ISP ISIF Register Accessibility During Frame Processing: [4]
- ISS ISIF Register Summary: [5]

Table 8-962. ISIF_CGAMMAWD

Address Offset	0x0000 0080		
Physical Address	0x5201 1080	**Instance**	ISS_ISIF
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED	WBEN2	WBEN1	WBEN0	RESERVED	OFSTEN2	OFSTEN1	OFSTEN0	RESERVED		CFAP	GWDI				CCDTBL

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15	RESERVED		R	0
14	WBEN2	White Balance Enable for H3A 0x0: Disable 0x1: Enable	RW	0
13	WBEN1	White Balance Enable for IPIPE 0x0: Disable 0x1: Enable	RW	0
12	WBEN0	White Balance Enable for memory capture 0x0: Disable 0x1: Enable	RW	0
11	RESERVED		R	0
10	OFSTEN2	Offset control Enable for H3A 0x0: Disable 0x1: Enable	RW	0
9	OFSTEN1	Offset control Enable for IPIPE 0x0: Disable 0x1: Enable	RW	0
8	OFSTEN0	Offset control Enable for SDRAM capture 0x0: Disable 0x1: Enable	RW	0
7:6	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
5	CFAP	Selects CFA pattern 0x0: Mosaic color pattern. It should look like this. G R G R G R G R . . . B G B G B G B G . . . G R G R G R G R . . . . 0x1: Stripe color pattern. It should look like this. R G B R G B R G B . . . R G B R G B R G B . . . R G B R G B R G B	RW	0
4:1	GWDI	Selects MSB position of Input Data 0x6: bit 9 0x1: bit 14 0xA: Reserved 0x7: bit 8 0xD: Reserved 0x0: bit 15 0x2: bit 13 0x8: bit 7 0x9: Reserved 0xB: Reserved 0x4: bit 11 0x5: bit 10 0xF: Reserved 0xC: Reserved 0x3: bit 12 0xE: Reserved	RW	0x0
0	CCDTBL	On/Off control of A-law table for SDRAM capture 0x0: Disable 0x1: Enable	RW	0

Table 8-963. Register Call Summary for Register ISIF_CGAMMAWD

ISS ISP

- ISS ISP ISIF Interface: [0] [1]
- ISS ISP ISIF White Balance: [2] [3] [4] [5] [6] [7] [8]
- ISS ISP ISIF A-Law Compression: [9] [10] [11]
- ISS ISP ISIF Hardware Setup/Initialization: [12] [13] [14] [15] [16] [17] [18] [19] [20]
- ISS ISP ISIF Register Accessibility During Frame Processing: [21]
- ISS ISIF Register Summary: [22]

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Table 8-964. ISIF_REC656IF

Address Offset	0x0000 0084		
Physical Address	0x5201 1084	**Instance**	ISS_ISIF
Description	INPUT CONFIG REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED														R656ON	ECCFVH

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:2	RESERVED		R	0x0000
1	R656ON	CCIR Rec.656 interface mode 0x0: Disable 0x1: Enable	RW	0
0	ECCFVH	Error correction of FVH code 0x0: Disable 0x1: Enable	RW	0

Table 8-965. Register Call Summary for Register ISIF_REC656IF

ISS ISP

- ISS ISP ISIF Hardware Setup/Initialization: [0] [1]
- ISS ISIF Register Summary: [2]
- ISS ISIF Register Description: [3]

Table 8-966. ISIF_CCDCFG

Address Offset	0x0000 0088		
Physical Address	0x5201 1088	**Instance**	ISS_ISIF
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																VLDC	RESERVED	MSBINVI	BSWD	Y8POS	EXTRG	TRGSEL	WENLOG	FIDMD		BT656	YCINSWP	RESERVED	RESERVED	SDRPACK	

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15	VLDC	On/off control of CPU registers resynchronize function by VSYNC. All the others are shadowed registers, where register values are updated at V-sync timing by default. If VDLC=1, ISIF register values are updated immediately after register write just like non-shadowed registers. 0x0: Enable 0x1: Disable	RW	0
14	RESERVED	Reserved. must always be set to 0.	RW	0

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Bits	Field Name	Description	Type	Reset
13	MSBINVI	MSB inverse of CIN port when the data are captured to SDRAM. The ISIF_MODESET.CCDW, ISIF_HSIZE.ADCR, ISIF_HSIZE.HSIZE, ISIF_CCDCFG.BSWD, ISIF_CCDCFG.MSBINV, ISIF_CCDCFG.SDRPACK bit fields control how pixel data are stored to SDRAM. 0x0: Disable 0x1: Enable	RW	0
12	BSWD	On/off control of Byte SWAP function when SDRAM capturing. The ISIF_MODESET.CCDW, ISIF_HSIZE.ADCR, ISIF_HSIZE.HSIZE, ISIF_CCDCFG.BSWD, ISIF_CCDCFG.MSBINV, ISIF_CCDCFG.SDRPACK bit fields control how pixel data are stored to SDRAM. 0x0: Disable 0x1: Enable (swap)	RW	0
11	Y8POS	Selects Y signal position when in 8bit input mode 0x0: even pixel 0x1: odd pixel	RW	0
10	EXTRG	Setting 1 to this register, the SDRAM address is initialized at the rising edge of FID input signal or DWEN register.	RW	0
9	TRGSEL	Select trigger source signal of SDRAM address initializing in case EXTRG=1. 0x0: DWEN register 0x1: FID input port	RW	0
8	WENLOG	Specifies the CCD valid area. 0x0: internal valid signal and WEN signal is ANDed logically. 0x1: internal valid signal and WEN signal is ORed logically.	RW	0
7:6	FIDMD	Specifies FID detection mode 0x0: latch the FID at the VSYNC timing 0x1: no latch the FID 0x3: Reserved 0x2: Reserved	RW	0x0
5	BT656	Selects bit width of CCIR656. This bit applies only if ISIF_REC656IF.R656ON = 1. 0x0: 8 bits 0x1: 10 bits	RW	0
4	YCINSWP	The ISIF module has a 16-bit interface. When 16-bit YUV data are input, the luma data (YIN7-0) are expected to be on the 8 MS bits and the chroma (CIN7-0) data are expected to be on the LS bits. This bit enables to swap the 8 MS bits with the 8 LS bits of the interface in case the luma and chroma do not come in the correct order. See the top-level ISIF block diagram. 0x0: YIN7-0 = Y signal / CIN7-0 = C signal 0x1: YIN7-0 = C signal / CIN7-0 = Y signal	RW	0
3	RESERVED	Reserved. must always be set to 0.	RW	0
2	RESERVED	Reserved. must always be set to 0.	RW	0

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Bits	Field Name	Description	Type	Reset
1:0	SDRPACK	This bit field selects how the data are stored to SDRAM. There can be 8, 12 or 16 bits per pixel. The ISIF_MODESET.CCDW, ISIF_HSIZE.ADCR, ISIF_HSIZE.HSIZE, ISIF_CCDCFG.BSWD, ISIF_CCDCFG.MSBINV, ISIF_CCDCFG.SDRPACK bit fields control how pixel data are stored to SDRAM. 0x0: 16 bits / pixel 0x1: 12 bits / pixel 0x3: Reserved 0x2: 8 bits / pixel	RW	0x0

Table 8-967. Register Call Summary for Register ISIF_CCDCFG

ISS ISP

- ISS ISP ISIF Interface: [0] [1] [2]
- ISS ISP ISIF Expected Bandwidth on BL Ports: [3]
- ISS ISP ISIF Hardware Setup/Initialization: [4] [5] [6] [7] [8] [9] [10] [11] [12] [13]
- ISS ISP ISIF Register Accessibility During Frame Processing: [14] [15]
- ISS ISP ISIF Summary of Constraints: [16]
- ISS ISIF Register Summary: [17]
- ISS ISIF Register Description: [18] [19] [20] [21] [22] [23] [24] [25] [26] [27] [28] [29] [30] [31] [32]

Table 8-968. ISIF_DFCCTL

Address Offset	0x0000 008C		
Physical Address	0x5201 108C	**Instance**	ISS_ISIF
Description	VERTICAL LINE DEFCT CTRL REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED					VDFLSFT			VDFCUDA	VDFCSL		VDFCEN	RESERVED			

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:11	RESERVED		R	0x00
10:8	VDFLSFT	Vertical line Defect level shift value Defect Level (value to be subtracted from the data) is 8bit width, but can be up-shifted up to 6bits by VDFLSFT. Left shift value = VDFLSFT (Range: 0-6) Setting 7 to VDFLSFT is not allowed.	RW	0x0
7	VDFCUDA	Vertical line Defect Correction upper pixels disable. 0x0: The whole line is corrected. 0x1: Pixels upper than the defect are not corrected.	RW	0
6:5	VDFCSL	Vertical line Defect Correction mode select. 0x0: Defect level subtraction. Just fed through if data are saturating. 0x1: Defect level subtraction. Horizontal interpolation ((i-2)+(i+2))/2 if data are saturating. 0x3: Reserved 0x2: Horizontal interpolation ((i-2)+(i+2))/2.	RW	0x0

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Bits	Field Name	Description	Type	Reset
4	VDFCEN	Vertical line Defect Correction enable. This bit field is latched by VD. 0x0: Disable 0x1: Enable	RW	0
3:0	RESERVED		R	0x0

Table 8-969. Register Call Summary for Register ISIF_DFCCTL

ISS ISP

- ISS ISP ISIF Vertical Line Defect Correction (VDFC): [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10]
- ISS ISP ISIF Hardware Setup/Initialization: [11] [12] [13] [14] [15]
- ISS ISP ISIF Register Accessibility During Frame Processing: [16]
- ISS ISIF Register Summary: [17]

Table 8-970. ISIF_VDFSATLV

Address Offset	0x0000 0090		
Physical Address	0x5201 1090	**Instance**	ISS_ISIF
Description	VERTICAL LINE DEFCT CTRL REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED				VDFSLV											

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	RESERVED		R	0x0
11:0	VDFSLV	Vertical line Defect Correction saturation level. VDFSLV is U12 (Range: 0 - 4,095).	RW	0x000

Table 8-971. Register Call Summary for Register ISIF_VDFSATLV

ISS ISP

- ISS ISP ISIF Vertical Line Defect Correction (VDFC): [0]
- ISS ISP ISIF Hardware Setup/Initialization: [1]
- ISS ISP ISIF Register Accessibility During Frame Processing: [2]
- ISS ISIF Register Summary: [3]

Table 8-972. ISIF_DFCMEMCTL

Address Offset	0x0000 0094		
Physical Address	0x5201 1094	**Instance**	ISS_ISIF
Description	VERTICAL LINE DEFCT CTRL REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED											DFCMCLR	RESERVED	DFCMARST	DFCMRD	DFCMWR

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Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:5	RESERVED		R	0x000
4	DFCMCLR	Defect correction. Memory clear. Writing 1 to this bit clears the memory contents to all zero. It will be automatically cleared to `0` when the memory clear is completed.	RW	0
3	RESERVED		R	0
2	DFCMARST	Defect correction. Memory address reset. Setting DFCMWR or DFCMRD with LSCMARST set starts memory access to address offset 0. DFCMARST is automatically cleared if data transfer completes. Setting DFCMWR or DFCMRD with LSCMARST cleared starts memory access to the next address. 0x0: Increment the memory address 0x1: Clear the memory address to offset 0	RW	0
1	DFCMRD	Defect correction. Memory read [for debug purpose] Writing 1 to this bit starts reading from the memory. It will be automatically cleared when the data transfer is completed, and the data can be read from DFCMEM4-0.	RW	0
0	DFCMWR	Defect correction. Memory write Writing 1 to this bit starts writing to the memory. It will be automatically cleared when the data transfer is completed. DFCMEM4-0 should be set prior to the memory access.	RW	0

Table 8-973. Register Call Summary for Register ISIF_DFCMEMCTL

ISS ISP

- ISS ISP ISIF Vertical Line Defect Correction (VDFC): [0] [1] [2] [3] [4] [5] [6] [7]
- ISS ISP ISIF Hardware Setup/Initialization: [8] [9] [10]
- ISS ISIF Register Summary: [11]

Table 8-974. ISIF_DFCMEM0

Address Offset	0x0000 0098		
Physical Address	0x5201 1098	**Instance**	ISS_ISIF
Description	Defect correction memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								DFCMEM0							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12:0	DFCMEM0	Defect correction memory 0 Sets V position of the defects.	RW	0x0000

Table 8-975. Register Call Summary for Register ISIF_DFCMEM0

ISS ISP

- ISS ISP ISIF Vertical Line Defect Correction (VDFC): [0] [1] [2] [3]
- ISS ISP ISIF Hardware Setup/Initialization: [4]
- ISS ISIF Register Summary: [5]

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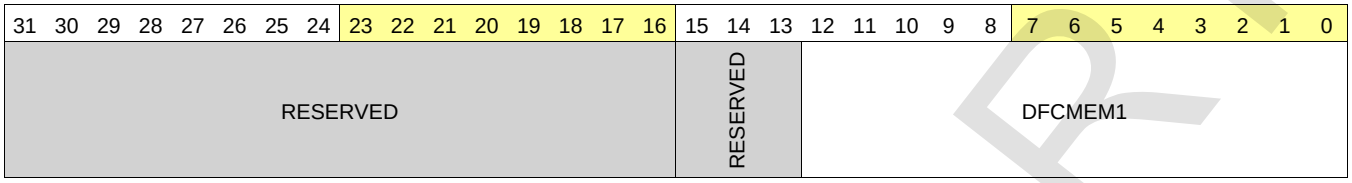
Table 8-976. ISIF_DFCMEM1

Address Offset	0x0000 009C		
Physical Address	0x5201 109C	**Instance**	ISS_ISIF
Description	Defect correction memory		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12:0	DFCMEM1	Defect correction memory 1 Sets H position of the defects.	RW	0x0000

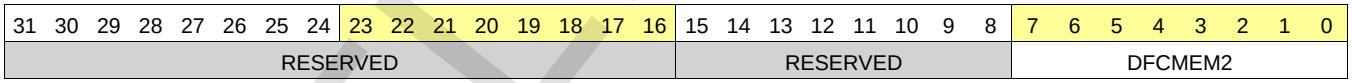
Table 8-977. Register Call Summary for Register ISIF_DFCMEM1

ISS ISP

- ISS ISP ISIF Vertical Line Defect Correction (VDFC): [0] [1] [2] [3]
- ISS ISP ISIF Hardware Setup/Initialization: [4]
- ISS ISIF Register Summary: [5]

Table 8-978. ISIF_DFCMEM2

Address Offset	0x0000 00A0		
Physical Address	0x5201 10A0	**Instance**	ISS_ISIF
Description	Defect correction memory		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:8	RESERVED		R	0x00
7:0	DFCMEM2	Defect correction Memory 2 Set SUB1: Defect level of the Vertical line defect position (V = Vdefect). DFCMEM2 can be up shifted according to VDFLSFT, and subtracted from the data for Vertical line defect correction.	RW	0x00

Table 8-979. Register Call Summary for Register ISIF_DFCMEM2

ISS ISP

- ISS ISP ISIF Vertical Line Defect Correction (VDFC): [0] [1] [2]
- ISS ISP ISIF Hardware Setup/Initialization: [3]
- ISS ISIF Register Summary: [4]

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Table 8-980. ISIF_DFCMEM3

Address Offset	0x0000 00A4		
Physical Address	0x5201 10A4	**Instance**	ISS_ISIF
Description	Defect correction memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								DFCMEM3							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:8	RESERVED		R	0x00
7:0	DFCMEM3	Defect correction Memory 3 Set SUB2: Defect level of the pixels upper than the Vertical line defect (V Vdefect). DFCMEM3 can be up shifted according to VDFLSFT, and subtracted from the data for Vertical line defect correction.	RW	0x00

Table 8-981. Register Call Summary for Register ISIF_DFCMEM3

ISS ISP

- ISS ISP ISIF Vertical Line Defect Correction (VDFC): [0] [1] [2]
- ISS ISP ISIF Hardware Setup/Initialization: [3]
- ISS ISIF Register Summary: [4]

Table 8-982. ISIF_DFCMEM4

Address Offset	0x0000 00A8		
Physical Address	0x5201 10A8	**Instance**	ISS_ISIF
Description	Defect correction memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								DFCMEM4							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:8	RESERVED		R	0x00
7:0	DFCMEM4	Memory 4 Set SUB3: Defect level of the pixels lower than the Vertical line defect (V Vdefect). DFCMEM4 can be up shifted according to VDFLSFT, and subtracted from the data for Vertical line defect correction.	RW	0x00

Table 8-983. Register Call Summary for Register ISIF_DFCMEM4

ISS ISP

- ISS ISP ISIF Vertical Line Defect Correction (VDFC): [0] [1] [2]
- ISS ISP ISIF Hardware Setup/Initialization: [3]
- ISS ISIF Register Summary: [4]

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Table 8-984. ISIF_CLAMPCFG

Address Offset	0x0000 00AC		
Physical Address	0x5201 10AC	**Instance**	ISS_ISIF
Description	BLACK CLAMP CTRL REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED											CLMD	RESERVED		CLHMD		CLEN

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:5	RESERVED		R	0x000
4	CLMD	Black clamp mode Clamp value can be calculated regardless of the color or can be calculated separately for each 4 colors. 0x0: Clamp value calculated regardless of the pixel color. 0x1: Clamp value calculated separately for each 4 colors.	RW	0
3	RESERVED		R	0
2:1	CLHMD	Horizontal Clamp mode 0x0: Horizontal clamp disabled. Only the Vertical clamp value is subtracted from the Image data. 0x1: Horizontal clamp value calculation enabled. The calculated Horizontal clamp value is subtracted from the Image data along with the Vertical clamp value. 0x3: Reserved 0x2: Horizontal clamp value not updated. The Horizontal clamp value used for the previous image is subtracted from the Image data along with the Vertical clamp value.	RW	0x0
0	CLEN	Black Clamp Enable Enables clamp value to be subtracted from Image data. 0x0: Disable 0x1: Enable	RW	0

Table 8-985. Register Call Summary for Register ISIF_CLAMPCFG

ISS ISP

- ISS ISP ISIF Black Clamp: [0] [1] [2] [3] [4]
- ISS ISP ISIF Hardware Setup/Initialization: [5] [6]
- ISS ISP ISIF Register Accessibility During Frame Processing: [7]
- ISS ISIF Register Summary: [8]
- ISS ISIF Register Description: [9] [10]

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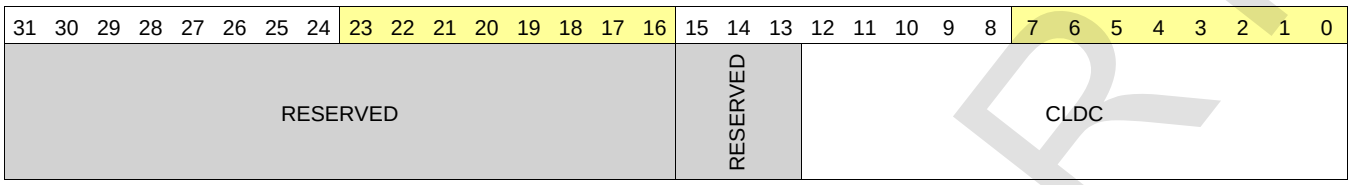
Table 8-986. ISIF_CLDCOFST

Address Offset	0x0000 00B0		
Physical Address	0x5201 10B0	**Instance**	ISS_ISIF
Description	BLACK CLAMP CTRL REGISTER		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12:0	CLDC	DC offset for black clamp This value is added to the incoming pixels regardless whether optical black clamp is enabled (ISIF_CLAMPCFG.CLEN). This value is in S13Q0 format.	RW	0x0000

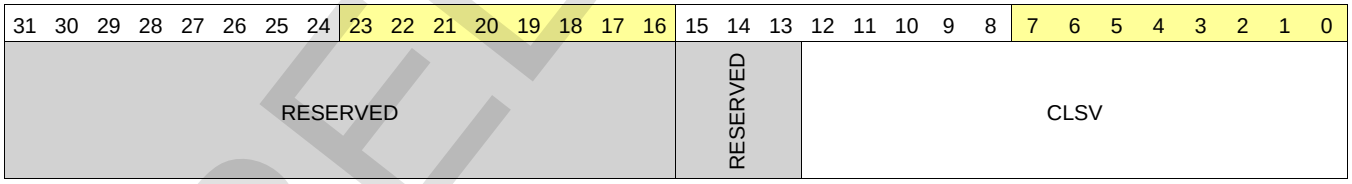
Table 8-987. Register Call Summary for Register ISIF_CLDCOFST

ISS ISP

- ISS ISP ISIF Black Clamp: [0]
- ISS ISP ISIF Hardware Setup/Initialization: [1] [2]
- ISS ISIF Register Summary: [3]

Table 8-988. ISIF_CLSV

Address Offset	0x0000 00B4		
Physical Address	0x5201 10B4	**Instance**	ISS_ISIF
Description	BLACK CLAMP CTRL REGISTER		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12:0	CLSV	Black Clamp Start position (V). Sets the line number where clamp value subtraction starts. Range: 0 - 8191	RW	0x0000

Table 8-989. Register Call Summary for Register ISIF_CLSV

ISS ISP

- ISS ISP ISIF Hardware Setup/Initialization: [0]
- ISS ISIF Register Summary: [1]

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Table 8-990. ISIF_CLHWIN0

Address Offset	0x0000 00B8		
Physical Address	0x5201 10B8	**Instance**	ISS_ISIF
Description	BLACK CLAMP CTRL REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED		CLHWN		RESERVED		CLHWM		RESERVED	CLHLMT	CLHWBS	CLHWC				

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:14	RESERVED		R	0x0
13:12	CLHWN	Horizontal Black clamp - Vertical dimension of a Window (2^N). 0x0: Window is 2 pixels tall (N=1) 0x1: Window is 4 pixels tall (N=2) 0x3: Window is 16 pixels tall (N=4) 0x2: Window is 8 pixels tall (N=3)	RW	0x0
11:10	RESERVED		R	0x0
9:8	CLHWM	Horizontal Black clamp - Horizontal dimension of a Window (2^M). 0x0: Window is 32 pixels wide (M=5) 0x1: Window is 64 pixels wide (M=6) 0x3: Window is 256 pixels wide (M=8) 0x2: Window is 128 pixels wide (M=7)	RW	0x0
7	RESERVED		R	0
6	CLHLMT	Horizontal Black clamp - Pixel value limitation for the Horizontal clamp value calculation. If this bit is set, the maximum pixel value to be used for the clamp value calculation would be limited to 1023. By setting this bit, the pixel value greater than 1023 will be replaced by the last pixel value which was equal to or less than 1023. In case ISIF_CLAMPCFG.CLMD=1 (4-color mode), the pixel value greater than 1023 will be replaced by the last pixel value of the same color which was equal to or less than 1023. 0x0: Limitation disabled 0x1: Limitation enabled	RW	0
5	CLHWBS	Horizontal Black clamp - Base Window select 0x0: The most left window 0x1: The most right window	RW	0
4:0	CLHWC	Horizontal Black clamp - Window count per color Window count = CLHWC+1 Range: 1 - 32	RW	0x00

Table 8-991. Register Call Summary for Register ISIF_CLHWIN0

ISS ISP

- ISS ISP ISIF Black Clamp: [0] [1] [2] [3] [4] [5] [6]
- ISS ISP ISIF Hardware Setup/Initialization: [7] [8] [9] [10] [11]
- ISS ISIF Register Summary: [12]

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Table 8-992. ISIF_CLHWIN1

Address Offset	0x0000 00BC		
Physical Address	0x5201 10BC	**Instance**	ISS_ISIF
Description	BLACK CLAMP CTRL REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED			CLHSH												

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12:0	CLHSH	Horizontal black clamp. Window Start position (H). Range: 0 - 8191	RW	0x0000

Table 8-993. Register Call Summary for Register ISIF_CLHWIN1

ISS ISP

- ISS ISP ISIF Black Clamp: [0]
- ISS ISP ISIF Hardware Setup/Initialization: [1]
- ISS ISIF Register Summary: [2]

Table 8-994. ISIF_CLHWIN2

Address Offset	0x0000 00C0		
Physical Address	0x5201 10C0	**Instance**	ISS_ISIF
Description	BLACK CLAMP CTRL REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED			CLHSV												

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12:0	CLHSV	Horizontal black clamp. Window Start position (V). Range: 0 - 8191	RW	0x0000

Table 8-995. Register Call Summary for Register ISIF_CLHWIN2

ISS ISP

- ISS ISP ISIF Black Clamp: [0]
- ISS ISP ISIF Hardware Setup/Initialization: [1]
- ISS ISIF Register Summary: [2]

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Table 8-996. ISIF_CLVRV

Address Offset	0x0000 00C4		
Physical Address	0x5201 10C4	**Instance**	ISS_ISIF
Description	BLACK CLAMP CTRL REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED				CLVRV											

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	RESERVED		R	0x0
11:0	CLVRV	Vertical black clamp reset value. (U12) Range: 0 to 4095	RW	0x000

Table 8-997. Register Call Summary for Register ISIF_CLVRV

ISS ISP

- ISS ISP ISIF Black Clamp: [0]
- ISS ISP ISIF Hardware Setup/Initialization: [1]
- ISS ISIF Register Summary: [2]

Table 8-998. ISIF_CLVWIN0

Address Offset	0x0000 00C8		
Physical Address	0x5201 10C8	**Instance**	ISS_ISIF
Description	BLACK CLAMP CTRL REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																CLVCOEF								RESERVED		CLVRVSL		RESERVED		CLVOBH	

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:8	CLVCOEF	Vertical Black clamp - Line average coefficient (k). Set a coefficient which is applied to the line average for clamp value calculation. (1-k) is applied to the clamp value of the previous line. Value in the U8Q8 format, the range is 0 to 255/256.	RW	0x00
7:6	RESERVED		R	0x0
5:4	CLVRVSL	Vertical Black clamp - reset value selection Select the reset value for the clamp value of the previous line 0x0: The base value calculated for Horizontal direction 0x1: Value set via the configuration register 0x3: Reserved 0x2: No update (same as the previous image)	RW	0x0
3	RESERVED		R	0

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Bits	Field Name	Description	Type	Reset
2:0	CLVOBH	Vertical Black clamp - Optical Black H valid (2^L). 0x6: Reserved 0x1: 4 pixels wide (L=2) 0x7: Reserved 0x0: 2 pixels wide (L=1) 0x2: 8 pixels wide (L=3) 0x4: 32 pixels wide (L=5) 0x5: 64 pixels wide (L=6) 0x3: 16 pixels wide (L=4)	RW	0x0

Table 8-999. Register Call Summary for Register ISIF_CLVWIN0

ISS ISP
- ISS ISP ISIF Black Clamp: [0] [1] [2] [3] [4]
- ISS ISP ISIF Hardware Setup/Initialization: [5] [6] [7]
- ISS ISIF Register Summary: [8]

Table 8-1000. ISIF_CLVWIN1

Address Offset	0x0000 00CC		
Physical Address	0x5201 10CC	**Instance**	ISS_ISIF
Description	BLACK CLAMP CTRL REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								CLVSH							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12:0	CLVSH	Vertical black clamp. Window Start position (H). Range: 0 - 8191	RW	0x0000

Table 8-1001. Register Call Summary for Register ISIF_CLVWIN1

ISS ISP
- ISS ISP ISIF Black Clamp: [0]
- ISS ISP ISIF Hardware Setup/Initialization: [1]
- ISS ISIF Register Summary: [2]

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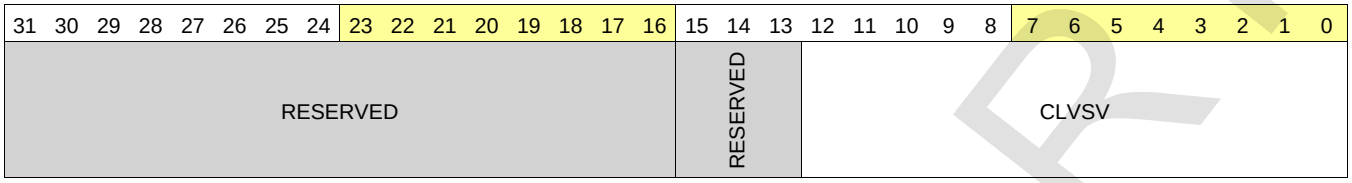
Table 8-1002. ISIF_CLVWIN2

Address Offset	0x0000 00D0		
Physical Address	0x5201 10D0	**Instance**	ISS_ISIF
Description	BLACK CLAMP CTRL REGISTER		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12:0	CLVSV	Vertical black clamp. Window Start position (V). Range: 0 - 8191	RW	0x0000

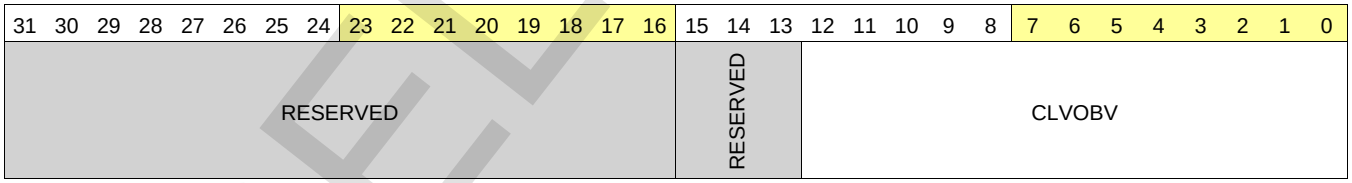
Table 8-1003. Register Call Summary for Register ISIF_CLVWIN2

ISS ISP

- ISS ISP ISIF Black Clamp: [0]
- ISS ISP ISIF Hardware Setup/Initialization: [1]
- ISS ISIF Register Summary: [2]

Table 8-1004. ISIF_CLVWIN3

Address Offset	0x0000 00D4		
Physical Address	0x5201 10D4	**Instance**	ISS_ISIF
Description	BLACK CLAMP CTRL REGISTER		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12:0	CLVOBV	Vertical black clamp. Optical black V valid (V). Range: 0 - 8191	RW	0x0000

Table 8-1005. Register Call Summary for Register ISIF_CLVWIN3

ISS ISP

- ISS ISP ISIF Black Clamp: [0]
- ISS ISP ISIF Hardware Setup/Initialization: [1]
- ISS ISIF Register Summary: [2]

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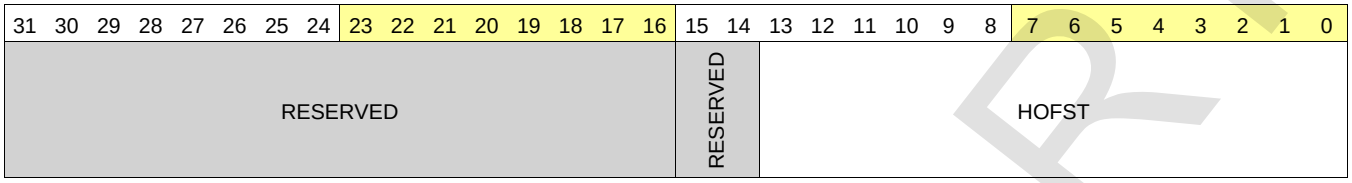
Table 8-1006. ISIF_LSCHOFST

Address Offset	0x0000 00D8		
Physical Address	0x5201 10D8	**Instance**	ISS_ISIF
Description	2D Lens Shading Correction Register		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:14	RESERVED		R	0x0
13:0	HOFST	H direction Data offset for Lens Shading Correction. Range: 0-16,383 Not valid if the Formatter is enabled.	RW	0x0000

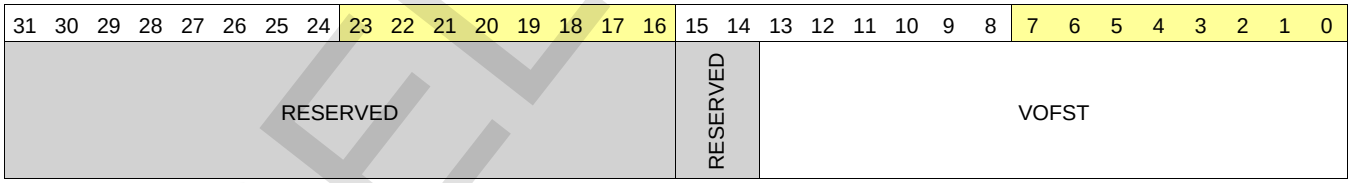
Table 8-1007. Register Call Summary for Register ISIF_LSCHOFST

ISS ISP

- ISS ISP ISIF Hardware Setup/Initialization: [0]
- ISS ISP ISIF Register Accessibility During Frame Processing: [1]
- ISS ISIF Register Summary: [2]

Table 8-1008. ISIF_LSCVOFST

Address Offset	0x0000 00DC		
Physical Address	0x5201 10DC	**Instance**	ISS_ISIF
Description	2D Lens Shading Correction Register		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:14	RESERVED		R	0x0
13:0	VOFST	V direction Data offset for Lens Shading Correction. Range: 0-16,383	RW	0x0000

Table 8-1009. Register Call Summary for Register ISIF_LSCVOFST

ISS ISP

- ISS ISP ISIF Hardware Setup/Initialization: [0]
- ISS ISP ISIF Register Accessibility During Frame Processing: [1]
- ISS ISIF Register Summary: [2]

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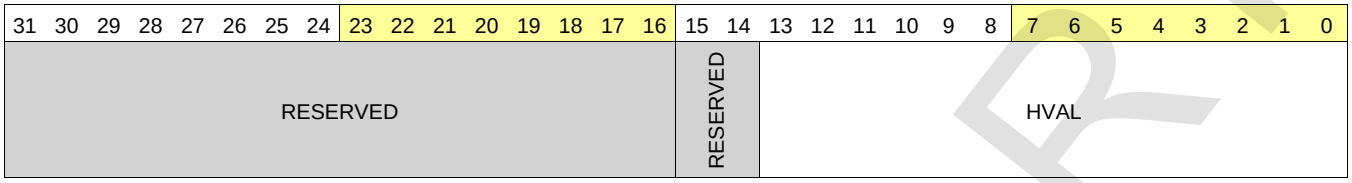
Table 8-1010. ISIF_LSCHVAL

Address Offset	0x0000 00E0		
Physical Address	0x5201 10E0	**Instance**	ISS_ISIF
Description	2D Lens Shading Correction Register		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:14	RESERVED		R	0x0
13:0	HVAL	Number of valid pixels in H direction. HVAL is for LSC. Number of valid pixels = HVAL+ 1	RW	0x0000

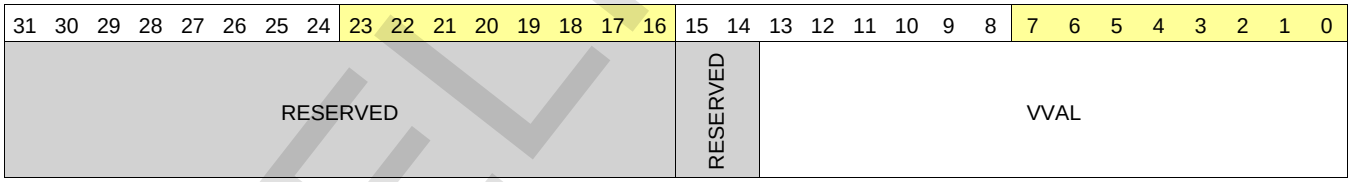
Table 8-1011. Register Call Summary for Register ISIF_LSCHVAL

ISS ISP

- ISS ISP ISIF Hardware Setup/Initialization: [0]
- ISS ISIF Register Summary: [1]

Table 8-1012. ISIF_LSCVVAL

Address Offset	0x0000 00E4		
Physical Address	0x5201 10E4	**Instance**	ISS_ISIF
Description	2D Lens Shading Correction Register		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:14	RESERVED		R	0x0
13:0	VVAL	Number of valid lines in V direction. VVAL is for LSC. Number of valid lines = VVAL+ 1	RW	0x0000

Table 8-1013. Register Call Summary for Register ISIF_LSCVVAL

ISS ISP

- ISS ISP ISIF Hardware Setup/Initialization: [0]
- ISS ISIF Register Summary: [1]

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Table 8-1014. ISIF_2DLSCCFG

Address Offset	0x0000 00E8		
Physical Address	0x5201 10E8	**Instance**	ISS_ISIF
Description	2D Lens Shading Correction Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED	GAIN_MODE_M			RESERVED	GAIN_MODE_N			BUSY	RESERVED			GAIN_FORMAT			ENABLE

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15	RESERVED		R	0
14:12	GAIN_MODE_M	Define the horizontal dimension of a paxel. Possible values are listed below. 0x6: Paxel is 64 pixels tall (M=64) 0x1: Reserved 0x7: Paxel is 128 pixels tall (M=128) 0x0: Reserved 0x2: Reserved 0x4: Paxel is 16 pixels tall (M=16) 0x5: Paxel is 32 pixels tall (M=32) 0x3: Paxel is 8 pixels tall (M=8)	RW	0x6
11	RESERVED		R	0
10:8	GAIN_MODE_N	Define the vertical dimension of a paxel. Possible values are listed below. 0x6: Paxel is 64 pixels tall (N=64) 0x1: Reserved 0x7: Paxel is 128 pixels tall (N=128) 0x0: Reserved 0x2: Reserved 0x4: Paxel is 16 pixels tall (N=16) 0x5: Paxel is 32 pixels tall (N=32) 0x3: Paxel is 8 pixels tall (N=8)	RW	0x6
7	BUSY	Busy bit Read 0x1: Busy Read 0x0: Idle	R	0
6:4	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
3:1	GAIN_FORMAT	Sets gain table format 0x6: Coded as 3-bit integer, 5-bit fraction Range from 0 to 7+31/32 0x1: Coded as 8-bit fraction + 1.0 of base Range from 1 to 1+255/256 0x7: Coded as 3-bit integer, 5-bit fraction + 1.0 Range from 1 to 8+31/32 0x0: Coded as 8-bit fraction Range from 0 to 255/256 0x2: Coded as 1-bit integer, 7-bit fraction Range from 0 to 1+127/128 0x4: Coded as 2-bit integer, 6-bit fraction Range from 0 to 3+63/64 0x5: Coded as 2-bit integer, 6-bit fraction + 1.0 Range from 1 to 4+63/64 0x3: Coded as 1-bit integer, 7-bit fraction + 1.0 Range from 1 to 2+127/128	RW	0x0
0	ENABLE	Enables/disables LSC 0x0: Disables the module at the end of the current frame. 0x1: Enables the module.	RW	0

Table 8-1015. Register Call Summary for Register ISIF_2DLSCCFG

ISS ISP

- ISS ISP ISIF Lens Shading Correction (2D-LSC): [0] [1] [2] [3] [4] [5]
- ISS ISP ISIF Expected Bandwidth on BL Ports: [6] [7] [8] [9] [10] [11] [12] [13]
- ISS ISP ISIF Hardware Setup/Initialization: [14] [15] [16] [17] [18]
- ISS ISIF Register Summary: [19]

Table 8-1016. ISIF_2DLSCOFST

Address Offset	0x0000 00EC		
Physical Address	0x5201 10EC	**Instance**	ISS_ISIF
Description	2D Lens Shading Correction Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																OFSTSF								RESERVED	OFSTSFT			RESERVED			OFSTEN

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:8	OFSTSF	Scaling factor for Offsets (U8Q7) Range: 0 to 1+127/128	RW	0x80
7	RESERVED		R	0

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Bits	Field Name	Description	Type	Reset
6:4	OFSTSFT	Shift up value for Offsets (S8Q0) 0x6: Reserved 0x1: 1bit left shift 0x7: Reserved 0x0: No shift 0x2: 2bits left shift 0x4: 4bits left shift 0x5: 5bits left shift 0x3: 3bits left shift	RW	0x0
3:1	RESERVED		R	0x0
0	OFSTEN	Enables/disables Offset control in LSC 0x0: Disable 0x1: Enable	RW	0

Table 8-1017. Register Call Summary for Register ISIF_2DLSCOFST

ISS ISP

- ISS ISP ISIF Lens Shading Correction (2D-LSC): [0] [1] [2] [3] [4]
- ISS ISP ISIF Expected Bandwidth on BL Ports: [5]
- ISS ISP ISIF Hardware Setup/Initialization: [6] [7] [8]
- ISS ISIF Register Summary: [9]

Table 8-1018. ISIF_2DLSCINI

Address Offset	0x0000 00F0		
Physical Address	0x5201 10F0	**Instance**	ISS_ISIF
Description	2D Lens Shading Correction Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED	Y							RESERVED	X						

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15	RESERVED		R	0
14:8	Y	Initial Y Y position, in pixels, of the first active pixel in reference to the first active paxel. Must be an even number.	RW	0x00
7	RESERVED		R	0
6:0	X	Initial X X position, in pixels, of the first active pixel in reference to the first active paxel. Must be an even number.	RW	0x00

Table 8-1019. Register Call Summary for Register ISIF_2DLSCINI

ISS ISP

- ISS ISP ISIF Lens Shading Correction (2D-LSC): [0] [1]
- ISS ISP ISIF Hardware Setup/Initialization: [2] [3]
- ISS ISP ISIF Summary of Constraints: [4]
- ISS ISIF Register Summary: [5]

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Table 8-1020. ISIF_2DLSCGRBU

Address Offset	0x0000 00F4		
Physical Address	0x5201 10F4	**Instance**	ISS_ISIF
Description	2D Lens Shading Correction Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																BASE31_16															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:0	BASE31_16	Gain Table address base (Upper 16-bits) Table address in bytes. Table is 32-bit aligned so this register must be a multiple of 4. This bit field sets the address of the gain table in memory.	RW	0x0000

Table 8-1021. Register Call Summary for Register ISIF_2DLSCGRBU

ISS ISP

- ISS ISP ISIF Lens Shading Correction (2D-LSC): [0]
- ISS ISP ISIF Hardware Setup/Initialization: [1]
- ISS ISIF Register Summary: [2]

Table 8-1022. ISIF_2DLSCGRBL

Address Offset	0x0000 00F8		
Physical Address	0x5201 10F8	**Instance**	ISS_ISIF
Description	2D Lens Shading Correction Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																BASE15_0															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:0	BASE15_0	Gain Table address base (Lower 16-bits) Table address in bytes. Table is 32-bit aligned so this register must be a multiple of 4. This bit field sets the address of the gain table in memory.	RW	0x0000

Table 8-1023. Register Call Summary for Register ISIF_2DLSCGRBL

ISS ISP

- ISS ISP ISIF Lens Shading Correction (2D-LSC): [0]
- ISS ISP ISIF Hardware Setup/Initialization: [1]
- ISS ISIF Register Summary: [2]

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Table 8-1024. ISIF_2DLSCGROF

Address Offset	0x0000 00FC		
Physical Address	0x5201 10FC	**Instance**	ISS_ISIF
Description	2D Lens Shading Correction Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																OFFSET															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:0	OFFSET	Gain Table offset Defines the length, in bytes, of one row of the table. Table is 32-bit aligned, so this value must be a multiple of 4. Note that the row in memory could be longer than what LSC uses.	RW	0x0000

Table 8-1025. Register Call Summary for Register ISIF_2DLSCGROF

ISS ISP

- ISS ISP ISIF Lens Shading Correction (2D-LSC): [0]
- ISS ISP ISIF Hardware Setup/Initialization: [1]
- ISS ISIF Register Summary: [2]

Table 8-1026. ISIF_2DLSCORBU

Address Offset	0x0000 0100		
Physical Address	0x5201 1100	**Instance**	ISS_ISIF
Description	2D Lens Shading Correction Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																BASE															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:0	BASE	Offset Table address base (Upper 16-bits) Table address in bytes. Table is 32-bit aligned so this register must be a multiple of 4. This bit field sets the address of the gain table in memory.	RW	0x0000

Table 8-1027. Register Call Summary for Register ISIF_2DLSCORBU

ISS ISP

- ISS ISP ISIF Lens Shading Correction (2D-LSC): [0]
- ISS ISP ISIF Hardware Setup/Initialization: [1]
- ISS ISIF Register Summary: [2]

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Table 8-1028. ISIF_2DLSCORBL

Address Offset	0x0000 0104		
Physical Address	0x5201 1104	**Instance**	ISS_ISIF
Description	2D Lens Shading Correction Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																BASE															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:0	BASE	Offset Table address base (Lower 16-bits) Table address in bytes. Table is 32-bit aligned so this register must be a multiple of 4. This bit field sets the address of the gain table in memory.	RW	0x0000

Table 8-1029. Register Call Summary for Register ISIF_2DLSCORBL

ISS ISP

- ISS ISP ISIF Lens Shading Correction (2D-LSC): [0]
- ISS ISP ISIF Hardware Setup/Initialization: [1]
- ISS ISIF Register Summary: [2]

Table 8-1030. ISIF_2DLSCOROF

Address Offset	0x0000 0108		
Physical Address	0x5201 1108	**Instance**	ISS_ISIF
Description	2D Lens Shading Correction Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																OFFSET															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:0	OFFSET	Offset Table offset Defines the length, in bytes, of one row of the table. Table is 32-bit aligned, so this value must be a multiple of 4. Note that the row in memory could be longer than what LSC uses.	RW	0x0000

Table 8-1031. Register Call Summary for Register ISIF_2DLSCOROF

ISS ISP

- ISS ISP ISIF Lens Shading Correction (2D-LSC): [0]
- ISS ISP ISIF Hardware Setup/Initialization: [1]
- ISS ISIF Register Summary: [2]

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Table 8-1032. ISIF_2DLSCIRQEN

Address Offset	0x0000 010C		
Physical Address	0x5201 110C	**Instance**	ISS_ISIF
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED												SOF	PREFETCH_COMPLETED	PREFETCH_ERROR	DONE

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:4	RESERVED		R	0x000
3	SOF	Interrupt status for LSC SOF Indicates the start of the LSC valid region. LSC configuration registers can be updated after LSC SOF for the next frame. 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
2	PREFETCH_COMPLETED	Interrupt enable for Prefetch Complete Indicates current state of the prefetch buffer. Could be used to start sending the data once the buffer is full to minimize the risk of an underflow. This event is triggered when the buffer contains 3 full paxel rows. 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
1	PREFETCH_ERROR	Interrupt enable for Prefetch Error The prefetch error indicates when the gain table was read to slowly from SDRAM. When this event is pending the module goes into transparent mode (output=input). Normal operation can be resumed at the start of the next frame after 1) clearing this event 2) disabling the LSC module 3) enabling it 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
0	DONE	Interrupt enable for LSC Done The event is triggered when the internal state of LSC toggles from BUSY to IDLE. 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0

Table 8-1033. Register Call Summary for Register ISIF_2DLSCIRQEN

ISS ISP

- ISS ISP ISIF Lens Shading Correction (2D-LSC): [0]
- ISS ISP ISIF Hardware Setup/Initialization: [1] [2] [3] [4]
- ISS ISIF Register Summary: [5]

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Table 8-1034. ISIF_2DLSCIRQST

Address Offset	0x0000 0110		
Physical Address	0x5201 1110	**Instance**	ISS_ISIF
Description	2D Lens Shading Correction Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED												SOF	PREFETCH_COMPLETED	PREFETCH_ERROR	DONE

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:4	RESERVED		R	0x000
3	SOF	Interrupt status for LSC SOF Indicates the start of the LSC valid region. LSC configuration registers can be updated after LSC SOF for the next frame. 0x0: Event is not pending (r) Bit remains unchanged (w) 0x1: Event is pending (r) Event is cleared (w)	RW	0
2	PREFETCH_COMPLETED	Interrupt status for Prefetch Complete Indicates current state of the prefetch buffer. Could be used to start sending the data once the buffer is full to minimize the risk of an underflow. This event is triggered when the buffer contains 3 full paxel rows. It could be used to minimize buffer underflow risks. 0x0: Event is not pending (r) Bit remains unchanged (w) 0x1: Event is pending (r) Event is cleared (w)	RW	0
1	PREFETCH_ERROR	Interrupt status for Prefetch Error The prefetch error indicates when the gain table was read to slowly from SDRAM. When this event is pending the module goes into transparent mode (output=input). Normal operation can be resumed at the start of the next frame after 1) clearing this event 2) disabling the LSC module 3) enabling it 0x0: Event is not pending (r) Bit remains unchanged (w) 0x1: Event is pending (r) Event is cleared (w)	RW	0
0	DONE	Interrupt status for LSC Done The event is triggered when the internal state of LSC toggles from BUSY to IDLE. 0x0: Event is not pending (r) Bit remains unchanged (w) 0x1: Event is pending (r) Event is cleared (w)	RW	0

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Table 8-1035. Register Call Summary for Register ISIF_2DLSCIRQST

ISS ISP

- ISS ISP ISIF Lens Shading Correction (2D-LSC): [0] [1] [2] [3] [4] [5] [6] [7] [8] [9]
- ISS ISIF Register Summary: [10]

Table 8-1036. ISIF_FMTCFG

Address Offset	0x0000 0114		
Physical Address	0x5201 1114	**Instance**	ISS_ISIF
Description	Input Data Formatter Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				FMTAINC				RESERVED		LNUM		RESERVED		LNALT	FMTCBL	FMTEN

Bits	Field Name	Description	Type	Reset
31:12	RESERVED		R	0x00000
11:8	FMTAINC	Address increment Address increment = (FMTAINC + 1) Range (1-16) *This bit is latched by VD.	RW	0x0
7:6	RESERVED		R	0x0
5:4	LNUM	Split/Combine number of lines *This bit is latched by VD. 0x0: 1 output line 0x1: 1 input line - 2 output lines (FMTCBL=0) 2 input lines - 1 output line (FMTCBL=1) 0x3: 1 input line - 4 output lines (FMTCBL=0) 4 input lines - 1 output line (FMTCBL=1) 0x2: 1 input line - 3 output lines (FMTCBL=0) 3 input lines - 1 output line (FMTCBL=1)	RW	0x0
3	RESERVED		R	0
2	LNALT	Line alternating *This bit is latched by VD. 0x0: Normal mode 0x1: Line alternative mode	RW	0
1	FMTCBL	Combine Input lines *This bit is latched by VD. 0x0: Split 1 input line into multiple output lines 0x1: Combine multiple input lines into 1 output line	RW	0
0	FMTEN	CCD Formatter enable *This bit is latched by VD. 0x0: Disable 0x1: Enable	RW	0

Table 8-1037. Register Call Summary for Register ISIF_FMTCFG

ISS ISP

- ISS ISP ISIF Input Data Formatter: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20]
- ISS ISP ISIF Hardware Setup/Initialization: [21] [22] [23] [24] [25]
- ISS ISIF Register Summary: [26]

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Table 8-1038. ISIF_FMTPLEN

Address Offset	0x0000 0118		
Physical Address	0x5201 1118	**Instance**	ISS_ISIF
Description	Input Data Formatter Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																FMTPLEN3				RESERVED		FMTPLEN2		FMTPLEN1				FMTPLEN0			

Bits	Field Name	Description	Type	Reset
31:15	RESERVED		R	0x00000
14:12	FMTPLEN3	Number of program entries for SET3 Number of entries = (FMTPLEN3 + 1) Range: 1-8 Valid only if FMTCBL is set *This bit is latched by VD.	RW	0x0
11	RESERVED		R	0
10:8	FMTPLEN2	Number of program entries for SET2 Number of entries = (FMTPLEN2 + 1) Range: 1-8 Valid only if FMTCBL is set *This bit is latched by VD.	RW	0x0
7:4	FMTPLEN1	Number of program entries for SET1 Number of entries = (FMTPLEN1 + 1) Range: 1-16 (FMTCBL = 0) 1-8 (FMTCBL = 1) Setting a value greater than 7 to FMTPLEN1 is not allowed if FMTCBL is set *This bit is latched by VD.	RW	0x0
3:0	FMTPLEN0	Number of program entries for SET0 Number of entries = (PLEN0 + 1) Range: 1-16 (FMTCBL = 0) 1-8 (FMTCBL = 1) Setting a value greater than 7 to FMTPLEN1 is not allowed if FMTCBL is set *This bit is latched by VD.	RW	0x0

Table 8-1039. Register Call Summary for Register ISIF_FMTPLEN

ISS ISP

- ISS ISP ISIF Input Data Formatter: [0] [1] [2] [3] [4] [5] [6] [7]
- ISS ISP ISIF Hardware Setup/Initialization: [8] [9] [10] [11]
- ISS ISIF Register Summary: [12]

Table 8-1040. ISIF_FMTSPH

Address Offset	0x0000 011C		
Physical Address	0x5201 111C	**Instance**	ISS_ISIF
Description	Input Data Formatter Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																FMTSPH															

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Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000
12:0	FMTSPH	The first pixel in a line fed into the formatter	RW	0x0000

Table 8-1041. Register Call Summary for Register ISIF_FMTSPH

ISS ISP

- ISS ISP ISIF Input Data Formatter: [0] [1] [2]
- ISS ISP ISIF Color Space Converter: [3]
- ISS ISP ISIF Hardware Setup/Initialization: [4]
- ISS ISP ISIF Register Accessibility During Frame Processing: [5]
- ISS ISIF Register Summary: [6]

Table 8-1042. ISIF_FMTLNH

Address Offset	0x0000 0120		
Physical Address	0x5201 1120	**Instance**	ISS_ISIF
Description	Input Data Formatter Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								FMTLNH							

Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000
12:0	FMTLNH	Number of pixels in a line fed to the formatter. Number of pixels = FMTLNH + 1	RW	0x0000

Table 8-1043. Register Call Summary for Register ISIF_FMTLNH

ISS ISP

- ISS ISP ISIF Input Data Formatter: [0] [1] [2]
- ISS ISP ISIF Color Space Converter: [3]
- ISS ISP ISIF Hardware Setup/Initialization: [4]
- ISS ISP ISIF Register Accessibility During Frame Processing: [5]
- ISS ISIF Register Summary: [6]

Table 8-1044. ISIF_FMTLSV

Address Offset	0x0000 0124		
Physical Address	0x5201 1124	**Instance**	ISS_ISIF
Description	Input Data Formatter Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								FMTSLV							

Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000
12:0	FMTSLV	Start line vertical	RW	0x0000

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Table 8-1045. Register Call Summary for Register ISIF_FMTLSV

ISS ISP
- ISS ISP ISIF Input Data Formatter: [0] [1] [2]
- ISS ISP ISIF Color Space Converter: [3]
- ISS ISP ISIF Hardware Setup/Initialization: [4]
- ISS ISP ISIF Register Accessibility During Frame Processing: [5]
- ISS ISIF Register Summary: [6]

Table 8-1046. ISIF_FMTLNV

Address Offset	0x0000 0128		
Physical Address	0x5201 1128	**Instance**	ISS_ISIF
Description	Input Data Formatter Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																FMTLNV															

Bits	Field Name	Description	Type	Reset
31:15	RESERVED		R	0x00000
14:0	FMTLNV	Number of lines in vertical Number of lines = FMTLNV + 1	RW	0x0000

Table 8-1047. Register Call Summary for Register ISIF_FMTLNV

ISS ISP
- ISS ISP ISIF Input Data Formatter: [0] [1] [2]
- ISS ISP ISIF Color Space Converter: [3]
- ISS ISP ISIF Hardware Setup/Initialization: [4]
- ISS ISP ISIF Register Accessibility During Frame Processing: [5]
- ISS ISIF Register Summary: [6]

Table 8-1048. ISIF_FMTRLEN

Address Offset	0x0000 012C		
Physical Address	0x5201 112C	**Instance**	ISS_ISIF
Description	Input Data Formatter Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																			FMTRLEN												

Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000
12:0	FMTRLEN	Number of pixels in an output line Maximum value = 4480	RW	0x0000

Table 8-1049. Register Call Summary for Register ISIF_FMTRLEN

ISS ISP
- ISS ISP ISIF Input Data Formatter: [0] [1] [2]
- ISS ISP ISIF Hardware Setup/Initialization: [3]
- ISS ISIF Register Summary: [4]

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Table 8-1050. ISIF_FMTHCNT

Address Offset	0x0000 0130		
Physical Address	0x5201 1130	**Instance**	ISS_ISIF
Description	Input Data Formatter Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								FMTHCNT							

Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000
12:0	FMTHCNT	HD interval for output lines Set all 0 to this register if combining multiple lines into a single line	RW	0x0000

Table 8-1051. Register Call Summary for Register ISIF_FMTHCNT

ISS ISP

- ISS ISP ISIF Input Data Formatter: [0] [1] [2]
- ISS ISP ISIF Hardware Setup/Initialization: [3]
- ISS ISIF Register Summary: [4]

Table 8-1052. ISIF_FMTAPTR0

Address Offset	0x0000 0134		
Physical Address	0x5201 1134	**Instance**	ISS_ISIF
Description	Input Data Formatter Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																LINE			INIT												

Bits	Field Name	Description	Type	Reset
31:15	RESERVED		R	0x00000
14:13	LINE	The output line the address belongs to Valid only if FMTCBL is cleared 0x0: 1st line 0x1: 2nd line 0x3: 4th line 0x2: 3rd line	RW	0x0
12:0	INIT	Initial address value for address pointer 0 This address can not exceed FMTRLEN - 1	RW	0x0000

Table 8-1053. Register Call Summary for Register ISIF_FMTAPTR0

ISS ISP

- ISS ISP ISIF Input Data Formatter: [0] [1]
- ISS ISIF Register Summary: [2]

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Table 8-1054. ISIF_FMTAPTR1

Address Offset	0x0000 0138		
Physical Address	0x5201 1138	**Instance**	ISS_ISIF
Description	Input Data Formatter Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																LINE			INIT												

Bits	Field Name	Description	Type	Reset
31:15	RESERVED		R	0x00000
14:13	LINE	The output line the address belongs to Valid only if FMTCBL is cleared 0x0: 1st line 0x1: 2nd line 0x3: 4th line 0x2: 3rd line	RW	0x0
12:0	INIT	Initial address value for address pointer 1 This address can not exceed FMTRLEN - 1	RW	0x0000

Table 8-1055. Register Call Summary for Register ISIF_FMTAPTR1

ISS ISP

- ISS ISP ISIF Input Data Formatter: [0]
- ISS ISIF Register Summary: [1]

Table 8-1056. ISIF_FMTAPTR2

Address Offset	0x0000 013C		
Physical Address	0x5201 113C	**Instance**	ISS_ISIF
Description	Input Data Formatter Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																LINE			INIT												

Bits	Field Name	Description	Type	Reset
31:15	RESERVED		R	0x00000
14:13	LINE	The output line the address belongs to Valid only if FMTCBL is cleared 0x0: 1st line 0x1: 2nd line 0x3: 4th line 0x2: 3rd line	RW	0x0
12:0	INIT	Initial address value for address pointer 2 This address can not exceed FMTRLEN - 1	RW	0x0000

Table 8-1057. Register Call Summary for Register ISIF_FMTAPTR2

ISS ISP

- ISS ISP ISIF Input Data Formatter: [0]
- ISS ISIF Register Summary: [1]

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Table 8-1058. ISIF_FMTAPTR3

Address Offset	0x0000 0140		
Physical Address	0x5201 1140	**Instance**	ISS_ISIF
Description	Input Data Formatter Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																LINE			INIT												

Bits	Field Name	Description	Type	Reset
31:15	RESERVED		R	0x00000
14:13	LINE	The output line the address belongs to Valid only if FMTCBL is cleared 0x0: 1st line 0x1: 2nd line 0x3: 4th line 0x2: 3rd line	RW	0x0
12:0	INIT	Initial address value for address pointer 3 This address can not exceed FMTRLEN - 1	RW	0x0000

Table 8-1059. Register Call Summary for Register ISIF_FMTAPTR3

ISS ISP

- ISS ISP ISIF Input Data Formatter: [0]
- ISS ISIF Register Summary: [1]

Table 8-1060. ISIF_FMTAPTR4

Address Offset	0x0000 0144		
Physical Address	0x5201 1144	**Instance**	ISS_ISIF
Description	Input Data Formatter Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																LINE			INIT												

Bits	Field Name	Description	Type	Reset
31:15	RESERVED		R	0x00000
14:13	LINE	The output line the address belongs to Valid only if FMTCBL is cleared 0x0: 1st line 0x1: 2nd line 0x3: 4th line 0x2: 3rd line	RW	0x0
12:0	INIT	Initial address value for address pointer 4 This address can not exceed FMTRLEN - 1	RW	0x0000

Table 8-1061. Register Call Summary for Register ISIF_FMTAPTR4

ISS ISP

- ISS ISP ISIF Input Data Formatter: [0]
- ISS ISIF Register Summary: [1]

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Table 8-1062. ISIF_FMTAPTR5

Address Offset	0x0000 0148		
Physical Address	0x5201 1148	**Instance**	ISS_ISIF
Description	Input Data Formatter Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																LINE			INIT												

Bits	Field Name	Description	Type	Reset
31:15	RESERVED		R	0x00000
14:13	LINE	The output line the address belongs to Valid only if FMTCBL is cleared 0x0: 1st line 0x1: 2nd line 0x3: 4th line 0x2: 3rd line	RW	0x0
12:0	INIT	Initial address value for address pointer 5 This address can not exceed FMTRLEN - 1	RW	0x0000

Table 8-1063. Register Call Summary for Register ISIF_FMTAPTR5

ISS ISP

- ISS ISP ISIF Input Data Formatter: [0]
- ISS ISIF Register Summary: [1]

Table 8-1064. ISIF_FMTAPTR6

Address Offset	0x0000 014C		
Physical Address	0x5201 114C	**Instance**	ISS_ISIF
Description	Input Data Formatter Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																LINE			INIT												

Bits	Field Name	Description	Type	Reset
31:15	RESERVED		R	0x00000
14:13	LINE	The output line the address belongs to Valid only if FMTCBL is cleared 0x0: 1st line 0x1: 2nd line 0x3: 4th line 0x2: 3rd line	RW	0x0
12:0	INIT	Initial address value for address pointer 6 This address can not exceed FMTRLEN - 1	RW	0x0000

Table 8-1065. Register Call Summary for Register ISIF_FMTAPTR6

ISS ISP

- ISS ISIF Register Summary: [0]

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Table 8-1066. ISIF_FMTAPTR7

Address Offset	0x0000 0150		
Physical Address	0x5201 1150	**Instance**	ISS_ISIF
Description	Input Data Formatter Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																LINE			INIT												

Bits	Field Name	Description	Type	Reset
31:15	RESERVED		R	0x00000
14:13	LINE	The output line the address belongs to Valid only if FMTCBL is cleared 0x0: 1st line 0x1: 2nd line 0x3: 4th line 0x2: 3rd line	RW	0x0
12:0	INIT	Initial address value for address pointer 7 This address can not exceed FMTRLEN - 1	RW	0x0000

Table 8-1067. Register Call Summary for Register ISIF_FMTAPTR7

ISS ISP

- ISS ISIF Register Summary: [0]

Table 8-1068. ISIF_FMTAPTR8

Address Offset	0x0000 0154		
Physical Address	0x5201 1154	**Instance**	ISS_ISIF
Description	Input Data Formatter Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																LINE			INIT												

Bits	Field Name	Description	Type	Reset
31:15	RESERVED		R	0x00000
14:13	LINE	The output line the address belongs to Valid only if FMTCBL is cleared 0x0: 1st line 0x1: 2nd line 0x3: 4th line 0x2: 3rd line	RW	0x0
12:0	INIT	Initial address value for address pointer 8 This address can not exceed FMTRLEN - 1	RW	0x0000

Table 8-1069. Register Call Summary for Register ISIF_FMTAPTR8

ISS ISP

- ISS ISIF Register Summary: [0]

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Table 8-1070. ISIF_FMTAPTR9

Address Offset	0x0000 0158		
Physical Address	0x5201 1158	**Instance**	ISS_ISIF
Description	Input Data Formatter Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																LINE			INIT												

Bits	Field Name	Description	Type	Reset
31:15	RESERVED		R	0x00000
14:13	LINE	The output line the address belongs to Valid only if FMTCBL is cleared 0x0: 1st line 0x1: 2nd line 0x3: 4th line 0x2: 3rd line	RW	0x0
12:0	INIT	Initial address value for address pointer 9 This address can not exceed FMTRLEN - 1	RW	0x0000

Table 8-1071. Register Call Summary for Register ISIF_FMTAPTR9

ISS ISP

- ISS ISIF Register Summary: [0]

Table 8-1072. ISIF_FMTAPTR10

Address Offset	0x0000 015C		
Physical Address	0x5201 115C	**Instance**	ISS_ISIF
Description	Input Data Formatter Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																LINE			INIT												

Bits	Field Name	Description	Type	Reset
31:15	RESERVED		R	0x00000
14:13	LINE	The output line the address belongs to Valid only if FMTCBL is cleared 0x0: 1st line 0x1: 2nd line 0x3: 4th line 0x2: 3rd line	RW	0x0
12:0	INIT	Initial address value for address pointer 10 This address can not exceed FMTRLEN - 1	RW	0x0000

Table 8-1073. Register Call Summary for Register ISIF_FMTAPTR10

ISS ISP

- ISS ISIF Register Summary: [0]

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Table 8-1074. ISIF_FMTAPTR11

Address Offset	0x0000 0160		
Physical Address	0x5201 1160	**Instance**	ISS_ISIF
Description	Input Data Formatter Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																LINE			INIT												

Bits	Field Name	Description	Type	Reset
31:15	RESERVED		R	0x00000
14:13	LINE	The output line the address belongs to Valid only if FMTCBL is cleared 0x0: 1st line 0x1: 2nd line 0x3: 4th line 0x2: 3rd line	RW	0x0
12:0	INIT	Initial address value for address pointer 11 This address can not exceed FMTRLEN - 1	RW	0x0000

Table 8-1075. Register Call Summary for Register ISIF_FMTAPTR11

ISS ISP

- ISS ISIF Register Summary: [0]

Table 8-1076. ISIF_FMTAPTR12

Address Offset	0x0000 0164		
Physical Address	0x5201 1164	**Instance**	ISS_ISIF
Description	Input Data Formatter Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																LINE			INIT												

Bits	Field Name	Description	Type	Reset
31:15	RESERVED		R	0x00000
14:13	LINE	The output line the address belongs to Valid only if FMTCBL is cleared 0x0: 1st line 0x1: 2nd line 0x3: 4th line 0x2: 3rd line	RW	0x0
12:0	INIT	Initial address value for address pointer 12 This address can not exceed FMTRLEN - 1	RW	0x0000

Table 8-1077. Register Call Summary for Register ISIF_FMTAPTR12

ISS ISP

- ISS ISIF Register Summary: [0]

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Table 8-1078. ISIF_FMTAPTR13

Address Offset	0x0000 0168		
Physical Address	0x5201 1168	**Instance**	ISS_ISIF
Description	Input Data Formatter Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																LINE			INIT												

Bits	Field Name	Description	Type	Reset
31:15	RESERVED		R	0x00000
14:13	LINE	The output line the address belongs to Valid only if FMTCBL is cleared 0x0: 1st line 0x1: 2nd line 0x3: 4th line 0x2: 3rd line	RW	0x0
12:0	INIT	Initial address value for address pointer 13 This address can not exceed FMTRLEN - 1	RW	0x0000

Table 8-1079. Register Call Summary for Register ISIF_FMTAPTR13

ISS ISP

- ISS ISIF Register Summary: [0]

Table 8-1080. ISIF_FMTAPTR14

Address Offset	0x0000 016C		
Physical Address	0x5201 116C	**Instance**	ISS_ISIF
Description	Input Data Formatter Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																LINE			INIT												

Bits	Field Name	Description	Type	Reset
31:15	RESERVED		R	0x00000
14:13	LINE	The output line the address belongs to Valid only if FMTCBL is cleared 0x0: 1st line 0x1: 2nd line 0x3: 4th line 0x2: 3rd line	RW	0x0
12:0	INIT	Initial address value for address pointer 14 This address can not exceed FMTRLEN - 1	RW	0x0000

Table 8-1081. Register Call Summary for Register ISIF_FMTAPTR14

ISS ISP

- ISS ISIF Register Summary: [0]

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Table 8-1082. ISIF_FMTAPTR15

Address Offset	0x0000 0170		
Physical Address	0x5201 1170	**Instance**	ISS_ISIF
Description	Input Data Formatter Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																LINE								INIT							

Bits	Field Name	Description	Type	Reset
31:15	RESERVED		R	0x00000
14:13	LINE	The output line the address belongs to Valid only if FMTCBL is cleared 0x0: 1st line 0x1: 2nd line 0x3: 4th line 0x2: 3rd line	RW	0x0
12:0	INIT	Initial address value for address pointer 15 This address can not exceed FMTRLEN - 1	RW	0x0000

Table 8-1083. Register Call Summary for Register ISIF_FMTAPTR15

ISS ISP

- ISS ISP ISIF Input Data Formatter: [0]
- ISS ISIF Register Summary: [1]

Table 8-1084. ISIF_FMTPGMVF0

Address Offset	0x0000 0174		
Physical Address	0x5201 1174	**Instance**	ISS_ISIF
Description	Input Data Formatter Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PGM15EN	PGM14EN	PGM13EN	PGM12EN	PGM11EN	PGM10EN	PGM09EN	PGM08EN	PGM07EN	PGM06EN	PGM05EN	PGM04EN	PGM03EN	PGM02EN	PGM01EN	PGM00EN

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15	PGM15EN	Program 15 Valid Flag 0x0: Skip this pixel 0x1: This pixel is valid	RW	0
14	PGM14EN	Program 14 Valid Flag 0x0: Skip this pixel 0x1: This pixel is valid	RW	0
13	PGM13EN	Program 13 Valid Flag 0x0: Skip this pixel 0x1: This pixel is valid	RW	0

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Bits	Field Name	Description	Type	Reset
12	PGM12EN	Program 12 Valid Flag 0x0: Skip this pixel 0x1: This pixel is valid	RW	0
11	PGM11EN	Program 11 Valid Flag 0x0: Skip this pixel 0x1: This pixel is valid	RW	0
10	PGM10EN	Program 10 Valid Flag 0x0: Skip this pixel 0x1: This pixel is valid	RW	0
9	PGM09EN	Program 9 Valid Flag 0x0: Skip this pixel 0x1: This pixel is valid	RW	0
8	PGM08EN	Program 8 Valid Flag 0x0: Skip this pixel 0x1: This pixel is valid	RW	0
7	PGM07EN	Program 7 Valid Flag 0x0: Skip this pixel 0x1: This pixel is valid	RW	0
6	PGM06EN	Program 6 Valid Flag 0x0: Skip this pixel 0x1: This pixel is valid	RW	0
5	PGM05EN	Program 5 Valid Flag 0x0: Skip this pixel 0x1: This pixel is valid	RW	0
4	PGM04EN	Program 4 Valid Flag 0x0: Skip this pixel 0x1: This pixel is valid	RW	0
3	PGM03EN	Program 3 Valid Flag 0x0: Skip this pixel 0x1: This pixel is valid	RW	0
2	PGM02EN	Program 2 Valid Flag 0x0: Skip this pixel 0x1: This pixel is valid	RW	0
1	PGM01EN	Program 1 Valid Flag 0x0: Skip this pixel 0x1: This pixel is valid	RW	0
0	PGM00EN	Program 0 Valid Flag 0x0: Skip this pixel 0x1: This pixel is valid	RW	0

Table 8-1085. Register Call Summary for Register ISIF_FMTPGMVF0

ISS ISP

- ISS ISP ISIF Input Data Formatter: [0] [1] [2] [3] [4]
- ISS ISP ISIF Hardware Setup/Initialization: [5]
- ISS ISIF Register Summary: [6]

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Table 8-1086. ISIF_FMTPGMVF1

Address Offset	0x0000 0178		
Physical Address	0x5201 1178	**Instance**	ISS_ISIF
Description	Input Data Formatter Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PGM31EN	PGM30EN	PGM29EN	PGM28EN	PGM27EN	PGM26EN	PGM25EN	PGM24EN	PGM23EN	PGM22EN	PGM21EN	PGM20EN	PGM19EN	PGM18EN	PGM17EN	PGM16EN

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15	PGM31EN	Program 31 Valid Flag 0x0: Skip this pixel 0x1: This pixel is valid	RW	0
14	PGM30EN	Program 30 Valid Flag 0x0: Skip this pixel 0x1: This pixel is valid	RW	0
13	PGM29EN	Program 29 Valid Flag 0x0: Skip this pixel 0x1: This pixel is valid	RW	0
12	PGM28EN	Program 28 Valid Flag 0x0: Skip this pixel 0x1: This pixel is valid	RW	0
11	PGM27EN	Program 27 Valid Flag 0x0: Skip this pixel 0x1: This pixel is valid	RW	0
10	PGM26EN	Program 26 Valid Flag 0x0: Skip this pixel 0x1: This pixel is valid	RW	0
9	PGM25EN	Program 25 Valid Flag 0x0: Skip this pixel 0x1: This pixel is valid	RW	0
8	PGM24EN	Program 24 Valid Flag 0x0: Skip this pixel 0x1: This pixel is valid	RW	0
7	PGM23EN	Program 23 Valid Flag 0x0: Skip this pixel 0x1: This pixel is valid	RW	0
6	PGM22EN	Program 22 Valid Flag 0x0: Skip this pixel 0x1: This pixel is valid	RW	0
5	PGM21EN	Program 21 Valid Flag 0x0: Skip this pixel 0x1: This pixel is valid	RW	0
4	PGM20EN	Program 20 Valid Flag 0x0: Skip this pixel 0x1: This pixel is valid	RW	0

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Bits	Field Name	Description	Type	Reset
3	PGM19EN	Program 19 Valid Flag 0x0: Skip this pixel 0x1: This pixel is valid	RW	0
2	PGM18EN	Program 18 Valid Flag 0x0: Skip this pixel 0x1: This pixel is valid	RW	0
1	PGM17EN	Program 17 Valid Flag 0x0: Skip this pixel 0x1: This pixel is valid	RW	0
0	PGM16EN	Program 16 Valid Flag 0x0: Skip this pixel 0x1: This pixel is valid	RW	0

Table 8-1087. Register Call Summary for Register ISIF_FMTPGMVF1

ISS ISP

- ISS ISP ISIF Input Data Formatter: [0] [1] [2]
- ISS ISP ISIF Hardware Setup/Initialization: [3]
- ISS ISIF Register Summary: [4]

Table 8-1088. ISIF_FMTPGMAPU0

Address Offset	0x0000 017C		
Physical Address	0x5201 117C	**Instance**	ISS_ISIF
Description	Input Data Formatter Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PGM15UPDT	PGM14UPDT	PGM13UPDT	PGM12UPDT	PGM11UPDT	PGM10UPDT	PGM9UPDT	PGM8UPDT	PGM7UPDT	PGM6UPDT	PGM5UPDT	PGM4UPDT	PGM3UPDT	PGM2UPDT	PGM1UPDT	PGM0UPDT

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15	PGM15UPDT	Program 15 Address Pointer Update 0x0: APTR* + N (Auto increment) 0x1: APTR* - N (Auto decrement)	RW	0
14	PGM14UPDT	Program 14 Address Pointer Update 0x0: APTR* + N (Auto increment) 0x1: APTR* - N (Auto decrement)	RW	0
13	PGM13UPDT	Program 13 Address Pointer Update 0x0: APTR* + N (Auto increment) 0x1: APTR* - N (Auto decrement)	RW	0
12	PGM12UPDT	Program 12 Address Pointer Update 0x0: APTR* + N (Auto increment) 0x1: APTR* - N (Auto decrement)	RW	0
11	PGM11UPDT	Program 11 Address Pointer Update 0x0: APTR* + N (Auto increment) 0x1: APTR* - N (Auto decrement)	RW	0

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Bits	Field Name	Description	Type	Reset
10	PGM10UPDT	Program 10 Address Pointer Update 0x0: APTR* + N (Auto increment) 0x1: APTR* - N (Auto decrement)	RW	0
9	PGM9UPDT	Program 9 Address Pointer Update 0x0: APTR* + N (Auto increment) 0x1: APTR* - N (Auto decrement)	RW	0
8	PGM8UPDT	Program 8 Address Pointer Update 0x0: APTR* + N (Auto increment) 0x1: APTR* - N (Auto decrement)	RW	0
7	PGM7UPDT	Program 7 Address Pointer Update 0x0: APTR* + N (Auto increment) 0x1: APTR* - N (Auto decrement)	RW	0
6	PGM6UPDT	Program 6 Address Pointer Update 0x0: APTR* + N (Auto increment) 0x1: APTR* - N (Auto decrement)	RW	0
5	PGM5UPDT	Program 5 Address Pointer Update 0x0: APTR* + N (Auto increment) 0x1: APTR* - N (Auto decrement)	RW	0
4	PGM4UPDT	Program 4 Address Pointer Update 0x0: APTR* + N (Auto increment) 0x1: APTR* - N (Auto decrement)	RW	0
3	PGM3UPDT	Program 3 Address Pointer Update 0x0: APTR* + N (Auto increment) 0x1: APTR* - N (Auto decrement)	RW	0
2	PGM2UPDT	Program 2 Address Pointer Update 0x0: APTR* + N (Auto increment) 0x1: APTR* - N (Auto decrement)	RW	0
1	PGM1UPDT	Program 1 Address Pointer Update 0x0: APTR* + N (Auto increment) 0x1: APTR* - N (Auto decrement)	RW	0
0	PGM0UPDT	Program 0 Address Pointer Update 0x0: APTR* + N (Auto increment) 0x1: APTR* - N (Auto decrement)	RW	0

Table 8-1089. Register Call Summary for Register ISIF_FMTPGMAPU0

ISS ISP

- ISS ISP ISIF Input Data Formatter: [0] [1] [2] [3] [4]
- ISS ISP ISIF Hardware Setup/Initialization: [5]
- ISS ISIF Register Summary: [6]

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Table 8-1090. ISIF_FMTPGMAPU1

Address Offset	0x0000 0180		
Physical Address	0x5201 1180	**Instance**	ISS_ISIF
Description	Input Data Formatter Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PGM31UPDT	PGM30UPDT	PGM29UPDT	PGM28UPDT	PGM27UPDT	PGM26UPDT	PGM25UPDT	PGM24UPDT	PGM23UPDT	PGM22UPDT	PGM21UPDT	PGM20UPDT	PGM19UPDT	PGM18UPDT	PGM17UPDT	PGM16UPDT

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15	PGM31UPDT	Program 31 Address Pointer Update 0x0: APTR* + N (Auto increment) 0x1: APTR* - N (Auto decrement)	RW	0
14	PGM30UPDT	Program 30 Address Pointer Update 0x0: APTR* + N (Auto increment) 0x1: APTR* - N (Auto decrement)	RW	0
13	PGM29UPDT	Program 29 Address Pointer Update 0x0: APTR* + N (Auto increment) 0x1: APTR* - N (Auto decrement)	RW	0
12	PGM28UPDT	Program 28 Address Pointer Update 0x0: APTR* + N (Auto increment) 0x1: APTR* - N (Auto decrement)	RW	0
11	PGM27UPDT	Program 27 Address Pointer Update 0x0: APTR* + N (Auto increment) 0x1: APTR* - N (Auto decrement)	RW	0
10	PGM26UPDT	Program 26 Address Pointer Update 0x0: APTR* + N (Auto increment) 0x1: APTR* - N (Auto decrement)	RW	0
9	PGM25UPDT	Program 25 Address Pointer Update 0x0: APTR* + N (Auto increment) 0x1: APTR* - N (Auto decrement)	RW	0
8	PGM24UPDT	Program 24 Address Pointer Update 0x0: APTR* + N (Auto increment) 0x1: APTR* - N (Auto decrement)	RW	0
7	PGM23UPDT	Program 23 Address Pointer Update 0x0: APTR* + N (Auto increment) 0x1: APTR* - N (Auto decrement)	RW	0
6	PGM22UPDT	Program 22 Address Pointer Update 0x0: APTR* + N (Auto increment) 0x1: APTR* - N (Auto decrement)	RW	0
5	PGM21UPDT	Program 21 Address Pointer Update 0x0: APTR* + N (Auto increment) 0x1: APTR* - N (Auto decrement)	RW	0

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Bits	Field Name	Description	Type	Reset
4	PGM20UPDT	Program 20 Address Pointer Update 0x0: APTR* + N (Auto increment) 0x1: APTR* - N (Auto decrement)	RW	0
3	PGM19UPDT	Program 19 Address Pointer Update 0x0: APTR* + N (Auto increment) 0x1: APTR* - N (Auto decrement)	RW	0
2	PGM18UPDT	Program 18 Address Pointer Update 0x0: APTR* + N (Auto increment) 0x1: APTR* - N (Auto decrement)	RW	0
1	PGM17UPDT	Program 17 Address Pointer Update 0x0: APTR* + N (Auto increment) 0x1: APTR* - N (Auto decrement)	RW	0
0	PGM16UPDT	Program 16 Address Pointer Update 0x0: APTR* + N (Auto increment) 0x1: APTR* - N (Auto decrement)	RW	0

Table 8-1091. Register Call Summary for Register ISIF_FMTPGMAPU1

ISS ISP
- ISS ISP ISIF Input Data Formatter: [0] [1] [2]
- ISS ISP ISIF Hardware Setup/Initialization: [3]
- ISS ISIF Register Summary: [4]

Table 8-1092. ISIF_FMTPGMAPS0

Address Offset	0x0000 0184		
Physical Address	0x5201 1184	**Instance**	ISS_ISIF
Description	Input Data Formatter Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PGM3APTR				PGM2APTR				PGM1APTR				PGM0APTR			

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	PGM3APTR	Program 3 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)	RW	0x0
11:8	PGM2APTR	Program 2 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)	RW	0x0
7:4	PGM1APTR	Program 1 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)	RW	0x0
3:0	PGM0APTR	Program 0 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)	RW	0x0

Table 8-1093. Register Call Summary for Register ISIF_FMTPGMAPS0

ISS ISP
- ISS ISP ISIF Input Data Formatter: [0] [1] [2]
- ISS ISP ISIF Hardware Setup/Initialization: [3]
- ISS ISIF Register Summary: [4]

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Table 8-1094. ISIF_FMTPGMAPS1

Address Offset	0x0000 0188		
Physical Address	0x5201 1188	**Instance**	ISS_ISIF
Description	Input Data Formatter Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PGM7APTR				PGM6APTR				PGM5APTR				PGM4APTR			

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	PGM7APTR	Program 7 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)	RW	0x0
11:8	PGM6APTR	Program 6 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)	RW	0x0
7:4	PGM5APTR	Program 5 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)	RW	0x0
3:0	PGM4APTR	Program 0 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)	RW	0x0

Table 8-1095. Register Call Summary for Register ISIF_FMTPGMAPS1

ISS ISP

- ISS ISP ISIF Hardware Setup/Initialization: [0]
- ISS ISIF Register Summary: [1]

Table 8-1096. ISIF_FMTPGMAPS2

Address Offset	0x0000 018C		
Physical Address	0x5201 118C	**Instance**	ISS_ISIF
Description	Input Data Formatter Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PGM11APTR				PGM10APTR				PGM9APTR				PGM8APTR			

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	PGM11APTR	Program 11 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)	RW	0x0
11:8	PGM10APTR	Program 10 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)	RW	0x0
7:4	PGM9APTR	Program 9 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)	RW	0x0
3:0	PGM8APTR	Program 8 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)	RW	0x0

Table 8-1097. Register Call Summary for Register ISIF_FMTPGMAPS2

ISS ISP

- ISS ISP ISIF Input Data Formatter: [0] [1]
- ISS ISP ISIF Hardware Setup/Initialization: [2]
- ISS ISIF Register Summary: [3]

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Table 8-1098. ISIF_FMTPGMAPS3

Address Offset	0x0000 0190		
Physical Address	0x5201 1190	**Instance**	ISS_ISIF
Description	Input Data Formatter Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PGM15APTR				PGM14APTR				PGM13APTR				PGM12APTR			

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	PGM15APTR	Program 15 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)	RW	0x0
11:8	PGM14APTR	Program 14 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)	RW	0x0
7:4	PGM13APTR	Program 13 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)	RW	0x0
3:0	PGM12APTR	Program 12 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)	RW	0x0

Table 8-1099. Register Call Summary for Register ISIF_FMTPGMAPS3

ISS ISP

- ISS ISP ISIF Hardware Setup/Initialization: [0]
- ISS ISIF Register Summary: [1]

Table 8-1100. ISIF_FMTPGMAPS4

Address Offset	0x0000 0194		
Physical Address	0x5201 1194	**Instance**	ISS_ISIF
Description	Input Data Formatter Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PGM19APTR				PGM18APTR				PGM17APTR				PGM16APTR			

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	PGM19APTR	Program 19 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)	RW	0x0
11:8	PGM18APTR	Program 18 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)	RW	0x0
7:4	PGM17APTR	Program 17 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)	RW	0x0
3:0	PGM16APTR	Program 16 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)	RW	0x0

Table 8-1101. Register Call Summary for Register ISIF_FMTPGMAPS4

ISS ISP

- ISS ISP ISIF Input Data Formatter: [0] [1]
- ISS ISP ISIF Hardware Setup/Initialization: [2]
- ISS ISIF Register Summary: [3]

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Table 8-1102. ISIF_FMTPGMAPS5

Address Offset	0x0000 0198		
Physical Address	0x5201 1198	**Instance**	ISS_ISIF
Description	Input Data Formatter Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PGM23APTR				PGM22APTR				PGM21APTR				PGM20APTR			

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	PGM23APTR	Program 23 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)	RW	0x0
11:8	PGM22APTR	Program 22 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)	RW	0x0
7:4	PGM21APTR	Program 21 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)	RW	0x0
3:0	PGM20APTR	Program 20 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)	RW	0x0

Table 8-1103. Register Call Summary for Register ISIF_FMTPGMAPS5

ISS ISP

- ISS ISP ISIF Hardware Setup/Initialization: [0]
- ISS ISIF Register Summary: [1]

Table 8-1104. ISIF_FMTPGMAPS6

Address Offset	0x0000 019C		
Physical Address	0x5201 119C	**Instance**	ISS_ISIF
Description	Input Data Formatter Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PGM27APTR				PGM26APTR				PGM25APTR				PGM24APTR			

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	PGM27APTR	Program 27 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)	RW	0x0
11:8	PGM26APTR	Program 26 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)	RW	0x0
7:4	PGM25APTR	Program 25 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)	RW	0x0
3:0	PGM24APTR	Program 24 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)	RW	0x0

Table 8-1105. Register Call Summary for Register ISIF_FMTPGMAPS6

ISS ISP

- ISS ISP ISIF Hardware Setup/Initialization: [0]
- ISS ISIF Register Summary: [1]

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Table 8-1106. ISIF_FMTPGMAPS7

Address Offset	0x0000 01A0		
Physical Address	0x5201 11A0	**Instance**	ISS_ISIF
Description	Input Data Formatter Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PGM31APTR				PGM30APTR				PGM29APTR				PGM28APTR			

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	PGM31APTR	Program 31 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)	RW	0x0
11:8	PGM30APTR	Program 30 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)	RW	0x0
7:4	PGM29APTR	Program 29 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)	RW	0x0
3:0	PGM28APTR	Program 28 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)	RW	0x0

Table 8-1107. Register Call Summary for Register ISIF_FMTPGMAPS7

ISS ISP

- ISS ISP ISIF Input Data Formatter: [0]
- ISS ISP ISIF Hardware Setup/Initialization: [1]
- ISS ISIF Register Summary: [2]

Table 8-1108. ISIF_CSCCTL

Address Offset	0x0000 01A4		
Physical Address	0x5201 11A4	**Instance**	ISS_ISIF
Description	Color Space Converter Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED															CSCEN

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:1	RESERVED		R	0x0000
0	CSCEN	Controls ON/OFF of Color Space converter. 0x0: Disable 0x1: Enable	RW	0

Table 8-1109. Register Call Summary for Register ISIF_CSCCTL

ISS ISP

- ISS ISP ISIF Color Space Converter: [0]
- ISS ISP ISIF Hardware Setup/Initialization: [1]
- ISS ISIF Register Summary: [2]

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Table 8-1110. ISIF_CSCM0

Address Offset	0x0000 01A8		
Physical Address	0x5201 11A8	**Instance**	ISS_ISIF
Description	Color Space Converter Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																CSCM01								CSCM00							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:8	CSCM01	Color Space convert coefficient value M01: This value is signed 8-bit with the 5-bits decimal.	RW	0x00
7:0	CSCM00	Color Space convert coefficient value M00: This value is signed 8-bit with the 5-bits decimal.	RW	0x00

Table 8-1111. Register Call Summary for Register ISIF_CSCM0

ISS ISP

- ISS ISP ISIF Color Space Converter: [0] [1]
- ISS ISP ISIF Hardware Setup/Initialization: [2]
- ISS ISIF Register Summary: [3]

Table 8-1112. ISIF_CSCM1

Address Offset	0x0000 01AC		
Physical Address	0x5201 11AC	**Instance**	ISS_ISIF
Description	Color Space Converter Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																CSCM03								CSCM02							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:8	CSCM03	Color Space convert coefficient value M03: This value is signed 8-bit with the 5-bits decimal.	RW	0x00
7:0	CSCM02	Color Space convert coefficient value M02: This value is signed 8-bit with the 5-bits decimal.	RW	0x00

Table 8-1113. Register Call Summary for Register ISIF_CSCM1

ISS ISP

- ISS ISP ISIF Color Space Converter: [0] [1]
- ISS ISP ISIF Hardware Setup/Initialization: [2]
- ISS ISIF Register Summary: [3]

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Table 8-1114. ISIF_CSCM2

Address Offset	0x0000 01B0		
Physical Address	0x5201 11B0	**Instance**	ISS_ISIF
Description	Color Space Converter Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																CSCM11								CSCM10							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:8	CSCM11	Color Space convert coefficient value M11: This value is signed 8-bit with the 5-bits decimal.	RW	0x00
7:0	CSCM10	Color Space convert coefficient value M10: This value is signed 8-bit with the 5-bits decimal.	RW	0x00

Table 8-1115. Register Call Summary for Register ISIF_CSCM2

ISS ISP

- ISS ISP ISIF Color Space Converter: [0] [1]
- ISS ISP ISIF Hardware Setup/Initialization: [2]
- ISS ISIF Register Summary: [3]

Table 8-1116. ISIF_CSCM3

Address Offset	0x0000 01B4		
Physical Address	0x5201 11B4	**Instance**	ISS_ISIF
Description	Color Space Converter Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																CSCM13								CSCM12							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:8	CSCM13	Color Space convert coefficient value M13: This value is signed 8-bit with the 5-bits decimal.	RW	0x00
7:0	CSCM12	Color Space convert coefficient value M12: This value is signed 8-bit with the 5-bits decimal.	RW	0x00

Table 8-1117. Register Call Summary for Register ISIF_CSCM3

ISS ISP

- ISS ISP ISIF Color Space Converter: [0] [1]
- ISS ISP ISIF Hardware Setup/Initialization: [2]
- ISS ISIF Register Summary: [3]

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Table 8-1118. ISIF_CSCM4

Address Offset	0x0000 01B8		
Physical Address	0x5201 11B8	**Instance**	ISS_ISIF
Description	Color Space Converter Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																CSCM21								CSCM20							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:8	CSCM21	Color Space convert coefficient value M21: This value is signed 8-bit with the 5-bits decimal.	RW	0x00
7:0	CSCM20	Color Space convert coefficient value M20: This value is signed 8-bit with the 5-bits decimal.	RW	0x00

Table 8-1119. Register Call Summary for Register ISIF_CSCM4

ISS ISP

- ISS ISP ISIF Color Space Converter: [0] [1]
- ISS ISP ISIF Hardware Setup/Initialization: [2]
- ISS ISIF Register Summary: [3]

Table 8-1120. ISIF_CSCM5

Address Offset	0x0000 01BC		
Physical Address	0x5201 11BC	**Instance**	ISS_ISIF
Description	Color Space Converter Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																CSCM23								CSCM22							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:8	CSCM23	Color Space convert coefficient value M23: This value is signed 8-bit with the 5-bits decimal.	RW	0x00
7:0	CSCM22	Color Space convert coefficient value M22: This value is signed 8-bit with the 5-bits decimal.	RW	0x00

Table 8-1121. Register Call Summary for Register ISIF_CSCM5

ISS ISP

- ISS ISP ISIF Color Space Converter: [0] [1]
- ISS ISP ISIF Hardware Setup/Initialization: [2]
- ISS ISIF Register Summary: [3]

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Table 8-1122. ISIF_CSCM6

Address Offset	0x0000 01C0		
Physical Address	0x5201 11C0	**Instance**	ISS_ISIF
Description	Color Space Converter Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																CSCM31								CSCM30							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:8	CSCM31	Color Space convert coefficient value M31: This value is signed 8-bit with the 5-bits decimal.	RW	0x00
7:0	CSCM30	Color Space convert coefficient value M30: This value is signed 8-bit with the 5-bits decimal.	RW	0x00

Table 8-1123. Register Call Summary for Register ISIF_CSCM6

ISS ISP

- ISS ISP ISIF Color Space Converter: [0] [1]
- ISS ISP ISIF Hardware Setup/Initialization: [2]
- ISS ISIF Register Summary: [3]

Table 8-1124. ISIF_CSCM7

Address Offset	0x0000 01C4		
Physical Address	0x5201 11C4	**Instance**	ISS_ISIF
Description	Color Space Converter Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																CSCM33								CSCM32							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:8	CSCM33	Color Space convert coefficient value M33: This value is signed 8-bit with the 5-bits decimal.	RW	0x00
7:0	CSCM32	Color Space convert coefficient value M32: This value is signed 8-bit with the 5-bits decimal.	RW	0x00

Table 8-1125. Register Call Summary for Register ISIF_CSCM7

ISS ISP

- ISS ISP ISIF Color Space Converter: [0] [1]
- ISS ISP ISIF Hardware Setup/Initialization: [2]
- ISS ISIF Register Summary: [3]

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Table 8-1126. ISIF_CLKCTL

Address Offset	0x0000 01F8		
Physical Address	0x5201 11F8	**Instance**	ISS_ISIF
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED														CLKEN1	CLKEN2

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:2	RESERVED		R	0x0000
1	CLKEN1	Forces isif_clken1 to be active. (Test mode) 0x0: normal mode 0x1: force isif_clken1 to be active	RW	0
0	CLKEN2	Forces isif_clken2 to be active. (Test mode) 0x0: normal mode 0x1: force isif_clken2 to be active	RW	0

Table 8-1127. Register Call Summary for Register ISIF_CLKCTL

ISS ISP
- ISS ISIF Register Summary: [0]

8.3.5.7 ISS IPIPEIF Registers

8.3.5.7.1 ISS IPIPEIF Register Summary

Table 8-1128. ISS IPIPEIF Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	ISS_IPIPEIF Base Address
IPIPEIF_ENABLE	RW	32	0x0000 0000	0x5201 1200
IPIPEIF_CFG1	RW	32	0x0000 0004	0x5201 1204
IPIPEIF_PPLN	RW	32	0x0000 0008	0x5201 1208
IPIPEIF_LPFR	RW	32	0x0000 000C	0x5201 120C
IPIPEIF_HNUM	RW	32	0x0000 0010	0x5201 1210
IPIPEIF_VNUM	RW	32	0x0000 0014	0x5201 1214
IPIPEIF_ADDRU	RW	32	0x0000 0018	0x5201 1218
IPIPEIF_ADDRL	RW	32	0x0000 001C	0x5201 121C
IPIPEIF_ADOFS	RW	32	0x0000 0020	0x5201 1220
IPIPEIF_RSZ	RW	32	0x0000 0024	0x5201 1224
IPIPEIF_GAIN	RW	32	0x0000 0028	0x5201 1228
IPIPEIF_DPCM	RW	32	0x0000 002C	0x5201 122C
IPIPEIF_CFG2	RW	32	0x0000 0030	0x5201 1230
IPIPEIF_INIRSZ	RW	32	0x0000 0034	0x5201 1234
IPIPEIF_OCLIP	RW	32	0x0000 0038	0x5201 1238
IPIPEIF_DTUDF	RW	32	0x0000 003C	0x5201 123C
IPIPEIF_CLKDIV	RW	32	0x0000 0040	0x5201 1240

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Table 8-1128. ISS IPIPEIF Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	ISS_IPIPEIF Base Address
IPIPEIF_DPC1	RW	32	0x0000 0044	0x5201 1244
IPIPEIF_DPC2	RW	32	0x0000 0048	0x5201 1248
IPIPEIF_RSZ3A	RW	32	0x0000 0054	0x5201 1254
IPIPEIF_INIRSZ3A	RW	32	0x0000 0058	0x5201 1258

8.3.5.7.2 ISS IPIPEIF Register Description

Table 8-1129. IPIPEIF_ENABLE

Address Offset	0x0000 0000		
Physical Address	0x5201 1200	**Instance**	ISS_IPIPEIF
Description	IPIPEIF Enable.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														SYNCOFF	ENABLE

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	SYNCOFF	VD output mask This register masks the VD output to the IPIPE module. This can be useful when one wants to read data from SDRAM which are stored in a double buffer. If the VD is not masked each time we start the module an new VD will be generated to the IPIPEIF module. Let's consider two buffers A and B of N lines each. *This bit field is latched by VD. 0x0: VD output mask is disabled. 0x1: VD output mask is enabled.	RW	0
0	ENABLE	IPIPE I/F Enable This register is used to start the operation of SDRAM buffer memory read and generates SYNC signals. This register is available when INPSRC1 or INPSCR2 = 1, 2 or 3. 0x0: disable 0x1: enable	RW	0

Table 8-1130. Register Call Summary for Register IPIPEIF_ENABLE

ISS ISP

- ISS ISP IPIPEIF Input Interface: [0]
- ISS ISP IPIPEIF Timing Generation: [1]
- ISS ISP IPIPEIF Hardware Setup/Initialization: [2]
- ISS ISP IPIPEIF Enable/Disable Hardware: [3] [4] [5] [6]
- ISS ISP IPIPEIF Register Accessibility During Frame Processing: [7] [8] [9]
- ISS IPIPEIF Register Summary: [10]

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Table 8-1131. IPIPEIF_CFG1

Address Offset	0x0000 0004		
Physical Address	0x5201 1204	**Instance**	ISS_IPIPEIF
Description	IPIPEIF Configuration #1		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																INPSRC1		DATASFT			CLKSEL	UNPACK		AVGFILT	RESERVED			INPSRC2		DECIM	ONESHOT

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:14	INPSRC1	Selects the source for the mux (VPORT / ISIF / SDRAM) as well as the data format type. 0x0: VPORT_RAW 0x1: SDRAM_RAW 0x3: SDRAM_YUV 0x2: ISIF_DARKFM Input ports to DFS submodule are ISIF and SDRAM.	RW	0x0
13:11	DATASFT	SDRAM read data shift This register is available when INPSRC1 or INPSRC2 = 1 or 2, that is, when data are read from SDRAM. 0x6: Output data[11:0] = (read data[15:4] 4) 0x0FFF 0x1: Output data[11:0] = (read data[11:0] 1) 0x0FFF 0x7: Output data[11:0] = (read data[15:4] 4) 0x0FFF 0x0: Output data[11:0] = (read data[11:0]) 0x0FFF 0x2: Output data[11:0] = (read data[11:0] 2) 0x0FFF 0x4: Output data[11:0] = (read data[11:0] 4) 0x0FFF 0x5: Output data[11:0] = (read data[15:4] 4) 0x0FFF 0x3: Output data[11:0] = (read data[11:0] 3) 0x0FFF	RW	0x0
10	CLKSEL	IPIPEIF IPIPE module pixel clock selection. This register must be set to 1 when INPSRC1 or INPSRC2 = 1 or 3, that is, data are solely read from SDRAM (VPORT inactive). 0x0: Selects the pixel clock from the VPORT. 0x1: Selects the pixel clock from the fractional clock divider. The fractional clock divider value is setup with the IPIPEIF_CLKDIV register.	RW	0
9:8	UNPACK	8-Bit, 12-bit Packed Mode When sensor raw data are stored in 8-bit packed mode or 12-bit packed mode, this register should code 1 or 3. This register is effective when INPSRC = 1 or 2. 0x0: 16 bits / pixel 0x1: 8 bits / pixel 0x3: 12 bits / pixel 0x2: 8 bits / pixel + inverse A law (8 bits to 10 bits)	RW	0x0
7	AVGFILT	Averaging Filter It applies (1,2,1) filter for the RGB/YCbCr data. *This bit field is latched by VD. 0x0: disable 0x1: enable	RW	0

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Bits	Field Name	Description	Type	Reset
6:4	RESERVED		R	0x0
3:2	INPSRC2	Selects the source for the mux (ISIF / SDRAM) as well as the data format type. 0x0: ISIF 0x1: SDRAM_RAW 0x3: SDRAM_YUV 0x2: ISIF_DARKFM Input ports to DFS submodule are VPORT and SDRAM.	RW	0x0
1	DECIM	Pixel Decimation The decimation rate defined by RSZ register. *This bit field is latched by VD. 0x0: No decimation 0x1: Decimation	RW	0
0	ONESHOT	One Shot Mode This register is available when INPSRC = 1 or 3. 0x0: Continuous mode 0x1: One shot mode	RW	0

Table 8-1132. Register Call Summary for Register IPIPEIF_CFG1

ISS ISP

- ISS ISP IPIPEIF Data Path Selection: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17]
- ISS ISP IPIPEIF Timing Generation: [18] [19] [20] [21] [22] [23] [24] [25] [26] [27] [28]
- ISS ISP IPIPEIF Decompression (DCPM) Subblock: Unpack and Decompression Function: [29] [30] [31] [32] [33] [34] [35] [36] [37] [38] [39] [40] [41]
- ISS ISP IPIPEIF Dark-Frame Subtraction Functionality: [42] [43] [44] [45] [46]
- ISS ISP IPIPEIF (1, 2, 1) Averaging Filter for IPIPE Data Path: [47] [48] [49] [50] [51]
- ISS ISP IPIPEIF Horizontal Pixel Decimator (Downsizer) for IPIPE Data Path: [52]
- ISS ISP IPIPEIF YUV4:2:2 8-bits Packed Data Input Coming From ISIF Module: [53]
- ISS ISP IPIPEIF YUV4:2:0 Data Input for Memory-to-Memory Resize Operations: [54] [55] [56] [57] [58] [59] [60] [61]
- ISS ISP IPIPEIF Hardware Setup/Initialization: [62] [63] [64] [65] [66] [67] [68] [69] [70]
- ISS ISP IPIPEIF Enable/Disable Hardware: [71] [72] [73] [74] [75]
- ISS ISP IPIPEIF Register Accessibility During Frame Processing: [76] [77]
- ISS ISP IPIPEIF Summary of Constraints: [78] [79]
- ISS IPIPEIF Register Summary: [80]
- ISS IPIPEIF Register Description: [81] [82] [83] [84]

Table 8-1133. IPIPEIF_PPLN

Address Offset	0x0000 0008		
Physical Address	0x5201 1208	**Instance**	ISS_IPIPEIF
Description	IPIPEIF Interval of HD / Start pixel in HD		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								PPLN							

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Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12:0	PPLN	Case-1: Interval of Horizontal Sync (HD) Specifies the interval of horizontal sync. This register is available when INPSRC = 1 or 3. Case-2: Start Pixel in Horizontal Sync (HD) Specifies the start pixel in horizontal sync. This register is available when INPSRC = 2 *This bit field is latched by VD.	RW	0x0000

Table 8-1134. Register Call Summary for Register IPIPEIF_PPLN

ISS ISP

- ISS ISP IPIPEIF Input Interface: [0] [1] [2] [3]
- ISS ISP IPIPEIF Hardware Setup/Initialization: [4]
- ISS ISP IPIPEIF Register Accessibility During Frame Processing: [5]
- ISS ISP IPIPEIF Summary of Constraints: [6]
- ISS IPIPEIF Register Summary: [7]

Table 8-1135. IPIPEIF_LPFR

Address Offset	0x0000 000C		
Physical Address	0x5201 120C	**Instance**	ISS_IPIPEIF
Description	IPIPEIF Interval of VD / Start line in VD		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								LPFR							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12:0	LPFR	Case-1: Interval of Vertical Sync (VD) Specifies the interval of vertical sync. This register is available when INPSRC = 1 or 3. Case-2: Start Pixel in Vertical Sync (VD) Specifies the start line in vertical sync. This register is available when INPSRC = 2 *This bit field is latched by VD.	RW	0x0000

Table 8-1136. Register Call Summary for Register IPIPEIF_LPFR

ISS ISP

- ISS ISP IPIPEIF Input Interface: [0] [1] [2] [3] [4]
- ISS ISP IPIPEIF Hardware Setup/Initialization: [5]
- ISS ISP IPIPEIF Summary of Constraints: [6] [7]
- ISS IPIPEIF Register Summary: [8]

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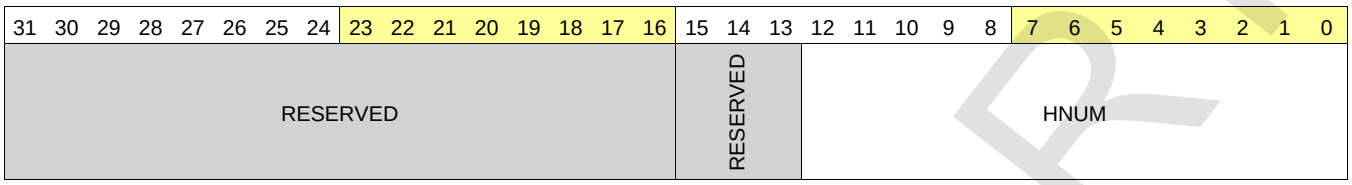
Table 8-1137. IPIPEIF_HNUM

Address Offset	0x0000 0010		
Physical Address	0x5201 1210	**Instance**	ISS_IPIPEIF
Description	IPIPEIF Number of valid pixels per line		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12:0	HNUM	The Number of Valid Pixels in a Line Specifies the number of valid pixels in a horizontal line. This register is available when INPSRC = 1, 2 or 3 *This bit field is latched by VD.	RW	0x0000

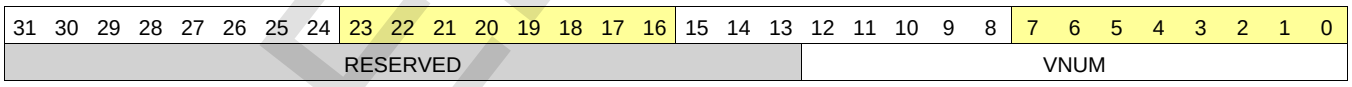
Table 8-1138. Register Call Summary for Register IPIPEIF_HNUM

ISS ISP

- ISS ISP IPIPEIF Input Interface: [0] [1] [2] [3]
- ISS ISP IPIPEIF Hardware Setup/Initialization: [4]
- ISS ISP IPIPEIF Register Accessibility During Frame Processing: [5]
- ISS ISP IPIPEIF Summary of Constraints: [6]
- ISS IPIPEIF Register Summary: [7]

Table 8-1139. IPIPEIF_VNUM

Address Offset	0x0000 0014		
Physical Address	0x5201 1214	**Instance**	ISS_IPIPEIF
Description	IPIPEIF Number of valid lines per frame		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000
12:0	VNUM	The Number of Valid Line in a Vertical Specifies the number of valid line in a vertical. This register is available when INPSRC = 1, 2 or 3 *This bit field is latched by VD.	RW	0x0000

Table 8-1140. Register Call Summary for Register IPIPEIF_VNUM

ISS ISP

- ISS ISP IPIPEIF Input Interface: [0] [1] [2] [3]
- ISS ISP IPIPEIF Hardware Setup/Initialization: [4]
- ISS ISP IPIPEIF Register Accessibility During Frame Processing: [5]
- ISS ISP IPIPEIF Summary of Constraints: [6]
- ISS IPIPEIF Register Summary: [7]

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Table 8-1141. IPIPEIF_ADDRU

Address Offset	0x0000 0018		
Physical Address	0x5201 1218	**Instance**	ISS_IPIPEIF
Description	IPIPEIF Memory Address (Upper)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								ADDRU							

Bits	Field Name	Description	Type	Reset
31:11	RESERVED		R	0x000000
10:0	ADDRU	Memory Address - Upper Memory address upper 11-bits are specified in units of 32-bytes This register is available when INPSRC = 1, 2 or 3. *This bit field is latched by VD.	RW	0x000

Table 8-1142. Register Call Summary for Register IPIPEIF_ADDRU

ISS ISP

- ISS ISP IPIPEIF Input Interface: [0]
- ISS ISP IPIPEIF Hardware Setup/Initialization: [1]
- ISS ISP IPIPEIF Register Accessibility During Frame Processing: [2]
- ISS IPIPEIF Register Summary: [3]

Table 8-1143. IPIPEIF_ADDRL

Address Offset	0x0000 001C		
Physical Address	0x5201 121C	**Instance**	ISS_IPIPEIF
Description	IPIPEIF Memory Address (Lower)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																ADDRL															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:0	ADDRL	Memory Address - Lower Memory address lower 16-bits are specified in units of 32-bytes. This register is available when INPSRC = 1, 2 or 3. *This bit field is latched by VD.	RW	0x0000

Table 8-1144. Register Call Summary for Register IPIPEIF_ADDRL

ISS ISP

- ISS ISP IPIPEIF Input Interface: [0]
- ISS ISP IPIPEIF Hardware Setup/Initialization: [1]
- ISS IPIPEIF Register Summary: [2]

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Table 8-1145. IPIPEIF_ADOFS

Address Offset	0x0000 0020		
Physical Address	0x5201 1220	**Instance**	ISS_IPIPEIF
Description	IPIPEIF Address offset		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				ADOFS											

Bits	Field Name	Description	Type	Reset
31:12	RESERVED		R	0x00000
11:0	ADOFS	Specifies the SDRAM stride for each line in units of 32-bytes. This register is available when reading data from SDRAM: INPSRC1 or INPSRC2 = 1, 2 or 3. Assuming that the first line is at position ADDR, the second line is at address ADDR+ ADOFS, etc. *This bit field is latched by VD.	RW	0x000

Table 8-1146. Register Call Summary for Register IPIPEIF_ADOFS

ISS ISP

- ISS ISP IPIPEIF Input Interface: [0]
- ISS ISP IPIPEIF Hardware Setup/Initialization: [1]
- ISS ISP IPIPEIF Register Accessibility During Frame Processing: [2]
- ISS IPIPEIF Register Summary: [3]

Table 8-1147. IPIPEIF_RSZ

Address Offset	0x0000 0024		
Physical Address	0x5201 1224	**Instance**	ISS_IPIPEIF
Description	IPIPEIF Horizontal Resizing Parameter on IPIPE data path		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RSZ							

Bits	Field Name	Description	Type	Reset
31:7	RESERVED		R	0x0000000
6:0	RSZ	Horizontal Resizing Parameter for IPIPE data path Specifies the horizontal resizing parameter. The RSZ register can be configured within 16 to 112 range. This resizing ratio is determined by 16/RSZ (= 1/1 to 1/7) *This bit field is latched by VD.	RW	0x10

Table 8-1148. Register Call Summary for Register IPIPEIF_RSZ

ISS ISP

- ISS ISP IPIPEIF Horizontal Pixel Decimator (Downsizer) for IPIPE Data Path: [0]
- ISS ISP IPIPEIF Hardware Setup/Initialization: [1]
- ISS ISP IPIPEIF Register Accessibility During Frame Processing: [2]
- ISS IPIPEIF Register Summary: [3]

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Table 8-1149. IPIPEIF_GAIN

Address Offset	0x0000 0028		
Physical Address	0x5201 1228	**Instance**	ISS_IPIPEIF
Description	IPIPEIF Gain Parameter		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								GAIN							

Bits	Field Name	Description	Type	Reset
31:10	RESERVED		R	0x000000
9:0	GAIN	Gain Parameter Specifies the gain applied to RAW data before it is forwarded to the IPIPE module. The gain value is expressed using the U10Q9 fractional format. The range is from 0.00195 (1/512) to 1.99805(1023/512). By default the unity gain is applied, that is, IPIPEIF_GAIN.GAIN = 0x200. The gain is applied to RAW data only (IPIPEIF_CFG1.INPSRC2 != 3): the gain is not applied if the input data is YCbCr. *This bit field is latched by VD.	RW	0x200

Table 8-1150. Register Call Summary for Register IPIPEIF_GAIN

ISS ISP

- ISS ISP IPIPEIF RAW Data Gain for IPIPE Data Path: [0]
- ISS ISP IPIPEIF Hardware Setup/Initialization: [1]
- ISS ISP IPIPEIF Register Accessibility During Frame Processing: [2]
- ISS IPIPEIF Register Summary: [3]
- ISS IPIPEIF Register Description: [4]

Table 8-1151. IPIPEIF_DPCM

Address Offset	0x0000 002C		
Physical Address	0x5201 122C	**Instance**	ISS_IPIPEIF
Description	IPIPEIF DPCM configuration This register applies only if IPIPEIF_CFG1.UNPACK = 1, that is, RAW8 data is read from SDRAM.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													BITS	PRED	ENA

Bits	Field Name	Description	Type	Reset
31:3	RESERVED		R	0x0000 0000
2	BITS	DPCM bit mode for SDRAM data 0x0: 8bit to 10bit DPCM decompression 0x1: 8bit to 12bit DPCM decompression	RW	0
1	PRED	DPCM prediction mode for SDRAM data 0x0: Simple predictor 0x1: Advanced predictor	RW	0

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Bits	Field Name	Description	Type	Reset
0	ENA	DPCM decompression enable for SDRAM data. 0x0: DPCM off (no decompression) 0x1: DPCM on	RW	0

Table 8-1152. Register Call Summary for Register IPIPEIF_DPCM

ISS ISP

- ISS ISP IPIPEIF Decompression (DCPM) Subblock: Unpack and Decompression Function: [0] [1] [2] [3] [4] [5] [6]
- ISS ISP IPIPEIF Hardware Setup/Initialization: [7] [8] [9]
- ISS IPIPEIF Register Summary: [10]

Table 8-1153. IPIPEIF_CFG2

Address Offset	0x0000 0030		
Physical Address	0x5201 1230	**Instance**	ISS_IPIPEIF
Description	IPIPEIF Configuration #2		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								YUV8P	YUV8	DFSDIR	RESERVED	YUV16	VDPOL	HDPOL	INTSW

Bits	Field Name	Description	Type	Reset
31:8	RESERVED		R	0x000000
7	YUV8P	8-bit YUV data unpacking to 16 bits When IPIPEIF_CFG1.INPSRC2 = 0 and IPIPEIF_CFG2.YUV16 = 1, the 8-bit YUV data are transformed into 16-bit YUV data. The way the data are unpacked from 8 bits to 16 bits is controlled by the IPIPEIF_CFG2.YUV8P register. The upper 8 bits of the 16-bit output are set to 0. 0x0: Y output on even pixels C output on odd pixels 0x1: C output on even pixels Y output on odd pixels	RW	0
6	YUV8	YUV 8bit mode When ISIF_CFG1.INPSRC2 = 0 and YUV16 = 1, setting this bit to 1 enables the conversion from 8-bit YUV input to 16-bit YUV. This register is used when the input data from the ISIF module is 8-bit YUV data. 0x0: YUV16 0x1: YUV8 to 16	RW	0
5	DFSDIR	DFS direction Selects the direction of dark frame subtraction. 0x0: VPORT IF(capture frame) - SDRAM (dark frame) 0x1: SDRAM (capture frame) - VPORT IF(dark frame)	RW	0
4	RESERVED	Read returns reset value	RW	0

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Bits	Field Name	Description	Type	Reset

3	YUV16	Data type selection. The behavior of this bit field depends upon other register settings. The functionality is best explained with the following pseudo code:
		if ((CFG1.INPSRC2==0 CFG2.YUV16) ||
		CFG1.INPSRC2==3) {
		data_out[15:0] = yuv[15:0]
		}
		else if (CFG1.INPSRC2==1 CFG2.YUV16
		CFG1.UNPACK=1) {
		data_out[15:8] = gain_clip[7:0];
		data_out[7:0] = 0;
		}
		else {
		data_out[15:12] = 0;
		data_out[11: 0] = gain_clip[11:0];
		}
		where:
		o data_out[15:0] = 16-bit YUV or 12-bit RAW data to ipipe
		o yuv[15:0] = 16-bit YUV data from "horizontal pixel decimator" block.
		o gain_clip[11:0] = 12-bit RAW data from "gain" block.
		0x0: 12-bit RAW data
		0x1: 16-bit YUV data
			RW	0

2	VDPOL	VD Sync Polarity When input VD is active low SYNC pulse, this bit needs to be set to 1. 0x0: Positive 0x1: Negative	RW	0
1	HDPOL	HD Sync Polarity When input HD is active low SYNC pulse, this bit needs to be set to 1. 0x0: Positive 0x1: Negative	RW	0
0	INTSW	IPIPEIF interrupt source selection. This register select the interrupt source. 0x0: Start position of VD from VPORT interface 0x1: Start position of VD from ISIF module	RW	0

Table 8-1154. Register Call Summary for Register IPIPEIF_CFG2

ISS ISP

- ISS ISP IPIPEIF Dark-Frame Subtraction Functionality: [0] [1] [2] [3] [4] [5]
- ISS ISP IPIPEIF (1, 2, 1) Averaging Filter for IPIPE Data Path: [6]
- ISS ISP IPIPEIF YUV4:2:2 8-bits Packed Data Input Coming From ISIF Module: [7] [8] [9]
- ISS ISP IPIPEIF YUV4:2:0 Data Input for Memory-to-Memory Resize Operations: [10] [11]
- ISS ISP IPIPEIF Module Events and Status Checking: [12]
- ISS ISP IPIPEIF Hardware Setup/Initialization: [13] [14] [15] [16] [17] [18] [19] [20]
- ISS IPIPEIF Register Summary: [21]
- ISS IPIPEIF Register Description: [22] [23]

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Table 8-1155. IPIPEIF_INIRSZ

Address Offset	0x0000 0034		
Physical Address	0x5201 1234	**Instance**	ISS_IPIPEIF
Description	IPIPEIF resize initial position - IPIPE data path.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																		ALNSYNC						INIRSZ							

Bits	Field Name	Description	Type	Reset
31:14	RESERVED		R	0x00000
13	ALNSYNC	Align the HSYNC, VSYNC to initial position defined by INIRSZ. 0x0: Disable 0x1: Enable	RW	0
12:0	INIRSZ	Offset used to re-initialize the HD/VD position after resizer. From 0 to 8191 PCLK cycles. Skips INIRSZ pixels for every line.	RW	0x0000

Table 8-1156. Register Call Summary for Register IPIPEIF_INIRSZ

ISS ISP

- ISS ISP IPIPEIF (1, 2, 1) Averaging Filter for IPIPE Data Path: [0]
- ISS ISP IPIPEIF Horizontal Pixel Decimator (Downsizer) for IPIPE Data Path: [1] [2]
- ISS ISP IPIPEIF Hardware Setup/Initialization: [3] [4]
- ISS IPIPEIF Register Summary: [5]

Table 8-1157. IPIPEIF_OCLIP

Address Offset	0x0000 0038		
Physical Address	0x5201 1238	**Instance**	ISS_IPIPEIF
Description	IPIPEIF output clipping value		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				OCLIP											

Bits	Field Name	Description	Type	Reset
31:12	RESERVED		R	0x00000
11:0	OCLIP	Output clipping value after gain control on IPIPE data path. This value is in U12Q0 data format.	RW	0xFFF

Table 8-1158. Register Call Summary for Register IPIPEIF_OCLIP

ISS ISP

- ISS ISP IPIPEIF RAW Data Gain for IPIPE Data Path: [0]
- ISS ISP IPIPEIF Hardware Setup/Initialization: [1]
- ISS IPIPEIF Register Summary: [2]

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Table 8-1159. IPIPEIF_DTUDF

Address Offset	0x0000 003C		
Physical Address	0x5201 123C	**Instance**	ISS_IPIPEIF
Description	IPIPEIF data underflow detection		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED															DTUDF

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:1	RESERVED		R	0x0000
0	DTUDF	Data under flow error status register. Reading 1 shows there is data under flow and at least one data is corrupted while reading from SDRAM. Writing 1 to this register clears (=0) the error (=1) status. Underflow errors are non recoverable at ISP level, need to do a soft reset at ISS level. The IPIPEIF_UDF interrupt is generated when an underflow happens. The interrupt avoids polling this register for errors.	RW	0

Table 8-1160. Register Call Summary for Register IPIPEIF_DTUDF

ISS ISP

- ISS IPIPEIF Register Summary: [0]

Table 8-1161. IPIPEIF_CLKDIV

Address Offset	0x0000 0040		
Physical Address	0x5201 1240	**Instance**	ISS_IPIPEIF
Description	IPIPEIF CLOCK DIVIDER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																CLKDIV															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:0	CLKDIV	IPIPEIF clock rate configuration IPIPE/IPIPEIF clock frequency = M/N x clk_vpss clock frequency. We have M = CLKDIV[15:8] + 1 and N = CLKDIV[7:0] + 1 This register is available when IPIPEIF_CFG1.CLKSEL = 1.	RW	0x0001

Table 8-1162. Register Call Summary for Register IPIPEIF_CLKDIV

ISS ISP

- ISS ISP IPIPEIF Timing Generation: [0] [1] [2]
- ISS ISP IPIPEIF Hardware Setup/Initialization: [3]
- ISS IPIPEIF Register Summary: [4]
- ISS IPIPEIF Register Description: [5]

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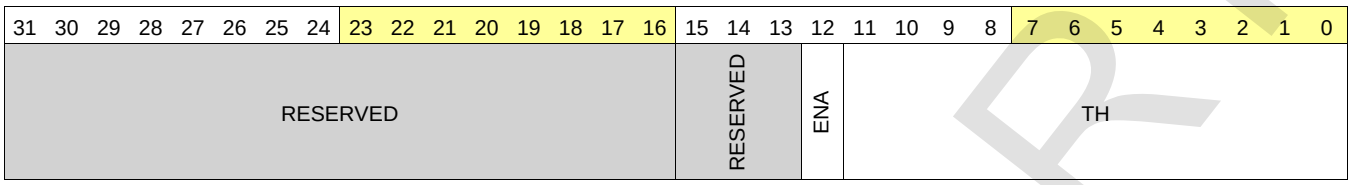
Table 8-1163. IPIPEIF_DPC1

Address Offset	0x0000 0044		
Physical Address	0x5201 1244	**Instance**	ISS_IPIPEIF
Description	IPIPEIF defect pixel correction #1		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12	ENA	DPC enable. Applies DPC for video port data, ISIF input path. 0x0: Disable 0x1: Enable	RW	0
11:0	TH	DPC threshold value	RW	0x000

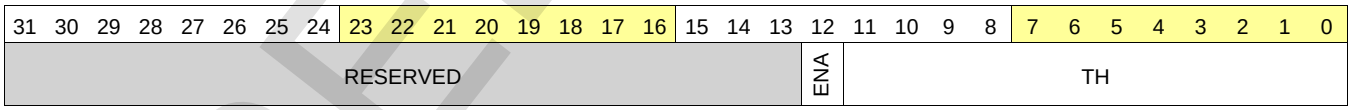
Table 8-1164. Register Call Summary for Register IPIPEIF_DPC1

ISS ISP

- ISS ISP IPIPEIF Dark-Frame Subtraction Functionality: [0] [1]
- ISS ISP IPIPEIF Hardware Setup/Initialization: [2] [3]
- ISS IPIPEIF Register Summary: [4]

Table 8-1165. IPIPEIF_DPC2

Address Offset	0x0000 0048		
Physical Address	0x5201 1248	**Instance**	ISS_IPIPEIF
Description	IPIPEIF defect pixel correction #2		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000
12	ENA	DPC enable. Applies DPC for SDRAM input path. 0x0: Disable 0x1: Enable	RW	0
11:0	TH	DPC threshold value	RW	0x000

Table 8-1166. Register Call Summary for Register IPIPEIF_DPC2

ISS ISP

- ISS ISP IPIPEIF Dark-Frame Subtraction Functionality: [0] [1]
- ISS ISP IPIPEIF Hardware Setup/Initialization: [2] [3]
- ISS IPIPEIF Register Summary: [4]

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Table 8-1167. IPIPEIF_RSZ3A

Address Offset	0x0000 0054		
Physical Address	0x5201 1254	**Instance**	ISS_IPIPEIF
Description	IPIPEIF HORIZONTAL RESIZING PARAMETER FOR H3A		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED						DECIM	AVGFILT	RESERVED	RSZ						

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:10	RESERVED		R	0x00
9	DECIM	Pixel Decimation Enable The decimation rate defined by the RSZ bit field. *This bit field is latched by VD. 0x0: No Decimation 0x1: Decimate	RW	0
8	AVGFILT	Averaging Filter It applies a (1, 2, 1) filter for the RGB/YCbCr data. *This bit field is latched by VD. 0x0: Disable 0x1: Enable	RW	0
7	RESERVED		R	0
6:0	RSZ	Horizontal Resizing Parameter for H3A data path Specifies the horizontal resizing parameter. The RSZ register can be configured within 16 to 112 range. This resizing ratio is determined by 16/RSZ (= 1/1 to 1/7) *This bit field is latched by VD.	RW	0x10

Table 8-1168. Register Call Summary for Register IPIPEIF_RSZ3A

ISS ISP

- ISS ISP IPIPEIF (1, 2 ,1) Averaging Filter for H3A Data Path: [0] [1]
- ISS ISP IPIPEIF Horizontal Pixel Decimator (Downsizer) for H3A Data Path: [2] [3]
- ISS ISP IPIPEIF Hardware Setup/Initialization: [4] [5] [6] [7] [8]
- ISS ISP IPIPEIF Register Accessibility During Frame Processing: [9] [10] [11]
- ISS IPIPEIF Register Summary: [12]

Table 8-1169. IPIPEIF_INIRSZ3A

Address Offset	0x0000 0058		
Physical Address	0x5201 1258	**Instance**	ISS_IPIPEIF
Description	IPIPEIF resize initial position - H3A data path.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																		ALNSYNC	INIRSZ												

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Bits	Field Name	Description	Type	Reset
31:14	RESERVED		R	0x00000
13	ALNSYNC	Align the HD, VD to initial position defined by the INIRSZ bit field. It means that HD and VD are effectively shifted by INIRSZ pixel clock cycles. 0x0: Disable 0x1: Enable	RW	0
12:0	INIRSZ	Offset used to re-initialize the HD/VD position after resizer. From 0 to 8191 PCLK cycles. Skips INIRSZ pixels for every line.	RW	0x0000

Table 8-1170. Register Call Summary for Register IPIPEIF_INIRSZ3A

ISS ISP
- ISS ISP IPIPEIF Horizontal Pixel Decimator (Downsizer) for H3A Data Path: [0] [1]
- ISS IPIPEIF Register Summary: [2]

8.3.5.8 ISS H3A Registers

8.3.5.8.1 ISS H3A Register Summary

Table 8-1171. ISS H3A Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	ISS_H3A Base Address
H3A_PID	R	32	0x0000 0000	0x5201 1400
H3A_PCR	RW	32	0x0000 0004	0x5201 1404
H3A_AFPAX1	RW	32	0x0000 0008	0x5201 1408
H3A_AFPAX2	RW	32	0x0000 000C	0x5201 140C
H3A_AFPAXSTART	RW	32	0x0000 0010	0x5201 1410
H3A_AFIIRSH	RW	32	0x0000 0014	0x5201 1414
H3A_AFBUFST	RW	32	0x0000 0018	0x5201 1418
H3A_AFCOEF010	RW	32	0x0000 001C	0x5201 141C
H3A_AFCOEF032	RW	32	0x0000 0020	0x5201 1420
H3A_AFCOEF054	RW	32	0x0000 0024	0x5201 1424
H3A_AFCOEF076	RW	32	0x0000 0028	0x5201 1428
H3A_AFCOEF098	RW	32	0x0000 002C	0x5201 142C
H3A_AFCOEF0010	RW	32	0x0000 0030	0x5201 1430
H3A_AFCOEF110	RW	32	0x0000 0034	0x5201 1434
H3A_AFCOEF132	RW	32	0x0000 0038	0x5201 1438
H3A_AFCOEF154	RW	32	0x0000 003C	0x5201 143C
H3A_AFCOEF176	RW	32	0x0000 0040	0x5201 1440
H3A_AFCOEF198	RW	32	0x0000 0044	0x5201 1444
H3A_AFCOEF1010	RW	32	0x0000 0048	0x5201 1448
H3A_AEWWIN1	RW	32	0x0000 004C	0x5201 144C
H3A_AEWINSTART	RW	32	0x0000 0050	0x5201 1450
H3A_AEWINBLK	RW	32	0x0000 0054	0x5201 1454
H3A_AEWSUBWIN	RW	32	0x0000 0058	0x5201 1458
H3A_AEWBUFST	RW	32	0x0000 005C	0x5201 145C
H3A_AEWCFG	RW	32	0x0000 0060	0x5201 1460
H3A_LINE_START	RW	32	0x0000 0064	0x5201 1464
H3A_VFV_CFG1	RW	32	0x0000 0068	0x5201 1468
H3A_VFV_CFG2	RW	32	0x0000 006C	0x5201 146C

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Table 8-1171. ISS H3A Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	ISS_H3A Base Address
H3A_VFV_CFG3	RW	32	0x0000 0070	0x5201 1470
H3A_VFV_CFG4	RW	32	0x0000 0074	0x5201 1474
H3A_HVF_THR	RW	32	0x0000 0078	0x5201 1478
H3A_ADVANCED	RW	32	0x0000 007C	0x5201 147C

8.3.5.8.2 ISS H3A Register Description

Table 8-1172. H3A_PID

Address Offset	0x0000 0000		
Physical Address	0x5201 1400	**Instance**	ISS_H3A
Description	Peripheral Revision and Class Information		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCHEME		RESERVED		FUNC												RTL					MAJOR			RESERVED					MINOR			

Bits	Field Name	Description	Type	Reset
31:30	SCHEME		R	0x1
29:28	RESERVED		R	0x0
27:16	FUNC		R	0xD01
15:11	RTL		R	0x00
10:8	MAJOR		R	0x0
7:6	RESERVED		R	0x0
5:0	MINOR		R	0x00

Table 8-1173. Register Call Summary for Register H3A_PID

ISS ISP

- ISS H3A Register Summary: [0]

Table 8-1174. H3A_PCR

Address Offset	0x0000 0004		
Physical Address	0x5201 1404	**Instance**	ISS_H3A
Description	Peripheral Control Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AVE2LMT										OVF	AF_VF_EN	AEW_MED_EN	BUSYAEAWB	AEW_ALAW_EN	AEW_EN	BUSYAF	FVMODE	RGBPOS			MED_TH									AF_MED_EN	AF_ALAW_EN	AF_EN

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Bits	Field Name	Description	Type	Reset
31:22	AVE2LMT	AE/AWB Saturation Limit This is the value that all sub sampled pixels in the AE/AWB engine are compared to. If the data is greater or equal to this data then the block is considered saturated.	RW	0x3FF
21	OVF	H3A module overflow status bit. If the H3A module overflows it will keep sending data. The software can read this status bit during vertical blanking period to ensure that no overflow happened while writing out the data to SDRAM. There is also an interrupt at ISP level (H3A_OVF) which can be used to monitor this. 0x0: Read 0: No overflow pending Write 0: Status bit unchanged 0x1: Read 1: Overflow happened while writing out the data. Output data likely to be corrupted. Write 1: Clear the status bit.	RW	0
20	AF_VF_EN	AF Vertical Focus Enable 0x0: 4 Color Horizontal FV only 0x1: 1 Color Horizontal FV and 1 Color Vertical FV	RW	0
19	AEW_MED_EN	AE/AWB Median filter Enable If the median filter is enabled, then the 1st 2 and last 2 pixels in the frame are not filtered. 0x0: Disable Auto Focus median filter 0x1: Enable Auto Focus median filter	RW	0
18	BUSYAEAWB	Busy bit for AE/AWB	R	0
17	AEW_ALAW_EN	AE/AWB A-law Enable 0x0: Disable Auto exposure/white balance A-law table 0x1: Enable Auto exposure/white balance A-law table.	RW	0
16	AEW_EN	AE/AWB enable 0x0: Disable Auto exposure/white balance 0x1: Enable Auto exposure/white balance	RW	0
15	BUSYAF	Busy bit for AF.	R	0
14	FVMODE	Focus Value Accumulation Mode 0x0: Sum mode. 0x1: Peak mode.	RW	0
13:11	RGBPOS	Red, Green, and blue pixel location in the AF windows RGBPOS(0): GR and GB as Bayer pattern RGBPOS(1): RG and GB as Bayer pattern RGBPOS(2): GR and BG as Bayer pattern RGBPOS(3): RG and BG as Bayer pattern RGBPOS(4): GG and RB as custom pattern RGBPOS(5): RB and GG as custom pattern 6 and 7 are reserved This Value is only used if VF is disabled	RW	0x0
10:3	MED_TH	Median filter threshold.	RW	0xFF
2	AF_MED_EN	Auto Focus Median filter Enable If the median filter is enabled, then the 1st 2 and last 2 pixels in the frame are not in the valid region. Therefore the paxel start/end and IIR filter start positions should not be set within the 1st and last 2 pixels. 0x0: Disable AF median filter. 0x1: Enable AF median filter.	RW	0
1	AF_ALAW_EN	AF A-law table enable 0x0: Disable Auto Focus A-law table 0x1: Enable Auto Focus A-law table	RW	0

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Bits	Field Name	Description	Type	Reset
0	AF_EN	AF enable 0x0: Disable Auto Focus Engine 0x1: Enable Auto Focus Engine	RW	0

Table 8-1175. Register Call Summary for Register H3A_PCR

ISS ISP

- ISS ISP H3A Interrupts: [0]
- ISS ISP H3A Optional Preprocessing: [1] [2] [3] [4]
- ISS ISP H3A Autofocus Engine: [5] [6] [7] [8]
- ISS ISP H3A AE/AWB Engine: [9]
- ISS ISP H3A Events and Status Checking: [10] [11] [12] [13] [14] [15]
- ISS ISP H3A Hardware Setup/Initialization: [16] [17] [18] [19] [20] [21] [22] [23] [24] [25]
- ISS ISP H3A Enable/Disable Hardware: [26] [27] [28] [29]
- ISS ISP H3A Register Accessibility During Frame Processing: [30] [31] [32] [33] [34] [35] [36]
- ISS ISP H3A Interframe Operations: [37]
- ISS H3A Register Summary: [38]

Table 8-1176. H3A_AFPAX1

Address Offset	0x0000 0008		
Physical Address	0x5201 1408	**Instance**	ISS_H3A
Description	Setup for the AF Engine Paxel Configuration		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PAXW								RESERVED								PAXH							

Bits	Field Name	Description	Type	Reset
31:24	RESERVED		R	0x00
23:16	PAXW	AF Engine Paxel Width The width of the paxel is the value of this register plus 1 multiplied by 2. The minimum width is expected to be 8 pixels. * This value is shadowed and latched on the rising edge of VSYNC.	RW	0x00
15:8	RESERVED		R	0x00
7:0	PAXH	AF Engine Paxel Height The height of the paxel is the value of this register plus 1 multiplied by 2 with a final value of 2-256 (even) * This value is shadowed and latched on the rising edge of VSYNC.	RW	0x00

Table 8-1177. Register Call Summary for Register H3A_AFPAX1

ISS ISP

- ISS ISP H3A Autofocus Engine: [0] [1] [2] [3] [4]
- ISS ISP H3A Hardware Setup/Initialization: [5] [6]
- ISS ISP H3A Register Accessibility During Frame Processing: [7]
- ISS ISP H3A Summary of Constraints: [8] [9] [10] [11] [12] [13] [14] [15] [16] [17]
- ISS H3A Register Summary: [18]

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Table 8-1178. H3A_AFPAX2

Address Offset	0x0000 000C		
Physical Address	0x5201 140C	**Instance**	ISS_H3A
Description	Setup for the AF Engine Paxel Configuration		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								AFINCH								AFINCV								PAXVC							
PAXHC																															

Bits	Field Name	Description	Type	Reset
31:21	RESERVED		R	0x000
20:17	AFINCH	AF Engine Column Increments Number of columns to increment in a paxel plus 1 multiplied by 2. Thus, the number of columns that can be skipped between two processed line pairs is 2-32 (even). The starting two columns in a paxel are first processed before this field is applied. This must be set so that there are at least 4 samples on a line when combined with the number of horizontal paxels. * This value is shadowed and latched on the rising edge of VSYNC.	RW	0x0
16:13	AFINCV	AF Engine Line Increments Number of lines to increment in a Paxel plus 1 multiplied by 2. Incrementing the line in a paxel is always done on a line pair due to the fact that the RGB pattern falls in two lines. If all the lines are to be processed, this field should be set to zero, and thus line count is incremented by 2 following a line pair. Thus, the number of lines that can be skipped between two processed line pairs is 0-30 (even). The starting two lines in a paxel are first processed before this field is applied. * This value is shadowed and latched on the rising edge of VSYNC.	RW	0x0
12:6	PAXVC	AF Engine Vertical Paxel Count The number of paxels in the vertical direction plus 1. The maximum number of vertical paxels in a frame should not exceed 128. The value should be set to ensure that the bandwidth requirements and buffer size are not exceeded. * This value is shadowed and latched on the rising edge of VSYNC.	RW	0x00
5:0	PAXHC	AF Engine Horizontal Paxel Count The number of paxels in the horizontal direction plus 1. It is illegal to set a number that is greater than 35 (total of 36 paxels in the horizontal direction). The minimum number of paxels should be 2 (valid range for the field is 1-35). * This value is shadowed and latched on the rising edge of VSYNC.	RW	0x00

Table 8-1179. Register Call Summary for Register H3A_AFPAX2

ISS ISP

- ISS ISP H3A Autofocus Engine: [0] [1] [2] [3] [4] [5] [6]
- ISS ISP H3A Hardware Setup/Initialization: [7] [8] [9] [10]
- ISS ISP H3A Register Accessibility During Frame Processing: [11]
- ISS ISP H3A Summary of Constraints: [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23] [24] [25] [26] [27] [28]
- ISS H3A Register Summary: [29]

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Table 8-1180. H3A_AFPAXSTART

Address Offset	0x0000 0010		
Physical Address	0x5201 1410	**Instance**	ISS_H3A
Description	Start Position for AF Engine Paxels		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PAXSH								RESERVED				PAXSV											

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:16	PAXSH	AF Engine Paxel Horizontal start position Range: 2-4094 PAXSH must be equal to or greater than (IIRSH + 2) This value must be even if Vertical mode is not enabled. If Vertical mode is enabled then the lower bit of PAXSH and IIRSH must be equal. * This value is shadowed and latched on the rising edge of VSYNC.	RW	0x000
15:12	RESERVED		R	0x0
11:0	PAXSV	AF Engine Paxel Vertical start position Range: 0-4095 Sets the vertical line for the first paxel. This value must be greater then or equal to 8 if the vertical mode is enabled. * This value is shadowed and latched on the rising edge of VSYNC.	RW	0x000

Table 8-1181. Register Call Summary for Register H3A_AFPAXSTART

ISS ISP

- ISS ISP H3A Autofocus Engine: [0] [1] [2] [3] [4]
- ISS ISP H3A Hardware Setup/Initialization: [5] [6]
- ISS ISP H3A Register Accessibility During Frame Processing: [7]
- ISS ISP H3A Summary of Constraints: [8] [9] [10] [11] [12] [13] [14]
- ISS H3A Register Summary: [15]

Table 8-1182. H3A_AFIIRSH

Address Offset	0x0000 0014		
Physical Address	0x5201 1414	**Instance**	ISS_H3A
Description	Start Position for IIRSH		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				IIRSH											

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Bits	Field Name	Description	Type	Reset
31:12	RESERVED		R	0x00000
11:0	IIRSH	AF Engine IIR Horizontal Start Position Range from 0-4094. When the horizontal position of a line equals this value the shift registers are cleared on the next pixel. This value must be even if Vertical mode is not enabled. If vertical mode is enabled then the lower bit must match the paxel horizontal start position. * This value is shadowed and latched on the rising edge of VSYNC.	RW	0x000

Table 8-1183. Register Call Summary for Register H3A_AFIIRSH

ISS ISP

- ISS ISP H3A Autofocus Engine: [0] [1] [2]
- ISS ISP H3A Hardware Setup/Initialization: [3]
- ISS ISP H3A Register Accessibility During Frame Processing: [4]
- ISS ISP H3A Summary of Constraints: [5] [6] [7] [8] [9] [10] [11] [12] [13] [14]
- ISS H3A Register Summary: [15]

Table 8-1184. H3A_AFBUFST

Address Offset	0x0000 0018		
Physical Address	0x5201 1418	**Instance**	ISS_H3A
Description	SDRAM destination address for AF engine statistics		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AFBUFST																								RESERVED							

Bits	Field Name	Description	Type	Reset
31:5	AFBUFST	SDRAM destination address for AF engine statistics The SDRAM destination address for the AF statistics. The 6 LSBs are ignored, address must be on a 64-byte boundary. This field can be altered even when the AF is busy. Change will take place only for the next frame. However, note that reading this register will always give the latest value.	RW	0x0000000
4:0	RESERVED		R	0x00

Table 8-1185. Register Call Summary for Register H3A_AFBUFST

ISS ISP

- ISS ISP H3A DMA Interface: [0] [1] [2]
- ISS ISP H3A Hardware Setup/Initialization: [3]
- ISS ISP H3A Summary of Constraints: [4]
- ISS H3A Register Summary: [5]

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Table 8-1186. H3A_AFCOEF010

Address Offset	0x0000 001C		
Physical Address	0x5201 141C	**Instance**	ISS_H3A
Description	IIR filter coefficient data for SET 0.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								COEFF1								RESERVED								COEFF0							

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:16	COEFF1	AF Engine IIR filter Coefficient #1 (Set 0) The range is signed -32 = value = 31 +63/64	RW	0x000
15:12	RESERVED		R	0x0
11:0	COEFF0	AF Engine IIR filter Coefficient #0 (Set 0) The range is signed -32 = value = 31 +63/64	RW	0x000

Table 8-1187. Register Call Summary for Register H3A_AFCOEF010

ISS ISP

- ISS ISP H3A Autofocus Engine: [0]
- ISS ISP H3A Hardware Setup/Initialization: [1]
- ISS H3A Register Summary: [2]

Table 8-1188. H3A_AFCOEF032

Address Offset	0x0000 0020		
Physical Address	0x5201 1420	**Instance**	ISS_H3A
Description	IIR filter coefficient data for SET 0.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								COEFF3								RESERVED								COEFF2							

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:16	COEFF3	AF Engine IIR filter Coefficient #3 (Set 0) The range is signed -32 = value = 31 +63/64	RW	0x000
15:12	RESERVED		R	0x0
11:0	COEFF2	AF Engine IIR filter Coefficient #2 (Set 0) The range is signed -32 = value = 31 +63/64	RW	0x000

Table 8-1189. Register Call Summary for Register H3A_AFCOEF032

ISS ISP

- ISS ISP H3A Hardware Setup/Initialization: [0]
- ISS H3A Register Summary: [1]

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Table 8-1190. H3A_AFCOEF054

Address Offset	0x0000 0024		
Physical Address	0x5201 1424	**Instance**	ISS_H3A
Description	IIR filter coefficient data for SET 0.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								COEFF5								RESERVED								COEFF4							

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:16	COEFF5	AF Engine IIR filter Coefficient #5 (Set 0) The range is signed -32 = value = 31 +63/64	RW	0x000
15:12	RESERVED		R	0x0
11:0	COEFF4	AF Engine IIR filter Coefficient #4 (Set 0) The range is signed -32 = value = 31 +63/64	RW	0x000

Table 8-1191. Register Call Summary for Register H3A_AFCOEF054

ISS ISP

- ISS ISP H3A Hardware Setup/Initialization: [0]
- ISS H3A Register Summary: [1]

Table 8-1192. H3A_AFCOEF076

Address Offset	0x0000 0028		
Physical Address	0x5201 1428	**Instance**	ISS_H3A
Description	IIR filter coefficient data for SET 0.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								COEFF7								RESERVED								COEFF6							

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:16	COEFF7	AF Engine IIR filter Coefficient #7 (Set 0) The range is signed -32 = value = 31 +63/64	RW	0x000
15:12	RESERVED		R	0x0
11:0	COEFF6	AF Engine IIR filter Coefficient #6 (Set 0) The range is signed -32 = value = 31 +63/64	RW	0x000

Table 8-1193. Register Call Summary for Register H3A_AFCOEF076

ISS ISP

- ISS ISP H3A Hardware Setup/Initialization: [0]
- ISS H3A Register Summary: [1]

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Table 8-1194. H3A_AFCOEF098

Address Offset	0x0000 002C		
Physical Address	0x5201 142C	**Instance**	ISS_H3A
Description	IIR filter coefficient data for SET 0.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								COEFF9								RESERVED				COEFF8											

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:16	COEFF9	AF Engine IIR filter Coefficient #9 (Set 0) The range is signed -32 = value = 31 +63/64	RW	0x000
15:12	RESERVED		R	0x0
11:0	COEFF8	AF Engine IIR filter Coefficient #8 (Set 0) The range is signed -32 = value = 31 +63/64	RW	0x000

Table 8-1195. Register Call Summary for Register H3A_AFCOEF098

ISS ISP

- ISS ISP H3A Hardware Setup/Initialization: [0]
- ISS H3A Register Summary: [1]

Table 8-1196. H3A_AFCOEF0010

Address Offset	0x0000 0030		
Physical Address	0x5201 1430	**Instance**	ISS_H3A
Description	IIR filter coefficient data for SET 0.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				COEFF10											

Bits	Field Name	Description	Type	Reset
31:12	RESERVED		R	0x00000
11:0	COEFF10	AF Engine IIR filter Coefficient #10 (Set 0) The range is signed -32 = value = 31 +63/64	RW	0x000

Table 8-1197. Register Call Summary for Register H3A_AFCOEF0010

ISS ISP

- ISS ISP H3A Autofocus Engine: [0]
- ISS ISP H3A Hardware Setup/Initialization: [1]
- ISS H3A Register Summary: [2]

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Table 8-1198. H3A_AFCOEF110

Address Offset	0x0000 0034		
Physical Address	0x5201 1434	**Instance**	ISS_H3A
Description	IIR filter coefficient data for SET 1.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								COEFF1								RESERVED								COEFF0							

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:16	COEFF1	AF Engine IIR filter Coefficient #1 (Set 1) The range is signed -32 = value = 31 +63/64	RW	0x000
15:12	RESERVED		R	0x0
11:0	COEFF0	AF Engine IIR filter Coefficient #0 (Set 1) The range is signed -32 = value = 31 +63/64	RW	0x000

Table 8-1199. Register Call Summary for Register H3A_AFCOEF110

ISS ISP

- ISS ISP H3A Autofocus Engine: [0]
- ISS ISP H3A Hardware Setup/Initialization: [1]
- ISS H3A Register Summary: [2]

Table 8-1200. H3A_AFCOEF132

Address Offset	0x0000 0038		
Physical Address	0x5201 1438	**Instance**	ISS_H3A
Description	IIR filter coefficient data for SET 1.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								COEFF3								RESERVED								COEFF2							

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:16	COEFF3	AF Engine IIR filter Coefficient #3 (Set 1) The range is signed -32 = value = 31 +63/64	RW	0x000
15:12	RESERVED		R	0x0
11:0	COEFF2	AF Engine IIR filter Coefficient #2 (Set 1) The range is signed -32 = value = 31 +63/64	RW	0x000

Table 8-1201. Register Call Summary for Register H3A_AFCOEF132

ISS ISP

- ISS ISP H3A Hardware Setup/Initialization: [0]
- ISS H3A Register Summary: [1]

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Table 8-1202. H3A_AFCOEF154

Address Offset	0x0000 003C		
Physical Address	0x5201 143C	**Instance**	ISS_H3A
Description	IIR filter coefficient data for SET 1.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								COEFF5								RESERVED								COEFF4							

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:16	COEFF5	AF Engine IIR filter Coefficient #5 (Set 1) The range is signed -32 = value = 31 +63/64	RW	0x000
15:12	RESERVED		R	0x0
11:0	COEFF4	AF Engine IIR filter Coefficient #4 (Set 1) The range is signed -32 = value = 31 +63/64	RW	0x000

Table 8-1203. Register Call Summary for Register H3A_AFCOEF154

ISS ISP

- ISS ISP H3A Hardware Setup/Initialization: [0]
- ISS H3A Register Summary: [1]

Table 8-1204. H3A_AFCOEF176

Address Offset	0x0000 0040		
Physical Address	0x5201 1440	**Instance**	ISS_H3A
Description	IIR filter coefficient data for SET 1.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								COEFF7								RESERVED								COEFF6							

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:16	COEFF7	AF Engine IIR filter Coefficient #7 (Set 1) The range is signed -32 = value = 31 +63/64	RW	0x000
15:12	RESERVED		R	0x0
11:0	COEFF6	AF Engine IIR filter Coefficient #6 (Set 1) The range is signed -32 = value = 31 +63/64	RW	0x000

Table 8-1205. Register Call Summary for Register H3A_AFCOEF176

ISS ISP

- ISS ISP H3A Hardware Setup/Initialization: [0]
- ISS H3A Register Summary: [1]

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Table 8-1206. H3A_AFCOEF198

Address Offset	0x0000 0044		
Physical Address	0x5201 1444	**Instance**	ISS_H3A
Description	IIR filter coefficient data for SET 1.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								COEFF9								RESERVED				COEFF8											

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:16	COEFF9	AF Engine IIR filter Coefficient #9 (Set 1) The range is signed -32 = value = 31 +63/64	RW	0x000
15:12	RESERVED		R	0x0
11:0	COEFF8	AF Engine IIR filter Coefficient #8 (Set 1) The range is signed -32 = value = 31 +63/64	RW	0x000

Table 8-1207. Register Call Summary for Register H3A_AFCOEF198

ISS ISP

- ISS ISP H3A Hardware Setup/Initialization: [0]
- ISS H3A Register Summary: [1]

Table 8-1208. H3A_AFCOEF1010

Address Offset	0x0000 0048		
Physical Address	0x5201 1448	**Instance**	ISS_H3A
Description	IIR filter coefficient data for SET 1.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				COEFF10											

Bits	Field Name	Description	Type	Reset
31:12	RESERVED		R	0x00000
11:0	COEFF10	AF Engine IIR filter Coefficient #10 (Set 1) The range is signed -32 = value = 31 +63/64	RW	0x000

Table 8-1209. Register Call Summary for Register H3A_AFCOEF1010

ISS ISP

- ISS ISP H3A Autofocus Engine: [0]
- ISS ISP H3A Hardware Setup/Initialization: [1]
- ISS H3A Register Summary: [2]

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Table 8-1210. H3A_AEWWIN1

Address Offset	0x0000 004C		
Physical Address	0x5201 144C	**Instance**	ISS_H3A
Description	Configuration for AE/AWB Windows.		
Type	RW		

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
WINH	RESERVED	WINW	WINVC	WINHC

Bits	Field Name	Description	Type	Reset
31:24	WINH	AE/AWB Engine Window Height This specifies the window height in an even number of pixels, the window height is the value plus 1 multiplied by 2. The final value can be from 2-512 (even) * This value is shadowed and latched on the rising edge of VSYNC.	RW	0x00
23:21	RESERVED		R	0x0
20:13	WINW	AE/AWB Engine Window Width This specifies the window width in an even number of pixels, the window width is the value plus 1 multiplied by 2. The minimum width is expected to be 8 pixels. * This value is shadowed and latched on the rising edge of VSYNC.	RW	0x00
12:6	WINVC	AE/AWB Engine Vertical Window Count The number of windows in the vertical direction plus 1. The maximum number of vertical windows in a frame should not exceed 128. The value should be set to ensure that the bandwidth requirements and buffer size are not exceeded * This value is shadowed and latched on the rising edge of VSYNC.	RW	0x00
5:0	WINHC	AE/AWB Engine Horizontal Window Count The number of horizontal windows plus 1. The maximum number of horizontal windows is 35 plus 1 (36). The minimum number of windows should be 2 (valid range for the field is 1-35). * This value is shadowed and latched on the rising edge of VSYNC.	RW	0x00

Table 8-1211. Register Call Summary for Register H3A_AEWWIN1

ISS ISP

- ISS ISP H3A AE/AWB Engine: [0] [1] [2] [3] [4] [5] [6] [7]
- ISS ISP H3A Hardware Setup/Initialization: [8] [9] [10] [11]
- ISS ISP H3A Register Accessibility During Frame Processing: [12]
- ISS ISP H3A Summary of Constraints: [13] [14] [15] [16] [17] [18] [19] [20] [21] [22]
- ISS H3A Register Summary: [23]

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Table 8-1212. H3A_AEWINSTART

Address Offset	0x0000 0050		
Physical Address	0x5201 1450	**Instance**	ISS_H3A
Description	Start position for AE/AWB Windows.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								WINSV								RESERVED								WINSH							

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:16	WINSV	AE/AWB Engine Vertical Window Start Position Sets the first line for the first window. Range 0-4095 * This value is shadowed and latched on the rising edge of VSYNC.	RW	0x000
15:12	RESERVED		R	0x0
11:0	WINSH	AE/AWB Engine Horizontal Window Start Position Sets the horizontal position for the first window on each line. Range 0-4095 * This value is shadowed and latched on the rising edge of VSYNC.	RW	0x000

Table 8-1213. Register Call Summary for Register H3A_AEWINSTART

ISS ISP

- ISS ISP H3A AE/AWB Engine: [0] [1] [2] [3]
- ISS ISP H3A Hardware Setup/Initialization: [4] [5]
- ISS ISP H3A Register Accessibility During Frame Processing: [6]
- ISS H3A Register Summary: [7]

Table 8-1214. H3A_AEWINBLK

Address Offset	0x0000 0054		
Physical Address	0x5201 1454	**Instance**	ISS_H3A
Description	Start position and height for black line of AE/AWB Windows		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								WINSV								RESERVED								WINH							

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:16	WINSV	AE/AWB Engine Vertical Window Start Position for single black line of windows Sets the first line for the single black line of windows. * This value is shadowed and latched on the rising edge of VSYNC. Range 0-4095 Note that the horizontal start and the horizontal number of windows will be similar to the regular windows	RW	0x000
15:7	RESERVED		R	0x000

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Bits	Field Name	Description	Type	Reset
6:0	WINH	AE/AWB Engine Window Height for the single black line of windows This specifies the window height in an even number of pixels, the window height is the value plus 1 multiplied by 2. The final value can be from 2-256 (even) * This value is shadowed and latched on the rising edge of VSYNC.	RW	0x00

Table 8-1215. Register Call Summary for Register H3A_AEWINBLK

ISS ISP

- ISS ISP H3A AE/AWB Engine: [0] [1] [2] [3]
- ISS ISP H3A Hardware Setup/Initialization: [4] [5]
- ISS ISP H3A Register Accessibility During Frame Processing: [6]
- ISS ISP H3A Summary of Constraints: [7] [8]
- ISS H3A Register Summary: [9]

Table 8-1216. H3A_AEWSUBWIN

Address Offset	0x0000 0058		
Physical Address	0x5201 1458	**Instance**	ISS_H3A
Description	Configuration for subsample data in AE/AWB window.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				AEWINCV				RESERVED				AEWINCH			

Bits	Field Name	Description	Type	Reset
31:12	RESERVED		R	0x00000
11:8	AEWINCV	AE/AWB Engine Vertical Sampling Point Increment Sets vertical distance between sub-samples within a window plus 1 multiplied by 2. The final range is 2-32. * This value is shadowed and latched on the rising edge of VSYNC.	RW	0x0
7:4	RESERVED		R	0x0
3:0	AEWINCH	AE/AWB Engine Horizontal Sampling Point Increment Sets horizontal distance between sub-samples within a window plus 1 multiplied by 2. The final range is 2-32. * This value is shadowed and latched on the rising edge of VSYNC.	RW	0x0

Table 8-1217. Register Call Summary for Register H3A_AEWSUBWIN

ISS ISP

- ISS ISP H3A AE/AWB Engine: [0] [1] [2] [3]
- ISS ISP H3A Hardware Setup/Initialization: [4] [5]
- ISS ISP H3A Register Accessibility During Frame Processing: [6]
- ISS ISP H3A Summary of Constraints: [7]
- ISS H3A Register Summary: [8]

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Table 8-1218. H3A_AEWBUFST

Address Offset	0x0000 005C		
Physical Address	0x5201 145C	**Instance**	ISS_H3A
Description	SDRAM destination address for AE/AWB engine statistics		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AEWBUFST																								RESERVED							

Bits	Field Name	Description	Type	Reset
31:5	AEWBUFST	SDRAM destination address for AE/AWB engine statistics The start location in SDRAM for the AE/AWB statistics. The 6 LSB are ignored, address should be on a 64-byte boundary This field can be altered even when the AE/AWB is busy. Change will take place only for the next frame. However, note that reading this register will always give the latest value.	RW	0x0000000
4:0	RESERVED		R	0x00

Table 8-1219. Register Call Summary for Register H3A_AEWBUFST

ISS ISP

- ISS ISP H3A DMA Interface: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23] [24] [25] [26] [27]
- ISS ISP H3A Hardware Setup/Initialization: [28]
- ISS ISP H3A Register Accessibility During Frame Processing: [29]
- ISS H3A Register Summary: [30]

Table 8-1220. H3A_AEWCFG

Address Offset	0x0000 0060		
Physical Address	0x5201 1460	**Instance**	ISS_H3A
Description	Configuration for AE/AWB		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						AEFMT		RESERVED				SUMSHFT			

Bits	Field Name	Description	Type	Reset
31:10	RESERVED		R	0x000000
9:8	AEFMT	AE/AWB output format 0 = sum of squares 1 = min/max 2 = sum only; no sum of squares or min/max * This value is shadowed and latched on the rising edge of VSYNC	RW	0x0
7:4	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
3:0	SUMSHFT	AE/AWB engine shift value for the accumulation of pixel values This bit field sets the right shift value which is applied on the result of the pixel accumulation before it is stored in the packet. The accumulation takes place on 26 bits which is enough for 10-bit data and a maximum widow size of 512 x 512 which results into the accumulation of 256 x 256 pixels of the same color. The shift value must be set such that the result fits on 16 bits. SUMSHFT = right shift value. Range: 0 -15 * This value is shadowed and latched on the rising edge of VSYNC	RW	0x0

Table 8-1221. Register Call Summary for Register H3A_AEWCFG

ISS ISP

- ISS ISP H3A AE/AWB Engine: [0] [1] [2] [3] [4]
- ISS ISP H3A DMA Interface: [5] [6] [7]
- ISS ISP H3A Hardware Setup/Initialization: [8] [9]
- ISS ISP H3A Register Accessibility During Frame Processing: [10]
- ISS H3A Register Summary: [11]

Table 8-1222. H3A_LINE_START

Address Offset	0x0000 0064		
Physical Address	0x5201 1464	**Instance**	ISS_H3A
Description	Line Framing Logic Register In certain cases the number of clock cycles between HD pulses will be greater than the line buffer included in the H3A module. The framing module prior to the line buffer enables to control the data which is input to the line buffer.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SLV																LINE_START															

Bits	Field Name	Description	Type	Reset
31:16	SLV	Start Line Vertical Specifies how many lines after the VD rising edge the real frame starts.	W	0x0000
15:0	LINE_START	Line Start The framing module uses the LINE_START bit field to find the position of the first pixel to place into the line buffer. Range: 0-65535	RW	0x0000

Table 8-1223. Register Call Summary for Register H3A_LINE_START

ISS ISP

- ISS ISP H3A Line Framing Logic: [0] [1] [2] [3]
- ISS ISP H3A Autofocus Engine: [4]
- ISS ISP H3A Hardware Setup/Initialization: [5] [6] [7] [8]
- ISS H3A Register Summary: [9]

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Table 8-1224. H3A_VFV_CFG1

Address Offset	0x0000 0068		
Physical Address	0x5201 1468	**Instance**	ISS_H3A
Description	Vertical focus value configuration 1.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VCOEF1_3								VCOEF1_2								VCOEF1_1								VCOEF1_0							

Bits	Field Name	Description	Type	Reset
31:24	VCOEF1_3	Vertical FV FIR 1 coefficient 3	RW	0x00
23:16	VCOEF1_2	Vertical FV FIR 1 coefficient 2	RW	0x00
15:8	VCOEF1_1	Vertical FV FIR 1 coefficient 1	RW	0x00
7:0	VCOEF1_0	Vertical FV FIR 1 coefficient 0	RW	0x00

Table 8-1225. Register Call Summary for Register H3A_VFV_CFG1

ISS ISP

- ISS ISP H3A Autofocus Engine: [0]
- ISS ISP H3A Hardware Setup/Initialization: [1]
- ISS H3A Register Summary: [2]

Table 8-1226. H3A_VFV_CFG2

Address Offset	0x0000 006C		
Physical Address	0x5201 146C	**Instance**	ISS_H3A
Description	Vertical focus value configuration 2.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VTHR1																RESERVED								VCOEF1_4							

Bits	Field Name	Description	Type	Reset
31:16	VTHR1	Threshold for vertical FV FIR 1	RW	0x0000
15:8	RESERVED		R	0x00
7:0	VCOEF1_4	Vertical FV FIR 1 coefficient 4	RW	0x00

Table 8-1227. Register Call Summary for Register H3A_VFV_CFG2

ISS ISP

- ISS ISP H3A Autofocus Engine: [0] [1] [2]
- ISS ISP H3A Hardware Setup/Initialization: [3]
- ISS H3A Register Summary: [4]

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Table 8-1228. H3A_VFV_CFG3

Address Offset	0x0000 0070		
Physical Address	0x5201 1470	**Instance**	ISS_H3A
Description	Vertical focus value configuration 4.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VCOEF2_3								VCOEF2_2								VCOEF2_1								VCOEF2_0							

Bits	Field Name	Description	Type	Reset
31:24	VCOEF2_3	Vertical FV FIR 2 coefficient 3	RW	0x00
23:16	VCOEF2_2	Vertical FV FIR 2 coefficient 2	RW	0x00
15:8	VCOEF2_1	Vertical FV FIR 2 coefficient 1	RW	0x00
7:0	VCOEF2_0	Vertical FV FIR 2 coefficient 0	RW	0x00

Table 8-1229. Register Call Summary for Register H3A_VFV_CFG3

ISS ISP

- ISS ISP H3A Autofocus Engine: [0]
- ISS ISP H3A Hardware Setup/Initialization: [1]
- ISS H3A Register Summary: [2]

Table 8-1230. H3A_VFV_CFG4

Address Offset	0x0000 0074		
Physical Address	0x5201 1474	**Instance**	ISS_H3A
Description	Vertical focus value configuration 4.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VTHR2																RESERVED								VCOEF2_4							

Bits	Field Name	Description	Type	Reset
31:16	VTHR2	Threshold for vertical FV FIR 2	RW	0x0000
15:8	RESERVED		R	0x00
7:0	VCOEF2_4	Vertical FV FIR 2 coefficient 4	RW	0x00

Table 8-1231. Register Call Summary for Register H3A_VFV_CFG4

ISS ISP

- ISS ISP H3A Autofocus Engine: [0] [1] [2]
- ISS ISP H3A Hardware Setup/Initialization: [3]
- ISS H3A Register Summary: [4]

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Table 8-1232. H3A_HVF_THR

Address Offset	0x0000 0078		
Physical Address	0x5201 1478	**Instance**	ISS_H3A
Description	Horizontal Focus Value Threshold		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HTHR2																HTHR1															

Bits	Field Name	Description	Type	Reset
31:16	HTHR2	Threshold for horizontal FV IIR 2	RW	0x0000
15:0	HTHR1	Threshold for horizontal FV IIR 1	RW	0x0000

Table 8-1233. Register Call Summary for Register H3A_HVF_THR

ISS ISP

- ISS ISP H3A Autofocus Engine: [0] [1]
- ISS ISP H3A Hardware Setup/Initialization: [2] [3]
- ISS H3A Register Summary: [4]

Table 8-1234. H3A_ADVANCED

Address Offset	0x0000 007C		
Physical Address	0x5201 147C	**Instance**	ISS_H3A
Description	Normal and Advanced AF stats collection mode		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																RESERVED															AF_MODE

Bits	Field Name	Description	Type	Reset
31:15	ID	0x0: This bit field must be set to 0xCA00 to enable AF advanced mode.	RW	0x00000
14:1	RESERVED		R	0x0000
0	AF_MODE	AF engine mode. 0x0: Normal Mode 0x1: Advanced mode. H3A_ADVANCED.ID must be set to 0xCA00 to enable this functionality.	RW	0

Table 8-1235. Register Call Summary for Register H3A_ADVANCED

ISS ISP

- ISS ISP H3A Autofocus Engine: [0] [1]
- ISS H3A Register Summary: [2]
- ISS H3A Register Description: [3]

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8.4 ISS Still Image Coprocessor

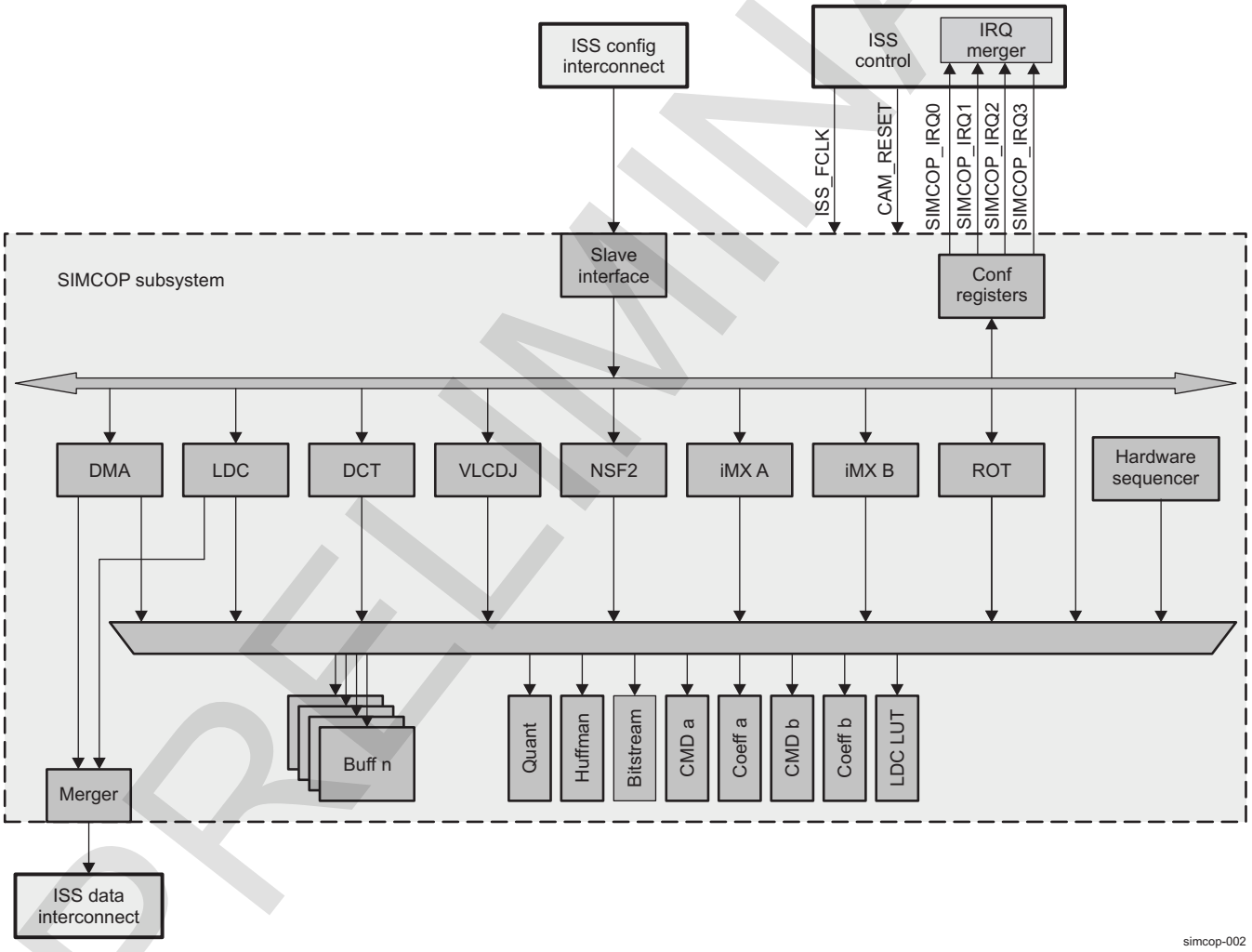
This section gives a high-level description of the ISS still iMage coprocessor (SIMCOP) in the device. For a high-level description of ISS level, see Section 8.1, *ISS:Overview*.

8.4.1 ISS SIMCOP Overview

The SIMCOP subsystem is designed to encode, decode, and process image data. The SIMCOP is a macroblock-based memory-to-memory processing engine. It fetches macroblocks from system memory and stores them into local memories. Different accelerators take the fetched data, perform processing, and send the processing outcome back to local memories. From there the data could be further processed by other accelerators or be sent back to system memory. The SIMCOP needs an external central processing unit (CPU) to perform high-level control tasks and configurations. The SIMCOP is closely coupled to a CPU for that purpose.

Figure 8-243 shows a block diagram of the SIMCOP subsystem.

Figure 8-243. SIMCOP Subsystem Overview



The ISS SIMCOP subsystem consists of:

- Noise filter (NSF2) for advanced noise filtering and an edge-enhancement
- Two image and video processing engines (iMXs) supplement various fixed-function processing blocks
- Variable-length coder/decoder for JPEG (VLCDJ) module handles quantization and variable length coding, decoding and inverse quantization
- Discrete cosine transform (DCT) module implements method in the compression flow to transform

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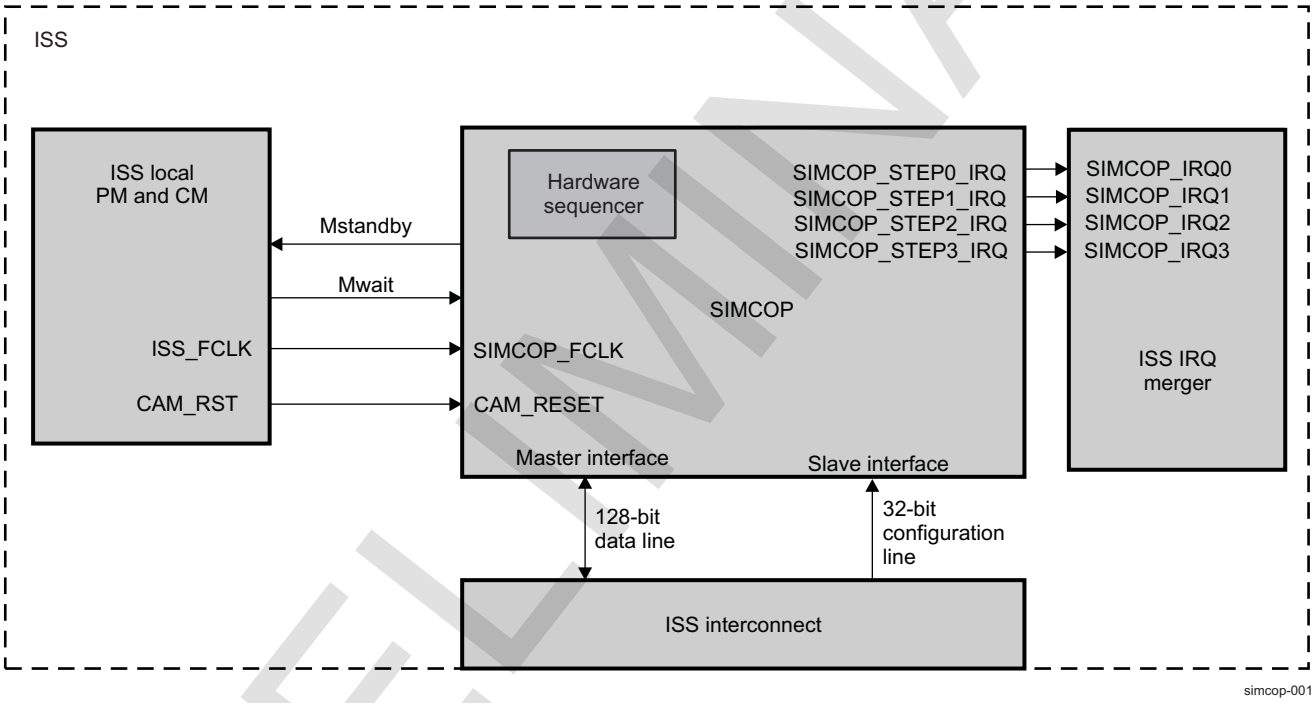
blocks of image

- Lens distortion correction (LDC) module deals with lens geometric distortion issues in the camera subsystem
- Rotation accelerator (ROT) engine blocks data rotation and shifting from a SIMCOP local memory to another SIMCOP local memory
- Hardware sequencer and buffers control SIMCOP modules/buffers to offload an external processor to perform low-level sequencing tasks
- Direct memory access (DMA) controller data transfers from SIMCOP memories to system memory or from system memory to SIMCOP memories

8.4.1.1 ISS SIMCOP Integration

The SIMCOP subsystem is connected to the rest of the system through the ISS local interconnect. Figure 8-244 shows the integration of the SIMCOP subsystem in the ISS.

Figure 8-244. SIMCOP Integration



NOTE: For more information about the IDLE hardware handshake and the wake-up request, see Section 3.1.1.1, *Clock Management*, in Chapter 3 , *Power, Reset, and Clock Management*.

This section gives an overview of typical uses of the module. See Chapter 3, *Power, Reset, and Clock Management*, for more information and settings of the PRCM relationship to ISS clocks and resets.

Table 8-1236 lists the integration attributes.

Table 8-1236. Integration Attributes

Module Instance	Attributes	
	Power Domain	Interconnect
SIMCOP	PD_CAM	

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Table 8-1237 lists the clocks and resets values.

Table 8-1237. Clocks and Resets

Clocks				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
SIMCOP	SIMCOP_FCLK	ISS_FCLK	PRCM	Functional clock provided by ISS_CLK from the PRCM module. It is used by all ISS submodules and ISS top-level resources.
Resets				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
SIMCOP	CAM_RESET	CAM_RST	PRCM	ISS and SIMCOP global reset

Table 8-1238 lists the hardware resets.

Table 8-1238. Hardware Requests

Interrupt Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
SIMCOP	SIMCOP_STEP 0_IRQ	SIMCOP_IRQ0	SIMCOP IRQ merger	Event triggered when a SIMCOP context is activated by the hardware sequencer
SIMCOP	SIMCOP_STEP 1_IRQ	SIMCOP_IRQ1	SIMCOP IRQ merger	Event triggered when a SIMCOP context is activated by the hardware sequencer
SIMCOP	SIMCOP_STEP 2_IRQ	SIMCOP_IRQ2	SIMCOP IRQ merger	Event triggered when a SIMCOP context is activated by the hardware sequencer
SIMCOP	SIMCOP_STEP 3_IRQ	SIMCOP_IRQ3	SIMCOP IRQ merger	Event triggered when a SIMCOP context is activated by the hardware sequencer

For more information about interrupt requests, see Section 8.4.1.2.3, *Interrupt Merger*.

8.4.1.2 ISS SIMCOP Functional Description

8.4.1.2.1 ISS SIMCOP Local Power and Clock Management

8.4.1.2.1.1 ISS SIMCOP Local Clock Management

ISS has five asynchronous clock domains. The SIMCOP belongs to the ISS_FCLK clock domain.

An externally provided clock-enable signal is used. Multiple subdomains exist internally to reduce dynamic power consumption. This feature does not require intervention by the PRCM module. For high-level description of the SIMCOP clock domain and configuration inside ISS, see Section 8.1.2.2, *ISS Clocks*.

Moreover, at high level the functional clock of ISS SIMCOP submodules can be cut by software to reduce power consumption by cutting off or turning on the modules from the SIMCOP_CLKCTRL register (see Table 8-1239).

When software wants to enable a submodule:

- Software sets the adequate bit in the SIMCOP_CLKCTRL register.
- Hardware enables the submodule functional and interface clocks.
- Hardware connects the configuration port of the submodule to the coprocessor bus.
- Hardware sets the appropriate bit in the SIMCOP_CLKCTRL register. Software must check if this bit is set before accessing the submodule.

Table 8-1239 lists the ISS SIMCOP clock control register settings.

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Table 8-1239. ISS SIMCOP Clock Control Register Settings

Module Name	Bit Field Name	Description
ROT	SIMCOP_CLKCTRL[7] ROT_A	Writing 0x1 enables the module
iMX B	SIMCOP_CLKCTRL[6] IMX_B	Writing 0x1 enables the module
iMX A	SIMCOP_CLKCTRL[5] IMX_A	Writing 0x1 enables the module
NSF2	SIMCOP_CLKCTRL[4] NSF2	Writing 0x1 enables the module
VLCDJ	SIMCOP_CLKCTRL[3] VLCDJ	Writing 0x1 enables the module
DCT	SIMCOP_CLKCTRL[2] DCT	Writing 0x1 enables the module
LDC	SIMCOP_CLKCTRL[1] LDC	Writing 0x1 enables the module
DMA	SIMCOP_CLKCTRL[0] DMA	Writing 0x1 enables the module

When software wants to shutdown a submodule:

- Software ensures that the submodule is idle. Mainly:
  - The submodule must not generate new events.
  - The submodule must not have any pending events.
  - For initiators: the submodule must stop interconnect transaction generation.
- Software clears the appropriate bit in the SIMCOP_CLKCTRL register.
- Hardware disconnects the configuration port of the module from the coprocessor bus: no more accesses are routed to the submodule. Ongoing transactions are finished (hardware stays in this state as long as required).
- For initiators: hardware waits until there are no more outstanding transactions:
  - SIMCOP DMA provides an MStandBy signal for that purpose.
  - The LDC does not provide this information. Software must ensure that the LDC is idle. SIMCOP hardware ensures that the internal MTC2OCP bridges have no outstanding transactions.
- Hardware cuts the submodules clock.
- Hardware clears the appropriate SIMCOP_CLKCTRL registers.

SIMCOP submodules support autogating. They can gate their functional and interface clock internally based on functional requirements. This feature could be disabled for debug or power consumption measurement purposes.

8.4.1.2.1.2 Local Clock Autogating

The SIMCOP subsystem modules support autogating. They can gate their functional and interface clock internally based on functional requirements. This feature can be disabled. Table 8-1240 summarizes which modules support autogating control and which control bit is used.

Table 8-1240. Autoclock Gating Bit Control

SIMCOP Resource	Autogating Override
SIMCOP top-level resources	N/A
SIMCOP DMA	N/A
LDC	N/A
DCT	DCT_CFG[5] AUTOGATING
VLCDJ	VLCDJ_CTRL[3] AUTOGATING
NSF2	N/A
iMX A	iMXa.IMX_CLKCNTRL[0] CLKCNTRL
iMX B	iMXb.IMX_CLKCNTRL[0] CLKCNTRL
ROT	ROT_CFG[9] AUTOGATING

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8.4.1.2.1.3 ISS SIMCOP Power Management

The SIMCOP supports the STANDBY power-management protocol. It is used by the SIMCOP to indicate when it has no more interconnect transactions to perform. This information is used at ISS level to control the SIMCOP and ISS shut-down sequence. The SIMCOP does not have any internal wake-up events. DISCONNECT and IDLE protocols are not supported.

The typical SIMCOP shut-down sequence is:

1. Software disables all SIMCOP submodules. This ensures the SIMCOP does not:
   (a) Generate any traffic on its master port: SIMCOP asserts the MStandby signal.
   (b) Generate new events (IRQs).
2. Software clears all pending events at SIMCOP level: All interrupt lines become inactive.
3. Software initiates the SIMCOP shut-down sequence by writing the appropriate bit at ISS level.
4. ISS hardware:
   (a) Disconnects the SIMCOP configuration port. Any access attempts to SIMCOP are blocked at ISS level. The DISCONNECT protocol is handled at ISS level: SIMCOP does not provide any handshake signals to support it.
   (b) Waits until MStandby from SIMCOP is asserted (always true in a normal case because SIMCOP submodules are inactive)
   (c) Asserts the SWait input of SIMCOP
   (d) Cuts the SIMCOP clock

The typical SIMCOP enable sequence is:

1. Software initiates the SIMCOP enable sequence by writing the appropriate bit at ISS level.
2. ISS hardware:
   (a) Enables the SIMCOP clock
   (b) Deasserts the SWait input of the SIMCOP
   (c) Connects the SIMCOP configuration port

Three modes for MStandBy control are supported. The mode is selected using the SIMCOP_HL_SYSCONFIG[5:4] STANDBYMODE bit field.

- Smart-standby: This is the normal mode to be used. When in this mode, the SIMCOP asserts the MStandBy signal when the MStandBy output of SIMCOP DMA is asserted, the LDC is effectively disabled (SIMCOP_CLKCTRL[1] LDC =0), and the MTCR2OCP bridge and the merger have no more outstanding transactions.
- Force-standby: This is a backup mode intended to be used only if smart-idle mode is bugged. When in this mode, the SIMCOP asserts MStandBy unconditionally. Software must ensure that the SIMCOP is in a correct quiet state before programming this mode.
- No-standby: This is a backup mode intended to be used only if smart-idle mode is bugged. When in this mode, the SIMCOP never asserts the MStandBy signal.

8.4.1.2.2 Software Reset

Software reset is intended to return the SIMCOP into a known state without requiring a complete device reset. A software reset at SIMCOP level is seen as a hardware reset for SIMCOP submodules. To perform a software reset, sets the SIMCOP_HL_SYSCONFIG[0] SOFTRESET bit to 1. The SIMCOP_HL_SYSCONFIG[0] SOFTRESET bit indicates that the software reset is ongoing when its value is 1. When the software reset completes, the SIMCOP_HL_SYSCONFIG[1] SOFTRESET bit is automatically reset. Software must ensure that the software reset completes before configuring the hardware sequencer or buffers.

8.4.1.2.3 Interrupt Merger

SIMCOP interrupts are merged at the SIMCOP subsystem level into four interrupts, as shown in Figure 8-245.

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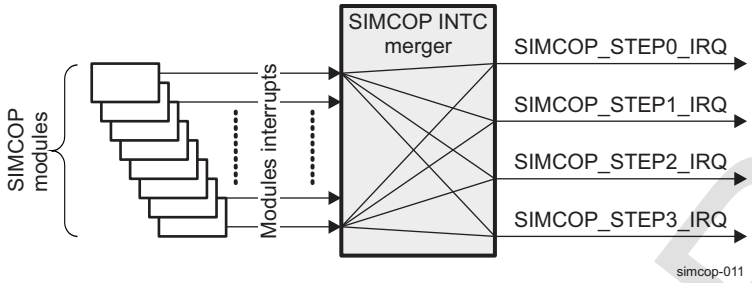
Figure 8-245. SIMCOP Interrupt Merger Overview



These four outputs interrupts can be configured through SIMCOP_HL_IRQENABLE_SET_i and SIMCOP_HL_IRQENABLE_CLR_i (where i = 0 to 3, corresponding to output interrupt) to enable or disable interrupt mask for each interrupt output. Software can poll the value of interrupt before masking (SIMCOP_HL_IRQSTATUS_RAW_i) and after masking (SIMCOP_HL_IRQSTATUS_i).

Software can configure how outputs interrupts are generated through SIMCOP_CTRL[i] IRQi_MODE (where i = 0 to 3):

- 0x0: OR, the interrupt is asserted when one of the selected events has occurred
- 0x1: AND, the interrupt is asserted when all selected events have occurred

Table 8-1241 shows how interrupts are mapped on the SIMCOP_HL_IRQSTATUS_RAW_i, SIMCOP_HL_IRQSTATUS_i, SIMCOP_HL_IRQENABLE_SET_i, and SIMCOP_HL_IRQENABLE_CLR_i registers.

Table 8-1241. SIMCOP Interrupts

Bit	Name	Description
0	SIMCOP_DMA_IRQ0	Interrupt triggered by SIMCOP DMA
1	LDC_FRAME_IRQ	A full frame has been processed by LDC2
2	DCT_IRQ	DCT operation has been completed (configured number of MCUs for YUV4:2:0/4:2:2 mode, or number of blocks for sequential block mode).
3	VLCDJ_BLOCK_IRQ	A macroblock has been processed (encode/decode).
4	NSF_IRQ	Event triggered by the NSF2 imaging accelerator when processing of a block is done
5	IMX_A_IRQ	Event triggered when iMX has executed a SLEEP instruction
6	IMX_B_IRQ	
7	ROT_A_IRQ	Event triggered by the ROT engine
8	RESERVED	Reserved
9	LDC_BLOCK_IRQ	A macroblock has been processed by LDC2.
10	SIMCOP_STEP0_IRQ	Event triggered when a SIMCOP context is activated by the hardware sequencer
11	SIMCOP_STEP1_IRQ	
12	SIMCOP_STEP2_IRQ	
13	SIMCOP_STEP3_IRQ	
14	DONE_IRQ	Event triggered when the hardware sequencer finishes the sequence: - the sequence step counter has reached the limit - All accelerator and DMA events for the last sequence step have been received.
15	VLCDJ_DECODE_ERR_IRQ	A decode error has been signaled by the VLCDJ
16	ICNT_ERR_IRQ	An error has been received on the SIMCOP master port on the L3 interconnect.
17	LDC2BRIDGE_ERR_IRQ	The LDC2 bridge has generated an error. This event must not trigger in a normal use case.
18	SIMCOP_DMA_IRQ1	Interrupt triggered by SIMCOP DMA
19	CPU_PROC_START_IRQ	This interrupt is used when CPU data processing is used in a macroblock processing pipeline. When the CPU receives this IRQ, data is ready to be processed. When CPU is done with processing it acknowledges by setting the SIMCOP_HWSEQ_CTRL.CPU_PROC_DONE bit. The interrupt is cleared as usual.

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8.4.1.2.4 ISS SIMCOP Modules Description

This section gives links to each subsection for each submodule in the ISS SIMCOP module.

The ISS module provides unique ISS_FCLK for all the submodules inside the SIMCOP (see Section 8.4.1.2.1.1, *ISS SIMCOP Local Clock Management*).

For information about hardware and software resets for each module see Table 8-1241.

For interrupt request information for each module, see Section 8.4.1.2.3, *Interrupt Merger*.

ISS SIMCOP consists of the following submodules:

- Hardware sequencer and buffers, for more information seeSection 8.4.2, *ISS SIMCOP Hardware Sequencer and Buffers*.
- DMA, for more information, see Section 8.4.3, *ISS SIMCOP DMA Module*.
- ROT, for more information, see Section 8.4.7, *ISS SIMCOP Rotation Accelerator (ROT) Module*.
- iMX
- NSF2
- VLCDJ, for more information, see Section 8.4.6, *ISS SIMCOP Variable Length Coder/Decoder for JPEG (VLCDJ) Module*.
- DCT, for more information, see Section 8.4.5, *ISS SIMCOP Discrete Cosine Transform (DCT) Module*.
- LDC, for more information, see Section 8.4.4, *ISS SIMCOP LDC Module*.

8.4.1.3 ISS SIMCOP Programming Models

8.4.1.3.1 Global Initialization

8.4.1.3.1.1 Surrounding Modules Global Initialization

This section identifies the requirements of initializing the surrounding modules when the ISS SIMCOP module is to be used for the first time after a device reset. This initialization of surrounding modules is based on the integration of the ISS SIMCOP.

Table 8-1242. Global Initialization of Surrounding Modules

Surrounding Modules	Comments
ISS local PM and CM	Module interface and functional clocks must be enabled. For more information, see Section 8.4.1.2.1, *ISS SIMCOP Local Power and Clock Management*.

8.4.1.3.1.2 ISS SIMCOP Module Global Initialization

This procedure initializes the ISS SIMCOP module after a power on or software reset.

Table 8-1243. ISS SIMCOP Global Initialization

Step	Register/Bit Field/Programming Model	Value
Execute software reset.	SIMCOP_HL_SYSCONFIG[0] SOFTRESET	0x1
Wait until reset completed?	SIMCOP_HL_SYSCONFIG[0] SOFTRESET	0x0
Configure STANDBYMODE.	SIMCOP_HL_SYSCONFIG[5:4] STANDBYMODE	0x2
Configure submodules interface and functional clock.	SIMCOP_CLKCTRL[7:0]	xxx
Interrupt configuration		
Set interrupt enable bit for the submodules.	SIMCOP_HL_IRQENABLE_SET_i[7:0]	xxx

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8.4.1.3.2 ISS SIMCOP Operational Modes Configuration

8.4.1.3.2.1 Interrupts

To unmask an interrupt for generation of SIMCOP_IRQi output interrupts, software must set the corresponding bit of SIMCOP_HL_IRQENABLE_SET_i (where i = 0 to 3) to 1.

Example 1, SIMCOP_IRQ1 is generated when DCT_IRQ or VLCDJ_BLOCK_IRQ are generated:

- SIMCOP_HL_IRQENABLE_SET_i[2] DCT_IRQ = 0x1 (where i = 1)
- SIMCOP_HL_IRQENABLE_SET_i[3] VLCDJ_BLOCK_IRQ = 0x1 (where i = 1)
- SIMCOP_CTRL[1] IRQ1_MODE = 0x0

Example 2, SIMCOP_IRQ3 is generated when IMX_A_IRQ and LDC_BLOCK_IRQ are generated:

- SIMCOP_HL_IRQENABLE_SET_i[5] IMX_A_IRQ = 0x1 (where i = 3)
- SIMCOP_HL_IRQENABLE_SET_i[9] LDC_BLOCK_IRQ = 0x1 (where i = 3)
- SIMCOP_CTRL[3] IRQ3_MODE = 0x1

To mask an interrupt for generation of SIMCOP_IRQi output interrupts, software must clear the corresponding bit of SIMCOP_HL_IRQENABLE_CLEAR_i (where i = 0 to 3) to 0.

When an event occurs, the corresponding bit in the SIMCOP_HL_IRQSTATUS_RAW_i (where i = 0 to 3) register is set regardless if the event has been enabled or not. Bits in the SIMCOP_HL_IRQSTATUS_i (where i = 0 to 3) registers are only set when an enabled event occurs. Software can clear a pending event by setting the adequate bit in the SIMCOP_HL_IRQSTATUS_i (where i = 0 to 3) register.

8.4.1.3.2.2 JPEG Encode Operational Mode Configuration

Figure 8-246 shows a typical JPEG encode macroblock pipeline.

Figure 8-246. JPEG Encode Pipeline

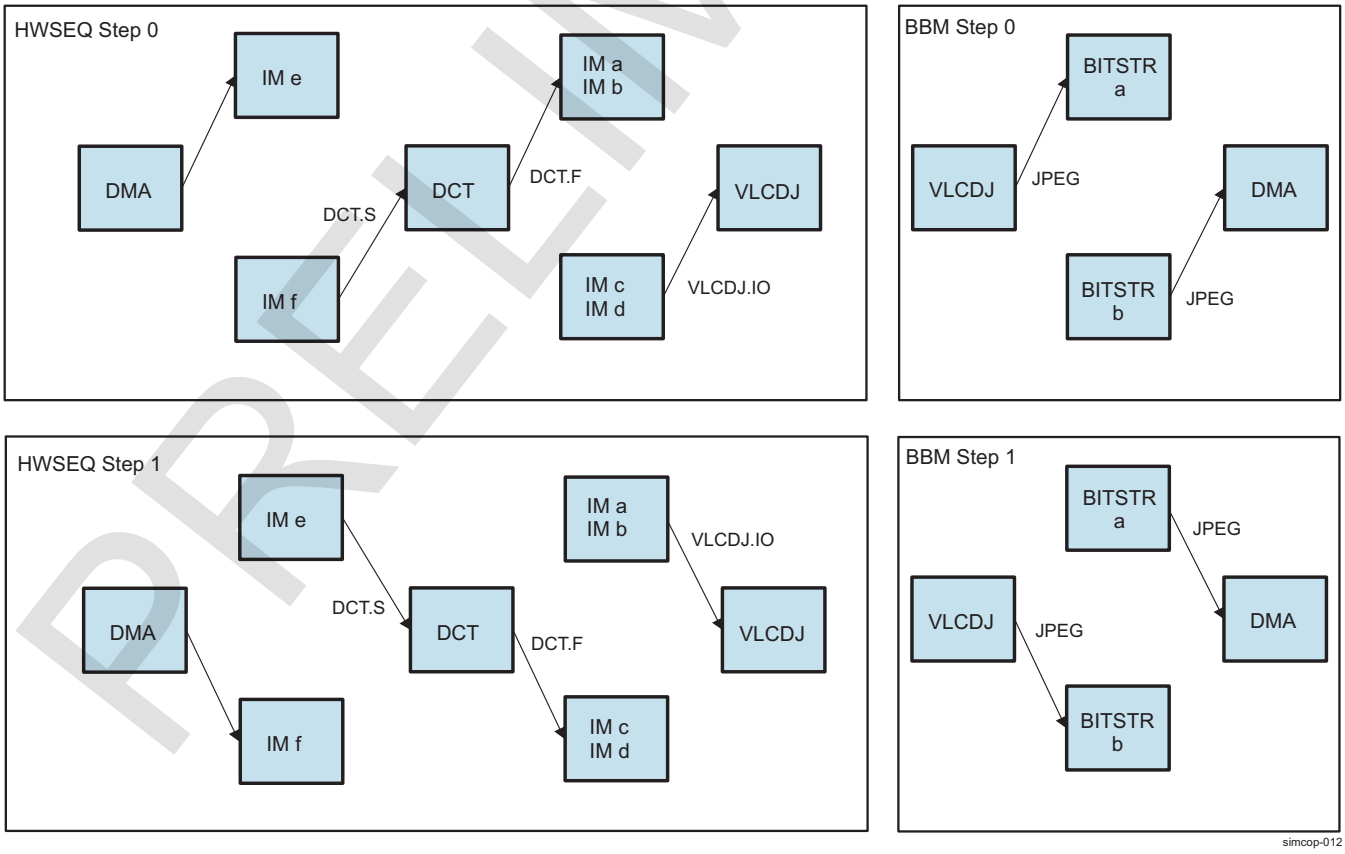

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Table 8-1244. JPEG Encode Pipeline

Step	Register/Bit Field/Programming Model	Value
Set SIMCOP DMA to fetch data from SDRAM and stored into an image buffer (IM e or IM f).	See DMA programming model Section 8.4.3.4	xxx
Set DCT to reads data from an image buffer (IM e or IM f).	DCT_SPTR[12:5] ADDR	xxx
Set DCT to store data into sets of two image buffers (IM a + IM b or IM c + IM d).	DCT_FPTR[12:4] ADDR	xxx
Set VLCDJ to read data from image buffers.	See VLCDJ programming model Section 8.4.6.4	xxx
Set VLCDJ to write the data to the bitstream buffer.	See VLCDJ programming model Section 8.4.6.4	xxx
Set the SIMCOP DMA to send the data to SDRAM.	See DMA programming model Section 8.4.3.4	xxx

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8.4.1.4 ISS SIMCOP Register Manual

8.4.1.4.1 SIMCOP Instance Summary

Table 8-1245 is the SIMCOP top level instance summary.

Table 8-1245. SIMCOP Instance Summary

Module Name	Base Address L3 Interconnect	Base Address Cortex-M3 Private Access	Size
SIMCOP_CONTROL	0x5202 0000	0x5506 0000	256 bytes

NOTE: Private Access is an access that does not use the L3/L4 interconnects.

8.4.1.4.2 SIMCOP Registers

8.4.1.4.2.1 SIMCOP Register Summary

Table 8-1246 is the SIMCOP_CONTROL register mapping summary.

Table 8-1246. SIMCOP_CONTROL Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	Physical Address L3 Interconnect	Physical Address Cortex-M3 Private Access
SIMCOP_HL_REVISION	R	32	0x0000 0000	0x5202 0000	0x5506 0000
SIMCOP_HL_HWINFO	R	32	0x0000 0004	0x5202 0004	0x5506 0004
SIMCOP_HL_SYSCONFIG	RW	32	0x0000 0010	0x5202 0010	0x5506 0010
RESERVED	RW	32	0x0000 001C	0x5202 001C	0x5506 001C
SIMCOP_HL_IRQSTATUS_RAW_i (1)	RW	32	0x0000 0020 + (0x10 * i)	0x5202 0020 + (0x10 * i)	0x5506 0020 + (0x10 * i)
SIMCOP_HL_IRQSTATUS_i (1)	RW	32	0x0000 0024 + (0x10 * i)	0x5202 0024 + (0x10 * i)	0x5506 0024 + (0x10 * i)
SIMCOP_HL_IRQENABLE_SET_i (1)	RW	32	0x0000 0028 + (0x10 * i)	0x5202 0028 + (0x10 * i)	0x5506 0028 + (0x10 * i)
SIMCOP_HL_IRQENABLE_CLR_i (1)	RW	32	0x0000 002C + (0x10 * i)	0x5202 002C + (0x10 * i)	0x5506 002C + (0x10 * i)
SIMCOP_CTRL	RW	32	0x0000 0060	0x5202 0060	0x5506 0060
SIMCOP_CLKCTRL	RW	32	0x0000 0064	0x5202 0064	0x5506 0064

(1) i = 0 to 3

8.4.1.4.2.2 SIMCOP_CONTROL Register Descriptions

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Table 8-1247. SIMCOP_HL_REVISION

Address Offset	0x0000 0000		
Physical Address	0x5202 0000 0x5506 0000	**Instance**	SIMCOP_CONTROL_L3 SIMCOP_CONTROL_CORTEX-M3
Description	MODULE REVISION This register contains the IP revision code in binary coded digital. For example, we have: 0x01 = revision 0.1 and 0x21 = revision 2.1		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REV																															

Bits	Field Name	Description	Type	Reset
31:0	REV	Revision ID	R	-(1)

(1) TI internal data

Table 8-1248. Register Call Summary for Register SIMCOP_HL_REVISION

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- ISS SIMCOP Register Manual: [0]

Table 8-1249. SIMCOP_HL_HWINFO

Address Offset	0x0000 0004		
Physical Address	0x5202 0004 0x5506 0004	**Instance**	SIMCOP_CONTROL_L3 SIMCOP_CONTROL_CORTEX-M3
Description	Information about the IP module's hardware configuration. It provides information about the generic parameters.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				LDCR_RESP_FIFO		IMAGE_BUFFERS		RESERVED	ROT_A_ENABLE	IMX_B_ENABLE	IMX_A_ENABLE	NSF_ENABLE	VLCDJ_ENABLE	DCT_ENABLE	LDC_ENABLE

Bits	Field Name	Description	Type	Reset
31:13	RESERVED	Read returns 0.	R	0x00000
12:10	LDCR_RESP_FIFO	Defines the size of the LDC read master response FIFO in words of 128-bits. Read 0x2: 8x128 bits Read 0x3: 16x128 bits Read 0x4: 32x128 bits Read 0x5: 64x128 bits Read 0x6: 128x128 bits Read 0x7: 256x256 bits	R	0x4
9:8	IMAGE_BUFFERS	This parameter defines the image buffer count. Read 0x0: 4 Image buffers (e, f, g, h) Read 0x1: 8 Image buffers	R	0x1
7	RESERVED	Read returns 0.	R	0

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Bits	Field Name	Description	Type	Reset
6	ROT_A_ENABLE	The ROT a is present when this parameter is set. Read 0x0: Disabled at design time Read 0x1: Enabled at design time	R	1
5	IMX_B_ENABLE	The iMX B module and the CMD b, COEFF b memories are present when this parameter is set. Read 0x0: Disabled at design time Read 0x1: Enabled at design time	R	1
4	IMX_A_ENABLE	The iMX A module and the CMD a, COEFF a memories are present when this parameter is set. Read 0x0: Disabled at design time Read 0x1: Enabled at design time	R	1
3	NSF_ENABLE	The NSF2 is present when this parameter is set. Read 0x0: Disabled at design time Read 0x1: Enabled at design time	R	1
2	VLCDJ_ENABLE	The VLCD module and the QUANT, HUFFMAN, BITSTREAM memories are present when this parameter is set. Read 0x0: Disabled at design time Read 0x1: Enabled at design time	R	1
1	DCT_ENABLE	The DCT module is present when this parameter is set. Read 0x0: Disabled at design time Read 0x1: Enabled at design time	R	1
0	LDC_ENABLE	The LDC module and the LDC LUT are present when this parameter is set. Read 0x0: Disabled at design time Read 0x1: Enabled at design time	R	1

Table 8-1250. Register Call Summary for Register SIMCOP_HL_HWINFO

ISS Still Image Coprocessor

- ISS SIMCOP Register Manual: [0]

Table 8-1251. SIMCOP_HL_SYSCONFIG

Address Offset	0x0000 0010		
Physical Address	0x5202 0010 0x5506 0010	**Instance**	SIMCOP_CONTROL_L3 SIMCOP_CONTROL_CORTEX-M3
Description	This register controls the various parameters of the OCP interface		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																										STANDBYMODE		RESERVED			SOFTRESET

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Bits	Field Name	Description	Type	Reset
31:6	RESERVED	Read returns 0.	R	0x0000000
5:4	STANDBYMODE	Configuration of the local initiator state management mode. By definition, initiator may generate read/write transaction as long as it is out of STANDBY state. 0x0: Force-standby mode: local initiator is unconditionally placed in standby state. Backup mode, for debug only. 0x1: No-standby mode: local initiator is unconditionally placed out of standby state. Backup mode, for debug only. 0x2: Smart-standby mode: local initiator standby status depends on local conditions, that is, the module's functional requirement from the initiator.	RW	0x0
3:1	RESERVED	Read returns 0.	R	0x0
0	SOFTRESET	Software reset Read 0x0: Reset done, no pending action Write 0x0: No action Write 0x1: Initiate software reset Read 0x1: Reset (software or other) ongoing	RW	0

Table 8-1252. Register Call Summary for Register SIMCOP_HL_SYSCONFIG

ISS Still Image Coprocessor

- ISS SIMCOP Functional Description: [0] [1] [2] [3]
- ISS SIMCOP Programming Models: [4] [5] [6]
- ISS SIMCOP Register Manual: [7]

Table 8-1253. SIMCOP_HL_IRQSTATUS_RAW_i

Address Offset	0x0000 0020 + (0x10 * i)		
Physical Address	0x5202 0020 + (0x10 * i) 0x5506 0020 + (0x10 * i)	**Instance**	SIMCOP_CONTROL_L3 SIMCOP_CONTROL_CORTEX-M3
Description	Per-event raw interrupt status vector Raw status is set even if event is not enabled. Write 1 to set the (raw) status, mostly for debug.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												CPU_PROC_START_IRQ	SIMCOP_DMA_IRQ1	LDC2BRIDGE_ERR_IRQ	ICNT_ERR_IRQ	VLCDJ_DECODE_ERR_IRQ	DONE_IRQ	STEP3_IRQ	STEP2_IRQ	STEP1_IRQ	STEP0_IRQ	LDC_BLOCK_IRQ	RESERVED	ROT_A	IMX_B_IRQ	IMX_A_IRQ	NSF_IRQ_IRQ	VLCDJ_BLOC_IRQ	DCT_IRQ	LDC_FRAME_IRQ	SIMCOP_DMA_IRQ0

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Bits	Field Name	Description	Type	Reset
31:20	RESERVED	Read returns 0.	R	0x000
19	CPU_PROC_START_IRQ	Event triggered by the hardware sequencer to instruct the CPU to process a macroblock Write 0x0: No action Read 0x0: No event pending Read 0x1: Event pending Write 0x1: Set event (debug)	RW W1toSet	0
18	SIMCOP_DMA_IRQ1	Event triggered by the SIMCOP DMA. This event is automatically cleared at SIMCOP level when it is cleared at SIMCOP DMA level. Check SIMCOP DMA IRQ registers. Read 0x0: No event pending Read 0x1: Event pending	R	0
17	LDC2BRIDGE_ERR_IRQ	The LDC2 bridge has generated an error. Write 0x0: No action Read 0x0: No event pending Read 0x1: Event pending Write 0x1: Set event (debug)	RW W1toSet	0
16	ICNT_ERR_IRQ	An error has been received on the SIMCOP master port. Write 0x0: No action Read 0x0: No event pending Read 0x1: Event pending Write 0x1: Set event (debug)	RW W1toSet	0
15	VLCDJ_DECODE_ERR_IRQ	A decode error has been signaled by the VLCDJ module Write 0x0: No action Read 0x0: No event pending Read 0x1: Event pending Write 0x1: Set event (debug)	RW W1toSet	0
14	DONE_IRQ	Event triggered when the hardware sequencer finishes the sequence: - the sequence step counter has reached the limit - all accelerator and DMA events for the last sequence step have been received. Write 0x0: No action Read 0x0: No event pending Read 0x1: Event pending Write 0x1: Set event (debug)	RW W1toSet	0
13	STEP3_IRQ	Event triggered when Step 3 is activated by the hardware sequencer Write 0x0: No action Read 0x0: No event pending Read 0x1: Event pending Write 0x1: Set event (debug)	RW W1toSet	0
12	STEP2_IRQ	Event triggered when Step 2 is activated by the hardware sequencer Write 0x0: No action Read 0x0: No event pending Read 0x1: Event pending Write 0x1: Set event (debug)	RW W1toSet	0

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Bits	Field Name	Description	Type	Reset
11	STEP1_IRQ	Event triggered when Step 1 is activated by the hardware sequencer Write 0x0: No action Read 0x0: No event pending Read 0x1: Event pending Write 0x1: Set event (debug)	RW W1toSet	0
10	STEP0_IRQ	Event triggered when Step 0 is activated by the hardware sequencer Write 0x0: No action Read 0x0: No event pending Read 0x1: Event pending Write 0x1: Set event (debug)	RW W1toSet	0
9	LDC_BLOCK_IRQ	This event is triggered by LDC when a macroblock has been processed Write 0x0: No action Read 0x0: No event pending Read 0x1: Event pending Write 0x1: Set event (debug)	RW W1toSet	0
8	RESERVED	Read returns 0.	R	0
7	ROT_A	Event triggered by the ROT a engine Write 0x0: No action Read 0x0: No event pending Read 0x1: Event pending Write 0x1: Set event (debug)	RW W1toSet	0
6	IMX_B_IRQ	Event triggered when iMX has executed a SLEEP instruction. Write 0x0: No action Read 0x0: No event pending Read 0x1: Event pending Write 0x1: Set event (debug)	RW W1toSet	0
5	IMX_A_IRQ	Event triggered when iMX has executed a SLEEP instruction. Write 0x0: No action Read 0x0: No event pending Read 0x1: Event pending Write 0x1: Set event (debug)	RW W1toSet	0
4	NSF_IRQ_IRQ	Event triggered by the NSF2 imaging accelerator when processing of a block is done. Write 0x0: No action Read 0x0: No event pending Read 0x1: Event pending Write 0x1: Set event (debug)	RW W1toSet	0
3	VLCDJ_BLOC_IRQ	This event is triggered by VLCDJ when a macroblock has been processed (encode/decode) Write 0x0: No action Read 0x0: No event pending Read 0x1: Event pending Write 0x1: Set event (debug)	RW W1toSet	0

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Bits	Field Name	Description	Type	Reset
2	DCT_IRQ	Event triggered when a block has been processed by the DCT module and the filter outcome has been stored to an image buffer. Write 0x0: No action Read 0x0: No event pending Read 0x1: Event pending Write 0x1: Set event (debug)	RW W1toSet	0
1	LDC_FRAME_IRQ	This event is triggered by LDC when a full frame has been processed Write 0x0: No action Read 0x0: No event pending Read 0x1: Event pending Write 0x1: Set event (debug)	RW W1toSet	0
0	SIMCOP_DMA_IRQ0	Event triggered by the SIMCOP DMA. This event is automatically cleared at SIMCOP level when it is cleared at SIMCOP DMA level. Check SIMCOP DMA IRQ registers. Read 0x0: No event pending Read 0x1: Event pending	R	0

Table 8-1254. Register Call Summary for Register SIMCOP_HL_IRQSTATUS_RAW_i

ISS Still Image Coprocessor

- ISS SIMCOP Functional Description: [0] [1]
- ISS SIMCOP Programming Models: [2]
- ISS SIMCOP Register Manual: [3]

Table 8-1255. SIMCOP_HL_IRQSTATUS_i

Address Offset	0x0000 0024 + (0x10 * i)		
Physical Address	0x5202 0024 + (0x10 * i) 0x5506 0024 + (0x10 * i)	**Instance**	SIMCOP_CONTROL_L3 SIMCOP_CONTROL_CORTEX-M3
Description	Per-event "enabled" interrupt status vector. Enabled status is not set unless event is enabled. Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, that is, even if not enabled).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												CPU_PROC_START_IRQ	SIMCOP_DMA_IRQ1	LDC2BRIDGE_ERR_IRQ	ICNT_ERR_IRQ	VLCDJ_DECODE_ERR_IRQ	DONE_IRQ	STEP3_IRQ	STEP2_IRQ	STEP1_IRQ	STEP0_IRQ	LDC_BLOCK_IRQ	RESERVED	ROT_A	IMX_B_IRQ	IMX_A_IRQ	NSF_IRQ_IRQ	VLCDJ_BLOC_IRQ	DCT_IRQ	LDC_FRAME_IRQ	SIMCOP_DMA_IRQ0

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Bits	Field Name	Description	Type	Reset
31:20	RESERVED	Read returns 0.	R	0x000
19	CPU_PROC_START_IRQ	Event triggered by the hardware sequencer to instruct the CPU to process a macroblock Write 0x0: No action Read 0x0: No (enabled) event pending Read 0x1: Event pending Write 0x1: Clear (raw) event	RW W1toClr	0
18	SIMCOP_DMA_IRQ1	Event triggered by the SIMCOP DMA. This event is automatically cleared at SIMCOP level when it is cleared at SIMCOP DMA level. Check SIMCOP DMA IRQ registers. Read 0x0: No (enabled) event pending Read 0x1: Event pending	R	0
17	LDC2BRIDGE_ERR_IRQ	The LDC2 bridge has generated an error. Write 0x0: No action Read 0x0: No (enabled) event pending Read 0x1: Event pending Write 0x1: Clear (raw) event	RW W1toClr	0
16	ICNT_ERR_IRQ	An error has been received on the SIMCOP master port. Write 0x0: No action Read 0x0: No (enabled) event pending Read 0x1: Event pending Write 0x1: Clear (raw) event	RW W1toClr	0
15	VLCDJ_DECODE_ERR_IRQ	A decode error has been signaled by the VLCDJ module Write 0x0: No action Read 0x0: No (enabled) event pending Read 0x1: Event pending Write 0x1: Clear (raw) event	RW W1toClr	0
14	DONE_IRQ	Event triggered when the hardware sequencer finishes the sequence: -The sequence step counter has reached the limit. All accelerator and DMA events for the last sequence step have been received. Write 0x0: No action Read 0x0: No (enabled) event pending Read 0x1: Event pending Write 0x1: Clear (raw) event	RW W1toClr	0
13	STEP3_IRQ	Event triggered when Step 3 is activated by the hardware sequencer Write 0x0: No action Read 0x0: No (enabled) event pending Read 0x1: Event pending Write 0x1: Clear (raw) event	RW W1toClr	0
12	STEP2_IRQ	Event triggered when Step 2 is activated by the hardware sequencer Write 0x0: No action Read 0x0: No (enabled) event pending Read 0x1: Event pending Write 0x1: Clear (raw) event	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
11	STEP1_IRQ	Event triggered when Step 1 is activated by the hardware sequencer Write 0x0: No action Read 0x0: No (enabled) event pending Read 0x1: Event pending Write 0x1: Clear (raw) event	RW W1toClr	0
10	STEP0_IRQ	Event triggered when Step 0 is activated by the hardware sequencer Write 0x0: No action Read 0x0: No (enabled) event pending Read 0x1: Event pending Write 0x1: Clear (raw) event	RW W1toClr	0
9	LDC_BLOCK_IRQ	This event is triggered by LDC when a macroblock has been processed Write 0x0: No action Read 0x0: No (enabled) event pending Read 0x1: Event pending Write 0x1: Clear (raw) event	RW W1toClr	0
8	RESERVED	Read returns 0.	R	0
7	ROT_A	Event triggered by the ROT a engine Write 0x0: No action Read 0x0: No (enabled) event pending Read 0x1: Event pending Write 0x1: Clear (raw) event	RW W1toClr	0
6	IMX_B_IRQ	Event triggered when iMX has executed a SLEEP instruction. Write 0x0: No action Read 0x0: No (enabled) event pending Read 0x1: Event pending Write 0x1: Clear (raw) event	RW W1toClr	0
5	IMX_A_IRQ	Event triggered when iMX has executed a SLEEP instruction. Write 0x0: No action Read 0x0: No (enabled) event pending Read 0x1: Event pending Write 0x1: Clear (raw) event	RW W1toClr	0
4	NSF_IRQ_IRQ	Event triggered by the NSF2 imaging accelerator when processing of a block is done. Write 0x0: No action Read 0x0: No (enabled) event pending Read 0x1: Event pending Write 0x1: Clear (raw) event	RW W1toClr	0
3	VLCDJ_BLOC_IRQ	This event is triggered by VLCDJ when a macroblock has been processed (encode/decode) Write 0x0: No action Read 0x0: No (enabled) event pending Read 0x1: Event pending Write 0x1: Clear (raw) event	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
2	DCT_IRQ	Event triggered when a block has been processed by the DCT module and the filter outcome has been stored to an image buffer. Write 0x0: No action Read 0x0: No (enabled) event pending Read 0x1: Event pending Write 0x1: Clear (raw) event	RW W1toClr	0
1	LDC_FRAME_IRQ	This event is triggered by LDC when a full frame has been processed Write 0x0: No action Read 0x0: No (enabled) event pending Read 0x1: Event pending Write 0x1: Clear (raw) event	RW W1toClr	0
0	SIMCOP_DMA_IRQ0	Event triggered by the SIMCOP DMA. This event is automatically cleared at SIMCOP level when it is cleared at SIMCOP DMA level. Check SIMCOP DMA IRQ registers. Read 0x0: No (enabled) event pending Read 0x1: Event pending	R	0

Table 8-1256. Register Call Summary for Register SIMCOP_HL_IRQSTATUS_i

ISS Still Image Coprocessor

- ISS SIMCOP Functional Description: [0] [1]
- ISS SIMCOP Programming Models: [2] [3]
- ISS SIMCOP Register Manual: [4]

Table 8-1257. SIMCOP_HL_IRQENABLE_SET_i

Address Offset	0x0000 0028 + (0x10 * i)		
Physical Address	0x5202 0028 + (0x10 * i) 0x5506 0028 + (0x10 * i)	**Instance**	SIMCOP_CONTROL_L3 SIMCOP_CONTROL_CORTEX-M3
Description	Per-event interrupt enable bit vector. Write 1 to set (enable interrupt). Readout equal to corresponding _CLR register.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												CPU_PROC_START_IRQ	SIMCOP_DMA_IRQ1	LDC2BRIDGE_ERR_IRQ	ICNT_ERR_IRQ	VLCDJ_DECODE_ERR_IRQ	DONE_IRQ	STEP3_IRQ	STEP2_IRQ	STEP1_IRQ	STEP0_IRQ	LDC_BLOCK_IRQ	RESERVED	ROT_A	IMX_B_IRQ	IMX_A_IRQ	NSF_IRQ_IRQ	VLCDJ_BLOC_IRQ	DCT_IRQ	LDC_FRAME_IRQ	SIMCOP_DMA_IRQ0

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Bits	Field Name	Description	Type	Reset
31:20	RESERVED	Read returns 0.	R	0x000
19	CPU_PROC_START_IRQ	Event triggered by the hardware sequencer to instruct the CPU to process a macroblock Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW W1toSet	0
18	SIMCOP_DMA_IRQ1	Event triggered by the SIMCOP DMA. Check SIMCOP DMA IRQ registers. Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW W1toSet	0
17	LDC2BRIDGE_ERR_IRQ	The LDC2 bridge has generated an error. Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW W1toSet	0
16	ICNT_ERR_IRQ	An error has been received on the SIMCOP master port. Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW W1toSet	0
15	VLCDJ_DECODE_ERR_IRQ	A decode error has been signaled by the VLCDJ module Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW W1toSet	0
14	DONE_IRQ	Event triggered when the hardware sequencer finishes the sequence: The sequence step counter has reached the limit. All accelerator and DMA events for the last sequence step have been received. Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW W1toSet	0
13	STEP3_IRQ	Event triggered when Step 3 is activated by the hardware sequencer Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW W1toSet	0
12	STEP2_IRQ	Event triggered when Step 2 is activated by the hardware sequencer Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW W1toSet	0

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Bits	Field Name	Description	Type	Reset
11	STEP1_IRQ	Event triggered when Step 1 is activated by the hardware sequencer Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW W1toSet	0
10	STEP0_IRQ	Event triggered when Step 0 is activated by the hardware sequencer Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW W1toSet	0
9	LDC_BLOCK_IRQ	This event is triggered by LDC when a macroblock has been processed Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW W1toSet	0
8	RESERVED	Read returns 0.	R	0
7	ROT_A	Event triggered by the ROT a engine Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW W1toSet	0
6	IMX_B_IRQ	Event triggered when iMX has executed a SLEEP instruction. Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW W1toSet	0
5	IMX_A_IRQ	Event triggered when iMX has executed a SLEEP instruction. Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW W1toSet	0
4	NSF_IRQ_IRQ	Event triggered by the NSF2 imaging accelerator when processing of a block is done. Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW W1toSet	0
3	VLCDJ_BLOC_IRQ	This event is triggered by VLCDJ when a macroblock has been processed (encode/decode) Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW W1toSet	0

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Bits	Field Name	Description	Type	Reset
2	DCT_IRQ	Event triggered when a block has been processed by the DCT module and the filter outcome has been stored to an image buffer. Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW W1toSet	0
1	LDC_FRAME_IRQ	This event is triggered by LDC when a full frame has been processed Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW W1toSet	0
0	SIMCOP_DMA_IRQ0	Event triggered by the SIMCOP DMA. Check SIMCOP DMA IRQ registers. Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW W1toSet	0

Table 8-1258. Register Call Summary for Register SIMCOP_HL_IRQENABLE_SET_i

ISS Still Image Coprocessor

- ISS SIMCOP Functional Description: [0] [1]
- ISS SIMCOP Programming Models: [2] [3] [4] [5] [6] [7]
- ISS SIMCOP Register Manual: [8]

Table 8-1259. SIMCOP_HL_IRQENABLE_CLR_i

Address Offset	0x0000 002C + (0x10 * i)		
Physical Address	0x5202 002C + (0x10 * i) 0x5506 002C + (0x10 * i)	**Instance**	SIMCOP_CONTROL_L3 SIMCOP_CONTROL_CORTEX-M3
Description	Per-event interrupt enable bit vector. Write 1 to clear (disable interrupt). Readout equal to corresponding _SET register.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												CPU_PROC_START_IRQ	SIMCOP_DMA_IRQ1	LDC2BRIDGE_ERR_IRQ	ICNT_ERR_IRQ	VLCDJ_DECODE_ERR_IRQ	DONE_IRQ	STEP3_IRQ	STEP2_IRQ	STEP1_IRQ	STEP0_IRQ	LDC_BLOCK_IRQ	RESERVED	ROT_A	IMX_B_IRQ	IMX_A_IRQ	NSF_IRQ_IRQ	VLCDJ_BLOC_IRQ	DCT_IRQ	LDC_FRAME_IRQ	SIMCOP_DMA_IRQ0

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Bits	Field Name	Description	Type	Reset
31:20	RESERVED	Read returns 0.	R	0x000
19	CPU_PROC_START_IRQ	Event triggered by the hardware sequencer to instruct the CPU to process a macroblock Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW W1toClr	0
18	SIMCOP_DMA_IRQ1	Event triggered by the SIMCOP DMA. Check SIMCOP DMA IRQ registers. Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW W1toClr	0
17	LDC2BRIDGE_ERR_IRQ	The LDC2 bridge has generated an error. Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW W1toClr	0
16	ICNT_ERR_IRQ	An error has been received on the SIMCOP master port. Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW W1toClr	0
15	VLCDJ_DECODE_ERR_IRQ	A decode error has been signaled by the VLCDJ module Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW W1toClr	0
14	DONE_IRQ	Event triggered when the hardware sequencer finishes the sequence: The sequence step counter has reached the limit. All accelerator and DMA events for the last sequence step have been received. Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW W1toClr	0
13	STEP3_IRQ	Event triggered when Step 3 is activated by the hardware sequencer Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW W1toClr	0
12	STEP2_IRQ	Event triggered when Step 2 is activated by the hardware sequencer Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
11	STEP1_IRQ	Event triggered when Step 1 is activated by the hardware sequencer Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW W1toClr	0
10	STEP0_IRQ	Event triggered when Step 0 is activated by the hardware sequencer Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW W1toClr	0
9	LDC_BLOCK_IRQ	This event is triggered by LDC when a macroblock has been processed Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW W1toClr	0
8	RESERVED	Read returns 0.	R	0
7	ROT_A	Event triggered by the ROT a engine Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW W1toClr	0
6	IMX_B_IRQ	Event triggered when iMX has executed a SLEEP instruction. Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW W1toClr	0
5	IMX_A_IRQ	Event triggered when iMX has executed a SLEEP instruction. Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW W1toClr	0
4	NSF_IRQ_IRQ	Event triggered by the NSF2 imaging accelerator when processing of a block is done. Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW W1toClr	0
3	VLCDJ_BLOC_IRQ	This event is triggered by VLCDJ when a macroblock has been processed (encode/decode) Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
2	DCT_IRQ	Event triggered when a block has been processed by the DCT module and the filter outcome has been stored to an image buffer. Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW W1toClr	0
1	LDC_FRAME_IRQ	This event is triggered by LDC when a full frame has been processed Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW W1toClr	0
0	SIMCOP_DMA_IRQ0	Event triggered by the SIMCOP DMA. Check SIMCOP DMA IRQ registers. Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW W1toClr	0

Table 8-1260. Register Call Summary for Register SIMCOP_HL_IRQENABLE_CLR_i

ISS Still Image Coprocessor

- ISS SIMCOP Functional Description: [0] [1]
- ISS SIMCOP Register Manual: [2]

Table 8-1261. SIMCOP_CTRL

Address Offset	0x0000 0060		
Physical Address	0x5202 0060 0x5506 0060	**Instance**	SIMCOP_CONTROL_L3 SIMCOP_CONTROL_CORTEX-M3
Description	SIMCOP control register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			LDC_R_BURST_BREAK	LDC_R_MAX_BURST_LENGHT		RESERVED		LDC_R_TAG_CNT			RESERVED	LDC_R_TAG_OFST				RESERVED	IMX_B_CMD	IMX_A_CMD		HUFF	QUANT	RESERVED	LDC_LUT	LDC_INPUT		NSF_WMEM		IRQ3_MODE	IRQ2_MODE	IRQ1_MODE	IRQ0_MODE

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Bits	Field Name	Description	Type	Reset
31:29	RESERVED	Read returns 0.	R	0x0
28	LDC_R_BURST_BREAK	Controls if bursts issued by the LDC2 bridge could cross burst length boundaries. When this register is set, the LDC2 bridge only issues aligned bursts. Register can only be used when LDC_R_MAX_BURST_LENGHT is 32, 64, or 128 bytes. 0x0: Yes. 0x1: No. OCP transactions must be split	RW	0
27:26	LDC_R_MAX_BURST_LENGHT	Limits the maximum burst length that could be used by the LDC2 bridge 0x0: 8 x 128 0x1: 6 x 128 0x2: 4 x 128 0x3: 2 x 128	RW	0x0
25	RESERVED	Read returns 0.	R	0
24:21	LDC_R_TAG_CNT	Limits the maximum number of outstanding requests to LDC_R_TAG_CNT+1	RW	0x3
20	RESERVED	Read returns 0.	R	0
19:16	LDC_R_TAG_OFST	First OCP tag ID that can be used by LDC reads. Software must prevent overlap with tags generated by the SIMCOP DMA. Typically this value should be equal to SIMCP_DMA_CTRL.TAG_CNT+1.	RW	0xC
15	RESERVED	Read returns 0.	R	0
14	IMX_B_CMD	Switch for iMX # command memory 0x0: Coprocessor bus 0x1: iMX B instruction read / write	RW	0
13:12	IMX_A_CMD	Switch for iMX A command memory 0x0: Coprocessor bus 0x1: iMX A instruction read/write 0x2: iMX B instruction read/write	RW	0x0
11	HUFF	Switch for Huffman table 0x0: Coprocessor 0x1: VLCDJ Huffman table read	RW	0
10	QUANT	Switch for quantization table 0x0: Coprocessor bus 0x1: VLCDJ quantization table read	RW	0
9	RESERVED	Read returns 0.	R	0
8	LDC_LUT	Switch for LDC LUT 0x0: Coprocessor bus 0x1: The LDC module could access the LDC LUT.	RW	0
7:6	LDC_INPUT	Selects input data buffer for LDC. Memories attached to LDC as working memories cannot be used by any other accelerators. HWSEQ or HWSEQ software override settings are ignored for those memories. 0x0: No input memory attached 0x1: Use image buffers a and b 0x2: Use image buffers a, b, c, and d 0x3: Use LDC private input memory.	RW	0x0

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Bits	Field Name	Description	Type	Reset
5:4	NSF_WMEM	Selects working memory for NSF. Memories attached to NSF as working memories cannot be used by any other accelerators. HWSEQ or HWSEQ software override settings are ignored for those memories. 0x0: No working memory attached to NSF2. NSF2 cannot be used. 0x1: iMX A coefficient memory used. 0x2: Image buffers a and b used. Those image buffers cannot be used for other purposes. This setting has higher priority than the context configuration. 0x3: Image buffers a, b, c, and d used. Those image buffers cannot be used for other purposes. This setting has higher priority than the context configuration.	RW	0x0
3	IRQ3_MODE	Interrupt generation method 0x0: The interrupt line is asserted when one of the events enabled in SIMCOP_IRQENABLE_3 is pending. 0x1: The interrupt line is asserted when all events enabled in SIMCOP_IRQENABLE_3 are pending.	RW	0
2	IRQ2_MODE	Interrupt generation method 0x0: The interrupt line is asserted when one of the events enabled in SIMCOP_IRQENABLE_2 is pending. 0x1: The interrupt line is asserted when all events enabled in SIMCOP_IRQENABLE_2 are pending.	RW	0
1	IRQ1_MODE	Interrupt generation method 0x0: The interrupt line is asserted when one of the events enabled in SIMCOP_IRQENABLE_1 is pending. 0x1: The interrupt line is asserted when all events enabled in SIMCOP_IRQENABLE_1 are pending.	RW	0
0	IRQ0_MODE	Interrupt generation method 0x0: The interrupt line is asserted when one of the events enabled in SIMCOP_IRQENABLE_0 is pending. 0x1: The interrupt line is asserted when all events enabled in SIMCOP_IRQENABLE_0 are pending.	RW	0

Table 8-1262. Register Call Summary for Register SIMCOP_CTRL

ISS Still Image Coprocessor

- ISS SIMCOP Functional Description: [0]
- ISS SIMCOP Programming Models: [1] [2]
- ISS SIMCOP Register Manual: [3]

Table 8-1263. SIMCOP_CLKCTRL

Address Offset	0x0000 0064		
Physical Address	0x5202 0064 0x5506 0064	**Instance**	SIMCOP_CONTROL_L3 SIMCOP_CONTROL_CORTEX-M3
Description	SIMCOP clock control register. Use to enable/disable the interface and functional clock of SIMCOP submodules. Disabled modules cannot be accessed		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								ROT_A	IMX_B	IMX_A	NSF2	VLCDJ	DCT	LDC	DMA

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Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Read returns 0.	R	0x000000
7	ROT_A	ROT A Write 0x0: Request shutdown of the submodule. No effect if the submodule clock is already off. Read 0x0: The submodule is off Read 0x1: The submodule is on Write 0x1: Request enable of the submodule. No effect if the submodule clock is already off.	RW	0
6	IMX_B	iMX B Write 0x0: Request shutdown of the submodule. No effect if the submodule clock is already off. Read 0x0: The submodule is off. Read 0x1: The submodule is on. Write 0x1: Request enable of the submodule. No effect if the submodule clock is already off.	RW	0
5	IMX_A	iMX A Write 0x0: Request shutdown of the submodule. No effect if the submodule clock is already off. Read 0x0: The submodule is off. Read 0x1: The submodule is on. Write 0x1: Request enable of the submodule. No effect if the submodule clock is already off.	RW	0
4	NSF2	NSF2 Write 0x0: Request shutdown of the submodule. No effect if the submodule clock is already off. Read 0x0: The submodule is off. Read 0x1: The submodule is on. Write 0x1: Request enable of the submodule. No effect if the submodule clock is already off.	RW	0
3	VLCDJ	VLCDJ Write 0x0: Request shutdown of the submodule. No effect if the submodule clock is already off. Read 0x0: The submodule is off. Read 0x1: The submodule is on. Write 0x1: Request enable of the submodule. No effect if the submodule clock is already off.	RW	0
2	DCT	DCT Write 0x0: Request shutdown of the submodule. No effect if the submodule clock is already off. Read 0x0: The submodule is off. Read 0x1: The submodule is on. Write 0x1: Request enable of the submodule. No effect if the submodule clock is already off.	RW	0
1	LDC	LDC Write 0x0: Request shutdown of the submodule. No effect if the submodule clock is already off. Read 0x0: The submodule is off. Read 0x1: The submodule is on. Write 0x1: Request enable of the submodule. No effect if the submodule clock is already off.	RW	0

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Bits	Field Name	Description	Type	Reset
0	DMA	DMA Write 0x0: Request shutdown of the submodule. No effect if the submodule clock is already off. Read 0x0: The submodule is off. Read 0x1: The submodule is on. Write 0x1: Request enable of the submodule. No effect if the submodule clock is already off.	RW	0

Table 8-1264. Register Call Summary for Register SIMCOP_CLKCTRL

ISS Still Image Coprocessor

- ISS SIMCOP Functional Description: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13]
- ISS SIMCOP Programming Models: [14]
- ISS SIMCOP Register Manual: [15]

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8.4.1.5 ISS SIMCOP Memory Mapping

Table 8-1265 shows the SIMCOP memory mapping seen by the L3 interconnect and the Cortex-M3 MPU subsystem. SIMCOP memory mapping has a 128-KB address space.

Table 8-1265. SIMCOP Memory Mapping

Module	L3 Address		Cortex-M3 Address		Size (Bits)
	Begin	End	Begin	End	
Hardware sequencer/buffer registers	0x5202 0000	0x5202 00FF	0x5506 0000	0x5506 00FF	256
LDC registers	0x5202 0100	0x5202 017F	0x5506 0100	0x5506 017F	128
iMX A registers	0x5202 0180	0x5202 01BF	0x5506 0180	0x5506 01BF	64
iMX B registers	0x5202 01C0	0x5202 01FF	0x5506 01C0	0x5506 01FF	64
SIMCOP DMA registers	0x5202 0200	0x5202 03FF	0x5506 0200	0x5506 03FF	512
Reserved	0x5202 0400	0x5202 05FF	0x5506 0400	0x5506 05FF	512
VLCDJ registers	0x5202 0600	0x5202 067F	0x5506 0600	0x5506 067F	128
Reserved	0x5202 0680	0x5202 06FF	0x5506 0680	0x5506 06FF	128
ROT registers	0x5202 0700	0x5202 073F	0x5506 0700	0x5506 073F	64
Reserved	0x5202 0740	0x5202 077F	0x5506 0740	0x5506 077F	64
NSF2 registers	0x5202 0780	0x5202 07FF	0x5506 0780	0x5506 07FF	128
DCT registers	0x5202 0800	0x5202 081F	0x5506 0800	0x5506 081F	32
Reserved	0x5202 0820	0x5202 0FFF	0x5506 0820	0x5506 0FFF	2016
Bitstream buffer	0x5202 1000	0x5202 1FFF	0x5506 1000	0x5506 1FFF	4096
Huffman tables	0x5202 2000	0x5202 2FFF	0x5506 2000	0x5506 2FFF	4096
Reserved	0x5202 3000	0x5202 3FFF	0x5506 3000	0x5506 3FFF	4096
iMX B command memory	0x5202 4000	0x5202 5FFF	0x5506 4000	0x5506 5FFF	8192
iMX A command memory	0x5202 6000	0x5202 6FFF	0x5506 6000	0x5506 6FFF	4096
Quantization tables	0x5202 7000	0x5202 73FF	0x5506 7000	0x5506 73FF	1024
LDC LUT	0x5202 7400	0x5202 75FF	0x5506 7400	0x5506 75FF	512
Reserved	0x5202 7600	0x5202 7FFF	0x5506 7600	0x5506 7FFF	2560
Image buffer A	0x5202 8000	0x5202 8FFF	0x5506 8000	0x5506 8FFF	4096
Image buffer B	0x5202 9000	0x5202 9FFF	0x5506 9000	0x5506 9FFF	4096
Image buffer C	0x5202 A000	0x5202 AFFF	0x5506 A000	0x5506 AFFF	4096
Image buffer D	0x5202 B000	0x5202 BFFF	0x5506 B000	0x5506 BFFF	4096
Image buffer E	0x5202 C000	0x5202 CFFF	0x5506 C000	0x5506 CFFF	4096
Image buffer F	0x5202 D000	0x5202 DFFF	0x5506 D000	0x5506 DFFF	4096
Image buffer G	0x5202 E000	0x5202 EFFF	0x5506 E000	0x5506 EFFF	4096
Image buffer H	0x5202 F000	0x5202 FFFF	0x5506 F000	0x5506 FFFF	4096
iMX A coeffficients memory	0x5203 0000	0x5203 3FFF	0x5507 0000	0x5507 3FFF	16,384
iMX B coeffficients memory	0x5203 4000	0x5203 7FFF	0x5507 4000	0x5507 7FFF	16,384

8.4.2 ISS SIMCOP Hardware Sequencer and Buffers

This section describes the hardware sequencer and buffers in the still image coprocessor (SIMCOP) subsystem.

8.4.2.1 ISS SIMCOP Hardware Sequencer and Buffers Overview

The SIMCOP hardware sequencer control all the modules included in the SIMCOP subsystem with their memories.

Figure 8-247 shows an overview of the hardware sequencer and buffers in the SIMCOP subsystem.

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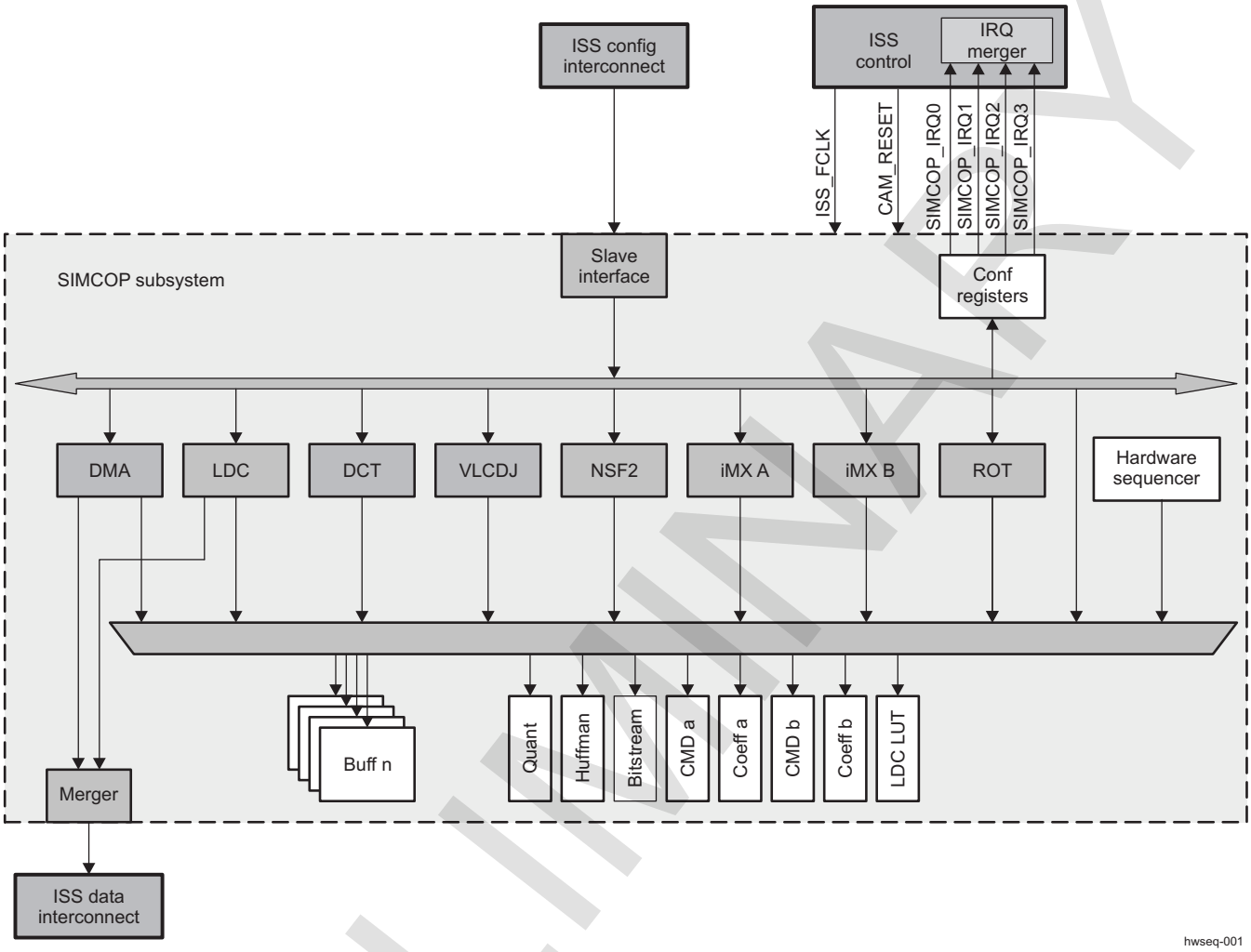
Figure 8-247. Hardware Sequencer and Buffers in the SIMCOP Subsystem



- Hardware acceleration for low-level sequencing tasks:
  - Synchronizes with DMA, DCT, VLCDJ, ROT, NSF2, LDC, and iMX
  - Supports 4 memory crossbar contexts
- On-chip memories (RAM):
  - Eight image buffers, 4KB each
  - Quantization table storage: 512 bytes
  - Huffman table storage: 4KB
  - Bitstream buffer: 4KB
  - Two iMX coefficient memories: 16KB each
  - Two iMX program memories: 4KB for iMX A and 8KB for iMX B
  - LDC look-up table (LUT) storage: 256 entries
- Power-management support

8.4.2.2 ISS SIMCOP Hardware Sequencer and Buffer Integration

The hardware sequencer and buffers module is part of the SIMCOP subsystem in the imaging subsystem (ISS).

Figure 8-248 shows the integration of the hardware sequencer and buffers in the SIMCOP subsystem.

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Figure 8-248. Hardware Sequencer and Buffer Integration

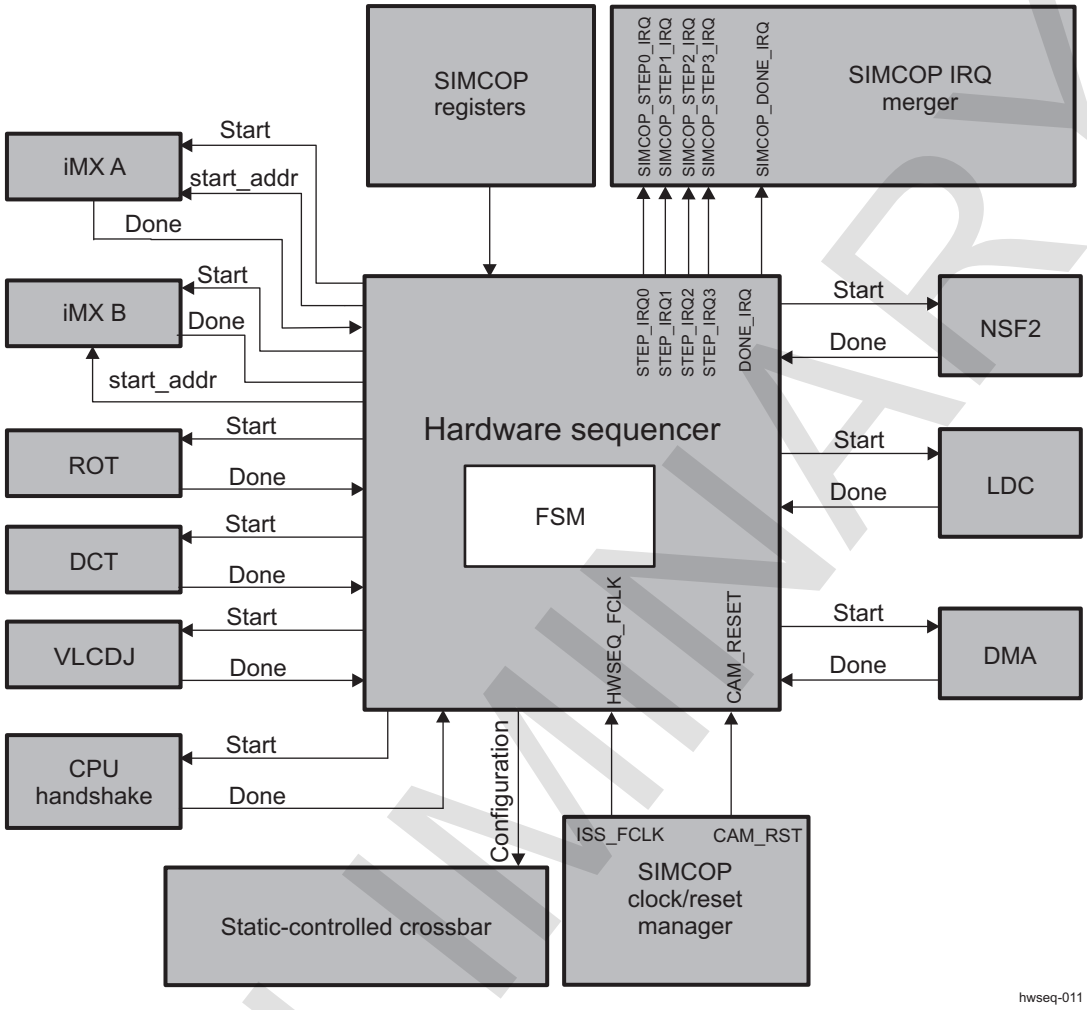

Table 8-1266 lists the integration attributes, Table 8-1267 lists the clocks and resets, and Table 8-1268 lists the hardware requests.

Table 8-1266. Integration Attributes

Module Instance	Attributes	
	Power Domain	Interconnect
Hardware sequencer and buffers	PD_CAM	

Table 8-1267. Clocks and Resets

Clocks				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
Hardware sequencer and buffers	HWSEQ_FCLK	ISS_FCLK	PRCM	Functional clock provided by ISS_CLK from PRCM . It is used by all ISS submodules and ISS top-level resources.
Resets				
Hardware sequencer and buffers	CAM_RESET	CAM_RST	PRCM	ISS and SIMCOP global reset

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For information about clock and reset management, see Section 8.4.1.2.1, *ISS SIMCOP Local Power and Clock Management*.

Table 8-1268. Hardware Requests

Interrupt Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
Hardware sequencer and buffers	STEP_IRQ0	SIMCOP_STEP0_IRQ	SIMCOP IRQ merger	Event triggered when a SIMCOP context is activated by the hardware sequencer
Hardware sequencer and buffers	STEP_IRQ1	SIMCOP_STEP1_IRQ	SIMCOP IRQ merger	Event triggered when a SIMCOP context is activated by the hardware sequencer
Hardware sequencer and buffers	STEP_IRQ2	SIMCOP_STEP2_IRQ	SIMCOP IRQ merger	Event triggered when a SIMCOP context is activated by the hardware sequencer
Hardware sequencer and buffers	STEP_IRQ3	SIMCOP_STEP3_IRQ	SIMCOP IRQ merger	Event triggered when a SIMCOP context is activated by the hardware sequencer
Hardware sequencer and buffers	DONE_IRQ	SIMCOP_DONE_IRQ	SIMCOP IRQ merger	Event triggered when the hardware sequencer finishes the sequence

For more information about interrupt requests, see Section 8.4.1.2.3, *Interrupt Merger.*

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8.4.2.3 ISS SIMCOP Hardware Sequencer and Buffers Functional Description

8.4.2.3.1 ISS SIMCOP Hardware Sequencer and Buffers Software Reset

For information about how to perform a software reset, see Section 8.4.1.2.2, *Software Reset*.

8.4.2.3.2 ISS SIMCOP Hardware Sequencer and Buffers Power Management

For more information about power management, see Section 8.4.1.2.1.3, *ISS SIMCOP Power Management*.

8.4.2.3.3 ISS SIMCOP Hardware Sequencer and Buffer Interrupt Requests

This module sends four interrupts to the ISS top level. For more information about interrupt management, see Section 8.4.1.2.3, *Interrupt Merger*.

8.4.2.3.4 ISS SIMCOP Hardware Sequencer Buffer Description

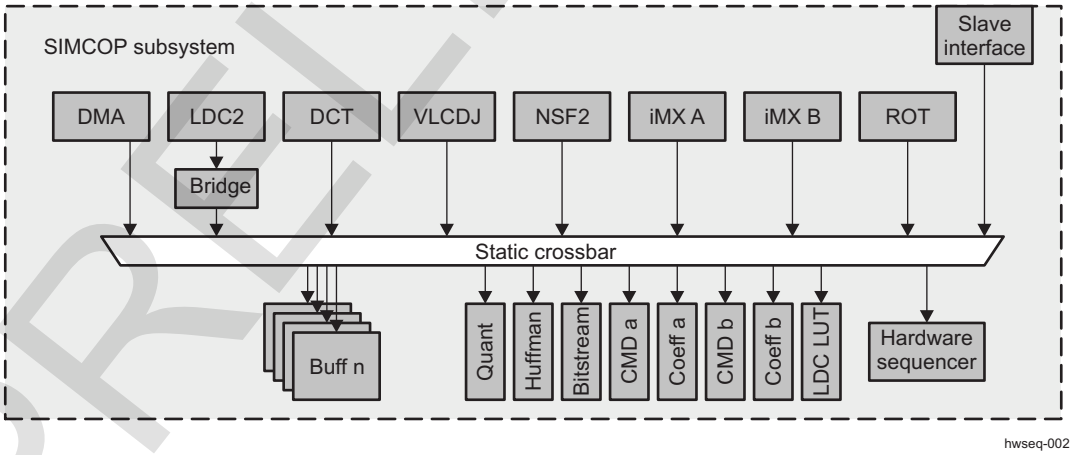
The SIMCOP subsystem includes the following memories:

- Eight image buffers, 4KB each
- Quantization table storage: 512 bytes
- Huffman table storage: 4KB
- Bitstream buffer: 4KB
- Two iMX coefficient memories: 16KB each
- Two iMX program memories: 4KB for iMX A and 8KB for iMX B
- LDC LUT storage: 256 entries
- LDC private working memory

8.4.2.3.4.1 Static Crossbar

The static crossbar connects SIMCOP modules to the SIMCOP memories as shown in Figure 8-249.

Figure 8-249. SIMCOP Static Crossbar Overview



The buses for QUANT, HUFF, LDC LUT, CMD a, and CMD b are controlled by an external initiator. Typically, those memories are initialized before SIMCOP starts processing, and the content remains unchanged until the full frame is processed. The amount of data transferred to those memories is low and transfer is not timing critical. Table 8-1269 shows how to connect these memories to SIMCOP modules.

NOTE: The transfer can only be done through the slave interface (for example, CPU or system DMA [sDMA]). The SIMCOP DMA cannot access those memories.

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Table 8-1269. Static Crossbar Control Summary

Memory	Register SIMCOP_CTRL	Value						
		Bus	iMX A inst	iMX B inst	VLCDJ HUFF	VLCDJ QUANT	LDC LUT	LDC INPUT
Quantization	[10] QUANT	0				1		
Huffman	[11] HUFF	0			1			
CMD a	[13:12] IMX_A_CMD	0	1	2				
CMD b	[14] IMX_B_CMD	0		1				
LDC LUT	[8] LDC_LUT	0					1	
LDC Priv	[7:6] LDC_INPUT							3

Image buffers and coefficient memories are used to store the data to be processed and processing results. Those memories can be accessed by the SIMCOP DMA, SIMCOP bus, and SIMCOP modules. Table 8-1270 shows possible connections in the SIMCOP static crossbar: for example DCT Freq port can access image buffer A when SIMCOP_HWSEQ_SWITCH_i[2:0] IMBUFF_A = 5 (where i = 0, 1, 2, or 3 corresponds to the active context).

SIMCOP supports multiple contexts for the configuration of those memories. Software or the hardware sequencer can activate different contexts.

The BITSTREAM data flow is asynchronous from the macroblock pipeline. Therefore it supports dynamic buffer switching logic.

Table 8-1270. Static Crossbar Control Summary (2/2)

Memory	Register (SIMCOP_HWSEQ_STEP_SWITCH_i and SIMCOP_HWSEQ_STEP_CTRL2_i)	Value													
		Bus	DMA	iMX data A	iMX data B	VLCDJ IO	VLCDJ BS	DCT Spatial	DCT Freq	NSF2 IO	NSF2 WMEM	LDC 0	LDC WMEM	ROT In	ROT Out
IMBUF A	[2:0] IMBUFF A	0	1	2	3	4			5		NSF2_WMEM = 2,3		LDC_INPUT= 1 or 2	6	
IMBUF B	[6:4] IMBUFF B	0	1	2	3	4			5					6	
IMBUF C	[10:8] IMBUFF C	0	1	2	3	4			5		NSF2_WMEM = 3		LDC_INPUT= 2	6	
IMBUF D	[14:12] IMBUFF D	0	1	2	3	4			5					6	
IMBUF E	[18:16] IMBUFF E	0	1	2	3			4		5		6			7
IMBUF F	[22:20] IMBUFF F	0	1	2	3			4		5		6			7
IMBUF G	[27:24] IMBUFF G	0	1	2	3	4		5	6	8		9			7
IMBUF H	[31:28] IMBUFF H	0	1	2	3	4		5	6	8		9			7
iMX A coeff	[2:0] COEFF_A	0	1	2	3	4			5		NSF2_WMEM = 1			6	
iMX B coeff	[6:4] COEFF_B	0	1	2	3	4			5						6
Bitstream	Handled by hardware	X	X				X								

8.4.2.3.4.2 Image Buffers

Image buffers are four banks × 256 × 32 bits (4KB) working memories used by the SIMCOP modules to perform image processing operations. Image buffers are shared between the iMX, NSF2, DCT, LDC, VLCDJ, ROT, DMA, and SIMCOP bus accesses. Not all initiators can access the image buffers simultaneously.

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Switches are controlled by the hardware sequencer or an external initiator through register configuration. Data is always organized in little-endian format.

One or multiple image buffers can be attached to a given accelerator port by configuring the adequate bits in the SIMCOP_HWSEQ_STEP_SWITCH_i registers.

The image buffer address mapping to different buses listed in Table 8-1271 is controlled using the adequate SIMCOP_HWSEQ_STEP_CTRL_i register bit fields.

Table 8-1271. Image Buffer Address Map

Port	OFST	0x0000	0x1000	0x2000	0x3000	0x4000	0x5000	0x6000	0x7000
DMA	0	A	B	C	D	E	F	G	H
	1	B	C	D	E	F	G	H	A
	2	C	D	E	F	G	H	A	B
	3	D	E	F	G	H	A	B	C
	4	E	F	G	H	A	B	C	D
	5	F	G	H	A	B	C	D	E
	6	G	H	A	B	C	D	E	F
	7	H	A	B	C	D	E	F	G
iMX A data	0	A	B	C	D				
	1	C	D	E	F				
	2	E	F	G	H				
	3	G	H	A	B				
iMX B data	0	A	B	C	D				
	1	C	D	E	F				
	2	E	F	G	H				
	3	G	H	A	B				
VLCDJ I/O	0	A	B	C	D				
	1	B	C	D	G				
	2	C	D	G	H				
	3	D	G	H	A				
	4	G	H	A	B				
	5	H	A	B	C				
	6								
	7								
DCT spatial	0	E	F						
	1	F	G						
	2	G	H						
	3	H	E						
DCT Freq	0	A	B	C	D				
	1	B	C	D	G				
	2	C	D	G	H				
	3	D	G	H	A				
	4	G	H	A	B				
	5	H	A	B	C				
	6								
	7								
NSF I/O	0	E	F						
	1	F	G						
	2	G	H						
	3	H	E						
NSF2 WMEM	N/A	A	B	C	D				

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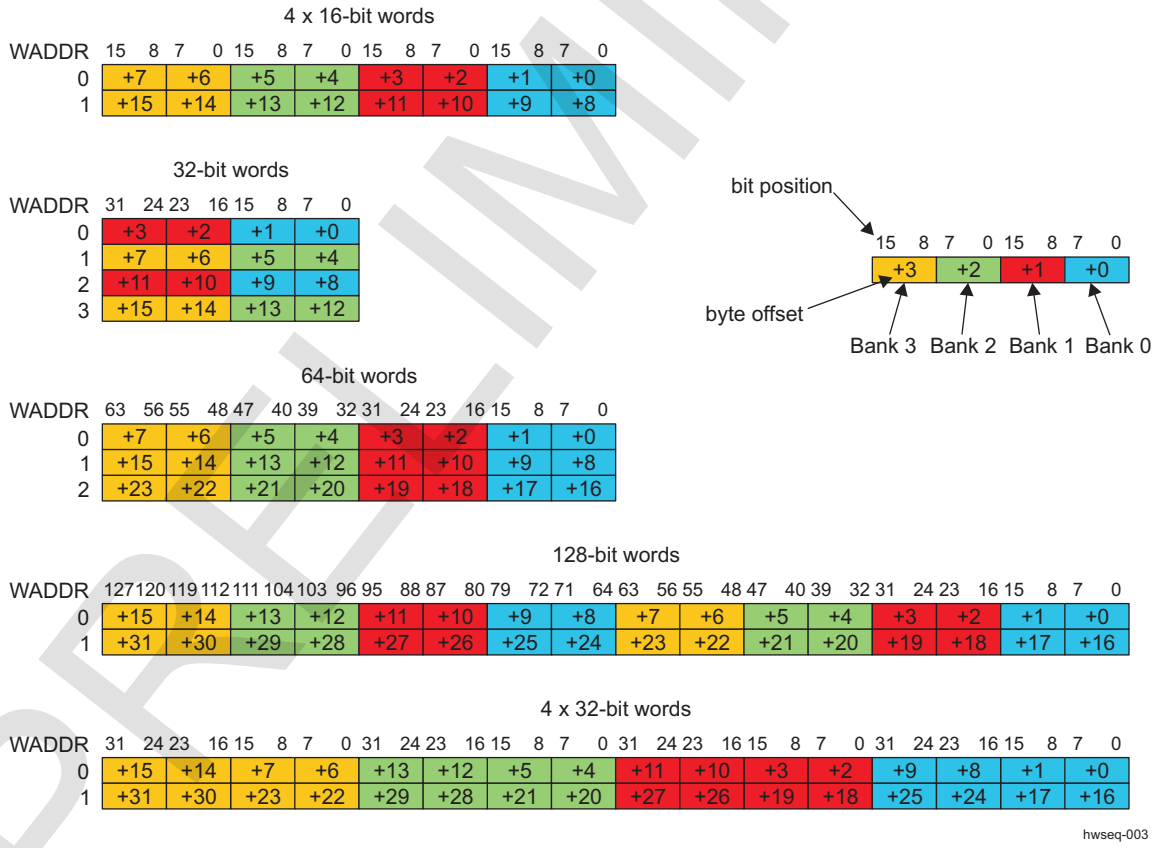
Table 8-1271. Image Buffer Address Map (continued)

Port	OFST	0x0000	0x1000	0x2000	0x3000	0x4000	0x5000	0x6000	0x7000
LDC O	0	E	F	G	H				
	1	F	G	H	E				
	2	G	H	E	F				
	3	H	E	F	G				
LDC W	N/A	A	B	C	D				
ROT in	0	A	B	C	D				
	1	B	C	D	A				
	2	C	D	A	B				
	3	D	A	B	C				
ROT out	0	E	F	G	H				
	1	F	G	H	E				
	2	G	H	E	F				
	3	H	E	F	G				

Figure 8-250 shows how width conversion and bank interleaving is performed. Each color corresponds to a different physical bank.

Figure 8-250. Image Buffer Width Translation



8.4.2.3.4.3 Coefficient Memories

The IMX_COEF_A memory is used by the NSF2 to store temporary data. The IMX_x also uses COEFF_A and COEFF_B to store coefficients used during certain operations. IMX_COEF_A and IMX_COEFF_B are shared between the iMX, DMA, DCT, VLCDJ, and SIMCOP bus accesses. Only one initiator can access a coefficient memory at given time.

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Switches are controlled by the hardware sequencer or an external initiator through register configuration. Data is always organized in little-endian format.

The initiators access types to the IMX_COEF_x memory are summarized in Table 8-1272. Coefficient memory configuration depends on the initiators. Data is always organized little endian.

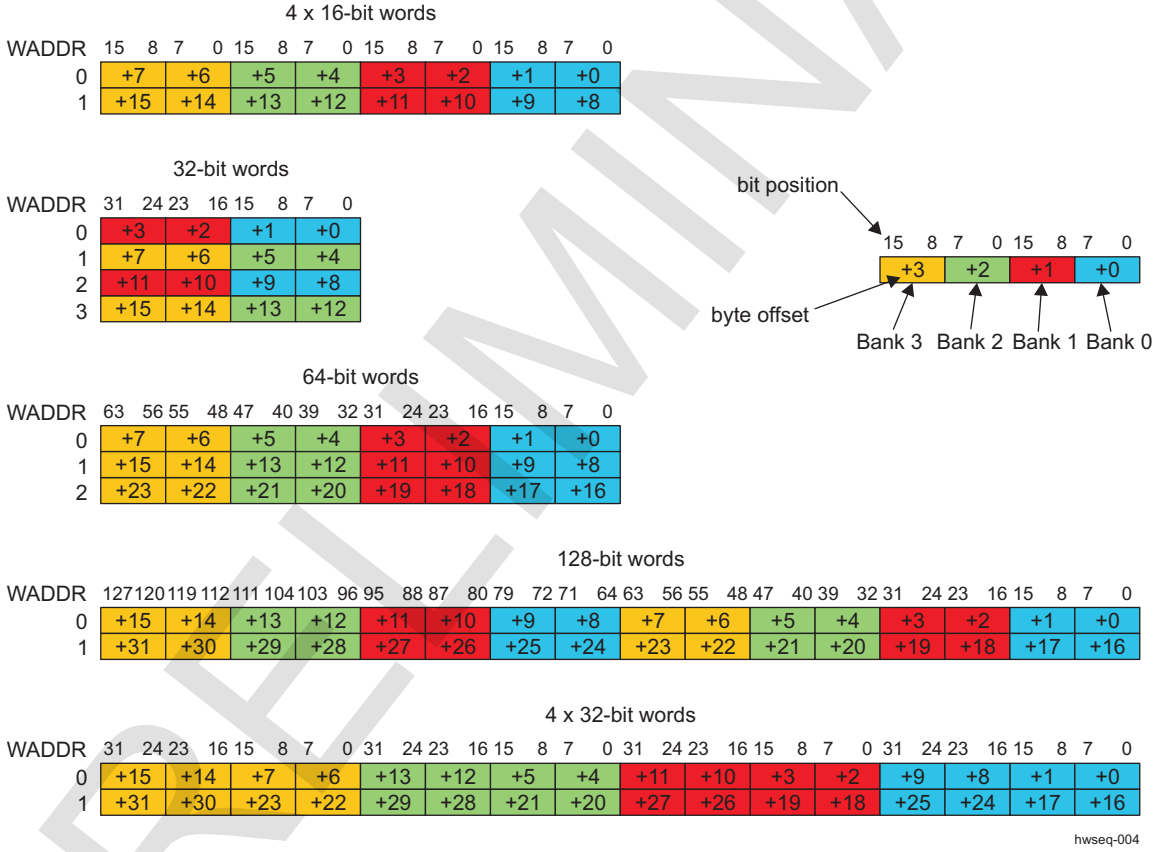
Table 8-1272. Coefficient Buffer Organization

iMX	Coprocessor Bus	ROT In	DMA
VLCDJ IO		ROT Out	DCT Freq
			NSF2 WMEM [1]
4 banks × 2048 words × 16 bits	4096 words × 32 bits	2048 words × 64 bits	1024 words × 128 bits

(1) IMX_COEFF_A only

Figure 8-251 shows how width conversion and bank interleaving is performed. Each color corresponds to a different physical bank.

Figure 8-251. Coefficient Memory Width Translation



8.4.2.3.4.4 Quantization Memories

The QUANT memory is used to store the quantization and dequantization tables for the VLCDJ module.

Coefficients are coded as 16-bit values. Every color component requires 8 × 8 quantization entries, therefore the QUANT memory of SIMCOP can hold up to four tables as shown in Table 8-1273.

Table 8-1273. Quantization Table Storage in QUANT Memory

Table	0	1	2	3
ADDR	0x000	0x0080	0x0100	0x0180
Encode only	Y quantization	UV quantization	Unused	Unused

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Table 8-1273. Quantization Table Storage in QUANT Memory (continued)

Table	0	1	2	3
Decode only	Unused	Unused	Y dequantization	UV dequantization
Encode and decode	Y quantization	UV quantization	Y dequantization	UV dequantization

QUANT is shared between the VLCDJ and SIMCOP bus accesses. All initiators cannot access QUANT simultaneously.

The initiators access types to the QUANT memory are summarized in Table 8-1274. QUANT memory configuration depends on the initiators.

Table 8-1274. QUANT Memory Organization

VLCDJ	Coprocessor Bus
128 words × 32 bits	128 words × 32 bits

8.4.2.3.4.5 Huffman Tables

The HUFF memory is used to store the Huffman table for the VLCDJ module. Details about the Huffman table organization can be found in the VLCDJ module description (see Section 8.4.6, *VLCDJ*).

HUFF memory is shared between the VLCDJ and SIMCOP bus accesses. All initiators cannot access HUFF simultaneously.

The initiators access types to the HUFF memory are summarized in Table 8-1275. HUFF memory configuration depends on the initiators.

Table 8-1275. HUFF Memory Organization

VLCDJ	Coprocessor Bus
1024 words × 32 bits	1024 words × 32 bits

8.4.2.3.4.6 Bitstream Buffer

8.4.2.3.4.6.1 Overview

The bitstream buffer is used to store the VLCDJ bitstream. The bitstream buffer is shared between the VLCDJ, DMA, and SIMCOP bus accesses.

The bitstream buffer can be used in manual or automatic mode.

In manual mode, software selects if SIMCOP DMA, VLCDJ bitstream port, or SIMCOP bus can access the bitstream buffer. Manual mode is typically used to interleave JPEG encode and decode, for example, to support JPEG transcoding. .

In automatic mode (SIMCOP_HWSEQ_CTRL[6:4] BITSTREAM = ENCODE or DECODE) the bitstream buffer is handled as two banks to prevent access collision between VLCDJ and SIMCOP DMA. A dedicated hardware engine (BBM) is used to ensure that VLCDJ and SIMCOP DMA access separate banks.

Automatic mode is disabled by writing SIMCOP_HWSEQ_CTRL[6:4] BITSTREAM = COPR.

The bitstream buffer mapping into the SIMCOP DMA address map depends on the SIMCOP_HWSEQ_CTRL[6:4] BITSTREAM and SIMCOP_HWSEQ_CTRL[3:2] BITSTR_XFER_SIZE bit fields and the internal state of the BBM. Table 8-1276 lists the mapping of the bitstream buffer for SIMCOP DMA.

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Table 8-1276. Bitstream Buffer Mapping to SIMCOP DMA

SIMCOP_HWSEQ_CTRL		Address Map		BBM count	Bitstream buffer	
BITSTREAM	XFER_SIZE					
0: COPRO	N/A	0x1000	0x1FFF	N/A	0x000	0xFFF
5: ENCODE or 6: DECODE	2048 bytes	0x1000	0x17FF	N/A	0x000	0x7FF
				N/A	0x800	0xFFF
		0x1800	0x1FFF	N/A	N/A	N/A
	1024 bytes	0x1000	0x13FF	0	0x000	0x3FF
				1	0x400	0x7FF
		0x1400	0x1FFF	N/A	N/A	N/A
	512 bytes	0x1000	0x11FF	0	0x000	0x1FF
				1	0x200	0x3FF
				2	0x400	0x5FF
				3	0x600	0x7FF
		0x1200	0x1FFF	N/A	N/A	N/A
	256 bytes	0x1000	0x10FF	0	0x000	0x0FF
				1	0x100	0x1FF
				2	0x200	0x2FF
				3	0x300	0x3FF
				4	0x400	0x4FF
				5	0x500	0x5FF
				6	0x600	0x6FF
				7	0x700	0x7FF
		0x1100	0x1FFF	N/A	N/A	N/A

8.4.2.3.4.6.2 Automatic Bitstream Buffer Management

To enter automatic mode software must write the following values into the BITSTREAM configuration register:

- SIMCOP_HWSEQ_CTRL[6:4] BITSTREAM=COPR (required to reset BBM)
- SIMCOP_HWSEQ_CTRL[6:4] BITSTREAM=JPEG_ENCODE or JPEG_DECODE

8.4.2.3.4.7 LDC Lookup Table

The LDC_LUT memory is used to store LUTs for the LDC module. LDC_LUT is shared between the LDC and SIMCOP bus accesses. All initiators cannot access LDC_LUT simultaneously.

The initiators access types to the QUANT memory are summarized in Table 8-1277. QUANT memory configuration depends on the initiators.

Table 8-1277. LDC_LUT Memory Organization

LDC	Coprocessor Bus
256 words × 14 bits	128 words × 32 bits (see Table 8-1278)

Table 8-1278. LUT Memory Format on 32-Bit Words

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								LDC_LUT [2a+1]								RESERVED								LDC_LUT [2a+0]							

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8.4.2.3.4.8 LDC Private Input Memory

The LDC has a private input memory that can be used when LDC operates in YUV 4:2:0 mode. For YUV 4:2:2 and RAW operation, LDC must use image buffers as input memories.

The LDC input memory is dedicated for LDC operation. It cannot be accessed from the SIMCOP bus or by any other SIMCOP module.

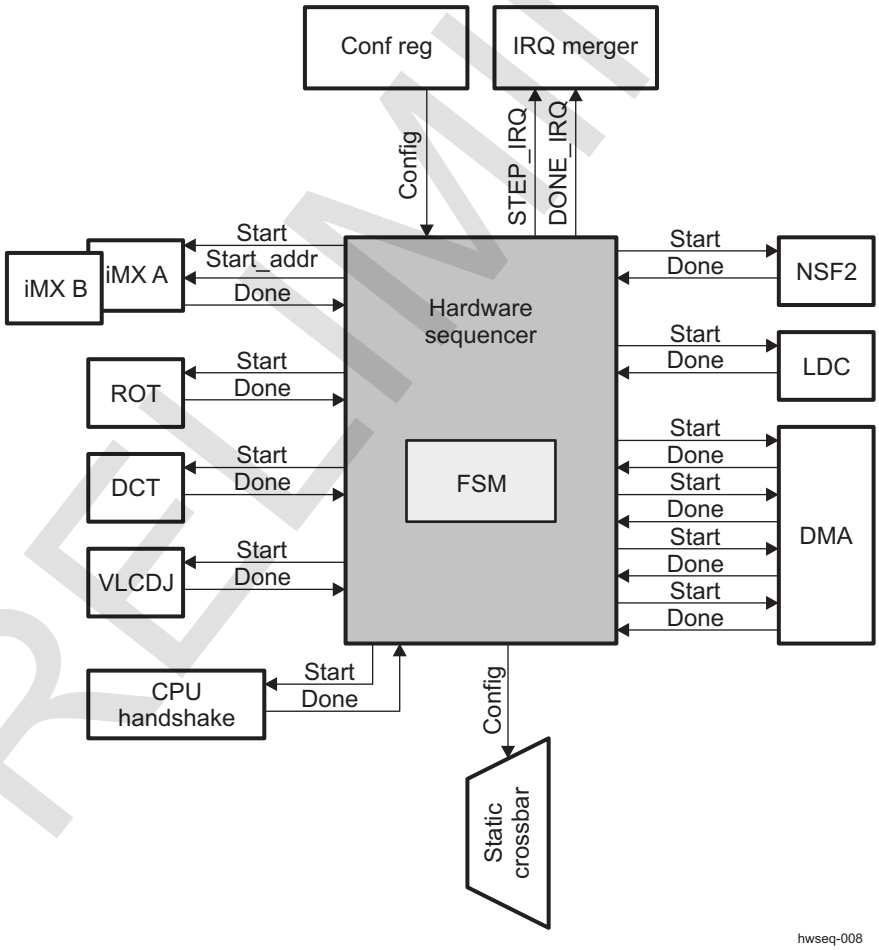
8.4.2.3.5 ISS SIMCOP Hardware Sequencer

SIMCOP typically processes a full frame on a macroblock by macroblock basis. SIMCOP modules and the DMA controller trigger an interrupt when they have completed a macroblock. This event can trigger an interrupt to an external initiator (manual mode) or trigger a context switch and resume DMA/SIMCOP module processing. Typically, initiator intervention is needed to fill the macroblock pipeline (called pipe-up. For example, first n macroblocks of an image) and to flush the macroblock pipeline (called pipe-down. For example, last n macroblocks of an image). Automatic sequencing mode is typically used for the rest of the image.

The hardware sequencer is particularly useful to offload the initiator during JPEG encode/decode, ROT, LDC, NSF2, or iMX processing.

Figure 8-252 shows the SIMCOP hardware sequencer overview.

Figure 8-252. SIMCOP Hardware Sequencer Overview



The hardware sequencer can automatically execute a predefined number of sequencing steps without

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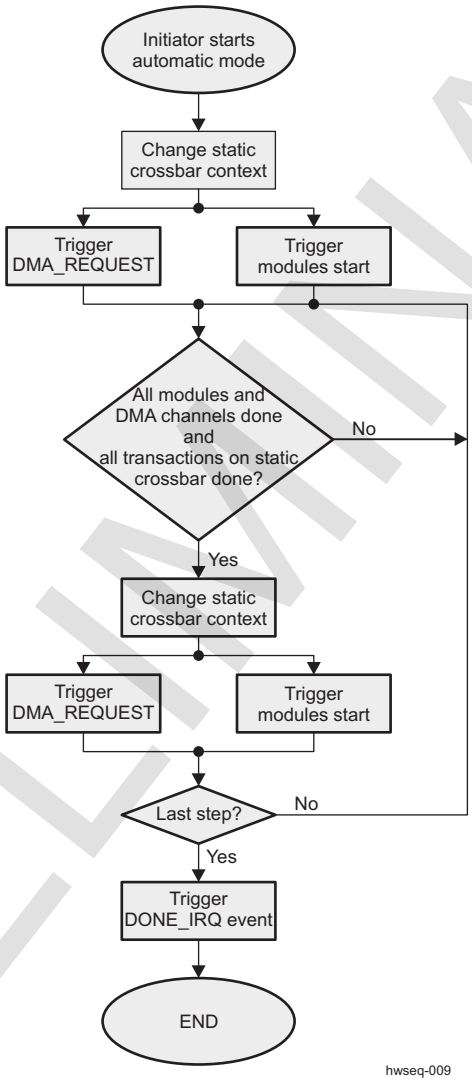
software intervention. That is called automatic operation. Automatic operation can also be used to pipeline filling and flushing with some limited software intervention. During automatic operation, the hardware sequencer controls generation of START/DONE pulses and the connections in the static-controlled crossbar. Software can take control over some resources while the hardware sequencer is running. That is called hardware sequencer override.

8.4.2.3.5.1 Automatic Operation

Figure 8-253 shows the flow diagram executed by the hardware sequencer.

Figure 8-253. Hardware Sequencing Example



The external initiator configures the different SIMCOP modules and DMA channels. When this is done, the initiator enables the hardware sequencer. This resets the internal state of the hardware sequencer (pending events, context switch counter).

It starts by running sequence step SIMCOP_HWSEQ_CTRL[12:11] STEP:

- Clear all pending completion events that have been selected for step 0 in the hardware sequencer. This does not affect the SIMCOP_IRQSTATUS register.
- Apply step SIMCOP_HWSEQ_CTRL[12:11] STEP configuration to the static crossbar.
- Start DMA transfers. Multiple channels can be enabled sequentially (for example, YUV 4:2:0 data transfers or SIMCOP→SDRAM followed by SDRAM→SIMCOP) by using the SIMCOP DMA linking feature.

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- Start hardware accelerators. The list of accelerators to start can be selected by software using the SIMCOP_HWSEQ_STEP_CTRL_i[7:0] *_SYNC register.

The hardware sequencer then waits for completion of events from selected SIMCOP modules and SIMCOP DMA channels.

The hardware sequencer also ensures that all SIMCOP memory accesses requested by accelerators and DMA channels enabled for the synchronization step are complete. This condition prevents data corruption due to early switching.

Steps can be chained to define the sequence to execute. Steps are started until the step counter reaches the limit defined by software. When the last step has completed, a DONE_IRQ event is triggered.

SIMCOP can execute one hardware sequence at a time. However, software can be used to execute multiple independent sequences in parallel (for example, two unrelated macroblock pipelines) using the override feature.

The hardware sequencer has no specific support for macroblock pipeline filling (pipe-up) or flushing (pipe-down). It needs some software intervention.

The hardware sequencer supports sequences composed of up to four steps. Longer sequences require software intervention.

Figure 8-253 shows hardware sequencer operation.

Figure 8-254. Hardware Sequencer Operation Example

The example involves use of two SIMCOP modules (or DMA channels) that are synchronized using the hardware sequencer. A total of five sequencing steps are executed (SIMCOP_HWSEQ_CTRL[31:6] HW_SEQ_STEP_COUNTER = 5). The sequence is two steps long and starts with step 1. These two steps are configured using the SIMCOP_HWSEQ_STEP_*_i registers (where i = 0 and 1).

SIMCOP modules processing is started using START pulses (green). When SIMCOP modules are done they return a DONE pulse (red). Software can choose which accelerators to run for a given step using the SIMCOP_HWSEQ_STEP_CTRL_i[7:0] *_SYNC registers. They do not need to finish at the same time because the hardware sequencer waits for reception of all DONE pulses of used accelerators before moving to the next step.

The hardware sequencer also triggers a series of interrupts that can be used by software. For example, it is possible for software to change the configuration of inactive sequencing steps. This can be particularly useful to run longer sequences than what is supported by hardware.

For example, software can set up a 4-step looping sequence: Step 0 → 1 → 2 → 3 → 0 → 1 → .... When the STEP1_IRQ event is triggered, software can load the configuration into the SIMCOP_HWSEQ_STEP_*_i registers, to be used the next time step 0 becomes active.

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8.4.2.3.5.2 Hardware Sequencer Override

By default, the hardware sequencer controls START/DONE pulses of all SIMCOP modules as well as the static-controlled crossbar. Software can take control over some resources by setting the adequate bits in the SIMCOP_HWSEQ_OVERRIDE register. Sequencing resources under software control are managed using the SIMCOP_HWSEQ_STEP_CTRL_OVERRIDE and SIMCOP_HWSEQ_STEP_SWITCH_OVERRIDE registers.

Changes to the SIMCOP_HWSEQ_STEP_CTRL_OVERRIDE[27:11] *_OFST and SIMCOP_HWSEQ_STEP_SWITCH_OVERRIDE registers have immediate effect. Software must ensure there is no active traffic on the affected connection in the static-controlled crossbar.

For example, when software wants to alternatively attach image buffers a and b to SIMCOP_DMA while preserving the buffer start address in the SIMCOP DMA address map constant, it sets the following for the full application duration:

- SIMCOP_HWSEQ_STEP_SWITCH_OVERRIDE[2:0] IMBUFF_A = 1
- SIMCOP_HWSEQ_STEP_SWITCH_OVERRIDE[6:4] IMBUFF_B = 1

It then changes the SIMCOP_HWSEQ_STEP_SWITCH_OVERRIDE[2:0] IMBUFF_A and SIMCOP_HWSEQ_STEP_SWITCH_OVERRIDE[6:4] IMBUFF_B registers to attach the image buffers to the correct SIMCOP submodule.

The settings in the SIMCOP_HWSEQ_STEP_CTRL_OVERRIDE and SIMCOP_HWSEQ_STEP_SWITCH_OVERRIDE registers for resources controlled by the hardware sequencer have no effect.

Synchronization with SIMCOP modules is controlled using the SIMCOP_HWSEQ_STEP_CTRL_OVERRIDE[7:0] *_TRIGGER bit fields. For ROT, NSF, VLCDJ, DCT, and LDC, a START pulse is send to the module when 1 is written into the adequate bit field. Software can trigger one or multiple start pulses at the time. The *_TRIGGER bit field is cleared by writing 1. It is automatically set by hardware when a DONE pulse is received from the relevant SIMCOP module.

Software can poll the status of the SIMCOP_HWSEQ_STEP_CTRL_OVERRIDE[7:0] *_TRIGGER bit field to detect when a SIMCOP module has completed its processing task. Alternatively, software can also use an interrupt. SIMCOP can merge one or multiple internal events into SIMCOP outgoing interrupts. Software can choose between two modes for each interrupt output (SIMCOP_CTRL[3:0] IRQx_MODE):

- 0x0: OR, the interrupt is asserted when one of the selected events has occurred.
- 0x1: AND, the interrupt is asserted when all selected events have occurred.

The AND mode leads to lower initiator load. In fact, the initiator is only interrupted once per sequencing step, even when events from multiple SIMCOP submodules are expected. Also, it does not need to poll the SIMCOP_HL_IRQSTATUS_i register to detect which events have occurred: it simply must write 0xFFF FFFF into the SIMCOP_HL_IRQSTATUS_i register to clear all pending events.

The SIMCOP DMA START/DONE control is slightly different. Software can trigger one or multiple DMA channels by writing into the SIMCOP_HWSEQ_STEP_CTRL_OVERRIDE[7:5] DMA_TRIGGER bit field. The DMA_TRIGGER bit field returns the written value when all expected DONE pulses are received from SIMCOP DMA.

Alternatively, SIMCOP modules (except LDC) may be triggered by direct writes into their configuration registers. However, this approach leads to higher initiator load because multiple writes must be done.

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8.4.2.4 ISS SIMCOP Hardware Sequencer and Buffers Basic Programming Model

8.4.2.4.1 ISS SIMCOP Application Programming Principle

Software must first configure SIMCOP access tag handling (SIMCOP_CTRL[24:21] LDC_R_TAG_CNT, SIMCOP_CTRL[19:16] LDC_R_TAG_OFST, and SIMCOP_DMA_CTRL[7:4] TAG_CNT). Software must ensure there is no active traffic on the SIMCOP master port before changing those registers.

Then it initializes Huffman, Quantization, and LDC LUT if they are used. Those memories must first be attached to the SIMCOP bus so they can be accessed from the slave port (SIMCOP_CTRL[11] HUFF, SIMCOP_CTRL[10] QUANT, and SIMCOP_CTRL[7:6] LDC_LUT). Then they can be preloaded using an external CPU or an external DMA engine. SIMCOP DMA cannot preload these tables.

Similarly, software can also preload data lsuch as filter coefficients into iMX coefficient memories or image buffers. This can be handled by SIMCOP DMA:

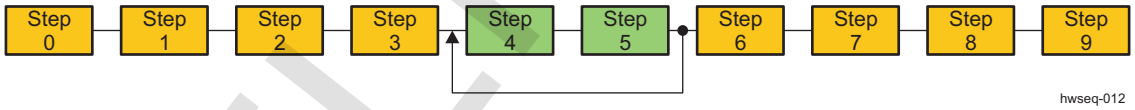
- The buffers must first be attached to the SIMCOP DMA using the SIMCOP_HWSEQ_OVERRIDE and SIMCOP_HWSEQ_STEP_SWITCH_OVERRIDE registers.
- Alternatively, software can use the SIMCOP_HWSEQ_STEP_*_i registers (where i = 0) instead of the override feature. The hardware sequencer ensures that the configuration of step 0 is applied when the hardware sequencer is disabled.
- Software then configures and starts one or multiple data transfers using the SIMCOP DMA.
- Software monitors SIMCOP DMA events to know when DMA transfers are complete. Other configuration tasks may happen concurrently, but software must ensure that transfers complete before attaching the memories to another module.

Software must then enable the modules to be used.

Typically, the first steps and last steps of the macroblock pipeline are different from the ones in the middle of the pipeline. The hardware sequencer has no specific support for pipe-up and pipe-down. However, software can cut the sequence into smaller sequences to benefit from the hardware sequencing and to avoid software sequencing.

Figure 8-255 shows an example of a 10-step sequence involving two DMA transfers and three modules.

Figure 8-255. Typical Hardware Sequencer-Controlled Sequencer With Pipe-Up and Pipe-Down



The macroblock pipeline is composed of a chain of three modules. Data between the modules is exchanged using ping-pong buffering.

Pipe-up and pipe-down require four sequencing steps each. The main processing can be done with two steps.

Software configures the hardware sequencer with the 4-step pipe-up sequence. Each step is executed once. When pipe-up is done, SIMCOP triggers the DONE_IRQ event.

Software then reconfigures the hardware sequencer for the 2-step main sequence. The number of steps is defined by the amount of data to process. When the main pipe is done, SIMCOP triggers the DONE_IRQ event.

Software finally reconfigures the hardware sequencer with the 4-step pipe-down sequence. Each step is executed once. When pipe-down is done, SIMCOP triggers the DONE_IRQ event.

Figure 8-256 shows an example of pipe-up and pipe-done.

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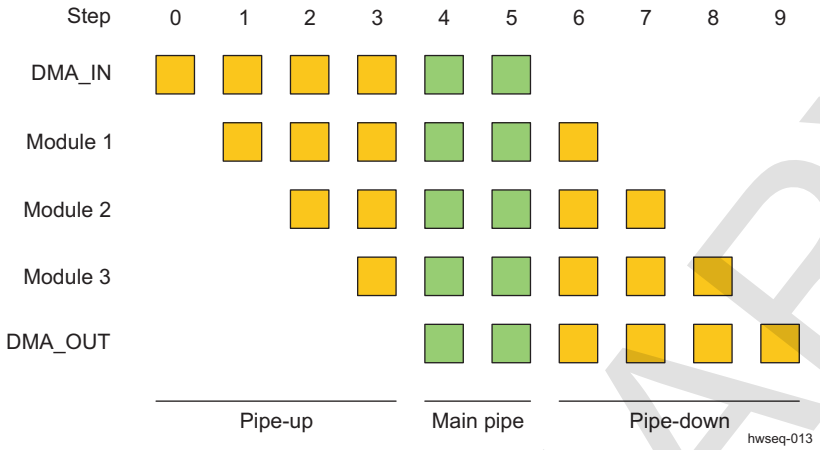
Figure 8-256. Pipe-Up and Pipe-Down



The hardware sequencer configuration determines which module can access a given SIMCOP memory for a sequence step.

8.4.2.4.2 External CPU Use for Data Processing

An external CPU can be used to perform some data processing, as SIMCOP hardware accelerators do. A similar mechanism to the START/DONE pulse interaction with SIMCOP hardware accelerators is implemented.

The external CPU receives the request to start processing by the CPU_PROC_START_IRQ interrupt merged at SIMCOP subsystem level. This interrupt is enabled and acknowledged as usual.

When processing completes, the CPU generates the DONE pulse to the hardware sequencer by setting the SIMCOP_HWSEQ_CTRL[10] CPU_PROC_DONE bit to 1.

8.4.2.4.3 Rotation Operational Mode Configuration

The macroblock pipeline is controlled by a 2-step hardware sequence:

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Figure 8-257. Rotation Macroblock Pipeline

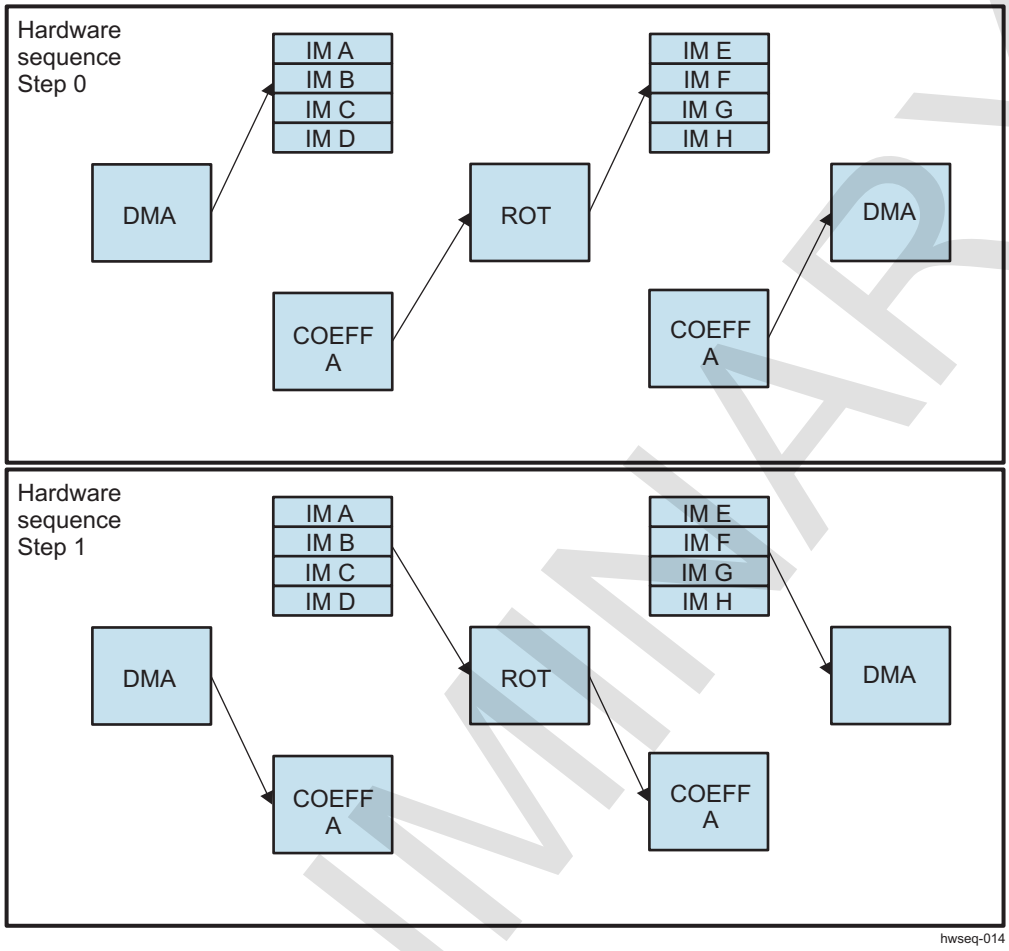

Table 8-1279. Rotation Macroblock Pipeline

Step	Register/Bit Field/Programming Model	Value
Set DMA to access IMBUFF_A.	SIMCOP_HWSEQ_STEP_SWITCH_i[2:0] IMBUFF_A (i = 0)	0x1
Set ROT_A_O to access IMBUFF_E.	SIMCOP_HWSEQ_STEP_SWITCH_i[18:16] IMBUFF_E (i = 0)	0x7
Set ROT_A_I to access COEFF_A.	SIMCOP_HWSEQ_STEP_CTRL2_i[2:0] = COEFF_A (i = 0)	0x6
Set DMA to access COEFF_B.	SIMCOP_HWSEQ_STEP_CTRL2_i[6:4] COEFF_B (i = 0)	0x1
Set ROT_A_I to access IMBUFF_A.	SIMCOP_HWSEQ_STEP_SWITCH_i[2:0] IMBUFF_A (i = 1)	0x6
Set DMA to access IMBUFF_E.	SIMCOP_HWSEQ_STEP_SWITCH_i[18:16] IMBUFF_E (i = 1)	0x1
Set DMA to access COEFF_A.	SIMCOP_HWSEQ_STEP_CTRL2_i[2:0] COEFF_A (i = 1)	0x1
Set ROT_A_O to access COEFF_B.	SIMCOP_HWSEQ_STEP_CTRL2_i[6:4] COEFF_B (i = 1)	0x6

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8.4.2.4.4 LDC Operational Mode Configuration

The LDC module fetches data from system memory, performs the transformation, and stores results into image buffers. DCT and VLCDJ modules are used to JPEG compress this data and store the results to the bitstream buffer. The SIMCOP DMA is used to transfer compressed data from bitstream buffer to system memory.

Figure 8-258. LDC Transformation Pipeline

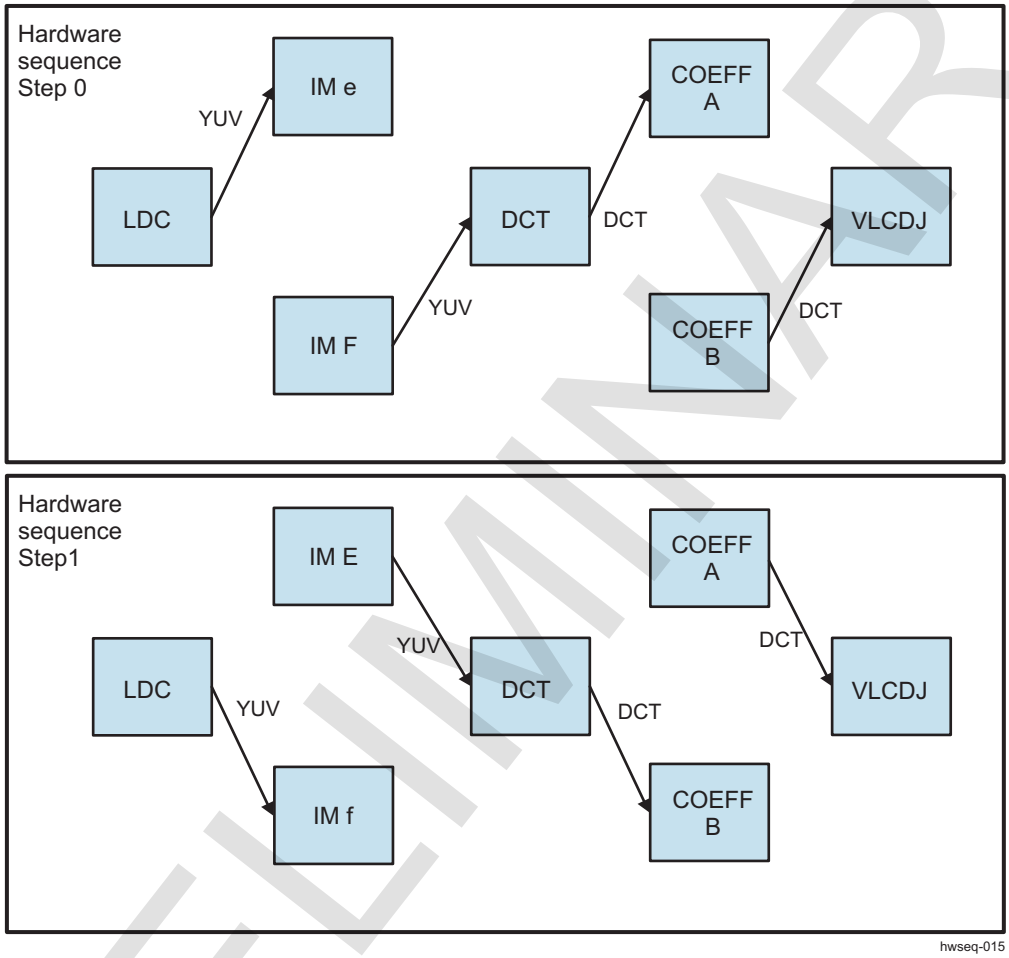

Table 8-1280. LDC Transformation

Step	Register/Bit Field/Programming Model	Value
Set IMBUFF_A and IMCUFF_B as input buffer.	SIMCOP_CTRL[7:6] LDC_INPUT	0x1
Set LDC to access IMBUFF_E.	SIMCOP_HWSEQ_STEP_SWITCH_i[18:16] IMBUFF_E	0x6
Set DCT to access COEFF_A.	SIMCOP_HWSEQ_STEP_CTRL2_i[2:0] COEFF_A	0x5
Set VLCDJ_IO to access COEFF_B.	SIMCOP_HWSEQ_STEP_CTRL2_i[6:4] COEFF_B	0x4
Set DCT to access IMBUFF_E.	SIMCOP_HWSEQ_STEP_SWITCH_i[18:16] IMBUFF_E	0x4
Set LDC to access IMBUFF_F.	SIMCOP_HWSEQ_STEP_SWITCH_i[18:16] IMBUFF_F	0x6
Set VLCDJ_IO to access COEFF_A.	SIMCOP_HWSEQ_STEP_CTRL2_i[2:0] COEFF_A	0x4
Set DCT to access COEFF_B.	SIMCOP_HWSEQ_STEP_CTRL2_i[6:4] COEFF_B	0x5

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8.4.2.4.5 Concurrent Software and Hardware Sequencing

Software can perform sequencing tasks concurrently with hardware sequencing. This is supported through the hardware sequencer override registers:

- SIMCOP_HWSEQ_OVERRIDE
- SIMCOP_HWSEQ_STEP_CTRL_OVERRIDE
- SIMCOP_HWSEQ_STEP_SWITCH_OVERRIDE
- SIMCOP_HWSEQ_STEP_CTRL2_OVERRIDE

Software can select which hardware resources are controlled by the hardware sequencer and which resources are controlled by software. Configuration parameters for software-controlled resources are provided using those registers as well.

Table 8-1281. Concurrent Software and Hardware Sequencing

Step	Register/Bit Field/Programming Model	Value
Set software to control IMBUFF_E.	SIMCOP_HWSEQ_OVERRIDE[13] IMBUFF_E	0x1
Set DMA to access IMBUFF_E.	SIMCOP_HWSEQ_STEP_SWITCH_OVERRIDE[18:16] IMBUFF_E	0x1
Set software to control IMBUFF_F.	SIMCOP_HWSEQ_OVERRIDE[14] IMBUFF_F	0x1
Set DCT_S to access IMBUFF_F.	SIMCOP_HWSEQ_STEP_SWITCH_OVERRIDE[22:20] IMBUFF_F	0x4
Set software to control COEFF_A.	SIMCOP_HWSEQ_OVERRIDE[17] COEFF_A	0x1
Set iMX A to access the COEFF_A.	SIMCOP_HWSEQ_STEP_CTRL2_OVERRIDE[2:0] COEFF_A	0x2
Set hardware sequencer to control COEFF_B.	SIMCOP_HWSEQ_OVERRIDE[18] COEFF_B	0x0
Set iMX B to access the COEFF_B.	SIMCOP_HWSEQ_STEP_CTRL2_i[6:4] COEFF_B	0x3

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8.4.2.5 ISS SIMCOP Hardware Sequencer and Buffers Register Manual

8.4.2.5.1 Hardware Sequencer Instance Summary

Table 8-1282 summarizes the hardware sequencer instance.

Table 8-1282. Hardware Sequencer Instance Summary

Module Name	Base Address L3 Interconnect	Base Address Cortex-M3 Private Access	Size
HWSEQ	0x5202 0000	0x5506 0000	256 bytes

NOTE: Private Access is an access that does not use the L3/L4 interconnects.

8.4.2.5.2 Hardware Sequencer Registers

8.4.2.5.2.1 Hardware Sequencer Register Summary

Table 8-1283 lists the HWSEQ register mapping.

Table 8-1283. HWSEQ Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	Physical Address L3 Interconnect	Physical Address Cortex-M3 Private Access
SIMCOP_HWSEQ_CTRL	RW	32	0x0000 0068	0x5202 0068	0x5506 0068
SIMCOP_HWSEQ_STATUS	R	32	0x0000 006C	0x5202 006C	0x5506 006C
SIMCOP_HWSEQ_OVERRIDE	RW	32	0x0000 0070	0x5202 0070	0x5506 0070
SIMCOP_HWSEQ_STEP_CTRL_OVERRIDE	RW	32	0x0000 0074	0x5202 0074	0x5506 0074
SIMCOP_HWSEQ_STEP_SWITCH_OVERRIDE	RW	32	0x0000 0078	0x5202 0078	0x5506 0078
SIMCOP_HWSEQ_STEP_CTRL2_OVERRIDE	RW	32	0x0000 007C	0x5202 007C	0x5506 007C
SIMCOP_HWSEQ_STEP_CTRL_i [(1)]	RW	32	0x0000 0080 + (0x10 * i)	0x5202 0080 + (0x10 * i)	0x5506 0080 + (0x10 * i)
SIMCOP_HWSEQ_STEP_SWITCH_i [(1)]	RW	32	0x0000 0084 + (0x10 * i)	0x5202 0084 + (0x10 * i)	0x5506 0084 + (0x10 * i)
SIMCOP_HWSEQ_STEP_IMX_CTRL_i [(1)]	RW	32	0x0000 0088 + (0x10 * i)	0x5202 0088 + (0x10 * i)	0x5506 0088 + (0x10 * i)
SIMCOP_HWSEQ_STEP_CTRL2_i [(1)]	RW	32	0x0000 008C + (0x10 * i)	0x5202 008C + (0x10 * i)	0x5506 008C + (0x10 * i)

(1) i = 0 to 3

8.4.2.5.2.2 Hardware Sequencer Register Descriptions

through describe the registers in detail.

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Table 8-1284. SIMCOP_HWSEQ_CTRL

Address Offset	0x0000 0068		
Physical Address	0x5202 0068 0x5506 0068	**Instance**	HWSEQ_L3 HWSEQ_CORTEX-M3
Description	SIMCOP hardware sequencer control register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HW_SEQ_STEP_COUNTER																RESERVED			STEP		CPU_PROC_DONE	BBM_SYNC_CHAN		BBM_STATUS	BITSTREAM			BITSTR_XFER_SIZE		HW_SEQ_STOP	HW_SEQ_START

Bits	Field Name	Description	Type	Reset
31:16	HW_SEQ_STEP_COUNTER	Number of steps executed by the hardware sequencer. HW_SEQ_STEP_COUNTER=0 corresponds to manual sequencing.	RW	0x0000
15:13	RESERVED	Read returns 0.	R	0x0
12:11	STEP	This register is automatically updated by the hardware sequencer when it is active. Otherwise, software can use it to activate the content of a given set of step registers (SIMCOP_HWSEQ_STEP_i) or to choose the first step number of a sequence.	RW	0x0
10	CPU_PROC_DONE	Used by the CPU to tell that it has completed data processing. This feature should be used together with the CPU_PROC_START_IRQ event Read's always return 0. Write 0x0: No effect. Write 0x1: CPU processing completed.	W	0
9:8	BBM_SYNC_CHAN	Defines the SIMCOP DMA hardware synchronization channel to be used for BBM. This register is only used when BITSTREAM=ENCODE or DECODE. Software must ensure that the same DMA hardware synchronization channel is not used by the hardware sequencer.	RW	0x0
7	BBM_STATUS	Status of the Bitstream buffer management hardware.Used only during automatic mode [BITSTREAM=5 or 6]. Equals 0 (IDLE) in manual mode [BITSTREAM=0..4].Set when automatic mode is entered. Automatic encode mode: used to detect when all banks have been flushed after the processing has completed (i.e. but request bank signals have been de-asserted by BBM). Automatic decode mode (BITSTREAM=DECODE): returns to 0 (IDLE) when automatic mode is left (BITSTREAM=COPR). Read 0x1: BBM is busy. Read 0x0: BBM is idle	R	0

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Bits	Field Name	Description	Type	Reset
6:4	BITSTREAM	Bitstream buffer access control 0x0: Bank 0: coprocessor bus (0x1000-0x17FF) Bank 1: coprocessor bus (0x1800-0x1FFF) 0x1: Bank 0: DMA (0x1000-0x17FF) Bank 1: DMA (0x1800-0x1FFF) 0x2: Bank 0: VLCDJ.B (0x000-0x7FF) Bank 1: VLCDJ.B (0x800-0xFFF) 0x3: Bank 0: DMA (0x1000-0x17FF) Bank 1: VLCDJ.B (0x800-0xFFF) 0x4: Bank 0: VLCDJ.B (0x000-0x7FF) Bank 1: DMA (0x1800-0x1FFF) 0x5: The bitstream buffer is managed by hardware as a PING/PONG buffer to support JPEG encode use case. It can be accessed by the SIMCOP DMA or the VLCDJ module. The BITSTREAM hardware sequence is reset when the mode is changed to COPR, VLCDJ or DMA. 0x6: The bitstream buffer is managed by hardware as a PING/PONG buffer to support JPEG decode use case. It can be accessed by the SIMCOP DMA or the VLCDJ module. The BITSTREAM hardware sequence is reset when the mode is changed to COPR, VLCDJ or DMA.	RW	0x0
3:2	BITSTR_XFER_SIZE	Defines the amount of data to be transferred per hardware request to the SIMCOP DMA. Bigger sizes lead to better SDRAM efficiency but prevents fine grained DMA transfer arbitration. This register is only used by hardware when BITSTREAM=ENCODE or BITSTREAM=DECODE. 0x0: 2048 bytes 0x1: 1024 bytes 0x2: 512 bytes 0x3: 256 bytes	RW	0x0
1	HW_SEQ_STOP	Stop the hardware sequencer. This feature is typically used to recover from an error condition. Read's always return 0. Write 0x0: No effect. Write 0x1: Stop the hardware sequence immediately (don't wait for expected DONE events). Setting this bit while the sequencer is idle has no effect.	W	0
0	HW_SEQ_START	Start the hardware sequencer. Read's always return 0. Write 0x0: No effect. Write 0x1: Starts step number SIMCOP_HWSEQ_CTRL[12:11] STEP of the hardware sequence. Setting this bit while the sequencer is running has no effect.	W	0

Table 8-1285. Register Call Summary for Register SIMCOP_HWSEQ_CTRL

ISS Still Image Coprocessor

- ISS SIMCOP Hardware Sequencer and Buffers Functional Description: [1] [2] [3] [4] [5] [6] [7] [11] [12] [13]
- ISS SIMCOP Hardware Sequencer and Buffers Basic Programming Model: [14]
- ISS SIMCOP Hardware Sequencer and Buffers Register Manual: [15] [16]

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Table 8-1286. SIMCOP_HWSEQ_STATUS

Address Offset	0x0000 006C		
Physical Address	0x5202 006C 0x5506 006C	**Instance**	HWSEQ_L3 HWSEQ_CORTEX-M3
Description	Hardware sequencer status register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HW_SEQ_STEP_COUNTER																RESERVED															STATE

Bits	Field Name	Description	Type	Reset
31:16	HW_SEQ_STEP_COUNTER	Current step number	R	0x0000
15:1	RESERVED	Read returns 0.	R	0x0000
0	STATE	Current state Read 0x0: Idle Read 0x1: Running	R	0

Table 8-1287. Register Call Summary for Register SIMCOP_HWSEQ_STATUS

ISS Still Image Coprocessor

- ISS SIMCOP Hardware Sequencer and Buffers Register Manual: [0]

Table 8-1288. SIMCOP_HWSEQ_OVERRIDE

Address Offset	0x0000 0070		
Physical Address	0x5202 0070 0x5506 0070	**Instance**	HWSEQ_L3 HWSEQ_CORTEX-M3
Description	Hardware sequencer override control register. Bits in this register select what configuration register control a resource. 0: Resource controlled by hardware sequencer. Hardware uses the value from SIMCOP_HWSEQ_STEP_xx registers for the chosen resource 1: Resource controlled by software. Hardware uses the value from SIMCOP_HWSEQ_STEP_x_OVERRIDE registers for the chosen resource The bit field name matches the one of the resource. For example, IMX_A_D_OFST_OVR selects if SIMCOP_HWSEQ_STEP_CTRL_i[12:11] IMX_A_D_OFST or SIMCOP_HWSEQ_STEP_CTRL_OVERRIDE[12:11] IMX_A_D_OFST controls how image buffers are arranged in the iMX A address map.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													COEFF_B	COEFF_A	IMBUFF_H	IMBUFF_G	IMBUFF_F	IMBUFF_E	IMBUFF_D	IMBUFF_C	IMBUFF_B	IMBUFF_A	LDC_O_OFST_OVR	ROT_O_OFST_OVR	ROT_I_OFST_OVR	NSF_IO_OFST_OVR	DCT_F_OFST_OVR	DCT_S_OFST_OVR	VLCDJ_IO_OFST_OVR	IMX_B_D_OFST_OVR	IMX_A_D_OFST_OVR

Bits	Field Name	Description	Type	Reset
31:19	RESERVED	Read returns 0.	R	0x0000
18	COEFF_B	See register description	RW	0
17	COEFF_A	See register description	RW	0
16	IMBUFF_H	See register description	RW	0
15	IMBUFF_G	See register description	RW	0

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Bits	Field Name	Description	Type	Reset
14	IMBUFF_F	See register description	RW	0
13	IMBUFF_E	See register description	RW	0
12	IMBUFF_D	See register description	RW	0
11	IMBUFF_C	See register description	RW	0
10	IMBUFF_B	See register description	RW	0
9	IMBUFF_A	See register description	RW	0
8	LDC_O_OFST_OVR	See register description	RW	0
7	ROT_O_OFST_OVR	See register description	RW	0
6	ROT_I_OFST_OVR	See register description	RW	0
5	NSF_IO_OFST_OVR	See register description	RW	0
4	DCT_F_OFST_OVR	See register description	RW	0
3	DCT_S_OFST_OVR	See register description	RW	0
2	VLCDJ_IO_OFST_OVR	See register description	RW	0
1	IMX_B_D_OFST_OVR	See register description	RW	0
0	IMX_A_D_OFST_OVR	See register description	RW	0

Table 8-1289. Register Call Summary for Register SIMCOP_HWSEQ_OVERRIDE

ISS Still Image Coprocessor

- ISS SIMCOP Hardware Sequencer and Buffers Functional Description: [0]
- ISS SIMCOP Hardware Sequencer and Buffers Basic Programming Model: [1] [2] [3] [4] [5] [6]
- ISS SIMCOP Hardware Sequencer and Buffers Register Manual: [7]

Table 8-1290. SIMCOP_HWSEQ_STEP_CTRL_OVERRIDE

Address Offset	0x0000 0074		
Physical Address	0x5202 0074 0x5506 0074	**Instance**	HWSEQ_L3 HWSEQ_CORTEX-M3
Description	Hardware sequencer override register. Used to execute software sequences in parallel to hardware sequencing steps		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				ROT_O_OFST		ROT_I_OFST		RESERVED		DCT_F_OFST		DCT_S_OFST		VLCDJ_IO_OFST		IMX_B_D_OFST		IMX_A_D_OFST		RESERVED		DMA_TRIGGER		ROT_A_TRIGGER		NSF_TRIGGER		VLCDJ_TRIGGER		DCT_TRIGGER		LDC_TRIGGER	

Bits	Field Name	Description	Type	Reset
31:28	RESERVED	Read returns 0.	R	0x0
27:26	ROT_O_OFST	Controls ROT.O bus mapping to image buffers: 0x0000 0x1000 0x2000 0x3000 0x0: EFGH 0x1: FGHE 0x2: GHEF 0x3: HEFG	RW	0x0

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Bits	Field Name	Description	Type	Reset
25:24	ROT_I_OFST	Controls ROT_I bus mapping to image buffers: 0x0000 0x1000 0x2000 0x3000 0x0: ABCD 0x1: BCDA 0x2: CDAB 0x3: DABC	RW	0x0
23	RESERVED	Read returns 0.	R	0
22:20	DCT_F_OFST	Controls DCT.F bus mapping to image buffers: 0x0000 0x1000 0x2000 0x3000 0x0: ABCD 0x1: BCDG 0x2: CDGH 0x3: DGHA 0x4: GHAB 0x5: HABC	RW	0x0
19:18	DCT_S_OFST	Controls DCT.S bus mapping to image buffers: 0x0000 0x1000 0x0: EF 0x1: FG 0x2: GH 0x3: HE	RW	0x0
17:15	VLCDJ_IO_OFST	Controls VLCDJ IO data bus mapping to image buffers: 0x0000 0x1000 0x2000 0x3000 0x0: ABCD 0x1: BCDG 0x2: CDGH 0x3: DGHA 0x4: GHAB 0x5: HABC	RW	0x0
14:13	IMX_B_D_OFST	Controls iMX B data bus mapping to image buffers: 0x0000 0x1000 0x2000 0x3000 0x0: ABCD 0x1: CDEF 0x2: EFGH 0x3: GHAB	RW	0x0
12:11	IMX_A_D_OFST	Controls iMX A data bus mapping to image buffers: 0x0000 0x1000 0x2000 0x3000 0x0: ABCD 0x1: CDEF 0x2: EFGH 0x3: GHAB	RW	0x0
10:8	RESERVED	Read returns 0.	R	0x0

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Bits	Field Name	Description	Type	Reset
7:5	DMA_TRIGGER	Software controlled START/DONE synchronization Write 0x0: No effect Read 0x0: No done pulse have been received since last non zero write into the DMA_TRIGGER register Read 0x1: DONE pulses for channel 0 and 1 have been received Write 0x1: Trigger channel 0 and 1. Clears all memorized done pulses for DMA. Write 0x2: Trigger channel 0, 1, 2. Clears all memorized done pulses for DMA. Read 0x2: DONE pulses for channel 0, 1 and 2 have been received Read 0x3: DONE pulses for channel 0, 1, 2 and 3 have been received. Write 0x3: Trigger channel 0, 1, 2 and 3. Clears all memorized done pulses for DMA. Read 0x4: DONE pulse for channel 0 has been received Write 0x4: Trigger channel 0. Clears all memorized done pulses for DMA. Write 0x5: Trigger channel 1. Clears all memorized done pulses for DMA. Read 0x5: DONE pulse for channel 1 has been received Read 0x6: DONE pulse for channel 2 has been received Write 0x6: Trigger channel 2. Clears all memorized done pulses for DMA. Write 0x7: Trigger channel 3. Clears all memorized done pulses for DMA. Read 0x7: DONE pulse for channel 3 has been received	RW	0x0
4	ROT_A_TRIGGER	Software controlled START/DONE synchronization Write 0x0: No Effect Read 0x0: No DONE pulse received since the last START pulse has been sent Read 0x1: DONE pulse received Write 0x1: Send a start pulse and clears the memorized done pulse	RW	0
3	NSF_TRIGGER	Software controlled START/DONE synchronization Write 0x0: No Effect Read 0x0: No DONE pulse received since the last START pulse has been sent Read 0x1: DONE pulse received Write 0x1: Send a start pulse and clears the memorized done pulse	RW	0
2	VLCDJ_TRIGGER	Software controlled START/DONE synchronization Write 0x0: No Effect Read 0x0: No DONE pulse received since the last START pulse has been sent Read 0x1: DONE pulse received Write 0x1: Send a start pulse and clears the memorized done pulse	RW	0

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Bits	Field Name	Description	Type	Reset
1	DCT_TRIGGER	Software controlled START/DONE synchronization Write 0x0: No Effect Read 0x0: No DONE pulse received since the last START pulse has been sent Read 0x1: DONE pulse received Write 0x1: Send a start pulse and clears the memorized done pulse	RW	0
0	LDC_TRIGGER	Software controlled START/DONE synchronization Write 0x0: No Effect Read 0x0: No DONE pulse received since the last START pulse has been sent Read 0x1: DONE pulse received Write 0x1: Send a start pulse and clears the memorized done pulse	RW	0

Table 8-1291. Register Call Summary for Register SIMCOP_HWSEQ_STEP_CTRL_OVERRIDE

ISS Still Image Coprocessor

- ISS SIMCOP Hardware Sequencer and Buffers Functional Description: [0] [1] [2] [3] [4] [5]
- ISS SIMCOP Hardware Sequencer and Buffers Basic Programming Model: [6]
- ISS SIMCOP Hardware Sequencer and Buffers Register Manual: [7] [8]

Table 8-1292. SIMCOP_HWSEQ_STEP_SWITCH_OVERRIDE

Address Offset	0x0000 0078		
Physical Address	0x5202 0078 0x5506 0078	**Instance**	HWSEQ_L3 HWSEQ_CORTEX-M3
Description	Hardware sequencer override register. Used to execute software sequences in parallel to hardware sequencing steps		
Type	RW		

31 30 29 28	27 26 25 24	23	22 21 20 19	18 17 16	15	14 13 12 11	10 9 8	7	6 5 4 3	2 1 0
IMBUFF_H	IMBUFF_G	RESERVED	IMBUFF_F	IMBUFF_E	RESERVED	IMBUFF_D	IMBUFF_C	RESERVED	IMBUFF_B	IMBUFF_A

Bits	Field Name	Description	Type	Reset
31:28	IMBUFF_H	Switch for image buffer h 0x0: Coprocessor bus 0x1: SIMCOP DMA 0x2: iMX A 0x3: iMX B 0x4: VLCDJ_IO 0x5: DCT_S 0x6: DCT_F 0x7: ROT_A_O 0x8: NSF_IO 0x9: LDC_O	RW	0x0
27:24	IMBUFF_G	Switch for image buffer g 0x0: Coprocessor bus 0x1: SIMCOP DMA	RW	0x0

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Bits	Field Name	Description	Type	Reset
		0x2: iMX A		
		0x3: iMX B		
		0x4: VLCDJ_IO		
		0x5: DCT_S		
		0x6: DCT_F		
		0x7: ROT_A_O		
		0x8: NSF_IO		
		0x9: LDC_O		
23	RESERVED	Read returns 0.	R	0
22:20	IMBUFF_F	Switch for image buffer f	RW	0x0
		0x0: Coprocessor bus		
		0x1: SIMCOP DMA		
		0x2: iMX A		
		0x3: iMX B		
		0x4: DCT_S		
		0x5: NSF_IO		
		0x6: LDC_O		
		0x7: ROT_A_O		
19	RESERVED	Read returns 0.	R	0
18:16	IMBUFF_E	Switch for image buffer e	RW	0x0
		0x0: Coprocessor bus		
		0x1: SIMCOP DMA		
		0x2: iMX A		
		0x3: iMX B		
		0x4: DCT_S		
		0x5: NSF_IO		
		0x6: LDC_O		
		0x7: ROT_A_O		
15	RESERVED	Read returns 0.	R	0
14:12	IMBUFF_D	Switch for image buffer d	RW	0x0
		0x0: Coprocessor bus		
		0x1: SIMCOP DMA		
		0x2: iMX A		
		0x3: iMX B		
		0x4: VLCDJ_IO		
		0x5: DCT_F		
		0x6: ROT_A_I		
		0x7: Reserved		
11	RESERVED	Read returns 0.	R	0
10:8	IMBUFF_C	Switch for image buffer c.	RW	0x0
		0x0: Coprocessor bus		
		0x1: SIMCOP DMA		
		0x2: iMX A		
		0x3: iMX B		
		0x4: VLCDJ_IO		
		0x5: DCT_F		
		0x6: ROT_A_I		
		0x7: Reserved		
7	RESERVED	Read returns 0.	R	0

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Bits	Field Name	Description	Type	Reset
6:4	IMBUFF_B	Switch for image buffer b. 0x0: Coprocessor bus 0x1: SIMCOP DMA 0x2: iMX A IMBUFF 0x3: iMX B IMBUFF 0x4: VLCDJ_IO 0x5: DCT_F 0x6: ROT_A_I 0x7: Reserved	RW	0x0
3	RESERVED	Read returns 0.	R	0
2:0	IMBUFF_A	Switch for image buffer a 0x0: Coprocessor bus 0x1: SIMCOP DMA 0x2: iMX A IMBUFF 0x3: iMX B IMBUFF 0x4: VLCDJ_IO 0x5: DCT_F 0x6: ROT_A_I 0x7: Reserved	RW	0x0

Table 8-1293. Register Call Summary for Register SIMCOP_HWSEQ_STEP_SWITCH_OVERRIDE

ISS Still Image Coprocessor

- ISS SIMCOP Hardware Sequencer and Buffers Functional Description: [0] [1] [2] [3] [4] [5] [6]
- ISS SIMCOP Hardware Sequencer and Buffers Basic Programming Model: [7] [8] [9] [10]
- ISS SIMCOP Hardware Sequencer and Buffers Register Manual: [11]

Table 8-1294. SIMCOP_HWSEQ_STEP_CTRL2_OVERRIDE

Address Offset	0x0000 007C		
Physical Address	0x5202 007C 0x5506 007C	**Instance**	HWSEQ_L3 HWSEQ_CORTEX-M3
Description	Hardware sequencer override register. Used to execute software sequences in parallel to hardware sequencing steps		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				NSF2_IO_OFST		LDC_O_OFST		RESERVED				RESERVED			
																								COEFF_B				COEFF_A			

Bits	Field Name	Description	Type	Reset
31:12	RESERVED	Read returns 0.	R	0x00000
11:10	NSF2_IO_OFST	Controls NSF_IO bus mapping to image buffers: 0x0000 0x1000 0x0: EF 0x1: FG 0x2: GH 0x3: HE	RW	0x0

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Bits	Field Name	Description	Type	Reset
9:8	LDC_O_OFST	Controls LDC.O bus mapping to image buffers: 0x0000 0x1000 0x2000 0x3000 0x0: EFGH 0x1: FGHE 0x2: GHEF 0x3: HEFG	RW	0x0
7	RESERVED	Read returns 0.	R	0
6:4	COEFF_B	Coefficient buffer b switch 0x0: Coprocessor bus 0x1: SIMCOP DMA 0x2: iMX A 0x3: iMX B 0x4: VLCDJ_IO 0x5: DCT_F 0x6: ROT A O 0x7: Reserved	RW	0x0
3	RESERVED	Read returns 0.	R	0
2:0	COEFF_A	Coefficient buffer a switch 0x0: Coprocessor bus 0x1: SIMCOP DMA 0x2: iMX A 0x3: iMX B 0x4: VLCDJ_IO 0x5: DCT_F 0x6: ROT A I 0x7: Reserved	RW	0x0

Table 8-1295. Register Call Summary for Register SIMCOP_HWSEQ_STEP_CTRL2_OVERRIDE

ISS Still Image Coprocessor

- ISS SIMCOP Hardware Sequencer and Buffers Basic Programming Model: [0] [1]
- ISS SIMCOP Hardware Sequencer and Buffers Register Manual: [2]

Table 8-1296. SIMCOP_HWSEQ_STEP_CTRL_i

Address Offset	0x0000 0080 + (0x10 * i)		
Physical Address	0x5202 0080 + (0x10 * i) 0x5506 0080 + (0x10 * i)	**Instance**	HWSEQ_L3 HWSEQ_CORTEX-M3
Description	Hardware sequencer step control register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CPU_SYNC	DMA_OFST					ROT_O_OFST		ROT_I_OFST		RESERVED	DCT_F_OFST			DCT_S_OFST		VLCDJ_IO_OFST		IMX_B_D_OFST		IMX_A_D_OFST		NEXT	RESERVED	DMA_SYNC		ROT_A_SYNC		NSF_SYNC		VLCDJ_SYNC	DCT_SYNC	LDC_SYNC

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Bits	Field Name	Description	Type	Reset
31	CPU_SYNC	Enable hardware synchronization with the CPU so that it can be used for some processing on in the macroblock pipeline. 0x0: Disabled 0x1: Enabled.	RW	0
30:28	DMA_OFST	Controls DMA bus mapping to image buffers: 0x0000 0x1000 0x2000 0x3000 0x4000 0x5000 0x6000 0x7000 0x0: ABCDEFGH 0x1: BCDEFGHA 0x2: CDEFGHAB 0x3: DEFGHABC 0x4: EFGHABCD 0x5: FGHABCDE 0x6: GHABCDEF 0x7: HABCDEFG	RW	0x0
27:26	ROT_O_OFST	Controls ROT.O bus mapping to image buffers: 0x0000 0x1000 0x2000 0x3000 0x0: EFGH 0x1: FGHE 0x2: GHEF 0x3: HEFG	RW	0x0
25:24	ROT_I_OFST	Controls ROT_I bus mapping to image buffers: 0x0000 0x1000 0x2000 0x3000 0x0: ABCD 0x1: BCDA 0x2: CDAB 0x3: DABC	RW	0x0
23	RESERVED	Read returns 0.	R	0
22:20	DCT_F_OFST	Controls DCT.F bus mapping to image buffers: 0x0000 0x1000 0x2000 0x3000 0x0: ABCD 0x1: BCDG 0x2: CDGH 0x3: DGHA 0x4: GHAB 0x5: HABC	RW	0x0
19:18	DCT_S_OFST	Controls DCT.S bus mapping to image buffers: 0x0000 0x1000 0x0: EF 0x1: FG 0x2: GH 0x3: HE	RW	0x0
17:15	VLCDJ_IO_OFST	Controls VLCDJ IO data bus mapping to image buffers: 0x0000 0x1000 0x2000 0x3000 0x0: ABCD 0x1: BCDG 0x2: CDGH 0x3: DGHA 0x4: GHAB 0x5: HABC	RW	0x0

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Bits	Field Name	Description	Type	Reset
14:13	IMX_B_D_OFST	Controls iMX B data bus mapping to image buffers: 0x0000 0x1000 0x2000 0x3000 0x0: ABCD 0x1: CDEF 0x2: EFGH 0x3: GHAB	RW	0x0
12:11	IMX_A_D_OFST	Controls iMX A data bus mapping to image buffers: 0x0000 0x1000 0x2000 0x3000 0x0: ABCD 0x1: CDEF 0x2: EFGH 0x3: GHAB	RW	0x0
10:9	NEXT	Next channel in the sync chain 0x0: Step 0 0x1: Step 1 0x2: Step 2 0x3: Step 3	RW	0x0
8	RESERVED	Read returns 0.	R	0
7:5	DMA_SYNC	Enable hardware synchronization with the SIMCOP DMA 0x0: Disabled 0x1: Channel 0 and 1 0x2: Channel 0, 1, 2 0x3: Channel 0, 1, 2 and 3 0x4: Channel 0 0x5: Channel 1 0x6: Channel 2 0x7: Channel 3	RW	0x0
4	ROT_A_SYNC	Enable hardware synchronization with the ROT #a module 0x0: Disabled 0x1: Enabled.	RW	0
3	NSF_SYNC	Enable hardware synchronization with the NSF module 0x0: Disabled 0x1: Enabled	RW	0
2	VLCDJ_SYNC	Enable hardware synchronization with the VLCDJ module 0x0: Disabled 0x1: Enabled	RW	0
1	DCT_SYNC	Enable hardware synchronization with the DCT module 0x0: Disabled 0x1: Enabled	RW	0
0	LDC_SYNC	Enable hardware synchronization with the LDC module 0x0: Disabled 0x1: Enabled	RW	0

Table 8-1297. Register Call Summary for Register SIMCOP_HWSEQ_STEP_CTRL_i

ISS Still Image Coprocessor

- ISS SIMCOP Hardware Sequencer and Buffers Functional Description: [0] [1] [2]
- ISS SIMCOP Hardware Sequencer and Buffers Register Manual: [3] [4]

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Table 8-1298. SIMCOP_HWSEQ_STEP_SWITCH_i

Address Offset	0x0000 0084 + (0x10 * i)		
Physical Address	0x5202 0084 + (0x10 * i) 0x5506 0084 + (0x10 * i)	**Instance**	HWSEQ_L3 HWSEQ_CORTEX-M3
Description	Image buffer switch control. The configuration of step #0 is used when hardware sequencer is idle.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IMBUFF_H				IMBUFF_G				RESERVED	IMBUFF_F			RESERVED	IMBUFF_E			RESERVED	IMBUFF_D			RESERVED	IMBUFF_C			RESERVED	IMBUFF_B			RESERVED	IMBUFF_A		

Bits	Field Name	Description	Type	Reset
31:28	IMBUFF_H	Switch for image buffer h 0x0: Coprocessor bus 0x1: SIMCOP DMA 0x2: iMX A 0x3: iMX B 0x4: VLCDJ_IO 0x5: DCT_S 0x6: DCT_F 0x7: ROT_A_O 0x8: NSF_IO 0x9: LDC_O	RW	0x0
27:24	IMBUFF_G	Switch for image buffer g 0x0: Coprocessor bus 0x1: SIMCOP DMA 0x2: iMX A 0x3: iMX B 0x4: VLCDJ_IO 0x5: DCT_S 0x6: DCT_F 0x7: ROT_A_O 0x8: NSF_IO 0x9: LDC_O	RW	0x0
23	RESERVED	Read returns 0.	R	0
22:20	IMBUFF_F	Switch for image buffer f 0x0: Coprocessor bus 0x1: SIMCOP DMA 0x2: iMX A 0x3: iMX B 0x4: DCT_S 0x5: NSF_IO 0x6: LDC_O 0x7: ROT_A_O	RW	0x0
19	RESERVED	Read returns 0.	R	0
18:16	IMBUFF_E	Switch for image buffer e 0x0: Coprocessor bus 0x1: SIMCOP DMA	RW	0x0

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Bits	Field Name	Description	Type	Reset
		0x2: iMX A 0x3: iMX B 0x4: DCT_S 0x5: NSF_IO 0x6: LDC_O 0x7: ROT_A_O		
15	RESERVED	Read returns 0.	R	0
14:12	IMBUFF_D	Switch for image buffer d 0x0: Coprocessor bus 0x1: SIMCOP DMA 0x2: iMX A 0x3: iMX B 0x4: VLCDJ_IO 0x5: DCT_F 0x6: ROT_A_I 0x7: Reserved	RW	0x0
11	RESERVED	Read returns 0.	R	0
10:8	IMBUFF_C	Switch for image buffer c. 0x0: Coprocessor bus 0x1: SIMCOP DMA 0x2: iMX A 0x3: iMX B 0x4: VLCDJ_IO 0x5: DCT_F 0x6: ROT_A_I 0x7: Reserved	RW	0x0
7	RESERVED	Read returns 0.	R	0
6:4	IMBUFF_B	Switch for image buffer b. 0x0: Coprocessor bus 0x1: SIMCOP DMA 0x2: iMX A IMBUFF 0x3: iMX B IMBUFF 0x4: VLCDJ_IO 0x5: DCT_F 0x6: ROT_A_I 0x7: Reserved	RW	0x0
3	RESERVED	Read returns 0.	R	0
2:0	IMBUFF_A	Switch for image buffer a 0x0: Coprocessor bus 0x1: SIMCOP DMA 0x2: iMX A IMBUFF 0x3: iMX B IMBUFF 0x4: VLCDJ_IO 0x5: DCT_F 0x6: ROT_A_I 0x7: Reserved	RW	0x0

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Table 8-1299. Register Call Summary for Register SIMCOP_HWSEQ_STEP_SWITCH_i

ISS Still Image Coprocessor

- ISS SIMCOP Hardware Sequencer and Buffers Functional Description: [0] [1]
- ISS SIMCOP Hardware Sequencer and Buffers Basic Programming Model: [2] [3] [4] [5] [6] [7] [8]
- ISS SIMCOP Hardware Sequencer and Buffers Register Manual: [9]

Table 8-1300. SIMCOP_HWSEQ_STEP_IMX_CTRL_i

Address Offset	0x0000 0088 + (0x10 * i)		
Physical Address	0x5202 0088 + (0x10 * i) 0x5506 0088 + (0x10 * i)	**Instance**	HWSEQ_L3 HWSEQ_CORTEX-M3
Description	Hardware sequencer step control register The configuration of step #0 is used when hardware sequencer is idle.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IMX_B_SYNC	RESERVED							IMX_B_START								IMX_A_SYNC	RESERVED							IMX_A_START							

Bits	Field Name	Description	Type	Reset
31	IMX_B_SYNC	Enable hardware synchronization with the iMX B module 0x0: Disabled 0x1: Enabled.	RW	0
30:29	RESERVED	Read returns 0.	R	0x0
28:16	IMX_B_START	This register is only used when SIMCOP_HWSEQ_STEP_IMX_CTRL_i[31] IMX_B_SYNC=1. It contains the address, in 16-bit words, of the first instruction iMX will execute when it gets started.	RW	0x0000
15	IMX_A_SYNC	Enable hardware synchronization with the iMX A module 0x0: Disabled 0x1: Enabled.	RW	0
14:13	RESERVED	Read returns 0.	R	0x0
12:0	IMX_A_START	This register is only used when SIMCOP_HWSEQ_STEP_IMX_CTRL_i[15] IMX_A_SYNC=1. It contains the address, in 16-bit words, of the first instruction iMX will execute when it gets started.	RW	0x0000

Table 8-1301. Register Call Summary for Register SIMCOP_HWSEQ_STEP_IMX_CTRL_i

ISS Still Image Coprocessor

- ISS SIMCOP Hardware Sequencer and Buffers Register Manual: [0] [1] [2]

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Table 8-1302. SIMCOP_HWSEQ_STEP_CTRL2_i

Address Offset	0x0000 008C + (0x10 * i)		
Physical Address	0x5202 008C + (0x10 * i) 0x5506 008C + (0x10 * i)	**Instance**	HWSEQ_L3 HWSEQ_CORTEX-M3
Description	Hardware sequencer step control register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				NSF2_IO_OFST		LDC_O_OFST		RESERVED				RESERVED			
																									COEFF_B				COEFF_A		

Bits	Field Name	Description	Type	Reset
31:12	RESERVED	Read returns 0.	R	0x00000
11:10	NSF2_IO_OFST	Controls NSF_IO bus mapping to image buffers: 0x0000 0x1000 0x0: EF 0x1: FG 0x2: GH 0x3: HE	RW	0x0
9:8	LDC_O_OFST	Controls LDC.O bus mapping to image buffers: 0x0000 0x1000 0x2000 0x3000 0x0: EFGH 0x1: FGHE 0x2: GHEF 0x3: HEFG	RW	0x0
7	RESERVED	Read returns 0.	R	0
6:4	COEFF_B	Coefficient buffer b switch 0x0: Coprocessor bus 0x1: SIMCOP DMA 0x2: iMX A 0x3: iMX B 0x4: VLCDJ_IO 0x5: DCT_F 0x6: ROT A O 0x7: Reserved	RW	0x0
3	RESERVED	Read returns 0.	R	0
2:0	COEFF_A	Coefficient buffer a switch 0x0: Coprocessor bus 0x1: SIMCOP DMA 0x2: iMX A 0x3: iMX B 0x4: VLCDJ_IO 0x5: DCT_F 0x6: ROT A I 0x7: Reserved	RW	0x0

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Table 8-1303. Register Call Summary for Register SIMCOP_HWSEQ_STEP_CTRL2_i

ISS Still Image Coprocessor

- ISS SIMCOP Hardware Sequencer and Buffers Functional Description: [0]
- ISS SIMCOP Hardware Sequencer and Buffers Basic Programming Model: [1] [2] [3] [4] [5] [6] [7] [8] [9]
- ISS SIMCOP Hardware Sequencer and Buffers Register Manual: [10]

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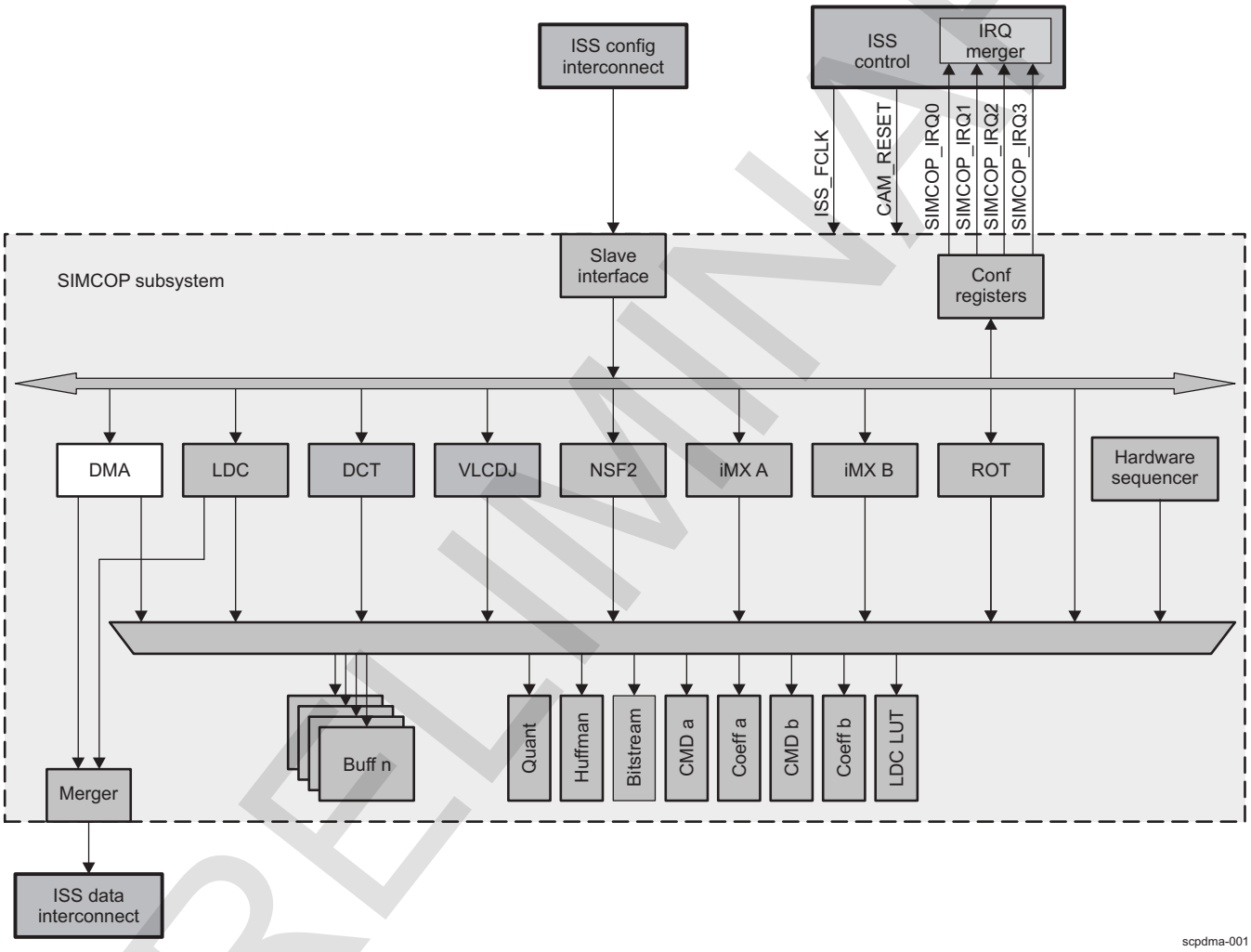
8.4.3 ISS SIMCOP DMA Module

This section describes the direct memory access (DMA) module in the still image coprocessor (SIMCOP) subsystem.

8.4.3.1 ISS SIMCOP DMA Overview

The direct memory access (DMA) module transfers data from system memory to the still image coprocessor (SIMCOP) memories and from SIMCOP memories. Figure 8-259 is an overview of the DMA module in the SIMCOP subsystem.

Figure 8-259. DMA in the SIMCOP Subsystem



The SIMCOP DMA supports the following features:

- Configuration interface, for register access
- Imaging subsystem (ISS) data interconnect master interface, for system memory access
  - Supports 1-dimensional (1D) and 2-dimensional (2D) burst
- SIMCOP crossbar master interface, for SIMCOP memories access
- Eight logical channels supported
- Hardware synchronization support
- 4-dimensional (4D) addressing modes
- 2D data block transfer (base address, stride, height, width)
- Array of 2D block transfer support

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- Performance: Software-controllable bandwidth limiter

8.4.3.2 ISS SIMCOP DMA Integration

The DMA module is part of the SIMCOP subsystem in the ISS. Figure 8-260 shows the integration of the DMA in the SIMCOP sybsystem.

Table 8-1304,Table 8-1305, and Table 8-1306 list the SIMCOP DMA integration attributes, clocks and resets, and hardware requests, respectively.

Figure 8-260. DMA Engine Integration

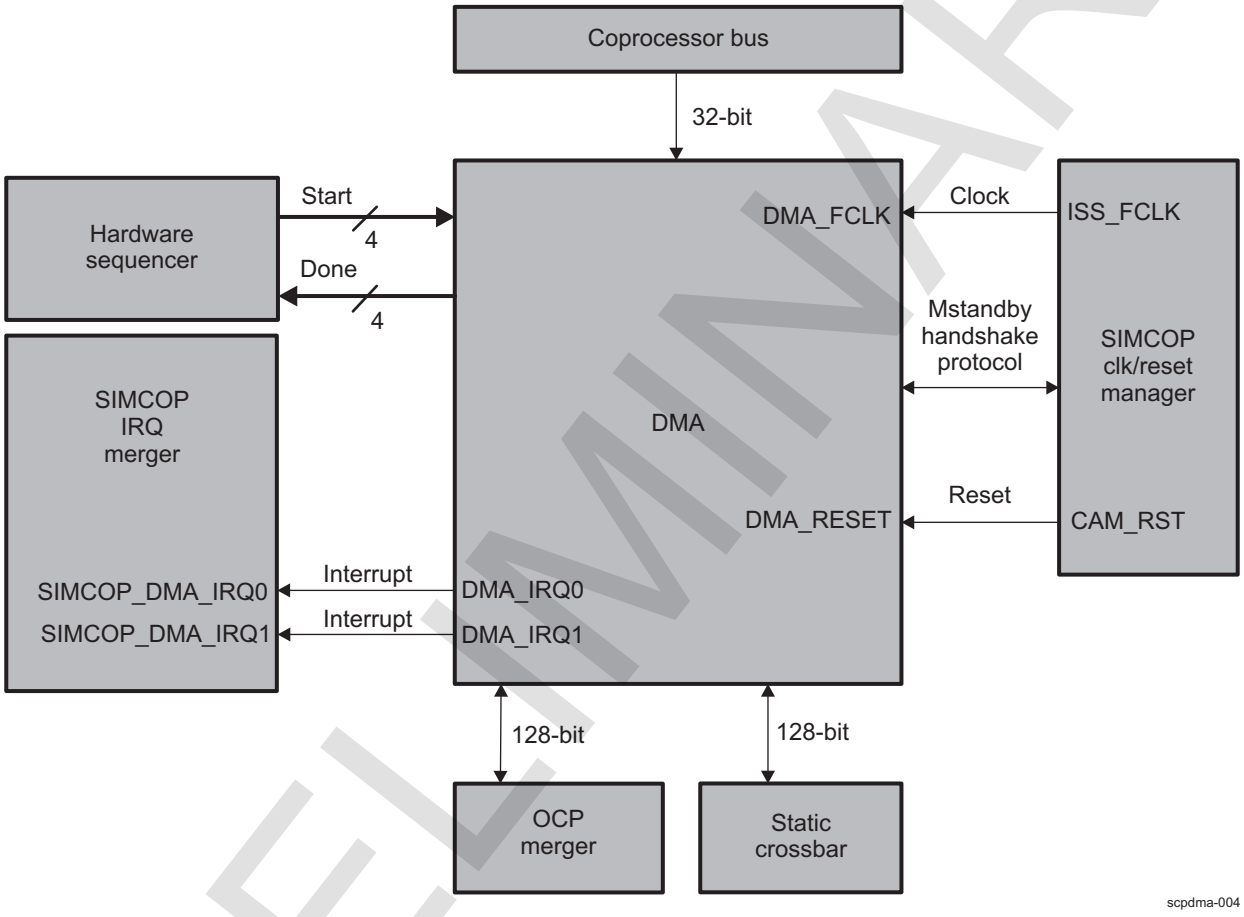

Table 8-1304. Integration Attributes

Module Instance	Attributes	
	Power Domain	Interconnect
DMA	PD_CAM	

Table 8-1305. Clocks and Resets

Clocks				
Module Instance	Destination Signal Name	Source Signal Name	Source	Description
DMA	DMA_FCLK	ISS_FCLK	PRCM	Functional clock provided by ISS_CLK from the PRCM module. It is used by all ISS submodules and ISS top-level resources.
Resets				

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Table 8-1305. Clocks and Resets (continued)

Module Instance	Destination Signal Name	Source Signal Name	Source	Description
DMA	DMA_RESET	CAM_RST	PRCM	ISS and SIMCOP global reset

For information about clock and reset management, see Section 8.4.1.2.1, *ISS SIMCOP Local Power and Clock Management*.

Table 8-1306. Hardware Requests

		Interrupt Requests		
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
DMA	DMA_IRQ0	SIMCOP_DMA_IRQ0	SIMCOP IRQ merger	Interrupt triggered by SIMCOP DMA
DMA	DMA_IRQ1	SIMCOP_DMA_IRQ1	SIMCOP IRQ merger	Interrupt triggered by SIMCOP DMA

For more information about interrupt requests, see Section 8.4.1.2.3, *Interrupt Merger*.

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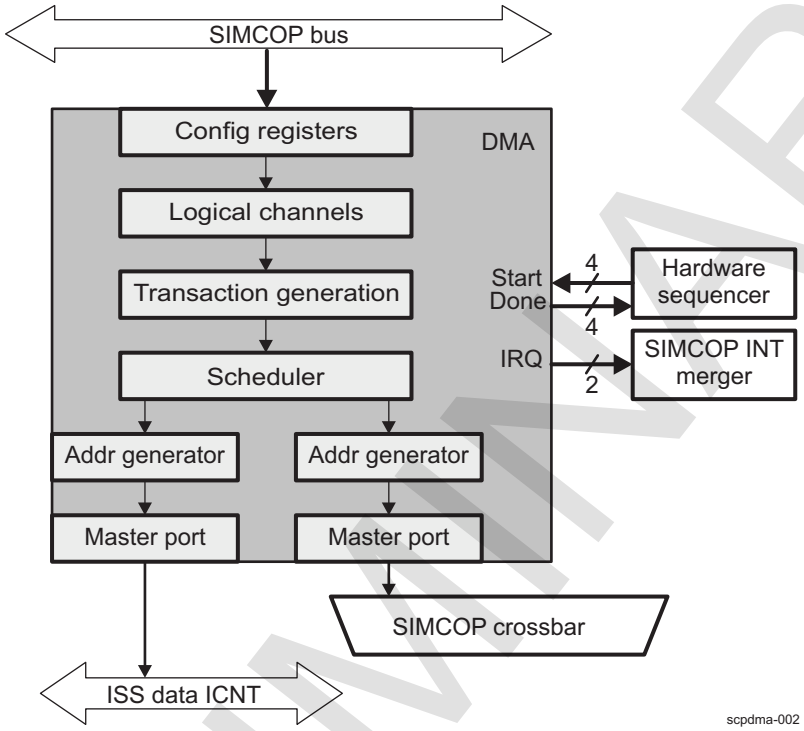
8.4.3.3 ISS SIMCOP DMA Functional Description

8.4.3.3.1 ISS SIMCOP DMA Block Diagram

Figure 8-261 is a block diagram of the SIMCOP DMA.

Figure 8-261. DMA Block Diagram



An external initiator sets up logical channels using the configuration interface.

When a logical channel becomes active, a transfer must be executed. A transfer corresponds to a 2D block of data copied from system memory to SIMCOP memory and vice versa.

A transfer is decomposed into one or multiple transactions by the transaction generation unit.

The scheduler issues transactions when tags are available. There can be one outstanding command per tag on the ISS data interconnect.

8.4.3.3.2 ISS SIMCOP DMA Power Management

Table 8-1307 lists the power-management features available in the DMA module.

Table 8-1307. Local Power-Management Features

Feature	Registers	Description
Master standby modes	SIMCOP_DMA_SYSCONFIG[5:4] STANDBYMODE	Force-standby, no-standby, and smart-standby modes are available.

8.4.3.3.3 ISS SIMCOP DMA Interrupt Requests

The SIMCOP DMA module can generate two interrupts, SIMCOP_DMA_IRQ0 and SIMCOP_DMA_IRQ1. These two interrupts are controlled by four registers:

- SIMCOP_DMA_IRQSTATUS_RAW_j: The status of the interrupt before masking
- SIMCOP_DMA_IRQSTATUS_j: The status of the interrupt after masking
- SIMCOP_DMA_IRQENABLE_SET_j: Enable an interrupt to propagate to SIMCOP_DMA_IRQi signal

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(unmask)

- SIMCOP_DMA_IRQENABLE_CLR_j: Disable an interrupt to propagate to SIMCOP_DMA_IRQi signal (mask)

To clear an interrupt, software must write 1 in the corresponding bit of the SIMCOP_DMA_IRQSTATUS_j register even if the event is not enabled (SIMCOP_DMA_IRQSTATUS_RAW_j is also cleared).

Table 8-1308 lists all the SIMCOP DMA events that can lead to an interrupt generation.

Table 8-1308. SIMCOP DMA Events List

Bit Name	Bit	Event
BUS_ERR	0	Error occurred on bus
CHAN0_BLOCK_DONE_IRQ	16	Channel 0 has completed transfer of one 2D block.
CHAN1_BLOCK_DONE_IRQ	17	Channel 1 has completed transfer of one 2D block.
CHAN2_BLOCK_DONE_IRQ	18	Channel 2 has completed transfer of one 2D block.
CHAN3_BLOCK_DONE_IRQ	19	Channel 3 has completed transfer of one 2D block.
CHAN4_BLOCK_DONE_IRQ	20	Channel 4 has completed transfer of one 2D block.
CHAN5_BLOCK_DONE_IRQ	21	Channel 5 has completed transfer of one 2D block.
CHAN6_BLOCK_DONE_IRQ	22	Channel 6 has completed transfer of one 2D block.
CHAN7_BLOCK_DONE_IRQ	23	Channel 7 has completed transfer of one 2D block.
CHAN0_FRAME_DONE_IRQ	24	Channel 0 has completed transfer of the full frame.
CHAN1_FRAME_DONE_IRQ	25	Channel 1 has completed transfer of the full frame.
CHAN2_FRAME_DONE_IRQ	26	Channel 2 has completed transfer of the full frame.
CHAN3_FRAME_DONE_IRQ	27	Channel 3 has completed transfer of the full frame.
CHAN4_FRAME_DONE_IRQ	28	Channel 4 has completed transfer of the full frame.
CHAN5_FRAME_DONE_IRQ	29	Channel 5 has completed transfer of the full frame.
CHAN6_FRAME_DONE_IRQ	30	Channel 6 has completed transfer of the full frame.
CHAN7_FRAME_DONE_IRQ	31	Channel 7 has completed transfer of the full frame.

8.4.3.3.4 ISS SIMCOP DMA Logical Channels

In the context of SIMCOP, multiple logical channels are required to offload the external initiator. Typical uses of multiple context are:

- Run a read transfer followed by a write transfer. That is the required mode to operate the NSF2 module. When the NSF2 completes processing, filtering outcome is first copied from the image buffers to system memory. When this transfer completes, new input data is fetched from system memory and stored in the image buffers.
- Read or write YUV4:2:0 data from system memory; YUV4:2:0 data is stored in two different system memory buffers.

8.4.3.3.4.1 Logical Channel States

The SIMCOP DMA supports up to eight ((SIMCOP_DMA_HWINFO[2] CHAN + 1)*4) logical channels. Each logical channel can be configured and triggered separately.

Idle logical channels must be configured and enabled (SIMCOP_DMA_CHAN_CTRL_i[0] ENABLE = 1) to be used.

Figure 8-262 shows the different states of a logical channel. Software can poll the current state from the SIMCOP_DMA_CHAN_CTRL_i[4:3] STATUS bit field.

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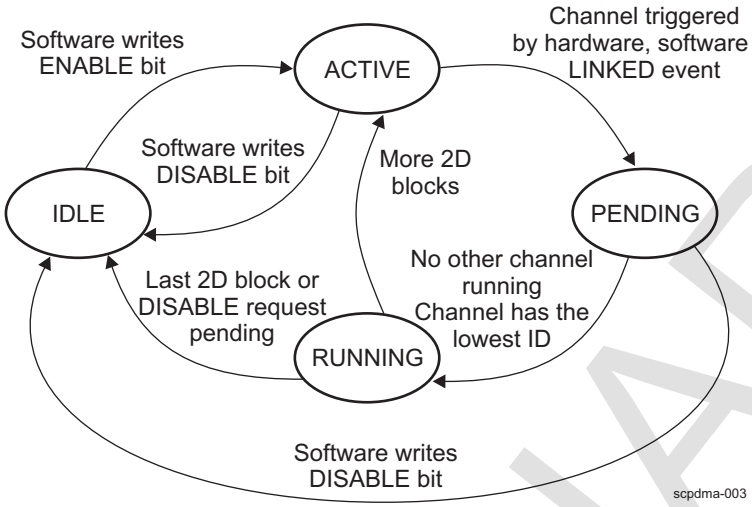
Figure 8-262. DMA Logical Channel States



When a trigger event is received by a channel in the ACTIVE state, it moves to the PENDING state. Trigger events received when the channel is in the IDLE, PENDING, or RUNNING state are discarded.

A logical channel is automatically disabled by hardware when a complete frame (all 2D blocks) is transferred. It can be disabled earlier by software by writing the SIMCOP_DMA_CHAN_CTRL_i[1] DISABLE bit. When a disable request occurs in the RUNNING state, it is memorized and executed when the channel leaves the RUNNING state. Pending disable requests have higher priority than channel trigger events.

When multiple logical channels are pending simultaneously, the following rules apply:

- An ongoing transfer of a 2D block is never stopped. It must complete before the next one starts.
- The logical channel with the lowest ID wins the arbitration (that is, CHAN0 has higher priority than CHAN1). Software can give higher priority to a channel by choosing a lower ID.

This situation can, for example, occur when software triggers a channel while a transfer is ongoing for another channel. Two types of interrupts can be generated:

- CHANx_BLOCK_DONE_IRQ (where x = channel number) is generated when the channel leaves the RUNNING state (RUNNING - ACTIVE or RUNNING - IDLE).
- CHANx_FRAME_DONE_IRQ (where x = channel number) is generated when the channel enters the IDLE state.

8.4.3.3.4.2 Logical Channel Chaining, Trigger, and Hardware Synchronization

Active logical channels can be triggered:

- By software. Writes the SIMCOP_DMA_CHAN_CTRL_i[2] SWTRIGGER bit
- By a hardware DMA request. A channel can be made sensitive to a pulse on the START[y] input when SIMCOP_DMA_CHAN_CTRL_i[19:17] HWSTART = y has been configured by software.
- When the previous channel in the linked list finishes. This feature is enabled through the SIMCOP_DMA_CHAN_CTRL_i[16:12] LINKED bit field of the preceding channel in the chain.

When a channel completes, it can optionally send a pulse to the DONE[y] output. Software enables this feature by configuring SIMCOP_DMA_CHAN_CTRL_i[22:20] HWSTOP = y.

Typically, the START + DONE synchronization mechanism is used together with the SIMCOP hardware sequencer. The hardware sequencer sends a pulse to START[y] a data transfer and the SIMCOP DMA responds with a DONE[y] pulse when the transfer completes. A transfer can be composed of one or multiple logical channels. For example, a YUV4:2:0-NV12 block copy from system memory to SIMCOP local memories requires two chained logical channels.

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Software must ensure that only one trigger event source is selected at a given time for a logical channel; otherwise, unpredictable behavior may occur.

Typically, the following combinations can be used:

- Single channel triggered by software: Hardware synchronization and linking are disabled. Software writes the SIMCOP_DMA_CHAN_CTRL_i[2] SWTRIGGER bit to start the transfer of one 2D block. Software must not trigger the channel again before the CHANx_BLOCK_DONE_IRQ (where x = channel number) event is generated by the DMA.
- Channels chain-triggered by software: Multiple channels are linked together using the SIMCOP_DMA_CHAN_CTRL_i[16:12] LINKED bit field. Software triggers the first one in the chain and monitors the CHANx_BLOCK_DONE_IRQ (where x = channel number) event to know when the chain can be triggered again.
- Single channel triggered by hardware synchronization: Sensitivity on START pulses is activated through the SIMCOP_DMA_CHAN_CTRL_i[19:17] HWSTART bit field. DONE pulses are activated using the SIMCOP_DMA_CHAN_CTRL_i[22:20] HWSTOP bit field.
- Channels chain-triggered by hardware: Multiple channels are linked together using the SIMCOP_DMA_CHAN_CTRL_i[16:12] LINKED bit field. Sensitivity on START pulses is activated for the first channel in the chain through the SIMCOP_DMA_CHAN_CTRL_i[19:17] HWSTART bit field. DONE pulses for the last channel in the chain are activated using the SIMCOP_DMA_CHAN_CTRL_i[22:20] HWSTOP bit field.

8.4.3.3.4.3 Logical Channel Data Transfer

Each logical channel can handle 4D transfers from system memory to SIMCOP memory and vice versa.

A frame is composed of SIMCOP_DMA_CHAN_FRAME_i[9:0] XCNT * SIMCOP_DMA_CHAN_FRAME_i[25:16] YCNT 2D blocks of data. One 2D block of data is transferred each time a logical channel is in the RUNNING state.

The size of a 2D block is SIMCOP_DMA_CHAN_BLOCK_SIZE_i[13:4] XNUM * SIMCOP_DMA_CHAN_BLOCK_SIZE_i[28:16] YNUM words of 128 bits. The SIMCOP DMA can transfer only full 128-bit words.

2D blocks may overlap in system memory. This feature is typically used for source data fetches from system memory to handle filter dependencies. If this feature is not used, software must set:

- SIMCOP_DMA_CHAN_BLOCK_SIZE_i[13:4] XNUM = SIMCOP_DMA_CHAN_BLOCK_STEP_i[14:4] XSTEP
- SIMCOP_DMA_CHAN_BLOCK_SIZE_i[28:16] YNUM = SIMCOP_DMA_CHAN_BLOCK_STEP_i[29:16] YSTEP

Figure 8-263 shows DMA addressing.

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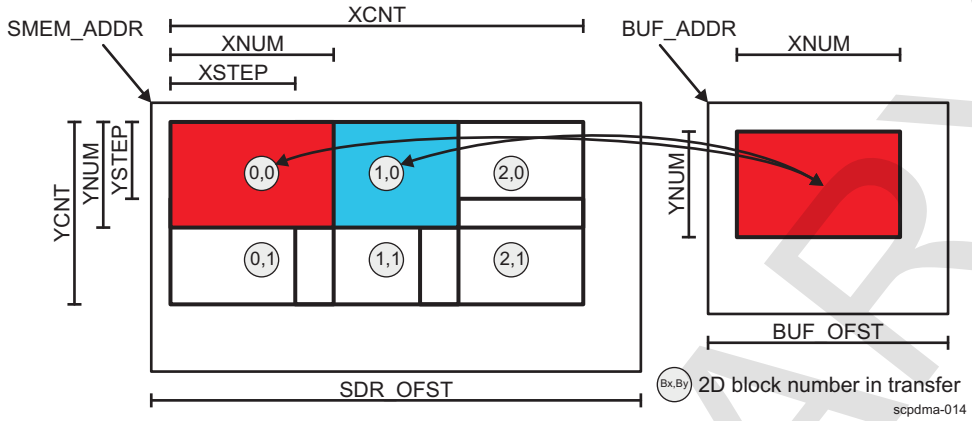
Figure 8-263. DMA Addressing



The base position of 2D blocks in system memory is automatically computed by the SIMCOP DMA. The base address is computed using the following formula:

SMEM_BASE = SIMCOP_DMA_CHAN_SMEM_ADDR_i[31:4] ADDR +
Bx * SIMCOP_DMA_CHAN_BLOCK_STEP_i[14:4] XSTEP +
By * SIMCOP_DMA_CHAN_BLOCK_STEP_i[29:16] YSTEP *
SIMCOP_DMA_CHAN_SMEM_OFST_i[19:4] OFST

All 2D blocks of a logical channel have the same location in SIMCOP local memories:

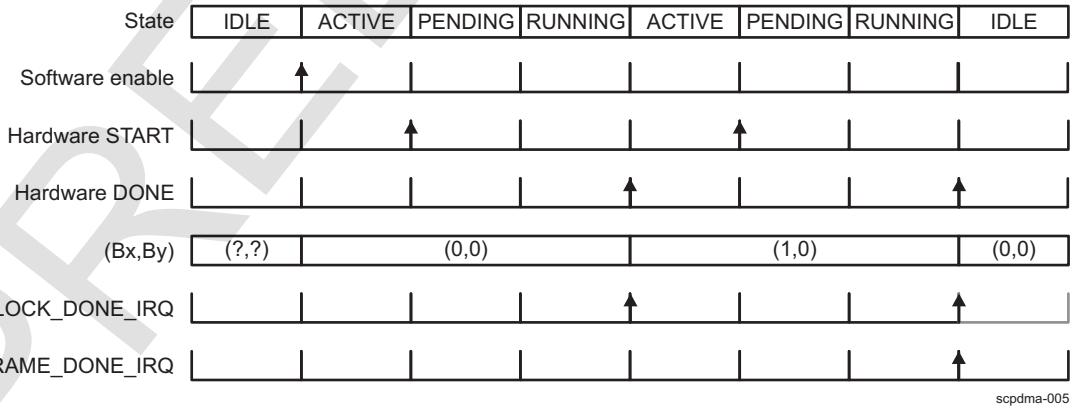
BUF_BASE = SIMCOP_DMA_CHAN_BUF_ADDR_i[23:4] ADDR

The same functionality can also be used to read or write sparse data from synchronous dynamic random access memory (SDRAM). Typically, that is useful to split processing between two SIMCOP accelerators (that is, iMX).

Software can poll the status of a channel using the SIMCOP_DMA_CHAN_CURRENT_BLOCK_i register. It holds the Bx, By values of the last-transferred 2D block. The Bx, By values are reset when a channel is enabled (set the SIMCOP_DMA_CHAN_CTRL_i[0] ENABLE bit) and they are updated when a channel enters the RUNNING state.

Figure 8-264 shows an example of a 2-block large transfer.

Figure 8-264. 2-Block Large Transfer Example



8.4.3.3.5 Transaction Generation

Each transfer is decomposed into one or multiple transactions by the DMA engine. The firmware can define:

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- Burst generation for regular or tiled accesses (SIMCOP_DMA_CHAN_CTRL_i[6] TILERMODE). Additional parameters must be defined for tiled accesses. See Section 8.4.3.3.5.2, *Block Bursts for Tiled Transfers*.
- The maximum burst size (SIMCOP_DMA_CTRL[1:0] MAX_BURST_SIZE). It must be aligned with the interconnect configuration.
- Use of posted or nonposted writes (SIMCOP_DMA_CTRL[3] POSTED_WRITES). It must be aligned with the interconnect configuration. Mainly, in a multichannel system memory, system bursts must be issued nonposted.

8.4.3.3.5.1 Incrementing Bursts for Regular Transfers

Lines of 2D blocks are processed sequentially. The following transaction process is used for a given line:

1. Perform a single nonaligned burst from the start address to the next SIMCOP_DMA_CTRL[1:0] MAX_BURST_SIZE boundary (or less if the transfer is smaller).
2. Perform "n" aligned bursts (n can be 0).
3. Perform a single nonaligned burst up to the end address (if needed).

A transaction is aligned when the start address modulo burst length is 0.

8.4.3.3.5.2 Block Bursts for Tiled Transfers

The line stride is configured using the SIMCOP_DMA_CHAN_SMEM_OFST_i[19:4] OFST bit field. The full register content is used for internal address computation. The SIMCOP_DMA_CHAN_SMEM_OFST_i[19:4] OFST bit field must be a multiple of the SIMCOP_DMA_CTRL[1:0] MAX_BURST_SIZE bit field.

The SIMCOP DMA has the following alignment constraints:

- SIMCOP_DMA_CHAN_SMEM_ADDR_i[31:4] ADDR is 128 bit-aligned.
- SIMCOP_DMA_CHAN_BLOCK_SIZE_i[13:4] XNUM is 128 bit-aligned.

Only the values in Table 8-1309 are allowed for the SIMCOP_DMA_CTRL[1:0] MAX_BURST_SIZE bit field. Other values lead to undefined behavior.

Table 8-1309. Allowed Maximum Burst Size

Minimum Burst Height	MAX_BURST_SIZE
2	2, 4, or 8 x 128 bits
4	4 or 8 x 128 bits

8.4.3.4 ISS SIMCOP DMA Basic Programming Model

8.4.3.4.1 Initialization of Surrounding Modules

To initialize the DMA, the surrounding modules must be initialized. Table 8-1310 lists these modules.

Table 8-1310. Initialization of Surrounding Modules

Module	Minimum Required Setting	Optional Settings
CLKC	Enable SIMCOP clock.	
Buffers	Configure DMA access to image buffer.	
SIMCOP CTRL		Configure SIMCOP CTRL to handle DMA interrupts.

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8.4.3.4.2 ISS SIMCOP DMA Channel Configuration and Hardware Synchronization

Software must fully configure a DMA channel before enabling it. It then configures channel linking and the used synchronization method.

The following example shows four logical channels chained with hardware synchronization used to copy YUV4:2:0-NV12 data from SIMCOP local memories to system memory, and then to copy YUV4:2:0-NV12 data from system memory to SIMCOP local memories.

YUV4:2:0-NV12 data is stored in two separate buffers in SDRAM. Therefore, two channels are used for the SIMCOP - system copy, and two channels are used for the system - SIMCOP copy.

In this example, the intent is to transfer a 2 x 2 array of 64 x 32 pixel blocks. It is assumed that input data is stored contiguously in system memory and that the output buffer size in system memory is 256 x 32 pixels. In SIMCOP local memories, data is contiguously stored starting at address 0.

The following configuration is used:

- Channel i = 0, input Y buffer:
  - SIMCOP_DMA_CHAN_SMEM_ADDR_i[31:4] ADDR = Start address of Y input buffer
  - SIMCOP_DMA_CHAN_SMEM_OFST_i[19:4] OFST = 16 (= 256 bytes)
  - SIMCOP_DMA_CHAN_BUF_ADDR_i[23:4] ADDR = 0
  - SIMCOP_DMA_CHAN_BUF_OFST_i[23:4] OFST = 8 (= 128 bytes)
  - SIMCOP_DMA_CHAN_BLOCK_SIZE_i[13:4] XNUM = 4 (= 64 bytes)
  - SIMCOP_DMA_CHAN_BLOCK_SIZE_i[28:16] YNUM = 32
  - SIMCOP_DMA_CHAN_FRAME_i[9:0] XCNT = 2
  - SIMCOP_DMA_CHAN_FRAME_i[25:16] YCNT = 2
  - SIMCOP_DMA_CHAN_BLOCK_STEP_i[14:4] XSTEP = 4 (= 64 bytes)
  - SIMCOP_DMA_CHAN_BLOCK_STEP_i[29:16] YSTEP = 32
- Channel i = 1, input UV buffer:
  - SIMCOP_DMA_CHAN_SMEM_ADDR_i[31:4] ADDR = Start address of UV input buffer
  - SIMCOP_DMA_CHAN_SMEM_OFST_i[19:4] OFST = 16 (= 256 bytes)
  - SIMCOP_DMA_CHAN_BUF_ADDR_i[23:4] ADDR = 128 (2KB)
  - SIMCOP_DMA_CHAN_BUF_OFST_i[23:4] OFST = 8 (= 128 bytes)
  - SIMCOP_DMA_CHAN_BLOCK_SIZE_i[13:4] XNUM = 4 (= 64 bytes)
  - SIMCOP_DMA_CHAN_BLOCK_SIZE_i[28:16] YNUM = 16
  - SIMCOP_DMA_CHAN_FRAME_i[9:0] XCNT = 2
  - SIMCOP_DMA_CHAN_FRAME_i[25:16] YCNT = 2
  - SIMCOP_DMA_CHAN_BLOCK_STEP_i[14:4] XSTEP = 4 (= 64 bytes)
  - SIMCOP_DMA_CHAN_BLOCK_STEP_i[29:16] YSTEP = 16
- Channel i = 2, output Y buffer:
  - SIMCOP_DMA_CHAN_SMEM_ADDR_i[31:4] ADDR = Start address of Y output buffer
  - SIMCOP_DMA_CHAN_SMEM_OFST_i[19:4] OFST = 16 (= 256 bytes)
  - SIMCOP_DMA_CHAN_BUF_ADDR_i[23:4] ADDR = 0
  - SIMCOP_DMA_CHAN_BUF_OFST_i[23:4] OFST = 8 (= 128 bytes)
  - SIMCOP_DMA_CHAN_BLOCK_SIZE_i[13:4] XNUM = 4 (= 64 bytes)
  - SIMCOP_DMA_CHAN_BLOCK_SIZE_i[28:16] YNUM = 32
  - SIMCOP_DMA_CHAN_FRAME_i[9:0] XCNT = 2
  - SIMCOP_DMA_CHAN_FRAME_i[25:16] YCNT = 2
  - SIMCOP_DMA_CHAN_BLOCK_STEP_i[14:4] XSTEP = 4 (= 64 bytes)
  - SIMCOP_DMA_CHAN_BLOCK_STEP_i[29:16] YSTEP = 32
- Channel i = 3, output UV buffer:

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- SIMCOP_DMA_CHAN_SMEM_ADDR_i[31:4] ADDR = Start address of UV output buffer
- SIMCOP_DMA_CHAN_SMEM_OFST_i[19:4] OFST = 16 (= 256 bytes)
- SIMCOP_DMA_CHAN_BUF_ADDR_i[23:4] ADDR = 128 (= 2KB)
- SIMCOP_DMA_CHAN_BUF_OFST_i[23:4] OFST = 8 (= 128 bytes)
- SIMCOP_DMA_CHAN_BLOCK_SIZE_i[13:4] XNUM = 4 (= 64 bytes)
- SIMCOP_DMA_CHAN_BLOCK_SIZE_i[28:16] YNUM = 16
- SIMCOP_DMA_CHAN_FRAME_i[9:0] XCNT = 2
- SIMCOP_DMA_CHAN_FRAME_i[25:16] YCNT = 2
- SIMCOP_DMA_CHAN_BLOCK_STEP_i[14:4] XSTEP = 4 (= 64 bytes)
- SIMCOP_DMA_CHAN_BLOCK_STEP_i[29:16] YSTEP = 16

Figure 8-265 shows the channel linking chain used. All four channels are executed sequentially. Doing so prevents access collision in SIMCOP local memories or system memories. Channel 0 is started by a START[0] pulse from SIMCOP. When Channel 3 completes the last transfer, a pulse to DONE[0] is sent back to SIMCOP.

Figure 8-266 shows the temporal channel sequence.

Figure 8-265. YUV4:2:0-NV12 Read/Write Chain

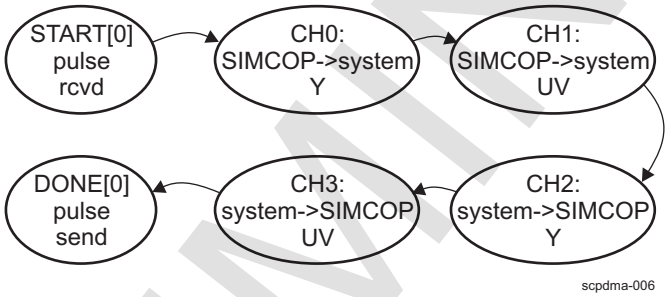
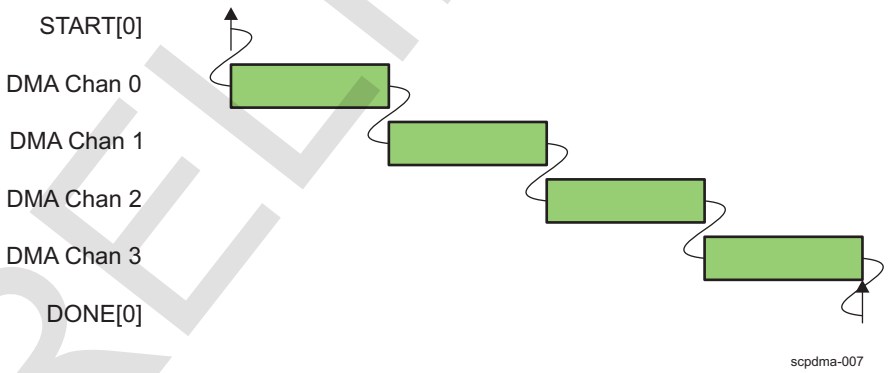


Figure 8-266. Temporal Channel Sequence



The following configuration is used for each channel:

- Channel i = 0, input Y buffer, first in sequence:
  - SIMCOP_DMA_CHAN_CTRL_i[16:12] LINKED = 0x11 (= CHAN1)
  - SIMCOP_DMA_CHAN_CTRL_i[19:17] HWSTART = 0x4 (= CHAN0)
  - SIMCOP_DMA_CHAN_CTRL_i[5] DIR = 1 (=SIMCOP buffers - system memory)
  - SIMCOP_DMA_CHAN_CTRL_i[0] ENABLE = 1
- Channel i = 1, input UV buffer, second in sequence:
  - SIMCOP_DMA_CHAN_CTRL_i[16:12] LINKED = 0x12 (= CHAN2)
  - SIMCOP_DMA_CHAN_CTRL_i[5] DIR = 1 (= SIMCOP buffers - system memory)
  - SIMCOP_DMA_CHAN_CTRL_i[0] ENABLE = 1

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- Channel i = 2, output Y buffer, third in sequence:
  - SIMCOP_DMA_CHAN_CTRL_i[16:12] LINKED = 0x13 (= CHAN3)
  - SIMCOP_DMA_CHAN_CTRL_i[5] DIR = 0 (= system memory - SIMCOP buffers)
  - SIMCOP_DMA_CHAN_CTRL_i[0] ENABLE = 1
- Channel i = 3, output UV buffer, last in sequence:
  - SIMCOP_DMA_CHAN_CTRL_i[16:12] LINKED = 0x00 (no link)
  - SIMCOP_DMA_CHAN_CTRL_i[22:20] HWSTART = 0x4 (= CHAN0)
  - SIMCOP_DMA_CHAN_CTRL_i[5] DIR = 0 (= system memory - SIMCOP buffers)
  - SIMCOP_DMA_CHAN_CTRL_i[0] ENABLE = 1

Software can read the status of a logical channel at any time. However, logical channel configuration registers can be changed only when the channel is in the IDLE state.

Software can disable a logical channel by writing the SIMCOP_DMA_CHAN_CTRL_i[1] DISABLE bit. A channel is effectively disabled when SIMCOP_DMA_CHAN_CTRL_i[4:3] STATUS = IDLE. In case of linked channels, software must disable all channels in the chain and wait until all of them are back in the IDLE state before channels can be reprogrammed.

8.4.3.4.3 Software Synchronization

Software performs the following sequence:

1. Configures the channel
2. Enables the channel
3. Triggers the channel by writing the SIMCOP_DMA_CHAN_CTRL_i[2] SWTRIGGER bit
4. Waits for BLOCK_DONE_IRQ

Step 2 and Step 4 are repeated until all 2D blocks have been transferred.

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8.4.3.5 ISS SIMCOP DMA Register Manual

8.4.3.5.1 ISS SIMCOP DMA Instance Summary

Table 8-1311 summarizes the DMA instance.

Table 8-1311. SIMCOP DMA Instance Summary

Module Name	Base Address L3 Interconnect	Base Address Cortex-M3 Private Access	Size
DMA	0x5202 0200	0x5506 0200	512 bytes

NOTE: Private Access is an access that does not use the L3/L4 interconnects.

8.4.3.5.2 ISS SIMCOP DMA Registers

8.4.3.5.2.1 ISS SIMCOP DMA Register Summary

Table 8-1312 summarizes the SIMCOP DMA register mapping.

Table 8-1312. DMA Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	Physical Address L3 Interconnect	Physical Address Cortex-M3 Private Access
SIMCOP_DMA_REVISION	R	32	0x0000 0000	0x5202 0200	0x5506 0200
SIMCOP_DMA_HWINFO	R	32	0x0000 0004	0x5202 0204	0x5506 0204
SIMCOP_DMA_SYSCONFIG	RW	32	0x0000 0010	0x5202 0210	0x5506 0210
RESERVED	R	32	0x0000 0018	0x5202 0218	0x5506 0218
SIMCOP_DMA_CTRL	RW	32	0x0000 001C	0x5202 021C	0x5506 0218
SIMCOP_DMA_IRQSTATUS_RAW_j (1)	RW	32	0x0000 0020 + (0x10 * j)	0x5202 0220 + (0x10 * j)	0x5506 0220 + (0x10 * j)
SIMCOP_DMA_IRQSTATUS_j (1)	RW	32	0x0000 0024 + (0x10 * j)	0x5202 0224 + (0x10 * j)	0x5506 0224 + (0x10 * j)
SIMCOP_DMA_IRQENABLE_SET_j (1)	RW	32	0x0000 0028 + (0x10 * j)	0x5202 0228 + (0x10 * j)	0x5506 0228 + (0x10 * j)
SIMCOP_DMA_IRQENABLE_CLR_j (1)	RW	32	0x0000 002C + (0x10 * j)	0x5202 022C + (0x10 * j)	0x5506 022C + (0x10 * j)
SIMCOP_DMA_CHAN_CTRL_i (2)	RW	32	0x0000 0080 + (0x30 * i)	0x5202 0280 + (0x30 * i)	0x5506 0280 + (0x30 * i)
SIMCOP_DMA_CHAN_SMEM_ADDR_i (2)	RW	32	0x0000 0084 + (0x30 * i)	0x5202 0284 + (0x30 * i)	0x5506 0284 + (0x30 * i)
SIMCOP_DMA_CHAN_SMEM_OFST_i (2)	RW	32	0x0000 0088 + (0x30 * i)	0x5202 0288 + (0x30 * i)	0x5506 0288 + (0x30 * i)
SIMCOP_DMA_CHAN_BUF_OFST_i (2)	RW	32	0x0000 008C + (0x30 * i)	0x5202 028C + (0x30 * i)	0x5506 028C + (0x30 * i)
SIMCOP_DMA_CHAN_BUF_ADDR_i (2)	RW	32	0x0000 0090 + (0x30 * i)	0x5202 0290 + (0x30 * i)	0x5506 0290 + (0x30 * i)
SIMCOP_DMA_CHAN_BLOCK_SIZE_i (2)	RW	32	0x0000 0094 + (0x30 * i)	0x5202 0294 + (0x30 * i)	0x5506 0294 + (0x30 * i)
SIMCOP_DMA_CHAN_FRAME_i (2)	RW	32	0x0000 0098 + (0x30 * i)	0x5202 0298 + (0x30 * i)	0x5506 0298 + (0x30 * i)
SIMCOP_DMA_CHAN_CURRENT_BLOCK_i (2)	R	32	0x0000 00A0 + (0x30 * i)	0x5202 02A0 + (0x30 * i)	0x5506 02A0 + (0x30 * i)
SIMCOP_DMA_CHAN_BLOCK_STEP_i (2)	RW	32	0x0000 00A4 + (0x30 * i)	0x5202 02A4 + (0x30 * i)	0x5506 02A4 + (0x30 * i)

(1) j = 0 to 7

(2) i = 0 to 1

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8.4.3.5.2.2 ISS SIMCOP DMA Register Descriptions

through describe the registers in details.

Table 8-1313. SIMCOP_DMA_REVISION

Address Offset	0x0000 0000		
Physical Address	0x5202 0200 0x5506 0200	**Instance**	DMA_L3 DMA_CORTEX-M3
Description	IP Revision Identifier (X.Y.R) Used by software to track features, bugs, and compatibility.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REV																															

Bits	Field Name	Description	Type	Reset
31:0	REV	Revision ID	R	-(1)

(1) TI internal data

Table 8-1314. Register Call Summary for Register SIMCOP_DMA_REVISION

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- ISS SIMCOP DMA Register Manual: [0]

Table 8-1315. SIMCOP_DMA_HWINFO

Address Offset	0x0000 0004		
Physical Address	0x5202 0204 0x5506 0204	**Instance**	DMA_L3 DMA_CORTEX-M3
Description	Information about the IP module's hardware configuration, that is, typically the module's HDL generics.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													CHAN	CONTEXT	

Bits	Field Name	Description	Type	Reset
31:3	RESERVED		R	0x0000 0000
2	CHAN	Logical channels Read 0x0: 4 Read 0x1: 8	R	1
1:0	CONTEXT	Maximum outstanding OCP transactions Read 0x0: 4 Read 0x1: 8 Read 0x2: 16	R	0x2

Table 8-1316. Register Call Summary for Register SIMCOP_DMA_HWINFO

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- ISS SIMCOP DMA Functional Description: [0]
- ISS SIMCOP DMA Register Manual: [1]

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Table 8-1317. SIMCOP_DMA_SYSCONFIG

Address Offset	0x0000 0010		
Physical Address	0x5202 0210 0x5506 0210	**Instance**	DMA_L3 DMA_CORTEX-M3
Description	Clock management configuration		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																										STANDBYMODE		RESERVED			

Bits	Field Name	Description	Type	Reset
31:6	RESERVED		R	0x0000000
5:4	STANDBYMODE	Configuration of the local initiator state management mode. By definition, initiator may generate read/write transaction as long as it is out of STANDBY state. 0x0: Force-standby mode: local initiator is unconditionally placed in standby state. Backup mode, for debug only. 0x1: No-standby mode: local initiator is unconditionally placed out of standby state. Backup mode, for debug only. 0x2: Smart-standby mode. 0x3: Smart-standby mode.	RW	0x2
3:0	RESERVED		R	0x0

Table 8-1318. Register Call Summary for Register SIMCOP_DMA_SYSCONFIG

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- ISS SIMCOP DMA Functional Description: [0]
- ISS SIMCOP DMA Register Manual: [1]

Table 8-1319. SIMCOP_DMA_CTRL

Address Offset	0x0000 001C		
Physical Address	0x5202 021C 0x5506 0218	**Instance**	DMA_L3 DMA_CORTEX-M3
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BW_LIMITER																RESERVED								TAG_CNT				POSTED_WRITES	RESERVED	MAX_BURST_SIZE	

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Bits	Field Name	Description	Type	Reset
31:16	BW_LIMITER	SIMCOP DMA guarantees that there are at least BW_LIMITER functional clock cycles between two OCP requests. No IDLE cycles are inserted during an OCP transaction. This parameter could be used to reduce traffic generated by the SIMCOP DMA for non timing critical applications. Doing so leaves more BW for other system initiators. Default value corresponds to maximum performance.	RW	0x0000
15:8	RESERVED		R	0x00
7:4	TAG_CNT	Limits the outstanding transactions count. Only tags 0 - TAG_CNT will be used by SIMCOP DMA The maximum allowed value is $2^{(SIMCOCP_DMA_GNC.CONTEXT+2)-1}$	RW	0x3
3	POSTED_WRITES	Select write type. Setting depend on the used interconnect 0x0: Only nonposted writes are generated 0x1: Only posted writes are generated	RW	0
2	RESERVED		R	0
1:0	MAX_BURST_SIZE	Defines the maximum burst length for INCR bursts. In case of 2D bursts, length x height is less or equal to this value. 0x0: Single requests only 0x1: less or equal to 2 0x2: less or equal to 4 0x3: less or equal to 8	RW	0x0

Table 8-1320. Register Call Summary for Register SIMCOP_DMA_CTRL

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- ISS SIMCOP DMA Functional Description: [0] [1] [2] [3] [5]
- ISS SIMCOP DMA Register Manual: [6]

Table 8-1321. SIMCOP_DMA_IRQSTATUS_RAW_j

Address Offset	0x0000 0020 + (0x10 * j)		
Physical Address	0x5202 0220 + (0x10 * j) 0x5506 0220 + (0x10 * j)	**Instance**	DMA_L3 DMA_CORTEX-M3
Description	Per-event raw interrupt status vector Raw status is set even if event is not enabled. Write 1 to set the (raw) status, mostly for debug.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHAN7_FRAME_DONE_IRQ	CHAN6_FRAME_DONE_IRQ	CHAN5_FRAME_DONE_IRQ	CHAN4_FRAME_DONE_IRQ	CHAN3_FRAME_DONE_IRQ	CHAN2_FRAME_DONE_IRQ	CHAN1_FRAME_DONE_IRQ	CHAN0_FRAME_DONE_IRQ	CHAN7_BLOCK_DONE_IRQ	CHAN6_BLOCK_DONE_IRQ	CHAN5_BLOCK_DONE_IRQ	CHAN4_BLOCK_DONE_IRQ	CHAN3_BLOCK_DONE_IRQ	CHAN2_BLOCK_DONE_IRQ	CHAN1_BLOCK_DONE_IRQ	CHAN0_BLOCK_DONE_IRQ	RESERVED															OCP_ERR

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Bits	Field Name	Description	Type	Reset
31	CHAN7_FRAME_DONE_IRQ	Channel has completed transfer of the full frame Write 0x0: No action Read 0x0: No event pending Read 0x1: Event pending Write 0x1: Set event (debug)	RW W1toSet	0
30	CHAN6_FRAME_DONE_IRQ	Channel has completed transfer of the full frame Write 0x0: No action Read 0x0: No event pending Read 0x1: Event pending Write 0x1: Set event (debug)	RW W1toSet	0
29	CHAN5_FRAME_DONE_IRQ	Channel has completed transfer of the full frame Write 0x0: No action Read 0x0: No event pending Read 0x1: Event pending Write 0x1: Set event (debug)	RW W1toSet	0
28	CHAN4_FRAME_DONE_IRQ	Channel has completed transfer of the full frame Write 0x0: No action Read 0x0: No event pending Read 0x1: Event pending Write 0x1: Set event (debug)	RW W1toSet	0
27	CHAN3_FRAME_DONE_IRQ	Channel has completed transfer of the full frame Write 0x0: No action Read 0x0: No event pending Read 0x1: Event pending Write 0x1: Set event (debug)	RW W1toSet	0
26	CHAN2_FRAME_DONE_IRQ	Channel has completed transfer of the full frame Write 0x0: No action Read 0x0: No event pending Read 0x1: Event pending Write 0x1: Set event (debug)	RW W1toSet	0
25	CHAN1_FRAME_DONE_IRQ	Channel has completed transfer of the full frame Write 0x0: No action Read 0x0: No event pending Read 0x1: Event pending Write 0x1: Set event (debug)	RW W1toSet	0
24	CHAN0_FRAME_DONE_IRQ	Channel has completed transfer of the full frame Write 0x0: No action Read 0x0: No event pending Read 0x1: Event pending Write 0x1: Set event (debug)	RW W1toSet	0
23	CHAN7_BLOCK_DONE_IRQ	Channel has completed transfer of one 2D block Write 0x0: No action Read 0x0: No event pending Read 0x1: Event pending Write 0x1: Set event (debug)	RW W1toSet	0

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Bits	Field Name	Description	Type	Reset
22	CHAN6_BLOCK_DONE_IRQ	Channel has completed transfer of one 2D block Write 0x0: No action Read 0x0: No event pending Read 0x1: Event pending Write 0x1: Set event (debug)	RW W1toSet	0
21	CHAN5_BLOCK_DONE_IRQ	Channel has completed transfer of one 2D block Write 0x0: No action Read 0x0: No event pending Read 0x1: Event pending Write 0x1: Set event (debug)	RW W1toSet	0
20	CHAN4_BLOCK_DONE_IRQ	Channel has completed transfer of one 2D block Write 0x0: No action Read 0x0: No event pending Read 0x1: Event pending Write 0x1: Set event (debug)	RW W1toSet	0
19	CHAN3_BLOCK_DONE_IRQ	Channel has completed transfer of one 2D block Write 0x0: No action Read 0x0: No event pending Read 0x1: Event pending Write 0x1: Set event (debug)	RW W1toSet	0
18	CHAN2_BLOCK_DONE_IRQ	Channel has completed transfer of one 2D block Write 0x0: No action Read 0x0: No event pending Read 0x1: Event pending Write 0x1: Set event (debug)	RW W1toSet	0
17	CHAN1_BLOCK_DONE_IRQ	Channel has completed transfer of one 2D block Write 0x0: No action Read 0x0: No event pending Read 0x1: Event pending Write 0x1: Set event (debug)	RW W1toSet	0
16	CHAN0_BLOCK_DONE_IRQ	Channel has completed transfer of one 2D block Write 0x0: No action Read 0x0: No event pending Read 0x1: Event pending Write 0x1: Set event (debug)	RW	0
15:1	RESERVED		R	0x0000
0	OCP_ERR	OCP error Write 0x0: No action Read 0x0: No event pending Read 0x1: Event pending Write 0x1: Set event (debug)	RW W1toSet	0

Table 8-1322. Register Call Summary for Register SIMCOP_DMA_IRQSTATUS_RAW_j

ISS Still Image Coprocessor

- ISS SIMCOP DMA Functional Description: [0] [1]
- ISS SIMCOP DMA Register Manual: [2]

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Table 8-1323. SIMCOP_DMA_IRQSTATUS_j

Address Offset	0x0000 0024 + (0x10 * j)		
Physical Address	0x5202 0224 + (0x10 * j) 0x5506 0224 + (0x10 * j)	**Instance**	DMA_L3 DMA_CORTEX-M3
Description	Per-event "enabled" interrupt status vector Enabled status is not set unless event is enabled. Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, that is, even if not enabled).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHAN7_FRAME_DONE_IRQ	CHAN6_FRAME_DONE_IRQ	CHAN5_FRAME_DONE_IRQ	CHAN4_FRAME_DONE_IRQ	CHAN3_FRAME_DONE_IRQ	CHAN2_FRAME_DONE_IRQ	CHAN1_FRAME_DONE_IRQ	CHAN0_FRAME_DONE_IRQ	CHAN7_BLOCK_DONE_IRQ	CHAN6_BLOCK_DONE_IRQ	CHAN5_BLOCK_DONE_IRQ	CHAN4_BLOCK_DONE_IRQ	CHAN3_BLOCK_DONE_IRQ	CHAN2_BLOCK_DONE_IRQ	CHAN1_BLOCK_DONE_IRQ	CHAN0_BLOCK_DONE_IRQ	RESERVED															BUS_ERR

Bits	Field Name	Description	Type	Reset
31	CHAN7_FRAME_DONE_IRQ	Channel has completed transfer of the full frame Write 0x0: No action Read 0x0: No (enabled) event pending Read 0x1: Event pending Write 0x1: Clear (raw) event	RW W1toClr	0
30	CHAN6_FRAME_DONE_IRQ	Channel has completed transfer of the full frame Write 0x0: No action Read 0x0: No (enabled) event pending Read 0x1: Event pending Write 0x1: Clear (raw) event	RW W1toClr	0
29	CHAN5_FRAME_DONE_IRQ	Channel has completed transfer of the full frame Write 0x0: No action Read 0x0: No (enabled) event pending Read 0x1: Event pending Write 0x1: Clear (raw) event	RW W1toClr	0
28	CHAN4_FRAME_DONE_IRQ	Channel has completed transfer of the full frame Write 0x0: No action Read 0x0: No (enabled) event pending Read 0x1: Event pending Write 0x1: Clear (raw) event	RW W1toClr	0
27	CHAN3_FRAME_DONE_IRQ	Channel has completed transfer of the full frame Write 0x0: No action Read 0x0: No (enabled) event pending Read 0x1: Event pending Write 0x1: Clear (raw) event	RW W1toClr	0
26	CHAN2_FRAME_DONE_IRQ	Channel has completed transfer of the full frame Write 0x0: No action Read 0x0: No (enabled) event pending Read 0x1: Event pending Write 0x1: Clear (raw) event	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
25	CHAN1_FRAME_DONE_IRQ	Channel has completed transfer of the full frame Write 0x0: No action Read 0x0: No (enabled) event pending Read 0x1: Event pending Write 0x1: Clear (raw) event	RW W1toClr	0
24	CHAN0_FRAME_DONE_IRQ	Channel has completed transfer of the full frame Write 0x0: No action Read 0x0: No (enabled) event pending Read 0x1: Event pending Write 0x1: Clear (raw) event	RW W1toClr	0
23	CHAN7_BLOCK_DONE_IRQ	Channel has completed transfer of one 2D block Write 0x0: No action Read 0x0: No (enabled) event pending Read 0x1: Event pending Write 0x1: Clear (raw) event	RW W1toClr	0
22	CHAN6_BLOCK_DONE_IRQ	Channel has completed transfer of one 2D block Write 0x0: No action Read 0x0: No (enabled) event pending Read 0x1: Event pending Write 0x1: Clear (raw) event	RW W1toClr	0
21	CHAN5_BLOCK_DONE_IRQ	Channel has completed transfer of one 2D block Write 0x0: No action Read 0x0: No (enabled) event pending Read 0x1: Event pending Write 0x1: Clear (raw) event	RW W1toClr	0
20	CHAN4_BLOCK_DONE_IRQ	Channel has completed transfer of one 2D block Write 0x0: No action Read 0x0: No (enabled) event pending Read 0x1: Event pending Write 0x1: Clear (raw) event	RW W1toClr	0
19	CHAN3_BLOCK_DONE_IRQ	Channel has completed transfer of one 2D block Write 0x0: No action Read 0x0: No (enabled) event pending Read 0x1: Event pending Write 0x1: Clear (raw) event	RW W1toClr	0
18	CHAN2_BLOCK_DONE_IRQ	Channel has completed transfer of one 2D block Write 0x0: No action Read 0x0: No (enabled) event pending Read 0x1: Event pending Write 0x1: Clear (raw) event	RW W1toClr	0
17	CHAN1_BLOCK_DONE_IRQ	Channel has completed transfer of one 2D block Write 0x0: No action Read 0x0: No (enabled) event pending Read 0x1: Event pending Write 0x1: Clear (raw) event	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
16	CHAN0_BLOCK_DONE_IRQ	Channel has completed transfer of one 2D block Write 0x0: No action Read 0x0: No (enabled) event pending Read 0x1: Event pending Write 0x1: Clear (raw) event	RW W1toClr	0
15:1	RESERVED		R	0x0000
0	BUS_ERR	BUS error Write 0x0: No action Read 0x0: No (enabled) event pending Read 0x1: Event pending Write 0x1: Clear (raw) event	RW W1toClr	0

Table 8-1324. Register Call Summary for Register SIMCOP_DMA_IRQSTATUS_j

ISS Still Image Coprocessor

- ISS SIMCOP DMA Functional Description: [0] [1]
- ISS SIMCOP DMA Register Manual: [2]

Table 8-1325. SIMCOP_DMA_IRQENABLE_SET_j

Address Offset	0x0000 0028 + (0x10 * j)		
Physical Address	0x5202 0228 + (0x10 * j) 0x5506 0228 + (0x10 * j)	**Instance**	DMA_L3 DMA_CORTEX-M3
Description	Per-event interrupt enable bit vector Write 1 to set (enable interrupt). Readout equal to corresponding _CLR register.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHAN7_FRAME_DONE_IRQ	CHAN6_FRAME_DONE_IRQ	CHAN5_FRAME_DONE_IRQ	CHAN4_FRAME_DONE_IRQ	CHAN3_FRAME_DONE_IRQ	CHAN2_FRAME_DONE_IRQ	CHAN1_FRAME_DONE_IRQ	CHAN0_FRAME_DONE_IRQ	CHAN7_BLOCK_DONE_IRQ	CHAN6_BLOCK_DONE_IRQ	CHAN5_BLOCK_DONE_IRQ	CHAN4_BLOCK_DONE_IRQ	CHAN3_BLOCK_DONE_IRQ	CHAN2_BLOCK_DONE_IRQ	CHAN1_BLOCK_DONE_IRQ	CHAN0_BLOCK_DONE_IRQ	RESERVED															OCP_ERR

Bits	Field Name	Description	Type	Reset
31	CHAN7_FRAME_DONE_IRQ	Channel has completed transfer of the full frame Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW W1toSet	0
30	CHAN6_FRAME_DONE_IRQ	Channel has completed transfer of the full frame Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW W1toSet	0

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Bits	Field Name	Description	Type	Reset
29	CHAN5_FRAME_DONE_IRQ	Channel has completed transfer of the full frame Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW W1toSet	0
28	CHAN4_FRAME_DONE_IRQ	Channel has completed transfer of the full frame Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW W1toSet	0
27	CHAN3_FRAME_DONE_IRQ	Channel has completed transfer of the full frame Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW W1toSet	0
26	CHAN2_FRAME_DONE_IRQ	Channel has completed transfer of the full frame Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW W1toSet	0
25	CHAN1_FRAME_DONE_IRQ	Channel has completed transfer of the full frame Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW W1toSet	0
24	CHAN0_FRAME_DONE_IRQ	Channel has completed transfer of the full frame Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW W1toSet	0
23	CHAN7_BLOCK_DONE_IRQ	Channel has completed transfer of one 2D block Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW W1toSet	0
22	CHAN6_BLOCK_DONE_IRQ	Channel has completed transfer of one 2D block Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW W1toSet	0
21	CHAN5_BLOCK_DONE_IRQ	Channel has completed transfer of one 2D block Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW W1toSet	0

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Bits	Field Name	Description	Type	Reset
20	CHAN4_BLOCK_DONE_IRQ	Channel has completed transfer of one 2D block Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW W1toSet	0
19	CHAN3_BLOCK_DONE_IRQ	Channel has completed transfer of one 2D block Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW W1toSet	0
18	CHAN2_BLOCK_DONE_IRQ	Channel has completed transfer of one 2D block Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW W1toSet	0
17	CHAN1_BLOCK_DONE_IRQ	Channel has completed transfer of one 2D block Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW W1toSet	0
16	CHAN0_BLOCK_DONE_IRQ	Channel has completed transfer of one 2D block Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW W1toSet	0
15:1	RESERVED		R	0x0000
0	OCP_ERR	OCP error Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW W1toSet	0

Table 8-1326. Register Call Summary for Register SIMCOP_DMA_IRQENABLE_SET_j

ISS Still Image Coprocessor

- ISS SIMCOP DMA Functional Description: [0]
- ISS SIMCOP DMA Register Manual: [1]

Table 8-1327. SIMCOP_DMA_IRQENABLE_CLR_j

Address Offset	0x0000 002C + (0x10 * j)		
Physical Address	0x5202 022C + (0x10 * j) 0x5506 022C + (0x10 * j)	**Instance**	DMA_L3 DMA_CORTEX-M3
Description	Per-event interrupt enable bit vector Write 1 to clear (disable interrupt). Readout equal to corresponding _SET register.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHAN7_FRAME_DONE_IRQ	CHAN6_FRAME_DONE_IRQ	CHAN5_FRAME_DONE_IRQ	CHAN4_FRAME_DONE_IRQ	CHAN3_FRAME_DONE_IRQ	CHAN2_FRAME_DONE_IRQ	CHAN1_FRAME_DONE_IRQ	CHAN0_FRAME_DONE_IRQ	CHAN7_BLOCK_DONE_IRQ	CHAN6_BLOCK_DONE_IRQ	CHAN5_BLOCK_DONE_IRQ	CHAN4_BLOCK_DONE_IRQ	CHAN3_BLOCK_DONE_IRQ	CHAN2_BLOCK_DONE_IRQ	CHAN1_BLOCK_DONE_IRQ	CHAN0_BLOCK_DONE_IRQ	RESERVED															OCP_ERR

Bits	Field Name	Description	Type	Reset
31	CHAN7_FRAME_DONE_IRQ	Channel has completed transfer of the full frame Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW W1toClr	0
30	CHAN6_FRAME_DONE_IRQ	Channel has completed transfer of the full frame Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW W1toClr	0
29	CHAN5_FRAME_DONE_IRQ	Channel has completed transfer of the full frame Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW W1toClr	0
28	CHAN4_FRAME_DONE_IRQ	Channel has completed transfer of the full frame Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW W1toClr	0
27	CHAN3_FRAME_DONE_IRQ	Channel has completed transfer of the full frame Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW W1toClr	0
26	CHAN2_FRAME_DONE_IRQ	Channel has completed transfer of the full frame Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW W1toClr	0
25	CHAN1_FRAME_DONE_IRQ	Channel has completed transfer of the full frame Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
24	CHAN0_FRAME_DONE_IRQ	Channel has completed transfer of the full frame Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW W1toClr	0
23	CHAN7_BLOCK_DONE_IRQ	Channel has completed transfer of one 2D block Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW W1toClr	0
22	CHAN6_BLOCK_DONE_IRQ	Channel has completed transfer of one 2D block Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW W1toClr	0
21	CHAN5_BLOCK_DONE_IRQ	Channel has completed transfer of one 2D block Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW W1toClr	0
20	CHAN4_BLOCK_DONE_IRQ	Channel has completed transfer of one 2D block Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW W1toClr	0
19	CHAN3_BLOCK_DONE_IRQ	Channel has completed transfer of one 2D block Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW W1toClr	0
18	CHAN2_BLOCK_DONE_IRQ	Channel has completed transfer of one 2D block Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW W1toClr	0
17	CHAN1_BLOCK_DONE_IRQ	Channel has completed transfer of one 2D block Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW W1toClr	0
16	CHAN0_BLOCK_DONE_IRQ	Channel has completed transfer of one 2D block Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW W1toClr	0
15:1	RESERVED		R	0x0000

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Bits	Field Name	Description	Type	Reset
0	OCP_ERR	OCP error Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW W1toClr	0

Table 8-1328. Register Call Summary for Register SIMCOP_DMA_IRQENABLE_CLR_j

ISS Still Image Coprocessor

- ISS SIMCOP DMA Functional Description: [0]
- ISS SIMCOP DMA Register Manual: [1]

Table 8-1329. SIMCOP_DMA_CHAN_CTRL_i

Address Offset	0x0000 0080 + (0x30 * i)		
Physical Address	0x5202 0280 + (0x30 * i) 0x5506 0280 + (0x30 * i)	**Instance**	DMA_L3 DMA_CORTEX-M3
Description	Logical channel control register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								HWSTOP				HWSTART				LINKED				RESERVED				TILERMODE	DIR	STATUS			SWTRIGGER	DISABLE	ENABLE

Bits	Field Name	Description	Type	Reset
31:23	RESERVED		R	0x000
22:20	HWSTOP	DMA logical channel hardware synchronization. Controls generation of the DONE pulse for the logical channel Only the values listed below are allowed. Other values lead to undefined behavior. 0x0: Disabled. 0x4: Use hardware synchronization channel 0 0x5: Use hardware synchronization channel 1 0x6: Use hardware synchronization channel 2 0x7: Use hardware synchronization channel 3	RW	0x0
19:17	HWSTART	DMA logical channel hardware synchronization. Controls sensitivity of the logical channel on a START pulse Only the values listed below are allowed. Other values lead to undefined behavior. 0x0: Disabled. 0x4: Use hardware synchronization channel 0 0x5: Use hardware synchronization channel 1 0x6: Use hardware synchronization channel 2 0x7: Use hardware synchronization channel 3	RW	0x0

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Bits	Field Name	Description	Type	Reset
16:12	LINKED	DMA logical channel linking. Only the values listed below are allowed. Other values lead to undefined behavior. 0x0: Disabled. 0x10: Start channel 0 when this channel has completed transfer of one 2D block 0x11: Start channel 1 when this channel has completed transfer of one 2D block 0x12: Start channel 2 when this channel has completed transfer of one 2D block 0x13: Start channel 3 when this channel has completed transfer of one 2D block 0x14: Start channel 4 when this channel has completed transfer of one 2D block 0x15: Start channel 5 when this channel has completed transfer of one 2D block 0x16: Start channel 6 when this channel has completed transfer of one 2D block 0x17: Start channel 7 when this channel has completed transfer of one 2D block	RW	0x00
11:7	RESERVED		R	0x0
6	TILERMODE	Selects OCP transaction breakdown algorithm 0x0: Regular mode. INCR burst are used. ADDR[32]=0 for OCP transactions 0x1: Tiler mode. BLCK burst are used. ADDR[32]=1 for OCP transactions	RW	-
5	DIR	Transfer direction 0x0: System memory - SIMCOP buffers 0x1: SIMCOP buffers - system memory	RW	0
4:3	STATUS	SW could poll this bit to know the state of the channel Read 0x0: Idle Read 0x1: Active Read 0x2: Pending Read 0x3: Running	R	0x0
2	SWTRIGGER	Software trigger of the DMA channel. Read of this register always returns 0. Write 0x0: No effect Write 0x1: Change the logical channel state to PENDING if it is in ACTIVE state. No effect if the channel is in RUNNING, PENDING or IDLE state	W	0
1	DISABLE	Disable control of the logical channel. Read of this register always returns 0. Write 0x0: No effect. Write 0x1: Disable the channel. Changes the logical channel state to IDLE when it is in ACTIVE state. Memorize a disable request when the channel is in RUNNING or PENDING state.	W	0
0	ENABLE	Enable control of the logical channel. Read of this register always returns 0. Write 0x0: No effect Write 0x1: Enable the channel. Changes the state of the logical channel from IDLE to ACTIVE.	W	0

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Table 8-1330. Register Call Summary for Register SIMCOP_DMA_CHAN_CTRL_i

ISS Still Image Coprocessor

- ISS SIMCOP DMA Functional Description: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15]
- ISS SIMCOP DMA Basic Programming Model: [18] [19] [20] [21] [22] [23] [24] [25] [26] [27] [28] [29] [30] [31] [32] [33] [34]
- ISS SIMCOP DMA Register Manual: [35]

Table 8-1331. SIMCOP_DMA_CHAN_SMEM_ADDR_i

Address Offset	0x0000 0084 + (0x30 * i)		
Physical Address	0x5202 0284 + (0x30 * i) 0x5506 0284 + (0x30 * i)	**Instance**	DMA_L3 DMA_CORTEX-M3
Description	System memory address		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR																												RESERVED			

Bits	Field Name	Description	Type	Reset
31:4	ADDR	Address in 128-bit words	RW	0x-------
3:0	RESERVED		R	0x0

Table 8-1332. Register Call Summary for Register SIMCOP_DMA_CHAN_SMEM_ADDR_i

ISS Still Image Coprocessor

- ISS SIMCOP DMA Functional Description: [0] [1]
- ISS SIMCOP DMA Basic Programming Model: [2] [3] [4] [5]
- ISS SIMCOP DMA Register Manual: [6]

Table 8-1333. SIMCOP_DMA_CHAN_SMEM_OFST_i

Address Offset	0x0000 0088 + (0x30 * i)		
Physical Address	0x5202 0288 + (0x30 * i) 0x5506 0288 + (0x30 * i)	**Instance**	DMA_L3 DMA_CORTEX-M3
Description	System memory line offset in 128-bit words. Maximum stride = 1MB		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												OFST																RESERVED			

Bits	Field Name	Description	Type	Reset
31:20	RESERVED		R	0x000
19:4	OFST	Line offset. In 128-bit words.	RW	0x----
3:0	RESERVED		R	0x0

Table 8-1334. Register Call Summary for Register SIMCOP_DMA_CHAN_SMEM_OFST_i

ISS Still Image Coprocessor

- ISS SIMCOP DMA Functional Description: [0] [1] [2]
- ISS SIMCOP DMA Basic Programming Model: [3] [4] [5] [6]
- ISS SIMCOP DMA Register Manual: [7]

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Table 8-1335. SIMCOP_DMA_CHAN_BUF_OFST_i

Address Offset	0x0000 008C + (0x30 * i)		
Physical Address	0x5202 028C + (0x30 * i) 0x5506 028C + (0x30 * i)	**Instance**	DMA_L3 DMA_CORTEX-M3
Description	SIMCOP memory line offset		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								OFST																				RESERVED			

Bits	Field Name	Description	Type	Reset
31:24	RESERVED		R	0x00
23:4	OFST	Line offset. In 128-bit words.	RW	0x-----
3:0	RESERVED		R	0x0

Table 8-1336. Register Call Summary for Register SIMCOP_DMA_CHAN_BUF_OFST_i

ISS Still Image Coprocessor

- ISS SIMCOP DMA Basic Programming Model: [0] [1] [2] [3]
- ISS SIMCOP DMA Register Manual: [4]

Table 8-1337. SIMCOP_DMA_CHAN_BUF_ADDR_i

Address Offset	0x0000 0090 + (0x30 * i)		
Physical Address	0x5202 0290 + (0x30 * i) 0x5506 0290 + (0x30 * i)	**Instance**	DMA_L3 DMA_CORTEX-M3
Description	SIMCOP memory address		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								ADDR																				RESERVED			

Bits	Field Name	Description	Type	Reset
31:24	RESERVED		R	0x00
23:4	ADDR	Address in 128-bit words.	RW	0x-----
3:0	RESERVED		R	0x0

Table 8-1338. Register Call Summary for Register SIMCOP_DMA_CHAN_BUF_ADDR_i

ISS Still Image Coprocessor

- ISS SIMCOP DMA Functional Description: [0]
- ISS SIMCOP DMA Basic Programming Model: [1] [2] [3] [4]
- ISS SIMCOP DMA Register Manual: [5]

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Table 8-1339. SIMCOP_DMA_CHAN_BLOCK_SIZE_i

Address Offset	0x0000 0094 + (0x30 * i)		
Physical Address	0x5202 0294 + (0x30 * i) 0x5506 0294 + (0x30 * i)	**Instance**	DMA_L3 DMA_CORTEX-M3
Description	2D block size		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								YNUM								RESERVED								XNUM							RESERVED

Bits	Field Name	Description	Type	Reset
31:29	RESERVED		R	0x0
28:16	YNUM	Height, in lines, per 2D block Valid values are 1- 8191.	RW	0bxxxxxxxxxxxxx
15:14	RESERVED		R	0x0
13:4	XNUM	Width, in 128-bit words, per 2D block. Valid values are 1-1023, that corresponds to 16 bytes to 16KB.	RW	0bxxxxxxxxxx
3:0	RESERVED		R	0x0

Table 8-1340. Register Call Summary for Register SIMCOP_DMA_CHAN_BLOCK_SIZE_i

ISS Still Image Coprocessor

- ISS SIMCOP DMA Functional Description: [0] [1] [2] [3] [4]
- ISS SIMCOP DMA Basic Programming Model: [5] [6] [7] [8] [9] [10] [11] [12]
- ISS SIMCOP DMA Register Manual: [13]

Table 8-1341. SIMCOP_DMA_CHAN_FRAME_i

Address Offset	0x0000 0098 + (0x30 * i)		
Physical Address	0x5202 0298 + (0x30 * i) 0x5506 0298 + (0x30 * i)	**Instance**	DMA_L3 DMA_CORTEX-M3
Description	Defines a frame. A frame is composed of 2D blocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								YCNT								RESERVED								XCNT							

Bits	Field Name	Description	Type	Reset
31:26	RESERVED	Reserved.	R	0x00
25:16	YCNT	Vertical count of 2D blocks per frame. Valid values are 1-1023	RW	0bxxxxxxxxxx
15:10	RESERVED	Reserved.	R	0x00
9:0	XCNT	Horizontal count of 2D blocks per frame. Valid values are 1-1023	RW	0bxxxxxxxxxx

Table 8-1342. Register Call Summary for Register SIMCOP_DMA_CHAN_FRAME_i

ISS Still Image Coprocessor

- ISS SIMCOP DMA Functional Description: [0] [1]
- ISS SIMCOP DMA Basic Programming Model: [2] [3] [4] [5] [6] [7] [8] [9]
- ISS SIMCOP DMA Register Manual: [10]

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Table 8-1343. SIMCOP_DMA_CHAN_CURRENT_BLOCK_i

Address Offset	0x0000 00A0 + (0x30 * i)		
Physical Address	0x5202 02A0 + (0x30 * i) 0x5506 02A0 + (0x30 * i)	**Instance**	DMA_L3 DMA_CORTEX-M3
Description	SW could read the coordinates of the last transferred block. The status is reset when the channel is enabled (change the state of CTRL.ENABLE from 0 to 1).		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								BY								RESERVED								BX							

Bits	Field Name	Description	Type	Reset
31:26	RESERVED	Reserved.	R	0x00
25:16	BY	Vertical position of the last transferred 2D block in the frame.	R	0bxxxxxxxxxx
15:10	RESERVED	Reserved.	R	0x00
9:0	BX	Horizontal position of the last transferred 2D block in the frame.	R	0bxxxxxxxxxx

Table 8-1344. Register Call Summary for Register SIMCOP_DMA_CHAN_CURRENT_BLOCK_i

ISS Still Image Coprocessor

- ISS SIMCOP DMA Functional Description: [0]
- ISS SIMCOP DMA Register Manual: [1]

Table 8-1345. SIMCOP_DMA_CHAN_BLOCK_STEP_i

Address Offset	0x0000 00A4 + (0x30 * i)		
Physical Address	0x5202 02A4 + (0x30 * i) 0x5506 02A4 + (0x30 * i)	**Instance**	DMA_L3 DMA_CORTEX-M3
Description	Offset between 2D blocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								YSTEP								RESERVED								XSTEP							RESERVED

Bits	Field Name	Description	Type	Reset
31:30	RESERVED		R	0x0
29:16	YSTEP	Vertical offset, in lines, between rows of 2D blocks. For contiguous 2D blocks YSTEP=YNUM Valid values are -8192 to +8191.	RW	0b0xxxxxxxxxxxxx
15	RESERVED		R	0
14:4	XSTEP	Horizontal offset, in 128-bit words, between 2D block columns. For contiguous 2D blocks XSTEP=XNUM Valid values are -1024 to +1023, that corresponds to 16 bytes to 16KB.	RW	0bxxxxxxxxxxx
3:0	RESERVED		R	0x0

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Table 8-1346. Register Call Summary for Register SIMCOP_DMA_CHAN_BLOCK_STEP_i

ISS Still Image Coprocessor

- ISS SIMCOP DMA Functional Description: [0] [1] [2] [3]
- ISS SIMCOP DMA Basic Programming Model: [4] [5] [6] [7] [8] [9] [10] [11]
- ISS SIMCOP DMA Register Manual: [12]

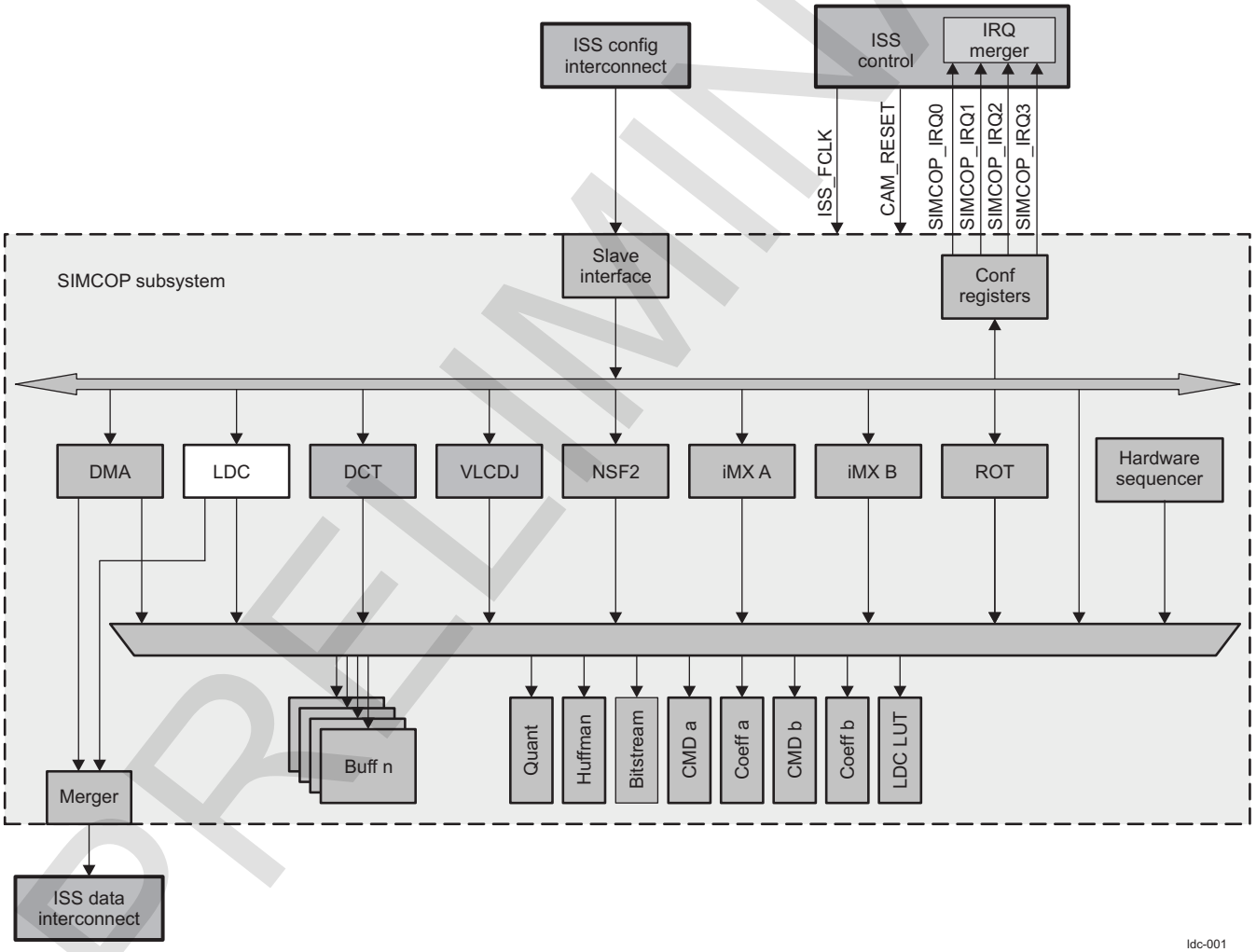
8.4.4 ISS SIMCOP LDC Module

This chapter describes the lens distortion correction (LDC) module in the still image coprocessor (SIMCOP) subsystem.

8.4.4.1 ISS SIMCOP LDC Overview

The LDC deals with lens geometric distortion issues, chromatic aberration, and affine transformation for camera images. Figure 8-267 is an overview of the LDC in the SIMCOP subsystem.

Figure 8-267. LDC in the SIMCOP Subsystem



For still image or video applications the LDC supports:

- Lens distortion correction:
  - YCbCr 4:2:2/4:2:0 data format input/output (I/O) for post-image-pipe correction
  - Correct barrel distortion and pin-cushion distortion
  - Radius-to-magnification-factor table to accommodate various distortion functions through

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programming
  - Configurable center point and horizontal/vertical adjustment
  - One 256-entry look-up table (LUT) for Y, Cb, and Cr
  - 8 bits for YCbCr
  - Bicubic interpolation for Y and bilinear interpolation for Cb/Cr
  - Bilinear interpolation mode for Y to offer faster processing
  - Up to 16,383 x 16,383 image dimension
  - Format restriction:
    - YCbCr 4:2:2 format: Tile width must be a multiple of 16.
    - YCbCr 4:2:0 format: Tile width must be a multiple of 32.
- Image warping, scaling, and rotation:
  - Affine transformation for image warping, scaling, and rotation
  - 8 bits for YCbCr
  - Bicubic interpolation for Y and bilinear interpolation for Cb/Cr
  - Bilinear interpolation mode for Y to offer double throughput
  - Format restriction:
    - YCbCr 4:2:2 format: Tile width must be a multiple of 16.
    - YCbCr 4:2:0 format: Tile width must be a multiple of 32.
- Chromatic aberration correction:
  - Supports Bayer data in unpacked 12-bit per pixel, 8-bit per pixel A-Law, 8-bit per pixel unpacked, and 12-bit per pixel packed formats
  - Radius-to-magnification-factor table to accommodate various distortion functions through programming
  - Configurable center point and horizontal/vertical adjustment
  - Red and blue distortion only. Green pixels are copied to output.
  - Independent 128-entry LUTs for red and blue
  - Bilinear interpolation
  - Up to 16,383 x 16,383 image dimension
  - Format restriction:
    - Unpacked 12-bit format: Tile width must be a multiple of 16.
    - A-Law 8-bit format: Tile width must be a multiple of 32.
    - Unpacked 8-bit format: Tile width must be a multiple of 32.
    - Packed 12-bit format: Tile width must be a multiple of 64.

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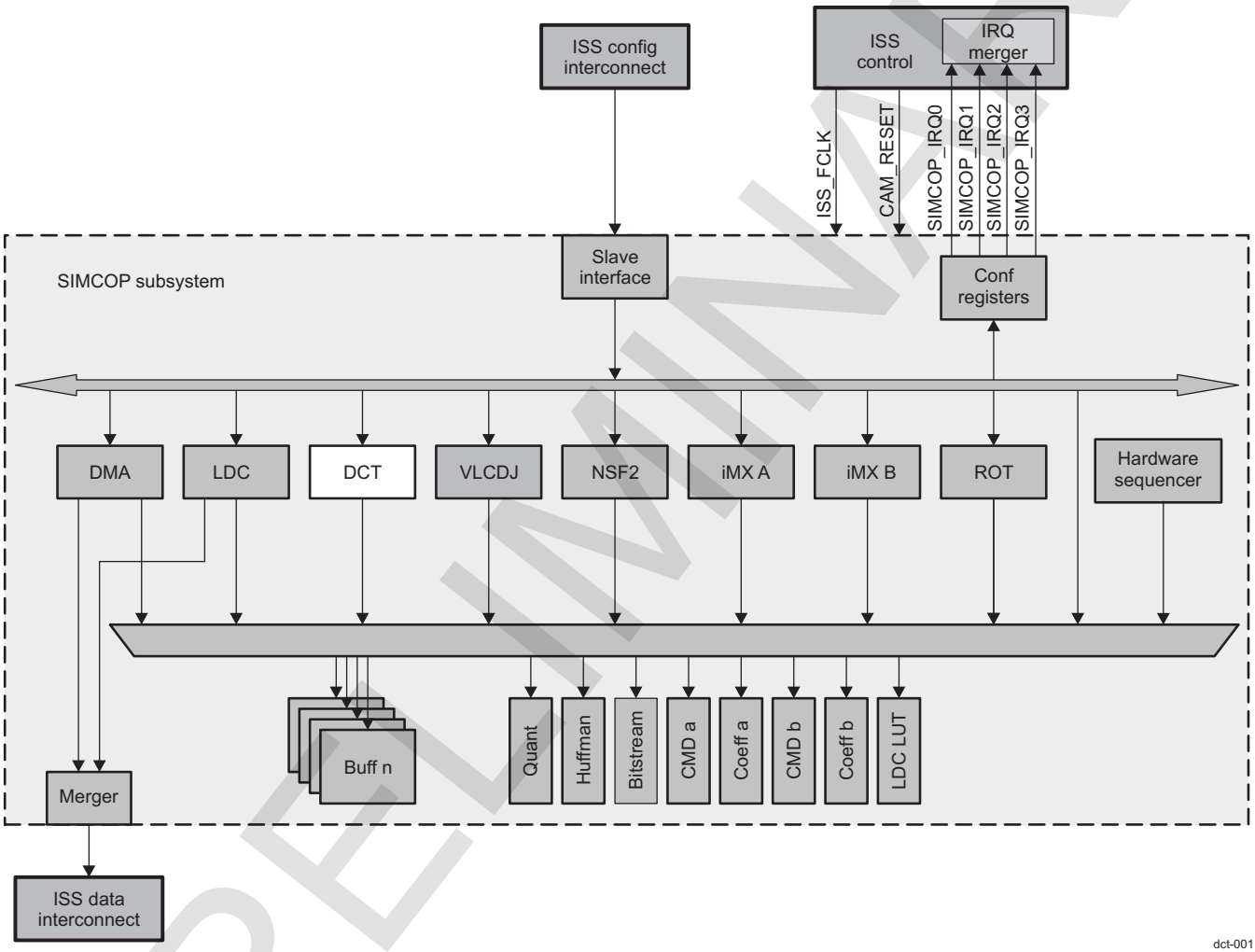
8.4.5 ISS SIMCOP Discrete Cosine Transform Module

This section describes the discrete cosine transform (DCT) module in the still-image coprocessor (SIMCOP) subsystem.

8.4.5.1 ISS SIMCOP DCT Overview

The DCT module performs DCT and inverse DCT (IDCT) operations required for still-image coder/decoder (codec) applications. Figure 8-268 is an overview of the DCT in the SIMCOP subsystem.

Figure 8-268. DCT in the SIMCOP Subsystem



For still-image or video applications, the DCT supports:

- 8-bit data in the spatial domain (input to DCT or output of IDCT) with –128 offset on color components
- 16-bit data in the frequency domain
- Exact input/output (I/O) range:
  - DCT expected input range [0, 255], subtracting 128 offset before transform, output saturated to [–1024, 1023]
  - IDCT expected input range [–1280, 1079], adding 128 to inverse transform outcome and saturating to [0, 255]
  - IDCT input range is from DCT output range plus [–256, 256] worst-case quantization error
- Configurable to process up to 32 microcontroller units (MCUs) at a time (21 MCUs for YUV4:2:0, and 32 MCUs for YUV4:2:2, because of memory size limitations)

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- The following formats are supported by the DCT:
  - 16 x 16-pixel block MCU for YUV4:2:0 format, spatial data storage follows NV12
  - 16 x 8-pixel block MCU for YUV4:2:2 format, spatial data storage follows UYVY
  - Sequential 8 x 8 block mode, other than YUV4:2:0 and YUV4:2:2, a color-neutral format to allow flexibility in color component configuration in MCU, processes up to 64 blocks per task
- JPEG baseline sequential is supported by sequential 8 x 8 block mode. Some post-processing to reorder data and color space conversion may be required.
- All frequency domain data are stored sequentially for each 8 x 8 block, 16 bits per data point.

8.4.5.2 ISS SIMCOP DCT Integration

The DCT is part of the SIMCOP subsystem in the imaging subsystem (ISS). Figure 8-269 shows the integration of the DCT in the SIMCOP subsystem.

Figure 8-269. DCT Engine Integration

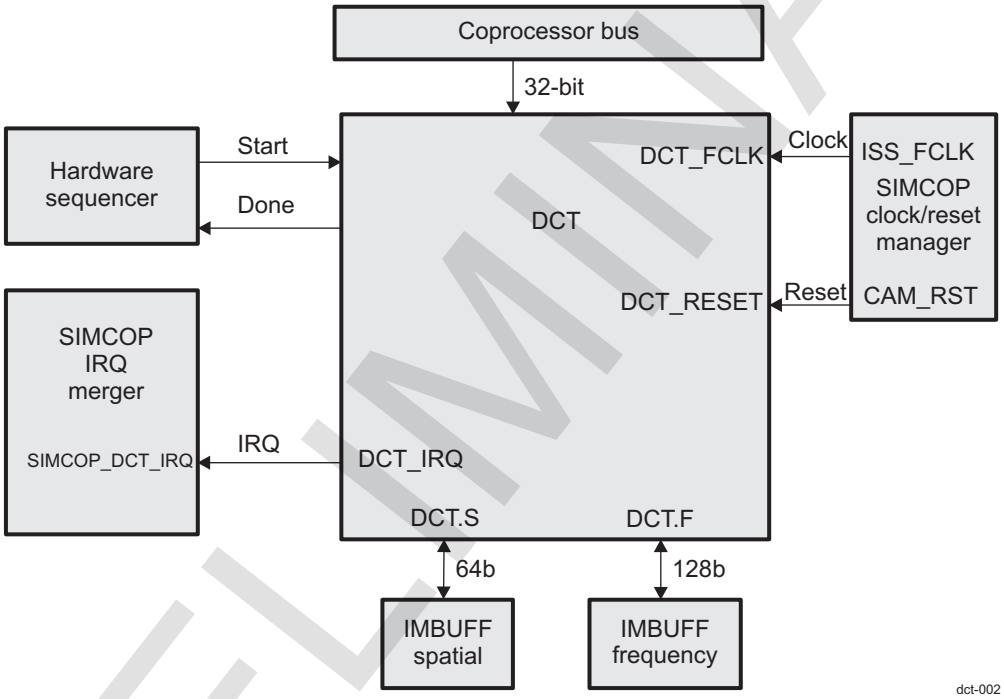

Table 8-1347 through Table 8-1349 list the integration attributes, clocks and resets, and hardware requests, respectively, for the DCT.

Table 8-1347. Integration Attributes

Module Instance	Attributes	
	Power Domain	Interconnect
DCT	PD_CAM	

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Table 8-1348. Clocks and Resets

Clocks				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
DCT	DCT_FCLK	ISS_FCLK	PRCM	Functional clock provided by ISS_CLK from the power, reset, and clock management (PRCM) module. It is used by all ISS submodules and ISS top-level resources.
Resets				
DCT	DCT_RESET	CAM_RST	PRCM	ISS and SIMCOP global reset

For information about clock and reset management, see Section 8.4.1.2.1, *ISS SIMCOP Local Power and Clock Management*.

Table 8-1349. Hardware Requests

Interrupt Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
DCT	DCT_IRQ	SIMCOP_DCT_IRQ	SIMCOP IRQ merger	DCT operation is complete.

For more information about interrupt requests, see Section 8.4.1.2.3, *Interrupt Merger*.

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8.4.5.3 ISS SIMCOP DCT Functional Description

8.4.5.3.1 ISS SIMCOP DCT Block Diagram

The DCT implements 8 × 8, 2-dimensional (2D) DCT and IDCT specified in JPEG image coding standards:

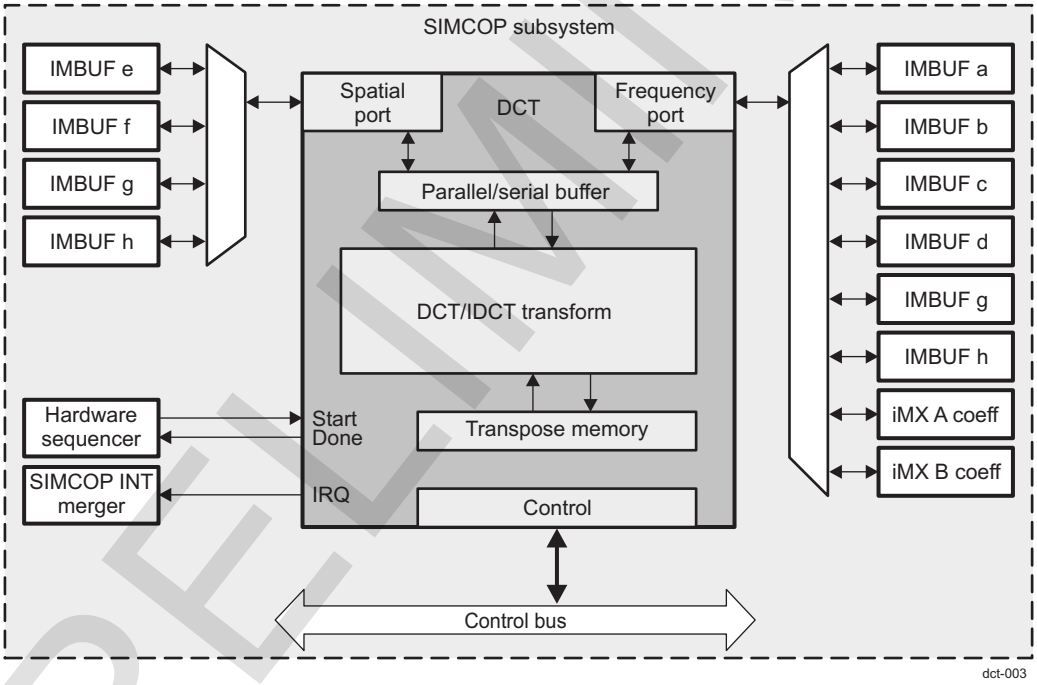
- In 4:2:0 mode, spatial domain data is organized in NV12 format. The frequency domain is organized as six blocks of 8 × 8.
- In 4:2:2 mode, spatial domain data is organized in UYVY format. The frequency domain is organized as four blocks of 8 × 8.
- In sequential 8 × 8 block mode, spatial and frequency domain data are organized as N blocks of 8 × 8 blocks.

NOTE:

- The spatial domain is the DCT input and IDCT output.
- The frequency domain is the DCT output and IDCT input.

Figure 8-270 is a block diagram of the DCT.

Figure 8-270. DCT Block Diagram



8.4.5.3.2 ISS SIMCOP DCT Power Management

Table 8-1350 describes the power-management features available for the DCT.

Table 8-1350. Local Power-Management Features

Feature	Registers	Description
Clock autogating	DCT_CFG[5] AUTOGATING	Free-running or autogating modes are available.

8.4.5.3.3 ISS SIMCOP DCT Interrupt Requests

Table 8-1351 lists the event flags, and their mask, that can cause module interrupts.

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Table 8-1351. Events

Event Flag	Event Mask	Map to	Description
N/A	DCT_CFG[3] INTEN	DCT_IRQ	End of processing

8.4.5.3.4 Control and Status

The DCT is controlled through the control registers accessed through the coprocessor bus by an external initiator. Before starting the DCT, the buffer memory must be configured for DCT access and initialized, and the control register must be set (for more information about DCT/IDCT processing, see Section 8.4.5.3.4.1, *DCT Configuration*).

The DCT_CFG[4] TRIG_SRC bit is used to select the DCT start source:

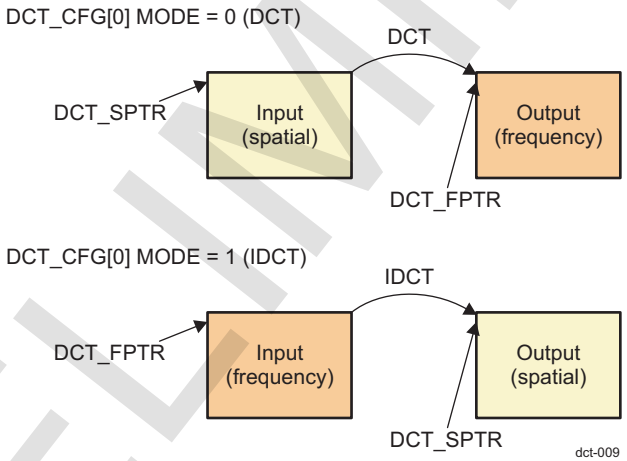
- If TRIG_SRC = 0, the DCT is started through the DCT_CTRL[0] EN bit.
- If TRIG_SRC = 1, the DCT is started by a hardware-start signal generated by the SIMCOP hardware sequencer.

When the DCT is configured for one trigger, the other trigger has no effect on the DCT.

An external initiator can read the state of the DCT (running or not running) by reading the DCT_CTRL[15] BUSY bit. When the BUSY bit goes back to 0, processing is complete (TRIG_SRC = 0 or 1).

Before starting the DCT, the DCT_SPTR and DCT_FPTR registers must be configured with spatial and frequency addresses. Figure 8-271 shows the use of spatial and frequency addresses.

Figure 8-271. DCT I/O Address Configuration



An interrupt can be generated when DCT operation completes (the configured number of MCUs for YUV4:2:0/4:2:2 mode, or the number of blocks for sequential block mode). To enable interrupt generation, set the DCT_CFG[3] INTEN bit to 1.

When the DCT_CFG[3] INTEN bit is set to 0, no interrupt generation is performed.

8.4.5.3.4.1 DCT Configuration

The following features can be configured in the DCT register:

- DCT module operation: The DCT_CFG[0] MODE bit configures the processing:
  - MODE = 0: DCT processing
  - MODE = 1: IDCT processing
- Number of MCUs to process: The number of MCUs to process –1 is configured in the DCT_CFG[13:8] NMCUS bit field:
  - YUV4:2:0 maximum MCUs = 21 (memory limitation, 126 blocks)
  - YUV4:2:2 maximum MCUs = 32 (128 blocks)

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– Sequential maximum MCUs = 64 (64 blocks)

8.4.5.3.5 Data Format

The DCT reads and writes data from and to image buffers. I/O format can be configured in the DCT_CFG[2:1] FMT bit field. The following formats can be configured:

- YUV4:2:0
- YUV4:2:2
- Sequential

8.4.5.3.5.1 YUV4:2:0 Format

In JPEG YUV4:2:0 format, each MCU is 16 × 16 pixels, and has 16 × 16 Y data points, 8 × 8 U data points, and 8 × 8 V data points. Each square array of 8 × 8 data points is called a block. Thus, an MCU with a YUV4:2:0 format has four Y blocks, one U block, and one V block.

This module follows the NV12 data storage format for YUV4:2:0 spatial data. For YUV4:2:0 format:

- line_offset_in_bytes = (DCT_CFG[13:8] NMCUS + 1) 16
- starting_addr_uv = DCT_SPTR + (DCT_CFG[13:8] NMCUS + 1) 256

Figure 8-272 shows the organization of the data for two MCUs in the spatial domain, when the DCT is configured to process two MCUs. To select the YUV4:2:0 format, write 0x0 in the DCT_CFG[2:1] FMT bit field. YUV4:2:0 processes six blocks (four Y, one U, and one V) during each MCU DCT processing.

Figure 8-272. YUV4:2:0 Format Data Order

Byte offset

	0	1	2	3		31
0	Y(0,0)	Y(1,0)	Y(2,0)	Y(3,0)	- - -	Y(15,0)
32	Y(0,1)	Y(1,1)	Y(2,1)	Y(3,1)	- - -	Y(15,1)
64	Y(0,2)	Y(1,2)	Y(2,2)	Y(3,2)	- - -	Y(15,2)
	⋮					
480	Y(0,15)	Y(1,15)	Y(2,15)	Y(3,15)	- - -	Y(15,15)
512	U(0,0)	V(0,0)	U(2,0)	V(2,0)	- - -	V(14,0)
544	U(0,2)	V(0,2)	U(2,2)	V(2,2)	- - -	V(14,2)
736	U(0,14)	V(0,14)	U(2,14)	V(2,14)	- - -	V(14,2)

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Each YUV4:2:0 has four Y blocks, one U block, and one V block. For the first MCU in Figure 8-272, the blocks are:

- Y_Block 0:
  - Y(0, 0), Y(1, 0), ..., Y(7, 0)
  - Y(0, 1), Y(1, 1), ..., Y(7, 1)
  - ....
  - Y(0, 7), Y(1, 7), ..., Y(7, 7)
- Y_Block 1:
  - Y(8, 0), Y(9, 0), ..., Y(15, 0)
  - Y(8, 1), Y(9, 1), ..., Y(15, 1)
  - ....
  - Y(8, 7), Y(9, 7), ..., Y(15, 7)
- Y_Block 2:
  - Y(0, 8), Y(1, 8), ..., Y(7, 8)
  - Y(0, 9), Y(1, 9), ..., Y(7, 9)

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  - ....
  - Y(0, 15), Y(1, 15), ..., Y(7, 15)
- Y_Block 3:
  - Y(8, 8), Y(9, 8), ..., Y(15, 8)
  - Y(8, 9), Y(9, 9), ..., Y(15, 9)
  - ....
  - Y(8, 15), Y(9, 15), ..., Y(15, 15)
- U_Block:
  - U(0, 0), U(2, 0), ..., U(14, 0)
  - U(0, 2), U(2, 2), ..., U(14, 2)
  - ....
  - U(0, 14), U(2, 14), ..., U(14, 14)
- V_Block:
  - V(0, 0), V(2, 0), ..., V(14, 0)
  - V(0, 2), V(2, 2), ..., V(14, 2)
  - ....
  - V(0, 14), V(2, 14), ..., V(14, 14)

8.4.5.3.5.2 YUV4:2:2 Format

In JPEG YUV4:2:2 format, each MCU is 16 × 8 pixels and has 16 × 8 Y data points, 8 × 8 U data points, and 8 × 8 V data points. Thus, an MCU with a YUV4:2:2 format has two Y blocks, one U block, and one V block.

This module follows the UYVY data storage format for YUV4:2:2 spatial data. For YUV4:2:2 format: line_offset_in_bytes = (DCT_CFG[13:8] NMCUS + 1) 32

Figure 8-273 shows the organization of the data for two MCUs in the spatial domain when the DCT is configured to process two MCUs. To select the YUV4:2:2 format, write 0x1 in the DCT_CFG[2:1] FMT bit field. YUV4:2:2 processes four blocks (two Y, one U, and one V) during each MCU DCT processing.

Figure 8-273. YUV4:2:2 Format Data Order

Byte offset

	0	1	2	3	4	5	6	7		31	32	33	34		63
0	U(0,0)	Y(0,0)	V(0,0)	Y(1,0)	U(2,0)	Y(2,0)	V(2,0)	Y(3,0)	- - -	Y(15,0)	U(16,0)	Y(16,0)	V(16,0)	- - -	Y(31,0)
64	U(0,1)	Y(0,1)	V(0,1)	Y(1,1)	U(2,1)	Y(2,1)	V(2,1)	Y(3,1)	- - -	Y(15,1)	U(16,1)	Y(16,1)	V(16,1)	- - -	Y(31,1)
128	U(0,2)	Y(0,2)	V(0,2)	Y(1,2)	U(2,2)	Y(2,2)	V(2,2)	Y(3,2)	- - -	Y(15,2)	U(16,2)	Y(16,2)	V(16,2)	- - -	Y(31,2)
	⋮								- - -					- - -	
448	U(0,7)	Y(0,7)	V(0,7)	Y(1,7)	U(2,7)	Y(2,7)	V(2,7)	Y(3,7)	- - -	Y(15,7)	U(16,7)	Y(16,7)	V(16,7)	- - -	Y(31,7)

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Each YUV4:2:2 has two Y blocks, one U block, and one V block. The four blocks of the first MCU are:

- Y_Block 0:
  - Y(0, 0), Y(1, 0), ..., Y(7, 0)
  - Y(0, 1), Y(1, 1), ..., Y(7, 1)
  - ....
  - Y(0, 7), Y(1, 7), ..., Y(7, 7)
- Y_Block 1:
  - Y(8, 0), Y(9, 0), ..., Y(15, 0)
  - Y(8, 1), Y(9, 1), ..., Y(15, 1)

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– ....
– Y(8, 7), Y(9, 7), ..., Y(15, 7)

8.4.5.3.5.3 Sequential Block Format

The sequential block format supports any color format other than YUV4:2:0 or YUV4:2:2. There is no notion of colors, and each 8 × 8 block is ordered sequentially. The DCT can be configured to process N blocks (versus N MCUs for YUV4:2:0 and YUV4:2:2, N is up to 64). In this format:

- Block i =
  – X(8*i, 0), X(8*i+1, 0), ..., X(8*i+7, 0)
  – X(8*i, 1), X(8*i+1, 1), ..., X(8*i+7, 1)
  – ....
  – X(8*i, 7), X(8*i+1, 7), ..., X(8*i+7, 7)

To select sequential block format, write 0x2 in the DCT_CFG[2:1] FMT bit field.

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8.4.5.4 ISS SIMCOP DCT Basic Programming Model

8.4.5.4.1 Initialization of Surrounding Modules

To initialize the DCT, the surrounding modules must be initialized. Table 8-1352 lists these modules.

Table 8-1352. Initialization of Surrounding Modules

Module	Minimum Required Setting	Optional Settings
CLKC	Enable the SIMCOP clock.	
Buffers	Configure DCT access to the image buffer.	
SIMCOP CTRL		Configure SIMCOP CTRL to handle DCT interrupts.

8.4.5.4.2 Using the DCT for DCT Processing

To configure the DCT for DCT processing, software must follow the procedure listed in Table 8-1353.

Table 8-1353. DCT Processing Procedure

Step	Register/Bit Field	Value
Prepare data in buffer memory.	SIMCOP buffers	
Switch buffer access to the DCT.	SIMCOP buffers	
Configure the start of the DCT input address (address must be in the memory buffer).	DCT_SPTR[12:5] ADDR	Start address (spatial domain)
Configure the start of the DCT output address (address must be in the memory buffer).	DCT_FPTR[13:4] ADDR	Start address (frequency domain)
Set the DCT_CFG register.	DCT_CFG[0] MODE	0 (DCT mode)
	DCT_CFG[2:1] FMT	Depends on data format
	DCT_CFG[3] INTEN	0: No interrupt 1: Interrupt at end of processing
	DCT_CFG[4] TRIG_SRC	1: Start controlled by hardware signal 0: Start controlled by a register
	DCT_CFG[13:8] NMCUS	Number of MCUs to process
IF: DCT_CFG[4] TRIG_SRC = 0		
Start DCT through the register.	DCT_CTRL[0] EN	1
ELSE		
Start the DCT using the hardware sequencer.	SIMCOP hardware sequencer	
ENDIF		

The DCT is now processing the blocks. To detect the end of DCT processing:

- If DCT_CFG[3] INTEN = 1, wait for the interrupt signal.
- If DCT_CFG[3] INTEN = 0, the processor must poll the DCT_CTRL[15] BUSY bit. When the BUSY bit is 0, processing is complete.

When DCT processing completes, the frequency output result is stored in the memory buffer at the address given by the DCT_FPTR[13:4] ADDR bit field.

8.4.5.4.3 Using the DCT for IDCT Processing

To configure the DCT for IDCT processing, software must follow the procedure listed in Table 8-1354.

Table 8-1354. IDCT Processing Procedure

Step	Register/Bit Field	Value
Prepare data in buffer memory.	SIMCOP buffers	
Switch buffer access to the DCT.	SIMCOP buffers	

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Table 8-1354. IDCT Processing Procedure (continued)

Step	Register/Bit Field	Value
Configure the start of the DCT output address (address must be in the memory buffer).	DCT_SPTR[12:5] ADDR	Start address (spatial domain)
Configure the start of the DCT input address (address must be in the memory buffer).	DCT_FPTR[13:4] ADDR	Start address (frequency domain)
Set the DCT_CFG register.	DCT_CFG[0] MODE	1 (IDCT mode)
	DCT_CFG[2:1] FMT	Depends on data format
	DCT_CFG[3] INTEN	0: No interrupt 1: Interrupt at end of processing
	DCT_CFG[4] TRIG_SRC	1: Start controlled by a hardware signal 0: Start controlled by a register
	DCT_CFG[13:8] NMCUS	Number of MCUs to process
IF: DCT_CFG[4] TRIG_SRC = 0		
Start the DCT through a register.	DCT_CTRL[0] EN	1
ELSE		
Start the DCT using hardware sequencer.	SIMCOP hardware sequencer	
ENDIF		

The DCT is now processing the blocks. To detect the end of IDCT processing:

- If DCT_CFG[3] INTEN = 1, wait for the interrupt signal.
- If DCT_CFG[3] INTEN = 0, the processor must poll the DCT_CTRL[15] BUSY bit. When the BUSY bit is 0, processing is complete.

When IDCT processing completes, the spatial output result is stored in the memory buffer at the address given by the DCT_SPTR[12:5] ADDR bit field.

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8.4.5.5 ISS SIMCOP DCT Register Manual

8.4.5.5.1 ISS SIMCOP DCT Instance Summary

Table 8-1355 summarizes the DCT instance.

Table 8-1355. ISS SIMCOP DCT Instance Summary

Module Name	Base Address L3 Interconnect	Base Address Cortex-M3 Private Access	Size
DCT	0x5202 0800	0x5506 0800	32 bytes

NOTE: Private Access is an access that does not use the L3/L4 interconnects.

8.4.5.5.2 DCT Registers

8.4.5.5.2.1 DCT Register Summary

Table 8-1356 summarizes the DCT register mapping.

Table 8-1356. DCT Register Mapping Summary

Register	Type	Register Width (Bits)	Address Offset	Physical Address L3 Interconnect	Physical Address Cortex-M3 Private Access
DCT_VERSION	R	32	0x0000 0000	0x5202 0800	0x5506 0800
DCT_CTRL	RW	32	0x0000 0004	0x5202 0804	0x5506 0804
DCT_CFG	RW	32	0x0000 0008	0x5202 0808	0x5506 0808
DCT_SPTR	RW	32	0x0000 000C	0x5202 080C	0x5506 080C
DCT_FPTR	RW	32	0x0000 0010	0x5202 0810	0x5506 0810

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8.4.5.5.2.2 DCT Register Descriptions

through describe the registers in detail.

Table 8-1357. DCT_VERSION

Address Offset	0x0000 0000		
Physical Address	0x5202 0800 0x5506 0800	**Instance**	DCT_L3 DCT_CORTEX-M3
Description	IP Revision		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP Revision	R	See (1)

(1) TI internal data

Table 8-1358. Register Call Summary for Register DCT_VERSION

ISS Still Image Coprocessor

- ISS SIMCOP DCT Register Manual: [0]

Table 8-1359. DCT_CTRL

Address Offset	0x0000 0004		
Physical Address	0x5202 0804 0x5506 0804	**Instance**	DCT_L3 DCT_CORTEX-M3
Description	DCT control register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																BUSY	RESERVED														EN

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Read returns 0.	R	0x0000
15	BUSY	IDCT/busy status 0: Idle 1: Busy	R	0x0
14:1	RESERVED	Read returns 0.	R	0x0000
0	EN	Write 1 when DCT_CFG[4] TRIG_SRC = 0 to start module operation. Read returns 0.	W	0x0

Table 8-1360. Register Call Summary for Register DCT_CTRL

ISS Still Image Coprocessor

- ISS SIMCOP DCT Functional Description: [0] [1]
- ISS SIMCOP DCT Basic Programming Model: [2] [3] [4] [5]
- ISS SIMCOP DCT Register Manual: [6]

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Table 8-1361. DCT_CFG

Address Offset	0x0000 0008		
Physical Address	0x5202 0808 0x5506 0808	**Instance**	DCT_L3 DCT_CORTEX-M3
Description	DCT configuration register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																NMCUS								RESERVED		AUTOGATING		TRIG_SRC		INTEN		FMT		MODE	

Bits	Field Name	Description	Type	Reset
31:14	RESERVED	Read returns 0.	R	0x00000
13:8	NMCUS	Number of MCUs (for FMT = 0, 1) or blocks (for FMT = 2) 0 = 1 MCU or block 1 = 2 MCUs or blocks ... 63 = 64 MCUs or blocks	RW	0x00
7:6	RESERVED	Read returns 0.	R	0x0
5	AUTOGATING	Internal clock gating on interface and functional clocks 0: Clocks are free-running 1: Clocks are gated off in subblocks that are not required for operation.	RW	0x0
4	TRIG_SRC	Trigger source 0: Memory mapper register 1: Hardware start signal	RW	0x0
3	INTEN	0: Interrupt disabled 1: Interrupt enabled	RW	0x0
2:1	FMT	Data format 0: YUV4:2:0 format 1: YUV4:2:2 format 2: Sequential blocks format 3: Reserved	RW	0x0
0	MODE	0: DCT 1: IDCT	RW	0x0

Table 8-1362. Register Call Summary for Register DCT_CFG

ISS Still Image Coprocessor

- ISS SIMCOP DCT Functional Description: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13]
- ISS SIMCOP DCT Basic Programming Model: [14] [15] [16] [17] [18] [19] [20] [21] [22] [23] [24] [25] [26] [27] [28] [29] [30] [31]
- ISS SIMCOP DCT Register Manual: [32] [33]

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Table 8-1363. DCT_SPTR

Address Offset	0x0000 000C		
Physical Address	0x5202 080C 0x5506 080C	**Instance**	DCT_L3 DCT_CORTEX-M3
Description	Spatial-domain data pointer, byte address		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								ADDR							
																														RESERVED	

Bits	Field Name	Description	Type	Reset
31:13	RESERVED	Read returns 0.	R	0x00000
12:5	ADDR	Address in 256-bit words Intention is that software write a byte address into the register. Hardware ignores the lowest 5 bits and bits 12..5 specifies the 256-bit/word memory address..	RW	0x00
4:0	RESERVED	Read returns 0.	R	0x00

Table 8-1364. Register Call Summary for Register DCT_SPTR

ISS Still Image Coprocessor

- ISS SIMCOP DCT Functional Description: [0] [1]
- ISS SIMCOP DCT Basic Programming Model: [2] [3] [4]
- ISS SIMCOP DCT Register Manual: [5]

Table 8-1365. DCT_FPTR

Address Offset	0x0000 0008		
Physical Address	0x5202 0810 0x5506 0810	**Instance**	DCT_L3 DCT_CORTEX-M3
Description	Frequency-domain data pointer, byte address		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								ADDR							
																														RESERVED	

Bits	Field Name	Description	Type	Reset
31:14	RESERVED	Read returns 0.	R	0x00000
13:4	ADDR	Address in 128-bit words. Intention is that software write a byte address into the register. Hardware ignores the lowest 4 bits and bits 13..4 specifies the 128-bit/word memory address.	RW	0x000
3:0	RESERVED	Read returns 0.	R	0x0

Table 8-1366. Register Call Summary for Register DCT_FPTR

ISS Still Image Coprocessor

- ISS SIMCOP DCT Functional Description: [0]
- ISS SIMCOP DCT Basic Programming Model: [1] [2] [3]
- ISS SIMCOP DCT Register Manual: [4]

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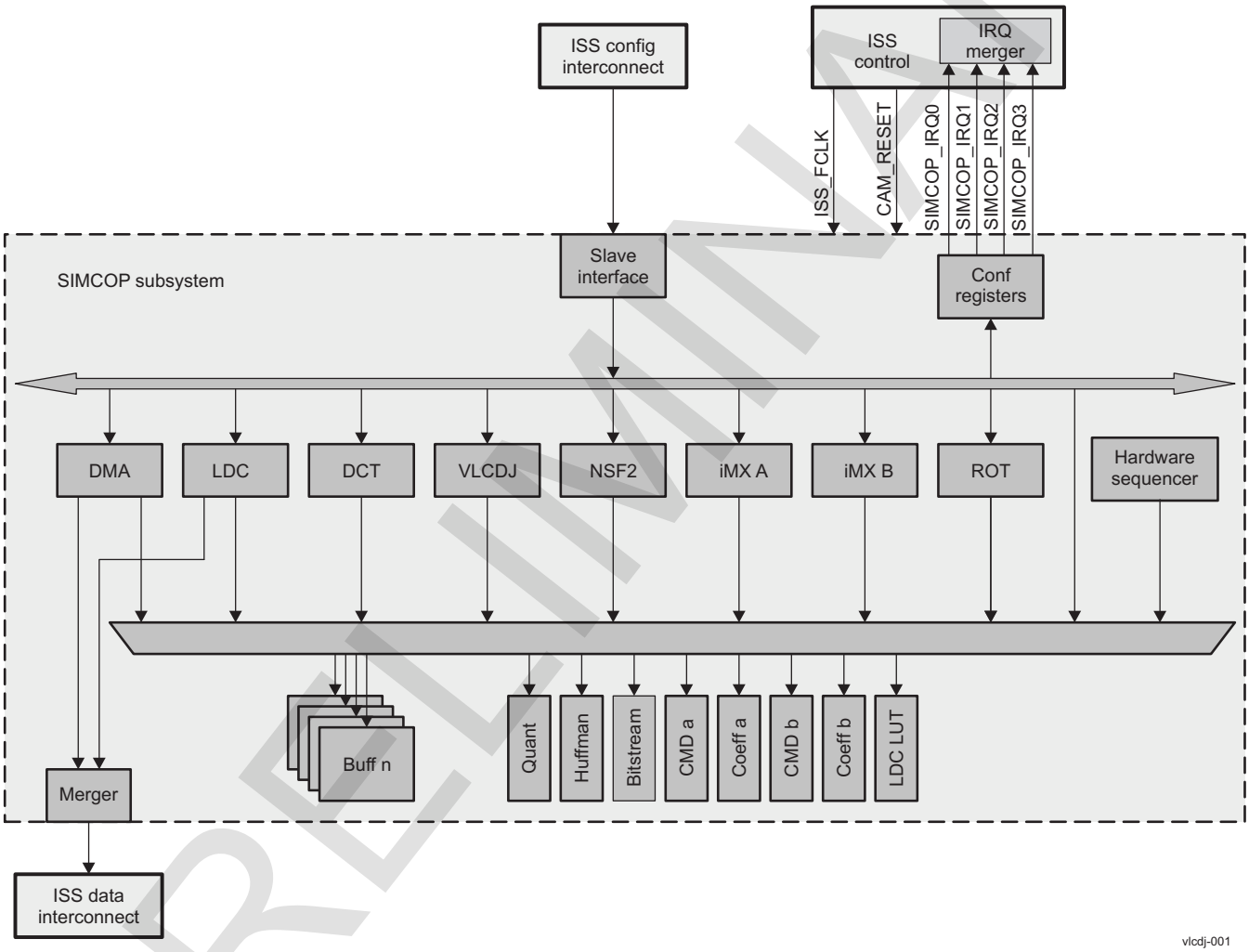
8.4.6 ISS SIMCOP Variable Length Coder/Decoder for JPEG Module

This section describes the variable-length coder/decoder for JPEG (VLCDJ) module in the still-image coprocessor (SIMCOP) subsystem.

8.4.6.1 ISS SIMCOP VLCDJ Overview

The VLCDJ module handles quantization (Q) and variable-length coding (VLC) in JPEG encoding, and variable-length decoding (VLD) and inverse quantization (IQ) in JPEG decoding. These operations are required for JPEG image compression and decompression. Figure 8-274 is an overview of the VLCDJ in the SIMCOP subsystem.

Figure 8-274. VLCDJ in the SIMCOP Subsystem



The VLCDJ supports the following operations:

- Q and VLC for JPEG encoding
- VLD and IQ for JPEG decoding
- Data formats:
  - YUV4:2:0 format in 16 × 16-pixel microcontroller unit (MCU)
  - YUV4:2:2 format in 16 × 8-pixel MCU
  - Sequential block mode to support arbitrary color component configuration within JPEG baseline sequential (software intervention required to context-switch among color components)
- Configurable for number of MCUs per initiation (up to 21 MCUs for YUV4:2:0, 32 MCUs for YUV4:2:2,

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64 8 × 8 blocks for sequential block mode)

- Discrete cosine transform (DCT) coefficients are stored sequentially for each 8 × 8 block, 16 bits per data point
- Stall processing for interface with bitstream data overrun/underrun protection
- Insertion of restart markers during encoding (YUV4:2:0, YUV4:2:2, sequential block modes)
- Record of restart marker locations during encoding (YUV4:2:0, YUV4:2:2 only)
- Processing of restart markers on the MCU boundary during decoding, reset of direct coefficient (DC) predictors as required by the JPEG standard (YUV4:2:0, YUV4:2:2, sequential block modes)

8.4.6.2 ISS SIMCOP VLCDJ Integration

The VLCDJ is part of the SIMCOP subsystem in the imaging subsystem (ISS). Figure 8-275 shows the integration of the VLCDJ in the SIMCOP subsystem.

Figure 8-275. VLCDJ Engine Integration

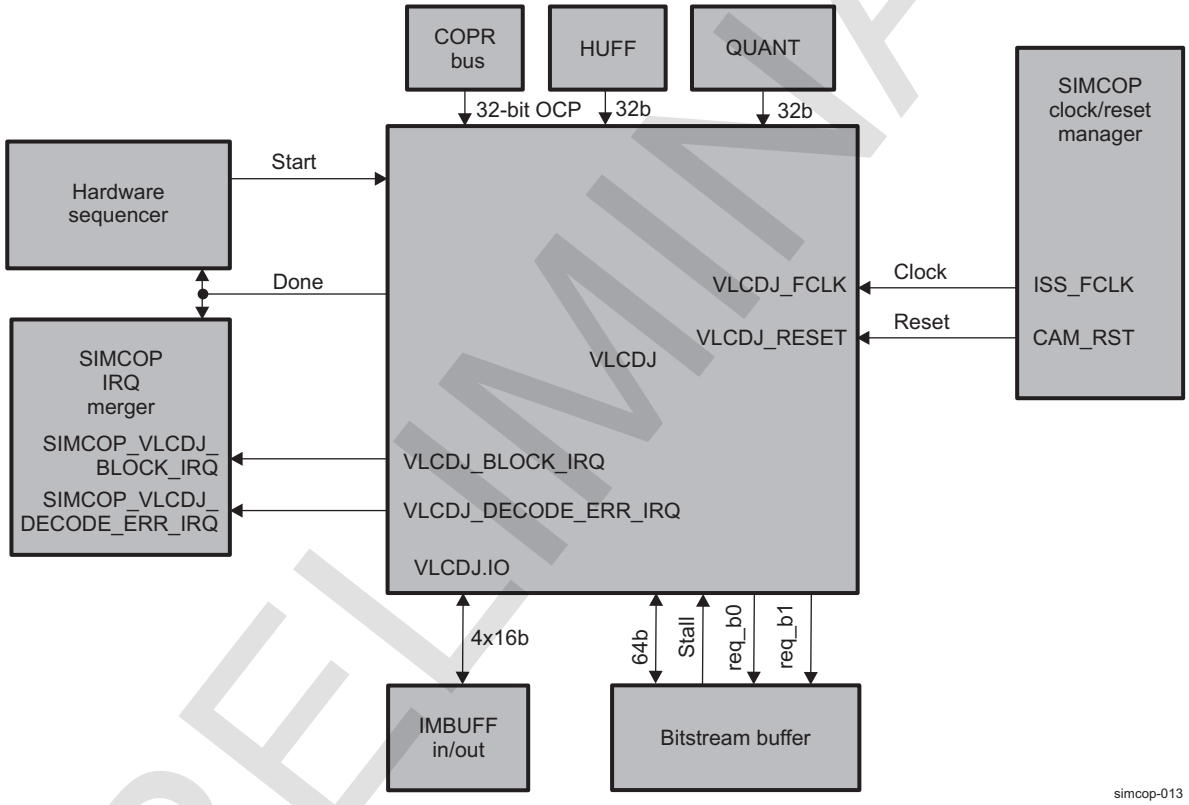

Table 8-1367 through Table 8-1369 list the integration attributes, clocks and resets, and hardware requests, respectively, for the VLCDJ.

Table 8-1367. Integration Attributes

Module Instance	Attributes
	Power Domain
VLCDJ	PD_CAM

Table 8-1368. Clocks and Resets

Clocks				
Module Instance	Destination Signal Name	Source Signal Name	Source	Description

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Table 8-1368. Clocks and Resets (continued)

VLCDJ	VLCDJ_FCLK	ISS_FCLK	PRCM	Functional clock provided by ISS_CLK from the power, reset, and clock management (PRCM) module. It is used by all ISS submodules and ISS top-level resources.
		Resets		
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
VLCDJ	VLCDJ_RESET	CAM_RST	PRCM	ISS and SIMCOP global reset

For information about clock and reset management, see Section 8.4.1.2.1, *ISS SIMCOP Local Power and Clock Management*.

Table 8-1369. Hardware Requests

		Interrupt Requests		
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
VLCDJ	VLCDJ_BLOCK_IRQ	SIMCOP_VLCDJ_BLOCK_IRQ	SIMCOP IRQ merger	A macroblock has been processed.
VLCDJ	VLCDJ_DECODE_ERR_IRQ	SIMCOP_VLCDJ_DECODE_ERR_IRQ	SIMCOP IRQ merger	A decode error has been signaled by the VLCDJ.

For more information about interrupt requests, see Section 8.4.1.2.3, *Interrupt Merger*.

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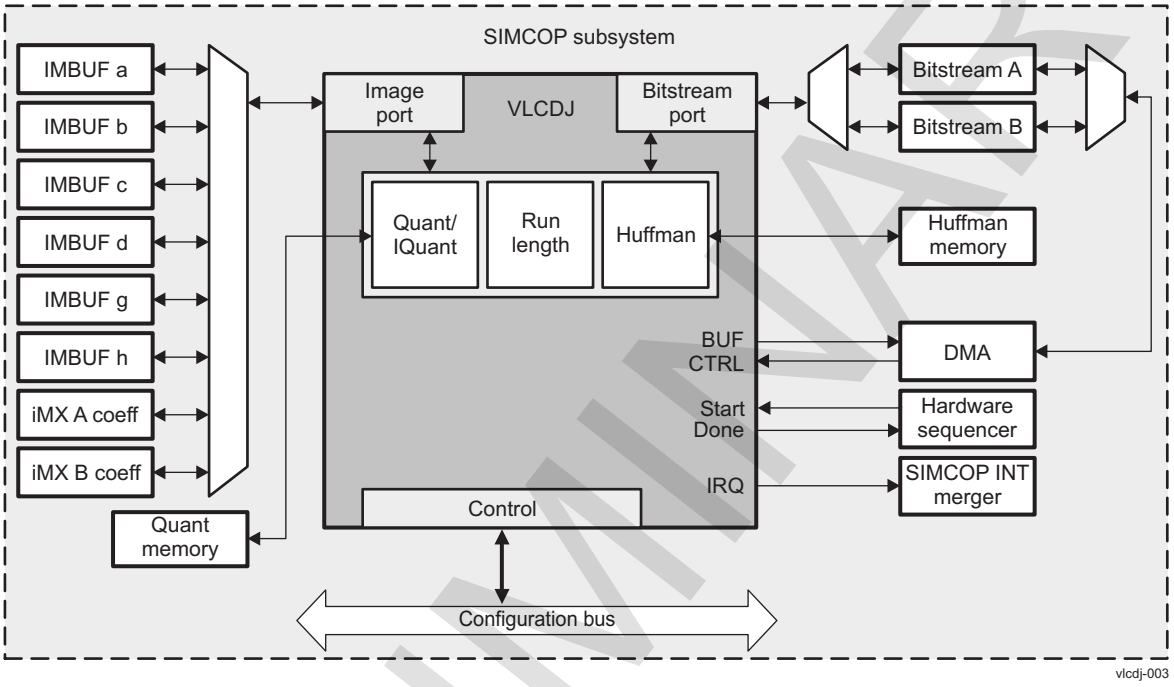
8.4.6.3 ISS SIMCOP VLCDJ Functional Description

8.4.6.3.1 ISS SIMCOP VLCDJ Block Diagram

The VLCDJ implements quantization, run-length encode, and Huffman encode stages of JPEG compression, and Huffman decode, run-length expansion, and dequantization stages of JPEG decompression. Figure 8-276 is a block diagram of the VLCDJ with connected memories and modules.

Figure 8-276. VLCDJ Block Diagram



8.4.6.3.2 ISS SIMCOP VLCDJ Power Management

The VLCDJ uses clock autogating to conserve power. When any substantial subblocks are not in use, the corresponding clock trees are gated off. Table 8-1370 describes the power-management feature available for the VLCDJ.

Table 8-1370. Local Power-Management Feature

Feature	Registers	Description
Clock autogating	VLCDJ_CTRL[3] AUTOGATING	Free-running or autogating modes are available.

8.4.6.3.3 ISS SIMCOP VLCDJ Interrupt Requests

Table 8-1371 lists the event flags and their masks that can cause module interrupts.

Table 8-1371. Events

Event Flag	Event Mask	Map to	Description
N/A	VLCDJ_CTRL[4] INTEN_DONE	VLCDJ_BLOCK_IRQ	End of block processing
N/A	VLCDJ_CTRL[5] INTEN_ERR	VLCDJ_DECODE_ER R_IRQ	Error occurred

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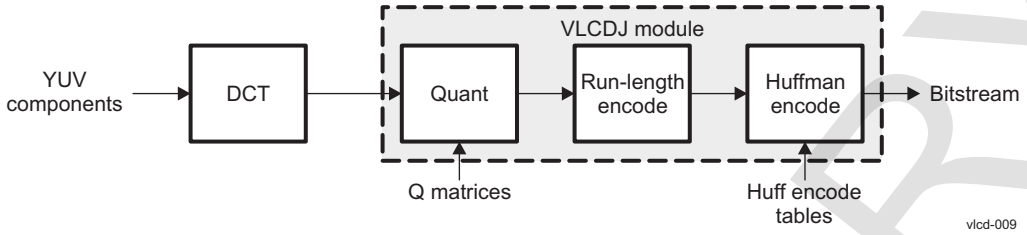
8.4.6.3.4 ISS SIMCOP VLCDJ in JPEG Encoding Flow

Figure 8-277 shows the JPEG compression or encoding flow.

Figure 8-277. JPEG Encoding Flow



The DCT coefficients are quantized by dividing each data point with a quantizer. The quantizers form an 8 × 8 matrix for Luma Y, and another 8 × 8 matrix for U and V, and the matrices are fixed in each image. The quantizer matrices can vary between images, and are sometimes fine-tuned in a multiple-pass process to regulate the compressed JPEG file size.

For quantization, the VLCDJ reads a reciprocal of the quantizer values (16 bits per entry carrying 2^{15}/quant) so that hardware performs multiplications rather than divisions. The result is rounded to the nearest integer.

After quantization, the DC terms (the first term in each 8 × 8 block of DCT coefficients) are differentially coded within each color. Thus, three predictors are used for the common formats.

Next, the coefficients are scanned in a zigzag order (the same order for all colors) to form DC term + zero-run and nonzero level pairs for the alternative coefficient (AC) terms. The run-level pairs are then coded with a Huffman table.

The DC level is first categorized into size groups, basically the number of bits that represents the absolute value of the level. This size is translated to a bit segment using the Huffman table. Then, additional bits are appended to represent the exact DC level.

For AC run-level pairs, the process is similar. Each AC level is first categorized into size groups, basically the number of bits that represents the absolute value of the level. The size and the run are combined and translated to a bit segment using the Huffman table. Then, additional bits are appended to represent the exact AC level.

The number of additional bits to encode after the Huffman-coded segment, for DC or AC level, equals the size value. For example, coefficient values –3, –2, and 3 are of size 2, because 2 bits are required to represent the absolute values 2 and 3. There are four coefficient values in the size –2 category, so 2 additional bits are required to uniquely identify each value.

Some special symbols go with the AC run/size pairs. The ZRL symbol represents a run of 15 zeros, and is used to code unusually long zero runs. The EOB symbol represents end of block, meaning that there are only 0 AC coefficients at the end.

In the bitstream management level, after each byte of 0xFF, a byte of 0 is inserted to prevent the decoder from detecting special markers in the bitstream.

Because the VLCDJ handles multiple MCUs and allows restart marker insertion in MCU boundaries inside a task, the inserted flags are flagged to prevent the insertion of a 0 byte after 0xFF.

8.4.6.3.5 ISS SIMCOP VLCDJ in JPEG Decoding Flow

Decoding or decompression operates in the reverse order, as shown in Figure 8-278.

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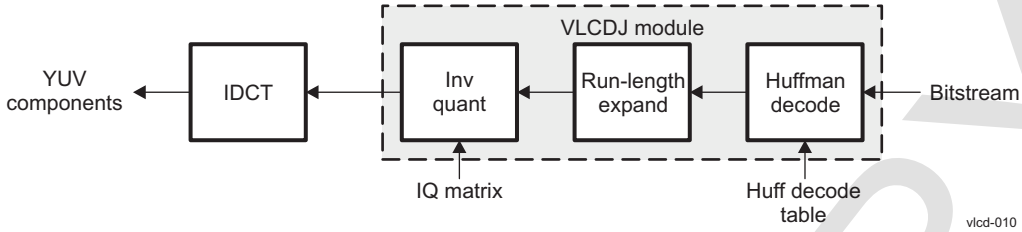
Figure 8-278. JPEG Decoding Flow



1. In decoding, in the MCU data section, when the VLCDJ recognizes the 0xFF byte in the bitstream, it detects whether the next byte is a 0 byte. If it is, the 0 byte is removed and decoding continues as if the 0 byte is not there (the 0xFF byte is kept). If the next byte is not a 0 byte, the VLCDJ flags this as a JPEG data error. This can be caused by an earlier bitstream error that causes the module to parse outside the MCU entropy data and into markers that are not supported by the module.
2. Because the VLCDJ decodes for multiple MCUs, restart markers can occur in MCU boundaries. Restart marker detection and processing work with the 0 byte removal logic to ensure that restart markers are detected and removed correctly. When the VLCDJ detects a restart marker, it resets the DC predictors in the IQ stage.
3. The VLCDJ looks up the Huffman table to convert a variable-length bit segment into a DC size or an AC run/size pair. The number of additional bits equal to the size is extracted and the DC/AC coefficient is reconstructed. Then, zero runs are expanded.
4. IQ is performed, which is simply multiplication of the coefficients with values in the quantizer matrices.

8.4.6.3.6 Memory Interfaces

The VLCDJ has four memory interfaces (all memories are inside the SIMCOP subsystem):

- Image buffer (input DCT coefficients for encoding and output DCT coefficients for decoding)
- Quantizer memory
- Huffman memory
- Bitstream memory (output for encoding and input for decoding)

8.4.6.3.6.1 Image Buffer

An image buffer stores DCT data in the context of the VLCDJ. This is an input in encode mode and an output in decode mode.

When multiple MCUs are configured, DCT coefficients for the MCUs are stored sequentially (MCU 0 is stored first, followed by MCU 1, and so on).

Blocks in an MCU are stored sequentially; that is, block 0 first, block 1 next, and so on. There are six blocks per MCU in YUV4:2:0 format, {Y0, Y1, Y2, Y3, U, V}, and four blocks per MCU in YUV4:2:2 format, {Y0, Y1, U, V}.

The 64 DCT coefficients for each block are stored in an 8 × 8 transposed format (the companion DCT module handles the transposed format). Each coefficient, up to [–2047, 2047] in range is stored on a 16-bit word. Table 8-1372 lists the data format in each 8 × 8 block of coefficients.

Table 8-1372. Image Buffer Block Format

Byte Offset								
0	1	2	3	4	5	...	14	15
c(0, 0)		c(0, 1)		c(0, 2)		...	c(0, 7)	
c(1, 0)		c(1, 1)		c(1, 2)		...	c(1, 7)	
c(2, 0)		c(2, 1)		c(2, 2)		...	c(2, 7)	
:								
c(7, 0)		c(7, 1)		c(7, 2)		...	c(7, 7)	

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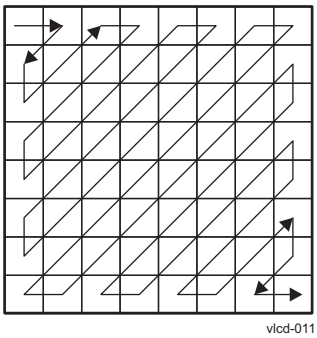
The DCT coefficients are processed in zigzag order (seeFigure 8-279), as required by JPEG.

Figure 8-279. JPEG Zigzag Order



8.4.6.3.6.2 Quantizer Memory

The quantization memory stores the reciprocal of quantizers, 2^{15}/qmat[i][j] so that hardware performs multiplications rather than divisions. Each data point is stored in 16 bits.

The quantizer matrices have a fixed size, 64 16-bit elements each. The quantizer memory (QMEM) is sized to hold up to four matrices (Table 8-1373 lists the recommended allocation for YUV4:2:0 and YUV4:2:2).

Table 8-1373. Recommended QMEM Allocation for YUV4:2:0 and YUV4:2:2

Quadrant of QMEM	Address Offset (Bytes)	Contents
00	0x000	(Encode) Quantizer reciprocal for Y (2^{15}/qmat[i][j])
01	0x080	(Encode) Quantizer reciprocal for UV (2^{15}/qmat[i][j])
10	0x100	(Decode) Quantizer for Y (qmat[i][j])
11	0x180	(Decode) Quantizer for UV (qmat[i][j])

Each matrix is stored in zigzag order to make quantization and inverse quantization more efficient.

8.4.6.3.6.3 Huffman Memory

Huffman memories store Huffman encode tables and Huffman control/decode tables. For information about Huffman tables, see Section 8.4.6.3.7, *Huffman Table Organization*.

8.4.6.3.6.4 Bitstream Memory

Bitstream memory is for input/output (I/O) bitstream. Bitstream data is stored in little-endian format in the memory. Circular buffer (CBUFF) start and end addresses are provided in registers to facilitate bitstream data management:

- VLCDJE_CBUF[11:10] START, start of ring buffer for encode mode (address must be 1KB-aligned)
- VLCDJE_CBUF[27:26] END, end of ring buffer for encode mode (address must be 1KB-aligned)
- VLCDJD_CBUF[11:10] START, start of ring buffer for decode mode (address must be 1KB-aligned)
- VLCDJD_CBUF[27:26] END, end of ring buffer for decode mode (address must be 1KB-aligned)

Figure 8-280 shows the start and end addresses of a ring buffer.

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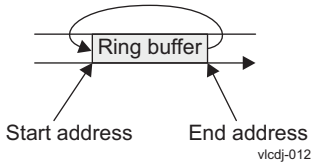
Figure 8-280. VLCDJ Ring Buffer



In encoding and decoding, a bit-level boundary defines bitstream data written (for encoding) or parsed (for decoding). To point to that boundary, bit and byte pointers are provided in the registers:

- VLCDJE_BSPTR[19:16] BITPTR (encoding)
- VLCDJE_BSPTR[11:0] BYTEPTR (encoding)
- VLCDJD_BSPTR[19:16] BITPTR (decoding)
- VLCDJD_BSPTR[11:0] BYTEPTR (decoding)

BYTEPTR (byte pointer) points to the byte where the boundary lies, and BITPTR (bit pointer) specifies the number of available vacant data bits (for encoding) or remaining data bits (for decoding). BITPTR is always in the range of 1 to 8, where 8 indicates that an entire byte is available for writing or reading.

For example, for encoding, if BYTEPTR = 0 and BITPTR = 8, after the hardware encodes a specified number of MCUs that together generate 30 bits, or 3 full bytes and 6 bits, BYTEPTR = 3 and BITPTR = 2. The JPEG standard requires that at the end of MCU data, any remaining bits of the last byte are padded with 1s. For example, if the last byte has 4 bits written 0101, the last byte of MCU data in the JPEG data is 0x5F.

8.4.6.3.7 Huffman Table Organization

8.4.6.3.7.1 Huffman Table for Encode Mode

Because the Huffman encode tables are compact, they are fixed relative to a common pointer:

- The Luma DC table starts at VLCDJE_VLCTBL[11:2] ADDR (12 entries × 4 = 48 bytes)
- The Luma AC table starts at VLCDJE_VLCTBL[11:2] ADDR + 48 bytes (11 × 16 × 4 = 704 bytes)
- The Chroma DC table starts at VLCDJE_VLCTBL[11:2] ADDR + 752 bytes (12 entries × 4 = 48 bytes)
- The Chroma AC table starts at VLCDJE_VLCTBL[11:2] ADDR + 800 bytes (11 × 16 × 4 = 704 bytes)

For DC tables, the index of each table corresponds to the size of the absolute value of the DC coefficient.

For AC tables, the index of each table corresponds to a formula including the size (of absolute value of nonzero AC coefficients) and the zero run: Index = SIZE × 16 + run. Because the size cannot be 0, the first 16 entries hold special symbols. EOB is at entry 0, and ZRL is at entry 15.

The size of a nonnegative value is the number of bits required to represent the value (for example, a size of 4..7 = 3).

Figure 8-281 shows the organization of the Huffman encode table.

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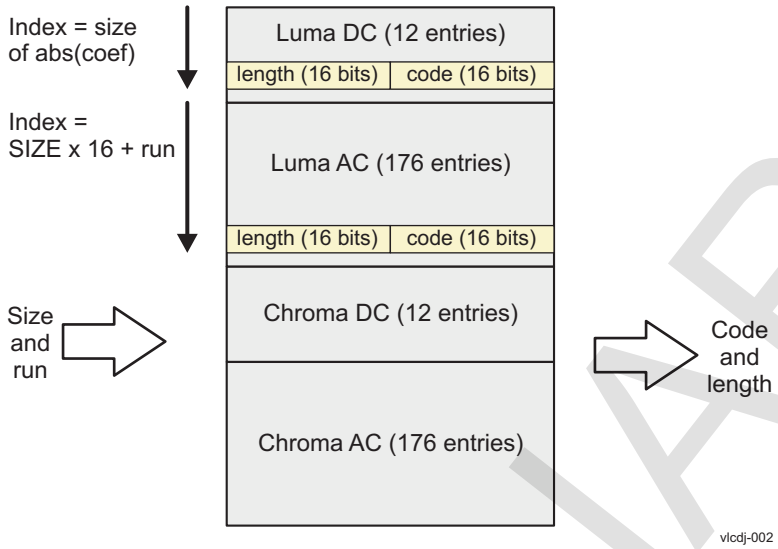
Figure 8-281. Huffman Encode Table Organization



8.4.6.3.8 Restart Marker

8.4.6.3.8.1 Restart Marker Insertion for Encode

As specified in the JPEG standard, the VLCDJ can insert a restart marker at a specified MCU interval (for information about restart markers, see Section 8.4.6.3.5, *ISS SIMCOP VLDCJ in JPEG Decoding Flow*). Any remaining bits in the last partial byte are padded with 1s.

When enabled, the VLCDJ inserts a restart marker at the end of a group of MCUs. A partial byte is automatically padded with 1s.

8.4.6.3.8.2 Restart Marker Location Recording

To facilitate reordering of compressed JPEG data sections to achieve JPEG rotation, the VLCDJ also records the restart marker locations.

8.4.6.3.8.3 Restart Marker Handling for Decoding

Restart markers are handled automatically during MCU data decoding according to the JPEG standard. The DC predictors are reset at the MCU boundary where restart markers are present.

Because the handling of restart markers is complex, there is no check of the consistency of restart marker value or existence/nonexistence with the restart interval (which is not part of the decoder register setting). Correct JPEG files are decoded correctly. Incorrect JPEG files can escape error detection.

To decode correctly, in spite of the presence of restart markers, software must configure the VLCDJ with the correct byte pointer for the VLCDJ. To reset DC predictors to occur before an MCU, the byte pointer must point to the restart marker before the MCU data in the bitstream data. In other words, the VLCDJ does not search for the correct marker and resume MCU decoding after the marker. The VLCDJ detects the presence of the marker only at the MCU boundaries.

8.4.6.3.9 Encode/Decode Context Switching

The bitstream memory is organized as two banks of memory. When the VLCDJ performs only encoding or only decoding, the two banks are used to achieve VLCDJ and DMA concurrence, and automatic bitstream data DMA is supported.

When the VLCDJ performs one encode and one decode concurrently, both contexts can coexist in the configuration registers, because encode and decode configurations are in separate registers. The bitstream memory must be partitioned half-and-half between encode and decode. For example:

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- VLCDJE_CBUF[11:10] START = 0x0
- VLCDJE_CBUF[27:26] END = 0x7FF
- VLCDJD_CBUF[11:10] START = 0x800
- VLCDJD_CBUF[27:26] END = 0xFFF

The byte pointers and the bitstream data DMA must be set up accordingly.

When the VLCDJ is encoding, the decode half of bitstream memory can be refilled by DMA. When the VLCDJ is decoding, the encode half of bitstream memory can be transferred out by DMA. Hardware does not support automatic triggering of DMA; software must submit DMA based on the byte pointer value of each context. For good SDRAM efficiency, the DMA block must be aligned correctly.

8.4.6.3.10 Using Sequential Block Mode for YUV4:4:4 Encoding/Decoding

In sequential block mode, because it deals with only one color component, the VLCDJ does the following:

- Uses DCPREDY for the DC predictor
- Uses the first quantizer matrix pointed by QM/QMR
- Starts from the first block pointed to by DCT
- Uses the first VLC/VLD table

Thus, to encode/decode YUV4:4:4 format using sequential block mode, software must switch context among Y, U, and V between initiations of the VLCDJ. Memory organization and registers are designed so that QM/QMR, DCT, and VLC/VLD tables can be swapped by changing the corresponding pointers in the registers. The DC predictor must be saved and restored.

For more information, see Section 8.4.6.4.6, *Example of YUV4:4:4 Encoding*.

8.4.6.3.11 Error Reporting

The VLCDJ can report the following decode errors:

- Invalid Huffman code
- Block exceeding 64 coefficients

NOTE: Decoding of an 0xFF byte followed by a nonzero byte is not reported as an error (for more information, see Section 8.4.6.3.5, *ISS SIMCOP VLCDJ in JPEG Decoding Flow*).

When there is a decode error, VLCDJ operation is suspended immediately. Bit and byte pointers to the bitstream near where the error occurs are reflected in the VLCDJD_BSPTR[19:16] BITPTR and VLCDJD_BSPTR[11:0] BYTEPTR bit fields. The DCT coefficient index, in zigzag order of the task, near where the error occurs, is also reflected in a read-only bit field, VLCDJD_DCTERR[13:0] ERRPTR. For example, if decoding fails at the fifth coefficient of the third block of the VLCDJ task (which can be multiple MCUs), ERRPTR returns 2 × 64 + 4 = 195.

The IQ stage of the hardware does not stop and runs to completion. When there is a decode error, the DC predictor and decoded DCT coefficient outcomes are indeterminate.

Because the VLCDJ does not start in the middle of an MCU, software must recover from the error and configure the VLCDJ from an MCU boundary.

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8.4.6.4 ISS SIMCOP VLCDJ Basic Programming Model

8.4.6.4.1 Initialization of Surrounding Modules

To initialize the VLCDJ, surrounding modules must be initialized. Table 8-1374 lists these modules.

Table 8-1374. Initialization of Surrounding Modules

Module	Minimum Required Setting	Optional Settings
CLKC	Enable the SIMCOP clock.	
Buffers	Configure VLCDJ access to the image buffer.	
SIMCOP CTRL		Configure SIMCOP CTRL to handle VLCDJ interrupts.

8.4.6.4.2 ISS SIMCOP VLCDJ Start and Register Modification During Processing

The module operation can be started with two mechanisms, depending on the status of the VLCDJ_CTRL[2] TRIG_SRC bit.

When the VLCDJ_CTRL[2] TRIG_SRC bit is set to 0 and the module is idle (the VLCDJ_CTRL[16] BUSY bit is set to 0), the module is started by setting the VLCDJ_CTRL[0] EN bit to 1. Any hardware start pulses are ignored. To simplify software control, in the same register write, changing the VLCDJ_CTRL[2] TRIG_SRC bit from 1 to 0 and setting the VLCDJ_CTRL[0] EN bit to 1 is recognized as a valid starting condition.

When the VLCDJ_CTRL[2] TRIG_SRC bit is set to 1 and the module is idle (the VLCDJ_CTRL[16] BUSY bit is set to 0), the module is started by the START signal going active. Any software write to the VLCDJ_CTRL[0] EN bit is ignored.

During encoding, encode configuration registers must not be modified by software, whereas decode configuration registers can be freely modified.

During decoding, decode configuration registers must not be modified by software, whereas encode configuration registers can be freely modified.

8.4.6.4.3 JPEG Encoding

For JPEG encoding of a YUV4:2:0 image consisting of eight MCUs per task, software first composes the JPEG header, which includes image dimension, YUV4:2:0 format, Huffman tables, quantizer matrices, and the start-of-scan marker and scan header, all before the MCU data. Software then sets up the encoding task, once per image, with the procedure listed in Table 8-1375.

Table 8-1375. JPEG Encoding Procedure

Step	Register/Bit Field	Value
Configure the encode configuration register.	VLCDJE_CFG[1:0] FMT	0 (YUV4:2:0 mode)
	VLCDJE_CFG[13:8] NMCUS	7 (eight MCUs)
	VLCDJE_CFG[2] RSTEN	0 (no restart marker)
Configure the DC predictor.	VLCDJE_DCPREDY[11:0] PREDY	0 (reset DC predictor for Y)
	VLCDJE_DCPREDUV[11:0] PREDU	0 (reset DC predictors for U)
	VLCDJE_DCPREDUV[27:16] PREDV	0 (reset DC predictors for V)
Configure the input and output memories.	VLCDJE_BSPTR[11:0] BYTEPTR	0 (beginning of bitstream memory)
	VLCDJE_BSPTR[19:16] BITPTR	8 (initially empty byte, thus 8 free bits)
	VLCDJE_CBUF[11:10] START	0 (bitstream starts from beginning of first quadrant of bitstream memory)
	VLCDJE_CBUF[27:26] END	3 (bitstream ends at end of fourth quadrant of bitstream memory)
	VLCDJE_DCTQM[13:4] DCT	0 (DCT coefficients at beginning of image buffer)

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Table 8-1375. JPEG Encoding Procedure (continued)

Step	Register/Bit Field	Value
Configure Huffman and quantizer memory pointers.	VLCDJE_DCTQM[24:23] QMR	0 (quantizer matrix reciprocal at beginning of QMEM)
	VLCDJE_VLCTBL[11:2] ADDR	0 (VLC table at beginning of HUFMEM)
Start encode with automatic ring buffer management.	VLCDJ_CTRL[1] MODE	0 (encode mode)
	VLCDJ_CTRL[0] EN	1 (start VLCDJ operation)

For each group of eight MCUs (the VLCDJ does not care if these MCUs cross multiple MCU rows), software sets the VLCDJ_CTRL[0] EN bit to 1 (restart VLCDJ operation).

Alternately, the hardware sequencer can start the VLCDJ. Usually, DMA is also configured to bring in YUV4:2:0 image data as input to DCT, and DMA, DCT, and VLCDJ are all put under control of the hardware sequencer.

Bitstream data is managed automatically between the VLCDJ and DMA throughout JPEG encoding of MCUs.

NOTE: Many registers change during the encoding of a frame, but software is not required to access these registers, because the VLCDJ manages the status information between tasks.

The last hardware task may require a smaller number of MCUs (the VLCDJE_CFG[13:8] NMCUS bit field) to adjust for the number of MCUs in the last group.

After the last VLCDJ task for the image, software must disable the automatic bitstream buffer management and prepare for the next image by setting the following values (these can be issued as a single write):

- VLCDJ_CTRL[6] RBEN = 0 (disable automatic DMA interaction)
- VLCDJ_CTRL[7] CLRRB = 1

Finally, software must pad the last data byte with bit 1s, then place an end-of-image marker after the last data byte. The VLCDJE_BSPTR[11:0] BYTEPTR and VLCDJE_BSPTR[19:16] BITPTR bit fields indicate the locations of the last data byte and bit, respectively. Software must then set up DMA to transfer out the remaining data in bitstream memory.

The number of MCUs processed by hardware per task must be set according to image buffer allocation. For example, with 8KB available for DCT coefficient memory, and YUV4:2:0 format, it is possible to process 8K/(16 × 16× 1.5 × 2) = 10 MCUs. Because the bitstream DMA is automatic, bitstream data does not overflow bitstream memory for this many MCUs in densely coded JPEG.

8.4.6.4.4 JPEG Decoding

For JPEG decoding of an image, software first parses the JPEG header, which includes image dimension, YUV sampling, Huffman tables, quantizer matrices, and start-of-scan marker and scan header, before the MCU data. Software then sets up DMA to load bitstream data into the first half of bitstream memory.

The Huffman tables must be processed to generate hardware control tables and decode tables for a particular JPEG file, unless the Huffman tables match previously processed tables for which the hardware control and decode tables are known. The hardware control and decode tables must be transferred to HUFMEM.

If the JPEG file is YUV4:2:0, and image buffer memory is sufficient to process eight MCUs per hardware task, software must set up the decode task, once per image, with the procedure listed in Table 8-1376.

Table 8-1376. JPEG Decoding Procedure

Step	Register/Bit Field	Value
Configure the decode configuration register.	VLCDJD_CFG[1:0] FMT	0 (YUV4:2:0 mode)

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Table 8-1376. JPEG Decoding Procedure (continued)

Step	Register/Bit Field	Value
	VLCDJD_CFG[13:8] NMCUS	7 (eight MCUs)
	VLCDJD_CFG[2] RSTEN	0 (no restart marker)
Configure the DC predictor.	VLCDJD_DCPREDY[11:0] PREDY	0 (reset DC predictor for Y)
	VLCDJD_DCPREDUV[11:0] PREDU	0 (reset DC predictors for U)
	VLCDJD_DCPREDUV[27:16] PREDV	0 (reset DC predictors for V)
Configure the input and output memories.	VLCDJD_BSPTR[11:0] BYTEPTR	0 (beginning of bitstream memory)
	VLCDJD_BSPTR[19:16] BITPTR	8 (initially empty byte, thus 8 free bits)
	VLCDJD_CBUF[11:10] START	0 (bitstream starts from beginning of first quadrant of bitstream memory)
	VLCDJD_CBUF[27:26] END	3 (bitstream ends at end of fourth quadrant of bitstream memory)
	VLCDJD_DCTQM[13:4] DCT	0 (DCT coefficients at the beginning of the image buffer)
Configure Huffman and quantizer memory pointers.	VLCDJD_DCTQM[24:23] QMR	0 (quantizer matrix at beginning of QMEM)
	VLCDJD_CTRLTBL[11:2] ADDR	0 (typically, control table is placed at the beginning of HUFMEM)
	VLCDJD_DCDTBL01[11:2] TBL0	30 (typically, the first decode table follows the control table, 60 shorts = 120 bytes = 30 words)
	VLCDJD_DCDTBL01[27:18] TBL1	? (where the second decode table starts)
	VLCDJD_DCDTBL23[11:2] TBL2	? (where the third decode table starts)
	VLCDJD_DCDTBL23[27:18] TBL3	? (where the fourth decode table starts)
Start decode with automatic ring buffer management.	VLCDJ_CTRL[1] MODE	1 (decode mode)
	VLCDJ_CTRL[0] EN	1 (start VLCDJ operation)

For each group of eight MCUs (the VLCDJ does not care if these MCUs cross multiple MCU rows), software sets the VLCDJ_CTRL[0] EN bit to 1 (restart VLCDJ operation).

Alternately, the hardware sequencer can start the VLCDJ, as well as control buffer switches and coordinate among the VLCDJ, DCT, and DMA.

Bitstream data is managed automatically between the VLCDJ and DMA throughout JPEG encoding of MCUs.

NOTE: Many registers change during the decoding of a frame, but software is not required to access these registers, because the VLCDJ manages the status information between tasks.

The last hardware task may require a smaller number of MCUs (the VLCDJD_CFG[13:8] NMCUS bit field) to adjust for the number of MCUs in the last group.

After the last VLCDJ task for the image, software must disable the automatic bitstream buffer management and prepare for the next image by setting the following values (these can be issued as a single write):

- VLCDJ_CTRL[6] RBEN = 0 (disable automatic DMA interaction)
- VLCDJ_CTRL[7] CLRRB = 1

Before the VLCDJ processes the next image decode, new bitstream data must be brought in, thereby overwriting the old data, and bit/byte pointers must be reset to the beginning of bitstream memory. As a result, any remaining bitstream data in bitstream memory afterward is harmless.

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The number of MCUs processed by hardware per task must be set according to image buffer allocation. For example, with 16KB available for DCT coefficient memory, and YUV4:2:0 format, it is possible to process 16K/(16 × 16 × 1.5 × 2) = 21 MCUs. Because the bitstream DMA is automatic, there is no bitstream data underrun for this many MCUs.

8.4.6.4.5 Concurrent JPEG Encoding and Decoding

For concurrent decoding and encoding, the two operations are configured separately but similarly.

Half of bitstream memory is used for encoding (for example, the first half), and the rest is used for decoding. Automatic bitstream DMA does not work in this case, so the number of MCUs must accommodate the worst-case bitstream size per MCU.

Theoretically, the worst case is 16 bits of Huffman code plus 12 additional bits per coefficient, or 28 bits per coefficient. With natural images, there are typically about 8 bits per pixel when quantizers are minimal (that is, all 1s). With 16 bits per coefficient, or 768 bytes per MCU in YUV4:2:0 (this is 24 bits per pixel and three times the typical worst case), half of bitstream memory is 2KB, which can safely hold two MCUs.

In this case, half of QMEM is used for encoding and half is used for decoding. Encode and decode Huffman tables are placed so that they coexist in HUFFMEM.

The Huffman tables for encoding, decoding, and quantizer matrices must be placed accordingly in HUFMEM and QMEM. Bitstream data is filled at the second half of bitstream memory for decoding.

Register fields are configured as listed in Table 8-1377.

Table 8-1377. Concurrent JPEG Encoding and Decoding

Step	Register/Bit Field	Value
Configure the encode register.	VLCDJE_CFG[1:0] FMT	0 (YUV4:2:0 mode)
	VLCDJE_CFG[13:8] NMCUS	1 (two MCUs)
	VLCDJD_CFG[2] RSTEN	0 (no restart marker)
	VLCDJE_DCPREDY[11:0] PREDY	0 (reset DC predictor for Y)
	VLCDJE_DCPREDUV[11:0] PREDU	0 (reset DC predictors for U)
	VLCDJE_DCPREDUV[27:16] PREDV	0 (reset DC predictors for V)
	VLCDJE_BSPTR[19:16] BITPTR	8 (initially empty byte, thus 8 free bits)
	VLCDJE_DCTQM[13:4] DCT	0 (DCT coefficients at beginning of image buffer)
Configure the decode register.	VLCDJD_CFG[1:0] FMT	0 (YUV4:2:0 mode)
	VLCDJD_CFG[13:8] NMCUS	1 (two MCUs)
	VLCDJD_CFG[2] RSTEN	0 (no restart marker)
	VLCDJD_DCPREDY[11:0] PREDY	0 (reset DC predictor for Y)
	VLCDJD_DCPREDUV[11:0] PREDU	0 (reset DC predictors for U)
	VLCDJD_DCPREDUV[27:16] PREDV	0 (reset DC predictors for V)
	VLCDJD_BSPTR[19:16] BITPTR	8 (initially empty byte, thus 8 free bits)
	VLCDJD_DCTQM[13:4] DCT	0 (DCT coefficients at the beginning of the image buffer)
Configure the byte pointer to bitstream memory.	VLCDJE_BSPTR[11:0] BYTEPTR	0 (beginning of bitstream memory)
	VLCDJD_BSPTR[11:0] BYTEPTR	0x800 (beginning of bitstream memory second half)
Configure the bitstream memory partition.	VLCDJE_CBUF[11:10] START	0 (bitstream starts at beginning of first quadrant of bitstream memory)
	VLCDJE_CBUF[27:26] END	1 (bitstream ends at end of second quadrant of bitstream memory)
	VLCDJD_CBUF[11:10] START	2 (bitstream starts at beginning of third quadrant of bitstream memory)
	VLCDJD_CBUF[27:26] END	3 (bitstream ends at end of fourth quadrant of bitstream memory)

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Table 8-1377. Concurrent JPEG Encoding and Decoding (continued)

Step	Register/Bit Field	Value
Configure the quantizer matrix pointer.	VLCDJE_DCTQM[24:23] QMR	0 (quantizer matrix at beginning of QMEM)
	VLCDJD_DCTQM[24:23] QMR	2 (quantizer matrix at second half of QMEM)
Configure Huffman tables.	VLCDJE_VLCTBL[11:2] ADDR	0 (VLC table at beginning of HUFMEM)
	VLCDJD_CTRLTBL[11:2] ADDR	376 (after VLC table, 2 × (24 + 352) shorts = 376 words)
	VLCDJD_DCDTBL01[11:2] TBL0	406 (after control table of 30 words)
	VLCDJD_DCDTBL01[27:18] TBL1	? (where the second decode table starts)
	VLCDJD_DCDTBL23[11:2] TBL2	? (where the third decode table starts)
	VLCDJD_DCDTBL23[27:18] TBL3	? (where the fourth decode table starts)

Software sets the following values to start encoding:

- VLCDJ_CTRL[1] MODE = 0 (encode mode)
- VLCDJ_CTRL[0] EN = 1 (start VLCDJ operation)

When the VLCDJ completion interrupt is detected by software, encoding is complete and software must service the encoded bitstream data in the first half of bitstream memory, letting hardware access the second half of the bitstream for decoding. Software sets up bitstream writes to transfer the encoded bitstream from bitstream memory[0] to bitstream memory[128 × (VLCDJE_BSPTR[11:0] BYTEPTR/128)] (rounding down to 128-byte alignment improves SDRAM efficiency). Software must identify the bitstream data already transferred out, for the next round of servicing encoded bitstream data. Software must also service to-encode input data to the DCT.

After kicking off encode DMAs, without waiting for DMA completion, software must set the following values to start VLCDJ decoding in parallel with the DMA:

- VLCDJ_CTRL[1] MODE = 1 (decode mode)
- VLCDJ_CTRL[0] EN = 1 (start VLCDJ operation)

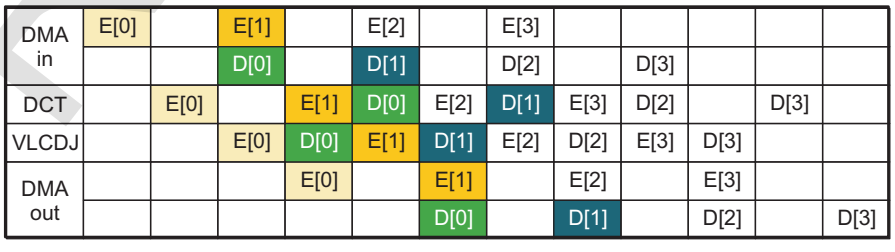
When the VLCDJ completion interrupt is detected by software, decoding is complete and software must service the decoded bitstream data in the second half of bitstream memory, letting hardware access the first half of the bitstream for encoding. Software sets up bitstream writes to transfer the bitstream to be decoded from bitstream memory[0] to bitstream memory[128 × (VLCDJD_BSPTR[11:0] BYTEPTR/128)] (rounding down to 128-byte alignment improves SDRAM efficiency). Software must identify the bitstream data already transferred in, for the next round of servicing bitstream data to be decoded. Software must also service decoded image data in the output image buffer of the DCT.

After kicking off decode DMAs, without waiting for DMA completion, software must start VLCDJ encoding in parallel with the DMA.

Software must continue to alternate between encoding and decoding until the image completes.

Figure 8-282 shows the concurrence schedule for JPEG encoding and decoding.

Figure 8-282. Concurrence Schedule for JPEG Encoding and Decoding



vlcdj-007

Management of bitstream I/O and image I/O is heavy in intervals of only two MCUs. It is better to run only encoding for many MCUs, switch context, and then run decoding for many MCUs.

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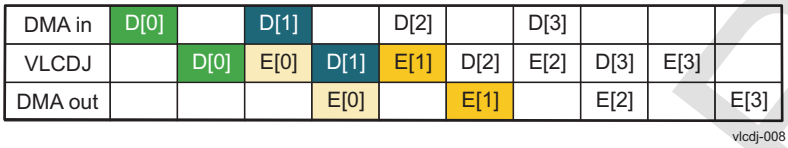
When running JPEG transcoding, decoding a picture and re-encoding it, to adjust quantizers and/or remove/insert restart markers, it can be more efficient to run encode and decode concurrently in VLCDJ, skipping DCT and image I/O DMA altogether. In this case, software handles only bitstream data I/O, which is more manageable.

Figure 8-283 shows the concurrence schedule for JPEG transcoding.

Figure 8-283. Concurrence Schedule for JPEG Transcoding



8.4.6.4.5.1 DMA and Buffer Manual Management

When the VLCDJ performs one encode and one decode concurrently, both contexts can coexist in the configuration registers, because encode and decode configurations are in separate registers. The bitstream memory must be partitioned half-and-half between encode and decode:

- VLCDJE_CBUF[11:10] START = 0 (0x0)
- VLCDJE_CBUF[27:26] END = 1 (0x7FF)
- VLCDJD_CBUF[11:10] START = 2 (0x800)
- VLCDJD_CBUF[27:26] END = 3 (0xFFF)

The byte pointers and the bitstream data DMA must be set up accordingly.

When the VLCDJ is encoding, the decode half of the bitstream memory can be refilled by DMA. When the VLCDJ is decoding, the encode half of the bitstream memory can be transferred out by DMA. Hardware does not support automatic triggering of DMA; software must submit DMA based on the byte pointer value of each context. For greater SDRAM efficiency, the DMA block must be aligned correctly. For example, the pseudocode that sets up the DMA for an encode task may appear as:

```
new_dma_ptr = VLCDJ_BSPTR.BYTEPTR  ~0x3F; // align to 64-byte
if (new_dma_ptr  saved_dma_ptr)
{
 setup_dma(saved_dma_ptr, new_dma_ptr - saved_dma_ptr);
 // start DMA at saved_dma_ptr, length = new_dma_ptr - saved_dma_ptr
}
else // wraps around, need to DMA 2 blocks
{
 setup_dma(saved_dma_ptr, 0x800 - saved_dma_ptr);
 setup_dma(saved_dma_ptr, new_dma_ptr);
}
saved_dma_ptr = new_dma_ptr;
```

This DMA setup can be carried out concurrently with VLCDJ operation; thus, this code is executed with each encode or decode task. When the VLCDJ is encoding, software can access the decode bit/byte points to set up DMA for decoding, and vice versa.

Because hardware stalling does not work in this case, the number of MCUs must be configured so that in the worst case there is no bitstream data overrun or underrun.

The bitstream buffer can be allocated at a quarter of bitstream memory granularity, or 1KB. This allows at most four separate buffers to coexist in bitstream memory.

If multiple encode and/or decode threads are performed concurrently, software must save and restore the appropriate configuration registers. The register map has common registers in one group, encode registers in another group, and decode registers in a third group. Bitstream memory partitioning and corresponding DMA submission are left to software.

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8.4.6.4.6 Example of YUV4:4:4 Encoding

The following pseudocode shows the general sequence involved in YUV4:4:4 encoding. Decoding can be similarly derived.

```
encode_yuv444()
{
 VLCDJ_CTRL[1] MODE = 0; /* encode */
 VLCDJE_CFG[1:0] FMT = 2; /* sequential block mode */
 VLCDJE_CFG[13:8] NMCUS = 0; /* 1 block at a time */
 pred_y = 0;
 pred_u = 0;
 pred_v = 0;
 for (i=0; inum_mcus; i++)
 {
 VLCDJE_DCPREDY = pred_y; /* restore Y context */
 VLCDJE_DCT = DCT_Y;
 VLCDJE_QMR = QMR_Y;
 VLCDJE_VLCTBL = VLC_Y;
 VLCDJ_CTRL[0] EN = 1; /* kick off VLCDJ for Y */
 pred_y = VLCDJE_DCPREDY; /* save Y context */
 VLCDJE_DCPREDY = pred_u; /* restore U context */
 VLCDJE_DCT = DCT_U;
 VLCDJE_QMR = QMR_UV;
 VLCDJE_VLCTBL = VLC_UV;
 VLCDJ_CTRL[0] EN = 1; /* kick off VLCDJ for U */
 pred_u = VLCDJE_DCPREDY; /* save U context */
 VLCDJE_DCPREDY = pred_v; /* restore V context */
 VLCDJE_DCT = DCT_V;
 VLCDJ_CTRL[0] EN = 1; /* kick off VLCDJ for V */
 pred_v = VLCDJE_DCPREDY; /* save V context */
 }
}
```

8.4.6.4.7 Example of Huffman Encode and Decode Tables

8.4.6.4.7.1 Huffman Encode Table

Sample JPEG Luma DC encode table:

```
unsigned short jpeg_dc_y[24] =
{
 0x0000,0x0002,0x0002,0x0003,0x0003,0x0003,0x0004,0x0003,
 0x0005,0x0003,0x0006,0x0003,0x000e,0x0004,0x001e,0x0005,
 0x003e,0x0006,0x007e,0x0007,0x00fe,0x0008,0x01fe,0x0009
};
```

Table 8-1378 corresponds to Table 17 in the JPEG standard *ISO/IEC JTC1/SC29/WG10 Standard 10918-1 (JPEG), Information Technology – Digital Compression and Coding of Continuous-Tone Still Images – Requirements and Guidelines.*

Table 8-1378. Sample Luma DC Huffman Code Table

Category	Code Length	Code Word
0	2	00
1	3	010
2	3	011
3	3	100
4	3	101
5	3	110
6	4	1110
7	5	11110
8	6	111110

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Table 8-1378. Sample Luma DC Huffman Code Table (continued)

Category	Code Length	Code Word
9	7	1111110
10	8	11111110
11	9	111111110

To code a DC coefficient value of –5:

Use abs(–5) = 5 to select a size of 3. Look up the encode table to find:

- jpeg_dc_y[2 × 3] = 4 (code)
- jpeg_dc_y[2 × 3 + 1] = 3 (length)

Thus, the VLCDJ adds 100 to the bitstream as the Huffman code of the size.

The additional bits for negative coefficients are ones complement of the absolute value, so for –5, this is 010, or 2. After the Huffman code of the size, the VLCDJ adds 010 to the bitstream.

The AC coefficient table is the same, except that the VLCDJ uses 16 × size + run to index the encode table.

8.4.6.4.7.2 Huffman Decode Tables

Sample JPEG Luma DC control and decode tables:

```
unsigned short jpeg_dc_y_ctl_tbl[13]=
{
 0x0000,0x0000,0x0000,0x0000,0x1800,0x2001,0x2802,0x3003,
 0x3804,0x4005,0x4806,0x4806,0x4806
};
unsigned short jpeg_dc_y_dcd_tbl[14]=
{
 0x0000,0x480b,0x400a,0x3809,0x3008,0x2807,0x2006,0x1805,
 0x1804,0x1803,0x1802,0x1801,0x1000,0x1000
};
```

These tables contain the same information as Table 8-1378, which complies with the JPEG standard.

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8.4.6.5 ISS SIMCOP VLCDJ Register Manual

8.4.6.5.1 ISS SIMCOP VLCDJ Instance Summary

Table 8-1379 summarizes the VLDCJ instance.

Table 8-1379. ISS SIMCOP VLCDJ Instance Summary

Module Name	Base Address L3 Interconnect	Base Address Cortex-M3 Private Access	Size
VLCDJ	0x5202 0600	0x5506 0600	128 bytes

NOTE: Private Access is an access that does not use the L3/L4 interconnects.

8.4.6.5.2 VLCDJ Registers

8.4.6.5.2.1 VLCDJ Register Summary

Table 8-1380 summarizes VLDCJ register mapping.

Table 8-1380. VLCDJ Register Mapping Summary

Register	Type	Register Width (Bits)	Address Offset	Physical Address L3 Interconnect	Physical Address Cortex-M3 Private Access
VLCDJ_REVISION	RW	32	0x0000 0000	0x5202 0600	0x5506 0600
VLCDJ_CTRL	RW	32	0x0000 0004	0x5202 0604	0x5506 0604
VLCDJE_CFG	RW	32	0x0000 0008	0x5202 0608	0x5506 0608
VLCDJE_DCPREDY	RW	32	0x0000 000C	0x5202 060C	0x5506 060C
VLCDJE_DCPREDUV	RW	32	0x0000 0010	0x5202 0610	0x5506 0610
VLCDJE_BSPTR	RW	32	0x0000 0014	0x5202 0614	0x5506 0614
VLCDJE_CBUF	RW	32	0x0000 0018	0x5202 0618	0x5506 0618
VLCDJE_RSTCFG	RW	32	0x0000 001C	0x5202 061C	0x5506 061C
VLCDJE_DCTQM	RW	32	0x0000 0020	0x5202 0620	0x5506 0620
VLCDJE_VLCTBL	RW	32	0x0000 0024	0x5202 0624	0x5506 0624
VLCDJE_RSTPTR	RW	32	0x0000 0028	0x5202 0628	0x5506 0628
VLCDJE_RSTOFST	RW	32	0x0000 002C	0x5202 062C	0x5506 062C
VLCDJD_CFG	RW	32	0x0000 0040	0x5202 0640	0x5506 0640
VLCDJD_DCPREDY	RW	32	0x0000 0044	0x5202 0644	0x5506 0644
VLCDJD_DCPREDUV	RW	32	0x0000 0048	0x5202 0648	0x5506 0648
VLCDJD_BSPTR	RW	32	0x0000 004C	0x5202 064C	0x5506 064C
VLCDJD_CBUF	RW	32	0x0000 0050	0x5202 0650	0x5506 0650
VLCDJD_DCTQM	RW	32	0x0000 0054	0x5202 0654	0x5506 0654
VLCDJD_CTRLTBL	RW	32	0x0000 0058	0x5202 0658	0x5506 0658
VLCDJD_DCDTBL01	RW	32	0x0000 005C	0x5202 065C	0x5506 065C
VLCDJD_DCDTBL23	RW	32	0x0000 0060	0x5202 0660	0x5506 0660
VLCDJD_DCTERR	R	32	0x0000 0064	0x5202 0664	0x5506 0664

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8.4.6.5.2.2 VLCDJ Register Descriptions

through describe the individual registers.

Table 8-1381. VLCDJ_REVISION

Address Offset	0x0000 0000		
Physical Address	0x5202 0600 0x5506 0600	**Instance**	VLCDJ_L3 VLCDJ_CORTEX-M3
Description	IP revision		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP Revision	R	TI internal data

Table 8-1382. Register Call Summary for Register VLCDJ_REVISION

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- ISS SIMCOP VLCDJ Register Manual: [0]

Table 8-1383. VLCDJ_CTRL

Address Offset	0x0000 0004		
Physical Address	0x5202 0604 0x5506 0604	**Instance**	VLCDJ_L3 VLCDJ_CORTEX-M3
Description	Controls common to encoding and decoding		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															BUSY	RESERVED								CLRRB	RBEN	INTEN_ERR	INTEN_DONE	AUTOGATING	TRIG_SRC	MODE	EN

Bits	Field Name	Description	Type	Reset
31:17	RESERVED	Read returns 0.	R	0x00
16	BUSY	Idle/busy status 0: Idle 1: Busy	R	0
15:8	RESERVED	Read returns 0.	R	0x00
7	CLRRB	Write only; read returns 0.	W	0
6	RBEN	Enable RB signaling.	RW	0
5	INTEN_ERR	Interrupt enable for decode error 0: No interrupt generated on decode error 1: Interrupt generated on decode error	RW	0
4	INTEN_DONE	Interrupt enable for task completion. DONE_VLCD is not gated by this and is always asserted at task completion. 0: No interrupt generated on task completion 1: Interrupt generated on task completion	RW	0

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Bits	Field Name	Description	Type	Reset
3	AUTOGATING	Internal clock gating on OCP clock and functional clock 0: Clocks are free-running. 1: Clocks are gated off in sub-blocks that are not required for operation.	RW	1
2	TRIG_SRC	Which mechanism starts VLCDJ operation 0: MMR write to VLCDJ_CTRL.EN 1: Hardware start signal	RW	0
1	MODE	0: Encode 1: Decode	RW	0
0	EN	Module enable by software (write-only, read returns 0). When TRIG_SRC = 0 and BUSY = 0, set this field to 1 to start VLCDJ. When TRIG_SRC = 1, writes to this field are ignored. Setting TRIG_SRC = 0 and EN = 1 on the same register write is recognized.	W	0

Table 8-1384. Register Call Summary for Register VLCDJ_CTRL

ISS Still Image Coprocessor

- ISS SIMCOP VLCDJ Functional Description: [0] [1] [2]
- ISS SIMCOP VLCDJ Basic Programming Model: [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [17] [18] [21] [22] [23] [25] [26] [29] [30] [32] [33] [34] [35]
- ISS SIMCOP VLCDJ Register Manual: [37] [38]

Table 8-1385. VLCDJE_CFG

Address Offset	0x0000 0008		
Physical Address	0x5202 0608 0x5506 0608	**Instance**	VLCDJ_L3 VLCDJ_CORTEX-M3
Description	Encode configuration		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																NMCUS								RESERVED				RLOCEN	RSTEN	FMT	

Bits	Field Name	Description	Type	Reset
31:14	RESERVED	Read returns 0.	R	0x00000
13:8	NMCUS	Number of MCUs (FMT = 0, 1) or blocks (FMT = 2) to encode 0: 1 MCU 1: 2 MCUs, etc.	RW	0x00
7:4	RESERVED	Read returns 0.	R	0x0
3	RLOCEN	Restart marker location recording enable 0: Restart marker location recording disabled 1: Restart marker location recording enabled	RW	0
2	RSTEN	Restart marker insertion enable 0: Restart marker insertion disabled 1: Restart marker insertion enabled	RW	0
1:0	FMT	0: YUV4:2:0 1: YUV4:2:2 2 : Sequential blocks	RW	0x0

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Table 8-1386. Register Call Summary for Register VLCDJE_CFG

ISS Still Image Coprocessor

- ISS SIMCOP VLCDJ Functional Description:
- ISS SIMCOP VLCDJ Basic Programming Model: [1] [2] [3] [4] [5] [6]
- ISS SIMCOP VLCDJ Register Manual: [9]

Table 8-1387. VLCDJE_DCPREDY

Address Offset	0x0000 000C		
Physical Address	0x5202 060C 0x5506 060C	**Instance**	VLCDJ_L3 VLCDJ_CORTEX-M3
Description	Encode DC predictor for Y		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				PREDY											

Bits	Field Name	Description	Type	Reset
31:12	RESERVED	Read returns 0.	R	0x00000
11:0	PREDY	DC predictor for Y	RW	0x000

Table 8-1388. Register Call Summary for Register VLCDJE_DCPREDY

ISS Still Image Coprocessor

- ISS SIMCOP VLCDJ Basic Programming Model: [0] [1]
- ISS SIMCOP VLCDJ Register Manual: [2]

Table 8-1389. VLCDJE_DCPREDUV

Address Offset	0x0000 0010		
Physical Address	0x5202 0610 0x5506 0610	**Instance**	VLCDJ_L3 VLCDJ_CORTEX-M3
Description	Encode DC predictor for U and V		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				PREDV												RESERVED				PREDU											

Bits	Field Name	Description	Type	Reset
31:28	RESERVED	Read returns 0.	R	0x0
27:16	PREDV	DC predictor for V	RW	0x000
15:12	RESERVED	Read returns 0.	R	0x0
11:0	PREDU	DC predictor for U	RW	0x000

Table 8-1390. Register Call Summary for Register VLCDJE_DCPREDUV

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- ISS SIMCOP VLCDJ Basic Programming Model: [0] [1] [2] [3]
- ISS SIMCOP VLCDJ Register Manual: [4]

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Table 8-1391. VLCDJE_BSPTR

Address Offset	0x0000 0014		
Physical Address	0x5202 0614 0x5506 0614	**Instance**	VLCDJ_L3 VLCDJ_CORTEX-M3
Description	Encode bitstream pointer		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												BITPTR				RESERVED				BYTEPTR											

Bits	Field Name	Description	Type	Reset
31:20	RESERVED	Read returns 0.	R	0x000
19:16	BITPTR	Bit pointer, 1..8, indicates number of available bits	RW	0x8
15:12	RESERVED	Read returns 0.	R	0x0
11:0	BYTEPTR	Byte pointer (to BSMEM)	RW	0x000

Table 8-1392. Register Call Summary for Register VLCDJE_BSPTR

ISS Still Image Coprocessor

- ISS SIMCOP VLCDJ Functional Description: [0] [1]
- ISS SIMCOP VLCDJ Basic Programming Model: [2] [3] [4] [5] [6] [7] [8]
- ISS SIMCOP VLCDJ Register Manual: [9]

Table 8-1393. VLCDJE_CBUF

Address Offset	0x0000 0018		
Physical Address	0x5202 0618 0x5506 0618	**Instance**	VLCDJ_L3 VLCDJ_CORTEX-M3
Description	Encode bitstream circular buffer		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				END		RESERVED										RESERVED				START		RESERVED									

Bits	Field Name	Description	Type	Reset
31:28	RESERVED	Read returns 0.	R	0x0
27:26	END	Ending quarter (1KB each unit) of bitstream buffer. Software can write a byte address into the upper 16 bits of the register.	RW	0x3
25:16	RESERVED	Read returns 0x3FF.	R; returns 1s	0x3FF
15:12	RESERVED	Read returns 0.	R	0x0
11:10	START	Starting quarter (1KB each unit) of bitstream buffer. Software can write a byte address to the lower 16 bits of the register.	RW	0x0
9:0	RESERVED	Read returns 0.	R	0x000

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Table 8-1394. Register Call Summary for Register VLCDJE_CBUF

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- ISS SIMCOP VLCDJ Functional Description: [0] [1] [2] [3]
- ISS SIMCOP VLCDJ Basic Programming Model: [4] [5] [6] [7] [8] [9]
- ISS SIMCOP VLCDJ Register Manual: [10]

Table 8-1395. VLCDJE_RSTCFG

Address Offset	0x0000 001C		
Physical Address	0x5202 061C 0x5506 061C	**Instance**	VLCDJ_L3 VLCDJ_CORTEX-M3
Description	Encode restart marker configuration		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				INC				RESERVED				INIT				RESERVED				PHASE								RESERVED				INTRVL			

Bits	Field Name	Description	Type	Reset
31	RESERVED	Read returns 0.	R	0
30:28	INC	Restart count increment value	RW	0x1
27	RESERVED	Read returns 0.	R	0
26:24	INIT	Restart marker initial count	RW	0x0
23:22	RESERVED	Read returns 0.	R	0x0
21:12	PHASE	MCU count within the interval	RW	0x000
11:10	RESERVED	Read returns 0.	R	0x0
9:0	INTRVL	Restart interval (in MCUs)	RW	0x000

Table 8-1396. Register Call Summary for Register VLCDJE_RSTCFG

ISS Still Image Coprocessor

- ISS SIMCOP VLCDJ Functional Description:
- ISS SIMCOP VLCDJ Basic Programming Model:
- ISS SIMCOP VLCDJ Register Manual: [13]

Table 8-1397. VLCDJE_DCTQM

Address Offset	0x0000 0020		
Physical Address	0x5202 0620 0x5506 0620	**Instance**	VLCDJ_L3 VLCDJ_CORTEX-M3
Description	Encode DCT coefficient and quantizer matrix pointers		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								QMR								RESERVED								DCT								RESERVED			

Bits	Field Name	Description	Type	Reset
31:25	RESERVED	Read returns 0.	R	0x00
24:23	QMR	Quarter (128 bytes/unit) of quantization matrix reciprocal. Software can write a byte address to the upper 16 bits of the register.	RW	0x0

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Bits	Field Name	Description	Type	Reset
22:14	RESERVED	Read returns 0.	R	0x000
13:4	DCT	128-bit/word address of DCT coefficients. Software can write a byte address to the lower 16 bits of the register.	RW	0x000
3:0	RESERVED	Read returns 0.	R	0x0

Table 8-1398. Register Call Summary for Register VLCDJE_DCTQM

ISS Still Image Coprocessor

- ISS SIMCOP VLCDJ Basic Programming Model: [0] [1] [2] [3]
- ISS SIMCOP VLCDJ Register Manual: [4]

Table 8-1399. VLCDJE_VLCTBL

Address Offset	0x0000 0024		
Physical Address	0x5202 0624 0x5506 0624	**Instance**	VLCDJ_L3 VLCDJ_CORTEX-M3
Description	Encode Huffman table pointer		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																ADDR														RESERVED	

Bits	Field Name	Description	Type	Reset
31:12	RESERVED	Read returns 0.	R	0x00000
11:2	ADDR	Encode Huffman table pointer, 32-bit word address. Software can write a byte address into the entire register.	RW	0x000
1:0	RESERVED	Read returns 0.	R	0x0

Table 8-1400. Register Call Summary for Register VLCDJE_VLCTBL

ISS Still Image Coprocessor

- ISS SIMCOP VLCDJ Functional Description: [0] [1] [2] [3]
- ISS SIMCOP VLCDJ Basic Programming Model: [4] [5]
- ISS SIMCOP VLCDJ Register Manual: [6]

Table 8-1401. VLCDJE_RSTPTR

Address Offset	0x0000 0028		
Physical Address	0x5202 0628 0x5506 0628	**Instance**	VLCDJ_L3 VLCDJ_CORTEX-M3
Description	Encode restart marker locations		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																ADDR														RESERVED	

Bits	Field Name	Description	Type	Reset
31:14	RESERVED	Read returns 0.	R	0x00000
13:4	ADDR	Pointer to restart marker locations in image buffer, 128-bit/word address Software can write a byte address into the entire register.	RW	0x000

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Bits	Field Name	Description	Type	Reset
3:0	RESERVED	Read returns 0.	R	0x0

Table 8-1402. Register Call Summary for Register VLCDJE_RSTPTR

ISS Still Image Coprocessor

- ISS SIMCOP VLCDJ Functional Description:
- ISS SIMCOP VLCDJ Register Manual: [2]

Table 8-1403. VLCDJE_RSTOFST

Address Offset	0x0000 002C		
Physical Address	0x5202 062C 0x5506 062C	**Instance**	VLCDJ_L3 VLCDJ_CORTEX-M3
Description	SDRAM address to add to encode restart marker locations		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OFFSET																															

Bits	Field Name	Description	Type	Reset
31:0	OFFSET	SDRAM address of bitstream buffer, to be added to the restart marker locations	RW	0x0000 0000

Table 8-1404. Register Call Summary for Register VLCDJE_RSTOFST

ISS Still Image Coprocessor

- ISS SIMCOP VLCDJ Functional Description:
- ISS SIMCOP VLCDJ Register Manual: [1]

Table 8-1405. VLCDJD_CFG

Address Offset	0x0000 0040		
Physical Address	0x5202 0640 0x5506 0640	**Instance**	VLCDJ_L3 VLCDJ_CORTEX-M3
Description	Decode configuration		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																NMCUS								RESERVED					RSTEN	FMT	

Bits	Field Name	Description	Type	Reset
31:14	RESERVED	Read returns 0.	R	0x00000
13:8	NMCUS	Number of MCUs (FMT = 0, 1) or blocks (FMT = 2) to decode 0: 1 MCU 1: 2 MCUs, etc.	RW	0x00
7:3	RESERVED	Read returns 0.	R	0x00
2	RSTEN	Restart marker detection/processing enable 0: Restart marker detection/processing disabled 1: Restart marker detection/processing enabled	RW	1
1:0	FMT	0: YUV4:2:0 1: YUV4:2:2 2: Sequential blocks	RW	0x0

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Table 8-1406. Register Call Summary for Register VLCDJD_CFG

ISS Still Image Coprocessor

- ISS SIMCOP VLCDJ Basic Programming Model: [0] [1] [2] [3] [4] [5] [6] [7]
- ISS SIMCOP VLCDJ Register Manual: [8]

Table 8-1407. VLCDJD_DCPREDY

Address Offset	0x0000 0044		
Physical Address	0x5202 0644 0x5506 0644	**Instance**	VLCDJ_L3 VLCDJ_CORTEX-M3
Description	Decode DC predictor for Y		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				PREDY											

Bits	Field Name	Description	Type	Reset
31:12	RESERVED	Read returns 0.	R	0x00000
11:0	PREDY	DC predictor for Y	RW	0x000

Table 8-1408. Register Call Summary for Register VLCDJD_DCPREDY

ISS Still Image Coprocessor

- ISS SIMCOP VLCDJ Basic Programming Model: [0] [1]
- ISS SIMCOP VLCDJ Register Manual: [2]

Table 8-1409. VLCDJD_DCPREDUV

Address Offset	0x0000 0048		
Physical Address	0x5202 0648 0x5506 0648	**Instance**	VLCDJ_L3 VLCDJ_CORTEX-M3
Description	Decode DC predictor for U and V		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				PREDV												RESERVED				PREDU											

Bits	Field Name	Description	Type	Reset
31:28	RESERVED	Read returns 0.	R	0x0
27:16	PREDV	DC predictor for V	RW	0x000
15:12	RESERVED	Read returns 0.	R	0x0
11:0	PREDU	DC predictor for U	RW	0x000

Table 8-1410. Register Call Summary for Register VLCDJD_DCPREDUV

ISS Still Image Coprocessor

- ISS SIMCOP VLCDJ Basic Programming Model: [0] [1] [2] [3]
- ISS SIMCOP VLCDJ Register Manual: [4]

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Table 8-1411. VLCDJD_BSPTR

Address Offset	0x0000 004C		
Physical Address	0x5202 064C 0x5506 064C	**Instance**	VLCDJ_L3 VLCDJ_CORTEX-M3
Description	Decode bitstream pointer		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												BITPTR				RESERVED				BYTEPTR											

Bits	Field Name	Description	Type	Reset
31:20	RESERVED	Read returns 0.	R	0x000
19:16	BITPTR	Bit pointer, 1..8, indicates number of available bits	RW	0x8
15:12	RESERVED	Read returns 0.	R	0x0
11:0	BYTEPTR	Byte pointer (to BSMEM)	RW	0x000

Table 8-1412. Register Call Summary for Register VLCDJD_BSPTR

ISS Still Image Coprocessor

- ISS SIMCOP VLCDJ Functional Description: [0] [1] [2] [3]
- ISS SIMCOP VLCDJ Basic Programming Model: [4] [5] [6] [7] [8]
- ISS SIMCOP VLCDJ Register Manual: [9]

Table 8-1413. VLCDJD_CBUF

Address Offset	0x0000 0050		
Physical Address	0x5202 0650 0x5506 0650	**Instance**	VLCDJ_L3 VLCDJ_CORTEX-M3
Description	Decode bitstream circular buffer		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				END		RESERVED										RESERVED				START		RESERVED									

Bits	Field Name	Description	Type	Reset
31:28	RESERVED	Read returns 0.	R	0x0
27:26	END	Ending quarter (1KB each unit) of bitstream buffer. Software can write a byte address into the upper 16 bits of the register.	RW	0x3
25:16	RESERVED	Read returns 0x3FF.	R; returns 1s	0x3FF
15:12	RESERVED	Read returns 0.	R	0x0
11:10	START	Starting quarter (1KB each unit) of bitstream buffer. Software can write a byte address to the lower 16 bits of the register.	RW	0x0
9:0	RESERVED	Read returns 0.	R	0x000

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Table 8-1414. Register Call Summary for Register VLCDJD_CBUF

ISS Still Image Coprocessor

- ISS SIMCOP VLCDJ Functional Description: [0] [1] [2] [3]
- ISS SIMCOP VLCDJ Basic Programming Model: [4] [5] [6] [7] [8] [9]
- ISS SIMCOP VLCDJ Register Manual: [10]

Table 8-1415. VLCDJD_DCTQM

Address Offset	0x0000 0054		
Physical Address	0x5202 0654 0x5506 0654	**Instance**	VLCDJ_L3 VLCDJ_CORTEX-M3
Description	Decode DCT coefficient and quantizer matrix pointers		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								QM								RESERVED								DCT								RESERVED							

Bits	Field Name	Description	Type	Reset
31:25	RESERVED	Read returns 0.	R	0x00
24:23	QM	Quarter (128 bytes/unit) of quantization matrix. Software can write a byte address to the upper 16 bits of the register.	RW	0x0
22:14	RESERVED	Read returns 0.	R	0x000
13:4	DCT	128-bit/word address of DCT coefficients. Software can write a byte address to the lower 16 bits of the register.	RW	0x000
3:0	RESERVED	Read returns 0.	R	0x0

Table 8-1416. Register Call Summary for Register VLCDJD_DCTQM

ISS Still Image Coprocessor

- ISS SIMCOP VLCDJ Basic Programming Model: [0] [1] [2] [3]
- ISS SIMCOP VLCDJ Register Manual: [4]

Table 8-1417. VLCDJD_CTRLTBL

Address Offset	0x0000 0058		
Physical Address	0x5202 0658 0x5506 0658	**Instance**	VLCDJ_L3 VLCDJ_CORTEX-M3
Description	Decode control table base		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								ADDR															RESERVED

Bits	Field Name	Description	Type	Reset
31:12	RESERVED	Read returns 0.	R	0x00000
11:2	ADDR	Starting address of decode control table, 32-bit word. Software can write a byte address into the entire register.	RW	0x000
1:0	RESERVED	Read returns 0.	R	0x0

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Table 8-1418. Register Call Summary for Register VLCDJD_CTRLTBL

ISS Still Image Coprocessor

- ISS SIMCOP VLCDJ Basic Programming Model: [0] [1]
- ISS SIMCOP VLCDJ Register Manual: [2]

Table 8-1419. VLCDJD_DCDTBL01

Address Offset	0x0000 005C		
Physical Address	0x5202 065C 0x5506 065C	**Instance**	VLCDJ_L3 VLCDJ_CORTEX-M3
Description	Decode Huffman tables 0 and 1		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								DCDTBL1								RESERVED								DCDTBL0							RESERVED

Bits	Field Name	Description	Type	Reset
31:28	RESERVED	Read returns 0.	R	0x0
27:18	DCDTBL1	Starting byte address of decode table 1, 32-bit word. Software can write a byte address into the lower 16 bits of the register. This is for Luma AC.	RW	0x000
17:12	RESERVED	Read returns 0.	R	0x00
11:2	DCDTBL0	Starting byte address of decode table 0, 32-bit word. Software can write a byte address into the lower 16 bits of the register. This is for Luma DC.	RW	0x000
1:0	RESERVED	Read returns 0.	R	0x0

Table 8-1420. Register Call Summary for Register VLCDJD_DCDTBL01

ISS Still Image Coprocessor

- ISS SIMCOP VLCDJ Functional Description:
- ISS SIMCOP VLCDJ Basic Programming Model: [2] [3] [4] [5]
- ISS SIMCOP VLCDJ Register Manual: [6]

Table 8-1421. VLCDJD_DCDTBL23

Address Offset	0x0000 0060		
Physical Address	0x5202 0660 0x5506 0660	**Instance**	VLCDJ_L3 VLCDJ_CORTEX-M3
Description	Decode Huffman tables 2 and 3		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								DCDTBL3								RESERVED								DCDTBL2							RESERVED

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Bits	Field Name	Description	Type	Reset
31:28	RESERVED	Read returns 0.	R	0x0
27:18	DCDTBL3	Starting byte address of decode table 3, 32-bit word. Software can write a byte address into the lower 16 bits of the register. This is for Chroma AC.	RW	0x000
17:12	RESERVED	Read returns 0.	R	0x00
11:2	DCDTBL2	Starting byte address of decode table 2, 32-bit word. Software can write a byte address into the lower 16 bits of the register. This is for Chroma DC.	RW	0x000
1:0	RESERVED	Read returns 0.	R	0x0

Table 8-1422. Register Call Summary for Register VLCDJD_DCDTBL23

ISS Still Image Coprocessor

- ISS SIMCOP VLCDJ Functional Description:
- ISS SIMCOP VLCDJ Basic Programming Model: [2] [3] [4] [5]
- ISS SIMCOP VLCDJ Register Manual: [6]

Table 8-1423. VLCDJD_DCTERR

Address Offset	0x0000 0064		
Physical Address	0x5202 0664 0x5506 0664	**Instance**	VLCDJ_L3 VLCDJ_CORTEX-M3
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																		ERRPTR													

Bits	Field Name	Description	Type	Reset
31:14	RESERVED	Read returns 0.	R	0x00000
13:0	ERRPTR	Byte address pointer to DCT coefficients, near where decode error occurs (read-only)	R	0x0000

Table 8-1424. Register Call Summary for Register VLCDJD_DCTERR

ISS Still Image Coprocessor

- ISS SIMCOP VLCDJ Functional Description: [0]
- ISS SIMCOP VLCDJ Register Manual: [1]

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8.4.7 ISS SIMCOP Rotation Accelerator Module

This section describes the rotation accelerator (ROT) module in the still-image coprocessor (SIMCOP) subsystem.

8.4.7.1 ISS SIMCOP ROT Overview

The ROT module is intended to be used in the SIMCOP to perform block data rotation and data shifting from one SIMCOP local memory to another. The following formats and operations are supported:

- YUV4:2:2 and generic 8-/16-/32-bit data block rotation by 90, 180, and 270 degrees
- YUV4:2:0 rotation by 90, 180, and 270 degrees
- Multiple-block rotation
- Data block shifting
- Data block horizontal circular shifting

The ROT supports a simple 1-block-per-initiation interaction, and includes a microcontroller unit (MCU) software-writable enable bit and hardware trigger signal to start the processing (see Section 8.4.7.3.7, *ISS SIMCOP ROT Synchronization*). It relies on external direct memory access (DMA) for transfers, and can work with the MCU or hardware sequencer to coordinate between transfer and computation.

The ROT has an input and output memory interface (see Figure 8-286). The rotation and horizontal-shifting operations read from the input memory and write to the output memory. The module connects to an input memory of up to 16KB (2048 × 64-bit), and an output memory of up to 16KB (2048 × 64-bit) using synchronous single-port memory interface.

Figure 8-284 is an overview of the ROT.

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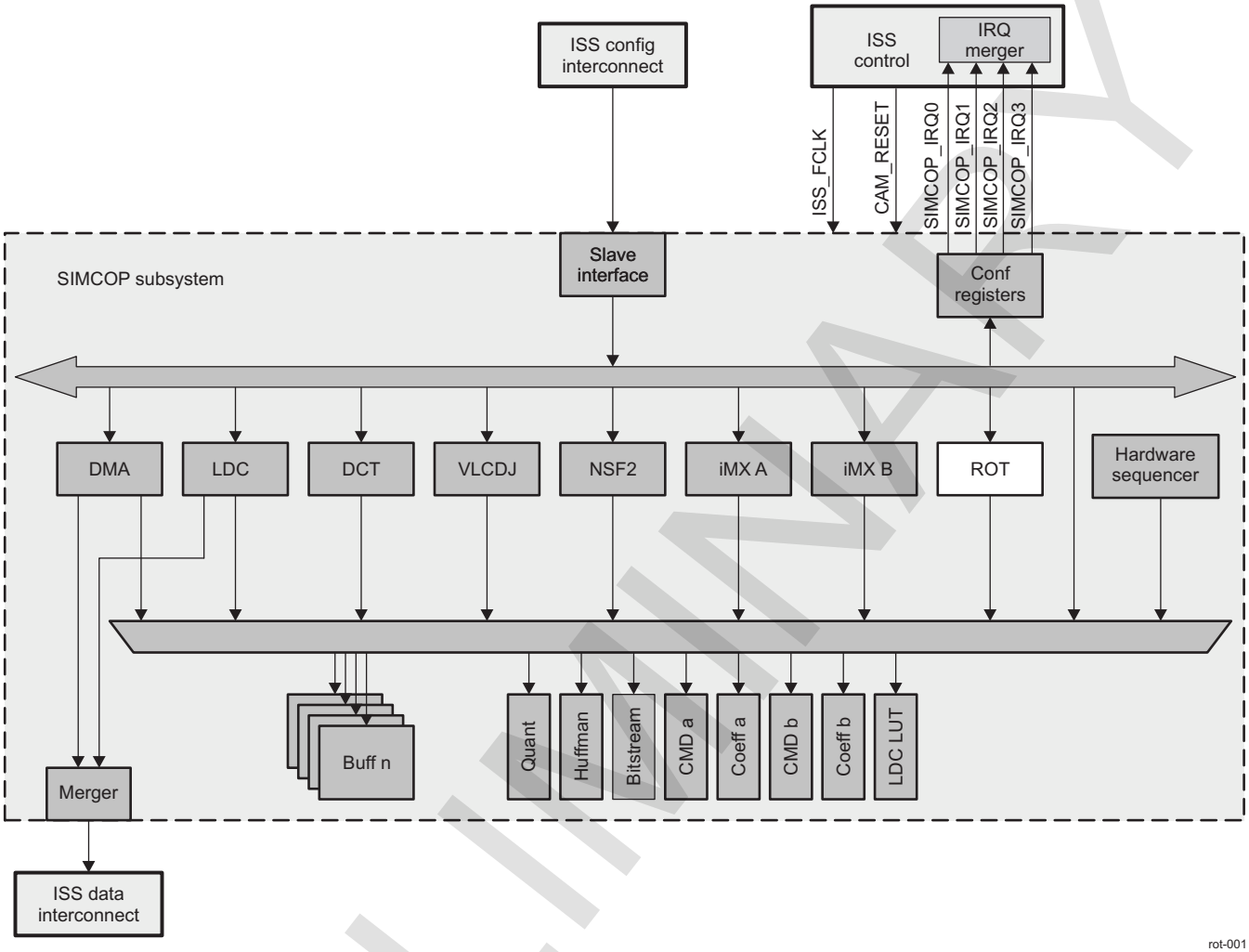
Figure 8-284. ISS SIMCOP ROT Module Overview



8.4.7.2 ISS SIMCOP ROT Integration

The ROT is part of the SIMCOP subsystem in the imaging subsystem (ISS). Figure 8-285 shows the integration of the ROT in the SIMCOP subsystem.

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Figure 8-285. ISS SIMCOP ROT Engine Integration

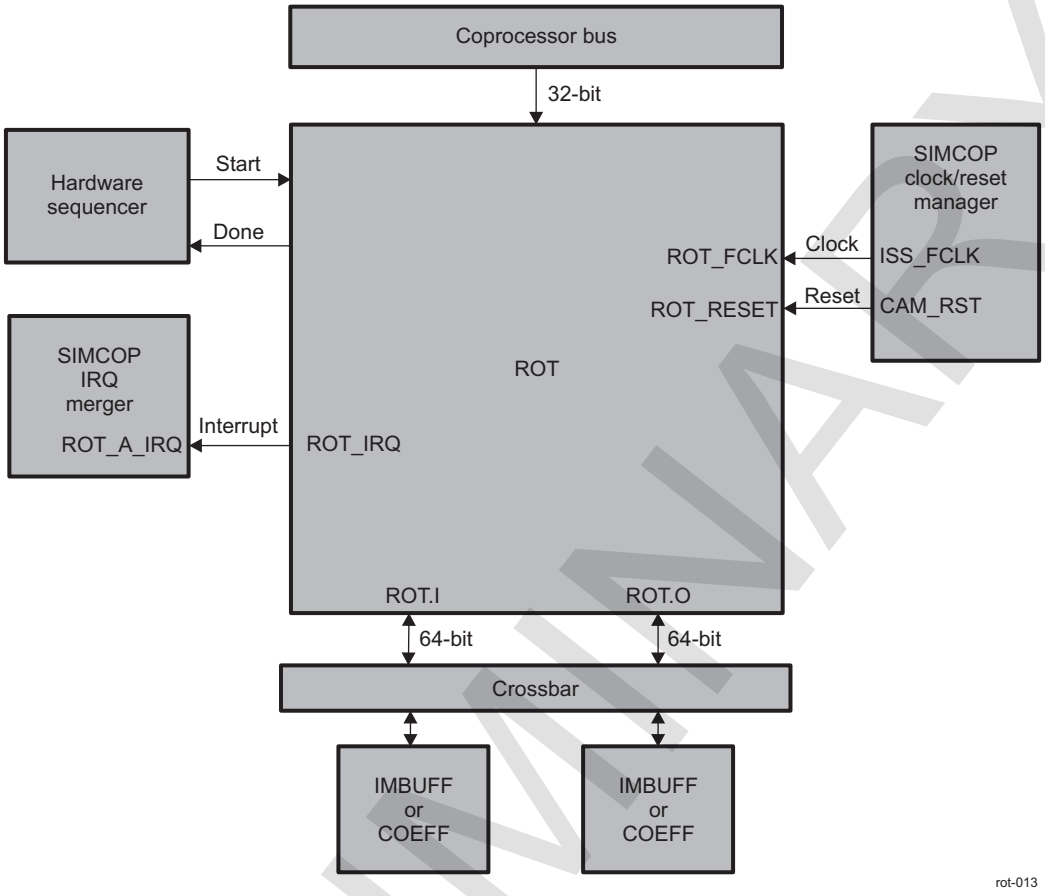

Table 8-1425 through Table 8-1427 list the integration attributes, clocks and resets, and hardware requests, respectively, of the SIMCOP ROT.

Table 8-1425. ISS SIMCOP ROT Integration Attributes

Module Instance	Attributes
	Power Domain
ROT	PD_CAM

Table 8-1426. ISS SIMCOP ROT Clocks and Resets

Clocks				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
ROT	ROT_FCLK	ISS_FCLK	PRCM	Functional clock provided by ISS_CLK from the power, reset, and clock management (PRCM) module. It is used by all ISS submodules and ISS top-level resources.
Resets				
ROT	ROT_RESET	CAM_RST	PRCM	ISS and SIMCOP global reset

For information about clock and reset management, see Section 8.4.1.2.1, *ISS SIMCOP Local Power and Clock Management*.

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Table 8-1427. ISS SIMCOP ROT Hardware Requests

Interrupt Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
ROT	ROT_IRQ	ROT_A_IRQ	SIMCOP IRQ merger	Event triggered by the ROT engine.

For more information about interrupt requests, see Section 8.4.1.2.3, *Interrupt Merger*.

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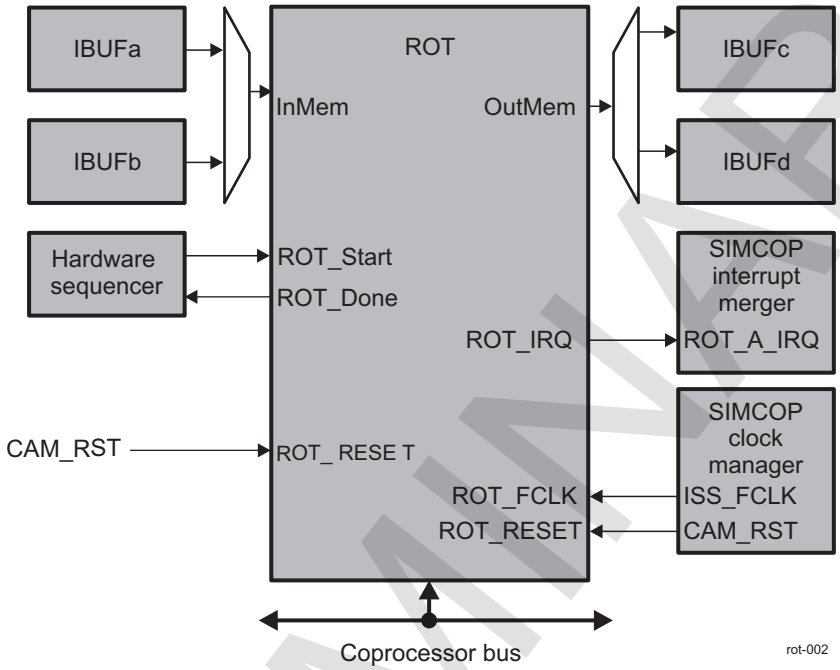
8.4.7.3 ISS SIMCOP ROT Functional Description

8.4.7.3.1 ISS SIMCOP ROT Block Diagram

Figure 8-286 shows the block diagram of the ROT.

Figure 8-286. ISS SIMCOP ROT Module Block Diagram



8.4.7.3.2 ISS SIMCOP ROT Clock Configuration

The ROT receives a functional clock (ISS_FCLK) from the ISS SIMCOP. The configuration clock is derived from the functional clock and interconnect clock enable signal (the ROT_CFG[9] AUTOGATING bit).

8.4.7.3.3 ISS SIMCOP ROT Reset

The ROT receives an asynchronous hardware reset signal (CAM_RST) from the ISS SIMCOP.

8.4.7.3.4 ISS SIMCOP ROT Power Management

The ROT uses clock autogating to conserve power. When a subblock is not in use, the corresponding clock tree is gated. The ROT_CFG[9] AUTOGATING bit controls whether autogating is enabled.

8.4.7.3.5 ISS SIMCOP ROT Interrupt Requests

One interrupt output line, ROT_A_IRQ, is used as a sideband signal of the interconnect slave port. This signal is connected to the SIMCOP interrupt merger. See Section 8.4.1.2.3, *Interrupt Merger*.

8.4.7.3.6 ISS SIMCOP ROT DMA Requests

The ROT has no DMA requests from the module.

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8.4.7.3.7 ISS SIMCOP ROT Synchronization

The ROT has a simple one-block-per-task interaction with outside logic/microprocessor unit (MPU). The module can be started by setting the ROT_CTRL[0] EN bit to 0x1, or through the ROT_START signal of the hardware sequencer interface. When the ROT completes the specified rotation or data shift task, it sends a pulse on the ROT_DONE signal and, when the interrupt is enabled, sends a pulse on the ROT_A_IRQ interrupt output.

The ROT_CFG[8] TRIG_SRC bit specifies to which source the hardware must respond:

- When the ROT is idle and the ROT_CFG[8] TRIG_SRC bit is set to 0x0, hardware responds to the memory mapped register (MMR) mechanism, and any pulses on the start signal are ignored.
- When the ROT is idle and the ROT_CFG[8] TRIG_SRC bit is set to 0x1, hardware responds to the hardware start signal, and any write operation to the enable bit field is ignored.

When the ROT is busy, both triggering mechanisms are ignored.

8.4.7.3.8 ISS SIMCOP ROT Formats and Operations

The ROT supports the formats and operations described in the following sections.

8.4.7.3.8.1 ISS SIMCOP ROT YUV4:2:0 and Generic 8-/16-/32-Bit Data Block Rotation

Rotation of YUV4:2:0 and generic 8-bit, 16-bit, 32-bit data blocks is straightforward. None of the data points are altered; each data point is copied to an appropriate address location. Zero-degree rotation is included for completeness of the programming model, and involves only data copy.

When YUV4:2:0 data have separate Y and UV processing and must be separately rotated, Y data can use generic 8-bit data rotation, and UV data can use generic 16-bit data rotation.

8.4.7.3.8.2 ISS SIMCOP ROT YUV4:2:2 Rotation

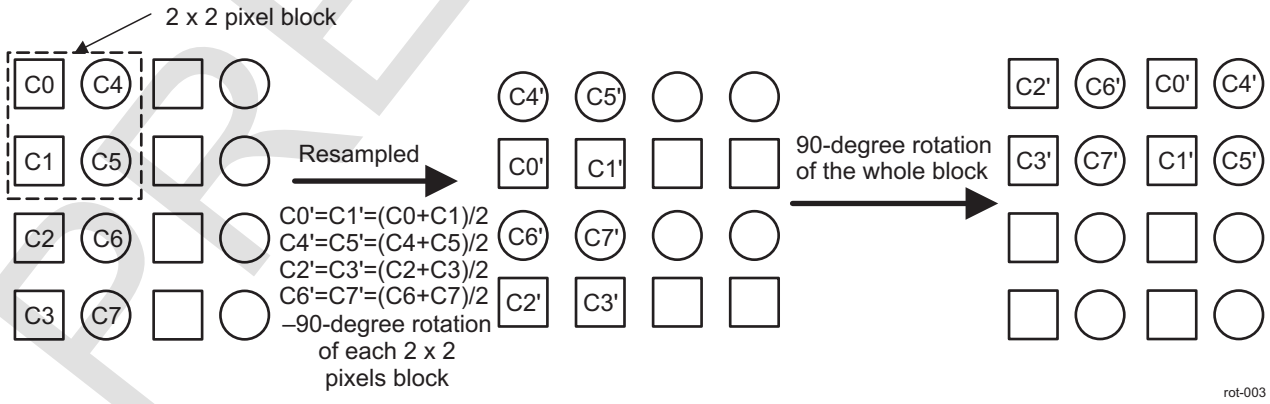
Various rotation cases of YUV4:2:2 data are described in the following and shown in Figure 8-287 through Figure 8-289 using 4 × 4-pixel block as an example.

The degree of rotation is defined as rotating clockwise. For 90-degree rotation:

- The two U samples in each 2 × 2-pixel input block are averaged and then replicated to provide the two U samples in the 2 × 2-pixel output block.
- V samples - processed in the same way.

Thus, each 2N × 2N-pixel output block depends on only one 2N × 2N-pixel input block. After resampling every 2 × 2-pixel block, it is rotated –90 degrees, and then the whole 2N × 2N block is rotated 90 degrees.

Figure 8-287. ISS SIMCOP ROT 90-Degree Rotation of YUV4:2:2 Data



The same algorithm is used for 270-degree rotation.

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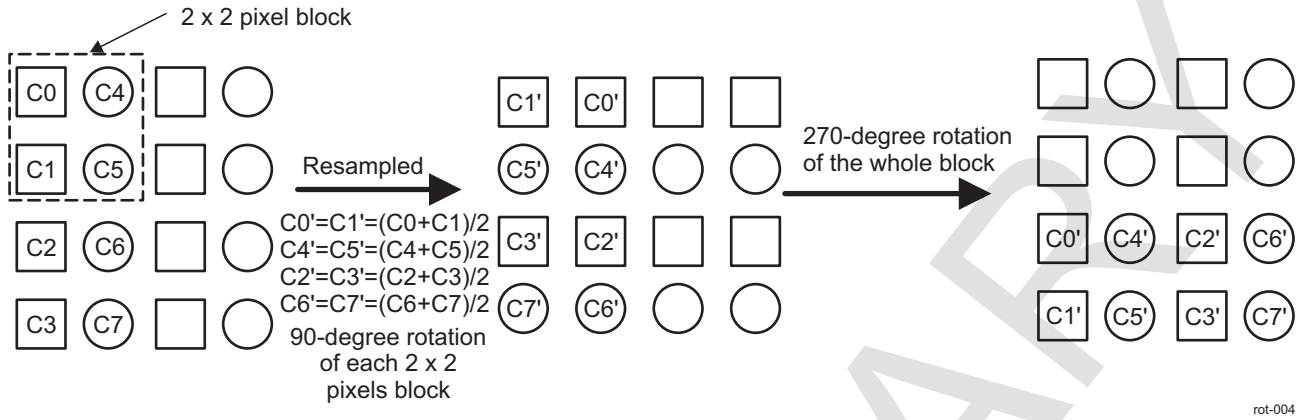
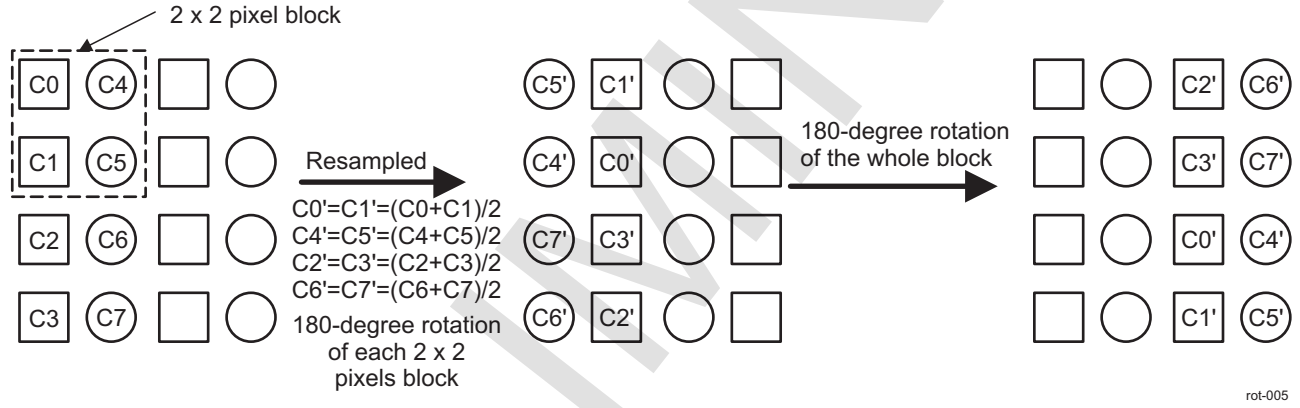
Figure 8-288. ISS SIMCOP ROT 270-Degree Rotation of YUV4:2:2 Data



For 180-degree rotation, there is no arithmetic operation; Chroma values are simply shifted horizontally before being rotated.

Figure 8-289. ISS SIMCOP ROT 180-Degree Rotation of YUV4:2:2 Data



NOTE: The intermediate process of 2 × 2 pixel block rotation, represented in the middle section in Figure 8-287 through Figure 8-289, does not involve data storage and reading into memory. This middle section is for better visualization of the process. The whole process is performed with a single memory reading and writing.

Zero-degree rotation is included for completeness of programming model, and involves only data copy.

8.4.7.3.8.3 ISS SIMCOP ROT Multiple-Block Rotation

For generic 8-/16-/32-bit data rotation and YUV4:2:0/4:2:2 rotation, multiple-block operation per hardware task is supported.

Figure 8-290 through Figure 8-293 show the multiple-block rotation feature.

The multiple blocks are in the horizontal dimension, and the blocks are horizontally adjacent to one another. In other words, in the source data and 180-degree rotated data, address offset between blocks is the source block width times the data size.

In the 90-degree and 270-degree rotated data, address offset is the source block height times the data size. The source/destination line offsets must be sufficiently large to accommodate the multiple blocks.

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Figure 8-290. ISS SIMCOP ROT Block Representation Before Rotation

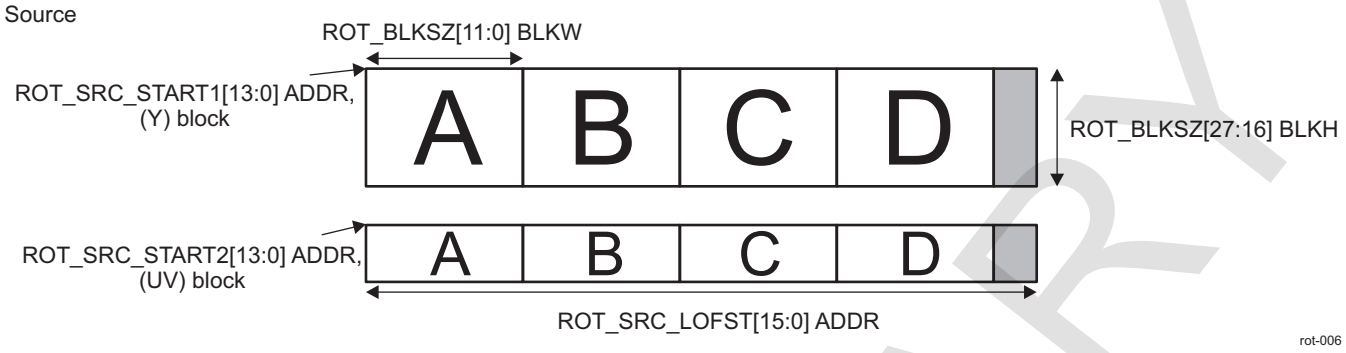


Figure 8-291. ISS SIMCOP ROT 90-Degree Block Rotation

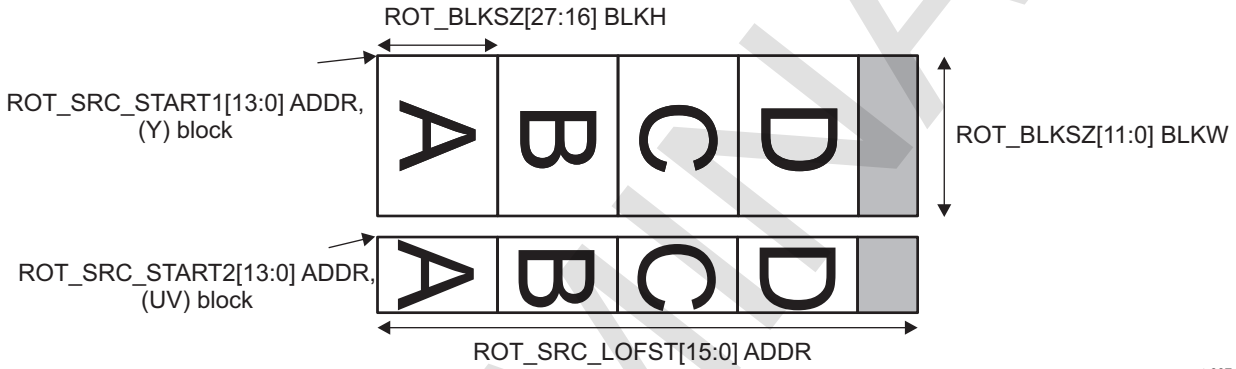


Figure 8-292. ISS SIMCOP ROT 180-Degree Block Rotation

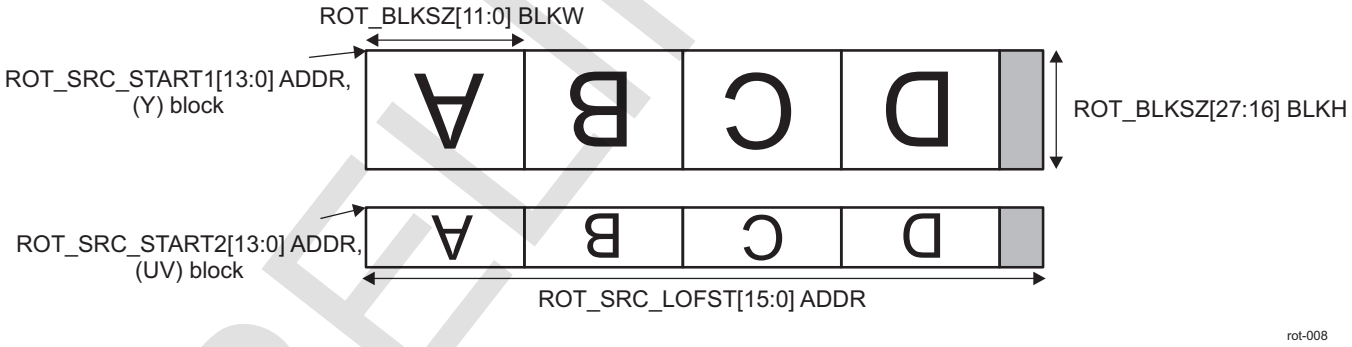
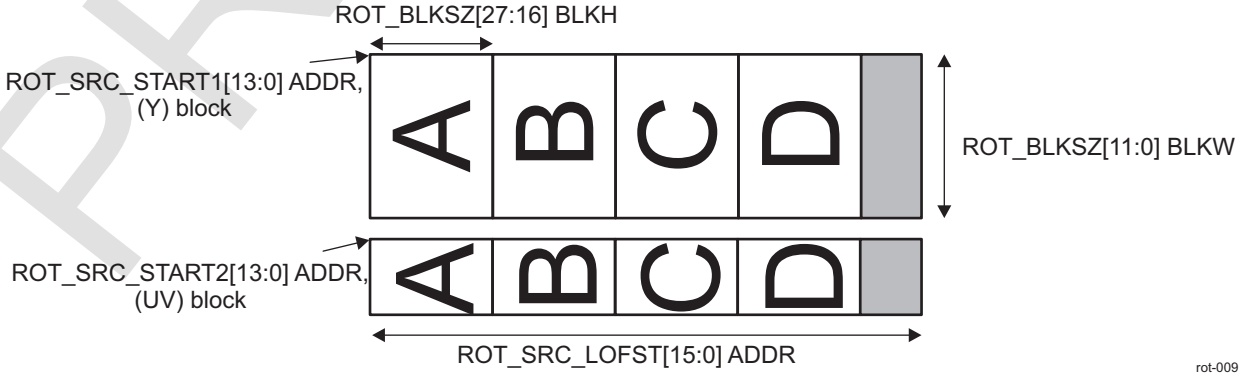


Figure 8-293. ISS SIMCOP ROT 270-Degree Block Rotation



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The operation is configured with these parameters:

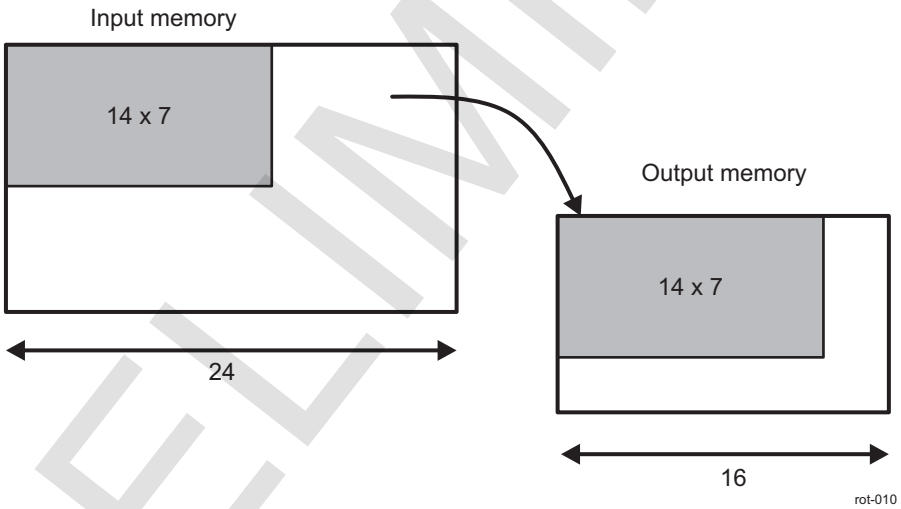
- ROT_CFG[2:0] OP (rotation orientation)
- ROT_CFG[6:4] FMT (data format)
- ROT_CFG[15:12] NBLKS (number of blocks minus 1; register value of 0 means one block, etc.)
- ROT_BLKSZ[11:0] BLKW (width of each block; all blocks have the same width/height)
- ROT_BLKSZ[27:16] BLKH (height of each block)
- ROT_SRC_START1[13:0] ADDR (starting address of the first input block)
- ROT_SRC_LOFST[15:0] ADDR (line offset of input block)
- ROT_DST_START1[13:0] ADDR (starting address of the first output block)
- ROT_DST_LOFST[15:0] ADDR (line offset of output block)
- ROT_SRC_START2[13:0] ADDR (starting address of the first input UV block, if format is YUV4:2:0)
- ROT_DST_START2[13:0] ADDR (starting address of the first output UV block, if format is YUV4:2:0)

8.4.7.3.8.4 ISS SIMCOP ROT Data-Block Shifting

The ROT supports shifting of 2-dimensional (2D) data blocks in 8-bit granularity. This function is intended to supplement the SIMCOP DMA module, which operates on 128-bit alignment.

Figure 8-294 is an example of a 14 × 7-byte data block copied from one location in input memory to another location in output memory.

Figure 8-294. ISS SIMCOP ROT Data-Block Shifting Example



The following parameters are specified:

- ROT_BLKSZ[11:0] BLKW = 14 (in bytes)
- ROT_BLKSZ[27:16] BLKH = 7 (in rows)
- ROT_SRC_LOFST[15:0] LOFST = 24 (in bytes)
- ROT_DST_LOFST[15:0] LOFST = 16 (in bytes)

NOTE: This function can be used to shift horizontally as well as vertically.

8.4.7.3.8.5 ISS SIMCOP ROT Data-Block Horizontal Circular Shifting

The ROT supports shifting of 2D data blocks in 8-bit granularity, with horizontal circular buffer addressing. This function is intended to supplement the SIMCOP DMA module, which operates on 128-bit alignment.

Figure 8-295 is an example of a 28 × 7-byte data block copied from one location in input memory to another location in output memory, and horizontal wrap-around occurs in the output memory.

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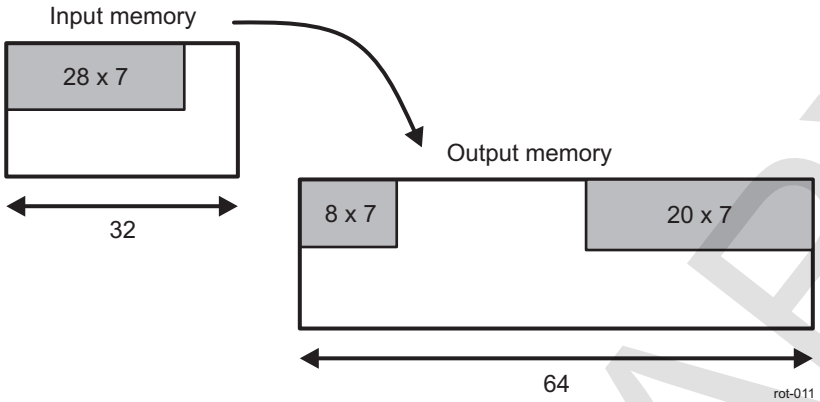
Figure 8-295. ISS SIMCOP ROT Horizontal Circular Shifting Example



The following parameters are specified:

- ROT_BLKSZ[11:0] BLKW = 28 (in bytes)
- ROT_BLKSZ[27:16] BLKH = 7 (in rows)
- ROT_SRC_LOFST[15:0] LOFST = 32 (in bytes)
- ROT_DST_LOFST[15:0] LOFST = 64 (in bytes)

Wrapping around is allowed in the input memory, in the output memory, or in both. For this mode of operation, the line offset of the source and destination must be a power of 2, and at least 32 bytes. Source and destination line offsets can be different. This function is used to handle misaligned SDRAM data. The following example shows that the line offset is at least the minimal transfer width, or the SDRAM burst. For target applications, 32 bytes is the minimal burst size to support.

NOTE: This function can be used to shift horizontally as well as vertically. Input and output blocks can also have different line offsets.

This mode of operation is intended to be used to manage 2D data blocks that are out of SDRAM alignment (for example, to crop out the left-most 2 pixels of the ISP YUV4:2:2 output image before JPEG compression). Assume that the ISP output is 64-byte SDRAM burst-aligned; thus, the starting address for JPEG input is 4 bytes out of alignment. Without the horizontal circular shifting function, the best solution is to use wide data blocks (for example, 128 pixels = 256 bytes wide) to reduce the bandwidth penalty of misalignment (costing five bursts to get four bursts worth of data). With horizontal circular shifting, the bandwidth penalty can be eliminated. In this example, the SIMCOP DMA is configured to transfer aligned data, and the ROT is used to perform the crop-out. A memory transaction log would be:

- The DMA writes columns 0–63, starting at byte address 0.
- The DMA writes columns 64–127, starting at byte address 64.
- The ROT module reads columns 4–67, starting at byte address 4.
- The DMA writes columns 128–191, starting at byte address 0.
- The ROT module reads columns 68–131, starting at byte address 68, and so on.

Figure 8-296 shows the data movement by the DMA and the ROT.

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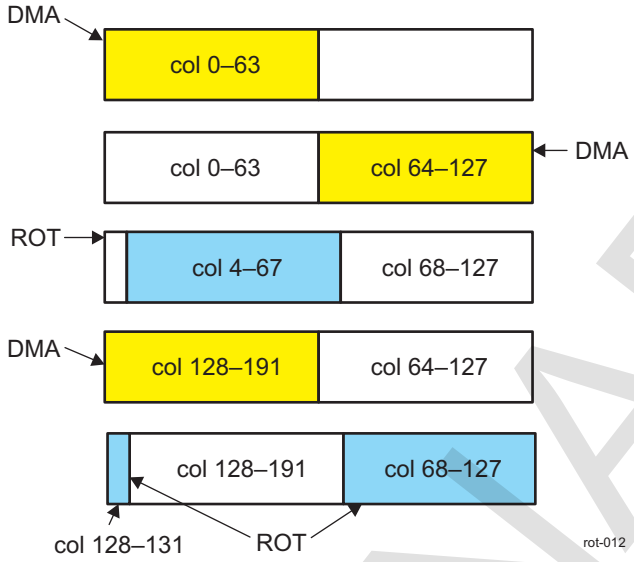
Figure 8-296. ISS SIMCOP ROT Using Horizontal Circular Shifting to Manage Misaligned Data



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8.4.7.4 ISS SIMCOP ROT Module Programming Guide

8.4.7.4.1 ISS SIMCOP ROT Low-Level Programming Models

This section describes the low-level programming sequences for configuration and use of the ROT.

8.4.7.4.1.1 ISS SIMCOP ROT Global Initialization

8.4.7.4.1.1.1 ISS SIMCOP ROT Surrounding Modules Global Initialization

This section identifies the requirements for initializing the surrounding modules when the ROT is to be used for the first time after a device reset. Initialization of surrounding modules is based on the integration and environment of the module.

Table 8-1428 describes the global initialization of the surrounding modules.

Table 8-1428. ISS SIMCOP ROT Global Initialization of Surrounding Modules

Surrounding Modules	Comments
SIMCOP (clock management)	The ROT functional clock must be enabled. See Section 8.4.7.3.2, *ISS SIMCOP ROT Clock Configuration*.
SIMCOP (power management)	The ROT must be enabled (SIMCOP_CLKCTRL[7] ROT_A). See Section 8.4.1.2.1, *ISS SIMCOP Local Power and Clock Management*.
Buffers	Configure the ROT access to the image buffer inside the SIMCOP_HWSEQ_STEP_SWITCH_i register. See Section 8.4.2, *ISS SIMCOP Hardware Sequencer and Buffers Module*.
SIMCOP IRQ merger	Configure SIMCOP to handle the ROT interrupts. See Section 8.4.1.2.3, *Interrupt Merger*.
SIMCOP hardware sequencer	Configure the hardware sequencer to activate the ROT. See Section 8.4.2, *ISS SIMCOP Hardware Sequencer and Buffers Module*.

8.4.7.4.1.1.2 ISS SIMCOP ROT Global Initialization

Table 8-1429 describes the global initialization of the ROT.

Table 8-1429. ISS SIMCOP ROT Global Initialization of the ROT

Step	Register/Bit Field/Programming Model	Value
Enable the ROT.	ROT_CTRL[0] EN	0x0

8.4.7.4.1.2 ISS SIMCOP ROT Operational Modes Configuration

8.4.7.4.1.2.1 ISS SIMCOP ROT Rotation

The proper value for the trigger source bit (ROT_CFG[8] TRIG_SRC) is set depending on whether the operation is to be triggered by software, writing to MMR, or by the hardware sequencer. Table 8-1430 lists the procedure to set the value of the trigger source bit.

Table 8-1430. ISS SIMCOP ROT Trigger Source Bit Value

Step	Register/Bit Field/Programming Model	Value
Configure the degree of rotation.	ROT_CFG[2:0] OP	xxx
Configure the data format.	ROT_CFG[6:4] FMT	xxx
Specify the block width and height.	ROT_BLKSZ[11:0] BLKW ROT_BLKSZ[27:16] BLKH	xxx
Specify the input and output starting addresses.	ROT_SRC_START1[13:0] ADDR, ROT_DST_START1[13:0] ADDR	xxx
Specify the line offsets.	ROT_SRC_LOFST[15:0] LOFST, ROT_DST_LOFST[15:0] LOFST	xxx

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Table 8-1430. ISS SIMCOP ROT Trigger Source Bit Value (continued)

Step	Register/Bit Field/Programming Model	Value
For UV data of YUV4:2:0, input and output second starting addresses.	ROT_SRC_START2[13:0] ADDR, ROT_DST_START2[13:0] ADDR	xxx

8.4.7.4.1.2.2 ISS SIMCOP ROT Data-Block Shifting

Table 8-1431 lists the bit field values for data-block shifting.

Table 8-1431. ISS SIMCOP ROT Data-Block Shifting

Step	Register/Bit Field/Programming Model	Value
Configure shifting.	ROT_CFG[2:0] OP	xxx
Set the data shifting block.	ROT_CFG[6:4] FMT	xxx
Specify the block width and height.	ROT_BLKSZ[11:0] BLKW, ROT_BLKSZ[27:16] BLKH	xxx
Specify the input and output starting addresses.	ROT_SRC_START1[13:0] ADDR, ROT_DST_START1[13:0] ADDR	xxx
Specify the line offsets.	ROT_SRC_LOFST[15:0] LOFST, ROT_DST_LOFST[15:0] LOFST	xxx

Once the input data and output buffer are available, the ROT_CTRL[0] EN bit is set to 1 to trigger the operation through software. Alternatively, DMA transfer(s) and the hardware sequencer are configured to trigger the ROT with the hardware start signal when appropriate.

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8.4.7.5 ISS SIMCOP ROT Register Manual

8.4.7.5.1 ISS SIMCOP ROT Instance Summary

Table 8-1432 lists the ROT instance.

Table 8-1432. ISS SIMCOP ROT Instance Summary

Module Name	Base Address L3 Interconnect	Base Address Cortex-M3 Private Access	Size
ROT	0x5202 0700	0x5506 0700	64 bytes

NOTE: Private Access is an access that does not use the L3/L4 interconnects.

8.4.7.5.2 ISS SIMCOP ROT Registers

8.4.7.5.2.1 ISS SIMCOP ROT Register Summary

Table 8-1433 summarizes the ROT registers.

Table 8-1433. ROT Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	Physical Address L3 Interconnect	Physical Address Cortex-M3 Private Access
ROT_REVISION	R	32	0x0000 0000	0x5202 0700	0x5506 0700
ROT_CTRL	W	32	0x0000 0004	0x5202 0704	0x5506 0704
ROT_CFG	RW	32	0x0000 0008	0x5202 0708	0x5506 0708
ROT_BLKSZ	RW	32	0x0000 000C	0x5202 070C	0x5506 070C
ROT_SRC_START1	RW	32	0x0000 0010	0x5202 0710	0x5506 0710
ROT_SRC_LOFST	RW	32	0x0000 0014	0x5202 0714	0x5506 0714
ROT_DST_START1	RW	32	0x0000 0018	0x5202 0718	0x5506 0718
ROT_DST_LOFST	RW	32	0x0000 001C	0x5202 071C	0x5506 071C
ROT_SRC_START2	RW	32	0x0000 0020	0x5202 0720	0x5506 0720
ROT_DST_START2	RW	32	0x0000 0024	0x5202 0724	0x5506 0724

8.4.7.5.2.2 ISS SIMCOP ROT Register Descriptions

through describe the ROT registers.

Table 8-1434. ROT_REVISION

Address Offset	0x0000 0000		
Physical Address	0x5202 0700 0x5506 0700	**Instance**	ROT_L3 ROT_CORTEX-M3
Description	Module revision		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

Bits	Field Name	Description	Type	Reset
31:0	RESERVED	IP Revision	R	TI Internal Data

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Table 8-1435. Register Call Summary for Register ROT_REVISION

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- ISS SIMCOP ROT Register Manual: [0]

Table 8-1436. ROT_CTRL

Address Offset	0x0000 0004		
Physical Address	0x5202 0704 0x5506 0704	**Instance**	ROT_L3 ROT_CORTEX-M3
Description	Control		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																BUSY	RESERVED														EN

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15	BUSY	Idle/busy status (read-only) 0 = Idle, 1 = Busy	R	0
14:1	RESERVED		R	0x0000
0	EN	Module enable, writing 1 starts the module; always reads as 0.	W	0

Table 8-1437. Register Call Summary for Register ROT_CTRL

ISS Still Image Coprocessor

- ISS SIMCOP ROT Functional Description: [0]
- ISS SIMCOP ROT Module Programming Guide: [1] [2]
- ISS SIMCOP ROT Register Manual: [3]

Table 8-1438. ROT_CFG

Address Offset	0x0000 0008		
Physical Address	0x5202 0708 0x5506 0708	**Instance**	ROT_L3 ROT_CORTEX-M3
Description	Configuration		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																NBLKS				RESERVED		AUTOGATING	TRIG_SRC	RESERVED			FMT			RESERVED		OP	

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	NBLKS	Number of blocks minus 1 0: 1 block, 1: 2 blocks, etc.	RW	0x0
11:10	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
9	AUTOGATING	Internal interconnect and functional clock gating 0: Interconnect and functional clocks are free-running. 1: Automatic clock gating is applied, based on the interface activity for the interface clock, and on the functional activity for the functional clocks.	RW	1
8	TRIG_SRC	Trigger source 0 = MMR write 1 = Hardware start signal	RW	0
7	RESERVED		R	0
6:4	FMT	Data format 0 = 8-bit data 1 = 16-bit data 2 = 32-bit data 3 = YUV4:2:2 data 4 = YUV4:2:0 data	RW	0x0
3	RESERVED		R	0
2:0	OP	Operation 0 = Rotate 0 degree 1 = Rotate 90 degrees 2 = Rotate 180 degrees 3 = Rotate 270 degrees 4 = Data shift (FMT = 0) 5 = Horizontal circular (FMT = 0) shift	RW	0x0

Table 8-1439. Register Call Summary for Register ROT_CFG

ISS Still Image Coprocessor

- ISS SIMCOP ROT Functional Description: [0] [1] [2] [3] [4] [5] [6] [7]
- ISS SIMCOP ROT Module Programming Guide: [8] [9] [10] [11] [12]
- ISS SIMCOP ROT Register Manual: [13]

Table 8-1440. ROT_BLKSZ

Address Offset	0x0000 000C		
Physical Address	0x5202 070C 0x5506 070C	**Instance**	ROT_L3 ROT_CORTEX-M3
Description	Block size		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								BLKH								RESERVED								BLKW							

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:16	BLKH	Block height, in pixels (YUV4:2:0/4:2:2) or number of rows (8-/16-/32-bit). Should be a multiple of 8, and at least 8, for rotation. Should be at least 1 for data shifting.	RW	0x000
15:12	RESERVED		R	0x0
11:0	BLKW	Block width, in pixels (YUV4:2:0/4:2:2) or data units (8-/16-/32-bit). Should be a multiple of 8, and at least 8, for rotation. Should be at least 4 for data shifting.	RW	0x000

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Table 8-1441. Register Call Summary for Register ROT_BLKSZ

ISS Still Image Coprocessor

- ISS SIMCOP ROT Functional Description: [0] [1] [2] [3] [4] [5]
- ISS SIMCOP ROT Module Programming Guide: [6] [7] [8] [9]
- ISS SIMCOP ROT Register Manual: [10]

Table 8-1442. ROT_SRC_START1

Address Offset	0x0000 0010		
Physical Address	0x5202 0710 0x5506 0710	**Instance**	ROT_L3 ROT_CORTEX-M3
Description	Source starting address		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																ADDR															

Bits	Field Name	Description	Type	Reset
31:14	RESERVED		R	0x00000
13:0	ADDR	Byte address Should be a multiple of 8 for rotation. No constraint for data shifting.	RW	0x0000

Table 8-1443. Register Call Summary for Register ROT_SRC_START1

ISS Still Image Coprocessor

- ISS SIMCOP ROT Functional Description: [0]
- ISS SIMCOP ROT Module Programming Guide: [1] [2]
- ISS SIMCOP ROT Register Manual: [3]

Table 8-1444. ROT_SRC_LOFST

Address Offset	0x0000 0014		
Physical Address	0x5202 0714 0x5506 0714	**Instance**	ROT_L3 ROT_CORTEX-M3
Description	Source line offset		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																LOFST															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:0	LOFST	Line offset in bytes Should be a multiple of 8 for rotation and normal data shifting. Should be a power of 2 and at least 32 for horizontal circular shifting.	RW	0x0000

Table 8-1445. Register Call Summary for Register ROT_SRC_LOFST

ISS Still Image Coprocessor

- ISS SIMCOP ROT Functional Description: [0] [1] [2]
- ISS SIMCOP ROT Module Programming Guide: [3] [4]
- ISS SIMCOP ROT Register Manual: [5]

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Table 8-1446. ROT_DST_START1

Address Offset	0x0000 0018		
Physical Address	0x5202 0718 0x5506 0718	**Instance**	ROT_L3 ROT_CORTEX-M3
Description	Destination starting address		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																ADDR															

Bits	Field Name	Description	Type	Reset
31:14	RESERVED		R	0x00000
13:0	ADDR	Byte address Should be a multiple of 8 for rotation. No constraint for data shifting.	RW	0x0000

Table 8-1447. Register Call Summary for Register ROT_DST_START1

ISS Still Image Coprocessor

- ISS SIMCOP ROT Functional Description: [0]
- ISS SIMCOP ROT Module Programming Guide: [1] [2]
- ISS SIMCOP ROT Register Manual: [3]

Table 8-1448. ROT_DST_LOFST

Address Offset	0x0000 001C		
Physical Address	0x5202 071C 0x5506 071C	**Instance**	ROT_L3 ROT_CORTEX-M3
Description	Destination line offset		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																LOFST															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:0	LOFST	Line offset in bytes Should be a multiple of 8 for rotation and normal data shifting. Should be a power of 2 and at least 32 for horizontal circular shifting.	RW	0x0000

Table 8-1449. Register Call Summary for Register ROT_DST_LOFST

ISS Still Image Coprocessor

- ISS SIMCOP ROT Functional Description: [0] [1] [2]
- ISS SIMCOP ROT Module Programming Guide: [3] [4]
- ISS SIMCOP ROT Register Manual: [5]

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Table 8-1450. ROT_SRC_START2

Address Offset	0x0000 0020		
Physical Address	0x5202 0720 0x5506 0720	**Instance**	ROT_L3 ROT_CORTEX-M3
Description	Source starting address 2 (only form YUV4:2:0 FMT = 2)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								ADDR							

Bits	Field Name	Description	Type	Reset
31:14	RESERVED		R	0x00000
13:0	ADDR	Byte address, should be a multiple of 8.	RW	0x0000

Table 8-1451. Register Call Summary for Register ROT_SRC_START2

ISS Still Image Coprocessor

- ISS SIMCOP ROT Functional Description: [0]
- ISS SIMCOP ROT Module Programming Guide: [1]
- ISS SIMCOP ROT Register Manual: [2]

Table 8-1452. ROT_DST_START2

Address Offset	0x0000 0024		
Physical Address	0x5202 0724 0x5506 0724	**Instance**	ROT_L3 ROT_CORTEX-M3
Description	Destination starting address 2 (only form YUV4:2:0 FMT = 2)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								ADDR							

Bits	Field Name	Description	Type	Reset
31:14	RESERVED		R	0x00000
13:0	ADDR	Byte address, should be a multiple of 8.	RW	0x0000

Table 8-1453. Register Call Summary for Register ROT_DST_START2

ISS Still Image Coprocessor

- ISS SIMCOP ROT Functional Description: [0]
- ISS SIMCOP ROT Module Programming Guide: [1]
- ISS SIMCOP ROT Register Manual: [2]

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Face Detect

This chapter describes the features and functions of the Face Detect (FDIF) module of the multimedia device.

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9.2 FDIF Integration 2110
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9.1 Face Detect Overview

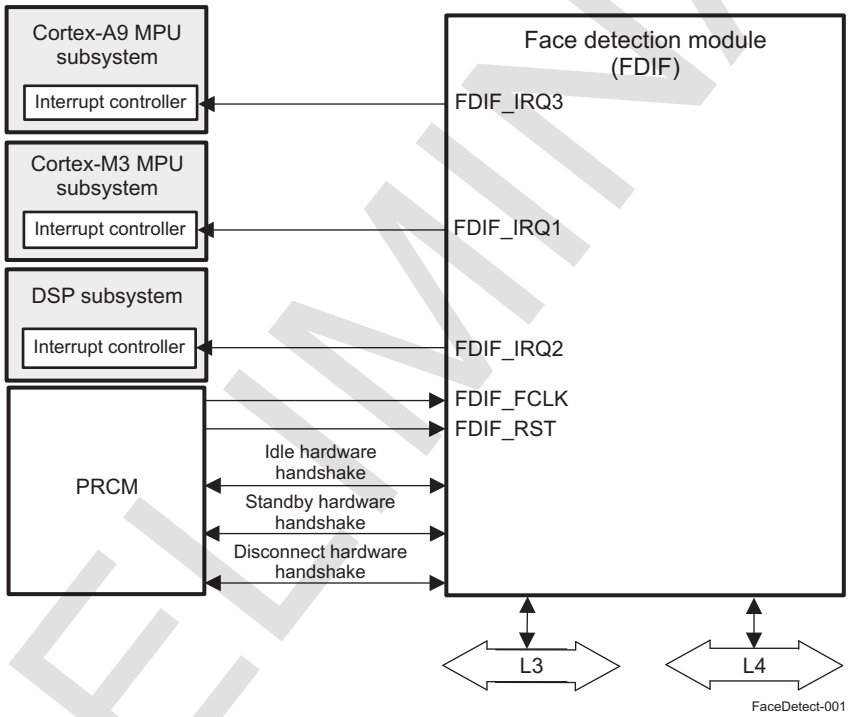
The FDIF module performs face detection within a picture stored in memory (QVGA luminance data resolution). This module is typically used for video encoding, face-based priority auto-focusing, or red-eye removal.

The face detect (FD) core is a standalone module: it embeds its own direct memory access (DMA) engine for accessing data in memory. The FD core is under microprocessor unit (MPU) control for its initialization and to start the processing operation.

The FD core supports single input resolution (QVGA) in a single format (8-bit luma). The FD core requires the input image to be stored in synchronous dynamic random access memory (SDRAM). The core also requires working memory mapped in SDRAM. The input image data (320x240) requires 75KB for the SDRAM and 51.25KB for the working memory.

Figure 9-1 is an overview of the FDIF. Three interrupt lines go to the three central processing units (CPUs) to allow control of the FD core module by different processors, but only one interrupt at a time can be active. The three interrupt lines provide flexibility for controlling the module.

Figure 9-1. Face Detect Highlight



9.1.1 Main Features

The FDIF has the following features:

- Two interconnects interface:
  - 32-bit-wide level 4 (L4) interface for register configuration
  - 32-bit-wide level 3 (L3) interface for command
- Supports the IDLE, STANDBY, and DISCONNECT protocols
- 3rd party IP features: For information about the input image features and detection capabilities, see Table 9-1.

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Table 9-1. 3rd Party IP Features

Items	Description
Input image size	QVGA input image size H x V = 320 x 240
Input data format	8-bit gray scale data in little-endian format (color pictures must be converted before FD can be applied) 0x00 = black and 0xFF = white
Face inclination	± 45 degrees
Face direction	Up/down: ± 30 degrees Left/right: ± 60 degrees
Maximum detection count	35 faces
Detection direction	The face orientation must be selected from the following possibilities: 0 degrees: Faces are vertical. + 90 degrees: Faces are rotated right by 90 degrees. – 90 degrees: Faces are rotated left by 90 degrees.
Detection minimum face size	Four grades are available: 20 pixels 25 pixels 32 pixels 40 pixels
Detection area	Detection start position: X = 0 to 160 Y = 0 to 120 Detection area size: X = 160 to 320 Y = 120 to 240
Detection result	The following information is provided by the module for each face: Size Position Angle Confidence level

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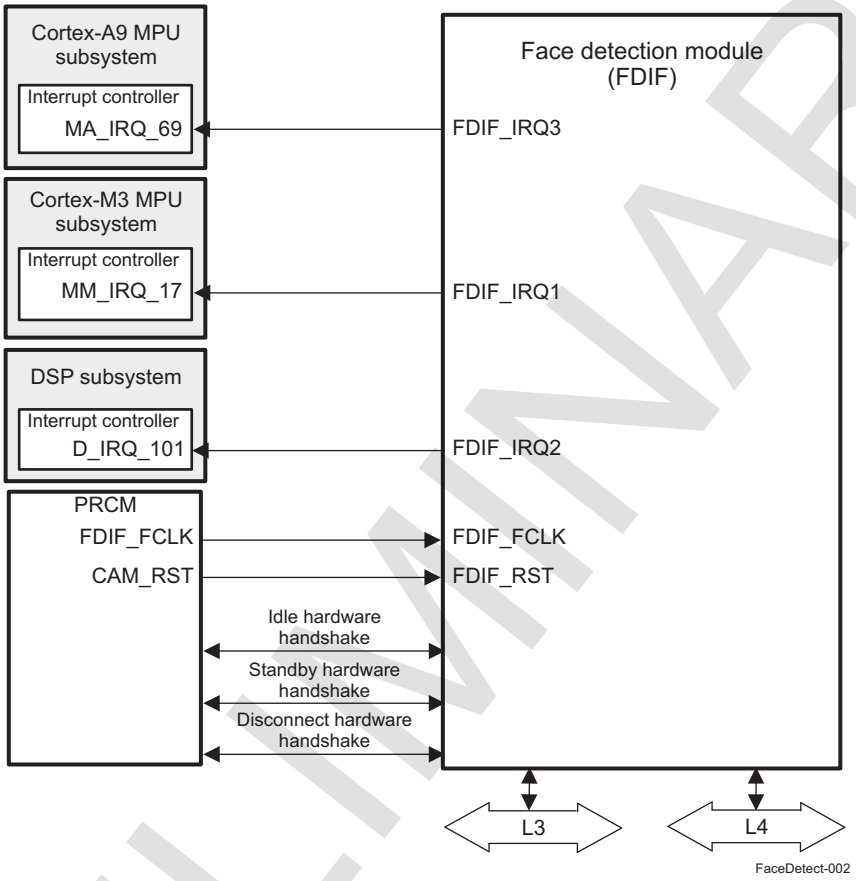
9.2 FDIF Integration

This section describes the integration of FDIF in the device, including information about clocks, resets, and hardware requests.

Figure 9-2 shows the integration of the module in the device.

Figure 9-2. FDIF Integration



NOTE: For more information about the IDLE, STANDBY, and DISCONNECT hardware handshakes, see Chapter 3, *Power, Reset, and Clock Management*.

Table 9-2 through Table 9-4 summarize the integration of the module in the device. For more information about the power domain or the clock and reset signals, see Chapter 3, *Power, Reset, and Clock Management*.

Table 9-2. Integration Attributes

Module Instance	Attributes		
	Power Domain	Wake-Up Capability	Interconnect
Face Detect	PD_CAM	No	L3

Table 9-3. Clocks and Resets

Clocks				
Module Instance	Destination Signal Name	Source Signal Name	Source	Description

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Table 9-3. Clocks and Resets (continued)

Face detect	FDIF_FCLK	FDIF_FCLK	PRCM	For information about PRCM clock gating and management, see Chapter 3, *Power, Reset, and Clock Management*.
Resets				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
Face detect	FDIF_RST	CAM_RST	PRCM	For information about PRCM reset sources and distribution, see Chapter 3, *Power, Reset, and Clock Management*.

Table 9-4. Hardware Requests

Interrupt Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
Face detect	FDIF_IRQ3	MA_IRQ_69	Cortex™-A9 MPU subsystem	FDIF interrupt to the Cortex-A9 MPU subsystem
Face detect	FDIF_IRQ1	MM_IRQ_17	Cortex™-M3 MPU subsystem	FDIF interrupt to the Cortex-M3 MPU subsystem
Face detect	FDIF_IRQ2	D_IRQ_101	DSP subsystem	FDIF interrupt to the digital signal processor (DSP) subsystem
No DMA Requests				

NOTE: For more information about interrupt sources, see Section 9.3.4, *Interrupts and Events*.

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9.3 FDIF Functional Description

9.3.1 FDIF Block Description

The FDIF is a standalone module. It has a port connected to the L4 interconnect, which is used for configuration, and a port connected to the L3 interconnect, which is used to read and write data to the system memory.

CAUTION

These ports are accessible only in 32 bits.

The FDIF core contains the following submodules:

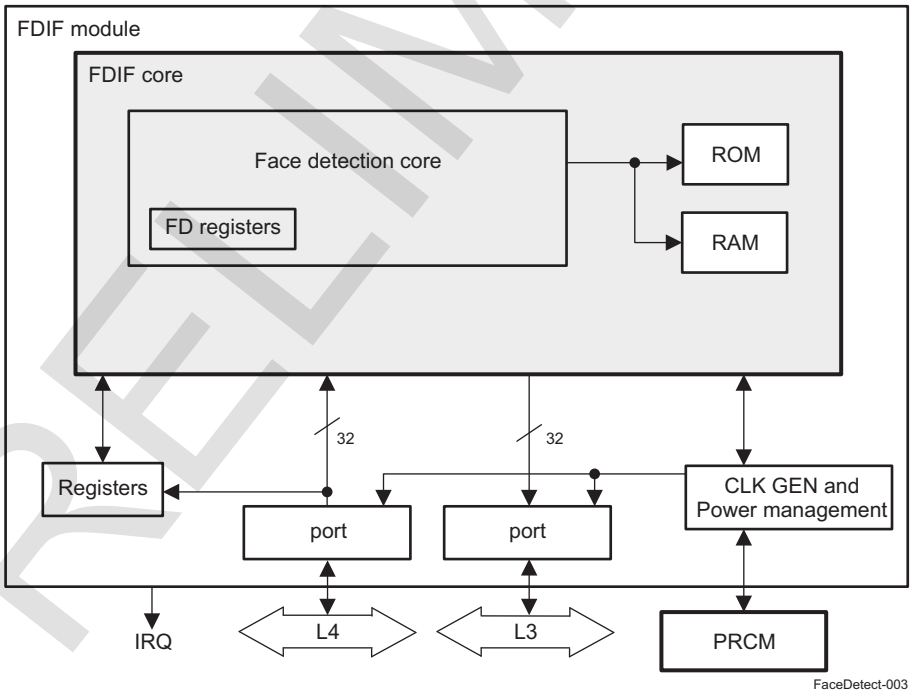
- Face detection (FD) IP core
- RAM and ROM memories

The FDIF module wraps the FD core for integration in the device. The following submodules are added:

- Clock generation
- Interrupt generation
- Power management
- L3 and L4 interface ports: Two ports required to decorrelate the FDIF clocks from other system clocks, one on the L3 port interface, and one on the L4 port interface.

Figure 9-3 shows the overall architecture of the FDIF.

Figure 9-3. FDIF Block Diagram



9.3.2 Software Reset

The module is reset by writing the FDIF_SYSCONFIG[0] SOFTRESET bit to 1. The bit is automatically reset by hardware. During reads, it always returns 0.

The FD core also provides a software reset setup by the FD_CTRL[0] SRST bit, but it is strongly recommended to use only the FDIF_SYSCONFIG[0] SOFTRESET bit.

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9.3.3 System Power Management

There is one clock domain in FDIF: the L4 port domain and L3 port domain are synchronized with the module functional clock domain, FDIF_FCLK.

Table 9-5 lists the power-management features available for FDIF.

NOTE:

- For more information about source clock gating, see Chapter 3, *Power, Reset, and Clock Management*.
- For descriptions of idle mode and standby mode and the power, reset, and clock management (PRCM) power handshake, see Chapter 3, *Power, Reset, and Clock Management*.

Table 9-5. Local Power-Management Features

Feature	Registers	Description
Clock autogating	No software control for it.	It is always enabled.
Slave idle modes	FDIF_SYSCONFIG[3:2] IDLEMODE	Force-idle, no-idle, and smart-idle modes are available
Clock activity	N/A	
Master standby modes	FDIF_SYSCONFIG[5:4] STANDBYMODE	Force-standby, no-standby, and smart-standby mode modes are available. See Section 9.3.3.2.1 for more information.
Global wake-up enable	N/A	
Wake-up sources enable	N/A	

9.3.3.1 Autogating

The FDIF performs clock autogating whenever possible. There is no software control for it; it is always enabled.

9.3.3.2 PRCM Hardware Handshake

The FDIF supports the IDLE protocol between the L4 port and the PRCM module and the STANDBY protocol between the L3 port and the PRCM module. The FDIF also supports the DISCONNECT protocol on the L4 and L3 ports.

The FDIF first initiates the STANDBY protocol with the PRCM module, which in turn generates the IDLE protocol with the FDIF. The functional clock is gated by the PRCM module only when the IDLE and STANDBY power-management protocols are complete.

For more information about these protocols, see Chapter 3, *Power, Reset, and Clock Management*.

9.3.3.2.1 Protocol Transitions

The FDIF goes to IDLE as soon as it is done processing and the MPU has read the results of the computation.

Figure 9-4 shows the principle. The 33-ms period corresponds to 30 fps, which is usually the target for imaging applications. Time spent in READ state (= ON state) is always the same, and the time in OFF state depends on the time spent in ON state.

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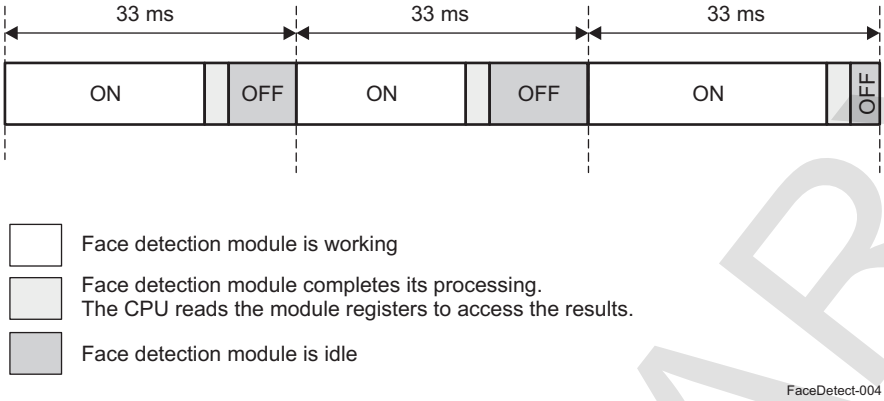
Figure 9-4. FDIF Power-Management Transitions



9.3.3.2.1.1 Normal Mode to Idle Mode

Software programs FDIF_SYSCONFIG[5:4] STANDBYMODE = 0x2 to program the power-management mode.

When its processing is complete, the FD core generates the FINISH_IRQ event. At this time the FD_CTRL[1] RUN bit reflects that the FD core is idle.

Software running on the MPU reads the results of the FD algorithm. When it finishes reading the results, it clears the FDIF_IRQSTATUS_RAW_j[8] FINISH_IRQ bit and writes FDIF_CTRL[5] MSTANDBY = 1 to initiate the MStandby signal generation. For more information about the STANDBY and IDLE hardware handshakes, see Chapter 3, *Power, Reset, and Clock Management*.

The FDIF clock can be gated only when the STANDBY and IDLE protocols are complete.

9.3.3.2.1.2 Idle Mode to Normal Mode

The PRCM module deasserts a signal to the FDIF under software control so that the module can switch back to normal mode. Then, the module functional clock is ensured and stable. Software disables the MStandby signal generation by writing FDIF_CTRL[5] MSTANDBY = 0, and then polls for FDIF_CTRL[6] MSTANDBY_HDSHK = 1 to ensure that the power-management handshaking is complete. For more information about the standby and idle modes, see Chapter 3, *Power, Reset, and Clock Management*.

9.3.4 Interrupts and Events

The FDIF has three interrupt lines (FDIF_IRQ1, FDIF_IRQ2, and FDIF_IRQ3) to enable flexibility for controlling the module. Each event can be enabled to only a single interrupt line (that is, to only one interrupt controller), because only one interrupt at a time can be active.

The FDIF generates events listed in Table 9-6. An interrupt can be enabled by using the FDIF_IRQENABLE_SET_j register and can be disabled by using the FDIF_IRQENABLE_CLR_j register.

Table 9-6. Interrupts and Events Description

Event Name	Description
FDIF_IRQSTATUS_RAW_j / FDIF_IRQSTATUS_j[8] FINISH_IRQ	This event is generated by the FD IP core. It flags the completion of the processing by the IP.
FDIF_IRQSTATUS_RAW_j / FDIF_IRQSTATUS_j[0] ERR_IRQ	This event flags that the L3 port has received an error.

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The FDIF_IRQSTATUS_RAW_j and FDIF_IRQSTATUS_j registers give the interrupt status. The difference between them is that the FDIF_IRQSTATUS_RAW_j register is set even if events are not enabled.

The FDIF_IRQSTATUS_j register can be used to clear events.

9.3.5 Typical Use

Typically, FD processing is applied to buffers provided by the ISP module, already in the correct format.

To enable FD processing, the 32-bit address of the input image in memory must be set up in the FDIF_PICADDR register, and the 32-bit address of the working memory must be set up in the FDIF_WKADDR register.

The detection condition settings can be set with the following registers:

- FD_DCOND
- FD_STARTX
- FD_STARTY
- FD_SIZEX
- FD_STARTY

For more information, see Section 9.4, *FDIF Programming Guide*.

When the FD_CTRL[1] RUN bit is set to 1, the process starts. When the process is complete (FD_CTRL[2] FINISH = 1), the results are available in the following registers:

- FD_DNUM
- FD_CENTERX_i
- FD_CENTERY_i
- FD_CONFSIZE_i
- FD_ANGLE_i

For more information, see Section 9.4, *FDIF Programming Guide*.

9.3.6 Performance Parameters

Table 9-7 lists the register settings that affect performance.

Table 9-7. Performance Parameters

Parameter	Comments
FD_DCOND[1:0] MIN	Sets the minimum face size. The permitted values are 20x20, 25x25, 32x32, and 40x40. A high value leads to higher performance.
FD_DCOND[3:2] DIR	Sets the detection direction setting. The permitted values are UP, RIGHT, and LEFT. The UP value should lead to better performance than RIGHT and LEFT.
FD_LHIT[3:0] LHIT	Sets the detection threshold. The permitted values are in the range of 0 to 9. A low value increases the FD probability detection, but it also increases false detections.

9.3.7 L3 Interconnect Parameters

The FDIF is an initiator on the L3 interconnect. L3 accesses can be configured with the FDIF_CTRL[4:1] MAX_TAGS bit field and the FDIF_CTRL[0] WRNP bit. For more information about these parameters, see Section 13.2 *L3 interconnect*.

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9.4 FDIF Programming Guide

9.4.1 FDIF Low-level Programming Models

This section describes the low-level hardware programming sequences for the configuration and use of the FDIF.

9.4.1.1 Global Initialization

9.4.1.1.1 Surrounding Modules Global Initialization

This section identifies the requirements for initializing the surrounding modules when the FDIF is to be used for the first time after a device reset. This initialization of the surrounding modules is based on the integration of the FDIF.

For more information, see Section 9.2, *FDIF Integration*.

Table 9-8. Global Initialization of Surrounding Modules

Surrounding Modules	Comments
PRCM	FDIF_FCLK functional clock must be enabled. See , *CD_CAM Clock Domain*, in Chapter 3, *Power, Reset, and Clock Management*.
Cortex-A9 MPU interrupt controller (INTC) (or Cortex-M3 MPU INTC or DSP INTC)	The Cortex-A9 MPU (or Cortex-M3 MPU or DSP) interrupt controller must be configured to enable the interrupt request generation to the Cortex-A9 MPU (or Cortex-M3 MPU or DSP) subsystem when interrupt requests are generated by the FDIF. See the respective Functional Description in Chapter 17, *Interrupt Controller*, for the MPUs Section 17.4.1, Section 17.4.2, and the DSP interrupt request lines in Chapter 5, *DSP Subsystem*, for the DSP.
Interconnect (L3 and L4)	For more information, see Section 13.2, *L3 Interconnect*, and Section 13.3, *L4 Interconnect*.

9.4.1.1.2 FDIF Global Initialization

9.4.1.1.2.1 Main Sequence – FDIF Global Initialization

Table 9-9 lists the procedure to initialize the FDIF after a power-on or software reset.

Table 9-9. FDIF Global Initialization

Step	Register/Bit Field/Programming Model	Value
Perform a software reset.	FDIF_SYSCONFIG[0] SOFTRESET	0x1
Wait until reset is finished.	FDIF_SYSCONFIG[0] SOFTRESET	0x0
Set the maximum interconnect tags.	FDIF_CTRL[4:1] MAX_TAGS	0xA
Enable ERROR type Interrupt.	FDIF_IRQENABLE_SET_j[0] ERR_IRQ	0x1

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9.4.1.2 FD Operational Modes Configuration

9.4.1.2.1 FD Processing Modes

9.4.1.2.1.1 Main Sequence – FDIF Polling Method

Step	Register/Bit Field/Programming Model	Value
Set image parameters.	See Section 9.4.1.2.1.3, *Subsequence – Set Image Parameters*.	
Request the processing.	FD_CTRL[1] RUN	0x1
Wait until process is finished.	FD_CTRL[2] FINISH	0x1
Read the results.	See Section 9.4.1.2.1.4	

9.4.1.2.1.2 Main Sequence – FDIF Interrupt Method

Step	Register/Bit Field/Programming Model	Value
Set image parameters.	See Section 9.4.1.2.1.3, *Subsequence – Set Image Parameters*.	
Enable FINISH type interrupt.	FDIF_IRQENABLE_SET_j[8] FINISH IRQ	0x1
Request the processing.	FD_CTRL[1] RUN	0x1

WHEN INTERRUPT OCCURS:

Step	Register/Bit Field/Programming Model	Value
IF: This is FD Process Complete Event?	FDIF_IRQSTATUS_j[8] FINISH_IRQ	0x1
Clear (Disable) FINISH type interrupt.	FDIF_IRQENABLE_CLR_j[8] FINISH IRQ	0x1
Read the results	See Section 9.4.1.2.1.4, *Subsequence – Read the Results*.	
ELSE		
Clear (Disable) ERROR type Interrupt.	FDIF_IRQENABLE_CLR_j[0] ERR_IRQ	0x1
Perform a software reset.	FDIF_SYSCONFIG[0] SOFTRESET	0x1
For possible errors and the explanations of them, see Chapter 13, *Interconnect*.		
ENDIF		

9.4.1.2.1.3 Subsequence – Set Image Parameters

Step	Register/Bit Field/Programming Model	Value
Set input image 32-bit address.	FDIF_PICADDR[31:5] ADDR	0x----
Set working memory 32-bit address.	FDIF_WKADDR[31:5] ADDR	0x----
Set the minimum face size.	FD_DCOND[1:0] MIN	0x-
Set the face direction.	FD_DCOND[3:2] DIR	0x-
Set the horizontal start position of the detection area.	FD_STARTX[7:0] STARTX	0x-
Set the vertical start position of the detection area.	FD_STARTY[6:0] STARTY	0x-
Set the horizontal start size of the detection area.	FD_SIZEX[8:0] SIZEX	0x–
Set the vertical start size of the detection area.	FD_SIZEY[7:0] SIZEY	0x-
Set the detection threshold.	FD_LHIT[3:0] LHIT	0x-

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9.4.1.2.1.4 Subsequence – Read the Results

Step	Register/Bit Field/Programming Model	Value
Read the number of found faces	FD_DNUM[5:0] DNUM	0x-
For each face detected, read the following parameters by processing loop until FD_DNUM[5:0] DNUM = 0:		
For each face read X_i coordinate	FD_CENTERX_i[8:0] CENTERX	0x–
For each face read Y_i coordinate	FD_CENTERY_i[7:0] CENTERY	0x-
For each face read confidence level	FD_CONFSIZE_i[11:8] CONF	0x-
For each face read size_i	FD_CONFSIZE_i[7:0] SIZE	0x-
For each face read the angle	FD_ANGLE_i[8:0] ANGLE	0x-

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9.5 FDIF Register Manual

9.5.1 FDIF Instance Summary

Table 9-10 is the FDIF instance.

Table 9-10. FDIF Instance Summary

Module Name	Base Address	Size
FDIF	0x4A10 A000	4 KB

9.5.2 FDIF Registers

Table 9-11 summarizes the FDIF register mapping. Table 9-12 through Table 9-54 describe the register bits.

9.5.2.1 FDIF Register Summary

Table 9-11. FDIF Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	FDIF L4 Base Address
FDIF_REVISION	R	32	0x0000 0000	0x4A10 A000
FDIF_HWINFO	R	32	0x0000 0004	0x4A10 A004
FDIF_SYSCONFIG	RW	32	0x0000 0010	0x4A10 A010
RESERVED	R	32	0x0000 0020	0x4A10 A020
FDIF_IRQSTATUS_RAW_j (1)	RW	32	0x0000 0024 + (0x10 * j)	0x4A10 A024 + (0x10 * j)
FDIF_IRQSTATUS_j (1)	RW	32	0x0000 0028 + (0x10 * j)	0x4A10 A028 + (0x10 * j)
FDIF_IRQENABLE_SET_j (1)	RW	32	0x0000 002C + (0x10 * j)	0x4A10 A02C + (0x10 * j)
FDIF_IRQENABLE_CLR_j (1)	RW	32	0x0000 0030 + (0x10 * j)	0x4A10 A030 + (0x10 * j)
FDIF_PICADDR	RW	32	0x0000 0060	0x4A10 A060
FDIF_CTRL	RW	32	0x0000 0064	0x4A10 A064
FDIF_WKADDR	RW	32	0x0000 0068	0x4A10 A068
FD_CTRL	RW	32	0x0000 0080	0x4A10 A080
FD_DNUM	R	32	0x0000 0084	0x4A10 A084
FD_DCOND	RW	32	0x0000 0088	0x4A10 A088
FD_STARTX	RW	32	0x0000 008C	0x4A10 A08C
FD_STARTY	RW	32	0x0000 0090	0x4A10 A090
FD_SIZEX	RW	32	0x0000 0094	0x4A10 A094
FD_SIZEY	RW	32	0x0000 0098	0x4A10 A098
FD_LHIT	RW	32	0x0000 009C	0x4A10 A09C
FD_CENTERX_i (2)	R	32	0x0000 0160 + (0x10 * i)	0x4A10 A160 + (0x10 * i)
FD_CENTERY_i (2)	R	32	0x0000 0164 + (0x10 * i)	0x4A10 A164 + (0x10 * i)
FD_CONFSIZE_i (2)	R	32	0x0000 0168 + (0x10 * i)	0x4A10 A168 + (0x10 * i)
FD_ANGLE_i (2)	R	32	0x0000 016C + (0x10 * i)	0x4A10 A16C + (0x10 * i)

(1) j = 0 to 2
(2) i = 0 to 34

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9.5.2.2 FDIF Register Description

Table 9-12. FDIF_REVISION

Address Offset	0x0000 0000		
Physical Address	0x4A10 A000	**Instance**	FDIF
Description	IP Revision Identifier (X.Y.R) Used by software to track features, bugs, and compatibility		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP Revision number	R	0x---- ---- TI Internal Data

Table 9-13. Register Call Summary for Register FDIF_REVISION

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- FDIF Register Summary: [0]

Table 9-14. FDIF_HWINFO

Address Offset	0x0000 0004		
Physical Address	0x4A10 A004	**Instance**	FDIF
Description	Information about the IP module's hardware configuration, that is, typically the module's HDL generics (if any). Actual field format and encoding is up to the module's designer to decide.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												FDIF_TAGS			

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved	R	0x0000000
3:0	FDIF_TAGS	Hardware design value. This bit field reflects the value of the FDIF_TAG generic parameter. 0x0: 1 tag supported 0x1: 2 tags supported [...] 0xF: 16 tags supported	R	0xF

Table 9-15. Register Call Summary for Register FDIF_HWINFO

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- FDIF Register Summary: [0]

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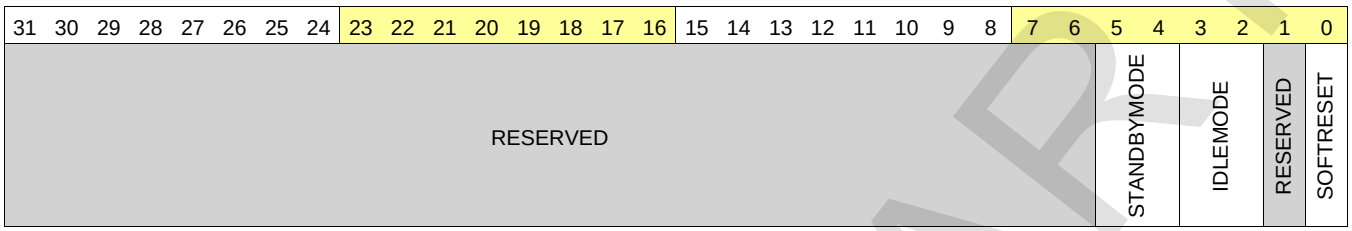
Table 9-16. FDIF_SYSCONFIG

Address Offset	0x0000 0010		
Physical Address	0x4A10 A010	**Instance**	FDIF
Description	Clock management configuration		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:6	RESERVED	Reserved	R	0x0000000
5:4	STANDBYMODE	Configuration of the local initiator state management mode. By definition, initiator may generate read/write transaction as long as it is out of STANDBY state. 0x0: Force-standby mode: local initiator is unconditionally placed in standby state. Backup mode, for debug only. 0x1: No-standby mode: local initiator is unconditionally placed out of standby state. Backup mode, for debug only. 0x2: Smart-standby mode: local initiator standby status depends on local conditions, that is, the module's functional requirement from the initiator. IP module shall not generate (initiator-related) wake-up events. 0x3: Reserved	RW	0x2
3:2	IDLEMODE	Configuration of the local target state management mode. By definition, target can handle read/write transaction as long as it is out of IDLE state. 0x0: Force-idle mode: local target's idle state follows (acknowledges) the system's idle requests unconditionally, that is, regardless of the IP module's internal requirements. Backup mode, for debug only. 0x1: No-idle mode: local target never enters idle state. Backup mode, for debug only. 0x2: Smart-idle mode: local target's idle state eventually follows (acknowledges) the system's idle requests, depending on the IP module's internal requirements. IP module shall not generate (IRQ- or DMA-request-related) wake-up events. 0x3: Reserved	RW	0x2
1	RESERVED	Reserved	R	0
0	SOFTRESET	Software reset. Read 0x0: Reset done, no pending action Write 0x0: No action Write 0x1: Initiate software reset Read 0x1: Reset (software or other) ongoing	RW	0

Table 9-17. Register Call Summary for Register FDIF_SYSCONFIG

FDIF Functional Description

- Software Reset: [0] [1]
- System Power Management: [2] [3]
- Protocol Transitions: [4]

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Table 9-17. Register Call Summary for Register FDIF_SYSCONFIG (continued)

FDIF Programming Guide • FDIF Global Initialization: [5] [6] • FD Processing Modes: [7]
FDIF Register Manual • FDIF Register Summary: [8] • FDIF Register Description: [9]

Table 9-18. FDIF_IRQSTATUS_RAW_j

Address Offset	0x0000 0024 + (0x10 * j)		
Physical Address	0x4A10 A024 + (0x10 * j)	**Instance**	FDIF
Description	Per-event raw interrupt status vector, line #n. Raw status is set even if event is not enabled. Write 1 to set the (raw) status, mostly for debug.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							FINISH_IRQ	RESERVED							ERR_IRQ

Bits	Field Name	Description	Type	Reset
31:9	RESERVED	Reserved	R	0x000000
8	FINISH_IRQ	Face detection processing done. Write 0x0: No action Read 0x0: No event pending Read 0x1: Event pending Write 0x1: Set event (debug)	RW W1toSet	0
7:1	RESERVED	Reserved	R	0x00
0	ERR_IRQ	Error received by the L3 port. Write 0x0: No action Read 0x0: No event pending Read 0x1: Event pending Write 0x1: Set event (debug)	RW W1toSet	0

Table 9-19. Register Call Summary for Register FDIF_IRQSTATUS_RAW_j

FDIF Functional Description • Protocol Transitions: [0] • Interrupts and Events: [1] [2] [3] [4]
FDIF Register Manual • FDIF Register Summary: [5]

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Table 9-20. FDIF_IRQSTATUS_j

Address Offset	0x0000 0028 + (0x10 * j)		
Physical Address	0x4A10 A028 + (0x10 * j)	**Instance**	FDIF
Description	Per-event "enabled" interrupt status vector, line #n. Enabled status is not set unless event is enabled. Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, that is, even if not enabled).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							FINISH_IRQ	RESERVED							ERR_IRQ

Bits	Field Name	Description	Type	Reset
31:9	RESERVED	Reserved	R	0x000000
8	FINISH_IRQ	Face detection processing done. Write 0x0: No action Read 0x0: No (enabled) event pending Read 0x1: Event pending Write 0x1: Clear (raw) event	RW W1toClr	0
7:1	RESERVED	Reserved	R	0x00
0	ERR_IRQ	Error received by the L3 port. Write 0x0: No action Read 0x0: No (enabled) event pending Read 0x1: Event pending Write 0x1: Clear (raw) event	RW W1toClr	0

Table 9-21. Register Call Summary for Register FDIF_IRQSTATUS_j

FDIF Functional Description
- Interrupts and Events: [0] [1] [2] [3]

FDIF Programming Guide
- FD Processing Modes: [4]

FDIF Register Manual
- FDIF Register Summary: [5]

Table 9-22. FDIF_IRQENABLE_SET_j

Address Offset	0x0000 002C + (0x10 * j)		
Physical Address	0x4A10 A02C + (0x10 * j)	**Instance**	FDIF
Description	Per-event interrupt enable bit vector, line #n. Write 1 to set (enable interrupt). Readout equal to corresponding _CLR register.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							FINISH_IRQ	RESERVED							ERR_IRQ

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Bits	Field Name	Description	Type	Reset
31:9	RESERVED	Reserved	R	0x000000
8	FINISH_IRQ	Face detection processing done. Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW W1toSet	0
7:1	RESERVED	Reserved	R	0x00
0	ERR_IRQ	Error received by the L3 port. Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW W1toSet	0

Table 9-23. Register Call Summary for Register FDIF_IRQENABLE_SET_j

FDIF Functional Description • Interrupts and Events: [0]
FDIF Programming Guide • FDIF Global Initialization: [1] • FD Processing Modes: [2]
FDIF Register Manual • FDIF Register Summary: [3]

Table 9-24. FDIF_IRQENABLE_CLR_j

Address Offset	0x0000 0030 + (0x10 * j)		
Physical Address	0x4A10 A030 + (0x10 * j)	**Instance**	FDIF
Description	Per-event interrupt enable bit vector, line #n. Write 1 to clear (disable interrupt). Readout equal to corresponding _SET register.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							FINISH_IRQ	RESERVED							ERR_IRQ

Bits	Field Name	Description	Type	Reset
31:9	RESERVED	Reserved	R	0x000000
8	FINISH_IRQ	Face detection processing done. Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW W1toClr	0
7:1	RESERVED	Reserved	R	0x00
0	ERR_IRQ	Error received by the L3 port. Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW W1toClr	0

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Table 9-25. Register Call Summary for Register FDIF_IRQENABLE_CLR_j

FDIF Functional Description • Interrupts and Events: [0]
FDIF Programming Guide • FD Processing Modes: [1] [2]
FDIF Register Manual • FDIF Register Summary: [3]

Table 9-26. FDIF_PICADDR

Address Offset	0x0000 0060		
Physical Address	0x4A10 A060	**Instance**	FDIF
Description	Picture data store address		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR																								RESERVED							

Bits	Field Name	Description	Type	Reset
31:5	ADDR	Picture data store address. The 5 least significant bits are forced to 0.	RW	0x0000000
4:0	RESERVED	Read returns 0.	R	0x00

Table 9-27. Register Call Summary for Register FDIF_PICADDR

FDIF Functional Description • Typical Use: [0]
FDIF Programming Guide • FD Processing Modes: [1]
FDIF Register Manual • FDIF Register Summary: [2]

Table 9-28. FDIF_CTRL

Address Offset	0x0000 0064		
Physical Address	0x4A10 A064	**Instance**	FDIF
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								MSTANDBY_HDSHK	MSTANDBY	MAX_TAGS					WRNP

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Bits	Field Name	Description	Type	Reset
31:7	RESERVED	Reserved	R	0x0000000
6	MSTANDBY_HDSHK	MStandby / Wait power management handshaking status bit The power management framework of the FDIF module is based on the handshaking of the MSTANDBY and WAIT signals. When going from a idle to normal power management transition, the software polls for FDIF_CTRL.MSTANDBY_HDSHK = 1 before starting the face detection processing. Read 0x0: Handshaking not completed. Do not initiate traffic on L3. Read 0x1: Handshaking completed. Can safely use the FDIF module.	R	0
5	MSTANDBY	MStandby signal generation. This bit shall be set to initiate a power management transition from NORMAL to IDLE or IDLE to NORMAL. 0x0: Write: Clear MStandby signal. One polls FDIF_CTRL.MSTANDBY_HDSHK = 1 after writing this bit to ensure that the power management handshaking is completed. 0x1: Write: Asserts MStandby signal	RW	1
4:1	MAX_TAGS	Max interconnect tags. This bit field sets the maximum number of interconnect tags that the module shall use. This number is programmable between 1 (MAX_TAGS = 0) and FDIF_TAGS (MAX_TAGS = FDIF_TAGS - 1). The value of MAX_TAGS is reflected in the FIDIF_HWINFO register setting. This register setting is expected to have impact on performance. It shall be set once at initialization. Higher value will give more bandwidth to the initiator. Lower value will give less bandwidth to the initiator. This value shall be set as low as possible such that other system initiators are not penalized.	RW	0xF
0	WRNP	L3 port non-posted write control. Dynamic usage of this feature is not supported. This bit shall be set at initialization and not modified hereafter until the processing is completed. When non-posted writes are used, tags shall be used for best performance (MAX_TAGS 1). 0x0: All writes are non posted 0x1: All writes are posted	RW	0

Table 9-29. Register Call Summary for Register FDIF_CTRL

FDIF Functional Description • Protocol Transitions: [0] [1] [2] • L3 Interconnect Parameters: [3] [4]
FDIF Programming Guide • FDIF Global Initialization: [5]
FDIF Register Manual • FDIF Register Summary: [6] • FDIF Register Description: [7] [8]

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Table 9-30. FDIF_WKADDR

Address Offset	0x0000 0068		
Physical Address	0x4A10 A068	**Instance**	FDIF
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR																								RESERVED							

Bits	Field Name	Description	Type	Reset
31:5	ADDR	Work area address The 5 least significant bits are forced to 0.	RW	0x0000000
4:0	RESERVED	Read returns 0.	R	0x00

Table 9-31. Register Call Summary for Register FDIF_WKADDR

FDIF Functional Description • Typical Use: [0]
FDIF Programming Guide • FD Processing Modes: [1]
FDIF Register Manual • FDIF Register Summary: [2]

Table 9-32. FD_CTRL

Address Offset	0x0000 0080		
Physical Address	0x4A10 A080	**Instance**	FDIF
Description	Control register Don't set more than 2 bits to "1" at the same time. Otherwise, operations cannot be guaranteed.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													FINISH	RUN	SRST

Bits	Field Name	Description	Type	Reset
31:3	RESERVED	Reserved	R	0x0000 0000
2	FINISH	Process Completion Flag Clear 0x0: Write: Disable Read: Process incomplete 0x1: Write: Process complete flag clear Read: Process complete	RW	0
1	RUN	Process Start Request 0x0: Write: Disable Read: No processing 0x1: Write: Process start request Read: Processing data	RW	0
0	SRST	Software Reset This bit shall not be used to reset the FDIF module. Instead, the FDIF_SYSCONFIG[0] SOFTRESET bit shall be used for complete soft reset. 0x0: Write: Disable Read: Reset cancel 0x1: Write: Reset Read: Under reset	RW	0

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Table 9-33. Register Call Summary for Register FD_CTRL

FDIF Functional Description • Software Reset: [0] • Protocol Transitions: [1] • Typical Use: [2] [3]
FDIF Programming Guide • FD Processing Modes: [4] [5] [6]
FDIF Register Manual • FDIF Register Summary: [7]

Table 9-34. FD_DNUM

Address Offset	0x0000 0084		
Physical Address	0x4A10 A084	**Instance**	FDIF
Description	Face Detection Result Count Register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								DNUM							

Bits	Field Name	Description	Type	Reset
31:6	RESERVED	Reserved	R	0x0000000
5:0	DNUM	Face detection result count. Up to 35 faces can be detected. Number of face(s) detected: 0x0: 0 face detected 0x1: 1 face detected 0x2: 2 faces detected [...] 0x23: 35 faces detected 0x24 to 0x3F: unused	R	0x00

Table 9-35. Register Call Summary for Register FD_DNUM

FDIF Functional Description • Typical Use: [0]
FDIF Programming Guide • FD Processing Modes: [1] [2]
FDIF Register Manual • FDIF Register Summary: [3]

Table 9-36. FD_DCOND

Address Offset	0x0000 0088		
Physical Address	0x4A10 A088	**Instance**	FDIF
Description	Detection Condition Setting Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												DIR		MIN	

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Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved	R	0x0000000
3:2	DIR	Detection direction setting 0x0: Executes only for UP 0x1: Executes only for RIGHT 0x2: Executes only for LEFT 0x3: Reserved	RW	0x0
1:0	MIN	Reserved 0x0: Set the min face size to 20 pixels 0x1: Set the min face size to 25 pixels 0x2: Set the min face size to 32 pixels 0x3: Set the min face size to 40 pixels	RW	0x0

Table 9-37. Register Call Summary for Register FD_DCOND

FDIF Functional Description • Typical Use: [0] • Performance Parameters: [1] [2]
FDIF Programming Guide • FD Processing Modes: [3] [4]
FDIF Register Manual • FDIF Register Summary: [5]

Table 9-38. FD_STARTX

Address Offset	0x0000 008C		
Physical Address	0x4A10 A08C	**Instance**	FDIF
Description	Detection Area Setting Register: X Start Coordinate.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								STARTX							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Reserved	R	0x000000
7:0	STARTX	Starting X coordinates Permitted values are 0=STARTX=160	RW	0x00

Table 9-39. Register Call Summary for Register FD_STARTX

FDIF Functional Description • Typical Use: [0]
FDIF Programming Guide • FD Processing Modes: [1]
FDIF Register Manual • FDIF Register Summary: [2]

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Table 9-40. FD_STARTY

Address Offset	0x0000 0090		
Physical Address	0x4A10 A090	**Instance**	FDIF
Description	Detection Area Setting Register: Y Start Coordinate.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								STARTY							

Bits	Field Name	Description	Type	Reset
31:7	RESERVED	Reserved	R	0x0000000
6:0	STARTY	Starting Y coordinates Permitted values are 0=STARTY=120	RW	0x00

Table 9-41. Register Call Summary for Register FD_STARTY

FDIF Functional Description • Typical Use: [0] [1]
FDIF Programming Guide • FD Processing Modes: [2]
FDIF Register Manual • FDIF Register Summary: [3]

Table 9-42. FD_SIZEX

Address Offset	0x0000 0094		
Physical Address	0x4A10 A094	**Instance**	FDIF
Description	Detection Area Setting Register: X Direction Size		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								SIZEX							

Bits	Field Name	Description	Type	Reset
31:9	RESERVED	Reserved	R	0x000000
8:0	SIZEX	X Direction Size	RW	0x140

Table 9-43. Register Call Summary for Register FD_SIZEX

FDIF Functional Description • Typical Use: [0]
FDIF Programming Guide • FD Processing Modes: [1]
FDIF Register Manual • FDIF Register Summary: [2]

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Table 9-44. FD_SIZEY

Address Offset	0x0000 0098		
Physical Address	0x4A10 A098	**Instance**	FDIF
Description	Detection Area Setting Register: Y Direction Size		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								SIZEY							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Reserved	R	0x000000
7:0	SIZEY	Y Direction Size	RW	0xF0

Table 9-45. Register Call Summary for Register FD_SIZEY

FDIF Programming Guide • FD Processing Modes: [0]
FDIF Register Manual • FDIF Register Summary: [1]

Table 9-46. FD_LHIT

Address Offset	0x0000 009C		
Physical Address	0x4A10 A09C	**Instance**	FDIF
Description	Threshold Setting Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												LHIT			

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved	R	0x0000000
3:0	LHIT	Threshold Permitted values are 0x0 to 0x9	RW	0x5

Table 9-47. Register Call Summary for Register FD_LHIT

FDIF Functional Description • Performance Parameters: [0]
FDIF Programming Guide • FD Processing Modes: [1]
FDIF Register Manual • FDIF Register Summary: [2]

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Table 9-48. FD_CENTERX_i

Address Offset	0x0000 0160 + (0x10 * i)		
Physical Address	0x4A10 A160 + (0x10 * i)	**Instance**	FDIF
Description	Detection Result: X Coordinate. Its value is undefined after reset.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								CENTERX							

Bits	Field Name	Description	Type	Reset
31:9	RESERVED	Reserved. Read returns reset value.	R	0x–
8:0	CENTERX	Face position: center X coordinate The coordinates given by (FD_CENTERX_i, FD_CENTERY_i) give the central coordinates of the face position. Permitted values are 0x0 to 0x13F	R	0x–

Table 9-49. Register Call Summary for Register FD_CENTERX_i

FDIF Functional Description • Typical Use: [0]
FDIF Programming Guide • FD Processing Modes: [1]
FDIF Register Manual • FDIF Register Summary: [2] • FDIF Register Description: [3] [4]

Table 9-50. FD_CENTERY_i

Address Offset	0x0000 0164 + (0x10 * i)		
Physical Address	0x4A10 A164 + (0x10 * i)	**Instance**	FDIF
Description	Detection Result: Y Coordinate. Its value is undefined after reset.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								CENTERY							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Reserved. Read returns reset value.	R	0x–
7:0	CENTERY	Face position: center Y coordinate The coordinates given by (FD_CENTERX_i, FD_CENTERY_i) give the central coordinates of the face position. Permitted values are 0x0 to 0xEF	R	0x–

Table 9-51. Register Call Summary for Register FD_CENTERY_i

FDIF Functional Description • Typical Use: [0]
FDIF Programming Guide • FD Processing Modes: [1]
FDIF Register Manual • FDIF Register Summary: [2] • FDIF Register Description: [3] [4]

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Table 9-52. FD_CONFSIZE_i

Address Offset	0x0000 0168 + (0x10 * i)		
Physical Address	0x4A10 A168 + (0x10 * i)	**Instance**	FDIF
Description	Detection Result: Confidence Level and Size. Its value is undefined after reset.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				CONF				SIZE							

Bits	Field Name	Description	Type	Reset
31:12	RESERVED	Reserved. Read returns reset value.	R	0x-
11:8	CONF	Confidence level Permitted values are 0x0 (high) to 0x9 (low)	R	0x-
7:0	SIZE	Detection result face size Permitted values 0x14 to 0xF0	R	0x–

Table 9-53. Register Call Summary for Register FD_CONFSIZE_i

FDIF Functional Description • Typical Use: [0]
FDIF Programming Guide • FD Processing Modes: [1] [2]
FDIF Register Manual • FDIF Register Summary: [3]

Table 9-54. FD_ANGLE_i

Address Offset	0x0000 016C + (0x10 * i)		
Physical Address	0x4A10 A16C + (0x10 * i)	**Instance**	FDIF
Description	Detection Result: Angle. Its value is undefined after reset.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								ANGLE							

Bits	Field Name	Description	Type	Reset
31:9	RESERVED	Reserved. Read returns reset value.	R	0x-
8:0	ANGLE	Detection result face angle Permitted values: When DIR = 0: 0x0 (0 deg) to 0x1E (30 deg) and 0x14A (330 deg) to 0x167 (359 deg) When DIR = 1: 0x03C (60 deg) to 0x078 (120 deg) When DIR = 2: 0x0F0 (240 deg) to 0x12C (300 deg)	R	0x–

Table 9-55. Register Call Summary for Register FD_ANGLE_i

FDIF Functional Description • Typical Use: [0]
FDIF Programming Guide • FD Processing Modes: [1]
FDIF Register Manual • FDIF Register Summary: [2]

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Display Subsystem

This chapter describes the display subsystem (DSS) for the device.

Topic **Page**

10.1 Display Subsystem Overview 2136
10.2 Display Controller 2158
10.3 MIPI Display Serial Interface 2404
10.4 High-Definition Multimedia Interface 2597
10.5 Remote Frame Buffer Interface 2600
10.6 Video Encoder 2647

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10.1 Display Subsystem Overview

The display subsystem (DSS) provides the logic to display a video frame from the memory frame buffer on a liquid-crystal display (LCD) panel or a TV set.

The DSS can display different pictures simultaneously by using the primary LCD1 and secondary LCD2 outputs, in addition to the TV output.

The primary LCD output can be one of the following:

- Display serial interface (DSI) (MIPI® DSI)
- Remote frame buffer interface (RFBI) (MIPI DBI 2.0)

The secondary LCD output can be one of the following:

- Parallel CMOS output (MIPI DPI 1.0)
- DSI (MIPI DSI)
- RFBI (MIPI DBI 2.0)

The TV output can be one of the following:

- Composite signal
- High-definition multimedia interface (HDMI)

The modules integrated in the DSS are:

- Display controller (DISPC):
  - One direct memory access (DMA) engine
  - Two LCD outputs and one TV output, each one with a dedicated overlay manager
  - One graphics pipeline (GFX), three video pipelines, and one write-back pipeline
- RFBI:
  - 8-, 9-, 16-bit parallel interface
  - Programmable pixel memory formats
  - Programmable output formats on one or multiple cycles per pixel
- Two DSI protocol engines:
  - 4-data lane complex input/output (I/O) for DSI1 and 2-data lane complex I/O for DSI2
  - Bidirectional data link support (only one data lane is used in reverse direction in command mode)
  - Supports video mode and command mode
  - Supports data interleaving
- NTSC/PAL video encoder (VENC):
  - Composite output signal through external video digital-to-analog converter (DAC)

NOTE: The video DAC (VDAC) function is not supported.

- HDMI protocol engine:
  - Supports HDMI 1.3 (including HDMI 1.4 3D frame-packing support up to 1080p, 24 Hz)
  - 30-bit RGB color
  - HDCP key protection
  - Deep color mode support (10-bit for 1080p and up to 12-bit for 1080i/720p)

The necessary phase-locked loops (PLLs) with their control modules and the physical layers (PHYs) are outside the DSS. The PHYs can be:

- HDMI-PHY
- VDAC
- DSI-PHY

To ensure efficient bandwidth, the DSS integrates:

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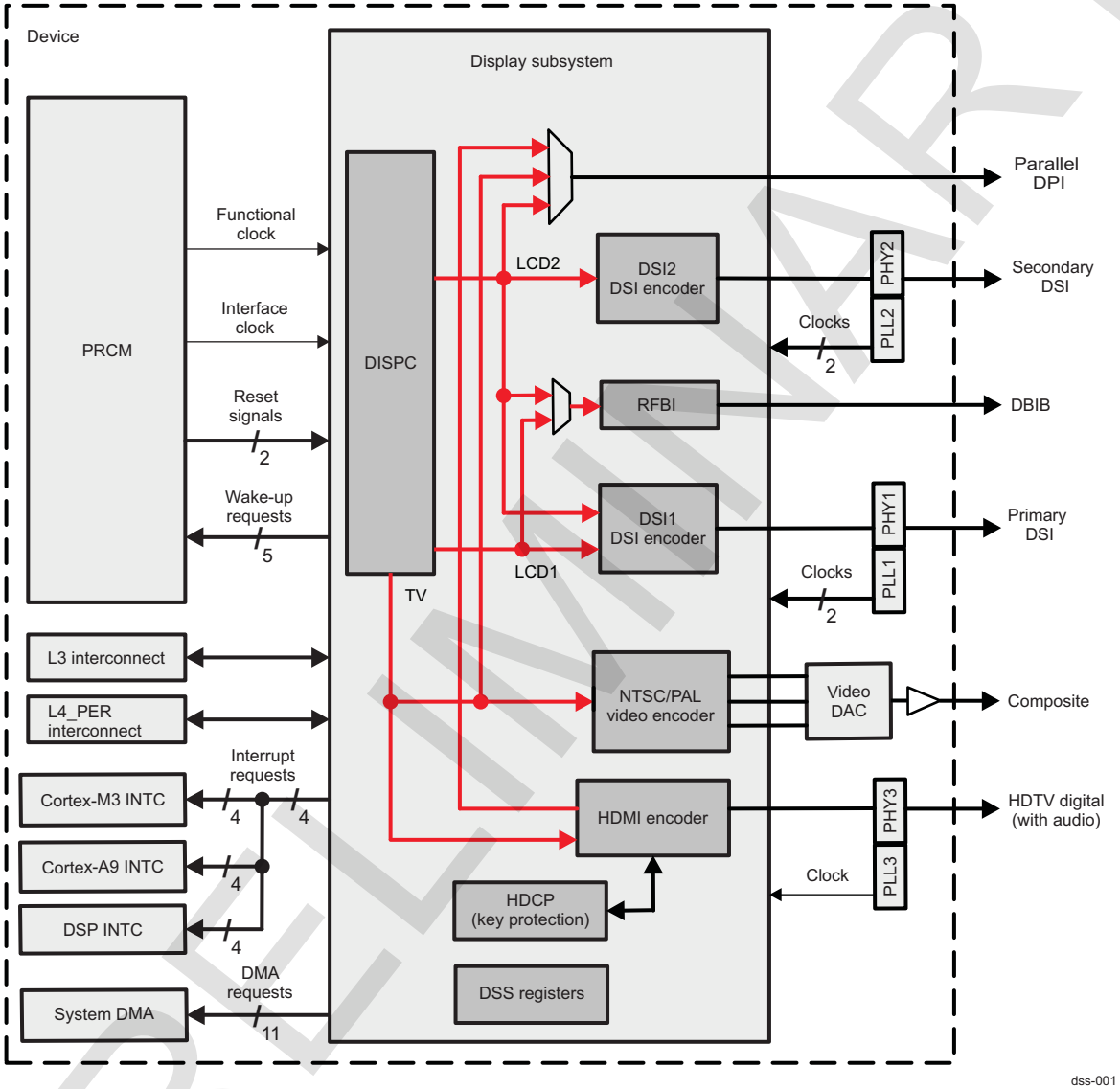
- Local 32-bit interconnect with a level 4 (L4_PER) connection to configure the DSS modules
- Connection between level 3 (L3) interconnect and the DISPC to exchange data with synchronous dynamic random access memory (SDRAM) and memory using the DISPC DMA engine

Figure 10-1 is a high-level diagram of the DSS.

Figure 10-1. DSS Overview



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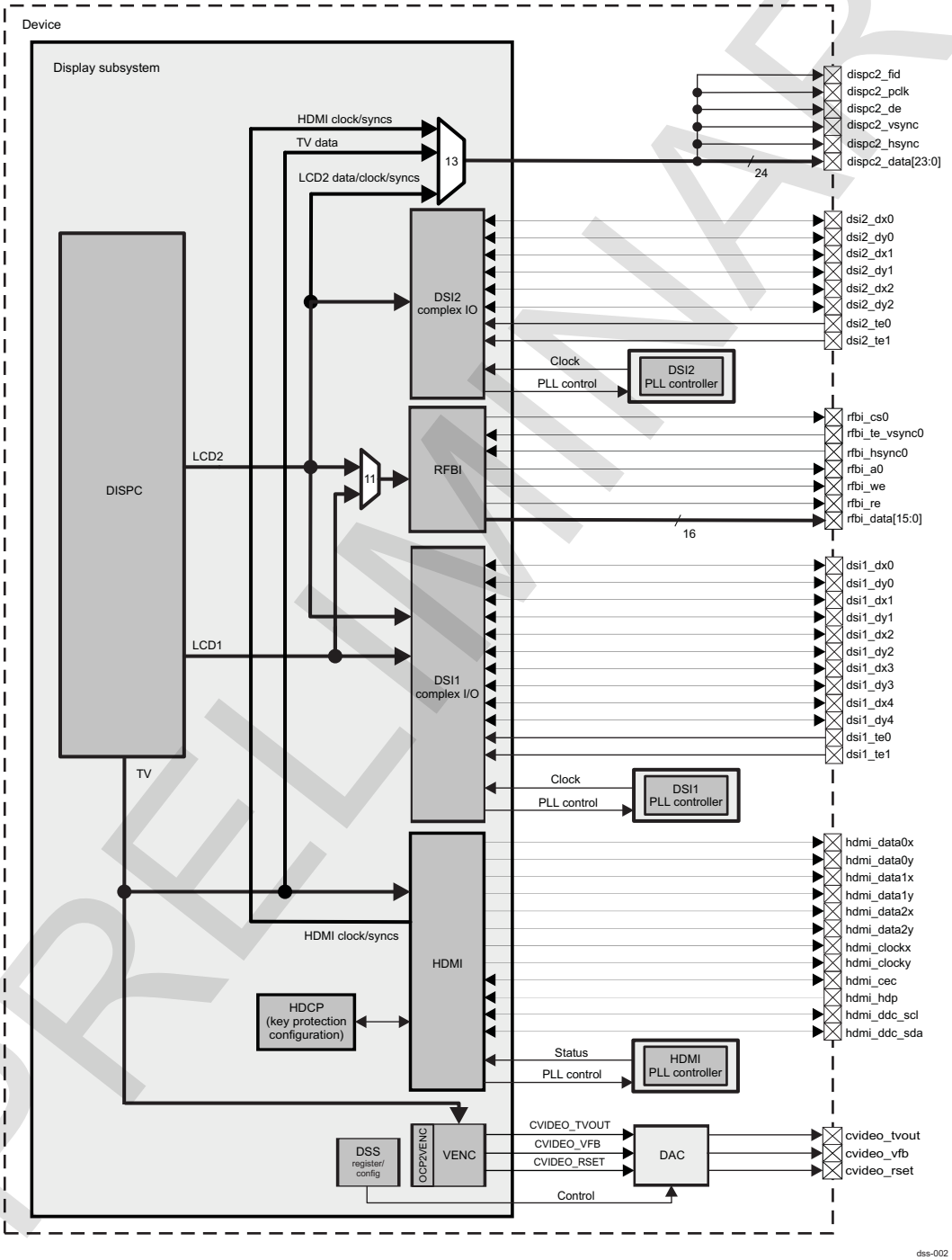
10.1.1 DSS Environment

This section describes the various outputs handled by the DSS:

- LCD support
- TV display support

Figure 10-2 is a diagram of the DSS environment.

Figure 10-2. DSS Environment



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10.1.1.1 DSS LCD Support

LCD panels must be connected to the DSS of the device using parallel and/or serial interfaces. Two modes are supported in parallel:

- DBIB
- Display parallel interface (DPI)

10.1.1.1.1 Parallel Interface

In parallel interface, the modules of the DSS path are the DISPC and the RFBI.

The DISPC is connected to the memory through the L3 interconnect and uses its own DMA (with embedded FIFO) to read data from the system memory.

The remote frame buffer (RFB) of the LCD panel is connected directly to the RFBI module of the device. The RFBI controls the reads/writes from/to the RFB. The RFBI receives the output data from the DISPC and generates the signals to control the LCD panel. Through the RFBI, the microprocessor unit (MPU) can send commands or parameter/display data to the LCD panel and directly set the DISPC registers to read/write the data from/to the memory in the LCD panel.

The RFBI can be connected to either of the DISPC LCD outputs, but only one at a time can be used. The selection (multiplexer 11 in Figure 10-2) is done through the DSS_CTRL[14] RFBI_SWITCH bit. It is not allowed to change the configuration, when the DISPC or RFBI modules are active.

For more details, see Section 10.2, *Display Controller*, and Section 10.5, *Remote Frame Buffer Interface*.

In synchronous parallel interface, the required data and control signals are provided directly to an external MIPI DPI-compatible parallel panel.
Two configuration options are available, selected through the DSS_CTRL[17] LCD2_TV_SEL bit field (multiplexer 13 in Figure 10-2):

- LCD2_TV_SEL = 0 (default): The LCD2 channel of DISPC (pixel data, clock and synchronization signals) is output on the parallel interface.
- LCD2_TV_SEL = 1: The TV channel of DISPC (pixel data), together with the pixel clock and synchronization signals of HDMI, is output on the parallel interface.

,Table 10-1 lists the exact DSS signals outgoing on the device boundary pads.

Table 10-1. Display Parallel Interface Signals Mapping

Signal names at device pads (See Figure 10-2)	DSS_CTRL[17] LCD2_TV_SEL = 0 DISPC LCD2 channel out (pixel data, clock, syncs)	DSS_CTRL[17] LCD2_TV_SEL = 1 DISPC TV channel out (pixel data) HDMI (pixel clock, syncs)
dispc2_fid	DISPC_LCD2_FID	HDMI_M_FID
dispc2_pclk	DISPC_LCD2_PCLK	HDMI_M_PCLK
dispc2_de	DISPC_LCD2_DE	HDMI_M_DE
dispc2_vsync	DISPC_LCD2_VSYNC	HDMI_M_VS
dispc2_hsync	DISPC_LCD2_HSYNC	HDMI_M_HS
dispc2_data[23:0]	DISPC_LCD2_DATA[23:0]	DISPC_TV_DATA[29:0]

For more details on LCD2 and TV out pixel data formats for the parallel interface, see Section 10.2.2, *Display Controller Environment*.

10.1.1.1.2 Serial Interfaces

In serial interface, the DISPC and the two DSI modules with their associated PLLs are used in the data path. The DISPC is connected to the memory through the L3 interconnect and uses its own DMA to read the data from the system memory.

The DSI module contains a PLL to multiply the pixel clock by an appropriate factor. The resulting serialized data is then transmitted on one to four differential data pairs and an additional clock pair that has a reference transition at the boundary between pixels.

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For more details, see Section 10.3, *MIPI DSI*.

10.1.1.2 DSS TV Display Support

10.1.1.2.1 Video Encoder

In a TV output configuration, the DISPC, the VENC and the associated PLL modules, and the Video DAC are used in the data path. The DISPC receives synchronization signals from the VENC and synchronously sends pixel data to the VENC with these signals. The digital output of the DISPC is always a 24-bit RGB value based on a pixel request from the VENC.

The VENC converts RGB video signals to conform to the NTSC/PAL standard for analog video.

For more details, see Section 10.6, *VENC*.

NOTE: The VDAC function is not supported.

10.1.1.2.2 HDMI

In an HDMI configuration, the DISPC, HDMI, and HDCP modules and the associated PLL modules are used in the data path. The HDMI module converts the RGB video into standard high-definition digital video format. The module has a PLL, which can multiply the pixel clock by an appropriate factor. The data is transmitted on three differential data pairs and an additional clock pair.

For more details, see Section 10.4, *HDMI*.

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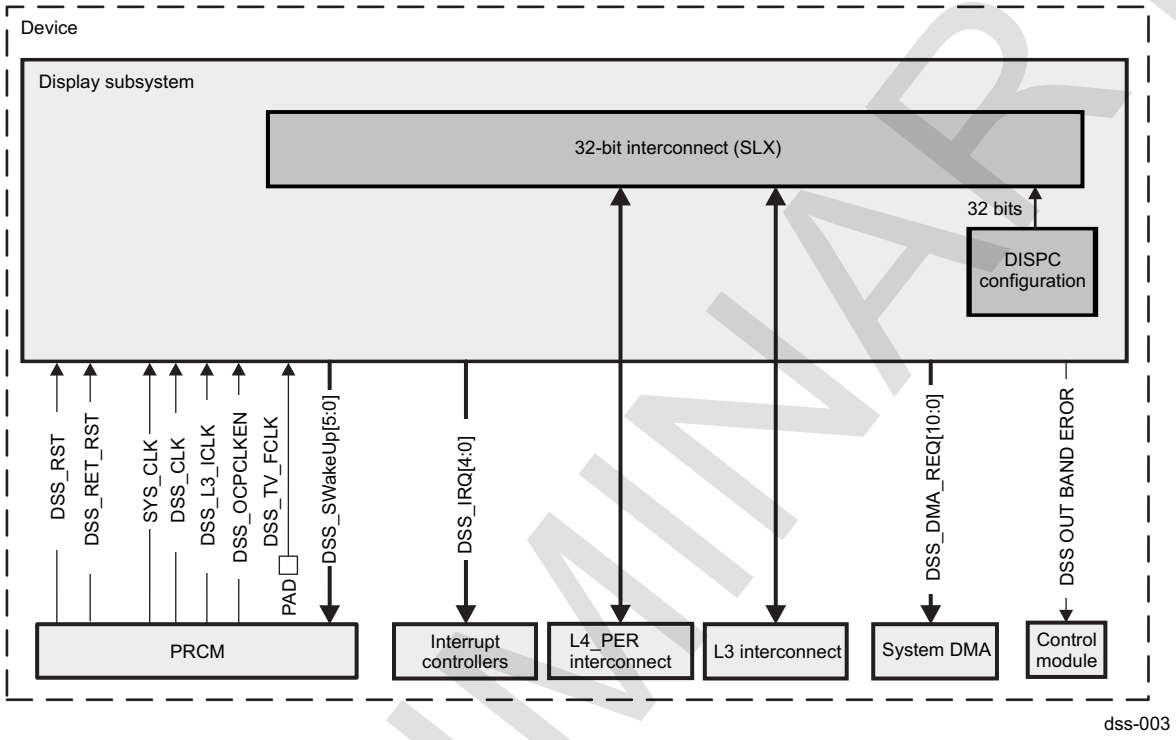
10.1.2 DSS Integration

This section describes the integration of the DSS module in the device, including information about clocks, resets, and hardware requests.

Figure 10-3 shows the integration of the DSS in the device.

Figure 10-3. DSS Integration



10.1.2.1 DSS Clocks

The power, reset, and clock management (PRCM) module provides clock signals to the DSS.

Figure 10-4 shows the details of the DSS clock tree.

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Figure 10-4. DSS Clock Tree

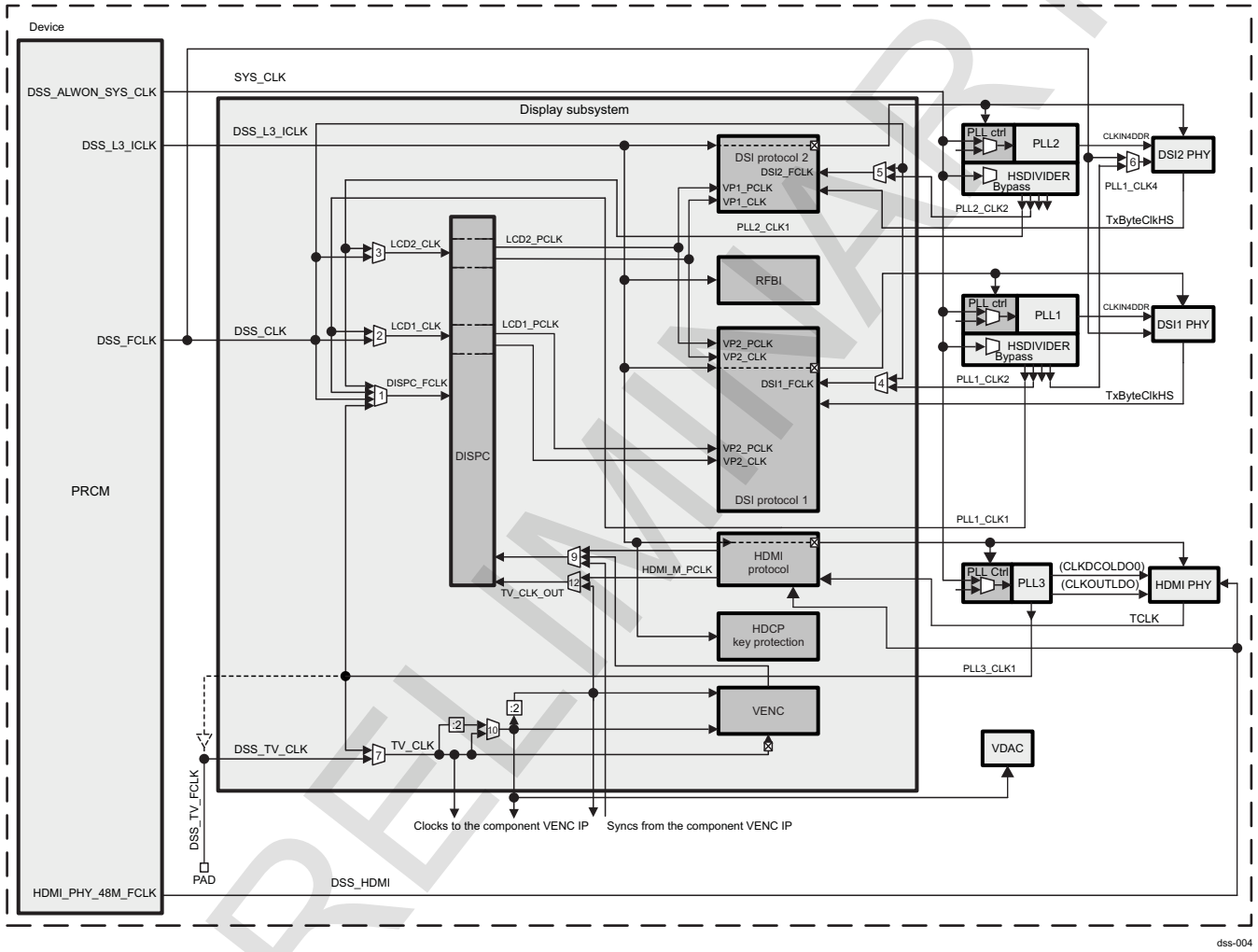

Table 10-2 lists the main DSS clocks and their sources.

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Table 10-2. DSS Clocks

Clocks				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
DSS	DSS_HDMI	HDMI_PHY_48M_FCLK	PRCM module	Functional clock
	DSS_CLK	DSS_FCLK	PRCM module	Functional clock
	SYS_CLK	DSS_ALWON_SYS_CLK	PRCM module	System clock
	DSS_TV_CLK	DSS_TV_FCLK	PAD	TV output interface clock
	DSS_L3_ICLK	DSS_L3_ICLK	PRCM module	Interface clock

- The clock source for the L3 interface clock is DSS_L3_ICLK.
- The clock sources for the DSS modules are listed in Table 10-3.

Table 10-3. DSS Modules Clock Sources

Destination	Source Signal Name	Source	Multiplexer Number	DSS_CTRL Register Bit Field
DISPC functional clock (DISPC_FCLK)	DSS_CLK	PER_PLL	1	[9:8] FCK_CLK_SWITCH
	PLL1_CLK1	PLL1	1	
	PLL2_CLK1	PLL2	1	
	PLL3_CLK1	PLL3	1	
DSI1 functional clock (LCD1_CLK)	DSS_CLK	PER_PLL	2	[0] LCD1_CLK_SWITCH
	PLL1_CLK1	PLL1	2	
DSI2 functional clock (LCD2_CLK)	DSS_CLK	PER_PLL	3	[12] LCD2_CLK_SWITCH
	PLL2_CLK1	PLL2	3	
DSI1 protocol engine functional clock (DSI1_FCLK)	DSS_CLK	PER_PLL	4	[1] DSI1_CLK_SWITCH
	PLL1_CLK2	PLL1	4	
DSI2 protocol engine functional clock (DSI2_FCLK)	DSS_CLK	PER_PLL	5	[10] DSI2_CLK_SWITCH
	PLL2_CLK2	PLL2	5	
VENC/HDMI functional clock (TV_CLK)	DSS_TV_CLK	PAD	7	[11] TV_CLK_SWITCH
	PLL3_CLK1	PLL3	7	
DISPC external clock (TV_CLK_OUT)	TV_CLK	Multiplexer 7	12	[15] VENC_HDMI_ SWITCH
	HDMI_M_PCLK	HDMI	12	

NOTE: : For more information about the DSI1 and DSI2 video port clocks (VPn_PCLK and VPn_CLK, where n = 1 or 2), see Table 10-4 and Section 10.3.4.2, *DSI Clock Configuration*.

NOTE: Multiplexer 9 in Figure 10-4 has the same control as multiplexer 12 when switched between VENC and HDMI.

Multiplexer 6 in Figure 10-4 allows the DSS_FCLK or PLL1_CLK4 clock to be sent on the DSI2 PHY bypass input. The use of the bypassed clock allows both DSI modules to run on DSS_FCLK or on a single PLL. The selection is done on device control module level. For more information, see Section 10.3.4.2, *DSI Clock Configuration* in Section 10.3, *MIPI Display Serila Interface*.

- VENC clocks generation

  The TV_CLK clock is divided into three balanced clocks, depending on the clock mode selected by the DSS_CTRL[2] VENC_CLOCK_MODE register bit. For more details on clock modes configuration see Section 10.6.3, *Video Encoder Integration*.

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Table 10-4 lists the maximum frequencies of various DSS clocks for OPP100 and OPP50.

Table 10-4. DSS Clock Frequencies

Clock Name	OPP100	OPP50	Notes
DSS_L3_ICLK	200 MHz	100 MHz	For the description and clock source, see Table 10-2.
DSS_CLK	186 MHz	186 MHz	For the description and clock source, see Table 10-2.
DISPC_FCLK	186 MHz	186 MHz	For the description and clock source, see Table 10-3.
DISPC_CORE_CLK	186 MHz	93 MHz	DISPC internal functional clock. Generated from DISPC_CLK after LCD divider at the DISPC module level. For more details, see Section 10.2.4.1, *Clock Configuration*.
LCDn_CLK (n = 1 or 2)	186 MHz	93 MHz	For description and clock source, see Table 10-3.
LCDn_PCLK (n = 1 or 2)	170 MHz	93 MHz	DISPC LCD output pixel clock. Generated from LCDn_CLK after two dividers (LCDn and PCDn) at the DISPC module level. For more details, see Section 10.2.4.1, *Clock Configuration*.
VPn_PCLK (n = 1 or 2)	148.5 MHz	74.25 MHz	DSI video port pixel clock. Sourced from LCDn_PCLK.
VPn_CLK (n = 1 or 2)	186 MHz	93 MHz	DSI video port clock. Generated from LCDn_CLK after a divider (LCDn) at DISPC module level. For more details, see Section 10.2.4.1, *Clock Configuration*.
DSIn_FCLK (n = 1 or 2)	170 MHz	93 MHz	For the description and clock source, see Table 10-3.
TV_CLK	59 MHz	59 MHz	For the description and clock source, see Table 10-3.
DSS_TV_CLK	59 MHz	59 MHz	DSS_TV_CLK from PAD
DSS_HDMI_TCLK	185.625 MHz	92.8125 MHz	TMDS clock from the HDMI PHY. For the clock source, see Figure 10-4.
TXCLKESC	20 MHz	20 MHz	DSI escape-mode transmit clock. For more details, see Section 10.3.4.4.4, *Clock Requirements*.
TXBYTECLKHS	112.5 MHz	103 MHz	DSI high-speed transmit byte clock (generated by the complex I/Os) TXBYTECLKHS = 112.5 MHz for up to three data lanes (900 Mbps per lane); TXBYTECLKHS = 103 MHz for four data lanes (824 Mbps per lane)
DSS_HDMI	48 MHz	48 MHz	For the description and clock source, see Table 10-2.

10.1.2.2 DSS Resets

The PRCM module provides two reset signals to the DSS.

Figure 10-5 shows the details of the reset tree for the DSS.

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Figure 10-5. DSS Reset Scheme

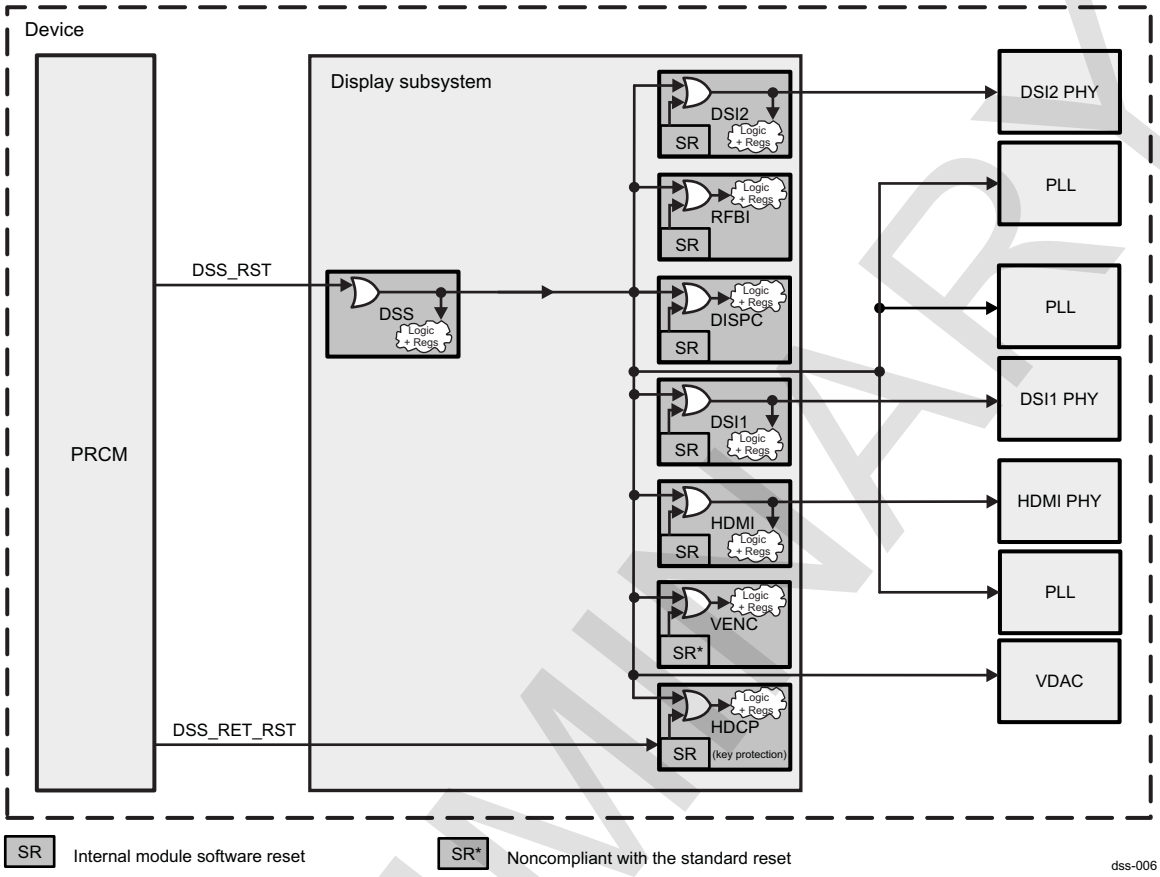

Table 10-5 lists the resets for the DSS.

Table 10-5. DSS Resets

Resets				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
DSS	DISPSS_RET_RST	DSS_RET_RST	PRCM module	Retention reset
	DISPSS_RST	DSS_RST	PRCM module	Nonretention reset

10.1.2.2.1 Hardware Reset

The DSS receives its DISPSS_RST reset signal (the reset signal of the DSS power domain) from the PRCM module. The DISPSS_RET_RST is used only for the HDCP key protection module.

10.1.2.3 DSS Power Management

The DSS modules are in the DSS power domain, except for the dual video DACs, which are in the analog VDDADAC voltage domain.

Table 10-6 lists the DSS power domains.

Table 10-6. DSS Power Domains

Module Instance	Attributes
	Power Domain
Display subsystem	PD_DSS
DISPC	For more details, see Section 10.2, *Display Controller*.

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Table 10-6. DSS Power Domains (continued)

MIPI DSI1	For more details, see Section 10.3, *MIPI Display Serial Interface*.
MIPI DSI2	For more details, see Section 10.3, *MIPI Display Serial Interface*.
RFBI	For more details, see Section 10.5, *Remote Frame Buffer Interface*.
HDMI	For more details, see Section 10.4, *High-Definition Multimedia Interface*.
Video encoder	For more details, see Section 10.6, *Video Encoder*.

10.1.2.3.1 Standby Mode

As part of the system-wide power-management scheme, the DSS supports the MStandby/MWait and SIdleReq/SIdleAck protocols:

- MStandby/MWait
  - DISPC
- SIdleReq/SIdleAck
  - DISPC
  - DSI1
  - DSI2
  - RFBI
  - HDMI
  - HDCP (key protection)
  - VENC
  - DSS interconnect

Figure 10-6 shows the details of the DSS wake-up generation.

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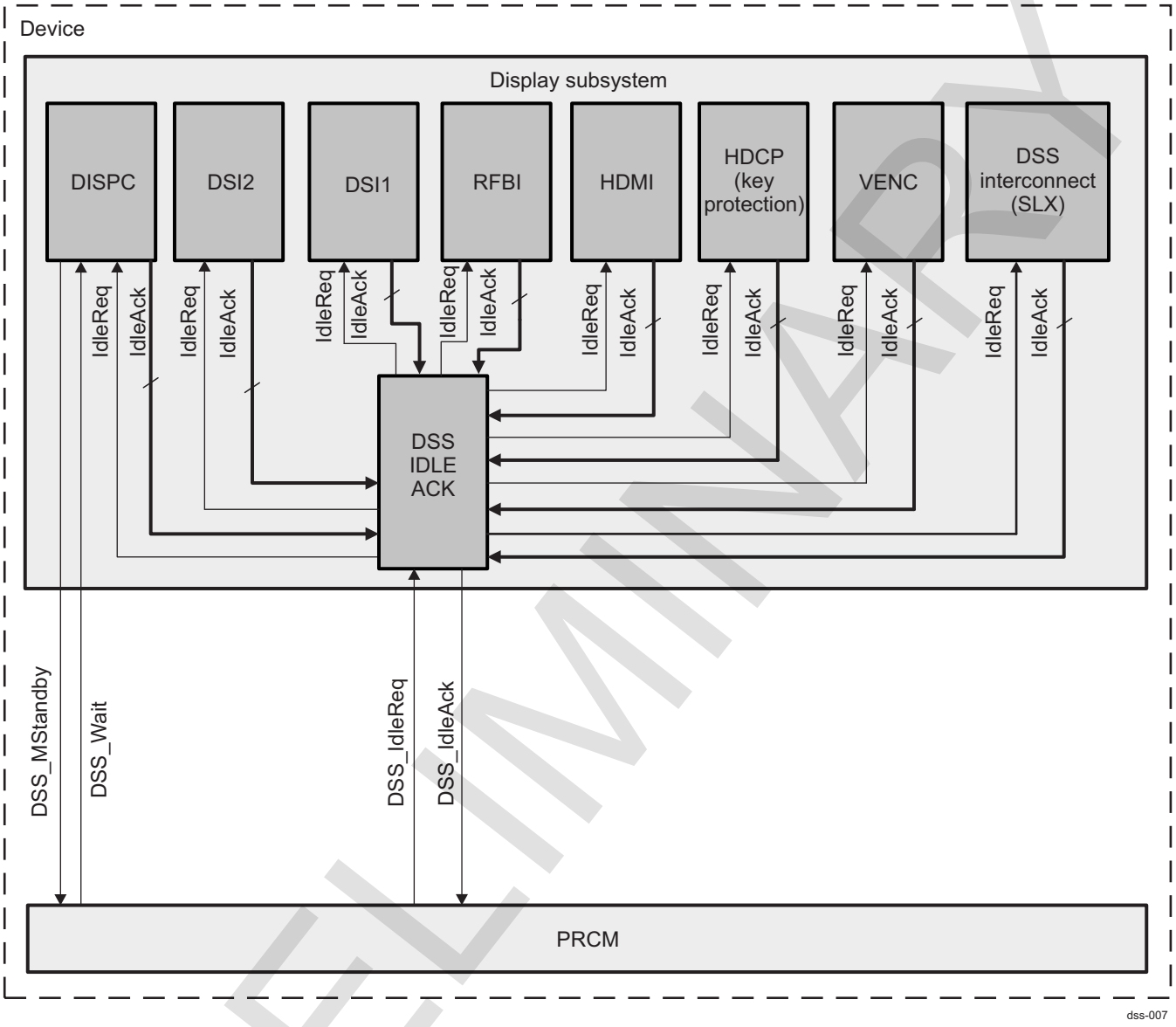
Figure 10-6. DSS SIdleAck/MStandby Generation



10.1.2.3.1.1 Conditions to Exit Standby Mode

For information about the conditions that allow the subsystem to exit standby mode, see Section 10.2, *Display Controller*.

10.1.2.3.1.2 Standby Procedure Description

When the DSS initiates a standby procedure, it also initiates a standby/wait handshake protocol with the PRCM module that lets the PRCM module cut the DSS clocks.

10.1.2.3.2 Wake-Up Mode

The DISPC, DSI1, DSI2, and HDMI modules support the wake-up protocol. DSS_HDMI_SWakeUp is associated with DSS_HMDI_IRQ, which is generated by the HDMI module. For the events that generate an Swakeup and the description and configuration of the registers, see the DISPC, DSI, and HDMI TRM chapters.

Figure 10-7 shows DSS wake-up generation.

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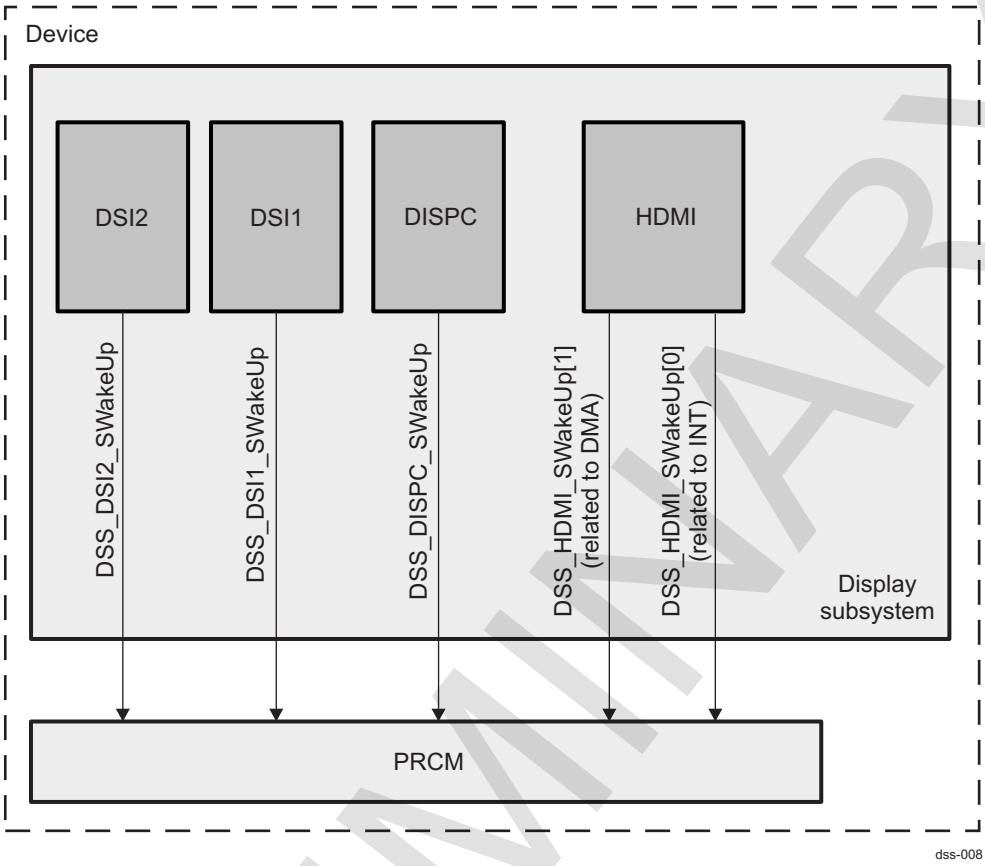
Figure 10-7. DSS Wake-Up Generation



10.1.2.4 DSS Interrupt Requests

The DSS has four interrupt lines. The interrupt signals are connected to the MPUs and DSP interrupt controller (INTC) modules. The interrupts are generated from the DISPC, DSI1 and DSI2 protocol engines, and HDMI.

Figure 10-8 shows DSS interrupt generation.

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Figure 10-8. DSS Interrupt Generation

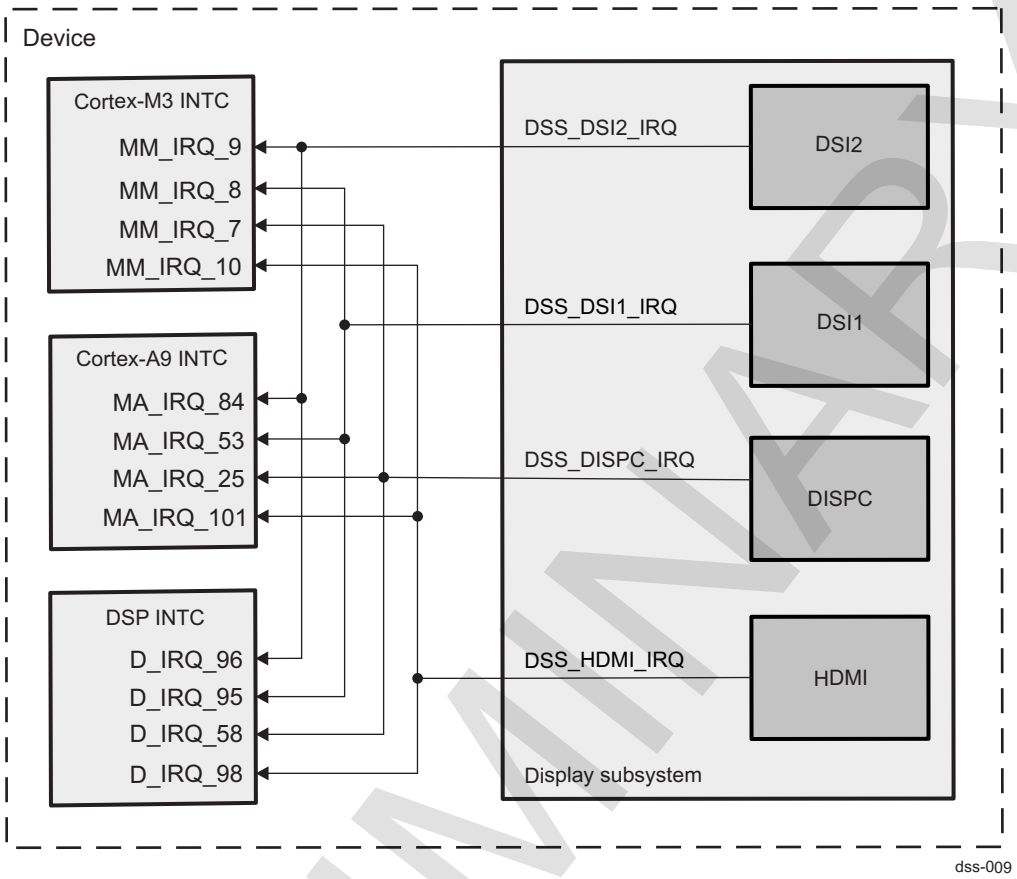

Table 10-7 lists the DSS interrupts.

Table 10-7. DSS Interrupts

Interrupt Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
DSS				
DISPC	DSS_DISPC_IRQ	D_IRQ_58	DSP INTC	DISPC interrupt request
		MA_IRQ_25	Cortex™-A9 INTC	DISPC interrupt request
		MM_IRQ_7	Cortex™-M3 INTC	DISPC interrupt request
MIPI DSI1	DSS_DSI1_IRQ	D_IRQ_95	DSP INTC	Display DSI1 interrupt request
		MA_IRQ_53	Cortex-A9 INTC	Display DSI1 interrupt request
		MM_IRQ_8	Cortex-M3 INTC	Display DSI1 interrupt request
MIPI DSI2	DSS_DSI2_IRQ	D_IRQ_96	DSP INTC	Display DSI2 interrupt request
		MA_IRQ_84	Cortex-A9 INTC	Display DSI2 interrupt request
		MM_IRQ_9	Cortex-M3 INTC	Display DSI2 interrupt request
HDMI	DSS_HDMI_IRQ	D_IRQ_98	DSP INTC	Display HDMI interrupt request
		MA_IRQ_101	Cortex-A9 INTC	Display HDMI interrupt request
		MM_IRQ_10	Cortex-M3 INTC	Display HDMI interrupt request

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10.1.2.5 DSS DMA Requests

Eleven DMA requests are connected to the system DMA (sDMA).

The DMA requests are:

- Four DMA request signals from each DSI protocol engine (data traffic: from SDRAM or IVA-HD SL2 to DSI protocol engine and from DSI protocol engine to SDRAM or IVA-HD SL2)
- One DMA request signal from RFBI module (data traffic: from SDRAM to RFBI)
- One DMA request signal from HDMI module (audio traffic: from SDRAM or IVA-HD SL2 to HDMI)
- One DMA request signal from DISPC module (used for synchronization of a logical channel in the sDMA for memory-to-memory transfers)

Figure 10-9 shows the details of DSS DMA request generation.

Figure 10-9. DSS DMA Request Generation

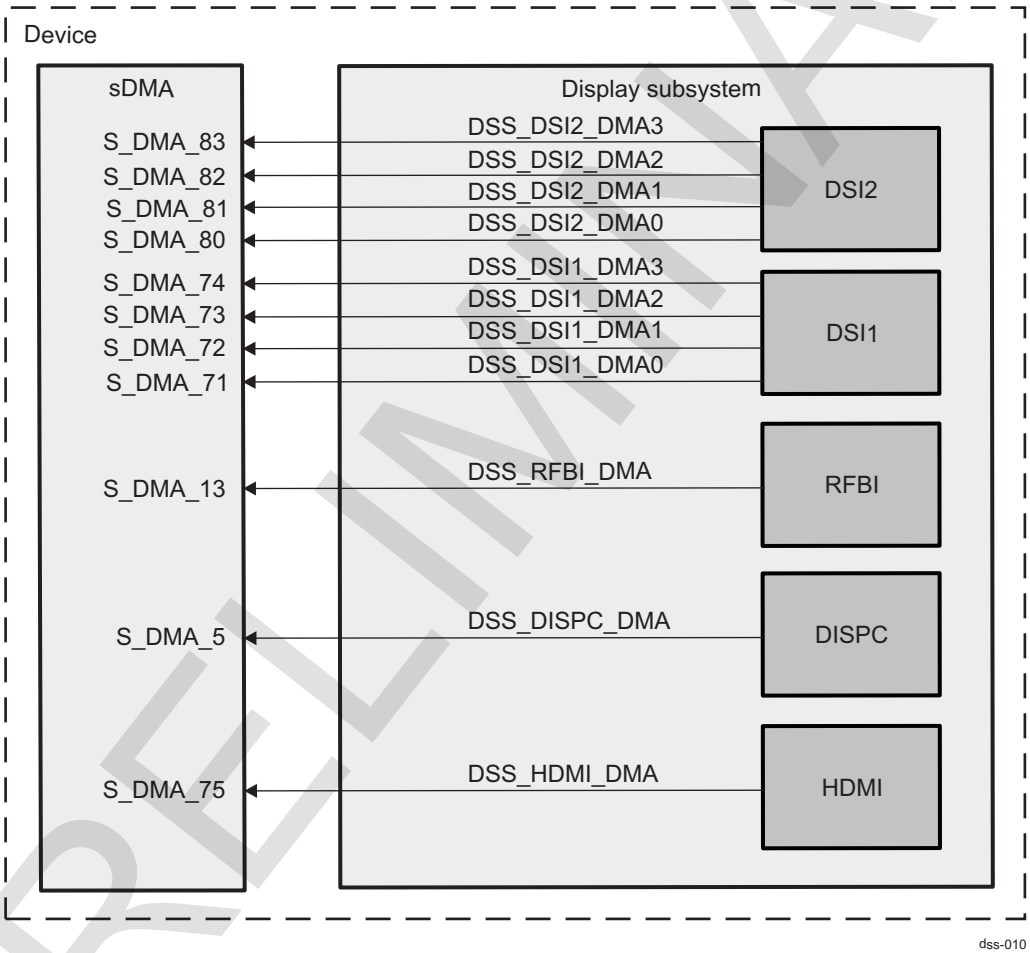

Table 10-8 lists the DSS DMA requests.

Table 10-8. DSS DMA Requests

DMA Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
RFBI	DSS_RFBI_DMA	S_DMA_13	sDMA	DSS RFBI DMA request
DISPC	DSS_DISPC_DMA	S_DMA_5	sDMA	The line trigger signal to synchronize a memory-to-memory logical channel in the DMA4 sDMA is generated by the DISPC IP.

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Table 10-8. DSS DMA Requests (continued)

MIPI DSI1	DSS_DSI1_DMA0	S_DMA_71	sDMA	DSS DSI1 DMA request 0
	DSS_DSI1_DMA1	S_DMA_72	sDMA	DSS DSI1 DMA request 1
	DSS_DSI1_DMA2	S_DMA_73	sDMA	DSS DSI1 DMA request 2
	DSS_DSI1_DMA3	S_DMA_74	sDMA	DSS DSI1 DMA request 3
MIPI DSI2	DSS_DSI2_DMA0	S_DMA_80	sDMA	DSS DSI2 DMA request 0
	DSS_DSI2_DMA1	S_DMA_81	sDMA	DSS DSI2 DMA request 1
	DSS_DSI2_DMA2	S_DMA_82	sDMA	DSS DSI2 DMA request 2
	DSS_DSI2_DMA3	S_DMA_83	sDMA	DSS DSI2 DMA request 3
HDMI	DSS_HDMI_DMA	S_DMA_75	sDMA	DSS HDMI audio DMA request

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10.1.3 DSS Register Manual

CAUTION

The main access to all DSS registers is through the L3 interconnect.

The access through the L4_PER interconnect is provided for back software compatibility.

10.1.3.1 DSS Instance Summary

Table 10-9. DSS Instance Summary

Module Name	L4_PER Base Address	L3 Base Address	Size
DSS	0x4804 0000	0x5800 0000	4KB

10.1.3.2 DSS Registers

10.1.3.2.1 DSS Registers Mapping Summary

Table 10-10 summarizes the DSS register mapping.

Table 10-10. DSS Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	DSS L4_PER Physical Address	DSS L3 Physical Address
DSS_REVISION	R	32	0x0000 0000	0x4804 0000	0x5800 0000
RESERVED	R	32	0x0000 0010	0x4804 0010	0x5800 0010
DSS_SYSSTATUS	R	32	0x0000 0014	0x4804 0014	0x5800 0014
DSS_CTRL	RW	32	0x0000 0040	0x4804 0040	0x5800 0040
DSS_STATUS	R	32	0x0000 005C	0x4804 005C	0x5800 005C

10.1.3.2.2 DSS Register Description

NOTE: The VDAC function is not supported.

Table 10-11 through Table 10-17 describe the register bits.

Table 10-11. DSS_REVISION

Address Offset	0x0000 0000		
Physical Address	0x4804 0000 0x5800 0000	**Instance**	DSS_PER_L4 DSS_L3
Description	This register contains the DSS revision number.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP revision	R	See (1)

(1) TI internal data

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Table 10-12. Register Call Summary for Register DSS_REVISION

Display Subsystem Overview

- DSS Registers Mapping Summary: [0]

Table 10-13. DSS_SYSSTATUS

Address Offset	0x0000 0014		
Physical Address	0x4804 0014 0x5800 0014	**Instance**	DSS_PER_L4 DSS_L3
Description	This register provides status information about the module.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															RESETDONE

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	RESETDONE	Internal reset monitoring Read 0x0: Internal module reset is ongoing. Read 0x1: Reset complete	R	0x1

Table 10-14. Register Call Summary for Register DSS_SYSSTATUS

Display Subsystem Overview

- DSS Registers Mapping Summary: [0]

Table 10-15. DSS_CTRL

Address Offset	0x0000 0040		
Physical Address	0x4804 0040 0x5800 0040	**Instance**	DSS_PER_L4 DSS_L3
Description	This register contains the DSS control bits.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														LCD2_TV_SEL	RESERVED	VENC_HDMI_SWITCH	RFBI_SWITCH	SYNC_SWITCH	LCD2_CLK_SWITCH	TV_CLK_SWITCH	DSI2_CLK_SWITCH	FCK_CLK_SWITCH		RESERVED	VENC_OUT_SEL	DAC_POWERDN_BGZ	DAC_DEMEN	VENC_CLOCK_4X_ENABLE	VENC_CLOCK_MODE	DSI1_CLK_SWITCH	LCD1_CLK_SWITCH

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Bits	Field Name	Description	Type	Reset
31: 18	RESERVED	Reserved	R	0x0000
17	LCD2_TV_SEL	Selection between LCD2 and TV channel out on the LCD2 parallel output (multiplexer 13) 0x0: Select LCD2 channel output (default selection) 0x1: Select TV channel output	RW	0x0
16	RESERVED	Reserved	R	0x0
15	VENC_HDMI_SWITCH	Selects HDMI sync and associated clock or VENC and its associated TV_CLK 0x0: VENC selected 0x1: HDMI selected	RW	0x0
14	RFBI_SWITCH	Selects the video port from DISPC between video port 1 and video port 2 (multiplexer 11). Read 0x0: Video port 1 (also named primary LCD output or LCD1) is selected (backward-compatible mode). Read 0x1: Video port 2 (also named secondary LCD output or LCD2) is selected.	RW	0x0
13	SYNC_SWITCH	Selects the sync generator for SD video (DSS VENC IP, or component VENC IP connected at the top) Read 0x0: Internal VENC IP selected Read 0x1: Component VENC IP selected	RW	0x0
12	LCD2_CLK_SWITCH	DSS_CLK/PLL2_CLK1 clock switch (multiplexer 3) Selects the clock source for the DISPC LCD2_CLK clock 0x0: DSS_CLK selected (from PRCM) 0x1: PLL2_CLK1 selected	RW	0x0
11	TV_CLK_SWITCH	DSS_TV_CLK/PLL3_CLK clock switch Selects the clock source for the VENC/HDMI functional clock 0x0: PLL3_CLK1 selected (from HDMI PLL) 0x1: DSS_TV_CLK selected (from PAD)	RW	0x0
10	DSI2_CLK_SWITCH	DSS_CLK/PLL2_CLK2 clock switch Selects the clock source for the DSI2 functional clock DSI2_CLK 0x0: DSS_CLK selected (from PRCM) 0x1: PLL2_CLK2 selected (from DSI2 PLL)	RW	0x0
9:8	FCK_CLK_SWITCH	Selects the clock source for the DISPC functional clock DISPC_FCLK 0x0: DSS_CLK selected (from PRCM) 0x1: PLL1_CLK1 selected (from DSI1 PLL) 0x2: PLL2_CLK1 selected (from DSI2 PLL) 0x3: PLL3_CLK1 selected (from HDMI PLL)	RW	0x0
7	RESERVED	Write 0's for future compatibility. Reads returns 0.	R	0x0
6	VENC_OUT_SEL	VENC mode selection for VENC output multiplexer 0x0: Composite VENC output selected 0x1: Luminance VENC output selected	RW	0x0
5	DAC_POWERDN_BGZ	DAC Power-down band gap control 0x0: DAC power-down band gap disabled 0x1: DAC power-down band gap enabled	RW	0x0
4	DAC_DEMEN	DAC Dynamic Element Matching Enable 0x0: DAC dynamic element matching disabled 0x1: DAC dynamic element matching enabled	RW	0x0

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Bits	Field Name	Description	Type	Reset
3	VENC_CLOCK_4X_ENABLE	VENC clock CLK4X enable This bit is used to control the CLK4X clock gating. 0x0: Disable 0x1: Enable	RW	0x0
2	VENC_CLOCK_MODE	VENC clock mode. See Section 10.6.3, *Video Encoder Integration*. 0x0: Clock Mode 0. 0x1: Clock Mode 1. In both clock modes, all three balanced clocks, derived from the TV_CLK clock, are provided to the VENC, if the VENC_CLOCK_4X_ENABLE [3] bit is set to 1 by software.	RW	0x0
1	DSI1_CLK_SWITCH	DSS_CLK/PLL1_CLK2 clock switch Selects the clock source for the DSI1 functional clock DSI1_CLK 0x0: DSS_CLK selected (from PRCM) 0x1: PLL1_CLK2 selected (from DSI1 PLL)	RW	0x0
0	LCD1_CLK_SWITCH	DSS_CLK/PLL1_CLK1 clock switch (multiplexer 2) Selects the clock source for the DISPC LCD1_CLK clock 0x0: DSS_CLK selected (from PRCM) 0x1: PLL1_CLK1 selected (from DSI1 PLL)	RW	0x0

Table 10-16. Register Call Summary for Register DSS_CTRL

Display Subsystem Overview
- Parallel Interface: [0] [1] [2] [3]
- DSS Clocks: [4] [5]
- DSS Registers Mapping Summary: [6]

Table 10-17. DSS_STATUS

Address Offset	0x0000 005C		
Physical Address	0x4804 005C 0x5800 005C	**Instance**	DSS_PER_L4 DSS_L3
Description	This register contains the DSS status.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										RFBI_STATUS	SYNC_STATUS	FCK_CLK_STATUS				TV_CLK_STATUS			LCD2_CLK_STATUS		DSI2_CLK_STATUS		DSI1_CLK_STATUS	TV_CLK_OUT_STATUS			RESERVED				LCD1_CLK_STATUS

Bits	Field Name	Description	Type	Reset
31:22	RESERVED	Reserved	R	0x000
21	RFBI_STATUS	Video port selection status (multiplexer 11) Indicates if video port 1 or video 2 from DISPC is used to provide data to the RFBI Read 0x0: Video port 1 (named also primary LCD output or LCD1) used to provide data to RFBI Read 0x1: Video port 2 (named also secondary LCD output or LCD2) used to provide data to RFBI	R	0x0

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Bits	Field Name	Description	Type	Reset
20:19	SYNC_STATUS	Sync generator selection status (multiplexer 9) Indicates if DSS VENC IP or external component VENC IP is selected as syncs generator (master mode) Read 0x0: Internal VENC IP selected Read 0x1: Component VENC IP selected Read 0x2: HDMI IP selected	R	0x0
18:15	FCK_CLK_STATUS	DISPC_FCLK clock selection status (multiplexer 1), indicates which clock is used by the glitch-free multiplexer selecting the source of DISPC_FCLK. The current and the new-selected clocks must be running to be able to switch. Both clocks are used at the same time while the switching is ongoing. Read 0x0: DSS_CLK clock switching is ongoing. Read 0x1: DSS_CLK is used by DISPC as DISPC_FCLK clock. Read 0x2: PLL1_CLK1 is used by DISPC as DISPC_FCLK clock. Read 0x4: PLL2_CLK1 is used by DISPC as DISPC_FCLK clock. Read 0x8: PLL3_CLK1 (TV_CLK) is used by DISPC as DISPC_FCLK clock.	R	0x1
14:13	TV_CLK_STATUS	TV_CLK clock selection status (multiplexer 7), indicates which clock is used by the multiplexer selecting the source of TV_CLK. The current and the new-selected clocks must be running to be able to switch. Both clocks are used at the same time while the switching is ongoing. Read 0x1: PLL3_CLK1 is used as TV_CLK. Read 0x2: DSS_TV_CLK is used as TV_CLK.	R	0x1
12:11	LCD2_CLK_STATUS	LCD2_CLK clock selection status (multiplexer 3), indicates which clock is used by the glitch-free multiplexer selecting the source of LCD2_CLK. The current and the new-selected clocks must be running to be able to switch. Both clocks are used at the same time while the switching is ongoing. Read 0x0: LCD2_CLK clock switching is ongoing. Read 0x1: DSS_CLK is used as LCD2_CLK. Read 0x2: PLL2_CLK1 is used by DISPC as LCD2_CLK clock.	R	0x1
10:9	DSI2_CLK_STATUS	DSI2_CLK clock selection status (multiplexer 5), indicates which clock is used by the glitch-free multiplexer selecting the source of DSI2_CLK. The current and the new-selected clocks must be running to be able to switch. Both clocks are used at the same time while the switching is ongoing. Read 0x0: DSI2_CLK clock switching is ongoing Read 0x1: DSS_CLK is used by DSI2 as DSI2_CLK clock. Read 0x2: PLL2_CLK2 is used by DSI2 as DSI2_CLK clock.	R	0x1

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Bits	Field Name	Description	Type	Reset
8:7	DSI1_CLK_STATUS	DSI1_CLK clock selection status (multiplexer 4), indicates which clock is used by the glitch-free multiplexer selecting the source of DSI1_CLK. The current and the new-selected clocks must be running to be able to switch. Both clocks are used at the same time while the switching is ongoing. Read 0x0: DSI1_CLK clock switching is ongoing. Read 0x1: DSS_CLK is used by DSI1 as DSI1_CLK clock. Read 0x2: PLL1_CLK2 is used by DSI1 as DSI1_CLK clock.	R	0x1
6:5	TV_CLK_OUT_STATUS	TV_CLK_OUT selection status (multiplexer 12) indicates which clock is used by the multiplexer selecting the TV_CLK_OUT of the DISPC. The current and the new-selected clocks must be running to be able to switch. Both clocks are used at the same time while the switching is ongoing. Read 0x1: TV_CLK is used by DISPC as TV_CLK_OUT clock. Read 0x2: HDMI_M_PCLK is used by DISPC as TV_CLK_OUT clock.	R	0x1
4:2	RESERVED	Reserved	R	0x0
1:0	LCD1_CLK_STATUS	LCD1_CLK clock selection status (multiplexer 2), indicates which clock is used by the glitch-free multiplexer selecting the source of LCD1_CLK. The current and the new-selected clocks must be running to be able to switch. Both clocks are used at the same time while the switching is ongoing. Read 0x0: LCD1_CLK clock switching is ongoing. Read 0x1: DSS_CLK is used as LCD1_CLK. Read 0x2: PLL1_CLK1 is used by DISPC as LCD1_CLK clock.	R	0x1

Table 10-18. Register Call Summary for Register DSS_STATUS

Display Subsystem Overview

- DSS Registers Mapping Summary: [0]

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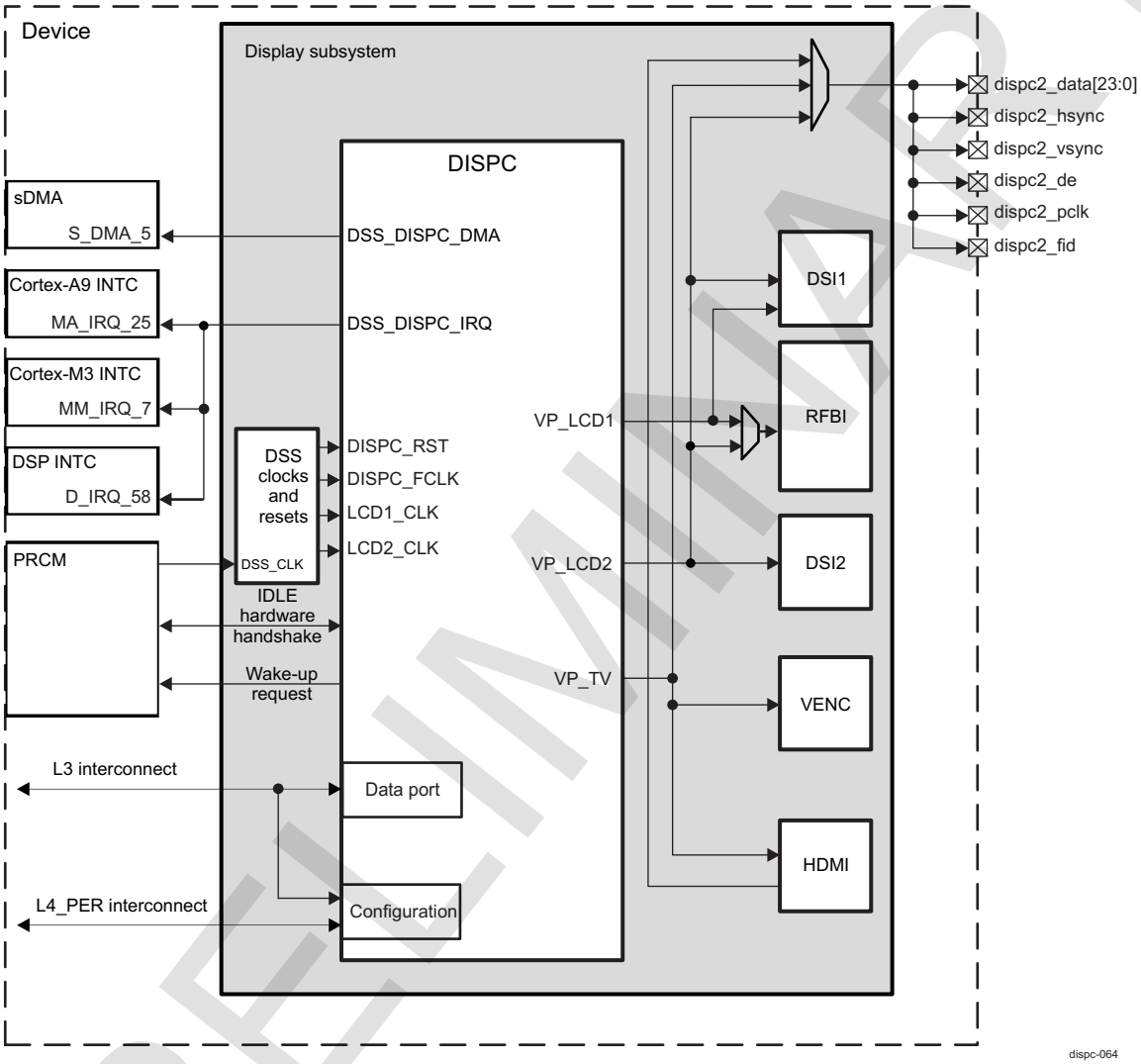
10.2 Display Controller

10.2.1 Display Controller Overview

Figure 10-10 shows a block diagram of the display subsystem.

Figure 10-10. Display Subsystem Highlight



The DISPC includes the following main features:

- Five pipelines for processing:
  - One Graphics pipeline (GFX):
    - Pixel formats: ARGB16-4444, xRGB12-4444, RGBA16-4444, RGBx12-4444, RGB16-565, ARGB16-1555, xRGB16-1555, ARGB32-8888, RGBA32-8888, xRGB32-8888, RGBx32-8888, RGB24-888, and BITMAP (1-, 2-, 4-, or 8-bits per pixel) (x means that the correspond bits in the container are not used)
    - Selection of the color depth expansion from ARGB16-4444, RGBA16-4444, and ARGB16-1555 to ARGB32-8888 and from xRGB12-4444, RGBx12-4444, and xRGB16-1555 to xRGB32-8888 (replication of the MSBs or adding 0s)
    - Support for color look-up table (CLUT): 256 × 24-bit entries palette in RGB
    - Support for antiflicker on RGB pixel formats using 3-tap filter.
  - Three Video pipelines (VID1,VID2, and VID3):

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- Pixel formats: ARGB16-4444, xRGB12-4444, RGBx12-4444, RGBA12-3333, RGBA16-4444, RGB16-565, ARGB16-1555, xRGB16-1555, ARGB32-8888, RGBA32-8888, xRGB32-8888, RGBx32-8888, RGB24-888, YUV4:2:2-UYVY, YUV4:2:2-YUV2, and YUV4:2:0-NV12 (x means that the correspond bits in the container are not used)
- Selection of the color depth expansion from ARGB16-4444, RGBA16-4444, and ARGB16-1555 to ARGB32-8888 and from xRGB12-4444, RGBx12-4444, and xRGB16-1555 to xRGB32-8888 (replication of the MSBs or adding 0s)
- Programmable polyphase filter:
  - Independent horizontal and vertical resampling: upsampling (up to x8) and downsampling (down to 1/4)
  - Maximum input width of 1920 pixels
  - No limitation on the input height
  - Supported input formats are ARGB32-8888, YUV4:2:2-UYVY, YUV4:2:2-YUV2, and YUV4:2:0-NV12
  - Alpha blending factor is rescaled like the R, G, and B color components.
- Programmable color space conversion from YUV4:2:2 (YUV4:4:4, YUV4:2:0 after Chroma upsampling through the scaler) into ARGB32-8888. Images in YUV4:2:2 format with 90/270 degree rotation are preprocessed to YUV4:4:4 before the scaler, by duplicating the missing Chroma.
- Programmable VC-1 range mapping

– One Write-back pipeline (WB): allows to take benefit of the hardware processing available inside the DISPC like color space conversion, rescaling, compositing to perform memory-to-memory transfer with data processing or capturing a displayed frame.
  - Programmable color space conversion RGB24 into YUV4:4:4 or to YUV4:2:2-UYVY, YUV4:2:2-YUV2, or YUV4:2:0-NV12 using programmable polyphase filter.
  - Programmable color space conversion RGB24 into YUV4:2:2-UYVY, YUV4:2:2-YUV2, or YUV4:2:0-NV12
  - Selection of the color depth reduction from RGB24 to RGB16
  - Programmable polyphase filter:
    - Independent horizontal and vertical resampling: upsampling (up to x8) and downsampling (down to 1/4)
    - Maximum input width of 1920 pixels
    - No limitation on the input height
    - Supported input formats are ARGB32-8888, YUV4:2:2-UYVY, YUV4:2:2-YUV2, and YUV:2:0-NV12
    - Alpha blending factor is rescaled like the R, G, and B color components.
  - Selection of the source of the data:
    - Overlay output:
      - Primary LCD
      - Secondary LCD
      - TV
    - Pipelines:
      - Graphic
      - Video 1
      - Video 2
      - Video 3

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- Two LCD outputs, primary (LCD1) and secondary (LCD2):
  - Input pixel format: ARGB32-8888
  - Output pixel format: RGB24-888
  - Overlay of graphic and video 1, 2, and 3 pipelines
  - Source and destination transparency color key
  - Global and pixel alpha blending (up to 8-bit blending factor)
  - Z-order programmable (full flexibility)
  - Three types of displays are supported:
    - Passive matrix monochrome: 4-/8-bit monochrome panel interface support (15 grayscale levels supported using dithering block)
    - Passive matrix color: 8-bit color panel interface support (3375 colors supported for a color panel using dithering block)
    - Active matrix color: 12-/16-/18-/24-bit panel interface support (replicated or dithered encoded pixel values)
  - Independent programmable timing generators for LCD1 and LCD2 to support:

Primary LCD	Using DSI1 interface	SXGA VESA timing @ 60 FPS
	Using RFBI	WVGA @ 30 fps
Secondary LCD	Using DSI2 interface	SXGA VESA timing @ 85 fps
	Using RFBI	WVGA @ 30 fps
	Using CMOS interface	SXGA VESA timing @ 85 fps1080i/720p CEA-861-D

  - Configurable LCD output mode: progressive or interlace mode
  - Selection between RGB and YUV4:2:2 output pixel format
  - Remote frame buffer support through the RFBI module
  - Partial display through the RFBI
  - Multiple-cycle output format on 8-/9-/12-/16-bit interface time division multiplexing (TDM)
- One TV output
  - Input pixel format: ARGB40-10.10.10.10
  - Output pixel format: ARGB40-10.10.10.10
  - Overlay of graphic and video 1, 2, and 3 pipelines
  - Source and destination transparency color key
  - Global and pixel alpha blending (up to 10-bit blending factor)
  - Z-order programmable (full flexibility)
  - Slave mode support (no master mode support) with synchronization signals provided by the VENC (NTSC/PAL encoder or HDMI TX)
    - HSYNC (horizontal synchronization signal)
    - VSYNC (vertical synchronization signal)
    - RE (data request signal)
    - FID (field ID: odd/even field information)
  - RGB24-888 data bus output for connection to the NTSC/PAL VENC
  - RGB30-10.10.10 data bus output for connection to HDMI TX and extended to 36 by duplication of the MSBs
  - SD-576i and SD-480i using NTSC/PAL VEC
  - HD-1080p, HD-1080i, HD-720p, SD-480p, SD-576p, SD-576i, and SD-480i using HDMI
  - HDMI deep color mode support, 30-bit data output to HDMI encoder
  - Pixel duplication capability (from one pixel clock cycle up to eight cycles)

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NOTE: The video DAC (VDAC) function is not supported.

- Panel support with MIPI DPI protocol
  - 4-/8-bit monochrome passive matrix panel interface support (15 grayscale levels supported using dithering block)
  - 8-bit color passive matrix panel interface support (3375 colors supported for a color panel using dithering block)
  - 12-/16-/18-/24-bit active matrix panel interface support (replicated or dithered encoded pixel values
- Common
  - Rotation 0, 90, 180, and 270 using DMM-TILER
  - Synchronized buffer update
  - Hardware cursor (using the graphics pipeline or one of the video pipelines)
  - Independent gamma curve support on primary LCD output, secondary LCD output and TV output
  - Multiple-buffer support
  - Mirroring/flip-flop support (using DMM-TILER)
  - Programmable color phase rotation (CPR)
  - Alpha blending support:
    - Embedded pixel factor (ARGB and RGBA)
    - Global alpha
- DMA (internal to the DISPC)
  - Support for accessing tiled structure through the TILER inside the dynamic memory management (DMM)
  - Support for rotation, flip-flop, and mirroring though the TILER inside the DMM
  - Support for memory fragmentation though the TILER inside the DMM
  - Integrated shared buffers between DMA engine and pipelines
  - Programmable buffer thresholds
  - Bandwidth limiter on write request (insertion on idle cycles between requests)
- Advanced
  - Mode outputting data on display only from the DMA buffer (self-refresh using the DMA FIFO)
  - DMA buffer hand-check in STALL mode
  - Arbitration between high/low priority (GFX, VID1, VID2, VID3, and WB pipelines)
- Power modes
  - Low-power saving modes
  - Support on-the-fly dynamic voltage and frequency scaling (DVFS)
  - Merge capability of the DMA buffers to support greater OFF period on the L3 interconnect
    - All buffers associated to a single pipeline
    - Reallocation of the buffers of the nonactive pipelines to the active pipelines

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10.2.2 Display Controller Environment

The DISPC provides the required control signals to interface directly to an external parallel panel for the MIPI DPI protocol.

Figure 10-11 shows the LCD support parallel interface.

NOTE: Parallel interface is available through the LCD2 and TV outputs of the DISPC.

The LCD2 data and control signals are multiplexed with the TV output data, and control signals provided by the HDMI module.
The selection can be done at DSS top level. For further details and signals mapping, see Section 10.1.1.1.1 *Parallel Interface*, under Section 10.1 *Display Subsystem Overview*.

Figure 10-11. LCD Support Parallel Interface

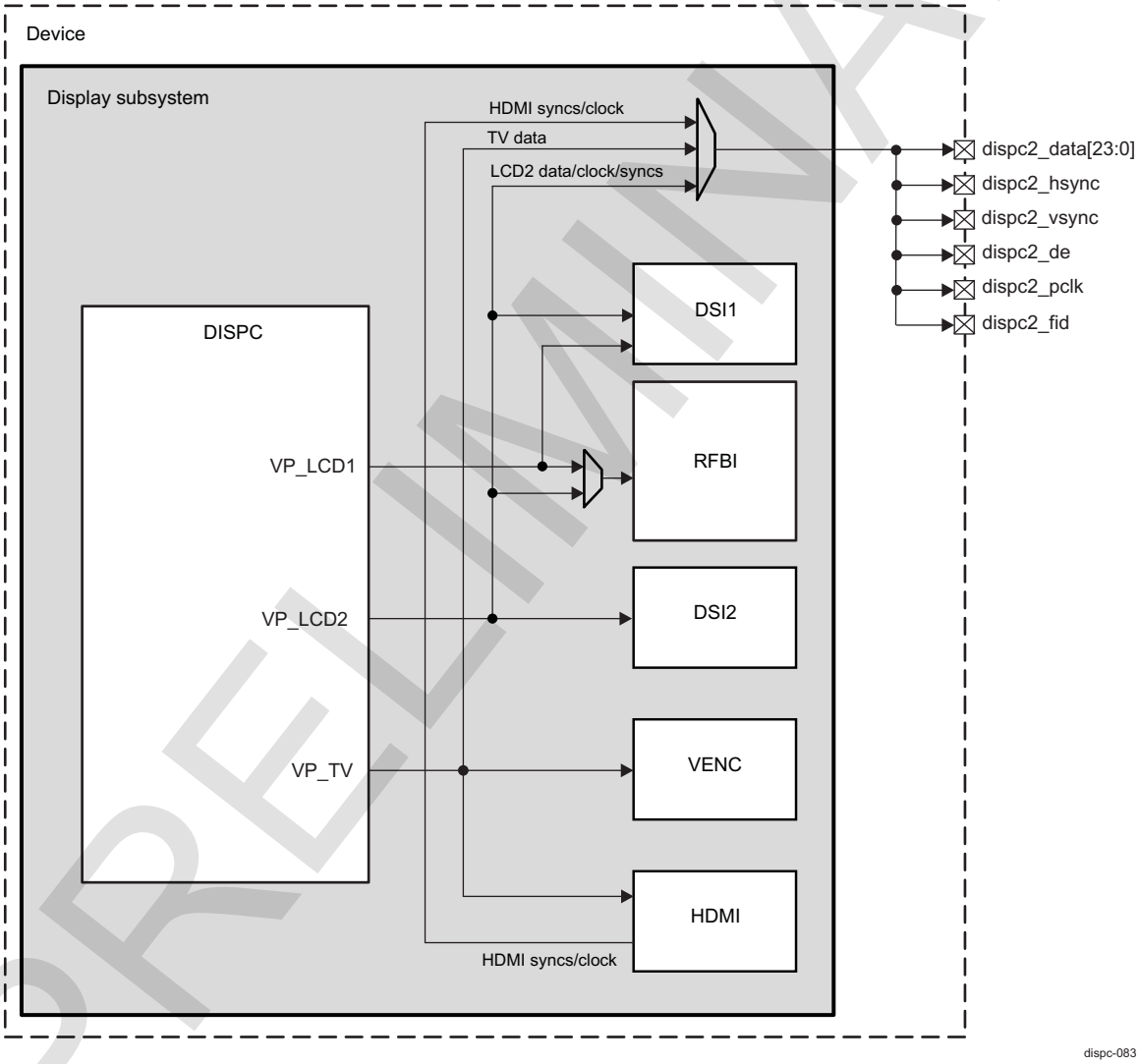

Table 10-19 describes the interface signals to/from the LCD panel in bypass mode.

Table 10-19. Parallel Interface Signals

Signal Name	Type (1)	Description
dispc2_data[23:0]	O	Pixels data

(1) I = Input, O = Output, I/O = Input/Output

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Table 10-19. Parallel Interface Signals (continued)

Signal Name	Type [1]	Description
dispc2_pclk	O	Pixel clock
dispc2_vsync	O	Vertical synchronization. The LCD frame clock (vsync) toggles after all the lines in a frame are transmitted to the LCD panel and a programmable number of line clock cycles has elapsed at the beginning and at the end of each frame.
dispc2_hsync	O	Horizontal synchronization. The LCD line clock (hsync) toggles after all pixels in a line are transmitted to the LCD panel and a programmable number of pixel clock wait-states elapse, at the beginning and the end of each line.
dispc2_de	O	• In passive matrix technology, the de signal is configured to transition each time a programmable number of line clocks occurs. To prevent a dc charge within the screen pixels, the power and ground supplies of the panel are periodically switched. The DISPC signals the panel to switch the polarity by toggling the de pin. • In active matrix technology, the de signal acts as an output-enable signal to indicate when data must be latched using the pixel clock.
dispc2_fid	O	The FID signal indicates the field identifier for the LCD output field • 0 means even. • 1 means odd.

10.2.2.1 LCD Output and Data Format for the Parallel Interface

This section describes the pixel data bus and shows timing diagrams of transactions and synchronizations.

Figure 10-12 through Figure 10-18 show the pixel data bus, depending on the use of 4-, 8-, 12-, 16-, 18-, or 24-pixel data output pins.

Table 10-20 lists the number of displayed pixels per pixel clock cycle based on the type of display panel.

Table 10-20. Number of Displayed Pixels per Pixel Clock Cycle Based on Display Type

Display Panel	Number of Displayed Pixels per Pixel Clock Cycle
Monochrome 4-bit	4
Monochrome 8-bit	8
Passive matrix color	8/3
Active matrix	1

- Passive matrix technology, monochrome mode

  Monochrome displays use a 4-bit or 8-bit interface. Each bit represents one pixel (on or off), which means that 4 or 8 pixels are sent to the LCD at each pixel clock.

  Figure 10-12 and Figure 10-13 show 4- and 8-bit monochrome displays, respectively.

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Figure 10-12. LCD Pixel Data Monochrome4 Passive Matrix

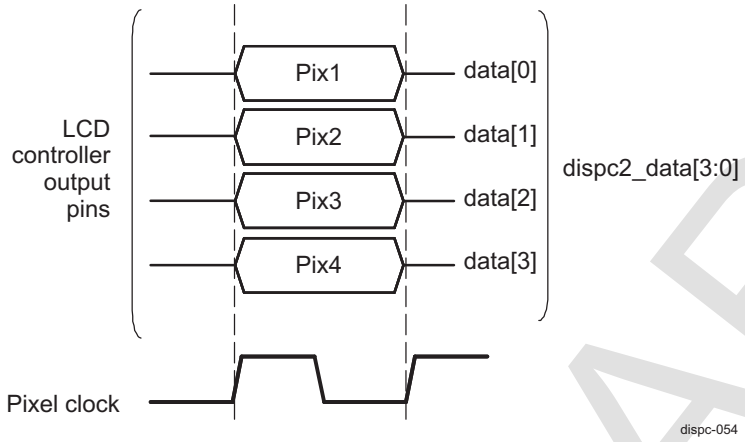
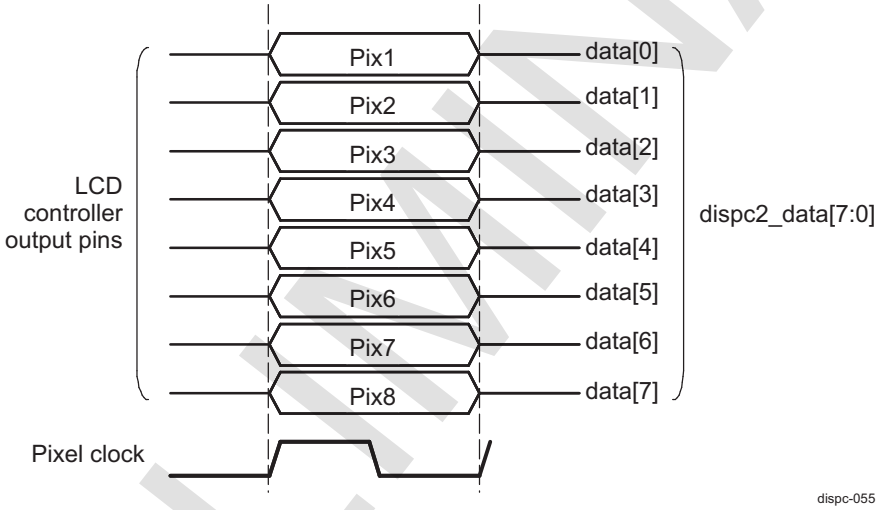


Figure 10-13. LCD Pixel Data Monochrome8 Passive Matrix



- Passive matrix technology, color mode

  Color passive displays use 8-bit data input lines. In a given pixel clock cycle, each line represents one color component (red, green, or blue).

  Figure 10-14 shows an 8-bit color passive matrix display.

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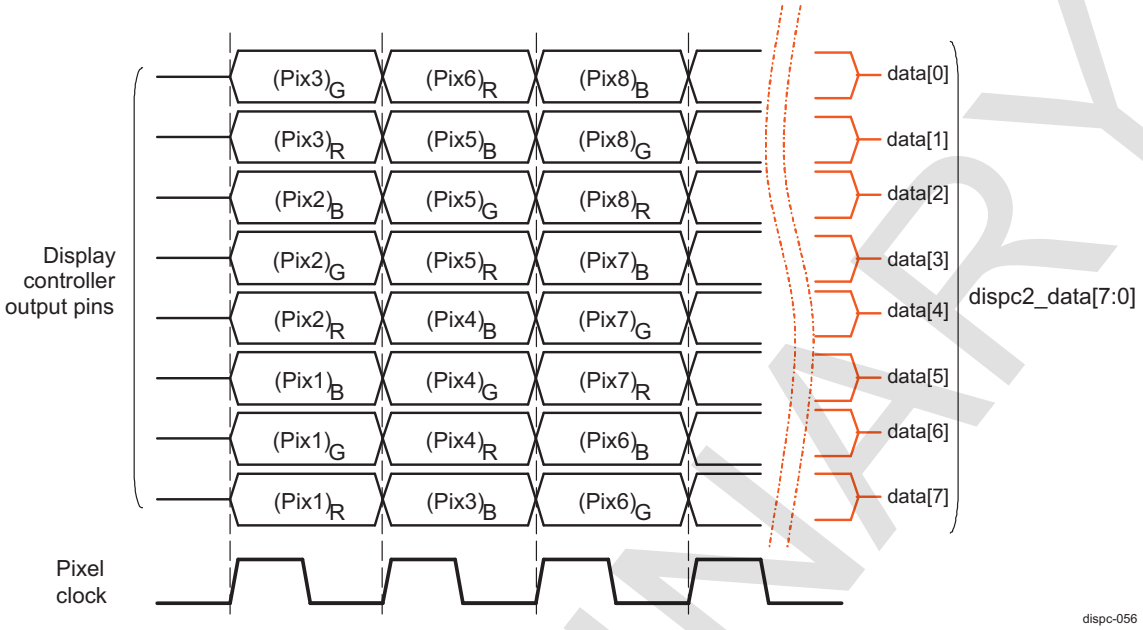
Figure 10-14. LCD Pixel Data 8-Bit Color Passive Matrix



- Active matrix technology

  Active matrix displays bypass the STN dithering logic block and the output FIFO. Each line represents one pixel.

  Figure 10-15 through Figure 10-18 show 12-, 16-, 18-, and 24-active matrix displays, respectively.

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Figure 10-15. LCD Pixel Data Color12 Active Matrix

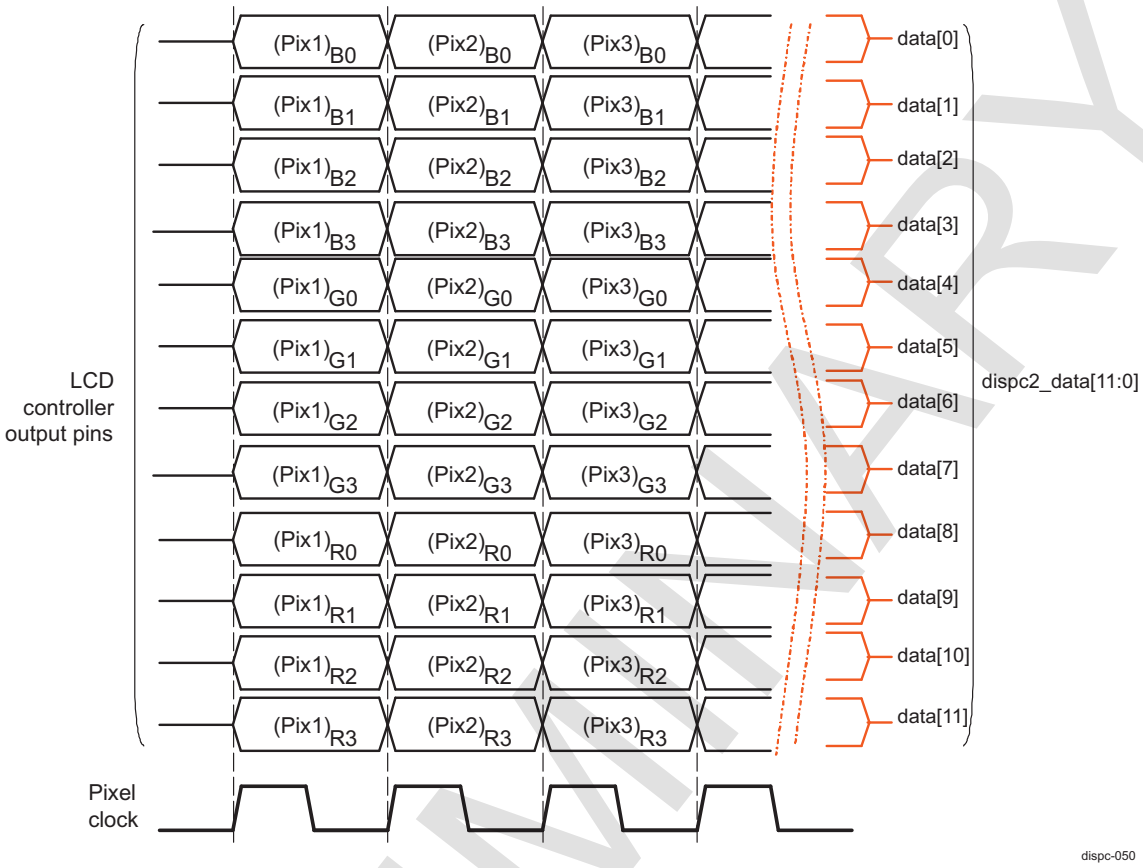

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Figure 10-16. LCD Pixel Data Color16 Active Matrix

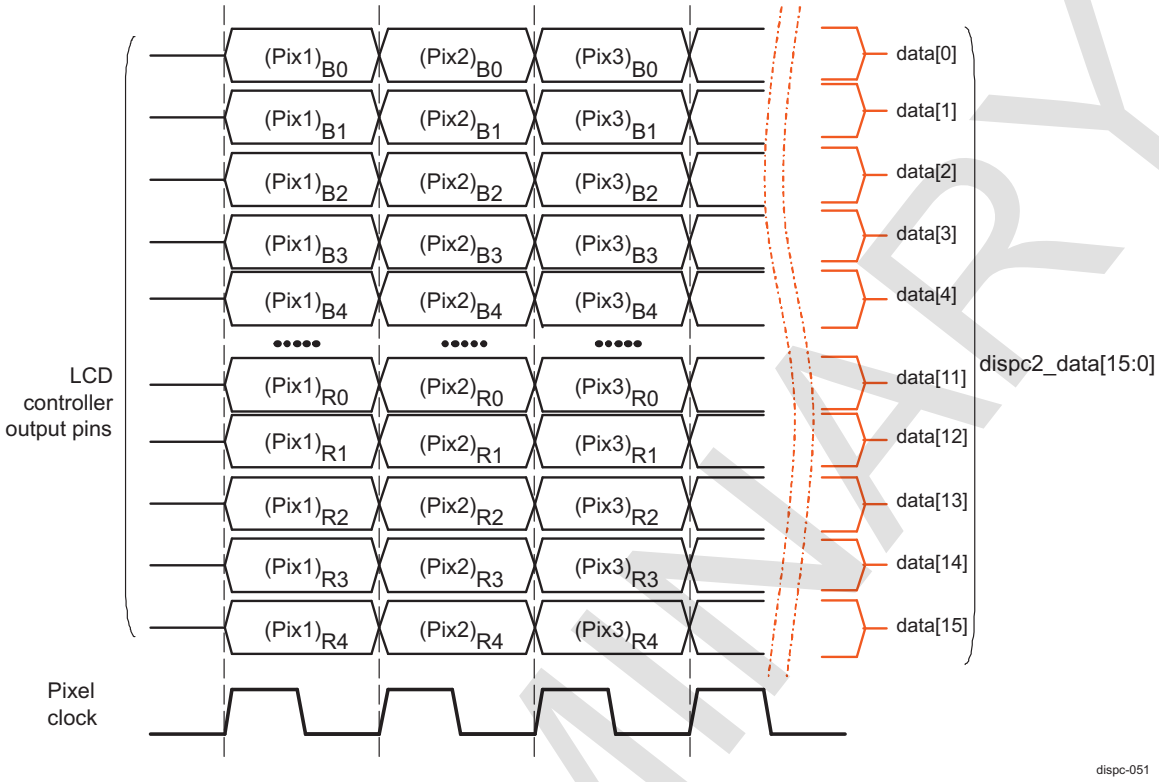

Figure 10-17. LCD Pixel Data Color18 Active Matrix

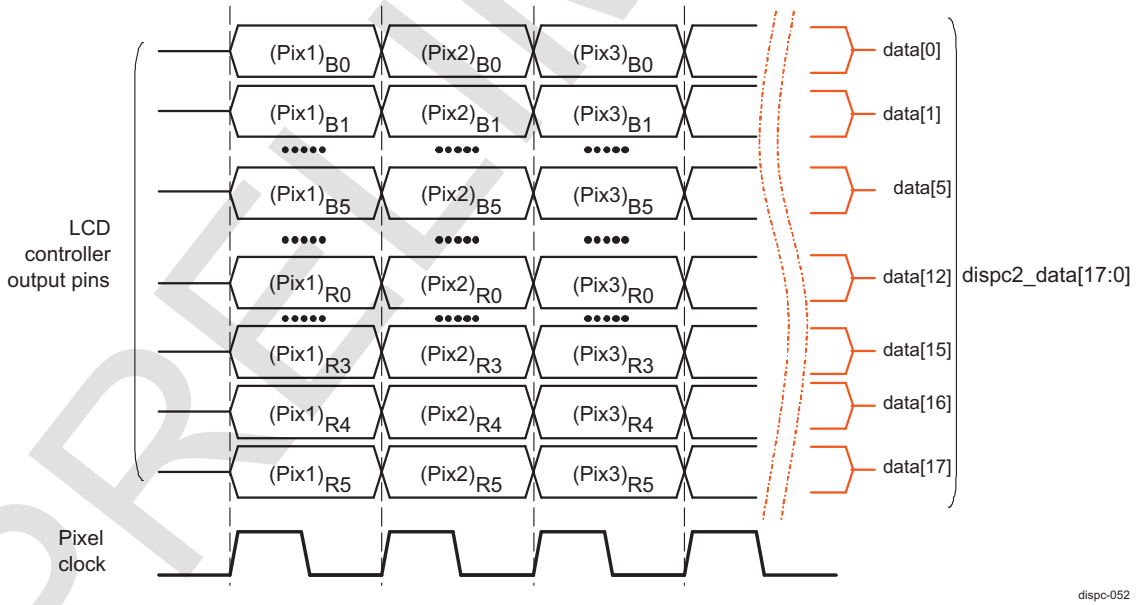

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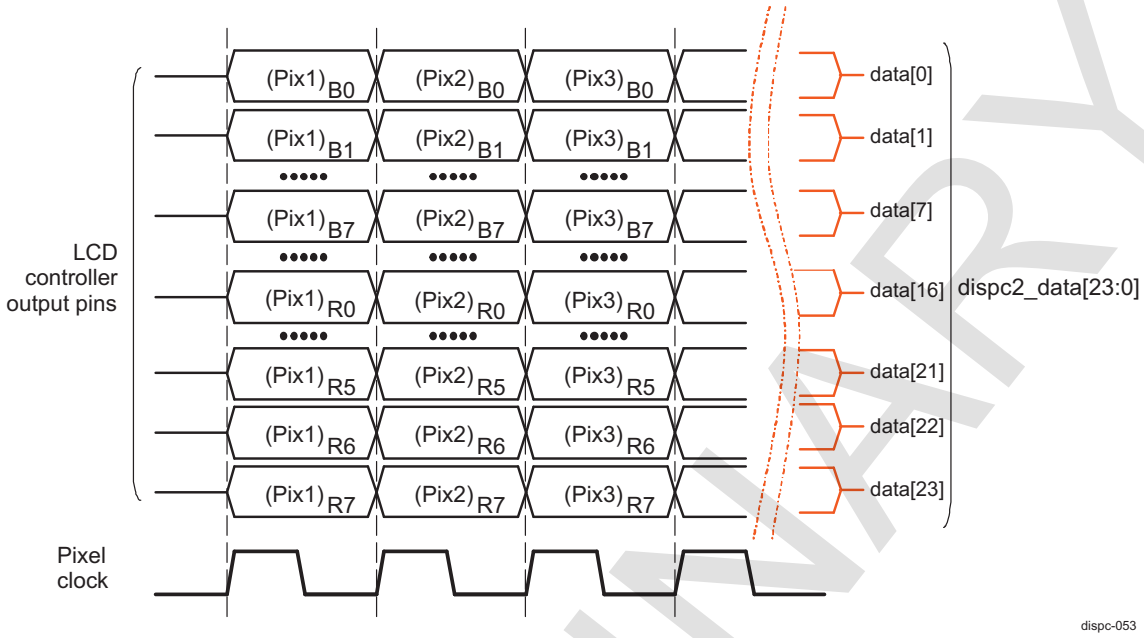
Figure 10-18. LCD Pixel Data Color24 Active Matrix



10.2.2.2 Transaction Timing Diagrams

Figure 10-19 through Figure 10-34 show timing diagrams of synchronization signals and pixel clock for passive matrix and active matrix panels. The DISPC directly drives these signals, which are related to the programmable fields described in Table 10-21.

Table 10-21. Programmable Fields in Bypass Mode

Name	Register	Description
PPL	DISPC_SIZE_LCDo[10:0] PPL bit field value + 1	Pixels per line
LPP	DISPC_SIZE_LCDo[26:16] LPP bit field value + 1	Lines per panel
HBP	DISPC_TIMING_Ho[31:20] HBP bit field value + 1	Horizontal back porch
HFP	DISPC_TIMING_Ho[19:8] HFP bit field value + 1	Horizontal front porch
HSW	DISPC_TIMING_Ho[7:0] HSW bit field value + 1	Horizontal synchronization pulse width
VBP	DISPC_TIMING_Vo[31:20] VBP bit field value	Vertical back porch
VFP	DISPC_TIMING_Vo[19:8] VFP bit field value	Vertical front porch
VSW	DISPC_TIMING_Vo[7:0] VSW bit field value + 1	Vertical synchronization pulse width
ONOFF	DISPC_POL_FREQo[17] ONOFF bit	DISPC_HSYNC and DISPC_VSYNC pixel clock control
RF	DISPC_POL_FREQo[16] RF bit	DISPC_HSYNC and DISPC_VSYNC pixel clock edge control
IEO	DISPC_POL_FREQo[15] IEO bit	Invert DISPC_ACBIAS
IPC	DISPC_POL_FREQo[14] IPC bit	Invert DISPC_PCLK
IHS	DISPC_POL_FREQo[13] IHS bit	Invert DISPC_HSYNC
IVS	DISPC_POL_FREQo[12] IVS bit	Invert DISPC_VSYNC

- Active matrix timing configuration 1
  - DISPC_POL_FREQo[17] ONOFF bit = 0
  - DISPC_POL_FREQo[16] RF bit = 0

    The HSYNC and VSYNC signals are driven on the opposite edge of PCLK from the pixel data.
  - DISPC_POL_FREQo[15] IEO = 0

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The DE signal is active high.

– DISPC_POL_FREQo[14] IPC = 0
  The pixel data are driven on the rising edge of PCLK.
– DISPC_POL_FREQo[13] IHS = 0
  The HSYNC signal is active high.
– DISPC_POL_FREQo[12] IVS = 0
  The VSYNC signal is active high.

Figure 10-19. Active Matrix Timing Diagram of Configuration 1 (Start of Frame)

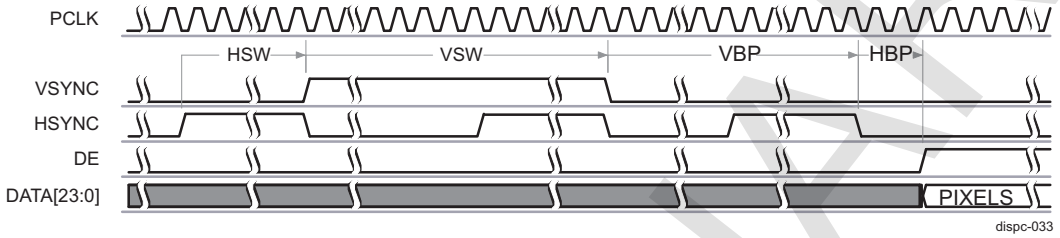


Figure 10-20. Active Matrix Timing Diagram of Configuration 1 (Between Lines)

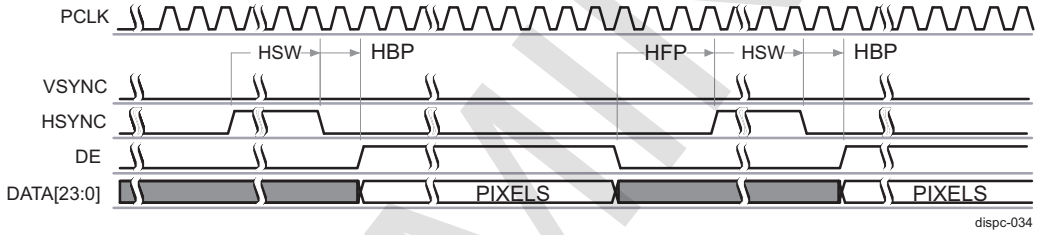


Figure 10-21. Active Matrix Timing Diagram of Configuration 1 (Between Frames)

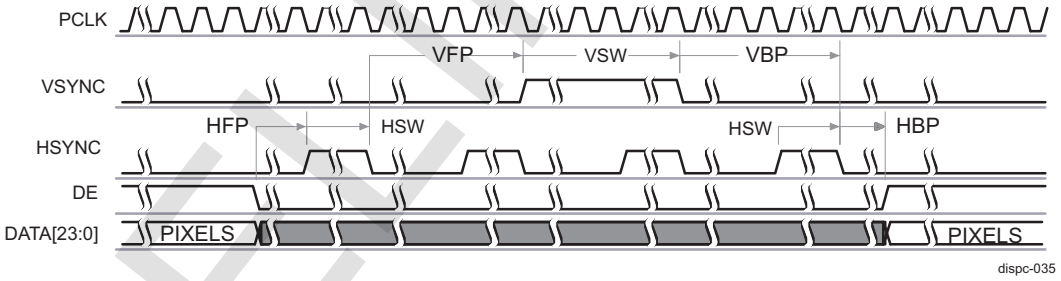
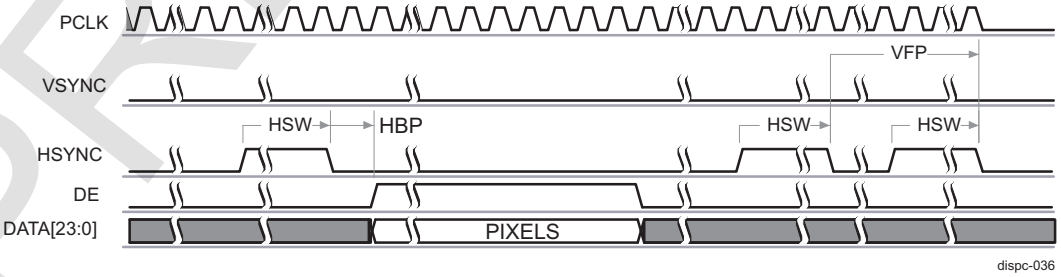


Figure 10-22. Active Matrix Timing Diagram of Configuration 1 (End of Frame)



- Active matrix timing configuration 2
  – DISPC_POL_FREQo[17] ONOFF bit = 1
  – DISPC_POL_FREQo[16] RF bit = 1
    The HSYNC and VSYNC signals are driven on the rising edge of PCLK.

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– DISPC_POL_FREQo[15] IEO = 1
  The DE signal is active low.
– DISPC_POL_FREQo[14] IPC = 1
  The pixel data is driven on the falling edge of PCLK.
– DISPC_POL_FREQo[13] IHS = 1
  The HSYNC signal is active low.
– DISPC_POL_FREQo[12] IVS = 1
  The VSYNC signal is active low.

Figure 10-23. Active Matrix Timing Diagram of Configuration 2 (Start of Frame)

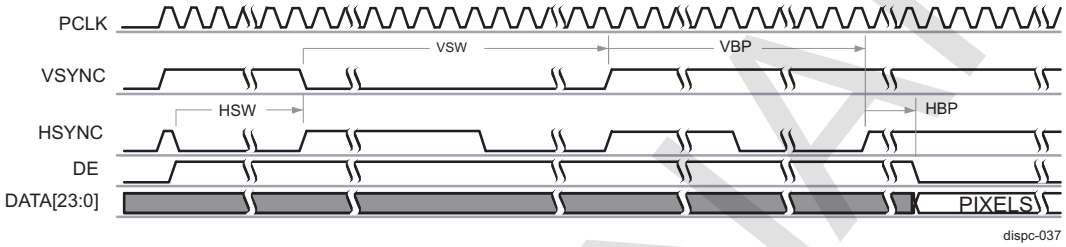


Figure 10-24. Active Matrix Timing Diagram of Configuration 2 (Between Lines)

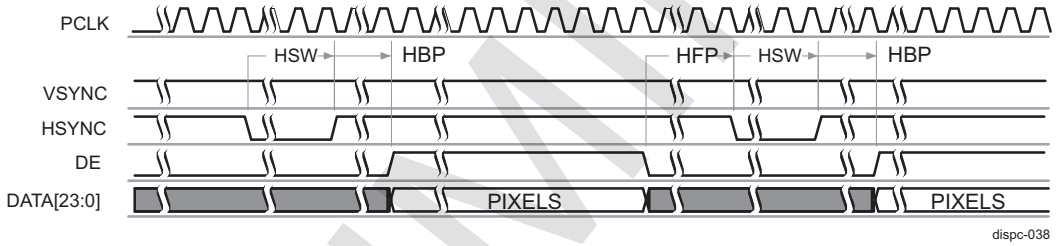


Figure 10-25. Active Matrix Timing Diagram of Configuration 2 (Between Frames)

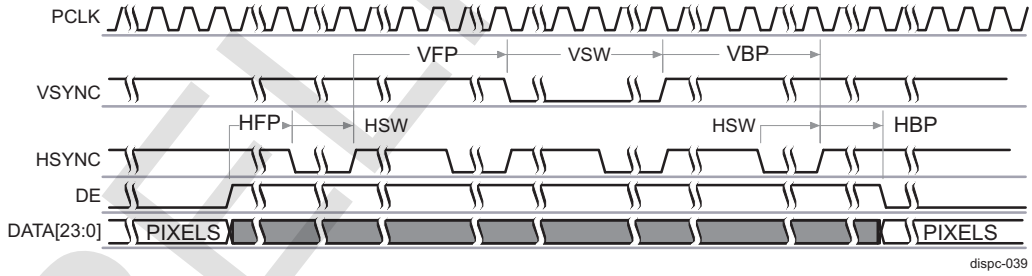
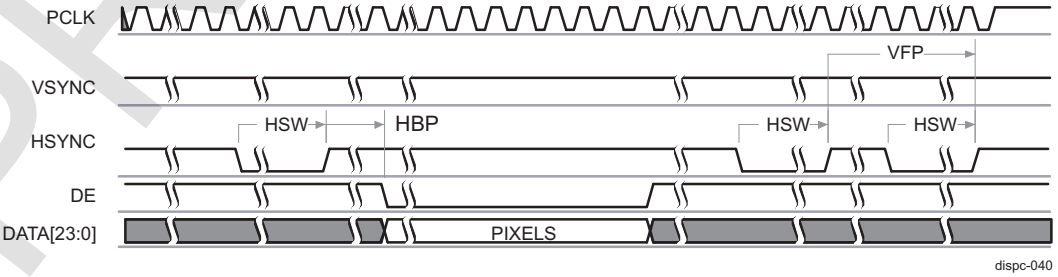


Figure 10-26. Active Matrix Timing Diagram of Configuration 2 (End of Frame)



- Active matrix timing configuration 3
  – DISPC_POL_FREQo[17] ONOFF bit = 1
  – DISPC_POL_FREQo[16] RF bit = 1

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The HSYNC and VSYNC signals are driven on the rising edge of PCLK.

– DISPC_POL_FREQo[15] IEO = 0
  The DE signal is active high.
– DISPC_POL_FREQo[14] IPC = 0
  The pixel data are driven on the rising edge of PCLK.
– DISPC_POL_FREQo[13] IHS = 0
  The HSYNC signal is active high.
– DISPC_POL_FREQo[12] IVS = 0
  The VSYNC signal is active high.

Figure 10-27. Active Matrix Timing Diagram of Configuration 3 (Start of Frame)

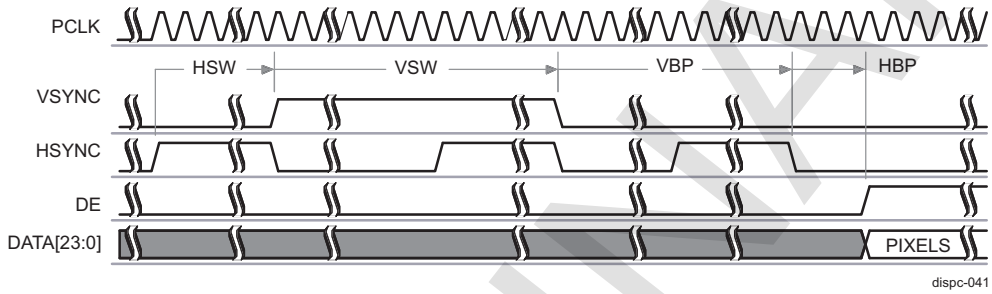

Figure 10-28. Active Matrix Timing Diagram of Configuration 3 (Between Lines)

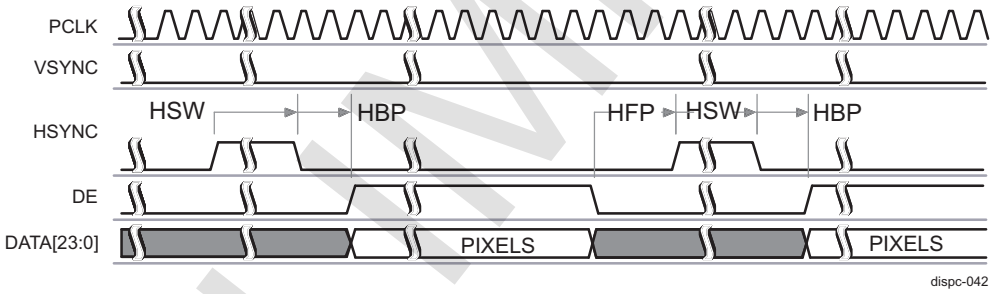

Figure 10-29. Active Matrix Timing Diagram of Configuration 3 (Between Frames)

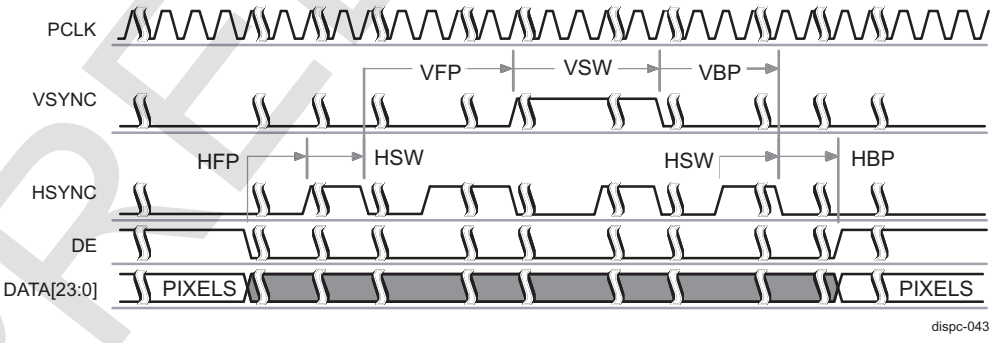

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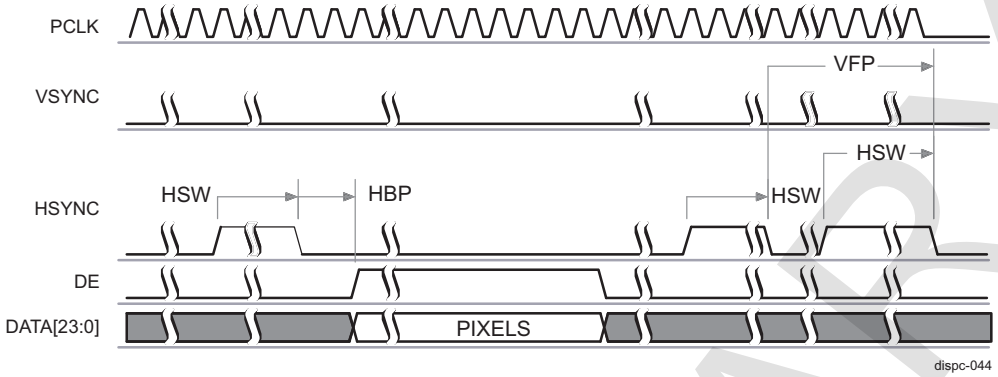
Figure 10-30. Active Matrix Timing Diagram of Configuration 3 (End of Frame)



- Passive matrix timing configuration
  - DISPC_POL_FREQo[17] ONOFF bit = 0
  - DISPC_POL_FREQo[16] RF bit = 0
    The HSYNC and VSYNC signals are driven on the opposite edge of PCLK from the pixel data.
  - DISPC_POL_FREQo[15] IEO = 0
    The DE signal is active high.
  - DISPC_POL_FREQo[14] IPC = 0
    The pixel data are driven on the rising edge of PCLK.
  - DISPC_POL_FREQo[13] IHS = 0
    The HSYNC signal is active high.
  - DISPC_POL_FREQo[12] IVS = 0
    The VSYNC signal is active high.

Figure 10-31. Passive Matrix Timing Diagram (Start of Frame)

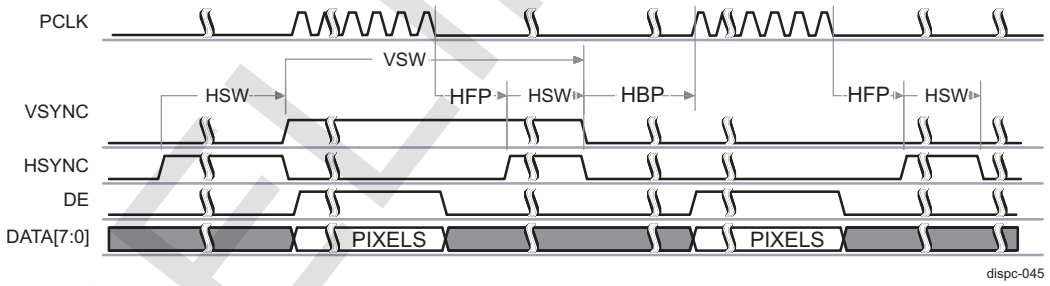


Figure 10-32. Passive Matrix Timing Diagram (Between Lines)

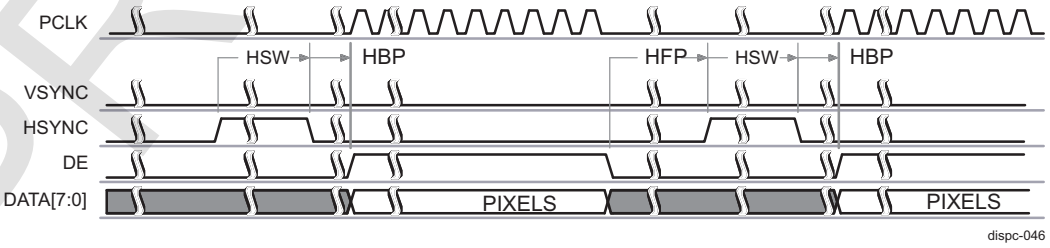


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Figure 10-33. Passive Matrix Timing Diagram (Between Frames)

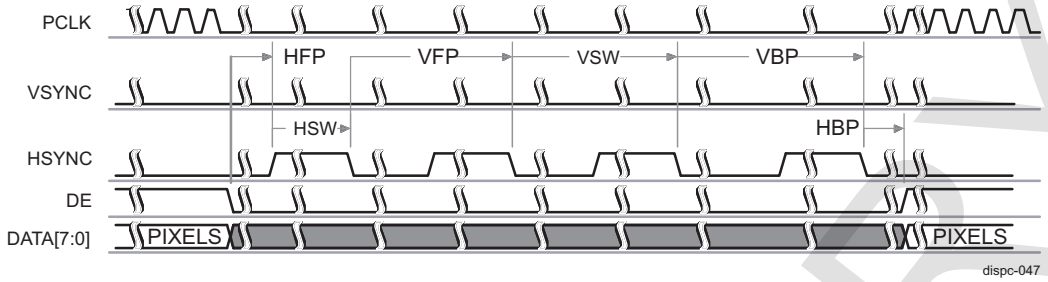
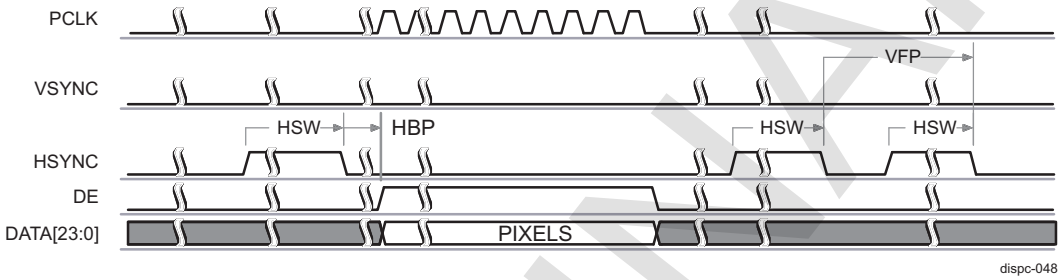


Figure 10-34. Passive Matrix Timing Diagram (End of Frame)



10.2.2.3 TV Output and Data Format for the Parallel Interface

This section describes the TV output pixel data bus for the parallel interface.

The TV pixel data interface is a 30-bit RGB interface. Only the MSB part of each color component is connected to the DSS boundary: R[9:2], G[9:2], B[9:2]. The output of the data is synchronized to the data request signal (HDMI_M_DE) from the HDMI encoder.

Figure 10-35 describes the TV output pixel data format.

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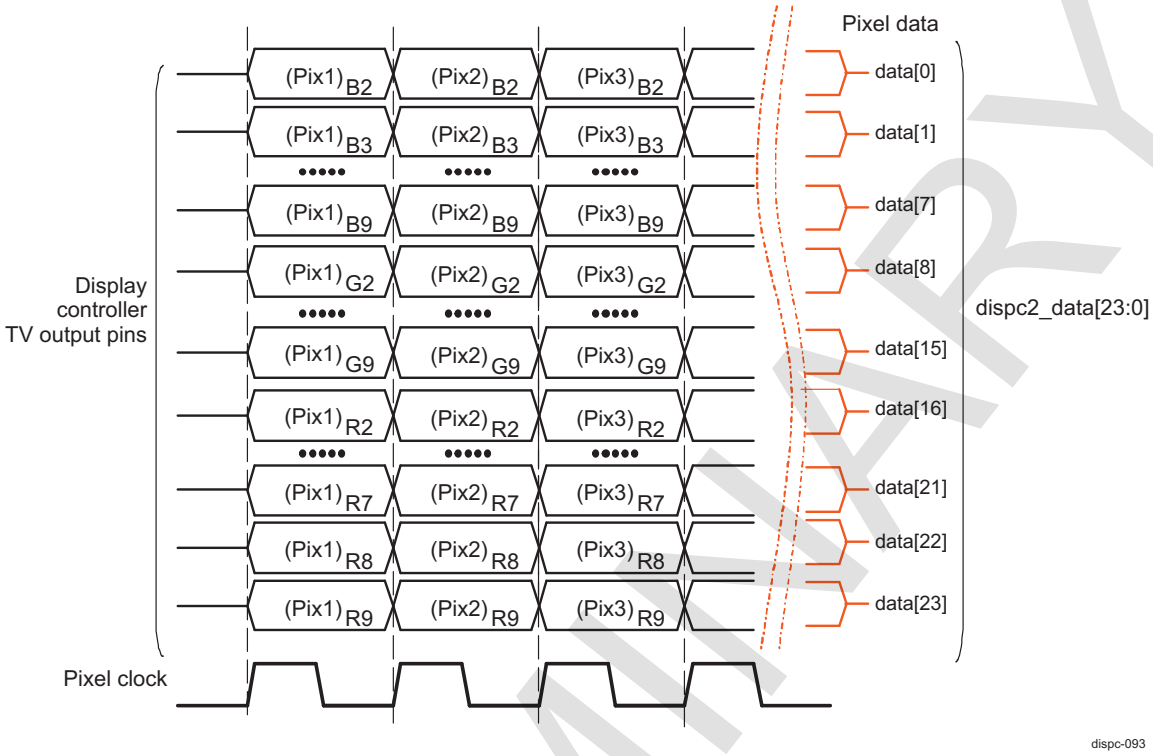
Figure 10-35. TV Output Pixel Data



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10.2.3 Display Controller Integration

This section describes the DISPC integration in the device. The complete details about clocks, resets are detailed in the Section 10.1, *Display Subsystem Overview*.

Figure 10-36. Display Controller Integration

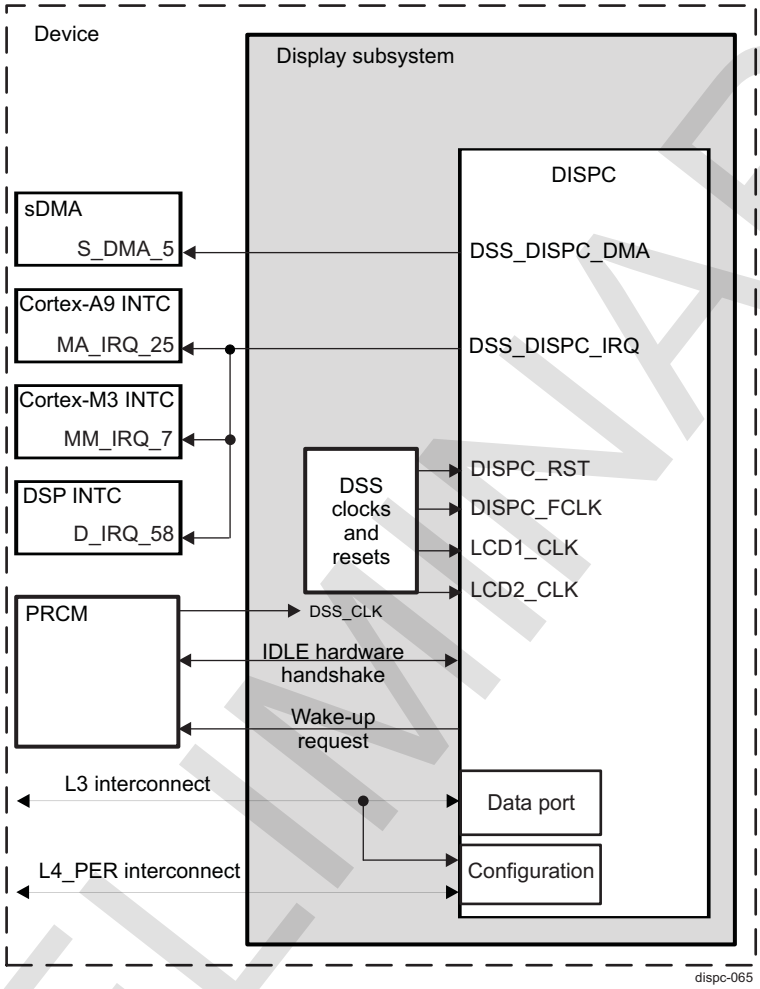

Table 10-22 and Table 10-23 list the integration attributes and clock and resets, respectively.

Table 10-24 summarize the integration of the module in the device.

Table 10-22. Integration Attributes

Module Instance	Attributes	
	Power Domain	Interconnect
DISPC	PD_DSS	L3 for data transfer L4_PER for configuration

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Table 10-23. Clocks and Resets

Clocks				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
DISPC	DISPC_FCLK	DSS_CLK/PLL1_CLK1/PLL2_CLK1/PLL3_CLK1	PRCM/PLLs	Functional clock for the DISPC logic. For multiplexing description and frequency ratings, see Section 10.1.2.1, *DSS Clocks*.
	LCD1_CLK	DSS_CLK/PLL1_CLK1	PRCM/PLL1	Clock used to generate the divided pixel clock for the primary LCD interface. For multiplexing description and frequency ratings, see Section 10.1.2.1, *DSS Clocks*.
	LCD2_CLK	DSS_CLK/PLL2_CLK1	PRCM/PLL2	Clock used to generate the divided pixel clock for the secondary LCD interface. For multiplexing description and frequency ratings, see Section 10.1.2.1, *DSS Clocks*.
Resets				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
DISPC	DISPC_RST	DISPSS_RST	PRCM/DSS	Hardware reset is coming form PRCM, or via a software reset performed at DSS level. For the tree reset description, see .Section 10.1.2.2, *DSS Resets.*

NOTE: If video mode is used, the VPn_PCLK and VPn_CLK clocks must be generated using a CLKIN4DDR clock.

Table 10-24. Hardware Requests

Interrupt Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
DISPC	DSS_DISPC_IRQ	MM_IRQ_	Cortex-M3	Display controller interrupt. For information about Cortex-M3 interrupt control, see Chapter 7.
	DSS_DISPC_IRQ	D_IRQ_58	DSP	Display controller interrupt. For information about DSP interrupt control, see Chapter 5.
	DSS_DISPC_IRQ	MA_IRQ_25	Cortex-A9	Display controller interrupt. For information about Cortex-A9 interrupt control, see Chapter 4.

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Table 10-24. Hardware Requests (continued)

DMA Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
DISPC	DSS_DISPC_DMA	S_DMA_5	System DMA	The line trigger signal informs the sDMA that a programmable number of lines are output to the LCD, and that the system memory can be updated. For more details, see Section 10.2.4.5, *sDMA Requests*.

NOTE:

- For a description of interrupt sources, see Section 10.2.4.4, *Interrupt Requests*.
- For a description of DMA sources, see Section 10.2.4.5, *sDMA Requests*.

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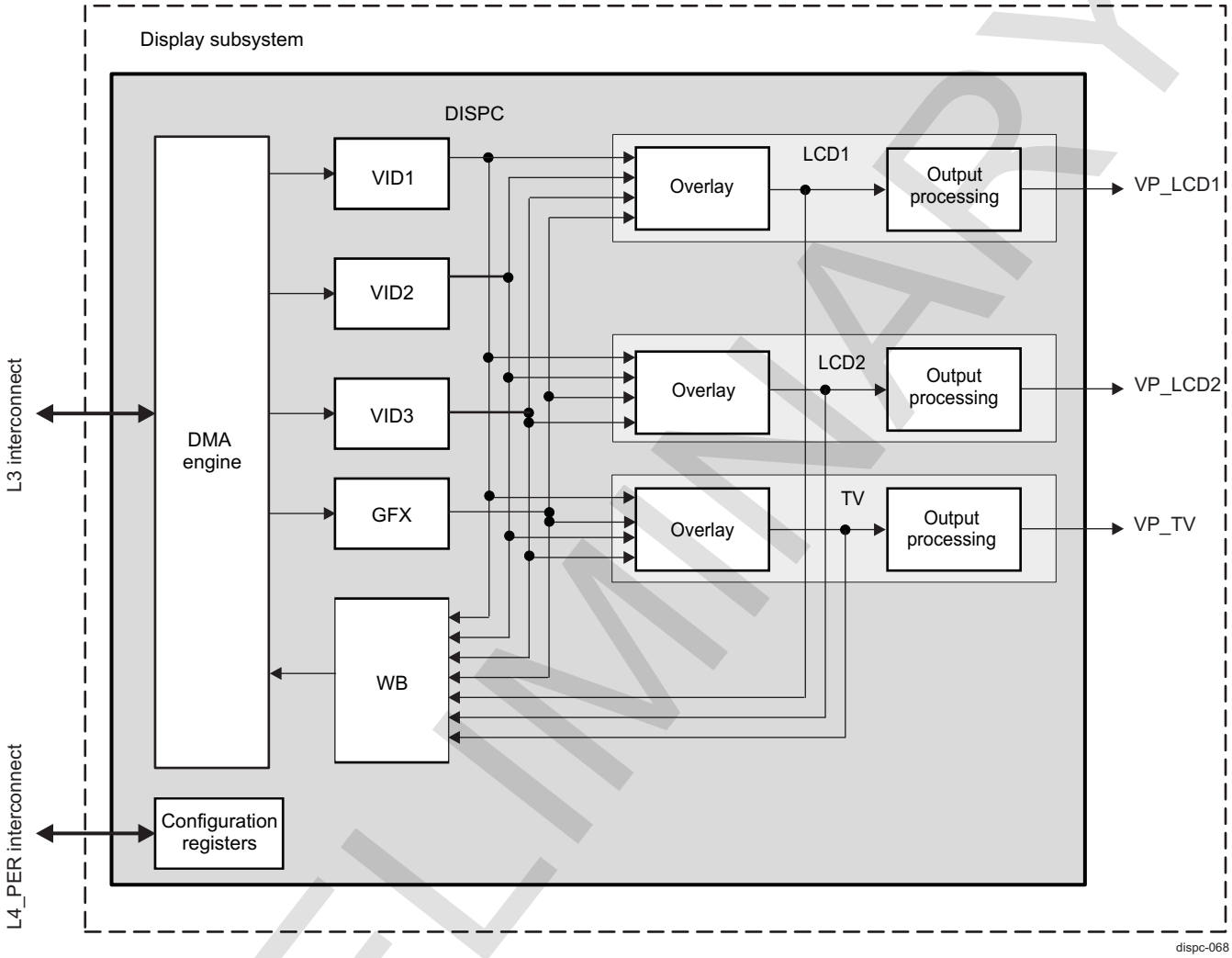
10.2.4 Display Controller Functional Description

The DISPC can read and display the encoded pixel data stored in memory (see Figure 10-37).

Figure 10-37. DISPC Architecture Overview



The DISPC can read and display the encoded pixel data stored in memory and write the output of one of the overlays or one of the pipelines into system memory.

Several processes can be configured to manage the graphics pipeline (palette, antiflicker) and video pipelines (VC-1, color space conversion, scaling, overlay, and transparency ...).

The data coming out of a pipeline is sent to one of the three outputs depending on user configuration. An overlay manager manages inputs of multiple pipelines. Timings user configuration for LCD and TV are available.

The DISPC allows capturing of one output of the pipeline or overlay manager to redirect it into the WB pipeline. It allows to take benefit of the hardware processing available inside the DISPC like color space conversion, rescaling, compositing, etc., to perform memory-to-memory transfer with data processing.

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10.2.4.1 Clock Configuration

The PCLK frequency for each LCD output is derived from a dedicated input clock: LCD1_CLK and LCD2_CLK for the primary and secondary LCD outputs, respectively. Each input clock is divided by the values of the DISPC_DIVISORo[23:16] LCD bit field and then the DISPC_DIVISORo[7:0] PCD bit field independently for each LCD pixel clock (see Figure 10-38). LCD1_PCLK and LCD2_PCLK are independent.

LCD1_PCLK = (LCD1_CLK/ LCD1) / PCD1

LCD2_PCLK = (LCD2_CLK/ LCD2) / PCD2

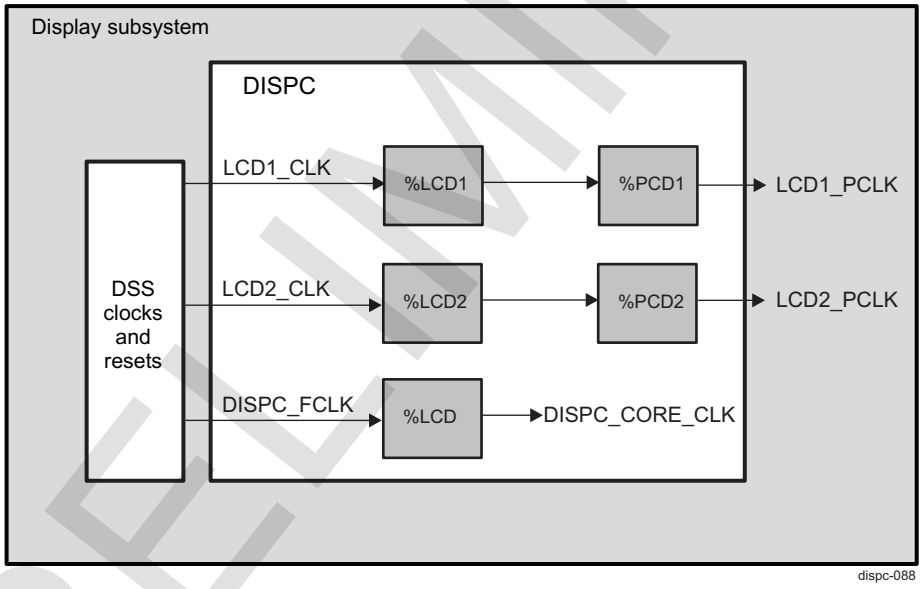
The functional clock of the DISPC (DISPC_CORE_CLK) is derived from DISPC_FCLK by an independent divisor. The dividing value is set in the DISPC_DIVISOR[23:16] LCD bit field.

NOTE: DISPC_CORE_CLK must be higher than or equal to the LCD1_PCLK, LCD2_PCLK, and TV_CLK clocks.

For more information about the DISPC clocks and frequency ratings, see Section 10.1.2.1, *DSS Clocks*.

For backward compatibility, the divisor value LCD can be set to the value of LCD1. To enable this functionality, the DISPC_DIVISOR[0] ENABLE bit must be set to 1.

Figure 10-38. DISPC Clock Tree Overview



10.2.4.2 Software Reset

To perform a software reset on the DISPC, set the DISPC_SYSCONFIG[1] SOFTRESET bit to 0x1. The DISPC_SYSSTATUS[0] RESETDONE bit indicates that the software reset is complete when its value is 0x1. When the software reset completes, the DISPC_SYSCONFIG[1] SOFTRESET bit is automatically reset. Software must ensure that the software reset completes before doing DISPC operations.

10.2.4.3 Power Management

The DISPC supports the MStandby/Wait, IdleReq/SidleAck, and wake-up protocols as defined in PRCM chapter.

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10.2.4.3.1 Idle Mode

The DISPC supports no-idle mode, force-idle mode, and smart-idle mode. The mode can be selected by programming the appropriate value in the DISPC_SYSCONFIG[4:3] SIDLEMODE bit field.

Condition of assertion of SIdleAck signal:

- In no-idle mode: In this mode, SIdleAck is never asserted.
- In force-idle mode: In this mode, SIdleAck is asserted unconditionally with a 1-configuration port interface clock cycle delay with respect to IdleReq assertion.

NOTE: A proper use of force-idle mode assumes that no interrupt need to be generated.

- In smart-idle mode: In this mode, SIdleAck is asserted when all at least the following conditions are satisfied:
  - No interrupt is pending.
  - The DISPC no longer uses the interface clock for the slave port.

Once SIdleAck is asserted:

- The DISPC interface lock used by the slave port may be shut down at any time.
- Any transactions on the configuration port (L4_PER interconnect) are ignored.

The condition of deassertion of SIdleAck signal are:

- In force-idle mode: In this mode, SIdleAck is deasserted with a 1-configuration port interface clock cycle delay with respect to IdleReq deassertion.
- In smart-idle mode: In this mode, SIdleAck is deasserted with a 1-configuration port interface clock cycle delay with respect to IdleReq deassertion.

Once SIdleAck is released, the DISPC is fully operational and a DMA request can be processed normally.

10.2.4.3.2 StandBy Mode

The DISPC supports the no-standby mode, the force-standby mode and a single smart-standby mode. The mode is set in MIDLEMODE field DISPC_SYSCONFIG[13:12]. The functional clock is always active if the module is enabled. The L3 clock can be shut down at any time independently of the status of MStandby.

The condition of assertion of MStandby signal are:

- In no-standby mode: In this mode, MStandby is never asserted.
- In force-standby mode: In this mode, MStandby is asserted when the module is disabled.
- In smart-standby: In the case of one of the following conditions:
  - GFX pipeline is disabled, or GFX pipeline is enabled but the data fetch is completed for GFX window, or GFX pipeline is enabled and the data fetch did not complete and data in the DMA buffer is greater than high threshold value.
  - VID1 pipeline is disabled, or VID1 pipeline is enabled but the data fetch is completed for VID1 window, or VID1 pipeline is enabled and the data fetch did not complete and data in the DMA buffer is greater than high threshold value.
  - VID2 pipeline is disabled, or VID2 pipeline is enabled but the data fetch is completed for VID2 window, or VID2 pipeline is enabled and the data fetch did not complete and data in the DMA buffer is greater than high threshold value.
  - VID3 pipeline is disabled, or VID3 pipeline is enabled but the data fetch is completed for VID3 window, or VID3 pipeline is enabled and the data fetch did not complete and data in the DMA buffer is greater than high threshold value.
  - WB pipeline is disabled, or WB pipeline is enabled but the data store to memory is completed for WB picture, or WB pipeline is enabled and the data storage did not complete but data in the DMA buffer is lower than low threshold value.

MStandby signal asserts whenever all five events have occurred or the DISPC is disabled. While the MStandby is asserted, the DISPC does not generate any transaction on the L3 master port.

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The condition of deassertion of the MStandby signal are:

- In force-standby mode: In this mode, MStandby is deasserted only when the DISPC is enabled.
- In smart-standby mode: In the case of one of the following conditions:
  - GFX pipeline is enabled and the data fetch did not complete for GFX window and the data in the DMA buffer is less than low threshold value.
  - VID1 pipeline is enabled and the data fetch did not complete for VID1 window and the data in the DMA buffer is less than low threshold value.
  - VID2 pipeline is enabled and the data fetch did not complete for VID2 window and the data in the DMA buffer is less than low threshold value.
  - VID3 pipeline is enabled and the data fetch did not complete for VID3 window and the data in the DMA buffer is less than low threshold value.
  - WB pipeline is enabled and the data store did not complete for WB picture and the data in the DMA buffer more than high threshold value.

Detection of the deassertion conditions assumes that the interface clocks are active.

10.2.4.3.3 Wakeup

The DISPC supports wake-up signaling. The mode can be selected by programming the appropriate value in the DISPC_SYSCONFIG[2] ENAWAKEUP bit. The SWakeUp signal is asynchronous so it does not require the interface clock.

The conditions of assertion of the SWakeUp signal are:

- GFX pipeline is enabled and the data fetch did not complete for the GFX window and the data in DMA buffer are less than low threshold value.
- VID1 pipeline is enabled and the data fetch did not complete for the VID1 window and the data in DMA buffer are less than low threshold value.
- VID2 pipeline is enabled and the data fetch did not complete for the VID2 window and the data in DMA buffer are less than low threshold value.
- VID3 pipeline is enabled and the data fetch did not complete for the VID3 window and the data in DMA buffer are less than low threshold value.
- WB pipeline is enabled and the data in DMA buffer are more than high threshold value.
- The last pixel displayed into LCD1 panel if it is not the last frame
- The last pixel displayed into LCD2 panel if it is not the last frame
- The last pixel displayed into TV panel if it is not the last frame

SWakeUp signal is asserted whenever any one of eight events occurs and IdleAck is asserted.

When one of the active pipelines reaches the low threshold and must refill its DMA buffer for the current frame, all other pipelines refill their own DMA buffer even if their low threshold has not been reached. The DISPC_CONFIG1[17] BUFFERFILLING bit field is used to increase the probability that the time increases, where there is no access to the L3 interconnect.

The condition of deassertion of SWakeUp signal is:

- Immediately after deassertion of IdleReq

10.2.4.4 Interrupt Requests

Table 10-25 details the interrupts generated for the DISPC.

The interrupt line, DSS_DISPC_IRQ, indicates when one or more events are detected by the hardware. Each event is independently maskable by setting the DISPC_IRQENABLE register.

To check when a particular interrupt event occurs and to reset a particular event, the DISPC_IRQSTATUS register must be accessed. This register regroups all the status of the module internal events that generate an interrupt (read 0: No interrupt occurred; read 1: Interrupt occurred; write 1: Status bit reset). See *Display Subsystem Register Manual*, for more information on checking and clearing interrupt events.

Table 10-25 lists the DISPC interrupt events.

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Table 10-25. DISPC Interrupts

Interrupt Name	Description
FRAMEDONE1_IRQ	Frame Done for LCD1 output: Active frame related to the LCD1 has completed and LCD1 output of the DISPC is disabled.
FRAMEDONE2_IRQ	Frame Done for LCD2 output: Active frame related to the LCD2 has completed and LCD2 output of the DISPC is disabled.
FRAMEDONETV_IRQ	Frame Done for TV output: Active frame related to the TV output has completed and TV output of the DISPC is disabled.
FRAMEDONEWB_IRQ	Frame Done for WB output: Active frame related to the WB has completed. First, it is used when the WB channel is connected to one of the pipelines to determine when the memory-to-memory transfer through DISPC is completed. Second, it is used when the WB channel is connected to one of the overlay output in nonreal-time mode to determine when the memory-to-memory transfer with overlay processing is completed.
VSYNC1_IRQ	VSYNC for primary LCD output: VSYNC interrupt for the primary LCD has occurred at the end of the frame.
VSYNC2_IRQ	VSYNC for secondary LCD output: VSYNC interrupt for the secondary LCD has occurred at the end of the frame.
EVSYNC_EVEN_IRQ	VSYNC for even field: EVSYNC_EVEN interrupt has occurred at the end of the frame (EVSYNC received and the field polarity is even) (VENC/HDMI)
EVSYNC_ODD_IRQ	VSYNC for odd field: EVSYNC_ODD interrupt has occurred at the end of the frame(EVSYNC received and the field polarity is odd) (VENC/HDMI)
ACBIASCOUNTSTATUS1_IRQ	AC Bias Count Status for LCD1 output: AC Bias transition counter has decremented to 0.
ACBIASCOUNTSTATUS2_IRQ	AC Bias Count Status for LCD2 output: AC Bias transition counter has decremented to 0
PROGRAMMEDLINENUMBER_IRQ	Programmed Line Number: The primary LCD has reached the user programmed line number.
VID1ENDWINDOW_IRQ	End of the VID1 window: The DMA engine has fetched all the data from memory for the VID1 for the current frame.
VID2ENDWINDOW_IRQ	End of the VID2 window: The DMA engine has fetched all the data from memory for the VID2 for the current frame.
VID3ENDWINDOW_IRQ	End of the VID3 window: The DMA engine has fetched all the data from memory for the VID3 for the current frame.
GFXENDWINDOW_IRQ	End of the graphics window: The DMA engine has fetched all the data from memory for the graphics for the current frame.
VID1BUFFERUNDERFLOW_IRQ	VID1 DMA buffer underflow: The input VID1 DMA buffer goes underflow.
VID2BUFFERUNDERFLOW_IRQ	VID2 DMA buffer underflow: The input VID2 DMA buffer goes underflow.
VID3BUFFERUNDERFLOW_IRQ	VID3 DMA buffer underflow: The input VID3 DMA buffer goes underflow.
WBBUFFEROVERFLOW_IRQ	WB DMA buffer overflow: The output WB DMA buffer goes overflow. It cannot occur when WB channel is used in memory-to-memory transfer mode but only in capture mode. In capture mode the timings are defined by the timer associated with the output. In memory-to-memory mode, there is timing constraint.
GFXBUFFERUNDERFLOW_IRQ	GFX DMA buffer underflow: The input Graphics DMA buffer goes underflow.
PALETTEGAMMALOADING_IRQ	Palette/Gamma Table Loading: The palette/Gamma table in the graphics pipeline has been loaded using the DISPC DMA engine.
WBUNCOMPLETEERROR_IRQ	The write back buffer has been flushed before been fully drained.
OCPERROR_IRQ	OCP Error: L3 interconnect has sent SResp = ERR

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Table 10-25. DISPC Interrupts (continued)

Interrupt Name	Description
SYNCLOST1_IRQ	Synchronization Lost on LCD1 output: Occurs when VSYNC width/front or back porches are not wide enough to load the pipelines with data (LCD output).
SYNCLOST2_IRQ	Synchronization Lost on LCD2 output: Occurs when VSYNC width/front or back porches are not wide enough to load the pipelines with data (LCD output).
SYNCLOSTTV_IRQ	Synchronization Lost on TV output: Occurs when porches are not wide enough to load the pipelines with data (TV output connected to the video NTSC/PAL encoder).
WAKEUP_IRQ	Wakeup: Occurs when the SWakeUp signal is asserted.

10.2.4.5 sDMA Requests

The DMA synchronization line, DSS_DISPC_DMA, is connected to the sDMA. This DMA request is not a classical one but rather a synchronization signal between the DISPC and sDMA. The sDMA is informed that a programmable number of lines are output to the LCD, and that a system memory can be updated. This request is related to the interrupt event PROGRAMMEDLINENUMBER_IRQ described in Table 10-25. This allows the sDMA channel to be synchronized with the display subsystem internal DMA controller.

In other words, it allows to synchronize a memory-to-memory frame buffer update based on the scan line of the frame buffer in system memory (SDRAM or SRAM) by the DISPC. The DSS_DISPC_DMA DMA request is generated at a programmable line number defined in the DISPC_LINE_NUMBER[10:0] LINENUMBER bit field. This process allows an application to use a single frame buffer and update it after a certain number of lines has been read by the DISPC.

10.2.4.6 DMA Engine

The DMA engine:

- Supplies data (encoded pixel data, palette, and gamma curve) from memories to GFX, VID1, VID2, and VID3 pipelines through the interconnect based on the configuration of the DISPC and pipelines settings.
- Stores (encoded pixel data) from GFX/VID pipelines or overlays to memories through the WB pipeline and interconnect based on the configuration of the DISPC and WB pipeline settings.

Each pipeline has a dedicated buffer and a channel with independent settings. The default size and allocation of the DMA buffer is detailed in Table 10-26. Each DMA buffer is divided into two spaces, top and bottom buffer. Depending on the application, a DMA buffer space can be associated to a pipeline or merged with other spaces. The total number of spaces for each individual pipeline is from 0 (pipeline inactive) to number of pipelines ×2 (in that case, all the DMA buffers are associated to a single pipeline). The sum of the number of spaces allocated for each pipeline must not be greater than the maximum number of spaces available. The correct number of spaces must be allocated to ensure no underflow. The spaces allocated to each pipeline must be greater than or equal to the minimum number of spaces required to support the throughput and the system latency. The space assignation are done in the DISPC_GLOBAL_BUFFER register.

Figure 10-39 shows an overview of the DMA engine.

Table 10-26. DMA Buffer Size

Pipelines	DMA Buffer Size
GFX	2 lines × 640 × 128 bits
VID1	2 lines × 1024 × 128 bits
VID2	2 lines × 1024 × 128 bits
VID3	2 lines × 1024 × 128 bits
WB	2 lines × 1024 × 128 bits

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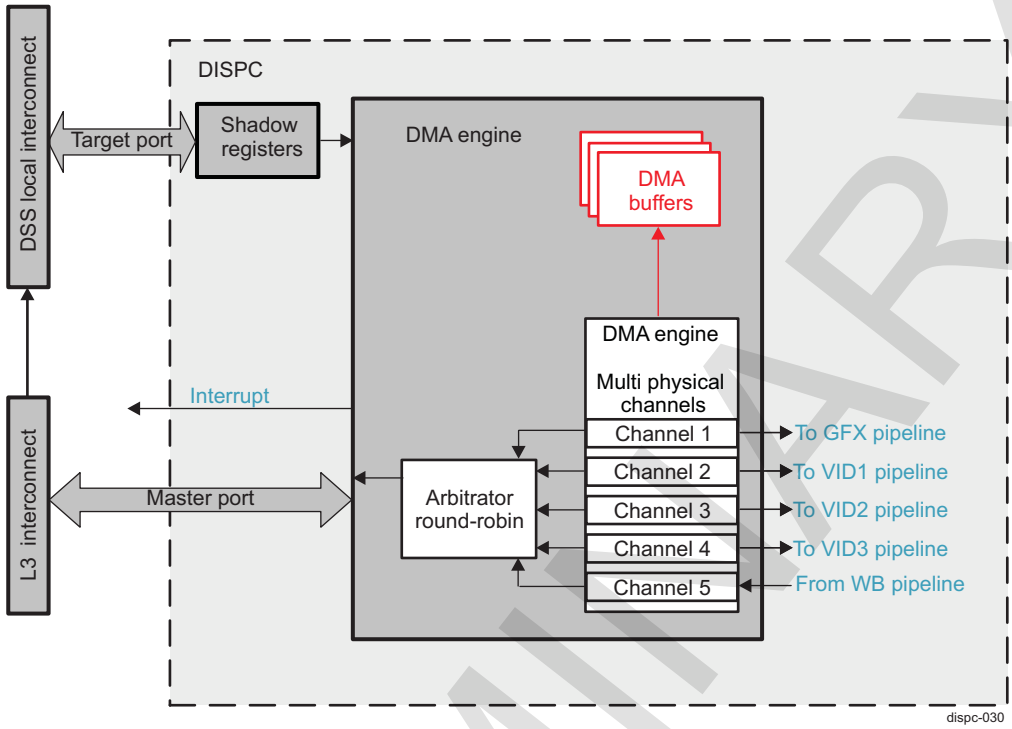
Figure 10-39. DMA Engine Overview



10.2.4.6.1 Addressing and Bursts

For each line to be fetched/stored, the DMA engine:

- Calculates the pixel address.
- Aligns the address.
- Defines the burst structure:
  - Type of the burst (1D or 2D burst structure).
  - Length of the burst.

The DMA engine generates scan addresses to read/write data from/to system memory. The base address defines the start address of the first pixel, then the address is incremented based on the number of pixels per line, offset between two consecutive lines and number of lines. The byte address of each pixel in the frame buffer in the system memory is determined by:

Pixel address = Base address + x × bpp + (y × ((width × bpp) + increment))

where:

- Base address corresponds to the base address (for YUV–NV12 format) defined by:
  - DISPC_GFX_BA_0[31:0], BA bit field
  - DISPC_GFX_BA_1[31:0], BA bit field
  - DISPC_VIDp_BA_0[31:0], BA bit field
  - DISPC_VIDp_BA_1[31:0], BA bit field
  - DISPC_VIDp_BA_UV_0[31:0], BA bit field
  - DISPC_VIDp_BA_UV_1[31:0], BA bit field
- bpp corresponds to the number of bits per pixel defined by the DISPC_GFX_ATTRIBUTES[4:1] FORMAT bit field or DISPC_VIDp_ATTRIBUTES[4:1] FORMAT bit field.
- width corresponds to the number of pixels per line defined by DISPC_GFX_SIZE[10:0] SIZEX+1 bit field or DISPC_VIDp_SIZE[10:0] SIZEX+1 bit field.
- increment corresponds to the number of bytes to skip between two contiguous lines defined by

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DISPC_GFX_ROW_INC[31:0] ROWINC –1 bit field or DISPC_VIDp_ROW_INC[31:0] ROWINC –1 bit field.

- x corresponds to the pixel position on the x-axis.
- y corresponds to the pixel position on the y-axis.

NOTE: For YUV format, the pixel values are defined in two separated buffers (Y and UV). The Y buffers base address are defined in the DISPC_VIDp_BA_j[31:0] BA bit field. The UV buffers base address are defined in the DISPC_VIDp_BA_UV_j[31:0] BA bit field.

Table 10-27 resumes the registers settings for a simple access of a picture in system memory.

Table 10-27. Register Settings for Accessing Image in Internal Memory

Registers	Value
DISPC_GFX_BA_j/DISPC_VIDp_BA_j/DISPC_WB_BA_j	PBA, the physical base address of image in the memory
DISPC_VIDp_BA_UV_j/DISPC_WB_BA_UV_j	PBA, the physical base address of UV buffers image in the memory
DISPC_GFX_PIXEL_INC / DISPC_VIDp_PIXEL_INC/DISPC_WB_PIXEL_INC	1 or other in pixel incremental value
DISPC_GFX_ROW_INC /DISPC_VIDp_ROW_INC/DISPC_WB_ROW_INC	1 or other in row incremental value

An interconnect request, 128-bits, corresponds to one or several pixels depending on bits per pixels. Therefore, the DMA engine determines the appropriate burst sequence to optimize each new line fetching/storing. The DMA engine must prevent a single burst from crossing two lines. The DMA engine supports bursts of 2 × 128 bits, 4 × 128 bits, and 8 × 128 bits. The default burst size at reset time is 8 × 128 bits. The maximum burst size can be configured for each pipeline by setting the DISPC_GFX_ATTRIBUTES[7:6] BURSTSIZE bit field or DISPC_VIDp_ATTRIBUTES[15:14] BURSTSIZE bit field. Because the burst size must be aligned to the burst boundary, in case of misalignment, the DMA engine may issue single and/or smaller burst requests. Two types of burst are present:

- 1D-burst is used if the fetch/storage is linear in memory through the TILER. There is no rotation of the frame buffer. The frame buffer is not tiled.
- 2D-burst is used if the frame buffer is tiled.

Even if the DISPC_VIDp_ROW_INC does not equal 1, the 2D-burst can be selected by the user. It is used when the DISPC is configured to read one field of a frame by accessing only the even and odd lines.

NOTE: The burst size is initialized once at configuration and can be changed when the DISPC is disabled.

10.2.4.6.2 DMA Buffers

10.2.4.6.2.1 READ DMA Buffers (GFX and VID Pipelines)

When the vertical front porch (VFP) period starts after the last horizontal front porch (HFP) of the last line or the external VSYNC is received, the DMA buffers are flushed according to the selected output associated with the pipeline. The DMA engine restarts fetching data from the memory through the L3 Interconnect. Enabling/disabling the DISPC flushes the DMA buffers (except WB DMA buffers).

Programmable high and low thresholds, independent for each DMA buffer, are used by the DMA engine to start and stop requesting data to the L3 interconnect.

- When low threshold (set in the DISPC_GFX_BUF_THRESHOLD[15:0] BUFLOWTHRESHOLD bit field or DISPC_VIDp_BUF_THRESHOLD[15:0] BUFLOWTHRESHOLD bit field) is reached, the DMA engine starts a request on the L3 interconnect to fill the DMA buffer.
- When high threshold (set in the DISPC_GFX_BUF_THRESHOLD[31:16] BUFHIGHTHRESHOLD bit field or DISPC_VIDp_BUF_THRESHOLD[31:16] BUFHIGHTHRESHOLD bit field) is reached, the DMA engine stops requesting encoded pixels.

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To avoid underflow at the beginning of a frame and have sufficient encoded pixel data to start some processing, a preloading of the DMA buffer is configurable between a fixed value of bytes or the high threshold value. The preload ensures a minimum number of pixels present in the buffer. When the preload value is reached, the associated channel must start pulling pixels out of the DMA buffer. To enable the preload based on the value entered in the DISPC_GFX_PRELOAD[11:0] PRELOAD bit field or DISPC_VIDp_PRELOAD[11:0] PRELOAD bit field, the DISPC_GFX_BUF_THRESHOLD[11]BUFPRELOAD bit, or DISPC_VIDp_BUF_THRESHOLD[19] BUFPRELOAD bit must be set to 0x0.

NOTE: When self-refresh mode is selected, meaning the data in the DMA buffers are used for multiple frames, and at the end of each frame, the DMA buffers are not flushed.

10.2.4.6.2.2 WRITE DMA Buffer (WB Pipeline)

Two modes are supported by the WB channel, selectable through the DISPC_WB_ATTRIBUTES[19] WRITEBACKMODE bit:

- Capture mode, WRITEBACKMODE bit set to 0: One of the overlay outputs going to LCD or TV outputs is captured and at the same time the data are sent on the output. The WB timings are controlled by the LCD or TV timings.
- Memory-to-memory mode, WRITEBACKMODE bit set to 1: One of the overlay outputs or one of the pipelines is captured in order to perform memory-to-memory transfer with some processing by the DISPC (rescaling, overlaying, color space conversion, etc.)

In capture mode: The WB DMA buffers are flushed when the VFP period starts after the HFP following the last line, or when the external VSYNC is received, depending on which output (LCD/TV) the WB pipeline is capturing data, if the programmed value in DISPC_WB_ATTRIBUTES2[7:0] WBDELAYCOUNT bit field is set to 0. If the programmed value in DISPC_WB_ATTRIBUTES2[7:0] WBDELAYCOUNT bit field is set to N (1:255), the write buffers DMA are flushed N lines later. The DMA engine starts storing data to memory through the L3-based interconnect as soon as enough data is available for the programmed burst size. When enabling/disabling the DISPC, the DMA buffers are flushed. The programmable thresholds low and high are used by the DMA engine to start and stop sending data to the L3 interconnect.

NOTE: If DISPC_WB_ATTRIBUTES2[7:0] WBDELAYCOUNT bit field is set to 0, the WB is reinitialized just at the end of the last line of a frame at the beginning of the VFP signal. To let the WB complete the data write to the external memory, the highest possible value compatible with the vertical blanking period must be set.

In memory-to-memory mode: The WB pipeline is not synchronized to any internal or external timing generator. The WB pipeline stores the output of one of the overlay outputs or one of the pipelines. When enabling/disabling the DISPC, the DMA buffers are flushed. The programmable thresholds low and high are used by the DMA engine to start and stop sending data to the L3 interconnect.

Programmable high and low thresholds are used by the DMA engine to start and stop sending data to the L3 interconnect.

- When high threshold (set in the DISPC_WB_BUF_THRESHOLD[31:16] BUFHIGHTHRESHOLD bit field) is reached, the DMA engines start sending data on the L3 interconnect to empty buffer.
- When low threshold (set in the DISPC_WB_BUF_THRESHOLD[15:0] BUFLOWTHRESHOLD bit field) is reached, the DMA engine stops sending encoded pixels.

At the end of the frame, in order to drain the DMA buffer, some smaller bursts (even single requests) must be issued to completely empty the DMA buffer. To limit the number of interconnect requests from the DISPC, a number of IDLE cycles between requests can be inserted. IDLE cycles can be inserted only when WB is used in memory-to-memory mode. It is ignored when WB is in capture mode.

The number of idle between requests can be activated and determined by :

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- Setting the DISPC_WB_ATTRIBUTES[27] IDLESIZE bit to 0x0 (default value) and entering the number of idles between requests in the DISPC_WB_ATTRIBUTES[31:28] IDLENUMBER bit field. Idle numbers vary from 0 to 15.
- Setting the DISPC_WB_ATTRIBUTES[27] IDLESIZE bit to 0x1, which considers the size of the burst (the field DISPC_WB_ATTRIBUTES[15:14] BURSTSIZE bit field) to determine the number of idles.
  - If BURSTSIZE = 0x0, then idle equals IDLENUMBER (0 to 15).
  - If BURSTSIZE = 0x1, then idle equals IDLENUMBER * 4 (0 to 60).
  - If BURSTSIZE = 0x2, then idle equals IDLENUMBER * 8 (0 to 120).

10.2.4.6.3 Predecimation

The predecimation process consists of downscaling an image by fetching only the necessary pixels in the memory. Vertical and horizontal predecimation are possible:

- Vertical predecimation: The picture store in memory can be predecimated vertically by skipping lines. Burst mode is used to fetch the data when skipping lines. Only the lines that will be used by the DISPC are fetched from memory; the other lines are skipped. The DMA engine sends requests only for the useful lines using 1D burst or 2D burst, depending on the setting. The base address indicates the first valid pixel to fetch from memory. The number of lines to skip is set in the DISPC_GFX_ROW_INC[31:0] ROWINC bit field or DISPC_VIDp_ROW_INC[31:0] ROWINC bit field.

  NOTE: When 2D burst mode is used, the access to data in memory is performed through the TILER module of DMM (see , *TILER*, for more details), and as a result a maximum of one line can be skipped.

- Horizontal predecimation: When fetching data from memory, it is possible to skip 1 out of 2 pixel data containers, up to 1 out of 16 pixel data containers, by setting the DISPC_GFX_PIXEL_INC[7:0] PIXELINC bit field or DISPC_VIDp_PIXEL_INC[7:0] PIXELINC bit field to the number of pixel data containers to skip (n), multiplied by the size of a pixel data container (in bytes), + 1. See the following note for more details.

  NOTE: The restriction to horizontal predecimation is that there is at least one useful pixel per 128-bit request. In that case, the DMA engine uses burst mode instead of singles to optimize the requests in terms of latency and SDRAM efficiency.

  No decimation is supported when the input format is 1, 2, 4, 8 BITMAP.

  For RGB and YUV4:2:0 data formats, each pixel data container in memory holds 1 pixel. Thus, when configuring the PIXELINC bit field, the value of n equals the number of pixels to skip:

  - For RGB format, one pixel data container = 32 bits = 1 pixel
  - For YUV format:
    - One Y pixel data container = 8 bits = 1 pixel
    - One UV pixel data container = 16 bits = 1 pixel

  For YUV4:2:2 format, each 32-bit pixel data container holds the Luma components for 2 pixels and the Chrominance component of 1 pixel (see the graphic representation in Figure 10-40). Therefore, for the valid values of the PIXELINC bit field in the following YUV4:2:2 format, caution must be taken, because n does not equal the number of pixels, but instead the number of pixel data containers to skip:

  - For n = 1, PIXELINC = 5
  - For n = 2, PIXELINC = 9
  - For n = 3, PIXELINC = 13
  - For n = 4, PIXELINC = 17, etc.

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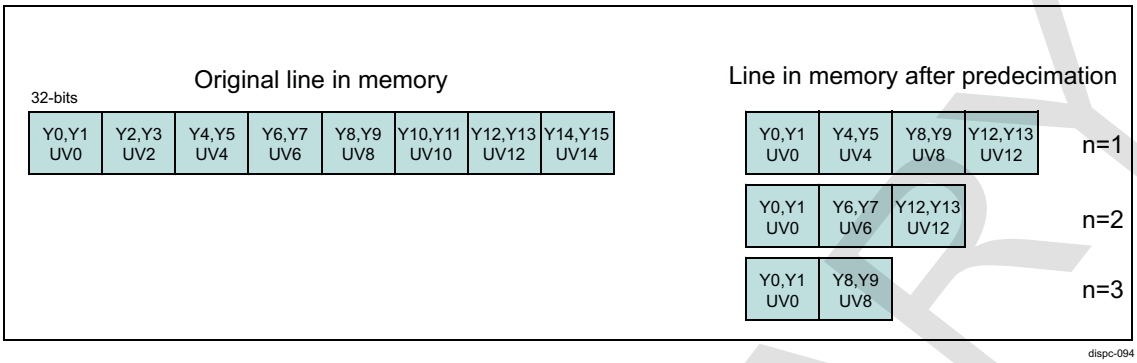
Figure 10-40. YUV4:2:2 Predecimation



10.2.4.6.4 Progressive-to-Interlaced Format Conversion

The DMA engine can be used to perform YUV4:2:0 NV12 progressive-to-interlaced data conversion with 0-degree orientation. This section provides generic approach details.

Two possible configurations are available, depending on the setting of the DISPC_VIDp_ATTRIBUTES[22] DOUBLESTRIDE bit, which defines the stride of each pixel value buffer for the YUV format. The following must be considered for both configurations:

- Bit [31] in the DISPC_VIDn_BA_j and DISPC_VIDn_BA_UV_j[31:0] BA bit fields, and the DISPC_VIDn_ATTRIBUTES[13:12] ROTATION bit field must be set to 0x0 to indicate 0-degree orientation.

Configuration 1 – YUV4:2:0 progressive to interlaced conversion

The DISPC_VIDp_ATTRIBUTES[22] DOUBLESTRIDE bit is set to 0x1. The CbCr container is twice the size of the Y container. All Luma and Chroma lines for even and odd fields are fetched from memory. The scaler unit of the respective pipeline can be used to downscale by 2 (through filtering) the fetched data to create the interlaced output. For more information about the scaler configuration, see Section 10.2.4.10.4, *Scaler Unit*.

Configuration 2 – YUV4:2:0 progressive to YUV4:2:2 interlaced conversion

The DISPC_VIDp_ATTRIBUTES[22] DOUBLESTRIDE bit is set to 0x0. The CbCr container is the same size as the Y container. The DISPC_VIDn_ROW_INC register for the respective pipeline must be configured so that only the Y data is vertically predecimated by 2 (see Section 10.2.4.6.3, *Predecimation*, for more information). The CbCr data must not be predecimated. As a result, only the even Luma lines for the even field and the odd Luma lines for the odd field are fetched from memory. To create the interlaced output, the Chroma lines are all fetched from memory.

10.2.4.6.5 Arbitration

The requests (reads or writes) sent to the L3 interconnect are pipelined and are arbitrated in a round-robin scheme. The default arbitration scheme must be modified by setting the priority attribute of each pipeline as defined in the DISPC_GFX_ATTRIBUTES[14] ARBITRATION bit, DISPC_VIDp_ATTRIBUTES[14] ARBITRATION bit, or DISPC_WB_ATTRIBUTES[14] ARBITRATION bit.

By default, all pipelines have the same priority (normal), which means all pipelines requests are treated in a round-robin order manner. If one or more pipelines require a higher number of requests going to the L3 interconnect, its priority can be moved up to high priority. In this case, the high-priority pipeline is granted access before any pipeline in normal priority. If more than one active pipeline is in high priority, the behavior is the same as all active pipelines in normal priority. Normal active pipelines are not treated until all high active pipelines are finished. The ARBITRATION bit cannot be modified during the entire frame.

This functionality balances the bandwidth of the pipeline depending on its constraint. It can be used to give higher priority to the pipelines with real-time constraints versus non-real-time pipelines. For example, pipelines associated with the LCD output in stall mode must have lower priority than pipelines associated with TV output.

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10.2.4.6.6 DMA Power Modes

10.2.4.6.6.1 Low-Power Mode

Each DMA buffer is divided into two spaces. Each space can be associated with the pipeline or merged with other spaces. The total number of spaces for each individual pipeline is from 0 (pipeline inactive) to the number of pipelines × 2 (in that case all the DMA buffers are associated with a single pipeline). The sum of the number of spaces allocated for each pipeline must not be greater than the maximum available. The correct number of spaces must be allocated to ensure no underflow. The spaces allocated to each pipeline must be greater than or equal to the minimum required to support the throughput and the system latency.

NOTE: When the number of spaces is changed, the thresholds must be reprogrammed to reflect the new DMA buffer configuration.

10.2.4.6.6.2 Ultralow-Power Mode

In low-power mode, the L3 interconnect is used to fill up the DMA buffers to store all the data required to display a full frame. The L3 interconnect is not used to fetch the new pixels for the following frames. The data in the DMA buffer are reused to display on the screen.

The setting of the mode is independent for each pipeline. One pipeline may have all the frame pixels in its DMA buffer and the other pipelines may have to refill their respective DMA buffers along the display scan because the frame buffer is too big to be stored in the DMA buffer.

The DMA buffers can be merged to optimize the L3 interconnect off time. Merging the DMA buffers into a single buffer can be used at the same time to improve ultralow-power mode (see Section 10.2.4.6.6.1), *Low-Power Mode*.

During the time in which the frames are fetched in the internal DMA buffer, MStandby must be asserted if the DISPC_SYSCONFIG[13:12] MIDLEMODE bit field is set to 0x2 (smart-standby mode).

Two ultralow power modes can be entered manually or automatically:

- Self-refresh mode: Starting self-refresh mode is done manually by setting the DISPC_GFX_ATTRIBUTES[15] SELFREFRESH bit or DISPC_VIDp_ATTRIBUTES[15] SELFREFRESH bit to 0x1 after capturing a frame in the DMA buffers. Stopping self-refresh mode is done by setting the SELFREFRESH bit to 0x0.
- Automatic self-refresh mode: By setting the DISPC_GFX_ATTRIBUTES[17] SELFREFRESHAUTO bit or DISPC_VIDp_ATTRIBUTES[17] SELFREFRESHAUTO bit to 0x1, the transition from OFF to ON self-refresh mode is done by hardware after capturing the first frame. The hardware reflects the status of the self-refresh mode by setting the SELFREFRESH bit to 0x1, which means that the data are read inside the DMA buffer without accessing the interconnect and system memory during the frame. Setting the SELFREFRESH bit to 0x0 updates the DMA buffer.

NOTE: The WB pipeline does not support ultralow-power mode.

10.2.4.7 Rotation and Mirroring

The DISPC provides flexible mechanisms for an efficient implementation of rotation using the DISPC, its DMA engine, and the rotation engine of the TILER module. The rotation is handled only through the TILER module, which supplies the encoded pixels to the DISPC.

NOTE: No rotation or mirroring is supported when accessing internal SDRAM directly .

The TILER supports:

- Rotation 0-, 90-, 180-, 270-degree views
- Mirroring

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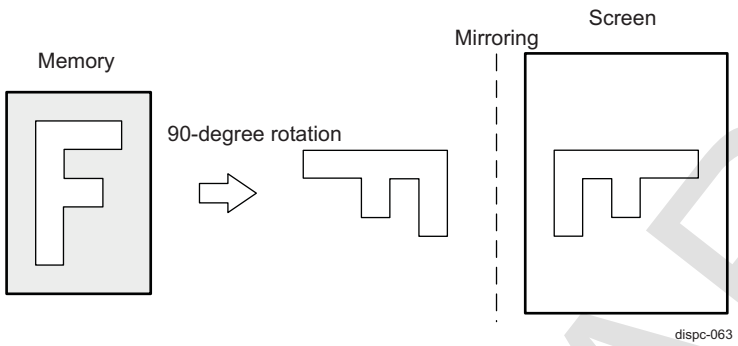
- Any combination of the two previous (for example, Rot-90 + mirroring, etc.)

Figure 10-41. 90-Degree Rotation With Mirroring



When accessing YUV4:2:2 data, each 32-bit value loaded into the DMA buffer can represent either:

- Two consecutive pixels on the same line (for instance, 0-/180-degree rotation)
- Two pixels adjacent vertically (for instance, 90-/270-degree rotation)

The reading from the DMA buffer supports the extraction of the two pixels regardless of the rotation. When the pixels are not consecutive on the same line (90-/270-degree rotation), the chrominance sample of the first pixel of each 32-bit value is duplicated for the second pixel in the same 32-bit value.

The rotation flag DISPC_VIDn_ATTRIBUTES[13:12] ROTATION and the DISPC_VIDn_ATTRIBUTES[4:1] FORMAT bit fields define the processing to extract the pixels from YUV4:2:2 32-bit values. Software must ensure that the settings of the ROTATION and FORMAT bit fields are coherent with the rotation/mirroring defined through the address format in the TILER-specific address map. For more information, see Section 15.2.3.6.2, *TILER Macro-Architecture*, in Section 15.2, *Dynamic Memory Manager*.

Table 10-28 describes the register settings of the DISPC when accessing, rotating, and mirroring an image using the TILER. A physical base address (PBA) for each rotation is determined and set as the buffer address (BA). The row incremental is determined and set in ROW_INC. The value of the pixel increment, PIXEL_INC, is set to 0x1 (contiguous pixels).

Table 10-28. Register Settings for Rotation Using TILER

Rotation	Registers	Rotation With and Without Mirroring
0 degree	DISPC_GFX_BA_j/DISPC_VIDp_BA_j/DISPC_WB_BA_j	PBA0
	DISPC_GFX_PIXEL_INC /DISPC_VIDp_PIXEL_INC/DISPC_WB_PIXEL_INC	1 to 16
	DISPC_GFX_ROW_INC /DISPC_VIDp_ROW_INC/DISPC_WB_ROW_INC	ROW0
90 degrees	DISPC_GFX_BA_j /DISPC_VIDp_BA_j/DISPC_WB_BA_j	PBA90
	DISPC_GFX_PIXEL_INC / DISPC_VIDp_PIXEL_INC/DISPC_WB_PIXEL_INC	1 to 16
	DISPC_GFX_ROW_INC / DISPC_VIDp_ROW_INC/DISPC_WB_ROW_INC	ROW90
180 degrees	DISPC_GFX_BA_j /DISPC_VIDp_BA_j/DISPC_WB_BA_j	PBA180
	DISPC_GFX_PIXEL_INC /DISPC_VIDp_PIXEL_INC/DISPC_WB_PIXEL_INC	1 to 16
	DISPC_GFX_ROW_INC / DISPC_VIDp_ROW_INC/DISPC_WB_ROW_INC	ROW180
270 degrees	DISPC_GFX_BA_j /DISPC_VIDp_BA_j/DISPC_WB_BA_j	PBA270
	DISPC_GFX_PIXEL_INC /DISPC_VIDp_PIXEL_INC/DISPC_WB_PIXEL_INC	1 to 16
	DISPC_GFX_ROW_INC / DISPC_VIDp_ROW_INC/DISPC_WB_ROW_INC	ROW270

NOTE: For YUV format, in addition to the DISPC_VIDp_BA_j register used for the Y component, the DISPC_VIDp_BA_UV_j register must be set to define the base address of the UV frame buffer in memory.

The PBA rotation is determined by:

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- PBA0 = PBA | (mode 27) | (orientation 29) | (132)
- PBA90 = PBA | (mode 27) | (orientation 29) | (132)
- PBA180 = PBA | (mode 27) | (orientation 29) | (132)
- PBA270 = PBA | (mode 27) | (orientation 29) | (132)

Where PBA is the physical base address of image in the memory.

The ROW rotation is determine by:

- If 8 bits per pixel:
  - ROW0 = 16384: Width of the video picture in memory (in bytes) + 1
  - ROW90 = 8192: Width of the video picture in memory (in bytes) + 1
  - ROW180 = 16384: Width of the video picture in memory (in bytes) + 1
  - ROW270 = 8192: Width of the video picture in memory (in bytes) + 1
- If 16 bits per pixel:
  - ROW0 = 32768: Width of the video picture in memory (in bytes) + 1
  - ROW90 = 8192: Width of the video picture in memory (in bytes) + 1
  - ROW180 = 32768: Width of the video picture in memory (in bytes) + 1
  - ROW270 = 8192: Width of the video picture in memory (in bytes) + 1
- If 32 bits per pixel:
  - ROW0 = 32768: Width of the video picture in memory (in bytes) + 1
  - ROW90 = 16384: Width of the video picture in memory (in bytes) + 1
  - ROW180 = 32768: Width of the video picture in memory (in bytes) + 1
  - ROW270 = 16384: Width of the video picture in memory (in bytes) + 1

Table 10-29. Mode Definition

	8-Bit Tiled	16-Bit Tiled	32-Bit Tiled	Page Tiled
Mode	0	1	2	3

Table 10-30. Orientation Definition

Type of Orientation	Value
0-degree view	0x0
180-degree view with mirroring	0x1
0-degree view with mirroring	0x2
180-degree view	0x3
270-degree view with mirroring	0x4
270-degree view	0x5
90-degree view	0x6
90-degree view with mirroring	0x7

NOTE: For YUV4:2:0 progressive pixel format, because the value of the DISPC_VIDp_ROW_INC register is defined for the Y buffer, the DISPC_VIDp_ATTRIBUTES[22] DOUBLESTRIDE bit field must be set to 1 when rotating the picture by 0 and 180 degrees and must be reset to 0 when rotating the picture by 90 and 270 degrees.

For YUV4:2:0 interlaced pixel format, because the value of the DISPC_VIDp_ROW_INC register is defined for the Y buffer, the DISPC_VIDp_ATTRIBUTES[22] DOUBLESTRIDE bit field must be set to 1 when rotating the picture by 0 and 180 degrees. Rotations of 90 and 270 degrees are not supported with this pixel format.

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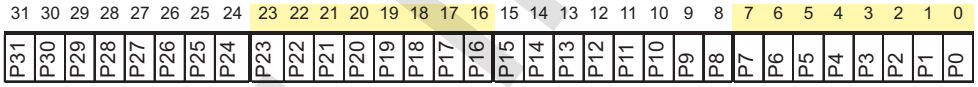
10.2.4.8 Memory Format

The graphic and video pipelines support various types of memory format. Table 10-31 list all supported formats for each pipeline. The nibble mode is enabled by setting the DISPC_GFX_ATTRIBUTES[9] NIBBLEMODE bit to 0x1 and applies only to BITMAP format for the GFX pipeline.

Table 10-31. Memory Formats Supported

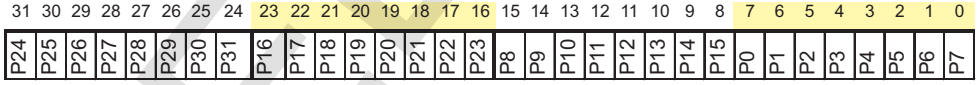
Formats	GFX	VID1	VID2	VID3	WB
BITMAP 1-BPP	x				
BITMAP 2-BPP	x				
BITMAP 4-BPP	x				
BITMAP 8-BPP	x				
xRGB12-4444	x	x	x	x	x
RGBx12-4444	x	x	x	x	x
ARGB16-4444	x	x	x	x	x
RGBA16-4444	x	x	x	x	x
RGB16-565	x	x	x	x	x
xRGB16-1555	x	x	x	x	x
ARGB16-1555	x	x	x	x	x
xRGB24-8888	x	x	x	x	x
RGBx24-8888	x	x	x	x	
RGB24-888	x	x	x	x	x
ARGB32-8888	x	x	x	x	x
RGBA32-8888	x	x	x	x	x
UYUV4:2:2		x	x	x	x
YUV2 4:2:2		x	x	x	x
YUV4:2:0 – NV12		x	x	x	x

- BITMAP 1-BPP data memory organization (CLUT)



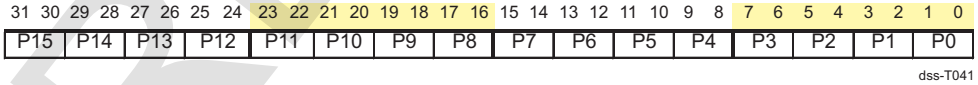
dss-T039

- BITMAP 1-BPP data memory organization (CLUT) in nibble mode



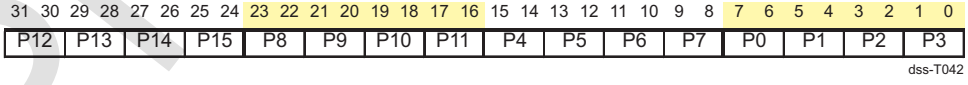
dss-T040

- BITMAP 2-BPP data memory organization (CLUT)



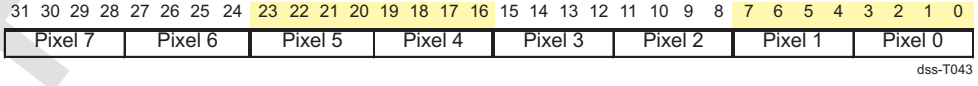
dss-T041

- BITMAP 2-BPP data memory organization (CLUT) in nibble mode



dss-T042

- BITMAP 4-BPP data memory organization (CLUT)



dss-T043

- BITMAP 4-BPP data memory organization (CLUT) in nibble mode

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31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Pixel 6	Pixel 7	Pixel 4	Pixel 5
Pixel 2	Pixel 3	Pixel 0	Pixel 1

dss-T044

- BITMAP 8-BPP data memory organization (CLUT)

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Pixel 3	Pixel 2	Pixel 1	Pixel 0

dss-T045

- xRGB12-4444 BPP data memory organization

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Unused	R1	G1	B1
Unused	R0	G0	B0

dss-T046

- RGBx12-4444 BPP data memory organization

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
R1	G1	B1	Unused
R0	G0	B0	Unused

dss-T047

- ARGB16-4444 BPP data memory organization

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
A1	R1	G1	B1
A0	R0	B0	G0

dss-T048

- RGBA16-4444 BPP data memory organization

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
R1	G1	B1	A1
R0	G0	B0	A0

dss-T050

- xRGB16-555 BPP data memory organization

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
U	R1	G1	B1
U	R0	B0	G0

dss-T062

- ARGB16-1555 BPP data memory organization

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
A1	R1	G1	B1
A0	R0	B0	G0

dss-T051

- RGB16-565 BPP data memory organization

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
R1	G1	B1	R0
G0	B0		

dss-T052

- xRGB24-8888 BPP data memory organization

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Unused	R	G	B

dss-T053

- RGBx24-8888 BPP data memory organization

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
R	G	B	Unused

dss-T054

- RGB24-888 BPP packed data memory organization

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
B1	R0	G0	B0	+0x0
G2	B2	R1	G1	+0x4
R3	G3	B3	R2	+0x8

dss-T055

- ARGB32-8888 BPP data memory organization

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
A	R	G	B

dss-T056

- RGBA32-8888 BPP data memory organization

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31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
R	G	B	A

dss-T057

- UYVY4:2:2 data memory organization

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Y1	Cr0	Y0	Cb0	+0x0
Y3	Cr2	Y2	Cb2	+0x4
Y5	Cr4	Y4	Cb4	+0x8
Y7	Cr6	Y6	Cb6	+0xC

dss-T059

- YUV2 4:2:2 data memory organization

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Cr0	Y1	Cb0	Y0	+0x0
Cr2	Y3	Cb2	Y2	+0x4
Cr4	Y5	Cb4	Y2	+0x8
Cr6	Y7	Cb6	Y6	+0xC

dss-T060

- YUV4:2:0-NV12 data memory organization

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Y3	Y2	Y1	Y0	+0x0
Y7	Y6	Y5	Y4	+0x4

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Cr1	Cb1	Cr0	Cb0	+0x0 + Offset
Cr3	Cb3	Cr2	Cb2	+0x4 + Offset
Cr5	Cb5	Cr4	Cb4	+0x8 + Offset
Cr7	Cb7	Cr6	Cb6	+0xC + Offset

dss-T061

10.2.4.9 Graphics Pipeline

The graphics pipeline is connected to the GFX FIFO for the input port and to the three overlay managers for the output or WB pipeline. The pixel output is directed to an LCD, TV, or WB path by setting the DISPC_GFX_ATTRIBUTES[8] CHANNELOUT bit and the DISPC_GFX_ATTRIBUTES[31:30] CHANNELOUT2 bit field. Table 10-50 resumes the bit field settings to orient a pipeline to an LCD/TV or WB output. The default value directs the GFX pipeline to LCD1.

The pipeline consists of programmable replication logic, an antiflicker filter, and one 256-entry palette table. The replication logic is used to convert the RGB pixels, excluding the RGB24 format, into an ARGB32-based format. The antiflicker filter processes the graphics data in RGB format to remove some of the vertical flicker. The 256-entry palette is used to convert bitmap formats into RGB formats or for gamma corrections when RGB format is inputted.

Table 10-31 lists the input formats supported by the graphics pipeline.

The graphics pipeline is enabled by setting the DISPC_GFX_ATTRIBUTES[0] ENABLE bit to 0x1.

Figure 10-42 shows the graphics pipeline.

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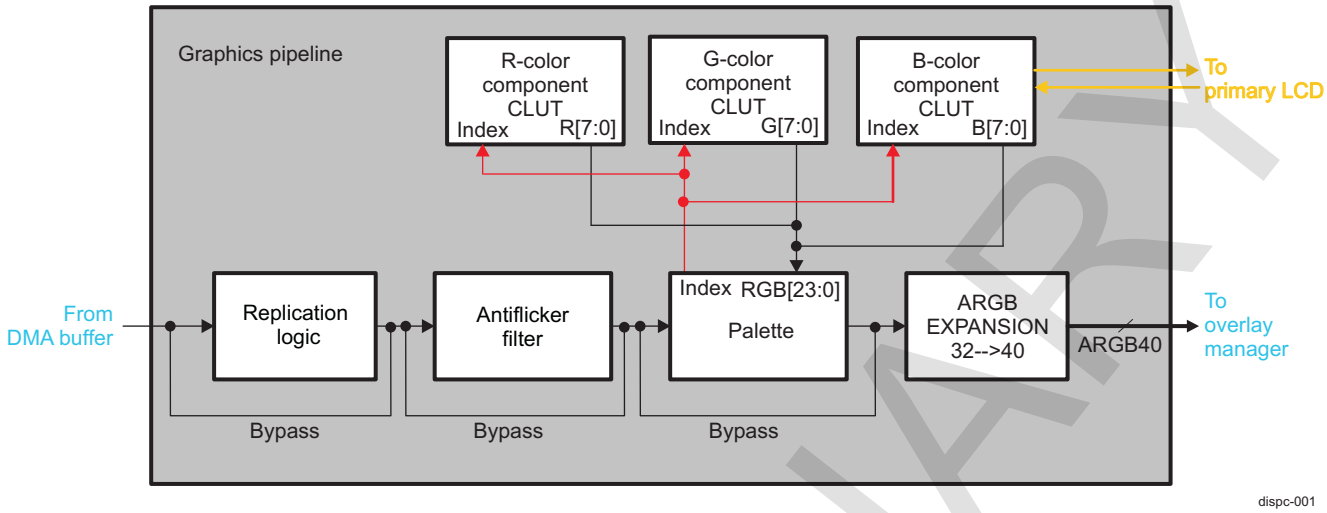
Figure 10-42. Graphics Pipeline



10.2.4.9.1 Replication Logic

The replication logic increases the color depth of the graphics-encoded pixels (from true color RGB 12, and 16 to 40 BPP).

- When the replication logic is enabled by setting the DISPC_GFX_ATTRIBUTES[5] REPLICATIONENABLE bit to 0x1, the MSBs are copied to the missing LSB. Table 10-34 describes the remapping of the RGB pixels into ARGB 40-bit values.

Table 10-32. Replication Enabled: RGB Pixel Formats Remapping Into ARGB40-10.10.10.10

	A[7:0]	R[7:0]	G[7:0]	G[7:0]
Formats	**MSB LSB**	**MSB LSB**	**MS LSB**	**MSB LSB**
xRGB12-4444	11111111	R[3:0]R[3:0]R[3:2]	G[3:0]G[3:0]G[3:2]	B[3:0]B[3:0]B[3:2]
RGBx12-4444	11111111	R[3:0]R[3:0]R[3:2]	G[3:0]G[3:0]G[3:2]	B[3:0]B[3:0]B[3:2]
RGB16-565	11111111	R[4:0]R[4:0]	G[5:0]G[5:2]	B[4:0]B[4:0]
xRGB16-1555	11111111	R[4:0]R[4:0]	G[4:0]G[4:0]	B[4:0]B[4:0]
ARGB16-1555	AAAAAAAA	R[4:0]R[4:0]	G[4:0]G[4:0]	B[4:0]B[4:0]
ARGB16-4444	A[3:0]A[3:0]A[3:2]	R[3:0]R[3:0]R[3:2]	G[3:0]G[3:0]G[3:2]	B[3:0]B[3:0]B[3:2]
RGBA16-4444	A[3:0]A[3:0]A[3:2]	R[3:0]R[3:0]R[3:2]	G[3:0]G[3:0]G[3:2]	B[3:0]B[3:0]B[3:2]

- When the replication logic is disabled by setting the DISPC_GFX_ATTRIBUTES[5] REPLICATIONENABLE bit to 0x0, the encoded pixel values are shifted to the MSB boundary of the 24-bit format. The missing bit values are filled with 0s. Table 10-35 describes the remapping of the RGB pixels into ARGB 40-bit values.

Table 10-33. Replication Disabled: RGB Pixel Formats Remapping Into ARGB40-10.10.10.10

	A[7:0]	R[7:0]	G[7:0]	B[7:0]
Formats	**MSB LSB**	**MSB LSB**	**MSB LSB**	**MSB LSB**
xRGB12-4444	1111111111	R[3:0]000000	G[3:0]000000	B[3:0]000000
RGBx12-4444	1111111111	R[3:0]000000	G[3:0]000000	B[3:0]000000
RGB16-565	1111111111	R[4:0]00000	G[5:0]0000	B[4:0]00000
xRGB16-1555	1111111111	R[4:0]00000	G[4:0]00000	B[4:0]00000
ARGB16-1555	AAAAAAAAAA	R[4:0]00000	G[4:0]00000	B[4:0]00000
ARGB16-4444	A[3:0]A[3:0]A[3:2]	R[3:0]000000	G[3:0]000000	B[3:0]000000
RGBA16-4444	A[3:0]A[3:0]A[3:2]	R[3:0]000000	G[3:0]000000	B[3:0]000000

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10.2.4.9.2 Antiflicker Filter

The antiflicker filter processes the graphics data to remove some of the vertical flicker. It is based on 3-tap FIR filter with fixed coefficients. For each pixel to be output from the graphics pipeline, the pixel above and the pixel below the current line must be read from the DMA graphics FIFO. Therefore, three lines of pixels must be stored in the DMA graphics FIFO.

The antiflickering equations for A, R, G, and B components are:

$A_{out}(x,y) = 0.25*A_{in}(x,y–1) + 0.5*A_{in}(x,y) + 0.25*A_{in}(x,y + 1)$

$R_{out}(x,y) = 0.25*R_{in}(x,y–1) + 0.5*R_{in}(x,y) + 0.25*R_{in}(x,y + 1)$

$G_{out}(x,y) = 0.25*G_{in}(x,y–1) + 0.5*G_{in}(x,y) + 0.25*G_{in}(x,y + 1)$

$B_{out}(x,y) = 0.25*B_{in}(x,y–1) + 0.5*B_{in}(x,y) + 0.25*B_{in}(x,y + 1)$

For the first line of processing, because there is no pixel above, the value (x, y) is duplicated.

Out(x,y) = 0.25*In(x,y) + 0.5*In(x,y) + 0.25*In(x,y + 1)

For the last line of processing, because there is no pixel below, the value (x, y) is duplicated.

Out(x,y) = 0.25*In(x,y–1) + 0.5*In(x,y) + 0.25*In(x,y)

NOTE: Antiflicker filtering is supported only in RGB formats and not in BITMAP formats.

Antiflickering is not supported for pictures with fewer than two lines. In this case, the user must disable the antiflickering processing.

10.2.4.9.3 Color Look-Up Table (CLUT)

The graphics pipeline supports conversion of the BITMAP formats into RGB24 formats through a palette table. To enable palette mode, the DISPC_CONFIG1[3] PALETTEGAMMATABLE bit must be set to 0x0. Figure 10-43 shows the internal architecture of the color look-up/gamma table.

The palette is split into three memories of 256-bit × 8-bit entries. For bitmap (CLUT) indexes, the same value (1-, 2-, 4-, or 8-BPP) indexes the three memories. The table can be reloaded every frame, once, or never (at the beginning of the frame before fetching pixels for the graphics). The table is loaded dynamically at the beginning of the frame by the DISPC DMA engine. The base address of the table buffer is set in the DISPC_GFX_TABLE_BA[31:0] TABLEBA bit field. It is possible to load the table for every frame or only for a specific frame by setting the DISPC_CONFIG1[2:1] LOAD MODE bit field.

The table can be loaded without fetching data for the graphics pipeline. The DMA buffer associated with the graphics pipeline is used to fetch the table from memory. Regardless of the mode (color or monochrome) for each entry into the table, one 32-bit value is fetched from memory.

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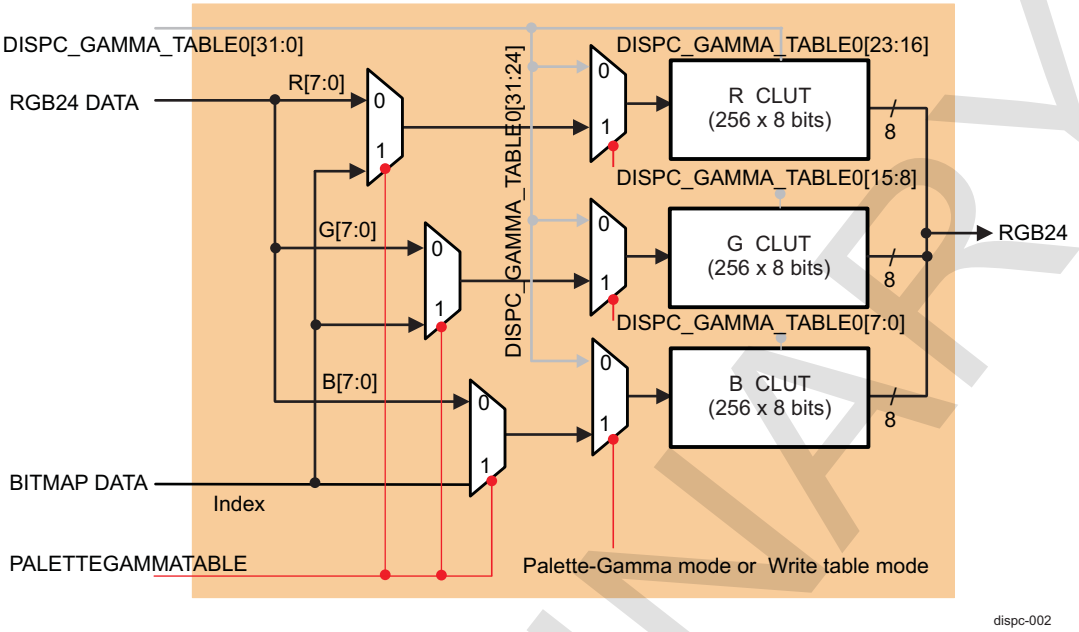
Figure 10-43. Palette/Gamma Correction Architecture



The palette mode uses the encoded pixel values from the input graphics FIFO as pointers to index the 24-bit-wide palette: 1-BPP pixels address 2 palette entries, 2-BPP pixels address 4 palette entries, 4-BPP pixels address 16 palette entries, and 8-BPP pixels address 256 palette entries. In color mode, the value within the palette is made up of three 8-bit fields, one for each color component: red, green, and blue (see Figure 10-44). For color operation, an individual frame is limited to a selection of 256 colors (the number of palette entries). In monochrome mode, only one 8-bit value is present. 256 grayscales and 16,777,216 colors are obtained after passing through the palette (see Figure 10-45)

Figure 10-44. Data Memory Organization: Color Mode

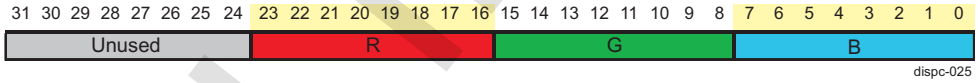
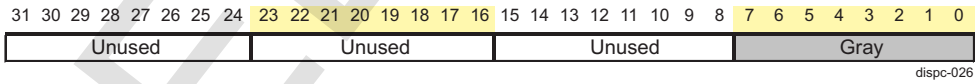


Figure 10-45. Data Memory Organization: Gray Mode



When a palette entry is selected by the encoded pixel value, both the content of the entry and the index are sent to the LCD1 overlay manager.

10.2.4.9.4 Expansion to ARGB40

The expansion module takes in inputs the RGB24 pixel format outputted from the pallette module. The module automatically replicates the 2 MSBs of each color component to create an ARGB40 pixel with the A component set to 0x3FF (see Figure 10-46).

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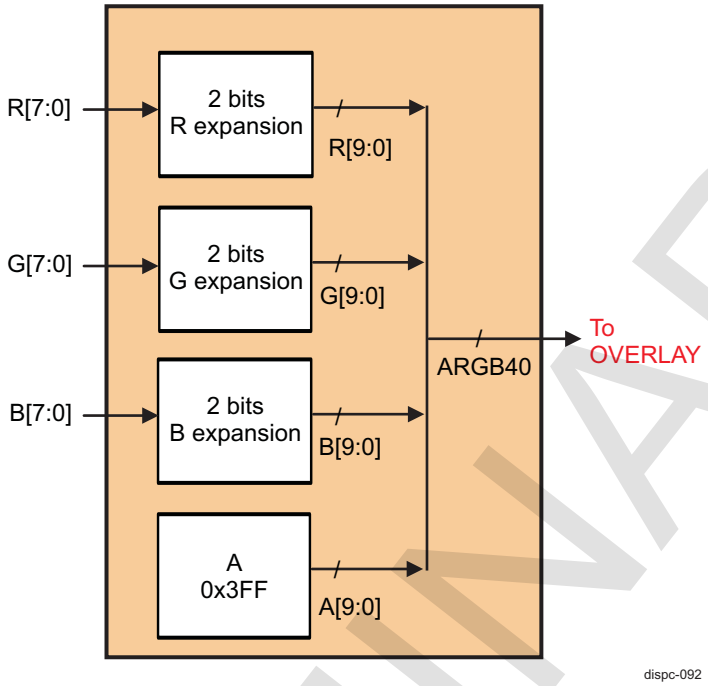
Figure 10-46. Expansion to ARGB40



10.2.4.10 Video Pipelines

Three identical video pipelines are available, VID1, VID2, and VID3. Each video pipeline is connected to its video FIFO controller for the input port and to the three overlay managers LCD 1, LCD2, and TV or WB pipeline. The pixel output is directed to the LCD, TV, or WB path by setting the DISPC_VIDp_ATTRIBUTES[8] CHANNELOUT bit and the DISPC_VIDp_ATTRIBUTES[31:30] CHANNELOUT2 bit field. Table 10-50 resumes the bit field settings to orient a pipeline to an LCD/TV or WB output. The default value directs all video pipelines to LCD1.

A video pipeline consists of a scaler unit, a color space conversion unit (CSC), a VC-1 range mapping unit, and some programmable replication logic. The video pipeline unit order can be configured in two manners (see Figure 10-47 and Figure 10-48):

- Configuration 1: VC-1 range mapping unit followed by a CSC unit and then a scaler unit. The configuration is used to support RGB, ARGB, and RGBA formats, and YUV4:2:2 in backward mode for both data types. Each block can be independently bypassed.
- Configuration 2: VC-1 range mapping unit followed by scaler unit, and then a CSC unit. The configuration is used to support RGB, ARGB, and RGBA formats, and YUV4:2:2 format and YUV420-NV12 formats taking advantage of the scaler to resample the chrominance using five taps horizontally and three or five taps vertically. Each block can be independently bypassed.

The DISPC_VIDn_ATTRIBUTES2[8] YUVCHROMARESAMPLING bit controls the order of the scaler unit in the video pipeline:

- When YUVCHROMARESAMPLING is set to 0x0, the video pipeline is in configuration 1, and the scaler is after the CSC unit. In case of YUV input data in 4:2:2 format, the chrominance resampling (4:2:2 to 4:4:4 format) is done by averaging the chrominance adjacent samples for only 0 degrees (zero rotation), because other rotation (90/180/270 degrees) is not supported in this mode. For more information about the supported chrominance resampling methods, see Section 10.2.4.10.3.1, *Chrominance Resampling*.
- When YUVCHROMARESAMPLING is set to 0x1, the video pipeline is in configuration 2, and the scaler is before the CSC unit.
  - In case of YUV4:2:2 input data with 90-/270-degree rotation, the data is preprocessed by duplicating the missing chrominance samples.

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– In case of YUV4:2:2 input data with 0-/180-degree rotation, the chroma upsampling is performed in the scaler unit.

Table 10-31lists the input formats supported by the video pipelines.

The video pipeline is enabled by setting ENABLE bit DISPC_VIDp_ATTRIBUTES[0] to 0x1.

Figure 10-47. Configuration 1: Video Pipeline

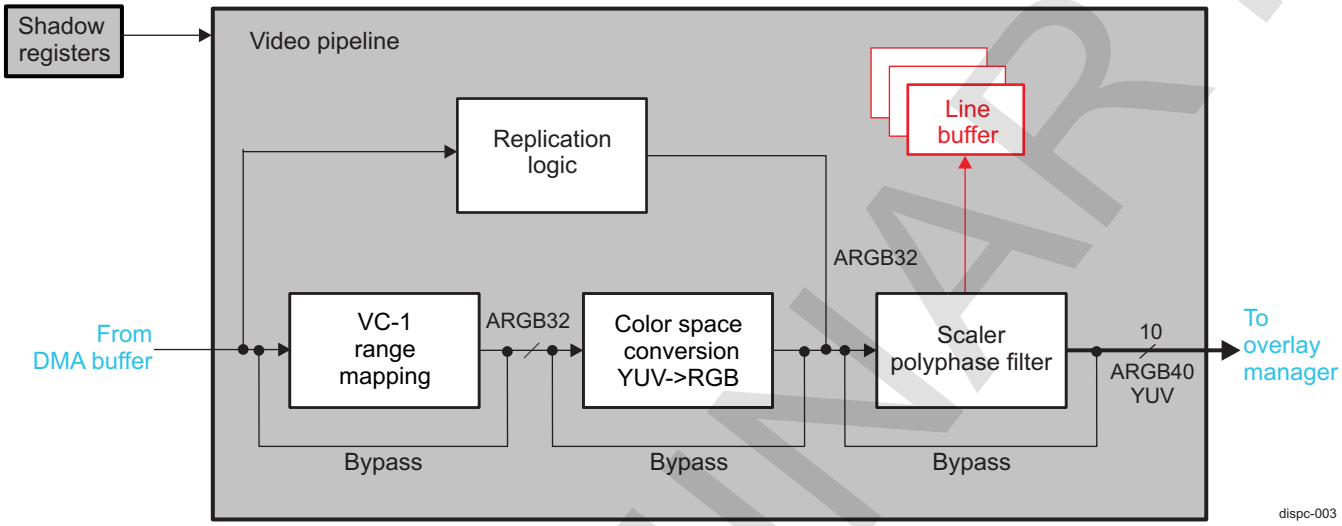
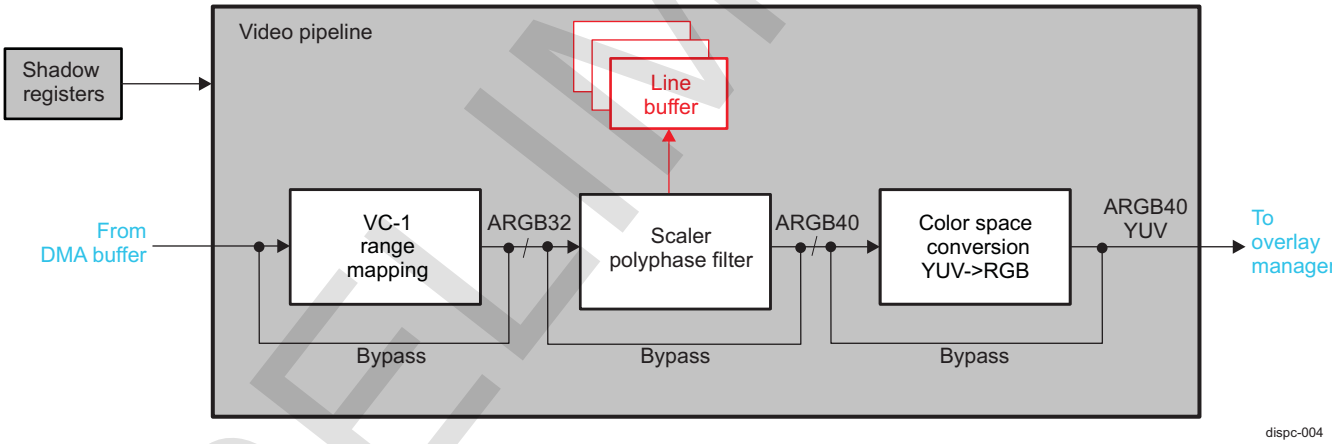


Figure 10-48. Configuration 2: Video Pipeline



10.2.4.10.1 Replication Logic

The replication logic increases the color depth of the video-encoded pixels (from true color RGB 12, and 16 to 32 BPP) and available only in configuration 1.

The expansion from 8 to 10 bits color component is done by:

- The CSC unit, when the scaler is after the CSC module and when the vertical scaler is disabled.
- The vertical scaler, when the scaler is after the CSC unit and enabled.
- The replication bit module, when both the CSC unit and scaler are disabled.
- When the replication logic is enabled by setting the DISPC_VIDp_ATTRIBUTES[10] REPLICATIONENABLE bit to 0x1, the MSBs are copied to the missing LSBs. Table 10-34 describes the remapping of the RGB pixels into ARGB 32-bit values.

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Table 10-34. Replication Enabled: RGB Pixel Formats Remapping Into ARGB32-8888

	A[7:0]	R[7:0]	G[7:0]	G[7:0]
Formats	**MSB LSB**	**MSB LSB**	**MSB LSB**	**MSB LSB**
xRGB12-4444	11111111	R[3:0]R[3:0]	G[3:0]G[3:0]	B[3:0]B[3:0]
RGBx12-4444	11111111	R[3:0]R[3:0]	G[3:0]G[3:0]	B[3:0]B[3:0]
RGB16-565	11111111	R[4:0]R[4:2]	G[5:0]G[5:4]	B[4:0]B[4:2]
xRGB16-1555	11111111	R[4:0]R[4:2]	G[4:0]G[4:2]	B[4:0]B[4:2]
ARGB16-1555	AAAAAAAA	R[4:0]R[4:2]	G[4:0]G[4:2]	B[4:0]B[4:2]
ARGB16-4444	A[3:0]A[3:0]	R[3:0]R[3:0]	G[3:0]G[3:0]	B[3:0]B[3:0]
RGBA16-4444	A[3:0]A[3:0]	R[3:0]R[3:0]	G[3:0]G[3:0]	B[3:0]B[3:0]

- When the replication logic is disabled by setting the DISPC_VIDp_ATTRIBUTES[10] REPLICATIONENABLE bit to 0x0, the encoded pixel values are shifted to the MSB boundary of the 24-bit format. The missing bit values are filled with 0s. Table 10-35 describes the remapping of the RGB pixels into ARGB 32-bit values.

Table 10-35. Replication Disabled: RGB Pixel Formats Remapping Into ARGB32-8888

	A[7:0]	R[7:0]	G[7:0]	B[7:0]
Formats	**MSB LSB**	**MSB LSB**	**MSB LSB**	**MSB LSB**
xRGB12-4444	11111111	R[3:0]0000	G[3:0]0000	B[3:0]0000
RGBx12-4444	11111111	R[3:0]0000	G[3:0]0000	B[3:0]0000
RGB16-565	11111111	R[4:0]000	G[5:0]00	B[4:0]000
xRGB16-1555	11111111	R[4:0]000	G[4:0]000	B[4:0]000
ARGB16-1555	AAAAAAAA	R[4:0]000	G[4:0]000	B[4:0]000
ARGB16-4444	A[3:0]A[3:0]	R[3:0]0000	G[3:0]0000	B[3:0]0000
RGBA16-4444	A[3:0]A[3:0]	R[3:0]0000	G[3:0]0000	B[3:0]0000

10.2.4.10.2 VC-1 Range Mapping Unit

The VC-1 range mapping unit is used when the video frame picture is decoded using a VC-1 codec by the video accelerator. It remaps the Y, Cb, and Cr components. The unit is used primarily for YUV4:2:0-NV12 pixel format but also can be applied to YUV4:2:2 pixel formats (YUV2 and UYVY).

The VC-1 range mapping unit is enabled by setting the DISPC_VIDp_ATTRIBUTES2[0] VC1ENABLE bit to 0x1. The DISPC_VIDp_ATTRIBUTES2[3:1] VC1_RANGE_Y and DISPC_VIDp_ATTRIBUTES2[6:4] VC1_RANGE_CBCR bit fields are two 3-bit values programmed by the user and are independent for each video pipeline. The module is governed by the equations:

$Y_{out} = CLIP(((Y_{int} – 128) \times (VC1_RANGE_Y + 9) + 4) / 8) + 128)$

$C_b = CLIP(((C_b – 128) \times (VC1_RANGE_CBCR + 9) + 4) / 8) + 128)$

$C_r = CLIP(((C_r – 128) \times (VC1_RANGE_CBCR + 9) + 4) / 8) + 128)$

NOTE: The input and output pixel values are unsigned (Y, Cr, and Cb).

The function CLIP () clips to 0 or 255 when min or max are reached respectively otherwise resulting output stay identical.

10.2.4.10.3 CSC Unit YUV to RGB

The CSC unit converts the video-encoded pixel values from YUV4:4:4 format into RGB24 or RGB30 format. The output format depends on the video pipeline configuration selected:

- Configuration 1: RGB24 output format, with 8-bit value per component: red, green, and blue
- Configuration 2: RGB30 output format, with 10-bit value per component: red, green, and blue

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In case of YUV4:2:0 or YUV4:2:2 formats, a chrominance resampling to YUV4:4:4 is required before converting the YUV into RGB values (see Section 10.2.4.10.3.1, *Chrominance Resampling*). YUV4:2:2 or YUV4:2:0 to YUV4:4:4 chrominance resampling is a preprocessing to the color space conversion.

Figure 10-49 to Figure 10-52 show the 3 × 3 11-bit coefficients used to convert from YUV4:4:4 into RGB24. The coefficients are set according to the standard used to encode the pixel data in YUV color space. Table 10-36 resumes the coefficients with their respective bit fields.

Table 10-36. Color Space Conversion YUV to RGB Bit Field Setting

Coefficients	Bit Field Registers
R_Y	RY field DISPC_VIDp_CONV_COEF0[10:0]
R_{Cr}	RCR field DISPC_VIDp_CONV_COEF0[26:16]
R_{Cb}	RCB field DISPC_VIDp_CONV_COEF1[10:0]
G_Y	GY field DISPC_VIDp_CONV_COEF1[26:16]
G_{Cr}	GCR field DISPC_VIDp_CONV_COEF2[10:0]
G_{Cb}	GCB field DISPC_VIDp_CONV_COEF2[26:16]
B_Y	BY field DISPC_VIDp_CONV_COEF3[10:0]
B_{Cr}	BCR field DISPC_VIDp_CONV_COEF3[26:16]
B_{Cb}	BCB field DISPC_VIDp_CONV_COEF4[10:0]

- For configuration 1 with an RGB24 output:

  If the active range for the luminance samples (Y) is [16:235] and [16:240] for the chrominance samples (Cb and Cr), the range selection is done by setting the DISPC_VIDp_ATTRIBUTES[11] FULLRANGE bit to 0x0. The values of R, G, and B output components are clipped to the range [0:255].

NOTE: The scaling and CSC clipping is set by the same bit, DISPC_VIDp_ATTRIBUTES[11] FULLRANGE.

Figure 10-49. YCbCr to RGB Registers (FULLRANGE = 0), 8-Bit Outputs

$$\begin{bmatrix} R_{OUT} \\ G_{OUT} \\ B_{OUT} \end{bmatrix} = \frac{1}{256} * \begin{bmatrix} R_Y & R_{cr} & R_{cb} \\ G_Y & G_{cr} & G_{cb} \\ B_Y & B_{cr} & B_{cb} \end{bmatrix} * \begin{bmatrix} Y_{IN} - 16 \\ Cr_{IN} - 128 \\ Cb_{IN} - 128 \end{bmatrix}$$

dispc-005

If the active range for the luminance samples (Y) and chrominance samples (Cb and Cr) is [0:255], the range selection is done by setting the DISPC_VIDp_ATTRIBUTES[11] FULLRANGE bit to 0x1 . The values of R, G, and B output components are clipped to the range [0:255].

Figure 10-50. YCbCr to RGB Registers (FULLRANGE = 1), 8-Bit Outputs

$$\begin{bmatrix} R_{OUT} \\ G_{OUT} \\ B_{OUT} \end{bmatrix} = \frac{1}{256} * \begin{bmatrix} R_Y & R_{cr} & R_{cb} \\ G_Y & G_{cr} & G_{cb} \\ B_Y & B_{cr} & B_{cb} \end{bmatrix} * \begin{bmatrix} Y_{IN} \\ Cr_{IN} - 128 \\ Cb_{IN} - 128 \end{bmatrix}$$

dispc-006

- For configuration 2 with an RGB30 output:

  If the active range for the luminance samples (Y) is [64:940] and [64:960] for the chrominance samples (Cb and Cr), the range selection is done by setting the DISPC_VIDp_ATTRIBUTES[11] FULLRANGE bit to 0x0. The values of R, G, and B output components are clipped to the range [0:1023].

NOTE: The scaling and CSC clipping is set by the same bit, DISPC_VIDp_ATTRIBUTES[11] FULLRANGE.

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Figure 10-51. YCbCr to RGB Registers (FULLRANGE = 0), 10-Bit Outputs

$$\begin{bmatrix} R_{OUT} \\ G_{OUT} \\ B_{OUT} \end{bmatrix} = \frac{1}{256} * \begin{bmatrix} R_Y & R_{cr} & R_{cb} \\ G_Y & G_{cr} & G_{cb} \\ B_Y & B_{cr} & B_{cb} \end{bmatrix} * \begin{bmatrix} Y_{IN} - 64 \\ Cr_{IN} - 512 \\ Cb_{IN} - 512 \end{bmatrix}$$

dispc-074

If the active range for the luminance samples (Y) and chrominance samples (Cb and Cr) is [0:1023], the range selection is done by setting the DISPC_VIDp_ATTRIBUTES[11] FULLRANGE bit to 0x1. The values of R, G, and B output components are clipped to the range [0:1023].

Figure 10-52. YCbCr to RGB Registers (FULLRANGE = 1), 10-Bit Outputs

$$\begin{bmatrix} R_{OUT} \\ G_{OUT} \\ B_{OUT} \end{bmatrix} = \frac{1}{256} * \begin{bmatrix} R_Y & R_{cr} & R_{cb} \\ G_Y & G_{cr} & G_{cb} \\ B_Y & B_{cr} & B_{cb} \end{bmatrix} * \begin{bmatrix} Y_{IN} \\ Cr_{IN} - 512 \\ Cb_{IN} - 512 \end{bmatrix}$$

dispc-075

10.2.4.10.3.1 Chrominance Resampling

Two methods are supported to resample chrominance:

- Averaging of the chrominance is done by software followed by hardware conversion when the video pipeline is in configuration 1.
- Filtering of the chrominance using the scaler unit (chrominance resampling and rescaling can be combined to support native rescaling of YUV format) when the video pipeline is in configuration 2.

To convert the YUV4:2:2 encoded pixel values into YUV4:4:4 format, the averaging of the chrominance technique can be used as shown in Figure 10-53. The missing chrominance samples (Cb and Cr) are interpolated using the average values of the two closest values on the same line (,) or are repeated from the second pixel in the same 32-bit container (see Figure 10-54). For the last pixel, the chrominance samples are duplicated using the values from the previous pixel; otherwise, the chrominance samples are averaged using the two adjacent values. Figure 10-55 shows the flow of the pixel.

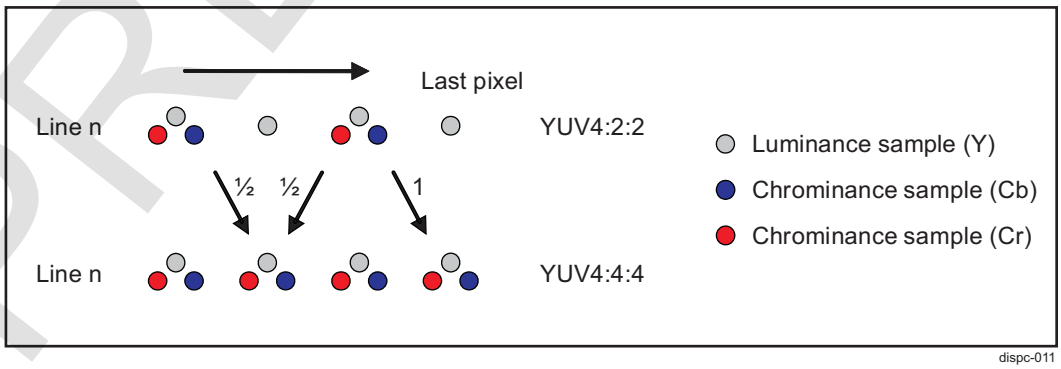
Figure 10-53. Averaging of the Chrominance Formula

$$Cb_n(YCbCr\ 444) = \frac{Cb_{n-1}(YCbCr\ 422) + Cb_{n+1}(YCbCr\ 422)}{2} (\text{n odd})$$

$$Cr_n(YCbCr\ 444) = \frac{Cr_{n-1}(YCbCr\ 422) + Cr_{n+1}(YCbCr\ 422)}{2} (\text{n odd})$$

dispc-010

Figure 10-54. Averaging of the Chrominance Representation



dispc-011

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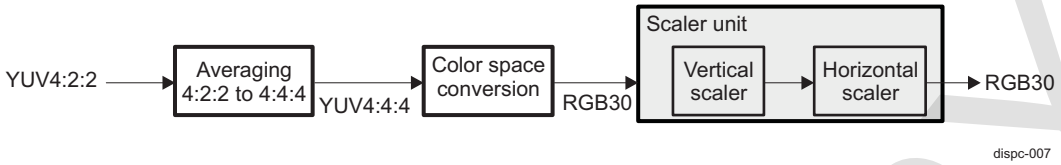
Figure 10-55. YUV4:2:2 to RGB30 Using Averaging of the Chrominance



The scaler unit can be used to resample the chrominance of YUV4:2:0 and YUV4:2:2, as shown in Figure 10-56 and Figure 10-57, respectively. The settings of the scaler unit to perform chrominance resampling are described in Section 10.2.4.10.4, *Scaler Unit*.

Figure 10-56. YUV4:2:0 to RGB30 Using Scaler Unit for Resampling Chrominance

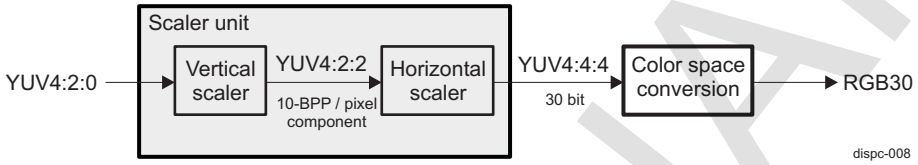
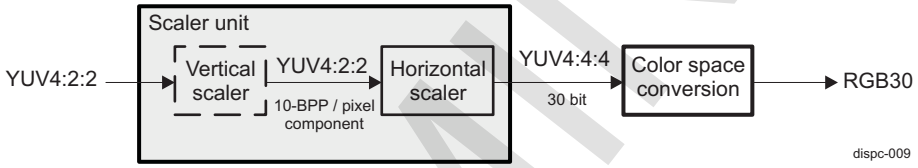


Figure 10-57. YUV4:2:2 to RGB30 Using Scaler Unit for Resampling Chrominance



NOTE: If rotation must be supported, YUV4:2:2 and YUV4:2:0 (0-/180-degree rotation) chrominance resampling is done as shown in Figure 10-57 and Figure 10-56, respectively.
For YUV4:2:2 (90-/270-degree rotation) data are preprocessed to present YUV4:4:4 on the scaler input (duplication of the missing chroma), as shown in Figure 10-55.

10.2.4.10.4 Scaler Unit

All video formats are supported, including formats with alpha blending. Alpha blending is scaled with the same parameters as RGB color components. For the YUV formats, Y and Cb/Cr are processed independently. The filter is based on a finite impulse response (FIR) filter. The filtering can be used for different processing:

- Upsampling of the picture
- Downsampling of the picture
- Antiflicker reduction
- De-interlacing using "bob" algorithm
- Chrominance resampling in case of YUV data formats

NOTE: The user must ensure the resizing frame displays in the LCD/screen boundaries.

Figure 10-58 shows an example of video upsampling.

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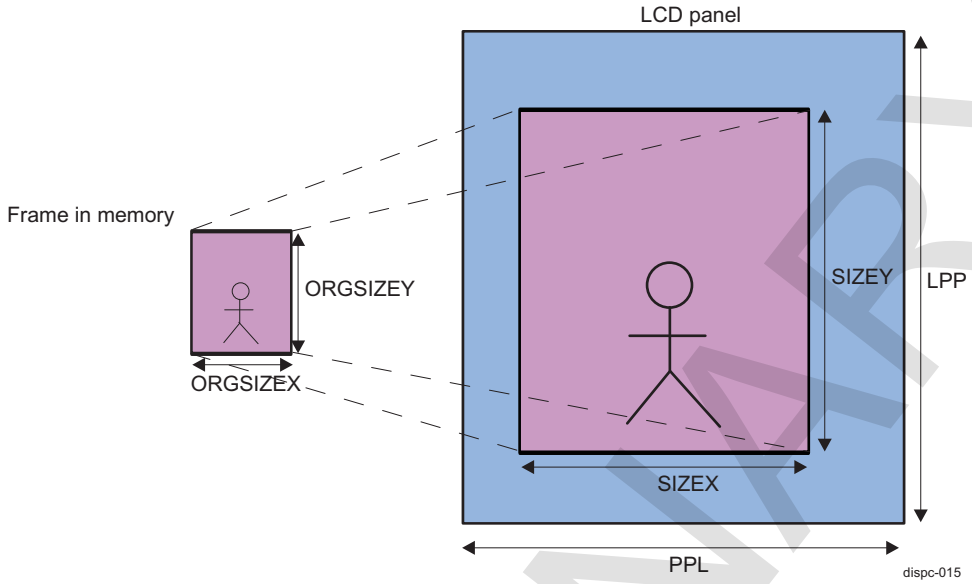
Figure 10-58. Video Upsampling



The up/downsampling filter is a polyphase filter with five taps and eight phases for the horizontal filter, and a programmable number of taps (three or five) and eight phases for vertical filter. The input buffer has five input memory lines. The following limitations must be considered:

- The upsampling ratio is up to x8.
- The downsampling ratio using 3-tap configuration is down to x0.5 for RGB format.
- The downsampling ratio using 5-tap configuration is down to x0.25 for RGB format.
- If the input format is changed from YUV4:2:2 toYUV4:2:0 (WB pipeline), the downsampling ratio is further reduced:
  - Using 5-tap configuration, the ratio is down to x0.5 for RGB format.
  - Using 3-tap configuration, no downscaling is available.

For the vertical up/downsampling in 3-tap configuration, the equations are:

For RGB formats

$$A_{out}(n)=(\sum_{i=-1}^{i=1} C_{vi}(\Phi_y)*A_{in}(n+i))>>5$$

$$R_{out}(n)=(\sum_{i=-1}^{i=1} C_{vi}(\Phi_y)*R_{in}(n+i))>>5$$

$$G_{out}(n)=(\sum_{i=-1}^{i=1} C_{vi}(\Phi_y)*G_{in}(n+i))>>5$$

$$B_{out}(n)=(\sum_{i=-1}^{i=1} C_{vi}(\Phi_y)*B_{in}(n+i))>>5$$

For YUV formats

$$Y_{out}(n)=(\sum_{i=-1}^{i=1} C_{vi}(\Phi_y)*Y_{in}(n+i))>>5$$

$$Cr_{out}(n)=(\sum_{i=-1}^{i=1} C_{vci}(\Phi_c)*Cb_{in}(n+i))>>5$$

$$Cb_{out}(n)=(\sum_{i=-1}^{i=1} C_{vci}(\Phi_c)*Cr_{in}(n+i))>>5$$

dispc-013

(7)

For the vertical up/downsampling in 5-tap configuration, the equations are:

For RGB formats

$$A_{out}(n)=(\sum_{i=-2}^{i=2} C_{vi}(\Phi_y)*A_{in}(n+i))>>5$$

$$R_{out}(n)=(\sum_{i=-2}^{i=2} C_{vi}(\Phi_y)*R_{in}(n+i))>>5$$

$$G_{out}(n)=(\sum_{i=-2}^{i=2} C_{vi}(\Phi_y)*G_{in}(n+i))>>5$$

$$B_{out}(n)=(\sum_{i=-2}^{i=2} C_{vi}(\Phi_y)*B_{in}(n+i))>>5$$

For YUV formats

$$Y_{out}(n)=(\sum_{i=-2}^{i=2} C_{vi}(\Phi_y)*Y_{in}(n+i))>>5$$

$$Cb_{out}(n)=(\sum_{i=-2}^{i=2} C_{vci}(\Phi_c)*Cb_{in}(n+i))>>5$$

$$Cr_{out}(n)=(\sum_{i=-2}^{i=2} C_{vci}(\Phi_c)*Cr_{in}(n+i))>>5$$

dispc-012

(8)

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For the horizontal up/downsampling in 5-tap configuration, the equations are:

For RGB formats

$$A_{out}(n)=\left(\sum_{i=-2}^{i=2} C_{hi}(\Phi)*A_{in}(n+i)\right)>>7$$

$$R_{out}(n)=\left(\sum_{i=-2}^{i=2} C_{hi}(\Phi)*R_{in}(n+i)\right)>>7$$

$$G_{out}(n)=\left(\sum_{i=-2}^{i=2} C_{hi}(\Phi)*G_{in}(n+i)\right)>>7$$

$$B_{out}(n)=\left(\sum_{i=-2}^{i=2} C_{hi}(\Phi)*B_{in}(n+i)\right)>>7$$

For YUV formats

$$Y_{out}(n)=\left(\sum_{i=-2}^{i=2} C_{hi}(\Phi_y)*Y_{in}(n+i)\right)>>7$$

$$Cb_{out}(n)=\left(\sum_{i=-2}^{i=2} C_{hci}(\Phi_c)*Cb_{in}(n+i)\right)>>7$$

$$Cr_{out}(n)=\left(\sum_{i=-2}^{i=2} C_{hci}(\Phi_c)*Cr_{in}(n+i)\right)>>7$$

dispc-014 (9)

NOTE: The pixel (n + 1) is the previous pixel with respect to pixel (n). The line (n + 1) is the previous line with respect to line (n).

The coefficients Ci() depend on the phase between input and output pixels.

NOTE: The coefficients are different for Y and Cr, Cb filtering because the calculations are independent due to the chrominance resampling for YUV4:2:2 and YUV4:2:0.

First, the vertical filter is applied to the encoded input pixel data, and then the horizontal filter is applied on the resulting pixel values to generate the output pixel values. The vertical input of the filter consists of five lines of 2048 × 32 bits for both 3-tap and 5-tap configurations (see Table 10-37).

Table 10-37. Line Buffer Width for Scaler Unit

Vertical Taps	Maximum Input Width (Pixels)
3, 5	2048 × 32 bits

At the beginning of frame scaling processing, the first line is duplicated to fill the first two lines in 3-tap configuration and the first three lines in 5-tap configuration.

At the end of frame scaling processing, the last line is duplicated if the scaling logic requires loading more lines and the last line has been reached.

The programmable coefficients of the polyphase filters are signed 8-bit values (except for the central coefficient, which is unsigned). The video scalers have an 8-bit input and a 10-bit output. The vertical scaling changes the 8-bit input into a 10-bit clipped output and the horizontal scaling takes the 10-bit input.

Figure 10-59 and Figure 10-60 show the scaler macro-architecture for the component A, R, G, B and Y. Figure 10-61 and Figure 10-62 show the scaler macro-architecture for component Cr and Cb.

The scaling output can be clipped to an output range of [0:1023] or [64:960] by configuring the DISPC_VIDp_ATTRIBUTES[11] FULLRANGE bit.

NOTE: The scaling and CSC clipping is set by the same bit, DISPC_VIDp_ATTRIBUTES[11] FULLRANGE.

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Figure 10-59. Macro-Architecture of the Vertical Scaling for A, R, G, B and Y Component

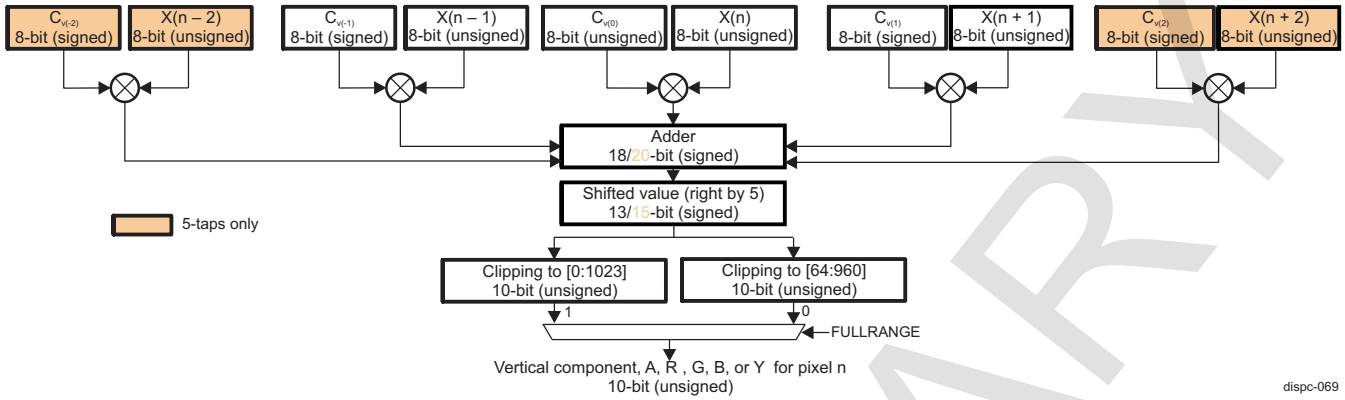

Figure 10-60. Macro-Architecture of the Horizontal Scaling for A, R, G, B and Y Component

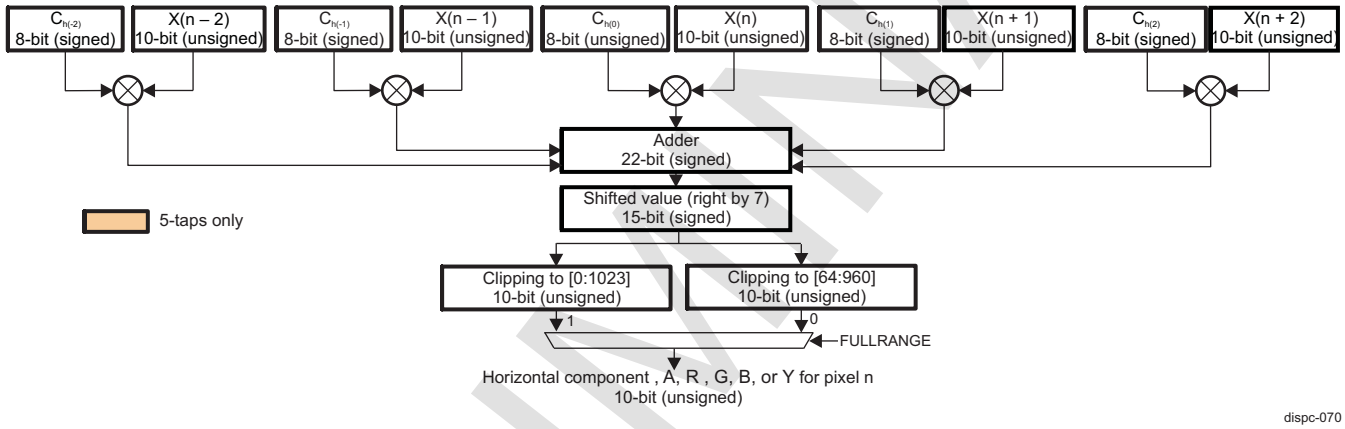

Figure 10-61. Macro-Architecture of the Vertical Scaling for Cr and Cb Component

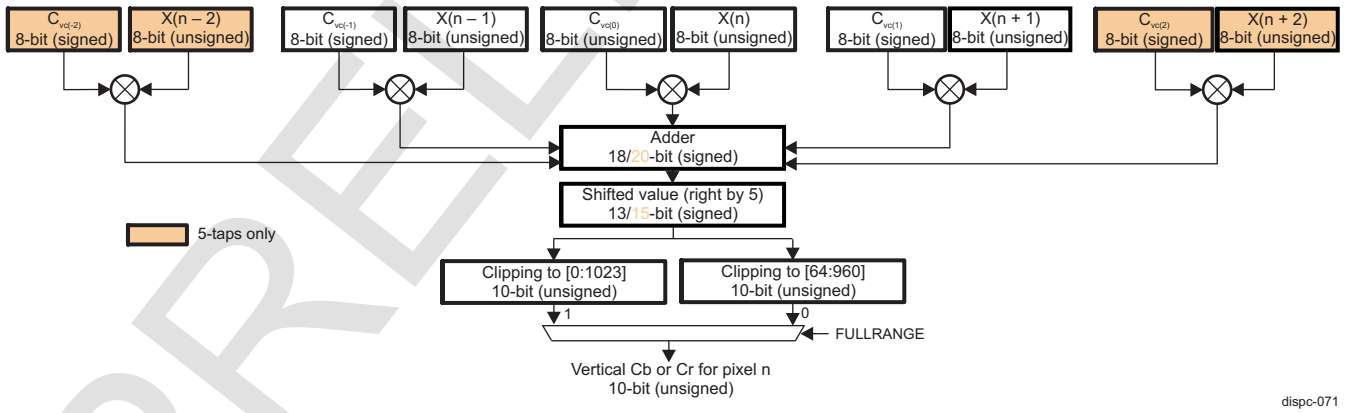

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Figure 10-62. Macro-Architecture of the Horizontal Scaling for Cr and Cb Component

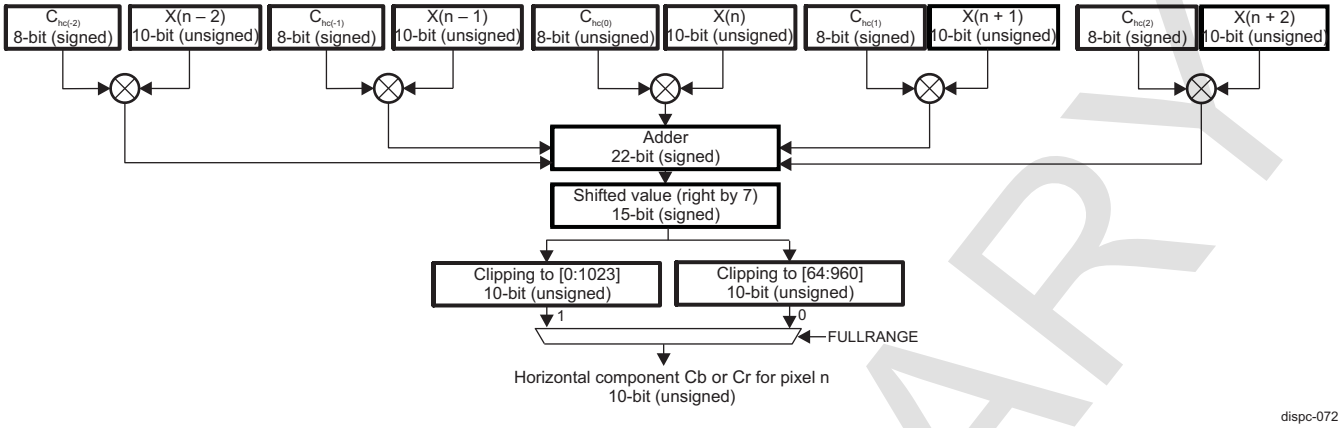

Table 10-38 and Table 10-39 resume all the bit fields in function to set for each coefficient.

Table 10-38. Register Bit Field Associated to Coefficient for ARGB and Y Configuration in VIDp Scaler

Taps	Coefficient	3 Taps	5 Taps	Registers
		Bit Field	Bit Field	
Vertical	Cv(–2)		FIRVC22	DISPC_VIDp_FIR_COEF_V_i
	Cv(–1)	FIRVC2	FIRVC2	DISPC_VIDp_FIR_COEF_HV_i
	Cv(0)	FIRVC1	FIRVC1	DISPC_VIDp_FIR_COEF_HV_i
	Cv(1)	FIRVC0	FIRVC0	DISPC_VIDp_FIR_COEF_HV_i
	Cv(2)		FIRVC00	DISPC_VIDp_FIR_COEF_V_i
Horizontal	Ch(–2)		FIRHC4	DISPC_VIDp_FIR_COEF_HV_i
	Ch(–1)		FIRHC3	DISPC_VIDp_FIR_COEF_H_i
	Ch(0)	N/A	FIRHC2	DISPC_VIDp_FIR_COEF_H_i
	Ch(1)		FIRHC1	DISPC_VIDp_FIR_COEF_H_i
	Ch(2)		FIRHC0	DISPC_VIDp_FIR_COEF_H_i

Table 10-39. Register Bit Field Associated to Coefficient for Cb and Cr Configuration in VIDp Scaler

Taps	Coefficient	3 Taps	5 Taps	Registers
		Bit Field	Bit Field	
Vertical	Cvc(–2)		FIRVC22	DISPC_VIDp_FIR_COEF_V2_i
	Cvc(–1)	FIRVC2	FIRVC2	DISPC_VIDp_FIR_COEF_HV2_i
	Cvc(0)	FIRVC1	FIRVC1	DISPC_VIDp_FIR_COEF_HV2_i
	Cvc(1)	FIRVC0	FIRVC0	DISPC_VIDp_FIR_COEF_HV2_i
	Cvc(2)		FIRVC00	DISPC_VIDp_FIR_COEF_V2_i

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Table 10-39. Register Bit Field Associated to Coefficient for Cb and Cr Configuration in VIDp Scaler (continued)

Taps	Coefficient	3 Taps	5 Taps	Registers
		Bit Field	Bit Field	
Horizontal	Chc(–2)	N/A	FIRHC4	DISPC_VIDp_FIR_COEF_HV2_i
	Chc(–1)		FIRHC3	DISPC_VIDp_FIR_COEF_H2_i
	Chc(0)		FIRHC2	DISPC_VIDp_FIR_COEF_H2_i
	Chc(1)		FIRHC1	DISPC_VIDp_FIR_COEF_H2_i
	Chc(2)		FIRHC0	DISPC_VIDp_FIR_COEF_H2_i

The VID scaler unit vertical or/and horizontal sampling is defined by setting/resetting the DISPC_VIDp_ATTRIBUTES[6:5] RESIZEENABLE bit.

A set of configurations must be valid before enabling the video up/downsampling block.

The following fields define the configuration of the video up/downsampling block for VIDp:

- Vertical up/downsampling increment value DISPC_VIDp_FIR[28:16] FIRVINC bit field. The unsigned integer value range is [1:4096]. Software calculates the value using the following equation:

$$FIRVINC = 1024 * \left(\frac{ORGSIZEY}{SIZEY} \right)$$

dispc-066 (10)

NOTE:

- If the value of the DISPC_VIDp_FIR[28:16] FIRVINC bit field is greater than 4096, it is clipped to 4096.
- If DISPC_VIDp_SIZE[26:16] SIZEY equals 0x1, SIZEY is replaced by 0x2 in the previous equation.
- The values of the DISPC_VIDp_PICTURE_SIZE[26:16] ORGSIZEY and DISPC_VIDp_SIZE[26:16] SIZEY bit fields must be programmed with the value desired minus 1.

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- Horizontal up/downsampling increment value DISPC_VIDp_FIR[12:0] FIRHINC bit field: The unsigned integer value range is [1:4096]. Software calculates the value using the following equation:

$$FIRHINC = 1024 * \left(\frac{ORGSIZEX}{SIZEX}\right)$$ dispc-067 (11)

NOTE:

- If the value of the DISPC_VIDp_FIR[12:0] FIRHINC bit field is greater than 4096, it is clipped to 4096.
- If DISPC_VIDp_SIZE[10:0] SIZEX equals 1, DISPC_VIDp_SIZE[10:0] SIZEX is replaced by 2 in the previous equation.
- The values of the DISPC_VIDp_PICTURE_SIZE[10:0] ORGSIZEX and DISPC_VIDp_SIZE[10:0] SIZEX bit field must be programmed with the value desired minus 1.

- Vertical up/downsampling accumulator value DISPC_VIDp_ACCU_j[26:16] VERTICALACCU bit field: The signed integer value range is [–1024:1023]. The accumulator value indicates on which phase the vertical filtering starts. The register DISPC_VIDp_ACCU_0 is used for progressive output and for interlace output; the DISPC_VIDp_ACCU_0 and DISPC_VIDp_ACCU_1 registers are used. Similarly, DISPC_VIDp_ACCU2_0 and DISPC_VIDp_ACCU2_1 are used in progressive or interlace output to set the accumulator value of the Cb and Cr components when scaling YUV format.
- Vertical up/downsampling line buffer configuration DISPC_VIDp_ATTRIBUTES[21] VERTICALTAPS bit: The default value at reset time is 0x0 (3-tap configuration is used). If the bit field is reset, the 3-tap configuration is used.
- Horizontal up/downsampling accumulator value DISPC_VIDp_ACCU_j[10:0] HORIZONTALACCU bit field: The signed integer value range is [–1024:1023]. The accumulator value indicates on which phase the horizontal filtering starts. The register DISPC_VIDp_ACCU_0 is used for progressive output and for interlace output; the DISPC_VIDp_ACCU_0 and DISPC_VIDp_ACCU_1 registers are used. Similarly, DISPC_VIDp_ACCU2_0 and DISPC_VIDp_ACCU2_1 are used in progressive or interlace output to set the accumulator value of the Cb and Cr components when scaling YUV format.

Table 10-40. Vertical/Horizontal Accumulator Phase

Accumulator Value	Phases f
0	0
128 or –896	1
256 or –768	2
384 or –640	3
512 or –512	4
640 or –384	5
768 or –256	6
896 or –128	7

- Vertical up/downsampling coefficients:
  - The 3-tap vertical up/downsampling coefficients are defined in the DISPC_VIDp_FIR_COEF_HV_i registers. There are eight registers for the eight phases with three coefficients for each, or a total of 24 programmable coefficients for the vertical up/downsampling block. Each register contains two 8-bit signed coefficients and one 8-bit unsigned coefficient (the central one).
  - The 5-tap vertical up/downsampling coefficients: Two extra-tap vertical up/downsampling coefficients are defined in the DISPC_VIDp_FIR_COEF_V_i registers. There are 8 registers for the 8 phases with 2 coefficients for each of them, so a total of 16 programmable coefficients for the vertical up/downsampling block are used in addition to the 3-tap registers previously defined.

  Four YUV vertical up/downsampling coefficients are set in DISPC_VIDp_FIR_COEF_HV2_i and DISPC_VIDp_FIR_COEF_V2_i registers. Table 10-38 and Table 10-39 resume all coefficients and their respective registers.
- Horizontal up/downsampling coefficients:

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– The DISPC_VIDp_FIR_COEF_H_i and DISPC_VIDp_FIR_COEF_HV_i registers define the 5-tap horizontal up/downsampling coefficients. Each DISPC_VIDp_FIR_COEF_H_i register contains three 8-bit signed coefficients and one 8-bit unsigned coefficient (the central one). Each DISPC_VIDp_FIR_COEF_HV_i register contains one 8-bit signed coefficient. A total of 40 programmable coefficients for the horizontal up/downsampling block are used.

Four YUV horizontal up/downsampling coefficients are set in the DISPC_VIDp_FIR_COEF_HV2_i and DISPC_VIDp_FIR_COEF_H2_i registers. Table 10-38 and Table 10-39 resume all coefficients and their respective registers.

10.2.4.10.4.1 Scaling Algorithms

Figure 10-63 and Figure 10-64 show details of the up/downsampling finite state-machines (FSM).

Figure 10-63 shows the vertical up/downsampling FSM.

Figure 10-63. Vertical Up/Downsampling Algorithm

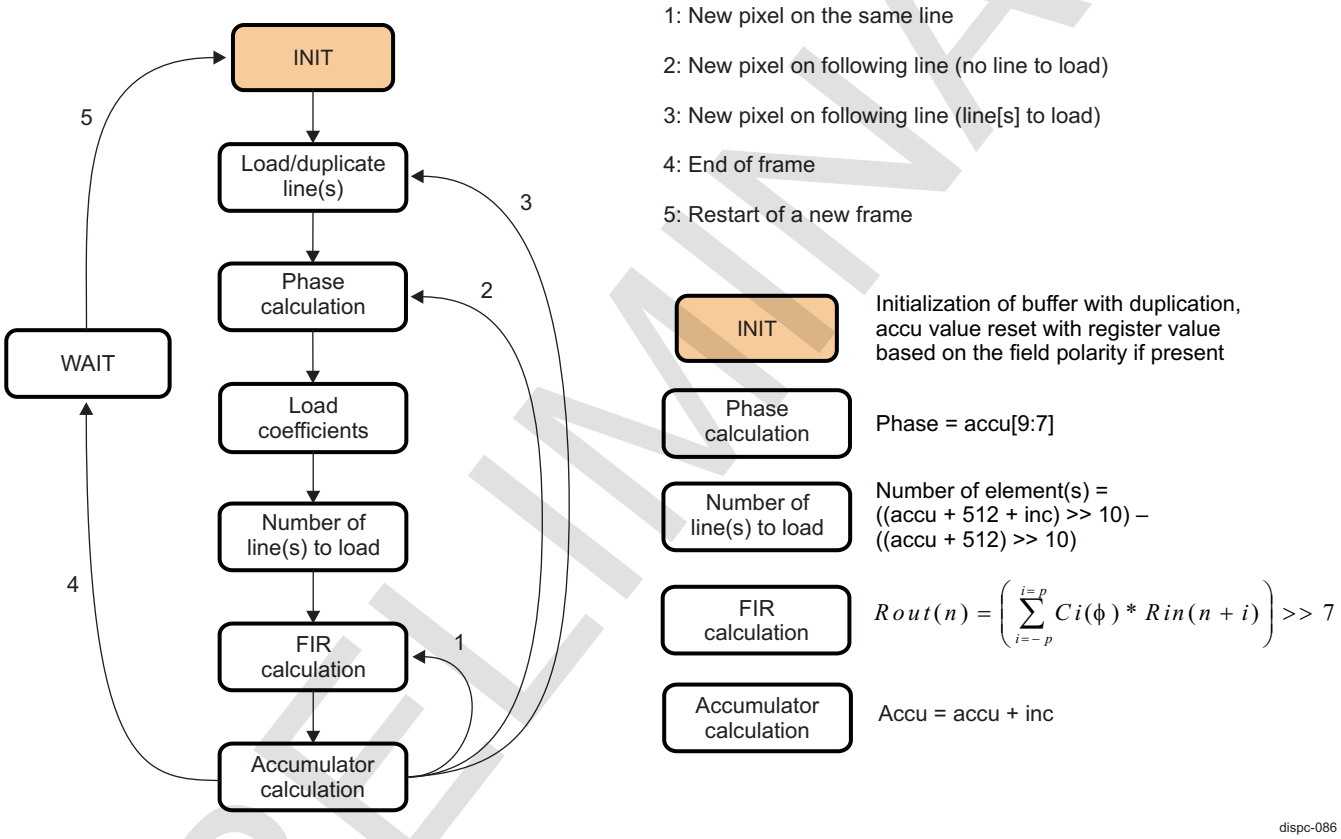

Figure 10-64 shows the horizontal up/downsampling FSM.

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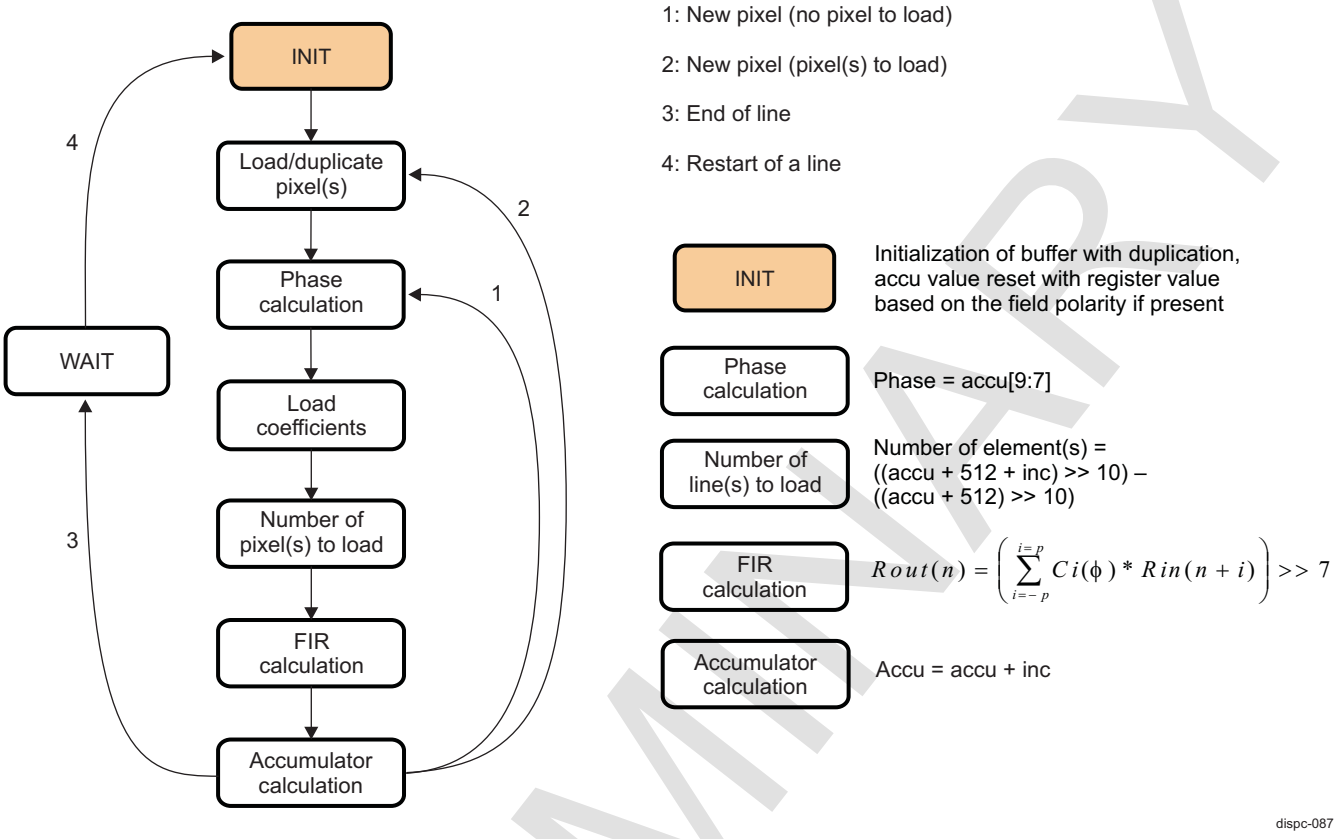
Figure 10-64. Horizontal Up/Downsampling Algorithm



10.2.4.10.4.2 Scaling Limitations

Table 10-41 through Table 10-44 list the minimum ratio between the pixel clock frequency (PCLK) and the functional clock (DISPC_CORE_CLK) in the input pixel format when using the scaler unit. PCLK and FCLK are asynchronous. For each LCD output, there is a dedicated LCD clock that is programmable with the LCD and PCD divisor values in DISPC_DIVISORo[23:16][7:0].

NOTE: The DISPC_CORE_CLK is derived from DISPC_FCLK through the LCD divisor.

Table 10-41. Pixel Clock Frequency Limitations (Any Pixel Format) – Active Matrix Display

DISPC_CORE_CLK/LCDn_PCLK Minimum Ratio	Horizontal Resampling				
	Off	Up	1:1–1:2	1:2–1:3	1:3–1:4
	2(1[(1)]	2(1[(1)])	2	3	4

(1) The minimum ratio can be 1 if the data are output on the rising edge of the PCLK (DISPC_POL_FREQo.IPC = 0); otherwise, the minimum ratio must be 2.

Table 10-42. Pixel Clock Frequency Limitations (Any Pixel Format) Passive Matrix Display – Mono4

DISPC_CORE_CLK/LCDn_PCLK Minimum Ratio	Horizontal Resampling				
	Off	Up	1:1–1:2	1:2–1:3	1:3–1:4
	4	4	8	12	16

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Table 10-43. Pixel Clock Frequency Limitations (Any Pixel Format) Passive Matrix Display – Mono8

DISPC_CORE_CLK/LCDn_PCLK Minimum Ratio	Horizontal Resampling				
	Off	Up	1:1–1:2	1:2–1:3	1:3–1:4
	8	8	16	24	32

Table 10-44. Pixel Clock Frequency Limitations (Any Pixel Format) Passive Matrix Display – Color

DISPC_CORE_CLK/LCDn_PCLK Minimum Ratio	Horizontal Resampling				
	Off	Up	1:1–1:2	1:2–1:3	1:3–1:4
	8	8	16	24	32

10.2.4.11 Write-Back Pipeline

The write-back pipeline is used to store in the system memory the capture of the overlay output or the output of one of the pipelines. The WB pipeline consists of a CSC unit, a scaler unit, and an RGB truncation logic. Because the overlay works on ARGB32-8888 format and the video accelerator works on YUV format, the color space conversion from RGB to YUV is used to directly output to memory the format that can be encoded with no extra processing.

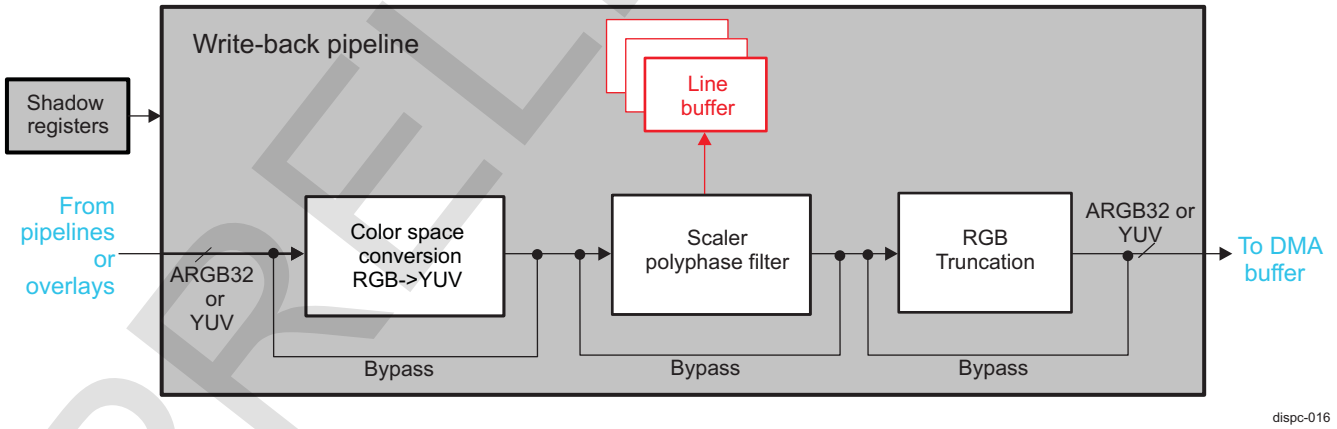
The write-back pipeline is connected to all the pipeline outputs (GFX, VD1, VID2, and VID3 pipelines) and to the output of the three overlay managers (LCD1, LCD2, and TV). The input is selected by setting the DISPC_WB_ATTRIBUTES[18:16] CHANNELIN bit field, and the capture frame rate is set in the DISPC_WB_ATTRIBUTES[26:24] CAPTUREMODE bit field.

Because the output format of the TV overlay manager is ARGB40, the graphics pipeline output is ARGB40, the video pipeline outputs are YUV4:2:2, YUV4:2:0, or ARGB40, and the WB input is ARGB32, the WB input does not consider the 2 LSBs of each ARGB component.

The WB pipeline is enabled by setting the DISPC_WB_ATTRIBUTES[0] ENABLE bit to 0x1.

Figure 10-65 shows the graphics pipeline.

Figure 10-65. Write-Back Pipeline



10.2.4.11.1 CSC Unit RGB to YUV

The RGB-to-YUV CSC unit converts the encoded pixel values from RGB24 into YUV4:4:4 format. For YUV4:2:0 or YUV4:2:2 formats, a chrominance subsampling is required after converting the RGB into YUV values. Because of the subsampling, the following limitations must be considered:

- When converting RGB into YUV4:2:0 NV12 format:
  - Maximum horizontal downscale = x0.5
  - Maximum vertical downscale = x0.5

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- When converting RGB into YUV4:2:2 format:
  - Maximum horizontal downscale = x0.5
  - Maximum vertical downscale = x0.25

Figure 10-66 and Figure 10-67 show the 3 × 3 11-bit coefficients used to convert from RGB24 into YUV4:4:4. The user sets the coefficients according to the standard used to encode the pixel data in YUV color space. Table 10-45 resumes the coefficients with their respective bit fields.

Table 10-45. CSC RGB to YUV Bit Field Setting

Coefficients	Bit Fields
Y_R	DISPC_WB_CONV_COEF0[10:0] YR
Y_G	DISPC_WB_CONV_COEF0[26:16] YG
Y_B	DISPC_WB_CONV_COEF1[10:0] YB
Cr_R	DISPC_WB_CONV_COEF1[26:16] CRR
Cr_G	DISPC_WB_CONV_COEF2[10:0] CRG
Cr_B	DISPC_WB_CONV_COEF2[26:16] CRB
Cb_R	DISPC_WB_CONV_COEF3[10:0] CBR
Cb_G	DISPC_WB_CONV_COEF3[26:16] CBG
Cb_B	DISPC_WB_CONV_COEF4[10:0] CBB

If the active range for the luminance samples (Y) is [16:235] and [16:240] for the chrominance samples (Cb and Cr), the values of Y, Cb, and Cr output components are clipped to the range [0:255]. The range selection is done by setting the DISPC_WB_ATTRIBUTES[11] FULLRANGE bit to 0x0.

Figure 10-66. RGB to YCbCr (FULLRANGE = 0)

$$\begin{bmatrix} Y_{OUT} \\ Cb_{OUT} \\ Cr_{OUT} \end{bmatrix} = \frac{1}{256} * \begin{bmatrix} Y_R & Y_G & Y_B \\ Cb_R & Cb_G & Cb_B \\ Cr_R & Cr_G & Cr_B \end{bmatrix} * \begin{bmatrix} R_{IN} \\ G_{IN} \\ B_{IN} \end{bmatrix} + \begin{bmatrix} 16 \\ 128 \\ 128 \end{bmatrix}$$

dispc-017

If the active range for the luminance samples (Y) and or the chrominance samples (Cb and Cr)is [0:255], the values of Y, Cb, and Cr output components are clipped to the range [0:255]. The range selection is done by setting the DISPC_WB_ATTRIBUTES[11] FULLRANGE bit to 0x1.

Figure 10-67. RGB to YCbCr (FULLRANGE = 1)

$$\begin{bmatrix} Y_{OUT} \\ Cb_{OUT} \\ Cr_{OUT} \end{bmatrix} = \frac{1}{256} * \begin{bmatrix} Y_R & Y_G & Y_B \\ Cb_R & Cb_G & Cb_B \\ Cr_R & Cr_G & Cr_B \end{bmatrix} * \begin{bmatrix} R_{IN} \\ G_{IN} \\ B_{IN} \end{bmatrix} + \begin{bmatrix} 0 \\ 128 \\ 128 \end{bmatrix}$$

dispc-018

10.2.4.11.2 Scaler Unit

The functional aspect of the WB pipeline scaler unit is identical to the video pipeline scaler unit (see Section 10.2.4.10.4), except in the output width when scaling ARGB components. The resulting output format is ARGB32 instead of ARGB40. In addition, the scaling limitations described in Section 10.2.4.10.4.2, *Scaling Limitations*, are relevant only to the video pipelines scaler units. In WB memory-to-memory mode there are no limitations on the DISPC_CORE_CLK/LCDn_PCLK ratio for horizontal resampling.

The programmable coefficients of the polyphase filters are signed 8-bit values (except for the central coefficient, which is unsigned). The WB scaler component has an 8-bit input and an 8-bit output.

Figure 10-68 and Figure 10-69 show the scaler macro-architecture for the component A, R, G, B, and Y. Figure 10-70 and Figure 10-71 show the scaler macro-architecture for component Cr and Cb.

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The scaling output can be clipped to an output range of [0:255] or [16:240] by configuring the DISPC_WB_ATTRIBUTES[11] FULLRANGE bit.

Figure 10-68. Macro-Architecture of the Vertical Scaling for A, R, G, B, and Y Component

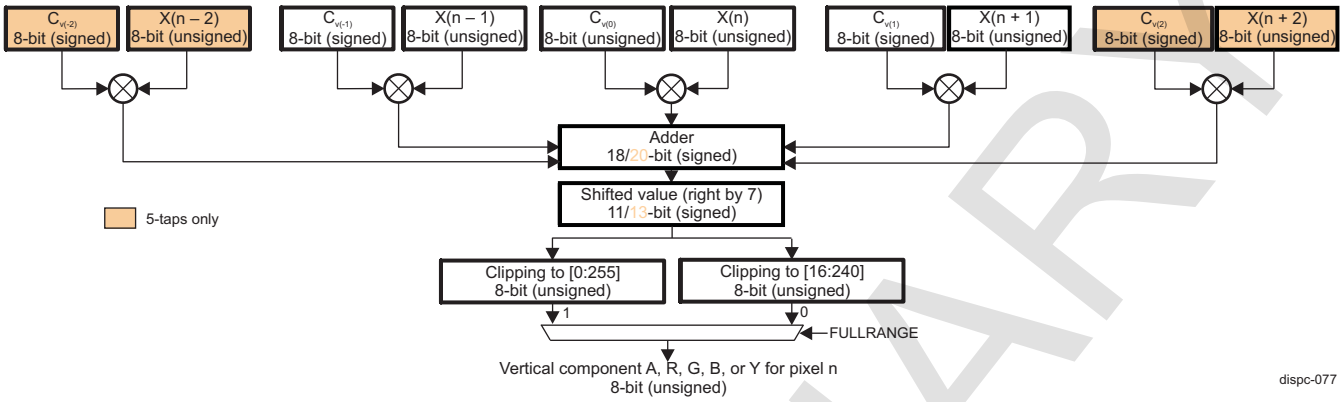

Figure 10-69. Macro-Architecture of the Horizontal Scaling for A, R, G, B, and Y Component

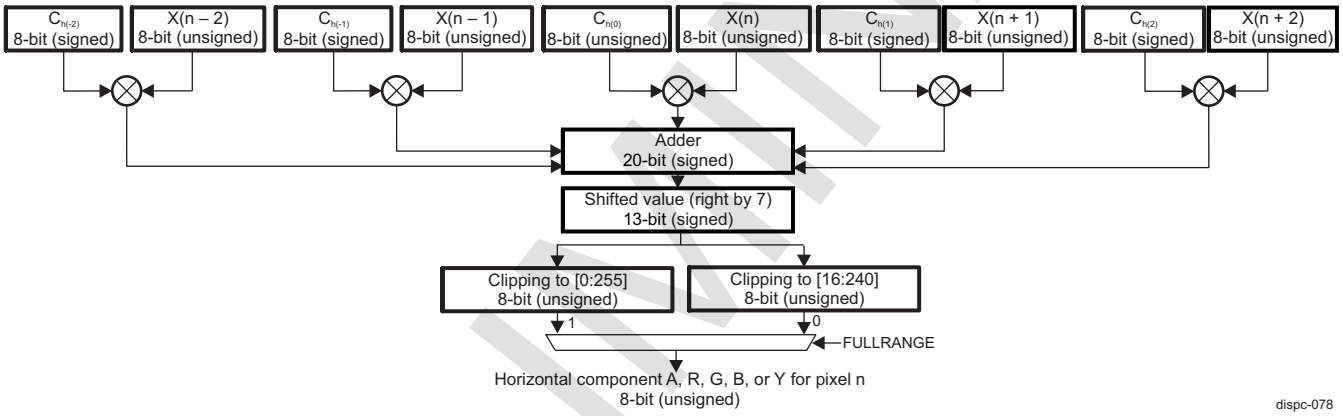

Figure 10-70. Macro-Architecture of the Vertical Scaling for Cr and Cb Component

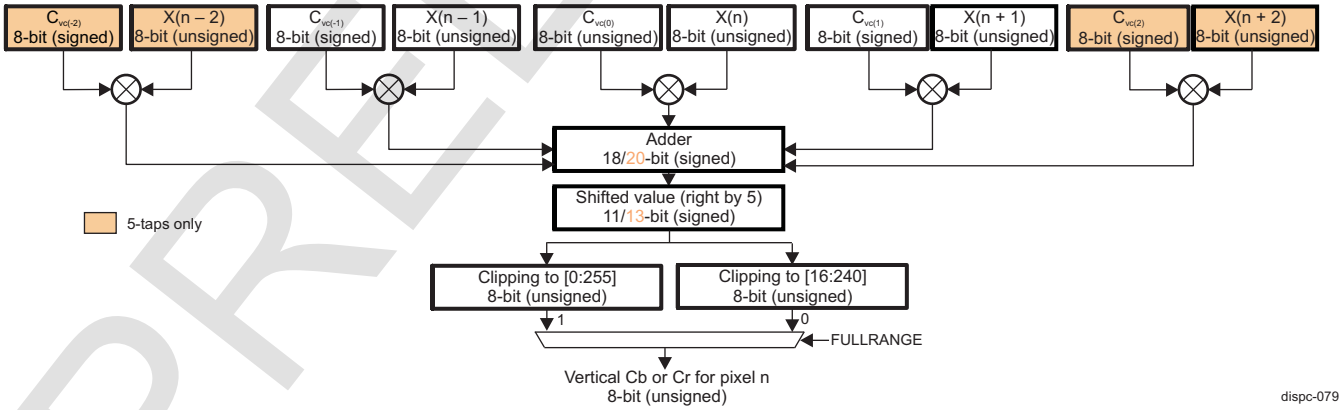

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Figure 10-71. Macro-Architecture of the Horizontal Scaling for Cr and Cb Component

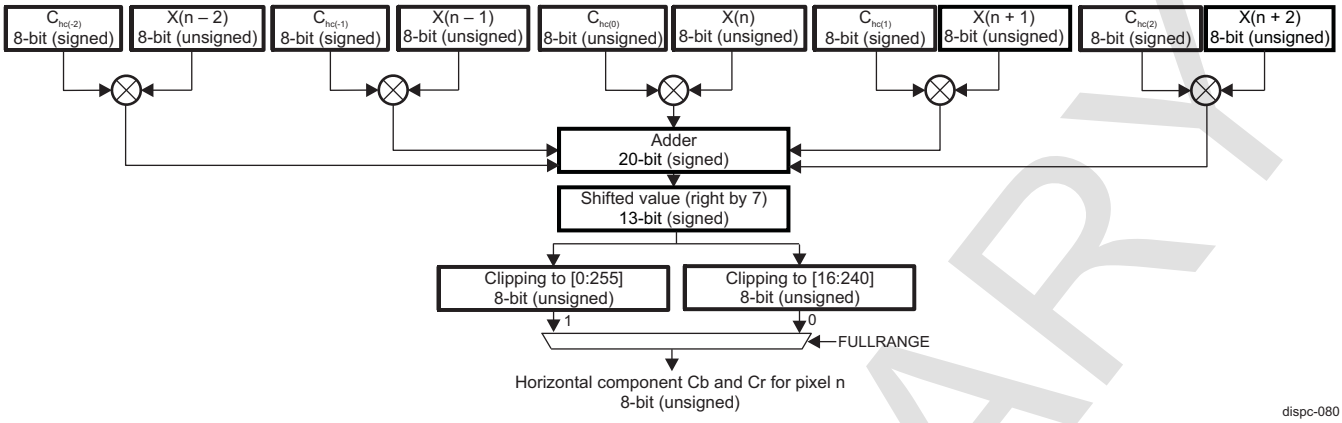

Table 10-46 and Table 10-47 resume all the bit fields in the function to set each coefficient.

Table 10-46. Register Bit Field Associated With Coefficient for ARGB and Y Configuration in WB Scaler

Taps	Coefficient	3 Taps	5 Taps	Registers
		Bit Field	Bit Field	
Vertical	Cv(-2)		FIRVC22	DISPC_WB_FIR_COEF_V_i
	Cv(-1)	FIRVC2	FIRVC2	DISPC_WB_FIR_COEF_HV_i
	Cv(0)	FIRVC1	FIRVC1	DISPC_WB_FIR_COEF_HV_i
	Cv(1)	FIRVC0	FIRVC0	DISPC_WB_FIR_COEF_HV_i
	Cv(2)		FIRVC00	DISPC_WB_FIR_COEF_V_i
Horizontal	Ch(-2)		FIRHC4	DISPC_WB_FIR_COEF_HV_i
	Ch(-1)		FIRHC3	DISPC_WB_FIR_COEF_H_i
	Ch(0)	N/A	FIRHC2	DISPC_WB_FIR_COEF_H_i
	Ch(1)		FIRHC1	DISPC_WB_FIR_COEF_H_i
	Ch(2)		FIRHC0	DISPC_WB_FIR_COEF_H_i

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Table 10-47. Register Bit Field Associated With Coefficient for Cb and Cr Configuration in WB Scaler

Taps	Coefficient	3 Taps	5 Taps	Registers
		Bit Field	Bit Field	
Vertical	Cvc(–2)		FIRVC22	DISPC_WB_FIR_COEF_V2_i
	Cvc(–1)	FIRVC2	FIRVC2	DISPC_WB_FIR_COEF_HV2_i
	Cvc(0)	FIRVC1	FIRVC1	DISPC_WB_FIR_COEF_HV2_i
	Cvc(1)	FIRVC0	FIRVC0	DISPC_WB_FIR_COEF_HV2_i
	Cvc(2)		FIRVC00	DISPC_WB_FIR_COEF_V2_i
Horizontal	Chc(–2)		FIRHC4	DISPC_WB_FIR_COEF_HV2_i
	Chc(–1)		FIRHC3	DISPC_WB_FIR_COEF_H2_i
	Chc(0)	N/A	FIRHC2	DISPC_WB_FIR_COEF_H2_i
	Chc(1)		FIRHC1	DISPC_WB_FIR_COEF_H2_i
	Chc(2)		FIRHC0	DISPC_WB_FIR_COEF_H2_i

The WB scaler unit vertical or/and horizontal sampling is defined by setting/resetting the DISPC_WB_ATTRIBUTES[6:5] RESIZEENABLE bit.

A set of configuration must be valid before enabling the video up/downsampling block.

The following fields define the configuration of the video up/downsampling block for WB:

- Vertical up/downsampling increments the value of the DISPC_WB_FIR[28:16] FIRVINC bit field. The unsigned integer value range is [1:4096]. Software calculates the value using the following equation:

$$FIRVINC = 1024 * \left(\frac{ORGSIZEY}{SIZEY}\right)$$

dispc-066 (12)

NOTE:

- If the value of the DISPC_WB_FIR[28:16] FIRVINC bit field is greater than 4096, it is clipped to 4096.
- If the DISPC_WB_SIZE[26:16] SIZEY bit field equals 0x1, SIZEY is replaced by 0x2 in the previous equation.
- The values of the DISPC_WB_PICTURE_SIZE[26:16] ORGSIZEY and DISPC_WB_SIZE[26:16] SIZEY bit fields must be programmed with the value desired minus 1.

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- Horizontal up/downsampling increments the value of the DISPC_WB_FIR[12:0] FIRHINC bit field: The unsigned integer value range is [1:4096]. Software calculates the value using the following equation:

$$FIRHINC = 1024 * \left(\frac{ORGSIZEX}{SIZEX}\right)$$

dispc-067 (13)

NOTE:

- If the value of the DISPC_WB_FIR[12:0] FIRHINC bit field is greater than 4096, it is clipped to 4096.
- If the DISPC_WB_SIZE[10:0] SIZEX bit field equals 1, the DISPC_WB_SIZE[10:0] SIZEX bit field is replaced by 2 in the previous equation.
- The value of the DISPC_WB_PICTURE_SIZE[10:0] ORGSIZEX and DISPC_WB_SIZE[10:0] SIZEX bit fields must be programmed with the value desired minus 1.

- Vertical up/downsampling accumulator value DISPC_WB_ACCU_j[26:16] VERTICALACCU bit field: The signed integer value range is [–1024:1023]. The accumulator value indicates on which phase the vertical filtering starts. The register DISPC_WB_ACCU_0 is used for progressive output and for interlace output; the DISPC_WB_ACCU_0 and DISPC_WB_ACCU_1 registers are used. Similarly, DISPC_WB_ACCU2_0 and DISPC_WB_ACCU2_1 are used in progressive or interlace output to set the accumulator value of the Cb and Cr components when scaling YUV format.
- Vertical up/downsampling line buffer configuration DISPC_WB_ATTRIBUTES[21] VERTICALTAPS bit: The default value at reset time is 0x0 (3-tap configuration is used). If the bit field is reset, the 3-tap configuration is used.
- Horizontal up/downsampling accumulator value DISPC_WB_ACCU_j[10:0] HORIZONTALACCU bit field: The signed integer value range is [–1024:1023]. The accumulator value indicates on which phase the horizontal filtering starts. The register DISPC_WB_ACCU_0 is used for progressive output and for interlace output; the DISPC_WB_ACCU_0 and DISPC_WB_ACCU_1 registers are used. Similarly, DISPC_WB_ACCU2_0 and DISPC_WB_ACCU2_1 are used in progressive or interlace output to set the accumulator value of Cb and Cr components when scaling YUV format.

Table 10-48. Vertical/Horizontal Accumulator Phase

Accumulator Value	Phases f
0	0
128 or –896	1
256 or –768	2
384 or –640	3
512 or –512	4
640 or –384	5
768 or –256	6
896 or –128	7

- Vertical up/downsampling coefficients:
  - The 3-tap vertical up/downsampling coefficients are defined in the DISPC_WB_FIR_COEF_HV_i registers. There are 8 registers for the 8 phases with 3 coefficients for each, or a total of 24 programmable coefficients for the vertical up/downsampling block. Each register contains two 8-bit signed coefficients and one 8-bit unsigned coefficient (the central one).
  - The 5-tap vertical up/downsampling coefficients: Two extra-tap vertical up/downsampling coefficients are defined in the DISPC_WB_FIR_COEF_V_i registers. There are 8 registers for the 8 phases with 2 coefficients for each of them, so a total of 16 programmable coefficients for the vertical up/downsampling block are used in addition to the 3-tap registers previously defined.

  Four YUV vertical up/downsampling coefficients are set in the DISPC_WB_FIR_COEF_HV2_i and DISPC_WB_FIR_COEF_V2_i registers. Table 10-46 and Table 10-47 resume all coefficients and their respective registers.
- Horizontal up/downsampling coefficients:

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– The DISPC_WB_FIR_COEF_H_i and DISPC_WB_FIR_COEF_HV_i registers define the 5-tap horizontal up/downsampling coefficients. Each DISPC_WB_FIR_COEF_H_i register contains three 8-bit signed coefficients and one 8-bit unsigned coefficient (the central one). Each DISPC_WB_FIR_COEF_HV_i register contains one 8-bit signed coefficient. A total of 40 programmable coefficients for the horizontal up/downsampling block are used.

Four YUV horizontal up/downsampling coefficients are set in the DISPC_WB_FIR_COEF_HV2_i and DISPC_WB_FIR_COEF_H2_i registers. Table 10-46 and Table 10-47 resume all coefficients and their respective registers.

10.2.4.11.3 RGB Truncation Logic

Truncation logic is used to convert a pixel from ARGB 32-bit format into a lower color depth: 12-or 16-bit format based. Setting the DISPC_WB_ATTRIBUTES[10] TRUNCATIONENABLE bit to 0x1 enables the truncation to the pixel format defined by the DISPC_WB_ATTRIBUTES[4:1] FORMAT bit field. The truncation is done by removing the necessary LSB of each component to match the output format. Table 10-49 describes the truncation done on each component of the pixel.

Table 10-49. Truncation Logic

	A[7:0]	R[7:0]	G[7:0]	GB[7:0]
Output Formats	**MSB LSB**	**MSB LSB**	**MSB LSB**	**MSB LSB**
xRGB12-4444	Ignored	R[7:4]	G[7:4]	B[7:4]
RGBx12-4444	Ignored	R[7:4]	G[7:4]	B[7:4]
RGB16-565	Ignored	R[7:3]	G[7:2]	B[7:3]
xRGB16-1555	Ignored	R[7:3]	G[7:3]	B[7:3]
ARGB16-4444	A[7:4]	R[7:4]	G[7:4]	B[7:4]
RGBA16-4444	A[7:4]	R[7:4]	G[7:4]	B[7:4]
ARGB16-1555	A[7]	R[7:3]	G[7:3]	B[7:3]

NOTE: If there is no alpha field in the pixel format description, 0s or 1s must fill the container. 0s must be used for transparent and 1s for opaque. For example, in xRGB12 pixel format, the upper 4 bits are set to 0s because the RGB value is only 12 bits inside a 16-bit container.

10.2.4.12 LCD Outputs

The LCD1 and LCD2 output paths consist of several processing blocks (see Figure 10-72):

- Overlay manager
- Gamma correction unit
- Color phase rotation (CPR) is also used for RGB-to-YUV conversion.
- Active matrix dithering with TDM
- Passive matrix dithering
- Synchronization buffer
- Timing generator

The display subsystem supports two types of display technologies (both monochrome and color modes):

- Passive matrix displays: supporting up to 16, 256, or 3375 colors to be displayed in each frame, depending on the color depth. The monochrome LCD has 15 grayscale levels available.
- Active matrix displays: the configuration of colors depends on the color depth:
  - 24 BPP supports 16,777,216 colors.
  - 18 BPP supports 262,144 colors.
  - 16 BPP supports 65,536 colors.
  - 12 BPP supports 4096 colors.

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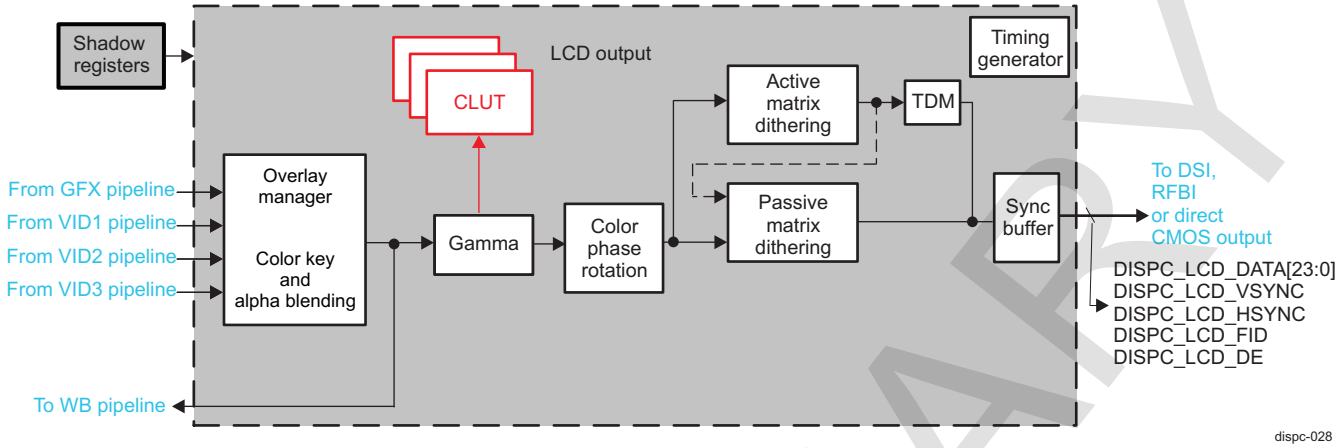
Figure 10-72. LCD Output Architecture



10.2.4.12.1 Overlay Manager

The overlay mechanism consists of displaying more than one layer (GFX, VID1 to VID3 layers) using:

- A priority rule based on a Z-order: Application can set the ordering layer of the frames.
- Transparency color keys: Destination and source transparency color keys can be set.
- Alpha blending values: Using the A component of a pixel or a blending set by the user for a layer, a level of transparency can be determined.

Each pipeline (GFX, VID1, VID2, and VID3) is assigned to a single overlay and, as a consequence, to a single display controller output, LCD1, LCD2, TV, or WB pipeline. An overlay manager can be connected to all four pipelines outputs simultaneously. The pipeline output is directed using the DISPC_GFX_ATTRIBUTES[8] CHANNELOUT bit and the DISPC_VIDp_ATTRIBUTES[31:30] CHANNELOUT2 bit field. Table 10-50 resumes the bit field settings to direct a pipeline to an LCD/TV or WB output. The default value directs all pipelines to LCD1.

Table 10-50. Pipeline Connection to LCD, TV, or WB Output

Overlay Manager/Output	DISPC_GFX_ATTRIBUTES/DISPC_VIDp_ATTRIBUTES	
	CHANNELOUT Bit	CHANNELOUT2 Bit Field
LCD1	0x0	0x0
LCD2	0x0	0x1
WB	0x0	0x3
TV	0x1	0x0 (or 0x2 for VID2; see the following Note)

NOTE: The combination of settings CHANNELOUT = 0x1 and CHANNELOUT2 = 0x1, 0x2, or 0x3 is reserved for the VID1 and VID3 pipelines. For the VID2 pipeline, this combination is reserved when any TV format other than HDMI 1.4 3D 1080p is to be output. Setting the DISPC_VID2_ATTRIBUTES register bit fields CHANNELOUT to 0x1 and CHANNELOUT2 to 0x2, is used in case of HDMI 1.4 3D 1080p format. For more information, see Section 10.2.4.13.4, *Timing and TV Format Settings*.

The output of each LCD overlay manager is connected to CPR block through the palette unit in the case of Gamma correction.

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NOTE:

- When the pixel format is ARGB or RGBA, the color key match logic uses only the RGB value defined by ARGB or RGBA. The alpha blending factor is ignored.
- For LCD1 output, the same CLUT is used for BITMAP support by the graphics pipeline and for Gamma correction. In case of BITMAP format for graphics, Gamma correction is not available on the primary LCD output.

10.2.4.12.1.1 Priority Rule

The overlay manager is configured using the Z-order parameter. The Z-order value defined for each pipeline indicates the visibility order to the window on the screen. If the Z-order value of window A is lower than the Z-order to layer B, layer A is displayed below layer B. The transparency color keys and the alpha blending factors are then used to blend the layers together (see Section 10.2.4.12.1.2 and Section 10.2.4.12.1.3). The Z-order is enabled by setting the DISPC_GFX_ATTRIBUTES[25] ZORDERENABLE bit or the DISPC_VIDp_ATTRIBUTES[25] ZORDERENABLE bit to 0x1 and by defining the Z-order in the DISPC_GFX_ATTRIBUTES[27:26] and DISPC_VIDp_ATTRIBUTES[27:26] ZORDER bit fields. Table 10-51 resumes the register settings to enable and set the Z-order of a pipeline. Table 10-51 shows the default Z-order values when LCDALPHABLENDERENABLE and ZORDERENABLE are disabled.

Table 10-51. Z-Order Register Settings and Default Configuration

Pipeline	LCDALPHA BLENDERENABLE (1)	ZORDERENABLE	ZORDER	Resulting Z-Order Number
GFX	0	0	Don't care	0
	0	1	ZORDER	ZORDER
	1	Don't care	Don't care	3
VID1	0	0	Don't care	1
	0	1	ZORDER	ZORDER
	1	Don't care	Don't care	0
VID2	0	0	Don't care	2
	0	1	ZORDER	ZORDER
	1	Don't care	Don't care	1
VID3	0	0	Don't care	3
	0	1	ZORDER	ZORDER
	1	Don't care	Don't care	2

(1) Applies only to LCD1

Figure 10-73 shows the architecture of the priority rule.

NOTE:

- If ZORDERENABLE = 1, each Z-order must be different for each active pipeline. It is not possible to use the same value for more than one pipeline.
- Two modes are maintained for backward compatibility with OMAP3430:
  - LCDALPHABLENDERENABLE = 0 and ZORDERENABLE = 0 equivalent to the normal mode overlay settings
  - LCDALPHABLENDERENABLE = 1 equivalent to the alpha mode overlay settings
- When OMAP3430 backward compatibility mode is to be used, the following must be considered:
  - If Z-order is disabled for the VID1 and VID2 pipelines, the pipeline data is output on the LCD1/LCD2/TV overlay.
  - If Z-order is disabled for the VID3 pipeline, the pipeline data is output only on the LCD2 overlay.

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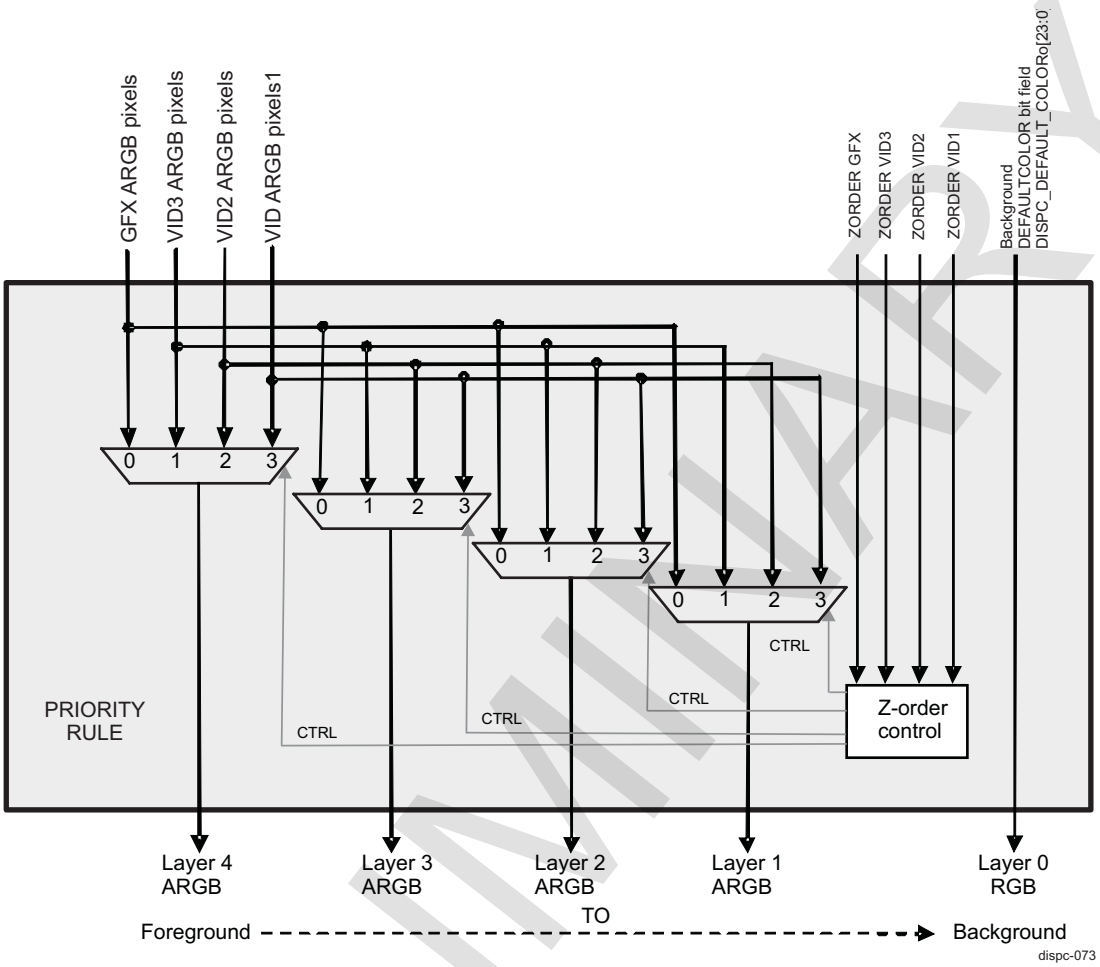
Figure 10-73. Priority Rule Architecture



The height and width of each enabled layer (pipeline) must be defined in the SIZEX and SIZEY bit fields DISPC_GFX_SIZE[26:16][10:0]/ DISPC_VIDp_SIZE[26:16][10:0], and its x and y positions defined in the POSX and POSY bit fields DISPC_GFX_POSITION[26:16][10:0]/DISPC_VIDp_POSITION[26:16][10:0]. If there are no graphics or video-encoded pixels at a specific position, the programmable, solid background color appears. The solid background color is set in the DISPC_DEFAULT_COLOR[23:0] DEFAULTCOLOR bit field. Figure 10-74 is an example of priority rule.

The Z-order reordering block must always map the pipelines to the blender logic in the same order—from background to foreground.

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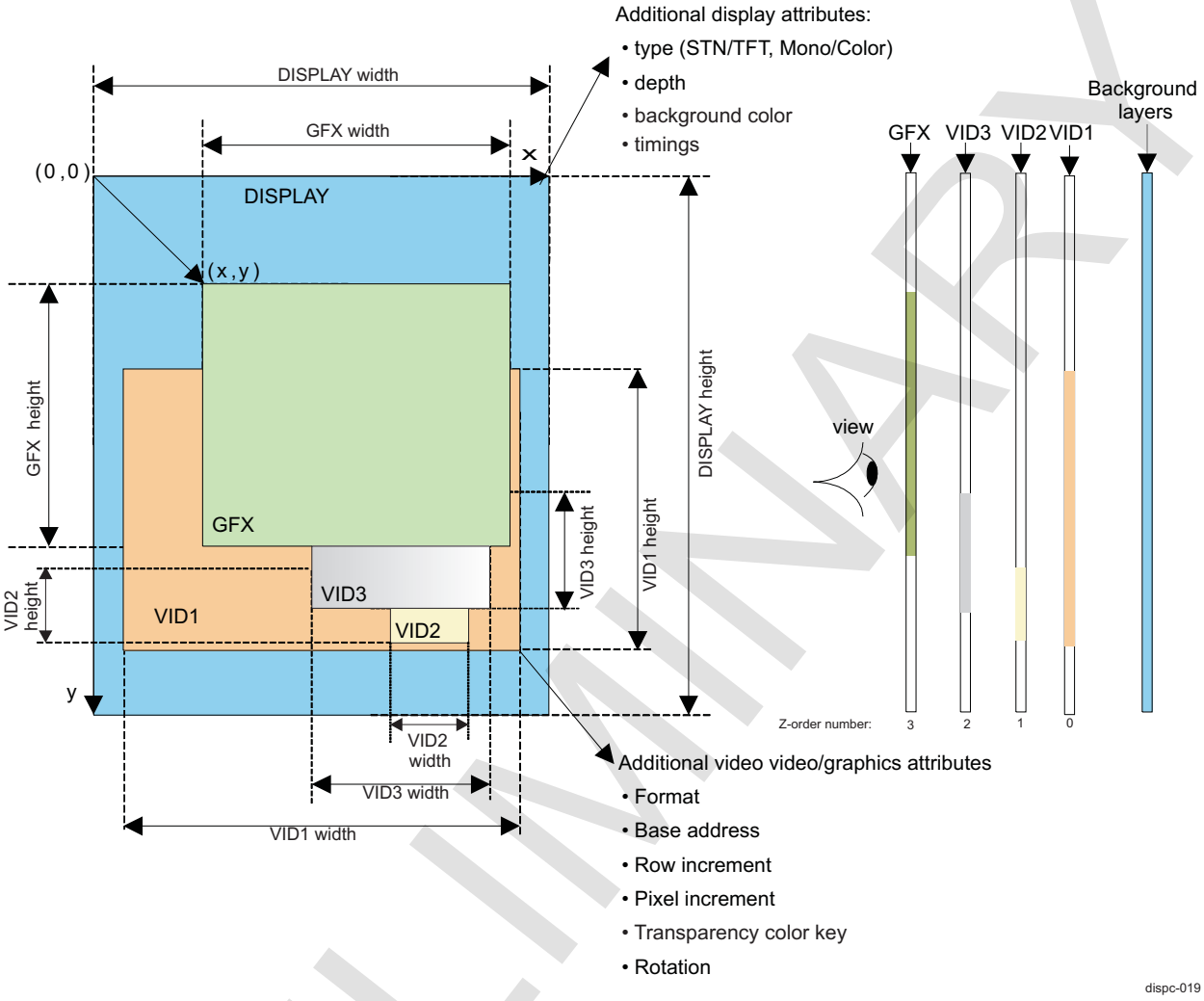
Figure 10-74. Example of Priority Rule: From Lower to Higher VID1, VID2, VID3, GFX



10.2.4.12.1.2 Alpha Blender

Figure 10-75 shows the alpha blending processing in detail.

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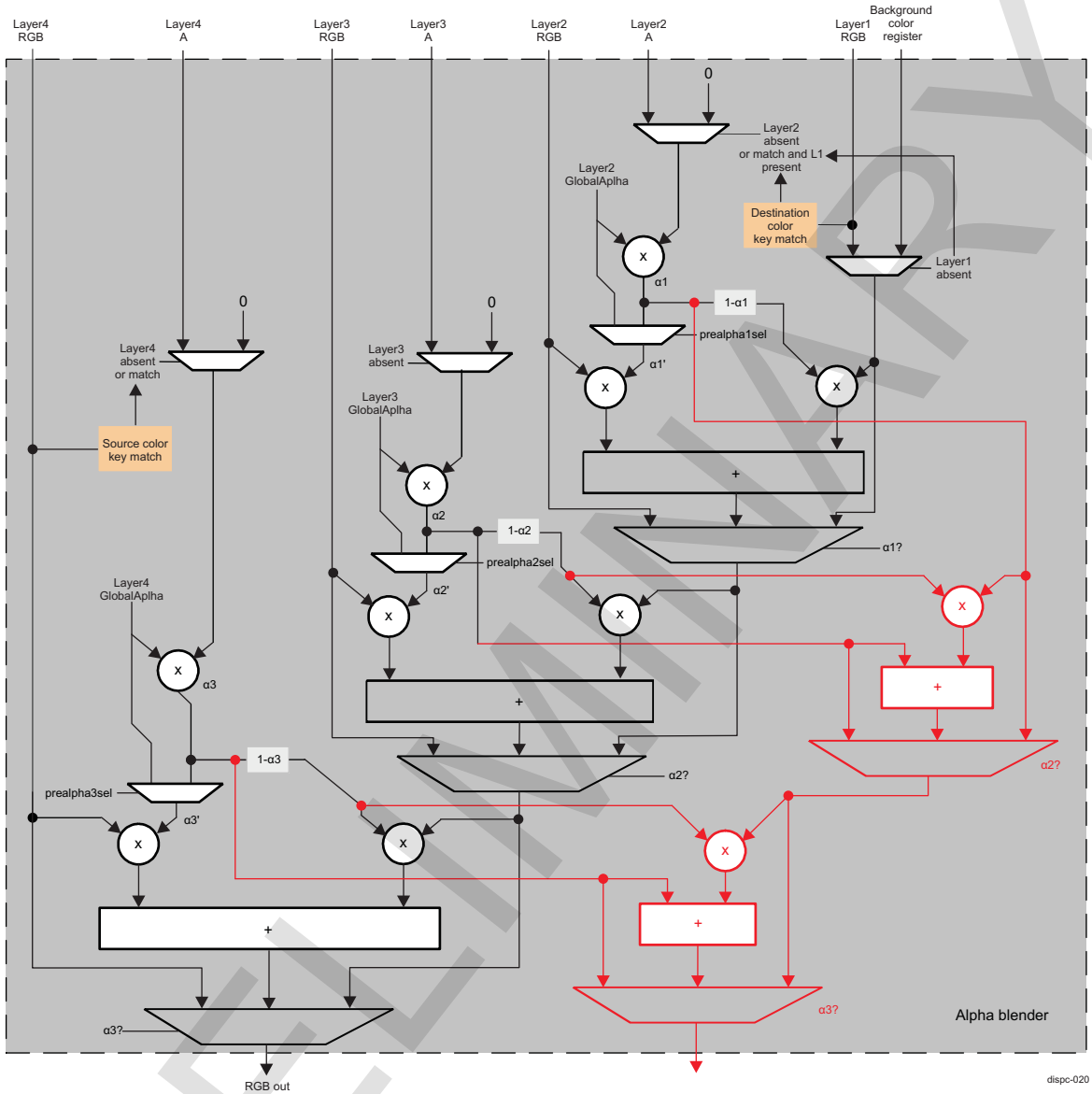
Figure 10-75. Alpha Blending Architecture With Premultiplied Alpha Support



NOTE: "1-alpha" operator corresponds to the basic 1s-complement operation.

The alpha blending value is defined by:

- The component value A when using an ARGB or RGBA pixel format.
  - For ARGB-1555, the alpha blending is defined using a 1-bit value. It is converted into an 8-bit value by duplicating the 1-bit value (see Table 10-52).
  - For ARGB-4444, the alpha blending is defined using a 4-bit value. It is converted into an 8-bit value by duplicating the 4-bit value (see Table 10-52).
  - If the pixel format contains no alpha blending value, the pixel alpha value is considered to be 0xFF and if alpha is equal to 0xFF, there is no multiplication.
  - For BITMAP or YUV formats, there is no alpha blending factor associated with each pixel value. Only the global alpha blending factor associated with the window displaying the BITMAP or YUV format is used.
- The global alpha blending value set in the individual bit fields of the DISPC_GLOBAL_ALPHA[31:0]

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register for LCD:

- VID3GLOBALALPHA
- VID2GLOBALALPHA
- VID1GLOBALALPHA
- GFXGLOBALALPHA

- A total alpha blending value can be used when a combination of the pixel alpha blending value A and a global alpha blending is present. The resulting alpha value is determined as : Alpha = (Pixel Alpha * Global Alpha) / 2.

Table 10-52 lists the percentage of alpha blending in the function of the alpha blending value on 8 bits.

Table 10-52. Alpha Blending – ARGB

Alpha Blending 1-Bit Value	Alpha Blending 4-Bit Value	Alpha Blending 8-Bit Value (Converted Value or Resulting Alpha)	% Blending
0x0	0x0	0x00	100% (transparent)
N/A	0x1	0x11	93.33%
N/A	0x2	0x22	86.6%
N/A	...	...	...
N/A	0xE	0xEE	6.6%
0x1	0xF	0xFF	0% (opaque)

Premultiplied Alpha

The image ARGB may have its RGB component already premultiplied with the alpha (ARGB) where:

- R = A*R
- G = A*G
- B = A*B

In that case, the processing is as follows:

- Color component of premultiplied layers are multiplied with the Global Alpha, if Global Alpha is not equal to 0.
- Color component of the composed underlying layers are multiplied with (1-A) * Global Alpha

The additional premultiplied alpha option is associated with the pipelines GFX, VID1, VID2, and VID3. The option is accessible through the [28] PREMULTIPLYALPHA bit for the respective pipeline register:

- DISPC_GFX_ATTRIBUTES
- DISPC_VID1_ATTRIBUTES
- DISPC_VID2_ATTRIBUTES
- DISPC_VID3_ATTRIBUTES

The following settings are available:

- PREMULTIPLYALPHA bit = 0: Source is not premultiplied with alpha. Full blending is done in the DISPC.
- PREMULTIPLYALPHA bit = 1: Source is premultiplied with alpha. Partial blending is done.

NOTE: The *prealphasel* controls in Figure 10-75, correspond to the PREMULTIPLYALPHA of the pipelines mapped on the respective layers.

The logic marked in red color in Figure 10-75 corresponds to the alpha value, computed when the Write Back channel copies back to memory the premultiplied color component: *A(destination) = A(source)+ (1-A(source)*A(destination))*

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When DISPC_WB_ATTRIBUTES[7] ALPHAENABLE bit is cleared, or when the overlay channel is not selected for WB, the computation of the A(destination) is disabled. The default value for DISPC_WB_ATTRIBUTES[7] ALPHAENABLE bit is 0x0. When the WB is configured to copy back one of the output channels (output of overlay), the following configurations are available:

- ALPHAENABLE bit is set to 0x1: The WB pipe copies back to memory the premultiplied alpha calculated through the overlay.
- ALPHAENABLE bit is set to 0x0: The alpha value is not written back.

NOTE: The DISPC_WB_ATTRIBUTES[7] ALPHAENABLE bit is effective only when one of the output channels is written back, otherwise it is ignored.

10.2.4.12.1.3 Transparency Color Keys

The two transparency color keys are the source transparency color key and the destination transparency color key. The transparency color key can be used only with BITMAP formats (1-, 2-, 4-, and 8-bits per pixel) and RGB formats (ARGB, RGB, RGBA, and RGBx). in this case the A information is ignored for the comparison between the pixel value and the color key value. It is possible to use YUV formats with some care because the comparison is between the input pixel value of the overlay manager from pipeline (GFX or one of the VID pipelines depending on the Z-order) and the color key value. The YUV data is converted to RGB format. If the original format is YUV, the user must consider the color space conversion processing to define the RGB color key value used for the comparison.

The transparency color key is enabled by setting the following bits to 0x1:

- DISPC_CONFIG1[10] TCKLCDENABLE for LCD1
- DISPC_CONFIG2[10] TCKLCDENABLE for LCD2
- DISPC_CONFIG1[12] TCKTVENABLE for TV

The transparent color key is determined in the following bit fields.

- DISPC_TRANS_COLOR0[23:0] TRANSCOLORKEY for LCD1
- DISPC_TRANS_COLOR2[23:0] TRANSCOLORKEY for LCD2
- DISPC_TRANS_COLOR1[23:0] TRANSCOLORKEY for TV

NOTE:

- The video source transparency color key and graphics destination transparency color key cannot be active at the same time.
- For CLUT bitmaps, the palette index is compared to the transparency color key and not to the palette value pointed out by the palette index.

- Video source transparency color key

  The video source transparency color key value defines the encoded pixel data considered as transparent pixel. The encoded pixel values with the source color key value are not visible and the under layers encoded pixel values or solid background color are visible (the pixel alpha blending value of layer 4 is forced to 0x00, fully transparent).

  The scaler can be enabled as a preprocessing in the VID pipeline. But it is necessary to consider the pixel scaling preprocessing in order to define the color key value to be used after the rescaling for the comparison between the input pixel value to the overlay manager and the color key value.

  The source transparency color key mode is selected by setting the following bits to 0x1:

  – DISPC_CONFIG1[11] TCKLCDSELECTION bit for LCD1
  – DISPC_CONFIG2[11] TCKLCDSELECTION bit for LCD2
  – DISPC_CONFIG1[13] TCKTVENABLE bit for TV

  Figure 10-76 shows an example of source color key. The pixels with the transparency color key are not displayed; instead, pixels of the resulting layer underneath are shown.

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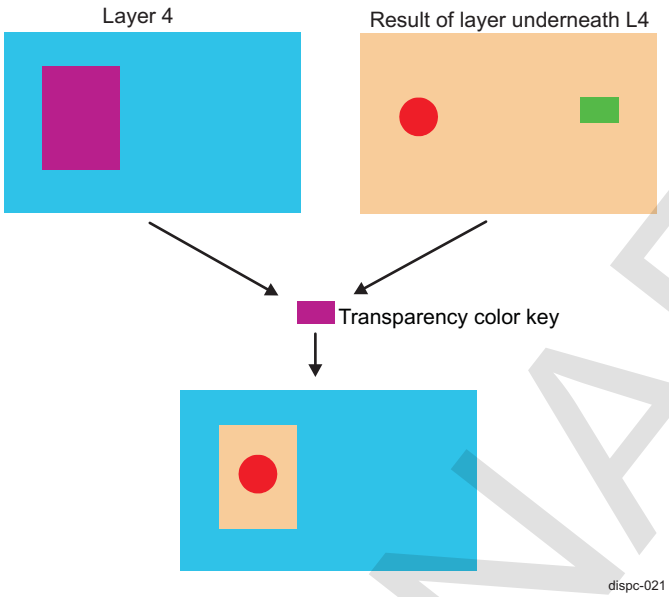
Figure 10-76. Source Transparency Color Key Example



- Graphics destination transparency color key value

  The graphics destination transparency color key value defines the encoded pixels in layer 1 which are not displayed. Other layer 1 pixels (nonequal to destination transparency color key) are displayed over layer 2. The encoded pixel values with the destination color key value are pixels not visible on the screen because pixels at the same position in layer 2 are visible otherwise encoded pixels are visible above layer 2 . The destination transparency color key is applicable only if layer 1 overlaps layer 2 (refer to the Z-order section for details on layer position depending on the Z-order parameter, Section 10.2.4.12.1.1, *Priority Rule*); otherwise, the destination transparency color key is ignored.

  The scaler can be enabled as a preprocessor in the VID pipeline. It is necessary, however, to consider the pixel scaling preprocessing to define the color key value to be used after rescaling for the comparison between the input pixel value to the overlay manager and the color key value.

  The destination transparency color key mode is selected by setting the following bits to 0x0:

  – DISPC_CONFIG1[11] TCKLCDSELECTION bit for LCD
  – DISPC_CONFIG2[11] TCKLCDSELECTION bit for LCD2
  – DISPC_CONFIG1[13] TCKTVSELECTION bit for TV

  Figure 10-77 shows an example of the destination color key. The pixels, equal to the transparency color key, are not displayed and are replaced by layer 2 pixels. All other layer 1 pixels, different from the transparency color key, are displayed over layer 2.

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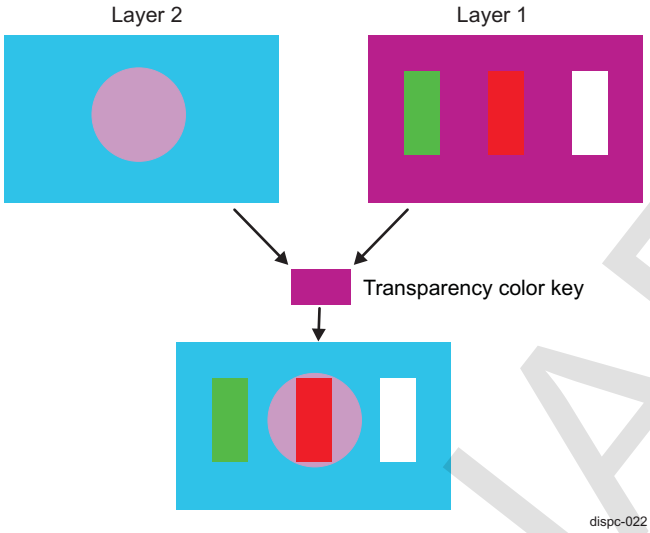
Figure 10-77. Destination Transparency Color Key Example



10.2.4.12.1.4 Overlay Optimization

The overlay optimization consists in fetching only the required pixels meaning pixels that contribute to the final picture to be displayed (LCD1, LCD2, or TV). The decision to fetch the pixel from memory is based on the information available in the registers and on the following rules:

- The layer is enabled.
- The global alpha blending factor for the layer is different than 0x00.
- The current layer is behind an nonopaque layer (global alpha blending factor is different than 0xFF for the layer in the preceding).

The result of the overlay optimization is a reduction of the bandwidth by fetching only the mandatory pixels. The overlay mechanism is independent for each overlay: LCD1, LCD2, and TV. Because each layer (GFX, VID1, VID2, and VID3) can be associated to only one overlay at a time, it is possible to optimize the fetch of the pixels for each layer based on the overlay information. The overlay optimization must be run on the DMA engine time window and not on the display time window. The pixels are fetched by the DMA engine before the display processing.

The overlay optimization is enabled by setting the following bits to 0x1:

- DISPC_CONTROL1[12] OVERLAYOPTIMIZATION bit for LCD1
- DISPC_CONTROL2[12] OVERLAYOPTIMIZATION bit for LCD2
- DISPC_CONTROL2[13] TVOVERLAYOPTIMIZATION bit for TV

NOTE:

- The overlay optimization is not functional when a layer is using BITMAP1, BITMAP2, or BITMAP4 pixel formats.
- The pixel alpha blending factor in case of ARGB and RGBA formats cannot be used to take advantage of the pixel fully transparent (alpha blending factor equals 0x00).

10.2.4.12.2 Gamma Correction Unit

In gamma curve mode, the selected encoded pixel values based on the color keys by the overlay manager from the video or graphics paths are sent to the gamma curve table. Each component of encoded pixel value is used as a pointer to index one out of 256 24-bit gamma curve entries in the table.

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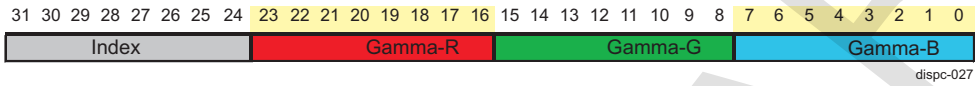
Each 8-bit component is replaced with the 8-bit table value corresponding to R, G, or B component. The table is loaded by software. It is possible to load only part of the table. For each access to the table, the 24-bit value is associated with index in the table by concatenating the 24-bit value (LSB of 32-bit access) and the 8-bit index value (MSB of the 32-bit access). Figure 10-78 describes the format of one of the gamma curve values in the memory.

NOTE: If the CLUT is used in the GFX pipeline for palette, the gamma correction unit is not available on the primary LCD.

Figure 10-78. Data Memory Organization for Gamma Mode in LCD Output



10.2.4.12.3 CPR Unit

The CPR unit can be used to correct the LCD output colorimetry in case of nonpure white backlight.

The CPR is enabled by setting the DISPC_CONFIGo[15] CPR bit to 0x1. The coefficients are programmed in the following registers:

- Red 10-bit signed coefficients in DISPC_CPRo_COEF_R
- Green 10-bit signed coefficients in DISPC_CPRo_COEF_G
- Blue 10-bit signed coefficients in DISPC_CPRo_COEF_B

The color phase rotation can be selected for passive and active matrix panel. The logic is integrated after the LCD overlay manager or the palette while using the gamma correction and before the spatial/temporal dithering. The color phase rotation can be selected to correct the nonpure white backlight of the LCD module by using a programmable matrix to convert the 24-bit RGB pixel value into a new 24-bit RGB pixel value. The matrix is programmed through a set of nine 10-bit signed coefficients. The output of the calculation is clipped to [0:255]. The color phase rotation is processed by the equation shown in Figure 10-79. Table 10-53 lists all coefficients with their respective bit field registers for settings.

Figure 10-79. Color Phase Rotation Matrix

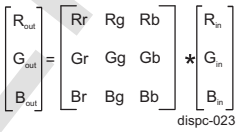


Table 10-53. CPR or RGB to YUV Coefficients With Associated Bit Fields

Registers	Bit Field	Color Space Conversion	RGB to YUV
DISPC_CPRo_COEF_R	RR	Rr	Yr
	RG	Rg	Yg
	RB	Rb	Yb
DISPC_CPRo_COEF_G	GR	Gr	Cbr
	GG	Gg	Cbg
	GB	Gb	Cbb
DISPC_CPRo_COEF_B	BR	Br	Crr
	BG	Bg	Crg
	BB	Bb	Crb

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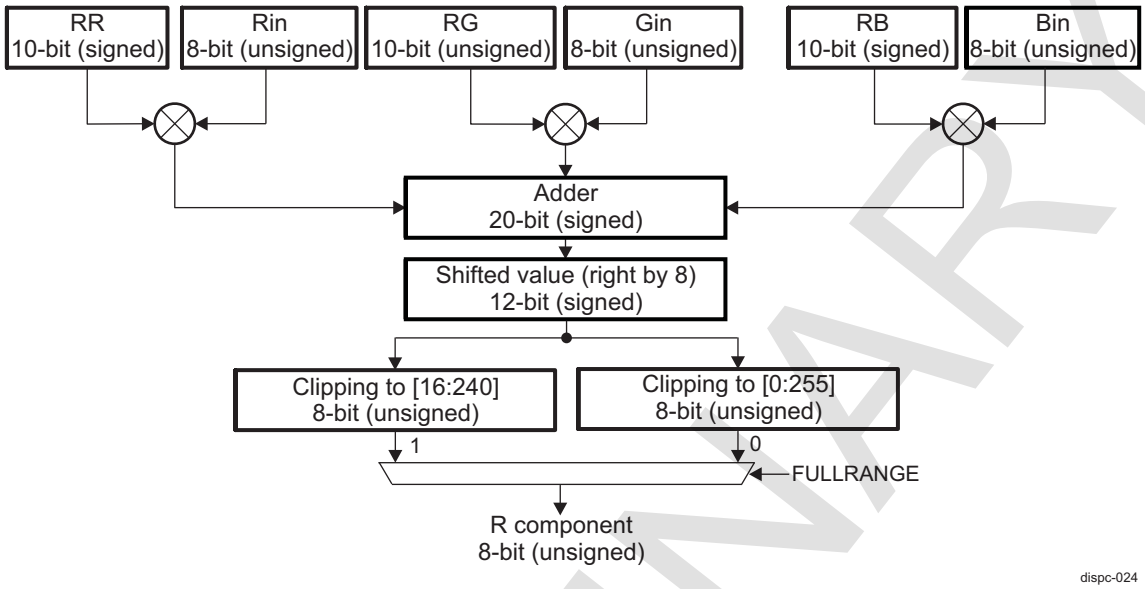
Figure 10-80 shows the color phase rotation macro-architecture.

Figure 10-80. Color Phase Rotation Macro-Architecture



10.2.4.12.4 Passive Matrix

The passive matrix display supports 16, 256, or 3375 colors to be displayed in each frame, depending on the color depth. The monochrome LCD has 15 grayscale levels available. To enable a passive matrix output, theDISPC_CONTROLo[3] STNTFT bit must be set to 0x0.

Spatial/temporal dithering is performed when using the passive matrix data path. The spatial/temporal dithering logic can be selected to enhance the quality of the passive matrix. When selected, the pixels are preprocessed by the spatial/temporal dithering logic before the passive matrix display dithering logic. The output format of the spatial/temporal dithering logic is RGB 12-bit (not configurable). The dithering logic is integrated after the color phase rotation. The dithering algorithm is based on the frame rate control. The dithering logic can process the pixels one frame, two frames, or four frames. The number of frames is selected by setting the DISPC_CONTROLo[31:30] SPATIALTEMPORALDITHERINGFRAMES bit field. The temporal dithering logic is enabled by setting the DISPC_CONTROLo [7] STDITHERENABLE bit to 0x1. The output format of the dithering logic is RGB 12-bit (not configurable).

After the pixels, from GFX, VID pipelines, are merged depending on the transparency status and overlay, the result is sent to a color/grayscale temporal dither generator. The monochrome data or each RGB color component are encoded on 4 bits, which are the 4 MSBs of 8-bit pixel-encoded component defined by the merge of the graphics data and the video data.

These 4-bit values are used to select on the 16 intensity levels. The gray/color intensity is controlled by turning individual pixels on and off at varying period rates, making the average time the pixel is off longer than the average time the pixel is on, thus producing more intense grays/colors. The dithering generator also uses the intensity of adjacent pixels in the calculation to give the screen image a smooth appearance. The proprietary dither algorithm is optimized to provide a range of intensity values that matches the visual perception of color/gray graduations.

Single-panel monochrome screens use four or eight data lines; single-panel color screens use eight data pins. The output width is configured by setting the DISPC_CONTROLo[4] M8B bit, and the monochrome or color mode is selected by the DISPC_CONTROLo[2] MONOCOLOR bit.

10.2.4.12.5 Active Matrix

Depending on the color depth, the active matrix output:

- 24 BPP supports 16,777,216 colors.
- 18 BPP supports 262,144 colors.

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- 16 BPP supports 65,536 colors.
- 12 BPP supports 4096 colors.

When in active matrix path configuration, after setting theDISPC_CONTROLo[3] STNTFT bit to 0x1, two submodules must be configured:

- Spatial/temporal dithering
- Multiple cycle output format (TDM)

10.2.4.12.5.1 Spatial/Temporal Dithering

When the active matrix path is used, the spatial/temporal dithering logic can be selected to enhance the quality of the active matrix outputs. The encoded pixel values are used by spatial/temporal dithering logic to display the data in a lower color depth on the LCD panel. The dithering logic is integrated after the CPR and before the TDM. The spatial/temporal dithering algorithm is based on the (x,y) pixel position and frame rate control. The dithering logic can process the pixels over one frame, two frames, or four frames. The number of frames is selected by setting the DISPC_CONTROLo[31:30] SPATIALTEMPORALDITHERINGFRAMES bit field. In the case of a single frame, only spatial processing is applied, and in multiple frames, spatial and temporal processing are applied to the pixels. The spatial/temporal dithering logic is enabled by setting the DISPC_CONTROLo[7] STDITHERENABLE bit to 0x1.

NOTE:

- If the interface data bus is smaller than the pixel format size and spatial/temporal dithering is not enabled, the MSBs of the pixel color components are output on the interface data bus.
- If the interface data bus is wider than the pixel format size, by programming the pixel components replication active/inactive, the MSB is replicated to the LSB of the interface data bus or the LSB is filled with 0s.

10.2.4.12.5.2 Multiple Cycle Output Format (TDM)

The pixels, after the active matrix display processing, are formatted on one or multiple cycles (from one to three cycles). The number of bits for each cycle is set in the DISPC_DATAo_CYCLE1 for the first cycle, DISPC_DATAo_CYCLE2 for the second cycle, and DISPC_DATAo_CYCLE3 for the third cycle. The interface data bus width can be 8, 9, 12, or 16 bits. The configuration of the data bus is done in the DIPSC_CONTROLo[9:8] TFTDATALINES bit field.

When the TDM is disabled, the DISPC outputs the pixels using the conventional formats: Passive matrix display/active matrix display monochrome/color.

NOTE: The passive matrix dithering logic is always bypassed in active matrix display.

Figure 10-81 through Figure 10-84 show various examples of TDM settings in the function of pixel data formats and the interface data bus width.

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Figure 10-81. 8-Bit Interface Settings

	24-BPP		
	1st cycle	2nd cycle	3rd cycle
Data[7]	R0[7]	G0[7]	B0[7]
Data[6]	R0[6]	G0[6]	B0[6]
Data[5]	R0[5]	G0[5]	B0[5]
Data[4]	R0[4]	G0[4]	B0[4]
Data[3]	R0[3]	G0[3]	B0[3]
Data[2]	R0[2]	G0[2]	B0[2]
Data[1]	R0[1]	G0[1]	B0[1]
Data[0]	R0[0]	G0[0]	B0[0]

DISPC_CONTROLo.TDMCYCLEFORMAT = 0x2
DISPC_DATAo_CYCLE1 = 0x00000008
DISPC_DATAo_CYCLE2 = 0x00000008
DISPC_DATAo_CYCLE3 = 0x00000008

	18-BPP		
	1st cycle	2nd cycle	3rd cycle
Data[7]	R0[5]	G0[3]	x
Data[6]	R0[4]	G0[2]	x
Data[5]	R0[3]	G0[1]	x
Data[4]	R0[2]	G0[0]	x
Data[3]	R0[1]	B0[5]	x
Data[2]	R0[0]	B0[4]	x
Data[1]	G0[5]	B0[3]	B0[1]
Data[0]	G0[4]	B0[2]	B0[0]

DISPC_CONTROLo.TDMCycleFormat = 0x2
DISPC_DATAo_CYCLE1 = 0x00000008
DISPC_DATAo_CYCLE2 = 0x00000008
DISPC_DATAo_CYCLE3 = 0x00000002

	16-BPP	
	1st cycle	2nd cycle
Data[7]	R0[4]	G0[2]
Data[6]	R0[3]	G0[1]
Data[5]	R0[2]	G0[0]
Data[4]	R0[1]	B0[4]
Data[3]	R0[0]	B0[3]
Data[2]	G0[5]	B0[2]
Data[1]	G0[4]	B0[1]
Data[0]	G0[3]	B0[0]

DISPC_CONTROLo.TDMCYCLEFORMAT = 0x1
DISPC_DATAo_CYCLE1 = 0x00000008
DISPC_DATAo_CYCLE2 = 0x00000008

	12-BPP	
	1st cycle	2nd cycle
Data[7]	R0[3]	x
Data[6]	R0[2]	x
Data[5]	R0[1]	x
Data[4]	R0[0]	x
Data[3]	G0[3]	B0[3]
Data[2]	G0[2]	B0[2]
Data[1]	G0[1]	B0[1]
Data[0]	G0[0]	B0[0]

DISPC_CONTROLo.TDMCYCLEFORMAT = 0x1
DISPC_DATAo_CYCLE1 = 0x00000008
DISPC_DATAo_CYCLE2 = 0x00000004

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Figure 10-82. 9-Bit Interface Settings

	24-BPP		
	1st cycle	2nd cycle	3rd cycle
Data[8]	R0[7]	G0[6]	x
Data[7]	R0[6]	G0[5]	x
Data[6]	R0[5]	G0[4]	x
Data[5]	R0[4]	G0[3]	B0[5]
Data[4]	R0[3]	G0[2]	B0[4]
Data[3]	R0[2]	G0[1]	B0[3]
Data[2]	R0[1]	G0[0]	B0[2]
Data[1]	R0[0]	B0[7]	B0[1]
Data[0]	G0[7]	B0[6]	B0[0]

DISPC_CONTROLo.TDMCycleFormat = 0x2
DISPC_DATAo_CYCLE1 = 0x00000009
DISPC_DATAo_CYCLE2 = 0x00000009
DISPC_DATAo_CYCLE3 = 0x00000006

	18-BPP	
	1st cycle	2nd cycle
Data[8]	R0[5]	G0[2]
Data[7]	R0[4]	G0[1]
Data[6]	R0[3]	G0[0]
Data[5]	R0[2]	B0[5]
Data[4]	R0[1]	B0[4]
Data[3]	R0[0]	B0[3]
Data[2]	G0[5]	B0[2]
Data[1]	G0[4]	B0[1]
Data[0]	G0[3]	B0[0]

DISPC_CONTROLo.TDMCYCLEFORMAT = 0x1
DISPC_DATAo_CYCLE1 = 0x00000009
DISPC_DATAo_CYCLE2 = 0x00000009

	16-BPP	
	1st cycle	2nd cycle
Data[8]	R0[4]	x
Data[7]	R0[3]	x
Data[6]	R0[2]	G0[1]
Data[5]	R0[1]	G0[0]
Data[4]	R0[0]	B0[4]
Data[3]	G0[5]	B0[3]
Data[2]	G0[4]	B0[2]
Data[1]	G0[3]	B0[1]
Data[0]	G0[2]	B0[0]

DISPC_CONTROLo.TDMCYCLEFORMAT = 0x1
DISPC_DATAo_CYCLE1 = 0x00000009
DISPC_DATAo_CYCLE2 = 0x00000007

	12-BPP	
	1st cycle	2nd cycle
Data[8]	R0[3]	x
Data[7]	R0[2]	x
Data[6]	R0[1]	x
Data[5]	R0[0]	x
Data[4]	G0[3]	x
Data[3]	G0[2]	x
Data[2]	G0[1]	B0[2]
Data[1]	G0[0]	B0[1]
Data[0]	B0[3]	B0[0]

DISPC_CONTROLo.TDMCYCLEFORMAT = 0x1
DISPC_DATAo_CYCLE1 = 0x00000009
DISPC_DATAo_CYCLE2 = 0x00000003

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Figure 10-83. 12-Bit Interface Settings

	24-BPP	
	1st cycle	2nd cycle
Data[11]	R0[7]	G0[3]
Data[10]	R0[6]	G0[2]
Data[9]	R0[5]	G0[1]
Data[8]	R0[4]	G0[0]
Data[7]	R0[3]	B0[7]
Data[6]	R0[2]	B0[6]
Data[5]	R0[1]	B0[5]
Data[4]	R0[0]	B0[4]
Data[3]	G0[7]	B0[3]
Data[2]	G0[6]	B0[2]
Data[1]	G0[5]	B0[1]
Data[0]	G0[4]	B0[0]

DISPC_CONTROLo.TDMCYCLEFORMAT = 0x1
DISPC_DATAo_CYCLE1 = 0x0000000C
DISPC_DATAo_CYCLE2 = 0x0000000C

	18-BPP		
	1st cycle	2nd cycle	3rd cycle
Data[11]	R0[5]	B0[5]	G1[5]
Data[10]	R0[4]	B0[4]	G1[4]
Data[9]	R0[3]	B0[3]	G1[3]
Data[8]	R0[2]	B0[2]	G1[2]
Data[7]	R0[1]	B0[1]	G1[1]
Data[6]	R0[0]	B0[0]	G1[0]
Data[5]	G0[5]	R1[5]	B1[5]
Data[4]	G0[4]	R1[4]	B1[4]
Data[3]	G0[3]	R1[3]	B1[3]
Data[2]	G0[2]	R1[2]	B1[2]
Data[1]	G0[1]	R1[1]	B1[1]
Data[0]	G0[0]	R1[0]	B1[0]

DISPC_CONTROLo.TDMCYCLEFORMAT = 0x3
DISPC_DATAo_CYCLE1 = 0x0000000C
DISPC_DATAo_CYCLE2 = 0x00060606
DISPC_DATAo_CYCLE3 = 0x000C0000

	16-BPP	
	1st cycle	2nd cycle
Data[11]	R0[4]	x
Data[10]	R0[3]	x
Data[9]	R0[2]	x
Data[8]	R0[1]	x
Data[7]	R0[0]	x
Data[6]	G0[5]	x
Data[5]	G0[4]	x
Data[4]	G0[3]	x
Data[3]	G0[2]	B0[3]
Data[2]	G0[1]	B0[2]
Data[1]	G0[0]	B0[1]
Data[0]	B0[4]	B0[0]

DISPC_CONTROLo.TDMCYCLEFORMAT = 0x1
DISPC_DATAo_CYCLE1 = 0x0000000C
DISPC_DATAo_CYCLE2 = 0x00000004

	12-BPP
	1st cycle
Data[11]	R0[3]
Data[10]	R0[2]
Data[9]	R0[1]
Data[8]	R0[0]
Data[7]	G0[3]
Data[6]	G0[2]
Data[5]	G0[1]
Data[4]	G0[0]
Data[3]	B0[3]
Data[2]	B0[2]
Data[1]	B0[1]
Data[0]	B0[0]

DISPC_CONTROLo.TDMCYCLEFORMAT = 0x0
DISPC_DATAo_CYCLE1 = 0x0000000C

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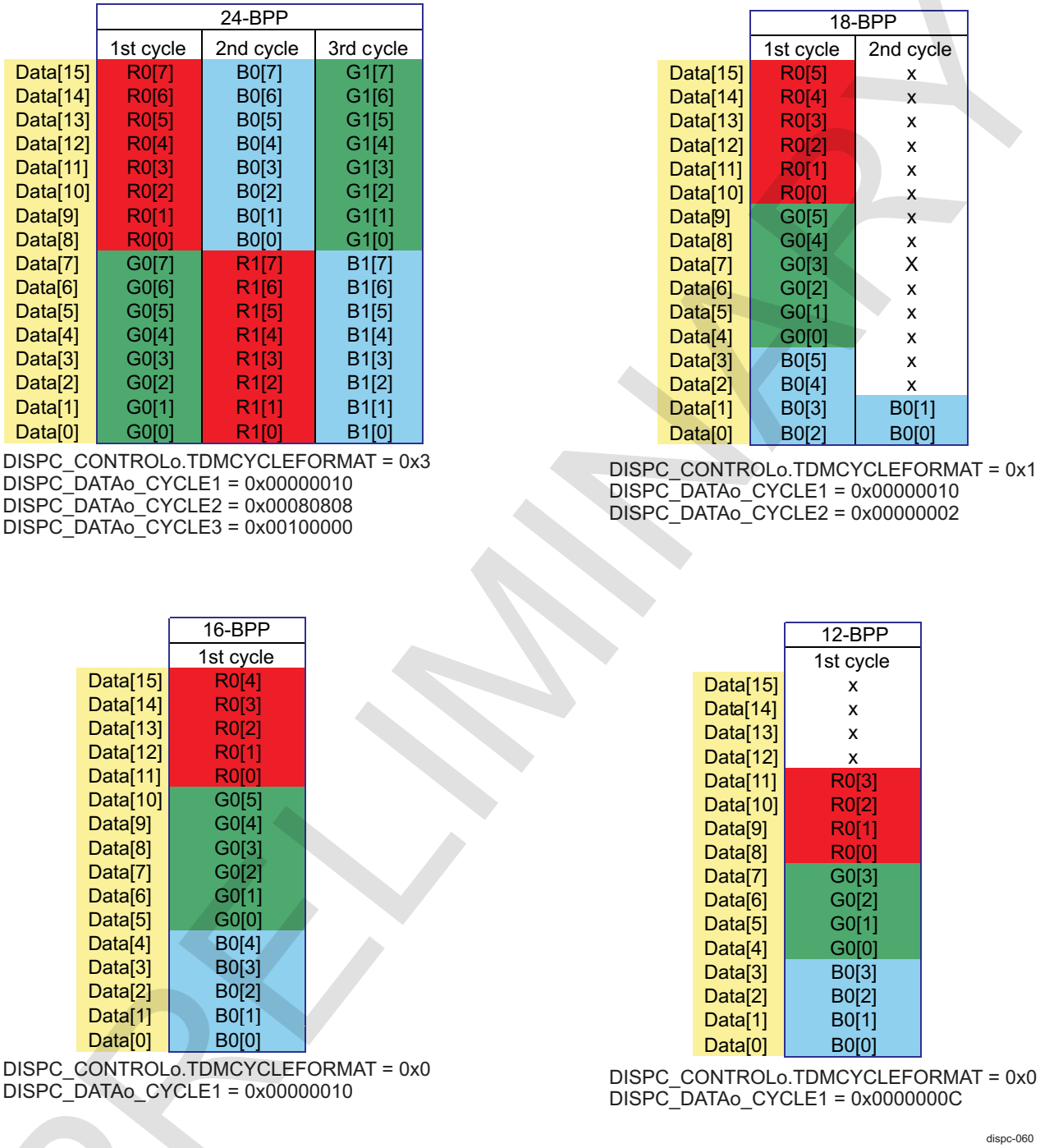
Figure 10-84. 16-Bit Interface Settings



10.2.4.12.6 Synchronized Buffer Update

A synchronization mismatch between the frame buffer and the display refreshes, named tearing effect, can lead to images that appear to be stretched on the screen. To avoid it, a synchronization mechanism is used between the DISPC and the process that updates the buffer. An interrupt is generated when the display reaches a predefined line number. The PROGRAMMEDLINENUMBER_IRQ interrupt (DISPC_IRQSTATUS and DISPC_IRQENABLE) is a level signal and stays active during the programmed line of the display.

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10.2.4.12.7 Timing Generator and Panel Settings

The size of and panel is defined by:

- Number of lines, DISPC_SIZE_LCDo[26:16] LPP bit field, with a value from 1 to 2048
- Number of pixels per line, DISPC_SIZE_LCDo[10:0]PPL bit field, with a value from 1 to 2048

Standard HSYNC/VSYNC timing generation are programmable for each LCD outputs independently:

- Horizontal front porch is set in the DISPC_TIMING_Ho[19:8] HFP bit field.
- Horizontal back porch is set in the DISPC_TIMING_Ho[31:20] HBP bit field.
- Horizontal synchronization pulse width is set in the DISPC_TIMING_Ho[7:0] HSW bit field.
- Vertical front porch is set in the DISPC_TIMING_Vo[19:8] VFP bit field.
- Vertical back porch is set in the DISPC_TIMING_Vo[31:20] VBP bit field.
- Vertical synchronization pulse width is set in the DISPC_TIMING_Vo[7:0] VSW bit field.

Horizontal/vertical synchronization and ACBIAS signals polarity are programmable by setting the DISPC_POL_FREQo[12] IVS, DISPC_POL_FREQo[13] IHS, and DISPC_POL_FREQo[15] IEO bits. These signals can be gated by setting the DISPC_CONFIGo[7] VSYNCGATED and DISPC_CONFIGo[6] HSYNCGATED bits.

The latch of data can be driven on the rising or falling edge of the pixel clock by setting the DISPC_POL_FREQo[14] IPC bit. The drive of the SYNC and VSYNC signals in the function of the pixel clock is done by setting the DISPC_POL_FREQo[16] RF bit.

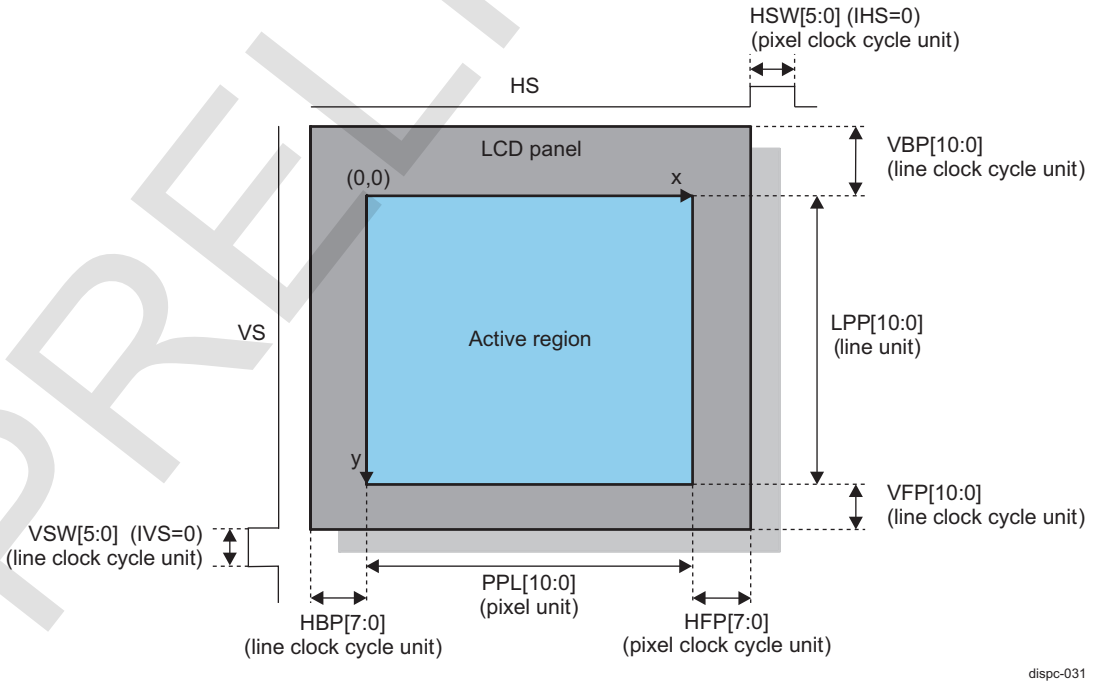
Table 10-54 describes the programming rules for LCD timing.

Table 10-54. Programming Rules

	No Downsampling	Downsampling H or V	Downsampling H + V
(HBP + HSW + HFP) * PCD	8	10	20

Figure 10-85 shows the timing values description in the case of an active matrix display.

Figure 10-85. Timing Values (Active Matrix Display)



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The 8-bit pixel clock divider (the DISPC_DIVISOR[7:0] PCD bit field) selects the pixel clock frequency. This bit field generates a range of pixel clock frequencies from LC/2 to LC/256, where LC is the logic clock from the divided functional clock of the DISPC by the DISPC_DIVISOR[23:16] LCD bit field.

The pixel clock is defined by the following equation:

Pixel Clock = (FunctionalClock/LCD[7:0])/PCD[7:0]

The pixel clock can be gated by setting the DISPC_CONFIGo[5] PIXELCLOCKGATED bit to 0x1.

The LCD output can be configured in progressive output or interlace output. The selection is done by writing into the DISPC_CONFIGo[22] OUTPUTMODEENABLE bit. The reset value is 0x0, which means progressive mode. When the progressive mode is selected, the FID signal associated to the LCD output is driven low (INACTIVE state). The selection can be changed only if the corresponding LCD output is disabled. The configuration is independent for each LCD output.

When in interlaced mode, the DISPC_CONFIGo[23] FIDFIRST bit indicates which field is output first:

- 0x0: Even field first (FID = 0)
- 0x1: Odd field first (FID = 1)

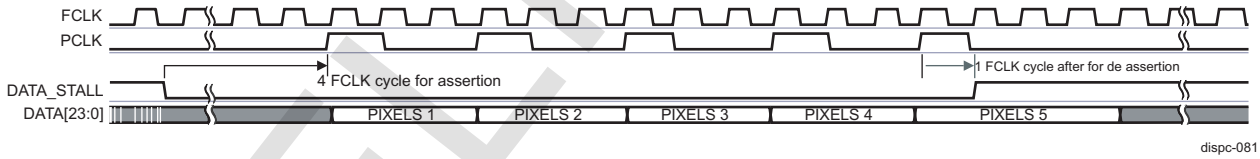
10.2.4.12.8 Stall Mode

Stall mode is used to indicate when the DISPC must stop sending data on the corresponding LCD output interface to avoid an overflow on the interface level. Stall mode is available when RFBI and DSI interface are used. The Interface asserts the stall signal to stop data output by the DISPC. It is deasserted by the interface to indicate when new data must be output by the DISPC .Figure 10-86 shows the RFBI data stall mode activated.

Stall mode is selected by setting the DISPC_CONTROLo[11] STALLMODE bit.

NOTE: The DISPC_CONTROLo[5] GOLCD bit must not be set, but the DISPC configuration (DMA engine, pipelines associated with the LCD output) must be set before enabling the LCD output by setting the DISPC_CONTROLo[1] LCDENABLE bit.

Figure 10-86. RFBI Data Stall Signal Diagram



To avoid an underflow of the DMA buffer, the DMA buffer handshake must be enabled by setting the DISPC_CONFIGo[16] BUFFERHANDCHECK bit. The fullness of the buffers associated to the pipelines used for the LCD output is checked before providing data to the pipeline when the STALL signal is inactive. It prevents emptying the DMA buffer when the RFBI or DSI module requests data and there is not enough data in the DMA buffer of the DISPC. This feature must be enabled only when stall mode is used (STALLMODE set to 0x1). When the DMA buffer handshake is activated, the pixel transfer to the RFBI or DSI module, outside a STALL period, can be stopped and restarted when there are enough data in the DMA buffer. The DMA buffer handshake ensures that the underflow does not occur for the pipelines associated with the LCD output when RFBI/DSI interfaces are used. The rate of the data transfer to the RFBI or DSI is, then, fully dependent on the state of the DMA buffer. Figure 10-87 shows the RFBI data stall with FIFO handcheck mode activated.

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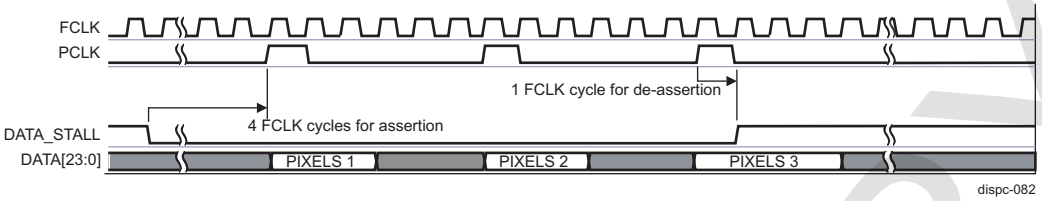
Figure 10-87. RFBI Data Stall Signal Diagram With Handcheck



Stall mode is independently used when the RFBI or DSI protocol engines are connected to the LCD outputs and receive the pixels to reformat the data.

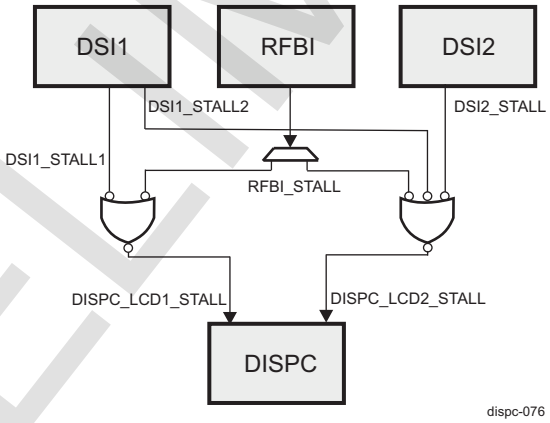
The STALL signals from the RFBI and DSI interfaces are merged into a single signal in the display subsystem. Only one signal for each LCD output is connected to the DISPC. Figure 10-88 shows the STALL signal implementation.

One STALL signal is generated by the RFBI. The RFBI module asserts the stall signal when no more data must be output by the DISPC. It is deasserted to indicate when new data must be output by the DISPC.

Two STALL signals are generated by the DSI1 protocol engine IP. It is used by the DSI1 protocol engine when data are provided from the DISPC to the DSI1 protocol engine using the two video ports in command mode only. If one of the two video ports is in video mode, the STALL signal associated with the video port from the DSI1 protocol engine is not used (must be in INACTIVE state from the DSI1 protocol engine IP).

One STALL signal is generated by the DSI2 P\protocol engine IP. It is used by the DSI2 protocol engine when data are provided from the DISPC to the DSI2 protocol engine using the single video port in command mode only. If the video port is in video mode, the STALL signal associated with the video port from the DSI2 protocol engine is not used (must be in INACTIVE state from the DSI2 protocol engine IP).

Figure 10-88. STALL Signal



10.2.4.13 TV Output

The TV output paths consist of several processing blocks (see Figure 10-89):

- Overlay manager
- Gamma correction unit
- Synchronization buffer

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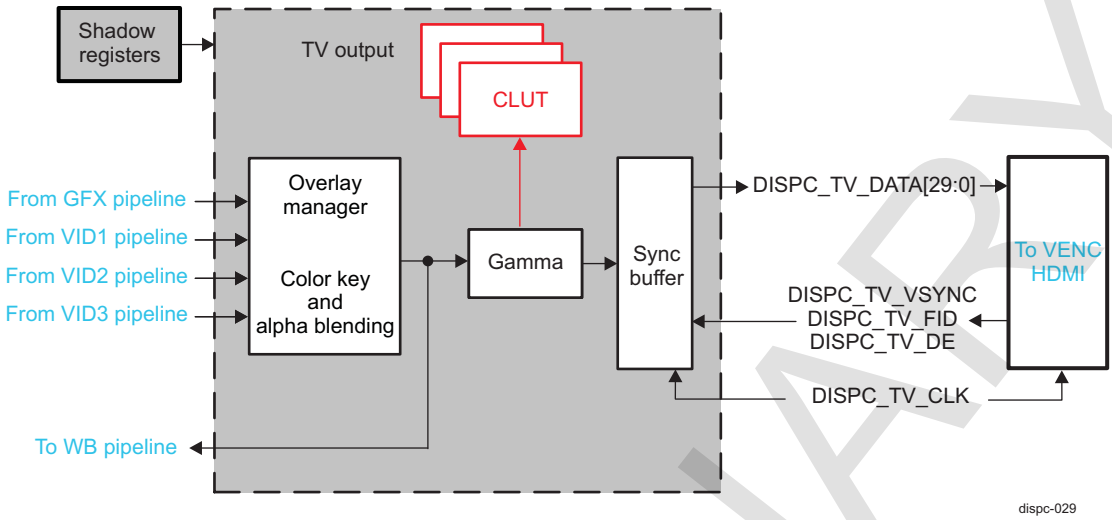
Figure 10-89. TV Output Architecture



The TV output is connected to the VENC or HDMI. In analog output or HDMI, the DISPC TV output receives an external clock, DISPC_TV_CLK, and based on the VSYNC generated by the VENC or HDMI, hold time, vertical offset, and horizontal offset, outputs the pixels synchronously. The size of the field/frame to output defines the number of pixels to output on each line and the number of lines for each field/frame.

NOTE: The VDAC function is not supported.

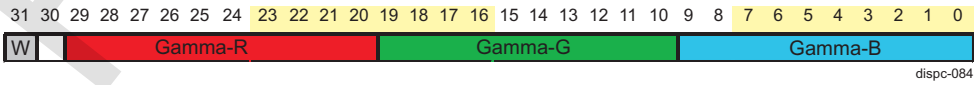
10.2.4.13.1 Overlay Manager

The overlay mechanism is identical in LCD1 and LCD2 (see Section 10.2.4.12.1, *Overlay Manager*).

10.2.4.13.2 Gamma Correction Unit

The gamma correction unit works as described in Section 10.2.4.12.2, *Gamma Correction Unit*. The only difference resides in the input pixel format RGB30. Each component of encoded pixel value is used as a pointer to index one out of 1024 30-bit gamma curve entries in the table. Each 10-bit component is replaced with the 10-bit table value corresponding to R, G, or B component. The table is loaded by software, through the DISPC_GAMMA_TABLE2 register. It is possible to load only part of the table. For each write access to the table, the 30-bit gamma value is associated with bit[31] INDEX to indicate that a new table is defined. Setting bit[31] INDEX to 0x1 for the first time, resets the internal index counter. All the following accesses are considered to be for incremented index addressing in the table (bit [31] INDEX set to 0 for each subsequent access). Figure 10-90 shows the format of one of the gamma curve values in the memory.

Figure 10-90. Data Memory Organization for Gamma Mode in TV Output



10.2.4.13.3 Synchronized Buffer Update

The synchronized buffer update is identical in LCD1 and LCD2 (see Section 10.2.4.12.6, *Synchronized Buffer Update*).

10.2.4.13.4 Timing and TV Format Settings

Figure 10-91 shows the TV formats supported.

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Figure 10-91. TV Formats

The size of a TV output format is defined by:

- Number of lines, DISPC_SIZE_TV[26:16] LPP bit field, with a value from 1 to 2048
- Number of pixels per line, DISPC_SIZE_TV[10:0] PPL bit field, with a value from 1 to 2048
- Delta size between odd/even field, DISPC_SIZE_TV[15:14] DELTA_LPP bit field. This bit field controls only the output channel and not the size of the data field fetched from the frame buffer in memory.

The hold time of the pixels on the data bus is determined in clock cycles by the DISPC_CONTROL1[19:17] HT bit field. The default value at reset time is 0x0 (one cycle).

- When connected to the video NTSC/PAL encoder in field mode, Table 10-56 indicates the DISPC_SIZE_TV (PPL and LPP) value for each standard PAL and NTSC.

Table 10-55. PPL and LLP Value for TV Standard

Standards		Active Pixels/Line	Active Lines	Digital Clock	DISPC_SIZE_TV
ITU-R BT.601	NTSC(J, M, 4.43)	720	480	13.5 MHz	0x00EF02CF
	PAL(B, D, G, H, I, N)	720	576	13.5 MHz	0x011F02CF
	PAL(M)	720	480	13.5 MHz	0x00EF02CF
Square Pixel	NTSC(J, M, 4.43)	640	480	12.2727 MHz	0x00EF027F
	PAL(B, D, G, H, I, N)	768	576	14.75 MHz	0x011F02FF
	PAL(M)	640	480	12.2727 MHz	0x00EF027F

NOTE: The VDAC function is not supported.

- When connected to the HDMI encoder, Table 10-56 indicates the DISPC_SIZE_TV (PPL and LPP) value for each HD standard.

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Table 10-56. PPL and LLP Value for HD Standard

Standards		Active Pixels/Line	Active Lines	Digital Clock	DISPC_SIZE_TV
HD standard	720p	1280	720	74.25/74.125 MHz (60/59.99..frames/s)	0x02CF04FF
	1080i	1920	540	74.25/74.125 MHz (60/59.99..frames/s)	0x021B07FF
	1080p	1920	1080	148.5/148.25 MHz (60/59.99..frames/s)	0x043707FF

- When connected to the HDMI encoder, to output any of the 3D frame-packing formats (720p@50 Hz, 720p@ 60 Hz, and 1080p @24 Hz, as defined in the HDMI v1.4 specification) supported by the device, Table 10-57 lists the DISPC_SIZE_TV (PPL and LPP) value for each 3D standard.

Table 10-57. PPL and LLP Value for 3D Standard

Standards		Active Pixels/Line	Active Lines	Digital Clock	DISPC_SIZE_TV
3D standard	720p	1280	1470	148.5 MHz (50; 60 frames/s)	5BD04FF
	1080p	1920	2205[(1)]	148.5 MHz (24 frames/s)	9C0780

(1) See the following Note for information about configuring the 3D 1080p format.

NOTE: When configuring the DISPC for outputting any supported 3D frame-packing format, the following generic details must be considered:

- As defined by the HDMI v1.4 specification, Section 8.2.3.2, 3D frame-packing is a video format structure composed of two stereoscopic pictures: left and right.
- The stereoscopic pictures can be processed through the three video pipelines (VID1, VID2, or VID3). For more information about the configuration of video pipelines, see Section 10.2.4.10, *Video Pipelines*.
- The 3D frame is generated by setting the TV overlay manager to combine the outputs of the selected video pipelines that hold the pictures. One video pipeline (VID1 or VID3) must carry the top field of the 3D frame (left stereoscopic picture), and the VID2 pipeline must always carry the bottom field of the frame (right stereoscopic picture). The top and bottom fields are separated by an active space area. For more information, see the HDMI v1.4 specification, Section 8.2.3.2.
- The pipeline carrying each field (top and bottom) of the 3D frame must have its height and width parameters defined in the [26:16] SIZEYand [10:0] SIZEX bit fields of DISPC_VIDp_SIZE register, and its Y and X positions defined in the [26:16] POSYand [10:0] POSX bit fields of the DISPC_VIDp_POSITION register. The active space area of the 3D frame can be encoded by setting the solid background color for the TV output (DISPC_DEFAULT_COLOR1[23:0] DEFAULTCOLOR bit field). For more information about the overlay mechanism, see Section 10.2.4.13.1, *Overlay Manager*.
- If the 3D 1080p format must be output, the following specific settings must be applied:
  - DISPC_VID2_ATTRIBUTES[31:30] CHANNELOUT2 bit-field = 0x2
  - DISPC_SIZE_TV[26:16] LPP bit-field = 0x9C

10.2.4.14 Shadow Registers

Some DISPC registers are termed *shadow registers*. A shadow register change has no direct effect on the configuration of the DISPC. The registers are shadow registers to allow software to change the values of the registers at any time. When all the registers for a given configuration are into the registers, software must set 1 bit only in order to validate the configuration. When the hardware reaches the end of the current frame and sees that the bit field has been set by software, the new configuration is now the configuration used by the hardware.

The bits enabling the hardware to use the new configuration are:

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- DISPC_CONTROL1[5] GOLCD bit for all the registers associated to the LCD1 output, and for all registers of WB and DMA, if the LCD1 channel is captured. The update of the registers of the WB and DMA is further delayed by the DISPC_WB_ATTRIBUTES2[7:0] WBDELAYCOUNT bit field or done when the next frame is captured (the DISPC_WB_ATTRIBUTES[26:24] CAPTUREMODE bit field must be different from 0). The update of the registers occurs at the VFP start period.
- DISPC_CONTROL1[6] GOTV bit for all the registers associated to the TV output, and for all registers of WB and DMA, if the TV channel is captured. The update of the registers of the WB and DMA is further delayed by the DISPC_WB_ATTRIBUTES2[7:0] WBDELAYCOUNT bit field or done when the next frame is captured (the DISPC_WB_ATTRIBUTES[26:24] CAPTUREMODE bit field must be different from 0). The update of the registers occurs at the external EVSYNC.
- DISPC_CONTROL2[5] GOLCD bit for all the registers associated to the LCD2 output, and for all registers of WB and DMA, if the LCD2 channel is captured. The update of the registers of the WB and DMA is further delayed by the DISPC_WB_ATTRIBUTES2[7:0] WBDELAYCOUNT bit field or done when the next frame is captured (the DISPC_WB_ATTRIBUTES[26:24] CAPTUREMODE bit field must be different from 0). The update of the registers occurs at the VFP start period.
- DISPC_WB_ATTRIBUTES[0] ENABLE bit for all the registers associated to the WB, if the transfer memory-to-memory is not associated with a channel out.
- The DISPC_CONTROL2[6] GOWB bit and the [5]GOLCD and [6]GOTV bits in the DISPC_CONTROL1/DISPC_CONTROL2 registers, combined with the synchronization event of the channel output selected for write back. This applies to all registers associated with the selected channel out and further delayed by the setting in the DISPC_WB_ATTRIBUTES2[7:0] WBDELAYCOUNT bit field for all registers of the write back and DMA. The GOWB bit is required to be set only in WB capture mode; it is not required when WB memory-to-memory mode is used.

NOTE: Before setting the GOLCD, GOTV, or GOWB bits, the user must ensure that the bits are cleared. The hardware resets the bit when the update completes.

Table 10-58 lists the shadow registers.

Table 10-58. Shadow Registers

Shadow Register Name	Updated on VFP Start Period (LCD1 Pipeline)	Updated on VFP Start Period (LCD2 Pipeline)	Updated on External VSYNC (TV Pipeline)	Updated on ENF of Frame (WB Pipeline)
DISPC_REVISION				
DISPC_SYSCONFIG				
DISPC_SYSSTATUS				
DISPC_IRQSTATUS				
DISPC_IRQENABLE				
DISPC_CONTROL1	x		x	
DISPC_CONFIG1	x	x	x	x
DISPC_DEFAULT_COLOR0	x			
DISPC_DEFAULT_COLOR1		x		
DISPC_TRANS_COLOR0	x			
DISPC_TRANS_COLOR1		x		
DISPC_LINE_STATUS				
DISPC_LINE_NUMBER	x			
DISPC_TIMING_H1	x			
DISPC_TIMING_V1	x			
DISPC_POL_FREQ1	x			
DISPC_DIVISOR1	x			

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Table 10-58. Shadow Registers (continued)

Shadow Register Name	Updated on VFP Start Period (LCD1 Pipeline)	Updated on VFP Start Period (LCD2 Pipeline)	Updated on External VSYNC (TV Pipeline)	Updated on ENF of Frame (WB Pipeline)
DISPC_GLOBAL_ALPHA	x	x	x	x
DISPC_SIZE_TV			x	
DISPC_SIZE_LCD1	x			
DISPC_GFX_BA_j [1]	x	x	x	x
DISPC_GFX_POSITION	x	x	x	x
DISPC_GFX_SIZE	x	x	x	x
DISPC_GFX_ATTRIBUTES	x	x	x	x
DISPC_GFX_BUF_THRESHOLD	x	x	x	x
DISPC_GFX_BUF_SIZE_STATUS	x	x	x	x
DISPC_GFX_ROW_INC	x	x	x	x
DISPC_GFX_PIXEL_INC	x	x	x	x
DISPC_GFX_WINDOW_SKIP	x	x	x	x
DISPC_GFX_TABLE_BA	x	x	x	x
DISPC_VID1_BA_j [2]	x	x	x	x
DISPC_VID1_POSITION	x	x	x	x
DISPC_VID1_SIZE	x	x	x	x
DISPC_VID1_ATTRIBUTES	x	x	x	x
DISPC_VID1_BUF_THRESHOLD	x	x	x	x
DISPC_VID1_BUF_SIZE_STATUS	x	x	x	x
DISPC_VID1_ROW_INC	x	x	x	x
DISPC_VID1_PIXEL_INC	x	x	x	x
DISPC_VID1_FIR	x	x	x	x
DISPC_VID1_PICTURE_SIZE	x	x	x	x
DISPC_VID1_ACCU_j [2]	x	x	x	x
DISPC_VID1_FIR_COEF_H_i [3]	x	x	x	x
DISPC_VID1_FIR_COEF_HV_i [3]	x	x	x	x
DISPC_VID1_CONV_COEF0	x	x	x	x
DISPC_VID1_CONV_COEF1	x	x	x	x
DISPC_VID1_CONV_COEF2	x	x	x	x

(1) j = 0 to 1
(2) j = 0 to 1
(3) i = 0 to 7

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Table 10-58. Shadow Registers (continued)

Shadow Register Name	Updated on VFP Start Period (LCD1 Pipeline)	Updated on VFP Start Period (LCD2 Pipeline)	Updated on External VSYNC (TV Pipeline)	Updated on ENF of Frame (WB Pipeline)
DISPC_VID1_CONV_COEF3	x	x	x	x
DISPC_VID1_CONV_COEF4	x	x	x	x
DISPC_VID2_BA_j [2]	x	x	x	x
DISPC_VID2_POSITION	x	x	x	x
DISPC_VID2_SIZE	x	x	x	x
DISPC_VID2_ATTRIBUTES	x	x	x	x
DISPC_VID2_BUF_THRESHOLD	x	x	x	x
DISPC_VID2_BUF_SIZE_STATUS	x	x	x	x
DISPC_VID2_ROW_INC	x	x	x	x
DISPC_VID2_PIXEL_INC	x	x	x	x
DISPC_VID2_FIR	x	x	x	x
DISPC_VID2_PICTURE_SIZE	x	x	x	x
DISPC_VID2_ACCU_j [4]	x	x	x	x
DISPC_VID2_FIR_COEF_H_i [5]	x	x	x	x
DISPC_VID2_FIR_COEF_HV_i [5]	x	x	x	x
DISPC_VID2_CONV_COEF0	x	x	x	x
DISPC_VID2_CONV_COEF1	x	x	x	x
DISPC_VID2_CONV_COEF2	x	x	x	x
DISPC_VID2_CONV_COEF3	x	x	x	x
DISPC_VID2_CONV_COEF4	x	x	x	x
DISPC_DATA1_CYCLE1	x	x	x	
DISPC_DATA1_CYCLE2	x	x	x	
DISPC_DATA1_CYCLE3	x	x	x	
DISPC_VID1_FIR_COEF_V_i [5]	x	x	x	x
DISPC_VID2_FIR_COEF_V_i [5]	x	x	x	x
DISPC_CPR1_COEF_R	x			
DISPC_CPR1_COEF_G	x			
DISPC_CPR1_COEF_B	x			
DISPC_GFX_PRELOAD	x	x	x	x

[4] j = 0 to 1
[5] i = 0 to 7

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Table 10-58. Shadow Registers (continued)

Shadow Register Name	Updated on VFP Start Period (LCD1 Pipeline)	Updated on VFP Start Period (LCD2 Pipeline)	Updated on External VSYNC (TV Pipeline)	Updated on ENF of Frame (WB Pipeline)
DISPC_VID1_PRELOAD	x	x	x	x
DISPC_VID2_PRELOAD	x	x	x	x
DISPC_CONTROL2	x	x		
DISPC_VID3_ACCU_j (5)	x	x	x	x
DISPC_VID3_BA_j (5)	x	x	x	x
DISPC_VID3_FIR_COEF_H_i (5)	x	x	x	x
DISPC_VID3_FIR_COEF_HV_i (5)	x	x	x	x
DISPC_VID3_FIR_COEF_V_i (5)	x	x	x	x
DISPC_VID3_ATTRIBUTES	x	x	x	x
DISPC_VID3_CONV_COEF0	x	x	x	x
DISPC_VID3_CONV_COEF1	x	x	x	x
DISPC_VID3_CONV_COEF2	x	x	x	x
DISPC_VID3_CONV_COEF3	x	x	x	x
DISPC_VID3_CONV_COEF4	x	x	x	x
DISPC_VID3_BUF_SIZE_STATUS	x	x	x	x
DISPC_VID3_BUF_THRESHOLD	x	x	x	x
DISPC_VID3_FIR	x	x	x	x
DISPC_VID3_PICTURE_SIZE	x	x	x	x
DISPC_VID3_PIXEL_INC	x	x	x	x
DISPC_VID3_POSITION	x	x	x	x
DISPC_VID3_PRELOAD	x	x	x	x
DISPC_VID3_ROW_INC	x	x	x	x
DISPC_VID3_SIZE	x	x	x	x
DISPC_DEFAULT_COLOR2		x		
DISPC_TRANS_COLOR2		x		
DISPC_CPR2_COEF_B		x		
DISPC_CPR2_COEF_G		x		
DISPC_CPR2_COEF_R		x		
DISPC_DATA2_CYCLE1		x		
DISPC_DATA2_CYCLE2		x		

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Table 10-58. Shadow Registers (continued)

Shadow Register Name	Updated on VFP Start Period (LCD1 Pipeline)	Updated on VFP Start Period (LCD2 Pipeline)	Updated on External VSYNC (TV Pipeline)	Updated on ENF of Frame (WB Pipeline)
DISPC_DATA2_CYCLE3		x		
DISPC_SIZE_LCD2		x		
DISPC_TIMING_H2		x		
DISPC_TIMING_V2		x		
DISPC_POL_FREQ2		x		
DISPC_DIVISOR2		x		
DISPC_WB_ACCU_j [6]	x	x	x	x
DISPC_WB_BA_j [6]	x	x	x	x
DISPC_WB_FIR_COEF_H_i [7]	x	x	x	x
DISPC_WB_FIR_COEF_HV_i [7]	x	x	x	x
DISPC_WB_FIR_COEF_V_i [7]	x	x	x	x
DISPC_WB_ATTRIBUTES	x	x	x	x
DISPC_WB_CONV_COEF0	x	x	x	x
DISPC_WB_CONV_COEF1	x	x	x	x
DISPC_WB_CONV_COEF2	x	x	x	x
DISPC_WB_CONV_COEF3	x	x	x	x
DISPC_WB_CONV_COEF4	x	x	x	x
DISPC_WB_BUF_SIZE_STATUS	x	x	x	x
DISPC_WB_BUF_THRESHOLD	x	x	x	x
DISPC_WB_FIR	x	x	x	x
DISPC_WB_PICTURE_SIZE	x	x	x	x
DISPC_WB_PIXEL_INC	x	x	x	x
DISPC_WB_ROW_INC	x	x	x	x
DISPC_WB_SIZE	x	x	x	x
DISPC_VID1_BA_UV_j [8]	x	x	x	x
DISPC_VID2_BA_UV_j [8]	x	x	x	x
DISPC_VID3_BA_UV_j [8]	x	x	x	x
DISPC_WB_BA_UV_j [8]	x	x	x	x
DISPC_CONFIG2		x		
DISPC_VID1_ATTRIBUTES2	x	x	x	x
DISPC_VID2_ATTRIBUTES2	x	x	x	x

[6] j = 0 to 1
[7] i = 0 to 7
[8] j = 0 to 1

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Table 10-58. Shadow Registers (continued)

Shadow Register Name	Updated on VFP Start Period (LCD1 Pipeline)	Updated on VFP Start Period (LCD2 Pipeline)	Updated on External VSYNC (TV Pipeline)	Updated on ENF of Frame (WB Pipeline)
DISPC_VID3_ATTRIBUTES2	x	x	x	x
DISPC_GAMMA_TABLE0	x	x	x	x
DISPC_GAMMA_TABLE1	x	x	x	x
DISPC_GAMMA_TABLE2	x	x	x	x
DISPC_VID1_FIR2	x	x	x	x
DISPC_VID1_ACCU2_j (8)	x	x	x	x
DISPC_VID1_FIR_COEF_H2_i (9)	x	x	x	x
DISPC_VID1_FIR_COEF_HV2_i (9)	x	x	x	x
DISPC_VID1_FIR_COEF_V2_i (9)	x	x	x	x
DISPC_VID2_FIR2	x	x	x	x
DISPC_VID2_ACCU2_j (8)	x	x	x	x
DISPC_VID2_FIR_COEF_H2_i (10)	x	x	x	x
DISPC_VID2_FIR_COEF_HV2_i (10)	x	x	x	x
DISPC_VID2_FIR_COEF_V2_i (10)	x	x	x	x
DISPC_VID3_FIR2	x	x	x	x
DISPC_VID3_ACCU2_j (11)	x	x	x	x
DISPC_VID3_FIR_COEF_H2_i (10)	x	x	x	x
DISPC_VID3_FIR_COEF_HV2_i (10)	x	x	x	x
DISPC_VID3_FIR_COEF_V2_i (10)	x	x	x	x
DISPC_WB_FIR2	x	x	x	x
DISPC_WB_ACCU2_j (11)	x	x	x	x
DISPC_WB_FIR_COEF_H2_i (10)	x	x	x	x
DISPC_WB_FIR_COEF_HV2_i (10)	x	x	x	x
DISPC_WB_FIR_COEF_V2_i (10)	x	x	x	x
DISPC_GLOBAL_BUFFER	x	x	x	x
DISPC_DIVISOR	x	x	x	x

(9) i = 0 to 7
(10) i = 0 to 7
(11) j = 0 to 1

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10.2.5 Display Controller Programming Guide

10.2.5.1 Display Controller Low-Level Programming Models

This section covers the low-level hardware programming sequences for the configuration and use of the module.

10.2.5.1.1 Global Initialization

10.2.5.1.1.1 Surrounding Modules Global Initialization

This section identifies the requirements of initializing the surrounding modules when the DISPC module is to be used for the first time after a device reset. This initialization of surrounding modules is based on the integration and environment of the DISPC. See the DISPC Module Integration and Environment Sections for more information.

Table 10-59. Global Initialization of Surrounding Modules

Surrounding Modules	Comments
PRCM	Module interface and functional clocks must be enabled. See Chapter 3, *Power, Reset, and Clock Management*.
Control Module	Module-specific pad muxing and configuration must be set in the control module. See Chapter 18, *Control Module*.
MPU INTC or DSP INTC	MPU and/or DSP interrupt controller configuration must be done to enable the interrupts from DISPC module. See Chapter 17, *Interrupt Controller*.
Interconnect	See Chapter 13, *Interconnect*, for more information about the interconnect configuration.

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10.2.5.1.2 Operational Modes Configuration

Table 10-60. DISPC Configuration

Step	Register / Bit Field / Programming Model
For a GFX pipeline configuration	
Configure the GFX DMA channel	Refer to Table 10-61
Configure the GFX pipeline	Refer to Table 10-64
Configure the LCD or TV output	For LCD output, refer to Table 10-82
	For TV output, refer to Table 10-88
For a Video pipeline configuration	
Configure the video DMA channel	Refer to Table 10-62
Configure the video pipeline	Refer to Table 10-69
Configure the LCD or TV output	For LCD output, refer to Table 10-82
	For TV output, refer to Table 10-88
For a WB pipeline configuration	
Configure the WB DMA channel	Refer to Table 10-63
Configure the WB pipeline	For video pipelines, refer to Table 10-77

10.2.5.1.2.1 DMA Configuration

10.2.5.1.2.1.1 Main Sequence - DISPC DMA Channel Configuration

This subsequence describes the parameters of the GFX, video, or WB DMA channel parameters.

Table 10-61. Configure the GFX DMA Channel

Step	Register / Bit Field / Programming Model	Value
Set the base address for RGB pixel format or BITMAP component format according to memory access type, rotation, mirroring (refer to section DMA)	DISPC_GFX_BA_j[31:0] BA	0x—
Set the rotation flag	DISPC_GFX_ATTRIBUTES[13:12] ROTATION	0x–
Set the number of bytes to increment at the end of the row	DISPC_GFX_ROW_INC[31:0] ROWINC	0x–
Set the number of bytes to increment between two pixels	DISPC_GFX_PIXEL_INC[7:0] PIXELINC	0x–
Determine the FIFO preload mode	DISPC_GFX_ATTRIBUTES[11] BUFPRELOAD	0x–
Set the preload value	DISPC_GFX_PRELOAD[11:0] PRELOAD	0x–
Determine the burst type	DISPC_GFX_ATTRIBUTES[29] BURSTTYPE	0x–
Set the burst size	DISPC_GFX_ATTRIBUTES[7:6] BURSTSIZE	0x–
Set the high level of DMA FIFO threshold	DISPC_GFX_BUF_THRESHOLD[31:16] BUFHIGHTRESHOLD	0x–
Set the low level of DMA FIFO threshold	DISPC_GFX_BUF_THRESHOLD[15:0] BUFLOWTRESHOLD	0x–
Enable Selfrefresh	DISPC_GFX_ATTRIBUTES[24] SELFREFRESH	0x–
Select priority over the other pipeline	DISPC_GFX_ATTRIBUTES[23] ARBITRATION	0x–

Table 10-62. Configure the Video DMA Channel

Step	Register / Bit Field / Programming Model	Value
Set the base address for RGB pixel format or Y component format according to memory access type, rotation, mirroring (refer to section DMA)	DISPC_VIDp_BA_j[31:0] BA	0x—

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Table 10-62. Configure the Video DMA Channel (continued)

Step	Register / Bit Field / Programming Model	Value
Set the base address for Cb and Cr components according to memory access type, rotation, mirroring (refer to section DMA)[1]	DISPC_VIDp_BA_UV_j[31:0] BA	0x—
Set the rotation flag	DISPC_VIDp_ATTRIBUTES[13:12] ROTATION	0x–
Set the number of bytes to increment at the end of the row	DISPC_VIDp_ROW_INC[31:0] ROWINC	0x–
Set the number of bytes to increment between two pixels	DISPC_VIDp_PIXEL_INC[7:0] PIXELINC	0x–
Set the X original image size	DISPC_VIDp_PICTURE_SIZE[10:0] ORGSIZEX	0x–
Set the Y original image size	DISPC_VIDp_PICTURE_SIZE[26:16] ORGSIZEY	0x–
Determine the FIFO preload mode	DISPC_VIDp_ATTRIBUTES[19] BUFPRELOAD	0x–
Set the preload value	DISPC_VIDp_PRELOAD[11:0] PRELOAD	0x–
Determine the burst type	DISPC_VIDp_ATTRIBUTES[29] BURSTTYPE	0x–
Set the burst size	DISPC_VIDp_ATTRIBUTES[15:14] BURSTSIZE	0x–
Set the high level of DMA FIFO threshold	DISPC_VIDp_BUF_THRESHOLD[31:16] BUFHIGHTRESHOLD	0x–
Set the low level of DMA FIFO threshold	DISPC_VIDp_BUF_THRESHOLD[15:0] BUFLOWTRESHOLD	0x–
Enable Selfrefresh	DISPC_VIDp_ATTRIBUTES[24] SELFREFRESH	0x–
Select priority over the other pipeline	DISPC_VIDp_ATTRIBUTES[23] ARBITRATION	0x–

(1) Applicable only for YUV pixel format

Table 10-63. Configure the WB DMA Channel

Step	Register / Bit Field / Programming Model	Value
Set the base address for RGB pixel format or Y component format according to memory access type, rotation, mirroring (refer to section DMA)	DISPC_WB_BA_j[31:0] BA	0x—
Set the base address for Cb and Cr components according to memory access type, rotation, mirroring (refer to section DMA) [1]	DISPC_WB_BA_UV_j[31:0] BA	0x—
Set the stride of CbCr component [2]	DISPC_WB_ATTRIBUTES[22] DOUBLESTRIDE	0x–
Set the rotation flag	DISPC_WB_ATTRIBUTES[13:12] ROTATION	0x–
Set the number of bytes to increment at the end of the row	DISPC_WB_ROW_INC[31:0] ROWINC	0x–
Set the number of bytes to increment between two pixels	DISPC_WB_PIXEL_INC[7:0] PIXELINC	0x–
Set the X final image size in system memory	DISPC_WB_PICTURE_SIZE[10:0] ORGSIZEX	0x–
Set the Y final image size in system memory	DISPC_WB_PICTURE_SIZE[26:16] ORGSIZEY	0x–
Set the burst size	DISPC_WB_ATTRIBUTES[15:14] BURSTSIZE	0x–
Set the high level of DMA FIFO threshold	DISPC_WB_BUF_THRESHOLD[31:16] BUFHIGHTRESHOLD	0x–
Set the low level of DMA FIFO threshold	DISPC_WB_BUF_THRESHOLD[15:0] BUFLOWTRESHOLD	0x–
Select priority over the other pipeline	DISPC_WB_ATTRIBUTES[23] ARBITRATION	0x–

(1) Applicable only for YUV pixel format
(2) Applicable only for YUV pixel format

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10.2.5.1.2.2 GFX Pipeline Configuration

10.2.5.1.2.2.1 Main Sequence - Configure the GFX Pipeline

This procedure details the steps for a GFX pipeline configuration described in Table 10-64

Table 10-64. Configure the GFX Pipeline

Step	Register / Bit Field / Programming Model	Value
Configure the GFX Window	Refer to Table 10-65	
Configure the GFX pipeline processing	Refer to Table 10-66	
Configure the GFX pipeline layer output	Refer to Table 10-68	
Validate the GFX configuration according to outputs associated to the pipeline	DISPC_CONTROL1[5] GOLCD	
	DISPC_CONTROL2[5] GOLCD	
	DISPC_CONTROL2[6] GOWB	
	DISPC_CONTROL1[6] GOTV	
Enable the GFX pipeline	DISPC_GFX_ATTRIBUTES[0] ENABLE	0x1

10.2.5.1.2.2.2 Subsequence - Configure the GFX Window

This subsequence describes the parameters of the image to be displayed on the LCD panel.

Table 10-65. Configure the GFX Window

Step	Register / Bit Field / Programming Model	Value
Select the format of image	DISPC_GFX_ATTRIBUTES[4:1] FORMAT	0x–
Set the X size of image to be displayed onto LCD panel	DISPC_GFX_SIZE[10:0] SIZEX	0x–
Set the Y size of image to be displayed onto LCD panel	DISPC_GFX_SIZE[26:16] SIZEY	0x–
Set the X position of image in respect to LCD panel	DISPC_GFX_POSITION[10:0] POSX	0x–
Set the Y position of image in respect to LCD panel	DISPC_GFX_POSITION[26:16] POSY	0x–

10.2.5.1.2.2.3 Subsequence - Configure the GFX Pipeline Processing

Table 10-66. Configure the GFX Pipeline Processing

Step	Register / Bit Field / Programming Model	Value
Enable replication logic	DISPC_GFX_ATTRIBUTES[5] REPLICATIONENABLE	0x1
Enable nibble mode	DISPC_GFX_ATTRIBUTES[9] NIBBLEMODE	0x1
Enable anti flicker filter	DISPC_GFX_ATTRIBUTES[24] ANTIFLICKER	0x1
Configure the palette table	Refer to Table 10-67	0x–

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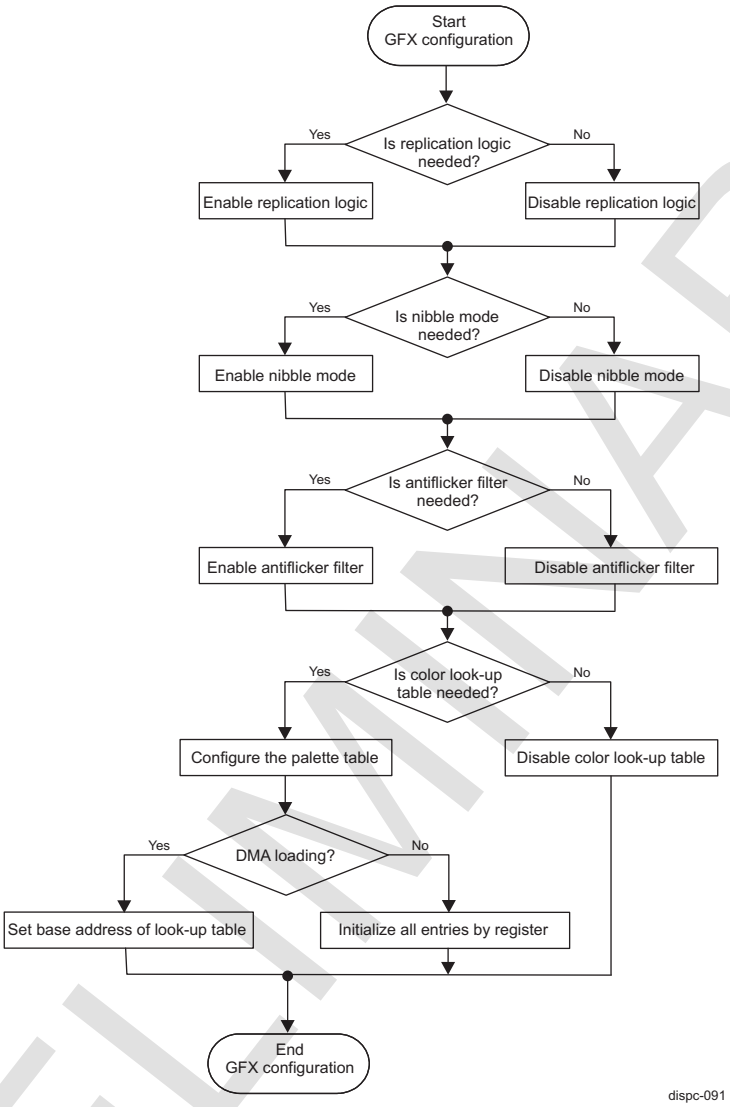
Figure 10-92. Video Pipeline Processing Configuration



10.2.5.1.2.2.4 Subsequence - Configure the Palette Table

This subsequence resumes the settings for configuring the Color Look-Up table as palette for GFX pipeline,

NOTE:

- Software must ensure there is no visible effect when modifying the table since it is not under hardware control and the synchronization done using the DMA engine inside the DISPC to load the table when it is not used for displaying the picture on the screen is not present for this mode.
- If GFX pipeline is in BITMAP pixel format, gamma corrections is not available for LCD1.

Table 10-67. Configure the Palette Table

Step	Register / Bit Field / Programming Model	Value
Set look up table as palette table	DISPC_CONFIG1[3] PALETTEGAMMATABLE	0x0
Select the load mode of the palette look-up table	DISPC_CONFIG1[2:1] LOADMODE	0x–

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Table 10-67. Configure the Palette Table (continued)

Step	Register / Bit Field / Programming Model	Value
DMA loading		
Set base address of look-up table	DISPC_GFX_TABLE_BA[31:0] TABLEBA	0x–
Initialize all entries by register		
Initialize all entries for the palette table by setting the table index and the RGB values associated to this index	DISPC_GAMMA_TABLE0[31:24][23:16][15:8][7:0], INDEX, VALUE_R, VALUE_G, VALUE_B	0x–

10.2.5.1.2.2.5 Subsequence - Configure the GFX Pipeline Layer Output

This subsequence resume the video layer settings available at the pipeline level necessary when using the overlay manager.

Table 10-68. Configure the GFX Pipeline Layer Output

Step	Register / Bit Field / Programming Model	Value
Set the LCD/TV output	DISPC_GFX_ATTRIBUTES[8] CHANNELOUT	0x–
If DISPC_GFX_ATTRIBUTES[8]=0, set the LCD output	DISPC_GFX_ATTRIBUTES[31:30] CHANNELOUT2	0x–
Set the Z-order priority of the layer for overlay manager	DISPC_GFX_ATTRIBUTES[27:26] ZORDER	0x–
Enable the video pipeline Z-order	DISPC_GFX_ATTRIBUTES[25] ZORDERENABLE	0x–
Set the Global Alpha value for the Alpha blender unit	DISPC_GLOBAL_ALPHA[7:0] GFXGLOBALALPHA	0x–

10.2.5.1.2.3 Video Pipeline Configuration

10.2.5.1.2.3.1 Main Sequence - Configure the Video Pipeline

This procedure details the steps for a video pipeline configuration described in Table 10-69.

Table 10-69. Configure the Video Pipeline

Step	Register / Bit Field / Programming Model	Value
Configure the video window	Refer to Table 10-70	
Configure the video pipeline processing	Refer to Table 10-71	
Configure the video pipeline layer output	Refer to Table 10-76	
Validate the video configuration according to outputs associated to the pipeline	DISPC_CONTROL1[5] GOLCD	
	DISPC_CONTROL2[5] GOLCD	
	DISPC_CONTROL2[6] GOWB	
	DISPC_CONTROL1[6] GOTV	
Enable video pipeline	DISPC_VIDp_ATTRIBUTES[0] ENABLE	0x1

10.2.5.1.2.3.2 Subsequence - Configure the Video Window

This subsequence describes the parameters of the image to be displayed on the LCD panel.

Table 10-70. Configure the Video Window

Step	Register / Bit Field / Programming Model	Value
Select the format of image	DISPC_VIDp_ATTRIBUTES[4:1] FORMAT	0x–
Set the X size of image to be displayed onto LCD panel	DISPC_VIDp_SIZE[10:0] SIZEX	0x–

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Table 10-70. Configure the Video Window (continued)

Step	Register / Bit Field / Programming Model	Value
Set the Y size of image to be displayed onto LCD panel	DISPC_VIDp_SIZE[10:0] SIZEY	0x–
Set the X position of image in respect to LCD panel	DISPC_VIDp_POSITION[10:0] POSX	0x–
Set the Y position of image in respect to LCD panel	DISPC_VIDp_POSITION[26:16] POSY	0x–

10.2.5.1.2.3.3 Subsequence - Configure the Video Pipeline Processing

Table 10-71. Configure the Video Pipeline Processing

Step	Register / Bit Field / Programming Model	Value
Select the video pipeline configuration 1 or 2	DISPC_VIDp_ATTRIBUTES2[8] YUVCHROMARESAMPLING	0x–
Enable/disable Replication Logic(1)	DISPC_VIDp_ATTRIBUTES[10] REPLICATIONENABLE	0x1
Configure the VC-1 range mapping(1)	Refer toSection 10.2.5.1.2.3.4	
Configure the video Color Space Conversion(1)	Refer to Section 10.2.5.1.2.3.5	
Configure the video Scaler Unit(1)	Refer to Section 10.2.5.1.2.3.6	

(1) This module configuration can be optional depending on:
- The video mode configuration selected, refer to Figure 10-93
- The video format and application needs

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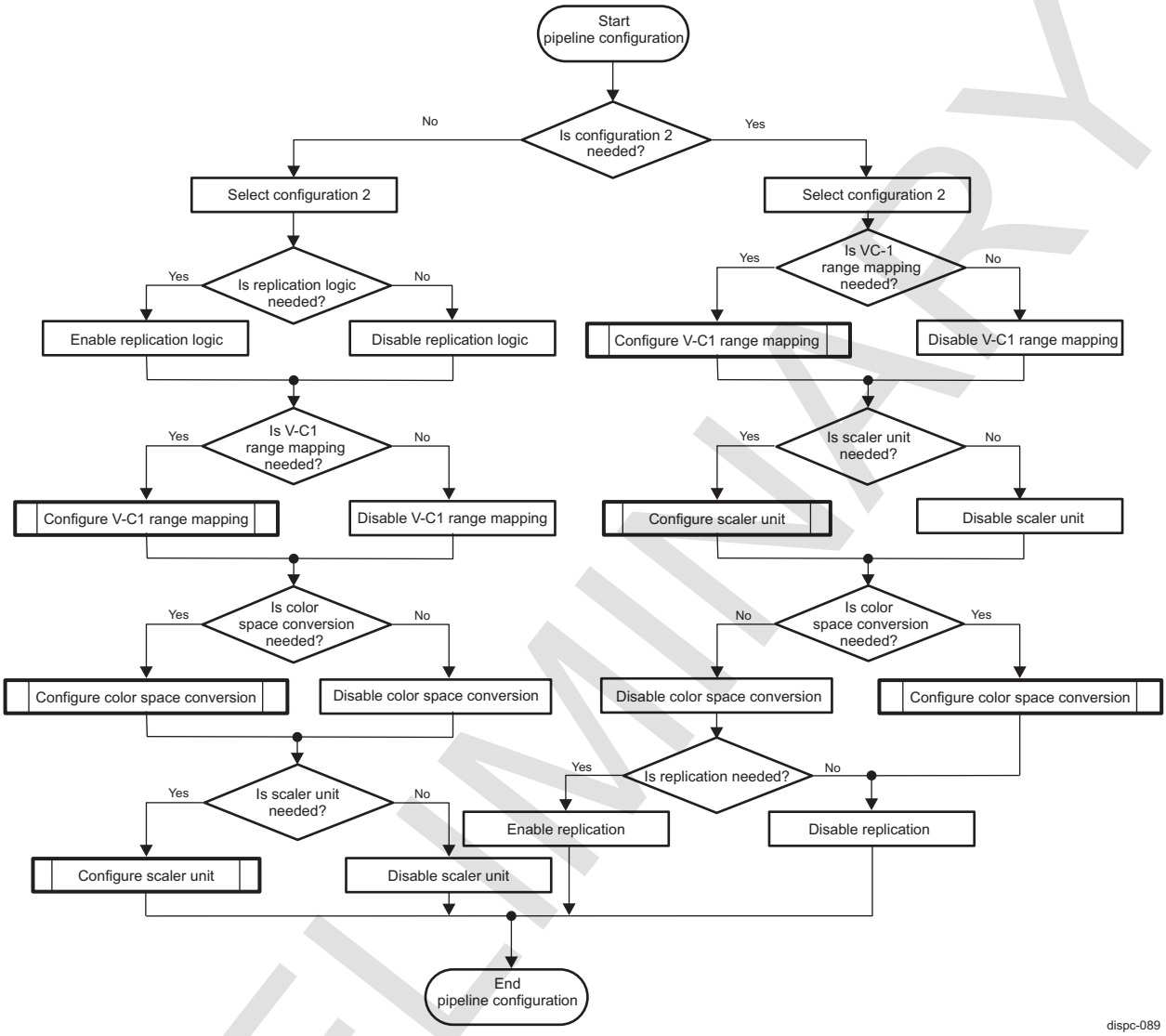
Figure 10-93. Video Pipeline Processing Configuration



10.2.5.1.2.3.4 Subsequence - Configure the VC-1 Range Mapping

Table 10-72. Configure the VC-1 Range Mapping

Step	Register / Bit Field / Programming Model	Value
Set the Y component VC-1 range mapping	DISPC_VIDp_ATTRIBUTES2[3:1] VC1_RANGE_Y	0x–
Set the Cb and Cr component VC-1 range mapping	DISPC_VIDp_ATTRIBUTES2[6:4] VC1_RANGE_CBCR	0x–
Enable VC-1 range mapping	DISPC_VIDp_ATTRIBUTES2[0] VC1ENABLE	0x1

10.2.5.1.2.3.5 Subsequence - Configure the Video Color Space Conversion

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Table 10-73. Configure the Video Color Space Conversion

Step	Register / Bit Field / Programming Model	Value
Select the range of the Color Space Conversion	DISPC_VIDp_ATTRIBUTES[11] FULLRANGE	0x–
Set the RCr and RY coefficients	DISPC_VIDp_CONV_COEF0[26:16][10:0] RCR, RY	0x–
Set the GY and RCb coefficients	DISPC_VIDp_CONV_COEF1[26:16][10:0] GY, RCB	0x–
Set the GCb and GCr coefficients	DISPC_VIDp_CONV_COEF2[26:16][10:0] GCB, GCR	0x–
Set the BCr and BY coefficients	DISPC_VIDp_CONV_COEF3[26:16][10:0] BCR, BY	0x–
Set the BCb coefficient	DISPC_VIDp_CONV_COEF4[10:0] BCB	0x–
Enable Color Space Conversion	DISPC_VIDp_ATTRIBUTES[9] COLORCONVENABLE	0x1

10.2.5.1.2.3.6 Subsequence - Configure the Video Scaler Unit

This subsequence configures the video scaler unit. Table 10-74 is applicable for RGB pixel format. Table 10-74 and Table 10-75 are applicable for YUV pixel format.

Table 10-74. Configure the Video Scaler Unit for RGB Pixel Formats or Y Component

Step	Register / Bit Field / Programming Model	Value
Configure horizontal scaling		
Set the horizontal resizing ratio	DISPC_VIDp_FIR[12:0] FIRHINC	0x–
Set the horizontal FIR coefficients	DISPC_VIDp_FIR_COEF_H_i[31:24][23:16][15:8][7:0] FIRHC3, FIRHC2, FIRHC1, FIRHC0	0x–
	DISPC_VIDp_FIR_COEF_HV_i[7:0] FIRHC4	0x–
Set the horizontal accumulators value	DISPC_VIDp_ACCU_j[10:0] HORIZONTALACCU	0x–
Configure vertical scaling		
Select number of vertical taps	DISPC_VIDp_ATTRIBUTES[21] VERTICALTAPS	0x–
Set the vertical resizing ratio	DISPC_VIDp_FIR[28:16] FIRVINC	0x–
Set the vertical FIR coefficients for RGB pixel format or Y component	DISPC_VIDp_FIR_COEF_HV_i[31:24][23:16][15:8] FIRVC2, FIRVC1, FIRVC0	0x–
	Only for 5-taps vertical: DISPC_VIDp_FIR_COEF_V_i[15:8][7:0] FIRVC22, FIRVC00	0x–
Set the vertical accumulators value for RGB pixel format or Y component	DISPC_VIDp_ACCU_j[26:16] VERTICALACCU	0x–
Enable horizontal and vertical Scaler Unit	DISPC_VIDp_ATTRIBUTES[6:5] RESIZEENABLE	0x–

Table 10-75. Configure the Video Scaler Unit for Cb and Cr Components

Step	Register / Bit Field / Programming Model	Value
Configure horizontal scaling		
Set the horizontal resizing ratio for Cb and Cr components	DISPC_VIDp_FIR2[12:0] FIRHINC	0x–
Set the horizontal FIR coefficients for Cb and Cr components	DISPC_VIDp_FIR_COEF_H2_i[31:24][23:16][15:8][7:0] FIRHC3, FIRHC2, FIRHC1, FIRHC0	0x–
	DISPC_VIDp_FIR_COEF_HV2_i[7:0] FIRHC4	0x–
Set the horizontal accumulators value for Cb and Cr components	DISPC_VIDp_ACCU2_j[10:0] HORIZONTALACCU	0x–
Configure vertical scaling		
Set the vertical resizing ratio for Cb and Cr components	DISPC_VIDp_FIR2[28:16] FIRVINC	0x–

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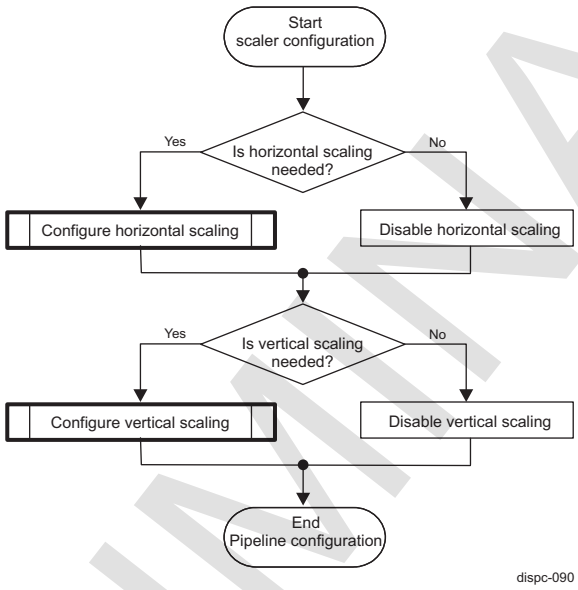
Table 10-75. Configure the Video Scaler Unit for Cb and Cr Components (continued)

Step	Register / Bit Field / Programming Model	Value
Set the vertical FIR coefficients for Cb and Cr components	DISPC_VIDp_FIR_COEF_HV2_i[31:24][23:16][15:8] FIRVC2, FIRVC1, FIRVC0	0x–
	Only for 5-taps vertical: DISPC_VIDp_FIR_COEF_V2_i[15:8][7:0] FIRVC22, FIRVC00	0x–
Set the vertical accumulators value for Cb and Cr components	DISPC_VIDp_ACCU2_j[26:16] VERTICALACCU	0x–

Figure 10-94. Scaler Unit Programming Flow



10.2.5.1.2.3.7 Subsequence - Configure the Video Pipeline Layer Output

This subsequence resume the video layer settings available at the pipeline level necessary when using the overlay manager.

Table 10-76. Configure the Video Pipeline Layer Output

Step	Register / Bit Field / Programming Model	Value
Set the LCD/TV output	DISPC_VIDp_ATTRIBUTES[16] CHANNELOUT	0x–
If DISPC_VIDp_ATTRIBUTES[16]=0, set the LCD output	DISPC_VIDp_ATTRIBUTES[31:30] CHANNELOUT2	0x–
Set the Z-order priority of the layer for overlay manager	DISPC_VIDp_ATTRIBUTES[27:26] ZORDER	0x–
Enable the video pipeline Z-order	DISPC_VIDp_ATTRIBUTES[25] ZORDERENABLE	0x–
Set the Global Alpha value for the Alpha blender unit	DISPC_GLOBAL_ALPHA[31:24][23:16][15:8] VID3GLOBALALPHA, VID2GLOBALALPHA , VID1GLOBALALPHA	0x–

10.2.5.1.2.4 WB Pipeline Configuration

10.2.5.1.2.4.1 Main Sequence - Configure the WB Pipeline

This procedure details the steps for a WB pipeline configuration described in Table 10-77.

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Table 10-77. Configure the WB Pipeline

Step	Register / Bit Field / Programming Model	Value
Configure the Capture window	Refer to Table 10-78	
Configure the WB Scaler unit	Refer to Table 10-79	
Enable truncation logic to match pixel size defined in the format of image DISPC_WB_ATTRIBUTES[4:1] FORMAT	DISPC_WB_ATTRIBUTES[10] TRUNCATIONENABLE	0x–
if DISPC_WB_ATTRIBUTES[10] != , Configure the WB Color Space Conversion unit	Refer to Table 10-81	
Validate the configuration according to the registers modification.(1)	DISPC_CONTROL2[6] GOWB	
Enable WB pipeline	DISPC_WB_ATTRIBUTES[0] ENABLE	0x1

(1) Setting the GOWB bit is required only in WB capture mode; it is not required in WB memory-to-memory mode.

10.2.5.1.2.4.2 Subsequence - Configure the Capture Window

This subsequence describes the parameters of the image to be captured in the system memory.

Table 10-78. Configure the Capture Window

Step	Register / Bit Field / Programming Model	Value
Set the input source	DISPC_WB_ATTRIBUTES[18:16] CHANNELIN	0x–
Select the format of image	DISPC_WB_ATTRIBUTES[4:1] FORMAT	0x–
Set the X size of image to be captured	DISPC_WB_SIZE[10:0] SIZEX	0x–
Set the Y size of image to be captured	DISPC_WB_SIZE[10:0] SIZEY	0x–

10.2.5.1.2.4.3 Subsequence - Configure the WB Scaler Unit

This subsequence configures the scaler unit. Table 10-74 is applicable for RGB pixel format. Table 10-74 and Table 10-75 are applicable for YUV pixel format.

Table 10-79. Configure the WB Scaler Unit for RGB Pixel Formats or Y Component

Step	Register / Bit Field / Programming Model	Value
Configure horizontal scaling		
Set the horizontal resizing ratio	DISPC_WB_FIR[12:0] FIRHINC	0x–
Set the horizontal FIR coefficients	DISPC_WB_FIR_COEF_H_i[31:24][23:16][15:8][7:0] FIRHC3, FIRHC2, FIRHC1, FIRHC0	0x–
	DISPC_WB_FIR_COEF_HV_i[7:0] FIRHC4	0x–
Set the horizontal accumulators value	DISPC_WB_ACCU_j[10:0] HORIZONTALACCU	0x–
Configure vertical scaling		
Select number of vertical taps	DISPC_WB_ATTRIBUTES[21] VERTICALTAPS	0x–
Set the vertical resizing ratio	DISPC_WB_FIR[28:16] FIRVINC	0x–
Set the vertical FIR coefficients for RGB pixel format or Y component	DISPC_WB_FIR_COEF_HV_i[31:24][23:16][15:8] FIRVC2, FIRVC1, FIRVC0	0x–
	Only for 5-taps vertical: DISPC_WB_FIR_COEF_V_i[15:8][7:0] FIRVC22, FIRVC00	0x–
Set the vertical accumulators value for RGB pixel format or Y component	DISPC_WB_ACCU_j[26:16] VERTICALACCU	0x–
Enable horizontal and vertical Scaler Unit	DISPC_WB_ATTRIBUTES[6:5] RESIZEENABLE	0x–

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Table 10-80. Configure the WB Scaler Unit for Cb and Cr Components

Step	Register / Bit Field / Programming Model	Value
Configure horizontal scaling		
Set the horizontal resizing ratio for Cb and Cr components	DISPC_WB_FIR2[12:0] FIRHINC	0x–
Set the horizontal FIR coefficients for Cb and Cr components	DISPC_WB_FIR_COEF_H2_i[31:24][23:16][15:8][7:0] FIRHC3, FIRHC2, FIRHC1, FIRHC0	0x–
	DISPC_WB_FIR_COEF_HV2_i[7:0] FIRHC4	0x–
Set the horizontal accumulators value for Cb and Cr components	DISPC_WB_ACCU2_j[10:0] HORIZONTALACCU	0x–
Configure vertical scaling		
Set the vertical resizing ratio for Cb and Cr components	DISPC_WB_FIR2[28:16] FIRVINC	0x–
Set the vertical FIR coefficients for Cb and Cr components	DISPC_WB_FIR_COEF_HV2_i[31:24][23:16][15:8] FIRVC2, FIRVC1, FIRVC0	0x–
	Only for 5-taps vertical: DISPC_WB_FIR_COEF_V2_i[15:8][7:0] FIRVC22, FIRVC00	0x–
Set the vertical accumulators value for Cb and Cr components	DISPC_WB_ACCU2_j[26:16] VERTICALACCU	0x–

10.2.5.1.2.4.4 Subsequence - Configure the WB Color Space Conversion Unit

Table 10-81. Configure the WB Color Space Conversion Unit

Step	Register / Bit Field / Programming Model	Value
Select the range of the Color Space Conversion	DISPC_WB_ATTRIBUTES[11] FULLRANGE	0x–
Set the RCr and RY coefficients	DISPC_WB_CONV_COEF0[26:16][10:0] YG, YR	0x–
Set the GY and RCb coefficients	DISPC_WB_CONV_COEF1[26:16][10:0] CRR, YB	0x–
Set the GCb and GCr coefficients	DISPC_WB_CONV_COEF2[26:16][10:0] CRB, CRG	0x–
Set the BCr and BY coefficients	DISPC_WB_CONV_COEF3[26:16][10:0] CBG, CBR	0x–
Set the BCb coefficient	DISPC_WB_CONV_COEF4[10:0] CBB	0x–
Enable Color Space Conversion	DISPC_WB_ATTRIBUTES[9] COLORCONVENABLE	0x1

10.2.5.1.2.5 LCD Output Configuration

10.2.5.1.2.5.1 Main Sequence - Configure the LCD Output

This procedure details the LCD output configuration.

Table 10-82. Configure the LCD Output

Step	Register / Bit Field / Programming Model
Configure the LCD overlay manager	Table 10-83
Configure the gamma table for gamma correction	Section 10.2.5.1.2.5.3
Configure the Color Phase Rotation	Table 10-86
Configure the LCD panel timings and parameters	Table 10-87
Validate the LCD output configuration according	DISPC_CONTROL1[5] GOLCD
	DISPC_CONTROL2[5] GOLCD
Enable LCD output	DISPC_CONTROL1[0] LCDENABLE
	DISPC_CONTROL2[0] LCDENABLE

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10.2.5.1.2.5.2 Subsequence - Configure the Overlay Manager

This subsequence resumes the overlay manager settings and transparency color key configuration.

Table 10-83. Configure the LCD Overlay Manager

Step	Register / Bit Field / Programming Model	Value
Set the LCD panel background color	DISPC_DEFAULT_COLORo[23:0] DEFAULTCOLOR	0x–
Enable/Disable overlay optimization	DISPC_CONTROLo[12] OVERLAYOPTIMIZATION	0x–
Enable the Alpha blender[(1)]	DISPC_CONFIG1[18] LCDALPHABLENDERENABLE	0x1
Configure the transparency color key		
Set source or destination transparency color key mode	DISPC_CONFIGo[11] TCKLCDSELECTION	0x–
Set the transparency color value	DISPC_TRANS_COLORo[23:0] TRANSCOLORKEY	0x–
Enable transparency color key mode	DISPC_CONFIGo[10] TCKLCDENABLE	0x–

(1) Backward compatibility with OMAP34xx only available for LCD1.

10.2.5.1.2.5.3 Subsequence - Configure the Gamma Table for Gamma Correction

This subsequence resumes the settings for configuring the gamma correction for LCD1, see Table 10-84 and LCD2, see Table 10-85.

NOTE:

- Software must ensure there is no visible effect when modifying the table because it is not under hardware control and the synchronization done using the DMA engine inside the DISPC to load the table when it is not used for displaying the picture on the screen is not present for this mode.
- If GFX pipeline is in BITMAP pixel format, gamma corrections is not available for LCD1.

Table 10-84. Configure the Gamma Table for LCD1

Step	Register / Bit Field / Programming Model	Value
Initialize all entries for the gamma table by setting the table index and the RGB values associated to this index	DISPC_GAMMA_TABLE0[31:24][23:16][15:8][7:0], INDEX, VALUE_R, VALUE_G, VALUE_B	0x–
Set look up table as gamma table	DISPC_CONFIG1[3] PALETTEGAMMATABLE	0x1
Select the load mode of the Gamma look-up table	DISPC_CONFIG1[2:1] LOADMODE	0x–

Table 10-85. Configure the Gamma Table for LCD2

Step	Register / Bit Field / Programming Model	Value
Enable Gamma table for LCD2 and TV	DISPC_CONFIG1[9] GAMATABLEENABLE	0x1
Initialize all entries for the gamma table by setting the table index and the RGB values associated to this index.	DISPC_GAMMA_TABLE1[31:24][23:16][15:8][7:0], INDEX, VALUE_R, VALUE_G, VALUE_B	0x–

10.2.5.1.2.5.4 Subsequence - Configure the Color Phase Rotation

Table 10-86 resumes the settings for the Color Phase Rotation unit.

Table 10-86. Configure the Color Phase Rotation

Step	Register / Bit Field / Programming Model	Value
Set the Red coefficients	DISPC_CPRo_COEF_R [31:22][20:11][9:0] RR, RG, RB	0x–
Set the Green coefficients	DISPC_CPRo_COEF_G [31:22][20:11][9:0] GR, GG, GB	0x–

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Table 10-86. Configure the Color Phase Rotation (continued)

Step	Register / Bit Field / Programming Model	Value
Set the Blue coefficients	DISPC_CPRo_COEF_B [31:22][20:11][9:0] BR, BG, BB	0x–
Disable Color Phase Rotation unit in RGB to YUV conversion	DISPC_CONFIGo[24] COLORCONVENABLE	0x0
Enable Color Phase Rotation unit	DISPC_CONFIGo[15] CPR	0x1

10.2.5.1.2.5.5 Subsequence - Configure the LCD Panel Timings and Parameters

This subsequence resumes the setting for horizontal and vertical synchronization and also the signals polarity.

Table 10-87. Configure the LCD Panel Timings and Parameters

Step	Register / Bit Field / Programming Model	Value
Configure Spatial/Temporal Dithering		
Select Spatial/Temporal number of frames	DISPC_CONTROLo[31:30] SPATIALTEMPORALDITHERINGFRAMES	0x–
Enable Spatial/Temporal dithering	DISPC_CONTROLo[7] STDITHERENABLE	0x–
Configure AC-bias		
Configure the VSYNC, HSYNC and AC bias polarity	DISPC_POL_FREQo	0x–
Configure the gating of AC bias polarity	DISPC_CONFIGo[8] ACBIASGATED	0x–
Configure the AC bias polarity	DISPC_POL_FREQo[15] IEO	0x–
Set the AC bias frequency	DISPC_POL_FREQo[7:0] ACB	0x–
Set the number of AC bias transitions per interrupt	DISPC_POL_FREQo[11:8] ACBI	0x–
Configure the pixel clock		
Set the DISPC logic clock divisor	DISPC_DIVISORo[23:16] LCD	0x–
Set the pixel clock divisor	DISPC_DIVISORo[7:0] PCD	0x–
Configure the gating of Pixel clock	DISPC_CONFIGo[5] PIXELCLOCKGATED	0x–
Configure the data		
Set the pixel clock edge to drive data output	DISPC_POL_FREQo[14] IPC	0x–
Configure the gating of data output	DISPC_CONFIGo[4] PIXELDATAGATED	0x–
Set the data output mode	DISPC_CONFIGo[22] OUTPUTMODEENABLE	0x–
Configure the panel parameters		
Set the vertical TV size	DISPC_SIZE_LCDo[26:16] LPP	0x–
Set the horizontal TV size	DISPC_SIZE_LCDo[10:0] PPL	0x–
Set the panel type	DISPC_CONTROLo[3] STNTFT	0x–
Configure the refresh rate and horizontal and vertical parameters		
Set the vertical synchronization timing	DISPC_TIMING_Vo[31:20][19:8][7:0],VBP, VFP, VSW	0x–
Configure the VSYNC polarity	DISPC_POL_FREQo[12] IVS	0x–
Configure the gating of VSYNC	DISPC_CONFIGo[7] VSYNCGATED	0x–
Set the horizontal synchronization timing	DISPC_TIMING_Ho[31:20][19:8][7:0],HBP, HFP, HSW	0x–
Configure the HSYNC polarity	DISPC_POL_FREQo[13] IHS	0x–
Configure the gating of HSYNC	DISPC_CONFIGo[6] HSYNCGATED	0x–
Set the opposition of HSYNC and VSYNC driving	DISPC_POL_FREQo[17] ONOFF	0x–
If DISPC_POL_FREQo[17] = 1, set the pixel clock edge to drive HSYNC and VSYNC	DISPC_POL_FREQo[16] RF	0x–
Set the alignment of HSYNC and VSYNC	DISPC_POL_FREQo[18] ALIGN	0x–

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10.2.5.1.2.6 TV Output Configuration

Main Sequence - Configure the TV Output

This procedure details the TV output configuration.

Table 10-88. Configure the TV Output

Step	Register / Bit Field / Programming Model
Configure the TV overlay manager	Refer to Table 10-89
Configure the gamma table for gamma correction	Refer to Table 10-90
Configure the TV panel timings and parameters	Refer to Table 10-91
Validate the TV output configuration according	DISPC_CONTROL1[6] GOTV
Enable TV output	DISPC_CONTROL1[1] TVENABLE

10.2.5.1.2.6.1 Subsequence - Configure the TV Overlay Manager

This subsequence resumes the overlay manager settings and transparency color key configuration.

Table 10-89. Configure the TV Overlay Manager

Step	Register / Bit Field / Programming Model	Value
Set the TV panel background color	DISPC_DEFAULT_COLOR1[23:0] DEFAULTCOLOR	0x–
Enable/Disable overlay optimization	DISPC_CONTROL2[13] TVOVERLAYOPTIMIZATION	0x–
Enable the Alpha blender(1)	DISPC_CONFIG1[19] TVALPHABLENDERENABLE	0x1
Configure the transparency color key		
Set source or destination transparency color key mode	DISPC_CONFIG1[13] TCKTVSELECTION	0x–
Set the transparency color value	DISPC_TRANS_COLOR1[23:0] TRANSCOLORKEY	0x–
Enable transparency color key mode	DISPC_CONFIG1[10] TCKTVENABLE	0x–

(1) Backward compatibility with OMAP34xx.

10.2.5.1.2.6.2 Subsequence - Configure the Gamma Table for Gamma Correction

NOTE:

- Software must ensure there is no visible effect when modifying the table since it is not under hardware control and the synchronization done using the DMA engine inside the DISPC to load the table when it is not used for displaying the picture on the screen is not present for this mode.

Table 10-90. Configure the Gamma Table for TV Output

Step	Register / Bit Field / Programming Model	Value
Enable Gamma table for LCD2 and TV	DISPC_CONFIG1[9] GAMATABLEENABLE	0x1
Initialize all entries for the gamma table by setting the table index and the RGB values. For more information, see Section 10.2.4.13.2, *Gamma Correction Unit*.	DISPC_GAMMA_TABLE2[31][29:20][19:10][9:0], INDEX, VALUE_R, VALUE_G, VALUE_B	0x–

10.2.5.1.2.6.3 Subsequence - Configure the TV Panel Timings and Parameters

This subsequence resumes the setting for horizontal and vertical synchronization and also the signals polarity.

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Table 10-91. Configure the TV Panel Timings and Parameters

Step	Register / Bit Field / Programming Model	Value
Set the hold time for TV data outputs	DISPC_CONFIG1[19:17]	0x–
Set the vertical TV size	DISPC_SIZE_TV[26:16] LPP	See Table 10-92 for NTSC/PAL and HD standards
Set the horizontal TV size	DISPC_SIZE_TV[10:0] PPL	

Table 10-92. DISPC_SIZE_TV Values NTSC/PAL and HD Standard

Standards		Active Pixels/line (PPL)	Active Lines (LPP)	Digital clock (DISPC_CONTROL1. HT=0)	DISPC_SIZE_TV
ITU-R BT.601	NTSC(J, M, 4.43)	720	480	13.5 MHz	0x00EF02CF
	PAL(B, D, G, H, I, N)	720	576	13.5 MHz	0x011F02CF
	PAL(M)	720	480	13.5 MHz	0x00EF02CF
Square Pixel	NTSC(J, M, 4.43)	640	480	12.2727 MHz	0x00EF027F
	PAL(B, D, G, H, I, N)	768	576	14.75 MHz	0x011F02FF
	PAL(M)	640	480	12.2727 MHz	0x00EF027F
HDTV	720p	1280	720	74.25/74.125 MHz (60/59.99..frames/s)	0x02CF04FF
	1080i	1920	540	74.25/74.125 MHz (60/59.99..fields/s)	0x021B07FF
	1080p	1920	1080	148.5/148.25 MHz (60/59.99..frames/s)	0x043707FF

NOTE: The VDAC function is not supported.

10.2.6 Display Controller Use Cases and Tips

10.2.6.1 Hardware Cursor

The video layer or graphics layer can be used to display the hardware cursor. The encoded pixel data for the cursor image are in xRGB12-4444, ARGB16-4444, RGBx12-4444, RGBA16-4444, ARGB16-1555, RGB16-565, RGB24-888, xRGB24-88888, RGBA32-8888 or ARGB32-8888 formats if the source transparency color key is used; otherwise, any pixel format can be used for the cursor image considering the limitation in term of pixel supported by the pipeline used to display the cursor image. To display nonrectangle cursor, the transparency color key can be used or the alpha blending (pixel alpha blending); see Section 10.2.4.12.1.3. The global alpha blending can be used in addition to the transparency source color key to make some fading effect when the cursor (with a nonrectangle shape) appears and disappears on the screen. The image of the cursor can be stored totally inside the DMA buffer in order to use the self-refresh mode (see Section 10.2.4.6.6.2). In that case, the image is loaded once and then displayed without accessing the system memory for loading the image for each frame. This saves bandwidth on interconnect and memory.

10.2.7 Display Controller Register Manual

CAUTION

The main access to all DISPC registers is through the L3 interconnect.

The access through L4_PER interconnect is provided for back software compatibility.

10.2.7.1 Display Controller Instance Summary

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Table 10-93. DISPC Instance Summary

Module Name	L4_PER Base Address	L3 Base Address	Size
DISPC	0x4804 1000	0x5800 1000	4KB

10.2.7.2 Display Controller Logical Register Mapping

Table 10-94. DISPC_VIDp_BA_j Logical Register Mapping

Hardware Register	Description
DISPC_VID1_BA_j	Base Address of Video Pipeline 1
DISPC_VID2_BA_j	Base Address of Video Pipeline 2
DISPC_VID3_BA_j	Base Address of Video Pipeline 3

Table 10-95. DISPC_VIDp_BA_UV_j Logical Register Mapping

Hardware Register	Description
DISPC_VID1_BA_UV_j	Base Address of UV components for Video Pipeline 1
DISPC_VID2_BA_UV_j	Base Address of UV components for Video Pipeline 2
DISPC_VID3_BA_UV_j	Base Address of UV components for Video Pipeline 3

Table 10-96. DISPC_VIDp_POSITION Logical Register Mapping

Hardware Register	Description
DISPC_VID1_POSITION	Position of the video window 1
DISPC_VID2_POSITION	Position of the video window 2
DISPC_VID3_POSITION	Position of the video window 3

Table 10-97. DISPC_VIDp_SIZE Logical Register Mapping

Hardware Register	Description
DISPC_VID1_SIZE	Size of the video window 1
DISPC_VID2_SIZE	Size of the video window 2
DISPC_VID3_SIZE	Size of the video window 3

Table 10-98. DISPC_VIDp_ATTRIBUTES Logical Register Mapping

Hardware Register	Description
DISPC_VID1_ATTRIBUTES	Configuration of the video pipeline 1
DISPC_VID2_ATTRIBUTES	Configuration of the video pipeline 2
DISPC_VID3_ATTRIBUTES	Configuration of the video pipeline 3

Table 10-99. DISPC_VIDp_ATTRIBUTES2 Logical Register Mapping

Hardware Register	Description
DISPC_VID1_ATTRIBUTES2	Configuration of the video pipeline 1
DISPC_VID2_ATTRIBUTES2	Configuration of the video pipeline 2
DISPC_VID3_ATTRIBUTES2	Configuration of the video pipeline 3

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Table 10-100. DISPC_VIDp_BUF_THRESHOLD Logical Register Mapping

Hardware Register	Description
DISPC_VID1_BUF_THRESHOLD	Configuration of the buffer for the video pipeline 1
DISPC_VID2_BUF_THRESHOLD	Configuration of the buffer for the video pipeline 2
DISPC_VID3_BUF_THRESHOLD	Configuration of the buffer for the video pipeline 3

Table 10-101. DISPC_VIDp_ROW_INC Logical Register Mapping

Hardware Register	Description
DISPC_VID1_ROW_INC	Configuration of the row increment for the video pipeline 1
DISPC_VID2_ROW_INC	Configuration of the row increment for the video pipeline 2
DISPC_VID3_ROW_INC	Configuration of the row increment for the video pipeline 3

Table 10-102. DISPC_VIDp_PIXEL_INC Logical Register Mapping

Hardware Register	Description
DISPC_VID1_PIXEL_INC	Configuration of the pixel increment for the video pipeline 1
DISPC_VID2_PIXEL_INC	Configuration of the pixel increment for the video pipeline 2
DISPC_VID3_PIXEL_INC	Configuration of the pixel increment for the video pipeline 3

Table 10-103. DISPC_VIDp_FIR Logical Register Mapping

Hardware Register	Description
DISPC_VID1_FIR	Configuration of the scaler for the video pipeline 1
DISPC_VID2_FIR	Configuration of the scaler for the video pipeline 2
DISPC_VID3_FIR	Configuration of the scaler for the video pipeline 3

Table 10-104. DISPC_VIDp_PICTURE_SIZE Logical Register Mapping

Hardware Register	Description
DISPC_VID1_PICTURE_SIZE	Size of the video window 1 before processing
DISPC_VID2_PICTURE_SIZE	Size of the video window 2 before processing
DISPC_VID3_PICTURE_SIZE	Size of the video window 3 before processing

Table 10-105. DISPC_VIDp_ACCU_j Logical Register Mapping

Hardware Register	Description
DISPC_VID1_ACCU_j	Configuration of the accumulator for the video pipeline 1
DISPC_VID2_ACCU_j	Configuration of the accumulator for the video pipeline 2
DISPC_VID2_ACCU_j	Configuration of the accumulator for the video pipeline 3

Table 10-106. DISPC_VIDp_FIR_COEF_H_i Logical Register Mapping

Hardware Register	Description
DISPC_VID1_FIR_COEF_H_i	Configuration of the horizontal scaling coefficients for the video pipeline 1
DISPC_VID2_FIR_COEF_H_i	Configuration of the horizontal scaling coefficients for the video pipeline 2
DISPC_VID3_FIR_COEF_H_i	Configuration of the horizontal scaling coefficients or the video pipeline 3

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Table 10-107. DISPC_VIDp_FIR_COEF_HV_i Logical Register Mapping

Hardware Register	Description
DISPC_VID1_FIR_COEF_HV_i	Configuration of the horizontal scaling coefficients for the video pipeline 1
DISPC_VID2_FIR_COEF_HV_i	Configuration of the horizontal scaling coefficients for the video pipeline 2
DISPC_VID3_FIR_COEF_HV_i	Configuration of the horizontal scaling coefficients for the video pipeline 3

Table 10-108. DISPC_VIDp_FIR_COEF_V_i Logical Register Mapping

Hardware Register	Description
DISPC_VID1_FIR_COEF_V_i	Configuration of the vertical scaling coefficients for the video pipeline 1
DISPC_VID2_FIR_COEF_V_i	Configuration of the vertical scaling coefficients for the video pipeline 2
DISPC_VID3_FIR_COEF_V_i	Configuration of the vertical scaling coefficients for the video pipeline 3

Table 10-109. DISPC_VIDp_FIR_COEF_H2_i Logical Register Mapping

Hardware Register	Description
DISPC_VID1_FIR_COEF_H2_i	Configuration of the horizontal Cb and Cr scaling coefficients for the video pipeline 1
DISPC_VID2_FIR_COEF_H2_i	Configuration of the horizontal Cb and Cr scaling coefficients for the video pipeline 2
DISPC_VID3_FIR_COEF_H2_i	Configuration of the horizontal Cb and Cr scaling coefficients or the video pipeline 3

Table 10-110. DISPC_VIDp_FIR_COEF_HV2_i Logical Register Mapping

Hardware Register	Description
DISPC_VID1_FIR_COEF_HV2_i	Configuration of the horizontal Cb and Cr scaling coefficients for the video pipeline 1
DISPC_VID2_FIR_COEF_HV2_i	Configuration of the horizontal Cb and Cr scaling coefficients for the video pipeline 2
DISPC_VID3_FIR_COEF_HV2_i	Configuration of the horizontal Cb and Cr scaling coefficients for the video pipeline 3

Table 10-111. DISPC_VIDp_FIR_COEF_V2_i Logical Register Mapping

Hardware Register	Description
DISPC_VID1_FIR_COEF_V2_i	Configuration of the vertical Cb and Cr scaling coefficients for the video pipeline 1
DISPC_VID2_FIR_COEF_V2_i	Configuration of the vertical Cb and Cr scaling coefficients for the video pipeline 2
DISPC_VID3_FIR_COEF_V2_i	Configuration of the vertical Cb and Cr scaling coefficients for the video pipeline 3

Table 10-112. DISPC_VIDp_CONV_COEF0 Logical Register Mapping

Hardware Register	Description
DISPC_VID1_CONV_COEF0	Configuration of the Color Space Conversion coefficients for the video pipeline 1
DISPC_VID2_CONV_COEF0	Configuration of the Color Space Conversion coefficient for the video pipeline 2
DISPC_VID3_CONV_COEF0	Configuration of the Color Space Conversion coefficient for the video pipeline 3

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Table 10-113. DISPC_VIDp_CONV_COEF1 Logical Register Mapping

Hardware Register	Description
DISPC_VID1_CONV_COEF1	Configuration of the Color Space Conversion coefficients for the video pipeline 1
DISPC_VID2_CONV_COEF1	Configuration of the Color Space Conversion coefficient for the video pipeline 2
DISPC_VID3_CONV_COEF1	Configuration of the Color Space Conversion coefficient for the video pipeline 3

Table 10-114. DISPC_VIDp_CONV_COEF2 Logical Register Mapping

Hardware Register	Description
DISPC_VID1_CONV_COEF2	Configuration of the Color Space Conversion coefficients for the video pipeline 1
DISPC_VID2_CONV_COEF2	Configuration of the Color Space Conversion coefficient for the video pipeline 2
DISPC_VID3_CONV_COEF2	Configuration of the Color Space Conversion coefficient for the video pipeline 3

Table 10-115. DISPC_VIDp_CONV_COEF3 Logical Register Mapping

Hardware Register	Description
DISPC_VID1_CONV_COEF3	Configuration of the Color Space Conversion coefficients for the video pipeline 1
DISPC_VID2_CONV_COEF3	Configuration of the Color Space Conversion coefficient for the video pipeline 2
DISPC_VID3_CONV_COEF3	Configuration of the Color Space Conversion coefficient for the video pipeline 3

Table 10-116. DISPC_VIDp_CONV_COEF4 Logical Register Mapping

Hardware Register	Description
DISPC_VID1_CONV_COEF4	Configuration of the Color Space Conversion coefficients for the video pipeline 1
DISPC_VID2_CONV_COEF4	Configuration of the Color Space Conversion coefficient for the video pipeline 2
DISPC_VID3_CONV_COEF4	Configuration of the Color Space Conversion coefficient for the video pipeline 3

Table 10-117. DISPC_CONTROLo Logical Register Mapping

Hardware Register	Description
DISPC_CONTROL1	Configuration control of the LCD1 and TV.
DISPC_CONTROL2	Configuration control of the LCD2.

Table 10-118. DISPC_CONFIGo Logical Register Mapping

Hardware Register	Description
DISPC_CONFIG1	Configuration of the LCD1 and TV.
DISPC_CONFIG2	Configuration of the LCD2.

Table 10-119. DISPC_DEFAULT_COLORo Logical Register Mapping

Hardware Register	Description
DISPC_DEFAULT_COLOR0	Configuration of the background color for LCD1.
DISPC_DEFAULT_COLOR1	Configuration of the background color for LCD2.

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Table 10-120. DISPC_TRANS_COLORo Logical Register Mapping

Hardware Register	Description
DISPC_TRANS_COLOR0	Configuration of the transparency color key for LCD1.
DISPC_TRANS_COLOR1	Configuration of the transparency color key for LCD2.

Table 10-121. DISPC_GAMMA_TABLEo Logical Register Mapping

Hardware Register	Description
DISPC_GAMMA_TABLE0	Configuration of the palette table for GFX or the gamma table for LCD1.
DISPC_GAMMA_TABLE1	Configuration of the gamma table for LCD2.
DISPC_GAMMA_TABLE2	Configuration of the gamma table for TV output.

Table 10-122. DISPC_TIMING_Ho Logical Register Mapping

Hardware Register	Description
DISPC_TIMING_H1	Configuration of the horizontal timing for LCD1.
DISPC_TIMING_H2	Configuration of the horizontal timing for LCD2.

Table 10-123. DISPC_TIMING_Vo Logical Register Mapping

Hardware Register	Description
DISPC_TIMING_V1	Configuration of the vertical timing for LCD1.
DISPC_TIMING_V2	Configuration of the vertical timing for LCD2.

Table 10-124. DISPC_POL_FREQo Logical Register Mapping

Hardware Register	Description
DISPC_POL_FREQ1	Configuration of the output signals for LCD1.
DISPC_POL_FREQ2	Configuration of the output signals for LCD2.

Table 10-125. DISPC_DIVISORo Logical Register Mapping

Hardware Register	Description
DISPC_DIVISOR1	Configuration of the divisors for LCD1.
DISPC_DIVISOR2	Configuration of the divisors for LCD2.

Table 10-126. DISPC_SIZE_LCDo Logical Register Mapping

Hardware Register	Description
DISPC_SIZE_LCD1	Configuration of the divisors for LCD1.
DISPC_SIZE_LCD2	Configuration of the divisors for LCD2.

Table 10-127. DISPC_SIZE Logical Register Mapping

Hardware Register	Description
DISPC_SIZE_LCD1	Configuration of the LCD size on LCD1.
DISPC_SIZE_LCD2	Configuration of the LCD size on LCD2.

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Table 10-128. DISPC_DATAo_CYCLE1 Logical Register Mapping

Hardware Register	Description
DISPC_DATA1_CYCLE1	Configuration of the output data format for 1st cycle on LCD1.
DISPC_DATA2_CYCLE1	Configuration of the output data format for 1st cycle on LCD2.

Table 10-129. DISPC_DATAo_CYCLE2 Logical Register Mapping

Hardware Register	Description
DISPC_DATA1_CYCLE2	Configuration of the output data format for 2nd cycle on LCD1.
DISPC_DATA2_CYCLE2	Configuration of the output data format for 2nd cycle on LCD2.

Table 10-130. DISPC_DATAo_CYCLE3 Logical Register Mapping

Hardware Register	Description
DISPC_DATA1_CYCLE3	Configuration of the output data format for 3rd cycle on LCD1.
DISPC_DATA2_CYCLE3	Configuration of the output data format for 3rd cycle on LCD2.

Table 10-131. DISPC_CPRo_COEF_R Logical Register Mapping

Hardware Register	Description
DISPC_CPR1_COEF_R	Configuration of the CPR matrix coefficients for the Red component on LCD1.
DISPC_CPR2_COEF_R	Configuration of the CPR matrix coefficients for the Red component on LCD2.

Table 10-132. DISPC_CPRo_COEF_G Logical Register Mapping

Hardware Register	Description
DISPC_CPR1_COEF_G	Configuration of the CPR matrix coefficients for the Green component on LCD1.
DISPC_CPR2_COEF_G	Configuration of the CPR matrix coefficients for the Green component on LCD2.

Table 10-133. DISPC_CPRo_COEF_B Logical Register Mapping

Hardware Register	Description
DISPC_CPR1_COEF_B	Configuration of the CPR matrix coefficients for the Blue component on LCD1.
DISPC_CPR2_COEF_B	Configuration of the CPR matrix coefficients for the Blue component on LCD2.

10.2.7.3 Display Controller Registers

10.2.7.3.1 Display Controller Register Summary

Table 10-134. Display Controller Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	DISPC L4_PER Physical Address	DISPC L3 Physical Address
DISPC_REVISION	R	32	0x0000 0000	0x4804 1000	0x5800 1000
DISPC_SYSCONFIG	RW	32	0x0000 0010	0x4804 1010	0x5800 1010
DISPC_SYSSTATUS	R	32	0x0000 0014	0x4804 1014	0x5800 1014
DISPC_IRQSTATUS	RW	32	0x0000 0018	0x4804 1018	0x5800 1018

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Table 10-134. Display Controller Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	DISPC L4_PER Physical Address	DISPC L3 Physical Address
DISPC_IRQENABLE	RW	32	0x0000 001C	0x4804 101C	0x5800 101C
DISPC_CONTROL1	RW	32	0x0000 0040	0x4804 1040	0x5800 1040
DISPC_CONFIG1	RW	32	0x0000 0044	0x4804 1044	0x5800 1044
RESERVED	R	32	0x0000 0048	0x4804 1048	0x5800 1048
DISPC_DEFAULT_COLOR0	RW	32	0x0000 004C	0x4804 104C	0x5800 104C
DISPC_DEFAULT_COLOR1	RW	32	0x0000 0050	0x4804 1050	0x5800 1050
DISPC_TRANS_COLOR0	RW	32	0x0000 0054	0x4804 1054	0x5800 1054
DISPC_TRANS_COLOR1	RW	32	0x0000 0058	0x4804 1058	0x5800 1058
DISPC_LINE_STATUS	R	32	0x0000 005C	0x4804 105C	0x5800 105C
DISPC_LINE_NUMBER	RW	32	0x0000 0060	0x4804 1060	0x5800 1060
DISPC_TIMING_H1	RW	32	0x0000 0064	0x4804 1064	0x5800 1064
DISPC_TIMING_V1	RW	32	0x0000 0068	0x4804 1068	0x5800 1068
DISPC_POL_FREQ1	RW	32	0x0000 006C	0x4804 106C	0x5800 106C
DISPC_DIVISOR1	RW	32	0x0000 0070	0x4804 1070	0x5800 1070
DISPC_GLOBAL_ALPHA	RW	32	0x0000 0074	0x4804 1074	0x5800 1074
DISPC_SIZE_TV	RW	32	0x0000 0078	0x4804 1078	0x5800 1078
DISPC_SIZE_LCD1	RW	32	0x0000 007C	0x4804 107C	0x5800 107C
DISPC_GFX_BA_j (1)	RW	32	0x0000 0080 + (0x4 * j)	0x4804 1080 + (0x4 * j)	0x5800 1080 + (0x4 * j)
DISPC_GFX_POSITION	RW	32	0x0000 0088	0x4804 1088	0x5800 1088
DISPC_GFX_SIZE	RW	32	0x0000 008C	0x4804 108C	0x5800 108C
DISPC_GFX_ATTRIBUTES	RW	32	0x0000 00A0	0x4804 10A0	0x5800 10A0
DISPC_GFX_BUF_THRESHOLD	RW	32	0x0000 00A4	0x4804 10A4	0x5800 10A4
DISPC_GFX_BUF_SIZE_STATUS	R	32	0x0000 00A8	0x4804 10A8	0x5800 10A8
DISPC_GFX_ROW_INC	RW	32	0x0000 00AC	0x4804 10AC	0x5800 10AC
DISPC_GFX_PIXEL_INC	RW	32	0x0000 00B0	0x4804 10B0	0x5800 10B0
DISPC_GFX_WINDOW_SKIP	R	32	0x0000 00B4	0x4804 10B4	0x5800 10B4
DISPC_GFX_TABLE_BA	RW	32	0x0000 00B8	0x4804 10B8	0x5800 10B8
DISPC_VID1_BA_j (1)	RW	32	0x0000 00BC + (0x4 * j)	0x4804 10BC + (0x4 * j)	0x5800 10BC + (0x4 * j)
DISPC_VID1_POSITION	RW	32	0x0000 00C4	0x4804 10C4	0x5800 10C4
DISPC_VID1_SIZE	RW	32	0x0000 00C8	0x4804 10C8	0x5800 10C8
DISPC_VID1_ATTRIBUTES	RW	32	0x0000 00CC	0x4804 10CC	0x5800 10CC
DISPC_VID1_BUF_THRESHOLD	RW	32	0x0000 00D0	0x4804 10D0	0x5800 10D0
DISPC_VID1_BUF_SIZE_STATUS	R	32	0x0000 00D4	0x4804 10D4	0x5800 10D4
DISPC_VID1_ROW_INC	RW	32	0x0000 00D8	0x4804 10D8	0x5800 10D8
DISPC_VID1_PIXEL_INC	RW	32	0x0000 00DC	0x4804 10DC	0x5800 10DC
DISPC_VID1_FIR	RW	32	0x0000 00E0	0x4804 10E0	0x5800 10E0
DISPC_VID1_PICTURE_SIZE	RW	32	0x0000 00E4	0x4804 10E4	0x5800 10E4
DISPC_VID1_ACCU_j (1)	RW	32	0x0000 00E8 + (0x4 * j)	0x4804 10E8 + (0x4 * j)	0x5800 10E8 + (0x4 * j)
DISPC_VID1_FIR_COEF_H_i (2)	RW	32	0x0000 00F0 + (0x8 * i)	0x4804 10F0 + (0x8 * i)	0x5800 10F0 + (0x8 * i)
DISPC_VID1_FIR_COEF_HV_i (2)	RW	32	0x0000 00F4 + (0x8 * i)	0x4804 10F4 + (0x8 * i)	0x5800 10F4 + (0x8 * i)
DISPC_VID1_CONV_COEF0	RW	32	0x0000 0130	0x4804 1130	0x5800 1130

(1) j = 0 to 1
(2) i = 0 to 7

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Table 10-134. Display Controller Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	DISPC L4_PER Physical Address	DISPC L3 Physical Address
DISPC_VID1_CONV_COEF1	RW	32	0x0000 0134	0x4804 1134	0x5800 1134
DISPC_VID1_CONV_COEF2	RW	32	0x0000 0138	0x4804 1138	0x5800 1138
DISPC_VID1_CONV_COEF3	RW	32	0x0000 013C	0x4804 113C	0x5800 113C
DISPC_VID1_CONV_COEF4	RW	32	0x0000 0140	0x4804 1140	0x5800 1140
DISPC_VID2_BA_j (1)	RW	32	0x0000 014C + (0x4 * j)	0x4804 114C + (0x4 * j)	0x5800 114C + (0x4 * j)
DISPC_VID2_POSITION	RW	32	0x0000 0154	0x4804 1154	0x5800 1154
DISPC_VID2_SIZE	RW	32	0x0000 0158	0x4804 1158	0x5800 1158
DISPC_VID2_ATTRIBUTES	RW	32	0x0000 015C	0x4804 115C	0x5800 115C
DISPC_VID2_BUF_THRESHOLD	RW	32	0x0000 0160	0x4804 1160	0x5800 1160
DISPC_VID2_BUF_SIZE_STATUS	R	32	0x0000 0164	0x4804 1164	0x5800 1164
DISPC_VID2_ROW_INC	RW	32	0x0000 0168	0x4804 1168	0x5800 1168
DISPC_VID2_PIXEL_INC	RW	32	0x0000 016C	0x4804 116C	0x5800 116C
DISPC_VID2_FIR	RW	32	0x0000 0170	0x4804 1170	0x5800 1170
DISPC_VID2_PICTURE_SIZE	RW	32	0x0000 0174	0x4804 1174	0x5800 1174
DISPC_VID2_ACCU_j (1)	RW	32	0x0000 0178 + (0x4 * j)	0x4804 1178 + (0x4 * j)	0x5800 1178 + (0x4 * j)
DISPC_VID2_FIR_COEF_H_i (3)	RW	32	0x0000 0180 + (0x8 * i)	0x4804 1180 + (0x8 * i)	0x5800 1180 + (0x8 * i)
DISPC_VID2_FIR_COEF_HV_i (3)	RW	32	0x0000 0184 + (0x8 * i)	0x4804 1184 + (0x8 * i)	0x5800 1184 + (0x8 * i)
DISPC_VID2_CONV_COEF0	RW	32	0x0000 01C0	0x4804 11C0	0x5800 11C0
DISPC_VID2_CONV_COEF1	RW	32	0x0000 01C4	0x4804 11C4	0x5800 11C4
DISPC_VID2_CONV_COEF2	RW	32	0x0000 01C8	0x4804 11C8	0x5800 11C8
DISPC_VID2_CONV_COEF3	RW	32	0x0000 01CC	0x4804 11CC	0x5800 11CC
DISPC_VID2_CONV_COEF4	RW	32	0x0000 01D0	0x4804 11D0	0x5800 11D0
DISPC_DATA1_CYCLE1	RW	32	0x0000 01D4	0x4804 11D4	0x5800 11D4
DISPC_DATA1_CYCLE2	RW	32	0x0000 01D8	0x4804 11D8	0x5800 11D8
DISPC_DATA1_CYCLE3	RW	32	0x0000 01DC	0x4804 11DC	0x5800 11DC
DISPC_VID1_FIR_COEF_V_i (3)	RW	32	0x0000 01E0 + (0x4 * i)	0x4804 11E0 + (0x4 * i)	0x5800 11E0 + (0x4 * i)
DISPC_VID2_FIR_COEF_V_i (3)	RW	32	0x0000 0200 + (0x4 * i)	0x4804 1200 + (0x4 * i)	0x5800 1200 + (0x4 * i)
DISPC_CPR1_COEF_R	RW	32	0x0000 0220	0x4804 1220	0x5800 1220
DISPC_CPR1_COEF_G	RW	32	0x0000 0224	0x4804 1224	0x5800 1224
DISPC_CPR1_COEF_B	RW	32	0x0000 0228	0x4804 1228	0x5800 1228
DISPC_GFX_PRELOAD	RW	32	0x0000 022C	0x4804 122C	0x5800 122C
DISPC_VID1_PRELOAD	RW	32	0x0000 0230	0x4804 1230	0x5800 1230
DISPC_VID2_PRELOAD	RW	32	0x0000 0234	0x4804 1234	0x5800 1234
DISPC_CONTROL2	RW	32	0x0000 0238	0x4804 1238	0x5800 1238
DISPC_VID3_ACCU_j (4)	RW	32	0x0000 0300 + (0x4 * j)	0x4804 1300 + (0x4 * j)	0x5800 1300 + (0x4 * j)
DISPC_VID3_BA_j (4)	RW	32	0x0000 0308 + (0x4 * j)	0x4804 1308 + (0x4 * j)	0x5800 1308 + (0x4 * j)
DISPC_VID3_FIR_COEF_H_i (3)	RW	32	0x0000 0310 + (0x8 * i)	0x4804 1310 + (0x8 * i)	0x5800 1310 + (0x8 * i)
DISPC_VID3_FIR_COEF_HV_i (3)	RW	32	0x0000 0314 + (0x8 * i)	0x4804 1314 + (0x8 * i)	0x5800 1314 + (0x8 * i)

(3) i = 0 to 7

(4) j = 0 to 1

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Table 10-134. Display Controller Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	DISPC L4_PER Physical Address	DISPC L3 Physical Address
DISPC_VID3_FIR_COEF_V_i [3]	RW	32	0x0000 0350 + (0x4 * i)	0x4804 1350 + (0x4 * i)	0x5800 1350 + (0x4 * i)
DISPC_VID3_ATTRIBUTES	RW	32	0x0000 0370	0x4804 1370	0x5800 1370
DISPC_VID3_CONV_COEF0	RW	32	0x0000 0374	0x4804 1374	0x5800 1374
DISPC_VID3_CONV_COEF1	RW	32	0x0000 0378	0x4804 1378	0x5800 1378
DISPC_VID3_CONV_COEF2	RW	32	0x0000 037C	0x4804 137C	0x5800 137C
DISPC_VID3_CONV_COEF3	RW	32	0x0000 0380	0x4804 1380	0x5800 1380
DISPC_VID3_CONV_COEF4	RW	32	0x0000 0384	0x4804 1384	0x5800 1384
DISPC_VID3_BUF_SIZE_STATUS	R	32	0x0000 0388	0x4804 1388	0x5800 1388
DISPC_VID3_BUF_THRESHOLD	RW	32	0x0000 038C	0x4804 138C	0x5800 138C
DISPC_VID3_FIR	RW	32	0x0000 0390	0x4804 1390	0x5800 1390
DISPC_VID3_PICTURE_SIZE	RW	32	0x0000 0394	0x4804 1394	0x5800 1394
DISPC_VID3_PIXEL_INC	RW	32	0x0000 0398	0x4804 1398	0x5800 1398
DISPC_VID3_POSITION	RW	32	0x0000 039C	0x4804 139C	0x5800 139C
DISPC_VID3_PRELOAD	RW	32	0x0000 03A0	0x4804 13A0	0x5800 13A0
DISPC_VID3_ROW_INC	RW	32	0x0000 03A4	0x4804 13A4	0x5800 13A4
DISPC_VID3_SIZE	RW	32	0x0000 03A8	0x4804 13A8	0x5800 13A8
DISPC_DEFAULT_COLOR2	RW	32	0x0000 03AC	0x4804 13AC	0x5800 13AC
DISPC_TRANS_COLOR2	RW	32	0x0000 03B0	0x4804 13B0	0x5800 13B0
DISPC_CPR2_COEF_B	RW	32	0x0000 03B4	0x4804 13B4	0x5800 13B4
DISPC_CPR2_COEF_G	RW	32	0x0000 03B8	0x4804 13B8	0x5800 13B8
DISPC_CPR2_COEF_R	RW	32	0x0000 03BC	0x4804 13BC	0x5800 13BC
DISPC_DATA2_CYCLE1	RW	32	0x0000 03C0	0x4804 13C0	0x5800 13C0
DISPC_DATA2_CYCLE2	RW	32	0x0000 03C4	0x4804 13C4	0x5800 13C4
DISPC_DATA2_CYCLE3	RW	32	0x0000 03C8	0x4804 13C8	0x5800 13C8
DISPC_SIZE_LCD2	RW	32	0x0000 03CC	0x4804 13CC	0x5800 13CC
DISPC_TIMING_H2	RW	32	0x0000 0400	0x4804 1400	0x5800 1400
DISPC_TIMING_V2	RW	32	0x0000 0404	0x4804 1404	0x5800 1404
DISPC_POL_FREQ2	RW	32	0x0000 0408	0x4804 1408	0x5800 1408
DISPC_DIVISOR2	RW	32	0x0000 040C	0x4804 140C	0x5800 140C
DISPC_WB_ACCU_j [5]	RW	32	0x0000 0500 + (0x4 * j)	0x4804 1500 + (0x4 * j)	0x5800 1500 + (0x4 * j)
DISPC_WB_BA_j [5]	RW	32	0x0000 0508 + (0x4 * j)	0x4804 1508 + (0x4 * j)	0x5800 1508 + (0x4 * j)
DISPC_WB_FIR_COEF_H_i [6]	RW	32	0x0000 0510 + (0x8 * i)	0x4804 1510 + (0x8 * i)	0x5800 1510 + (0x8 * i)
DISPC_WB_FIR_COEF_HV_i [6]	RW	32	0x0000 0514 + (0x8 * i)	0x4804 1514 + (0x8 * i)	0x5800 1514 + (0x8 * i)
DISPC_WB_FIR_COEF_V_i [6]	RW	32	0x0000 0550 + (0x4 * i)	0x4804 1550 + (0x4 * i)	0x5800 1550 + (0x4 * i)
DISPC_WB_ATTRIBUTES	RW	32	0x0000 0570	0x4804 1570	0x5800 1570
DISPC_WB_CONV_COEF0	RW	32	0x0000 0574	0x4804 1574	0x5800 1574
DISPC_WB_CONV_COEF1	RW	32	0x0000 0578	0x4804 1578	0x5800 1578
DISPC_WB_CONV_COEF2	RW	32	0x0000 057C	0x4804 157C	0x5800 157C
DISPC_WB_CONV_COEF3	RW	32	0x0000 0580	0x4804 1580	0x5800 1580
DISPC_WB_CONV_COEF4	RW	32	0x0000 0584	0x4804 1584	0x5800 1584

(5) j = 0 to 1
(6) i = 0 to 7

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Table 10-134. Display Controller Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	DISPC L4_PER Physical Address	DISPC L3 Physical Address
DISPC_WB_BUF_SIZE_STATUS	R	32	0x0000 0588	0x4804 1588	0x5800 1588
DISPC_WB_BUF_THRESHOLD	RW	32	0x0000 058C	0x4804 158C	0x5800 158C
DISPC_WB_FIR	RW	32	0x0000 0590	0x4804 1590	0x5800 1590
DISPC_WB_PICTURE_SIZE	RW	32	0x0000 0594	0x4804 1594	0x5800 1594
DISPC_WB_PIXEL_INC	RW	32	0x0000 0598	0x4804 1598	0x5800 1598
DISPC_WB_ROW_INC	RW	32	0x0000 05A4	0x4804 15A4	0x5800 15A4
DISPC_WB_SIZE	RW	32	0x0000 05A8	0x4804 15A8	0x5800 15A8
DISPC_VID1_BA_UV_j [5]	RW	32	0x0000 0600 + (0x4 * j)	0x4804 1600 + (0x4 * j)	0x5800 1600 + (0x4 * j)
DISPC_VID2_BA_UV_j [5]	RW	32	0x0000 0608 + (0x4 * j)	0x4804 1608 + (0x4 * j)	0x5800 1608 + (0x4 * j)
DISPC_VID3_BA_UV_j [5]	RW	32	0x0000 0610 + (0x4 * j)	0x4804 1610 + (0x4 * j)	0x5800 1610 + (0x4 * j)
DISPC_WB_BA_UV_j [5]	RW	32	0x0000 0618 + (0x4 * j)	0x4804 1618 + (0x4 * j)	0x5800 1618 + (0x4 * j)
DISPC_CONFIG2	RW	32	0x0000 0620	0x4804 1620	0x5800 1620
DISPC_VID1_ATTRIBUTES2	RW	32	0x0000 0624	0x4804 1624	0x5800 1624
DISPC_VID2_ATTRIBUTES2	RW	32	0x0000 0628	0x4804 1628	0x5800 1628
DISPC_VID3_ATTRIBUTES2	RW	32	0x0000 062C	0x4804 162C	0x5800 162C
DISPC_GAMMA_TABLE0	W	32	0x0000 0630	0x4804 1630	0x5800 1630
DISPC_GAMMA_TABLE1	W	32	0x0000 0634	0x4804 1634	0x5800 1634
DISPC_GAMMA_TABLE2	W	32	0x0000 0638	0x4804 1638	0x5800 1638
DISPC_VID1_FIR2	RW	32	0x0000 063C	0x4804 163C	0x5800 163C
DISPC_VID1_ACCU2_j [7]	RW	32	0x0000 0640 + (0x4 * j)	0x4804 1640 + (0x4 * j)	0x5800 1640 + (0x4 * j)
DISPC_VID1_FIR_COEF_H2_i [8]	RW	32	0x0000 0648 + (0x8 * i)	0x4804 1648 + (0x8 * i)	0x5800 1648 + (0x8 * i)
DISPC_VID1_FIR_COEF_HV2_i [8]	RW	32	0x0000 064C + (0x8 * i)	0x4804 164C + (0x8 * i)	0x5800 164C + (0x8 * i)
DISPC_VID1_FIR_COEF_V2_i [8]	RW	32	0x0000 0688 + (0x4 * i)	0x4804 1688 + (0x4 * i)	0x5800 1688 + (0x4 * i)
DISPC_VID2_FIR2	RW	32	0x0000 06A8	0x4804 16A8	0x5800 16A8
DISPC_VID2_ACCU2_j [7]	RW	32	0x0000 06AC + (0x4 * j)	0x4804 16AC + (0x4 * j)	0x5800 16AC + (0x4 * j)
DISPC_VID2_FIR_COEF_H2_i [8]	RW	32	0x0000 06B4 + (0x8 * i)	0x4804 16B4 + (0x8 * i)	0x5800 16B4 + (0x8 * i)
DISPC_VID2_FIR_COEF_HV2_i [8]	RW	32	0x0000 06B8 + (0x8 * i)	0x4804 16B8 + (0x8 * i)	0x5800 16B8 + (0x8 * i)
DISPC_VID2_FIR_COEF_V2_i [8]	RW	32	0x0000 06F4 + (0x4 * i)	0x4804 16F4 + (0x4 * i)	0x5800 16F4 + (0x4 * i)
DISPC_VID3_FIR2	RW	32	0x0000 0724	0x4804 1724	0x5800 1724
DISPC_VID3_ACCU2_j [7]	RW	32	0x0000 0728 + (0x4 * j)	0x4804 1728 + (0x4 * j)	0x5800 1728 + (0x4 * j)
DISPC_VID3_FIR_COEF_H2_i [8]	RW	32	0x0000 0730 + (0x8 * i)	0x4804 1730 + (0x8 * i)	0x5800 1730 + (0x8 * i)
DISPC_VID3_FIR_COEF_HV2_i [8]	RW	32	0x0000 0734 + (0x8 * i)	0x4804 1734 + (0x8 * i)	0x5800 1734 + (0x8 * i)
DISPC_VID3_FIR_COEF_V2_i [8]	RW	32	0x0000 0770 + (0x4 * i)	0x4804 1770 + (0x4 * i)	0x5800 1770 + (0x4 * i)

[7] j = 0 to 1
[8] i = 0 to 7

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Table 10-134. Display Controller Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	DISPC L4_PER Physical Address	DISPC L3 Physical Address
DISPC_WB_FIR2	RW	32	0x0000 0790	0x4804 1790	0x5800 1790
DISPC_WB_ACCU2_j [7]	RW	32	0x0000 0794 + (0x4 * j)	0x4804 1794 + (0x4 * j)	0x5800 1794 + (0x4 * j)
DISPC_WB_FIR_COEF_H2_i [8]	RW	32	0x0000 07A0 + (0x8 * i)	0x4804 17A0 + (0x8 * i)	0x5800 17A0 + (0x8 * i)
DISPC_WB_FIR_COEF_HV2_i [8]	RW	32	0x0000 07A4 + (0x8 * i)	0x4804 17A4 + (0x8 * i)	0x5800 17A4 + (0x8 * i)
DISPC_WB_FIR_COEF_V2_i [8]	RW	32	0x0000 07E0 + (0x4 * i)	0x4804 17E0 + (0x4 * i)	0x5800 17E0 + (0x4 * i)
DISPC_GLOBAL_BUFFER	RW	32	0x0000 0800	0x4804 1800	0x5800 1800
DISPC_DIVISOR	RW	32	0x0000 0804	0x4804 1804	0x5800 1804
DISPC_WB_ATTRIBUTES2	RW	32	0x0000 0810	0x4804 1810	0x5800 1810

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10.2.7.3.2 Display Controller Register Description

Table 10-135. DISPC_REVISION

Address Offset	0x0000 0000		
Physical Address	0x4804 1000 0x5800 1000	**Instance**	DISPC_PER_L4 DISPC_L3
Description	IP Revision		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REV																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP revision	R	See(1)

(1) TI internal data

Table 10-136. Register Call Summary for Register DISPC_REVISION

Display Controller

- Shadow Registers: [0]
- Display Controller Register Summary: [1]

Table 10-137. DISPC_SYSCONFIG

Address Offset	0x0000 0010		
Physical Address	0x4804 1010 0x5800 1010	**Instance**	DISPC_PER_L4 DISPC_L3
Description	This register allows to control various parameters of the OCP interface.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																		MIDLEMODE		RESERVED		CLOCKACTIVITY		RESERVED		WARMRESET		SIDLEMODE		ENWAKEUP		SOFTRESET		AUTOIDLE	

Bits	Field Name	Description	Type	Reset
31:14	RESERVED	Write 0s for future compatibility. Reads returns 0	R	0x00000
13:12	MIDLEMODE	Master interface power management, standby/wait control 0x0: Force-standby. MStandby is only asserted when the module is disabled. MStandby is only asserted when the module is disabled. 0x1: No-Standby: MStandby is never asserted. 0x2: Smart-Standby. MStandby is asserted based on the internal activity of the module 0x3: Reserved	RW	0x0
11:10	RESERVED	Write 0s for future compatibility. Reads returns 0	R	0x0

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Bits	Field Name	Description	Type	Reset
9:8	CLOCKACTIVITY	Clocks activity during wake up mode period 0x0: OCP and Functional clocks can be switched off 0x1: Functional clocks can be switched off and OCP clocks are maintained during wake up period 0x2: OCP clocks can be switched off and Functional clocks are maintained during wake up period 0x3: OCP and Functional clocks are maintained during wake up period	RW	0x0
7:6	RESERVED	Write 0s for future compatibility. Reads returns 0	R	0x0
5	WARMRESET	Warm reset. Set this bit to 1 triggers a module warm reset. The bit is automatically reset by the hardware. During reads, it always returns 0. The warm reset keep the configuration registers unchanged. 0x0: Normal mode 0x1: the warmreset is set	RW	0
4:3	SIDLEMODE	Slave interface power management, Idle req/ack control 0x0: Force-idle. An idle request is acknowledged unconditionally 0x1: No-idle. An idle request is never acknowledged 0x2: Smart-idle. Acknowledgment to an idle request is given based on the internal activity of the module. 0x3: Reserved	RW	0x0
2	ENWAKEUP	WakeUp feature control 0x0: Wakeup is disabled 0x1: Wakeup is enabled	RW	0
1	SOFTRESET	Software reset. Set this bit to 1 to trigger a module reset. The bit is automatically reset by the hardware. During reads, it always returns 0. 0x0: Normal mode 0x1: The module is reset	RW	0
0	AUTOIDLE	Internal OCP clock gating strategy 0x0: OCP clock is free-running 0x1: Automatic OCP L3 and L4 clocks gating strategy is applied, based on the OCP interface activity. Automatic functional clock gating is also applied to the functional clock based on the module activity (for instance DISPC_pipe_ATTRIBUTES.ENABLE)	RW	1

Table 10-138. Register Call Summary for Register DISPC_SYSCONFIG

Display Controller

- Software Reset: [0] [1]
- Idle Mode: [2]
- StandBy Mode: [3]
- Wakeup: [4]
- DMA Power Modes: [5]
- Shadow Registers: [6]
- Display Controller Register Summary: [7]

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Table 10-139. DISPC_SYSSTATUS

Address Offset	0x0000 0014		
Physical Address	0x4804 1014 0x5800 1014	**Instance**	DISPC_PER_L4 DISPC_L3
Description	This register provides status information about the module, excluding the interrupt status information.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RESERVED							RESETDONE

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x000000
0	RESETDONE	Internal reset monitoring Read 0x0: Internal module reset is on-going Read 0x1: Reset completed	R	1

Table 10-140. Register Call Summary for Register DISPC_SYSSTATUS

Display Controller
- Software Reset: [0]
- Shadow Registers: [1]
- Display Controller Register Summary: [2]

Table 10-141. DISPC_IRQSTATUS

Address Offset	0x0000 0018		
Physical Address	0x4804 1018 0x5800 1018	**Instance**	DISPC_PER_L4 DISPC_L3
Description	This register regroups all the status of the module internal events that generate an interrupt. Write 1 to a given bit resets this bit		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						WBBUFFEROVERFLOW_IRQ	FRAMEDONETV_IRQ	FRAMEDONEWB_IRQ	FRAMEDONE2_IRQ	ACBIASCOUNTSTATUS2_IRQ	VID3BUFFERUNDERFLOW_IRQ	VID3ENDWINDOW_IRQ	VSYNC2_IRQ	SYNCLOST2_IRQ	WAKEUP_IRQ	SYNCLOSTTV_IRQ	SYNCLOST1_IRQ	VID2ENDWINDOW_IRQ	VID2BUFFERUNDERFLOW_IRQ	VID1ENDWINDOW_IRQ	VID1BUFFERUNDERFLOW_IRQ	OCPERROR_IRQ	PALETTEGAMMALOADING_IRQ	GFXENDWINDOW_IRQ	GFXBUFFERUNDERFLOW_IRQ	PROGRAMMEDLINENUMBER_IRQ	ACBIASCOUNTSTATUS1_IRQ	EVSYNC_ODD_IRQ	EVSYNC_EVEN_IRQ	VSYNC1_IRQ	FRAMEDONE1_IRQ

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Bits	Field Name	Description	Type	Reset
31:26	RESERVED	Write 0s for future compatibility. Reads returns 0	R	0x00
25	WBBUFFER OVERFLOW_IRQ	Write-back DMA Buffer Overflow. The DMA buffer is full. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
24	FRAME DONETV_IRQ	Frame Done for the TV. The TV output has been disabled by user. All the data have been sent. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
23	FRAME DONEWB_IRQ	Frame Done for the write-back channel. The write-back channel has output the frame. All the data of the frame have been sent to the memory. There is no pending data inside the DMA engine for the write-back channel to be transferred to memory. It is available only when the write-back pipeline transfers back to memory the output of one of the pipelines. In case of overlay capture, the interrupt is not generated and the user shall use the FrameDone for the corresponding captured output. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
22	FRAME DONE2_IRQ	Frame Done for the secondary LCD. The secondary LCD output has been disabled by user. All the data have been sent. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
21	ACBIASCOUNT STATUS2_IRQ	AC Bias Count Status for the secondary LCD 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
20	VID3BUFFER UNDERFLOW_IRQ	Video 3 DMA Buffer Underflow. The DMA buffer is not necessarily empty but required data are not present in the DMA buffer (due to out of order responses) 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
19	VID3END WINDOW_IRQ	The end of the video 3 Window has been reached. It is detected by the overlay manager when the full video 3 has been displayed. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
18	VSYNC2_IRQ	Vertical Synchronization for the secondary LCD 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
17	SYNC LOST2_IRQ	Synchronization Lost on the secondary LCD output. The required data are not output at the correct time due to too short blanking periods or stall of at least one pipelines associated with the secondary LCD output. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
16	WAKEUP_IRQ	Wake-up 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
15	SYNCLOST TV_IRQ	Synchronization Lost on the TV output. The required data are not output at the correct time due to too short blanking periods or stall of at least one pipelines associated with the TV output. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
14	SYNC LOST1_IRQ	Synchronization Lost on the primary LCD output. The required data are not output at the correct time due to too short blanking periods or stall of at least one pipelines associated with the primary LCD output. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
13	VID2END WINDOW_IRQ	The end of the video 2 Window has been reached. It is detected by the overlay manager when the full video 2 has been displayed. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
12	VID2BUFFER UNDERFLOW_IRQ	Video 2 DMA Buffer Underflow. The DMA buffer is not necessarily empty but required data are not present in the DMA buffer (due to out of order responses) 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
11	VID1END WINDOW_IRQ	The end of the video 1 Window has been reached. It is detected by the overlay manager when the full video 1 has been displayed. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
10	VID1BUFFER UNDERFLOW_IRQ	Video 1 DMA Buffer Underflow. The DMA buffer is not necessarily empty but required data are not present in the DMA buffer (due to out of order responses) 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
9	OCPERROR_IRQ	OCP Error. L3 Interconnect has sent SResp=ERR. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
8	PALETTEGAMMA LOADING_IRQ	Palette Gamma Loading status. The palette used as Color Look Up Table (CLUT) for the graphics BITMAP formats (1-, 2-, 4-, or 4-bpp) or as gamma table for the overlay output for the primary LCD output has been loaded successfully. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
7	GFXEND WINDOW_IRQ	The end of the graphics Window has been reached. It is detected by the overlay manager when the full graphics has been displayed. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
6	GFXBUFFER UNDERFLOW_IRQ	Graphics DMA Buffer Underflow. The DMA buffer is not necessarily empty but required data are not present in the DMA buffer (due to out of order responses) 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
5	PROGRAMMED LINENUMBER_IRQ	Programmed Line Number. It indicates that the scan of the primary LCD has reached the programmed user line number. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
4	ACBIASCOUNT STATUS1_IRQ	AC Bias Count Status for the primary LCD 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
3	EVSYNC_ ODD_IRQ	VSYNC for odd field from the TV encoder (VENC or HDMI) 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
2	EVSYNC_ EVEN_IRQ	VSYNC for even field from the TV encoder (VENC or HDMI) 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
1	VSYNC1_IRQ	Vertical Synchronization for the primary LCD. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
0	FRAME DONE1_IRQ	Frame Done for the primary LCD. The primary LCD output has been disabled by user. All the data have been sent. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0

Table 10-142. Register Call Summary for Register DISPC_IRQSTATUS

Display Controller

- Interrupt Requests: [0]
- Synchronized Buffer Update: [1]
- Shadow Registers: [2]
- Display Controller Register Summary: [3]

Table 10-143. DISPC_IRQENABLE

Address Offset	0x0000 001C		
Physical Address	0x4804 101C 0x5800 101C	**Instance**	DISPC_PER_L4 DISPC_L3
Description	This register allows to mask/unmask the module internal sources of interrupt, on an event-by-event basis		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						WBBUFFEROVERFLOW_EN	FRAMEDONETV_EN	FRAMEDONEWB_EN	FRAMEDONE2_EN	ACBIASCOUNTSTATUS2_EN	VID3BUFFERUNDERFLOW_EN	VID3ENDWINDOW_EN	VSYNC2_EN	SYNCLOST2_EN	WAKEUP_EN	SYNCLOSTTV_EN	SYNCLOST1_EN	VID2ENDWINDOW_EN	VID2BUFFERUNDERFLOW_EN	ENDVID1WINDOW_EN	VID1BUFFERUNDERFLOW_EN	OCPERROR_EN	PALETTEGAMMA_EN	GFXENDWINDOW_EN	GFXBUFFERUNDERFLOW_EN	PROGRAMMEDLINENUMBER_EN	ACBIASCOUNTSTATUS1_EN	EVSYNC_ODD_EN	EVSYNC_EVEN_EN	VSYNC1_EN	FRAMEDONE_EN

Bits	Field Name	Description	Type	Reset
31:26	RESERVED	Write 0s for future compatibility. Reads returns 0	R	0x00
25	WBBUFFER OVERFLOW_EN	Write-back DMA Buffer Overflow. The DMA buffer is full 0x0: WBBufferOverflow is masked 0x1: WBBufferOverflow generates an interrupt when it occurs	RW	0
24	FRAME DONETV_EN	Frame Done for the TV. The TV output has been disabled by user. All the data have been sent. 0x0: Frame Done for the TV output is masked 0x1: Frame Done for the TV output generates an interrupt when it occurs	RW	0
23	FRAME DONEWB_EN	Frame Done for the write-back channel. The write-back channel has output the frame. All the data have been sent for the frame have been sent to the memory. There is no pending data inside the DMA engine for the write-back channel to be transferred to memory. 0x0: Frame Done for the write-back is masked 0x1: Frame Done for the write-back generates an interrupt when it occurs	RW	0

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Bits	Field Name	Description	Type	Reset
22	FRAME DONE2_EN	Frame Done for the secondary LCD. The secondary LCD output has been disabled by user. All the data have been sent. 0x0: Frame Done for the secondary LCD is masked 0x1: Frame Done for the secondary LCD generates an interrupt when it occurs	RW	0
21	ACBIASCOUNT STATUS2_EN	AC Bias Count Status for the secondary LCD 0x0: ACBiasCountStatus for the secondary LCD output is masked 0x1: ACBiasCountStatus for the secondary LCD output generates an interrupt when it occurs	RW	0
20	VID3BUFFER UNDERFLOW_EN	Video 3 DMA Buffer Underflow. The DMA buffer is not necessary empty but required data are not present in the DMA buffer (due to out of order responses) 0x0: Vid3BufferUnderflow is masked 0x1: Vid3BufferUnderflow generates an interrupt when it occurs	RW	0
19	VID3END WINDOW_EN	The end of the video 3 Window has been reached. It is detected by the overlay manager when the full video 3 has been displayed. 0x0: Vid3EndWindow is masked 0x1: Vid3EndWindow generates an interrupt when it occurs	RW	0
18	VSYNC2_EN	Vertical Synchronization for the secondary LCD 0x0: VSYNC for the secondary LCD output is masked 0x1: VSYNC for the secondary LCD output generates an interrupt when it occurs	RW	0
17	SYNC LOST2_EN	Synchronization Lost on the secondary LCD output. The required data are not output at the correct time due to too short blanking periods or stall of at least one pipelines associated with the secondary LCD output. 0x0: Synchronization Lost on the secondary LCD output is masked 0x1: Synchronization Lost on the secondary LCD output generates an interrupt when it occurs	RW	0
16	WAKEUP_EN	Wake Up Mask 0x0: WakeUp is masked 0x1: WakeUp generates an interrupt when it occurs	RW	0
15	SYNC LOSTTV_EN	Synchronization Lost on the TV output. The required data are not output at the correct time due to too short blanking periods or stall of at least one pipelines associated with the TV output. 0x0: Synchronization Lost on the TV output is masked 0x1: Synchronization Lost on the TV output generates an interrupt when it occurs	RW	0
14	SYNC LOST1_EN	Synchronization Lost for the primary LCD 0x0: SyncLost for the primary LCD output is masked 0x1: SyncLost for the primary LCD output generates an interrupt when it occurs	RW	0
13	VID2END WINDOW_EN	The end of the video 2 Window has been reached. It is detected by the overlay manager when the full video 2 has been displayed. 0x0: Vid2EndWindow is masked 0x1: Vid2EndWindow generates an interrupt when it occurs	RW	0
12	VID2BUFFER UNDERFLOW_EN	Video 2 DMA Buffer Underflow. The DMA buffer is not necessary empty but required data are not present in the DMA buffer (due to out of order responses) 0x0: Vid2BufferUnderflow is masked 0x1: Vid2BufferUnderflow generates an interrupt when it occurs	RW	0
11	ENDVID1 WINDOW_EN	The end of the video 1 Window has been reached. It is detected by the overlay manager when the full video 1 has been displayed. 0x0: EndVid1Window is masked 0x1: EndVid1Window generates an interrupt when it occurs	RW	0

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Bits	Field Name	Description	Type	Reset
10	VID1BUFFER UNDERFLOW_EN	Video 1 DMA Buffer Underflow. The DMA buffer is not necessary empty but required data are not present in the DMA buffer (due to out of order responses) 0x0: Vid1BufferUnderflow is masked 0x1: Vid1BufferUnderflow generates an interrupt when it occurs	RW	0
9	OCPERROR_EN	OCP Error. L3 Interconnect has sent SResp=ERR. 0x0: OCPError is masked 0x1: OCPError generates an interrupt when it occurs	RW	0
8	PALETTE GAMMA_EN	Palette Gamma Loading mask. The palette used as Color Look Up Table (CLUT) for the graphics BITMAP formats (1-, 2-, 4-, or 4-bpp) or as gamma table for the overlay output for the primary LCD output has been loaded successfully. 0x0: PaletteGamma is masked 0x1: PaletteGamma generates an interrupt when it occurs	RW	0
7	GFXEND WINDOW_EN	The end of the graphics Window has been reached. It is detected by the overlay manager when the full graphics has been displayed. 0x0: GfxEndWindow is masked 0x1: GfxEndWindow generates an interrupt when it occurs	RW	0
6	GFXBUFFER UNDERFLOW_EN	Graphics DMA Buffer Underflow. The DMA buffer is not necessarily empty but required data are not present in the DMA buffer (due to out of order responses) 0x0: GfxBufferUnderflow is masked 0x1: GfxBufferUnderflow generates an interrupt when it occurs	RW	0
5	PROGRAMMED LINENUMBER_EN	Programmed Line Number. It indicates that the scan of the primary LCD has reached the programmed user line number. 0x0: ProgrammedLineNumber is masked 0x1: ProgrammedLineNumber generates an interrupt when it occurs	RW	0
4	ACBIASCOUNT STATUS1_EN	AC Bias Count Status for the primary LCD 0x0: ACBiasCountStatus for the primary LCD output is masked 0x1: ACBiasCountStatus for the primary LCD output generates an interrupt when it occurs	RW	0
3	EVSYNC_ODD_EN	VSYNC for odd field from the TV encoder (VENC or HDMI) 0x0: EVSYNC_ODD for the TV output is masked 0x1: EVSYNC_ODD for the TV output generates an interrupt when it occurs	RW	0
2	EVSYNC_EVEN_EN	VSYNC for even field from the TV encoder (VENC or HDMI) 0x0: EVSYNC_EVEN for the TV output is masked 0x1: EVSYNC_EVEN for the TV output generates an interrupt when it occurs	RW	0
1	VSYNC1_EN	Vertical Synchronization for the primary LCD. 0x0: VSYNC for the primary LCD output is masked 0x1: VSYNC for the primary LCD output generates an interrupt when it occurs	RW	0
0	FRAMEDONE_EN	Frame Done for the primary LCD. The primary LCD output has been disabled by user. All the data have been sent. 0x0: FrameDone for the primary LCD output is masked 0x1: FrameDone for the primary LCD output generates an interrupt when it occurs	RW	0

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Table 10-144. Register Call Summary for Register DISPC_IRQENABLE

Display Controller

- Interrupt Requests: [0]
- Synchronized Buffer Update: [1]
- Shadow Registers: [2]
- Display Controller Register Summary: [3]

Table 10-145. DISPC_CONTROL1

Address Offset	0x0000 0040		
Physical Address	0x4804 1040 0x5800 1040	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The control register configures the Display Controller module for the primary LCD and TV outputs.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPATIALTEMPORALDITHERINGFRAMES		LCDENABLEPOL	LCDENABLESIGNAL	PCKFREEENABLE	TDMUNUSEDBITS		TDMCYCLEFORMAT	TDMPARALLELMODE			TDMENABLE	HT			GPOUT1	GPOUT0	GPIN1	GPIN0	OVERLAYOPTIMIZATION	STALLMODE	RESERVED	TFTDATALINES		STDITHERENABLE	GOTV	GOLCD	M8B	STNTFT	MONOCOLOR	TVENABLE	LCDENABLE

Bits	Field Name	Description	Type	Reset
31:30	SPATIALTEMPORAL DITHERINGFRAMES	Spatial/Temporal dithering number of frames for the primary LCD output wr: VFP start period of primary LCD 0x0: Spatial only 0x1: Spatial and temporal over 2 frames 0x2: Spatial and temporal over 4 frames 0x3: Reserved	RW	0x0
29	LCDENABLEPOL	Write 0s for future compatibility. Reads return 0.	R	0
28	LCDENABLESIGNAL	Write 0s for future compatibility. Reads return 0.	R	0
27	PCKFREEENABLE	Write 0s for future compatibility. Reads return 0.	R	0
26:25	TDMUNUSEDBITS	State of unused bits (TDM mode only) for the primary LCD output. wr: VFP start period of primary LCD 0x0: low level (0) 0x1: high level (1) 0x2: unchanged from previous state 0x3: reserved	RW	0x0
24:23	TDMCYCLEFORMAT	Cycle format (TDM mode only) for the primary LCD output wr: VFP start period of primary LCD 0x0: 1 cycle for 1 pixel 0x1: 2 cycles for 1 pixel 0x2: 3 cycles for 1 pixel 0x3: 3 cycles for 2 pixels	RW	0x0

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Bits	Field Name	Description	Type	Reset
22:21	TDMPARALLELMODE	Output Interface width (TDM mode only) for the primary LCD output wr: VFP start period of primary LCD 0x0: 8-bit parallel output interface selected 0x1: 9-bit parallel output interface selected 0x2: 12-bit parallel output interface selected 0x3: 16-bit parallel output interface selected	RW	0x0
20	TDMENABLE	Enable the multiple cycle format (TDM mode only used for TFT mode with the RFBI enable bit off) for the primary LCD output. wr: VFP start period of primary LCD 0x0: TDM disabled 0x1: TDM enabled	RW	0
19:17	HT	Hold Time for TV output wr: EVSYNC Encoded value (from 1 to 8) to specify the number of external digital clock periods to hold the data (programmed value = value minus 1)	RW	0x0
16	GPOUT1	General Purpose Output Signal wr:immediate 0x0: The GPout1 is reset 0x1: The GPout1 is set	RW	0
15	GPOUT0	General Purpose Output Signal wr:immediate 0x0: The GPout0 is reset 0x1: The GPout0 is set	RW	0
14	GPIN1	General Purpose Input Signal wr: immediately Read 0x0: The GPin1 has been reset Read 0x1: The GPin1 has been set	R	0
13	GPIN0	General Purpose Input Signal wr: immediately Read 0x0: The GPin0 has been reset Read 0x1: The GPin0 has been set	R	0
12	OVERLAYOPTIMIZATION	Overlay Optimization for the primary LCD output wr: VFP start period of the primary LCD 0x0: All the data for all the enabled pipelines are fetched from memory regardless of the overlay/alpha blending configuration. 0x1: The data not used by the overlay manager because of overlap between layers with no alpha blending between them shall not be fetched from memory in order to optimize the bandwidth.	RW	0
11	STALLMODE	STALL Mode for the primary LCD output wr: VFP start period of primary LCD 0x0: Normal mode selected 0x1: STALL mode selected. The Display Controller sends the data without considering the VSYNC/HSYNC. The LCD output is disabled at the end of the transfer of the frame. The S/W has to re-enable the LCD output in order to generate a new frame. The stall mode is used in RFBI and DSI command modes.	RW	0
10	RESERVED	Reserved	R	0
9:8	TFTDATALINES	Number of lines of the primary LCD interface wr: VFP start period of primary LCD 0x0: 12-bit output aligned on the LSB of the pixel data interface 0x1: 16-bit output aligned on the LSB of the pixel data interface 0x2: 18-bit output aligned on the LSB of the pixel data interface 0x3: 24-bit output aligned on the LSB of the pixel data interface	RW	0x0
7	STDITHERENABLE	Spatial Temporal dithering enable for the primary LCD output wr: VFP start period of primary LCD 0x0: Spatial/Temporal dithering logic disabled 0x1: Spatial/Temporal dithering logic enabled	RW	0

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Bits	Field Name	Description	Type	Reset
6	GOTV	GO Command for the TV output. It is used to synchronized the pipelines (graphics and/or video ones) associated with the TV output. wr: immediate 0x0: The hardware has finished updating the internal shadow registers of the pipeline(s) associated with the TV output using the user values. The hardware resets the bit when the update is completed. 0x1: The user has finished to program the shadow registers of the pipeline(s) associated with the TV output and the hardware can update the internal registers at the external VSYNC.	RW	0
5	GOLCD	GO Command for the primary LCD output. It is used to synchronized the pipelines (graphics and/or video ones) associated with the primary LCD output. wr: immediate 0x0: The hardware has finished updating the internal shadow registers of the pipeline(s) connected to the LCD output using the user values. The hardware resets the bit when the update is completed. 0x1: The user has finished to program the shadow registers of the pipeline(s) associated with the LCD output and the hardware can update the internal registers at the VFP start period	RW	0
4	M8B	Mono 8-bit mode of the primary LCD wr: VFP start period of primary LCD output 0x0: Pixel data [3:0] is used to output four pixel values to the panel at each pixel clock transition. (only in Passive Mono 4-bit mode). 0x1: Pixel data [7:0] is used to output eight pixel values to the panel each pixel clock transition. (only in Passive Mono 8-bit mode).	RW	0
3	STNTFT	LCD Display type of the primary LCD wr: VFP start period of primary LCD output 0x0: Passive or STN display operation enabled. STN dither logic is enabled. 0x1: Active or TFT display operation enabled. STN Dither logic and output FIFO bypassed.	RW	0
2	MONOCOLOR	Monochrome/Color selection for the primary LCD wr: VFP start period of primary LCD output 0x0: Color operation enabled (STN mode only) 0x1: Monochrome operation enabled (STN mode only)	RW	0
1	TVENABLE	Enable the TV output wr: immediate effect only occurs at the end of the current frame. 0x0: TV output disabled (at the end of the current field if interlace output when the bit is reset) 0x1: TV output enabled	RW	0
0	LCDENABLE	Enable the primary LCD outputs wr: immediate Effect only occurs at the end of the current frame 0x0: LCD output disabled (at the end of the frame when the bit is reset) 0x1: LCD output enabled	RW	0

Table 10-146. Register Call Summary for Register DISPC_CONTROL1

Display Controller

- Overlay Manager: [0]
- Timing and TV Format Settings: [1]
- Shadow Registers: [2] [3] [4] [5]
- Operational Modes Configuration: [6] [7] [8] [9] [10] [11] [12] [13] [14]
- Display Controller Logical Register Mapping: [15]
- Display Controller Register Summary: [16]

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Table 10-147. DISPC_CONFIG1

Address Offset	0x0000 0044		
Physical Address	0x4804 1044 0x5800 1044	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The control register configures the Display Controller module for the primary LCD output and TV output. Shadow register, updated on VFP start period of primary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						FULLRANGE	COLORCONVENABLE	FIDFIRST	OUTPUTMODEENABLE	RESERVED		TVALPHABLENDERENABLE	LCDALPHABLENDERENABLE	BUFFERFILLING	BUFFERHANDCHECK	CPR	BUFFERMERGE	TCKTVSELECTION	TCKTVENABLE	TCKLCDSELECTION	TCKLCDENABLE	GAMATABLEENABLE	ACBIASGATED	VSYNCGATED	HSYNCGATED	PIXELCLOCKGATED	PIXELDATAGATED	PALETTEGAMMATABLE	LOADMODE	PIXELGATED	

Bits	Field Name	Description	Type	Reset
31:26	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
25	FULLRANGE	Color Space Conversion full range setting. wr: VFP start of primary LCD 0x0: Limited range selected. 0x1: Full range selected.	RW	0
24	COLORCONV ENABLE	Enable the color space conversion. It shall be reset when CPR bit field is set to 0x1. wr: VFP start of primary LCD 0x0: Disable Color Space Conversion RGB to YUV 0x1: Enable Color Space Conversion RGB to YUV	RW	0
23	FIDFIRST	Selects the first field to output in case of interlace mode. In case of progressive mode, the value is not used. wr: VFP start of primary LCD 0x0: First field is even. 0x1: Odd field is first.	RW	0
22	OUTPUTMODE ENABLE	Selects between progressive and interlace mode for the primary LCD output. wr: VFP start of primary LCD 0x0: Progressive mode selected. 0x1: Interlace mode selected.	RW	0
21:20	RESERVED	Write 0s for future compatibility. Reads return 0.	RW	0
19	TVALPHABLENDER ENABLE	Selects the alpha blender overlay manager for the TV output instead of the color key alpha blender (LCD output). The bit field is deprecated. It is present for software backward compatibility only. When it is enabled, the Z-order defined in each ATTRIBUTES registers for only the pipelines associated pipeline connected to the TV output are invalid and replaced by the following: graphics z-order = 3, video3 z-order = 2, video2 z-order =1 and video1 z-order=0 If it disabled, the z-order and z-order enable bit fields defined in each ATTRIBUTES register are used. wr: EVSYNC start of primary LCD 0x0: Alpha blender is disabled. 0x1: The alpha blender is enabled.	RW	0

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Bits	Field Name	Description	Type	Reset
18	LCDALPHABLENDER ENABLE	Selects the alpha blender overlay manager for the primary LCD output instead of the color key alpha blender (LCD output). The bit field is deprecated. It is present for software backward compatibility only. When it is enabled, the Z-order defined in each ATTRIBUTES registers for only the pipelines associated with the primary LCD output are invalid and replaced by the following: graphics z-order = 3, video3 z-order = 2, video2 z-order =1 and video1 z-order=0 If it disabled, the z-order and z-order enable bit fields defined in each ATTRIBUTES register are used. wr: VFP start of primary LCD 0x0: Alpha blender is disabled. The color key alpha blending is used. 0x1: The alpha blender is enabled.	RW	0
17	BUFFERFILLING	Controls if the DMA buffers are refilled only when the LOW threshold is reached or if all DMA buffers are refilled when at least one of them reaches the LOW threshold. wr: immediate 0x0: Each DMA buffer is refilled when it reaches LOW threshold. 0x1: All DMA buffers are refilled up to high threshold when at least one of them reaches the LOW threshold. (only active DMA buffers shall be considered and when reaching the end of the frame the DMA buffer goes to empty condition so no need to fill it again).	RW	0
16	BUFFERHAND CHECK	Controls the handcheck between DMA buffer and STALL signal in order to prevent from underflow. The bit shall be set to 0 when the module is not in STALL mode. (primary LCD output) wr: VFP start of primary LCD 0x0: Only the STALL signal (generated by RFBI, DSI1 or DSI2 depending on which IP uses the LCD output) is used regardless of the DMA buffer fullness information in order to provide data to the RFBI,DSI1 or DS2 module. 0x1: The STALL signal (generated by RFBI, DSI1 or DSI2 depending on which IP uses the LCD output) is used in combination with the DMA buffer fullness information in order to provide data to the RFBI, DSI1 or DSI2 module only when it does not generated buffer underflow.	RW	0
15	CPR	Color Phase Rotation Control (primary LCD output). It shall be reset when ColorConvEnable bit field is set to 1 wr: VFP start period of primary LCD output 0x0: Color Phase Rotation Disabled 0x1: Color Phase Rotation Enabled	RW	0
14	BUFFERMERGE	Buffer merge control wr: EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory or VFP When enabled, the DISPC_GLOBAL_BUFFER register is ignored. This bit must be set to zero when the write back channel is used. When DISPC_CONTROL2.GOWB is used BUFFERMERGE MUST be zero. When DISPC_CONTROL2.GOWB is used BUFFERMERGE MUST be zero. wr: immediate 0x0: DMA buffer merge disabled Each DMA buffer is dedicated to one pipeline. 0x1: DMA buffer merge enabled All the DMA buffers are merged into a single one to be used by the single active pipeline.	RW	0
13	TCKTV SELECTION	Transparency Color Key Selection (TV output) wr: EVSYNC 0x0: Destination transparency color key selected 0x1: Source transparency color key selected	RW	0
12	TCKTVENABLE	Transparency Color Key Enabled (TV output) wr: EVSYNC 0x0: Disable the transparency color key for the TV output 0x1: Enable the transparency color key for the TV output	RW	0
11	TCKLCD SELECTION	Transparency Color Key Selection (primary LCD output) wr: VFP start period of primary LCD output 0x0: Destination transparency color key selected 0x1: Source transparency color key selected	RW	0

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Bits	Field Name	Description	Type	Reset
10	TCKLCDENABLE	Transparency Color Key Enabled (primary LCD output) wr: VFP start period of primary LCD output 0x0: Disable the transparency color key for the LCD 0x1: Enable the transparency color key for the LCD	RW	0
9	GAMATABLE ENABLE	For backward compatibility, an enable bit has been added on the 2 additional gamma tables (secondary display TV). Gamma table of LCD1 is always enabled. 0x0: Gamma table LDC2 TV are bypassed 0x1: Gamma table LCD2 TV are enabled	RW	0
8	ACBIASGATED	ACBias Gated Enabled (primary LCD output) wr: VFP start period of primary LCD output 0x0: AcBias Gated Disabled 0x1: AcBias Gated Enabled	RW	0
7	VSYNCGATED	VSYNC Gated Enabled (primary LCD output) wr: VFP start period of primary LCD output 0x0: VSYNC Gated Disabled 0x1: VSYNC Gated Enabled	RW	0
6	HSYNCGATED	HSYNC Gated Enabled (primary LCD output) wr: VFP start period of primary LCD output 0x0: HSYNC Gated Disabled 0x1: HSYNC Gated Enabled	RW	0
5	PIXELCLOCK GATED	Pixel Clock Gated Enabled (primary LCD output) wr: VFP start period of primary LCD output 0x0: Pixel Clock Gated Disabled 0x1: Pixel Clock Gated Enabled	RW	0
4	PIXELDATAGATED	Pixel Data Gated Enabled (primary LCD output) wr: VFP start period of primary LCD output 0x0: Pixel Data Gated Disabled 0x1: Pixel Data Gated Enabled	RW	0
3	PALETTEGAMMA TABLE	Palette/Gamma Table selection wr: VFP start period of primary LCD output or VFP start period of secondary LCD output or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the graphics pipeline: primary LCD, secondary LCD, TV output or write-back to the memory. In case of the table is used as gamma table, it is used for the primary LCD output only. 0x0: LUT used as palette (only if graphics format is BITMAP1, 2, 4, and 8) 0x1: LUT used as gamma table (only if graphics format is NOT BITMAP1, 2, 4, and 8 or no graphics window present)	RW	0
2:1	LOADMODE	Loading Mode for the Palette/Gamma Table wr: VFP start period of primary LCD output or VFP start period of secondary LCD output or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory 0x0: Palette/Gamma Table and data are loaded every frame 0x1: Palette/Gamma Table to be loaded. The user sets the bit when the palette/gamma table has to be loaded. Hardware resets the bit to 0x2 when table has been loaded. (DISPC_GFX_ATTRIBUTES.ENABLE has to be set to 1). 0x2: Frame data only loaded every frame 0x3: Palette/Gamma Table and frame data loaded on first frame then switch to 0x2 (Hardware).	RW	0x0

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Bits	Field Name	Description	Type	Reset
0	PIXELGATED	Pixel Gated Enable (only for TFT) (primary LCD output) wr: VFP start period of primary LCD output 0x0: Pixel clock always toggles (only in TFT mode) 0x1: Pixel clock only toggles when there is valid data to display. (only in TFT mode)	RW	0

Table 10-148. Register Call Summary for Register DISPC_CONFIG1

Display Controller

- Wakeup: [0]
- Color Look-Up Table (CLUT): [1] [2]
- Overlay Manager: [3] [4] [5] [6] [7] [8]
- Shadow Registers: [9]
- Operational Modes Configuration: [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20]
- Display Controller Logical Register Mapping: [21]
- Display Controller Register Summary: [22]

Table 10-149. DISPC_DEFAULT_COLOR0

Address Offset	0x0000 004C		
Physical Address	0x4804 104C 0x5800 104C	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The control register allows to configure the default solid background color for the primary LCD. Shadow register, updated on VFP start period of the primary LCD		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								DEFAULTCOLOR																							

Bits	Field Name	Description	Type	Reset
31:24	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
23:0	DEFAULTCOLOR	24-bit RGB color value to specify the default solid color to display when there is no data from the overlays.	RW	0x000000

Table 10-150. Register Call Summary for Register DISPC_DEFAULT_COLOR0

Display Controller

- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1]
- Display Controller Register Summary: [2]

Table 10-151. DISPC_DEFAULT_COLOR1

Address Offset	0x0000 0050		
Physical Address	0x4804 1050 0x5800 1050	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The control register allows to configure the default solid background color for the TV output. Shadow register, updated on EVSYNC		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								DEFAULTCOLOR																							

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Bits	Field Name	Description	Type	Reset
31:24	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
23:0	DEFAULTCOLOR	24-bit RGB color value to specify the default solid color to display when there is no data from the overlays.	RW	0x000000

Table 10-152. Register Call Summary for Register DISPC_DEFAULT_COLOR1

Display Controller

- Timing and TV Format Settings: [0]
- Shadow Registers: [1]
- Operational Modes Configuration: [2]
- Display Controller Logical Register Mapping: [3]
- Display Controller Register Summary: [4]

Table 10-153. DISPC_TRANS_COLOR0

Address Offset	0x0000 0054		
Physical Address	0x4804 1054 0x5800 1054	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register sets the transparency color value for the video/graphics overlays for the primary LCD output. Shadow register, updated on VFP start period of the primary LCD		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TRANSCOLORKEY																							

Bits	Field Name	Description	Type	Reset
31:24	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
23:0	TRANSCOLORKEY	Transparency Color Key Value in RGB format [0] BITMAP 1 (CLUT), [23,1] set to 0s [1:0] BITMAP 2 (CLUT), [23,2] set to 0s [3:0] BITMAP 4 (CLUT), [23,4] set to 0s [7:0] BITMAP 8 (CLUT), [23,8] set to 0s [11:0] RGB 12, [23,12] set to 0s [15:0] RGB 16, [23,16] set to 0s [23:0] RGB 24	RW	0x000000

Table 10-154. Register Call Summary for Register DISPC_TRANS_COLOR0

Display Controller

- Overlay Manager: [0]
- Shadow Registers: [1]
- Display Controller Logical Register Mapping: [2]
- Display Controller Register Summary: [3]

Table 10-155. DISPC_TRANS_COLOR1

Address Offset	0x0000 0058		
Physical Address	0x4804 1058 0x5800 1058	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register sets the transparency color value for the video/graphics overlays for the TV output. Shadow register, updated on EVSYNC		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TRANSCOLORKEY																							

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Bits	Field Name	Description	Type	Reset
31:24	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
23:0	TRANSCOLORKEY	Transparency Color Key Value in RGB format [0] BITMAP 1 (CLUT), [23,1] set to 0s [1:0] BITMAP 2 (CLUT), [23,2] set to 0s [3:0] BITMAP 4 (CLUT), [23,4] set to 0s [7:0] BITMAP 8 (CLUT), [23,8] set to 0s [11:0] RGB 12, [23,12] set to 0s [15:0] RGB 16, [23,16] set to 0s [23:0] RGB 24	RW	0x000000

Table 10-156. Register Call Summary for Register DISPC_TRANS_COLOR1

Display Controller

- Overlay Manager: [0]
- Shadow Registers: [1]
- Operational Modes Configuration: [2]
- Display Controller Logical Register Mapping: [3]
- Display Controller Register Summary: [4]

Table 10-157. DISPC_LINE_STATUS

Address Offset	0x0000 005C		
Physical Address	0x4804 105C 0x5800 105C	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The control register indicates the current primary LCD panel display line number.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																					LINENUMBER										

Bits	Field Name	Description	Type	Reset
31:11	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x000000
10:0	LINENUMBER	Current LCD panel line number Current display line number. The first active line has the value 0. During blanking lines the line number is not incremented.	R	0x000

Table 10-158. Register Call Summary for Register DISPC_LINE_STATUS

Display Controller

- Shadow Registers: [0]
- Display Controller Register Summary: [1]

Table 10-159. DISPC_LINE_NUMBER

Address Offset	0x0000 0060		
Physical Address	0x4804 1060 0x5800 1060	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The control register indicates the primary LCD panel display line number for the interrupt and the DMA request. Shadow register, updated on VFP start period of primary LCD.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																					LINENUMBER										

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Bits	Field Name	Description	Type	Reset
31:11	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x000000
10:0	LINENUMBER	LCD panel line number programming LCD line number defines the line on which the programmable interrupt is generated and the DMA request occurs.	RW	0x000

Table 10-160. Register Call Summary for Register DISPC_LINE_NUMBER

Display Controller
- sDMA Requests: [0]
- Shadow Registers: [1]
- Display Controller Register Summary: [2]

Table 10-161. DISPC_TIMING_H1

Address Offset	0x0000 0064		
Physical Address	0x4804 1064 0x5800 1064	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the timing logic for the HSYNC signal. It is used for the primary LCD output. Shadow register, updated on VFP start period of primary LCD		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HBP																HFP								HSW							

Bits	Field Name	Description	Type	Reset
31:20	HBP	Horizontal Back Porch. Encoded value (from 1 to 4096) to specify the number of pixel clock periods to add to the beginning of a line transmission before the first set of pixels is output to the display (program to value minus 1). When in BT mode and interlaced, this field corresponds to the vertical field blanking No 2 for Even Field.	RW	0x000
19:8	HFP	Horizontal front porch. Encoded value (from 1 to 4096) to specify the number of pixel clock periods to add to the end of a line transmission before line clock is asserted (program to value minus 1). When in BT mode and interlaced, this field corresponds to the vertical field blanking No 1 for Even Field.	RW	0x000
7:0	HSW	Horizontal synchronization pulse width Encoded value (from 1 to 256) to specify the number of pixel clock periods to pulse the line clock at the end of each line (program to value minus 1). When in BT mode, this field corresponds to the horizontal blanking	RW	0x00

Table 10-162. Register Call Summary for Register DISPC_TIMING_H1

Display Controller
- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1]
- Display Controller Register Summary: [2]

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Table 10-163. DISPC_TIMING_V1

Address Offset	0x0000 0068		
Physical Address	0x4804 1068 0x5800 1068	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the timing logic for the VSYNC signal. It is used for the primary LCD output. Shadow register, updated on VFP start period of primary LCD		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VBP																VFP								VSW							

Bits	Field Name	Description	Type	Reset
31:20	VBP	Vertical back porch Encoded value (from 0 to 4095) to specify the number of line clock periods to add to the beginning of a frame.	RW	0x000
19:8	VFP	Vertical front porch Encoded value (from 0 to 4095) to specify the number of line clock periods to add to the end of each frame.	RW	0x000
7:0	VSW	Vertical synchronization pulse width In active mode, encoded value (from 1 to 256) to specify the number of line clock periods (program to value minus 1) to pulse the frame clock (VSYNC) pin at the end of each frame after the end of frame wait (VFP) period elapses. Frame clock uses as VSYNC signal in active mode. In passive mode, encoded value (from 1 to 256) to specify the number of extra line clock periods (program to value minus 1) to insert after the vertical front porch (VFP) period has elapsed.	RW	0x00

Table 10-164. Register Call Summary for Register DISPC_TIMING_V1

Display Controller

- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1]
- Display Controller Register Summary: [2]

Table 10-165. DISPC_POL_FREQ1

Address Offset	0x0000 006C		
Physical Address	0x4804 106C 0x5800 106C	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the signal configuration. It is used for the primary LCD output. Shadow register, updated on VFP start period of primary LCD.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ALIGN	ONOFF	RF	IEO	IPC	IHS	IVS	ACBI				ACB							

Bits	Field Name	Description	Type	Reset
31:19	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0000
18	ALIGN	Defines the alignment between HSYNC and VSYNC assertion. 0x0: VSYNC and HSYNC are not aligned 0x1: VSYNC and HSYNC assertions are aligned.	RW	0
17	ONOFF	HSYNC/VSYNC Pixel clock Control On/Off 0x0: HSYNC and VSYNC are driven on opposite edges of pixel clock than pixel data 0x1: HSYNC and VSYNC are driven according to bit 16	RW	0

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Bits	Field Name	Description	Type	Reset
16	RF	Program HSYNC/VSYNC Rise or Fall 0x0: HSYNC and VSYNC are driven on falling edge of pixel clock (if bit 17 set to 1) 0x1: HSYNC and VSYNC are driven on rising edge of pixel clock (if bit 17 set to 1)	RW	0
15	IEO	Invert output enable 0x0: Ac-bias is active high (active display mode) 0x1: Ac-bias is active low (active display mode)	RW	0
14	IPC	Invert pixel clock 0x0: Data is driven on the LCD data lines on the rising-edge of the pixel clock 0x1: Data is driven on the LCD data lines on the falling-edge of the pixel clock	RW	0
13	IHS	Invert HSYNC 0x0: Line clock pin is active high and inactive low 0x1: Line clock pin is active low and inactive high	RW	0
12	IVS	Invert VSYNC 0x0: Frame clock pin is active high and inactive low 0x1: Frame clock pin is active low and inactive high	RW	0
11:8	ACBI	AC Bias Pin transitions per interrupt Value (from 0 to 15) used to specify the number of AC Bias pin transitions	RW	0x0
7:0	ACB	AC Bias Pin Frequency Value (from 0 to 255) used to specify the number of line clocks to count before transitioning the AC Bias pin. This pin is used to periodically invert the polarity of the power supply to prevent DC charge build-up within the display.	RW	0x00

Table 10-166. Register Call Summary for Register DISPC_POL_FREQ1

Display Controller

- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1]
- Display Controller Register Summary: [2]

Table 10-167. DISPC_DIVISOR1

Address Offset	0x0000 0070		
Physical Address	0x4804 1070 0x5800 1070	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the divisors. It is used for the primary LCD output Shadow register, updated on VFP start period of primary LCD		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								LCD								RESERVED								PCD							

Bits	Field Name	Description	Type	Reset
31:24	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
23:16	LCD	Display Controller Logic Clock Divisor Value (from 1 to 255) to specify the intermediate pixel clock frequency based on the LCD1_CLK. The value 0 is invalid.	RW	0x04
15:8	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
7:0	PCD	Pixel Clock Divisor Value (from 1 to 255) to specify the frequency of the pixel clock based on the LCD1_CLK divided by DISPC_DIVISOR1.LCD value. The values 0 is invalid.	RW	0x01

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Table 10-168. Register Call Summary for Register DISPC_DIVISOR1

Display Controller

- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1]
- Display Controller Register Summary: [2]
- Display Controller Register Description: [3] [4] [5] [6]

Table 10-169. DISPC_GLOBAL_ALPHA

Address Offset	0x0000 0074		
Physical Address	0x4804 1074 0x5800 1074	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register defines the global alpha value for the graphics and three video pipelines. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory for each bit field depending on the association of the each pipeline with the primary LCD, secondary LCD or TV output.		
Type	RW		

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
VID3GLOBALALPHA	VID2GLOBALALPHA	VID1GLOBALALPHA	GFXGLOBALALPHA

Bits	Field Name	Description	Type	Reset
31:24	VID3GLOBALALPHA	Global alpha value from 0 to 255. 0 corresponds to fully transparent and 255 to fully opaque.	RW	0xFF
23:16	VID2GLOBALALPHA	Global alpha value from 0 to 255. 0 corresponds to fully transparent and 255 to fully opaque.	RW	0xFF
15:8	VID1GLOBALALPHA	Global alpha value from 0 to 255. 0 corresponds to fully transparent and 255 to fully opaque.	RW	0xFF
7:0	GFXGLOBALALPHA	Global alpha value from 0 to 255. 0 corresponds to fully transparent and 255 to fully opaque.	RW	0xFF

Table 10-170. Register Call Summary for Register DISPC_GLOBAL_ALPHA

Display Controller

- Overlay Manager: [0]
- Shadow Registers: [1]
- Operational Modes Configuration: [2] [3]
- Display Controller Register Summary: [4]

Table 10-171. DISPC_SIZE_TV

Address Offset	0x0000 0078		
Physical Address	0x4804 1078 0x5800 1078	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the size of the TV output field (interlace), frame (progressive) (horizontal and vertical). Shadow register, updated on EVSYNC. A delta value is used to indicate if the odd field has same vertical size as the even field or +/- one line.		
Type	RW		

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14	13 12 11 10 9 8	7 6 5 4 3 2 1 0
RESERVED	LPP	DELTA_LPP	RESERVED	PPL

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Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
26:16	LPP	Lines per panel Encoded value (from 1 to 2048) to specify the number of lines per panel.	RW	0x000
15:14	DELTA_LPP	Indicates the delta size value of the odd field compared to the even field 0x0: Same size 0x1: Odd size = Even size +1 0x2: Odd size = Even Size -1	RW	0x0
13:11	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0
10:0	PPL	Pixels per line Encoded value (from 1 to 2048) to specify the number of pixels contains within each line on the display.	RW	0x000

Table 10-172. Register Call Summary for Register DISPC_SIZE_TV

Display Controller

- Timing and TV Format Settings: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9]
- Shadow Registers: [10]
- Operational Modes Configuration: [11] [12] [13]
- Display Controller Register Summary: [14]
- Display Controller Register Description: [15]

Table 10-173. DISPC_SIZE_LCD1

Address Offset	0x0000 007C		
Physical Address	0x4804 107C 0x5800 107C	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the panel size (horizontal and vertical). Shadow register, updated on VFP start period of primary LCD. A delta value is used to indicate if the odd field has same vertical size as the even field or +/- one line.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								LPP								DELTA_LPP		RESERVED						PPL							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
26:16	LPP	Lines per panel Encoded value (from 1 to 2048) to specify the number of lines per panel (program to value minus 1).	RW	0x000
15:14	DELTA_LPP	Indicates the delta size value of the odd field compared to the even field 0x0: same size 0x1: Odd size = Even size +1 0x2: Odd size = Even Size -1	RW	0x0
13:11	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0
10:0	PPL	Pixels per line Encoded value (from 1 to 2048) to specify the number of pixels contains within each line on the display (program to value minus 1). In STALL mode, any value is valid. In non STALL mode, only values multiple of 8 pixels are valid.	RW	0x000

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Table 10-174. Register Call Summary for Register DISPC_SIZE_LCD1

Display Controller

- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1] [2]
- Display Controller Register Summary: [3]
- Display Controller Register Description: [4]

Table 10-175. DISPC_GFX_BA_j

Address Offset	0x0000 0080 + (0x4 * j)	**Index**	j = 0 to 1
Physical Address	0x4804 1080 + (0x4 * j) 0x5800 1080 + (0x4 * j)	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the base address of the graphics buffer displayed in the graphics window (0 1 :for ping-pong mechanism with external trigger, based on the field polarity, 0 only used when graphics pipeline on the LCD output and 0 1 when on the TV output). Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BA																															

Bits	Field Name	Description	Type	Reset
31:0	BA	Graphics base address Base address of the graphics buffer (aligned on pixel size boundary) (in case 1-, 2-, and 4-bpp, byte alignment is required, in case of RGB24 packed format, 4-pixel alignment is required) When the TILER is addressed, the bits: [28:27] = 0x0 for 8-bit tiled [28:27] = 0x1 for 16-bit tiled [28:27] = 0x2 for 32-bit tiled [28:27] = 0x3 for page mode [31:29] = 0x0 for 0-degree view [31:29] = 0x1 for 180-degree view + mirroring [31:29] = 0x2 for 0-degree view + mirroring [31:29] = 0x3 for 180-degree view [31:29] = 0x4 for 270-degree view + mirroring [31:29] = 0x5 for 270-degree view [31:29] = 0x6 for 90-degree view [31:29] = 0x7 for 90-degree view + mirroring Otherwise the bits indicated the corresponding bit address to access the SDRAM.	RW	0x0000 0000

Table 10-176. Register Call Summary for Register DISPC_GFX_BA_j

Display Controller

- Addressing and Bursts: [0]
- Rotation and Mirroring: [1] [2] [3] [4]
- Shadow Registers: [5]
- Operational Modes Configuration: [6]
- Display Controller Register Summary: [7]

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Table 10-177. DISPC_GFX_POSITION

Address Offset	0x0000 0088		
Physical Address	0x4804 1088 0x5800 1088	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the position of the graphics window. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								POSY								RESERVED								POSX							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
26:16	POSY	Y position of the graphics window. Encoded value (from 0 to 2047) to specify the Y position of the graphics window on the screen. The line at the top has the Y-position 0.	RW	0x000
15:11	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
10:0	POSX	X position of the graphics window. Encoded value (from 0 to 2047) to specify the X position of the graphics window on the screen. The first pixel on the left of the screen has the X-position 0.	RW	0x000

Table 10-178. Register Call Summary for Register DISPC_GFX_POSITION

Display Controller

- Overlay Manager: [0]
- Shadow Registers: [1]
- Operational Modes Configuration: [2] [3]
- Display Controller Register Summary: [4]

Table 10-179. DISPC_GFX_SIZE

Address Offset	0x0000 008C		
Physical Address	0x4804 108C 0x5800 108C	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the size of the graphics window. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								SIZEY								RESERVED								SIZEX							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
26:16	SIZEY	Number of lines of the graphics window. Encoded value (from 1 to 2048) to specify the number of lines of the graphics window (program to value minus 1).	RW	0x000
15:11	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
10:0	SIZEX	Number of pixels of the graphics window. Encoded value (from 1 to 2048) to specify the number of pixels per line of the graphics window (program to value minus 1).	RW	0x000

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Table 10-180. Register Call Summary for Register DISPC_GFX_SIZE

Display Controller

- Addressing and Bursts: [0]
- Overlay Manager: [1]
- Shadow Registers: [2]
- Operational Modes Configuration: [3] [4]
- Display Controller Register Summary: [5]

Table 10-181. DISPC_GFX_ATTRIBUTES

Address Offset	0x0000 00A0		
Physical Address	0x4804 10A0 0x5800 10A0	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the graphics attributes. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31 30	29	28	27 26	25	24	23 22 21 20 19 18	17	16	15	14	13 12	11	10	9	8	7 6	5	4 3 2 1	0
CHANNELOUT2	BURSTTYPE	PREMULTIPLYALPHA	ZORDER	ZORDERENABLE	ANTIFLICKER	RESERVED	SELFREFRESHAUTO	RESERVED	SELFREFRESH	ARBITRATION	ROTATION	BUFPRELOAD	RESERVED	NIBBLEMODE	CHANNELOUT	BURSTSIZE	REPLICATIONENABLE	FORMAT	ENABLE

Bits	Field Name	Description	Type	Reset
31:30	CHANNELOUT2	It is not used if CHANNELOUT is set to TV. Reserved when CHANNELOUT = 1 (should set to zero) wr: immediate 0x0: primary LCD output selected. 0x1: Secondary LCD output selected. 0x3: Write-back output to the memory selected.	RW	0x0
29	BURSTTYPE	The type of burst can be INCR (incremental) or BLCK (2D block). The 2D block is required when the TILER is targeted by the DMA engine. (It does not apply to the palette loading OCP requests using INCR burst only) 0x0: INC burst type is used. 0x1: 2D block burst type is used.	RW	0
28	PREMULTIPLYALPHA	The field configures the DISPC GFX to process incoming data as premultiplied alpha data or non premultiplied alpha data. Default setting is non premultiplied alpha data. 0x0: Non premultiplyalpha data color component 0x1: Premultiplyalpha data color component	RW	0

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Bits	Field Name	Description	Type	Reset
27:26	ZORDER	Z-Order defining the priority of the layer compared to others when overlaying. It is software responsibility to ensure that each layer connected to the same overlay manager has a different z-order value. If bit 25 is set to 0, the ZORDER bit field is ignored and replaced by the value 0. 0x0: Z-order 0: layer above solid background color and below layer with higher Z-order values. 0x1: Z-order 1: layer above layer with z-order value of 0 and below layers with z-order values of 2 and 3 0x3: Z-order 3: layer above all the other layers 0x2: Z-order 2: layer above layers with z-order value of 0 and 1 and below layer with z-order value of 3	RW	0x0
25	ZORDERENABLE	Z-order Enable. The bit field ZORDER is only used when the Z-order is enabled. 0x0: Z-order disabled. The Z-order of the layer is 0. 0x1: Z-order enabled. The Z-order is defined by the bit field ZORDER (bits 26 and 27).	RW	0
24	ANTIFLICKER	Antiflicker filtering using a 3-tap filter with hardcoded coefficients (1/4, 1/2, 1/4) 0x0: Antiflicker disabled. 0x1: Antiflicker enabled.	RW	0
23:18	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
17	SELFREFRESHAUTO	Automatic self-refresh mode 0x0: The transition from Selfrefresh "disabled" to "enabled" is controlled by software 0x1: The transition from Selfrefresh "disabled" to "enabled" is controlled only by hardware	RW	0
16	RESERVED		R	0
15	SELFREFRESH	Enables the self refresh of the graphics window from its own DMA buffer. This bit should be set only after having set the GO bit of the channel and read back a zero in its field. 0x0: The graphics pipeline accesses the interconnect to fetch data from the system memory. 0x1: The graphics pipeline does not need anymore to fetch data from memory. Only the graphics DMA buffer is used. It takes effect after the frame has been loaded in the DMA buffer.	RW	0
14	ARBITRATION	Determines the priority of the graphics pipeline. When the graphics pipeline is one of the high priority pipelines. The arbitration wheel gives always the priority first to the high priority pipelines using round-robin between them. When there is only normal priority pipelines sending requests, the round-robin applies between them. 0x0: The graphics pipeline is one of the normal priority pipeline. 0x1: The graphics pipeline is one of the high priority pipeline.	RW	0
13:12	ROTATION	Graphics Rotation Flag 0x0: No rotation 0x1: Rotation by 90 degrees 0x3: Rotation by 270 degrees 0x2: Rotation by 180 degrees	RW	0x0

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Bits	Field Name	Description	Type	Reset
11	BUFPRELOAD	Graphics Preload Value 0x0: Hardware prefetches pixels up to the preload value defined in the preload register 0x1: Hardware prefetches pixels up to high threshold value	RW	0
10	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0
9	NIBBLEMODE	Graphics Nibble Mode (only for 1-, 2- and 4-bpp) 0x0: Nibble mode is disabled 0x1: Nibble mode is enabled	RW	0
8	CHANNELOUT	Graphics Channel Out configuration: LCD, WB or TV. wr: immediate 0x0: LCD output or WB to the memory selected. bit fields 31 and 30 defines the output associated (primary, secondary or write-back). 0x1: TV output selected	RW	0
7:6	BURSTSIZE	Graphics DMA Burst Size 0x0: 2x128bit bursts 0x1: 4x128bit bursts 0x3: Reserved 0x2: 8x128bit bursts	RW	0x2
5	REPLICATIONENABLE	Graphics Replication Enabled: RGB . ARGB, and RGBA formats are converted into ARGB32-8888 using replication of the MSBs or '0s 0x0: Disable Graphics replication logic. The conversion to ARGB32-8888 is done by adding 0s for the LSBs 0x1: Enable Graphics replication logic. The conversion to ARGB32-8888 is done by duplicating the MSBs for the LSBs	RW	1
4:1	FORMAT	Graphics format. It defines the pixel format when fetching the graphics picture into memory. 0x6: RGB16-565 0x1: BITMAP2 (CLUT is required to be used) 0xA: RGBx12-4444 0x7: ARGB16-1555 0xD: RGBA32-8888 0x0: BITMAP1 (CLUT is required to be used) 0x2: BITMAP4 (CLUT is required to be used) 0x8: xRGB24-8888 (32-bit container) 0x9: RGB24-888 (24-bit container) 0xB: RGBA12-4444 0x4: xRGB12-4444 0x5: ARGB16-4444 0xF: xRGB15-1555 0xC: ARGB32-8888 0x3: BITMAP8 (CLUT is required to be used) 0xE: RGBx24-8888 (24-bit RGB aligned on MSB of the 32-bit container)	RW	0x0
0	ENABLE	Graphics Enable 0x0: Graphics disabled (graphics pipeline inactive and graphics window not present) 0x1: Graphics enabled (graphics pipeline active and graphics window present on the screen)	RW	0

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Table 10-182. Register Call Summary for Register DISPC_GFX_ATTRIBUTES

Display Controller

- Addressing and Bursts: [0] [1]
- Arbitration: [2]
- DMA Power Modes: [3] [4]
- Memory Format: [5]
- Graphics Pipeline: [6] [7] [8]
- Replication Logic: [9] [10]
- Overlay Manager: [11] [12] [13] [14] [15]
- Shadow Registers: [16]
- Operational Modes Configuration: [17] [18] [19] [20] [21] [22] [23] [24] [25] [26] [27] [28] [29] [30] [31] [32]
- Display Controller Register Summary: [33]
- Display Controller Register Description: [34]

Table 10-183. DISPC_GFX_BUF_THRESHOLD

Address Offset	0x0000 00A4		
Physical Address	0x4804 10A4 0x5800 10A4	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the graphics buffer. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BUFHIGHTHRESHOLD																BUFLOWTHRESHOLD															

Bits	Field Name	Description	Type	Reset
31:16	BUFHIGHTHRESHOLD	DMA buffer High Threshold Number of 128-bits defining the threshold value.	RW	0x04FF
15:0	BUFLOWTHRESHOLD	DMA buffer Low Threshold Number of 128-bits defining the threshold value. The value put is this register should always be greater than zero.	RW	0x04F8

Table 10-184. Register Call Summary for Register DISPC_GFX_BUF_THRESHOLD

Display Controller

- DMA Buffers: [0] [1] [2]
- Shadow Registers: [3]
- Operational Modes Configuration: [4] [5]
- Display Controller Register Summary: [6]

Table 10-185. DISPC_GFX_BUF_SIZE_STATUS

Address Offset	0x0000 00A8		
Physical Address	0x4804 10A8 0x5800 10A8	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register defines the Graphics buffer size		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																BUFSIZE															

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Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0000
15:0	BUFSIZE	DMA buffer Size in number of 128-bits	R	0x0500

Table 10-186. Register Call Summary for Register DISPC_GFX_BUF_SIZE_STATUS

Display Controller

- Shadow Registers: [0]
- Display Controller Register Summary: [1]

Table 10-187. DISPC_GFX_ROW_INC

Address Offset	0x0000 00AC		
Physical Address	0x4804 10AC 0x5800 10AC	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the number of bytes to increment at the end of the row. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ROWINC																															

Bits	Field Name	Description	Type	Reset
31:0	ROWINC	Number of bytes to increment at the end of the row Encoded unsigned value to specify the number of bytes to increment at the end of the row in the graphics buffer. The value 0 is invalid. The value 1 means next pixel. The value 1+n*bpp means increment of n pixels. The value 1- (n+1)*bpp means decrement of n pixels.	RW	0x0000 0001

Table 10-188. Register Call Summary for Register DISPC_GFX_ROW_INC

Display Controller

- Addressing and Bursts: [0] [1]
- Predecimation: [2]
- Rotation and Mirroring: [3] [4] [5] [6]
- Shadow Registers: [7]
- Operational Modes Configuration: [8]
- Display Controller Register Summary: [9]

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Table 10-189. DISPC_GFX_PIXEL_INC

Address Offset	0x0000 00B0		
Physical Address	0x4804 10B0 0x5800 10B0	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the number of bytes to increment between two pixels. For more information, see Section 10.2.4.6.3, *Predecimation*. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								PIXELINC							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x000000
7:0	PIXELINC	Number of bytes to increment between two pixels. Encoded unsigned value (from 1 to 255) to specify the number of bytes between two pixels in the graphics buffer. The value 0 is invalid. The value 1 means next pixel. The value 1+n*bpp means increment of n pixels.	RW	0x01

Table 10-190. Register Call Summary for Register DISPC_GFX_PIXEL_INC

Display Controller

- Addressing and Bursts: [0]
- Predecimation: [1]
- Rotation and Mirroring: [2] [3] [4] [5]
- Shadow Registers: [6]
- Operational Modes Configuration: [7]
- Display Controller Register Summary: [8]

Table 10-191. DISPC_GFX_WINDOW_SKIP

Address Offset	0x0000 00B4		
Physical Address	0x4804 10B4 0x5800 10B4	**Instance**	DISPC_PER_L4 DISPC_L3
Description	Write 0s for future compatibility. Reads return 0.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WINDOWSKIP																															

Bits	Field Name	Description	Type	Reset
31:0	WINDOWSKIP	Number of bytes to skip during the video window 1. Encoded signed value (from -231-1 to 231) to specify the number of bytes to skip in the graphics buffer when the video window 1 is displayed on top of the graphics and no transparency color is enabled.	R	0x0000 0000

Table 10-192. Register Call Summary for Register DISPC_GFX_WINDOW_SKIP

Display Controller

- Shadow Registers: [0]
- Display Controller Register Summary: [1]

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Table 10-193. DISPC_GFX_TABLE_BA

Address Offset	0x0000 00B8		
Physical Address	0x4804 10B8 0x5800 10B8	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the base address of the palette buffer or the gamma table buffer. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TABLEBA																															

Bits	Field Name	Description	Type	Reset
31:0	TABLEBA	Base address of the palette/gamma table buffer (24-bit entries in 32-bit containers, aligned on 32-bit boundary).	RW	0x0000 0000

Table 10-194. Register Call Summary for Register DISPC_GFX_TABLE_BA

Display Controller

- Color Look-Up Table (CLUT): [0]
- Shadow Registers: [1]
- Operational Modes Configuration: [2]
- Display Controller Register Summary: [3]

Table 10-195. DISPC_VID1_BA_j

Address Offset	0x0000 00BC + (0x4 * j)	**Index**	j = 0 to 1
Physical Address	0x4804 10BC + (0x4 * j) 0x5800 10BC + (0x4 * j)	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the base address of the video buffer for the video window 1 (DISPC_VID1_BA_0 DISPC_VID1_BA_1 for ping-pong mechanism with external trigger, based on the field polarity otherwise only DISPC_VID1_BA_0 is used). Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BA																															

Bits	Field Name	Description	Type	Reset
31:0	BA	Video base address Base address of the video buffer (aligned on pixel size boundary except in case of RGB24 packed format, 4-pixel alignment is required; in case of YUV4:2:2, 2-pixel alignment is required, and YUV4:2:0, byte alignment is supported)). It case of YUV4:2:0 format, it indicates the base address of the Y buffer. When the TILER is addressed, the bits: [28:27] = 0x0 for 8-bit tiled [28:27] = 0x1 for 16-bit tiled [28:27] = 0x2 for 32-bit tiled [28:27] = 0x3 for page mode [31:29] = 0x0 for 0-degree view [31:29] = 0x1 for 180-degree view + mirroring [31:29] = 0x2 for 0-degree view + mirroring [31:29] = 0x3 for 180-degree view [31:29] = 0x4 for 270-degree view + mirroring [31:29] = 0x5 for 270-degree view [31:29] = 0x6 for 90-degree view [31:29] = 0x7 for 90-degree view + mirroring Otherwise the bits indicated the corresponding bit address to access the SDRAM.	RW	0x0000 0000

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Table 10-196. Register Call Summary for Register DISPC_VID1_BA_j

Display Controller

- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1]
- Display Controller Register Summary: [2]

Table 10-197. DISPC_VID1_POSITION

Address Offset	0x0000 00C4		
Physical Address	0x4804 10C4 0x5800 10C4	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the position of the video window 1. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								POSY								RESERVED								POSX							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
26:16	POSY	Y position of the video window 1 Encoded value (from 0 to 2047) to specify the Y position of the video window 1 .The line at the top has the Y-position 0.	RW	0x000
15:11	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
10:0	POSX	X position of the video window 1 Encoded value (from 0 to 2047) to specify the X position of the video window 1. The first pixel on the left of the display screen has the X-position 0.	RW	0x000

Table 10-198. Register Call Summary for Register DISPC_VID1_POSITION

Display Controller

- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1]
- Display Controller Register Summary: [2]

Table 10-199. DISPC_VID1_SIZE

Address Offset	0x0000 00C8		
Physical Address	0x4804 10C8 0x5800 10C8	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the size of the video window 1. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								SIZEY								RESERVED								SIZEX							

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Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
26:16	SIZEY	Number of lines of the video 1 Encoded value (from 1 to 2048) to specify the number of lines of the video window 1. Program to value minus 1.	RW	0x000
15:11	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
10:0	SIZEX	Number of pixels of the video window 1 Encoded value (from 1 to 2048) to specify the number of pixels of the video window 1. Program to value minus 1.	RW	0x000

Table 10-200. Register Call Summary for Register DISPC_VID1_SIZE

Display Controller

- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1]
- Display Controller Register Summary: [2]

Table 10-201. DISPC_VID1_ATTRIBUTES

Address Offset	0x0000 00CC		
Physical Address	0x4804 10CC 0x5800 10CC	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the attributes of the video window 1. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31 30	29	28	27 26	25	24	23	22	21	20	19	18	17	16	15 14	13 12	11	10	9	8	7 6 5 4 3 2 1 0		
CHANNELOUT2	BURSTTYPE	PREMULTIPHYALPHA	ZORDER	ZORDERENABLE	SELFREFRESH	ARBITRATION	DOUBLESTRIDE	VERTICALTAPS	DMAOPTIMIZATION	BUFPRELOAD	RESERVED	SELFREFRESHAUTO	CHANNELOUT	BURSTSIZE	ROTATION	FULLRANGE	REPLICATIONENABLE	COLORCONVENABLE	VRESIZECONF	HRESIZECONF	RESIZEENABLE	FORMAT	ENABLE

Bits	Field Name	Description	Type	Reset
31:30	CHANNELOUT2	It is not used if CHANNELOUT is set to TV. Reserved when CHANNELOUT = 1 (should be set to zero) wr: immediate 0x0: primary LCD output selected. 0x1: Secondary LCD output selected. 0x3: Write-back output to the memory selected.	RW	0x0
29	BURSTTYPE	The type of burst can be INCR (incremental) or BLCK (2D block). The 2D block is required when the TILER is targeted by the DMA engine. 0x0: INC burst type is used. 0x1: 2D block burst type is used.	RW	0
28	PREMULTIPHYALPHA	The field configures the DISPC VID1 to process incoming data as premultiplied alpha data or non premultiplied alpha data. Default setting is non premultiplied alpha data. 0x0: Non premultiplyalpha data color component 0x1: Premultiplyalpha data color component	RW	0

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Bits	Field Name	Description	Type	Reset
27:26	ZORDER	Z-Order defining the priority of the layer compared to others when overlaying. It is software responsibility to ensure that each layer connected to the same overlay manager has a different z-order value. If bit 25 is set to 0, the ZORDER bit field is ignored and replaced by the value 0. 0x0: Z-order 0: layer above solid background color and below layer with higher Z-order values. 0x1: Z-order 1: layer above layer with z-order value of 0 and below layers with z-order values of 2 and 3 0x3: Z-order 3: layer above all the other layers 0x2: Z-order 2: layer above layers with z-order value of 0 and 1 and below layer with z-order value of 3	RW	0x0
25	ZORDERENABLE	Z-order Enable. The bit field ZORDER is only used when the Z-order is enabled. 0x0: Z-order disabled. The Z-order of the layer is 0. 0x1: Z-order enabled. The Z-order is defined by the bit field ZORDER (bits 26 and 27).	RW	0
24	SELFREFRESH	Enables the self refresh of the video window from its own DMA buffer only. 0x0: The video pipeline accesses the interconnect to fetch data from the system memory. 0x1: The video pipeline does not need anymore to fetch data from memory. Only the DMA buffer associated with the video1 is used. It takes effect after the frame has been loaded in the DMA buffer.	RW	0
23	ARBITRATION	Determines the priority of the video pipeline. The video pipeline is one of the high priority pipeline. The arbitration gives always the priority first to the high priority pipelines using round-robin between them. When there is only normal priority pipelines sending requests, the round-robin applies between them. 0x0: The video pipeline is one of the normal priority pipeline. 0x1: The video pipeline is one of the high priority pipeline.	RW	0
22	DOUBLESTRIDE	Determines if the stride for CbCr buffer is the 1x or 2x of the Y buffer stride. It is only used in case of YUV4:2:0. 0x0: The CbCr stride value is equal to the Y stride. 0x1: The CbCr stride value is double to the Y stride.	RW	0
21	VERTICALTAPS	Video Vertical Resize Tap Number. The vertical polyphase filter can be configured in 3-tap or 5-tap configuration. According to the number of taps, the maximum input picture width is double while using 3-tap compared to 5-tap. 0x0: 3 taps are used for the vertical filtering logic. The 2 other taps are not used. The associated bit fields for the 2 other taps coefficients do not need to be initialized. 0x1: 5 taps are used for the vertical filtering logic.	RW	0
20	DMAOPTIMIZATION	Write 0s for future compatibility. Reads return 0.	R	0
19	BUFPRELOAD	Video Preload Value 0x0: Hardware prefetches pixels up to the preload value defined in the preload register 0x1: Hardware prefetches pixels up to high threshold value	RW	0
18	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0

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Bits	Field Name	Description	Type	Reset
17	SELFREFRESHAUTO	Automatic self-refresh mode 0x0: The transition from SELFREFRESH "disabled" to "enabled" is controlled by SW. 0x1: The transition from SELFREFRESH "disabled" to "enabled" is controlled only by hardware.	RW	0
16	CHANNELOUT	Video Channel Out configuration: LCD, WB or TV. wr: immediate 0x0: LCD output or WB to the memory selected. bit fields 31 and 30 defines the output associated (primary, secondary or write-back). 0x1: TV output selected	RW	0
15:14	BURSTSIZE	Video DMA Burst Size 0x0: 2x128bit bursts 0x1: 4x128bit bursts 0x3: Reserved 0x2: 8x128bit bursts	RW	0x2
13:12	ROTATION	Video Rotation Flag 0x0: No rotation 0x1: Rotation by 90 degrees 0x3: Rotation by 270 degrees 0x2: Rotation by 180 degrees	RW	0x0
11	FULLRANGE	Color Space Conversion full range setting. 0x0: Limited range selected: 16 subtracted from Y before color space conversion 0x1: Full range selected: Y is not modified before the color space conversion	RW	0
10	REPLICATIONENABLE	Replication Enable 0x0: Disable Video replication logic 0x1: Enable Video replication logic	RW	1
9	COLORCONVENABLE	Enable the color space conversion. The hardware does not enable/disable the conversion based on the pixel format. The bit field shall be reset when the format is not YUV. 0x0: Disable Color Space Conversion YUV to RGB 0x1: Enable Color Space Conversion YUV to RGB	RW	0
8	VRESIZECONF	Write 0s for future compatibility. Reads return 0.	R	0
7	HRESIZECONF	Write 0s for future compatibility. Reads return 0.	R	0
6:5	RESIZEENABLE	Video Resize Enable 0x0: Disable both horizontal and vertical resize processing 0x1: Enable the horizontal resize processing 0x3: Enable both horizontal and vertical resize processing 0x2: Enable the vertical resize processing	RW	0x0

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Bits	Field Name	Description	Type	Reset
4:1	FORMAT	Video Format. It defines the pixel format when fetching the video 1 picture into memory. 0x6: RGB16-565 0x1: RGB12x-4444 0xA: YUV2 4:2:2 co-sited 0x7: ARGB16-1555 0xD: RGBA32-8888 0x0: NV12 4:2:0 2 buffers (Y + UV) 0x2: RGBA12-4444 0x8: xRGB24-8888 (32-bit container) 0x9: RGB24-888 (24-bit container) 0xB: UYVY 4:2:2 co-sited 0x5: ARGB16-4444 0xF: xRGB15-1555 0xC: ARGB32-8888 0x4: xRGB12-4444 0xE: RGBx24-8888 (24-bit RGB aligned on MSB of the 32-bit container)	RW	0x0
0	ENABLE	Video Enable 0x0: Video disabled (video pipeline inactive and window not present) 0x1: Video enabled (video pipeline active and window present on the screen)	RW	0

Table 10-202. Register Call Summary for Register DISPC_VID1_ATTRIBUTES

Display Controller

- Overlay Manager: [0]
- Shadow Registers: [1]
- Display Controller Logical Register Mapping: [2]
- Display Controller Register Summary: [3]
- Display Controller Register Description: [4] [5] [6]

Table 10-203. DISPC_VID1_BUF_THRESHOLD

Address Offset	0x0000 00D0		
Physical Address	0x4804 10D0 0x5800 10D0	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the video buffer associated with the video pipeline 1. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BUFHIGHTHRESHOLD																BUFLOWTHRESHOLD															

Bits	Field Name	Description	Type	Reset
31:16	BUFHIGHTHRESHOLD	Video DMA buffer High Threshold Number of 128-bits defining the threshold value.	RW	0x07FF
15:0	BUFLOWTHRESHOLD	DMA buffer High Threshold Number of 128-bits defining the threshold value.	RW	0x07F8

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Table 10-204. Register Call Summary for Register DISPC_VID1_BUF_THRESHOLD

Display Controller

- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1]
- Display Controller Register Summary: [2]

Table 10-205. DISPC_VID1_BUF_SIZE_STATUS

Address Offset	0x0000 00D4		
Physical Address	0x4804 10D4 0x5800 10D4	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register defines the Video buffer size for the video pipeline 1.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																BUFSIZE															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0000
15:0	BUFSIZE	Video 1 DMA buffer Size in number of 128-bits	R	0x0800

Table 10-206. Register Call Summary for Register DISPC_VID1_BUF_SIZE_STATUS

Display Controller

- Shadow Registers: [0]
- Display Controller Register Summary: [1]

Table 10-207. DISPC_VID1_ROW_INC

Address Offset	0x0000 00D8		
Physical Address	0x4804 10D8 0x5800 10D8	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the number of bytes to increment at the end of the row for the buffer associated with the video window 1. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ROWINC																															

Bits	Field Name	Description	Type	Reset
31:0	ROWINC	Number of bytes to increment at the end of the row Encoded signed value (from $2^{31}1$ to 2^{31}) to specify the number of bytes to increment at the end of the row in the video buffer. The value 0 is invalid. The value 1 means next pixel. The value 1 + n * bpp means increment of n pixels. The value 1 (n + 1)* bpp means decrement of n pixels.	RW	0x0000 0001

Table 10-208. Register Call Summary for Register DISPC_VID1_ROW_INC

Display Controller

- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1]
- Display Controller Register Summary: [2]

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Table 10-209. DISPC_VID1_PIXEL_INC

Address Offset	0x0000 00DC		
Physical Address	0x4804 10DC 0x5800 10DC	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the number of bytes to increment between two pixels for the buffer associated with the video window 2. For more information, see Section 10.2.4.6.3, *Predecimation*. The register is used only when the TILER is not present in the system in order to perform low performance rotation. When the TILER IP is present it is highly recommended to use it for performing the rotation. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								PIXELINC							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x000000
7:0	PIXELINC	Number of bytes to increment between two pixels. Encoded unsigned value (from 1 to 255) to specify the number of bytes between two pixels in the video buffer. The value 0 is invalid. The value 1 means next pixel. The value 1+n*bpp means increment of n pixels. For YUV4:2:0, Max supported value is 128.	RW	0x01

Table 10-210. Register Call Summary for Register DISPC_VID1_PIXEL_INC

Display Controller

- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1]
- Display Controller Register Summary: [2]

Table 10-211. DISPC_VID1_FIR

Address Offset	0x0000 00E0		
Physical Address	0x4804 10E0 0x5800 10E0	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the resize factors for horizontal and vertical up/downsampling of the video window 1. It is used for ARGB and Y setting. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			FIRVINC													RESERVED			FIRHINC												

Bits	Field Name	Description	Type	Reset
31:29	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0
28:16	FIRVINC	Vertical increment of the up/downsampling filter. Encoded value (from 1 to 4096). The value 0 is invalid. The values greater than 4096 are invalid.	RW	0x0400
15:13	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0

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Bits	Field Name	Description	Type	Reset
12:0	FIRHINC	Horizontal increment of the up/downsampling filter. Encoded value (from 1 to 4096). The value 0 is invalid. The values greater than 4096 are invalid.	RW	0x0400

Table 10-212. Register Call Summary for Register DISPC_VID1_FIR

Display Controller
- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1]
- Display Controller Register Summary: [2]

Table 10-213. DISPC_VID1_PICTURE_SIZE

Address Offset	0x0000 00E4		
Physical Address	0x4804 10E4 0x5800 10E4	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the size of the video picture associated with the video layer 1 before up/down-scaling. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								ORGSIZEY								RESERVED								ORGSIZEX							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
26:16	ORGSIZEY	Number of lines of the video picture. Encoded value (from 1 to 2048) to specify the number of lines of the video picture in memory (program to value minus 1). When predecimation is set, the value represents the size of the image after predecimation but the max size of the unpredecimated image size in memory is still bounded to 2^{11}.	RW	0x000
15:11	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
10:0	ORGSIZEX	Number of pixels of the video picture Encoded value (from 1 to 2048) to specify the number of pixels of the video picture in memory (program to value minus 1). The size is limited to the size of the line buffer of the vertical sampling block in case the video picture is processed by the vertical filtering unit. (program to value minus 1). When predecimation is set, the value represents the size of the image after predecimation but the max size of the unpredecimated image size in memory is still bounded to 2^{11}.	RW	0x000

Table 10-214. Register Call Summary for Register DISPC_VID1_PICTURE_SIZE

Display Controller
- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1]
- Display Controller Register Summary: [2]

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Table 10-215. DISPC_VID1_ACCU_j

Address Offset	0x0000 00E8 + (0x4 * j)	**Index**	j = 0 to 1
Physical Address	0x4804 10E8 + (0x4 * j) 0x5800 10E8 + (0x4 * j)	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the resize accumulator init values for horizontal and vertical up/downsampling of the video window 1 (DISPC_VID1_ACCU_0 DISPC_VID1_ACCU_1 for ping-pong mechanism with external trigger, based on the field polarity) It is used for ARGB and Y setting. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								VERTICALACCU								RESERVED								HORIZONTALACCU							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
26:16	VERTICALACCU	Vertical initialization accu value Encoded value (from -1024 to 1023).	RW	0x000
15:11	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
10:0	HORIZONTALACCU	Horizontal initialization accu value Encoded value (from -1024 to 1023).	RW	0x000

Table 10-216. Register Call Summary for Register DISPC_VID1_ACCU_j

Display Controller

- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1]
- Display Controller Register Summary: [2]

Table 10-217. DISPC_VID1_FIR_COEF_H_i

Address Offset	0x0000 00F0 + (0x8 * i)	**Index**	i = 0 to 7
Physical Address	0x4804 10F0 + (0x8 * i) 0x5800 10F0 + (0x8 * i)	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The bank of registers configure the up/down-scaling coefficients for the horizontal resize of the video picture associated with the video window 1 for the phases from 0 to 7. It is used for ARGB and Y setting. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIRHC3								FIRHC2								FIRHC1								FIRHC0							

Bits	Field Name	Description	Type	Reset
31:24	FIRHC3	Signed coefficient C3 for the horizontal up/down-scaling with the phase n	RW	0x00
23:16	FIRHC2	Unsigned coefficient C2 for the horizontal up/down-scaling with the phase n	RW	0x00
15:8	FIRHC1	Signed coefficient C1 for the horizontal up/down-scaling with the phase n	RW	0x00
7:0	FIRHC0	Signed coefficient C0 for the horizontal up/down-scaling with the phase n	RW	0x00

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Table 10-218. Register Call Summary for Register DISPC_VID1_FIR_COEF_H_i

Display Controller

- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1]
- Display Controller Register Summary: [2]

Table 10-219. DISPC_VID1_FIR_COEF_HV_i

Address Offset	0x0000 00F4 + (0x8 * i)	**Index**	i = 0 to 7
Physical Address	0x4804 10F4 + (0x8 * i) 0x5800 10F4 + (0x8 * i)	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The bank of registers configure the down/up/down-scaling coefficients for the vertical and horizontal resize of the video picture associated with the video window 1 for the phases from 0 to 7. It is used for ARGB and Y setting. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIRVC2								FIRVC1								FIRVC0								FIRHC4							

Bits	Field Name	Description	Type	Reset
31:24	FIRVC2	Signed coefficient C2 for the vertical up/down-scaling with the phase n	RW	0x00
23:16	FIRVC1	Unsigned coefficient C1 for the vertical up/down-scaling with the phase n	RW	0x00
15:8	FIRVC0	Signed coefficient C0 for the vertical up/down-scaling with the phase n	RW	0x00
7:0	FIRHC4	Signed coefficient C4 for the horizontal up/down-scaling with the phase n	RW	0x00

Table 10-220. Register Call Summary for Register DISPC_VID1_FIR_COEF_HV_i

Display Controller

- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1]
- Display Controller Register Summary: [2]

Table 10-221. DISPC_VID1_CONV_COEF0

Address Offset	0x0000 0130		
Physical Address	0x4804 1130 0x5800 1130	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the color space conversion matrix coefficients for the video pipeline 1. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								RCR								RESERVED								RY							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
26:16	RCR	RCr Coefficient Encoded signed value (from -1024 to 1023).	RW	0x000
15:11	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00

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Bits	Field Name	Description	Type	Reset
10:0	RY	RY Coefficient Encoded signed value (from -1024 to 1023).	RW	0x000

Table 10-222. Register Call Summary for Register DISPC_VID1_CONV_COEF0

Display Controller
- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1]
- Display Controller Register Summary: [2]

Table 10-223. DISPC_VID1_CONV_COEF1

Address Offset	0x0000 0134		
Physical Address	0x4804 1134 0x5800 1134	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the color space conversion matrix coefficients for the video pipeline 1. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								GY								RESERVED								RCB							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
26:16	GY	GY Coefficient Encoded signed value (from -1024 to 1023).	RW	0x000
15:11	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
10:0	RCB	RCb Coefficient Encoded signed value (from -1024 to 1023).	RW	0x000

Table 10-224. Register Call Summary for Register DISPC_VID1_CONV_COEF1

Display Controller
- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1]
- Display Controller Register Summary: [2]

Table 10-225. DISPC_VID1_CONV_COEF2

Address Offset	0x0000 0138		
Physical Address	0x4804 1138 0x5800 1138	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the color space conversion matrix coefficients for the video pipeline 1. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								GCB								RESERVED								GCR							

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Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
26:16	GCB	GCb Coefficient Encoded signed value (from -1024 to 1023).	RW	0x000
15:11	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
10:0	GCR	GCr Coefficient Encoded signed value (from -1024 to 1023).	RW	0x000

Table 10-226. Register Call Summary for Register DISPC_VID1_CONV_COEF2

Display Controller

- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1]
- Display Controller Register Summary: [2]

Table 10-227. DISPC_VID1_CONV_COEF3

Address Offset	0x0000 013C		
Physical Address	0x4804 113C 0x5800 113C	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the color space conversion matrix coefficients for the video pipeline 1. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								BCR								RESERVED								BY							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
26:16	BCR	BCr coefficient Encoded signed value (from -1024 to 1023).	RW	0x000
15:11	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
10:0	BY	BY coefficient Encoded signed value (from -1024 to 1023).	RW	0x000

Table 10-228. Register Call Summary for Register DISPC_VID1_CONV_COEF3

Display Controller

- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1]
- Display Controller Register Summary: [2]

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Table 10-229. DISPC_VID1_CONV_COEF4

Address Offset	0x0000 0140		
Physical Address	0x4804 1140 0x5800 1140	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the color space conversion matrix coefficients for the video pipeline 1. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																					BCB										

Bits	Field Name	Description	Type	Reset
31:11	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x000000
10:0	BCB	BCb Coefficient Encoded signed value (from -1024 to 1023).	RW	0x000

Table 10-230. Register Call Summary for Register DISPC_VID1_CONV_COEF4

Display Controller

- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1]
- Display Controller Register Summary: [2]

Table 10-231. DISPC_VID2_BA_j

Address Offset	0x0000 014C + (0x4 * j)	**Index**	j = 0 to 1
Physical Address	0x4804 114C + (0x4 * j) 0x5800 114C + (0x4 * j)	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the base address of the video buffer for the video window 2 (DISPC_VID2_BA_0 DISPC_VID2_BA_1 for ping-pong mechanism with external trigger, based on the field polarity otherwise only DISPC_VID2_BA_0 is used)). Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BA																															

Bits	Field Name	Description	Type	Reset
31:0	BA	Video base address Base address of the video buffer (aligned on pixel size boundary except in case of RGB24 packed format, 4-pixel alignment is required; in case of YUV4:2:2, 2-pixel alignment is required, and YUV4:2:0, byte alignment is supported)). It case of YUV4:2:0 format, it indicates the base address of the Y buffer. When the TILER is addressed, the bits: [28:27] = 0x0 for 8-bit tiled [28:27] = 0x1 for 16-bit tiled [28:27] = 0x2 for 32-bit tiled [28:27] = 0x3 for page mode [31:29] = 0x0 for 0-degree view [31:29] = 0x1 for 180-degree view + mirroring [31:29] = 0x2 for 0-degree view + mirroring [31:29] = 0x3 for 180-degree view [31:29] = 0x4 for 270-degree view + mirroring [31:29] = 0x5 for 270-degree view [31:29] = 0x6 for 90-degree view [31:29] = 0x7 for 90-degree view + mirroring Otherwise the bits indicated the corresponding bit address to access the SDRAM.	RW	0x0000 0000

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Table 10-232. Register Call Summary for Register DISPC_VID2_BA_j

Display Controller

- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1]
- Display Controller Register Summary: [2]

Table 10-233. DISPC_VID2_POSITION

Address Offset	0x0000 0154		
Physical Address	0x4804 1154 0x5800 1154	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the position of the video window 2. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								POSY								RESERVED								POSX							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
26:16	POSY	Y position of the video window 2 Encoded value (from 0 to 2047) to specify the Y position of the video window 2 .The line at the top has the Y-position 0.	RW	0x000
15:11	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
10:0	POSX	X position of the video window 2 Encoded value (from 0 to 2047) to specify the X position of the video window 2. The first pixel on the left of the display screen has the X-position 0.	RW	0x000

Table 10-234. Register Call Summary for Register DISPC_VID2_POSITION

Display Controller

- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1]
- Display Controller Register Summary: [2]

Table 10-235. DISPC_VID2_SIZE

Address Offset	0x0000 0158		
Physical Address	0x4804 1158 0x5800 1158	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the size of the video window 2. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								SIZEY								RESERVED								SIZEX							

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Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
26:16	SIZEY	Number of lines of the video 2 Encoded value (from 1 to 2048) to specify the number of lines of the video window 2. Program to value minus 1.	RW	0x000
15:11	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
10:0	SIZEX	Number of pixels of the video window 2 Encoded value (from 1 to 2048) to specify the number of pixels of the video window 2. Program to value minus 1.	RW	0x000

Table 10-236. Register Call Summary for Register DISPC_VID2_SIZE

Display Controller

- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1]
- Display Controller Register Summary: [2]

Table 10-237. DISPC_VID2_ATTRIBUTES

Address Offset	0x0000 015C		
Physical Address	0x4804 115C 0x5800 115C	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the attributes of the video window 2. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31 30	29	28	27 26	25	24	23	22	21	20	19	18	17	16	15 14	13 12	11	10	9	8	7	6	5 4 3 2 1	0
CHANNELOUT2	BURSTTYPE	PREMULTIPLYALPHA	ZORDER	ZORDERENABLE	SELFREFRESH	ARBITRATION	DOUBLESTRIDE	VERTICALTAPS	DMAOPTIMIZATION	BUFPRELOAD	RESERVED	SELFREFRESHAUTO	CHANNELOUT	BURSTSIZE	ROTATION	FULLRANGE	REPLICATIONENABLE	COLORCONVENABLE	VRESIZECONF	HRESIZECONF	RESIZEENABLE	FORMAT	ENABLE

Bits	Field Name	Description	Type	Reset
31:30	CHANNELOUT2	Value 0x2 is reserved when [16] CHANNELOUT bit = 0. Values 0x1, 0x2 and 0x3 are reserved when CHANNELOUT bit = 1 and TV format other than HDMI 1.4 3D 1080p is to be output. wr: immediate. 0x0: primary LCD output selected. 0x2: TV output selected. Used only for HDMI 1.4 3D 1080p format. 0x1: Secondary LCD output selected. 0x3: Write-back output to the memory selected.	RW	0x0
29	BURSTTYPE	The type of burst can be INCR (incremental) or BLCK (2D block). The 2D block is required when the TILER is targeted by the DMA engine. 0x0: INC burst type is used. 0x1: 2D block burst type is used.	RW	0

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Bits	Field Name	Description	Type	Reset
28	PREMULTIPLYALPHA	The field configures the DISPC VID2 to process incoming data as premultiplied alpha data or non premultiplied alpha data. Default setting is non premultiplied alpha data. 0x0: Non premultiplyalpha data color component 0x1: Premultiplyalpha data color component	RW	0
27:26	ZORDER	Z-Order defining the priority of the layer compared to others when overlaying. It is software responsibility to ensure that each layer connected to the same overlay manager has a different z-order value. If bit 25 is set to 0, the ZORDER bit field is ignored and replaced by the value 0. 0x0: Z-order 0: layer above solid background color and below layer with higher Z-order values. 0x1: Z-order 1: layer above layer with z-order value of 0 and below layers with z-order values of 2 and 3 0x3: Z-order 3: layer above all the other layers 0x2: Z-order 2: layer above layers with z-order value of 0 and 1 and below layer with z-order value of 3	RW	0x0
25	ZORDERENABLE	Z-order Enable. The bit field ZORDER is only used when the Z-order is enabled. 0x0: Z-order disabled. The Z-order of the layer is 0. 0x1: Z-order enabled. The Z-order is defined by the bit field ZORDER (bits 26 and 27).	RW	0
24	SELFREFRESH	Enables the self refresh of the video window from its own DMA buffer only. 0x0: The video pipeline accesses the interconnect to fetch data from the system memory. 0x1: The video pipeline does not need anymore to fetch data from memory. Only the DMA buffer associated with the video2 is used. It takes effect after the frame has been loaded in the DMA buffer.	RW	0
23	ARBITRATION	Determines the priority of the video pipeline. The video pipeline is one of the high priority pipeline. The arbitration gives always the priority first to the high priority pipelines using round-robin between them. When there is only normal priority pipelines sending requests, the round-robin applies between them. 0x0: The video pipeline is one of the normal priority pipeline. 0x1: The video pipeline is one of the high priority pipeline.	RW	0
22	DOUBLESTRIDE	Determines if the stride for CbCr buffer is the 1x or 2x of the Y buffer stride. It is only used in case of YUV4:2:0. 0x0: The CbCr stride value is equal to the Y stride. 0x1: The CbCr stride value is double to the Y stride.	RW	0
21	VERTICALTAPS	Video Vertical Resize Tap Number 0x0: 3 taps are used for the vertical filtering logic. The 2 other taps are not used. The associated bit fields for the 2 other taps coefficients do not need to be initialized. 0x1: 5 taps are used for the vertical filtering logic.	RW	0
20	DMAOPTIMIZATION	Write 0s for future compatibility. Reads return 0.	R	0
19	BUFPRELOAD	Video Preload Value 0x0: Hardware prefetches pixels up to the preload value defined in the preload register 0x1: Hardware prefetches pixels up to high threshold value	RW	0

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Bits	Field Name	Description	Type	Reset
18	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0
17	SELFREFRESHAUTO	Automatic self-refresh mode 0x0: The transition from SELFREFRESH "disabled" to "enabled" is controlled by SW. 0x1: The transition from SELFREFRESH "disabled" to "enabled" is controlled only by hardware.	RW	0
16	CHANNELOUT	Video Channel Out configuration: LCD, WB or TV. wr: immediate 0x0: LCD output or WB to the memory selected. bit fields 31 and 30 defines the output associated (primary, secondary or write-back). 0x1: TV output selected	RW	0
15:14	BURSTSIZE	Video DMA Burst Size 0x0: 2x128bit bursts 0x1: 4x128bit bursts 0x3: Reserved 0x2: 8x128bit bursts	RW	0x2
13:12	ROTATION	Video Rotation Flag 0x0: No rotation 0x1: Rotation by 90 degrees 0x3: Rotation by 270 degrees 0x2: Rotation by 180 degrees	RW	0x0
11	FULLRANGE	Color Space Conversion full range setting. 0x0: Limited range selected: 16 subtracted from Y before color space conversion 0x1: Full range selected: Y is not modified before the color space conversion	RW	0
10	REPLICATIONENABLE	Replication Enable 0x0: Disable Video replication logic 0x1: Enable Video replication logic	RW	1
9	COLORCONVENABLE	Enable the color space conversion. The hardware does not enable/disable the conversion based on the pixel format. The bit field shall be reset when the format is not YUV. 0x0: Disable Color Space Conversion YUV to RGB 0x1: Enable Color Space Conversion YUV to RGB	RW	0
8	VRESIZECONF	Write 0s for future compatibility. Reads return 0.	R	0
7	HRESIZECONF	Write 0s for future compatibility. Reads return 0.	R	0
6:5	RESIZEENABLE	Video Resize Enable 0x0: Disable both horizontal and vertical resize processing 0x1: Enable the horizontal resize processing 0x3: Enable both horizontal and vertical resize processing 0x2: Enable the vertical resize processing	RW	0x0

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Bits	Field Name	Description	Type	Reset
4:1	FORMAT	Video Format. It defines the pixel format when fetching the video 2 picture into memory. 0x6: RGB16-565 0x1: RGB12x-4444 0xA: YUV2 4:2:2 co-sited 0x7: ARGB16-1555 0xD: RGBA32-8888 0x0: NV12 4:2:0 2 buffers (Y + UV) 0x2: RGBA12-4444 0x8: xRGB24-8888 (32-bit container) 0x9: RGB24-888 (24-bit container) 0xB: UYVY 4:2:2 co-sited 0x5: ARGB16-4444 0xF: xRGB15-1555 0xC: ARGB32-8888 0x4: xRGB12-4444 0xE: RGBx24-8888 (24-bit RGB aligned on MSB of the 32-bit container)	RW	0x0
0	ENABLE	VidEnable 0x0: Video disabled (video pipeline inactive and window not present) 0x1: Video enabled (video pipeline active and window present on the screen)	RW	0

Table 10-238. Register Call Summary for Register DISPC_VID2_ATTRIBUTES

Display Controller

- Overlay Manager: [0] [1]
- Timing and TV Format Settings: [2]
- Shadow Registers: [3]
- Display Controller Logical Register Mapping: [4]
- Display Controller Register Summary: [5]

Table 10-239. DISPC_VID2_BUF_THRESHOLD

Address Offset	0x0000 0160		
Physical Address	0x4804 1160 0x5800 1160	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the DMA buffer associated with the video pipeline 2. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BUFHIGHTHRESHOLD																BUFLOWTHRESHOLD															

Bits	Field Name	Description	Type	Reset
31:16	BUFHIGHTHRESHOLD	DMA buffer High Threshold Number of 128-bits defining the threshold value.	RW	0x07FF
15:0	BUFLOWTHRESHOLD	DMA buffer High Threshold Number of 128-bits defining the threshold value.	RW	0x07F8

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Table 10-240. Register Call Summary for Register DISPC_VID2_BUF_THRESHOLD

Display Controller

- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1]
- Display Controller Register Summary: [2]

Table 10-241. DISPC_VID2_BUF_SIZE_STATUS

Address Offset	0x0000 0164		
Physical Address	0x4804 1164 0x5800 1164	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register defines the DMA buffer size for the video pipeline 2.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																BUFSIZE															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0000
15:0	BUFSIZE	DMA buffer size in number of 128 bits	R	0x0800

Table 10-242. Register Call Summary for Register DISPC_VID2_BUF_SIZE_STATUS

Display Controller

- Shadow Registers: [0]
- Display Controller Register Summary: [1]

Table 10-243. DISPC_VID2_ROW_INC

Address Offset	0x0000 0168		
Physical Address	0x4804 1168 0x5800 1168	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the number of bytes to increment at the end of the row for the buffer associated with the video window 2. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ROWINC																															

Bits	Field Name	Description	Type	Reset
31:0	ROWINC	Number of bytes to increment at the end of the row Encoded signed value (from $2^{31}1$ to 2^{31}) to specify the number of bytes to increment at the end of the row in the video buffer. The value 0 is invalid. The value 1 means next pixel. The value 1 + n * bpp means increment of n pixels. The value 1 (n + 1) * bpp means decrement of n pixels.	RW	0x0000 0001

Table 10-244. Register Call Summary for Register DISPC_VID2_ROW_INC

Display Controller

- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1]
- Display Controller Register Summary: [2]

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Table 10-245. DISPC_VID2_PIXEL_INC

Address Offset	0x0000 016C		
Physical Address	0x4804 116C 0x5800 116C	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the number of bytes to increment between two pixels for the buffer associated with the video window 2. For more information, see Section 10.2.4.6.3, *Predecimation*. The register is used only when the TILER is not present in the system in order to perform low performance rotation. When the TILER IP is present it is highly recommended to use it for performing the rotation. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								PIXELINC							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x000000
7:0	PIXELINC	Number of bytes to increment between two pixels. Encoded unsigned value (from 1 to 255) to specify the number of bytes between two pixels in the video buffer. The value 0 is invalid. The value 1 means next pixel. The value 1+n*bpp means increment of n pixels. For YUV4:2:0, Max supported value is 128.	RW	0x01

Table 10-246. Register Call Summary for Register DISPC_VID2_PIXEL_INC

Display Controller

- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1]
- Display Controller Register Summary: [2]

Table 10-247. DISPC_VID2_FIR

Address Offset	0x0000 0170		
Physical Address	0x4804 1170 0x5800 1170	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the resize factors for horizontal and vertical up/downsampling of the video window 2. It is used for ARGB and Y setting. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			FIRVINC													RESERVED			FIRHINC												

Bits	Field Name	Description	Type	Reset
31:29	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0
28:16	FIRVINC	Vertical increment of the up/downsampling filter Encoded value (from 1 to 4096). The value 0 is invalid. The values greater than 4096 are invalid.	RW	0x0400
15:13	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0

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Bits	Field Name	Description	Type	Reset
12:0	FIRHINC	Horizontal increment of the up/downsampling filter Encoded value (from 1 to 4096). The value 0 is invalid. The values greater than 4096 are invalid.	RW	0x0400

Table 10-248. Register Call Summary for Register DISPC_VID2_FIR

Display Controller

- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1]
- Display Controller Register Summary: [2]

Table 10-249. DISPC_VID2_PICTURE_SIZE

Address Offset	0x0000 0174		
Physical Address	0x4804 1174 0x5800 1174	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the size of the video picture associated with the video layer 2 before up/down-scaling. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								ORGSIZEY								RESERVED								ORGSIZEX							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
26:16	ORGSIZEY	Number of lines of the video picture Encoded value (from 1 to 2048) to specify the number of lines of the video picture in memory (program to value minus 1). When predecimation is set, the value represents the size of the image after predecimation but the max size of the unpredecimated image size in memory is still bounded 2^{11}.	RW	0x000
15:11	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
10:0	ORGSIZEX	Number of pixels of the video picture Encoded value (from 1 to 2048) to specify the number of pixels of the video picture in memory (program to value minus 1). The size is limited to the size of the line buffer of the vertical sampling block in case the video picture is processed by the vertical filtering unit. (program to value minus 1). When predecimation is set, the value represents the size of the image after predecimation but the max size of the unpredecimated image size in memory is still bounded 2^{11}.	RW	0x000

Table 10-250. Register Call Summary for Register DISPC_VID2_PICTURE_SIZE

Display Controller

- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1]
- Display Controller Register Summary: [2]

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Table 10-251. DISPC_VID2_ACCU_j

Address Offset	0x0000 0178 + (0x4 * j)	**Index**	j = 0 to 1
Physical Address	0x4804 1178 + (0x4 * j) 0x5800 1178 + (0x4 * j)	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the resize accumulator init values for horizontal and vertical up/downsampling of the video window 2 (DISPC_VID2_ACCU_0 DISPC_VID2_ACCU_1 for ping-pong mechanism with external trigger, based on the field polarity). It is used for ARGB and Y setting. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								VERTICALACCU								RESERVED								HORIZONTALACCU							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
26:16	VERTICALACCU	Vertical initialization accu value Encoded value (from -1024 to 1023).	RW	0x000
15:11	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
10:0	HORIZONTALACCU	Horizontal initialization accu value Encoded value (from -1024 to 1023).	RW	0x000

Table 10-252. Register Call Summary for Register DISPC_VID2_ACCU_j

Display Controller

- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1] [2]
- Display Controller Register Summary: [3]

Table 10-253. DISPC_VID2_FIR_COEF_H_i

Address Offset	0x0000 0180 + (0x8 * i)	**Index**	i = 0 to 7
Physical Address	0x4804 1180 + (0x8 * i) 0x5800 1180 + (0x8 * i)	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The bank of registers configure the up/down-scaling coefficients for the horizontal resize of the video picture associated with the video window 2 for the phases from 0 to 7. It is used for ARGB and Y setting. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIRHC3								FIRHC2								FIRHC1								FIRHC0							

Bits	Field Name	Description	Type	Reset
31:24	FIRHC3	Signed coefficient C3 for the horizontal up/down-scaling with the phase n	RW	0x00
23:16	FIRHC2	Unsigned coefficient C2 for the horizontal up/down-scaling with the phase n	RW	0x00
15:8	FIRHC1	Signed coefficient C1 for the horizontal up/down-scaling with the phase n	RW	0x00
7:0	FIRHC0	Signed coefficient C0 for the horizontal up/down-scaling with the phase n	RW	0x00

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Table 10-254. Register Call Summary for Register DISPC_VID2_FIR_COEF_H_i

Display Controller

- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1]
- Display Controller Register Summary: [2]

Table 10-255. DISPC_VID2_FIR_COEF_HV_i

Address Offset	0x0000 0184 + (0x8 * i)	**Index**	i = 0 to 7
Physical Address	0x4804 1184 + (0x8 * i) 0x5800 1184 + (0x8 * i)	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The bank of registers configure the down/up/down-scaling coefficients for the vertical and horizontal resize of the video picture associated with the video window 2 for the phases from 0 to 7. It is used for ARGB and Y setting. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIRVC2								FIRVC1								FIRVC0								FIRHC4							

Bits	Field Name	Description	Type	Reset
31:24	FIRVC2	Signed coefficient C2 for the vertical up/down-scaling with the phase n	RW	0x00
23:16	FIRVC1	Unsigned coefficient C1 for the vertical up/down-scaling with the phase n	RW	0x00
15:8	FIRVC0	Signed coefficient C0 for the vertical up/down-scaling with the phase n	RW	0x00
7:0	FIRHC4	Signed coefficient C4 for the horizontal up/down-scaling with the phase n	RW	0x00

Table 10-256. Register Call Summary for Register DISPC_VID2_FIR_COEF_HV_i

Display Controller

- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1]
- Display Controller Register Summary: [2]

Table 10-257. DISPC_VID2_CONV_COEF0

Address Offset	0x0000 01C0		
Physical Address	0x4804 11C0 0x5800 11C0	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the color space conversion matrix coefficients for the video pipeline 2. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								RCR								RESERVED								RY							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
26:16	RCR	RCr Coefficient Encoded signed value (from -1024 to 1023).	RW	0x000
15:11	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00

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Bits	Field Name	Description	Type	Reset
10:0	RY	RY Coefficient Encoded signed value (from -1024 to 1023).	RW	0x000

Table 10-258. Register Call Summary for Register DISPC_VID2_CONV_COEF0

Display Controller

- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1]
- Display Controller Register Summary: [2]

Table 10-259. DISPC_VID2_CONV_COEF1

Address Offset	0x0000 01C4		
Physical Address	0x4804 11C4 0x5800 11C4	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the color space conversion matrix coefficients for the video pipeline 2. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								GY								RESERVED								RCB							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
26:16	GY	GY Coefficient Encoded signed value (from -1024 to 1023).	RW	0x000
15:11	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
10:0	RCB	RCb Coefficient Encoded signed value (from -1024 to 1023).	RW	0x000

Table 10-260. Register Call Summary for Register DISPC_VID2_CONV_COEF1

Display Controller

- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1]
- Display Controller Register Summary: [2]

Table 10-261. DISPC_VID2_CONV_COEF2

Address Offset	0x0000 01C8		
Physical Address	0x4804 11C8 0x5800 11C8	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the color space conversion matrix coefficients for the video pipeline 2. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								GCB								RESERVED								GCR							

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Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
26:16	GCB	GCb Coefficient Encoded signed value (from -1024 to 1023).	RW	0x000
15:11	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
10:0	GCR	GCr Coefficient Encoded signed value (from -1024 to 1023).	RW	0x000

Table 10-262. Register Call Summary for Register DISPC_VID2_CONV_COEF2

Display Controller

- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1]
- Display Controller Register Summary: [2]

Table 10-263. DISPC_VID2_CONV_COEF3

Address Offset	0x0000 01CC		
Physical Address	0x4804 11CC 0x5800 11CC	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the color space conversion matrix coefficients for the video pipeline 2. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								BCR								RESERVED								BY							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
26:16	BCR	BCr coefficient Encoded signed value (from -1024 to 1023).	RW	0x000
15:11	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
10:0	BY	BY coefficient Encoded signed value (from -1024 to 1023).	RW	0x000

Table 10-264. Register Call Summary for Register DISPC_VID2_CONV_COEF3

Display Controller

- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1]
- Display Controller Register Summary: [2]

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Table 10-265. DISPC_VID2_CONV_COEF4

Address Offset	0x0000 01D0		
Physical Address	0x4804 11D0 0x5800 11D0	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the color space conversion matrix coefficients for the video pipeline 2. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								BCB							

Bits	Field Name	Description	Type	Reset
31:11	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x000000
10:0	BCB	BCb Coefficient Encoded signed value (from -1024 to 1023).	RW	0x000

Table 10-266. Register Call Summary for Register DISPC_VID2_CONV_COEF4

Display Controller

- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1]
- Display Controller Register Summary: [2]

Table 10-267. DISPC_DATA1_CYCLE1

Address Offset	0x0000 01D4		
Physical Address	0x4804 11D4 0x5800 11D4	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The control register configures the output data format for 1st cycle. Shadow register, updated on VFP start period of primary LCD		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				BITALIGNMENTPIXEL2				RESERVED			NBBITSPIXEL2					RESERVED				BITALIGNMENTPIXEL1				RESERVED				NBBITSPIXEL1			

Bits	Field Name	Description	Type	Reset
31:28	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0
27:24	BITALIGNMENTPIXEL2	Bit alignment. Alignment of the bits from pixel 2 on the output interface	RW	0x0
23:21	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0
20:16	NBBITSPIXEL2	Number of bits Number of bits from the pixel 2 (value from 0 to 16 bits). The values from 17 to 31 are invalid.	RW	0x00
15:12	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0
11:8	BITALIGNMENTPIXEL1	Bit alignment. Alignment of the bits from pixel 1 on the output interface	RW	0x0
7:5	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0
4:0	NBBITSPIXEL1	Number of bits Number of bits from the pixel 1 (value from 0 to 16 bits). The values from 17 to 31 are invalid.	RW	0x00

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Table 10-268. Register Call Summary for Register DISPC_DATA1_CYCLE1

Display Controller

- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1]
- Display Controller Register Summary: [2]

Table 10-269. DISPC_DATA1_CYCLE2

Address Offset	0x0000 01D8		
Physical Address	0x4804 11D8 0x5800 11D8	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The control register configures the output data format for 2nd cycle. Shadow register, updated on VFP start period of primary LCD		
Type	RW		

31 30 29 28	27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
RESERVED	BITALIGNMENTPIXEL2	RESERVED / NBBITSPIXEL2	RESERVED / BITALIGNMENTPIXEL1	RESERVED / NBBITSPIXEL1

Bits	Field Name	Description	Type	Reset
31:28	RESERVED	Write 0s for future compatibility Reads return 0.	R	0x0
27:24	BITALIGNMENTPIXEL2	Bit alignment. Alignment of the bits from pixel 2 on the output interface	RW	0x0
23:21	RESERVED	Write 0s for future compatibility Reads return 0.	R	0x0
20:16	NBBITSPIXEL2	Number of bits Number of bits from the pixel 2 (value from 0 to 16 bits). The values from 17 to 31 are invalid.	RW	0x00
15:12	RESERVED	Write 0s for future compatibility Reads return 0.	R	0x0
11:8	BITALIGNMENTPIXEL1	Bit alignment. Alignment of the bits from pixel 1 on the output interface	RW	0x0
7:5	RESERVED	Write 0s for future compatibility Reads return 0.	R	0x0
4:0	NBBITSPIXEL1	Number of bits Number of bits from the pixel 1 (value from 0 to 16 bits). The values from 17 to 31 are invalid.	RW	0x00

Table 10-270. Register Call Summary for Register DISPC_DATA1_CYCLE2

Display Controller

- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1]
- Display Controller Register Summary: [2]

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Table 10-271. DISPC_DATA1_CYCLE3

Address Offset	0x0000 01DC		
Physical Address	0x4804 11DC 0x5800 11DC	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The control register configures the output data format for 3rd cycle. Shadow register, updated on VFP start period of primary LCD		
Type	RW		

31 30 29 28	27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5	4 3 2 1 0
RESERVED	BITALIGNMENTPIXEL2	RESERVED / NBBITSPIXEL2	RESERVED / BITALIGNMENTPIXEL1	RESERVED	NBBITSPIXEL1

Bits	Field Name	Description	Type	Reset
31:28	RESERVED	Write 0s for future compatibility Reads return 0.	R	0x0
27:24	BITALIGNMENTPIXEL2	Bit alignment. Alignment of the bits from pixel 2 on the output interface	RW	0x0
23:21	RESERVED	Write 0s for future compatibility Reads return 0.	R	0x0
20:16	NBBITSPIXEL2	Number of bits Number of bits from the pixel 2 (value from 0 to 16 bits). The values from 17 to 31 are invalid.	RW	0x00
15:12	RESERVED	Write 0s for future compatibility Reads return 0.	R	0x0
11:8	BITALIGNMENTPIXEL1	Bit alignment. Alignment of the bits from pixel 1 on the output interface	RW	0x0
7:5	RESERVED	Write 0s for future compatibility Reads return 0.	R	0x0
4:0	NBBITSPIXEL1	Number of bits Number of bits from the pixel 1 (value from 0 to 16 bits). The values from 17 to 31 are invalid.	RW	0x00

Table 10-272. Register Call Summary for Register DISPC_DATA1_CYCLE3

Display Controller

- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1]
- Display Controller Register Summary: [2]

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Table 10-273. DISPC_VID1_FIR_COEF_V_i

Address Offset	0x0000 01E0 + (0x4 * i)	**Index**	i = 0 to 7
Physical Address	0x4804 11E0 + (0x4 * i) 0x5800 11E0 + (0x4 * i)	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The bank of registers configure the down/up/down-scaling coefficients for the vertical resize of the video picture associated with the video window 1 for the phases from 0 to 7. It is used for ARGB and Y setting. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																FIRVC22								FIRVC00							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0000
15:8	FIRVC22	Signed coefficient C22 for the vertical up/down-scaling with the phase n	RW	0x00
7:0	FIRVC00	Signed coefficient C00 for the vertical up/down-scaling with the phase n	RW	0x00

Table 10-274. Register Call Summary for Register DISPC_VID1_FIR_COEF_V_i

Display Controller

- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1]
- Display Controller Register Summary: [2]

Table 10-275. DISPC_VID2_FIR_COEF_V_i

Address Offset	0x0000 0200 + (0x4 * i)	**Index**	i = 0 to 7
Physical Address	0x4804 1200 + (0x4 * i) 0x5800 1200 + (0x4 * i)	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The bank of registers configure the down/up/down-scaling coefficients for the vertical resize of the video picture associated with the video window 2 for the phases from 0 to 7. It is used for ARGB and Y setting. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																FIRVC22								FIRVC00							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0000
15:8	FIRVC22	Signed coefficient C22 for the vertical up/down-scaling with the phase n	RW	0x00
7:0	FIRVC00	Signed coefficient C00 for the vertical up/down-scaling with the phase n	RW	0x00

Table 10-276. Register Call Summary for Register DISPC_VID2_FIR_COEF_V_i

Display Controller

- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1]
- Display Controller Register Summary: [2]

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Table 10-277. DISPC_CPR1_COEF_R

Address Offset	0x0000 0220		
Physical Address	0x4804 1220 0x5800 1220	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the color phase rotation matrix coefficients for the Red component. It is used for the primary LCD output. Shadow register, updated on VFP start period of primary LCD		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RR										RESERVED						RG								RESERVED							
RB																															

Bits	Field Name	Description	Type	Reset
31:22	RR	RR Coefficient Encoded signed value (from -512 to 511).	RW	0x000
21	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0
20:11	RG	RG Coefficient Encoded signed value (from -512 to 511).	RW	0x000
10	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0
9:0	RB	RB Coefficient Encoded signed value (from -512 to 511).	RW	0x000

Table 10-278. Register Call Summary for Register DISPC_CPR1_COEF_R

Display Controller

- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1]
- Display Controller Register Summary: [2]

Table 10-279. DISPC_CPR1_COEF_G

Address Offset	0x0000 0224		
Physical Address	0x4804 1224 0x5800 1224	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the color phase rotation matrix coefficients for the Green component. It is used for the primary LCD output. Shadow register, updated on VFP start period of primary LCD		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GR										RESERVED						GG								RESERVED							
GB																															

Bits	Field Name	Description	Type	Reset
31:22	GR	GR Coefficient Encoded signed value (from -512 to 511).	RW	0x000
21	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0
20:11	GG	GG Coefficient Encoded signed value (from -512 to 511).	RW	0x000
10	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0
9:0	GB	GB Coefficient Encoded signed value (from -512 to 511).	RW	0x000

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Table 10-280. Register Call Summary for Register DISPC_CPR1_COEF_G

Display Controller

- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1]
- Display Controller Register Summary: [2]

Table 10-281. DISPC_CPR1_COEF_B

Address Offset	0x0000 0228		
Physical Address	0x4804 1228 0x5800 1228	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the color phase rotation matrix coefficients for the Blue component. It is used for the primary LCD output. Shadow register, updated on VFP start period of primary LCD		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BR										RESERVED						BG					RESERVED			BB							

Bits	Field Name	Description	Type	Reset
31:22	BR	BR Coefficient Encoded signed value (from -512 to 511).	RW	0x000
21	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0
20:11	BG	BG Coefficient Encoded signed value (from -512 to 511).	RW	0x000
10	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0
9:0	BB	BB Coefficient Encoded signed value (from -512 to 511).	RW	0x000

Table 10-282. Register Call Summary for Register DISPC_CPR1_COEF_B

Display Controller

- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1]
- Display Controller Register Summary: [2]

Table 10-283. DISPC_GFX_PRELOAD

Address Offset	0x0000 022C		
Physical Address	0x4804 122C 0x5800 122C	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the graphics DMA buffer Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								PRELOAD							

Bits	Field Name	Description	Type	Reset
31:12	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00000
11:0	PRELOAD	DMA buffer preload value Number of 128-bit words defining the preload value.	RW	0x100

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Table 10-284. Register Call Summary for Register DISPC_GFX_PRELOAD

Display Controller

- DMA Buffers: [0]
- Shadow Registers: [1]
- Operational Modes Configuration: [2]
- Display Controller Register Summary: [3]

Table 10-285. DISPC_VID1_PRELOAD

Address Offset	0x0000 0230		
Physical Address	0x4804 1230 0x5800 1230	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the DMA buffer of the video 1 pipeline. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				PRELOAD											

Bits	Field Name	Description	Type	Reset
31:12	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00000
11:0	PRELOAD	DMA buffer preload value Number of 128-bit words defining the preload value.	RW	0x100

Table 10-286. Register Call Summary for Register DISPC_VID1_PRELOAD

Display Controller

- Shadow Registers: [0]
- Display Controller Register Summary: [1]

Table 10-287. DISPC_VID2_PRELOAD

Address Offset	0x0000 0234		
Physical Address	0x4804 1234 0x5800 1234	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the DMA buffer of the video 2 pipeline. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				PRELOAD											

Bits	Field Name	Description	Type	Reset
31:12	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00000
11:0	PRELOAD	DMA buffer preload value Number of 128-bit words defining the preload value.	RW	0x100

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Table 10-288. Register Call Summary for Register DISPC_VID2_PRELOAD

Display Controller

- Shadow Registers: [0]
- Display Controller Register Summary: [1]

Table 10-289. DISPC_CONTROL2

Address Offset	0x0000 0238		
Physical Address	0x4804 1238 0x5800 1238	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The control register configures the Display Controller module for the secondary LCD output.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPATIALTEMPORALDITHERINGFRAMES		RESERVED			TDMUNUSEDBITS		TDMCYCLEFORMAT		TDMPARALLELMODE		TDMENABLE	RESERVED						TVOVERLAYOPTIMIZATION	OVERLAYOPTIMIZATION	STALLMODE	RESERVED		TFTDATALINES		STDITHERENABLE	GOWB	GOLCD	M8B	STNTFT	MONOCOLOR	RESERVED	LCDENABLE

Bits	Field Name	Description	Type	Reset
31:30	SPATIALTEMPORAL DITHERINGFRAMES	Spatial/Temporal dithering number of frames for the secondary LCD output wr: VFP start period of secondary LCD output 0x0: Spatial only 0x1: Spatial and temporal over 2 frames 0x2: Spatial and temporal over 4 frames 0x3: Reserved	RW	0x0
29:27	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0
26:25	TDMUNUSED BITS	State of unused bits (TDM mode only) for the secondary LCD output wr: VFP start period of secondary LCD output 0x0: low level (0) 0x1: high level (1) 0x2: unchanged from previous state 0x3: reserved	RW	0x0
24:23	TDMCYCLE FORMAT	Cycle format (TDM mode only) for the secondary LCD output wr: VFP start period of secondary LCD output 0x0: 1 cycle for 1 pixel 0x1: 2 cycles for 1 pixel 0x2: 3 cycles for 1 pixel 0x3: 3 cycles for 2 pixels	RW	0x0

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Bits	Field Name	Description	Type	Reset
22:21	TDMPARALLEL MODE	Output Interface width (TDM mode only) for the secondary LCD output wr: VFP start period of secondary LCD output 0x0: 8-bit parallel output interface selected 0x1: 9-bit parallel output interface selected 0x2: 12-bit parallel output interface selected 0x3: 16-bit parallel output interface selected	RW	0x0
20	TDMENABLE	Enable the multiple cycle format (TDM mode only used for Active Matrix mode with the RFBI enable bit off) for the secondary LCD output wr: VFP start period of secondary LCD output 0x0: TDM disabled 0x1: TDM enabled	RW	0
19:14	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
13	TVOVERLAY OPTIMIZATION	Overlay Optimization for the TV output wr: VFP or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory 0x0: All the data for all the enabled pipelines are fetched from memory regardless of the overlay/alpha blending configuration. 0x1: The data not used by the overlay manager because of overlap between layers with no alpha blending between them shall not be fetched from memory in order to optimize the bandwidth.	RW	0
12	OVERLAY OPTIMIZATION	Overlay Optimization for the secondary LCD output wr: VFP or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory 0x0: All the data for all the enabled pipelines are fetched from memory regardless of the overlay/alpha blending configuration. 0x1: The data not used by the overlay manager because of overlap between layers with no alpha blending between them shall not be fetched from memory in order to optimize the bandwidth.	RW	0
11	STALLMODE	STALL Mode for the secondary LCD output wr: VFP start period of secondary LCD output 0x0: Normal mode selected 0x1: STALL mode selected. The Display Controller sends the data without considering the VSYNC/HSYNC. The LCD output is disabled at the end of the transfer of the frame. The S/W has to re-enable the LCD output in order to generate a new frame.	RW	0
10	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0
9:8	TFTDATALINES	Number of lines of the secondary LCD interface wr: VFP start period of secondary LCD output 0x0: 12-bit output aligned on the LSB of the pixel data interface 0x1: 16-bit output aligned on the LSB of the pixel data interface 0x2: 18-bit output aligned on the LSB of the pixel data interface 0x3: 24-bit output aligned on the LSB of the pixel data interface	RW	0x0
7	STDITHER ENABLE	Spatial Temporal dithering enable for the secondary LCD output wr: VFP start period of secondary LCD output 0x0: Spatial/Temporal dithering logic disabled 0x1: Spatial/Temporal dithering logic enabled	RW	0

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Bits	Field Name	Description	Type	Reset
6	GOWB	GO Command for the write-back output. It is used to synchronized the pipelines (graphics and/or video ones) associated with the write-back output to the memory. wr:immediate 0x0: The hardware has finished updating the internal shadow registers of the pipeline(s) connected to the write-back pipeline using the user values. The hardware resets the bit when the update is completed. 0x1: The user has finished to program the shadow registers of the pipeline(s) associated with the write-back pipeline and the hardware can update the internal registers immediately	RW	0
5	GOLCD	GO Command for the secondary LCD output. It is used to synchronized the pipelines (graphics and/or video ones) associated with the secondary LCD output. wr:immediate 0x0: The hardware has finished updating the internal shadow registers of the pipeline(s) connected to the LCD output using the user values. The hardware resets the bit when the update is completed. 0x1: The user has finished to program the shadow registers of the pipeline(s) associated with the LCD output and the hardware can update the internal registers at the VFP start period	RW	0
4	M8B	Mono 8-bit mode of the secondary LCD wr: VFP start period of secondary LCD output 0x0: Pixel data [3:0] is used to output four pixel values to the panel at each pixel clock transition. (only in Passive Mono 4-bit mode). 0x1: Pixel data [7:0] is used to output eight pixel values to the panel each pixel clock transition. (only in Passive Mono 8-bit mode).	RW	0
3	STNTFT	LCD Display type of the secondary LCD wr: VFP start period of secondary LCD output 0x0: Passive Matrix display operation enabled. Passive Matrix dither logic is enabled. 0x1: Active or TFT display operation enabled. STN Dither logic and output FIFO bypassed.	RW	0
2	MONOCOLOR	Monochrome/Color selection for the secondary LCD wr: VFP start period of secondary LCD output 0x0: Color operation enabled (Passive Matrix mode only) 0x1: Monochrome operation enabled (Passive Matrix mode only)	RW	0
1	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0
0	LCDENABLE	Enable the secondary LCD output wr:immediate 0x0: LCD output disabled (at the end of the frame when the bit is reset) 0x1: LCD output enabled	RW	0

Table 10-290. Register Call Summary for Register DISPC_CONTROL2

Display Controller

- Overlay Manager: [0] [1]
- Shadow Registers: [2] [3] [4] [5]
- Operational Modes Configuration: [6] [7] [8] [9] [10] [11] [12] [13]
- Display Controller Logical Register Mapping: [14]
- Display Controller Register Summary: [15]
- Display Controller Register Description: [16] [17] [18] [19] [20] [21] [22] [23] [24] [25] [26] [27] [28] [29] [30] [31] [32] [33] [34] [35] [36] [37] [38] [39] [40] [41] [42] [43] [44] [45] [46] [47] [48] [49] [50] [51] [52] [53] [54] [55] [56] [57] [58] [59] [60] [61] [62] [63] [64] [65] [66] [67] [68] [69] [70] [71] [72] [73] [74] [75] [76] [77] [78] [79] [80] [81] [82] [83] [84] [85] [86] [87] [88] [89] [90] [91] [92] [93] [94] [95] [96] [97] [98] [99] [100] [101] [102] [103] [104] [105] [106] [107] [108] [109] [110] [111] [112] [113] [114] [115] [116] [117] [118] [119] [120] [121] [122] [123] [124] [125] [126] [127] [128] [129] [130] [131] [132] [133] [134]

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Table 10-291. DISPC_VID3_ACCU_j

Address Offset	0x0000 0300 + (0x4 * j)	**Index**	j = 0 to 1
Physical Address	0x4804 1300 + (0x4 * j) 0x5800 1300 + (0x4 * j)	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the resize accumulator init values for horizontal and vertical up/downsampling of the video window 3 (DISPC_VID3_ACCU_0 DISPC_VID3_ACCU_1 for ping-pong mechanism with external trigger, based on the field polarity). It is used for ARGB and Y setting. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								VERTICALACCU								RESERVED								HORIZONTALACCU							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
26:16	VERTICALACCU	Vertical initialization accu value Encoded value (from -1024 to 1023).	RW	0x000
15:11	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
10:0	HORIZONTALACCU	Horizontal initialization accu value Encoded value (from -1024 to 1023).	RW	0x000

Table 10-292. Register Call Summary for Register DISPC_VID3_ACCU_j

Display Controller

- Shadow Registers: [0]
- Display Controller Register Summary: [1]

Table 10-293. DISPC_VID3_BA_j

Address Offset	0x0000 0308 + (0x4 * j)	**Index**	j = 0 to 1
Physical Address	0x4804 1308 + (0x4 * j) 0x5800 1308 + (0x4 * j)	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the base address of the video buffer for the video window 3 (DISPC_VID3_BA_0 DISPC_VID3_BA_1 for ping-pong mechanism with external trigger, based on the field polarity otherwise only DISPC_VID3_BA_0 is used)). Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BA																															

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Bits	Field Name	Description	Type	Reset
31:0	BA	Video base address Base address of the video buffer (aligned on pixel size boundary except in case of RGB24 packed format, 4-pixel alignment is required; in case of YUV4:2:2, 2-pixel alignment is required, and YUV4:2:0, byte alignment is supported)). It case of YUV4:2:0 format, it indicates the base address of the Y buffer. When the TILER is addressed, the bits: [28:27] = 0x0 for 8-bit tiled [28:27] = 0x1 for 16-bit tiled [28:27] = 0x2 for 32-bit tiled [28:27] = 0x3 for page mode [31:29] = 0x0 for 0-degree view [31:29] = 0x1 for 180-degree view + mirroring [31:29] = 0x2 for 0-degree view + mirroring [31:29] = 0x3 for 180-degree view [31:29] = 0x4 for 270-degree view + mirroring [31:29] = 0x5 for 270-degree view [31:29] = 0x6 for 90-degree view [31:29] = 0x7 for 90-degree view + mirroring Otherwise the bits indicated the corresponding bit address to access the SDRAM.	RW	0x0000 0000

Table 10-294. Register Call Summary for Register DISPC_VID3_BA_j

Display Controller

- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1]
- Display Controller Register Summary: [2]

Table 10-295. DISPC_VID3_FIR_COEF_H_i

Address Offset	0x0000 0310 + (0x8 * i)	**Index**	i = 0 to 7
Physical Address	0x4804 1310 + (0x8 * i) 0x5800 1310 + (0x8 * i)	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The bank of registers configure the up/down-scaling coefficients for the horizontal resize of the video picture associated with the video window 3 for the phases from 0 to 7. It is used for ARGB and Y setting. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIRHC3								FIRHC2								FIRHC1								FIRHC0							

Bits	Field Name	Description	Type	Reset
31:24	FIRHC3	Signed coefficient C3 for the horizontal up/down-scaling with the phase n	RW	0x00
23:16	FIRHC2	Unsigned coefficient C2 for the horizontal up/down-scaling with the phase n	RW	0x00
15:8	FIRHC1	Signed coefficient C1 for the horizontal up/down-scaling with the phase n	RW	0x00
7:0	FIRHC0	Signed coefficient C0 for the horizontal up/down-scaling with the phase n	RW	0x00

Table 10-296. Register Call Summary for Register DISPC_VID3_FIR_COEF_H_i

Display Controller

- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1]
- Display Controller Register Summary: [2]

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Table 10-297. DISPC_VID3_FIR_COEF_HV_i

Address Offset	0x0000 0314 + (0x8 * i)	**Index**	i = 0 to 7
Physical Address	0x4804 1314 + (0x8 * i) 0x5800 1314 + (0x8 * i)	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The bank of registers configure the down/up/down-scaling coefficients for the vertical and horizontal resize of the video picture associated with the video window 3 for the phases from 0 to 7. It is used for ARGB and Y setting. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIRVC2								FIRVC1								FIRVC0								FIRHC4							

Bits	Field Name	Description	Type	Reset
31:24	FIRVC2	Signed coefficient C2 for the vertical up/down-scaling with the phase n	RW	0x00
23:16	FIRVC1	Unsigned coefficient C1 for the vertical up/down-scaling with the phase n	RW	0x00
15:8	FIRVC0	Signed coefficient C0 for the vertical up/down-scaling with the phase n	RW	0x00
7:0	FIRHC4	Signed coefficient C4 for the horizontal up/down-scaling with the phase n	RW	0x00

Table 10-298. Register Call Summary for Register DISPC_VID3_FIR_COEF_HV_i

Display Controller

- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1]
- Display Controller Register Summary: [2]

Table 10-299. DISPC_VID3_FIR_COEF_V_i

Address Offset	0x0000 0350 + (0x4 * i)	**Index**	i = 0 to 7
Physical Address	0x4804 1350 + (0x4 * i) 0x5800 1350 + (0x4 * i)	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The bank of registers configure the down/up/down-scaling coefficients for the vertical resize of the video picture associated with the video window 3 for the phases from 0 to 7. It is used for ARGB and Y setting. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																FIRVC22								FIRVC00							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0000
15:8	FIRVC22	Signed coefficient C22 for the vertical up/down-scaling with the phase n	RW	0x00
7:0	FIRVC00	Signed coefficient C00 for the vertical up/down-scaling with the phase n	RW	0x00

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Table 10-300. Register Call Summary for Register DISPC_VID3_FIR_COEF_V_i

Display Controller

- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1]
- Display Controller Register Summary: [2]

Table 10-301. DISPC_VID3_ATTRIBUTES

Address Offset	0x0000 0370		
Physical Address	0x4804 1370 0x5800 1370	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the attributes of the video window 3. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31 30	29	28	27 26	25 24	23	22	21	20	19	18	17	16	15 14	13 12	11	10	9	8	7	6	5	4	3	2	1	0
CHANNELOUT2	BURSTTYPE	PREMULTIPLYALPHA	ZORDER	ZORDERENABLE	SELFREFRESH	ARBITRATION	DOUBLESTRIDE	VERTICALTAPS	DMAOPTIMIZATION	BUFPRELOAD	RESERVED	SELFREFRESHAUTO	CHANNELOUT	BURSTSIZE	ROTATION	FULLRANGE	REPLICATIONENABLE	COLORCONVENABLE	VRESIZECONF	HRESIZECONF	RESIZEENABLE	FORMAT				ENABLE

Bits	Field Name	Description	Type	Reset
31:30	CHANNELOUT2	It is not used if CHANNELOUT is set to TV. Reserved when CHANNELOUT = 1 (should be set to zero) wr: immediate 0x0: primary LCD output selected. 0x1: Secondary LCD output selected. 0x3: Write-back output to the memory selected.	RW	0x0
29	BURSTTYPE	The type of burst can be INCR (incremental) or BLCK (2D block). The 2D block is required when the TILER is targeted by the DMA engine. 0x0: INC burst type is used. 0x1: 2D block burst type is used.	RW	0
28	PREMULTIPLYALPHA	The field configures the DISPC VID3 to process incoming data as premultiplied alpha data or non premultiplied alpha data. Default setting is non premultiplied alpha data. 0x0: Non premultiplyalpha data color component 0x1: Premultiplyalpha data color component	RW	0

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Bits	Field Name	Description	Type	Reset
27:26	ZORDER	Z-Order defining the priority of the layer compared to others when overlaying. It is software responsibility to ensure that each layer connected to the same overlay manager has a different z-order value. If bit 25 is set to 0, the ZORDER bit field is ignored and replaced by the value 0. 0x0: Z-order 0: layer above solid background color and below layer with higher Z-order values. 0x1: Z-order 1: layer above layer with z-order value of 0 and below layers with z-order values of 2 and 3 0x3: Z-order 3: layer above all the other layers 0x2: Z-order 2: layer above layers with z-order value of 0 and 1 and below layer with z-order value of 3	RW	0x0
25	ZORDERENABLE	Z-order Enable. The bit field ZORDER is only used when the Z-order is enabled. 0x0: Z-order disabled. The Z-order of the layer is 0. 0x1: Z-order enabled. The Z-order is defined by the bit field ZORDER (bits 26 and 27).	RW	0
24	SELFREFRESH	Enables the self refresh of the video window from its own DMA buffer only. 0x0: The video pipeline accesses the interconnect to fetch data from the system memory. 0x1: The video pipeline does not need anymore to fetch data from memory. Only the DMA buffer associated with the video3 is used. It takes effect after the frame has been loaded in the DMA buffer.	RW	0
23	ARBITRATION	Determines the priority of the video pipeline. The video pipeline is one of the high priority pipeline. The arbitration gives always the priority first to the high priority pipelines using round-robin between them. When there is only normal priority pipelines sending requests, the round-robin applies between them. 0x0: The video pipeline is one of the normal priority pipeline. 0x1: The video pipeline is one of the high priority pipeline.	RW	0
22	DOUBLESTRIDE	Determines if the stride for CbCr buffer is the 1x or 2x of the Y buffer stride. It is only used in case of YUV4:2:0. 0x0: The CbCr stride value is equal to the Y stride. 0x1: The CbCr stride value is double to the Y stride.	RW	0
21	VERTICALTAPS	Video Vertical Resize Tap Number 0x0: 3 taps are used for the vertical filtering logic. The 2 other taps are not used. The associated bit fields for the 2 other taps coefficients do not need to be initialized. 0x1: 5 taps are used for the vertical filtering logic.	RW	0
20	DMAOPTIMIZATION	Write 0s for future compatibility. Reads return 0.	R	0
19	BUFPRELOAD	Video Preload Value 0x0: Hardware prefetches pixels up to the preload value defined in the preload register 0x1: Hardware prefetches pixels up to high threshold value	RW	0
18	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0

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Bits	Field Name	Description	Type	Reset
17	SELFREFRESHAUTO	Automatic self-refresh mode 0x0: The transition from SELFREFRESH "disabled" to "enabled" is controlled by SW. 0x1: The transition from SELFREFRESH "disabled" to "enabled" is controlled only by hardware.	RW	0
16	CHANNELOUT	Video Channel Out configuration: LCD, WB or TV. wr: immediate 0x0: LCD output or WB to the memory selected. bit fields 31 and 30 defines the output associated (primary, secondary or write-back). 0x1: TV output selected	RW	0
15:14	BURSTSIZE	Video DMA Burst Size 0x0: 2x128bit bursts 0x1: 4x128bit bursts 0x3: Reserved 0x2: 8x128bit bursts	RW	0x2
13:12	ROTATION	Video Rotation Flag 0x0: No rotation 0x1: Rotation by 90 degrees 0x3: Rotation by 270 degrees 0x2: Rotation by 180 degrees	RW	0x0
11	FULLRANGE	Color Space Conversion full range setting. 0x0: Limited range selected: 16 subtracted from Y before color space conversion 0x1: Full range selected: Y is not modified before the color space conversion	RW	0
10	REPLICATIONENABLE	Replication Enable 0x0: Disable Video replication logic 0x1: Enable Video replication logic	RW	1
9	COLORCONVENABLE	Enable the color space conversion. The hardware does not enable/disable the conversion based on the pixel format. The bit field shall be reset when the format is not YUV. 0x0: Disable Color Space Conversion YUV to RGB 0x1: Enable Color Space Conversion YUV to RGB	RW	0
8	VRESIZECONF	Write 0s for future compatibility. Reads return 0.	R	0
7	HRESIZECONF	Write 0s for future compatibility. Reads return 0.	R	0
6:5	RESIZEENABLE	Video Resize Enable 0x0: Disable both horizontal and vertical resize processing 0x1: Enable the horizontal resize processing 0x3: Enable both horizontal and vertical resize processing 0x2: Enable the vertical resize processing	RW	0x0

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Bits	Field Name	Description	Type	Reset
4:1	FORMAT	Video Format. It defines the pixel format when fetching the video 3 picture into memory. 0x6: RGB16-565 0x1: RGB12x-4444 0xA: YUV2 4:2:2 co-sited 0x7: ARGB16-1555 0xD: RGBA32-8888 0x0: NV12 4:2:0 2 buffers (Y + UV) 0x2: RGBA12-4444 0x8: RGB24-8888 (32-bit container) 0x9: RGB24-888 (24-bit container) 0xB: UYVY 4:2:2 co-sited 0x5: ARGB16-4444 0xF: xRGB15-1555 0xC: ARGB32-8888 0x4: xRGB12-4444 0xE: RGBx24-8888 (24-bit RGB aligned on MSB of the 32-bit container)	RW	0x0
0	ENABLE	Video Enable 0x0: Video disabled (video pipeline inactive and window not present) 0x1: Video enabled (video pipeline active and window present on the screen)	RW	0

Table 10-302. Register Call Summary for Register DISPC_VID3_ATTRIBUTES

Display Controller

- Overlay Manager: [0]
- Shadow Registers: [1]
- Display Controller Logical Register Mapping: [2]
- Display Controller Register Summary: [3]

Table 10-303. DISPC_VID3_CONV_COEF0

Address Offset	0x0000 0374		
Physical Address	0x4804 1374 0x5800 1374	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the color space conversion matrix coefficients for the video pipeline 3. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								RCR								RESERVED								RY							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
26:16	RCR	RCr Coefficient Encoded signed value (from -1024 to 1023).	RW	0x000
15:11	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
10:0	RY	RY Coefficient Encoded signed value (from -1024 to 1023).	RW	0x000

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Table 10-304. Register Call Summary for Register DISPC_VID3_CONV_COEF0

Display Controller

- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1]
- Display Controller Register Summary: [2]

Table 10-305. DISPC_VID3_CONV_COEF1

Address Offset	0x0000 0378		
Physical Address	0x4804 1378 0x5800 1378	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the color space conversion matrix coefficients for the video pipeline 3. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								GY								RESERVED								RCB							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
26:16	GY	GY Coefficient Encoded signed value (from -1024 to 1023).	RW	0x000
15:11	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
10:0	RCB	RCb Coefficient Encoded signed value (from -1024 to 1023).	RW	0x000

Table 10-306. Register Call Summary for Register DISPC_VID3_CONV_COEF1

Display Controller

- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1]
- Display Controller Register Summary: [2]

Table 10-307. DISPC_VID3_CONV_COEF2

Address Offset	0x0000 037C		
Physical Address	0x4804 137C 0x5800 137C	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the color space conversion matrix coefficients for the video pipeline 3. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								GCB								RESERVED								GCR							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
26:16	GCB	GCb Coefficient Encoded signed value (from -1024 to 1023).	RW	0x000
15:11	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
10:0	GCR	GCr Coefficient Encoded signed value (from -1024 to 1023).	RW	0x000

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Table 10-308. Register Call Summary for Register DISPC_VID3_CONV_COEF2

Display Controller

- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1]
- Display Controller Register Summary: [2]

Table 10-309. DISPC_VID3_CONV_COEF3

Address Offset	0x0000 0380		
Physical Address	0x4804 1380 0x5800 1380	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the color space conversion matrix coefficients for the video pipeline 3. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								BCR								RESERVED								BY							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
26:16	BCR	BCr coefficient Encoded signed value (from -1024 to 1023).	RW	0x000
15:11	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
10:0	BY	BY coefficient Encoded signed value (from -1024 to 1023).	RW	0x000

Table 10-310. Register Call Summary for Register DISPC_VID3_CONV_COEF3

Display Controller

- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1]
- Display Controller Register Summary: [2]

Table 10-311. DISPC_VID3_CONV_COEF4

Address Offset	0x0000 0384		
Physical Address	0x4804 1384 0x5800 1384	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the color space conversion matrix coefficients for the video pipeline 3. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																					BCB										

Bits	Field Name	Description	Type	Reset
31:11	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x000000
10:0	BCB	BCb Coefficient Encoded signed value (from -1024 to 1023).	RW	0x000

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Table 10-312. Register Call Summary for Register DISPC_VID3_CONV_COEF4

Display Controller

- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1]
- Display Controller Register Summary: [2]

Table 10-313. DISPC_VID3_BUF_SIZE_STATUS

Address Offset	0x0000 0388		
Physical Address	0x4804 1388 0x5800 1388	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register defines the DMA buffer size for the video pipeline 3.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																BUFSIZE															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0000
15:0	BUFSIZE	DMA buffer Size in number of 128-bits.	R	0x0800

Table 10-314. Register Call Summary for Register DISPC_VID3_BUF_SIZE_STATUS

Display Controller

- Shadow Registers: [0]
- Display Controller Register Summary: [1]

Table 10-315. DISPC_VID3_BUF_THRESHOLD

Address Offset	0x0000 038C		
Physical Address	0x4804 138C 0x5800 138C	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the DMA buffer associated with the video pipeline 3. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BUFHIGHTHRESHOLD																BUFLOWTHRESHOLD															

Bits	Field Name	Description	Type	Reset
31:16	BUFHIGHTHRESHOLD	DMA buffer High Threshold Number of 128-bits defining the threshold value.	RW	0x07FF
15:0	BUFLOWTHRESHOLD	DMA buffer High Threshold Number of 128-bits defining the threshold value.	RW	0x07F8

Table 10-316. Register Call Summary for Register DISPC_VID3_BUF_THRESHOLD

Display Controller

- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1]
- Display Controller Register Summary: [2]

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Table 10-317. DISPC_VID3_FIR

Address Offset	0x0000 0390		
Physical Address	0x4804 1390 0x5800 1390	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the resize factors for horizontal and vertical up/downsampling of the video window 3. It is used for ARGB and Y setting. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								FIRVINC								RESERVED								FIRHINC							

Bits	Field Name	Description	Type	Reset
31:29	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0
28:16	FIRVINC	Vertical increment of the up/downsampling filter Encoded value (from 1 to 4096). The value 0 is invalid. The values greater than 4096 are invalid.	RW	0x0400
15:13	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0
12:0	FIRHINC	Horizontal increment of the up/downsampling filter Encoded value (from 1 to 4096). The value 0 is invalid. The values greater than 4096 are invalid.	RW	0x0400

Table 10-318. Register Call Summary for Register DISPC_VID3_FIR

Display Controller

- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1]
- Display Controller Register Summary: [2]

Table 10-319. DISPC_VID3_PICTURE_SIZE

Address Offset	0x0000 0394		
Physical Address	0x4804 1394 0x5800 1394	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the size of the video picture associated with the video layer 3 before up/down-scaling. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								ORGSIZEY								RESERVED								ORGSIZEX							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
26:16	ORGSIZEY	Number of lines of the video picture Encoded value (from 1 to 2048) to specify the number of lines of the video picture in memory (program to value minus 1). When predecimation is set, the value represents the size of the image after predecimation but the max size of the unpredecimated image size in memory is still bounded 2^{11}.	RW	0x000
15:11	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00

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Bits	Field Name	Description	Type	Reset
10:0	ORGSIZEX	Number of pixels of the video picture Encoded value (from 1 to 2048) to specify the number of pixels of the video picture in memory (program to value minus 1). The size is limited to the size of the line buffer of the vertical sampling block in case the video picture is processed by the vertical filtering unit. (program to value minus 1). When predecimation is set, the value represents the size of the image after predecimation but the max size of the unpredecimated image size in memory is still bounded 2^{11}.	RW	0x000

Table 10-320. Register Call Summary for Register DISPC_VID3_PICTURE_SIZE

Display Controller

- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1]
- Display Controller Register Summary: [2]

Table 10-321. DISPC_VID3_PIXEL_INC

Address Offset	0x0000 0398		
Physical Address	0x4804 1398 0x5800 1398	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the number of bytes to increment between two pixels for the buffer associated with the video window 3. For more information, see Section 10.2.4.6.3, *Predecimation*. The register is used only when the TILER is not present in the system in order to perform low performance rotation. When the TILER IP is present it is highly recommended to use it for performing the rotation. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								PIXELINC							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x000000
7:0	PIXELINC	Number of bytes to increment between two pixels. Encoded unsigned value (from 1 to 255) to specify the number of bytes between two pixels in the video buffer. The value 0 is invalid. The value 1 means next pixel. The value 1+n*bpp means increment of n pixels. For YUV4:2:0, Max supported value is 128.	RW	0x01

Table 10-322. Register Call Summary for Register DISPC_VID3_PIXEL_INC

Display Controller

- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1]
- Display Controller Register Summary: [2]

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Table 10-323. DISPC_VID3_POSITION

Address Offset	0x0000 039C		
Physical Address	0x4804 139C 0x5800 139C	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the position of the video window 3. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								POSY								RESERVED								POSX							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
26:16	POSY	Y position of the video window 2 Encoded value (from 0 to 2047) to specify the Y position of the video window 2 .The line at the top has the Y-position 0.	RW	0x000
15:11	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
10:0	POSX	X position of the video window 2 Encoded value (from 0 to 2047) to specify the X position of the video window 2. The first pixel on the left of the display screen has the X-position 0.	RW	0x000

Table 10-324. Register Call Summary for Register DISPC_VID3_POSITION

Display Controller

- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1]
- Display Controller Register Summary: [2]

Table 10-325. DISPC_VID3_PRELOAD

Address Offset	0x0000 03A0		
Physical Address	0x4804 13A0 0x5800 13A0	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the DMA buffer of the video 3 pipeline. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								PRELOAD							

Bits	Field Name	Description	Type	Reset
31:12	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00000
11:0	PRELOAD	DMA buffer preload value Number of 128-bit words defining the preload value.	RW	0x100

Table 10-326. Register Call Summary for Register DISPC_VID3_PRELOAD

Display Controller

- Shadow Registers: [0]
- Display Controller Register Summary: [1]

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Table 10-327. DISPC_VID3_ROW_INC

Address Offset	0x0000 03A4		
Physical Address	0x4804 13A4 0x5800 13A4	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the number of bytes to increment at the end of the row for the buffer associated with the video window 3. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ROWINC																															

Bits	Field Name	Description	Type	Reset
31:0	ROWINC	Number of bytes to increment at the end of the row Encoded signed value (from $2^{31}1$ to 2^{31}) to specify the number of bytes to increment at the end of the row in the video buffer. The value 0 is invalid. The value 1 means next pixel. The value 1 + n * bpp means increment of n pixels. The value 1 (n + 1) * bpp means decrement of n pixels.	RW	0x0000 0001

Table 10-328. Register Call Summary for Register DISPC_VID3_ROW_INC

Display Controller

- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1]
- Display Controller Register Summary: [2]

Table 10-329. DISPC_VID3_SIZE

Address Offset	0x0000 03A8		
Physical Address	0x4804 13A8 0x5800 13A8	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the size of the video window 3. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								SIZEY								RESERVED								SIZEX							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
26:16	SIZEY	Number of lines of the video 3 Encoded value (from 1 to 2048) to specify the number of lines of the video window 3. Program to value minus 1.	RW	0x000
15:11	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
10:0	SIZEX	Number of pixels of the video window 3 Encoded value (from 1 to 2048) to specify the number of pixels of the video window 3. Program to value minus 1.	RW	0x000

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Table 10-330. Register Call Summary for Register DISPC_VID3_SIZE

Display Controller

- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1]
- Display Controller Register Summary: [2]

Table 10-331. DISPC_DEFAULT_COLOR2

Address Offset	0x0000 03AC		
Physical Address	0x4804 13AC 0x5800 13AC	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The control register allows to configure the default solid background color for the secondary LCD Shadow register, updated on VFP start period of secondary LCD		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								DEFAULTCOLOR																							

Bits	Field Name	Description	Type	Reset
31:24	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
23:0	DEFAULTCOLOR	24-bit RGB color value to specify the default solid color to display when there is no data from the overlays.	RW	0x000000

Table 10-332. Register Call Summary for Register DISPC_DEFAULT_COLOR2

Display Controller

- Shadow Registers: [0]
- Display Controller Register Summary: [1]

Table 10-333. DISPC_TRANS_COLOR2

Address Offset	0x0000 03B0		
Physical Address	0x4804 13B0 0x5800 13B0	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register sets the transparency color value for the video/graphics overlays for the secondary LCD output. Shadow register, updated on VFP start period of the secondary LCD		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TRANSCOLORKEY																							

Bits	Field Name	Description	Type	Reset
31:24	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
23:0	TRANSCOLORKEY	Transparency Color Key Value in RGB format [0] BITMAP 1 (CLUT), [23,1] set to 0s [1:0] BITMAP 2 (CLUT), [23,2] set to 0s [3:0] BITMAP 4 (CLUT), [23,4] set to 0s [7:0] BITMAP 8 (CLUT), [23,8] set to 0s [11:0] RGB 12, [23,12] set to 0s [15:0] RGB 16, [23,16] set to 0s [23:0] RGB 24	RW	0x000000

Table 10-334. Register Call Summary for Register DISPC_TRANS_COLOR2

Display Controller

- Overlay Manager: [0]
- Shadow Registers: [1]
- Display Controller Register Summary: [2]

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Table 10-335. DISPC_CPR2_COEF_B

Address Offset	0x0000 03B4		
Physical Address	0x4804 13B4 0x5800 13B4	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the color phase rotation matrix coefficients for the Blue component. It is used for the secondary LCD output. Shadow register, updated on VFP start period of secondary LCD		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BR										RESERVED						BG					RESERVED			BB							

Bits	Field Name	Description	Type	Reset
31:22	BR	BR Coefficient Encoded signed value (from -512 to 511).	RW	0x000
21	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0
20:11	BG	BG Coefficient Encoded signed value (from -512 to 511).	RW	0x000
10	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0
9:0	BB	BB Coefficient Encoded signed value (from -512 to 511).	RW	0x000

Table 10-336. Register Call Summary for Register DISPC_CPR2_COEF_B

Display Controller

- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1]
- Display Controller Register Summary: [2]

Table 10-337. DISPC_CPR2_COEF_G

Address Offset	0x0000 03B8		
Physical Address	0x4804 13B8 0x5800 13B8	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the color phase rotation matrix coefficients for the Green component. It is used for the secondary LCD output. Shadow register, updated on VFP start period of secondary LCD		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GR										RESERVED						GG					RESERVED			GB							

Bits	Field Name	Description	Type	Reset
31:22	GR	GR Coefficient Encoded signed value (from -512 to 511).	RW	0x000
21	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0
20:11	GG	GG Coefficient Encoded signed value (from -512 to 511).	RW	0x000
10	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0
9:0	GB	GB Coefficient Encoded signed value (from -512 to 511).	RW	0x000

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Table 10-338. Register Call Summary for Register DISPC_CPR2_COEF_G

Display Controller

- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1]
- Display Controller Register Summary: [2]

Table 10-339. DISPC_CPR2_COEF_R

Address Offset	0x0000 03BC		
Physical Address	0x4804 13BC 0x5800 13BC	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the color phase rotation matrix coefficients for the Red component. Shadow register, updated on VFP start period of secondary LCD		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RR										RESERVED						RG								RESERVED							
																								RB							

Bits	Field Name	Description	Type	Reset
31:22	RR	RR Coefficient Encoded signed value (from -512 to 511).	RW	0x000
21	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0
20:11	RG	RG Coefficient Encoded signed value (from -512 to 511).	RW	0x000
10	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0
9:0	RB	RB Coefficient Encoded signed value (from -512 to 511).	RW	0x000

Table 10-340. Register Call Summary for Register DISPC_CPR2_COEF_R

Display Controller

- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1]
- Display Controller Register Summary: [2]

Table 10-341. DISPC_DATA2_CYCLE1

Address Offset	0x0000 03C0		
Physical Address	0x4804 13C0 0x5800 13C0	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The control register configures the output data format for 1st cycle. Shadow register, updated on VFP start period of secondary LCD		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				BITALIGNMENTPIXEL2				RESERVED				NBBITSPIXEL2				RESERVED				BITALIGNMENTPIXEL1				RESERVED				NBBITSPIXEL1			

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Bits	Field Name	Description	Type	Reset
31:28	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0
27:24	BITALIGNMENTPIXEL2	Bit alignment. Alignment of the bits from pixel 2 on the output interface	RW	0x0
23:21	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0
20:16	NBBITSPIXEL2	Number of bits Number of bits from the pixel 2 (value from 0 to 16 bits). The values from 17 to 31 are invalid.	RW	0x00
15:12	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0
11:8	BITALIGNMENTPIXEL1	Bit alignment. Alignment of the bits from pixel 1 on the output interface	RW	0x0
7:5	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0
4:0	NBBITSPIXEL1	Number of bits Number of bits from the pixel 1 (value from 0 to 16 bits). The values from 17 to 31 are invalid.	RW	0x00

Table 10-342. Register Call Summary for Register DISPC_DATA2_CYCLE1

Display Controller

- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1]
- Display Controller Register Summary: [2]

Table 10-343. DISPC_DATA2_CYCLE2

Address Offset	0x0000 03C4		
Physical Address	0x4804 13C4 0x5800 13C4	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The control register configures the output data format for 2nd cycle. Shadow register, updated on VFP start period of secondary LCD		
Type	RW		

31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
RESERVED	BITALIGNMENTPIXEL2	RESERVED	NBBITSPIXEL2	RESERVED	BITALIGNMENTPIXEL1	RESERVED	NBBITSPIXEL1

Bits	Field Name	Description	Type	Reset
31:28	RESERVED	Write 0s for future compatibility Reads return 0.	R	0x0
27:24	BITALIGNMENTPIXEL2	Bit alignment. Alignment of the bits from pixel 2 on the output interface	RW	0x0
23:21	RESERVED	Write 0s for future compatibility Reads return 0.	R	0x0
20:16	NBBITSPIXEL2	Number of bits Number of bits from the pixel 2 (value from 0 to 16 bits). The values from 17 to 31 are invalid.	RW	0x00
15:12	RESERVED	Write 0s for future compatibility Reads return 0.	R	0x0
11:8	BITALIGNMENTPIXEL1	Bit alignment. Alignment of the bits from pixel 1 on the output interface	RW	0x0
7:5	RESERVED	Write 0s for future compatibility Reads return 0.	R	0x0
4:0	NBBITSPIXEL1	Number of bits Number of bits from the pixel 1 (value from 0 to 16 bits). The values from 17 to 31 are invalid.	RW	0x00

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Table 10-344. Register Call Summary for Register DISPC_DATA2_CYCLE2

Display Controller

- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1]
- Display Controller Register Summary: [2]

Table 10-345. DISPC_DATA2_CYCLE3

Address Offset	0x0000 03C8		
Physical Address	0x4804 13C8 0x5800 13C8	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The control register configures the output data format for 3rd cycle. Shadow register, updated on VFP start period of secondary LCD		
Type	RW		

31 30 29 28	27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4 3 2 1 0
RESERVED	BITALIGNMENTPIXEL2	RESERVED	NBBITSPIXEL2	RESERVED	BITALIGNMENTPIXEL1	RESERVED	NBBITSPIXEL1

Bits	Field Name	Description	Type	Reset
31:28	RESERVED	Write 0s for future compatibility Reads return 0.	R	0x0
27:24	BITALIGNMENTPIXEL2	Bit alignment. Alignment of the bits from pixel 2 on the output interface	RW	0x0
23:21	RESERVED	Write 0s for future compatibility Reads return 0.	R	0x0
20:16	NBBITSPIXEL2	Number of bits Number of bits from the pixel 2 (value from 0 to 16 bits). The values from 17 to 31 are invalid.	RW	0x00
15:12	RESERVED	Write 0s for future compatibility Reads return 0.	R	0x0
11:8	BITALIGNMENTPIXEL1	Bit alignment. Alignment of the bits from pixel 1 on the output interface	RW	0x0
7:5	RESERVED	Write 0s for future compatibility Reads return 0.	R	0x0
4:0	NBBITSPIXEL1	Number of bits Number of bits from the pixel 1 (value from 0 to 16 bits). The values from 17 to 31 are invalid.	RW	0x00

Table 10-346. Register Call Summary for Register DISPC_DATA2_CYCLE3

Display Controller

- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1]
- Display Controller Register Summary: [2]

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Table 10-347. DISPC_SIZE_LCD2

Address Offset	0x0000 03CC		
Physical Address	0x4804 13CC 0x5800 13CC	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the panel size (horizontal and vertical). It is used for the secondary LCD output. Shadow register, updated on VFP start period of secondary LCD. A delta value is used to indicate if the odd field has same vertical size as the even field or +/- one line.		
Type	RW		

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14	13 12 11 10 9 8	7 6 5 4 3 2 1 0
RESERVED	LPP	DELTA_LPP	RESERVED	PPL

Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
26:16	LPP	Lines per panel Encoded value (from 1 to 2048) to specify the number of lines per panel (program to value minus 1).	RW	0x000
15:14	DELTA_LPP	Indicates the delta size value of the odd field compared to the even field 0x0: same size 0x1: odd size = even size +1 0x2: Odd size = even size -1	RW	0x0
13:11	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0
10:0	PPL	Pixels per line Encoded value (from 1 to 2048) to specify the number of pixels contains within each line on the display (program to value minus 1). In STALL mode, any value is valid. In non STALL mode, only values multiple of 8 pixels are valid.	RW	0x000

Table 10-348. Register Call Summary for Register DISPC_SIZE_LCD2

Display Controller

- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1] [2]
- Display Controller Register Summary: [3]
- Display Controller Register Description: [4]

Table 10-349. DISPC_TIMING_H2

Address Offset	0x0000 0400		
Physical Address	0x4804 1400 0x5800 1400	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the timing logic for the HSYNC signal. It is used for the secondary LCD output. Shadow register, updated on VFP start period of secondary LCD		
Type	RW		

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
HBP	HFP		HSW

Bits	Field Name	Description	Type	Reset
31:20	HBP	Horizontal Back Porch. Encoded value (from 1 to 4096) to specify the number of pixel clock periods to add to the beginning of a line transmission before the first set of pixels is output to the display (program to value minus 1).	RW	0x000

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Bits	Field Name	Description	Type	Reset
19:8	HFP	Horizontal front porch. Encoded value (from 1 to 4096) to specify the number of pixel clock periods to add to the end of a line transmission before line clock is asserted (program to value minus 1).	RW	0x000
7:0	HSW	Horizontal synchronization pulse width Encoded value (from 1 to 256) to specify the number of pixel clock periods to pulse the line clock at the end of each line (program to value minus 1).	RW	0x00

Table 10-350. Register Call Summary for Register DISPC_TIMING_H2

Display Controller

- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1]
- Display Controller Register Summary: [2]

Table 10-351. DISPC_TIMING_V2

Address Offset	0x0000 0404		
Physical Address	0x4804 1404 0x5800 1404	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the timing logic for the VSYNC signal. It is used for the secondary LCD output. Shadow register, updated on VFP start period of secondary LCD		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VBP																VFP								VSW							

Bits	Field Name	Description	Type	Reset
31:20	VBP	Vertical back porch Encoded value (from 0 to 4095) to specify the number of line clock periods to add to the beginning of a frame before the first set of pixels is output to the display.	RW	0x000
19:8	VFP	Vertical front porch Encoded value (from 0 to 4095) to specify the number of line clock periods to add to the end of each frame.	RW	0x000
7:0	VSW	Vertical synchronization pulse width In active mode, encoded value (from 1 to 256) to specify the number of line clock periods (program to value minus 1) to pulse the frame clock (VSYNC) pin at the end of each frame after the end of frame wait (VFP) period elapses. Frame clock uses as VSYNC signal in active mode. In passive mode, encoded value (from 1 to 256) to specify the number of extra line clock periods (program to value minus 1) to insert after the vertical front porch (VFP) period has elapsed.	RW	0x00

Table 10-352. Register Call Summary for Register DISPC_TIMING_V2

Display Controller

- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1]
- Display Controller Register Summary: [2]

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Table 10-353. DISPC_POL_FREQ2

Address Offset	0x0000 0408		
Physical Address	0x4804 1408 0x5800 1408	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the signal configuration. It is used for the secondary LCD output. Shadow register, updated on VFP start period of secondary LCD		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ALIGN	ONOFF	RF	IEO	IPC	IHS	IVS	ACBI				ACB							

Bits	Field Name	Description	Type	Reset
31:19	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0000
18	ALIGN	Defines the alignment between HSYNC and VSYNC assertion. 0x0: VSYNC and HSYNC are not aligned 0x1: VSYNC and HSYNC assertions are aligned.	RW	0
17	ONOFF	HSYNC/VSYNC Pixel clock Control On/Off 0x0: HSYNC and VSYNC are driven on opposite edges of pixel clock than pixel data 0x1: HSYNC and VSYNC are driven according to bit 16	RW	0
16	RF	Program HSYNC/VSYNC Rise or Fall 0x0: HSYNC and VSYNC are driven on falling edge of pixel clock (if bit 17 set to 1) 0x1: HSYNC and VSYNC are driven on rising edge of pixel clock (if bit 17 set to 1)	RW	0
15	IEO	Invert output enable 0x0: Ac-bias is active high (active display mode) 0x1: Ac-bias is active low (active display mode)	RW	0
14	IPC	Invert pixel clock 0x0: Data is driven on the LCD data lines on the rising-edge of the pixel clock 0x1: Data is driven on the LCD data lines on the falling-edge of the pixel clock	RW	0
13	IHS	Invert HSYNC 0x0: Line clock pin is active high and inactive low 0x1: Line clock pin is active low and inactive high	RW	0
12	IVS	Invert VSYNC 0x0: Frame clock pin is active high and inactive low 0x1: Frame clock pin is active low and inactive high	RW	0
11:8	ACBI	AC Bias Pin transitions per interrupt Value (from 0 to 15) used to specify the number of AC Bias pin transitions	RW	0x0
7:0	ACB	AC Bias Pin Frequency Value (from 0 to 255) used to specify the number of line clocks to count before transitioning the AC Bias pin. This pin is used to periodically invert the polarity of the power supply to prevent DC charge build-up within the display.	RW	0x00

Table 10-354. Register Call Summary for Register DISPC_POL_FREQ2

Display Controller

- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1]
- Display Controller Register Summary: [2]

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Table 10-355. DISPC_DIVISOR2

Address Offset	0x0000 040C		
Physical Address	0x4804 140C 0x5800 140C	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the divisors. It is used for the secondary LCD output. Shadow register, updated on VFP start period of secondary LCD		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								LCD								RESERVED								PCD							

Bits	Field Name	Description	Type	Reset
31:24	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
23:16	LCD	Display Controller Logic Clock Divisor Value (from 1 to 255) to specify the intermediate pixel clock frequency based on the LCD2_CLK. The value 0 is invalid.	RW	0x04
15:8	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
7:0	PCD	Pixel Clock Divisor Value (from 1 to 255) to specify the frequency of the pixel clock based on the LCD2_CLK divided by DISPC_DIVISOR2.LCD value. The values 0 is invalid.	RW	0x01

Table 10-356. Register Call Summary for Register DISPC_DIVISOR2

Display Controller

- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1]
- Display Controller Register Summary: [2]
- Display Controller Register Description: [3]

Table 10-357. DISPC_WB_ACCU_j

Address Offset	0x0000 0500 + (0x4 * j)	**Index**	j = 0 to 1
Physical Address	0x4804 1500 + (0x4 * j) 0x5800 1500 + (0x4 * j)	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the resize accumulator init values for horizontal and vertical up/downsampling of the write back pipeline (DISPC_WB_ACCU_0 DISPC_WB_ACCU_1 for ping-pong mechanism with external trigger, based on the field polarity). It is used for ARGB and Y setting. Shadow register, updated when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline) when the WB pipeline is directly connected to one of the pipelines (graphics or video), otherwise updated on VFP start period of primary LCD or VFP start period of secondary LCD or EVSYNC depending on which overlay output is selected as an input to the WB pipeline		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								VERTICALACCU								RESERVED								HORIZONTALACCU							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
26:16	VERTICALACCU	Vertical initialization accu value Encoded value (from -1024 to 1023).	RW	0x000
15:11	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
10:0	HORIZONTALACCU	Horizontal initialization accu value Encoded value (from -1024 to 1023).	RW	0x000

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Table 10-358. Register Call Summary for Register DISPC_WB_ACCU_j

Display Controller

- Scaler Unit: [0] [1]
- Shadow Registers: [2]
- Operational Modes Configuration: [3] [4]
- Display Controller Register Summary: [5]

Table 10-359. DISPC_WB_BA_j

Address Offset	0x0000 0508 + (0x4 * j)	**Index**	j = 0 to 1
Physical Address	0x4804 1508 + (0x4 * j) 0x5800 1508 + (0x4 * j)	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the base address of the WB buffer (DISPC_WB_BA_0 DISPC_WB_BA_1 for ping-pong mechanism with external trigger, based on the field polarity otherwise only DISPC_WB_BA_0 is used). Shadow register, updated when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline) when the WB pipeline is directly connected to one of the pipelines (graphics or video), otherwise updated on VFP start period of primary LCD or VFP start period of secondary LCD or EVSYNC depending on which overlay output is selected as an input to the WB pipeline		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BA																															

Bits	Field Name	Description	Type	Reset
31:0	BA	Write-back base address Base address of the WB buffer (aligned on pixel size boundary except in case of RGB24 packed format, 4-pixel alignment is required; in case of YUV4:2:2, 2-pixel alignment is required, and YUV4:2;0, byte alignment is supported)). It case of YUV4:2:0 format, it indicates the base address of the Y buffer. When the TILER is addressed, the bits: [28:27] = 0x0 for 8-bit tiled [28:27] = 0x1 for 16-bit tiled [28:27] = 0x2 for 32-bit tiled [28:27] = 0x3 for page mode [31:29] = 0x0 for 0-degree view [31:29] = 0x1 for 180-degree view + mirroring [31:29] = 0x2 for 0-degree view + mirroring [31:29] = 0x3 for 180-degree view [31:29] = 0x4 for 270-degree view + mirroring [31:29] = 0x5 for 270-degree view [31:29] = 0x6 for 90-degree view [31:29] = 0x7 for 90-degree view + mirroring Otherwise the bits indicated the corresponding bit address to access the SDRAM.	RW	0x0000 0000

Table 10-360. Register Call Summary for Register DISPC_WB_BA_j

Display Controller

- Addressing and Bursts: [0]
- Rotation and Mirroring: [1] [2] [3] [4]
- Shadow Registers: [5]
- Operational Modes Configuration: [6]
- Display Controller Register Summary: [7]

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Table 10-361. DISPC_WB_FIR_COEF_H_i

Address Offset	0x0000 0510 + (0x8 * i)	**Index**	i = 0 to 7
Physical Address	0x4804 1510 + (0x8 * i) 0x5800 1510 + (0x8 * i)	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The bank of registers configure the up/down-scaling coefficients for the horizontal resize of the video picture associated with the write back pipeline for the phases from 0 to 7. It is used for ARGB and Y setting. Shadow register, updated when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline) when the WB pipeline is directly connected to one of the pipelines (graphics or video), otherwise updated on VFP start period of primary LCD or VFP start period of secondary LCD or EVSYNC depending on which overlay output is selected as an input to the WB pipeline		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIRHC3								FIRHC2								FIRHC1								FIRHC0							

Bits	Field Name	Description	Type	Reset
31:24	FIRHC3	Signed coefficient C3 for the horizontal up/down-scaling with the phase n	RW	0x00
23:16	FIRHC2	Unsigned coefficient C2 for the horizontal up/down-scaling with the phase n	RW	0x00
15:8	FIRHC1	Signed coefficient C1 for the horizontal up/down-scaling with the phase n	RW	0x00
7:0	FIRHC0	Signed coefficient C0 for the horizontal up/down-scaling with the phase n	RW	0x00

Table 10-362. Register Call Summary for Register DISPC_WB_FIR_COEF_H_i

Display Controller

- Scaler Unit: [0] [1] [2] [3] [4] [5]
- Shadow Registers: [6]
- Operational Modes Configuration: [7]
- Display Controller Register Summary: [8]

Table 10-363. DISPC_WB_FIR_COEF_HV_i

Address Offset	0x0000 0514 + (0x8 * i)	**Index**	i = 0 to 7
Physical Address	0x4804 1514 + (0x8 * i) 0x5800 1514 + (0x8 * i)	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The bank of registers configure the down/up/down-scaling coefficients for the vertical and horizontal resize of the video picture associated with the write back pipeline for the phases from 0 to 7. It is used for ARGB and Y setting. Shadow register, updated when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline) when the WB pipeline is directly connected to one of the pipelines (graphics or video), otherwise updated on VFP start period of primary LCD or VFP start period of secondary LCD or EVSYNC depending on which overlay output is selected as an input to the WB pipeline		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIRVC2								FIRVC1								FIRVC0								FIRHC4							

Bits	Field Name	Description	Type	Reset
31:24	FIRVC2	Signed coefficient C2 for the vertical up/down-scaling with the phase n	RW	0x00
23:16	FIRVC1	Unsigned coefficient C1 for the vertical up/down-scaling with the phase n	RW	0x00
15:8	FIRVC0	Signed coefficient C0 for the vertical up/down-scaling with the phase n	RW	0x00
7:0	FIRHC4	Signed coefficient C4 for the horizontal up/down-scaling with the phase n	RW	0x00

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Table 10-364. Register Call Summary for Register DISPC_WB_FIR_COEF_HV_i

Display Controller

- Scaler Unit: [0] [1] [2] [3] [4] [5] [6]
- Shadow Registers: [7]
- Operational Modes Configuration: [8] [9]
- Display Controller Register Summary: [10]

Table 10-365. DISPC_WB_FIR_COEF_V_i

Address Offset	0x0000 0550 + (0x4 * i)	**Index**	i = 0 to 7
Physical Address	0x4804 1550 + (0x4 * i) 0x5800 1550 + (0x4 * i)	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The bank of registers configure the down/up/down-scaling coefficients for the vertical resize of the video picture associated with the write back pipeline for the phases from 0 to 7. It is used for ARGB and Y setting. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																FIRVC22								FIRVC00							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0000
15:8	FIRVC22	Signed coefficient C22 for the vertical up/down-scaling with the phase n	RW	0x00
7:0	FIRVC00	Signed coefficient C00 for the vertical up/down-scaling with the phase n	RW	0x00

Table 10-366. Register Call Summary for Register DISPC_WB_FIR_COEF_V_i

Display Controller

- Scaler Unit: [0] [1] [2]
- Shadow Registers: [3]
- Operational Modes Configuration: [4]
- Display Controller Register Summary: [5]

Table 10-367. DISPC_WB_ATTRIBUTES

Address Offset	0x0000 0570		
Physical Address	0x4804 1570 0x5800 1570	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the attributes of the viwrite back pipeline. Shadow register, updated when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline) when the WB pipeline is directly connected to one of the pipelines (graphics or video), otherwise updated on VFP start period of primary LCD or VFP start period of secondary LCD or EVSYNC depending on which overlay output is selected as an input to the WB pipeline		
Type	RW		

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31 30 29 28	27	26 25 24	23	22	21	20	19	18 17 16	15 14	13 12	11	10	9	8	7	6	5 4 3 2	1	0
IDLENUMBER	IDLESIZE	CAPTUREMODE	ARBITRATION	DOUBLESTRIDE	VERTICALTAPS	RESERVED	WRITEBACKMODE	CHANNELIN	BURSTSIZE	RESERVED	FULLRANGE	TRUNCATIONENABLE	COLORCONVENABLE	BURSTTYPE	ALPHAENABLE	RESIZEENABLE	FORMAT		ENABLE

Bits	Field Name	Description	Type	Reset
31:28	IDLENUMBER	Determines the number of idles between requests on the L3 interconnect. It is only used when the write-back pipeline does data transfer from memory to memory. When the output of an overlay is stored in memory through the write-back pipeline in capture mode, the bit field IDLENUMBER is ignored since a timing generator is used to time the transfer. The number of IDLE cycles is IDLENUMBER (from 0 to 15) if IDLESIZE=0. The number of IDLE cycles is IDLENUMBERx8 (from 0 to 120) if IDLESIZE=1 and BURSTSIZE=2. The number of IDLE cycles is IDLENUMBERx4 (from 0 to 60) if IDLESIZE=1 and BURSTSIZE=1. The number of IDLE cycles is IDLENUMBERx2 (from 0 to 30) if IDLESIZE=1 and BURSTSIZE=0.	RW	0x0
27	IDLESIZE	Determines if the IDLENUMBER corresponds to a number of bursts or singles. 0x0: The number of idles between requests is defined by IDLENUMBER as number of cycles. 0x1: The number of idles between requests is defined by IDLENUMBER multiplied by burst size as number of cycles.	RW	0
26:24	CAPTUREMODE	Defines the frame rate capture. 0x6: Only one out of six frames is captured. The first one is captured then the second one is skipped and so on. 0x1: Only one frame is captured. 0x7: Only one out of seven frames is captured. The first one is captured then the second one is skipped and so on. 0x0: All frames are captures until the write-back channel is disabled or there is no more data generated by the overlay or the pipeline attached to the write-back channel. 0x2: Only one out of two frames is captured. The first one is captured then the second one is skipped and so on. 0x4: Only one out of four frames is captured. The first one is captured then the second one is skipped and so on. 0x5: Only one out of five frames is captured. The first one is captured then the second one is skipped and so on. 0x3: Only one out of three frames is captured. The first one is captured then the second one is skipped and so on.	RW	0x0

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Bits	Field Name	Description	Type	Reset
23	ARBITRATION	Determines the priority of the write-back pipeline. The write-back pipeline is one of the high priority pipeline. The arbitration gives always the priority first to the high priority pipelines using round-robin between them. When there is only normal priority pipelines sending requests, the round-robin applies between them. 0x0: The write-back pipeline is one of the normal priority pipeline. 0x1: The write-back pipeline is one of the high priority pipeline.	RW	0
22	DOUBLESTRIDE	Determines if the stride for CbCr buffer is the 1x or 2x of the Y buffer stride. It is only used in case of YUV4:2:0. 0x0: The CbCr stride value is equal to the Y stride. 0x1: The CbCr stride value is double to the Y stride.	RW	0
21	VERTICALTAPS	Video Vertical Resize Tap Number 0x0: 3 taps are used for the vertical filtering logic. The 2 other taps are not used. 0x1: 5 taps are used for the vertical filtering logic.	RW	0
20	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0
19	WRITEBACKMODE	When connected to the overlay output of a channel the write back can operate as a simple transfer from memory to memory (composition engine) or as a capture channel. 0x0: Capture mode (default mode) 0x1: Memory-to-memory mode	RW	0x0
18:16	CHANNELIN	Video Channel In configuration wr: immediate 0x6: Video3 pipeline output 0x1: Secondary LCD output 0x0: Primary LCD overlay output 0x2: TV overlay output 0x4: Video1 pipeline output 0x5: Video2 pipeline output 0x3: Graphics pipeline output	RW	0x0
15:14	BURSTSIZE	Write-back DMA Burst Size 0x0: 2x128bit bursts 0x1: 4x128bit bursts 0x3: Reserved 0x2: 8x128bit bursts	RW	0x2
13:12	RESERVED	RESERVED	RW	0x0
11	FULLRANGE	Color Space Conversion full range setting. 0x0: Limited range selected: 16 subtracted from Y before color space conversion 0x1: Full range selected: Y is not modified before the color space conversion	RW	0
10	TRUNCATIONENABLE	It applies only when the input format to the write-back pipeline from the overlay or directly from one of the pipelines is ARGB32. If the format is one of the YUV supported formats, the bit field is ignored. 0x0: Disable truncation logic 0x1: Enable truncation logic from ARGB32 to the pixel format defined in the field FORMAT.	RW	0

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Bits	Field Name	Description	Type	Reset
9	COLORCONVENABLE	Enable the color space conversion. The hardware does not enable/disable the conversion based on the pixel format. The bit field shall be reset when the format is not YUV. 0x0: Disable Color Space Conversion RGB to YUV 0x1: Enable Color Space Conversion RGB to YUV	RW	0
8	BURSTTYPE	The type of burst can be INCR (incremental) or BLCK (2D block). The 2D block is required when the TILER is targeted by the DMA engine. 0x0: INC burst type is used. 0x1: 2D block burst type is used.	RW	0
7	ALPHAENABLE	Premultiplied alpha enable Read 0x1: Enabled Read 0x0: Disabled. This bit also disable the logic present in the associated channel out that compute the alpha component sent to the WB pipe. When the WB is configured to copy back one of the output channels (output of overlay), the following configurations are available: 0x1: The WB pipe copies back to memory the premultiplied alpha calculated through the overlay. 0x0: The alpha value is not written back.	RW	0
6:5	RESIZEENABLE	Resize Enable 0x0: Disable the resize processing 0x1: Enable the horizontal resize processing 0x3: Enable both horizontal and vertical resize processing 0x2: Enable the vertical resize processing	RW	0x0
4:1	FORMAT	Write-back Format. It defines the pixel format when storing the write-back picture into memory. 0x6: RGB16-565 0x1: RGB12x-4444 0xA: YUV2 4:2:2 co-sited 0x7: ARGB16-1555 0xD: RGBA32-8888 0x0: NV12 4:2:0 2 buffers (Y + UV) 0x2: RGBA12-4444 0x8: xRGB24-8888 (32-bit container) 0x9: RGB24-888 (24-bit container) 0xB: UYVY 4:2:2 co-sited 0x5: ARGB16-4444 0xF: xRGB15-1555 0xC: ARGB32-8888 0x4: xRGB12-4444 0xE: RGBx24-8888 (24-bit RGB aligned on MSB of the 32-bit container)	RW	0x0
0	ENABLE	Write-back Enable. wr: immediate 0x0: Write-back disabled 0x1: Write-back enabled	RW	0

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Table 10-368. Register Call Summary for Register DISPC_WB_ATTRIBUTES

Display Controller

- DMA Buffers: [0] [1] [2] [3] [4]
- Arbitration: [5]
- Write-Back Pipeline: [6] [7] [8]
- CSC Unit RGB to YUV: [9] [10]
- Scaler Unit: [11] [12] [13]
- RGB Truncation Logic: [14] [15]
- Overlay Manager: [16] [17] [18]
- Shadow Registers: [19] [20] [21] [22] [23]
- Operational Modes Configuration: [24] [25] [26] [27] [28] [29] [30] [31] [32] [33] [34] [35] [36] [37]
- Display Controller Register Summary: [38]

Table 10-369. DISPC_WB_CONV_COEF0

Address Offset	0x0000 0574		
Physical Address	0x4804 1574 0x5800 1574	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the color space conversion matrix coefficients for the write back pipeline (YUV4:4:4 to RGB24) Shadow register, updated when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline) when the WB pipeline is directly connected to one of the pipelines (graphics or video), otherwise updated on VFP start period of primary LCD or VFP start period of secondary LCD or EVSYNC depending on which overlay output is selected as an input to the WB pipeline		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					YG											RESERVED					YR											

Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
26:16	YG	YG Coefficient Encoded signed value (from -1024 to 1023).	RW	0x000
15:11	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
10:0	YR	YR Coefficient Encoded signed value (from -1024 to 1023).	RW	0x000

Table 10-370. Register Call Summary for Register DISPC_WB_CONV_COEF0

Display Controller

- CSC Unit RGB to YUV: [0] [1]
- Shadow Registers: [2]
- Operational Modes Configuration: [3]
- Display Controller Register Summary: [4]

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Table 10-371. DISPC_WB_CONV_COEF1

Address Offset	0x0000 0578		
Physical Address	0x4804 1578 0x5800 1578	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the color space conversion matrix coefficients for the write back pipeline. Shadow register, updated when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline) when the WB pipeline is directly connected to one of the pipelines (graphics or video), otherwise updated on VFP start period of primary LCD or VFP start period of secondary LCD or EVSYNC depending on which overlay output is selected as an input to the WB pipeline		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								CRR								RESERVED								YB							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
26:16	CRR	CrR Coefficient Encoded signed value (from -1024 to 1023).	RW	0x000
15:11	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
10:0	YB	YB Coefficient Encoded signed value (from -1024 to 1023).	RW	0x000

Table 10-372. Register Call Summary for Register DISPC_WB_CONV_COEF1

Display Controller

- CSC Unit RGB to YUV: [0] [1]
- Shadow Registers: [2]
- Operational Modes Configuration: [3]
- Display Controller Register Summary: [4]

Table 10-373. DISPC_WB_CONV_COEF2

Address Offset	0x0000 057C		
Physical Address	0x4804 157C 0x5800 157C	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the color space conversion matrix coefficients for the write back pipeline. Shadow register, updated when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline) when the WB pipeline is directly connected to one of the pipelines (graphics or video), otherwise updated on VFP start period of primary LCD or VFP start period of secondary LCD or EVSYNC depending on which overlay output is selected as an input to the WB pipeline		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								CRB								RESERVED								CRG							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
26:16	CRB	CrB Coefficient Encoded signed value (from -1024 to 1023).	RW	0x000
15:11	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
10:0	CRG	CrG Coefficient Encoded signed value (from -1024 to 1023).	RW	0x000

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Table 10-374. Register Call Summary for Register DISPC_WB_CONV_COEF2

Display Controller

- CSC Unit RGB to YUV: [0] [1]
- Shadow Registers: [2]
- Operational Modes Configuration: [3]
- Display Controller Register Summary: [4]

Table 10-375. DISPC_WB_CONV_COEF3

Address Offset	0x0000 0580		
Physical Address	0x4804 1580 0x5800 1580	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the color space conversion matrix coefficients for the write back pipeline. Shadow register, updated when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline) when the WB pipeline is directly connected to one of the pipelines (graphics or video), otherwise updated on VFP start period of primary LCD or VFP start period of secondary LCD or EVSYNC depending on which overlay output is selected as an input to the WB pipeline		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								CBG								RESERVED								CBR							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
26:16	CBG	CbG coefficient Encoded signed value (from -1024 to 1023).	RW	0x000
15:11	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
10:0	CBR	CbR coefficient Encoded signed value (from -1024 to 1023).	RW	0x000

Table 10-376. Register Call Summary for Register DISPC_WB_CONV_COEF3

Display Controller

- CSC Unit RGB to YUV: [0] [1]
- Shadow Registers: [2]
- Operational Modes Configuration: [3]
- Display Controller Register Summary: [4]

Table 10-377. DISPC_WB_CONV_COEF4

Address Offset	0x0000 0584		
Physical Address	0x4804 1584 0x5800 1584	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the color space conversion matrix coefficients for the write back pipeline. Shadow register, updated when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline) when the WB pipeline is directly connected to one of the pipelines (graphics or video), otherwise updated on VFP start period of primary LCD or VFP start period of secondary LCD or EVSYNC depending on which overlay output is selected as an input to the WB pipeline		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								CBB							

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Bits	Field Name	Description	Type	Reset
31:11	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x000000
10:0	CBB	CbB Coefficient Encoded signed value (from -1024 to 1023).	RW	0x000

Table 10-378. Register Call Summary for Register DISPC_WB_CONV_COEF4

Display Controller
- CSC Unit RGB to YUV: [0]
- Shadow Registers: [1]
- Operational Modes Configuration: [2]
- Display Controller Register Summary: [3]

Table 10-379. DISPC_WB_BUF_SIZE_STATUS

Address Offset	0x0000 0588		
Physical Address	0x4804 1588 0x5800 1588	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register defines the DMA buffer size for the write back pipeline.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																BUFSIZE															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0000
15:0	BUFSIZE	DMA buffer Size in number of 128-bits.	R	0x0800

Table 10-380. Register Call Summary for Register DISPC_WB_BUF_SIZE_STATUS

Display Controller
- Shadow Registers: [0]
- Display Controller Register Summary: [1]

Table 10-381. DISPC_WB_BUF_THRESHOLD

Address Offset	0x0000 058C		
Physical Address	0x4804 158C 0x5800 158C	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the DMA buffer associated with the write-back pipeline. Shadow register, updated when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline) when the WB pipeline is directly connected to one of the pipelines (graphics or video), otherwise updated on VFP start period of primary LCD or VFP start period of secondary LCD or EVSYNC depending on which overlay output is selected as an input to the WB pipeline		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BUFHIGHTHRESHOLD																BUFLOWTHRESHOLD															

Bits	Field Name	Description	Type	Reset
31:16	BUFHIGHTHRESHOLD	DMA buffer High Threshold Number of 128-bits defining the threshold value.	RW	0x07FF
15:0	BUFLOWTHRESHOLD	DMA buffer High Threshold Number of 128-bits defining the threshold value.	RW	0x07F8

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Table 10-382. Register Call Summary for Register DISPC_WB_BUF_THRESHOLD

Display Controller

- DMA Buffers: [0] [1]
- Shadow Registers: [2]
- Operational Modes Configuration: [3] [4]
- Display Controller Register Summary: [5]

Table 10-383. DISPC_WB_FIR

Address Offset	0x0000 0590		
Physical Address	0x4804 1590 0x5800 1590	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the resize factors for horizontal and vertical up/downsampling of the write back pipeline. It is used for ARGB and Y setting. Shadow register, updated when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline) when the WB pipeline is directly connected to one of the pipelines (graphics or video), otherwise updated on VFP start period of primary LCD or VFP start period of secondary LCD or EVSYNC depending on which overlay output is selected as an input to the WB pipeline		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								FIRVINC								RESERVED								FIRHINC							

Bits	Field Name	Description	Type	Reset
31:29	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0
28:16	FIRVINC	Vertical increment of the up/downsampling filter Encoded value (from 1 to 4096). The value 0 is invalid. The values greater than 4096 are invalid.	RW	0x0400
15:13	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0
12:0	FIRHINC	Horizontal increment of the up/downsampling filter Encoded value (from 1 to 4096). The value 0 is invalid. The values greater than 4096 are invalid.	RW	0x0400

Table 10-384. Register Call Summary for Register DISPC_WB_FIR

Display Controller

- Scaler Unit: [0] [1] [2] [3]
- Shadow Registers: [4]
- Operational Modes Configuration: [5] [6]
- Display Controller Register Summary: [7]

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Table 10-385. DISPC_WB_PICTURE_SIZE

Address Offset	0x0000 0594		
Physical Address	0x4804 1594 0x5800 1594	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the size of the write-back picture associated with the write back pipeline after up/down-scaling. Shadow register, updated when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline) when the WB pipeline is directly connected to one of the pipelines (graphics or video), otherwise updated on VFP start period of primary LCD or VFP start period of secondary LCD or EVSYNC depending on which overlay output is selected as an input to the WB pipeline		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								ORGSIZEY								RESERVED								ORGSIZEX							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
26:16	ORGSIZEY	Number of lines of the video picture Encoded value (from 1 to 2048) to specify the number of lines of the video picture in memory (program to value minus 1).	RW	0x000
15:11	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
10:0	ORGSIZEX	Number of pixels of the video picture Encoded value (from 1 to 2048) to specify the number of pixels of the video picture in memory (program to value minus 1). The size is limited to the size of the line buffer of the vertical sampling block in case the video picture is processed by the vertical filtering unit.	RW	0x000

Table 10-386. Register Call Summary for Register DISPC_WB_PICTURE_SIZE

Display Controller

- Scaler Unit: [0] [1]
- Shadow Registers: [2]
- Operational Modes Configuration: [3] [4]
- Display Controller Register Summary: [5]

Table 10-387. DISPC_WB_PIXEL_INC

Address Offset	0x0000 0598		
Physical Address	0x4804 1598 0x5800 1598	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the number of bytes to increment between two pixels for the buffer associated with the write back pipeline. The register is used only when the TILER is not present in the system in order to perform low performance rotation. When the TILER IP is present it is highly recommended to use it for performing the rotation. Shadow register, updated when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline) when the WB pipeline is directly connected to one of the pipelines (graphics or video), otherwise updated on VFP start period of primary LCD or VFP start period of secondary LCD or EVSYNC depending on which overlay output is selected as an input to the WB pipeline		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								PIXELINC							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x000000
7:0	PIXELINC	Values other than 1 are invalid	RW	0x01

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Table 10-388. Register Call Summary for Register DISPC_WB_PIXEL_INC

Display Controller

- Addressing and Bursts: [0]
- Rotation and Mirroring: [1] [2] [3] [4]
- Shadow Registers: [5]
- Operational Modes Configuration: [6]
- Display Controller Register Summary: [7]

Table 10-389. DISPC_WB_ROW_INC

Address Offset	0x0000 05A4		
Physical Address	0x4804 15A4 0x5800 15A4	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the number of bytes to increment at the end of the row for the buffer associated with the vwrite back pipeline. Shadow register, updated when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline) when the WB pipeline is directly connected to one of the pipelines (graphics or video), otherwise updated on VFP start period of primary LCD or VFP start period of secondary LCD or EVSYNC depending on which overlay output is selected as an input to the WB pipeline		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ROWINC																															

Bits	Field Name	Description	Type	Reset
31:0	ROWINC	Number of bytes to increment at the end of the row Encoded signed value (from $2^{31}1$ to 2^{31}) to specify the number of bytes to increment at the end of the row in the video buffer. The value 0 is invalid. The value 1 means next pixel. The value 1 + n *bpp means increment of n pixels. The value 1 (n + 1) * bpp means decrement of n pixels.	RW	0x0000 0001

Table 10-390. Register Call Summary for Register DISPC_WB_ROW_INC

Display Controller

- Addressing and Bursts: [0]
- Rotation and Mirroring: [1] [2] [3] [4]
- Shadow Registers: [5]
- Operational Modes Configuration: [6]
- Display Controller Register Summary: [7]

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Table 10-391. DISPC_WB_SIZE

Address Offset	0x0000 05A8		
Physical Address	0x4804 15A8 0x5800 15A8	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the size of the output of overlay connected to the write-back pipeline when the overlay output is only used by the write-back pipeline. When the overlay is output on the primary LCD or secondary LCD or TV outputs, the size of the frame is defined in the DISPC_SIZE_LCD1, DISPC_SIZE_LCD2, and DISPC_SIZE_TV respectively. Shadow register, updated when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline) when the WB pipeline is directly connected to one of the pipelines (graphics or video), otherwise updated on VFP start period of primary LCD or VFP start period of secondary LCD or EVSYNC depending on which overlay output is selected as an input to the WB pipeline		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								SIZEY								RESERVED								SIZEX							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
26:16	SIZEY	Number of lines of the Write-back picture Encoded value (from 1 to 2048) to specify the number of lines of the write-back picture. Program to value minus 1.	RW	0x000
15:11	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
10:0	SIZEX	Number of pixels of the Write-back picture Encoded value (from 1 to 2048) to specify the number of pixels of the write-back picture. Program to value minus 1.	RW	0x000

Table 10-392. Register Call Summary for Register DISPC_WB_SIZE

Display Controller

- Scaler Unit: [0] [1] [2] [3] [4]
- Shadow Registers: [5]
- Operational Modes Configuration: [6] [7]
- Display Controller Register Summary: [8]

Table 10-393. DISPC_VID1_BA_UV_j

Address Offset	0x0000 0600 + (0x4 * j)	**Index**	j = 0 to 1
Physical Address	0x4804 1600 + (0x4 * j) 0x5800 1600 + (0x4 * j)	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the base address of the UV buffer for the video window 1. (DISPC_VID1_BA_UV_0 DISPC_VID1_BA_UV_1 for ping-pong mechanism with external trigger, based on the field polarity otherwise only DISPC_VID1_BA_UV_0 is used)). Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BA																															

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Bits	Field Name	Description	Type	Reset
31:0	BA	Video base address aligned on 16-bit boundary Base address of the UV video buffer used only in case of YUV4:2:0-NV12 When the TILER is addressed, the bits: [28:27] = 0x0 for 8-bit tiled [28:27] = 0x1 for 16-bit tiled [28:27] = 0x2 for 32-bit tiled [28:27] = 0x3 for page mode [31:29] = 0x0 for 0-degree view [31:29] = 0x1 for 180-degree view + mirroring [31:29] = 0x2 for 0-degree view + mirroring [31:29] = 0x3 for 180-degree view [31:29] = 0x4 for 270-degree view + mirroring [31:29] = 0x5 for 270-degree view [31:29] = 0x6 for 90-degree view [31:29] = 0x7 for 90-degree view + mirroring Otherwise the bits indicated the corresponding bit address to access the SDRAM.	RW	0x0000 0000

Table 10-394. Register Call Summary for Register DISPC_VID1_BA_UV_j

Display Controller

- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1]
- Display Controller Register Summary: [2]

Table 10-395. DISPC_VID2_BA_UV_j

Address Offset	0x0000 0608 + (0x4 * j)	**Index**	j = 0 to 1
Physical Address	0x4804 1608 + (0x4 * j) 0x5800 1608 + (0x4 * j)	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the base address of the UV buffer for the video window 2. (DISPC_VID2_BA_UV_0 DISPC_VID2_BA_UV_1 for ping-pong mechanism with external trigger, based on the field polarity otherwise only DISPC_VID2_BA_UV_0 is used)). Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BA																															

Bits	Field Name	Description	Type	Reset
31:0	BA	Video base address aligned on 16-bit boundary Base address of the UV video buffer used only in case of YUV4:2:0-NV12 When the TILER is addressed, the bits: [28:27] = 0x0 for 8-bit tiled [28:27] = 0x1 for 16-bit tiled [28:27] = 0x2 for 32-bit tiled [28:27] = 0x3 for page mode [31:29] = 0x0 for 0-degree view [31:29] = 0x1 for 180-degree view + mirroring [31:29] = 0x2 for 0-degree view + mirroring [31:29] = 0x3 for 180-degree view [31:29] = 0x4 for 270-degree view + mirroring [31:29] = 0x5 for 270-degree view [31:29] = 0x6 for 90-degree view [31:29] = 0x7 for 90-degree view + mirroring Otherwise the bits indicated the corresponding bit address to access the SDRAM.	RW	0x0000 0000

Table 10-396. Register Call Summary for Register DISPC_VID2_BA_UV_j

Display Controller

- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1]
- Display Controller Register Summary: [2]

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Table 10-397. DISPC_VID3_BA_UV_j

Address Offset	0x0000 0610 + (0x4 * j)	**Index**	j = 0 to 1
Physical Address	0x4804 1610 + (0x4 * j) 0x5800 1610 + (0x4 * j)	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the base address of the UV buffer for the video window 3. (DISPC_VID3_BA_UV_0 DISPC_VID3_BA_UV_1 for ping-pong mechanism with external trigger, based on the field polarity otherwise only DISPC_VID3_BA_UV_0 is used)). Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BA																															

Bits	Field Name	Description	Type	Reset
31:0	BA	Video base address alinged on 16-bit boundary Base address of the UV video buffer used only in case of YUV4:2:0-NV12 When the TILER is addressed, the bits: [28:27] = 0x0 for 8-bit tiled [28:27] = 0x1 for 16-bit tiled [28:27] = 0x2 for 32-bit tiled [28:27] = 0x3 for page mode [31:29] = 0x0 for 0-degree view [31:29] = 0x1 for 180-degree view + mirroring [31:29] = 0x2 for 0-degree view + mirroring [31:29] = 0x3 for 180-degree view [31:29] = 0x4 for 270-degree view + mirroring [31:29] = 0x5 for 270-degree view [31:29] = 0x6 for 90-degree view [31:29] = 0x7 for 90-degree view + mirroring Otherwise the bits indicated the corresponding bit address to access the SDRAM.	RW	0x0000 0000

Table 10-398. Register Call Summary for Register DISPC_VID3_BA_UV_j

Display Controller

- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1]
- Display Controller Register Summary: [2]

Table 10-399. DISPC_WB_BA_UV_j

Address Offset	0x0000 0618 + (0x4 * j)	**Index**	j = 0 to 1
Physical Address	0x4804 1618 + (0x4 * j) 0x5800 1618 + (0x4 * j)	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the base address of the UV buffer for the write-back pipeline. (DISPC_WB_BA_UV_0 DISPC_WB_BA_UV_1 for ping-pong mechanism with external trigger, based on the field polarity otherwise only DISPC_WB_BA_UV_0 is used)). Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BA																															

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Bits	Field Name	Description	Type	Reset
31:0	BA	Video base address alinged on 16-bit boundary Base address of the UV video buffer used only in case of YUV4:2:0-NV12 When the TILER is addressed, the bits: [28:27] = 0x0 for 8-bit tiled [28:27] = 0x1 for 16-bit tiled [28:27] = 0x2 for 32-bit tiled [28:27] = 0x3 for page mode [31:29] = 0x0 for 0-degree view [31:29] = 0x1 for 180-degree view + mirroring [31:29] = 0x2 for 0-degree view + mirroring [31:29] = 0x3 for 180-degree view [31:29] = 0x4 for 270-degree view + mirroring [31:29] = 0x5 for 270-degree view [31:29] = 0x6 for 90-degree view [31:29] = 0x7 for 90-degree view + mirroring Otherwise the bits indicated the corresponding bit address to access the SDRAM.	RW	0x0000 0000

Table 10-400. Register Call Summary for Register DISPC_WB_BA_UV_j

Display Controller

- Addressing and Bursts: [0]
- Shadow Registers: [1]
- Operational Modes Configuration: [2]
- Display Controller Register Summary: [3]

Table 10-401. DISPC_CONFIG2

Address Offset	0x0000 0620		
Physical Address	0x4804 1620 0x5800 1620	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The control register configures the Display Controller module for the secondary LCD output. Shadow register, updated on VFP start period of secondary LCD or EVSYNC		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						FULLRANGE	COLORCONVENABLE	FIDFIRST	OUTPUTMODEENABLE	RESERVED					BUFFERHANDCHECK	CPR	RESERVED			TCKLCDSELECTION	TCKLCDENABLE	RESERVED	ACBIASGATED	VSYNCGATED	HSYNCGATED	PIXELCLOCKGATED	PIXELDATAGATED	RESERVED			PIXELGATED

Bits	Field Name	Description	Type	Reset
31:26	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
25	FULLRANGE	Color Space Conversion full range setting. 0x0: Limited range selected. 0x1: Full range selected.	RW	0
24	COLORCONV ENABLE	Enable the color space conversion. It shall be reset when CPR bit field is set to 0x1. 0x0: Disable Color Space Conversion RGB to YUV 0x1: Enable Color Space Conversion RGB to YUV	RW	0
23	FIDFIRST	Selects the first field to output in case of interlace mode. In case of progressive mode, the value is not used. 0x0: First field is even. 0x1: Odd field is first.	RW	0
22	OUTPUTMODE ENABLE	Selects between progressive and interlace mode for the secondary LCD output. 0x0: Progressive mode selected. 0x1: Interlace mode selected.	RW	0
21:17	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00

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Bits	Field Name	Description	Type	Reset
16	BUFFERHAND CHECK	Controls the handcheck between DMA buffer and STALL signal in order to prevent from underflow. The bit shall be set to 0 when the module is not in STALL mode. (secondary LCD output) 0x0: Only the STALL signal (generated by RFBI or DSI2 depending on which IP uses the LCD output) is used regardless of the DMA buffer fullness information in order to provide data to the RFBI or DS2 module. 0x1: The STALL signal (generated by RFBI or DSI2 depending on which IP uses the LCD output) is used in combination with the DMA buffer fullness information in order to provide data to the RFBI or DSI2 module only when it does not generated buffer underflow.	RW	0
15	CPR	Color Phase Rotation Control secondary LCD output). It shall be reset when ColorConvEnable bit field is set to 1. wr: VFP start period of secondary LCD output 0x0: Color Phase Rotation Disabled 0x1: Color Phase Rotation Enabled	RW	0
14:12	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0
11	TCKLCD SELECTION	Transparency Color Key Selection (secondary LCD output) wr: VFP start period of secondary LCD output 0x0: Destination transparency color key selected 0x1: Source transparency color key selected	RW	0
10	TCKLCDENABLE	Transparency Color Key Enabled (secondary LCD output) wr: VFP start period of secondary LCD output 0x0: Disable the transparency color key for the LCD 0x1: Enable the transparency color key for the LCD	RW	0
9	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0
8	ACBIASGATED	ACBias Gated Enabled (secondary LCD output) wr: VFP start period of secondary LCD output 0x0: AcBias Gated Disabled 0x1: AcBias Gated Enabled	RW	0
7	VSYNCGATED	VSYNC Gated Enabled (secondary LCD output) wr: VFP start period of secondary LCD output 0x0: VSYNC Gated Disabled 0x1: VSYNC Gated Enabled	RW	0
6	HSYNCGATED	HSYNC Gated Enabled (secondary LCD output) wr: VFP start period of secondary LCD output 0x0: HSYNC Gated Disabled 0x1: HSYNC Gated Enabled	RW	0
5	PIXELCLOCK GATED	Pixel Clock Gated Enabled (secondary LCD output) wr: VFP start period of secondary LCD output 0x0: Pixel Clock Gated Disabled 0x1: Pixel Clock Gated Enabled	RW	0
4	PIXELDATA GATED	Pixel Data Gated Enabled (secondary LCD output) wr: VFP start period of secondary LCD output 0x0: Pixel Data Gated Disabled 0x1: Pixel Data Gated Enabled	RW	0
3:1	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0
0	PIXELGATED	Pixel Gated Enable (only for Active Matrix) (secondary LCD output) wr: VFP start period of secondary LCD output 0x0: Pixel clock always toggles (only in Active Matrix mode) 0x1: Pixel clock only toggles when there is valid data to display. (only in Active Matrix mode)	RW	0

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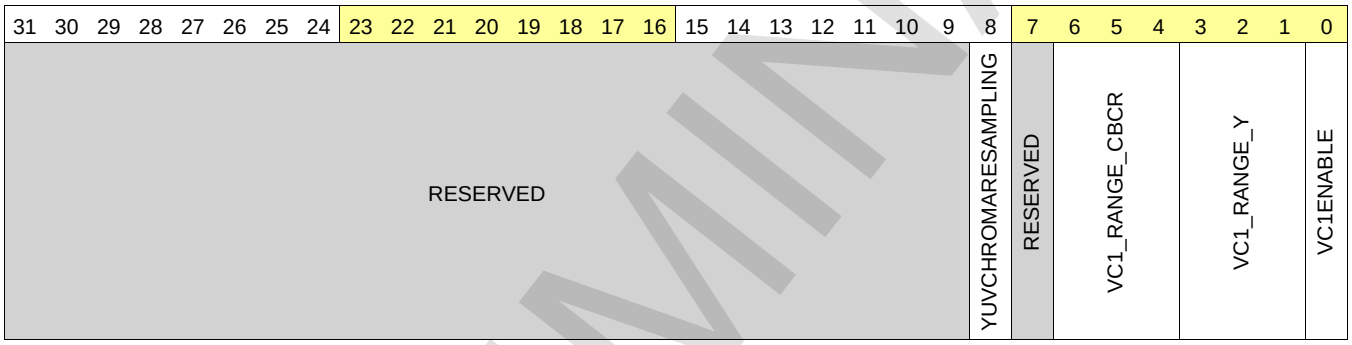
Table 10-402. Register Call Summary for Register DISPC_CONFIG2

Display Controller

- Overlay Manager: [0] [1] [2]
- Shadow Registers: [3]
- Display Controller Logical Register Mapping: [4]
- Display Controller Register Summary: [5]

Table 10-403. DISPC_VID1_ATTRIBUTES2

Address Offset	0x0000 0624		
Physical Address	0x4804 1624 0x5800 1624	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the attributes of the video window 1. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:9	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x000000
8	YUVCHROMARESAMPLING	The YUV chrominance can be resampled using averaging of the adjacent chrominance samples, without using the polyphase filter for 4:2:2 input or can be calculated using the polyphase filter for 4:2:2/4:2:0. The polyphase filter is mandatory for the 4:2:0 format. This bit controls the order in which the processing is done on the video pipe. 0x0: When input is 4:2:2, the missing chrominance samples are calculated by averaging the adjacent samples if DISPC_VID1_ATTRIBUTES.ROTATION=0 only. Other rotation configurations are not supported. 0x1: For 4:2:2 (or 4:2:0), the missing chrominance samples are calculated by filtering the adjacent samples (5-tap polyphase filter). See Figure 10-48, *Configuration 2: Video Pipeline*. All rotation configurations are supported.	RW	0
7	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0
6:4	VC1_RANGE_CBCR	Defines the VC-1 range value for the CbCr component from 0 to 7.	RW	0x0
3:1	VC1_RANGE_Y	Defines the VC-1 range value for the Y component from 0 to 7.	RW	0x0
0	VC1ENABLE	Enable/disable the VC-1 range mapping processing. The bit field is ignored if the format is not one of the supported YUV formats. 0x0: VC-1 range mapping disabled 0x1: VC-1 range mapping enabled	RW	0

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Table 10-404. Register Call Summary for Register DISPC_VID1_ATTRIBUTES2

Display Controller

- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1]
- Display Controller Register Summary: [2]

Table 10-405. DISPC_VID2_ATTRIBUTES2

Address Offset	0x0000 0628		
Physical Address	0x4804 1628 0x5800 1628	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the attributes of the video window 2. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							YUVCHROMARESAMPLING	RESERVED		VC1_RANGE_CBCR			VC1_RANGE_Y		VC1ENABLE

Bits	Field Name	Description	Type	Reset
31:9	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x000000
8	YUVCHROMARESAMPLING	The YUV chrominance can be resampled using averaging of the adjacent chrominance samples, without using the polyphase filter for 4:2:2 input or can be calculated using the polyphase filter for 4:2:2/4:2:0. The polyphase filter is mandatory for the 4:2:0 format. This bit controls the order in which the processing is done on the video pipe. 0x0: When input is in 4:2:2, the missing chrominance samples are calculated by averaging the adjacent samples if DISPC_VID1_ATTRIBUTES. ROTATION=0 only. Other rotation configurations are not supported. 0x1: For 4:2:2 (or 4:2:0), the missing chrominance samples are calculated by filtering the adjacent samples (5-tap polyphase filter). See Figure 10-48, *Configuration 2: Video Pipeline*. All rotation configurations are supported.	RW	0
7	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0
6:4	VC1_RANGE_CBCR	Defines the VC-1 range value for the CbCr component from 0 to 7.	RW	0x0
3:1	VC1_RANGE_Y	Defines the VC-1 range value for the Y component from 0 to 7.	RW	0x0
0	VC1ENABLE	Enable/disable the VC-1 range mapping processing. The bit field is ignored if the format is not one of the supported YUV formats. 0x0: VC-1 range mapping disabled 0x1: VC-1 range mapping enabled	RW	0

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Table 10-406. Register Call Summary for Register DISPC_VID2_ATTRIBUTES2

Display Controller

- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1]
- Display Controller Register Summary: [2]

Table 10-407. DISPC_VID3_ATTRIBUTES2

Address Offset	0x0000 062C		
Physical Address	0x4804 162C 0x5800 162C	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the attributes of the video window 3. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							YUVCHROMARESAMPLING	RESERVED		VC1_RANGE_CBCR		VC1_RANGE_Y		VC1ENABLE	

Bits	Field Name	Description	Type	Reset
31:9	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x000000
8	YUVCHROMARESAMPLING	The YUV chrominance can be resampled using averaging of the adjacent chrominance samples, without using the polyphase filter for 4:2:2 input or can be calculated using the polyphase filter for 4:2:2/4:2:0. The polyphase filter is mandatory for the 4:2:0 format. This bit controls the order in which the processing is done on the video pipe. 0x0: When input is in 4:2:2, the missing chrominance samples are calculated by averaging the adjacent samples if DISPC_VID1_ATTRIBUTES. ROTATION=0 only. Other rotation configurations are not supported. 0x1: For 4:2:2 (or 4:2:0), the missing chrominance samples are calculated by filtering the adjacent samples (5-tap polyphase filter). See Figure 10-48, *Configuration 2: Video Pipeline*. All rotation configurations are supported.	RW	0
7	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0
6:4	VC1_RANGE_CBCR	Defines the VC-1 range value for the CbCr component from 0 to 7.	RW	0x0
3:1	VC1_RANGE_Y	Defines the VC-1 range value for the Y component from 0 to 7.	RW	0x0
0	VC1ENABLE	Enable/disable the VC-1 range mapping processing. The bit field is ignored if the format is not one of the supported YUV formats. 0x0: VC-1 range mapping disabled 0x1: VC-1 range mapping enabled	RW	0

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Table 10-408. Register Call Summary for Register DISPC_VID3_ATTRIBUTES2

Display Controller

- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1]
- Display Controller Register Summary: [2]

Table 10-409. DISPC_GAMMA_TABLE0

Address Offset	0x0000 0630		
Physical Address	0x4804 1630 0x5800 1630	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the look up table used as color look up table for BITMAP formats (1-, 2-, 4, and 8-bpp) on the graphics pipeline or as gamma table on the primary LCD output.		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INDEX								VALUE_R								VALUE_G								VALUE_B							

Bits	Field Name	Description	Type	Reset
31:24	INDEX	Defines the location in the table where the bit field VALUE is stored.	W	0x00
23:16	VALUE_R	8-bit value used to defined the value to store at the location in the table defined by the bit field INDEX.	W	0x00
15:8	VALUE_G	8-bit value used to defined the value to store at the location in the table defined by the bit field INDEX.	W	0x00
7:0	VALUE_B	8-bit value used to defined the value to store at the location in the table defined by the bit field INDEX.	W	0x00

Table 10-410. Register Call Summary for Register DISPC_GAMMA_TABLE0

Display Controller

- Shadow Registers: [0]
- Operational Modes Configuration: [1] [2]
- Display Controller Logical Register Mapping: [3]
- Display Controller Register Summary: [4]

Table 10-411. DISPC_GAMMA_TABLE1

Address Offset	0x0000 0634		
Physical Address	0x4804 1634 0x5800 1634	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the gamma table on the secondary LCD output.		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INDEX								VALUE_R								VALUE_G								VALUE_B							

Bits	Field Name	Description	Type	Reset
31:24	INDEX	Defines the location in the table where the bit field VALUE is stored.	W	0x00
23:16	VALUE_R	8-bit value used to defined the value to store at the location in the table defined by the bit field INDEX.	W	0x00
15:8	VALUE_G	8-bit value used to defined the value to store at the location in the table defined by the bit field INDEX.	W	0x00
7:0	VALUE_B	8-bit value used to defined the value to store at the location in the table defined by the bit field INDEX.	W	0x00

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Table 10-412. Register Call Summary for Register DISPC_GAMMA_TABLE1

Display Controller

- Shadow Registers: [0]
- Operational Modes Configuration: [1]
- Display Controller Logical Register Mapping: [2]
- Display Controller Register Summary: [3]

Table 10-413. DISPC_GAMMA_TABLE2

Address Offset	0x0000 0638		
Physical Address	0x4804 1638 0x5800 1638	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the gamma table on the TV output.		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INDEX	RESERVED	VALUE_R														VALUE_G								VALUE_B							

Bits	Field Name	Description	Type	Reset
31	INDEX	Setting this bit to 1 resets the internal index counter to zero. Each subsequent access to the register (with the INDEX bit kept at 0) increments the address for the next storage location into the table memory.	W	0
30	RESERVED		W	0
29:20	VALUE_R	10-bit color component value to store in the table.	W	0x000
19:10	VALUE_G	10-bit color component value to store in the table.	W	0x000
9:0	VALUE_B	10-bit color component value to store in the table.	W	0x000

Table 10-414. Register Call Summary for Register DISPC_GAMMA_TABLE2

Display Controller

- Gamma Correction Unit: [0]
- Shadow Registers: [1]
- Operational Modes Configuration: [2]
- Display Controller Logical Register Mapping: [3]
- Display Controller Register Summary: [4]

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Table 10-415. DISPC_VID1_FIR2

Address Offset	0x0000 063C		
Physical Address	0x4804 163C 0x5800 163C	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the resize factors for horizontal and vertical up/downsampling of the video window 1. It is used for Crb and Cr setting. It is used only when the pixel format at the input of the filter is one of the YUV formats. If the pixel format at the input of the filter is ARGB (all ARGB, RGB, RGBA are converted to ARGB32-8888 by the color space conversion before going to the filter is the color space conversion is done before the filter). When the register is not used by the hardware, any value can be used for the bit fields. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								FIRVINC								RESERVED								FIRHINC							

Bits	Field Name	Description	Type	Reset
31:29	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0
28:16	FIRVINC	Vertical increment of the up/downsampling filter for Cb and Cr. Encoded value (from 1 to 4096). The value 0 is invalid. The values greater than 4096 are invalid.	RW	0x0400
15:13	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0
12:0	FIRHINC	Horizontal increment of the up/downsampling filter for Cb and Cr. Encoded value (from 1 to 4096). The value 0 is invalid. The values greater than 4096 are invalid.	RW	0x0400

Table 10-416. Register Call Summary for Register DISPC_VID1_FIR2

Display Controller

- Shadow Registers: [0]
- Display Controller Register Summary: [1]

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Table 10-417. DISPC_VID1_ACCU2_j

Address Offset	0x0000 0640 + (0x4 * j)	**Index**	j = 0 to 1
Physical Address	0x4804 1640 + (0x4 * j) 0x5800 1640 + (0x4 * j)	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the resize accumulator init values for horizontal and vertical up/downsampling of the video window 1 (DISPC_VID1_ACCU2_0 DISPC_VID1_ACCU2_1 for ping-pong mechanism with external trigger, based on the field polarity) It is used for Cb and Cr setting. It is used only when the pixel format at the input of the filter is one of the YUV formats. If the pixel format at the input of the filter is ARGB (all ARGB, RGB, RGBA are converted to ARGB32-8888 by the color space conversion before going to the filter is the color space conversion is done before the filter). When the register is not used by the hardware, any value can be used for the bit fields. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								VERTICALACCU								RESERVED								HORIZONTALACCU							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
26:16	VERTICALACCU	Vertical initialization accu value Encoded value (from -1024 to 1023).	RW	0x000
15:11	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
10:0	HORIZONTALACCU	Horizontal initialization accu value Encoded value (from -1024 to 1023).	RW	0x000

Table 10-418. Register Call Summary for Register DISPC_VID1_ACCU2_j

Display Controller

- Shadow Registers: [0]
- Display Controller Register Summary: [1]

Table 10-419. DISPC_VID1_FIR_COEF_H2_i

Address Offset	0x0000 0648 + (0x8 * i)	**Index**	i = 0 to 7
Physical Address	0x4804 1648 + (0x8 * i) 0x5800 1648 + (0x8 * i)	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The bank of registers configure the up/down-scaling coefficients for the horizontal resize of the video picture associated with the video window 1 for the phases from 0 to 7. It is used for Crb and Cr setting. It is used only when the pixel format at the input of the filter is one of the YUV formats. If the pixel format at the input of the filter is ARGB (all ARGB, RGB, RGBA are converted to ARGB32-8888 by the color space conversion before going to the filter is the color space conversion is done before the filter). When the register is not used by the hardware, any value can be used for the bit fields. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIRHC3								FIRHC2								FIRHC1								FIRHC0							

Bits	Field Name	Description	Type	Reset
31:24	FIRHC3	Signed coefficient C3 for the horizontal up/down-scaling with the phase n	RW	0x00
23:16	FIRHC2	Unsigned coefficient C2 for the horizontal up/down-scaling with the phase n	RW	0x00
15:8	FIRHC1	Signed coefficient C1 for the horizontal up/down-scaling with the phase n	RW	0x00

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Bits	Field Name	Description	Type	Reset
7:0	FIRHC0	Signed coefficient C0 for the horizontal up/down-scaling with the phase n	RW	0x00

Table 10-420. Register Call Summary for Register DISPC_VID1_FIR_COEF_H2_i

Display Controller
- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1]
- Display Controller Register Summary: [2]

Table 10-421. DISPC_VID1_FIR_COEF_HV2_i

Address Offset	0x0000 064C + (0x8 * i)	**Index**	i = 0 to 7
Physical Address	0x4804 164C + (0x8 * i) 0x5800 164C + (0x8 * i)	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The bank of registers configure the down/up/down-scaling coefficients for the vertical and horizontal resize of the video picture associated with the video window 1 for the phases from 0 to 7. It is used for Crb and Cr setting. It is used only when the pixel format at the input of the filter is one of the YUV formats. If the pixel format at the input of the filter is ARGB (all ARGB, RGB, RGBA are converted to ARGB32-8888 by the color space conversion before going to the filter is the color space conversion is done before the filter). When the register is not used by the hardware, any value can be used for the bit fields. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIRVC2								FIRVC1								FIRVC0								FIRHC4							

Bits	Field Name	Description	Type	Reset
31:24	FIRVC2	Signed coefficient C2 for the vertical up/down-scaling with the phase n	RW	0x00
23:16	FIRVC1	Unsigned coefficient C1 for the vertical up/down-scaling with the phase n	RW	0x00
15:8	FIRVC0	Signed coefficient C0 for the vertical up/down-scaling with the phase n	RW	0x00
7:0	FIRHC4	Signed coefficient C4 for the horizontal up/down-scaling with the phase n	RW	0x00

Table 10-422. Register Call Summary for Register DISPC_VID1_FIR_COEF_HV2_i

Display Controller
- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1]
- Display Controller Register Summary: [2]

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Table 10-423. DISPC_VID1_FIR_COEF_V2_i

Address Offset	0x0000 0688 + (0x4 * i)	**Index**	i = 0 to 7
Physical Address	0x4804 1688 + (0x4 * i) 0x5800 1688 + (0x4 * i)	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The bank of registers configure the down/up/down-scaling coefficients for the vertical resize of the video picture associated with the video window 1 for the phases from 0 to 7. It is used for Crb and Cr setting. It is used only when the pixel format at the input of the filter is one of the YUV formats. If the pixel format at the input of the filter is ARGB (all ARGB, RGB, RGBA are converted to ARGB32-8888 by the color space conversion before going to the filter is the color space conversion is done before the filter). When the register is not used by the hardware, any value can be used for the bit fields. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																FIRVC22								FIRVC00							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0000
15:8	FIRVC22	Signed coefficient C22 for the vertical up/down-scaling with the phase n	RW	0x00
7:0	FIRVC00	Signed coefficient C00 for the vertical up/down-scaling with the phase n	RW	0x00

Table 10-424. Register Call Summary for Register DISPC_VID1_FIR_COEF_V2_i

Display Controller

- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1]
- Display Controller Register Summary: [2]

Table 10-425. DISPC_VID2_FIR2

Address Offset	0x0000 06A8		
Physical Address	0x4804 16A8 0x5800 16A8	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the resize factors for horizontal and vertical up/downsampling of the video window 2. It is used for Crb and Cr setting. It is used only when the pixel format at the input of the filter is one of the YUV formats. If the pixel format at the input of the filter is ARGB (all ARGB, RGB, RGBA are converted to ARGB32-8888 by the color space conversion before going to the filter is the color space conversion is done before the filter). When the register is not used by the hardware, any value can be used for the bit fields. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								FIRVINC								RESERVED								FIRHINC							

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Bits	Field Name	Description	Type	Reset
31:29	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0
28:16	FIRVINC	Vertical increment of the up/downsampling filter for Cb and Cr. Encoded value (from 1 to 4096). The value 0 is invalid. The values greater than 4096 are invalid.	RW	0x0400
15:13	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0
12:0	FIRHINC	Horizontal increment of the up/downsampling filter for Cb and Cr. Encoded value (from 1 to 4096). The value 0 is invalid. The values greater than 4096 are invalid.	RW	0x0400

Table 10-426. Register Call Summary for Register DISPC_VID2_FIR2

Display Controller

- Shadow Registers: [0]
- Display Controller Register Summary: [1]

Table 10-427. DISPC_VID2_ACCU2_j

Address Offset	0x0000 06AC + (0x4 * j)	**Index**	j = 0 to 1
Physical Address	0x4804 16AC + (0x4 * j) 0x5800 16AC + (0x4 * j)	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the resize accumulator init values for horizontal and vertical up/downsampling of the video window 2 (DISPC_VID2_ACCU2_0 DISPC_VID2_ACCU2_1 for ping-pong mechanism with external trigger, based on the field polarity). It is used for Cb and Cr setting. It is used only when the pixel format at the input of the filter is one of the YUV formats. If the pixel format at the input of the filter is ARGB (all ARGB, RGB, RGBA are converted to ARGB32-8888 by the color space conversion before going to the filter is the color space conversion is done before the filter). When the register is not used by the hardware, any value can be used for the bit fields. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								VERTICALACCU								RESERVED								HORIZONTALACCU							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
26:16	VERTICALACCU	Vertical initialization accu value Encoded value (from -1024 to 1023).	RW	0x000
15:11	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
10:0	HORIZONTALACCU	Horizontal initialization accu value Encoded value (from -1024 to 1023).	RW	0x000

Table 10-428. Register Call Summary for Register DISPC_VID2_ACCU2_j

Display Controller

- Shadow Registers: [0]
- Display Controller Register Summary: [1]

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Table 10-429. DISPC_VID2_FIR_COEF_H2_i

Address Offset	0x0000 06B4 + (0x8 * i)	**Index**	i = 0 to 7
Physical Address	0x4804 16B4 + (0x8 * i) 0x5800 16B4 + (0x8 * i)	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The bank of registers configure the up/down-scaling coefficients for the horizontal resize of the video picture associated with the video window 2 for the phases from 0 to 7. It is used for Crb and Cr setting. It is used only when the pixel format at the input of the filter is one of the YUV formats. If the pixel format at the input of the filter is ARGB (all ARGB, RGB, RGBA are converted to ARGB32-8888 by the color space conversion before going to the filter is the color space conversion is done before the filter). When the register is not used by the hardware, any value can be used for the bit fields. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIRHC3								FIRHC2								FIRHC1								FIRHC0							

Bits	Field Name	Description	Type	Reset
31:24	FIRHC3	Signed coefficient C3 for the horizontal up/down-scaling with the phase n	RW	0x00
23:16	FIRHC2	Unsigned coefficient C2 for the horizontal up/down-scaling with the phase n	RW	0x00
15:8	FIRHC1	Signed coefficient C1 for the horizontal up/down-scaling with the phase n	RW	0x00
7:0	FIRHC0	Signed coefficient C0 for the horizontal up/down-scaling with the phase n	RW	0x00

Table 10-430. Register Call Summary for Register DISPC_VID2_FIR_COEF_H2_i

Display Controller

- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1]
- Display Controller Register Summary: [2]

Table 10-431. DISPC_VID2_FIR_COEF_HV2_i

Address Offset	0x0000 06B8 + (0x8 * i)	**Index**	i = 0 to 7
Physical Address	0x4804 16B8 + (0x8 * i) 0x5800 16B8 + (0x8 * i)	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The bank of registers configure the down/up/down-scaling coefficients for the vertical and horizontal resize of the video picture associated with the video window 2 for the phases from 0 to 7. It is used for Crb and Cr setting. It is used only when the pixel format at the input of the filter is one of the YUV formats. If the pixel format at the input of the filter is ARGB (all ARGB, RGB, RGBA are converted to ARGB32-8888 by the color space conversion before going to the filter is the color space conversion is done before the filter). When the register is not used by the hardware, any value can be used for the bit fields. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIRVC2								FIRVC1								FIRVC0								FIRHC4							

Bits	Field Name	Description	Type	Reset
31:24	FIRVC2	Signed coefficient C2 for the vertical up/down-scaling with the phase n	RW	0x00
23:16	FIRVC1	Unsigned coefficient C1 for the vertical up/down-scaling with the phase n	RW	0x00
15:8	FIRVC0	Signed coefficient C0 for the vertical up/down-scaling with the phase n	RW	0x00

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Bits	Field Name	Description	Type	Reset
7:0	FIRHC4	Signed coefficient C4 for the horizontal up/down-scaling with the phase n	RW	0x00

Table 10-432. Register Call Summary for Register DISPC_VID2_FIR_COEF_HV2_i

Display Controller
- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1]
- Display Controller Register Summary: [2]

Table 10-433. DISPC_VID2_FIR_COEF_V2_i

Address Offset	0x0000 06F4 + (0x4 * i)	**Index**	i = 0 to 7
Physical Address	0x4804 16F4 + (0x4 * i) 0x5800 16F4 + (0x4 * i)	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The bank of registers configure the down/up/down-scaling coefficients for the vertical resize of the video picture associated with the video window 2 for the phases from 0 to 7. It is used for Crb and Cr setting. It is used only when the pixel format at the input of the filter is one of the YUV formats. If the pixel format at the input of the filter is ARGB (all ARGB, RGB, RGBA are converted to ARGB32-8888 by the color space conversion before going to the filter is the color space conversion is done before the filter). When the register is not used by the hardware, any value can be used for the bit fields. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																FIRVC22								FIRVC00							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0000
15:8	FIRVC22	Signed coefficient C22 for the vertical up/down-scaling with the phase n	RW	0x00
7:0	FIRVC00	Signed coefficient C00 for the vertical up/down-scaling with the phase n	RW	0x00

Table 10-434. Register Call Summary for Register DISPC_VID2_FIR_COEF_V2_i

Display Controller
- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1]
- Display Controller Register Summary: [2]

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Table 10-435. DISPC_VID3_FIR2

Address Offset	0x0000 0724		
Physical Address	0x4804 1724 0x5800 1724	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the resize factors for horizontal and vertical up/downsampling of the video window 3. It is used for Crb and Cr setting. It is used only when the pixel format at the input of the filter is one of the YUV formats. If the pixel format at the input of the filter is ARGB (all ARGB, RGB, RGBA are converted to ARGB32-8888 by the color space conversion before going to the filter is the color space conversion is done before the filter). When the register is not used by the hardware, any value can be used for the bit fields. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								FIRVINC								RESERVED								FIRHINC							

Bits	Field Name	Description	Type	Reset
31:29	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0
28:16	FIRVINC	Vertical increment of the up/downsampling filter for Cb and Cr. Encoded value (from 1 to 4096). The value 0 is invalid. The values greater than 4096 are invalid.	RW	0x0400
15:13	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0
12:0	FIRHINC	Horizontal increment of the up/downsampling filter for Cb and Cr. Encoded value (from 1 to 4096). The value 0 is invalid. The values greater than 4096 are invalid.	RW	0x0400

Table 10-436. Register Call Summary for Register DISPC_VID3_FIR2

Display Controller

- Shadow Registers: [0]
- Display Controller Register Summary: [1]

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Table 10-437. DISPC_VID3_ACCU2_j

Address Offset	0x0000 0728 + (0x4 * j)	**Index**	j = 0 to 1
Physical Address	0x4804 1728 + (0x4 * j) 0x5800 1728 + (0x4 * j)	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the resize accumulator init values for horizontal and vertical up/downsampling of the video window 3 (DISPC_VID3_ACCU2_0 DISPC_VID3_ACCU2_1 for ping-pong mechanism with external trigger, based on the field polarity). It is used for Cb and Cr setting. It is used only when the pixel format at the input of the filter is one of the YUV formats. If the pixel format at the input of the filter is ARGB (all ARGB, RGB, RGBA are converted to ARGB32-8888 by the color space conversion before going to the filter is the color space conversion is done before the filter). When the register is not used by the hardware, any value can be used for the bit fields. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								VERTICALACCU								RESERVED								HORIZONTALACCU							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
26:16	VERTICALACCU	Vertical initialization accu value Encoded value (from -1024 to 1023).	RW	0x000
15:11	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
10:0	HORIZONTALACCU	Horizontal initialization accu value Encoded value (from -1024 to 1023).	RW	0x000

Table 10-438. Register Call Summary for Register DISPC_VID3_ACCU2_j

Display Controller

- Shadow Registers: [0]
- Display Controller Register Summary: [1]

Table 10-439. DISPC_VID3_FIR_COEF_H2_i

Address Offset	0x0000 0730 + (0x8 * i)	**Index**	i = 0 to 7
Physical Address	0x4804 1730 + (0x8 * i) 0x5800 1730 + (0x8 * i)	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The bank of registers configure the up/down-scaling coefficients for the horizontal resize of the video picture associated with the video window 3 for the phases from 0 to 7. It is used for Crb and Cr setting. It is used only when the pixel format at the input of the filter is one of the YUV formats. If the pixel format at the input of the filter is ARGB (all ARGB, RGB, RGBA are converted to ARGB32-8888 by the color space conversion before going to the filter is the color space conversion is done before the filter). When the register is not used by the hardware, any value can be used for the bit fields. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIRHC3								FIRHC2								FIRHC1								FIRHC0							

Bits	Field Name	Description	Type	Reset
31:24	FIRHC3	Signed coefficient C3 for the horizontal up/down-scaling with the phase n	RW	0x00
23:16	FIRHC2	Unsigned coefficient C2 for the horizontal up/down-scaling with the phase n	RW	0x00
15:8	FIRHC1	Signed coefficient C1 for the horizontal up/down-scaling with the phase n	RW	0x00

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Bits	Field Name	Description	Type	Reset
7:0	FIRHC0	Signed coefficient C0 for the horizontal up/down-scaling with the phase n	RW	0x00

Table 10-440. Register Call Summary for Register DISPC_VID3_FIR_COEF_H2_i

Display Controller
- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1]
- Display Controller Register Summary: [2]

Table 10-441. DISPC_VID3_FIR_COEF_HV2_i

Address Offset	0x0000 0734 + (0x8 * i)	**Index**	i = 0 to 7
Physical Address	0x4804 1734 + (0x8 * i) 0x5800 1734 + (0x8 * i)	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The bank of registers configure the down/up/down-scaling coefficients for the vertical and horizontal resize of the video picture associated with the video window 3 for the phases from 0 to 7. It is used for Crb and Cr setting. It is used only when the pixel format at the input of the filter is one of the YUV formats. If the pixel format at the input of the filter is ARGB (all ARGB, RGB, RGBA are converted to ARGB32-8888 by the color space conversion before going to the filter is the color space conversion is done before the filter). When the register is not used by the hardware, any value can be used for the bit fields. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIRVC2								FIRVC1								FIRVC0								FIRHC4							

Bits	Field Name	Description	Type	Reset
31:24	FIRVC2	Signed coefficient C2 for the vertical up/down-scaling with the phase n	RW	0x00
23:16	FIRVC1	Unsigned coefficient C1 for the vertical up/down-scaling with the phase n	RW	0x00
15:8	FIRVC0	Signed coefficient C0 for the vertical up/down-scaling with the phase n	RW	0x00
7:0	FIRHC4	Signed coefficient C4 for the horizontal up/down-scaling with the phase n	RW	0x00

Table 10-442. Register Call Summary for Register DISPC_VID3_FIR_COEF_HV2_i

Display Controller
- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1]
- Display Controller Register Summary: [2]

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Table 10-443. DISPC_VID3_FIR_COEF_V2_i

Address Offset	0x0000 0770 + (0x4 * i)	**Index**	i = 0 to 7
Physical Address	0x4804 1770 + (0x4 * i) 0x5800 1770 + (0x4 * i)	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The bank of registers configure the down/up/down-scaling coefficients for the vertical resize of the video picture associated with the video window 3 for the phases from 0 to 7. It is used for Crb and Cr setting. It is used only when the pixel format at the input of the filter is one of the YUV formats. If the pixel format at the input of the filter is ARGB (all ARGB, RGB, RGBA are converted to ARGB32-8888 by the color space conversion before going to the filter is the color space conversion is done before the filter). When the register is not used by the hardware, any value can be used for the bit fields. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																FIRVC22								FIRVC00							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0000
15:8	FIRVC22	Signed coefficient C22 for the vertical up/down-scaling with the phase n	RW	0x00
7:0	FIRVC00	Signed coefficient C00 for the vertical up/down-scaling with the phase n	RW	0x00

Table 10-444. Register Call Summary for Register DISPC_VID3_FIR_COEF_V2_i

Display Controller

- Shadow Registers: [0]
- Display Controller Logical Register Mapping: [1]
- Display Controller Register Summary: [2]

Table 10-445. DISPC_WB_FIR2

Address Offset	0x0000 0790		
Physical Address	0x4804 1790 0x5800 1790	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the resize factors for horizontal and vertical up/downsampling of the write-back pipeline. It is used for Crb and Cr setting. It is used only when the pixel format at the input of the filter is one of the YUV formats. If the pixel format at the input of the filter is ARGB (all ARGB, RGB, RGBA are converted to ARGB32-8888 by the color space conversion before going to the filter is the color space conversion is done before the filter). When the register is not used by the hardware, any value can be used for the bit fields. Shadow register, updated when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline) when the WB pipeline is directly connected to one of the pipelines (graphics or video), otherwise updated on VFP start period of primary LCD or VFP start period of secondary LCD or EVSYNC depending on which overlay output is selected as an input to the WB pipeline		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								FIRVINC								RESERVED								FIRHINC							

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Bits	Field Name	Description	Type	Reset
31:29	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0
28:16	FIRVINC	Vertical increment of the up/downsampling filter for Cb and Cr. Encoded value (from 1 to 4096). The value 0 is invalid. The values greater than 4096 are invalid.	RW	0x0400
15:13	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0
12:0	FIRHINC	Horizontal increment of the up/downsampling filter for Cb and Cr. Encoded value (from 1 to 4096). The value 0 is invalid. The values greater than 4096 are invalid.	RW	0x0400

Table 10-446. Register Call Summary for Register DISPC_WB_FIR2

Display Controller

- Shadow Registers: [0]
- Operational Modes Configuration: [1] [2]
- Display Controller Register Summary: [3]

Table 10-447. DISPC_WB_ACCU2_j

Address Offset	0x0000 0794 + (0x4 * j)	**Index**	j = 0 to 1
Physical Address	0x4804 1794 + (0x4 * j) 0x5800 1794 + (0x4 * j)	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the resize accumulator init values for horizontal and vertical up/downsampling of the write back pipeline (DISPC_WB_ACCU2_0 DISPC_WB_ACCU2_1 for ping-pong mechanism with external trigger, based on the field polarity). It is used for Cb and Cr setting. It is used only when the pixel format at the input of the filter is one of the YUV formats. If the pixel format at the input of the filter is ARGB (all ARGB, RGB, RGBA are converted to ARGB32-8888 by the color space conversion before going to the filter is the color space conversion is done before the filter). When the register is not used by the hardware, any value can be used for the bit fields. Shadow register, updated when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline) when the WB pipeline is directly connected to one of the pipelines (graphics or video), otherwise updated on VFP start period of primary LCD or VFP start period of secondary LCD or EVSYNC depending on which overlay output is selected as an input to the WB pipeline		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					VERTICALACCU											RESERVED					HORIZONTALACCU										

Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
26:16	VERTICALACCU	Vertical initialization accu value Encoded value (from -1024 to 1023).	RW	0x000
15:11	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
10:0	HORIZONTALACCU	Horizontal initialization accu value Encoded value (from -1024 to 1023).	RW	0x000

Table 10-448. Register Call Summary for Register DISPC_WB_ACCU2_j

Display Controller

- Shadow Registers: [0]
- Operational Modes Configuration: [1] [2]
- Display Controller Register Summary: [3]

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Table 10-449. DISPC_WB_FIR_COEF_H2_i

Address Offset	0x0000 07A0 + (0x8 * i)	**Index**	i = 0 to 7
Physical Address	0x4804 17A0 + (0x8 * i) 0x5800 17A0 + (0x8 * i)	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The bank of registers configure the up/down-scaling coefficients for the horizontal resize of the video picture associated with the write back pipeline for the phases from 0 to 7. It is used for Crb and Cr setting. It is used only when the pixel format at the input of the filter is one of the YUV formats. If the pixel format at the input of the filter is ARGB (all ARGB, RGB, RGBA are converted to ARGB32-8888 by the color space conversion before going to the filter is the color space conversion is done before the filter). When the register is not used by the hardware, any value can be used for the bit fields. Shadow register, updated when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline) when the WB pipeline is directly connected to one of the pipelines (graphics or video), otherwise updated on VFP start period of primary LCD or VFP start period of secondary LCD or EVSYNC depending on which overlay output is selected as an input to the WB pipeline		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIRHC3								FIRHC2								FIRHC1								FIRHC0							

Bits	Field Name	Description	Type	Reset
31:24	FIRHC3	Signed coefficient C3 for the horizontal up/down-scaling with the phase n	RW	0x00
23:16	FIRHC2	Unsigned coefficient C2 for the horizontal up/down-scaling with the phase n	RW	0x00
15:8	FIRHC1	Signed coefficient C1 for the horizontal up/down-scaling with the phase n	RW	0x00
7:0	FIRHC0	Signed coefficient C0 for the horizontal up/down-scaling with the phase n	RW	0x00

Table 10-450. Register Call Summary for Register DISPC_WB_FIR_COEF_H2_i

Display Controller

- Scaler Unit: [0] [1] [2] [3] [4]
- Shadow Registers: [5]
- Operational Modes Configuration: [6]
- Display Controller Register Summary: [7]

Table 10-451. DISPC_WB_FIR_COEF_HV2_i

Address Offset	0x0000 07A4 + (0x8 * i)	**Index**	i = 0 to 7
Physical Address	0x4804 17A4 + (0x8 * i) 0x5800 17A4 + (0x8 * i)	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The bank of registers configure the down/up/down-scaling coefficients for the vertical and horizontal resize of the video picture associated with the write back pipeline for the phases from 0 to 7. It is used for Crb and Cr setting. It is used only when the pixel format at the input of the filter is one of the YUV formats. If the pixel format at the input of the filter is ARGB (all ARGB, RGB, RGBA are converted to ARGB32-8888 by the color space conversion before going to the filter is the color space conversion is done before the filter). When the register is not used by the hardware, any value can be used for the bit fields. Shadow register, updated when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline) when the WB pipeline is directly connected to one of the pipelines (graphics or video), otherwise updated on VFP start period of primary LCD or VFP start period of secondary LCD or EVSYNC depending on which overlay output is selected as an input to the WB pipeline		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIRVC2								FIRVC1								FIRVC0								FIRHC4							

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Bits	Field Name	Description	Type	Reset
31:24	FIRVC2	Signed coefficient C2 for the vertical up/down-scaling with the phase n	RW	0x00
23:16	FIRVC1	Unsigned coefficient C1 for the vertical up/down-scaling with the phase n	RW	0x00
15:8	FIRVC0	Signed coefficient C0 for the vertical up/down-scaling with the phase n	RW	0x00
7:0	FIRHC4	Signed coefficient C4 for the horizontal up/down-scaling with the phase n	RW	0x00

Table 10-452. Register Call Summary for Register DISPC_WB_FIR_COEF_HV2_i

Display Controller

- Scaler Unit: [0] [1] [2] [3] [4] [5]
- Shadow Registers: [6]
- Operational Modes Configuration: [7] [8]
- Display Controller Register Summary: [9]

Table 10-453. DISPC_WB_FIR_COEF_V2_i

Address Offset	0x0000 07E0 + (0x4 * i)	**Index**	i = 0 to 7
Physical Address	0x4804 17E0 + (0x4 * i) 0x5800 17E0 + (0x4 * i)	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The bank of registers configure the down/up/down-scaling coefficients for the vertical resize of the video picture associated with the write back pipeline for the phases from 0 to 7. It is used for Crb and Cr setting. It is used only when the pixel format at the input of the filter is one of the YUV formats. If the pixel format at the input of the filter is ARGB (all ARGB, RGB, RGBA are converted to ARGB32-8888 by the color space conversion before going to the filter is the color space conversion is done before the filter). When the register is not used by the hardware, any value can be used for the bit fields. Shadow register, updated when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline) when the WB pipeline is directly connected to one of the pipelines (graphics or video), otherwise updated on VFP start period of primary LCD or VFP start period of secondary LCD or EVSYNC depending on which overlay output is selected as an input to the WB pipeline		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																FIRVC22								FIRVC00							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0000
15:8	FIRVC22	Signed coefficient C22 for the vertical up/down-scaling with the phase n	RW	0x00
7:0	FIRVC00	Signed coefficient C00 for the vertical up/down-scaling with the phase n	RW	0x00

Table 10-454. Register Call Summary for Register DISPC_WB_FIR_COEF_V2_i

Display Controller

- Scaler Unit: [0] [1] [2]
- Shadow Registers: [3]
- Operational Modes Configuration: [4]
- Display Controller Register Summary: [5]

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Table 10-455. DISPC_GLOBAL_BUFFER

Address Offset	0x0000 0800		
Physical Address	0x4804 1800 0x5800 1800	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the DMA buffers allocations to the pipeline (graphics, video1, video2, video3 and write-back). Both TOP and BOTTOM must be allocated to the same pipeline.		
Type	RW		

31 30	29 28 27	26 25 24	23 22 21	20 19 18	17 16	15 14 13 12	11 10 9	8	7 6	5 4 3	2 1 0
RESERVED	WB_BOTTOM_BUFFER	WB_TOP_BUFFER	VID3_BOTTOM_BUFFER	VID3_TOP_BUFFER	VID2_BOTTOM_BUFFER	VID2_TOP_BUFFER	VID1_BOTTOM_BUFFER	VID1_TOP_BUFFER	GFX_BOTTOM_BUFFER	GFX_TOP_BUFFER	

Bits	Field Name	Description	Type	Reset
31:30	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0
29:27	WB_BOTTOM_ BUFFER	Write-back DMA BOTTOM buffer (half of the full DMA buffer) allocation to one of the pipelines. By default to write-back pipeline. 0x0: DMA buffer allocated to the graphics pipeline. 0x1: DMA buffer allocated to the video1 pipeline. 0x2: DMA buffer allocated to the vdieo2 pipeline. 0x3: DMA buffer allocated to the vdieo3 pipeline. 0x4: DMA buffer allocated to the write-back pipeline.	RW	0x4
26:24	WB_TOP_ BUFFER	Write-back DMA TOP buffer (half of the full DMA buffer) allocation to one of the pipelines. By default to write-back pipeline. 0x0: DMA buffer allocated to the graphics pipeline. 0x1: DMA buffer allocated to the video1 pipeline. 0x2: DMA buffer allocated to the vdieo2 pipeline. 0x3: DMA buffer allocated to the vdieo3 pipeline. 0x4: DMA buffer allocated to the write-back pipeline.	RW	0x4
23:21	VID3_BOTTOM_ BUFFER	Video3 DMA BOTTOM buffer (half of the full DMA buffer) allocation to one of the pipelines. By default to video3 pipeline. 0x0: DMA buffer allocated to the graphics pipeline. 0x1: DMA buffer allocated to the video1 pipeline. 0x2: DMA buffer allocated to the vdieo2 pipeline. 0x3: DMA buffer allocated to the vdieo3 pipeline. 0x4: DMA buffer allocated to the write-back pipeline.	RW	0x3
20:18	VID3_TOP_ BUFFER	Video3 DMA TOP buffer (half of the full DMA buffer) allocation to one of the pipelines. By default to video3 pipeline. 0x0: DMA buffer allocated to the graphics pipeline. 0x1: DMA buffer allocated to the video1 pipeline. 0x2: DMA buffer allocated to the vdieo2 pipeline. 0x3: DMA buffer allocated to the vdieo3 pipeline. 0x4: DMA buffer allocated to the write-back pipeline.	RW	0x3

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Bits	Field Name	Description	Type	Reset
17:15	VID2_BOTTOM_ BUFFER	Video2 DMA BOTTOM buffer (half of the full DMA buffer) allocation to one of the pipelines. By default to video2 pipeline. 0x0: DMA buffer allocated to the graphics pipeline. 0x1: DMA buffer allocated to the video1 pipeline. 0x2: DMA buffer allocated to the vdieo2 pipeline. 0x3: DMA buffer allocated to the vdieo3 pipeline. 0x4: DMA buffer allocated to the write-back pipeline.	RW	0x2
14:12	VID2_TOP_ BUFFER	Video2 DMA TOP buffer (half of the full DMA buffer) allocation to one of the pipelines. By default to video2 pipeline. 0x0: DMA buffer allocated to the graphics pipeline. 0x1: DMA buffer allocated to the video1 pipeline. 0x2: DMA buffer allocated to the vdieo2 pipeline. 0x3: DMA buffer allocated to the vdieo3 pipeline. 0x4: DMA buffer allocated to the write-back pipeline.	RW	0x2
11:9	VID1_BOTTOM_ BUFFER	Video1 DMA BOTTOM buffer (half of the full DMA buffer) allocation to one of the pipelines. By default to video1 pipeline. 0x0: DMA buffer allocated to the graphics pipeline. 0x1: DMA buffer allocated to the video1 pipeline. 0x2: DMA buffer allocated to the vdieo2 pipeline. 0x3: DMA buffer allocated to the vdieo3 pipeline. 0x4: DMA buffer allocated to the write-back pipeline.	RW	0x1
8:6	VID1_TOP_ BUFFER	Video1 DMA TOP buffer (half of the full DMA buffer) allocation to one of the pipelines. By default to video 1 pipeline. 0x0: DMA buffer allocated to the graphics pipeline. 0x1: DMA buffer allocated to the video1 pipeline. 0x2: DMA buffer allocated to the vdieo2 pipeline. 0x3: DMA buffer allocated to the vdieo3 pipeline. 0x4: DMA buffer allocated to the write-back pipeline.	RW	0x1
5:3	GFX_BOTTOM_ BUFFER	Graphics DMA BOTTOM buffer (half of the full DMA buffer) allocation to one of the pipelines. By default to graphics pipeline. 0x0: DMA buffer allocated to the graphics pipeline. 0x1: DMA buffer allocated to the video1 pipeline. 0x2: DMA buffer allocated to the vdieo2 pipeline. 0x3: DMA buffer allocated to the vdieo3 pipeline. 0x4: DMA buffer allocated to the write-back pipeline.	RW	0x0
2:0	GFX_TOP_ BUFFER	Graphics DMA TOP buffer (half of the full DMA buffer) allocation to one of the pipelines. By default to graphics pipeline. 0x0: DMA buffer allocated to the graphics pipeline. 0x1: DMA buffer allocated to the video1 pipeline. 0x2: DMA buffer allocated to the vdieo2 pipeline. 0x3: DMA buffer allocated to the vdieo3 pipeline. 0x4: DMA buffer allocated to the write-back pipeline.	RW	0x0

Table 10-456. Register Call Summary for Register DISPC_GLOBAL_BUFFER

Display Controller

- DMA Engine: [0]
- Shadow Registers: [1]
- Display Controller Register Summary: [2]
- Display Controller Register Description: [3]

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Table 10-457. DISPC_DIVISOR

Address Offset	0x0000 0804		
Physical Address	0x4804 1804 0x5800 1804	**Instance**	DISPC_PER_L4 DISPC_L3
Description	The register configures the divisor value for generating the core functional clock. There is a backward compatibility mode enabled by default in order to use DISPC_DIVISOR1.LCD value instead of DISPC_DIVISOR.LCD bit field for generating the core functional clock.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								LCD								RESERVED															ENABLE

Bits	Field Name	Description	Type	Reset
31:24	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
23:16	LCD	Display Controller Logic Clock Divisor Value (from 1 to 255) to specify the frequency of the Display Controller logic clock based on the function clock. The value 0 is invalid.	RW	0x4
15:1	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0000
0	ENABLE	When the bit field is set to 1, the bit field LCD is used to generated the core functional clock from the input clock. When the bit field is set to 0, the value DISPC_DIVISOR1.LCD is used instead. 0x0: DISPC_DIVISOR1.LCD bit field is used 0x1: DISPC_DIVISOR.LCD bit field is used	RW	0

Table 10-458. Register Call Summary for Register DISPC_DIVISOR

Display Controller

- Clock Configuration: [0] [1] [2] [3]
- Timing Generator and Panel Settings: [4] [5]
- Shadow Registers: [6]
- Display Controller Register Summary: [7]
- Display Controller Register Description: [8] [9]

Table 10-459. DISPC_WB_ATTRIBUTES2

Address Offset	0x0000 0810
Physical Address	0x4804 1810 0x5800 1810
Description	The register set the counter to control the delay to flush the WB pipe after the end of the frame in capture mode. Shadow register, updated on VFP start period of primary LCD or VFP start period of secondary LCD or EVSYNC depending on which overlay output is selected as an input to the WB pipeline
Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								WBDELAYCOUNT							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED		R	0x000000
7:0	WBDELAYCOUNT	Delays the WB pipe flush after the end of the frame.delay = n x (1/F_clk) n = 0:255	RW	0x00

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Table 10-460. Register Call Summary for Register DISPC_WB_ATTRIBUTES2

Display Controller

- DMA Buffers: [0] [1] [2]
- Shadow Registers: [3] [4] [5] [6]
- Display Controller Register Summary: [7]

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10.3 MIPI Display Serial Interface

This section describes the MIPI® display serial interface (DSI) module for the device.

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10.3.1 MIPI DSI Overview

The display serial interface (DSI) module connects to a DSI display module directly or through an external DSI bridge. The DSI module is connected to DISPC and L3/L4_PER interconnects

Figure 10-95 is a block diagram of the DSI module.

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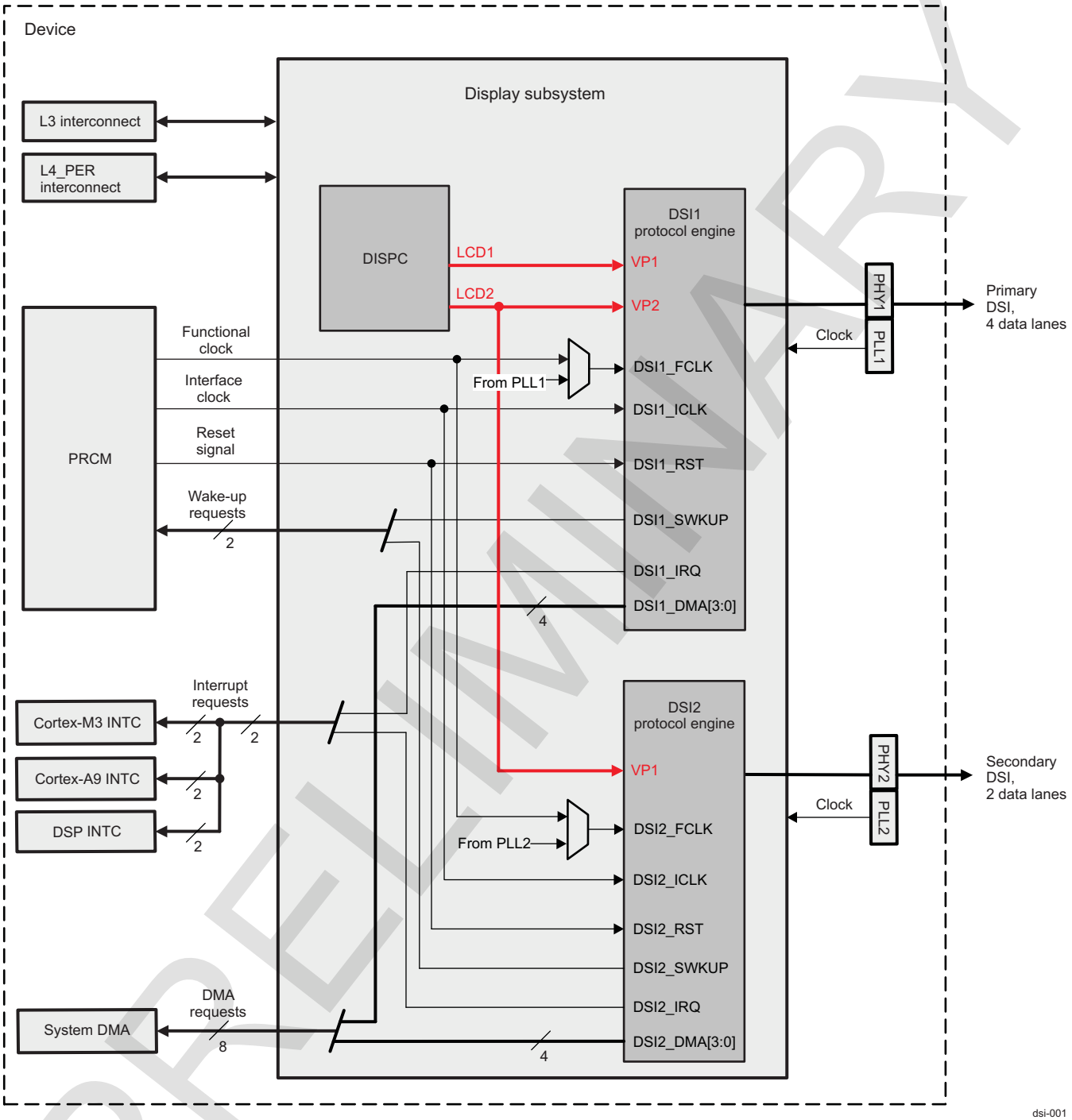
Figure 10-95. DSI Overview



There are two DSI modules in the display subsystem (DSS) that provide the following main features:

- DSI 1 (primary)
  - Supports MIPI-DSI (up to four data lanes + one clock lane)
  - Supports video mode and command mode
  - Support multiple displays (one video mode and one command mode). In command mode, pixel data are provided from the level 3 (L3) interface or from one of the overlay manager outputs.
  - Bidirectional data link support for command mode (only one data lane is used in reverse direction)

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  - RGB16, RGB18 nonpacked, and RGB24 formats supported for command mode
  - RGB16, RGB18 packed and nonpacked, and RGB24 formats supported for video mode
  - Burst support for the video mode
  - Supports up to four data-configurable lanes, in addition to the clock signaling
  - Maximum data rate of 824 Mbps per data pair for four-data lane configuration, and 900 Mbps for up to three-data lane configuration
  - Data splitter for 2-data, 3-data and 4-data lane configurations
  - Data interleaving support for one synchronous stream (video mode) from the DISPC and up to three asynchronous streams (command mode) from the interconnect concurrently, or up to four asynchronous streams (command mode) from the interconnect
  - Transfer of pixels and data received on the video port or L3 interconnect to the display through DSI DSI_PHY
  - Serial configuration port (SCP) for the DSI_PHY complex input/output (I/O) and DSI phase-locked loop (PLL)
  - Connection to the DSI_PHY complex I/O through PPI
  - Error-correction code (ECC) and checksum generation
  - MIPI DCS support
- DSI 2 (secondary)
  - Supports MIPI-DSI (up to two data lanes + one clock lane)
  - Supports video mode and command mode
  - Support multiple displays (one video mode and one command mode). In command mode, pixel data are provided from the L3 interface or from one of the overlay manager outputs.
  - Bidirectional data link support for command mode (only one data lane is used in reverse direction)
  - RGB16, RGB18 nonpacked, and RGB24 formats supported for command mode
  - RGB16, RGB18 packed and nonpacked, and RGB24 formats supported for video mode
  - Burst support for the video mode
  - Supports one data-configurable lane, in addition to the clock signaling
  - Maximum data rate of 900 Mbps per data pair
  - Data splitter for 2-data lane configuration
  - Data interleaving support for one synchronous stream (video mode) from the DISPC and up to three asynchronous streams (command mode) from the interconnect concurrently, or up to four asynchronous streams (command mode) from the interconnect
  - Transfer pixels and data received on the video port or Interface interconnect to the display through DSI DSI_PHY
  - Serial configuration port (SCP) for the DSI_PHY complex I/O and DSI PLL
  - Connection to the DSI_PHY complex I/O through the physical layer (PHY) protocol interface (PPI)
  - ECC and checksum generation
  - MIPI DCS support

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10.3.2 DSI Environment

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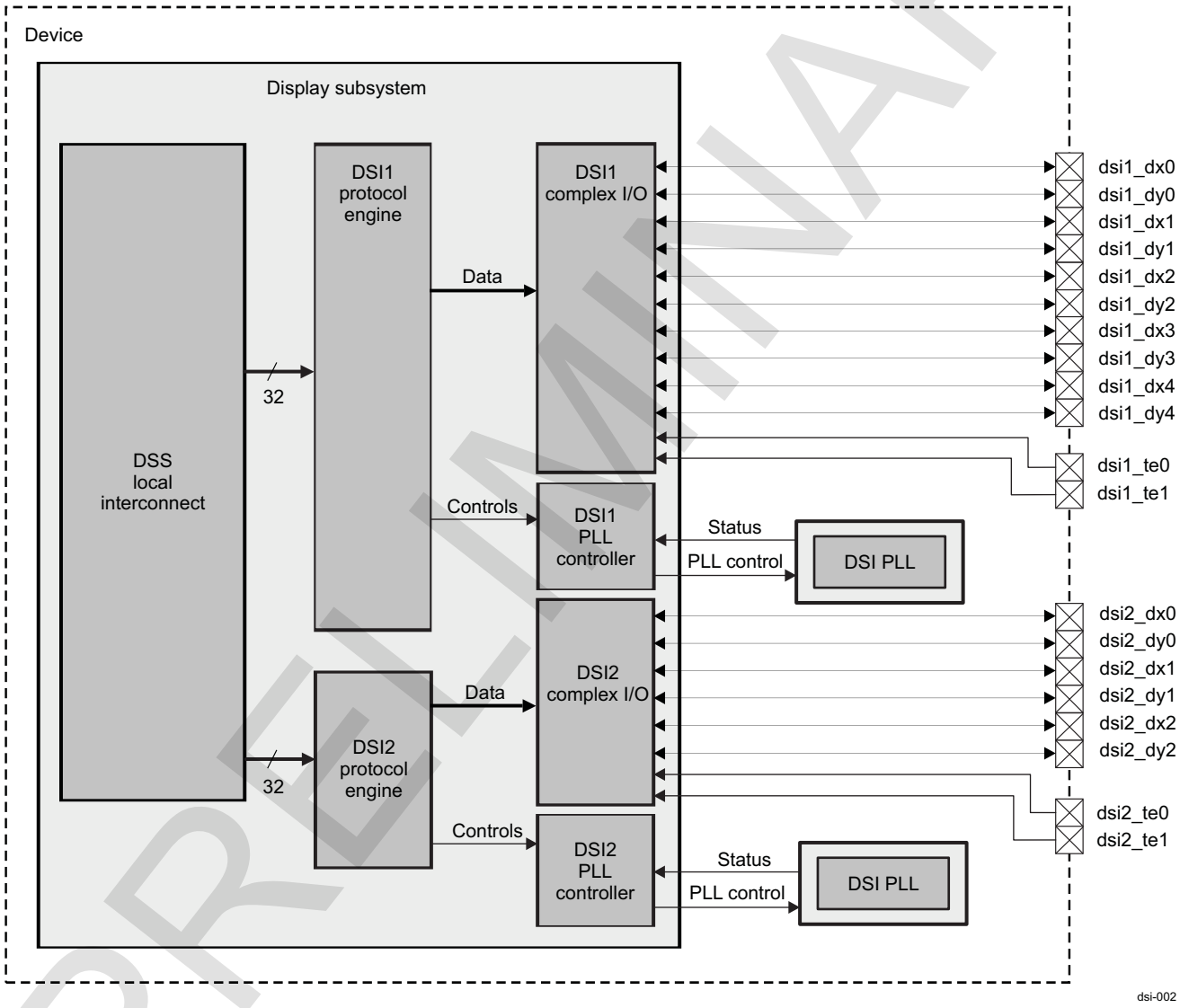
This section describes the DSI application fields from an environment point of view (external connections). It describes the DSI connectivity options, lists all possible interfaces, and describes the protocol and data format used in each case.

Figure 10-96 is a block diagram of the DSI environment.

Figure 10-96. DSI Environment



The DSI is a bidirectional differential serial interface with data/clock for the PHY (configured in unidirectional link in case the display module is only unidirectional). The maximum capacity of a DSI data transfer is 824 Mbps for four data lanes. The speed of the link can be configured by software only when the DSI_PHY is in STOP state or ULTRALOW-POWER state (ULPS).

Figure 10-97 shows the high-level data flow of the DSI transmitter/receiver.

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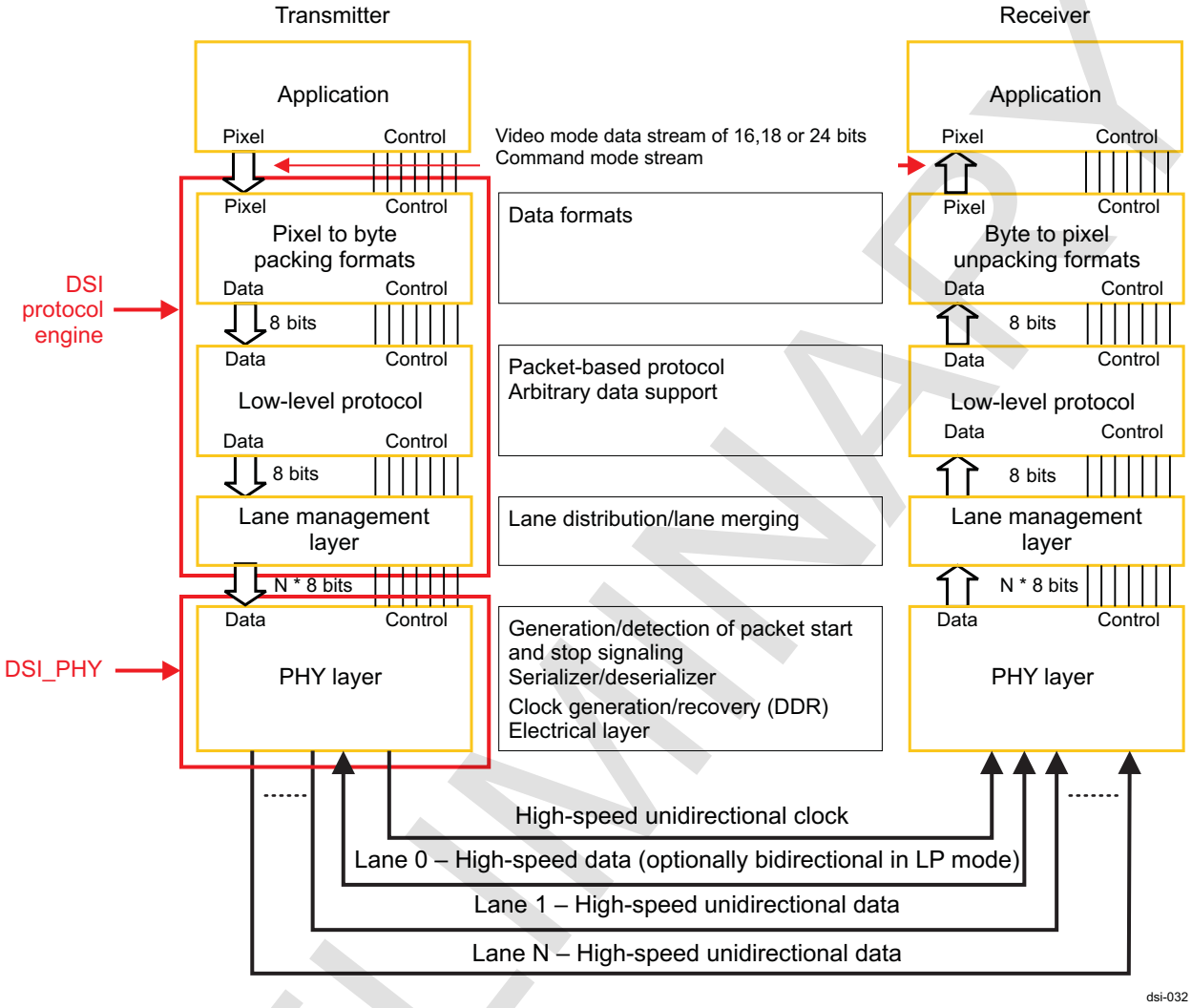
Figure 10-97. DSI Transmitter/Receiver Data Flow



10.3.2.1 DSI PHY

Table 10-461 lists the DSI1 I/Os.

Table 10-461. I/O Description of DSI1

Signal Name		I/O [1]	Description	Value at Reset
dsi1_dx0 dsi1_dy0	line 1	I/O	Serial data/clock lane	N/A
dsi1_dx1 dsi1_dy1	line 2	I/O	Serial data/clock lane	N/A
dsi1_dx2 dsi1_dy2	line 3	I/O	Serial data/clock lane	N/A
dsi1_dx3 dsi1_dy3	line 4	I/O	Serial data/clock lane	N/A
dsi1_dx4 dsi1_dy4	line 5	I/O	Serial data/clock lane	N/A
dsi1_te0	te0	I	DSI1 tearing effect (TE) input 0	N/A

(1) I = Input; O = Output

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Table 10-461. I/O Description of DSI1 (continued)

Signal Name		I/O [1]	Description	Value at Reset
dsi1_te1	te1	I	DSI1 TE input 1	N/A

NOTE: Each serial line (line 1 through line 5) can be used as a clock lane or a data lane. All polarities are supported. The MIPI DSI 1.01 protocol requires at least one clock line and one data lane.

Table 10-462 lists the DS2 I/Os.

Table 10-462. I/O Description of DSI2

Signal Name		I/O [1]	Description	Value at Reset
dsi2_dx0 dsi2_dy0	line 1	I/O	Serial data/clock lane	N/A
dsi2_dx1 dsi2_dy1	line 2	I/O	Serial data/clock lane	N/A
dsi2_dx2 dsi2_dy2	line 3	I/O	Serial data/clock lane	N/A
dsi2_te0	te0	I	DSI2 TE input 0	N/A
dsi2_te1	te1	I	DSI2 TE input 1	N/A

(1) I = Input; O = Output

NOTE: Each serial line (line 1 through line 3) can be used as a clock lane or a data lane. All polarities are supported. The MIPI DSI 1.01 protocol requires at least one clock line and one data lane.

Lanes support four operating modes:

- HS mode: High-speed transmit mode
- LP mode: Low-power transmit mode (also called low-power state [LPS])
- ULPS: ULTRALOW-POWER state used between two transmissions
- Off mode: Lane is off.

NOTE: The CONTROL_DSIPHY register in the control module of the device provides the following control over the DSI lanes:

- Enable and disable each lane (the DSI2_LANEENABLE[31:29] and DSI1_LANEENABLE[28:24] bit fields).
- Pulldown enable and disable on each lane (the DSI2_PIPD[23:19] and DSI1_PIPD[18:14] bit fields)

For more information, see Section 18.6.6, *SYSCTRL_PADCONF_CORE Register Summary*, in Chapter 18, *Control Module*.

10.3.2.1.1 Data/Clock Configuration

Data-clock signaling consists of one to four data pairs and one clock pair. The minimum configuration is one data pair and one clock pair.

- The data signal carries the bit serial data. The DSI transmitter in the host sends the data in-quadrature with the dual data rate (DDR) clock in HS mode; otherwise, the clock is extracted from the received data in LS mode. The data is transmitted byte-wise LSB first.
- The clock signal carries the DDR clock signal in HS transmission.
- Software users must configure the order of the data lanes to indicate the byte order while splitting the

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byte stream for each DSI_PHY into bytes.

Table 10-463 lists some of the DSI lane configurations.

NOTE: All combinations for the order of the clock and data lanes are supported but not explicitly described in Table 10-463.

Table 10-463. DSI Lane Configuration

DSI_PHY Lane Configuration	Data/Clock Lane Position					Description
	1	2	3	4	5	
Mode CLK + DATA1						Single data lane
	CLK	DATA1				
	DATA1	CLK				
Mode CLK + DATA1 + DATA2						Two data lanes
	CLK	DATA1	DATA2			
	CLK	DATA2	DATA1			
	DATA1	CLK	DATA2			
	DATA2	CLK	DATA1			
	DATA1	DATA2	CLK			
	DATA2	DATA1	CLK			
Mode CLK + DATA1 + DATA2 + DATA3						Three data lanes
	CLK	DATA1	DATA2	DATA3		
	CLK	DATA3	DATA2	DATA1		
	DATA1	CLK	DATA2	DATA3		
	DATA1	CLK	DATA3	DATA2		
	DATA2	CLK	DATA1	DATA3		
	DATA2	CLK	DATA3	DATA1		
	DATA3	CLK	DATA1	DATA2		
	DATA3	CLK	DATA2	DATA1		
	DATA3	DATA1	CLK	DATA2		
	DATA3	DATA2	CLK	DATA1		
	DATA3	DATA2	CLK	DATA1		
	DATA1	DATA2	CLK	DATA3		
	DATA2	DATA3	CLK	DATA1		
	DATA1	DATA3	CLK	DATA2		
	DATA1	DATA2	DATA3	CLK		
	DATA3	DATA2	DATA1	CLK		
Mode CLK + DATA1 + DATA2 + DATA3 + DATA4						Four data lanes
	CLK	DATA1	DATA2	DATA3	DATA4	
	DATA4	DATA3	DATA2	DATA1	CLK	
	DATA3	DATA1	CLK	DATA2	DATA4	
	DATA4	DATA2	CLK	DATA1	DATA3	
	DATA2	DATA1	CLK	DATA3	DATA4	
	DATA4	DATA3	CLK	DATA1	DATA2	
	DATA3	DATA4	CLK	DATA2	DATA1	
	DATA1	DATA2	CLK	DATA4	DATA3	
	DATA1	DATA4	CLK	DATA3	DATA2	

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Table 10-463. DSI Lane Configuration (continued)

DSI_PHY Lane Configuration	Data/Clock Lane Position					Description
	1	2	3	4	5	
	DATA1	DATA3	CLK	DATA4	DATA2	

NOTE:

- The byte on Dn is sent before the byte on Dn + 1; all the combinations of data and clock are supported through programming of the DSI_COMPLEXIO_CFG1 register. The CLOCK_POSITION and CLOCK_POL bit fields configure which lane transmits the clock and define its polarity. Eight bit fields (DATA1_POSITION and DATA1_POL, through DATA4_POSITION and DATA4_POL) configure the data lanes and their polarity. The DATA2_POSITION through DATA4_POSITION bit fields can be set to 0; in this case, only the data lane defined in the DATA1_POSITION bit field is used, and data is transmitted on only one clock lane and one data lane.
- Only DATA1 is bidirectional in command mode. The low-power received information is always sent by the display panel using DATA1. Because any lane of the DSI complex I/O can be configured as data lane DATA1, all lanes of the complex I/O are bidirectional.

10.3.2.1.2 ULPS

Each lane can be put in ULPS by software configuration. The ULPS mode requires the following conditions:

- The lane must be in ULP state.
- For data lanes, no data must be pending in the DSI module.
- For data lane 1, no bus turnaround (BTA) should have been sent. The DSI module must have control of the bus.

For more information on ULPS configuration, see Section 10.3.4.4.16, *Ultralow-Power State Configuration*.

10.3.2.2 DSI Protocol Layer

Low-level protocol (LLP) is a byte-oriented protocol. It supports short and long packet formats. The DSI protocol layer defines how the display data is transported onto the PHY. Packets can be sent using HS mode or low-speed (LS) mode. LLP is selected through DSI registers. The features of the DSI protocol layer are:

- Transport of arbitrary data (payload independent)
- 8-bit word size
- Support for up to four interleaved VCs on the same link
- Special packets for frame start, frame end, line start, and line end information
- Descriptor for the type, pixel depth, and format of application-specific payload data
- ECC for 1-bit or 2-bit error detection in the header
- 16-bit checksum code for error detection

Figure 10-98 shows the protocol layer with short and long packets.

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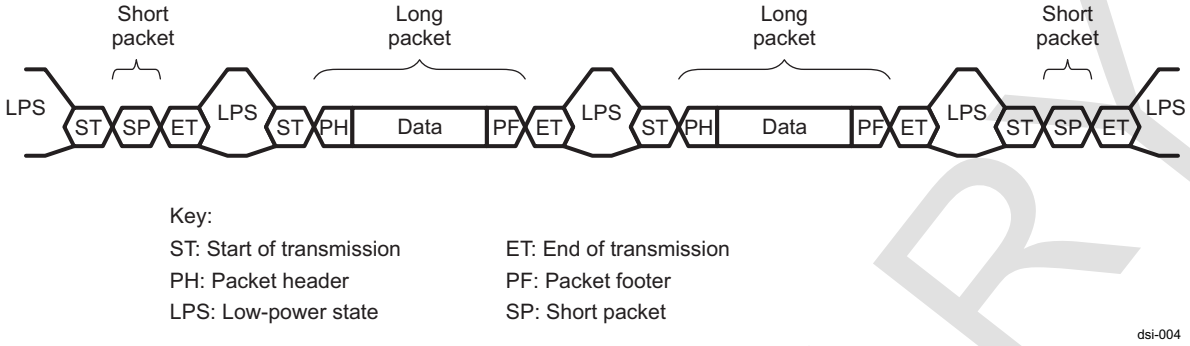
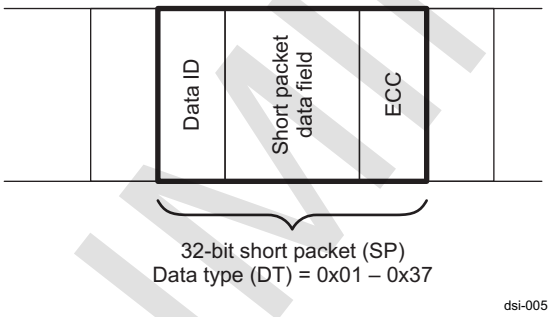
Figure 10-98. Protocol Layer With Short and Long Packets



10.3.2.2.1 Short Packet

Figure 10-99 shows the structure of the short packet. A short packet must contain an 8-bit data ID followed by two command or data bytes and an 8-bit ECC. No packet footer (PF) should be present. Short packets must be 4 bytes long. The ECC byte allows correction of single-bit errors and detection of 2-bit errors in the short packet.

Figure 10-99. Short Packet Structure



NOTE: The short packets can be sent in LP mode or HS mode.

The DSI_VC_SHORT_PACKET_HEADER_i register is used to send only short packets (ECC can be calculated by hardware or by software users for debug purposes). This register is not used for video mode data because the short packets are generated by hardware based on the following events:

- Synchronization events received on the video port (assertion/deassertion of the HSYNC and VSYNC input signals)
- DSI_CTRL[18] VP_HSYNC_END
- DSI_CTRL[17] VP_HSYNC_START
- DSI_CTRL[16] VP_VSYNC_END
- DSI_CTRL[15] VP_VSYNC_START
- DSI_CTRL[11] VP_VSYNC_POL
- DSI_CTRL[10] VP_HSYNC_POL
- DSI_VC_CTRL_i[1] SOURCE

10.3.2.2.2 Long Packet

Figure 10-100 shows the structure of the long packet. A long packet must consist of three elements: 32-bit packet header (PH), application-specific data payload with a variable number of bytes, and 16-bit PF.

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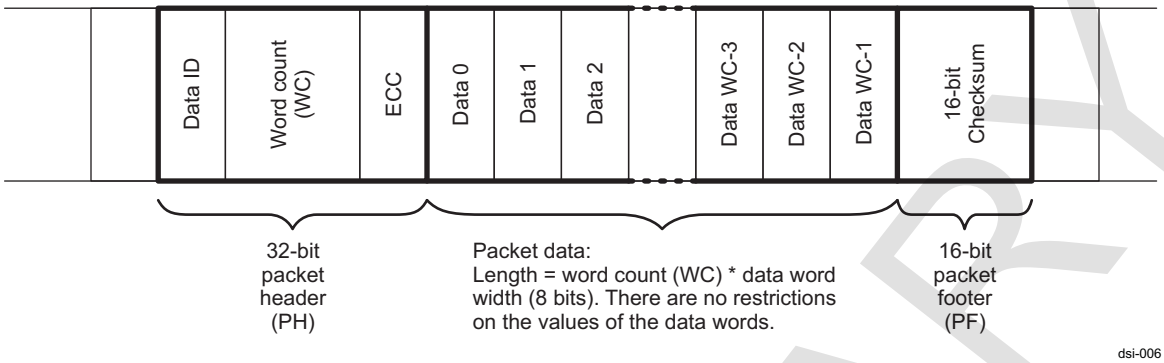
Figure 10-100. Long Packet Structure



The PH is further composed as follows:

- 8-bit data identifier: The data identifier defines the VC for the data and the DT for the application-specific payload data.
- 16-bit word count: The word count defines the number of bytes in the data payload between the end of the PH and the start of the PF. The PH and the PF must not be included in the word count.
- 8-bit ECC: The ECC byte allows single-bit errors to be corrected and 2-bit errors to be detected in the PH. This includes the data identifier and the word count fields.

After the end of the PH, the receiver reads the next word count × bytes of the data payload. There are no limitations on the value of a data word within the data payload block (that is, no embedded codes are used). Once the receiver has read the data payload, it reads the checksum in the PF. The host processor must always calculate and transmit a checksum in the PF. Peripherals are not required to calculate a checksum. In the special case of a 0-byte data payload, if the payload length is 0, the checksum calculation results in (0xFFFF). If the checksum is not calculated, the PF must consist of 2 bytes of 0s (0x0000). In the generic case, the length of the data payload must be a multiple of bytes. In addition, each data format can impose additional restrictions on the length of the payload data (that is, a multiple of 4 bytes). Each byte is transmitted LSB first. Payload data can be transmitted in any byte order, restricted only by data format requirements. Multibyte elements, such as word count and checksum, must be transmitted least-significant byte (LSByte) first.

NOTE: Long packets can be sent in LP or HS mode.

The DSI_VC_LONG_PACKET_HEADER_i register provides headers for long packets (ECC is always calculated by hardware). The register is used for video and command modes.

If video mode is enabled for a virtual channel, it is not possible to transfer data concurrently (interleaved in a frame) using long packets received on the video and L3 interconnect ports because the DSI_VC_LONG_PACKET_HEADER_i register is used by the video mode. The register can be unprogrammed by the user to send long packets received on the L3 interconnect port only when there is no expected data on the video port. Software must program the register correctly to send sequentially long packets in video and command modes.

The word count (WC) defined in the DSI_VC_LONG_PACKET_HEADER_i register for the VC associated with the video port indicates the number of bytes to receive (one line or two lines can be used, depending on the WC and the size of the line buffer). The total size defined in the WC of the header register cannot exceed the size of the line buffer multiplied by the number of buffer lines.

The DSI_VC_LONG_PACKET_PAYLOAD_i register is used to provide payload data for long packets (checksum is calculated by hardware when DSI_VC_CTRL_i[7] CS_TX_EN is set to 1; otherwise, the value is 0x00). The register is not used in video mode because payload data are provided by the video port.

Software must ensure that the following sequence for write accesses to the header and payload registers (DSI_VC_LONG_PACKET_HEADER_i and DSI_VC_LONG_PACKET_PAYLOAD_i, respectively) is followed:

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- A long PH value with WC = 0 written in the DSI_VC_LONG_PACKET_HEADER_i register can be followed by any access.
- A long PH value with WC 0 written in the DSI_VC_LONG_PACKET_HEADER_i register must be followed by one or more writes to the DSI_VC_LONG_PACKET_PAYLOAD_i register defined by the WC value before writing again to the same DSI_VC_LONG_PACKET_HEADER_i register.

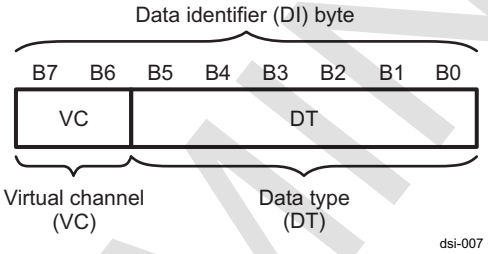
CAUTION

If this sequence is not followed, no error is generated. Access to other DSI registers during this sequence is allowed.

10.3.2.2.3 Data Identifier

The data identifier byte contains the values for the virtual channel ID and data type, as shown in Figure 10-101. The virtual channel ID is contained in the 2 MSBs of the data identifier byte and identify the data as directed to one of four virtual channels. The value of the data type is contained in the 6 LSBs of the data identifier byte.

Figure 10-101. Data Identifier Structure

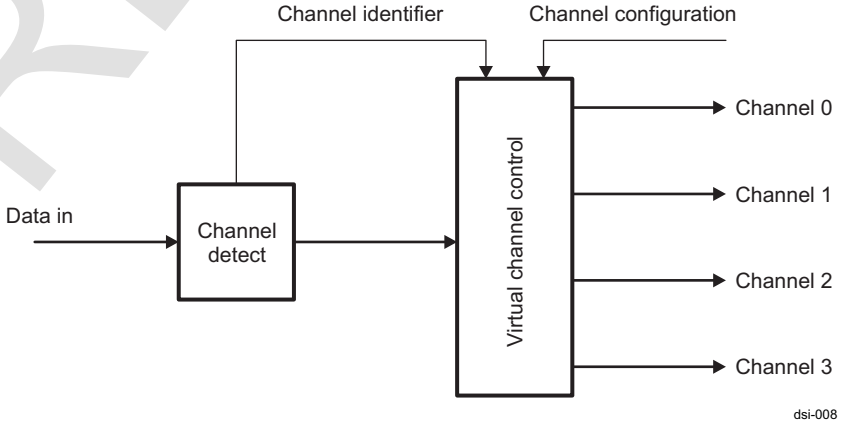


10.3.2.2.3.1 VC ID – VC Field, DI[7:6]

The host can service up to four peripherals with tagged commands or blocks of data using the VC ID field of the header for packets targeted at different peripherals. The VC ID enables one serial stream to service two or more virtual peripherals by multiplexing packets onto a common transmission channel. Each packet sent in a single transmission has its own VC assignment and can be directed to different peripherals. The VC ID is defined in the DSI_VC_SHORT_PACKET_HEADER_i and DSI_VC_LONG_PACKET_HEADER_i registers for short and long packets, respectively. It will not be modified by hardware. There is one set of registers for each VC. Each set of registers defines the characteristics of the traffic between the host and the display associated with the VC.

Figure 10-102 shows the VC controller.

Figure 10-102. VC Controller



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10.3.2.2.3.2 Data Type Field DT[5:0]

The data type field specifies whether the packet is long or short and the packet format. The data type field, and the word count field for long packets, informs the receiver about how many bytes to expect in the rest of the packet. This is necessary because the beginning and end of a packet are not indicated by special packet start/end sync codes. This permits packets to convey arbitrary data, but it also requires the PH to specify the size of the packet.

10.3.2.2.4 Synchronization Codes

Each frame can be identified by two synchronization codes:

- For the start of the vertical synchronization (VSSC) pulse
- For the end of the vertical synchronization (VSEC) pulse

Each line can be identified by two synchronization codes:

- For the start of the horizontal synchronization (HSSC) pulse
- For the end of the horizontal synchronization (HSEC) pulse

The synchronization events are not be required by the display (peripheral): they are optional. Users can program which synchronization events are generated to the display from the timings received from the DISPC in video mode. When data are received on the L3 interconnect port, the synchronization codes are not automatically generated by the protocol engine. They can be provided on the L3 interconnect port by writing to the registers with limited timing control. It is highly recommended to use the video port from the DISPC to receive the synchronization events to automatically generate short synchronization packets to the peripheral.

When the DSI protocol engine detects that the VSYNC signal from the DISPC transitions from inactive to active state, the VSSC short packet replaces the following HSSC corresponding to the following HSYNC synchronization short packet (if the generation is enabled).

When the transition from active to inactive state is detected, the VSEC short packet is generated (if the generation is enabled) replacing the HSEC synchronization packet corresponding to the following HSYNC.

When the DSI protocol engine detects that the HSYNC signal from the DISPC transitions from inactive to active state, the HSSC short packet is generated (if the generation is enabled).

When the transition from active to inactive state is detected, the HSEC short packet is generated (if generation is enabled).

For the first frame, any HSYNC and data received on the video port before the first VSYNC must be ignored. Because the first VSYNC sent to the display is also recognized as an HSYNC for the first line, there is no HSYNC sent for the first line. To send the synchronization codes, the DSI protocol engine uses the short packets. Table 10-464 lists the 6-bit DT synchronization code values.

Table 10-464. Synchronization Codes

Synchronization Code	Value	Comments
Vertical sync start code (VSSC)	0x1	Optional
Vertical sync end code (VSEC)	0x11	Optional
Horizontal sync start code (HSSC)	0x21	Optional
Horizontal sync end code (HSEC)	0x31	Optional

10.3.2.2.5 Blanking

To keep the DSI link in HS state while using video mode, during blanking periods, long blanking packets are sent to the display. The DSI_VM_TIMINGx (where x = 1 to 8) registers define the size of the long blanking packets after:

- Horizontal sync start code (short packet)

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- Horizontal sync end code (short packet)
- Vertical sync start code (short packet)
- Vertical sync end code (short packet)
- Pixels (long packet)

Table 10-465 defines the short packet values for the synchronization packets:

Table 10-465. Sync Short Packet Values

VC ID	Sync Code	Header (First Byte)	Header (Second Byte): Data Field LSB	Header (Third Byte): Data Field MSB	Header (ECC)
0x0	0x1	0x1	0x0	0x0	See Notes following this table.
	0x11	0x11			
	0x21	0x21			
	0x31	0x31			
0x1	0x1	0x41			
	0x11	0x51			
	0x21	0x61			
	0x31	0x91			
0x2	0x1	0x81			
	0x11	0x81			
	0x21	0xA1			
	0x31	0xB1			
0x3	0x1	0xC1			
	0x11	0xD1			
	0x21	0xC1			
	0x31	0xF1			

NOTE:

- If the ECC is enabled by setting the DSI_VC_CTRL_i[8] ECC_TX_EN bit to 1 for the VC in video mode, the ECC value is calculated; otherwise, 0x00 is used for the blanking long packets and sync short packets. If the CRC is enabled by setting the DSI_VC_CTRL_i[7] CS_TX_EN bit to 1 for the VC in video mode, the checksum value is calculated; otherwise, 0x00 is used for the blanking long packets.
- In other cases, when the DSI_VC_CTRL_i[7] CS_TX_EN bit is set to 0, the value 0x00 is always used for the CRC (long packets). When the DSI_VC_CTRL_i[8] ECC_TX_EN bit is set to 0, the value 0x00 is used for the ECC for short and long packets, except when the header is provided by the register, because the ECC field is available in the register. It can be used to generate invalid ECC values when the header is provided by the register.

The DSI link (lanes and clock separately) can be put in ULPS. While using the blanking values formerly defined, the packets (short and long) are considered in HS mode.

Timing parameters VSA, VBP, VFP, HSA, HBP, HFP, VACT, and t_L are defined in the DSI_VM_TIMING1 through DSI_VM_TIMING8 registers. HSA, HBP, HFP, and t_L are defined using the byte clock unit (TXBYTECLKHS - HS transmit byte clock generated by DSI_PHY) and also in low-power clock cycles (TxClkEsc). VSA, VBP, VFP, and VACT are defined by the number of lines. When the HS blanking packets are sent during the blanking periods, the parameters are used to determine the blanking packet payload size (taking into account the 4-byte header and the 2-byte checksum).

The configuration of the DISPC timing generator must be used when the DISPC timings are used to generate DSI HS video mode transfer.

Special care must be taken in the case of the last line of the frame. The LPS transition is required when the link is in HS mode for the whole frame.

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When BTA is sent for the data packets, the following blanking period cannot be used for sending any data from the TX FIFO. When the blanking period starts with one HS packet from one VC, it can be followed only by another HS packet from the same VC, or by a trigger (for example, BTA). When there is no more HS data to send for this VC, the lane is in LPS.

When the blanking period starts with one LP packet from one VC, it can be followed only by another LP packet from the same VC, by another VC, by trigger (BTA, for example), or by extra LP NULL packets. If the trigger is sent, it is not possible to send any more data. When there is no more data from the TX FIFO to send in LP mode or the trigger has been sent, the lane is put into LPS. If the lanes must be kept in HS mode during blanking periods (except for the last blanking period of the frame), the HS blanking packets must be used. If one trigger is sent at the beginning of the blanking period, the rest of the blanking period is in LPS.

Figure 10-103 and Figure 10-104 show a nonburst transfer in DSI video mode with and without VE and HE, respectively. Figure 10-105 shows a burst transfer in DSI video mode without VE and HE.

Figure 10-103. DSI Video Mode: Nonburst Transfer With VE and HE

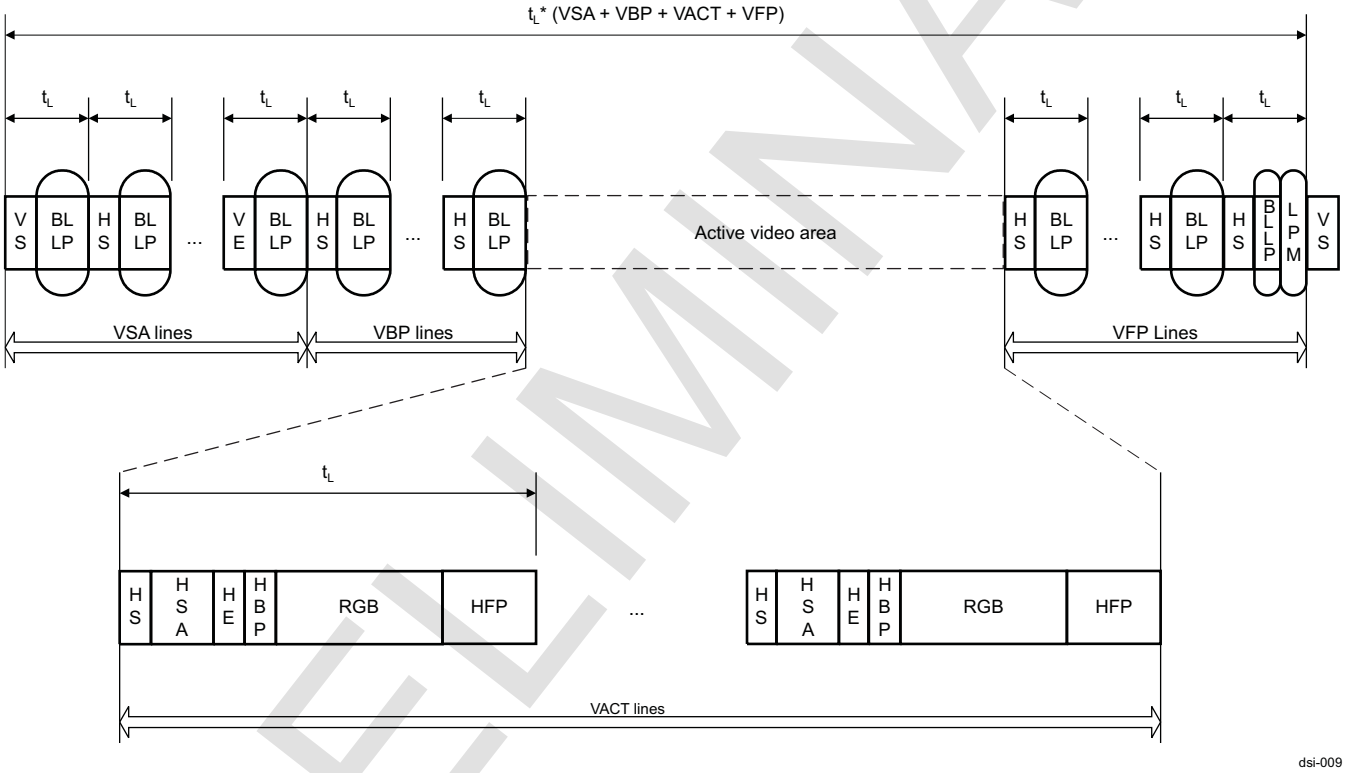

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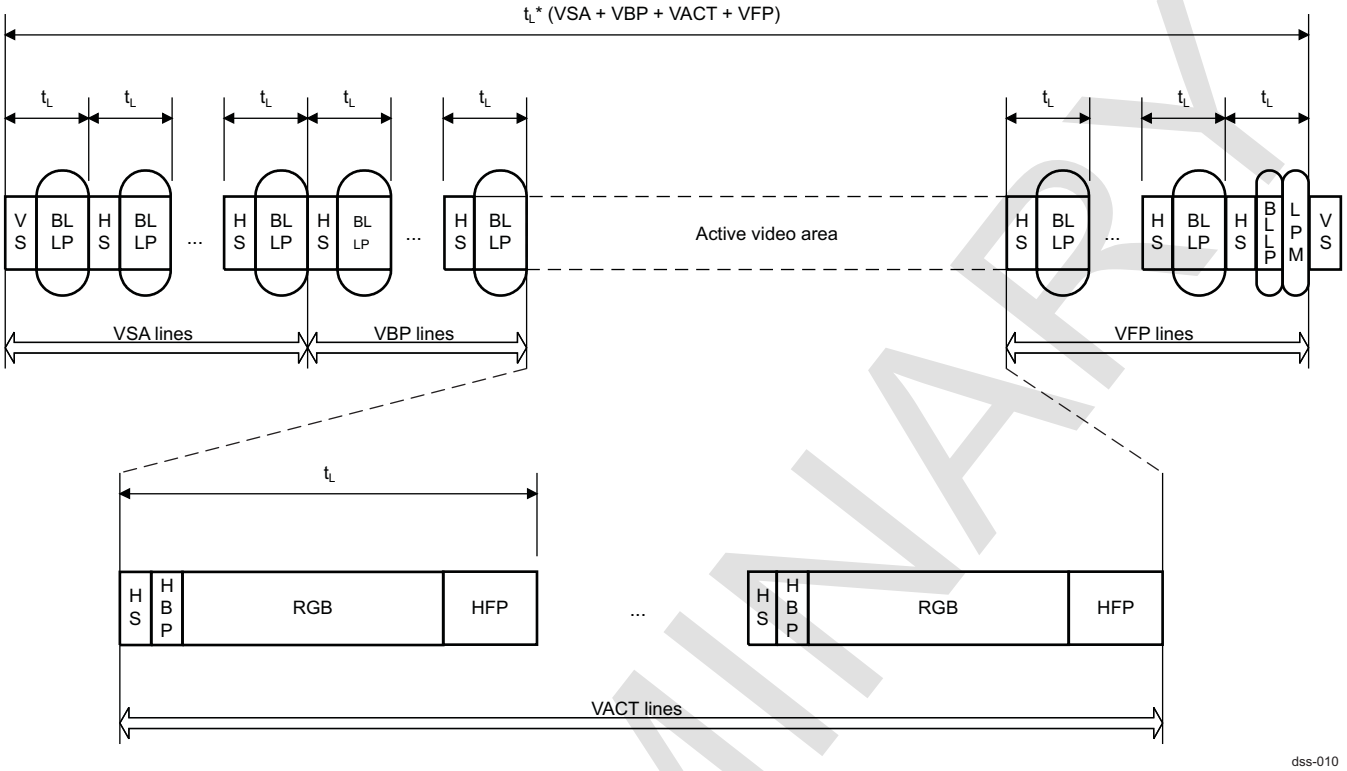
Figure 10-104. DSI Video Mode: Nonburst Transfer Without VE and HE



NOTE: HSA timing is not used and does not have to be programmed when HE short packet is not generated.

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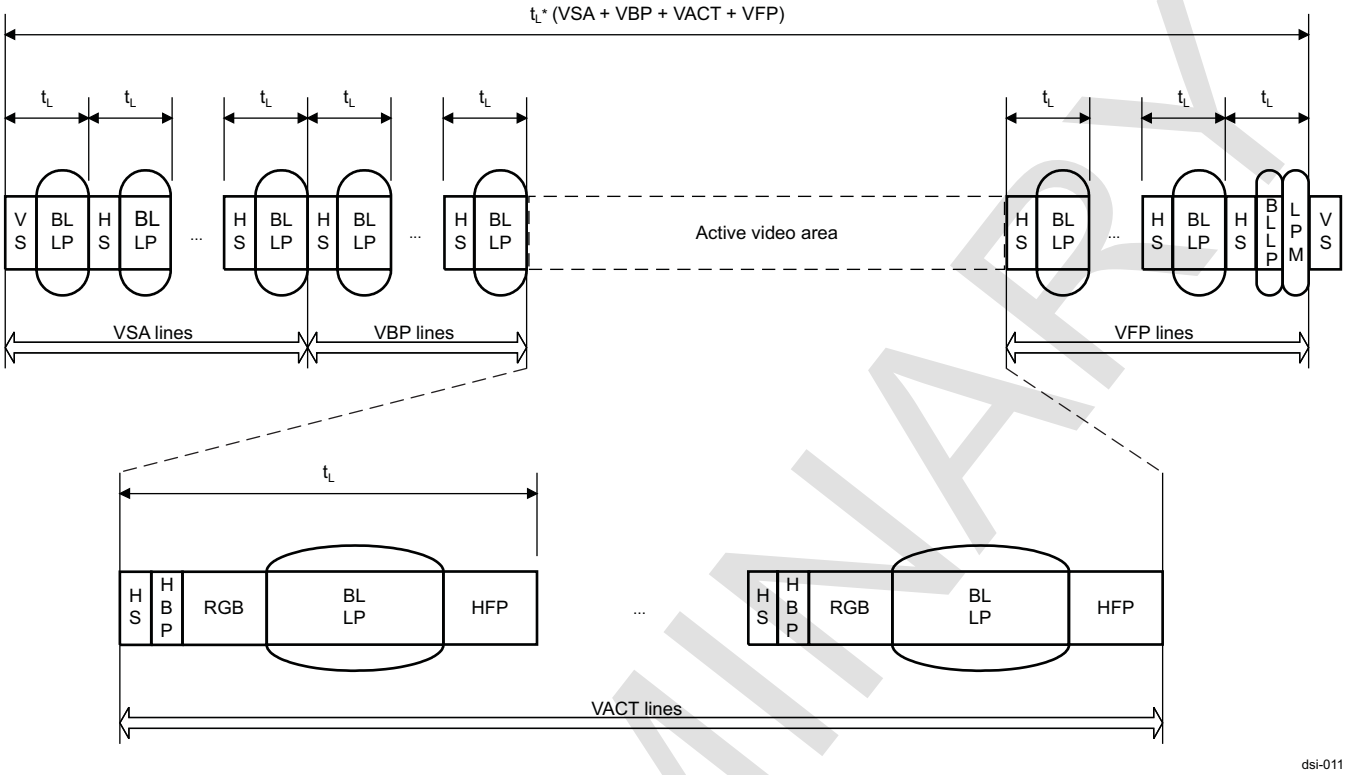
Figure 10-105. DSI Video Mode: Burst Transfer Without VE and HE



NOTE: HSA timing is not used and does not have to be programmed when HE short packet is not generated.

In Figure 10-104 and Figure 10-105, if HSYNC end short packet is not generated (HSA does not exist), HBP must not be 0.

10.3.2.2.6 Frame Structures

NOTE: The figures in this section show only pixel packets and blanking periods; they do not show synchronization packets.

Figure 10-106 shows the DSI general frame structure.

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Figure 10-106. DSI General Frame Structure

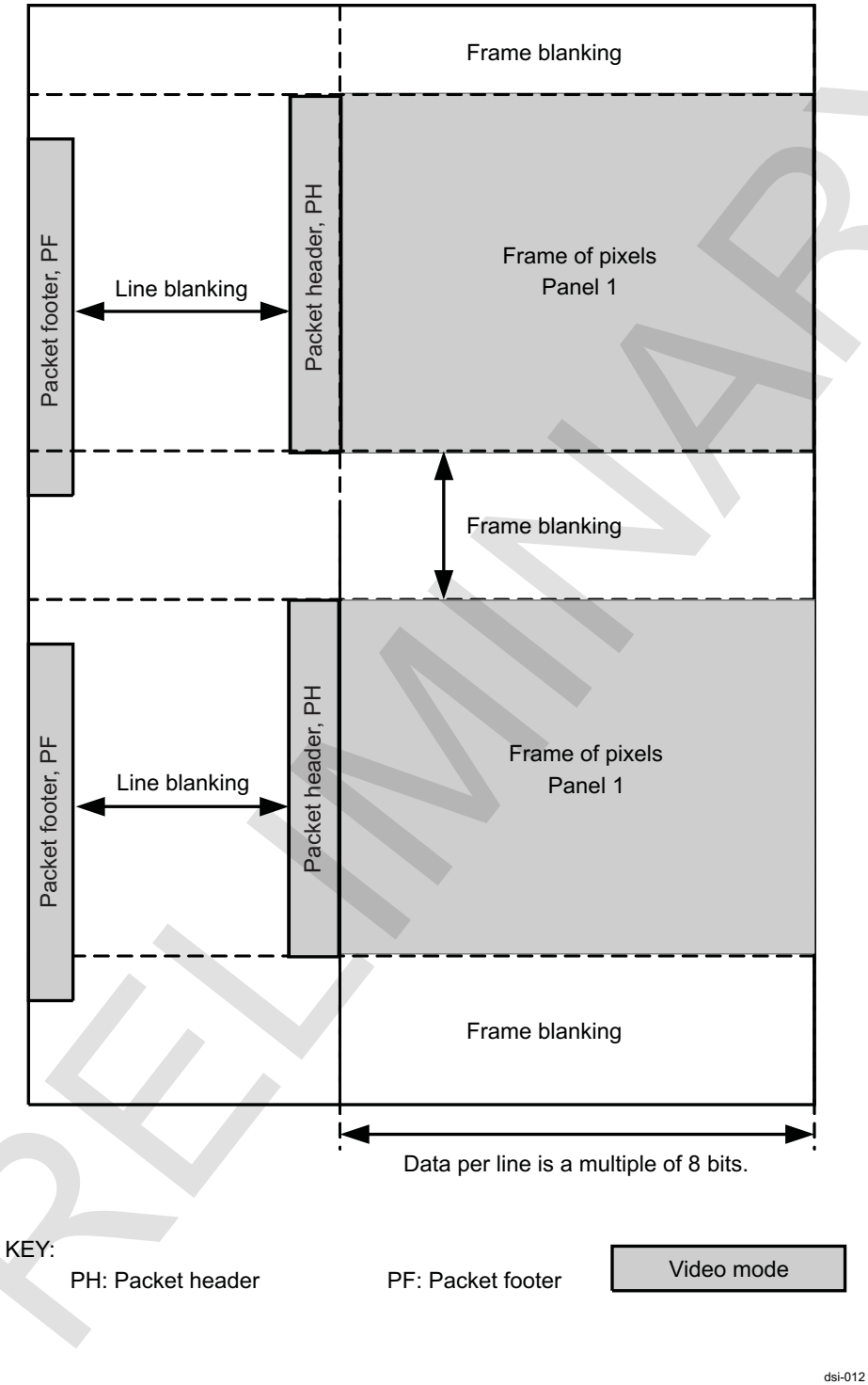

Figure 10-107 shows the general frame structure using burst mode.

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Figure 10-107. DSI General Frame Structure Using Burst Mode

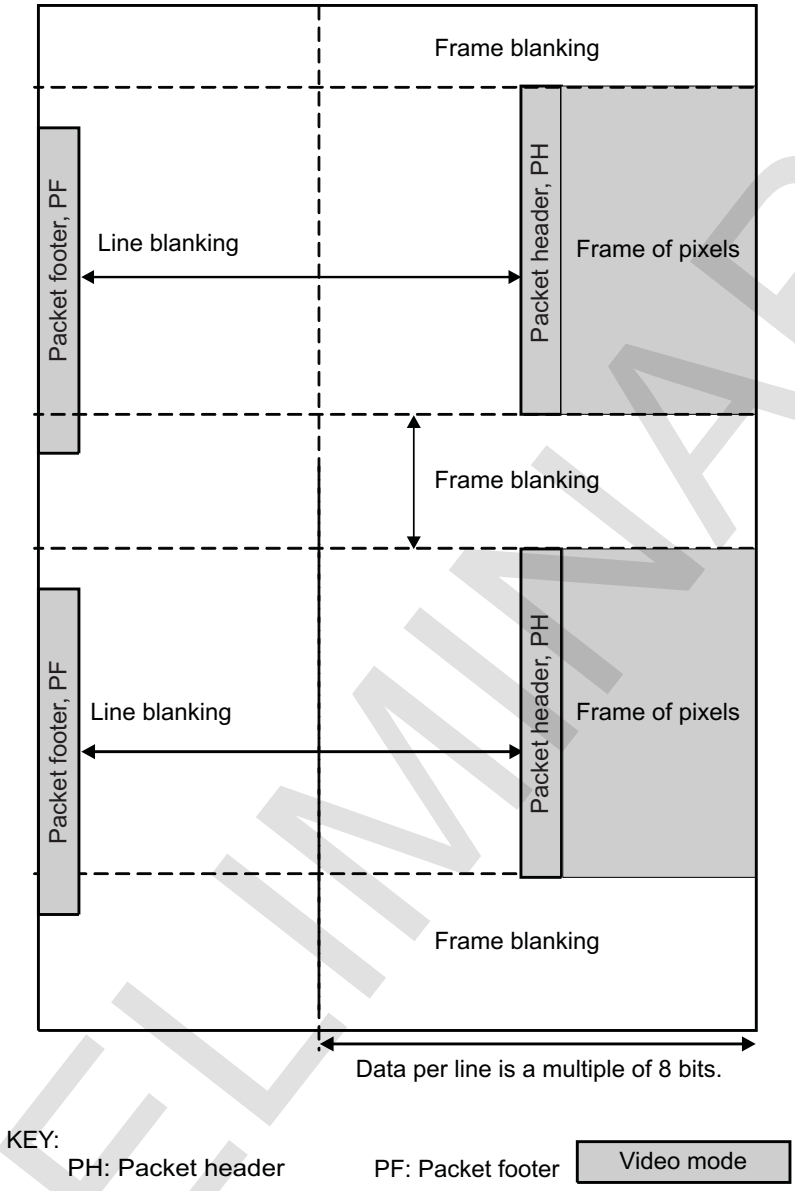

Figure 10-108 shows the general frame structure using burst mode and interleaving.

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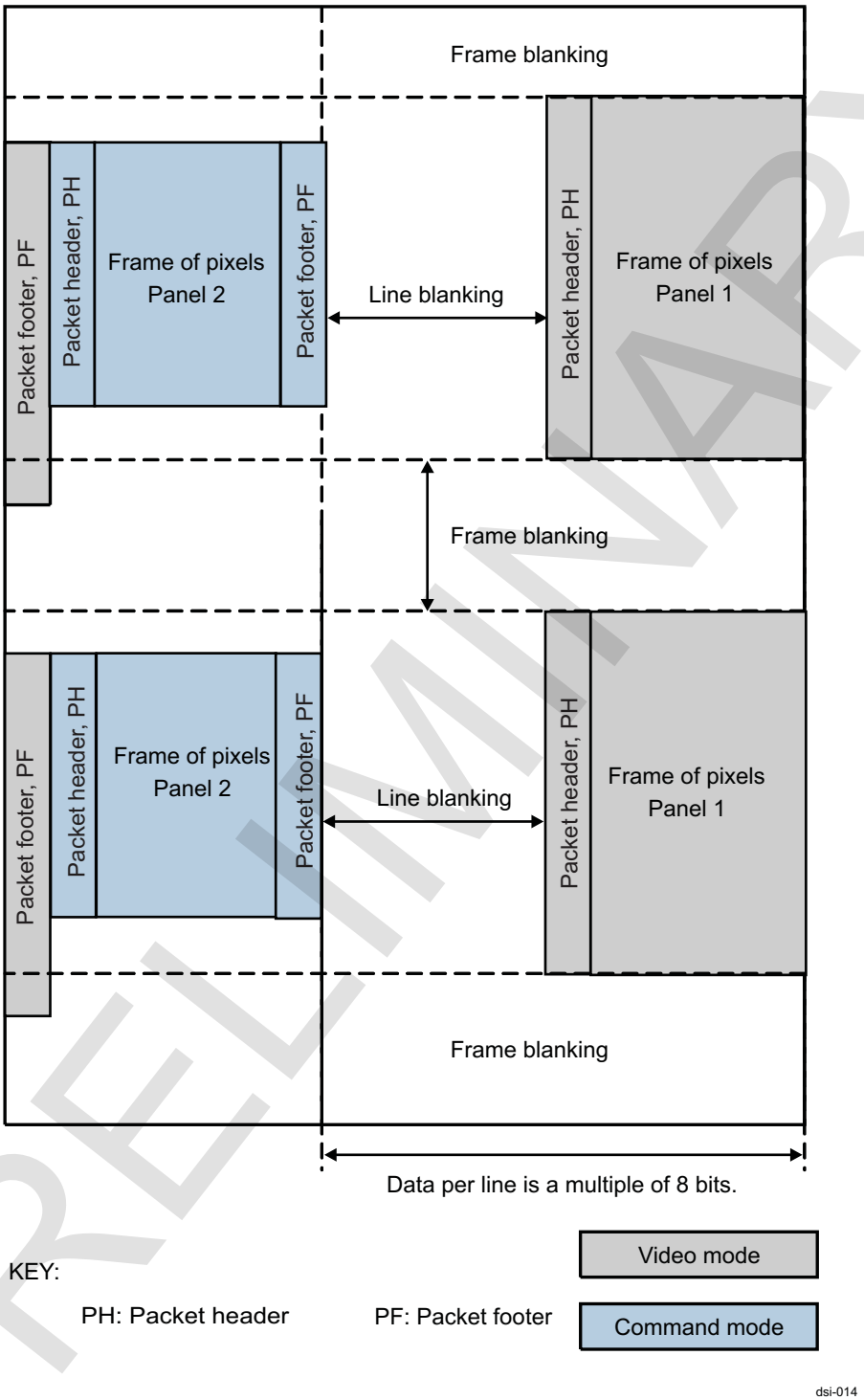
Figure 10-108. DSI General Frame Structure Using Burst Mode and Interleaving



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10.3.2.2.7 VCs

The DSI protocol layer transports VCs. VCs separate different data flows, which are interleaved in the same data stream. Each VC is identified by a unique channel identification number in the PH. The channel identification number is encoded in 2 bits. The DSI protocol engine determines the channel identifier number to be used for generating the PH and multiplexes the interleaved data streams. The DSI protocol engine supports multiple (up to 4) concurrent VCs. Table 10-466 summarizes the VC values used for each channel.

Table 10-466. VC Values

VC Number	Value
VC 0	0x0
VC 1	0x1
VC 2	0x2
VC 3	0x3

If multiple displays are connected to a single DSI port on the host, a hub can be used to route the data stream to the appropriate display based on the VC ID. Typically, VC ID 0x0 is used for the primary display and 0x1 for the secondary. The hub may have its own VC ID to provide communication capability between the host and the hub.

There is one set of registers for each VC. The attributes of the VC define the following characteristics:

- Transfer mode (DSI_VC_CTRL_i[4] MODE bit):
  - Video mode
  - Command mode
- Data type
- Source (DSI_VC_CTRL_i[1] SOURCE bit)
  - Video port
  - Slave interconnect port
- HS or LP forward transmission
- Automatic BTA generation
  - Short packets (DSI_VC_CTRL_i[2] BTA_SHORT_EN bit)
  - Long packets (DSI_VC_CTRL_i[3] BTA_LONG_EN bit)
- DMA request configurations for RX and TX
  - DMA request number (DSI_VC_CTRL_i[29:27] DMA_RX_REQ_NB bit field for RX FIFO and DSI_VC_CTRL_i[23:21] DMA_TX_REQ_NB bit field for TX FIFO)
  - DMA threshold (DSI_VC_CTRL_i[26:24] DMA_RX_THRESHOLD bit field for RX FIFO and DSI_VC_CTRL_i[19:17] DMA_TX_THRESHOLD bit field for TX FIFO)
- Mode speed (DSI_VC_CTRL_i[9] MODE_SPEED bit)
- ECC transmission (DSI_VC_CTRL_i[8] ECC_TX_EN bit)
- CS transmission (DSI_VC_CTRL_i[7] CS_TX_EN bit)

NOTE: The VC ID is not calculated by the DSI module but is provided while writing into the DSI_VC_SHORT_PACKET_HEADER_i and DSI_VC_LONG_PACKET_HEADER_i registers.

10.3.2.3 DSI Multilane Layer

A layer consists of lane splitter logic to split the incoming byte stream into a serial stream. The bits are sent with the LSB first. The number of active lanes is configurable through a register. The order of the lanes is configurable. The number of lanes can be changed only in ULPS or when all data lanes are in STOP state.

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10.3.2.3.1 SoT and EoT in Multilane Configurations

Because a HS transmission is composed of an arbitrary number of bytes that may not be an integer multiple of the number of lanes, some lanes may run out of data before others. Therefore, the lane management layer, as it buffers up the final set of less-than-N bytes, deasserts its valid data signal into lanes for which there is no further data. Although all lanes start simultaneously with parallel start-of-transmissions (SoTs), each lane operates independently and may complete the HS transmission before the other lanes, sending an end-of-transmission (EoT) one cycle (byte) earlier.

10.3.2.3.2 Lane Splitter

The lane splitter can split the byte stream into two, three, or four lanes (for one lane, the splitter is bypassed). Figure 10-109 through Figure 10-112 show the byte position in each serial link for one-, two-, three-, and four-data lane configurations. The byte stream always starts from lane 1. It finishes on one of the lanes, depending on the number of bytes to send and the number of lanes. The splitter module is used only when packets are sent using HS mode. In LS mode, only data lane 1 is used.

Figure 10-109. Four-Data Lane Configuration

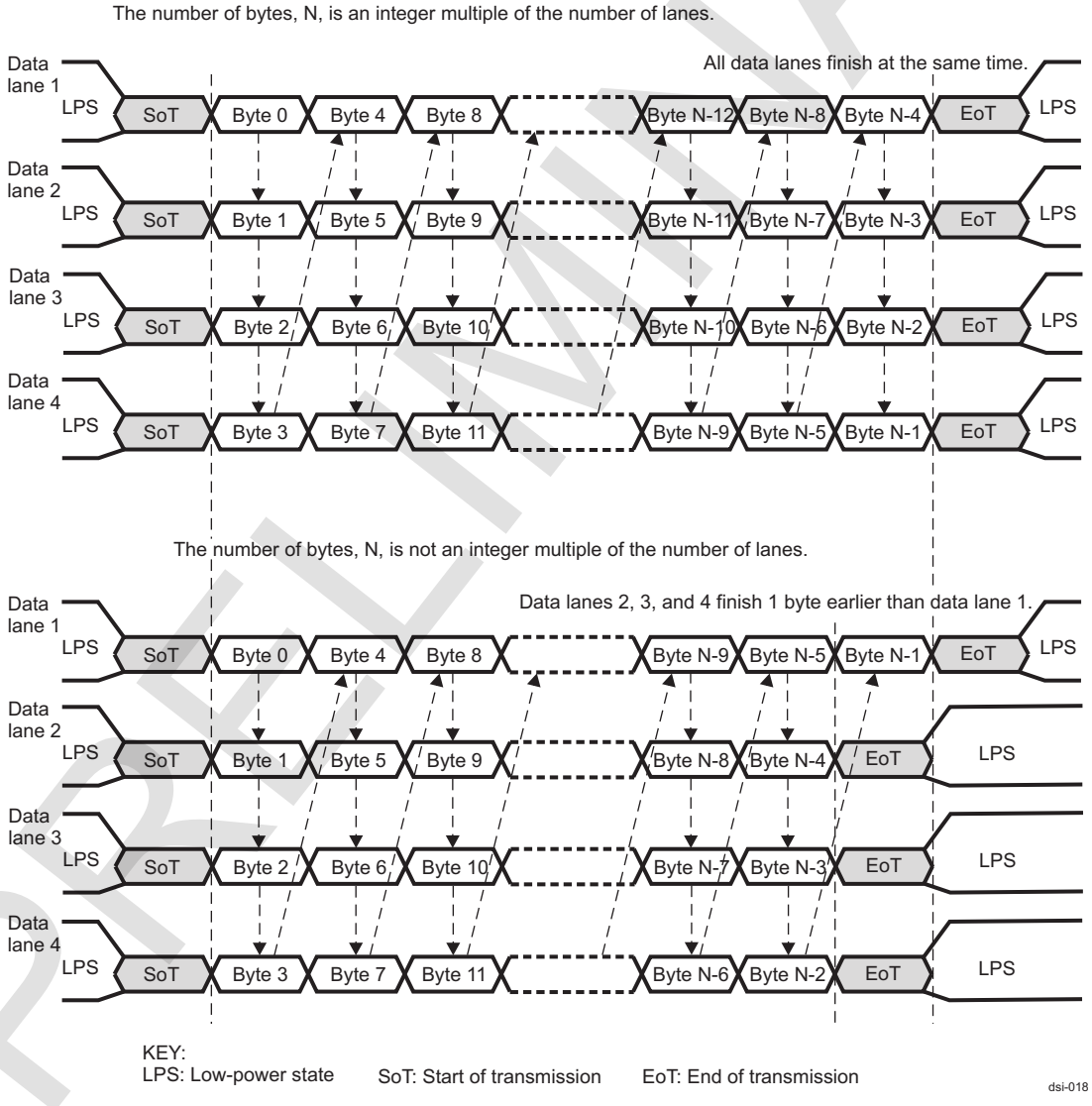

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Figure 10-110. Three-Data Lane Configuration

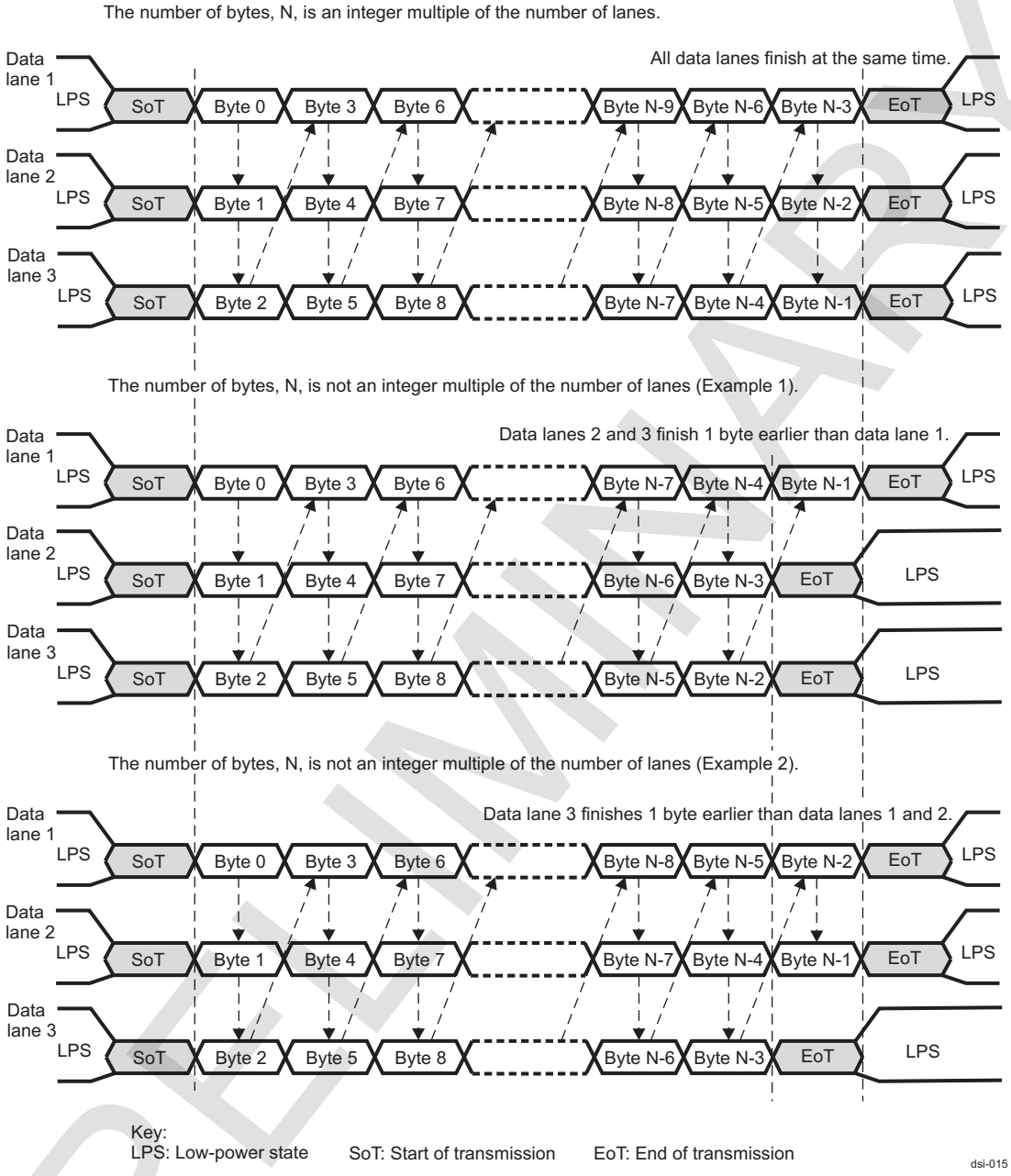

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Figure 10-111. Two-Data Lane Configuration

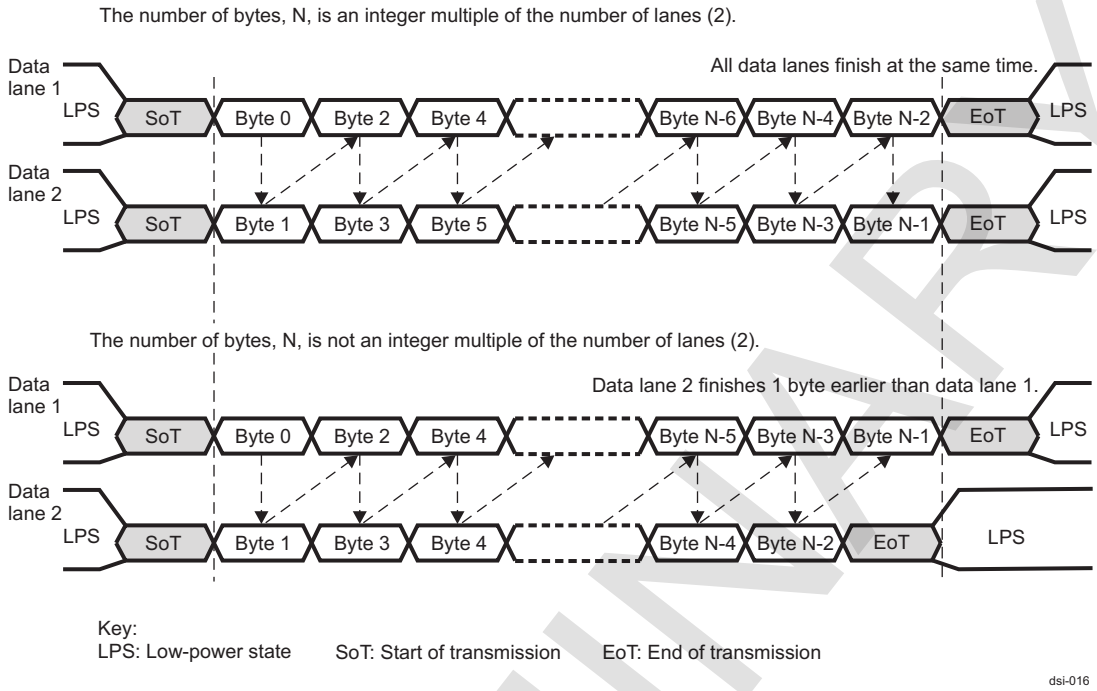
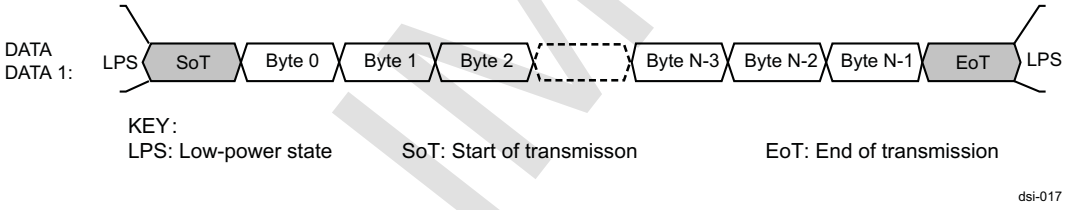
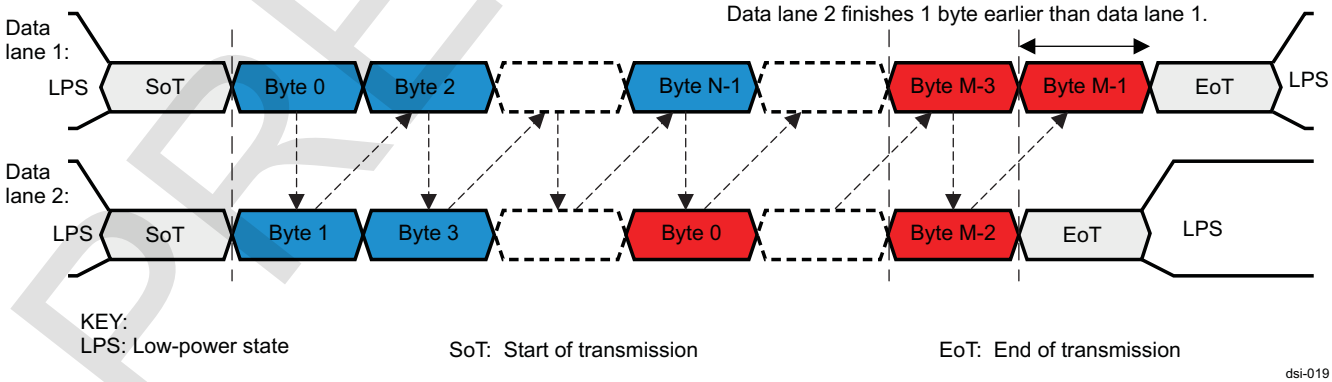


Figure 10-112. One-Data Lane Configuration



For back-to-back packets, the byte stream is considered as a single packet by the splitter module. Figure 10-113 shows an example of two packets sent back-to-back. N bytes are used for the first packet and M bytes for the second packet.

Figure 10-113. Two Packets Using Two-Data Lane Configuration (Example)



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10.3.2.4 DSI Pixel Data Formats

This section describes how the DSI-supported pixel data formats in video mode are transmitted over the serial interface. The DSI protocol engine can cope with all data formats if the data line length sent through the DSI physical protocol is a multiple of a pixel. This condition is required for the DSI protocol engine to work properly.

10.3.2.4.1 Pixel Data Formats in Video Mode

The host can send different pixel formats in video mode. Table 10-467 lists the pixel formats supported by the DSI in video mode.

Table 10-467. Pixel Data Format in Video Mode

Mode	Description
RGB888 (using 24-bit container)	RGB888
RGB666 (using 24-bit container)	RGB666
RGB666 (18-bit packet using 18-bit container)	RGB666_PACKET
RGB565 (using 16-bit container)	RGB565

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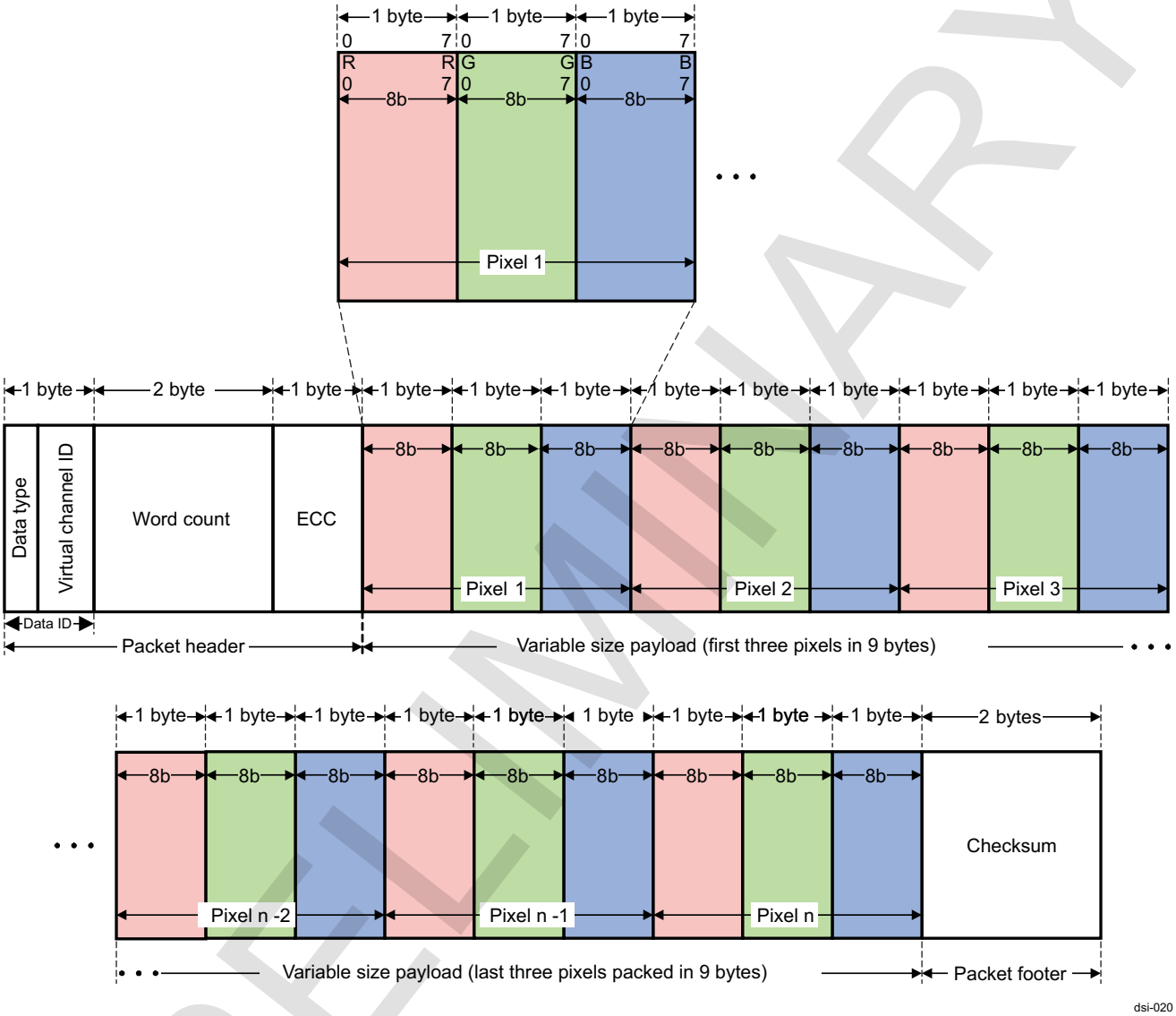
10.3.2.4.2 24 bpp – RGB Color Format, Long Packet (Video Mode)

Figure 10-114 shows the RGB888 format.

Figure 10-114. 24-bpp RGB Color Format, Long Packet (Video Mode)



Packed-pixel stream, 24-bit format is a long packet used to transmit image data formatted as 24-bit pixels to a video-mode display module. The packet consists of the data ID byte, a 2-byte WC, an ECC byte, a payload of length WC bytes, and a 2-byte checksum. The pixel format is R (8 bits), G (8 bits), and B (8 bits), in that order. Each color component occupies 1 byte in the pixel stream; no components are split across byte boundaries. Within a color component, the LSB is sent first and the MSB last.

10.3.2.4.3 24 Bits per Pixel - RGB Color Format, Long Packet (Command Mode)

Figure 10-115 shows the RGB888 format.

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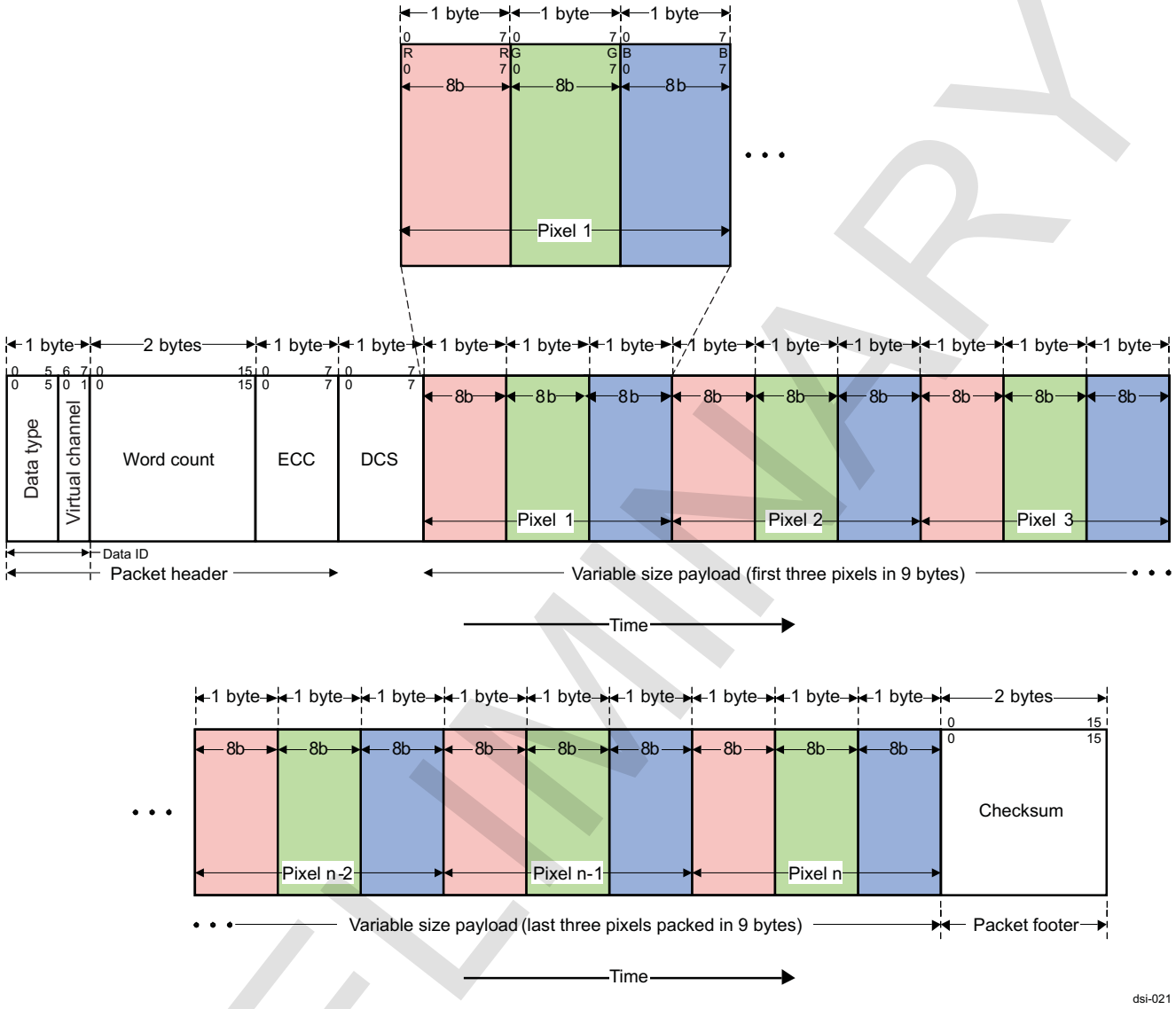
Figure 10-115. 24-bpp RGB Color Format, Long Packet (Command Mode)



This format is the same as the packed pixel stream format.

10.3.2.4.4 18 bpp (Loosely Packed) – RGB Color Format, Long Packet (Transparent for DSI Protocol Engine) (Video Mode)

Figure 10-116 shows the RGB666 format.

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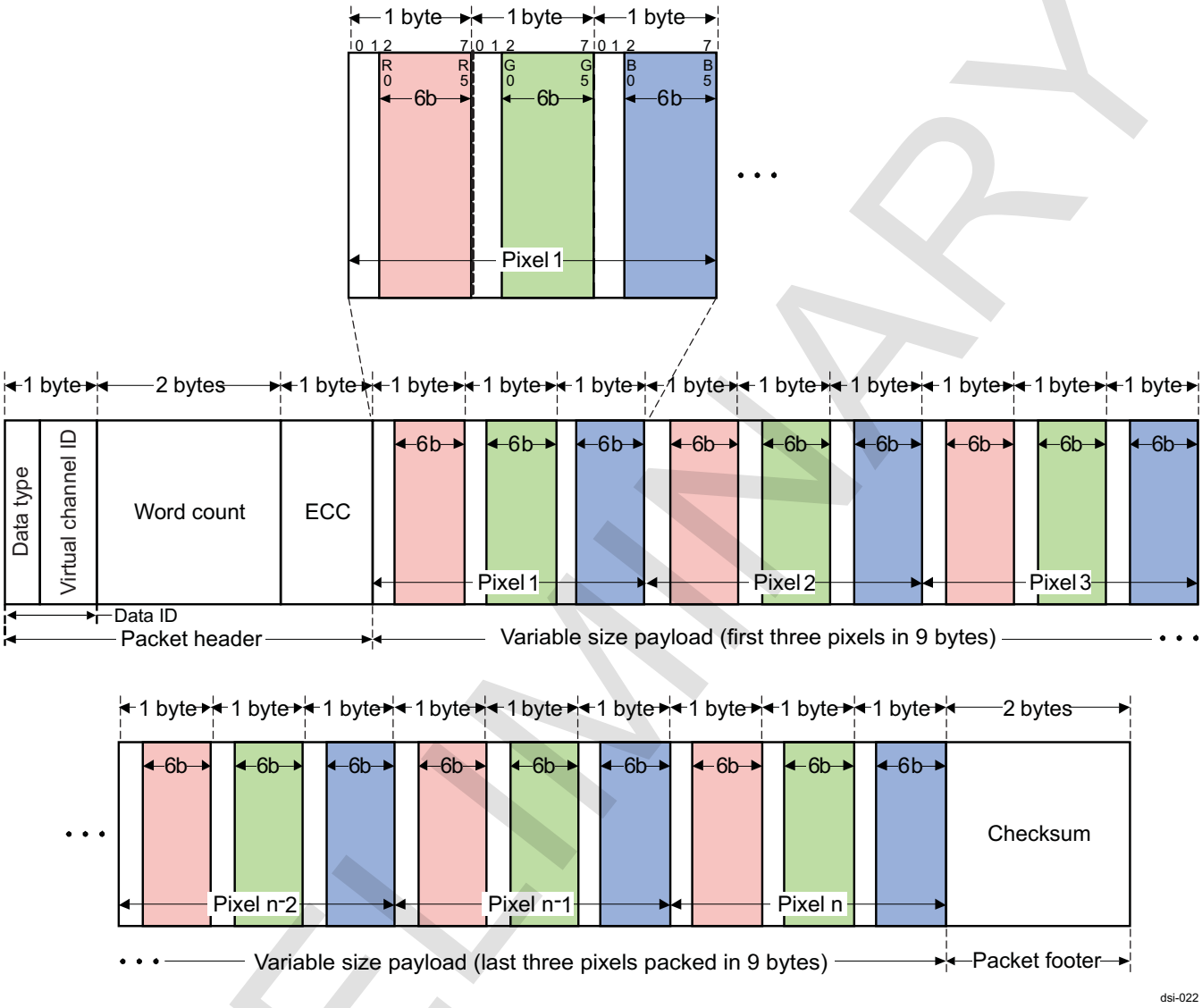
Figure 10-116. 18-bpp (Loosely Packed) RGB Color Format, Long Packet (Transparent for DSI Protocol Engine) (Video Mode)



In 18-bit loosely packed pixel format, each R, G, and B color component is 6 bits but is shifted to the upper bits of the byte, such that the valid pixel bits occupy bits [7:2] of each byte. Bits [1:0] of each payload byte representing active pixels are ignored. As a result, each pixel requires 3 bytes as it is transmitted across the link. This requires more bandwidth than packed format but requires less shifting and multiplexing logic in the packing and unpacking functions on each end of the link. This format is used to transmit RGB image data formatted as pixels to a video mode display module that displays 18-bit pixels. The packet consists of the data ID byte, a 2-byte WC, an ECC byte, a payload of length WC bytes, and a 2-byte checksum. The pixel format is R (6 bits), G (6 bits), and B (6 bits), in that order. Within a color component, the LSB is sent first and the MSB last.

10.3.2.4.5 18-bpp (Loosely Packed) – RGB Color Format, Long Packet (Command Mode)

Figure 10-117 shows the RGB666 format.

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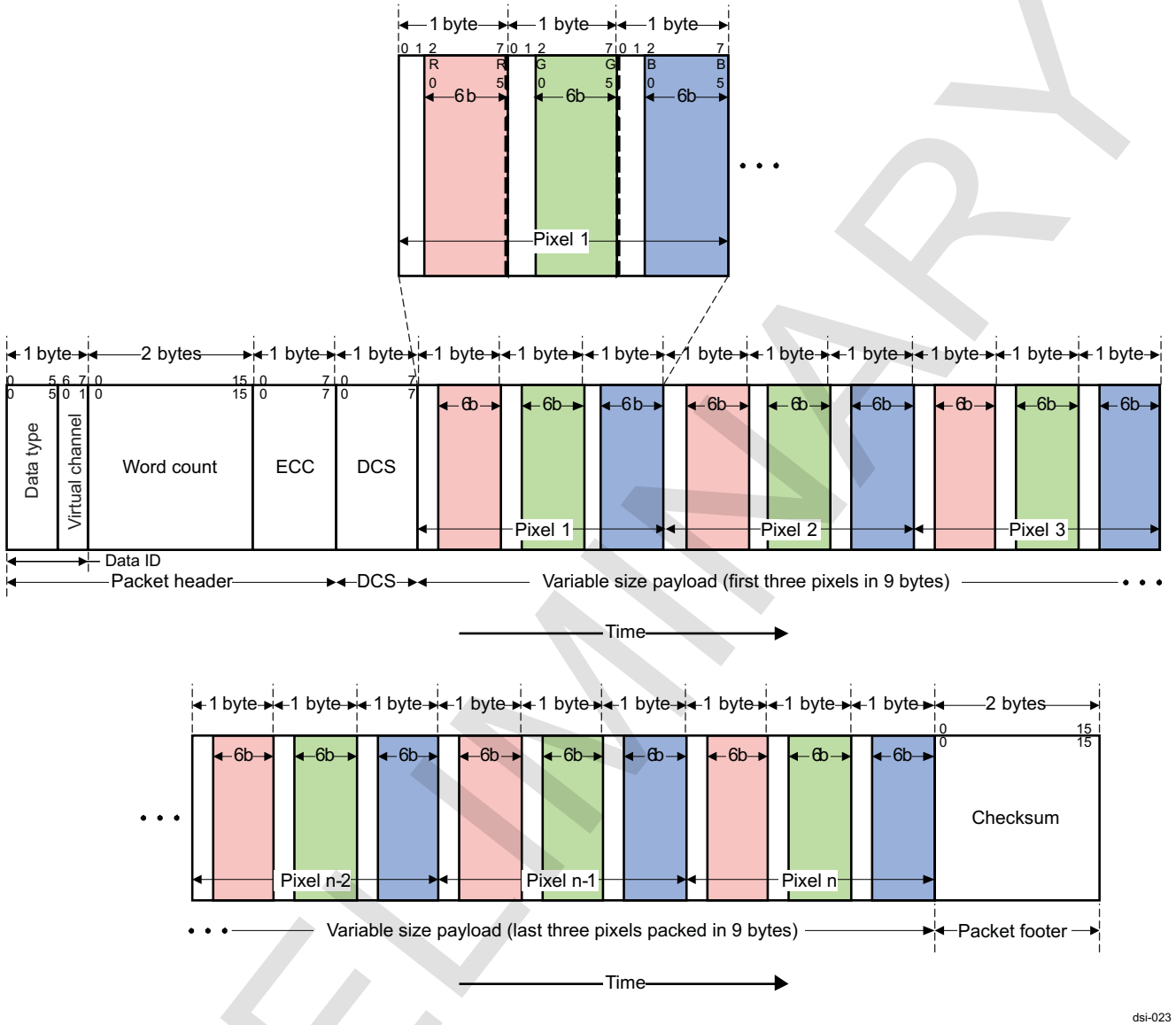
Figure 10-117. 18-bpp (Loosely Packed) RGB Color Format, Long Packet (Command Mode)



This format is the same as the packed-pixel stream format.

10.3.2.4.6 18-bpp (Packed) – RGB Color Format, Long Packet (Video Mode)

Figure 10-118 shows the RGB666_PACKED format.

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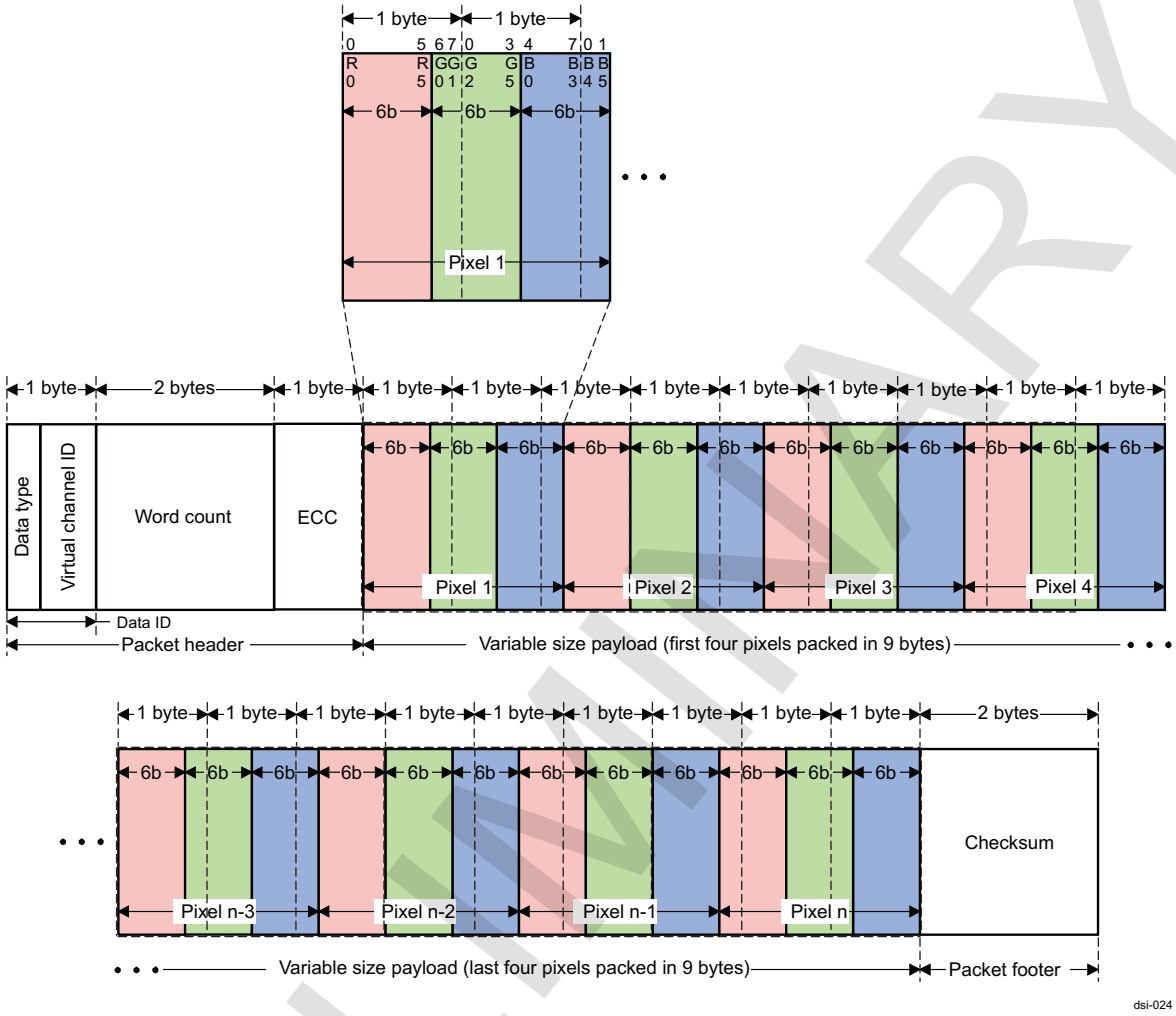
Figure 10-118. 18-bpp (Packed) RGB Color Format, Long Packet (Video Mode)



Packed pixel stream 18-bit format is a long packet. It is used to transmit RGB image data formatted as pixels to a video mode display module that displays 18-bit pixels The packet consists of the data ID byte, a 2-byte WC, an ECC byte, a payload of length WC bytes, and a 2-byte checksum. The pixel format is R (6 bits), G (6 bits), and B (6 bits), in that order. Within a color component, the LSB is sent first and the MSB last. With this format, it is strongly recommended that the total line width be a multiple of 4 pixels (9 bytes). This format is not supported in command mode.

10.3.2.4.7 16 bpp – RGB Color Format, Long Packet (Video Mode)

Figure 10-119 shows the RGB565 format.

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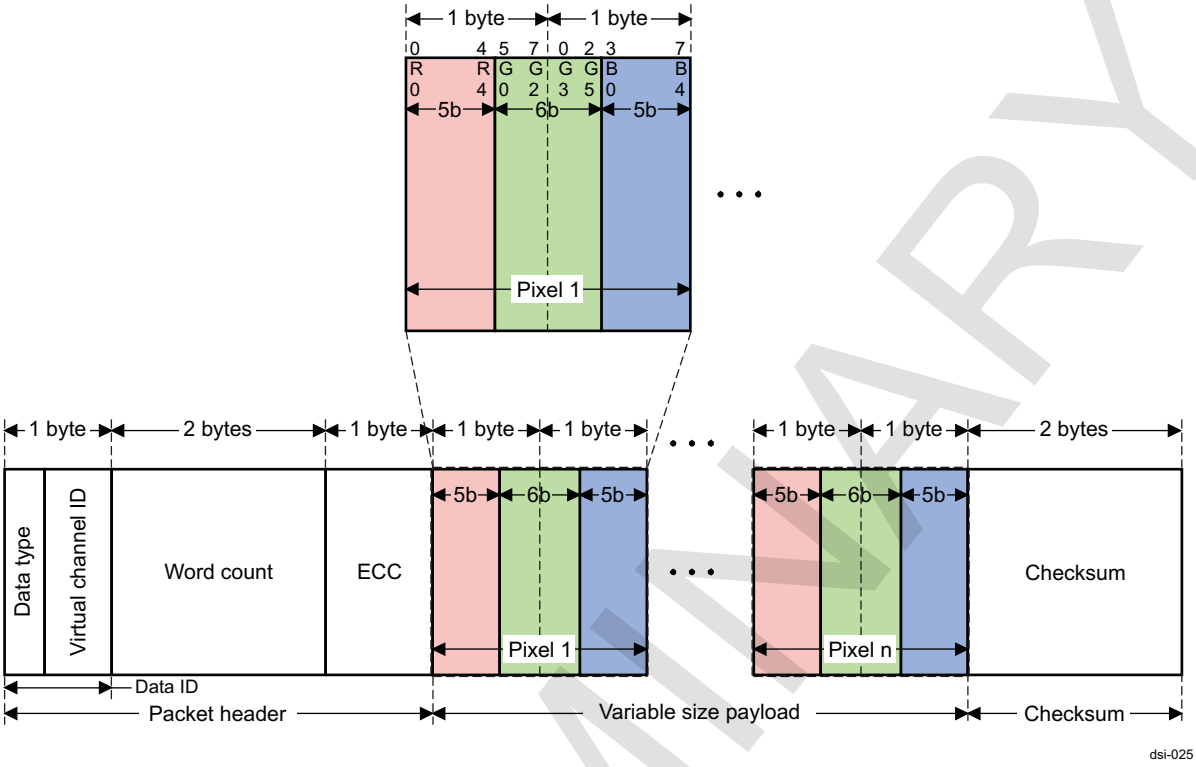
Figure 10-119. 16-bpp RGB Color Format, Long Packet (Video Mode)



Packed-pixel stream, 16-bit format is a long packet used to transmit image data formatted as 16-bit pixels to a video mode display module. The packet consists of the data ID byte, a 2-byte WC, an ECC byte, a payload of length WC bytes, and a 2-byte checksum. The pixel format is R (5 bits), G (6 bits; split across 2 bytes), and B (5 bits), in that order. Within a color component, the LSB is sent first and the MSB last.

10.3.2.4.8 16 bpp – RGB Color Format, Long Packet (Command Mode)

Figure 10-120 shows the RGB565 format.

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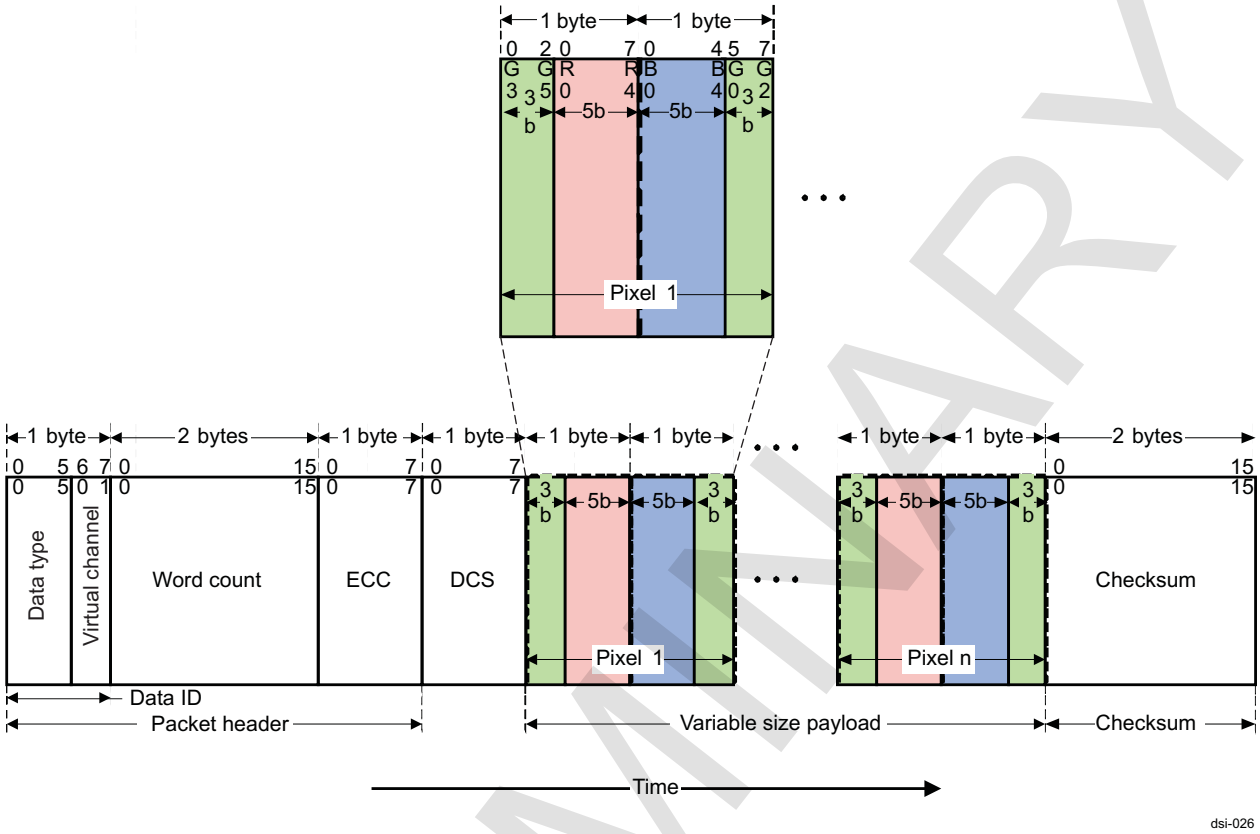
Figure 10-120. 16-bpp RGB Color Format, Long Packet (Command Mode)



This is the opposite byte order from the packed pixel stream format. To retain flexibility, the byte order is made programmable using DSI_VC_CTRL_i[12] RGB565_ORDER bit, with this order the default for command mode through the video port.

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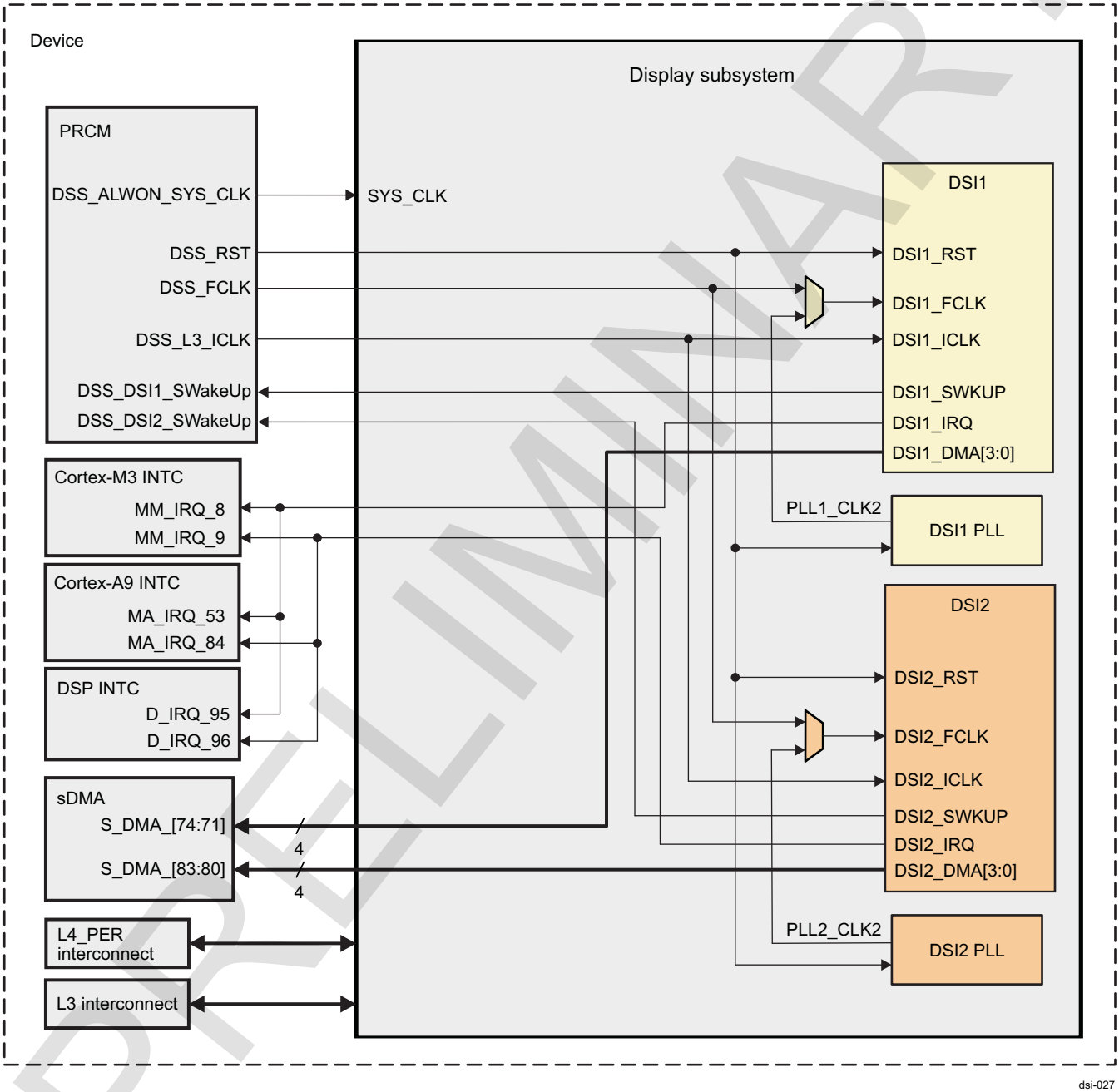
10.3.3 DSI Integration

This section describes the integration of the DSI in the device, including information about clocks, resets, and hardware requests.

Figure 10-121 shows the integration of the DSI in the device.

Figure 10-121. DSI Integration



NOTE: For more information about the wake-up request, see Section 3.1.1.1, *Clock Management*, in Chapter 3, *Power, Reset, and Clock Management*.

Table 10-468 through Table 10-471 summarize the integration of the DSI module in the device.

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Table 10-468. Integration Attributes

Module Instance	Attributes	
	Power Domain	Interconnect
MIPI DSI1	PD_DSS	L3 for data L4_PER for configuration
MIPI DSI2	PD_DSS	L3 for data L4_PER for configuration

NOTE: L3 interconnect is used primarily for data.

L4_PER interconnect is used primarily for configuration but is also used for backward software compatibility.

Table 10-469. Clocks and Resets

Clocks				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
	SYS_CLK	DSS_ALWON_SYS_CLK	PRCM module	Functional clock for the DSI PLLs
MIPI DSI1	DSI1_FCLK	DSS_FCLK PLL1_CLK2	PRCM module DSI1 PLL	Functional clock
	DSI1_ICLK	DSS_L3_ICLK	PRCM module	Interface clock
MIPI DSI2	DSI2_FCLK	DSS_FCLK PLL2_CLK2	PRCM module DSI2 PLL	Functional clock
	DSI2_ICLK	DSS_L3_ICLK	PRCM module	Interface clock
Resets				
MIPI DSI1	DSI1_RST	DISPSS_RST	PRCM module	Nonretention reset
MIPI DSI2	DSI2_RST	DISPSS_RST	PRCM module	Nonretention reset

NOTE: If video mode is used, the VPn_PCLK and VPn_CLK clocks must be generated using a CLKIN4DDR clock.

NOTE: For information about clock distribution and configuration inside the module, see Section 10.3.4.2, *DSI Clock Configuration*.

Table 10-470. Interrupt Requests

Interrupt Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
MIPI DSI1	DSS_DSI1_IRQ	D_IRQ_95	DSP INTC	Display DSI1 interrupt request
	DSS_DSI1_IRQ	MA_IRQ_53	Cortex-A9 INTC	Display DSI1 interrupt request
	DSS_DSI1_IRQ	MM_IRQ_8	Cortex-M3 INTC	Display DSI1 interrupt request
MIPI DSI2	DSS_DSI2_IRQ	D_IRQ_96	DSP INTC	Display DSI2 interrupt request
	DSS_DSI2_IRQ	MA_IRQ_84	Cortex-A9 INTC	Display DSI2 interrupt request
	DSS_DSI2_IRQ	MM_IRQ_9	Cortex-M3 INTC	Display DSI2 interrupt request

NOTE: For a description of the interrupt source, see Section 10.3.4.3, *DSI Interrupt Requests*.

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Table 10-471. DMA Requests

DMA Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
MIPI DSI1	DSS_DSI1_DMA0	S_DMA_71	sDMA	DSI1 DMA request 0
	DSS_DSI1_DMA1	S_DMA_72	sDMA	DSI1 DMA request 1
	DSS_DSI1_DMA2	S_DMA_73	sDMA	DSI1 DMA request 2
	DSS_DSI1_DMA3	S_DMA_74	sDMA	DSI1 DMA request 3
MIPI DSI2	DSS_DSI2_DMA0	S_DMA_80	sDMA	DSI2 DMA request 0
	DSS_DSI2_DMA1	S_DMA_81	sDMA	DSI2 DMA request 1
	DSS_DSI2_DMA2	S_DMA_82	sDMA	DSI2 DMA request 2
	DSS_DSI2_DMA3	S_DMA_83	sDMA	DSI2 DMA request 3

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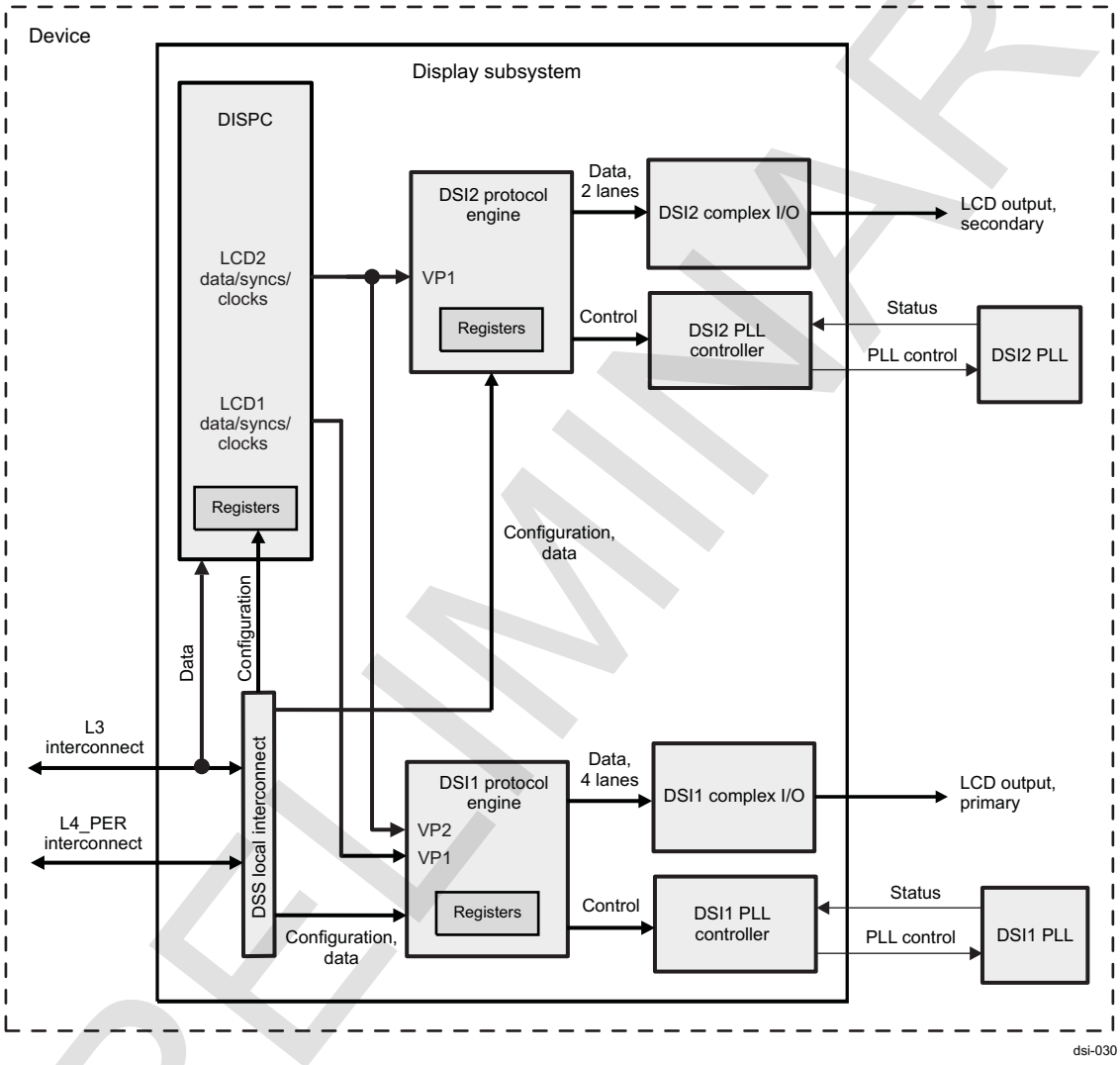
10.3.4 DSI Functional Description

This section describes the functions of the DSI1 and DSI2 modules.

10.3.4.1 DSI Block Diagram

Figure 10-122 is a schematic of DSI1 and DSI2.

Figure 10-122. DSI Schematic



10.3.4.2 DSI Clock Configuration

Figure 10-123 shows the clock tree for DSI1 and DSI2.

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Figure 10-123. DSI Clock Tree

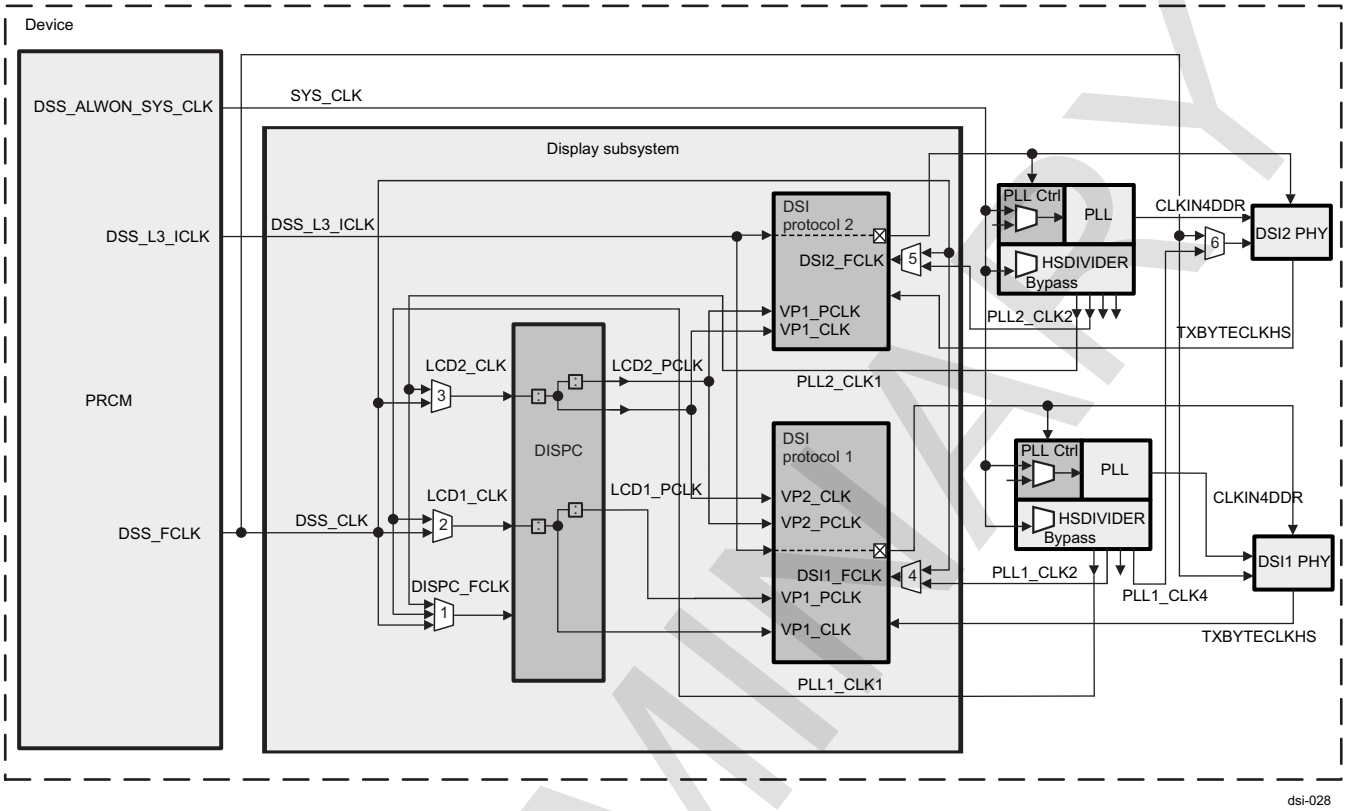

Table 10-472 shows the controls for clock multiplexers.

Table 10-472. DSI Multiplexer Controls

Destination	Source Signal Name	Source	Multiplexer Number	DSS Register Bit Field
DISPC functional clock (DISPC_FCLK)	DSS_CLK	PER_PLL	1	For more information, see Section 10.1.2 , *DSS Integration.*
	PLL1_CLK1	PLL1	1	
	PLL2_CLK1	PLL2	1	
	PLL3_CLK1	PLL3	1	
DSI1 functional clock (LCD1_CLK)	DSS_CLK	PER_PLL	2	For more information, see Section 10.1.2 , *DSS Integration.*
	PLL1_CLK1	PLL1	2	
DSI2 functional clock (LCD2_CLK)	DSS_CLK	PER_PLL	3	For more information, see Section 10.1.2 , *DSS Integration.*
	PLL2_CLK1	PLL2	3	
DSI1 protocol engine functional clock (DSI1_FCLK)	DSS_CLK	PER_PLL	4	For more information, see Section 10.1.2 , *DSS Integration.*
	PLL1_CLK2	PLL1	4	
DSI2 protocol engine functional clock (DSI2_FCLK)	DSS_CLK	PER_PLL	5	For more information, see Section 10.1.2 , *DSS Integration.*
	PLL2_CLK2	PLL2	5	

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NOTE: For more information about the DSI1 and DSI2 video port clocks (VPn_CLK and VPn_PCLK, where n = 1 or 2), see Section 10.3.4.4.5, *Video Port Interface*.

NOTE: For the frequency ratings of the various DSI clocks, see Section 10.1.2.1, *DSS Clocks*.

NOTE: Multiplexer 6, shown in Figure 10-123, allows the DSS_FCLK or PLL1_CLK4 clock to be sent on DSI2 PHY bypass input. The use of the bypassed clock allows both DSI modules to run on DSS_FCLK or on a single PLL (DSI1 PLL).

- To select the clock source for the DSI2 PHY bypass input, configure the CONTROL.CONTROL_DSS_CONTROL[0] DSS_MUX6_SELECT bit in the device control module. See Chapter 18, *Control Module*.
- To enable the bypass input for the DSI1 PHY or DSI2 PHY module, set the DSI_PLL_CONFIGURATION2[15] BYPASSEN bit to 1.

10.3.4.3 DSI Interrupt Requests

The DSI protocol engine requires a single interrupt line. The DSI_IRQSTATUS register indicates the general interrupt events. Each VC and complex I/O has a dedicated interrupt register: DSI_VC_IRQSTATUS_i and DSI_COMPLEXIO_IRQSTATUS, respectively.

Table 10-473 lists the DSI global interrupt events.

Table 10-473. DSI Global Interrupts

IRQ Name	Description
Resynchronization_IRQ	Resynchronization in video mode
TA_TO_IRQ	Turnaround timer expired
SYNC_LOST_IRQ	Synchronization with video port is lost (video mode only).
ACK_TRIGGER_IRQ	Acknowledge trigger is received.
TE_TRIGGER_IRQ	TE PHY trigger is received.
WAKEUP_IRQ	Occurs when the SWakeUp signal is asserted.
HS_TX_TO_IRQ	HS TX time-out Interrupt
LP_RX_TO_IRQ	LS RX time-out Interrupt
COMPLEXIO_ERR_IRQ	Error signaling from complex I/O: The interrupt is triggered when an error is received from the complex I/O (events are defined in DSI_COMPLEXIO_IRQSTATUS).
PLL_RECAL_IRQ	PLL recalibration event (assertion of DSIRecal signal from the DSI PLL control module)
PLL_UNLOCK_IRQ	PLL un-lock event (deassertion of DSILock signal from the DSI PLL control module)
PLL_LOCK_IRQ	PLL lock event (assertion of DSILock signal from the DSI PLL control module)
VIRTUAL_CHANNEL3_IRQ	VC 3 error signaling from DSI VC 3: The interrupt is triggered when an error is received from DSI VC 3 (events are defined in DSI_VC-_IRQENABLE_i register, where i = 3).
VIRTUAL_CHANNEL2_IRQ	VC 2 error signaling from DSI VC 2: The interrupt is triggered when an error is received from DSI VC 2 (events are defined in DSI_VC_IRQENABLE_i register, where i = 2).
VIRTUAL_CHANNEL1_IRQ	VC 1 error signaling from DSI VC 1: The interrupt is triggered when an error is received from DSI VC 1 (events are defined in DSI_VC_IRQENABLE _i register, where i = 1).
VIRTUAL_CHANNEL0_IRQ	VC 0 error signaling from DSI VC 0: The interrupt is triggered when an error is received from DSI VC 0 (events are defined in DSI_VC_IRQENABLE_i register, where i = 0).
TE0_LINE_IRQ	TE detected on TE0 CMOS input signal
TE1_LINE_IRQ	TE detected on TE1 CMOS input signal

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NOTE: For information about other internal DSI interrupt events, see Table 10-491 and Table 10-498 .

10.3.4.4 DSI Protocol Engine

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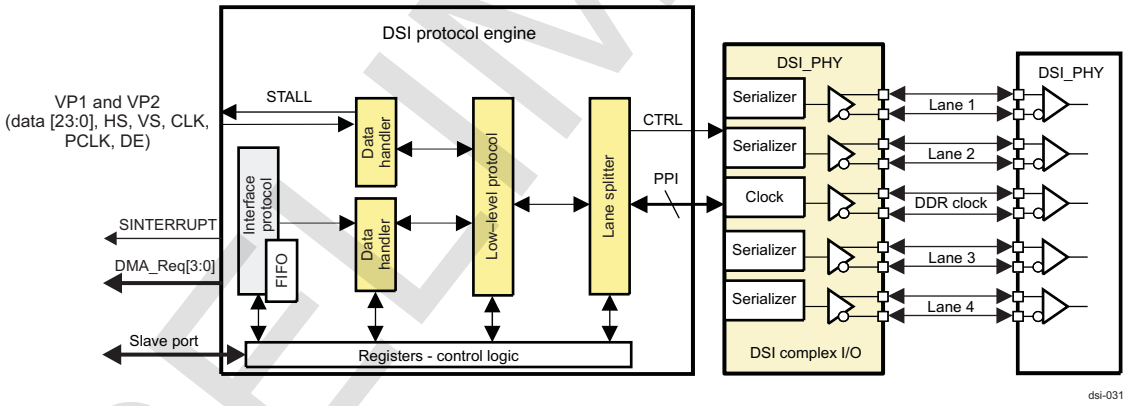
The DSI protocol engine integrates the DSI with the display through the DSI_PHY module, local interconnect interface, and video interface from the DISPC. The DSI_PHY or complex I/O module is described in Section 10.3.4.6, *DSI Complex I/O*. The DSI transmitter (protocol engine + PHY) port can be connected to multiple displays using a single DSI host port. The DSI protocol engine controls the DSI PLL control module described in Section 10.3.4.5, *DSI PLL Controllers*. The DSI transmitter port can be used in video mode or/and command mode.

10.3.4.4.1 DSI Protocol Overview

The DSI protocol engine receives data from the DISPC video port and/or the L3 interconnect slave port, encapsulates them with the VC ID, generates the ECC and checksum, and splits the data into byte streams to the DSI_PHY to be sent using LS or HS protocol. The DSI protocol engine receives data and acknowledges from the panel using the same DSI link in case of bidirectional panel. Multiple data streams can be interleaved to support multiple panels connected to the same host DSI port. Figure 10-124 shows the DSI protocol engine, with an example of data lane and clock lane ordering. It is possible to configure other orders through registers as described in Section 10.3.2.1.1, *Data/Clock Configuration*.

Figure 10-124. DSI Protocol Engine



NOTE: Figure 10-124 gives information for DSI1 with its four data lanes. DSI2 has only two data lanes.

NOTE: The order of the PHY pairs (clock and data lanes) is informative. Each PHY pair can be clock or data. DSI complex I/O receives the configuration for the pin order and the differential ± in a pair from the settings in the DSI_COMPLEXIO_CFG1 register.

10.3.4.4.2 DSI Global Register Controls

Before receiving data from the DSI complex I/O, the DSI_PHY SCP registers in the DSI complex I/O must be configured. Table 10-474 lists the register access width limitations for all the DSI modules.

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Table 10-474. Register Access Width Limitations

Register Name	Register Access Width
All DSI complex I/O registers (DSI_PHY SCP)	32-bit only
All DSI PLL control module registers	32-bit only
DSI_VC_LONG_PACKET_HEADER_i	32-bit only
DSI_VC_SHORT_PACKET_HEADER_i	32-bit only
DSI_VC_LONG_PACKET_PAYLOAD_i	16- and 32-bit
All other DSI protocol engine registers	8-, 16-, and 32-bit

CAUTION

If a different access width than listed in Table 10-474 is used, an interface error is generated in response to the write using SResp = ERR.

The DSI protocol engine is globally controlled by the DSI_CTRL register. The interface to the complex I/O is enabled by setting the DSI_CTRL[0] IF_EN bit. When the interface is disabled, it is possible to provide data to the TX FIFO and read pending data in the RX FIFO. When the DSI_CTRL[0] IF_EN bit is set to 1, the pending packets are sent to the DSI complex I/O, and the data transfer from the video port is ignored until the first vertical sync event is received.

When the DSI_CTRL[0] IF_EN bit is reset by software, the DSI protocol engine must finish the transfer of the pending data in the TX FIFO and wait for a response if BTA has been sent (the protocol engine is in receive mode); hardware then resets the DSI_CTRL[0] IF_EN bit. When using video mode, the VC associated with the video port must be enabled before enabling the interface according to the following sequence:

1. The DSI_CTRL[0] IF_EN bit is equal to 0.
2. Enable the VC associated with video mode by setting the DSI_VC_CTRL_i[0] VC_EN bit.
3. Set the DSI_CTRL[0] IF_EN bit to 1.

10.3.4.4.3 DSI Transfer Modes

Two main transfer modes are supported by the DSI modules:

- Video mode: Pixels are received from the video port (VP1 or VP2.) There are some real-time constraints (pixels must be sent at the pixel frequency required by the panel module).
- Command mode: Pixels can be received from the video port or from the L3 interconnect slave port. There are no real-time constraints except that the TE must be avoided by starting the transfer at the correct time during the scan of the display and that it must be fast enough.

10.3.4.4.3.1 Video Mode

Video mode refers to the MIPI display pixel interface (DPI) standard. The sync events and pixels must be sent according to the display mode timings. Data is received from the video ports. The DISPC fetches the data from the system memory and provides it to the DSI protocol engine through VP1 or VP2. The short packets used for the sync event use precalculated 32-bit values. The long packets are constructed using the header defined in the DSI_VC_LONG_PACKET_HEADER_i registers. In case of synchronization short packets for video mode, because hardware generates short packets without using the DSI_VC_SHORT_PACKET_HEADER_i register, if the DSI_VC_CTRL_i[8] ECC_TX_EN bit is set, the ECC is calculated; otherwise, 0 is used. The feature is used to generate incorrect ECC for debug purpose and to ease the check of the link and peripheral error detection and correction.

The DSI_VM_TIMING1 through DSI_VM_TIMING8 registers define the timings of the video mode.

The DSI_VM_TIMING2[27:24] WINDOW_SYNC bit field defines the synchronization period. The recommended value is 0x4 based on the implementation of the resynchronization scheme.

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The DSI_CTRL[20] BLANKING_MODE bit defines whether long blanking packets or LPS are used during the blanking periods (except HFP, HBP, and HSA defined by other bits) when there is no pending data in TX FIFO ready to be sent. Software must ensure that there is no data in the TX FIFO, no BTA, no RESET trigger sent, and the DSI_VC_CTRL_i[9] MODE_SPEED bit is set to 1 (HS mode) to keep the video mode transfer in HS mode during blanking periods (except for the last blanking period, because it is required to go to LPS at least once per frame).

The DSI_CTRL[21] HFP_BLANKING_MODE, DSI_CTRL[22] HBP_BLANKING_MODE, and DSI_CTRL[23] HSA_BLANKING_MODE bits define whether during these blanking packets data from TX FIFO or long blanking packets are sent.

To ensure that the writes to the DSI_VC_LONG_PACKET_HEADER_i register are handled correctly as header information for video mode long packets, the following registers must be programmed:

- DSI_VC_CTRL_i[0] VC_EN bit set to 0
- DSI_VC_CTRL_i[4] MODE bit set to 1
- DSI_VC_LONG_PACKET_HEADER_i register access
- DSI_VC_CTRL_i[0] VC_EN bit set to 1

NOTE: The hardware ignores DSI_VC_CTRL_i[1] SOURCE and DSI_VC_CTRL_i[9] MODE_SPEED bits when video mode is selected (the DSI_VC_CTRL_i[4] MODE bit set to 1).

The SYNC_LOST_IRQ and RESYNCHRONIZATION_IRQ interrupt events indicate whether the DSI protocol engine has not been able to resynchronize the video port timing to its own timing base or if it has been done. The RESYNCHRONIZATION_IRQ indicates to the software user that the video port works but the configuration of the timings for the DISPC and for DSI protocol engine may need to be modified to avoid the resynchronization. The SYNC_LOST_IRQ and RESYNCHRONIZATION_IRQ events can be respectively monitored in DSI_IRQSTATUS[18] SYNC_LOST_IRQ and DSI_IRQSTATUS[5] RESYNCHRONIZATION_IRQ status bits.

10.3.4.4.3.2 Command Mode

The command mode refers to the MIPI display command set (DCS) standard. The commands, parameters, and pixels are sent to the display module with limited real-time constraints (as defined in Section 10.3.4.4.3.1, *Video Mode*). The pixels can be provided on one of the two video ports by the DISPC or on the L3 interconnect slave port.

The DSI_VC_LONG_PACKET_HEADER_i registers are used for the header of long packets; the DSI_VC_SHORT_PACKET_HEADER_i registers are used for the short packets.

For the payload, the DSI_VC_LONG_PACKET_PAYLOAD_i register is used. Each 32-bit payload data is written to the DSI_VC_LONG_PACKET_PAYLOAD_i register from the MPU subsystem or sDMA. It is buffered to send packets with higher rate than the L3 interconnect frequency can provide. If DSI_VC_CTRL_i[30] DCS_CMD_ENABLE = 1, the word count defined in the DSI_VC_LONG_PACKET_HEADER_i register is used to determine the number of bytes to be sent using the DSI_VC_LONG_PACKET_PAYLOAD_i register minus the size of the DCS command header added by the protocol engine at the beginning of the payload (also sent using the DSI_VC_LONG_PACKET_PAYLOAD_i register). If DSI_VC_CTRL_i[30] DCS_CMD_ENABLE = 0, the word count defined in the register DSI_VC_LONG_PACKET_HEADER_i register is used to determine the number of bytes to be sent using the DSI_VC_LONG_PACKET_PAYLOAD_i register.

The DSI_VC_CTRL_i[11:10] OCP_DATA_BUS_WIDTH bit field is used to define the size of the data on the L3 interconnect slave port for the write access (read access to the RX FIFO in not affected by the bit field value):

- 0x0: 16-bit data width (LSB of the 32-bit interface port data bus)
- 0x1: 24-bit data width (LSB of the 32-bit interface port data bus)
- 0x2: 2x16-bit data width (first pixel on the LSB of the 32-bit Interface port data bus and second pixel on the MSB of the 32-bit interface port data bus for the same interface access)
- 0x3: 32-bit data width (no bit, no byte, no pixel manipulation)

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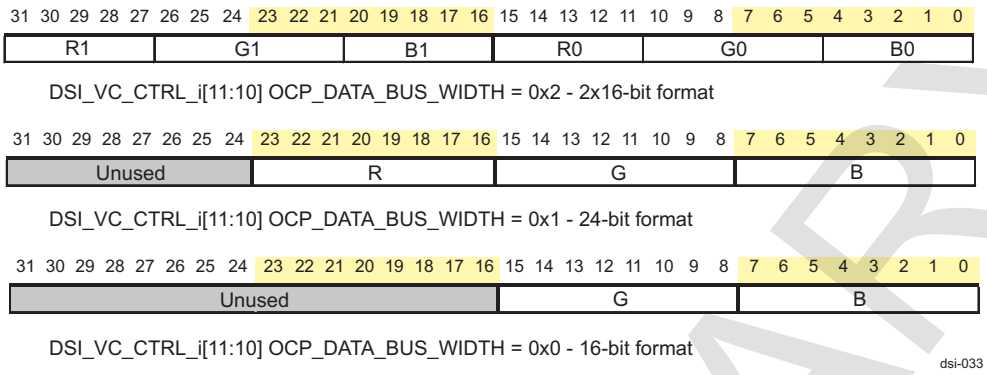
Figure 10-125 shows the different data width configurations of the L3 interconnect slave port.

Figure 10-125. Interface Data Configuration



NOTE: To provide 18-bit pixel loosely packed format to the L3 interconnect slave port, the DSI_VC_CTRL_i[11:10] OCP_DATA_BUS_WIDTH bit field must be set to 0x1. The 18-bit pixel packed format is not supported in case of command mode on the L3 interconnect slave port.

The write into the DSI_VC_LONG_PACKET_HEADER_i register is required before accessing the DSI_VC_LONG_PACKET_PAYLOAD_i register. The DSI protocol engine must extract the length of the payload and discard the extra data sent using the DSI_VC_LONG_PACKET_PAYLOAD_i register. Writes into the DSI_VC_LONG_PACKET_HEADER_i register are valid only if the VC is enabled; otherwise, the write is ignored. When receiving pixels on the video port, only the DSI_VC_LONG_PACKET_HEADER_i register is used. The video port pixels are used for the payload.

10.3.4.4.3.2.1 Command Mode TX FIFO

The single TX FIFO is used to store data from the L3 interconnect before sending it to the panel. The configuration of the FIFO for a specific VC must be done only when the VC is disabled.

The VC must not be enabled when data is still pending in the TX FIFO for the corresponding space allocated for the VC from the previous active period. When the VC space in the TX FIFO is empty, the VC can be enabled.

For each VC, two dedicated registers (DSI_VC_LONG_PACKET_HEADER_i and DSI_VC_LONG_PACKET_PAYLOAD_i) are used to provide data for long packets. The DSI_VC_SHORT_PACKET_HEADER_i register is used to provide data for short packets (32 bits long).

For each long packet, the DSI_VC_LONG_PACKET_HEADER_i register must be written first, and then the DSI_VC_LONG_PACKET_PAYLOAD_i register. The only exception is when the word count defined in the header equals 0. In that case, it is not required to write into the payload register. For consecutive long packets, the header must be written into the DSI_VC_LONG_PACKET_HEADER_i register even if the value remains the same.

The TX FIFO stores all the pending bytes to be sent to the peripheral(s). Multiple receivers can be addressed using the VC capability.

The 32-bit write requests for each VC to the TX FIFO are kept in order while sending the data to the DSI_PHY inside the VC requests. The only exception is the last 32-bit write for the last bytes of the payload data, because it can be 1, 2, 3, or 4 bytes.

When the last transfer is a 32-bit write, but the number of valid bytes is only 1, 2, or 3 (calculated using the header word count and the number of bytes are received for the payload), hardware stores the 32-bit value into the TX FIFO but the invalid bytes are not sent and are discarded.

When the word count defined in the DSI_VC_LONG_PACKET_HEADER_i register is not a multiple of the request threshold value defined in the DSI_VC_CTRL_i[19:17] DMA_TX_THRESHOLD bit field, 32-bit requests and/or bytes are discarded by hardware to store in FIFO only the exact number of valid bytes.

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The triggering event to send data to the DSI link is one of the following events:

- All bytes have been received in the FIFO (header + payload).
- The space of the FIFO allocated for the VC is full.
- The space of the FIFO allocated for the VC is not enough to request more data using DMA request (the threshold value is bigger than the space left in the TX FIFO for the VC).
- When the VC is disabled, the remaining bytes in the FIFO are sent to the DSI link.

NOTE: In case video mode is active, the blanking period must be large enough to allow the transfer of the packet(s).

Sequential arbitration must be set (DSI_CTRL[3] bit TX_FIFO_ARBITRATION = 0x1) if only one VC is used to send multiple packets during the same blanking period.

When consecutive packets should be sent in HS mode, to ensure that there is no LP transition between them, at least one of the following conditions must be valid:

- Packets from the same VC
- Short packets or long packets with a payload size multiple of 4 bytes

To stop a transfer immediately when packets are being transferred from the TX FIFO to DSI_PHY, a flush of the FIFO is necessary. It can be required in a dead-lock situation to flush the FIFO even if bytes are still in the FIFO. In that case, it is necessary to ensure having a known state of the whole DSI protocol engine module (software reset may be required) to start of new transfer through the TX FIFO.

To flush the FIFO (discard the data) for some pending bytes:

1. Change the size of the space of FIFO to 0 by writing DSI_TX_FIFO_VC_SIZE VCi_FIFO_SIZE bit fields (where i is the VC number from 0 to 3).
2. Disable the VC by resetting the DSI_VC_CTRL_i[0] VC_EN bit to 0.
3. Wait for DSI_VC_CTRL_i[15] VC_BUSY = 0 (VC_BUSY is set to 0 after TX FIFO flush is done).

It is necessary to check that there is no pending request before changing the size of the allocated FIFO for the VC by reading the relevant DSI_VC_CTRL_i[15] VC_BUSY bit or by using the interrupt PACKET_SENT_IRQ. This interrupt is monitored by reading the DSI_VC_IRQSTATUS_i[2] PACKET_SENT_IRQ status bit.

The DSI_CTRL[3] TX_FIFO_ARBITRATION bit defines the arbitration scheme:

- Round-robin between enabled VCs with pending ready requests (that is, all bytes for the packets are in the FIFO or the space of the FIFO for the VC is full) starting from the VC that has the lowest VC ID number.
- Sequential: All the pending ready requests for one VC are sent before moving to another VC. The condition of "space of the FIFO is full" is evaluated after the end of each packet.

To use in-order for all requests for all channels, a single VC must be used. (The VC ID defined in the header provided to hardware using the DSI_VC_LONG_PACKET_HEADER_i or DSI_VC_SHORT_PACKET_HEADER_i register is not used and not modified by the DSI protocol engine.)

The DSI_TX_FIFO_VC_SIZE register defines the allocated number of 33-bit values for each VC in the TX FIFO and the start address for each VC. The size of the space allocated in the TX FIFO is defined by the DSI_TX_FIFO_VC_SIZE register - VCi_FIFO_SIZE bit fields. It must be a multiple of the threshold defined in the DSI_VC_CTRL_i[19:17] DMA_TX_THRESHOLD bit field. To change the size of the space of the memory allocated for a specific VC, the VC must be disabled by setting the DSI_VC_CTRL_i[0] VC_EN bit to 0. The whole FIFO cannot be used by all the VCs at the same time because a VC can be disabled to change one or multiple parameters. Software users must configure the start address and size for each VC correctly.

Table 10-475 lists the corresponding values for the size of the space allocated in the FIFO.

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Table 10-475. VC TX FIFO Size Values

DSI_TX_FIFO_VC_SIZE.VCi_FIFO_SIZE (where i = 0, 3)	Space Size (up to the Size of the FIFO)
0	0 x 33 bits
1	32 x 33 bits
2	64 x 33 bits
3	96 x 33 bits
4	128 x 33 bits

NOTE: TX FIFO is 128 x 33 bits. Therefore, the sum of all VC FIFO allocations cannot exceed 128 x 33 bits.

CAUTION

Bit 32 of each location in the FIFO is used by the DSI protocol engine to tag the data in the TX FIFO. It is for internal use only.

Table 10-476 lists the start address of the space in the FIFO.

Table 10-476. VC TX FIFO Start Address

DSI_TX_FIFO_VC_SIZE.VCx_FIFO_ADD (where x = 0, 2)	Start Address
0	0
1	32
2	64
3	96
4	128

CAUTION

The different VC spaces must not overlap.

When the TX FIFO is full:

- The overflow interrupt (FIFO_TX_OVF_IRQ) is generated in the DSI_VC_IRQSTATUS_i[3] FIFO_TX_OVF_IRQ status bit.
- There is no L3 interconnect error generated.
- The interface commands are accepted but the data are not written into the FIFO.

To ensure that all writes are stored correctly in the TX FIFO, the FIFO must not be full. The room in the space allocated for the VC in the TX FIFO is given in the DSI_TX_FIFO_VC_EMPTINESS register. When there is no space allocated in the TX FIFO for the VC, the DSI_TX_FIFO_VC_EMPTINESS register indicates a value of 0 for the VC space emptiness.

While waiting to receive the first VSYNC event on the video port to start video mode on the DSI link, no command data from TX FIFO is sent on the interface. This is required to ensure that, when receiving the VSYNC event, there is no ongoing command mode transfer that could delay the start of video mode on the the DSI link.

10.3.4.4.3.2.2 Command Mode RX FIFO

The RX FIFO stores the data received from the DSI complex I/O. The data are always packed in the RX FIFO (single or multiple packets received during single or multiple BTA periods).

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The read requests (single or burst) can be less than, equal to, or greater than the packet size. If the packet size is smaller than the read request, the following packet(s) is also transferred. If the packet size is longer than the read request, only part of the packet is transferred. In that case, the logic keeps the VC information to provide the rest of the data during the next read request(s).

The DSI_RX_FIFO_VC_SIZE register defines the allocated number of 33-bit values for each VC in the RX FIFO and the start address for each VC. Only the enabled VCs are considered.

To change the size of the memory space allocated for a specific VC, the VC must be disabled by resetting the DSI_VC_CTRL_i[0] VC_EN bit to 0. The entire FIFO cannot be used by the entire VC at the same time because a VC can be disabled to change one or multiple parameters. Software users must configure the start address and size for each VC correctly.

Table 10-477 lists the corresponding values for the size of the space allocated in the FIFO:

Table 10-477. VC RX FIFO Size Values

DSI_RX_FIFO_VC_SIZE.VCi_FIFO_SIZE (where i = 0, 3)	Space Size (up to the size of the FIFO)
0	0 x 33 bits
1	32 x 33 bits
2	64 x 33 bits
3	96 x 33 bits
4	128 x 33 bits

NOTE: RX FIFO is 128 x 33 bits. Therefore, the sum of all VC FIFO allocations cannot exceed 128 x 33 bits.

CAUTION

Bit 32 of each location in the FIFO is used by the DSI protocol engine to tag the data in the RX FIFO. It is for internal use only.

Table 10-478 lists the start address of the space in the FIFO.

Table 10-478. VC RX FIFO Start Address

DSI_RX_FIFO_VC_SIZE.VCx_FIFO_ADD (where x = 0, 2)	Start Address
0	0
1	32
2	64
3	96
4	128

CAUTION

The different VC spaces must not overlap.

While reading the received bytes in the RX FIFO, only the DSI_VC_SHORT_PACKET_HEADER_i register is used, because hardware does not keep track of the header position for long packets and the start/end of each packet. Software must extract the information from the bytes read from the RX FIFO. There is no specific hardware to track the received bytes in the RX FIFO. The DSI_VC_LONG_PACKET_HEADER_i and DSI_VC_LONG_PACKET_PAYLOAD_i registers are not used.

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The ECC is used only by the first header when receiving multiple packets during the same LP RX transfer from the peripheral because the DSI protocol engine does not parse the header to identify the length of the packets. In case of multiple packets, the checksum is not enabled because hardware checks the checksum considering a single packet. The ECC in the first header is used to correct and check the header. For the following headers in the same LP RX transfer, hardware does not detect a header and cannot check and/or detect errors in the headers of the packets except for the first packet.

When the RX FIFO is empty:

- No interface error is generated.
- Commands are accepted and the data for the responses are 0s.

10.3.4.4.3.2.3 Command Mode DMA Requests

The DMA requests (DSI_DMA_REQ) are used to allow automatic transfer by the sDMA or MPU (with less efficiency and throughput capability) from the DSI RX FIFO to the system memory and from the system memory to the DSI TX FIFO. Two independent DMA requests for RX FIFO and TX FIFO for the same VC are supported. The read and write accesses can use burst structure.

The thresholds used for requests for the TX FIFO and RX FIFO are programmable through the DSI_VC_CTRL_i[19:17] DMA_TX_THRESHOLD and DSI_VC_CTRL_i[26:24] DMA_RX_THRESHOLD bit fields for TX FIFO and RX FIFO, respectively. DMA requests are asserted on the threshold value. The size of the space allocated in TX FIFO for each VC must be a multiple of the value of the DSI_VC_CTRL_i[19:17] DMA_TX_THRESHOLD bit field.

In the case of TX FIFO, if all the bytes defined by the word count field in the DSI_VC_LONG_PACKET_HEADER_i register are received, the DMA request is no longer asserted. Even during the last transfer, less than the DMA_TX_THRESHOLD number of bytes are received because the word count is not a multiple of the DMA_TX_THRESHOLD value.

In the case of RX FIFO, while the DMA request is used to transfer the data from the RX FIFO to the system memory, the sDMA must be programmed to read the exact number of received bytes in the FIFO. If users do not know the size of the received bytes, the direct access of the RX FIFO through the DSI_VC_SHORT_PACKET_HEADER_i register is performed until the DSI_VC_CTRL_i[20] RX_FIFO_NOT_EMPTY bit goes to 0.

The only exception is when the LP data transfer finishes and the threshold value is not reached. In this case, the DMA request is asserted. The drain of the FIFO is supported in that configuration to empty the FIFO even if the number of data received is not a multiple of the threshold value.

The use of each DMA request is programmable by software. The DSI_VC_CTRL_i[23:21] DMA_TX_REQ_NB bit field is dedicated to DMA request numbering for the TX FIFO. The DSI_VC_CTRL_i[29:27] DMA_RX_REQ_NB bit field is dedicated to DMA request numbering for the RX FIFO.

When the DMA request is used to indicate the number of 32-bit values ready in the RX FIFO that BTA has received from the peripheral, which indicates an end of the transfer from the peripheral to the host for a transfer to the system memory, the DMA request that corresponds to the VC ID is generated.

The sDMA transfers the number of 32-bit values defined in the threshold register or the exact number of bytes received from the peripheral (the user must know the number of expected received bytes to program the sDMA correctly). When the sDMA transfers a multiple number of threshold values, the DSI protocol engine sends 0s for the data when there is no more received data in the RX FIFO for the VC. Software users must parse the data and determine the valid bytes.

The size of the DMA transfer can be determined by reading the DSI_RX_FIFO_VC_FULLNESS register. The BTA interrupt (BTA_IRQ) must be used to know when to read the number of received bytes. The BTA interrupt must be monitored by reading the DSI_VC_IRQSTATUS_i[5] BTA_IRQ status bit. The DMA request must not be enabled until the sDMA is programmed with the correct number of data to read from RX FIFO.

This method must also be used when the RX FIFO space for the VC is expected to overflow because the expected number of data to be received is greater than the space allocated for the VC. Instead, the DMA request is asserted as soon as the threshold is reached or when BTA is received.

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When the DMA request is used to indicate the number of 33-bit entries empty in the TX FIFO for a transfer from the system memory, the DMA request corresponding to the VC ID is generated.

NOTE: For the most efficient transfer, the size of the request (read or write, single or burst) must be aligned with the threshold value.

Concurrent access using interlaced requests (read/write) to the TX and RX FIFO is supported for the same VC ID or different VC IDs.

10.3.4.4.3.3 Video + Command Mode

The two modes can be interlaced to send two DSI streams to two types of panels: video or command. The number of concurrent video streams is limited to one. The number of concurrent command mode streams is limited to four when there is no video stream, and three when there is a video stream.

- For DSI1, which has two video ports (see Section 10.3.4.4.5, *Video Port Interface*), it is possible to send video or command mode streams from DISPC to DSI1 primary video port (VP1), and a command stream on the secondary VP (VP2) for interleaving. In addition, it is also possible to send concurrently a command mode stream on the L3 Interconnect slave port for interleaving.
- For DSI2, which has one video port, it is possible to send a video stream or a command mode stream from DISPC to DSI2 primary VP (VP1). There is no secondary VP. Interleaving of command mode transfers is only possible through L3 Interconnect slave port.

10.3.4.4.3.4 Burst Mode

Frequency and transparent burst modes are supported:

- Frequency burst mode is used to reduce the HS period by increasing the clock frequency on the DSI link. In some cases, it reduces power consumption on the link. The non-HS period used typically to drive the main panel can be used to send data to the secondary panel or to allow feedback (acknowledge) from the primary and secondary panels. The DSI protocol engine must buffer a full line before sending the HS packets for the line. A double-buffering mechanism is required to send a line while the following one is being received on the video port. For more information about double-buffering, see Section 10.3.4.4.5.4, *Ping-Pong Buffer*.
- The transparent burst mode is used by increasing the pixel clock frequency generated by the DISPC with an increase of the horizontal blanking period.

10.3.4.4.3.5 Interleaving Mode

Video mode can output command mode packets, which are provided to DSI through the L3 interconnect, during the blanking periods of the video stream sequence on the PPI link. These command mode packets can be programmed as HS packets or low-power packets.

During a video stream sequence on the PPI link, four types of gap exist:

- BLLP gap: Blanking period during VSA, VBP, and VFP lines
- HSA gap: Blanking period during VACT lines; always between HS and HE short packet
- HBP gap: Blanking period during VACT lines; always between HS/HE short packet and data pixel long packet
- HFP gap: Blanking period during VACT lines; always between data pixel long packet and the end of the current VACT line

To perform interleaving in a particular gap, video mode must be set to go into LPS during the blanking gap. Each type of gap has separate configurable register bits that determine whether a blanking long packet will be sent or the link will go into LPS during the gap on the PPI link. If LPS is set during a gap, the DSI module performs interleaving during that period.

Two set of registers are available for:

- HS interleaving (when HS command mode packets must be sent during a video stream on the PPI link)

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- Low-power interleaving (when low-power command mode packets must be sent during a video stream on the PPI link)

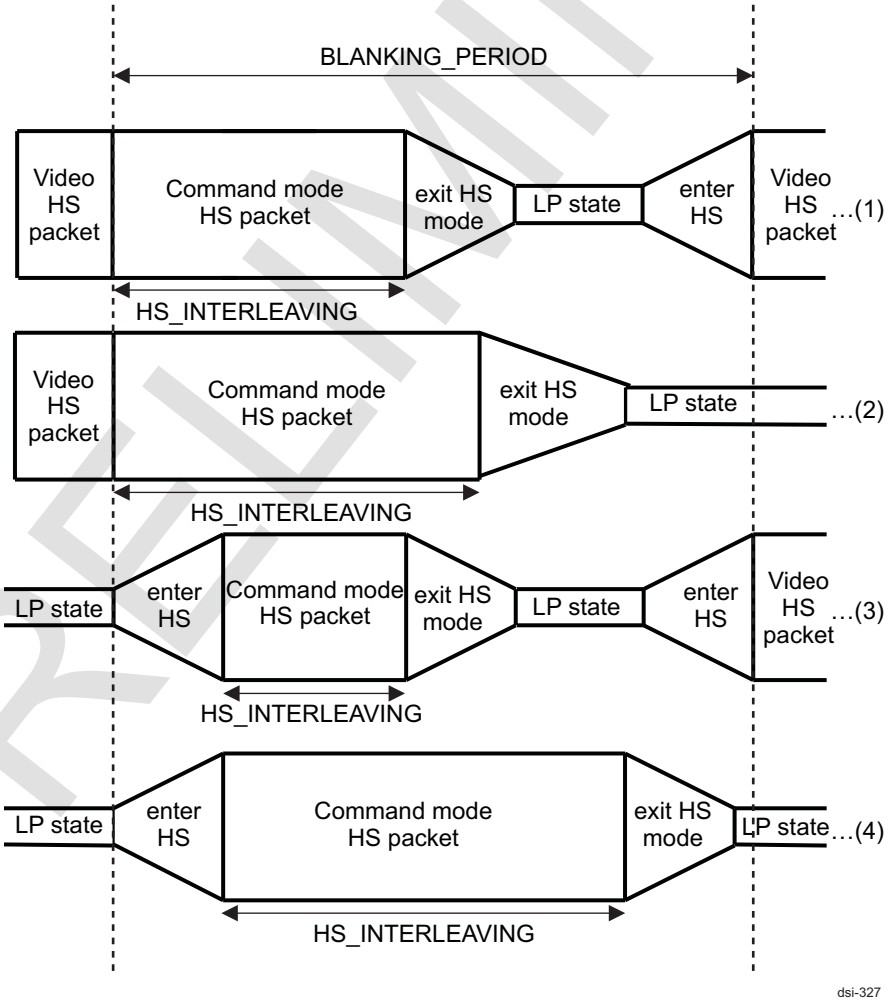
10.3.4.4.3.5.1 HS Command Mode Interleaving

Figure 10-126 shows the various HS mode scenarios in interleaving mode during a blanking gap. For each type of blanking gap, a dedicated bit field determines the number of TXBYTECLKHS clock cycles used for interleaving in HS command mode packets.

- The DSI_VM_TIMING6[31:16] BL_HS_INTERLEAVING bit field defines the number of TXBYTECLKHS clock cycles used to interleave HS command mode packets during a BLLP gap.
- The DSI_VM_TIMING4[7:0] HBP_HS_INTERLEAVING bit field defines the number of TXBYTECLKHS clock cycles used to interleave HS command mode packets during an HBP gap.
- The DSI_VM_TIMING4[15:8] HFP_HS_INTERLEAVING bit field defines the number of TXBYTECLKHS clock cycles used to interleave HS command mode packets during an HFP gap.
- The DSI_VM_TIMING4[23:16] HSA_HS_INTERLEAVING bit field defines the number of TXBYTECLKHS clock cycles used to interleave HS command mode packets during an HSA gap.

These programmable values must be programmed to satisfy the timings for the clock and data lane to enter and exit HS mode latency. According to the scenario, different equations must be considered when calculating the register values.

Figure 10-126. HS Command Mode Interleaving



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NOTE: For calculations and equations, the following abbreviations are used: EXIT_CLK_HS_MODE represents the exit HS mode latency for the clock lane. There is no dedicated register for this value but the programmer must know this value for further calculations:

$$EXIT_CLK_HS_MODE = T_{CLK\text{-}TRAIL} + TH_{S\text{-}EXIT}$$

NOTE: For more information about other timing parameters used in the following equations, see Section 10.3.4.4.4.1, *Timing Parameters for an LP to HS Transaction*, and Section 10.3.4.4.4.2, *Timing Parameters for an HS to LP Transaction*.

For the following equations, BLANKING_PERIOD represents the BLLP, HSA, HBP, or HFP blanking periods. The HS_INTERLEAVING period represents the maximal period HS command mode packets. Its value is set in the BL_HS_INTERLEAVING, HSA_HS_INTERLEAVING, HBP_HS_INTERLEAVING, or HFP_HS_INTERLEAVING bit fields, depending on the blanking type.

In each scenario, two calculations are present, depending on the value of the DSI_CLK_CTRL[13] DDR_CLK_ALWAYS_ON bit:

- DDR_CLK_ALWAYS_ON = 1: Clock lane is always active.
- DDR_CLK_ALWAYS_ON = 0: Clock lane is activated only when there are HS packets to be sent on the PPI link.

CAUTION

When the DDR_CLK_ALWAYS_ON bit is programmed to 1, the following must be considered:

- LP state can be achieved on the PPI link only if the data lane has enough time to go out from HS mode and enter a new HS mode during a period inside which the PPI link is meant to be in LP state.
- This can be expressed with the following equation:

  EXIT_HS_MODE_LATENCY + max{ENTER_HS_MODE_LATENCY, 2} + 1 ≤ BLANKING_PERIOD
- If the equation cannot be satisfied, because the LP state period is too short, software must program the DSI module in a way that during this blanking period a HS blanking packet is sent.

When the DDR_CLK_ALWAYS_ON bit is programmed to 0, the following must be considered:

- LP state can be achieved on the PPI link only if the data and clock lanes have enough time to go out from HS mode and enter a new HS mode during a period inside which the PPI link is meant to be in LP state.
- This can be expressed with the following equations:

  EXIT_HS_MODE_LATENCY + max{ENTER_HS_MODE_LATENCY, 2} + 1 ≤ BLANKING_PERIOD

  DDR_CLK_POST + EXIT_CLK_HS_MODE + DDR_CLK_PRE + ENTER_HS_MODE_LATENCY(data lane) + 1 ≤ BLANKING_PERIOD
- If both equations cannot be satisfied, because the LP state period is too short, software must program the DSI module in a way that during this blanking period a HS blanking packet is sent.

- Scenario 1: The gap for interleaving starts and ends with a regular video stream HS packet.
  - DDR_CLK_ALWAYS_ON = 1

    HS_INTERLEAVING = BLANKING_PERIOD – (EXIT_HS_MODE_LATENCY + max{ ENTER_HS_MODE_LATENCY, 2} + 1)
  - DDR_CLK_ALWAYS_ON = 0

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HS_INTER1 = BLANKING_PERIOD – (EXIT_HS_MODE_LATENCY + max{ ENTER_HS_MODE_LATENCY, 2} + 1)

HS_INTER2 = BLANKING_PERIOD – (DDR_CLK_POST + EXIT_CLK_HS_MODE + DDR_CLK_PRE+ ENTER_HS_MODE_LATENCY + 1)

HS_INTERLEAVING = min{HS_INTER1, HS_INTER2}

- Scenario 2: The gap for interleaving starts with a regular video stream HS packet and ends in LPS.
  - DDR_CLK_ALWAYS_ON = 1

    HS_INTERLEAVING = BLANKING_PERIOD – (EXIT_HS_MODE_LATENCY + 3)
  - DDR_CLK_ALWAYS_ON = 0

    HS_INTER1 = BLANKING_PERIOD – (EXIT_HS_MODE_LATENCY + 3)

    HS_INTER1 = BLANKING_PERIOD – (DDR_CLK_POST + EXIT_CLK_HS_MODE + 3)

    HS_INTERLEAVING = min{HS_INTER1, HS_INTER2}
- Scenario 3: The gap for interleaving starts with the LPS and ends with a regular video stream HS packet.
  - DDR_CLK_ALWAYS_ON = 1

    HS_INTERLEAVING = BLANKING_PERIOD – (ENTER_HS_MODE_LATENCY + EXIT_HS_MODE_LATENCY + max{ ENTER_HS_MODE_LATENCY, 2} + 1)
  - DDR_CLK_ALWAYS_ON = 0

    HS_INTER1 = BLANKING_PERIOD – (DDR_CLK_PRE + ENTER_HS_MODE_LATENCY + EXIT_HS_MODE_LATENCY + max{ENTER_HS_MODE_LATENCY, 2} + 1)

    HS_INTER2 = BLANKING_PERIOD – (DDR_CLK_PRE + ENTER_HS_MODE_LATENCY + DDR_CLK_POST + EXIT_CLK_HS_MODE + DDR_CLK_PRE+ ENTER_HS_MODE_LATENCY + 1)

    HS_INTERLEAVING = min{HS_INTER1, HS_INTER2})
- Scenario 4: The gap for interleaving starts with the LPS and ends with a regular video stream HS packet.
  - DDR_CLK_ALWAYS_ON = 1

    HS_INTERLEAVING = BLANKING_PERIOD – (ENTER_HS_MODE_LATENCY + EXIT_HS_MODE_LATENCY + 3)
  - DDR_CLK_ALWAYS_ON = 0

    HS_INTER1 = BLANKING_PERIOD – (DDR_CLK_PRE+ ENTER_HS_MODE_LATENCY + EXIT_HS_MODE_LATENCY + 3)

    HS_INTER2 = BLANKING_PERIOD – (DDR_CLK_PRE+ ENTER_HS_MODE_LATENCY + DDR_CLK_POST + EXIT_CLK_HS_MODE + 1)

    HS_INTERLEAVING = min{HS_INTER1, HS_INTER2}

10.3.4.4.3.5.2 LP Command Mode Interleaving

Figure 10-127 shows the various LP mode scenarios in interleaving mode during a blanking gap. For each type of blanking gap, a dedicated bit field determines the number of TXBYTECLKHS clock cycles used for interleaving in LP command mode packets.

- The DSI_VM_TIMING6[15:0] BL_LP_INTERLEAVING bit field defines the number of TXBYTECLKHS clock cycles used to interleave the HS command mode packets during a BLLP gap.
- The DSI_VM_TIMING5[7:0] HBP_LP_INTERLEAVING bit field defines the number of TXBYTECLKHS clock cycles used to interleave the HS command mode packets during an HBP gap.
- The DSI_VM_TIMING5[15:8] HFP_LP_INTERLEAVING bit field defines the number of TXBYTECLKHS clock cycles used to interleave HS command mode packets during an HFP gap.
- The DSI_VM_TIMING5[23:16] HSA_LP_INTERLEAVING bit field defines the number of TXBYTECLKHS clock cycles used to interleave HS command mode packets during an HSA gap.

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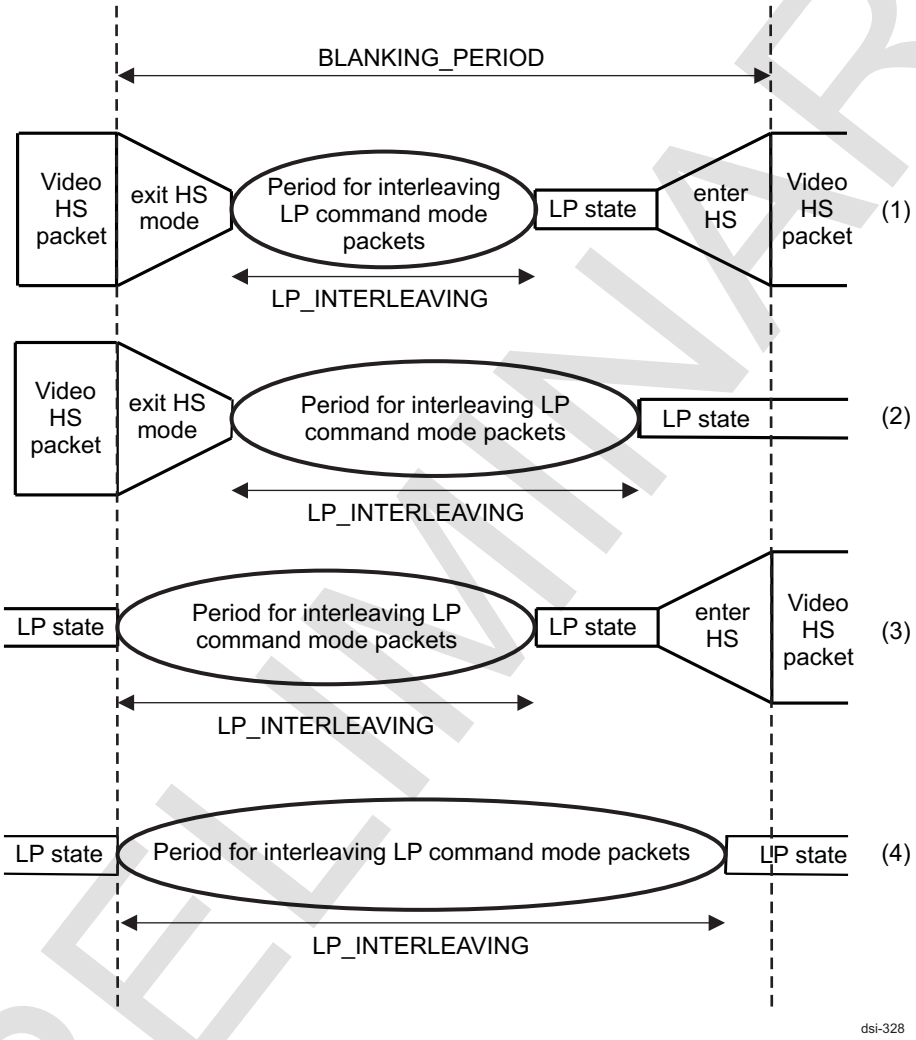
These values must be programmed to satisfy the timings for clock and data lane enter and exit LP mode latency. Clock lane timings do not affect LP command mode interleaving, because the clock lane can be controlled separately, compared with the data lane HS and low-power mutually exclusive control. Clock lanes can be in HS mode while the data lanes are in HS data transfer mode, low-power data transfer mode, or in LPS.

According to this scenario, different equations must be considered for calculating register values.

Figure 10-127. LP Command Mode Interleaving



For the following equations, BLANKING_PERIOD represents the BLLP, HSA, HBP, or HFP blanking periods. The LP_INTERLEAVING period represents the maximal period in LP command mode packets. Its value is set in the BL_LP_INTERLEAVING, HSA_LP_INTERLEAVING, HBP_LP_INTERLEAVING, or HFP_LP_INTERLEAVING bit fields, depending on the blanking type.

ALLOWED_HSBYTE_CLOCKS_FOR_LP represents the number of TXBYTECLKHS clock cycles during which LP interleaving can appear.

To calculate the LP_INTERLEAVING value:

1. Calculate how many TXBYTECLKHS clock cycles can be reserved for LP interleaving during the appropriate blanking video mode gap.
2. Calculate the value of LP_INTERLEAVING according to the results of Step 1.

Step 1:

- Scenario 1: The gap for interleaving starts and ends with a regular video stream HS packet.

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ALLOWED_HSBYTE_CLOCKS_FOR_LP = BLANKING_PERIOD – (EXIT_HS_MODE_LATENCY + max{ENTER_HS_MODE_LATENCY, 2} + 1)

- Scenario 2: The gap for interleaving starts with a regular video stream HS packet and ends in LPS.

  ALLOWED_HSBYTE_CLOCKS_FOR_LP = BLANKING_PERIOD – (EXIT_HS_MODE_LATENCY + 1)
- Scenario 3: The gap for interleaving starts with the LPS and ends with a regular video stream HS packet.

  ALLOWED_HSBYTE_CLOCKS_FOR_LP = BLANKING_PERIOD – (max{ENTER_HS_MODE_LATENCY, 2} + 1)
- Scenario 4: The gap for interleaving starts with the LPS and ends with a regular video stream HS packet.

  ALLOWED_HSBYTE_CLOCKS_FOR_LP = BLANKING_PERIOD – 1

After finishing Step 1, the time period available for LP interleaving is known:

$T_{lp_available}$ = ALLOWED_HSBYTE_CLOCKS_FOR_LP *T TXBYTECLKHS

Step 2:

The resulting value must be programmed in the appropriate video mode register for LP interleaving.

$$LP_INTERLEAVING < \left\lceil \frac{\frac{Tlp_available - 8*Thsbyte_clk - 5*Tdsif_clk}{Ttxclkesc}}{16} - 26 \right\rceil$$

dsi-E124

Thsbyte_clk: Period of TXBYTECLKHS clock of DSI_PHY module

Tdsif_clk: Period of DSI functional clock

Ttxclkesc: Period of LP transmit escape clock

10.3.4.4.4 Clock Requirements

The serial clock generated by the DSI host and sent to the display can be a continuous clock. The clock lane supports clock transmission even if there is no data to send for displays that require continuous clock. It is software-programmed through the DSI_CLK_CTRL[13] DDR_CLK_ALWAYS_ON bit: This bit can be programmed only when the interface is disabled (the DSI_CTRL[0] IF_EN bit set to 0).

The peripheral can use two different kinds of clocks. The first one is the DDR clock provided on the clock lane. The second clock is some transitions on the data lane 1 even if there is no valid data to send using LP mode.

The LP clock (TxClkEsc) frequency provided to the DSI complex I/O is in the range of 67 percent to 150 percent of the peripheral low-power (LP) clock frequency. It is generated internally by the DSI protocol engine module using the DSI functional clock. The DSI functional clock is divided by 1, 2, 3, up to 8191 using the value programmed in the DSI_CLK_CTRL[12:0] LP_CLK_DIVISOR bit field. The LP clock generated from the DSI functional clock must be in the range of 20 MHz to 32 kHz. The duty cycle must be 50/50 (minimum high time = 24ns). LP clock frequency visible on the pads (DP x or DN) is half the frequency of TxClkEsc.

The DSI_CLK_CTRL[20] LP_CLK_ENABLE bit is used to enable or disable the clock. When disabled, the value of the DSI_CLK_CTRL[12:0] LP_CLK_DIVISOR bit field is ignored and does not have to be programmed by software users.

10.3.4.4.4.1 Timing Parameters for an LP to HS Transaction

Figure 10-128 shows the timing requirement when switching the data and clock lane state from LP to HS.

lists the LP to HS timing parameters.

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Figure 10-128. LP to HS Timing

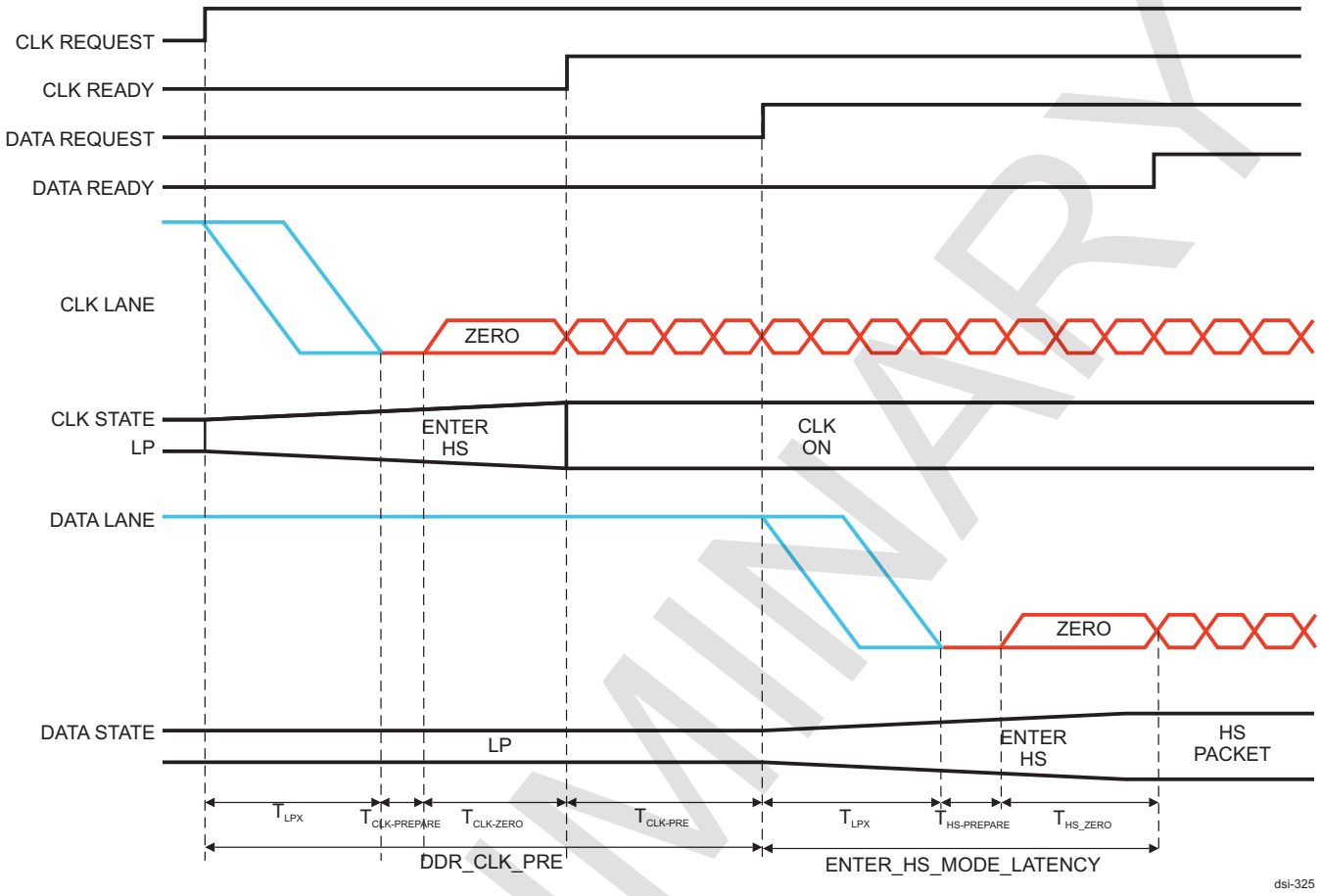

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Table 10-479. LP to HS Timing Parameters

Timings	Description	Registers/Associated Bit Fields	Register Settings	Timing Seen on the Line
T_{LPX}	Length of any low-power state period	DSI_PHY_REGISTER1[20:16] REG_TLPXBY2 The value set in this bit field is half of the T_{LPX}	CEIL (25 ns / DDR_Clock_Period)	CEIL (2 * REG_TLPXBY2/4) * 4 * DDR_Clock_Period
$T_{CLK-PREPARE}$	Time to drive the CLK lane to LP-00 state, to prepare for HS clock transmission	DSI_PHY_REGISTER2[7:0] REG_TCLKPREPARE	CEIL (65 ns / DDR_Clock_Period)	REG_TCLKPREPARE * DDR_Clock_Period + (~– 25 ns – +5 ns)
$T_{CLK-ZERO}$	Time to drive the CLK lane to HS-0 state, before starting the clock	DSI_PHY_REGISTER1[7:0] REG_TCLKZERO	CEIL (265 ns / DDR_Clock_Period)	{CEIL [(REG_TCLKZERO + 3)/4] * 4 + CEIL (REG_TCLKPREPARE/ 4) * 4 – REG_TCLKPREPARE + 2} * DDR_Clock_Period + (~ 0 ns – +5 ns)
$T_{CLK-PRE}$	Time that the HS clock must be driven before any associated data lane begins the transition from LP to HS mode	N/A	N/A	DDR_CLK_PRE - T_{LPX} - $T_{CLK-PREPARE}$ - $T_{CLK-ZERO}$
$T_{HS-PREPARE}$	Time to drive the data lane to LP-00 state, to prepare for HS packet transmission	DSI_PHY_REGISTER0[31:24] REG_THSPREPARE	CEIL (70 ns / DDR_Clock_Period) + 2	REG_THSPREPARE * DDR_Clock_Period + (–26.5 ns – + 4 ns)
$T_{HS-ZERO}$ + $T_{HS-PREPARE}$	$T_{HS-ZERO}$: Time to drive the data lane to HS-0 state before the synchronous sequence.	DSI_PHY_REGISTER0[23:16] REG_THSPRPR_THSZERO	CEIL (175 ns / DDR_Clock_Period) + 2	{CEIL [(N + 3)/4] * 4 + CEIL (M/4) * 4 + 3} * DDR_Clock_Period + (~ – 29 ns – 0 ns). Where N = REG_THSPREPARE_THSZERO – REG_THSPREPARE M = REG_THSPREPARE
DDR_CLK_PRE	Time between the CLK lane request assertion and the data request assertion to switch the data lanes to HS	DSI_CLK_TIMING[15:8] DDR_CLK_PRE	CEIL [(T_{LPX} + $T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$ + $T_{CLK-PRE}$) / TxByteClkHS] (1)(2)	
ENTER_HS_MODE_LATENCY (3)	Time to enter data lane into HS mode.	DSI_VM_TIMING7[31:16] ENTER_HS_MODE_LATENCY	CEIL [(T_{LPX} + $T_{HS-PREPARE}$ + $T_{HS-ZERO}$) / TxByteClkHS] (1)	

(1) The timings seen on the line should be used to determine the register value.
(2) See the MIPI D-PHY specification for the $T_{CLK-PRE}$ value.
(3) ENTER_HS_MODE_LATENCY timing applies only to video mode. It does not need to be programmed in command mode.

In the example in Table 10-480, the DDR clock = 400 MHz; TxByteClkHS = 100 MHz.

Table 10-480. LP to HS Timing Parameters Example for 400-MHz DDR Clock

Timings	Registers/Associated Bit Fields	Default Register Settings (Programmed at Reset)	Timing Seen on the Line
T_{LPX}	DSI_PHY_REGISTER1[20:16] REG_TLPXBY2	10	50 ns
$T_{CLK-PREPARE}$	DSI_PHY_REGISTER2[7:0] REG_TCLKPREPARE	26	40–70 ns

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Table 10-480. LP to HS Timing Parameters Example for 400-MHz DDR Clock (continued)

Timings	Registers/Associated Bit Fields	Default Register Settings (Programmed at Reset)	Timing Seen on the Line
$T_{CLK-ZERO}$	DSI_PHY_REGISTER1[7:0] REG_TCLKZERO	106	280–285 ns
$T_{CLK-PRE}$ (1)	N/A	N/A	80 ns
$T_{HS-PREPARE}$	DSI_PHY_REGISTER0[31:24] REG_THSPREPARE	30	48.5–79 ns
$T_{HS-ZERO}$	DSI_PHY_REGISTER0[23:16] REG_THSPRPR_THSZERO	72	178.5–207.5 ns
DDR_CLK_PRE	DSI_CLK_TIMING[15:8] DDR_CLK_PRE	45–49 (2)	450–490 ns
ENTER_HS_MODE_LATENCY	DSI_VM_TIMING7[31:16] ENTER_HS_MODE_LATENCY	24 * TxByteClkHS or 112 * DDR_CLOCK 34 * TxByteClkHS or 136 * DDR_CLOCK (2)	277–336.5 ns

(1) See the MIPI D-PHY specification for the $T_{CLK-PRE}$ value.
(2) Register setting calculated based on the values in the Timing Seen on the Line column.

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10.3.4.4.4.2 Timing Parameters for an HS to LP Transaction

Figure 10-129 shows the timing requirement when switching the state of the data and clock lanes from HS to LP. lists the HS to LP timing parameters.

Figure 10-129. HS to LP Timing

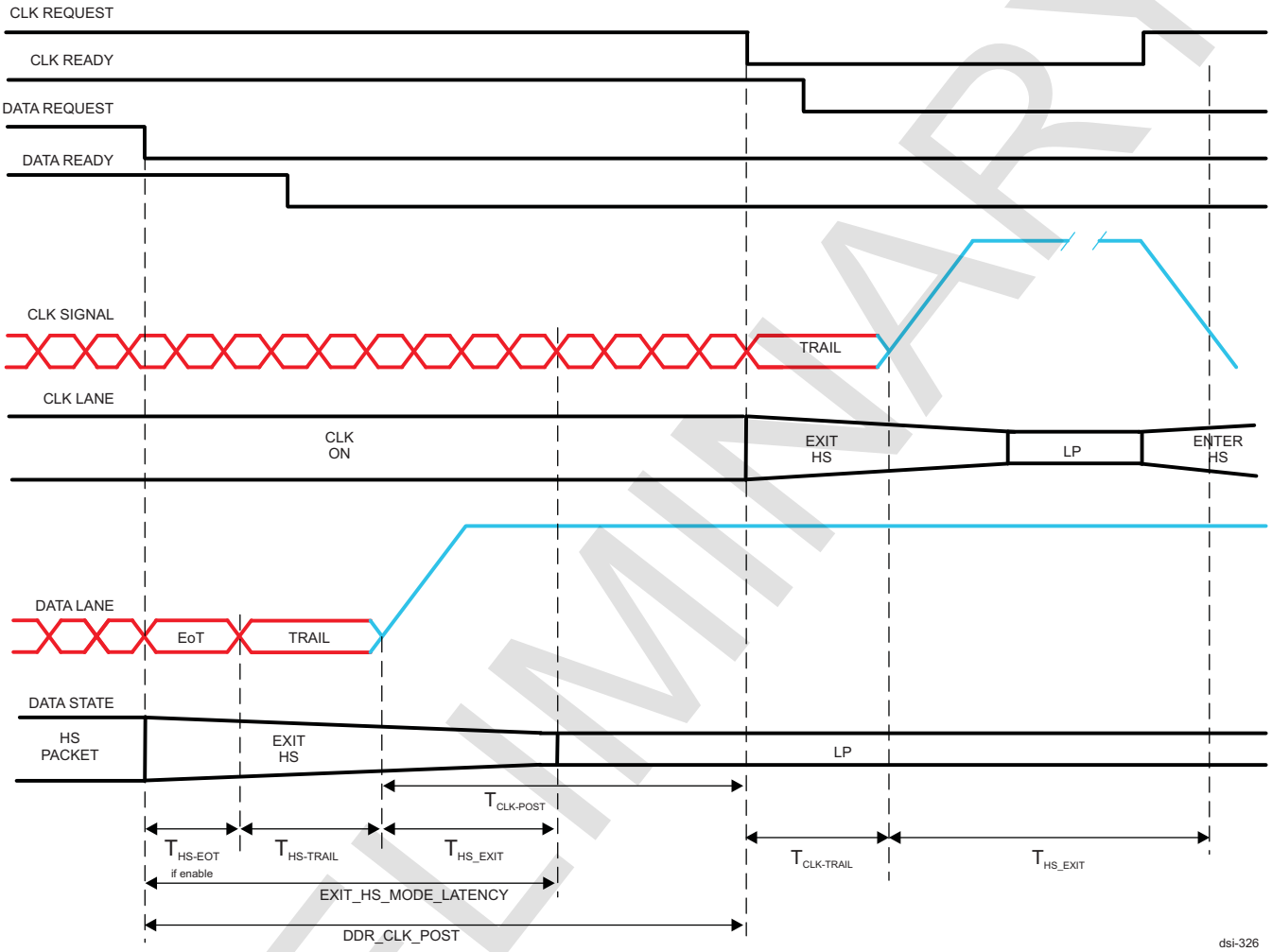

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Table 10-481. HS to LP Timing Parameters

Timings	Description	Registers/Associated Bit Fields	Register Settings	Timing Seen on the Line
T_{HS-EOT}	If EoT is enabled, a delay is added to EXIT_HS_MODE_LATENCY to send the EoT packet. The EoT period depends on the number of data lanes.	N/A	N/A	DIVROUNDUP (4, NB_DATA_LANES) Thus: One data lane = Four DDR clocks Two data lanes = Two DDR clocks
$T_{HS-TRAIL}$	Time to drive flipped differential state after last payload data bit of an HS transmission burst	DSI_PHY_REGISTER0[15:8] REG_THSTRAIL	CEIL (60 ns / DDR_Clock_Period) + 5	{CEIL [(REG_THSTRAIL + 3)/4] * 4 – 2.75} * DDR_Clock_Period + (~ 0 ns – 5 ns)
$T_{HS-EXIT}$	Time to drive data lane to LP-11 state, after HS burst	DSI_PHY_REGISTER0[7:0] REG_THSEXIT	CEIL (145 ns / DDR_Clock_Period)	[CEIL (REG_THSEXIT/4) * 4] * DDR_Clock_Period – (~ 3 ns – 45 ns)
$T_{CLK-POST}$	Time that the transmitter must continue sending HS clock after the last associated data lane has transitioned to LP mode	N/A	N/A	DDR_CLK_POST - T_{HS-EOT} (1) - $T_{HS-TRAIL}$
$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of an HS transmission burst	DSI_PHY_REGISTER1[15:8] REG_TCLKTRAIL	CEIL (60 ns / DDR_Clock_Period) + 2	{CEIL [(REG_TCLKTRAIL + 3)/4] * 4 – 1.5} * DDR_Clock_Period + (~ 0 ns – 5 ns)
DDR_CLK_POST	Time between the data lane request deassertion and the CLK request deassertion to switch the data lanes into LP mode. The DDR_CLK_POST value must follow the rule: DDR_CLK_POST ≥ $T_{HS-TRAIL}$ + T_{HS-EOT} + $T_{CLK-POST}$	DSI_CLK_TIMING[7:0] DDR_CLK_POST	CEIL [($T_{HS-TRAIL}$ + T_{HS-EOT} (1) + $T_{CLK-POST}$) / TxByteClkHS] (2) (3)	
EXIT_HS_MODE_LATENCY (4)	Time to exit HS mode	DSI_VM_TIMING7[15:0] EXIT_HS_MODE_LATENCY	CEIL [($T_{HS-TRAIL}$ + $T_{HS-EXIT}$ + T_{HS-EOT} (1)) / TxByteClkHS] (2)	

(1) If T_{HS-EOT} is enabled
(2) The timings seen on the line should be used to determine the register value.
(3) See the MIPI D-PHY specification for the$T_{CLK-POST}$ value.
(4) EXIT_HS_MODE_LATENCY timing applies only to video mode. It does not need to be programmed in command mode.

In the example in Table 10-482, the DDR clock = 400 MHz; TxByteClkHS = 100 MHz; two data lanes.

Table 10-482. HS to LP Timing Parameters Example for 400-MHz DDR Clock and Two Data Lanes

Timings	Registers/Associated Bit Fields	Default Register Settings (Programmed at Reset)	Timing Seen on the Line (T_{HS-EOT} Enabled)	Timing Seen on the Line (T_{HS-EOT} Disabled)
T_{HS-EOT}	N/A	N/A	5 ns	N/A
$T_{HS-TRAIL}$	DSI_PHY_REGISTER0[15:8] REG_THSTRAIL	29	73.125–78.125 ns	73.125–78.125 ns

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Table 10-482. HS to LP Timing Parameters Example for 400-MHz DDR Clock and Two Data Lanes (continued)

Timings	Registers/Associated Bit Fields	Default Register Settings (Programmed at Reset)	Timing Seen on the Line (T_{HS-EOT} Enabled)	Timing Seen on the Line (T_{HS-EOT} Disabled)
$T_{HS-EXIT}$	DSI_PHY_REGISTER0[7:0] REG_THSEXIT	58	105–147 ns	105–147 ns
$T_{CLK-POST}$ (1)	N/A	N/A	585 ns	580 ns
$T_{CLK-TRAIL}$	DSI_PHY_REGISTER1[15:8] REG_TCLKTRAIL	26	76.25–81.25 ns	76.25–81.25 ns
DDR_CLK_POST	DSI_CLK_TIMING[7:0] DDR_CLK_POST	66 * TxByteClkHS or 264 * DDR_CLOCK	658.125–663.125 ns	653.125–658.125 ns
		67 * TxByteClkHS or 268 * DDR_CLOCK (2)		
EXIT_HS_MODE_LATENCY	DSI_VM_TIMING7[15:0] EXIT_HS_MODE_LATENCY	19 * TxByteClkHS or 76 * DDR_CLOCK	183.125–230.125 ns	178.125–225.125 ns
		24 * TxByteClkHS or 96 * DDR_CLOCK (2)		

(1) See the MIPI D-PHY specification.
(2) Register setting calculated based on the values in Timing Seen on the Line (T_{HS-EOT} Enabled) column.

10.3.4.4.4.3 Extra LP Transitions

Some DSI receivers require extra clock cycles in LP mode to process the data. The DSI protocol engine can be programmed to send automatically one NULL long packet. It applies only when no more data are ready to be sent from the internal FIFO to the peripheral on the last LS transfer. The same value is used for all the VCs sending packets in LS mode.

The size of the payload is defined by the DSI_CLK_CTRL[17:16] LP_CLK_NULL_PACKET_SIZE bit field. The header value depends on the size of the payload as described in Table 10-483 and Table 10-484.

NOTE: In Table 10-483 and Table 10-484, ECC and checksum are enabled.

Table 10-483. Extra NULL PH

VC ID	Payload size (DSI_CLK_CTRL[17:16] LP_CLK_NULL_PACKET_SIZE)	Header (1st Byte)	Header (2nd Byte): WC LSB	Header (3rd Byte): WC MSB	Header (ECC)
0x0	0	0x9	0x0	0x0	0x9
	1		0x1		0x13
	2		0x2		0x2F
	3		0x3		0x35
0x1	0	0x49	0x0		0x1F
	1		0x1		0x05
	2		0x2		0x39
	3		0x3		0x23
0x2	0	0x89	0x0		0x10
	1		0x1		0x0A
	2		0x2		0x36
	3		0x3		0x2C
0x3	0	0xC9	0x0		0x06
	1		0x1		0x1C
	2		0x2		0x20

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Table 10-483. Extra NULL PH (continued)

VC ID	Payload size (DSI_CLK_CTRL[17:16] LP_CLK_NULL_ PACKET_SIZE)	Header (1st Byte)	Header (2nd Byte): WC LSB	Header (3rd Byte): WC MSB	Header (ECC)
	3		0x3		0x3A

Table 10-484. Extra NULL Packet Payload

Payload size (DSI_CLK_CTRL[17:16] LP_CLK_NULL_PACKET_ SIZE)	Payload (1st byte)	Payload (2nd byte)	Payload (3rd byte)	Payload (CRC) LSB	Payload (CRC) MSB
0	NA(1)	NA	NA	0xFF	0xFF
1	0	NA	NA	0x87	0x0F
2	0	0	NA	0xB8	0xF0
3	0	0	0	0x33	0x39

(1) N/A = Not available

10.3.4.4.5 Video Port Interface

NOTE: The signals described in this section are internal and not bounded outside the device. This section describes the internal connections between the DISPC and the DSI protocol engine.

Table 10-485 and Table 10-486 summarize the video interface signals.

- DSI1 has two video ports (VP1 and VP2):
  - VP1 is connected to the LCD1 output of DISPC.
  - VP2 is connected to the LCD2 output of DISPC.
- DSI2 has one video port (VP1):
  - VP1 is connected to the LCD2 output of DISPC.

These interfaces are used to connect the DISPC outputs to the DSI protocol engine to send real-time data streams. For video mode, only the active matrix timings are supported by DSI protocol engine.

When the two video ports of DSI1 are used for two video mode transfers, only the synchronization signals on video port 1 are used by the DSI protocol engine. The synchronization signals on video port 2 are ignored. When only one video mode is enabled, it must be connected to video port 1. It is not possible to enable video mode on video port 2 without enabling video mode on video 1 (dual-video mode).The HSYNC/VSYNC/DE/DATA signals are driven on the rising or falling edge of the pixel clock (VP_PCLK).

Table 10-485. Video Port 1 Signals for DSI1 and DSI2 Protocol Engines

Signal Name	Type (1)	Description
VP1_HSYNC	I	Horizontal synchronization signal
VP1_VSYNC	I	Vertical synchronization signal
VP1_DATA[23:0]	I	Parallel output data: Bits 0 to 23
VP1_PCLK	I	Pixel clock. In case of STALL configuration, it is used to indicate when new data is on the data bus during the clock period of VP1_CLK. The VP1_PCLK is generated from VP1_CLK through division inside the DISPC. The clock ratio is indicated in the DSI_CTRL[4] VP_CLK_RATIO bit and must be aligned with the configuration of the clock divisor in the display controller (DISPC_DIVISOR1[7:0] PCD bit field for DISPC LCD1 output, and the DISPC_DIVISOR2[7:0] PCD bit field for DISPC LCD2 output). The source of the VP1_PCLK for DSI1 is the LCD1_PCLK. The source of the VP1_PCLK for DSI2 is LCD2_PCLK. For more information, see Section 10.2.4.1, *Clock Configuration*, and Section 10.3.4.2, *DSI Clock Configuration*.

(1) I = Input; O = Output

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Table 10-485. Video Port 1 Signals for DSI1 and DSI2 Protocol Engines (continued)

Signal Name	Type [1]	Description
VP1_DE	I	Data enable
VP1_STALL	O	The stall signal must be deasserted to receive pixel and asserted to stop receiving pixel. (It can be used only while the DISPC is configured in STALL mode; in that mode, HSYNC and VSYNC are not generated).
VP1_CLK	I	DISPC internal clock. It is a free-running clock. The source of VP1_CLK for DSI1 is LCD1_CLK, divided down. The source of VP1_CLK for DSI2 is LCD2_CLK, divided down. For more information, see Section 10.2.4.1, *Clock Configuration*, and Section 10.3.4.2, *DSI Clock Configuration.*

Table 10-486. Video Port 2 Signals for DSI1 Protocol Engine

Signal Name	Type [1]	Description
VP2_HSYNC	I	Horizontal synchronization signal
VP2_VSYNC	I	Vertical synchronization signal
VP2_DATA[23:0]	I	Parallel output data: Bits 0 to 23
VP2_PCLK	I	Pixel clock. In case of STALL configuration, it is used to indicate when new data is on the data bus during the clock period of VP2_CLK. The VP2_PCLK is generated from VP2_CLK through division inside the DISPC. The clock ratio is indicated in the DSI_CTRL2[4] VP_CLK_RATIO bit and must be aligned with the configuration of the clock divisor in the display controller (DISPC_DIVISOR2[7:0] PCD bit field for DISPC LCD2 output). The source of the VP2_PCLK for DSI1 is LCD2_PCLK. For more information, see Section 10.2.4.1, *Clock Configuration*, and Section 10.3.4.2, *DSI Clock Configuration.*
VP2_DE	I	Data enable
VP2_STALL	O	The stall signal must be deasserted to receive pixel and asserted to stop receiving pixel. (It can be used only while the DISPC is configured in STALL mode; in that mode, HSYNC and VSYNC are not generated).
VP2_CLK	I	DISPC internal clock. It is a free-running clock. The source of the VP2_CLK for DSI1 is LCD2_CLK, divided down. For more information, see Section 10.2.4.1, *Clock Configuration*, and Section 10.3.4.2, *DSI Clock Configuration.*.

[1] I = Input; O = Output

NOTE:

- The polarities of VP_HSYNC and VP_VSYNC are programmable by setting the DSI_CTRL and DSI_CTRL2 registers.
- Clocks VP_CLK and VP_PCLK can have the same frequency.
- The number of bits to be captured on the video port (the width of the data bus) is defined in the DSI_CTRL[7:6] VP_DATA_BUS_WIDTH bit field for DSI1 and the DSI_CTRL2[7:6] VP_DATA_BUS_WIDTH for DSI2. The supported formats are 16, 18, and 24 bits.
- For the 18-bit pixel format using 24 bits on the DSI link, the format to be used by the DSI protocol engine is 24-bit because the DISPC must convert the 18-bit pixels into 24-bit pixels. There is no logic inside the DSI protocol engine to convert from 18-bit format to 24-bit format.

The data received on the video port can be stored in the line buffer memories or sent directly on the DSI interface in two cases:

- The line buffer size is too small compared to the line from the DISPC.
- There is no line buffer instantiated. If there is no line buffer, the burst mode, defined as frequency burst mode, cannot be used. Only transparency burst mode is supported.

NOTE: The DSI_CTRL[13:12] LINE_BUFFER and DSI_CTRL2[13:12] LINE_BUFFER bit fields define the number of lines to be used for transferring data from the video port to the DSI1and DSI2 link.

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10.3.4.4.5.1 Video Port Used for Video Mode

If the video port is used for video mode, VP_STALL is not used. Table 10-487 and Table 10-488 list the active signals on the video port.

Table 10-487. Video Port 1 for DSI1 and DSI2 in the Context of Video Mode

Signal Name	Type (1)	Description
VP1_HSYNC	I	Horizontal synchronization signal
VP1_VSYNC	I	Vertical synchronization signal
VP1_DATA[23:0]	I	Parallel output data: Bits 0 to 23
VP1_PCLK	I	Pixel clock
VP1_DE	I	Data enable
VP1_CLK	I	It is a free-running clock used as the DISPC functional clock.

(1) I = Input; O = Output

Table 10-488. Video Port 2 for DSI1 in the Context of Video Mode

Signal Name	Type (1)	Description
VP2_HSYNC	I	Horizontal synchronization signal
VP2_VSYNC	I	Vertical synchronization signal
VP2_DATA[23:0]	I	Parallel output data: Bits 0 to 23
VP2_PCLK	I	Pixel clock
VP2_DE	I	Data enable
VP2_CLK	I	It is a free-running clock used as the DISPC functional clock.

(1) I = Input; O = Output

Three video modes are available:

- No-line buffer: The data received on the video port are directly outputted to the DSI port without buffering. The ratio of VP_PCLK and the DSI HS clock period must ensure the same throughput on the two ports (the two clocks must be generated using the same PLL; the subsystem must provide this configuration).
- One-line buffer:
  - The data can be transferred as described in the no-line buffer configuration.
  - The data are first stored in the line buffer; and then when all the data for one line are received, the DSI protocol engine sends the entire line. Software must adjust timings to let enough time for storing all line data into the line buffer before sending to DSI outputs. The synchronization packets are never stored in the line buffer.
- Two-line buffers:
  - The data can be transferred as described in the one-line buffer configuration.
  - One line is stored when the second line is output on the DSI port. This allows burst capability. While receiving the first line of the frame, no RGB packets are sent, because the line buffers are empty. To send the last line of the frame, a dummy line must be provided by the display controller to flush the line buffers. The synchronization packets are never stored in the line buffer.

NOTE: If more active lines are received on the video port than the number of lines defined in the DSI_VM_TIMING3[15:0] VACT bit field, the extra lines are discarded by the DSI protocol engine. These lines are treated as blanking lines.

Figure 10-130 through Figure 10-132 show these three video modes.

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Figure 10-130. DSI Video Mode Without Burst (No-Line Buffer)

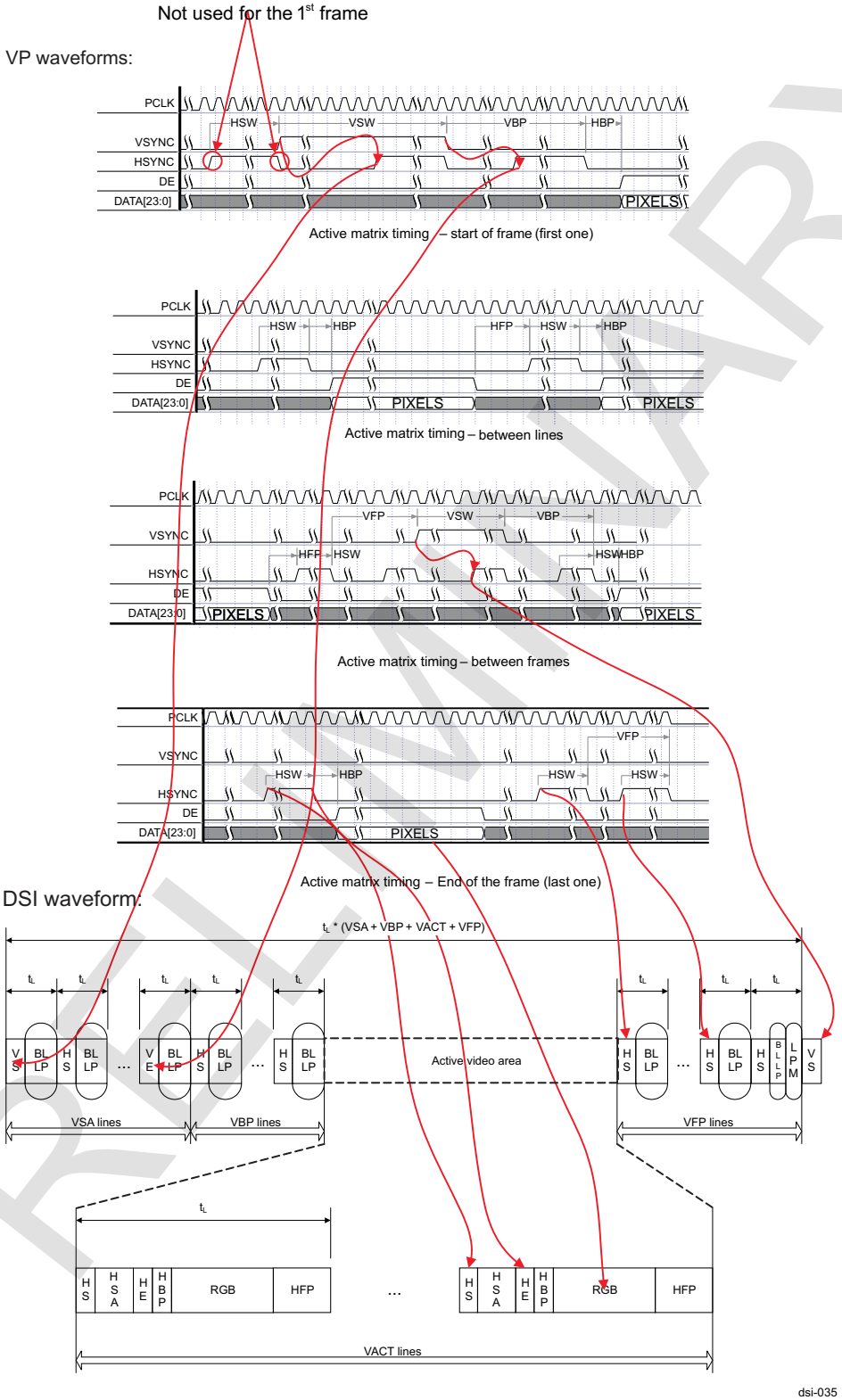

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Figure 10-131. DSI Video Mode Without Burst (One-Line Buffer)

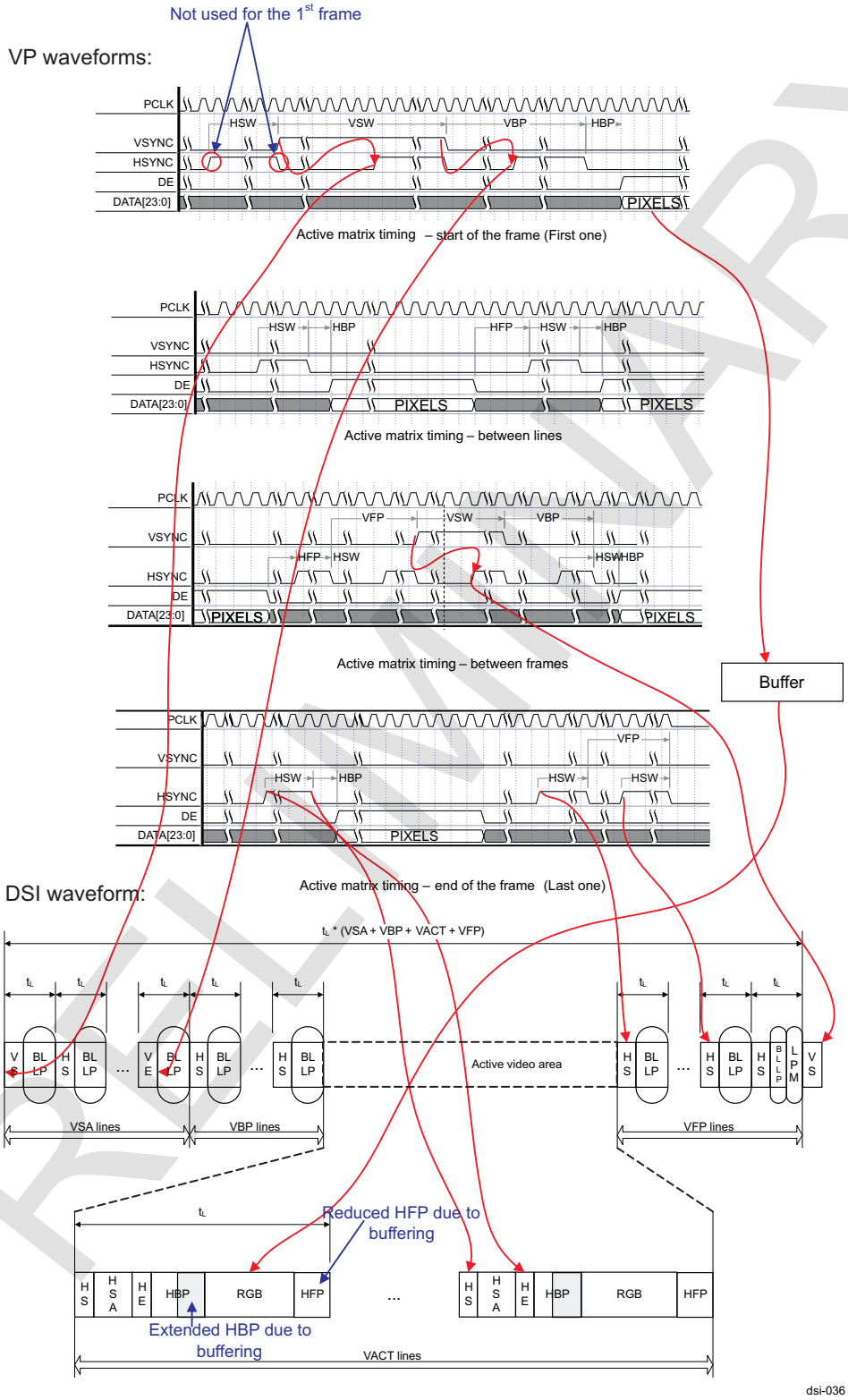

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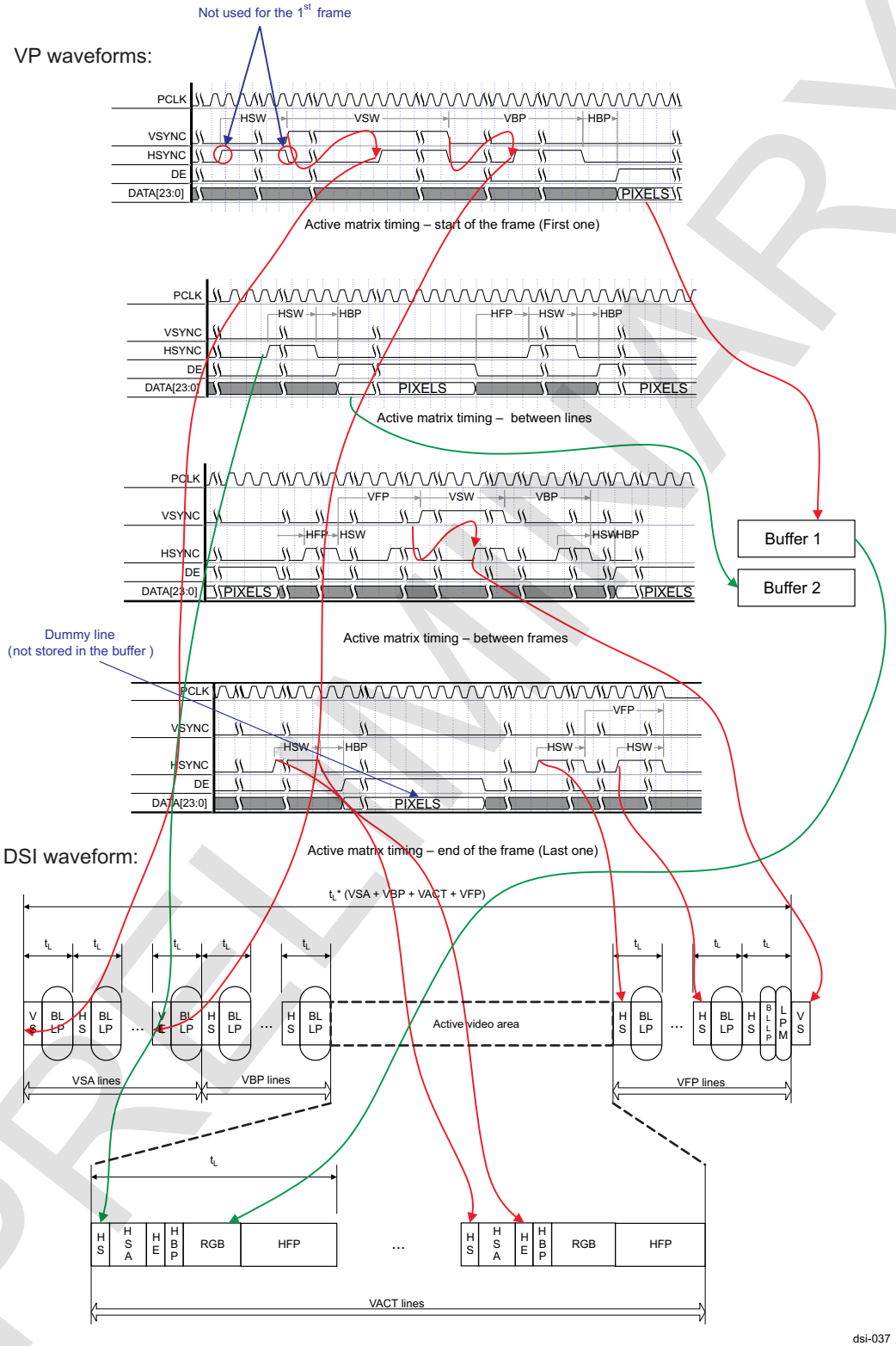
Figure 10-132. DSI Video Mode With Burst (Two-Line Buffers)



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NOTE: In Figure 10-130 through Figure 10-132:

- When HSyNC start and HSYNC end short packets are not generated (HSA does not exist), the HBP signal must not be 0.
- Software must ensure that VBP is always defined so that there is at least one HSYNC during VBP.
- In blanking low-power mode (BL-LP), two options are possible:
  - The lane remains in ULPS, and the DSI_CTRL[20] BLANKING_MODE bit is set to 0x0.
  - Dummy bytes are sent during LP with the DSI_CTRL[20] BLANKING_MODE bit set to 0x1; the number of sent bytes is determined by the DSI_VM_TIMING6[15:0] BL_LP_INTERLEAVING bit field.

If the signal VP_DE is not asserted during enough VP_PCLK cycles to be able to capture the number of bytes defined in the word count of the header, the module must send the valid data received on the video port followed by bytes of 0s to match the required number of bytes to transmit. The VP_PCLK must be present during all extra cycles where the DSI protocol engine is expecting pixels.

If the VP_DE signal is asserted for too many VP_PCLK cycles, the module stops capturing the data on the video port while the number of bytes to capture, as defined in the word count field of the header, is reached.

The HS checks that the received synchronization events on the video port (VSYNC and HSYNC) are within the synchronization window based on expected timings. If the timings (internal and received) are out of sync, the interrupt for out-of-sync is generated and the interface is disabled (the DSI_CTRL[0] IF_EN bit is automatically reset by hardware). The unsynchronization window is defined by the DSI_VM_TIMING2[27:24] WINDOW_SYNC bit field.

10.3.4.4.5.2 Video Port Used for Command Mode

If the video port is used for command mode, the VP_HSYNC, VP_VSYNC, and VP_DE signals are not used. Table 10-489 and Table 10-490 describe the active signals on video port 1 and video port 2, respectively .

Table 10-489. Video Port 1 for DSI1 and DSI2 in the Context of Command Mode

Signal Name	Type (1)	Description
VP1_DATA[23:0]	I	Parallel output data: Bits 0 to 23
VP1_PCLK	I	One pulse is generated every time new data is output on the data bus.
VP1_STALL	O	The stall signal must be deasserted to receive pixel and asserted to stop receiving pixel. (It can be used only while the DISPC is configured in stall mode; in that mode, HSYNC and VSYNC are not generated).
VP1_CLK	I	DISPC internal clock: It is a free-running clock used as the DISPC functional clock.

(1) I = Input; O = Output

Table 10-490. Video Port 2 for DSI1 in the Context of Command Mode

Signal Name	Type (1)	Description
VP2_DATA[23:0]	I	Parallel output data: Bits 0 to 23
VP2_PCLK	I	One pulse is generated every time new data is output on the data bus.
VP2_STALL	O	The stall signal must be deasserted to receive pixel and asserted to stop receiving pixel. (It can be used only while the DISPC is configured in stall mode; in that mode, HSYNC and VSYNC are not generated).
VP2_CLK	I	DISPC internal clock: It is a free running-clock used as the DISPC functional clock.

(1) I = Input; O = Output

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NOTE: The stall signal must be deasserted to receive pixels and asserted to stop receiving pixels.

Figure 10-133 and Figure 10-134 show the VP_STALL signal assertion and deassertion on rising and falling edges, respectively.

Figure 10-133. Stall Timing With Pixel on Rising Edge

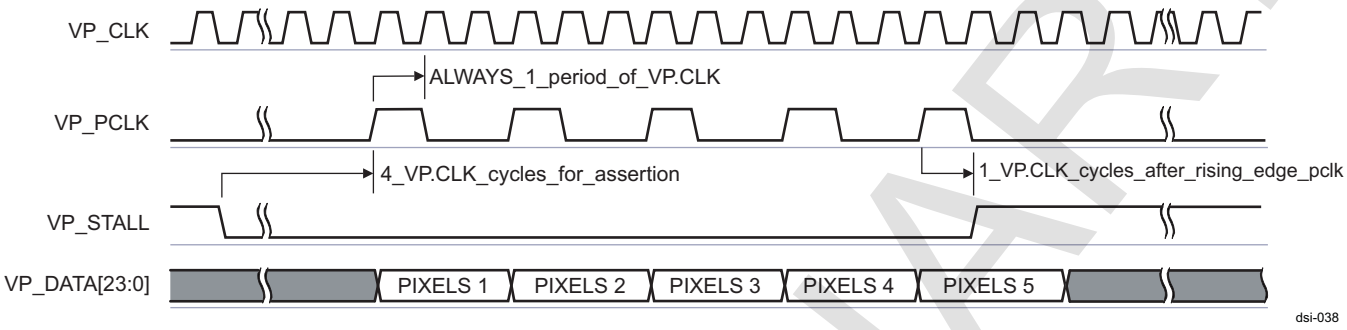
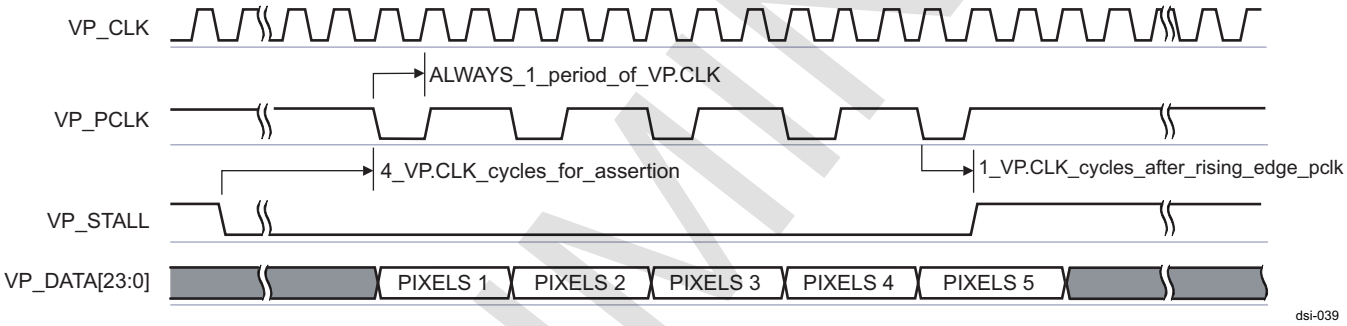


Figure 10-134. Stall Timing With Pixel on Falling Edge



The VP_STALL signal is asserted to stop the transfer when the last data is output. The data can be output on the rising or falling edge of the VP_PCLK through registers in the DISPC module. Data output on the falling edge of VP_PCLK is supported by the DSI protocol engine.

The VP_PCLK clock is generated from VP_CLK; these two clocks are balanced. Assertion and deassertion of VP_PCLK is done on the rising edge of VP_CLK. The width of the VP_PCLK pulse depends on the configuration of the clock divisor in the DISPC. For more information, see Section 10.2, *Display Controller*. In the DSI protocol engine, the information is defined in the DSI_CTRL[4] VP_CLK_RATIO bit and must be aligned with the DISPC configuration.

Deassertion of the VP_STALL signal occurs at least four VP_CLK cycles before assertion of VP_PCLK. Assertion of VP_STALL occurs one cycle VP_CLK after deassertion of VP_PCLK for the last pixel to be transferred. The VP_CLK clock is generated by the DISPC under software control. It can be kept running between assertion and deassertion of VP_STALL.

The stall assertion/deassertion depends on the number of bytes to be received considering the size of the video port bus defined in the DSI_CTRL[7:6] VP_DATA_BUS_WIDTH bit field for video port 1 and the DSI_CTRL2[7:6] VP_DATA_BUS_WIDTH bit field for video port 2.

Figure 10-135 shows the data flow in command mode using the video port.

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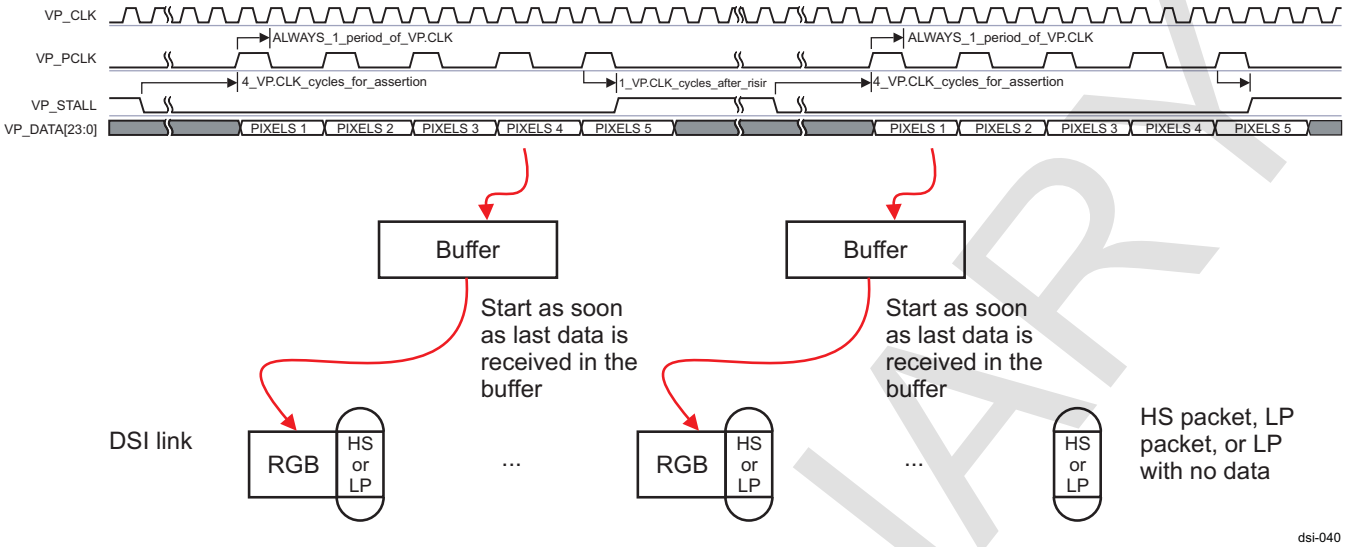
Figure 10-135. Data Flow in Command Mode Using the Video Port



Two command modes are available:

- One-line buffer: The data are stored in the line buffer before being sent.
- Two-line buffers: The two lines are used if the word count defined in the DSI_VC_LONG_PACKET_HEADER_i register is bigger than the line size; otherwise, one-line buffer must be used.

NOTE: In command mode, the video port can be used only in one- or two-line buffer configuration. No-line buffer configuration is not allowed.

The packets can be sent using high speed or low speed.

The DCS command in the payload can be inserted automatically using the DSI_VC_CTRL_i[30] DCS_CMD_ENABLE bit. If TE is used, hardware automatically inserts the DCS Write Start command for the first packet of the frame transfer and DCS Write Continue command for all subsequent packets. The DSI_VC_CTRL_i[31] DCS_CMD_CODE bit is ignored.

10.3.4.4.5.3 Burst Mode

When burst mode is enabled, the video port receives data from the DISPC at the pixel clock. The DSI protocol engine buffers the data in its own line FIFO (double-line buffer size). The read speed of the line can be twice the pixel clock to increase the blanking time of the video mode and to allow command mode traffic to be interleaved during the blanking period. Burst mode uses a dual-line buffer.

The DSI port can output data from one line buffer while the second line buffer is accessed by the video port. The two processes are concurrent but they do not access the same line at the same time. The DSI transfer can start only when the entire video port line is transferred into a line buffer. The switch is controlled by the VP_HS signal on the video port side and by an internal signal on the DSI port indicating that the last data for the current line has been written into the line buffer.

NOTE: The line buffers are used to store only the pixels. The synchronization codes are not stored in the line buffers; they must be sent according to the video port timings.

NOTE: The number of line buffers to be used while receiving data on the video port can be selected by setting the DSI_CTRL[13:12] LINE_BUFFER bit field.

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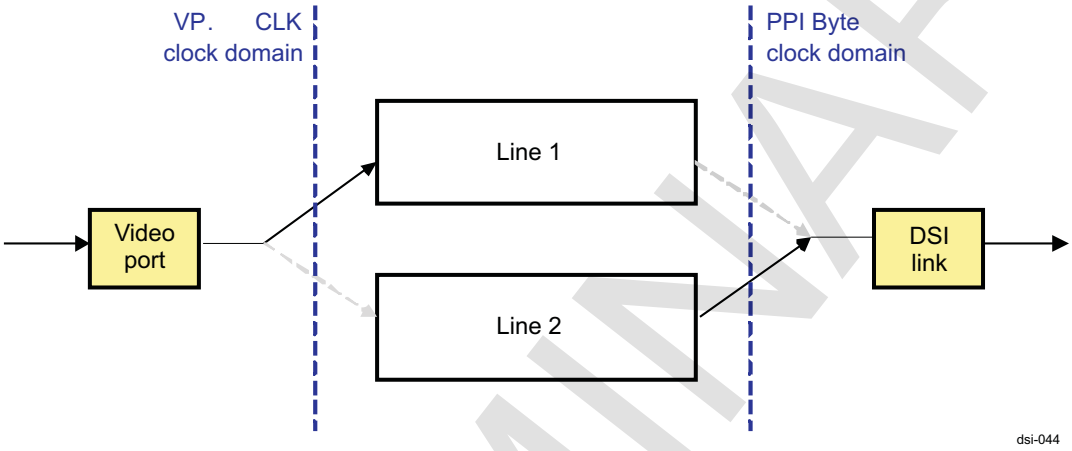
10.3.4.4.5.4 Ping-Pong Buffer

The ping-pong buffer stores data incoming from the DISPC in one of the two line buffers. When one line buffer is used to store the pixels received on the video port, the second line buffer is used to provide data on the DSI link. The ping-pong buffer is supported in command mode, provided the size of the packet defined in the header register is less than the size of each line buffer (768 x 32 bits for VP1of DSI2 and VP2 of DSI1, and 960 x 32bits for VP1 of DSI1). If the size of the packet is greater than the size of the line buffer, the ping-pong mechanism cannot be used (both lines are used as a single line).

Figure 10-136 shows the video port used in ping-pong mode .

Figure 10-136. Ping-Pong Mode



The ping-pong buffer status can be checked by the DSI_VC_CTRL_i[14] PP_BUSY bit.

- When PP_BUSY equals 1, the ping-pong buffer is active and the line buffers are not ready to receive data; therefore, the a new header cannot be updated.
- When PP_BUSY equals 0, at least one line buffer is empty; therefore, a new header can be updated. PP_BUSY is then set to 0x1. If both line buffers are empty, two headers can be written, one following the other. PP_BUSY remains at 0x0 after the first header is written, and is set to 0x1 after second header is written.

An IRQ is available to update header on events. The IRQ is enabled by setting the DSI_VC_IRQENABLE_i[8] PP_BUSY_CHANGE_IRQ bit to 0x1, and its status is accessible on the DSI_VC_IRQSTATUS_i[8] PP_BUSY_CHANGE_IRQ bit.

10.3.4.4.6 SCP Interface

The SCP interface is used to transfer register values from the DSI protocol engine to the DSI PLL control module and to the DSI complex I/O. It spends several cycles to serialize the data to be sent. Software users must consider the delay in processing the transfer of the data from/to the L3 Interconnect slave port to/from the module.

10.3.4.4.6.1 Shadowing Register

The first three SCP registers for the DSI complex I/O address map must be implemented as shadow registers. The shadowing mechanism is enabled and disabled using the DSI_COMPLEXIO_CFG1[31] SHADOWING bit:

- When setting the DSI_COMPLEXIO_CFG1[31] SHADOWING bit to 1, the transfer of the values from the three first local interconnect port registers into the three first registers of the DSI complex I/O (DSI_PHY_REGISTER0 through DSI_PHY_REGISTER2) is done only when the DISPC_UPDATE_SYNC signal from the DISPC is active and the DSI_COMPLEXIO_CFG1[30] GOBIT bit is set to 1. If there is no pending update for the three registers when the DISPC_UPDATE_SYNC signal is asserted, the DSI_COMPLEXIO_CFG1[30] GOBIT bit is reset by hardware and there is no SCP transfer.
  - If there is only one register to update, only the corresponding new value is transferred. The second

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and third registers in the DSI complex I/O are not updated. When the transfer completes, the DSI_COMPLEXIO_CFG1[30] GOBIT bit is reset by hardware.

– If the two registers need to be updated, the register with the lower address is transferred first, followed by the second register. When the transfers complete, the DSI_COMPLEXIO_CFG1[30] GOBIT bit is reset by hardware.

– If the three registers need to be updated, the register with the lowest address is transferred first, and then the other registers are transferred according to incremental address. When the transfers complete, the GOBIT bit is reset by hardware.

When there is an on-going transfer (read or write) to any SCP register, the transfer must complete before updating the shadowing registers.

- When unsetting the DSI_COMPLEXIO_CFG1[31] SHADOWING bit to 0, if the transfer into the first two DSI complex I/O registers has already started, it should be finished.

NOTE: When reading the shadow registers, the local value stored in the DSI protocol engine is returned if the update is pending; otherwise, the values stored in the DSI complex I/O are returned.

10.3.4.4.6.2 Busy Signal

The SCPBusy signal indicates there is still activity using the SCPClk clock provided by the PRCM module. The SCPClk clock is the devided DSS_L3_ICLK/4 clock.

10.3.4.4.7 Timers

NOTE: Among the timers described in this section, only the HS TX, LP RX, and TurnRequests timers generate interrupts immediately when the timer value is null. The ForceTxStopMode timer ends counting instantly and ForceTxStopMode is not asserted.

10.3.4.4.7.1 T_{wakeup} Timer

The T_{WakeUp} timer is not implemented in the DSI protocol engine. The general-purpose (GP) timer must be used to handle wakeup. This timer is used for exiting ULP status mode for the active lanes (clock and/or data lanes). The sequence to exit ULP state is:

1. Change the state of TxULPSExit for each lane to ACTIVE.
2. Wait for the interrupt that indicates all lanes with TxULPSExit ACTIVE have acknowledged by asserting ULPSActiveNot. This is done by reading the DSI_COMPLEXIO_IRQSTATUS register - ULPSACTIVENOT_ALLi_IRQ bit fields (where i = 0, 1).
3. Start the application wake-up timer (GP timer).
4. Wait for the time-out.
5. Change the TxUlpsClk signals to INACTIVE state for the clock lane and/or TxRequestEsc INACTIVE state for the data lane(s).

NOTE: The minimum time for the wake-up period is 1 ms.

To enter ULPS mode for clock lane, TxUlpsClk state must be changed to ACTIVE state. To enter ULPS mode for data lane, TxRequestEsc state must be changed to ACTIVE state (also TxUlpsEsc, if it is not in ACTIVE state already).

10.3.4.4.7.2 ForceTxStopMode FSM

The ForceTxStopMode signal is used at initialization time (DSI complex I/O). Figure 10-137 shows the ForceTxStopMode finite state-machine (FSM) to assert and deassert the ForceTxStopMode signal.

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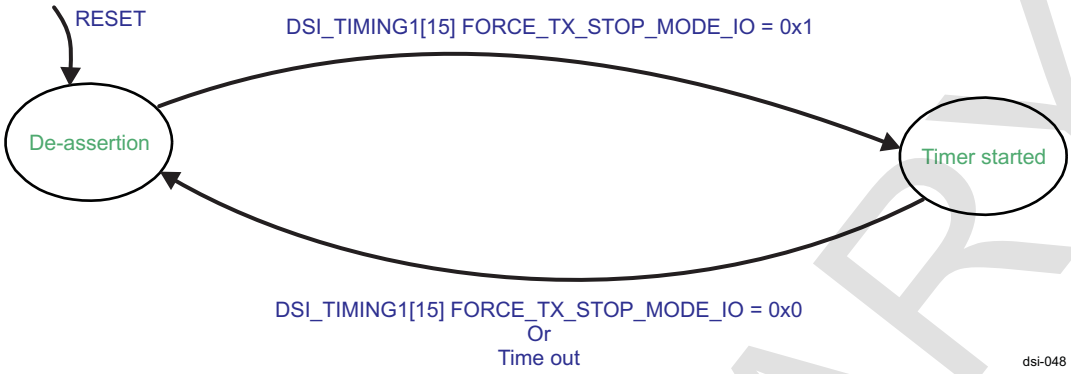
Figure 10-137. ForceTxStopMode FSM



The DSI protocol engine asserts the ForceTxStopMode signal by setting the DSI_TIMING1[15] FORCE_TX_STOP_MODE_IO bit to 1. Asserting the FORCE_TX_STOP_MODE_IO bit allows the lanes to be initialized. The lanes are in STOP state when the ForceTxStopMode signal is high.

No data can be sent before the ForceTxStopMode signal is deasserted. The deassertion time is defined by the STOP_STATE_COUNTER_IO, STOP_STATE_X4_IO and STOP_STATE_X16_IO bit fields in DSI_TIMING1[14:0] register. The DSI_TIMING1[15:0] FORCE_TX_STOP_MODE_IO bit is reset by hardware when the time is reached.

This bit can be reset by software.

The calculation of the number of DSI_CLK functional clock cycles assertion period is defined by:

Total period in DSI_FCLK cycles = STOP_STATE_COUNTER_IO x ((STOP_STATE_X16_IO x 15) + 1) x ((STOP_STATE_X4_IO x 3)).

10.3.4.4.7.3 TurnRequest FSM

The TurnRequest signal is used to request a turnaround. It is valid only for the data lane 1 because the other data lanes cannot be used in reverse direction to receive data from the DSI receiver. When the TurnRequest signal is asserted, the TA_TO timer is started. Figure 10-138 shows the TurnRequest FSM to assert and deassert the TurnRequest signal.

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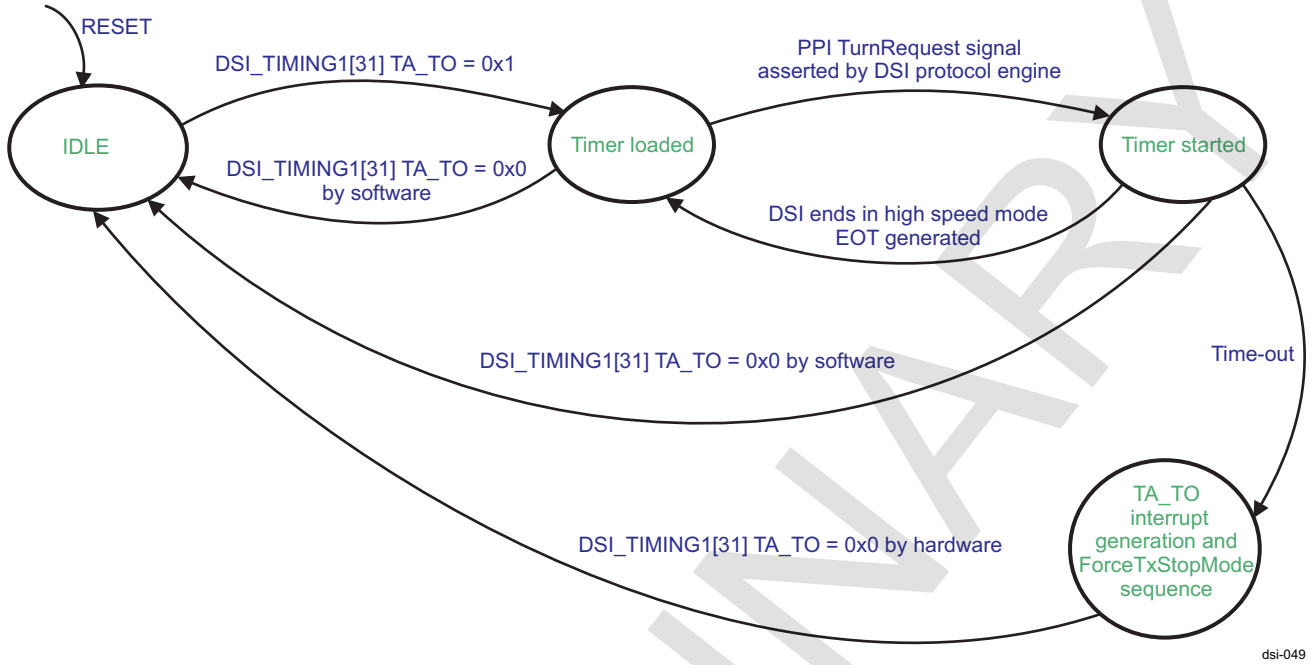
Figure 10-138. TurnRequest FSM



The DSI protocol engine asserts the TurnRequest signal during one TxClkEsc cycle when turnaround is enabled through the DSI_VC_CTRL_i[6] BTA_EN bit (for more information, see Section 10.3.4.4.8, *Bus Turnaround*). The DSI_TIMING1[31] TA_TO bit is set/reset by software to enable or disable the timer for turnaround procedure failure. It can be reset by software or automatically by hardware when the time-out occurs.

The timer is loaded with the value in the number of DSI_FCLK cycles:

DSI_TIMING1[28:16] TA_TO_COUNTER x ((DSI_TIMING1[30] TA_TO_X16 x 15) + 1) x ((DSI_TIMING1[29] TA_TO_X8 x 7) + 1).

When the TA_TO_IRQ interrupt is generated (the turnaround timer expired and the procedure failed), hardware automatically resets the DSI_TIMING1[31] TA_TO bit and asserts the ForceTXStopMode signal (see Section 10.3.4.4.7.2, *ForceTxStopMode FSM*) for the DSI_PHY to drive the LP-11 STOP state. The ForceTXStopMode timer is used to define the minimum duration of the LP-11 state. The STOP state can be longer if there is no activity.

Hardware resets the DSI_TIMING1[15] FORCE_TX_STOP_MODE_IO bit , followed by an internal logic reset except for all register values and TX FIFO content, and then resets the DSI_CTRL[0] IF_EN bit. Software must take action to recover (for example, by resetting the peripheral if it is not responding). It must wait for the DSI_CTRL[0] IF_EN bit to be reset to 0 before starting the recovery sequence.

10.3.4.4.7.4 Peripheral Reset Timer

The peripheral reset timer is not implemented in the DSI protocol engine module. Instead, a GP timer must be used in case of reset of the peripheral to determine when the peripheral is ready to operate again.

10.3.4.4.7.5 HS TX Timer

The HS TX timer is used to detect when the host has been in TX mode for too long. When time-out occurs, the EOT is forced. The timer is reloaded when a start of HS transmission occurs. It is enabled and disabled by software through the DSI_TIMING2[31] HS_TX_TO bit. The interrupt HS_TX_TO_IRQ is generated when the timer expires. The DSI_IRQSTATUS[14] HS_TX_TO_IRQ bit is set to 1 when the HS TX time-out occurs.

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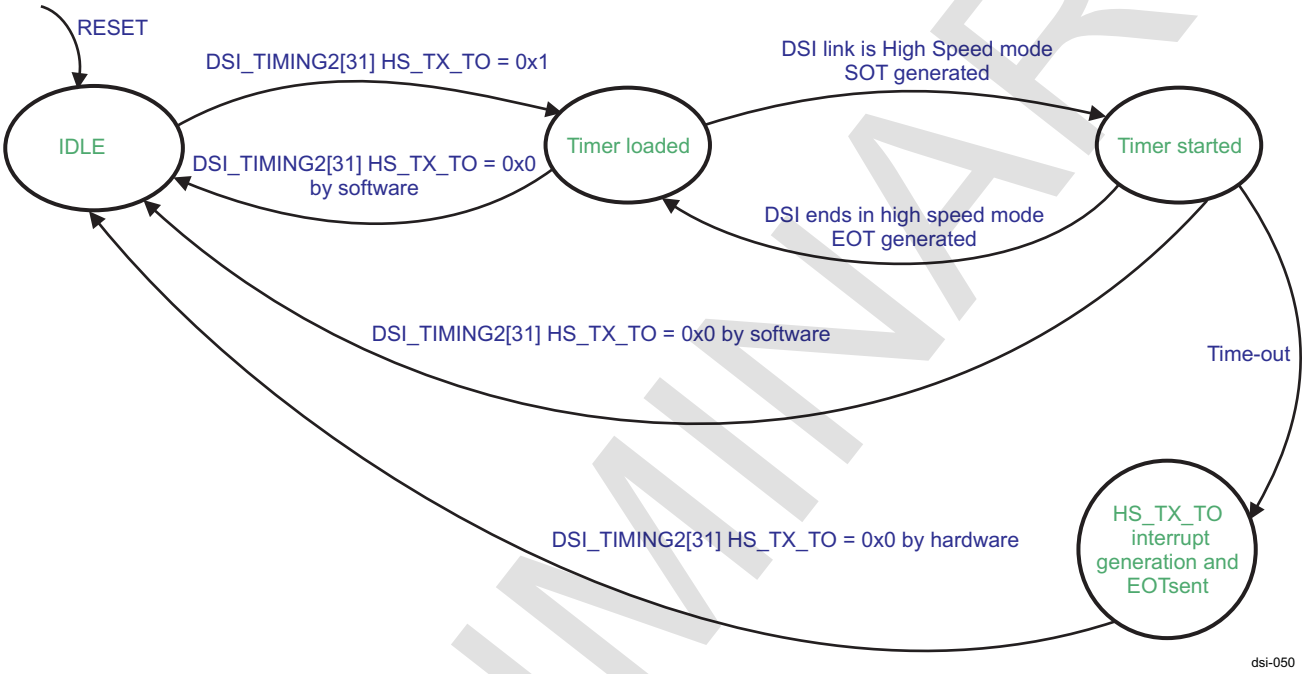
The maximum time supported is 20 ms. It can be used to determine that at least once per frame in video mode, the HS mode is stopped to enter ULPS.

The timer is loaded with the value in the number of TXBYTECLKHS:

DSI_TIMING2[28:16] HS_TX_TO_COUNTER x (1 + (DSI_TIMING2[30] HS_TX_TO_X64 x 63) x (1 + (DSI_TIMING2[29] HS_TX_TO_X16 x15))

Figure 10-139 shows the HS TX timer FSM.

Figure 10-139. HS TX Timer FSM



When the time-out occurs, hardware sends an EOT request for the DSI complex I/O to drive LP-11 STOP state. This is followed by the generation of the interrupt. Hardware performs an internal logic reset including the TX FIFO content but excluding the register values, and then resets the DSI_CTRL[0] IF_EN bit.

Software must take action to recover (for example, by resetting the peripheral if it is not responding). It must wait for the DSI_CTRL[0] IF_EN bit to be reset to 0 before taking any recovery action.

10.3.4.4.7.6 LP RX Timer

When the host is in low-power receive mode after a BTA, the LP RX timer is loaded. When the timer expires, the host requests the DSI complex I/O to drive LP-11. The interrupt LP_RX_TO_IRQ is generated when the timer expires. The DSI_IRQSTATUS[15] LP_RX_TO_IRQ bit is set to 1 when the LP RX time-out occurs.

The DSI_TIMING2[15] LP_RX_TO bit is set/reset by software to enable or disable the timer.

The timer is loaded with the value in the number of DSI_CLK functional clock cycles:

DSI_TIMING2[12:0] LP_RX_TO_COUNTER x ((DSI_TIMING2[14] LP_RX_TO_X16 x 15) + 1) x ((DSI_TIMING2[13] LP_RX_TO_X4 x 3) + 1)

Figure 10-140 shows the LP RX timer FSM.

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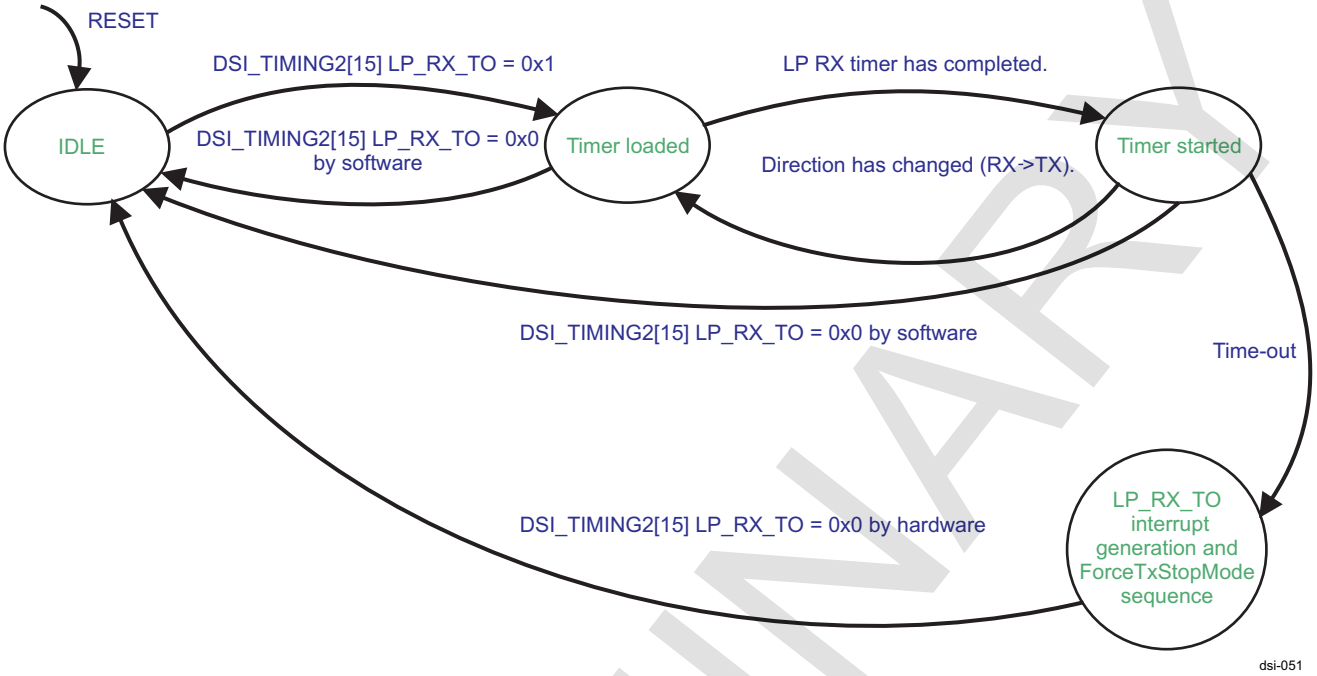
Figure 10-140. LP RX Timer FSM



When the interrupt is generated, hardware automatically resets the DSI_TIMING2[15] LP_RX_TO bit and then asserts ForceTXStopMode for the DSI complex I/O to drive LP-11 STOP state. The ForceTXStopMode timer is used to define the minimum duration of the LP-11 state. The STOP state can be longer if there is no activity.

Hardware resets the ForceTXStopMode bit, followed by an internal logic reset except for all register values and TX FIFO content, and then resets the DSI_CTRL[0] IF_EN bit. Software must take action to recover (for example, by resetting the peripheral if it is not responding). It must wait for the DSI_TIMING1[15] FORCE_TX_STOP_MODE_IO and DSI_CTRL[0] IF_EN bits to be reset before starting the recovery sequence. The TX FIFO is not flushed (the FIFO is flushed only when DSI_VC_CTRL_i[0] VC_EN is set to 1).

10.3.4.4.8 Bus Turnaround

The bus turnaround (BTA) is not automatically sent by default after each packet is sent to the panel(s). It is programmable independently for each VC ID. BTA generation can be enabled when the DSI_VC_CTRL_i[6] BTA_EN bit is set to 1 by software. Software must ensure that when the BTA is sent to the peripheral, enough time is allocated for the response and for the BTA from the peripheral to the host. For more information about possible DSI PHY timing adjustments during the turnaround procedure, see Section 10.3.4.6.5.3, *Turnaround Request in Transmit Mode*, and Section 10.3.4.6.5.4, *Turnaround Request in Receive Mode*.

When setting the DSI_VC_CTRL_i[6] BTA_EN bit to 1, one BTA is sent manually to the peripheral. This manual mode can be used for packets in command or video mode.

Acknowledgment from the peripheral for successful BTA is indicated by asserting the BTA_IRQ interrupt, if it is enabled in the DSI_VC_IRQENABLE_i[5] BTA_IRQ_EN bit. To monitor the BTA interrupt, the user must read the DSI_VC_IRQSTATUS_i[5] BTA_IRQ status bit.

CAUTION

The BTA should be sent when the RX FIFO is empty. Users must empty the RX FIFO before sending BTA to the peripheral to ensure that when receiving new data from the peripheral, the allocated spaces for all the VCs are empty.

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In automatic mode, the BTA is sent automatically at the end of short or long packet transmission, if the DSI_VC_CTRL_i[2] BTA_SHORT_EN or DSI_VC_CTRL_i[3] BTA_LONG_EN bit is set to 1.

Two modes can be used for each VC ID:

- Automatic: After each packet, a BTA is sent. To determine the size of the long packet, the protocol engine on the host side reads the word count defined in the header (in the DSI_VC_LONG_PACKET_HEADER_i register) and uses it to determine the last data to be sent on the DSI link. For short packets, the size is always 4 bytes. The BTA is then sent to the peripheral. The word count is also used to determine how many bytes are to be transferred from the 32-bit write access to the payload register (DSI_VC_LONG_PACKET_PAYLOAD_i).
- Manual:
  - Data transfer through L3 interconnect: When transferring data using the L3 interconnect port, while all data have been provided to the DSI protocol engine, users can select the BTA for the last packet provided to the L3 interconnect port only by setting the DSI_VC_CTRL_i[6] BTA_EN bit, or for the last packets and the following ones by setting automatic mode.
  - Data transfer through video port: In the case of data transfer using the video port, the DSI_VC_CTRL_i[6] BTA_EN bit can be selected at any time during the transfer of the packet.
- For video mode packets (data and synchronization events), it is not possible to determine when the BTA is sent; therefore, it is highly recommended to use manual BTA mode only in command mode. It is possible, however, to use the BTA for a VC in video mode.

  For data provided on the video port, an interrupt for end of packet transfer PACKET_SENT_IRQ is provided to indicate when the packet is completely sent by the DSI complex I/O. PACKET_SENT_IRQ can be monitored in the DSI_VC_IRQSTATUS_i[2] PACKET_SENT_IRQ status bit. The BTA is available even if the space allocated in the TX FIFO for the corresponding VC is empty. It must be sent later even if no packet was sent before the BTA request. The DSI_VC_CTRL_i[6] BTA_EN bit must be reset if the BTA request was sent, even if automatic mode for this specific type of packets is enabled.

The BTA is supported for video and command mode packets. It is not possible to send the BTA during the blanking periods of video mode when HS blanking packets should be sent; that is, when one of the following bits is set to 1:

- DSI_CTRL[20] BLANKING_MODE
- DSI_CTRL[21] HFP_BLANKING_MODE
- DSI_CTRL[22] HBP_BLANKING_MODE
- DSI_CTRL[23] HSA_BLANKING_MODE

Therefore, in video mode, the BTA request is delayed until there is a blanking period without HS blanking packets.

When the TurnRequest signal is asserted (always only for data lane 1), the TA_TO timer is started. If the direction signal is not changed according to the turnaround request, the TA_TO interrupt is generated. When the direction signal is in output mode, any data on the input data bus is ignored because the DSI is in transmission mode (data and triggers must be ignored). For more information about the TA_TO timer, see Section 10.3.4.4.7.3, *TurnRequest FSM*.

10.3.4.4.9 PHY Triggers

The DSI protocol engine uses three triggers that are supported only for data lane 1:

- Reset trigger from host to display
- Tearing effect (TE) trigger from display to host
- Acknowledge trigger from display to host

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CAUTION

Each trigger is associated with a dedicated user-configurable receive or transmit pattern, which is loaded in the DSI_PHY_REGISTER3 or DSI_PHY_REGISTER4 bit fields. The default (reset) values of the bit fields are aligned with the *MIPI D-PHY Specification v1.0* . If any of these values need to be changed, the following must be considered:

- If any of the bit fields is written with a nondefault value, the other bit fields in the same register must also be configured with different values. This is to ensure that two different trigger bit fields are not programmed with the same pattern.
- If two or more bit fields are written with equal values, unpredictable behavior of the DSI PHY module may occur.

10.3.4.4.9.1 Reset

The DSI protocol engine can use one of the triggers of the DSI_PHY to send a reset to the display. The reset trigger pattern is configurable through the DSI_PHY_REGISTER3[31:24] REG_TXTRIGGERESC3 bit field. To send the reset pattern to the peripheral, the DSI_CTRL[5] TRIGGER_RESET bit must be set to 1. When software requires the trigger reset pattern to be sent, the DSI protocol engine resets its own logic, but not the registers. Software can select between two reset modes:

- Immediate reset: All pending requests in TX FIFO not already considered for transfer scheduling, the RX FIFO requests, and the data from video port are ignored. Only the current transfer on the DSI link and those already scheduled are transmitted. All the other transfers are discarded.
- Synchronized reset: The mode is valid only if there is VC using the video mode and if it is active. The principle is to wait for the current video frame to be transferred on the link. Any data on the video port after the current frame are ignored.

To select reset mode, the DSI_CTRL[14] TRIGGER_RESET_MODE bit must be programmed.

CAUTION

For both reset modes, the DSI protocol engine flushes the FIFOs, synchronization buffers, and line buffers before resetting the DSI_CTRL[0] IF_EN bit.

10.3.4.4.9.2 Tearing Effect

TE on the display is avoided by having synchronization information from the display. It is used only in command mode and is not functional in video mode.

There are two types of TE triggers:

- DSI PHY TE trigger
- CMOS TE line (one of the two input signals can be selected for the TE trigger of a VC; the signal is asynchronous).

Software must set and send the appropriate sequence to receive the TE trigger pattern from the peripheral on the DSI link, or use the CMOS TE line. The value of the expected TE trigger pattern can be configured through the DSI_PHY_REGISTER4[23:16] REG_RXTRIGGERESC2 bit field.

When the TE PHY trigger pattern is received, the DSI protocol engine generates the TE_TRIGGER_IRQ interrupt with a TE event, if the interrupt is enabled. To enable the interrupt, the DSI_IRQENABLE[16] TE_TRIGGER_IRQ_EN bit must be set to 1. The DSI_IRQSTATUS[16] TE_TRIGGER_IRQ status bit indicates whether the interrupt event has been generated.

When using the TE CMOS signal, the DSI protocol engine generates the TE0_LINE or TE1_LINE interrupt, if it is enabled, depending on which line is used. One or multiple VCs can be synchronized using the same TE line. Both lines can be active at the same time for different VCs.

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The DSI_VC_TE_i[30] TE_EN bit must be set and the DSI_VC_TE_i[29] TE_LINE bit must be reset to indicate that hardware must use the TE PHY trigger to start the transfer of the data from the related VC. TE_EN is reset when all the data are sent to the peripheral.

The DSI_VC_TE_i[30] TE_EN, DSI_VC_TE_i[29] TE_LINE, and DSI_VC_TE_i[28] TE_LINE_NB bits must be set to select between the TE0 and TE1 line to indicate that hardware must use the TE0 line or TE1 line to start the transfer of the data from the related VC. The bits are reset when all the data are sent to the peripheral.

The DSI_TE_VSYNC_WIDTH_j, DSI_TE_HSYNC_WIDTH_j, and DSI_TE_HSYNC_NUMBER_j registers indicate which mode is used to detect the start of the transfer:

- If DSI_TE_HSYNC_NUMBER_j[10:0] LINE_NUMBER = 0, DSI_TE_HSYNC_WIDTH is ignored. When a pulse on the TE line is detected to be wider than the DSI_TE_VSYNC_WIDTH_j[19:8] MIN_VSYNC_PULSE_WIDTH bit field, data transfer starts from the protocol engine to the peripheral at the falling edge of the TE CMOS line.
- If the DSI_TE_HSYNC_NUMBER_j[10:0] LINE_NUMBER bit field is greater than 0, DSI_TE_HSYNC_WIDTH_j is used. The DSI protocol engine waits until it detects a pulse wider than the DSI_TE_VSYNC_WIDTH_j[19:8] MIN_VSYNC_PULSE_WIDTH bit field, and then counts each pulse wider than DSI_TE_HSYNC_WIDTH_j[19:8] MIN_HSYNC_PULSE_WIDTH but smaller than DSI_TE_VSYNC_WIDTH_j[19:8] MIN_VSYNC_PULSE_WIDTH. When the number of HSYNC pulses is reached, data transfer from the DSI protocol engine to the peripheral starts. In case the number of HSYNC pulses is not reached due to a new VSYNC pulse being detected, the counter of HSYNC pulses restarts from 0.

NOTE: DSI_TE_HSYNC_WIDTH_j[19:8] MIN_HSYNC_PULSE_WIDTH is always programmed with a value smaller than DSI_TE_VSYNC_WIDTH_j[19:8] MIN_VSYNC_PULSE_WIDTH.

NOTE: The following must always be set before DSI_VC_TE_i[30] TE_EN is enabled:

- DSI_TE_HSYNC_WIDTH_j[19:8] MIN_HSYNC_PULSE_WIDTH
- DSI_TE_VSYNC_WIDTH_j[19:8] MIN_VSYNC_PULSE_WIDTH
- DSI_VC_TE_i[29] TE_LINE
- DSI_VC_TE_i[28] TE_LINE_NB

The DSI_VC_TE_i[31] TE_START bit must be used when automatic mode is disabled (DSI_VC_TE_i[30] TE_EN bit = 0). It allows users to start the transfer manually based on application events or based on the TE trigger interrupt (TE_TRIGGER_IRQ).

The number of bytes to be transferred is defined by using the DSI_VC_TE_i[23:0] TE_SIZE bit field. The TE_SIZE bit field is decremented for each payload byte (it does not include checksum) sent on the DSI link. The register content must not be modified by software during a transfer. The DSI_VC_TE_i[23:0] TE_SIZE bit field must be set first to indicate that the following accesses to the DSI_VC_LONG_PACKET_HEADER_i register must be used for TE transfer.

The data can be provided from two sources (select by setting the DSI_VC_CTRL_i[1] SOURCE bit):

- L3 interconnect slave port using DMA request: The DMA request DSI_DMA_REQi must be asserted only when the TE trigger is received or when the DSI_VC_TE_i[31] TE_START bit is set by the user and must no longer be asserted when all the bytes defined in the DSI_VC_TE_i[23:0] TE_SIZE bit field are sent on the DSI link. The VC is associated with a DMA request by programming the number in the DSI_VC_CTRL_i[23:21] DMA_TX_REQ_NB bit field. The DSI_VC_LONG_PACKET_PAYLOAD_i register is used to provide the number of bytes defined by the DSI_VC_TE_i[23:0] TE_SIZE bit field (the checksum value is not provided in the DSI_VC_LONG_PACKET_PAYLOAD_i register). The size of the header is not considered in the number of bytes to transfer. The DSI_VC_SHORT_PACKET_HEADER_i register is not used.

NOTE: All DMA requests associated to a VC must be disabled when they are not used (DSI_VC_CTRLi[23:21] DMA_TX_REQ_NB = 0x4).

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- Video port: The DMA request is not asserted. The data are captured in the line buffer using the STALL mechanism. If no line buffer is instantiated (that is, the DSI_CTRL[13:12] LINE_BUFFER bit field is set to 0), it is not possible to use the video port to provide data. The line buffer is filled according to the word count defined in the DSI_VC_LONG_PACKET_HEADER_i register header. The value must be written before the TE trigger event is received or before the DSI_VC_TE_i[31] TE_START bit is set to 1 by software. If the total number of bytes defined by the DSI_VC_TE_i[23:0] TE_SIZE bit field is not a multiple of the word count defined in the DSI_VC_LONG_PACKET_HEADER_i register, all the packets are the same size defined by the WC of the header, except the last transfer. The size of the last transfer is defined by the remaining bytes to send. Because the DSI_VC_TE_i[23:0] TE_SIZE bit field is modified after each packet transfer, the size of the last packet is equal to the value of the DSI_VC_TE_i[23:0] TE_SIZE bit field before the last transfer (the header and the payload checksum sizes are not included in the DSI_VC_TE_i[23:0] TE_SIZE bit field).

When the transfer completes, the value of the DSI_VC_TE_i[23:0] TE_SIZE bit field is equal to 0. Software must ensure that the pending data in the TX FIFO for the corresponding VC using TE are related to the TE transfer. Any data in the TX FIFO that must be sent before the reception of the TE trigger must be sent before the TE. This is done by not enabling the TE trigger until all data for the corresponding VC are sent to the peripheral. Software can check that the space allocated for the VC in the TX FIFO is empty by reading the DSI_VC_CTRL_i[5] TX_FIFO_NOT_EMPTY status bit.

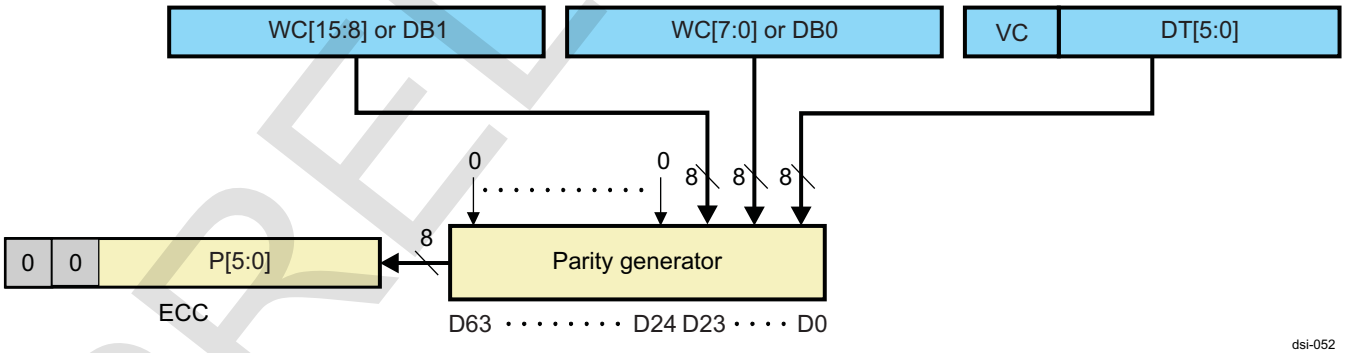
10.3.4.4.9.3 Acknowledge

The corresponding acknowledge interrupt (ACK_TRIGGER_IRQ) is generated when the acknowledge trigger is received. The value of the expected acknowledge trigger pattern can be configured through the DSI_PHY_REGISTER4[15:8] REG_RXTRIGGERESC1 bit field. To enable the acknowledge interrupt, set the DSI_IRQENABLE[17] ACK_TRIGGER_IRQ_EN bit to 1. When the interrupt is generated, the DSI_IRQSTATUS[17] ACK_TRIGGER_IRQ status bit is set to 1.

10.3.4.4.10 ECC Generation

The DSI protocol uses a 4-byte PH. Because ECC generation requires a fixed word length of 64-bits, the packet headers must be padded with additional bits to form a full 8-byte value for ECC generation and checking. The PH minus the ECC byte should occupy bits D[23:0], and the pad bits should occupy bits D[63:24]. All padding bits must be 0 to generate the ECC byte. ECC can be generated using a parallel approach, as shown in Figure 10-141.

Figure 10-141. 64-Bit ECC Generation on TX Side



The ECC generation/check can be enabled and disabled by software. It is defined by a common bit for all the VCs:

- The DSI_CTRL[2] ECC_RX_EN bit enables and disables ECC generation in the receive direction.
- The DSI_VC_CTRL_i[8] ECC_TX_EN bit enables and disables ECC generation in the transmit direction

The ECC can be provided while writing the ECC value directly into the DSI_VC_LONG_PACKET_HEADER_i and DSI_VC_SHORT_PACKET_HEADER_i registers. The DSI_VC_CTRL_i[8] ECC_TX_EN bit indicates whether the ECC value will be calculated or whether the value written in the register will be used instead for command and video modes.

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10.3.4.4.11 Checksum Generation for Long Packet Payloads

Long packets are comprised of a PH protected by an ECC byte and a payload of 0 to 2^{16} - 1 bytes. To detect the errors during the transmission of long packets, a checksum is calculated over the payload portion of the data packet. For the special case of a 0-length payload, the 2-byte checksum is set to 0xFFFF. The checksum can only indicate the presence of one or more errors in the payload. Unlike ECC, the checksum does not enable error correction. For this reason, checksum calculation is not useful for some unidirectional DSI implementations, because the peripheral has no way to report errors to the host processor. Checksum generation and transmission is mandatory for host processors sending long packets to peripherals; it is optional for peripherals transmitting long packets to the host processor. However, the format of long packets is fixed; the peripherals that do not support checksum generation must transmit 2 bytes with a value of 0x0000 in place of the checksum bytes when sending long packets to the host processor. The host processor must disable checksum checking for received long packets from peripherals that do not support checksum generation.

Checksum must be realized as a 16-bit CRC with a generator polynomial of $x^{16}+x^{12}+x^5+x^0$. The LSByte is sent first, followed by the MSByte. Within the byte, the LSB is sent first.

Figure 10-142 shows the checksum transmission.

Figure 10-142. Checksum Transmission

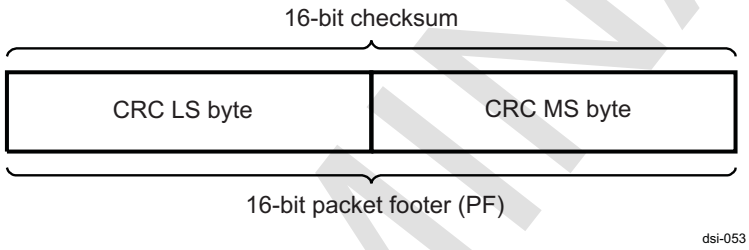
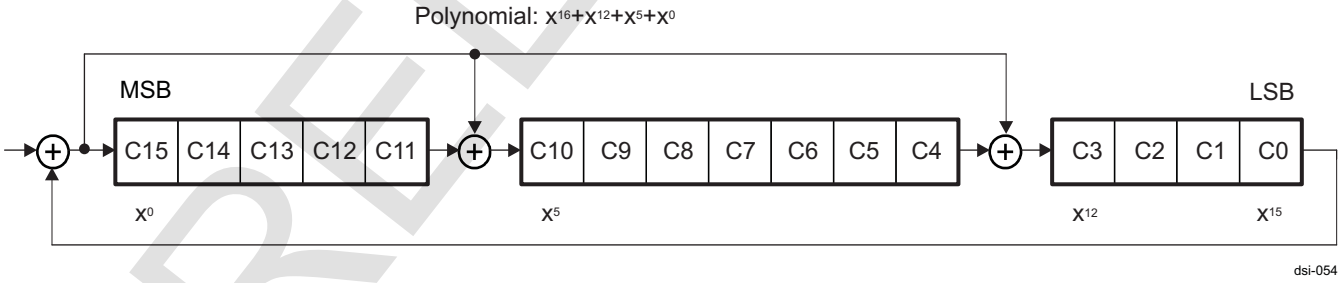


Figure 10-143 shows the CRC implementation. The CRC shift register is initialized to 0xFFFF before packet data enters. Packet data not including the PH then enters as a bitwise data stream from the left, LSB first. Each bit is fed through the CRC shift register before it is passed to the output for transmission to the peripheral. After all bytes in the packet payload have passed through the CRC shift register, the shift register contains the checksum. C15 contains the MSB of the checksum, and C0 contains the LSB of the 16-bit checksum. The checksum is then appended to the data stream and sent to the receiver.

Figure 10-143. 16 Bit CRC Generation Using a Shift Register



Checksum generation/check can be enabled and disabled by software. It is defined by a common bit for all the VCs:

- The DSI_CTRL[1] CS_RX_EN bit enables and disables checksum generation in the receive direction.
- The DSI_VC_CTRL_i[7] CS_TX_EN bit enables and disables checksum generation in the transmit direction

10.3.4.4.12 EOT Packet

A new packet type allows the DSI protocol (rather than the DSI_PHY) at the display to detect the HS EOT. This is a fixed short packet (4 bytes) that is added at every HS to LP transition. This function is enabled by the DSI_CTRL[19] EOT_ENABLE bit.

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The EOT packet has a fixed format:

- Data Type = DI [5:0] = 0b001000
- Virtual Channel = DI [7:6] = 0b00
- Payload Data [15:0] = 0x0F0F
- ECC [7:0] = 0x01

When more that one data lane is used, the EOT packet bytes are distributed across the multiple lanes. EOT packet generation is supported only for the end of HS transmissions. No EOT packet is added at the end of LP transmissions. For LP reception, any EOT packet received is simply passed through as any other packet, but no internal decode or use is made of the EOT information.

10.3.4.4.13 Software Reset

The DSI protocol engine can be reset by software. This reset can be done for debug purposes or after a protocol error and has the same effect as the hardware reset. The DSI protocol engine can be reset by setting the DSI_SYSCONFIG[1] SOFT_RESET bit to 1. Software can monitor the DSI_SYSSTATUS[0] RESET_DONE status bit to wait for the reset to complete. If after five reads the DSI_SYSSTATUS[0] RESET_DONE status bit still returns 0, it can be assumed that an error occurred during the reset stage.

NOTE: This software reset is optional because a hardware reset is always performed on the DSI protocol engine at device reset.

10.3.4.4.14 Power Management

The power-management behavior of the DSI protocol engine is controlled by the DSI_SYSCONFIG register. This register controls the way the module interacts with the PRCM module. The DSI_SYSCONFIG[0] AUTO_IDLE bit must be set to 1 (default value) to enable automatic clock gating in the module.

The DSI protocol engine implements a handshake protocol on the L3 interconnect slave port with the PRCM module. The protocol engine provides control signal CIO_CLK_ICG to gate the SCPClk (DSS_L3_ICLK/4). It allows reduction of the power consumption of the complex I/O while the DSI link is not in use (DSI_CLK_CTRL[14] CIO_CLK_ICG).

10.3.4.4.15 Power Control of DSI PHY Complex I/O and DSI PLL

The DSI protocol engine can control and send power commands for the DSI complex I/O and DSI PLL controller modules.

10.3.4.4.15.1 Complex I/O Power Control Commands

10.3.4.4.15.1.1 Complex I/O Power Control Commands

The DSI complex I/O can be set in three modes:

- OFF: In this power state, the complete DSI_PHY circuit is powered down. The internal LDO is OFF.
- ON: In this power state, the complete DSI_PHY circuit is powered on and functional.
- ULPS: In this power state, the ULPS exit detection circuit power switch is ON for the lanes that are in receive ULPS. For the lanes that are in transmit ULPS, the circuitry for weak pulldown is ON. The ULTRALOW POWER state must be used only when all the three lanes are in ULPS (transmit or receive).

10.3.4.4.15.1.2 Complex I/O Power FSM

Figure 10-144 shows the FSM to control the power state of the complex I/O.

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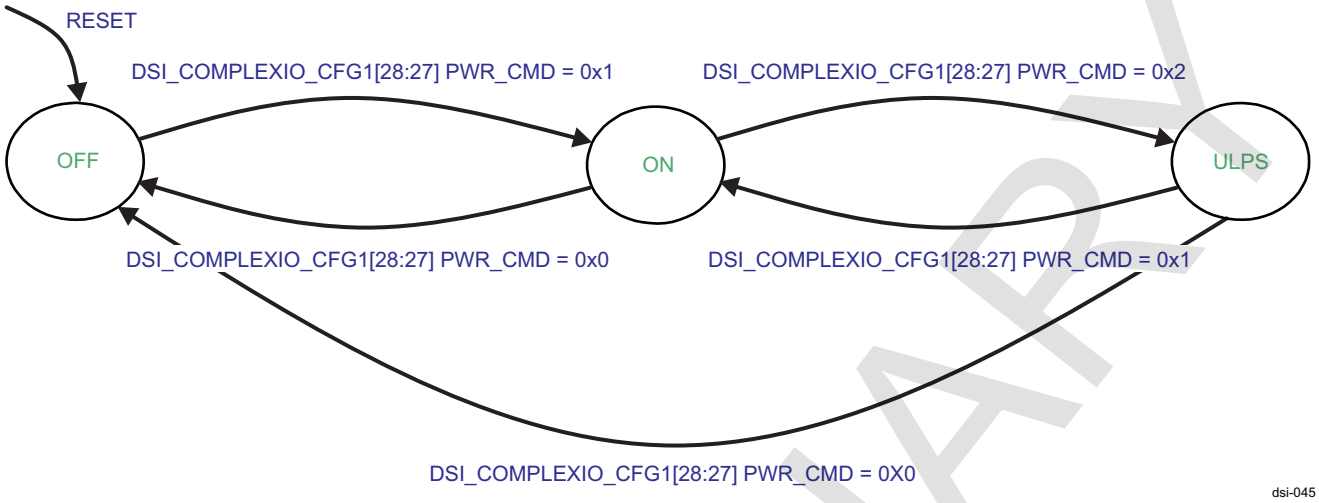
Figure 10-144. Complex I/O Power FSM



The PwrCmdOff, PwrCmdUlp, and PwrCmdOn commands control the state transition of the DSI complex I/O. The DSI_COMPLEXIO_CFG1[28:27] PWR_CMD bit field allows the state to be modified. The allowed transitions are: OFF - ON, and ON - ULPS, and ULPS - OFF. The DSI_COMPLEXIO_CFG1[26:25] PWR_STATUS bit field gives a status on the current state of the DSI complex I/O.

CAUTION

- In automatic mode, software must ensure that the DSI complex I/O is in ON state (that is, ON command already sent) before sending requests to the complex I/O.
- In a command request to change to a state that is the current one (acknowledge has been received), the command is ignored (nothing is sent to the DSI complex I/O).
- To change the state to ULPS, all ULPSActiveNot signals must be low. The ULPSActiveNot_ALL0_IRQ interrupt indicates the state of the ULPSActiveNot signals. The change from ULPS to ON state is required before starting the ULP exit sequence (for information, see Section 10.3.4.4.7.1, T_{wakeup} *Timer*).

10.3.4.4.15.2 DSI PLL Power Control Commands

The DSI PLL controller module can be set in four modes:

- OFF: DSI PLL and HSDIVIDER are OFF.
- ON ALL: Both DSI PLL and HSDIVIDER are ON. The CLKIN4DDR clock is provided to the DSI complex I/O and the second clock output is provided to the HSDIVIDER.
- ON HSCLK: The DSI PLL is ON. The HSDIVIDER is OFF. The CLKIN4DDR clock is provided to the DSI complex I/O, but the second clock output is not provided to the HSDIVIDER.
- ON DIV: DSI PLL and HSDIVIDER are ON. The CLKIN4DDR clock is not provided to the DSI complex I/O, but the second clock output is provided to the HSDIVIDER.

10.3.4.4.15.2.1 DSI-PLL Power FSM

Figure 10-145 shows the DSI PLL power FSM.

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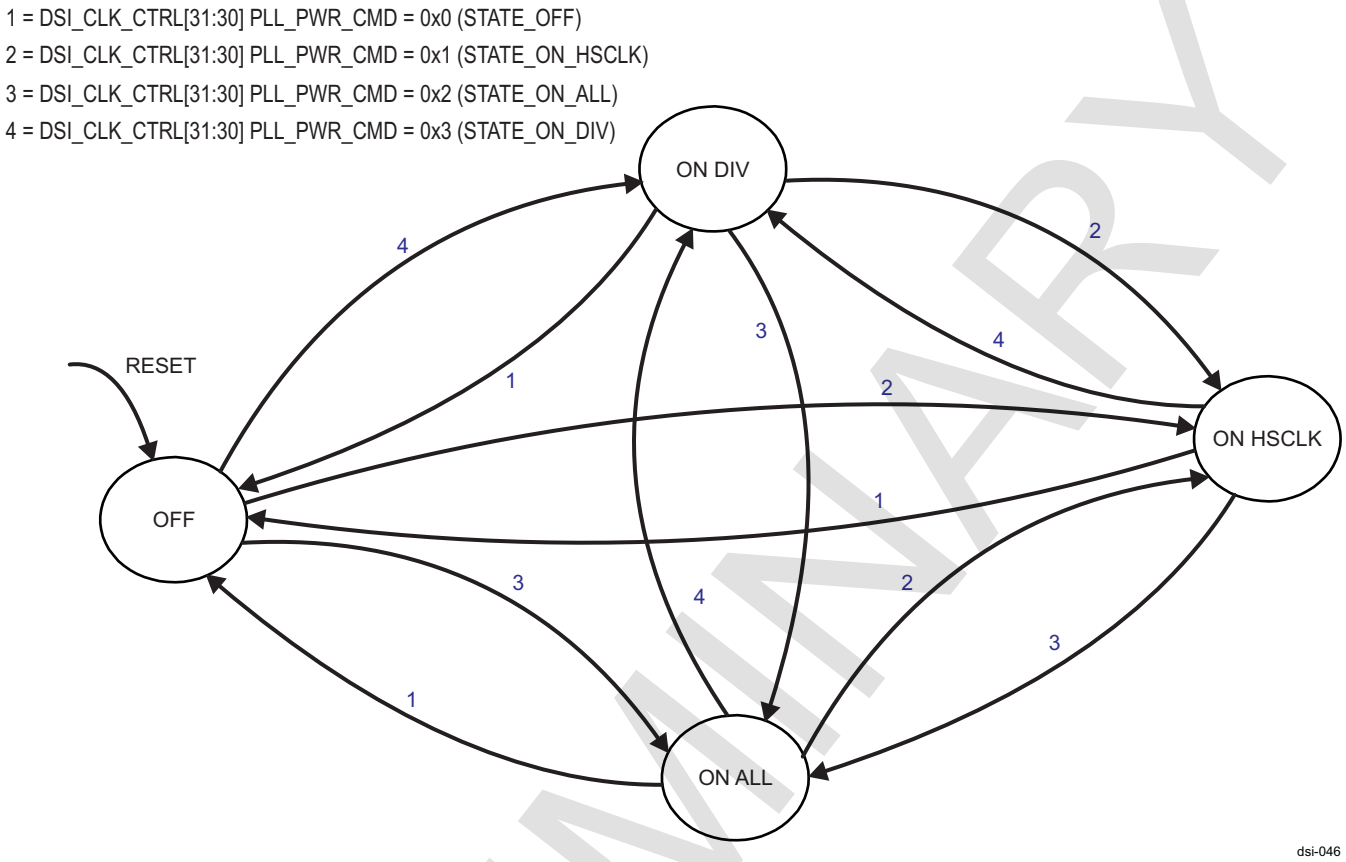
Figure 10-145. DSI PLL Power FSM



The following commands control the state transition of the DSI PLL control module:

- PLLPwrCmdOff
- PLLPwrCmdOnAll
- PLLPwrCmdOnDIV
- PLLPwrCmdOnHSClk

Setting the DSI_CLK_CTRL[31:30] PLL_PWR_CMD bit field modifies the state. The DSI_CLK_CTRL[29:28] PLL_PWR_STATUS bit field gives a status on the current state of the DSI PLL controller.

NOTE: If a command requests to change to a state that is the current one (acknowledge has been received), the command is ignored (nothing is sent to the DSI PLL control module).

10.3.4.4.15.2.1.1 DSI PLL HS Clock Signals

The DSIStopClk signal is provided to the DSI PLL control module. It indicates when the DSI protocol engine does not need to use the HS mode and the PLL HS output (CLKIN4DDR clock) can be stopped. The following conditions must also be met when DISPC_UPDATE_SYNC may be generated by the DISPC, because that must result in the PLL HS output being stopped.

When the interface is disabled (DSI_CTRL[0] IF_EN bit set to 0) and the clock lane is stopped (DSI_CLK_CTRL[13] DDR_CLK_ALWAYS_ON = 0), the signal DSIStopClk is asserted.

Assertion of the DSIStopClk depends on the following conditions:

- Clock lane TxRequestHS is deasserted (the DDR clock on the clock lane is no longer required). For TxRequestHS deassertion, the following conditions are required:

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– The DSI_CLK_CTRL[13] DDR_CLK_ALWAYS_ON bit must be reset to 0 and no HS data transfer must be on-going or already scheduled.
– No VC ACTIVE in video mode. No VC using the video mode is enabled. If the VC is enabled, the mode is command mode only (the DSI_VC_CTRL_i[0] VC_EN bit set to 1 and DSI_VC_CTRL_i[4] MODE bit set to 0).
– No command mode requiring HS transfer (one or more VCs using command mode can be active)
– Or DSI_CTRL[0] IF_EN bit is reset to 0 (the previous conditions are not all required, except the DSI_CLK_CTRL[13] DDR_CLK_ALWAYS_ON bit must be set to 0 after resetting the DSI_CTRL[0] IF_EN bit)

The deassertion of the DSIStopClk depends on one of the following conditions (the DSI interface is enabled by setting the DSI_CTRL[0] IF_EN bit to 1):

- Clock lane TxRequestHS must be asserted (the DDR clock on the clock lane is required).
- One video mode VC ACTIVE
- At least one VC in command mode requiring HS transfer
- The DSI_CLK_CTRL[13] DDR_CLK_ALWAYS_ON bit is set to 1 by software users (the DSI_CTRL[0] IF_EN bit must be reset to 0 for updating the value of the DDR_CLK_ALWAYS_ON bit).

Automatic assertion/deassertion is enabled by using the DSI_CLK_CTRL[18] HS_AUTO_STOP_ENABLE bit.

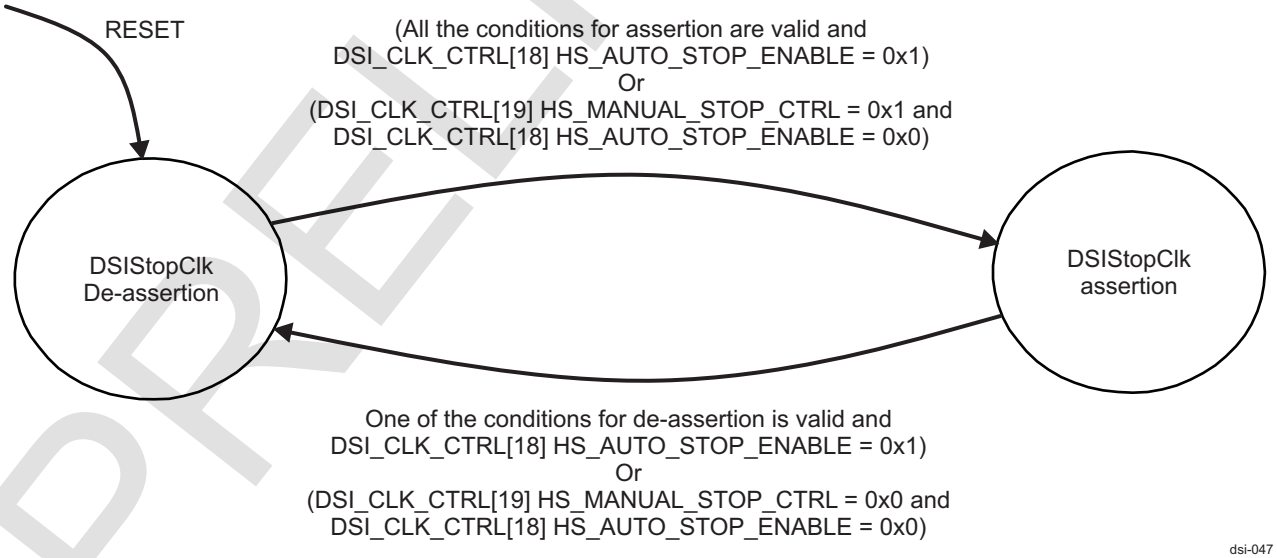
Manual mode can be used by setting/resetting the DSI_CLK_CTRL[19] HS_MANUAL_STOP_CTRL bit to assert/deassert the DSIStopClk signal.

NOTE: Setting the DSI_CTRL[24] DISPC_UPDATE _SYNC bit to 0x1 enables the use of the Dispc_Update_Sync signal to synchronize.

10.3.4.4.15.2.1.2 DSI-PLL HS Clock FSM

Figure 10-146 shows the DSI PLL HS clock FSM.

Figure 10-146. DSI PLL HS Clock FSM



When DSIStopClk is used there is a latency through other modules (DSI PLL controller and DSI_PHY) before TXBYTECLKHS is stopped. This latency must be considered to prevent any issue when DSIStopClk is deasserted soon after being asserted. This is done using a hardware timer programmed using the DSI_STOPCLK_TIMING[7:0] DSI_STOPCLK_LATENCY bit field. This timer is programmed in number of periods of the DSI protocol functional clock (DSI_FCLK). At reset value, the timer is programmed with value 0x80 (128).

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CAUTION

The programmed value in the DSI_STOPCLK_TIMING[7:0] DSI_STOPCLK_LATENCY bit field must be greater than ((3 x L3_ICLK period) + (5 x CLKIN4DDR period))/(DSI_FCLK period).

10.3.4.4.16 Ultralow-Power State Configuration

This section describes how to enter/exit to/from ULTRALOW-POWER state (ULPS).

NOTE: The DSI_COMPLEXIO_CFG2[9:0] LANEx_ULPS_SIGy bits (***x*** range is 1 to 5, corresponding to lane 1 to lane 5 for DSI1, and 1 to 3, corresponding to lane 1 to lane 3 for DSI2; ***y*** range is 1 to 2) must be read back after writing to verify that the write operations are effective before proceeding to the next step. This is to take latency at low TxClkEsc frequencies into account.

10.3.4.4.16.1 Entering ULPS

To enter into ULPS for a clock lane, the following sequence is required:

1. Wait for DSI_COMPLEXIO_CFG2[16] HS_BUSY and DSI_COMPLEXIO_CFG2[17] LP_BUSY bits to be reset to 0 and ensure that the DSI_CLK_CTRL[13] DDR_CLK_ALWAYS_ON bit is 0.
2. TxUlpsClk state should change from inactive to active by setting the DSI_COMPLEXIO_CFG2[9:5] LANEx_ULPS_SIG2 bit to 1.

To enter into ULPS for a data lane, the following sequence is required:

1. Wait for all TX_FIFOs for all VCs working in HS are empty, for video mode is not active, and for DSI_COMPLEXIO_CFG2[16] HS_BUSY bit is reset to 0 (in addition for data lane 1, DSI_COMPLEXIO_CFG2[17] LP_BUSY bit is reset to 0)
2. TxRequestEsc state should change from inactive to active by setting the DSI_COMPLEXIO_CFG2[9:5] LANEx_ULPS_SIG2 bit to 1.

10.3.4.4.16.2 Exiting ULPS

To exit from ULPS for a clock lane, the following sequence is required:

1. Change the state of TxUlpsExit for each lane to ACTIVE by setting the DSI_COMPLEXIO_CFG2[4:0] LANEx_ULPS_SIG1 bit to 1.
2. Wait for the ULPSACTIVENOT_ALL1_IRQ interrupt indicating that all lanes with TxUlpsExit active have acknowledged by asserting UlpsActiveNot. This is performed by monitoring the DSI_COMPLEXIO_IRQSTATUS[31] ULPSACTIVENOT_ALL1_IRQ status bit.
3. Start the wake-up timer (GPTimer).
4. Wait for the time-out.
5. Change TxUlpsClk signals to INACTIVE state for the clock lane by resetting the DSI_COMPLEXIO_CFG2[9:5] LANEx_ULPS_SIG2 bit to 0.
6. Reset the DSI_COMPLEXIO_CFG2[4:0] LANEx_ULPS_SIG1 bit to 0.

NOTE: When the DSI_COMPLEXIO_CFG2[9:5] LANEx_ULPS_SIG2 and DSI_COMPLEXIO_CFG2[4:0] LANEx_ULPS_SIG1 bits are both being written to 0, they can be combined into one write. Both bits must be read back to confirm they are effective before proceeding.

To exit from ULPS for a clock lane, in case the complex I/O is in OFF state (the DSI protocol engine sends the complex I/O to OFF state (PWROFF command) by setting DSI_COMPLEXIO_CFG1[28:27] PWR_CMD = 0x0), the sequence is:

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1. Change TxUlpsClk signals to INACTIVE state for the clock lane by resetting the DSI_COMPLEXIO_CFG2[9:5] LANEx_ULPS_SIG2 bit to 0.
2. Change the state of TxUlpsExit for clock lane to INACTIVE state by resetting the DSI_COMPLEXIO_CFG2[4:0] LANEx_ULPS_SIG1 bit to 0. This step is necessary only in case a PWROFF command (the command for power control of the complex I/O) is issued while the sequence for exiting is in progress (TxUlpsExit signal is already in ACTIVE state).

NOTE: When the DSI_COMPLEXIO_CFG2 LANEx_ULPS_SIG2[9:5] and DSI_COMPLEXIO_CFG2[4:0] LANEx_ULPS_SIG1 bits are both being written to 0, they can be combined into one write. Both bits must be read back to confirm they are effective before proceeding.

To exit from ULPS for a data lane, the following sequence is required:

1. Change the state of TxUlpsExit for each lane to ACTIVE by setting the DSI_COMPLEXIO_CFG2[4:0] LANEx_ULPS_SIG1 bit to 1.
2. Wait for the ULPSACTIVENOT_ALL1_IRQ interrupt indicating that all lanes with TxUlpsExit active have acknowledged by asserting UlpsActiveNot. This is performed by monitoring the DSI_COMPLEXIO_IRQSTATUS[31] ULPSACTIVENOT_ALL1_IRQ status bit.
3. Start the application wake-up timer (GPtimer).
4. Wait for the time-out.
5. Change TxRequestEsc signals to INACTIVE state for the data lane by resetting the DSI_COMPLEXIO_CFG2[9:5] LANEx_ULPS_SIG2 bit to 0.
6. Reset the DSI_COMPLEXIO_CFG2[4:0] LANEx_ULPS_SIG1 bit to 0.

NOTE: When the DSI_COMPLEXIO_CFG2[9:5] LANEx_ULPS_SIG2 and DSI_COMPLEXIO_CFG2[4:0] LANEx_ULPS_SIG1 bits are both being written to 0, they can be combined into one write. Both bits must be read back to confirm they are effective before proceeding.

To exit from ULPS for a data lane, in case the complex I/O is in OFF state (the DSI protocol engine sends the complex I/O into OFF state by setting DSI_COMPLEXIO_CFG1[28:27] PWR_CMD = 0x0), the sequence is:

1. Change TxRequestEsc signals to INACTIVE state by resetting the DSI_COMPLEXIO_CFG2[9:5] LANEx_ULPS_SIG2 bit to 0.
2. Change the state of TxUlpsExit to INACTIVE state by resetting the DSI_COMPLEXIO_CFG2[4:0] LANEx_ULPS_SIG1 bit to 0. This step is necessary only in case a PWROFF command is issued while the sequence for exiting is in progress (TxUlpsExit signal is already in ACTIVE state).

NOTE: When the DSI_COMPLEXIO_CFG2[9:5] LANEx_ULPS_SIG2 and DSI_COMPLEXIO_CFG2[4:0] LANEx_ULPS_SIG1 bits are both being written to 0, they can be combined into one write. Both bits must be read back to confirm they are effective before proceeding.

When the sequence for entering/exiting into/from ULP state is started for specific lanes, users should wait for the completion of the sequence before changing the state of the same or other lanes.

10.3.4.4.17 Interrupts

There is a single interrupt request generated by each DSI: DSI_IRQ. This interrupt line is merged with another interrupt line from the DISPC_IRQ into a single interrupt request IRQ. The DSI_IRQ events are generated only for the enabled VC(s). Two registers are used to enable and monitor the DSI interrupt events:

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- DSI_IRQENABLE: This register enables and disables interrupt event reporting for the VCs. Each event for the VC is configured in the DSI_VC_IRQENABLE_i register dedicated to the VC number. In addition, it includes 1 bit to enable error reporting for the complex I/O. The interrupt is triggered when any error is received from the complex I/O.
- DSI_IRQSTATUS: The register flags which VC(s) have generated an interrupt. Based on the VC number, the DSI_VC_IRQSTATUS_i register indicates the event generating the interrupt. In addition, it includes 1 bit for the status of error reporting for the complex I/O.

Table 10-491 lists the DSI VC interrupt events

Table 10-491. DSI VC Interrupts

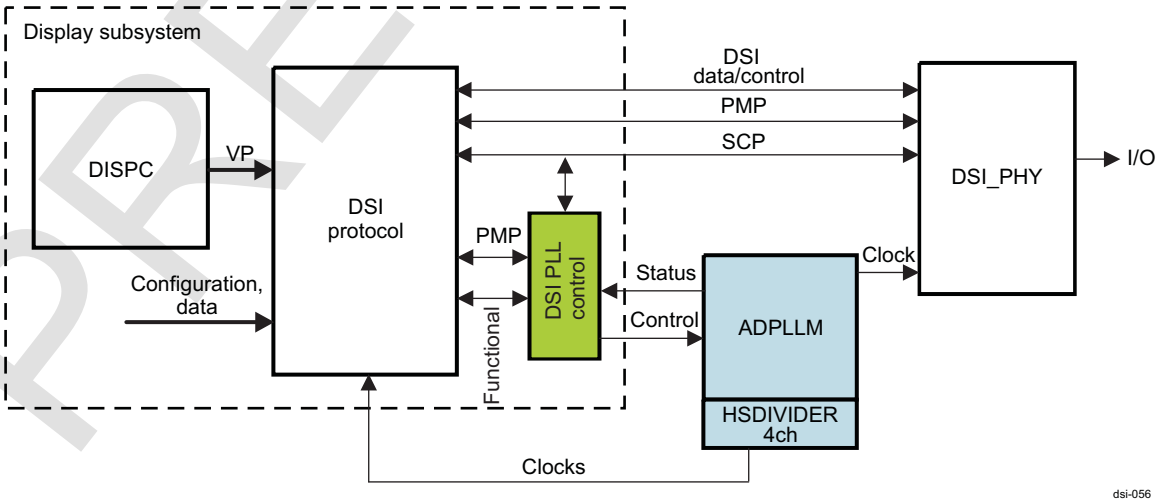
IRQ Name	Description
ECC_CORRECTION_IRQ	Indicates whether a 1-bit error correction has occurred using ECC (short and long packets).
PACKET_SENT_IRQ	Indicates that a packet has been sent. It is used when BTA manual mode is used.
CS_IRQ	Virtual channel. Checksum of the payload mismatch detection.
FIFO_RX_OVF_IRQ	RX FIFO overflow. The FIFO used on the L3 interconnect slave port for buffering the data received on the DSI link has overflowed.
FIFO_TX_OVF_IRQ	TX FIFO overflow. The FIFO used on the L3 interconnect slave port for buffering the data received on the interface slave port has overflowed.
BTA_IRQ	BTA is received from the peripheral (the VC ID used for the last BTA request transfer to the peripheral will be used to determine which VC will be used to flag the interrupt).
ECC_NO_CORRECTION_IRQ	ECC error (short and long packets). No correction of the header because of more than 1-bit error.
FIFO_TX_UDF_IRQ	TX FIFO underflow. The FIFO used on the slave port for buffering the data received on the L3 interconnect slave port has underflowed in the middle of a packet transfer.

10.3.4.5 DSI PLL Controllers

10.3.4.5.1 DSI PLL Controllers Overview

Two DSI PLL controller modules are part of the DSS. They use the SCP (see Section 10.3.4.4.6, *Serial Configuration Port Interface*) and power-management port (PMP) as the primary interfaces to the DSI protocol engines. The SCP interface is used to set the configuration of the digital phase-locked loop (DPLL) and HSDIVIDER modules, primarily the various counter values. The PMP is used to control the power state of the DPLL and HSDIVIDER modules. Figure 10-147 is an overview of a single DSI PLL controller module in the display subsystem.

Figure 10-147. DSI PLL Controller Overview



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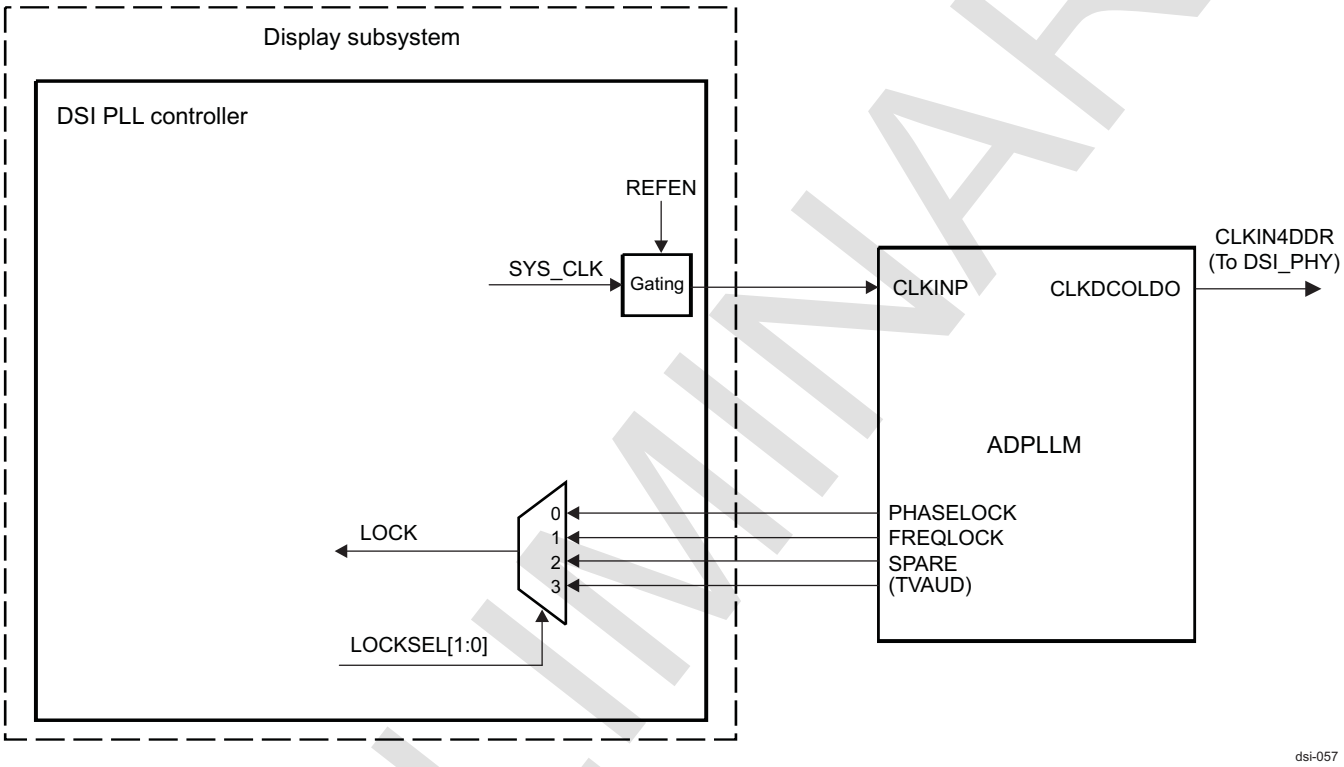
NOTE: The DSI PLL controller modules do not have an interface to L3/L4_PER interconnects. The programmable features are managed by registers mapped into the DSI protocol engines.

10.3.4.5.2 DSI PLL Controllers Architecture

The DSI PLLs use instances of the ADPLLM modules.

Figure 10-148 shows the internal reference diagram of a single DSI PLL.

Figure 10-148. DSI PLL Reference Diagram



The DSI PLL clock output (CLKDCOLDO) corresponds to the CLKIN4DDR clock of a DSI complex I/O (DSI_PHY) module.

Only the SYS_CLK clock is used as an input reference clock for the ADPLLM. The DSI PLL controller can gate this clock by setting the DSI_PLL_CONFIGURATION2[13] PLL_REFEN bit.

Figure 10-149 is a simplified block diagram of the ADPLLM instance used for the DSI modules.

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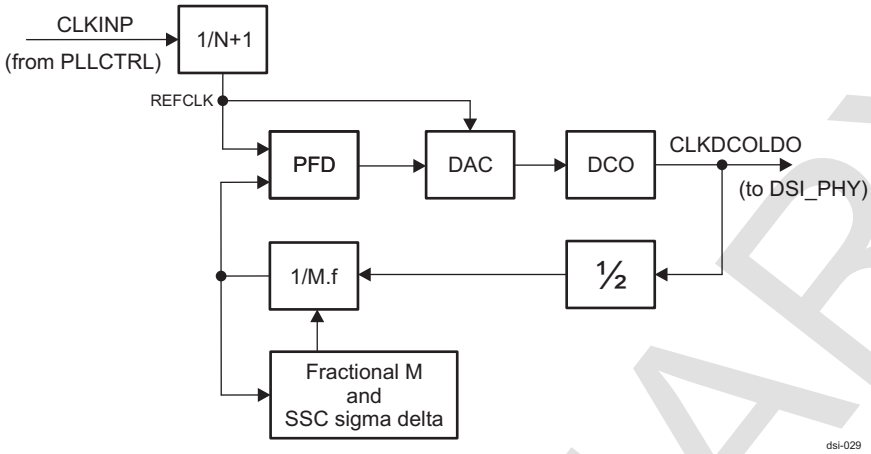
Figure 10-149. ADPLLM Functional Block Diagram



The input clock CLKINP goes to a predivider N + 1. The entire loop runs on the REFCLK clock after this predivider. The value of N + 1 is controlled through the DSI_PLL_CONFIGURATION1[8:1] PLL_REGN bit field. The frequency range for the CLKINP and REFCLK clocks is 0.032 MHz to 52 MHz.

The output clock CLKDCOLDO is synthesized by digitally controlled oscillator (the DCO block), that automatically detects the frequency range. The CLKDCOLDO frequency can be given with CLKDCOLDO = CLKINP*2*M/(N + 1). For that purpose the feedback multiplier M must be configured through the DSI_PLL_CONFIGURATION1[20:9] PLL_REGM bit field.

The ADPLLM module supports fractional synthesis; that is, the frequency multiplication factor M can be programmed as fractional. This is done through the use of a sigma delta feedback divider (M). A fractional value (REGM.f) of 18 bits is supported, thus enabling control for better accuracy. Programming the fractional value is done by setting the DSI_PLL_CONFIGURATION4[17:0] PLL_REGM_F register bit field. Fractional synthesis is supported only in the following range: 20 <= M <= 2045.

The module also supports spread spectrum clocking (SSC) on its output clocks. SSC is used to spread the spectral peaking of the clock to reduce electromagnetic interference (EMI). When SSC is enabled, the clock spectrum is spread by the amount of frequency spread, and the attenuation is given by the ratio of the frequency spread (df) and the modulation frequency (fm); that is, $[\{10*\log_{10}(df/fm)\} - 10]$ dB.

The SSC is performed by changing the feedback divider (M) in a triangular pattern, which means the frequency of the output clock varies in a triangular pattern. The frequency of the triangular pattern is modulation frequency (fm). The peak (dM) or the amplitude of the triangular pattern as a percent of M is equal to the percent of the frequency spread (df) (that is, dM/M = df/Fout).

Because this is in band modulation for the DSI PLL, the modulation frequency (fm) must be within the bandwidth of the PLL (lowest BW of REFCLK/70; that is, REFCLK must be > fm*70). A higher modulation frequency results in less spreading in the output clock.

The SSC can be enabled and disabled by asserting the DSI_PLL_SSC_CONFIGURATION1[0] EN_SSC bit. The acknowledge signal SSCACK, observed by the DSI_PLL_STATUS[12] SSC_EN_ACK bit, notifies the exact start and end of SSC. When EN_SSC is deasserted, SSC is disabled only after completion of one full cycle of the triangular pattern given by the modulation frequency. This is done to maintain the average frequency.

The modulation frequency (fm) can be programmed as a ratio of REFCLK/4; that is, the value of ModFreqDivider programmed in the DSI_PLL_SSC_CONFIGURATION2[29:20] MODFREQDIVIDER bit field must be = REFCLK/(4*fm). The ModFreqDivider is split into Mantissa and $2^{Exponent}$ (ModFreqDivider = ModFreqDividerMantissa * $2^{ModFreqDividerExponent}$).

- The Mantissa is controlled by bits [26:20] of the MODFREQDIVIDER bit field.
- The Exponent is controlled by bits [29:27] of the MODFREQDIVIDER bit field.

Although the same value of ModFreqDivider can be obtained by different combinations of Mantissa and Exponent values, it is preferred to get the target ModFreqDivider by programming maximum Mantissa and minimum Exponent values.

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To define the frequency spread (df), M must be controlled as explained previously. To define M, the step size of M for each REFCLK during the triangular pattern bust be programmed (that is, M = ModFreqDivider * DeltaMStep). DeltaMStep is controlled by the DSI_PLL_SSC_CONFIGURATION2[19:0] DELTAM bit field. DeltaMStep is split into an integer part and a fractional part:

- The integer part is controlled by bits [19:18] of the DELTAM bit field.
- The fractional part is controlled by bits [17:0] of the DELTAM bit field.

The frequency spread achieved, however, has an overshoot of 20% or an inaccuracy of +20%.

If the DSI_PLL_SSC_CONFIGURATION1[2] DOWNSPREAD bit is set to 1, the frequency spread on the lower side is twice the programmed value. The frequency spread on the higher side is 0 (except for the overshoot, as described above).

NOTE: There is a restriction in the range of M values. The restriction is that (M – dM) must be >= 20. Also, M + dM must be <= 2045. If the DSI_PLL_SSC_CONFIGURATION1[2] DOWNSPREAD bit is set to 1, then (M – 2*dM) must be >= 20 and M <= 2045.

10.3.4.5.3 DSI PLL Operations

The DSI PLL configuration signals operate according to Table 10-492, which indicates the operation when the PLLs are not locked.

Table 10-492. DSI PLL Operation Modes When Not Locked

DSI PLL Operation Mode	Stop Mode Low Power [1]	Stop Mode Fast Relock [1]	Idle Bypass
Mode Description	Output clocks stopped Lowest power standby	Output clocks stopped Fastest start-up time	Selects when PLLs and HSDIVIDERs bypass clocks are used
DSI_PLL_CONFIGURATION2[0] PLL_IDLE	0	0	1
DSI_PLL_CONFIGURATION2[6] PLL_LOWCURRSTBY	1	0	1
DSI_PLL_CONFIGURATION1[0] PLL_STOPMODE	1	1	x

(1) This mode must be used for better performance.

When locked, the PLL output frequency is: Input frequency * 2 * M/(N + 1), where:

- M multiplier is programmed in the DSI_PLL_CONFIGURATION1[20:9] PLL_REGM bit field.
- N divider is programmed in the DSI_PLL_CONFIGURATION1[8:1] PLL_REGN bit field.

10.3.4.5.4 DSI PLL Controllers Shadowing Mechanism

The configuration registers are accessed through the DSI protocol engine register spaces using the SCP interface. This includes all the configuration signals and returning status signals.

CAUTION

All writes must be 32-bit operations, because the SCP interface always transfers 32 bits; 16-or 8-bit operations may lead to unpredictable errors.

A shadow mechanism is implemented for appropriate register values so that configurations can optionally be updated in synchronization with the DISPC and DSI protocol engines. The front porch time from the DISPC indicates the time when making the update of the value. All the required updated values must be written before this signal is asserted. For more information, seeSection 10.3.4.4.6.1, *Shadowing Register*.

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10.3.4.5.5 Error Handling

The PLL lock and recalibration signals can be monitored to detect the loss of lock or the requirement to recalibrate (caused by a large temperature change since the last lock request):

- The DSI_PLL_STATUS[1] PLL_LOCK status bit gives the DSI PLL lock state.
- The DSI_PLL_STATUS[2] PLL_RECAL status bit informs whether the PLL must be uncalibrated.

These signals can also generate interrupts at the DSI protocol engine level:

- The PLL_LOCK_IRQ interrupt indicates that the DSI PLL control module has sent a lock request to the DSI PLL. To monitor this event, read the DSI_IRQSTATUS[7] PLL_LOCK_IRQ bit. Set this bit to 1 to clear the status bit.
- The PLL_UNLOCK_IRQ interrupt indicates that the DSI PLL control module has sent an unlock request to the DSI PLL. To monitor this event, read the DSI_IRQSTATUS[8] PLL_UNLOCK_IRQ bit. Set this bit to 1 to clear the status bit.
- The PLL_RECAL_IRQ interrupt indicates that the DSI PLL control module has sent a recalibration request to the DSI PLL. To monitor this event, read the DSI_IRQSTATUS[9] PLL_RECAL_IRQ bit. Set this bit to 1 to clear the status bit.

The PLL reference loss and limp status signals can also be monitored:

- The DSI_PLL_STATUS[3] PLL_LOSSREF status bit informs whether the DSI PLL has lost the reference.
- The DSI_PLL_STATUS[4] PLL_LIMP bit informs about the DSI PLL limp status.

10.3.4.5.6 Software Reset

The DSI PLL control modules do not have their own software reset. They are reset by the global DSS_RST signal at PRCM module level. See Section 10.1.2.2, *DSS Resets*. Nevertheless, software users can monitor the reset statuses of the DSI PLL control modules by reading the DSI_PLL_STATUS[0] PLLCTRL_RESET_DONE status bits.

10.3.4.5.7 Power Management

PLLCTRL manages only the LDO power of the ADPLLM and HSDIVIDER; this is done by overriding the SYSRESET signals. All other power-management signals are integrated with the display subsystem power management..

Figure 10-150 shows the power states that are controlled through the PMP.

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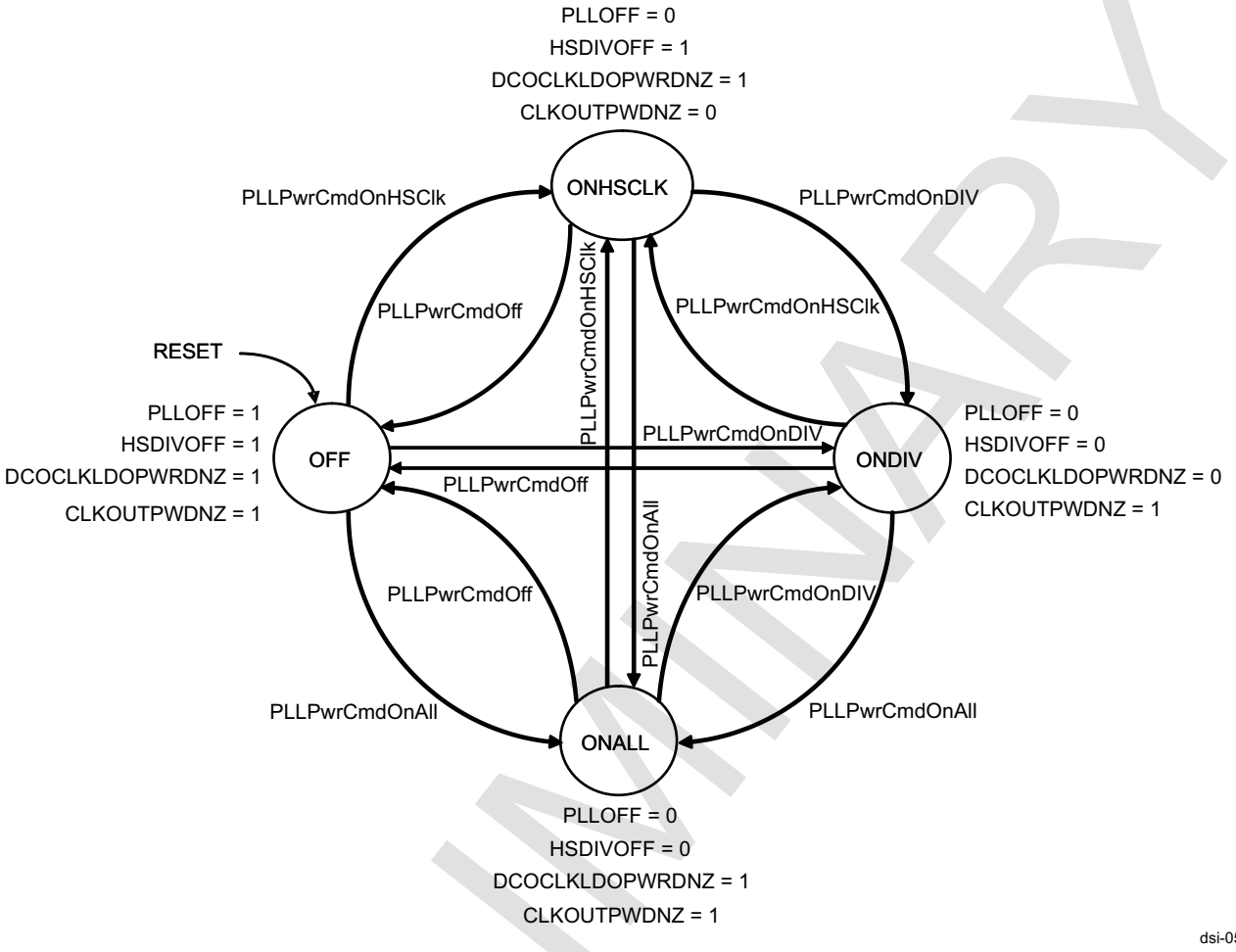
Figure 10-150. Power State Diagram



10.3.4.5.8 DSI PLL Clock-Gating Sequence

Clock gating can be used to reduce system power consumption when the DSI protocol engine indicates that it does not need the clock. If the HSDIVIDER is not used, the PLL can also be stopped (at the cost of additional unstarting latency).

The DSI protocol engines must verify when the PLLs have unstarted by inspecting the LOCK signal (the DSI_PLL_STATUS[1] PLL_LOCK status bit), because the TXBYTECLKHS clocks are stopped when the CLKIN4DDR clocks generated by the DSI PLL are stopped. This eliminates the need for any explicit feedback that the clock has been unstarted. This flow chart should run even if the DSI_PLL_GO[0] PLL_GO bit is not set.

Figure 10-151 shows the DSI PLL gated mode sequence.

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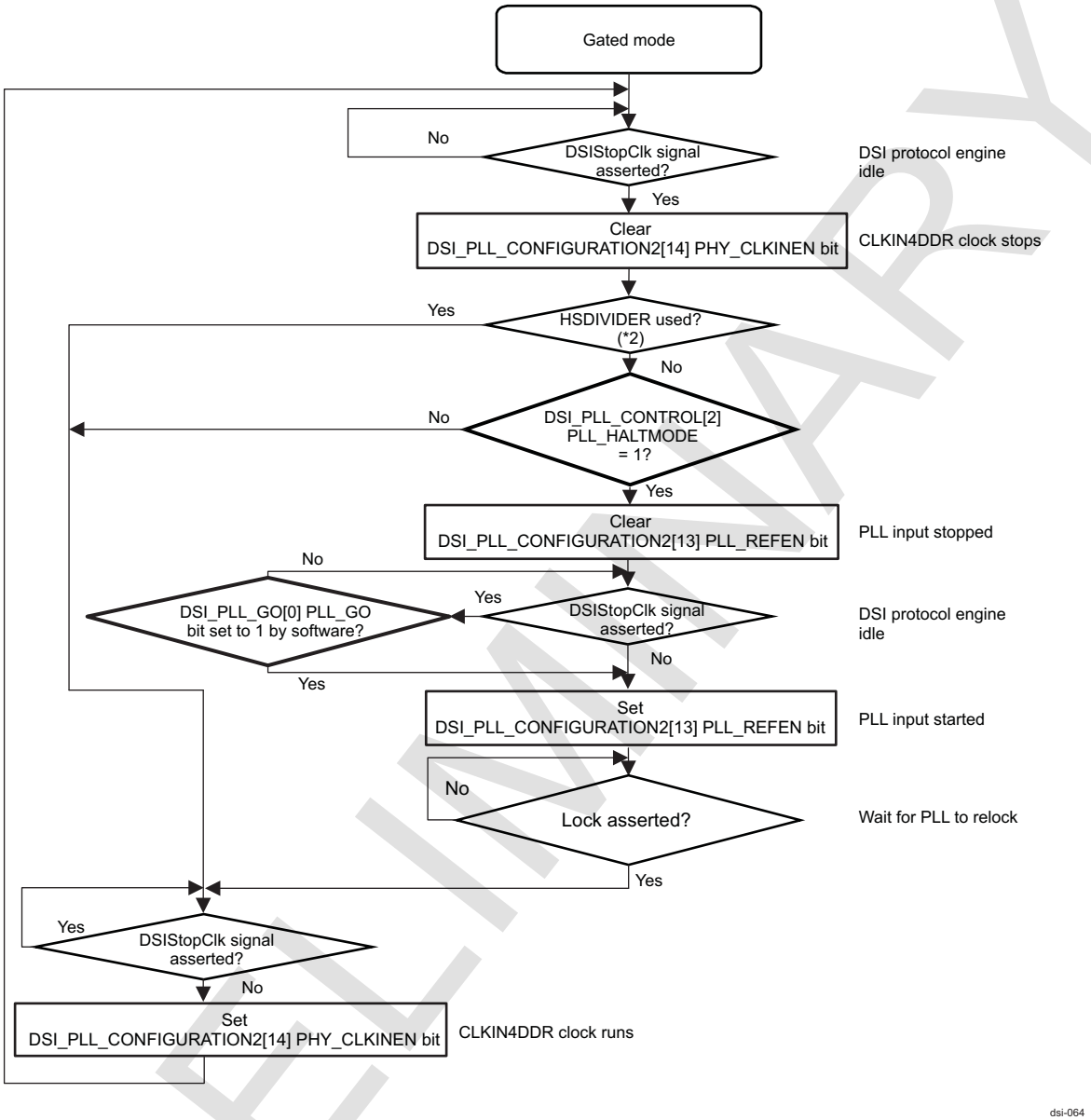
Figure 10-151. Gated Mode Sequence



(1) All thick-outlined blocks show operations performed by software. Other blocks show operations performed by hardware.

(2) HSDIVIDER is used if any of the following bits is set to 1:

- DSS_CTRL[12] LCD2_CLK_SWITCH
- DSS_CTRL[0] LCD1_CLK_SWITCH
- DSS_CTRL[1] DSI1_CLK_SWITCH
- DSS_CTRL[10] DSI2_CLK_SWITCH

(3) For more information, see Section 10.1 *Display Subsystem Overview*.

Table 10-493. Register Call Summary for Gated Mode Sequence

Register Name	Register Name	Register Name
DSI_PLL_CONFIGURATION2	DSI_PLL_CONTROL	DSI_PLL_GO

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10.3.4.5.9 DSI PLL Clock Sequence

The two DSI PLLs generate the CLKIN4DDR clocks. Each HSDIVIDER outputs two clocks: PLLx_CLK1, connected to the DISPC; and PLLx_CLK2, connected to the DSI protocol engine (where x is the number of the dedicated DSI PLLs [1 or 2]). If these two clocks are not used, the HSDIVIDER functions are not required. In addition, the HSDIVIDER of the DSI1 PLL generates one more clock, PLL1_CLK4, which is used as bypass input for DSI2_PHY.

The CLKIN4DDR clocks are twice the data rate and four times the DSI output clock frequency. The DSI PLL factors must be calculated based on the required input and output frequencies, keeping the PLL internal reference frequency in the appropriate range:

- REGM factor is programed by the DSI_PLL_CONFIGURATION1[20:9] PLL_REGM bit field.
- REGN factor is programed by the DSI_PLL_CONFIGURATION1[8:1] PLL_REGN bit field.
- M4REG factor is programed by the DSI_PLL_CONFIGURATION1[25:21] M4_CLOCK_DIV bit field, and applies to PLLx_CLK1.
- M5REG factor is programed by the DSI_PLL_CONFIGURATION1[30:26] M5_CLOCK_DIV bit field, and applies to PLLx_CLK2.
- M7 factor is programed by the DSI_PLL_CONFIGURATION3[9:5] M7_CLOCK_DIV field, and applies to PLL1_CLK4.

Figure 10-152 shows the programming sequence.

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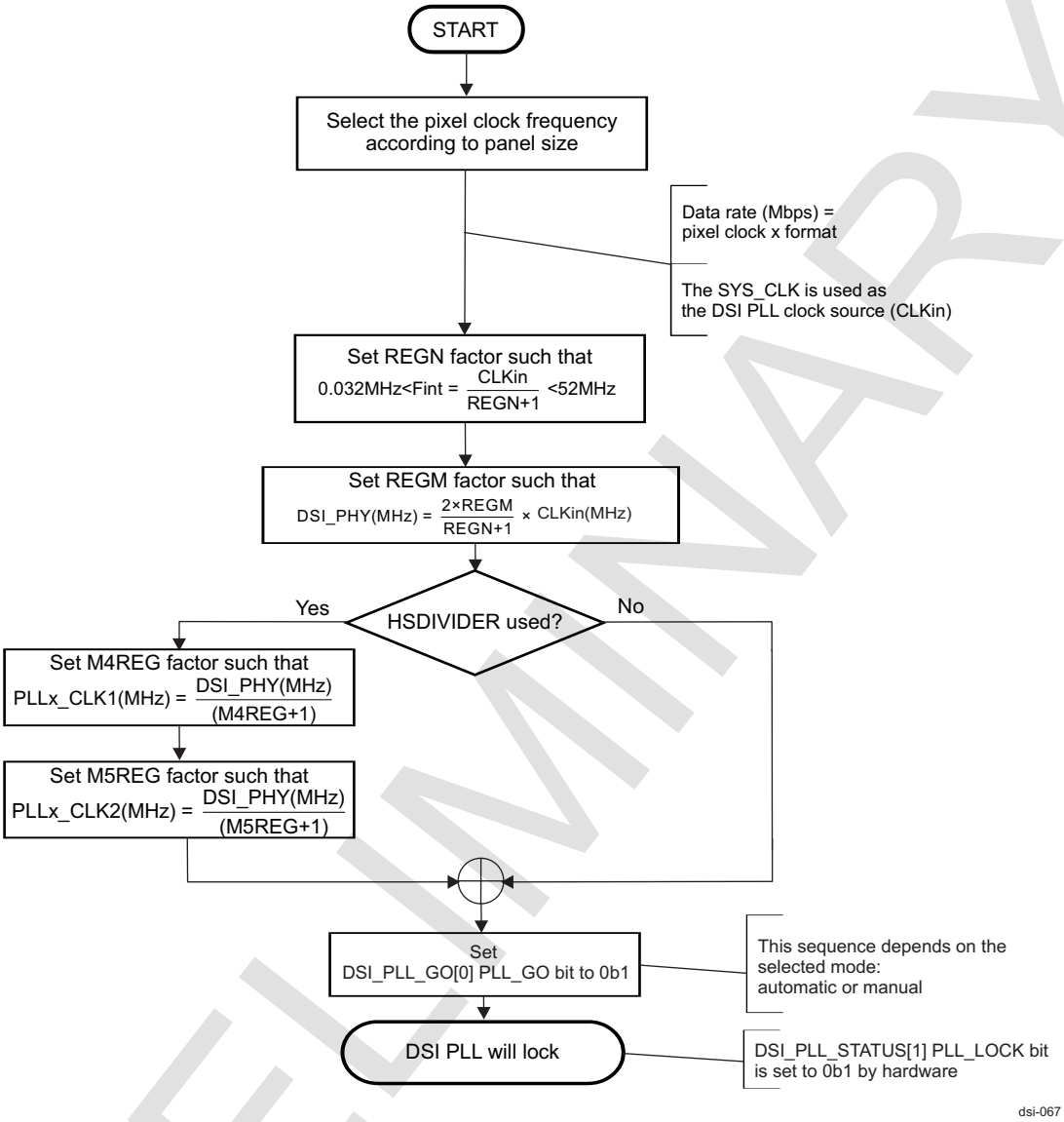
Figure 10-152. DSI PLL Programming Sequence



NOTE:

- The M4REG and M5REG factors must be set respecting the following conditions:
  - The PLLx_CLK1 frequency must be a multiple of PCLK frequency (for proper settings of the PCD and LCD factors in the DISPC).
  - The PLLx_CLK1 and PLLx_CLK2 frequencies must be lower than 186 MHz. For more information about clock frequency ratings, see Section 10.1.2.1, *DSS Clocks*.
- Most of the other DSI PLL programming values are available for software flexibility, but it is not recommended to update the values in normal use. For the recommended DSI PLL values, see Section 10.3.4.5.11, *DSI PLL Recommended Values*.

Table 10-494. Register Call Summary for DSI PLL Programming Sequence

Register Name	Register Name	Register Name
DSI_PLL_CONFIGURATION2	DSI_PLL_GO	DSI_PLL_STATUS

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10.3.4.5.10 DSI PLL Go Sequence

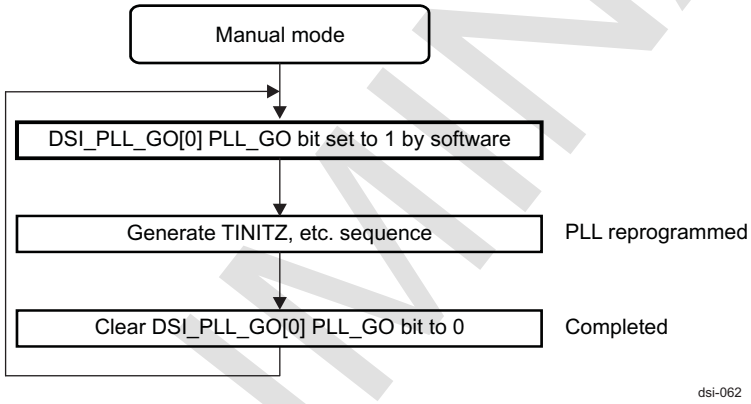
In manual mode (the DSI_PLL_CONTROL[0] PLL_AUTOMODE bit is set to 0), the DPLL requires a sequence on TINITZ, TENABLE, and TENABLEDIV to update the configuration values and start the locking sequence.

When all the configuration values are programmed into the registers, the GO bit must be set. The appropriate sequence is then sent on the TINITZ, TENABLE, and TENABLEDIV pins, respecting the timing requirements of the ADPLLM. The DSI_PLL_GO[0] PLL_GO bit is cleared to 0 at the end of the sequence.

The TENABLEDIV signal is shared with the HSDIVIDER module so that it is programmed at the same time. In this mode, software must deassert CLKINEN by unsetting the DSI_PLL_CONFIGURATION2[14] PHY_CLKINEN to 0 and assert HSDIVBYPASS correctly by setting the DSI_PLL_CONFIGURATION2[20] HSDIVBYPASS bit to 1 to prevent uncontrolled frequencies affecting DSI_PHY and the display subsystem during PLL locking. In manual mode, the shadow register is updated anyway so that valid values are present when later selecting automatic mode.

Figure 10-153 shows the DSI PLL Go flow chart in manual mode (the DSI_PLL_CONTROL[0] PLL_AUTOMODE bit is set to 0).

Figure 10-153. DSI PLL Go Sequence (Manual Mode)



(1) All thick-outlined blocks show operations performed by software. Other blocks show operations performed by hardware.

In automatic mode (the DSI_PLL_CONTROL[0] PLL_AUTOMODE bit is set to 1), the TINITZ, TENABLE, and TENABLEDIV sequence and the update of the PLL configuration from the DSI_PLL_CONFIGURATION2 register are deferred until the time of the front porch time signal sent by the DISPC module. This is intended to simplify the software to implement a configuration change (such as a frequency change to support a different link bandwidth). In this mode, CLKINEN, HSDIVBYPASS, and REFEN are automatically controlled and the register value is overridden.

Figure 10-154 shows the DSI PLL Go flow chart in automatic mode (the DSI_PLL_CONTROL[0] PLL_AUTOMODE bit is set to 1).

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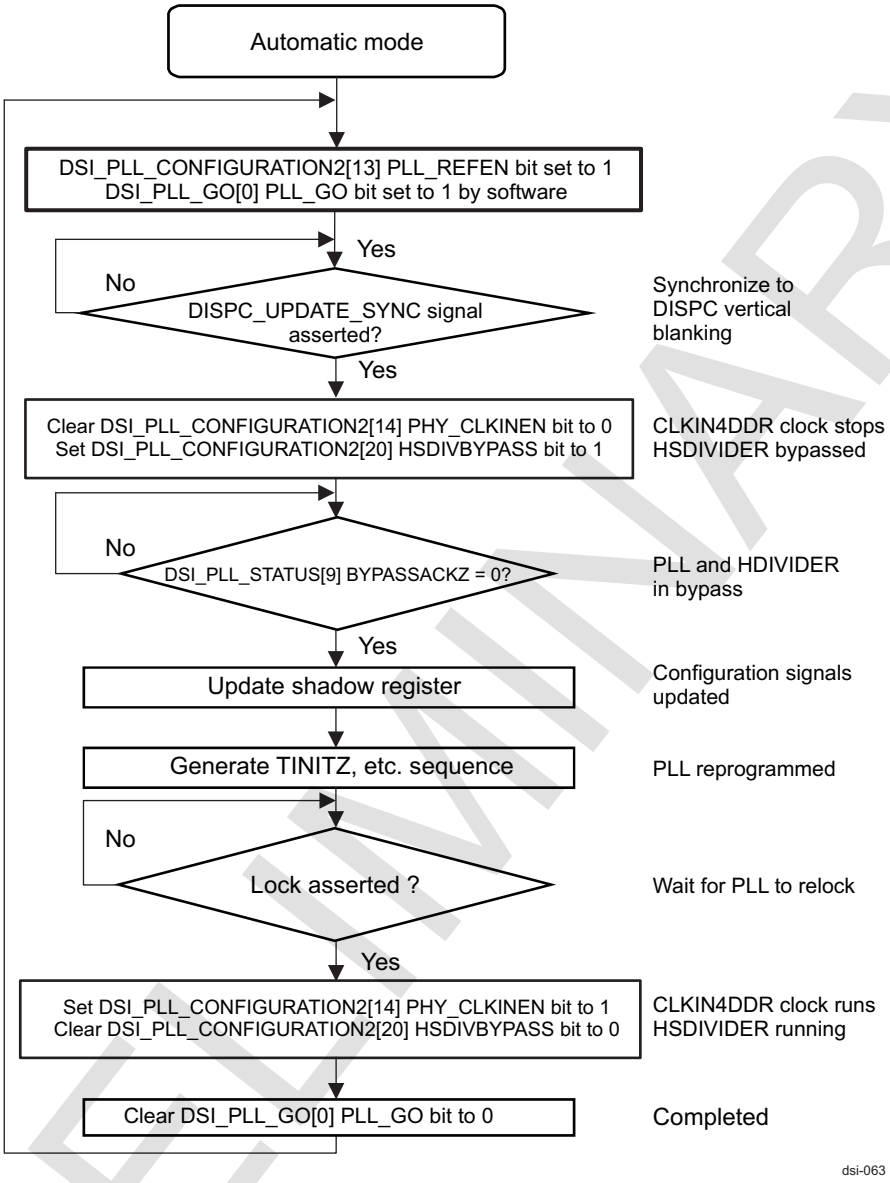
Figure 10-154. DSI PLL Go Sequence (Automatic Mode)



(1) All thick-outlined blocks show operations performed by software. Other blocks show operations performed by hardware.

Table 10-495. Register Call Summary for DSI PLL Go Sequence (Automatic Mode)

Register Name	Register Name	Register Name
DSI_PLL_CONFIGURATION2	DSI_PLL_STATUS	DSI_PLL_GO

10.3.4.5.11 DSI PLL Recommended Values

Table 10-496 shows the DSI PLL recommended values.

Table 10-496. Recommended Programming Values

Field Name	Value	Description
DSI_PLL_CONTROL[4] HSDIV_SYSRESET	0	Allow power FSM to control
DSI_PLL_CONTROL[3] PLL_SYSRESET	0	Allow power FSM to control

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Table 10-496. Recommended Programming Values (continued)

Field Name	Value	Description
DSI_PLL_CONTROL[2] PLL_HALTMODE	-	For information, see Section 10.3.4.5.8, *DSI PLL Clock-Gating Sequence*.
DSI_PLL_CONTROL[1] PLL_GATEMODE	-	For information, seeSection 10.3.4.5.8, *DSI PLL Clock-Gating Sequence*.
DSI_PLL_CONTROL[0] PLL_AUTOMODE	-	For information, see Section 10.3.4.5.8, *DSI PLL Clock-Gating Sequence*.
DSI_PLL_GO[0] PLL_GO	1 - 0	Write 1 when PLL is to be (re)locked with new parameters. This bit is cleared by hardware when the PLL request completes.
DSI_PLL_CONFIGURATION1[30:36] M5_CLOCK_DIV	See (1).	DSI protocol engine clock divider
DSI_PLL_CONFIGURATION1[25:21] M4_CLOCK_DIV	See (1).	DSS clock divider
DSI_PLL_CONFIGURATION1[20:9] PLL_REGM	See (1).	Feedback clock divider
DSI_PLL_CONFIGURATION1[8:1] PLL_REGN	See (2).	Reference clock divider
DSI_PLL_CONFIGURATION1[0] PLL_STOPMODE	1	Required to use the GATEMODE bit
DSI_PLL_CONFIGURATION2[20] HSDIVBYPASS	0	PLL controls HSDIVIDER bypass
DSI_PLL_CONFIGURATION2[19] M5_CLOCK_PWDN	0	If PLL/HSDIVIDER is used as the DSI protocol clock source
DSI_PLL_CONFIGURATION2[18] M5_CLK_EN	1	If PLL/HSDIVIDER is used as the DSI protocol clock source
DSI_PLL_CONFIGURATION2[17] M4_CLOCK_PWDN	0	If PLL/HSDIVIDER is used as the clock source
DSI_PLL_CONFIGURATION2[16] M4_CLOCK_EN	1	If PLL/HSDIVIDER is used as the clock source
DSI_PLL_CONFIGURATION2[15] BYPASSEN	0	To use PLL as the clock source. For small displays, it may be possible to use the display subsystem functional clock, DSS_CLK, in which case this bit must be set to 1. See Section 10.3.4.2, *DSI Clock Configuration*.
DSI_PLL_CONFIGURATION2[14] PHY_CLKINEN	1	Enable CLKIN4DDR clock
DSI_PLL_CONFIGURATION2[13] PLL_REFEN	1	Enable PLL reference
DSI_PLL_CONFIGURATION2[10:9] PLL_LOCKSEL	0x0	Phase lock criteria to lock the PLL
DSI_PLL_CONFIGURATION2[8] PLL_DRIFTGUARDEN	0x0	The RECAL status/interrupt must be used to decide when to perform a PLL uncalibration. No automatic uncalibration is performed
DSI_PLL_CONFIGURATION2[6] PLL_LOWCURRSTDBY	0/1	Set to 0 for fast PLL unlock, but higher standby current. Set to 1 for leakage level standby current, but longer unlock time.
DSI_PLL_CONFIGURATION2[5] PLLLPMODE	0	Normal operation. For smaller display sizes, it may be possible to set to 1.
DSI_PLL_CONFIGURATION2[0] PLL_IDLE	0	PLL active

(1) The value of the bit field must be set according to the desired clock frequency.
(2) The value of the bit field must be set according to the desired clock frequency.

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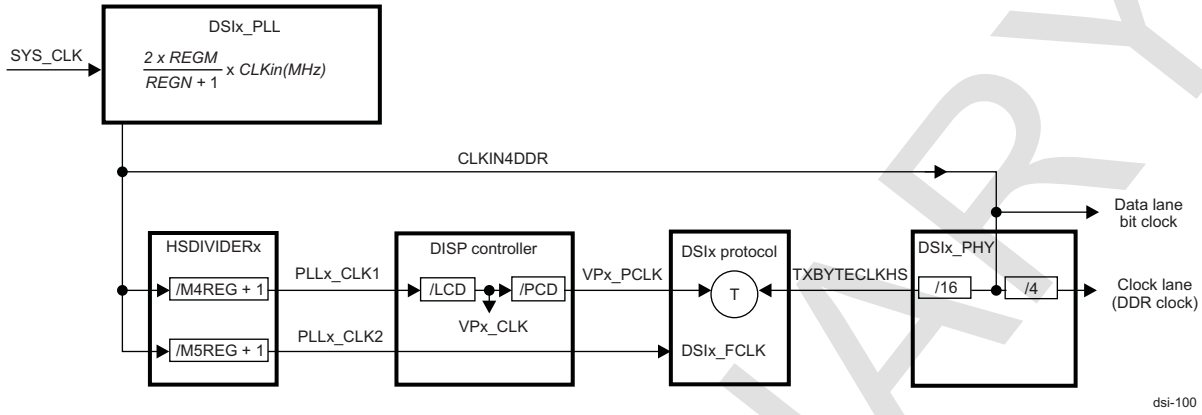
10.3.4.5.12 How to Configure the DSI PLL in Video Mode

Figure 10-155 is a global overview of the DSI1 and DSI2 clock trees when used in video mode.

Figure 10-155. DSI Clock Tree in Video Mode



The settings of the DSI PLL registers can be summarized by the following equations.

Equation 1

$$N \times T_{VP_CLK} = T_L \times T_{TXBYTECLKHS}$$

dsi-e101

where

- $T_L = T_{HS} + HSA_{DSI} + T_{HE} + HFP_{DSI} + ceiling((WC + 6) / NDL) + HBP_{DSI}$
- N is an integer.
- NDL: Number of data lanes
- WC: Word count or payload in bytes
- HSA_{DSI} is HSA period in video mode.
- HBP_{DSI} is HBP period in video mode.
- HFP_{DSI} is HFP period in video mode.

T_{HS} is the length of HSYNC start short packet in the number of byte clock cycles (TXBYTECLKHS).

- The generation of this packet can be enabled by setting the DSI_CTRL[17] VP_HSYNC_START bit to 1.
- T_{HS} is equal to ceiling(4 / NDL), if VP_HSYNC_START = 1; else, it is 0.

T_{HE} is the length of HSYNC end short packet in the number of byte clock cycles (TXBYTECLKHS).

- The generation of this packet can be enabled by setting the DSI_CTRL[18] VP_HSYNC_END bit to 1.
- T_{HE} is equal to 1, if (VP_HSYNC_START = 1, VP_HSYNC_END = 1, HSA_{DSI} = 0, and NDL = 3), else
- T_{HE} is equal to ceiling(4 / NDL), if (VP_HSYNC_START = 1 and VP_HSYNC_END = 1); else, it is 0.

NOTE: HSA_{DSI} timing is not used and does not have to be programmed when HE short packet is not generated.

Equation 2

$$R = T_{TXBYTECLKHS} / T_{VP_PCLK}$$

dsi-e102

To synchronize the DISPC and DSI protocol engines, users must follow the ratio R between TXBYTECLKHS and VP_PCLK, as listed in Table 10-497.

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Table 10-497. Ratio R

Number of Data Lanes (Up to 4 Data Lanes for DSI1) (Up to 2 Data Lanes for DSI2)	Pixel Format	Ratio R
1	16-bit pixel	1/2
1	18-bit pixel	4/9
1	24-bit pixel	1/3
2	16-bit pixel	1
2	18-bit pixel	8/9
2	24-bit pixel	2/3
3	16-bit pixel	3/2
3	18-bit pixel	4/3
3	24-bit pixel	1
4	16-bit pixel	2
4	18-bit pixel	16/9
4	24-bit pixel	4/3

All cases are covered by:

$$F_{VP_PCLK} \times bits_per_pixel = F_{TXBYTECLKHS} \times NDL \times 8$$

dsi-e110

Equation 3

$$(HSA_{DISPC} + HFP_{DISPC} + PPL + HBP_{DISPC}) \times T_{VP_PCLK} = (4/NDL + HFP_{DSI} + (WC + 6)/NDL + HBP_{DSI}) \times T_{TXBYTECLKHS}$$

dsi-e103

Equation 4

$$HFP_{DSI} = ((HFP_{DISPC} \times bits_per_pixel)/(NDL \times 8)) - (2 / NDL)$$

dsi-e109

Example

The desired performances are:

- Clock lane at 150 MHz
- RGB24-888
- 1-data lane
- LCD size 480 × 640 with $HSA_{DISP} = HFP_{DISP} = HBP_{DISP} = 20$, $VSA_{DISP} = VFP_{DISP} = VBP_{DISP} = 2$

Step 1. Determine REGM and REGN.

To obtain correct stability, F_{int} must be kept between 0.032 MHz and 52 MHz. In this case, F_{int} is maintained at 2 MHz. For more information, see Section 10.3.4.5.2, *DSI PLL Controllers Architecture*, Section 10.3.4.5.9, *DSI PLL Clock Sequence*, and Section 10.3.5.2.1.1, *Main Sequence – DSI PLL Setup*.

$$REGN = (F_{SYS_CLK}/F_{int}) - 1$$

$$REGN = 12$$

$$REGM = (REGN + 1) \times F_{CLKIN4DDR}/(2 \times F_{SYS_CLK})$$

$$REGM = 150$$

dsi-e113

where

- SYS_CLK = 26 MHz is used as a reference clock.

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Step 2. Determine VP_PCLK and TXBYTECLKHS clocks.

TXBYTECLKHS frequency is equal to 37.5 MHz. With ratio R equal to 1/3, VP_PCLK frequency is equal to 12.5 MHz. The frame rate can be estimated by:

$$\text{Frame rate} = F_{VP_PCLK} / \left(HSA_{DISPC} + HFP_{DISPC} + PPL + HBP_{DISPC}\right) \times \left(VSA_{DISPC} + LPP + VBP_{DISPC}\right)$$

$$\text{Frame rate} = 12.5\ \text{MHz} / \left(540\right) \times \left(646\right)$$

$$\text{Frame rate} = 35.83\ \text{frame/sec}$$

dsi-e123

Step 3. Determine LCD, PCD, and M4REG.

$$T_{CLKIN4DDR} = T_{TXBYTECLKHS} / 16 = T_{VP_PCLK} / \left(\left(M4REG + 1\right) \times LCD \times PCD\right)$$

$$\left(\left(M4REG + 1\right) \times LCD \times PCD\right) = 16 \times 3$$

dsi-e115

If LCD and PCD are set to 1 and 3, respectively, M4REG is equal to 15.

Step 4. Verify N as integer.

First, TL must be determined:

$$\left(HSA_{DISPC} + HFP_{DISPC} + PPL + HBP_{DISPC}\right) \times T_{VP_PCLK} / T_{TXBYTECLKHS} = T_L = 1620$$

dsi-e116

From **Equation 1** follows:

$N \times T_{VP_CLK} = T_L \times T_{TXBYTECLKHS}$

$N = T_{TXBYTECLKHS} \times T_L / T_{VP_CLK} = T_L / (R \times PCD)$

$N = 14580$

N is an integer.

Step 5. Determine HFP and HBP of the DSI protocol engine.

From **Equation 3** follows:

$$\left(\left(HSA_{DISPC} + HFP_{DISPC} + PPL + HBP_{DISPC}\right) \times T_{VP_PCLK} / T_{TXBYTECLKHS}\right) - \left(4 / NDL + \left(WC + 6\right) / NDL\right) = HFP_{DSI} + HBP_{DSI}$$

$$HFP_{DSI} + HBP_{DSI} = 170$$

dsi-e117

From **Equation 4** follows:

$$HFP_{DSI} = \left(\left(HFP_{DISP} \times bits_per_pixel\right) / NDL \times 8\right)\right) - \left(2 / NDL\right)$$

$$HFP_{DSI} = 58$$

$$HBP_{DSI} = 170 - 58 = 112$$

dsi-e121

10.3.4.6 DSI Complex I/O

10.3.4.6.1 DSI Complex I/O Overview

DSI_PHY is a complex I/O with five unidirectional (HS) lane modules. This includes four data lane modules and one clock lane module. Each lane module has two data pads (DX, DY). These data pads are connected with a complementary lane module on the DSI receiver device using a point-to-point interconnect.

Lane modules support HS burst mode. Forward direction and reverse direction escape modes are also supported. Escape modes can be used for low-power data transmission, among other things.

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The maximum data rate supported in HS mode is 824 Mbps for four data lanes, and 900 Mbps for up to three data lanes. The lane module function and position are configurable; that is, any lane module can be chosen as a clock lane module, and the DX/DY data pad for each lane module can be configured as a DP or DN pin defined by the D-PHY specification.

DSI_PHY interacts with the higher layers of the DSI link through the PPI. DSI_PHY does not include a PLL; a high-frequency clock input is expected in HS mode (CLKIN4DDR). DSI_PHY also supports the SCP interface to set various configuration and control registers.

10.3.4.6.2 Software Reset

The clock domain using the TXBYTECLKHS byte clock from the DSI complex I/O has dedicated reset-done information in the DSI_COMPLEXIO_CFG1[29] RESET_DONE bit. The DSI_SYSCONFIG[1] SOFT_RESET bit is used to reset the byte clock power domain. A dummy read using the SCP interface to any DSI_PHY register is required after DSI_PHY reset to complete the reset of the DSI complex I/O.

10.3.4.6.3 Reset-Done Bits

The DSI complex I/O has several clock domains. The reset status for each clock domain is provided in the DSI_PHY_REGISTER5 register:

- DSI_PHY_REGISTER5[31] RESETDONETXBYTECLK bit: Reset done for the TXBYTECLK domain.
- DSI_PHY_REGISTER5[28:24] RESETDONETXCLKESCi bit field: Reset done for the TXCLKESC domain for lane i (where i = 0 to 4).
- DSI_PHY_REGISTER5[30] RESETDONESCPCLK bit: Reset done for the SCP clock domain. Software users must perform a dummy read on this bit to initiate the reset sequence of the SCP FSM. When the reset sequence completes, the RESETDONESCPCLK signal goes high, and software users can read again the DSI_PHY_REGISTER5[30] RESETDONESCPCLK bit to ensure that the value is now 1.

NOTE: Software must not write in the DSI_PHY SCP registers before the DSI_PHY_REGISTER5[30] RESETDONESCPCLK bit is set to 1.

- DSI_PHY_REGISTER5[29] RESETDONEPWRCLK bit: Reset done for the PWR clock domain. The reset sequence of the PWR FSM is complete when the RESETDONEPWRCLK signal goes high.

10.3.4.6.4 Pad Configuration

The number of lanes is configurable through the DSI_COMPLEXIO_CFG1 register.

It is not allowed to change on the fly the position (by modifying the DATAx_POSITION, where x = 1 through 4, and CLOCK_POSITION fields), the P/N order (positive/negative order of the differential pair by modifying the DATAy_POL, where y = 1 through 4, and CLOCK_POL), or the number of active data lanes (by modifying the DSI_COMPLEXIO_CFG1[10:8] DATA2_POSITION, DSI_COMPLEXIO_CFG1[14:12] DATA3_POSITION, and DSI_COMPLEXIO_CFG1[18:16] DATA4_POSITION bit fields). To add or remove lanes 2, 3, or 4, it is required to be in OFF mode for the DSI complex I/O.

The configuration of the DSI complex I/O (number of data lanes, position, differential order) must not be changed while the DSI_CLK_CTRL[20] LP_CLK_ENABLE bit is set to 1. For hardware to recognize a new configuration of the complex I/O (done in the DSI_COMPLEXIO_CFG1 register), the following sequence shall be followed:

1. Set the DSI_CTRL[0] IF_EN bit to 1.
2. Reset the DSI_CTRL[0] IF_EN bit to 0.
3. Set DSI_CLK_CTRL[20] LP_CLK_ENABLE bit to 1.
4. Set again the DSI_CTRL[0] IF_EN bit to 1.

If the sequence is not followed, the DSI complex I/O configuration is undetermined.

The minimum requirement for the number of lanes is one clock lane and one data lane. By default, data lanes 2, 3, and 4 are not connected (the reset value of the DATAx_POSITION bit fields is 0).

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10.3.4.6.5 Display Timing Configuration

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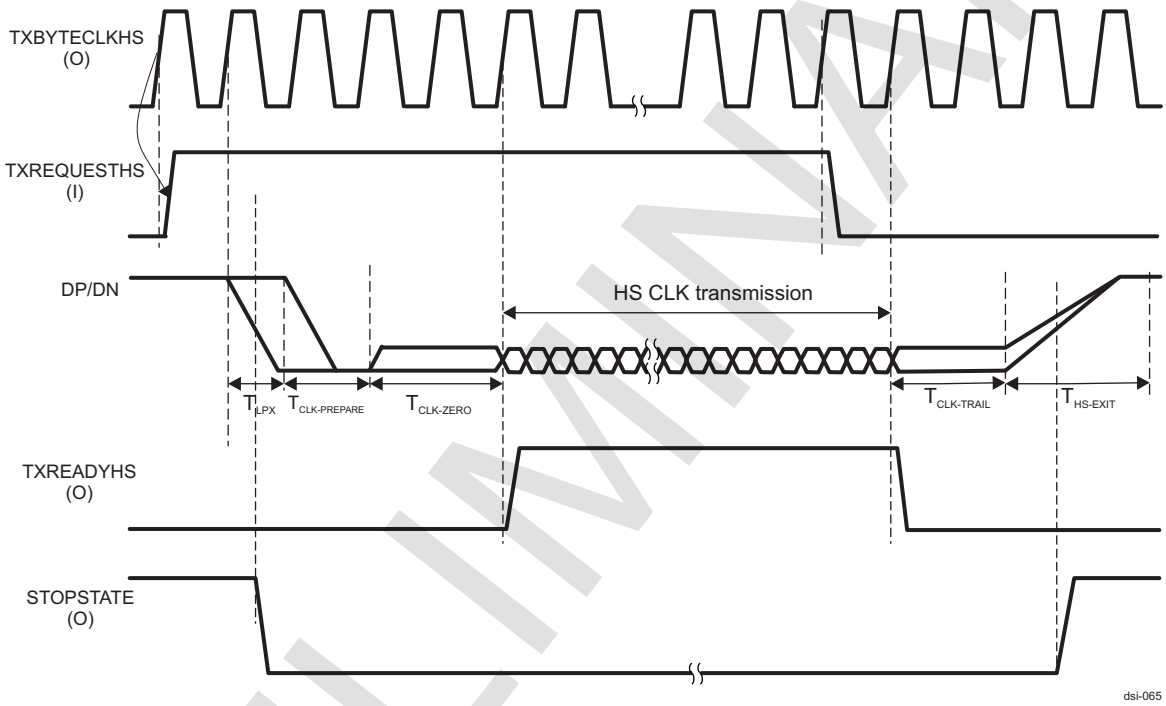
Depending on the CLKIN4DDR clock frequency settings programmed with the DSI PLL control module, software users must program accordingly the timing parameters in the DSI complex I/O registers.

10.3.4.6.5.1 High-Speed Clock Transmission

Figure 10-156 shows an example of HS clock transmission.

Figure 10-156. HS Clock Transmission



TXBYTECLKHS is an output clock that is derived by dividing CLKIN4DDR by 16.
The TXBYTECLKHS clock is driven by DSI_PHY when:

- The CLKIN4DDR is running and DSI_PLL_CONFIGURATION2[14] PHY_CLKINEN bit is set to '1'.
- DSI_PHY is in ON power state (DSI_COMPLEXIO_CFG1[28:27] PWR_CMD bit = 1) and at least one lane is enabled.

To begin transmission, the protocol drives TXREQUESTHS high on a rising edge of TXBYTECLKHS. The PHY detects this signal on the next rising edge, after which it initiates the LP SoT procedure.

During an HS clock transmission, these parameters are defined in multiples of CLKIN4DDR and are programmed by the following bit fields:

- TLPX timing is programmed by DSI_PHY_REGISTER1[20:16] TLPXBY2.
- THS-PREPARE timing is programmed by DSI_PHY_REGISTER0[31:24] THSPREPARE.
- TCLK-ZERO timing is programmed by DSI_PHY_REGISTER1[7:0] TCLKZERO.

TCLK-ZERO is extended, if required, so that the entire LP SoT procedure lasts an integer number of TXBYTECLKHS cycles.

At the end of the SoT procedure, HS clock transmission begins. At the same time, TXREADYHS is made high.

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To stop clock transmission, the protocol drives TXREQUESTHS low on a rising edge of TXBYTECLKHS. The DSI_PHY detects this change in TXREQUESTHS on the next edge and stops clock transmission. TXREADYHS is made low.

The DSI_PHY then goes through the LP EoT procedure. The TCLK-TRAIL and THS-EXIT parameters are also multiples of CLKIN4DDR and are programmed by the following bit fields:

- TCLK-TRAIL timing is programmed by DSI_PHY_REGISTER1[15:8] TCLKTRAIL.
- THS-EXIT timing is programmed by DSI_PHY_REGISTER0[7:0] THSEXIT.

The DSI_PHY completes the SoT and EoT procedures, once begun, regardless of any change in the PPI signals. If TXREQUESTHS goes low during the SoT procedure, the PHY starts the EoT procedure immediately after finishing the SoT procedure and no clock is transmitted.

STOPSTATE is high whenever the line is in LP-11 state, as determined by the outputs of the low-power receivers. This signal is not synchronized with TXBYTECLKHS.

The HS clock must be present for a period of time before (TCLK-PRE) and after (TCLK-POST) HS data transmission. The protocol must ensure that these timings are met by asserting and deasserting TXREQUESTHS appropriately.

The PHY ensures that the clock signal has a quadrature phase with respect to a toggling bit sequence on any data lane, and a rising edge in the center of the first transmitted bit of each data byte. These relations are not described in the timing diagram.

CLKIN4DDR can be shut off 300 ns after the clock lane goes to STOPSTATE. Alternatively, CLKIN4DDR can be shut down after TCLK-Trail + THS-Exit + 2 Txbyteclk periods after the TxRequestHS falling edge is received by DSI_PHY.

The DSI protocol engine must ensure that TXREQUESTESC, TXULPSCLK, and TURNREQUEST are low whenever TXREQUESTHS is asserted.

10.3.4.6.5.2 High-Speed Data Transmission

Figure 10-157 shows an example of HS data transmission.

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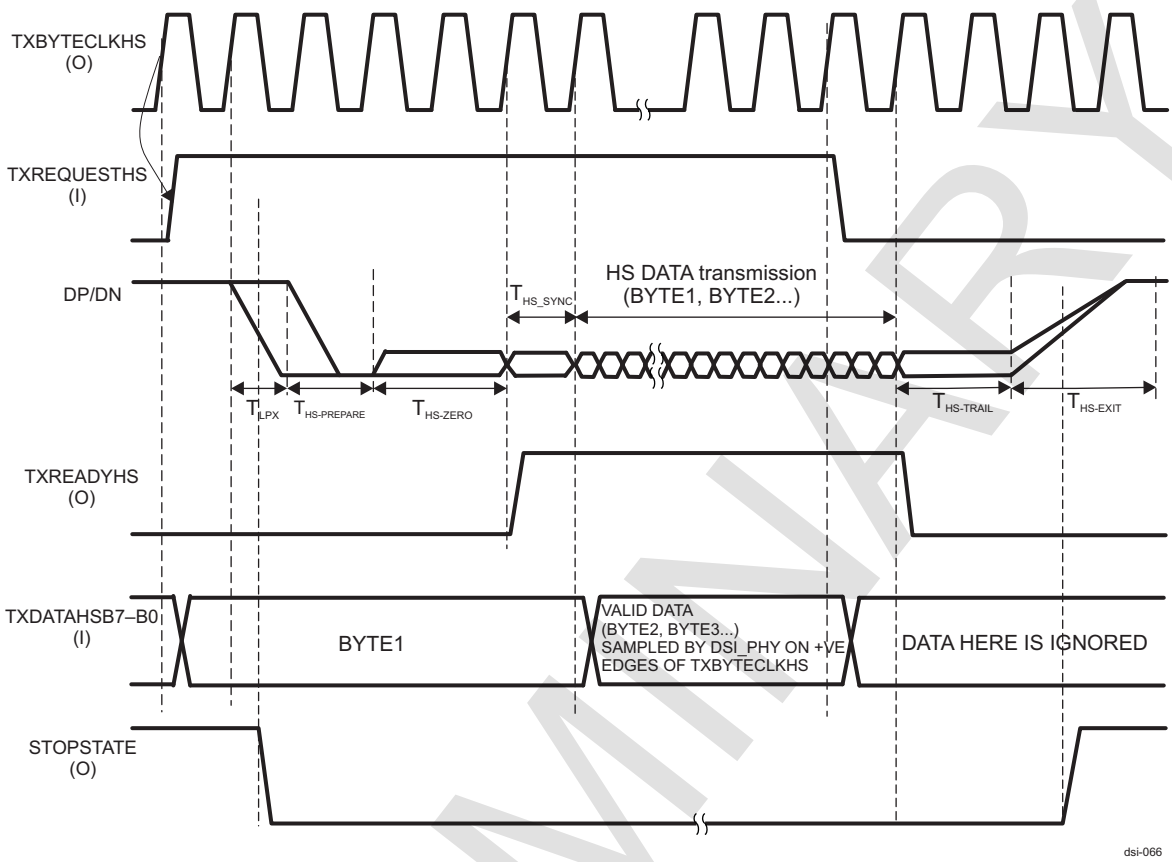
Figure 10-157. HS Data Transmission



To begin transmission, the protocol drives TXDATAHS with the first byte of data on a rising edge of TXBYTECLKHS. It also makes TXREQUESTHS high on the same rising edge. The PHY detects TXREQUESTHS going high on the next rising edge of TXBYTECLKHS, following which it initiates the LP SoT procedure.

During an HS data transmission, these timings are multiples of CLKIN4DDR and are programmed by the following bit fields:

- TLPX timing is programmed by DSI_PHY_REGISTER1[20:16] TLPXBY2.
- THS-PREPARE + THS-ZERO timing is programmed by DSI_PHY_REGISTER0[23:16] THSPRPR_THSZERO.

THS-ZERO is extended, if required, so that the entire LP SoT procedure lasts an integer number of TXBYTECLKHS cycles. THS-SYNC corresponds to the length of the sync pattern (8 HS bits), and can be configured through the DSI_PHY_REGISTER2[31:24] HSSYNCPATTERN bit field.

Toward the end of the SoT procedure, the PHY makes TXREADYHS high on a positive edge of TXBYTECLKHS and then starts accepting data from TXDATAHS from the next positive edge onward. The protocol is expected to provide (new) valid data on TXDATAHS on every positive edge of TXBYTECLKHS if TXREADYHS is high.

At the end of the SoT procedure, HS data transmission begins. HS data transmission happens LSB first.

To stop data transmission, the protocol drives TXREQUESTHS low on a rising edge of TXBYTECLKHS. The PHY detects this change in TXREQUESTHS on the next edge and stops data transmission. TXREADYHS is made low and data on TXDATAHS, from that point, is ignored.

The PHY then goes through the LP EoT procedure. THS-TRAIL and THS-EXIT are also multiples of CLKIN4DDR and are programmed by the following bit fields:

- THS-TRAIL timing is programmed by DSI_PHY_REGISTER0[15:8] THSTRAIL.

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- THS-EXIT timing is programmed by DSI_PHY_REGISTER0[7:0] THSEXIT.

The PHY completes the SoT and EoT procedures, once begun, regardless of any change in PPI signals. If TXREQUESTHS goes low during the SoT procedure, the PHY starts the EoT procedure immediately after finishing the SoT procedure and no data is transmitted.

STOPSTATE is high whenever the line is in LP-11 state, as determined by the outputs of the low-power receivers. This signal is not synchronized with TXBYTECLKHS.

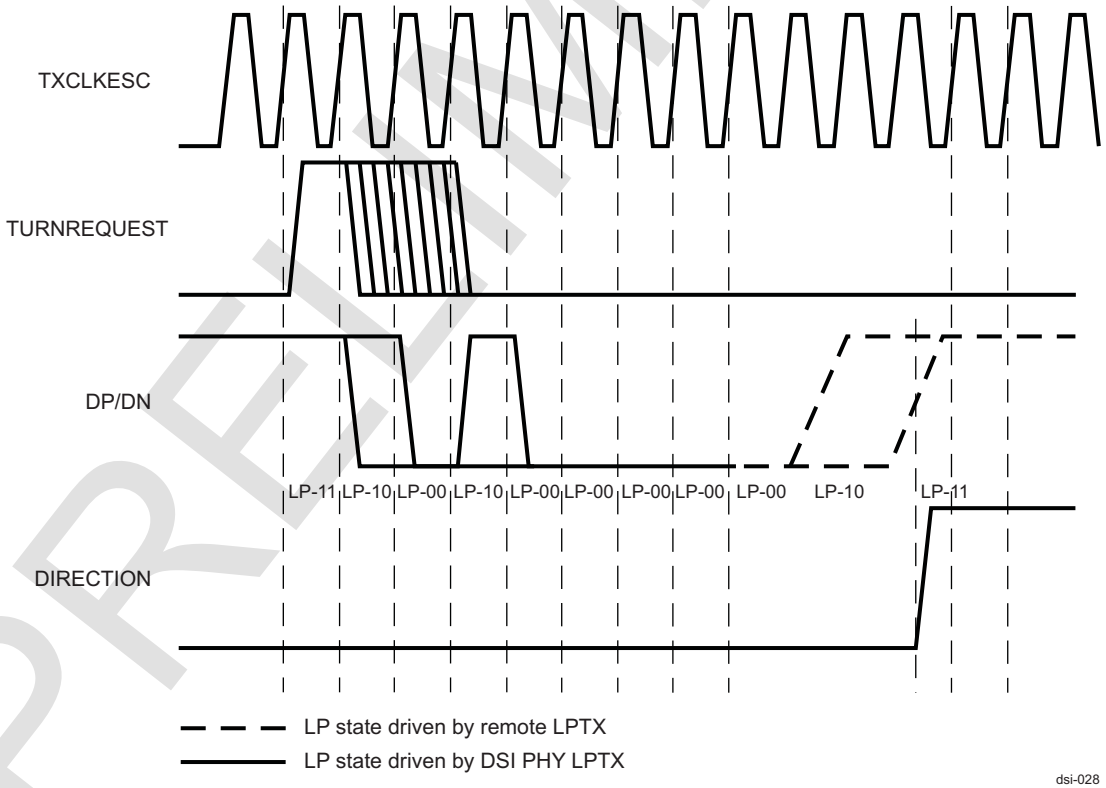
The protocol must ensure that TXREQUESTESC, TXULPSCLK, and TURNREQUEST are low whenever TXREQUESTHS is asserted.

10.3.4.6.5.3 Turnaround Request in Transmit Mode

When the DSI PHY is in transmit mode, the DSI protocol engine can request a turnaround by making the TurnRequest signal high for at least one clock cycle of TxClkEsc (see Section 10.3.4.4.7.3, *TurnRequest FSM*).

The DSI PHY transmits the turnaround request pattern (LP 11-10-00-10-00-00-00-00) (see Figure 10-158). The number of 00 states at the end of the pattern is defined by the T_{TA-GO} timing parameter and is programmable through the DSI_PHY_REGISTER1[31:29] REG_TTAGO bit field, in number of TxClkEsc clocks. Following the transmission of the pattern, the DSI PHY disables its LP transmitters and waits for an acknowledgment from the remote device. The remote device detects the turnaround request and acknowledges it by driving LP 10, followed by the STOP state. When this acknowledgment is received (BTA_IRQ is asserted, as described in Section 10.3.4.4.8, Bus Turnaround), the DSI PHY switches to receive mode and indicates the completion of the turnaround procedure by changing the direction (BTA_EN = 0).

Figure 10-158. Turnaround Request in Transmit Mode



The DSI protocol engine must not stop TxClkEsc after the turnaround process completes (the DSI_CLK_CTRL[20] LP_CLK_ENABLE bit must be kept at 1), because TxClkEsc is also used in handling a turnaround request transmitted by a remote slave device (see Section 10.3.4.6.5.4, *Turnaround Request in Receive Mode*).

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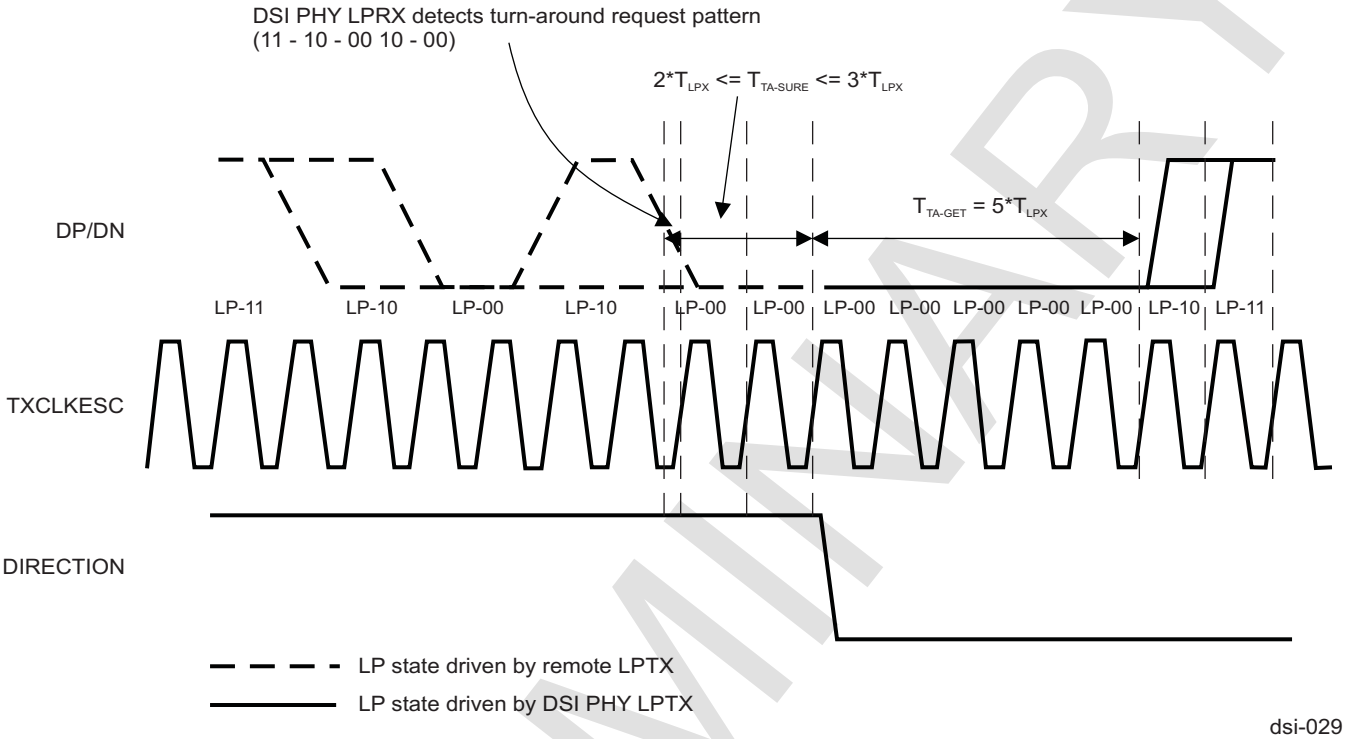
10.3.4.6.5.4 Turnaround Request in Receive Mode

When DSI PHY is in receive mode, an LP pattern of 11-10-00-10-00 on DP/DN lines indicates a turnaround request from the remote device (see Figure 10-159).

Figure 10-159. Turnaround Request in Receive Mode



dsi-029

If the line stays in LP-00 for a time $T_{TA-SURE}$, the DSI PHY accepts the turnaround request, changes the direction, transmits LP-00 for a time T_{TA-GET}, and then transmits the acknowledgment pattern LP-10, followed by the STOP state.

This completes the turnaround procedure. The $T_{TA-SURE}$ and T_{TA-GET} timing parameters are programmable through DSI_PHY_REGISTER1 in number of TxClkEsc clocks:

- $T_{TA-SURE}$ can be configured in the [28:27] REG_TTASURE bit field.
- T_{TA-GET} can be configured in the [26:24] REG_TTAGET bit field.

10.3.4.6.5.5 Other DSI PHY Transmission and Reception

The timings of the following sequences defined in the DSI_PHY protocol cannot be programed by the user:

- Low-power data transmission
- Escape mode trigger command transmission
- ULPS command transmission on data lanes
- ULPS transmission on clock lane
- Low-power data in receive mode
- Low-power trigger in receive mode
- ULPS command on clock lane in receive mode
- ULPS command on data lane in receive mode

10.3.4.6.6 Power Management

Power management of the DSI_PHY analog circuitry is done through the internal power FSM, which is controlled by the subsystem. The control interface is a basic command and acknowledge protocol. The

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subsystem is the master of the interface. There is a dedicated command pin for each power state of DSI_PHY and a common acknowledge pin. The subsystem sends the power command and clock. The internal FSM does the sequencing and control generation of internal power domains. It then asserts the acknowledge, which signals the completion of the power state transition. The internal power control FSM is powered by a constant power supply.

The main features of the power control interface are:

- One dedicated command line per power state
- Only one command line can be asserted at a time.
- One acknowledge signal common to all command lines
- The command line cannot be cleared unless the acknowledge has been returned.
- All the command lines and the acknowledge signal must be cleared before triggering a new command.

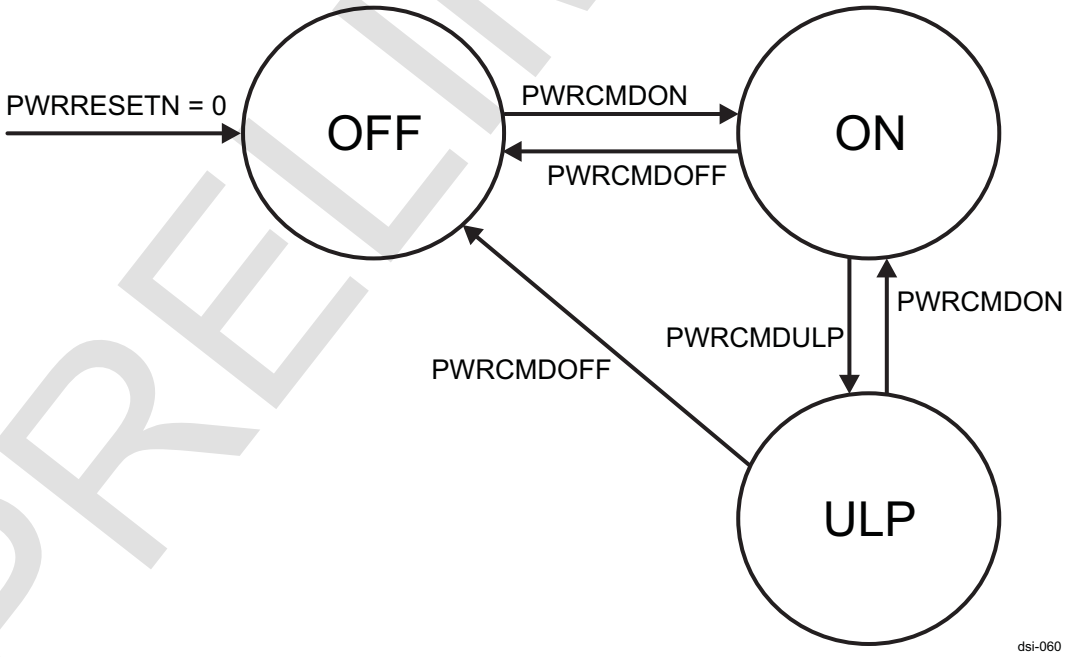
DSI_PHY supports three power states:

- OFF/GPIO mode (OFF): The entire analog circuit is powered down. Internal LDO is OFF. All analog circuitry on 1.8-V supply is powered down. The ULPS exit detection circuit power switch is OFF. DSI_PHY takes leakage level current.
- ON: Complete analog circuit is powered on and functional. LDO is ON. (DSI_PHY calibrates every time the module enters power on state.)
- ULPS: Only the DSI_PHY mode ULPS exit detection circuit power switch is ON. All the other analog circuitry is switched OFF. LDO is OFF.

NOTE: ULPS must be entered only when all used lane modules go into ULPS state. PHY power state must be returned to ON power state when any one of the used modules goes out of ULPS. No PPI signal except TXULPSEXIT must be toggled when in this power state.

Figure 10-160 shows the power states of the DSI complex I/O

Figure 10-160. Power State Diagram



10.3.4.6.7 Error Handling

A dedicated register for the DSI complex I/O (DSI_COMPLEXIO_IRQSTATUS) indicates the state of each error provided by the DSI complex I/O error signals. The DSI_PHY reports the following errors:

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- DSI_COMPLEXIO_IRQSTATUS[9:5] ERRESCi_IRQ: ERRESC is asserted if an unrecognized Escape entry command is received. This remains high until the next change in the line state.
- DSI_COMPLEXIO_IRQSTATUS[4:0] ERRSYNCESCi_IRQ: If the number of bits received during a low-power data transmission is not a multiple of 8 when the transmission ends, ERRSYNCESC is made high and remains high until the next change in line state.
- DSI_COMPLEXIO_IRQSTATUS[14:10] ERRCONTROLi_IRQ: ERRCONTROL is asserted if an incorrect line state sequence is detected. For example, if a turnaround request or escape mode request is immediately followed by a STOP state instead of the required BRIDGE state, this signal is asserted and remains asserted until the next change in the line state.
- DSI_COMPLEXIO_IRQSTATUS ERRCONTENTIONLP0_i_IRQ: ERRCONTENTION0LPDX and ERRCONTENTION0LPDY are asserted when the lane module detects a contention situation on lines DX and DY, respectively, while trying to drive the lines low. Contention is detected only if it lasts at least 50 ns.
- DSI_COMPLEXIO_IRQSTATUS ERRCONTENTIONLP1_i_IRQ: ERRCONTENTION1LPDX and ERRCONTENTION1LPDY are asserted when the lane module detects a contention situation on lines DX and DY, respectively, while trying to drive the lines high. Contention is detected only if it lasts at least 50 ns.

The ULPSACTIVENOT signal goes low, which indicates to the protocol that the PHY has entered ULPS. When all the ULPSActiveNot signals are low, the DSI_COMPLEXIO_IRQSTATUS[30] ULPSACTIVENOT_ALL0_IRQ event is generated. When all the ULPSActiveNot signals are high, the DSI_COMPLEXIO_IRQSTATUS[31] ULPSACTIVENOT_ALL1_IRQ event is generated.

When any of the events defined in the DSI_COMPLEXIO_IRQSTATUS register happen, the DSI_IRQSTATUS[10] COMPLEXIO_ERR_IRQ bit is set to 1 at DSI protocol engine level.

Table 10-498 lists the DSI complex I/O interrupt events.

Table 10-498. DSI Complex I/O Interrupts

IRQ Name	Description
ULPSActiveNot_ALL0_IRQ	All the ULPSActiveNOT signals are 0.
ULPSActiveNot_ALL1_IRQ	All the ULPSActiveNOT signals corresponding to the lanes with TXULPSExit being high are high.
STATEULPM5_IRQ	Lane 5 in ULPS
STATEULPM4_IRQ	Lane 4 in ULPS
STATEULPM3_IRQ	Lane 3 in ULPS
STATEULPM2_IRQ	Lane 2 in ULPS
STATEULPM1_IRQ	Lane 1 in UlLPS
ERRCONTROL5_IRQ	Control error for lane 5
ERRCONTROL4_IRQ	Control error for lane 4
ERRCONTROL3_IRQ	Control error for lane 3
ERRCONTROL2_IRQ	Control error for lane 2
ERRCONTROL1_IRQ	Control error for lane 1
ERRESC5_IRQ	Escape entry error for lane 5 (edge trigger interrupt)
ERRESC4_IRQ	Escape entry error for lane 4 (edge trigger interrupt)
ERRESC3_IRQ	Escape entry error for lane 3 (edge trigger interrupt)
ERRESC2_IRQ	Escape entry error for lane 2 (edge trigger interrupt)
ERRESC1_IRQ	Escape entry error for lane 1(edge trigger interrupt)
ERRCONTENTIONLP1_1_IRQ	Contention LP1 error for lane 1
ERRCONTENTIONLP0_1_IRQ	Contention LP0 error for lane 1
ERRCONTENTIONLP1_2_IRQ	Contention LP1 error for lane 2
ERRCONTENTIONLP0_2_IRQ	Contention LP0 error for lane 2
ERRCONTENTIONLP1_3_IRQ	Contention LP1 error for lane 3
ERRCONTENTIONLP0_3_IRQ	Contention LP0 error for lane 3
ERRCONTENTIONLP1_4_IRQ	Contention LP1 error for lane 4

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Table 10-498. DSI Complex I/O Interrupts (continued)

IRQ Name	Description
ERRCONTENTIONLP0_4_IRQ	Contention LP0 error for lane 4
ERRCONTENTIONLP1_5_IRQ	Contention LP1 error for lane 5
ERRCONTENTIONLP0_5_IRQ	Contention LP0 error for lane 5
ERRSYNCESC5_IRQ	Low-power data transmission synchronization error for lane 5
ERRSYNCESC4_IRQ	Low-power data transmission synchronization error for lane 4
ERRSYNCESC3_IRQ	Low-power data transmission synchronization error for lane 3
ERRSYNCESC2_IRQ	Low-power data transmission synchronization error for lane 2
ERRSYNCESC1_IRQ	Low-power data transmission synchronization error for lane 1

Software must take appropriate action when receiving the interrupt indicating the error from the complex I/O. The action can be:

- Reset the DSI protocol engine module
- Reset the peripheral through the reset trigger or directly driving the hardware reset pin of the display module
- Ignore the error

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10.3.5 DSI Programming Model

This section describes the low-level hardware programming sequences for the configuration and use of the DSI module.

10.3.5.1 DSI Global Initialization

10.3.5.1.1 Surrounding Modules Global Initialization

This section describes the requirements to initialize the surrounding modules when the DSI module is to be used for the first time after a device reset. This initialization of surrounding modules is based on the integration and environment of the DSI. For more information, see Section 10.3.3, *DSI Integration*, and Section 10.3.2, *DSI Environment* .

Table 10-499 describes the global initialization of the surrounding modules.

Table 10-499. Global Initialization of Surrounding Modules

Surrounding Modules	Comments
PRCM	DSI module interface and functional clocks must be enabled. The module power management (idle and sleep modes) must be configured. For more information, see Chapter 3, *Power, Reset, and Clock Management* .
MPU INTC	MPU interrupt controller (INTC) configuration must be done to enable interrupts from the DSI module. For more information about the module configuration, see Chapter 17, *Interrupt Controllers*.
DSP INTC	DSP INTC configuration must be done to enable interrupts from the DSI module. For more information about the module configuration, see Chapter 5, *DSP Subsystem*
sDMA	DMA configuration must be done to enable DSI module DMA channel requests. For more information about the configuration, see Chapter 16, *sDMA* .
L3 / L4_PER Interconnect	For information about the interconnect configuration, see Chapter 13, *Interconnect*.

10.3.5.1.2 DSI Global Initialization

10.3.5.1.2.1 Main Sequence - DSI Global Initialization

This procedure initializes the DSI after a power on or software reset.

Table 10-500 summarizes the DSI global initialization.

Table 10-500. DSI Global Initialization

Steps	Registers	Value
Reset IRQ status.	DSI_IRQSTATUS[31:0]	0x0
Set clock activity.	DSI_SYSCONFIG[9:8] CLOCKACTIVITY	x
Configure power management.	DSI_SYSCONFIG[4:3] SIDLEMODE	x
Reset DSI protocol engine.	DSI_SYSCONFIG[1] SOFT_RESET	0x1
Wait until five reads of reset status?	Software test condition	
Read reset status.	DSI_SYSSTATUS[0] RESET_DONE	
IF: Is reset ongoing?	DSI_SYSSTATUS[0] RESET_DONE	= 0x0
Error occurred during reset stage(1)		
ENDIF		

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10.3.5.2 DSI Operational Modes Configuration

10.3.5.2.1 DSI Video Mode Using the DISPC Video Port

10.3.5.2.1.1 Main Sequence - DSI PLL Setup

Table 10-501 lists the steps required to configure DSI PLL.

Table 10-501. DSI PLL Configuration Registers

Steps	Registers	Value
Turn ON/OFF the PLL and HSDIVIDER.	DSI_CLK_CTRL[31:30] PLL_PWR_CMD	x
Wait until the status of the PLL is set (value according to the previous step)?	DSI_CLK_CTRL[29:28] PLL_PWR_STATUS	= x
Set the divider value for DSI protocol engine clock source M5REG.	DSI_PLL_CONFIGURATION1[30:26] M5_CLOCK_DIV	x
Set the divider value for clock source M4REG.	DSI_PLL_CONFIGURATION1[25:21] M4_CLOCK_DIV	x
Set the value for M divider for PLL.	DSI_PLL_CONFIGURATION1[20:9] DSI_PLL_REGM	x
Set the value for N divider for PLL.	DSI_PLL_CONFIGURATION1[8:1] DSI_PLL_REGN	x
Enable/disable PLL STOPMODE.	DSI_PLL_CONFIGURATION1[0] PLL_STOPMODE	x
Enable/disable DSI protocol engine clock divider.	DSI_PLL_CONFIGURATION2[18] M5_CLOCK_EN	x
Enable/disable M4 clock source divider.	DSI_PLL_CONFIGURATION2[16] M4_CLOCK_EN	x
Enable/disable DSI PHY clock.	DSI_PLL_CONFIGURATION2[14] PHY_CLKINEN	x
Enable/disable PLL reference clock.	DSI_PLL_CONFIGURATION2[13] PLL_REFEN	x
Set PLL automatic update mode.	DSI_PLL_CONTROL[0] PLL_AUTOMODE	x
Request PLL locking sequence.	DSI_PLL_GO[0] PLL_GO	0x1
Read until PLL_GO bit = 0?	DSI_PLL_GO[0] PLL_GO	= 0x0
Wait until PLL is locked?	DSI_PLL_STATUS[1] PLL_LOCK	= 0x1
Set the ratio for the LP clock.	DSI_CLK_CTRL[12:0] LP_CLK_DIVISOR	x
Enable/disable DSS_L3_ICLK clock gating to DSI_PHY and PLL module.	DSI_CLK_CTRL[14] CIO_CLK_ICG	x
Enable/disable the automatic assertion/deassertion of DSIStopClk.	DSI_CLK_CTRL[18] HS_AUTO_STOP_ENABLE	x
Configure the DSI functional clock synchronization and clock speed.	DSI_CLK_CTRL[21] LP_RX_SYNCHRO_ENABLE	x
Turn ON/OFF PLL and HSDIVIDER.	DSI_CLK_CTRL[31:30] PLL_PWR_CMD	x

10.3.5.2.1.2 Main Sequence - Set Up DSI Protocol Engine

10.3.5.2.1.2.1 Set Up DSI Control Registers

Table 10-502 lists the steps to set up the DSI control registers. Table 10-503 lists the steps to set up the DSI complex I/O registers.

Table 10-502. DSI Control Registers

Steps	Registers	Value
Enable the interrupt event for lost synchronization with the video port.	DSI_IRQENABLE[18] SYNC_LOST_IRQ_EN	0x1
Enable interrupt event for sent packet on desired VC.	DSI_VC_IRQENABLE_i[2] PACKET_SENT_IRQ_EN	x
Enable HSYNC END pulse detection (short packet generation).	DSI_CTRL[17] VP_HSYNC_START	0x1
Enable VSYNC START pulse detection (short packet generation).	DSI_CTRL[15] VP_VSYNC_START	0x1

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Table 10-502. DSI Control Registers (continued)

Steps	Registers	Value
Select trigger reset mode.	DSI_CTRL[14] TRIGGER_RESET_MODE	x
Set the number of line buffers.	DSI_CTRL[13:12] LINE_BUFFER	x
Set video port HSYNC signal polarity.	DSI_CTRL[10] VP_HSYNC_POL	x
Set video port VSYNC signal polarity.	DSI_CTRL[11] VP_VSYNC_POL	x
Set video port data enable signal polarity.	DSI_CTRL[9] VP_DE_POL	x
Set the size of the video port data bus.	DSI_CTRL[7:6] VP_DATA_BUS_WIDTH	x
Set the arbitration scheme for granting the VC pending ready requests in the TX FIFO.	DSI_CTRL[3] TX_FIFO_ARBITRATION	x
Enable/disable the ECC check for the received header.	DSI_CTRL[2] ECC_RX_EN	0x1

Table 10-503. DSI Complex I/O Registers

Steps	Registers	Value
Configure synchronized update on the shadow register.	DSI_COMPLEXIO_CFG1[30] GOBIT	x
Set the complex I/O power state.	DSI_COMPLEXIO_CFG1[28:27] PWR_CMD	x
Set the position of data lane 1.	DSI_COMPLEXIO_CFG1[6:4] DATA1_POSITION	x
Set the position of the clock lane.	DSI_COMPLEXIO_CFG1[2:0] CLOCK_POSITION	x
Clear the Interrupt status register.	DSI_COMPLEXIO_IRQSTATUS	0xFFFF FFFF
Disable all interrupt events.	DSI_COMPLEXIO_IRQENABLE	0x0
Enable the DSI protocol engine.	DSI_CTRL[0] IF_EN	0x1
Disable the DSI protocol engine.	DSI_CTRL[0] IF_EN	0x0
Wait until the interface is disabled?	DSI_CTRL[0] IF_EN	= 0x0
Enable the low-power clock (TXCLKESC).	DSI_CLK_CTRL[20] LP_CLK_ENABLE	0x1
Wait until reset is done?	DSI_COMPLEXIO_CFG1[29] RESET_DONE	= 0x1
Check if power control is ON?	DSI_COMPLEXIO_CFG1[26:25] PWR_STATUS	= 0x1
Wait until internal module reset is complete?	DSI_SYSSTATUS[0] RESETDONE	= 0x1

10.3.5.2.1.2.2 Configure DSI Timing and VCs

Table 10-504 lists the steps to configure DSI timing and the VCs.

Table 10-504. DSI Timing Registers

Steps	Registers	Value
Determine the number of DSI_FCLK clock cycles for the STOP-STATE counter.	DSI_TIMING1[12:0] STOP_STATE_COUNTER_IO	0x-
Determine the number of BYTE_CLK clock cycles for the HS RX timer.	DSI_TIMING2[28:16] HS_TX_TO_COUNTER	0x-
Enable/disable the multiplication factor of 16 for the number of BYTE_CLK clock cycles for the HS TX timer.	DSI_TIMING2[29] HS_TX_TO_X16	0x-
Determine the number of DSI_FCLK clock cycles for the LP RX timer.	DSI_TIMING2[12:0] LP_RX_TO_COUNTER	0x-
Enable/disable the multiplication factor of 16 for the number of DSI_FCLK clock cycles for the LP RX timer.	DSI_TIMING2[14] LP_RX_TO_X16	0x-
Set the horizontal sync active period.	DSI_VM_TIMING1[31:24] HSA	0x-
Set the horizontal front porch.	DSI_VM_TIMING1[23:12] HFP	0x-
Set the horizontal back porch.	DSI_VM_TIMING1[11:0] HBP	0x-

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Table 10-504. DSI Timing Registers (continued)

Steps	Registers	Value
Set the number of BYTE clock cycles for the sync window.	DSI_VM_TIMING2[27:24] WINDOW_SYNC	0x-
Set the vertical sync active period.	DSI_VM_TIMING2[23:16] VSA	0x-
Set the vertical front porch.	DSI_VM_TIMING2[15:8] VFP	0x-
Set the vertical back porch.	DSI_VM_TIMING2[7:0] VBP	0x-
Set the line length.	DSI_VM_TIMING3[31:16] TL	0x-
Set the number of active lines.	DSI_VM_TIMING3[15:0] VACT	0x-
Set the number of TXBYTECLKHS clock cycles for entering HS mode.	DSI_VM_TIMING7[31:16] ENTER_HS_MODE_LATENCY	0x-
Set the number of TXBYTECLKHSe clock cycles for exiting HS mode.	DSI_VM_TIMING7[15:0] EXIT_HS_MODE_LATENCY	0x-
Set the number of TXBYTECLKHS clock cycles between the start of the DDR clock and the assertion of the data request signal.	DSI_CLK_TIMING[15:8] DDR_CLK_PRE	0x-
Set the number of TXBYTECLKHS clock cycles after the deassertion of the data request signal and the stop of the DDR clock.	DSI_CLK_TIMING[7:0] DDR_CLK_POST	0x-
Configure the RX FIFO DMA request.	DSI_VC_CTRL_i[29:27] DMA_RX_REQ_NB	0x-
Configure the TX FIFO DMA request.	DSI_VC_CTRL_i[23:21] DMA_TX_REQ_NB	0x-
Enable/disable the ECC generation for the transmit header.	DSI_VC_CTRL_i[8] ECC_TX_EN	0x-
Enable/disable the checksum generation for the transmit payload.	DSI_VC_CTRL_i[7] CS_TX_EN	0x-
Select video mode.	DSI_VC_CTRL_i[4] MODE	0x-

10.3.5.2.1.3 Main Sequence - Configure DSI_PHY

Table 10-505 summarizes the timing in the functions of DDR_CLK_P. For more information about the timing calculation, see Section 10.3.4.4.4, *Clock Requirements*.

Table 10-505. Calculate DSI_PHY Timing

Steps	Registers	Value
Settings of the DSI protocol timing. For a complete description of the timing specifications, see Section 10.3.4.4.4, *Clock Requirements.*	DSI_PHY_REGISTER0[31:24] REG_THSPREPARE	ceil(70ns/DDR clock period) + 2
	DSI_PHY_REGISTER0[23:16] REG_PRPR_THSZERO	ceil(175ns/DDR clock period) + 2
	DSI_PHY_REGISTER0[7:0] REG_THSEXIT	ceil(145ns/DDR clock period)
	DSI_PHY_REGISTER0[15:8] REG_THSTRAIL	ceil(60ns/DDR clock period) + 5
	DSI_PHY_REGISTER2[7:0] REG_TCLKPREPARE	ceil(65ns/DDR clock period)
	DSI_PHY_REGISTER1[7:0] REG_TCLKZERO	ceil(265ns/DDR clock period)
	DSI_PHY_REGISTER1[15:8] REG_TCLKTRAIL	ceil(60ns/DDR clock period) + 2
	DSI_PHY_REGISTER1[20:16] REG_TLPXBY2	ceil(25ns/DDR clock period)

10.3.5.2.1.4 Main Sequence - Drive STOP State

Table 10-506 lists the steps to drive STOP state.

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Table 10-506. Drive STOP State

Steps	Registers	Value
Force TX stop mode.	DSI_TIMING1[15] FORCE_TX_STOP_MODE_IO	0x1
Wait until FORCE_TX_STOP_MODE_IO = 0?	DSI_TIMING1[15] FORCE_TX_STOP_MODE_IO	= 0x0

10.3.5.2.1.5 Main Sequence - Enable Video Mode

Table 10-506 lists the steps to enable video mode.

Table 10-507. Enable Video Mode

Steps	Registers	Value
Set up long packet header.	DSI_VC_LONG_PACKET_HEADER_i	0x-
Enable desired VC.	DSI_VC_CTRL_i[1] VC_EN	0x1
Enable DSI module.	DSI_CTRL[0] IF_EN	0x1
Wait until IF_EN = 1?	DSI_CTRL[0] IF_EN	= 0x1

10.3.5.2.2 DSI Command Mode Using the DISPC Video Port

This section explains the basic programming model of command mode using the DISPC video port.

10.3.5.2.2.1 Main Sequence - Configure DSI PLL

Table 10-508 lists the steps required to configure the DSI PLL.

Table 10-508. Configure DSI PLL

Steps	Register/Bit Field/Programming	Value
Set PLL and HSDIVIDER to ON state.	DSI_CLK_CTRL[31:30] PLL_PWR_CMD	0x2
Wait until PLL and HSDIVIDER are enabled?	DSI_CLK_CTRL[29:28] PLL_PWR_STATUS	= 0x2
Set the M5REG value.	DSI_PLL_CONFIGURATION1[30:26] M5_CLK_DIV	x
Set the M4REG value.	DSI_PLL_CONFIGURATION1[25:21] M4_CLOCK_DIV	x
Set the REGN value.	DSI_PLL_CONFIGURATION1[8:1] PLL_REGN	x
Set the REGM value.	DSI_PLL_CONFIGURATION1[20:9] PLL_REGM	x
Select PLL STOPMODE.	DSI_PLL_CONFIGURATION1[0] PLL_STOPMODE	0x1
Enable/disable PLL reference clock control.	DSI_PLL_CONFIGURATION2[13] PLL_REFEN	x
Enable/disable CLKIN4DDR control.	DSI_PLL_CONFIGURATION2[14] PHY_CLKINEN	x
Enable/disable DSS clock divider.	DSI_PLL_CONFIGURATION2[16] M4_CLOCK_EN	x
Enable/disable DSI protocol engine clock divider.	DSI_PLL_CONFIGURATION2[18] M5_CLOCK_EN	x
Configure synchronization of configuration update with DISPC_UPDATE_SYNC.	DSI_PLL_CONTROL[0] PLL_AUTOMODE	x
Start PLL locking sequence.	DSI_PLL_GO[0] PLL_GO	0x1
Wait until there is no pending action?	DSI_PLL_GO[0] PLL_GO	= 0x0
Check whether PLL is locked?	DSI_PLL_STATUS[1] PLL_LOCK	= 0x1
Set the LP mode clock ratio.	DSI_CLK_CTRL[12:0] LP_CLK_DIVISOR	x
Configure DSS_L3_ICLK clock to the DSI complex I/O.	DSI_CLK_CTRL[14] CIO_CLK_ICG	x
Enable/disable the automatic assertion/deassertion of the DSIStopClk signal.	DSI_CLK_CTRL[18] HS_AUTO_STOP_ENABLE	x
Define the DSI functional clock value and synchronization.	DSI_CLK_CTRL[21] LP_RX_SYNCHRO_ENABLE	x
Turn on PLL and HSDIVIDER.	DSI_CLK_CTRL[31:30] PLL_PWR_CMD	0x2

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10.3.5.2.2.2 Main Sequence - Switch to DSI PLL Clock Source

Table 10-509 lists the sequence to switch the DSI and DISPC module clocks to DSI PLL clock source.

Table 10-509. Switch to DSI PLL Clock Source

Steps	Reference	Value
Switch DISPC clock to PLL1_CLK1.	For more information, see Section 10.1.2,*DSS Integration*	
Switch DSI clock to PLL1_CLK2.	For more information, see Section 10.1.2, *DSS Integration*.	

10.3.5.2.2.3 Main Sequence - Configure DSI Protocol Engine

10.3.5.2.2.3.1 Set Up DSI Control Registers

Table 10-510 lists the steps required to set up the DSI control registers. Table 10-511 lists the steps to set up the DSI complex I/O registers.

Table 10-510. DSI Control Registers

Steps	Register/Bit Field/Programming	Value
Enable IRQ for lost synchronization with video port.	DSI_IRQENABLE[18] SYNC_LOST_IRQ_EN	0x1
Enable IRQ to indicate that packet has been sent on desired VC.	DSI_VC_IRQENABLE_i[2] PACKET_SENT_IRQ_EN	0x1
Set the trigger reset mode.	DSI_CTRL[14] TRIGGER_RESET_MODE	x
Configure the number of active line buffers.	DSI_CTRL[13:12] LINE_BUFFER	x
Set the size of the video port data bus.	DSI_CTRL[7:6] VP_DATA_BUS_WIDTH	x
Define the ratio between VP_CLK and VP_PCLK.	DSI_CTRL[4] VP_CLK_RATIO	x
Set the arbitration scheme for granting the VC pending ready requests in the TX FIFO.	DSI_CTRL[3] TX_FIFO_ARBITRATION	x
Enable/disable the ECC check for the received header.	DSI_CTRL[2] ECC_RX_EN	x

Table 10-511. DSI Complex I/O Registers

Steps	Register/Bit Field/Programming	Value
Determine the position of the clock lane.	DSI_COMPLEXIO_CFG1[2:0] CLOCK_POSITION	x
Set the position of data lane 1.	DSI_COMPLEXIO_CFG1[6:4] DATA1_POSITION	x
Configure the power state of the complex I/O.	DSI_COMPLEXIO_CFG1[28:27] PWR_CMD	x
Enable the synchronization of the shadow registers with DISPC_UPDATE_SYNC.	DSI_COMPLEXIO_CFG1[30] GOBIT	0x1
Clear the complex I/O IRQ status.	DSI_COMPLEXIO_IRQSTATUS	0xFFFF FFFF
Disable all complex I/O IRQ events.	DSI_COMPLEXIO_IRQENABLE	0x0
Enable the DSI protocol engine interface.	DSI_CTRL[0] IF_EN	0x1
Disable the DSI protocol engine interface.	DSI_CTRL[0] IF_EN	0x0
Wait until interface is disabled?	DSI_CTRL[0] IF_EN	= 0x0
Enable the LP clock.	DSI_CLK_CTRL[20] LP_CLK_ENABLE	0x1
Check whether internal reset is complete?	DSI_COMPLEXIO_CFG1[29] RESET_DONE	= 0x1
Check whether power state of complex I/O is ON?	DSI_COMPLEXIO_CFG1[26:25] PWR_STATUS	= 0x1
Check whether reset is complete?	DSI_SYSSTATUS[0] RESETDONE	= 0x1

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10.3.5.2.2.3.2 Configure DSI Timing and VCs

Table 10-512 lists the steps to configure DSI timing and the VCs.

Table 10-512. DSI Timing Registers

Steps	Register/Bit Field/Programming	Value
Determine the number of DSI_FCLK clock cycles for the STOP-STATE counter.	DSI_TIMING1[12:0] STOP_STATE_COUNTER_IO	0x-
Enable/disable the multiplication factor of 4 for the number of DSI_FCLK clock cycles for the STOP-STATE counter.	DSI_TIMING1[13] STOP_STATE_X4_IO	0x-
Enable/disable the multiplication factor of 16 for the number of DSI_FCLK clock cycles for the STOP-STATE counter.	DSI_TIMING1[14] STOP_STATE_X16_IO	0x-
Clear turnaround timer settings.	DSI_TIMING1[30:16]	0x0
Determine the number of DSI_FCLK clock cycles for the LP RX timer.	DSI_TIMING2[12:0] LP_RX_TO_COUNTER	0x-
Enable/disable the multiplication factor of 4 for the number of DSI_FCLK clock cycles for the LP RX timer.	DSI_TIMING2[13] LP_RX_TO_X4	0x-
Enable/disable the multiplication factor of 16 for the number of DSI_FCLK clock cycles for the LP RX timer.	DSI_TIMING2[14] LP_RX_TO_X16	0x-
Determine the number of BYTE_CLK clock cycles for the HS RX timer.	DSI_TIMING2[28:16] HS_TX_TO_COUNTER	0x-
Enable/disable the multiplication factor of 16 for the number of BYTE_CLK clock cycles for the HS TX timer.	DSI_TIMING2[29] HS_TX_TO_X16	0x-
Enable/disable the multiplication factor of 64 for the number of BYTE_CLK clock cycles for the HS TX timer.	DSI_TIMING2[30] HS_TX_TO_X64	0x-
Set the number of TXBYTECLKHS clock cycles	DSI_CLK_TIMING[15:8] DDR_CLK_PRE and DSI_CLK_TIMING[7:0] DDR_CLK_POST	0x-
Configuration of VCi		
Select source of data and enable VP_STALL.	DSI_VC_CTRL_i[1] SOURCE	0x1
Enable/disable the checksum generation for the transmit payload.	DSI_VC_CTRL_i[7] CS_TX_EN	0x-
Enable/disable the ECC generation for the transmit header.	DSI_VC_CTRL_i[8] ECC_TX_EN	0x-
Enable/disable HS mode to send short and long packets to the peripheral.	DSI_VC_CTRL_i[9] MODE_SPEED	0x-
Configure DMA request for TX FIFO.	DSI_VC_CTRL_i[23:21] DMA_TX_REQ_NB	0x-
Configure DMA request for RX FIFO.	DSI_VC_CTRL_i[29:27] DMA_RX_REQ_NB	0x-
Configuration TX and RX FIFO		
Set size of the RX FIFO allocated for used VC.	DSI_RX_FIFO_VC_SIZE	0x-
Set size of the TX FIFO allocated for used VC.	DSI_TX_FIFO_VC_SIZE	0x-

10.3.5.2.2.4 Main Sequence - Configure DSI_PHY Timing

Table 10-513 summarizes DSI_PHY timing settings. For more information about timing calculation, see Section 10.3.4.4.4, *Clock Requirements*.

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Table 10-513. Configure DSI_PHY Timing

Steps	Register/Bit Field/Programming	Value
Settings of the DSI protocol timing. For a complete description of timing specifications, see Section 10.3.4.4.4, *Clock Requirements*.	DSI_PHY_REGISTER0[31:24] REG_THSPREPARE	ceil(70ns/DDR clock period) + 2
	DSI_PHY_REGISTER0[23:16] REG_THSPRPR_THSZERO	ceil(175ns/DDR clock period) + 2
	DSI_PHY_REGISTER0[7:0] REG_THSEXIT	ceil(145ns/DDR clock period)
	DSI_PHY_REGISTER0[15:8] REG_THSTRAIL	ceil(60ns/DDR clock period) + 5
	DSI_PHY_REGISTER2[7:0] REG_TCLKPREPARE	ceil(65ns/DDR clock period)
	DSI_PHY_REGISTER1[7:0] REG_TCLKZERO	ceil(265ns/DDR clock period)
	DSI_PHY_REGISTER1[15:8] REG_TCLKTRAIL	ceil(60ns/DDR clock period) + 2
	DSI_PHY_REGISTER1[20:16] REG_TLPXBY2	ceil(25ns/DDR clock period)

10.3.5.2.2.5 Main Sequence - Drive STOP State

Table 10-514 lists the steps to drive the STOP state.

Table 10-514. Drive STOP State

Steps	Register/Bit Field/Programming	Value
Force TX stop mode.	DSI_TIMING1[15] FORCE_TX_STOP_MODE_IO	0x1
Wait until the end of TX stop mode assertion?	DSI_TIMING1[15] FORCE_TX_STOP_MODE_IO	= 0x1

10.3.5.2.2.6 Main Sequence - Enable Command Mode Using DISPC Video Port

Table 10-515 lists the steps to enable DISPC to send frames continuously. Two BTAs must be generated:

- The first BTA gives bus possession to the display module.
- The second BTA obtains the TE trigger.

Table 10-515. Enable Command Mode and Automatic TE

Steps	Register/Bit Field/Programming	Value
Insert DCS write memory continue/start code.	DSI_VC_CTRL_i[31] DCS_CMD_CODE	0x-
Enable/disable automatic insertion of DCS command codes when data is sourced by the video port.	DSI_VC_CTRL_i[30] DCS_CMD_ENABLE	0x-
Enable used VC.	DSI_VC_CTRL_i[0] VC_EN	0x1
Enable DSI protocol engine interface.	DSI_CTRL[0] IF_EN	0x1
Wait until interface is enabled?	DSI_CTRL[0] IF_EN	= 0x0
Send the sequence to receive the TE trigger from the peripheral.	DSI_VC_SHORT_PACKET_HEADER_i[31:0] HEADER	0x-
Wait until packet is sent?	DSI_VC_IRQSTATUS_i[2] PACKET_SENT_IRQ	= 0x1
Write 1 to reset the status bit.	DSI_VC_IRQSTATUS_i[2] PACKET_SENT_IRQ	0x1

NOTE: Keep Reserved bits at reset value in DSI_PHY_REGISTER1 and DSI_PHY_REGISTER2.

10.3.5.2.2.7 Main Sequence - Send Frame Data to LCD Panel Using Automatic TE

Table 10-516 summarizes the steps to send a frame data to the LCD panel using automatic TE.

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Table 10-516. Send Frame Data to LCD Panel Using Automatic TE

Steps	Register/Bit Field/Programming	Value
Enable the transfer between DISPC and DSI. Reset after the transfer is done.	For more information, see Section 10.2 , *Display Controller* chapter.	
Specify the number of bytes to send. When DCS insertion is used, word count (WC) must include this one DCS byte.	DSI_VC_TE_i[23:0] TE_SIZE	(WC+1)*LPP
Set up long packet header.	DSI_VC_LONG_PACKET_HEADER_i[31:0] HEADER	0x-
Enable/disable TE control.	DSI_VC_TE_i[30] TE_EN	0x1
Wait until RX FIFO is empty?	DSI_VC_CTRL_i[20] RX_FIFO_NOT_EMPTY	= 0x0
Wait until TX FIFO is not full?	DSI_VC_CTRL_i[16] TX_FIFO_FULL	= 0x0
Enable first BTA to give bus possession to the display module.	DSI_VC_CTRL_i[6] BTA_EN	0x1
Wait until BTA IRQ event occurs?	DSI_VC_IRQSTATUS_i[5] BTA_IRQ	= 0x1
Write 1 to clear BTA IRQ status bit.	DSI_VC_IRQSTATUS_i[5] BTA_IRQ	0x1
Enable the second BTA to get the TE trigger.	DSI_VC_CTRL_i[6] BTA_EN	0x1
Wait until BTA IRQ event occurs?	DSI_VC_IRQSTATUS_i[5] BTA_IRQ	= 0x1
Write 1 to clear BTA IRQ status bit.	DSI_VC_IRQSTATUS_i[5] BTA_IRQ	0x1
Wait until transfer is complete?	DSI_VC_TE_i[30] TE_EN	= 0x0

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10.3.6 DSI Register Manual

This section describes the DSI module registers.

CAUTION

The main access to all DSI registers is through the L3 interconnect.

The access through L4_PER interconnect is provided for back software compatibility.

10.3.6.1 DSI Instance Summary

Table 10-517 summarizes the DSI module instances.

Table 10-517. DSI Instance Summary

Module Name	L3 Base Address	L4_PER Base Address	Size
DSI1_PROTOCOL_ENGINE	0x5800 4000	0x4804 4000	512 bytes
DSI1_PHY	0x5800 4200	0x4804 4200	64 bytes
DSI1_PLLCTRL	0x5800 4300	0x4804 4300	32 bytes
DSI2_PROTOCOL_ENGINE	0x5800 5000	0x4804 5000	512 bytes
DSI2_PHY	0x5800 5200	0x4804 5200	64 bytes
DSI2_PLLCTRL	0x5800 5300	0x4804 5300	32 bytes

10.3.6.2 DSI_PROTOCOL_ENGINE Registers

10.3.6.2.1 DSI_PROTOCOL_ENGINE Register Summary

Table 10-518. DSI1_PROTOCOL_ENGINE Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	DSI1_PROTOCOL_ENGINE L3 Physical Address	DSI1_PROTOCOL_ENGINE L4_PER Physical Address
DSI_REVISION	R	32	0x0000 0000	0x5800 4000	0x4804 4000
DSI_SYSCONFIG	RW	32	0x0000 0010	0x5800 4010	0x4804 4010
DSI_SYSSTATUS	R	32	0x0000 0014	0x5800 4014	0x4804 4014
DSI_IRQSTATUS	RW	32	0x0000 0018	0x5800 4018	0x4804 4018
DSI_IRQENABLE	RW	32	0x0000 001C	0x5800 401C	0x4804 401C
DSI_CTRL	RW	32	0x0000 0040	0x5800 4040	0x4804 4040
DSI_GNQ	R	32	0x0000 0044	0x5800 4044	0x4804 4044
DSI_COMPLEXIO_CFG1	RW	32	0x0000 0048	0x5800 4048	0x4804 4048
DSI_COMPLEXIO_IRQSTATUS	RW	32	0x0000 004C	0x5800 404C	0x4804 404C
DSI_COMPLEXIO_IRQENABLE	RW	32	0x0000 0050	0x5800 4050	0x4804 4050
DSI_CLK_CTRL	RW	32	0x0000 0054	0x5800 4054	0x4804 4054
DSI_TIMING1	RW	32	0x0000 0058	0x5800 4058	0x4804 4058
DSI_TIMING2	RW	32	0x0000 005C	0x5800 405C	0x4804 405C
DSI_VM_TIMING1	RW	32	0x0000 0060	0x5800 4060	0x4804 4060
DSI_VM_TIMING2	RW	32	0x0000 0064	0x5800 4064	0x4804 4064
DSI_VM_TIMING3	RW	32	0x0000 0068	0x5800 4068	0x4804 4068
DSI_CLK_TIMING	RW	32	0x0000 006C	0x5800 406C	0x4804 406C

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Table 10-518. DSI1_PROTOCOL_ENGINE Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	DSI1_PROTOCOL_ENGINE L3 Physical Address	DSI1_PROTOCOL_ENGINE L4_PER Physical Address
DSI_TX_FIFO_VC_SIZE	RW	32	0x0000 0070	0x5800 4070	0x4804 4070
DSI_RX_FIFO_VC_SIZE	RW	32	0x0000 0074	0x5800 4074	0x4804 4074
DSI_COMPLEXIO_CFG2	RW	32	0x0000 0078	0x5800 4078	0x4804 4078
DSI_RX_FIFO_VC_FULLNESS	R	32	0x0000 007C	0x5800 407C	0x4804 407C
DSI_VM_TIMING4	RW	32	0x0000 0080	0x5800 4080	0x4804 4080
DSI_TX_FIFO_VC_EMPTINESS	R	32	0x0000 0084	0x5800 4084	0x4804 4084
DSI_VM_TIMING5	RW	32	0x0000 0088	0x5800 4088	0x4804 4088
DSI_VM_TIMING6	RW	32	0x0000 008C	0x5800 408C	0x4804 408C
DSI_VM_TIMING7	RW	32	0x0000 0090	0x5800 4090	0x4804 4090
DSI_STOPCLK_TIMING	RW	32	0x0000 0094	0x5800 4094	0x4804 4094
DSI_CTRL2	RW	32	0x0000 0098	0x5800 4098	0x4804 4098
DSI_VM_TIMING8	RW	32	0x0000 009C	0x5800 409C	0x4804 409C
DSI_TE_HSYNC_WIDTH_j (1)	RW	32	0x0000 00A0 + (0xc * j)	0x5800 40A0 + (0xc * j)	0x4804 40A0 + (0xc * j)
DSI_TE_VSYNC_WIDTH_j (1)	RW	32	0x0000 00A4 + (0xc * j)	0x5800 40A4 + (0xc * j)	0x4804 40A4 + (0xc * j)
DSI_TE_HSYNC_NUMBER_j (1)	RW	32	0x0000 00A8 + (0xc * j)	0x5800 40A8 + (0xc * j)	0x4804 40A8 + (0xc * j)
DSI_VC_CTRL_i (2)	RW	32	0x0000 0100 + (0x20 * i)	0x5800 4100 + (0x20 * i)	0x4804 4100 + (0x20 * i)
DSI_VC_TE_i (2)	RW	32	0x0000 0104 + (0x20 * i)	0x5800 4104 + (0x20 * i)	0x4804 4104 + (0x20 * i)
DSI_VC_LONG_PACKET_HEADER_i (2)	W	32	0x0000 0108 + (0x20 * i)	0x5800 4108 + (0x20 * i)	0x4804 4108 + (0x20 * i)
DSI_VC_LONG_PACKET_PAYLOAD_i (2)	W	32	0x0000 010C + (0x20 * i)	0x5800 410C + (0x20 * i)	0x4804 410C + (0x20 * i)
DSI_VC_SHORT_PACKET_HEADER_i (2)	RW	32	0x0000 0110 + (0x20 * i)	0x5800 4110 + (0x20 * i)	0x4804 4110 + (0x20 * i)
DSI_VC_IRQSTATUS_i (2)	RW	32	0x0000 0118 + (0x20 * i)	0x5800 4118 + (0x20 * i)	0x4804 4118 + (0x20 * i)
DSI_VC_IRQENABLE_i (2)	RW	32	0x0000 011C + (0x20 * i)	0x5800 411C + (0x20 * i)	0x4804 411C + (0x20 * i)

(1) j = 0 to 1
(2) i = 0 to 3

Table 10-519. DSI2_PROTOCOL_ENGINE Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	DSI2_PROTOCOL_ENGINE L3 Physical Address	DSI2_PROTOCOL_ENGINE L4_PER Physical Address
DSI_REVISION	R	32	0x0000 0000	0x5800 5000	0x4804 5000
DSI_SYSCONFIG	RW	32	0x0000 0010	0x5800 5010	0x4804 5010
DSI_SYSSTATUS	R	32	0x0000 0014	0x5800 5014	0x4804 5014

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Table 10-519. DSI2_PROTOCOL_ENGINE Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	DSI2_PROTOCOL_ENGINE L3 Physical Address	DSI2_PROTOCOL_ENGINE L4_PER Physical Address
DSI_IRQSTATUS	RW	32	0x0000 0018	0x5800 5018	0x4804 5018
DSI_IRQENABLE	RW	32	0x0000 001C	0x5800 501C	0x4804 501C
DSI_CTRL	RW	32	0x0000 0040	0x5800 5040	0x4804 5040
DSI_GNQ	R	32	0x0000 0044	0x5800 5044	0x4804 5044
DSI_COMPLEXIO_CFG1	RW	32	0x0000 0048	0x5800 5048	0x4804 5048
DSI_COMPLEXIO_IRQSTATUS	RW	32	0x0000 004C	0x5800 504C	0x4804 504C
DSI_COMPLEXIO_IRQENABLE	RW	32	0x0000 0050	0x5800 5050	0x4804 5050
DSI_CLK_CTRL	RW	32	0x0000 0054	0x5800 5054	0x4804 5054
DSI_TIMING1	RW	32	0x0000 0058	0x5800 5058	0x4804 5058
DSI_TIMING2	RW	32	0x0000 005C	0x5800 505C	0x4804 505C
DSI_VM_TIMING1	RW	32	0x0000 0060	0x5800 5060	0x4804 5060
DSI_VM_TIMING2	RW	32	0x0000 0064	0x5800 5064	0x4804 5064
DSI_VM_TIMING3	RW	32	0x0000 0068	0x5800 5068	0x4804 5068
DSI_CLK_TIMING	RW	32	0x0000 006C	0x5800 506C	0x4804 506C
DSI_TX_FIFO_VC_SIZE	RW	32	0x0000 0070	0x5800 5070	0x4804 5070
DSI_RX_FIFO_VC_SIZE	RW	32	0x0000 0074	0x5800 5074	0x4804 5074
DSI_COMPLEXIO_CFG2	RW	32	0x0000 0078	0x5800 5078	0x4804 5078
DSI_RX_FIFO_VC_FULLNESS	R	32	0x0000 007C	0x5800 507C	0x4804 507C
DSI_VM_TIMING4	RW	32	0x0000 0080	0x5800 5080	0x4804 5080
DSI_TX_FIFO_VC_EMPTINESS	R	32	0x0000 0084	0x5800 5084	0x4804 5084
DSI_VM_TIMING5	RW	32	0x0000 0088	0x5800 5088	0x4804 5088
DSI_VM_TIMING6	RW	32	0x0000 008C	0x5800 508C	0x4804 508C
DSI_VM_TIMING7	RW	32	0x0000 0090	0x5800 5090	0x4804 5090
DSI_STOPCLK_TIMING	RW	32	0x0000 0094	0x5800 5094	0x4804 5094
DSI_CTRL2	RW	32	0x0000 0098	0x5800 5098	0x4804 5098
DSI_VM_TIMING8	RW	32	0x0000 009C	0x5800 509C	0x4804 509C
DSI_TE_HSYNC_WIDTH_j (1)	RW	32	0x0000 00A0 + (0xc * j)	0x5800 50A0 + (0xc * j)	0x4804 50A0 + (0xc * j)
DSI_TE_VSYNC_WIDTH_j (1)	RW	32	0x0000 00A4 + (0xc * j)	0x5800 50A4 + (0xc * j)	0x4804 50A4 + (0xc * j)
DSI_TE_HSYNC_NUMBER_j (1)	RW	32	0x0000 00A8 + (0xc * j)	0x5800 50A8 + (0xc * j)	0x4804 50A8 + (0xc * j)
DSI_VC_CTRL_i (2)	RW	32	0x0000 0100 + (0x20 * i)	0x5800 5100 + (0x20 * i)	0x4804 5100 + (0x20 * i)
DSI_VC_TE_i (2)	RW	32	0x0000 0104 + (0x20 * i)	0x5800 5104 + (0x20 * i)	0x4804 5104 + (0x20 * i)
DSI_VC_LONG_PACKET_HEADER_i (2)	W	32	0x0000 0108 + (0x20 * i)	0x5800 5108 + (0x20 * i)	0x4804 5108 + (0x20 * i)

(1) j = 0 to 1
(2) i = 0 to 3

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Table 10-519. DSI2_PROTOCOL_ENGINE Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	DSI2_PROTOCOL_ENGINE L3 Physical Address	DSI2_PROTOCOL_ENGINE L4_PER Physical Address
DSI_VC_LONG_PACKET_PAYLOAD_i (2)	W	32	0x0000 010C + (0x20 * i)	0x5800 510C + (0x20 * i)	0x4804 510C + (0x20 * i)
DSI_VC_SHORT_PACKET_HEADER_i (2)	RW	32	0x0000 0110 + (0x20 * i)	0x5800 5110 + (0x20 * i)	0x4804 5110 + (0x20 * i)
DSI_VC_IRQSTATUS_i (2)	RW	32	0x0000 0118 + (0x20 * i)	0x5800 5118 + (0x20 * i)	0x4804 5118 + (0x20 * i)
DSI_VC_IRQENABLE_i (2)	RW	32	0x0000 011C + (0x20 * i)	0x5800 511C + (0x20 * i)	0x4804 511C + (0x20 * i)

10.3.6.2.2 DSI_PROTOCOL_ENGINE Register Description

Table 10-520. DSI_REVISION

Address Offset	0x0000 0000		
Physical Address	0x5800 4000 0x4804 4000 0x5800 5000 0x4804 5000	**Instance**	DSI1_PROTOCOL_ENGINE_L3 DSI1_PROTOCOL_ENGINE_PER_L4 DSI2_PROTOCOL_ENGINE_L3 DSI2_PROTOCOL_ENGINE_PER_L4
Description	IP Revision		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP Revision	R	See (1)

(1) TI Internal data

Table 10-521. Register Call Summary for Register DSI_REVISION

MIPI Display Serial Interface
- DSI_PROTOCOL_ENGINE Register Summary: [0] [1]

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Table 10-522. DSI_SYSCONFIG

Address Offset	0x0000 0010		
Physical Address	0x5800 4010 0x4804 4010 0x5800 5010 0x4804 5010	**Instance**	DSI1_PROTOCOL_ENGINE_L3 DSI1_PROTOCOL_ENGINE_PER_L4 DSI2_PROTOCOL_ENGINE_L3 DSI2_PROTOCOL_ENGINE_PER_L4
Description	SYSTEM CONFIGURATION REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						CLOCKACTIVITY		RESERVED			SIDLEMODE		ENWAKEUP	SOFT_RESET	AUTO_IDLE

Bits	Field Name	Description	Type	Reset
31:10	RESERVED		R	0x000000
9:8	CLOCKACTIVITY	Clocks activity during wake up mode period 0x0: Interface and Functional clocks can be switched off 0x1: Functional clocks can be switched off and Interface clocks are maintained during wake up period 0x2: Interface clocks can be switched off and Functional clocks are maintained during wake up period 0x3: Interface and Functional clocks are maintained during wake up period	RW	0x0
7:5	RESERVED		R	0x0
4:3	SIDLEMODE	Slave interface power management, Idle req/ack control 0x0: Force-idle. An idle request is acknowledged unconditionally 0x1: No-idle. An idle request is never acknowledged 0x2: Smart-idle. Acknowledgement to an idle request is given based on the internal activity of the module. 0x3: Reserved	RW	0x2
2	ENWAKEUP	Wake-up mode enable bit 0x0: Wakeup is disabled 0x1: Wakeup is enabled	RW	0
1	SOFT_RESET	Software reset. Set the bit to 1 to trigger a module reset. The bit is automatically reset by the hardware. During reads return 0. 0x0: Normal mode. 0x1: The module is reset	RW	0
0	AUTO_IDLE	Internal interface gating strategy 0x0: Interface clock is free-running. 0x1: Automatic Interface clock gating strategy is applied based on the interface activity.	RW	1

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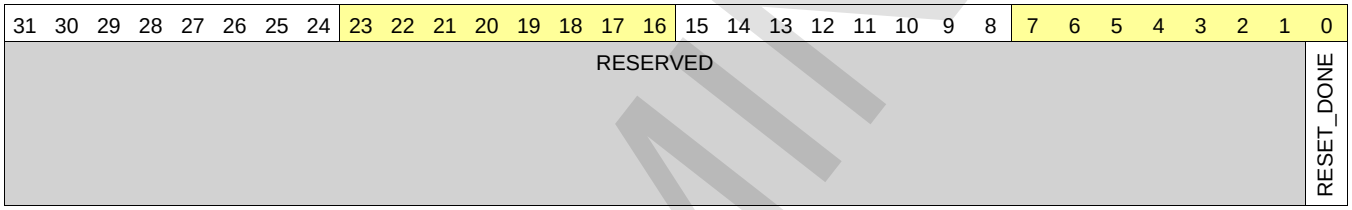
Table 10-523. Register Call Summary for Register DSI_SYSCONFIG

MIPI Display Serial Interface

- Software Reset: [0]
- Power Management: [1] [2]
- Software Reset: [3]
- DSI Global Initialization: [4] [5] [6]
- DSI_PROTOCOL_ENGINE Register Summary: [7] [8]

Table 10-524. DSI_SYSSTATUS

Address Offset	0x0000 0014		
Physical Address	0x5800 4014 0x4804 4014 0x5800 5014 0x4804 5014	**Instance**	DSI1_PROTOCOL_ENGINE_L3 DSI1_PROTOCOL_ENGINE_PER_L4 DSI2_PROTOCOL_ENGINE_L3 DSI2_PROTOCOL_ENGINE_PER_L4
Description	SYSTEM STATUS REGISTER This register provides status information about the module, excluding the interrupt status register.		
Type	R		



Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	RESET_DONE	Internal reset monitoring Read 0x0: Internal module reset is on going. Read 0x1: Reset completed.	R	1

Table 10-525. Register Call Summary for Register DSI_SYSSTATUS

MIPI Display Serial Interface

- Software Reset: [0] [1]
- DSI Global Initialization: [2] [3]
- DSI Video Mode Using the DISPC Video Port: [4]
- DSI Command Mode Using the DISPC Video Port: [5]
- DSI_PROTOCOL_ENGINE Register Summary: [6] [7]

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Table 10-526. DSI_IRQSTATUS

Address Offset	0x0000 0018		
Physical Address	0x5800 4018 0x4804 4018 0x5800 5018 0x4804 5018	**Instance**	DSI1_PROTOCOL_ENGINE_L3 DSI1_PROTOCOL_ENGINE_PER_L4 DSI2_PROTOCOL_ENGINE_L3 DSI2_PROTOCOL_ENGINE_PER_L4
Description	INTERRUPT STATUS REGISTER - All virtual channels + Complex I/O + PLL This register associates one bit for each virtual channel in order to determine which virtual channel has generated the interrupt. The virtual channel shall be enabled for events to be generated on that virtual channel. If the virtual channel is disabled, the interrupt is not generated.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TE1_LINE_IRQ	TE0_LINE_IRQ	TA_TO_IRQ	RESERVED	SYNC_LOST_IRQ	ACK_TRIGGER_IRQ	TE_TRIGGER_IRQ	LP_RX_TO_IRQ	HS_TX_TO_IRQ	RESERVED			COMPLEXIO_ERR_IRQ	PLL_RECAL_IRQ	PLL_UNLOCK_IRQ	PLL_LOCK_IRQ	RESERVED	RESYNCHRONIZATION_IRQ	WAKEUP_IRQ	VIRTUAL_CHANNEL3_IRQ	VIRTUAL_CHANNEL2_IRQ	VIRTUAL_CHANNEL1_IRQ	VIRTUAL_CHANNEL0_IRQ	

Bits	Field Name	Description	Type	Reset
31:23	RESERVED		R	0x000
22	TE1_LINE_IRQ	The VSYNC and corresponding HSYNC pulses defined in DSI_TE_HSYNC_NUMBER for the line TE1 have been received by the DSI protocol engine and have trigger the start of the data transfer to the peripheral. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW	0
21	TE0_LINE_IRQ	The VSYNC and corresponding HSYNC pulses defined in DSI_TE_HSYNC_NUMBER for the line TE0 have been received by the DSI protocol engine and have trigger the start of the data transfer to the peripheral. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW	0
20	TA_TO_IRQ	Turn-around Time out. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW	0
19	RESERVED	Reserved. Keep at reset value.	RW	0
18	SYNC_LOST_IRQ	Synchronization with Video port is lost (Video mode only) 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW	0

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Bits	Field Name	Description	Type	Reset
17	ACK_TRIGGER_IRQ	Acknowledge Trigger 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW	0
16	TE_TRIGGER_IRQ	Tearing Effect Trigger 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW	0
15	LP_RX_TO_IRQ	Interrupt for Low Power Rx Time out 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW	0
14	HS_TX_TO_IRQ	Interrupt for High Speed Tx Time out. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW	0
13:11	RESERVED		R	0x0
10	COMPLEXIO_ERR_IRQ	Error signaling from Complex I/O: status of the complex I/O errors received from the complex I/O (events are defined in DSI_COMPLEXIO_IRQSTATUS). Read 0x0: READS: Event is false. Read 0x1: READS: Event is true (pending).	R	0
9	PLL_RECAL_IRQ	PLL recal event (assertion of DSIRecal signal from the DSI PLL Control module) 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW	0
8	PLL_UNLOCK_IRQ	PLL un-clock event (de-assertion of DSILock signal from the DSI PLL Control module) 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW	0
7	PLL_LOCK_IRQ	PLL clock event (assertion of DSILock signal from the DSI PLL Control module) 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW	0
6	RESERVED		R	0
5	RESYNCHRONIZATION_IRQ	Video mode resynchronization indicates to the software users that the video port works but the configuration of the timings for the display controller (DISPC) and for DSI Protocol engine may need to be modified to avoid the resynchronization to occur. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW	0

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Bits	Field Name	Description	Type	Reset
4	WAKEUP_IRQ	Wakeup 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW	0
3	VIRTUAL_CHANNEL3_IRQ	Virtual channel 3 Read 0x0: READS: Event is false. Read 0x1: READS: Event is true (pending).	R	0
2	VIRTUAL_CHANNEL2_IRQ	Virtual channel 2 Read 0x0: READS: Event is false. Read 0x1: READS: Event is true (pending).	R	0
1	VIRTUAL_CHANNEL1_IRQ	Virtual channel 1 Read 0x0: READS: Event is false. Read 0x1: READS: Event is true (pending).	R	0
0	VIRTUAL_CHANNEL0_IRQ	Virtual channel 0 Read 0x0: READS: Event is false. Read 0x1: READS: Event is true (pending).	R	0

Table 10-527. Register Call Summary for Register DSI_IRQSTATUS

MIPI Display Serial Interface

- DSI Interrupt Requests: [0]
- DSI Transfer Modes: [1] [2]
- Timers: [3] [4]
- PHY Triggers: [5] [6]
- Interrupts: [7]
- Error Handling: [8] [9] [10]
- Error Handling: [11]
- DSI Global Initialization: [12]
- DSI_PROTOCOL_ENGINE Register Summary: [13] [14]

Table 10-528. DSI_IRQENABLE

Address Offset	0x0000 001C		
Physical Address	0x5800 401C 0x4804 401C 0x5800 501C 0x4804 501C	**Instance**	DSI1_PROTOCOL_ENGINE_L3 DSI1_PROTOCOL_ENGINE_PER_L4 DSI2_PROTOCOL_ENGINE_L3 DSI2_PROTOCOL_ENGINE_PER_L4
Description	INTERRUPT ENABLE REGISTER - This register associates one bit for each virtual channel in order to enable/disable each virtual channel individually.		
Type	RW		

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31 30 29 28 27 26 25 24	23	22	21	20	19	18	17	16	15	14	13 12 11 10	9	8	7	6	5	4	3 2 1 0
RESERVED		TE1_LINE_IRQ_EN	TE0_LINE_IRQ_EN	TA_TO_IRQ_EN	RESERVED	SYNC_LOST_IRQ_EN	ACK_TRIGGER_IRQ_EN	TE_TRIGGER_IRQ_EN	LP_RX_TO_IRQ_EN	HS_TX_TO_IRQ_EN	RESERVED	PLL_RECAL_IRQ_EN	PLL_UNLOCK_IRQ_EN	PLL_LOCK_IRQ_EN	RESERVED	RESYNCHRONIZATION_IRQ_EN	WAKEUP_IRQ_EN	RESERVED

Bits	Field Name	Description	Type	Reset
31:23	RESERVED		R	0x000
22	TE1_LINE_IRQ_EN	The VSYNC and corresponding HSYNC pulses defined in DSI_TE_HSYNC_NUMBER for the line TE1 have been received by the DSI protocol engine and have trigger the start of the data transfer to the peripheral. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
21	TE0_LINE_IRQ_EN	The VSYNC and corresponding HSYNC pulses defined in DSI_TE_HSYNC_NUMBER for the line TE0 have been received by the DSI protocol engine and have trigger the start of the data transfer to the peripheral. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
20	TA_TO_IRQ_EN	Turn-around Time out. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
19	RESERVED	Reserved. Keep at reset value.	RW	0
18	SYNC_LOST_IRQ_EN	Synchronization with Video port is lost (Video mode only) 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
17	ACK_TRIGGER_IRQ_EN	Acknowledge trigger 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
16	TE_TRIGGER_IRQ_EN	Tearing Effect trigger 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
15	LP_RX_TO_IRQ_EN	Interrupt for Low Power Rx Time out. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
14	HS_TX_TO_IRQ_EN	Interrupt for High Speed Tx Time out. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
13:10	RESERVED		R	0x0
9	PLL_RECAL_IRQ_EN	PLL recal event (assertion of DSIRecal signal from the DSI PLL Control module) 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0

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Bits	Field Name	Description	Type	Reset
8	PLL_UNLOCK_IRQ_EN	PLL un-clock event (de-assertion of DSILock signal from the DSI PLL Control module) 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
7	PLL_LOCK_IRQ_EN	PLL clock event (assertion of DSILock signal from the DSI PLL Control module) 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
6	RESERVED		R	0
5	RESYNCHRONIZATION_IRQ_EN	Video mode resynchronization 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
4	WAKEUP_IRQ_EN	Wakeup 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
3:0	RESERVED		R	0x0

Table 10-529. Register Call Summary for Register DSI_IRQENABLE

MIPI Display Serial Interface

- PHY Triggers: [0] [1]
- Interrupts: [2]
- DSI Video Mode Using the DISPC Video Port: [3]
- DSI Command Mode Using the DISPC Video Port: [4]
- DSI_PROTOCOL_ENGINE Register Summary: [5] [6]

Table 10-530. DSI_CTRL

Address Offset	0x0000 0040		
Physical Address	0x5800 4040 0x4804 4040 0x5800 5040 0x4804 5040	**Instance**	DSI1_PROTOCOL_ENGINE_L3 DSI1_PROTOCOL_ENGINE_PER_L4 DSI2_PROTOCOL_ENGINE_L3 DSI2_PROTOCOL_ENGINE_PER_L4
Description	GLOBAL CONTROL REGISTER This register controls the DSI Protocol Engine module. This register shall not be modified dynamically (except IF_EN bit fields).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							DISPC_UPDATE_SYNC	HSA_BLANKING_MODE	HBP_BLANKING_MODE	HFP_BLANKING_MODE	BLANKING_MODE	EOT_ENABLE	VP_HSYNC_END	VP_HSYNC_START	VP_VSYNC_END	VP_VSYNC_START	TRIGGER_RESET_MODE	LINE_BUFFER		VP_VSYNC_POL	VP_HSYNC_POL	VP_DE_POL	VP_CLK_POL	VP_DATA_BUS_WIDTH		TRIGGER_RESET	VP_CLK_RATIO	TX_FIFO_ARBITRATION	ECC_RX_EN	CS_RX_EN	IF_EN

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Bits	Field Name	Description	Type	Reset
31:25	RESERVED		R	0x00
24	DISPC_UPDATE_SYNC	Determines if the Dispc_Update_Sync signal from the display controller is used. 0x0: Dispc_Update_Sync signal is not used. 0x1: Dispc_Update_Sync signal is used.	RW	0
23	HSA_BLANKING_MODE	Blanking mode 0x0: Packets in TX FIFO are sent during HSA blanking period of video mode or LPS is used. 0x1: LONG BLANKING PACKETS only are used during HSA blanking period of video mode.	RW	0
22	HBP_BLANKING_MODE	Blanking mode 0x0: Packets in TX FIFO are sent during HBP blanking period of video mode or LPS is used. 0x1: LONG BLANKING PACKETS only are used during HBP blanking period of video mode.	RW	0
21	HFP_BLANKING_MODE	Blanking mode 0x0: Packets in TX FIFO are sent during HFP blanking period of video mode or LPS is used. 0x1: LONG BLANKING PACKETS only are used during HFP blanking period of video mode.	RW	0
20	BLANKING_MODE	Blanking mode 0x0: LPS is used during blanking periods of video mode (except HSA, HBP, HFP defined in HSA_BLANKING_MODE, HBP_BLANKING_MODE AND HFP_BLANKING_MODE respectively) when there is no command mode data in TX FIFO ready to be sent. So blanking periods can be different during the frame depending on the TX FIFO. 0x1: LONG BLANKING PACKETS are used during blanking periods of video mode (except HSA, HBP, HFP defined in HSA_BLANKING_MODE, HBP_BLANKING_MODE AND HFP_BLANKING_MODE respectively) regardless of the packets present in the TX FIFO ready to be sent	RW	0
19	EOT_ENABLE	Enable EOT packets at the end of HS transmission. 0x0: No EOT packets 0x1: EOT packet is sent at all HS to LP transitions.	RW	0
18	VP_HSYNC_END	HSYNC end pulse. 0x0: Disabled. No HSYNC END short packet is generated. 0x1: Enabled. While the HSYNC END pulse is detected, the associated short packet HSYNC END is generated.	RW	0
17	VP_HSYNC_START	HSYNC start pulse. 0x0: Disabled. No HSYNC START short packet is generated. 0x1: Enabled. While the HSYNC start pulse is detected, the associated short packet HSYNC START is generated.	RW	0
16	VP_VSYNC_END	VSYNC end pulse. 0x0: Disabled. No VSYNC END short packet is generated. 0x1: Enabled. While the VSYNC END pulse is detected, the associated short packet VSYNC END is generated.	RW	0

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Bits	Field Name	Description	Type	Reset
15	VP_VSYNC_START	VSYNC start pulse. 0x0: Disabled. No VSYNC START short packet is generated. 0x1: Enabled. While the VSYNC START pulse is detected, the associated short packet VSYNC START is generated.	RW	0
14	TRIGGER_RESET_MODE	Selection of the trigger reset mode 0x0: Synchronized: the mode is only valid if there is virtual channel using the video mode and it is active. The principal is to wait for the current video frame to be transferred on the link. Any data received after the VSYNC are ignored. 0x1: Immediate: all pending requests in TX FIFO are taken into account for transfer scheduling, the RX FIFO is ignored, and the data from video port are ignored as soon as possible. Only the current transfer on DSI link and already scheduled ones are transmitted. All the other transfers are discarded.	RW	0
13:12	LINE_BUFFER	Number of line buffers to be used while receiving data on the video port. The valid values are from 0 to DSI_GNQ[17:16] VP1_NB_LINE_BUFFER. 0x0: No line buffer 0x1: 1 line buffer 0x2: 2 line buffers	RW	0x0
11	VP_VSYNC_POL	VP vertical synchronization signal polarity 0x0: VSYNC signal on the video port is active low. 0x1: VSYNC signal on the video port is active high.	RW	0
10	VP_HSYNC_POL	VP horizontal synchronization signal polarity 0x0: HSYNC signal on the video port is active low. 0x1: HSYNC signal on the video port is active high.	RW	0
9	VP_DE_POL	VP data enable signal polarity 0x0: DE signal on the video port is active low. 0x1: DE signal on the video port is active high.	RW	0
8	VP_CLK_POL	VP pixel clock polarity 0x0: The DSI Protocol Engine module captures the data on the VP on the pixel clock falling edge. The module connected to the VP shall drive the data on the pixel clock rising edge. 0x1: The DSI Protocol Engine module captures the data on the VP on the pixel clock raising edge. The module connected to the VP shall drive the data on the pixel clock falling edge.	RW	1
7:6	VP_DATA_BUS_WIDTH	Defines the size of the video port data bus 0x0: 16-bits data width (LSB of the 24-bit video port data bus) 0x1: 18-bits data width (LSB of the 24-bit video port data bus) 0x2: 24-bits data width (LSB of the 24-bit video port data bus)	RW	0x0
5	TRIGGER_RESET	Send the reset trigger to the peripheral. 0x0: READS: Reset trigger generation is completed. It is reset by hardware when it is completed. WRITES: Cancellation of the request for Reset trigger generation (maybe too late since it is already on going) 0x1: READS: Generation of the reset trigger has been requested by user (could be on going but not completed yet). WRITES: Request for Reset trigger to be sent to the peripheral.	RW	0

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Bits	Field Name	Description	Type	Reset
4	VP_CLK_RATIO	The field indicates the clock ratio between VP_CLK and VP_PCLK. The clock VP_PCLK is generated from VP_CLK. It is divided down. The information is only used when the video port is used to provide data in command mode. In the case of video mode, it is not used. 0x0: The clock VP_PCLK is the clock VP_CLK divided by 2. The duty cycle of VP_PCLK is 50/50. 0x1: The clock VP_PCLK is the clock VP_CLK divided by 3 or more. The duty cycle of VP_PCLK is not 50/50 for odd ratio numbers (3,5,7,...).	RW	0
3	TX_FIFO_ARBITRATION	Defines the arbitration scheme for granting the virtual channel pending ready requests in the TX FIFO 0x0: Round-Robin Scheme is used 0x1: Sequential Scheme is used	RW	0
2	ECC_RX_EN	Enables the Error Correction Code check for the received header (short and long packets for all virtual channel ids). 0x0: Disabled 0x1: Enabled	RW	0
1	CS_RX_EN	Enables the checksum check for the received payload (long packet only for all virtual channel ids). 0x0: Disabled 0x1: Enabled	RW	0
0	IF_EN	Enables the module. When the module is disabled the signals from the complex I/O are gated (no updates of the interrupt status register). It is not possible to change the bit fields in the register DSI_CTRL except IF_EN when it is enabled. All the other registers can be changed except the ones that require DSI_VC_CTRL_i[0] VC_EN to be equal to 0 to be modified. 0x0: The interface is disabled. If one of the virtual channel uses the video mode with the video port to receive the data, the DSI protocol engines is disabled when the next VSYNC is received and all the data in the FIFO for the other virtual channels in command mode are sent to the peripherals (if BTA_EN is enabled, the DSI protocol needs to wait for the response and BTA from the peripheral before disabling all the internal logic since an acknowledge is requested). 0x1: The interface is enabled immediately, the data acquisition on the video port starts on the next VSYNC (video mode) or first data received in the Slave port FIFO (command mode).	RW	0

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Table 10-531. Register Call Summary for Register DSI_CTRL

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- Short Packet: [0] [1] [2] [3] [4] [5]
- DSI Global Register Controls: [6] [7] [8] [9] [10] [11] [12]
- DSI Transfer Modes: [13] [14] [15] [16] [17] [18]
- Clock Requirements: [19]
- Video Port Interface: [20] [21] [22] [23] [24] [25] [26] [27] [28] [29]
- Timers: [30] [31] [32] [33] [34] [35]
- Bus Turnaround: [36] [37] [38] [39]
- PHY Triggers: [40] [41] [42] [43]
- ECC Generation: [44]
- Checksum Generation for Long Packet Payloads: [45]
- EOT Packet: [46]
- Power Control of DSI PHY Complex I/O and DSI PLL: [47] [48] [49] [50] [51] [52]
- How to Configure the DSI PLL in Video Mode: [53] [54]
- Pad Configuration: [55] [56] [57]
- DSI Video Mode Using the DISPC Video Port: [58] [59] [60] [61] [62] [63] [64] [65] [66] [67] [68] [69] [70] [71] [72]
- DSI Command Mode Using the DISPC Video Port: [73] [74] [75] [76] [77] [78] [79] [80] [81] [82] [83]
- DSI_PROTOCOL_ENGINE Register Summary: [84] [85]
- DSI_PROTOCOL_ENGINE Register Description: [86] [87] [88] [89] [90] [91] [92] [93]

Table 10-532. DSI_GNQ

Address Offset	0x0000 0044		
Physical Address	0x5800 4044 0x4804 4044 0x5800 5044 0x4804 5044	**Instance**	DSI1_PROTOCOL_ENGINE_L3 DSI1_PROTOCOL_ENGINE_PER_L4 DSI2_PROTOCOL_ENGINE_L3 DSI2_PROTOCOL_ENGINE_PER_L4
Description	GENERIC PARAMETER REGISTER This register provide a way to read the generic parameters used in the design.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							NB_VIDEO_PORTS	VP2_NB_LINE_BUFFER		RESERVED	VP2_LINE_BUFFER_SIZE			VP1_NB_LINE_BUFFER		RESERVED	VP1_LINE_BUFFER_SIZE			NB_DATA_LANES				NB_DMA_REQUEST				RX_FIFODEPTH			TX_FIFODEPTH			

Bits	Field Name	Description	Type	Reset
31:25	RESERVED		R	0x00
24	NB_VIDEO_PORTS	Number of video ports Read 0x0: Video port 1 only is present Read 0x1: Video port 1 and video port 2 are present	R	0

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Bits	Field Name	Description	Type	Reset
23:22	VP2_NB_LINE_BUFFER	Determines the number of video buffer lines associated to video port 2. Read 0x0: No line buffer Read 0x1: 1 line buffer of the size defined in LINE_BUFFER_SIZE Read 0x2: 2 line buffers of the size defined in LINE_BUFFER_SIZE	R	0x2 for DSI1 0x0 for DSI2
21	RESERVED		R	0
20:18	VP2_LINE_BUFFER_SIZE	Determines the video line buffer size associated to video port 2 . Read 0x1: 512x24-bits, 682x18-bits, 768x16bits (memory of 384x32-bits) Read 0x2: 682x24-bits, 910x18-bits, 1024x16bits (memory of 512x32-bits) Read 0x3: 853x24-bits, 1137x18-bits, 1280x16bits (memory of 640x32-bits) Read 0x4: 1024x24-bits, 1365x18-bits, 1536x16bits (memory of 768x32-bits) Read 0x5: 1194x24-bits, 1592x18-bits, 1792x16bits (memory of 896x32-bits) Read 0x6: 1365x24-bits, 1820x18-bits, 2048x16bits (memory of 1024x32-bits)	R	0x4 for DSI1 0x1 for DSI2
17:16	VP1_NB_LINE_BUFFER	Determines the number of video buffer lines associated to video port 1. Read 0x0: No line buffer Read 0x1: 1 line buffer of the size defined in LINE_BUFFER_SIZE Read 0x2: 2 line buffers of the size defined in LINE_BUFFER_SIZE	R	0x2
15	RESERVED		R	0
14:12	VP1_LINE_BUFFER_SIZE	Determines the video line buffer size associated to video port 1 . Read 0x1: 512x24-bits, 682x18-bits, 768x16bits (memory of 384x32-bits) Read 0x2: 682x24-bits, 910x18-bits, 1024x16bits (memory of 512x32-bits) Read 0x3: 853x24-bits, 1137x18-bits, 1280x16bits (memory of 640x32-bits) Read 0x4: 1024x24-bits, 1365x18-bits, 1536x16bits (memory of 768x32-bits) Read 0x5: 1194x24-bits, 1592x18-bits, 1792x16bits (memory of 896x32-bits) Read 0x6: 1365x24-bits, 1820x18-bits, 2048x16bits (memory of 1024x32-bits)	R	0x6 for DSI1 0x4 for DSI2
11:9	NB_DATA_LANES	Determines the number of data lanes supported by the DSI protocol engine . Read 0x1: 1 Data lane Read 0x2: 2 Data lanes Read 0x3: 3 Data lanes Read 0x4: 4 Data lanes	R	0x4 for DSI1 0x2 for DSI2
8:6	NB_DMA_REQUEST	Determines the number of DMA_REQ signals. Read 0x0: No DMA request Read 0x1: 1 DMA request Read 0x2: 2 DMA requests Read 0x3: 3 DMA requests Read 0x4: 4 DMA requests	R	0x4

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Bits	Field Name	Description	Type	Reset
5:3	RX_FIFODEPTH	Determines the data RX FIFO depth (32-bit words) on the slave port. Read 0x4: 32x 33 bits Read 0x5: 64x 33 bits Read 0x6: 128 x 33 bits Read 0x7: 256 x 33 bits	R	0x6
2:0	TX_FIFODEPTH	Determines the data TX FIFO depth (33-bit words) on the slave port. Read 0x4: 32x 33 bits Read 0x5: 64x 33 bits Read 0x6: 128 x 33 bits Read 0x7: 256 x 33 bits	R	0x6

Table 10-533. Register Call Summary for Register DSI_GNQ

MIPI Display Serial Interface

- DSI_PROTOCOL_ENGINE Register Summary: [0] [1]
- DSI_PROTOCOL_ENGINE Register Description: [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23] [24] [25] [26] [27] [28] [29]

Table 10-534. DSI_COMPLEXIO_CFG1

Address Offset	0x0000 0048		
Physical Address	0x5800 4048 0x4804 4048 0x5800 5048 0x4804 5048	**Instance**	DSI1_PROTOCOL_ENGINE_L3 DSI1_PROTOCOL_ENGINE_PER_L4 DSI2_PROTOCOL_ENGINE_L3 DSI2_PROTOCOL_ENGINE_PER_L4
Description	COMPLEXIO CONFIGURATION REGISTER for the complex I/O This register contains the lane configuration for the order and position of the lanes (clock and data) and the polarity order for the control of the PHY differential signals in addition to the control bit for the power FSM.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SHADOWING	GOBIT	RESET_DONE	PWR_CMD		PWR_STATUS			RESERVED			RESERVED	RESERVED	DATA4_POL		DATA4_POSITION				DATA3_POL			DATA3_POSITION			DATA2_POL			DATA2_POSITION			DATA1_POL			DATA1_POSITION			CLOCK_POL			CLOCK_POSITION	

Bits	Field Name	Description	Type	Reset
31	SHADOWING	Shadowing configuration. 0x0: Disabled. The writes to the DSI_PHY_REGISTER0 through DSI_PHY_REGISTER2 registers is done like the other SCP registers. 0x1: Enabled. The writes to the DSI_PHY_REGISTER0 through DSI_PHY_REGISTER2 registers is done only when the GOBIT is set and when the signal DISPCUpdataSync from the display controller module is active.	RW	0

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Bits	Field Name	Description	Type	Reset
30	GOBIT	Allows the synchronized update of the shadow registers when the signal DISPCUpdateSync is active. 0x0: Resets the GOBIT. The hardware has finished the update of the shadow SCP registers. The bit is reset by Hardware. The software can reset the bit in case the user decides to abort it. There is no guarantee that the software reset is done before the transfer of the values to the complex IO. 0x1: Set the GOBIT. Only when the transfer of the new values for the three first registers is completed (3, 2, 1, or 0 transfers are performed based on the number of registers to update), the GOBIT is reset. The DISPCUpdateSync signal is used to synchronize the update. The bit shall be set only when it is in reset state.	RW	0
29	RESET_DONE	Internal reset monitoring of the power domain using the TXBYTECLKHS clock from the complex I/O Read 0x0: Internal module reset is on going. Read 0x1: Reset completed.	R	1
28:27	PWR_CMD	Command for power control of the complex I/O 0x0: Command to change to OFF state 0x1: Command to change to ON state 0x2: Command to change to ULTRALOW-POWER state	RW	0x0
26:25	PWR_STATUS	Status of the power control of the complex I/O Read 0x0: Complex I/O in OFF state Read 0x1: Complex I/O in ON state Read 0x2: Complex I/O in ULTRALOW-POWER state	R	0x0
24:22	RESERVED	Reserved	R	0x0
21	RESERVED	Reserved	R	0
20	RESERVED	Reserved	RW	0
19	DATA4_POL	+/- differential pin order of DATA lane 4. Applicable only to DS1. For DSI2 this bit field is RESERVED. 0x0: +/- pin order (DSI.DX=+ and DSi.DY=-) 0x1: -/+ pin order (DSI.DX=- and DSi.DY=+)	RW	0
18:16	DATA4_POSITION	Position and order of the DATA lane 4. Applicable only to DS1. For DSI2 this bit field is RESERVED. 0x0: Not used/connected 0x1: Data lane 4 is at the position 1 (line 1). 0x2: Data lane 4 is at the position 2 (line 2). 0x3: Data lane 4 is at the position 3 (line 3). 0x4: Data lane 4 is at the position 4 (line 4). 0x5: Data lane 4 is at the position 5 (line 5).	RW	0x0
15	DATA3_POL	+/- differential pin order of DATA lane 3. Applicable only to DS1. For DSI2 this bit field is RESERVED. 0x0: +/- pin order (DSI.DX=+ and DSi.DY=-) 0x1: -/+ pin order (DSI.DX=- and DSi.DY=+)	RW	0

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Bits	Field Name	Description	Type	Reset
14:12	DATA3_POSITION	Position and order of the DATA lane 3. Applicable only to DS1. For DSI2 this bit field is RESERVED. 0x0: Not used/connected 0x1: Data lane 3 is at the position 1 (line 1). 0x2: Data lane 3 is at the position 2 (line 2). 0x3: Data lane 3 is at the position 3 (line 3). 0x4: Data lane 3 is at the position 4 (line 4). 0x5: Data lane 3 is at the position 5 (line 5).	RW	0x0
11	DATA2_POL	+/- differential pin order of DATA lane 2. 0x0: +/- pin order (DSI.DX=+ and DSi.DY=-) 0x1: -/+ pin order (DSI.DX=- and DSi.DY=+)	RW	0
10:8	DATA2_POSITION	Position and order of the DATA lane 2. 0x0: Not used/connected 0x1: Data lane 2 is at the position 1 (line 1). 0x2: Data lane 2 is at the position 2 (line 2). 0x3: Data lane 2 is at the position 3 (line 3). 0x4: Data lane 2 is at the position 4 (line 4). 0x5: Data lane 2 is at the position 5 (line 5).	RW	0x0
7	DATA1_POL	+/- pin differential pin order of DATA lane 1 0x0: +/- pin order (DSI.DX=+ and DSi.DY=-) 0x1: -/+ pin order (DSI.DX=- and DSi.DY=+)	RW	0
6:4	DATA1_POSITION	Position and order of the DATA lane 1. The data lane 1 is always present. 0x1: Data lane 1 is at the position 1 (line 1). 0x2: Data lane 1 is at the position 2 (line 2). 0x3: Data lane 1 is at the position 3 (line 3). 0x4: Data lane 1 is at the position 4 (line 4). 0x5: Data lane 1 is at the position 5 (line 5).	RW	0x0
3	CLOCK_POL	+/- differential pin order of CLOCK lane. 0x0: +/- pin order (DSI.DX=+ and DSi.DY=-) 0x1: -/+ pin order (DSI.DX=- and DSi.DY=+)	RW	0
2:0	CLOCK_POSITION	Position and order of the CLOCK lane. 0, 5, 6 and 7 are reserved. The clock lane is always present but cannot be at the position 5 even if the COMPLEX I/O consists of 5 lanes. 0x1: Clock lane is at the position 1 (line 1). 0x2: Clock lane is at the position 2 (line 2). 0x3: Clock lane is at the position 3 (line 3). 0x4: Clock lane is at the position 4 (line 4).	RW	0x0

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Table 10-535. Register Call Summary for Register DSI_COMPLEXIO_CFG1

MIPI Display Serial Interface

- Data/Clock Configuration: [0]
- DSI Protocol Overview: [1]
- SCP Interface: [2] [3] [4] [5] [6] [7] [8]
- Power Control of DSI PHY Complex I/O and DSI PLL: [9] [10]
- Ultralow-Power State Configuration: [11] [12]
- Software Reset: [13]
- Pad Configuration: [14] [15] [16] [17] [18]
- Display Timing Configuration: [19]
- DSI Video Mode Using the DISPC Video Port: [20] [21] [22] [23] [24] [25]
- DSI Command Mode Using the DISPC Video Port: [26] [27] [28] [29] [30] [31]
- DSI_PROTOCOL_ENGINE Register Summary: [32] [33]

Table 10-536. DSI_COMPLEXIO_IRQSTATUS

Address Offset	0x0000 004C		
Physical Address	0x5800 404C 0x4804 404C 0x5800 504C 0x4804 504C	**Instance**	DSI1_PROTOCOL_ENGINE_L3 DSI1_PROTOCOL_ENGINE_PER_L4 DSI2_PROTOCOL_ENGINE_L3 DSI2_PROTOCOL_ENGINE_PER_L4
Description	INTERRUPT STATUS REGISTER - All errors from complex I/O		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ULPSACTIVENOT_ALL1_IRQ	ULPSACTIVENOT_ALL0_IRQ	ERRCONTENTIONLP1_5_IRQ	ERRCONTENTIONLP0_5_IRQ	ERRCONTENTIONLP1_4_IRQ	ERRCONTENTIONLP0_4_IRQ	ERRCONTENTIONLP1_3_IRQ	ERRCONTENTIONLP0_3_IRQ	ERRCONTENTIONLP1_2_IRQ	ERRCONTENTIONLP0_2_IRQ	ERRCONTENTIONLP1_1_IRQ	ERRCONTENTIONLP0_1_IRQ	STATEULPS5_IRQ	STATEULPS4_IRQ	STATEULPS3_IRQ	STATEULPS2_IRQ	STATEULPS1_IRQ	ERRCONTROL5_IRQ	ERRCONTROL4_IRQ	ERRCONTROL3_IRQ	ERRCONTROL2_IRQ	ERRCONTROL1_IRQ	ERRESC5_IRQ	ERRESC4_IRQ	ERRESC3_IRQ	ERRESC2_IRQ	ERRESC1_IRQ	ERRSYNCESC5_IRQ	ERRSYNCESC4_IRQ	ERRSYNCESC3_IRQ	ERRSYNCESC2_IRQ	ERRSYNCESC1_IRQ

Bits	Field Name	Description	Type	Reset
31	ULPSACTIVENOT_ALL1_IRQ	All the ULPSActiveNOT signals corresponding to the lanes with TXULPSExit being high are high. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW	0
30	ULPSACTIVENOT_ALL0_IRQ	All signals ULPSActiveNOT are 0 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW	0
29	ERRCONTENTIONLP1_5_IRQ	Contention LP1 error for lane 5 Applicable only to DS1. For DSI2 this bit field is RESERVED. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW	0

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Bits	Field Name	Description	Type	Reset
28	ERRCONTENTIONLP0_5_IRQ	Contention LP0 error for lane 5 Applicable only to DS1. For DSI2 this bit field is RESERVED. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW	0
27	ERRCONTENTIONLP1_4_IRQ	Contention LP1 error for lane 4 Applicable only to DS1. For DSI2 this bit field is RESERVED. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW	0
26	ERRCONTENTIONLP0_4_IRQ	Contention LP0 error for lane 4 Applicable only to DS1. For DSI2 this bit field is RESERVED. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW	0
25	ERRCONTENTIONLP1_3_IRQ	Contention LP1 error for lane 3 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW	0
24	ERRCONTENTIONLP0_3_IRQ	Contention LP0 error for lane 3 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW	0
23	ERRCONTENTIONLP1_2_IRQ	Contention LP1 error for lane 2 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW	0
22	ERRCONTENTIONLP0_2_IRQ	Contention LP0 error for lane 2 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW	0
21	ERRCONTENTIONLP1_1_IRQ	Contention LP1 error for lane 1 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW	0
20	ERRCONTENTIONLP0_1_IRQ	Contention LP0 error for lane 1 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW	0
19	STATEULPS5_IRQ	lane 5 in ULTRALOW-POWER State Applicable only to DS1. For DSI2 this bit field is RESERVED. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW	0

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Bits	Field Name	Description	Type	Reset
18	STATEULPS4_IRQ	lane 4 in ultralow-power mode Applicable only to DS1. For DSI2 this bit field is RESERVED. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW	0
17	STATEULPS3_IRQ	lane 3 in ULTRALOW-POWER state 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW	0
16	STATEULPS2_IRQ	lane 2 in ULTRALOW-POWER state 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW	0
15	STATEULPS1_IRQ	lane 1 in ULTRALOW-POWER state 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW	0
14	ERRCONTROL5_IRQ	Control error for lane 5 Applicable only to DS1. For DSI2 this bit field is RESERVED. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW	0
13	ERRCONTROL4_IRQ	Control error for lane 4 Applicable only to DS1. For DSI2 this bit field is RESERVED. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW	0
12	ERRCONTROL3_IRQ	Control error for lane 3 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW	0
11	ERRCONTROL2_IRQ	Control error for lane 2 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW	0
10	ERRCONTROL1_IRQ	Control error for lane 1 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW	0
9	ERRESC5_IRQ	Escape entry error for lane 5 Applicable only to DS1. For DSI2 this bit field is RESERVED. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW	0

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Bits	Field Name	Description	Type	Reset
8	ERRESC4_IRQ	Escape entry error for lane 4 Applicable only to DS1. For DSI2 this bit field is RESERVED. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW	0
7	ERRESC3_IRQ	Escape entry error for lane 3 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW	0
6	ERRESC2_IRQ	Escape entry error for lane 2 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW	0
5	ERRESC1_IRQ	Escape entry error for lane 1 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW	0
4	ERRSYNCESC5_IRQ	Low power Data transmission synchronization error for lane 5 Applicable only to DS1. For DSI2 this bit field is RESERVED. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW	0
3	ERRSYNCESC4_IRQ	Low power Data transmission synchronization error for lane 4 Applicable only to DS1. For DSI2 this bit field is RESERVED. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW	0
2	ERRSYNCESC3_IRQ	Low power Data transmission synchronization error for lane 3 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW	0
1	ERRSYNCESC2_IRQ	Low power Data transmission synchronization error for lane 2 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW	0
0	ERRSYNCESC1_IRQ	Low power Data transmission synchronization error for lane 1 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW	0

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Table 10-537. Register Call Summary for Register DSI_COMPLEXIO_IRQSTATUS

MIPI Display Serial Interface

- DSI Interrupt Requests: [0] [1]
- Timers: [2]
- Ultralow-Power State Configuration: [3] [4]
- Error Handling: [5] [6] [7] [8] [9] [10] [11] [12] [13]
- DSI Video Mode Using the DISPC Video Port: [14]
- DSI Command Mode Using the DISPC Video Port: [15]
- DSI_PROTOCOL_ENGINE Register Summary: [16] [17]
- DSI_PROTOCOL_ENGINE Register Description: [18]

Table 10-538. DSI_COMPLEXIO_IRQENABLE

Address Offset	0x0000 0050		
Physical Address	0x5800 4050 0x4804 4050 0x5800 5050 0x4804 5050	**Instance**	DSI1_PROTOCOL_ENGINE_L3 DSI1_PROTOCOL_ENGINE_PER_L4 DSI2_PROTOCOL_ENGINE_L3 DSI2_PROTOCOL_ENGINE_PER_L4
Description	INTERRUPT ENABLE REGISTER - All errors from complex I/O		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ULPSACTIVENOT_ALL1_IRQ_EN	ULPSACTIVENOT_ALL0_IRQ_EN	ERRCONTENTIONLP1_5_IRQ_EN	ERRCONTENTIONLP0_5_IRQ_EN	ERRCONTENTIONLP1_4_IRQ_EN	ERRCONTENTIONLP0_4_IRQ_EN	ERRCONTENTIONLP1_3_IRQ_EN	ERRCONTENTIONLP0_3_IRQ_EN	ERRCONTENTIONLP1_2_IRQ_EN	ERRCONTENTIONLP0_2_IRQ_EN	ERRCONTENTIONLP1_1_IRQ_EN	ERRCONTENTIONLP0_1_IRQ_EN	STATEULPS5_IRQ_EN	STATEULPS4_IRQ_EN	STATEULPS3_IRQ_EN	STATEULPS2_IRQ_EN	STATEULPS1_IRQ_EN	ERRCONTROL5_IRQ_EN	ERRCONTROL4_IRQ_EN	ERRCONTROL3_IRQ_EN	ERRCONTROL2_IRQ_EN	ERRCONTROL1_IRQ_EN	ERRESC5_IRQ_EN	ERRESC4_IRQ_EN	ERRESC3_IRQ_EN	ERRESC2_IRQ_EN	ERRESC1_IRQ_EN	ERRSYNCSESC5_IRQ_EN	ERRSYNCSESC4_IRQ_EN	ERRSYNCSESC3_IRQ_EN	ERRSYNCSESC2_IRQ_EN	ERRSYNCSESC1_IRQ_EN

Bits	Field Name	Description	Type	Reset
31	ULPSACTIVENOT_ALL1_IRQ_EN	All the ULPSActiveNOT signals corresponding to the lanes with TXULPSExit being high are high. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
30	ULPSACTIVENOT_ALL0_IRQ_EN	All signals ULPSActiveNOT are 0 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
29	ERRCONTENTIONLP1_5_IRQ_EN	Contention LP1 error for lane 5 Applicable only to DS1. For DSI2 this bit field is RESERVED. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
28	ERRCONTENTIONLP0_5_IRQ_EN	Contention LP0 error for lane 5 Applicable only to DS1. For DSI2 this bit field is RESERVED. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0

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Bits	Field Name	Description	Type	Reset
27	ERRCONTENTIONLP1_4_IRQ_EN	Contention LP1 error for lane 4 Applicable only to DS1. For DSI2 this bit field is RESERVED. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
26	ERRCONTENTIONLP0_4_IRQ_EN	Contention LP0 error for lane 4 Applicable only to DS1. For DSI2 this bit field is RESERVED. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
25	ERRCONTENTIONLP1_3_IRQ_EN	Contention LP1 error for lane 3 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
24	ERRCONTENTIONLP0_3_IRQ_EN	Contention LP0 error for lane 3 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
23	ERRCONTENTIONLP1_2_IRQ_EN	Contention LP1 error for lane 2 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
22	ERRCONTENTIONLP0_2_IRQ_EN	Contention LP0 error for lane 2 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
21	ERRCONTENTIONLP1_1_IRQ_EN	Contention LP1 error for lane 1 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
20	ERRCONTENTIONLP0_1_IRQ_EN	Contention LP0 error for lane 1 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
19	STATEULPS5_IRQ_EN	lane 5 in ULTRALOW-POWER state Applicable only to DS1. For DSI2 this bit field is RESERVED. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
18	STATEULPS4_IRQ_EN	lane 4 in ULTRALOW-POWER state Applicable only to DS1. For DSI2 this bit field is RESERVED. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
17	STATEULPS3_IRQ_EN	lane 3 in ULTRALOW-POWER state 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
16	STATEULPS2_IRQ_EN	lane 2 in ULTRALOW-POWER state 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
15	STATEULPS1_IRQ_EN	lane 1 in ULTRALOW-POWER state 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
14	ERRCONTROL5_IRQ_EN	Control error for lane 5 Applicable only to DS1. For DSI2 this bit field is RESERVED. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0

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Bits	Field Name	Description	Type	Reset
13	ERRCONTROL4_IRQ_EN	Control error for lane 4 Applicable only to DS1. For DSI2 this bit field is RESERVED. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
12	ERRCONTROL3_IRQ_EN	Control error for lane 3 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
11	ERRCONTROL2_IRQ_EN	Control error for lane 2 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
10	ERRCONTROL1_IRQ_EN	Control error for lane 1 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
9	ERRESC5_IRQ_EN	Escape entry error for lane 5 Applicable only to DS1. For DSI2 this bit field is RESERVED. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
8	ERRESC4_IRQ_EN	Escape entry error for lane 4 Applicable only to DS1. For DSI2 this bit field is RESERVED. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
7	ERRESC3_IRQ_EN	Escape entry error for lane 3 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
6	ERRESC2_IRQ_EN	Escape entry error for lane 2 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
5	ERRESC1_IRQ_EN	Escape entry error for lane 1 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
4	ERRSYNCSESC5_IRQ_EN	Low power Data transmission synchronization error for lane 5 Applicable only to DS1. For DSI2 this bit field is RESERVED. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
3	ERRSYNCSESC4_IRQ_EN	Low power Data transmission synchronization error for lane 4 Applicable only to DS1. For DSI2 this bit field is RESERVED. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
2	ERRSYNCSESC3_IRQ_EN	Low power Data transmission synchronization error for lane 3 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
1	ERRSYNCSESC2_IRQ_EN	Low power Data transmission synchronization error for lane 2 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0

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Bits	Field Name	Description	Type	Reset
0	ERRSYNCSESC1_IRQ_EN	Low power Data transmission synchronization error for lane 1 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0

Table 10-539. Register Call Summary for Register DSI_COMPLEXIO_IRQENABLE

MIPI Display Serial Interface

- DSI Video Mode Using the DISPC Video Port: [0]
- DSI Command Mode Using the DISPC Video Port: [1]
- DSI_PROTOCOL_ENGINE Register Summary: [2] [3]

Table 10-540. DSI_CLK_CTRL

Address Offset	0x0000 0054		
Physical Address	0x5800 4054 0x4804 4054 0x5800 5054 0x4804 5054	**Instance**	DSI1_PROTOCOL_ENGINE_L3 DSI1_PROTOCOL_ENGINE_PER_L4 DSI2_PROTOCOL_ENGINE_L3 DSI2_PROTOCOL_ENGINE_PER_L4
Description	CLOCK CONTROL This register controls the CLOCK GENERATION. The register can be modified only when IF_EN is reset.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PLL_PWR_CMD		PLL_PWR_STATUS		RESERVED						LP_RX_SYNCHRO_ENABLE	LP_CLK_ENABLE	HS_MANUAL_STOP_CTRL	HS_AUTO_STOP_ENABLE	LP_CLK_NULL_PACKET_SIZE		LP_CLK_NULL_PACKET_ENABLE	CIO_CLK_ICG	DDR_CLK_ALWAYS_ON	LP_CLK_DIVISOR										

Bits	Field Name	Description	Type	Reset
31:30	PLL_PWR_CMD	Command for power control of the DSI PLL Control module 0x0: Command to change to OFF state 0x1: Command to change to ON state for PLL only (HSDIVISER is OFF) 0x2: Command to change to ON state for both PLL and HSDIVISER 0x3: Command to change to ON state for both PLL and HSDIVISER (no clock output to the DSI complex I/O)	RW	0x0

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Bits	Field Name	Description	Type	Reset
29:28	PLL_PWR_STATUS	Status of the power control of the DSI PLL Control module Read 0x0: DSI PLL Control module in OFF state Read 0x1: DSI PLL Control module in ON state for PLL only (HSDIVISER is OFF) Read 0x2: DSI PLL Control module in ON state for both PLL and HSDIVISER Read 0x3: DSI PLL Control module in ON state for both PLL and HSDIVISER (no clock output to the DSI complex I/O)	R	0x0
27:22	RESERVED		R	0x00
21	LP_RX_SYNCHRO_ENABLE	Defines if the functional is higher or lower than 30 MHz. The information is used to define synchronization to be used for RxValidEsc. 0x0: The DSI functional clock is equal or slower than 30 MHz. The synchronization is falling/rising. 0x1: The DSI functional clock is higher than 30 MHz. The synchronization is rising/rising.	RW	0
20	LP_CLK_ENABLE	Controls the gating of the TXCLKESC clock. 0x0: Disabled. The clock is not generated. The value of LP_CLK_DIVISOR is not used and does not need to be programmed. 0x1: Enabled. The clock is generated. The value of LP_CLK_DIVISOR is used and needs to be programmed.	RW	0
19	HS_MANUAL_STOP_CTRL	In case HS_AUTO_STOP_ENABLE=0, the bit field allows manual control of the assertion/de-assertion of the signal DSIStopClk by the user. 0x0: DSIStopClk de-assertion unconditionally. 0x1: DSIStopClk assertion unconditionally.	RW	0
18	HS_AUTO_STOP_ENABLE	Enables the automatic assertion/de-assertion of DSIStopClk signal. 0x0: Auto mode disabled. 0x1: Auto mode enabled.	RW	0
17:16	LP_CLK_NULL_PACKET_SIZE	Indicates the size of LP NULL Packets to be sent automatically when after the last LP packet transfer. It is used by the receiver to drain its internal pipeline. The valid values are from 0 to 3 bytes for the payload size.	RW	0x0
15	LP_CLK_NULL_PACKET_ENABLE	Enables the generation of NULL packet in low speed. 0x0: Disabled. The NULL packet is not sent in LP mode after the last LP packet. 0x1: Enabled. The NULL packet is sent in LP mode after the last LP packet.	RW	0
14	CIO_CLK_ICG	Gates SCPClk clock provided to DSI_PHY and PLL-CTRL module. 0x0: Disabled. SCPClk is not generated. It remains at 0. 0x1: Enabled. SCPClk is generated (OCP_CLK/4)	RW	0
13	DDR_CLK_ALWAYS_ON	Defines if the DDR clock is also sent when there is no HS packets sent to the peripheral (low-power mode). So TXRequest for the clock lane is not de-asserted. 0x0: Disabled. The DDR clock is only provided when HS packets are sent. 0x1: Enabled. The DDR clock is always sent to the peripheral regardless of the state of the data lanes (HS or LS mode).	RW	0
12:0	LP_CLK_DIVISOR	Defines the ratio to be used for the generation of the low-power mode clock from DSI functional clock. The supported values are from 1 to 8191(the value 0 is invalid). The output frequency shall be in the range between 20 MHz and 32 kHz.	RW	0x0001

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Table 10-541. Register Call Summary for Register DSI_CLK_CTRL

MIPI Display Serial Interface

- DSI Transfer Modes: [0]
- Clock Requirements: [1] [2] [3] [4] [5] [6] [7]
- Power Management: [8]
- Power Control of DSI PHY Complex I/O and DSI PLL: [9] [10] [11] [12] [13] [14] [15] [16]
- Ultralow-Power State Configuration: [17]
- Pad Configuration: [18] [19]
- Display Timing Configuration: [20]
- DSI Video Mode Using the DISPC Video Port: [21] [22] [23] [24] [25] [26] [27] [28]
- DSI Command Mode Using the DISPC Video Port: [29] [30] [31] [32] [33] [34] [35] [36]
- DSI_PROTOCOL_ENGINE Register Summary: [37] [38]
- DSI_PROTOCOL_ENGINE Register Description: [39] [40]

Table 10-542. DSI_TIMING1

Address Offset	0x0000 0058		
Physical Address	0x5800 4058 0x4804 4058 0x5800 5058 0x4804 5058	**Instance**	DSI1_PROTOCOL_ENGINE_L3 DSI1_PROTOCOL_ENGINE_PER_L4 DSI2_PROTOCOL_ENGINE_L3 DSI2_PROTOCOL_ENGINE_PER_L4
Description	TIMING1 REGISTER This register controls the DSI Protocol Engine module timers. Any bit field can be modified while DSI_CTRL[0] IF_EN is set to '1'. It is used to indicate the number of DSI1_CLK and DSI2_CLK functional clocks cycles for the timers FORCE_TX_STOP_TIMER and TA_TO_TIMER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TA_TO	TA_TO_X16	TA_TO_X8	TA_TO_COUNTER													FORCE_TX_STOP_MODE_IO	STOP_STATE_X16_IO	STOP_STATE_X4_IO	STOP_STATE_COUNTER_IO												

Bits	Field Name	Description	Type	Reset
31	TA_TO	Enables the turn-around timer 0x0: Turn-around counter is disabled. 0x1: Turn-around counter is enabled (required to receive TA interrupt in case the turn-around procedure is not successful).	RW	0
30	TA_TO_X16	Multiplication factor for the number of DSI_CLK functional clocks cycles defined in TA_TO_COUNTER bit field 0x0: The number of DSI_CLK functional clock cycles defined in TA_TO_COUNTER is multiplied by 1x 0x1: The number of DSI_CLK functional clock cycles defined in TA_TO_COUNTER is multiplied by 16x	RW	1

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Bits	Field Name	Description	Type	Reset
29	TA_TO_X8	Multiplication factor for the number of DSI_CLK functional clock cycles defined in TA_TO_COUNTER bit field 0x0: The number of DSI_CLK functional clock cycles defined in TA_TO_COUNTER is multiplied by 1x 0x1: The number of DSI_CLK functional clock cycles defined in TA_TO_COUNTER is multiplied by 8x	RW	1
28:16	TA_TO_COUNTER	Turn around counter. It indicates the number of DSI_CLK function clock to wait for the change of the Direction PPI signal according to the TurnRequest signal The value is from 0 to 8191.	RW	0x1FFF
15	FORCE_TX_STOP_MODE_IO	Control of ForceTxStopMode signal 0x0: De-assertion of ForceTxStopMode. The hardware reset the bit at the end of the ForceTXStopMode assertion. The software can reset the bit in order to stop the assertion of the ForceTXStopMode signal prior to the completion of the period. 0x1: Assertion of ForceTxStopMode	RW	0
14	STOP_STATE_X16_IO	Multiplication factor for the number of DSI_CLK functional clock cycles defined in STOP_STATE_COUNTER_IO bit field 0x0: The number of DSI_CLK functional clock cycles defined in STOP_STATE _COUNTER_IO is multiplied by 1x 0x1: The number of DSI_CLK functional clock cycles defined in STOP_STATE _COUNTER_IO is multiplied by 16x	RW	1
13	STOP_STATE_X4_IO	Multiplication factor for the number of DSI_CLK functional clock cycles defined in STOP_STATE_COUNTER_IO bit field 0x0: The number of DSI_CLK functional clock cycles defined in STOP_STATE _COUNTER is multiplied by 1x 0x1: The number of DSI_CLK functional clock cycles defined in STOP_STATE _COUNTER_IO is multiplied by 4x	RW	1
12:0	STOP_STATE_COUNTER_IO	Stop state counter. It indicates the number of DSI_CLK function clock to assert ForceTXStopMode signal. The value is from 0 to 8191.	RW	0x1FFF

Table 10-543. Register Call Summary for Register DSI_TIMING1

MIPI Display Serial Interface

- Timers: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9]
- DSI Video Mode Using the DISPC Video Port: [10] [11] [12]
- DSI Command Mode Using the DISPC Video Port: [13] [14] [15] [16] [17] [18]
- DSI_PROTOCOL_ENGINE Register Summary: [19] [20]

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Table 10-544. DSI_TIMING2

Address Offset	0x0000 005C		
Physical Address	0x5800 405C 0x4804 405C 0x5800 505C 0x4804 505C	**Instance**	DSI1_PROTOCOL_ENGINE_L3 DSI1_PROTOCOL_ENGINE_PER_L4 DSI2_PROTOCOL_ENGINE_L3 DSI2_PROTOCOL_ENGINE_PER_L4
Description	TIMING2 REGISTER This register controls the DSI Protocol Engine module timers. Any bit field can be modified while DSI_CTRL[0] IF_EN is set to '1'. It is used to indicate the number of DSI_FCLK clock cycles for the timer LP_RX_TIMER and the number of BYTE_CLK functional clock cycles for the timer HS_TX_TIMER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HS_TX_TO	HS_TX_TO_X64	HS_TX_TO_X16	HS_TX_TO_COUNTER													LP_RX_TO	LP_RX_TO_X16	LP_RX_TO_X4	LP_RX_TO_COUNTER												

Bits	Field Name	Description	Type	Reset
31	HS_TX_TO	Enables the HS TX timer. 0x0: Time-out counter is disabled. 0x1: Time-out counter is enabled (required to receive TA interrupt in case the turn-around procedure is not successful).	RW	0
30	HS_TX_TO_X64	Multiplication factor for the number of BYTE_CLK functional clock cycles defined in HS_TX_COUNTER bit field. BYTE_CLK is a high speed transmit byte clock signal generated by the DSI_PHY. 0x0: The number of BYTE_CLK functional clock cycles defined in HS_TX_TO_COUNTER is multiplied by 1x 0x1: The number of BYTE_CLK functional clock cycles defined in HS_TX_TO_COUNTER is multiplied by 64x	RW	1
29	HS_TX_TO_X16	Multiplication factor for the number of BYTE_CLK functional clock cycles defined in HS_TX_COUNTER bit 0x0: The number of BYTE_CLK functional clock cycles defined in HS_TX_TO_COUNTER is multiplied by 1x 0x1: The number of BYTE_CLK functional clock cycles defined in HS_TX_TO_COUNTER is multiplied by 16x	RW	1
28:16	HS_TX_TO_COUNTER	HS_TX_TIMER counter. It indicates the number of BYTE_CLK function clock for the HS TX timer. The value is from 0 to 8191.	RW	0x1FFF
15	LP_RX_TO	Enables the LP RX timer. 0x0: Turn-around counter is disabled. 0x1: Turn-around counter is enabled (required to receive TA interrupt in case the turn-around procedure is not successful).	RW	0
14	LP_RX_TO_X16	Multiplication factor for the number of DSI_FCLK clock cycles defined in LP_RX_COUNTER bit field 0x0: The number of DSI_FCLK clock cycles defined in LP_RX_TO_COUNTER is multiplied by 1x 0x1: The number of DSI_FCLK clock cycles defined in LP_RX_TO_COUNTER is multiplied by 16x	RW	1

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Bits	Field Name	Description	Type	Reset
13	LP_RX_TO_X4	Multiplication factor for the number of DSI_FCLK clock cycles defined in LP_RX_COUNTER bit 0x0: The number of DSI_FCLK clock cycles defined in LP_RX_TO_COUNTER is multiplied by 1x 0x1: The number of DSI_FCLK clock cycles defined in LP_RX_TO_COUNTER is multiplied by 4x	RW	1
12:0	LP_RX_TO_COUNTER	LP_RX_TIMER counter. It indicates the number of DSI_FCLK clock for the LP RX timer. The value is from 0 to 8191.	RW	0x1FFF

Table 10-545. Register Call Summary for Register DSI_TIMING2

MIPI Display Serial Interface

- Timers: [0] [1] [2] [3] [4] [5] [6] [7] [8]
- DSI Video Mode Using the DISPC Video Port: [9] [10] [11] [12]
- DSI Command Mode Using the DISPC Video Port: [13] [14] [15] [16] [17] [18]
- DSI_PROTOCOL_ENGINE Register Summary: [19] [20]

Table 10-546. DSI_VM_TIMING1

Address Offset	0x0000 0060		
Physical Address	0x5800 4060 0x4804 4060 0x5800 5060 0x4804 5060	**Instance**	DSI1_PROTOCOL_ENGINE_L3 DSI1_PROTOCOL_ENGINE_PER_L4 DSI2_PROTOCOL_ENGINE_L3 DSI2_PROTOCOL_ENGINE_PER_L4
Description	VIDEO MODE TIMING REGISTER This register defines the video mode timing.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HSA								HFP																HBP							

Bits	Field Name	Description	Type	Reset
31:24	HSA	Defines the horizontal Sync active period used in video mode in number of byte clock cycles (TXBYTECLKHS clock) The supported values are from 0 to 255.	RW	0x00
23:12	HFP	Defines the horizontal front porch used in video mode in number of byte clock cycles (TXBYTECLKHS clock) The supported values are from 0 to 4095	RW	0x000
11:0	HBP	Defines the horizontal back porch used in video mode in number of byte clock cycles (TXBYTECLKHS clock) The supported values are from 0 to 4095	RW	0x000

Table 10-547. Register Call Summary for Register DSI_VM_TIMING1

MIPI Display Serial Interface

- Blanking: [0]
- DSI Transfer Modes: [1]
- DSI Video Mode Using the DISPC Video Port: [2] [3] [4]
- DSI_PROTOCOL_ENGINE Register Summary: [5] [6]

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Table 10-548. DSI_VM_TIMING2

Address Offset	0x0000 0064		
Physical Address	0x5800 4064 0x4804 4064 0x5800 5064 0x4804 5064	**Instance**	DSI1_PROTOCOL_ENGINE_L3 DSI1_PROTOCOL_ENGINE_PER_L4 DSI2_PROTOCOL_ENGINE_L3 DSI2_PROTOCOL_ENGINE_PER_L4
Description	VIDEO MODE TIMING REGISTER This register defines the video mode timing.		
Type	RW		

31 30 29 28	27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
RESERVED	WINDOW_SYNC	VSA	VFP	VBP

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:24	WINDOW_SYNC	Number of BYTE clock cycles for the synchronization window. An interrupt for synchronization lost is generated when the received synchornization on video port is not inside the window. DSI does not change its own timings if the synch is inside the window. The valid values are from 4 to 15.	RW	0x0
23:16	VSA	Defines the vertical Sync active period used in video mode in number of lines. The supported values are from 0 to 255 It is used to generate the short packet for End of Vertical synchronization.	RW	0x00
15:8	VFP	Defines the vertical front porch used in video mode in number of lines. The supported values are from 0 to 255	RW	0x00
7:0	VBP	Defines the vertical back porch used in video mode in number of lines. The supported values are from 0 to 255	RW	0x00

Table 10-549. Register Call Summary for Register DSI_VM_TIMING2

MIPI Display Serial Interface

- DSI Transfer Modes: [0]
- Video Port Interface: [1]
- DSI Video Mode Using the DISPC Video Port: [2] [3] [4] [5]
- DSI_PROTOCOL_ENGINE Register Summary: [6] [7]

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Table 10-550. DSI_VM_TIMING3

Address Offset	0x0000 0068		
Physical Address	0x5800 4068 0x4804 4068 0x5800 5068 0x4804 5068	**Instance**	DSI1_PROTOCOL_ENGINE_L3 DSI1_PROTOCOL_ENGINE_PER_L4 DSI2_PROTOCOL_ENGINE_L3 DSI2_PROTOCOL_ENGINE_PER_L4
Description	VIDEO MODE TIMING REGISTER This register defines the video mode timing.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TL																VACT															

Bits	Field Name	Description	Type	Reset
31:16	TL	Defines the number of length of the line in video mode in number of byte clock cycles (TXBYTECLKHS clock) The supported values are from 0 to 8192. The values from 8193 to 65535 are not supported.	RW	0x0000
15:0	VACT	Defines the number of active lines used in video mode. The supported values are from 0 to 65535	RW	0x0000

Table 10-551. Register Call Summary for Register DSI_VM_TIMING3

MIPI Display Serial Interface

- Video Port Interface: [0]
- DSI Video Mode Using the DISPC Video Port: [1] [2]
- DSI_PROTOCOL_ENGINE Register Summary: [3] [4]

Table 10-552. DSI_CLK_TIMING

Address Offset	0x0000 006C		
Physical Address	0x5800 406C 0x4804 406C 0x5800 506C 0x4804 506C	**Instance**	DSI1_PROTOCOL_ENGINE_L3 DSI1_PROTOCOL_ENGINE_PER_L4 DSI2_PROTOCOL_ENGINE_L3 DSI2_PROTOCOL_ENGINE_PER_L4
Description	CLOCK TIMING REGISTER This register controls the DSI Protocol Engine module timers. This register shall not be modified while DSI_CTRL.IF_EN is set to '1'.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																DDR_CLK_PRE								DDR_CLK_POST							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:8	DDR_CLK_PRE	Indicates the number of TXBYTECLKHS clock cycles between the start of the DDR clock and the assertion of the data request signal. The values from 1 to 255 are valid. The value 0 is reserved. The value is not used if DSI_CLK_CTRL[13] DDR_CLK_ALWAYS_ON is set to '1' since the DDR clock is always present.	RW	0x01

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Bits	Field Name	Description	Type	Reset
7:0	DDR_CLK_POST	Indicates the number of TXBYTECLKHS clock cycles after the de-assertion of the data request signal and the stop of the DDR clock. The values from 1 to 255 are valid. The value 0 is reserved. The value is not used if DSI_CLK_CTRL[13] DDR_CLK_ALWAYS_ON is set to '1' since the DDR clock is always present.	RW	0x01

Table 10-553. Register Call Summary for Register DSI_CLK_TIMING

MIPI Display Serial Interface

- Clock Requirements: [0] [1] [2] [3]
- DSI Video Mode Using the DISPC Video Port: [4] [5]
- DSI Command Mode Using the DISPC Video Port: [6] [7]
- DSI_PROTOCOL_ENGINE Register Summary: [8] [9]

Table 10-554. DSI_TX_FIFO_VC_SIZE

Address Offset	0x0000 0070		
Physical Address	0x5800 4070 0x4804 4070 0x5800 5070 0x4804 5070	**Instance**	DSI1_PROTOCOL_ENGINE_L3 DSI1_PROTOCOL_ENGINE_PER_L4 DSI2_PROTOCOL_ENGINE_L3 DSI2_PROTOCOL_ENGINE_PER_L4
Description	Defines the corresponding memory entries allocated for each virtual channel. The virtual channel shall be disabled in order to allocate/un-allocate some entries in the TX FIFO.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VC3_FIFO_SIZE				RESERVED	VC3_FIFO_ADD			VC2_FIFO_SIZE				RESERVED	VC2_FIFO_ADD			VC1_FIFO_SIZE				RESERVED	VC1_FIFO_ADD			VC0_FIFO_SIZE				RESERVED	VC0_FIFO_ADD		

Bits	Field Name	Description	Type	Reset
31:28	VC3_FIFO_SIZE	Size of the FIFO allocated for virtual channel 3. For a complete description, refer to Table 10-475, *Virtual Channel TX FIFO Size Values.*	RW	0x0
27	RESERVED		R	0
26:24	VC3_FIFO_ADD	Address of the space allocated in the FIFO for virtual channel 3. For a complete description, refer to Table 10-476, *Virtual Channel TX FIFO Start Address.*	RW	0x0
23:20	VC2_FIFO_SIZE	Size of the FIFO allocated for virtual channel 2. For a complete description, refer to Table 10-475, *Virtual Channel TX FIFO Size Values.*	RW	0x0
19	RESERVED		R	0
18:16	VC2_FIFO_ADD	Address of the space allocated in the FIFO for virtual channel 2. For a complete description, refer to Table 10-476, *Virtual Channel TX FIFO Start Address.*	RW	0x0
15:12	VC1_FIFO_SIZE	Size of the FIFO allocated for virtual channel 1. For a complete description, refer to Table 10-475, *Virtual Channel TX FIFO Size Values.*	RW	0x0
11	RESERVED		R	0
10:8	VC1_FIFO_ADD	Address of the space allocated in the FIFO for virtual channel 1. For a complete description, refer to Table 10-476, *Virtual Channel TX FIFO Start Address.*	RW	0x0

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Bits	Field Name	Description	Type	Reset
7:4	VC0_FIFO_SIZE	Size of the FIFO allocated for virtual channel 0. For a complete description, refer to Table 10-475, *Virtual Channel TX FIFO Size Values.*	RW	0x0
3	RESERVED		R	0
2:0	VC0_FIFO_ADD	Address of the space allocated in the FIFO for virtual channel 0. For a complete description, refer to Table 10-476, *Virtual Channel TX FIFO Start Address.*	RW	0x0

Table 10-555. Register Call Summary for Register DSI_TX_FIFO_VC_SIZE

MIPI Display Serial Interface

- DSI Transfer Modes: [0] [1] [2] [3] [4]
- DSI Command Mode Using the DISPC Video Port: [5]
- DSI_PROTOCOL_ENGINE Register Summary: [6] [7]

Table 10-556. DSI_RX_FIFO_VC_SIZE

Address Offset	0x0000 0074		
Physical Address	0x5800 4074 0x4804 4074 0x5800 5074 0x4804 5074	**Instance**	DSI1_PROTOCOL_ENGINE_L3 DSI1_PROTOCOL_ENGINE_PER_L4 DSI2_PROTOCOL_ENGINE_L3 DSI2_PROTOCOL_ENGINE_PER_L4
Description	Defines the corresponding memory entries allocated for each virtual channel and the addresses. The virtual channel shall be disabled in order to allocate/un-allocate some entries in the RX FIFO.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VC3_FIFO_SIZE				RESERVED	VC3_FIFO_ADD			VC2_FIFO_SIZE				RESERVED	VC2_FIFO_ADD			VC1_FIFO_SIZE				RESERVED	VC1_FIFO_ADD			VC0_FIFO_SIZE				RESERVED	VC0_FIFO_ADD		

Bits	Field Name	Description	Type	Reset
31:28	VC3_FIFO_SIZE	Size of the FIFO allocated for virtual channel 3. For a complete description, refer to Table 10-477, *Virtual Channel RX FIFO Size Values.*	RW	0x0
27	RESERVED		R	0
26:24	VC3_FIFO_ADD	Address of the space allocated in the FIFO for virtual channel 3. For a complete description, refer to Table 10-478, *Virtual Channel RX FIFO Start Address.*	RW	0x0
23:20	VC2_FIFO_SIZE	Size of the FIFO allocated for virtual channel 2. For a complete description, refer to Table 10-477, *Virtual Channel RX FIFO Size Values.*	RW	0x0
19	RESERVED		R	0
18:16	VC2_FIFO_ADD	Address of the space allocated in the FIFO for virtual channel 2. For a complete description, refer to Table 10-478, *Virtual Channel RX FIFO Start Address.*	RW	0x0
15:12	VC1_FIFO_SIZE	Size of the FIFO allocated for virtual channel 1. For a complete description, refer to Table 10-477, *Virtual Channel RX FIFO Size Values.*	RW	0x0
11	RESERVED		R	0
10:8	VC1_FIFO_ADD	Address of the space allocated in the FIFO for virtual channel 1. For a complete description, refer to Table 10-478, *Virtual Channel RX FIFO Start Address.*	RW	0x0

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Bits	Field Name	Description	Type	Reset
7:4	VC0_FIFO_SIZE	Size of the FIFO allocated for virtual channel 0. For a complete description, refer to Table 10-477, *Virtual Channel RX FIFO Size Values.*	RW	0x0
3	RESERVED		R	0
2:0	VC0_FIFO_ADD	Address of the space allocated in the FIFO for virtual channel 0. For a complete description, refer to Table 10-478, *Virtual Channel RX FIFO Start Address.*	RW	0x0

Table 10-557. Register Call Summary for Register DSI_RX_FIFO_VC_SIZE

MIPI Display Serial Interface

- DSI Transfer Modes: [0] [1] [2]
- DSI Command Mode Using the DISPC Video Port: [3]
- DSI_PROTOCOL_ENGINE Register Summary: [4] [5]

Table 10-558. DSI_COMPLEXIO_CFG2

Address Offset	0x0000 0078		
Physical Address	0x5800 4078 0x4804 4078 0x5800 5078 0x4804 5078	**Instance**	DSI1_PROTOCOL_ENGINE_L3 DSI1_PROTOCOL_ENGINE_PER_L4 DSI2_PROTOCOL_ENGINE_L3 DSI2_PROTOCOL_ENGINE_PER_L4
Description	COMPLEXIO CONFIGURATION REGISTER for the complex I/O This register contains the lane configuration for the ULPS for each lane.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														LP_BUSY	HS_BUSY	RESERVED						LANE5_ULPS_SIG2	LANE4_ULPS_SIG2	LANE3_ULPS_SIG2	LANE2_ULPS_SIG2	LANE1_ULPS_SIG2	LANE5_ULPS_SIG1	LANE4_ULPS_SIG1	LANE3_ULPS_SIG1	LANE2_ULPS_SIG1	LANE1_ULPS_SIG1

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17	LP_BUSY	Indicates when there are still pending operations for VCs configured for LP mode. Forced to 1 when at least one VC is enabled and configured for LP mode. Read 0x0: LP logic is idle Read 0x1: LP logic is active	R	0
16	HS_BUSY	Indicates when there are still pending operations for VCs configured for HS mode. Forced to 1 when at least one VC is enabled and configured for HS mode. Read 0x0: HS logic is idle Read 0x1: HS logic is active	R	0
15:10	RESERVED		R	0x00

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Bits	Field Name	Description	Type	Reset
9	LANE5_ULPS_SIG2	Applicable only to DS1. For DSI2 this bit field is RESERVED. Enables the ULPS for the lane 5. The hardware shall change the state of the lane to ULPS only when it is in stop state and there is no data pending inside the DSI protocol engine and the DSI protocol engine has control of the bus (BTA has not been sent). The state of the signal TxRequestEsc is changed if lane 5 is a data lane. The state of the signal TxUlpsClk is changed if lane 5 is a clock lane. There will be a latency depending on the frequency of TxClkExc. This bit should be read back to confirm a write has been effective. 0x0: READ:Inactive state effective. WRITE: Request to change to inactive state 0x1: READ:Active state effective. WRITE: Change request to active. If the lane is a data lane, TxRequestEsc is asserted and synchronously TxUlpsEsc is asserted for one period of TxClkEsc.	RW	0
8	LANE4_ULPS_SIG2	Applicable only to DS1. For DSI2 this bit field is RESERVED. Enables the ULPS for the lane 4. The hardware shall change the state of the lane to ULPS only when it is in stop state and there is no data pending inside the DSI protocol engine and the DSI protocol engine has control of the bus (BTA has not been sent). The state of the signal TxRequestEsc is changed if lane 4 is a data lane. The state of the signal TxUlpsClk is changed if lane 4 is a clock lane. There will be a latency depending on the frequency of TxClkExc. This bit should be read back to confirm a write has been effective. 0x0: READ: Inactive state effective. WRITE: Request to change to inactive state 0x1: READ:Active state effective. WRITE: Change request to active. If the lane is a data lane, TxRequestEsc is asserted and synchronously TxUlpsEsc is asserted for one period of TxClkEsc.	RW	0
7	LANE3_ULPS_SIG2	Enables the ULPS for the lane 3. The hardware shall change the state of the lane to ULPS only when it is in stop state and there is no data pending inside the DSI protocol engine and the DSI protocol engine has control of the bus (BTA has not been sent). The state of the signal TxRequestEsc is changed if lane 3 is a data lane. The state of the signal TxUlpsClk is changed if lane 3 is a clock lane. There will be a latency depending on the frequency of TxClkExc. This bit should be read back to confirm a write has been effective. 0x0: READ: Inactive state effective. WRITE: Request to change to inactive state 0x1: READ:Active state effective. WRITE: Change request to active. If the lane is a data lane, TxRequestEsc is asserted and synchronously TxUlpsEsc is asserted for one period of TxClkEsc.	RW	0

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Bits	Field Name	Description	Type	Reset
6	LANE2_ULPS_SIG2	Enables the ULPS for the lane 2. The hardware shall change the state of the lane to ULPS only when it is in stop state and there is no data pending inside the DSI protocol engine and the DSI protocol engine has control of the bus (BTA has not been sent). The state of the signal TxRequestEsc is changed if lane 2 is a data lane. The state of the signal TxUlpsClk is changed if lane 2 is a clock lane. There will be a latency depending on the frequency of TxClkExc. This bit should be read back to confirm a write has been effective. 0x0: READ: Inactive state effective. WRITE: Request to change to inactive state 0x1: READ:Active state effective. WRITE: Change request to active. If the lane is a data lane, TxRequestEsc is asserted and synchronously TxUlpsEsc is asserted for one period of TxClkEsc.	RW	0
5	LANE1_ULPS_SIG2	Enables the ULPS for the lane 1. The hardware shall change the state of the lane to ULPS only when it is in stop state and there is no data pending inside the DSI protocol engine and the DSI protocol engine has control of the bus (BTA has not been sent). The state of the signal TxRequestEsc is changed if lane 1 is a data lane. The state of the signal TxUlpsClk is changed if lane 1 is a clock lane. There will be a latency depending on the frequency of TxClkExc. This bit should be read back to confirm a write has been effective. 0x0: READ: Inactive state effective. WRITE: Request to change to inactive state 0x1: READ:Active state effective. WRITE: Change request to active. If the lane is a data lane, TxRequestEsc is asserted and synchronously TxUlpsEsc is asserted for one period of TxClkEsc.	RW	0
4	LANE5_ULPS_SIG1	Applicable only to DS1. For DSI2 this bit field is RESERVED. Enables the ULPS for the lane 5. The hardware shall change the state of the lane to ULPS only when it is in stop state and there is no data pending inside the DSI protocol engine and the DSI protocol engine has control of the bus (BTA has not been sent). The state of the signal TxULPSExit is changed if the lane 5 is a clock lane. There will be a latency depending on the frequency of TxClkExc. This bit should be read back to confirm a write has been effective. 0x0: READ:Inactive state effective. WRITE: Request to change to inactive state 0x1: READ:Active state effective. WRITE: Change request to active. If the lane is a data lane, TxRequestEsc is asserted and synchronously TxUlpsEsc is asserted for one period of TxClkEsc	RW	0

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Bits	Field Name	Description	Type	Reset
3	LANE4_ULPS_SIG1	Applicable only to DS1. For DSI2 this bit field is RESERVED. Enables the ULPS for the lane 4. The hardware shall change the state of the lane to ULPS only when it is in stop state and there is no data pending inside the DSI protocol engine and the DSI protocol engine has control of the bus (BTA has not been sent). The state of the signal TxULPSExit is changed if the lane 4 is a clock lane. There will be a latency depending on the frequency of TxClkExc. This bit should be read back to confirm a write has been effective. 0x0: READ: Inactive state effective. WRITE: Request to change to inactive state 0x1: READ:Active state effective. WRITE: Change request to active. If the lane is a data lane, TxRequestEsc is asserted and synchronously TxUlpsEsc is asserted for one period of TxClkEsc	RW	0
2	LANE3_ULPS_SIG1	Enables the ULPS for the lane 3. The hardware shall change the state of the lane to ULPS only when it is in stop state and there is no data pending inside the DSI protocol engine and the DSI protocol engine has control of the bus (BTA has not been sent). The state of the signal TxULPSExit is changed if the lane 3 is a clock lane. There will be a latency depending on the frequency of TxClkExc. This bit should be read back to confirm a write has been effective. 0x0: READ: Inactive state effective. WRITE: Request to change to inactive state 0x1: READ:Active state effective. WRITE: Change request to active. If the lane is a data lane, TxRequestEsc is asserted and synchronously TxUlpsEsc is asserted for one period of TxClkEsc	RW	0
1	LANE2_ULPS_SIG1	Enables the ULPS for the lane 2. The hardware shall change the state of the lane to ULPS only when it is in stop state and there is no data pending inside the DSI protocol engine and the DSI protocol engine has control of the bus (BTA has not been sent). The state of the signal TxULPSExit is changed if the lane 2 is a clock lane. There will be a latency depending on the frequency of TxClkExc. This bit should be read back to confirm a write has been effective. 0x0: READ: Inactive state effective. WRITE: Request to change to inactive state 0x1: READ:Active state effective. WRITE: Change request to active. If the lane is a data lane, TxRequestEsc is asserted and synchronously TxUlpsEsc is asserted for one period of TxClkEsc	RW	0
0	LANE1_ULPS_SIG1	Enables the ULPS for the lane 1. The hardware shall change the state of the lane to ULPS only when it is in stop state and there is no data pending inside the DSI protocol engine and the DSI protocol engine has control of the bus (BTA has not been sent). The state of the signal TxULPSExit is changed if the lane 1 is a clock lane. There will be a latency depending on the frequency of TxClkExc. This bit should be read back to confirm a write has been effective. 0x0: READ:Inactive state effective. WRITE: Request to change to inactive state 0x1: READ:Active state effective WRITE: Change request to active. If the lane is a data lane, TxRequestEsc is asserted and synchronously TxUlpsEsc is asserted for one period of TxClkEsc	RW	0

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Table 10-559. Register Call Summary for Register DSI_COMPLEXIO_CFG2

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- Ultralow-Power State Configuration: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23] [24]
- DSI_PROTOCOL_ENGINE Register Summary: [25] [26]

Table 10-560. DSI_RX_FIFO_VC_FULLNESS

Address Offset	0x0000 007C		
Physical Address	0x5800 407C 0x4804 407C 0x5800 507C 0x4804 507C	**Instance**	DSI1_PROTOCOL_ENGINE_L3 DSI1_PROTOCOL_ENGINE_PER_L4 DSI2_PROTOCOL_ENGINE_L3 DSI2_PROTOCOL_ENGINE_PER_L4
Description	Defines the fullness of each space allocated for each virtual channel.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VC3_FIFO_FULLNESS								VC2_FIFO_FULLNESS								VC1_FIFO_FULLNESS								VC0_FIFO_FULLNESS							

Bits	Field Name	Description	Type	Reset
31:24	VC3_FIFO_FULLNESS	Fullness of the FIFO allocated for virtual channel 3.The valid values are from 0 to DSI_GNQ[5:3] RX_FIFODEPTH-1 corresponding to 1x33-bit,...up to DSI_GNQ[5:3] RX_FIFODEPTH x33-bit.	R	0x00
23:16	VC2_FIFO_FULLNESS	Fullness of the FIFO allocated for virtual channel 2.The valid values are from 0 to DSI_GNQ[5:3] RX_FIFODEPTH-1 corresponding to 1x33-bit,...up to DSI_GNQ[5:3] RX_FIFODEPTH x33-bit.	R	0x00
15:8	VC1_FIFO_FULLNESS	Fullness of the FIFO allocated for virtual channel 1.The valid values are from 0 to DSI_GNQ[5:3] RX_FIFODEPTH-1 corresponding to 1x33-bit,...up to DSI_GNQ[5:3] RX_FIFODEPTH x33-bit.	R	0x00
7:0	VC0_FIFO_FULLNESS	Fullness of the FIFO allocated for virtual channel 0.The valid values are from 0 to DSI_GNQ[5:3] RX_FIFODEPTH-1 corresponding to 1x33-bit,...up to DSI_GNQ[5:3] RX_FIFODEPTH x33-bit.	R	0x00

Table 10-561. Register Call Summary for Register DSI_RX_FIFO_VC_FULLNESS

MIPI Display Serial Interface

- DSI Transfer Modes: [0]
- DSI_PROTOCOL_ENGINE Register Summary: [1] [2]

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Table 10-562. DSI_VM_TIMING4

Address Offset	0x0000 0080		
Physical Address	0x5800 4080 0x4804 4080 0x5800 5080 0x4804 5080	**Instance**	DSI1_PROTOCOL_ENGINE_L3 DSI1_PROTOCOL_ENGINE_PER_L4 DSI2_PROTOCOL_ENGINE_L3 DSI2_PROTOCOL_ENGINE_PER_L4
Description	VIDEO MODE TIMING REGISTER This register defines the video mode timing.		
Type	RW		

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
RESERVED	HSA_HS_INTERLEAVING	HFP_HS_INTERLEAVING	HBP_HS_INTERLEAVING

Bits	Field Name	Description	Type	Reset
31:24	RESERVED		R	0x00
23:16	HSA_HS_INTERLEAVING	Defines the number of TXBYTECLKHS clock cycles that can be used for interleaving High Speed command mode packet into Video Mode stream during HSA blanking period. The supported values are from 0 to 255.	RW	0x00
15:8	HFP_HS_INTERLEAVING	Defines the number of TXBYTECLKHS clock cycles that can be used for interleaving High Speed command mode packet into Video Mode stream during HFP blanking period. The supported values are from 0 to 255	RW	0x00
7:0	HBP_HS_INTERLEAVING	Defines the number of TXBYTECLKHS clock cycles that can be used for interleaving High Speed command mode packet into Video Mode stream during HBP blanking period. The supported values are from 0 to 255	RW	0x00

Table 10-563. Register Call Summary for Register DSI_VM_TIMING4

MIPI Display Serial Interface

- DSI Transfer Modes: [0] [1] [2]
- DSI_PROTOCOL_ENGINE Register Summary: [3] [4]

Table 10-564. DSI_TX_FIFO_VC_EMPTINESS

Address Offset	0x0000 0084		
Physical Address	0x5800 4084 0x4804 4084 0x5800 5084 0x4804 5084	**Instance**	DSI1_PROTOCOL_ENGINE_L3 DSI1_PROTOCOL_ENGINE_PER_L4 DSI2_PROTOCOL_ENGINE_L3 DSI2_PROTOCOL_ENGINE_PER_L4
Description	Defines the emptiness of each space allocated for each virtual channel.		
Type	R		

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
VC3_FIFO_EMPTINESS	VC2_FIFO_EMPTINESS	VC1_FIFO_EMPTINESS	VC0_FIFO_EMPTINESS

Bits	Field Name	Description	Type	Reset
31:24	VC3_FIFO_EMPTINESS	Emptiness of the FIFO allocated for virtual channel 3.The valid values are from 0 to DSI_GNQ[2:0] TX_FIFODEPTH-1 corresponding to 1x33-bit,...up to DSI_GNQ[2:0] TX_FIFODEPTH x33-bit.	R	0x00

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Bits	Field Name	Description	Type	Reset
23:16	VC2_FIFO_EMPTINESS	Emptiness of the FIFO allocated for virtual channel 2.The valid values are from 0 to DSI_GNQ[2:0] TX_FIFODEPTH-1 corresponding to 1x33-bit,...up to DSI_GNQ[2:0] TX_FIFODEPTH x33-bit.	R	0x00
15:8	VC1_FIFO_EMPTINESS	Emptiness of the FIFO allocated for virtual channel 1.The valid values are from 0 to DSI_GNQ[2:0] TX_FIFODEPTH-1 corresponding to 1x33-bit,...up to DSI_GNQ[2:0] TX_FIFODEPTH x33-bit.	R	0x00
7:0	VC0_FIFO_EMPTINESS	Emptiness of the FIFO allocated for virtual channel 0.The valid values are from 0 to DSI_GNQ[2:0] TX_FIFODEPTH-1 corresponding to 1x33-bit,...up to DSI_GNQ[2:0] TX_FIFODEPTH x33-bit.	R	0x00

Table 10-565. Register Call Summary for Register DSI_TX_FIFO_VC_EMPTINESS

MIPI Display Serial Interface

- DSI Transfer Modes: [0] [1]
- DSI_PROTOCOL_ENGINE Register Summary: [2] [3]

Table 10-566. DSI_VM_TIMING5

Address Offset	0x0000 0088		
Physical Address	0x5800 4088 0x4804 4088 0x5800 5088 0x4804 5088	**Instance**	DSI1_PROTOCOL_ENGINE_L3 DSI1_PROTOCOL_ENGINE_PER_L4 DSI2_PROTOCOL_ENGINE_L3 DSI2_PROTOCOL_ENGINE_PER_L4
Description	VIDEO MODE TIMING REGISTER This register defines the video mode timing.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								HSA_LP_INTERLEAVING								HFP_LP_INTERLEAVING								HBP_LP_INTERLEAVING							

Bits	Field Name	Description	Type	Reset
31:24	RESERVED		R	0x00
23:16	HSA_LP_INTERLEAVING	Defines the number of bytes of Low Power command mode packets that can be sent on PPI link during HSA blanking period. The supported values are from 0 to 255.	RW	0x00
15:8	HFP_LP_INTERLEAVING	Defines the number of bytes of Low Power command mode packets that can be sent on PPI link during HFP blanking period. The supported values are from 0 to 255	RW	0x00
7:0	HBP_LP_INTERLEAVING	Defines the number of bytes of Low Power command mode packets that can be sent on PPI link during HBP blanking period. The supported values are from 0 to 255	RW	0x00

Table 10-567. Register Call Summary for Register DSI_VM_TIMING5

MIPI Display Serial Interface

- DSI Transfer Modes: [0] [1] [2]
- DSI_PROTOCOL_ENGINE Register Summary: [3] [4]

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Table 10-568. DSI_VM_TIMING6

Address Offset	0x0000 008C		
Physical Address	0x5800 408C 0x4804 408C 0x5800 508C 0x4804 508C	**Instance**	DSI1_PROTOCOL_ENGINE_L3 DSI1_PROTOCOL_ENGINE_PER_L4 DSI2_PROTOCOL_ENGINE_L3 DSI2_PROTOCOL_ENGINE_PER_L4
Description	VIDEO MODE TIMING REGISTER This register defines the video mode timing.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BL_HS_INTERLEAVING																BL_LP_INTERLEAVING															

Bits	Field Name	Description	Type	Reset
31:16	BL_HS_INTERLEAVING	Defines the number of TXBYTECLKHS clock cycles that can be used for interleaving High Speed command mode packet into Video Mode stream during blanking periods during VSA, VBP, VFP periods inside one video frame on PPI link. The supported values are from 0 to 65535 .	RW	0x0000
15:0	BL_LP_INTERLEAVING	Defines the maximum number of bytes of Low Power command mode packets that can be sent on PPI link during blanking periods during VSA, VBP or VFP periods inside one video frame on PPI link. The supported values are from 0 to 65535	RW	0x0000

Table 10-569. Register Call Summary for Register DSI_VM_TIMING6

MIPI Display Serial Interface

- DSI Transfer Modes: [0] [1]
- Video Port Interface: [2]
- DSI_PROTOCOL_ENGINE Register Summary: [3] [4]

Table 10-570. DSI_VM_TIMING7

Address Offset	0x0000 0090		
Physical Address	0x5800 4090 0x4804 4090 0x5800 5090 0x4804 5090	**Instance**	DSI1_PROTOCOL_ENGINE_L3 DSI1_PROTOCOL_ENGINE_PER_L4 DSI2_PROTOCOL_ENGINE_L3 DSI2_PROTOCOL_ENGINE_PER_L4
Description	Defines the minimum number of HS bytes clock cycles that are required to allow for the delays in entering and exiting HS mode. The supported values are from 0 to 65535		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ENTER_HS_MODE_LATENCY																EXIT_HS_MODE_LATENCY															

Bits	Field Name	Description	Type	Reset
31:16	ENTER_HS_MODE_LATENCY	Defines the number of TXBYTECLKHS clock cycles necessary for entering to HS mode. It corresponds to the delay in number of HS clock cycles from assertion of TxRequestHS signal to 1 until assertion of TxReadyHS signal to 1. The supported values are from 0 to 65535 .	RW	0x0000

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Bits	Field Name	Description	Type	Reset
15:0	EXIT_HS_MODE_LATENCY	Defines the number of TXBYTECLKHS clock cycles necessary for exiting from HS mode. It corresponds to the maximum delay in number of TXBYTECLKHS clock from de-assertion of TxRequestHS signal until PPI link is in LP-11 state from which a new entrance to HS mode can be initiated which does not take more than ENTER_HS_MODE_LATENCY clock cycles. The supported values are from 0 to 65535	RW	0x0000

Table 10-571. Register Call Summary for Register DSI_VM_TIMING7

MIPI Display Serial Interface

- Clock Requirements: [0] [1] [2] [3]
- DSI Video Mode Using the DISPC Video Port: [4] [5]
- DSI_PROTOCOL_ENGINE Register Summary: [6] [7]

Table 10-572. DSI_STOPCLK_TIMING

Address Offset	0x0000 0094		
Physical Address	0x5800 4094 0x4804 4094 0x5800 5094 0x4804 5094	**Instance**	DSI1_PROTOCOL_ENGINE_L3 DSI1_PROTOCOL_ENGINE_PER_L4 DSI2_PROTOCOL_ENGINE_L3 DSI2_PROTOCOL_ENGINE_PER_L4
Description	Number of functional clock cycles to wait for TXBYTECLKHS to stop/start after change in DSIStopClk signal		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								DSI_STOPCLK_LATENCY							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED		R	0x000000
7:0	DSI_STOPCLK_LATENCY	Clock gating latency from DSI Protocol to TXBYTECLKHS	RW	0x80

Table 10-573. Register Call Summary for Register DSI_STOPCLK_TIMING

MIPI Display Serial Interface

- Power Control of DSI PHY Complex I/O and DSI PLL: [0] [1]
- DSI_PROTOCOL_ENGINE Register Summary: [2] [3]

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Table 10-574. DSI_CTRL2

Address Offset	0x0000 0098		
Physical Address	0x5800 4098 0x4804 4098 0x5800 5098 0x4804 5098	**Instance**	DSI1_PROTOCOL_ENGINE_L3 DSI1_PROTOCOL_ENGINE_PER_L4 DSI2_PROTOCOL_ENGINE_L3 DSI2_PROTOCOL_ENGINE_PER_L4
Description	Additional control bits for use with Video Port 2		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																		LINE_BUFFER		VP_VSYNC_POL		VP_HSYNC_POL		VP_DE_POL		VP_CLK_POL		VP_DATA_BUS_WIDTH		RESERVED		VP_CLK_RATIO		RESERVED			

Bits	Field Name	Description	Type	Reset
31:14	RESERVED		R	0x00000
13:12	LINE_BUFFER	Number of line buffers to be used while receiving data on the video port. The valid values are from 0 to DSI_GNQ[23:22] VP2_NB_LINE_BUFFER. 0x0: No line buffer 0x1: 1 line buffer 0x2: 2 line buffers	RW	0x0
11	VP_VSYNC_POL	VP vertical synchronization signal polarity 0x0: VSYNC signal on the video port is active low. 0x1: VSYNC signal on the video port is active high.	RW	0
10	VP_HSYNC_POL	VP horizontal synchronization signal polarity 0x0: HSYNC signal on the video port is active low. 0x1: HSYNC signal on the video port is active high.	RW	0
9	VP_DE_POL	VP data enable signal polarity 0x0: DE signal on the video port is active low. 0x1: DE signal on the video port is active high.	RW	0
8	VP_CLK_POL	VP pixel clock polarity 0x0: The DSI Protocol Engine module captures the data on the VP on the pixel clock falling edge. The module connected to the VP shall drive the data on the pixel clock rising edge. 0x1: The DSI Protocol Engine module captures the data on the VP on the pixel clock raising edge. The module connected to the VP shall drive the data on the pixel clock falling edge.	RW	1
7:6	VP_DATA_BUS_WIDTH	Defines the size of the video port data bus 0x0: 16-bits data width (LSB of the 24-bit video port data bus) 0x1: 18-bits data width (LSB of the 24-bit video port data bus) 0x2: 24-bits data width (LSB of the 24-bit video port data bus)	RW	0x0
5	RESERVED		R	0

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Bits	Field Name	Description	Type	Reset
4	VP_CLK_RATIO	The field indicates the clock ratio between VP_CLK and VP_PCLK. The clock VP_PCLK is generated from VP_CLK. It is divided down. The information is only used when the video port is used to provide data in command mode. In the case of video mode, it is not used. 0x0: The clock VP_PCLK is the clock VP_CLK divided by 2. The duty cycle of VP_PCLK is 50/50. 0x1: The clock VP_PCLK is the clock VP_CLK divided by 3 or more. The duty cycle of VP_PCLK is not 50/50 for odd ratio numbers (3,5,7,...).	RW	0
3:0	RESERVED		R	0x0

Table 10-575. Register Call Summary for Register DSI_CTRL2

MIPI Display Serial Interface
- Video Port Interface: [0] [1] [2] [3] [4]
- DSI_PROTOCOL_ENGINE Register Summary: [5] [6]
- DSI_PROTOCOL_ENGINE Register Description: [7] [8] [9] [10]

Table 10-576. DSI_VM_TIMING8

Address Offset	0x0000 009C		
Physical Address	0x5800 409C 0x4804 409C 0x5800 509C 0x4804 509C	**Instance**	DSI1_PROTOCOL_ENGINE_L3 DSI1_PROTOCOL_ENGINE_PER_L4 DSI2_PROTOCOL_ENGINE_L3 DSI2_PROTOCOL_ENGINE_PER_L4
Description	VIDEO MODE TIMING REGISTER This register defines the video mode timing.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														HFPX	

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1:0	HFPX	Extension to the HFP register. Additional bits added to MSB.	RW	0x0

Table 10-577. Register Call Summary for Register DSI_VM_TIMING8

MIPI Display Serial Interface
- Blanking: [0]
- DSI Transfer Modes: [1]
- DSI_PROTOCOL_ENGINE Register Summary: [2] [3]

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Table 10-578. DSI_TE_HSYNC_WIDTH_j

Address Offset	0x0000 00A0 + (0xc * j)	**Index**	j = 0 to 1
Physical Address	0x5800 40A0 + (0xc * j) 0x4804 40A0 + (0xc * j) 0x5800 50A0 + (0xc * j) 0x4804 50A0 + (0xc * j)	**Instance**	DSI1_PROTOCOL_ENGINE_L3 DSI1_PROTOCOL_ENGINE_PER_L4 DSI2_PROTOCOL_ENGINE_L3 DSI2_PROTOCOL_ENGINE_PER_L4
Description	The register configures the TE HSYNC minimum pulse width for TE0 and TE1 CMOS signals The input TE signal is asynchronous and needs to be resynchronizred to DSI_CLK clock domain.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								MIN_HSYNC_PULSE_WIDTH																RESERVED							

Bits	Field Name	Description	Type	Reset
31:20	RESERVED		R	0x000
19:8	MIN_HSYNC_PULSE_WIDTH	Programmable min HSYNC pulse width Minimum HSYNC pulse width. Number of DSI_CLK clock cycles times 256 to determine when HSYNC pulse occurs. The value 0 is invalid.	RW	0x001
7:0	RESERVED		R	0x00

Table 10-579. Register Call Summary for Register DSI_TE_HSYNC_WIDTH_j

MIPI Display Serial Interface

- PHY Triggers: [0] [1] [2] [3] [4]
- DSI_PROTOCOL_ENGINE Register Summary: [5] [6]

Table 10-580. DSI_TE_VSYNC_WIDTH_j

Address Offset	0x0000 00A4 + (0xc * j)	**Index**	j = 0 to 1
Physical Address	0x5800 40A4 + (0xc * j) 0x4804 40A4 + (0xc * j) 0x5800 50A4 + (0xc * j) 0x4804 50A4 + (0xc * j)	**Instance**	DSI1_PROTOCOL_ENGINE_L3 DSI1_PROTOCOL_ENGINE_PER_L4 DSI2_PROTOCOL_ENGINE_L3 DSI2_PROTOCOL_ENGINE_PER_L4
Description	The register configures the TE VSYNC minimum pulse width for TE0 and TE1 CMOS signals The input TE signal is asynchronous and needs to be resynchronizred to DSI_CLK clock domain.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								MIN_VSYNC_PULSE_WIDTH																RESERVED							

Bits	Field Name	Description	Type	Reset
31:20	RESERVED		R	0x000
19:8	MIN_VSYNC_PULSE_WIDTH	Programmable min VSYNC pulse width Minimum VSYNC pulse width. Number of DSI_CLK cycles times 256 to determine when VSYNC pulse occurs. The value 0 is invalid. The value shall be greater than MIN_HSYNC_PULSE_WIDTH when DSI_TE_HSYNC_NUMBER is greather than 0	RW	0x001
7:0	RESERVED		R	0x00

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Table 10-581. Register Call Summary for Register DSI_TE_VSYNC_WIDTH_j

MIPI Display Serial Interface
- PHY Triggers: [0] [1] [2] [3] [4] [5]
- DSI_PROTOCOL_ENGINE Register Summary: [6] [7]

Table 10-582. DSI_TE_HSYNC_NUMBER_j

Address Offset	0x0000 00A8 + (0xc * j)	**Index**	j = 0 to 1
Physical Address	0x5800 40A8 + (0xc * j) 0x4804 40A8 + (0xc * j) 0x5800 50A8 + (0xc * j) 0x4804 50A8 + (0xc * j)	**Instance**	DSI1_PROTOCOL_ENGINE_L3 DSI1_PROTOCOL_ENGINE_PER_L4 DSI2_PROTOCOL_ENGINE_L3 DSI2_PROTOCOL_ENGINE_PER_L4
Description	The register configures the number of HSYNC to synchronize the beginning of the transfer on DSI link based on the number of HSYNC pulse received on the TE line. The input TE signal is asynchronous and needs to be resynchronizred to DSI_CLK clock domain.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								LINE_NUMBER							

Bits	Field Name	Description	Type	Reset
31:11	RESERVED		R	0x000000
10:0	LINE_NUMBER	Programmable line number Line number from 0 to 2047. Number of HSYNC after the VSYNC occurs before the beginning of the transfer. Any HSYNC before VSYNC is ignored.	RW	0x000

Table 10-583. Register Call Summary for Register DSI_TE_HSYNC_NUMBER_j

MIPI Display Serial Interface
- PHY Triggers: [0] [1] [2]
- DSI_PROTOCOL_ENGINE Register Summary: [3] [4]

Table 10-584. DSI_VC_CTRL_i

Address Offset	0x0000 0100 + (0x20 * i)	**Index**	i = 0 to 3
Physical Address	0x5800 4100 + (0x20 * i) 0x4804 4100 + (0x20 * i) 0x5800 5100 + (0x20 * i) 0x4804 5100 + (0x20 * i)	**Instance**	DSI1_PROTOCOL_ENGINE_L3 DSI1_PROTOCOL_ENGINE_PER_L4 DSI2_PROTOCOL_ENGINE_L3 DSI2_PROTOCOL_ENGINE_PER_L4
Description	CONTROL REGISTER - Virtual channel This register controls the virtual channel.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DCS_CMD_CODE	DCS_CMD_ENABLE	DMA_RX_REQ_NB			DMA_RX_THRESHOLD			DMA_TX_REQ_NB			RX_FIFO_NOT_EMPTY	DMA_TX_THRESHOLD			TX_FIFO_FULL	VC_BUSY	PP_BUSY	VP_SOURCE	RGB565_ORDER	OCP_DATA_BUS_WIDTH		MODE_SPEED	ECC_TX_EN	CS_TX_EN	BTA_EN	TX_FIFO_NOT_EMPTY	MODE	BTA_LONG_EN	BTA_SHORT_EN	SOURCE	VC_EN

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Bits	Field Name	Description	Type	Reset
31	DCS_CMD_CODE	DCS command code value to insert between header and video port or Interface slave data when enabled by DCS_CMD_ENABLE (only when TE mechanism is not used otherwise the bit field DCS_CMD_CODE is ignored by DSI protocol engine). 0x0: DCS write memory continue code is inserted. 0x1: DCS write memory start code is inserted.	RW	0
30	DCS_CMD_ENABLE	Enables automatic insertion of DCS command codes when data is sourced by the video port. 0x0: DCS command code is NOT inserted when command mode traffic is coming from the Video Port or Interface slave port. 0x1: DCS command code is inserted automatically when command mode traffic is coming from the Video Port or Interface slave port.	RW	0
29:27	DMA_RX_REQ_NB	Selection of the use of the DMA request (associated to the RX FIFO) 0x0: DMA_req0 is selected (valid only if DSI_GNQ[8:6] NB_DMA_REQUEST is greater than 0) 0x1: DMA_req1 is selected (valid only if DSI_GNQ[8:6] NB_DMA_REQUEST is greater than 1) 0x2: DMA_req2 is selected (valid only if DSI_GNQ[8:6] NB_DMA_REQUEST is greater than 2) 0x3: DMA_req3 is selected (valid only if DSI_GNQ[8:6] NB_DMA_REQUEST is equal to 3) 0x4: No DMA req selected	RW	0x0
26:24	DMA_RX_THRESHOLD	Defines the threshold value for the DMA request (associated to the RX FIFO) 0x0: 1x 32 bits 0x1: 2 x 32 bits 0x2: 4 x 32 bits 0x3: 8 x 32 bits 0x4: 16 x 32 bits 0x5: 32 x 32 bits	RW	0x0
23:21	DMA_TX_REQ_NB	Selection of the use of the DMA request (associated to the TX FIFO) 0x0: DMA_req0 is selected (valid only if DSI_GNQ[8:6] NB_DMA_REQUEST is greater than 0) 0x1: DMA_req1 is selected (valid only if DSI_GNQ[8:6] NB_DMA_REQUEST is greater than 1) 0x2: DMA_req2 is selected (valid only if DSI_GNQ[8:6] NB_DMA_REQUEST is greater than 2) 0x3: DMA_req3 is selected (valid only if DSI_GNQ[8:6] NB_DMA_REQUEST is equal to 3) 0x4: No DMA req selected	RW	0x0
20	RX_FIFO_NOT_EMPTY	FIFO status in command mode. Otherwise, this bit can be ignored. Read 0x0: The RX FIFO is empty (the FIFO does not contain any data for the virtual channel) Read 0x1: The RX FIFO is not empty (the FIFO contains at least one byte for the virtual channel)	R	0

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Bits	Field Name	Description	Type	Reset
19:17	DMA_TX_THRESHOLD	Defines the threshold value for the DMA request (associated to the TX FIFO) 0x0: 1x 32 bits 0x1: 2 x 32 bits 0x2: 4 x 32 bits 0x3: 8 x 32 bits 0x4: 16 x 32 bits 0x5: 32 x 32 bits	RW	0x0
16	TX_FIFO_FULL	FIFO status in command mode. Otherwise, this bit can be ignored. Read 0x0: The TX FIFO is not full (the FIFO can accept at least one more 32-bit valuel) Read 0x1: The TX FIFO is full	R	0
15	VC_BUSY	Indicates if previously scheduled activities (packets, BTA) are still being processed. Forced to 1 if VC is enabled. Software should check this bit is 0 before changing channel configuration. Read 0x0: No pending operations for this VC Read 0x1: Pending operations for this VC	R	0
14	PP_BUSY	Ping-pong buffer busy status. Read 0x0: Software is permitted to write a new header for VP command mode traffic. Read 0x1: Software is NOT permitted to write a new header for VP command mode traffic.	R	0
13	VP_SOURCE	Selection between video port 1 and video port 2. If DSI_GNQ[24] NB_VIDEO_PORTS = 0, the bit field is ignored since only video port 1 is present. 0x0: The video port 1 is selected. 0x1: The video port 2 is selected. Note: This selection applies only to DSI1. For DSI2 to work properly, the VP_SOURCE bit must always be set to 0x0.	RW	0
12	RGB565_ORDER	Byte order for RBG565 0x0: Byte order as for DBI compliance 0x1: Byte order as for video mode	RW	0
11:10	OCP_DATA_BUS_WIDTH	Defines the size of the Interface data bus 0x0: 16-bits data width (LSB of the 32-bit Interface port data bus) 0x1: 24-bits data width (LSB of the 32-bit Interface port data bus) 0x2: 2x16-bits data width (first pixel on the LSB of the 32-bit Interface port data bus and second pixel on the MSB of the 32-bit Interface port data bus for the same Interface access) 0x3: 32-bits data width	RW	0x0
9	MODE_SPEED	Selection of the mode. The information is used by hardware only if MODE=COMMAND_MODE otherwise it is ignored. 0x0: Low-power mode (CMOS) is used to send short and long packets to the peripheral. 0x1: High Speed mode (SLVS) is used to send short and long packets to the peripheral.	RW	0

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Bits	Field Name	Description	Type	Reset
8	ECC_TX_EN	Enables the Error Correction Code generation for the transmit header (short and long packets). 0x0: Disabled 0x1: Enabled	RW	0
7	CS_TX_EN	Enables the checksum generation for the transmit payload (long packet only). 0x0: Disabled. The value 0x00 is used. 0x1: Enabled. The checksum value is calculated by HW.	RW	0
6	BTA_EN	Send the bus turn around to the peripheral. It can be used when the automatic mode is enabled (BTA_SHORT_EN=1 or/and BTA_LONG_EN=1). In that case only one BTA is sent to the peripheral. The manual mode is used to allow the user to define for which packets, the turn around is required for example getting acknowledge from the peripheral. 0x0: READS: BTA generation is completed. It is reset by hardware when it is completed. WRITES: Cancellation of the BTA generation (not guarantee since it could already on going, shall not be used). 0x1: READS: BTA generation has been requested by user (it could be on going but not completed). WRITES: Request for BTA generation.	RW	0
5	TX_FIFO_NOT_EMPTY	FIFO status Read 0x0: The TX FIFO is empty (the FIFO does not contain any data for the virtual channel) Read 0x1: The TX FIFO is not empty (the FIFO contains at least one byte for the virtual channel)	R	0
4	MODE	Selection of the mode 0x0: Command mode. 0x1: Video mode. The bit fields MODE_SPEED and SOURCE are not used by hardware. The bit field VP_SOURCE is used to select between video port 1 and video port 2 when two video ports are present.	RW	0
3	BTA_LONG_EN	Enables the automatic bus turn-around after completion of each long packet transmission. 0x0: Disabled 0x1: Enabled	RW	0
2	BTA_SHORT_EN	Enables the automatic bus turn-around after completion of each short packet transmission. 0x0: Disabled 0x1: Enabled	RW	0

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Bits	Field Name	Description	Type	Reset
1	SOURCE	Selection of the source between Interface and the Video port(s) (used by the hardware only if MODE=COMMAND MODE (0x0) otherwise it is ignored). The number of available video ports is defined in DSI_GNQ[24] NB_VIDEO_PORTS bit. 0x0: All the data are provided by the slave port. Any transfer on the video port is ignored for this virtual channel. 0x1: If MODE=VIDEO_MODE. the data received on the video port 1 or video port 2, selected using VP_SOURCE (pixels and enabled synchronization events using DSI_CTRL[17] VP_HSYNC_START, DSI_CTRL[18] VP_HSYNC_END, DSI_CTRL[15] VP_VSYNC_START, DSI_CTRL[16] VP_VSYNC_END for video port 1 and DSI_CTRL2[] VP_HSYNC_START, DSI_CTRL2[] VP_HSYNC_END, DSI_CTRL2[] VP_VSYNC_START, DSI_CTRL2[] VP_VSYNC_END for video port 2) are sent on the virtual channel (only one virtual channel can be associated with the video port, it is the software responsibility to ensure that no more than one virtual channel is enabled with the video port as the main source for data). If MODE=COMMAND_MODE, the VP.STALL signal is used by the protocol engine to indicate when new data are required. The synchronization signals are not generated by the display controller. Regardless of the MODE, no data can be provided on the Interface slave port.	RW	0
0	VC_EN	Enables the virtual channel. 0x0: Disabled. The virtual channel shall be disabled for any register change in the DSI_VC_... registers to the corresponding VC ID (except for setting the DSI_VC_CTRL_i[6] BTA_EN, DSI_VC_TE_i[23:0] TE_SIZE and DSI_VC_TE_i[31] TE_START bit fields, and DSI_VC_LONG_,,, DSI_VC_SHORT_..., DSI_VC_IRQ... registers). 0x1: Enabled. No change is allowed to the virtual channel registers expect resetting the VC_EN.	RW	0

Table 10-585. Register Call Summary for Register DSI_VC_CTRL_i

MIPI Display Serial Interface

- Short Packet: [0]
- Long Packet: [1]
- Blanking: [2] [3] [4] [5]
- VCs: [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16]
- 16 bpp – RGB Color Format, Long Packet (Command Mode): [17]
- DSI Global Register Controls: [18]
- DSI Transfer Modes: [19] [20] [21] [22] [23] [24] [25] [26] [27] [28] [29] [30] [31] [32] [33] [34] [35] [36] [37] [38] [39] [40] [41] [42] [43]
- Video Port Interface: [44] [45] [46]
- Timers: [47] [48]
- Bus Turnaround: [49] [50] [51] [52] [53] [54] [55]
- PHY Triggers: [56] [57] [58]
- ECC Generation: [59] [60]
- Checksum Generation for Long Packet Payloads: [61]
- Power Control of DSI PHY Complex I/O and DSI PLL: [62] [63]
- DSI Video Mode Using the DISPC Video Port: [64] [65] [66] [67] [68] [69]
- DSI Command Mode Using the DISPC Video Port: [70] [71] [72] [73] [74] [75] [76] [77] [78] [79] [80] [81] [82]
- DSI_PROTOCOL_ENGINE Register Summary: [83] [84]
- DSI_PROTOCOL_ENGINE Register Description: [85] [86]

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Table 10-586. DSI_VC_TE_i

Address Offset	0x0000 0104 + (0x20 * i)	**Index**	i = 0 to 3
Physical Address	0x5800 4104 + (0x20 * i) 0x4804 4104 + (0x20 * i) 0x5800 5104 + (0x20 * i) 0x4804 5104 + (0x20 * i)	**Instance**	DSI1_PROTOCOL_ENGINE_L3 DSI1_PROTOCOL_ENGINE_PER_L4 DSI2_PROTOCOL_ENGINE_L3 DSI2_PROTOCOL_ENGINE_PER_L4
Description	CONTROL REGISTER - Virtual channel This register controls the tearing effect logic. It defines the size of the transfer when TE occurs and enables the automatic TE mode.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TE_START	TE_EN	TE_LINE	TE_LINE_NB	RESERVED				TE_SIZE																							

Bits	Field Name	Description	Type	Reset
31	TE_START	Manual control of the start of the transfer. The user can use the TE interrupt in order to know that the TE trigger has been received prior to set the TE_START bit field. It is not mandatory to use the TE interrupt. 0x0: Indicates the end of the transfer. The bit can be used by user to cancel the transfer if not already started. The FIFO shall be flushed by software to ensure there is no data remaining in it. 0x1: Starts the transfer of the data. The size is defined in TE_SIZE. The bit field is set until the transfer is completed. It is reset by hardware when the transfer is completed.	RW	0
30	TE_EN	Tearing Effect Control 0x0: Disables the automatic transfer. The user shall use the interruption in order to know when TE PHY trigger is received or when the TE is detected on the input CMOS signals. The hardware reset the bit field when the transfer is completed (TE_SIZE=0). 0x1: Enables the automatic transfer of the data using the TE PHY trigger or one of the TE input signals as a synchronization event. The bit field TE_LINE defines if the CMOS signal is used or if the PHY trigger is used.	RW	0
29	TE_LINE	0x0: Disabled the TE CMOS signalling for the automatic data transfer. The DSI PHY trigger is used for the automactic data transfer. 0x1: Enables the TE CMOS signalling for the automatic data transfer. The DSI PHY trigger is not used for the automactic data transfer.	RW	0
28	TE_LINE_NB	Selection between TE0 and TE1 CMOS signals. 0x0: TE0 CMOS input line is selected 0x1: TE1 CMOS input line is selected	RW	0
27:24	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
23:0	TE_SIZE	Defines the number of byte (payload data excluding the check -sum) to be sent. The write into the register DSI_VC_LONG_PACKET_HEADER_i shall be performed by the user before sending data from the register DSI_VC_LONG_PACKET_PAYLOAD_i. The register value is decremented for every byte sent of the DSI link. At the end of the transfer (TE_SIZE=0), the bit field TE_EN is reset by hardware. The DMA request will be asserted when the trigger is received in order to receive data in the TX FIFO. It should not be deasserted until all data (TE_SIZE) have been received in the FIFO.	RW	0x000000

Table 10-587. Register Call Summary for Register DSI_VC_TE_i

MIPI Display Serial Interface

- PHY Triggers: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20]
- DSI Command Mode Using the DISPC Video Port: [21] [22] [23]
- DSI_PROTOCOL_ENGINE Register Summary: [24] [25]
- DSI_PROTOCOL_ENGINE Register Description: [26] [27]

Table 10-588. DSI_VC_LONG_PACKET_HEADER_i

Address Offset	0x0000 0108 + (0x20 * i)	**Index**	i = 0 to 3
Physical Address	0x5800 4108 + (0x20 * i) 0x4804 4108 + (0x20 * i) 0x5800 5108 + (0x20 * i) 0x4804 5108 + (0x20 * i)	**Instance**	DSI1_PROTOCOL_ENGINE_L3 DSI1_PROTOCOL_ENGINE_PER_L4 DSI2_PROTOCOL_ENGINE_L3 DSI2_PROTOCOL_ENGINE_PER_L4
Description	LONG PACKET HEADER INFORMATION -Virtual channel This register sets the 32-bit DATA_ID + Word count + ECC (the virtual channel id can be different than VC). The ECC will be computed if ECC_TX_EN is set to 1. DATA_ID is located at bit[7:0] WC is located at bit[23:8] ECC is located at bit[31:24] (Least significant byte first and least significant bit first)		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HEADER																															

Bits	Field Name	Description	Type	Reset
31:0	HEADER	Packet header information: DATA ID + WORD COUNT +ECC	W	0x0000 0000

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Table 10-589. Register Call Summary for Register DSI_VC_LONG_PACKET_HEADER_i

MIPI Display Serial Interface

- Long Packet: [0] [1] [2] [3] [4] [5] [6]
- Data Identifier: [7]
- VCs: [8]
- DSI Global Register Controls: [9]
- DSI Transfer Modes: [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23] [24] [25]
- Video Port Interface: [26]
- Bus Turnaround: [27]
- PHY Triggers: [28] [29] [30]
- ECC Generation: [31]
- DSI Video Mode Using the DISPC Video Port: [32]
- DSI Command Mode Using the DISPC Video Port: [33]
- DSI_PROTOCOL_ENGINE Register Summary: [34] [35]
- DSI_PROTOCOL_ENGINE Register Description: [36]

Table 10-590. DSI_VC_LONG_PACKET_PAYLOAD_i

Address Offset	0x0000 010C + (0x20 * i)	**Index**	i = 0 to 3
Physical Address	0x5800 410C + (0x20 * i) 0x4804 410C + (0x20 * i) 0x5800 510C + (0x20 * i) 0x4804 510C + (0x20 * i)	**Instance**	DSI1_PROTOCOL_ENGINE_L3 DSI1_PROTOCOL_ENGINE_PER_L4 DSI2_PROTOCOL_ENGINE_L3 DSI2_PROTOCOL_ENGINE_PER_L4
Description	LONG PACKET PAYLOAD INFORMATION -Virtual channel This register sets the payload information (excluding checksum). The hardware shall capture the word count in the packet header (in DSI_VC_LONG_PACKET_HEADER) in order to determine the last valid data (the virtual channel id can be different than VC). Byte1 is bit[7:0] Byte2 is bit[15:8] Byte3 is bit[23:16] Byte4 is bit[31:24] Byten is sent before Byten+1 (Least significant byte first and least significant bit first)		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PAYLOAD																															

Bits	Field Name	Description	Type	Reset
31:0	PAYLOAD	Packet payload information (excluding checksum)	W	0x0000 0000

Table 10-591. Register Call Summary for Register DSI_VC_LONG_PACKET_PAYLOAD_i

MIPI Display Serial Interface

- Long Packet: [0] [1] [2]
- DSI Global Register Controls: [3]
- DSI Transfer Modes: [4] [5] [6] [7] [8] [9] [10] [11] [12] [13]
- Bus Turnaround: [14]
- PHY Triggers: [15] [16]
- DSI_PROTOCOL_ENGINE Register Summary: [17] [18]
- DSI_PROTOCOL_ENGINE Register Description: [19]

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Table 10-592. DSI_VC_SHORT_PACKET_HEADER_i

Address Offset	0x0000 0110 + (0x20 * i)	**Index**	i = 0 to 3
Physical Address	0x5800 4110 + (0x20 * i) 0x4804 4110 + (0x20 * i) 0x5800 5110 + (0x20 * i) 0x4804 5110 + (0x20 * i)	**Instance**	DSI1_PROTOCOL_ENGINE_L3 DSI1_PROTOCOL_ENGINE_PER_L4 DSI2_PROTOCOL_ENGINE_L3 DSI2_PROTOCOL_ENGINE_PER_L4
Description	SHORT PACKET HEADER INFORMATION -Virtual channel This register sets the 24-bit DATA_ID + Short Packet Data Field + ECC (the virtual channel id can be different than VC). The ECC will be computed if ECC_TX_EN is set to 1. DATA_ID is located at bit[7:0] Short Packet Data field is located at bit[23:8] ECC is located at bit[31:24] (Least significant byte first and least significant bit first)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HEADER																															

Bits	Field Name	Description	Type	Reset
31:0	HEADER	WRITES: Packet header information: DATA ID + DATA FIELD +ECC written into the TX FIFO READS: 32-bit values read from the RX FIFO	RW	0x0000 0000

Table 10-593. Register Call Summary for Register DSI_VC_SHORT_PACKET_HEADER_i

MIPI Display Serial Interface

- Short Packet: [0]
- Data Identifier: [1]
- VCs: [2]
- DSI Global Register Controls: [3]
- DSI Transfer Modes: [4] [5] [6] [7] [8] [9]
- PHY Triggers: [10]
- ECC Generation: [11]
- DSI Command Mode Using the DISPC Video Port: [12]
- DSI_PROTOCOL_ENGINE Register Summary: [13] [14]

Table 10-594. DSI_VC_IRQSTATUS_i

Address Offset	0x0000 0118 + (0x20 * i)	**Index**	i = 0 to 3
Physical Address	0x5800 4118 + (0x20 * i) 0x4804 4118 + (0x20 * i) 0x5800 5118 + (0x20 * i) 0x4804 5118 + (0x20 * i)	**Instance**	DSI1_PROTOCOL_ENGINE_L3 DSI1_PROTOCOL_ENGINE_PER_L4 DSI2_PROTOCOL_ENGINE_L3 DSI2_PROTOCOL_ENGINE_PER_L4
Description	INTERRUPT STATUS REGISTER - Virtual channel This register regroups all the events related to the virtual channel.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							PP_BUSY_CHANGE_IRQ	FIFO_TX_UDF_IRQ	ECC_NO_CORRECTION_IRQ	BTA_IRQ	FIFO_RX_OVF_IRQ	FIFO_TX_OVF_IRQ	PACKET_SENT_IRQ	ECC_CORRECTION_IRQ	CS_IRQ

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	PP_BUSY_CHANGE_IRQ	Video Port ping-pong buffer busy status. PP_BUSY has changed from 1 to 0. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW	0
7	FIFO_TX_UDF_IRQ	FIFO underflow status. The FIFO used on the L3 interconnect slave port for buffering the data for the virtual channel has underflowed which means that the data for the current packet have not been received in time since the transfer of the packet are already started (transfer started since the packet size is bigger than space allocated in the FIFO). 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW	0
6	ECC_NO_CORRECTION_IRQ	ECC error status (short and long packets). No correction of the header because of more than 1-bit error. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW	0
5	BTA_IRQ	Virtual channel - BTA status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW	0
4	FIFO_RX_OVF_IRQ	FIFO overflow error status. The FIFO used on the L3 interconnect slave port for buffering the data received on the DSI link for the virtual channel has overflowed. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW	0
3	FIFO_TX_OVF_IRQ	FIFO overflow error status. The FIFO used on the L3 interconnect slave port for buffering the data for the virtual channel has overflowed. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW	0

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Bits	Field Name	Description	Type	Reset
2	PACKET_SENT_IRQ	Indicates that a packet has been sent. It is used when BTA manual mode is used. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW	0
1	ECC_CORRECTION_IRQ	Virtual channel - ECC has been used to do the correction of the only 1-bit error status (short and long packet). 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW	0
0	CS_IRQ	Virtual channel - checksum mismatch status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW	0

Table 10-595. Register Call Summary for Register DSI_VC_IRQSTATUS_i

MIPI Display Serial Interface

- DSI Interrupt Requests: [0]
- DSI Transfer Modes: [1] [2] [3]
- Video Port Interface: [4]
- Bus Turnaround: [5] [6]
- Interrupts: [7]
- DSI Command Mode Using the DISPC Video Port: [8] [9] [10] [11] [12] [13]
- DSI_PROTOCOL_ENGINE Register Summary: [14] [15]

Table 10-596. DSI_VC_IRQENABLE_i

Address Offset	0x0000 011C + (0x20 * i)	**Index**	i = 0 to 3
Physical Address	0x5800 411C + (0x20 * i) 0x4804 411C + (0x20 * i) 0x5800 511C + (0x20 * i) 0x4804 511C + (0x20 * i)	**Instance**	DSI1_PROTOCOL_ENGINE_L3 DSI1_PROTOCOL_ENGINE_PER_L4 DSI2_PROTOCOL_ENGINE_L3 DSI2_PROTOCOL_ENGINE_PER_L4
Description	INTERRUPT ENABLE REGISTER - Virtual channel This register regroups all the events related to virtual channel.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							PP_BUSY_CHANGE_IRQ_EN	FIFO_TX_UDF_IRQ_EN	ECC_NO_CORRECTION_IRQ_EN	BTA_IRQ_EN	FIFO_RX_OVF_IRQ_EN	FIFO_TX_OVF_IRQ_EN	PACKET_SENT_IRQ_EN	ECC_CORRECTION_IRQ_EN	CS_IRQ_EN									

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Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	PP_BUSY_CHANGE_IRQ_EN	Video Port ping-pong buffer busy status. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
7	FIFO_TX_UDF_IRQ_EN	FIFO underflow enable. The FIFO used for buffering the data received on the L3 interface slave port for the virtual channel has underflowed which means that the data for the current packet have not been received in time since the transfer of the packet are already started (transfer started since the packet size is bigger than space allocated in the FIFO). 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
6	ECC_NO_CORRECTION_IRQ_EN	ECC error (short and long packets). No correction of the header because of more than 1-bit error. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
5	BTA_IRQ_EN	Virtual channel -Bus turn around reception 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
4	FIFO_RX_OVF_IRQ_EN	FIFO overflow enable. The FIFO used on the L3 interconnect slave port for buffering the data received on the DSI link for the virtual channel has overflowed. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
3	FIFO_TX_OVF_IRQ_EN	FIFO overflow enable. The FIFO used on the L3 interconnect slave port for buffering the data received on the Interface slave port for the virtual channel has overflowed. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
2	PACKET_SENT_IRQ_EN	Indicates that a packet has been sent. It is used when BTA manual mode is used. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
1	ECC_CORRECTION_IRQ_EN	Virtual channel - ECC has been used to correct the only 1-bit error (short and long packet). 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
0	CS_IRQ_EN	Virtual channel - checksum of the payload mismatch detection 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0

Table 10-597. Register Call Summary for Register DSI_VC_IRQENABLE_i

MIPI Display Serial Interface

- DSI Interrupt Requests: [0] [1]
- Video Port Interface: [2]
- Bus Turnaround: [3]
- Interrupts: [4]
- DSI Video Mode Using the DISPC Video Port: [5]
- DSI Command Mode Using the DISPC Video Port: [6]
- DSI_PROTOCOL_ENGINE Register Summary: [7] [8]

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10.3.6.3 DSI_PHY Registers

10.3.6.3.1 DSI_PHY Register Summary

Table 10-598. DSI1_PHY Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	DSI1_PHY L3 Physical Address	DSI1_PHY L4_PER Physical Address
DSI_PHY_REGISTER0	RW	32	0x0000 0000	0x5800 4200	0x4804 4200
DSI_PHY_REGISTER1	RW	32	0x0000 0004	0x5800 4204	0x4804 4204
DSI_PHY_REGISTER2	RW	32	0x0000 0008	0x5800 4208	0x4804 4208
DSI_PHY_REGISTER3	RW	32	0x0000 000C	0x5800 420C	0x4804 420C
DSI_PHY_REGISTER4	RW	32	0x0000 0010	0x5800 4210	0x4804 4210
DSI_PHY_REGISTER5	W	32	0x0000 0014	0x5800 4214	0x4804 4214

Table 10-599. DSI2_PHY Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	DSI2_PHY L3 Physical Address	DSI2_PHY L4_PER Physical Address
DSI_PHY_REGISTER0	RW	32	0x0000 0000	0x5800 5200	0x4804 5200
DSI_PHY_REGISTER1	RW	32	0x0000 0004	0x5800 5204	0x4804 5204
DSI_PHY_REGISTER2	RW	32	0x0000 0008	0x5800 5208	0x4804 5208
DSI_PHY_REGISTER3	RW	32	0x0000 000C	0x5800 520C	0x4804 520C
DSI_PHY_REGISTER4	RW	32	0x0000 0010	0x5800 5210	0x4804 5210
DSI_PHY_REGISTER5	W	32	0x0000 0014	0x5800 5214	0x4804 5214

10.3.6.3.2 DSI_PHY Register Description

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Table 10-600. DSI_PHY_REGISTER0

Address Offset	0x0000 0000		
Physical Address	0x5800 4200 0x4804 4200 0x5800 5200 0x4804 5200	**Instance**	DSI1_PHY_L3 DSI1_PHY_PER_L4 DSI2_PHY_L3 DSI2_PHY_PER_L4
Description	Configuration register for HS mode timings		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REG_THSPREPARE								REG_THSPRPR_THSZERO								REG_THSTRAIL								REG_THSEXIT							

Bits	Field Name	Description	Type	Reset
31:24	REG_THSPREPARE	REG_THSPREPARE timing parameter in multiples of DDR clock period. DDR clock = CLKIN4DDR/4. D-PHY specification: 40 ns + 4 * UI ÷ 85 ns + 6 * UI. UI = Unit Interval, equal to the duration of any HS state on the clock lane. Default value is programmed for 400 MHz.	RW	0x1E
23:16	REG_THSPRPR_THSZERO	REG_THSPREPARE_THSZERO timing parameter in multiples of DDR clock period. DDR clock = CLKIN4DDR/4. D-PHY specification: 145 ns + 10 * UI. Default value is programmed for 400 MHz.	RW	0x48
15:8	REG_THSTRAIL	REG_THSTRAIL timing parameter in multiples of DDR clock period. DDR clock = CLKIN4DDR/4. D-PHY specification: 60 ns + 4 * UI. Default value is programmed for 400 MHz.	RW	0x1D
7:0	REG_THSEXIT	REG_THSEXIT timing parameter in multiples of DDR clock frequency. DDR clock = CLKIN4DDR/4. D-PHY specification: 100 ns. Default value is programmed for 400 MHz.	RW	0x3A

Table 10-601. Register Call Summary for Register DSI_PHY_REGISTER0

MIPI Display Serial Interface

- Clock Requirements: [0] [1] [2] [3] [4] [5] [6] [7]
- SCP Interface: [8]
- Display Timing Configuration: [9] [10] [11] [12] [13]
- DSI Video Mode Using the DISPC Video Port: [14] [15] [16] [17]
- DSI Command Mode Using the DISPC Video Port: [18] [19] [20] [21]
- DSI_PROTOCOL_ENGINE Register Description: [22] [23]
- DSI_PHY Register Summary: [24] [25]

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Table 10-602. DSI_PHY_REGISTER1

Address Offset	0x0000 0004		
Physical Address	0x5800 4204 0x4804 4204 0x5800 5204 0x4804 5204	**Instance**	DSI1_PHY_L3 DSI1_PHY_PER_L4 DSI2_PHY_L3 DSI2_PHY_PER_L4
Description	Configuration register for LP mode and HS mode timings		
Type	RW		

31 30 29	28 27	26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
REG_TTAGO	REG_TTASURE	REG_TTAGET	RESERVED	REG_TLPXBY2	REG_TCLKTRAIL	REG_TCLKZERO

Bits	Field Name	Description	Type	Reset
31:29	REG_TTAGO	TTA-GO timing in terms of number of TXCLKESC clocks. 0x0: 2 cycles 0x1: 3 cycles 0x2: 4 cycles 0x3: 5 cycles 0x4: 6 cycles 0x5: 7 cycles 0x6: 8 cycles 0x7: 9 cycles Default value: 4 cycles	RW	0x2
28:27	REG_TTASURE	TTA-SURE timing in terms of number of TXCLKESC clocks. 0x0: 2 cycles 0x1: 1 cycles 0x2: 3 cycles 0x3: 4 cycles Default value: 2 cycles	RW	0x0
26:24	REG_TTAGET	TTA-GET timing in terms of number of TXCLKESC clocks. 0x0: 3 cycles 0x1: 4 cycles 0x2: 5 cycles 0x3: 6 cycles 0x4: 7 cycles 0x5: 8 cycles 0x6: 9 cycles 0x7: 10 cycles Default value: 5 cycles	RW	0x2
23:21	RESERVED	Reserved	R	0x0
20:16	REG_TLPXBY2	(TLPX)/2 timing parameter in multiples of DDR clock frequency. DDR clock = CLKIN4DDR/4. Default value is programmed for 400 MHz. This is the internal timer value. The value seen on line will have variance due to rise/fall mismatch effects.	RW	0x0A

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Bits	Field Name	Description	Type	Reset
		Note: TLPX is used to define the length of LP-01 state in HS start of Transmission sequences on clock and data lanes. For all other purposes TLPX is defined by the period of TXLPESC		
15:8	REG_TCLKTRAIL	REG_TCLKTRAIL timing parameter in multiples of DDR clock frequency. DDR clock = CLKIN4DDR/4. D-PHY specification: 60 ns. Default value is programmed for 400 MHz	RW	0x1A
7:0	REG_TCLKZERO	REG_TCLKZERO timing parameter in multiples of DDR clock period. DDR clock = CLKIN4DDR/4. D-PHY specification: (REG_TCLKPREPARE + REG_TCLKZERO) 300 ns. Derived specification for REG_TCLKZERO (Min REG_TCLKPREPARE = 38 ns): REG_TCLKZERO 262 ns. Default value is programmed for 400 MHz	RW	0x6A

Table 10-603. Register Call Summary for Register DSI_PHY_REGISTER1

MIPI Display Serial Interface

- Clock Requirements: [0] [1] [2] [3] [4] [5]
- Display Timing Configuration: [6] [7] [8] [9] [10] [11]
- DSI Video Mode Using the DISPC Video Port: [12] [13] [14]
- DSI Command Mode Using the DISPC Video Port: [15] [16] [17] [18]
- DSI_PHY Register Summary: [19] [20]

Table 10-604. DSI_PHY_REGISTER2

Address Offset	0x0000 0008		
Physical Address	0x5800 4208 0x4804 4208 0x5800 5208 0x4804 5208	**Instance**	DSI1_PHY_L3 DSI1_PHY_PER_L4 DSI2_PHY_L3 DSI2_PHY_PER_L4
Description	Sync pattern		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HSSYNCPATTERN								RESERVED							OVRRDULPMTX	REGULPMTX						RESERVED		REG_TCLKPREPARE							

Bits	Field Name	Description	Type	Reset
31:24	HSSYNCPATTERN	Default : 184 (10111000). MSB (last received bit of sync pattern), LSB (first received bit of sync pattern).	RW	0xB8
23:17	RESERVED	Reserved. Read returns zero. Write only zero for future compatibility.	R	0x00
16	OVRRDULPMTX	Global enable of the weak pulldown on the DSI lanes, configured through the [15:11] REGULPMTX bit field: 1: Enable weak pulldown on DSI lanes. 0: Disable weak pulldown on DSI lanes (default).	RW	0
15:11	REGULPMTX	Configuration of the weak pulldowns on the DSI lanes. For each bit, the following settings apply: 1: Enable weak pulldown on the lane.	RW	0x00

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Bits	Field Name	Description	Type	Reset
		0: Disable weak pulldown on the lane (default). Bit [15]: DSI lane 4 (applies only to DSI1; reserved for DSI2) Bit [14]: DSI lane 3 (applies only to DSI1; reserved for DSI2) Bit [13]: DSI lane 2 (applies to DSI1 and DSI2) Bit [12]: DSI lane 1 (applies to DSI1 and DSI2) Bit [11]: DSI lane 0 (applies to DSI1 and DSI2)		
10:8	RESERVED	Reserved	RW	0x0
7:0	REG_TCLKPREPARE	TCLK-PREPARE timing parameter in multiples of DDR clock period. D-PHY specification: 38 ns ÷ 95 ns. Default value is programmed for 400 MHz.	RW	0x1A

Table 10-605. Register Call Summary for Register DSI_PHY_REGISTER2

MIPI Display Serial Interface
- Clock Requirements: [0] [1]
- SCP Interface: [2]
- Display Timing Configuration: [3]
- DSI Video Mode Using the DISPC Video Port: [4]
- DSI Command Mode Using the DISPC Video Port: [5] [6]
- DSI_PROTOCOL_ENGINE Register Description: [7] [8]
- DSI_PHY Register Summary: [9] [10]

Table 10-606. DSI_PHY_REGISTER3

Address Offset	0x0000 000C		
Physical Address	0x5800 420C 0x4804 420C 0x5800 520C 0x4804 520C	**Instance**	DSI1_PHY_L3 DSI1_PHY_PER_L4 DSI2_PHY_L3 DSI2_PHY_PER_L4
Description	Transmitted pattern		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REG_TXTRIGGERESC3								REG_TXTRIGGERESC2								REG_TXTRIGGERESC1								REG_TXTRIGGERESC0							

Bits	Field Name	Description	Type	Reset
31:24	REG_TXTRIGGERESC3	Transmitted pattern when REG_TXTRIGGERESC3 is asserted (first bit transmitted to last bit transmitted). Default: 01100010	RW	0x62
23:16	REG_TXTRIGGERESC2	Default: 01011101	RW	0x5D
15:8	REG_TXTRIGGERESC1	Default: 00100001	RW	0x21
7:0	REG_TXTRIGGERESC0	Default: 10100000	RW	0xA0

Table 10-607. Register Call Summary for Register DSI_PHY_REGISTER3

MIPI Display Serial Interface
- PHY Triggers: [0] [1]
- DSI_PHY Register Summary: [2] [3]

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Table 10-608. DSI_PHY_REGISTER4

Address Offset	0x0000 0010		
Physical Address	0x5800 4210 0x4804 4210 0x5800 5210 0x4804 5210	**Instance**	DSI1_PHY_L3 DSI1_PHY_PER_L4 DSI2_PHY_L3 DSI2_PHY_PER_L4
Description	Received pattern		
Type	RW		

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
REG_RXTRIGGERESC3	REG_RXTRIGGERESC2	REG_RXTRIGGERESC1	REG_RXTRIGGERESC0

Bits	Field Name	Description	Type	Reset
31:24	REG_RXTRIGGERESC3	Received pattern for which REG_RXTRIGGERESC3 is asserted (first bit transmitted to last bit transmitted). Default: 01100010	RW	0x62
23:16	REG_RXTRIGGERESC2	Default: 01011101	RW	0x5D
15:8	REG_RXTRIGGERESC1	Default: 00100001	RW	0x21
7:0	REG_RXTRIGGERESC0	Default: 10100000	RW	0xA0

Table 10-609. Register Call Summary for Register DSI_PHY_REGISTER4

MIPI Display Serial Interface

- PHY Triggers: [0] [1] [2]
- DSI_PHY Register Summary: [3] [4]

Table 10-610. DSI_PHY_REGISTER5

Address Offset	0x0000 0014		
Physical Address	0x5800 4214 0x4804 4214 0x5800 5214 0x4804 5214	**Instance**	DSI1_PHY_L3 DSI1_PHY_PER_L4 DSI2_PHY_L3 DSI2_PHY_PER_L4
Description	Reset done bits		
Type	R		

31	30	29	28	27	26	25	24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
RESETDONETXBYTECLK	RESETDONESCPCLK	RESETDONEPWRCLK	RESETDONETXCLKESC4	RESETDONETXCLKESC3	RESETDONETXCLKESC2	RESETDONETXCLKESC1	RESETDONETXCLKESC0	RESERVED		

Bits	Field Name	Description	Type	Reset
31	RESETDONETXBYTECLK	RESETDONETXBYTECLK 0x0: No reset 0x1: Reset done for the TXBYTECLK domain	R	0
30	RESETDONESCPCLK	RESETDONESCPCLK 0x0: No reset 0x1: Reset done for the SCP clock domain	R	0

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Bits	Field Name	Description	Type	Reset
29	RESETDONEPWRCLK	RESETDONEPWRCLK 0x0: No reset 0x1: Reset done for the PWR clock domain	R	0
28	RESETDONETXCLKESC4	RESETDONETXCLKESC4 0x0: No reset 0x1: Reset done for the TXCLKESC domain for lane 4	R	0
27	RESETDONETXCLKESC3	RESETDONETXCLKESC3 0x0: No reset 0x1: Reset done for the TXCLKESC domain for lane 3	R	0
26	RESETDONETXCLKESC2	RESETDONETXCLKESC2 0x0: No reset 0x1: Reset done for the TXCLKESC domain for lane 2	R	0
25	RESETDONETXCLKESC1	RESETDONETXCLKESC1 0x0: No reset 0x1: Reset done for the TXCLKESC domain for lane 1	R	0
24	RESETDONETXCLKESC0	RESETDONETXCLKESC0 0x0: No reset 0x1: Reset done for the TXCLKESC domain for lane 0	R	0
23:0	RESERVED	Read-Only register. Read returns zero.	R	0x000000

Table 10-611. Register Call Summary for Register DSI_PHY_REGISTER5

MIPI Display Serial Interface

- Reset-Done Bits: [0] [1] [2] [3] [4] [5] [6]
- DSI_PHY Register Summary: [7] [8]

10.3.6.4 DSI _PLLCTRL Registers

10.3.6.4.1 DSI_PLLCTRL Register Summary

Table 10-612. DSI1_PLLCTRL Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	DSI1_PLLCTRL L3 Physical Address	DSI1_PLLCTRL L4_PER Physical Address
DSI_PLL_CONTROL	RW	32	0x0000 0000	0x5800 4300	0x4804 4300
DSI_PLL_STATUS	R	32	0x0000 0004	0x5800 4304	0x4804 4304
DSI_PLL_GO	RW	32	0x0000 0008	0x5800 4308	0x4804 4308
DSI_PLL_CONFIGURATION1	RW	32	0x0000 000C	0x5800 430C	0x4804 430C
DSI_PLL_CONFIGURATION2	RW	32	0x0000 0010	0x5800 4310	0x4804 4310
DSI_PLL_CONFIGURATION3	RW	32	0x0000 0014	0x5800 4314	0x4804 4314
DSI_PLL_SSC_CONFIGURATION1	RW	32	0x0000 0018	0x5800 4318	0x4804 4318
DSI_PLL_SSC_CONFIGURATION2	RW	32	0x0000 001C	0x5800 431C	0x4804 431C
DSI_PLL_CONFIGURATION4	RW	32	0x0000 0020	0x5800 4320	0x4804 4320

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Table 10-613. DSI2_PLLCTRL Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	DSI2_PLLCTRL L3 Physical Address	DSI2_PLLCTRL L4_PER Physical Address
DSI_PLL_CONTROL	RW	32	0x0000 0000	0x5800 5300	0x4804 5300
DSI_PLL_STATUS	R	32	0x0000 0004	0x5800 5304	0x4804 5304
DSI_PLL_GO	RW	32	0x0000 0008	0x5800 5308	0x4804 5308
DSI_PLL_CONFIGURATION1	RW	32	0x0000 000C	0x5800 530C	0x4804 530C
DSI_PLL_CONFIGURATION2	RW	32	0x0000 0010	0x5800 5310	0x4804 5310
DSI_PLL_CONFIGURATION3	RW	32	0x0000 0014	0x5800 5314	0x4804 5314
DSI_PLL_SSC_CONFIGURATION1	RW	32	0x0000 0018	0x5800 5318	0x4804 5318
DSI_PLL_SSC_CONFIGURATION2	RW	32	0x0000 001C	0x5800 531C	0x4804 531C
DSI_PLL_CONFIGURATION4	RW	32	0x0000 0020	0x5800 5320	0x4804 5320

10.3.6.4.2 DSI_PLLCTRL Register Description

Table 10-614. DSI_PLL_CONTROL

Address Offset	0x0000 0000		
Physical Address	0x5800 4300 0x4804 4300 0x5800 5300 0x4804 5300	**Instance**	DSI1_PLLCTRL_L3 DSI1_PLLCTRL_PER_L4 DSI2_PLLCTRL_L3 DSI2_PLLCTRL_PER_L4
Description	This register controls the PLL reset/power and modes		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																											HSDIV_SYSRESET	PLL_SYSRESET	PLL_HALTMODE	PLL_GATEMODE	PLL_AUTOMODE

Bits	Field Name	Description	Type	Reset
31:5	RESERVED	Reads as zero.	R	0x0000000
4	HSDIV_SYSRESET	Force HSDIVIDER SYSRESET 0x0: HSDIVIDER SYSRESET controlled by power FSM 0x1: HSDIVIDER SYSRESET forced active	RW	0
3	PLL_SYSRESET	Force ADPLLM SYSRESET 0x0: PLL SYSRESET controlled by power FSM 0x1: PLL SYSRESET forced active	RW	0
2	PLL_HALTMODE	Allow PLL to be halted if no activity. Reserved when DSI1_PLLCTRL_AUTO is 0. 0x0: PLL will not be halted 0x1: PLL will be halted based on activity	RW	0

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Bits	Field Name	Description	Type	Reset
1	PLL_GATEMODE	Allow PLL clock gating for power saving Reserved when DSI1_PLLCTRL_AUTO is 0. 0x0: CLKIN4DDR clock on 0x1: CLKIN4DDR clock gated by DSI Protocol Engine activity	RW	0
0	PLL_AUTOMODE	Automatic update mode. If this bit is set then the configuration updates will be synchronised to DISPCUpdateSync. If this bit is clear configuration updates will be done immediately. Reserved when DSI1_PLLCTRL_AUTO is 0. 0x0: Manual mode 0x1: Automatic mode	RW	0

Table 10-615. Register Call Summary for Register DSI_PLL_CONTROL

MIPI Display Serial Interface

- DSI PLL Clock-Gating Sequence: [0]
- DSI PLL Go Sequence: [1] [2] [3] [4]
- DSI PLL Recommended Values: [5] [6] [7] [8] [9]
- DSI Video Mode Using the DISPC Video Port: [10]
- DSI Command Mode Using the DISPC Video Port: [11]
- DSI_PLLCTRL Register Summary: [12] [13]

Table 10-616. DSI_PLL_STATUS

Address Offset	0x0000 0004		
Physical Address	0x5800 4304 0x4804 4304 0x5800 5304 0x4804 5304	**Instance**	DSI1_PLLCTRL_L3 DSI1_PLLCTRL_PER_L4 DSI2_PLLCTRL_L3 DSI2_PLLCTRL_PER_L4
Description	This register contains the status information		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																			SSC_EN_ACK	M7_CLOCK_ACK	RESERVED	BYPASSACKZ	M5_CLOCK_ACK	M4_CLOCK_ACK	PLL_BYPASS	PLL_HIGHJITTER	PLL_LIMP	PLL_LOSSREF	PLL_RECAL	PLL_LOCK	DSI1_PLLCTRL_RESET_DONE

Bits	Field Name	Description	Type	Reset
31:13	RESERVED	Reads as zero.	R	0x00000
12	SSC_EN_ACK	Spread Spectrum Clocking acknowledge Read 0x0: Spread Spectrum Clocking inactive Read 0x1: Spread Spectrum Clocking active	R	0

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Bits	Field Name	Description	Type	Reset
11	M7_CLOCK_ACK	Acknowledge for enable of clock Verify the status before selecting this source in the clock mux Read 0x0: M7 clock inactive Read 0x1: M7 clock active	R	0
10	RESERVED	Reserved	R	0
9	BYPASSACKZ	State of bypass mode on PHY and HSDIVIDER Read 0x0: DSI_PHY and HSDIVIDER have switched to using the bypass clocks. Read 0x1: PLL outputs are still being used by DSI_PHY or HSDIVIDER	R	0
8	M5_CLOCK_ACK	Acknowledge for enable of DSI Protcol Engine clock Verify the status before selecting this source in the DSI Protcol Engine clock mux Read 0x0: M5 Protocol Engine clock inactive Read 0x1: M5 Protocol Engine clock active	R	0
7	M4_CLOCK_ACK	Acknowledge for enable of clock Verify the status before selecting this source in the clock mux Read 0x0: M4 clock inactive Read 0x1: M4 clock active	R	0
6	PLL_BYPASS	DSI PLL Bypass status Read 0x0: PLL not bypassing Read 0x1: PLL bypass	R	0
5	PLL_HIGHJITTER	PLL High Jitter status Read 0x0: PLL in normal jitter condition Read 0x1: PLL in high jitter condition: Phase error 24%	R	0
4	PLL_LIMP	PLL Limp status Read 0x0: LIMP mode inactive Read 0x1: LIMP mode active	R	0
3	PLL_LOSSREF	PLL Reference Loss status Read 0x0: Reference input active Read 0x1: Reference input inactive	R	0
2	PLL_RECAL	PLL recalibration status If this bit is active, the PLL needs to be recalibrated Read 0x0: Recalibration is not required Read 0x1: Recalibration is required	R	0
1	PLL_LOCK	PLL Lock status See the programming guide for the use of this bit Read 0x0: PLL is not locked Read 0x1: PLL is locked	R	0
0	DSI1_PLLCTRL_RESET_DONE	DSI1_PLLCTRL reset done status Read 0x0: Reset is in progress Read 0x1: Reset has completed	R	0

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Table 10-617. Register Call Summary for Register DSI_PLL_STATUS

MIPI Display Serial Interface

- DSI PLL Controllers Architecture: [0]
- Error Handling: [1] [2] [3] [4]
- Software Reset: [5]
- DSI PLL Clock-Gating Sequence: [6]
- DSI PLL Clock Sequence: [7]
- DSI PLL Go Sequence: [8]
- DSI Video Mode Using the DISPC Video Port: [9]
- DSI Command Mode Using the DISPC Video Port: [10]
- DSI_PLLCTRL Register Summary: [11] [12]

Table 10-618. DSI_PLL_GO

Address Offset	0x0000 0008		
Physical Address	0x5800 4308 0x4804 4308 0x5800 5308 0x4804 5308	**Instance**	DSI1_PLLCTRL_L3 DSI1_PLLCTRL_PER_L4 DSI2_PLLCTRL_L3 DSI2_PLLCTRL_PER_L4
Description	This register contains the GO bit		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															PLL_GO

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved. Wirte only zero for future compatibility. Reads return zero.	R	0x0000 0000
0	PLL_GO	Request (re-)locking sequence of the PLL. If the AutoMode bit is set, then this will be deferred until DISPCUpdate Sync goes active 0x0: No pending action 0x1: Request PLL (re-)locking/locking pending	RW	0

Table 10-619. Register Call Summary for Register DSI_PLL_GO

MIPI Display Serial Interface

- DSI PLL Clock-Gating Sequence: [0] [1]
- DSI PLL Clock Sequence: [2]
- DSI PLL Go Sequence: [3] [4]
- DSI PLL Recommended Values: [5]
- DSI Video Mode Using the DISPC Video Port: [6] [7]
- DSI Command Mode Using the DISPC Video Port: [8] [9]
- DSI_PLLCTRL Register Summary: [10] [11]

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Table 10-620. DSI_PLL_CONFIGURATION1

Address Offset	0x0000 000C		
Physical Address	0x5800 430C 0x4804 430C 0x5800 530C 0x4804 530C	**Instance**	DSI1_PLLCTRL_L3 DSI1_PLLCTRL_PER_L4 DSI2_PLLCTRL_L3 DSI2_PLLCTRL_PER_L4
Description	This register contains the latched PLL and HSDIVDER configuration bits		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	M5_CLOCK_DIV							M4_CLOCK_DIV								PLL_REGM								PLL_REGN							PLL_STOPMODE

Bits	Field Name	Description	Type	Reset
31	RESERVED		R	0
30:26	M5_CLOCK_DIV	Divider value for Protocol Engine clock source M5REG	RW	0x00
25:21	M4_CLOCK_DIV	Divider value for clock source M4REG	RW	0x00
20:9	PLL_REGM	M Divider for PLL	RW	0x000
8:1	PLL_REGN	N Divider for PLL (Reference) **Note:** As a result of device-specific integration, the 8th MSB of this field has no effect; thus, the divider factor can be 0 to 127.	RW	0x00
0	PLL_STOPMODE	PLL STOPMODE 0x0: STOPMODE is not selected 0x1: STOPMODE is selected	RW	0

Table 10-621. Register Call Summary for Register DSI_PLL_CONFIGURATION1

MIPI Display Serial Interface

- DSI PLL Controllers Architecture: [0] [1]
- DSI PLL Operations: [2] [3] [4]
- DSI PLL Clock Sequence: [5] [6] [7] [8]
- DSI PLL Recommended Values: [9] [10] [11] [12] [13]
- DSI Video Mode Using the DISPC Video Port: [14] [15] [16] [17] [18]
- DSI Command Mode Using the DISPC Video Port: [19] [20] [21] [22] [23]
- DSI_PLLCTRL Register Summary: [24] [25]

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Table 10-622. DSI_PLL_CONFIGURATION2

Address Offset	0x0000 0010		
Physical Address	0x5800 4310 0x4804 4310 0x5800 5310 0x4804 5310	**Instance**	DSI1_PLLCTRL_L3 DSI1_PLLCTRL_PER_L4 DSI2_PLLCTRL_L3 DSI2_PLLCTRL_PER_L4
Description	This register contains the unlatched PLL and HSDIVDER configuration bits These bits are "shadowed" when automatic mode is selected		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					M7_CLOCK_PWDN	M7_CLOCK_EN	RESERVED	RESERVED	RESERVED		HSDIVBYPASS	M5_CLOCK_PWDN	M5_CLOCK_EN	M4_CLOCK_PWDN	M4_CLOCK_EN	BYPASSEN	PHY_CLKINEN	PLL_REFEN	RESERVED	RESERVED	PLL_LOCKSEL		PLL_DRIFTGUARDEN	RESERVED	PLL_LOWCURRSTBY	PLL_PLLPMODE	RESERVED	RESERVED		PLL_IDLE

Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Read as zero.	R	0x00
26	M7_CLOCK_PWDN	Power down for M7 clock source 0x0: M7 clock divider is active 0x1: M7 clock divider is powered-down	RW	0
25	M7_CLOCK_EN	Enable for M7 clock source 0x0: M7 clock divider is disbled 0x1: M7 clock divider is enabled	RW	0
24	RESERVED	Reserved	R	0
23	RESERVED	Reserved	R	0
22:21	RESERVED	Reserved	R	0x0
20	HSDIVBYPASS	Forces HSDIVIDER to bypass mode 0x0: HSDIVIDER in normal operation. Bypass controlled by PLL. 0x1: HSDIVIDER forced to bypass mode.	RW	0
19	M5_CLOCK_PWDN	Power down for Protocol Engine clock source 0x0: DSI Protocol Engine clock divider is active 0x1: DSI Protocol Engine clock divider is powered-down	RW	0
18	M5_CLOCK_EN	Enable for Protocol Engine clock source 0x0: DSI Protocol Engine clock divider is disabled 0x1: DSI Protocol Engine clock divider is enabled	RW	0
17	M4_CLOCK_PWDN	Power down for M4 clock source 0x0: clock divider is active 0x1: clock divider is powered-down	RW	0
16	M4_CLOCK_EN	Enable for M4 clock source 0x0: clock divider is disabled 0x1: clock divider is enabled	RW	0

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Bits	Field Name	Description	Type	Reset
15	BYPASSEN	Selects functional clock asCLKIN4DDR clock source 0x0: PLL controls CLKIN4DDR clock source: PLL DCO if PLL is locked functional clock if not locked 0x1: Force functional clock to be used as CLKIN4DDR clock source	RW	0
14	PHY_CLKINEN	CLKIN4DDR clock control 0x0: CLKIN4DDR clock is disabled 0x1: CLKIN4DDR clock is enabled	RW	0
13	PLL_REFEN	PLL reference clock control 0x0: PLL reference clock disabled 0x1: PLL reference clock enabled	RW	0
12	RESERVED	Reserved. Keep at reset value.	R	0
11	RESERVED	Reserved. Keep at reset value.	R	0
10:9	PLL_LOCKSEL	Selects the lock criteria for the PLL 0x0: Phase Lock 0x1: Frequency Lock 0x2: Spare	RW	0x0
8	PLL_DRIFTGUARDEN	PLL DRIFTGUARDEN 0x0: Only RECAL flag is asserted in case of temperature drift. The programmer should take appropriate action. 0x1: Temperature drift will initiate automatic recalibration. RECAL flag will be asserted while this is taking place.	RW	0
7	RESERVED		R	0
6	PLL_LOWCURRSTBY	PLL LOW CURRENT STANDBY 0x0: LOWCURRSTBY is not selected 0x1: LOWCURRSTBY is selected	RW	0
5	PLL_PLLLPMODE	Select the power / performance of the PLL 0x0: Full performance, minimised jitter 0x1: Reduced power, increased jitter	RW	0
4	RESERVED	Reads return zero.	R	0
3:1	RESERVED	Reserved	R	0
0	PLL_IDLE	PLL IDLE: 0x0: IDLE is not selected 0x1: IDLE is selected	RW	0

Table 10-623. Register Call Summary for Register DSI_PLL_CONFIGURATION2

MIPI Display Serial Interface

- DSI Clock Configuration: [0]
- DSI PLL Controllers Architecture: [1]
- DSI PLL Operations: [2] [3]
- DSI PLL Clock-Gating Sequence: [4]
- DSI PLL Clock Sequence: [5]
- DSI PLL Go Sequence: [6] [7] [8] [9]
- DSI PLL Recommended Values: [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22]
- Display Timing Configuration: [23]
- DSI Video Mode Using the DISPC Video Port: [24] [25] [26] [27]
- DSI Command Mode Using the DISPC Video Port: [28] [29] [30] [31]
- DSI_PLLCTRL Register Summary: [32] [33]

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Table 10-624. DSI_PLL_CONFIGURATION3

Address Offset	0x0000 0014		
Physical Address	0x5800 4314 0x4804 4314 0x5800 5314 0x4804 5314	**Instance**	DSI1_PLLCTRL_L3 DSI1_PLLCTRL_PER_L4 DSI2_PLLCTRL_L3 DSI2_PLLCTRL_PER_L4
Description	HSDIVIDER configuration bits for the M5 and M6 dividers		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED						M7_CLOCK_DIV							RESERVED		

Bits	Field Name	Description	Type	Reset
31:18	RESERVED	Reserved	R	0x0000
17:10	RESERVED	Reserved	R	0x000
9:5	M7_CLOCK_DIV	Divider value for M7 divider.	RW	0x00
4:0	RESERVED	Reserved	R	0x00

Table 10-625. Register Call Summary for Register DSI_PLL_CONFIGURATION3

MIPI Display Serial Interface

- DSI PLL Clock Sequence: [0]
- DSI_PLLCTRL Register Summary: [1] [2]

Table 10-626. DSI_PLL_SSC_CONFIGURATION1

Address Offset	0x0000 0018		
Physical Address	0x5800 4318 0x4804 4318 0x5800 5318 0x4804 5318	**Instance**	DSI1_PLLCTRL_L3 DSI1_PLLCTRL_PER_L4 DSI2_PLLCTRL_L3 DSI2_PLLCTRL_PER_L4
Description	Configuration for PLL Spread Spectrum Clocking modulation		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													DOWNSPREAD	RESERVED	EN_SSC

Bits	Field Name	Description	Type	Reset
31:3	RESERVED	RESERVED	R	0x0000 0000
2	DOWNSPREAD	Forces the clock spreading only in the down spectrum. 0x0: Clock spreading not forced. 0x1: Spectrum spreading only in down direction.	RW	0
1	RESERVED	Reserved. Reads return 0.	R	0
0	EN_SSC	Spread Spectrum Clockiing enable 0x0: Spread Spectrum Clockiing disabled 0x1: Spread Spectrum Clockiing enabled	RW	0

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Table 10-627. Register Call Summary for Register DSI_PLL_SSC_CONFIGURATION1

MIPI Display Serial Interface

- DSI PLL Controllers Architecture: [0] [1] [2]
- DSI_PLLCTRL Register Summary: [3] [4]

Table 10-628. DSI_PLL_SSC_CONFIGURATION2

Address Offset	0x0000 001C		
Physical Address	0x5800 431C 0x4804 431C 0x5800 531C 0x4804 531C	**Instance**	DSI1_PLLCTRL_L3 DSI1_PLLCTRL_PER_L4 DSI2_PLLCTRL_L3 DSI2_PLLCTRL_PER_L4
Description	Configuration for PLL Spread Spectrum Clocking modulation		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								MODFREQDIVIDER																DELTAM							

Bits	Field Name	Description	Type	Reset
31:30	RESERVED	Reads as zero	R	0x0
29:20	MODFREQDIVIDER	Modulation Frequency Divider (ModFreqDivider) control for SSC The ModFreqDivider is split into Mantissa and $2^{Exponent}$ (ModFreqDivider = ModFreqDividerMantissa * $2^{ModFreqDividerExponent}$). Bits [26:20] define the Mantissa. Bits [29:27] define the Exponent.	RW	0x000
19:0	DELTAM	DeltaM control for SSC. Split into integer and fractional parts. Bits [19:18] define the integer part. Bits [17:0] define the fractional part.	RW	0x00000

Table 10-629. Register Call Summary for Register DSI_PLL_SSC_CONFIGURATION2

MIPI Display Serial Interface

- DSI PLL Controllers Architecture: [0] [1]
- DSI_PLLCTRL Register Summary: [2] [3]

Table 10-630. DSI_PLL_CONFIGURATION4

Address Offset	0x0000 0020		
Physical Address	0x5800 4320 0x4804 4320 0x5800 5320 0x4804 5320	**Instance**	DSI1_PLLCTRL_L3 DSI1_PLLCTRL_PER_L4 DSI2_PLLCTRL_L3 DSI2_PLLCTRL_PER_L4
Description	Allows setting the fractional M divider for PLL.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PLL_REGM_F															

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Bits	Field Name	Description	Type	Reset
31:18	RESERVED	Reads as zero.	R	0x0000
17:0	PLL_REGM_F	Fractional part of M divider.	RW	0x00000

Table 10-631. Register Call Summary for Register DSI_PLL_CONFIGURATION4

MIPI Display Serial Interface

- DSI PLL Controllers Architecture: [0]
- DSI_PLLCTRL Register Summary: [1] [2]

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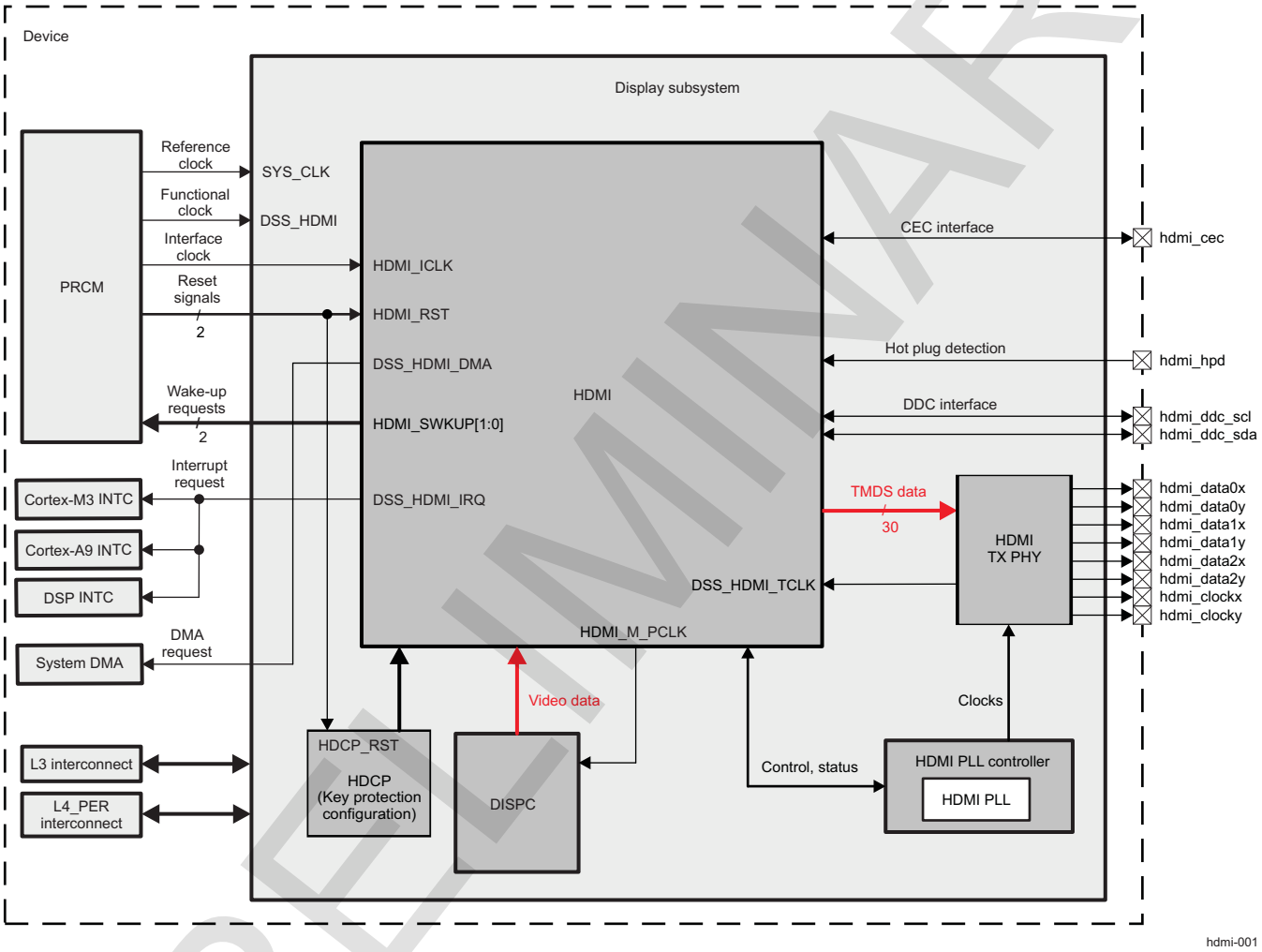
10.4 High-Definition Multimedia Interface

This section introduces the high-definition multimedia interface (HDMI) module. It also describes its main functions and connections in the device.

10.4.1 High-Definition Multimedia Interface (HDMI) Overview

Figure 10-161 shows an overview of the HDMI module.

Figure 10-161. HDMI Overview



10.4.1.1 HDMI Main Features

The HDMI module provides the following main features:

- HDMI 1.3, HDCP 1.2, and DVI 1.0 compliant
  - Including support for the 3D stereoscopic frame-packing formats of the HDMI v1.4 standard (720p, 50 Hz; 720p, 60 Hz; and 1080p, 24 Hz)
- EIA/CEA-861-D video format support (refer to Table 10-632 for more details)
- VESA DMT video format support (refer to Table 10-633 for more details)
- Support for deep-color mode:
  - 10-bit/component color depth up to 1080p @60Hz
  - 12-bit/component color depth up to 720p/1080i @60Hz
- Supports up to 148.5 MHz pixel clock (1920 x 1080p @60Hz)

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- Video formats: 24-bit RGB
- Uncompressed multi-channel (up to 8 channels) audio (L-PCM) support
- Master I2C interface for Display Data Channel (DDC) connection
- Consumer Electronic Control (CEC) interface
- Integrated High-bandwith Digital Content Protection (HDCP) encryption engine for transmitting protected audio and video content (authentication performed by software)
- Integrated Transition Minimized Differential Signaling (TMDS) and TMDS Error Reduction Coding (TERC4) encoders for data island support
- Integrated TMDS PHY (3 TMDS differential data lanes + TMDS differential clock lane)
  - Up to 1,85625 Gbps per lane at (1080p @60Hz at 10 bits/component, lower resolutions at 12 bits/component)
  - 928,125Mbps per lane at (720p/1080i @60Hz 10 bits/component, lower resolutions at 12 bits/component)
  - 337,5 Mbps at (576p @50Hz/480p @60Hz 10 bits/component)

10.4.1.2 HDMI Video Formats and Timings

10.4.1.2.1 CEA-861-D video formats and timings

Table 10-632 presents the video timings supported by the HDMI module, according to the CEA-861-D standart:

Table 10-632. HDMI Video Timings (CEA-861-D)

Refresh Rate	Resolution
24 Hz (Low field rate)	1920 x 1080p
50 Hz	1920 x 1080p 1920 x 1080i 1280 x 720p 2880 x 576p 1440 x 576p 1440 x 576i 720 x 576p
59.94 Hz	1920 x 1080p 2880 x 480p 1440 x 480p 1440 x 480i 720 x 480p 640 x 480p
60 Hz	1920 x 1080p 1920 x 1080i 2880 x 480p 1280 x 720p 1440 x 480p 1440 x 480i 720 x 480p 640 x 480p

10.4.1.2.2 VESA DMT video formats and timings

Table 10-633 presents the video timings supported by the HDMI module, according to the VESA DMT standart:

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Table 10-633. HDMI Video timings (VESA DMT)

Refresh Rate	Resolution
60 Hz	640 x 480p 800 x 600p 848 x 480p 1024 x 768p 1280 x 768p 1280 x 800p 1280 x 960p 1280 x 1024p 1360 x 768p 1366 x 768p 1400 x 1050p 1440 x 900p 1680 x 1050p 1920 x 1080p
60 Hz (Reduced Blanking)	1280 x 768p 1280 x 800p 1400 x 1050p 1440 x 900p 1680 x 1050p

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10.5 Remote Frame Buffer Interface

This section describes the remote frame buffer interface (RFBI).

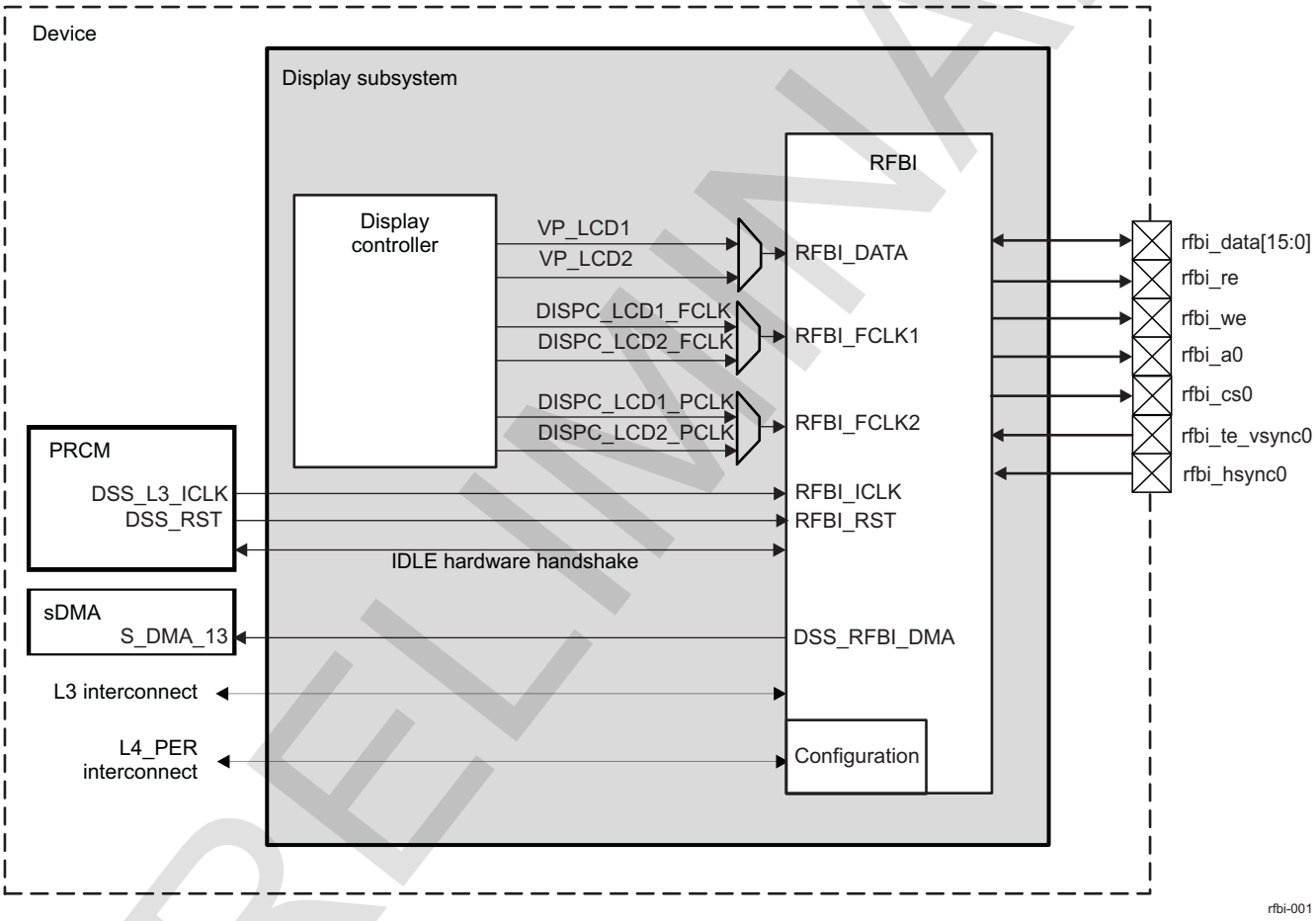
10.5.1 Remote Frame Buffer Interface Overview

The RFBI module is part of the display subsystem that provides the logic to display a picture from the memory frame buffer (SDRAM or SRAM) on a LCD panel.

The RFBI is connected to the L3 and L4_PER interconnect through the display subsystem local interconnect. It is preferred from a performance point of view to use the L4_PER interconnect for configuration and the L3 interconnect for data transfer.

Figure 10-162 shows an overview of the RFBI.

Figure 10-162. RFBI Highlight



The RFBI supports the MIPI DBI protocol with the following features:

- Access to RFB direct MPU interface
  - Sends commands to the RFB panel through the slave port interconnect
  - Sends data, received from the DISPC or from the MPU through the DISPC pixel data bus, to the RFB panel
  - Reads data/status from the RFB to the slave port interconnect
- RFB interface
  - 8-/9-/16-bit parallel interface
  - One programmable configuration for one LCD connected to the RFBI
- Data formats

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  - Programmable pixel modes (12-/16-/18-/24-BPP modes in RGB format)
  - Programmable output formats on one/multiple cycles per pixel (data from the DISPC and the L3 interconnect)
- FIFO
  - One slave port with DMA request and interconnect FIFO of 24 × 32-bit depth (for write access to the RFBI_DATA register only)
  - One video port FIFO of 8 × 24-bit depth receiving data from the DISPC through RFBI_DATA

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10.5.2 RFBI Environment

In the display subsystem, data are read by the DISPC from the memory frame buffer (SDRAM, SRAM, IVA-HD SL2, etc.), and sent through the RFBI to the external LCD/RFB.

The DISPC associated with the RFBI implements the MIPI DBI protocol.

The DISPC provides the required control signals to interface the memory frame buffer (SDRAM, SRAM or IVAHD-SL2) directly to the external displays. The RFBI is connected to the memory through the L3 interconnect and has its own DMA (with embedded FIFOs) to read data from the system memory. There is one master port (L3 interconnect) and two slave ports (one for L4_PER interconnect and the other for L3 interconnect).

The DISPC_CONTROL1[16] GPOUT[1] and DISPC_CONTROL1[15] GPOUT[0] bits control selection of the display subsystem modules (see Table 10-634).

Table 10-634. I/O Pad Mode Selection

DSS.DISPC_CONTROL[16] GPOUT1	DSS.DISPC_CONTROL[15] GPOUT0	Mode
0	0	Reset
0	1	RFBI mode
1	0	Invalid
1	1	Bypass mode

The RFB of the LCD panel is directly connected to the RFBI of the device. The RFBI controls the reads/writes from/to the RFB. The RFBI receives data from its slave port or output from the DISPC and generates the signals to control the LCD panel. Through the RFBI, the MPU can send commands or parameter/display data to the LCD panel and directly set the DISPC registers to read/write data from/to the memory in the LCD panel. The RFBI can manage only one LCD panel.

10.5.2.1 RFBI Parallel Interface (MIPI DBI Protocol)

Figure 10-163 shows the LCD support parallel interface in RFBI mode.

Figure 10-163. RFBI LCD Support Interface

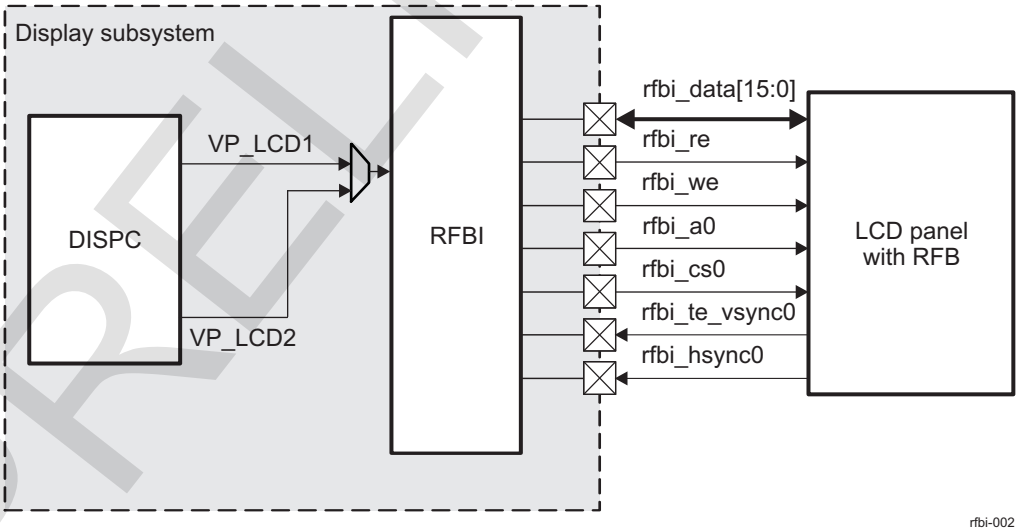

Table 10-635 describes the interface signals to/from the LCD panel.

Table 10-635. LCD Interface Signals

Signal Name	Type [1]	Description
rfbi_data[15:0]	I/O	RFBI I/O data

[1] I = Input; O = Output; I/O = Input/Output

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Table 10-635. LCD Interface Signals (continued)

Signal Name	Type [1]	Description
rfbi_re	O	Read access signal
rfbi_we	O	Write access signal
rfbi_a0	O	Command/data selection signal
rfbi_cs0	O	Chip-select (CS) signal for LCD 1
rfbi_te_vsync0	I	Tearing effect (TE) synchronization signal (TE or VSYNC for LCD panel 1)
rfbi_hsync0	I	HSYNC from LCD panel 1

- rfbi_data[15:0]: The pixel data comprises the RFBI pixel data (bits 15:0). A write/read command must be sent to the LCD panel to send/read the data.

  Before any data access, the application must send commands and parameters when it is necessary to configure an LCD panel. The data is used as input in read operations during production test and also to read the status of the registers in the LCD panel and pixels from the embedded frame buffer in the LCD panel.
- rfbi_re: This is the read-enable signal used to indicate when a read from the embedded memory in the LCD panel is ongoing. The RFBI registers describe the behavior of the read signal (off/on/cycle time). The polarity of the read-enable signal is programmable. The read is used to get status/data information from the LCD panel.
- rfbi_we: The write-enable signal is used to indicate when a write is ongoing. The RFBI registers allow flexible behavior of the write signal (programmable off/on/cycle times and signal polarity).
- rfbi_a0: The signal is asserted to indicate its status: Command or data. The polarity is programmable and the status of the signal depends on the RFBI registers written by the application (CMD/READ/STATUS/PARAM/PIXEL). The register in use by the hardware defines the status of rfbi_a0. The order of the writes/reads to the RFBI registers CMD/READ/STATUS/PARAM/PIXEL defines the transitions of A0.
- rfbi_cs0: The signal is the chip-select (CS0) asserted to indicate which LCD panel is selected and must be ready to receive/transmit commands and data. When RE or WE is on, CS*0* must not be changed.

  To select the trigger mode, configure the RFBI_CONFIG[3:2] TRIGGERMODE bit field (0x0: Internal trigger mode with the RFBI_CONTROL[4] ITE bit, 0x1: External trigger mode with the TE signal rfbi_tevsync0, 0x2: External trigger mode with the rfbi_tevsync0, and rfbi_hsync0 signals with the programmable line counter).
- rfbi_te_vsync0 (only used by RFBI if RFBI_CONFIG[3:2] TRIGGERMODE = 0x1 or 0x2, otherwise ignored): Based on the trigger mode selected, the signal is the TE pulse signal or the LCD panel vertical synchronization (VSYNC) pulse signal. rfbi_te_vsync0 is used by the TE logic as the synchronization signal to send the pixel to the LCD panel.
- rfbi_hsync0 (only used by RFBI if RFBI_CONFIG[3:2] TRIGGERMODE = 0x2, otherwise ignored): The HSYNC pulse signals indicate to the RFBI when horizontal synchronization occurs. The polarity of the HSYNC signals is programmable. The minimum pulse width of the signal is two RFBI_ICLK clock cycles. rfbi_hsync0 is used by the TE logic as a synchronization signal to send the pixel to the LCD panel.

10.5.2.1.1 Description of the Tearing Effect Pulse Signal

The TE signal can be generated externally by the RFBI depending on the value of the RFBI_CONFIG[3:2] TRIGGERMODE bit field:

- TRIGGERMODE = 0x1: external trigger mode with TE signal. TE signal corresponds to rfbi_te_vsync0 pad.
- TRIGGERMODE = 0x2: external trigger mode with HSYNC/VSYNC signals. HSYNC signal corresponds to rfbi_hsync0 pad and VSYNC signal to rfbi_te_vsync0 pad.

The externally generated TE synchronization signal is a logical OR or AND operation between the HSYNC and VSYNC signals (see Figure 10-164). The logical operation (OR or AND) depends on the HSYNC and VSYNC signals polarity. The VSYNC signal indicates to the RFBI when vertical synchronization occurs; the HSYNC signal indicates to the RFBI when horizontal synchronization occurs.

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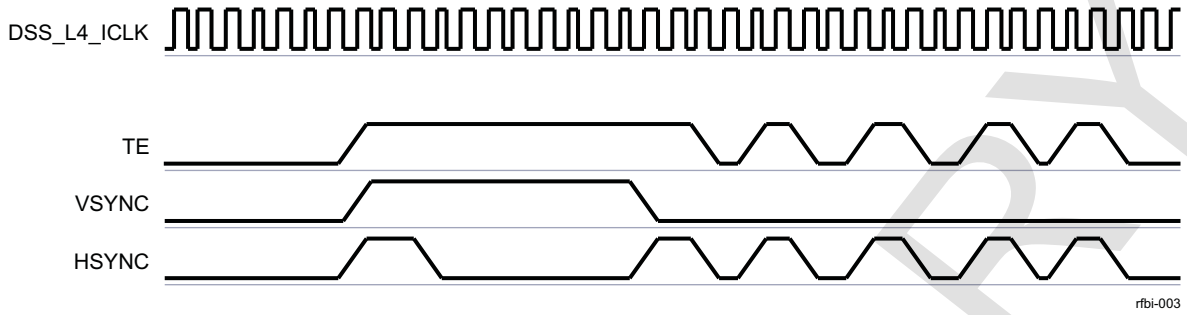
Figure 10-164. External Generation of TE Signal Based on Logical OR Operation Between HSYNC and VSYNC (Active-High)



- TE signal is connected to rfbi_te_vsync0 external pad when the RFBI_CONFIG[3:2] TRIGGERMODE bit field is set to 0x1.
- HSYNC and VSYNC signals are connected to rfbi_hsync0 and rfbi_te_vsync0, respectively, when the RFBI_CONFIG[3:2] TRIGGERMODE bit field is set to 0x2.

The RFBI module detects the VSYNC and HSYNC pulses embedded in the received signal. VSYNC is detected based on the minimum pulse width defined by the RFBI_VSYNC_WIDTH register. VSYNC is not triggered by an inactive-to-active edge.

HSYNC is detected based on the minimum pulse width defined by the RFBI_HSYNC_WIDTH register. HSYNC is not triggered by an inactive-to-active edge.

The signal is generated from external logic based on VSYNC and HSYNC of the LCD panel. The automatic trigger can be programmed based on the external RFBI_TE signal or use the RFBI_CONTROL[4] ITE bit to start data capture (internal trigger mode).

The polarity of the TE signal is programmable in the RFBI_CONFIG register. HSYNC and VSYNC pulses embedded in the TE signal have the same polarity, which is active high for an ORed signal and active low for an ANDed signal. The minimum pulse width of the signal is two RFBI_ICLK clock cycles. Hardware resets the line counter when VSYNC occurs and increments it at every HSYNC. Transfer to the LCD panel begins when the line counter reaches the programmable line number.

10.5.2.2 Transaction Timing Diagrams

Table 10-636 lists the programmable timing fields. Figure 10-165 through Figure 10-167 show timing diagrams of read/write transactions to the LCD panel for the RFBI. In these figures, the polarity 0 (active low) is used to describe the RFBI_A0, RFBI_CSi, RFBI_RE, and RFBI_WE signals.

Table 10-636. Programmable Timing Fields in RFBI Mode

Timing Name	Register Field	Description
CSOnTime	RFBI_ONOFF_TIME[3:0] CSONTIME bit field	CS assertion time from start access time
CSOffTime	RFBI_ONOFF_TIME[9:4] CSOFFTIME bit field	CS deassertion time from start access time
WECycleTime	RFBI_CYCLE_TIME[5:0] WECYCLETIME bit field	The time when A0 becomes valid until write cycle completion
WEOnTime	RFBI_ONOFF_TIME[13:10] WEONTIME bit field	WE assertion delay time from start access time
WEOffTime	RFBI_ONOFF_TIME[19:14] WEOFFTIME bit field	WE deassertion delay time from start access time
RECycleTime	RFBI_CYCLE_TIME[11:6] RECYCLETIME bit field	The time when A0 becomes valid until read cycle completion
REOnTime	RFBI_ONOFF_TIME[23:20] REONTIME bit field	RE assertion delay time from start access time
REOffTime	RFBI_ONOFF_TIME[29:24] REOFFTIME bit field	RE deassertion delay time from start access time
CSPulseWidth	RFBI_CYCLE_TIME[17:12] CSPULSEWIDTH bit field	The time when write cycle time or read cycle time completes

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Figure 10-165. Command Data Write

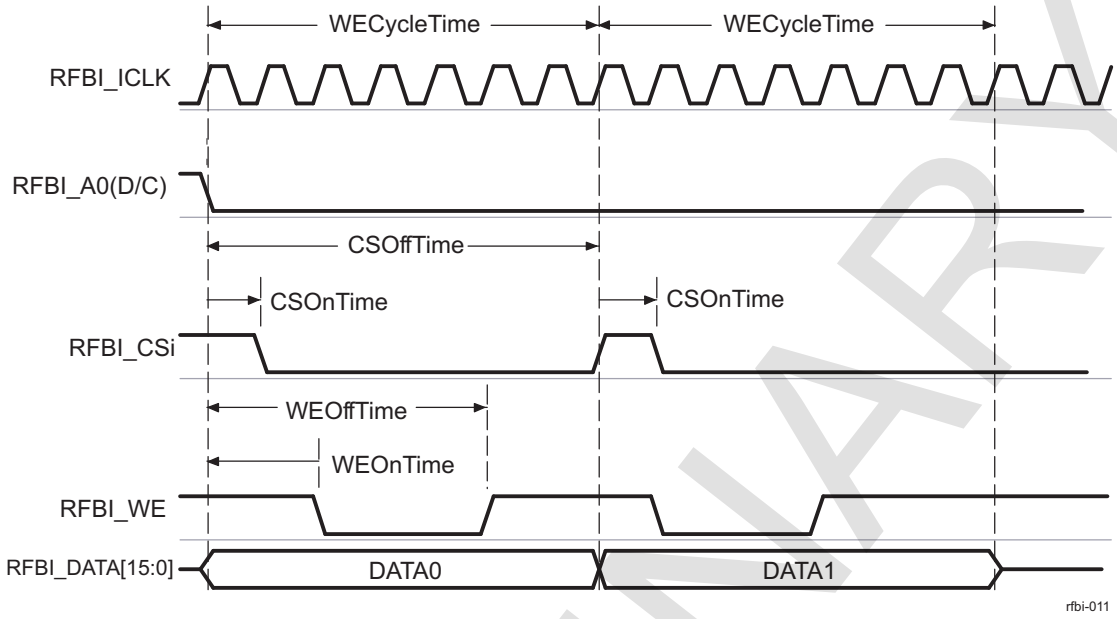

Figure 10-166. Display Data Read

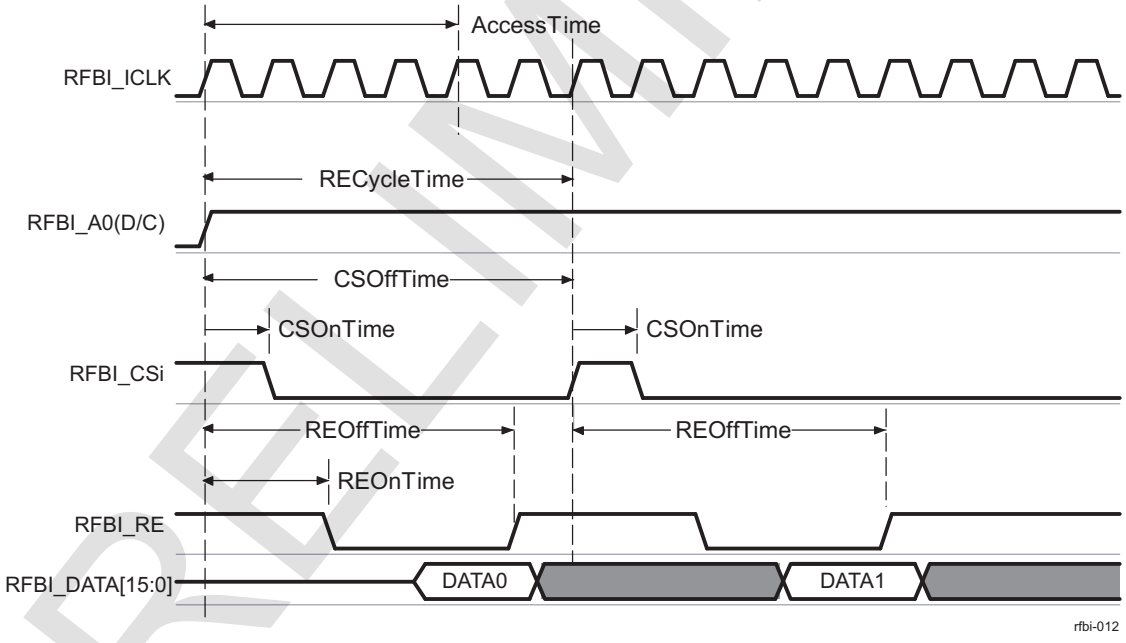

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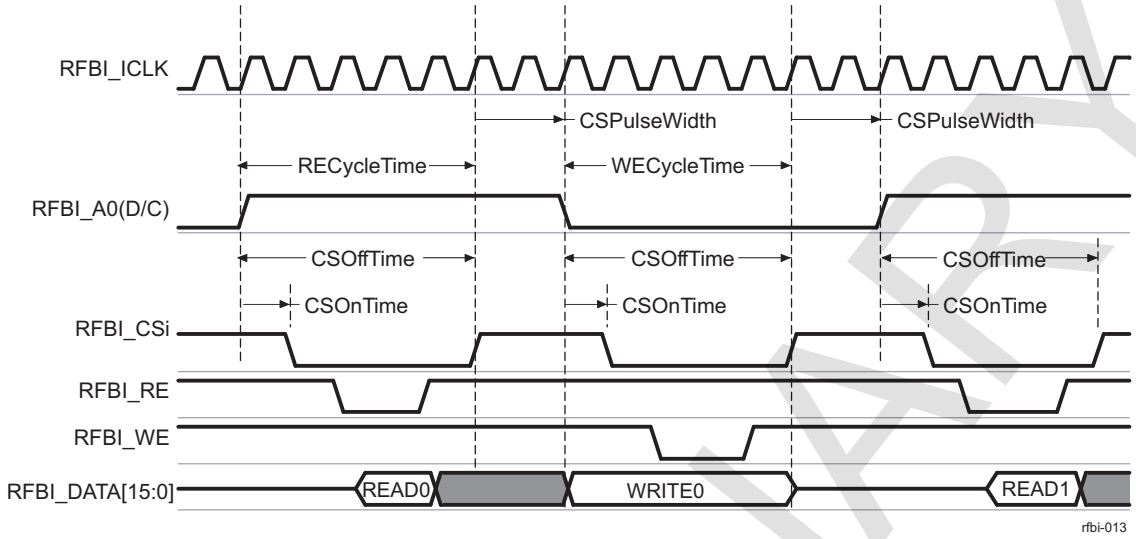
Figure 10-167. Read to Write and Write to Read



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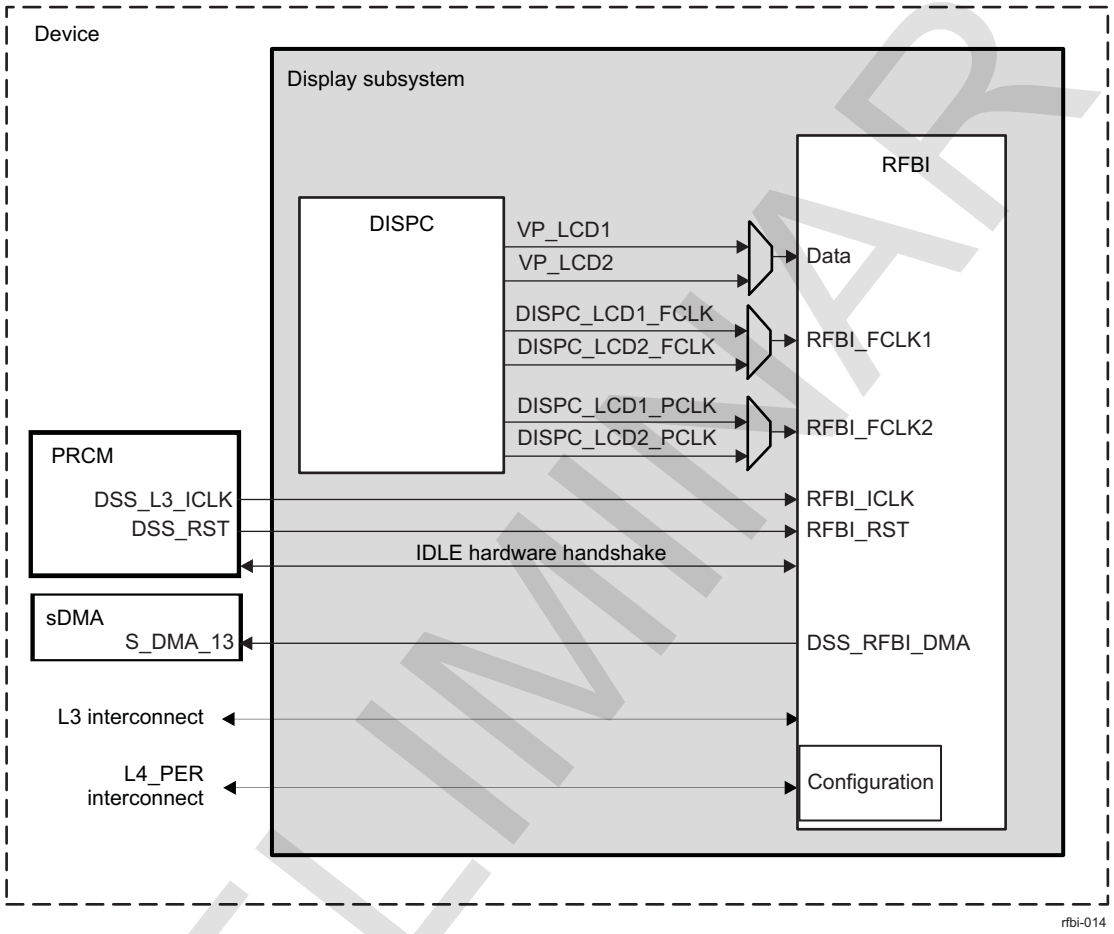
10.5.3 RFBI Integration

This section describes the RFBI integration in the device, including information about clocks, resets, and hardware requests.

Figure 10-168 shows the RFBI module integration.

Figure 10-168. RFBI Integration



NOTE: For more information about the IDLE hardware handshake, see Section 3.1.1.1.2, *Module-Level Clock Management*, Chapter 3, *Power, Reset, and Clock Management*.

Table 10-637 through Table 10-639 summarize the integration of the module in the device.

Table 10-637. Integration Attributes

Module Instance	Attributes		
	Power Domain	Wake-Up Capability	Interconnect
RFBI	PD_DSS	No	L3 L4_PER

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Table 10-638. Clocks and Resets

Clocks				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
RFBI	RFBI_FCLK1	DISPC_LCDx_FCLK	DISPC	Logic clock used by the RFBI when capturing data on the video port and for the generation of the RFBI_STALL signal
	RFBI_FCLK2	DISPC_LCDx_PCLK	DISPC	Pixel clock used by the RFBI to capture the pixels
	RFBI_ICLK	DSS_L3_ICLK	PRCM	L3 interface clock
Resets				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
RFBI	RFBI_RST	DSS_RST	PRCM	Display subsystem global hardware reset

NOTE: If video mode is used, the VPn_PCLK and VPn_CLK clocks must be generated using a CLKIN4DDR clock.

Table 10-639. Hardware Requests

DMA Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
RFBI	DSS_RFBI_DMA	S_DMA_13	sDMA	RFBI DMA request

NOTE: For DMA source description, see Section 10.5.3.1, *DMA Requests*.

10.5.3.1 DMA Requests

All peripherals internal to the device use the transition-sensitive scheme for DMA requests. For more information about the transition-sensitive scheme, see Chapter 16, *sDMA*.

Table 10-640 describes the RFBI DMA request.

Table 10-640. RFBI DMA Request Description

DMA	Source	Description	Sensitivity [1]
RFBI_DMA	DSS_RFBI_DMA	The DMA request can be used to transfer data using the sDMA from memory to RFBI interconnect slave FIFO.	T

(1) T: Transition-sensitive (fixed in hardware) active low request

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10.5.4 RFBI Functional Description

This section describes the functions of the RFBI.

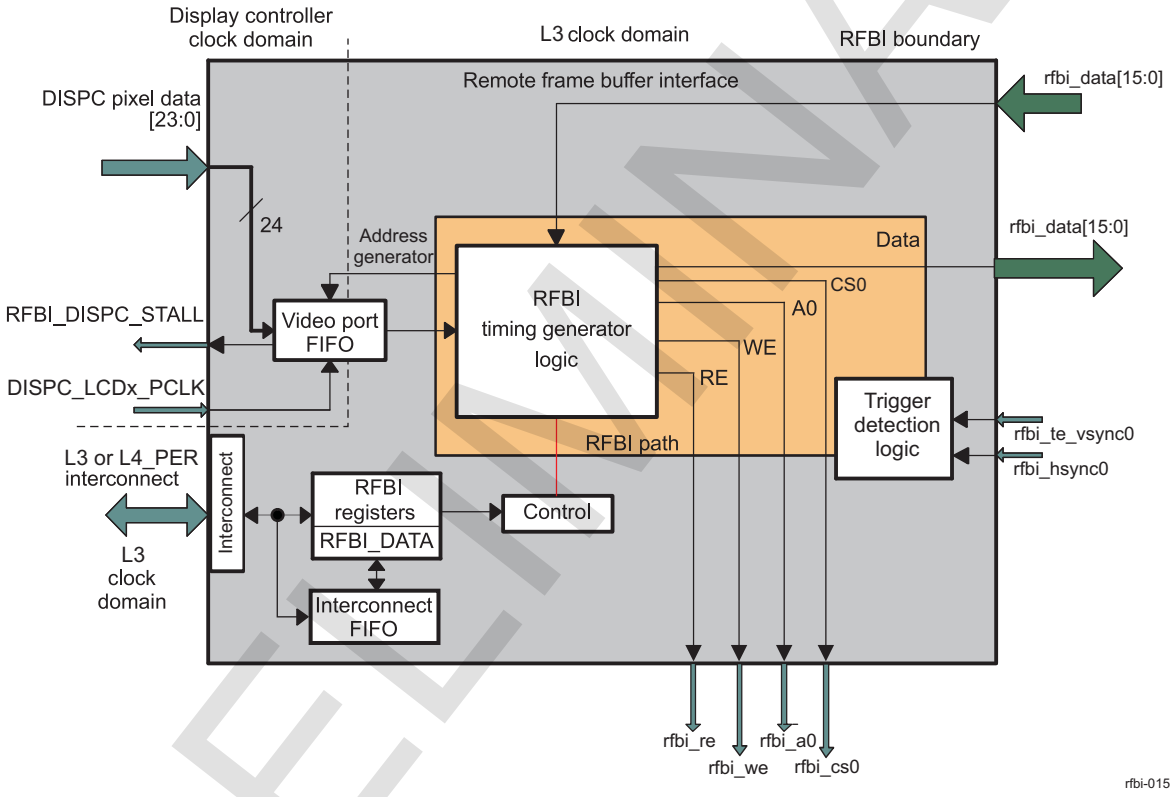
10.5.4.1 Block Diagram

The RFBI can capture the output pixel from the DISPC and send the data to the RFB in the LCD panel. The application configures the RFBI, sends commands, reads data, and configures the DISPC to send data fetched from the system memory by the DISPC DMA engine. The commands/data are sent using an 8-, 9-, or 16-bit parallel interface.

The DISPC is configured to send the data in 12-, 16-, 18-, or 24-BPP format. In the video port FIFO, the encoded pixel values are in an LSB alignment independent of the endianness in system memory.

Figure 10-169 is an overview of the RFBI architecture.

Figure 10-169. RFBI Architecture Overview



10.5.4.2 Clock Configuration

The RFBI functional clocks (RFBI_FCLK1 and RFBI_FCLK2) are provided internally to the display subsystem by the DISPC. For more details about the DISPC clocks, see, Section 10.2 *Display Controller*.

10.5.4.3 Software Reset

To perform a software reset, set the RFBI_SYSCONFIG[1] SOFTRESET bit to 1. The RFBI_SYSSTATUS[0] RESETDONE bit indicates that the software reset is complete when its value is 1. When the software reset completes, the RFBI_SYSCONFIG[1] SOFTRESET bit is automatically reset. Software must ensure that the software reset completes before performing any RFBI operation.

10.5.4.4 Power Management

Table 10-641 describes power-management features available for the RFBI.

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NOTE: For information about source clock gating description, see Section 3.1.1.1.2, *Module-Level Clock Management* in Chapter 3, *Power, Reset and Clock Management*.

Table 10-641. Local Power Management Features

Feature	Registers	Description
Clock autogating	RFBI_SYSCONFIG[0] AUTOIDLE bit	This bit allows a local power optimization inside the module by gating functional clocks (RFBI_FCLK1, RFBI_FCLK2) and interface clock (RFBI_ICLK) upon the internal activity.
Slave idle modes	RFBI_SYSCONFIG[4:3] SIDLEMODE bit field	Force-idle, no-idle, and smart-idle. For more details, see below.
Clock activity	N/A	Feature not available
Master standby modes	N/A	Feature not available
Global wake-up enable	N/A	Feature not available
Wake-up sources enable	N/A	Feature not available

As shown in Table 10-641, the RFBI supports the No-Idle, Force-idle, and Smart-Idle modes.

The conditions of assertion of the SIdleAck signal are:

- No-idle mode: SIdleAck is never asserted.
- Force-idle mode: SIdleAck is asserted unconditionally after one RFBI_ICLK clock cycle delay with respect to assertion of IdleReq.
- Smart-idle mode: SIdleAck is asserted when the following conditions are satisfied:
  - The RFBI stops using the RFBI_ICLK clock and all the data have been sent to the RFB (LCD panel).

Once SIdleAck signal is asserted:

- The RFBI_ICLK (DSS_L3_ICLK) clock can shutdown at any time.
- Any transaction on the RFBI configuration port is ignored

The conditions of deassertion of the SIdleAck signal are:

- Force-idle mode: In this mode SIdleAck is deasserted after one RFBI_ICLK clock cycle delay with respect to deassertion of IdleReq.
- Smart-idle mode: In this mode SIdleAck is deasserted after one RFBI_ICLK clock cycle delay with respect to deassertion of IdleReq.

Once SIdleAck is released, the RFBI is fully operational (guaranteed only in the case of smart-idle mode).

10.5.4.5 Interrupt Requests

The RFBI does not generate interrupts but the following DISPC interrupts can be enabled depending on which LCD output of DISPC is currently used for connection to the RFBI:

- FRAMEDONE1_IRQ
- PROGRAMMEDLINENUMBER_IRQ
- GFXFIFOUNDERFLOW_IRQ
- GFXENDWINDOW_IRQ
- PALETTEGAMMALOADING_IRQ
- OCPERROR_IRQ
- VID1FIFOUNDERFLOW_IRQ
- VID1ENDWINDOW_IRQ
- VID2FIFOUNDERFLOW_IRQ
- VID2ENDWINDOW_IRQ

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- SYNCLOST1_IRQ
- WAKEUP_IRQ
- SYNCLOST2_IRQ
- VID3FIFOUNDERFLOW_IRQ
- VID3ENDWINDOW_IRQ
- FRAMEDONE2_IRQ

NOTE: For more details about DISPC interrupts, see, Section 10.2 *Display Controller*.

The other DISPC interrupts are not used in the RFBI.

10.5.4.6 DMA Requests

Table 10-642 lists event flags and their mask, that can cause RFBI DMA requests.

Table 10-642. DMA Requests Events

DMA Request Name	DMA Request Mask	Map to	Description
DSS_RFBI_DMA	RFBI_CONTROL[7] DISABLE_DMA_REQ	S_DMA_XX	DMA request used to transfer data using the sDMA from memory to the RFBI interconnect FIFO

NOTE: For more details about DMA requests, see Figure 10-175.

10.5.4.7 Video Port FIFO

10.5.4.7.1 Description

The input video port FIFO receives data from the DISPC at the pixel clock. The data in the video port FIFO are read by the RFBI and sent to the LCD panel. The video port FIFO is 24 bits wide and each pixel in 12-, 16-, 18-, and 24-BPP format is stored in the video port FIFO using one 24-bit value aligned on the 24-bit LSB. Section 10.5.4.9, *RFBI Output Parallel Modes*, provides examples of various output configurations based on the interface width (up to 16 bits) and pixel format output (up to 24 bits). Setting the RFBI_CONTROL[1] RFBIMODE bit to 0 directs the MPU to send commands, parameters, and data from the input video port FIFO.

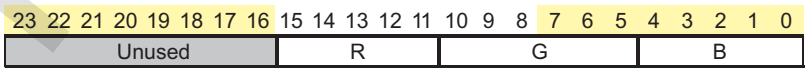
10.5.4.7.2 RFBI Input Formats

The encoded pixel formats supported at the RFBI input interface connected to the DISPC are: RGB12-444, RGB16-565, RGB18-666, and RGB24-888. This input data width is controlled by the RFBI_CONFIG[6:5] DATATYPE bit field. The following graphics describe the bit representation of each format in the video port FIFO. The output of the DISPC is aligned on the LSB of the interface. The pixels are then formatted in accordance with the configuration of the output intercaces (multiple cycles); for more details, see Section 10.5.4.9.1, *Cycle Mode Selection*.

- RGB12-444 format:

rfbi-016

- RGB16-565 format:



rfbi-017

- RGB18-666 format:

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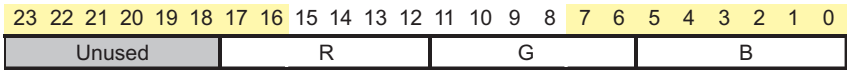
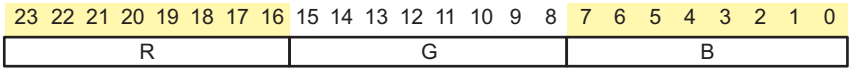


- RGB24-888 format:



NOTE: These pixel formats are also supported when data are provided from the slave port interconnect (for writing parameters).

10.5.4.7.3 Stall Mechanism

The stall signal (RFBI_STALL) is generated by the video port FIFO and used to indicate when the DISPC must stop sending data on the corresponding LCD output interface. This stall signal is used for both LCD outputs (DISPC_LCD1_DATA_STALL and DISPC_LCD2_DATA_STALL) only when the DISPC is configured in stall mode. The stall mode is activated by setting the DISPC_CONTROLo[11] STALLMODE bit to 1 for the primary LCD output and DISPC_CONTROLo[11] STALLMODE bit to 1 for the secondary LCD output.

NOTE: When the DISPC is configured in stall mode, the minimum transfer size is 1 byte.

The RFBI_STALL signal allows the RFBI to reformat the data.

RFBI_STALL is asserted when at least one of the following cases occurs:

- Default status when there is no data to capture from the DISPC
- High FIFO threshold reached
- End of transfer (number of data to output)
- RFBI reset
- RFBI_CONTROL[0] ENABLE bit reset to 0x0

RFBI_STALL is deasserted when the RFBI_CONTROL[0] ENABLE bit is set to 0x1 and at least one of the following cases occurs:

- Low FIFO threshold reached
- External TE occurs and the RFBI_CONFIG[3:2] TRIGGERMODE bit field is set to 0x1 for automatic external trigger (start of the transfer, the FIFO pointers are reset, the FIFO is empty).
- RFBI_CONTROL[4] ITE bit set to 0x1 by users (start of transfer, the FIFO pointers are reset, the FIFO is empty)

NOTE: This stall mechanism is also used by the DSI protocol engines. When multiple modules are connected to the same LCD output (RFBI and DSI protocol engines), the STALL signals from the modules are merged into a single DISPC_LCDx_DATA_STALL signal inside the display subsystem. Only one signal for each LCD output is connected the DISPC (two signals total for the two LCD outputs). In that case, only one module can control the STALL assertion/deassertion. The module which is not using the LCD output interface at that time is not disturbed because the STALL signal is asserted/deasserted by another module. For more details, see chapter *Display Subsystem* .

The RFBI asserts the STALL signal to stop data output by the DISPC. It is deasserted to indicate when new data must be output by the DISPC.

10.5.4.7.3.1 Data Stall Diagram Without DMA Buffer Handshake

Figure 10-170 shows the RFBI data stall diagram when DISPC_DIVISOR[7:0] PCD bit field is set to 3.

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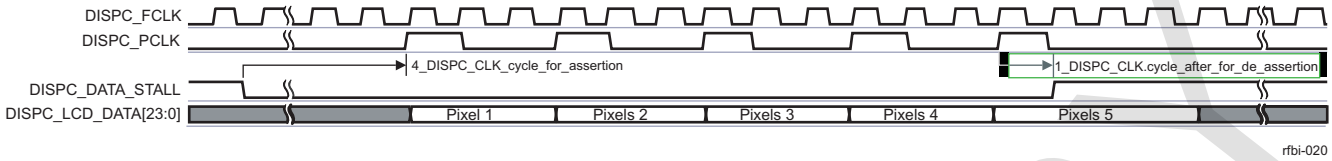
Figure 10-170. RFBI Data Stall Signal Diagram With PCD=3

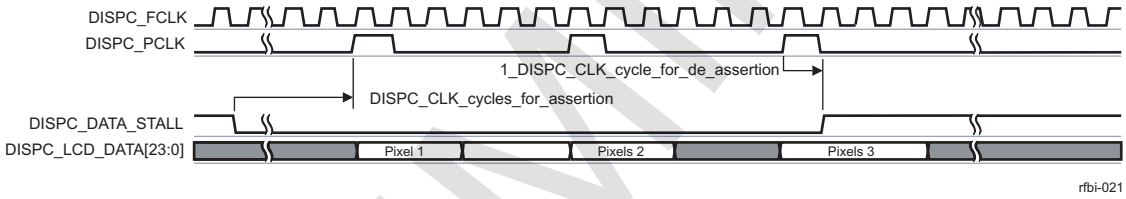


10.5.4.7.3.2 Data Stall Diagram with DMA Buffer Handshake

To avoid underflow of the DMA buffer, the DMA buffer handshake feature can be enabled by setting the DISPC_CONFIGo[16] BUFFERHANDCHECK bit to 1. The fullness of the FIFOs associated with the pipelines used for the LCD output is checked when the STALL signal is inactive before providing data to the pipeline. This prevents emptying the FIFO when the RFBI requests data and there is not enough data in the DISPC DMA buffer. This feature must be enabled only when stall mode is used (DISPC_CONTROLo[11] STALLMODE bit set to 1).

When the DMA buffer handshake feature is activated, the pixel transfer to the RFBI during STALL inactivity period can be stopped (no DISPC_LCD1_PCLK or DISPC_LCD2_PCLK pulse) and restarted when there is enough data in the DMA buffer. The DMA buffer handshake ensures that underflow cannot occur for the pipelines associated with the LCD output in stall mode. Figure 10-171 shows the RFBI data stall with DMA buffer handshake mode activated (PCD=3).

Figure 10-171. RFBI Data Stall Signal Diagram With Handshake With PCD=3



10.5.4.8 Interconnect FIFO

10.5.4.8.1 Description

The interconnect FIFO receives the data from RFBI_DATA write requests to the slave port interconnect slave port. The data in the interconnect FIFO are read by the RFBI and sent to the LCD panel. The interconnect FIFO is 32 bits wide. The size of the interconnect FIFO is 24 words of 32 bits (that is, 24 words of RFBI_DATA). The address of the RFBI_DATA register is used to access the interconnect FIFO. The DSS_RFBI_DMA DMA request can be used to transfer data using the system DMA from memory to interconnect FIFO.

10.5.4.8.2 Using DMA Request With Interconnect FIFO

10.5.4.8.2.1 Threshold for DMA Request Generation

The RFBI_CONTROL[6:5] HIGHTHRESHOLD bit field is used to define the threshold to be used for the generation of the DMA request to receive data into the interconnect FIFO (24 × 32 FIFO depth) through the address of the register RFBI_DATA. The sDMA configuration regarding the size of the burst depends on the value of the RFBI_CONTROL[6:5] HIGHTHRESHOLD bit field. The supported values are 4 × 32, 8 × 32 and 16 × 32. When for example, 4 words of 32 bits are set for the threshold, the sDMA sends a burst of 4 × 32 bits only. The sDMA receives the DMA request and is in charge of providing the correct number of bytes.

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10.5.4.8.2.2 Disabling DMA Request

If the RFBI_CONTROL[7] DISABLE_DMA_REQ bit is reset, the DMA request is generated when there is enough room in the interconnect FIFO to accept the full burst. In case the RFBI receives writes slave port requests to the RFBI_DATA location when the interconnect FIFO is full, the request is not accepted. The RFBI waits for a free entry in the interconnect FIFO to accept the slave port request.

If the RFBI_CONTROL[7] DISABLE_DMA_REQ bit is set, the DMA request is not generated. The threshold value is ignored.

NOTE: Software users can access the RFBI_DATA location without using the DMA request and without programming the high threshold value (backward compatibility mode).

10.5.4.8.2.3 Smart DMA Request Mode

If the RFBI_CONTROL[8] SMART_DMA_REQ bit is reset (smart DMA mode disabled), the DMA request is asserted and deasserted depending on the interconnect FIFO space even if MIdlereq is high in smart-idle/no-idle mode and the entire burst gets error responses from the RFBI. The RFBI waits for a free entry in the interconnect FIFO to accept the burst request.

If the RFBI_CONTROL[8] SMART_DMA_REQ bit is set (smart DMA mode enabled), the DMA request is deasserted after two RFBI_ICLK clock cycles if it has been asserted for more than or equal to two RFBI_ICLK clock cycles and MIdlereq is high in smart-idle or no-idle mode. If asserting time is less than two RFBI_ICLK clock cycles, no more burst requests are accepted even if the space is available in the interconnect FIFO.

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10.5.4.9 RFBI Output Parallel Modes

10.5.4.9.1 Cycle Mode Selection

The RFBI_CONFIG[10:9] CYCLEFORMAT bit field defines the number of cycles to output a pixel. The number of cycles determines the number of registers used to format the data in the interconnect FIFO with the appropriate number of bits (starting from the LSB) and with the alignment on the interface. The data are formatted based on the configuration of the RFBI_DATA_CYCLEi registers.

- One cycle: RFBI_CONFIG[10:9] CYCLEFORMAT bit field = 0x00 and the RFBI_DATA_CYCLE1 register
- Two cycles: RFBI_CONFIG [10:9] CYCLEFORMAT bit field = 0x01 and the RFBI_DATA_CYCLE1 and RFBI_DATA_CYCLE2 registers
- Three cycles: RFBI_CONFIG[10:9] CYCLEFORMAT bit field = 0x10 and the RFBI_DATA_CYCLE1, RFBI_DATA_CYCLE2, and RFBI_DATA_CYCLE3 registers

Figure 10-172 through Figure 10-174 list the bits position of the pixel during the cycles for an 8-, 9- and 16-bit parallel output, respectively.

Figure 10-172. 8-Bit Interface Settings

	24-BPP		
	1st cycle	2nd cycle	3rd cycle
Data[7]	R0[7]	G0[7]	B0[7]
Data[6]	R0[6]	G0[6]	B0[6]
Data[5]	R0[5]	G0[5]	B0[5]
Data[4]	R0[4]	G0[4]	B0[4]
Data[3]	R0[3]	G0[3]	B0[3]
Data[2]	R0[2]	G0[2]	B0[2]
Data[1]	R0[1]	G0[1]	B0[1]
Data[0]	R0[0]	G0[0]	B0[0]

RFBI_CONFIG.CYCLEFORMAT = 0x2
RFBI_DATA_CYCLE1 = 0x00000008
RFBI_DATA_CYCLE2 = 0x00000008
RFBI_DATA_CYCLE3 = 0x00000008

	18-BPP		
	1st cycle	2nd cycle	3rd cycle
Data[7]	R0[5]	G0[3]	x
Data[6]	R0[4]	G0[2]	x
Data[5]	R0[3]	G0[1]	x
Data[4]	R0[2]	G0[0]	x
Data[3]	R0[1]	B0[5]	x
Data[2]	R0[0]	B0[4]	x
Data[1]	G0[5]	B0[3]	B0[1]
Data[0]	G0[4]	B0[2]	B0[0]

RFBI_CONFIG.CYCLEFORMAT = 0x2
RFBI_DATA_CYCLE1 = 0x00000008
RFBI_DATA_CYCLE2 = 0x00000008
RFBI_DATA_CYCLE3 = 0x00000002

	16-BPP	
	1st cycle	2nd cycle
Data[7]	R0[4]	G0[2]
Data[6]	R0[3]	G0[1]
Data[5]	R0[2]	G0[0]
Data[4]	R0[1]	B0[4]
Data[3]	R0[0]	B0[3]
Data[2]	G0[5]	B0[2]
Data[1]	G0[4]	B0[1]
Data[0]	G0[3]	B0[0]

RFBI_CONFIG.CYCLEFORMAT = 0x1
RFBI_DATA_CYCLE1 = 0x00000008
RFBI_DATA_CYCLE2 = 0x00000008

	12-BPP	
	1st cycle	2nd cycle
Data[7]	R0[3]	x
Data[6]	R0[2]	x
Data[5]	R0[1]	x
Data[4]	R0[0]	x
Data[3]	G0[3]	B0[3]
Data[2]	G0[2]	B0[2]
Data[1]	G0[1]	B0[1]
Data[0]	G0[0]	B0[0]

RFBI_CONFIG.CYCLEFORMAT = 0x1
RFBI_DATA_CYCLE1 = 0x00000008
RFBI_DATA_CYCLE2 = 0x00000004

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Figure 10-173. 9-Bit Interface Settings

	24-BPP		
	1st cycle	2nd cycle	3rd cycle
Data[8]	R0[7]	G0[6]	x
Data[7]	R0[6]	G0[5]	x
Data[6]	R0[5]	G0[4]	x
Data[5]	R0[4]	G0[3]	B0[5]
Data[4]	R0[3]	G0[2]	B0[4]
Data[3]	R0[2]	G0[1]	B0[3]
Data[2]	R0[1]	G0[0]	B0[2]
Data[1]	R0[0]	B0[7]	B0[1]
Data[0]	G0[7]	B0[6]	B0[0]

RFBI_CONFIG.CYCLEFORMAT= 0x2
RFBI_DATA_CYCLE1 = 0x00000009
RFBI_DATA_CYCLE2 = 0x00000009
RFBI_DATA_CYCLE3 = 0x00000006

	18-BPP	
	1st cycle	2nd cycle
Data[8]	R0[5]	G0[2]
Data[7]	R0[4]	G0[1]
Data[6]	R0[3]	G0[0]
Data[5]	R0[2]	B0[5]
Data[4]	R0[1]	B0[4]
Data[3]	R0[0]	B0[3]
Data[2]	G0[5]	B0[2]
Data[1]	G0[4]	B0[1]
Data[0]	G0[3]	B0[0]

RFBI_CONFIG.CYCLEFORMAT = 0x1
RFBI_DATA_CYCLE1 = 0x0000000912
RFBI_DATA_CYCLE2 = 0x00000009

	16-BPP	
	1st cycle	2nd cycle
Data[8]	R0[4]	x
Data[7]	R0[3]	x
Data[6]	R0[2]	G0[1]
Data[5]	R0[1]	G0[0]
Data[4]	R0[0]	B0[4]
Data[3]	G0[5]	B0[3]
Data[2]	G0[4]	B0[2]
Data[1]	G0[3]	B0[1]
Data[0]	G0[2]	B0[0]

RFBI_CONFIG.CYCLEFORMAT = 0x1
RFBI_DATA_CYCLE1 = 0x00000009
RFBI_DATA_CYCLE2 = 0x00000007

	12-BPP	
	1st cycle	2nd cycle
Data[8]	R0[3]	x
Data[7]	R0[2]	x
Data[6]	R0[1]	x
Data[5]	R0[0]	x
Data[4]	G0[3]	x
Data[3]	G0[2]	x
Data[2]	G0[1]	B0[2]
Data[1]	G0[0]	B0[1]
Data[0]	B0[3]	B0[0]

RFBI_CONFIG.CYCLEFORMAT = 0x1
RFBI_DATA_CYCLE1 = 0x00000009
RFBI_DATA_CYCLE2 = 0x00000003

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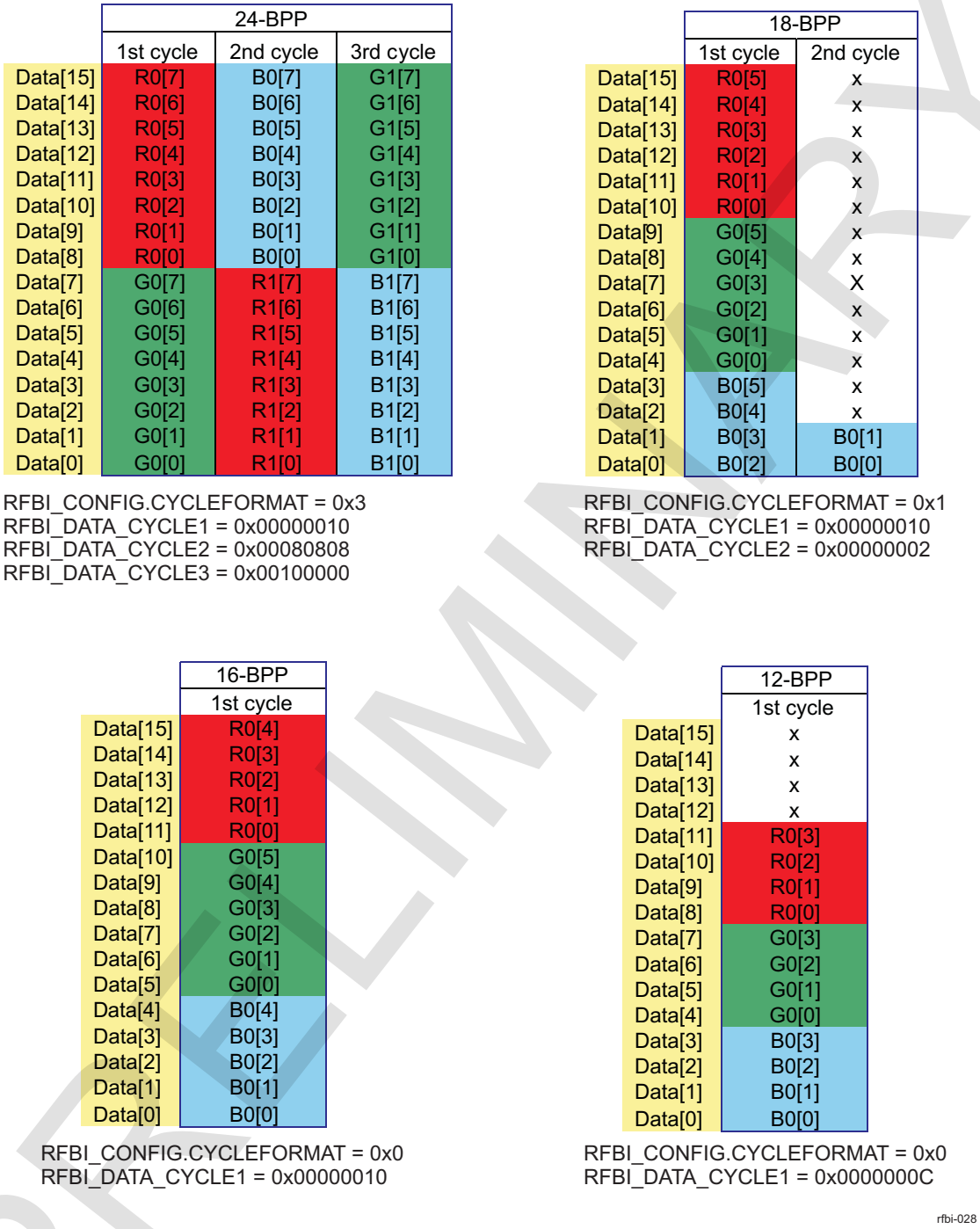
Figure 10-174. 16-Bit Interface Settings



10.5.4.9.2 Unmodified Bits

In a cycle, if every bit in the interface does not have a pixel value, the status of the unused bits can be programmed to be 0, 1, or the previous value (I/O power consumption optimization). Based on the configuration, the undefined bits for each cycle are defined with the previous values of the bits at the same position in the previous cycle, 0s, or 1s (the unused bits can be at any position). The RFBI_CONFIG[12:11] UNUSEDBITS bit field is used.

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10.5.4.9.3 Number of Pixels to Transfer

The RFBI_PIXEL_CNT[31:0] PIXELCNT bit field indicates the number of pixels to be transferred to the LCD panel. The value can be changed only when the RFBI_CONTROL[0] ENABLE bit is reset.

During the transfer, the hardware decrements the register when a pixel is sent to the RFB. When the RFBI_CONTROL[0] ENABLE bit is set and a new value is written in the RFBI_PIXEL_CNT register, and the current value in the register is a not 0 (the remaining number of pixels to transfer), the ongoing transfer is aborted.

10.5.4.10 RFBI Timing Generator

10.5.4.10.1 Configuration Selection

The RFBI_CONTROL[3:2] CONFIGSELECT bit field selects the chip select.

10.5.4.10.2 Read/Write

Depending on the status of A0, WE, and RE, the commands and display/parameter data are written to the panel (handled by the state-machine for the commands/parameter data and stored in memory for the display data), or the display data/status values are read from the LCD panel (status and display data in the LCD panel memory). The polarity of A0 (RFBI_A0 signal), WE (RFBI_WE signal), RE (RFBI_RE signal), and CS0 (RFBI_CS0 signal) is programmable.

Table 10-643 describes the read/write function.

Table 10-643. Read/Write Function Description

A0 (RFBI_A0)	WE (RFBI_WE)	RE (RFBI_RE)	Function Description
1	0	1	Display data write, parameter data write
1	1	0	Display data read
0	1	0	Status read
0	0	1	Command data write

A minimum of RFBI_Cs cycle time, as defined in Table 10-644, is required to keep the RFBI_CS0 signal asserted between write transfers of multiple pixels.

Table 10-644 lists the minimum cycle time for RFBI_CS0, depending on the source of pixels (DISPC or slave port) and the cycle format (1pixel/cycle, 1 pixel/2 cycles, or 1 pixel/3 cycles).

Table 10-644. Minimum Cycle Time for CS0/WE Always Asserted

RFBI Performance	RFBI_CONFIG[10:9] CYCLEFORMAT	RFBI_CONFIG[8:7] PORTFORMAT	Minimum Cycle Time (in Number of RFBI_ICLK Clock Cycles)
Slave port interconnect	1 pixel/cycle	1 pixel	5
	1 pixel/2 cycles	1 pixel	4
	1 pixel/3 cycles	1 pixel	4
	1 pixel/cycle	2 pixels	4
	1 pixel/2 cycles	2 pixels	4
	1 pixel/3 cycles	2 pixels	4
DISPC	1 pixel/cycle	N/A	4
	1 pixel/2 cycles	N/A	3
	1 pixel/3 cycles	N/A	3
	2 pixel/3 cycles	N/A	6

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10.5.4.10.3 RFBI State-Machine

The RFBI_A0, RFBI_RE, and RFBI_WE signals are asserted and deasserted based on the register accessed (RFBI_CMD, RFBI_PARAM, RFBI_DATA, RFBI_READ, or RFBI_STATUS). (See Table 10-643.) When the RFBI_SYSSTATUS[8] BUSY bit is set by hardware, any access to the registers is stalled, except for the RFBI_DATA register.

The RFBI_SYSSTATUS[9] BUSYRFBIDATA bit indicates whether there are still pending data in the interconnect FIFO associated with the RFBI_DATA register only.

- Command register

  Write one command at a time by writing through the slave port interconnect into the RFBI_CMD register. If the previous command is not processed, the RFBI_SYSSTATUS[8] BUSY bit is set by hardware and the access to writing a new command is stalled.

- Parameter register

  Write one parameter at a time by writing in the RFBI_PARAM register.

  If the previous parameter is not processed, the RFBI_SYSSTATUS[8] BUSY bit is set by hardware and the access to writing a new parameter is stalled.

- Data register

  Write one or two pixels at a time by writing in the RFBI_DATA register.

  The pixels are formatted based on the specified cycle format. If two pixels are written into the 32-data register, the RFBI_CONFIG[8:7] PORTFORMAT bit field indicates the number of pixels for each slave port access to the register and the order of the pixels.

  If the previous data are not processed, the RFBI_SYSSTATUS[8] BUSY bit is set by hardware and any access for writing new data is stalled. When the RFBI_SYSSTATUS[8] BUSY bit is reset by hardware, the access is not stalled.

- Read/status register

  Send through the command and parameter registers the correct information to receive data in the data or status register. The read data from the LCD panel is initiated by writing into the RFBI_READ or RFBI_STATUS registers. In this case, the RFBI_SYSSTATUS[8] BUSY bit is set until the data are available in the register.

  When the RFBI_SYSSTATUS[8] BUSY bit is set by hardware, the read or write access is stalled until the register is updated with a new value from the LCD panel. To avoid the stall, the software can poll the RFBI_SYSSTATUS[8] BUSY bit until it is reset by hardware. To receive the data, send the appropriate command/parameters.

10.5.4.10.4 RFBI Timings

The timing registers can be accessed only when there is no transaction in progress (based on the value of the RFBI_CONTROL[3:2] CONFIGSELECT bit field). Granularity is defined using the RFBI_CONFIG[4] TIMEGRANULARITY bit. This feature allows the extension of programmable ranges of timing parameters for the RFBI interface. See Table 10-645 for the configuration values of the timing bits.

- Chip-select assertion/deassertion time (CSOnTime/CSOffTime)

  RFBI_A0 setup time to chip-select assertion is assured by the programmable chip-select assertion time from the start access time:
  RFBI_ONOFF_TIME[3:0] CSONTIME bit field.

  The chip-select deassertion time from the start access time is programmable:
  RFBI_ONOFF_TIME[9:4] CSOFFTIME bit field

CAUTION

Configuring RFBI_ONOFF_TIME[3:0] CSONTIME = RFBI_ONOFF_TIME[9:4] CSOFFTIME = 0 is not supported and must be avoided. This configuration creates contention on the bus and progressively damages the LCD panel.

- Chip-select pulse width (CSPulseWidth)

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The total chip-select pulse width is the time when write cycle time or read cycle time has completed and is programmable:
RFBI_CYCLE_TIME[17:12] CSPULSEWIDTH bit field

It applies on the read-to-write, write-to-read, read-to-read, and write-to-write access based on:

– The RFBI_CYCLE_TIME[19] RRENABLE bit: Read-to-read access
– The RFBI_CYCLE_TIME[20] WWENABLE bit: Write-to-write access
– The RFBI_CYCLE_TIME[18] RWENABLE bit: Read-to-write access
– The RFBI_CYCLE_TIME[21] WRENABLE bit: Write-to-read access

By default, it applies to any access (read-to-read, read-to-write, write-to-read, write-to-write) when the chip-select CS0 is activated by setting the RFBI_CONTROL[3:2] CONFIGSELECT bit field to 0x1.

- Access time

  Access time is the time delay between A0 assertion to data sampling before RE signal deassertion; access time is programmable:
  RFBI_CYCLE_TIME[27:22] ACCESSTIME bit field

  When reading the data on the bus, the data are sampled at the end of the access time, which occurs before the end of the read off time (RFBI_ONOFF_TIME[29:24] REOFFTIME).

- Write-enable cycle time (WECycleTime)

  The total write-enable cycle time is the time when A0 becomes valid until write cycle completion; the write-enable cycle time is programmable:
  The RFBI_CYCLE_TIME[5:0] WECYCLETIME bit field

- Write-enable assertion/deassertion time (WEOnTime/WEOffTime)

  The WE assertion delay time from start access time is programmable:
  RFBI_ONOFF_TIME[13:10] WEONTIME bit field

  The WE deassertion delay time from the start access time is programmable:
  RFBI_ONOFF_TIME[19:14] WEOFFTIME bit field

- Read-enable cycle time (RECycleTime)

  The total read-enable cycle time is the time when A0 becomes valid until read cycle completion; the read-enable cycle time is programmable:
  The RFBI_CYCLE_TIME[11:6] RECYCLETIME bit field

- Read-enable assertion/deassertion time (REOnTime/REOffTime)

  The RE assertion delay time from the start access time is programmable:
  RFBI_ONOFF_TIME[23:20] REONTIME bit field

  The RE deassertion delay time from the start access time is programmable:
  RFBI_ONOFF_TIME[29:24] REOFFTIME bit field

At cycle time completion (read access or write access), all control signals (RFBI_CS0, RFBI_WE, and RFBI_RE) are deasserted regardless of their deassertion time parameter values, if they are not deasserted already.

However, an exception to this forced deassertion exists when a pipelined request to CS0 is pending. Also, a control signal with deassertion time parameters equal to the cycle time parameter is not necessarily deasserted when a pipelined request to the same chip-select or different chip-select is pending. This prevents any unnecessary glitch transitions.

If no inactive cycles are required between successive accesses to the same chip-select (the RFBI_CYCLE_TIME[17:12] CSPULSEWIDTH bit field = 0), and if assertion time parameters associated with the following access equal 0, the asserted control signals (RFBI_CS0, RFBI_WE, and RFBI_RE) stay asserted. This applies only to write-to-write access combination. In case of read-to-write, read-to-read, or write-to-read sequences, the RFBI_CS0, RFBI_WE, and RFBI_RE signals are always deasserted.

Table 10-645 lists the configuration values for each timing bit.

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Table 10-645. RFBI Timings Configuration

Timing Configuration Bits	Granularity (1)	
	One	Two
RFBI_ONOFF_TIME[3:0] CSONTIME	0 to 15	0 to 30
RFBI_ONOFF_TIME[9:4] CSOFFTIME	0 to 63	0 to 126
RFBI_CYCLE_TIME[17:12] CSPULSEWIDTH	0 to 63	0 to 126
RFBI_CYCLE_TIME[27:22] ACCESSTIME	0 to 63	0 to 126
RFBI_CYCLE_TIME[5:0] WECYCLETIME	0 to 63	0 to 126
RFBI_ONOFF_TIME[13:10] WEONTIME	0 to 15	0 to 30
RFBI_ONOFF_TIME[19:14] WEOFFTIME	0 to 63	0 to 126
RFBI_CYCLE_TIME[11:6] RECYCLETIME	0 to 63	0 to 126
RFBI_ONOFF_TIME[23:20] REONTIME	0 to 15	0 to 30
RFBI_ONOFF_TIME[29:24] REOFFTIME	0 to 63	0 to 126

(1) Number of RFBI_ICLK clock cycles. The granularity can be configured using the RFBI_CONFIG[4] TIMEGRANULARITY bit.

10.5.4.11 Trigger Detection Logic

10.5.4.11.1 Trigger Mode

Setting the RFBI_CONFIG[3:2] TRIGGERMODE bit field configures the different trigger modes:

- Internal trigger mode with the internal programmable RFBI_CONTROL[4] ITE bit
- External trigger mode with external TE signal (RFBI_TE_VSYNC)
- External trigger mode with external VSYNC/HSYNC signals

10.5.4.11.2 Internal Trigger Mode

10.5.4.11.2.1 ITE Bit

Set the RFBI_CONTROL[4] ITE bit to start capturing the data from the DISPC. The DISPC must be configured in the RFBI mode to account for the RFBI_DISPC_STALL signal. Setting the trigger mode to external (RFBI_CONFIG[3:2] TRIGGERMODE bit field set to 0x1 or 0x2) causes the RFBI_CONTROL[4] ITE bit to be ignored. The chip-select CS0 must be selected (RFBI_CONTROL[3:2] CONFIGSELECT set to 0x1) when this bit is set by users.

10.5.4.11.3 External Trigger Mode

There are two external trigger modes:

- TE only: VSYNC and HSYNC are merged by logical OR operation, and are detected through VSYNC and HSYNC pulse widths.
- HSYNC/VSYNC: This mode uses the two external signals which are detected through VSYNC and HSYNC pulse widths.

10.5.4.11.3.1 Programmable Line Number

When the trigger mode is set to external trigger mode with HSYNC and VSYNC or the TE, hardware resets the line counter when the VSYNC occurs and, after a programmable number of lines programmed by the user in the RFBI_LINE_NUMBER[10:0] LINENUMBER bit field (the HSYNC pulse occurs for every line), the transfer to the LCD panel begins. When the programmable line number is 0, only the VSYNC pulse indicates the beginning of the transfer in both modes: HSYNC/VSYNC and TE (logical OR operation between HSYNC and VSYNC).

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10.5.4.11.3.2 VSYNC Pulse Width (Minimum Value)

The RFBI_VSYNC_WIDTH[15:0] MINVSYNCPULSEWIDTH bit field defines the minimum number of RFBI_ICLK clock cycles of the VSYNC pulse for detection on VSYNC. It allows differentiation between VSYNC and HSYNC, which are ORed on the same signal, and is also used in HSYNC/VSYNC mode on the two separate input lines.

- The VSYNC pulse width must be equal to at least two RFBI_ICLK clock cycles when HSYNC is not present (TE trigger mode only).
- The VSYNC pulse width must be equal to at least four RFBI_ICLK clock cycles when HSYNC is present (TE trigger mode only).

10.5.4.11.3.3 HSYNC Pulse Width (Minimum Value)

The RFBI_HSYNC_WIDTH[15:0] MINHSYNCPULSEWIDTH bit field defines the minimum number of RFBI_ICLK clock cycles of the HSYNC pulse for detection on HSYNC. It allows differentiation between VSYNC and HSYNC, which are ORed on the same signal, and is also used in VSYNC/HSYNC mode on the separate two input lines. To be detected, the HSYNC/VSYNC pulse width must always be equal to at least two RFBI_ICLK clock cycles. See Table 10-646.

Table 10-646. Minimum Pulse Width (HSYNC/VSYNC)

Configuration Bits	TE Mode	HSYNC/VSYNC Mode
RFBI_HSYNC_WIDTH[15:0] MINHSYNCPULSEWIDTH field value	2	2
RFBI_VSYNC_WIDTH[15:0] MINVSYNCPULSEWIDTH field value	4	2

The pulse received by the RFBI must be at least two RFBI_ICLK clock cycles to be detected. In case of TE mode, since the minimum value for differentiate VSYNC and HSYNC is two RFBI_ICLK clock cycles, the VSYNC pulse width must be at least four RFBI_ICLK clock cycles and the HSYNC pulse width must be at least two RFBI_ICLK clock cycles

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10.5.5 RFBI Programming Guide

10.5.5.1 RFBI Low-Level Programming Models

This section covers the low-level hardware programming sequences for configuration and use of the RFBI.

10.5.5.1.1 Global Initialization

10.5.5.1.1.1 Surrounding Modules Global Initialization

This section identifies the requirements of initializing the surrounding modules when the RFBI is to be used for the first time after a device reset. This initialization of surrounding modules is based on the integration and environment of the RFBI. For more information, see Section 10.5.2, *RFBI Environment*, and Section 10.5.3, *RFBI Integraton*.

Table 10-647 describes the global initialization of surrounding modules.

Table 10-647. Global Initialization of Surrounding Modules

Surrounding Modules	Comments
PRCM	RFBI_ICLK interface clock must be enabled. See Chapter 3, *Power, Reset, and Clock Management.*
DISPC	RFBI_FCLK1 and RFBI_FCLK2 functional clocks must be enabled. See , *Display Controller*.
Control module	rfbi_re pad muxing must be set in the SYSCTRL_PADCONF_CORE module. rfbi_we pad muxing must be set in the SYSCTRL_PADCONF_CORE module. rfbi_cs0 pad muxing must be set in the SYSCTRL_PADCONF_CORE module. rfbi_te_vsync0 pad muxing must be set in the SYSCTRL_PADCONF_CORE module. rfbi_data[15:0] pads muxing must be set in the SYSCTRL_PADCONF_CORE module. rfbi_hsync0 pad muxing must be set in the SYSCTRL_PADCONF_CORE module. rfbi_a0 pad muxing must be set in the SYSCTRL_PADCONF_CORE module. See Chapter 18, *Control Module*.
MPU INTC	MPU interrupt controller configuration must be done to enable the interrupts from the DISPC module. See Chapter 17, *Interrupt Controllers*.
sDMA	DMA configuration must be done to enable the RFBI module DMA channel requests. See Chapter 16, *Direct Memory Access*.
Interconnect	See Chapter 13, *Interconnect*, for more information about the interconnect configuration.

NOTE: The MPU INTC and the sDMA configurations are necessary if the interrupt- and DMA-based communication modes are used.

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10.5.5.1.1.2 RFBI Global Initialization

10.5.5.1.1.2.1 Main Sequence RFBI Global Initialization

This procedure initializes the RFB and DISPC after a power on or software reset. See Table 10-648.

Table 10-648. RFBI Global Initialization

Step	Register/Bit Field Programming Model	Value
DISPC configuration in RFBI mode	See Section 10.5.5.1.1.2.2, *Subsequence: DISPC Configuration*.	
RFBI configuration	See Section 10.5.5.1.1.2.3, *Subsequence: RFBI Configuration.*	
LCD panel configuration	See Section 10.5.5.1.1.2.4, *Subsequence: LCD Panel Configuration*.	

10.5.5.1.1.2.2 Subsequence: DISPC Configuration

This procedure configures the DISPC registers in RFBI mode. See Table 10-649.

Table 10-649. DISPC Configuration in RFBI Mode

Step	Register/Bit Field Programming Model	Value
DISPC pipeline configuration	Configuration of the pipeline associated to the LCD output (DMA engine, pipelines associated to the LCD output, etc.). See Section 10.2.4, *Display Controller Functional Description*	
Enable TFT mode.	DISPC_CONTROLo[3] STNTFT	0x1
Program the DISPC in RFBI mode.	DISPC_CONTROLo[11] STALLMODE	0x1
Reset the DISPC signal configuration to default value.	DISPC_POL_FREQo	0x00
Select the RFBI data path.	DISPC_CONTROL1[16:15] GPOUT	0x1
Enable the hardware handshake to avoid the DISPC FIFO underflow (applies to the pipeline connected to the LCD output).	DISPC_CONFIGo[16] BUFFERHANDCHECK	0x1

NOTE: In RFBI mode, the DISPC_CONTROLo[5] GOLCD bit must not be set to 1. It must be disabled before resetting the DISPC_CONTROLo[11] STALLMODE bit to 0.

The hardware handshake applies to the pipelines connected to the LCD output. It must be disabled before resetting the DISPC_CONTROLo[11] STALLMODE bit to 0.

10.5.5.1.1.2.3 Subsequence: RFBI Configuration

This procedure configures the RFBI registers. See Table 10-650.

CAUTION

The RFBI configuration registers for CS0 configuration can be accessed only when the configuration is not in use (that is, when the RFBI_CONTROL[3:2] CONFIGSELECT is set to 0x0).

Table 10-650. RFBI Configuration – Main Sequence

Step	Register/Bit Field Programming Model	Value
Enable the RFBI data path.	RFBI_CONTROL[1] RFBIMODE	0x0
DMA mode configuration	See Section 10.5.5.1.1.2.3.1, *Subsequence: DMA Mode Configuration.*	

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Table 10-650. RFBI Configuration – Main Sequence (continued)

Step	Register/Bit Field Programming Model	Value
Disable the chip-select and configuration (this step is necessary to configure the timing registers).	RFBI_CONTROL[3:2] CONFIGSELECT	0x0
Timing and polarity signals configuration	See Section 10.5.5.1.1.2.3.2, *Subsequence: Timing and Polarity Signals Configuration*.	
Configure the parallel input data width.	RFBI_CONFIG[6:5] DATATYPE	x(1)
Configure the number of cycles.	RFBI_CONFIG[10:9] CYCLEFORMAT	x(1)
Trigger mode settings	See Section 10.5.5.1.1.2.3.3, *Subsequence: Trigger Mode Settings*.	
Program the data format per cycle.	RFBI_DATA_CYCLE_1	xxx(1)
	RFBI_DATA_CYCLE_2	xxx(1)
	RFBI_DATA_CYCLE_3	xxx(1)
Select the configuration of CS0	RFBI_CONTROL[3:2] CONFIGSELECT	0x1

(1) Values depend on the application

10.5.5.1.1.2.3.1 Subsequence: DMA Mode Configuration

Figure 10-175 shows DMA mode configuration.

Figure 10-175. DMA Mode Configuration

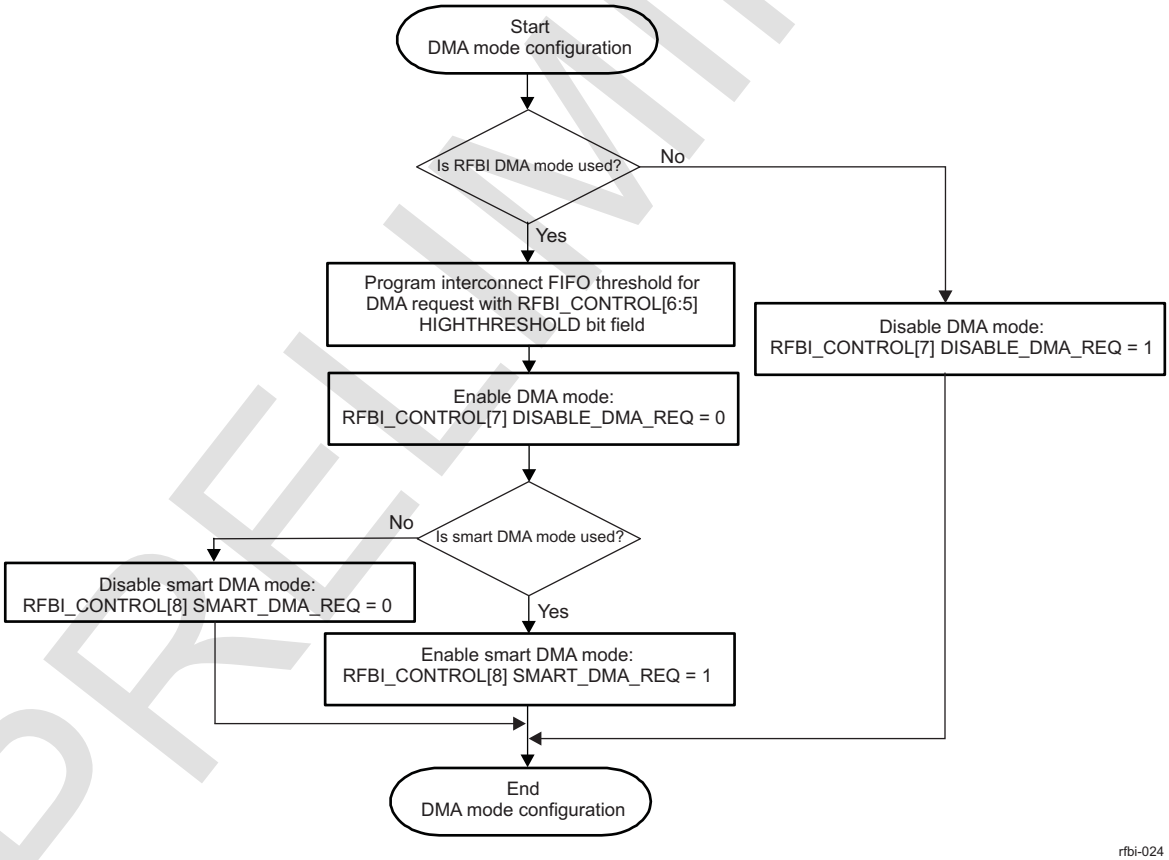

Table 10-651 describes DMA mode configuration.

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Table 10-651. Register Call Summary for Subsequence: DMA Mode Configuration

Register Name
RFBI_CONTROL

10.5.5.1.1.2.3.2 Subsequence: Timing and Polarity Signals Configuration

Table 10-652 describes timing and polarity signals configuration.

Table 10-652. Timing and Polarity Signals Configuration

Step	Register/Bit Field Programming Model	Value
Program ON/OFF timings.	RFBI_ONOFF_TIME	xxx(1)
Program cycle timings.	RFBI_CYCLE_TIME	xxx(1)
Program CS polarity.	RFBI_CONFIG[19] CSPOLARITY	x(1)
Program WE polarity.	RFBI_CONFIG[18] WEPOLARITY	x(1)
Program RE polarity.	RFBI_CONFIG[17] REPOLARITY	x(1)
Program A0 polarity.	RFBI_CONFIG[16] A0POLARITY	x(1)
Program unused bits.	RFBI_CONFIG[12:11] UNUSEDBITS	x(1)
Program the factor x2 latency.	RFBI_CONFIG[4] TIMEGRANULARITY	x(1)

(1) Values depend on the application.

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10.5.5.1.1.2.3.3 Subsequence: Trigger Mode Settings

Figure 10-176 shows trigger mode settings.

Figure 10-176. Trigger Mode Settings

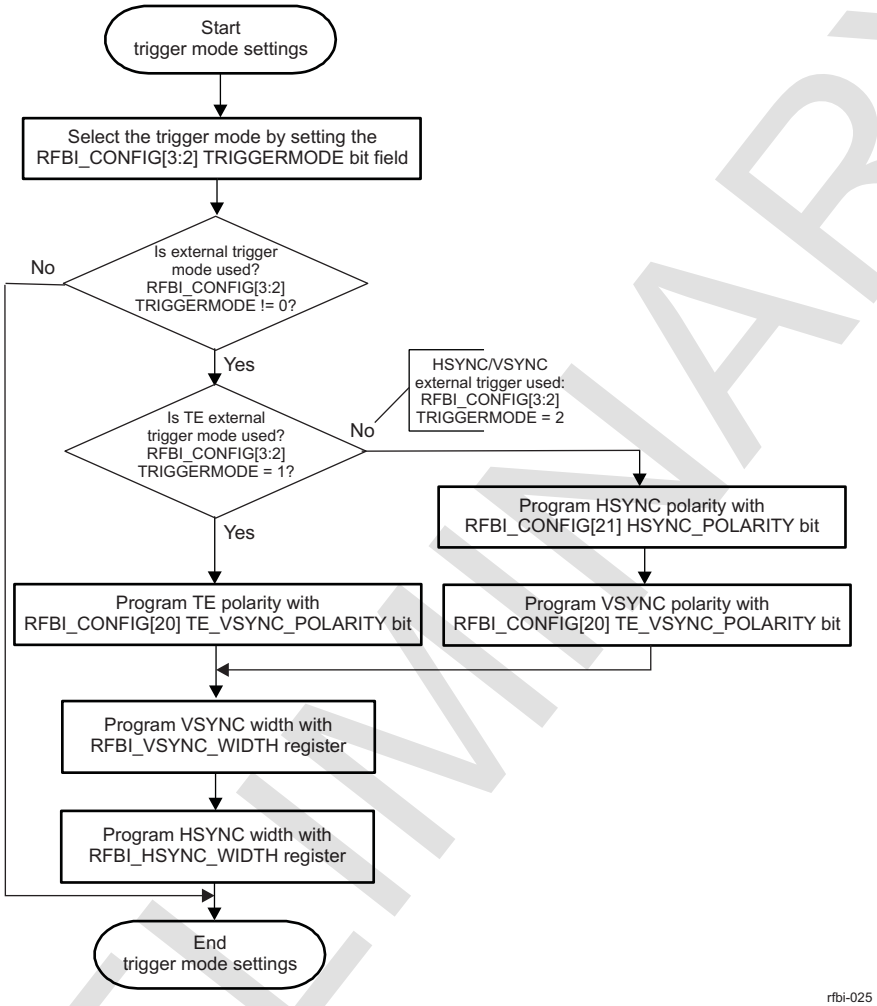

Table 10-653 describes register call summary for subsequence: trigger mode settings

Table 10-653. Register Call Summary for Subsequence: Trigger Mode Settings

Register Name		
RFBI_CONFIG	RFBI_VSYNC_WIDTH	RFBI_HSYNC_WIDTH

10.5.5.1.1.2.4 Subsequence: LCD Panel Configuration

This procedure consists of sending and receiving commands. See Table 10-654 and Table 10-655.

Table 10-654. RFBI Command Interface: Writing Command to the LCD Panel

Step	Register/Bit Field Programming Model	Value
Write command to the LCD panel.	RFBI_CMD[8:0] CMD	0x(1)
Wait until BUSY != 1.	RFBI_SYSSTATUS[8] BUSY	

(1) Value depends on the command sent to the LCD panel.

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Table 10-655. RFBI Command Interface: Reading Command From the LCD Panel

Step	Register/Bit Field Programming Model	Value
Initialize reading command.	RFBI_STATUS[8:0] STATUS	0x
Initialize reading command.	RFBI_READ [8:0] READ	0x
Wait until BUSY != 1.	RFBI_SYSSTATUS[8] BUSY	
Read command from the LCD panel.	RFBI_STATUS[8:0] STATUS	0x(1)
	RFBI_READ [8:0] READ	0x(1)

(1) Value depends on the command read from the LCD panel.

10.5.5.1.2 Operational Modes Configuration

10.5.5.1.2.1 RFBI Start Transfer

10.5.5.1.2.1.1 Main Sequence: RFBI Start Transfer With Polling Method

Table 10-656 describes the RFBI start transfer polling method.

Table 10-656. RFBI Start Transfer With Polling Method

Step	Register/Bit Field Programming Model	Value
Enable DISPC module output.	See Section 10.5.5.1.2.1.4, *Subsequence: DISPC Output Enable.*	
Enable RFBI module output.	See Section 10.5.5.1.2.1.5, *Subsequence: RFBI Interrupts Enable.*	
Detect event.	See Table 10-662.	

10.5.5.1.2.1.2 Main Sequence: RFBI Start Transfer With Interrupts and DMA Method

Table 10-657 describes the RFBI start transfer interrupts method.

Table 10-657. RFBI Start Transfer With Interrupts Method

Step	Register/Bit Field Programming Model	Value
Enable DISPC interrupts.	See Table 10-658.	
Enable DISPC module output.	See Section 10.5.5.1.2.1.4, *Subsequence: DISPC Output Enable.*	
Enable RFBI module output.	See Section 10.5.5.1.2.1.5, *RFBI Interrupts Enable*.	
Detect Event.	See Table 10-662.	

10.5.5.1.2.1.3 Subsequence: DISPC Interrupts Enable

This procedure enables the DISPC interrupts used in RFBI mode. See Table 10-658.

Table 10-658. DISPC Interrupts Enable

Step	Register/Bit Field Programming Model	Value
Clears all interrupts	DISPC_IRQSTATUS	0xFFFF
Enable the FRAMEDONEi IRQ.	DISPC_IRQENABLE FRAMEDONEi_EN	0x1
Enable the BUFFERUNDERFLOW IRQ.	DISPC_IRQENABLE BUFFERUNDERFLOW_EN	0x1
Enable the SYNCLOSTi IRQ.	DISPC_IRQENABLE SYNCLOSTi_EN	0x1

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NOTE: The other interrupts requests (see Section 10.5.4.5, *Interrupt Requests*) can also be enabled, depending on the application.

10.5.5.1.2.1.4 Subsequence: DISPC Output Enable

This procedure enables the DISPC output. See Table 10-659.

Table 10-659. DISPC Output Enable

Step	Register/Bit Field Programming Model	Value
Enable the video or GFX pipeline.	DISPC_VIDp_ATTRIBUTES[0] ENABLE	0x1
	DISPC_GFX_ATTRIBUTES[0] ENABLE	0x1
Enable the DISPC output.	DISPC_CONTROLo[0] LCDENABLE	0x1

10.5.5.1.2.1.5 Subsequence: RFBI Output Enable

This procedure enables the RFBI output. Figure 10-177 details the settings for this subsequence.

Figure 10-177. RFBI Output Enable Flow Chart

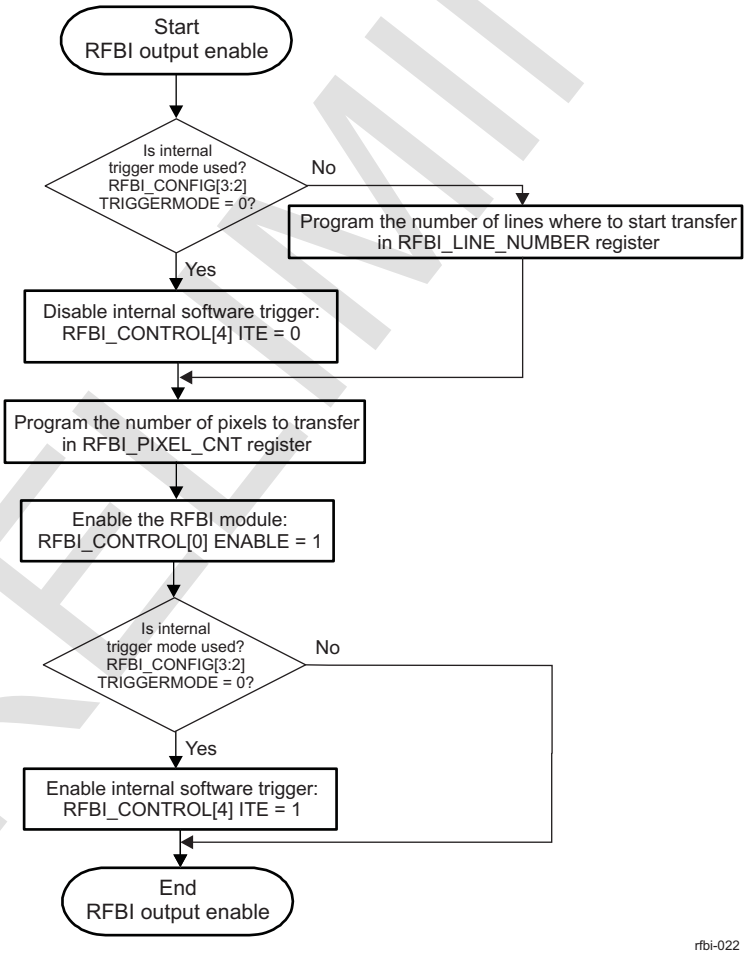

Table 10-660 describes RFBI output enable.

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Table 10-660. Register Call Summary for Subsequence: RFBI Output Enable

Register Name		
RFBI_CONFIG	RFBI_CONTROL	RFBI_LINE_NUMBER
RFBI_PIXEL_CNT		

Table 10-661 describes the RFBI behavior depending on the RFBI output enable.

Table 10-661. RFBI Behavior

RFBI_CONTROL[0] ENABLE Bit Value	RFBI Behavior
0	Slave port interconnect can write command/parameter/data and read data/status from the RFB. Slave port interconnect access can only be done to the active CS0.
1	The DISPC sends pixels to the RFB.

NOTE: The LCD output is disabled at the end of the transfer of the frame. The software must reenable the LCD output to generate a new frame by setting the DISPC_CONTROLo[0] LCDENABLE bit to 1.

CAUTION

The following registers must not be modified when the module is enabled (the RFBI_CONTROL[0] ENABLE bit set to 1):

- RFBI_CONTROL
- RFBI_PIXEL_CNT
- RFBI_LINE_NUMBER
- RFBI_STATUS
- RFBI_CONFIG
- RFBI_ONOFF_TIME
- RFBI_CYCLE_TIME
- RFBI_DATA_CYCLEi (i = 1 to 3)
- RFBI_VSYNC_WIDTH
- RFBI_HSYNC_WIDTH

NOTE: The RFBI_STALL STALL signal is asserted when the RFBI is disabled. Through the slave port, pixels can be sent to the LCD panel only when the pixel count has reached 0x0.

10.5.5.1.2.1.6 Subsequence: Detect Event

Table 10-662 describes the detect event.

Table 10-662. Detect Event

Step	Register/Bit Field Programming Model	Value
Wait until DISPC_IRQSTATUS != 0.	DISPC_IRQSTATUS	
Service event.	See Section 10.5.5.1.3, *RFBI Events Servicing*.	

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10.5.5.1.3 RFBI Events Servicing

10.5.5.1.3.1 FRAMEDONE Interrupt Servicing

The FRAMEDONE event occurs each time a frame has been transferred to the LCD panel. Figure 10-178 details how to serve this event.

Figure 10-178. FRAMEDONE Event Servicing Flow Chart

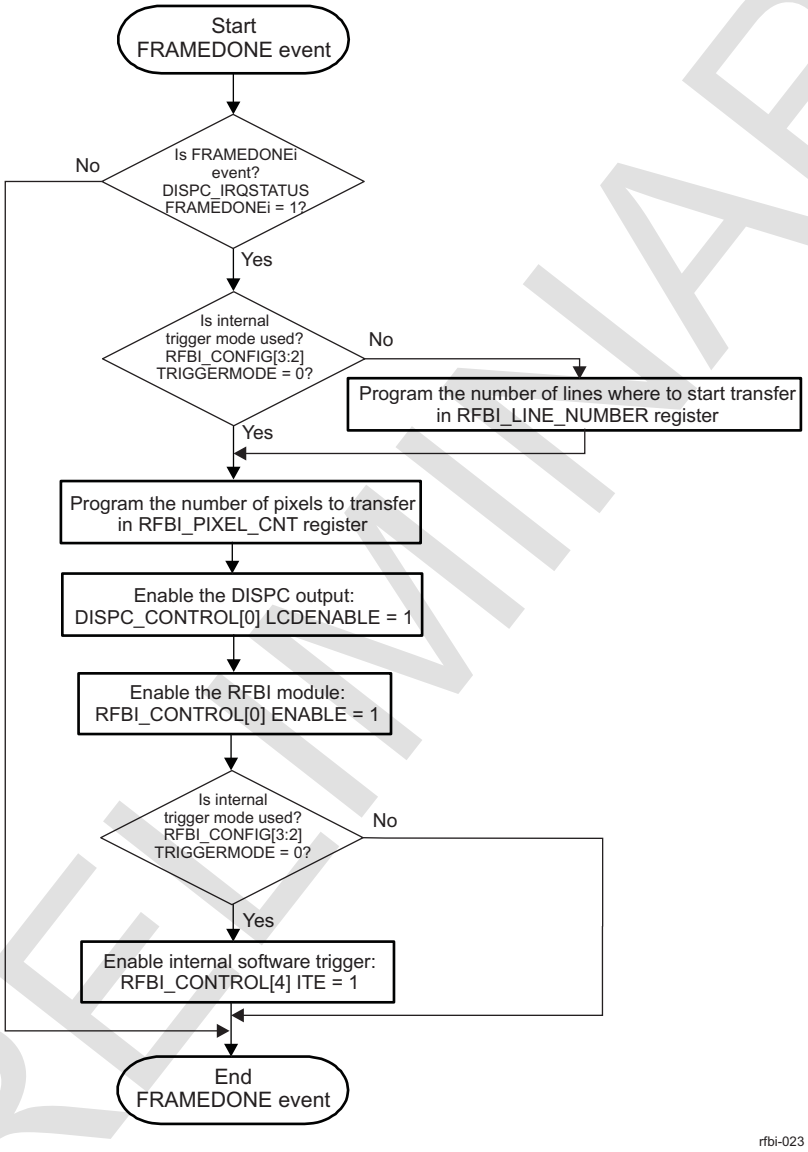

Table 10-663 describes FRAMEDONE interrupt servicing.

Table 10-663. Register Call Summary for RFBI Events Servicing: FRAMEDONE Interrupt Servicing

Register Name		
DISPC_IRQSTATUS	RFBI_CONFIG	RFBI_LINE_NUMBER
RFBI_PIXEL_CNT	DISPC_CONTROL	RFBI_CONTROL

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10.5.6 RFBI Hardware Status Features

Table 10-664 lists the RFBI hardware status features.

Table 10-664. RFBI Hardware Status Features

Feature	Type	Register/Bit Field/Observability Control	Description
Data pending	Status	RFBI_SYSTATUS[9] BUSYRFBIDATA	It is set to 1 when some data are pending to be processed from interconnect FIFO.
Slave port bus busy	Status	RFBI_SYSTATUS[9] BUSY	It is set to 1 when the slave port bus is busy and access of some RFBI registers (RFBI_CMD, RFBI_STATUS, RFBI_PARAM, and RFBI_READ) is stalled.

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10.5.7 RFBI Register Manual

CAUTION

The main access to all RFBI registers is through the L3 interconnect.

The access through L4_PER interconnect is provided for back software compatibility.

10.5.7.1 RFBI Instance Summary

Table 10-665. RFBI Instance Summary

Module Name	L3 Base Address	L4_PER Base Address	Size
RFBI	0x5800 2000	0x4804 2000	4KB

10.5.7.2 RFBI Registers

10.5.7.2.1 RFBI Register Summary

Table 10-666. RFBI Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	RFBI L3 Physical Address	RFBI L4_PER Physical Address
RFBI_REVISION	R	32	0x0000 0000	0x5800 2000	0x4804 2000
RFBI_SYSCONFIG	RW	32	0x0000 0010	0x5800 2010	0x4804 2010
RFBI_SYSSTATUS	R	32	0x0000 0014	0x5800 2014	0x4804 2014
RFBI_CONTROL	RW	32	0x0000 0040	0x5800 2040	0x4804 2040
RFBI_PIXEL_CNT	RW	32	0x0000 0044	0x5800 2044	0x4804 2044
RFBI_LINE_NUMBER	RW	32	0x0000 0048	0x5800 2048	0x4804 2048
RFBI_CMD	W	32	0x0000 004C	0x5800 204C	0x4804 204C
RFBI_PARAM	W	32	0x0000 0050	0x5800 2050	0x4804 2050
RFBI_DATA	W	32	0x0000 0054	0x5800 2054	0x4804 2054
RFBI_READ	RW	32	0x0000 0058	0x5800 2058	0x4804 2058
RFBI_STATUS	RW	32	0x0000 005C	0x5800 205C	0x4804 205C
RFBI_CONFIG	RW	32	0x0000 0060	0x5800 2060	0x4804 2060
RFBI_ONOFF_TIME	RW	32	0x0000 0064	0x5800 2064	0x4804 2064
RFBI_CYCLE_TIME	RW	32	0x0000 0068	0x5800 2068	0x4804 2068
RFBI_DATA_CYCLEi [(1)]	RW	32	0x0000 006C + (0x04 * i)	0x5800 206C + (0x04 * i)	0x4804 206C + (0x04 * i)
RFBI_VSYNC_WIDTH	RW	32	0x0000 0090	0x5800 2090	0x4804 2090
RFBI_HSYNC_WIDTH	RW	32	0x0000 0094	0x5800 2094	0x4804 2094

(1) i = 0 to 2

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10.5.7.2.2 RFBI Register Description

Table 10-667. RFBI_REVISION

Address Offset	0x0000 0000		
Physical Address	See Table 10-666.	**Instance**	RFBI
Description	This register contains the IP revision.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISON	IP revision	R	See(1)

(1) Ti internal data

Table 10-668. Register Call Summary for Register RFBI_REVISION

Remote Frame Buffer Interface
- RFBI Register Summary: [0]

Table 10-669. RFBI_SYSCONFIG

Address Offset	0x0000 0010		
Physical Address	See Table 10-666.	**Instance**	RFBI
Description	This register controls various parameters of the slave port interface.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RESERVED	RESERVED	SIDLEMODE			RESERVED	SOFTRESET	AUTOIDLE

Bits	Field Name	Description	Type	Reset
31:7	RESERVED	Write 0's for future compatibility. Reads returns 0.	RO	0x0000000
6	RESERVED	Write 0's for future compatibility. Reads returns 0.	RO	0
5	RESERVED	Write 0's for future compatibility. Reads returns 0.	RO	0
4:3	SIDLEMODE	Slave interface power management, Idle req/ack control. 0x0: Force-idle. An idle request is acknowledged unconditionally. 0x1: No-idle. An idle request is never acknowledged 0x2: Smart-idle. Acknowledgement to an idle request is given based on the internal activity of the module.	RW	0x0
2	RESERVED	Write 0's for future compatibility. Reads returns 0.	RO	0
1	SOFTRESET	Software reset Sets this bit to 1 to trigger a module reset. The bit is automatically reset by the hardware. During reads, it always returns 0. 0x0: Normal mode 0x1: The module is reset	RW	0

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Bits	Field Name	Description	Type	Reset
0	AUTOIDLE	Internal clock gating strategy (RFBI_ICLK clock and DISPC clock) 0x0: RFBI_ICLK clock and DISPC clock are free-running 0x1: Automatic clock gating strategy is applied for the RFBI_ICLK clock and DISPC clock, based on the slave port interface and internal activity.	RW	1

Table 10-670. Register Call Summary for Register RFBI_SYSCONFIG

Remote Frame Buffer Interface

- Software Reset: [0] [1]
- Power Management: [2] [3]
- RFBI Register Summary: [4]
- RFBI Register Description: [5]

Table 10-671. RFBI_SYSSTATUS

Address Offset	0x0000 0014		
Physical Address	See Table 10-666.	**Instance**	RFBI
Description	This register provides status information about the module, excluding the interrupt status information.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						BUSYRFBIDATA	BUSY	RESERVED							RESETDONE

Bits	Field Name	Description	Type	Reset
31:10	RESERVED	Reserved for module-specific status information Read returns 0	RO	0x000000
9	BUSYRFBIDATA	Data are pending to be processed from interconnect FIFO. Read 0x0: No data pending Read 0x1: Some data are pending	R	0
8	BUSY	Slave port busy status bit Read 0x0: The access to the following register is not stalled: RFBI_CMD, RFBI_STATUS, RFBI_PARAM, RFBI_READ. Read 0x1: The access to any of the following registers is stalled: RFBI_CMD, RFBI_STATUS, RFBI_PARAM, RFBI_READ.	R	0
7:1	RESERVED	Reserved. Read returns 0.	RO	0x00
0	RESETDONE	Internal reset monitoring. It can be used to determine when a hardware reset is completed or when a software reset is completed (software has set RFBI_SYSCONFIG[0] SOFTRESET to 1). Read 0x0: Internal module reset is ongoing Read 0x1: Reset completed	R	1

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Table 10-672. Register Call Summary for Register RFBI_SYSSTATUS

Remote Frame Buffer Interface

- Software Reset: [0]
- RFBI State-Machine: [1] [2] [3] [4] [5] [6] [7] [8] [9]
- Global Initialization: [10] [11]
- RFBI Register Summary: [12]

Table 10-673. RFBI_CONTROL

Address Offset	0x0000 0040		
Physical Address	See Table 10-666.	**Instance**	RFBI
Description	The register configures the RFBI module.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							SMART_DMA_REQ	DISABLE_DMA_REQ	HIGHTHRESHOLD		ITE	CONFIGSELECT		RFBIMODE	ENABLE

Bits	Field Name	Description	Type	Reset
31:9	RESERVED	Write 0's for future compatibility. Reads return 0.	RO	0x000000
8	SMART_DMA_REQ	Smart DMA request 0x0: The dmareq is asserted and deasserted depending on FIFO space even if MIdlereq is high in smart-idle/no-idle mode and the entire burst gets error responses from the module. 0x1: The dmareq is deasserted after 2 clock cycles if it has been asserted for more than or equal to 2 clock cycles and MIdlereq is high in smart-idle or no-idle mode. No more burst requests will be given even if the space is available in the FIFO.	RW	0
7	DISABLE_DMA_REQ	Disable DMA request 0x0: The dmareq is enabled and the signal is generated based on the space available and the request coming into the data register. 0x1: The dmareq is disabled and the signal is not generated at all based on space in FIFO. It stays high until the DISABLE DM AREQ is high even if there is space in FIFO to take requests.	RW	0
6:5	HIGHTHRESHOLD	Defines the FIFO high threshold used by hardware to assert DMA request. Used only if data written to RFBI_DATA are sent using system DMA. 0x0: Size of the transfer of 4 words of 32-bit wide 0x1: Size of the transfer of 8 words of 32-bit wide 0x2: Size of the transfer of 16 words of 32-bit wide	RW	0x0
4	ITE	Internal Trigger 0x0: Hardware waits for ITE bit to be set if in internal trigger mode for the configuration in use. 0x1: User sets the ITE bit to start the transfer, when hardware takes into account the bit, the hardware resets it.	RW	0

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Bits	Field Name	Description	Type	Reset
3:2	CONFIGSELECT	Select the CS and configuration 0x0: No CS selected 0x1: CS0 selected 0x2: Reserved 0x3: Reserved	RW	0x0
1	RFBIMODE	RFBI Mode 0x0: The RFBI mode is selected. 0x1: The RFBI mode is not selected.	RW	1
0	ENABLE	Enable/Disable flag 0x0: Disable the RFBI module. 0x1: Enable the RFBI module.	RW	0

Table 10-674. Register Call Summary for Register RFBI_CONTROL

Remote Frame Buffer Interface

- RFBI Parallel Interface (MIPI DBI Protocol): [0]
- Description of the Tearing Effect Pulse Signal: [1]
- DMA Requests: [2]
- Description: [3]
- Stall Mechanism: [4] [5] [6]
- Using DMA Request With Interconnect FIFO: [7] [8] [9] [10] [11] [12]
- Number of Pixels to Transfer: [13] [14]
- Configuration Selection: [15]
- RFBI Timings: [16] [17]
- Trigger Mode: [18]
- Internal Trigger Mode: [19] [20] [21]
- Global Initialization: [22] [23] [24] [25] [26]
- Operational Modes Configuration: [27] [28] [29] [30]
- RFBI Events Servicing: [31]
- RFBI Register Summary: [32]

Table 10-675. RFBI_PIXEL_CNT

Address Offset	0x0000 0044		
Physical Address	See Table 10-666.	**Instance**	RFBI
Description	The register configures the RFBI pixel count value.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PIXELCNT																															

Bits	Field Name	Description	Type	Reset
31:0	PIXELCNT	Pixel counter value The software indicates the number of pixels to transfer to the LCD panel frame buffer. The value is set when the module is disabled. During the transfer the hardware decrements the register when a pixel has been sent to the RFB.	RW	0x0000 0000

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Table 10-676. Register Call Summary for Register RFBI_PIXEL_CNT

Remote Frame Buffer Interface

- Number of Pixels to Transfer: [0] [1]
- Operational Modes Configuration: [2] [3]
- RFBI Events Servicing: [4]
- RFBI Register Summary: [5]

Table 10-677. RFBI_LINE_NUMBER

Address Offset	0x0000 0048		
Physical Address	See Table 10-666.	**Instance**	RFBI
Description	The register configures the number of lines to synchronize the beginning of the transfer.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																					LINENUMBER										

Bits	Field Name	Description	Type	Reset
31:11	RESERVED	Write 0's for future compatibility. Reads return 0.	RO	0x000000
10:0	LINENUMBER	Programmable line number Line number from 0 to 2047. Number of HSYNC after the VSYNC occurs before the beginning of the transfer.	RW	0x000

Table 10-678. Register Call Summary for Register RFBI_LINE_NUMBER

Remote Frame Buffer Interface

- External Trigger Mode: [0]
- Operational Modes Configuration: [1] [2]
- RFBI Events Servicing: [3]
- RFBI Register Summary: [4]
- RFBI Register Description: [5] [6]

Table 10-679. RFBI_CMD

Address Offset	0x0000 004C		
Physical Address	See Table 10-666.	**Instance**	RFBI
Description	The register configures the RFBI command.		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								CMD							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Write 0's for future compatibility. Reads return 0.	RO	0x000000
7:0	CMD	Command Value	W	0x00

Table 10-680. Register Call Summary for Register RFBI_CMD

Remote Frame Buffer Interface

- RFBI State-Machine: [0] [1]
- Global Initialization: [2]
- RFBI Hardware Status Features: [3]
- RFBI Register Summary: [4]
- RFBI Register Description: [5] [6]

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Table 10-681. RFBI_PARAM

Address Offset	0x0000 0050		
Physical Address	See Table 10-666.	**Instance**	RFBI
Description	The register configures the RFBI parameter.		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								PARAM							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Write 0's for future compatibility. Reads return 0.	RO	0x000000
7:0	PARAM	Parameter value	W	0x00

Table 10-682. Register Call Summary for Register RFBI_PARAM

Remote Frame Buffer Interface

- RFBI State-Machine: [0] [1]
- RFBI Hardware Status Features: [2]
- RFBI Register Summary: [3]
- RFBI Register Description: [4] [5]

Table 10-683. RFBI_DATA

Address Offset	0x0000 0054		
Physical Address	See Table 10-666.	**Instance**	RFBI
Description	The register configures the RFBI data.		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															

Bits	Field Name	Description	Type	Reset
31:0	DATA	Data value 12/16/18/24/2x16 bit value depending on: DataType [11:0] 12-bit DataType [15:0] 16-bit DataType [17:0] 18-bit DataType [23:0] 24-bit DataType [31:0] 2x16-bit	W	0x0000 0000

Table 10-684. Register Call Summary for Register RFBI_DATA

Remote Frame Buffer Interface

- Remote Frame Buffer Interface Overview: [0] [1]
- Description: [2] [3] [4]
- Using DMA Request With Interconnect FIFO: [5] [6] [7]
- RFBI State-Machine: [8] [9] [10] [11]
- RFBI Register Summary: [12]
- RFBI Register Description: [13]

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Table 10-685. RFBI_READ

Address Offset	0x0000 0058		
Physical Address	See Table 10-666.	**Instance**	RFBI
Description	The register configures the RFBI read.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								READ							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Write 0's for future compatibility. Reads return 0.	RO	0x000000
7:0	READ	Read value	RW	0x00

Table 10-686. Register Call Summary for Register RFBI_READ

Remote Frame Buffer Interface

- RFBI State-Machine: [0] [1]
- Global Initialization: [2] [3]
- RFBI Hardware Status Features: [4]
- RFBI Register Summary: [5]
- RFBI Register Description: [6] [7]

Table 10-687. RFBI_STATUS

Address Offset	0x0000 005C		
Physical Address	See Table 10-666.	**Instance**	RFBI
Description	The register configures the RFBI status.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								STATUS							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Write 0's for future compatibility. Reads return 0.	RO	0x000000
7:0	STATUS	Status value	RW	0x00

Table 10-688. Register Call Summary for Register RFBI_STATUS

Remote Frame Buffer Interface

- RFBI State-Machine: [0] [1]
- Global Initialization: [2] [3]
- Operational Modes Configuration: [4]
- RFBI Hardware Status Features: [5]
- RFBI Register Summary: [6]
- RFBI Register Description: [7] [8]

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Table 10-689. RFBI_CONFIG

Address Offset	0x0000 0060		
Physical Address	See Table 10-666.	**Instance**	RFBI
Description	The control register sets the configuration for the LCD 0 and LCD 1.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										HSYNCPOLARITY	TE_VSYNC_POLARITY	CSPOLARITY	WEPOLARITY	REPOLARITY	A0POLARITY	RESERVED			UNUSEDBITS		CYCLEFORMAT		PORTFORMAT	DATATYPE		TIMEGRANULARITY		TRIGGERMODE		PARALLELMODE	

Bits	Field Name	Description	Type	Reset
31:22	RESERVED	Write 0's for future compatibility. Reads return 0.	RO	0x000
21	HSYNCPOLARITY	HSYNC polarity 0x0: HSYNC active low 0x1: HSYNC active high	RW	1
20	TE_VSYNC_POLARITY	TE or VSYNC polarity 0x0: active low 0x1: active high	RW	1
19	CSPOLARITY	CS polarity 0x0: CS active low 0x1: CS active high	RW	0
18	WEPOLARITY	WE polarity 0x0: Active low 0x1: Active high	RW	0
17	REPOLARITY	RE polarity 0x0: Active low 0x1: Active high	RW	0
16	A0POLARITY	A0 polarity 0x0: A0 active low 0x1: A0 active high	RW	1
15:13	RESERVED	Write 0's for future compatibility. Reads return 0.	RO	0x0
12:11	UNUSEDBITS	State of unused bits 0x0: Low level (0) 0x1: High level (1) 0x2: Unchanged from previous state	RW	0x0
10:9	CYCLEFORMAT	Cycle format 0x0: 1 cycle for 1 pixel 0x1: 2 cycles for 1 pixel 0x2: 3 cycles for 1 pixel 0x3: 3 cycles for 2 pixels	RW	0x0

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Bits	Field Name	Description	Type	Reset
8:7	PORTFORMAT	Slave port write access format 0x0: 1 pixel per slave port access to the register data 0x2: 2 pixels per slave port access to the register data with first pixel at the position [15:0] 0x3: 2 pixels per slave port access to the register data with first pixel at the position [31:16]	RW	0x0
6:5	DATATYPE	Data type from the DISPC and slave port 0x0: 12-bit 0x1: 16-bit 0x2: 18-bit 0x3: 24-bit	RW	0x0
4	TIMEGRANULARITY	Multiplies signal timing latencies by 2 0x0: x2 latencies disabled 0x1: x2 latencies enabled	RW	0
3:2	TRIGGERMODE	Trigger mode 0x0: 00 Internal trigger mode (ITE bit mode) 0x1: External trigger mode (Tearing Effect Signal, rfbi_tevsync0 with programmable line counter defined in RFBI_LINE_NUMBER register) 0x2: External trigger mode (rfbi_tevsync0/rfbi_hsync0 with programmable line counter defined in RFBI_LINE_NUMBER register)	RW	0x0
1:0	PARALLELMODE	Parallel mode 0x0: 8-bit parallel output interface selected 0x1: 9-bit parallel output interface selected 0x2: Reserved 0x3: 16-bit parallel output interface selected	RW	0x0

Table 10-690. Register Call Summary for Register RFBI_CONFIG

Remote Frame Buffer Interface

- RFBI Parallel Interface (MIPI DBI Protocol): [0] [1] [2]
- Description of the Tearing Effect Pulse Signal: [3] [4] [5] [6]
- RFBI Input Formats: [7]
- Stall Mechanism: [8]
- Cycle Mode Selection: [9] [10] [11] [12]
- Unmodified Bits: [13]
- Read/Write: [14] [15]
- RFBI State-Machine: [16]
- RFBI Timings: [17]
- Trigger Mode: [18]
- Internal Trigger Mode: [19]
- Global Initialization: [20] [21] [22] [23] [24] [25] [26] [27] [28]
- Operational Modes Configuration: [29] [30]
- RFBI Events Servicing: [31]
- RFBI Register Summary: [32]

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Table 10-691. RFBI_ONOFF_TIME

Address Offset	0x0000 0064		
Physical Address	See Table 10-666.	**Instance**	RFBI
Description	The control register configures the RFBI timings for the LCD 0 and LCD 1.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								REOFFTIME								REONTIME								WEOFFTIME							
WEONTIME								CSOFFTIME								CSONTIME															

Bits	Field Name	Description	Type	Reset
31:30	RESERVED	Write 0's for future compatibility. Reads return 0.	RO	0x0
29:24	REOFFTIME	Read enable deassertion time from start access time. Number of RFBI_ICLK cycles	RW	0x00
23:20	REONTIME	Read enable assertion time from start access time. Number of RFBI_ICLK cycles	RW	0x0
19:14	WEOFFTIME	Write enable deassertion time from start access time. Number of RFBI_ICLK cycles	RW	0x00
13:10	WEONTIME	Write enable assertion time from start access time. Number of RFBI_ICLK cycles	RW	0x0
9:4	CSOFFTIME	CS deassertion time from start access time. Number of RFBI_ICLK cycles	RW	0x00
3:0	CSONTIME	CS assertion time from start access time. Number of RFBI_ICLK cycles	RW	0x0

Table 10-692. Register Call Summary for Register RFBI_ONOFF_TIME

Remote Frame Buffer Interface

- Transaction Timing Diagrams: [0] [1] [2] [3] [4] [5]
- RFBI Timings: [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20]
- Global Initialization: [21]
- Operational Modes Configuration: [22]
- RFBI Register Summary: [23]

Table 10-693. RFBI_CYCLE_TIME

Address Offset	0x0000 0068		
Physical Address	See Table 10-666.	**Instance**	RFBI
Description	The control register configures the RFBI timings for the LCD 0 and LCD 1.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								ACCESSTIME								WRENABLE	WWENABLE	RRENABLE	RWENABLE	CSPULSEWIDTH								RECYCLETIME			
WECYCLETIME																															

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Bits	Field Name	Description	Type	Reset
31:28	RESERVED	Write 0's for future compatibility. Reads return 0.	RO	0x0
27:22	ACCESSTIME	Access time number of RFBI_ICLK cycles	RW	0x00
21	WRENABLE	Write-to-read pulse width enable (same CS) 0x0: CSPULSEWIDTH does not apply on Write-to-Read access 0x1: CSPULSEWIDTH applies on Write-to-Read access	RW	0
20	WWENABLE	Write-to-write pulse width enable (same CS) 0x0: CSPULSEWIDTH does not apply on Write-to-Write access 0x1: CSPULSEWIDTH applies on Write-to-Write access	RW	0
19	RRENABLE	Read-to-read pulse width enable (same CS) 0x0: CSPULSEWIDTH does not apply on Read-to-Read access 0x1: CSPULSEWIDTH applies on Read-to-Read access	RW	0
18	RWENABLE	Read-to-write pulse width enable (same CS): 0x0: CSPULSEWIDTH does not apply on Read-to-Write access 0x1: CSPULSEWIDTH applies on Read-to-Write access	RW	0
17:12	CSPULSEWIDTH	CS pulse width number of RFBI_ICLK cycles	RW	0x00
11:6	RECYCLETIME	RE cycle time number of RFBI_ICLK cycles	RW	0x00
5:0	WECYCLETIME	WE cycle time number of RFBI_ICLK cycles	RW	0x00

Table 10-694. Register Call Summary for Register RFBI_CYCLE_TIME

Remote Frame Buffer Interface

- Transaction Timing Diagrams: [0] [1] [2]
- RFBI Timings: [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15]
- Global Initialization: [16]
- Operational Modes Configuration: [17]
- RFBI Register Summary: [18]

Table 10-695. RFBI_DATA_CYCLEi

Address Offset	0x0000 006C + (0x04 * i)	**Index**	i = 0 to 2
Physical Address	See Table 10-666.	**Instance**	RFBI
Description	The control register configures the RFBI data format for ith cycle (i = 1 for firstcycle, i = 2 for second cycle, i = 3 for thrid cycle).		
Type	RW		

31 30 29 28	27 26 25 24	23 22 21	20 19 18 17 16	15 14 13 12	11 10 9 8	7 6 5	4 3 2 1 0
RESERVED	BITALIGNMENTPIXEL2	RESERVED	NBBITSPIXEL2	RESERVED	BITALIGNMENTPIXEL1	RESERVED	NBBITSPIXEL1

Bits	Field Name	Description	Type	Reset
31:28	RESERVED	Write 0's for future compatibility. Reads return 0.	RO	0x0
27:24	BITALIGNMENTPIXEL2	Alignment of the bits from pixel 2 on the output interface	RW	0x0
23:21	RESERVED	Write 0's for future compatibility. Reads return 0.	RO	0x0

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Bits	Field Name	Description	Type	Reset
20:16	NBBITSPIXEL2	Number of bits from the pixel 2 (value from 0 to 16 bits). The values from 17 to 31 are invalid.	RW	0x00
15:12	RESERVED	Write 0's for future compatibility. Reads return 0.	RO	0x0
11:8	BITALIGNMENTPIXEL1	Alignment of the bits from pixel 1 on the output interface	RW	0x0
7:5	RESERVED	Write 0's for future compatibility. Reads return 0.	RO	0x0
4:0	NBBITSPIXEL1	Number of bits from the pixel 1 (value from 0 to 16 bits). The values from 17 to 31 are invalid.	RW	0x00

Table 10-696. Register Call Summary for Register RFBI_DATA_CYCLEi

Remote Frame Buffer Interface

- Cycle Mode Selection: [0]
- Operational Modes Configuration: [1]
- RFBI Register Summary: [2]

Table 10-697. RFBI_VSYNC_WIDTH

Address Offset	0x0000 0090		
Physical Address	See Table 10-666.	**Instance**	RFBI
Description	The register configures the RFBI VSYNC minimum pulse width.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																MINVSYNCPULSEWIDTH															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Write 0's for future compatibility. Reads return 0.	RO	0x0000
15:0	MINVSYNCPULSEWIDTH	Programmable minimum VSYNC pulse width Minimum VSYNC pulse width from 0 to 65535. Number of RFBI_ICLK clock cycles to determine when VSYNC pulse occurs. The values 0 and 1 are invalid.	RW	0x0000

Table 10-698. Register Call Summary for Register RFBI_VSYNC_WIDTH

Remote Frame Buffer Interface

- Description of the Tearing Effect Pulse Signal: [0]
- External Trigger Mode: [1] [2]
- Global Initialization: [3]
- Operational Modes Configuration: [4]
- RFBI Register Summary: [5]

Table 10-699. RFBI_HSYNC_WIDTH

Address Offset	0x0000 0094		
Physical Address	See Table 10-666.	**Instance**	RFBI
Description	The register configures the RFBI HSYNC minimum pulse width.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																MINHSYNCPULSEWIDTH															

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Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Write 0's for future compatibility. Reads return 0.	RO	0x0000
15:0	MINHSYNCPULSEWIDTH	Programmable minimum HSYNC pulse width minimum HSYNC pulse width from 0 to 65535. Number of RFBI_ICLK clock cycles to determine when HSYNC pulse occurs.The values 0 and 1 are invalid.	RW	0x0000

Table 10-700. Register Call Summary for Register RFBI_HSYNC_WIDTH

Remote Frame Buffer Interface

- Description of the Tearing Effect Pulse Signal: [0]
- External Trigger Mode: [1] [2]
- Global Initialization: [3]
- Operational Modes Configuration: [4]
- RFBI Register Summary: [5]

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10.6 Video Encoder

This section describes the video encoder for the device.

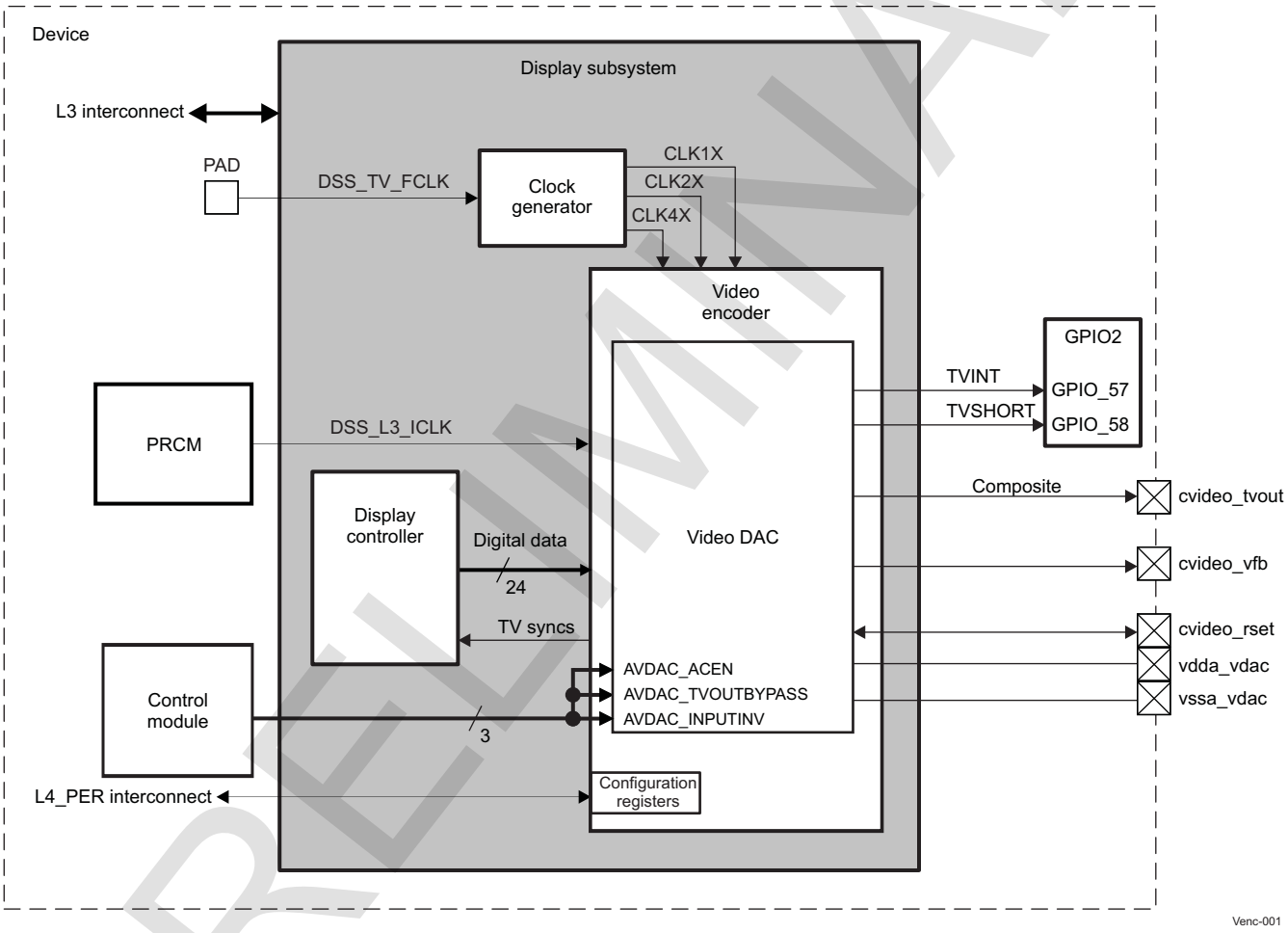
NOTE: The VDAC function is not supported.

10.6.1 Video Encoder Overview

The display subsystem provides the logic to display a video frame from the memory frame buffer (either SDRAM or SRAM) on a a TV set.

Figure 10-179 shows a block diagram of the display subsystem.

Figure 10-179. Video Encoder Overview



The video encoder includes the following features:

- Supports the following standards for composite video (CVBS) :
  - NTSC-J, M
  - PAL-B, D, G, H, I
  - PAL-M
- Input data interface compatible with the following protocols:
  - 24-bit input bus compatible with external sync
  - RGB 4:4:4
- 10-bit interface for internal digital-to-analog converter (DAC) that supports:

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  - 1.1V digital power supply, 1.8V analog power supply
  - 10-bit resolution
  - DNL within 1 LSB and INL within 1 LSB
  - Sample rate of up to 60 megasamples per second (MSPS)
  - Supports composite video standart output
  - Supports TVOUT buffer bypass mode (DAC only mode)
  - Full-scale voltage output: 1.2 Vpp with a 75-Ω load
  - Internal TV detect feature
  - Signal-to-noise ratio (SNR) is 54 dB (taking into account the ac coupling)
  - Suitable for low-power wireless applications
  - Power-down mode with less than 12-µA standby current
  - Differential gain error and differential phase error: within 3% and 1°, respectively
- TV output data supports ITU-R BT 470-7 recommendation standard for consumer market
- Master clock input 13.5 MHz, 27 MHz (supports ITU-R 601 sampling for NTSC/PAL), and 54 MHz
- Programmable horizontal sync, vertical timing, and waveforms
- Programmable subcarrier frequency and SCH
- Internal test pattern generation (color bar, flat field, color burst)
- 2x/4x oversampling
- TV detection gating pulse generation
- Supports square pixel sampling (NTSC: 12.27 MHz, 24.54 MHz, 49.09 MHz PAL: 14.75 MHz, 29.5 MHz, 59 MHz)

CAUTION

In square pixel mode, an external clock generator is required to provide sampling frequencies.

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10.6.2 Video Encoder Environment

To display on a TV, the path used is as follow:

- Display controller
- Video encoder
- 10-bit DAC with video amplifiers

NOTE: The VDAC function is not supported.

The display controller module receives synchronization signals from the video encoder and synchronously sends pixel data to the video encoder with these signals. The digital output of the display controller is always a 24-bit RGB value based on a pixel request from the video encoder. For more information on the display controller settings and features, see Section 10.2, *Display Controller*.

The video encoder converts RGB video signals to conform to the NTSC/PAL standard analog video. The video encoder includes an integrated synchronization signal generator and a video digital-to-analog converter (DAC) with video amplifiers, data manager, luma stage, chroma stage, modulator, and a control interface.

The video encoder also provides the synchronization signals to the display controller: VSYNC, active VIDeo (AVID), and field ID (FID).

NOTE: To enhance the TV color display, it is highly recommended to set the DSS_CONTROL[4] DAC_DEMEN bit.

Figure 10-180 through Figure 10-182 show the TV display interface in composite mode.

Figure 10-180. Video Encoder Environment, Normal Mode DC-Coupling

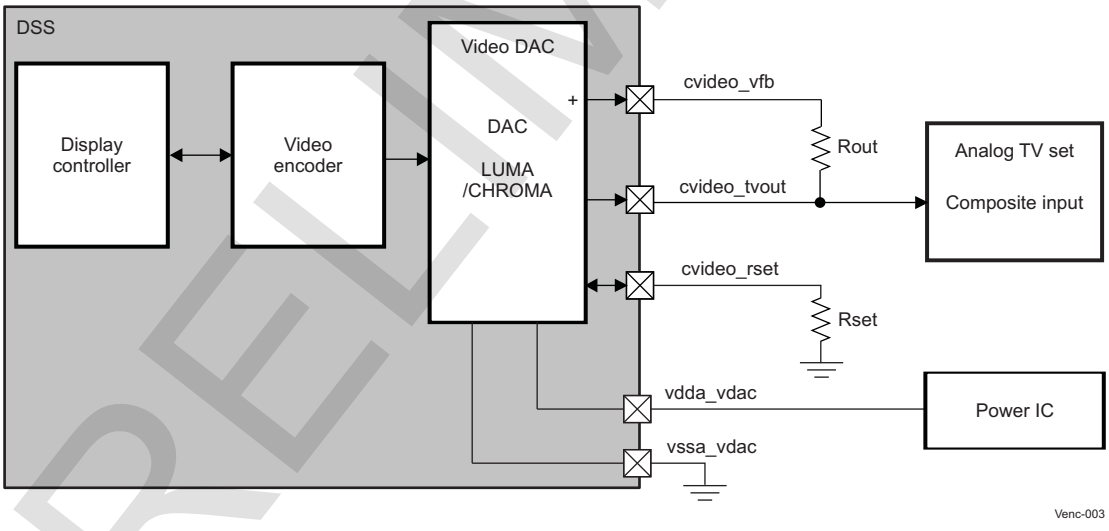

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Figure 10-181. Video Encoder Environment, Normal Mode AC-Coupling

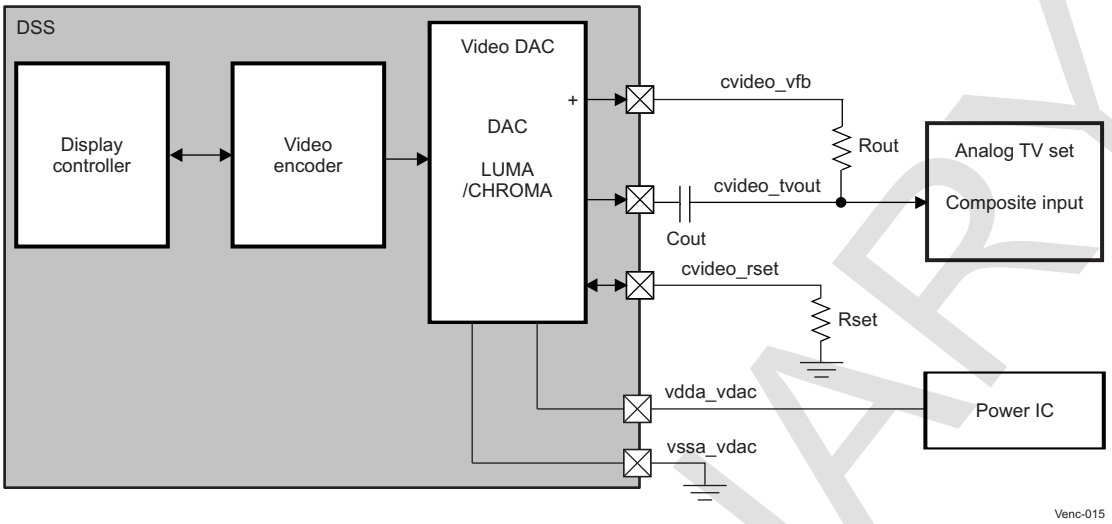

Figure 10-182. Video Encoder Environment, Bypass Mode

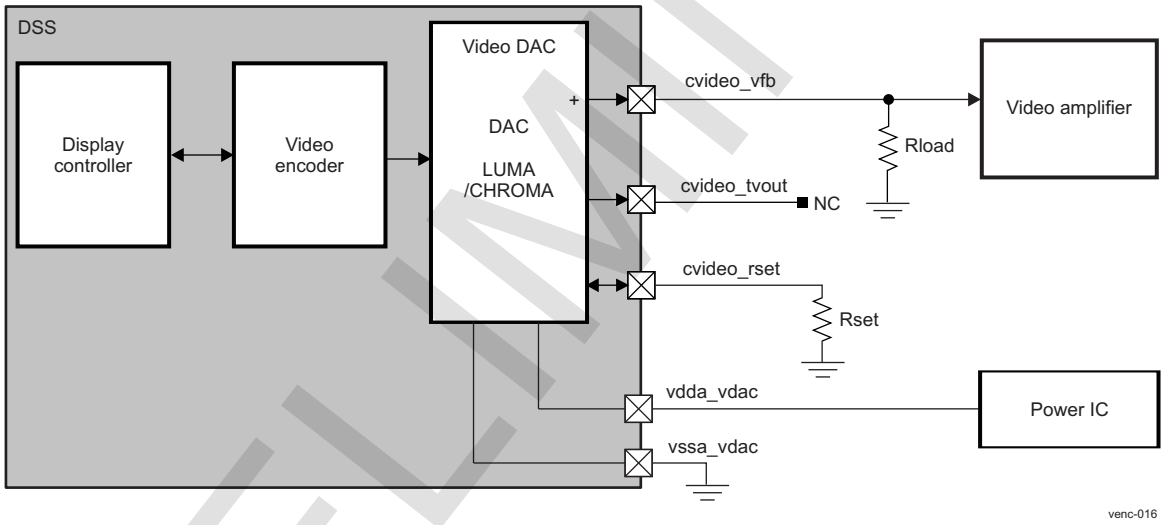

Table 10-701 describes the interface signals to/from the TV set for TV display support.

Table 10-701. TV Display Interface Pins

Pin Name	Type [1]	Description
cvideo_tvout	O	Analog luma or composite video output. An external resistor (Rout) is connected between this node and the *cvideo_vfb* pin. The nominal value of Rout is 2700 Ω. This is the output node that drives the load (75 Ω). In AC-coupling mode, a series capacitor (Cout) must be connected. The nominal value for Cout is ≥ 200 µF.
cvideo_vfb	O	In Normal mode (video DAC+Buffer), it acts as the buffer feedback node. An external resistor (Rout) shall be connected between this node and *cvideo_tvout* pin. In TVOUT Bypass mode, it acts as the video DAC output. A load resistor (Rload) shall be connected to the pin to ground. The nominal value of Rload is 1500 Ω.

(1) I = input; O = output; power = power pin

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Table 10-701. TV Display Interface Pins (continued)

Pin Name	Type [1]	Description
cvideo_rset	I/O	External resistor (Rset) shall be connected to this pin to set the reference current of the video DAC. The value of the resistor depends on the mode of operation (Normal or TVOUT Bypass). In Normal mode, the nominal value for Rset is 4700 Ω. In TVOUT Bypass mode, the nominal value for Rset is 10000 Ω.
vdda_vdac	Power	Analog supply voltage for the video DAC
vssa_vdac	Power	Analog ground for the video DAC

CAUTION

- *cvideo_tvout* is a very high-frequency analog signal and must be routed with extreme care. As a result, the path of this signal must be as short as possible, and as isolated as possible from other interfering signals.
- During board design, the onboard traces and parasites must be matched for the channel. *cvideo_vfb* pin is the most sensitive pins in the TV out system. Low onboard resistance is required for the traces that connect the Rout to the *cvideo_vfb* and *cvideo_tvout* pins. The resistance on those trace affects output impedance matching. Therefore, Rout resistor is suggested to be placed as close as possible to the device pins. The onboard traces lead to the TV OUT pin must have a characteristic impedance of 75 Ohm starting from the closest possible place to the device pin output.
- If the TV output is not used, the following configuration for the VDAC pins must be applied:
  - vdda_vdac (connected to the vdda_hdmi_vdac ball, commonly used with the HDMI module):
    - If the HDMI module is used, then the vdda_hdmi_vdac ball is supplied. Respectively, the vdda_vdac pin is also supplied. The VDAC must be maintained in total power-down mode by software. For more information, see Section 10.6.4.6.7, *Video DAC Power Management*.
    - If the HDMI module is not used, the vdda_vdac pin must be grounded.
  - vssa_vdac: Must be grounded
  - cvideo_rset: Must be floating, left unconnected
  - cvideo_tvout: Must be floating, left unconnected
  - cvideo_vfb: Must be floating, left unconnected
- To avoid current leakage, the following bits must be set to 0:
  - DSS.DSS_CONTROL[5] DAC_POWERDN_BGZ
  - VENC_OUTPUT_CONTROL[1] COMPOSITE_ENABLE
  - PRCM.CM_DSS_DSS_CLKCTRL[11] OPTFCLKEN_TV_FCLK
  - CONTROL.CONTROL_AVDAC[30] AVDAC_TVOUTBYPASS

Table 10-702 lists the typical values of the external components for different modes of the TV display interface.

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Table 10-702. Typical Values for Rout, Rset, Rload, and Cout

	Composite, DC-Coupled	Composite, AC-Coupled	Bypass Mode	Unit
Rout	2700	2700	N/A	Ω
Rset	4700	4700	10,000	Ω
Rload	N/A	N/A	1500	Ω
Cout	N/A	≥ 220	N/A	µF

10.6.3 Video Encoder Integration

This section describes the integration of the display subsystem and details clocks, resets, hardware requests, and power modes.

Figure 10-183 shows the integration of the display subsystem in the device.

Figure 10-183. Video Encoder Integration

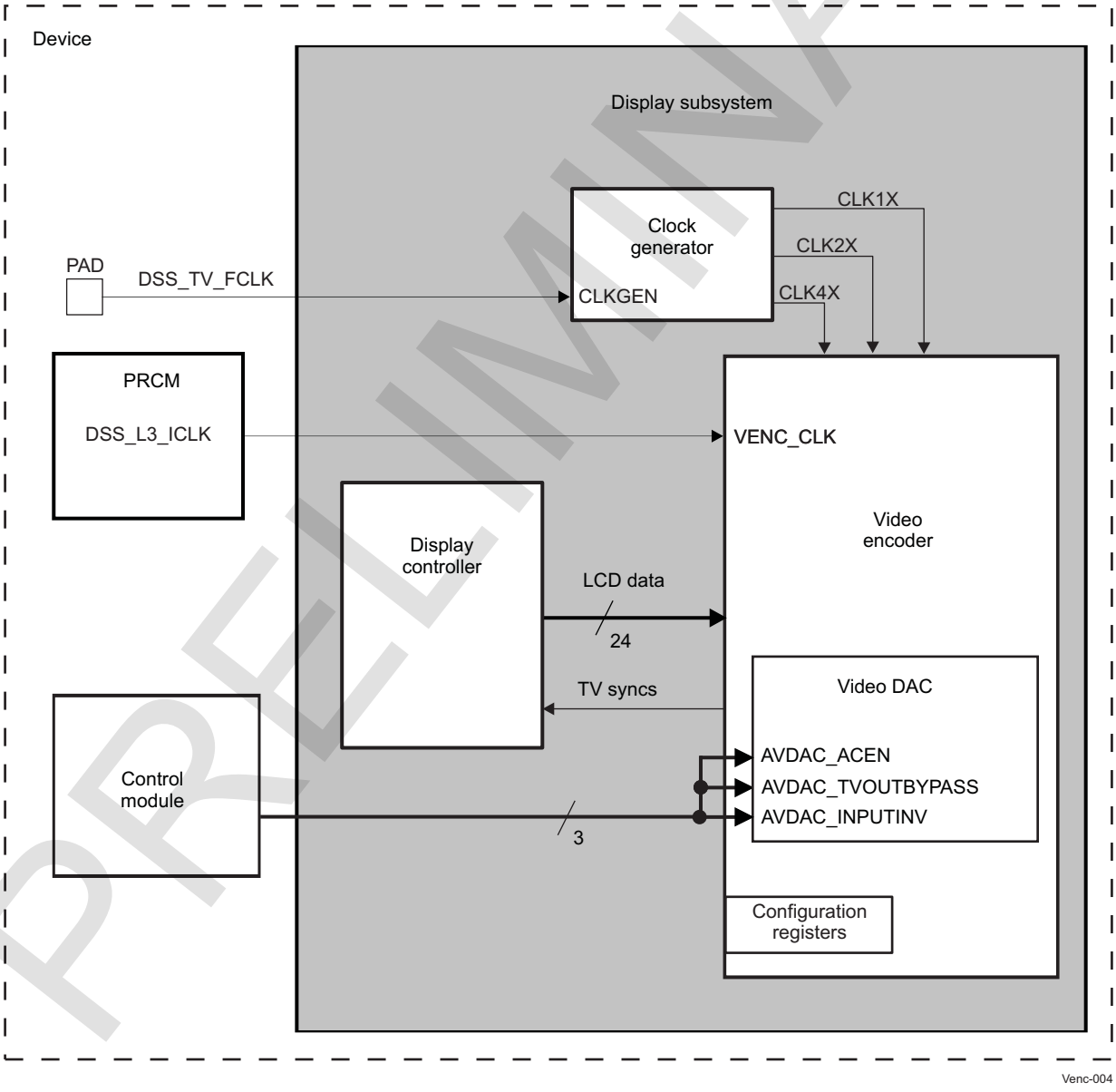

Table 10-703 describes the different clocks with their possible frequency values.

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Table 10-703. Clocks

Clocks				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
Video encoder	VENC_CLK	DSS_L3_ICLK	PRCM	For information about PRCM clock gating and management, see Chapter 3,*Power, Reset, and Clock Management*.
Clock generator	CLKGEN	DSS_TV_FCLK	PAD	Functional clock provided on pad. Controlled by the PRCM module.
Resets				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
Video encoder DAC	DSS_RST	DSS_RST	PRCM	Reset signal of the display subsystem power domain, from the PRCM module.

- Video encoder clock:

  The CLKGEN is divided into three balanced clocks (see Table 10-704), depending on the clock mode selected through the DSS.DSS_CTRL[2] VENC_CLOCK_MODE bit (see Section 10.1.3, *DSS Register Manual*).

Table 10-704. Digital Clock Division for the Video Encoder

Clock Output	**Clock Mode**	
	Clock mode 0	**Clock mode 1**
CLK4X	DSS_TV_FCLK	DSS_TV_FCLK or 0 (gated)
CLK2X	DSS_TV_FCLK/2	DSS_TV_FCLK
CLK1X	DSS_TV_FCLK/4	DSS_TV_FCLK/2

NOTE: The DSS_TV_CLK clock is derived from the SYS_ALTCLK clock.

The source for the SYS_ALTCLK clock can be the fref_xtal_in or fref_slicer_in device pad.

An external clock generator must be connected to the fref_slicer_in or fref_xtal_in pad. A 54-MHz clock is needed for PAL or NTSC 601, a 49.04-MHz clock is needed for NTSC square pixel, and a 59-MHz clock is needed for the PAL square pixel.

The selection of the input source pad for the SYS_ALTCLK clock:

- Depends on the configuration of the sys_boot[7:6] device pads. For more information, see Section 27.2.4.1, *Clock Source Selection*, in Chapter 27, *Initialization*.
- Depends on the required use case:
  - If DSS_TV_FCLK = 27 MHz is required, then the fref_slicer_in or fref_xtal_in pad can be used as the source for SYS_ALTCLK.
  - If DSS_TV_FCLK = 49.04, 54 MHz, or 59 MHz is required, then the fref_xtal_in pad must be used as the source for SYS_ALTCLK.

Gating control over SYS_ALTCLK is provided in PRCM module registers. For more information, see Section 3.6.13.4, *Clock Domain Module Attributes*, in Chapter 3, *Power, Reset, and Clock Management*.

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NOTE: Clock mode 1 can be used with both an external clock 27 MHz provided to VENC, but also with a 27-MHz clock generated internally by the HDMI PLL module. The source of the TV_CLK can be either DSS_TV_FCLK or PLL3_CLK1 clock signals (see Section 10.1.2.1, *DSS Clocks*).

After device reset, clock mode 0 is selected by default, and DSS_TV_FCLK clock is disabled.

For proper Video DAC configuration in both clock mode 0 or clock mode 1, clock output CLK4X shall always be active by setting the DSS.DSS_CTR[3] VENC_CLOCK_4X_ENABLE bit to 1 (see Section 10.1.3, *DSS Register Manual*).

The TV_CLK/4 in clock mode 0, or TV_CLK/2 in clock mode 1, is used into the DISPC to send data to the VENC.

- Video DAC clocks:
  The video data are latched on the positive edge of the DSS_TV_FCLK clock.

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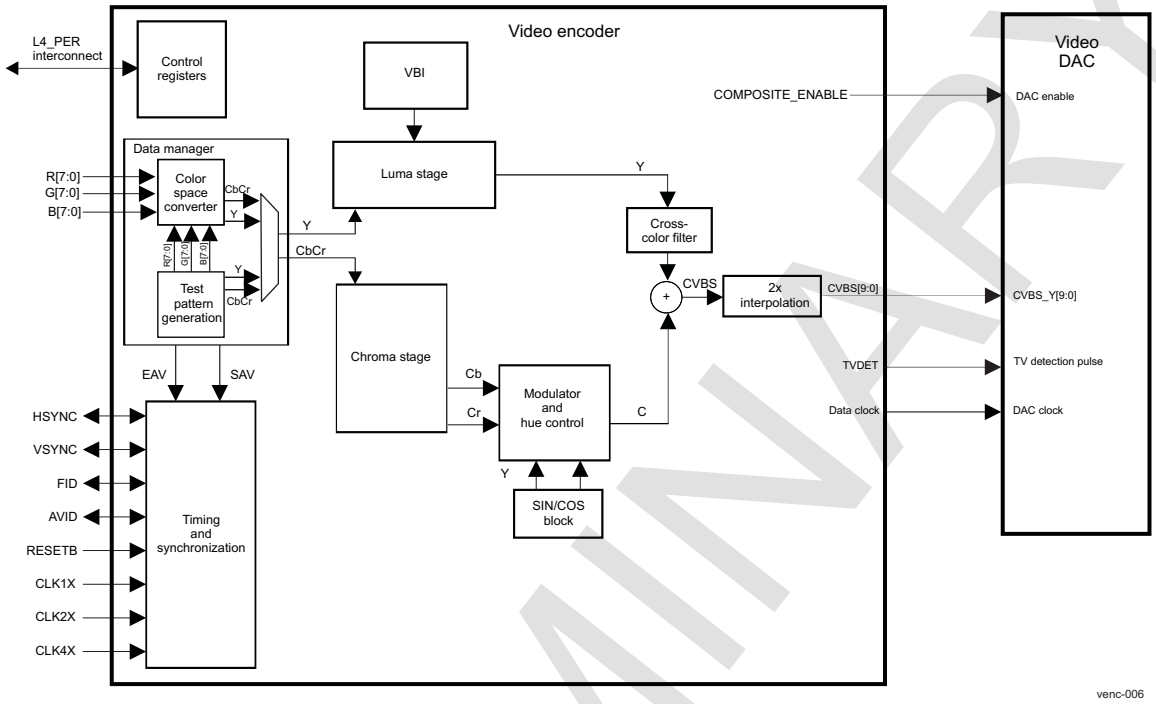
10.6.4 Video Encoder Functional Description

Figure 10-184 shows an overview of the video encoder architecture.

Figure 10-184. Video Encoder Architecture Overview



10.6.4.1 Data Manager

The data manager allows user to select two sources of data inputs:

- Data coming from the Display Controller.
- Data coming from the test pattern generation.

The source is selected by programming SVDS field VENC_F_CONTROL[7:6].

10.6.4.1.1 Color Space Converter

In the display subsystem, the input format from the display controller is always 24-bit RGB coming from the display controller or the test pattern generation. The RGB-to-YCbCr color space converter converts the 24-bit RGB pixel data into 16-bit YCbCr 4:2:2 data.

10.6.4.1.2 Test Pattern Generation

For diagnostic purposes, the data manager can be forced to output 100/100 color bar RGB/YCbCr data. To use the test pattern generation, SVDS VENC_F_CONTROL[7:6] field shall be set to 0x1. If FMT field VENC_F_CONTROL[1:0] is set to 0x0 then the 24-bits RGB test pattern data will be converted into 16-bit YCbCr 4:2:2 data by the Color Space Converted. Otherwise if FMT field VENC_F_CONTROL[1:0] is set to 0x2 then 16-bit YCbCr 4:2:2 test pattern data are outputed directly, the color space converted is bypassed. Table 10-705 resume the test paten generator datas.

Table 10-705. 100/100 Color Bar Table

COLOR	R	G	B	Y	Cb	Cr
White	255	255	255	235	128	128
Yellow	255	255	0	210	16	146
Cyan	0	255	255	170	166	16

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Table 10-705. 100/100 Color Bar Table (continued)

Green	0	255	0	145	54	34
Magenta	255	0	255	106	202	222
Red	255	0	0	81	90	240
Blue	0	0	255	41	240	110
Black	0	0	0	16	128	128

10.6.4.2 Luma Stage

The luma stage includes a luma pipeline delay, luma shaping, 2x interpolation filter, and luma variable delay. The luma pipeline delay block is used to match luma path length to chroma path length. In the luma gain shaper, a programmable gain is first applied to the luminance data output. The luminance gain is defined by the VENC_GAIN_Y register. Horizontal sync, vertical sync, and setup insertion are then performed.

Black level and blank level are programmable through the VENC_BLACK_LEVEL and VENC_BLANK_LEVEL registers. All the transition edges of the luminance signal, such as sync edges and active video edges, are properly shaped and filtered to keep the bandwidth within the standards.

After all required components of the luminance signal are added, the resulting signal is low-passed and interpolated to 2x-pixel rate. This 2x interpolation simplifies the external analog reconstruction filter design and improves the signal-to-noise ratio.

10.6.4.3 Chroma Stage

The chroma stage includes a low-pass filter, first-stage 2x interpolation, chroma gain shaper, and second-stage 2x interpolation. A pair of programmable gains adjusts the time-multiplexed U/V signal. The gains for U and V are independently controlled by the VENC_GAIN_U and VENC_GAIN_V register bits.

10.6.4.4 Subcarrier and Burst Generation

The encoder uses a 32-bit subcarrier increment to synthesize the subcarrier. The value of the subcarrier increments required to generate the desired subcarrier frequency for NTSC and PAL format is found by:

$S_CARR = ROUND ([F_{sc}/F_{CLK2X}] \times 2^{32})$

where:

F_{sc} = Frequency of the subcarrier

F_{CLK2X} = Frequency of the internal video encoder

The VENC_S_CARR register controls the subcarrier frequency. The VENC_C_PHASE register controls the phase of the subcarrier. The phase of the color subcarrier is reset to VENC_C_PHASE. Table 10-706 presents the VENC_S_CARR register values depending the standard and pixel type used.

Table 10-706. VENC_S_CARR Register Recommended Values

Standard	Pixel Type	Subcarrier Frequency (Fsc) (MHz)	Fclkenc (MHz)	VENC_S_CARR Register Value (hexa)
NTSC-M, J	ITU-R601	3.579545	27	0x21F07C1F
PAL-M	ITU-R601	3.5756083125	27	0x21E6EFE3
PAL-B, D, G, H, I	ITU-R601	4.43361875	27	0x2A098ACB
NTSC-M, J	Square pixel	3.579545	24.5454(1)	0x25555555
PAL-M	Square pixel	3.579561149	24.5454(1)	0x1F15C01E
PAL-B, D, G, H, I	Square pixel	4.43361875	29.50(1)	0x26798C0C

(1) In square pixel mode, an external clock generator is needed to provide sampling frequencies (49.09 MHz for NTSC square pixel or 59 MHz for PAL square pixel).

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The color subcarrier reset has four modes:

- No reset
- Reset every two lines
- Reset every two fields
- Reset every eight fields

The VENC_C_PHASE register can be used to adjust the SCH (subcarrier to horizontal sync phase). The VENC_BSTAMP_WSS_DATA[6:0] BSTAP bit field sets the amplitude of the color burst.

Phase alternation line refers to the encoding scheme in which the subcarrier alternates between two phases every scan line. Setting to 0x1, the VENC_M_CONTROL[1] PAL bit enables phase alternation line encoding. Otherwise, a normal subcarrier is generated. .Two possible alternation sequences are possible by setting the VENC_M_CONTROL[5] PALPHS bit.

10.6.4.5 Vertical Blanking Interval

10.6.4.5.1 Closed Caption Encoding

The encoder can be programmed to encode closed-caption data and extended data in the selected line. The closed-caption data are sent to the encoder through the L4_PER interconnect. The data stream consists of 7-bit US-ASCII code and 1 odd-parity bit (see Table 10-707).

Table 10-707. Closed-Caption Data Format

MSB							LSB
Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Odd parity

The standard service encodes closed caption in both fields; the extended service encodes closed caption in even fields. When set to 1, the VENC_L21_WC_CTL L21EN[0] bit enables closed-caption encoding in odd fields. When set to 1, the VENC_L21_WC_CTL L21EN[1] bit enables closed-caption encoding in even fields.

To select the scan line where the CC data are encoded, program the VENC_LN_SEL[4:0] SLINE bit field.

CAUTION

The setting of the SLINE[4:0] bit field value depends on the video standard:

- PAL mode: Because there is a one-line offset, program the desired line number – 1. To activate the closed caption on line 21 (0x15), program the value 0x15 – 1 = 0x14. The default value is 0x15 + 1 = 0x16 (line 22).
- NTSC mode: Because there is a four-line offset, program the desired line number – 4. To activate the closed caption on line 21 (0x15), program the value 0x15 – 4 = 0x11. The default value is 0x15 + 4 = 0x19 (line 25).

The VENC_LN_SEL[25:16] LN21_RUNIN bit field should be kept at reset value (0x10B). Four closed-caption data registers contain the data to be encoded. The VENC_LINE21[15:8] L21O and VENC_LINE21[7:0] L21O bit fields contain the first and the second bytes, respectively, of closed-caption data to be encoded in the odd field. The VENC_LINE21[31:24] L21E and VENC_LINE21[23:16] L21E bit fields contain the first and the second bytes, respectively, of data to be encoded in the even field.

Immediately after the closed-caption data is written to the registers, in either the odd field or even field, the corresponding closed-caption status bit (VENC_STATUS[4] CCE or VENC_STATUS[3] CCO) is reset to 0 to indicate that the closed-caption data is available in the closed-caption data registers and yet to be encoded.

Immediately after the closed-caption data is encoded, the VENC_STATUS[4] CCE bit or the VENC_STATUS[3] CCO bit is set to 1 to indicate that the closed-caption data has been encoded and is ready to accept new data. As seen in Figure 10-185, a null character is automatically inserted if the closed-caption data is not written to the closed-caption data registers in time for encoding.

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The running clock frequency is controlled by the VENC_CC_CARR_WSS_CARR[15:0] FCC bit field which should be kept at reset value (0x2631) to get 5034960.5Hz (32xfline) for NTSC-601. The closed-caption running clock common frequencies are detailed in Table 10-708.

Table 10-708. Closed-Caption RunClock Frequency Settings

	NTSC-601	PAL-601	NTSC Square Pixel	PAL Square Pixel
VENC_CC_CARR_WSS_CARR[15:0] FCC bit field value	0x2631	0x25ED	0x2A03	0x22B6

The closed-caption data is encoded in nonreturn-to-zero (NRZ) format. Additionally, the data translates to the IRE scale as follows:

- 0 = 0 IRE
- Sync pulse = -40 IRE
- 1 = 50 IRE

Figure 10-185 shows the parameters of closed-caption line data implemented in different standards.

Figure 10-185. Closed Captioning Timing

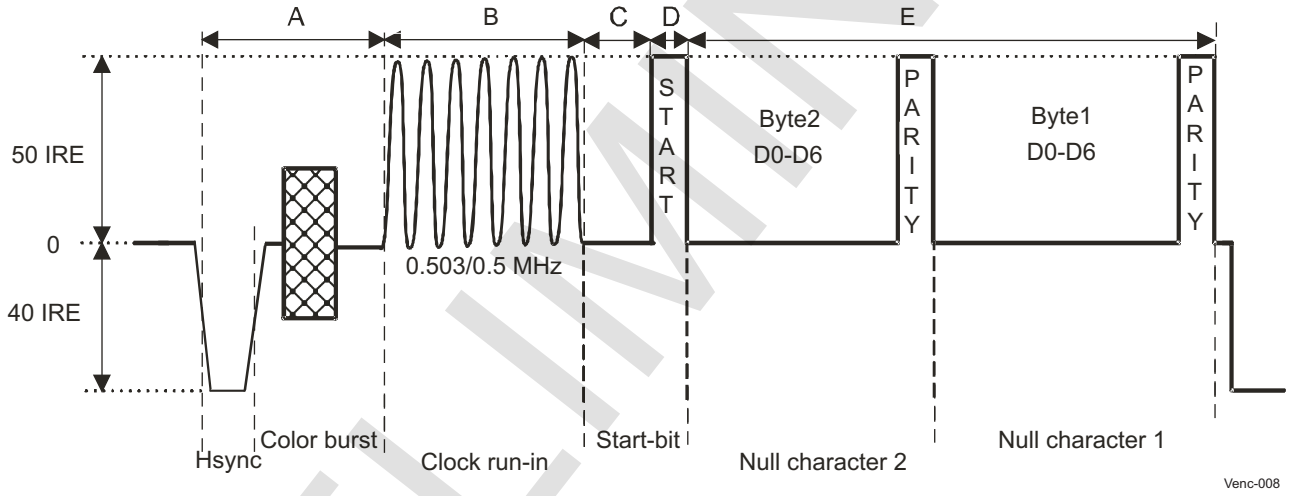

Table 10-709. Closed-Caption Standard Timing Values

Intervals	Description	Timing Values for Encoding			Timing Values for Decoding		
		Minimal	Nominal	Maximal	Lower Bound	Nominal	Upper Bound
A	HSYNC to clock running	10.250 µs	10.500 µs	10.750 µs	10.000 µs	10.500 µs	11.000 µs
B	Clock running		12.910 µs			12.910 µs	
C	Clock running to third start bit		3.972 µs			3.972 µs	
D	Start bit		1.986 µs			1.986 µs	
E	Data characters		31.778 µs			31.778 µs	

NOTE:

- The interval A is controlled by the VENC_LN_SEL[25:16] LN21_RUNIN bit field.
- The interval B is controlled by VENC_CC_CARR_WSS_CARR[15:0] FCC bit field.

All timing values listed in Table 10-709 are measured from the mid-point (half amplitude) on all edges.

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For a complete description of closed-caption standard including CGMS-A copy protection, see the CEA-608-x standard.

10.6.4.5.2 Wide-Screen Signaling (WSS) Encoding

The encoder can embed data, encoded in accordance with the IEC61880 and ITU-R 1119 data insertion standard, within the vertical blanking interval.

The encoder supports WSS data insertion on line 20 of every frame in the NTSC format. WSS data insertion is enabled by activating the VENC_L21_WC_CTL[14:13] EVEN_ODD_EN bit and by programming the VENC_BSTAMP_WSS_DATA[27:8] WSS_DATA bit field.

The running clock frequency is controlled by the VENC_CC_CARR_WSS_CARR[31:16] FWSS bit field. The wide-screen signaling running clock common frequencies are detailed in Table 10-710

Table 10-710. Wide-Screen Signaling RunClock Frequency Settings

	NTSC-601	PAL-601	NTSC Square Pixel	PAL Square Pixel
VENC_CC_CARR_WSS_CARR[31:16] FWSS bit field value	0x043F	0x2F72	0x04AC	0x2B6D

To select the line where the WSS data are encoded, program the VENC_L21_WC_CTL[12:8] LINE bit field.

CAUTION

The setting of the LINE[12:8] bit field value depends on the video standard:

- PAL mode: Because there is a one-line offset, program the desired line number – 1. The recommended value on line 23 is 0x16 + 1 = 0x17. The default value is 0x14 + 1 = 0x15 (line 21).
- NTSC mode: Because there is a four-line offset, program the desired line number – 4. The recommended value on line 20 is 0x10 + 4 = 0x14. The default value is 0x14 + 4 = 0x18 (line 24).

The WSS encoding block assumes that a full 10-bit video range is used to determine the 70 percent of peak-white amplitude of a logic-1 bit. The encoder also supports WSS data insertion on line 23 in the PAL format. Both waveforms are shown in Figure 10-186.

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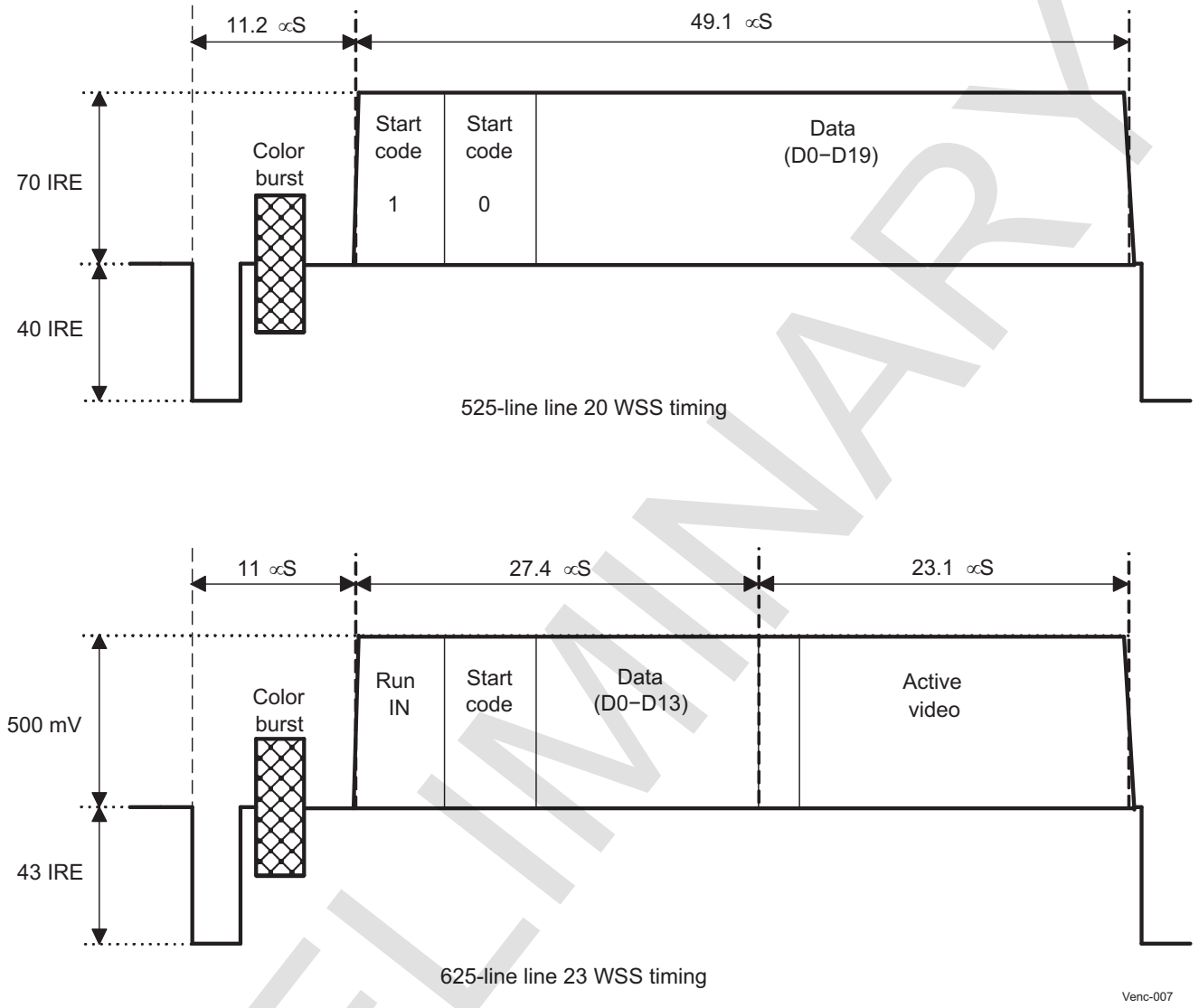
Figure 10-186. WSS Timing



10.6.4.6 Video DAC

NOTE: The VDAC function is not supported.

Figure 10-187 shows the architecture of the 10-bit video DAC.

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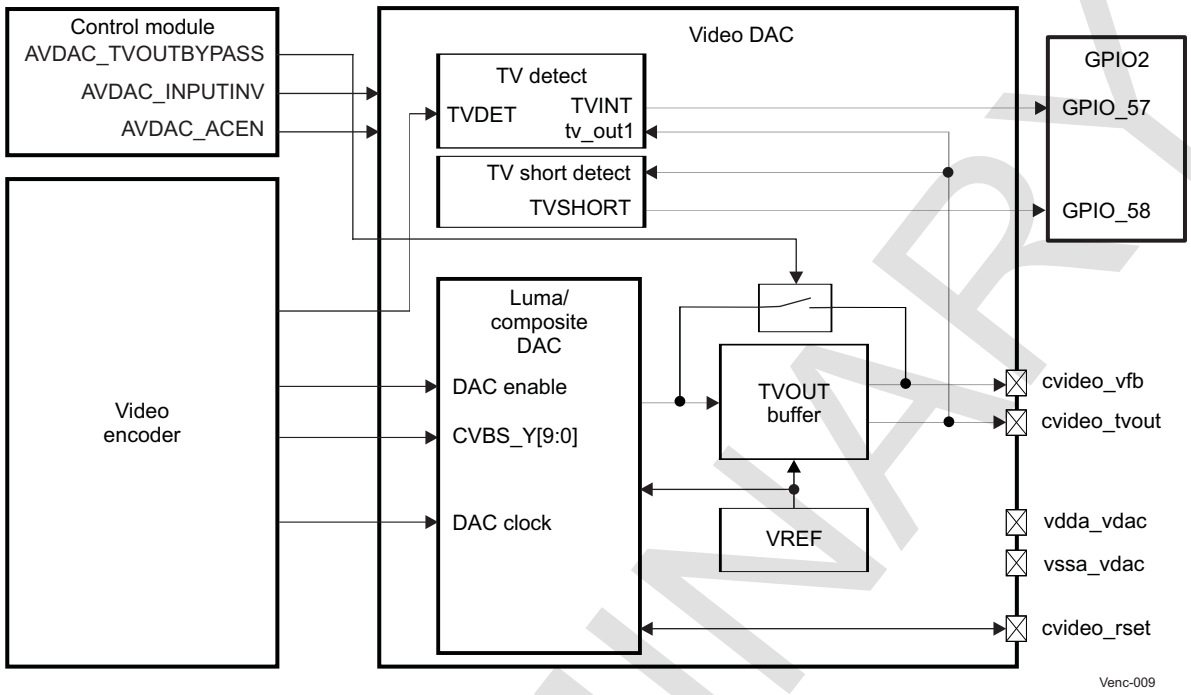
Figure 10-187. 10-Bit Video DAC Architecture



The display subsystem provides the necessary control signals to interface the memory frame buffer directly to external displays (TV sets). A 10-bit current steering DAC is used to generate the video analog signal. The video mode DAC also includes the TV detection/disconnection and power-down mode features.

10.6.4.6.1 Video DC/AC Coupled TV Load

The 10-bit video DAC supports both dc-coupled and ac-coupled TV loads. The CONTROL.CONTROL_AVDAC[31] AVDAC_ACEN bit is used to define which output coupling is used. This bit is the first one to be programed according to the TV load on the PCB board.

NOTE: When dc coupling is used, note that there is a 385-mV dc offset at the TVOUT output.

10.6.4.6.2 TV Detection/Disconnection Pulse Generation and Use

10.6.4.6.2.1 TV Detection/Disconnection Pulse Generation

The TV detect block is an integral part of the video DAC module.

NOTE:

- The TV detection/disconnection feature is supported on the video DAC.
- The TV disconnection feature is recommended for power saving purpose. The TV detection/disconnection is only operational when video out is active. Therefore to detect cable connection automatically, it is necessary to periodically activate the video out to test for cable presence.

This block compares the output (*cvideo_tvout*) to reference voltage, to sense the condition of the load. To operate, the TV detect requires two digital signals, TVACEN and TVDET. The

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TVACEN signal indicates to both TVOUT buffer and the TV detect circuit if the load is ac or dc coupling to adjust accordingly. TVDET is a digital pulse at the frequency of the TV sync pulses. The operation of the circuit is based on the difference in voltage levels in the output of the buffer depending of the load status. The TV detect block compares the output against a couple of references and the result is latched at the start of every sync pulse. The status is read later in with the TVDET pulse rising edge.

The following registers are used to set the TV detection/disconnection pulse:

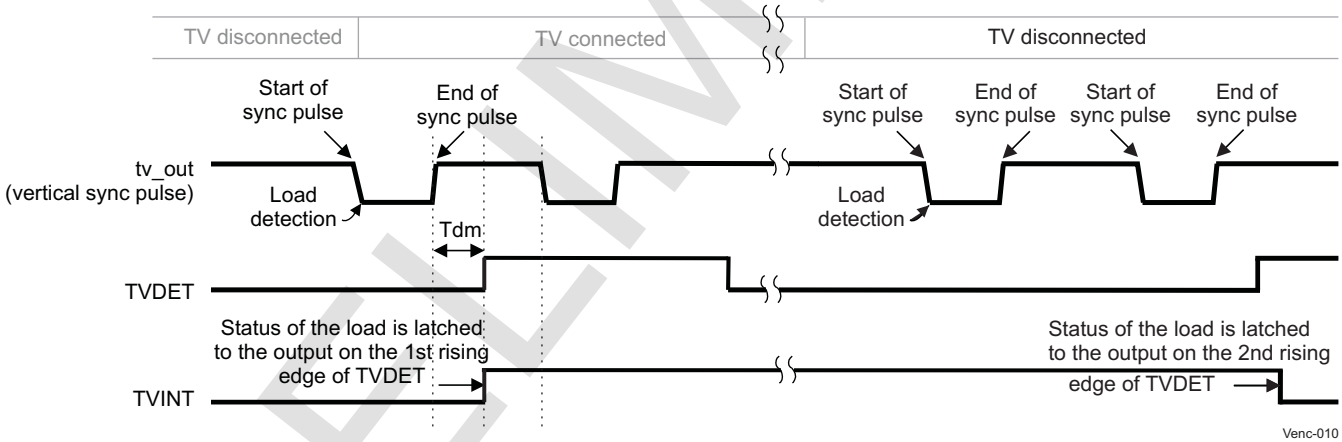
- The VENC_TVDETGP_INT_START_STOP_X register defines which pixels are used to start and stop the pulse inside their respective line.
- The VENC_TVDETGP_INT_START_STOP_Y register defines which lines are used to start and stop the pulse.
- The VENC_GEN_CTRL[0] EN bit enables or disables the TVDET pulse (0: Disable; 1: Enable).
- The VENC_GEN_CTRL[16] TVDP bit sets the TVDET pulse polarity (0: Active low; 1: Active high).

10.6.4.6.2.2 Recommended TV Detection/Disconnection Pulse Waveform

To enable the detection/disconnection of the load, the circuit requires that the TVDET pulse resembles the following waveform. By using the video encoder registers, the TVDET pulse polarity, start and stop is programmable. The only critical parameter is Tdm, which should be longer than the delay through the DAC and TVOUT buffer, which is at least 750 ns.

If dc-coupling is selected, the TVINT output signal for TV detection is latched at the rising edge of the first TVDET signal but the TVINT output signal for TV disconnection is latched after the next rising edge of the TVDET signal that happens during the next VSYNC timing. Figure 10-188 shows the waveforms for the dc-coupling TV detect pulse (TVDET) when load is connected and disconnected.

Figure 10-188. DC-Coupling TV Detect Waveforms for TV Connected and Disconnected



If ac-coupling is selected, the TVINT output signal for TV detection is latched after the next rising edge of the TVDET signal that happens during the next VSYNC timing but the TVINT output signal for TV disconnection is latched at the rising edge of the first TVDET signal. Figure 10-189 shows the waveforms for the ac-coupling TV detect pulse (TVDET) when load is connected and disconnected.

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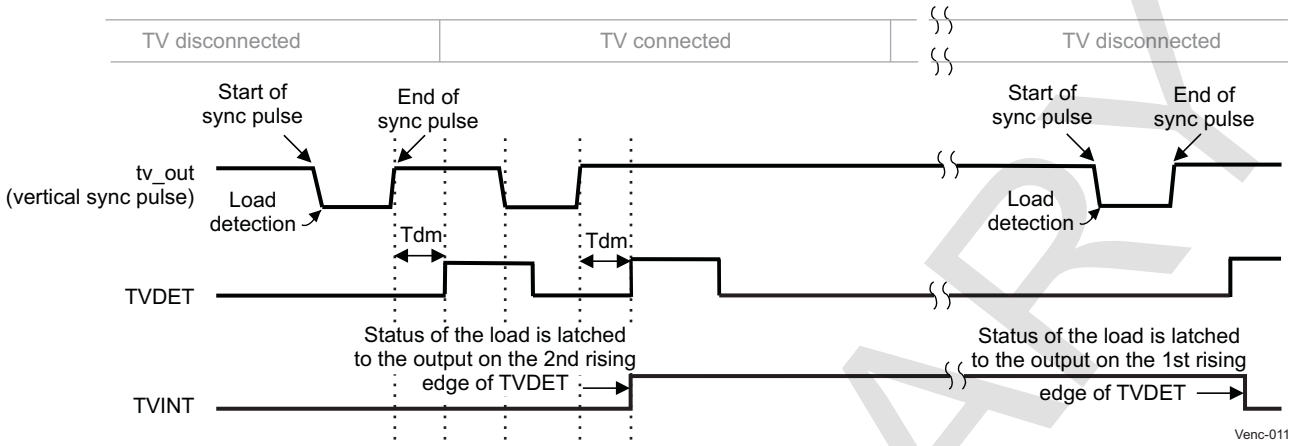
Figure 10-189. AC-Coupling TV Detect Waveforms for TV Connected and Disconnected



NOTE:

- When setting the VENC_TVDETGP_INT_START_STOP_X register, software users must ensure that the TVDET signal is in the active area. To avoid any problem, the TVDET signal must not be longer than one line.
- The activation of the TVDET signal will not have a visual impact on the *cvideo_tvout* output signal.

10.6.4.6.2.3 TV Detection/Disconnection Use

The TV-detection/TV-disconnection is based on the difference in voltage levels in the output of the TV buffer depending on the load status. The operation is slightly different for ac and for dc operation. For dc operation, the *cvideo_tvout* voltage is compared against a voltage reference that makes the comparator trigger in each sync pulse while the load is connected. For ac operation, the *cvideo_tvout* voltage is compared against a voltage reference that makes the comparator trigger in each sync pulse while the load is disconnected. In both cases, the TVINT output signal produces a logic 1 when a load is connected and a logic 0 when a load is disconnected.

For dc-coupling mode, see Figure 10-190 and for ac-coupling mode, see Figure 10-191

NOTE: Because the video DAC and the video encoder must be awake for connection detection, consider that the video DAC can take up to 10 µs to wake up.

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Figure 10-190. GPIO Signal Waveform Proposal for TV Detection/Disconnection in DC-Coupling Mode

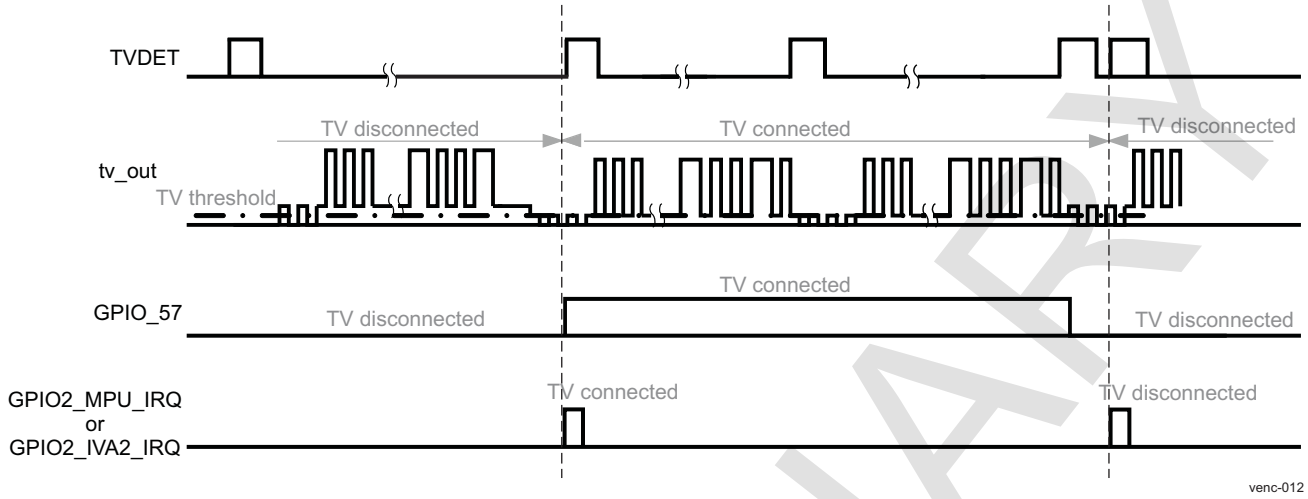
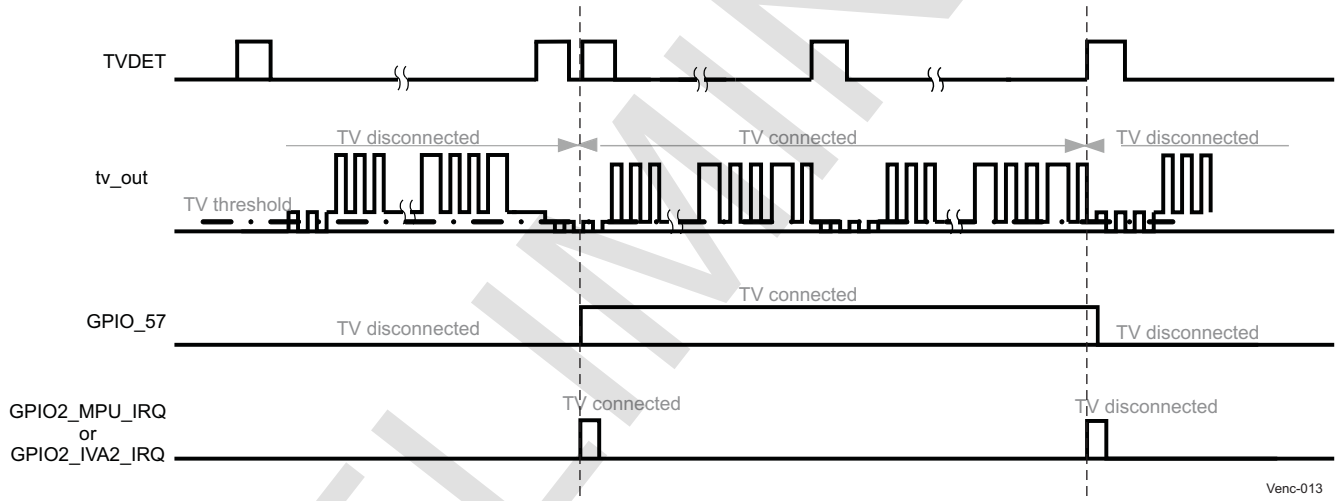


Figure 10-191. GPIO Signal Waveform Proposal for TV Detection/Disconnection in AC-Coupling Mode



10.6.4.6.3 TV Short Detection

A TV short-detection circuit, which can detect a short circuit condition at cvideo_tvout output during the vertical sync pulse, is integrated in the video DAC module (see Figure 10-187).

When the output is shorted to ground, the TVSHORT signal turns to logic high. The TVSHORT signal is internally mapped in the device to the GPIO_58 signal (channel 26 of the GPIO2 module), which allows interrupt generation on this channel (see Chapter 25, *General-Purpose Interface*). TV short detection is valid after two video frames pass with the short/no-short condition.

TV short detection has priority over TV load detection (see Section 10.6.4.6.2.2, *TV Detection/Disconnection Pulse Generation and Use*). Whenever a short is detected (with load or no-load), TVINT output is masked as long as the short remains. When released, TV load detection resumes (see Section 10.6.4.6.2.2, *TV Detection/Disconnection Pulse Generation and Use*).

CAUTION

If TV short is detected, the video DAC must be powered down by setting the DSS.DSS_CTRL[5] DAC_POWERDN_BGZ bit to 0.

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10.6.4.6.4 Video DAC Normal Mode

The normal mode of operation (DAC + TVOUT buffer) is the default mode of the video DAC, with the CONTROL.CONTROL_AVDAC[30] AVDAC_TVOUTBYPASS bit set to 0 at device reset. The output of the DAC is internally connected to the TVOUT buffer, which can drive the composite video signal to 75 Ω load directly. For information about external connectivity, see Section 10.6.2, *Video Encoder Environment*.

In normal mode, higher input values of the DAC code result in lower output voltage levels by default, because of the inverting configuration of the TVOUT buffer. The CONTROL.CONTROL_AVDAC[29] AVDAC_INPUTINV bit provides inversion control over the data input of the DAC, to allow alignment of the output voltage with VENC data. If the AVDAC_INPUTINV bit is set to 1, the DAC input code is inverted. Thus, higher DAC code values provided by the VENC result in higher output voltage.

10.6.4.6.5 Video DAC Bypass Mode

The 10-bit video DAC has a TVOUT buffer bypass mode that turns off the TVOUT buffer and redirects directly the DAC output to the *cvideo_vfb* pin.

This bypass mode is activated by setting the CONTROL.CONTROL_AVDAC[30] AVDAC_TVOUTBYPASS bit to 1. The reset value of the CONTROL.CONTROL_AVDAC[30] AVDAC_TVOUTBYPASS bit is 0 (that is, the TVOUT buffer is not bypassed).

NOTE: In bypass mode:

- *cvideo_rset* pin requires a Rset resistor connected to the ground. The typical value of the Rset resistor is 10000 Ω.
- *cvideo_vfb* pin require a Rload resistor connected to the ground. The typical value of the Rload resistor is 1500 Ω.

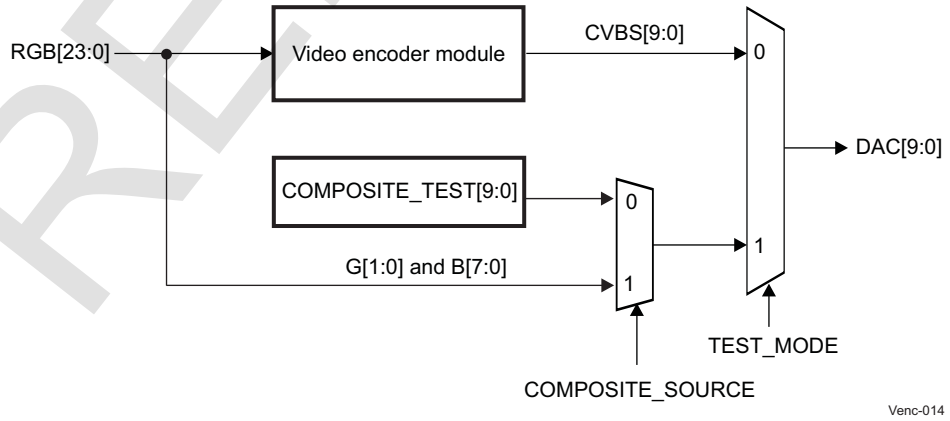
CAUTION

- The TV detect feature is not available in bypass mode.
- In bypass mode, an external amplifier is needed on the *cvideo_vfb* pin.

10.6.4.6.6 Video DAC Test Mode

10-bit external or internal datas values can be used to stimulate the DAC in debug, see Figure 10-192.

Figure 10-192. DAC Test Mode in Composite Video Mode



- Setting to 0x1 the VENC_OUTPUT_CONTROL[4] TEST_MODE bit will place the DAC under test.
- By setting the value of the VENC_OUTPUT_CONTROL[6] COMPOSITE_SOURCE bit to:
  - 0x0: the DAC input is coming from VENC_OUTPUT_TEST[9:0] COMPOSITE_TEST bit field
  - 0x1: the DAC input is coming from the display controller G[1:0], B[7:0]. To perform this

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configuration, the video encoder shall be configure to generate correct timing signals with the display controller even if the video encoder is bypassed from the data path perspective.

10.6.4.6.7 Video DAC Power Management

After device reset, the DSS.DSS_CTRL[5] DAC_POWERDN_BGZ bit is set to 0, and the video DAC is in power-down state.

Table 10-711 lists the possible power-management configurations and the corresponding register settings.

Table 10-711. Video DAC Power-Management Configurations

Power Management Controls				
DSS_CTRL[5] DAC_POWERDN_BGZ	**VENC_OUTPUT_CONTROL[1] COMPOSITE_ENABLE**	**CONTROL_AVDAC[30] AVDAC_TVOUTBYPASS**	**CONTROL_AVDAC[31] AVDAC_ACEN**	**Power State**
0	x	x	x	Total power down. Bandgap powered down.
1	0	x	x	Standby (analog in power down except bandgap/LDO)
1	1	0	0	Full power up in DC normal mode
1	1	0	1	Full power up in AC normal mode
1	1	1	x	Full power up in TVOUT bypass mode (DAC-only mode)

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10.6.5 Video Encoder Programming Guide

10.6.5.1 Video Encoder Low-level Programming Models

10.6.5.1.1 Surrounding Modules Global Initialization

This section identifies the requirements of initializing the surrounding modules when the video emodule is to be used for the first time after a device reset. This initialization of the surrounding modules is based on the integration and environment of the video encoder (for more information, see Section 10.6.2 and Section 10.6.3).

Table 10-712. Global Initialization of Surrounding Modules

Surrounding Modules	Comments
PRCM	Module interface and functional clocks must be enabled. See Chapter 3, *Power, Reset, and Clock Management*
Control module	Module-specific pad muxing and configuration must be set in the control module. See Chapter 18, *Control Module*.
Display controller	See Section 10.2, *Display Controller,* for more information about the configuration.

10.6.5.1.2 Video Encoder Global Initialization

10.6.5.1.2.1 Main Sequence—Start Video Encoder

Table 10-713 details the procedure to initialize the video encoder after a power-on or software reset.

Table 10-713. Start Video Encoder

Step	Register/Bit Field/Programming Model	Value
Perform a video encoder reset.	See Section 10.6.5.1.2.3.	
Save the DSS IRQ enable register value (DSS interrupts context).	DISPC_IRQENABLE	
Reset all DSS IRQ.	DISPC_IRQENABLE	0x00
Configure the video encoder registers for PAL 601 or NTSC 601.	See Table 10-720.	0x--
Set the input video source and format.	VENC_F_CONTROL	See Table 10-720.
Set the synchronization modes.	VENC_SYNC_CTRL	See Table 10-720.
Configure the TV connection detection (optional).	See Section 10.6.5.1.2.4.	
Enable the composite video signal output.	See Section 10.6.5.1.2.6.	
Enable the display controller pipeline	See the display controller programming guide.	
Wait until the first VSYNC pulse signal.		
Clear the SYNCLOSTDIGITAL interrupt.	DISPC_IRQSTATUS[15] SYNCLOSTDIGITAL	0x1
Restore the DSS IRQ enable register.	DISPC_IRQENABLE	0x--

10.6.5.1.2.2 Main Sequence—Stop Video Encoder

Table 10-714 details the procedure to stop the output of the composite signal.

Table 10-714. Start Video Encoder

Step	Register/Bit Field/Programming Model	Value
Perform TV disconnection detection (optional).	See Section 10.6.5.1.2.5.	
Disable the composite video signal output.	See Section 10.6.5.1.2.7.	

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10.6.5.1.2.3 Subsequence—Video Encoder Software Reset

Table 10-715 details the reset procedure.

Table 10-715. Reset Video Encoder

Step	Register/Bit Field/Programming Model	Value
Activate reset.	VENC_F_CONTROL[8] RESET	0x1
Wait until reset is complete.	VENC_F_CONTROL[8] RESET	0x0

NOTE: Before changing the standard (NTSC or PAL) and related registers, a software reset is required to properly initialize the VENC module.

10.6.5.1.2.4 Subsequence—TV Connection Detection

Table 10-716 details the TV connection detection procedure.

Table 10-716. TV Connection Detection Subsequence

Step	Register/Bit Field/Programming Model	Value
Set the pixel TV detection start and stop value.	VENC_TVDETGP_INT_START_STOP_X	0x--
Set the line TV detection start and stop value.	VENC_TVDETGP_INT_START_STOP_Y	0x--
Set the polarity of TV detection.	VENC_GEN_CTRL[16] TVDP	0x--
Enable TV detection.	VENC_GEN_CTRL[0] EN	0x1
Enable the composite video signal output.	See Section 10.6.5.1.2.6.	
Wait until TVINT = 1.	See the GPIO programming guide.	

CAUTION

- If ac coupling is selected, two TVDET pulses are required to set high the TVINT signal. Due to the internal logic of the video DAC, the TVINT signal is generated after the next positive edge of the TVDET signal that happens during the next VSYNC timing.
- If dc coupling is selected, only one TVDET pulse is required to set high the TVINT signal.

10.6.5.1.2.5 Subsequence—TV Disconnection Detection

Table 10-717 details the TV disconnection detection procedure.

Table 10-717. TV Disconnection Detection Subsequence

Step	Register/Bit Field/Programming Model	Value
Set the pixel TV detection start and stop value.	VENC_TVDETGP_INT_START_STOP_X	0x--
Set the line TV detection start and stop value.	VENC_TVDETGP_INT_START_STOP_Y	0x--
Set the polarity of TV detection.	VENC_GEN_CTRL[16] TVDP	0x--
Enable TV disconnection.	VENC_GEN_CTRL[0] EN	0x1
Wait until TVINT = 0.	See the GPIO programming guide.	

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CAUTION

- If dc coupling is selected, two TVDET pulses are required to set low the TVINT signal. Because of the internal logic of the video DAC, the TVINT signal is generated after the next positive edge of the TVDET signal that happens during the next VSYNC timing.
- If ac coupling is selected, only one TVDET pulse is required to set low the TVINT signal.

10.6.5.1.2.6 Subsequence—Enable Video Composite Signal Output

Table 10-718 details the procedure to enable the video composite signal output.

Table 10-718. Enable Video Composite Signal Output

Step	Register/Bit Field/Programming Model	Value
Enable the composite video signal output.	VENC_OUTPUT_CONTROL	0x0000 000A
Power up the vdda_vdac voltage for VDAC and the TVOUT buffer.		

10.6.5.1.2.7 Subsequence—Disable Video Composite Signal Output

Table 10-719 details the procedure to enable the video composite signal output.

Table 10-719. Disable Video Composite Signal Output

Step	Register/Bit Field/Programming Model	Value
Disable the composite video signal output.	VENC_OUTPUT_CONTROL	0x00000000
Power down the vdda_vdac voltage for VDAC and the TVOUT buffer.		

10.6.6 Video Encoder Use Case and Tips

10.6.6.1 Video Encoder Register Settings

Table 10-720 lists the register values to use in typical video encoder applications.

These values are validated programming values only for NTSC 601 and PAL 601 standards with a TV display resolution of 720*488 and 720*576, respectively.

Table 10-720. Video Encoder Register Programming Values

Register Name	NTSC 601	PAL 601
VENC_F_CONTROL	0x00000000	0x00000000
VENC_VIDOUT_CTRL	0x00000001	0x00000001
VENC_SYNC_CTRL	0x00008040	0x00000040
VENC_LLEN	0x00000359	0x0000035F
VENC_FLENS	0x0000020C	0x00000270
VENC_HFLTR_CTRL	0x00000000	0x00000000
VENC_CC_CARR_WSS_CARR	0x043F2631	0x2F7225ED
VENC_C_PHASE	0x00000000	0x00000000
VENC_GAIN_U	0x00000102	0x00000111
VENC_GAIN_V	0x0000016C	0x00000181
VENC_GAIN_Y	0x0000012F	0x00000140
VENC_BLACK_LEVEL	0x00000043	0x0000003B

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Table 10-720. Video Encoder Register Programming Values (continued)

Register Name	NTSC 601	PAL 601
VENC_BLANK_LEVEL	0x00000038	0x0000003B
VENC_X_COLOR	0x00000007	0x00000007
VENC_M_CONTROL	0x00000001	0x00000002
VENC_BSTAMP_WSS_DATA	0x00000038	0x0000003F
VENC_S_CARR	0x21F07C1F	0x2A098ACB
VENC_LINE21	0x00000000	0x00000000
VENC_LN_SEL	0x01310011	0x01290015
VENC_L21_WC_CTL	0x0000F003	0x0000F603
VENC_HTRIGGER_VTRIGGER	0x00000000	0x00000000
VENC_SAVID_EAVID	0x069300F4	0x06A70108
VENC_FLEN_FAL	0x0016020C	0x00180270
VENC_LAL_PHASE_RESET	0x00060107	0x00040135
VENC_HS_INT_START_STOP_X	0x008E0350	0x00880358
VENC_HS_EXT_START_STOP_X	0x000F0359	0x000F035F
VENC_VS_INT_START_X	0x01A00000	0x01A70000
VENC_VS_INT_STOP_X_VS_INT_START_Y	0x020701A0	0x000001A7
VENC_VS_INT_STOP_Y_VS_EXT_START_X	0x01AC0024	0x01AF0000
VENC_VS_EXT_STOP_X_VS_EXT_START_Y	0x020D01AC	0x000101AF
VENC_VS_EXT_STOP_Y	0x00000006	0x00000025
VENC_AVID_START_STOP_X	0x03480078	0x03530083
VENC_AVID_START_STOP_Y	0x02060024	0x026C002E
VENC_FID_INT_START_X_FID_INT_START_Y	0x0001008A	0x0001008A
VENC_FID_INT_OFFSET_Y_FID_EXT_START_X	0x01AC0106	0x002E0138
VENC_FID_EXT_START_Y_FID_EXT_OFFSET_Y	0x01060006	0x01380001
VENC_TVDETGP_INT_START_STOP_X	0x00140001	0x00140001
VENC_TVDETGP_INT_START_STOP_Y	0x00010001	0x00010001
VENC_GEN_CTRL	0x00F90000	0x00FF0000
VENC_OUTPUT_CONTROL	0x0000000A	0x0000000A
VENC_OUTPUT_TEST	0x00000000	0x00000000

NOTE: The following display controller fields must be programmed to the NTSC 601 video standard:

- DISPC_SIZE_DIG[10:0] PPL = 720 - 1 = 719 = 0x2CF
- DISPC_SIZE_DIG[26:16] LPP = (488/2) - 1 = 243 = 0xF3

The following display controller fields must be programmed to the PAL 601 video standard:

- DISPC_SIZE_DIG[10:0] PPL = 720 - 1 = 719 = 0x2CF
- DISPC_SIZE_DIG[26:16] LPP = (576/2) - 1 = 287 = 0x11F

For both standard, the base addresses should be handle as follow:

- DISPC_GFX_BA0 or DISPC_VIDn_BA0 = Base address of even bit field data
- DISPC_GFX_BA1 or DISPC_VIDn_BA1 = Base address of odd bit field data

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10.6.7 Video Encoder Register Manual

CAUTION

The main access to all Video Encoder registers is through the L3 interconnect.

The access through L4_PER interconnect is provided for back software compatibility.

10.6.7.1 Video Encoder Instance Summary

Table 10-721. Video Encoder Instance Summary

Module Name	L3 Base Address	L4_PER Base Address	Size
VENC	0x5800 3000	0x4804 3000	4 KB

CAUTION

The VENC registers have no register data width access restriction and can be accessed in 8-bit, 16-bit and 32-bit access.

10.6.7.2 Video Encoder Registers

10.6.7.2.1 Video Encoder Register Summary

Table 10-722. Video Encoder Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	VENC L3 Physical Address	VENC L4_PER Physical Address
VENC_REV_ID	R	32	0x0000 0000	0x5800 3000	0x4804 3000
VENC_STATUS	R	32	0x0000 0004	0x5800 3004	0x4804 3004
VENC_F_CONTROL	RW	32	0x0000 0008	0x5800 3008	0x4804 3008
VENC_VIDOUT_CTRL	RW	32	0x0000 0010	0x5800 3010	0x4804 3010
VENC_SYNC_CTRL	RW	32	0x0000 0014	0x5800 3014	0x4804 3014
VENC_LLEN	RW	32	0x0000 001C	0x5800 301C	0x4804 301C
VENC_FLENS	RW	32	0x0000 0020	0x5800 3020	0x4804 3020
VENC_HFLTR_CTRL	RW	32	0x0000 0024	0x5800 3024	0x4804 3024
VENC_CC_CARR_WSS_CARR	RW	32	0x0000 0028	0x5800 3028	0x4804 3028
VENC_C_PHASE	RW	32	0x0000 002C	0x5800 302C	0x4804 302C
VENC_GAIN_U	RW	32	0x0000 0030	0x5800 3030	0x4804 3030
VENC_GAIN_V	RW	32	0x0000 0034	0x5800 3034	0x4804 3034
VENC_GAIN_Y	RW	32	0x0000 0038	0x5800 3038	0x4804 3038
VENC_BLACK_LEVEL	RW	32	0x0000 003C	0x5800 303C	0x4804 303C
VENC_BLANK_LEVEL	RW	32	0x0000 0040	0x5800 3040	0x4804 3040
VENC_X_COLOR	RW	32	0x0000 0044	0x5800 3044	0x4804 3044
VENC_M_CONTROL	RW	32	0x0000 0048	0x5800 3048	0x4804 3048

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Table 10-722. Video Encoder Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	VENC L3 Physical Address	VENC L4_PER Physical Address
VENC_BSTAMP_WSS_DATA	RW	32	0x0000 004C	0x5800 304C	0x4804 304C
VENC_S_CARR	RW	32	0x0000 0050	0x5800 3050	0x4804 3050
VENC_LINE21	RW	32	0x0000 0054	0x5800 3054	0x4804 3054
VENC_LN_SEL	RW	32	0x0000 0058	0x5800 3058	0x4804 3058
VENC_L21_WC_CTL	RW	32	0x0000 005C	0x5800 305C	0x4804 305C
VENC_HTRIGGER_VTRIGGER	RW	32	0x0000 0060	0x5800 3060	0x4804 3060
VENC_SAVID_EAVID	RW	32	0x0000 0064	0x5800 3064	0x4804 3064
VENC_FLEN_FAL	RW	32	0x0000 0068	0x5800 3068	0x4804 3068
VENC_LAL_PHASE_RESET	RW	32	0x0000 006C	0x5800 306C	0x4804 306C
VENC_HS_INT_START_STOP_X	RW	32	0x0000 0070	0x5800 3070	0x4804 3070
VENC_HS_EXT_START_STOP_X	RW	32	0x0000 0074	0x5800 3074	0x4804 3074
VENC_VS_INT_START_X	RW	32	0x0000 0078	0x5800 3078	0x4804 3078
VENC_VS_INT_STOP_X_VS_INT_START_Y	RW	32	0x0000 007C	0x5800 307C	0x4804 307C
VENC_VS_INT_STOP_Y_VS_EXT_START_X	RW	32	0x0000 0080	0x5800 3080	0x4804 3080
VENC_VS_EXT_STOP_X_VS_EXT_START_Y	RW	32	0x0000 0084	0x5800 3084	0x4804 3084
VENC_VS_EXT_STOP_Y	RW	32	0x0000 0088	0x5800 3088	0x4804 3088
VENC_AVID_START_STOP_X	RW	32	0x0000 0090	0x5800 3090	0x4804 3090
VENC_AVID_START_STOP_Y	RW	32	0x0000 0094	0x5800 3094	0x4804 3094
VENC_FID_INT_START_X_FID_INT_START_Y	RW	32	0x0000 00A0	0x5800 30A0	0x4804 30A0
VENC_FID_INT_OFFSET_Y_FID_EXT_START_X	RW	32	0x0000 00A4	0x5800 30A4	0x4804 30A4
VENC_FID_EXT_START_Y_FID_EXT_OFFSET_Y	RW	32	0x0000 00A8	0x5800 30A8	0x4804 30A8
VENC_TVDETGP_INT_START_STOP_X	RW	32	0x0000 00B0	0x5800 30B0	0x4804 30B0
VENC_TVDETGP_INT_START_STOP_Y	RW	32	0x0000 00B4	0x5800 30B4	0x4804 30B4
VENC_GEN_CTRL	RW	32	0x0000 00B8	0x5800 30B8	0x4804 30B8
VENC_OUTPUT_CONTROL	RW	32	0x0000 00C4	0x5800 30C4	0x4804 30C4
VENC_OUTPUT_TEST	RW	32	0x0000 00C8	0x5800 30C8	0x4804 30C8

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10.6.7.2.2 Video Encoder Register Description

Table 10-723. VENC_REV_ID

Address Offset	0x0000 0000		
Physical Address	0x5800 3000 0x4804 3000	**Instance**	VENC_L3 VENC_PER_L4
Description	Revision ID for the encoder		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP Revision	R	See (1)

(1) TI internal data

Table 10-724. Register Call Summary for Register VENC_REV_ID

Video Encoder

- Video Encoder Register Summary: [0]

Table 10-725. VENC_STATUS

Address Offset	0x0000 0004		
Physical Address	0x5800 3004 0x4804 3004	**Instance**	VENC_L3 VENC_PER_L4
Description	STATUS		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																											CCE	CCO	FSQ			

Bits	Field Name	Description	Type	Reset
31:5	RESERVED		R	0x0000000
4	CCE	Closed Caption Status for Even Field. This bit is set immediately after the data in registers LINE21_E0 and LINE21_E1 have been encoded to closed caption. This bit is reset when both of these registers are written.	R	0
3	CCO	Closed Caption Status for Odd Field. This bit is set immediately after the data in registers LINE21_O0 and LINE21_O1 have been encoded to closed caption. This bit is reset when both of these registers are written.	R	0
2:0	FSQ	Field Sequence ID. For PAL, all three FSQ[2:0] are used whereas for NTSC only FSQ[1:0] is meaningful. Furthermore, FSQ[0] represents ODD field when it is '0' and EVEN field when it is '1'. Read 0x0: ODD field Read 0x1: EVEN field	R	0x0

Table 10-726. Register Call Summary for Register VENC_STATUS

Video Encoder

- Closed Caption Encoding: [0] [1] [2] [3]
- Video Encoder Register Summary: [4]

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Table 10-727. VENC_F_CONTROL

Address Offset	0x0000 0008		
Physical Address	0x5800 3008 0x4804 3008	**Instance**	VENC_L3 VENC_PER_L4
Description	This register specifies the input video source and format		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							RESET	SVDS		RGBF	BCOLOR			FMT	

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	RESET	RESET the encoder 0x0: No effect 0x1: Reset the encoder, after reset, this bit is automatically set to zero.	RW	0
7:6	SVDS	Select Video Data Source. 0x0: Use external video source 0x1: Use internal Color BAR 0x2: Use background color 0x3: Reserved	RW	0x2
5	RGBF	RGB /YCrCb input coding range 0x0: The input RGB data are in binary format with coding range 0-255 The input YCrCb data are in binary format with coding range 0-255 0x1: The input RGB data are in binary format with coding range 16-235 The input YCrCb data are in binary format conforming to ITU-601 standard	RW	0
4:2	BCOLOR	Background color select 0x0: 0x1: 0x2: 0x3: 0x4: 0x5: 0x6: 0x7:	RW	0x1
1:0	FMT	These two bits specify the video input data stream format and timing 0x0: 24-bit 4:4:4 RGB 0x1: 24-bit 4:4:4 0x2: 16-bit 4:2:2 0x3: 8-bit ITU-R 656 4:2:2	RW	0x3

Table 10-728. Register Call Summary for Register VENC_F_CONTROL

Video Encoder

- Data Manager: [0]
- Test Pattern Generation: [1] [2] [3]
- Video Encoder Global Initialization: [4] [5] [6]
- Video Encoder Register Settings: [7]
- Video Encoder Register Summary: [8]

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Table 10-729. VENC_VIDOUT_CTRL

Address Offset	0x0000 0010		
Physical Address	0x5800 3010 0x4804 3010	**Instance**	VENC_L3 VENC_PER_L4
Description	Encoder output clock		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															MHZ_27_54

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	MHZ_27_54	Encoder output clock 0x0: 54 MHz, 4x oversampling 0x1: 27MHz, 2x oversampling, the last 2x oversampling filter bypassed	RW	0

Table 10-730. Register Call Summary for Register VENC_VIDOUT_CTRL

Video Encoder

- Video Encoder Register Settings: [0]
- Video Encoder Register Summary: [1]

Table 10-731. VENC_SYNC_CTRL

Address Offset	0x0000 0014		
Physical Address	0x5800 3014 0x4804 3014	**Instance**	VENC_L3 VENC_PER_L4
Description	SYNC Control register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																FREE	ESAV	IGNP	NBLNKS	VBLKM		HBLKM		M_S	FID_POL	RESERVED		VS_POL	HS_POL	RESERVED	FHVMOD

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	reserved_5	R	0x0000
15	FREE	Free running 0x0: Free running disabled 0x1: Free running enabled. HSYNC and VSYNC are ignored	RW	1
14	ESAV	Enable to detect F and V bits only on EAV in ITU-R 656 input mode 0x0: Detection of F and V bits on both EAV and SAV 0x1: Detection of F and V bits only on EAV	RW	0
13	IGNP	Ignore protection bits in ITU-R 656 input mode 0x0: Protection bits are not ignored 0x1: Protection bits are ignored	RW	0

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Bits	Field Name	Description	Type	Reset
12	NBLNKS	Blank shaping	RW	0
		0x0: Blank shaping enabled		
		0x1: Blank shaping disabled		
11:10	VBLKM	Vertical blanking mode	RW	0x0
		0x0: Internal default blanking		
		0x1: Internal default blanking AND internal programmable blanking defined by FAL and LAL		
		0x2: Reserved		
		0x3: Reserved		
9:8	HBLKM	Horizontal blanking mode	RW	0x0
		0x0: Internal default blanking		
		0x1: Internal programmable blanking defined by SAVID and EAVID		
		0x2: External blanking defined by AVID		
		0x3: Reserved		
7	M_S	Encoder is master or slave of external sync	RW	0
		0x0: Sync master. Encoder outputs Vsync, Hsync, FID and AVID.		
		0x1: Sync slave. Encoder is synchronized to external Vsync, Hsync, FID and AVID.		
6	FID_POL	FID output polarity	RW	0
		0x0: ODD field = '0' EVEN field = '1'		
		0x1: ODD field = '1' EVEN field = '0'		
5:4	RESERVED		R	0x0
3	VS_POL	VS input polarity	RW	0
		0x0: VS is active high		
		0x1: VS is active low		
2	HS_POL	HS input polarity	RW	0
		0x0: HS is active high		
		0x1: HS is active low		
1	RESERVED		R	0
0	FHVMOD	FID extracted from external FID or HSYNC and VSYNC	RW	0
		0x0: External FID		
		0x1: Extracted from HSYNC and VSYNC		

Table 10-732. Register Call Summary for Register VENC_SYNC_CTRL

Video Encoder

- Video Encoder Global Initialization: [0]
- Video Encoder Register Settings: [1]
- Video Encoder Register Summary: [2]

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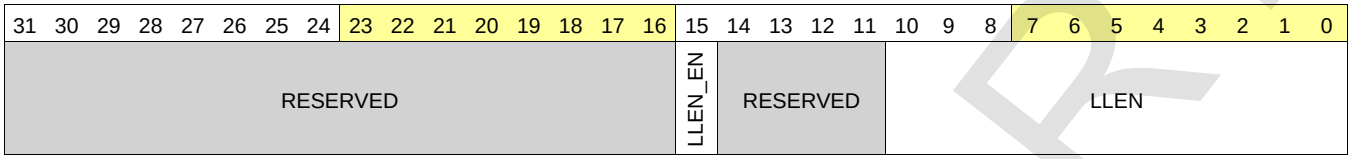
Table 10-733. VENC_LLEN

Address Offset	0x0000 001C		
Physical Address	0x5800 301C 0x4804 301C	**Instance**	VENC_L3 VENC_PER_L4
Description	LLEN		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15	LLEN_EN	LLEN_EN 0x0: disable 0x1: enable	RW	0
14:11	RESERVED		R	0x0
10:0	LLEN	LLEN[10:0] Line length or total number of pixels in a scan line including active video and blanking. Total number of pixels in a scan line = LLEN NOTE: A write to bit 11 of this bit field is illegal.	RW	0x359

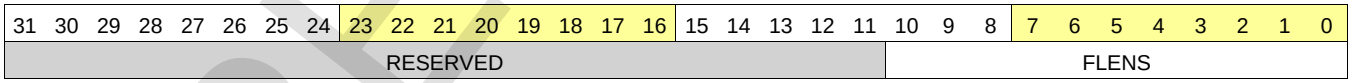
Table 10-734. Register Call Summary for Register VENC_LLEN

Video Encoder

- Video Encoder Register Settings: [0]
- Video Encoder Register Summary: [1]

Table 10-735. VENC_FLENS

Address Offset	0x0000 0020		
Physical Address	0x5800 3020 0x4804 3020	**Instance**	VENC_L3 VENC_PER_L4
Description	FLENS		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:11	RESERVED		R	0x000000
10:0	FLENS	The frame length or total number of lines in a frame including active video and blanking from the source image. Total number of lines in a frame from the source image = FLENS + 1	RW	0x20C

Table 10-736. Register Call Summary for Register VENC_FLENS

Video Encoder

- Video Encoder Register Settings: [0]
- Video Encoder Register Summary: [1]

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Table 10-737. VENC_HFLTR_CTRL

Address Offset	0x0000 0024		
Physical Address	0x5800 3024 0x4804 3024	**Instance**	VENC_L3 VENC_PER_L4
Description	HFLTR_CTRL		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													CINTP		YINTP

Bits	Field Name	Description	Type	Reset
31:3	RESERVED		R	0x0000 0000
2:1	CINTP	Chrominance interpolation filter control 0x0: The chrominance interpolation filter is enabled 0x1: The first section of the chrominance interpolation filter is bypassed 0x2: The second section of the chrominance interpolation filter is bypassed 0x3: Both sections of the filter are bypassed	RW	0x0
0	YINTP	Luminance interpolation filter control 0x0: The luminance interpolation filter is enabled 0x1: The luminance interpolation filter is bypassed	RW	0

Table 10-738. Register Call Summary for Register VENC_HFLTR_CTRL

Video Encoder

- Video Encoder Register Settings: [0]
- Video Encoder Register Summary: [1]

Table 10-739. VENC_CC_CARR_WSS_CARR

Address Offset	0x0000 0028		
Physical Address	0x5800 3028 0x4804 3028	**Instance**	VENC_L3 VENC_PER_L4
Description	Frequencie code control		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FWSS																FCC															

Bits	Field Name	Description	Type	Reset
31:16	FWSS	Wide screen signaling run-in code frequency control. For 50-Hz systems, FWSS = 2^{18} * 5 * 10^6/(LLEN * Fh), where LLEN = total number of pixels in a scan line Fh = line frequency.	RW	0x043F
15:0	FCC	Close caption run-in code frequency control. For 60-Hz system, FCC = 2^{18} * 0.5035 * 10^6/(LLEN * Fh) For 50-Hz systems, FCC = 2^{18} * 0.500 * 10^6/(LLEN * Fh), where LLEN = total number of pixels in a scan line Fh = line frequency.	RW	0x2631

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Table 10-740. Register Call Summary for Register VENC_CC_CARR_WSS_CARR

Video Encoder

- Closed Caption Encoding: [0] [1] [2]
- Wide-Screen Signaling (WSS) Encoding: [3] [4]
- Video Encoder Register Settings: [5]
- Video Encoder Register Summary: [6]

Table 10-741. VENC_C_PHASE

Address Offset	0x0000 002C		
Physical Address	0x5800 302C 0x4804 302C	**Instance**	VENC_L3 VENC_PER_L4
Description	C_PHASE		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								CPHS							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED		R	0x000000
7:0	CPHS	Phase of the encoded video color subcarrier (including the color burst) relative to H-sync. The adjustable step is 360/256 degrees.	RW	0x00

Table 10-742. Register Call Summary for Register VENC_C_PHASE

Video Encoder

- Subcarrier and Burst Generation: [0] [1] [2]
- Video Encoder Register Settings: [3]
- Video Encoder Register Summary: [4]

Table 10-743. VENC_GAIN_U

Address Offset	0x0000 0030		
Physical Address	0x5800 3030 0x4804 3030	**Instance**	VENC_L3 VENC_PER_L4
Description	Gain control for Cb signal		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								GU							

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8:0	GU	Gain control for Cb signal. Following are typical programming examples for NTSC and PAL standards. NTSC with 7.5 IRE pedestal: WHITE - BLACK = 92.5 IRE GU = 0x102 NTSC with no pedestal: WHITE - BLACK = 100 IRE GU = 0x117 PAL with no pedestal: WHITE - BLACK = 100 IRE GU = 0x111	RW	0x102

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Table 10-744. Register Call Summary for Register VENC_GAIN_U

Video Encoder

- Chroma Stage: [0]
- Video Encoder Register Settings: [1]
- Video Encoder Register Summary: [2]

Table 10-745. VENC_GAIN_V

Address Offset	0x0000 0034		
Physical Address	0x5800 3034 0x4804 3034	**Instance**	VENC_L3 VENC_PER_L4
Description	Gain control of Cr signal		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								GV							

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8:0	GV	Gain control of Cr signal. Following are typical programming examples for NTSC and PAL standards. NTSC with 7.5 IRE pedestal: WHITE - BLACK = 92.5 IRE GV = 0x16C NTSC with no pedestal: WHITE - BLACK = 100 IRE GV = 0x189 PAL with no pedestal: WHITE - BLACK = 100 IRE GV = 0x181	RW	0x16C

Table 10-746. Register Call Summary for Register VENC_GAIN_V

Video Encoder

- Chroma Stage: [0]
- Video Encoder Register Settings: [1]
- Video Encoder Register Summary: [2]

Table 10-747. VENC_GAIN_Y

Address Offset	0x0000 0038		
Physical Address	0x5800 3038 0x4804 3038	**Instance**	VENC_L3 VENC_PER_L4
Description	Gain control of Y signal		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								GY							

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8:0	GY	Gain control of Y signal. Following are typical programming examples for NTSC/PAL standards. NTSC with 7.5 IRE pedestal: WHITE - BLACK = 92.5 IRE GY = 0x12F NTSC with no pedestal: WHITE - BLACK = 100 IRE GY = 0x147 PAL with no pedestal: WHITE - BLACK = 100 IRE GY = 0x140	RW	0x12F

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Table 10-748. Register Call Summary for Register VENC_GAIN_Y

Video Encoder

- Luma Stage: [0]
- Video Encoder Register Settings: [1]
- Video Encoder Register Summary: [2]

Table 10-749. VENC_BLACK_LEVEL

Address Offset	0x0000 003C		
Physical Address	0x5800 303C 0x4804 303C	**Instance**	VENC_L3 VENC_PER_L4
Description	BLACK LEVEL		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								BLACK							

Bits	Field Name	Description	Type	Reset
31:7	RESERVED		R	0x0000000
6:0	BLACK	Black level setting. Following are typical programming examples for NTSC/PAL standards. NTSC with 7.5 IRE pedestal: WHITE - BLACK = 92.5 IRE BLACK_LEVEL = 0x43 NTSC with no pedestal: WHITE - BLACK = 100 IRE BLACK_LEVEL = 0x38 PAL with no pedestal: WHITE - BLACK = 100 IRE BLACK_LEVEL = 0x3B	RW	0x43

Table 10-750. Register Call Summary for Register VENC_BLACK_LEVEL

Video Encoder

- Luma Stage: [0]
- Video Encoder Register Settings: [1]
- Video Encoder Register Summary: [2]

Table 10-751. VENC_BLANK_LEVEL

Address Offset	0x0000 0040		
Physical Address	0x5800 3040 0x4804 3040	**Instance**	VENC_L3 VENC_PER_L4
Description	BLANK LEVEL		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								BLANK							

Bits	Field Name	Description	Type	Reset
31:7	RESERVED		R	0x0000000
6:0	BLANK	Blank level setting. Following are typical programming examples for NTSC/PAL standards. NTSC with 7.5 IRE pedestal: WHITE - BLACK = 92.5 IRE BLANK_LEVEL = 0x38 NTSC with no pedestal: WHITE - BLACK = 100 IRE BLANK_LEVEL = 0x38 PAL with no pedestal: WHITE - BLACK = 100 IRE BLANK_LEVEL = 0x3B	RW	0x38

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Table 10-752. Register Call Summary for Register VENC_BLANK_LEVEL

Video Encoder

- Luma Stage: [0]
- Video Encoder Register Settings: [1]
- Video Encoder Register Summary: [2]

Table 10-753. VENC_X_COLOR

Address Offset	0x0000 0044		
Physical Address	0x5800 3044 0x4804 3044	**Instance**	VENC_L3 VENC_PER_L4
Description	Cross-Colour Control register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								XCE	RESERVED		XCBW		LCD		

Bits	Field Name	Description	Type	Reset
31:7	RESERVED		R	0x0000000
6	XCE	Cross color reduction enable for composite video output. Cross color does not affect S-video output 0x0: Cross color reduction is disabled 0x1: Cross color is enabled	RW	0
5	RESERVED		R	0
4:3	XCBW	Cross color reduction filter selection 0x0: The notch is at 32.8 % of the frequency of the encoding pixel clock 0x1: The notch is at 26.5 % of the frequency of the encoding pixel clock 0x2: The notch is at 30.0 % of the frequency of the encoding pixel clock 0x3: The notch is at 29.2 % of the frequency of the encoding pixel clock	RW	0x0
2:0	LCD	These three bits can be used for chroma channel delay compensation. Delay on Luma channel. 0x0: 0 0x1: 0.5 pixel clock period 0x2: 1.0 pixel clock period 0x3: 1.5 pixel clock period 0x4: -2.0 pixel clock period 0x5: -1.5 pixel clock period 0x6: -1.0 pixel clock period 0x7: -0.5 pixel clock period	RW	0x0

Table 10-754. Register Call Summary for Register VENC_X_COLOR

Video Encoder

- Video Encoder Register Settings: [0]
- Video Encoder Register Summary: [1]

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Table 10-755. VENC_M_CONTROL

Address Offset	0x0000 0048		
Physical Address	0x5800 3048 0x4804 3048	**Instance**	VENC_L3 VENC_PER_L4
Description	M_CONTROL		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								PALI	PALN	PALPHS	CBW			PAL	FFRQ

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Reserved	R	0x000000
7	PALI	PAL I enable 0x0: Normal oeration 0x1: PAL I Enable	RW	0
6	PALN	PAL N Enable 0x0: Normal operation 0x1: PAL N enable	RW	0
5	PALPHS	PAL switch phase setting 0x0: PAL switch phase is nominal 0x1: PAL switch phase is inverted compared to nominal	RW	0
4:2	CBW	Chrominance lowpass filter bandwidth control 0x0: -6db at 21.8 % of encoding pixel clock frequency 0x1: -6db at 19.8 % of encoding pixel clock frequency 0x2: -6db at 18.0 % of encoding pixel clock frequency 0x3: Reserved 0x4: Reserved 0x5: -6db at 23.7 % of encoding pixel clock frequency 0x6: -6db at 26.8 % of encoding pixel clock frequency 0x7: Chrominance lowpass filter bypass	RW	0x0
1	PAL	Phase alternation line encoding selection 0x0: Phase alternation line encoding disabled 0x1: Phase alternation line encoding enabled	RW	0
0	FFRQ	The value of this field and the SQP bit in the BSTAMP_WSS_DATA register control the number of horizontal pixels displayed per scan line # OF MODE SQP FFRQ PIXEL PER LINE ITU-R 601 NTSC 0 1 858 Square pixel NTSC 1 1 780 ITU-R 601 PAL 0 0 864 Square pixel PAL 1 0 944	RW	1

Table 10-756. Register Call Summary for Register VENC_M_CONTROL

Video Encoder

- Subcarrier and Burst Generation: [0] [1]
- Video Encoder Register Settings: [2]
- Video Encoder Register Summary: [3]

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Table 10-757. VENC_BSTAMP_WSS_DATA

Address Offset	0x0000 004C		
Physical Address	0x5800 304C 0x4804 304C	**Instance**	VENC_L3 VENC_PER_L4
Description	BSTAMP and WSS_DATA		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								WSS_D																SQP	BSTAP							

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:8	WSS_D	Wide Screen Signaling data NTSC: WORD 0 D0, D1 WORD 1 D2, D3, D4, D5 WORD 2 D6, D7, D8, D9, D10, D11, D12, D13 CRC D14, D15, D16, D17, D18, D19 PAL: GROUP A D0, D1, D2, D3 GROUP B D4, D5, D6, D7 GROUP C D8, D9 ,D10 GROUP D D11, D12, D13	RW	0x00000
7	SQP	Square-pixel sampling rate. See FFRQ in M_CONTROL register for programming information. 0x0: ITU-R 601 sampling rate 0x1: Square-pixel sampling rate	RW	0
6:0	BSTAP	Setting of amplitude of color burst.	RW	0x38

Table 10-758. Register Call Summary for Register VENC_BSTAMP_WSS_DATA

Video Encoder

- Subcarrier and Burst Generation: [0]
- Wide-Screen Signaling (WSS) Encoding: [1]
- Video Encoder Register Settings: [2]
- Video Encoder Register Summary: [3]

Table 10-759. VENC_S_CARR

Address Offset	0x0000 0050		
Physical Address	0x5800 3050 0x4804 3050	**Instance**	VENC_L3 VENC_PER_L4
Description	Color Subcarrier Frequency Registers.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FSC																															

Bits	Field Name	Description	Type	Reset
31:0	FSC	These four bytes' data are used to program color subcarrier frequency. These four bytes are determined by the following formula. S_CARR = ROUND((Fsc/Fclkenc) * 232) Where Fsc = Frequency of the subcarrier Fclkenc = Frequency of the internal video encoding clock = 2*LLEN *Fh LLEN = Number of pixels in a scan line Fh = Line frequency See the description of LLEN registers (subaddresses 0x42 and 0x43).	RW	0x21F0 7C1F

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Table 10-760. Register Call Summary for Register VENC_S_CARR

Video Encoder

- Subcarrier and Burst Generation: [0] [1] [2]
- Video Encoder Register Settings: [3]
- Video Encoder Register Summary: [4]

Table 10-761. VENC_LINE21

Address Offset	0x0000 0054		
Physical Address	0x5800 3054 0x4804 3054	**Instance**	VENC_L3 VENC_PER_L4
Description	LINE 21		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
L21E																L21O															

Bits	Field Name	Description	Type	Reset
31:16	L21E	The two bytes of the closed caption data in the even field. For the data stream content, see Table 10-707. [31:24] First byte of data [23:16] Second byte of data	RW	0x0000
15:0	L21O	The two bytes of the closed caption data in the odd field For the data stream content, see Table 10-707. [15:8] First byte of data [7:0] Second byte of data	RW	0x0000

Table 10-762. Register Call Summary for Register VENC_LINE21

Video Encoder

- Closed Caption Encoding: [0] [1] [2] [3]
- Video Encoder Register Settings: [4]
- Video Encoder Register Summary: [5]

Table 10-763. VENC_LN_SEL

Address Offset	0x0000 0058		
Physical Address	0x5800 3058 0x4804 3058	**Instance**	VENC_L3 VENC_PER_L4
Description	LN_SEL		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								LN21_RUNIN								RESERVED								SLINE							

Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x00
25:16	LN21_RUNIN	The two Bytes of the closed caption runin code position from the HSYNC	RW	0x10B
15:5	RESERVED		R	0x000
4:0	SLINE	Selects the line where closed caption or extended service data are encoded.	RW	0x15

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Bits	Field Name	Description	Type	Reset
		PAL mode: Because there is a one-line offset, program the desired line number – 1. NTSC mode: Because there is a four-line offset, program the desired line number – 4.		

Table 10-764. Register Call Summary for Register VENC_LN_SEL

Video Encoder

- Closed Caption Encoding: [0] [1] [2]
- Video Encoder Register Settings: [3]
- Video Encoder Register Summary: [4]

Table 10-765. VENC_L21_WC_CTL

Address Offset	0x0000 005C		
Physical Address	0x5800 305C 0x4804 305C	**Instance**	VENC_L3 VENC_PER_L4
Description	L21 WC_CTL registers		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																INV	EVEN_ODD_EN		LINE					RESERVED						L21EN	

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15	INV	WSS inverter 0x0: no effect 0x1: invert WSS data	RW	0
14:13	EVEN_ODD_EN	This bit controls the WSS encoding. 0x0: WSS encoding OFF 0x1: Enables encoding in 2nd field (odd field) 0x2: Enables encoding in 1st field (even field) 0x3: Enables encoding in both fields	RW	0x0
12:8	LINE	Selects the line where WSS data are encoded. PAL mode: Because there is a one-line offset, program the desired line number – 1. NTSC mode: Because there is a four-line offset, program the desired line number – 4.	RW	0x14
7:2	RESERVED		R	0x00
1:0	L21EN	Those bits controls the Line21 closed caption encoding according to the mode. 0x0: Line21 encoding OFF 0x1: Enables encoding in 1st field (ODD field) 0x2: Enables encoding in 2d field (EVEN field) 0x3: Enables encoding in both fields	RW	0x0

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Table 10-766. Register Call Summary for Register VENC_L21_WC_CTL

Video Encoder

- Closed Caption Encoding: [0] [1]
- Wide-Screen Signaling (WSS) Encoding: [2] [3]
- Video Encoder Register Settings: [4]
- Video Encoder Register Summary: [5]

Table 10-767. VENC_HTRIGGER_VTRIGGER

Address Offset	0x0000 0060		
Physical Address	0x5800 3060 0x4804 3060	**Instance**	VENC_L3 VENC_PER_L4
Description	HTRIGGER and VTRIGGER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								VTRIG								RESERVED								HTRIG							

Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x00
25:16	VTRIG	Vertical trigger reference for VSYNC. These bits specify the phase between VSYNC input and the lines in a field. The VTRIG field is expressed in units of half-line.	RW	0x000
15:11	RESERVED		R	0x00
10:0	HTRIG	Horizontal trigger phase, which sets HSYNC. HTRIG is expressed in half-pixels or clk2x (27 MHz) periods	RW	0x000

Table 10-768. Register Call Summary for Register VENC_HTRIGGER_VTRIGGER

Video Encoder

- Video Encoder Register Settings: [0]
- Video Encoder Register Summary: [1]

Table 10-769. VENC_SAVID_EAVID

Address Offset	0x0000 0064		
Physical Address	0x5800 3064 0x4804 3064	**Instance**	VENC_L3 VENC_PER_L4
Description	SAVID and EAVID		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								EAVID								RESERVED								SAVID							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED		R	0x00
26:16	EAVID	End of active video. These bits define the ending pixel position on a horizontal display line where active video will be displayed.	RW	0x693
15:11	RESERVED		R	0x00
10:0	SAVID	Start of active video. These bits define the starting pixel position on a horizontal line where active video will be displayed.	RW	0x0F4

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Table 10-770. Register Call Summary for Register VENC_SAVID_EAVID

Video Encoder

- Video Encoder Register Settings: [0]
- Video Encoder Register Summary: [1]

Table 10-771. VENC_FLEN_FAL

Address Offset	0x0000 0068		
Physical Address	0x5800 3068 0x4804 3068	**Instance**	VENC_L3 VENC_PER_L4
Description	FLEN and FAL		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								FAL								RESERVED								FLEN							

Bits	Field Name	Description	Type	Reset
31:25	RESERVED		R	0x00
24:16	FAL	First Active Line of Field. These bits define the first active line of a field	RW	0x016
15:10	RESERVED		R	0x00
9:0	FLEN	Field length. These bits define the number of half_lines in each field. Length of field = (FLEN + 1) half_lines	RW	0x20C

Table 10-772. Register Call Summary for Register VENC_FLEN_FAL

Video Encoder

- Video Encoder Register Settings: [0]
- Video Encoder Register Summary: [1]

Table 10-773. VENC_LAL_PHASE_RESET

Address Offset	0x0000 006C		
Physical Address	0x5800 306C 0x4804 306C	**Instance**	VENC_L3 VENC_PER_L4
Description	LAL and PHASE_RESET		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													PRES		SBLANK	RESERVED								LAL							

Bits	Field Name	Description	Type	Reset
31:19	RESERVED		R	0x0000
18:17	PRES	Phase reset mode. 0x0: No reset 0x1: Reset every two lines 0x2: Reset every eight fields. Color subcarrier phase is reset to C_Phase (subaddress 5A) upon reset 0x3: Reset every four fields. Color subcarrier phase is reset to C_Phase (subaddress 5A) upon reset	RW	0x3

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Bits	Field Name	Description	Type	Reset
16	SBLANK	Vertical blanking setting 0x0: Vertical blanking is defined by the setting of FAL and LAL registers. 0x1: Vertical blanking is forced automatically during field synchronization and equalization.	RW	0
15:9	RESERVED		R	0x00
8:0	LAL	Last Active Line of Field. These bits define the last active line of a field	RW	0x107

Table 10-774. Register Call Summary for Register VENC_LAL_PHASE_RESET

Video Encoder
- Video Encoder Register Settings: [0]
- Video Encoder Register Summary: [1]

Table 10-775. VENC_HS_INT_START_STOP_X

Address Offset	0x0000 0070		
Physical Address	0x5800 3070 0x4804 3070	**Instance**	VENC_L3 VENC_PER_L4
Description	HS_INT_START_STOP_X		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								HS_INT_STOP_X								RESERVED								HS_INT_START_X							

Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x00
25:16	HS_INT_STOP_X	HSYNC internal stop. These bits define HSYNC internal stop pixel value	RW	0x07E
15:10	RESERVED		R	0x00
9:0	HS_INT_START_X	HSYNC internal start. These bits define HSYNC internal start pixel value	RW	0x34E

Table 10-776. Register Call Summary for Register VENC_HS_INT_START_STOP_X

Video Encoder
- Video Encoder Register Settings: [0]
- Video Encoder Register Summary: [1]

Table 10-777. VENC_HS_EXT_START_STOP_X

Address Offset	0x0000 0074		
Physical Address	0x5800 3074 0x4804 3074	**Instance**	VENC_L3 VENC_PER_L4
Description	HS_EXT_START_STOP_X		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								HS_EXT_STOP_X								RESERVED								HS_EXT_START_X							

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Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x00
25:16	HS_EXT_STOP_X	HSYNC external stop. These bits define HSYNC external stop pixel value	RW	0x00F
15:10	RESERVED		R	0x00
9:0	HS_EXT_START_X	HSYNC external start. These bits define HSYNC external start pixel value	RW	0x359

Table 10-778. Register Call Summary for Register VENC_HS_EXT_START_STOP_X

Video Encoder

- Video Encoder Register Settings: [0]
- Video Encoder Register Summary: [1]

Table 10-779. VENC_VS_INT_START_X

Address Offset	0x0000 0078		
Physical Address	0x5800 3078 0x4804 3078	**Instance**	VENC_L3 VENC_PER_L4
Description	VS_INT_START_X		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								VS_INT_START_X								RESERVED															

Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x00
25:16	VS_INT_START_X	VSYNC internal start. These bits define VSYNC internal start pixel value.	RW	0x1A0
15:0	RESERVED		R	0x0000

Table 10-780. Register Call Summary for Register VENC_VS_INT_START_X

Video Encoder

- Video Encoder Register Settings: [0]
- Video Encoder Register Summary: [1]

Table 10-781. VENC_VS_INT_STOP_X_VS_INT_START_Y

Address Offset	0x0000 007C		
Physical Address	0x5800 307C 0x4804 307C	**Instance**	VENC_L3 VENC_PER_L4
Description	VS_INT_STOP_X and VS_INT_START_Y		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								VS_INT_START_Y								RESERVED								VS_INT_STOP_X							

Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x00
25:16	VS_INT_START_Y	VSYNC internal start. These bits define VSYNC internal start line value	RW	0x209
15:10	RESERVED		R	0x00
9:0	VS_INT_STOP_X	VSYNC internal stop. These bits define VSYNC internal stop pixel value	RW	0x1A0

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Table 10-782. Register Call Summary for Register VENC_VS_INT_STOP_X_VS_INT_START_Y

Video Encoder

- Video Encoder Register Settings: [0]
- Video Encoder Register Summary: [1]

Table 10-783. VENC_VS_INT_STOP_Y_VS_EXT_START_X

Address Offset	0x0000 0080		
Physical Address	0x5800 3080 0x4804 3080	**Instance**	VENC_L3 VENC_PER_L4
Description	VS_INT_STOP_Y and VS_EXT_START_X		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								VS_EXT_START_X								RESERVED								VS_INT_STOP_Y							

Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x00
25:16	VS_EXT_START_X	VSYNC external start. These bits define VSYNC external start pixel value.	RW	0x1AC
15:10	RESERVED		R	0x00
9:0	VS_INT_STOP_Y	VSYNC internal stop. These bits define VSYNC internal stop line value.	RW	0x022

Table 10-784. Register Call Summary for Register VENC_VS_INT_STOP_Y_VS_EXT_START_X

Video Encoder

- Video Encoder Register Settings: [0]
- Video Encoder Register Summary: [1]

Table 10-785. VENC_VS_EXT_STOP_X_VS_EXT_START_Y

Address Offset	0x0000 0084		
Physical Address	0x5800 3084 0x4804 3084	**Instance**	VENC_L3 VENC_PER_L4
Description	VS_EXT_STOP_X and VS_EXT_START_Y		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								VS_EXT_START_Y								RESERVED								VS_EXT_STOP_X							

Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x00
25:16	VS_EXT_START_Y	VSYNC external start. These bits define VSYNC external start line value.	RW	0x20D
15:10	RESERVED		R	0x00
9:0	VS_EXT_STOP_X	VSYNC external stop. These bits define VSYNC external stop pixel value.	RW	0x1AC

Table 10-786. Register Call Summary for Register VENC_VS_EXT_STOP_X_VS_EXT_START_Y

Video Encoder

- Video Encoder Register Settings: [0]
- Video Encoder Register Summary: [1]

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Table 10-787. VENC_VS_EXT_STOP_Y

Address Offset	0x0000 0088		
Physical Address	0x5800 3088 0x4804 3088	**Instance**	VENC_L3 VENC_PER_L4
Description	VS_EXT_STOP_Y		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								VS_EXT_STOP_Y							

Bits	Field Name	Description	Type	Reset
31:10	RESERVED		R	0x000000
9:0	VS_EXT_STOP_Y	VSYNC external stop. These bits define VSYNC external stop line value.	RW	0x006

Table 10-788. Register Call Summary for Register VENC_VS_EXT_STOP_Y

Video Encoder

- Video Encoder Register Settings: [0]
- Video Encoder Register Summary: [1]

Table 10-789. VENC_AVID_START_STOP_X

Address Offset	0x0000 0090		
Physical Address	0x5800 3090 0x4804 3090	**Instance**	VENC_L3 VENC_PER_L4
Description	AVID_START_STOP_X		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								AVID_STOP_X								RESERVED								AVID_START_X							

Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x00
25:16	AVID_STOP_X	AVID stop. These bits define AVID stop pixel value	RW	0x348
15:10	RESERVED		R	0x00
9:0	AVID_START_X	AVID start. These bits define AVID start pixel value	RW	0x078

Table 10-790. Register Call Summary for Register VENC_AVID_START_STOP_X

Video Encoder

- Video Encoder Register Settings: [0]
- Video Encoder Register Summary: [1]

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Table 10-791. VENC_AVID_START_STOP_Y

Address Offset	0x0000 0094		
Physical Address	0x5800 3094 0x4804 3094	**Instance**	VENC_L3 VENC_PER_L4
Description	AVID_START_STOP_Y		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								AVID_STOP_Y								RESERVED								AVID_START_Y							

Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x00
25:16	AVID_STOP_Y	AVID stop. These bits define AVID stop line value.	RW	0x206
15:10	RESERVED		R	0x00
9:0	AVID_START_Y	AVID start. These bits define AVID start line value	RW	0x026

Table 10-792. Register Call Summary for Register VENC_AVID_START_STOP_Y

Video Encoder

- Video Encoder Register Settings: [0]
- Video Encoder Register Summary: [1]

Table 10-793. VENC_FID_INT_START_X_FID_INT_START_Y

Address Offset	0x0000 00A0		
Physical Address	0x5800 30A0 0x4804 30A0	**Instance**	VENC_L3 VENC_PER_L4
Description	FID_INT_START_X and FID_INT_START_Y		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								FID_INT_START_Y								RESERVED								FID_INT_START_X							

Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x00
25:16	FID_INT_START_Y	FID internal stop. These bits define FID internal start line value	RW	0x001
15:10	RESERVED		R	0x00
9:0	FID_INT_START_X	FID internal start. These bits define FID internal start pixel value	RW	0x08A

Table 10-794. Register Call Summary for Register VENC_FID_INT_START_X_FID_INT_START_Y

Video Encoder

- Video Encoder Register Settings: [0]
- Video Encoder Register Summary: [1]

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Table 10-795. VENC_FID_INT_OFFSET_Y_FID_EXT_START_X

Address Offset	0x0000 00A4		
Physical Address	0x5800 30A4 0x4804 30A4	**Instance**	VENC_L3 VENC_PER_L4
Description	FID_INT_OFFSET_Y and FID_EXT_START_X		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								FID_EXT_START_X								RESERVED								FID_INT_OFFSET_Y							

Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x00
25:16	FID_EXT_START_X	FID external start. These bits define FID external start pixel value	RW	0x1AC
15:10	RESERVED		R	0x00
9:0	FID_INT_OFFSET_Y	FID internal offset. These bits define FID internal offset linel value	RW	0x106

Table 10-796. Register Call Summary for Register VENC_FID_INT_OFFSET_Y_FID_EXT_START_X

Video Encoder

- Video Encoder Register Settings: [0]
- Video Encoder Register Summary: [1]

Table 10-797. VENC_FID_EXT_START_Y_FID_EXT_OFFSET_Y

Address Offset	0x0000 00A8		
Physical Address	0x5800 30A8 0x4804 30A8	**Instance**	VENC_L3 VENC_PER_L4
Description	FID_EXT_START_Y and FID_EXT_OFFSET_Y		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								FID_EXT_OFFSET_Y								RESERVED								FID_EXT_START_Y							

Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x00
25:16	FID_EXT_OFFSET_Y	FID external offset. These bits define FID external offset line value	RW	0x106
15:10	RESERVED		R	0x00
9:0	FID_EXT_START_Y	FID external start. These bits define FID external start line value.	RW	0x006

Table 10-798. Register Call Summary for Register VENC_FID_EXT_START_Y_FID_EXT_OFFSET_Y

Video Encoder

- Video Encoder Register Settings: [0]
- Video Encoder Register Summary: [1]

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Table 10-799. VENC_TVDETGP_INT_START_STOP_X

Address Offset	0x0000 00B0		
Physical Address	0x5800 30B0 0x4804 30B0	**Instance**	VENC_L3 VENC_PER_L4
Description	TVDETGP_INT_START_STOP_X		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TVDETGP_INT_STOP_X								RESERVED								TVDETGP_INT_START_X							

Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x00
25:16	TVDETGP_INT_STOP_X	TVDETGP internal stop. These bits define TVDETGP internal stop pixel value.	RW	0x014
15:10	RESERVED		R	0x00
9:0	TVDETGP_INT_START_X	TVDETGP internal start. These bits define TVDETGP internal start pixel value	RW	0x001

Table 10-800. Register Call Summary for Register VENC_TVDETGP_INT_START_STOP_X

Video Encoder

- TV Detection/Disconnection Pulse Generation and Use: [0] [1]
- Video Encoder Global Initialization: [2] [3]
- Video Encoder Register Settings: [4]
- Video Encoder Register Summary: [5]

Table 10-801. VENC_TVDETGP_INT_START_STOP_Y

Address Offset	0x0000 00B4		
Physical Address	0x5800 30B4 0x4804 30B4	**Instance**	VENC_L3 VENC_PER_L4
Description	TVDETGP_INT_START_STOP_Y		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TVDETGP_INT_STOP_Y								RESERVED								TVDETGP_INT_START_Y							

Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x00
25:16	TVDETGP_INT_STOP_Y	TVDETGP internal stop. These bits define TVDETGP internal stop line value.	RW	0x001
15:10	RESERVED		R	0x00
9:0	TVDETGP_INT_START_Y	TVDETGP internal start. These bits define TVDETGP internal start line value	RW	0x001

Table 10-802. Register Call Summary for Register VENC_TVDETGP_INT_START_STOP_Y

Video Encoder

- TV Detection/Disconnection Pulse Generation and Use: [0]
- Video Encoder Global Initialization: [1] [2]
- Video Encoder Register Settings: [3]
- Video Encoder Register Summary: [4]

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Table 10-803. VENC_GEN_CTRL

Address Offset	0x0000 00B8		
Physical Address	0x5800 30B8 0x4804 30B8	**Instance**	VENC_L3 VENC_PER_L4
Description	TVDETGP enable and SYNC_POLARITY and UVPHASE_POL		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					MS	UVPHASE_POL_656	CBAR	HIP	VIP	HEP	VEP	AVIDP	FIP	FEP	TVDP	RESERVED															EN

Bits	Field Name	Description	Type	Reset
31:27	RESERVED		R	0x00
26	MS	UVPHASE_POL MS mode UV phase 0x0: CbCr 0x1: CrCb	RW	0
25	UVPHASE_POL_656	UVPHASE_POL 656 input mode UV phase 0x0: CbCr 0x1: CrCb	RW	0
24	CBAR	UVPHASE_POL CBAR mode UV phase 0x0: CbCr 0x1: CrCb	RW	0
23	HIP	HSYNC internal polarity 0x0: Active Low 0x1: Active High	RW	1
22	VIP	VSYNC internal polarity 0x0: Active Low 0x1: Active High	RW	1
21	HEP	HSYNC external polarity 0x0: Active Low 0x1: Active High	RW	1
20	VEP	VSYNC externall polarity 0x0: Active Low 0x1: Active High	RW	1
19	AVIDP	AVID polarity 0x0: Active Low 0x1: Active High	RW	1
18	FIP	FID internal polarity 0x0: Active Low 0x1: Active High	RW	1
17	FEP	FID external polarity 0x0: Active Low 0x1: Active High	RW	1

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Bits	Field Name	Description	Type	Reset
16	TVDP	TVDETGP polarity 0x0: Active Low 0x1: Active High	RW	1
15:1	RESERVED		R	0x0000
0	EN	TVDETGP generation enable 0x0: Disabled 0x1: Enabled	RW	0

Table 10-804. Register Call Summary for Register VENC_GEN_CTRL

Video Encoder

- TV Detection/Disconnection Pulse Generation and Use: [0] [1]
- Video Encoder Global Initialization: [2] [3] [4] [5]
- Video Encoder Register Settings: [6]
- Video Encoder Register Summary: [7]

Table 10-805. VENC_OUTPUT_CONTROL

Address Offset	0x0000 00C4		
Physical Address	0x5800 30C4 0x4804 30C4	**Instance**	VENC_L3 VENC_PER_L4
Description	Output channel control register Also contains some test control features		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																									COMPOSITE_SOURCE	RESERVED	TEST_MODE	VIDEO_INVERT	RESERVED	COMPOSITE_ENABLE	RESERVED

Bits	Field Name	Description	Type	Reset
31:7	RESERVED		R	0x00
6	COMPOSITE_SOURCE	Source of composite video data in test mode 0x0: Composite test data comes from internal register OUTPUT_TEST[9:0] 0x1: Composite test data comes from display controller video port G[1:0], B[7:0]	RW	0
5	RESERVED		RW	0x00
4	TEST_MODE	This enables the video DACs to be tested. The values sent to the DACs comes from a register for each output channel (Luma, Composite or Chroma) or from the display controller video port bits G[1:0], B[7:0], depending on the setting of the Source bits 0x0: Video outputs are in normal operation 0x1: Test mode. Video outputs are directly connected to either internal registers or the display controller video port.	RW	0
3	VIDEO_INVERT	Controls the video output polarity. This may be used to correct for inversion in an external video amplifier. 0x0: Video outputs are inverted 0x1: Video outputs are normal polarity	RW	1

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Bits	Field Name	Description	Type	Reset
2	RESERVED		RW	0x00
1	COMPOSITE_ENABLE	Enable the Composite output channel 0x0: Composite output is disabled 0x1: Composite output is enabled	RW	0
0	RESERVED		RW	0x00

Table 10-806. Register Call Summary for Register VENC_OUTPUT_CONTROL

Video Encoder

- Video Encoder Environment: [0]
- Video DAC Test Mode: [1] [2]
- Video DAC Power Management: [3]
- Video Encoder Global Initialization: [4] [5]
- Video Encoder Register Settings: [6]
- Video Encoder Register Summary: [7]

Table 10-807. VENC_OUTPUT_TEST

Address Offset	0x0000 00C8		
Physical Address	0x5800 30C8 0x4804 30C8	**Instance**	VENC_L3 VENC_PER_L4
Description	Test values for the Luma/Composite Video DAC		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								COMPOSITE_TEST							

Bits	Field Name	Description	Type	Reset
31:10	RESERVED		R	0x00
9:0	COMPOSITE_TEST	In test mode, DAC input value (if composite video is selected)	RW	0x000

Table 10-808. Register Call Summary for Register VENC_OUTPUT_TEST

Video Encoder

- Video DAC Test Mode: [0]
- Video Encoder Register Settings: [1]
- Video Encoder Register Summary: [2]

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2D/3D Graphics Accelerator

This chapter describes the 2D/3D graphics accelerator (SGX) for the device.

NOTE: The SGX subsystem is an instantiation by Texas Instruments of the POWERVR™ SGX540 core from Imagination Technologies Ltd.

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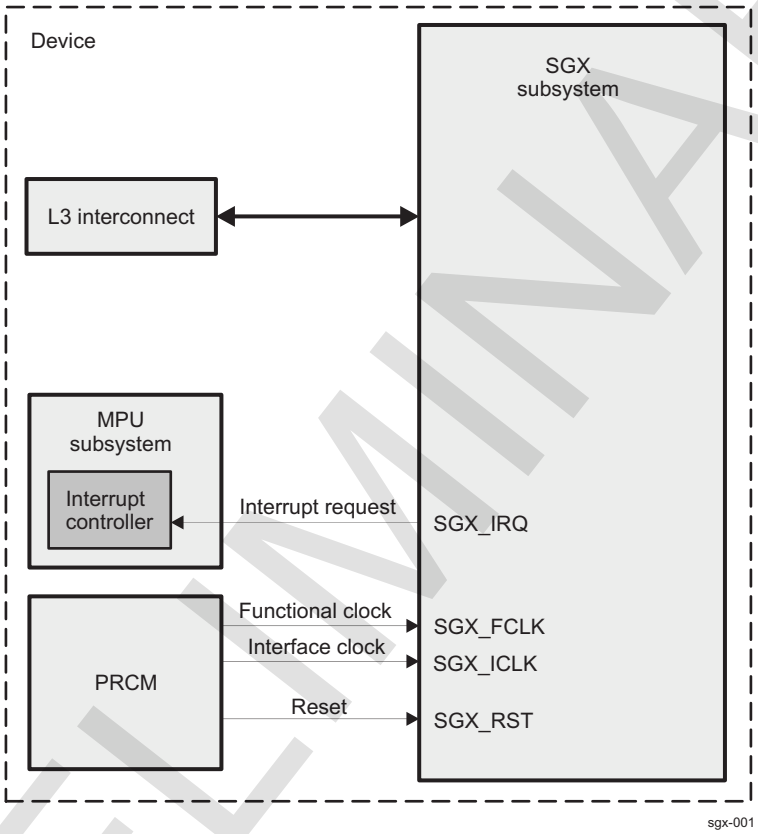
11.1 SGX Overview

The 2D/3D graphics accelerator (SGX) subsystem accelerates 2-dimensional (2D) and 3-dimensional (3D) graphics applications. The SGX subsystem is based on the POWERVR® SGX core from Imagination Technologies. SGX is a new generation of programmable POWERVR graphics IP cores. The POWERVR SGX540 v1.2.0 architecture is scalable and can target all market segments from mainstream mobile devices to high-end desktop graphics. Targeted applications include feature phones, PDAs, and handheld gaming applications.

Figure 11-1 shows the SGX subsystem.

Figure 11-1. SGX Overview



The SGX graphics accelerator efficiently processes a number of various multimedia data types concurrently:

- Pixel data
- Vertex data
- General-purpose processing

The multithreaded architecture uses two levels of scheduling and data partitioning to enable zero overhead task switching.

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11.1.1 POWERVR SGX Main Features

- 3D graphics, vector graphics, and video supported on common hardware
- Tile-based architecture
- Universal scalable shader engine (USSE™): a multithreaded engine that incorporates pixel and vertex shader functionality and reduces die area
- Advanced shader feature set in excess of Microsoft VS3.0, PS3.0, and OpenGL™2.0
- Industry standard application programming interface (API) support: OpenGL ES 1.1 and 2.0, OpenVG v1.1
- Fine-grained task switching, load balancing, and power management
- Advanced geometry, direct memory access (DMA)-driven operation for minimum CPU interaction
- Programmable high-quality image antialiasing
- Fully virtualized memory addressing for operating system (OS) operation in a unified memory architecture

11.1.2 SGX 3D Features

- Deferred pixel shading
- On-chip tile floating-point depth buffer
- 8-bit stencil with on-chip tile stencil buffer
- Scissor test
- Texture support:
  - Cube map
  - Projected textures
  - Nonsquare textures
- Texture formats:
  - RGBA 8888, 565, 1555
  - Monochromatic 8, 16, 16f, 32f, 32int
  - Dual channel, 8:8, 16:16, 16f:16f
  - Compressed textures PVR-TC1, PVR-TC2, ETC1
  - Programmable support for all YUV formats
- Resolution support:
  - Frame buffer maximum size = 2048 x 2048
  - Texture maximum size = 2048 x 2048
- Texture filtering:
  - Bilinear, trilinear
  - Independent minimum and maximum control
- Antialiasing:
  - 4x multisampling
  - Programmable sample positions
- Indexed primitive list support
  - Bus mastered
- Programmable vertex DMA
- Render to texture:
  - Including twiddled formats
  - Auto MipMap generation
- Multiple on-chip render targets (MRTs)

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NOTE: Performance is limited when on-chip memory is not available for the SGX core.

11.1.3 SGX Universal Scalable Shader Engine – Key Features

The USSE is the engine core of the POWERVR SGX architecture and supports a broad range of instructions.

- Single programming model:
  - Multithreaded with 16 simultaneous execution threads and up to 64 simultaneous data instances
  - Zero-cost swapping in and out of threads
  - Cached program execution model
  - Dedicated pixel processing instructions
  - Dedicated vertex processing instructions
- SIMD execution unit supporting operations in:
  - 32-bit IEEE float
  - 2-way 16-bit fixed point
  - 4-way 8-bit integer
  - 32-bit bit-wise (logical only)
- Static and dynamic flow control:
  - Subroutine calls
  - Loops
  - Conditional branches
  - Zero-cost instruction predication
- Procedural geometry:
  - Allows generation of primitives
  - Effective geometry compression
  - High-order surface support
- External data access:
  - Permits reads from main memory using cache
  - Permits writes to main memory
  - Data fence facility
  - Dependent texture reads

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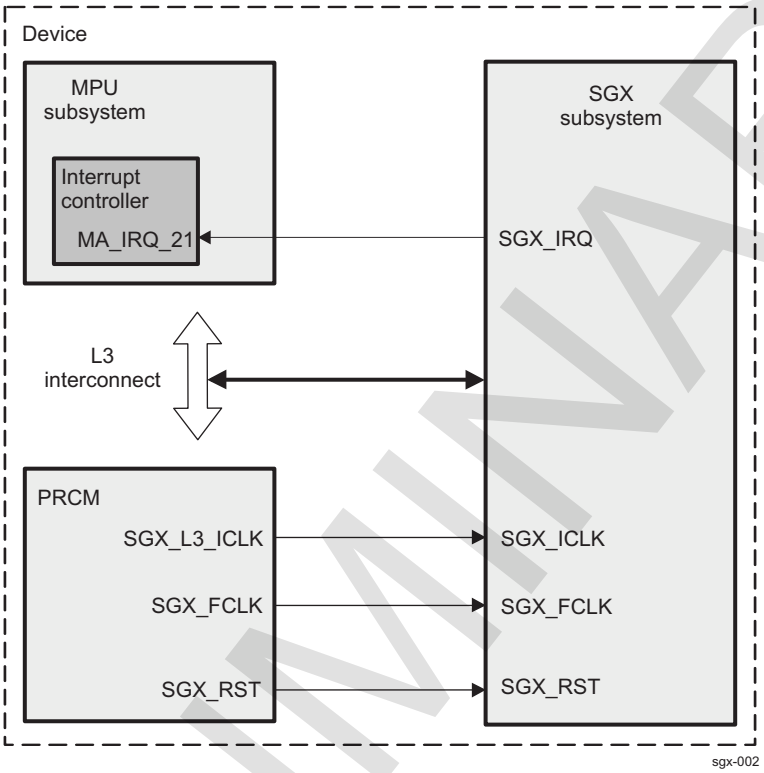
11.2 SGX Integration

This section describes module integration in the device, including information about clocks, resets, and hardware requests.

Figure 11-2 shows SGX integration.

Figure 11-2. SGX Integration



The SGX subsystem is connected to the level 3 (L3) interconnect by a 128-bit master and a 64-bit slave interface.

Table 11-1 through Table 11-3 summarize the integration of the module in the device.

Table 11-1. Integration Attributes

Module Instance	Attributes	
	Power Domain	Interconnect
SGX	PD_GFX	L3

Table 11-2. Clocks and Resets

Clocks				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
SGX	SGX_ICLK	SGX_L3_ICLK	PRCM	SGX interface clock
SGX	SGX_FCLK	SGX_FCLK	PRCM	SGX functional clock
Resets				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
SGX	SGX_RST	SGX_RST	PRCM	SGX reset signal

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Table 11-3. Hardware Requests

Interrupt Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
SGX	SGX_IRQ	MA_IRQ_21	Cortex-A9 INTC	SGX interrupt request to the MPU interrupt controller (INTC)

NOTE:

- For a description of the interrupt source, see Section 11.3.5, *Interrupt Requests*.

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11.3 SGX Functional Description

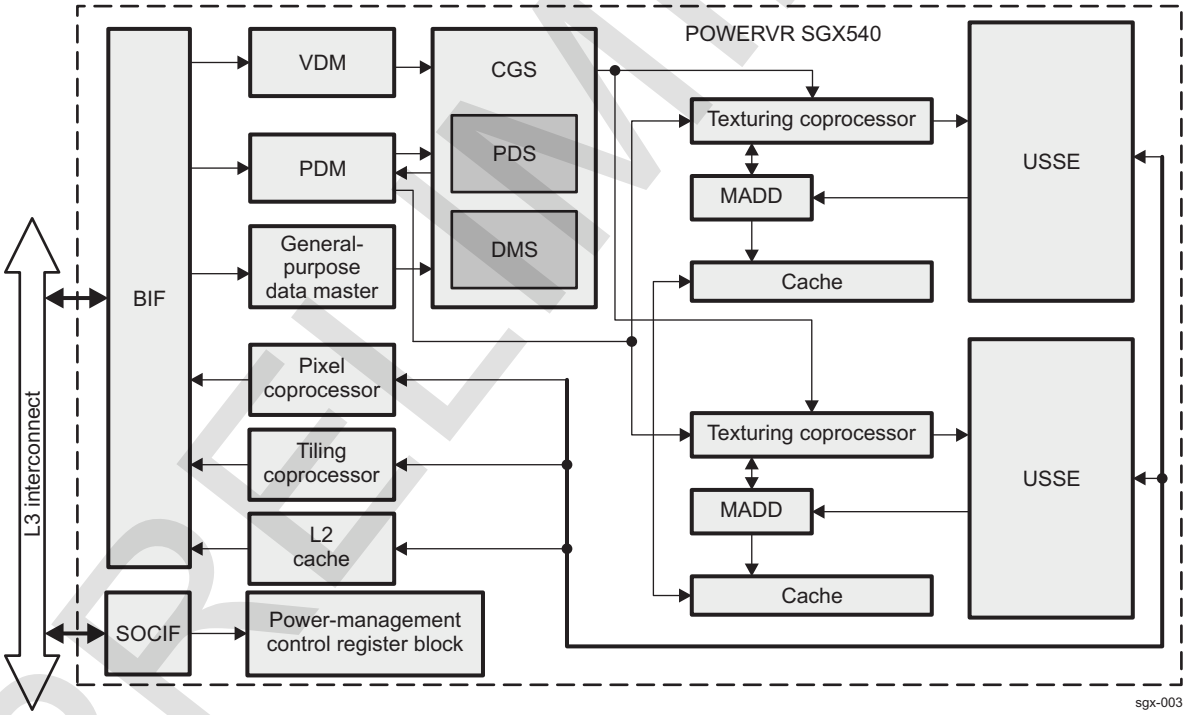
11.3.1 SGX Block Diagram

The SGX subsystem is based on the POWERVR SGX540 core from Imagination Technologies. The architecture uses both programmable and hard-coded pipelines to perform various processing tasks required in 2D, 3D, and video processing. The SGX architecture comprises the following elements:

- Coarse grain scheduler (CGS)
  - Programmable data sequencer (PDS)
  - Data master selector (DMS)
- Vertex data master (VDM)
- Pixel data master (PDM)
- General-purpose data master
- USSE
- Tiling coprocessor
- Pixel coprocessor
- Texturing coprocessor
- Multilevel cache

Figure 11-3 shows the SGX block diagram.

Figure 11-3. SGX Block Diagram



11.3.1.1 CGS

The CGS is the main system controller for the POWERVR SGX architecture and consists of two stages: the DMS and the PDS. The DMS processes requests from the data masters and determines which tasks can be executed given the resource requirements. The PDS then controls the loading and processing of data on the USSE.

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11.3.1.2 Data Masters

The SGX core includes three data masters:

- VDM: the initiator of transform and lighting processing within the system. The VDM reads an input control stream, which contains triangle index data and state data. The state data indicates the PDS program, the size of the vertices, and the amount of USSE output buffer resource available to the VDM. The triangle data is parsed to determine unique indices that must be processed by the USSE. These are grouped together based on the configuration provided by the driver and presented to the DMS.
- PDM: the initiator of the rasterization processing within the system. Each pixel pipeline processes pixels for a different half of a given tile, which allows for optimum efficiency within each pipe due to the locality of the data. For each task it determines the amount of resource required within the USSE. It merges this with the state address and issues a request for execution on the USSE to the DMS.
- General-purpose data master: responds to events within the system (such as the end of a pass of triangles from the ISP, end of a tile from the ISP, end of a render, or parameter stream breakpoint event). Each event causes either an interrupt to the host or the synchronized execution of a program on the PDS. The program might or might not cause a subsequent task to be executed on the USSE.

11.3.1.3 USSE

The USSE is a user-programmable processing unit. Although general in nature, its instructions and features are optimized for three types of task: processing vertices (vertex shading), processing pixels (pixel shading), and video/imaging processing.

11.3.1.4 Multilevel Cache

The multilevel cache is a 2-level cache consisting of two modules: the main cache and the mux/arbiter/demux/decompression unit (MADD). The MADD is a wrapper around the main cache module designed to manage and format requests to and from the cache as well as provide level 0 caching for texture and USSE requests.

The MADD can accept requests from the PDS, USSE, and texture address generator modules. Arbitration is performed between the three data streams; any required texture decompression is also performed.

11.3.1.5 Texturing Coprocessor

The texturing coprocessor performs texture address generation and formatting of texture data. It receives requests from the iterators or the USSE modules and translates these into requests to the multilevel cache. Data returned from the cache are then formatted based on the texture format selected and sent to the USSE for pixel-shading operations.

11.3.1.6 Tiling Coprocessor

To process pixels in a tiled manner, the screen is divided into tiles and arranged as groups of tiles by the tiling coprocessor. An inherent advantage of tiling architecture is that a large amount of vertex data can be rejected at this stage, thus reducing both the memory storage requirements and the amount of pixel processing performed.

11.3.1.7 Pixel Coprocessor

The pixel coprocessor is the final stage of the pixel-processing pipeline and controls the format of the final pixel data sent to the memory. It supplies the USSE with an address to the output buffer, and the USSE returns the relevant pixel data. The address order is determined by the mode of the frame buffer. The pixel coprocessor contains a dithering and packing function.

11.3.2 SGX Clock Configuration

The SGX subsystem operates from two clocks: an interface clock (SGX_ICLK) and a functional clock (SGX_FCLK). The power, reset, and clock management (PRCM) module generates and distributes both clocks inside the device.

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- The SGX_ICLK interface clock manages the data transfer on the L3 master and slave ports.

  The SGX_ICLK frequency is selected based on the whole device L3 interconnect clock frequency. For more information on the interface clock, see Section 3.6.11, *CD_SGX Clock Domains*.

  When no longer required by the SGX subsystem, SGX_ICLK can be disabled by software at the PRCM level. For more information, see Section 3.7.8, *PD_SGX Description*.

  NOTE: SGX_ICLK is cut only if the SGX is ready to go into IDLE state.

- SGX_FCLK is the functional clock and is used inside the SGX subsystem to generate clock signals to multiple SGX clock domains.

  Depending on the clock source selection and the DPLL settings, SGX_FCLK can support a frequency of up to 384 MHz.

  The SGX_FCLK clock is provided by either the PRCM module or the peripheral DPLL, as described in Section 3.6.11, *CD_SGX Clock Domains*. Selection is made at the PRCM level.

  When no longer needed by the SGX subsystem, SGX_FCLK can be cut by software at the PRCM level, if the module is ready to enter the IDLE state. For more information, see Section 3.7.8, *PD_SGX Description*.

11.3.3 SGX Software Reset

The SGX subsystem has its own reset domain. Global reset of the SGX is performed by activating the SGX_RST signal in the SGX_RST domain.

NOTE: The APIs delivered with the SGX provide a software reset functionally equivalent to a hardware reset.

11.3.4 SGX Power Management

The SGX subsystem has its own power domain (SGX power domain). For additional information about the SGX power domain, see Section 3.7.8, *PD_SGX Description*, in Chapter 3, *Power, Reset, and Clock Management*.

NOTE: The SGX handles automatic clock gating performed on the multiple internal module clock domains.

In addition, software-controlled clock gating is managed inside the SGX and handled by the related API delivered with the module.

11.3.5 SGX Interrupt Requests

The SGX subsystem can generate one interrupt signal to the MPU INTC mapped to SGX_IRQ.

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11.4 SGX Register Manual

CAUTION

All SGX registers are limited to 32-bit data accesses; 8- and 16-bit accesses are not allowed because they can corrupt register content.

11.4.1 SGX Instance Summary

Table 11-4. SGX Instance Summary

Module Name	Base Address	Size
SGX	0x5600 0000	32MB

11.4.2 SGX OCP Registers

11.4.2.1 SGX OCP Register Summary

Table 11-5. SGX Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	SGX Physical Address
OCP_REVISION	R	32	0x0000 FE00	0x5600 FE00
OCP_HWINFO	R	32	0x0000 FE04	0x5600 FE04
OCP_SYSCONFIG	RW	32	0x0000 FE10	0x5600 FE10
OCP_IRQSTATUS_RAW_0	RW	32	0x0000 FE24	0x5600 FE24
OCP_IRQSTATUS_RAW_1	RW	32	0x0000 FE28	0x5600 FE28
OCP_IRQSTATUS_RAW_2	RW	32	0x0000 FE2C	0x5600 FE2C
OCP_IRQSTATUS_0	RW	32	0x0000 FE30	0x5600 FE30
OCP_IRQSTATUS_1	RW	32	0x0000 FE34	0x5600 FE34
OCP_IRQSTATUS_2	RW	32	0x0000 FE38	0x5600 FE38
OCP_IRQENABLE_SET_0	RW	32	0x0000 FE3C	0x5600 FE3C
OCP_IRQENABLE_SET_1	RW	32	0x0000 FE40	0x5600 FE40
OCP_IRQENABLE_SET_2	RW	32	0x0000 FE44	0x5600 FE44
OCP_IRQENABLE_CLR_0	RW	32	0x0000 FE48	0x5600 FE48
OCP_IRQENABLE_CLR_1	RW	32	0x0000 FE4C	0x5600 FE4C
OCP_IRQENABLE_CLR_2	RW	32	0x0000 FE50	0x5600 FE50
OCP_PAGE_CONFIG	RW	32	0x0000 FF00	0x5600 FF00
OCP_INTERRUPT_EVENT	RW	32	0x0000 FF04	0x5600 FF04
OCP_DEBUG_CONFIG	RW	32	0x0000 FF08	0x5600 FF08
OCP_DEBUG_STATUS	RW	32	0x0000 FF0C	0x5600 FF0C

11.4.2.2 SGX OCP Register Description

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Table 11-6. OCP_REVISION

Address Offset	0x0000 FE00		
Physical Address	0x5600 FE00	**Instance**	SGX
Description	OCP Revision Register.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISIONID																															

Bits	Field Name	Description	Type	Reset
31:0	REVISIONID	Revision value.	R	See (1)

(1) TI internal data

Table 11-7. Register Call Summary for Register OCP_REVISION

SGX Register Manual

- SGX OCP Register Summary: [0]

Table 11-8. OCP_HWINFO

Address Offset	0x0000 FE04		
Physical Address	0x5600 FE04	**Instance**	SGX
Description	Hardware implementation information		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													MEM_BUS_WIDTH	SYS_BUS_WIDTH	

Bits	Field Name	Description	Type	Reset
31:3	RESERVED		R	0x0000 0000
2	MEM_BUS_WIDTH	Memory bus width: Read 0x0: Memory bus width is 64 bits. Read 0x1: Memory bus width is 128 bits.	R	–
1:0	SYS_BUS_WIDTH	System bus width: Read 0x0: System bus width is 32 bits. Read 0x1: System bus width is 64 bits. Read 0x2: System bus width is 128 bits. Read 0x3: Reserved	R	0x-

Table 11-9. Register Call Summary for Register OCP_HWINFO

SGX Register Manual

- SGX OCP Register Summary: [0]

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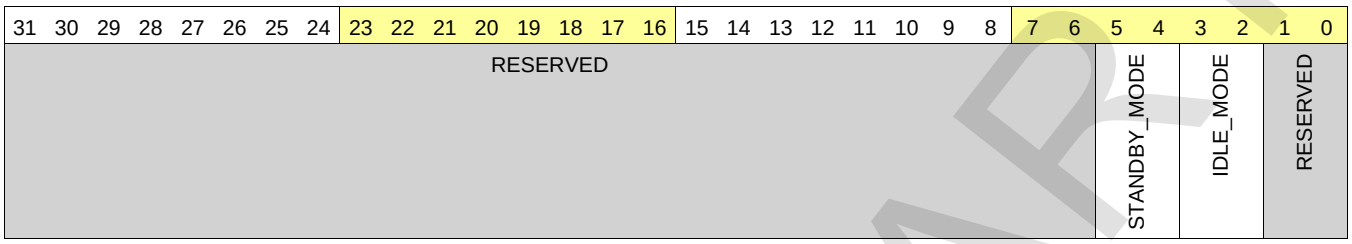
Table 11-10. OCP_SYSCONFIG

Address Offset	0x0000 FE10		
Physical Address	0x5600 FE10	**Instance**	SGX
Description	System Configuration register		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:6	RESERVED		R	0x0000000
5:4	STANDBY_MODE	Clock standby mode: 0x0: Force-standby mode 0x1: No-standby mode 0x2, 0x3: Smart-standby mode	RW	0x2
3:2	IDLE_MODE	Clock Idle mode: 0x0: Force-idle mode 0x1: No-idle mode 0x2, 0x3: Smart-idle mode	RW	0x2
1:0	RESERVED		R	0x0

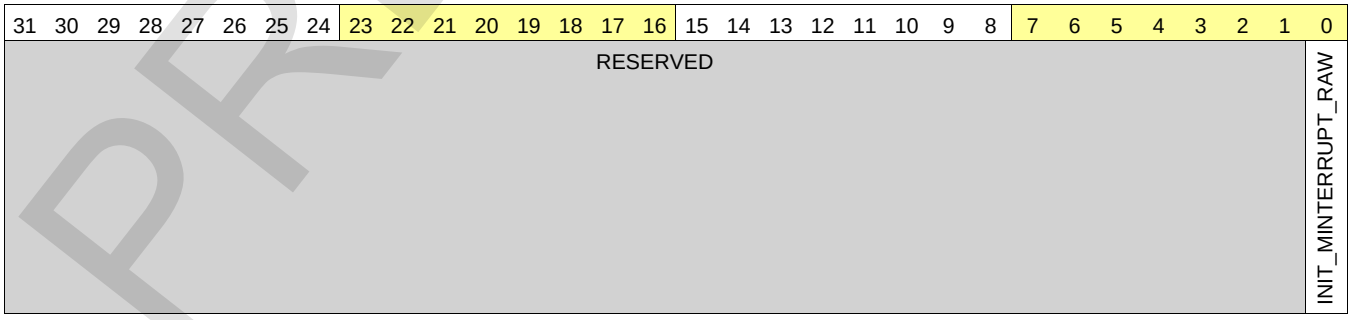
Table 11-11. Register Call Summary for Register OCP_SYSCONFIG

SGX Register Manual

- SGX OCP Register Summary: [0]

Table 11-12. OCP_IRQSTATUS_RAW_0

Address Offset	0x0000 FE24		
Physical Address	0x5600 FE24	**Instance**	SGX
Description	Raw IRQ 0 Status		
Type	RW		



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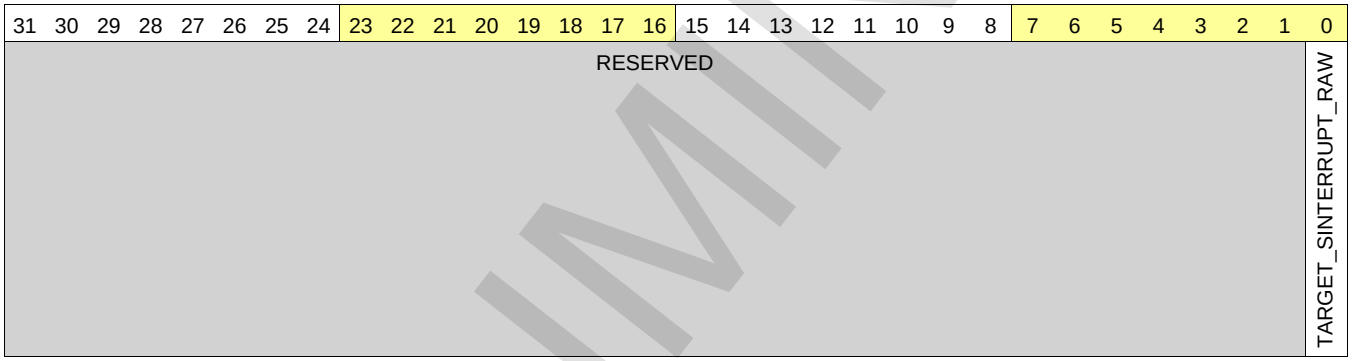
Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	INIT_MINTERRUPT_RAW	Interrupt 0 - Master port raw event: Write 0x0: No action. Read 0x0: No event pending. Read 0x1: Event pending. Write 0x1: Set event (used for debug).	RW	0

Table 11-13. Register Call Summary for Register OCP_IRQSTATUS_RAW_0

SGX Register Manual
- SGX OCP Register Summary: [0]

Table 11-14. OCP_IRQSTATUS_RAW_1

Address Offset	0x0000 FE28		
Physical Address	0x5600 FE28	**Instance**	SGX
Description	Raw IRQ 1 Status. Slave port interrupt.		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	TARGET_SINTERRUPT_RAW	Interrupt 1- Slave port raw event Write 0x0: No action. Read 0x0: No event pending. Read 0x1: Event pending. Write 0x1: Set event (used for debug).	RW	0

Table 11-15. Register Call Summary for Register OCP_IRQSTATUS_RAW_1

SGX Register Manual
- SGX OCP Register Summary: [0]

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Table 11-16. OCP_IRQSTATUS_RAW_2

Address Offset	0x0000 FE2C		
Physical Address	0x5600 FE2C	**Instance**	SGX
Description	Raw IRQ 2 Status. Core interrupt.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															CORE_IRQ_RAW

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	CORE_IRQ_RAW	Interrupt 2 - Core raw event Write 0x0: No action. Read 0x0: No event pending. Read 0x1: Event pending. Write 0x1: Set event (used for debug).	RW	0

Table 11-17. Register Call Summary for Register OCP_IRQSTATUS_RAW_2

SGX Register Manual

- SGX OCP Register Summary: [0]

Table 11-18. OCP_IRQSTATUS_0

Address Offset	0x0000 FE30		
Physical Address	0x5600 FE30	**Instance**	SGX
Description	Interrupt 0 Status event. Master port interrupt.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															INIT_MINTERRUPT_STATUS

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Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	INIT_MINTERRUPT_STATUS	Interrupt 0 - Master port status event Write 0x0: No action. Read 0x0: No event pending. Read 0x1: Event pending and interrupt enabled. Write 0x1: Clear event.	RW	0

Table 11-19. Register Call Summary for Register OCP_IRQSTATUS_0

SGX Register Manual
- SGX OCP Register Summary: [0]

Table 11-20. OCP_IRQSTATUS_1

Address Offset	0x0000 FE34		
Physical Address	0x5600 FE34	**Instance**	SGX
Description	Interrupt 1 - slave port status event		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															TARGET_SINTERRUPT_STATUS

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	TARGET_SINTERRUPT_STATUS	Interrupt 1 - Slave port status event Write 0x0: No action. Read 0x0: No event pending. Read 0x1: Event pending and interrupt enabled. Write 0x1: Clear event.	RW	0

Table 11-21. Register Call Summary for Register OCP_IRQSTATUS_1

SGX Register Manual
- SGX OCP Register Summary: [0]

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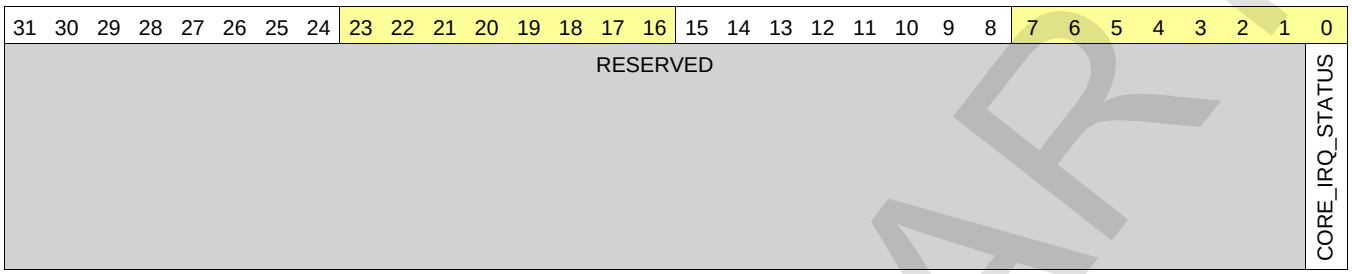
Table 11-22. OCP_IRQSTATUS_2

Address Offset	0x0000 FE38		
Physical Address	0x5600 FE38	**Instance**	SGX
Description	Interrupt 2 - Core status event		
Type	RW		



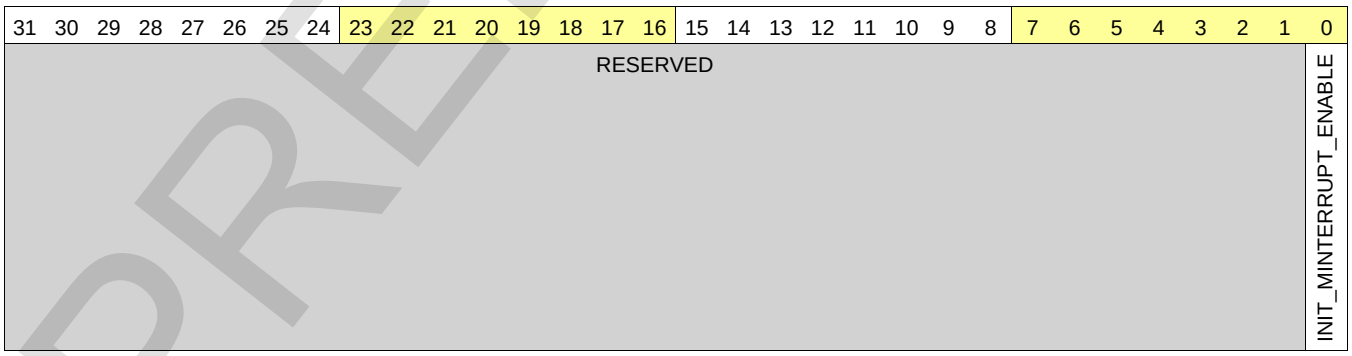
Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	CORE_IRQ_STATUS	Interrupt 2 - Core status event Write 0x0: No action. Read 0x0: No event pending. Read 0x1: Event pending and interrupt enabled. Write 0x1: Clear event.	RW	0

Table 11-23. Register Call Summary for Register OCP_IRQSTATUS_2

SGX Register Manual
- SGX OCP Register Summary: [0]

Table 11-24. OCP_IRQENABLE_SET_0

Address Offset	0x0000 FE3C		
Physical Address	0x5600 FE3C	**Instance**	SGX
Description	Enable Interrupt 0 - Master port		
Type	RW		



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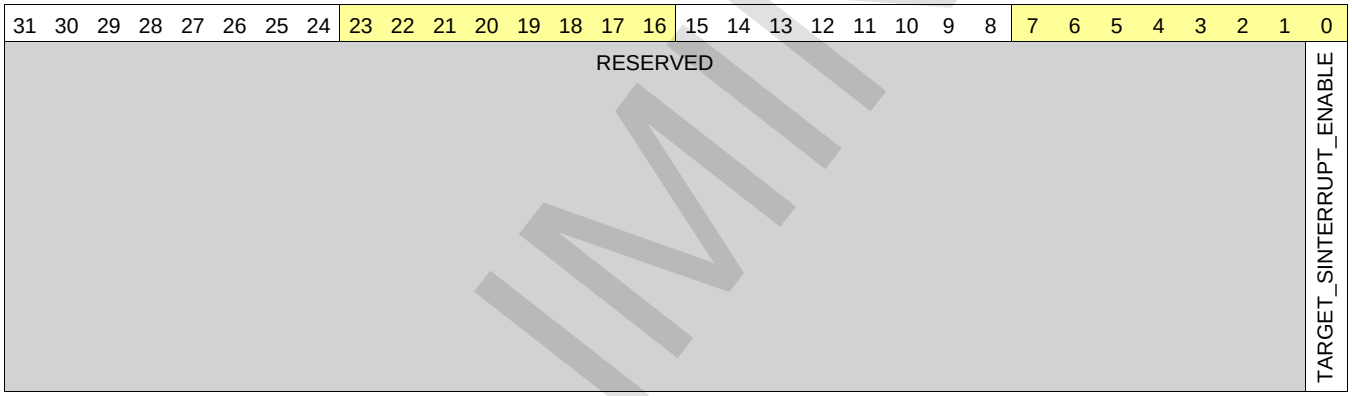
Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	INIT_MINTERRUPT_ENABLE	Enable interrupt 0 - Master port Write 0x0: No action. Read 0x0: Interrupt is enabled. Read 0x1: Interrupt is disabled. Write 0x1: Enable interrupt.	RW	0

Table 11-25. Register Call Summary for Register OCP_IRQENABLE_SET_0

SGX Register Manual
- SGX OCP Register Summary: [0]

Table 11-26. OCP_IRQENABLE_SET_1

Address Offset	0x0000 FE40		
Physical Address	0x5600 FE40	**Instance**	SGX
Description	Enable Interrupt 1. Target port interrupt.		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	TARGET_SINTERRUPT_ENABLE	Enable interrupt 1 - Slave port interrupt Write 0x0: No action. Read 0x0: Interrupt is enabled. Read 0x1: Interrupt is disabled. Write 0x1: Enable interrupt.	RW	0

Table 11-27. Register Call Summary for Register OCP_IRQENABLE_SET_1

SGX Register Manual
- SGX OCP Register Summary: [0]

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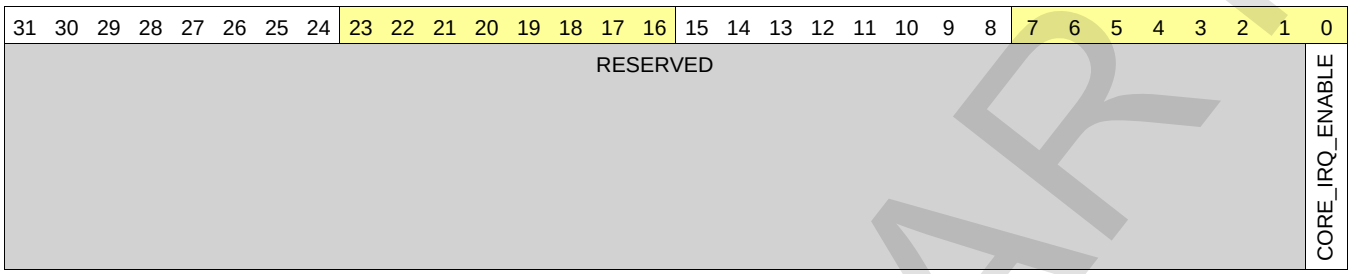
Table 11-28. OCP_IRQENABLE_SET_2

Address Offset	0x0000 FE44		
Physical Address	0x5600 FE44	**Instance**	SGX
Description	Enable Interrupt 2. Core interrupt.		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	CORE_IRQ_ENABLE	Enable interrupt 2 - Core interrupt Write 0x0: No action. Read 0x0: Interrupt is enabled. Read 0x1: Interrupt is disabled. Write 0x1: Enable interrupt.	RW	0

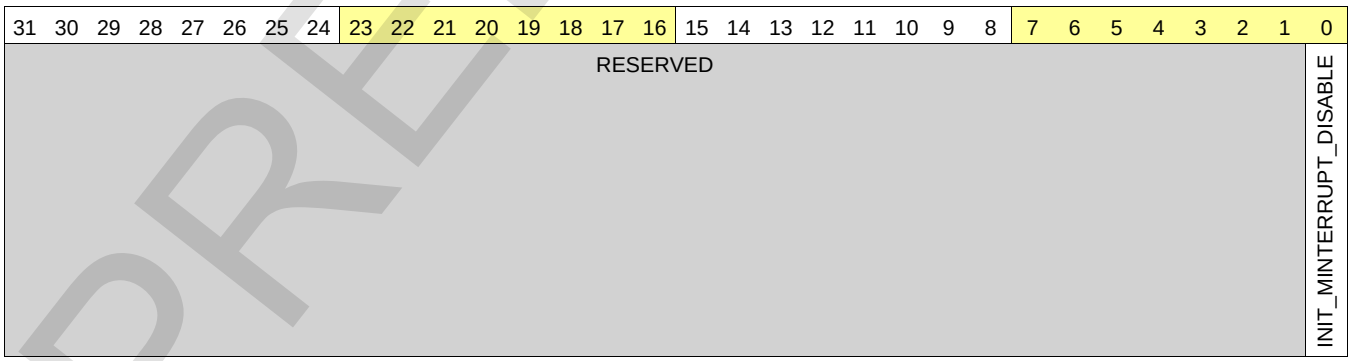
Table 11-29. Register Call Summary for Register OCP_IRQENABLE_SET_2

SGX Register Manual

- SGX OCP Register Summary: [0]

Table 11-30. OCP_IRQENABLE_CLR_0

Address Offset	0x0000 FE48		
Physical Address	0x5600 FE48	**Instance**	SGX
Description	Disable Interrupt 0 - Master port		
Type	RW		



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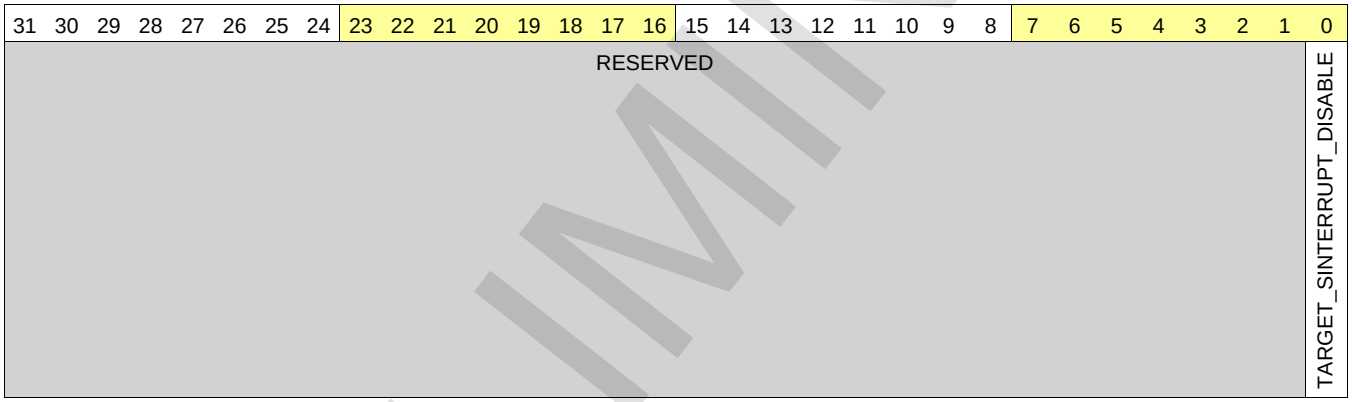
Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	INIT_MINTERRUPT_DISABLE	Disable interrupt 0 - Master port Write 0x0: No action. Read 0x0: Interrupt is enabled. Read 0x1: Interrupt is disabled. Write 0x1: Disable interrupt.	RW	0

Table 11-31. Register Call Summary for Register OCP_IRQENABLE_CLR_0

SGX Register Manual
- SGX OCP Register Summary: [0]

Table 11-32. OCP_IRQENABLE_CLR_1

Address Offset	0x0000 FE4C		
Physical Address	0x5600 FE4C	**Instance**	SGX
Description	Disable Interrupt 1 - slave port		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	TARGET_SINTERRUPT_DISABLE	Disable interrupt 1 - Slave port Write 0x0: No action. Read 0x0: Interrupt is enabled. Read 0x1: Interrupt is disabled. Write 0x1: Disable interrupt.	RW	0

Table 11-33. Register Call Summary for Register OCP_IRQENABLE_CLR_1

SGX Register Manual
- SGX OCP Register Summary: [0]

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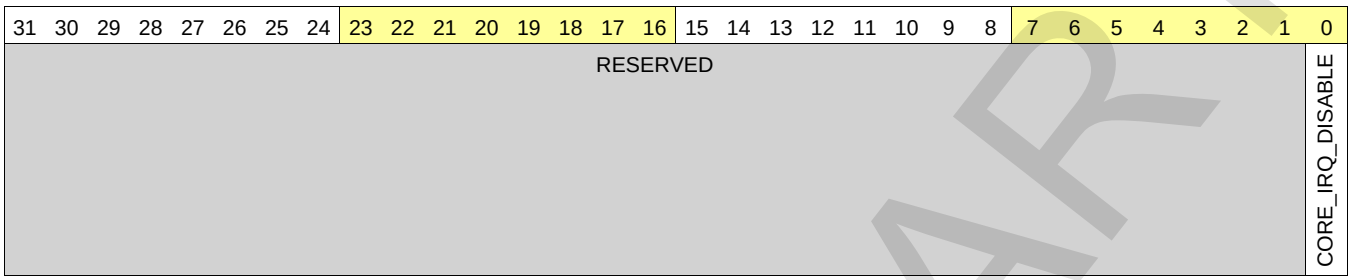
Table 11-34. OCP_IRQENABLE_CLR_2

Address Offset	0x0000 FE50		
Physical Address	0x5600 FE50	**Instance**	SGX
Description	Disable Interrupt 2 - Core interrupt		
Type	RW		



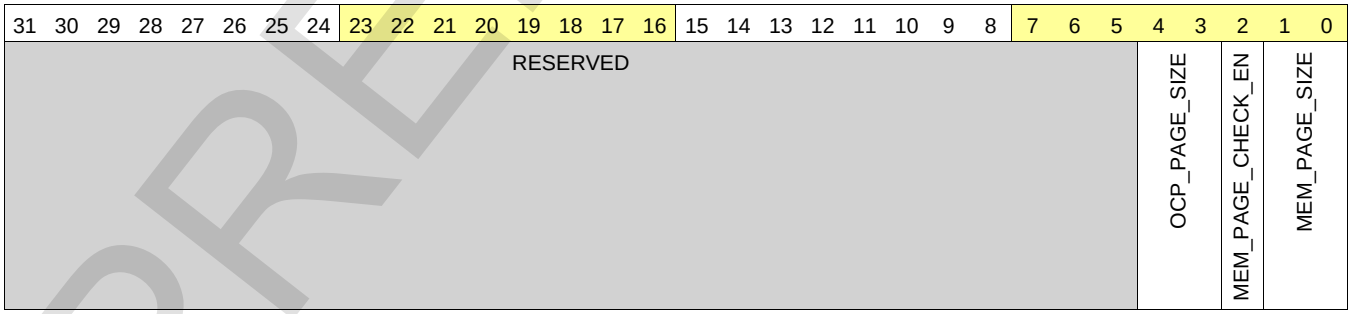
Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	CORE_IRQ_DISABLE	Disable interrupt 2 - Core interrupt Write 0x0: No action. Read 0x0: Interrupt is enabled. Read 0x1: Interrupt is disabled. Write 0x1: Disable interrupt.	RW	0

Table 11-35. Register Call Summary for Register OCP_IRQENABLE_CLR_2

SGX Register Manual
- SGX OCP Register Summary: [0]

Table 11-36. OCP_PAGE_CONFIG

Address Offset	0x0000 FF00		
Physical Address	0x5600 FF00	**Instance**	SGX
Description	Configure memory pages..		
Type	RW		



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Bits	Field Name	Description	Type	Reset
31:5	RESERVED		R	0x0000000
4:3	OCP_PAGE_SIZE	Defines the page size on OCP memory interface 0x0: Page size is 4KB. 0x1: Page size is 2KB 0x2: Page size is 1KB. 0x3: Page size is 512B.	RW	0x2
2	MEM_PAGE_CHECK_EN	Enable page boundary checking. 0x0: Page boundary checking disabled. 0x1: Page boundary checking enabled.	RW	1
1:0	MEM_PAGE_SIZE	Defines the page size on internal memory interface 0x0: Page size is 4KB. 0x1: Page size is 2KB 0x2: Page size is 1KB. 0x3: Page size is 512B.	RW	0x0

Table 11-37. Register Call Summary for Register OCP_PAGE_CONFIG

SGX Register Manual

- SGX OCP Register Summary: [0]

Table 11-38. OCP_INTERRUPT_EVENT

Address Offset	0x0000 FF04		
Physical Address	0x5600 FF04	**Instance**	SGX
Description	Interrupt events		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																					TARGET_INVALID_OCP_CMD	TARGET_CMD_FIFO_FULL	TARGET_RESP_FIFO_FULL	RESERVED		INIT_MEM_REQ_FIFO_OVERRUN	INIT_READ_TAG_FIFO_OVERRUN	INIT_PAGE_CROSS_ERROR	INIT_RESP_ERROR	INIT_RESP_UNUSED_TAG	INIT_RESP_UNEXPECTED

Bits	Field Name	Description	Type	Reset
31:11	RESERVED		R	0x000000
10	TARGET_INVALID_OCP_CMD	Invalid command from OCP Write 0x0: Clear the event. Read 0x0: No event pending. Read 0x1: Event pending. Write 0x1: Set event and interrupt if enabled (debug only).	RW	0

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Bits	Field Name	Description	Type	Reset
9	TARGET_CMD_FIFO_FULL	Command FIFO full Write 0x0: Write 0 to clear the event. Read 0x0: Read 0 implies no event pending. Read 0x1: Read 1 indicates event pending. Write 0x1: Write 1 to set event and interrupt if enabled (debug only).	RW	0
8	TARGET_RESP_FIFO_FULL	Response FIFO full. Write 0x0: Clear the event. Read 0x0: No event pending. Read 0x1: Event pending. Write 0x1: Set event and interrupt if enabled (debug only).	RW	0
7:6	RESERVED		R	0x0
5	INIT_MEM_REQ_FIFO_OVERRUN	Memory request FIFO overrun. Write 0x0: Clear the event. Read 0x0: No event pending. Read 0x1: Event pending. Write 0x1: Set event and interrupt if enabled (debug only).	RW	0
4	INIT_READ_TAG_FIFO_OVERRUN	Read tag FIFO overrun. Write 0x0: Clear the event. Read 0x0: No event pending. Read 0x1: Event pending. Write 0x1: Set event and interrupt if enabled (debug only).	RW	0
3	INIT_PAGE_CROSS_ERROR	Memory page had been crossed during a burst. Write 0x0: Clear the event. Read 0x0: No event pending. Read 0x1: Event pending. Write 0x1: Set event and interrupt if enabled (debug only).	RW	0
2	INIT_RESP_ERROR	Receiving error response Write 0x0: Clear the event. Read 0x0: No event pending. Read 0x1: Event pending. Write 0x1: Set event and interrupt if enabled (debug only).	RW	0
1	INIT_RESP_UNUSED_TAG	Receiving response on an unused tag Write 0x0: Clear the event. Read 0x0: No event pending. Read 0x1: Event pending. Write 0x1: Set event and interrupt if enabled (debug only).	RW	0
0	INIT_RESP_UNEXPECTED	Receiving response when not expected Write 0x0: Clear the event. Read 0x0: No event pending. Read 0x1: Event pending. Write 0x1: Set event and interrupt if enabled (debug only).	RW	0

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Table 11-39. Register Call Summary for Register OCP_INTERRUPT_EVENT

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- SGX OCP Register Summary: [0]

Table 11-40. OCP_DEBUG_CONFIG

Address Offset	0x0000 FF08		
Physical Address	0x5600 FF08	**Instance**	SGX
Description	Configuration of debug modes.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CORE_INT_BYPASS	RESERVED																									SELECT_INIT_IDLE	FORCEPASSDATA	FORCEINITIDLE		FORCETARGETIDLE	

Bits	Field Name	Description	Type	Reset
31	CORE_INT_BYPASS	Bypass OCP IPG interrupt logic. 0x0: Don't Bypass. 0x1: Bypass core interrupt to IO pin, ie disregard the interrupt enable setting in IPG register.	RW	0
30:6	RESERVED		R	0x0000000
5	SELECT_INIT_IDLE	To select which idle the disconnect protocol should act on 0 0x0: Whole SGX Idle. 0x1: OCP initiator idle only.	RW	0
4	FORCE_PASS_DATA	Forces the initiator to pass data independent of disconnect protocol 0x0: Normal mode. Don't force. 0x1: Never fence request to OCP.	RW	0
3:2	FORCE_INIT_IDLE	Forces the OCP master port to idle. 0x0: Normal mode - no force. 0x1: Force port to be always idle. 0x2: Forces target port to never be in idle mode. 0x3: Normal mode. No force.	RW	0x0
1:0	FORCE_TARGET_IDLE	Forces the OCP target port to idle. 0x0: Normal mode - no force. 0x1: Force port to be always idle. 0x2: Forces target port to never be in idle mode. 0x3: Normal mode. No force.	RW	0x0

Table 11-41. Register Call Summary for Register OCP_DEBUG_CONFIG

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- SGX OCP Register Summary: [0]

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Table 11-42. OCP_DEBUG_STATUS

Address Offset	0x0000 FF0C		
Physical Address	0x5600 FF0C	**Instance**	SGX
Description	Status of debug.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMD_DEBUG_STATE	CMD_RESP_DEBUG_STATE	TARGET_IDLE	RESP_FIFO_FULL	CMD_FIFO_FULL	RESP_ERROR	WHICH_TARGET_REGISTER					TARGET_CMD_OUT			INIT_MSTANDBY	INIT_MWAIT	INIT_MDISCREQ		INIT_MDISCACK	INIT_SCONNECT2	INIT_SCONNECT1	INIT_SCONNECT0	INIT_MCONNECT		TARGET_SIDLEACK		TARGET_SDISCACK		TARGET_SIDLEREQ	TARGET_SCONNECT	TARGET_MCONNECT	

Bits	Field Name	Description	Type	Reset
31	CMD_DEBUG_STATE	Target command state-machine 0x0: Idle 0x1: Accept command.	RW	–
30	CMD_RESP_DEBUG_STATE	Target response state-machine 0x0: Send accept. 0x1: Wait accept.	RW	–
29	TARGET_IDLE	Target idle	R	–
28	RESP_FIFO_FULL	Target response FIFO full	R	–
27	CMD_FIFO_FULL	Target command FIFO full	R	–
26	RESP_ERROR	Respond to OCP with error, which could be caused by either address misalignment or invalid byte enable.	R	–
25:21	WHICH_TARGET_REGISTER	Indicates which OCP target registers to read	RW	0bxxxxx
20:18	TARGET_CMD_OUT	Command received from OCP Read 0x0: Command WRSYS received Read 0x1: Command RDSYS received Read 0x2: Command WR_ERROR received Read 0x3: Command RD_ERROR received Read 0x4: Command CHK_WRADDR_PAGE received. Not used. Read 0x5: Command CHK_RDADDR_PAGE received. Not used. Read 0x6: Command TARGET_REG_WRITE received. Read 0x7: Command TARGET_REG_READ received	R	0bxxx
17	INIT_MSTANDBY	Status of init_MStandby signal	R	–
16	INIT_MWAIT	Status of init_MWait signal	R	–
15:14	INIT_MDISCREQ	Disconnect status of the OCP interface Read 0x0: State is FUNCT Read 0x1: State is SLEEP TRANS Read 0x2: Reserved Read 0x3: State is IDLE.	R	0bxx

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Bits	Field Name	Description	Type	Reset
13	INIT_MDISCACK	Memory request FIFO full Write 0x0: Clear the event. Read 0x0: No event pending Read 0x1: Event pending Write 0x1: Set the event and interrupt if enabled (debug only)	RW	–
12	INIT_SCONNECT2	Defines whether to wait in M_WAIT state for MConnect FSM Read 0x0: Skip M_WAIT state. Read 0x1: Wait in M_WAIT state.	R	–
11	INIT_SCONNECT1	Defines the busy-ness state of the slave Read 0x0: Slave is drained. Read 0x1: Slave is loaded.	R	–
10	INIT_SCONNECT0	Disconnect from slave Read 0x0: Disconnect request from slave. Read 0x1: Connect request from slave.	R	–
9:8	INIT_MCONNECT	Initiator MConnect state Read 0x0: State is M_OFF. Read 0x1: State is M_WAIT. Read 0x2: State is M_DISC. Read 0x3: State is M_CON.	R	0bxx
7:6	TARGET_SIDLEACK	Acknowledge the SIdleAck state machine Read 0x0: State is FUNCT. Read 0x1: State is SLEEP TRANS. Read 0x2: Reserved Read 0x3: State is IDLE.	R	0bxx
5:4	TARGET_SDISCACK	Acknowledge the SDiscAck state-machine Read 0x0: State is FUNCT. Read 0x1: State is TRANS. Read 0x2: Reserved Read 0x3: State is IDLE.	R	0bxx
3	TARGET_SIDLEREQ	Request the target to go idle. Read 0x0: Don't go idle, or go active. Read 0x1: Go idle.	R	–
2	TARGET_SCONNECT	Target SConnect state Read 0x0: Disconnect interface. Read 0x1: Connect OCP interface.	R	–
1:0	TARGET_MCONNECT	Target MConnect state Read 0x0: Target is in M_OFF state. Read 0x1: Target is in M_WAIT disconnect state. Read 0x2: Target is in M_DISC state. Read 0x3: Target is in M_CON state.	R	0bxx

Table 11-43. Register Call Summary for Register OCP_DEBUG_STATUS

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- SGX OCP Register Summary: [0]

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Audio Back End

This chapter describes the audio back end (ABE) module.

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12.1 ABE Overview

The audio back end (ABE) module is a subsystem that manages various audio and voice uplink and downlink streams between the initiator (the Cortex™-A9 microprocessor unit [MPU], digital signal processor [DSP], or direct memory access [DMA] controller) and the peripheral physical interfaces (multichannel buffered serial port [McBSP], SLIMbus®, digital microcontroller [DMIC], multichannel pulse density modulation [McPDM], and multichannel audio serial port [McASP]).

The ABE module handles the audio processing for the applications. It receives voice or audio samples from the initiator or the external audio chip (TWL6040 or other) and sends them to the peripheral interfaces or memories after processing. The ABE can perform buffering of audio samples, mix audio with a voice down stream and/or a microphone up stream (sidetone), and can apply some post-processing.

The ABE integrates the following modules:

- Peripheral physical interfaces:
  - Three McBSP modules
  - One McASP module
  - One mobile industry processor interface (MIPI) SLIMbus interface
  - One DMIC module to support up to six mono and up to three stereo digital microphones
  - One McPDM module to support interconnect with an external audio chip.
- Audio engine (AE):
  - Performs real-time signal processing like sample rate conversion, filtering, equalizing, and side-tone
  - Audio traffic controller (ATC):
    - Performs data move in the ABE
    - Generates interrupt requests to the DSP and Cortex-A9 interrupt controllers
  - On-chip memory:
    - 64KB of RAM; 32-bit data memory (DMEM)
    - 6KB for coefficient memory RAM (CMEM)
    - 18KB for sample memory RAM (SMEM)
- Local L4 interconnect (L4_ABE) to:
  - L3 interconnect
  - Cortex-A9 MPU
  - DSP

  The Cortex-A9 MPU and the DSP have private access to the L4_ABE interconnect. All other initiators (sDMA) can access the L4_ABE only through the L3 interconnect.
- Timers:
  - Four general-purpose (GP) timers
  - One watchdog timer
- Clock and reset management: Receives clock and reset signals from the device PRCM module. The audio engine operates from the DPLL_ABE, which is in the PRCM module. The ABE modules can be supplied with clock signals from the DPLL_ABE or the DPLL_PER. The ABE has its own hardware reset domain (AUDIO_RST).
- Power management: The ABE module is power-independent. It has its own dedicated power domain (PD_ABE) and can execute audio processing with the rest of the device in retention or in off mode.
- Each peripheral in the ABE can be accessed directly by the initiator when the AE is bypassed (legacy mode, for old software compatability).

Figure 12-1 is a high-level overview of the ABE.

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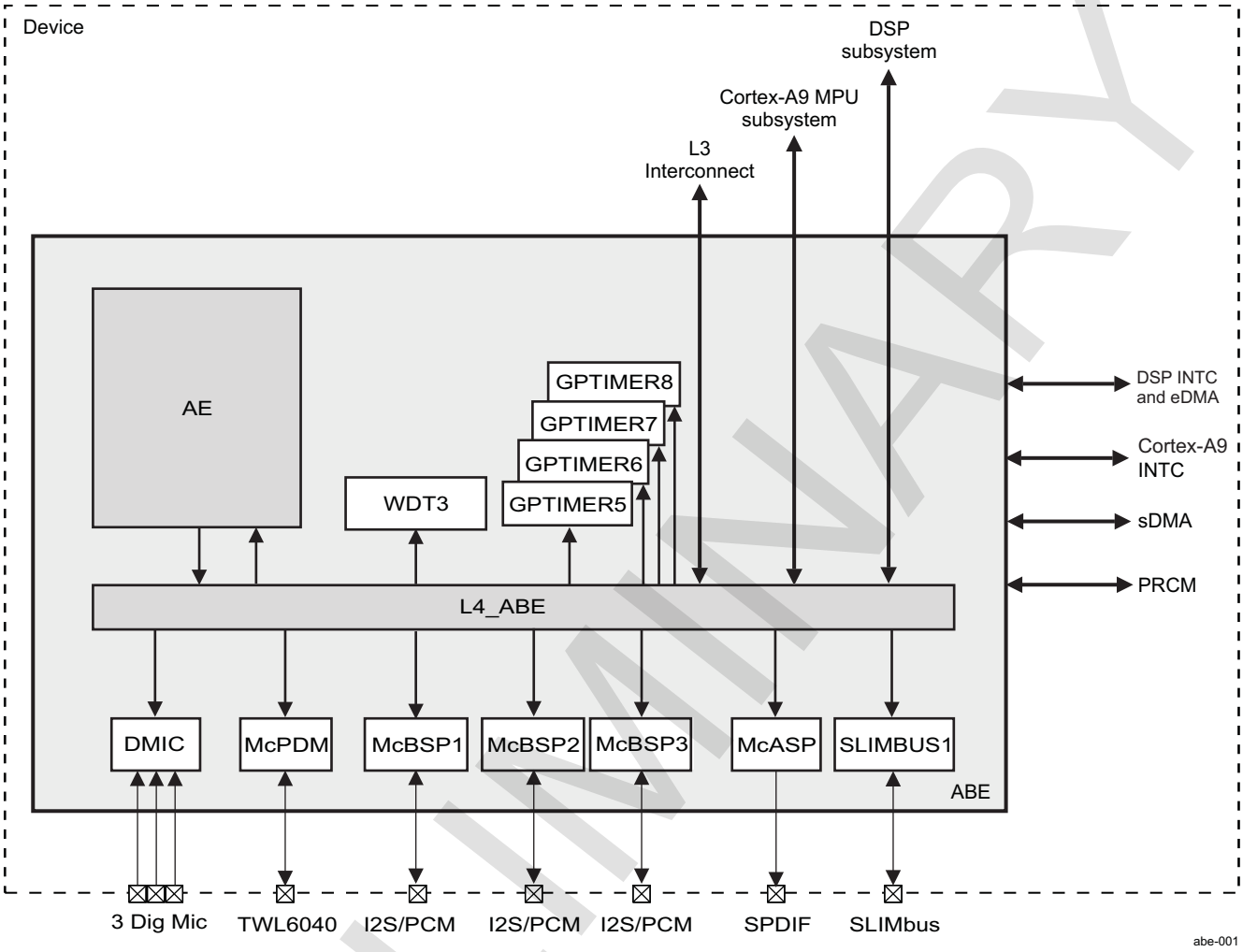
Figure 12-1. Audio Back End



12.1.1 AE Subsystem

The AE is the core of the ABE subsystem. It performs the real-time audio processing within the ABE: mixing, muxing, volume control, smooth muting, sampling rate conversion, and side-tone equalization. The AE subsystem also processes and executes all data transfers. To optimize the global processing, the ATC moves the data. An IRQ/DMA controller controls system IRQ and DMA requests. Input DMA requests come from the ABE peripherals, and output DMA requests and IRQ are generated and sent to the system (Cortex-A9 MPU interrupt controller, DSP interrupt controller, system DMA [sDMA], and the DSP enhanced direct memory access controller [eDMA]).

The AE subsystem contains:

- AE: processes the sample in SMEM with help of CMEM.
  - SMEM
  - CMEM
- DMEM contains the audio buffer and communication circular buffer.
- ATC: Transfers data between all modules in the ABE
- IRQ DMA controller

For more information about the audio engine, see the *Hardware Abstraction Layer (HAL) Addendum*.

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12.1.2 Local Audio Interconnect

The ABE has its own audio local interconnect (L4_ABE), which interconnects and manages the data flow among all ABE modules.

L4_ABE main features are:

- Initiator ports: Cortex-A9 MPU, DSP, L3 interconnect, and AE subsystem. The sDMA operates with the L4_ABE interconnect through the L3 interconnect initiator port. The eDMA operates with the L4_ABE interconnect through the DSP initiator port.
- Target ports:AE subsystem, McBSP1/2/3, DMIC, McPDM, McASP, GPTIMER5/6/7/8, WDT3, and SLIMBUS1
- 8-, 16-, or 32-bit data, single access
- 4-bit x 32-bit initiator ports for each interconnect instance
- Auto clock-gating feature
- Little-endian transaction assumed for all packing/unpacking operations
- Nonblocking architecture with fair arbitration between threads
- Target interconnect interfaces support fully synchronous and divided synchronous accesses.

For more information, see Chapter 13, *Interconnect*.

12.1.3 GP Timers

The ABE embeds four GP timers: GPTIMER5 through GPTIMER8. All GP timers have interrupts connected to the Cortex-A9 MPU, DSP, and AE subsystems.

GP timer controllers have the following functions:

- Interconnect slave interface (L4) supports:
  - 32-bit data bus width
  - 16-/32-bit access supported
  - 10-bit address bus width
  - Burst not supported
  - WNP (Write-Non-Posted) supported
- Interrupts generated on overflow, compare, and capture
- Free-running 32-bit upward counter
- Supported modes:
  - Compare and capture modes
  - Auto-reload mode
  - Start-stop mode
- Programmable divider clock source
- Dedicated input trigger for capture mode and dedicated OUT trigger/PWM signal
- On-the-fly read/write register
- Supports disconnect protocol

For more information, see Section 22.2, *General-Purpose Timers*.

12.1.4 Watchdog Timer

The ABE embeds one watchdog timer, WDT3, that generates an interrupt condition to the Cortex-A9 MPU on overflow, which can be used by the application software through the PRCM module to indirectly trigger a global warm reset.

WDT3 main features are:

- Interconnect slave interface (L4) supports:
  - 32-bit data bus width

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  - 16- and 32-bit access supported
  - 11-bit address bus width
  - Burst not supported
  - WNP supported
- Free-running 32-bit upward counter
- Programmable divider clock source
- Watchdog is reset on power up or after a warm reset and then starts counting.
- Reset or interrupt actions on a timer overflow condition and according to the watchdog timer source
- Support of disconnect protocol

For more information, see Section 22.3, *Watchdog Timers*.

12.1.5 Digital Microphone Controller

The DMIC allows support of up to three digital stereo microphones that send it a pulse-density modulated stream of bits, transferred on one period or one half-period of the clock (over-sampling clock) provided to the DMIC. Each microphone is directly connected to the TX filter decimator to extract the audio samples with a maximum OF 96 db SNR with a frequency sampling set to 96 kHz.

The DMIC has the following features:

- Six external pin connections (three data lines and three clock lines)
- Delivers one common clock (on the three clock lines) for all digital microphones
- Supports idle request/acknowledge protocol
- Supports stereo and mono digital microphones (up to three)
- Rising or falling edge configuration for the clock signal sampling
- DMIC-clock-programmable
- Interconnect slave interface (internal interconnect) supports 32-bit data bus width.
- One DMA request capability on a programmable FIFO threshold
- One RX FIFO (16-bit x 24-bit word depth) per microphone
- Complies with PRCM interrupts to the Cortex-A9 MPU and DSP subsystems
- Interconnect sample format: 32 bits (only 24 are significant)
- Supports idle request/acknowledge PRCM protocol

For more information, see Section 23.7, *DMIC*.

12.1.6 SLIMbus

There is one SLIMbus module instantiation inside the ABE, SLIMbus1. The SLIMbus controller provides a bidirectional, multidrop, multichannel 2-line serial interface between the ABE and up to seven off-chip components in a system such as an audio codec, a Bluetooth® module, or an FM radio receiver/transmitter. Because of its versatility, SLIMbus can accommodate a wide range of peripherals and clocked frame-oriented protocols (I2S, pulse code modulation [PCM], time division multiplexing [TDM]).

SLIMbus has the following features:

- Supports idle request/acknowledge PRCM protocol
- Complies with MIPI SLIMbus standard version 1.0
- Interconnect slave interface (L4) supports:
  - 32-bit data bus width
  - 8-, 16-, and 32-bit access supported
  - 11-bit address bus width
  - Burst not supported
  - WNP supported
- Support of seven SLIMbus devices:

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  - One manager
  - One framer
  - One interface
  - Four generic
- Message protocol partially implemented in SLIMbus module hardware:
  - Information elements are not stored in the module.
  - Message interpretation is not processed in the module.
  - FIFO size: 32 bytes for TX, 32 bytes for RX
- Support for eight TX and eight RX independent ports (data channels):
  - Supported transport protocols: Isochronous, pulled, pushed, asynchronous
  - Programmable segment data length (sample size) from 8 to 32 bits (8, 12, 16, 20, 24, 28, 32), including DATA and AUX
  - Programmable FIFO sizes
  - Programmable port assignment to any of the four generic devices
  - One DMA request line per port
- Operating frequencies of 0 to 24.576 MHz
- Supports disconnect protocol

For more information, see Section 23.9, *Serial Low-Power Inter-Chip Media Bus Controller*.

12.1.7 Multichannel Audio Serial Port

The multichannel audio serial port (McASP) is a GP audio serial port. It is useful for intercomponent (DIT) transmission. The McASP is intended to be flexible enough so that it may connect gluelessly to audio A/D, D/A, CODEC and SPDIF transmit physical layer components.

McASP has the following features:

- 2-interconnect slave interface supports:
  - One interconnect configuration slave interface
  - One interconnect DMA slave interface
  - 32-bit data bus width
  - 16- and 32-bit access
  - 10-bit address bus width
  - Burst not supported
  - WNP
- Supports idle request/acknowledge protocol
- Buffers for transmit/receive operations
- DMA requests (one per direction) link with the 32-bit register
- Up to four transmit channels
- Four serializers implemented
- Support of disconnect protocol

For more information, see Section 23.8, *McASP*.

12.1.8 Multichannel Buffered Serial Port

There are three McBSP instantiations: McBSP1 through McBSP3. They provide a full-duplex direct serial interface between the ABE and external devices, such as other modems, BT chips, or codecs. Because of its versatility, a McBSP can accommodate a wide range of peripherals and clocked frame-oriented protocols (I2S, PCM, TDM).

List of recommended usage per McBSP:

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- MCBSP1: BT voice/audio data
- MCBSP2: Digital baseband (DBB) voice data
- MCBSP3: MIDI FM data

The McBSP has the following features:

- Interconnect slave interface (internal interconnect) supports:
  - 32-bit data bus width
  - 8-, 16-, and 32- bit access
  - 10-bit address bus width
  - Burst not supported
  - WNP
- Buffers for transmit/receive operations: 128/128 32-bit words (McBSP1, 2, 3)
- Interrupts configurable in legacy mode (two requests) or PRCM-compliant (one request)
- DMA requests (one per direction) triggered with programmable FIFO thresholds
- Multidrop support
- Serial interface description
- Four-pin configuration (McBSP1, 2, 3)
- Full-duplex communication
- Multichannel selection modes
- Support to enable or block transfers in each channel
- Up to 128 channels for transmission and for reception
- Supported protocols
- Direct interface to industry-standard codecs, analog interface chips (AICs), and other serially connected A/D and D/A devices:
  - I2S-compliant devices
  - TDM bus devices
  - PCM devices
- A wide selection of data sizes: 8, 12, 16, 20, 24, and 32 bits
- Supports idle request/acknowledge protocol
- Clock generation support:
  - Independent clocking and framing for reception and for transmission up to 48 MHz
  - Support for external generation of clock signals and frame-synchronization (frame-sync) signals
  - A programmable sample rate generator for internal generation and control of clock signals and frame-sync signals
- Support of disconnect protocol

For a complete description, see Section 23.5, *Multichannel Buffered Serial Port*.

12.1.9 Multichannel Pulse Density Modulation Module

The McPDM is a proprietary interface based on multichannel pulse density modulation. The module consists of five downlinks and three uplinks. Two other uplink channels are reserved for status communication.

The McPDM has the following features:

- Interconnect slave interface (L4_ABE internal interconnect) supports:
  - 32-bit data bus width
  - 10-bit address bus width
  - Burst not supported
  - WNP

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- Full-duplex communication:
  - Five audio downstream channels
  - three audio upstream channels
- RX/TX FIFO operations: 32-bit words per channels
- Complies with PRCM interrupts:
  - One to the MPU subsystem
  - One to the DSP subsystem
- DMA requests (one per direction) triggered with programmable FIFO thresholds; depending on the FIFO implementation, one per channel or one per direction
- Decimation filter for embedded uplink paths (five paths if two status paths)
- Oversampling for embedded uplinks (five paths)
- Sigma delta for embedded downlinks (three paths)
- Deserializers for the two status upstream channels
- Support of disconnect protocol

For more information, see Section 23.6, *Multichannel PDM Controller*.

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Interconnect

This chapter describes the device interconnect.

NOTE: The L3 interconnect is instantiation of the NoC interconnect from Arteris, Inc. Arteris is a registered trademark of Arteris, Inc.

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NoC is an abbreviation for Network On Chip.

NOTE: The L4 interconnects are instantiations of the Sonics3220™ interconnect from Sonics, Inc.

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SMX is an abbreviation for SonicsMX.

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13.1 Interconnect Overview

13.1.1 Terminology

The following terminology is critical to understanding the interconnect:

- Initiator: Module able to initiate read and write requests to the chip interconnect (typically: processors, direct memory access [DMA], etc.).
- Target: Unlike an initiator, a target module cannot generate read/write requests to the chip interconnect, but it can respond to these requests. However, it may generate interrupts or a DMA request to the system (typically: peripherals, memory controllers).

NOTE: A module can have several separate ports; therefore, a module can be an initiator and a target.

- Agent: Each connection of one module to one interconnect is done using an agent, which is an adaptation (sometimes configurable) between the module and the interconnect. A target module is connected by a target agent (TA), and an initiator module is connected by an initiator agent (IA).
- Interconnect: The decoding, routing, and arbitration logic that enables the connection between multiple initiator modules and multiple target modules connected on it.
- Register target (RT): Special TA used to access the interconnect internal configuration registers
- Data-flow signal: Any signal that is part of a clearly identified transfer or data flow (typically: command, address, byte enables, etc.). Signal behavior is defined by the protocol semantics.
- Sideband signal: Any signal whose behavior is not associated to a precise transaction or data flow.
- Out-of-band error: Any signal whose behavior is associated to a device error-reporting scheme, as opposed to in-band errors.

NOTE: Interrupt requests and DMA requests are not routed by the interconnect in the device.

- Firewall: A programmable feature integrated in a TA or L4 interconnect to prevent unauthorized access to or from a module. A firewall can be configured using three criteria:
  - Initiator requesting access
  - Address space access
  - Type of access
- ConnID: Any transaction in the system interconnect is tagged by an in-band qualifier ConnID, which uniquely identifies the initiator at a given interconnect point. A ConnID is transmitted in band with the request and is used for firewall and error-logging mechanism.
- Firewall comparison mechanism: A comparison made in the firewall between access in-band qualifiers and access permissions that are programmed in the firewall configuration registers. If the comparison is successful, access is allowed; otherwise, access is denied.
- MCmd qualifier: Command bus that indicates the type of transfer requested. Table 13-1 lists the commands encoded. For information specific to L3 Interconnect error logging, see Table 13-26.

Table 13-1. MCmd Qualifier Description

MCmd[2:0]	Transaction Type
0 0 0	Idle
0 0 1	Write
0 1 0	Read
0 1 1	ReadEx
1 0 0	Not used
1 0 1	Write nonposted
1 1 0	Not used
1 1 1	Not used

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- MReqInfo qualifier: Four MReqInfo qualifiers describe the access during the use of the firewall comparison mechanism, as described in Table 13-2.

Table 13-2. MReqInfo Qualifier Description

Qualifiers	Description
MReqType	0: Data access
	1: Opcode fetch
MReqSupervisor	0: User mode
	1: Supervisor mode
MReqDebug	0: Functional access
	1: Debug access

- Register that configures the combination of the MReqInfo, allowing access permission to the TM based on the MReqInfo in-band qualifier values.
- SError: Target that indicates an error condition to the initiator.
- SResp qualifier: Response from the target to the initiator concerning the transaction, as described in Table 13-3.

Table 13-3. SResp Qualifier Description

SResp[1:0]	Description
0 0	No response
0 1	Data valid/accept
1 0	Not used
1 1	Error

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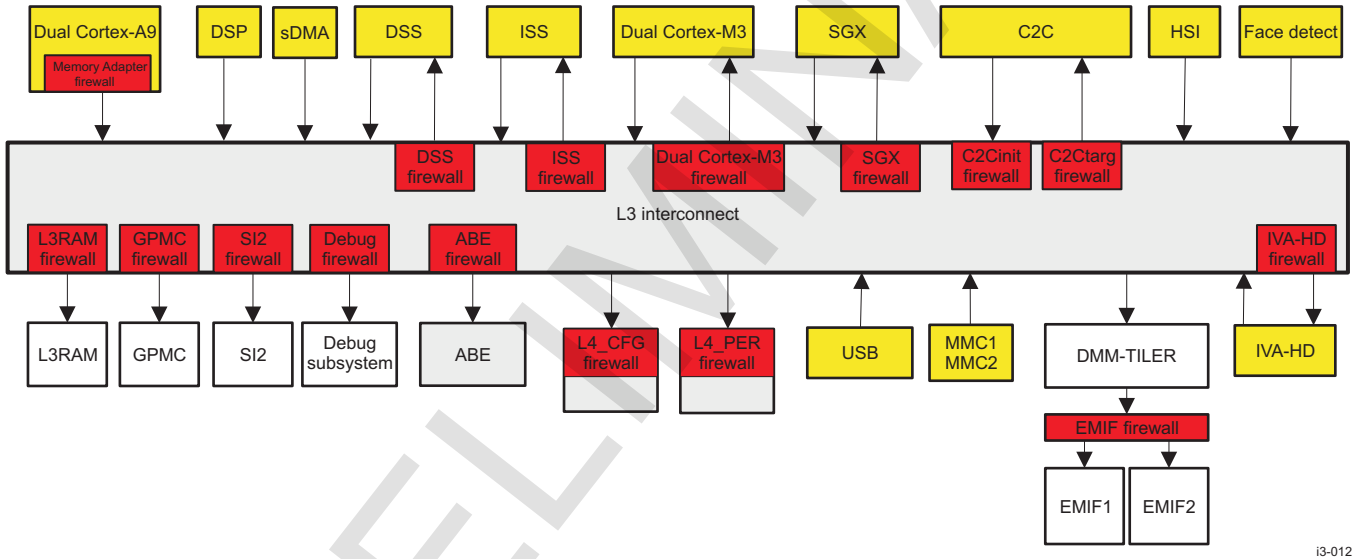
13.1.2 Architecture Overview

The device memory hierarchy includes four levels:

- Level 1 (L1) is internal to the central processing units (CPUs). It concerns data exchange with the internal Level 1 cache memory subsystem, and it is the closest memory to the microprocessor unit (MPU) core and the IVAHD core.
- Level 2 (L2) is included in the IVAHD subsystem and the MPU subsystem.
- The chip-level interconnect consists of one level 3 (L3) interconnect and four level 4 (L4) interconnects. It enables communication among the modules and subsystems in the device.

Figure 13-1 shows an overview of the L3 and L4 interconnect architecture.

Figure 13-1. Interconnect Overview



- L3 handles many types of data transfers, especially exchanges with system-on-chip (SoC)/external memories. L3 transfers data with a maximum width of 128 bits from the initiator to the target. The L3 interconnect is a little-endian platform.
- The L4 is composed of the following:
  - L4_CFG: Includes the majority of the configuration interface for L3 system modules and peripheral interconnect; L4_PER: Includes the main peripherals that require system direct memory access (sDMA).
  - L4_WKUP: Includes peripherals attached to the WKUP power domain.

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Modules are connected to the interconnect through an IA for the initiator module and a TA for target modules. Each module/subsystem connection is statically configured to tune the access, depending on the characteristics of the module.

To unauthorize a module or L4 interconnect access, some TAs include configurable firewalls (FWs). A firewall restricts or filters the accesses allowed to an initiator according to different access criteria. The firewalls can usually be configured by software.

The L3 and L4 interconnect default settings are fully functional; they enable all possible functional data paths and a minimal default protection setting. However, the interconnect parameters can be modified to fit user expectations.

13.1.3 Module Distribution

IAs and TAs provide the interface to connect the different modules and the interconnect.

Table 13-4 through Table 13-11 list the device modules, subsystems, and associated agents. The agents are listed for each interconnect domain:

- L3 initiator (master network interface units [NIUs] – MN) and target (slave NIUs – SN) agents
- L4_PER initiator and target agents
- L4_CFG initiator and target agents
- L4_WKUP initiator and target agents

13.1.3.1 L3 Interconnect Module Distribution

Table 13-4 and Table 13-5 list the IAs and TAs, respectively, of the L3 interconnect.

Table 13-4. Master NIUs

Master NIU Name	Description
L3_MN_CORTEXA9	Cortex™-A9 microprocessor unit subsystem
L3_MN_DSP	DSP subsystem
L3_MN_DSS	Display subsystem
L3_MN_MMC1/2	Multimedia controller
L3_MN_IVAHD	Video accelerator subsystem
L3_MN_SGX	Graphic accelerator
L3_MN_ISS	Imaging accelerator subsystem
L3_MN_CORTEXM3	Cortex™-M3 microprocessor subsystem
L3_MN_FACEDETECT	Face detection module
L3_MN_SDMA_rd	sDMA
L3_MN_SDMA_wr	sDMA
L3_MN_HSI	High-speed synchronous serial interface controller
L3_MN_FSUSB	Full-speed USB host controller
L3_MN_HSUSBOTG	High-speed (HS) on-the-go (OTG) USB controller
L3_MN_HSUSBHOST	Multiport USB host controller
L3_MN_C2C	Chip-to-chip (C2C)
L3_MN_DAP	JTAG®/emulation access to system resources

Table 13-5. Slave NIUs

Slave NIU Name	Description
L3_SN_OCM_RAM	On-chip memory controller
L3_SN_GPMC	General-purpose memory controller (GPMC)
L3_SN_C2C	Chip-to-chip
L3_SN_DMM1	Dynamic memory management

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Table 13-5. Slave NIUs (continued)

Slave NIU Name	Description
L3_SN_DMM2	Dynamic memory management
L3_SN_SGX	Graphic accelerator
L3_SN_ISS	Imaging accelerator subsystem
L3_SN_IVAHD_CFG	Video accelerator subsystem configuration
L3_SN_IVAHD_SL2	Video accelerator subsystem shared memory
L3_SN_DSP	DSP subsystem
L3_SN_CORTEXM3	Cortex-M3 MPU subsystem
L3_SN_DSS	Display subsystem
L3 interconnect	L3 internal registers
L3_SN_ABE	Audio back end
L3_SN_L4_CFG	L4 interconnect configuration
L3_SN_L4_PER0/1/2/3	L4 interconnect peripherals
L3_SN_L4_EMU	L4 interconnect EMU subsystem

13.1.3.2 L4 Interconnect Module Distribution

IAs and TAs provide the interface to connect the different modules to their associated interconnect.

Table 13-6 through Table 13-11 list all modules and subsystems with their associated agents. The agents are listed for each L4 interconnect domain.

13.1.3.2.1 L4_PER Interconnect Agents

The L4_PER interconnect handles transfers only to peripherals in the PER power domain. Table 13-6 lists the PER TAs.

Table 13-6. L4_PER TAs

Module Target Name	Description
PER_TA_UART1	Universal asynchronous receiver transmitter (UART) port 1 module
PER_TA_UART2	UART port 2 module
PER_TA_UART3	UART port 3 module
PER_TA_UART4	UART port 4 module
PER_TA_GPTIMER2	General-purpose timer 2 (GPTIMER2) module
PER_TA_GPTIMER3	GPTIMER3 module
PER_TA_GPTIMER4	GPTIMER4 module
PER_TA_GPTIMER9	GPTIMER9 module
PER_TA_GPTIMER10	GPTIMER10 module
PER_TA_GPTIMER11	GPTIMER11 module
PER_TA_DSS	Display subsystem configuration module
PER_TA_GPIO2	General-purpose input/output 2 (GPIO2) module
PER_TA_GPIO3	GPIO3 module
PER_TA_GPIO4	GPIO4 module
PER_TA_GPIO5	GPIO5 module
PER_TA_GPIO6	GPIO6 module
PER_TA_I2C1	Multimaster inter-integrated circuit 1 (I2C1) module
PER_TA_I2C2	Multimaster I2C2 module
PER_TA_I2C3	Multimaster I2C3 module
PER_TA_I2C4	Multimaster I2C4 module

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Table 13-6. L4_PER TAs (continued)

Module Target Name	Description
PER_TA_SLIMBUS2	Silmbus 2 module
PER_TA_ELM	Error location module
PER_TA_MCBSP4	Multichannel buffered serial port 4 (McBSP4) module
PER_TA_MCSPI1	Multichannel serial peripheral interface 1 (McBSP1) module
PER_TA_MCSPI2	McSPI2 module
PER_TA_MCSPI3	McSPI3 module
PER_TA_MCSPI4	McSPI4 module
PER_TA_HSMMC1	Multimedia card (MMC) controller 1 module
PER_TA_HSMMC2	MMC controller 2 module
PER_TA_HSMMC3	MMC controller 3 module
PER_TA_HSMMC4	MMC controller 4 module
PER_TA_HSMMC5	MMC controller 5 module
PER_TA_HDQ	Single-wire serial link low-rate module

Four ports communicate between the L3 interconnect and the L4_PER interconnect to allow the L3 initiators to access the L4_PER targets. Table 13-7 lists the L4_PER initiator TAs.

For the list of initiators authorized to access the L4 peripheral peripherals, see , *Connectivity Matrix*.

Table 13-7. L4_PER IAs

Module Initiator Name	Description
PER_IA_0	L3 sDMA RD interconnect port
PER_IA_1	L3 sDMA WR interconnect port
PER_IA_2	L3 MPU susbystem interconnect port
PER_IA_3	L3 others interconnect port

13.1.3.2.2 L4_CFG Interconnect Agents

The L4_CFG interconnect handles only transfers to peripherals in the CORE power domain. Table 13-8 lists the TAs.

Table 13-8. L4_CFG TAs

Module Target Name	Description
CFG_TA_SYSCTRL_GENERAL_CORE	System control general core module
CFG_TA_SYSCTRL_PADCONF_CORE	System control padconf core module
CFG_TA_CM1	Clock manager 1 module
CFG_TA_CM2	Clock manager 1 module
CFG_TA_SDMA	sDMA module
CFG_TA_HSI	HS synchronous serial interface (SSI) module
CFG_TA_SAR_ROM	Save-and-restore ROM
CFG_TA_HSUSBOTG	HS universal serial bus (USB) OTG module
CFG_TA_FSUSBHOST	FS USB OTG module
CFG_TA_HSUSBHOST	HS USB host module
CFG_TA_HSUSBPHY	HS USB PHY module
CFG_TA_HSUSBTLL	USB TTL module
CFG_TA_DSP	Digital signal processor (DSP) subsystem
CFG_TA_SR1	SmartReflex1 module

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Table 13-8. L4_CFG TAs (continued)

Module Target Name	Description
CFG_TA_SR2	SmartReflex2 module
CFG_TA_SR3	SmartReflex3 module
CFG_TA_MAILBOX	Mailbox module
CFG_TA_SPINLOCK	Spinlock module
CFG_TA_FACEDETECT	Face detect module
CFG_TA_EMIFFW	EMIF firewall
CFG_TA_GPMCFW	GPMC firewall
CFG_TA_OCMRAMFW	RAM firewall
CFG_TA_SGXFW	SGX firewall
CFG_TA_ISSFW	ISS firewall
CFG_TA_CORTEXM3FW	Cortex-M3 firewall
CFG_TA_DSSFW	Display subsystem (DSS) firewall
CFG_TA_SL2FW	SL2 firewall
CFG_TA_IVAHDFW	Image and video accelerator high-definition (IVA-HD) firewall
CFG_TA_EMUSSFW	EMU subsystem firewall
CFG_TA_ABEFW	Audio back-end (ABE) firewall
CFG_TA_L4WKUP	L4_WKUP connection

A unique port, CFG_IA_0, communicates between the L3 interconnect and the L4_CFG interconnect to allow the L3 initiators to access the L4_CFG targets (see Table 13-9).

For the list of initiators authorized to access the L4_CFG peripherals, see , *Connectivity Matrix*.

Table 13-9. L4_CFG IAs

Module Initiator Name	Description
CFG_IA_0	L3 interconnect port

13.1.3.2.3 L4_WKUP Interconnect Agents

The L4_WKUP interconnect handles transfers only to peripherals in the WKUP power domain. Table 13-10 lists the TAs. Table 13-11 lists the L4_WKUP IAs.

Table 13-10. L4_WKUP TAs

Module Target Name	Description
WKUP_TA_GPIO1	GPIO1 module
WKUP_TA_32KTIMER	32-kHz timer module
WKUP_TA_SAR_RAM	Save-and-restore RAM
WKUP_TA_KEYBOARD	Keyboard module
WKUP_TA_SYSCTRL_GENERAL_WKUP	System control general WKUP module
WKUP_TA_SYSCTRL_PADCONF_WKUP	System control padconf WKUP module
WKUP_TA_PRM	Power reset management module
WKUP_TA_SCRM	System clock and reset management module
WKUP_TA_WDTIMER2	WDTIMER2 module

Table 13-11. L4_WKUP IAs

Module Initiator Name	Description
WKUP_IA_0	L4_CFG interconnect port

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13.1.4 Connectivity Matrix

Figure 13-2 shows the functional paths between the L3 interconnect initiator modules and the L3 and L4 TAs. The functional paths are indicated by the use of the following:

- A cell contains a + sign when a functional path exists.
- A cell is blank when a functional path does not exists.

Figure 13-2. L3 Connectivity Matrix

	Slave NIU (SN)																		
Master NIU (MN)	L3_SN_DMM1	L3_SN_DMM2	L3_SN_C2C	L3_SN_GPMC	L3_SN_OCM_RAM	L3_SN_L4_PER0	L3_SN_L4_PER1	L3_SN_L4_PER2	L3_SN_L4_PER3	L3_SN_L4_CFG	L3_SN_EMU	L3_SN_CORTEXM3	L3_SN_ABE	L3_SN_SGX	L3_SN_ISS	L3_SN_DSS	L3_SN_SL2	L3_SN_IVAHD	L3 internal regs
L3_MN_CORTEXA9	+		+	+	+			+		+	+	+	+	+	+	+	+	+	+
L3_MN_CORTEXM3	+		+	+	+				+	+	+		+	+		+	+	+	+
L3_MN_DSP	+			+					+	+	+		+		+				
L3_MN_IVAHD	+																		
L3_MN_SGX	+																+		
L3_MN_ISS		+															+		
L3_MN_DSS		+																	
L3_MN_SDMA_RD		+	+	+	+	+				+	+	+	+		+	+	+	+	+
L3_MN_SDMA_WR		+	+	+	+		+			+	+	+	+		+	+	+	+	+
L3_MN_C2C									+	+			+						
L3_MN_HSUSBOTG		+			+								+						
L3_MN_DAP		+	+	+	+				+	+	+	+	+	+	+	+	+	+	+
L3_MN_FSUSB		+																	
L3_MN_HSUSBHOST		+											+						
L3_MN_HSI		+											+						
L3_MN_MMC1	+																		
L3_MN_MMC2	+																		

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13.2 L3 Interconnect

This section describes the L3 interconnect and its components. With the exception of register points, each component includes functions for the request and response networks.

13.2.1 L3 Interconnect Overview

The L3 interconnect links cores in a flexible topology that couples low power with high performance. Innovative physical structures and advanced protocols ensure bandwidth and latency to individual IP cores, providing dedicated connections between IP cores and logical connections over a shared interconnect.

The main features of the L3 interconnects are:

- NIUs: Master NIUs for the IAs and slave NIUs for the TAs
- A partially depleted crossbar exchange network
- A special internal slave NIU for accessing L3 interconnect configuration registers
- True little-endian platform
- Transaction errors tracking and logging registers
- All signaling support for chip-level power-management infrastructure

Figure 13-3 is an overview of the L3 interconnect and the peripherals attached to it.

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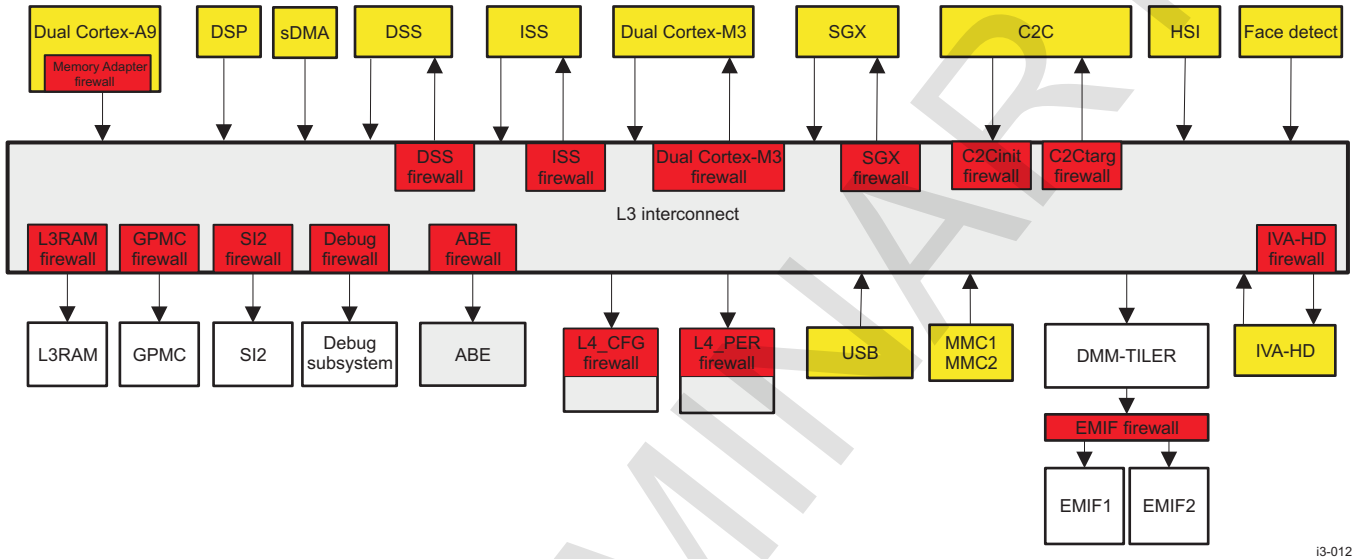
Figure 13-3. L3 Interconnect Overview



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13.2.2 L3 Interconnect Integration

Table 13-12 through Table 13-14 summarize the integration of the module in the device.

Table 13-12. Integration Attributes

Module Instance	Attributes
	Power Domain
L3	PD_CORE

Table 13-13. Clocks and Resets

Clocks				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
L3	L3_CLK2	L3_ICLK2	PRCM	Functional and interface clock
	L3_CLK1	L3_ICLK1	PRCM	Functional and interface clock
	L3_CLK3	INSTR_L3_ICLK	PRCM	Functional and interface clock
Resets				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
L3	L3_CORE_RET_RST	CORE_RET_RST	PRCM	Reset of L3_PER interconnect retention registers
	L3_CORE_RST	CORE_RST	PRCM	Reset of L3_PER interconnect

Table 13-14. Hardware Requests

Interrupt Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
L3	L3_APP_IRQ	C2C_IRQ_18	C2C INTC	Interrupt to the SSCM
	L3_DBG_IRQ	MA_IRQ_9	Cortex-A9 INTC	Interrupt to the Cortex-A9
	L3_APP_IRQ	D_IRQ_84	DSP INTC	Interrupt to the DSP
	L3_APP_IRQ	MA_IRQ_10	Cortex-A9 INTC	Interrupt to the Cortex-A9

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13.2.3 L3 Interconnect Functional Description

13.2.3.1 Module Use in L3 Interconnect

The L3 interconnect network components have ConnID values for each master NIU or slave NIU. The ID uniquely identifies the master NIU or the slave NIU for an interconnect transfer. The interconnect uses ConnIDs for a number of purposes, including the following:

- Slave NIUs for error logging
- Power disconnect slave NIU for error logging
- FLAGMUX to mask interrupts: Three, one for each clock domain
- STATCOLL for configuring and monitoring: The STATCOLL components compute the traffic statistics within a user-defined window and periodically report to the user through the debug interface.
- Bandwidth regulator for configuration: The bandwidth critical masters are IVAHD, ISS, DSS, and SGX.
- Some rate adapters for configuration of throughput ratio

13.2.3.2 Module Distribution

Master NIUs and slave NIUs provide the interface to connect the different modules to their associated interconnect.

Table 13-15 and Table 13-16 list all the modules and subsystems with their associated agents. The agents are listed for each L3 interconnect domain.

13.2.3.2.1 L3 Interconnect Agents

Any initiator or target core is connected to the L3 interconnect through an NIU. NIUs act as entry points to the L3 interconnect, and also include various programming registers. Table 13-15 lists the supported master NIU ports.

Table 13-15. Master NIUs

Master NIU	Description
L3_MN_CORTEXA9	Cortex-A9 MPU subsystem
L3_MN_DSP	DSP subsystem
L3_MN_DSS	Display subsystem
L3_MN_MMC1/2	Multimedia controller
L3_MN_IVAHD	Video accelerator subsystem
L3_MN_SGX	Graphic accelerator
L3_MN_ISS	Imaging accelerator subsystem
L3_MN_CORTEXM3	Cortex-M3 MPU subsystem
L3_MN_FACEDETECT	Face detection module
L3_MN_SDMA_rd	sDMA
L3_MN_SDMA_wr	sDMA
L3_MN_HSI	HS synchronous serial interrupt controller (INTC)
L3_MN_FSUSB	Full-speed USB host controller
L3_MN_HSUSBOTG	HS OTG USB controller
L3_MN_HSUSBHOST	Multiport USB host controller
L3_MN_C2C	C2C
L3_MN_DAP	JTAG/emulation access to system resources

Table 13-16 lists the supported slave NIU ports.

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Table 13-16. Slave NIUs

Slave NIU	Description
L3_SN_OCM_RAM	On-chip memory controller
L3_SN_GPMC	GPMC
L3_SN_C2C	C2C
L3_SN_DMM1	Dynamic memory management
L3_SN_DMM2	Dynamic memory management
L3_SN_SGX	Graphic accelerator
L3_SN_ISS	Imaging accelerator subsystem
L3_SN_IVAHD_CFG	Video accelerator subsystem configuration
L3_SN_IVAHD_SL2	Video accelerator subsystem shared memory
L3_SN_DSP	DSP subsystem
L3_SN_CORTEXM3	Cortex-M3 MPU subsystem
L3_SN_DSS	Display subsystem
L3 interconnect	L3 internal registers
L3_SN_ABE	Audio back end
L3_SN_L4_CFG	L4 interconnect configuration
L3_SN_L4_PER0/1/2/3	L4 interconnect peripherals
L3_SN_L4_EMU	L4 interconnect EMU subsystem

13.2.3.2.2 L3 Connectivity Matrix

The L3 interconnect is divided into three subclock domains:

- L3_CLK1: Low-power domain
- L3_CLK2: Peripherals and multimedia
- L3_CLK3: Instrumentation (debug)

Each is implemented in a different clock domain.

13.2.3.2.2.1 Clock Domain Mapping of the L3 Interconnect Modules

Each clock domain (CLK1, CLK2, and CLK3) has it own host, flag mux, slave NIUs, and bandwidth regulators.

Table 13-17. L3 Clock Domains and Elements

Domain	Elements
CLK1	HOST_CLK1
	DMM1/2
	ABE
	L4_CFG
	FLAGMUX
	DSS_BW
	PWR_DISK
CLK2	HOST_CLK2
	GPMC
	OCM_RAM
	DSS
	ISS
	CORTEXM3
	SGX
	IVAHD

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Table 13-17. L3 Clock Domains and Elements (continued)

Domain	Elements
	SL2
	L4_PER0/1/2/3
	FLAGMUX
	ISS_BW
	ISS_BW
	IVAHD_BW
	SGX_BW
	C2C
CLK3	HOST_CLK3
	L4_EMU
	FLAGMUX
	STATCOLL

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Figure 13-4 lists the functional paths between the L3 interconnect master NIUs and the L3 and L4 slave NIU agents. The functional paths in the figure are indicated by the following:

- A cell contains a plus sign when a functional path exists.
- A cell is blank when a functional path does not exist.

Figure 13-4. L3 Connectivity Matrix

Master NIU (MN) \ Slave NIU (SN)	L3_SN_DMM1	L3_SN_DMM2	L3_SN_C2C	L3_SN_GPMC	L3_SN_OCM_RAM	L3_SN_L4_PER0	L3_SN_L4_PER1	L3_SN_L4_PER2	L3_SN_L4_PER3	L3_SN_L4_CFG	L3_SN_EMU	L3_SN_CORTEXM3	L3_SN_ABE	L3_SN_SGX	L3_SN_ISS	L3_SN_DSS	L3_SN_SL2	L3_SN_IVAHD	L3 internal regs
L3_MN_CORTEXA9	+		+	+	+			+		+	+	+	+	+	+	+	+	+	+
L3_MN_CORTEXM3	+		+	+	+				+	+	+		+	+		+	+	+	+
L3_MN_DSP	+			+					+	+	+		+		+				
L3_MN_IVAHD	+																		
L3_MN_SGX	+																+		
L3_MN_ISS		+															+		
L3_MN_DSS		+																	
L3_MN_SDMA_RD		+	+	+	+	+				+	+	+	+		+	+	+	+	+
L3_MN_SDMA_WR		+	+	+	+		+			+	+	+	+		+	+	+	+	+
L3_MN_C2C									+	+			+						
L3_MN_HSUSBOTG		+			+								+						
L3_MN_DAP		+	+	+	+				+	+	+	+	+	+	+	+	+	+	+
L3_MN_FSUSB		+																	
L3_MN_HSUSBHOST		+											+						
L3_MN_HSI		+											+						
L3_MN_MMC1	+																		
L3_MN_MMC2	+																		

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13.2.3.2.3 Master NIU Identification

An master NIU ID (ConnID) is assigned to every module in the device. The ID uniquely identifies the master NIU for an interconnect transfer (see Table 13-18). The interconnect uses ConnID values for a number of purposes, including:

- Master source identification for the protection mechanism
- Response route generation
- Firewall error logging
- L3 interconnect error logging

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Table 13-18. ConnID Values

ConnID	Master NIU
0x0	Cortex-A9
0x1	DAP
0x2	DSP
0x3	IVAHD
0x4	ISS
0x4	Cortex-M3
0x4	FaceDetect
0x5 0x5	sDMA_rd sDMA_wr
0x6	SGX
0x7	DSS
0x8	C2C
0x9	HSI
0xA 0xA	MMC1 MMC2
0xC	HSUSBHOST
0xC	FSUSB
0xC	HSUSBOTG
0xD	Reserved
0xE	Reserved
0xF	Reserved

13.2.3.3 Bandwidth Regulators

The bandwidth regulators prevent master NIUs from consuming too much bandwidth of a link, or a slave NIU that is shared between several data flows: packets are then transported at a slower rate. The value of a bandwidth can be programmed in the bandwidth regulator. When the bandwidth is below the programmed value, the pressure bit is set to 1, giving priority to this master. When the bandwidth is above the programmed value, the pressure bit is set to 0 and the concerned master has the same weight as others.

The bandwidth registers regulate the packet flow by applying flow control on the RX port, thus ensuring that the traffic does not exceed the allocated bandwidth. The next packet is sent only when an internal timer expires. The registers in this group are:

- L3_BW_R_WATERMARK: Gives the amount of data allowed to exceed the average bandwidth during a short time period
- L3_BW_R_PRESS: Describes the pressure applied to outgoing packets
- L3_BW_R_CLEARHISTORY: Resets the traffic counter when set to 1. It is used after an update in the L3_BW_R_BANDWIDTH and L3_BW_R_WATERMARK registers (see Section 13.2.5.1.6, *L3 BW Regulator Register Summary and Description*).

13.2.3.4 Flag Mux Generators

The flag mux generator collects information such as errors and interrupts from slave NIUs and the interconnect firewall. The result signals are then sent to the MPU INTC without interfering with the interconnect traffic. The L3_FLAGMUX_MASK registers can be used to prevent the flag mux from seeing certain events.

The unit has a standard COREREG register for identification of the attached core type. The L3_FLAGMUX_STDHOSTHDR_VERSIONREG register identifies the characteristics of the attached core.

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The unit-specific registers (MASK bit 0 or bit 1 of the flag inputs, and L3_FLAGMUX_REGERR bit 0 or bit 1) are used to read the input errors. Each register is dedicated to reporting the bit corresponding to the register number; for example, L3_FLAGMUX_REGERR0 reports on bit 0, and L3_FLAGMUX_REGERR1 reports on bit 1. Any given L3_FLAGMUX_REGERR register reports the same bit for all flag source inputs (see Table 13-162).

13.2.3.5 Rate Adapter Generators

The rate adapter generators give the option to configure the L3 interconnect to work in auto-adaptive mode or pipeline mode for sending the packets by using the CNF register. The rate adapter can be configured in store-and-forward mode when the throughput ratio is not well defined, or in auto-adaptive mode when the throughput ratio is predictable. Because the ratios are predictable in the L3 interconnect, the rate adapters are always used in auto-adaptive mode, except for the rate adapter on the L4_CFG and L4_ ABE responses path. L4_CFG and L4_ABE are configured in store-and-forward mode. The main rate adapt registers are:

- CLK1_RATE_ADAPT_RESP_32TO128_CLK1: Removes WAIT cycles on responses coming from ABE, L4CFG, and power disconnect to host
- CLK2_RATE_ADAPT_RESP_32TO128_CLK2: Removes WAIT cycles on responses coming from CLK2 32-bit slaves (see Table 13-192)

13.2.3.6 Statistic Collectors Group

Statistic collectors are internal masters that share the same master address as the master NIUs. These components compute the traffic statistics within a defined window and periodically report through the DEBUG interface. The key features of the statistic collector are:

- Nonintrusive monitoring
- Programmable filters and counters
- Results collected at a programmable time interval

Event detectors are programmed through the L3_STCOL_REQEVT and L3_STCOL_RSPEVT configuration registers for request and response ports, respectively. The following events can be identified:

- Word transfer
- WAIT cycles
- Flow control
- Payload transfers
- Latency measurements

Performance monitoring is enabled through the L3_STCOL_EN register. The L3_STCOL_SOFTEN register enables software to monitor the performance. Event muxes are programmed through the L3_STCOL_EVTMUX_SEL0 configuration register, which determines which port will be monitored by a filter configured by the filter registers (see).

Filters are programmed through the configuration register, along with additional selection criteria programmed through the mask/match registers (see Table 13-201). A filter can be configured to accept or reject:

- Read operations
- Write operations
- Errors
- Addresses

Filter operations are programmed through the L3_STCOL_OP registers (see Table 13-201).

13.2.3.7 L3 Protection and Firewalls

Device protection relies on L3 firewalls and their configuration.

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13.2.3.7.1 L3 Firewall Reset

The values of L3 firewall registers on reset are tied in hardware or exported from the control module registers.

Values exported from the control module are intended to give defined rights to the firewalls at reset and thus ensure the content after going out of reset. Because the control module consists of retention flip-flops (RFFs), which immunize it against register content loss during retention power state, the registers of the control module storing the exported values are not subject to a soft reset.

The L3 firewall registers are also retention-capable and are immune against content loss during CORE RETENTION power state. The control module registers are reset only by a cold reset, whereas the L3 firewall registers are reset by clearing the REGUPDATE_CONTROL[1] FW_LOAD_REQ bit. When the REGUPDATE_CONTROL[1] FW_LOAD_REQ bit comes back automatically to 1, the exported values are loaded.

CAUTION

Before reprogramming the firewall registers and/or before using the FW_LOAD_REQ mechanism, the request must be asserted by configuring the REGUPDATE_CONTROL[0] BUSY_REQ bit.

To load the exported values at run time:

1. Set the REGUPDATE_CONTROL[0] BUSY_REQ bit to 0x1 to ensure that no transaction can reach the slave NIU (suspend).
2. Clear the REGUPDATE_CONTROL[1] FW_LOAD_REQ bit by writing 0x1 to it.
3. Wait until the REGUPDATE_CONTROL[1] FW_LOAD_REQ bit is reset to 0x1 by hardware.
4. Set the REGUPDATE_CONTROL[0] BUSY_REQ bit to 0x0 to allow transactions to reach the slave NIU (resume).

To reprogram the firewall registers at run time:

1. Set the REGUPDATE_CONTROL[0] BUSY_REQ bit to 0x1 to ensure that no transaction can reach the slave NIU (suspend).
2. Upload the new values to all firewall registers.
3. Set the REGUPDATE_CONTROL[0] BUSY_REQ bit to 0x0 to allow transactions to reach the slave NIU (resume).

NOTE: Hardware reset values can be modified by exported values from the control module at reset.

13.2.3.7.1.1 L3 Firewall – Exported Reset Values

Table 13-19 and Table 13-20 list the exported reset values and mapping, respectively.

Table 13-19. L3 Firewall Exported Reset Values

MRM_PERMISSION_REGION_LOW_j [15:12]	MRM_PERMISSION_REGION_LOW_j [11:0]
0x0	0xFFF
0xF	0xFFF
0x0	0x038
0x2	0x038

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Table 13-20. L3 Firewall Exported Values Mapping

CONTROL_CORE_L3_HW_FW_EXPORTED_VALUES_CONF Bits	Slave NIU Firewall
[0] and [16]	GPMC
[1] and [17]	C2CINIT
[2] and [18]	C2CTARG
[3] and [19]	L3 RAM
[4] and [20]	DSS
[5] and [21]	ISS and dual Cortex-M3 subsystem
[6] and [22]	SGX
[7] and [23]	SL2
[8] and [24]	IVA-HD
[11] and [27]	EMIF
[12] and [28]	DEBUG
[13] and [29]	L4 AUDIO

For more information, see Chapter 18, *Control Module*.

13.2.3.7.2 Power Management

As part of the system-wide power-management scheme, the L3 interconnect goes into IDLE state after receiving a request from the power, reset, and clock management (PRCM) module after all commands are serviced. This function is handled by hardware.

To reduce power consumption, the L3 interconnect automatically performs internal clock autogating. This is managed by hardware; no software configurations or settings are required.

Retention is performed on all software-accessible registers:

- Statistic collectors
- Internal rate adapters
- Bandwidth regulators
- TAs
- Firewalls

This process prevents reconfiguration after a clock domain switches off.

13.2.3.7.3 L3 Firewall Functionality

The access to the slave NIUs is granted only to master NIUs according to in-band attributes sent in each transaction crossing the L3 interconnect, such as:

- MCMD: Specifies the type of access (read or write) required by the master NIU
- ConnID: Used to determine the permission of the master NIU
- MReqInfo: Transaction attribute adding information about the access type

Table 13-21 lists the MReqInfo Values.

Table 13-21. MReqInfo Values

Qualifier	Access Definition	Access Description
MReqType	0: Data 1: Opcode	Indicates whether the request is for instruction fetch or data access
MReqDebug	0: Functional 1: Debug	When set, indicates that the request has been issued by a master NIU in DEBUG state
MReqSupervisor	0: User 1: Privilege	When set, indicates that the request is qualified with the supervisor attribute. It can be provided by a processor running in supervisor mode or by a module that inherited this attribute from the processor (DMA channel with a supervisor attribute).

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The firewall comparison mechanism enables access to a protected slave NIU only when a correct combination of three MReqInfo in-band parameters is transmitted.

MReqInfo is a combination of a fixed 3-bit pattern that corresponds to a combination of the parameters MReqDebug, MReqType, and MReqSupervisor. See Table 13-22.

Table 13-22. L3 ReqInfo Mapping

ReqInfo Name		MReqDebug	MReqType	MReqSupervisor
Master NIUs	L3_MN_CORTEXA9	x	x	x
	L3_MN_CORTEXM3	x	x	x
	L3_MN_DSP	x	x	
	L3_MN_IVAHD			
	L3_MN_SGX			
	L3_MN_DSS			
	L3_MN_ISS			
	L3_MN_C2C	x	x	x
	L3_MN_DAP	x		x
	L3_MN_SDMA_RD		x	x
	L3_MN_SDMA_WR		x	x
	L3_MN_HSUSBOTG			
	L3_MN_HSUSBHOST			
	L3_MN_FSUSB			
	L3_MN_HSI			x
	L3_MN_FACEDETECT			
	L3_MN_MMC1/2			
Slave NIUs	L3_SN_DMM1	x	x	x
	L3_SN_DMM2	x	x	x
	L3_SN_GPMC			
	L3_SN_OCM_RAM			
	L3_SN_L4_PER0/1/2/3	x		x
	L3_SN_L4_CFG	x		x
	L3_SN_L4_ABE	x		
	L3_SN_CORTEXM3			
	L3_SN_SGX			
	L3_SN_DAP	x		
	L3_SN_ISS			
	L3_SN_DSS			x
	L3_SN_IVAHD	x		
	L3_SN_SL2			
	L3_SN_C2C	x	x	x

13.2.3.7.3.1 Protection Regions

Each slave NIU address space is subdivided into protection regions (maximum of 10). The regions are configurable with a size of 4-KB granularity. The firewalls can also be multiport while using the description of the same regions for dual access memories or to support interleaving mechanisms on several memories.

Table 13-23 lists the number of protected regions and ports for each slave NIU.

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Table 13-23. Slave NIU Firewall and Region Configuration

Slave NIU	Firewall	Number of Regions	Number of Ports
L3 RAM	L3 RAM	10	1
GPMC	GPMC	8	1
SL2	SL2	1	1
SGX	SGX	1	1
C2C	C2CTARG	1	1
L3 interconnect	C2CINIT	4	2
ISS	ISS	1	1
Dual Cortex-M3 subsystem	Dual Cortex-M3	1	1
DSS	DSS	1	1
IVA-HD	IVA-HD	1	1
DEBUG subsystem	DEBUG	2	1
ABE	ABE	1	1
EMIF	EMIF	8	3

Two types of regions are distinguished in a slave NIU firewall:

- Default region: Available in all slave NIUs. It covers the entire slave NIU address range and must be reset or overlaid by other firewall configured regions, because it always has the lowest priority.
- Normal region: The number of normal regions varies in a slave NIU; they have identical capabilities (see Table 13-23).

Each region has the following characteristics:

- Start address: Physical slave NIU start address
- End address: Physical slave NIU end address
- Specific access rights (see Section 13.2.3.7.3.3, *Protection Mechanism per Region Examples*)
- Priority level from 0 (lowest) to 10 (highest)

Depending on its priority level, a region can override the settings of another region; the access rights of the region with the highest priority apply. All regions have a fixed (not configurable) priority level that corresponds to their number: Region 1 has priority level 1, region 2 has priority level 2, and so on.

Figure 13-5 shows the priority level with associated regions. This priority level scheme allows multiplying the flexibility and capability of the firewall. Figure 13-5 shows a 7-region firewall setting that creates 13 regions (twice the number of regions created than originally available).

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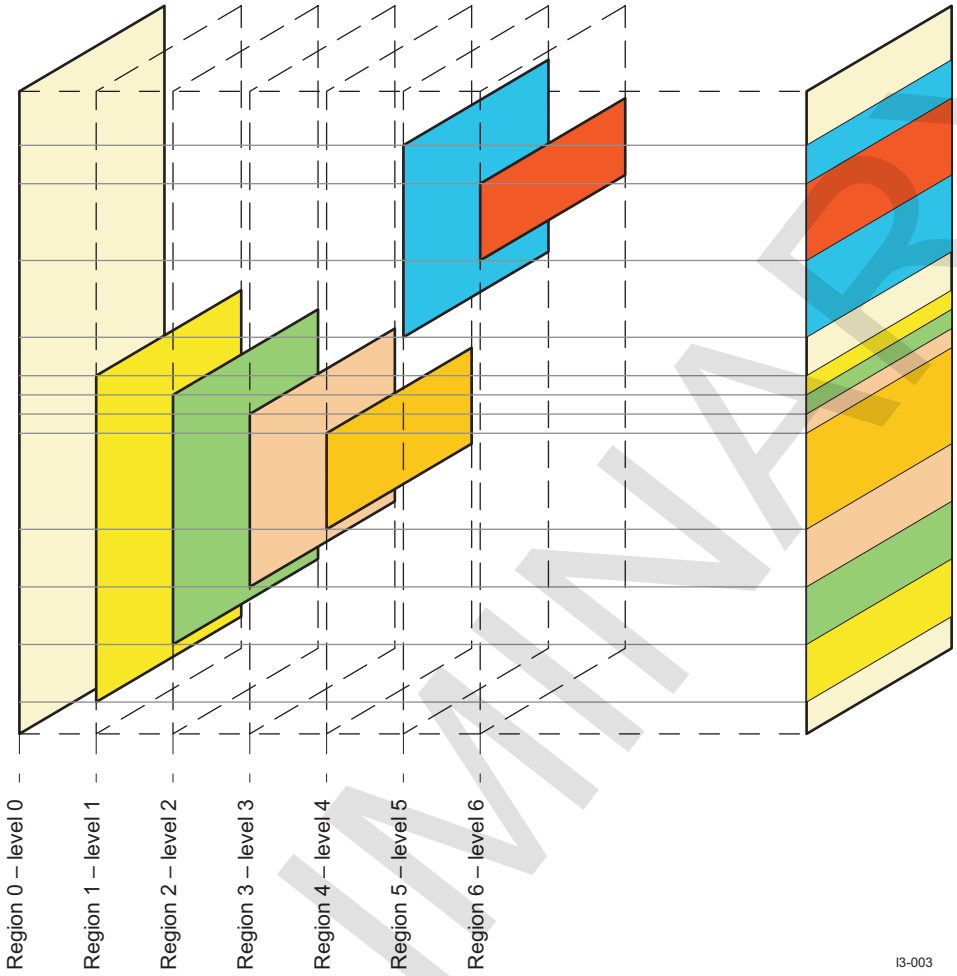
Figure 13-5. L3 Interconnect Region Overlay and Priority Level Overview



The address range covered by the regions is defined in the START_REGION_i and END_REGION_i registers. The boundary checks are done on a minimum size of 4-KB pages; thus, bits [11:0] of those 32-bit registers are not checked.

The address space size of the slave NIUs ([bits [31:12]) depends on the size of the slave NIU to protect (that is, if a memory is only 48KB, then the size is defined through bits [16:12] of the slave NIU start/end address registers of the firewall region (START_REGION_i[16:12] and END_REGION_i[16:12]).

NOTE: The EMIF firewall sees only the 4GB that require protection.

Bit [31] is replaced by bit [32] of the EMIF address space seen by firewalls to have 2GB of LPDDR2-SDRAM and 2GB of LPDDR2-NVM contiguous.

For more information, see Section 15.3, *EMIF Controller*.

On multiport firewalls (EMIF), the checking of each REGION {0, n} can be activated on one or several ports at the same time. However, if interleaving is not desired on some parts of the protected memory space, it is possible to apply or not apply region checking on selected ports using the region enable/disable on port instance capability of the END_REGION_i register.

Most slave NIUs support only one input port (port 0) except:

- The EMIF module protected by the EMIF firewall has three ports:
  - Port 0 for Cortex-A9 accesses
  - Port 1 for the first L3 interconnect accesses

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– Port 2 for the second L3 interconnect accesses

A region can be applied or not to each port independently. To enable and disable the regions:

- For port 0: Set/clear the END_REGION_i[0] REGION_ENABLE_PORT0 bit (for all L3 firewalls).
- For port 1: Set/clear the END_REGION_i[1] REGION_ENABLE_PORT1 bit (only for Crypto and EMIF firewalls).
- For port 2: Set/clear the END_REGION_i[2] REGION_ENABLE_PORT2 bit (only for EMIF firewalls).

13.2.3.7.3.2 L3 Firewall Registers Overview

Table 13-24 and Table 13-25 list the L3 firewall permission-setting registers.

Table 13-24. L3 Firewall Read/Write Permission-Setting Register

Register Name	Bits	Field Name	Description (see Table 13-18)	Field Modifiability
MRM_PERMISSION_REGION_HIGH_j	31	RESERVED	Reserved	–
	30	RESERVED	Reserved	–
	29	RESERVED	Reserved	–
	28	RESERVED	Reserved	–
	27	RESERVED	Reserved	–
	26	RESERVED	Reserved	–
	25	W12	ConnID = 12 write permission	RW
	24	R12	ConnID = 12 read permission	RW
	23	RESERVED	Reserved	–
	22	RESERVED	Reserved	–
	21	W10	ConnID = 10 write permission	RW
	20	R10	ConnID = 10 read permission	RW
	19	W9	ConnID = 9 write permission	RW
	18	R9	ConnID = 9 read permission	RW
	17	W8	ConnID = 8 write permission	RW
	16	R8	ConnID = 8 read permission	RW
	15	W7	ConnID = 7 write permission	RW
	14	R7	ConnID = 7 read permission	RW
	13	W6	ConnID = 6 write permission	RW
	12	R6	ConnID = 6 read permission	RW
	11	W5	ConnID = 5 write permission	RW
	10	R5	ConnID = 5 read permission	RW
	9	W4	ConnID = 4 write permission	RW
	8	R4	ConnID = 4 read permission	RW
	7	W3	ConnID = 3 write permission	RW
	6	R3	ConnID = 3 read permission	RW
	5	W2	ConnID = 2 write permission	RW
	4	R2	ConnID = 2 read permission	RW
	3	W1	ConnID = 1 write permission	RW
	2	R1	ConnID = 1 read permission	RW
	1	W0	ConnID = 0 write permission	RW
	0	R0	ConnID = 0 read permission	RW

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Table 13-25. L3 Firewall Permission-Setting Register

Register name	Type of Permission	Bits	Field Name	Description	Field Modifiability
MRM_PERMISSION_REGION_LOW_j	DEBUG	15	PUB_PRV_DEBUG	Privilege debug allowed	RW
		14	PUB_USR_DEBUG	User debug allowed	RW
	Access	13:12	Reserved	Reserved	RW
		11	PUB_PRV_WRITE	Privilege write allowed	RW
		10	PUB_PRV_READ	Privilege read allowed	RW
		9	PUB_PRV_EXE	Privilege exe allowed	RW
		8	PUB_USR_WRITE	User write access allowed	RW
		7	PUB_USR_READ	User read access allowed	RW
		6	PUB_USR_EXE	User exe access allowed	RW

13.2.3.7.3.3 Protection Mechanism per Region Examples

The access permission of each region is configurable and defined through the MRM_PERMISSION_REGION_HIGH_j and MRM_PERMISSION_REGION_LOW_j registers (see Section 13.2.3.7.3.2, *L3 Firewall Registers Overview*).

Master NIU permissions:

1. To give read access to the master NIU with ConnID = n, set the MRM_PERMISSION_REGION_HIGH_j[n * 2] Rn bit.
2. To give write access to the master NIU with ConnID = n, set the MRM_PERMISSION_REGION_HIGH_j[n * 2 + 1] Wn bit.

Debug permissions:

1. To give privilege debug access, set the MRM_PERMISSION_REGION_LOW_j[15] PUB_PRV_DEBUG bit.
2. To give user debug access, set the MRM_PERMISSION_REGION_LOW_j[14] PUB_USR_DEBUG bit.

User, read/write/executable permissions:

1. To give privilege write access, set the MRM_PERMISSION_REGION_LOW_j[11] PUB_PRV_WRITE bit.
2. To give privilege read access, set the MRM_PERMISSION_REGION_LOW_j[10] PUB_PRV_READ bit.
3. To give privilege exe access, set the MRM_PERMISSION_REGION_LOW_j[9] PUB_PRV_EXE bit.
4. To give user write access, set the MRM_PERMISSION_REGION_LOW_j[8] PUB_USR_WRITE bit.
5. To give user read access, set the MRM_PERMISSION_REGION_LOW_j[7] PUB_USR_READ bit.
6. To give user exe access, set the MRM_PERMISSION_REGION_LOW_j[6] PUB_USR_EXE bit.

Example: To provide debug write privilege access to the master NIU ConnID = 7, the following bits must be set:

- MRM_PERMISSION_REGION_HIGH_j[15] W7
- MRM_PERMISSION_REGION_LOW_j[15] PUB_PRV_DEBUG

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13.2.3.7.3.4 L3 Firewall Error Logging

If a protection violation error is detected, the following signals are generated:

- An in-band error is generated to the master NIU of the access.
- An interrupt is generated to the Cortex-A9 and DSP INTCs.

The L3 interconnect does not differentiate errors generated by firewalls from all other supported types of errors.

An in-band error is generated by modules each time an access is not allowed. When an in-band error is sent back into the transaction it is seen as an external prefetch or data abort by the initiator, depending on whether the transaction was an instruction fetch or a data access.

Information about in-band errors is logged into two registers:

- ERROR_LOG_k: Logs the information about the start/end address of the hit region and the qualifiers of the transaction
- LOGICAL_ADDR_ERRLOG_k[31:12]: Logs the address of the failed access

NOTE: When a multiport firewall is implemented, these registers are duplicated for each port.

Table 13-26 lists the L3 firewall error-logging registers.

Table 13-26. L3 Firewall Error-Logging Registers

Register Name	Register Field Name	Field Modifiability	Parameter Comments
ERROR_LOG_k	RESERVED[31:24]	Read only	Reads return 0s.
	BLK_BURST_VIOLATION[23]	Read/write	Read 0x1: 2D burst not allowed or exceeds allowed size. Write to clear the ERROR_LOG_k and LOGICAL_ADDR_ERRLOG_k registers.
	RESERVED[22]	Read only	Reads return 0s.
	REGION_START_ERRLOG[21:17]	Read/write	Read: Wrong access hit this region number. Write to clear the ERROR_LOG_k and LOGICAL_ADDR_ERRLOG_k registers.
	REGION_END_ERRLOG[16:12]	Read/write	Read: Wrong access hit this region number. Write to clear the ERROR_LOG_k and LOGICAL_ADDR_ERRLOG_k registers.
	REQINFO_ERRLOG[11:0]	Read/write	Mapping of the error according to the reqinfo vector: [11:8] ConnID [3:0] [7] MCMD [0] [3] MReqDebug [1] MReqSupervisor [0] MReqType

L3 firewall errors can be cleared by writing to the ERROR_LOG_k register in the firewall that recorded the error. Clearing the ERROR_LOG_k register deasserts the corresponding error if it exists.

The L3 firewall register ERROR_LOG_k must be cleared before clearing the CONTROL_CORE_SEC_ERR_STATUS_FUNC and CONTROL_CORE_SEC_ERR_STATUS_DEBUG registers in the control module.

When a protection violation occurs, an interrupt is sent to the MPU and IVAHD INTC (if enabled). An in-band error is sent back, and an error is logged in the CONTROL_SEC_ERR_STATUS_FUNC and CONTROL_SEC_ERR_STATUS_DEBUG registers, depending on the functional mode:

- In application mode:
  - CONTROL_SEC_ERR_STATUS_FUNC[01] – L3 RAM protection violation
  - CONTROL_SEC_ERR_STATUS_FUNC[02] – GPMC protection violation
  - CONTROL_SEC_ERR_STATUS_FUNC[03] – EMIF protection violation
  - CONTROL_SEC_ERR_STATUS_FUNC[04] – IVAHD protection violation

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  - CONTROL_SEC_ERR_STATUS_FUNC[05] – Cortex-M3 protection violation
  - CONTROL_SEC_ERR_STATUS_FUNC[06] – SL2 protection violation
  - CONTROL_SEC_ERR_STATUS_FUNC[12] – C2C slave NIU protection violation
  - CONTROL_SEC_ERR_STATUS_FUNC[13] – SGX protection violation
  - CONTROL_SEC_ERR_STATUS_FUNC[14] – DSS protection violation
  - CONTROL_SEC_ERR_STATUS_FUNC[15] – ISS protection violation
  - CONTROL_SEC_ERR_STATUS_FUNC[18] – DEBUG protection violation
  - CONTROL_SEC_ERR_STATUS_FUNC[19] – ABE protection violation
  - CONTROL_SEC_ERR_STATUS_FUNC[20] – C2C init protection violation
- In debug mode:
  - CONTROL_SEC_ERR_STATUS_DEBUG[01] – L3 RAM protection violation
  - CONTROL_SEC_ERR_STATUS_DEBUG[02] – GPMC protection violation
  - CONTROL_SEC_ERR_STATUS_DEBUG[03] – EMIF protection violation
  - CONTROL_SEC_ERR_STATUS_DEBUG[04] – IVAHD protection violation
  - CONTROL_SEC_ERR_STATUS_DEBUG[05] – Cortex-M3 protection violation
  - CONTROL_SEC_ERR_STATUS_DEBUG[06] – SL2 protection violation
  - CONTROL_SEC_ERR_STATUS_DEBUG[12] – C2C slave NIU protection violation
  - CONTROL_SEC_ERR_STATUS_DEBUG[13] – SGX protection violation
  - CONTROL_SEC_ERR_STATUS_DEBUG[14] – DSS protection violation
  - CONTROL_SEC_ERR_STATUS_DEBUG[15] – ISS protection violation
  - CONTROL_SEC_ERR_STATUS_DEBUG[18] – DEBUG protection violation
  - CONTROL_SEC_ERR_STATUS_DEBUG[19] – ABE protection violation
  - CONTROL_SEC_ERR_STATUS_DEBUG[20] – C2C init protection violation

For more information, see Chapter 18, *Control Module*.

13.2.3.7.3.5 L3 Firewall Default Configuration

Table 13-27 summarizes the configuration of the L3 firewalls.

Table 13-27. L3 Firewalls Default Configurations

Device/Region: 0						
Permission Type	**Reset Value**	**Reset Value**	**Reset Type**	**Run Time**	**Firewall Register (where j = 0)**	**Control Module Register**
ACCESS_ PERMISSION	All	0xFFF	Exported	Configurable	MRM_PERMISSION_REGION_LOW_j[11:0]	CONTROL_CORE_L3_HW_FW_ EXPORTED_VALUES_CONF[k]
DEBUG_ PERMISSION	All	0xF	Exported	Configurable	MRM_PERMISSION_REGION_LOW_j[15:12]	CONTROL_CORE_L3_HW_FW_ EXPORTED_VALUES_CONF[l] CONTROL_CORE_L3_HW_FW_ EXPORTED_VALUES_CONF[k]
INITIATOR_ PERMISSION	All	0xFFF FFFFF	Tied	Configurable	MRM_PERMISSION_REGION_HIGH_j[31:0]	N/A

NOTE: For the values of k and l, see Table 13-28.

Table 13-28. Control Module Register – Factorization

Variable Value		Module Name	Regions
k	**l**		
3	19	L3 RAM firewall	Regions 1 to 9
0	16	GPMC firewall	Regions 1 to 7

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Table 13-28. Control Module Register – Factorization (continued)

Variable Value		Module Name	Regions
7	23	SL2 firewall	Regions 1 to 7
6	22	SGX firewall	Regions 1 to 7
5	21	ISS firewall	Regions 1 to 7
5	21	Cortex-M3 firewall	Regions 1 to 7
4	20	DSS firewall	Regions 1 to 7
8	24	IVAHD firewall	Regions 1 to 7
12	28	DEBUG firewall	Region 1
13	29	ABE firewall	Region 1
1	17	C2C slave NIU firewall	Region 1
9	25	C2C init firewall	Regions 1 to 3
11	27	EMIF firewall	Regions 1 to 7

13.2.3.8 L3 Interconnect Error Handling

Error logging is enabled in the L3 interconnect. The three major types of errors are:

- Slave NIU errors
- Firewall errors (see Section 13.2.3.7.3.4, *L3 Firewall Error Logging*)
- Flag mux errors

13.2.3.8.1 Global Error-Routing Scheme

Figure 13-6 shows the L3 global error-routing scheme.

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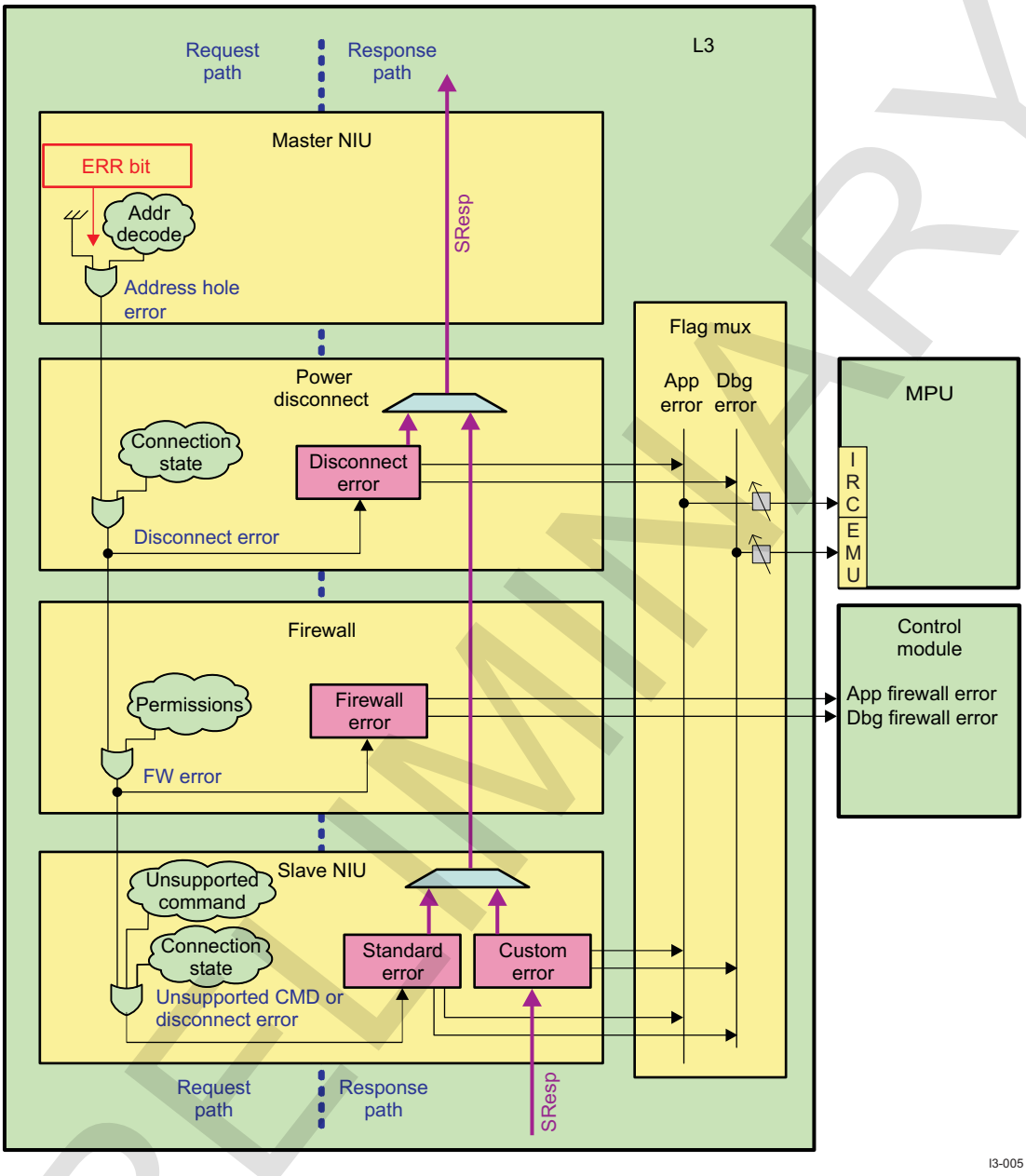
Figure 13-6. L3 Global Error-Routing Scheme



13.2.3.8.2 Slave NIU Error Logging

Error logging is implemented only at slave NIUs. Because the interconnect does not support master NIU error logging, an erroneous packet must be created and sent to one of the slave NIUs. The slave NIU that receives an erroneous packet is predictable but can change per master (see Table 13-29).

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Table 13-29. L3 Connectivity and Holes Error Routing

Master	Connectivity and Hole Errors Logged Into Slave NIUs
L3_MN_DAP	L3_SN_GPMC
L3_MN_CORTEXM3	
L3_MN_CORTEXA9	
L3_MN_SDMA_RD	
L3_MN_SDMA_WR	
L3_MN_DSP	
L3_MN_IVANHD	L3_SN_DMM1
L3_MN_MMC1	
L3_MN_MMC2	
L3_MN_SGX	
L3_MN_DSS	L3_SN_DMM2
L3_MN_ISS	
L3_MN_FACEDETECT	
L3_MN_FSUSB	
L3_MN_HSUSBOTG	L3_SN_OCM_RAM
L3_MN_HSI	L3_SN_ABE
L3_MN_HSUSBHOST	
L3_MN_C2C	L3_SN_L4_PER3

The slave NIU can be configured to report standard errors (errors generated within the interconnect):

- Firewall error: Protection violation; this error indicates that a request was rejected by a firewall and is reported to the control module. For more information, see Section 13.2.3.7.3.4, *L3 Firewall Error Logging.*
- Address hole: This error reports an unknown address for a request. The address map is local to each master NIU; therefore, an address hole error is reported each time a master NIU requests an access to a slave NIU to which it is not logically connected, even if this address exists in the global L3 address map. This error is detected only once per burst.
- Unsupported commands: This error reports that the master NIU sent a command that cannot be processed, because the slave NIU cannot accept it and no conversion to another command is possible. This error is detected only once per burst.
- Report custom errors: Basically, when the slave answer is SResp = ERR
- Report severity level, for standard error and custom errors:
  - None: Error logging for this type of error is disabled.
  - Error: Error is logged for this type of error.
  - Fault: Error is logged and interrupt is generated for this type of error.
- Generate interrupt on 2 bits depending on the MReqDebug qualifier:
  - Application error - Fault[0]
  - Debug error - Fault[1]

  By default, all slave NIUs are configured with standard and custom error levels set to FAULT. The errors are reported on the two flag muxes (see Figure 13-6), depending on the access type, application or debug. For more information, see Section 13.2.3.8.3, *Flag Mux Error Logging*.

  The slave NIU power-disconnect component also has error logging enabled. This is because the slave NIU in this case is in a clock domain that is switched off and therefore cannot catch the error. By nature, this component can generate only standard errors. By default, it is configured with the error level set to FAULT.

  Wake up on demand: If an error packet reaches a slave NIU that is set with MDiscBehave = 1 (wake up on demand), then the active signal is asserted and L3 processes the error generation when the slave is awake. This is inefficient but it simplifies NIU implementation and should not be a problem, because errors are supposed to occur only during software debug.

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13.2.3.8.3 Flag Mux Error Logging

All fault signals are sent to a flag mux component. There are four important FLAGMUX registers:

- L3_FLAGMUX_MASK0: Masks application error sources
- L3_FLAGMUX_MASK1: Masks debug error sources
- L3_FLAGMUX_REGERR0: Checks which application error sources are active
- L3_FLAGMUX_REGERR1: Checks which debug error sources are active

The two L3_FLAGMUXMASK registers mask bit 0 or bit 1 of the flag inputs, and the L3_FLAGMUX_REGERR registers read input errors. Each register is dedicated to reporting the bit corresponding to the register number.

Table 13-30 describes the mapping of the flags to the corresponding sources.

Table 13-30. Interconnect Flag Mapping

	Flag Mux Input	Source
CLK1 flag mux	0	L3_SN_DMM1
	1	L3_SN_DMM2
	2	L3_SN_ABE
	3	L3_SN_L4CFG
	4	CLK2 PWR DISC
CLK2 flag mux	0	L3_SN_Cortex-M3
	1	L3_SN_DSS
	2	L3_SN_GPMC
	3	L3_SN_ISS
	4	L3_SN_IVAHD
	5	Reserved
	6	L3_SN_L4PER0
	7	L3_SN_OCMCRAM
	8	L3_SN_GPMC
	9	L3_SN_SGX
	10	L3_SN_SL2
	11	L3_SN_C2C
	12	CLK1 PWR DISC
	13	Reserved
	14	Reserved
	15	L3_SN_L4PER3
	16	L3_SN_L4PER1
	17	L3_SN_L4PER2
CLK3 flag mux	0	DEBUGSS

13.2.3.8.4 Severity Level of Standard and Custom Errors

The slave NIU registers are important for error logging.

- The L3_TARG_STDERRLOG_SVRTSTDLVL register shows the severity level for standard errors. According to the severity level, error logging is disabled, enabled with level ERROR, or enabled with level ERROR and flag FAULT.
- The L3_TARG_STDERRLOG_SVRTCUSTOMLVL register shows the severity level for custom errors (see).
- The L3_TARG_STDERRLOG_MAIN register is the main register for error-logging management. It shows the validity of the logged information, standard or custom.
- The L3_TARG_STDERRLOG_HDR register stores packets in case of a standard error.

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- The L3_TARG_STDERRLOG_MSTADDR register returns the MSTADDR field of the logged packet.
- The L3_TARG_STDERRLOG_SLVADDR register returns the SLVADDR field of the stored packet.
- The L3_TARG_STDERRLOG_INFO register saves the information field of the logged packet.

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13.2.4 L3 Interconnect Programming Guide

13.2.4.1 L3 Interconnect Low-Level Programming Models

This section describes the low-level hardware programming sequences for configuring and using the L3 interconnect module.

13.2.4.1.1 Global Initialization

13.2.4.1.1.1 Global Initialization of Surrounding Modules

This section identifies the requirements for initializing the surrounding modules when the L3 interconnect module is to be used for the first time after a device reset. The initialization of surrounding modules is based on the integration and environment of the L3 interconnect. For more information, see Section 13.2.2, *L3 Interconnect Integration* .

Table 13-31. Global Initialization of Surrounding Modules

Surrounding Modules	Comments
PRCM	For information about the configuration of the PRCM module, see Chapter 3, *Power, Reset, and Clock Management*.
Control module	For information about the configuration of the control module, see Chapter 18 , *Control Module*.
MPU INTC	The MPU INTC must be configured to enable interrupts from the L3 interconnect module. See Chapter 17, *Interrupt Controllers*.
sDMA	For information about the configuration of the sDMA, see Chapter 16, *sDMA*.
L3 interconnect	For information about the configuration of the interconnect, see , *Interconnect*.

13.2.4.2 Operational Modes Configuration

13.2.4.2.1 L3 Interconnect Error Analysis Mode

13.2.4.2.1.1 Main Sequence: L3 Interconnect Error Analysis Mode

The information required to analyze an error source is logged in several registers. The number of registers to access depends on the error source.

Figure 13-7 shows the software sequence required in most cases.

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Figure 13-7. Typical Error Analysis Sequence

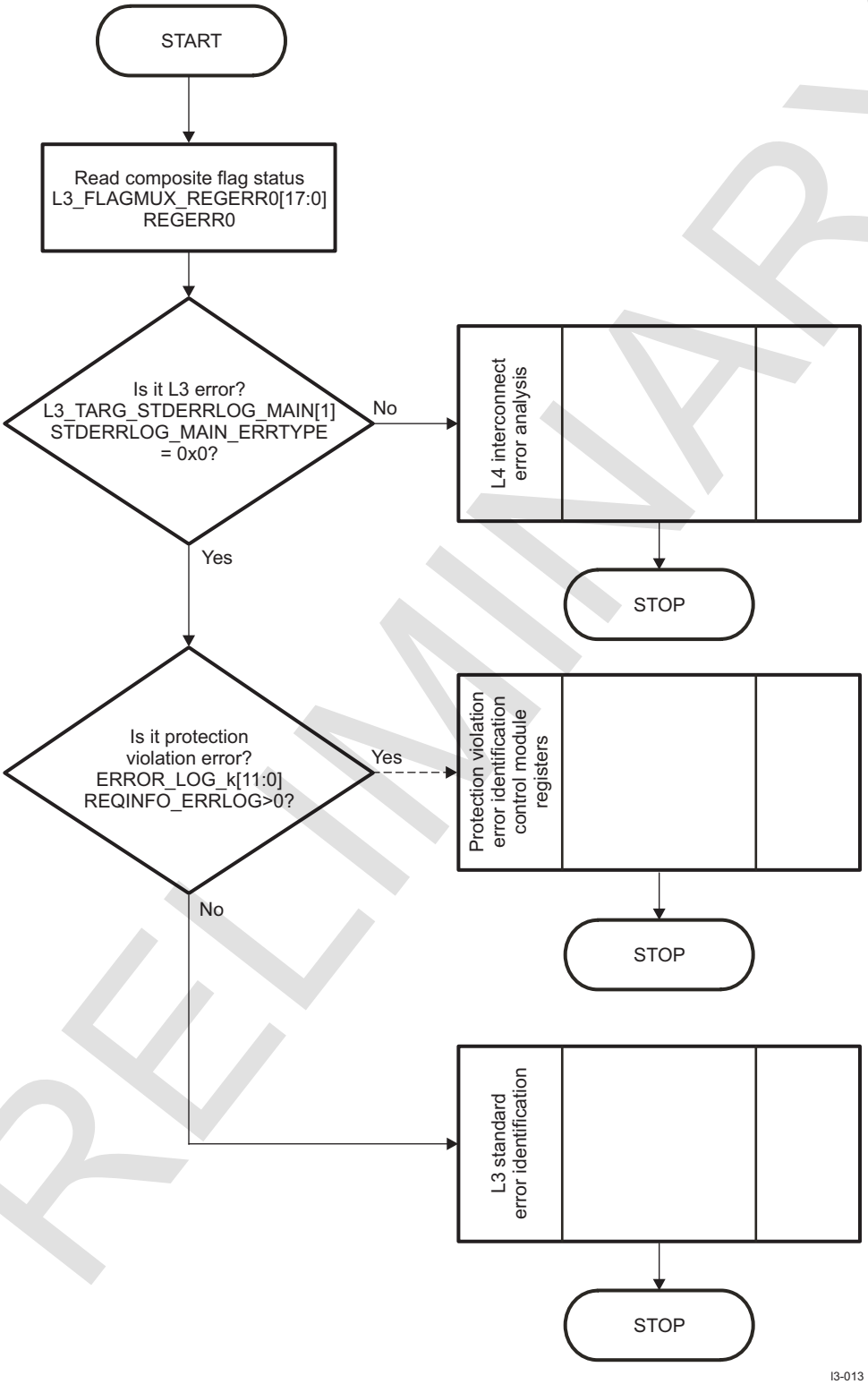

Table 13-32 lists the register call summary for error analysis mode in the main sequence.

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Table 13-32. Register Call Summary: Main Sequence – Error Analysis Mode

Register Name	Register Name	Register Name
ERROR_LOG_k	L3_FLAGMUX_REGERR0	L3_FLAGMUX_REGERR1
L3_TARG_STDERRLOG_MAIN	CONTROL.CONTROL_SEC_ERR_STATUS_FUNC	CONTROL.CONTROL_SEC_ERR_STATUS_DEBUG

Table 13-33 lists the subprocess call summary for error analysis mode in the main sequence.

Table 13-33. Subprocess Call Summary for Main Sequence – Error Analysis Mode

Subprocess	Cross-Reference
L4 interconnect error analysis	See Section 13.2.4.2.1, *L4 Interconnect Error Analysis Mode.*
L3 interconnect protection violation error identification	See Section 13.2.4.2.1.1.1, *Subsequence: L3 Interconnect Protection Violation Error Identification.*
L3 interconnect unsupported command/address hole error identification	See Section 13.2.4.2.1.1.2, *Subsequence: L3 Interconnect Unsupported Command/Address Hole Error Identification.*
L3 interconnect reset FLAGMUX and module	See Section 13.2.4.2.1.1.3, *Subsequence: L3 Interconnect Reset FLAGMUX and Module.*

13.2.4.2.1.1.1 Subsequence: L3 Interconnect Protection Violation Error Identification

The procedure listed in Table 13-34 describes protection violation error identification and where it is logged in the control module registers. Two types of errors are logged: application errors and debug errors.

Table 13-34. Protection Violation Error Identification

Step	Register/Bit Field/Programming Model	Value
Read the burst violation.	ERROR_LOG_k[23] BLK_BURST_VIOLATION	xxx
Read the initiator ID.	ERROR_LOG_k[11:8] CONNID	xxx
Read the command that caused the error.	ERROR_LOG_k[7] MCMD	xxx
Read the address of the request that caused the error.	LOGICAL_ADDR_ERRLOG_k[31:12] SLVOFS_LOGICAL	xxx
IF: Is it an application error?	L3_FLAGMUX_REGERR0[17:0] REGERROR0	= 0x0
Read the status bits to see which module firewall has worked.	CONTROL.CONTROL_SEC_ERR_STATUS_FUNC[20:0]	xxx
Clear the status bits.	CONTROL.CONTROL_SEC_ERR_STATUS_FUNC[20:0]	xxx
Clear the status bit.	L3_TARG_STDERRLOG_MAIN[31] STDERRLOG_MAIN_CLRLOG	0x0
ELSE IF	L3_FLAGMUX_REGERR1[17:0] REGERROR1	= 0x1
Read the status bits to see the module.	CONTROL.CONTROL_SEC_ERR_STATUS_DEBUG[20:0]	xxx
Clear the status bits.	CONTROL.CONTROL_SEC_ERR_STATUS_DEBUG[20:0]	xxx
Clear the status bit.	L3_TARG_STDERRLOG_MAIN[31] STDERRLOG_MAIN_CLRLOG	0x0
ENDIF		
Clear the burst violation.	ERROR_LOG_k[23] BLK_BURST_VIOLATION	0x0
Clear the error status.	ERROR_LOG_k[21:17] REGION_START_ERRLOG	0x00

13.2.4.2.1.1.2 Subsequence: L3 Interconnect Standard Error Identification

The procedure listed in Table 13-35 describes the identification of standard errors inside the L3 interconnect. The standard errors are: unsupported command, address hole, and disconnect.

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Table 13-35. L3 Standard Error Identification

Step	Register/Bit Field/Programming Model	Value
IF: Is an error detected?	L3_TARG_STDERRLOG_MAIN[18] STDERRLOG_MAIN_ERRCNT	= 0x1
Read the corresponding flag.	L3_FLAGMUX_REGERR0[17:0] REGERROR0	xxx
Read the corresponding flag.	L3_FLAGMUX_REGERR1[17:0] REGERROR1	xxx
Localize the slave NIU that generated the error.	See Table 13-30, *Interconnect Flag Mapping*.	
ELSE		
Clear the error log.	L3_TARG_STDERRLOG_MAIN[31] STDERRLOG_MAIN_CLRLOG	0x0
Clear the severity error status.	L3_TARG_STDERRLOG_SVRTSTDLVL[1:0] STDERRLOG_SVRTSTDLVL_0	0x2
ENDIF		

13.2.4.2.1.1.3 Subsequence: L3 Interconnect FLAGMUX Configuration

The procedure listed in Table 13-36 gives information about the configuration of FLAGMUX masks.

Table 13-36. FLAGMUX Configuration

Step	Register/Bit Field/Programming Model	Value
Set the FLAGMUX masks to mask an event.	L3_FLAGMUX_MASK0[17:0] MASK0 L3_FLAGMUX_MASK1[17:0] MASK1	xxx
Read the REGERR bits to see if an error is recorded.	L3_FLAGMUX_REGERR0[17:0] REGERR0 L3_FLAGMUX_REGERR1[17:0] REGERR1	xxx
Clear the slave NIU error log and the FLAGMUX error.	L3_TARG_STDERRLOG_MAIN[31] STDERRLOG_SVRTSTDLVL_0	0x2

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13.2.5 L3 Interconnect Register Manual

13.2.5.1 L3 Register Group Summary

The registers in the L3 interconnect are divided into eight groups:

- Firewall registers Table 13-38
- HOST registers Table 13-61
- TARG registers Table 13-97
- PWR_DISK registers Table 13-139
- FLAGMUX registers Table 13-163
- BW registers Table 13-178
- RA registers Table 13-193
- STATCOLL registers Table 13-201

13.2.5.1.1 L3 Firewall Registers Summary and Description

Table 13-37. L3 Firewall Instance Summary

Module Name	Base Address	Size
C2C-Master NIU Firewall	0x4A20 4000	4KB
C2C-Slave NIU Firewall	0x4A20 6000	4KB
MA Firewall	0x4A20 A000	4KB
EMIF Firewall	0x4A20 C000	4KB
GPMC Firewall	0x4A21 0000	4KB
L3 RAM Firewall	0x4A21 2000	4KB
SGX Firewall	0x4A21 4000	4KB
ISS Firewall	0x4A21 6000	4KB
Dual Cortex-M3 Firewall	0x4A21 8000	4KB
DSS Firewall	0x4A21 C000	4KB
SL2 Firewall	0x4A21 E000	4KB
IVA-HD Firewall	0x4A22 0000	4KB
Debug Firewall	0x4A22 6000	4KB
L4-ABE Firewall	0x4A22 8000	4KB

13.2.5.1.1.1 L3 Firewall Registers Summary

Table 13-38. L3 Firewall Registers Summary

Register Name	Type	Register Width (Bits)	Address Offset	MA Firewall L3 Physical Address	EMIF Firewall L3 Physical Address	GPMC Firewall L3 Physical Address	L3 RAM Firewall L3 Physical Address
ERROR_LOG_k (1)	RW	32	0x000+(0x10*k)	0x4A20 A000+(0x10*k)	0x4A20 C000+(0x10*k)	0x4A21 0000+(0x10*k)	0x4A21 2000+(0x10*k)
LOGICAL_ADDR_ERRLOG_k (1)	RO	32	0x004+(0x10*k)	0x4A20 A004+(0x10*k)	0x4A20 C004+(0x10*k)	0x4A21 0004+(0x10*k)	0x4A21 2004+(0x10*k)
REGUPDATE_CONTROL	RW	32	0x040	0x4A20 A040	0x4A20 C040	0x4A21 0040	0x4A21 2040

(1) k = 0 to 2 for EMIF Firewall
k = 0 to 2 for MA Firewall
k = 0 for GPMC Firewall
k = 0 for L3 RAM Firewall

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Table 13-38. L3 Firewall Registers Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	MA Firewall L3 Physical Address	EMIF Firewall L3 Physical Address	GPMC Firewall L3 Physical Address	L3 RAM Firewall L3 Physical Address
START_REGION_i [2]	RW	32	0x080+(0x10*i)	0x4A20 A080+(0x10*i)	0x4A20 C080+(0x10*i)	0x4A21 0080+(0x10*i)	0x4A21 2080+(0x10*i)
END_REGION_i [2]	RW	32	0x084+(0x10*i)	0x4A20 A084+(0x10*i)	0x4A20 C084+(0x10*i)	0x4A21 0084+(0x10*i)	0x4A21 2084+(0x10*i)
MRM_PERMISSION_REGION_HIGH_j [3]	RW	32	0x08C+(0x10*j)	0x4A20 A08C+(0x10*j)	0x4A20 C08C+(0x10*j)	0x4A21 008C+(0x10*j)	0x4A21 208C+(0x10*j)
MRM_PERMISSION_REGION_LOW_j [3]	RW	32	0x088+(0x10*j)	0x4A20 A088+(0x10*j)	0x4A20 C088+(0x10*j)	0x4A21 0088+(0x10*j)	0x4A21 2088+(0x10*j)

(2) i = 1 to 7 for EMIF Firewall
i = 1 to 7 for MA Firewall
i = 1 to 7 for GPMC Firewall
i = 1 to 9 for L3 RAM Firewall

(3) j = 0 to 7 for EMIF Firewall
j = 0 to 7 for MA Firewall
j = 0 to 7 for GPMC Firewall
j = 0 to 9 for L3 RAM Firewall

Table 13-39. L3 Firewall Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	SGX Firewall L3 Physical Address	ISS Firewall L3 Physical Address	Dual Cortex-M3 Firewall L3 Physical Address
ERROR_LOG_k [1]	RW	32	0x000+(0x10*k)	0x4A21 4000+(0x10*k)	0x4A21 6000+(0x10*k)	0x4A21 8000+(0x10*k)
LOGICAL_ADDR_ERRLOG_k [1]	RO	32	0x004+(0x10*k)	0x4A21 4004+(0x10*k)	0x4A21 6004+(0x10*k)	0x4A21 8004+(0x10*k)
REGUPDATE_CONTROL	RW	32	0x040	0x4A21 4040	0x4A21 6040	0x4A21 8040
START_REGION_i [2]	RW	32	0x080+(0x10*i)	N/A	N/A	N/A
END_REGION_i [2]	RW	32	0x084+(0x10*i)	N/A	N/A	N/A
MRM_PERMISSION_REGION_HIGH_j [3]	RW	32	0x08C+(0x10*j)	0x4A21 408C+(0x10*j)	0x4A21 608C+(0x10*j)	0x4A21 808C+(0x10*j)
MRM_PERMISSION_REGION_LOW_j [3]	RW	32	0x088+(0x10*j)	0x4A21 4088+(0x10*j)	0x4A21 6088+(0x10*j)	0x4A21 8088+(0x10*j)

(1) k = 0 for SGX Firewall
k = 0 for ISS Firewall
k = 0 for Dual Cortex-M3 Firewall

(2) i = 0 for SGX Firewall
i = 0 for ISS Firewall
i = 0 for Dual Cortex-M3 Firewall

(3) j = 0 for SGX Firewall
j = 0 for ISS Firewall
j = 0 for Dual Cortex-M3 Firewall

Table 13-40. L3 Firewall Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	DSS Firewall L3 Physical Address	SL2 Firewall L3 Physical Address	IVA-HD Firewall L3 Physical Address
ERROR_LOG_k [1]	RW	32	0x000+(0x10*k)	0x4A21 C000+(0x10*k)	0x4A21 E000+(0x10*k)	0x4A22 0000+(0x10*k)
LOGICAL_ADDR_ERRLOG_k [1]	RO	32	0x004+(0x10*k)	0x4A21 C004+(0x10*k)	0x4A21 E004+(0x10*k)	0x4A22 0004+(0x10*k)

(1) k = 0 for DSS Firewall
k = 0 for SL2 Firewall
k = 0 for IVA-HD Firewall

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Table 13-40. L3 Firewall Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	DSS Firewall L3 Physical Address	SL2 Firewall L3 Physical Address	IVA-HD Firewall L3 Physical Address
REGUPDATE_CONTROL	RW	32	0x040	0x4A21 C040	0x4A21 E040	0x4A22 0040
START_REGION_i	RW	32	0x080+(0x10*i)	N/A	N/A	N/A
END_REGION_i	RW	32	0x084+(0x10*i)	N/A	N/A	N/A
MRM_PERMISSION_REGION_HIGH_j (2)	RW	32	0x08C+(0x10*j)	0x4A21 C08C+(0x10*j)	0x4A21 E08C+(0x10*j)	0x4A22 008C+(0x10*j)
MRM_PERMISSION_REGION_LOW_j (2)	RW	32	0x088+(0x10*j)	0x4A21 C088+(0x10*j)	0x4A21 E088+(0x10*j)	0x4A22 0088+(0x10*j)

(2) j = 0 for DSS Firewall
j = 0 for SL2 Firewall
j = 0 for IVA-HD Firewall

Table 13-41. L3 Firewall Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	Debug Firewall L3 Physical Address	L4-ABE Firewall L3 Physical Address
ERROR_LOG_k (1)	RW	32	0x000+(0x10*k)	0x4A22 6000+(0x10*k)	0x4A22 8000+(0x10*k)
LOGICAL_ADDR_ERRLOG_k (1)	RO	32	0x004+(0x10*k)	0x4A22 6004+(0x10*k)	0x4A22 8004+(0x10*k)
REGUPDATE_CONTROL	RW	32	0x040	0x4A22 6040	0x4A22 8040
START_REGION_i (2)	RW	32	0x080+(0x10*i)	0x4A22 6080+(0x10*i)	N/A
END_REGION_i (2)	RW	32	0x084+(0x10*i)	0x4A22 6084+(0x10*i)	N/A
MRM_PERMISSION_REGION_HIGH_j (3)	RW	32	0x08C+(0x10*j)	0x4A22 608C+(0x10*j)	0x4A22 808C+(0x10*j)
MRM_PERMISSION_REGION_LOW_j (3)	RW	32	0x088+(0x10*j)	0x4A22 6088+(0x10*j)	0x4A22 8088+(0x10*j)

(1) k = 0 for Debug Firewall
k = 0 for L4-ABE Firewall
(2) i = 1 for Debug Firewall
i= 0 for L4-ABE Firewall
(3) j = 0 to 1 for Debug Firewall
j = 0 for L4-ABE Firewall

Table 13-42. L3 Firewall Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	C2C-Master NIU Firewall L3 Physical Address	C2C-Slave NIU Firewall L3 Physical Address
ERROR_LOG_k (1)	RW	32	0x000+(0x10*k)	0x4A20 4000+(0x10*k)	0x4A20 6000+(0x10*k)
LOGICAL_ADDR_ERRLOG_k (1)	RO	32	0x004+(0x10*k)	0x4A20 4004+(0x10*k)	0x4A22 6004+(0x10*k)
REGUPDATE_CONTROL	RW	32	0x040	0x4A20 4040	0x4A22 6040
START_REGION_i (2)	RW	32	0x080+(0x10*i)	0x4A20 4080+(0x10*i)	N/A
END_REGION_i (2)	RW	32	0x084+(0x10*i)	0x4A20 4084+(0x10*i)	N/A

(1) k = 0 for C2C-Master NIU Firewall
k = 0 for C2C-Slave NIU Firewall
(2) i = 1 to 3 for C2C-Master NIU Firewall

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Table 13-42. L3 Firewall Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	C2C-Master NIU Firewall L3 Physical Address	C2C-Slave NIU Firewall L3 Physical Address
MRM_PERMISSION_REGION_HIGH_j [3]	RW	32	0x08C+(0x10*j)	0x4A20 408C+(0x10*j)	0x4A22 608C+(0x10*j)
MRM_PERMISSION_REGION_LOW_j [3]	RW	32	0x088+(0x10*j)	0x4A20 4088+(0x10*j)	0x4A22 6088+(0x10*j)

(3) j = 0 for C2C-Master NIU Firewall
j = 0 to 3 for C2C-Slave NIU Firewall

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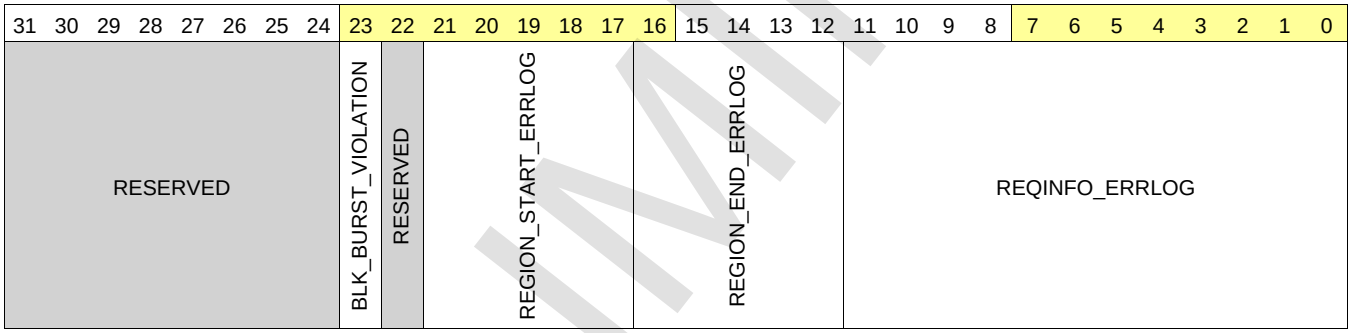
13.2.5.1.1.2 L3 Firewall Registers Description

NOTE: Hardware reset values can be modified by exported values from the control module at reset.

Table 13-43. ERROR_LOG_k

Address Offset	0x0000 0000+(0x10*k)	**Index**	See Table 13-38 to Table 13-42.
Physical Address	0x4A20 A000+(0x10*k) 0x4A20 C000+(0x10*k) 0x4A21 0000+(0x10*k) 0x4A21 2000+(0x10*k) 0x4A21 4000+(0x10*k) 0x4A21 6000+(0x10*k) 0x4A21 8000+(0x10*k) 0x4A21 C000+(0x10*k) 0x4A21 E000+(0x10*k) 0x4A22 0000+(0x10*k) 0x4A22 6000+(0x10*k) 0x4A22 8000+(0x10*k) 0x4A20 4000+(0x10*k) 0x4A20 6000+(0x10*k)		
Description	Error log register for port k		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:24	RESERVED	Reads return 0s.	R	0x00
23	BLK_BURST_VIOLATION	Read 0x1: 2D burst not allowed or exceeding allowed size Write to clear ERROR_LOG_k and LOGICAL_ADDR_ERRLOG_k registers	RW	0
22	RESERVED	Reads return 0s.	R	0
21:17	REGION_START_ERRLOG	Read: Wrong access hit this region number Write to clear ERROR_LOG_k and LOGICAL_ADDR_ERRLOG_k registers	RW	0x00
16:12	REGION_END_ERRLOG	Read: Wrong access hit this region number Write to clear ERROR_LOG_k and LOGICAL_ADDR_ERRLOG_k registers	RW	0x00
11:0	REQINFO_ERRLOG	Read: Error in reqinfo vector mapped as follows: [11: 8] ConnID [3:0] [7] MCMD [0] [6:4] Reserved [3] MReqDebug [2] Reserved [1] MReqSupervisor [0] MReqType Write to clear ERROR_LOG_k and LOGICAL_ADDR_ERRLOG_k registers	RW	0x000

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Table 13-44. Register Call Summary for Register ERROR_LOG_k

L3 Interconnect

- L3 Firewall Functionality: [0] [1] [2] [3] [4] [5] [6] [7]
- L3 Interconnect Error Analysis Mode: [8] [9] [10] [11] [12] [13]
- L3 Firewall Registers Summary and Description: [14] [15] [16] [17] [18] [19] [20] [21] [22]

Table 13-45. LOGICAL_ADDR_ERRLOG_k

Address Offset	0x0000 0004+(0x10*k)	**Index**	See Table 13-38 to Table 13-42.
Physical Address	0x4A20 A004+(0x10*k) 0x4A20 C004+(0x10*k) 0x4A21 0004+(0x10*k) 0x4A21 2004+(0x10*k) 0x4A21 4004+(0x10*k) 0x4A21 6004+(0x10*k) 0x4A21 8004+(0x10*k) 0x4A21 C004+(0x10*k) 0x4A21 E004+(0x10*k) 0x4A22 0004+(0x10*k) 0x4A22 6004+(0x10*k) 0x4A22 8004+(0x10*k) 0x4A20 4004+(0x10*k) 0x4A22 6004+(0x10*k)		
Description	Logical Physical Address Error log register for port k		
Type	RO		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SLVOFS_LOGICAL																															

Bits	Field Name	Description	Type	Reset
31[(1)]:0	SLVOFS_LOGICAL	Address generated by the Initiator before being translated	R	0x00000

(1) * = Size of the target

Table 13-46. Register Call Summary for Register LOGICAL_ADDR_ERRLOG_k

L3 Interconnect

- L3 Firewall Functionality: [0] [1] [2] [3]
- L3 Interconnect Error Analysis Mode: [4]
- L3 Firewall Registers Summary and Description: [5] [6] [7] [8] [9] [10] [11] [12] [13]

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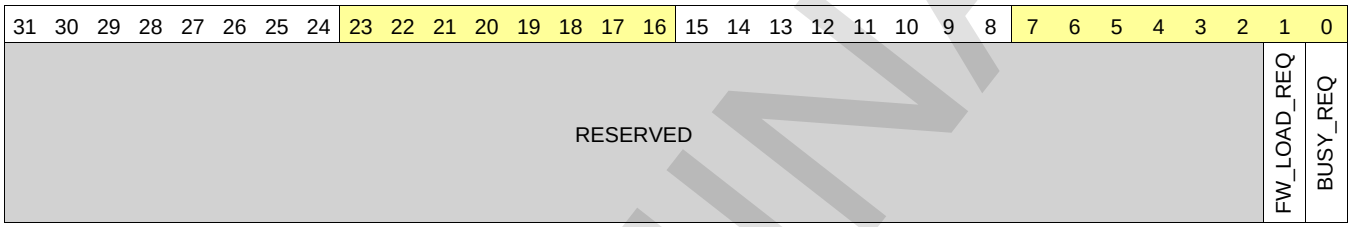
Table 13-47. REGUPDATE_CONTROL

Address Offset	0x0000 0040
Physical Address	0x4A20 A040 0x4A20 C040 0x4A21 0040 0x4A21 2040 0x4A21 4040 0x4A21 6040 0x4A21 8040 0x4A21 C040 0x4A21 E040 0x4A22 0040 0x4A22 6040 0x4A22 8040 0x4A20 4040 0x4A22 6040
Description	Register update control register
Type	RW



Bits	Field Name	Description	Type	Reset
31:2	RESERVED	Reads return 0s.	R	0x0000 0000
1	FW_LOAD_REQ	Hadrdware set/Software clear	R	0x1
0	BUSY_REQ	Busy request	RW	0x0

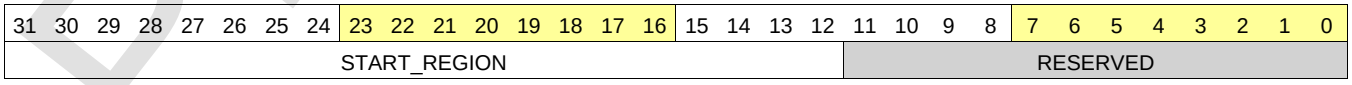
Table 13-48. Register Call Summary for Register REGUPDATE_CONTROL

L3 Interconnect

- L3 Firewall Reset: [0] [1] [2] [3] [4] [5] [6] [7] [8]
- L3 Firewall Registers Summary and Description: [9] [10] [11] [12] [13]

Table 13-49. START_REGION_i

Address Offset	0x0000 0080+(0x10*i)	**Index**	See Table 13-38 to Table 13-42.
Physical Address	0x4A20 A080+(0x10*i) 0x4A20 C080+(0x10*i) 0x4A21 0080+(0x10*i) 0x4A21 2080+(0x10*i) 0x4A22 6080+(0x10*i) 0x4A20 4080+(0x10*i)		
Description	Start physical address of region i		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:12	START_REGION	Physical target start address of firewall region i. The size of this bit field depends on target addressable space, the maximum is [31:12]. See Table 13-51.	RW	0x00000
11:0	RESERVED	Reads return 0s.	R	0x0000

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Table 13-50. Register Call Summary for Register START_REGION_i

L3 Interconnect

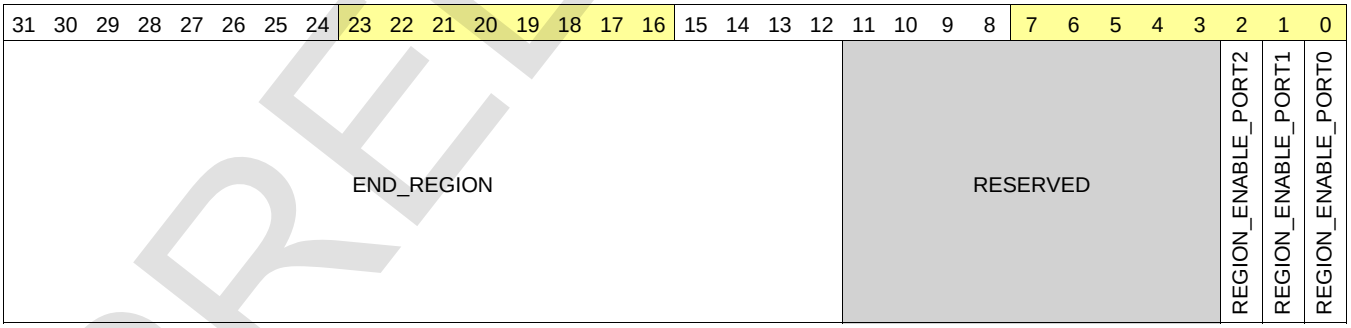
- L3 Firewall Functionality: [0] [1]
- L3 Firewall Registers Summary and Description: [2] [3] [4] [5] [6] [7] [8] [9] [10] [11]

Table 13-51. Size of START_REGION_i[] START_REGION Bit Field

Firewall	Bit Field
EMIF Firewall	START_REGION_i[31:12] START_REGION
GPMC Firewall	START_REGION_i[30:12] START_REGION
L3 RAM Firewall	START_REGION_i[15:12] START_REGION
SGX Firewall	N/A
ISS Firewall	N/A
Dual Cortex-M3 Firewall	N/A
DSS Firewall	N/A
SL2 Firewall	N/A
IVA-HD Firewall	N/A
Debug Firewall	START_REGION_i[21:12] START_REGION
L4-AUDIO Firewall	N/A
C2C-Slave NIU Firewall	N/A
C2C-Master NIU Firewall	START_REGION_i[28:12] START_REGION

Table 13-52. END_REGION_i

Address Offset	0x0000 0084+(0x10*i)	**Index**	See Table 13-38 to Table 13-42.
Physical Address	0x4A20 A084+(0x10*i) 0x4A20 C084+(0x10*i) 0x4A21 0084+(0x10*i) 0x4A21 2084+(0x10*i) 0x4A22 6084+(0x10*i) 0x4A20 4084+(0x10*i)		
Description	End physical address of region i		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:12	END_REGION	Physical target end address of firewall region i. The size of this bit field depends on target addressable space, the maximum is [31:12]. See Table 13-54.	RW	0x00000
11:3	RESERVED	Reads return 0s.	R	0x0000
2	REGION_ENABLE_PORT2	Enable this region for port 2(1).	RW	0x0
1	REGION_ENABLE_PORT1	Enable this region for port 1(2).	RW	0x0

(1) Only for multiport firewalls with at least 2 ports: EMIF Firewall
(2) Only for multiport firewalls with at least 1 port: EMIF and Crypto Firewall

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Bits	Field Name	Description	Type	Reset
0	REGION_ENABLE_PORT0	Enable this region for port 0.	RW	0x0

Table 13-53. Register Call Summary for Register END_REGION_i

L3 Interconnect

- L3 Firewall Functionality: [0] [1] [2] [3] [4] [5]
- L3 Firewall Registers Summary and Description: [6] [7] [8] [9] [10] [11] [12] [13] [14] [15]

Table 13-54. Size of END_REGION_i[] END_REGION Bit Field

Firewall	Bit Field
EMIF Firewall	END_REGION_i[31:12] END_REGION
GPMC Firewall	END_REGION_i[30:12] END_REGION
L3 RAM Firewall	END_REGION_i[15:12] END_REGION
SGX Firewall	N/A
ISS Firewall	N/A
Dual Cortex-M3 Firewall	N/A
DSS Firewall	N/A
SL2 Firewall	N/A
IVA-HD Firewall	N/A
Debug Firewall	END_REGION_i[21:12] END_REGION
L4-AUDIO Firewall	N/A
C2C-Slave NIU Firewall	N/A
C2C-Master NIU Firewall	END_REGION_i[28:12] END_REGION

Table 13-55. MRM_PERMISSION_REGION_HIGH_j

Address Offset	0x0000 008C+(0x10*i)	**Index**	See Table 13-38 to Table 13-42.
Physical Address	0x4A20 A08C+(0x10*j) 0x4A20 C08C+(0x10*j) 0x4A21 008C+(0x10*j) 0x4A21 208C+(0x10*j) 0x4A21 408C+(0x10*j) 0x4A21 608C+(0x10*j) 0x4A21 808C+(0x10*j) 0x4A21 C08C+(0x10*j) 0x4A21 E08C+(0x10*j) 0x4A22 008C+(0x10*j) 0x4A22 608C+(0x10*j) 0x4A22 808C+(0x10*j) 0x4A20 408C+(0x10*j) 0x4A22 608C+(0x10*j)		
Description	Region j Permission High		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						W12	R12	RESERVED	RESERVED	W10	R10	W9	R9	W8	R8	W7	R7	W6	R6	W5	R5	W4	R4	W3	R3	W2	R2	W1	R1	W0	R0

Bits	Field Name	Description	Type	Reset
31:26	RESERVED	Reserved	RW	0x3F
25	W12	Master NIU ConnID = 12 write permission	RW	0x1
24	R12	Master NIU ConnID = 12 read permission	RW	0x1

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Bits	Field Name	Description	Type	Reset
23	RESERVED	Reserved	RW	0x1
22	RESERVED	Reserved	RW	0x1
21	W10	Master NIU ConnID = 10 write permission	RW	0x1
20	R10	Master NIU ConnID = 10 read permission	RW	0x1
19	W9	Master NIU ConnID = 9 write permission	RW	0x1
18	R9	Master NIU ConnID = 9 read permission	RW	0x1
17	W8	Master NIU ConnID = 8 write permission	RW	0x1
16	R8	Master NIU ConnID = 8 read permission	RW	0x1
15	W7	Master NIU ConnID = 7 write permission	RW	0x1
14	R7	Master NIU ConnID = 7 read permission	RW	0x1
13	W6	Master NIU ConnID = 6 write permission	RW	0x1
12	R6	Master NIU ConnID = 6 read permission	RW	0x1
11	W5	Master NIU ConnID = 5 write permission	RW	0x1
10	R5	Master NIU ConnID = 5 read permission	RW	0x1
9	W4	Master NIU ConnID = 4 write permission	RW	0x1
8	R4	Master NIU ConnID = 4 read permission	RW	0x1
7	W3	Master NIU ConnID = 3 write permission	RW	0x1
6	R3	Master NIU ConnID = 3 read permission	RW	0x1
5	W2	Master NIU ConnID = 2 write permission	RW	0x1
4	R2	Master NIU ConnID = 2 read permission	RW	0x1
3	W1	Master NIU ConnID = 1 write permission	RW	0x1
2	R1	Master NIU ConnID = 1 read permission	RW	0x1
1	W0	Master NIU ConnID = 0 write permission	RW	0x1
0	R0	Master NIU ConnID = 0 read permission	RW	0x1

Table 13-56. Register Call Summary for Register MRM_PERMISSION_REGION_HIGH_j

L3 Interconnect

- L3 Firewall Functionality: [0] [1] [2] [3] [4] [5]
- L3 Firewall Registers Summary and Description: [6] [7] [8] [9] [10]

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Table 13-57. MRM_PERMISSION_REGION_LOW_j

Address Offset	0x0000 0088+(0x10*i)	**Index**	See Table 13-38 to Table 13-42.
Physical Address	0x4A20 A088+(0x10*j) 0x4A20 C088+(0x10*j) 0x4A21 0088+(0x10*j) 0x4A21 2088+(0x10*j) 0x4A21 4088+(0x10*j) 0x4A21 6088+(0x10*j) 0x4A21 8088+(0x10*j) 0x4A21 C088+(0x10*j) 0x4A21 E088+(0x10*j) 0x4A22 0088+(0x10*j) 0x4A22 6088+(0x10*j) 0x4A22 8088+(0x10*j) 0x4A20 4088+(0x10*j) 0x4A22 6088+(0x10*j)		
Description	Region j Permission Low		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	PUB_PRV_DEBUG	PUB_USR_DEBUG	RESERVED	RESERVED	PUB_PRV_WRITE	PUB_PRV_READ	PUB_PRV_EXE	PUB_USR_WRITE	PUB_USR_READ	PUB_USR_EXE	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED

Bits	Field Name	Description	Type	Reset
31	RESERVED	Reserved	RW	See Table 13-59.
30	RESERVED	Reserved	RW	See Table 13-59.
29	RESERVED	Reserved	RW	See Table 13-59.
28	RESERVED	Reserved	RW	See Table 13-59.
27	RESERVED	Reserved	RW	See Table 13-59.
26	RESERVED	Reserved	RW	See Table 13-59.
25	RESERVED	Reserved	RW	See Table 13-59.
24	RESERVED	Reserved	RW	See Table 13-59.
23	RESERVED	Reserved	RW	See Table 13-59.
22	RESERVED	Reserved	RW	See Table 13-59.
21	RESERVED	Reserved	RW	See Table 13-59.
20	RESERVED	Reserved	RW	See Table 13-59.
19	RESERVED	Reserved	RW	See Table 13-59.
18	RESERVED	Reserved	RW	See Table 13-59.
17	RESERVED	Reserved	RW	See Table 13-59.
16	RESERVED	Reserved	RW	See Table 13-59.
15	PUB_PRV_DEBUG	Public Privilege Debug Allowed	RW	See Table 13-59.
14	PUB_USR_DEBUG	Public User Debug Allowed	RW	See Table 13-59.
13	RESERVED	Reserved	RW	See Table 13-59.
12	RESERVED	Reserved	RW	See Table 13-59.
11	PUB_PRV_WRITE	Public Privilege Write Allowed	RW	See Table 13-59.
10	PUB_PRV_READ	Public Privilege Read Allowed	RW	See Table 13-59.
9	PUB_PRV_EXE	Public Privilege Exe Allowed	RW	See Table 13-59.
8	PUB_USR_WRITE	Public User Write Access Allowed	RW	See Table 13-59.
7	PUB_USR_READ	Public User Read Access Allowed	RW	See Table 13-59.
6	PUB_USR_EXE	Public User Exe Access Allowed	RW	See Table 13-59.

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Bits	Field Name	Description	Type	Reset
5	RESERVED	Reserved	RW	See Table 13-59.
4	RESERVED	Reserved	RW	See Table 13-59.
3	RESERVED	Reserved	RW	See Table 13-59.
2	RESERVED	Reserved	RW	See Table 13-59.
1	RESERVED	Reserved	RW	See Table 13-59.
0	RESERVED	Reserved	RW	See Table 13-59.

Table 13-58. Register Call Summary for Register MRM_PERMISSION_REGION_LOW_j

L3 Interconnect
- L3 Firewall Reset: [0] [1]
- L3 Firewall Functionality: [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14]
- L3 Firewall Registers Summary and Description: [15] [16] [17] [18] [19]

Table 13-59. Reset Value for MRM_PERMISSION_REGION_LOW_j

Region	Reset Value
Region j = 0 (except EMIF firewall)	0xFFFF0000
Region j = 0 (for EMIF firewall)	0xFFFFFFFF
Region j 0 (for all firewalls)	0xFFFFFFFF

13.2.5.1.2 L3 Host Register Summary and Description

Table 13-60. HOST Instance Summary

Module Name	Base Address	Size
CLK1_HOST_CLK1	0x4400 0000	8MB
CLK2_HOST_CLK2	0x4480 0000	8MB
CLK3_HOST_CLK3	0x4500 0000	8MB

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13.2.5.1.2.1 L3 HOST Register Summary

Table 13-61. HOST Registers Summary

Register Name	Type	Register Width (Bits)	Address Offset for CLK1_HOST_CLK1	CLK1_HOST_CLK1 L3 Physical Address	Address Offset for CLK2_HOST_CLK2	CLK2_HOST_CLK2 L3 Physical Address	Address Offset for CLK3_HOST_CLK3	CLK3_HOST_CLK3 L3 Physical Address
L3_HOST_STDHOSTHDR_COREREG	R	32	0x0000 0000	0x4400 0000	0x0080 0000	0x4480 0000	0x0100 0000	0x4500 0000
L3_HOST_STDHOSTHDR_VERSIONREG	R	32	0x0000 0004	0x4400 0004	0x0080 0004	0x4480 0004	0x0100 0004	0x4500 0004
L3_HOST_STDHOSTHDR_MAINCTLREG	R	32	0x0000 0008	0x4400 0008	0x0080 0008	0x4480 0008	0x0100 0008	0x4500 0008
L3_HOST_STDERRLOG_SVRTSTDLVL	RW	32	0x0000 0040	0x4400 0040	0x0080 0040	0x4480 0040	0x0100 0040	0x4500 0040
L3_HOST_STDERRLOG_SVRTCUSTOMLVL	RW	32	0x0000 0044	0x4400 0044	0x0080 0044	0x4480 0044	0x0100 0044	0x4500 0044
L3_HOST_STDERRLOG_MAIN	RW	32	0x0000 0048	0x4400 0048	0x0080 0048	0x4480 0048	0x0100 0048	0x4500 0048
L3_HOST_STDERRLOG_HDR	R	32	0x0000 004C	0x4400 004C	0x0080 004C	0x4480 004C	0x0100 004C	0x4500 004C
L3_HOST_STDERRLOG_MSTADDR	R	32	0x0000 0050	0x4400 0050	0x0080 0050	0x4480 0050	0x0100 0050	0x4500 0050
L3_HOST_STDERRLOG_SLVADDR	R	32	0x0000 0054	0x4400 0054	0x0080 0054	0x4480 0054	0x0100 0054	0x4500 0054
L3_HOST_STDERRLOG_INFO	R	32	0x0000 0058	0x4400 0058	0x0080 0058	0x4480 0058	0x0100 0058	0x4500 0058
L3_HOST_STDERRLOG_SLVOFSLSB	R	32	0x0000 005C	0x4400 005C	0x0080 005C	0x4480 005C	0x0100 005C	0x4500 005C
L3_HOST_STDERRLOG_SLVOFSMSB	R	32	0x0000 0060	0x4400 0060	0x0080 0060	0x4480 0060	0x0100 0060	0x4500 0060
L3_HOST_STDERRLOG_CUSTOMINFO_MSTADDR	R	32	0x0000 0064	0x4400 0064	0x0080 0064	0x4480 0064	0x0100 0064	0x4500 0064
L3_HOST_STDERRLOG_CUSTOMINFO_INFO	R	32	0x0000 0068	0x4400 0068	0x0080 0068	0x4480 0068	0x0100 0068	0x4500 0068
L3_HOST_STDERRLOG_CUSTOMINFO_WR	R	32	0x0000 006C	0x4400 006C	0x0080 006C	0x4480 006C	0x0100 006C	0x4500 006C
L3_HOST_STDERRLOG_CUSTOMINFO_ADDR	R	32	0x0000 0070	0x4400 0070	0x0080 0070	0x4480 0070	0x0100 0070	0x4500 0070
L3_HOST_STDERRLOG_CUSTOMINFO_DECERR	R	32	0x0000 0074	0x4400 0074	0x0080 0074	0x4480 0074	0x0100 0074	0x4500 0074

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13.2.5.1.2.2 L3 HOST Register Description

Table 13-62. L3_HOST_STDHOSTHDR_COREREG

Address Offset	See Table 13-61.		
Physical Address	0x4400 0000 0x4480 0000 0x4500 0000	**Instance**	CLK1_HOST_CLK1 CLK2_HOST_CLK2 CLK3_HOST_CLK3
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								STDHOSTHDR_COREREG_CORECODE								RESERVED								STDHOSTHDR_COREREG_VENDORCODE							

Bits	Field Name	Description	Type	Reset
31:22	RESERVED		R	0x000
21:16	STDHOSTHDR_COREREG_CORECODE	The Core Code field is a constant reporting a vendor-specific core generator code. Type: Constant. Reset value: 0x1A.	R	0x1A
15:1	RESERVED		R	0x0000
0	STDHOSTHDR_COREREG_VENDORCODE	The Vendor Code field is a constant reporting the core generator vendor code. Type: Constant. Reset value: 0x1. Read 0x0: Third-party vendor. Read 0x1:	R	1

Table 13-63. Register Call Summary for Register L3_HOST_STDHOSTHDR_COREREG

L3 Interconnect

- L3 Host Register Summary and Description: [0]

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Table 13-64. L3_HOST_STDHOSTHDR_VERSIONREG

Address Offset	See Table 13-61.		
Physical Address	0x4400 0004 0x4480 0004 0x4500 0004	**Instance**	CLK1_HOST_CLK1 CLK2_HOST_CLK2 CLK3_HOST_CLK3
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STDHOSTHDR_VERSIONREG_REVISIONID								STDHOSTHDR_VERSIONREG_COREPARAMSCHECKSUM																							

Bits	Field Name	Description	Type	Reset
31:24	STDHOSTHDR_VERSIONREG_REVISIONID	The Revision Identifier field is a constant reporting the core generator revision number. Type: Constant. Reset value: 0x0.	R	0x00
23:0	STDHOSTHDR_VERSIONREG_COREPARAMSCHECKSUM	Reserved. Type: Reserved. Reset value: Reserved.	R	0x000000

Table 13-65. Register Call Summary for Register L3_HOST_STDHOSTHDR_VERSIONREG

L3 Interconnect

- L3 Host Register Summary and Description: [0]

Table 13-66. L3_HOST_STDHOSTHDR_MAINCTLREG

Address Offset	See Table 13-61.		
Physical Address	0x4400 0008 0x4480 0008 0x4500 0008	**Instance**	CLK1_HOST_CLK1 CLK2_HOST_CLK2 CLK3_HOST_CLK3
Description			
Type	R		

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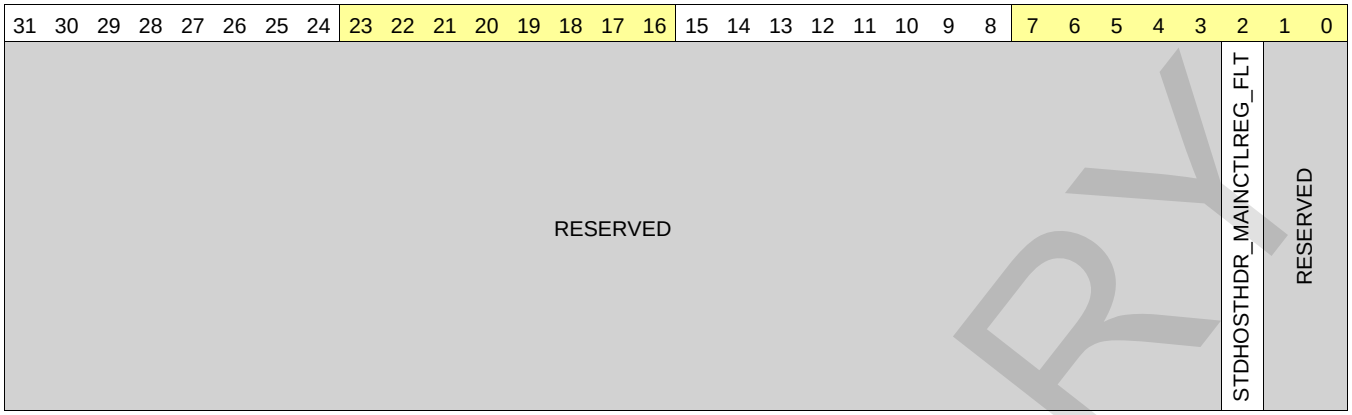


Bits	Field Name	Description	Type	Reset
31:3	RESERVED		R	0x0000 0000
2	STDHOSTHDR_MAINCTLREG_FLT	Asserted when a Fault condition is detected: if the unit includes Error Logging, Flt is asserted when the FltCnt register field indicates a Fault, and deasserted when FltCnt is reset. If no Error Logging is implemented, this bit becomes unit-dependent. In all cases, Flt bit and Flt pin (service network) have the same logical level. Type: Status. Reset value: X.	R	0
1:0	RESERVED		R	0x0

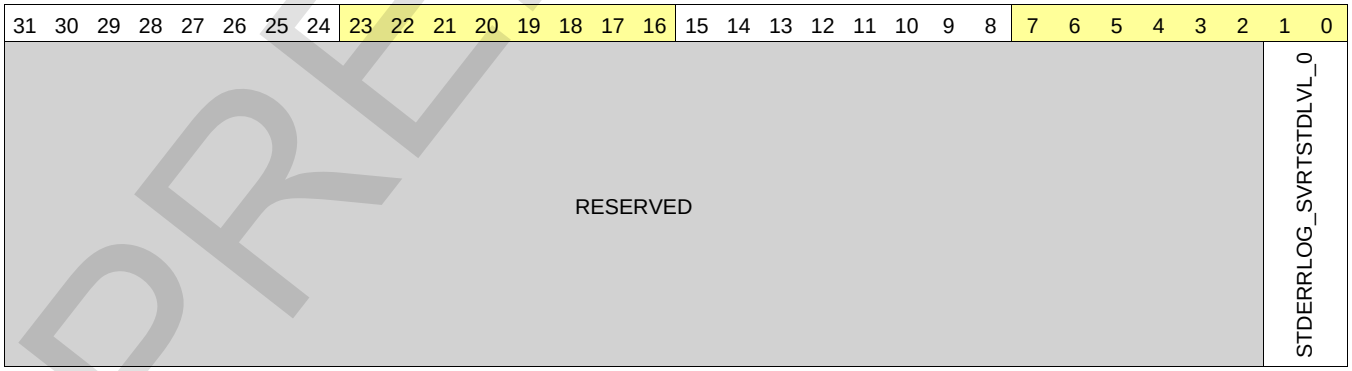
Table 13-67. Register Call Summary for Register L3_HOST_STDHOSTHDR_MAINCTLREG

L3 Interconnect

- L3 Host Register Summary and Description: [0]

Table 13-68. L3_HOST_STDERRLOG_SVRTSTDLVL

Address Offset	See Table 13-61.		
Physical Address	0x4400 0040 0x4480 0040 0x4500 0040	**Instance**	CLK1_HOST_CLK1 CLK2_HOST_CLK2 CLK3_HOST_CLK3
Description			
Type	RW		



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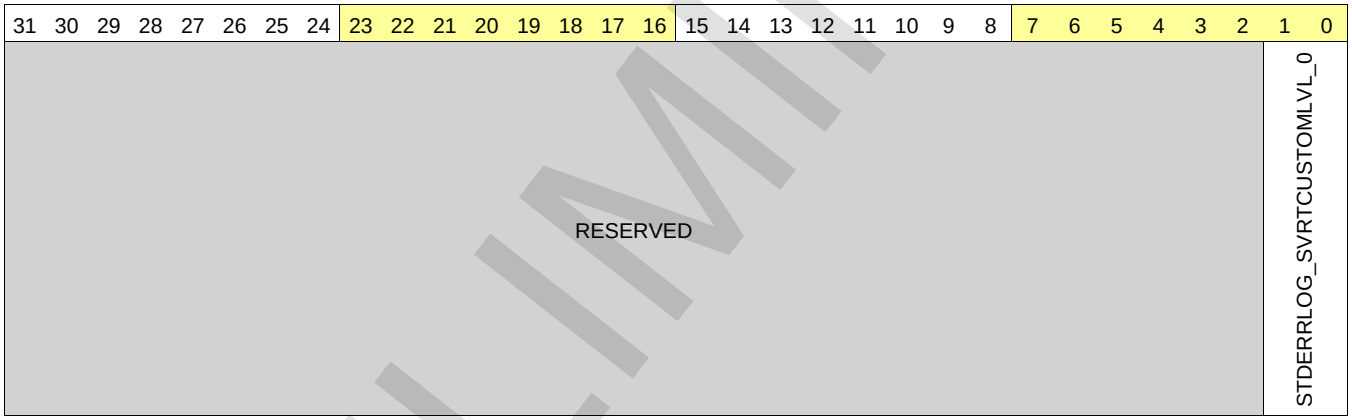
Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1:0	STDERRLOG_SVRTSTDLVL_0	Severity level parameters Type: Control. Reset value: 0x0. 0x0: Error logging is disabled. 0x1: Errors are logged with severity level Error. 0x2: Errors are logged with severity level Fault.	RW	0x0

Table 13-69. Register Call Summary for Register L3_HOST_STDERRLOG_SVRTSTDLVL

L3 Interconnect
- L3 Host Register Summary and Description: [0]

Table 13-70. L3_HOST_STDERRLOG_SVRTCUSTOMLVL

Address Offset	See Table 13-61.		
Physical Address	0x4400 0044 0x4480 0044 0x4500 0044	**Instance**	CLK1_HOST_CLK1 CLK2_HOST_CLK2 CLK3_HOST_CLK3
Description			
Type	RW		



Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1:0	STDERRLOG_SVRTCUSTOMLVL_0	Severity level parameters Type: Control. Reset value: 0x0. 0x0: Error logging is disabled. 0x1: Errors are logged with severity level Error. 0x2: Errors are logged with severity level Fault.	RW	0x0

Table 13-71. Register Call Summary for Register L3_HOST_STDERRLOG_SVRTCUSTOMLVL

L3 Interconnect
- L3 Host Register Summary and Description: [0]

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Table 13-72. L3_HOST_STDERRLOG_MAIN

Address Offset	See Table 13-61.		
Physical Address	0x4400 0048 0x4480 0048 0x4500 0048	**Instance**	CLK1_HOST_CLK1 CLK2_HOST_CLK2 CLK3_HOST_CLK3
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STDERRLOG_MAIN_CLRLOG	RESERVED											STDERRLOG_MAIN_FLTCNT	STDERRLOG_MAIN_ERRCNT	RESERVED																	STDERRLOG_MAIN_ERRTYPE	STDERRLOG_MAIN_ERRLOGVLD

Bits	Field Name	Description	Type	Reset
31	STDERRLOG_MAIN_CLRLOG	Clears Error Logging Valid bit when written to 1. Type: Give_AutoCleared. Reset value: 0x0.	RW	0
30:20	RESERVED		R	0x000
19	STDERRLOG_MAIN_FLTCNT	Asserted when at least one error with severity level FAULT is detected. Reset when written to 1. Type: Take. Reset value: 0x0.	RW	0
18	STDERRLOG_MAIN_ERRCNT	Asserted when at least one error with severity level ERROR is detected. Reset when written to 1. Type: Take. Reset value: 0x0.	RW	0
17:2	RESERVED		R	0x0000
1	STDERRLOG_MAIN_ERRTYPE	Indicates logging type. Type: Status. Reset value: X. Read 0x0: Logged Error format is standard (header and necker recorded). Read 0x1: Logged Error format is module dependent. CustomInfo register(s) may be implemented to store additional information.	R	0
0	STDERRLOG_MAIN_ERRLOGVLD	Error Logging Valid. Asserted when logging information is valid(indicates that an error has been logged). Type: Status. Reset value: X.	R	0

Table 13-73. Register Call Summary for Register L3_HOST_STDERRLOG_MAIN

L3 Interconnect

- L3 Host Register Summary and Description: [0]

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Table 13-74. L3_HOST_STDERRLOG_HDR

Address Offset	See Table 13-61.		
Physical Address	0x4400 004C 0x4480 004C 0x4500 004C	**Instance**	CLK1_HOST_CLK1 CLK2_HOST_CLK2 CLK3_HOST_CLK3
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								STDERRLOG_HDR_LEN1						RESERVED		STDERRLOG_HDR_STOPOFSWRPSZ				STDERRLOG_HDR_ERR	RESERVED			STDERRLOG_HDR_PRESSURE	RESERVED			STDERRLOG_HDR_OPCODE			

Bits	Field Name	Description	Type	Reset
31:24	RESERVED		R	0x00
23:18	STDERRLOG_HDR_LEN1	This field contains the number of payload cell(s) minus one of the logged packet. Type: Status. Reset value: X.	R	0x00
17:16	RESERVED		R	0x0
15:12	STDERRLOG_HDR_STOPOFSWRPSZ	StopOfs or WrapSize field of the logged packet (meaning depends on Wrp bit of logged opcode). Type: Status. Reset value: X.	R	0x0
11	STDERRLOG_HDR_ERR	Err bit of the logged packet. Type: Status. Reset value: X.	R	0
10:7	RESERVED		R	0x0
6	STDERRLOG_HDR_PRESSURE	Pressure field of the logged packet. Type: Status. Reset value: X.	R	0
5:4	RESERVED		R	0x0
3:0	STDERRLOG_HDR_OPCODE	Opcode of the logged packet. Type: Status. Reset value: X.	R	0x0

Table 13-75. Register Call Summary for Register L3_HOST_STDERRLOG_HDR

L3 Interconnect

- L3 Host Register Summary and Description: [0]

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Table 13-76. L3_HOST_STDERRLOG_MSTADDR

Address Offset	See Table 13-61.		
Physical Address	0x4400 0050 0x4480 0050 0x4500 0050	**Instance**	CLK1_HOST_CLK1 CLK2_HOST_CLK2 CLK3_HOST_CLK3
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								STDERRLOG_MSTADDR							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED		R	0x000000
7:0	STDERRLOG_MSTADDR	Master Address field of the logged packet. Type: Status. Reset value: X.	R	0x00

Table 13-77. Register Call Summary for Register L3_HOST_STDERRLOG_MSTADDR

L3 Interconnect

- L3 Host Register Summary and Description: [0]

Table 13-78. L3_HOST_STDERRLOG_SLVADDR

Address Offset	See Table 13-61.		
Physical Address	0x4400 0054 0x4480 0054 0x4500 0054	**Instance**	CLK1_HOST_CLK1 CLK2_HOST_CLK2 CLK3_HOST_CLK3
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																											STDERRLOG_SLVADDR				

Bits	Field Name	Description	Type	Reset
31:5	RESERVED		R	0x0000000
4:0	STDERRLOG_SLVADDR	Slave Address field of the logged packet. Type: Status. Reset value: X.	R	0x00

Table 13-79. Register Call Summary for Register L3_HOST_STDERRLOG_SLVADDR

L3 Interconnect

- L3 Host Register Summary and Description: [0]

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Table 13-80. L3_HOST_STDERRLOG_INFO

Address Offset	See Table 13-61.		
Physical Address	0x4400 0058 0x4480 0058 0x4500 0058	**Instance**	CLK1_HOST_CLK1 CLK2_HOST_CLK2 CLK3_HOST_CLK3
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								STDERRLOG_INFO							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED		R	0x000000
7:0	STDERRLOG_INFO	Info field of the logged packet. Type: Status. Reset value: X.	R	0x00

Table 13-81. Register Call Summary for Register L3_HOST_STDERRLOG_INFO

L3 Interconnect

- L3 Host Register Summary and Description: [0]

Table 13-82. L3_HOST_STDERRLOG_SLVOFSLSB

Address Offset	See Table 13-61.		
Physical Address	0x4400 005C 0x4480 005C 0x4500 005C	**Instance**	CLK1_HOST_CLK1 CLK2_HOST_CLK2 CLK3_HOST_CLK3
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STDERRLOG_SLVOFSLSB																															

Bits	Field Name	Description	Type	Reset
31:0	STDERRLOG_SLVOFSLSB	LSB of the slave offset field, concatenated with start offset field of the logged packet. Type: Status. Reset value: X.	R	0x0000 0000

Table 13-83. Register Call Summary for Register L3_HOST_STDERRLOG_SLVOFSLSB

L3 Interconnect

- L3 Host Register Summary and Description: [0]

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Table 13-84. L3_HOST_STDERRLOG_SLVOFSMSB

Address Offset	See Table 13-61.		
Physical Address	0x4400 0060 0x4480 0060 0x4500 0060	**Instance**	CLK1_HOST_CLK1 CLK2_HOST_CLK2 CLK3_HOST_CLK3
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															STDERRLOG_SLVOFSMSB

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	STDERRLOG_SLVOFSMSB	MSB of the slave offset field of the logged packet (according to NTTP packet format, this register field may exceed the actual slave offset size. Unused bits are stuck at 0, if any). Type: Status. Reset value: X.	R	0

Table 13-85. Register Call Summary for Register L3_HOST_STDERRLOG_SLVOFSMSB

L3 Interconnect

- L3 Host Register Summary and Description: [0]

Table 13-86. L3_HOST_STDERRLOG_CUSTOMINFO_MSTADDR

Address Offset	See Table 13-61.		
Physical Address	0x4400 0064 0x4480 0064 0x4500 0064	**Instance**	CLK1_HOST_CLK1 CLK2_HOST_CLK2 CLK3_HOST_CLK3
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								STDERRLOG_CUSTOMINFO_MSTADDR							

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Bits	Field Name	Description	Type	Reset
31:8	RESERVED		R	0x000000
7:0	STDERRLOG_CUSTOMINFO_MSTADDR	Type: Status. Reset value: X.	R	0x00

Table 13-87. Register Call Summary for Register L3_HOST_STDERRLOG_CUSTOMINFO_MSTADDR

L3 Interconnect

- L3 Host Register Summary and Description: [0]

Table 13-88. L3_HOST_STDERRLOG_CUSTOMINFO_INFO

Address Offset	See Table 13-61.		
Physical Address	0x4400 0068 0x4480 0068 0x4500 0068	**Instance**	CLK1_HOST_CLK1 CLK2_HOST_CLK2 CLK3_HOST_CLK3
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								STDERRLOG_CUSTOMINFO_INFO							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED		R	0x000000
7:0	STDERRLOG_CUSTOMINFO_INFO	Type: Status. Reset value: X.	R	0x00

Table 13-89. Register Call Summary for Register L3_HOST_STDERRLOG_CUSTOMINFO_INFO

L3 Interconnect

- L3 Host Register Summary and Description: [0]

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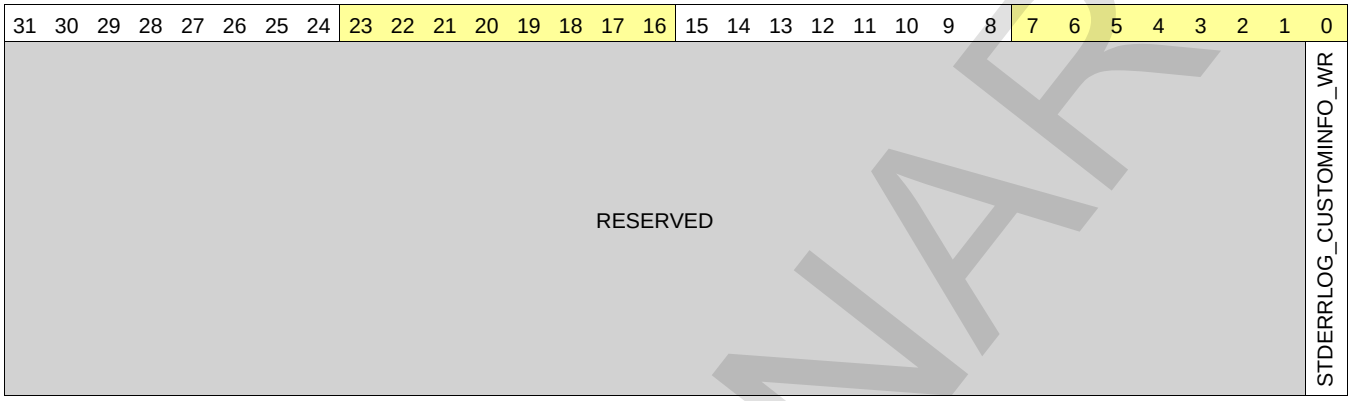
Table 13-90. L3_HOST_STDERRLOG_CUSTOMINFO_WR

Address Offset	See Table 13-61.		
Physical Address	0x4400 006C 0x4480 006C 0x4500 006C	**Instance**	CLK1_HOST_CLK1 CLK2_HOST_CLK2 CLK3_HOST_CLK3
Description			
Type	R		



Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	STDERRLOG_CUSTOMINFO_WR	Type: Status. Reset value: X.	R	0

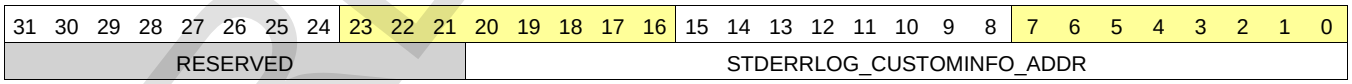
Table 13-91. Register Call Summary for Register L3_HOST_STDERRLOG_CUSTOMINFO_WR

L3 Interconnect

- L3 Host Register Summary and Description: [0]

Table 13-92. L3_HOST_STDERRLOG_CUSTOMINFO_ADDR

Address Offset	See Table 13-61.		
Physical Address	0x4400 0070 0x4480 0070 0x4500 0070	**Instance**	CLK1_HOST_CLK1 CLK2_HOST_CLK2 CLK3_HOST_CLK3
Description			
Type	R		



Bits	Field Name	Description	Type	Reset
31:21	RESERVED		R	0x000
20:0	STDERRLOG_CUSTOMINFO_ADDR	Type: Status. Reset value: X.	R	0x000000

Table 13-93. Register Call Summary for Register L3_HOST_STDERRLOG_CUSTOMINFO_ADDR

L3 Interconnect

- L3 Host Register Summary and Description: [0]

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Table 13-94. L3_HOST_STDERRLOG_CUSTOMINFO_DECERR

Address Offset	See Table 13-61.		
Physical Address	0x4400 0074 0x4480 0074 0x4500 0074	**Instance**	CLK1_HOST_CLK1 CLK2_HOST_CLK2 CLK3_HOST_CLK3
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															STDERRLOG_CUSTOMINFO_DECERR

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	STDERRLOG_CUSTOMINFO_DECERR	Type: Status. Reset value: X.	R	0

Table 13-95. Register Call Summary for Register L3_HOST_STDERRLOG_CUSTOMINFO_DECERR

L3 Interconnect

- L3 Host Register Summary and Description: [0]

13.2.5.1.3 L3 TARG Register Summary and Description

Table 13-96. TARG Instance Summary

Module Name	Base Address	Size
CLK1_DMM1_TARG	0x4400 0100	4KB
CLK1_DMM2_TARG	0x4400 0200	4KB
CLK1_ABE_TARG	0x4400 0300	4KB
CLK1_L4CFG_TARG	0x4400 0400	4KB
CLK2_GPMC_TARG	0x4480 0100	4KB
CLK2_OCMRAM_TARG	0x4480 0200	4KB
CLK2_DSS_TARG	0x4480 0300	4KB
CLK2_ISS_TARG	0x4480 0400	4KB
CLK2_CORTEXM3_TARG	0x4480 0500	4KB
CLK2_SGX_TARG	0x4480 0600	4KB
CLK2_IVAHD_TARG	0x4480 0700	4KB
CLK2_SL2_TARG	0x4480 0800	4KB
CLK2_L4PER0_TARG	0x4480 0900	4KB
CLK2_L4PER1_TARG	0x4480 0A00	4KB

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Table 13-96. TARG Instance Summary (continued)

Module Name	Base Address	Size
CLK2_L4PER2_TARG	0x4480 0B00	4KB
CLK2_L4PER3_TARG	0x4480 0C00	4KB
CLK2_C2C_TARG	0x4480 1600	4KB
CLK3_L4EMU_TARG	0x4500 0100	4KB

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13.2.5.1.3.1 L3 TARG Registers Summary

Table 13-97. TARG Registers Summary

Register Name	Type	Register Width (Bits)	Address Offset for CLK1_DMM1	CLK1_DMM1_TARG L3 Physical Address	Address Offset for CLK1_DMM2	CLK1_DMM2_TARG L3 Physical Address	Address Offset for CLK1_ABE	CLK1_ABE_TARG L3 Physical Address
L3_TARG_STDHOSTHDR_COREREG	R	32	0x0000 0100	0x4400 0100	0x0000 0200	0x4400 0200	0x0000 0300	0x4400 0300
L3_TARG_STDHOSTHDR_VERSIONREG	R	32	0x0000 0104	0x4400 0104	0x0000 0204	0x4400 0204	0x0000 0304	0x4400 0304
L3_TARG_STDHOSTHDR_MAINCTLREG	RW	32	0x0000 0108	0x4400 0108	0x0000 0208	0x4400 0208	0x0000 0308	0x4400 0308
L3_TARG_STDHOSTHDR_NTTPADDR_0	R	32	0x0000 0110	0x4400 0110	0x0000 0210	0x4400 0210	0x0000 0310	0x4400 0310
L3_TARG_STDERRLOG_SVRTSTDLVL	RW	32	0x0000 0140	0x4400 0140	0x0000 0240	0x4400 0240	0x0000 0340	0x4400 0340
L3_TARG_STDERRLOG_SVRTCUSTOMLVL	RW	32	0x0000 0144	0x4400 0144	0x0000 0244	0x4400 0244	0x0000 0344	0x4400 0344
L3_TARG_STDERRLOG_MAIN	RW	32	0x0000 0148	0x4400 0148	0x0000 0248	0x4400 0248	0x0000 0348	0x4400 0348
L3_TARG_STDERRLOG_HDR	R	32	0x0000 014C	0x4400 014C	0x0000 024C	0x4400 024C	0x0000 034C	0x4400 034C
L3_TARG_STDERRLOG_MSTADDR	R	32	0x0000 0150	0x4400 0150	0x0000 0250	0x4400 0250	0x0000 0350	0x4400 0350
L3_TARG_STDERRLOG_SLVADDR	R	32	0x0000 0154	0x4400 0154	0x0000 0254	0x4400 0254	0x0000 0354	0x4400 0354
L3_TARG_STDERRLOG_INFO	R	32	0x0000 0158	0x4400 0158	0x0000 0258	0x4400 0258	0x0000 0358	0x4400 0358
L3_TARG_STDERRLOG_SLVOFSLSB	R	32	0x0000 015C	0x4400 015C	0x0000 025C	0x4400 025C	0x0000 035C	0x4400 035C
L3_TARG_STDERRLOG_SLVOFSMSB	R	32	0x0000 0160	0x4400 0160	0x0000 0260	0x4400 0260	0x0000 0360	0x4400 0360
L3_TARG_STDERRLOG_CUSTOMINFO_INFO	R	32	0x0000 0164	0x4400 0164	0x0000 0264	0x4400 0264	0x0000 0364	0x4400 0364
L3_TARG_STDERRLOG_CUSTOMINFO_MSTADDR	R	32	0x0000 0168	0x4400 0168	0x0000 0268	0x4400 0268	0x0000 0368	0x4400 0368
L3_TARG_STDERRLOG_CUSTOMINFO_OPCODE	R	32	0x0000 016C	0x4400 016C	0x0000 026C	0x4400 026C	0x0000 036C	0x4400 036C
L3_TARG_ADDRSPACESIZELOG	RW	32	0x0000 0180	0x4400 0180	0x0000 0280	0x4400 0280	0x0000 0380	0x4400 0380

Table 13-98. TARG Registers Summary

Register Name	Type	Register Width (Bits)	Address Offset for CLK1_L4CFG	CLK1_L4CFG_TARG L3 Physical Address	Address Offset for CLK2_GPMC	CLK2_GPMC_TARG L3 Physical Address	Address Offset for CLK2_OCMRAM	CLK2_OCMRAM_TARG L3 Physical Address
L3_TARG_STDHOSTHDR_COREREG	R	32	0x0000 0400	0x4400 0400	0x0080 0100	0x4480 0100	0x0080 0200	0x4480 0200
L3_TARG_STDHOSTHDR_VERSIONREG	R	32	0x0000 0404	0x4400 0404	0x0080 0104	0x4480 0104	0x0080 0204	0x4480 0204
L3_TARG_STDHOSTHDR_MAINCTLREG	RW	32	0x0000 0408	0x4400 0408	0x0080 0108	0x4480 0108	0x0080 0208	0x4480 0208
L3_TARG_STDHOSTHDR_NTTPADDR_0	R	32	0x0000 0410	0x4400 0410	0x0080 0110	0x4480 0110	0x0080 0210	0x4480 0210
L3_TARG_STDERRLOG_SVRTSTDLVL	RW	32	0x0000 0440	0x4400 0440	0x0080 0140	0x4480 0140	0x0080 0240	0x4480 0240
L3_TARG_STDERRLOG_SVRTCUSTOMLVL	RW	32	0x0000 0444	0x4400 0444	0x0080 0144	0x4480 0144	0x0080 0244	0x4480 0244

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Table 13-98. TARG Registers Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset for CLK1_L4CFG	CLK1_L4CFG_TARG L3 Physical Address	Address Offset for CLK2_GPMC	CLK2_GPMC_TARG L3 Physical Address	Address Offset for CLK2_OCMRAM	CLK2_OCMRAM_TARG L3 Physical Address
L3_TARG_STDERRLOG_MAIN	RW	32	0x0000 0448	0x4400 0448	0x0080 0148	0x4480 0148	0x0080 0248	0x4480 0248
L3_TARG_STDERRLOG_HDR	R	32	0x0000 044C	0x4400 044C	0x0080 014C	0x4480 014C	0x0080 024C	0x4480 024C
L3_TARG_STDERRLOG_MSTADDR	R	32	0x0000 0450	0x4400 0450	0x0080 0150	0x4480 0150	0x0080 0250	0x4480 0250
L3_TARG_STDERRLOG_SLVADDR	R	32	0x0000 0454	0x4400 0454	0x0080 0154	0x4480 0154	0x0080 0254	0x4480 0254
L3_TARG_STDERRLOG_INFO	R	32	0x0000 0458	0x4400 0458	0x0080 0158	0x4480 0158	0x0080 0258	0x4480 0258
L3_TARG_STDERRLOG_SLVOFSLSB	R	32	0x0000 045C	0x4400 045C	0x0080 015C	0x4480 015C	0x0080 025C	0x4480 025C
L3_TARG_STDERRLOG_SLVOFSMSB	R	32	0x0000 0460	0x4400 0460	0x0080 0160	0x4480 0160	0x0080 0260	0x4480 0260
L3_TARG_STDERRLOG_CUSTOMINFO_INFO	R	32	0x0000 0464	0x4400 0464	0x0080 0164	0x4480 0164	0x0080 0264	0x4480 0264
L3_TARG_STDERRLOG_CUSTOMINFO_MSTADDR	R	32	0x0000 0468	0x4400 0468	0x0080 0168	0x4480 0168	0x0080 0268	0x4480 0268
L3_TARG_STDERRLOG_CUSTOMINFO_OPCODE	R	32	0x0000 046C	0x4400 046C	0x0080 016C	0x4480 016C	0x0080 026C	0x4480 026C
L3_TARG_ADDRSPACESIZELOG	RW	32	0x0000 0480	0x4400 0480	0x0080 0180	0x4480 0180	0x0080 0280	0x4480 0280

Table 13-99. TARG Registers Summary

Register Name	Type	Register Width (Bits)	Address Offset for CLK2_DSS	CLK2_DSS_TARG L3 Physical Address	Address Offset for CLK2_ISS	CLK2_ISS_TARG L3 Physical Address	Address Offset for CLK2_CORTEXM3	CLK2_CORTEXM3_TARG L3 Physical Address
L3_TARG_STDHOSTHDR_COREREG	R	32	0x0080 0300	0x4480 0300	0x0080 0400	0x4480 0400	0x0080 0500	0x4480 0500
L3_TARG_STDHOSTHDR_VERSIONREG	R	32	0x0080 0304	0x4480 0304	0x0080 0404	0x4480 0404	0x0080 0504	0x4480 0504
L3_TARG_STDHOSTHDR_MAINCTLREG	RW	32	0x0080 0308	0x4480 0308	0x0080 0408	0x4480 0408	0x0080 0508	0x4480 0508
L3_TARG_STDHOSTHDR_NTTPADDR_0	R	32	0x0080 0310	0x4480 0310	0x0080 0410	0x4480 0410	0x0080 0510	0x4480 0510
L3_TARG_STDERRLOG_SVRTSTDLVL	RW	32	0x0080 0340	0x4480 0340	0x0080 0440	0x4480 0440	0x0080 0540	0x4480 0540
L3_TARG_STDERRLOG_SVRTCUSTOMLVL	RW	32	0x0080 0344	0x4480 0344	0x0080 0444	0x4480 0444	0x0080 0544	0x4480 0544
L3_TARG_STDERRLOG_MAIN	RW	32	0x0080 0348	0x4480 0348	0x0080 0448	0x4480 0448	0x0080 0548	0x4480 0548
L3_TARG_STDERRLOG_HDR	R	32	0x0080 034C	0x4480 034C	0x0080 044C	0x4480 044C	0x0080 054C	0x4480 054C
L3_TARG_STDERRLOG_MSTADDR	R	32	0x0080 0350	0x4480 0350	0x0080 0450	0x4480 0450	0x0080 0550	0x4480 0550
L3_TARG_STDERRLOG_SLVADDR	R	32	0x0080 0354	0x4480 0354	0x0080 0454	0x4480 0454	0x0080 0554	0x4480 0554
L3_TARG_STDERRLOG_INFO	R	32	0x0080 0358	0x4480 0358	0x0080 0458	0x4480 0458	0x0080 0558	0x4480 0558
L3_TARG_STDERRLOG_SLVOFSLSB	R	32	0x0080 035C	0x4480 035C	0x0080 045C	0x4480 045C	0x0080 055C	0x4480 055C
L3_TARG_STDERRLOG_SLVOFSMSB	R	32	0x0080 0360	0x4480 0360	0x0080 0460	0x4480 0460	0x0080 0560	0x4480 0560
L3_TARG_STDERRLOG_CUSTOMINFO_INFO	R	32	0x0080 0364	0x4480 0364	0x0080 0464	0x4480 0464	0x0080 0564	0x4480 0564

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Table 13-99. TARG Registers Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset for CLK2_DSS	CLK2_DSS_TARG L3 Physical Address	Address Offset for CLK2_ISS	CLK2_ISS_TARG L3 Physical Address	Address Offset for CLK2_CORTEXM3	CLK2_CORTEXM3_TARG L3 Physical Address
L3_TARG_STDERRLOG_CUSTOMINFO_MSTADDR	R	32	0x0080 0368	0x4480 0368	0x0080 0468	0x4480 0468	0x0080 0568	0x4480 0568
L3_TARG_STDERRLOG_CUSTOMINFO_OPCODE	R	32	0x0080 036C	0x4480 036C	0x0080 046C	0x4480 046C	0x0080 056C	0x4480 056C
L3_TARG_ADDRSPACESIZELOG	RW	32	0x0080 0380	0x4480 0380	0x0080 0480	0x4480 0480	0x0080 0580	0x4480 0580

Table 13-100. TARG Registers Summary

Register Name	Type	Register Width (Bits)	Address Offset for CLK2_SGX	CLK2_SGX_TARG L3 Physical Address	Address Offset for CLK2_IVAHD	CLK2_IVAHD_TARG L3 Physical Address	Address Offset for CLK2_SL2	CLK2_SL2_TARG L3 Physical Address
L3_TARG_STDHOSTHDR_COREREG	R	32	0x0080 0600	0x4480 0600	0x0080 0700	0x4480 0700	0x0080 0800	0x4480 0800
L3_TARG_STDHOSTHDR_VERSIONREG	R	32	0x0080 0604	0x4480 0604	0x0080 0704	0x4480 0704	0x0080 0804	0x4480 0804
L3_TARG_STDHOSTHDR_MAINCTLREG	RW	32	0x0080 0608	0x4480 0608	0x0080 0708	0x4480 0708	0x0080 0808	0x4480 0808
L3_TARG_STDHOSTHDR_NTTPADDR_0	R	32	0x0080 0610	0x4480 0610	0x0080 0710	0x4480 0710	0x0080 0810	0x4480 0810
L3_TARG_STDERRLOG_SVRTSTDLVL	RW	32	0x0080 0640	0x4480 0640	0x0080 0740	0x4480 0740	0x0080 0840	0x4480 0840
L3_TARG_STDERRLOG_SVRTCUSTOMLVL	RW	32	0x0080 0644	0x4480 0644	0x0080 0744	0x4480 0744	0x0080 0844	0x4480 0844
L3_TARG_STDERRLOG_MAIN	RW	32	0x0080 0648	0x4480 0648	0x0080 0748	0x4480 0748	0x0080 0848	0x4480 0848
L3_TARG_STDERRLOG_HDR	R	32	0x0080 064C	0x4480 064C	0x0080 074C	0x4480 074C	0x0080 084C	0x4480 084C
L3_TARG_STDERRLOG_MSTADDR	R	32	0x0080 0650	0x4480 0650	0x0080 0750	0x4480 0750	0x0080 0850	0x4480 0850
L3_TARG_STDERRLOG_SLVADDR	R	32	0x0080 0654	0x4480 0654	0x0080 0754	0x4480 0754	0x0080 0854	0x4480 0854
L3_TARG_STDERRLOG_INFO	R	32	0x0080 0658	0x4480 0658	0x0080 0758	0x4480 0758	0x0080 0858	0x4480 0858
L3_TARG_STDERRLOG_SLVOFSLSB	R	32	0x0080 065C	0x4480 065C	0x0080 075C	0x4480 075C	0x0080 085C	0x4480 085C
L3_TARG_STDERRLOG_SLVOFSMSB	R	32	0x0080 0660	0x4480 0660	0x0080 0760	0x4480 0760	0x0080 0860	0x4480 0860
L3_TARG_STDERRLOG_CUSTOMINFO_INFO	R	32	0x0080 0664	0x4480 0664	0x0080 0764	0x4480 0764	0x0080 0864	0x4480 0864
L3_TARG_STDERRLOG_CUSTOMINFO_MSTADDR	R	32	0x0080 0668	0x4480 0668	0x0080 0768	0x4480 0768	0x0080 0868	0x4480 0868
L3_TARG_STDERRLOG_CUSTOMINFO_OPCODE	R	32	0x0080 066C	0x4480 066C	0x0080 076C	0x4480 076C	0x0080 086C	0x4480 086C
L3_TARG_ADDRSPACESIZELOG	RW	32	0x0080 0680	0x4480 0680	0x0080 0780	0x4480 0780	0x0080 0880	0x4480 0880

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Table 13-101. TARG Registers Summary

Register Name	Type	Register Width (Bits)	Address Offset for CLK2_L4PER 0	CLK2_L4PER 0_TARG L3 Physical Address	Address Offset for CLK2_L4PER1	CLK2_L4PER 1_TARG L3 Physical Address	Address Offset for CLK2_L4PER2	CLK2_L4PER2_ TARG L3 Physical Address
L3_TARG_STDHOSTHDR_COREREG	R	32	0x0080 0900	0x4480 0900	0x0080 0A00	0x4480 0A00	0x0080 0B00	0x4480 0B00
L3_TARG_STDHOSTHDR_VERSIONREG	R	32	0x0080 0904	0x4480 0904	0x0080 0A04	0x4480 0A04	0x0080 0B04	0x4480 0B04
L3_TARG_STDHOSTHDR_MAINCTLREG	RW	32	0x0080 0908	0x4480 0908	0x0080 0A08	0x4480 0A08	0x0080 0B08	0x4480 0B08
L3_TARG_STDHOSTHDR_NTTPADDR_0	R	32	0x0080 0910	0x4480 0910	0x0080 0A10	0x4480 0A10	0x0080 0B10	0x4480 0B10
L3_TARG_STDERRLOG_SVRTSTDLVL	RW	32	0x0080 0940	0x4480 0940	0x0080 0A40	0x4480 0A40	0x0080 0B40	0x4480 0B40
L3_TARG_STDERRLOG_SVRTCUSTOMLVL	RW	32	0x0080 0944	0x4480 0944	0x0080 0A44	0x4480 0A44	0x0080 0B44	0x4480 0B44
L3_TARG_STDERRLOG_MAIN	RW	32	0x0080 0948	0x4480 0948	0x0080 0A48	0x4480 0A48	0x0080 0B48	0x4480 0B48
L3_TARG_STDERRLOG_HDR	R	32	0x0080 094C	0x4480 094C	0x0080 0A4C	0x4480 0A4C	0x0080 0B4C	0x4480 0B4C
L3_TARG_STDERRLOG_MSTADDR	R	32	0x0080 0950	0x4480 0950	0x0080 0A50	0x4480 0A50	0x0080 0B50	0x4480 0B50
L3_TARG_STDERRLOG_SLVADDR	R	32	0x0080 0954	0x4480 0954	0x0080 0A54	0x4480 0A54	0x0080 0B54	0x4480 0B54
L3_TARG_STDERRLOG_INFO	R	32	0x0080 0958	0x4480 0958	0x0080 0A58	0x4480 0A58	0x0080 0B58	0x4480 0B58
L3_TARG_STDERRLOG_SLVOFSLSB	R	32	0x0080 095C	0x4480 095C	0x0080 0A5C	0x4480 0A5C	0x0080 0B5C	0x4480 0B5C
L3_TARG_STDERRLOG_SLVOFSMSB	R	32	0x0080 0960	0x4480 0960	0x0080 0A60	0x4480 0A60	0x0080 0B60	0x4480 0B60
L3_TARG_STDERRLOG_CUSTOMINFO_INFO	R	32	0x0080 0964	0x4480 0964	0x0080 0A64	0x4480 0A64	0x0080 0B64	0x4480 0B64
L3_TARG_STDERRLOG_CUSTOMINFO_MSTADDR	R	32	0x0080 0968	0x4480 0968	0x0080 0A68	0x4480 0A68	0x0080 0B68	0x4480 0B68
L3_TARG_STDERRLOG_CUSTOMINFO_OPCODE	R	32	0x0080 096C	0x4480 096C	0x0080 0A6C	0x4480 0A6C	0x0080 0B6C	0x4480 0B6C
L3_TARG_ADDRSPACESIZELOG	RW	32	0x0080 0980	0x4480 0980	0x0080 0A80	0x4480 0A80	0x0080 0B80	0x4480 0B80

Table 13-102. TARG Registers Summary

Register Name	Type	Register Width (Bits)	Address Offset for CLK2_L4PER3	CLK2_L4PER3_TARG L3 Physical Address
L3_TARG_STDHOSTHDR_COREREG	R	32	0x0080 0C00	0x4480 0C00
L3_TARG_STDHOSTHDR_VERSIONREG	R	32	0x0080 0C04	0x4480 0C04
L3_TARG_STDHOSTHDR_MAINCTLREG	RW	32	0x0080 0C08	0x4480 0C08
L3_TARG_STDHOSTHDR_NTTPADDR_0	R	32	0x0080 0C10	0x4480 0C10
L3_TARG_STDERRLOG_SVRTSTDLVL	RW	32	0x0080 0C40	0x4480 0C40
L3_TARG_STDERRLOG_SVRTCUSTOMLVL	RW	32	0x0080 0C44	0x4480 0C44
L3_TARG_STDERRLOG_MAIN	RW	32	0x0080 0C48	0x4480 0C48
L3_TARG_STDERRLOG_HDR	R	32	0x0080 0C4C	0x4480 0C4C
L3_TARG_STDERRLOG_MSTADDR	R	32	0x0080 0C50	0x4480 0C50
L3_TARG_STDERRLOG_SLVADDR	R	32	0x0080 0C54	0x4480 0C54

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Table 13-102. TARG Registers Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset for CLK2_L4PER3	CLK2_L4PER3_TARG L3 Physical Address
L3_TARG_STDERRLOG_INFO	R	32	0x0080 0C58	0x4480 0C58
L3_TARG_STDERRLOG_SLVOFSLSB	R	32	0x0080 0C5C	0x4480 0C5C
L3_TARG_STDERRLOG_SLVOFSMSB	R	32	0x0080 0C60	0x4480 0C60
L3_TARG_STDERRLOG_CUSTOMINFO_INFO	R	32	0x0080 0C64	0x4480 0C64
L3_TARG_STDERRLOG_CUSTOMINFO_MSTADDR	R	32	0x0080 0C68	0x4480 0C68
L3_TARG_STDERRLOG_CUSTOMINFO_OPCODE	R	32	0x0080 0C6C	0x4480 0C6C
L3_TARG_ADDRSPACESIZELOG	RW	32	0x0080 0C80	0x4480 0C80

Table 13-103. TARG Registers Summary

Register Name	Type	Register Width (Bits)	Address Offset for CLK2_C2C	CLK2_C2C_TARG L3 Physical Address	Address Offset for CLK2_L4EMU	CLK3_L4EMU_TARG L3 Physical Address
L3_TARG_STDHOSTHDR_COREREG	R	32	0x0080 1600	0x4480 1600	0x0100 0100	0x4500 0100
L3_TARG_STDHOSTHDR_VERSIONREG	R	32	0x0080 1604	0x4480 1604	0x0100 0104	0x4500 0104
L3_TARG_STDHOSTHDR_MAINCTLREG	RW	32	0x0080 1608	0x4480 1608	0x0100 0108	0x4500 0108
L3_TARG_STDHOSTHDR_NTTPADDR_0	R	32	0x0080 1610	0x4480 1610	0x0100 0110	0x4500 0110
L3_TARG_STDERRLOG_SVRTSTDLVL	RW	32	0x0080 1640	0x4480 1640	0x0100 0140	0x4500 0140
L3_TARG_STDERRLOG_SVRTCUSTOMLVL	RW	32	0x0080 1644	0x4480 1644	0x0100 0144	0x4500 0144
L3_TARG_STDERRLOG_MAIN	RW	32	0x0080 1648	0x4480 1648	0x0100 0148	0x4500 0148
L3_TARG_STDERRLOG_HDR	R	32	0x0080 164C	0x4480 164C	0x0100 014C	0x4500 014C
L3_TARG_STDERRLOG_MSTADDR	R	32	0x0080 1650	0x4480 1650	0x0100 0150	0x4500 0150
L3_TARG_STDERRLOG_SLVADDR	R	32	0x0080 1654	0x4480 1654	0x0100 0154	0x4500 0154
L3_TARG_STDERRLOG_INFO	R	32	0x0080 1658	0x4480 1658	0x0100 0158	0x4500 0158
L3_TARG_STDERRLOG_SLVOFSLSB	R	32	0x0080 165C	0x4480 165C	0x0100 015C	0x4500 015C
L3_TARG_STDERRLOG_SLVOFSMSB	R	32	0x0080 1660	0x4480 1660	0x0100 0160	0x4500 0160
L3_TARG_STDERRLOG_CUSTOMINFO_INFO	R	32	0x0080 1664	0x4480 1664	0x0100 0164	0x4500 0164
L3_TARG_STDERRLOG_CUSTOMINFO_MSTADDR	R	32	0x0080 1668	0x4480 1668	0x0100 0168	0x4500 0168
L3_TARG_STDERRLOG_CUSTOMINFO_OPCODE	R	32	0x0080 166C	0x4480 166C	0x0100 016C	0x4500 016C
L3_TARG_ADDRSPACESIZELOG	RW	32	0x0080 1680	0x4480 1680	0x0100 0180	0x4500 0180

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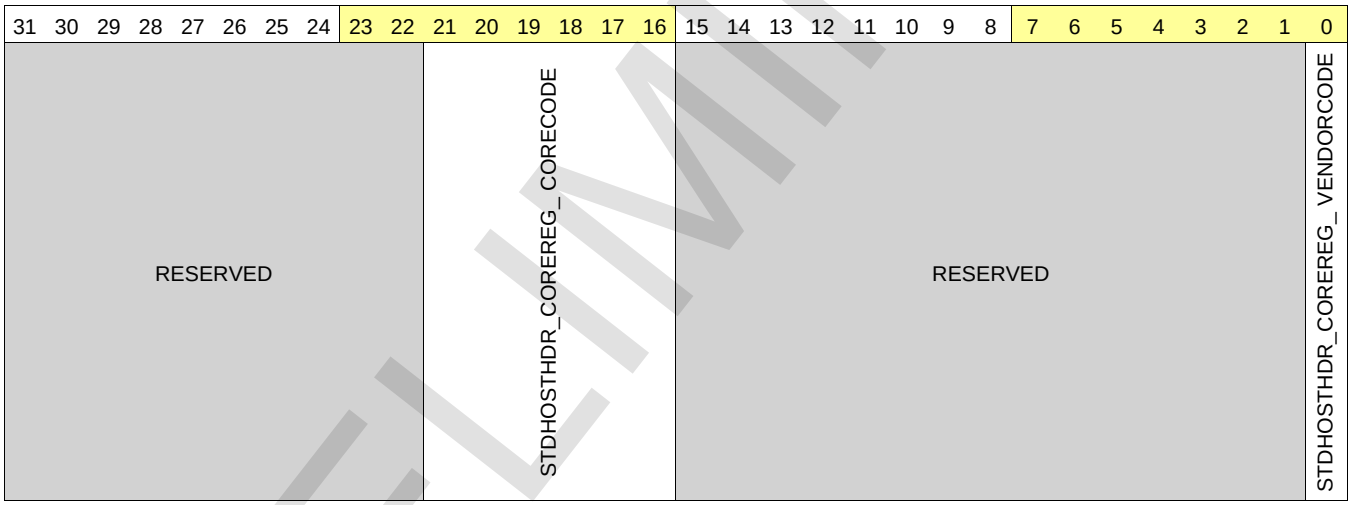
13.2.5.1.3.2 L3 TARG Registers Description

Table 13-104. L3_TARG_STDHOSTHDR_COREREG

Address Offset	See Table 13-97.		
Physical Address	0x4400 0100	**Instance**	CLK1_DMM1_TARG
	0x4400 0200		CLK1_DMM2_TARG
	0x4400 0300		CLK1_ABE_TARG
	0x4400 0400		CLK1_L4CFG_TARG
	0x4480 0100		CLK2_GPMC_TARG
	0x4480 0200		CLK2_OCMRAM_TARG
	0x4480 0300		CLK2_DSS_TARG
	0x4480 0400		CLK2_ISS_TARG
	0x4480 0500		CLK2_CORTEXM3_TARG
	0x4480 0600		CLK2_SGX_TARG
	0x4480 0700		CLK2_IVAHD_TARG
	0x4480 0800		CLK2_SL2_TARG
	0x4480 0900		CLK2_L4PER0_TARG
	0x4480 0A00		CLK2_L4PER1_TARG
	0x4480 0B00		CLK2_L4PER2_TARG
	0x4480 0C00		CLK2_L4PER3_TARG
	0x4480 1600		CLK2_C2C_TARG
	0x4500 0100		CLK3_L4EMU_TARG
Description			
Type	R		



Bits	Field Name	Description	Type	Reset
31:22	RESERVED		R	0x000
21:16	STDHOSTHDR_COREREG_ CORECODE	The Core Code field is a constant reporting a vendor-specific core generator code. Type: Constant. Reset value: 0x13.	R	0x13
15:1	RESERVED		R	0x0000
0	STDHOSTHDR_COREREG_ VENDORCODE	The Vendor Code field is a constant reporting the core generator vendor code. Type: Constant. Reset value: 0x1. Read 0x0: Third-party vendor. Read 0x1:	R	1

Table 13-105. Register Call Summary for Register L3_TARG_STDHOSTHDR_COREREG

L3 Interconnect

- L3 TARG Register Summary and Description: [0] [1] [2] [3] [4] [5] [6]

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Table 13-106. L3_TARG_STDHOSTHDR_VERSIONREG

Address Offset	See Table 13-97.		
Physical Address	0x4400 0104	**Instance**	CLK1_DMM1_TARG
	0x4400 0204		CLK1_DMM2_TARG
	0x4400 0304		CLK1_ABE_TARG
	0x4400 0404		CLK1_L4CFG_TARG
	0x4480 0104		CLK2_GPMC_TARG
	0x4480 0204		CLK2_OCMRAM_TARG
	0x4480 0304		CLK2_DSS_TARG
	0x4480 0404		CLK2_ISS_TARG
	0x4480 0504		CLK2_CORTEXM3_TARG
	0x4480 0604		CLK2_SGX_TARG
	0x4480 0704		CLK2_IVAHD_TARG
	0x4480 0804		CLK2_SL2_TARG
	0x4480 0904		CLK2_L4PER0_TARG
	0x4480 0A04		CLK2_L4PER1_TARG
	0x4480 0B04		CLK2_L4PER2_TARG
	0x4480 0C04		CLK2_L4PER3_TARG
	0x4480 1604		CLK2_C2C_TARG
	0x4500 0104		CLK3_L4EMU_TARG
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STDHOSTHDR_VERSIONREG_REVISIONID								STDHOSTHDR_VERSIONREG_COREPARAMSCHECKSUM																							

Bits	Field Name	Description	Type	Reset
31:24	STDHOSTHDR_VERSIONREG_REVISIONID	The Revision Identifier field is a constant reporting the core generator revision number. Type: Constant. Reset value: 0x0.	R	0x00
23:0	STDHOSTHDR_VERSIONREG_COREPARAMSCHECKSUM	Reserved. Type: Reserved. Reset value: Reserved.	R	0x000000

Table 13-107. Register Call Summary for Register L3_TARG_STDHOSTHDR_VERSIONREG

L3 Interconnect

- L3 TARG Register Summary and Description: [0] [1] [2] [3] [4] [5] [6]

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Table 13-108. L3_TARG_STDHOSTHDR_MAINCTLREG

Address Offset	See Table 13-97.		
Physical Address	0x4400 0108	**Instance**	CLK1_DMM1_TARG
	0x4400 0208		CLK1_DMM2_TARG
	0x4400 0308		CLK1_ABE_TARG
	0x4400 0408		CLK1_L4CFG_TARG
	0x4480 0108		CLK2_GPMC_TARG
	0x4480 0208		CLK2_OCMRAM_TARG
	0x4480 0308		CLK2_DSS_TARG
	0x4480 0408		CLK2_ISS_TARG
	0x4480 0508		CLK2_CORTEXM3_TARG
	0x4480 0608		CLK2_SGX_TARG
	0x4480 0708		CLK2_IVAHD_TARG
	0x4480 0808		CLK2_SL2_TARG
	0x4480 0908		CLK2_L4PER0_TARG
	0x4480 0A08		CLK2_L4PER1_TARG
	0x4480 0B08		CLK2_L4PER2_TARG
	0x4480 0C08		CLK2_L4PER3_TARG
	0x4480 1608		CLK2_C2C_TARG
	0x4500 0108		CLK3_L4EMU_TARG
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																											RESERVED	STDHOSTHDR_MAINCTLREG_CM	STDHOSTHDR_MAINCTLREG_FLT	RESERVED	STDHOSTHDR_MAINCTLREG_EN

Bits	Field Name	Description	Type	Reset
31:5	RESERVED	Reserved	R	0x0000000
4	RESERVED	Reserved	R	0
3	STDHOSTHDR_MAINCTLREG_CM	Reserved for internal testing. Must be set to 0. Type: Control. Reset value: 0x0.	R	0
2	STDHOSTHDR_MAINCTLREG_FLT	Asserted when a Fault condition is detected: if the unit includes Error Logging, Flt is asserted when the FltCnt register field indicates a Fault, and deasserted when FltCnt is reset. If no Error Logging is implemented, this bit becomes unit-dependent. In all cases, Flt bit and Flt pin (service network) have the same logical level. Type: Status. Reset value: X.	R	0
1	RESERVED	Reserved	R	0
0	STDHOSTHDR_MAINCTLREG_EN	Sets the global core enable. Note: A disabled master does not generate any NTTP requests, and a disabled slave replies with an error packet to any request it receives. Type: Control. Reset value: 0x1.	RW	1

Table 13-109. Register Call Summary for Register L3_TARG_STDHOSTHDR_MAINCTLREG

L3 Interconnect

- L3 TARG Register Summary and Description: [0] [1] [2] [3] [4] [5] [6]

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Table 13-110. L3_TARG_STDHOSTHDR_NTTPADDR_0

Address Offset	See Table 13-97.		
Physical Address	0x4400 0110	**Instance**	CLK1_DMM1_TARG
	0x4400 0210		CLK1_DMM2_TARG
	0x4400 0310		CLK1_ABE_TARG
	0x4400 0410		CLK1_L4CFG_TARG
	0x4480 0110		CLK2_GPMC_TARG
	0x4480 0210		CLK2_OCMRAM_TARG
	0x4480 0310		CLK2_DSS_TARG
	0x4480 0410		CLK2_ISS_TARG
	0x4480 0510		CLK2_CORTEXM3_TARG
	0x4480 0610		CLK2_SGX_TARG
	0x4480 0710		CLK2_IVAHD_TARG
	0x4480 0810		CLK2_SL2_TARG
	0x4480 0910		CLK2_L4PER0_TARG
	0x4480 0A10		CLK2_L4PER1_TARG
	0x4480 0B10		CLK2_L4PER2_TARG
	0x4480 0C10		CLK2_L4PER3_TARG
	0x4480 1610		CLK2_C2C_TARG
	0x4500 0110		CLK3_L4EMU_TARG
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								STDHOSTHDR_NTTPADDR_0							

Bits	Field Name	Description	Type	Reset
31:5	RESERVED	Reserved	R	0x0000000
4:0	STDHOSTHDR_NTTPADDR_0	Sets the RX port address. Type: Control. Reset value: 0x15.	R	0x15

Table 13-111. Register Call Summary for Register L3_TARG_STDHOSTHDR_NTTPADDR_0

L3 Interconnect

- L3 TARG Register Summary and Description: [0] [1] [2] [3] [4] [5] [6]

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Table 13-112. L3_TARG_STDERRLOG_SVRTSTDLVL

Address Offset	See Table 13-97.		
Physical Address	0x4400 0140	**Instance**	CLK1_DMM1_TARG
	0x4400 0240		CLK1_DMM2_TARG
	0x4400 0340		CLK1_ABE_TARG
	0x4400 0440		CLK1_L4CFG_TARG
	0x4480 0140		CLK2_GPMC_TARG
	0x4480 0240		CLK2_OCMRAM_TARG
	0x4480 0340		CLK2_DSS_TARG
	0x4480 0440		CLK2_ISS_TARG
	0x4480 0540		CLK2_CORTEXM3_TARG
	0x4480 0640		CLK2_SGX_TARG
	0x4480 0740		CLK2_IVAHD_TARG
	0x4480 0840		CLK2_SL2_TARG
	0x4480 0940		CLK2_L4PER0_TARG
	0x4480 0A40		CLK2_L4PER1_TARG
	0x4480 0B40		CLK2_L4PER2_TARG
	0x4480 0C40		CLK2_L4PER3_TARG
	0x4480 1640		CLK2_C2C_TARG
	0x4500 0140		CLK3_L4EMU_TARG
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														STDERRLOG_SVRTSTDLVL_0	

Bits	Field Name	Description	Type	Reset
31:2	RESERVED	Reserved	R	0x0000 0000
1:0	STDERRLOG_SVRTSTDLVL_0	Severity level parameters Type: Control. Reset value: 0x2. 0x0: Error logging is disabled. 0x1: Errors are logged with severity level Error. 0x2: Errors are logged with severity level Fault.	RW	0x2

Table 13-113. Register Call Summary for Register L3_TARG_STDERRLOG_SVRTSTDLVL

L3 Interconnect

- Severity Level of Standard and Custom Errors: [0]
- L3 Interconnect Error Analysis Mode: [1]
- L3 TARG Register Summary and Description: [2] [3] [4] [5] [6] [7] [8]

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Table 13-114. L3_TARG_STDERRLOG_SVRTCUSTOMLVL

Address Offset	See Table 13-97.		
Physical Address	0x4400 0144	**Instance**	CLK1_DMM1_TARG
	0x4400 0244		CLK1_DMM2_TARG
	0x4400 0344		CLK1_ABE_TARG
	0x4400 0444		CLK1_L4CFG_TARG
	0x4480 0144		CLK2_GPMC_TARG
	0x4480 0244		CLK2_OCMRAM_TARG
	0x4480 0344		CLK2_DSS_TARG
	0x4480 0444		CLK2_ISS_TARG
	0x4480 0544		CLK2_CORTEXM3_TARG
	0x4480 0644		CLK2_SGX_TARG
	0x4480 0744		CLK2_IVAHD_TARG
	0x4480 0844		CLK2_SL2_TARG
	0x4480 0944		CLK2_L4PER0_TARG
	0x4480 0A44		CLK2_L4PER1_TARG
	0x4480 0B44		CLK2_L4PER2_TARG
	0x4480 0C44		CLK2_L4PER3_TARG
	0x4480 1644		CLK2_C2C_TARG
	0x4500 0144		CLK3_L4EMU_TARG
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														STDERRLOG_SVRTCUSTOMLVL_0	

Bits	Field Name	Description	Type	Reset
31:2	RESERVED	Reserved	R	0x0000 0000
1:0	STDERRLOG_SVRTCUSTOMLVL_0	Severity level parameters Type: Control. Reset value: 0x2. 0x0: Error logging is disabled. 0x1: Errors are logged with severity level Error. 0x2: Errors are logged with severity level Fault.	RW	0x2

Table 13-115. Register Call Summary for Register L3_TARG_STDERRLOG_SVRTCUSTOMLVL

L3 Interconnect

- Severity Level of Standard and Custom Errors: [0]
- L3 TARG Register Summary and Description: [1] [2] [3] [4] [5] [6] [7]

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Table 13-116. L3_TARG_STDERRLOG_MAIN

Address Offset	See Table 13-97.		
Physical Address	0x4400 0148	**Instance**	CLK1_DMM1_TARG
	0x4400 0248		CLK1_DMM2_TARG
	0x4400 0348		CLK1_ABE_TARG
	0x4400 0448		CLK1_L4CFG_TARG
	0x4480 0148		CLK2_GPMC_TARG
	0x4480 0248		CLK2_OCMRAM_TARG
	0x4480 0348		CLK2_DSS_TARG
	0x4480 0448		CLK2_ISS_TARG
	0x4480 0548		CLK2_CORTEXM3_TARG
	0x4480 0648		CLK2_SGX_TARG
	0x4480 0748		CLK2_IVAHD_TARG
	0x4480 0848		CLK2_SL2_TARG
	0x4480 0948		CLK2_L4PER0_TARG
	0x4480 0A48		CLK2_L4PER1_TARG
	0x4480 0B48		CLK2_L4PER2_TARG
	0x4480 0C48		CLK2_L4PER3_TARG
	0x4480 1648		CLK2_C2C_TARG
	0x4500 0148		CLK3_L4EMU_TARG
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STDERRLOG_MAIN_CLRLOG	RESERVED											STDERRLOG_MAIN_FLTCNT	STDERRLOG_MAIN_ERRCNT	RESERVED																	STDERRLOG_MAIN_ERRTYPE	STDERRLOG_MAIN_ERRLOGVLD	

Bits	Field Name	Description	Type	Reset
31	STDERRLOG_MAIN_CLRLOG	Clears Error Logging Valid bit when written to 1. Type: Give_AutoCleared. Reset value: 0x0.	RW	0
30:20	RESERVED	Reserved	R	0x000
19	STDERRLOG_MAIN_FLTCNT	Asserted when at least one error with severity level FAULT is detected. Reset when written to 1. Type: Take. Reset value: 0x0.	RW	0
18	STDERRLOG_MAIN_ERRCNT	Asserted when at least one error with severity level ERROR is detected. Reset when written to 1. Type: Take. Reset value: 0x0.	RW	0
17:2	RESERVED	Reserved	R	0x0000
1	STDERRLOG_MAIN_ERRTYPE	Indicates logging type. Type: Status. Reset value: X. Read 0x0: Logged Error format is standard (header and necker recorded). Read 0x1: Logged Error format is module dependent. CustomInfo register(s) may be implemented to store additional information.	R	0
0	STDERRLOG_MAIN_ERRLOGVLD	Error Logging Valid. Asserted when logging information is valid(indicates that an error has been logged). Type: Status. Reset value: X.	R	0

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Table 13-117. Register Call Summary for Register L3_TARG_STDERRLOG_MAIN

L3 Interconnect

- Severity Level of Standard and Custom Errors: [0]
- L3 Interconnect Error Analysis Mode: [1] [2] [3] [4] [5] [6]
- L3 TARG Register Summary and Description: [7] [8] [9] [10] [11] [12] [13]

Table 13-118. L3_TARG_STDERRLOG_HDR

Address Offset	See Table 13-97.		
Physical Address	0x4400 014C	**Instance**	CLK1_DMM1_TARG
	0x4400 024C		CLK1_DMM2_TARG
	0x4400 034C		CLK1_ABE_TARG
	0x4400 044C		CLK1_L4CFG_TARG
	0x4480 014C		CLK2_GPMC_TARG
	0x4480 024C		CLK2_OCMRAM_TARG
	0x4480 034C		CLK2_DSS_TARG
	0x4480 044C		CLK2_ISS_TARG
	0x4480 054C		CLK2_CORTEXM3_TARG
	0x4480 064C		CLK2_SGX_TARG
	0x4480 074C		CLK2_IVAHD_TARG
	0x4480 084C		CLK2_SL2_TARG
	0x4480 094C		CLK2_L4PER0_TARG
	0x4480 0A4C		CLK2_L4PER1_TARG
	0x4480 0B4C		CLK2_L4PER2_TARG
	0x4480 0C4C		CLK2_L4PER3_TARG
	0x4480 164C		CLK2_C2C_TARG
	0x4500 014C		CLK3_L4EMU_TARG
Description			
Type	R		

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
RESERVED	STDERRLOG_HDR_LEN1	RESERVED	STDERRLOG_HDR_STOPOFSWRPSZ	STDERRLOG_HDR_ERR	RESERVED	STDERRLOG_HDR_PRESSURE	RESERVED	STDERRLOG_HDR_OPCODE

Bits	Field Name	Description	Type	Reset
31:24	RESERVED	Reserved	R	0x00
23:18	STDERRLOG_HDR_LEN1	This field contains the number of payload cell(s) minus one of the logged packet. Type: Status. Reset value: X.	R	0x00
17:16	RESERVED	Reserved	R	0x0
15:12	STDERRLOG_HDR_STOPOFSWRPSZ	StopOfs or WrapSize field of the logged packet (meaning depends on Wrp bit of logged opcode). Type: Status. Reset value: X.	R	0x0
11	STDERRLOG_HDR_ERR	Err bit of the logged packet. Type: Status. Reset value: X.	R	0
10:7	RESERVED	Reserved	R	0x0
6	STDERRLOG_HDR_PRESSURE	Pressure field of the logged packet. Type: Status. Reset value: X.	R	0
5:4	RESERVED	Reserved	R	0x0

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Bits	Field Name	Description	Type	Reset
3:0	STDERRLOG_HDR_OPCODE	Opcode of the logged packet. Type: Status. Reset value: X.	R	0x0

Table 13-119. Register Call Summary for Register L3_TARG_STDERRLOG_HDR

L3 Interconnect

- Severity Level of Standard and Custom Errors: [0]
- L3 TARG Register Summary and Description: [1] [2] [3] [4] [5] [6] [7]

Table 13-120. L3_TARG_STDERRLOG_MSTADDR

Address Offset	See Table 13-97.		
Physical Address	0x4400 0150	**Instance**	CLK1_DMM1_TARG
	0x4400 0250		CLK1_DMM2_TARG
	0x4400 0350		CLK1_ABE_TARG
	0x4400 0450		CLK1_L4CFG_TARG
	0x4480 0150		CLK2_GPMC_TARG
	0x4480 0250		CLK2_OCMRAM_TARG
	0x4480 0350		CLK2_DSS_TARG
	0x4480 0450		CLK2_ISS_TARG
	0x4480 0550		CLK2_CORTEXM3_TARG
	0x4480 0650		CLK2_SGX_TARG
	0x4480 0750		CLK2_IVAHD_TARG
	0x4480 0850		CLK2_SL2_TARG
	0x4480 0950		CLK2_L4PER0_TARG
	0x4480 0A50		CLK2_L4PER1_TARG
	0x4480 0B50		CLK2_L4PER2_TARG
	0x4480 0C50		CLK2_L4PER3_TARG
	0x4480 1650		CLK2_C2C_TARG
	0x4500 0150		CLK3_L4EMU_TARG
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								STDERRLOG_MSTADDR							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Reserved	R	0x000000
7:0	STDERRLOG_MSTADDR	Master Address field of the logged packet. Type: Status. Reset value: X.	R	0x00

Table 13-121. Register Call Summary for Register L3_TARG_STDERRLOG_MSTADDR

L3 Interconnect

- Severity Level of Standard and Custom Errors: [0]
- L3 TARG Register Summary and Description: [1] [2] [3] [4] [5] [6] [7]

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Table 13-122. L3_TARG_STDERRLOG_SLVADDR

Address Offset	See Table 13-97.		
Physical Address	0x4400 0154	**Instance**	CLK1_DMM1_TARG
	0x4400 0254		CLK1_DMM2_TARG
	0x4400 0354		CLK1_ABE_TARG
	0x4400 0454		CLK1_L4CFG_TARG
	0x4480 0154		CLK2_GPMC_TARG
	0x4480 0254		CLK2_OCMRAM_TARG
	0x4480 0354		CLK2_DSS_TARG
	0x4480 0454		CLK2_ISS_TARG
	0x4480 0554		CLK2_CORTEXM3_TARG
	0x4480 0654		CLK2_SGX_TARG
	0x4480 0754		CLK2_IVAHD_TARG
	0x4480 0854		CLK2_SL2_TARG
	0x4480 0954		CLK2_L4PER0_TARG
	0x4480 0A54		CLK2_L4PER1_TARG
	0x4480 0B54		CLK2_L4PER2_TARG
	0x4480 0C54		CLK2_L4PER3_TARG
	0x4480 1654		CLK2_C2C_TARG
	0x4500 0154		CLK3_L4EMU_TARG
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								STDERRLOG_SLVADDR							

Bits	Field Name	Description	Type	Reset
31:5	RESERVED	Reserved	R	0x0000000
4:0	STDERRLOG_SLVADDR	Slave Address field of the logged packet. Type: Status. Reset value: X.	R	0x00

Table 13-123. Register Call Summary for Register L3_TARG_STDERRLOG_SLVADDR

L3 Interconnect

- Severity Level of Standard and Custom Errors: [0]
- L3 TARG Register Summary and Description: [1] [2] [3] [4] [5] [6] [7]

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Table 13-124. L3_TARG_STDERRLOG_INFO

Address Offset	See Table 13-97.		
Physical Address	0x4400 0158	**Instance**	CLK1_DMM1_TARG
	0x4400 0258		CLK1_DMM2_TARG
	0x4400 0358		CLK1_ABE_TARG
	0x4400 0458		CLK1_L4CFG_TARG
	0x4480 0158		CLK2_GPMC_TARG
	0x4480 0258		CLK2_OCMRAM_TARG
	0x4480 0358		CLK2_DSS_TARG
	0x4480 0458		CLK2_ISS_TARG
	0x4480 0558		CLK2_CORTEXM3_TARG
	0x4480 0658		CLK2_SGX_TARG
	0x4480 0758		CLK2_IVAHD_TARG
	0x4480 0858		CLK2_SL2_TARG
	0x4480 0958		CLK2_L4PER0_TARG
	0x4480 0A58		CLK2_L4PER1_TARG
	0x4480 0B58		CLK2_L4PER2_TARG
	0x4480 0C58		CLK2_L4PER3_TARG
	0x4480 1658		CLK2_C2C_TARG
	0x4500 0158		CLK3_L4EMU_TARG
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								STDERRLOG_INFO							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Reserved	R	0x000000
7:0	STDERRLOG_INFO	Info field of the logged packet. Type: Status. Reset value: X.	R	0x00

Table 13-125. Register Call Summary for Register L3_TARG_STDERRLOG_INFO

L3 Interconnect

- Severity Level of Standard and Custom Errors: [0]
- L3 TARG Register Summary and Description: [1] [2] [3] [4] [5] [6] [7]

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Table 13-126. L3_TARG_STDERRLOG_SLVOFSLSB

Address Offset	See Table 13-97.		
Physical Address	0x4400 015C	**Instance**	CLK1_DMM1_TARG
	0x4400 025C		CLK1_DMM2_TARG
	0x4400 035C		CLK1_ABE_TARG
	0x4400 045C		CLK1_L4CFG_TARG
	0x4480 015C		CLK2_GPMC_TARG
	0x4480 025C		CLK2_OCMRAM_TARG
	0x4480 035C		CLK2_DSS_TARG
	0x4480 045C		CLK2_ISS_TARG
	0x4480 055C		CLK2_CORTEXM3_TARG
	0x4480 065C		CLK2_SGX_TARG
	0x4480 075C		CLK2_IVAHD_TARG
	0x4480 085C		CLK2_SL2_TARG
	0x4480 095C		CLK2_L4PER0_TARG
	0x4480 0A5C		CLK2_L4PER1_TARG
	0x4480 0B5C		CLK2_L4PER2_TARG
	0x4480 0C5C		CLK2_L4PER3_TARG
	0x4480 165C		CLK2_C2C_TARG
	0x4500 015C		CLK3_L4EMU_TARG
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STDERRLOG_SLVOFSLSB																															

Bits	Field Name	Description	Type	Reset
31:0	STDERRLOG_SLVOFSLSB	LSB of the slave offset field, concatenated with start offset field of the logged packet. Type: Status. Reset value: X.	R	0x0000 0000

Table 13-127. Register Call Summary for Register L3_TARG_STDERRLOG_SLVOFSLSB

L3 Interconnect

- L3 TARG Register Summary and Description: [0] [1] [2] [3] [4] [5] [6]

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Table 13-128. L3_TARG_STDERRLOG_SLVOFSMSB

Address Offset	See Table 13-97.		
Physical Address	0x4400 0160	**Instance**	CLK1_DMM1_TARG
	0x4400 0260		CLK1_DMM2_TARG
	0x4400 0360		CLK1_ABE_TARG
	0x4400 0460		CLK1_L4CFG_TARG
	0x4480 0160		CLK2_GPMC_TARG
	0x4480 0260		CLK2_OCMRAM_TARG
	0x4480 0360		CLK2_DSS_TARG
	0x4480 0460		CLK2_ISS_TARG
	0x4480 0560		CLK2_CORTEXM3_TARG
	0x4480 0660		CLK2_SGX_TARG
	0x4480 0760		CLK2_IVAHD_TARG
	0x4480 0860		CLK2_SL2_TARG
	0x4480 0960		CLK2_L4PER0_TARG
	0x4480 0A60		CLK2_L4PER1_TARG
	0x4480 0B60		CLK2_L4PER2_TARG
	0x4480 0C60		CLK2_L4PER3_TARG
	0x4480 1660		CLK2_C2C_TARG
	0x4500 0160		CLK3_L4EMU_TARG
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															STDERRLOG_SLVOFSMSB

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	STDERRLOG_SLVOFSMSB	MSB of the slave offset field of the logged packet (according to NTTP packet format, this register field may exceed the actual slave offset size. Unused bits are stuck at 0, if any). Type: Status. Reset value: X.	R	0

Table 13-129. Register Call Summary for Register L3_TARG_STDERRLOG_SLVOFSMSB

L3 Interconnect

- L3 TARG Register Summary and Description: [0] [1] [2] [3] [4] [5] [6]

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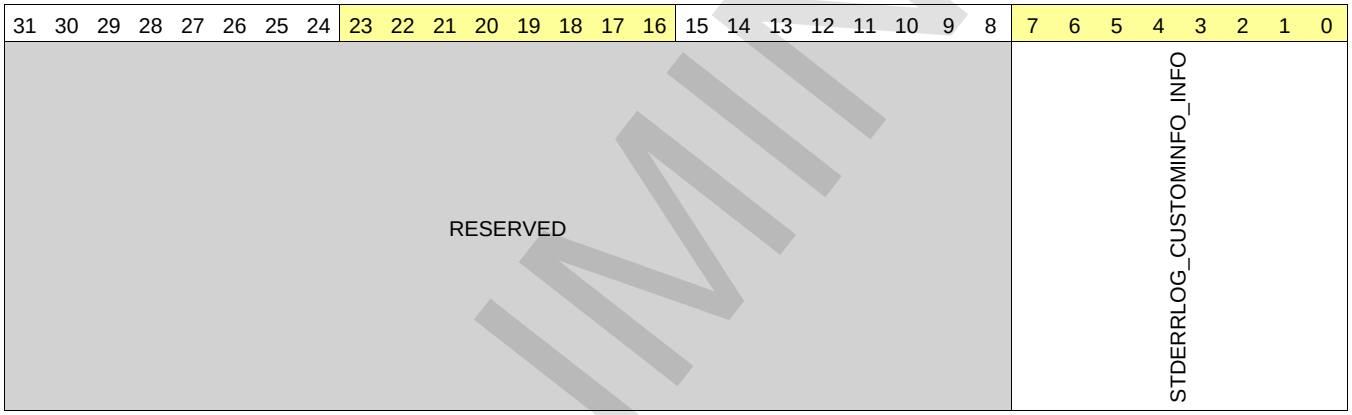
Table 13-130. L3_TARG_STDERRLOG_CUSTOMINFO_INFO

Address Offset	See Table 13-97.		
Physical Address	0x4400 0164	**Instance**	CLK1_DMM1_TARG
	0x4400 0264		CLK1_DMM2_TARG
	0x4400 0364		CLK1_ABE_TARG
	0x4400 0464		CLK1_L4CFG_TARG
	0x4480 0164		CLK2_GPMC_TARG
	0x4480 0264		CLK2_OCMRAM_TARG
	0x4480 0364		CLK2_DSS_TARG
	0x4480 0464		CLK2_ISS_TARG
	0x4480 0564		CLK2_CORTEXM3_TARG
	0x4480 0664		CLK2_SGX_TARG
	0x4480 0764		CLK2_IVAHD_TARG
	0x4480 0864		CLK2_SL2_TARG
	0x4480 0964		CLK2_L4PER0_TARG
	0x4480 0A64		CLK2_L4PER1_TARG
	0x4480 0B64		CLK2_L4PER2_TARG
	0x4480 0C64		CLK2_L4PER3_TARG
	0x4480 1664		CLK2_C2C_TARG
	0x4500 0164		CLK3_L4EMU_TARG
Description			
Type	R		



Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Reserved	R	0x000000
7:0	STDERRLOG_CUSTOMINFO_INFO	Info field of the response packet. Type: Status. Reset value: X.	R	0x00

Table 13-131. Register Call Summary for Register L3_TARG_STDERRLOG_CUSTOMINFO_INFO

L3 Interconnect

- L3 TARG Register Summary and Description: [0] [1] [2] [3] [4] [5] [6]

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Table 13-132. L3_TARG_STDERRLOG_CUSTOMINFO_MSTADDR

Address Offset	See Table 13-97.		
Physical Address	0x4400 0168	**Instance**	CLK1_DMM1_TARG
	0x4400 0268		CLK1_DMM2_TARG
	0x4400 0368		CLK1_ABE_TARG
	0x4400 0468		CLK1_L4CFG_TARG
	0x4480 0168		CLK2_GPMC_TARG
	0x4480 0268		CLK2_OCMRAM_TARG
	0x4480 0368		CLK2_DSS_TARG
	0x4480 0468		CLK2_ISS_TARG
	0x4480 0568		CLK2_CORTEXM3_TARG
	0x4480 0668		CLK2_SGX_TARG
	0x4480 0768		CLK2_IVAHD_TARG
	0x4480 0868		CLK2_SL2_TARG
	0x4480 0968		CLK2_L4PER0_TARG
	0x4480 0A68		CLK2_L4PER1_TARG
	0x4480 0B68		CLK2_L4PER2_TARG
	0x4480 0C68		CLK2_L4PER3_TARG
	0x4480 1668		CLK2_C2C_TARG
	0x4500 0168		CLK3_L4EMU_TARG
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								STDERRLOG_CUSTOMINFO_MSTADDR							
R-0																								R-0							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Reserved	R	0x000000
7:0	STDERRLOG_CUSTOMINFO_MSTADDR	MstAddr field of the response packet. Type: Status. Reset value: X.	R	0x00

Table 13-133. Register Call Summary for Register L3_TARG_STDERRLOG_CUSTOMINFO_MSTADDR

L3 Interconnect

- L3 TARG Register Summary and Description: [0] [1] [2] [3] [4] [5] [6]

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Table 13-134. L3_TARG_STDERRLOG_CUSTOMINFO_OPCODE

Address Offset	See Table 13-97.		
Physical Address	0x4400 016C 0x4400 026C 0x4400 036C 0x4400 046C 0x4480 016C 0x4480 026C 0x4480 036C 0x4480 046C 0x4480 056C 0x4480 066C 0x4480 076C 0x4480 086C 0x4480 096C 0x4480 0A6C 0x4480 0B6C 0x4480 0C6C 0x4480 166C 0x4500 016C	**Instance**	CLK1_DMM1_TARG CLK1_DMM2_TARG CLK1_ABE_TARG CLK1_L4CFG_TARG CLK2_GPMC_TARG CLK2_OCMRAM_TARG CLK2_DSS_TARG CLK2_ISS_TARG CLK2_CORTEXM3_TARG CLK2_SGX_TARG CLK2_IVAHD_TARG CLK2_SL2_TARG CLK2_L4PER0_TARG CLK2_L4PER1_TARG CLK2_L4PER2_TARG CLK2_L4PER3_TARG CLK2_C2C_TARG CLK3_L4EMU_TARG
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														STDERRLOG_CUSTOMINFO_OPCODE	

Bits	Field Name	Description	Type	Reset
31:2	RESERVED	Reserved	R	0x0000 0000
1:0	STDERRLOG_CUSTOMINFO_OPCODE	Opcode of the response packet. Type: Status. Reset value: X.	R	0x0

Table 13-135. Register Call Summary for Register L3_TARG_STDERRLOG_CUSTOMINFO_OPCODE

L3 Interconnect

- L3 TARG Register Summary and Description: [0] [1] [2] [3] [4] [5] [6]

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Table 13-136. L3_TARG_ADDRSPACESIZELOG

Address Offset	See Table 13-97.		
Physical Address	0x4400 0180	**Instance**	CLK1_DMM1_TARG
	0x4400 0280		CLK1_DMM2_TARG
	0x4400 0380		CLK1_ABE_TARG
	0x4400 0480		CLK1_L4CFG_TARG
	0x4480 0180		CLK2_GPMC_TARG
	0x4480 0280		CLK2_OCMRAM_TARG
	0x4480 0380		CLK2_DSS_TARG
	0x4480 0480		CLK2_ISS_TARG
	0x4480 0580		CLK2_CORTEXM3_TARG
	0x4480 0680		CLK2_SGX_TARG
	0x4480 0780		CLK2_IVAHD_TARG
	0x4480 0880		CLK2_SL2_TARG
	0x4480 0980		CLK2_L4PER0_TARG
	0x4480 0A80		CLK2_L4PER1_TARG
	0x4480 0B80		CLK2_L4PER2_TARG
	0x4480 0C80		CLK2_L4PER3_TARG
	0x4480 1680		CLK2_C2C_TARG
	0x4500 0180		CLK3_L4EMU_TARG
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								ADDRSPACESIZELOG							

Bits	Field Name	Description	Type	Reset
31:5	RESERVED	Reserved	R	0x0000000
4:0	ADDRSPACESIZELOG	The address space size is equal to 2**AddrSpaceSizeLog * 4K in bytes. Type: Control. Reset value: 0x1F.	RW	0x1F

Table 13-137. Register Call Summary for Register L3_TARG_ADDRSPACESIZELOG

L3 Interconnect

- L3 TARG Register Summary and Description: [0] [1] [2] [3] [4] [5] [6]

13.2.5.1.4 L3 PWR_DISC Register Summary and Description

Table 13-138. PWR_DISC Instance Summary

Module Name	Base Address	Size
CLK1_CLK1_TARG_PWR_DISC_CLK2	0x4400 0600	4KB
CLK2_CLK2_TARG_PWR_DISC_CLK1	0x4480 1100	4KB

13.2.5.1.4.1 L3 PWR_DISC Register Summary

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Table 13-139. PWR_DISC Registers Summary

Register Name	Type	Register Width (Bits)	Address Offset for CLK1_CLK1_TARG_PWR_DISC_CLK2	CLK1_CLK1_TARG_PWR_DISC_CLK2 L3 Physical Address	Address Offset for CLK2_CLK2_TARG_PWR_DISC_CLK`	CLK2_CLK2_TARG_PWR_DISC_CLK1 L3 Physical Address
L3_PWR_DISC_STDHOSTHDR_COREREG	R	32	0x0000 0600	0x4400 0600	0x0080 1100	0x4480 1100
L3_PWR_DISC_STDHOSTHDR_VERSIONREG	R	32	0x0000 0604	0x4400 0604	0x0080 1104	0x4480 1104
L3_PWR_DISC_STDHOSTHDR_MAINCTLREG	R	32	0x0000 0608	0x4400 0608	0x0080 1108	0x4480 1108
L3_PWR_DISC_STDERRLOG_SVRTSTDLVL	RW	32	0x0000 0640	0x4400 0640	0x0080 1140	0x4480 1140
L3_PWR_DISC_STDERRLOG_MAIN	RW	32	0x0000 0648	0x4400 0648	0x0080 1148	0x4480 1148
L3_PWR_DISC_STDERRLOG_HDR	R	32	0x0000 064C	0x4400 064C	0x0080 114C	0x4480 114C
L3_PWR_DISC_STDERRLOG_MSTADDR	R	32	0x0000 0650	0x4400 0650	0x0080 1150	0x4480 1150
L3_PWR_DISC_STDERRLOG_SLVADDR	R	32	0x0000 0654	0x4400 0654	0x0080 1154	0x4480 1154
L3_PWR_DISC_STDERRLOG_INFO	R	32	0x0000 0658	0x4400 0658	0x0080 1158	0x4480 1158
L3_PWR_DISC_STDERRLOG_SLVOFSLSB	R	32	0x0000 065C	0x4400 065C	0x0080 115C	0x4480 115C
L3_PWR_DISC_STDERRLOG_SLVOFSMSB	R	32	0x0000 0660	0x4400 0660	0x0080 1160	0x4480 1160

13.2.5.1.4.2 L3 PWR_DISC Register Description

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Table 13-140. L3_PWR_DISC_STDHOSTHDR_COREREG

Address Offset	See Table 13-139.		
Physical Address	0x4400 0600 0x4480 1100	**Instance**	CLK1_CLK1_TARG_PWR_DISC_CLK2 CLK2_CLK2_TARG_PWR_DISC_CLK1
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								STDHOSTHDR_COREREG_CORECODE								RESERVED								STDHOSTHDR_COREREG_VENDORCODE							

Bits	Field Name	Description	Type	Reset
31:22	RESERVED	RESERVED	R	0x000
21:16	STDHOSTHDR_COREREG_CORECODE	The Core Code field is a constant reporting a vendor-specific core generator code. Type: Constant. Reset value: 0x38.	R	0x38
15:1	RESERVED	RESERVED	R	0x0000
0	STDHOSTHDR_COREREG_VENDORCODE	The Vendor Code field is a constant reporting the core generator vendor code. Type: Constant. Reset value: 0x1. Read 0x0: Third-party vendor. Read 0x1:	R	1

Table 13-141. Register Call Summary for Register L3_PWR_DISC_STDHOSTHDR_COREREG

L3 Interconnect

- L3 PWR_DISC Register Summary and Description: [0]

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Table 13-142. L3_PWR_DISC_STDHOSTHDR_VERSIONREG

Address Offset	See Table 13-139.		
Physical Address	0x4400 0604 0x4480 1104	**Instance**	CLK1_CLK1_TARG_PWR_DISC_CLK2 CLK2_CLK2_TARG_PWR_DISC_CLK1
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STDHOSTHDR_VERSIONREG_REVISIONID								STDHOSTHDR_VERSIONREG_COREPARAMSCHECKSUM																							

Bits	Field Name	Description	Type	Reset
31:24	STDHOSTHDR_VERSIONREG_REVISIONID	The Revision Identifier field is a constant reporting the core generator revision number. Type: Constant. Reset value: 0x0.	R	0x00
23:0	STDHOSTHDR_VERSIONREG_COREPARAMSCHECKSUM	Reserved. Type: Reserved. Reset value: Reserved.	R	0x000000

Table 13-143. Register Call Summary for Register L3_PWR_DISC_STDHOSTHDR_VERSIONREG

L3 Interconnect

- L3 PWR_DISC Register Summary and Description: [0]

Table 13-144. L3_PWR_DISC_STDHOSTHDR_MAINCTLREG

Address Offset	See Table 13-139.		
Physical Address	0x4400 0608 0x4480 1108	**Instance**	CLK1_CLK1_TARG_PWR_DISC_CLK2 CLK2_CLK2_TARG_PWR_DISC_CLK1
Description			
Type	R		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																											RESERVED	STDHOSTHDR_MAINCTLREG_CM	STDHOSTHDR_MAINCTLREG_FLT	RESERVED		

Bits	Field Name	Description	Type	Reset
31:5	RESERVED	Reserved	R	0x0000000
4	RESERVED	Reserved	R	0
3	STDHOSTHDR_MAINCTLREG_CM	Reserved for internal testing. Must be set to 0. Type: Control. Reset value: 0x0.	R	0
2	STDHOSTHDR_MAINCTLREG_FLT	Asserted when a Fault condition is detected: if the unit includes Error Logging, Flt is asserted when the FltCnt register field indicates a Fault, and deasserted when FltCnt is reset. If no Error Logging is implemented, this bit becomes unit-dependent. In all cases, Flt bit and Flt pin (service network) have the same logical level. Type: Status. Reset value: X.	R	0
1:0	RESERVED	Reserved	R	0x0

Table 13-145. Register Call Summary for Register L3_PWR_DISC_STDHOSTHDR_MAINCTLREG

L3 Interconnect

- L3 PWR_DISC Register Summary and Description: [0]

Table 13-146. L3_PWR_DISC_STDERRLOG_SVRTSTDLVL

Address Offset	See Table 13-139.		
Physical Address	0x4400 0640 0x4480 1140	**Instance**	CLK1_CLK1_TARG_PWR_DISC_CLK2 CLK2_CLK2_TARG_PWR_DISC_CLK1
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														STDERRLOG_SVRTSTDLVL_0	

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Bits	Field Name	Description	Type	Reset
31:2	RESERVED	Reserved	R	0x0000 0000
1:0	STDERRLOG_SVRTSTDLVL_0	Severity level parameters Type: Control. Reset value: 0x2. 0x0: Error logging is disabled. 0x1: Errors are logged with severity level Error. 0x2: Errors are logged with severity level Fault.	RW	0x2

Table 13-147. Register Call Summary for Register L3_PWR_DISC_STDERRLOG_SVRTSTDLVL

L3 Interconnect

- L3 PWR_DISC Register Summary and Description: [0]

Table 13-148. L3_PWR_DISC_STDERRLOG_MAIN

Address Offset	See Table 13-139.		
Physical Address	0x4400 0648 0x4480 1148	**Instance**	CLK1_CLK1_TARG_PWR_DISC_CLK2 CLK2_CLK2_TARG_PWR_DISC_CLK1
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STDERRLOG_MAIN_CLRLOG	RESERVED											STDERRLOG_MAIN_FLTCNT	STDERRLOG_MAIN_ERRCNT	RESERVED																	STDERRLOG_MAIN_ERRTYPE	STDERRLOG_MAIN_ERRLOGVLD

Bits	Field Name	Description	Type	Reset
31	STDERRLOG_MAIN_CLRLOG	Clears Error Logging Valid bit when written to 1. Type: Give_AutoCleared. Reset value: 0x0.	RW	0
30:20	RESERVED	Reserved	R	0x000
19	STDERRLOG_MAIN_FLTCNT	Asserted when at least one error with severity level FAULT is detected. Reset when written to 1. Type: Take. Reset value: 0x0.	RW	0
18	STDERRLOG_MAIN_ERRCNT	Asserted when at least one error with severity level ERROR is detected. Reset when written to 1. Type: Take. Reset value: 0x0.	RW	0
17:2	RESERVED	Reserved	R	0x0000
1	STDERRLOG_MAIN_ERRTYPE	Indicates logging type. Type: Status. Reset value: X. Read 0x0: Logged Error format is standard (header and necker recorded). Read 0x1: Logged Error format is module dependent. CustomInfo register(s) may be implemented to store additional information.	R	0
0	STDERRLOG_MAIN_ERRLOGVLD	Error Logging Valid. Asserted when logging information is valid(indicates that an error has been logged). Type: Status. Reset value: X.	R	0

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Table 13-149. Register Call Summary for Register L3_PWR_DISC_STDERRLOG_MAIN

L3 Interconnect

- L3 PWR_DISC Register Summary and Description: [0]

Table 13-150. L3_PWR_DISC_STDERRLOG_HDR

Address Offset	See Table 13-139.		
Physical Address	0x4400 064C 0x4480 114C	**Instance**	CLK1_CLK1_TARG_PWR_DISC_CLK2 CLK2_CLK2_TARG_PWR_DISC_CLK1
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								STDERRLOG_HDR_LEN1						RESERVED		STDERRLOG_HDR_STOPOFSWRPSZ				STDERRLOG_HDR_ERR	RESERVED			STDERRLOG_HDR_PRESSURE	RESERVED			STDERRLOG_HDR_OPCODE			

Bits	Field Name	Description	Type	Reset
31:24	RESERVED	Reserved	R	0x00
23:18	STDERRLOG_HDR_LEN1	This field contains the number of payload cell(s) minus one of the logged packet. Type: Status. Reset value: X.	R	0x00
17:16	RESERVED	Reserved	R	0x0
15:12	STDERRLOG_HDR_STOPOFSWRPSZ	StopOfs or WrapSize field of the logged packet (meaning depends on Wrp bit of logged opcode). Type: Status. Reset value: X.	R	0x0
11	STDERRLOG_HDR_ERR	Err bit of the logged packet. Type: Status. Reset value: X.	R	0
10:7	RESERVED	Reserved	R	0x0
6	STDERRLOG_HDR_PRESSURE	Pressure field of the logged packet. Type: Status. Reset value: X.	R	0
5:4	RESERVED	Reserved	R	0x0
3:0	STDERRLOG_HDR_OPCODE	Opcode of the logged packet. Type: Status. Reset value: X.	R	0x0

Table 13-151. Register Call Summary for Register L3_PWR_DISC_STDERRLOG_HDR

L3 Interconnect

- L3 PWR_DISC Register Summary and Description: [0]

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Table 13-152. L3_PWR_DISC_STDERRLOG_MSTADDR

Address Offset	See Table 13-139.		
Physical Address	0x4400 0650 0x4480 1150	**Instance**	CLK1_CLK1_TARG_PWR_DISC_CLK2 CLK2_CLK2_TARG_PWR_DISC_CLK1
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								STDERRLOG_MSTADDR							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Reserved	R	0x000000
7:0	STDERRLOG_MSTADDR	Master Address field of the logged packet. Type: Status. Reset value: X.	R	0x00

Table 13-153. Register Call Summary for Register L3_PWR_DISC_STDERRLOG_MSTADDR

L3 Interconnect

- L3 PWR_DISC Register Summary and Description: [0]

Table 13-154. L3_PWR_DISC_STDERRLOG_SLVADDR

Address Offset	See Table 13-139.		
Physical Address	0x4400 0654 0x4480 1154	**Instance**	CLK1_CLK1_TARG_PWR_DISC_CLK2 CLK2_CLK2_TARG_PWR_DISC_CLK1
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																											STDERRLOG_SLVADDR				

Bits	Field Name	Description	Type	Reset
31:5	RESERVED	Reserved	R	0x0000000
4:0	STDERRLOG_SLVADDR	Slave Address field of the logged packet. Type: Status. Reset value: X.	R	0x00

Table 13-155. Register Call Summary for Register L3_PWR_DISC_STDERRLOG_SLVADDR

L3 Interconnect

- L3 PWR_DISC Register Summary and Description: [0]

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Table 13-156. L3_PWR_DISC_STDERRLOG_INFO

Address Offset	See Table 13-139.		
Physical Address	0x4400 0658 0x4480 1158	**Instance**	CLK1_CLK1_TARG_PWR_DISC_CLK2 CLK2_CLK2_TARG_PWR_DISC_CLK1
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								STDERRLOG_INFO							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Reserved	R	0x000000
7:0	STDERRLOG_INFO	Info field of the logged packet. Type: Status. Reset value: X.	R	0x00

Table 13-157. Register Call Summary for Register L3_PWR_DISC_STDERRLOG_INFO

L3 Interconnect

- L3 PWR_DISC Register Summary and Description: [0]

Table 13-158. L3_PWR_DISC_STDERRLOG_SLVOFSLSB

Address Offset	See Table 13-139.		
Physical Address	0x4400 065C 0x4480 115C	**Instance**	CLK1_CLK1_TARG_PWR_DISC_CLK2 CLK2_CLK2_TARG_PWR_DISC_CLK1
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STDERRLOG_SLVOFSLSB																															

Bits	Field Name	Description	Type	Reset
31:0	STDERRLOG_SLVOFSLSB	LSB of the slave offset field, concatenated with start offset field of the logged packet. Type: Status. Reset value: X.	R	0x0000 0000

Table 13-159. Register Call Summary for Register L3_PWR_DISC_STDERRLOG_SLVOFSLSB

L3 Interconnect

- L3 PWR_DISC Register Summary and Description: [0]

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Table 13-160. L3_PWR_DISC_STDERRLOG_SLVOFSMSB

Address Offset	See Table 13-139.		
Physical Address	0x4400 0660 0x4480 1160	**Instance**	CLK1_CLK1_TARG_PWR_DISC_CLK2 CLK2_CLK2_TARG_PWR_DISC_CLK1
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															STDERRLOG_SLVOFSMSB

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	STDERRLOG_SLVOFSMSB	MSB of the slave offset field of the logged packet (according to NTTP packet format, this register field may exceed the actual slave offset size. Unused bits are stuck at 0, if any). Type: Status. Reset value: X.	R	0

Table 13-161. Register Call Summary for Register L3_PWR_DISC_STDERRLOG_SLVOFSMSB

L3 Interconnect

- L3 PWR_DISC Register Summary and Description: [0]

13.2.5.1.5 L3 FLAGMUX Register Summary and Description

Table 13-162. FLAGMUX Instance Summary

Module Name	Base Address	Size
CLK1_FLAGMUX_CLK1	0x4400 0500	4KB
CLK2_FLAGMUX_CLK2	0x4480 1000	4KB
CLK3_FLAGMUX_CLK3	0x4500 0200	4KB

13.2.5.1.5.1 L3 FLAGMUX Register Summary

Table 13-163. FLAGMUX Registers Summary

Register Name	Type	Register Width (Bits)	Address Offset for CLK1	CLK1_FLAGMUX_CLK1 L3 Physical Address
L3_FLAGMUX_STDHOSTHDR_COREREG	R	32	0x0000 0500	0x4400 0500
L3_FLAGMUX_STDHOSTHDR_VERSIONREG	R	32	0x0000 0504	0x4400 0504
L3_FLAGMUX_MASK0	RW	32	0x0000 0508	0x4400 0508
L3_FLAGMUX_REGERR0	R	32	0x0000 050C	0x4400 050C
L3_FLAGMUX_MASK1	RW	32	0x0000 0510	0x4400 0510
L3_FLAGMUX_REGERR1	RW	32	0x0000 0514	0x4400 0514

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Table 13-164. FLAGMUX Registers Summary

Register Name	Type	Register Width (Bits)	Address Offset for CLK2	CLK2_FLAGMUX_CLK2 L3 Physical Address	Address Offset for CLK3	CLK3_FLAGMUX_CLK3 L3 Physical Address
L3_FLAGMUX_STDHOSTHDR_COREREG	R	32	0x0080 1000	0x4480 1000	0x0100 0200	0x4500 0200
L3_FLAGMUX_STDHOSTHDR_VERSIONREG	R	32	0x0080 1004	0x4480 1004	0x0100 0204	0x4500 0204
L3_FLAGMUX_MASK0	RW	32	0x0080 1008	0x4480 1008	0x0100 0208	0x4500 0208
L3_FLAGMUX_REGERR0	R	32	0x0080 100C	0x4480 100C	0x0100 0210	0x4500 020C
L3_FLAGMUX_MASK1	RW	32	0x0080 1010	0x4480 1010	0x0100 0240	0x4500 0210
L3_FLAGMUX_REGERR1	RW	32	0x0080 1014	0x4480 1014	0x0100 0244	0x4500 0214

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13.2.5.1.5.2 L3 FLAGMUX Register Description

Table 13-165. L3_FLAGMUX_STDHOSTHDR_COREREG

Address Offset	See Table 13-163.		
Physical Address	0x4400 0500 0x4480 1000 0x4500 0200	**Instance**	CLK1_FLAGMUX_CLK1 CLK2_FLAGMUX_CLK2 CLK3_FLAGMUX_CLK3
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								STDHOSTHDR_COREREG_CORECODE								RESERVED								STDHOSTHDR_COREREG_VENDORCODE							

Bits	Field Name	Description	Type	Reset
31:22	RESERVED	Reserved	R	0x000
21:16	STDHOSTHDR_COREREG_CORECODE	The Core Code field is a constant reporting a vendor-specific core generator code. Type: Constant. Reset value: 0x37.	R	0x37
15:1	RESERVED	Reserved	R	0x0000
0	STDHOSTHDR_COREREG_VENDORCODE	The Vendor Code field is a constant reporting the core generator vendor code. Type: Constant. Reset value: 0x1. Read 0x0: Third-party vendor. Read 0x1:	R	1

Table 13-166. Register Call Summary for Register L3_FLAGMUX_STDHOSTHDR_COREREG

L3 Interconnect

- L3 FLAGMUX Register Summary and Description: [0] [1]

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Table 13-167. L3_FLAGMUX_STDHOSTHDR_VERSIONREG

Address Offset	See Table 13-163.		
Physical Address	0x4400 0504 0x4480 1004 0x4500 0204	**Instance**	CLK1_FLAGMUX_CLK1 CLK2_FLAGMUX_CLK2 CLK3_FLAGMUX_CLK3
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STDHOSTHDR_VERSIONREG_REVISIONID								STDHOSTHDR_VERSIONREG_COREPARAMSCHECKSUM																							

Bits	Field Name	Description	Type	Reset
31:24	STDHOSTHDR_VERSIONREG_REVISIONID	The Revision Identifier field is a constant reporting the core generator revision number. Type: Constant. Reset value: 0x0.	R	0x00
23:0	STDHOSTHDR_VERSIONREG_COREPARAMSCHECKSUM	Reserved. Type: Reserved. Reset value: Reserved.	R	0x000000

Table 13-168. Register Call Summary for Register L3_FLAGMUX_STDHOSTHDR_VERSIONREG

L3 Interconnect

- Flag Mux Generators: [0]
- L3 FLAGMUX Register Summary and Description: [1] [2]

Table 13-169. L3_FLAGMUX_MASK0

Address Offset	See Table 13-163.		
Physical Address	0x4400 0508 0x4480 1008 0x4500 0208	**Instance**	CLK1_FLAGMUX_CLK1 CLK2_FLAGMUX_CLK2 CLK3_FLAGMUX_CLK3
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																MASK0															

Bits	Field Name	Description	Type	Reset
31:18	RESERVED	Reserved	R	0x0000
17:0	MASK0	Mask flag inputs 0 Type: Control. Reset value: 0x3FFFF.	RW	0x3FFFF

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Table 13-170. Register Call Summary for Register L3_FLAGMUX_MASK0

L3 Interconnect

- Flag Mux Error Logging: [0]
- L3 Interconnect Error Analysis Mode: [1]
- L3 FLAGMUX Register Summary and Description: [2] [3]

Table 13-171. L3_FLAGMUX_REGERR0

Address Offset	See Table 13-163.		
Physical Address	0x4400 050C 0x4480 100C 0x4500 020C	**Instance**	CLK1_FLAGMUX_CLK1 CLK2_FLAGMUX_CLK2 CLK3_FLAGMUX_CLK3
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								REGERR0																							

Bits	Field Name	Description	Type	Reset
31:18	RESERVED	Reserved	R	0x0000
17:0	REGERR0	Flag inputs 0 Type: Status. Reset value: X.	R	0x00000

Table 13-172. Register Call Summary for Register L3_FLAGMUX_REGERR0

L3 Interconnect

- Flag Mux Generators: [0]
- Flag Mux Error Logging: [1]
- L3 Interconnect Error Analysis Mode: [2] [3] [4] [5]
- L3 FLAGMUX Register Summary and Description: [6] [7]

Table 13-173. L3_FLAGMUX_MASK1

Address Offset	See Table 13-163.		
Physical Address	0x4400 0510 0x4480 1010 0x4500 0210	**Instance**	CLK1_FLAGMUX_CLK1 CLK2_FLAGMUX_CLK2 CLK3_FLAGMUX_CLK3
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								MASK1																							

Bits	Field Name	Description	Type	Reset
31:18	RESERVED	Reserved	R	0x0000
17:0	MASK1	Mask flag inputs 1 Type: Control. Reset value: 0x3FFFF.	RW	0x3FFFF

Table 13-174. Register Call Summary for Register L3_FLAGMUX_MASK1

L3 Interconnect

- Flag Mux Error Logging: [0]
- L3 Interconnect Error Analysis Mode: [1]
- L3 FLAGMUX Register Summary and Description: [2] [3]

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Table 13-175. L3_FLAGMUX_REGERR1

Address Offset	See Table 13-163.		
Physical Address	0x4400 0514 0x4480 1014 0x4500 0214	**Instance**	CLK1_FLAGMUX_CLK1 CLK2_FLAGMUX_CLK2 CLK3_FLAGMUX_CLK3
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																REGERR1															

Bits	Field Name	Description	Type	Reset
31:18	RESERVED	Reserved	R	0x0000
17:0	REGERR1	Flag inputs 1 Type: Status. Reset value: X.	R	0x00000

Table 13-176. Register Call Summary for Register L3_FLAGMUX_REGERR1

L3 Interconnect

- Flag Mux Generators: [0]
- Flag Mux Error Logging: [1]
- L3 Interconnect Error Analysis Mode: [2] [3] [4] [5]
- L3 FLAGMUX Register Summary and Description: [6] [7]

13.2.5.1.6 L3 BW Regulator Register Summary and Description

Table 13-177. BW_REGULATOR Instance Summary

Module Name	Base Address	Size
CLK1_DSS_BW_REGULATOR	0x4400 0700	256 bytes
CLK2_ISS_BW_REGULATOR	0x4480 1300	256 bytes
CLK2_IVAHD_BW_REGULATOR	0x4480 1400	256 bytes
CLK2_SGX_BW_REGULATOR	0x4480 1500	256 bytes

13.2.5.1.6.1 L3 BW Regulator Register Summary

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Table 13-178. BW_REGULATOR Registers Summary

Register Name	Type	Register Width (Bits)	Address Offset for CLK1_DSS_BW_REGULATOR	CLK1_DSS_BW_REGULATOR L3 Physical Address	Address Offset for CLK2_ISS_BW_REGULATOR	CLK2_ISS_BW_REGULATOR L3 Physical Address	Address Offset for CLK2_IVAHD_BW_REGULATOR	CLK2_IVAHD_BW_REGULATOR L3 Physical Address
L3_BW_R_STDHOSTHDR_COREREG	R	32	0x0000 0700	0x4400 0700	0x0080 1300	0x4480 1300	0x0080 1400	0x4480 1400
L3_BW_R_STDHOSTHDR_VERSIONREG	R	32	0x0000 0704	0x4400 0704	0x0080 1304	0x4480 1304	0x0080 1404	0x4480 1404
L3_BW_R_BANDWIDTH	RW	32	0x0000 0708	0x4400 0708	0x0080 1308	0x4480 1308	0x0080 1408	0x4480 1408
L3_BW_R_WATERMARK	RW	32	0x0000 0710	0x4400 070C	0x0080 130C	0x4480 130C	0x0080 140C	0x4480 140C
L3_BW_R_PRESS	R	32	0x0000 0740	0x4400 0710	0x0080 1310	0x4480 1310	0x0080 1410	0x4480 1410
L3_BW_R_CLEARHISTORY	RW	32	0x0000 0744	0x4400 0714	0x0080 1314	0x4480 1314	0x0080 1414	0x4480 1414

Table 13-179. BW_REGULATOR Registers Summary

Register Name	Type	Register Width (Bits)	Address Offset for CLK2_SGX_BW_REGULATOR	CLK2_SGX_BW_REGULATOR
L3_BW_R_STDHOSTHDR_COREREG	R	32	0x0080 1500	0x4480 1500
L3_BW_R_STDHOSTHDR_VERSIONREG	R	32	0x0080 1504	0x4480 1504
L3_BW_R_BANDWIDTH	RW	32	0x0080 1508	0x4480 1508
L3_BW_R_WATERMARK	RW	32	0x0080 150C	0x4480 150C
L3_BW_R_PRESS	R	32	0x0080 1510	0x4480 1510
L3_BW_R_CLEARHISTORY	RW	32	0x0080 1514	0x4480 1514

13.2.5.1.6.2 L3 BW Regulator Register Description

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Table 13-180. L3_BW_R_STDHOSTHDR_COREREG

Address Offset	See Table 13-178.		
Physical Address	0x4400 0700 0x4480 1300 0x4480 1400	**Instance**	CLK1_DSS_BW_REGULATOR CLK2_ISS_BW_REGULATOR CLK2_IVAHD_BW_REGULATOR
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								STDHOSTHDR_COREREG_CORECODE								RESERVED								STDHOSTHDR_COREREG_VENDORCODE							

Bits	Field Name	Description	Type	Reset
31:22	RESERVED	Reserved	R	0x000
21:16	STDHOSTHDR_COREREG_CORECODE	The Core Code field is a constant reporting a vendor-specific core generator code. Type: Constant. Reset value: 0x31.	R	0x31
15:1	RESERVED	Reserved	R	0x0000
0	STDHOSTHDR_COREREG_VENDORCODE	The Vendor Code field is a constant reporting the core generator vendor code. Type: Constant. Reset value: 0x1. Read 0x0: Third-party vendor. Read 0x1:	R	1

Table 13-181. Register Call Summary for Register L3_BW_R_STDHOSTHDR_COREREG

L3 Interconnect

- L3 BW Regulator Register Summary and Description: [0] [1]

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Table 13-182. L3_BW_R_STDHOSTHDR_VERSIONREG

Address Offset	See Table 13-178.		
Physical Address	0x4400 0704 0x4480 1304 0x4480 1404	**Instance**	CLK1_DSS_BW_REGULATOR CLK2_ISS_BW_REGULATOR CLK2_IVAHD_BW_REGULATOR
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STDHOSTHDR_VERSIONREG_REVISIONID								STDHOSTHDR_VERSIONREG_COREPARAMSCHECKSUM																									

Bits	Field Name	Description	Type	Reset
31:24	STDHOSTHDR_VERSIONREG_REVISIONID	The Revision Identifier field is a constant reporting the core generator revision number. Type: Constant. Reset value: 0x0.	R	0x00
23:0	STDHOSTHDR_VERSIONREG_COREPARAMSCHECKSUM	Reserved. Type: Reserved. Reset value: Reserved.	R	0x000000

Table 13-183. Register Call Summary for Register L3_BW_R_STDHOSTHDR_VERSIONREG

L3 Interconnect

- L3 BW Regulator Register Summary and Description: [0] [1]

Table 13-184. L3_BW_R_BANDWIDTH

Address Offset	See Table 13-178.		
Physical Address	0x4400 0708 0x4480 1308 0x4480 1408	**Instance**	CLK1_DSS_BW_REGULATOR CLK2_ISS_BW_REGULATOR CLK2_IVAHD_BW_REGULATOR
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																BANDWIDTH															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x0000
15:0	BANDWIDTH	Bandwidth, in bytes per second. Type: Control. Reset value: 0x0.	RW	0x0000

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Table 13-185. Register Call Summary for Register L3_BW_R_BANDWIDTH

L3 Interconnect

- Bandwidth Regulators: [0]
- L3 BW Regulator Register Summary and Description: [1] [2]

Table 13-186. L3_BW_R_WATERMARK

Address Offset	See Table 13-178.		
Physical Address	0x4400 070C 0x4480 130C 0x4480 140C	**Instance**	CLK1_DSS_BW_REGULATOR CLK2_ISS_BW_REGULATOR CLK2_IVAHD_BW_REGULATOR
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								WATERMARK							

Bits	Field Name	Description	Type	Reset
31:12	RESERVED	Reserved	R	0x00000
11:0	WATERMARK	Peak permissible bandwidth, in bytes. Type: Control. Reset value: 0x1.	RW	0x001

Table 13-187. Register Call Summary for Register L3_BW_R_WATERMARK

L3 Interconnect

- Bandwidth Regulators: [0] [1]
- L3 BW Regulator Register Summary and Description: [2] [3]

Table 13-188. L3_BW_R_PRESS

Address Offset	See Table 13-178.		
Physical Address	0x4400 0710 0x4480 1310 0x4480 1410	**Instance**	CLK1_DSS_BW_REGULATOR CLK2_ISS_BW_REGULATOR CLK2_IVAHD_BW_REGULATOR
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														PRESS_LOW	PRESS_HIGH

Bits	Field Name	Description	Type	Reset
31:2	RESERVED	Reserved	R	0x0000 0000
1	PRESS_LOW	Pressure value inserted if the measured bandwidth is over the watermark. The pressure is bar graph encoded. Type: Control. Reset value: 0x0.	R	0
0	PRESS_HIGH	Pressure value inserted if the measured bandwidth is under the watermark. The pressure is bar graph encoded. Type: Control. Reset value: 0x1.	R	1

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Table 13-189. Register Call Summary for Register L3_BW_R_PRESS

L3 Interconnect
- Bandwidth Regulators: [0]
- L3 BW Regulator Register Summary and Description: [1] [2]

Table 13-190. L3_BW_R_CLEARHISTORY

Address Offset	See Table 13-178.		
Physical Address	0x4400 0714 0x4480 1314 0x4480 1414	**Instance**	CLK1_DSS_BW_REGULATOR CLK2_ISS_BW_REGULATOR CLK2_IVAHD_BW_REGULATOR
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															CLEARHISTORY

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	CLEARHISTORY	Write a 1 clear the traffic counter Type: Give_AutoCleared. Reset value: 0x0.	RW	0

Table 13-191. Register Call Summary for Register L3_BW_R_CLEARHISTORY

L3 Interconnect
- Bandwidth Regulators: [0]
- L3 BW Regulator Register Summary and Description: [1] [2]

13.2.5.1.7 L3 Rate Adapt Register Summary and Description

Table 13-192. Rate Adapt Instance Summary

Module Name	Base Address	Size
CLK1_RATE_ADAPT_RESP_32TO128_CLK1	0x4400 0800	4KB
CLK2_RATE_ADAPT_RESP_32TO128_CLK2	0x4480 1200	4KB

13.2.5.1.7.1 L3 Rate Adapt Register Summary

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Table 13-193. Rate Adapt Register Summary

Register Name	Type	Register Width (Bits)	Address Offset for CLK1_RATE_ADAPT_RESP_32TO128_CLK1	CLK1_RATE_ADAPT_RESP_32TO128_CLK1 L3 Physical Address	Address Offset for CLK2_RATE_ADAPT_RESP_32TO128_CLK2	CLK2_RATE_ADAPT_RESP_32TO128_CLK2 L3 Physical Address
L3_RA_STDHOSTHDR_COREREG	R	32	0x0000 0800	0x4400 0800	0x0080 1200	0x4480 1200
L3_RA_STDHOSTHDR_VERSIONREG	R	32	0x0000 0804	0x4400 0804	0x0080 1204	0x4480 1204
L3_RA_CNF	RW	32	0x0000 0808	0x4400 0808	0x0080 1208	0x4480 1208

13.2.5.1.7.2 L3 Rate Adapt Register Description

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Table 13-194. L3_RA_STDHOSTHDR_COREREG

Address Offset	See Table 13-193.		
Physical Address	0x4400 0800 0x4480 1200	**Instance**	CLK1_RATE_ADAPT_RESP_32 TO128_CLK1 CLK2_RATE_ADAPT_RESP_32 TO128_CLK2
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								STDHOSTHDR_COREREG_CORECODE								RESERVED								STDHOSTHDR_COREREG_VENDORCODE							

Bits	Field Name	Description	Type	Reset
31:22	RESERVED	Reserved	R	0x000
21:16	STDHOSTHDR_COREREG_CORECODE	The Core Code field is a constant reporting a vendor-specific core generator code. Type: Constant. Reset value: 0x2D.	R	0x2D
15:1	RESERVED	Reserved	R	0x0000
0	STDHOSTHDR_COREREG_VENDORCODE	The Vendor Code field is a constant reporting the core generator vendor code. Type: Constant. Reset value: 0x1. Read 0x0: Third-party vendor. Read 0x1:	R	1

Table 13-195. Register Call Summary for Register L3_RA_STDHOSTHDR_COREREG

L3 Interconnect

- L3 Rate Adapt Register Summary and Description: [0]

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Table 13-196. L3_RA_STDHOSTHDR_VERSIONREG

Address Offset	See Table 13-193.		
Physical Address	0x4400 0804 0x4480 1204	**Instance**	CLK1_RATE_ADAPT_RESP_32 TO128_CLK1 CLK2_RATE_ADAPT_RESP_32 TO128_CLK2
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STDHOSTHDR_VERSIONREG_REVISIONID								STDHOSTHDR_VERSIONREG_COREPARAMSCHECKSUM																							

Bits	Field Name	Description	Type	Reset
31:24	STDHOSTHDR_VERSIONREG_REVISIONID	The Revision Identifier field is a constant reporting the core generator revision number. Type: Constant. Reset value: 0x0.	R	0x00
23:0	STDHOSTHDR_VERSIONREG_COREPARAMSCHECKSUM	Reserved. Type: Reserved. Reset value: Reserved.	R	0x000000

Table 13-197. Register Call Summary for Register L3_RA_STDHOSTHDR_VERSIONREG

L3 Interconnect

- L3 Rate Adapt Register Summary and Description: [0]

Table 13-198. L3_RA_CNF

Address Offset	See Table 13-193.		
Physical Address	0x4400 0808 0x4480 1208	**Instance**	CLK1_RATE_ADAPT_RESP_32 TO128_CLK1 CLK2_RATE_ADAPT_RESP_32 TO128_CLK2
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																											CNF_RATE				CNF_STANDFWD

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Bits	Field Name	Description	Type	Reset
31:5	RESERVED	Reserved	R	0x0000000
4:1	CNF_RATE	Indicates the throughput ratio between input and output (Rate = [16 x (Incoming_Throughput/Outgoing_Throuput)] - 1), when bit StAndFwd bit is reset. Ignored when StAndFwd bit is set. Type: Control. Reset value: 0x3.	RW	0x3
0	CNF_STANDFWD	When this bit is set, the Packet Transport Unit stores the entire NTTP packet, then forwards it on TX port. Type: Control. Reset value: 0x0.	RW	0

Table 13-199. Register Call Summary for Register L3_RA_CNF

L3 Interconnect

- L3 Rate Adapt Register Summary and Description: [0]

13.2.5.1.8 L3 STATCOLL Register Summary and Description

Table 13-200. STATCOLL Instance Summary

Module Name	Base Address	Size
CLK3_STATCOLL_SDRAM	0x4500 1000	512 bytes
CLK3_STATCOLL_LAT0	0x4500 2000	512 bytes
CLK3_STATCOLL_LAT1	0x4500 3000	512 bytes

13.2.5.1.8.1 L3 STATCOLL Register Summary

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Table 13-201. STATCOLL Register Summary

Register Name	Type	Register Width (Bits)	Address Offset for SDRAM	CLK3_STATCOLL_SDRAM L3 Physical Address	Address Offset for LAT0	CLK3_STATCOLL_LAT0 L3 Physical Address	Address Offset for LAT1	CLK3_STATCOLL_LAT1 L3 Physical Address
L3_STCOL_STDHOSTHDR_COREREG	R	32	0x0100 1000	0x4500 1000	0x0100 2000	0x4500 2000	0x0100 3000	0x4500 3000
L3_STCOL_STDHOSTHDR_VERSIONREG	R	32	0x0100 1004	0x4500 1004	0x0100 2004	0x4500 2004	0x0100 3004	0x4500 3004
L3_STCOL_EN	RW	32	0x0100 1008	0x4500 1008	0x0100 2008	0x4500 2008	0x0100 3008	0x4500 3008
L3_STCOL_SOFTEN	RW	32	0x0100 100C	0x4500 100C	0x0100 200C	0x4500 200C	0x0100 300C	0x4500 300C
L3_STCOL_TRIGEN	RW	32	0x0100 1014	0x4500 1014	0x0100 2014	0x4500 2014	0x0100 3014	0x4500 3014
L3_STCOL_REQEVT	RW	32	0x0100 1018	0x4500 1018	0x0100 2018	0x4500 2018	0x0100 3018	0x4500 3018
L3_STCOL_RSPEVT	RW	32	0x0100 101C	0x4500 101C	0x0100 201C	0x4500 201C	0x0100 301C	0x4500 301C
L3_STCOL_EVTMUX_SEL0	RW	32	0x0100 1020	0x4500 1020	0x0100 2020	0x4500 2020	0x0100 3020	0x4500 3020
L3_STCOL_EVTMUX_SEL1	RW	32	0x0100 1024	0x4500 1024	0x0100 2024	0x4500 2024	0x0100 3024	0x4500 3024
L3_STCOL_EVTMUX_SEL2	RW	32	0x0100 1028	0x4500 1028	0x0100 2028	0x4500 2028	0x0100 3028	0x4500 3028
L3_STCOL_EVTMUX_SEL3	RW	32	0x0100 102C	0x4500 102C	0x0100 202C	0x4500 202C	0x0100 302C	0x4500 302C
L3_STCOL_EVTMUX_SEL4	RW	32	0x0100 1030	0x4500 1030	N/A	N/A	N/A	N/A
L3_STCOL_DUMP_IDENTIFIER	R	32	0x0100 1040	0x4500 1040	0x0100 2040	0x4500 2040	0x0100 3040	0x4500 3040
L3_STCOL_DUMP_COLLECTTIME	RW	32	0x0100 1044	0x4500 1044	0x0100 2044	0x4500 2044	0x0100 3044	0x4500 3044
L3_STCOL_DUMP_SLVADDR	R	32	0x0100 1048	0x4500 1048	0x0100 2048	0x4500 2048	0x0100 3048	0x4500 3048
L3_STCOL_DUMP_MSTADDR	R	32	0x0100 104C	0x4500 104C	0x0100 204C	0x4500 204C	0x0100 304C	0x4500 304C
L3_STCOL_DUMP_SLVOFS	RW	32	0x0100 1050	0x4500 1050	0x0100 2050	0x4500 2050	0x0100 3050	0x4500 3050
L3_STCOL_DUMP_MANUAL	RW	32	0x0100 1054	0x4500 1054	0x0100 2054	0x4500 2054	0x0100 3054	0x4500 3054
L3_STCOL_DUMP_SEND	RW	32	0x0100 1058	0x4500 1058	0x0100 2058	0x4500 2058	0x0100 3058	0x4500 3058
L3_STCOL_FILTER_i_GLOBALEN	RW	32	0x0100 10AC	0x4500 10AC	0x0100 20AC	0x4500 20AC	0x0100 30AC	0x4500 30AC
L3_STCOL_FILTER_i_ADDRMIN	RW	32	0x0100 10B0	0x4500 10B0	N/A	N/A	N/A	N/A
L3_STCOL_FILTER_i_ADDRMAX	RW	32	0x0100 10B4	0x4500 10B4	N/A	N/A	N/A	N/A
L3_STCOL_FILTER_i_ADDREN	RW	32	0x0100 10B8	0x4500 10B8	N/A	N/A	N/A	N/A
L3_STCOL_FILTER_i_EN_k	RW	32	0x0100 10BC	0x4500 10BC	0x0100 20BC	0x4500 20BC	0x0100 30BC	0x4500 30BC
L3_STCOL_FILTER_i_MASK_m_MSTADDR	RW	32	0x0100 10C8	0x4500 10C8	0x0100 20C8	0x4500 20C8	0x0100 30C8	0x4500 30C8
L3_STCOL_FILTER_i_MASK_m_RD	RW	32	0x0100 10C0	0x4500 10C0	0x0100 20C0	0x4500 20C0	0x0100 30C0	0x4500 30C0
L3_STCOL_FILTER_i_MASK_m_WR	RW	32	0x0100 10C4	0x4500 10C4	0x0100 20C4	0x4500 20C4	0x0100 30C4	0x4500 30C4
L3_STCOL_FILTER_i_MASK_m_ERR	RW	32	0x0100 10D0	0x4500 10D0	0x0100 20D0	0x4500 20D0	0x0100 30D0	0x4500 30D0

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Table 13-201. STATCOLL Register Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset for SDRAM	CLK3_STATCOLL_ SDRAM L3 Physical Address	Address Offset for LAT0	CLK3_STATCOLL _LAT0 L3 Physical Address	Address Offset for LAT1	CLK3_STATCOLL_ LAT1 L3 Physical Address
L3_STCOL_FILTER_i_MASK_m_USERINFO	RW	32	0x0100 10D4	0x4500 10D4	N/A	N/A	N/A	N/A
L3_STCOL_FILTER_i_MATCH_m_MSTADDR	RW	32	0x0100 10E8	0x4500 10E8	0x0100 20E8	0x4500 20E8	0x0100 30E8	0x4500 30E8
L3_STCOL_FILTER_i_MATCH_m_RD	RW	32	0x0100 10E0	0x4500 10E0	0x0100 20E0	0x4500 20E0	0x0100 30E0	0x4500 30E0
L3_STCOL_FILTER_i_MATCH_m_WR	RW	32	0x0100 10E4	0x4500 10E4	0x0100 20E4	0x4500 20E4	0x0100 30E4	0x4500 30E4
L3_STCOL_FILTER_i_MATCH_m_ERR	RW	32	0x0100 10F0	0x4500 10F0	0x0100 20F0	0x4500 20F0	0x0100 30F0	0x4500 30F0
L3_STCOL_FILTER_i_MATCH_m_USERINFO	RW	32	0x0100 10F4	0x4500 10F4	N/A	N/A	N/A	N/A
L3_STCOL_OP_i_THRESHOLD_MINVAL	RW	32	0x0100 11F0	0x4500 11F0	0x0100 21F0	0x4500 21F0	0x0100 31F0	0x4500 31F0
L3_STCOL_OP_i_THRESHOLD_MAXVAL	RW	32	0x0100 11F4	0x4500 11F4	0x0100 21F4	0x4500 21F4	0x0100 31F4	0x4500 31F4
L3_STCOL_OP_i_EVTINFOSEL	RW	32	0x0100 11F8	0x4500 11F8	0x0100 21F8	0x4500 21F8	0x0100 31F8	0x4500 31F8
L3_STCOL_OP_i_SEL	RW	32	0x0100 11FC	0x4500 11FC	0x0100 21FC	0x4500 21FC	0x0100 31FC	0x4500 31FC

13.2.5.1.8.2 L3 STATCOLL Register Description

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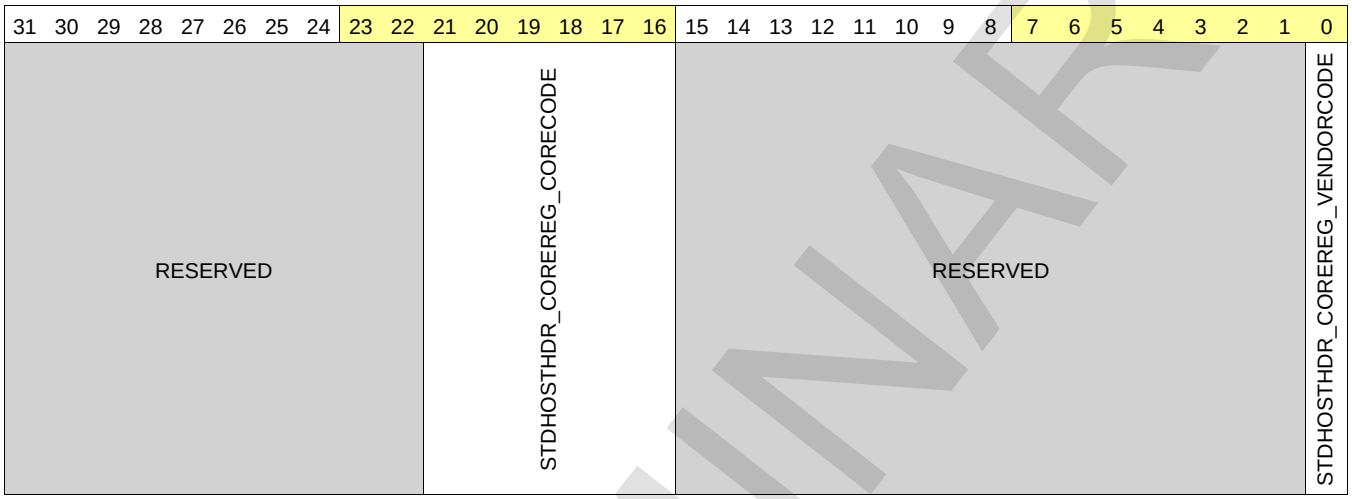
Table 13-202. L3_STCOL_STDHOSTHDR_COREREG

Address Offset	See Table 13-201.		
Physical Address	0x4500 1000 0x4500 2000 0x4500 3000	**Instance**	CLK3_STATCOLL_SDRAM CLK3_STATCOLL_LAT0 CLK3_STATCOLL_LAT1
Description			
Type	R		



Bits	Field Name	Description	Type	Reset
31:22	RESERVED	Reserved	R	0x000
21:16	STDHOSTHDR_COREREG_CORECODE	The Core Code field is a constant reporting a vendor-specific core generator code. Type: Constant. Reset value: 0x3A.	R	0x3A
15:1	RESERVED	Reserved	R	0x0000
0	STDHOSTHDR_COREREG_VENDORCODE	The Vendor Code field is a constant reporting the core generator vendor code. Type: Constant. Reset value: 0x1. Read 0x0: Third-party vendor. Read 0x1:	R	1

Table 13-203. Register Call Summary for Register L3_STCOL_STDHOSTHDR_COREREG

L3 Interconnect

- L3 STATCOLL Register Summary and Description: [0]

Table 13-204. L3_STCOL_STDHOSTHDR_VERSIONREG

Address Offset	See Table 13-201.		
Physical Address	0x4500 1004 0x4500 2004 0x4500 3004	**Instance**	CLK3_STATCOLL_SDRAM CLK3_STATCOLL_LAT0 CLK3_STATCOLL_LAT1
Description			
Type	R		

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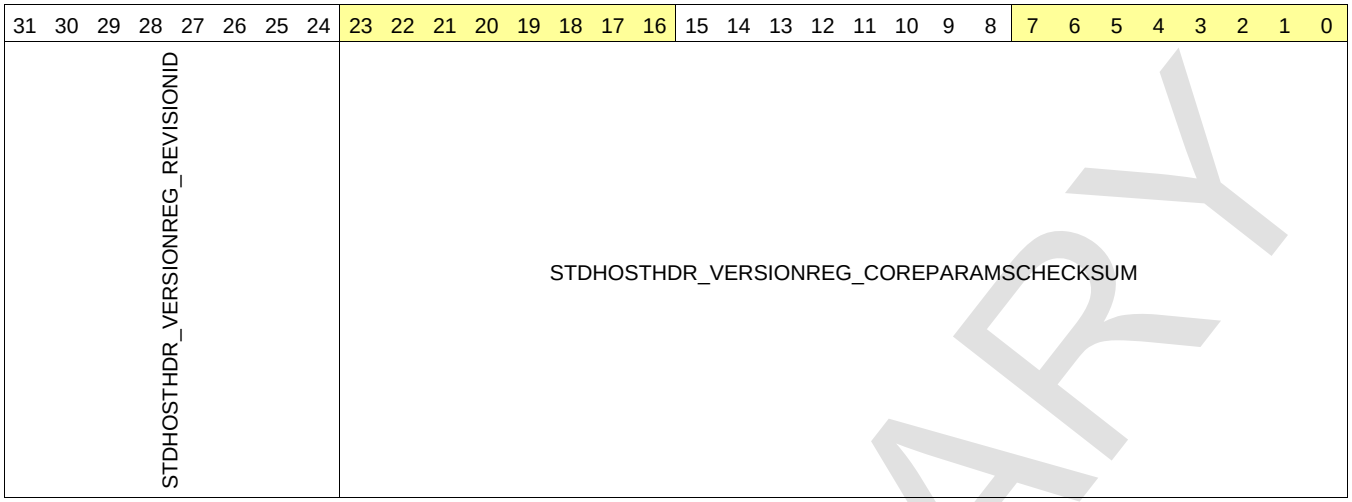


Bits	Field Name	Description	Type	Reset
31:24	STDHOSTHDR_VERSIONREG_REVISIONID	The Revision Identifier field is a constant reporting the core generator revision number. Type: Constant. Reset value: 0x0.	R	0x00
23:0	STDHOSTHDR_VERSIONREG_COREPARAMSCHECKSUM	Reserved. Type: Reserved. Reset value: Reserved.	R	0x000000

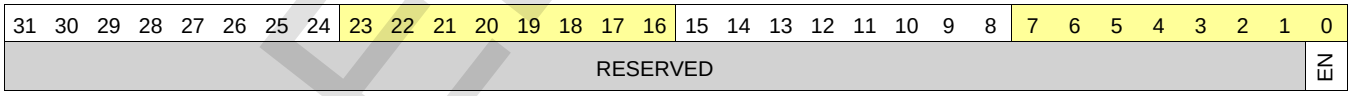
Table 13-205. Register Call Summary for Register L3_STCOL_STDHOSTHDR_VERSIONREG

L3 Interconnect

- L3 STATCOLL Register Summary and Description: [0]

Table 13-206. L3_STCOL_EN

Address Offset	See Table 13-201.		
Physical Address	0x4500 1008 0x4500 2008 0x4500 3008	**Instance**	CLK3_STATCOLL_SDRAM CLK3_STATCOLL_LAT0 CLK3_STATCOLL_LAT1
Description			
Type	RW		



Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	EN	Enable performance monitoring, this will also shut down the clock if En = 0 Type: Control. Reset value: 0x0.	RW	0

Table 13-207. Register Call Summary for Register L3_STCOL_EN

L3 Interconnect

- Statistic Collectors Group: [0]
- L3 STATCOLL Register Summary and Description: [1]

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Table 13-208. L3_STCOL_SOFTEN

Address Offset	See Table 13-201.		
Physical Address	0x4500 100C 0x4500 200C 0x4500 300C	**Instance**	CLK3_STATCOLL_SDRAM CLK3_STATCOLL_LAT0 CLK3_STATCOLL_LAT1
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															SOFTEN

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	SOFTEN	Software enable for performance monitoring Type: Control. Reset value: 0x0.	RW	0

Table 13-209. Register Call Summary for Register L3_STCOL_SOFTEN

L3 Interconnect

- Statistic Collectors Group: [0]
- L3 STATCOLL Register Summary and Description: [1]

Table 13-210. L3_STCOL_TRIGEN

Address Offset	See Table 13-201.		
Physical Address	0x4500 1014 0x4500 2014 0x4500 3014	**Instance**	CLK3_STATCOLL_SDRAM CLK3_STATCOLL_LAT0 CLK3_STATCOLL_LAT1
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															TRIGEN

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	TRIGEN	TrigEn when set, it enable the external trigger start and stop Type: Control. Reset value: 0x0.	RW	0

Table 13-211. Register Call Summary for Register L3_STCOL_TRIGEN

L3 Interconnect

- L3 STATCOLL Register Summary and Description: [0]

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Table 13-212. L3_STCOL_REQEVT

Address Offset	See Table 13-201.		
Physical Address	0x4500 1018 0x4500 2018 0x4500 3018	**Instance**	CLK3_STATCOLL_SDRAM CLK3_STATCOLL_LAT0 CLK3_STATCOLL_LAT1
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														REQEVT	

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved	R	0x0000000
3:0	REQEVT	Req event select Type: Control. Reset value: 0x0. 0x0: Collect is disabled default value 0x1: Collect all event: hit always (cycle) 0x2: Collect transfers: actually used cycle for transferring aN NTTP word 0x3: Collect wait cycle: transfer has been delayed by source 0x4: Collect busy: transfer has been delayed by destination 0x5: Collect packet: new packet start 0x6: Collect data: data cycle transfer, write for requests, read for responses 0x7: Collect idles: transfer is not initiated by source 0x8: Collect latency: hit when actually detecting debug bit on response links	RW	0x0

Table 13-213. Register Call Summary for Register L3_STCOL_REQEVT

L3 Interconnect

- Statistic Collectors Group: [0]
- L3 STATCOLL Register Summary and Description: [1]

Table 13-214. L3_STCOL_RSPEVT

Address Offset	See Table 13-201.		
Physical Address	0x4500 101C 0x4500 201C 0x4500 301C	**Instance**	CLK3_STATCOLL_SDRAM CLK3_STATCOLL_LAT0 CLK3_STATCOLL_LAT1
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														RSPEVT	

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Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved	R	0x0000000
3:0	RSPEVT	Rsp event select Type: Control. Reset value: 0x0. 0x0: Collect is disabled default value 0x1: Collect all event: hit always (cycle) 0x2: Collect transfers: actually used cycle for transferring a NTTP word 0x3: Collect wait cycle: transfer has been delayed by source 0x4: Collect busy: transfer has been delayed by destination 0x5: Collect packet: new packet start 0x6: Collect data: data cycle transfer, write for requests, read for responses 0x7: Collect idles: transfer is not initiated by source 0x8: Collect latency: hit when actually detecting debug bit on response links	RW	0x0

Table 13-215. Register Call Summary for Register L3_STCOL_RSPEVT

L3 Interconnect
- Statistic Collectors Group: [0]
- L3 STATCOLL Register Summary and Description: [1]

Table 13-216. L3_STCOL_EVTMUX_SEL0

Address Offset	See Table 13-201.		
Physical Address	0x4500 1020 0x4500 2020 0x4500 3020	**Instance**	CLK3_STATCOLL_SDRAM CLK3_STATCOLL_LAT0 CLK3_STATCOLL_LAT1
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														EVTMUX_SEL0	

Bits	Field Name	Description	Type	Reset
31:3	RESERVED	Reserved	R	0x0000 0000
2:0	EVTMUX_SEL0	The select of the mux 0 Type: Control. Reset value: 0x0.	RW	0x0

Table 13-217. Register Call Summary for Register L3_STCOL_EVTMUX_SEL0

L3 Interconnect
- Statistic Collectors Group: [0]
- L3 STATCOLL Register Summary and Description: [1]

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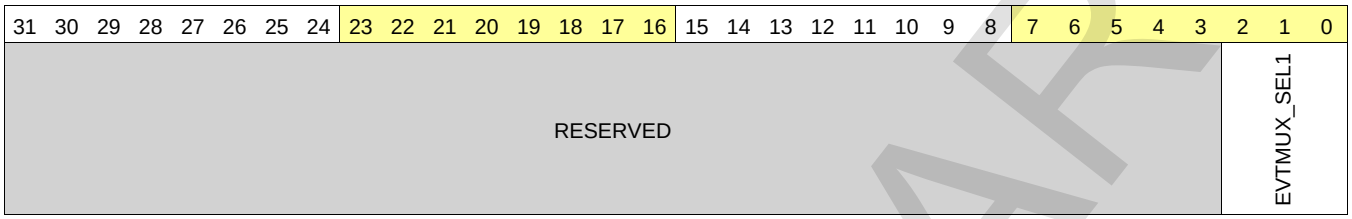
Table 13-218. L3_STCOL_EVTMUX_SEL1

Address Offset	See Table 13-201.		
Physical Address	0x4500 1024 0x4500 2024 0x4500 3024	**Instance**	CLK3_STATCOLL_SDRAM CLK3_STATCOLL_LAT0 CLK3_STATCOLL_LAT1
Description			
Type	RW		



Bits	Field Name	Description	Type	Reset
31:3	RESERVED	Reserved	R	0x0000 0000
2:0	EVTMUX_SEL1	The select of the mux 1 Type: Control. Reset value: 0x0.	RW	0x0

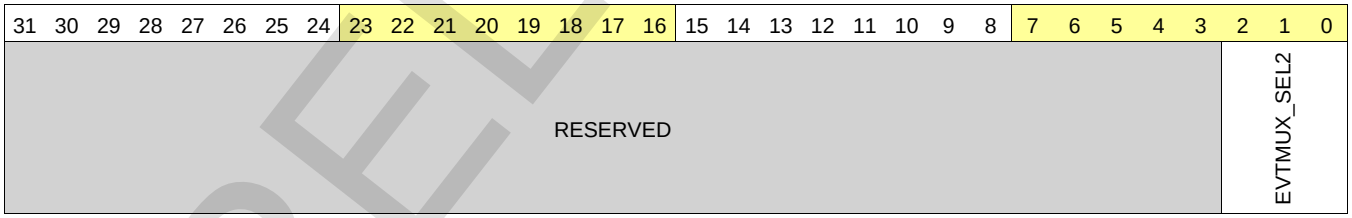
Table 13-219. Register Call Summary for Register L3_STCOL_EVTMUX_SEL1

L3 Interconnect

- L3 STATCOLL Register Summary and Description: [0]

Table 13-220. L3_STCOL_EVTMUX_SEL2

Address Offset	See Table 13-201.		
Physical Address	0x4500 1028 0x4500 2028 0x4500 3028	**Instance**	CLK3_STATCOLL_SDRAM CLK3_STATCOLL_LAT0 CLK3_STATCOLL_LAT1
Description			
Type	RW		



Bits	Field Name	Description	Type	Reset
31:3	RESERVED	Reserved	R	0x0000 0000
2:0	EVTMUX_SEL2	The select of the mux 2 Type: Control. Reset value: 0x0.	RW	0x0

Table 13-221. Register Call Summary for Register L3_STCOL_EVTMUX_SEL2

L3 Interconnect

- L3 STATCOLL Register Summary and Description: [0]

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Table 13-222. L3_STCOL_EVTMUX_SEL3

Address Offset	See Table 13-201.		
Physical Address	0x4500 102C 0x4500 202C 0x4500 302C	**Instance**	CLK3_STATCOLL_SDRAM CLK3_STATCOLL_LAT0 CLK3_STATCOLL_LAT1
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														EVTMUX_SEL3	

Bits	Field Name	Description	Type	Reset
31:3	RESERVED	Reserved	R	0x0000 0000
2:0	EVTMUX_SEL3	The select of the mux 3 Type: Control. Reset value: 0x0.	RW	0x0

Table 13-223. Register Call Summary for Register L3_STCOL_EVTMUX_SEL3

L3 Interconnect

- L3 STATCOLL Register Summary and Description: [0]

Table 13-224. L3_STCOL_EVTMUX_SEL4

Address Offset	See Table 13-201.		
Physical Address	0x4500 1030	**Instance**	CLK3_STATCOLL_SDRAM
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														EVTMUX_SEL4	

Bits	Field Name	Description	Type	Reset
31:3	RESERVED	Reserved	R	0x0000 0000
2:0	EVTMUX_SEL4	The select of the mux 4 Type: Control. Reset value: 0x0.	RW	0x0

Table 13-225. Register Call Summary for Register L3_STCOL_EVTMUX_SEL4

L3 Interconnect

- L3 STATCOLL Register Summary and Description: [0]

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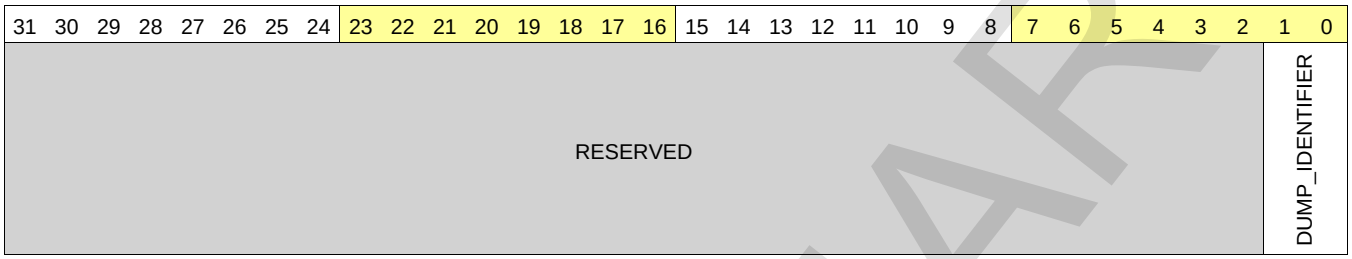
Table 13-226. L3_STCOL_DUMP_IDENTIFIER

Address Offset	See Table 13-201.		
Physical Address	0x4500 1040 0x4500 2040 0x4500 3040	**Instance**	CLK3_STATCOLL_SDRAM CLK3_STATCOLL_LAT0 CLK3_STATCOLL_LAT1
Description			
Type	R		



Bits	Field Name	Description	Type	Reset
31:2	RESERVED	Reserved	R	0x0000 0000
1:0	DUMP_IDENTIFIER	Probe identifier Type: Control. Reset value: 0x0.	R	0x0

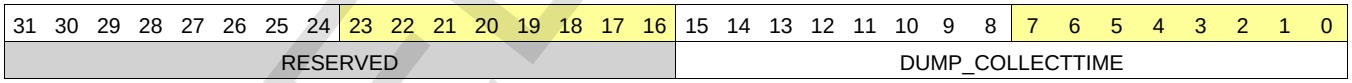
Table 13-227. Register Call Summary for Register L3_STCOL_DUMP_IDENTIFIER

L3 Interconnect

- L3 STATCOLL Register Summary and Description: [0]

Table 13-228. L3_STCOL_DUMP_COLLECTTIME

Address Offset	See Table 13-201.		
Physical Address	0x4500 1044 0x4500 2044 0x4500 3044	**Instance**	CLK3_STATCOLL_SDRAM CLK3_STATCOLL_LAT0 CLK3_STATCOLL_LAT1
Description			
Type	RW		



Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x0000
15:0	DUMP_COLLECTTIME	Number of cycle to wait between two statistics frame Type: Control. Reset value: 0x0.	RW	0x0000

Table 13-229. Register Call Summary for Register L3_STCOL_DUMP_COLLECTTIME

L3 Interconnect

- L3 STATCOLL Register Summary and Description: [0]

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Table 13-230. L3_STCOL_DUMP_SLVADDR

Address Offset	See Table 13-201.		
Physical Address	0x4500 1048 0x4500 2048 0x4500 3048	**Instance**	CLK3_STATCOLL_SDRAM CLK3_STATCOLL_LAT0 CLK3_STATCOLL_LAT1
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								DUMP_SLVADDR							

Bits	Field Name	Description	Type	Reset
31:5	RESERVED	Reserved	R	0x0000000
4:0	DUMP_SLVADDR	Dump slave address Type: Control. Reset value: 0x19.	R	0x19

Table 13-231. Register Call Summary for Register L3_STCOL_DUMP_SLVADDR

L3 Interconnect

- L3 STATCOLL Register Summary and Description: [0]

Table 13-232. L3_STCOL_DUMP_MSTADDR

Address Offset	See Table 13-201.		
Physical Address	0x4500 104C 0x4500 204C 0x4500 304C	**Instance**	CLK3_STATCOLL_SDRAM CLK3_STATCOLL_LAT0 CLK3_STATCOLL_LAT1
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								DUMP_MSTADDR							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Reserved	R	0x000000
7:0	DUMP_MSTADDR	Dump master address Type: Control. Reset value: 0xE0.	R	0xE0

Table 13-233. Register Call Summary for Register L3_STCOL_DUMP_MSTADDR

L3 Interconnect

- L3 STATCOLL Register Summary and Description: [0]

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Table 13-234. L3_STCOL_DUMP_SLVOFS

Address Offset	See Table 13-201.		
Physical Address	0x4500 1050 0x4500 2050 0x4500 3050	**Instance**	CLK3_STATCOLL_SDRAM CLK3_STATCOLL_LAT0 CLK3_STATCOLL_LAT1
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DUMP_SLVOFS																															

Bits	Field Name	Description	Type	Reset
31:0	DUMP_SLVOFS	Dump slave offset Type: Control. Reset value: 0x800.	RW	0x0000 0800

Table 13-235. Register Call Summary for Register L3_STCOL_DUMP_SLVOFS

L3 Interconnect

- L3 STATCOLL Register Summary and Description: [0]

Table 13-236. L3_STCOL_DUMP_MANUAL

Address Offset	See Table 13-201.		
Physical Address	0x4500 1054 0x4500 2054 0x4500 3054	**Instance**	CLK3_STATCOLL_SDRAM CLK3_STATCOLL_LAT0 CLK3_STATCOLL_LAT1
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															DUMP_MANUAL

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	DUMP_MANUAL	Define the dump mode: if != 0 the dump is controlled by the Send register. Type: Control. Reset value: 0x0.	RW	0

Table 13-237. Register Call Summary for Register L3_STCOL_DUMP_MANUAL

L3 Interconnect

- L3 STATCOLL Register Summary and Description: [0]

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Table 13-238. L3_STCOL_DUMP_SEND

Address Offset	See Table 13-201.		
Physical Address	0x4500 1058 0x4500 2058 0x4500 3058	**Instance**	CLK3_STATCOLL_SDRAM CLK3_STATCOLL_LAT0 CLK3_STATCOLL_LAT1
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															DUMP_SEND

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	DUMP_SEND	In manual mode, is used to send the dump content and initialize the counters. Type: Give_AutoCleared. Reset value: 0x0. • Dumping can be performed only if monitoring is enabled • For “one shot metrics dump” the DUMP_SEND command has to be issued before disabling monitoring	RW	0

Table 13-239. Register Call Summary for Register L3_STCOL_DUMP_SEND

L3 Interconnect

- L3 STATCOLL Register Summary and Description: [0]

Table 13-240. L3_STCOL_FILTER_i_GLOBALEN

Address Offset	See Table 13-201.		
Physical Address	0x4500 10AC 0x4500 20AC 0x4500 30AC	**Instance**	CLK3_STATCOLL_SDRAM CLK3_STATCOLL_LAT0 CLK3_STATCOLL_LAT1
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															FILTER_i_GLOBALEN

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	FILTER_i_GLOBALEN	Filter global enable Type: Control. Reset value: 0x0.	RW	0

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Table 13-241. Register Call Summary for Register L3_STCOL_FILTER_i_GLOBALEN

L3 Interconnect

- L3 STATCOLL Register Summary and Description: [0]

Table 13-242. L3_STCOL_FILTER_i_ADDRMIN

Address Offset	See Table 13-201		
Physical Address	0x4500 10B0	**Instance**	CLK3_STATCOLL_SDRAM
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								FILTER1_ADDRMIN																							

Bits	Field Name	Description	Type	Reset
31:23	RESERVED	Reserved	R	0bxxxxxxxxx
22:0	FILTER1_ADDRMIN	min addr range Type: Control. Reset value: 0x0.	RW	0x000000

Table 13-243. Register Call Summary for Register L3_STCOL_FILTER_i_ADDRMIN

L3 Interconnect

- L3 STATCOLL Register Summary and Description: [0]

Table 13-244. L3_STCOL_FILTER_i_ADDRMAX

Address Offset	See Table 13-201		
Physical Address	0x4500 10B4	**Instance**	CLK3_STATCOLL_SDRAM
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								FILTER1_ADDRMAX																							

Bits	Field Name	Description	Type	Reset
31:23	RESERVED	Reserved	R	0bxxxxxxxxx
22:0	FILTER1_ADDRMAX	max addr range Type: Control. Reset value: 0x0.	RW	0x000000

Table 13-245. Register Call Summary for Register L3_STCOL_FILTER_i_ADDRMAX

L3 Interconnect

- L3 STATCOLL Register Summary and Description: [0]

Table 13-246. L3_STCOL_FILTER_i_ADDREN

Address Offset	See Table 13-201		
Physical Address	0x4500 10B8	**Instance**	CLK3_STATCOLL_SDRAM
Description			
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															FILTER1_ADDREN

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0bxxxxxxxxxxxxxxxx xxxxxxxxxxxxxx
0	FILTER1_ADDREN	max filtering enable Type: Control. Reset value: 0x0.	RW	0

Table 13-247. Register Call Summary for Register L3_STCOL_FILTER_i_ADDREN

L3 Interconnect

- L3 STATCOLL Register Summary and Description: [0]

Table 13-248. L3_STCOL_FILTER_i_EN_k

Address Offset	See Table 13-201.		
Physical Address	0x4500 10BC 0x4500 20BC 0x4500 30BC	**Instance**	CLK3_STATCOLL_SDRAM CLK3_STATCOLL_LAT0 CLK3_STATCOLL_LAT1
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															FILTER_i_EN0

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	FILTER_i_EN0	Enable filter stage 0 Type: Control. Reset value: 0x0.	RW	0

Table 13-249. Register Call Summary for Register L3_STCOL_FILTER_i_EN_k

L3 Interconnect

- L3 STATCOLL Register Summary and Description: [0]

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Table 13-250. L3_STCOL_FILTER_i_MASK_m_MSTADDR

Address Offset	See Table 13-201.		
Physical Address	0x4500 10C8 0x4500 20C8 0x4500 30C8	**Instance**	CLK3_STATCOLL_SDRAM CLK3_STATCOLL_LAT0 CLK3_STATCOLL_LAT1
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								FILTER_i_MASK_m_MSTADDR							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Reserved	R	0x000000
7:0	FILTER_i_MASK_m_MSTADDR	Mask/Match of MstAddr Type: Control. Reset value: 0x0.	RW	0x00

Table 13-251. Register Call Summary for Register L3_STCOL_FILTER_i_MASK_m_MSTADDR

L3 Interconnect

- L3 STATCOLL Register Summary and Description: [0]

Table 13-252. L3_STCOL_FILTER_i_MASK_m_RD

Address Offset	See Table 13-201.		
Physical Address	0x4500 10C0 0x4500 20C0 0x4500 30C0	**Instance**	CLK3_STATCOLL_SDRAM CLK3_STATCOLL_LAT0 CLK3_STATCOLL_LAT1
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															FILTER_i_MASK_m_RD

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	FILTER_i_MASK_m_RD	Mask/Match of Rd Type: Control. Reset value: 0x0.	RW	0

Table 13-253. Register Call Summary for Register L3_STCOL_FILTER_i_MASK_m_RD

L3 Interconnect

- L3 STATCOLL Register Summary and Description: [0]

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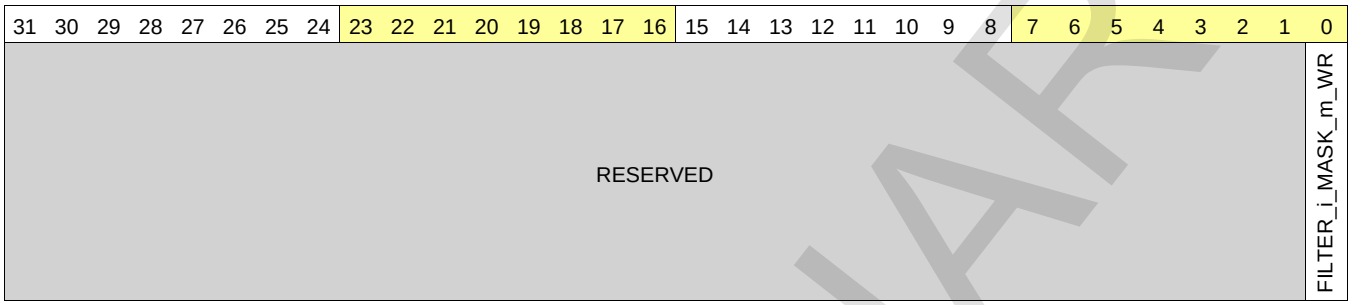
Table 13-254. L3_STCOL_FILTER_i_MASK_m_WR

Address Offset	See Table 13-201.		
Physical Address	0x4500 10C4 0x4500 20C4 0x4500 30C4	**Instance**	CLK3_STATCOLL_SDRAM CLK3_STATCOLL_LAT0 CLK3_STATCOLL_LAT1
Description			
Type	RW		



Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	FILTER_i_MASK_m_WR	Mask/Match of Wr Type: Control. Reset value: 0x0.	RW	0

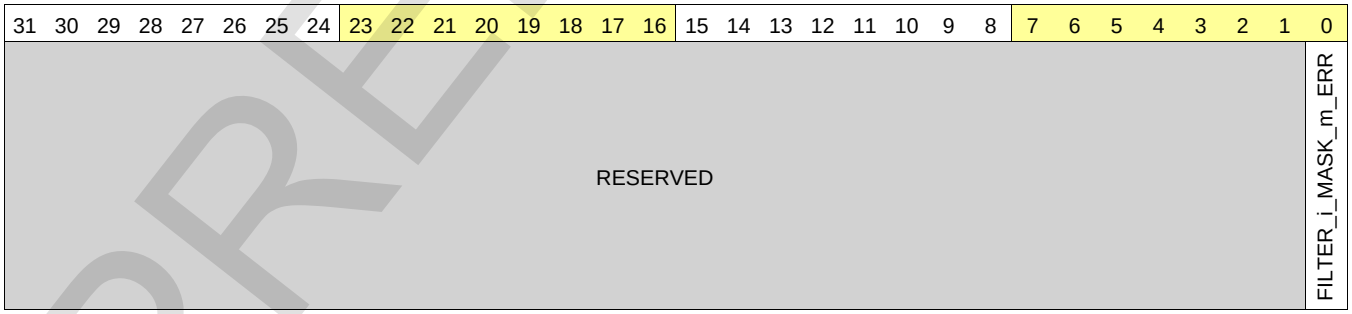
Table 13-255. Register Call Summary for Register L3_STCOL_FILTER_i_MASK_m_WR

L3 Interconnect

- L3 STATCOLL Register Summary and Description: [0]

Table 13-256. L3_STCOL_FILTER_i_MASK_m_ERR

Address Offset	See Table 13-201.		
Physical Address	0x4500 10D0 0x4500 20D0 0x4500 30D0	**Instance**	CLK3_STATCOLL_SDRAM CLK3_STATCOLL_LAT0 CLK3_STATCOLL_LAT1
Description			
Type	RW		



Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	FILTER_i_MASK_m_ERR	Mask/Match of Err Type: Control. Reset value: 0x0.	RW	0

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Table 13-257. Register Call Summary for Register L3_STCOL_FILTER_i_MASK_m_ERR

L3 Interconnect

- L3 STATCOLL Register Summary and Description: [0]

Table 13-258. L3_STCOL_FILTER_i_MASK_m_USERINFO

Address Offset	See Table 13-201.		
Physical Address	0x4500 10D4	**Instance**	CLK3_STATCOLL_SDRAM
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																FILTER_i_MASK_m_USERINFO															

Bits	Field Name	Description	Type	Reset
31:18	RESERVED	Reserved	R	0x0000
17:0	FILTER_i_MASK_m_USERINFO	Mask/Match of UserInfo Type: Control. Reset value: 0x0.	RW	0x00000

Table 13-259. Register Call Summary for Register L3_STCOL_FILTER_i_MASK_m_USERINFO

L3 Interconnect

- L3 STATCOLL Register Summary and Description: [0]

Table 13-260. L3_STCOL_FILTER_i_MATCH_m_MSTADDR

Address Offset	See Table 13-201.		
Physical Address	0x4500 10E8 0x4500 20E8 0x4500 30E8	**Instance**	CLK3_STATCOLL_SDRAM CLK3_STATCOLL_LAT0 CLK3_STATCOLL_LAT1
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								FILTER_i_MATCH_m_MSTADDR							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Reserved	R	0x000000
7:0	FILTER_i_MATCH_m_MSTADDR	Mask/Match of MstAddr Type: Control. Reset value: 0x0.	RW	0x00

Table 13-261. Register Call Summary for Register L3_STCOL_FILTER_i_MATCH_m_MSTADDR

L3 Interconnect

- L3 STATCOLL Register Summary and Description: [0]

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Table 13-262. L3_STCOL_FILTER_i_MATCH_m_RD

Address Offset	See Table 13-201.		
Physical Address	0x4500 10E0 0x4500 20E0 0x4500 30E0	**Instance**	CLK3_STATCOLL_SDRAM CLK3_STATCOLL_LAT0 CLK3_STATCOLL_LAT1
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															FILTER_i_MATCH_m_RD

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	FILTER_i_MATCH_m_RD	Mask/Match of Rd Type: Control. Reset value: 0x0.	RW	0

Table 13-263. Register Call Summary for Register L3_STCOL_FILTER_i_MATCH_m_RD

L3 Interconnect

- L3 STATCOLL Register Summary and Description: [0]

Table 13-264. L3_STCOL_FILTER_i_MATCH_m_WR

Address Offset	See Table 13-201.		
Physical Address	0x4500 10E4 0x4500 20E4 0x4500 30E4	**Instance**	CLK3_STATCOLL_SDRAM CLK3_STATCOLL_LAT0 CLK3_STATCOLL_LAT1
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															FILTER_i_MATCH_m_WR

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	FILTER_i_MATCH_m_WR	Mask/Match of Wr Type: Control. Reset value: 0x0.	RW	0

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Table 13-265. Register Call Summary for Register L3_STCOL_FILTER_i_MATCH_m_WR

L3 Interconnect

- L3 STATCOLL Register Summary and Description: [0]

Table 13-266. L3_STCOL_FILTER_i_MATCH_m_ERR

Address Offset	See Table 13-201.		
Physical Address	0x4500 10F0 0x4500 20F0 0x4500 30F0	**Instance**	CLK3_STATCOLL_SDRAM CLK3_STATCOLL_LAT0 CLK3_STATCOLL_LAT1
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															FILTER_i_MATCH_m_ERR

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	FILTER_i_MATCH_m_ERR	Mask/Match of Err Type: Control. Reset value: 0x0.	RW	0

Table 13-267. Register Call Summary for Register L3_STCOL_FILTER_i_MATCH_m_ERR

L3 Interconnect

- L3 STATCOLL Register Summary and Description: [0]

Table 13-268. L3_STCOL_FILTER_i_MATCH_m_USERINFO

Address Offset	See Table 13-201.		
Physical Address	0x4500 10F4	**Instance**	CLK3_STATCOLL_SDRAM
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																FILTER_i_MATCH_m_USERINFO															

Bits	Field Name	Description	Type	Reset
31:18	RESERVED	Reserved	R	0x0000
17:0	FILTER_i_MATCH_m_USERINFO	Mask/Match of UserInfo Type: Control. Reset value: 0x0.	RW	0x00000

Table 13-269. Register Call Summary for Register L3_STCOL_FILTER_i_MATCH_m_USERINFO

L3 Interconnect

- L3 STATCOLL Register Summary and Description: [0]

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Table 13-270. L3_STCOL_OP_i_THRESHOLD_MINVAL

Address Offset	See Table 13-201.		
Physical Address	0x4500 11F0 0x4500 21F0 0x4500 31F0	**Instance**	CLK3_STATCOLL_SDRAM CLK3_STATCOLL_LAT0 CLK3_STATCOLL_LAT1
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				OP_i_THRESHOLD_MINVAL											

Bits	Field Name	Description	Type	Reset
31:12	RESERVED	Reserved	R	0x00000
11:0	OP_i_THRESHOLD_MINVAL	Min value Type: Control. Reset value: 0x0.	RW	0x000

Table 13-271. Register Call Summary for Register L3_STCOL_OP_i_THRESHOLD_MINVAL

L3 Interconnect

- L3 STATCOLL Register Summary and Description: [0]

Table 13-272. L3_STCOL_OP_i_THRESHOLD_MAXVAL

Address Offset	See Table 13-201.		
Physical Address	0x4500 11F4 0x4500 21F4 0x4500 31F4	**Instance**	CLK3_STATCOLL_SDRAM CLK3_STATCOLL_LAT0 CLK3_STATCOLL_LAT1
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				OP_i_THRESHOLD_MAXVAL											

Bits	Field Name	Description	Type	Reset
31:12	RESERVED	Reserved	R	0x00000
11:0	OP_i_THRESHOLD_MAXVAL	Max value Type: Control. Reset value: 0x0.	RW	0x000

Table 13-273. Register Call Summary for Register L3_STCOL_OP_i_THRESHOLD_MAXVAL

L3 Interconnect

- L3 STATCOLL Register Summary and Description: [0]

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Table 13-274. L3_STCOL_OP_i_EVTINFOSEL

Address Offset	See Table 13-201.		
Physical Address	0x4500 11F8 0x4500 21F8 0x4500 31F8	**Instance**	CLK3_STATCOLL_SDRAM CLK3_STATCOLL_LAT0 CLK3_STATCOLL_LAT1
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														OP_i_EVTINFOSEL	

Bits	Field Name	Description	Type	Reset
31:2	RESERVED	Reserved	R	0x0000 0000
1:0	OP_i_EVTINFOSEL	Select event info data to add to counter (len/press or latency) Type: Control. Reset value: 0x0. 0x0: Select len from event info list 0x1: Select pressure if available from event info list 0x2: Select latency if available from event info list	RW	0x0

Table 13-275. Register Call Summary for Register L3_STCOL_OP_i_EVTINFOSEL

L3 Interconnect

- L3 STATCOLL Register Summary and Description: [0]

Table 13-276. L3_STCOL_OP_i_SEL

Address Offset	See Table 13-201.		
Physical Address	0x4500 11FC 0x4500 21FC 0x4500 31FC	**Instance**	CLK3_STATCOLL_SDRAM CLK3_STATCOLL_LAT0 CLK3_STATCOLL_LAT1
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												OP_i_SEL			

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Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved	R	0x0000000
3:0	OP_i_SEL	Select logical operation Type: Control. Reset value: 0x0. 0x0: Increment counter on each mask/match filter hit 0x1: Increment counter on each min/max level hit 0x2: Add to counter the selected event info value (len/press or latency) 0x3: increment counter when all filter event hits (And(Fi)) 0x4: Increment counter if any of filter event hits (Or(Fi)) 0x5: Add to counter the number of current request event that hit 0x6: Add to counter the number of current response event that hit 0x7: Add to counter the number of all event that hit 0x8:Increment counter on each selected external event hit	RW	0x0

Table 13-277. Register Call Summary for Register L3_STCOL_OP_i_SEL

L3 Interconnect

- L3 STATCOLL Register Summary and Description: [0]

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13.3 L4 Interconnects

This section details the device L4 interconnects.

13.3.1 L4 Interconnect Overview

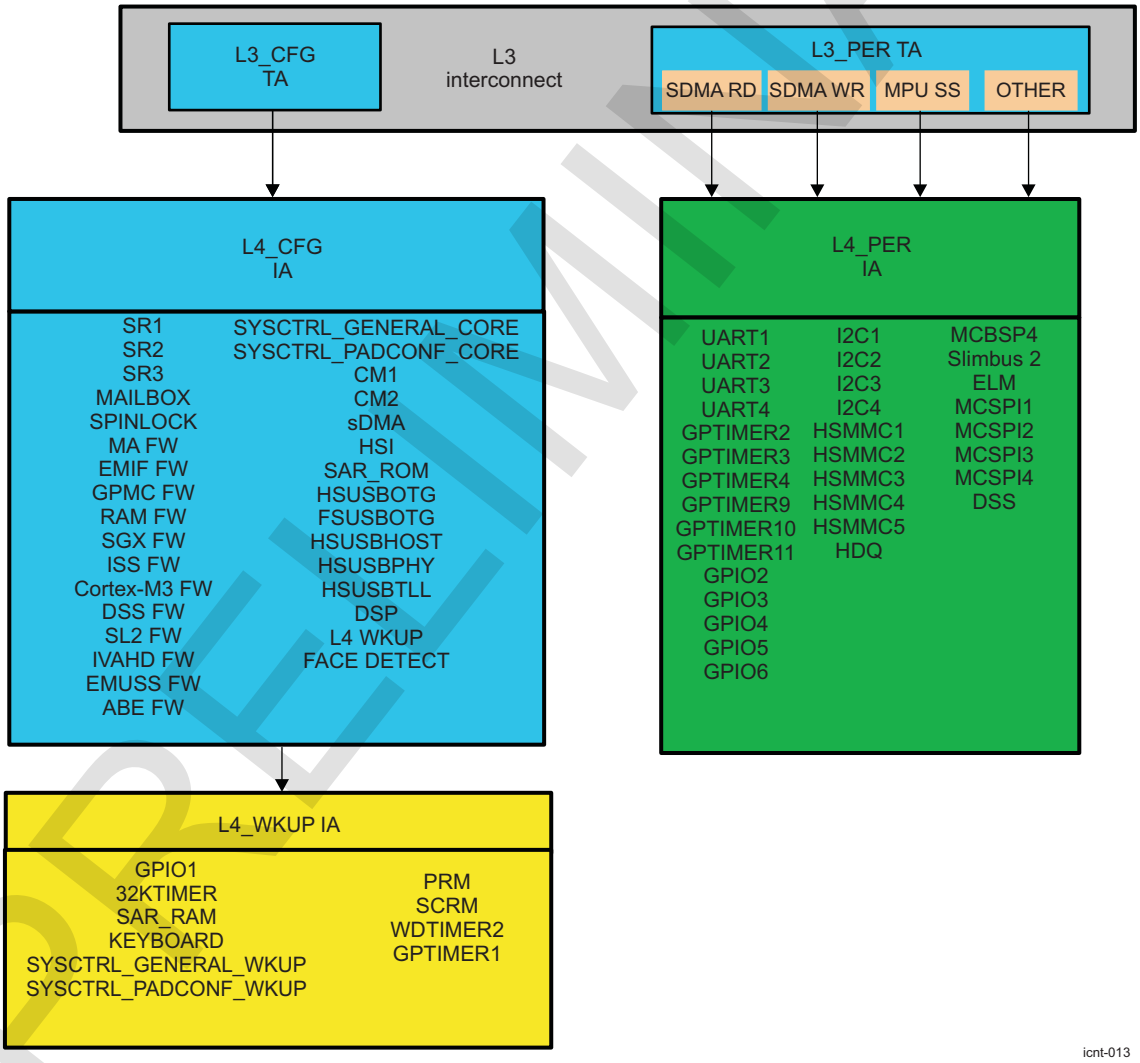
The device uses three separate L4 interconnect structures to connect peripheral modules. All L4s handle transfers with peripherals but are located in distinct power domains.

Figure 13-8 is an overview of the L4 interconnects and the peripherals attached to them.

The L4 interconnect is composed of the following interconnects:

- L4_CFG: Includes the majority of the configuration interface for L3 system modules and peripheral interconnect
- L4_PER: Includes the main peripherals that require sDMA access
- L4_WKUP: Includes peripherals attached to the WKUP power domain

Figure 13-8. L4 Interconnect Overview



The main features of the L4 interconnects are:

- From one to four 32-bit initiator ports for each L4 interconnect instance.
- 8-, 16-, or 32-bit data, single, or burst transactions
- Little endian

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- Nonblocking architecture with fair arbitration between threads
- Target interfaces: Fully synchronous or divided synchronous
- L4_CFG and L4_PER frequency equal half of L3 frequency
- Protection logic that provides user-configurable access control to targets by each initiator
- Implementation of RFFs to support low-voltage dynamic power switching

13.3.2 L4 Interconnect Integration

Table 13-278 and Table 13-279 summarize the integration of the module in the device.

Table 13-278. Integration Attributes

Module Instance	Attributes
	Power Domain
L4_PER	PD_L4_PER
L4_CFG	PD_CORE
L4_WKUP	PD_WKUP

Table 13-279. Clocks and Resets

Clocks				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
L4_PER	L4_PER_CLK	PER_L4_ICLK	PRCM module	Functional and interface clock
L4_CFG	L4_CFG_CLK	CFG_L4_ICLK	PRCM module	Functional and interface clock
L4_WKUP	L4_WKUP_CLK	WKUP_L4_ICLK2	PRCM module	Functional and interface clock
Resets				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
L4_PER	L4_PER_RST	L4_PER_RST	PRCM module	Reset of L4_PER interconnect
	L4_PER_RET_RST	L4_PER_RET_RST	PRCM module	Reset of L4_PER interconnect retention registers. For information about retention reset, see Chapter 3, *Power, Reset, and Clock Management*.
L4_CFG	L4_CFG_RST	CORE_RST	PRCM module	Reset of L4_CFG interconnect
	L4_CFG_RET_RST	CORE_RET_RST	PRCM module	Reset of L4_CFG interconnect retention registers. For information about retention reset, see Chapter 3, *Power, Reset, and Clock Management*.
L4_WKUP	L4_WKUP_RST	WKUP_RST	PRCM module	Reset of L4_WKUP interconnect

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13.3.3 L4 Interconnect Functional Description

13.3.3.1 Module Distribution

IAs and TAs provide the interface to connect the different modules to their associated interconnect.

Table 13-280 through Table 13-285 list all the modules and subsystems with their associated agents. The agents are listed for each L4 interconnect domain.

13.3.3.1.1 L4_PER Interconnect Agents

The L4_PER interconnect handles transfers only to peripherals in the PER power domain. Table 13-280 lists the PER TAs.

Table 13-280. L4 PER TAs

Module Target Name	Description
PER_TA_UART1	UART port 1 module
PER_TA_UART2	UART port 2 module
PER_TA_UART3	UARTport 3 module
PER_TA_UART4	UART port 4 module
PER_TA_GPTIMER2	GPTIMER2 module
PER_TA_GPTIMER3	GPTIMER3 module
PER_TA_GPTIMER4	GPTIMER4 module
PER_TA_GPTIMER9	GPTIMER9 module
PER_TA_GPTIMER10	GPTIMER10 module
PER_TA_GPTIMER11	GPTIMER11 module
PER_TA_DSS	Display subsystem configuration module
PER_TA_GPIO2	General-purpose input/output 2 (GPIO2) module
PER_TA_GPIO3	GPIO3 module
PER_TA_GPIO4	GPIO4 module
PER_TA_GPIO5	GPIO5 module
PER_TA_GPIO6	GPIO6 module
PER_TA_I2C1	I2C1 module
PER_TA_I2C2	Multimaster I2C2 module
PER_TA_I2C3	Multimaster I2C3 module
PER_TA_I2C4	Multimaster I2C4 module
PER_TA_SLIMBUS2	Silmbus 2 module
PER_TA_ELM	Error location module
PER_TA_MCBSP4	McBSP4 module
PER_TA_MCSPI1	McSPI1 module
PER_TA_MCSPI2	MCSPI2 module
PER_TA_MCSPI3	MCSPI3 module
PER_TA_MCSPI4	MCSPI4 module
PER_TA_HSMMC1	MMC controller 1 module
PER_TA_HSMMC2	MMC controller 2 module
PER_TA_HSMMC3	MMC controller 3 module
PER_TA_HSMMC4	MMC controller 4 module
PER_TA_HSMMC5	MMC controller 5 module
PER_TA_HDQ	Single-wire serial link low-rate module

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Four ports communicate between the L3 interconnect and the L4_PER interconnect to allow the L3 initiators to access the L4_PER targets. Table 13-281 lists the L4_PER initiator TAs.

For the list of initiators authorized to access the L4 peripheral peripherals, see , *Connectivity Matrix*.

Table 13-281. L4_PER IAs

Module Iniator Name	Description
PER_IA_0	L3 system direct memory access (sDMA) RD interconnect port
PER_IA_1	L3 sDMA WR interconnect port
PER_IA_2	L3 MPU susbystem interconnect port
PER_IA_3	L3 others interconnect port

13.3.3.1.2 L4_CFG Interconnect Agents

The L4_CFG interconnect handles only transfers to peripherals in the core power domain. Table 13-282 lists the TAs.

Table 13-282. L4_CFG TAs

Module Target Name	Description
CFG_TA_SYSCTRL_GENERAL_CORE	System control general core module
CFG_TA_SYSCTRL_PADCONF_CORE	System control padconf core module
CFG_TA_CM1	Clock manager 1 module
CFG_TA_CM2	Clock manager 1 module
CFG_TA_SDMA	sDMA module
CFG_TA_HSI	HS SSI module
CFG_TA_SAR_ROM	Save-and-restore ROM
CFG_TA_HSUSBOTG	HS USB OTG module
CFG_TA_FSUSBHOST	FS USB OTG module
CFG_TA_HSUSBHOST	HS USB host module
CFG_TA_HSUSBPHY	HS USB PHY module
CFG_TA_HSUSBTLL	USB TTL module
CFG_TA_DSP	DSP subsystem
CFG_TA_SR1	SmartReflex1 module
CFG_TA_SR2	SmartReflex2 module
CFG_TA_SR3	SmartReflex3 module
CFG_TA_MAILBOX	Mailbox module
CFG_TA_SPINLOCK	Spinlock module
CFG_TA_FACEDETECT	Face detect module
CFG_TA_MAFW	Memory Adapter firewall
CFG_TA_EMIFFW	EMIF firewall
CFG_TA_GPMCFW	GPMC firewall
CFG_TA_OCMRAMFW	RAM firewall
CFG_TA_SGXFW	SGX firewall
CFG_TA_ISSFW	ISS firewall
CFG_TA_CORTEXM3FW	Cortex-M3 firewall
CFG_TA_DSSFW	Dispay subsystem (DSS) firewall
CFG_TA_SL2FW	SL2 firewall
CFG_TA_IVAHDFW	IVA-HD firewall
CFG_TA_EMUSSFW	EMU subsystem firewall
CFG_TA_ABEFW	ABE firewall
CFG_TA_L4WKUP	L4_WKUP connection

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A unique port, CFG_IA_0, communicates between the L3 interconnect and the L4_CFG interconnect to allow the L3 initiators to access the L4_CFG targets (see Table 13-283).

For the list of initiators authorized to access the L4_CFG peripherals, see , *Connectivity Matrix*.

Table 13-283. L4_CFG IAs

Module Iniator Name	Description
CFG_IA_0	L3 interconnect port

13.3.3.1.3 L4_WKUP Interconnect Agents

The L4-WKUP interconnect handles transfers only to peripherals in the WKUP power domain. Table 13-284 lists the TAs. Table 13-285 lists the L4 WKUP initiator agents.

Table 13-284. L4_WKUP TAs

Module Target Name	Description
WKUP_TA_GPIO1	GPIO1 module
WKUP_TA_32KTIMER	32-kHz timer module
WKUP_TA_SAR_RAM	Save-and-restore RAM
WKUP_TA_KEYBOARD	Keyboard module
WKUP_TA_SYSCTRL_GENERAL_WKUP	System control general WKUP module
WKUP_TA_SYSCTRL_PADCONF_WKUP	System control padconf WKUP module
WKUP_TA_PRM	Power reset management module
WKUP_TA_SCRM	System clock and reset management module
WKUP_TA_WDTIMER2	WDTIMER2 module
WKUP_TA_GPTIMER1	GPTIMER1 module

Table 13-285. L4_WKUP IAs

Module Iniator Name	Description
WKUP_IA_0	L4_CFG interconnect port

13.3.3.2 Power Management

As part of the system-wide power-management scheme, the L4 interconnects go into IDLE state after receiving a request from the PRCM module after all commands are serviced. This function is handled by hardware. For more information, see Chapter 3, *Power, Reset, and Clock Management*.

To reduce power consumption, each L4 interconnect automatically performs internal clock autogating. This is managed by hardware; no software configurations or settings are required.

Retention is performed on all software-accessible registers at IAs, TAs, and firewalls. This process prevents reconfiguration after a clock domain switches off. For more information, see Chapter 3, *Power, Reset, and Clock Management*.

13.3.3.3 L4 Firewalls

Figure 13-9 is an internal view of the L4 interconnects in the overall interconnect. This architecture, with one initiator subsystem centralizing all initiator master requests and distributing them to all target modules (peripherals), enables the L4 interconnect firewall functions to be centralized at the L4 initiator subsystem level. The L4 firewall filters the accesses based on the configurable protection groups defined in the L4 address protection (AP) registers. Each module or TA is assigned to a protection group. The configuration is also defined in the L4 AP and is programmable on a module-per-module basis.

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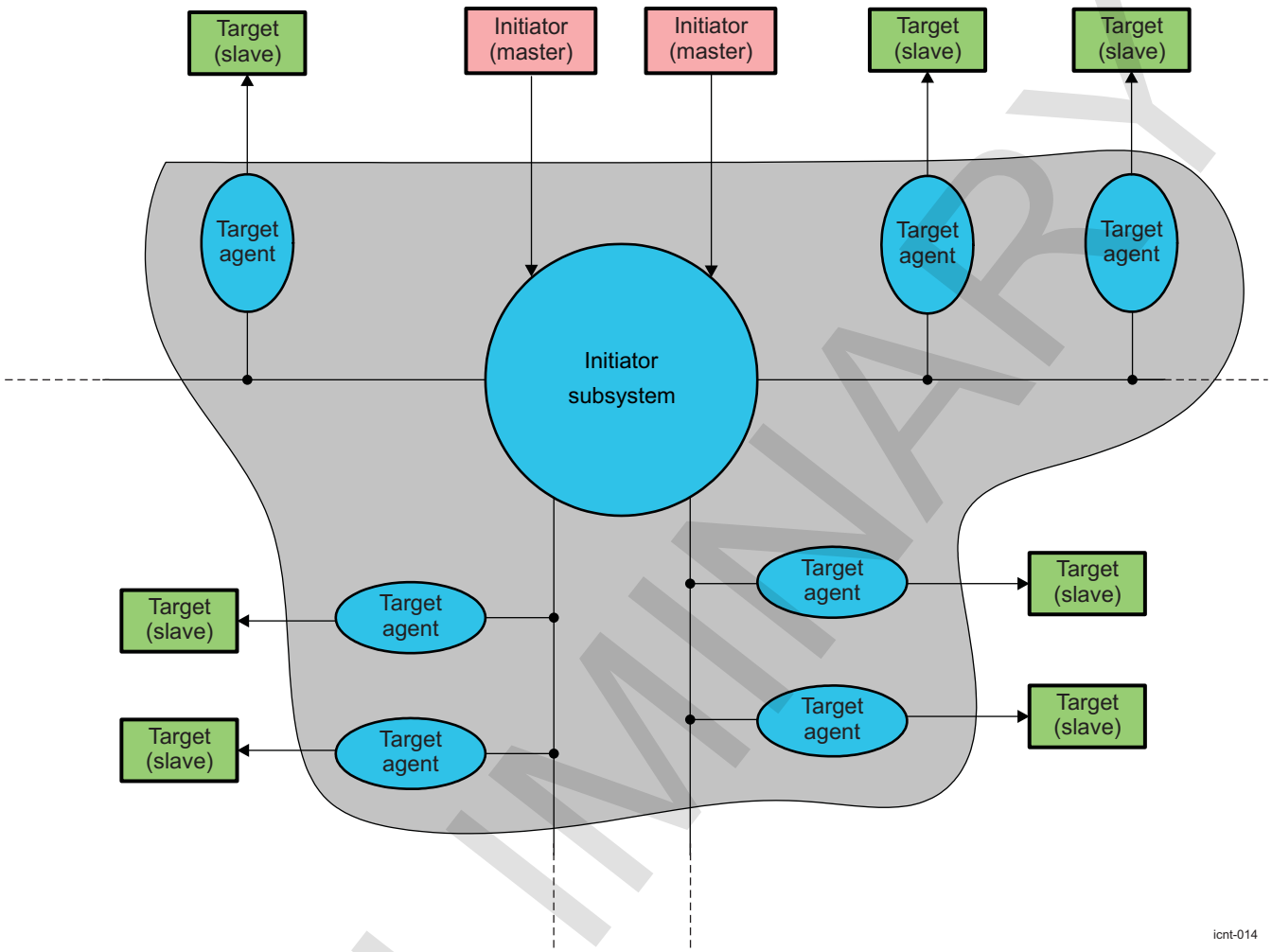
Figure 13-9. L4 Initiator-Target Connectivity



NOTE: As Figure 13-9 shows, targets are attached to branches. Branches do not impact the function of the L4 interconnect but are present to simplify timing closure and reduce active power consumption.

Because of the large address spaces and the number of peripherals connected to an L4 interconnect, two parameters are used to set up access permission:

- Programmable groups for initiators
  - Eight protection groups for L4_PER and L4_CFG interconnect
- Segments divided into regions of 4KB
  - 100 regions for the L4_PER interconnect
  - 104 regions for the L4_CFG interconnect

NOTE:

- Regions and segments are present for the L4_WKUP interconnect but cannot be programmed.
- L4_WKUP protection is done through the L4_CFG interconnect.

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Protection group members are TAs with the same protection settings. A region is programmed to allow access to a unique selectable protection group. For better protection, different regions are grouped into protection group regions and associated with a protection group member.

All L4 interconnect information, such as numbers of protection groups, regions, and segments, is available in the L4_LA_INITIATOR_INFO_L register.

13.3.3.3.1 Protection Group

A protection group is defined by its initiators and REQ_INFO is allowed. Two registers define these two settings:

- The CONNID_BIT_VECTOR field L4_AP_PROT_GROUP_MEMBERS_k_L is a 1-bit vector that defines which initiator belongs to a group. A protection group is accessible by an initiator when the bit position corresponding to its ConnID is set to 1 in the CONNID_BIT_VECTOR field. Table 13-286 lists all the ConnID available at the L4 levels.
- The ENABLE field L4_AP_PROT_GROUP_ROLES_k_L lists all possible REQ_INFO combinations associated with the L4_AP_PROT_GROUP_MEMBERS_k_L register. Setting a Req bit in this register determines the initiators type of access. For more information, see , *L3 Firewall Functionality*. Two REQ_INFOs are used in L4 interconnects: MReqDebug and MReqSupervisor.

NOTE: Permissions are identical for read and write accesses in L4 interconnect.

k indicates the protection group number.

L indicates the region number.

Table 13-286. L4 ConnID Definition

ConnID	Initiator
0	Cortex™-A9 MPU subsystem
1	DAP
2	DSP subsystem
3	Reserved
4	Reserved
5	sDMA
6	Reserved
7	Reserved
8	C2C
9	Reserved
A	Reserved
B	Reserved
C	Reserved
D	Reserved
E	Reserved
F	Reserved

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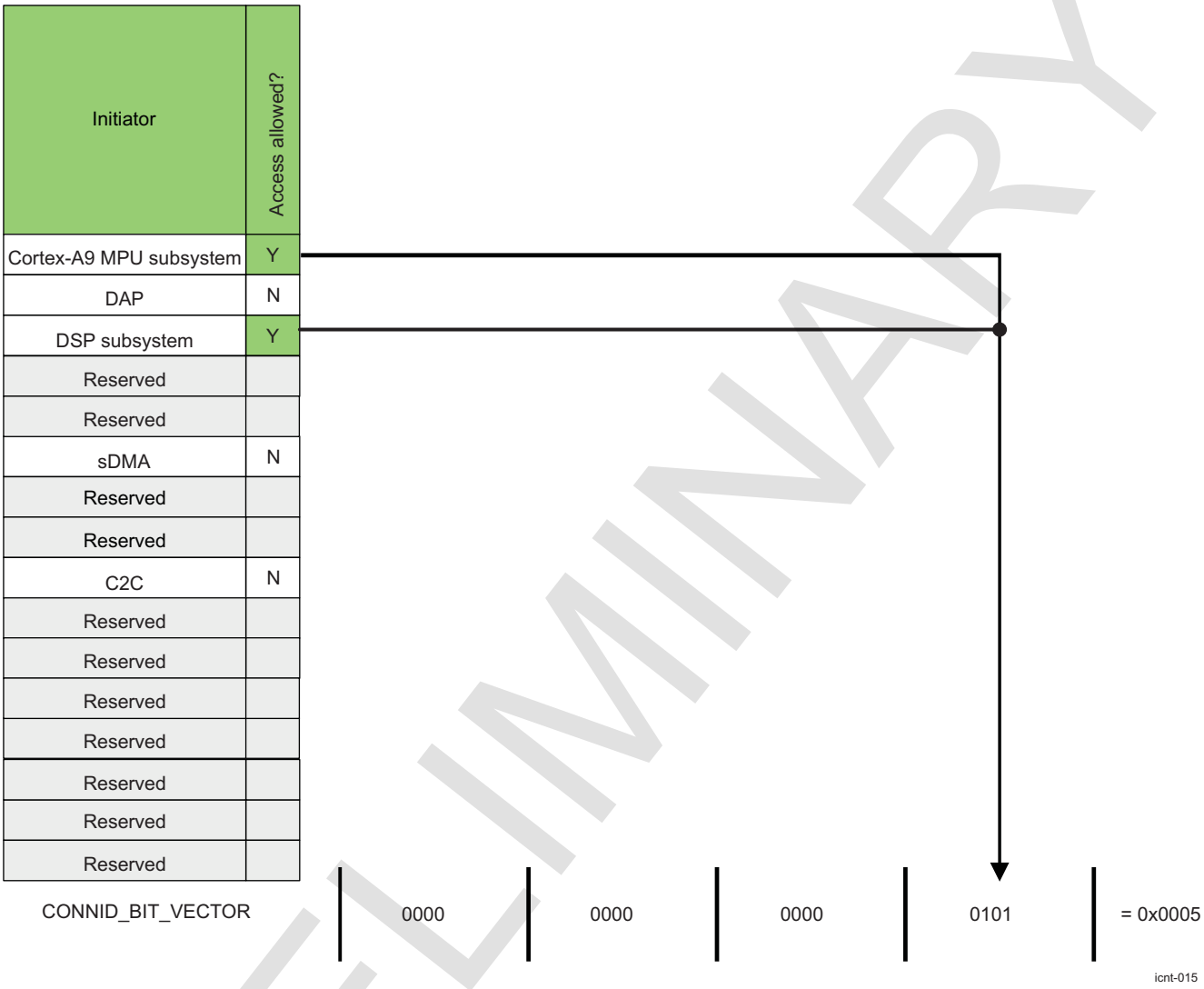
Figure 13-10 is an example of CONNID_BIT_VECTOR.

Figure 13-10. Example of CONNID_BIT_VECTOR L4_AP_PROT_GROUP_MEMBERS_k



Setting bits 0 and 2 in the PROT_GROUP_ID_1 register defines a group initiator that can access targets in protection group 1, and includes the following:

- Cortex-A9 MPU subsystem
- DSP subsystem

Protection group 1 can be applied to multiple protection regions with no limitation. Each protection region that is configured with protection group 1 enables permission access only to the two initiators.

The L4_AP_REGION_I_H PROT_GROUP_ID field determines the region to which the protection group member is attached.

The values of some CONNID_BIT_VECTOR and ENABLE fields are exported by the SCM at reset or are user writable (see Table 13-409 for more information).

Table 13-287 and Table 13-288 list the default configuration of the various groups for each L4 interconnect. For each group, some modules/regions are associated with it with default initiator members.

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Table 13-287. L4_PER Firewall Default Configuration

Group	Default Modules Associated With Group	Register	Modifiability	Default Value
Group 0 AP registers	AP registers	L4_AP_PROT_GROUP_ROLES_0_L	No	0xFFFF FFFF (all)
		L4_AP_PROT_GROUP_MEMBERS_0_L	No	0xFFFF (all)
Group 1	Reserved	L4_AP_PROT_GROUP_ROLES_1_L	No	0xFFFF FFFF (all)
		L4_AP_PROT_GROUP_MEMBERS_1_L	No	0xFFFF (all)
Group 2	Reserved	L4_AP_PROT_GROUP_ROLES_2_L	No	0xFFFF FFFF (all)
		L4_AP_PROT_GROUP_MEMBERS_2_L	No	0xFFFF (All)
Group 3–6 Free	No modules attached	L4_AP_PROT_GROUP_ROLES_3_L L4_AP_PROT_GROUP_ROLES_4_L L4_AP_PROT_GROUP_ROLES_5_L L4_AP_PROT_GROUP_ROLES_6_L	Yes	0xFFFF FFFF (all)
		L4_AP_PROT_GROUP_MEMBERS_3_L L4_AP_PROT_GROUP_MEMBERS_4_L L4_AP_PROT_GROUP_MEMBERS_5_L L4_AP_PROT_GROUP_MEMBERS_6_L	Yes	0xFFFF (all)
Group 7 Other modules	Other L4_PER modules	L4_AP_PROT_GROUP_ROLES_7_L	Yes	0xFFFF FFFF (all)
		L4_AP_PROT_GROUP_MEMBERS_7_L	Yes	0xFFFF (all)

Table 13-288. L4_CFG Firewall Default Configuration

Group	Default Modules Associated With Group	Register	Modifiability	Default Value
Group 0 AP registers	AP registers	L4_AP_PROT_GROUP_ROLES_0_L	No	0xFFFF FFFF (all)
		L4_AP_PROT_GROUP_MEMBERS_0_L	No	0xFFFF (all)
Group 1	SAR_RAM3, all FW registers	L4_AP_PROT_GROUP_ROLES_1_L	No	0xFFFF FFFF (all)
		L4_AP_PROT_GROUP_MEMBERS_1_L	No	0xFFFF (all)
Group 3 SAR_RAM2	SAR_RAM2	L4_AP_PROT_GROUP_ROLES_3_L	No	0xFFFF FFFF (all)
		L4_AP_PROT_GROUP_MEMBERS_3_L	No	0xFFFF (all)
Group 4 SAR_RAM4	SAR_RAM4	L4_AP_PROT_GROUP_ROLES_4_L	No	0xFFFF FFFF (all)
		L4_AP_PROT_GROUP_MEMBERS_4_L	No	0xFFFF (all)
Group 5 Free	Reserved	L4_AP_PROT_GROUP_ROLES_5_L	Yes	0xFFFF FFFF (all)
		L4_AP_PROT_GROUP_MEMBERS_5_L	Yes	0xFFFF (all)

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Table 13-288. L4_CFG Firewall Default Configuration (continued)

Group	Default Modules Associated With Group	Register	Modifiability	Default Value
Group 6 Free	No modules attached	L4_AP_PROT_GROUP_ROLES_6_L	Yes	0xFFFF FFFF (all)
		L4_AP_PROT_GROUP_MEMBERS_6_L	Yes	0xFFFF (all)
Group 7 Other modules	Other L4_CFG modules	L4_AP_PROT_GROUP_ROLES_7_L	Yes	0xFFFF FFFF (all)
		L4_AP_PROT_GROUP_MEMBERS_7_L	Yes	0xFFFF (all)

13.3.3.3.2 Segments and Regions

The protection mechanism for L4 interconnects is based on a hierarchical segmentation, as shown in Figure 13-11. By default, some regions are attached to specific protection group members. This specificity lets users set up the permission access to certain types of modules requiring the same access protection without managing region allocation.

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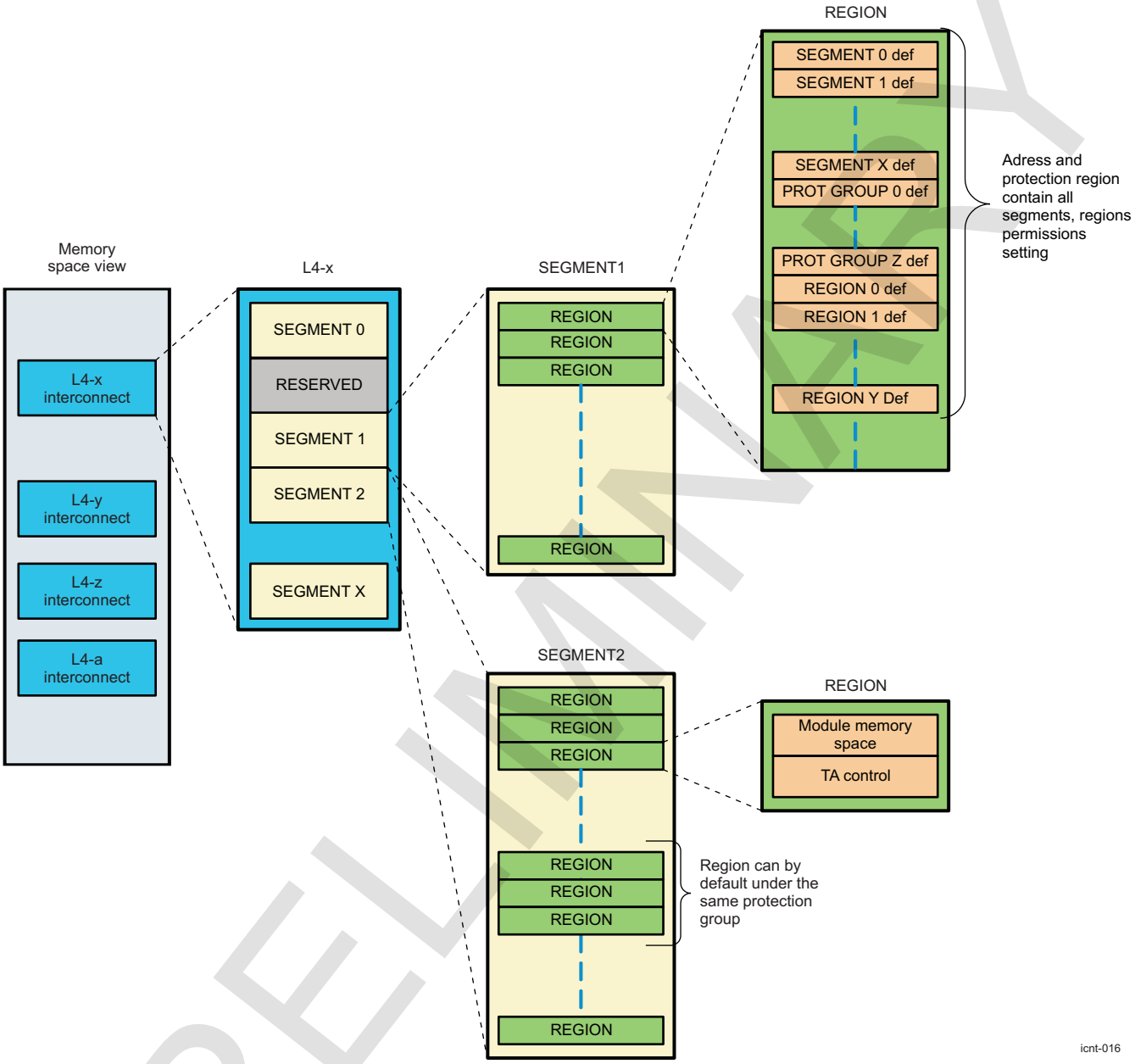
Figure 13-11. L4 Segmentation



All interconnect address spaces are covered by regions. Table 13-289 through Table 13-291 list the module mapping with their addresses, region numbers, and default protection group allocated to them.

NOTE: Module refers to the configuration registers of the module.

TA refers to the interconnect configuration registers of the TA associated with the module.

Table 13-289. Region Allocations for L4_PER Interconnect

Module	Region	Description
L4_PER CONFIG	0	Firewall
	1	PER_IA_0
	2	Link agent

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Table 13-289. Region Allocations for L4_PER Interconnect (continued)

Module	Region	Description
UART3	3	TA
	4	Module
GPTIMER2	5	TA
	6	Module
GPTIMER3	7	TA
	8	Module
GPTIMER4	9	TA
	10	Module
GPTIMER9	11	TA
	12	Module
DSS	13	TA
	14	Module
GPIO2	15	TA
	16	Module
GPIO3	17	TA
	18	Module
GPIO4	19	TA
	20	Module
GPIO5	21	TA
	22	Module
GPIO6	23	TA
	24	Module
I2C3	36	Module
	25	TA
UART1	26	TA
	27	Module
UART2	28	TA
	29	Module
UART4	30	TA
	31	Module
I2C1	32	TA
	33	Module
I2C2	34	TA
	35	Module
MCBSP4	37	TA
	38	Module
SLIMBUS2	39	TA
	40	Module
ELM	41	TA
	42	Module
GPTIMER10	43	TA
	44	Module
GPTIMER11	45	TA
	46	Module
MCSPI1	49	TA
	50	Module
MCSPI2	51	TA

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Table 13-289. Region Allocations for L4_PER Interconnect (continued)

Module	Region	Description
	52	Module
HSMMC1	53	TA
	54	Module
HSMMC3	63	TA
	64	Module
HDQ	65	TA
	66	Module
HSMMC2	67	TA
	68	Module
MCSPI3	69	TA
	70	Module
MCSPI4	71	TA
	72	Module
HSMMC4	73	TA
	74	Module
HSMMC5	75	TA
	76	Module
I2C4	77	TA
	78	Module
L4_PER CONFIG	81	PER_IA_1
	82	PER_IA_2
	83	PER_IA_3

Table 13-290. Region Allocations for L4_CFG Interconnect

Module	Region	Description
L4_CFG CONFIG	0	Firewall
	1	CFG_IA_0
	2	Link agent
CFG_SYSCTRL_GENERAL_CORE	3	TA
	4	Module
CM1	5	TA
	6	Module
sDMA	7	TA
	8	Module
HSI	9	TA
	10	Module
HSUSBTLL	11	TA
	12	Module
SR1	13	TA
	14	Module
SR2	15	TA
	16	Module
SR3	17	TA
	18	Module
CFG_SYSCTRL_PADCONF_CORE	21	TA
	22	Module
CM2	23	TA

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Table 13-290. Region Allocations for L4_CFG Interconnect (continued)

Module	Region	Description
	24	Module
DSP subsystem	25	TA
	26	Module
Mailbox	27	TA
	28	Module
SPINLOCK	29	TA
	30	Module
SL2FW	31	TA
	32	Module
MAFW	33	TA
	34	Module
C2CFW	35	TA
	36	Module
OCMCRAMFW	39	TA
	40	Module
EMIFFW	41	TA
	42	Module
GPMCFW	43	TA
	44	Module
ISSFW	45	TA
	46	Module
SGXFW	47	TA
	48	Module
CORTEXM3FW	49	TA
	50	Module
IVAHDFW	51	TaA
	52	Module
EMUSSFW	53	TA
	54	Module
ABEFW	55	TA
	56	Module
DSSFW	59	TA
	60	Module
FACEDETECT	65	TA
	66	Module
L4WKUP	67	L4_WKUP regions 0, 1, 2, 3, 4, 15, 16, 17, 18, 19, 20
	68	Module
	71	L4_WKUP regions 23, 24, 25, 26
	72	L4_WKUP regions 27, 28
	73	L4_WKUP region 13
	74	L4_WKUP region 29
	75	L4_WKUP region 30
	76	L4_WKUP region 31
	77	–
SAR_ROM	80	TA
	81	Module
USBFS	82	TA

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Table 13-290. Region Allocations for L4_CFG Interconnect (continued)

Module	Region	Description
	83	Module
USBOTGHS	84	TA
	85	Module
USBHOSTHS	86	TA
	87	Module
USBPHY	88	TA
	89	Module
L4WKUP	90	L4_WKUP region 14
	91	–
	92	L4_WKUP region (5, 6, 7, 8)
	93	L4_WKUP region (9, 10)
	94	L4_WKUP region (11, 12)
	95	L4_WKUP region (21, 22)

Table 13-291. Region Allocations for L4_WKUP Interconnect

Module	Region	Description
L4 WKUP CONFIG	0	AP
	1	CFG_IA_0
	2	Link agent
PRM	3	TA
	4	Module
GPIO1	5	TA
	6	Module
WDTIMER2	7	TA
	8	Module
Timer 1 ms	9	Module
	10	TA
KEYBOARD	11	TA
	12	Module
SAR_RAM	13	TA
	14	Module
SCRM	15	TA
	16	Module
32KTIMER	17	TA
	18	Module
WKUP_SYSCTRL_GENERAL_WKUP	19	TA
	20	Module
WKUP_TA_SYSCTRL_PADCONF_WKUP	21	TA
	22	Module
SAR_RAM	29	TA
	30	TA
	31	TA

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13.3.3.3.3 L4 Firewall Address and Protection Register Settings

Table 13-292 lists the settings of the AP registers relative to an L4 interconnect firewall. These values are computed based on the physical implementation of each L4 interconnect.

Table 13-292. L4 Firewall Register Description Overview

Register Type	Register Name	Bits	Field	Description
Segment	L4_AP_SEGMENT_i_L (1)	23:0	BASE	Segment base address
	L4_AP_SEGMENT_i_H (1)	4:0	SIZE	Segment size equals to 2^{SIZE}
Protection groups	L4_AP_PROT_GROUP_MEMBERS_k_L (2)	15:0	CONNID_BIT_VECTOR	For L4ConnID, see Table 13-286.
	L4_AP_PROT_GROUP_ROLES_k_L (2)	31:0	ENABLE	See for REQ_INFO description(3)
Region setting	L4_AP_REGION_l_L (4)	23:0	BASE	Defines the base address of region with respect to its segment base address
	L4_AP_REGION_l_H (4)	27:24	SEGMENT_ID	Segment ID number of the region
		22:20	PROT_GROUP_ID	Protection group member attached to the region
		19:17	BYTE_DATA_WIDTH_EXP	Determines the number of byte in an access
		5:1	SIZE	Size of the region equals to 2^{SIZE}
		0	ENABLE	Enables the region protection

(1) i = 0 to 1 for PER_AP
i = 0 to 6 for CFG_AP
(2) k = 0 to 7 for PER_AP
k = 0 to 7 for CFG_AP
(3) For L interconnects, only MReqDebug and MReqSupervisor are available.
(4) l = 0 to 96 for PER_AP
l = 0 to 113 for CFG_AP

13.3.3.4 L4 Error Detection and Reporting

13.3.3.4.1 IA and TA Error Detection and Logging

The L4 interconnect provides mechanisms for handling internally detected errors or errors reported by modules attached to the L4 target ports.

NOTE: L4_IA denotes the IA for all L4 interconnects: L4_PER, L4_CFG, and L4_WKUP.

L4_TA denotes the TA for all L4 interconnects: L4_PER, L4_CFG, and L4_WKUP.

The L4 interconnects handle four types of errors:

- No target core found or address hole, detected and logged at IA
- Unsupported command, detected and logged at IA
- Protection violation, detected and logged at IA (see Section 13.3.3.3, *L4 Firewalls*)
- Target does not service a request before a time-out expires. The error is detected and logged at TA (see Section 13.3.3.4.2, *Time-Out*).

Table 13-293 lists the value of the L4_IA_ERROR_LOG_L[25:24] CODE bit field stored when an error occurs.

Table 13-293. L4 CODE Bit Field Definition

CODE (bits 1:0)	Error Type	REQ_INFO	Secondary	ConnID	CMD
0	No error				
1	Unsupported command	x	x	x	x

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Table 13-293. L4 CODE Bit Field Definition (continued)

CODE (bits 1:0)	Error Type	REQ_INFO	Secondary	ConnID	CMD
2	Address hole	x	x	x	x
3	Protection violation	x		x	x

- No target core found/address hole: This error indicates that a request was addressed to a hole in the L4 address map. When this error occurs, an in-band error response is returned to the L3 level. The error is also logged into the L4_IA_AGENT_STATUS_L[27] INBAND_ERROR bit. Additionally, an address hole error code is logged to the L4_IA_ERROR_LOG_L[25:24] CODE bit field.
- Unsupported command: This error indicates that the command type of the request is not supported by the accessed target register. The error is logged into the L4_IA_AGENT_STATUS_L[27] INBAND ERROR bit. An unsupported command error code is written to the L4_IA_ERROR_LOG_L[25:24] CODE bit field for the initiator interface.
- Protection violation: This error indicates that a request is not issued from an allowed initiator member or is issued with the inappropriate ReqInfo qualifiers associated with the target region. This error is reported using an in-band error and is written to the L4_IA_AGENT_STATUS_L[27] INBAND_ERROR bit. A protection violation error code is saved into the L4_IA_ERROR_LOG_L[25:24] CODE bit field for the same initiator interface. A protection violation is also logged in the L4_IA_AGENT_STATUS_L[31] PROT_ERROR_SECONDARY or [30] PROT_ERROR_PRIMARY bit when in debug or applicative mode, respectively.

  The L4_IA_ERROR_LOG_L[30] SECONDARY bit indicates whether the error occurred in application or debug.

  The L4_IA_ERROR_LOG_H[15:0] REQ_INFO bit field returns the type access (REQ_INFO qualifier) that caused the error.

  The L4_IA_ERROR_LOG_L[11:8] CONNID bit field returns the ID of the initiator that caused the error.

  The L4_IA_ERROR_LOG_ADDR_L[31:0] register logs the address for error conditions.

  A L4_IA_ERROR_LOG_L[31] MULTI bit is asserted when multiple errors are detected. In this case, the error code corresponds to the first error that occurs.

13.3.3.4.2 Time-Out

A time-out mechanism can be enabled at the interconnect level and on a per-target basis. If the mechanism is enabled for a TA and interconnect and commands are not accepted or responses are not returned within the expected delay, the L4 interconnect generates an error event.

NOTE: The time-out mechanism is not available on the L4_WKUP interconnect, but L4_WKUP timeouts are detected in CFG_TA_L4WKUP of the L4_CFG interconnect.

The error is logged in the L4_TA_AGENT_STATUS_L[8] REQ_TIMEOUT bit. The affected TA enters an error state that causes it to send an error response to any new request targeted at it. To recover from this state, the TA must be reset by the system software. The time-out is counted starting from the moment a command is presented to the target, regardless of the target response to this command.

The L4 interconnect implements a centralized time-base circuit that broadcasts a set of four periodic pulse signals to all connected TAs. The time-base circuit offers four possible sets of four time-base signals. Selection is done by programming the L4_LA_NETWORK_CONTROL_L[10:8] TIMEOUT_BASE bit field.

The selected time-base signals are available at any TA. Each TA can be programmed to refer to one of these four time-base signals, using the L4_TA_AGENT_CONTROL_L[10:8] REQ_TIMEOUT bit field. These four signals are referred to as 1X time-base, 4X time-base, 16X time-base, and 64X time-base.

Table 13-294 lists all values in number of L4 clock cycles.

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Table 13-294. L4 Time-Out Link and TA Programming

	L4_TA_AGENT_CONTROL_L REQ_TIMEOUT[2:0]				
L4_LA_NETWORK_CONTROL_L TIMEOUT_BASE[2:0]	0	1	2	3	4
0	All L4 time-out features are disabled.				
1	Locally disabled	64	256	1024	4096
2		256	1024	4096	16,384
3		1024	4096	16,384	65,536
4		4096	16,384	65,536	262,144

The default reset value is 0x2 for REQ_TIMEOUT and 0x4 for TIMEOUT_BASE, implying 16,384 clock cycles.

A time-out condition is detected when the command acceptance or the response is not received after a delay of from one to three time-base periods.

Example:

- L4 frequency = 65 MHz
- TIMEOUT_BASE = 4 in the L4_LA_NETWORK_CONTROL_L register
- REQ_TIMEOUT = 2 in the L4_TA_AGENT_CONTROL_L for TA A
- REQ_TIMEOUT = 4 in the L4_TA_AGENT_CONTROL_L for TA B

At agent A, the time-base unit is 16,384 cycles. A time-out is issued when a request to the attached module is not accepted, or no response is sent after a delay of 252 µs to 756 µs.

At agent B, the time-base unit is 262,144 cycles. A time-out is issued when a request to the attached module is not accepted or no response is sent after a delay of 4 ms to 12 ms.

On detection of a time-out condition, the TA logs the error in the L4_TA_AGENT_STATUS_L[8] REQ_TIMEOUT bit, and it also reports the error to the IA, which forward it to the L3 interconnects.

After the time-out is detected and logged, the behavior of the attached module is ignored. A new request targeting the module arriving at the timed-out TA receives an error response. If the request is addressed to the agent internal registers, it is processed normally.

To recover from a time-out error, software is assumed to first reset the faulty module and then the TA using the L4_TA_AGENT_CONTROL_L[0] OCP_RESET bit.

13.3.3.4.3 Error Reporting

Figure 13-12 shows the error-reporting scheme used in the L4 interconnects. All L4 in-band errors are reported to their respective L3 TA, where errors are converted in an out-of band error signal (the L3 applicative and debug composite flags) going to the L3 Interrupt controllers.

Two levels of mask are present to report the error at INTC level:

- At the applicative and debug composite flag, to enable interrupt reporting, the following bits must be set:
  - L4 CFG in L3_CLK1_FLAG_MASK_0[3] and L3_CLK1_FLAG_STATUS_1[3]
  - L4 PER in L3_CLK2_FLAG_MASK_0[17][16][15][6] and L3_CLK2_FLAG_STATUS_1[17][16][15][6]
- At the L3 TA level, see , *L3 Interconnect*.

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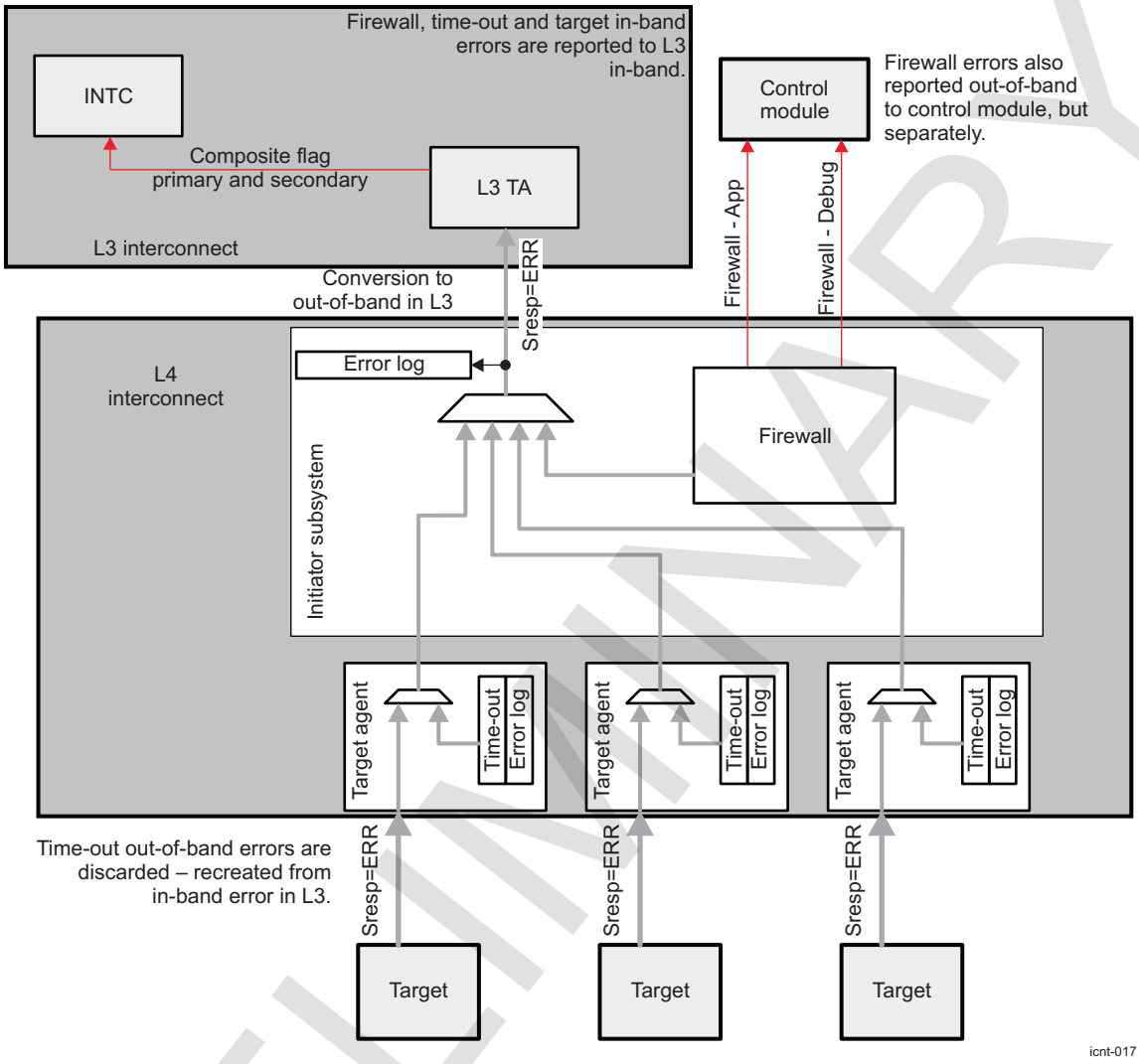
Figure 13-12. L4 Error Reporting



13.3.3.4.4 Error Recovery

Writing 1 to the L4_TA_AGENT_CONTROL_L[0] OCP_RESET bit initiates the software reset period. Software reset must be asserted for at least 16 cycles of the target module interface clock, which can be a divided clock with respect to the L4 clock.

During the software reset period:

- Requests sent to the target module receive error responses. Therefore, if the faulty request is part of a DMA transfer, it is necessary to stop the DMA to prevent unwanted errors.
- Requests sent to the TA register block are processed as usual.
- The L4_TA_AGENT_STATUS_L[8] REQ_TIMEOUT status bit is cleared.

Writing 0 to the L4_TA_AGENT_CONTROL_L[0] OCP_RESET bit terminates the software reset period.

The attached module must then be reset to complete the recovery.

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13.3.3.4.5 Firewall Error Logging in the Control Module

When a protection violation occurs, an interrupt is send to the INTCs (if enabled). An in-band error is sent back to L3 IA and an out-band error can also be logged in the CONTROL.CONTROL_SEC_ERR_STATUS register in the system control module (SCM). These out-band errors are enabled/disabled at the L4 IA level by setting the L4_IA_AGENT_CONTROL_L[31][30] PROT_ERROR_SECONDARY_REP or PROT_ERROR_PRIMARY_REP bit to 1 for debug and application mode, respectively.

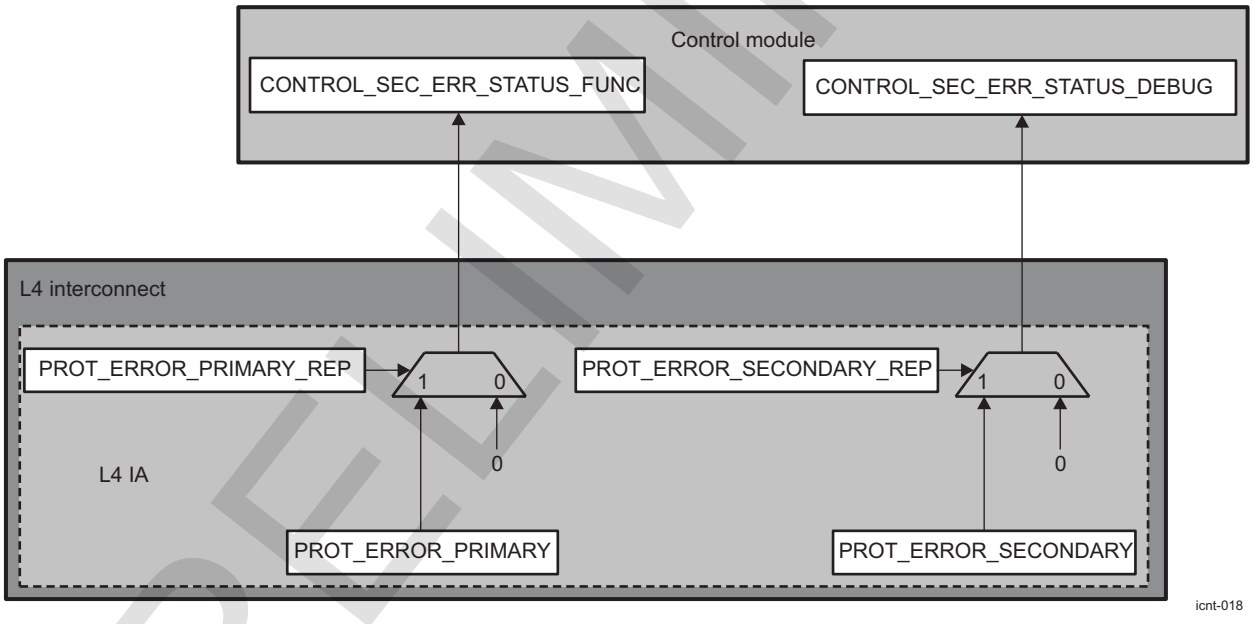
At the control module level, two logging registers are used, depending on the mode:

- In application mode or primary error reporting:
  - CONTROL.CONTROL_SEC_ERR_STATUS_FUNC[16] = L4_CFG protection violation
  - CONTROL.CONTROL_SEC_ERR_STATUS_FUNC[17] = L4_PER protection violation
- In debug mode or secondary error reporting:
  - CONTROL.CONTROL_SEC_ERR_STATUS_DEBUG[16] = L4_CFG protection violation
  - CONTROL.CONTROL_SEC_ERR_STATUS_DEBUG[17] = L4_PER protection violation

NOTE: The CONTROL.CONTROL_SEC_ERR_STATUS_xxx registers are only readable.

Figure 13-13 shows the global protection error reporting to at the control module.

Figure 13-13. Protection Violation Out-of-Band Error Reporting



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13.3.4 L4 Interconnect Programming Guide

13.3.4.1 L4 Interconnect Low-level Programming Models

This section describes the low-level hardware programming sequences for configuring and using the L4 interconnect module.

13.3.4.1.1 Global Initialization

13.3.4.1.1.1 Surrounding Modules Global Initialization

This section identifies the requirements of initializing the surrounding modules when the L4 interconnect module is to be used for the first time after a device reset. This initialization of surrounding modules is based on the integration and environment of the L4 interconnect. For more information, see Section 13.3.2, *L4 Interconnect Integration* .

Table 13-295. Global Initialization of Surrounding Modules

Surrounding Modules	Comments
PRCM	For more information about the configuration of the module, see Chapter 3, *Power, Reset, and Clock Management*.
Control module	For more information about the configuration of the module, see Chapter 18, *Control Module*.
MPU INTC	The MPU INTC must be configured to enable the interrupts from L4 interconnect module. SeeChapter 17 *Interrupt Controllers*.
sDMA	For more information about the configuration of the sDMA, see Chapter 16, *sDMA* .
L3 interconnect	For more information about the interconnect configuration, see , *Interconnect*.

13.3.4.1.2 Operational Modes Configuration

13.3.4.1.2.1 L4 Interconnect Error Analysis Mode

13.3.4.1.2.1.1 Main Sequence: L4 Interconnect Error Analysis Mode

The information required to analyze an error source is logged in several registers.The number of registers to access depends on the error source.

Figure 13-14 and Figure 13-15 show the software sequence required in most cases.

Table 13-296 and Table 13-297 show the main sequence for error analysis mode and its subprocess call summary, respectively.

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Figure 13-14. Typical Error Analysis Sequence

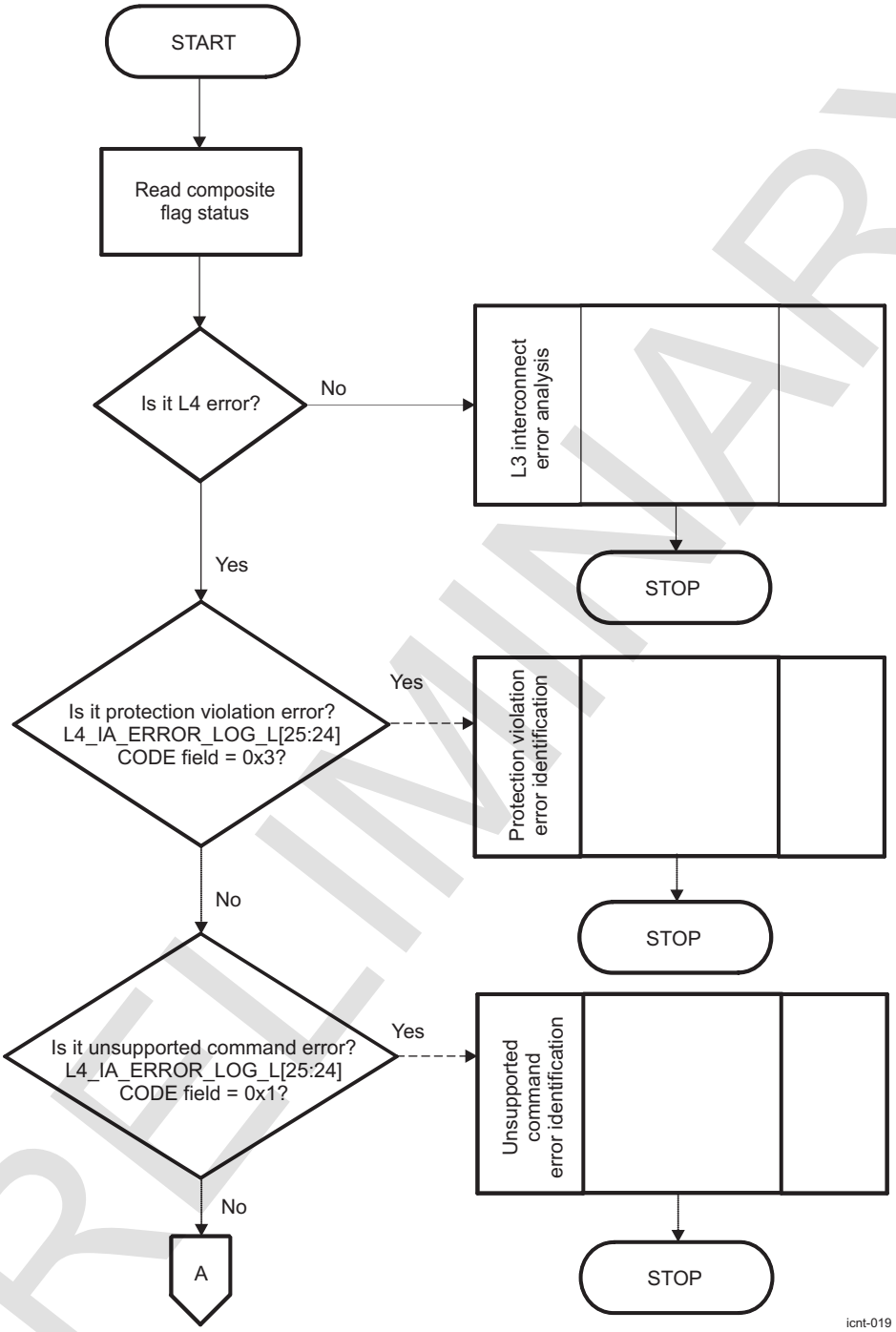

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Figure 13-15. Typical Error Analysis Sequence

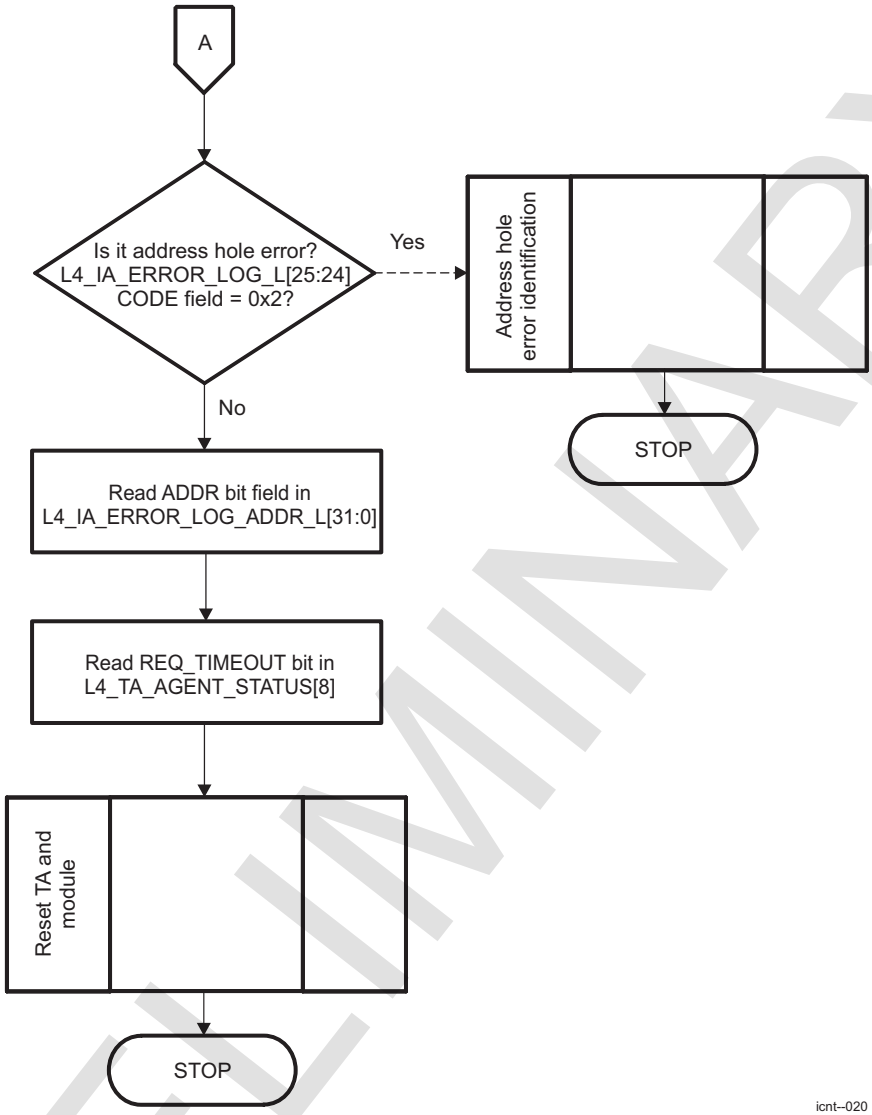

Table 13-296. Main Sequence – Error Analysis Mode

Register Name	Register Name	Register Name
L4_IA_ERROR_LOG_L	L4_IA_ERROR_LOG_ADDR_L	L4_IA_AGENT_STATUS_L
L4_IA_AGENT_CONTROL_L	CONTROL.CONTROL_SEC_ERR_STATUS_FUNC	CONTROL.CONTROL_SEC_ERR_STATUS_DEBUG
L4_TA_AGENT_STATUS_L		

Table 13-297. Subprocess Call Summary for Main Sequence – Error Analysis Mode

Subprocess	Cross-Reference
L3 interconnect error analysis	, *L3 Interconnect Error Handling*
L4 interconnect protection violation error identification	Section 13.3.4.1.2.1.2, *Subsequence: L4 Interconnect Protection Violation Error Identification*
L4 interconnect unsupported command/address hole error identification	Section 13.3.4.1.2.1.3, *Subsequence: L4 Interconnect Unsupported Command/Address Hole Error Identification*
L4 interconnect reset TA and module	Section 13.3.4.1.2.1.4, *Subsequence: L4 Interconnect Reset TA and Module*

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13.3.4.1.2.1.2 Subsequence: L4 Interconnect Protection Violation Error Identification

This procedure describes the protection violation error identification (see Table 13-298).

Table 13-298. Protection Violation Error Identification

Step	Register/Bit Field/Programming Model	Value
Read multiple errors detection.	L4_IA_ERROR_LOG_L[31] MULTI	
Read initiator ID.	L4_IA_ERROR_LOG_L[11:8] CONNID	
Read command that cause the error.	L4_IA_ERROR_LOG_L[2:0] CMD	
Read address of request that caused the error.	L4_IA_ERROR_LOG_ADDR_L[31:0] ADDR	
IF: Is it a primary error?	L4_IA_AGENT_STATUS_L[30] PROT_ERROR_PRIMARY	=0x1
Read status bits.	CONTROL.CONTROL_SEC_ERR_STATUS_FUNC[17:16]	
Write 1 to clear status bits.	CONTROL.CONTROL_SEC_ERR_STATUS_FUNC[17:16]	0x3
Write 1 to clear IA status bit.	L4_IA_AGENT_STATUS_L[30] PROT_ERROR_PRIMARY	0x1
ELSE		
Read status bits.	CONTROL.CONTROL_SEC_ERR_STATUS_DEBUG[17:16]	
Write 1 to clear status bits.	CONTROL.CONTROL_SEC_ERR_STATUS_DEBUG[17:16]	0x3
Write 1 to clear IA status bit	L4_IA_AGENT_STATUS_L[31] PROT_ERROR_SECONDARY	0x1
ENDIF		
Write 1 to clear multiple errors detection.	L4_IA_ERROR_LOG_L[31] MULTI	0x1
Write 1 to clear in-band error status.	L4_IA_AGENT_STATUS_L[24] INBAND_ERROR	0x1

13.3.4.1.2.1.3 Subsequence: L4 Interconnect Unsupported Command/Address Hole Error Identification

This procedure describes the identification of unsupported command/address hole error (see Table 13-299).

Table 13-299. Unsupported Command/Address Hole Error Identification

Step	Register/Bit Field/Programming Model	Value
Read multiple errors detection.	L4_IA_ERROR_LOG_L[31] MULTI	
Read initiator ID.	L4_IA_ERROR_LOG_L[11:8] CONNID	
Read command that caused the error.	L4_IA_ERROR_LOG_L[2:0] CMD	
Read address of request that caused the error.	L4_IA_ERROR_LOG_ADDR_L[31:0] ADDR	
Read secondary status.	L4_IA_ERROR_LOG_L[30] SECONDARY	
Write 1 to clear secondary status.	L4_IA_ERROR_LOG_L[30] SECONDARY	0x1
Write 1 to clear multiple errors detection.	L4_IA_ERROR_LOG_L[31] MULTI	0x1
Write 1 to clear inband error status.	L4_IA_AGENT_STATUS_L[24] INBAND_ERROR	0x1

13.3.4.1.2.1.4 Subsequence: L4 Interconnect Reset TA and Module

This procedure resets the TA and module (see Table 13-300).

Table 13-300. Reset TA and Module

Step	Register/Bit Field/Programming Model	Value
Reset TA.	L4_TA_AGENT_CONTROL_L[0] OCP_RESET	0x1
Wait until target module clock = 16 cycles.		

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Table 13-300. Reset TA and Module (continued)

Step	Register/Bit Field/Programming Model	Value
Write 0 to clear TA time - out status.	L4_TA_AGENT_CONTROL_L[10:8] REQ_TIMEOUT	0x0
Write 0 to clear TA reset.	L4_TA_AGENT_CONTROL_L[0] OCP_RESET	0x0
Reset the attached module.(1)		

(1) For more information, see the respective module chapter.

13.3.4.1.2.2 L4 Interconnect Time-Out Configuration Mode

13.3.4.1.2.2.1 Main Sequence: L4 Interconnect Time-Out Configuration Mode

This procedure describes the time-out configuration sequence (see Table 13-301).

Table 13-301. Time-Out Configuration

Step	Register/Bit Field/Programming Model	Value
Disable time-out.	L4_LA_NETWORK_CONTROL_L[10:8] TIMEOUT_BASE	0x0
Clear TA time-out error status.(1)	L4_TA_AGENT_STATUS_L[8] REQ_TIMEOUT	0x1
Set time-out at TA level.(1)	L4_TA_AGENT_CONTROL_L[10:8] REQ_TIMEOUT	xxx
Set time-out base.	L4_LA_NETWORK_CONTROL_L[10:8] TIMEOUT_BASE	xxx

(1) Must be done for each TA.

13.3.4.1.2.3 L4 Interconnect Firewall Configuration Mode

13.3.4.1.2.3.1 Main Sequence: L4 Interconnect Firewall Configuration Mode

This procedure describes the firewall configuration sequence (see Table 13-302).

Table 13-302. Firewall Configuration

Step	Register/Bit Field/Programming Model	Value
Define the members of protection group k.(1)	L4_AP_PROT_GROUP_MEMBERS_k_L[15:0] CONNID_BIT_VECTOR	xxx
Define the access type of a protection group k.(1)	L4_AP_PROT_GROUP_ROLES_k_L[15:0] ENABLE	xx
Set region affiliation to protection group.(2)	L4_AP_REGION_l_L[22:20] PROT_GROUP_ID	xxx

(1) Must be done for each protection group.
(2) Must be done for each region.

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13.3.5 L4 Interconnects Register Manual

Table 13-303 through Table 13-305 list all L4 register blocks for IA, TA, AP, and LA. Each module instance is shown with the module register mapping and bit and bit field definitions.

13.3.5.1 L4 Interconnects Instance Summary

Table 13-303. L4_PER Instance Summary

Module Name	L3 Base Address	Size
PER_AP	0x4800 0000	2KB
PER_IA_0	0x4800 1000	2KB
PER_LA	0x4800 0800	4KB
PER_TA_UART3	0x4802 1000	4KB
PER_TA_GPTIMER2	0x4803 3000	4KB
PER_TA_GPTIMER3	0x4803 5000	4KB
PER_TA_GPTIMER4	0x4803 7000	4KB
PER_TA_GPTIMER9	0x4803 F000	4KB
PER_TA_DSS	0x4805 0000	4KB
PER_TA_GPIO2	0x4805 6000	4KB
PER_TA_GPIO3	0x4805 8000	4KB
PER_TA_GPIO4	0x4805 A000	4KB
PER_TA_GPIO5	0x4805 C000	4KB
PER_TA_GPIO6	0x4805 E000	4KB
PER_TA_I2C3	0x4806 1000	4KB
PER_TA_UART1	0x4806 B000	4KB
PER_TA_UART2	0x4806 D000	4KB
PER_TA_UART4	0x4806 F000	4KB
PER_TA_I2C1	0x4807 1000	4KB
PER_TA_I2C2	0x4807 3000	4KB
PER_TA_SLIMBUS2	0x4807 7000	4KB
PER_TA_ELM	0x4807 9000	4KB
PER_TA_GPTIMER10	0x4808 7000	4KB
PER_TA_GPTIMER11	0x4808 9000	4KB
PER_TA_MCBSP4	0x4809 7000	4KB
PER_TA_MCSPI1	0x4809 9000	4KB
PER_TA_MCSPI2	0x4809 B000	4KB
PER_TA_HSMMC1	0x4809 D000	4KB
PER_TA_HSMMC3	0x480A E000	4KB
PER_TA_HDQ	0x480B 3000	4KB
PER_TA_HSMMC2	0x480B 5000	4KB
PER_TA_MCSPI3	0x480B 9000	4KB
PER_TA_MCSPI4	0x480B B000	4KB
PER_TA_HSMMC4	0x480D 2000	4KB
PER_TA_HSMMC5	0x480D 6000	4KB
PER_TA_I2C4	0x4835 1000	4KB

Table 13-304. L4_CFG Instance Summary

Module Name	L3 Base Address	Size
CFG_AP	0x4A00 0000	2KB
CFG_IA_0	0x4A00 1000	2KB

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Table 13-304. L4_CFG Instance Summary (continued)

Module Name	L3 Base Address	Size
CFG_LA	0x4A00 0800	4KB
CFG_TA_SYSCTRL_GENERAL_CORE	0x4A00 3000	4KB
CFG_TA_CM1	0x4A00 5000	4KB
CFG_TA_CM2	0x4A00 A000	4KB
CFG_TA_SDMA	0x4A05 7000	4KB
CFG_TA_HSI	0x4A05 C000	4KB
CFG_TA_SAR_ROM	0x4A06 0000	4KB
CFG_TA_HSUSBTLL	0x4A06 3000	4KB
CFG_TA_USBHOSTHS	0x4A06 5000	4KB
CFG_TA_DSP	0x4A06 7000	4KB
CFG_TA_USBFS	0x4A0A A000	4KB
CFG_TA_USBOTGHS	0x4A0A C000	4KB
CFG_TA_USBPHY	0x4A0A E000	4KB
CFG_TA_SR1	0x4A0D A000	4KB
CFG_TA_SR2	0x4A0DC000	4KB
CFG_TA_SR3	0x4A0D E000	4KB
CFG_TA_MAILBOX	0x4A0F 5000	4KB
CFG_TA_SPINLOCK	0x4A0F 7000	4KB
CFG_TA_SYSCTRL_PADCONF_CORE	0x4A10 1000	4KB
CFG_TA_FACEDETECT	0x4A10 B000	4KB
CFG_TA_MAFW	0x4A20 A000	4KB
CFG_TA_EMIFFW	0x4A20 D000	4KB
CFG_TA_GPMCFW	0x4A21 1000	4KB
CFG_TA_OCMCRAMFW	0x4A21 3000	4KB
CFG_TA_SGXFW	0x4A21 5000	4KB
CFG_TA_ISSFW	0x4A21 7000	4KB
CFG_TA_CORTEXM3FW	0x4A21 9000	4KB
CFG_TA_DSSFW	0x4A21 D000	4KB
CFG_TA_SL2FW	0x4A21 F000	4KB
CFG_TA_IVAHDFW	0x4A22 1000	4KB
CFG_TA_EMUSSFW	0x4A22 7000	4KB
CFG_TA_ABEFW	0x4A22 9000	4KB
CFG_TA_L4WKUP	0x4A34 0000	4KB

Table 13-305. L4_WKUP Instance Summary

Module Name	L3 Base Address	Size
WKUP_IA_0	0x4A30 1000	2KB
WKUP_LA	0x4A30 0800	4KB
WKUP_TA_32KTIMER	0x4A30 5000	4KB
WKUP_TA_PRM	0x4A30 8000	4KB
WKUP_TA_SCRM	0x4A30 B000	4KB
WKUP_TA_SYSCTRL_GENERAL_WKUP	0x4A30 D000	4KB
WKUP_TA_GPIO1	0x4A31 1000	4KB
WKUP_TA_WDTIMER2	0x4A31 5000	4KB
WKUP_TA_DM_TIMER1MS_1	0x4A31 9000	4KB
WKUP_TA_KEYBOARD	0x4A31 D000	4KB
WKUP_TA_SYSCTRL_PADCONF_WKUP	0x4A31 F000	4KB

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Table 13-305. L4_WKUP Instance Summary (continued)

Module Name	L3 Base Address	Size
WKUP_TA_SAR_RAM	0x4A32 A000	4KB

13.3.5.2 L4 Initiator Agent (L4 IA)

13.3.5.2.1 L4 Initiator Agent (L4 IA) Register Summary

Table 13-306 summarizes the L4 IA register mapping.

Table 13-306. IA Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	PER_IA_0 L3 Physical Address	CFG_IA_0 L3 Physical Address	WKUP_IA_0 L3 Physical Address
L4_IA_COMPONENT_L	R	32	0x0000 0000	0x4800 1000	0x4A00 1000	0x4A30 1000
L4_IA_COMPONENT_H	R	32	0x0000 0004	0x4800 1004	0x4A00 1004	0x4A30 1004
L4_IA_CORE_L	R	32	0x0000 0018	0x4800 1018	0x4A00 1018	0x4A30 1018
L4_IA_CORE_H	R	32	0x0000 001C	0x4800 101C	0x4A00 101C	0x4A30 101C
L4_IA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4800 1020	0x4A00 1020	0x4A30 1020
L4_IA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4800 1024	0x4A00 1024	0x4A30 1024
L4_IA_AGENT_STATUS_L	RW	32	0x0000 0028	0x4800 1028	0x4A00 1028	0x4A30 1028
L4_IA_AGENT_STATUS_H	R	32	0x0000 002C	0x4800 102C	0x4A00 102C	0x4A30 102C
L4_IA_ERROR_LOG_L	RW	32	0x0000 0058	0x4800 1058	0x4A00 1058	0x4A30 1058
L4_IA_ERROR_LOG_H	R	32	0x0000 005C	0x4800 105C	0x4A00 105C	0x4A30 105C
L4_IA_ERROR_LOG_ADDR_L	R	32	0x0000 0060	0x4800 1060	0x4A00 1060	0x4A30 1060
L4_IA_ERROR_LOG_ADDR_H	R	32	0x0000 0064	0x4800 1064	0x4A00 1064	0x4A30 1064

13.3.5.2.2 L4 Initiator Agent (L4 IA) Register Description

Table 13-307 through Table 13-329 describe the L4 IA registers.

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Table 13-307. L4_IA_COMPONENT_L

Address Offset	0x0000 0000
Physical Address	0x4800 1000 0x4A00 1000 0x4A30 1000
Description	COMPONENT register identifies the component to which this register block belongs. The register contains a component code and revision, which are used to identify the hardware of the component. The COMPONENT register is read-only.
Type	R

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CODE																REV															

Bits	Field Name	Description	Type	Reset
31:16	CODE	Interconnect code	R	See (1).
15:0	REV	Component revision code	R	See(1).

(1) TI Internal Data

Table 13-308. Register Call Summary for Register L4_IA_COMPONENT_L

L4 Interconnects

- L4 Initiator Agent (L4 IA) Register Summary: [0]

Table 13-309. L4_IA_COMPONENT_H

Address Offset	0x0000 0004
Physical Address	0x4800 1004 0x4A00 1004 0x4A30 1004
Description	COMPONENT register identifies the component to which this register block belongs. The register contains a component code and revision, which are used to identify the hardware of the component. The COMPONENT register is read-only.
Type	R

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

Bits	Field Name	Description	Type	Reset
31:0	RESERVED	Read returns 0.	R	0x0000

Table 13-310. Register Call Summary for Register L4_IA_COMPONENT_H

L4 Interconnects

- L4 Initiator Agent (L4 IA) Register Summary: [0]

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Table 13-311. L4_IA_CORE_L

Address Offset	0x0000 0018
Physical Address	0x4800 1018 0x4A00 1018 0x4A30 1018
Description	Provide information about the core initiator
Type	R

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CORE_CODE																CORE_REV															

Bits	Field Name	Description	Type	Reset
31:16	CORE_CODE	Interconnect core code	R	See (1).
15:0	CORE_REV	Component revision code code	R	See(1).

(1) TI Internal Data

Table 13-312. Register Call Summary for Register L4_IA_CORE_L

L4 Interconnects

- L4 Initiator Agent (L4 IA) Register Summary: [0]

Table 13-313. L4_IA_CORE_H

Address Offset	0x0000 001C
Physical Address	0x4800 101C 0x4A00 101C 0x4A30 101C
Description	Provide information about the core initiator
Type	R

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																VENDOR_CODE															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x0000
15:0	VENDOR_CODE	Vendor revision core code	R	See (1).

(1) TI Internal Data

Table 13-314. Register Call Summary for Register L4_IA_CORE_H

L4 Interconnects

- L4 Initiator Agent (L4 IA) Register Summary: [0]

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Table 13-315. L4_IA_AGENT_CONTROL_L

Address Offset	0x0000 0020
Physical Address	0x4800 1020 0x4A00 1020 0x4A30 1020
Description	Enable error reporting on an initiator interface.The error reporting mechanism is enabled when the INBAND_ERROR_REP bit field is set to 1. The out-of-band OCP MError reporting mechanism is enabled when the MERROR_REP bit field is set to 1.
Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROT_ERROR_SECONDARY_REP	PROT_ERROR_PRIMARY_REP	RESERVED		INBAND_ERROR_REP	RESERVED																										

Bits	Field Name	Description	Type	Reset
31	PROT_ERROR_SECONDARY_REP	Out-of-band reporting of protection mechanism secondary errors	RW	1
30	PROT_ERROR_PRIMARY_REP	Out-of-band reporting of protection mechanism primary errors	RW	1
29:28	RESERVED	Read returns 0.	R	0x0
27	INBAND_ERROR_REP	Setting this field to 1 reports on in-band errors using the INBAND_ERROR log bit of IA.AGENT_STATUS register.	RW	1
26:0	RESERVED	Read returns 0.	R	0x0

Table 13-316. Register Call Summary for Register L4_IA_AGENT_CONTROL_L

L4 Interconnects

- Firewall Error Logging in the Control Module: [0]
- Operational Modes Configuration: [1]
- L4 Initiator Agent (L4 IA) Register Summary: [2]

Table 13-317. L4_IA_AGENT_CONTROL_H

Address Offset	0x0000 0024
Physical Address	0x4800 1024 0x4A00 1024 0x4A30 1024
Description	Enable error reporting on an initiator interface.
Type	R

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

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Bits	Field Name	Description	Type	Reset
31:0	RESERVED	Read returns 0.	R	0x0000 0000

Table 13-318. Register Call Summary for Register L4_IA_AGENT_CONTROL_H

L4 Interconnects

- L4 Initiator Agent (L4 IA) Register Summary: [0]

Table 13-319. L4_IA_AGENT_STATUS_L

Address Offset	0x0000 0028
Physical Address	0x4800 1028 0x4A00 1028 0x4A30 1028
Description	Stores status information for an initiator. The INBAND_ERROR and MERROR fields are read/write and are implemented as log bits.
Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROT_ERROR_SECONDARY	PROT_ERROR_PRIMARY	RESERVED		INBAND_ERROR	RESERVED																										

Bits	Field Name	Description	Type	Reset
31	PROT_ERROR_SECONDARY	0x0: Secondary Protection error not present.0x1: Secondary Protection error present	RW W1toClr	0
30	PROT_ERROR_PRIMARY	0x0: Primary Protection error not present.0x1: Primary Protection error present	RW W1toClr	0
29:28	RESERVED	Read returns 0.	R	0x0
27	INBAND_ERROR	0x0 No In-Band error present.0x1 In-Band error present.	RW W1toClr	0
26:0	RESERVED	Read returns 0.	R	0x0

Table 13-320. Register Call Summary for Register L4_IA_AGENT_STATUS_L

L4 Interconnects

- IA and TA Error Detection and Logging: [0] [1] [2] [3]
- Operational Modes Configuration: [4] [5] [6] [7] [8] [9]
- L4 Initiator Agent (L4 IA) Register Summary: [10]

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Table 13-321. L4_IA_AGENT_STATUS_H

Address Offset	0x0000 002C
Physical Address	0x4800 102C 0x4A00 102C 0x4A30 102C
Description	Stores status information for an initiator.
Type	R

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

Bits	Field Name	Description	Type	Reset
31:0	RESERVED	Read returns 0.	R	0x0000 0000

Table 13-322. Register Call Summary for Register L4_IA_AGENT_STATUS_H

L4 Interconnects

- L4 Initiator Agent (L4 IA) Register Summary: [0]

Table 13-323. L4_IA_ERROR_LOG_L

Address Offset	0x0000 0058
Physical Address	0x4800 1058 0x4A00 1058 0x4A30 1058
Description	Log information about error conditions. The CODE field logs any protection violation or address hole errors detected by the initiator subsystem while decoding a request.
Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MULTI	SECONDARY	RESERVED				CODE		RESERVED								CONNID								RESERVED						CMD	

Bits	Field Name	Description	Type	Reset
31	MULTI	Multiple errors detected	RW W1toClr	0
30	SECONDARY	Indicates whether protection violation was a primary or secondary error	RW W1toClr	0
29:26	RESERVED	Read returns 0.	R	0x0
25:24	CODE	The error code of an initiator request. 0x00: No errors 0x01: Reserved 0x10: Address hole 0x11: Protection violation	RW W1toClr	0x0
23:14	RESERVED	Read returns 0.	R	0x000
13:8	CONNID	ConnID of request causing the error, refer to Table 13-286	R	0x00
7:3	RESERVED	Read returns 0.	R	0x00
2:0	CMD	Command that caused error	R	0x0

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Table 13-324. Register Call Summary for Register L4_IA_ERROR_LOG_L

L4 Interconnects

- IA and TA Error Detection and Logging: [0] [1] [2] [3] [4] [5] [6]
- Operational Modes Configuration: [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17]
- L4 Initiator Agent (L4 IA) Register Summary: [18]

Table 13-325. L4_IA_ERROR_LOG_H

Address Offset	0x0000 005C
Physical Address	0x4800 105C 0x4A00 105C 0x4A30 105C
Description	Log information about error conditions.
Type	R

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																REQ_INFO															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Read returns 0.	R	0x0000
15:0	REQ_INFO	MReqInfo bits of request that caused the error REQ_INFO[0] = supervisor, REQ_INFO[1] = Debug	R	0x0000

Table 13-326. Register Call Summary for Register L4_IA_ERROR_LOG_H

L4 Interconnects

- IA and TA Error Detection and Logging: [0]
- L4 Initiator Agent (L4 IA) Register Summary: [1]

Table 13-327. L4_IA_ERROR_LOG_ADDR_L

Address Offset	0x0000 0060
Physical Address	0x4800 1060 0x4A00 1060 0x4A30 1060
Description	Extended error log (address information)
Type	R

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR																															

Bits	Field Name	Description	Type	Reset
31:0	ADDR	Address of request that caused the error. N is the number MAddr bits.	R	0x0000 0000

Table 13-328. Register Call Summary for Register L4_IA_ERROR_LOG_ADDR_L

L4 Interconnects

- IA and TA Error Detection and Logging: [0]
- Operational Modes Configuration: [1] [2] [3]
- L4 Initiator Agent (L4 IA) Register Summary: [4]

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Table 13-329. L4_IA_ERROR_LOG_ADDR_H

Address Offset	0x0000 0064
Physical Address	0x4800 1064 0x4A00 1064 0x4A30 1064
Description	Extended error log (address information)
Type	R

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

Bits	Field Name	Description	Type	Reset
31:0	RESERVED	Read returns 0.	R	0x0000 0000

Table 13-330. Register Call Summary for Register L4_IA_ERROR_LOG_ADDR_H

L4 Interconnects

- L4 Initiator Agent (L4 IA) Register Summary: [0]

13.3.5.3 L4 Target Agent (L4 TA)

13.3.5.3.1 L4 Target Agent (L4 TA) Register Summary

Table 13-331 through Table 13-361 summarizes the L4 TA mapping of the CFG_TA, PER_TA, and WKUP_TA registers.

Table 13-331. CFG_TA Register Mapping Summary 1

Register Name	Type	Register Width (Bits)	Address Offset	CFG_TA_SYSCTRL_GENERAL_CORE L3 Physical Address	CFG_TA_CM1 L3 Physical Address	CFG_TA_CM2 L3 Physical Address
L4_TA_COMPONENT_H	R	32	0x0000 0000	0x4A00 3000	0x4A00 5000	0x4A00 A000
L4_TA_COMPONENT_L	R	32	0x0000 0004	0x4A00 3004	0x4A00 5004	0x4A00 A004
L4_TA_CORE_L	R	32	0x0000 0018	0x4A00 3018	0x4A00 5018	0x4A00 A018
L4_TA_CORE_H	R	32	0x0000 001C	0x4A00 301C	0x4A00 501C	0x4A00 A01C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4A00 3020	0x4A00 5020	0x4A00 A020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4A00 3024	0x4A00 5024	0x4A00 A024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4A00 3028	0x4A00 5028	0x4A00 A028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4A00 302C	0x4A00 502C	0x4A00 A02C

Table 13-332. CFG_TA Register Mapping Summary 2

Register Name	Type	Register Width (Bits)	Address Offset	CFG_TA_SDMA L3 Physical Address	CFG_TA_HSI L3 Physical Address	CFG_TA_SAR_ROM L3 Physical Address
L4_TA_COMPONENT_H	R	32	0x0000 0000	0x4A05 7000	0x4A05 C000	0x4A06 0000

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Table 13-332. CFG_TA Register Mapping Summary 2 (continued)

Register Name	Type	Register Width (Bits)	Address Offset	CFG_TA_SDMA L3 Physical Address	CFG_TA_HSI L3 Physical Address	CFG_TA_SAR_ROM L3 Physical Address
L4_TA_COMPONENT_L	R	32	0x0000 0004	0x4A05 7004	0x4A05 C004	0x4A06 0004
L4_TA_CORE_L	R	32	0x0000 0018	0x4A05 7018	0x4A05 C018	0x4A06 0018
L4_TA_CORE_H	R	32	0x0000 001C	0x4A05 701C	0x4A05 C01C	0x4A06 001C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4A05 7020	0x4A05 C020	0x4A06 0020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4A05 7024	0x4A05 C024	0x4A06 0024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4A05 7028	0x4A05 C028	0x4A06 0028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4A05 702C	0x4A05 C02C	0x4A06 002C

Table 13-333. CFG_TA Register Mapping Summary 3

Register Name	Type	Register Width (Bits)	Address Offset	CFG_TA_HSUSBTLL L3 Physical Address	CFG_TA_USBHOSTHS L3 Physical Address	CFG_TA_DSP L3 Physical Address
L4_TA_COMPONENT_H	R	32	0x0000 0000	0x4A06 3000	0x4A06 5000	0x4A06 7000
L4_TA_COMPONENT_L	R	32	0x0000 0004	0x4A06 3004	0x4A06 5004	0x4A06 7004
L4_TA_CORE_L	R	32	0x0000 0018	0x4A06 3018	0x4A06 5018	0x4A06 7018
L4_TA_CORE_H	R	32	0x0000 001C	0x4A06 301C	0x4A06 501C	0x4A06 701C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4A06 3020	0x4A06 5020	0x4A06 7020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4A06 3024	0x4A06 5024	0x4A06 7024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4A06 3028	0x4A06 5028	0x4A06 7028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4A06 302C	0x4A06 502C	0x4A06 702C

Table 13-334. CFG_TA Register Mapping Summary 4

Register Name	Type	Register Width (Bits)	Address Offset	CFG_TA_USBFS L3 Physical Address	CFG_TA_USBOTGHS L3 Physical Address	CFG_TA_USBPHY L3 Physical Address
L4_TA_COMPONENT_H	R	32	0x0000 0000	0x4A0A A000	0x4A0A C000	0x4A0A E000
L4_TA_COMPONENT_L	R	32	0x0000 0004	0x4A0A A004	0x4A0A C004	0x4A0A E004
L4_TA_CORE_L	R	32	0x0000 0018	0x4A0A A018	0x4A0A C018	0x4A0A E018
L4_TA_CORE_H	R	32	0x0000 001C	0x4A0A A01C	0x4A0A C01C	0x4A0A E01C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4A0A A020	0x4A0A C020	0x4A0A E020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4A0A A024	0x4A0A C024	0x4A0A E024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4A0A A028	0x4A0A C028	0x4A0A E028

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Table 13-334. CFG_TA Register Mapping Summary 4 (continued)

Register Name	Type	Register Width (Bits)	Address Offset	CFG_TA_USBFS L3 Physical Address	CFG_TA_USBOTGHS L3 Physical Address	CFG_TA_USBPHY L3 Physical Address
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4A0A A02C	0x4A0A C02C	0x4A0A E02C

Table 13-335. CFG_TA Register Mapping Summary 5

Register Name	Type	Register Width (Bits)	Address Offset	CFG_TA_SR1 L3 Physical Address	CFG_TA_SR2 L3 Physical Address	CFG_TA_SR3 L3 Physical Address
L4_TA_COMPONENT_H	R	32	0x0000 0000	0x4A0D A000	0x4A0D C000	0x4A0D E000
L4_TA_COMPONENT_L	R	32	0x0000 0004	0x4A0D A004	0x4A0D C004	0x4A0D E004
L4_TA_CORE_L	R	32	0x0000 0018	0x4A0D A018	0x4A0D C018	0x4A0D E018
L4_TA_CORE_H	R	32	0x0000 001C	0x4A0D A01C	0x4A0D C01C	0x4A0D E01C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4A0D A020	0x4A0D C020	0x4A0D E020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4A0D A024	0x4A0D C024	0x4A0D E024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4A0D A028	0x4A0D C028	0x4A0D E028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4A0D A02C	0x4A0D C02C	0x4A0D E02C

Table 13-336. CFG_TA Register Mapping Summary 6

Register Name	Type	Register Width (Bits)	Address Offset	CFG_TA_MAILBOX L3 Physical Address	CFG_TA_SPINLOCK L3 Physical Address
L4_TA_COMPONENT_H	R	32	0x0000 0000	0x4A0F 5000	0x4A0F 7000
L4_TA_COMPONENT_L	R	32	0x0000 0004	0x4A0F 5004	0x4A0F 7004
L4_TA_CORE_L	R	32	0x0000 0018	0x4A0F 5018	0x4A0F 7018
L4_TA_CORE_H	R	32	0x0000 001C	0x4A0F 501C	0x4A0F 701C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4A0F 5020	0x4A0F 7020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4A0F 5024	0x4A0F 7024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4A0F 5028	0x4A0F 7028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4A0F 502C	0x4A0F 702C

Table 13-337. CFG_TA Register Mapping Summary 7

Register Name	Type	Register Width (Bits)	Address Offset	CFG_TA_SYSCTRL_PADCONF_CORE L3 Physical Address
L4_TA_COMPONENT_H	R	32	0x0000 0000	0x4A10 1000
L4_TA_COMPONENT_L	R	32	0x0000 0004	0x4A10 1004
L4_TA_CORE_L	R	32	0x0000 0018	0x4A10 1018

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Table 13-337. CFG_TA Register Mapping Summary 7 (continued)

Register Name	Type	Register Width (Bits)	Address Offset	CFG_TA_SYSCTRL_PADCONF_CORE L3 Physical Address
L4_TA_CORE_H	R	32	0x0000 001C	0x4A10 101C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4A10 1020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4A10 1024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4A10 1028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4A10 102C

Table 13-338. CFG_TA Register Mapping Summary 8

Register Name	Type	Register Width (Bits)	Address Offset	CFG_TA_FACEDETECT L3 Physical Address
L4_TA_COMPONENT_H	R	32	0x0000 0000	0x4A10 B000
L4_TA_COMPONENT_L	R	32	0x0000 0004	0x4A10 B004
L4_TA_CORE_L	R	32	0x0000 0018	0x4A10 B018
L4_TA_CORE_H	R	32	0x0000 001C	0x4A10 B01C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4A10 B020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4A10 B024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4A10 B028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4A10 B02C

Table 13-339. CFG_TA Register Mapping Summary 9

Register Name	Type	Register Width (Bits)	Address Offset	CFG_TA_MAFW L3 Physical Address	CFG_TA_EMIFFW L3 Physical Address	CFG_TA_GPMCFW L3 Physical Address
L4_TA_COMPONENT_H	R	32	0x0000 0000	0x4A20 A000	0x4A20 D000	0x4A21 1000
L4_TA_COMPONENT_L	R	32	0x0000 0004	0x4A20 A004	0x4A20 D004	0x4A21 1004
L4_TA_CORE_L	R	32	0x0000 0018	0x4A20 A018	0x4A20 D018	0x4A21 1018
L4_TA_CORE_H	R	32	0x0000 001C	0x4A20 A01C	0x4A20 D01C	0x4A21 101C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4A20 A020	0x4A20 D020	0x4A21 1020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4A20 A024	0x4A20 D024	0x4A21 1024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4A20 A028	0x4A20 D028	0x4A21 1028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4A20 A02C	0x4A20 D02C	0x4A21 102C

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Table 13-340. CFG_TA Register Mapping Summary 10

Register Name	Type	Register Width (Bits)	Address Offset	CFG_TA_OCMC RAMFW L3 Physical Address	CFG_TA_SGXF W L3 Physical Address	CFG_TA_ISSF W L3 Physical Address
L4_TA_COMPONENT_H	R	32	0x0000 0000	0x4A21 3000	0x4A21 5000	0x4A21 7000
L4_TA_COMPONENT_L	R	32	0x0000 0004	0x4A21 3004	0x4A21 5004	0x4A21 7004
L4_TA_CORE_L	R	32	0x0000 0018	0x4A21 3018	0x4A21 5018	0x4A21 7018
L4_TA_CORE_H	R	32	0x0000 001C	0x4A21 301C	0x4A21 501C	0x4A21 701C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4A21 3020	0x4A21 5020	0x4A21 7020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4A21 3024	0x4A21 5024	0x4A21 7024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4A21 3028	0x4A21 5028	0x4A21 7028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4A21 302C	0x4A21 502C	0x4A21 702C

Table 13-341. CFG_TA Register Mapping Summary 11

Register Name	Type	Register Width (Bits)	Address Offset	CFG_TA_CORTEXM3FW L3 Physical Address	CFG_TA_DSSF W L3 Physical Address	CFG_TA_SL2F W L3 Physical Address
L4_TA_COMPONENT_H	R	32	0x0000 0000	0x4A21 9000	0x4A21 D000	0x4A21 F000
L4_TA_COMPONENT_L	R	32	0x0000 0004	0x4A21 9004	0x4A21 D004	0x4A21 F004
L4_TA_CORE_L	R	32	0x0000 0018	0x4A21 9018	0x4A21 D018	0x4A21 F018
L4_TA_CORE_H	R	32	0x0000 001C	0x4A21 901C	0x4A21 D01C	0x4A21 F01C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4A21 9020	0x4A21 D020	0x4A21 F020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4A21 9024	0x4A21 D024	0x4A21 F024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4A21 9028	0x4A21 D028	0x4A21 F028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4A21 902C	0x4A21 D02C	0x4A21 F02C

Table 13-342. CFG_TA Register Mapping Summary 12

Register Name	Type	Register Width (Bits)	Address Offset	CFG_TA_IVAHD FW L3 Physical Address	CFG_TA_EMUS SFW L3 Physical Address	CFG_TA_ABEF W L3 Physical Address
L4_TA_COMPONENT_H	R	32	0x0000 0000	0x4A22 1000	0x4A22 7000	0x4A22 9000
L4_TA_COMPONENT_L	R	32	0x0000 0004	0x4A22 1004	0x4A22 7004	0x4A22 9004
L4_TA_CORE_L	R	32	0x0000 0018	0x4A22 1018	0x4A22 7018	0x4A22 9018
L4_TA_CORE_H	R	32	0x0000 001C	0x4A22 101C	0x4A22 701C	0x4A22 901C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4A22 1020	0x4A22 7020	0x4A22 9020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4A22 1024	0x4A22 7024	0x4A22 9024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4A22 1028	0x4A22 7028	0x4A22 9028

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Table 13-342. CFG_TA Register Mapping Summary 12 (continued)

Register Name	Type	Register Width (Bits)	Address Offset	CFG_TA_IVAHD FW L3 Physical Address	CFG_TA_EMUS SFW L3 Physical Address	CFG_TA_ABEF W L3 Physical Address
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4A22 102C	0x4A22 702C	0x4A22 902C

Table 13-343. CFG_TA Register Mapping Summary 13

Register Name	Type	Register Width (Bits)	Address Offset	CFG_TA_L4WKUP L3 Physical Address
L4_TA_COMPONENT_H	R	32	0x0000 0000	0x4A34 0000
L4_TA_COMPONENT_L	R	32	0x0000 0004	0x4A34 0004
L4_TA_CORE_L	R	32	0x0000 0018	0x4A34 0018
L4_TA_CORE_H	R	32	0x0000 001C	0x4A34 001C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4A34 0020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4A34 0024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4A34 0028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4A34 002C

Table 13-344. PER_TA Register Mapping Summary 1

Register Name	Type	Register Width (Bits)	Address Offset	PER_TA_UART 3 L3 Physical Address	PER_TA_GPTIM ER2 L3 Physical Address	PER_TA_GPTIM ER3 L3 Physical Address
L4_TA_COMPONENT_H	R	32	0x0000 0000	0x4802 1000	0x4803 3000	0x4803 5000
L4_TA_COMPONENT_L	R	32	0x0000 0004	0x4802 1004	0x4803 3004	0x4803 5004
L4_TA_CORE_L	R	32	0x0000 0018	0x4802 1018	0x4803 3018	0x4803 5018
L4_TA_CORE_H	R	32	0x0000 001C	0x4802 101C	0x4803 301C	0x4803 501C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4802 1020	0x4803 3020	0x4803 5020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4802 1024	0x4803 3024	0x4803 5024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4802 1028	0x4803 3028	0x4803 5028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4802 102C	0x4803 302C	0x4803 502C

Table 13-345. PER_TA Register Mapping Summary 2

Register Name	Type	Register Width (Bits)	Address Offset	PER_TA_GPTIM ER4 L3 Physical Address	PER_TA_GPTIM ER9 L3 Physical Address	PER_TA_DSS L3 Physical Address
L4_TA_COMPONENT_H	R	32	0x0000 0000	0x4803 7000	0x4803 F000	0x4805 0000
L4_TA_COMPONENT_L	R	32	0x0000 0004	0x4803 7004	0x4803 F004	0x4805 0004

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Table 13-345. PER_TA Register Mapping Summary 2 (continued)

Register Name	Type	Register Width (Bits)	Address Offset	PER_TA_GPTIMER4 L3 Physical Address	PER_TA_GPTIMER9 L3 Physical Address	PER_TA_DSS L3 Physical Address
L4_TA_CORE_L	R	32	0x0000 0018	0x4803 7018	0x4803 F018	0x4805 0018
L4_TA_CORE_H	R	32	0x0000 001C	0x4803 701C	0x4803 F01C	0x4805 001C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4803 7020	0x4803 F020	0x4805 0020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4803 7024	0x4803 F024	0x4805 0024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4803 7028	0x4803 F028	0x4805 0028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4803 702C	0x4803 F02C	0x4805 002C

Table 13-346. PER_TA Register Mapping Summary 3

Register Name	Type	Register Width (Bits)	Address Offset	PER_TA_GPIO2 L3 Physical Address	PER_TA_GPIO3 L3 Physical Address	PER_TA_GPIO4 L3 Physical Address
L4_TA_COMPONENT_H	R	32	0x0000 0000	0x4805 6000	0x4805 8000	0x4805 A000
L4_TA_COMPONENT_L	R	32	0x0000 0004	0x4805 6004	0x4805 8004	0x4805 A004
L4_TA_CORE_L	R	32	0x0000 0018	0x4805 6018	0x4805 8018	0x4805 A018
L4_TA_CORE_H	R	32	0x0000 001C	0x4805 601C	0x4805 801C	0x4805 A01C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4805 6020	0x4805 8020	0x4805 A020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4805 6024	0x4805 8024	0x4805 A024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4805 6028	0x4805 8028	0x4805 A028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4805 602C	0x4805 802C	0x4805 A02C

Table 13-347. PER_TA Register Mapping Summary 4

Register Name	Type	Register Width (Bits)	Address Offset	PER_TA_GPIO5 L3 Physical Address	PER_TA_GPIO6 L3 Physical Address	PER_TA_I2C3 L3 Physical Address
L4_TA_COMPONENT_H	R	32	0x0000 0000	0x4805 C000	0x4805 E000	0x4806 1000
L4_TA_COMPONENT_L	R	32	0x0000 0004	0x4805 C004	0x4805 E004	0x4806 1004
L4_TA_CORE_L	R	32	0x0000 0018	0x4805 C018	0x4805 E018	0x4806 1018
L4_TA_CORE_H	R	32	0x0000 001C	0x4805 C01C	0x4805 E01C	0x4806 101C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4805 C020	0x4805 E020	0x4806 1020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4805 C024	0x4805 E024	0x4806 1024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4805 C028	0x4805 E028	0x4806 1028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4805 C02C	0x4805 E02C	0x4806 102C

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Table 13-348. PER_TA Register Mapping Summary 5

Register Name	Type	Register Width (Bits)	Address Offset	PER_TA_UART 1 L3 Physical Address	PER_TA_UART 2 L3 Physical Address	PER_TA_UART 4 L3 Physical Address
L4_TA_COMPONENT_H	R	32	0x0000 0000	0x4806 B000	0x4806 D000	0x4806 F000
L4_TA_COMPONENT_L	R	32	0x0000 0004	0x4806 B004	0x4806 D004	0x4806 F004
L4_TA_CORE_L	R	32	0x0000 0018	0x4806 B018	0x4806 D018	0x4806 F018
L4_TA_CORE_H	R	32	0x0000 001C	0x4806 B01C	0x4806 D01C	0x4806 F01C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4806 B020	0x4806 D020	0x4806 F020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4806 B024	0x4806 D024	0x4806 F024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4806 B028	0x4806 D028	0x4806 F028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4806 B02C	0x4806 D02C	0x4806 F02C

Table 13-349. PER_TA Register Mapping Summary 6

Register Name	Type	Register Width (Bits)	Address Offset	PER_TA_I2C1 L3 Physical Address	PER_TA_I2C2 L3 Physical Address
L4_TA_COMPONENT_H	R	32	0x0000 0000	0x4807 1000	0x4807 3000
L4_TA_COMPONENT_L	R	32	0x0000 0004	0x4807 1004	0x4807 3004
L4_TA_CORE_L	R	32	0x0000 0018	0x4807 1018	0x4807 3018
L4_TA_CORE_H	R	32	0x0000 001C	0x4807 101C	0x4807 301C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4807 1020	0x4807 3020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4807 1024	0x4807 3024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4807 1028	0x4807 3028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4807 102C	0x4807 302C

Table 13-350. PER_TA Register Mapping Summary 7

Register Name	Type	Register Width (Bits)	Address Offset	PER_TA_SLIMBUS2 L3 Physical Address	PER_TA_ELM L3 Physical Address	PER_TA_GPTIMER10 L3 Physical Address
L4_TA_COMPONENT_H	R	32	0x0000 0000	0x4807 7000	0x4807 9000	0x4808 7000
L4_TA_COMPONENT_L	R	32	0x0000 0004	0x4807 7004	0x4807 9004	0x4808 7004
L4_TA_CORE_L	R	32	0x0000 0018	0x4807 7018	0x4807 9018	0x4808 7018
L4_TA_CORE_H	R	32	0x0000 001C	0x4807 701C	0x4807 901C	0x4808 701C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4807 7020	0x4807 9020	0x4808 7020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4807 7024	0x4807 9024	0x4808 7024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4807 7028	0x4807 9028	0x4808 7028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4807 702C	0x4807 902C	0x4808 702C

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Table 13-351. PER_TA Register Mapping Summary 8

Register Name	Type	Register Width (Bits)	Address Offset	PER_TA_GPTIMER11 L3 Physical Address	PER_TA_MCBSP4 L3 Physical Address	PER_TA_MCSPI1 L3 Physical Address
L4_TA_COMPONENT_H	R	32	0x0000 0000	0x4808 9000	0x4809 7000	0x4809 9000
L4_TA_COMPONENT_L	R	32	0x0000 0004	0x4808 9004	0x4809 7004	0x4809 9004
L4_TA_CORE_L	R	32	0x0000 0018	0x4808 9018	0x4809 7018	0x4809 9018
L4_TA_CORE_H	R	32	0x0000 001C	0x4808 901C	0x4809 701C	0x4809 901C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4808 9020	0x4809 7020	0x4809 9020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4808 9024	0x4809 7024	0x4809 9024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4808 9028	0x4809 7028	0x4809 9028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4808 902C	0x4809 702C	0x4809 902C

Table 13-352. PER_TA Register Mapping Summary 9

Register Name	Type	Register Width (Bits)	Address Offset	PER_TA_MCSPI2 L3 Physical Address	PER_TA_HSMMC1 L3 Physical Address
L4_TA_COMPONENT_H	R	32	0x0000 0000	0x4809 B000	0x4809 D000
L4_TA_COMPONENT_L	R	32	0x0000 0004	0x4809 B004	0x4809 D004
L4_TA_CORE_L	R	32	0x0000 0018	0x4809 B018	0x4809 D018
L4_TA_CORE_H	R	32	0x0000 001C	0x4809 B01C	0x4809 D01C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4809 B020	0x4809 D020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4809 B024	0x4809 D024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4809 B028	0x4809 D028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4809 B02C	0x4809 D02C

Table 13-353. PER_TA Register Mapping Summary 10

Register Name	Type	Register Width (Bits)	Address Offset	PER_TA_HSMMC3 L3 Physical Address
L4_TA_COMPONENT_H	R	32	0x0000 0000	0x480A E000
L4_TA_COMPONENT_L	R	32	0x0000 0004	0x480A E004
L4_TA_CORE_L	R	32	0x0000 0018	0x480A E018
L4_TA_CORE_H	R	32	0x0000 001C	0x480A E01C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x480A E020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x480A E024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x480A E028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x480A E02C

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Table 13-354. PER_TA Register Mapping Summary 11

Register Name	Type	Register Width (Bits)	Address Offset	PER_TA_HDQ L3 Physical Address	PER_TA_HSMM C2 L3 Physical Address	PER_TA_MCSPI 3 L3 Physical Address
L4_TA_COMPONENT_H	R	32	0x0000 0000	0x480B 3000	0x480B 5000	0x480B 9000
L4_TA_COMPONENT_L	R	32	0x0000 0004	0x480B 3004	0x480B 5004	0x480B 9004
L4_TA_CORE_L	R	32	0x0000 0018	0x480B 3018	0x480B 5018	0x480B 9018
L4_TA_CORE_H	R	32	0x0000 001C	0x480B 301C	0x480B 501C	0x480B 901C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x480B 3020	0x480B 5020	0x480B 9020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x480B 3024	0x480B 5024	0x480B 9024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x480B 3028	0x480B 5028	0x480B 9028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x480B 302C	0x480B 502C	0x480B 902C

Table 13-355. PER_TA Register Mapping Summary 12

Register Name	Type	Register Width (Bits)	Address Offset	PER_TA_MCSPI 4 L3 Physical Address	PER_TA_HSMM C4 L3 Physical Address	PER_TA_HSMM C5 L3 Physical Address
L4_TA_COMPONENT_H	R	32	0x0000 0000	0x480B B000	0x480D 2000	0x480D 6000
L4_TA_COMPONENT_L	R	32	0x0000 0004	0x480B B004	0x480D 2004	0x480D 6004
L4_TA_CORE_L	R	32	0x0000 0018	0x480B B018	0x480D 2018	0x480D 6018
L4_TA_CORE_H	R	32	0x0000 001C	0x480B B01C	0x480D 201C	0x480D 601C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x480B B020	0x480D 2020	0x480D 6020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x480B B024	0x480D 2024	0x480D 6024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x480B B028	0x480D 2028	0x480D 6028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x480B B02C	0x480D 202C	0x480D 602C

Table 13-356. PER_TA Register Mapping Summary 13

Register Name	Type	Register Width (Bits)	Address Offset	PER_TA_I2C4 L3 Physical Address
L4_TA_COMPONENT_H	R	32	0x0000 0000	0x4835 1000
L4_TA_COMPONENT_L	R	32	0x0000 0004	0x4835 1004
L4_TA_CORE_L	R	32	0x0000 0018	0x4835 1018
L4_TA_CORE_H	R	32	0x0000 001C	0x4835 101C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4835 1020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4835 1024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4835 1028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4835 102C

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Table 13-357. WKUP_TA Register Mapping Summary 1

Register Name	Type	Register Width (Bits)	Address Offset	WKUP_TA_32K TIMER L3 Physical Address	WKUP_TA_PRM L3 Physical Address	WKUP_TA_SCRM L3 Physical Address
L4_TA_COMPONENT_H	R	32	0x0000 0000	0x4A30 5000	0x4A30 8000	0x4A30 B000
L4_TA_COMPONENT_L	R	32	0x0000 0004	0x4A30 5004	0x4A30 8004	0x4A30 B004
L4_TA_CORE_L	R	32	0x0000 0018	0x4A30 5018	0x4A30 8018	0x4A30 B018
L4_TA_CORE_H	R	32	0x0000 001C	0x4A30 501C	0x4A30 801C	0x4A30 B01C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4A30 5020	0x4A30 8020	0x4A30 B020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4A30 5024	0x4A30 8024	0x4A30 B024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4A30 5028	0x4A30 8028	0x4A30 B028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4A30 502C	0x4A30 802C	0x4A30 B02C

Table 13-358. WKUP_TA Register Mapping Summary 2

Register Name	Type	Register Width (Bits)	Address Offset	WKUP_TA_SYSCTRL_GENERAL_WKUP L3 Physical Address	WKUP_TA_GPIO1 L3 Physical Address	WKUP_TA_WDTIMER2 L3 Physical Address
L4_TA_COMPONENT_H	R	32	0x0000 0000	0x4A30 D000	0x4A31 1000	0x4A31 5000
L4_TA_COMPONENT_L	R	32	0x0000 0004	0x4A30 D004	0x4A31 1004	0x4A31 5004
L4_TA_CORE_L	R	32	0x0000 0018	0x4A30 D018	0x4A31 1018	0x4A31 5018
L4_TA_CORE_H	R	32	0x0000 001C	0x4A30 D01C	0x4A31 101C	0x4A31 501C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4A30 D020	0x4A31 1020	0x4A31 5020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4A30 D024	0x4A31 1024	0x4A31 5024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4A30 D028	0x4A31 1028	0x4A31 5028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4A30 D02C	0x4A31 102C	0x4A31 502C

Table 13-359. WKUP_TA Register Mapping Summary 3

Register Name	Type	Register Width (Bits)	Address Offset	WKUP_TA_DM_TIMER1MS_1 L3 Physical Address	WKUP_TA_KEYBOARD L3 Physical Address
L4_TA_COMPONENT_H	R	32	0x0000 0000	0x4A31 9000	0x4A31 D000
L4_TA_COMPONENT_L	R	32	0x0000 0004	0x4A31 9004	0x4A31 D004
L4_TA_CORE_L	R	32	0x0000 0018	0x4A31 9018	0x4A31 D018
L4_TA_CORE_H	R	32	0x0000 001C	0x4A31 901C	0x4A31 D01C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4A31 9020	0x4A31 D020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4A31 9024	0x4A31 D024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4A31 9028	0x4A31 D028

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Table 13-359. WKUP_TA Register Mapping Summary 3 (continued)

Register Name	Type	Register Width (Bits)	Address Offset	WKUP_TA_DM_TIMER1MS_1 L3 Physical Address	WKUP_TA_KEYBOARD L3 Physical Address
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4A31 902C	0x4A31 D02C

Table 13-360. WKUP_TA Register Mapping Summary 4

Register Name	Type	Register Width (Bits)	Address Offset	WKUP_TA_SYSCTRL_PADCONF_WKUP L3 Physical Address
L4_TA_COMPONENT_H	R	32	0x0000 0000	0x4A31 F000
L4_TA_COMPONENT_L	R	32	0x0000 0004	0x4A31 F004
L4_TA_CORE_L	R	32	0x0000 0018	0x4A31 F018
L4_TA_CORE_H	R	32	0x0000 001C	0x4A31 F01C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4A31 F020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4A31 F024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4A31 F028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4A31 F02C

Table 13-361. WKUP_TA Register Mapping Summary 5

Register Name	Type	Register Width (Bits)	Address Offset	WKUP_TA_SAR_RAM L3 Physical Address
L4_TA_COMPONENT_H	R	32	0x0000 0000	0x4A32 A000
L4_TA_COMPONENT_L	R	32	0x0000 0004	0x4A32 A004
L4_TA_CORE_L	R	32	0x0000 0018	0x4A32 A018
L4_TA_CORE_H	R	32	0x0000 001C	0x4A32 A01C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4A32 A020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4A32 A024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4A32 A028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4A32 A02C

13.3.5.3.2 L4 Target Agent (L4 TA) Register Description

Table 13-362 through Table 13-376 describe the L4 TA registers.

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Table 13-362. L4_TA_COMPONENT_H

Address Offset	0x0000 0000
Physical Address	See Table 13-331 to Table 13-343.
Description	Contains a component code and revision.
Type	R

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

Bits	Field Name	Description	Type	Reset
31:0	RESERVED	Read returns 0	R	0x0000 000

Table 13-363. Register Call Summary for Register L4_TA_COMPONENT_H

L4 Interconnects

- L4 Target Agent (L4 TA) Register Summary: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23] [24] [25] [26] [27] [28] [29] [30]

Table 13-364. L4_TA_COMPONENT_L

Address Offset	0x0000 0004
Physical Address	See Table 13-331 to Table 13-343.
Description	Contains a component code and revision.
Type	R

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CODE																REV															

Bits	Field Name	Description	Type	Reset
31:16	CODE	Interconnect code.	R	See (1).
15:0	REV	Component revision code.	R	See (1).

(1) TI Internal Data

Table 13-365. Register Call Summary for Register L4_TA_COMPONENT_L

L4 Interconnects

- L4 Target Agent (L4 TA) Register Summary: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23] [24] [25] [26] [27] [28] [29] [30]

Table 13-366. L4_TA_CORE_L

Address Offset	0x0000 0018
Physical Address	See Table 13-331 to Table 13-343.
Description	Contains a component code and revision.
Type	R

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CORE_CODE																CORE_REV															

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Bits	Field Name	Description	Type	Reset
31:16	CORE_CODE	Interconnect core code	R	See (1).
15:0	CORE_REV	Component revision code code	R	See (1).

(1) TI Internal Data

Table 13-367. Register Call Summary for Register L4_TA_CORE_L

L4 Interconnects

- L4 Target Agent (L4 TA) Register Summary: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23] [24] [25] [26] [27] [28] [29] [30]

Table 13-368. L4_TA_CORE_H

Address Offset	0x0000 001C
Physical Address	See Table 13-331 to Table 13-343.
Description	Contains a component code and revision.
Type	R

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																VENDOR_CODE															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x0000
15:0	VENDOR_CODE	Vendor revision core code	R	See (1).

(1) TI Internal Data

Table 13-369. Register Call Summary for Register L4_TA_CORE_H

L4 Interconnects

- L4 Target Agent (L4 TA) Register Summary: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23] [24] [25] [26] [27] [28] [29] [30]

Table 13-370. L4_TA_AGENT_CONTROL_L

Address Offset	0x0000 0020
Physical Address	See Table 13-331 to Table 13-343.
Description	Enable error reporting
Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							SERROR_REP	RESERVED													REQ_TIMEOUT			RESERVED							OCP_RESET

Bits	Field Name	Description	Type	Reset
31:25	RESERVED	Read returns 0.	R	0x00
24	SERROR_REP	Enable logging of error	R	0x0
23:11	RESERVED	Read returns 0.	UNDEFINED_TYPE_STRING	

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Bits	Field Name	Description	Type	Reset
10:8	REQ_TIMEOUT	Time-out Bound. Values are: 0 - No time-out 1 - 1x base cycles. 2 - 4x base cycles. 3 - 16x base cycles. 4 - 64x base cycles.	RW	0x2
7:1	RESERVED	Read returns 0.	R	0x00
0	OCP_RESET	The OCP_RESET field controls the OCP reset signal to the attached core. Setting this bit clears any pending transfers and resets the OCP interface. The bit must be cleared to deassert the OCP reset signal. When the software reset feature is available on a target agent, the target agent OCP must also have a reset signal directed to the target core.	RW	0

Table 13-371. Register Call Summary for Register L4_TA_AGENT_CONTROL_L

L4 Interconnects

- Time-Out: [0] [1] [2] [3] [4]
- Error Recovery: [5] [6]
- Operational Modes Configuration: [7] [8] [9] [10]
- L4 Target Agent (L4 TA) Register Summary: [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23] [24] [25] [26] [27] [28] [29] [30] [31] [32] [33] [34] [35] [36] [37] [38] [39] [40] [41]

Table 13-372. L4_TA_AGENT_CONTROL_H

Address Offset	0x0000 0024
Physical Address	See Table 13-331 to Table 13-343.
Description	Enable clock power management
Type	R

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							EXT_CLOCK	RESERVED							

Bits	Field Name	Description	Type	Reset
31:9	RESERVED	Read returns 0.	R	0x000000
8	EXT_CLOCK	When set to 1, the ext_clk_off_i signal on a target agent indicates when the target agent should shut off.	R	0
7:0	RESERVED	Read returns 0.	R	0x00

Table 13-373. Register Call Summary for Register L4_TA_AGENT_CONTROL_H

L4 Interconnects

- L4 Target Agent (L4 TA) Register Summary: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23] [24] [25] [26] [27] [28] [29] [30]

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Table 13-374. L4_TA_AGENT_STATUS_L

Address Offset	0x0000 0028
Physical Address	See Table 13-331 to Table 13-343.
Description	Error reporting
Type	R

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								RESERVED															REQ_TIMEOUT	RESERVED							

Bits	Field Name	Description	Type	Reset
31:24	RESERVED	Read returns 0.	R	0x00
23:9	RESERVED	Read returns 0.	R	0x0001
8	REQ_TIMEOUT	Time-out status: 0x0: No request time-out 0x1: A request time-out has occurred	R 1toCLR	0
7:0	RESERVED	Read returns 0.	R	0x00

Table 13-375. Register Call Summary for Register L4_TA_AGENT_STATUS_L

L4 Interconnects

- Time-Out: [0] [1]
- Error Recovery: [2]
- Operational Modes Configuration: [3] [4]
- L4 Target Agent (L4 TA) Register Summary: [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23] [24] [25] [26] [27] [28] [29] [30] [31] [32] [33] [34] [35]

Table 13-376. L4_TA_AGENT_STATUS_H

Address Offset	0x0000 002C
Physical Address	See Table 13-331 to Table 13-343.
Description	Error reporting
Type	R

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

Bits	Field Name	Description	Type	Reset
31:0	RESERVED	Read returns 0	R	0x0000 000

Table 13-377. Register Call Summary for Register L4_TA_AGENT_STATUS_H

L4 Interconnects

- L4 Target Agent (L4 TA) Register Summary: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23] [24] [25] [26] [27] [28] [29] [30]

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13.3.5.4 L4 Link Agent (L4 LA)

13.3.5.4.1 L4 Link Agent (L4 LA) Register Summary

Table 13-378 summarizes the L4 LA register mapping.

Table 13-378. LA Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	PER_LA L3 Physical Address	CFG_LA L3 Physical Address	WKUP_LA L3 Physical Address
L4_LA_COMPONENT_L	R	32	0x0000 0000	0x4800 0800	0x4A00 0800	0x4A30 0800
L4_LA_COMPONENT_H	R	32	0x0000 0004	0x4800 0804	0x4A00 0804	0x4A30 0804
L4_LA_NETWORK_L	R	32	0x0000 0010	0x4800 0810	0x4A00 0810	0x4A30 0810
L4_LA_NETWORK_H	R	32	0x0000 0014	0x4800 0814	0x4A00 0814	0x4A30 0814
L4_LA_INITIATOR_INFO_L	R	32	0x0000 0018	0x4800 0818	0x4A00 0818	0x4A30 0818
L4_LA_INITIATOR_INFO_H	R	32	0x0000 001C	0x4800 081C	0x4A00 081C	0x4A30 081C
L4_LA_NETWORK_CONTROL_L	RW	32	0x0000 0020	0x4800 0820	0x4A00 0820	0x4A30 0820
L4_LA_NETWORK_CONTROL_H	RW	32	0x0000 0024	0x4800 0824	0x4A00 0824	0x4A30 0824

13.3.5.4.2 L4 Link Agent (L4 LA) Register Description

Table 13-379 through Table 13-395 describe the L4 LA registers.

Table 13-379. L4_LA_COMPONENT_L

Address Offset	0x0000 0000
Physical Address	0x4800 0800 0x4A00 0800 0x4A30 0800
Description	Contain a component code and revision, which are used to identify the hardware of the component.
Type	R

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CODE																REV															

Bits	Field Name	Description	Type	Reset
31:16	CODE	Interconnect code.	R	See (1).
15:0	REV	Component revision code.	R	See (1).

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Table 13-380. Register Call Summary for Register L4_LA_COMPONENT_L

L4 Interconnects

- L4 Link Agent (L4 LA) Register Summary: [0]

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Table 13-381. L4_LA_COMPONENT_H

Address Offset	0x0000 0004
Physical Address	0x4800 0804 0x4A00 0804 0x4A30 0804
Description	Contain a component code and revision, which are used to identify the hardware of the component.
Type	R

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

Bits	Field Name	Description	Type	Reset
31:0	RESERVED	Read returns 0.	R	0x0000 0000

Table 13-382. Register Call Summary for Register L4_LA_COMPONENT_H

L4 Interconnects

- L4 Link Agent (L4 LA) Register Summary: [0]

Table 13-383. L4_LA_NETWORK_L

Address Offset	0x0000 0010
Physical Address	0x4800 0810 0x4A00 0810 0x4A30 0810
Description	Identify the interconnect
Type	R

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

Bits	Field Name	Description	Type	Reset
31:0	RESERVED	Read returns 0	R	0x0000 0000

Table 13-384. Register Call Summary for Register L4_LA_NETWORK_L

L4 Interconnects

- L4 Link Agent (L4 LA) Register Summary: [0]

Table 13-385. L4_LA_NETWORK_H

Address Offset	0x0000 0014
Physical Address	0x4800 0814 0x4A00 0814 0x4A30 0814
Description	Identify the interconnect
Type	R

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																															

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Bits	Field Name	Description	Type	Reset
31:0	ID	The ID field uniquely identifies this interconnect.	R	0x00010000

Table 13-386. Register Call Summary for Register L4_LA_NETWORK_H

L4 Interconnects
- L4 Link Agent (L4 LA) Register Summary: [0]

Table 13-387. L4_LA_INITIATOR_INFO_L

Address Offset	0x0000 0018
Physical Address	0x4800 0818 0x4A00 0818 0x4A30 0818
Description	Contain initiator subsystem information.
Type	R

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				PROT_GROUPS				NUMBER_REGIONS								RESERVED								SEGMENTS							

Bits	Field Name	Description	Type	Reset
31:28	RESERVED	Read returns 0.	R	0x0
27:24	PROT_GROUPS	Number of protection group of in the current L4 0x0: No protection group 0x1: 1 protection group 0x2: 2 protection groups .... 0x8: 8 protection groups 0x9 to 0xF: Reserved	R	see Table 13-389
23:16	NUMBER_REGIONS	Number of regions in the current L4 0x0: Reserved 0x1: 1 region 0x2: 2 regions .... Max regions +1 to 0xFF: Reserved, maximum regions is listed in Table 13-389	R	see Table 13-389
15:4	RESERVED	Read returns 0.	R	0x000
3:0	SEGMENTS	Number of segments in the current L4 0x0: Reserved 0x1: 1 segment 0x2: 2 segments .... 0x8: 8 segments	R	see Table 13-389

Table 13-388. Register Call Summary for Register L4_LA_INITIATOR_INFO_L

L4 Interconnects
- L4 Firewalls: [0]
- L4 Link Agent (L4 LA) Register Summary: [1]

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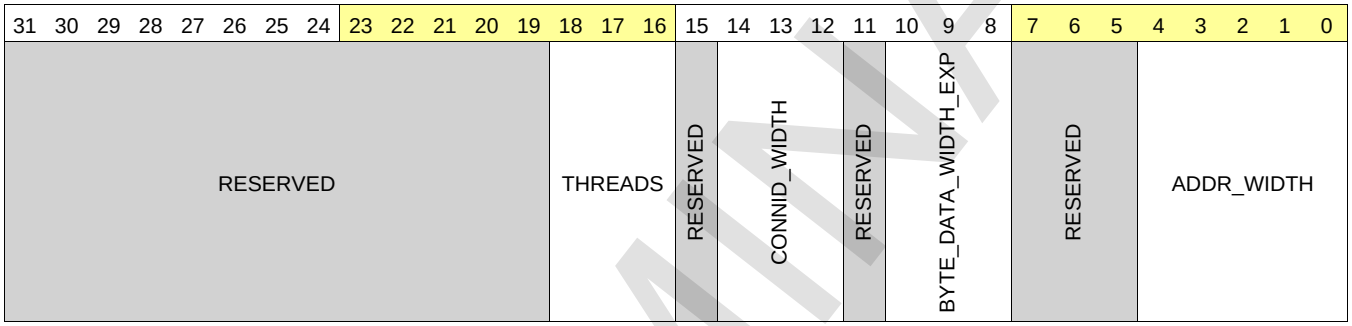
Table 13-389. Reset value for L4_LA_INITIATOR_INFO_L

Field Name	L4 PER	L4 CFG	L4 WKUP
PROT_GROUPS	0x8	0x8	0x0
NUMBER_REGIONS	0x55	0x5C	0x20
SEGMENTS	0x2	0x5	0x3

Table 13-390. L4_LA_INITIATOR_INFO_H

Address Offset	0x0000 001C
Physical Address	0x4800 081C 0x4A00 081C 0x4A30 081C
Description	Contain initiator subsystem information.
Type	R



Bits	Field Name	Description	Type	Reset
31:19	RESERVED	Read returns 0.	R	0x0000
18:16	THREADS	The THREADS field specifies the number of initiator threads connected to the interconnect. The field contains read-only configuration information for the initiator subsystem.	R	see Table 13-392
15	RESERVED	Read returns 0.	R	0
14:12	CONNID_WIDTH	The initiator subsystem ConnID width. The CONNID_WIDTH field contains read-only configuration information for the initiator subsystem.	R	see Table 13-392
11	RESERVED	Read returns 0.	R	0
10:8	BYTE_DATA_WIDTH_EXP	This field specifies the initiator subsystem data width.The BYTE_DATA_WIDTH_EXP field contains read-only configuration information for the initiator subsystem. 0x1: 16-bit data width is specified 0x2: 32-bit data width is specified	R	see Table 13-392
7:5	RESERVED	Read returns 0.	R	0x0
4:0	ADDR_WIDTH	This field specifies the initiator subsystem address width. The ADDR_WIDTH field contains read-only configuration information for the initiator subsystem.	R	see Table 13-392

Table 13-391. Register Call Summary for Register L4_LA_INITIATOR_INFO_H

L4 Interconnects

- L4 Link Agent (L4 LA) Register Summary: [0]

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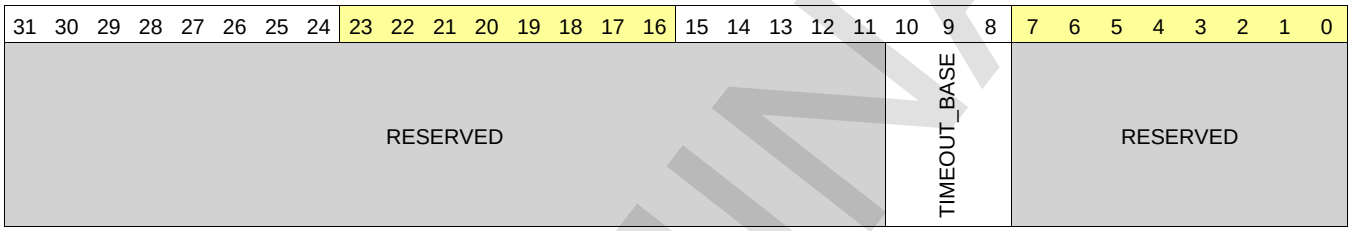
Table 13-392. Reset value for L4_LA_INITIATOR_INFO_H

Field Name	L4 PER	L4 CFG	L4 WKUP
THREADS	0x4	0x1	0x1
CONNID_WIDTH	0x4	0x4	0x0
BYTE_DATA_WIDTH_EXP	0x2	0x2	0x2
ADDR_WIDTH	0x18	0x18	0x12

Table 13-393. L4_LA_NETWORK_CONTROL_L

Address Offset	0x0000 0020
Physical Address	0x4800 0820 0x4A00 0820 0x4A30 0820
Description	Control interconnect minimum timeout values.
Type	RW



Bits	Field Name	Description	Type	Reset
31:11	RESERVED	Read returns 0.	R	0x000000
10:8	TIMEOUT_BASE	The TIMEOUT_BASE field indicates the time-out period (that is, base cycles) for the highest frequency time-base signal sent from the L4 initiator subsystem to all target agents that have time-out enabled. Values for the field are: 0 - Time-out disabled 1 - L4 interconnect clock cycles divided by 64 2 - L4 interconnect clock cycles divided by 256 3 - L4 interconnect clock cycles divided by 1024 4 - L4 interconnect clock cycles divided by 4096	RW	0x4
7:0	RESERVED	Read returns 0.	R	0x00

Table 13-394. Register Call Summary for Register L4_LA_NETWORK_CONTROL_L

L4 Interconnects

- Time-Out: [0] [1] [2]
- Operational Modes Configuration: [3] [4]
- L4 Link Agent (L4 LA) Register Summary: [5]

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Table 13-395. L4_LA_NETWORK_CONTROL_H

Address Offset	0x0000 0024
Physical Address	0x4800 0824 0x4A00 0824 0x4A30 0824
Description	Control interconnect global power control
Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							CLOCK_GATE_DISABLE	RESERVED			THREAD0_PRI	RESERVED											EXT_CLOCK	RESERVED							

Bits	Field Name	Description	Type	Reset
31:25	RESERVED	Read returns 0.	R	0x00
24	CLOCK_GATE_DISABLE	When set to 1 this field disables all clock gating.	RW	0
23:21	RESERVED	Read returns 0.	R	0x0
20	THREAD0_PRI	Sets thread priority. If the field is set to 0, the default, all initiator threads are treated the same. Setting the THREAD0_PRI field to 1 assigns a higher arbitration priority to thread 0 of the first initiator OCP interface. To avoid starvation, arbitration is imposed by the initiator subsystem. When multiple requests from different initiator threads are dispatched to targets simultaneously, the oldest request is dispatched first. If thread 0 is assigned a higher priority, a request on thread 0 always wins arbitration. Assigning thread 0 of the first initiator OCP the highest priority on a request or response can result in the starvation of other threads.	R	1
19:9	RESERVED	Read returns 0.	R	0x000
8	EXT_CLOCK	When set to 1, the ext_clk_off_i signal on the initiator subsystem instructs the entire L4 to shut off.	R	1
7:0	RESERVED	Read returns 0.	R	0x00

Table 13-396. Register Call Summary for Register L4_LA_NETWORK_CONTROL_H

L4 Interconnects

- L4 Link Agent (L4 LA) Register Summary: [0]

13.3.5.5 L4 Address Protection (L4 AP)

13.3.5.5.1 L4 Address Protection (L4 AP) Register Summary

Table 13-397 summarizes the L4 AP register mapping.

Table 13-397. L4 AP Register Summary

Register Name	Type	Register Width (Bits)	Address Offset	PER_AP Physical Address	CFG_AP Physical Address
L4_AP_COMPONENT_L	R	32	0x0000 0000	0x4800 0 000	0x4A00 0 000
L4_AP_COMPONENT_H	R	32	0x0000 0004	0x4800 0004	0x4A00 0004

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Table 13-397. L4 AP Register Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	PER_AP Physical Address	CFG_AP Physical Address
L4_AP_SEGMENT_i_L (1)	RW	32	0x0000 0100 + (0x08*i)	0x4800 0100 + (0x08*i)	0x4A00 0100 + (0x08*i)
L4_AP_SEGMENT_i_H (1)	RW	32	0x0000 0104 + (0x08*i)	0x4800 0104 + (0x08*i)	0x4A00 0104 + (0x08*i)
L4_AP_PROT_GROUP_MEMBERS_k_L (2)	R	32	0x0000 0200 + (0x08*k)	0x4800 0200 + (0x08*k)	0x4A00 0200 + (0x08*k)
L4_AP_PROT_GROUP_MEMBERS_k_H (2)	R	32	0x0000 0204 + (0x08*k)	0x4800 0204 + (0x08*k)	0x4A00 0204 + (0x08*k)
L4_AP_PROT_GROUP_ROLES_k_L (2)	R	32	0x0000 0280 + (0x08*k)	0x4800 0280 + (0x08*k)	0x4A00 0280 + (0x08*k)
L4_AP_PROT_GROUP_ROLES_k_H (2)	R	32	0x0000 0284 + (0x08*k)	0x4800 0284 + (0x08*k)	0x4A00 0284 + (0x08*k)
L4_AP_REGION_l_L (3)	RW	32	0x0000 0300 + (0x08*l)	0x4800 0300 + (0x08*l)	0x4A00 0300 + (0x08*l)
L4_AP_REGION_l_H (3)	RW	32	0x0000 0304 + (0x08*l)	0x4800 0304 + (0x08*l)	0x4A00 0304 + (0x08*l)

(1) i = 0 to 1 for PER_AP
i = 0 to 6 for CFG_AP
(2) k = 0 to 7 for PER_AP
k = 0 to 7 for CFG_AP
(3) l = 0 to 96 for PER_AP
l = 0 to 113 for CFG_AP

13.3.5.5.2 L4 Address Protection (L4 AP) Register Description

Table 13-398 through Table 13-422 describe the L4 AP registers.

Table 13-398. L4_AP_COMPONENT_L

Address Offset	0x000
Physical address	0x4800 0 000 0x4A00 0 000
Description	Contains a component code and revision, which are used to identify the hardware of the component.
Type	R

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CODE																REV															

Bits	Field Name	Description	Type	Reset
31:16	CODE	Interconnect code	R	See (1).
15:0	REV	Component revision code	R	See (1).

(1) TI Internal Data

Table 13-399. Register Call Summary for Register L4_AP_COMPONENT_L

L4 Interconnects
- L4 Address Protection (L4 AP) Register Summary: [0]

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Table 13-400. L4_AP_COMPONENT_H

Address Offset	0x004
Physical address	0x4800 0004 0x4A00 0004
Description	Contains a component code and revision, which are used to identify the hardware of the component.
Type	R

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																															

Bits	Field Name	Description	Type	Reset
31:0	Reserved	Read returns 0	R	0x0000 0000

Table 13-401. Register Call Summary for Register L4_AP_COMPONENT_H

L4 Interconnects

- L4 Address Protection (L4 AP) Register Summary: [0]

Table 13-402. L4_AP_SEGMENT_i_L

Address Offset	0x100 + (0x08*i)	**Index**	i = 0 to 1 for PER_AP i = 0 to 6 for CFG_AP
Physical address	0x4800 0100 + (0x08*i) 0x4A00 0100 + (0x08*i)		
Description	Define the base address of each segments		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								BASE																							

Bits	Field Name	Description	Type	Reset
31:24	Reserved	Read returns 0.	R	0x00
23:0	BASE	The base address of the segment (with 0s from bit 0 to bit SIZE-1).	R	see Table 13-406

Table 13-403. Register Call Summary for Register L4_AP_SEGMENT_i_L

L4 Interconnects

- L4 Firewall Address and Protection Register Settings: [0]
- L4 Address Protection (L4 AP) Register Summary: [1]

Table 13-404. L4_AP_SEGMENT_i_H

Address Offset	0x104 + (0x08*i)	**Index**	i = 0 to 1 for PER_AP i = 0 to 6 for CFG_AP
Physical address	0x4800 0104 + (0x08*i) 0x4A00 0104 + (0x08*i)		
Description	Define the size of each segments		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																												SIZE			

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Bits	Field Name	Description	Type	Reset
31:5	Reserved	Read returns 0.	R	0x0000000
4:0	SIZE	Segment size is a power of 2, where 2^{SIZE} is the byte size of a segment (all segment registers use the same size).	R	see Table 13-406

Table 13-405. Register Call Summary for Register L4_AP_SEGMENT_i_H

L4 Interconnects

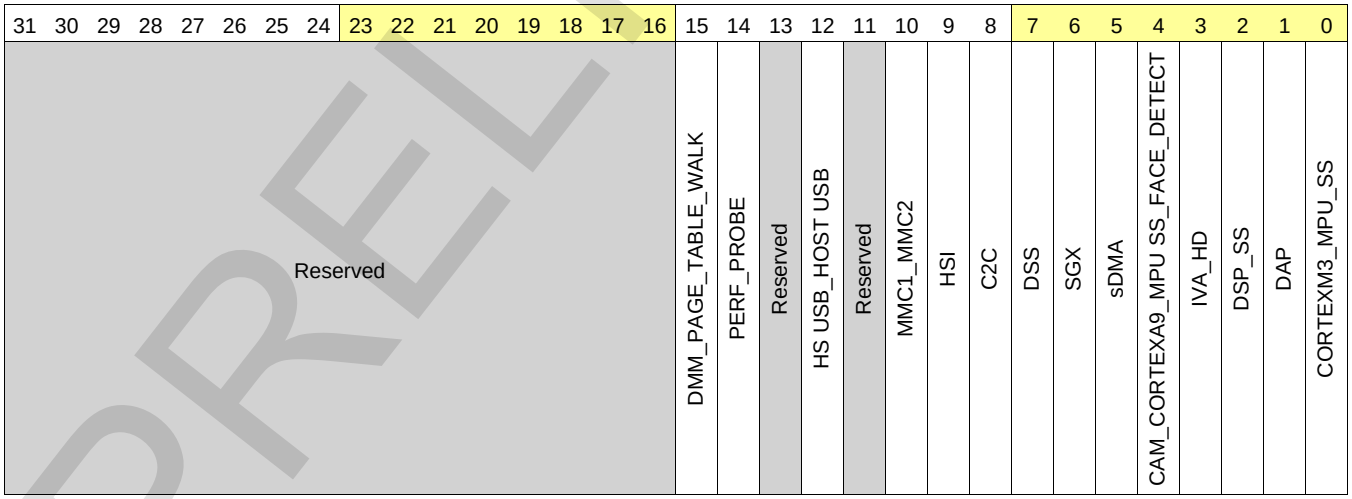
- L4 Firewall Address and Protection Register Settings: [0]
- L4 Address Protection (L4 AP) Register Summary: [1]

Table 13-406. Reset Value for L4_AP_SEGMENT_i

i	L4 PER		L4 CFG	
	BASE	SIZE	BASE	SIZE
0	0x00 0000	0x15	0x00 0000	0x13
1	0x02 0000	0x15	0x08 0000	0x13
2	-	-	0x10 0000	0x13
3	-	-	0x18 0000	0x13
4	-	-	0x20 0000	0x13
5	-	-	0x28 0000	0x13
6	-	-	0x30 0000	0x13

Table 13-407. L4_AP_PROT_GROUP_MEMBERS_k_L

Address Offset	0x200 + (0x08*k)	**Index**	k = 0 to 7 for PER_AP k = 0 to 7 for CFG_AP
Physical address	0x4800 0200 + (0x08*k) 0x4A00 0200 + (0x08*k)		
Description	Define ConnID bit vectors for a protection group.		
Type	R		



Bits	Field Name	Description	Type	Reset
31:16	Reserved	Reserved	R	0x000000000000
15	DMM_PAGE_TABLE_WALK	Included in the protection group k 0x0: Not a member 0x1: Member	RW	See Table 13-409

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Bits	Field Name	Description	Type	Reset
14	PERF_PROBE	Included in the protection group k 0x0: Not a member 0x1: Member	RW	See Table 13-409
13	Reserved	Reserved	RW	See Table 13-409
12	HS USB_HOST USB	Included in the protection group k 0x0: Not a member 0x1: Member	RW	See Table 13-409.
11	Reserved	Reserved	RW	See Table 13-409.
10	MMC1_MMC2	Included in the protection group k 0x0: Not a member 0x1: Member	RW	See Table 13-409.
9	HSI	Included in the protection group k 0x0: Not a member 0x1: Member	RW	See Table 13-409.
8	C2C	Included in the protection group k 0x0: Not a member 0x1: Member	RW	See Table 13-409.
7	DSS	Included in the protection group k 0x0: Not a member 0x1: Member	RW	See Table 13-409.
6	SGX	Included in the protection group k 0x0: Not a member 0x1: Member	RW	See Table 13-409.
5	sDMA	Included in the protection group k 0x0: Not a member 0x1: Member	RW	See Table 13-409.
4	CAM_CORTEXA9_MPU SS_FACE_DETECT	Included in the protection group k 0x0: Not a member 0x1: Member	RW	See Table 13-409.
3	IVA_HD	Included in the protection group k 0x0: Not a member 0x1: Member	RW	See Table 13-409.
2	DSP_SS	Included in the protection group k 0x0: Not a member 0x1: Member	RW	See Table 13-409.
1	DAP	Included in the protection group k 0x0: Not a member 0x1: Member	RW	See Table 13-409.
0	CORTEXM3_MPU_SS	Included in the protection group k 0x0: Not a member 0x1: Member	RW	See Table 13-409

Table 13-408. Register Call Summary for Register L4_AP_PROT_GROUP_MEMBERS_k_L

L4 Interconnects

- Protection Group: [0] [1]
- L4 Firewall Address and Protection Register Settings: [2]
- Operational Modes Configuration: [3]
- L4 Address Protection (L4 AP) Register Summary: [4]

Table 13-409. Reset Value for L4_AP_PROT_GROUP_MEMBERS_k

k	L4 PER		L4 CFG	
	Type	Reset Value	Type	Reset Value
0	RW	0xFFFF(1)	RW	0xFFFF(1)
1	RW	0xFFFF(1)	RW	0xFFFF(1)
2	RW	0xFFFF(1)	RW	0x0000(1)
3	RW	0xFFFF	RW	0xFFFF(1)

(1) Value exported from SCM and valid for GP device only (see *System Control Module*). The values of the other protection registers can be modified during run time.

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Table 13-409. Reset Value for L4_AP_PROT_GROUP_MEMBERS_k (continued)

k	L4 PER		L4 CFG	
	Type	Reset Value	Type	Reset Value
4	RW	0xFFFF	RW	0xFFFF(1)
5	RW	0xFFFF	RW	0xFFFF
6	RW	0xFFFF	RW	0xFFFF
7	RW	0xFFFF	RW	0xFFFF

Table 13-410. L4_AP_PROT_GROUP_MEMBERS_k_H

Address Offset	0x204 + (0x08*k)	**Index**	k = 0 to 7 for PER_AP k = 0 to 7 for CFG_AP
Physical address	0x4800 0204 + (0x08*k) 0x4A00 0204 + (0x08*k)		
Description	Define ConnID bit vectors for a protection group.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																															

Bits	Field Name	Description	Type	Reset
31:0	Reserved	Read returns 0's	R	0x0000 0000

Table 13-411. Register Call Summary for Register L4_AP_PROT_GROUP_MEMBERS_k_H

L4 Interconnects

- L4 Address Protection (L4 AP) Register Summary: [0]

Table 13-412. L4_AP_PROT_GROUP_ROLES_k_L

Address Offset	0x200 + (0x08*k)	**Index**	k = 0 to 7 for PER_AP k = 0 to 7 for CFG_AP
Physical address	0x4800 0280 + (0x08*k) 0x4A00 0280 + (0x08*k)		
Description	Define MReqInfo bit vectors for a protection group.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																ENABLE															

Bits	Field Name	Description	Type	Reset
31:16	Reserved	Read returns 0	R	0x0000
15:0	ENABLE	Setting of type acces allowed for the group of initiators.	R	0xFFFF

Table 13-413. Register Call Summary for Register L4_AP_PROT_GROUP_ROLES_k_L

L4 Interconnects

- Protection Group: [0]
- L4 Firewall Address and Protection Register Settings: [1]
- Operational Modes Configuration: [2]
- L4 Address Protection (L4 AP) Register Summary: [3]

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Table 13-414. Reset Value for L4_AP_PROT_GROUP_ROLES_k

k	L4_PER		L4_CFG	
	Type	Reset Value	Type	Reset Value
0	R	0xFFFF FFFF(1)	R	0xFFFF FFFF(1)
1	R	0xFFFF FFFF(1)	R	0xFFFF FFFF(1)
2	R	0xFFFF FFFF(1)	R	0x0000 0000(1)
3	RW	0xFFFF FFFF	R	0xFFFF FFFF(1)
4	RW	0xFFFF FFFF	R	0xFFFF FFFF(1)
5	RW	0xFFFF FFFF	RW	0xFFFF FFFF
6	RW	0xFFFF FFFF	RW	0xFFFF FFFF
7	RW	0xFFFF FFFF	RW	0xFFFF FFFF

(1) Value exported from SCM and valid for GP device only (see *System Control Module*). The values of the other protection registers can be modified during run time.

Table 13-415. L4_AP_PROT_GROUP_ROLES_k_H

Address Offset	0x204 + (0x08*k)	**Index**	k = 0 to 7 for PER_AP k = 0 to 7 for CFG_AP
Physical address	0x4800 0284 + (0x08*k) 0x4A00 0284 + (0x08*k)		
Description	Define ConnID bit vectors for a protection group.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																															

Bits	Field Name	Description	Type	Reset
31:0	Reserved	Read returns 0's	R	0x0000 0000

Table 13-416. Register Call Summary for Register L4_AP_PROT_GROUP_ROLES_k_H

L4 Interconnects

- L4 Address Protection (L4 AP) Register Summary: [0]

Table 13-417. L4_AP_REGION_l_L

Address Offset	0x300 + (0x08*l)	**Index**	l = 0 to 96 for PER_AP l = 0 to 113 for CFG_AP
Physical address	0x4800 0300 + (0x08*l) 0x4A00 0300 + (0x08*l)		
Description	Define the base address of the region in respect to the segment it belongs to.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								BASE																							

Bits	Field Name	Description	Type	Reset
31:24	Reserved	Read returns 0.	R	0x00
23:0	BASE	Sets the base address of the region relative to its segment base.	R	See Table 13-421 to Table 13-422

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Table 13-418. Register Call Summary for Register L4_AP_REGION_I_L

L4 Interconnects

- L4 Firewall Address and Protection Register Settings: [0]
- Operational Modes Configuration: [1]
- L4 Address Protection (L4 AP) Register Summary: [2]

Table 13-419. L4_AP_REGION_I_H

Address Offset	0x304 + (0x08*I)	**Index**	I = 0 to 99 for CORE_AP
Physical address	0x4800 0304 + (0x08*I) 0x4A00 0304 + (0x08*I)		
Description	Define the size, protection group and segment ID of the region		
Type	RW		

31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12 11 10 9 8	7 6	5 4 3 2 1	0
Reserved	SEGMENT_ID	Reserved	PROT_GROUP_ID	BYTE_DATA_WIDTH_EXP	Reserved	SIZE	ENABLE

Bits	Field Name	Description	Type	Reset
31:28	Reserved	Read returns 0	R	0x0
27:24	SEGMENT_ID	The segment associated to the region.	R	See Table 13-421 and Table 13-422.
23	Reserved	Read returns 0.	R	0
22:20	PROT_GROUP_ID	The protection group associated to the region.	RW	See Table 13-421 and Table 13-422.
19:17	BYTE_DATA_WIDTH_EXP	The target data byte width is $2^{(BYTE_DATA_WIDTH_EXP)}$ bytes.	R	See Table 13-421 and Table 13-422.
16:6	Reserved	Read returns 0.	R	0x0
5:1	SIZE	Define the size of the region in bytes. 2^{SIZE} equals the region.	R	See Table 13-421 and Table 13-422.
0	ENABLE	0x0: Disable the region, no access allows 0x1: Enable the region, with access as define in registers	R	0x1

Table 13-420. Register Call Summary for Register L4_AP_REGION_I_H

L4 Interconnects

- Protection Group: [0]
- L4 Firewall Address and Protection Register Settings: [1]
- L4 Address Protection (L4 AP) Register Summary: [2]

Table 13-421. L4_AP_REGION_I Reset Value for L4 PER

Region	MADDRSPACE	SEGMENT_ID	PROT_GROUP_ID	BYTE_DATA_WIDTH_EXP	SIZE	BASE
0	0x0	0x0	0x0	0x2	0x0B	0x000000
1	0x1	0x0	0x7	0x2	0x0B	0x000800
2	0x5	0x0	0x7	0x2	0x0C	0x001000
3	0x0	0x0	0x7	0x2	0x0C	0x020000

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Table 13-421. L4_AP_REGION_l Reset Value for L4 PER (continued)

Region	MADDRSPACE	SEGMENT_ID	PROT_GROUP_ID	BYTE_DATA_WIDTH_EXP	SIZE	BASE
4	0x0	0x0	0x7	0x2	0x0C	0x021000
5	0x0	0x0	0x7	0x2	0x0C	0x032000
6	0x0	0x0	0x7	0x2	0x0C	0x033000
7	0x0	0x0	0x7	0x2	0x0C	0x034000
8	0x0	0x0	0x7	0x2	0x0C	0x035000
9	0x0	0x0	0x7	0x2	0x0C	0x036000
10	0x0	0x0	0x7	0x2	0x0C	0x037000
11	0x0	0x0	0x7	0x2	0x0C	0x03E000
12	0x0	0x0	0x7	0x2	0x0C	0x03F000
13	0x0	0x0	0x2	0x2	0x10	0x040000
14	0x0	0x0	0x7	0x2	0x0C	0x050000
15	0x0	0x0	0x7	0x2	0x0C	0x055000
16	0x0	0x0	0x7	0x2	0x0C	0x056000
17	0x0	0x0	0x7	0x2	0x0C	0x057000
18	0x0	0x0	0x7	0x2	0x0C	0x058000
19	0x0	0x0	0x7	0x2	0x0C	0x059000
20	0x0	0x0	0x7	0x2	0x0C	0x05A000
21	0x0	0x0	0x7	0x2	0x0C	0x05B000
22	0x0	0x0	0x7	0x2	0x0C	0x05C000
23	0x0	0x0	0x7	0x2	0x0C	0x05D000
24	0x0	0x0	0x7	0x2	0x0C	0x05E000
25	0x0	0x0	0x7	0x1	0x0C	0x060000
26	0x0	0x0	0x7	0x2	0x0C	0x06A000
27	0x0	0x0	0x7	0x2	0x0C	0x06B000
28	0x0	0x0	0x7	0x2	0x0C	0x06C000
29	0x0	0x0	0x7	0x2	0x0C	0x06D000
30	0x1	0x0	0x7	0x2	0x0C	0x06E000
31	0x0	0x0	0x7	0x2	0x0C	0x06F000
32	0x0	0x0	0x7	0x1	0x0C	0x070000
33	0x0	0x0	0x7	0x1	0x0C	0x071000
34	0x0	0x0	0x7	0x1	0x0C	0x072000
35	0x0	0x0	0x7	0x1	0x0C	0x073000
36	0x0	0x0	0x7	0x1	0x0C	0x061000
37	0x0	0x0	0x7	0x2	0x0C	0x074000
38	0x0	0x0	0x7	0x2	0x0C	0x075000
39	0x0	0x0	0x7	0x2	0x0C	0x076000
40	0x0	0x0	0x7	0x2	0x0C	0x077000
41	0x0	0x0	0x7	0x2	0x0C	0x078000
42	0x0	0x0	0x7	0x2	0x0C	0x079000
43	0x0	0x0	0x7	0x2	0x0C	0x086000
44	0x0	0x0	0x7	0x2	0x0C	0x087000
45	0x0	0x0	0x7	0x2	0x0C	0x088000
46	0x0	0x0	0x7	0x2	0x0C	0x089000
47	0x0	0x0	0x7	0x2	0x0C	0x096000
48	0x0	0x0	0x7	0x2	0x0C	0x097000
49	0x0	0x0	0x7	0x2	0x0C	0x098000
50	0x0	0x0	0x7	0x2	0x0C	0x099000

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Table 13-421. L4_AP_REGION_l Reset Value for L4 PER (continued)

Region	MADDRSPACE	SEGMENT_ID	PROT_GROUP_ID	BYTE_DATA_WIDTH_EXP	SIZE	BASE
51	0x0	0x0	0x7	0x2	0x0C	0x09A000
52	0x0	0x0	0x7	0x2	0x0C	0x09B000
53	0x0	0x0	0x7	0x2	0x0C	0x09C000
54	0x0	0x0	0x7	0x2	0x0C	0x09D000
55	0x0	0x0	0x7	0x2	0x0C	0x09E000
56	0x0	0x0	0x7	0x2	0x0C	0x09F000
57	0x0	0x0	0x1	0x2	0x0C	0x0A0000
58	0x0	0x0	0x7	0x2	0x0C	0x0A1000
59	0x0	0x0	0x1	0x2	0x0C	0x0A2000
60	0x0	0x0	0x7	0x2	0x0C	0x0A3000
61	0x0	0x0	0x1	0x2	0x0D	0x0A8000
62	0x0	0x0	0x7	0x2	0x0C	0x0AA000
63	0x0	0x0	0x7	0x2	0x0C	0x0AD000
64	0x0	0x0	0x7	0x2	0x0C	0x0AE000
65	0x0	0x0	0x7	0x2	0x0C	0x0B2000
66	0x0	0x0	0x7	0x2	0x0C	0x0B3000
67	0x0	0x0	0x7	0x2	0x0C	0x0B4000
68	0x0	0x0	0x7	0x2	0x0C	0x0B5000
69	0x0	0x0	0x7	0x2	0x0C	0x0B8000
70	0x0	0x0	0x7	0x2	0x0C	0x0B9000
71	0x0	0x0	0x7	0x2	0x0C	0x0BA000
72	0x0	0x0	0x7	0x2	0x0C	0x0BB000
73	0x0	0x0	0x7	0x2	0x0C	0x151000
74	0x0	0x0	0x7	0x2	0x0C	0x0D2000
75	0x0	0x0	0x7	0x2	0x0C	0x0D5000
76	0x0	0x0	0x7	0x2	0x0C	0x0D6000
77	0x0	0x1	0x7	0x2	0x0C	0x150000
78	0x0	0x1	0x7	0x2	0x0C	0x151000
79	0x0	0x0	0x7	0x1	0x0C	0x0A2000
80	0x0	0x0	0x7	0x1	0x0C	0x0A3000
81	0x2	0x0	0x7	0x2	0x0A	0x001400
82	0x3	0x0	0x7	0x2	0x0A	0x001800
83	0x4	0x0	0x7	0x2	0x0A	0x001C00
84	0x1	0x0	0x1	0x2	0x0C	0x0A5000

Table 13-422. L4_AP_REGION_l Reset Value for L4 CFG

Region	MADDRSPACE	SEGMENT_ID	PROT_GROUP_ID	BYTE_DATA_WIDTH_EXP	SIZE	BASE
0	0x0	0x0	0x0	0x2	0x0B	0x00000
1	0x1	0x0	0x7	0x2	0x0B	0x00800
2	0x5	0x0	0x7	0x2	0x0C	0x01000
3	0x0	0x0	0x7	0x2	0x0C	0x02000
4	0x0	0x0	0x7	0x2	0x0C	0x03000
5	0x0	0x0	0x7	0x2	0x0C	0x04000
6	0x0	0x0	0x7	0x2	0x0C	0x05000
7	0x0	0x0	0x7	0x2	0x0C	0x56000

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Table 13-422. L4_AP_REGION_l Reset Value for L4 CFG (continued)

Region	MADDRSPACE	SEGMENT_ID	PROT_GROUP_ID	BYTE_DATA_WIDTH_EXP	SIZE	BASE
8	0x0	0x0	0x7	0x2	0x0C	0x57000
9	0x0	0x0	0x7	0x2	0x0C	0x5C000
10	0x0	0x0	0x7	0x2	0x0E	0x58000
11	0x0	0x0	0x7	0x2	0x0C	0x62000
12	0x0	0x0	0x7	0x2	0x0C	0x63000
13	0x0	0x1	0x7	0x2	0x0C	0x59000
14	0x0	0x1	0x7	0x2	0x0C	0x5A000
15	0x0	0x0	0x7	0x2	0x0E	0x5B000
16	0x0	0x0	0x7	0x2	0x0C	0x5C000
17	0x0	0x0	0x7	0x2	0x0E	0x5D000
18	0x0	0x0	0x7	0x2	0x0C	0x5E000
19	0x0	0x1	0x5	0x2	0x0C	0x60000
20	0x0	0x1	0x7	0x2	0x0C	0x61000
21	0x0	0x2	0x7	0x2	0x0C	0x00000
22	0x0	0x2	0x7	0x2	0x0C	0x01000
23	0x0	0x0	0x7	0x2	0x0C	0x08000
24	0x0	0x0	0x7	0x2	0x0C	0x0A000
25	0x0	0x0	0x7	0x2	0x0C	0x66000
26	0x0	0x0	0x7	0x2	0x0C	0x67000
27	0x0	0x1	0x1	0x2	0x0C	0x74000
28	0x0	0x1	0x7	0x2	0x0C	0x75000
29	0x0	0x1	0x7	0x2	0x0C	0x76000
30	0x0	0x1	0x7	0x2	0x0C	0x77000
31	0x0	0x4	0x1	0x2	0x0C	0x1E000
32	0x0	0x4	0x7	0x2	0x0C	0x1F000
33	0x0	0x4	0x1	0x2	0x0C	0x6C000
34	0x0	0x4	0x7	0x2	0x0C	0x0B000
35	0x0	0x4	0x1	0x2	0x0C	0x04000
36	0x0	0x4	0x7	0x2	0x0C	0x05000
37	0x0	0x4	0x1	0x2	0x0C	0x06000
38	0x0	0x4	0x7	0x2	0x0C	0x07000
39	0x1	0x4	0x1	0x2	0x0D	0x12000
40	0x2	0x1	0x7	0x2	0x0C	0x13000
41	0x0	0x0	0x1	0x2	0x0D	0x0C000
42	0x0	0x0	0x7	0x2	0x0C	0x0D000
43	0x0	0x0	0x1	0x2	0x0C	0x10000
44	0x0	0x0	0x7	0x2	0x0C	0x11000
45	0x0	0x1	0x1	0x2	0x0C	0x16000
46	0x0	0x1	0x7	0x2	0x0C	0x17000
47	0x0	0x1	0x1	0x2	0x0C	0x14000
48	0x0	0x1	0x7	0x2	0x0C	0x15000
49	0x0	0x4	0x1	0x2	0x0C	0x18000
50	0x0	0x4	0x7	0x2	0x0C	0x19000
51	0x0	0x4	0x1	0x2	0x0C	0x20000
52	0x0	0x4	0x7	0x2	0x0C	0x21000
53	0x0	0x4	0x1	0x2	0x0C	0x26000
54	0x0	0x4	0x7	0x2	0x0C	0x27000

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Table 13-422. L4_AP_REGION_l Reset Value for L4 CFG (continued)

Region	MADDRSPACE	SEGMENT_ID	PROT_GROUP_ID	BYTE_DATA_WIDTH_EXP	SIZE	BASE
55	0x0	0x4	0x1	0x2	0x0C	0x28000
56	0x0	0x4	0x7	0x2	0x0C	0x29000
57	0x0	0x4	0x1	0x2	0x0C	0x2A000
58	0x0	0x4	0x7	0x2	0x0C	0x1D000
59	0x0	0x4	0x1	0x2	0x0C	0x1C000
60	0x0	0x4	0x7	0x2	0x0C	0x1D000
61	0x0	0x2	0x1	0x2	0x0C	0x02000
62	0x0	0x2	0x7	0x2	0x0C	0x03000
63	0x0	0x2	0x1	0x2	0x0C	0x08000
64	0x0	0x2	0x7	0x2	0x0C	0x09000
65	0x0	0x2	0x1	0x2	0x0C	0x0A000
66	0x0	0x2	0x7	0x2	0x0C	0x0B000
67	0x0	0x6	0x1	0x2	0x11	0x00000
68	0x0	0x6	0x7	0x2	0x0C	0x40000
69	0x0	0x1	0x1	0x2	0x0C	0x36000
70	0x0	0x1	0x7	0x2	0x0C	0x37000
71	0x1	0x6	0x1	0x2	0x0E	0x20000
72	0x2	0x6	0x2	0x2	0x0D	0x24000
73	0x3	0x6	0x1	0x2	0x0C	0x26000
74	0x4	0x6	0x7	0x2	0x0C	0x27000
75	0x5	0x6	0x1	0x2	0x0C	0x27000
76	0x6	0x4	0x4	0x2	0x0C	0x29000
77	0x9	0x4	0x1	0x2	0x10	0x30000
78	0x0	0x4	0x7	0x2	0x0C	0x4D000
79	0x0	0x2	0x7	0x2	0x0C	0x4E000
80	0x0	0x0	0x7	0x2	0x0D	0x5E000
81	0x0	0x0	0x7	0x2	0x0C	0x60000
82	0x0	0x1	0x7	0x2	0x0C	0x29000
83	0x0	0x1	0x7	0x2	0x0C	0x2A000
84	0x0	0x1	0x7	0x2	0x0C	0x2B000
85	0x0	0x1	0x7	0x2	0x0C	0x2C000
86	0x0	0x0	0x7	0x2	0x0C	0x64000
87	0x0	0x0	0x7	0x2	0x0C	0x65000
88	0x0	0x2	0x7	0x2	0x0C	0x2D000
89	0x0	0x4	0x1	0x2	0x0C	0x2E000
90	0x7	0x6	0x7	0x2	0x0D	0x2A000
91	0x8	0x6	0x1	0x2	0x0E	0x2C000

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Chip-to-Chip Interface (C2C)

This chapter describes the C2C interconnection of the device.

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14.1 C2C Overview

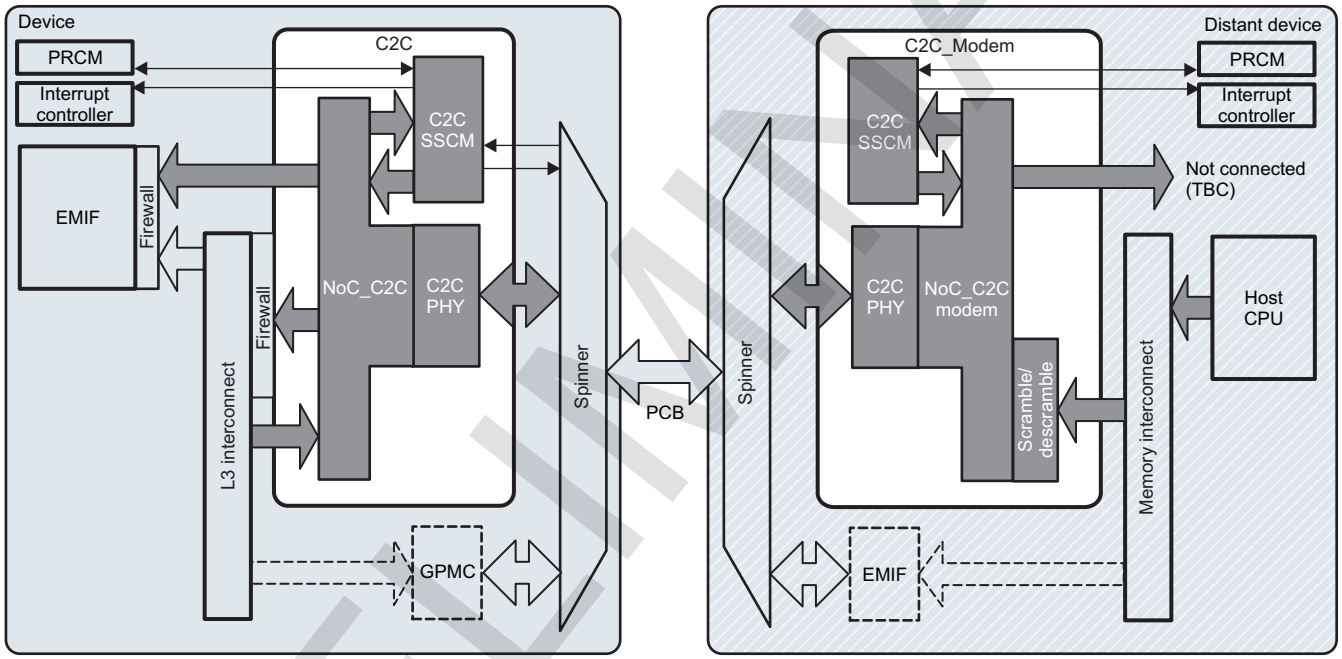
The chip-to-chip (C2C) is a serial, low-latency, peer-to-peer communication protocol that enables the extension of an internal protocol bus to one physical device over a printed circuit board (PCB). The C2C accomplishes this function by serializing local bus transactions in one device. The serialized transactions are transferred between devices through C2C ports, and the remote bus transactions are deserialized.

The C2C includes three main functional submodules:

- The Arteris® interconnect (NoC_C2C_Device), including the interface ports and the C2C port
- The physical interface (PHY_C2C_Device)
- The subsystem control module (SSCM), which supports the clock division during operating performance point (OPP) changes, wake-up and sleep sequences, and sideband signal protocol encapsulation

Figure 14-1 shows an example of the C2C implementation mirror mode.

Figure 14-1. C2C Implemenation Mirror Mode Example



The C2C includes the following general features:

- Low-pin-count interface
- Scalability up to 16 inputs/16 outputs (The device supports up to 8 inputs/16 outputs or 16 inputs/8 outputs only.)
- No mandatory 3-state signals
- All signals driven using source synchronous clocking (two dual data rate [DDR] clock signals per direction for TX and RX paths)
- Supports two PHY voltages: 1.2 and 1.8 V
- Supports symmetric (peer-to-peer) and asymmetric (host/peripheral) communication operations
- Protocol support of in-band flow control
- No extra pins needed
- All request packets, response packets, and flow control information multiplexed and sent across the same physical pins
- Supports multiple outstanding transaction reads, writes, and interrupts
- Supports mirror mode to enable self-test with identical device

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- Provides signals for system power management

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14.2 C2C Integration

This section describes module integration in the device, including information about clocks, resets, and hardware requests.

Table 14-1 through Table 14-3 summarize the integration of the module in the device.

Table 14-1. Integration Attributes

Module Instance	Attributes
	Power Domain
C2C	PD_CORE

Table 14-2. Clocks and Resets

		Clocks		
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
C2C	C2C_L3_ICLK	C2C_L3_ICLK	PRCM	L3 interconnect clock enable
C2C	C2C_L3X2_ICLK	C2C_L3X2_ICLK	PRCM	Functional clock
		Resets		
C2C	C2C_RST	CORE_RST	PRCM	Global warm

Table 14-3. Hardware Requests

		Interrupt Requests		
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
C2C	C2C_SSCM_IRQ0	MA_IRQ_27	Cortex™-A9 INTC	Interrupt request to the Cortex-A9 interrupt controller (INTC)
	C2C_SSCM_IRQ1	MA_IRQ_88	Cortex-A9 INTC	Interrupt request to the Cortex-A9 INTC
	C2C_SSCM_IRQ0	MM_IRQ_46	Cortex™-M3 INTC	Interrupt request to the Cortex-M3 INTC
	C2C_SSCM_IRQ1	MM_IRQ_47	Cortex-M3 INTC	Interrupt request to the Cortex-M3 INTC
	C2C_SSCM_IRQ0	D_IRQ_85	DSP INTC	Interrupt request to the digital signal processor (DSP) INTC
	C2C_SSCM_IRQ1	D_IRQ_86	DSP INTC	Interrupt request to the DSP INTC
		DMA Requests		
C2C	C2C_SSCM_GPO 0	S_DMA_20	sDMA	Destination is system DMA (sDMA)
	C2C_SSCM_GPO 1	S_DMA_21	sDMA	Destination is sDMA
	C2C_SSCM_GPO 2	S_DMA_67	sDMA	Destination is sDMA
	C2C_SSCM_GPO 3	S_DMA_68	sDMA	Destination is sDMA

NOTE: The gpio_wk0 device pad can be used as a C2C pre-wakeup pin. The purpose of this pin is to start the APE wakeup before C2C is ready on the distant device to trigger the c2c_wakereqin pad. The signal from the C2C pre-wakeup pin goes only to the PRCM module, not to the C2C module.

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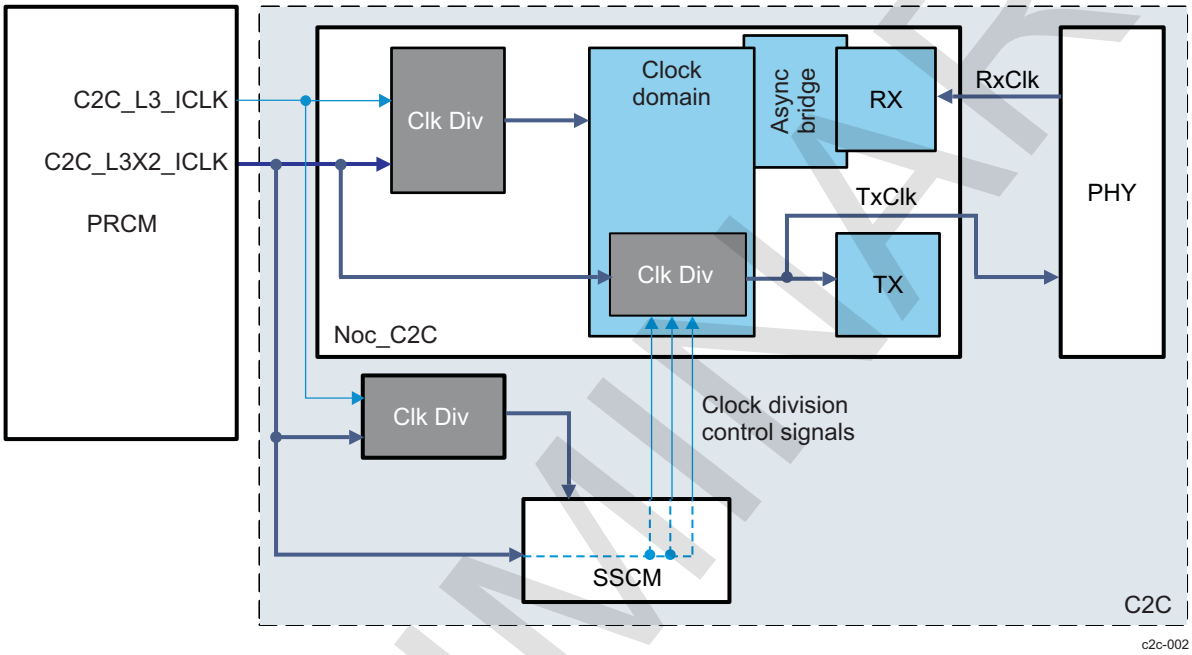
14.3 C2C Power, Reset, and Clock Management

14.3.1 PRCM Overview

The power, reset, and clock management (PRCM) module provides device-level clock, reset, and power control for other modules, as well as clock and reset signals to the C2C.

Figure 14-2 shows the C2C mode-specific overview of the PRCM.

Figure 14-2. PRCM Overview



14.3.2 Reset Manager Functional Description

14.3.2.1 Reset Sources

This section describes the reset sources triggering the reset managers in the power and reset manager (PRM).

14.3.2.1.1 Global Reset Sources

Table 14-4 lists the global reset sources of the device. The global reset source signals received by the reset manager trigger the reset of all device modules. For all hardware reset signals, the source of the reset is identified; for the software reset signals, the reset triggering bit is identified.

Table 14-4. Global Reset Sources

Type	Name	Source/Control	Description
Hardware	C2C_WARM_RST	C2C module	Global hardware warm reset

14.3.2.2 Reset Domains

A power domain can receive power-on reset (PWRON_RST) and/or normal reset (RST) signals. These signals reset nonretention logic and behave as follows:

- RST and PWRON_RST are asserted on any global or local cold reset.
- Only RST is asserted on any global or local warm reset.

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A power domain can receive two additional retention logic reset signals: power-on retention reset (PWRON_RET_RST) and/or retention reset (RET_RST). These signals behave as follows:

- RET_RST and PWRON_RET_RST are asserted on any global cold reset or wakeup from OFF state to ON-ACTIVE state.
- Only RET_RST is asserted on any global warm reset.
- These signals are not asserted on wakeup from RETENTION state.

This section presents the trigger sources and attributes for all reset domains of the device. See Section 14.3.2.1, *Reset Sources*, for an explanation of each reset trigger source for the device.

Table 14-5 identifies the associated power and rest domains for each module.

Table 14-5. C2C Power and Reset Domain Association

Module	Power Domain	Reset Domains
C2C	PD_CORE	CORE_RET_RST, CORE_RST
C2C_FW	PD_CORE	CORE_PWRON_RET_RST, CORE_RST

Table 14-6 lists the reset sources that trigger the reset domains of the device.

Table 14-6. Reset Sources For the Reset Domains

Reset Domain	Reset Source	Reset Source Type
AUDIO_RST	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	CORTEXA9_WDT_RST	Global warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_IVA_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	C2C_WARM_RST	Global warm
ALWON_CM1_RST	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	CORTEXA9_WDT_RST	Global warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_IVA_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	C2C_WARM_RST	Global warm
ALWON_CORE_RST	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	CORTEXA9_WDT_RST	Global warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_IVA_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	C2C_WARM_RST	Global warm
ALWON_IVA_RST	GLOBAL_COLD_SW_RST	Global cold

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Table 14-6. Reset Sources For the Reset Domains (continued)

Reset Domain	Reset Source	Reset Source Type
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	CORTEXA9_WDT_RST	Global warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_IVA_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	C2C_WARM_RST	Global warm
ALWON_MPU_RST	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	CORTEXA9_WDT_RST	Global warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_IVA_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	C2C_WARM_RST	Global warm
CAM_RST	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	CORTEXA9_WDT_RST	Global warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_IVA_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	C2C_WARM_RST	Global warm
CM2_RET_RST	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	CORTEXA9_WDT_RST	Global warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_IVA_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	C2C_WARM_RST	Global warm
CORE_RET_RST	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	CORTEXA9_WDT_RST	Global warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_IVA_VOLT_MGR_RST	Global warm

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Table 14-6. Reset Sources For the Reset Domains (continued)

Reset Domain	Reset Source	Reset Source Type
	VDD_MPU_VOLT_MGR_RST	Global warm
	C2C_WARM_RST	Global warm
CORE_RST	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	CORTEXA9_WDT_RST	Global warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_IVA_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	C2C_WARM_RST	Global warm
DLL_RST	DLL_FREQCHANGE_RST	Local warm
	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	CORTEXA9_WDT_RST	Global warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_IVA_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	C2C_WARM_RST	Global warm
DSS_RET_RST	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	CORTEXA9_WDT_RST	Global warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_IVA_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	C2C_WARM_RST	Global warm
DSS_RST	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	CORTEXA9_WDT_RST	Global warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_IVA_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	C2C_WARM_RST	Global warm
CORTEXM3_RET_RST	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	CORTEXA9_WDT_RST	Global warm

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Table 14-6. Reset Sources For the Reset Domains (continued)

Reset Domain	Reset Source	Reset Source Type
	RM_CORTEXM3_RSTCTRL_RST3	Local warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_IVA_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	C2C_WARM_RST	Global warm
CORTEXM3_RST1	CORTEXM3_ICECRUSHER1_RST	Local warm
	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	CORTEXA9_WDT_RST	Global warm
	RM_CORTEXM3_RSTCTRL_RST1	Local warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_IVA_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	C2C_WARM_RST	Global warm
CORTEXM3_RST2	CORTEXM3_ICECRUSHER2_RST	Local warm
	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	CORTEXA9_WDT_RST	Global warm
	RM_CORTEXM3_RSTCTRL_RST2	Local warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_IVA_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	C2C_WARM_RST	Global warm
CORTEXM3_RST3	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	CORTEXA9_WDT_RST	Global warm
	RM_CORTEXM3_RSTCTRL_RST3	Local warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_IVA_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	C2C_WARM_RST	Global warm
EMU_RST	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	CORTEXA9_WDT_RST	Global warm
	SYS_PWRON_RST	Global cold

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Table 14-6. Reset Sources For the Reset Domains (continued)

Reset Domain	Reset Source	Reset Source Type
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_IVA_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	C2C_WARM_RST	Global warm
SGX_RST	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	CORTEXA9_WDT_RST	Global warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_IVA_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	C2C_WARM_RST	Global warm
IVAHD_RST	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	CORTEXA9_WDT_RST	Global warm
	RM_IVAHD_RSTCTRL_RST3	Local warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_IVA_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	C2C_WARM_RST	Global warm
IVAHD_SEQ1_RST	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	IVAHD_ICECRUSHER1_RST	Local warm
	CORTEXA9_WDT_RST	Global warm
	RM_IVAHD_RSTCTRL_RST1	Local warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_IVA_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	C2C_WARM_RST	Global warm
IVAHD_SEQ2_RST	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	IVAHD_ICECRUSHER2_RST	Local warm
	CORTEXA9_WDT_RST	Global warm
	RM_IVAHD_RSTCTRL_RST2	Local warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm

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Table 14-6. Reset Sources For the Reset Domains (continued)

Reset Domain	Reset Source	Reset Source Type
	VDD_IVA_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	C2C_WARM_RST	Global warm
L3_INIT_RET_RST	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	CORTEXA9_WDT_RST	Global warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_IVA_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	C2C_WARM_RST	Global warm
L3_INIT_RST	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	CORTEXA9_WDT_RST	Global warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_IVA_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	C2C_WARM_RST	Global warm
L4_PER_RET_RST	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	CORTEXA9_WDT_RST	Global warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_IVA_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	C2C_WARM_RST	Global warm
L4_PER_RST	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	CORTEXA9_WDT_RST	Global warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_IVA_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	C2C_WARM_RST	Global warm
CORTEXA9_RST	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	CORTEXA9_ICECRUSHER_RST	Local warm

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Table 14-6. Reset Sources For the Reset Domains (continued)

Reset Domain	Reset Source	Reset Source Type
	CORTEXA9_WDT_RST	Global warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_IVA_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	C2C_WARM_RST	Global warm
SDMA_RET_RST	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	CORTEXA9_WDT_RST	Global warm
	SDMA_RESTORE_RST	Local warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_IVA_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	C2C_WARM_RST	Global warm
DSP_RST	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	CORTEXA9_WDT_RST	Global warm
	RM_DSP_RSTCTRL_RST1	Local warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	DSP_EMU_RESET_REQ_TR	Local warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_IVA_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	C2C_WARM_RST	Global warm
DSP_RET_RST	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	CORTEXA9_WDT_RST	Global warm
	RM_DSP_RSTCTRL_RST2	Local warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_IVA_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	C2C_WARM_RST	Global warm
DSP_SYS_RST	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	CORTEXA9_WDT_RST	Global warm
	RM_DSP_RSTCTRL_RST2	Local warm
	SYS_PWRON_RST	Global cold

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Table 14-6. Reset Sources For the Reset Domains (continued)

Reset Domain	Reset Source	Reset Source Type
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_IVA_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	C2C_WARM_RST	Global warm
WKUP_RST	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	CORTEXA9_WDT_RST	Global warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_IVA_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	C2C_WARM_RST	Global warm

14.3.3 Clock Manager Functional Description

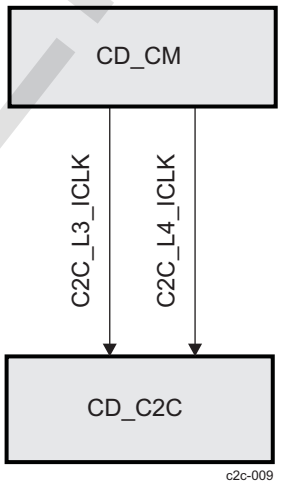
14.3.3.1 CD_C2C Clock Domain

This section identifies the modes supported by the clock domain, the associated control and status bits, and their dependencies on other device clock domains.

14.3.3.1.1 Overview

Figure 14-3 shows an overview of the clock domain.

Figure 14-3. CD_C2C Overview



14.3.3.1.2 Clock Domain Modes

Table 14-7 lists the clock domain modes supported by the clock domain.

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Table 14-7. CD_C2C Clock Domain Modes

NO_SLEEP	SW_SLEEP	SW_WKUP	HW_AUTO
Available	Not available	Available	Available

Table 14-8 lists the clock domain state transition control and status bits for the clock in this clock domain.

Table 14-8. CD_C2C Control and Status Parameters

Parameter Name	Control/Status Bit Field
C2C_L3_ICLK clock status	CM_C2C_CLKSTCTRL[8] CLKACTIVITY_L3_C2C_ICLK
C2C_L4_ICLK clock status	CM_C2C_CLKSTCTRL[9] CLKACTIVITY_L4_C2C_ICLK
Clock domain state transition control	CM_C2C_CLKSTCTRL[1:0] CLKTRCTRL

14.3.3.1.3 Clock Domain Dependency

CD_C2C has no module wake-up dependency on any other device clock domains.

14.3.3.1.3.1 Static Dependency

Table 14-9 lists the static dependency of the clock domain on other device clock domains.

Table 14-9. CD_C2C Static Dependency Association Parameters

Clock Domain Name	Default Setting	Control Bit Field	Access Type
CD_ABE	Disabled	CM_C2C_STATICDEP[3] ABE_STATDEP	Read/write
CD_IVAHD	Disabled	CM_C2C_STATICDEP[2] IVAHD_STATDEP	Read/write
CD_L3_1	Disabled	CM_C2C_STATICDEP[5] L3_1_STATDEP	Read/write
CD_L3_2	Disabled	CM_C2C_STATICDEP[6] L3_2_STATDEP	Read/write
CD_L3_INIT	Disabled	CM_C2C_STATICDEP[7] L3INIT_STATDEP	Read/write
CD_L4_CFG	Disabled	CM_C2C_STATICDEP[12] L4CFG_STATDEP	Read/write
CD_L4_PER	Disabled	CM_C2C_STATICDEP[13] L4PER_STATDEP	Read/write
CD_EMIF	Enabled	CM_C2C_STATICDEP[4] MEMIF_STATDEP	Read/write

14.3.3.1.3.2 Dynamic Dependency

Table 14-10 lists the dynamic dependency of the clock domain on other device clock domains.

Table 14-10. CD_C2C Dynamic Dependency Association Parameters

Clock Domain Name	Default Setting	Control Bit Field	Access Type
CD_L3_2	Always enabled	CM_C2C_DYNAMICDEP[6] L3_2_DYNDEP	Read only
CD_EMIF	Always enabled	CM_C2C_DYNAMICDEP[4] MEMIF_DYNDEP	Read only

14.3.3.1.4 Clock Domain Module Attributes

Table 14-11 lists the clocks received by each module of the clock domain and their role (that is, as a functional or interface clock).

Table 14-11. CD_C2C Module Clocks Association

Module	Clock	Clock Type
C2C	C2C_L3_ICLK	Interface
C2C_FW	C2C_L3_ICLK	Interface
	C2C_L4_ICLK	Interface

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Table 14-12 lists the supported wake-up request generation capability for each module of the clock domain.

Table 14-12. CD_C2C Module Wake-Up Request

Module	Wake-Up Feature
C2C	Master wake-up request
C2C_FW	None

Table 14-13 lists the supported clock management modes and associated software control bit fields for each module of the power domain.

Table 14-13. CD_C2C Module Clock Management Modes and Control

Module	Clock Mgmt. Protocol	Status Bit Field	Role
C2C	Master/slave	CM_C2C_C2C_CLKCTRL[18] STBYST	Standby status
		CM_C2C_C2C_CLKCTRL[17:16] IDLEST	Idle status
C2C_FW	Slave	CM_C2C_C2C_FW_CLKCTRL [17:16] IDLEST	Idle status

Table 14-14 lists the supported clock management modes and associated software control bit fields for each module of the power domain.

Table 14-14. CD_C2C Modules Slave Clock Management Modes and Control

Module	Disabled	Auto	Enabled	Control Bit Field	Access Type
C2C	N/A	Available	N/A	CM_C2C_C2C_CLKCTRL[1:0] MODULEMODE	Read only
C2C_FW	N/A	Available	N/A	CM_C2C_C2C_FW_CLKCTRL[1:0] MODULEMODE	Read only

14.3.3.2 CD_CORTEXA9 Clock Domain

This section identifies the modes supported by the clock domain, the associated control and status bits, and their dependencies on other device clock domains.

14.3.3.2.1 Clock Domain Dependency

CD_CORTEXA9 has no module wake-up dependency on any other device clock domain.

14.3.3.2.1.1 Static Dependency

Table 14-15 lists the static dependency of the clock domain on other device clock domains.

Table 14-15. CD_CORTEXA9 Static Dependency Association Parameters

Clock Domain Name	Default Setting	Control Bit Field	Access Type
CD_C2C	Always disabled	CM_MPU_STATICDEP[18] C2C_STATDEP	Read only

14.3.3.3 CD_L4_CFG Clock Domain

This section identifies the modes supported by the clock domain, the associated control and status bits, and their dependencies on other device clock domains.

14.3.3.3.1 Clock Domain Dependency

CD_L4_CFG has no static or module wake-up dependency on any other device clock domain.

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14.3.3.3.1.1 Dynamic Dependency

Table 14-16 lists the dynamic dependency of the clock domain on other device clock domains.

Table 14-16. CD_L4_CFG Dynamic Dependency Association Parameters

Clock Domain Name	Default Setting	Control Bit Field	Access Type
CD_C2C	Always enabled	CM_L4CFG_DYNAMICDEP[18] C2C_DYNDEP	Read only

14.3.3.4 CD_L3_2 Clock Domain

This section identifies the modes supported by the clock domain, the associated control and status bits, and their dependencies on other device clock domains.

14.3.3.4.1 Clock Domain Dependency

CD_L3_2 has no static or module wake-up dependency on any other device clock domain.

14.3.3.4.1.1 Dynamic Dependency

Table 14-17 identifies the dynamic dependency of the clock domain on other device clock domains.

Table 14-17. CD_L3_2 Dynamic Dependency Association Parameters

Clock Domain Name	Default Setting	Control Bit Field	Access Type
CD_C2C	Always enabled	CM_L3_2_DYNAMICDEP[18] C2C_DYNDEP	Read only

14.3.4 Power Management Functional Description

The section highlights the functional concepts of power-domain-level power management in the device.

The PD_CORE power domain supports the DPS with switching times of less than 5 µs.

14.3.4.1 PD_CORE Description

PD_CORE contains the following clock domains:

- CD_C2C
- CD_DMA
- CD_CORTEXM3
- CD_EMIF
- CD_L3_1
- CD_L3_2
- CD_L3_INSTR
- CD_L4_CFG

Table 14-18 lists the logic retention capability for each module of the power domain.

Table 14-18. PD_CORE C2C Power Attributes

Module	Logic Retention	DFF Context Status	RFF Context Status
C2C	Partial	RM_C2C_C2C_CONTEXT[0] LOSTCONTEXT_DFF	RM_C2C_C2C_CONTEXT[1] LOSTCONTEXT_RFF
C2C_FW	Partial	RM_C2C_C2C_FW_CONTEXT[0] LOSTCONTEXT_DFF	RM_C2C_C2C_FW_CONTEXT[1] LOSTCONTEXT_RFF

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14.3.5 PRCM Register Manual

14.3.5.1 PRM Instance Summary

Table 14-19 lists the PRCM registers and their addresses and sizes.

Table 14-19. PRM Instance Summary

Module Name	L4 Base Address	Size
INTRCONN_SOCKET_PRM	0x4A30 6000	256 bytes
CKGEN_PRM	0x4A30 6100	256 bytes
MPU_PRM	0x4A30 6300	256 bytes
DSP_PRM	0x4A30 6400	256 bytes
ABE_PRM	0x4A30 6500	256 bytes
ALWAYS_ON_PRM	0x4A30 6600	256 bytes
CORE_PRM	0x4A30 6700	2K bytes
IVAHD_PRM	0x4A30 6F00	256 bytes
CAM_PRM	0x4A30 7000	256 bytes
DSS_PRM	0x4A30 7100	256 bytes
SGX_PRM	0x4A30 7200	256 bytes
L3INIT_PRM	0x4A30 7300	256 bytes
L4PER_PRM	0x4A30 7400	512 bytes
WKUP_PRM	0x4A30 7700	256 bytes
WKUP_CM	0x4A30 7800	256 bytes
EMU_PRM	0x4A30 7900	256 bytes
EMU_CM	0x4A30 7A00	256 bytes
DEVICE_PRM	0x4A30 7B00	256 bytes
INSTR_PRM	0x4A30 7F00	256 bytes

14.3.5.2 CORE_PRM Registers

14.3.5.2.1 CORE_PRM Register Summary

Table 14-20 summarizes the CORE_PRM registers.

Table 14-20. CORE_PRM Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	CORE_PRM L4 Base Address
RM_C2C_C2C_CONTEXT	RW	32	0x0000 0524	0x4A30 6C24
RM_C2C_C2C_FW_CONTEXT	RW	32	0x0000 0534	0x4A30 6C34

14.3.5.2.2 CORE_PRM Register Description

Table 14-21 through Table 14-23 describe the individual CORE_PRM registers in detail.

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Table 14-21. RM_C2C_C2C_CONTEXT

Address Offset	0x0000 0524		
Physical Address	0x4A30 6C24	**Instance**	CORE_PRM
Description	This register contains dedicated C2C context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														LOSTCONTEXT_RFF	LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	LOSTCONTEXT_RFF	Specifies whether RFF-based context has been lost due to a previous power transition or other reset source (set upon assertion of CORE_RST signal) 0x0: Context has been maintained. 0x1: Context has been lost.	RW W1toClr	1
0	LOSTCONTEXT_DFF	Specifies whether DFF-based context has been lost due to a previous power transition or other reset source (set upon assertion of CORE_RST signal) 0x0: Context has been maintained. 0x1: Context has been lost.	RW W1toClr	1

Table 14-22. Register Call Summary for Register RM_C2C_C2C_CONTEXT

C2C Power, Reset, and Clock Management
- PD_CORE Description: [0] [1]
- CORE_PRM Registers: [2]

Table 14-23. RM_C2C_C2C_FW_CONTEXT

Address Offset	0x0000 0534		
Physical Address	0x4A30 6C34	**Instance**	CORE_PRM
Description	This register contains dedicated C2C_FW context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														LOSTCONTEXT_RFF	LOSTCONTEXT_DFF

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Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	LOSTCONTEXT_RFF	Specifies whether RFF-based context has been lost due to a previous power transition or other reset source (set upon assertion of CORE_RET_RST signal) 0x0: Context has been maintained. 0x1: Context has been lost.	RW W1toClr	1
0	LOSTCONTEXT_DFF	Specifies whether DFF-based context has been lost due to a previous power transition or other reset source (set upon assertion of CORE_RST signal) 0x0: Context has been maintained. 0x1: Context has been lost.	RW W1toClr	1

Table 14-24. Register Call Summary for Register RM_C2C_C2C_FW_CONTEXT

C2C Power, Reset, and Clock Management
- PD_CORE Description: [0] [1]
- CORE_PRM Registers: [2]

14.3.5.3 CORE_CM2 Registers

14.3.5.3.1 CORE_CM2 Register Summary

Table 14-36 summarizes the CORE_CM2 registers.

Table 14-25. CORE_CM2 Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	CORE_CM2 L4 Base Address
CM_C2C_CLKSTCTRL	RW	32	0x0000 0500	0x4A00 8C00
CM_C2C_STATICDEP	RW	32	0x0000 0504	0x4A00 8C04
CM_C2C_DYNAMICDEP	RW	32	0x0000 0508	0x4A00 8C08
CM_C2C_C2C_CLKCTRL	R	32	0x0000 0520	0x4A00 8C20
CM_C2C_C2C_FW_CLKCTRL	R	32	0x0000 0530	0x4A00 8C30
CM_L4CFG_DYNAMICDEP	RW	32	0x0000 0608	0x4A00 8D08

14.3.5.3.2 CORE_CM2 Register Description

Table 14-26 through Table 14-36 describe the individual CORE_CM2 registers in detail.

Table 14-26. CM_C2C_CLKSTCTRL

Address Offset	0x0000 0500		
Physical Address	See Table 14-25.	**Instance**	CORE_CM2
Description	This register enables the domain power state transition. It controls the hardware-supervised domain power state transition between On-Active and On-Inactive states. It also holds 1 status bit per clock input of the domain.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																					CCLKACTIVITY_ L3X2_C2C _ICLK	CLKACTIVITY_L4_C2C_ICLK	CLKACTIVITY_L3_C2C_ICLK	RESERVED							CLKTRCTRL	

Bits	Field Name	Description	Type	Reset
31:11	RESERVED		R	0x000000
10	CCLKACTIVITY_ L3X2_C2C_ICLK	This field indicates the state of theL3X2_C2C_ICLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated. Read 0x1: Corresponding clock is running or gating/ungating transition is ongoing.	R	0
9	CLKACTIVITY_L4_C2C_ICLK	This field indicates the state of the L4_C2C_ICLK clock in the domain. [warm reset insensitive] Read 0x0: On-Inactive is definitely gated. Read 0x1: On-Inactive is running or gating/ungating transition is ongoing.	R	0
8	CLKACTIVITY_L3_C2C_ICLK	This field indicates the state of the L3_C2C_ICLK clock in the domain. [warm reset insensitive] Read 0x0: On-Inactive is definitely gated. Read 0x1: On-Inactive is running or gating/ungating transition is ongoing.	R	0
7:2	RESERVED		R	0x00
1:0	CLKTRCTRL	Controls the clock state transition of the C2C clock domain. 0x0: NO_SLEEP: Sleep transition cannot be initiated. Wakeup transition may occur. Read 0x1: Reserved 0x2: SW_WKUP: Start a software forced wake-up transition on the domain. 0x3: HW_AUTO: Automatic transition is enabled. Sleep and wakeup transitions are based upon hardware conditions.	RW	0x3

Table 14-27. Register Call Summary for Register CM_C2C_CLKSTCTRL

C2C Power, Reset, and Clock Management

- CD_C2C Clock Domain: [0] [1] [2]
- CORE_CM2 Registers: [3]

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Table 14-28. CM_C2C_STATICDEP

Address Offset	0x0000 0504		
Physical Address	See Table 14-25.	**Instance**	CORE_CM2
Description	This register controls the static domain dependancies from C2C domain toward target domains. It is relevant only for a domain having system initiator(s).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																		L4PER_STATDEP	L4CFG_STATDEP	RESERVED				L3INIT_STATDEP	L3_2_STATDEP	L3_1_STATDEP	MEMIF_STATDEP	ABE_STATDEP	IVAHD_STATDEP	RESERVED	

Bits	Field Name	Description	Type	Reset
31:14	RESERVED		R	0x00000
13	L4PER_STATDEP	Static dependency toward L4_PER clock domain 0x0: Dependency is disabled. 0x1: Dependency is enabled.	RW	0
12	L4CFG_STATDEP	Static dependency toward L4_CFG clock domain 0x0: Dependency is disabled. 0x1: Dependency is enabled.	RW	0
11:8	RESERVED		R	0x0
7	L3INIT_STATDEP	Static dependency toward L3_INIT clock domain 0x0: Dependency is disabled. 0x1: Dependency is enabled.	RW	0
6	L3_2_STATDEP	Static dependency toward L3_2 clock domain 0x0: Dependency is disabled. 0x1: Dependency is enabled.	RW	0
5	L3_1_STATDEP	Static dependency toward L3_1 clock domain 0x0: Dependency is disabled. 0x1: Dependency is enabled.	RW	0
4	MEMIF_STATDEP	Static dependency toward MEMIF clock domain 0x0: Dependency is disabled. 0x1: Dependency is enabled.	RW	1
3	ABE_STATDEP	Static dependency toward ABE clock domain 0x0: Dependency is disabled. 0x1: Dependency is enabled.	RW	0
2	IVAHD_STATDEP	Static dependency toward IVAHD clock domain 0x0: Dependency is disabled. 0x1: Dependency is enabled.	RW	0
1:0	RESERVED		R	0x0

Table 14-29. Register Call Summary for Register CM_C2C_STATICDEP

C2C Power, Reset, and Clock Management

- CD_C2C Clock Domain: [0] [1] [2] [3] [4] [5] [6] [7]
- CORE_CM2 Registers: [8]

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Table 14-30. CM_C2C_DYNAMICDEP

Address Offset	0x0000 0508		
Physical Address	See Table 14-25.	**Instance**	CORE_CM2
Description	This register controls the dynamic domain dependancies from C2C domain toward target domains. It is relevant only for domain having INTRCONN master port(s).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				WINDOWSIZE				RESERVED																	L3_2_DYNDEP	RESERVED	MEMIF_DYNDEP	RESERVED			

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:24	WINDOWSIZE	Size of sliding window used to monitor INTRCONN interface activity for determination of autosleep feature. Time unit defined by CM_DYN_DEP_PRESCAL register.	RW	0x4
23:7	RESERVED		R	0x00000
6	L3_2_DYNDEP	Dynamic dependency toward L3_2 clock domain Read 0x1: Dependency is enabled.	R returns 1s	1
5	RESERVED		R	0
4	MEMIF_DYNDEP	Dynamic dependency toward MEMIF clock domain Read 0x1: Dependency is enabled.	R returns 1s	1
3:0	RESERVED		R	0x0

Table 14-31. Register Call Summary for Register CM_C2C_DYNAMICDEP

C2C Power, Reset, and Clock Management

- CD_C2C Clock Domain: [0] [1]
- CORE_CM2 Registers: [2]

Table 14-32. CM_C2C_C2C_CLKCTRL

Address Offset	0x0000 0520		
Physical Address	See Table 14-25.	**Instance**	CORE_CM2
Description	This register manages the C2C clocks.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													STBYST	IDLEST		RESERVED														MODULEMODE	

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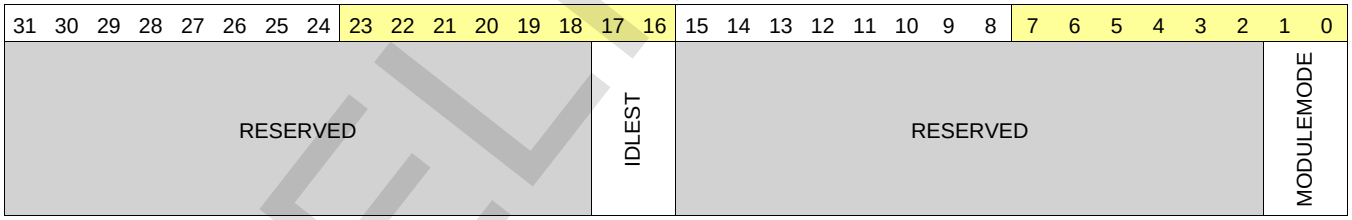
Bits	Field Name	Description	Type	Reset
31:19	RESERVED		R	0x0000
18	STBYST	C2C module standby status [warm reset insensitive] Read 0x0: Module is functional (not in standby). Read 0x1: Module is in standby.	R	1
17:16	IDLEST	C2C interface idle status [warm reset insensitive] Read 0x0: C2C interface is in functional state. Read 0x1: C2C interface is in a transitory state. Read 0x2: C2C interface is in Idle state.	R	0x2
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Controls the way mandatory clocks are managed. Read 0x1: Module is managed automatically by hardware according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CLKTRCTRL = 3, any INTRCONN access to module is always granted. Module clocks may be gated according to the clock domain state.	R Rreturns	0x1

Table 14-33. Register Call Summary for Register CM_C2C_C2C_CLKCTRL

C2C Power, Reset, and Clock Management
- CD_C2C Clock Domain: [0] [1] [2]
- CORE_CM2 Registers: [3]

Table 14-34. CM_C2C_C2C_FW_CLKCTRL

Address Offset	0x0000 0530		
Physical Address	See Table 14-25.	**Instance**	CORE_CM2
Description	This register manages the C2C_FW clocks.		
Type	R		



Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN. Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion. Read 0x2: Module is in Idle mode (only INTRCONN part). It is functional if using separate functional clock. Read 0x3: Module is disabled and cannot be accessed.	R	0x3
15:2	RESERVED		R	0x0000

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Bits	Field Name	Description	Type	Reset
1:0	MODULEMODE	Controls the way mandatory clocks are managed Read 0x1: Module is managed automatically by hardware according to clock domain transition. A clock domain sleep transition puts module into idle. A wakeup domain transition puts it back into function. If CLKTRCTRL = 3, any INTRCONN access to module is always granted. Module clocks may be gated according to the clock domain state.	R Rreturns	0x1

Table 14-35. Register Call Summary for Register CM_C2C_C2C_FW_CLKCTRL

C2C Power, Reset, and Clock Management

- CD_C2C Clock Domain: [0] [1]
- CORE_CM2 Registers: [2]

Table 14-36. CM_L4CFG_DYNAMICDEP

Address Offset	0x0000 0608		
Physical Address	See Table 14-25.	**Instance**	CORE_CM2
Description	This register controls the dynamic domain dependancies from L4_CFG domain toward target domains. It is relevant only for domain having INTRCONN master port(s).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				WINDOWSIZE				RESERVED					C2C_DYNDEP	RESERVED	ALWONCORE_DYNDEP	L4WKUP_DYNDEP	RESERVED			SDMA_DYNDEP	RESERVED	CAM_DYNDEP	DSS_DYNDEP	L3_INIT_DYNDEP	L3_2_DYNDEP	L3_1_DYNDEP	MEMIF_DYNDEP	RESERVED		DSP_DYNDEP	RESERVED

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:24	WINDOWSIZE	Size of sliding window used to monitor INTRCONN interface activity for determination of autosleep feature. Time unit defined by CM_DYN_DEP_PRESCAL register.	RW	0x4
23:19	RESERVED		R	0x00
18	C2C_DYNDEP	Dynamic dependency toward C2C clock domain Read 0x1: Dependency is enabled.	R Rreturns 1s	1
17	RESERVED		R	1
16	ALWONCORE_DYNDEP	Dynamic dependency toward ALWONCORE clock domain Read 0x1: Dependency is enabled.	R Rreturns 1s	1
15	L4WKUP_DYNDEP	Dynamic dependency toward L4_WKUP clock domain Read 0x1: Dependency is enabled.	R Rreturns 1s	1
14:12	RESERVED		R	0x0
11	SDMA_DYNDEP	Dynamic dependency toward sDMA clock domain Read 0x1: Dependency is enabled.	R Rreturns 1s	1
10	RESERVED		R	0
9	CAM_DYNDEP	Dynamic dependency toward ISS clock domain Read 0x0: Dependency is disabled.	R	0

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Bits	Field Name	Description	Type	Reset
8	DSS_DYNDEP	Dynamic dependency toward DSS clock domain Read 0x1: Dependency is enabled.	R Rreturns 1s	1
7	L3_INIT_DYNDEP	Dynamic dependency toward L3_INIT clock domain Read 0x1: Dependency is enabled.	R Rreturns 1s	1
6	L3_2_DYNDEP	Dynamic dependency toward L3_2 clock domain Read 0x1: Dependency is enabled.	R Rreturns 1s	1
5	L3_1_DYNDEP	Dynamic dependency toward L3_1 clock domain Read 0x1: Dependency is enabled.	R Rreturns 1s	1
4	MEMIF_DYNDEP	Dynamic dependency toward MEMIF clock domain Read 0x1: Dependency is enabled.	R Rreturns 1s	1
3:2	RESERVED		R	0x0
1	DSP_DYNDEP	Dynamic dependency toward DSP clock domain Read 0x1: Dependency is enabled.	R Rreturns 1s	1
0	RESERVED		R	0

Table 14-37. Register Call Summary for Register CM_L4CFG_DYNAMICDEP

C2C Power, Reset, and Clock Management
- CD_L4_CFG Clock Domain: [0]
- CORE_CM2 Registers: [1]

14.3.5.4 SCRM Instance Summary

Table 14-38 lists the register instances for the system clock and reset manager (SCRM).

Table 14-38. SCRM Instance Summary

Module Name	L4 Base Address	Size
SCRM	0x4A30 A000	256 bytes

14.3.5.5 SCRM Registers

14.3.5.5.1 SCRM Register Summary

Table 14-39 summarizes the SCRM registers.

Table 14-39. SCRM Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	SCRM L4 Base Address
C2CCLKM	RW	32	0x0000 011C	0x4A30 A11C
C2CCLKREQ	RW	32	0x0000 0234	0x4A30 A234
C2CRSTCTRL	RW	32	0x0000 041C	0x4A30 A41C
EXTWARMRSTCTRL	RW	32	0x0000 0500	0x4A30 A500
APEWARMRSTCTRL	RW	32	0x0000 0504	0x4A30 A504
RESERVED	RW	32	0x0000 0508	0x4A30 A508
C2CWARMRSTCTRL	RW	32	0x0000 050C	0x4A30 A50C
C2CWARMRSTST_REG	RW	32	0x0000 051C	0x4A30 A51C

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14.3.5.5.2 SCRM Register Description

Table 14-40 through Table 14-52 describe the individual SCRM registers in detail.

Table 14-40. C2CCLKM

Address Offset	0x0000 011C		
Physical Address	0x4A30 A11C	**Instance**	SCRM
Description	This register controls the clocks of the external C2C interface.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														SYSCLK	CLK_32KHZ

Bits	Field Name	Description	Type	Reset
31:2	RESERVED	Reads return 0.	R	0x0000 0000
1	SYSCLK	This bit allows to enable and disable the system clock version of the external C2C interface. 0x0: The system clock version for the external C2C interface is disabled. 0x1: The system clock version for the external C2C interface is enabled.	RW	0
0	CLK_32KHZ	This bit allows to enable and disable the 32-kHz clock version of the external C2C interface. 0x0: The 32-kHz clock version for the external C2C interface is disabled. 0x1: The 32-kHz clock version for the external C2C interface is enabled.	RW	0

Table 14-41. Register Call Summary for Register C2CCLKM

C2C Power, Reset, and Clock Management
- SCRM Registers: [0]

Table 14-42. C2CCLKREQ

Address Offset	0x0000 0234		
Physical Address	0x4A30 A234	**Instance**	SCRM
Description	This register holds qualifiers for the external C2C interface clock request.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														ACCURACY	POLARITY

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Bits	Field Name	Description	Type	Reset
31:2	RESERVED	Reads return 0.	R	0x0000 0000
1	ACCURACY	This bit qualifies the external C2C interface clock request as an accurate clock request. 0x0: An active external C2C interface clock request does not generate an accurate clock request. 0x1: An active external C2C interface clock request generates an accurate clock request.	RW	0
0	POLARITY	This bit defines the active level of the external C2C interface clock request. 0x0: The external C2C interface clock request is active low. 0x1: The external C2C interface clock request is active high.	RW	1

Table 14-43. Register Call Summary for Register C2CCLKREQ

C2C Power, Reset, and Clock Management
- SCRM Registers: [0]

Table 14-44. C2CRSTCTRL

Address Offset	0x0000 041C		
Physical Address	0x4A30 A41C	**Instance**	SCRM
Description	This register controls the release of the external C2C interface reset lines.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														WARMRST	COLDRST

Bits	Field Name	Description	Type	Reset
31:2	RESERVED	Reads return 0.	R	0x0000 0000
1	WARMRST	This bit allows to release the warm reset line of the external C2C interface. [warm reset sensitive] 0x0: Clearing this bit releases the warm reset line of the external C2C interface. 0x1: Writing this bit asserts the warm reset line of the external C2C interface.	RW	1
0	COLDRST	This bit allows to release the cold reset line of the external C2C interface. 0x0: Clearing this bit releases the cold reset line of the external C2C interface. 0x1: Writing this bit asserts the cold reset line of the external C2C interface.	RW	1

Table 14-45. Register Call Summary for Register C2CRSTCTRL

C2C Power, Reset, and Clock Management
- SCRM Registers: [0]

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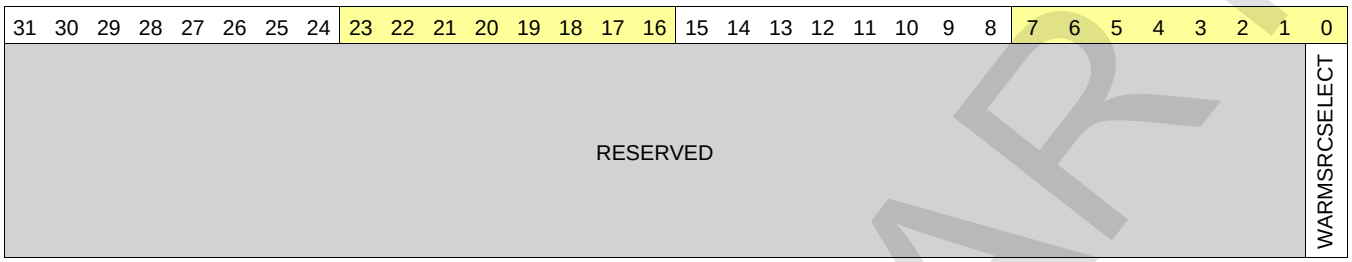
Table 14-46. EXTWARMRSTCTRL

Address Offset	0x0000 0500		
Physical Address	0x4A30 A500	**Instance**	SCRM
Description	This register allows selection of the external warm reset source as a global warm reset for the platform.		
Type	RW		



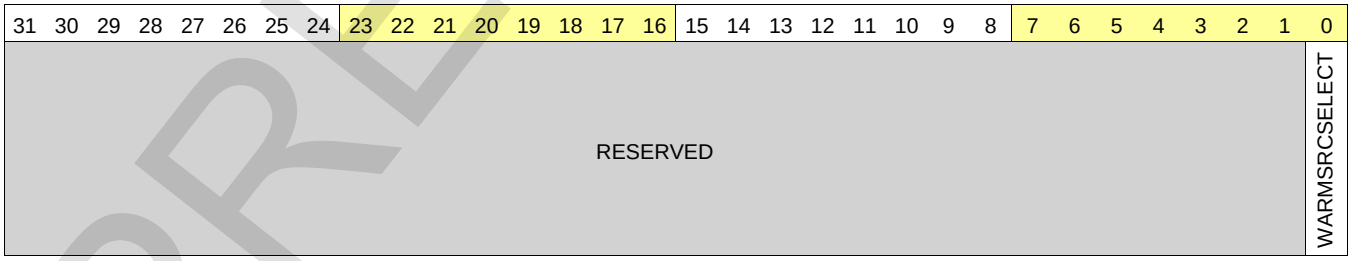
Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reads return 0.	R	0x0000 0000
0	WARMSRCSELECT	Selects the external warm reset source as a global warm reset 0x0: The external warm reset source does not reset (warm) the other functions (APE, modem, and external C2C interface). 0x1: The external warm reset source resets (warm) the other functions (APE, modem, and external C2C interface).	RW	1

Table 14-47. Register Call Summary for Register EXTWARMRSTCTRL

C2C Power, Reset, and Clock Management
- SCRM Registers: [0]

Table 14-48. APEWARMRSTCTRL

Address Offset	0x0000 0504		
Physical Address	0x4A30 A504	**Instance**	SCRM
Description	This register allows selection of the APE warm reset source as a global warm reset for the platform.		
Type	RW		



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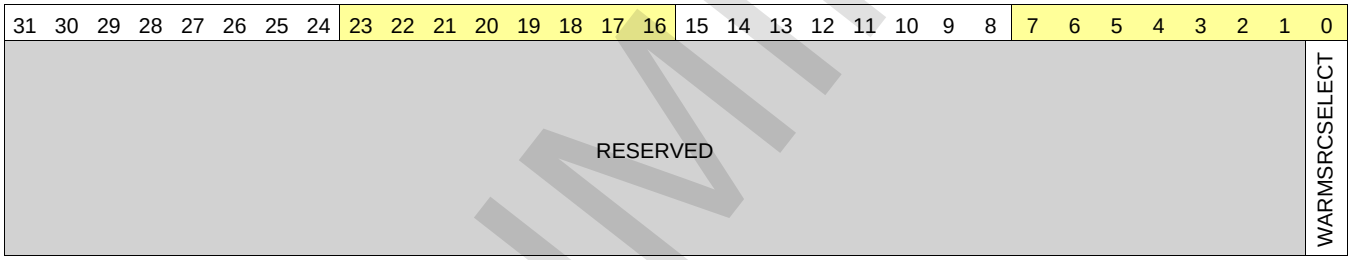
Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reads return 0.	R	0x0000 0000
0	WARMSRCSELECT	Select the APE warm reset source as a global warm reset. 0x0: The APE warm reset source does not reset (warm) the other functions (external peripherals, modem, and external C2C interface). 0x1: The APE warm reset source resets (warm) the other functions (external peripherals, modem, and external C2C interface).	RW	1

Table 14-49. Register Call Summary for Register APEWARMRSTCTRL

C2C Power, Reset, and Clock Management • SCRM Registers: [0]

Table 14-50. C2CWARMRSTCTRL

Address Offset	0x0000 050C		
Physical Address	0x4A30 A50C	**Instance**	SCRM
Description	This register allows selection of the external C2C interface warm reset source as a global warm reset for the platform.		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reads return 0.	R	0x0000 0000
0	WARMSRCSELECT	Select the external C2C interface warm reset source as a global warm reset. 0x0: The external C2C interface warm reset source does not reset (warm) the other functions (external peripherals, APE, and modem). 0x1: The external C2C interface warm reset source resets (warm) the other functions (external peripherals, APE, and modem).	RW	0

Table 14-51. Register Call Summary for Register C2CWARMRSTCTRL

C2C Power, Reset, and Clock Management • SCRM Registers: [0]

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Table 14-52. C2CWARMRSTST_REG

Address Offset	0x0000 051C		
Physical Address	0x4A30 A51C	**Instance**	SCRM
Description	This register logs the source of warm reset on the external C2C interface. Each bit is set upon release of the external C2C interface warm reset and must be cleared by software.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												C2CWARMRSTST	Reserved		

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reads return 0.	R	0x0000000
3	C2CWARMRSTST	This bit logs the C2C warm reset source. 0x0: No C2C warm reset occurred. 0x1: A C2C warm reset occurred.	RW W1toClr	0
2 : 0	Reserved	Read returns 0	R	0x0

Table 14-53. Register Call Summary for Register C2CWARMRSTST_REG

C2C Power, Reset, and Clock Management

- SCRM Registers: [0]

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14.4 C2C L3 Interconnect

NOTE: The L3 interconnect is an instantiation of the Arteris interconnect from Arteris, Inc.

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NoC is an abbreviation for network on chip.

14.4.1 C2C Interconnect Overview

Figure 14-4 shows the L3 interconnect interface.

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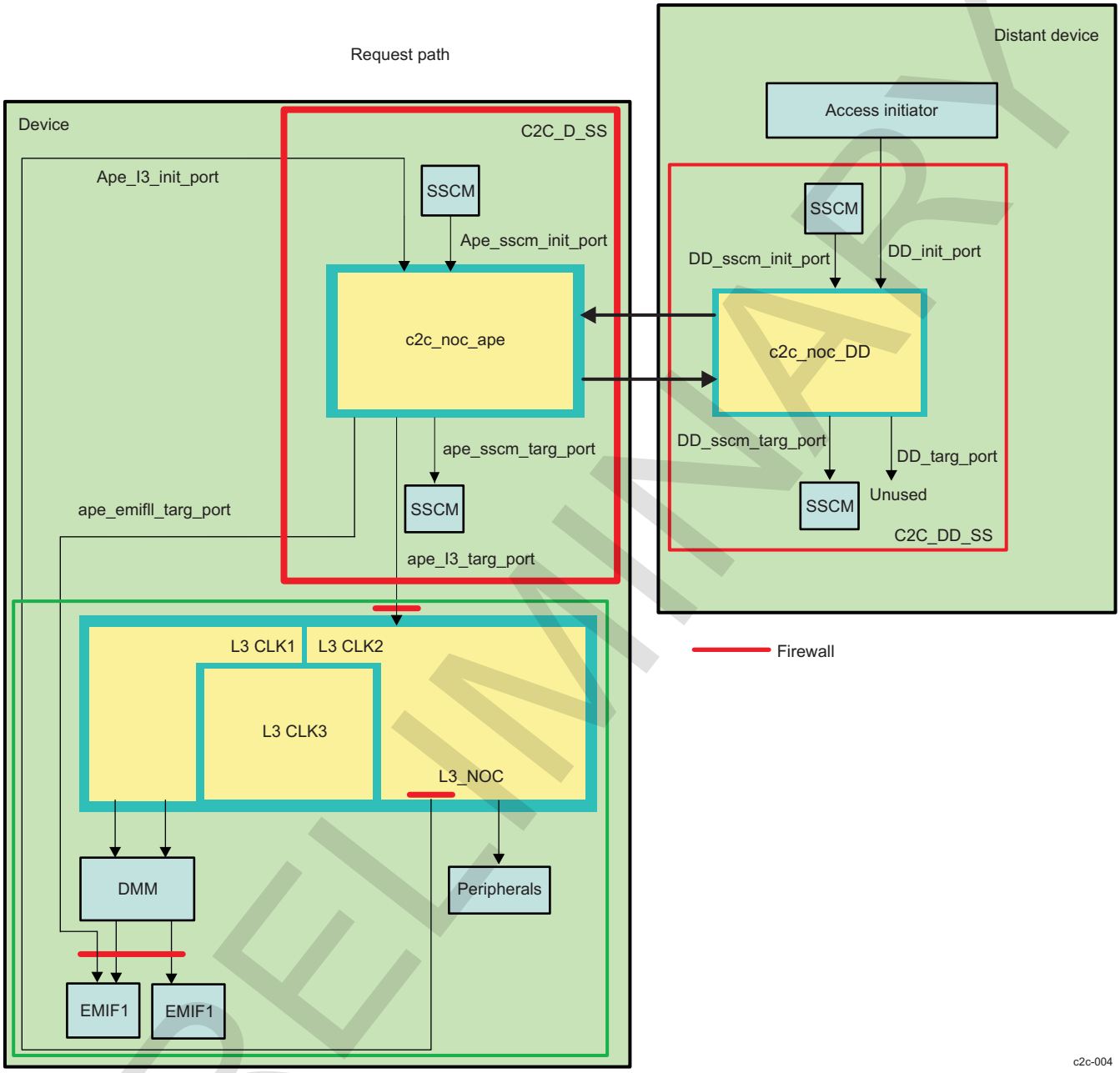
Figure 14-4. C2C L3 Interface



The C2C L3 interface includes the following main features:

- Network interface units (NIUs): Master NIUs for the initiator agents (IAs) and slave NIUs for the target agents (TAs)
- A partially depleted crossbar exchange network
- A special internal slave NIU to access L3 interconnect configuration registers
- True little-endian platform
- Transaction errors tracking and logging registers
- Provides all signaling support for the chip-level, power-management infrastructure

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14.4.2 C2C Interconnect Integration

14.4.2.1 Clocking, Reset, and Power-Management Scheme

14.4.2.1.1 Clocks

Table 14-54 lists the C2C L3 interconnect clocks. For more information, see Chapter 3, *Power, Reset, and Clock Management*.

Table 14-54. Clocks

Module	Type	Name	Source	Description
C2C L3	Interface	C2C_L3_ICLK	PRCM	Interface/functional clock for the C2C

14.4.2.1.2 Resets

Table 14-55 lists the C2C L3 interconnect resets. For more information, see Chapter 3, *Power, Reset, and Clock Management*.

Table 14-55. Resets

Module	Name	Source	Description
C2C L3	CORE_RST	PRCM	Global warm reset

14.4.2.1.3 Power Management

The L3 interconnect ports belong to the CORE power domain. As part of the system-wide power-management scheme, the L3 ports go into IDLE state after receiving a request from the PRCM module and after all commands are serviced. For more information, see Chapter 3, *Power, Reset, and Clock Management*.

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14.4.3 C2C Interconnect Functional Description

14.4.3.1 Slave NIU Configuration

All external subsystem master NIUs can initiate transactions to the L3 applicative slave NIUs listed in Table 14-56 through the C2C port link, as shown in Table 14-56.

Table 14-56. C2C Connectivity

	Slave NIUs				
Master NIUs	APE_L3_SN	APE_emifll_SN	APE_SSCM	DD_L3_SN	DD_SSCM
APE_L3_MN			0	0(1)	0(2)
APE_SSCM_MN					0
DD_SSCM_MN			0		
DD_L3_MN	0	0	0(2)		0

(1) This connection must be assessed according to system requirements on a case-by-case basis.
(2) These connections are present only for debugging purposes.

Table 14-57 lists the mapping of the C2C required information.

Table 14-57. C2C ReqInfo Mapping

	ReqInfo Name	MReqDebug	MReqType	MReqSupervisor
MNs	APE_L3	x	0	x
	APE_SSCM			
	DD_L3	x	0	x
SNs	APE_L3	x	0	x
	APE_EMIF1	x	0	x
	APE_SSCM			
	DD_SSCM			
	DD_MNs	x	0	x

14.4.3.2 Global Error Routing Scheme

Error logging is not enabled on the C2C because it is already enabled in the L3 interconnect. The C2C L3 only reports in-band errors. For more information about L3 interconnect error logging, see Section 13.2, *L3 Interconnect*.

Figure 14-5 shows the C2C global error routing scheme.

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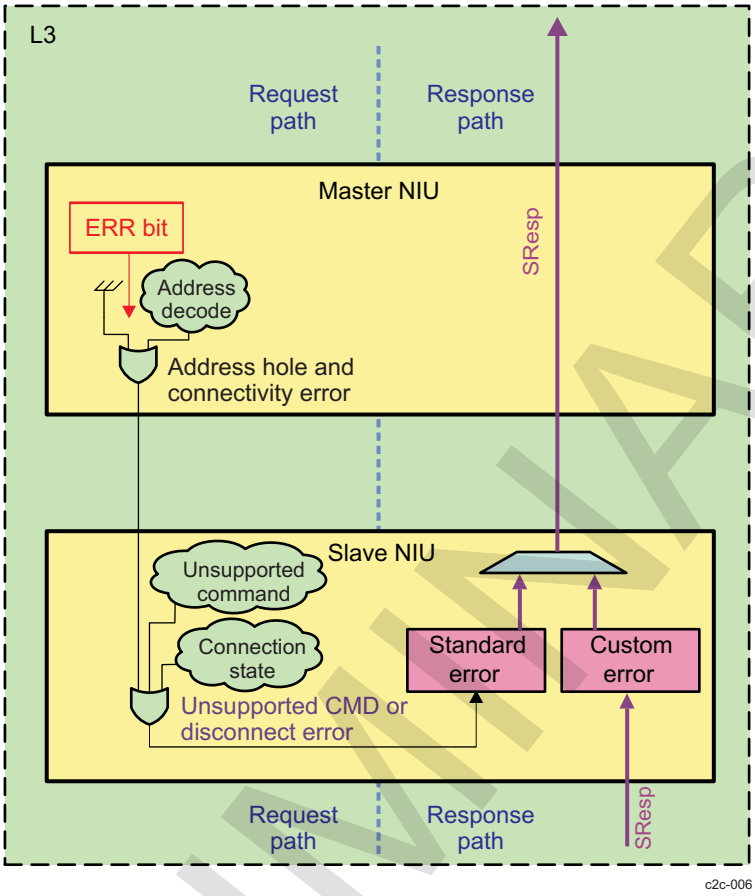
Figure 14-5. C2C Global Error Routing Scheme



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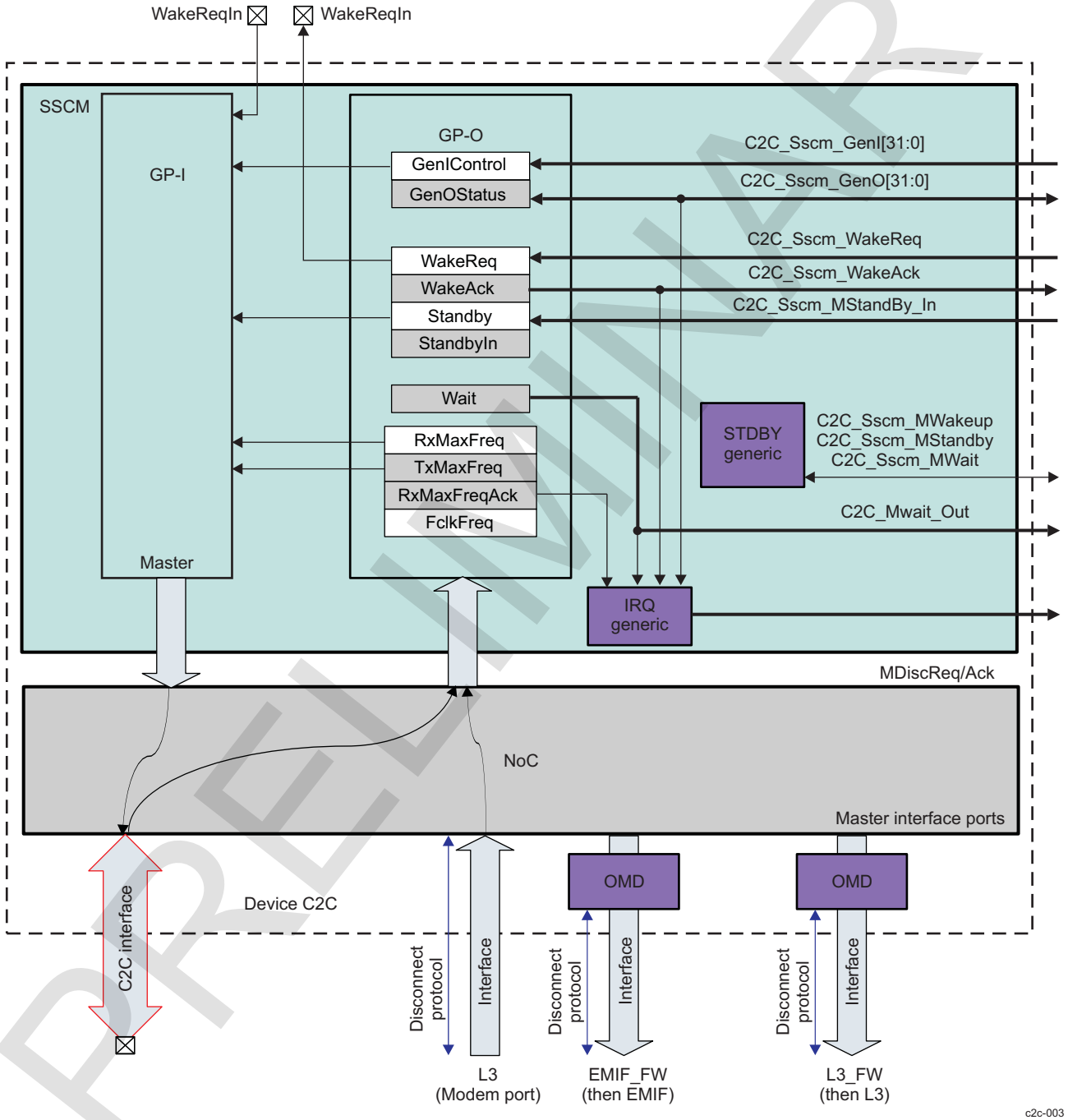
14.5 C2C SSCM

14.5.1 SSCM Overview

The SSCM supports clock division during OPP changes, the wake-up and sleep sequences, and interrupts signaling. Figure 14-7 shows the C2C SSCM block diagram.

Figure 14-6. C2C SSCM Block Diagram



The C2C SSCM supports:

- Different handshakes for local and distant OPP changes
- Sleep and wake-up sequences initiated locally or from a remote side

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- TX clock automatic division
- Transport of general-purpose signals to and from distant C2C
- GPI and GPO submodules

14.5.2 SSCM Interrupts

14.5.2.1 SSCM GPI Interrupt Mapping

Table 14-58 lists the SSCM GPI interrupt mapping.

Table 14-58. SSCM GPI Interrupt Mapping

C2C_SSCM_GPI	Source	Description
C2C_SSCM_GPI[0]	SYS.IRQ1n	External interrupt
C2C_SSCM_GPI[1]	MAIL_U3_C2C_IRQ	Device to DD mailbox interrupt
C2C_SSCM_GPI[2]	MODEM_ICR_IRQ	Distant (Modem) ICR Interrupt
C2C_SSCM_GPI[3]	UART1_IRQ	UART module 1
C2C_SSCM_GPI[4]	UART2_IRQ	UART module 2
C2C_SSCM_GPI[5]	UART3_IRQ	UART module 3
C2C_SSCM_GPI[6]	GPT6_IRQ	General-purpose timer 6
C2C_SSCM_GPI[7]	GPT7_IRQ	General-purpose timer 7
C2C_SSCM_GPI[8]	GPT8_IRQ	General-purpose timer 8
C2C_SSCM_GPI[9]	GPT9_IRQ	General-purpose timer 9
C2C_SSCM_GPI[10]	GPIO1_MPU_IRQ	GPIO module 1
C2C_SSCM_GPI[11]	GPIO2_MPU_IRQ	GPIO module 2
C2C_SSCM_GPI[12]	GPIO3_MPU_IRQ	GPIO module 3
C2C_SSCM_GPI[13]	GPIO4_MPU_IRQ	GPIO module 4
C2C_SSCM_GPI[14]	HS_USB_MC_NINT	Module HS USB OTG
C2C_SSCM_GPI[15]	HS_USB_DMA_NINT	Module HS USB OTG DMA controller interrupt
C2C_SSCM_GPI[16]	FSUSB_IRQ	FS USB-HOST controller interrupt
C2C_SSCM_GPI[17]	FSUSB_SMI_IRQ	FS USB-HOST controller SMI
C2C_SSCM_GPI[18]	L3_APP_IRQ	Application errors on L3
C2C_SSCM_GPI[19]	ONCHI_IRQ	HSUSB MP host interrupt
C2C_SSCM_GPI[20]	EHCI_IRQ	HSUSB MP host interrupt
C2C_SSCM_GPI[21]	TLL_IRQ	TLL interrupt
C2C_SSCM_GPI[22]	SYS.IRQ2n	External interrupt
C2C_SSCM_GPI[23:29]	Reserved	Reserved
C2C_SSCM_GPI[30]	Modem_shutdown_irqModem_wake_irq	PRCM Modem_shutdown_irq
C2C_SSCM_GPI[31]	Modem_wake_irq	PRCM Modem_wake_irq

14.5.3 SSCM GPO

The interrupts described in Section 14.1, *C2C Overview*, are active in GPO mode.

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14.6 Intersystem Communication Register Module

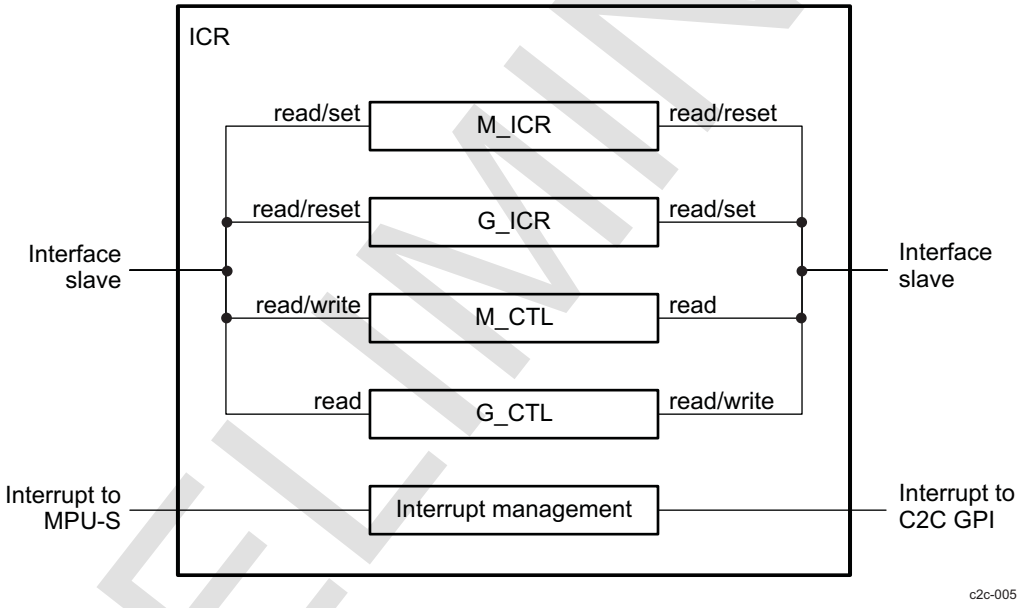
14.6.1 intersystem Communication Register Overview

The intersystem communication register (ICR) module synchronizes microprocessor unit (MPU) and modem activity, relying on flag mechanisms that are shared by both systems. Basically, the MPU sets a flag that is reset by the modem and vice versa. For a given direction, all flags are set by the source subsystem and are reset by the destination subsystem when it wants to. Each subsystem can read flags without resetting them. To avoid continuous polling on the ICRs, each subsystem can receive an interrupt when an operation that is related to it (set or reset) completes.

14.6.2 ICR Functional Description

The ICR is used when the device is connected to an external initiator device connected on the C2C port. Otherwise, the ICR is not used. The MPU and the external systems communicate with the help of two ICRs. One ICR (G_ICR) is used by the external system to inform the device MPU subsystem of an event and to send commands to the MPU-S. In the same way, the other ICR (M_ICR) is used by the device MPU subsystem to inform the external system of an event and to send commands to the MPU subsystem. The bits definition of the G_ICR and M_ICR registers are defined by software.

Figure 14-7. ICR Block Diagram



14.6.2.1 ICR Clocking Scheme

The ICR function operates from the L4-core interface clock.

14.6.2.2 Flag Management

Flags are used to notify the other subsystem of an event. Software determines the meaning of each flag. The following communication sequence from the MPU-S to the modem-S is typical:

- The MPU-S writes one or more flags in the M_ICR register.
- An interrupt is sent to the modem-S (if enabled).
- The modem-S reads the M_ICR register to check which flags are set.
- The modem-S resets one of more flags in the M_ICR register.
- An interrupt is sent to the MPU-S (if enabled).
- The MPU-S reads the M_ICR register to check which flags are reset.

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14.6.2.3 Setting and Reseting a Flag

To set a flag, the MPU-S must set the desired bit of the M_ICR register to 1. Setting a bit of M_ICR to 0 does not change its content (that is, if previous value was 1, bit value remains 1 after the write access, [modem-S does the same thing with G_ICR register]).

To reset a flag, the MPU-S must set the desired bit of the G_ICR register to 1 (that is, if previous value of the bit was 1, then it becomes 0 else it remains 0, [modem-S does the same thing with M_ICR register]).

14.6.2.4 Interrupt Management

Interrupt behavior is the same on both sides (MPU and modem).

Two kinds of events can generate an interrupt to the MPU:

- The modem sets a flag in G_ICR register.
- The modem resets a flag in M_ICR register.

Interrupt generation is controlled by the M_CTL register.

Interrupt generation mechanism to the modem is exactly the same as on the MPU side:

- The MPU sets a flag in the M_ICR register.
- The MPU resets a flag in the G_ICR register.

Interrupt generation is controlled by the G_CTL register. To acknowledge an interrupt, the MPU must clear the M_IRQ_STATUS register by setting to 1 the bits that caused the interrupt. Acknowledgment on the modem side follows the same procedure with the G_IRQ_STATUS register.

14.6.3 ICR Register Manual

14.6.3.1 ICR Instance Summary

Table 14-59. C2C Instance Summary

Module Name	Module Base Address	Size
ICR_MPU	0x4A0B 6000	4KB
ICR_MDM	0x4A0C D000	4KB

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14.6.3.2 ICR_MDM and ICR_MPU Registers

14.6.3.2.1 ICR Register Summary

Table 14-60 lists the mapping summary of the ICR registers.

Table 14-60. ICR Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	ICR_MDM Base Address	ICR_MPU Base Address
ICR_REVISION	R	32	0x0000 0000	0x4A0C D000	0x4A0B 6000
SYS_CONFIG	RW	32	0x0000 0010	0x4A0C D010	0x4A0B 6010
SYS_STATUS	R	32	0x0000 0014	0x4A0C D014	0x4A0B 6014
M_IRQ_STATUS	RW	32	0x0000 0018	0x4A0C D018	0x4A0B 6018
G_IRQ_STATUS	RW	32	0x0000 001C	0x4A0C D01C	0x4A0B 601C
M_ICR	RW	32	0x0000 0020	0x4A0C D020	0x4A0B 6020
G_ICR	RW	32	0x0000 0024	0x4A0C D024	0x4A0B 6024
M_CTL	R	32	0x0000 0028	0x4A0C D028	0x4A0B 6028
G_CTL	RW	32	0x0000 002C	0x4A0C D02C	0x4A0B 602C

14.6.3.2.2 ICR Register Description

Table 14-61 through Table 14-77 describe each ICR register.

Table 14-61. ICR_REVISION

Address Offset	0x0000 0000		
Physical Address	0x4A0C D000 0x4A0B 6000	**Instance**	ICR_MDM ICR_MPU
Description	This register contains the IP revision code.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP Revision	R	TI internal data

Table 14-62. Register Call Summary for Register ICR_REVISION

Intersystem Communication Register Module

- ICR_MDM and ICR_MPU Registers: [0]

Table 14-63. SYS_CONFIG

Address Offset	0x0000 0010		
Physical Address	0x4A0C D010 0x4A0B 6010	**Instance**	ICR_MDM ICR_MPU
Description	This register allows controlling various parameters of the OCP interface.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																											IDLEMODE		RESERVED	SOFTRESET	AUTOIDLE

Bits	Field Name	Description	Type	Reset
31:5	RESERVED	Read returns 0	R	0x0000000
4:3	IDLEMODE	Slave interface power management, req/ack control 0x0: Force-idle 0x1: No-idle 0x3: Reserved 0x2: Smart-idle	RW	0x0
2	RESERVED	Read returns 0	R	0
1	SOFTRESET	Software reset. Set this bit to 1 to trigger a module reset. The bit is automatically reset by the hardware. During reads, it always return 0. 0: Normal mode 1: The module is reset	RW	0
0	AUTOIDLE	Internal OCP clock gating 0: OCP clock is free running 1: Automatic OCP clock gating strategy is applied based on the OCP interface activity	RW	0

Table 14-64. Register Call Summary for Register SYS_CONFIG

Intersystem Communication Register Module

- ICR_MDM and ICR_MPU Registers: [0]

Table 14-65. SYS_STATUS

Address Offset	0x0000 0014		
Physical Address	0x4A0C D014 0x4A0B 6014	**Instance**	ICR_MDM ICR_MPU
Description	This register provides status information about the module, excluding the interrupt status information.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															RESETDONE

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	RESETDONE	Internal reset monitoring 0: Internal module reset ongoing 1: Reset completed Read 0x1: Reset completed Read 0x0: Internal module reset in ongoing	R	0

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Table 14-66. Register Call Summary for Register SYS_STATUS

Intersystem Communication Register Module

- ICR_MDM and ICR_MPU Registers: [0]

Table 14-67. M_IRQ_STATUS

Address Offset	0x0000 0018		
Physical Address	0x4A0C D018 0x4A0B 6018	**Instance**	ICR_MDM ICR_MPU
Description	The interrupt status register regroups all the status of the module internal events that can generate an interrupt - Write 1 to a given bit resets this bit.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														FLAG_SET	FLAG_RESET

Bits	Field Name	Description	Type	Reset
31:2	RESERVED	Reads returns 0	R	0x0000 0000
1	FLAG_SET	Flag has been set in G_ICR register. Write 0x0: Received command (Rx path) status bit unchanged Write 0x1: Received command (Rx path) status bit is reset Read 0x1: Received command (Rx path) is true ("pending") Read 0x0: Received command (Rx path) false	RW	0
0	FLAG_RESET	Flag has been reset in M_ICR register. Write 0x0: Received command (Rx path) status bit unchanged Write 0x1: Received command (Rx path) status bit is reset Read 0x1: Received command (Rx path) is true ("pending") Read 0x0: Received command (Rx path) false	RW	0

Table 14-68. Register Call Summary for Register M_IRQ_STATUS

Intersystem Communication Register Module

- Interrupt Management: [0]
- ICR_MDM and ICR_MPU Registers: [1]

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Table 14-69. G_IRQ_STATUS

Address Offset	0x0000 001C		
Physical Address	0x4A0C D01C 0x4A0B 601C	**Instance**	ICR_MDM ICR_MPU
Description	The interrupt status register regroups all the status of the module internal events that can generate an interrupt - Write 1 to a given bit resets this bit.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														FLAG_SET	FLAG_RESET

Bits	Field Name	Description	Type	Reset
31:2	RESERVED	Reads returns 0	R	0x0000 0000
1	FLAG_SET	Flag has been set in M_ICR register. Write 0x0: Received command (Rx path) status bit unchanged Write 0x1: Received command (Rx path) status bit is reset Read 0x1: Received command (Rx path) is true ("pending") Read 0x0: Received command (Rx path) false	RW W1toClr	0
0	FLAG_RESET	Flag has been reset in G_ICR register. Write 0x0: Received command (Rx path) status bit unchanged Write 0x1: Received command (Rx path) status bit is reset Read 0x1: Received command (Rx path) is true ("pending") Read 0x0: Received command (Rx path) false	RW W1toClr	0

Table 14-70. Register Call Summary for Register G_IRQ_STATUS

Intersystem Communication Register Module

- Interrupt Management: [0]
- ICR_MDM and ICR_MPU Registers: [1]

Table 14-71. M_ICR

Address Offset	0x0000 0020		
Physical Address	0x4A0C D020 0x4A0B 6020	**Instance**	ICR_MDM ICR_MPU
Description	Flags are used to notify an event to the other subsystem. The meaning of each flag is software dependent.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FLAGS																															

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Bits	Field Name	Description	Type	Reset
31:0	FLAGS	Meaning is software dependent.	RW W1toClr	0x0000 0000

Table 14-72. Register Call Summary for Register M_ICR

Intersystem Communication Register Module

- ICR Functional Description: [0] [1]
- Flag Management: [2] [3] [4] [5]
- Setting and Reseting a Flag: [6] [7] [8]
- Interrupt Management: [9] [10]
- ICR_MDM and ICR_MPU Registers: [11] [12] [13]

Table 14-73. G_ICR

Address Offset	0x0000 0024		
Physical Address	0x4A0C D024 0x4A0B 6024	**Instance**	ICR_MDM ICR_MPU
Description	Flags are used to notify an event to the other subsystem. The meaning of each flag is software dependent.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FLAGS																															

Bits	Field Name	Description	Type	Reset
31:0	FLAGS	Meaning is software dependent.	RW W1toSet	0x0000 0000

Table 14-74. Register Call Summary for Register G_ICR

Intersystem Communication Register Module

- ICR Functional Description: [0] [1]
- Setting and Reseting a Flag: [2] [3]
- Interrupt Management: [4] [5]
- ICR_MDM and ICR_MPU Registers: [6] [7] [8]

Table 14-75. M_CTL

Address Offset	0x0000 0028		
Physical Address	0x4A0C D028 0x4A0B 6028	**Instance**	ICR_MDM ICR_MPU
Description	Enables interrupts to subsystems.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														G_ICR_INTEN	M_ICR_INTEN

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Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	G_ICR_INTEN	Enable interrupt to MPU-S 0: No interrupt is generated 1: An interrupt is generated when Modem-S sets a flag to MPU-S	R	0
0	M_ICR_INTEN	Enable interrupt to MPU-S 0: No interrupt is generated 1: An interrupt is generated when Modem-S resets a flag set by MPU-S	R	0

Table 14-76. Register Call Summary for Register M_CTL

Intersystem Communication Register Module

- Interrupt Management: [0]
- ICR_MDM and ICR_MPU Registers: [1]

Table 14-77. G_CTL

Address Offset	0x0000 002C		
Physical Address	0x4A0C D02C 0x4A0B 602C	**Instance**	ICR_MDM ICR_MPU
Description	Enables interrupts to subsystems.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														M_ICR_INTEN	G_ICR_INTEN

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		RW	0x0000 0000
1	M_ICR_INTEN	Enable interrupt to Modem-S 0: No interrupt is generated 1: An interrupt is generated when MPU-S sets a flag to Modem-S	RW	0
0	G_ICR_INTEN	Enable interrupt to Modem-S 0: No interrupt is generated 1: An interrupt is generated when MPU-S resets a flag set by Modem-S	RW	0

Table 14-78. Register Call Summary for Register G_CTL

Intersystem Communication Register Module

- Interrupt Management: [0]
- ICR_MDM and ICR_MPU Registers: [1]

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14.7 C2C Register Manual

14.7.1 C2C Instance Summary

Table 14-79. C2C Instance Summary

Module Name	Base Address	Size
C2C	0x5C000000	64MB

14.7.2 C2C Registers

14.7.2.1 C2C Register Summary

Table 14-80 summarizes the C2C registers.

Table 14-80. C2C Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	C2C L3 Physical Address
C2C_REVISION	R	32	0x0000 0000	0x5C000000
C2C_SYSCONFIG	R	32	0x0000 0004	0x5C000004
C2C_SYSSTATUS	R	32	0x0000 0008	0x5C000008
C2C_PORTCONFIG	RW	32	0x0000 000C	0x5C00000C
C2C_MIRRORMODE	RW	32	0x0000 0010	0x5C000010
C2C_IRQ_RAW_STATUS_0	RW	32	0x0000 0014	0x5C000014
C2C_IRQ_RAW_STATUS_1	RW	32	0x0000 0018	0x5C000018
C2C_IRQ_ENABLE_STATUS_0	RW	32	0x0000 001C	0x5C00001C
C2C_IRQ_ENABLE_STATUS_1	RW	32	0x0000 0020	0x5C000020
C2C_IRQ_ENABLE_SET_0	RW	32	0x0000 0024	0x5C000024
C2C_IRQ_ENABLE_SET_1	RW	32	0x0000 0028	0x5C000028
C2C_IRQ_ENABLE_CLEAR_0	RW	32	0x0000 002C	0x5C00002C
C2C_IRQ_ENABLE_CLEAR_1	RW	32	0x0000 0030	0x5C000030
C2C_FCLK_FREQ	RW	32	0x0000 0040	0x5C000040
C2C_RX_MAX_FREQ	RW	32	0x0000 0044	0x5C000044
C2C_TX_MAX_FREQ	RW	32	0x0000 0048	0x5C000048
C2C_RX_MAX_FREQ_ACK	RW	32	0x0000 004C	0x5C00004C
C2C_WAKE_REQ	RW	32	0x0000 0050	0x5C000050
C2C_WAKE_ACK	RW	32	0x0000 0054	0x5C000054
C2C_STANDBY	RW	32	0x0000 0060	0x5C000060
C2C_STANDBY_IN	RW	32	0x0000 0064	0x5C000064
C2C_WAIT	RW	32	0x0000 0068	0x5C000068
C2C_GENI_CONTROL	RW	32	0x0000 0070	0x5C000070
C2C_GENI_MASK	RW	32	0x0000 0074	0x5C000074
C2C_GENO_STATUS	RW	32	0x0000 0080	0x5C000080
C2C_GENO_INTERRUPT	RW	32	0x0000 0084	0x5C000084
C2C_GENO_LEVEL	RW	32	0x0000 0088	0x5C000088

14.7.2.2 C2C Register Description

Table 14-81 through Table 14-133 describe the individual C2C registers in detail.

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Table 14-81. C2C_REVISION

Address Offset	0x0000 0000		
Physical Address	0x5C000000	**Instance**	C2C
Description	IP Revision identifier (X.Y.R) Used by software to track features, bugs, and compatibility		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP Revision	R	TI internal data

Table 14-82. Register Call Summary for Register C2C_REVISION

C2C Register Manual

- C2C Register Summary: [0]

Table 14-83. C2C_SYSCONFIG

Address Offset	0x0000 0004		
Physical Address	0x5C000004	**Instance**	C2C
Description	System configuration register (not used)		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

Bits	Field Name	Description	Type	Reset
31:0	RESERVED	Reserved	R	0x0000 0000

Table 14-84. Register Call Summary for Register C2C_SYSCONFIG

C2C Register Manual

- C2C Register Summary: [0]

Table 14-85. C2C_SYSSTATUS

Address Offset	0x0000 0008		
Physical Address	0x5C000008	**Instance**	C2C
Description	Reserved		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

Bits	Field Name	Description	Type	Reset
31:0	RESERVED	Reserved	R	0x0000 0000

Table 14-86. Register Call Summary for Register C2C_SYSSTATUS

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- C2C Register Summary: [0]

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Table 14-87. C2C_PORTCONFIG

Address Offset	0x0000 000C		
Physical Address	0x5C00000C	**Instance**	C2C
Description	This register defines the widths of the TX and RX buses on the C2C interface.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RX_WIDTH				TX_WIDTH			

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Reserved	R	0x000000
7:4	RX_WIDTH	0000: Bus width is set to 8 bits (default mode). 0001: Bus width is set to 10 bits (possible only if TX = 8). 0010: Bus width is set to 16 bits. Other values are reserved, and should not be used.	RW	0x0
3:0	TX_WIDTH	0000: Bus width is set to 8 bits. 0001: Bus width is set to 10 bits (possible only if RX = 8). 0010: Bus width is set to 16 bits (default mode). Other values are reserved, and shall not be used.	RW	0x2

Table 14-88. Register Call Summary for Register C2C_PORTCONFIG

C2C Register Manual
- C2C Register Summary: [0]

Table 14-89. C2C_MIRRORMODE

Address Offset	0x0000 0010		
Physical Address	0x5C000010	**Instance**	C2C
Description	This register sets the C2C L3 in mirror mode. See debug section.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															MIRRORMODE

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	MIRRORMODE	Mirror mode. 0x0: Functional default mode 0x1: Mirror mode for debug	RW	0

Table 14-90. Register Call Summary for Register C2C_MIRRORMODE

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- C2C Register Summary: [0]

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Table 14-91. C2C_IRQ_RAW_STATUS_0

Address Offset	0x0000 0014		
Physical Address	0x5C000014	**Instance**	C2C
Description	Interrupt status register (OCP-compliant IRQ line) for C2c_Sscm_Irq(0), regardless of enable settings		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												WAIT_IRQ	WAKE_ACK_IRQ	RX_MAX_FREQ_ACK_IRQ	TX_FREQ_IRQ

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved	R	0x0000000
3	WAIT_IRQ	Reading 1 indicates WAIT value in WAIT register has been modified by distant C2C. Writing 1 to this bit sets the bit. Writing 0 has no effect.	RW W1toSet	0x0
2	WAKE_ACK_IRQ	Reading 1 indicates WAKE_ACK value in the WAKE_ACK register has been modified by distant C2C. Writing 1 to this bit sets the bit. Writing 0 has no effect.	RW W1toSet	0x0
1	RX_MAX_FREQ_ACK_IRQ	Reading 1 indicates GPI is not turned on OR RX_MAX_FREQ_ACK value in the RX_MAX_FREQ_ACK register equal RX_MAX_FREQ value in the RX_MAX_FREQ register. Writing 1 to this bit sets the bit. Writing 0 has no effect.	RW W1toSet	0x0
0	TX_FREQ_IRQ	Reading 1 indicates that the FCLK_FREQ value in the FCLK_FREQ register has been updated AND the SSCM has finished updating the new division for the TX clock. Writing 1 to this bit sets the bit. Writing 0 has no effect.	RW W1toSet	0x0

Table 14-92. Register Call Summary for Register C2C_IRQ_RAW_STATUS_0

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- C2C Register Summary: [0]

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Table 14-93. C2C_IRQ_RAW_STATUS_1

Address Offset	0x0000 0018		
Physical Address	0x5C000018	**Instance**	C2C
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GENO_IRQ_31	GENO_IRQ_30	GENO_IRQ_29	GENO_IRQ_28	GENO_IRQ_27	GENO_IRQ_26	GENO_IRQ_25	GENO_IRQ_24	GENO_IRQ_23	GENO_IRQ_22	GENO_IRQ_21	GENO_IRQ_20	GENO_IRQ_19	GENO_IRQ_18	GENO_IRQ_17	GENO_IRQ_16	GENO_IRQ_15	GENO_IRQ_14	GENO_IRQ_13	GENO_IRQ_12	GENO_IRQ_11	GENO_IRQ_10	GENO_IRQ_9	GENO_IRQ_8	GENO_IRQ_7	GENO_IRQ_6	GENO_IRQ_5	GENO_IRQ_4	GENO_IRQ_3	GENO_IRQ_2	GENO_IRQ_1	GENO_IRQ_0

Bits	Field Name	Description	Type	Reset
31	GENO_IRQ_31	Reading 1 indicates C2c_Sscm_GENO (31) signal and GENO_31 value in GENO_STATUS register have been modified by distant C2C. Writing 1 to this bit sets the bit. Writing 0 has no effect.	RW W1toSet	0
30	GENO_IRQ_30	Reading 1 indicates C2c_Sscm_GENO (30) signal and GENO_30 value in GENO_STATUS register have been modified by distant C2C. Writing 1 to this bit sets the bit. Writing 0 has no effect.	RW W1toSet	0
29	GENO_IRQ_29	Reading 1 indicates C2c_Sscm_GENO (29) signal and GENO_29 value in GENO_STATUS register have been modified by distant C2C. Writing 1 to this bit sets the bit. Writing 0 has no effect.	RW W1toSet	0
28	GENO_IRQ_28	Reading 1 indicates C2c_Sscm_GENO (28) signal and GENO_28 value in GENO_STATUS register have been modified by distant C2C. Writing 1 to this bit sets the bit. Writing 0 has no effect.	RW W1toSet	0
27	GENO_IRQ_27	Reading 1 indicates C2c_Sscm_GENO (27) signal and GENO_27 value in GENO_STATUS register have been modified by distant C2C. Writing 1 to this bit sets the bit. Writing 0 has no effect.	RW W1toSet	0
26	GENO_IRQ_26	Reading 1 indicates C2c_Sscm_GENO (26) signal and GENO_26 value in GENO_STATUS register have been modified by distant C2C. Writing 1 to this bit sets the bit. Writing 0 has no effect.	RW W1toSet	0
25	GENO_IRQ_25	Reading 1 indicates C2c_Sscm_GENO (25) signal and GENO_25 value in GENO_STATUS register have been modified by distant C2C. Writing 1 to this bit sets the bit. Writing 0 has no effect.	RW W1toSet	0
24	GENO_IRQ_24	Reading 1 indicates C2c_Sscm_GENO (24) signal and GENO_24 value in GENO_STATUS register have been modified by distant C2C. Writing 1 to this bit sets the bit. Writing 0 has no effect.	RW W1toSet	0

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Bits	Field Name	Description	Type	Reset
23	GENO_IRQ_23	Reading 1 indicates C2c_Sscm_GENO (23) signal and GENO_23 value in GENO_STATUS register have been modified by distant C2C. Writing 1 to this bit sets the bit. Writing 0 has no effect.	RW W1toSet	0
22	GENO_IRQ_22	Reading 1 indicates C2c_Sscm_GENO (22) signal and GENO_22 value in GENO_STATUS register have been modified by distant C2C. Writing 1 to this bit sets the bit. Writing 0 has no effect.	RW W1toSet	0
21	GENO_IRQ_21	Reading 1 indicates C2c_Sscm_GENO (21) signal and GENO_21 value in GENO_STATUS register have been modified by distant C2C. Writing 1 to this bit sets the bit. Writing 0 has no effect.	RW W1toSet	0
20	GENO_IRQ_20	Reading 1 indicates C2c_Sscm_GENO (20) signal and GENO_20 value in GENO_STATUS register have been modified by distant C2C. Writing 1 to this bit sets the bit. Writing 0 has no effect.	RW W1toSet	0
19	GENO_IRQ_19	Reading 1 indicates C2c_Sscm_GENO (19) signal and GENO_19 value in GENO_STATUS register have been modified by distant C2C. Writing 1 to this bit sets the bit. Writing 0 has no effect.	RW W1toSet	0
18	GENO_IRQ_18	Reading 1 indicates C2c_Sscm_GENO (18) signal and GENO_18 value in GENO_STATUS register have been modified by distant C2C. Writing 1 to this bit sets the bit. Writing 0 has no effect.	RW W1toSet	0
17	GENO_IRQ_17	Reading 1 indicates C2c_Sscm_GENO (17) signal and GENO_17 value in GENO_STATUS register have been modified by distant C2C. Writing 1 to this bit sets the bit. Writing 0 has no effect.	RW W1toSet	0
16	GENO_IRQ_16	Reading 1 indicates C2c_Sscm_GENO (16) signal and GENO_16 value in GENO_STATUS register have been modified by distant C2C. Writing 1 to this bit sets the bit. Writing 0 has no effect.	RW W1toSet	0
15	GENO_IRQ_15	Reading 1 indicates C2c_Sscm_GENO (15) signal and GENO_15 value in GENO_STATUS register have been modified by distant C2C. Writing 1 to this bit sets the bit. Writing 0 has no effect.	RW W1toSet	0
14	GENO_IRQ_14	Reading 1 indicates C2c_Sscm_GENO (14) signal and GENO_14 value in GENO_STATUS register have been modified by distant C2C. Writing 1 to this bit sets the bit. Writing 0 has no effect.	RW W1toSet	0
13	GENO_IRQ_13	Reading 1 indicates C2c_Sscm_GENO (13) signal and GENO_13 value in GENO_STATUS register have been modified by distant C2C. Writing 1 to this bit sets the bit. Writing 0 has no effect.	RW W1toSet	0

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Bits	Field Name	Description	Type	Reset
12	GENO_IRQ_12	Reading 1 indicates C2c_Sscm_GENO (12) signal and GENO_12 value in GENO_STATUS register have been modified by distant C2C. Writing 1 to this bit sets the bit. Writing 0 has no effect.	RW W1toSet	0
11	GENO_IRQ_11	Reading 1 indicates C2c_Sscm_GENO (11) signal and GENO_11 value in GENO_STATUS register have been modified by distant C2C. Writing 1 to this bit sets the bit. Writing 0 has no effect.	RW W1toSet	0
10	GENO_IRQ_10	Reading 1 indicates C2c_Sscm_GENO (10) signal and GENO_10 value in GENO_STATUS register have been modified by distant C2C. Writing 1 to this bit sets the bit. Writing 0 has no effect.	RW W1toSet	0
9	GENO_IRQ_9	Reading 1 indicates C2c_Sscm_GENO (9) signal and GENO_9 value in GENO_STATUS register have been modified by distant C2C. Writing 1 to this bit sets the bit. Writing 0 has no effect.	RW W1toSet	0
8	GENO_IRQ_8	Reading 1 indicates C2c_Sscm_GENO (8) signal and GENO_8 value in GENO_STATUS register have been modified by distant C2C. Writing 1 to this bit sets the bit. Writing 0 has no effect.	RW W1toSet	0
7	GENO_IRQ_7	Reading 1 indicates C2c_Sscm_GENO (7) signal and GENO_7 value in GENO_STATUS register have been modified by distant C2C. Writing 1 to this bit sets the bit. Writing 0 has no effect.	RW W1toSet	0
6	GENO_IRQ_6	Reading 1 indicates C2c_Sscm_GENO (6) signal and GENO_6 value in GENO_STATUS register have been modified by distant C2C. Writing 1 to this bit sets the bit. Writing 0 has no effect.	RW W1toSet	0
5	GENO_IRQ_5	Reading 1 indicates C2c_Sscm_GENO (5) signal and GENO_5 value in GENO_STATUS register have been modified by distant C2C. Writing 1 to this bit sets the bit. Writing 0 has no effect.	RW W1toSet	0
4	GENO_IRQ_4	Reading 1 indicates C2c_Sscm_GENO (4) signal and GENO_4 value in GENO_STATUS register have been modified by distant C2C. Writing 1 to this bit sets the bit. Writing 0 has no effect.	RW W1toSet	0
3	GENO_IRQ_3	Reading 1 indicates C2c_Sscm_GENO (3) signal and GENO_3 value in GENO_STATUS register have been modified by distant C2C. Writing 1 to this bit sets the bit. Writing 0 has no effect.	RW W1toSet	0
2	GENO_IRQ_2	Reading 1 indicates C2c_Sscm_GENO (2) signal and GENO_2 value in GENO_STATUS register have been modified by distant C2C. Writing 1 to this bit sets the bit. Writing 0 has no effect.	RW W1toSet	0

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Bits	Field Name	Description	Type	Reset
1	GENO_IRQ_1	Reading 1 indicates C2c_Sscm_GENO (1) signal and GENO_1 value in GENO_STATUS register have been modified by distant C2C. Writing 1 to this bit sets the bit. Writing 0 has no effect.	RW W1toSet	0
0	GENO_IRQ_0	Reading 1 indicates C2c_Sscm_GENO (0) signal and GENO_0 value in GENO_STATUS register have been modified by distant C2C. Writing 1 to this bit sets the bit. Writing 0 has no effect.	RW W1toSet	0

Table 14-94. Register Call Summary for Register C2C_IRQ_RAW_STATUS_1

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- C2C Register Summary: [0]

Table 14-95. C2C_IRQ_ENABLE_STATUS_0

Address Offset	0x0000 001C		
Physical Address	0x5C00001C	**Instance**	C2C
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												WAIT_IRQ	WAKE_ACK_IRQ	RX_MAX_FREQ_ACK_IRQ	TX_FREQ_IRQ

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved	R	0x0000000
3	WAIT_IRQ	Reading 1 indicates WAIT value in WAIT register has been modified by distant C2C and interrupt source is not masked. Writing 1 to this bit clears the bit. Writing 0 has no effect.	RW W1toClr	0
2	WAKE_ACK_IRQ	Reading 1 indicates WAKE_ACK value in the WAKE_ACK register has been modified by distant C2C and interrupt source is not masked. Writing 1 to this bit clears the bit. Writing 0 has no effect.	RW W1toClr	0
1	RX_MAX_FREQ_ACK_IRQ	Reading 1 indicates GPI is not turned on OR RX_MAX_FREQ_ACK value in the RX_MAX_FREQ_ACK register equal RX_MAX_FREQ value in the RX_MAX_FREQ register.	RW W1toClr	0
0	TX_FREQ_IRQ	Reading 1 indicates that the FCLK_FREQ value in the FCLK_FREQ register has been updated AND the SSCM has finished updating the new division for the Tx clock.	RW W1toClr	0

Table 14-96. Register Call Summary for Register C2C_IRQ_ENABLE_STATUS_0

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- C2C Register Summary: [0]

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Table 14-97. C2C_IRQ_ENABLE_STATUS_1

Address Offset	0x0000 0020		
Physical Address	0x5C000020	**Instance**	C2C
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GENO_IRQ_31	GENO_IRQ_30	GENO_IRQ_29	GENO_IRQ_28	GENO_IRQ_27	GENO_IRQ_26	GENO_IRQ_25	GENO_IRQ_24	GENO_IRQ_23	GENO_IRQ_22	GENO_IRQ_21	GENO_IRQ_20	GENO_IRQ_19	GENO_IRQ_18	GENO_IRQ_17	GENO_IRQ_16	GENO_IRQ_15	GENO_IRQ_14	GENO_IRQ_13	GENO_IRQ_12	GENO_IRQ_11	GENO_IRQ_10	GENO_IRQ_9	GENO_IRQ_8	GENO_IRQ_7	GENO_IRQ_6	GENO_IRQ_5	GENO_IRQ_4	GENO_IRQ_3	GENO_IRQ_2	GENO_IRQ_1	GENO_IRQ_0

Bits	Field Name	Description	Type	Reset
31	GENO_IRQ_31	Reading 1 indicates C2c_Sscm_GENO (31) signal and GENO_31 value in GENO_STATUS register have been modified by distant C2C and interrupt source is not masked. Writing 1 to this bit clears the bit. Writing 0 has no effect.	RW W1toClr	0
30	GENO_IRQ_30	Reading 1 indicates C2c_Sscm_GENO (30) signal and GENO_30 value in GENO_STATUS register have been modified by distant C2C and interrupt source is not masked. Writing 1 to this bit clears the bit. Writing 0 has no effect.	RW W1toClr	0
29	GENO_IRQ_29	Reading 1 indicates C2c_Sscm_GENO (29) signal and GENO_29 value in GENO_STATUS register have been modified by distant C2C and interrupt source is not masked. Writing 1 to this bit clears the bit. Writing 0 has no effect.	RW W1toClr	0
28	GENO_IRQ_28	Reading 1 indicates C2c_Sscm_GENO (28) signal and GENO_28 value in GENO_STATUS register have been modified by distant C2C and interrupt source is not masked. Writing 1 to this bit clears the bit. Writing 0 has no effect.	RW W1toClr	0
27	GENO_IRQ_27	Reading 1 indicates C2c_Sscm_GENO (27) signal and GENO_27 value in GENO_STATUS register have been modified by distant C2C and interrupt source is not masked. Writing 1 to this bit clears the bit. Writing 0 has no effect.	RW W1toClr	0
26	GENO_IRQ_26	Reading 1 indicates C2c_Sscm_GENO (26) signal and GENO_26 value in GENO_STATUS register have been modified by distant C2C and interrupt source is not masked. Writing 1 to this bit clears the bit. Writing 0 has no effect.	RW W1toClr	0
25	GENO_IRQ_25	Reading 1 indicates C2c_Sscm_GENO (25) signal and GENO_25 value in GENO_STATUS register have been modified by distant C2C and interrupt source is not masked. Writing 1 to this bit clears the bit. Writing 0 has no effect.	RW W1toClr	0
24	GENO_IRQ_24	Reading 1 indicates C2c_Sscm_GENO (24) signal and GENO_24 value in GENO_STATUS register have been modified by distant C2C and interrupt source is not masked. Writing 1 to this bit clears the bit. Writing 0 has no effect.	RW W1toClr	0
23	GENO_IRQ_23	Reading 1 indicates C2c_Sscm_GENO (23) signal and GENO_23 value in GENO_STATUS register have been modified by distant C2C and interrupt source is not masked. Writing 1 to this bit clears the bit. Writing 0 has no effect.	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
22	GENO_IRQ_22	Reading 1 indicates C2c_Sscm_GENO (22) signal and GENO_22 value in GENO_STATUS register have been modified by distant C2C and interrupt source is not masked. Writing 1 to this bit clears the bit. Writing 0 has no effect.	RW W1toClr	0
21	GENO_IRQ_21	Reading 1 indicates C2c_Sscm_GENO (21) signal and GENO_21 value in GENO_STATUS register have been modified by distant C2C and interrupt source is not masked. Writing 1 to this bit clears the bit. Writing 0 has no effect.	RW W1toClr	0
20	GENO_IRQ_20	Reading 1 indicates C2c_Sscm_GENO (20) signal and GENO_20 value in GENO_STATUS register have been modified by distant C2C and interrupt source is not masked. Writing 1 to this bit clears the bit. Writing 0 has no effect.	RW W1toClr	0
19	GENO_IRQ_19	Reading 1 indicates C2c_Sscm_GENO (19) signal and GENO_19 value in GENO_STATUS register have been modified by distant C2C and interrupt source is not masked. Writing 1 to this bit clears the bit. Writing 0 has no effect.	RW W1toClr	0
18	GENO_IRQ_18	Reading 1 indicates C2c_Sscm_GENO (18) signal and GENO_18 value in GENO_STATUS register have been modified by distant C2C and interrupt source is not masked. Writing 1 to this bit clears the bit. Writing 0 has no effect.	RW W1toClr	0
17	GENO_IRQ_17	Reading 1 indicates C2c_Sscm_GENO (17) signal and GENO_17 value in GENO_STATUS register have been modified by distant C2C and interrupt source is not masked. Writing 1 to this bit clears the bit. Writing 0 has no effect.	RW W1toClr	0
16	GENO_IRQ_16	Reading 1 indicates C2c_Sscm_GENO (16) signal and GENO_16 value in GENO_STATUS register have been modified by distant C2C and interrupt source is not masked. Writing 1 to this bit clears the bit. Writing 0 has no effect.	RW W1toClr	0
15	GENO_IRQ_15	Reading 1 indicates C2c_Sscm_GENO (15) signal and GENO_15 value in GENO_STATUS register have been modified by distant C2C and interrupt source is not masked. Writing 1 to this bit clears the bit. Writing 0 has no effect.	RW W1toClr	0
14	GENO_IRQ_14	Reading 1 indicates C2c_Sscm_GENO (14) signal and GENO_14 value in GENO_STATUS register have been modified by distant C2C and interrupt source is not masked. Writing 1 to this bit clears the bit. Writing 0 has no effect.	RW W1toClr	0
13	GENO_IRQ_13	Reading 1 indicates C2c_Sscm_GENO (13) signal and GENO_13 value in GENO_STATUS register have been modified by distant C2C and interrupt source is not masked. Writing 1 to this bit clears the bit. Writing 0 has no effect.	RW W1toClr	0
12	GENO_IRQ_12	Reading 1 indicates C2c_Sscm_GENO (12) signal and GENO_12 value in GENO_STATUS register have been modified by distant C2C and interrupt source is not masked. Writing 1 to this bit clears the bit. Writing 0 has no effect.	RW W1toClr	0
11	GENO_IRQ_11	Reading 1 indicates C2c_Sscm_GENO (11) signal and GENO_11 value in GENO_STATUS register have been modified by distant C2C and interrupt source is not masked. Writing 1 to this bit clears the bit. Writing 0 has no effect.	RW W1toClr	0
10	GENO_IRQ_10	Reading 1 indicates C2c_Sscm_GENO (10) signal and GENO_10 value in GENO_STATUS register have been modified by distant C2C and interrupt source is not masked. Writing 1 to this bit clears the bit. Writing 0 has no effect.	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
9	GENO_IRQ_9	Reading 1 indicates C2c_Sscm_GENO (9) signal and GENO_9 value in GENO_STATUS register have been modified by distant C2C and interrupt source is not masked. Writing 1 to this bit clears the bit. Writing 0 has no effect.	RW W1toClr	0
8	GENO_IRQ_8	Reading 1 indicates C2c_Sscm_GENO (8) signal and GENO_8 value in GENO_STATUS register have been modified by distant C2C and interrupt source is not masked. Writing 1 to this bit clears the bit. Writing 0 has no effect.	RW W1toClr	0
7	GENO_IRQ_7	Reading 1 indicates C2c_Sscm_GENO (7) signal and GENO_7 value in GENO_STATUS register have been modified by distant C2C and interrupt source is not masked. Writing 1 to this bit clears the bit. Writing 0 has no effect.	RW W1toClr	0
6	GENO_IRQ_6	Reading 1 indicates C2c_Sscm_GENO (6) signal and GENO_6 value in GENO_STATUS register have been modified by distant C2C and interrupt source is not masked. Writing 1 to this bit clears the bit. Writing 0 has no effect.	RW W1toClr	0
5	GENO_IRQ_5	Reading 1 indicates C2c_Sscm_GENO (5) signal and GENO_5 value in GENO_STATUS register have been modified by distant C2C and interrupt source is not masked. Writing 1 to this bit clears the bit. Writing 0 has no effect.	RW W1toClr	0
4	GENO_IRQ_4	Reading 1 indicates C2c_Sscm_GENO (4) signal and GENO_4 value in GENO_STATUS register have been modified by distant C2C and interrupt source is not masked. Writing 1 to this bit clears the bit. Writing 0 has no effect.	RW W1toClr	0
3	GENO_IRQ_3	Reading 1 indicates C2c_Sscm_GENO (3) signal and GENO_3 value in GENO_STATUS register have been modified by distant C2C and interrupt source is not masked. Writing 1 to this bit clears the bit. Writing 0 has no effect.	RW W1toClr	0
2	GENO_IRQ_2	Reading 1 indicates C2c_Sscm_GENO (2) signal and GENO_2 value in GENO_STATUS register have been modified by distant C2C and interrupt source is not masked. Writing 1 to this bit clears the bit. Writing 0 has no effect.	RW W1toClr	0
1	GENO_IRQ_1	Reading 1 indicates C2c_Sscm_GENO (1) signal and GENO_1 value in GENO_STATUS register have been modified by distant C2C and interrupt source is not masked. Writing 1 to this bit clears the bit. Writing 0 has no effect.	RW W1toClr	0
0	GENO_IRQ_0	Reading 1 indicates C2c_Sscm_GENO (0) signal and GENO_0 value in GENO_STATUS register have been modified by distant C2C and interrupt source is not masked. Writing 1 to this bit clears the bit. Writing 0 has no effect.	RW W1toClr	0

Table 14-98. Register Call Summary for Register C2C_IRQ_ENABLE_STATUS_1

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- C2C Register Summary: [0]

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Table 14-99. C2C_IRQ_ENABLE_SET_0

Address Offset	0x0000 0024		
Physical Address	0x5C000024	**Instance**	C2C
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												WAIT_IRQ_EN	WAKE_ACK_IRQ_EN	RX_MAX_FREQ_ACK_IRQ_EN	TX_FREQ_IRQ_EN

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved	R	0x0000000
3	WAIT_IRQ_EN	Interrupt enable for WAIT IRQ. Writing 1 to this bit sets the bit. Writing 0 has no effect.	RW W1toSet	0
2	WAKE_ACK_IRQ_EN	Interrupt enable for WAKE_ACK IRQ. Writing 1 to this bit sets the bit. Writing 0 has no effect.	RW W1toSet	0
1	RX_MAX_FREQ_ACK_IRQ_EN	Interrupt enable for RX_MAX_FREQ_ACK IRQ. Writing 1 to this bit sets the bit. Writing 0 has no effect.	RW W1toSet	0
0	TX_FREQ_IRQ_EN	Interrupt enable for TX_FREQ IRQ. Writing 1 to this bit sets the bit. Writing 0 has no effect.	RW W1toSet	0

Table 14-100. Register Call Summary for Register C2C_IRQ_ENABLE_SET_0

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- C2C Register Summary: [0]

Table 14-101. C2C_IRQ_ENABLE_SET_1

Address Offset	0x0000 0028		
Physical Address	0x5C000028	**Instance**	C2C
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GENO_IRQ_31_EN	GENO_IRQ_30_EN	GENO_IRQ_29_EN	GENO_IRQ_28_EN	GENO_IRQ_27_EN	GENO_IRQ_26_EN	GENO_IRQ_25_EN	GENO_IRQ_24_EN	GENO_IRQ_23_EN	GENO_IRQ_22_EN	GENO_IRQ_21_EN	GENO_IRQ_20_EN	GENO_IRQ_19_EN	GENO_IRQ_18_EN	GENO_IRQ_17_EN	GENO_IRQ_16_EN	GENO_IRQ_15_EN	GENO_IRQ_14_EN	GENO_IRQ_13_EN	GENO_IRQ_12_EN	GENO_IRQ_11_EN	GENO_IRQ_10_EN	GENO_IRQ_9_EN	GENO_IRQ_8_EN	GENO_IRQ_7_EN	GENO_IRQ_6_EN	GENO_IRQ_5_EN	GENO_IRQ_4_EN	GENO_IRQ_3_EN	GENO_IRQ_2_EN	GENO_IRQ_1_EN	GENO_IRQ_0_EN

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Bits	Field Name	Description	Type	Reset
31	GENO_IRQ_31_EN	Interrupt enable for GENO_IRQ_31 IRQ.	RW W1toSet	0
30	GENO_IRQ_30_EN	Interrupt enable for GENO_IRQ_30 IRQ.	RW W1toSet	0
29	GENO_IRQ_29_EN	Interrupt enable for GENO_IRQ_29 IRQ.	RW W1toSet	0
28	GENO_IRQ_28_EN	Interrupt enable for GENO_IRQ_28 IRQ.	RW W1toSet	0
27	GENO_IRQ_27_EN	Interrupt enable for GENO_IRQ_27 IRQ.	RW W1toSet	0
26	GENO_IRQ_26_EN	Interrupt enable for GENO_IRQ_26 IRQ.	RW W1toSet	0
25	GENO_IRQ_25_EN	Interrupt enable for GENO_IRQ_25 IRQ.	RW W1toSet	0
24	GENO_IRQ_24_EN	Interrupt enable for GENO_IRQ_24 IRQ.	RW W1toSet	0
23	GENO_IRQ_23_EN	Interrupt enable for GENO_IRQ_23 IRQ.	RW W1toSet	0
22	GENO_IRQ_22_EN	Interrupt enable for GENO_IRQ_22 IRQ.	RW W1toSet	0
21	GENO_IRQ_21_EN	Interrupt enable for GENO_IRQ_21 IRQ.	RW W1toSet	0
20	GENO_IRQ_20_EN	Interrupt enable for GENO_IRQ_20 IRQ.	RW W1toSet	0
19	GENO_IRQ_19_EN	Interrupt enable for GENO_IRQ_19 IRQ.	RW W1toSet	0
18	GENO_IRQ_18_EN	Interrupt enable for GENO_IRQ_18 IRQ.	RW W1toSet	0
17	GENO_IRQ_17_EN	Interrupt enable for GENO_IRQ_17 IRQ.	RW W1toSet	0
16	GENO_IRQ_16_EN	Interrupt enable for GENO_IRQ_16 IRQ.	RW W1toSet	0
15	GENO_IRQ_15_EN	Interrupt enable for GENO_IRQ_15 IRQ.	RW W1toSet	0
14	GENO_IRQ_14_EN	Interrupt enable for GENO_IRQ_14 IRQ.	RW W1toSet	0
13	GENO_IRQ_13_EN	Interrupt enable for GENO_IRQ_13 IRQ.	RW W1toSet	0
12	GENO_IRQ_12_EN	Interrupt enable for GENO_IRQ_12 IRQ.	RW W1toSet	0
11	GENO_IRQ_11_EN	Interrupt enable for GENO_IRQ_11 IRQ.	RW W1toSet	0
10	GENO_IRQ_10_EN	Interrupt enable for GENO_IRQ_10 IRQ.	RW W1toSet	0
9	GENO_IRQ_9_EN	Interrupt enable for GENO_IRQ_9 IRQ.	RW W1toSet	0
8	GENO_IRQ_8_EN	Interrupt enable for GENO_IRQ_8 IRQ.	RW W1toSet	0
7	GENO_IRQ_7_EN	Interrupt enable for GENO_IRQ_7 IRQ.	RW W1toSet	0
6	GENO_IRQ_6_EN	Interrupt enable for GENO_IRQ_6 IRQ.	RW W1toSet	0
5	GENO_IRQ_5_EN	Interrupt enable for GENO_IRQ_5 IRQ.	RW W1toSet	0
4	GENO_IRQ_4_EN	Interrupt enable for GENO_IRQ_4 IRQ.	RW W1toSet	0
3	GENO_IRQ_3_EN	Interrupt enable for GENO_IRQ_3 IRQ.	RW W1toSet	0

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Bits	Field Name	Description	Type	Reset
2	GENO_IRQ_2_EN	Interrupt enable for GENO_IRQ_2 IRQ.	RW W1toSet	0
1	GENO_IRQ_1_EN	Interrupt enable for GENO_IRQ_1 IRQ.	RW W1toSet	0
0	GENO_IRQ_0_EN	Interrupt enable for GENO_IRQ_0 IRQ.	RW W1toSet	0

Table 14-102. Register Call Summary for Register C2C_IRQ_ENABLE_SET_1

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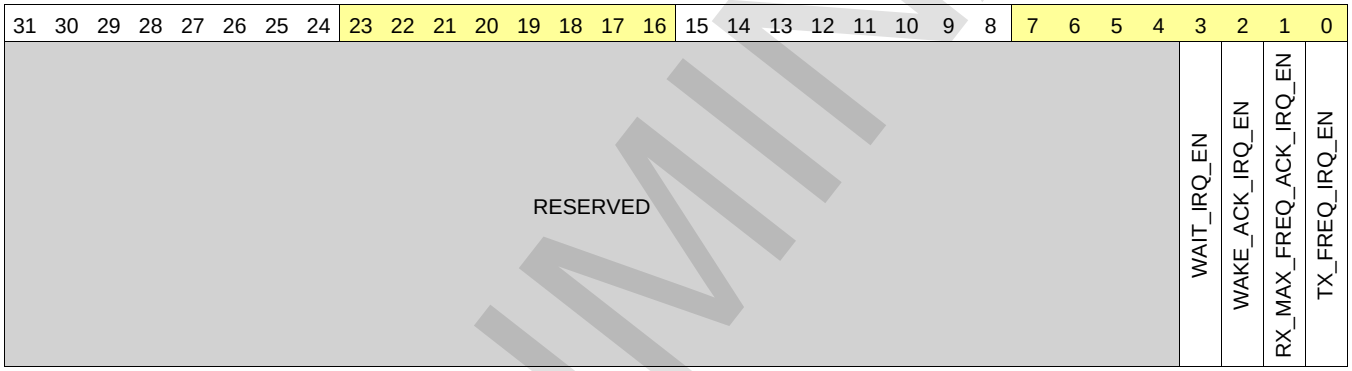
- C2C Register Summary: [0]

Table 14-103. C2C_IRQ_ENABLE_CLEAR_0

Address Offset	0x0000 002C		
Physical Address	0x5C00002C	**Instance**	C2C
Description			
Type	RW		



Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved	R	0x0000000
3	WAIT_IRQ_EN	Interrupt enable for WAIT IRQ.	RW W1toClr	0
2	WAKE_ACK_IRQ_EN	Interrupt enable for WAKE_ACK IRQ.	RW W1toClr	0
1	RX_MAX_FREQ_ACK_IRQ_EN	Interrupt enable for RX_MAX_FREQ_ACK IRQ.	RW W1toClr	0
0	TX_FREQ_IRQ_EN	Interrupt enable for TX_FREQ IRQ.	RW W1toClr	0

Table 14-104. Register Call Summary for Register C2C_IRQ_ENABLE_CLEAR_0

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- C2C Register Summary: [0]

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Table 14-105. C2C_IRQ_ENABLE_CLEAR_1

Address Offset	0x0000 0030		
Physical Address	0x5C000030	**Instance**	C2C
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GENO_IRQ_31_EN	GENO_IRQ_30_EN	GENO_IRQ_29_EN	GENO_IRQ_28_EN	GENO_IRQ_27_EN	GENO_IRQ_26_EN	GENO_IRQ_25_EN	GENO_IRQ_24_EN	GENO_IRQ_23_EN	GENO_IRQ_22_EN	GENO_IRQ_21_EN	GENO_IRQ_20_EN	GENO_IRQ_19_EN	GENO_IRQ_18_EN	GENO_IRQ_17_EN	GENO_IRQ_16_EN	GENO_IRQ_15_EN	GENO_IRQ_14_EN	GENO_IRQ_13_EN	GENO_IRQ_12_EN	GENO_IRQ_11_EN	GENO_IRQ_10_EN	GENO_IRQ_9_EN	GENO_IRQ_8_EN	GENO_IRQ_7_EN	GENO_IRQ_6_EN	GENO_IRQ_5_EN	GENO_IRQ_4_EN	GENO_IRQ_3_EN	GENO_IRQ_2_EN	GENO_IRQ_1_EN	GENO_IRQ_0_EN

Bits	Field Name	Description	Type	Reset
31	GENO_IRQ_31_EN	Interrupt enable for GENO_IRQ_31 IRQ. Writing 1 to this bit clears the bit. Writing 0 has no effect.	RW W1toClr	0
30	GENO_IRQ_30_EN	Interrupt enable for GENO_IRQ_30 IRQ.	RW W1toClr	0
29	GENO_IRQ_29_EN	Interrupt enable for GENO_IRQ_29 IRQ.	RW W1toClr	0
28	GENO_IRQ_28_EN	Interrupt enable for GENO_IRQ_28 IRQ.	RW W1toClr	0
27	GENO_IRQ_27_EN	Interrupt enable for GENO_IRQ_27 IRQ.	RW W1toClr	0
26	GENO_IRQ_26_EN	Interrupt enable for GENO_IRQ_26 IRQ.	RW W1toClr	0
25	GENO_IRQ_25_EN	Interrupt enable for GENO_IRQ_25 IRQ.	RW W1toClr	0
24	GENO_IRQ_24_EN	Interrupt enable for GENO_IRQ_24 IRQ.	RW W1toClr	0
23	GENO_IRQ_23_EN	Interrupt enable for GENO_IRQ_23 IRQ.	RW W1toClr	0
22	GENO_IRQ_22_EN	Interrupt enable for GENO_IRQ_22 IRQ.	RW W1toClr	0
21	GENO_IRQ_21_EN	Interrupt enable for GENO_IRQ_21 IRQ.	RW W1toClr	0
20	GENO_IRQ_20_EN	Interrupt enable for GENO_IRQ_20 IRQ.	RW W1toClr	0
19	GENO_IRQ_19_EN	Interrupt enable for GENO_IRQ_19 IRQ.	RW W1toClr	0
18	GENO_IRQ_18_EN	Interrupt enable for GENO_IRQ_18 IRQ.	RW W1toClr	0
17	GENO_IRQ_17_EN	Interrupt enable for GENO_IRQ_17 IRQ.	RW W1toClr	0
16	GENO_IRQ_16_EN	Interrupt enable for GENO_IRQ_16 IRQ.	RW W1toClr	0
15	GENO_IRQ_15_EN	Interrupt enable for GENO_IRQ_15 IRQ.	RW W1toClr	0
14	GENO_IRQ_14_EN	Interrupt enable for GENO_IRQ_14 IRQ.	RW W1toClr	0
13	GENO_IRQ_13_EN	Interrupt enable for GENO_IRQ_13 IRQ.	RW W1toClr	0
12	GENO_IRQ_12_EN	Interrupt enable for GENO_IRQ_12 IRQ.	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
11	GENO_IRQ_11_EN	Interrupt enable for GENO_IRQ_11 IRQ.	RW W1toClr	0
10	GENO_IRQ_10_EN	Interrupt enable for GENO_IRQ_10 IRQ.	RW W1toClr	0
9	GENO_IRQ_9_EN	Interrupt enable for GENO_IRQ_9 IRQ.	RW W1toClr	0
8	GENO_IRQ_8_EN	Interrupt enable for GENO_IRQ_8 IRQ.	RW W1toClr	0
7	GENO_IRQ_7_EN	Interrupt enable for GENO_IRQ_7 IRQ.	RW W1toClr	0
6	GENO_IRQ_6_EN	Interrupt enable for GENO_IRQ_6 IRQ.	RW W1toClr	0
5	GENO_IRQ_5_EN	Interrupt enable for GENO_IRQ_5 IRQ.	RW W1toClr	0
4	GENO_IRQ_4_EN	Interrupt enable for GENO_IRQ_4 IRQ.	RW W1toClr	0
3	GENO_IRQ_3_EN	Interrupt enable for GENO_IRQ_3 IRQ.	RW W1toClr	0
2	GENO_IRQ_2_EN	Interrupt enable for GENO_IRQ_2 IRQ.	RW W1toClr	0
1	GENO_IRQ_1_EN	Interrupt enable for GENO_IRQ_1 IRQ.	RW W1toClr	0
0	GENO_IRQ_0_EN	Interrupt enable for GENO_IRQ_0 IRQ.	RW W1toClr	0

Table 14-106. Register Call Summary for Register C2C_IRQ_ENABLE_CLEAR_1

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- C2C Register Summary: [0]

Table 14-107. C2C_FCLK_FREQ

Address Offset	0x0000 0040		
Physical Address	0x5C000040	**Instance**	C2C
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								FCLK_FREQ							

Bits	Field Name	Description	Type	Reset
31:10	RESERVED	Reserved	R	0x000000
9:0	FCLK_FREQ	Value of the Functional clock frequency according to OPP written by software. Default value is 400 (MHz).	RW	0x190

Table 14-108. Register Call Summary for Register C2C_FCLK_FREQ

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- C2C Register Summary: [0]

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Table 14-109. C2C_RX_MAX_FREQ

Address Offset	0x0000 0044		
Physical Address	0x5C000044	**Instance**	C2C
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RX_MAX_FREQ							

Bits	Field Name	Description	Type	Reset
31:10	RESERVED	Reserved	R	0x000000
9:0	RX_MAX_FREQ	Value of the requested RX maximum clock frequency according to OPP written by software. Default value is 50 (MHz).	RW	0x032

Table 14-110. Register Call Summary for Register C2C_RX_MAX_FREQ

C2C Register Manual

- C2C Register Summary: [0]

Table 14-111. C2C_TX_MAX_FREQ

Address Offset	0x0000 0048		
Physical Address	0x5C000048	**Instance**	C2C
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								TX_MAX_FREQ							

Bits	Field Name	Description	Type	Reset
31:10	RESERVED	Reserved	R	0x000000
9:0	TX_MAX_FREQ	Value of the requested TX maximum clock frequency set by distant C2C. Default value is 50 (MHz).	RW	0x032

Table 14-112. Register Call Summary for Register C2C_TX_MAX_FREQ

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- C2C Register Summary: [0]

Table 14-113. C2C_RX_MAX_FREQ_ACK

Address Offset	0x0000 004C		
Physical Address	0x5C00004C	**Instance**	C2C
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RX_MAX_FREQ_ACK							

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Bits	Field Name	Description	Type	Reset
31:10	RESERVED	Reserved	R	0x000000
9:0	RX_MAX_FREQ_ACK	Acknowledged maximum Rx clock frequency. Set by distant C2C. Default value is 50 (MHz).	RW	0x032

Table 14-114. Register Call Summary for Register C2C_RX_MAX_FREQ_ACK

C2C Register Manual
- C2C Register Summary: [0]

Table 14-115. C2C_WAKE_REQ

Address Offset	0x0000 0050		
Physical Address	0x5C000050	**Instance**	C2C
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															WAKE_REQ

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	WAKE_REQ	Value of the WAKE_REQ set by software	RW	0

Table 14-116. Register Call Summary for Register C2C_WAKE_REQ

C2C Register Manual
- C2C Register Summary: [0]

Table 14-117. C2C_WAKE_ACK

Address Offset	0x0000 0054		
Physical Address	0x5C000054	**Instance**	C2C
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															WAKE_ACK

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	WAKE_ACK	Value of the WAKE_ACK set by distant C2C	RW	0

Table 14-118. Register Call Summary for Register C2C_WAKE_ACK

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- C2C Register Summary: [0]

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Table 14-119. C2C_STANDBY

Address Offset	0x0000 0060		
Physical Address	0x5C000060	**Instance**	C2C
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															STANDBY

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	STANDBY	Value of the STANDBY set by software	RW	1

Table 14-120. Register Call Summary for Register C2C_STANDBY

C2C Register Manual

- C2C Register Summary: [0]

Table 14-121. C2C_STANDBY_IN

Address Offset	0x0000 0064		
Physical Address	0x5C000064	**Instance**	C2C
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															STANDBY

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	STANDBY	Value of the STANDBY set by distant C2C	RW	1

Table 14-122. Register Call Summary for Register C2C_STANDBY_IN

C2C Register Manual

- C2C Register Summary: [0]

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Table 14-123. C2C_WAIT

Address Offset	0x0000 0068		
Physical Address	0x5C000068	**Instance**	C2C
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															WAIT

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	WAIT	Value of the WAIT set by distant C2C	RW	1

Table 14-124. Register Call Summary for Register C2C_WAIT

C2C Register Manual

- C2C Register Summary: [0]

Table 14-125. C2C_GENI_CONTROL

Address Offset	0x0000 0070		
Physical Address	0x5C000070	**Instance**	C2C
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GENI_31	GENI_30	GENI_29	GENI_28	GENI_27	GENI_26	GENI_25	GENI_24	GENI_23	GENI_22	GENI_21	GENI_20	GENI_19	GENI_18	GENI_17	GENI_16	GENI_15	GENI_14	GENI_13	GENI_12	GENI_11	GENI_10	GENI_9	GENI_8	GENI_7	GENI_6	GENI_5	GENI_4	GENI_3	GENI_2	GENI_1	GENI_0

Bits	Field Name	Description	Type	Reset
31	GENI_31	If GENI_MASK_31 in GENI_MASK register is reset, GENI_31 is the value of C2C_Sscm_GenI_31 and cannot be modified by software. (signal is not masked) If GENI_MASK_31 is set (signal is masked), GENI_31 can be modified by software.	RW	0
30	GENI_30	f GENI_MASK_30 in GENI_MASK register is reset, GENI_30 is the value of C2C_Sscm_GenI_30 and cannot be modified by software. (signal is not masked) If GENI_MASK_30 is set (signal is masked), GENI_30 can be modified by software.	RW	0
29	GENI_29	f GENI_MASK_29 in GENI_MASK register is reset, GENI_29 is the value of C2C_Sscm_GenI_29 and cannot be modified by software. (signal is not masked) If GENI_MASK_29 is set (signal is masked), GENI_29 can be modified by software.	RW	0
28	GENI_28	f GENI_MASK_28 in GENI_MASK register is reset, GENI_28 is the value of C2C_Sscm_GenI_28 and cannot be modified by software. (signal is not masked) If GENI_MASK_28 is set (signal is masked), GENI_28 can be modified by software.	RW	0
27	GENI_27	f GENI_MASK_27 in GENI_MASK register is reset, GENI_27 is the value of C2C_Sscm_GenI_27 and cannot be modified by software. (signal is not masked) If GENI_MASK_27 is set (signal is masked), GENI_27 can be modified by software.	RW	0

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Bits	Field Name	Description	Type	Reset
26	GENI_26	f GENI_MASK_26 in GENI_MASK register is reset, GENI_26 is the value of C2C_Sscm_GenI_26 and cannot be modified by software. (signal is not masked) If GENI_MASK_26 is set (signal is masked), GENI_26 can be modified by software.	RW	0
25	GENI_25	f GENI_MASK_25 in GENI_MASK register is reset, GENI_25 is the value of C2C_Sscm_GenI_25 and cannot be modified by software. (signal is not masked) If GENI_MASK_25 is set (signal is masked), GENI_25 can be modified by software.	RW	0
24	GENI_24	f GENI_MASK_24 in GENI_MASK register is reset, GENI_24 is the value of C2C_Sscm_GenI_24 and cannot be modified by software. (signal is not masked) If GENI_MASK_24 is set (signal is masked), GENI_24 can be modified by software.	RW	0
23	GENI_23	f GENI_MASK_23 in GENI_MASK register is reset, GENI_23 is the value of C2C_Sscm_GenI_23 and cannot be modified by software. (signal is not masked) If GENI_MASK_23 is set (signal is masked), GENI_23 can be modified by software.	RW	0
22	GENI_22	f GENI_MASK_22 in GENI_MASK register is reset, GENI_22 is the value of C2C_Sscm_GenI_22 and cannot be modified by software. (signal is not masked) If GENI_MASK_22 is set (signal is masked), GENI_22 can be modified by software.	RW	0
21	GENI_21	f GENI_MASK_21 in GENI_MASK register is reset, GENI_21 is the value of C2C_Sscm_GenI_31 and cannot be modified by software. (signal is not masked) If GENI_MASK_21 is set (signal is masked), GENI_21 can be modified by software.	RW	0
20	GENI_20	f GENI_MASK_20 in GENI_MASK register is reset, GENI_20 is the value of C2C_Sscm_GenI_20 and cannot be modified by software. (signal is not masked) If GENI_MASK_20 is set (signal is masked), GENI_20 can be modified by software.	RW	0
19	GENI_19	f GENI_MASK_19 in GENI_MASK register is reset, GENI_19 is the value of C2C_Sscm_GenI_19 and cannot be modified by software. (signal is not masked) If GENI_MASK_19 is set (signal is masked), GENI_19 can be modified by software.	RW	0
18	GENI_18	f GENI_MASK_18 in GENI_MASK register is reset, GENI_18 is the value of C2C_Sscm_GenI_31 and cannot be modified by software. (signal is not masked) If GENI_MASK_18 is set (signal is masked), GENI_18 can be modified by software.	RW	0
17	GENI_17	f GENI_MASK_17 in GENI_MASK register is reset, GENI_17 is the value of C2C_Sscm_GenI_31 and cannot be modified by software. (signal is not masked) If GENI_MASK_17 is set (signal is masked), GENI_17 can be modified by software.	RW	0
16	GENI_16	f GENI_MASK_16 in GENI_MASK register is reset, GENI_16 is the value of C2C_Sscm_GenI_16 and cannot be modified by software. (signal is not masked) If GENI_MASK_156is set (signal is masked), GENI_16 can be modified by software.	RW	0
15	GENI_15	f GENI_MASK_15 in GENI_MASK register is reset, GENI_15 is the value of C2C_Sscm_GenI_15 and cannot be modified by software. (signal is not masked) If GENI_MASK_15 is set (signal is masked), GENI_15 can be modified by software.	RW	0
14	GENI_14	f GENI_MASK_14 in GENI_MASK register is reset, GENI_14 is the value of C2C_Sscm_GenI_14 and cannot be modified by software. (signal is not masked) If GENI_MASK_14 is set (signal is masked), GENI_14 can be modified by software.	RW	0

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Bits	Field Name	Description	Type	Reset
13	GENI_13	f GENI_MASK_13 in GENI_MASK register is reset, GENI_13 is the value of C2C_Sscm_GenI_13 and cannot be modified by software. (signal is not masked) If GENI_MASK_13 is set (signal is masked), GENI_13 can be modified by software.	RW	0
12	GENI_12	f GENI_MASK_12 in GENI_MASK register is reset, GENI_12 is the value of C2C_Sscm_GenI_12 and cannot be modified by software. (signal is not masked) If GENI_MASK_12 is set (signal is masked), GENI_12 can be modified by software.	RW	0
11	GENI_11	f GENI_MASK_11 in GENI_MASK register is reset, GENI_11 is the value of C2C_Sscm_GenI_11 and cannot be modified by software. (signal is not masked) If GENI_MASK_11 is set (signal is masked), GENI_11 can be modified by software.	RW	0
10	GENI_10	f GENI_MASK_10 in GENI_MASK register is reset, GENI_10 is the value of C2C_Sscm_GenI_10 and cannot be modified by software. (signal is not masked) If GENI_MASK_10 is set (signal is masked), GENI_10 can be modified by software.	RW	0
9	GENI_9	f GENI_MASK_9 in GENI_MASK register is reset, GENI_9 is the value of C2C_Sscm_GenI_9 and cannot be modified by software. (signal is not masked) If GENI_MASK_9 is set (signal is masked), GENI_9 can be modified by software.	RW	0
8	GENI_8	f GENI_MASK_8 in GENI_MASK register is reset, GENI_8 is the value of C2C_Sscm_GenI_8 and cannot be modified by software. (signal is not masked) If GENI_MASK_8 is set (signal is masked), GENI_8 can be modified by software.	RW	0
7	GENI_7	f GENI_MASK_7 in GENI_MASK register is reset, GENI_7 is the value of C2C_Sscm_GenI_7 and cannot be modified by software. (signal is not masked) If GENI_MASK_7 is set (signal is masked), GENI_7 can be modified by software.	RW	0
6	GENI_6	f GENI_MASK_6 in GENI_MASK register is reset, GENI_6 is the value of C2C_Sscm_GenI_6 and cannot be modified by software. (signal is not masked) If GENI_MASK_6 is set (signal is masked), GENI_6 can be modified by software.	RW	0
5	GENI_5	f GENI_MASK_5 in GENI_MASK register is reset, GENI_5 is the value of C2C_Sscm_GenI_5 and cannot be modified by software. (signal is not masked) If GENI_MASK_5 is set (signal is masked), GENI_5 can be modified by software.	RW	0
4	GENI_4	f GENI_MASK_4 in GENI_MASK register is reset, GENI_4 is the value of C2C_Sscm_GenI_4 and cannot be modified by software. (signal is not masked) If GENI_MASK_4 is set (signal is masked), GENI_4 can be modified by software.	RW	0
3	GENI_3	f GENI_MASK_3 in GENI_MASK register is reset, GENI_3 is the value of C2C_Sscm_GenI_3 and cannot be modified by software. (signal is not masked) If GENI_MASK_3 is set (signal is masked), GENI_3 can be modified by software.	RW	0
2	GENI_2	f GENI_MASK_2 in GENI_MASK register is reset, GENI_2 is the value of C2C_Sscm_GenI_2 and cannot be modified by software. (signal is not masked) If GENI_MASK_2 is set (signal is masked), GENI_2 can be modified by software.	RW	0
1	GENI_1	f GENI_MASK_1 in GENI_MASK register is reset, GENI_1 is the value of C2C_Sscm_GenI_1 and cannot be modified by software. (signal is not masked) If GENI_MASK_1 is set (signal is masked), GENI_1 can be modified by software.	RW	0

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Bits	Field Name	Description	Type	Reset
0	GENI_0	f GENI_MASK_0 in GENI_MASK register is reset, GENI_0 is the value of C2C_Sscm_GenI_0 and cannot be modified by software. (signal is not masked) If GENI_MASK_0 is set (signal is masked), GENI_0 can be modified by software.	RW	0

Table 14-126. Register Call Summary for Register C2C_GENI_CONTROL

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- C2C Register Summary: [0]

Table 14-127. C2C_GENI_MASK

Address Offset	0x0000 0074		
Physical Address	0x5C000074	**Instance**	C2C
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GENI_MASK_31	GENI_MASK_30	GENI_MASK_29	GENI_MASK_28	GENI_MASK_27	GENI_MASK_26	GENI_MASK_25	GENI_MASK_24	GENI_MASK_23	GENI_MASK_22	GENI_MASK_21	GENI_MASK_20	GENI_MASK_19	GENI_MASK_18	GENI_MASK_17	GENI_MASK_16	GENI_MASK_15	GENI_MASK_14	GENI_MASK_13	GENI_MASK_12	GENI_MASK_11	GENI_MASK_10	GENI_MASK_9	GENI_MASK_8	GENI_MASK_7	GENI_MASK_6	GENI_MASK_5	GENI_MASK_4	GENI_MASK_3	GENI_MASK_2	GENI_MASK_1	GENI_MASK_0

Bits	Field Name	Description	Type	Reset
31	GENI_MASK_31	If GENI_MASK_31 is reset, C2C_Sscm_GenI_31 signal is not masked If GENI_MASK_31 is set, signal is masked.	RW	0
30	GENI_MASK_30	If GENI_MASK_30 is reset, C2C_Sscm_GenI_30 signal is not masked If GENI_MASK_30 is set, signal is masked.	RW	0
29	GENI_MASK_29	If GENI_MASK_29 is reset, C2C_Sscm_GenI_29 signal is not masked If GENI_MASK_29 is set, signal is masked.	RW	0
28	GENI_MASK_28	If GENI_MASK_28 is reset, C2C_Sscm_GenI_28 signal is not masked If GENI_MASK_28 is set, signal is masked.	RW	0
27	GENI_MASK_27	If GENI_MASK_27 is reset, C2C_Sscm_GenI_27 signal is not masked If GENI_MASK_27 is set, signal is masked.	RW	0
26	GENI_MASK_26	If GENI_MASK_26 is reset, C2C_Sscm_GenI_26 signal is not masked If GENI_MASK_26 is set, signal is masked.	RW	0
25	GENI_MASK_25	If GENI_MASK_26 is reset, C2C_Sscm_GenI_25 signal is not masked If GENI_MASK_26 is set, signal is masked.	RW	0
24	GENI_MASK_24	If GENI_MASK_24 is reset, C2C_Sscm_GenI_24 signal is not masked If GENI_MASK_24 is set, signal is masked.	RW	0
23	GENI_MASK_23	If GENI_MASK_23 is reset, C2C_Sscm_GenI_23 signal is not masked If GENI_MASK_23 is set, signal is masked.	RW	0
22	GENI_MASK_22	If GENI_MASK_22 is reset, C2C_Sscm_GenI_22 signal is not masked If GENI_MASK_22 is set, signal is masked.	RW	0

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Bits	Field Name	Description	Type	Reset
21	GENI_MASK_21	If GENI_MASK_21 is reset, C2C_Sscm_GenI_21 signal is not masked If GENI_MASK_21 is set, signal is masked.	RW	0
20	GENI_MASK_20	If GENI_MASK_20 is reset, C2C_Sscm_GenI_20 signal is not masked If GENI_MASK_20 is set, signal is masked.	RW	0
19	GENI_MASK_19	If GENI_MASK_19 is reset, C2C_Sscm_GenI_19 signal is not masked If GENI_MASK_19 is set, signal is masked.	RW	0
18	GENI_MASK_18	If GENI_MASK_18 is reset, C2C_Sscm_GenI_18 signal is not masked If GENI_MASK_18 is set, signal is masked.	RW	0
17	GENI_MASK_17	If GENI_MASK_17 is reset, C2C_Sscm_GenI_17 signal is not masked If GENI_MASK_17 is set, signal is masked.	RW	0
16	GENI_MASK_16	If GENI_MASK_16 is reset, C2C_Sscm_GenI_16 signal is not masked If GENI_MASK_16 is set, signal is masked.	RW	0
15	GENI_MASK_15	If GENI_MASK_15 is reset, C2C_Sscm_GenI_15 signal is not masked If GENI_MASK_15 is set, signal is masked.	RW	0
14	GENI_MASK_14	If GENI_MASK_14 is reset, C2C_Sscm_GenI_14 signal is not masked If GENI_MASK_14 is set, signal is masked.	RW	0
13	GENI_MASK_13	If GENI_MASK_13 is reset, C2C_Sscm_GenI_13 signal is not masked If GENI_MASK_13 is set, signal is masked.	RW	0
12	GENI_MASK_12	If GENI_MASK_12is reset, C2C_Sscm_GenI_12 signal is not masked If GENI_MASK_12 is set, signal is masked.	RW	0
11	GENI_MASK_11	If GENI_MASK_11 is reset, C2C_Sscm_GenI_11 signal is not masked If GENI_MASK_11 is set, signal is masked.	RW	0
10	GENI_MASK_10	If GENI_MASK_10 is reset, C2C_Sscm_GenI_10 signal is not masked If GENI_MASK_10 is set, signal is masked.	RW	0
9	GENI_MASK_9	If GENI_MASK_9 is reset, C2C_Sscm_GenI_9 signal is not masked If GENI_MASK_9 is set, signal is masked.	RW	0
8	GENI_MASK_8	If GENI_MASK_8 is reset, C2C_Sscm_GenI_8 signal is not masked If GENI_MASK_8 is set, signal is masked.	RW	0
7	GENI_MASK_7	If GENI_MASK_7 is reset, C2C_Sscm_GenI_7 signal is not masked If GENI_MASK_7 is set, signal is masked.	RW	0
6	GENI_MASK_6	If GENI_MASK_6 is reset, C2C_Sscm_GenI_6 signal is not masked If GENI_MASK_6 is set, signal is masked.	RW	0
5	GENI_MASK_5	If GENI_MASK_5 is reset, C2C_Sscm_GenI_5 signal is not masked If GENI_MASK_5 is set, signal is masked.	RW	0
4	GENI_MASK_4	If GENI_MASK_4 is reset, C2C_Sscm_GenI_4 signal is not masked If GENI_MASK_4 is set, signal is masked.	RW	0
3	GENI_MASK_3	If GENI_MASK_3 is reset, C2C_Sscm_GenI_3 signal is not masked If GENI_MASK_3 is set, signal is masked.	RW	0
2	GENI_MASK_2	If GENI_MASK_2 is reset, C2C_Sscm_GenI_2 signal is not masked If GENI_MASK_2 is set, signal is masked.	RW	0
1	GENI_MASK_1	If GENI_MASK_1 is reset, C2C_Sscm_GenI_1 signal is not masked If GENI_MASK_1 is set, signal is masked.	RW	0
0	GENI_MASK_0	If GENI_MASK_0 is reset, C2C_Sscm_GenI_0 signal is not masked If GENI_MASK_0 is set, signal is masked.	RW	0

Table 14-128. Register Call Summary for Register C2C_GENI_MASK

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- C2C Register Summary: [0]

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Table 14-129. C2C_GENO_STATUS

Address Offset	0x0000 0080		
Physical Address	0x5C000080	**Instance**	C2C
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GENO_31	GENO_30	GENO_29	GENO_28	GENO_27	GENO_26	GENO_25	GENO_24	GENO_23	GENO_22	GENO_21	GENO_20	GENO_19	GENO_18	GENO_17	GENO_16	GENO_15	GENO_14	GENO_13	GENO_12	GENO_11	GENO_10	GENO_9	GENO_8	GENO_7	GENO_6	GENO_5	GENO_4	GENO_3	GENO_2	GENO_1	GENO_0

Bits	Field Name	Description	Type	Reset
31	GENO_31	GENO_31 is the value of C2C_Sscm_GenO_31 signal.	RW	0
30	GENO_30	GENO_30 is the value of C2C_Sscm_GenO_30 signal.	RW	0
29	GENO_29	GENO_29 is the value of C2C_Sscm_GenO_29 signal.	RW	0
28	GENO_28	GENO_28 is the value of C2C_Sscm_GenO_28 signal.	RW	0
27	GENO_27	GENO_27 is the value of C2C_Sscm_GenO_27 signal.	RW	0
26	GENO_26	GENO_26 is the value of C2C_Sscm_GenO_26 signal.	RW	0
25	GENO_25	GENO_25 is the value of C2C_Sscm_GenO_25 signal.	RW	0
24	GENO_24	GENO_24 is the value of C2C_Sscm_GenO_24 signal.	RW	0
23	GENO_23	GENO_23 is the value of C2C_Sscm_GenO_23 signal.	RW	0
22	GENO_22	GENO_22 is the value of C2C_Sscm_GenO_22 signal.	RW	0
21	GENO_21	GENO_21 is the value of C2C_Sscm_GenO_21 signal.	RW	0
20	GENO_20	GENO_20 is the value of C2C_Sscm_GenO_20 signal.	RW	0
19	GENO_19	GENO_19 is the value of C2C_Sscm_GenO_19 signal.	RW	0
18	GENO_18	GENO_18 is the value of C2C_Sscm_GenO_18 signal.	RW	0
17	GENO_17	GENO_17 is the value of C2C_Sscm_GenO_17 signal.	RW	0
16	GENO_16	GENO_16 is the value of C2C_Sscm_GenO_16 signal.	RW	0
15	GENO_15	GENO_15 is the value of C2C_Sscm_GenO_15 signal.	RW	0
14	GENO_14	GENO_14 is the value of C2C_Sscm_GenO_14 signal.	RW	0
13	GENO_13	GENO_13 is the value of C2C_Sscm_GenO_13 signal.	RW	0
12	GENO_12	GENO_12 is the value of C2C_Sscm_GenO_12 signal.	RW	0
11	GENO_11	GENO_11 is the value of C2C_Sscm_GenO_11 signal.	RW	0
10	GENO_10	GENO_10 is the value of C2C_Sscm_GenO_10 signal.	RW	0
9	GENO_9	GENO_9 is the value of C2C_Sscm_GenO_9 signal.	RW	0
8	GENO_8	GENO_8 is the value of C2C_Sscm_GenO_8 signal.	RW	0
7	GENO_7	GENO_7 is the value of C2C_Sscm_GenO_7 signal.	RW	0
6	GENO_6	GENO_6 is the value of C2C_Sscm_GenO_6 signal.	RW	0
5	GENO_5	GENO_5 is the value of C2C_Sscm_GenO_5 signal.	RW	0
4	GENO_4	GENO_4 is the value of C2C_Sscm_GenO_4 signal.	RW	0
3	GENO_3	GENO_3 is the value of C2C_Sscm_GenO_3 signal.	RW	0
2	GENO_2	GENO_2 is the value of C2C_Sscm_GenO_2 signal.	RW	0
1	GENO_1	GENO_1 is the value of C2C_Sscm_GenO_1 signal.	RW	0
0	GENO_0	GENO_0 is the value of C2C_Sscm_GenO_0 signal.	RW	0

Table 14-130. Register Call Summary for Register C2C_GENO_STATUS

C2C Register Manual

- C2C Register Summary: [0]

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Table 14-131. C2C_GENO_INTERRUPT

Address Offset	0x0000 0084		
Physical Address	0x5C000084	**Instance**	C2C
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GENO_INT_31	GENO_INT_30	GENO_INT_29	GENO_INT_28	GENO_INT_27	GENO_INT_26	GENO_INT_25	GENO_INT_24	GENO_INT_23	GENO_INT_22	GENO_INT_21	GENO_INT_20	GENO_INT_19	GENO_INT_18	GENO_INT_17	GENO_INT_16	GENO_INT_15	GENO_INT_14	GENO_INT_13	GENO_INT_12	GENO_INT_11	GENO_INT_10	GENO_INT_9	GENO_INT_8	GENO_INT_7	GENO_INT_6	GENO_INT_5	GENO_INT_4	GENO_INT_3	GENO_INT_2	GENO_INT_1	GENO_INT_0

Bits	Field Name	Description	Type	Reset
31	GENO_INT_31	If GENO_INT_31=0, GENO_IRQ_31=1 when GENO_31 toggles; If GENO_INT_31=1: IF GENO_LEVEL_31=0, GENO_IRQ_31 =1 when GENO_31 toggles to 0. IF GENO_LEVEL_31=1, GENO_IRQ_31 =1 when GENO_31 toggles to 1.	RW	0
30	GENO_INT_30	If GENO_INT_30=0, GENO_IRQ_30=1 when GENO_30 toggles; If GENO_INT_30=1: IF GENO_LEVEL_30=0, GENO_IRQ_30 =1 when GENO_30 toggles to 0. IF GENO_LEVEL_30=1, GENO_IRQ_30 =1 when GENO_30 toggles to 1.	RW	0
29	GENO_INT_29	If GENO_INT_29=0, GENO_IRQ_29=1 when GENO_29 toggles; If GENO_INT_29=1: IF GENO_LEVEL_29=0, GENO_IRQ_29 =1 when GENO_29 toggles to 0. IF GENO_LEVEL_29=1, GENO_IRQ_29 =1 when GENO_29 toggles to 1.	RW	0
28	GENO_INT_28	If GENO_INT_28=0, GENO_IRQ_28=1 when GENO_28 toggles; If GENO_INT_28=1: IF GENO_LEVEL_28=0, GENO_IRQ_28 =1 when GENO_28 toggles to 0. IF GENO_LEVEL_28=1, GENO_IRQ_28 =1 when GENO_28 toggles to 1.	RW	0
27	GENO_INT_27	If GENO_INT_27=0, GENO_IRQ_27=1 when GENO_27 toggles; If GENO_INT_27=1: IF GENO_LEVEL_27=0, GENO_IRQ_27 =1 when GENO_27 toggles to 0. IF GENO_LEVEL_27=1, GENO_IRQ_27 =1 when GENO_27 toggles to 1.	RW	0
26	GENO_INT_26	If GENO_INT_26=0, GENO_IRQ_26=1 when GENO_26 toggles; If GENO_INT_26=1: IF GENO_LEVEL_26=0, GENO_IRQ_26 =1 when GENO_26 toggles to 0. IF GENO_LEVEL_26=1, GENO_IRQ_26 =1 when GENO_26 toggles to 1.	RW	0
25	GENO_INT_25	If GENO_INT_25=0, GENO_IRQ_25=1 when GENO_25 toggles; If GENO_INT_25=1: IF GENO_LEVEL_25=0, GENO_IRQ_25 =1 when GENO_25 toggles to 0. IF GENO_LEVEL_25=1, GENO_IRQ_25 =1 when GENO_25 toggles to 1.	RW	0
24	GENO_INT_24	If GENO_INT_24=0, GENO_IRQ_24=1 when GENO_24 toggles; If GENO_INT_24=1: IF GENO_LEVEL_24=0, GENO_IRQ_24 =1 when GENO_24 toggles to 0. IF GENO_LEVEL_24=1, GENO_IRQ_24 =1 when GENO_24 toggles to 1.	RW	0
23	GENO_INT_23	If GENO_INT_23=0, GENO_IRQ_23=1 when GENO_23 toggles; If GENO_INT_23=1: IF GENO_LEVEL_23=0, GENO_IRQ_23 =1 when GENO_23 toggles to 0. IF GENO_LEVEL_23=1, GENO_IRQ_23 =1 when GENO_23 toggles to 1.	RW	0

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Bits	Field Name	Description	Type	Reset
22	GENO_INT_22	If GENO_INT_22=0, GENO_IRQ_22=1 when GENO_22 toggles; If GENO_INT_22=1: IF GENO_LEVEL_22=0, GENO_IRQ_22 =1 when GENO_22 toggles to 0. IF GENO_LEVEL_22=1, GENO_IRQ_22 =1 when GENO_22 toggles to 1.	RW	0
21	GENO_INT_21	If GENO_INT_21=0, GENO_IRQ_21=1 when GENO_21 toggles; If GENO_INT_21=1: IF GENO_LEVEL_21=0, GENO_IRQ_21 =1 when GENO_21 toggles to 0. IF GENO_LEVEL_21=1, GENO_IRQ_21 =1 when GENO_21 toggles to 1.	RW	0
20	GENO_INT_20	If GENO_INT_20=0, GENO_IRQ_20=1 when GENO_20 toggles; If GENO_INT_20=1: IF GENO_LEVEL_20=0, GENO_IRQ_20 =1 when GENO_20 toggles to 0. IF GENO_LEVEL_20=1, GENO_IRQ_20 =1 when GENO_20 toggles to 1.	RW	0
19	GENO_INT_19	If GENO_INT_19=0, GENO_IRQ_19=1 when GENO_19 toggles; If GENO_INT_19=1: IF GENO_LEVEL_19=0, GENO_IRQ_19 =1 when GENO_19 toggles to 0. IF GENO_LEVEL_19=1, GENO_IRQ_19 =1 when GENO_19 toggles to 1.	RW	0
18	GENO_INT_18	If GENO_INT_18=0, GENO_IRQ_18=1 when GENO_18 toggles; If GENO_INT_18=1: IF GENO_LEVEL_18=0, GENO_IRQ_18 =1 when GENO_18 toggles to 0. IF GENO_LEVEL_18=1, GENO_IRQ_18 =1 when GENO_18 toggles to 1.	RW	0
17	GENO_INT_17	If GENO_INT_17=0, GENO_IRQ_17=1 when GENO_17 toggles; If GENO_INT_17=1: IF GENO_LEVEL_17=0, GENO_IRQ_17 =1 when GENO_17 toggles to 0. IF GENO_LEVEL_17=1, GENO_IRQ_17 =1 when GENO_17 toggles to 1.	RW	0
16	GENO_INT_16	If GENO_INT_16=0, GENO_IRQ_16=1 when GENO_16 toggles; If GENO_INT_16=1: IF GENO_LEVEL_16=0, GENO_IRQ_16 =1 when GENO_16 toggles to 0. IF GENO_LEVEL_16=1, GENO_IRQ_16 =1 when GENO_16 toggles to 1.	RW	0
15	GENO_INT_15	If GENO_INT_15=0, GENO_IRQ_15=1 when GENO_15 toggles; If GENO_INT_15=1: IF GENO_LEVEL_15=0, GENO_IRQ_15 =1 when GENO_15 toggles to 0. IF GENO_LEVEL_15=1, GENO_IRQ_15 =1 when GENO_15 toggles to 1.	RW	0
14	GENO_INT_14	If GENO_INT_14=0, GENO_IRQ_14=1 when GENO_14 toggles; If GENO_INT_14=1: IF GENO_LEVEL_14=0, GENO_IRQ_14 =1 when GENO_14 toggles to 0. IF GENO_LEVEL_14=1, GENO_IRQ_14 =1 when GENO_14 toggles to 1.	RW	0
13	GENO_INT_13	If GENO_INT_13=0, GENO_IRQ_13=1 when GENO_13 toggles; If GENO_INT_13=1: IF GENO_LEVEL_13=0, GENO_IRQ_13 =1 when GENO_13 toggles to 0. IF GENO_LEVEL_13=1, GENO_IRQ_13 =1 when GENO_13 toggles to 1.	RW	0
12	GENO_INT_12	If GENO_INT_12=0, GENO_IRQ_12=1 when GENO_12 toggles; If GENO_INT_12=1: IF GENO_LEVEL_12=0, GENO_IRQ_12 =1 when GENO_12 toggles to 0. IF GENO_LEVEL_12=1, GENO_IRQ_12 =1 when GENO_12 toggles to 1.	RW	0
11	GENO_INT_11	If GENO_INT_11=0, GENO_IRQ_11=1 when GENO_11 toggles; If GENO_INT_11=1: IF GENO_LEVEL_11=0, GENO_IRQ_11 =1 when GENO_11 toggles to 0. IF GENO_LEVEL_11=1, GENO_IRQ_11 =1 when GENO_11 toggles to 1.	RW	0
10	GENO_INT_10	If GENO_INT_10=0, GENO_IRQ_10=1 when GENO_10 toggles; If GENO_INT_10=1: IF GENO_LEVEL_10=0, GENO_IRQ_10 =1 when GENO_10 toggles to 0. IF GENO_LEVEL_10=1, GENO_IRQ_10 =1 when GENO_10 toggles to 1.	RW	0

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Bits	Field Name	Description	Type	Reset
9	GENO_INT_9	If GENO_INT_9=0, GENO_IRQ_9=1 when GENO_9 toggles; If GENO_INT_9=1: IF GENO_LEVEL_9=0, GENO_IRQ_9 =1 when GENO_9 toggles to 0. IF GENO_LEVEL_9=1, GENO_IRQ_9 =1 when GENO_9 toggles to 1.	RW	0
8	GENO_INT_8	If GENO_INT_8=0, GENO_IRQ_8=1 when GENO_8 toggles; If GENO_INT_8=1: IF GENO_LEVEL_8=0, GENO_IRQ_8 =1 when GENO_8 toggles to 0. IF GENO_LEVEL_8=1, GENO_IRQ_8 =1 when GENO_8 toggles to 1.	RW	0
7	GENO_INT_7	If GENO_INT_7=0, GENO_IRQ_7=1 when GENO_7 toggles; If GENO_INT_7=1: IF GENO_LEVEL_7=0, GENO_IRQ_7 =1 when GENO_7 toggles to 0. IF GENO_LEVEL_7=1, GENO_IRQ_7 =1 when GENO_7 toggles to 1.	RW	0
6	GENO_INT_6	If GENO_INT_6=0, GENO_IRQ_6=1 when GENO_6 toggles; If GENO_INT_6=1: IF GENO_LEVEL_6=0, GENO_IRQ_6 =1 when GENO_6 toggles to 0. IF GENO_LEVEL_6=1, GENO_IRQ_6 =1 when GENO_6 toggles to 1.	RW	0
5	GENO_INT_5	If GENO_INT_5=0, GENO_IRQ_5=1 when GENO_5 toggles; If GENO_INT_5=1: IF GENO_LEVEL_5=0, GENO_IRQ_5 =1 when GENO_5 toggles to 0. IF GENO_LEVEL_5=1, GENO_IRQ_5 =1 when GENO_5 toggles to 1.	RW	0
4	GENO_INT_4	If GENO_INT_4=0, GENO_IRQ_4=1 when GENO_4 toggles; If GENO_INT_4=1: IF GENO_LEVEL_4=0, GENO_IRQ_4 =1 when GENO_4 toggles to 0. IF GENO_LEVEL_4=1, GENO_IRQ_4 =1 when GENO_4 toggles to 1.	RW	0
3	GENO_INT_3	If GENO_INT_3=0, GENO_IRQ_3=1 when GENO_3 toggles; If GENO_INT_3=1: IF GENO_LEVEL_3=0, GENO_IRQ_3 =1 when GENO_3 toggles to 0. IF GENO_LEVEL_3=1, GENO_IRQ_3 =1 when GENO_3 toggles to 1.	RW	0
2	GENO_INT_2	If GENO_INT_2=0, GENO_IRQ_2=1 when GENO_2 toggles; If GENO_INT_2=1: IF GENO_LEVEL_2=0, GENO_IRQ_2 =1 when GENO_2 toggles to 0. IF GENO_LEVEL_2=1, GENO_IRQ_2 =1 when GENO_2 toggles to 1.	RW	0
1	GENO_INT_1	If GENO_INT_1=0, GENO_IRQ_1=1 when GENO_1 toggles; If GENO_INT_1=1: IF GENO_LEVEL_1=0, GENO_IRQ_1 =1 when GENO_1 toggles to 0. IF GENO_LEVEL_1=1, GENO_IRQ_1 =1 when GENO_1 toggles to 1.	RW	0
0	GENO_INT_0	If GENO_INT_0=0, GENO_IRQ_0=1 when GENO_0 toggles; If GENO_INT_0=1: IF GENO_LEVEL_0=0, GENO_IRQ_0 =1 when GENO_0 toggles to 0. IF GENO_LEVEL_0=1, GENO_IRQ_0 =1 when GENO_0 toggles to 1.	RW	0

Table 14-132. Register Call Summary for Register C2C_GENO_INTERRUPT

C2C Register Manual

- C2C Register Summary: [0]

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Table 14-133. C2C_GENO_LEVEL

Address Offset	0x0000 0088		
Physical Address	0x5C000088	**Instance**	C2C
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GENO_LEVEL_31	GENO_LEVEL_30	GENO_LEVEL_29	GENO_LEVEL_28	GENO_LEVEL_27	GENO_LEVEL_26	GENO_LEVEL_25	GENO_LEVEL_24	GENO_LEVEL_23	GENO_LEVEL_22	GENO_LEVEL_21	GENO_LEVEL_20	GENO_LEVEL_19	GENO_LEVEL_18	GENO_LEVEL_17	GENO_LEVEL_16	GENO_LEVEL_15	GENO_LEVEL_14	GENO_LEVEL_13	GENO_LEVEL_12	GENO_LEVEL_11	GENO_LEVEL_10	GENO_LEVEL_9	GENO_LEVEL_8	GENO_LEVEL_7	GENO_LEVEL_6	GENO_LEVEL_5	GENO_LEVEL_4	GENO_LEVEL_3	GENO_LEVEL_2	GENO_LEVEL_1	GENO_LEVEL_0

Bits	Field Name	Description	Type	Reset
31	GENO_LEVEL_31	IF GENO_LEVEL_31=0, GENO_IRQ_31 =1 when GENO_31 toggles to 0. IF GENO_LEVEL_31=1, GENO_IRQ_31 =1 when GENO_31 toggles to 1.	RW	0
30	GENO_LEVEL_30	IF GENO_LEVEL_30=0, GENO_IRQ_30 =1 when GENO_30 toggles to 0. IF GENO_LEVEL_30=1, GENO_IRQ_30 =1 when GENO_30 toggles to 1.	RW	0
29	GENO_LEVEL_29	IF GENO_LEVEL_29=0, GENO_IRQ_29 =1 when GENO_29 toggles to 0. IF GENO_LEVEL_29=1, GENO_IRQ_29 =1 when GENO_29 toggles to 1.	RW	0
28	GENO_LEVEL_28	IF GENO_LEVEL_28=0, GENO_IRQ_28 =1 when GENO_28 toggles to 0. IF GENO_LEVEL_28=1, GENO_IRQ_28 =1 when GENO_28 toggles to 1.	RW	0
27	GENO_LEVEL_27	IF GENO_LEVEL_27=0, GENO_IRQ_27 =1 when GENO_27 toggles to 0. IF GENO_LEVEL_27=1, GENO_IRQ_27 =1 when GENO_27 toggles to 1.	RW	0
26	GENO_LEVEL_26	IF GENO_LEVEL_26=0, GENO_IRQ_26 =1 when GENO_26 toggles to 0. IF GENO_LEVEL_26=1, GENO_IRQ_26 =1 when GENO_26 toggles to 1.	RW	0
25	GENO_LEVEL_25	IF GENO_LEVEL_25=0, GENO_IRQ_25 =1 when GENO_25 toggles to 0. IF GENO_LEVEL_25=1, GENO_IRQ_25 =1 when GENO_25 toggles to 1.	RW	0
24	GENO_LEVEL_24	IF GENO_LEVEL_24=0, GENO_IRQ_24 =1 when GENO_24 toggles to 0. IF GENO_LEVEL_24=1, GENO_IRQ_24 =1 when GENO_24 toggles to 1.	RW	0
23	GENO_LEVEL_23	IF GENO_LEVEL_23=0, GENO_IRQ_23 =1 when GENO_23 toggles to 0. IF GENO_LEVEL_23=1, GENO_IRQ_23 =1 when GENO_23 toggles to 1.	RW	0
22	GENO_LEVEL_22	IF GENO_LEVEL_22=0, GENO_IRQ_22 =1 when GENO_22 toggles to 0. IF GENO_LEVEL_22=1, GENO_IRQ_22 =1 when GENO_22 toggles to 1.	RW	0
21	GENO_LEVEL_21	IF GENO_LEVEL_21=0, GENO_IRQ_21 =1 when GENO_21 toggles to 0. IF GENO_LEVEL_21=1, GENO_IRQ_21 =1 when GENO_21 toggles to 1.	RW	0
20	GENO_LEVEL_20	IF GENO_LEVEL_20=0, GENO_IRQ_20 =1 when GENO_20 toggles to 0. IF GENO_LEVEL_20=1, GENO_IRQ_20 =1 when GENO_20 toggles to 1.	RW	0
19	GENO_LEVEL_19	IF GENO_LEVEL_19=0, GENO_IRQ_19 =1 when GENO_19 toggles to 0. IF GENO_LEVEL_19=1, GENO_IRQ_19 =1 when GENO_19 toggles to 1.	RW	0
18	GENO_LEVEL_18	IF GENO_LEVEL_18=0, GENO_IRQ_18 =1 when GENO_18 toggles to 0. IF GENO_LEVEL_18=1, GENO_IRQ_18 =1 when GENO_18 toggles to 1.	RW	0

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Bits	Field Name	Description	Type	Reset
17	GENO_LEVEL_17	IF GENO_LEVEL_17=0, GENO_IRQ_17 =1 when GENO_17 toggles to 0. IF GENO_LEVEL_17=1, GENO_IRQ_17 =1 when GENO_17 toggles to 1.	RW	0
16	GENO_LEVEL_16	IF GENO_LEVEL_16=0, GENO_IRQ_16 =1 when GENO_16 toggles to 0. IF GENO_LEVEL_16=1, GENO_IRQ_16 =1 when GENO_16 toggles to 1.	RW	0
15	GENO_LEVEL_15	IF GENO_LEVEL_15=0, GENO_IRQ_15 =1 when GENO_15 toggles to 0. IF GENO_LEVEL_15=1, GENO_IRQ_15 =1 when GENO_15 toggles to 1.	RW	0
14	GENO_LEVEL_14	IF GENO_LEVEL_14=0, GENO_IRQ_14 =1 when GENO_14 toggles to 0. IF GENO_LEVEL_14=1, GENO_IRQ_14 =1 when GENO_14 toggles to 1.	RW	0
13	GENO_LEVEL_13	IF GENO_LEVEL_13=0, GENO_IRQ_13 =1 when GENO_13 toggles to 0. IF GENO_LEVEL_13=1, GENO_IRQ_13 =1 when GENO_13 toggles to 1.	RW	0
12	GENO_LEVEL_12	IF GENO_LEVEL_12=0, GENO_IRQ_12 =1 when GENO_12 toggles to 0. IF GENO_LEVEL_12=1, GENO_IRQ_12 =1 when GENO_12 toggles to 1.	RW	0
11	GENO_LEVEL_11	IF GENO_LEVEL_11=0, GENO_IRQ_11 =1 when GENO_11 toggles to 0. IF GENO_LEVEL_11=1, GENO_IRQ_11 =1 when GENO_11 toggles to 1.	RW	0
10	GENO_LEVEL_10	IF GENO_LEVEL_10=0, GENO_IRQ_10 =1 when GENO_10 toggles to 0. IF GENO_LEVEL_10=1, GENO_IRQ_10 =1 when GENO_10 toggles to 1.	RW	0
9	GENO_LEVEL_9	IF GENO_LEVEL_9=0, GENO_IRQ_9 =1 when GENO_9 toggles to 0. IF GENO_LEVEL_9=1, GENO_IRQ_9 =1 when GENO_9 toggles to 1.	RW	0
8	GENO_LEVEL_8	IF GENO_LEVEL_8=0, GENO_IRQ_8 =1 when GENO_8 toggles to 0. IF GENO_LEVEL_8=1, GENO_IRQ_8 =1 when GENO_8 toggles to 1.	RW	0
7	GENO_LEVEL_7	IF GENO_LEVEL_7=0, GENO_IRQ_7 =1 when GENO_7 toggles to 0. IF GENO_LEVEL_7=1, GENO_IRQ_7 =1 when GENO_7 toggles to 1.	RW	0
6	GENO_LEVEL_6	IF GENO_LEVEL_6=0, GENO_IRQ_6 =1 when GENO_6 toggles to 0. IF GENO_LEVEL_6=1, GENO_IRQ_6 =1 when GENO_6 toggles to 1.	RW	0
5	GENO_LEVEL_5	IF GENO_LEVEL_5=0, GENO_IRQ_5 =1 when GENO_5 toggles to 0. IF GENO_LEVEL_5=1, GENO_IRQ_5 =1 when GENO_5 toggles to 1.	RW	0
4	GENO_LEVEL_4	IF GENO_LEVEL_4=0, GENO_IRQ_4 =1 when GENO_4 toggles to 0. IF GENO_LEVEL_4=1, GENO_IRQ_4 =1 when GENO_4 toggles to 1.	RW	0
3	GENO_LEVEL_3	IF GENO_LEVEL_3=0, GENO_IRQ_3 =1 when GENO_3 toggles to 0. IF GENO_LEVEL_3=1, GENO_IRQ_3 =1 when GENO_3 toggles to 1.	RW	0
2	GENO_LEVEL_2	IF GENO_LEVEL_2=0, GENO_IRQ_2 =1 when GENO_2 toggles to 0. IF GENO_LEVEL_2=1, GENO_IRQ_2 =1 when GENO_2 toggles to 1.	RW	0
1	GENO_LEVEL_1	IF GENO_LEVEL_1=0, GENO_IRQ_1 =1 when GENO_1 toggles to 0. IF GENO_LEVEL_1=1, GENO_IRQ_1 =1 when GENO_1 toggles to 1.	RW	0
0	GENO_LEVEL_0	IF GENO_LEVEL_0=0, GENO_IRQ_0 =1 when GENO_0 toggles to 0. IF GENO_LEVEL_0=1, GENO_IRQ_0 =1 when GENO_0 toggles to 1.	RW	0

Table 14-134. Register Call Summary for Register C2C_GENO_LEVEL

C2C Register Manual

- C2C Register Summary: [0]

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Memory Subsystem

This chapter introduces the memory subsystem of the device.

Topic **Page**

15.1 Memory Subsystem Overview 3010
15.2 Dynamic Memory Manager 3015
15.3 EMIF Controller 3095
15.4 General-Purpose Memory Controller 3169
15.5 Error Location Module 3308
15.6 On-Chip Memory (OCM) Subsystem 3335

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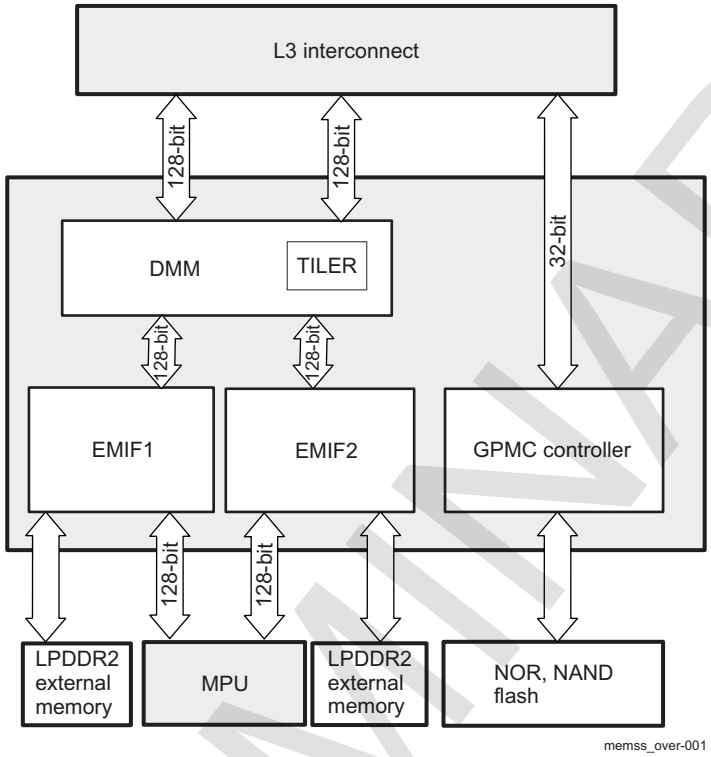
15.1 Memory Subsystem Overview

Figure 15-1 shows a functional diagram of all memory subsystems in the device.

Figure 15-1. Memory Subsystem Functional Diagram



15.1.1 DMM Overview

The dynamic memory manager (DMM) module is typically located immediately in front of the synchronous dynamic random access memory (SDRAM) controller (SDRC), as shown in Figure 15-1.

In a broad sense, the DMM manages various aspects of memory accesses such as:

- Initiator-indexed priority generation
- Multizone SDRAM interleaving configuration
- Block object transfer optimization – tiling
- Centralized low-latency page translation – MMU-like feature

The dynamic qualifier for memory management highlights the software configurability, and hence the runtime nature, of the four aspects of memory management handled by the DMM.

15.1.1.1 DMM Features

From a functional perspective, the role of the DMM is to:

- Add initiator-based priority to any incoming requests
- Perform to/from tiling conversions of tiled requests
- Make on-the-fly basic transforms, such as quadrant rotations and mirroring
- Optionally, provide a low-latency page-based translation to handle memory fragmentation – MMU
- Distribute the traffic on all attached memory controllers according to the interleaving configuration

The main features of the DMM are:

- Programmable multizone DRAM mapping and interleaving configuration
- Programmable initiator-based request priority extension

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- Multichannel memory transfer optimization
- Single SDRAM page request generation
- Low-latency interconnect port
- Page-grained address translation to manage memory fragmentation
- Automatic synchronized reloading of the address translation table

15.1.2 TILER Overview

The tiling and isometric lightweight engine for rotation (TILER) is a submodule of the DMM (see Figure 15-1) and is therefore described in Section 15.2, *Dynamic Memory Manager*.

The TILER is intended to improve bidimensional (tiled) block transfer efficiency. It is, therefore, a module aimed at:

- Primarily, efficient handling of 2-dimension (2D) data mapped in tiles, such as video or graphics macroblocks
- Optionally, managing the memory fragmentation and zero-copy physical frame-buffer swapping through a page-grained translation
- Making isometric (distance preserving) transforms, such as 90-, 180-, or 270-degree rotations, with a horizontal or vertical reflection

The lightweight qualifier of this engine highlights its limited support of isometric transforms, as:

- Rotation performs only basic quadrant rotations by some multiple of 90 degrees.
- Reflection is limited to horizontal and vertical flip.
- Translation is restricted to a 4-KB page granularity.

Written differently, the functionality of the TILER is to map a 2D virtually addressed interconnect request into one or more physically addressed interconnect requests by:

- Transforming the virtual address, data, and byte-enable to match the requested 0-, 90-, 180-, or 270-degree orientation in a tiled 2D addressing space
- Optionally, translating the oriented tiled address by a page-specific vector to manage memory fragmentation and physical object aliasing

15.1.2.1 TILER Features

The main features of the TILER are:

- Efficiency improvement of 2D block access on SDRAMs
- Optimized interlaced access on tiled frames
- 2D virtual-to-physical address translation of SDRAM bidimensional objects to handle rotation
- Page-grained address translation to manage memory fragmentation and physical buffer aliasing
- Unlimited number of 2D tiled objects supported in any (0, 90, 180, or 270 degrees) orientation
- Full bandwidth use by minimizing the size of raster-based initiator buffers
- Optimization of multichannel memory transfers
- Interconnect request granularity balance (in X and Y directions)

15.1.3 EMIF Overview

The extended memory interface (EMIF) module is typically located near the DMM module, as shown in Figure 15-1.

The EMIF provides connectivity between the device and LPDDR2-type memory. It manages data bus read/write accesses between external memories, the microprocessor unit (MPU), and the direct memory access (DMA) controller. It acts as the primary interface between SDRAM and all functional blocks, such as the ARM®, IVA-HD, imaging subsystem (ISS), GFX, and DMA controllers.

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15.1.3.1 Main Features

The EMIF has the following capabilities:

- Supports JEDEC standard-compliant LPDDR2-SDRAM (S2 and S4) and LPDDR2-NVM devices
- 2-GB SDRAM address range over two chip selects (CSs) (configurable with the DMM; see Section 15.2, *Dynamic Memory Manager*, for more information)
- Supports two independent CSs, with their corresponding register sets, and independent page tracking
- Both CSs must have the same memory type and size if they are both SDRAM or both nonvolatile memory (NVM). LPDDR2-SDRAM can be used in parallel with LPDDR2-NVM and can have a different size.
- Flexible address muxing scheme that permits choosing different bank-mapping allocation by configuring the bank, column, and row-address decoding ordering
- 16- or 32-bit data path to external SDRAM
- Supports LPDDR2 devices with 1, 2, 4, or 8 internal banks
- Supports the following data bus widths:
  - 128-bit level 3 (L3) interconnect data bus width
  - 16- and 32-bit SDRAM data bus width
- Supports the following CAS latencies: 3, 4, 5, 6, 7, and 8
- Supports 256-, 512-, 1024-, and 2048-word page sizes
- Supports the following burst lengths: 8
- Supports sequential burst type
- SDRAM auto-initialization from reset or configuration change
- Supports bank interleaving across both CSs if same memory type
- Supports self-refresh and precharge power-down modes for low power (per CS, manual entry/exit self-refresh, and deep power-down modes)
- Supports deep power-down mode for low power
- Supports partial array self-refresh and temperature-controlled self-refresh modes for low power. Temperature-controlled self-refresh is supported only for mobile SDRAM having an on-chip temperature sensor.
- Supports prioritized refresh
- Programmable SDRAM refresh rate and backlog counter
- Supports ZQ calibration
- Supports temperature monitoring

15.1.4 GPMC Overview

The general-purpose memory controller (GPMC) is an unified memory controller dedicated to interfacing external memory devices:

- Asynchronous SRAM-like memories and application-specific integrated circuit (ASIC) devices
- Asynchronous, synchronous, and page mode (available only in nonmuxed mode) burst NOR flash devices
- NAND flash
- Pseudo-SRAM devices

15.1.4.1 GPMC Features

The GPMC is the external memory controller of the device. The GPMC data access engine provides a flexible programming model for communication with all standard memories. The GPMC supports various accesses:

- Asynchronous read/write access
- Asynchronous read page access (4, 8, and 16 Word16)

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- Synchronous read/write access
- Synchronous read/write burst access without wrap capability (4, 8, and 16 Word16)
- Synchronous read/write burst access with wrap capability (4, 8, and 16 Word16)
- Address/data-multiplexed access
- Little- and big-endian access

The GPMC can communicate with a wide range of external devices:

- External asynchronous or synchronous 8-bit wide memory or device (nonburst device)
- External asynchronous or synchronous 16-bit wide memory or device
- External 16-bit nonmultiplexed device with limited address range (2KB)
- External 16-bit address/data-multiplexed NOR flash device
- External 8-bit and 16-bit NAND flash device
- External 16-bit pseudo-SRAM (pSRAM) device

The main features of the GPMC are:

- 8- or 16-bit-wide data path to external memory device
- Supports up to eight CS regions of programmable size and programmable base addresses in a total address space of 1GB
- Supports transactions controlled by a firewall
- On-the-fly error code detection using the Bose-ChaudhurI-Hocquenghem (BCH) (t = 4, 8, or 16) or Hamming code to improve the reliability of NAND with a minimum effect on software (NAND flash with 512-byte page size or greater)
- Fully pipelined operation for optimal memory bandwidth use
- External device clock provided from the L3 clock divided by 1, 2, 3, or 4
- Supports programmable autoclock gating when no access is detected
- Independent and programmable control signal timing parameters for setup and hold time on a per-chip basis. Parameters are set according to the memory device timing parameters, with a timing granularity of one L3 clock cycle.
- Flexible internal access time control (WAIT state) and flexible handshake mode using external WAIT pin monitoring
- Support bus keeping
- Support bus turnaround
- Prefetch and write posting engine associated with system DMA (sDMA) to achieve full performance from the AND device with minimum effect on NOR/SRAM concurrent access

NOTE: Page mode is available only in nonmultiplexed mode.

15.1.5 ELM Overview

NAND flash memories are dense and nonvolatile, but error-prone. Whenever NAND flash memories are read from, some level of error correction is required. In the case of NAND modules with no internal correction capability, sometimes referred to as bare NAND, the correction process is delegated to the memory controller.

The error location module (ELM) must be used in conjunction with the GPMC. The GPMC probes data read from an external NAND flash and uses them to compute checksum-like information, called syndrome polynomials, on a per-block basis. Each syndrome polynomial gives a status of the read operations for a full block, including 512 bytes of data, parity bits, and an optional spare area data field, with a maximum block size of 1023 bytes. Computation is based on the BCH algorithm. The ELM extracts error addresses from these syndrome polynomials.

Based on the syndrome polynomial value, the ELM can detect errors, compute the number of errors, and give the location of each error bit. The actual data is not required to complete the error correction algorithm. Errors can be reported anywhere in the NAND flash block, including in the parity bits.

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The maximum acceptable number of errors that can be corrected depends on a configuration parameter. Error correction levels of 4, 8, and 16 bits are supported. The ELM relies on a static definition of the generator polynomial for each error correction level that corresponds to the generator polynomials defined in the GPMC. A larger number of errors can be detected, but the ELM cannot correct them all. The offending block is then tagged as uncorrectable.

When the error location process completes, an interrupt is triggered to inform a central processing unit (CPU) that its status can be checked. The error locations for the NAND page can be retrieved from the module through register accesses.

15.1.5.1 ELM Features

The ELM features:

- 4, 8, and 16 bits per 512-byte block error location based on BCH algorithm
- Eight simultaneous processing contexts
- Page-based and continuous modes
- Interrupt generation when error location process completes:
  - When the full page has been processed in page mode
  - For each syndrome polynomial in continuous mode

15.1.6 OCM Overview

The on-chip memory (OCM) subsystem consists of the following OCM controllers: one connected to an on-chip ROM (SAR ROM), one connected to an on-chip RAM (SAR RAM), and one connected to an on-chip SRAM (L3 SRAM). Each memory controller has its own dedicated interface to the L3 interconnect.

15.1.6.1 SAR ROM

This on-chip ROM contains 4KB of memory and a linked list of descriptors used by sDMA during the restore context operation (when the device transitions from off to on mode).

The device-embedded SAR ROM has the following characteristics:

- 4-KB ROM
- 32-bit access per cycle
- Support for single- and burst-access transactions

15.1.6.2 SAR RAM

The on-chip SAR RAM contains 8KB and is mapped as four blocks with irregular region sizes. This memory content is preserved when the device goes into off mode (as long as the wake-up voltage domain remains supplied). It is used as context-saving memory to be written by software so that sDMA restores its saved content when the device transitions from off to on mode.

The device-embedded SAR RAM has the following characteristics:

- Support for single-access transactions
  - Operates at full L4-PER interconnect clock frequency
  - 32-bit access per cycle

15.1.6.3 L3 OCM_RAM

The on-chip L3 OCM_RAM contains 56KB of RAM, and partitioning is defined by the L3 firewall logic. The device-embedded L3 OCM_RAM has the following characteristics:

- Support for single and burst access transactions:
  - Operates at full L3 interconnect clock frequency
  - Fully pipelined, one 32-bit access per cycle
- Restricted access support

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15.2 Dynamic Memory Manager

15.2.1 DMM Overview

This section describes the dynamic memory manager (DMM) and its tiling and isometric lightweight engine for rotation (TILER) submodule.

The DMM is introduced in Section 15.1, *Memory Subsytem Overview* in Chapter 15, *Memory Subsystem*.

The function of the DMM is to:

- Add initiator-based priority to any incoming requests
- Perform to-and-from tiling conversions of tiled requests
- Make on-the-fly basic transforms, such as quadrant rotations and mirroring
- Optionally provide a low-latency page-based translation to handle memory fragmentation – memory management unit (MMU)
- Distribute the traffic on all attached memory controllers according to the interleaving configuration

The TILER is also introduced in Section 15.1, *Memory Subsystem Overview* in Chapter 15, *Memory Subsystem*.

The functions of the TILER are:

- Primary handling efficiently 2-dimensional (2D) data mapped in tiles, such as video or graphics macroblocks
- Optionally managing the memory fragmentation and zero-copy physical frame buffers swapping through a page-grained translation
- Allowing optimized interlaced accesses on tiled frames
- Making (distance preserving) transforms, such as 90-, 180-, or 270-degree rotations, with a horizontal or vertical reflection
- Interleaving the memory accesses among the two memory controllers (also called EMIF). For more information, see Section 15.3, *EMIF Controller*.

Figure 15-2 is an overview of the DMM and TILER in the device.

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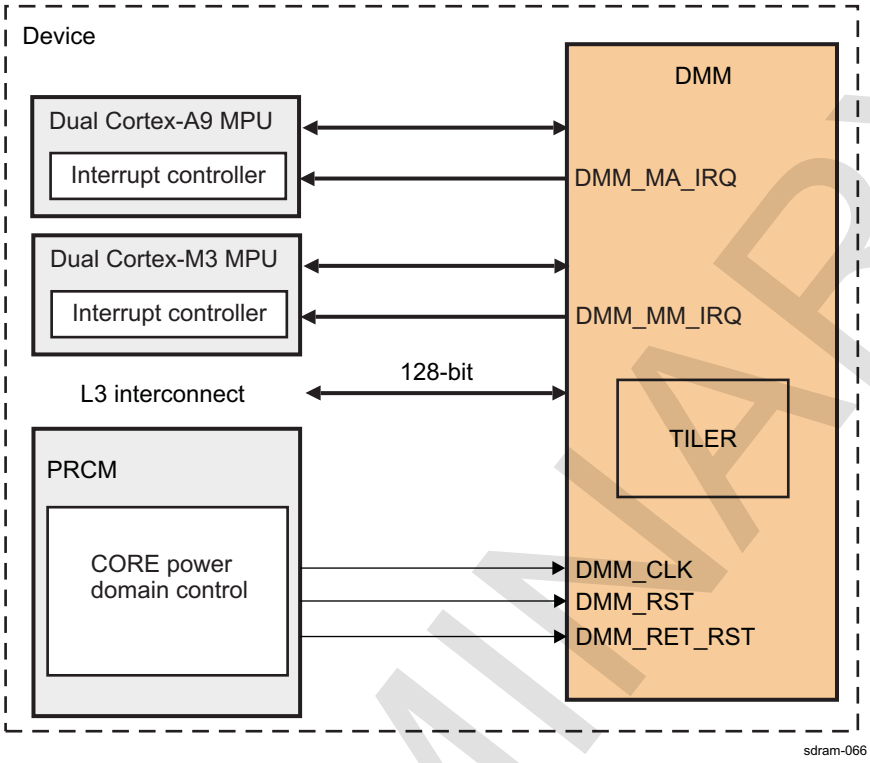
Figure 15-2. DMM and Tiler Overview



15.2.2 DMM Integration

This section describes module integration in the device, including information about clocks, resets, and hardware requests.

- IDLE hardware handshake (the DMM supports only smart-idle mode)
- No STANDBY hardware handshake
- No wake-up request
- No system direct memory access (sDMA) requests
- One interrupt line for interrupt request (IRQ)
- One functional clock

Figure 15-3 shows the integration of DMM in the device.

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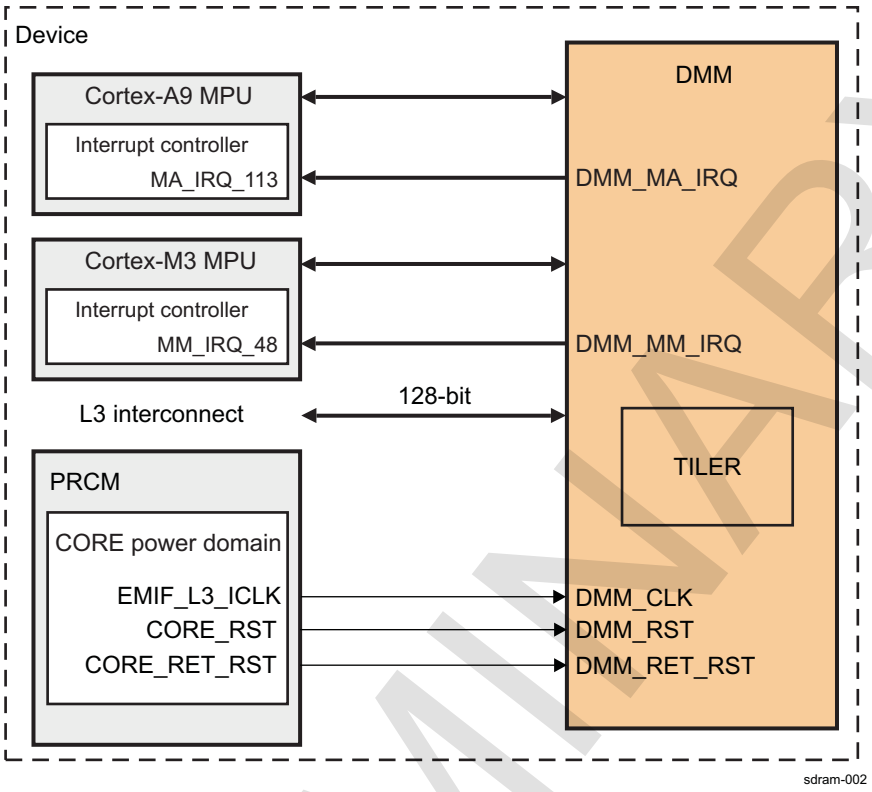
Figure 15-3. DMM Integration



NOTE: For more information about the IDLE hardware handshake, see Chapter 3, *Power, Reset, and Clock Management*.

Table 15-1 through Table 15-3 summarize the integration of DMM in the device.

Table 15-1. DMM Integration Attributes

Module Instance	Attributes		
	Power Domain	Wake-Up Capability	Interconnect
DMM	PD_CORE	No	N/A

Table 15-2. DMM Clocks and Resets

Clocks				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
DMM	DMM_CLK	EMIF_L3_ICLK	PRCM	DMM interface and functional clock. For information about power, reset, and clock management (PRCM) module clock gating and management, see Chapter 3, *Power, Reset, and Clock Management*.
Resets				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
DMM	DMM_RST	CORE_RST	PRCM	Functional reset. For information about PRCM reset sources and distribution, see Chapter 3, *Power, Reset, and Clock Management*.
DMM	DMM_RET_RST	CORE_RET_RST	PRCM	Reset for retention flip-flop (RFF) registers, namely: DMM_SYSCONFIG

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Table 15-2. DMM Clocks and Resets (continued)

				DMM_LISA_LOCK DMM_LISA_MAP_i DMM_TILER_OR0 DMM_TILER_OR1 DMM_PAT_VIEW0 DMM_PAT_VIEW1 DMM_PAT_VIEW_MAP_i DMM_PAT_VIEW_MAP_BASE DMM_PAT_DESCR_i DMM_PAT_AREA_i DMM_PAT_CTRL_i DMM_PAT_DATA_i DMM_PEG_PRIO_k DMM_PEG_PRIO_PAT For information about PRCM reset sources and distribution, see Chapter 3, *Power, Reset, and Clock Management*.

Table 15-3. Hardware Requests

Interrupt Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
DMM	DMM_MA_IRQ	MA_IRQ_113	Dual Cortex™-A9 MPU	DMM interrupt to the dual Cortex-A9 MPU subsystem
DMM	DMM_MM_IRQ	MM_IRQ_48	Dual Cortex™-M3 MPU	DMM interrupt to the dual Cortex-M3 MPU subsystem
No DMA Requests				

15.2.2.1 DMM Configuration

Table 15-4 lists all configured parameters for the DMM. These parameters are read-only.

Table 15-4. DMM TILER Container Geometry

Scope	Bit field	Configuration Value	Description
LISA	DMM_HWINFO[3:0] TILER_CNT	0x2	Two TILER instances in the DMM
	DMM_HWINFO[19:16] ROBIN_CNT	0x2	Two ROBIN instances in the DMM
	DMM_LISA_HWINFO[4:0] SECTION_CNT	0x2	Two DMM sections
	DMM_LISA_HWINFO[11:8] SDRC_CNT	0x2	Two SDRAM controllers (SDRCs) attached
TILER	DMM_TILER_HWINFO[6:0] OR_CNT	0x10	16 orientation entries
PAT	DMM_PAT_GEOMETRY[4:0] PAGE_SZ	0x0C	4-kiB page granularity
	DMM_PAT_GEOMETRY[19:16] CONT_WDTH	0x8	Container width of 256 pages
	DMM_PAT_GEOMETRY[26:24] CONT_HGHT	0x7	Container height of 128 pages
	DMM_PAT_GEOMETRY[13:8] ADDR_RANGE	0x10	2-GiB PAT output physical address range
	DMM_PAT_HWINFO[6:0] VIEW_CNT	0x10	16 view entries
	DMM_PAT_HWINFO[11:8] VIEW_MAP_CNT	0x4	Four view maps
	DMM_PAT_HWINFO[20:16] LUT_CNT	0x1	One PAT LUT
	DMM_PAT_HWINFO[28:24] ENGINE_CNT	0x2	Two PAT refill engines

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Table 15-4. DMM TILER Container Geometry (continued)

Scope	Bit field	Configuration Value	Description
PEG	DMM_PEG_HWINFO[6:0] PRIO_CNT	0x10	16 priority entries

15.2.3 DMM Functional Description

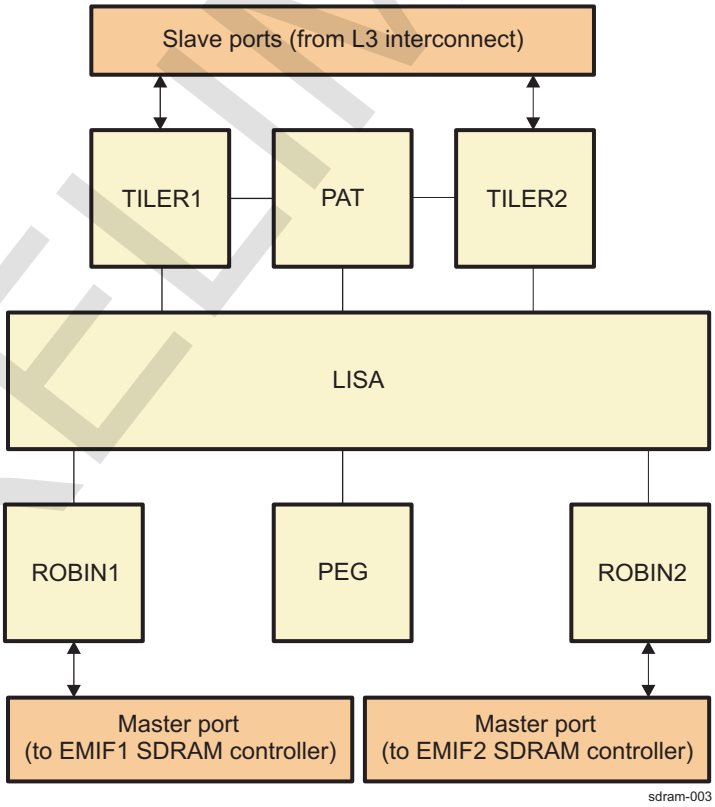
15.2.3.1 DMM Block Diagram

Figure 15-4 shows the DMM macro architecture. The DMM consists of six blocks:

- Two TILERs, each with its own interconnect slave port for converting requests back and forth between the input virtual addressing mode and the output physical tiledaddressing mode. The tiling conversions of requests, write data, and responses is performed entirely in the TILER blocks.
- Two reordering buffer and initiator nodes (ROBINs), each with its own interconnect master port to initiate requests to the SDRC and allow tiled data, tiled response, and split response reconstruction. The ROBIN block manages only the reordering buffer and performs data reordering due to the orientation.
- A physical address translator (PAT) for managing the memory fragmentation
- A priority extension generator (PEG) to generate priorities required by the SDRC; these priorities are not used in the DMM.
- A local interconnect and synchronization agent (LISA) to synchronize all DMM subsystems and provide access to their configuration registers

Figure 15-4 is a block diagram of the DMM.

Figure 15-4. DMM Block Diagram



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The interconnect must ensure that virtually addressed requests target only a TILER port.

15.2.3.2 DMM Clock Configuration

Table 15-5 describes the DMM clocks.

Table 15-5. DMM Clocks

Signal	I/O [1]	Description
DMM_CLK	I	Functional and interface clock

(1) I = Input; O = Output

The DMM is concerned with SDRC management and is in the MEMIF clock domain among the SDRCs. The DMM is a fully synchronous module, which uses the clock and clock-enable signals provided in the MEMIF clock domain to generate its interface and functional clocks.

To configure DMM_CLK control and settings, see Table 15-2.

15.2.3.3 DMM Power Management

DMM power is supplied by the CORE power domain, and DMM power management complies with system power-management guidelines.

Table 15-6 describes the power-management features available for the DMM module.

Table 15-6. DMM Local Power-Management Features

Feature	Registers	Description
Clock auto gating	N/A	Feature not available
Slave idle modes	DMM_SYSCONFIG[3:2] SIDLEMODE bit field	Only smart-idle wake-up mode is available.
Clock activity	N/A	Feature not available
Master standby modes	N/A	Feature not available
Global wake-up enable	N/A	Feature not available
Wake-up sources enable	N/A	Feature not available

Some of the DMM module registers are affected by the save-and-restore (SAR) mechanism. For more information about SAR, see Chapter 3, *Power, Reset, and Clock Management*.

15.2.3.4 DMM Interrupt Requests

Errors in PAT area refill registers are reported through the DMM_PAT_STATUS_i[15:10] ERROR bit field (see Table 15-7).

Table 15-7. DMM Hardware Status Features

Feature	Type	Register	Description
PAT error flags	Read-only	DMM_PAT_STATUS_i[15:10] ERROR (i = 0 to 3)	Unexpected update of the PAT area refill registers

Table 15-8 lists the event flags, and their masks, that can cause module interrupts.

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Table 15-8. Events

Interrupt	Event Flag	Event Mask
ERR_LUT_MISS3	DMM_PAT_IRQSTATUS[31] EVENT0 DMM_PAT_IRQSTATUS_RAW[31] EVENT0	DMM_PAT_IRQENABLE_SET[31] EVENT0 DMM_PAT_IRQENABLE_CLR[31] EVENT0
ERR_UPD_DATA3	DMM_PAT_IRQSTATUS[30] EVENT0 DMM_PAT_IRQSTATUS_RAW[30] EVENT0	DMM_PAT_IRQENABLE_SET[30] EVENT0 DMM_PAT_IRQENABLE_CLR[30] EVENT0
ERR_UPD_CTRL3	DMM_PAT_IRQSTATUS[29] EVENT0 DMM_PAT_IRQSTATUS_RAW[29] EVENT0	DMM_PAT_IRQENABLE_SET[29] EVENT0 DMM_PAT_IRQENABLE_CLR[29] EVENT0
ERR_UPD_AREA3	DMM_PAT_IRQSTATUS[28] EVENT0 DMM_PAT_IRQSTATUS_RAW[28] EVENT0	DMM_PAT_IRQENABLE_SET[28] EVENT0 DMM_PAT_IRQENABLE_CLR[28] EVENT0
ERR_INV_DATA3	DMM_PAT_IRQSTATUS[27] EVENT0 DMM_PAT_IRQSTATUS_RAW[27] EVENT0	DMM_PAT_IRQENABLE_SET[27] EVENT0 DMM_PAT_IRQENABLE_CLR[27] EVENT0
ERR_INV_DSC3	DMM_PAT_IRQSTATUS[26] EVENT0 DMM_PAT_IRQSTATUS_RAW[26] EVENT0	DMM_PAT_IRQENABLE_SET[26] EVENT0 DMM_PAT_IRQENABLE_CLR[26] EVENT0
FILL_LST3	DMM_PAT_IRQSTATUS[25] EVENT0 DMM_PAT_IRQSTATUS_RAW[25] EVENT0	DMM_PAT_IRQENABLE_SET[25] EVENT0 DMM_PAT_IRQENABLE_CLR[25] EVENT0
FILL_DSC3	DMM_PAT_IRQSTATUS[24] EVENT0 DMM_PAT_IRQSTATUS_RAW[24] EVENT0	DMM_PAT_IRQENABLE_SET[24] EVENT0 DMM_PAT_IRQENABLE_CLR[24] EVENT0
ERR_LUT_MISS2	DMM_PAT_IRQSTATUS[23] EVENT0 DMM_PAT_IRQSTATUS_RAW[23] EVENT0	DMM_PAT_IRQENABLE_SET[23] EVENT0 DMM_PAT_IRQENABLE_CLR[23] EVENT0
ERR_UPD_DATA2	DMM_PAT_IRQSTATUS[22] EVENT0 DMM_PAT_IRQSTATUS_RAW[22] EVENT0	DMM_PAT_IRQENABLE_SET[22] EVENT0 DMM_PAT_IRQENABLE_CLR[22] EVENT0
ERR_UPD_CTRL2	DMM_PAT_IRQSTATUS[21] EVENT0 DMM_PAT_IRQSTATUS_RAW[21] EVENT0	DMM_PAT_IRQENABLE_SET[21] EVENT0 DMM_PAT_IRQENABLE_CLR[21] EVENT0
ERR_UPD_AREA2	DMM_PAT_IRQSTATUS[20] EVENT0 DMM_PAT_IRQSTATUS_RAW[20] EVENT0	DMM_PAT_IRQENABLE_SET[20] EVENT0 DMM_PAT_IRQENABLE_CLR[20] EVENT0
ERR_INV_DATA2	DMM_PAT_IRQSTATUS[19] EVENT0 DMM_PAT_IRQSTATUS_RAW[19] EVENT0	DMM_PAT_IRQENABLE_SET[19] EVENT0 DMM_PAT_IRQENABLE_CLR[19] EVENT0
ERR_INV_DSC2	DMM_PAT_IRQSTATUS[18] EVENT0 DMM_PAT_IRQSTATUS_RAW[18] EVENT0	DMM_PAT_IRQENABLE_SET[18] EVENT0 DMM_PAT_IRQENABLE_CLR[18] EVENT0
FILL_LST2	DMM_PAT_IRQSTATUS[17] EVENT0 DMM_PAT_IRQSTATUS_RAW[17] EVENT0	DMM_PAT_IRQENABLE_SET[17] EVENT0 DMM_PAT_IRQENABLE_CLR[17] EVENT0
FILL_DSC2	DMM_PAT_IRQSTATUS[16] EVENT0 DMM_PAT_IRQSTATUS_RAW[16] EVENT0	DMM_PAT_IRQENABLE_SET[16] EVENT0 DMM_PAT_IRQENABLE_CLR[16] EVENT0
ERR_LUT_MISS1	DMM_PAT_IRQSTATUS[15] EVENT0 DMM_PAT_IRQSTATUS_RAW[15] EVENT0	DMM_PAT_IRQENABLE_SET[15] EVENT0 DMM_PAT_IRQENABLE_CLR[15] EVENT0
ERR_UPD_DATA1	DMM_PAT_IRQSTATUS[14] EVENT0 DMM_PAT_IRQSTATUS_RAW[14] EVENT0	DMM_PAT_IRQENABLE_SET[14] EVENT0 DMM_PAT_IRQENABLE_CLR[14] EVENT0
ERR_UPD_CTRL1	DMM_PAT_IRQSTATUS[13] EVENT0 DMM_PAT_IRQSTATUS_RAW[13] EVENT0	DMM_PAT_IRQENABLE_SET[13] EVENT0 DMM_PAT_IRQENABLE_CLR[13] EVENT0
ERR_UPD_AREA1	DMM_PAT_IRQSTATUS[12] EVENT0 DMM_PAT_IRQSTATUS_RAW[12] EVENT0	DMM_PAT_IRQENABLE_SET[12] EVENT0 DMM_PAT_IRQENABLE_CLR[12] EVENT0
ERR_INV_DATA1	DMM_PAT_IRQSTATUS[11] EVENT0 DMM_PAT_IRQSTATUS_RAW[11] EVENT0	DMM_PAT_IRQENABLE_SET[11] EVENT0 DMM_PAT_IRQENABLE_CLR[11] EVENT0
ERR_INV_DSC1	DMM_PAT_IRQSTATUS[10] EVENT0 DMM_PAT_IRQSTATUS_RAW[10] EVENT0	DMM_PAT_IRQENABLE_SET[10] EVENT0 DMM_PAT_IRQENABLE_CLR[10] EVENT0
FILL_LST1	DMM_PAT_IRQSTATUS[9] EVENT0 DMM_PAT_IRQSTATUS_RAW[9] EVENT0	DMM_PAT_IRQENABLE_SET[9] EVENT0 DMM_PAT_IRQENABLE_CLR[9] EVENT0
FILL_DSC1	DMM_PAT_IRQSTATUS[8] EVENT0 DMM_PAT_IRQSTATUS_RAW[8] EVENT0	DMM_PAT_IRQENABLE_SET[8] EVENT0 DMM_PAT_IRQENABLE_CLR[8] EVENT0
ERR_LUT_MISS0	DMM_PAT_IRQSTATUS[7] EVENT0 DMM_PAT_IRQSTATUS_RAW[7] EVENT0	DMM_PAT_IRQENABLE_SET[7] EVENT0 DMM_PAT_IRQENABLE_CLR[7] EVENT0
ERR_UPD_DATA0	DMM_PAT_IRQSTATUS[6] EVENT0 DMM_PAT_IRQSTATUS_RAW[6] EVENT0	DMM_PAT_IRQENABLE_SET[6] EVENT0 DMM_PAT_IRQENABLE_CLR[6] EVENT0
ERR_UPD_CTRL0	DMM_PAT_IRQSTATUS[5] EVENT0 DMM_PAT_IRQSTATUS_RAW[5] EVENT0	DMM_PAT_IRQENABLE_SET[5] EVENT0 DMM_PAT_IRQENABLE_CLR[5] EVENT0
ERR_UPD_AREA0	DMM_PAT_IRQSTATUS[4] EVENT0 DMM_PAT_IRQSTATUS_RAW[4] EVENT0	DMM_PAT_IRQENABLE_SET[4] EVENT0 DMM_PAT_IRQENABLE_CLR[4] EVENT0

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Table 15-8. Events (continued)

Interrupt	Event Flag	Event Mask
ERR_INV_DATA0	DMM_PAT_IRQSTATUS[3] EVENT0 DMM_PAT_IRQSTATUS_RAW[3] EVENT0	DMM_PAT_IRQENABLE_SET[3] EVENT0 DMM_PAT_IRQENABLE_CLR[3] EVENT0
ERR_INV_DSC0	DMM_PAT_IRQSTATUS[2] EVENT0 DMM_PAT_IRQSTATUS_RAW[2] EVENT0	DMM_PAT_IRQENABLE_SET[2] EVENT0 DMM_PAT_IRQENABLE_CLR[2] EVENT0
FILL_LST0	DMM_PAT_IRQSTATUS[1] EVENT0 DMM_PAT_IRQSTATUS_RAW[1] EVENT0	DMM_PAT_IRQENABLE_SET[1] EVENT0 DMM_PAT_IRQENABLE_CLR[1] EVENT0
FILL_DSC0	DMM_PAT_IRQSTATUS[0] EVENT0 DMM_PAT_IRQSTATUS_RAW[0] EVENT0	DMM_PAT_IRQENABLE_SET[0] EVENT0 DMM_PAT_IRQENABLE_CLR[0] EVENT0

15.2.3.5 DMM

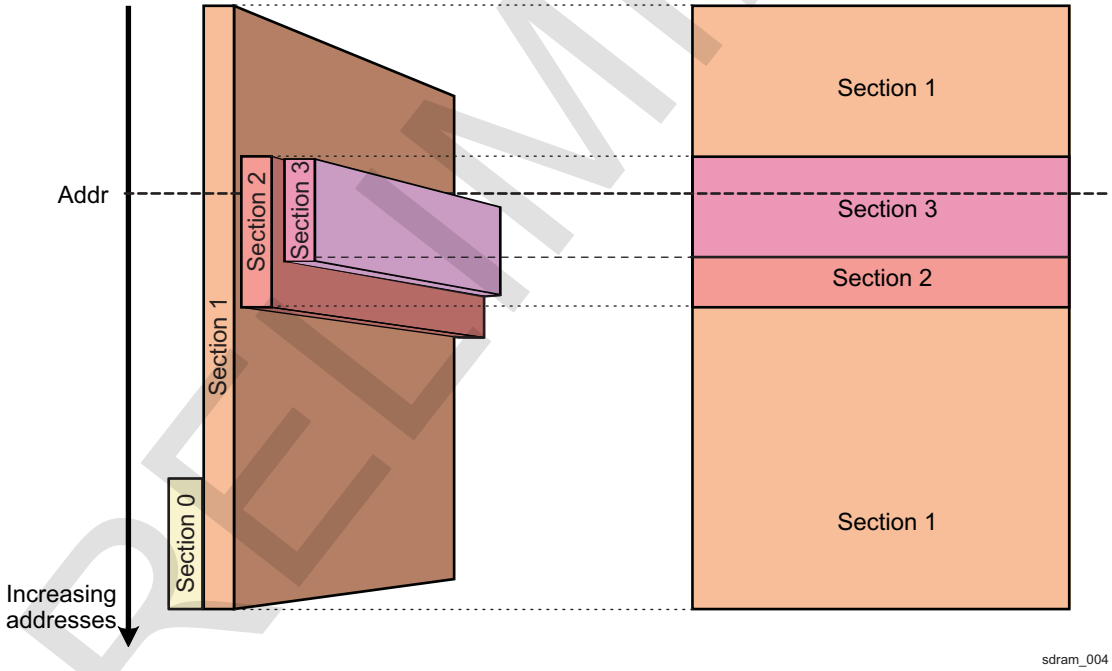
15.2.3.5.1 DMM Concepts

The DMM introduces the concepts of dynamic mapping and DMM atomic units.

15.2.3.5.1.1 Dynamic Mapping

The DMM manages its internal memory space as an ordered set of up to four sections. Figure 15-5 shows the DMM sections and memory mapping.

Figure 15-5. DMM Sections and Memory Mapping



In the DMM, a section is:

- A segment of 16MiB to 2GiB, which is power-of-two in size and aligned to that size in the system map
- An area with a constant interleaving scheme: constant interleaving granularity on a constant set of SDRC (EMIF) targets
- Given a priority equal to its index: the higher the index, the higher the priority

NOTE: Whenever a request hits more than one DMM section, it follows the interleaving scheme of the section having the highest index.

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The interleaving configuration of the DMM, its section-based dynamic memory mapping, is shown on the right in Figure 15-5. In this example, a request at the system address Addr follows the interleaving scheme of section 3, although it hits sections 1, 2, and 3. Similarly, the DMM configuration given in this example prevents any request from using the interleaving scheme of section 0, because section 0 is fully masked by section 1, which has a higher priority.

Each of the four sections is configured through a DMM_LISA_MAP_i register, where i = 0 to 3.

NOTE: The DMM and SDRC registers (Table 15-88 and EMIF registers; see , *EMIF Controller*) are declared in two extra static DMM sections of the highest priority so that they cannot be masked by any standard programmable DMM section.

NOTE: The DMM atomic size is:

- 1kiB in noninterleaved sections
- Equal to the interleaving granularity (128, 256, or 512 bytes) in interleaved sections

15.2.3.5.1.2 Address Mapping

The address mapping inside the DMM is configurable through up to four sections. Each section is defined based on:

- Its system address: The base address of the decoding range for the section
- Its size: The encoding is the number of bits used in the upper 8 bits of the incoming system address
- Its physical address: The base address of the memory range access in the external memory controller
- Its address space: The address space used on the external memory controller when hitting this section
- The target memory controller. The section is not used if this bit field is set to 2'b00.
- Its interleaving definition

The address decoding is priority-based. In case of overlapping sections, only the highest-order one is hit. Register memory spaces have priority over regular memory sections. In case of four sections, the priority order is therefore:

1. Registers
2. DMM_LISA_MAP_3
3. DMM_LISA_MAP_2
4. DMM_LISA_MAP_1
5. DMM_LISA_MAP_0

All register-related addresses are reserved and fixed in the overall address mapping:

- DMM registers: 0x4E00_0000 to 0x4FFF_FFFF
- EMIF1 registers: 0x4C00_0000 to 0x4CFF_FFFF
- EMIF2 registers: 0x4D00_0000 to 0x4DFF_FFFF

There is no overlapping between register sections.

NOTE: Section decoding happens after PAT address translation in the case of TILER. In non-bypass mode, the system address considered for TILER accesses is the virtual address computed based on the PAT translation tables.

The DMM_LISA_LOCK register is used to lock the configuration once set. If written to 1, the LOCK bit prevents further writes to all DMM_LISA_MAP_i registers. The LOCK bit cannot be written back to 0. A reset is required to reprogram the sections.

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15.2.3.5.1.3 Address Translation

The PAT engine of the DMM is composed of a 32-k entry physical address translation vector table and one or two refill engines. The refill engine is a specialized DMA for refilling the content of the PAT table.

The address translation mechanism is available only when the incoming request hits a page mode or tiled mode container; that is, when the incoming address targets the TILER or its aliased view in the system addressing space. Otherwise, the PAT logic is bypassed so that the resulting physical address corresponds to the input address.

The PAT engine supports multiple address translation schemes, called views, which can be bound to one or more initiators through a view mapping mechanism.

15.2.3.5.1.3.1 PAT View Mappings

The PAT engine can have up to 16 groups of initiators that share a set of four PAT views. The connection from an initiator to a PAT view is made through the DMM_PAT_VIEW register. Given that each PAT view index is coded on 4 bits, the DMM_PAT_VIEW register is a 64-bit register split into two 32-bit registers (DMM_PAT_VIEW0 for the first eight PAT view indexes and DMM_PAT_VIEW1 for the last eight PAT view indexes.

The PAT view index that corresponds to the initiator having the value i as the 4 most-significant bits (MSBs) of its L3 ConnID uses the view referenced in entry i of the DMM_PAT_VIEW. For example, the initiator 0xC4 uses the thirteenth view index of the DMM_PAT_VIEW register, the fifth view index in the DMM_PAT_VIEW1 register.

The PAT view index of the initiator i is found in the Vi field. The Wi field is aimed at writing the corresponding Vi. When writing to the DMM_PAT_VIEW registers, the only Vi view indexes that are updated are those having their corresponding Wi bit, and byte enable, set. The Wi bits are always read as 0. For instance, to set the PAT view indexes V3 and V7 to 2 and 1, respectively, the DMM_PAT_VIEW0 register must be written with 5000 6000h.

15.2.3.5.1.3.2 PAT View Map Base Address

The PAT view map base address defines the base address of all PAT translated addresses.

Bit [31] of all PAT translated addresses is set to BASE_ADDR. For example, if the DMM_PAT_VIEW_MAP_BASE register is set to 8000 0000h, all PAT translated addresses will have bit [31] set to 1 so that the translated addresses range from 8000 0000h to FFFF FFFFh. All reserved bits of this DMM PAT base address register are read to 0.

15.2.3.5.1.3.3 PAT Views

A PAT view defines the kind of physical address translation to perform for each mode accesses (page, 8-bit, 16-bit and 32-bit). Each mode of each PAT view can be configured to use a container-grained translation or page-mode translation.

15.2.3.5.1.3.3.1 PAT Direct Access Translation

The container-grained translation is named the direct access. In this mode, the translation vector is given directly by the CONT_x bit field that corresponds to the accessed mode.

- A page mode access uses the vector contained in the DMM_PAT_VIEW_MAP_i[27:24] CONT_PAGE bit field.
- A 32-bit mode access uses the vector contained in the DMM_PAT_VIEW_MAP_i[19:16] CONT_32 bit field.
- A 16-bit mode access uses the vector contained in the DMM_PAT_VIEW_MAP_i[11:8] CONT_16 bit field.
- An 8-bit mode access uses the vector contained in the DMM_PAT_VIEW_MAP_i[3:0] CONT_8 bit field.

See Figure 15-6.

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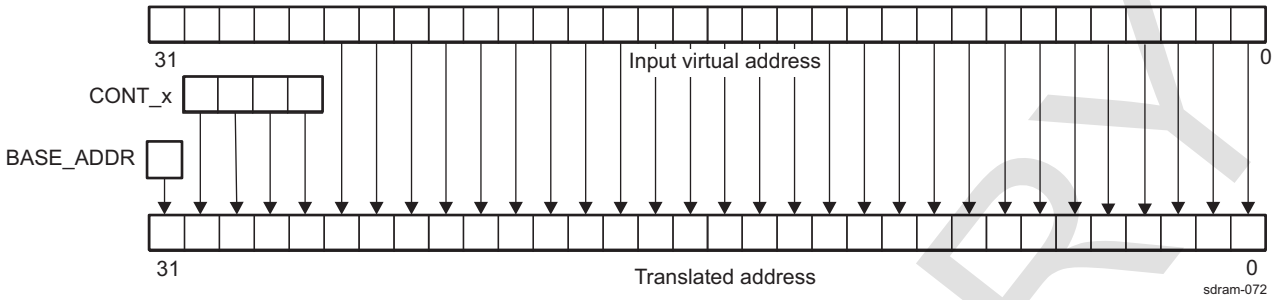
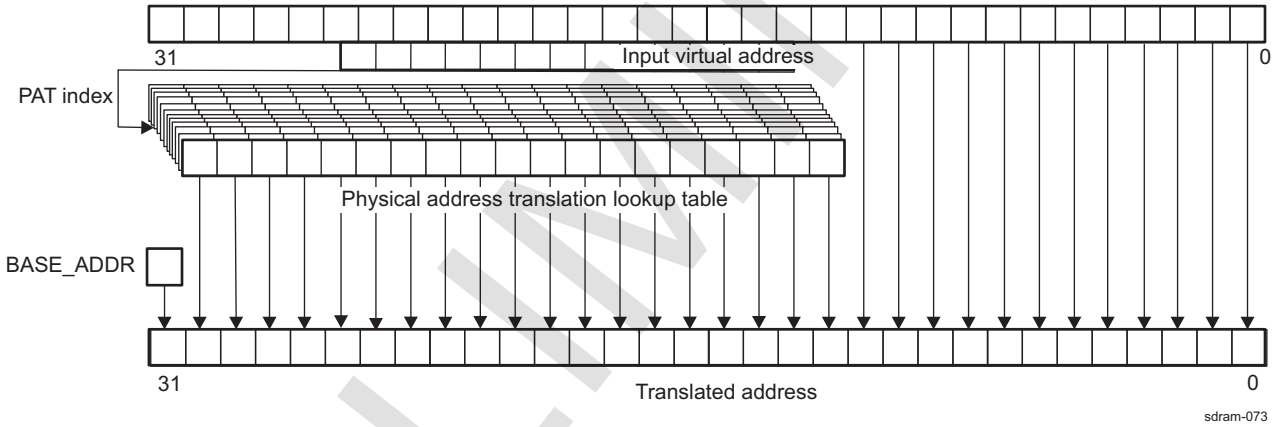
Figure 15-6. PAT Direct Access Translation



15.2.3.5.1.3.3.2 PAT Indirect Access Translation

The page-grained translation is named the indirect access. In this mode the translation vector is found in the internal 32-k entry physical address translation vector table at the index given by bits [26:12] of the input virtual address, and the DMM_PAT_VIEW_MAP_i CONT_x bit field references the internal physical address translation table to use. Because the DMM uses only one such table, in this mode the CONT_x bit field must be written as 0. See Figure 15-7.

Figure 15-7. PAT Indirect Access Translation



Each entry of the PAT lookup table (LUT) is a 19-bit vector that replaces bits [30:12] of the input virtual address. The PAT index aimed at selecting the vector in the table consists of bits [26:12] of the input virtual address.

15.2.3.5.1.3.3.3 PAT View Configuration

There are four different views in a DMM, each with its own DMM_PAT_VIEW_MAP_i register for defining the kind of address translation to perform.

The PAT view type of each mode is selected by the ACCESS_x bit field in the DMM_PAT_VIEW_MAP_i register, i being the index of the considered view. When this field is set to 1, the indirect access scheme is used; otherwise, the PAT performs the address translation in a direct way with the corresponding CONT_x vector.

When configuring a mode in a view to use the indirect access, the corresponding CONT_x bit field must be filled with 0.

15.2.3.5.1.3.3.4 PAT Address Translation LUT

The PAT LUT has the same geometry as the DMM container. It has 128 lines of 256 entries of 19-bit each. See Figure 15-8.

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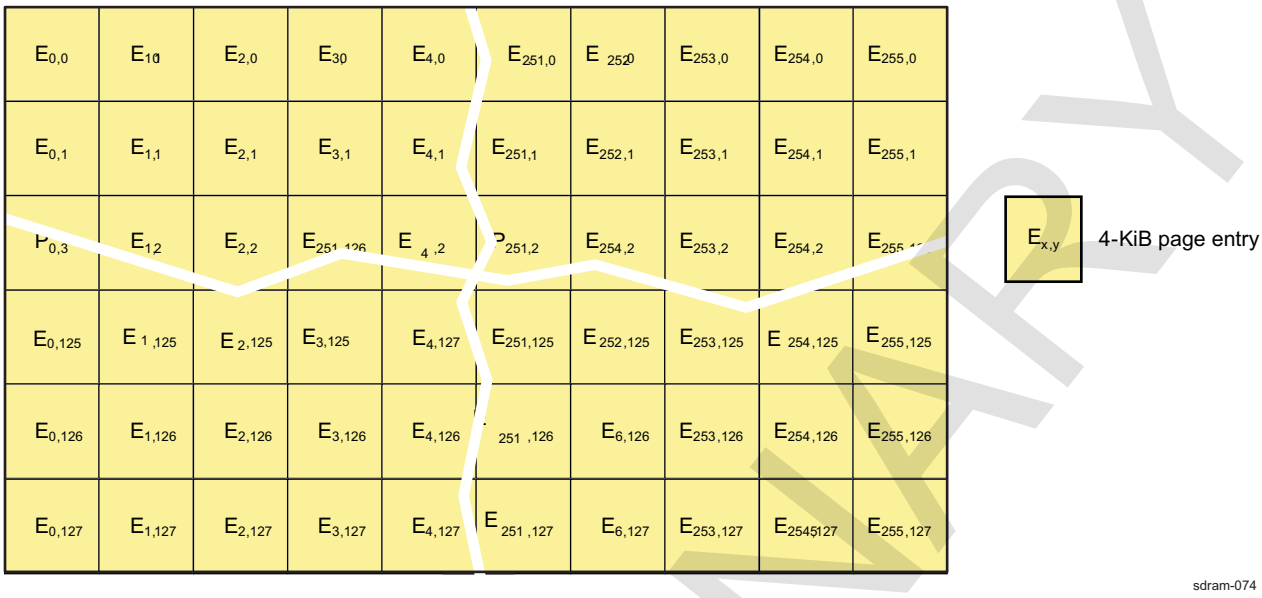
Figure 15-8. Physical Address Translation Table



Each entry of the PAT address corresponds to the page in the DMM container that has the same location. The entry (74, 42) in the table corresponds to the page (74, 42) in any DMM container.

15.2.3.5.1.3.3.5 Direct Access to the PAT Table Vectors

The PAT table is typically refilled with specialized DMA called refill engines. Some direct read and write access to the content of this table is granted when disabling the use of one or the other refill engine by writing 1 in the MODEi field of the DMM_PAT_CONFIG register that corresponds to the refill engine i to disable.

In this mode, often called the debug mode, the data read in or written to the DMM_PAT_DATA_i register corresponds to the vector in the PAT table, whose index is in the X0 and Y0 fields of the DMM_PAT_AREA_i register.

15.2.3.5.1.3.3.6 Automatic Refill Through the Refill Engines

See Section 15.2.4.1, *PAT Use Cases*.

15.2.3.5.2 DMM Transaction Flows

15.2.3.5.2.1 Nontiled Transaction Flow

Each nontiled interconnect transaction that reaches the DMM on a TILER port is subject to the same processing.

The TILER blocks consider separated request, data, and response paths. An overview of each path follows and more detailed information is in Section 15.2.3.5.3, *DMM Internal Macro-Architecture*.

On the request path, the flow consists of:

- Allocating a TILER response context for the timely generation of the appropriate responses
- Splitting 2D requests in a collection of 1D requests – TILER ports
- Splitting requests at DMM unit boundaries; the split granularity is provided by the LISA mapping registers
- Allocating an available buffer in the appropriate ROBIN, for both read and write requests
- In case of a write request, allocating and updating a TILER write context to direct the incoming write data into the relevant reordering buffer

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- Generating the initiator-indexed priority extension by use of the PEG block

On the write data path, the flow consists of forwarding incoming data to the relevant reordering buffer in accordance with the corresponding TILER write context.

On the response path, responses are returned when:

- At least one response has entered each related buffer, in case of read requests
- All related responses have returned from the SDRC, in case of write requests
- AND no other previous pending response with the same tag exists

15.2.3.5.2.2 Tiled Transaction Flow

Similarly, each tiled interconnect transaction that reaches the DMM is subject to the same processing.

The TILER blocks consider separated request, data, and response paths. An overview of each path follows, and more detailed information is in Section 15.2.3.5.3, *DMM Internal Macro-Architecture*.

On the request path, the processing phase consists of:

- Decoding the address to qualify whether the request targets the TILER or the memory directly
- Transforming TILER-specific requests to their natural representation; the address, width, and height are modified accordingly

On the request path, the generation phase consists of:

- Allocating a TILER response context for the timely generation of the appropriate responses
- Splitting malformed: The request stride differs from the container stride and from the double of this container stride – tiled 2D requests in a collection of 1D requests
- Splitting tiled requests at tile boundaries
- Performing the page-based address translation by use of the PAT block
- Allocating an available buffer in the appropriate ROBIN, for read and write requests
- In case of a write request, allocating and updating a TILER write context to direct the incoming write data into the relevant reordering buffer
- Generating the initiator-indexed priority extension by use of the PEG block

On the data path, any incoming data is transformed in accordance with the corresponding TILER write context and sent to the appropriate reordering buffer.

On the response path, responses are returned when:

- A minimal number of responses have entered the corresponding buffers, in case of read requests
- All related responses have returned from the SDRCs, in case of write requests
- No other previous pending response with the same tag exists

15.2.3.5.3 DMM Internal Macro-Architecture

This section describes the DMM internal macro-architecture, specifically:

- Input request decoding
- PAT and synchronized translation table reloading
- Output request and response generation
- Memory mapping in the system addressing space, including interleaving
- Tag management
- Priority handling
- Contexts
- Maximum allowed burst size
- Reconstruction buffer dimensioning

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15.2.3.5.3.1 LISA Description

The LISA is a full crossbar aimed at setting priorities, managing tag, and mapping memory.

The interconnect routes are:

- TILER requests on the ROBIN initiator nodes
- TILER write data on the ROBIN write buffers
- ROBIN read data to the relevant TILER initiators

The LISA block registers are DMM_LISA_MAP_i (where i = 0 to 3) and DMM_LISA_LOCK.

When two ROBINs are in use, the two ports are interleaved at a programmable boundary from 128 bytes or more (configurable with the DMM_LISA_MAP_i[19:18] SDRC_INTL bit field).

15.2.3.5.3.2 PAT Description

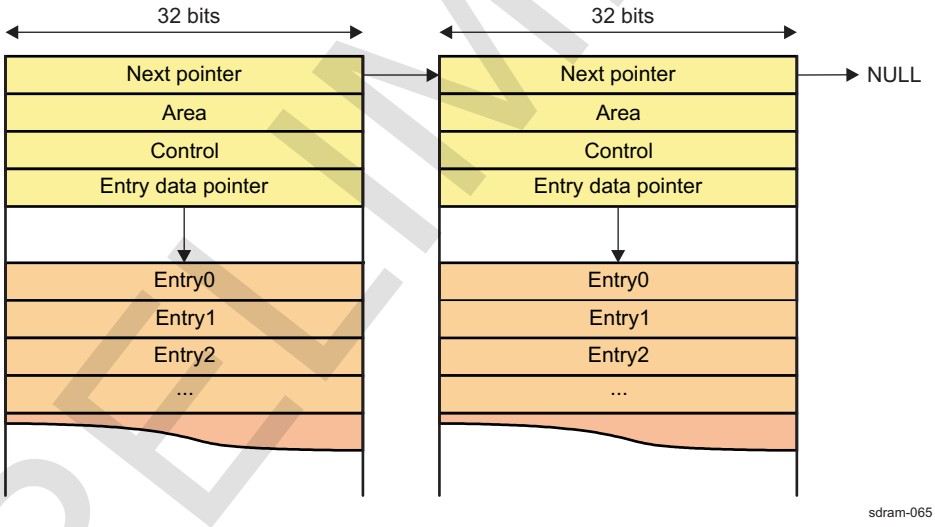
The PAT block maps physical pages to each TILER container page. The internal address translation memories used in the PAT block are designed with RFFs. It consists of:

- A memory-based LUT which has the same geometry as the container pages
- A refill engine for modifying entries in a given area of the internal LUT

A PAT descriptor is a singly-linked list node (see Figure 15-9) that contains:

- A description of the LUT area to reload
- A description of how to reload the defined LUT area
- A pointer to the location where the corresponding LUT entries are stored

Figure 15-9. PAT Descriptors



PAT descriptors are chained and processed until a NULL pointer is encountered. The PAT bank allocation scheme allows the updating of four consecutive entries of a line in a single cycle regardless of the refilling orientation.

The PAT descriptor structure directly maps the following registers (where i = 0 to 3):

- DMM_PAT_DESCR_i
- DMM_PAT_AREA_i
- DMM_PAT_CTRL_i
- DMM_PAT_DATA_i

The PAT refill engine can be started by:

- Filling manually all the necessary registers:
  - DMM_PAT_AREA_i with the (x0, y0) (x1, y1) area definition

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  - DMM_PAT_DATA_i with the physical address of the corresponding area entry table
  - DMM_PAT_CTRL_i[6:4] DIRECTION bit field with the relevant (S, Y, X) direction of the area refill
  - DMM_PAT_CTRL_i[0] START bit with 1
- Writing the physical address of a memory-mapped PAT descriptor in DMM_PAT_DESCR_i, which updates:
  - DMM_PAT_AREA_i with the area value of the descriptor
  - DMM_PAT_DATA_i with the data value of the descriptor
  - DMM_PAT_CTRL_i with the control value of the descriptor
  - DMM_PAT_DESCR_i with the next value of the descriptor
- The data part of the PAT refill starts only when the DMM_PAT_CTRL_i[0] START bit is asserted.

The DMM_PAT_STATUS_i register can be used to see whether the process has completed without errors.

15.2.3.5.3.3 PEG Description

The PEG is a dynamic software-programmable, initiator-ConnID-indexed table of priorities. Its role is to change on the fly the priority of an initiator, for initiators that do not generate their own per-transaction priority. The mapping of each initiator to the table (split into eight registers) is based on its 6-MSB group ConnID (see Table 28-20, *ConnID Mapping (Debug View)*, in Chapter 28, *On-Chip Debug Support*.

When an interconnect request enters the DMM, its priority is extracted from the PEG LUT and set in its MReqInfo field.

The 64 priority entries are software-programmable with eight DMM_PEG_PRIO registers (DMM_PEG_PRIO_k).

These eight registers are each split into eight 4-bit fields, each field mapping an entry of the LUT with:

- The 3-bit priority coded on the 3 least-significant bits (LSBs): Px field. A priority of 0 defines the highest priority and a priority of 7 defines the lowest priority. The priority of a request with ConnId equal to y is written in (8.n + x) P field, where n is the number of the priority register (n = 0 to 7) and x is the number of the P field in the corresponding register (x = 0 to 7). If the ConnId is 0x16, its priority is written in the third priority register (where n = 2), in the P4 bit field ([18:16]), because x = 4.
- A $\overline{W}$x field-specific active-low local write enable bit, always read as 0, on the most-significant bit (MSB). The role of the $\overline{W}$ bit is to allow the modification of a single entry without requiring a read-modify-write sequence. Because its $\overline{W}$ bits are always read as 0, writing back the modified register updates all priority fields of the register.

Although this priority information is generated before entering the LISA block, it is not used internally in the local interconnect arbitration but is forwarded to the SDRC as an MReqInfo, where it indicates the command priority.

It is also possible to give a priority for the internal PAT engine through the DMM_PEG_PRIO_PAT register.

15.2.3.5.3.4 ROBIN Description

The ROBIN is a block that provides some working buffering for converting data and responses to-and-from between raster and tiled organizations, and a master port to connect to the SDRC.

The ROBIN block:

- Forwards requests
- Writes data and buffers responses
- Keeps write data ordering
- Performs intraword tiling and orientation transforms
- Handles tags

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15.2.3.5.3.5 TILER Description

The main function of the TILER is request conversion caused by tiling.

The TILER block:

- Decodes the address to qualify whether the request targets the TILER or the memory directly
- Converts TILER-specific requests to their natural representation; address, width, and height are modified accordingly
- Allocates an internal response context for the timely generation of appropriate responses
- Splits tiled requests at tile boundaries and not-tiled requests at DMM atomic section boundaries
- Requests the page-based address translation
- Requests buffer allocation in the appropriate ROBIN
- In case of a write request, allocates and updates an internal write context to direct the incoming write data into the relevant reordering buffer

The interdependent tilingand isometric transform concepts introduced in the TILER are described in the following section.

15.2.3.6 TILER

15.2.3.6.1 TILER Concepts

This section describes the concepts behind the TILER transforms, through a top-down approach starting from the main object container.

15.2.3.6.1.1 TILER Rationale

This section is a synthesis of all TILER concepts, giving one rule per TILER structure level.

Figure 15-10 shows the TILER address space structure for tiled modes.

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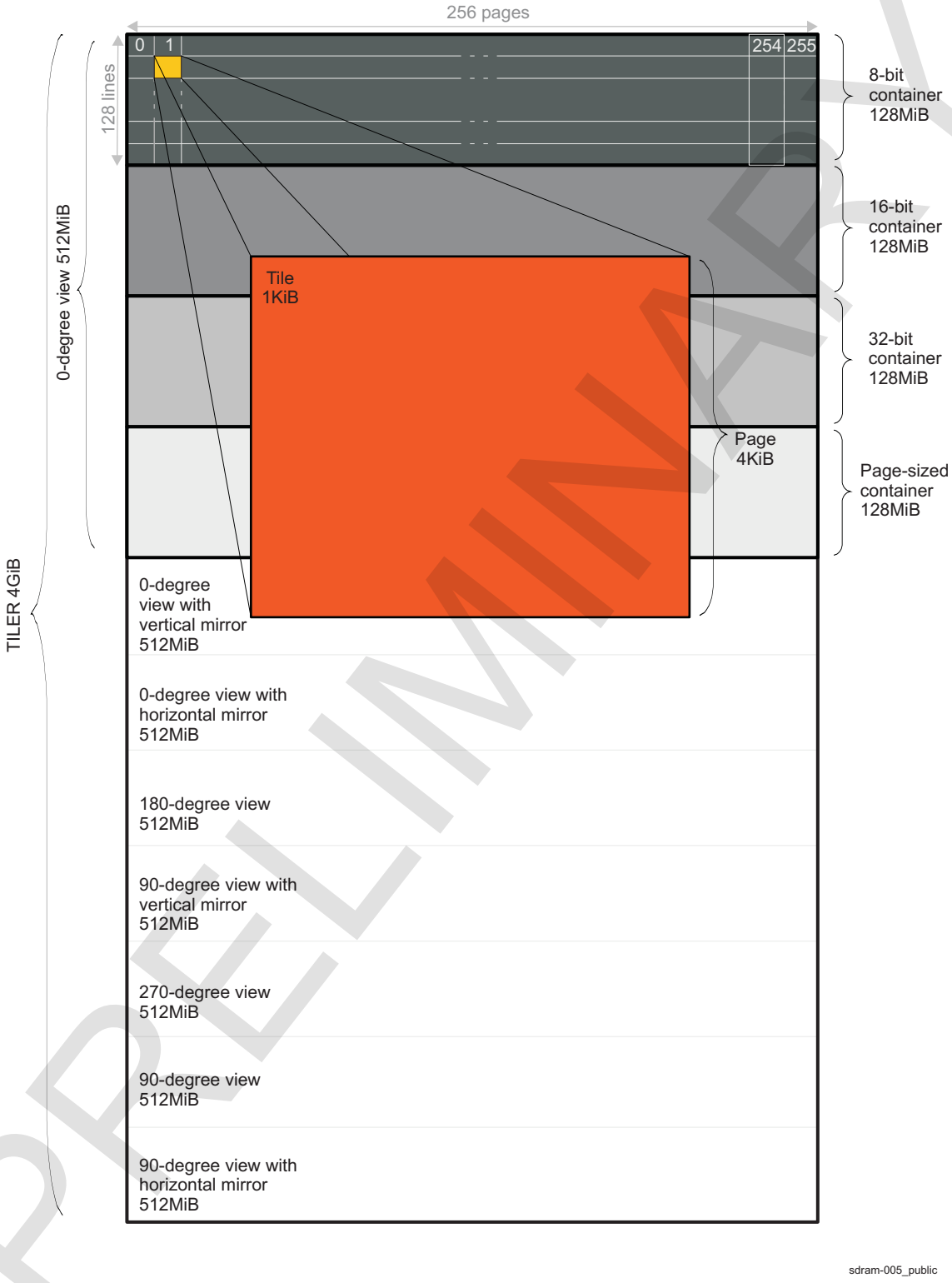
Figure 15-10. TILER Address Space Structure for Tiled Modes



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15.2.3.6.1.1.1 The TILER is a 4-GiB Virtual Address Space Composed of Eight Views

There is one view for each of the eight possible ways of scanning a frame-buffer:

- From left to right then from top to bottom

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- From right to left then from top to bottom
- From left to right then from bottom to top
- From right to left then from bottom to top
- From top to bottom then from left to right
- From top to bottom then from right to left
- From bottom to top then from left to right
- From bottom to top then from right to left

15.2.3.6.1.1.2 A View is a 512-MiB Virtual Address Space Composed of Four Containers

There is one container per element size to allow correct access patterns in any of the eight possible orientations. The container is the entity where all objects of a given element type are allocated.

The element is the entity of maximum size (8, 16, 32 bits or page-sized), which is invariant in any orientation.

15.2.3.6.1.1.3 A Container is a 128-MiB Virtual Address Space

A container is composed of an array of 128 lines of 256 pages of 4kiB each.

The page defines the granularity of physical memory allocation through a PAT unit – MMU.

15.2.3.6.1.1.4 A Page is a 4-kiB Virtual Address Space

A page is composed of two lines. Each line consists of two tiles.

15.2.3.6.1.1.5 A Tile is a 1-kiB Address Space

The tile is designed to offer bidimensional data locality in a single SDRAM page. In this respect, it is sized to 1 kiB; that is, to the size of the smallest SDRAM page.

15.2.3.6.1.2 TILER Modes

The TILER supports three major modes, bypass, page, and tiled. Each mode has a specific output request generation.

15.2.3.6.1.2.1 Bypass Mode

This mode is transparent from the TILER perspective. However, from the DMM perspective:

- 2D block bursts are broken down on a line basis in a set of incremental bursts.
- Incremental bursts, including those issued by a 2D block burst breakdown, are split at the DMM atomic unit of the section hit by the burst at:
  - The interleaving granularity of the section (128, 256, or 512 bytes) in interleaved sections
  - 1-kiB boundary in noninterleaved sections

15.2.3.6.1.2.2 Page Mode

This mode uses the DMM address translation mechanism for nontiled accesses. In this respect it is similar to bypass mode:

- 2D block bursts are broken down on a line basis in a set of incremental bursts.
- Incremental bursts, including those issued by a 2D block burst breakdown, are split at:
  - The interleaving granularity of the section (128, 256, or 512 bytes) in interleaved sections
  - 1-kiB boundary in noninterleaved sections

15.2.3.6.1.2.3 Tiled Mode

Tiled mode has two major breakdown algorithms:

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- One for well-formed 2D block requests that conform to the orientation, mode, and stride listed in Table 15-9
- One for 1D incremental requests and ill-formed 2D block requests

Table 15-9. Well-Formed Tiled Mode 2D Block Requests

Orientation			Mode		Stride	Description
S	$\overline{Y}$	$\overline{X}$	M1	M0	(bytes)	
0	x	x	0	0	16,384	Plain access to an 8-bit progressive frame in 0 or 180 degrees
					32,768	Field access to an 8-bit interlaced frame 0 or 180 degrees
			0	1	32,768	Plain access to a 16-bit progressive frame in 0 or 180 degrees
					65,536	Field access to a 16-bit interlaced frame 0 or 180 degrees
			1	0	32,768	Plain access to a 32-bit progressive frame in 0 or 180 degrees
					65,536	Field access to a 32-bit interlaced frame 0 or 180 degrees
1	x	x	0	0	8192	Plain access to an 8-bit progressive frame in 90 or 270 degrees
					16,384	Field access to an 8-bit interlaced frame 90 or 270 degrees
			0	1	8192	Plain access to a 16-bit progressive frame in 90 or 270 degrees
					16,384	Field access to a 16-bit interlaced frame 90 or 270 degrees
			1	0	16,384	Plain access to a 32-bit progressive frame in 90 or 270 degrees
					32,768	Field access to a 32-bit interlaced frame 90 or 270 degrees

Similar to the bypass and page modes, ill-formed 2D block requests are broken down on a line basis in a set of incremental bursts. In tiled mode, however, these incremental virtual bursts do not translate to 1D physical burst requests.

15.2.3.6.1.3 Object Container Definition

The object container is the unique addressable entry point of the TILER. It is a 128-MiB virtual address space, where all objects of a same kind and orientation are allocated.

Four main types of containers are present in the TILER, each referred by a mode:

- 8-bit element mode, for efficiently accessing bidimensional arrays of 8-bit data
- 16-bit element mode, for efficiently accessing bidimensional arrays of 16-bit data
- 32-bit element mode, for efficiently accessing bidimensional arrays of 32-bit data
- Page mode, for efficient 1D accesses

Figure 15-11 shows the TILER object containers and views.

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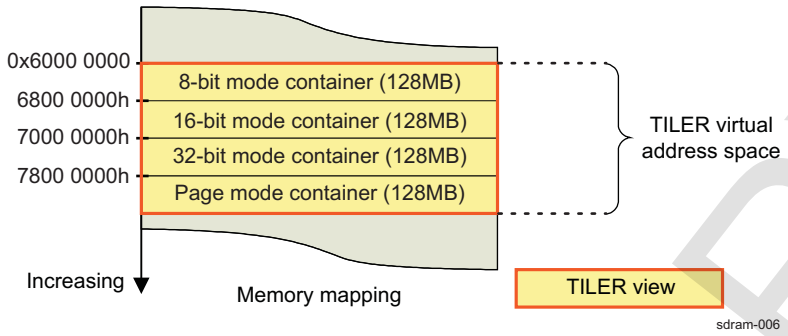
Figure 15-11. TILER Object Containers and Views

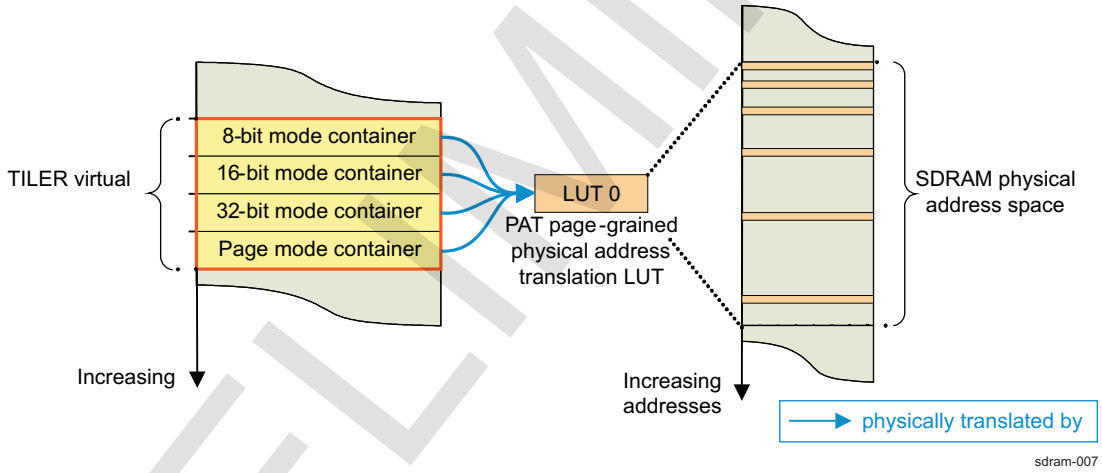


The 512-MiB virtual address space composed of four 128-MiB object containers of different modes is called a view. Because eight orientations are available per mode, the TILER actually manages 32 kinds of containers.

The physical memory footprint of a 512-MiB TILER view is directly subject to the nature of the PAT unit.

A unique PAT LUT is instantiated in the DMM. This table is shared by all TILER modes. Hence, each of the four modes cannot be given its own private page-grained PAT LUT. A maximum of 128MiB of objects among all TILER modes can be managed as shown in Figure 15-12.

Figure 15-12. TILER Memory Footprint With PAT and Shared Physical Address Translation LUT



Although each of the four modes has its own separate virtual 128-MiB object container, these containers are all mapped to the same piecewise 128-MiB physical address space, and are then not physically separated. Consequently, a memory-related system constraint is that no more than 128-MiB of objects can be available simultaneously in a TILER view.

NOTE: Software must ensure that any object allocated in a mode does not physically overlap with any other object, even in another mode.

15.2.3.6.1.4 Page Definition

A TILER page defines the granularity of object allocation in virtual TILER containers.

Because the subpage structure is mode-specific, the page is the smallest granularity common to all modes, making it the granularity to consider in the TILER resource manager for object allocation.

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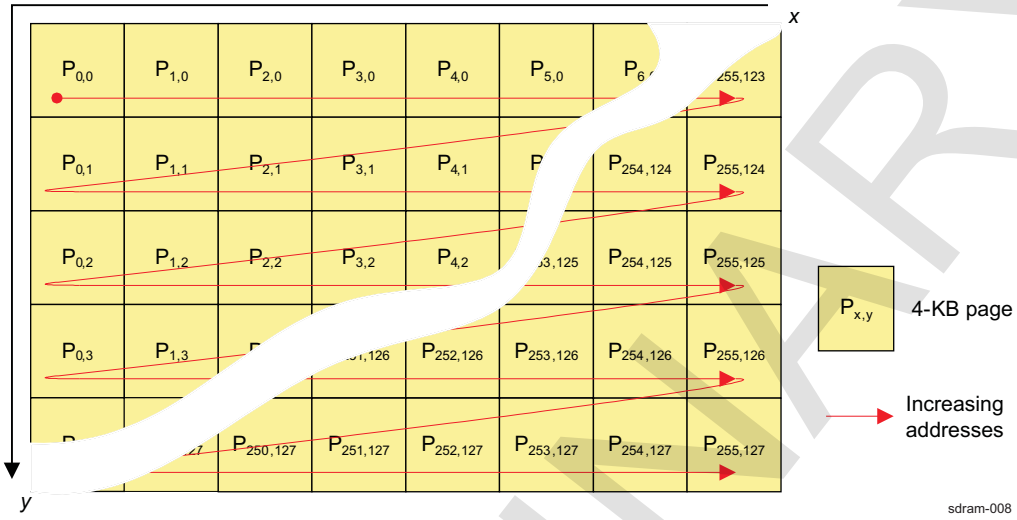
15.2.3.6.1.4.1 Container Geometry With 4-kiB Pages

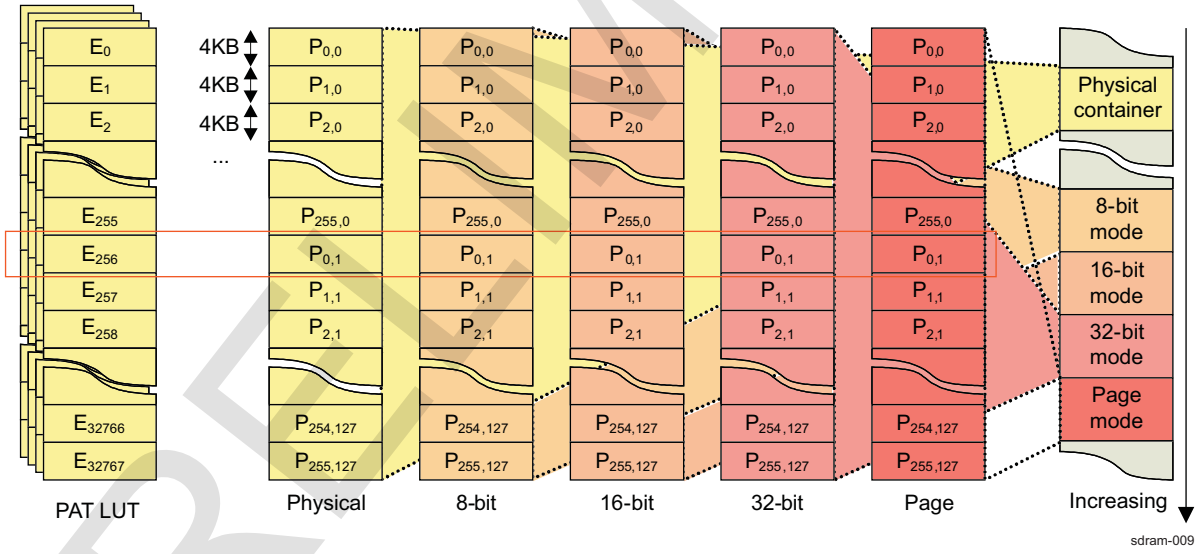
Because the size of the page is 4kiB, any 128-MiB object container is a set of 32,768 pages, organized in an array of 256 columns and 128 rows, as shown in Figure 15-13.

Figure 15-13. Object Container Geometry With 4-kiB Pages



This array of pages is mapped to the system address space, as shown in Figure 15-14.

Figure 15-14. TILER Page Mapping When Using 4-kiB Pages



In any 128-MiB object container, the 4-kiB page Px,y at column x (where 0 = x 256) and row y (where 0 = y 128), is found at an offset of 4096.(x+256.y) bytes from the base address of the related object container.

Similarly, the page Px,y at column x (where 0 = x 256) and row y (where 0 = y 128), is translated by the LUT entry Ex+256.y found at the index x+256.y.

15.2.3.6.1.4.2 Container Geometry and Page Mapping Summary

The TILER has a page size of 4096 bytes. The page $P_{x,y}$:

- Has max_x = 256 and max_y = 128
- Is found at an offset of 4096.(x + max_x.y) bytes from the base address of the related object container
- Is translated by the entry at the index (x + max_x.y) of the LUT

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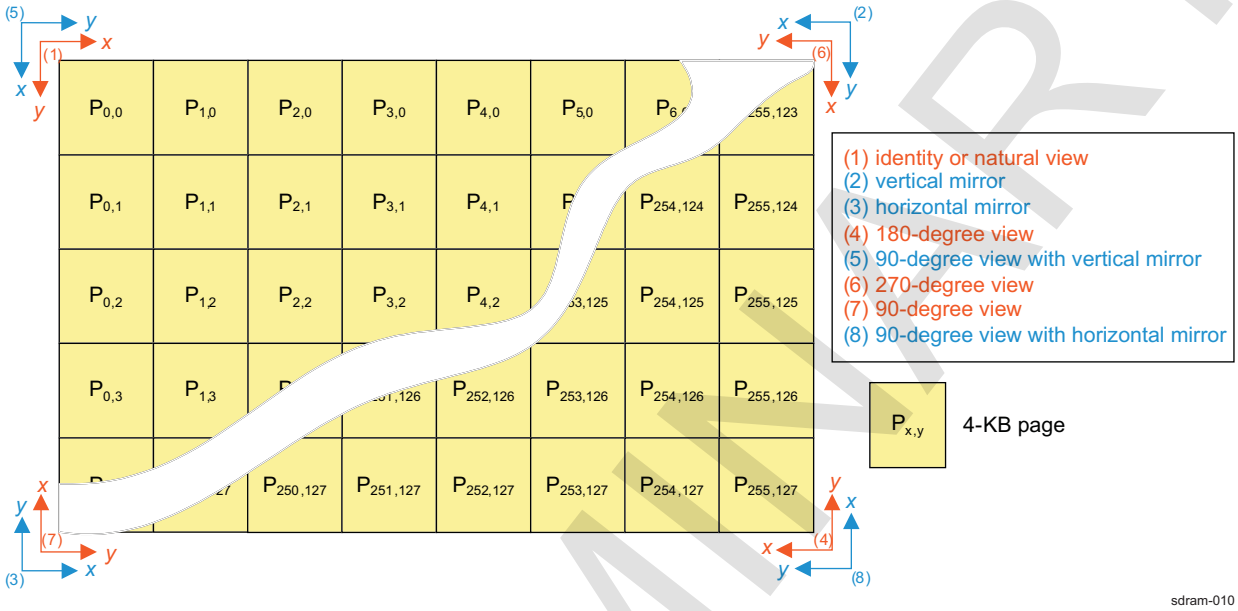
15.2.3.6.1.5 Orientation

This section describes the eight on-the-fly orientation-related isometric transforms, which correspond to all available changes of orthonormal basis in the bidimensional space of the TILER container.

Figure 15-15 shows isometric transforms in the TILER container

Figure 15-15. Isometric Transforms in the TILER Container



Mathematically speaking, all these transforms correspond to the composition of a 0-, 90-, 180-, or 270-degree rotation with an optional reflection. The nature of this orientation is based on the three following binary parameters:

- *X* to change the direction of the $_{x}$ axis of the TILER container
- *Y* to change the direction of the $_{y}$ axis of the TILER container
- *S* to swap the modified $_{x}$ and $_{y}$ axis

Hereafter in this document the term orientation refers to any composition of a "quadrant" rotation with an optional horizontal (flip-flop) or vertical mirroring.

15.2.3.6.1.6 Tile Definition

A tile is a subdivision of a page that is aimed at:

- Representing a 2D block to better balance accesses in both directions
- Ensuring that any tiled access that fits within a tile is made atomic in the SDRC and fits in a single SDRAM memory page
- Minimizing the number of SDRAM page openings per 2D block transfer

The tile is defined as a 1-kiB 2D block, and a 4-kiB page as an array of two lines of two tiles each.

When the considered page is in an interleaved DMM section, it is necessary that:

- The DMM memory interleaving size of tiled accesses is set to 1kiB (a tile size) so that any tiled request that fits within a tile, fits in a single SDRAM memory page.
- Any request that spans two or four tiles is distributed on a maximum number of SDRCs.

15.2.3.6.1.7 TILER Virtual Addressing

The TILER can be virtually accessed in four different modes: 8-, 16-, 32-bit, and page modes. Each mode defines the element granularity to apply isometric transforms, as summarized in Table 15-10.

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Table 15-10. Coding and Description of TILER Modes

Mode	Name	Granularity (Element Size)
0	8-bit tiled mode	8 bits
1	16-bit tiled mode	16 bits
2	32-bit tiled mode	32 bits
3	Page mode	4096 bytes

For instance, making a vertical mirror of a 16-byte horizontal line that contains the word 000102030405060708090A0B0C0D0E0Fh, leads to:

- 0F0E0D0C0B0A09080706050403020100h in 8-bit tiled mode
- 0E0F0C0D0A0B08090607040502030001h in 16-bit tiled mode
- 0C0D0E0F08090A0B0405060700010203h in 32-bit tiled mode
- 000102030405060708090A0B0C0D0E0Fh in page mode – unchanged because the element granularity is 4KB

Besides, because each of the eight orientations is available for any of the four modes, the TILER has 32 addressing possibilities (see Table 15-11).

Table 15-11. Coding and Description of TILER Orientations

S	$\overline{Y}$	$\overline{X}$	Description	Alternate description
0	0	0	0-degree view	Natural view
0	0	1	0-degree view with vertical mirror	180-degree view with horizontal mirror
0	1	0	0-degree view with horizontal mirror	180-degree view with vertical mirror
0	1	1	180-degree view	
1	0	0	90-degree view with vertical mirror	270-degree view with horizontal mirror
1	0	1	270-degree view	
1	1	0	90-degree view	
1	1	1	90-degree view with horizontal mirror	270-degree view with vertical mirror

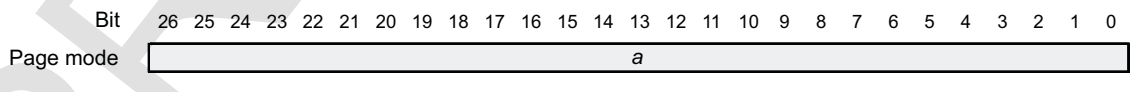
15.2.3.6.1.7.1 Page Mode Virtual Addressing and Characteristics

When used in page mode, the 128-MiB TILER space is seen as an orientation-specific sequence of 32,768 pages of 4kiB each. The access sequence inside a page is left unchanged.

Therefore, in page mode, the TILER is accessed similarly to any 128-MiB memory, with a 27-bit byte-based address.

NOTE: From here forward, the address is noted as *a* (see Figure 15-16).

Figure 15-16. Page Mode Virtual Addressing



15.2.3.6.1.7.2 Tiled Mode Virtual Addressing and Characteristics

When used in tiled mode, the 128-MiB TILER space is seen as a giant frame-buffer, the container. The addressing and characteristics of this giant frame-buffer depend on:

- The tiled mode, which defines the considered atomic element size
- The orientation, which potentially swaps its x and y axis, and hence the container geometry

Table 15-12 summarizes the container characteristics in tiled mode.

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Table 15-12. Tiled Mode Container Characteristics

Orientation			Element Size (Bits)	Width (Elements)	Height (Elements)	Stride (Bytes)	
S	Y	X				Progressive	Interlaced
0	x	x	8	16,384	8192	16,384	32,768
			16	16,384	4096	32,768	65,536
			32	8192	4096	32,768	65,536
1	x	x	8	8192	16,384	8192	16,384
			16	4096	16,384	8192	16,384
			32	4096	8192	16,384	32,768

As a result, the coordinate (x_0, y_0) of a pixel in an oriented view is translated in a virtual address, as shown in Figure 15-17 and Figure 15-18.

Figure 15-17. Tiled Mode Addressing in 0- or 180-Degree Orientation (S = 0)

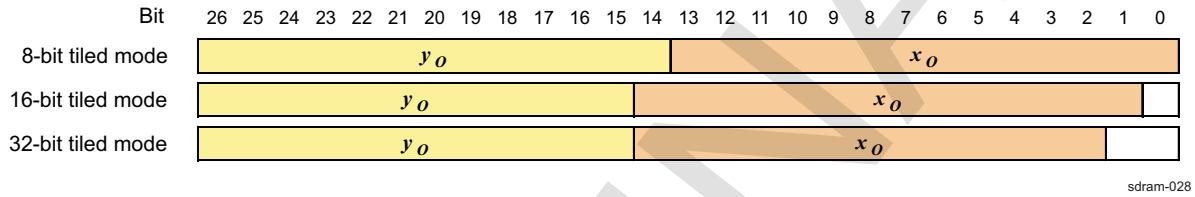
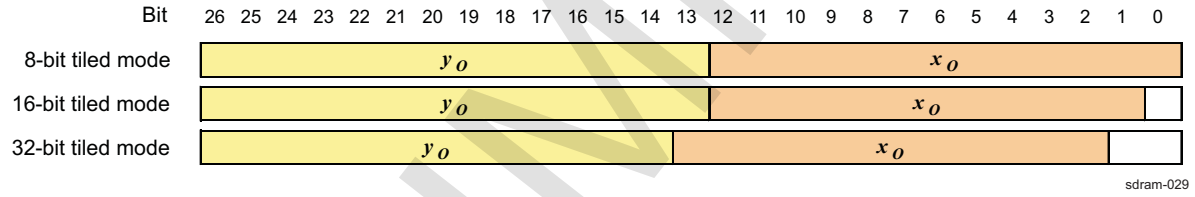


Figure 15-18. Tiled Mode Addressing in 90- or 270-Degree Orientation (S = 1)



15.2.3.6.1.7.3 Element Ordering in the TILER Container

This section describes how elements (8-, 16-, or 32-bit data or a 4-kiB page) are ordered in the container. In other words, this section describes how the path of incrementing virtual addresses is mapped in the container.

Regardless of the mode, and hence the element size, the sequence for ordering the elements in their related container is strictly similar and depends only on the related orientation. In other words:

- Mode is concerned with element granularity.
- Orientation is concerned with change of orthornormal basis for ordering the elements in the mode-specific container.

A corollary to the previous statements is that in a given mode the internal structure of an element is unchanged regardless of the orientation. In page mode for instance, the offset of a word inside a page is invariant by orientation; the content of a page is always accessed in the same manner.

In the following sections, the natural container orthonormal basis is referenced as:

$$(\vec{x}_N, \vec{y}_N)$$

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and the oriented orthonormal basis is referenced as:

$$(\vec{x}_O, \vec{y}_O)$$

sdram-031

PRELIMINARY

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15.2.3.6.1.7.3.1 Natural View or 0-Degree View (Orientation 0)

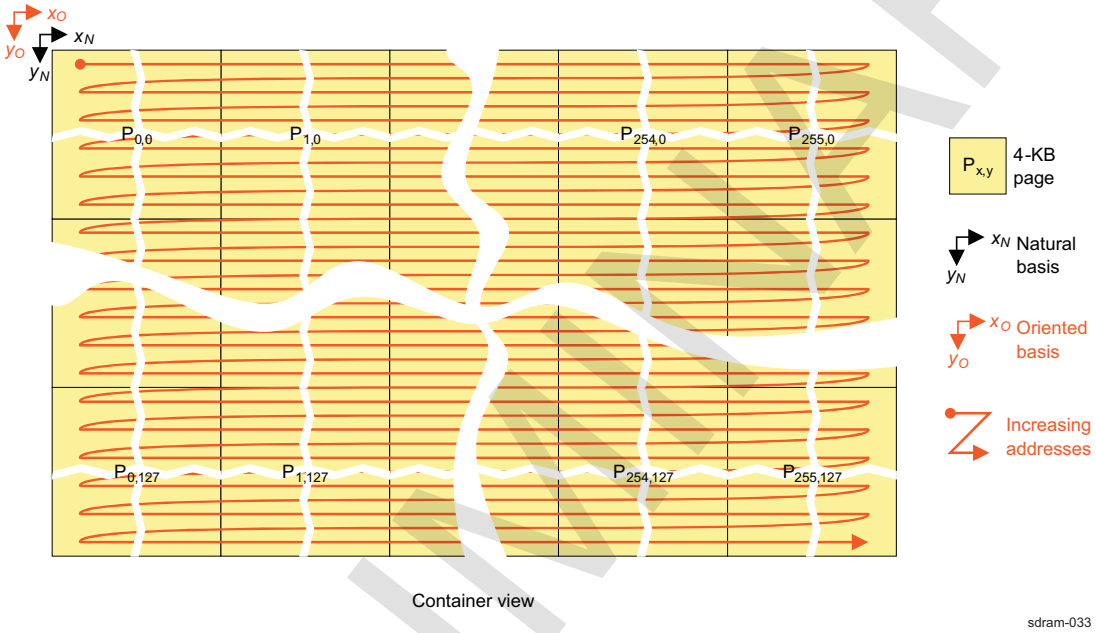
This orientation defined by S = 0, $\overline{Y}$ = 0, and $\overline{X}$ = 0 means that the operated change of basis is:

$$\begin{cases} \vec{x}_O = \vec{x}_N \\ \vec{y}_O = \vec{y}_N \end{cases}$$

sdram-032

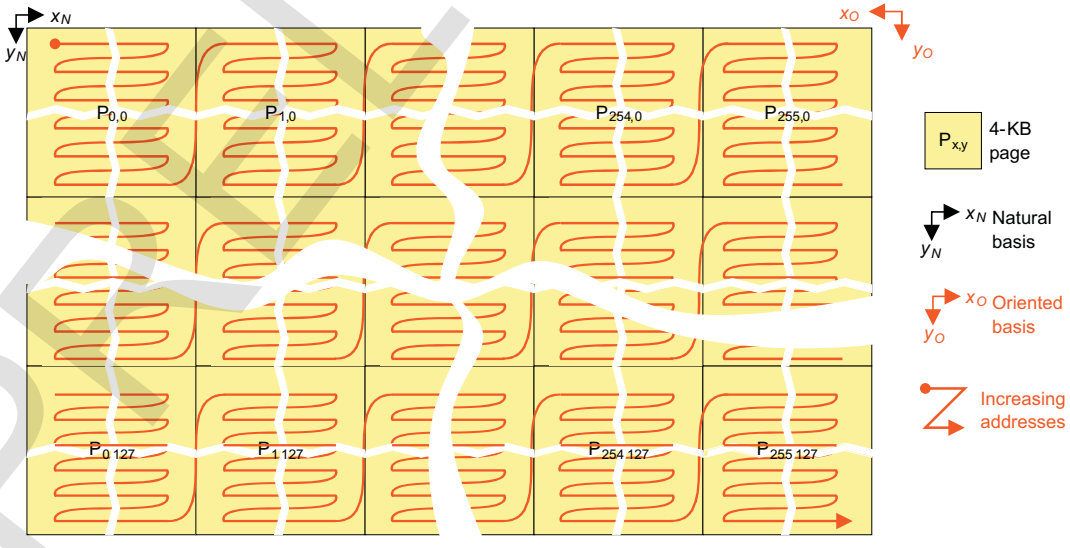
In any TILER mode, the elements are ordered from left to right and then from top to bottom in their container, as shown in Figure 15-19 and Figure 15-20.

Figure 15-19. Tiled Mode Ordering of Elements in Natural View



sdram-033

Figure 15-20. Page Mode Ordering of Elements in Natural View



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15.2.3.6.1.7.3.2 0-Degree View With Vertical Mirror or 180-Degree View With Horizontal Mirror

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(Orientation 1)

This orientation defined by S = 0, $\overline{Y}$ = 0, and $\overline{X}$ = 1 and means that the operated change of basis is:

$$\begin{cases} \vec{x}_O = -\vec{x}_N \\ \vec{y}_O = \vec{y}_N \end{cases}$$

sdram-035

In any TILER mode, the elements are then ordered from right to left and then from top to bottom in their container, as shown in Figure 15-21 and Figure 15-22.

Figure 15-21. Tiled Mode Ordering of Elements in 0-Degree View With Vertical Mirror

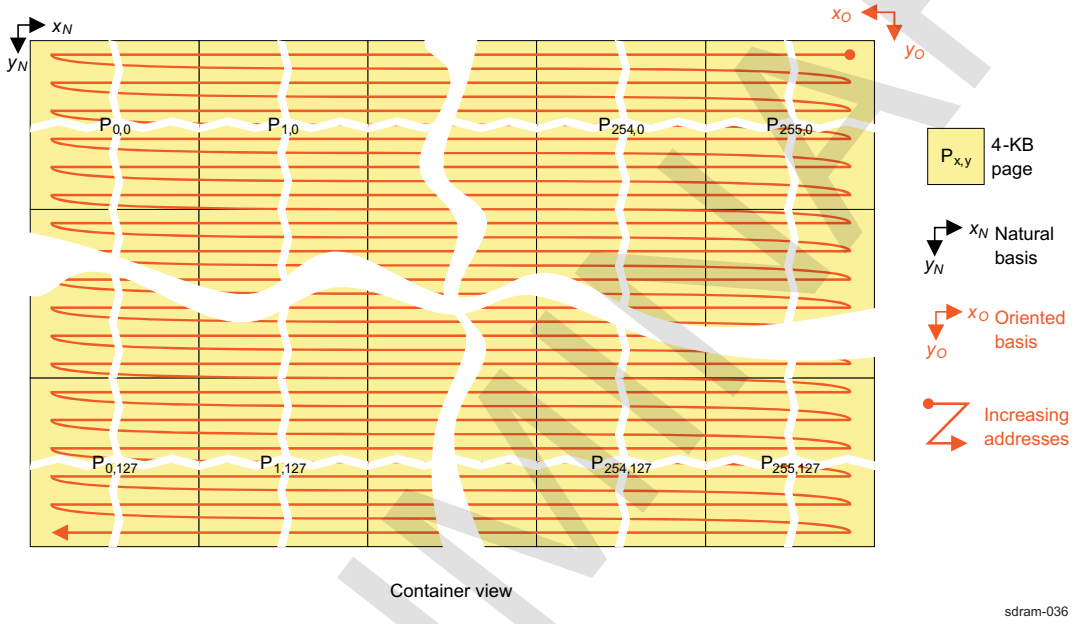
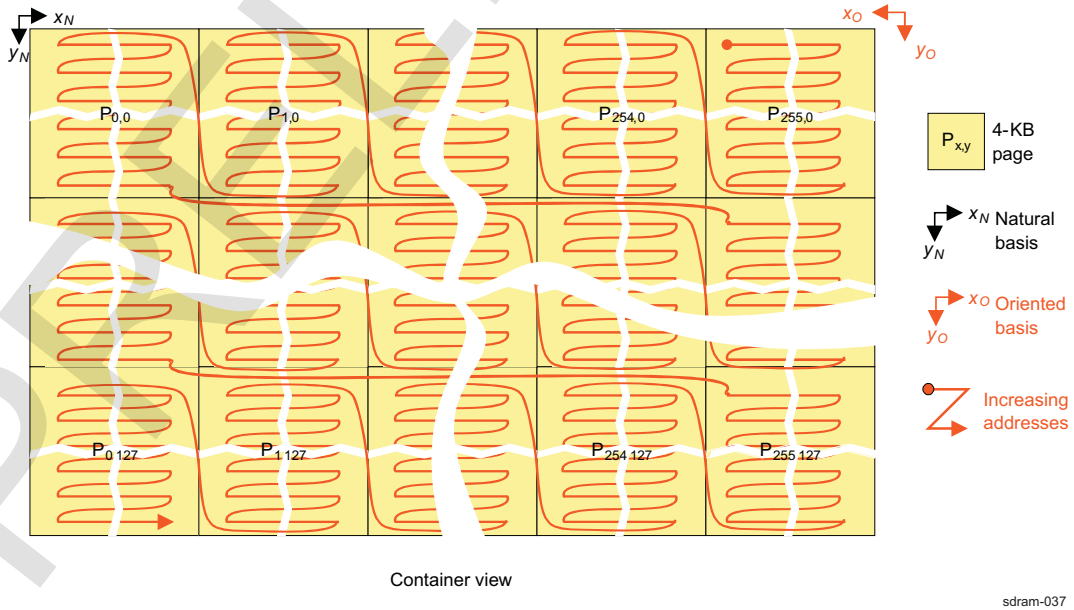


Figure 15-22. Page Mode Ordering of Elements in 0-Degree View With Vertical Mirror



15.2.3.6.1.7.3.3 0-Degree View With Horizontal Mirror or 180-Degree View With Vertical Mirror

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(Orientation 2)

This orientation defined by S = 0, $\overline{Y}$ = 1, and $\overline{X}$ = 0 and means that the operated change of basis is:

$$\begin{cases} \vec{x}_O = \vec{x}_N \\ \vec{y}_O = -\vec{y}_N \end{cases}$$

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In any TILER mode, the elements are ordered from left to right and then from bottom to top in their container, as shown in Figure 15-23 and Figure 15-24.

Figure 15-23. Tiled Mode Ordering of Elements in 0-Degree View With Horizontal Mirror

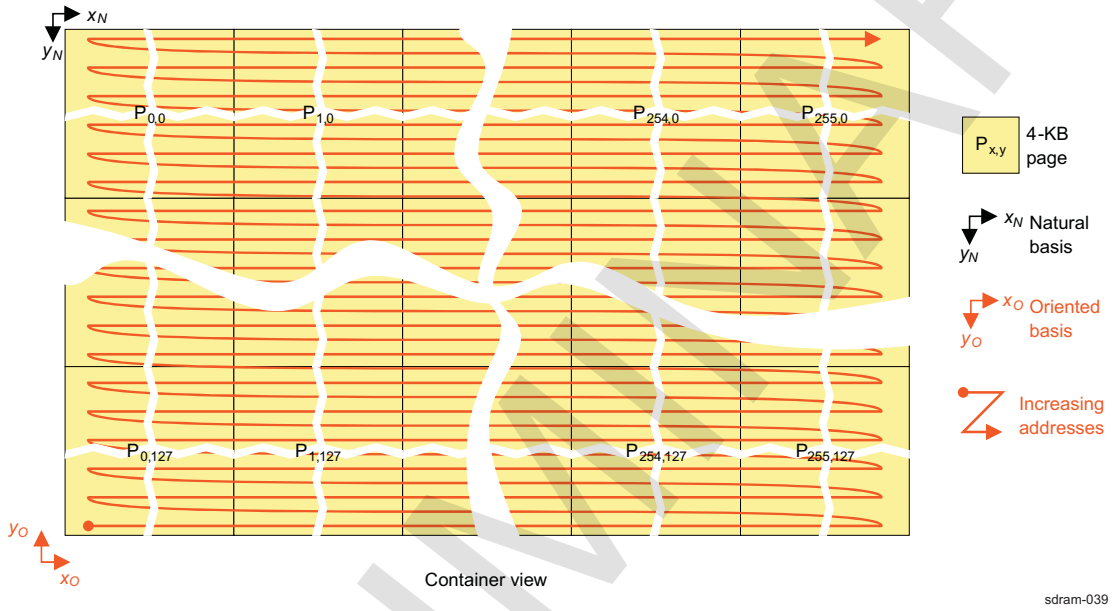
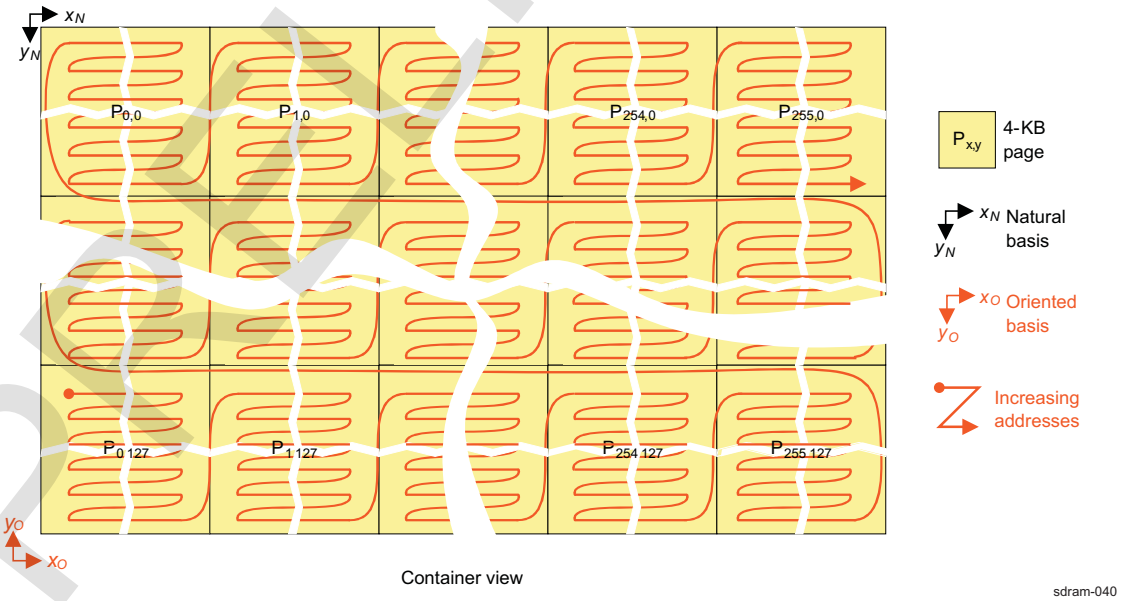


Figure 15-24. Page Mode Ordering of Elements in 0-Degree View With Horizontal Mirror



15.2.3.6.1.7.3.4 180-Degree View (Orientation 3)

This orientation defined by S = 0, $\overline{Y}$ = 1, and $\overline{X}$ = 1 and means that the operated change of basis is:

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$$\begin{cases} \vec{x}_O = -\vec{x}_N \\ \vec{y}_O = -\vec{y}_N \end{cases}$$

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In any TILER mode, the elements are ordered from right to left and then from bottom to top in their container, as shown in Figure 15-25 and Figure 15-26.

Figure 15-25. Tiled Mode Ordering of Elements in 180-Degree View

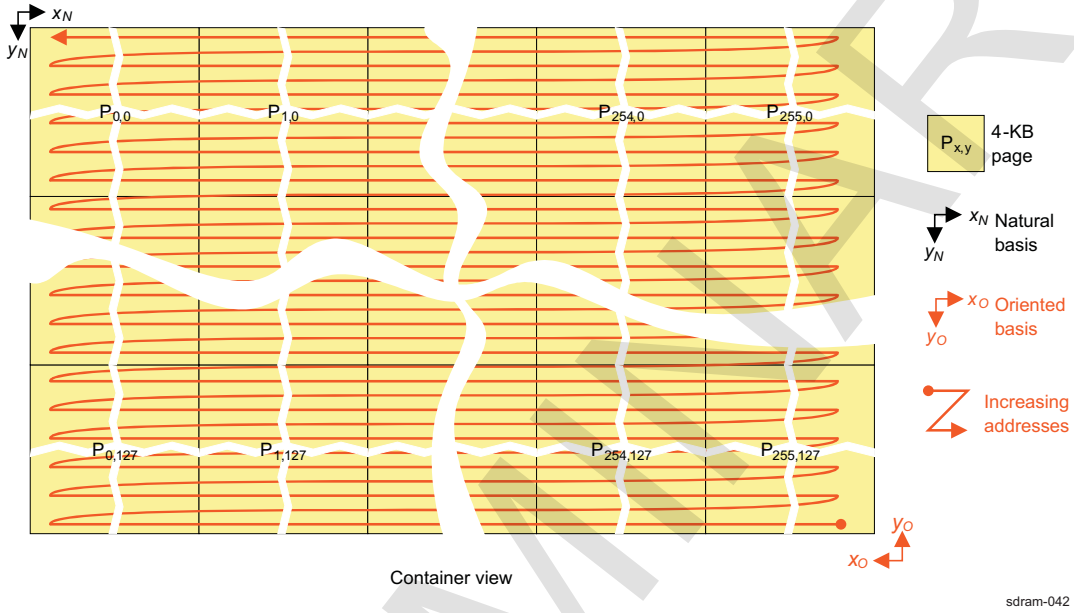
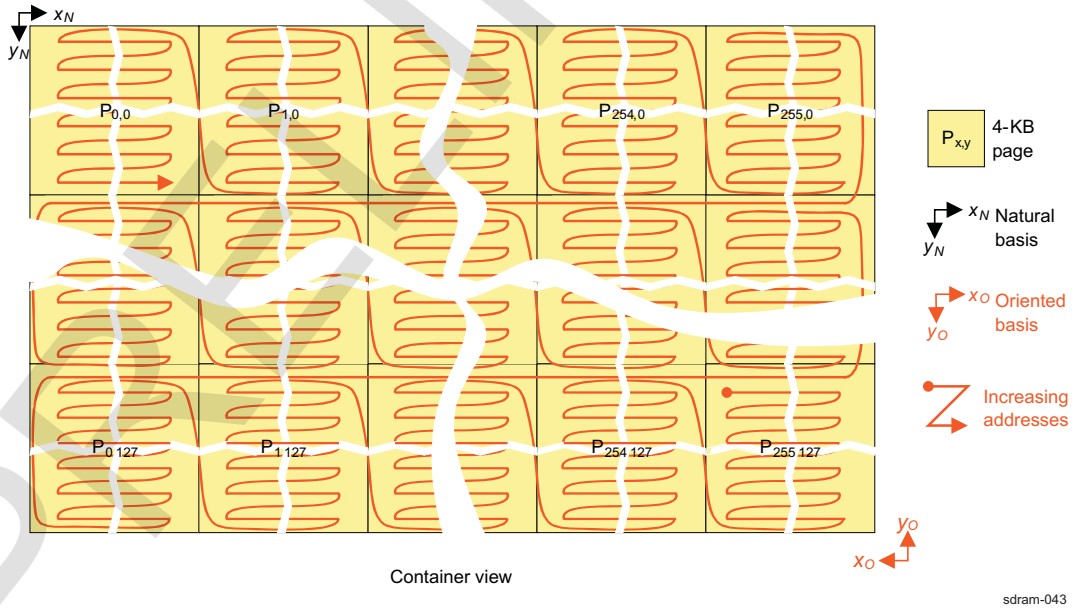


Figure 15-26. Page Mode Ordering of Elements in 180-Degree View



15.2.3.6.1.7.3.5 90-Degree View With Vertical Mirror or 270-Degree View With Horizontal Mirror (Orientation 4)

This orientation defined by S = 1, $\overline{Y}$ = 0, and $\overline{X}$ = 0 and means that the operated change of basis is:

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$$\begin{cases} \vec{x}_O = \vec{y}_N \\ \vec{y}_O = \vec{x}_N \end{cases}$$

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In any TILER mode, the elements are ordered from top to bottom and then from left to right in their container, as shown in Figure 15-27 and Figure 15-28.

Figure 15-27. Tiled Mode Ordering of Elements in 90-Degree View With Vertical Mirror

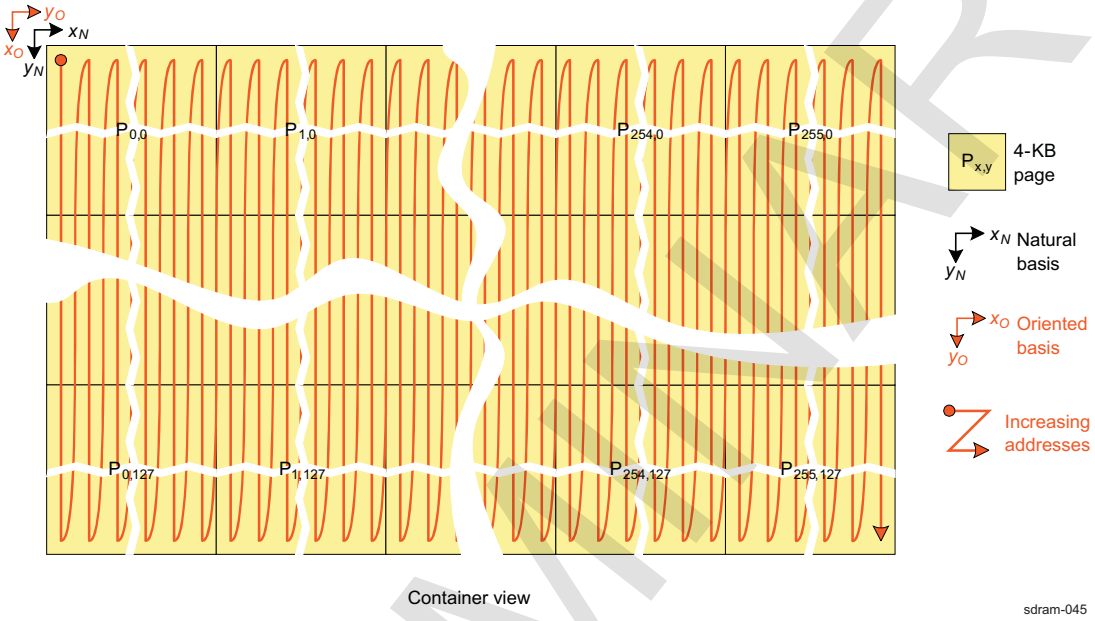
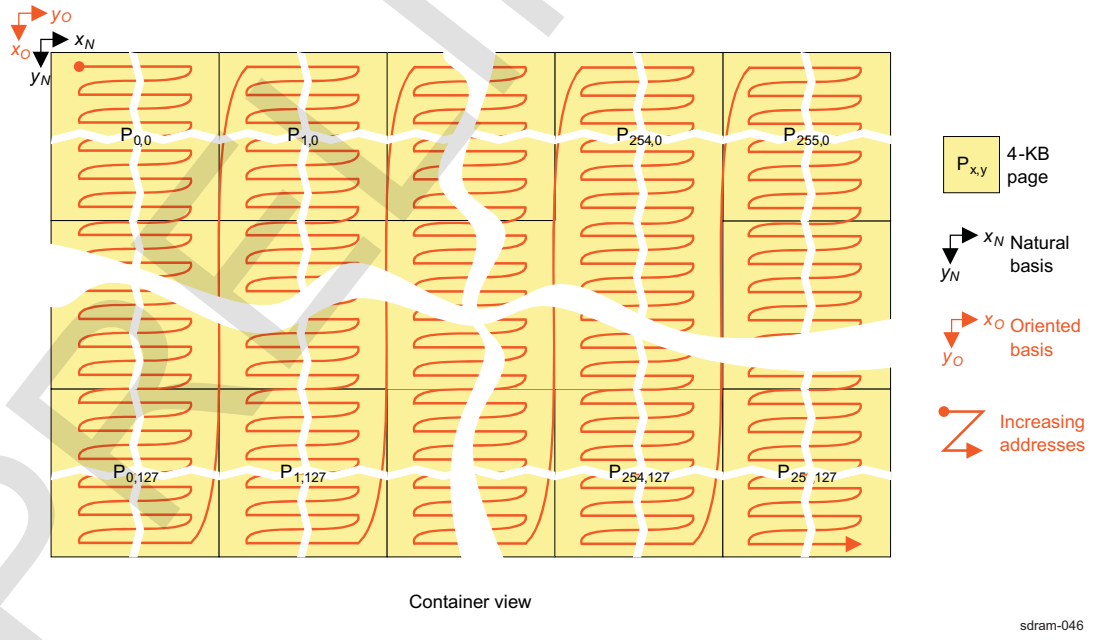


Figure 15-28. Page Mode Ordering of Elements in 90-Degree View With Vertical Mirror



15.2.3.6.1.7.3.6 270-Degree View (Orientation 5)

This orientation defined by S = 1, $\overline{Y}$ = 0, and $\overline{X}$ = 1 and means that the operated change of basis is:

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$$\begin{cases} \vec{x}_O = \vec{y}_N \\ \vec{y}_O = -\vec{x}_N \end{cases}$$

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In any TILER mode, the elements are ordered from top to bottom and then from right to left in their container, as shown in Figure 15-29 and Figure 15-30.

Figure 15-29. Tiled Mode Ordering of Elements in 270-Degree View

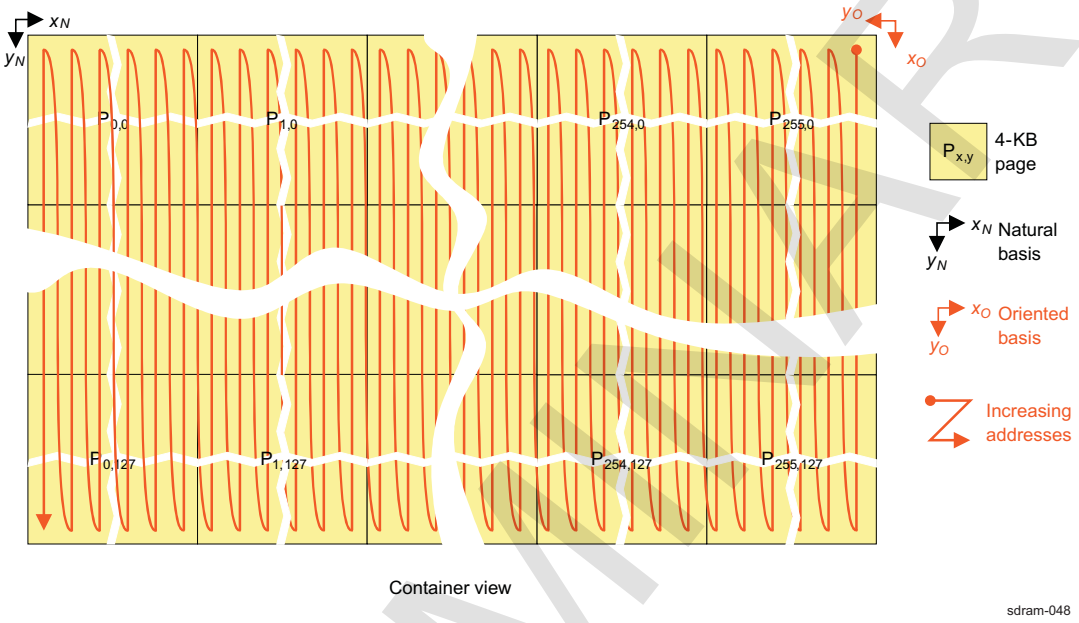
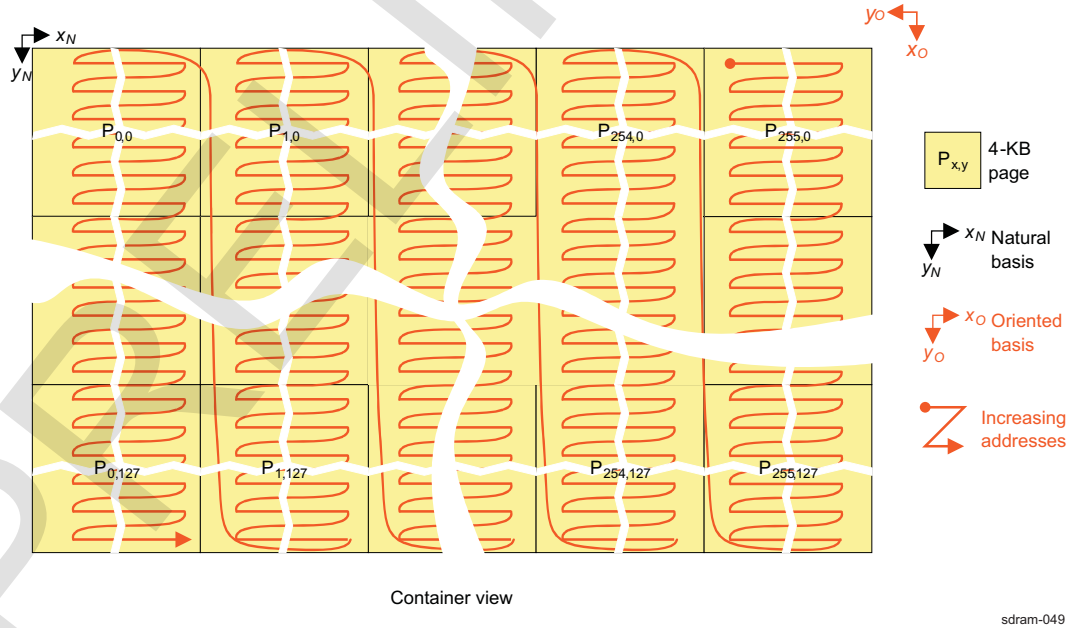


Figure 15-30. Page Mode Ordering of Elements in 270-Degree View



15.2.3.6.1.7.3.7 90-Degree View (Orientation 6)

This orientation defined by S = 1, $\overline{Y}$ = 1, and $\overline{X}$ = 0 and means that the operated change of basis is:

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$$\begin{cases} \vec{x}_O = -\vec{y}_N \\ \vec{y}_O = \vec{x}_N \end{cases}$$

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In any TILER mode, the elements are ordered from bottom to top and then from left to right in their container, as shown in Figure 15-31 and Figure 15-32.

Figure 15-31. Tiled Mode Ordering of Elements in 90-Degree View

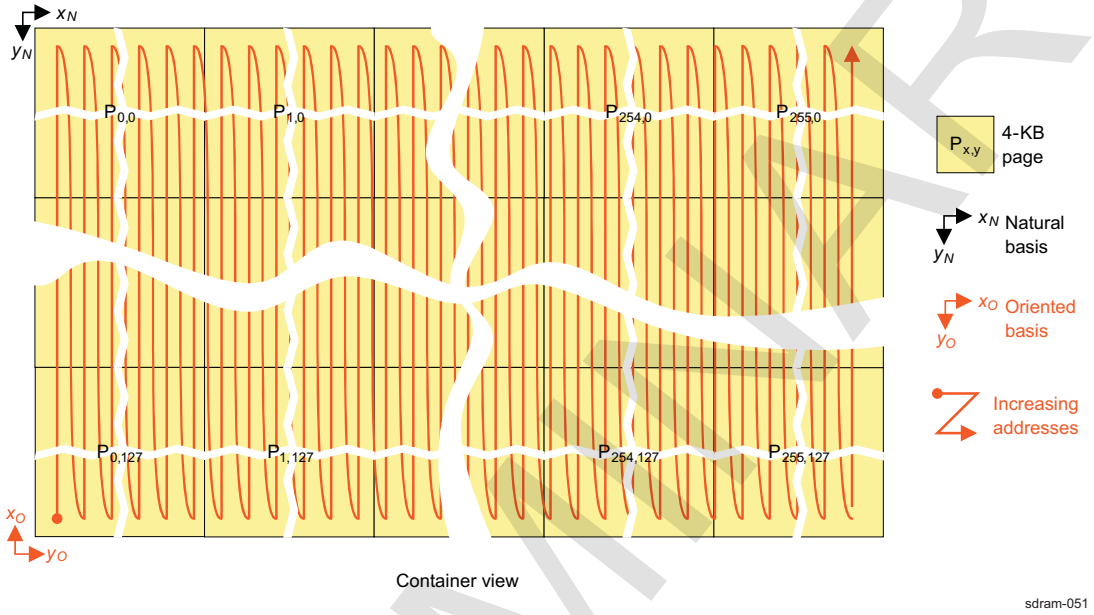
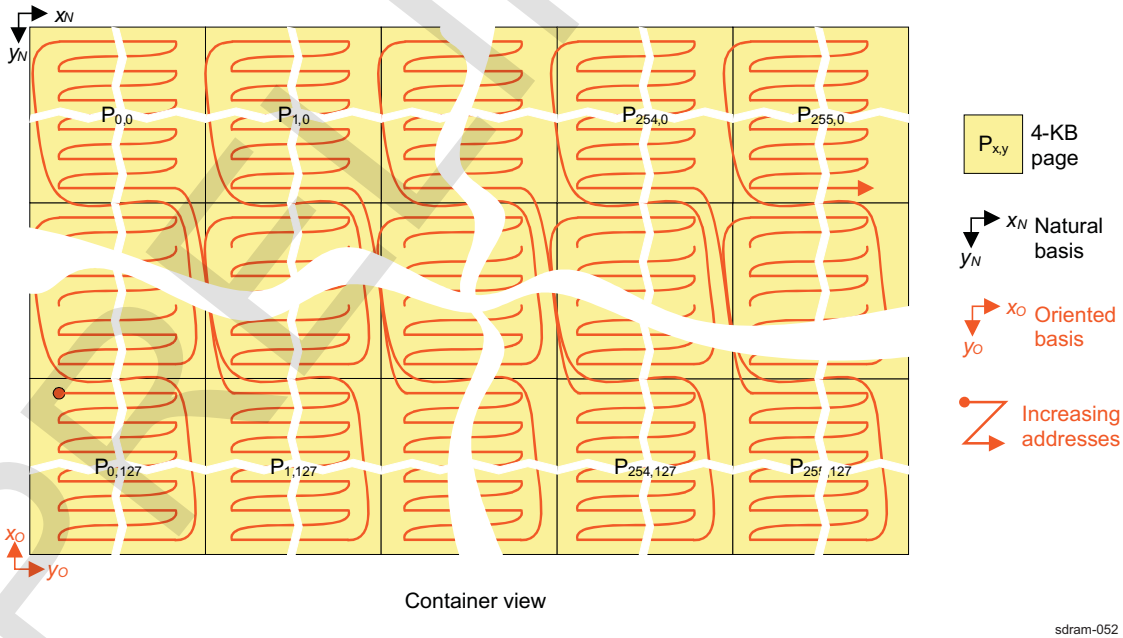


Figure 15-32. Page Mode Ordering of Elements in 90-Degree View



15.2.3.6.1.7.3.8 90-Degree View With Horizontal Mirror or 270-Degree View With Vertical Mirror (Orientation 7)

This orientation defined by S = 1, $\overline{Y}$ = 1, and $\overline{X}$ = 1 and means that the operated change of basis is:

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$$\begin{cases} \vec{x}_O = -\vec{y}_N \\ \vec{y}_O = -\vec{x}_N \end{cases}$$

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In any TILER mode, the elements are ordered from bottom to top and then from right to left in their container, as shown in Figure 15-33 and Figure 15-34.

Figure 15-33. Tiled Mode Ordering of Elements in 90-Degree View With Horizontal Mirror

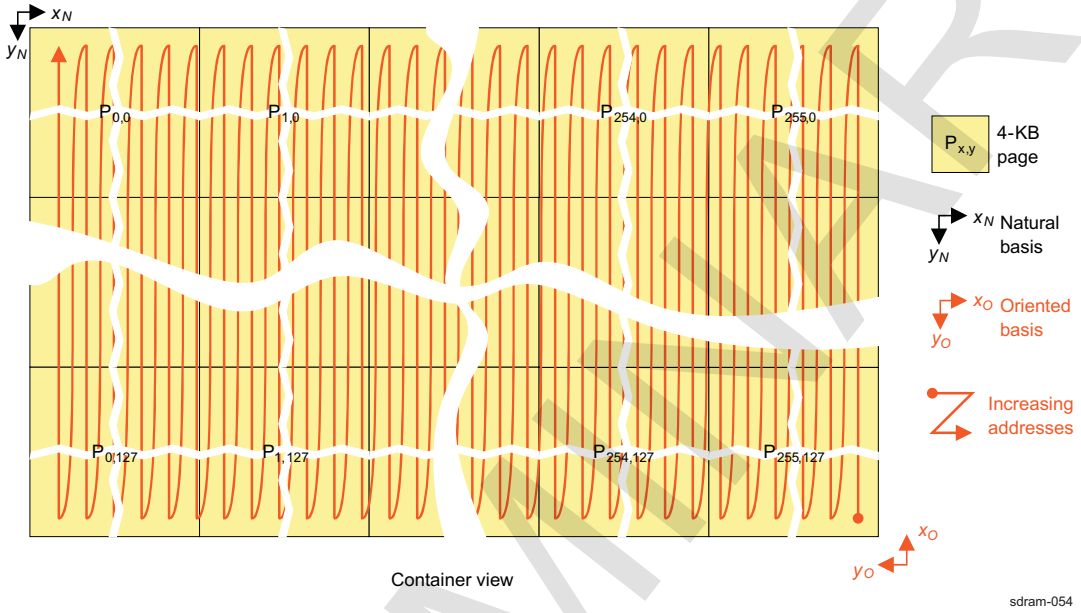
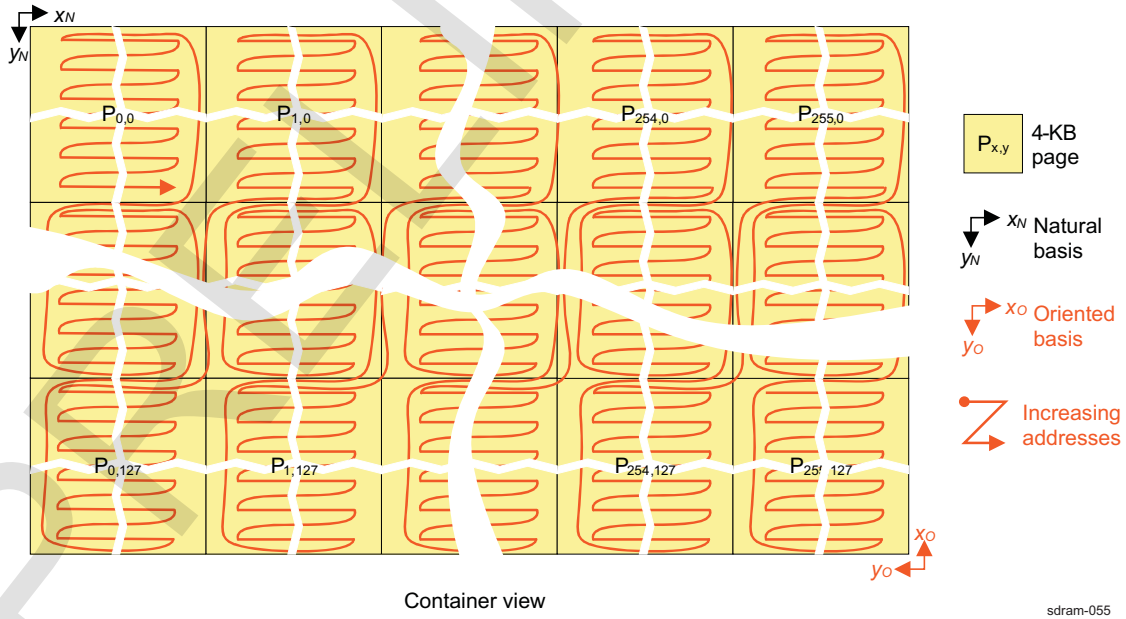


Figure 15-34. Page Mode Ordering of Elements in 90-Degree View With Horizontal Mirror



15.2.3.6.2 TILER Macro-Architecture

The TILER requires a 4-GiB addressing space to map its 128-MiB physical container in four modes and

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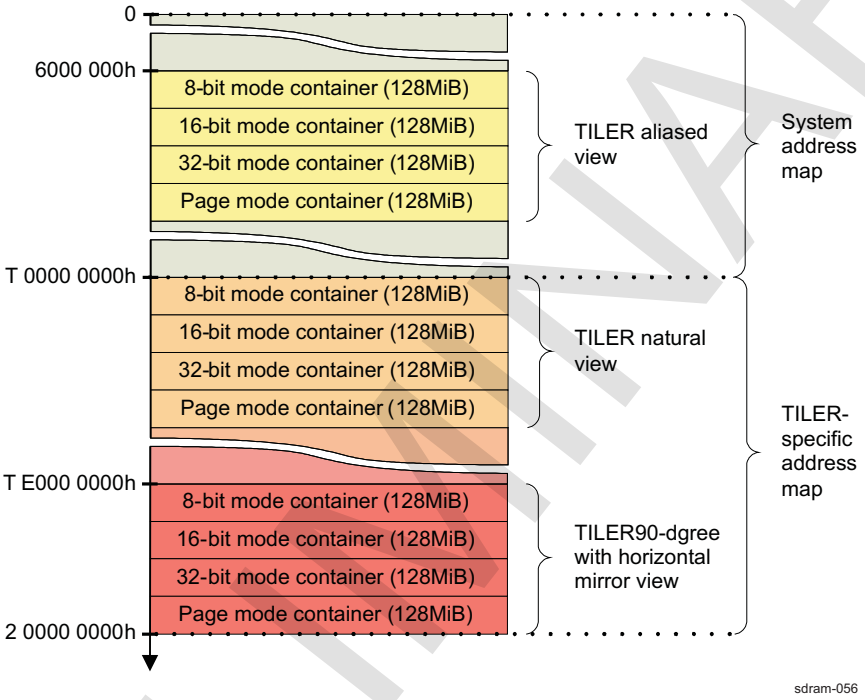
eight orientations. Because its addressing space alone fills the 4-GiB global system address map, the TILER addressing space cannot enter as-is into the system address map. Besides, putting in place a register-based mechanism per initiator to specify the orientation of the following accesses and then reducing the TILER addressing space to a single 512-MiB view is not an option; this is because most of the bandwidth-hungry initiators require simultaneous accesses to the TILER container in different views.

As a result, 32 bits are not enough to address all these requests, because the TILER port must convey not only virtually addressed requests to the "oriented" TILER containers but also physically addressed requests to the attached SDRCs. A thirty-third address bit is necessary to distinguish the two separated address maps, as shown in Figure 15-35.

Figure 15-35. TILER Port Address Map



Still, having separated systems and TILER-specific address maps is not sufficient. In a system many existing and external IP blocks still rely on a 32-bit address and would then be limited to one or the other 4-GiB addressing space. To overcome this limitation, one 512-MiB view is aliased in the system address map as (see Table 15-13 and Figure 15-36).

Table 15-13. TILER Aliased View in the L3 Interconnect Mapping

Start Address (hex)	End Address (hex)	Size
0x6000_0000	0x7FFF_FFFF	512MB

From all incoming requests, TILER requests are filtered as having an address that fits one of the following:

- The address format in the TILER-specific address map given in Table 15-14, or
- The address format of the aliased view in the system address map given in Table 15-15; other requests are forwarded directly to the SDRC in TILER bypass mode.

Table 15-14. Address Format in the TILER-Specific Address Map

32	31	30	29	28	27	26 ... 4	3 ... 0
T	Orientation			Mode		Virtual address	
1	S	$\overline{Y}$	$\overline{X}$	M1	M0	A26 ... A4	0

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Table 15-15. Address Format of the TILER Aliased View in the System Address Map

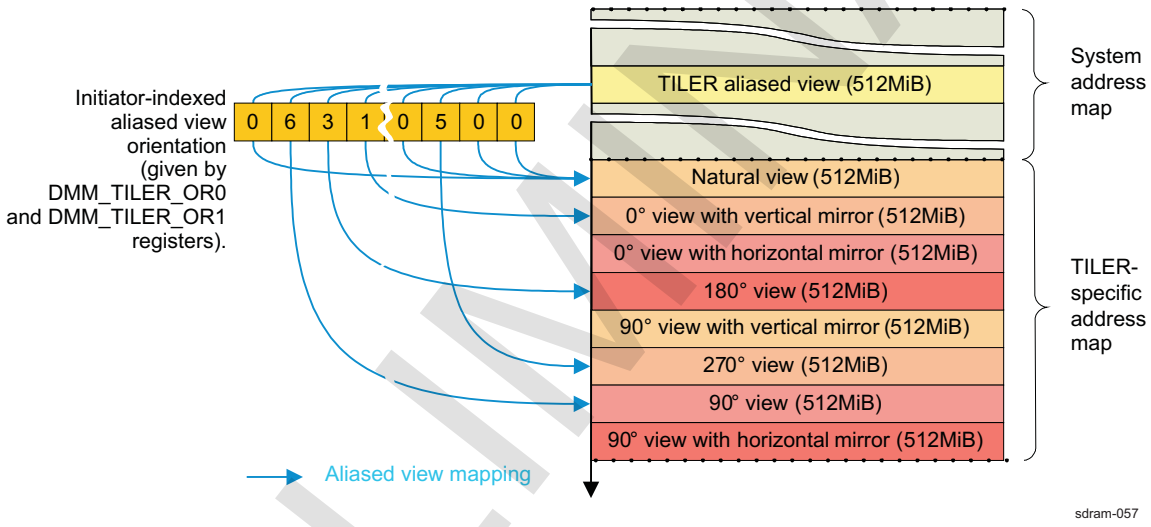
32	31	30	29	28	27	26 ... 4	3 ... 0
T	TILER aliasing			Mode		Virtual address	
0	0	1	1	M1	M0	A26 ... A4	0

In these address formats:

- The thirty-third bit, noted T, is aimed at distinguishing the standard 4-GiB system address map from the 4-GiB TILER-specific address map.
- The orientation bits, noted S, $\overline{Y}$, and $\overline{X}$, define the request orientation, as specified in Table 15-11.
- The mode bits, noted M1 and M0, define the request mode, as specified in Table 15-10.
- The remaining 27 bits, noted A0 to A26, define the mode and orientation specific virtual address, as defined in Figure 15-16, Figure 15-17, and Figure 15-18.

The orientation of the aliased TILER view is extracted from an initiator-indexed LUT, as shown in Figure 15-36.

Figure 15-36. TILER Aliased View Orientation



As shown in Figure 15-36, an internal initiator-indexed LUT stores the current orientation of the aliased view for each initiator.

When an interconnect request hits the TILER aliased view in the system address map, the request initiator orientation is extracted from the LUT and the request address is translated according to this orientation: the T bit is set and bits [31:29] are replaced with the orientation.

Regarding the dimensioning of this LUT, given that initiators simultaneously accessing multiple views use the TILER-specific address map, and many initiators do not need to access any view or can be restricted to accessing only the natural view, only a limited number of initiators are likely to dynamically modify the orientation of its aliased TILER view.

The orientation LUT is limited to 16 entries. These 16 orientation entries are mapped on the two 32-bit DMM_TILER_OR0 and DMM_TILER_OR1 registers.

The first eight entries of the LUT are mapped in the DMM_TILER_OR0 register, and the last eight entries are mapped in the DMM_TILER_OR1 register. Therefore, given an index x, the orientation related to this index is given in the ORx field.

Each of these registers is split into eight 4-bit fields, each field mapping an entry of the LUT with:

- An S, $\overline{Y}$, $\overline{X}$ orientation code on the 3 LSBs
- An $\overline{W}$ field-specific active-low local write-enable bit, always read as 0, on the MSB.

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The registers fields that correspond to initiators that do not need any dynamic configuration of their aliased view orientation must be specified as reserved fields, and only written with zeros.

The $\overline{W}$ bit allows the modification of a single entry without requiring a read-modify-write sequence. This approach is then more accommodating:

- In a system where multiple initiators can modify their own fields in the registers
- With initiators unable to make the read-modify-write sequence, such as DMA

Still, the $\overline{W}$ bit is active-low to keep the compatibility with the usual read-modify-write sequence. When reading an aliased view orientation register, because all its $\overline{W}$ bits are read as 0, if these bits are untouched by the modification—as they should be—writing back the modified register updates all orientation fields of the register.

15.2.3.6.3 TILER Guidelines for Initiators

15.2.3.6.3.1 Buffered Raster-Based Initiators

15.2.3.6.3.1.1 Buffer Size

The necessary minimum buffer size depends on the SDRAM prefetch size and on initiator support in terms of the following:

- Element size
- Orientation
- Maximum number of elements per line in all supported element sizes and orientations

Let N be the maximum number of elements per line for a given mode (element size) and orientation, P be the SDRAM memory prefetch size in bytes, and *max* be the function returning the maximum of the two parameters. The minimum necessary line buffer size to handle all resolutions in a given mode and orientation is listed in Table 15-16.

Table 15-16. Minimum Buffer Size to Efficiently Handle Lines of up to N Elements

	0- or 180- Degree Orientation (S = 0)	90- or 270-Degree Orientation (S = 1)
8-bit mode	4 x N bytes	*max* (4,P/4) x N bytes
16-bit mode	None	*max* (8,P/2) x N bytes
32-bit mode	None	*max* (8,P/2) x N bytes

This minimal buffer size can be reached only with an advanced FIFO management scheme. The standard ping-pong buffer requires twice this buffer size.

NOTE: Given their nature, field accesses to an interlaced frame-buffer require buffers twice as small as in the standard progressive case.

For instance, an initiator that must handle only a single progressive frame-buffer in any orientation of:

- Up to 1920 × 1080 in YUV4:2:0
- Up to 1600 × 1200 in 16-bit RGB565
- Up to 800 × 600 in 32-bit ARGB

requires a line buffer of at least 15,360 bytes because:

- 4 × 1920 + 4 × 2960 = 15,360 bytes required for a 3-plane YUV4:2:0 frame of 1920 × 1080
- 4 × 1920 + 8 × 960 = 15,360 bytes required for a 2-plane YUV4:2:0 frame of 1920 × 1080
- 8 × 1600 = 12,800 bytes required for a 16-bit RGB565 frame of 1600 × 1200
- 8 × 800 = 6400 bytes required for a 32-bit ARGB frame of 800 × 600

and a line buffer of at least 30,720 bytes when using a simple ping-pong buffer scheme.

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15.2.3.6.3.1.2 Performance

Table 15-17 gives the ratio of effective data to transferred data at the external memory interface for buffered raster-based initiators in each mode and orientation, when using an up-to-32-bit DDR, lpDDR, or lpDDR2 SDRAM, or an up-to-16-bit DDR2 memory.

Table 15-17. Memory Data Payload for Buffered Raster-Based Initiators on Up-to-32-Bit DDR, lpDDR, or lpDDR2

	0- or 180-Degree Orientation (S = 0)		90- or 270-Degree Orientation (S = 1)	
	Progressive	Interlaced	Progressive	Interlaced
8-bit mode	100%	100%	100%	50%
16-bit mode	100%	100%	100%	50%
32-bit mode	100%	100%	100%	50%
Page mode	100%	N/A	100%	100%

When using 32-bit DDR, lpDDR, or lpDDR2 SDRAMs, or 16-bit DDR, DDR2, lpDDR, or lpDDR2 memories, whenever all previous guidelines are fulfilled, there is no penalty for these initiators to access a tiled object in any orientation, except for accesses to an interlaced frame in 90- or 270-degree orientation where the memory bandwidth is twice the requested bandwidth.

When using up-to-32-bit DDR, lpDDR, lpDDR2, or up-to-16-bit DDR2 SDRAMs, all accesses, except interlaced accesses in a 90- or 270-degree orientation, are equally efficient and offer the full possible memory bandwidth.

Because of its progressive nature, page mode does not introduce any performance hit.

Table 15-18 lists the ratio of effective data-to-transferred data at the external memory interface for the buffered raster-based initiators in each mode and orientation when using a 32-bit DDR2 or DDR3 memory.

Table 15-18. Memory Data Payload for Buffered Raster-Based Initiators on 32-Bit DDR2 or DDR3

	0- or 180-Degree Orientation (S = 0)		90- or 270-Degree Orientation (S = 1)	
	Progressive	Interlaced	Progressive	Interlaced
8-bit mode	100%	50%	100%	50%
16-bit mode	100%	50%	100%	50%
32-bit mode	100%	50%	100%	50%
Page mode	100%	N/A	100%	100%

When using 32-bit DDR2 or DDR3 SDRAMs, whenever all previous guidelines are fulfilled, there is no penalty for these initiators to access a tiled object in any orientation, except for accesses to an interlaced frame in any orientation where the memory bandwidth is twice the requested bandwidth.

When using DDR2 or DDR3 SDRAMs, all accesses, except interlaced accesses, are equally efficient and offer the full possible memory bandwidth.

Similarly, page mode does not introduce any performance hit.

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15.2.4 DMM Use Cases and Tips

15.2.4.1 PAT Use Cases

Five ways to use PAT are:

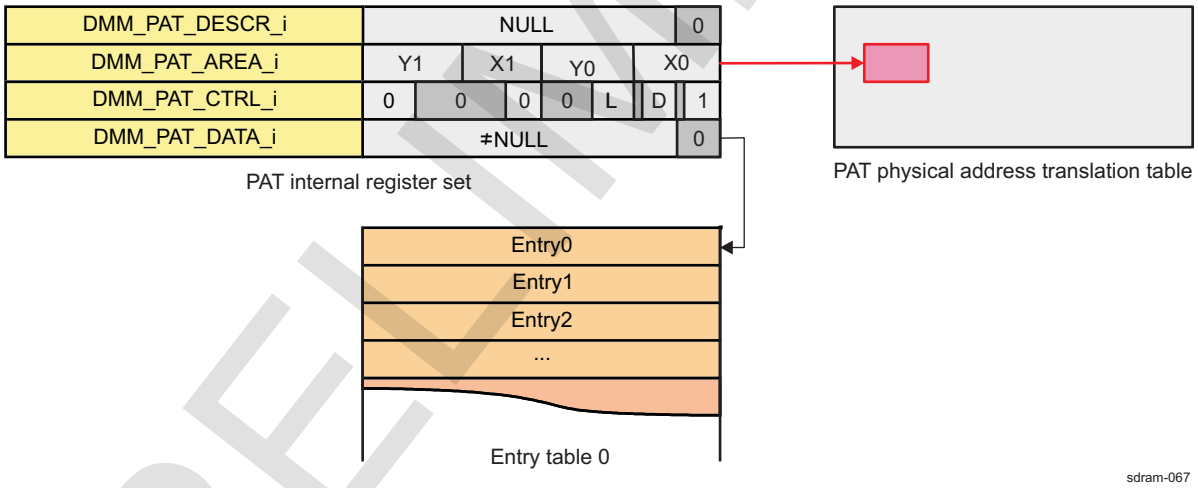
- Simple manual area refill
- Single auto-configured area refill
- Chained auto-configured area refill
- Synchronized auto-configured area refill
- Cyclic synchronized auto-configured area refill

15.2.4.1.1 Simple Manual Area Refill

The following must be performed to create a 16-byte aligned memory-mapped entry table containing all entries of the defined area (see Figure 15-37):

1. Write the DMM_PAT_AREA_i register with the relevant (x0, y0) (x1, y1) area definition.
2. Write the DMM_PAT_DATA_i register with the physical address of the created entry table.
3. Write the DMM_PAT_CTRL_i register with the requested refill direction and assert the DMM_PAT_CTRL_i[0] START bit with the requested refill direction D and with the LUT ID L if multiple LUTs are present in the system.
4. The refill is done when the DMM_PAT_STATUS_i[3] DONE bit is set.
5. A new refill can be initiated when the DMM_PAT_STATUS_i[0] READY bit is set.

Figure 15-37. Simple Manual Area Refill Scheme



15.2.4.1.2 Single Auto-Configured Area Refill

The following must be performed to create a 16-byte aligned memory-mapped entry table containing all entries of the defined area (see Figure 15-38):

1. Create a 16-byte aligned memory-mapped descriptor structure where:
   - The next field is set to NULL.
   - The area field is set with the relevant (x0, y0) (x1, y1) area definition.
   - The ctrl field is set with the requested direction D, with the requested LUT ID L if multiple LUTs are present in the system, and the START bit is asserted to start refilling as soon as this descriptor enters the PAT refill engine.
   - The data field is set to the physical address of the created entry table.
2. Write the DMM_PAT_DESCR_i register with the physical address of the created descriptor.
3. The refill is done when the DMM_PAT_STATUS_i[3] DONE bit is set.

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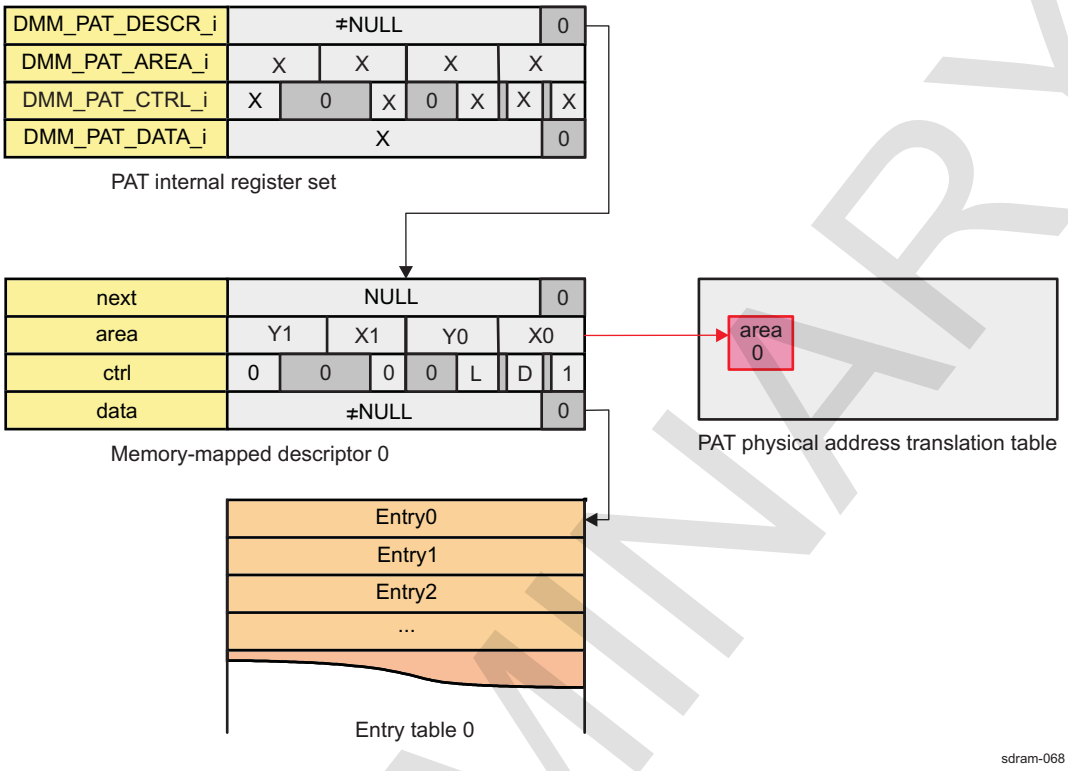
4. A new refill can be initiated when the DMM_PAT_STATUS_i[0] READY bit is set.

Figure 15-38. Single Auto-Configured Area Refill Scheme



15.2.4.1.3 Chained Auto-Configured Area Refill

The following must be performed to create one 16-byte aligned memory-mapped entry table per area containing the entries for the corresponding area (see Figure 15-39):

1. Create one 16-byte aligned memory-mapped descriptor structure per area where:
   - The next field is set to the physical address of the next descriptor or NULL for the last one.
   - The area field is set with the relevant (x0, y0) (x1, y1) area definition.
   - The ctrl field is set with the requested direction D, with the requested LUT ID L if multiple LUTs are present in the system, and the START bit is asserted to start refilling as soon as the previous area refill is done.
   - The data field is set to the physical address of the corresponding entry table.
2. Write the DMM_PAT_DESCR_i register with the physical address of the first created descriptor.
3. Each area refill is done when the DMM_PAT_STATUS_i[3] DONE bit is set.
4. All area refills are done when the DMM_PAT_STATUS_i[0] READY bit is set.
5. A new refill can be initiated when the DMM_PAT_STATUS_i[0] READY bit is set.

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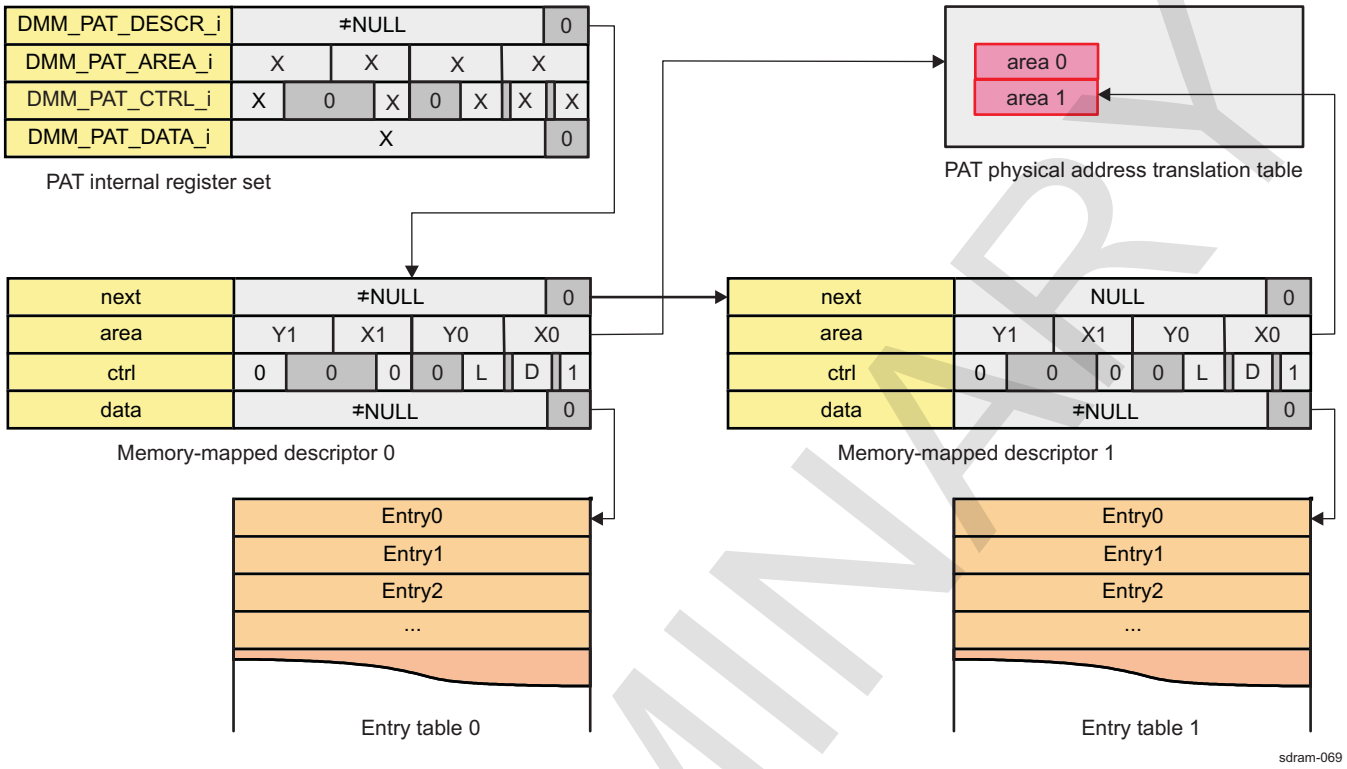
Figure 15-39. Chained Auto-Configured Area Refill Scheme



15.2.4.1.4 Synchronized Auto-Configured Area Refill

The following must be performed to create one 16-byte aligned memory-mapped entry table per area containing the entries for the corresponding area (see Figure 15-40):

1. Create one 16-byte aligned memory-mapped descriptor structure per area where:
   - The next field is set to the physical address of the next descriptor or NULL for the last one.
   - The area field is set with the relevant (x0, y0) (x1, y1) area definition.
   - The ctrl field is set with the synchronizing initiator identifier I, the SYNC bit is asserted, the requested direction D and the requested LUT ID L if multiple LUTs are present in the system, and the START bit is asserted to start refilling as soon as the previous area refill is done and initiator I has made one access in the previous area.
   - The data field is set to the physical address of the corresponding entry table.
2. Write the DMM_PAT_DESCR_i register with the physical address of the first created descriptor.
3. Each area refill is done when the DMM_PAT_STATUS_i[3] DONE bit is set.
4. All area refills are done when the DMM_PAT_STATUS_i[0] READY bit is set.
5. A new refill can be initiated when the DMM_PAT_STATUS_i[0] READY bit is set.

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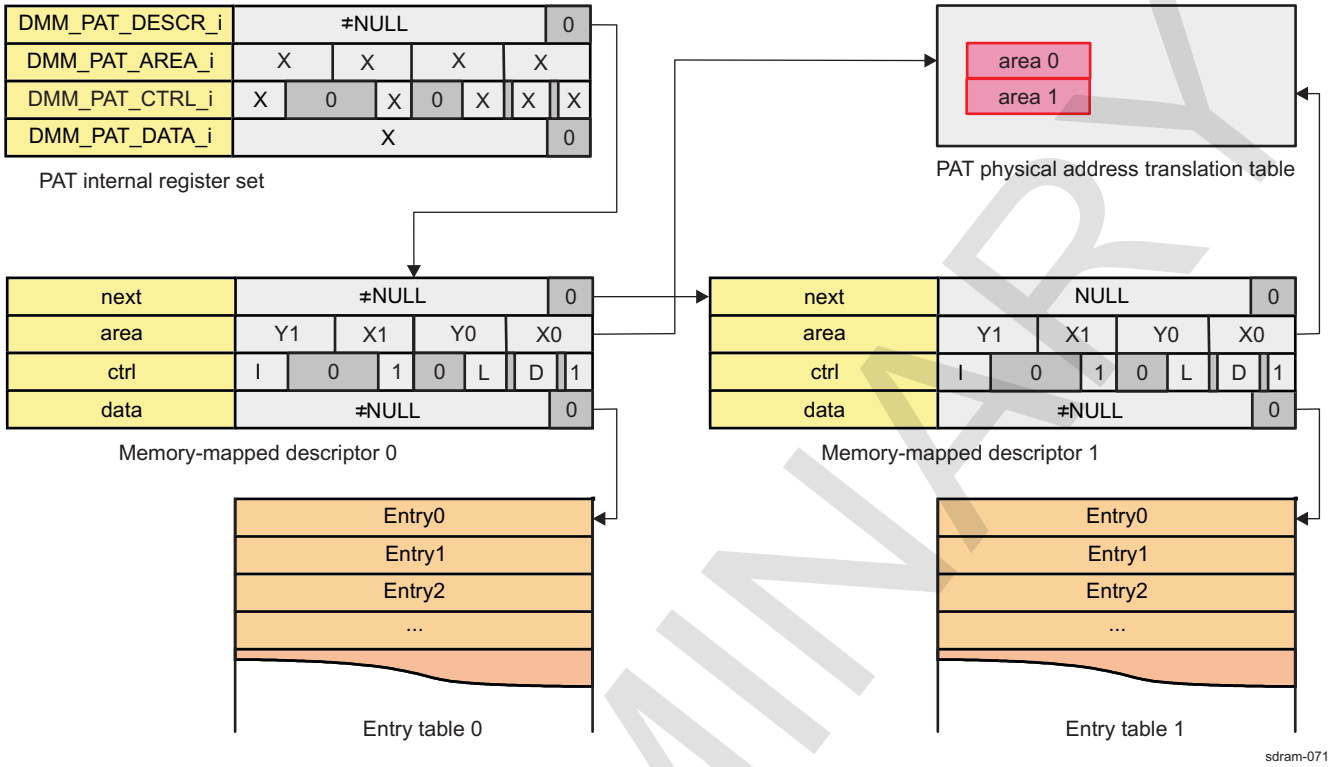
Figure 15-40. Synchronized Auto-Configured Area Refill Scheme



15.2.4.1.5 Cyclic Synchronized Auto-Configured Area Refill

The following must be performed to create one 16-byte aligned memory-mapped entry table per area containing the entries for the corresponding area (see Figure 15-41):

1. Create one 16-byte aligned memory-mapped descriptor structure per area where:
   - The next field is set to the physical address of the next descriptor in the circular list.
   - The area field is set with the relevant (x0, y0) (x1, y1) area definition.
   - The control field is set with the synchronizing initiator identifier I, the SYNC bit asserted, the requested direction D and requested LUT ID L if multiple LUTs are present in the system, and the START bit is asserted to start refilling as soon as the previous area refill is done and initiator I has made one access in the previous area.
   - The data field is set to the physical address of the corresponding entry table.
2. Write the DMM_PAT_DESCR_i register with the physical address of the initial descriptor.
3. Each area refill is done when the DMM_PAT_STATUS_i[3] DONE bit is set.
4. A new refill can be initiated by writing any value to the DMM_PAT_DESCR_i register to abort the current one.

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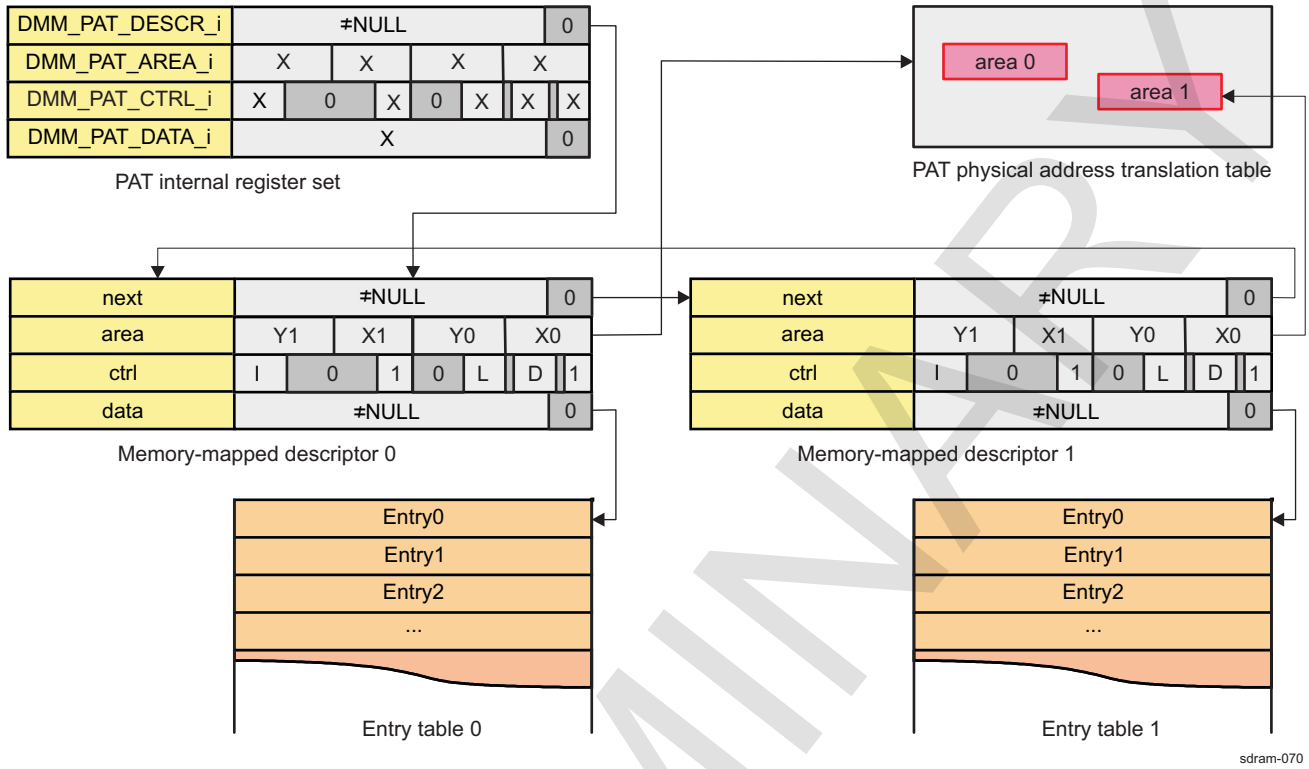
Figure 15-41. Cyclic Synchronized Auto-Configured Area Refill Scheme



NOTE: Never use circular lists of descriptors where all descriptors have the DMM_PAT_CTRL_i[0] START bit set and there is no synchronization. This leads to an endless continuous refill.

15.2.4.2 Addressing Management with LISA

The device has two memory controllers (EMIFs) and one address space per memory controller.

15.2.4.2.1 Case 1: Use of One Memory Controller

In this example, assume there is 1GB of external memory evenly spread onto two address spaces. The address range for address space 0 must start at offset 0x4000_0000 (see Table 15-19).

Table 15-19. Address Definition

Address Range	Memory Controller	Memory Controller Address Range
0x8000_0000 to 0x9FFF_FFFF	0x1	0x0000_0000 to 0x0FFF_FFFF
0xA000_0000 to 0xBFFF_FFFF	0x0	0x4000_0000 to 0x5FFF_FFFF

This configuration requires two nonoverlapping sections to be set. They can be defined in any order because there is no concern with priority in this case (see Table 15-20):

Table 15-20. Configuration

Bit Field	Section 0 (DMM_LISA_MAP_0)	Section 1 (DMM_LISA_MAP_1)
[31:24] SYS_ADDR	0x80	0xA0
[22:20] SYS_SIZE	0x5	0x5
[19:18] SDRC_INTL	0x0 (not applicable)	0x0 (not applicable)
[17:16] SDRC_ADDRSPC	0x1	0x0

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Table 15-20. Configuration (continued)

Bit Field	Section 0 (DMM_LISA_MAP_0)	Section 1 (DMM_LISA_MAP_1)
[8] SDRC_MAP	0x1	0x1
[7:0] SDRC_ADDR	0x00	0x40

To check whether an address hits a section, use the 8 upper address bits of the address and mask them with the hit mask: $28–2^{SYS_SIZE}$. If the result is equal to SYS_ADDR, the section is hit.

To define the physical address to be issued to the memory controller, use the 8 upper address bits of the system address, mask them with the address mask: $2^{SYS_SIZE}–1$, and OR them with SDRC_ADDR. This gives the resulting 8 upper physical address bits. All lower address bits are forwarded unchanged.

Request to address 0x99AE_37F0:

- Upper address bits: 0x99
- Hit mask: 28–25 = 0xE0
- Masked upper address bits: 0x80 – hits section 0
- Address mask: 25–1 = 0x1F
- Masked upper address bits: 0x19
- OR with SDRC_ADDR: 0x19
- Physical address: 0x19AE_37F0

This request is forwarded to address 0x19AE_37F0, address space 1 of the memory controller.

Request to address 0xB7FF_0340:

- Upper address bits: 0xB7
- Hit mask: 28–25 = 0xE0
- Masked upper address bits: 0xA0 – hits section 1
- Address mask: 25–1 = 0x1F
- Masked upper address bits: 0x17
- OR with SDRC_ADDR: 0x57
- Physical address: 0x57FF_0340

This request is forwarded to address 0x57FF_0340, address space 0 of the memory controller.

15.2.4.2.2 Case 2: Use of Two Memory Controllers

In the case of 512MB interleaved at 256-B boundaries and 256MB noninterleaved on the second memory controller, the following results (see Table 15-21):

Table 15-21. Address Definition

Address Range	Memory Controller	Memory Controller Address Space	Memory Controller Address Range
0x8000_0000 to 0x9FFF_FFFF	1 and 2, interleaved at 256-byte boundaries	0 on both controllers	0x0000_0000 to 0x0FFF_FFFF on both controllers
0xA000_0000 to 0xAFFF_FFFF	Two only	0	0x1000_0000 to 0x1FFF_FFFF

Two sections are used to map such a configuration, see Table 15-22:

Table 15-22. Configuration

Bit Field	Section 0 (DMM_LISA_MAP_0)	Section 1 (DMM_LISA_MAP_1)
[31:24] SYS_ADDR	0x80	0xA0
[22:20] SYS_SIZE	0x5	0x4
[19:18] SDRC_INTL	0x2	0x0 (not applicable)

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Table 15-22. Configuration (continued)

Bit Field	Section 0 (DMM_LISA_MAP_0)	Section 1 (DMM_LISA_MAP_1)
[17:16] SDRC_ADDRSPC	0x0	0x0
[8] SDRC_MAP	0x3	0x2
[7:0] SDRC_ADDR	0x00	0x10

Detecting a section hit is the same for the interleaved case as for the single controller case: to check whether an address hits a section, use the 8 upper address bits of the address and mask them with the hit mask: $28–2^{SYS_SIZE}$. If the result is equal to SYS_ADDR, the section is hit.

The physical address generation is modified for the interleaved case. In case of 256-byte interleaving, the first chunk of 256 bytes is mapped to the first controller, the second chunk to the second controller, and so on. This results in system address bit 8 to be decoded as the controller indicator, 0 for the first controller, and 1 for the second controller (system address bit 7 is used for interleaving at the 128-byte boundary, and bit 9 for 512 bytes). This bit is not included in the computed physical address, meaning the upper system address bits [31:9] are shifted to bits [30:8] when generating the physical address.

The rest of the address generation is handled the same as for the single controller case: to define the physical address to be issued to the memory controller, use the 8 upper address bits of the system address, mask them with the address mask: $2^{SYS_SIZE}–1$, and OR them with SDRC_ADDR. This gives the resulting 8 upper physical address bits. All lower address bits are forwarded unchanged.

Request to address 0x99AE_37F0:

- Upper address bits: 0x99
- Hit mask: 28–25 = 0xE0
- Masked upper address bits: 0x80 – hits section 0
- Address mask: 25–1 = 0x1F
- Masked upper address bits: 0x19
- Full masked address: 0x19AE_37F0
- Bit 8 is 1 – targets the second memory controller
- Full masked shifted address (suppressing bit 8): 0x0CD7_1BF0 (see Section 15.2.4.2.2.1)
- OR upper physical address bits with SDRC_ADDR: 0x0CD7_1BF0
- Physical address: 0x0CD7_1BF0

This request is forwarded to address 0x0CD7_1BF0, address space 0, of the second memory controller.

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15.2.4.2.2.1 Address Upper Bits Shifting

Table 15-23 describes shifting the address upper bits.

Table 15-23. Address Upper Bits Shifting

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Address Before Interleaving																															
0	0	0	1	1	0	0	1	1	0	1	0	1	1	1	0	0	0	1	1	0	1	1	1	1	1	1	1	0	0	0	0
Address After Interleaving																															
0	0	0	0	1	1	0	0	1	1	0	1	0	1	1	1	0	0	0	1	1	0	1	1	1	1	1	1	0	0	0	0

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15.2.5 DMM Basic Programming Model

The programming model section:

- Describes how objects can be addressed in all TILER modes and orientations
- Explains how the physical containers and PAT LUT can be shared between different modes
- Does not give an exhaustive description of the TILER and DMM registers, because these are described in Section 15.2.3.5, *DMM*, and Section 15.2.3.6, *TILER*.

15.2.5.1 Global Initialization

This section identifies the requirements for initializing the surrounding modules when the DMM is to be used for the first time after a device reset. This initialization of surrounding modules is based on the integration and environment of the DMM (see Table 15-24).

Table 15-24. Global Initialization of Surrounding Modules

Surrounding Modules	Comments
PRCM	The module interface and functional clocks must be enabled. See Chapter 3, *Power, Reset, and Clock Management.*
Dual Cortex - M3 microprocessor unit (MPU)	Cortex-M3 interrupt controller (INTC) configuration must be done to enable the interrupts from the DMM. See Chapter 17, *Interrupt Controllers.*
Dual Cortex - A9 MPU	Cortex-A9 INTC configuration must be done to enable interrupts from the DMM. See Chapter 17, *Interrupt Controllers.*
L3 interconnect	Data interface

15.2.5.2 DMM Module Global Initialization

This procedure in Table 15-25 initializes the DMM after a power-on reset (POR).

Table 15-25. DMM Global Initialization

Step	Register/Bit Field/Programming Model	Value
Configure the DMM for smart-idle power management mode.	DMM_SYSCONFIG[3:2] IDLE_MODE	0x2

15.2.5.3 DMM Operational Modes Configuration

15.2.5.3.1 Different Operational Modes

The TILER can be virtually accessed in four different modes: 8-, 16-, 32-bit, and page modes. Each mode defines the element granularity to apply isometric transforms (see Table 15-26).

Table 15-26. Coding and Description of TILER Modes

Mode	Name	Granularity (Element Size)
0	8-bit tiled mode	8 bits
1	16-bit tiled mode	16 bits
2	32-bit tiled mode	32 bits
3	Page mode	4096 bytes

15.2.5.3.2 Configuration Settings and LUT Refill

The procedure inTable 15-27 provides the configuration settings and LUT refill.

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Table 15-27. Configuration Settings and LUT Refill

Step	Register/Bit Field/Programming Model	Value
PAT configuration refill Engine 0	DMM_PAT_CONFIG[0] MODE0	xxx
PAT configuration refill Engine 1	DMM_PAT_CONFIG[1] MODE1	xxx
Set DMM PAT view register value for each initiator.	DMM_PAT_VIEW0 Vx DMM_PAT_VIEW1 Vx	xxx
Set DMM PAT write enable for the initiators.	DMM_PAT_VIEW0 Wx DMM_PAT_VIEW1 Wx	xxx
Choosing container type and access method	DMM_PAT_VIEW_MAP_i	xxx
Define the base address of all view mappings.	DMM_PAT_VIEW_MAP_BASE[31] BASE_ADDR	xxx
Set area definition for DMM physical address translator.	DMM_PAT_AREA_i	xxx
Set physical address of the current table refill entry data or entry data when in manual mode.	DMM_PAT_DATA_i[31:4] ADDR	xxx
Define the direction of this PAT table refill (S Y X), different from 0x011.	DMM_PAT_CTRL_i[6:4] DIRECTION	xxx
Start a PAT table refill.	DMM_PAT_CTRL_i[0] START	0x1

15.2.5.3.3 Interleaving Settings

The procedure inTable 15-28 provides the interleaving settings.

Table 15-28. Interleaving Settings

Step	Register/Bit Field/Programming Model	Value
Set DMM system section address MSB.	DMM_LISA_MAP_i[31:24] SYS_ADDR	xxx
Set DMM system section size.	DMM_LISA_MAP_i[22:20] SYS_SIZE	xxx
Set SDRC interleaving mode.	DMM_LISA_MAP_i[19:18] SDRC_INTL	xxx
Set SDRC address space.	DMM_LISA_MAP_i[17:16] SDRC_ADDRSPC	xxx
Set SDRC mapping.	DMM_LISA_MAP_i[9:8] SDRC_MAP	xxx
Set SDRC address MSB.	DMM_LISA_MAP_i[7:0] SDRC_ADDR	xxx
Enable/disable DMM memory mapping lock.	DMM_LISA_LOCK[0] LOCK	xxx

15.2.5.3.4 Aliased Tiled View Orientation Settings and LUT Refill

The procedure in Table 15-29 provides the settings for aliased tiled view and LUT refill.

Table 15-29. Aliased Tiled View Orientation Settings and LUT Refill

Step	Register/Bit Field/Programming Model	Value
Set DMM TILER orientation for each initiator.	DMM_TILER_OR0 ORx DMM_TILER_OR1 ORx	xxx
Set DMM TILER write enable for the initiators.	DMM_TILER_OR0 Wx DMM_TILER_OR1 Wx	xxx
Define the base address of all view mappings.	DMM_PAT_VIEW_MAP_BASE[31] BASE_ADDR	xxx
DMM PAT initiator for synchronization	DMM_PAT_CTRL_i[31:28] INITIATOR	xxx
Set DMM PAT table reload synchronization.	DMM_PAT_CTRL_i[16] SYNC	xxx
Set DMM PAT LUT index.	DMM_PAT_CTRL_i[9:8] LUT_ID	xxx
Define the direction of this PAT table refill (S Y X).	DMM_PAT_CTRL_i[6:4] DIRECTION	xxx
Start a PAT table refill.	DMM_PAT_CTRL_i[0] START	0x1

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15.2.5.3.5 Priority Settings

The procedure in Table 15-30 provides the sequence to set priorities.

Table 15-30. Priority Settings

Step	Register/Bit Field/Programming Model	Value
Set priority for each initiator.	DMM_PEG_PRIO_k Px	xxx
Set write enable for P_PAT field.	DMM_PEG_PRIO_PAT[4] W_PAT	xxx
Set priority for PAT engine.	DMM_PEG_PRIO_PAT[2:0] P_PAT	xxx

15.2.5.3.6 Error Handling

The procedure in Table 15-31 provides the sequence for error handling.

Table 15-31. Error Handling

Step	Register/Bit Field/Programming Model	Value
Enable interrupt for selected type of error.	DMM_PAT_IRQENABLE_SET[15:9] DMM_PAT_IRQENABLE_SET[7:0]	xxx
When interrupt occurs		
Disable type of error to handle.	DMM_PAT_IRQENABLE_CLR[15:9] DMM_PAT_IRQENABLE_CLR[7:0]	xxx
Check error status.	DMM_PAT_IRQSTATUS[15:9] DMM_PAT_IRQSTATUS[7:0]	xxx

15.2.5.3.7 PAT Programming Model

The PAT maps the tiled data anywhere in the 4-GB physical address range, with a PAGE granularity. (The TILER page is the granularity of physical memory allocation in the TILER container. Each page is 4kiB).

A PAT view defines the kind of PAT to perform for each page, 8-, 16-, and 32-bit mode access. Each mode in each PAT view can be programmed in two different modes: direct translation and indirect translation.

15.2.5.3.7.1 PAT in Direct Translation Mode

In this mode, the PAT performs a translation of the 128-MB virtual container as a whole in the physical address space (that is, in the SDRAM). This mode is used only for debug or in case of a DMM without a PAT.

15.2.5.3.7.2 PAT in Indirect Translation Mode

This is the most commonly used mode. In this mode, the PAT performs a translation of each 4-KB page individually. In this way the 128-MB virtual address space can be scattered in the whole 2GB of the physical address space. This is achieved by using a 32,678-word LUT that converts each page index (32,768 possible values) into 19 address bits that represent this page address in the physical memory. The main characteristic of this mode is there is no constraint on the use of the physical memory except that it is uses a multiple of 4-KB areas located at 4-KB boundaries in the physical memory. In this mode, the translation vector is in the internal 32-k entry PAT vector table at the index given by bits [26:12] of the input virtual address, and CONT_x = 0.

Programming sequence:

1. Set the DMM_PAT_VIEW0 register (or DMM_PAT_VIEW1, depending on the L3 CONN_ID of the initiator that is to perform the tiled accesses) with the appropriate value. For example, if the L3 CONN_ID equals 0, then the DMM_PAT_VIEW0 register must be programmed with the value 0x0000_0001 (PAT view 1 selected for initiator 0).
2. Set DMM_PAT_VIEW_MAP_BASE[31] = 0x8000_0000 (must always be programmed at 1 to select the upper 2GB of the physical address space that corresponds to the external memory).

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3. Set all 16-bit tiled accesses in indirect translation mode by setting at least the field ACCESS_16 to 1 (DMM_PAT_VIEW_MAP_1 = 0x0000_8000), program DMM_PAT_VIEW_MAP_1 at 0x8080_8080.

15.2.5.4 Addressing an Object in Tiled Mode

This section describes how a frame-buffer with a top-left pixel at (x0,y0) in the natural view container and a bottom right pixel at (x1,y1) in the natural view container is addressed in any tiled mode and orientation.

15.2.5.4.1 Frame-Buffer Addressing

NOTE: In this section, the (x,y) coordinates are given in pixel units.

Given an (S, $\overline{Y}$, $\overline{X}$) orientation, the (x,y) coordinates of the first pixel of the frame in the oriented view (where W = the width and H = the height in pixels of the container in the considered frame mode) is:

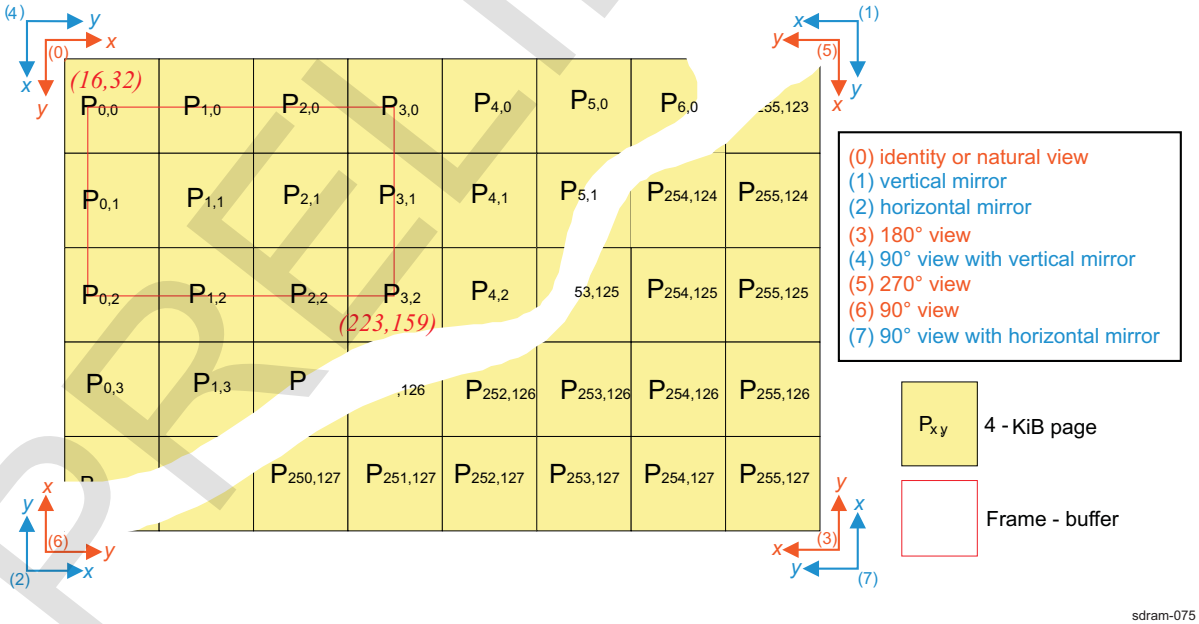
(x,y) = (x_{or}, y_{or}) when S, (y_{or}, x_{or}) otherwise
with:
x_{or} = x_0 when $\overline{X}$, W-1-x_1 otherwise
y_{or} = y_0 when $\overline{Y}$, H-1-y_1 otherwise

Given a (M_1, M_0) TILER mode where M_1 # 0 or M_0 # 0, the size in bytes of a pixel is 2^{2M1+M0}.

Therefore, given an (S, $\overline{Y}$, $\overline{X}$) orientation and a n(M_1, M_0) TILER mode where M_1 # 0 or M_0 # 0, the byte offset of the base address of the considered oriented frame in its container is:
base_address((x_0, y_0), (x_1, y_1), (S, $\overline{Y}$, $\overline{X}$), (M_1, M_0)) = (y_{or}W + x_{or}) P_5 when S, (x_{or}H + y_{or}) P_5 otherwise
with:
x_{or} = x_0 when $\overline{X}$, W-1-x_1 otherwise
y_{or} = y_0 when $\overline{Y}$, H-1-y_1 otherwise
P_5 = 2^{2M1+M0}

In its natural orientation, the TILER container consists of 8192 lines of 16,384 pixels of 8 bits, or 4096 lines of 16,384 pixels of 16 bits, or 4096 lines of 8192 pixels of 32 bits.

Figure 15-42. Example of 8-Bit Frame-Buffer Addressing in any Orientation



This frame-buffer address generation is independent from the page size. For instance, the 8-bit frame-buffer shown in Figure 15-42 that ranges from the top-left pixel at (16, 32) to the bottom-right pixel at (223, 159) in the natural orientation view, corresponds to the 29-bit view address offsets and full 33-bit TILER addresses given in Table 15-32.

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Table 15-32. 29-Bit View Address Offset and 33-Bit Full TILER Address for an 8-Bit Frame-Buffer

S	$\overline{Y}$	$\overline{X}$	x_{or}	y_{or}	29-Bit Address Offset in View	Full 33-Bit TILER Address
0	0	0	16	32	00080010h	100080010h
0	0	1	16,160	32	00083F20h	120083F20h
0	1	0	16	8032	07D80010h	147D80010h
0	1	1	16,160	8032	07D83F20h	167D83F20h
1	0	0	16	32	00020020h	180020020h
1	0	1	16,160	32	07E40020h	1A7E40020h
1	1	0	16	8032	00021F60h	1C0021F60h
1	1	1	16,160	8032	07E41F60h	1E7E41F60h

In this example the TILER is addressed in 8-bit mode, which translates to addresses with all mode bits (bits 27 and 28) cleared in the 29-bit address offset in view and in the full 33-bit TILER address.

15.2.5.4.2 TILER Page Mapping

Let:

- c (c = 0, 1, or 2) be the TILER page configuration (0 for 4-kiB pages, 1 for 16-kiB pages, and 2 for 64-kiB pages)
- (x_0, y_0) be the top-left pixel and (x_1, y_1) be the bottom-right pixel of a frame in its natural orientation
- W be the width and H the height in pixels of the container in the considered frame mode

The top-left page coordinates (P_{x0}, P_{y0}) and bottom-right page coordinates (P_{x1}, P_{y1}) that correspond to the frame are given by: $P_{x0} = (64.x_0.2^{2-c}) / W$, $P_{y0} = (32.y_0.2^{2-c}) / H$, $P_{x1} = (64.x_1.2^{2-c}) / W$ and $P_{y1} = (32.y_1.2^{2-c}) / H$.

In its natural orientation, the TILER container consists of 8192 lines of 16,384 pixels of 8 bits, or 4096 lines of 16,384 pixels of 16 bits, or 4096 lines of 8192 pixels of 32 bits.

NOTE: The page area type has the same structure as the DMM_PAT_AREA_i registers. For instance, the 8-bit frame-buffer described in Figure 15-42 and ranging from the top-left pixel at (16, 32) to the bottom-right pixel at (223, 159) in the natural orientation view, is mapped from the top-left page at P0,0 to the bottom-right page P3,2.

15.2.5.5 Addressing an Object in Page Mode

In page mode, the orientation modifies only the sequence of accessed pages, not their content. In this respect the orientation must be seen as a way to optimize the one-dimensional (1D) object allocation in a TILER container by allowing a 1D object spanning multiple pages to map a set of adjacent pages in any direction. For instance, a 1.25-MiB object, mapped on 320 pages of 4kiB can be allocated in a TILER container in any of the eight orientations (see Section 15.2.3.6.1.7.3, *Element Ordering in the TILER Container*).

The initial page can be chosen freely among all pages. In this respect, the address offset of a page in a TILER container is expressed as:

Let:

- c (c = 0, 1 or 2) be the TILER page configuration (0 for 4-kiB pages, 1 for 16-kiB pages, and 2 for 64-kiB pages)
- $(S, \overline{Y}, \overline{X})$ be the orientation of the considered 1D object in page mode
- (P_x, P_y) be the coordinate of the initial page in the natural orientation view

The byte offset of the base address of the considered initial page in its oriented container is:
$base_address((P_x, P_y), (S, \overline{Y}, \overline{X})) = 4096.(64.y_{or}.2^{2-c} + x_{or}).2^{2.c}$ when S, $4096.(32.x_{or}.2^{2-c} + y_{or}).2^{2.c}$ otherwise with:
$x_{or} = P_x$ when $\overline{X}$, $64.2^{2-c}\text{-}1\text{-}P_x$ otherwise
$y_{or} = P_y$ when $\overline{Y}$, $32.2^{2-c}\text{-}1\text{-}P_y$ otherwise

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For instance, a 1D object starting from the page P32,63 in the natural orientation view on a DMM using 4-kiB pages, corresponds to the 29-bit view address offsets and full 33-bit TILER addresses given in Table 15-33.

Table 15-33. 29-Bit View Address Offset and 33-Bit Full TILER Address for a 1D Object

S	$\overline{Y}$	$\overline{X}$	x_{or}	y_{or}	29-Bit Address Offset in View	Full 33-Bit TILER Address
0	0	0	32	63	1BF20000h	11BF20000h
0	0	1	223	63	1BFDF000h	13BFDF000h
0	1	0	32	64	1C020000h	15C020000h
0	1	1	223	64	1C0DF000h	17C0DF000h
1	0	0	32	63	1903F000h	19903F000h
1	0	1	223	63	1EFBF000h	1BEFBF000h
1	1	0	32	64	19040000h	1D9040000h
1	1	1	223	64	1EFC0000h	1FEFC0000h

In this example the TILER is addressed in page mode, which translates to addresses with mode bits (bits 27 and 28) set in the 29-bit address offset in view and full 33-bit TILER address.

15.2.5.6 Sharing Containers Between Different Modes

When allocating objects in TILER containers, take care to ensure that no two objects physically overlap.

In this respect, and to ease the object allocation and deallocation, it is strongly advised to share a TILER page only for different objects that do both of the following:

- Belong to the same mode
- Have the same lifetime (that is, are allocated and deallocated simultaneously)

Two objects of different modes can physically overlap if:

- One physical page is mapped twice in two different locations of the DMM LUT.
- The two objects share the DMM LUT and the intersection of their two page set is not empty.

  These two issues can be easily avoided by allocating a physical page only once in the DMM LUT.

  The second issue is a bit more difficult, especially if the allocation of objects in the various TILER containers must be dynamic. Managing the fragmentation within a flat memory model in a space-constrained system is not straightforward, and is the main reason for the existence of MMUs in most current processors, which adds yet another constraint to the problem (the y dimension, which makes it even more difficult).

Returning to the CPU-analogy, the memory fragmentation issue has been mostly solved by using a virtual memory space larger than the actual physical memory space and a virtual-to-physical translation system. This allows contiguous virtual memory allocation when sufficient physical memory is available and the larger contiguous physical buffer is smaller than the requested memory allocation.

Similarly, the DMM answer to this object allocation in the TILER containers is two-fold:

- The DMM must have sufficient virtual address space in all modes to permit a static allocation of a pool of virtual buffers in all TILER modes for all TILER-aware initiators.
- Each TILER-aware initiator must dynamically manage its own pool of virtual buffers.

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15.2.6 DMM Register Manual

This section provides information about the DMM registers.Table 15-34 describes the DMM instance.

15.2.6.1 DMM Instance Summary

Table 15-34. DMM Instance Summary

Module Name	Base Address	Size
DMM	0x4E00 0000	32MB

15.2.6.2 DMM Registers

15.2.6.2.1 DMM Register Summary

Table 15-35 provides a summary of the DMM registers.

Table 15-35. DMM Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	DMM L3 Physical Address
DMM_REVISION	R	32	0x0000 0000	0x4E00 0000
DMM_HWINFO	R	32	0x0000 0004	0x4E00 0004
DMM_LISA_HWINFO	R	32	0x0000 0008	0x4E00 0008
DMM_SYSCONFIG	RW	32	0x0000 0010	0x4E00 0010
DMM_LISA_LOCK	RW	32	0x0000 001C	0x4E00 001C
DMM_LISA_MAP_i (1)	RW	32	0x0000 0040 + (0x4 * i)	0x4E00 0040 + (0x4 * i)
DMM_TILER_HWINFO	R	32	0x0000 0208	0x4E00 0208
DMM_TILER_OR0	RW	32	0x0000 0220	0x4E00 0220
DMM_TILER_OR1	RW	32	0x0000 0224	0x4E00 0224
DMM_PAT_HWINFO	R	32	0x0000 0408	0x4E00 0408
DMM_PAT_GEOMETRY	R	32	0x0000 040C	0x4E00 040C
DMM_PAT_CONFIG	RW	32	0x0000 0410	0x4E00 0410
DMM_PAT_VIEW0	RW	32	0x0000 0420	0x4E00 0420
DMM_PAT_VIEW1	RW	32	0x0000 0424	0x4E00 0424
DMM_PAT_VIEW_MAP_i (1)	RW	32	0x0000 0440 + (0x4 * i)	0x4E00 0440 + (0x4 * i)
DMM_PAT_VIEW_MAP_BASE	RW	32	0x0000 0460	0x4E00 0460
DMM_PAT_IRQSTATUS_RAW	RW	32	0x0000 0480	0x4E00 0480
DMM_PAT_IRQSTATUS	RW	32	0x0000 0490	0x4E00 0490
DMM_PAT_IRQENABLE_SET	RW	32	0x0000 04A0	0x4E00 04A0
DMM_PAT_IRQENABLE_CLR	RW	32	0x0000 04B0	0x4E00 04B0
DMM_PAT_STATUS_i (1)	R	32	0x0000 04C0 + (0x4 * i)	0x4E00 04C0 + (0x4 * i)
DMM_PAT_DESCR_i (1)	RW	32	0x0000 0500 + (0x10 * i)	0x4E00 0500 + (0x10 * i)
DMM_PAT_AREA_i (1)	RW	32	0x0000 0504 + (0x10 * i)	0x4E00 0504 + (0x10 * i)
DMM_PAT_CTRL_i (1)	RW	32	0x0000 0508 + (0x10 * i)	0x4E00 0508 + (0x10 * i)
DMM_PAT_DATA_i (1)	RW	32	0x0000 050C + (0x10 * i)	0x4E00 050C + (0x10 * i)
DMM_PEG_HWINFO	R	32	0x0000 0608	0x4E00 0608
DMM_PEG_PRIO_k (2)	RW	32	0x0000 0620 + (0x4 * k)	0x4E00 0620 + (0x4 * k)

(1) i = 0 to 3 for DMM
(2) k = 0 to 7

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Table 15-35. DMM Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	DMM L3 Physical Address
DMM_PEG_PRIO_PAT	RW	32	0x0000 0640	0x4E00 0640

15.2.6.2.2 DMM Register Description

Table 15-36 through Table 15-90 describe the DMM registers.

Table 15-36. DMM_REVISION

Address Offset	0x0000 0000		
Physical Address	0x4E00 0000	**Instance**	DMM
Description	DMM Revision Number		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	Revision Number	R	0x---- ---- (1)

(1) TI internal data

Table 15-37. Register Call Summary for Register DMM_REVISION

Dynamic Memory Manager
- DMM Register Summary: [0]

Table 15-38. DMM_HWINFO

Address Offset	0x0000 0004		
Physical Address	0x4E00 0004	**Instance**	DMM
Description	DMM hardware configuration		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												ROBIN_CNT				RESERVED				ELLA_CNT				RESERVED				TILER_CNT			

Bits	Field Name	Description	Type	Reset
31:20	RESERVED	Reserved	R	0x000
19:16	ROBIN_CNT	Number of ROBIN in the DMM	R	0x2
15:12	RESERVED	Reserved	R	0x0
11:8	ELLA_CNT	Number of ELLA in the DMM	R	0x0
7:4	RESERVED	Reserved	R	0x0
3:0	TILER_CNT	Number of TILER in the DMM	R	0x2

Table 15-39. Register Call Summary for Register DMM_HWINFO

Dynamic Memory Manager
- DMM Configuration: [0] [1]
- DMM Register Summary: [2]

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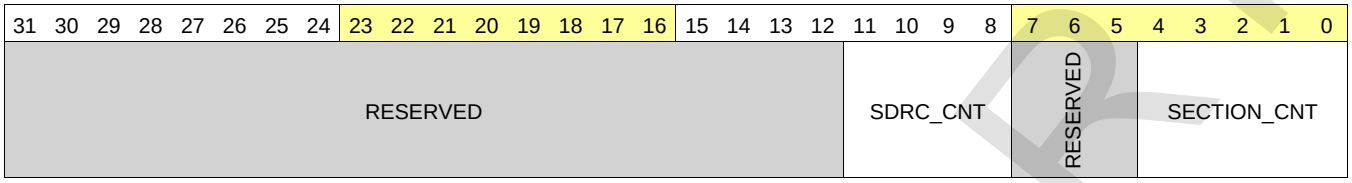
Table 15-40. DMM_LISA_HWINFO

Address Offset	0x0000 0008		
Physical Address	0x4E00 0008	**Instance**	DMM
Description	DMM hardware configuration for LISA		
Type	R		



Bits	Field Name	Description	Type	Reset
31:12	RESERVED	Reserved	R	0x00000
11:8	SDRC_CNT	Number of attached SDRAM controllers	R	0x2
7:5	RESERVED	Reserved	R	0x0
4:0	SECTION_CNT	Number of DMM sections	R	0x02

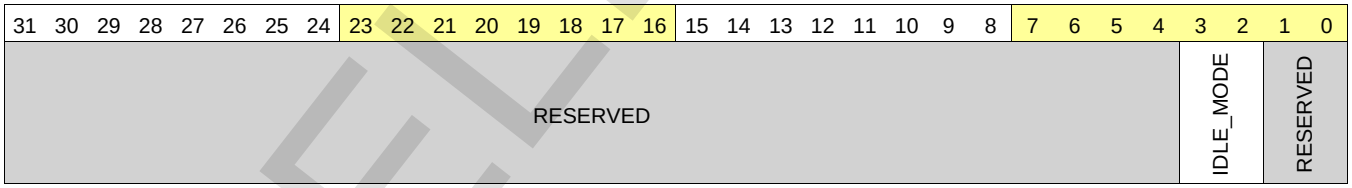
Table 15-41. Register Call Summary for Register DMM_LISA_HWINFO

Dynamic Memory Manager

- DMM Configuration: [0] [1]
- DMM Register Summary: [2]

Table 15-42. DMM_SYSCONFIG

Address Offset	0x0000 0010		
Physical Address	0x4E00 0010	**Instance**	DMM
Description	DMM clock management configuration		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved	R	0x0000000
3:2	IDLE_MODE	Configuration of the local target state management mode. 0x0: Force-idle mode: local target's idle state follows (acknowledges) the system's idle requests unconditionally, that is, regardless of the IP module's internal requirements. Backup mode, for debug only. 0x1: No-idle mode: local target never enters idle state. Backup mode, for debug only 0x3: Reserved 0x2: Smart-idle mode: local target's idle state eventually follows (acknowledges) the system's idle requests, depending on the IP module's internal requirements. IP module shall not generate (IRQ- or DMA-request-related) wake-up events.	RW	0x2

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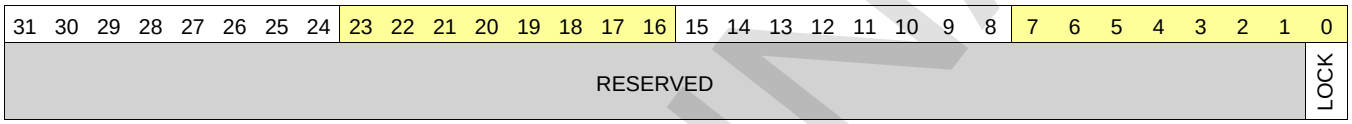
Bits	Field Name	Description	Type	Reset
1:0	RESERVED	Reserved	RW W0Only	0x0

Table 15-43. Register Call Summary for Register DMM_SYSCONFIG

Dynamic Memory Manager
- DMM Integration: [0]
- DMM Power Management: [1]
- DMM Module Global Initialization: [2]
- DMM Register Summary: [3]

Table 15-44. DMM_LISA_LOCK

Address Offset	0x0000 001C		
Physical Address	0x4E00 001C	**Instance**	DMM
Description	DMM memory mapping lock		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Should be written as 0	R	0x0000 0000
0	LOCK	DMM lock map Write 0x0: No effect (clear on reset only) Read 0x0: DMM_LISA_MAP_i unlocked Read 0x1: DMM_LISA_MAP_i locked Write 0x1: Locking DMM_LISA_MAP_i registers	RW	0

Table 15-45. Register Call Summary for Register DMM_LISA_LOCK

Dynamic Memory Manager
- DMM Integration: [0]
- DMM Concepts: [1]
- DMM Internal Macro-Architecture: [2]
- Interleaving Settings: [3]
- DMM Register Summary: [4]

Table 15-46. DMM_LISA_MAP_i

Address Offset	0x0000 0040 + (0x4 * i)	**Index**	i = 0 to 3
Physical Address	0x4E00 0040 + (0x4 * i)	**Instance**	DMM
Description	DMM memory mapping n = 0 for the first memory mapping register, n = 1 for the second memory mapping register.		
Type	RW		

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31 30 29 28 27 26 25 24	23 22 21 20	19 18	17 16	15 14 13 12 11 10	9 8	7 6 5 4 3 2 1 0
SYS_ADDR	RESERVED	SYS_SIZE	SDRC_INTL	SDRC_ADDRSPC	RESERVED	SDRC_MAP	SDRC_ADDR

Bits	Field Name	Description	Type	Reset
31:24	SYS_ADDR	DMM system section address MSB for view mapping n	RW	0x00
23	RESERVED	Reserved	RW W0Only	0
22:20	SYS_SIZE	DMM system section size for view mapping n 0x0: 16-MiB section 0x1: 32-MiB section 0x2: 64-MiB section 0x3: 128-MiB section 0x4: 256-MiB section 0x5: 512-MiB section 0x6: 1-GiB section 0x7: 2-GiB section	RW	0x0
19:18	SDRC_INTL	SDRAM controller interleaving mode 0x0: No interleaving 0x1: 128-byte interleaving 0x2: 256-byte interleaving 0x3: 512-byte interleaving The 128-/256-/512-byte interleaving applies only to nontiled regions. If accesses are made to tiled regions, interleaving is forced to 1kiB. SDRC_INTL is don't care if SDRC_MAP is not 0x3 (no interleaving).	RW	0x0
17:16	SDRC_ADDRSPC	SDRAM controller address space for view mapping n	RW	0x0
15:10	RESERVED	Reserved	RW W0Only	0x00
9:8	SDRC_MAP	SDRAM controller mapping for view mapping n 0x0: Unmapped 0x1: Mapped on SDRC 0 only (not interleaved) 0x2: Mapped on SDRC 1 only (not interleaved) 0x3: Mapped on SDRC 0 and SDRC 1 (interleaved) To enable interleaving, SDRC_MAP must be 0x3 and SDRC_INTL must be a nonzero value.	RW	0
7:0	SDRC_ADDR	SDRAM controller address MSB for view mapping n	RW	0x00

Table 15-47. Register Call Summary for Register DMM_LISA_MAP_i

Dynamic Memory Manager

- DMM Integration: [0]
- DMM Concepts: [1] [2]
- DMM Internal Macro-Architecture: [3] [4]
- Interleaving Settings: [5] [6] [7] [8] [9] [10]
- DMM Register Summary: [11]
- DMM Register Description: [12] [13] [14]

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Table 15-48. DMM_TILER_HWINFO

Address Offset	0x0000 0208		
Physical Address	0x4E00 0208	**Instance**	DMM
Description	DMM hardware configuration for TILER		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														OR_CNT	

Bits	Field Name	Description	Type	Reset
31:5	RESERVED	Reserved	R	0x0000000
4:0	OR_CNT	Number of TILER orientation entries Read 0x1: One orientation entry Read 0x2: Two orientation entries Read 0x4: Four orientation entries Read 0x8: Eight orientation entries Read 0x10: Sixteen orientation entries	R	0x10

Table 15-49. Register Call Summary for Register DMM_TILER_HWINFO

Dynamic Memory Manager

- DMM Configuration: [0]
- DMM Register Summary: [1]

Table 15-50. DMM_TILER_OR0

Address Offset	0x0000 02200	**Index**	0
Physical Address	0x4E00 0220	**Instance**	DMM
Description	DMM TILER orientation (initiators 0 to 7)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
W7	OR7			W6	OR6			W5	OR5			W4	OR4			W3	OR3			W2	OR2			W1	OR1			W0	OR0		

Bits	Field Name	Description	Type	Reset
31	W7	Write-enable for OR7 bit field Write 0x0: OR7 field is unchanged Write 0x1: OR7 field is updated	RW	0
30:28	OR7	Orientation for initiator 7	RW	0x0
27	W6	Write-enable for OR6 bit field Write 0x0: OR6 field is unchanged Write 0x1: OR6 field is updated	RW	0
26:24	OR6	Orientation for initiator 6	RW	0x0
23	W5	Write-enable for OR5 bit field Write 0x0: OR5 field is unchanged Write 0x1: OR5 field is updated	RW	0
22:20	OR5	Orientation for initiator 5	RW	0x0
19	W4	Write-enable for OR4 bit field Write 0x0: OR4 field is unchanged Write 0x1: OR4 field is updated	RW	0

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Bits	Field Name	Description	Type	Reset
18:16	OR4	Orientation for initiator 4	RW	0x0
15	W3	Write-enable for OR3 bit field Write 0x0: OR3 field is unchanged Write 0x1: OR3 field is updated	RW	0
14:12	OR3	Orientation for initiator 3	RW	0x0
11	W2	Write-enable for OR2 bit field Write 0x0: OR2 field is unchanged Write 0x1: OR2 field is updated	RW	0
10:8	OR2	Orientation for initiator 2	RW	0x0
7	W1	Write-enable for OR1 bit field Write 0x0: OR1 field is unchanged Write 0x1: OR1 field is updated	RW	0
6:4	OR1	Orientation for initiator 1	RW	0x0
3	W0	Write-enable for OR0 bit field Write 0x0: OR0 field is unchanged Write 0x1: OR0 field is updated	RW	0
2:0	OR0	Orientation for initiator 0	RW	0x0

Table 15-51. Register Call Summary for Register DMM_TILER_OR0

Dynamic Memory Manager

- DMM Integration: [0]
- TILER Macro-Architecture: [1] [2]
- Aliased Tiled View Orientation Settings and LUT Refill: [3] [4]
- DMM Register Summary: [5]

Table 15-52. DMM_TILER_OR1

Address Offset	0x0000 02204	**Index**	0
Physical Address	0x4E00 0224	**Instance**	DMM
Description	DMM TILER orientation (initiators 8 to 15)		
Type	RW		

31	30 29 28	27	26 25 24	23	22 21 20	19	18 17 16	15	14 13 12	11	10 9 8	7	6 5 4	3	2 1 0
W15	OR15	W14	OR14	W13	OR13	W12	OR12	W11	OR11	W10	OR10	W9	OR9	W8	OR8

Bits	Field Name	Description	Type	Reset
31	W15	Write-enable for OR15 bit field Write 0x0: OR15 field is unchanged Write 0x1: OR15 field is updated	RW	0
30:28	OR15	Orientation for initiator 15	RW	0x0
27	W14	Write-enable for OR14 bit field Write 0x0: OR14 field is unchanged Write 0x1: OR14 field is updated	RW	0
26:24	OR14	Orientation for initiator 14	RW	0x0
23	W13	Write-enable for OR13 bit field Write 0x0: OR13 field is unchanged Write 0x1: OR13 field is updated	RW	0
22:20	OR13	Orientation for initiator 13	RW	0x0

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Bits	Field Name	Description	Type	Reset
19	W12	Write-enable for OR12 bit field Write 0x0: OR12 field is unchanged Write 0x1: OR12 field is updated	RW	0
18:16	OR12	Orientation for initiator 12	RW	0x0
15	W11	Write-enable for OR11 bit field Write 0x0: OR11 field is unchanged Write 0x1: OR11 field is updated	RW	0
14:12	OR11	Orientation for initiator 11	RW	0x0
11	W10	Write-enable for OR10 bit field Write 0x0: OR10 field is unchanged Write 0x1: OR10 field is updated	RW	0
10:8	OR10	Orientation for initiator 10	RW	0x0
7	W9	Write-enable for OR9 bit field Write 0x0: OR9 field is unchanged Write 0x1: OR9 field is updated	RW	0
6:4	OR9	Orientation for initiator 9	RW	0x0
3	W8	Write-enable for OR8 bit field Write 0x0: OR8 field is unchanged Write 0x1: OR8 field is updated	RW	0
2:0	OR8	Orientation for initiator 8	RW	0x0

Table 15-53. Register Call Summary for Register DMM_TILER_OR1

Dynamic Memory Manager

- DMM Integration: [0]
- TILER Macro-Architecture: [1] [2]
- Aliased Tiled View Orientation Settings and LUT Refill: [3] [4]
- DMM Register Summary: [5]

Table 15-54. DMM_PAT_HWINFO

Address Offset	0x0000 0408		
Physical Address	0x4E00 0408	**Instance**	DMM
Description	DMM hardware configuration for PAT		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			ENGINE_CNT					RESERVED			LUT_CNT					RESERVED				VIEW_MAP_CNT				RESERVED	VIEW_CNT						

Bits	Field Name	Description	Type	Reset
31:29	RESERVED	Reserved	R	0x0
28:24	ENGINE_CNT	Number of PAT refill engines	R	0x04
23:21	RESERVED	Reserved	R	0x0
20:16	LUT_CNT	Number of PAT LUT for page-grained physical address translation	R	0x01
15:12	RESERVED	Reserved	R	0x0

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Bits	Field Name	Description	Type	Reset
11:8	VIEW_MAP_CNT	Number of internal PAT view mappings. Read 0x1: One view map Read 0x2: Two view maps Read 0x4: Four view maps Read 0x8: Eight view maps	R	0x4
7	RESERVED	Reserved	R	0
6:0	VIEW_CNT	Number of PAT view entries Read 0x1: One view entry Read 0x2: Two view entries Read 0x4: Four view entries Read 0x8: Eight view entries Read 0x10: Sixteen view entries Read 0x20: Thirty-two view entries Read 0x40: Sixty-four view entries	R	0x10

Table 15-55. Register Call Summary for Register DMM_PAT_HWINFO

Dynamic Memory Manager
- DMM Configuration: [0] [1] [2] [3]
- DMM Register Summary: [4]

Table 15-56. DMM_PAT_GEOMETRY

Address Offset	0x0000 040C		
Physical Address	0x4E00 040C	**Instance**	DMM
Description	PAT geometry-related settings		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					CONT_HGHT			RESERVED				CONT_WDTH				RESERVED		ADDR_RANGE						RESERVED				PAGE_SZ			

Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Reserved	R	0x00
26:24	CONT_HGHT	Container height in pages Read 0x1: Container height of 32 pages Read 0x2: Container height of 64 pages Read 0x4: Container height of 128 pages	R	0x4
23:20	RESERVED	Reserved	R	0x0
19:16	CONT_WDTH	Container width in pages Read 0x2: Container width of 64 pages Read 0x4: Container width of 128 pages Read 0x8: Container width of 256 pages	R	0x8
15:14	RESERVED	Reserved	R	0x0

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Bits	Field Name	Description	Type	Reset
13:8	ADDR_RANGE	PAT output physical address range Read 0x1: 128-MiB range Read 0x2: 256-MiB range Read 0x4: 512-MiB range Read 0x8: 1-GiB range Read 0x10: 2-GiB range Read 0x20: 4-GiB range	R	0x10
7:5	RESERVED	Reserved	R	0x0
4:0	PAGE_SZ	Page size in 4-kiB granularity Read 0x1: 4-kiB page Read 0x4: 16-kiB page Read 0x10: 64-kiB page	R	0x01

Table 15-57. Register Call Summary for Register DMM_PAT_GEOMETRY

Dynamic Memory Manager
- DMM Configuration: [0] [1] [2] [3]
- DMM Register Summary: [4]

Table 15-58. DMM_PAT_CONFIG

Address Offset	0x0000 0410		
Physical Address	0x4E00 0410	**Instance**	DMM
Description	This is the PAT configuration register aimed at defining the major PAT configuration of each refill engine.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												MODE3	MODE2	MODE1	MODE0

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved	R	0x0000000
3	MODE3	Mode of refill engine 3 0: Normal mode 1: Direct LUT access	RW	0
2	MODE2	Mode of refill engine 2 0: Normal mode 1: Direct LUT access	RW	0
1	MODE1	Mode of refill engine 1 0: Normal mode 1: Direct LUT access	RW	0
0	MODE0	Mode of refill engine 0 0: Normal mode 1: Direct LUT access	RW	0

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Table 15-59. Register Call Summary for Register DMM_PAT_CONFIG

Dynamic Memory Manager

- DMM Concepts: [0]
- Configuration Settings and LUT Refill: [1] [2]
- DMM Register Summary: [3]

Table 15-60. DMM_PAT_VIEW0

Address Offset	0x0000 0420	**Index**	
Physical Address	0x4E00 0420	**Instance**	DMM
Description	DMM PAT View register (initiators 0 to 7)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
W7	RESERVED	V7		W6	RESERVED	V6		W5	RESERVED	V5		W4	RESERVED	V4		W3	RESERVED	V3		W2	RESERVED	V2		W1	RESERVED	V1		W0	RESERVED	V0	

Bits	Field Name	Description	Type	Reset
31	W7	Write-enable for V7 bit field Write 0x0: V7 field is unchanged Write 0x1: V7 field is updated	RW	0
30	RESERVED	Reserved	RW W0Only	0
29:28	V7	PAT view for initiator 7	RW	0x0
27	W6	Write-enable for V6 bit field Write 0x0: V6 field is unchanged Write 0x1: V6 field is updated	RW	0
26	RESERVED	Reserved	RW W0Only	0
25:24	V6	PAT view for initiator 6	RW	0x0
23	W5	Write-enable for V5 bit field Write 0x0: V5 field is unchanged Write 0x1: V5 field is updated	RW	0
22	RESERVED	Reserved	RW W0Only	0
21:20	V5	PAT view for initiator 5	RW	0x0
19	W4	Write-enable for V4 bit field Write 0x0: V4 field is unchanged Write 0x1: V4 field is updated	RW	0
18	RESERVED	Reserved	RW W0Only	0
17:16	V4	PAT view for initiator 4	RW	0x0
15	W3	Write-enable for V3 bit field Write 0x0: V3 field is unchanged Write 0x1: V3 field is updated	RW	0
14	RESERVED	Reserved	RW W0Only	0
13:12	V3	PAT view for initiator 3	RW	0x0

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Bits	Field Name	Description	Type	Reset
11	W2	Write-enable for V2 bit field Write 0x0: V2 field is unchanged Write 0x1: V2 field is updated	RW	0
10	RESERVED	Reserved	RW W0Only	0
9:8	V2	PAT view for initiator 2	RW	0x0
7	W1	Write-enable for V1 bit field Write 0x0: V1 field is unchanged Write 0x1: V1 field is updated	RW	0
6	RESERVED	Reserved	RW W0Only	0
5:4	V1	PAT view for initiator 1	RW	0x0
3	W0	Write-enable for V0 bit field Write 0x0: V0 field is unchanged Write 0x1: V0 field is updated	RW	0
2	RESERVED	Reserved	RW W0Only	0
1:0	V0	PAT view for initiator 0	RW	0x0

Table 15-61. Register Call Summary for Register DMM_PAT_VIEW0

Dynamic Memory Manager
- DMM Integration: [0]
- DMM Concepts: [1] [2]
- Configuration Settings and LUT Refill: [3] [4]
- PAT Programming Model: [5] [6]
- DMM Register Summary: [7]

Table 15-62. DMM_PAT_VIEW1

Address Offset	0x0000 0424	**Index**	
Physical Address	0x4E00 0424	**Instance**	DMM
Description	DMM PAT view register (initiators 8 to 15)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
W15	RESERVED	V15		W14	RESERVED	V14		W13	RESERVED	V13		W12	RESERVED	V12		W11	RESERVED	V11		W10	RESERVED	V10		W9	RESERVED	V9		W8	RESERVED	V8	

Bits	Field Name	Description	Type	Reset
31	W15	Write-enable for V15 bit field Write 0x0: V15 field is unchanged Write 0x1: V15 field is updated	RW	0
30	RESERVED	Reserved	RW W0Only	0
29:28	V15	PAT view for initiator 15	RW	0x0
27	W14	Write-enable for V14 bit field Write 0x0: V14 field is unchanged Write 0x1: V14 field is updated	RW	0

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Bits	Field Name	Description	Type	Reset
26	RESERVED	Reserved	RW W0Only	0
25:24	V14	PAT view for initiator 14	RW	0x0
23	W13	Write-enable for V13 bit field Write 0x0: V13 field is unchanged Write 0x1: V13 field is updated	RW	0
22	RESERVED	Reserved	RW W0Only	0
21:20	V13	PAT view for initiator 13	RW	0x0
19	W12	Write-enable for V12 bit field Write 0x0: V12 field is unchanged Write 0x1: V12 field is updated	RW	0
18	RESERVED	Reserved	RW W0Only	0
17:16	V12	PAT view for initiator 12	RW	0x0
15	W11	Write-enable for V11 bit field Write 0x0: V11 field is unchanged Write 0x1: V11 field is updated	RW	0
14	RESERVED	Reserved	RW W0Only	0
13:12	V11	PAT view for initiator 11	RW	0x0
11	W10	Write-enable for V10 bit field Write 0x0: V10 field is unchanged Write 0x1: V10 field is updated	RW	0
10	RESERVED	Reserved	RW W0Only	0
9:8	V10	PAT view for initiator 10	RW	0x0
7	W9	Write-enable for V9 bit field Write 0x0: V9 field is unchanged Write 0x1: V9 field is updated	RW	0
6	RESERVED	Reserved	RW W0Only	0
5:4	V9	PAT view for initiator 9	RW	0x0
3	W8	Write-enable for V8 bit field Write 0x0: V8 field is unchanged Write 0x1: V8 field is updated	RW	0
2	RESERVED	Reserved	RW W0Only	0
1:0	V8	PAT view for initiator 8	RW	0x0

Table 15-63. Register Call Summary for Register DMM_PAT_VIEW1

Dynamic Memory Manager

- DMM Integration: [0]
- DMM Concepts: [1] [2]
- Configuration Settings and LUT Refill: [3] [4]
- PAT Programming Model: [5]
- DMM Register Summary: [6]

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Table 15-64. DMM_PAT_VIEW_MAP_i

Address Offset	0x0000 0440 + (0x4 * i)	**Index**	i = 0 to 3
Physical Address	0x4E00 0440 + (0x4 * i)	**Instance**	DMM
Description	PAT view mapping register n = 0 for the first view mapping register, n = 1 for the second view mapping register.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ACCESS_PAGE	RESERVED			CONT_PAGE				ACCESS_32	RESERVED			CONT_32				ACCESS_16	RESERVED			CONT_16				ACCESS_8	RESERVED			CONT_8			

Bits	Field Name	Description	Type	Reset
31	ACCESS_PAGE	Kind of access for this page mode container in view mapping n 0x0: Direct access, container base address given in CONT_PAGE 0x1:Indirect access through the LUT indexed by CONT_PAGE	RW	0
30:28	RESERVED	Reserved	RW W0Only	0x0
27:24	CONT_PAGE	Container for page mode in view mapping n	RW	0x0
23	ACCESS_32	Kind of access for this 32-bit mode container in view mapping n 0x0: Direct access, container base address given in CONT_32 0x1: Indirect access through the LUT indexed by CONT_32	RW	0
22:20	RESERVED	Reserved	RW W0Only	0x0
19:16	CONT_32	Container for 32-bit mode in view mapping n	RW	0x0
15	ACCESS_16	Kind of access for this 16-bit mode container in view mapping n 0x0: Direct access, container base address given in CONT_16 0x1: Indirect access through the LUT indexed by CONT_16	RW	0
14:12	RESERVED	Reserved	RW W0Only	0x0
11:8	CONT_16	Container for 16-bit mode in view mapping n	RW	0x0
7	ACCESS_8	Kind of access for this 8-bit mode container in view mapping n 0x0: Direct access, container base address given in CONT_8 0x1: Indirect access through the LUT indexed by CONT_8	RW	0
6:4	RESERVED	Reserved	RW W0Only	0x0
3:0	CONT_8	Container for 8-bit mode in view mapping n	RW	0x0

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Table 15-65. Register Call Summary for Register DMM_PAT_VIEW_MAP_i

Dynamic Memory Manager

- DMM Integration: [0]
- DMM Concepts: [1] [2] [3] [4] [5] [6] [7]
- Configuration Settings and LUT Refill: [8]
- DMM Register Summary: [9]

Table 15-66. DMM_PAT_VIEW_MAP_BASE

Address Offset	0x0000 0460		
Physical Address	0x4E00 0460	**Instance**	DMM
Description	Base address of all view mappings		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BASE_ADDR	RESERVED																														

Bits	Field Name	Description	Type	Reset
31	BASE_ADDR	MSB of the PAT view mapping base address	RW	0
30:0	RESERVED	Reserved	RW W0Only	0x0000 0000

Table 15-67. Register Call Summary for Register DMM_PAT_VIEW_MAP_BASE

Dynamic Memory Manager

- DMM Integration: [0]
- DMM Concepts: [1]
- Configuration Settings and LUT Refill: [2]
- Aliased Tiled View Orientation Settings and LUT Refill: [3]
- PAT Programming Model: [4]
- DMM Register Summary: [5]

Table 15-68. DMM_PAT_IRQSTATUS_RAW

Address Offset	0x0000 0480		
Physical Address	0x4E00 0480	**Instance**	DMM
Description	Per-event raw interrupt status vector. Raw status is set even if the related event is not enabled. Write 1 to set the (raw) status, mostly for debug. n = 0 for the first interrupt status raw register, n = 1 for the second interrupt status raw register.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																ERR_LUT_MISS1	ERR_UPD_DATA1	ERR_UPD_CTRL1	ERR_UPD_AREA1	ERR_INV_DATA1	ERR_INV_DSC1	FILL_LST1	FILL_DSC1	ERR_LUT_MISS0	ERR_UPD_DATA0	ERR_UPD_CTRL0	ERR_UPD_AREA0	ERR_INV_DATA0	ERR_INV_DSC0	FILL_LST0	FILL_DSC0

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Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	RW W0Only	0x0000
15	ERR_LUT_MISS1	Access to a yet-to-be-refilled area event in area 4.n+1 Write 0x0: Keep current error event Read 0x0: No such error event Read 0x1: Error event happened Write 0x1: Set error event	RW W1toSet	0
14	ERR_UPD_DATA1	Data register update while refilling error event in area 4.n+1 Write 0x0: Keep current error event Read 0x0: No such error event Read 0x1: Error event happened Write 0x1: Set error event	RW W1toSet	0
13	ERR_UPD_CTRL1	Control register update while refilling error event in area 4.n+1 Write 0x0: Keep current error event Read 0x0: No such error event Read 0x1: Error event happened Write 0x1: Set error event	RW W1toSet	0
12	ERR_UPD_AREA1	Area register update while refilling error event in area 4.n+1 Write 0x0: Keep current error event Read 0x0: No such error event Read 0x1: Error event happened Write 0x1: Set error event	RW W1toSet	0
11	ERR_INV_DATA1	Invalid entry-table pointer error event in area 4.n+1 Write 0x0: Keep current error event Read 0x0: No such error event Read 0x1: Error event happened Write 0x1: Set error event	RW W1toSet	0
10	ERR_INV_DSC1	Invalid descriptor pointer error event in area 4.n+1 Write 0x0: Keep current error event Read 0x0: No such error event Read 0x1: Error event happened Write 0x1: Set error event	RW W1toSet	0
9	FILL_LST1	End of refill event for the last descriptor in area 4.n+1 Write 0x0: Keep area 1 refill done event Read 0x0: Area 1 is yet-to-be refilled Read 0x1: Area 1 is refilled Write 0x1: Set area 1 refill done event	RW W1toSet	0
8	FILL_DSC1	End of refill event for any descriptor in area 4.n+1 Write 0x0: Keep area 1 refill done event Read 0x0: Area 1 is yet-to-be refilled Read 0x1: Area 1 is refilled Write 0x1: Set area 1 refill done event	RW W1toSet	0
7	ERR_LUT_MISS0	Access to a yet-to-be-refilled area event in area 4.n Write 0x0: Keep current error event Read 0x0: No such error event Read 0x1: Error event happened Write 0x1: Set error event	RW W1toSet	0

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Bits	Field Name	Description	Type	Reset
6	ERR_UPD_DATA0	Data register update while refilling error event in area 4.n Write 0x0: Keep current error event Read 0x0: No such error event Read 0x1: Error event happened Write 0x1: Set error event	RW W1toSet	0
5	ERR_UPD_CTRL0	Control register update while refilling error event in area 4.n Write 0x0: Keep current error event Read 0x0: No such error event Read 0x1: Error event happened Write 0x1: Set error event	RW W1toSet	0
4	ERR_UPD_AREA0	Area register update while refilling error event in area 4.n Write 0x0: Keep current error event Read 0x0: No such error event Read 0x1: Error event happened Write 0x1: Set error event	RW W1toSet	0
3	ERR_INV_DATA0	Invalid entry-table pointer error event in area 4.n Write 0x0: Keep current error event Read 0x0: No such error event Read 0x1: Error event happened Write 0x1: Set error event	RW W1toSet	0
2	ERR_INV_DSC0	Invalid descriptor pointer error event in area 4.n Write 0x0: Keep current error event Read 0x0: No such error event Read 0x1: Error event happened Write 0x1: Set error event	RW W1toSet	0
1	FILL_LST0	End of refill event for the last descriptor in area 4.n Write 0x0: Keep area 0 refill done event Read 0x0: Area 0 is yet-to-be refilled Read 0x1: Area 0 is refilled Write 0x1: Set area 0 refill done event	RW W1toSet	0
0	FILL_DSC0	End of refill event for any descriptor in area 4.n Write 0x0: Keep area 0 refill done event Read 0x0: Area 0 is yet-to-be refilled Read 0x1: Area 0 is refilled Write 0x1: Set area 0 refill done event	RW W1toSet	0

Table 15-69. Register Call Summary for Register DMM_PAT_IRQSTATUS_RAW

Dynamic Memory Manager

- DMM Interrupt Requests: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23] [24] [25] [26] [27] [28] [29] [30] [31]
- DMM Register Summary: [32]

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Table 15-70. DMM_PAT_IRQSTATUS

Address Offset	0x0000 0490		
Physical Address	0x4E00 0490	**Instance**	DMM
Description	Per-event "enabled" interrupt status vector. Enabled status is not set unless the event is enabled. Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, that is, even if not enabled). n = 0 for the first interrupt status register, n = 1 for the second interrupt status register.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																ERR_LUT_MISS1	ERR_UPD_DATA1	ERR_UPD_CTRL1	ERR_UPD_AREA1	ERR_INV_DATA1	ERR_INV_DSC1	FILL_LST1	FILL_DSC1	ERR_LUT_MISS0	ERR_UPD_DATA0	ERR_UPD_CTRL0	ERR_UPD_AREA0	ERR_INV_DATA0	ERR_INV_DSC0	FILL_LST0	FILL_DSC0

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	RW W0Only	0x0000
15	ERR_LUT_MISS1	Access to a yet-to-be-refilled area event in area 4.n+1 Write 0x0: Keep current maskable error event Read 0x0: No such error event or this event is masked Read 0x1: Error event happened Write 0x1: Clear this maskable error event	RW W1toClr	0
14	ERR_UPD_DATA1	Data register update while refilling error event in area 4.n+1 Write 0x0: Keep current maskable error event Read 0x0: No such error event or this event is masked Read 0x1: Error event happened Write 0x1: Clear this maskable error event	RW W1toClr	0
13	ERR_UPD_CTRL1	Control register update while refilling error event in area 4.n+1 Write 0x0: Keep current maskable error event Read 0x0: No such error event or this event is masked Read 0x1: Error event happened Write 0x1: Clear this maskable error event	RW W1toClr	0
12	ERR_UPD_AREA1	Area register update while refilling error event in area 4.n+1 Write 0x0: Keep current maskable error event Read 0x0: No such error event or this event is masked Read 0x1: Error event happened Write 0x1: Clear this maskable error event	RW W1toClr	0
11	ERR_INV_DATA1	Invalid entry-table pointer error event in area 4.n+1 Write 0x0: Keep current maskable error event Read 0x0: No such error event or this event is masked Read 0x1: Error event happened Write 0x1: Clear this maskable error event	RW W1toClr	0
10	ERR_INV_DSC1	Invalid descriptor pointer error event in area 4.n+1 Write 0x0: Keep current maskable error event Read 0x0: No such error event or this event is masked Read 0x1: Error event happened Write 0x1: Clear this maskable error event	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
9	FILL_LST1	End of refill event for the last descriptor in area 4.n+1 Write 0x0: Keep current area refill done maskable event Read 0x0: Current area is yet-to-be refilled or this event is masked Read 0x1: Current area is refilled Write 0x1: Clear current area refill done maskable event	RW W1toClr	0
8	FILL_DSC1	End of refill event for any descriptor in area 4.n+1 Write 0x0: Keep current area refill done maskable event Read 0x0: Current area is yet-to-be refilled or this event is masked Read 0x1: Current area is refilled Write 0x1: Clear current area refill done maskable event	RW W1toClr	0
7	ERR_LUT_MISS0	Access to a yet-to-be-refilled area event in area 4.n Write 0x0: Keep current maskable error event Read 0x0: No such error event or this event is masked Read 0x1: Error event happened Write 0x1: Clear this maskable error event	RW W1toClr	0
6	ERR_UPD_DATA0	Data register update while refilling error event in area 4.n Write 0x0: Keep current maskable error event Read 0x0: No such error event or this event is masked Read 0x1: Error event happened Write 0x1: Clear this maskable error event	RW W1toClr	0
5	ERR_UPD_CTRL0	Control register update while refilling error event in area 4.n Write 0x0: Keep current maskable error event Read 0x0: No such error event or this event is masked Read 0x1: Error event happened Write 0x1: Clear this maskable error event	RW W1toClr	0
4	ERR_UPD_AREA0	Area register update while refilling error event in area 4.n Write 0x0: Keep current maskable error event Read 0x0: No such error event or this event is masked Read 0x1: Error event happened Write 0x1: Clear this maskable error event	RW W1toClr	0
3	ERR_INV_DATA0	Invalid entry-table pointer error event in area 4.n Write 0x0: Keep current maskable error event Read 0x0: No such error event or this event is masked Read 0x1: Error event happened Write 0x1: Clear this maskable error event	RW W1toClr	0
2	ERR_INV_DSC0	Invalid descriptor pointer error event in area 4.n Write 0x0: Keep current maskable error event Read 0x0: No such error event or this event is masked Read 0x1: Error event happened Write 0x1: Clear this maskable error event	RW W1toClr	0
1	FILL_LST0	End of refill event for the last descriptor in area 4.n Write 0x0: Keep current area refill done maskable event Read 0x0: Current area is yet-to-be refilled or this event is masked Read 0x1: Current area is refilled Write 0x1: Clear current area refill done maskable event	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
0	FILL_DSC0	End of refill event for any descriptor in area 4.n Write 0x0: Keep current area refill done maskable event Read 0x0: Current area is yet-to-be refilled or this event is masked Read 0x1: Current area is refilled Write 0x1: Clear current area refill done maskable event	RW W1toClr	0

Table 15-71. Register Call Summary for Register DMM_PAT_IRQSTATUS

Dynamic Memory Manager

- DMM Interrupt Requests: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23] [24] [25] [26] [27] [28] [29] [30] [31]
- Error Handling: [32] [33]
- DMM Register Summary: [34]

Table 15-72. DMM_PAT_IRQENABLE_SET

Address Offset	0x0000 04A0		
Physical Address	0x4E00 04A0	**Instance**	DMM
Description	Per-event interrupt enable bit vector. Write 1 to set (enable interrupt). Readout equal to corresponding _CLR register. n = 0 for the first interrupt enable set register, n = 1 for the second interrupt enable set register.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																ERR_LUT_MISS1	ERR_UPD_DATA1	ERR_UPD_CTRL1	ERR_UPD_AREA1	ERR_INV_DATA1	ERR_INV_DSC1	FILL_LST1	FILL_DSC1	ERR_LUT_MISS0	ERR_UPD_DATA0	ERR_UPD_CTRL0	ERR_UPD_AREA0	ERR_INV_DATA0	ERR_INV_DSC0	FILL_LST0	FILL_DSC0

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	RW W0Only	0x0000
15	ERR_LUT_MISS1	Unexpected access to a yet-to-be-refilled area interrupt source mask for area 4.n+1 Write 0x0: Keep current mask of this interrupt source Read 0x0: This interrupt source is disabled (masked) Read 0x1: This interrupt source is enabled (unmasked) Write 0x1: Enable (unmask) this interrupt source	RW W1toSet	0
14	ERR_UPD_DATA1	Unexpected data register update while refilling interrupt source mask for area 4.n+1 Write 0x0: Keep current mask of this interrupt source Read 0x0: This interrupt source is disabled (masked) Read 0x1: This interrupt source is enabled (unmasked) Write 0x1: Enable (unmask) this interrupt source	RW W1toSet	0
13	ERR_UPD_CTRL1	Unexpected control register update while refilling interrupt source mask for area 4.n+1 Write 0x0: Keep current mask of this interrupt source Read 0x0: This interrupt source is disabled (masked) Read 0x1: This interrupt source is enabled (unmasked) Write 0x1: Enable (unmask) this interrupt source	RW W1toSet	0

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Bits	Field Name	Description	Type	Reset
12	ERR_UPD_AREA1	Unexpected area register update while refilling interrupt source mask for area 4.n+1 Write 0x0: Keep current mask of this interrupt source Read 0x0: This interrupt source is disabled (masked) Read 0x1: This interrupt source is enabled (unmasked) Write 0x1: Enable (unmask) this interrupt source	RW W1toSet	0
11	ERR_INV_DATA1	Invalid entry-table pointer interrupt source mask for area 4.n+1 Write 0x0: Keep current mask of this interrupt source Read 0x0: This interrupt source is disabled (masked) Read 0x1: This interrupt source is enabled (unmasked) Write 0x1: Enable (unmask) this interrupt source	RW W1toSet	0
10	ERR_INV_DSC1	Invalid descriptor pointer interrupt source mask for area 4.n+1 Write 0x0: Keep current mask of this interrupt source Read 0x0: This interrupt source is disabled (masked) Read 0x1: This interrupt source is enabled (unmasked) Write 0x1: Enable (unmask) this interrupt source	RW W1toSet	0
9	FILL_LST1	End of refill interrupt source mask for the last descriptor in area 4.n+1 Write 0x0: Keep current mask of this interrupt source Read 0x0: This interrupt source is disabled (masked) Read 0x1: This interrupt source is enabled (unmasked) Write 0x1: Enable (unmask) this interrupt source	RW W1toSet	0
8	FILL_DSC1	End of refill interrupt source mask for any descriptor in area 4.n+1 Write 0x0: Keep current mask of this interrupt source Read 0x0: This interrupt source is disabled (masked) Read 0x1: This interrupt source is enabled (unmasked) Write 0x1: Enable (unmask) this interrupt source	RW W1toSet	0
7	ERR_LUT_MISS0	Unexpected access to a yet-to-be-refilled area interrupt source mask for area 4.n Write 0x0: Keep current mask of this interrupt source Read 0x0: This interrupt source is disabled (masked) Read 0x1: This interrupt source is enabled (unmasked) Write 0x1: Enable (unmask) this interrupt source	RW W1toSet	0
6	ERR_UPD_DATA0	Unexpected data register update while refilling interrupt source mask for area 4.n Write 0x0: Keep current mask of this interrupt source Read 0x0: This interrupt source is disabled (masked) Read 0x1: This interrupt source is enabled (unmasked) Write 0x1: Enable (unmask) this interrupt source	RW W1toSet	0
5	ERR_UPD_CTRL0	Unexpected control register update while refilling interrupt source mask for area 4.n Write 0x0: Keep current mask of this interrupt source Read 0x0: This interrupt source is disabled (masked) Read 0x1: This interrupt source is enabled (unmasked) Write 0x1: Enable (unmask) this interrupt source	RW W1toSet	0

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Bits	Field Name	Description	Type	Reset
4	ERR_UPD_AREA0	Unexpected area register update while refilling interrupt source mask for area 4.n Write 0x0: Keep current mask of this interrupt source Read 0x0: This interrupt source is disabled (masked) Read 0x1: This interrupt source is enabled (unmasked) Write 0x1: Enable (unmask) this interrupt source	RW W1toSet	0
3	ERR_INV_DATA0	Invalid entry-table pointer interrupt source mask for area 4.n Write 0x0: Keep current mask of this interrupt source Read 0x0: This interrupt source is disabled (masked) Read 0x1: This interrupt source is enabled (unmasked) Write 0x1: Enable (unmask) this interrupt source	RW W1toSet	0
2	ERR_INV_DSC0	Invalid descriptor pointer interrupt source mask for area 4.n Write 0x0: Keep current mask of this interrupt source Read 0x0: This interrupt source is disabled (masked) Read 0x1: This interrupt source is enabled (unmasked) Write 0x1: Enable (unmask) this interrupt source	RW W1toSet	0
1	FILL_LST0	End of refill interrupt source mask for the last descriptor in area 4.n Write 0x0: Keep current mask of this interrupt source Read 0x0: This interrupt source is disabled (masked) Read 0x1: This interrupt source is enabled (unmasked) Write 0x1: Enable (unmask) this interrupt source	RW W1toSet	0
0	FILL_DSC0	End of refill interrupt source mask for any descriptor in area 4.n Write 0x0: Keep current mask of this interrupt source Read 0x0: This interrupt source is disabled (masked) Read 0x1: This interrupt source is enabled (unmasked) Write 0x1: Enable (unmask) this interrupt source	RW W1toSet	0

Table 15-73. Register Call Summary for Register DMM_PAT_IRQENABLE_SET

Dynamic Memory Manager

- DMM Interrupt Requests: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23] [24] [25] [26] [27] [28] [29] [30] [31]
- Error Handling: [32] [33]
- DMM Register Summary: [34]

Table 15-74. DMM_PAT_IRQENABLE_CLR

Address Offset	0x0000 04B0		
Physical Address	0x4E00 04B0	**Instance**	DMM
Description	Per-event interrupt enable bit vector. Write 1 to clear (disable interrupt). Readout equal to corresponding _SET register. n = 0 for the first interrupt enable clear register, n = 1 for the second interrupt enable clear register.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																ERR_LUT_MISS1	ERR_UPD_DATA1	ERR_UPD_CTRL1	ERR_UPD_AREA1	ERR_INV_DATA1	ERR_INV_DSC1	FILL_LST1	FILL_DSC1	ERR_LUT_MISS0	ERR_UPD_DATA0	ERR_UPD_CTRL0	ERR_UPD_AREA0	ERR_INV_DATA0	ERR_INV_DSC0	FILL_LST0	FILL_DSC0

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	RW W0Only	0x0000
15	ERR_LUT_MISS1	Unexpected access to a yet-to-be-refilled area interrupt source mask for area 4.n+1 Write 0x0: Keep current mask of this interrupt source Read 0x0: This interrupt source is disabled (masked) Read 0x1: This interrupt source is enabled (unmasked) Write 0x1: Disable (mask) this interrupt source	RW W1toClr	0
14	ERR_UPD_DATA1	Unexpected data register update while refilling interrupt source mask for area 4.n+1 Write 0x0: Keep current mask of this interrupt source Read 0x0: This interrupt source is disabled (masked) Read 0x1: This interrupt source is enabled (unmasked) Write 0x1: Disable (mask) this interrupt source	RW W1toClr	0
13	ERR_UPD_CTRL1	Unexpected control register update while refilling interrupt source mask for area 4.n+1 Write 0x0: Keep current mask of this interrupt source Read 0x0: This interrupt source is disabled (masked) Read 0x1: This interrupt source is enabled (unmasked) Write 0x1: Disable (mask) this interrupt source	RW W1toClr	0
12	ERR_UPD_AREA1	Unexpected area register update while refilling interrupt source mask for area 4.n+1 Write 0x0: Keep current mask of this interrupt source Read 0x0: This interrupt source is disabled (masked) Read 0x1: This interrupt source is enabled (unmasked) Write 0x1: Disable (mask) this interrupt source	RW W1toClr	0
11	ERR_INV_DATA1	Invalid entry-table pointer interrupt source mask for area 4.n+1 Write 0x0: Keep current mask of this interrupt source Read 0x0: This interrupt source is disabled (masked) Read 0x1: This interrupt source is enabled (unmasked) Write 0x1: Disable (mask) this interrupt source	RW W1toClr	0
10	ERR_INV_DSC1	Invalid descriptor pointer interrupt source mask for area 4.n+1 Write 0x0: Keep current mask of this interrupt source Read 0x0: This interrupt source is disabled (masked) Read 0x1: This interrupt source is enabled (unmasked) Write 0x1: Disable (mask) this interrupt source	RW W1toClr	0
9	FILL_LST1	End of refill interrupt source mask for the last descriptor in area 4.n+1 Write 0x0: Keep current mask of this interrupt source Read 0x0: This interrupt source is disabled (masked) Read 0x1: This interrupt source is enabled (unmasked) Write 0x1: Disable (mask) this interrupt source	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
8	FILL_DSC1	End of refill interrupt source mask for any descriptor in area 4.n+1 Write 0x0: Keep current mask of this interrupt source Read 0x0: This interrupt source is disabled (masked) Read 0x1: This interrupt source is enabled (unmasked) Write 0x1: Disable (mask) this interrupt source	RW W1toClr	0
7	ERR_LUT_MISS0	Unexpected access to a yet-to-be-refilled area interrupt source mask for area 4.n Write 0x0: Keep current mask of this interrupt source Read 0x0: This interrupt source is disabled (masked) Read 0x1: This interrupt source is enabled (unmasked) Write 0x1: Disable (mask) this interrupt source	RW W1toClr	0
6	ERR_UPD_DATA0	Unexpected data register update while refilling interrupt source mask for area 4.n Write 0x0: Keep current mask of this interrupt source Read 0x0: This interrupt source is disabled (masked) Read 0x1: This interrupt source is enabled (unmasked) Write 0x1: Disable (mask) this interrupt source	RW W1toClr	0
5	ERR_UPD_CTRL0	Unexpected control register update while refilling interrupt source mask for area 4.n Write 0x0: Keep current mask of this interrupt source Read 0x0: This interrupt source is disabled (masked) Read 0x1: This interrupt source is enabled (unmasked) Write 0x1: Disable (mask) this interrupt source	RW W1toClr	0
4	ERR_UPD_AREA0	Unexpected area register update while refilling interrupt source mask for area 4.n Write 0x0: Keep current mask of this interrupt source Read 0x0: This interrupt source is disabled (masked) Read 0x1: This interrupt source is enabled (unmasked) Write 0x1: Disable (mask) this interrupt source	RW W1toClr	0
3	ERR_INV_DATA0	Invalid entry-table pointer interrupt source mask for area 4.n Write 0x0: Keep current mask of this interrupt source Read 0x0: This interrupt source is disabled (masked) Read 0x1: This interrupt source is enabled (unmasked) Write 0x1: Disable (mask) this interrupt source	RW W1toClr	0
2	ERR_INV_DSC0	Invalid descriptor pointer interrupt source mask for area 4.n Write 0x0: Keep current mask of this interrupt source Read 0x0: This interrupt source is disabled (masked) Read 0x1: This interrupt source is enabled (unmasked) Write 0x1: Disable (mask) this interrupt source	RW W1toClr	0
1	FILL_LST0	End of refill interrupt source mask for the last descriptor in area 4.n Write 0x0: Keep current mask of this interrupt source Read 0x0: This interrupt source is disabled (masked) Read 0x1: This interrupt source is enabled (unmasked) Write 0x1: Disable (mask) this interrupt source	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
0	FILL_DSC0	End of refill interrupt source mask for any descriptor in area 4.n Write 0x0: Keep current mask of this interrupt source Read 0x0: This interrupt source is disabled (masked) Read 0x1: This interrupt source is enabled (unmasked) Write 0x1: Disable (mask) this interrupt source	RW W1toClr	0

Table 15-75. Register Call Summary for Register DMM_PAT_IRQENABLE_CLR

Dynamic Memory Manager

- DMM Interrupt Requests: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23] [24] [25] [26] [27] [28] [29] [30] [31]
- Error Handling: [32] [33]
- DMM Register Summary: [34]

Table 15-76. DMM_PAT_STATUS_i

Address Offset	0x0000 04C0 + (0x4 * i)	**Index**	i = 0 to 3
Physical Address	0x4E00 04C0 + (0x4 * i)	**Instance**	DMM
Description	Status register for each refill engine n = 0 for the first engine status register, n = 1 for the second engine status register.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								CNT								ERROR						RESERVED		BYPASSED	RESERVED		LINKED	DONE	RUN	VALID	READY

Bits	Field Name	Description	Type	Reset
31:25	RESERVED	Reserved	R	0x00
24:16	CNT	Counter of remaining lines to reload for engine n	R	0x000
15:10	ERROR	Error happened in engine n Read 0x0: No error Read 0x1: Invalid descriptor provided Read 0x2: Invalid data pointer provided Read 0x4: Unexpected area register update while refilling Read 0x8: Unexpected control register update while refilling Read 0x10: Unexpected data register update while refilling Read 0x20: Unexpected access to a yet-to-be-refilled location	R	0x00
9:8	RESERVED	Reserved	R	0x0
7	BYPASSED	Engine n is bypassed. Direct access to the LUT is provided.	R	0
6:5	RESERVED	Reserved	R	0x0
4	LINKED	Area reconfiguration link asserted for engine n	R	0
3	DONE	Area reloading finished for engine n	R	0
2	RUN	Area currently reloading for engine n	R	0
1	VALID	Valid area description for engine n	R	0
0	READY	Area registers ready for engine n	R	1

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Table 15-77. Register Call Summary for Register DMM_PAT_STATUS_i

Dynamic Memory Manager

- DMM Interrupt Requests: [0] [1]
- DMM Internal Macro-Architecture: [2]
- Simple Manual Area Refill: [3] [4]
- Single Auto-Configured Area Refill: [5] [6]
- Chained Auto-Configured Area Refill: [7] [8] [9]
- Synchronized Auto-Configured Area Refill: [10] [11] [12]
- Cyclic Synchronized Auto-Configured Area Refill: [13]
- DMM Register Summary: [14]

Table 15-78. DMM_PAT_DESCR_i

Address Offset	0x0000 0500 + (0x10 * i)	**Index**	i = 0 to 3
Physical Address	0x4E00 0500 + (0x10 * i)	**Instance**	DMM
Description	Physical address of the next table refill descriptor n = 0 for the descriptor register of the first engine, n = 1 for the descriptor register of the second engine. Writing to this register aborts the current ongoing area reload and resets the corresponding DMM_PAT_AREA__x, DMM_PAT_CTRL__x and DMM_PAT_DATA__x registers.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR																												RESERVED			

Bits	Field Name	Description	Type	Reset
31:4	ADDR	Physical address of the next table refill descriptor of engine n	RW WtoClr	0x0000000
3:0	RESERVED	Reserved	RW W0Only	0x0

Table 15-79. Register Call Summary for Register DMM_PAT_DESCR_i

Dynamic Memory Manager

- DMM Integration: [0]
- DMM Internal Macro-Architecture: [1] [2] [3]
- Single Auto-Configured Area Refill: [4]
- Chained Auto-Configured Area Refill: [5]
- Synchronized Auto-Configured Area Refill: [6]
- Cyclic Synchronized Auto-Configured Area Refill: [7] [8]
- DMM Register Summary: [9]

Table 15-80. DMM_PAT_AREA_i

Address Offset	0x0000 0504 + (0x10 * i)	**Index**	i = 0 to 3
Physical Address	0x4E00 0504 + (0x10 * i)	**Instance**	DMM
Description	Area definition for DMM physical address translator n = 0 for the area register of the first engine, n = 1 for the area register of the second engine.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	Y1							X1								RESERVED	Y0							X0							

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Bits	Field Name	Description	Type	Reset
31	RESERVED	Reserved	RW W0Only	0
30:24	Y1	Y-coordinate of the bottom-right corner of the PAT area for engine n	RW	0x00
23:16	X1	X-coordinate of the bottom-right corner of the PAT area for engine n	RW	0x00
15	RESERVED	Reserved	RW W0Only	0
14:8	Y0	Y-coordinate of the top-left corner of the PAT area for engine n	RW	0x00
7:0	X0	X-coordinate of the top-left corner of the PAT area for engine n	RW	0x00

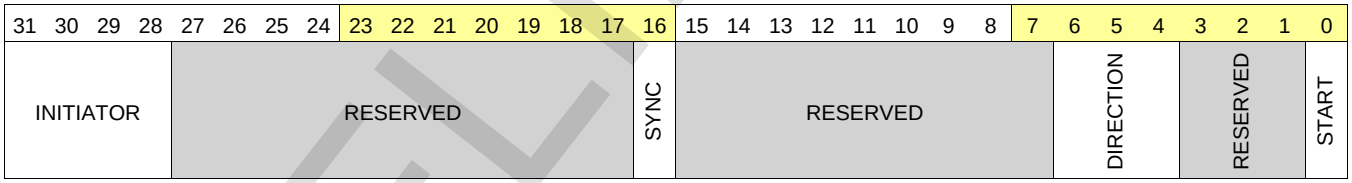
Table 15-81. Register Call Summary for Register DMM_PAT_AREA_i

Dynamic Memory Manager

- DMM Integration: [0]
- DMM Concepts: [1]
- DMM Internal Macro-Architecture: [2] [3] [4]
- Simple Manual Area Refill: [5]
- Configuration Settings and LUT Refill: [6]
- TILER Page Mapping: [7]
- DMM Register Summary: [8]

Table 15-82. DMM_PAT_CTRL_i

Address Offset	0x0000 0508 + (0x10 * i)	**Index**	i = 0 to 3
Physical Address	0x4E00 0508 + (0x10 * i)	**Instance**	DMM
Description	DMM physical address translator control register n = 0 for the control register of the first engine, n = 1 for the control register of the second engine.		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:28	INITIATOR	DMM PAT initiator for synchronization in engine n	RW	0x0
27:17	RESERVED	Reserved	RW W0Only	0x000
16	SYNC	DMM PAT table reload synchronization for engine n 0x0: Not synchronized 0x1: Synchronized	RW	0
15:7	RESERVED	Reserved	RW W0Only	0x000
6:4	DIRECTION	Direction of this PAT table refill for engine n	RW	0x0
3:1	RESERVED	Reserved	RW W0Only	0x0
0	START	Starting a PAT table refill with engine n	RW	0

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Table 15-83. Register Call Summary for Register DMM_PAT_CTRL_i

Dynamic Memory Manager

- DMM Integration: [0]
- DMM Internal Macro-Architecture: [1] [2] [3] [4] [5]
- Simple Manual Area Refill: [6] [7]
- Cyclic Synchronized Auto-Configured Area Refill: [8]
- Configuration Settings and LUT Refill: [9] [10]
- Aliased Tiled View Orientation Settings and LUT Refill: [11] [12] [13] [14] [15]
- DMM Register Summary: [16]

Table 15-84. DMM_PAT_DATA_i

Address Offset	0x0000 050C + (0x10 * i)	**Index**	i = 0 to 3
Physical Address	0x4E00 050C + (0x10 * i)	**Instance**	DMM
Description	Physical address of the current table refill entry data n = 0 for the data register of the first engine, n = 1 for the data register of the second engine.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR																												RESERVED			

Bits	Field Name	Description	Type	Reset
31:4	ADDR	Physical address of the current table refill entry data or single actual entry data when in manual mode for engine n	RW	0x0000000
3:0	RESERVED	Reserved	RW W0Only	0x0

Table 15-85. Register Call Summary for Register DMM_PAT_DATA_i

Dynamic Memory Manager

- DMM Integration: [0]
- DMM Concepts: [1]
- DMM Internal Macro-Architecture: [2] [3] [4]
- Simple Manual Area Refill: [5]
- Configuration Settings and LUT Refill: [6]
- DMM Register Summary: [7]

Table 15-86. DMM_PEG_HWINFO

Address Offset	0x0000 0608		
Physical Address	0x4E00 0608	**Instance**	DMM
Description	DMM hardware configuration for PEG		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								PRIO_CNT							

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Bits	Field Name	Description	Type	Reset
31:7	RESERVED	Reserved	R	0x0000000
6:0	PRIO_CNT	Number of PEG priority entries Read 0x1: One priority entry Read 0x2: Two priority entries Read 0x4: Four priority entries Read 0x8: Eight priority entries Read 0x10: Sixteen priority entries Read 0x20: Thirty-two priority entries Read 0x40: Sixty-four priority entries	R	0x40

Table 15-87. Register Call Summary for Register DMM_PEG_HWINFO

Dynamic Memory Manager
- DMM Configuration: [0]
- DMM Register Summary: [1]

Table 15-88. DMM_PEG_PRIO_k

Address Offset	0x0000 0620 + (0x4 * k)	**Index**	k = 0 to 7
Physical Address	0x4E00 0620 + (0x4 * k)	**Instance**	DMM
Description	DMM PEG Priority register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
W7	P7			W6	P6			W5	P5			W4	P4			W3	P3			W2	P2			W1	P1			W0	P0		

Bits	Field Name	Description	Type	Reset
31	W7	Write-enable for P7 bit field Write 0x0: P7 field is unchanged Write 0x1: P7 field is updated	RW	0
30:28	P7	Priority for initiator 8.k+7	RW	0x4
27	W6	Write-enable for P6 bit field Write 0x0: P6 field is unchanged Write 0x1: P6 field is updated	RW	0
26:24	P6	Priority for initiator 8.k+6	RW	0x4
23	W5	Write-enable for P5 bit field Write 0x0: P5 field is unchanged Write 0x1: P5 field is updated	RW	0
22:20	P5	Priority for initiator 8.k+5	RW	0x4
19	W4	Write-enable for P4 bit field Write 0x0: P4 field is unchanged Write 0x1: P4 field is updated	RW	0
18:16	P4	Priority for initiator 8.k+4	RW	0x4
15	W3	Write-enable for P3 bit field Write 0x0: P3 field is unchanged Write 0x1: P3 field is updated	RW	0
14:12	P3	Priority for initiator 8.k+3	RW	0x4

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Bits	Field Name	Description	Type	Reset
11	W2	Write-enable for P2 bit field Write 0x0: P2 field is unchanged Write 0x1: P2 field is updated	RW	0
10:8	P2	Priority for initiator 8.k+2	RW	0x4
7	W1	Write-enable for P1 bit field Write 0x0: P1 field is unchanged Write 0x1: P1 field is updated	RW	0
6:4	P1	Priority for initiator 8.k+1	RW	0x4
3	W0	Write-enable for P0 bit field Write 0x0: P0 field is unchanged Write 0x1: P0 field is updated	RW	0
2:0	P0	Priority for initiator 8.k	RW	0x4

Table 15-89. Register Call Summary for Register DMM_PEG_PRIO_k

Dynamic Memory Manager
- DMM Integration: [0]
- DMM Internal Macro-Architecture: [1]
- Priority Settings: [2]
- DMM Register Summary: [3]

Table 15-90. DMM_PEG_PRIO_PAT

Address Offset	0x0000 0640		
Physical Address	0x4E00 0640	**Instance**	DMM
Description	DMM PEG priority register for the internal PAT engine.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												W_PAT	P_PAT		

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved	RW W0Only	0x0000000
3	W_PAT	Write-enable for P_PAT bit field Write 0x0: P_PAT field is updated Write 0x1: P_PAT field is unchanged	RW	0
2:0	P_PAT	Priority for PAT engine	RW	0x4

Table 15-91. Register Call Summary for Register DMM_PEG_PRIO_PAT

Dynamic Memory Manager
- DMM Integration: [0]
- DMM Internal Macro-Architecture: [1]
- Priority Settings: [2] [3]
- DMM Register Summary: [4]

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15.3 EMIF Controller

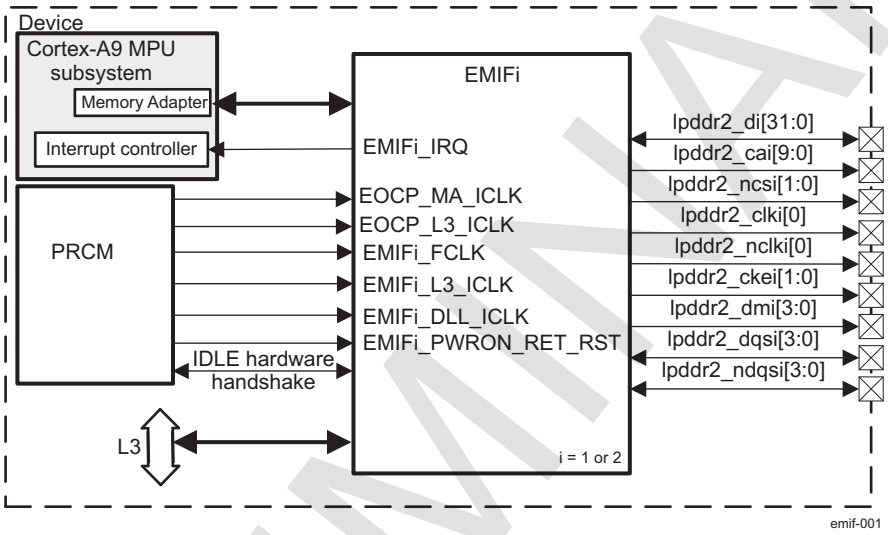
This section describes the features and functions of the external memory interface (EMIF) module of the device.

15.3.1 EMIF Module Overview

The EMIF module provides connectivity between the device and the LPDDR2-type memories and manages data bus read/write accesses between external memories, the microprocessor unit (MPU), and the direct memory access (DMA) controller.

The device includes two EMIF controllers. Figure 15-43 is an overview of the EMIF module.

Figure 15-43. EMIF Module Overview



15.3.1.1 EMIF Module Main Features

The EMIF module supports the following features:

- JEDEC standard-compliant LPDDR2-SDRAM (S2 and S4) and LPDDR2-NVM devices
- 2-GB SDRAM address ranges over two chip-selects (CSs) (1GB per CS) (configurable with the dynamic memory manager (DMM) module; see Section 15.2, *Dynamic Memory Manager*, for more information)
- Two independent CSs with their corresponding register sets and independent page tracking
- Both CSs must have the same memory type and size if they are both synchronous dynamic random access memory (SDRAM) or both non-volatile memory (NVM).

  LPDDR2-SDRAM can be used in parallel with LPDDR2-NVM and can have a different size.
- Flexible address muxing scheme, which permits the choosing of different bank mapping allocation by configuring the decoding order of the bank, column, and row address
- 16- or 32-bit data path to external SDRAM
- LPDDR2 devices with one, two, four, or eight internal banks
- Data bus widths:
  - 128-bit L3 interconnect data bus width
  - 16- and 32-bit SDRAM data bus widths
- CAS latencies: 3, 4, 5, 6, 7, and 8
- 256-, 512-, 1024-, and 2048-word page sizes
- Burst lengths: 8
- Sequential burst type

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- SDRAM auto initialization from reset or configuration change
- Bank interleaving across both CSs if the same memory type
- Self-refresh and precharge power-down modes for low power (per CS, manual entry/exit self-refresh and deep power-down modes)
- Deep power-down mode for low power
- Partial array self-refresh and temperature-controlled self-refresh modes for low power. Temperature-controlled self-refresh is supported only for mobile SDRAM having on-chip temperature sensor.
- Prioritized refresh
- Programmable SDRAM refresh rate and backlog counter
- Output impedance (ZQ) calibration
- Active power-down
- Temperature monitoring

15.3.1.2 Not Supported Features

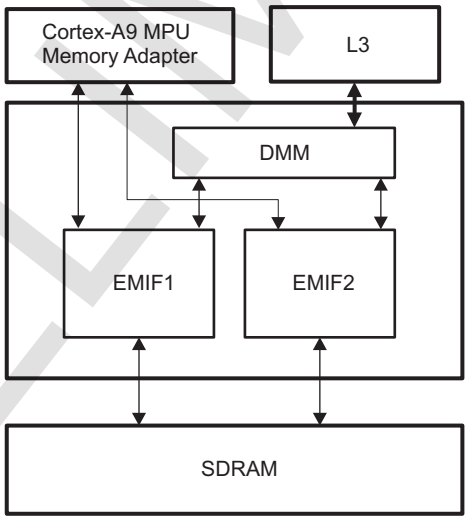
The EMIF module does not support:

- Interleave burst type
- Auto precharge
- Per-bank refreshes for LPDDR2-SDRAM

15.3.1.3 EMIF Overall Architecture

Figure 15-44 shows the EMIF connection with the surrounding modules.

Figure 15-44. EMIF Overall Architecture



15.3.2 EMIF Environment

This section describes the EMIF application fields from an environment point of view (external connections).

Figure 15-45 shows the EMIF generic configuration.

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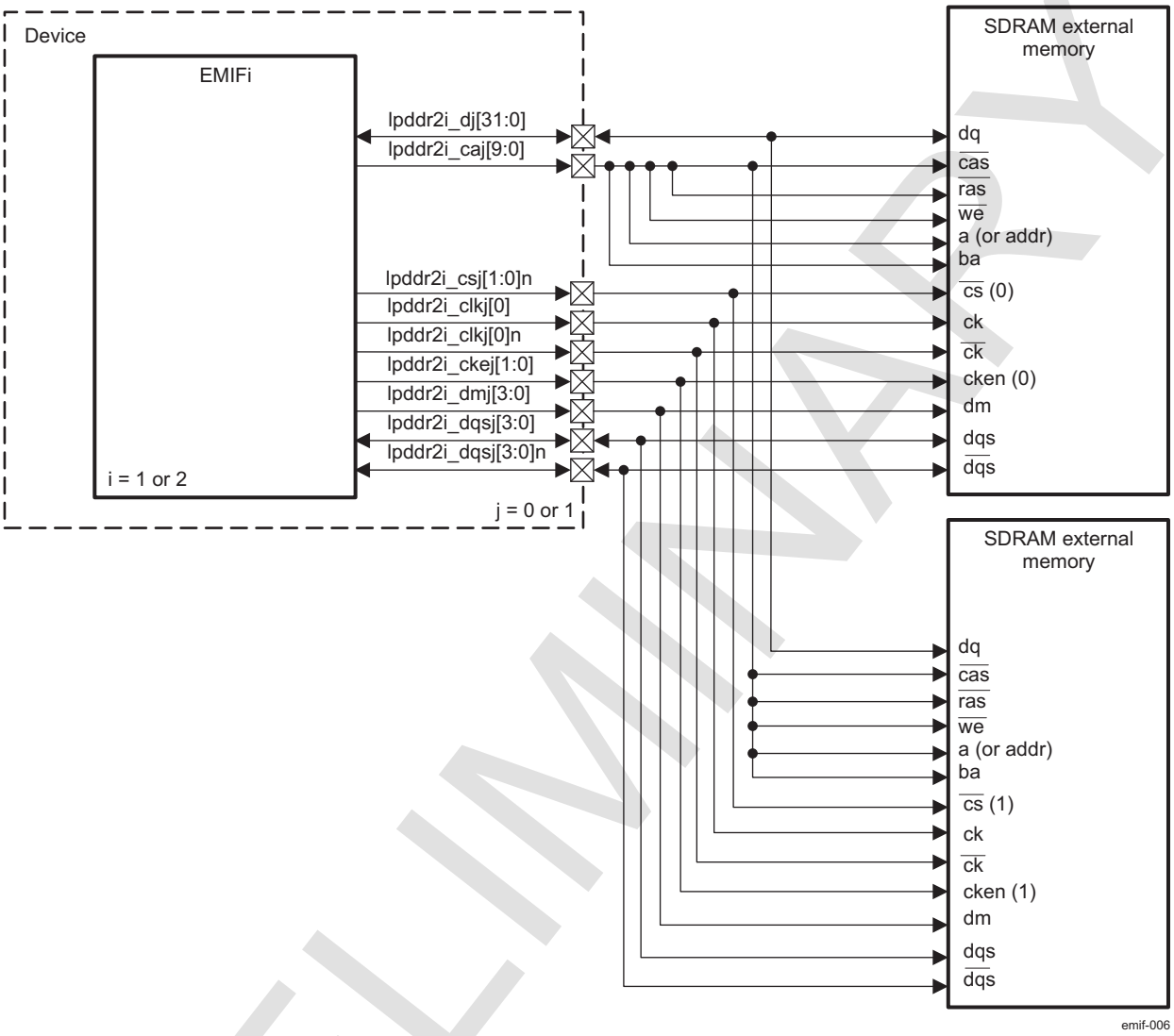
Figure 15-45. EMIF Generic Configuration



15.3.2.1 EMIF Signals

Table 15-92 describes the module signals and specifies their links to functions.

Table 15-92. I/O Signals

Signal	I/O [1]	Description
EMIF1		
lpddr21_dq[31:0]	I/O	Data bus
lpddr21_ca[9:0]	O	Double-data rate (DDR) command/address
lpddr21_ncs[1:0]	O	Chip selects 1–0 (active low)
lpddr21_clk	O	Clock
lpddr21_nclk	O	Clock invert
lpddr21_cke[1:0]	O	Clock enables 1–0
lpddr21_dm[3:0]	I/O	Data mask
lpddr21_dqs[3:0]	I/O	Data strobe
lpddr21_ndqs[3:0]	I/O	Data strobe invert

(1) I = Input; O = Output

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Table 15-92. I/O Signals (continued)

Signal	I/O [1]	Description
EMIF2		
lpddr22_dq[31:0]	I/O	Data bus
lpddr22_ca[9:0]	O	DDR command/address
lpddr22_ncs[1:0]	O	Chip selects 1–0 (active low)
lpddr22_clk	O	Clock
lpddr22_nclk	O	Clock invert
lpddr22_cke[1:0]	O	Clock enables 1–0
lpddr22_dm[3:0]	I/O	Data mask
lpddr22_dqs[3:0]	I/O	Data strobe
lpddr22_ndqs[3:0]	I/O	Data strobe invert

The CKE memory pin is dynamically driven by the SDRAM controller (SDRC) according to the memory interface activity. Each CS has its own CKE pin so that each CS can be controlled independently in terms of power-down, deep power-down, and self-refresh modes.

Each LPDDR2 channel (that is, each EMIF controller) can be connected to two external LPDDR2 memories. For more information, see Section 15.2, *Dynamic Memory Manager*.

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15.3.3 EMIF Integration

This section describes the integration of the module in the device, and includes information about clocks, resets, and hardware requests.

Figure 15-46 shows the integration of the EMIF1 module in the device.

Figure 15-46. EMIF1 Integration

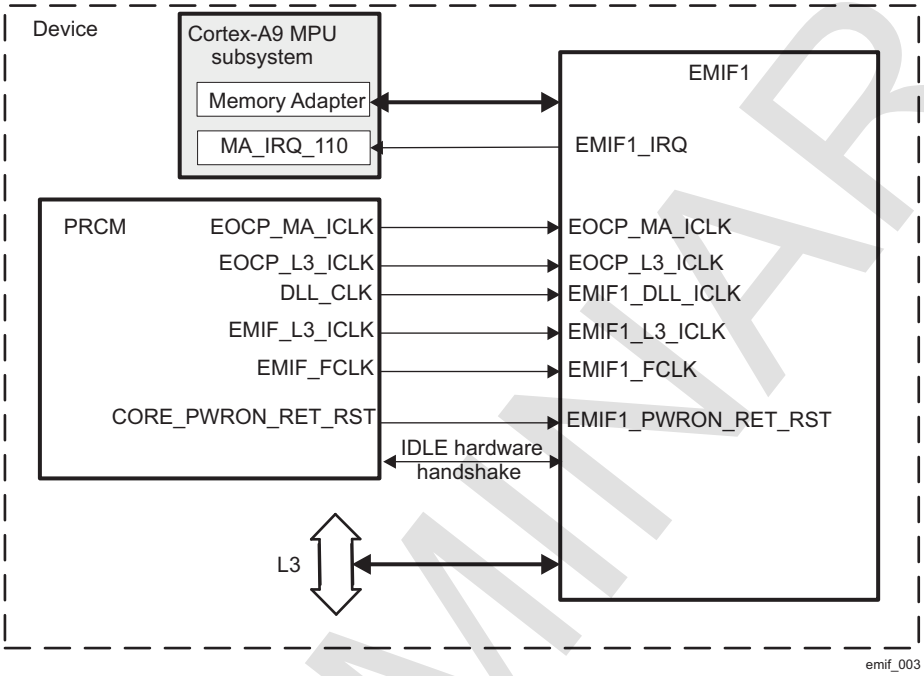
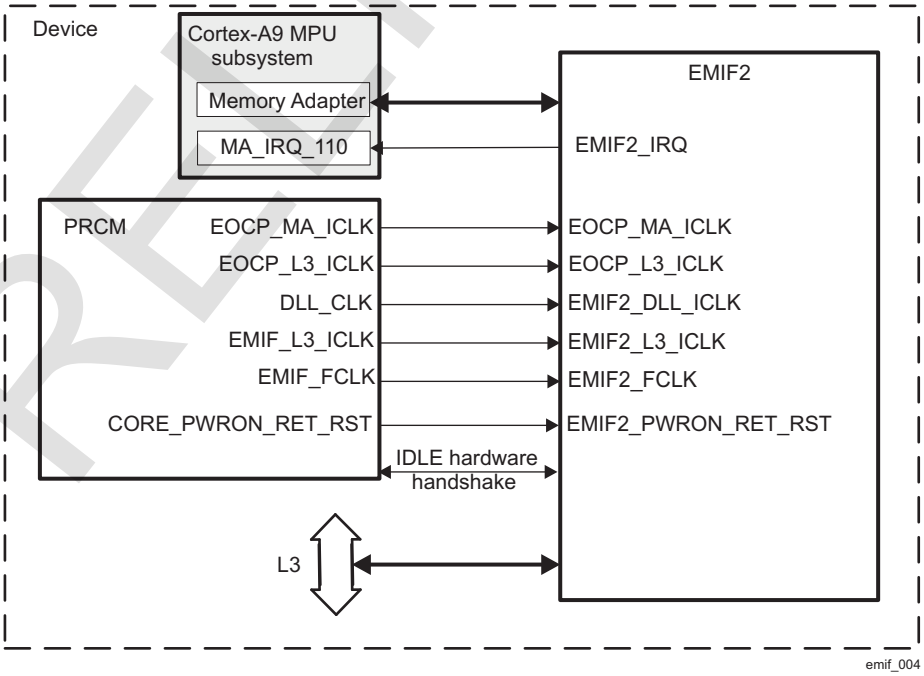


Figure 15-47 shows the integration of the EMIF2 module in the device.

Figure 15-47. EMIF2 Integration



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NOTE: For more information about the IDLE hardware handshake, see Chapter 3, *Power, Reset, and Clock Management*.

Table 15-93 through Table 15-95 summarize the integration of the module in the device.

Table 15-93. Integration Attributes

Module Instance	Attributes		
	Power Domain	Wake-Up Capability	Interconnect
EMIF1	PD_CORE	No	L3
EMIF2	PD_CORE	No	L3

Table 15-94. Clocks and Resets

Clocks				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
EMIF1	EMIF1_FCLK	EMIF_FCLK	PRCM	Functional
	EMIF1_L3_ICLK	EMIF_L3_ICLK	PRCM	Interface clock
	EOCP_MA_ICLK	EOCP_MA_ICLK	PRCM	Interface clock
	EOCP_L3_ICLK	EOCP_L3_ICLK	PRCM	Interface clock
	EMIF1_DLL_ICLK	DLL_CLK	PRCM	Interface clock
EMIF2	EMIF2_FCLK	EMIF_FCLK	PRCM	Functional
	EMIF2_L3_ICLK	EMIF_L3_ICLK	PRCM	Interface clock
	EOCP_MA_ICLK	EOCP_MA_ICLK	PRCM	Interface clock
	EOCP_L3_ICLK	EOCP_L3_ICLK	PRCM	Interface clock
	EMIF2_DLL_ICLK	DLL_CLK	PRCM	Interface clock
Resets				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
EMIF1	EMIF1_PWRON_RET_RST	CORE_PWRON_RET_RST	PRCM	Retention reset
EMIF2	EMIF2_PWRON_RET_RST	CORE_PWRON_RET_RST	PRCM	Retention reset

NOTE: The two clocks EOCP_MA_ICLK and EOCP_L3_ICLK are exclusive. EMIF modules are clocked by EOCP_MA_ICLK when MPU is active, otherwise EOCP_L3_ICLK clock is used.

NOTE: EMIFi_FCLK is equal to DDR_PHY_CLK divided by 2. DDR_PHY_CLK is equal to PHY_ROOT_CLK divided by 2.

Table 15-95. Hardware Requests

Interrupt Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
EMIF1	EMIF1_IRQ	MA_IRQ_110	Cortex™-A9 interrupt controller (INTC)	Interrupt to the MPU subsystem
EMIF2	EMIF2_IRQ	MA_IRQ_111	Cortex™-A9 INTC	Interrupt to the MPU subsystem
No DMA Requests				

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NOTE: For the description of the interrupt source, see Section 15.3.4.5, *Interrupt Requests*.

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15.3.4 EMIF Functional Description

15.3.4.1 Block Diagram

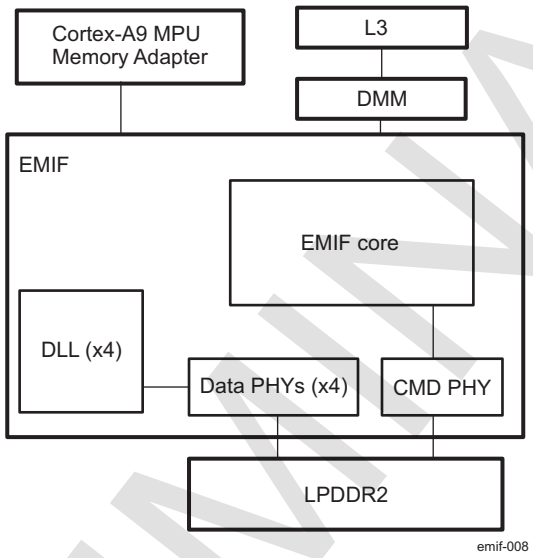
The EMIF is an L3 bus peripheral that provides an interface to the LPDDR2 memories.

Figure 15-48 shows the interconnection between the EMIF module and the other modules.

Digital locked loops (DLLs) are used to delay the input DQS signals during reads so that these strobe signals can be used to latch incoming data on the DQ pins, as required by the LPDDR2 standard.

Physical layers (PHYs) are hard macros that convert single-data rate (SDR) signals to DDR signals.

Figure 15-48. EMIF Block Diagram



15.3.4.1.1 L3 Interface

The EMIF supports three local interfaces: one connects to the system interconnect, one to a low-latency master, and one comes from the MPU half of the EMIF-to-MPU connection. These interfaces are used to request all external memory device accesses, to access the EMIF registers, and to transfer all data to and from the EMIF controller. Table 15-96 shows the MAddrSpace mapping to different CSs. A third interface arranges the connection between the EMIF and the MPU. It is separated to the MPU half of the EMIF-to-MPU L3 Interface and the EMIF half of the EMIF-to-MPU L3 Interface.

Table 15-96. MAddrSpace Mapping to CSs

MAddrSpace	Chip-Select	Description	Exclusions
0x0	lpddr2i_cs[1:0]n (where i = 1 or 2)	SDRAM, which CS connects to an SDRAM or an NVM and is software configurable	
0x1	lpddr2i_cs[1]n (where i = 1 or 2)	LPDDR2-NVM, which CS connects to an SDRAM or an NVM and is software configurable	
0x2	N/A	Reserved	Not visible to the MA port
0x3	N/A	Internal registers	Not visible to the MA port

15.3.4.1.2 FIFO Description

The EMIF module contains the following FIFOs:

- Command FIFO

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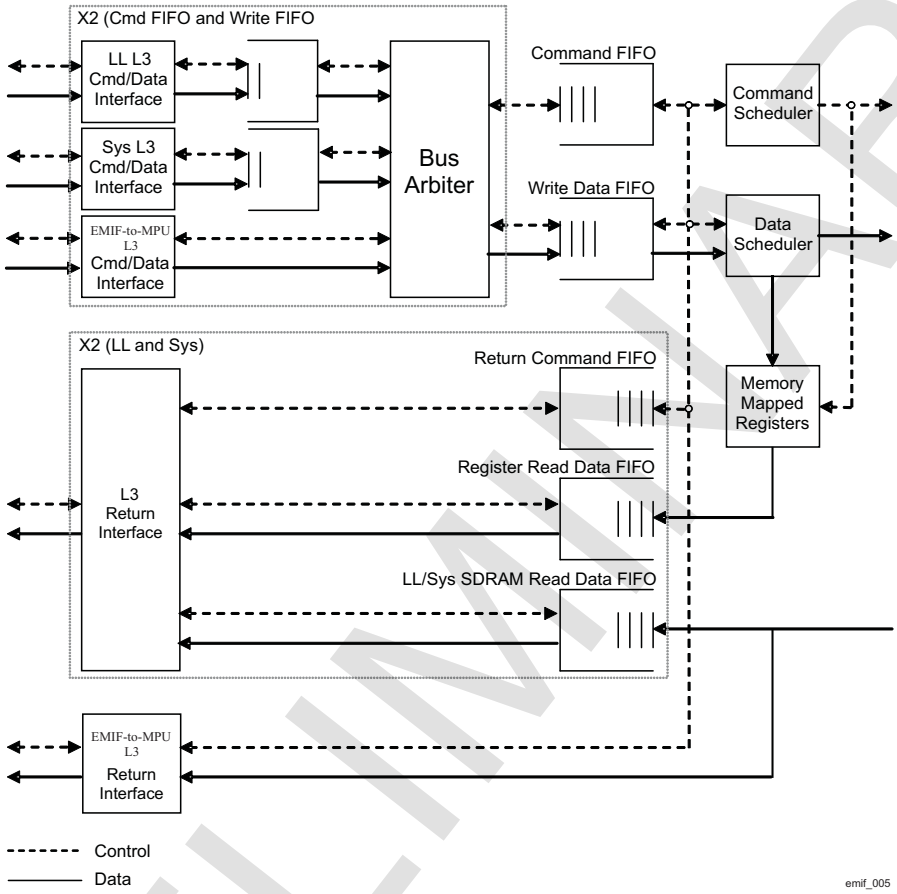
- Write data FIFO
- Return command FIFO
- Two read data FIFOs

Figure 15-49 shows the overall architecture of the EMIF module.

Figure 15-49. FIFO Block Diagram



Because the system (128-bit) L3 interface is the main interface, it has a higher allocation of FIFO slots than the low-latency (64-bit) L3 interface. Table 15-97 lists the allocation of the entries.

Table 15-97. FIFO Allocation

Parameter	System L3 Interface Entries	Low-Latency L3 Interface Entries	MPU Half of the EMIF-to-MPU L3 Interface Entries
Pre Command FIFO	5	5	3
Command FIFO	Programmable (1)	Programmable (1)	Programmable (1)
Pre Write FIFO	8	8	8
Write Data FIFO	Up to 19+8	Up to 19 + 8	Up to 19 + 8
Return Command FIFO	22	17	13
SDRAM Read Data FIFO	22	17	20
Register Read Data FIFO	2	2	0

(1) The total number of entries in the command FIFO is 10.

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The command FIFO is shared between the three L3 interfaces, whereas there are three different FIFOs for every other type, one dedicated to each L3 interface.

The command FIFO stores all the commands coming in on the L3 command interface. The allocation of entries in the command FIFO is programmable per L3 interface using the EMIF_L3_CONFIG[27:24] REG_SYS_THRESH_MAX, EMIF_L3_CONFIG[19:16] REG_LL_THRESH_MAX, and EMIF_L3_CONFIG[23:20] REG_MPU_TRESH_MAX bit fields.

If the addition of the EMIF_L3_CONFIG[27:24] REG_SYS_THRESH_MAX and EMIF_L3_CONFIG[19:16] REG_LL_THRESH_MAX bit fields is greater than the number of entries in the command FIFO, the allocation depends on the traffic on the interfaces. For example, if both fields are programmed to 7, then either of the interfaces can use seven entries in the command FIFO if the other interface is idle. If both interfaces have traffic, then the EMIF starts to gradually allocate entries to both interfaces until it settles down to seven entries for the low-latency interface and three entries for the system interface, because the low-latency interface has higher priority. If the low-latency interface has no traffic, the system interface can use seven entries.

The allocation also depends on the traffic on the interfaces, if the EMIF_L3_CONFIG[27:24] REG_SYS_THRESH_MAX and EMIF_L3_CONFIG[19:16] REG_LL_THRESH_MAX bit fields are programmed to be equal to or greater than the number of entries in the command FIFO. For example, if both fields are programmed to 10, then the low-latency port can use all the entries if there is no traffic on the system interface. However, if there is no traffic on the low-latency interface, the system interface can use all but one entry. This is because the low-latency interface has higher priority than the system interface. The only way for the system interface to use all command FIFO entries is to set the EMIF_L3_CONFIG[19:16] REG_LL_THRESH_MAX bit field to 0. Writing 0 reserves no space for the associated interface. If the value is set to 0 and a request is seen for that interface, the command FIFO assumes a value of 1 for that interface.

The write data FIFO stores the write data for all the write transactions coming in on the L3 write data interface. The write FIFO is shared for all the ports. A similar token mechanism is used to allocate the write FIFO with the following exceptions. All ports are given a minimum of four tokens, which ensures that each has ensured access to three write FIFO locations. Any one port can only use up to 19 of the 25 write FIFO locations. Because there is an 8-word pre-FIFO, each port can have up to 27 backlogged writes.

The return command FIFO stores all the return transactions that are to be issued to the L3 return interface. These include the write status return and the read data return commands.

Two read data FIFOs store the read data to be sent to the L3 return interface. One read data FIFO stores read data from the memory mapped registers. The other read data FIFO stores read data from external memory.

A write command is executed only when four L3 words of the corresponding data is received in the write data FIFO, or when it is the last data, and if there is space in the return command FIFO. The EMIF schedules a read-only if the results can fit into the return command FIFO and the corresponding read data FIFOs.

15.3.4.1.3 MPU Port Restrictions

The EMIF MPU port is defined only to process memory requests. All register accesses are processed through the system or LL ports of the EMIF. The EMIF MPU port does not support 2D or register requests required or provided by the system and LL interfaces. The port priority is as follows:

1. LL port (highest priority)
2. System or MPU, depending on the MPriority field of the MReqInfo bus

The EMIF considers an address that matches and requires coherency if the arriving address rounded down to the nearest 1-K block matches any address in the FIFO rounded down to the nearest 1-K block plus or minus 1-K block. This ensures that any address within a burst will be coherent with any address within any other burst. This ensures that any address within 1024 bytes will be coherent. It is possible to be coherent up to 2048 bytes apart depending on the address. To maintain coherency two rules must be followed:

- Rule A: Any command arriving on any interface (MPU, system, or LL) that matches an address in the cFIFO is executed after the command in the cFIFO.

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- Rule B: Any command arriving within a 10-cycle window of another, from the different interfaces that do not match any address in the cFIFO but may match command addresses arriving on a different interface, can be executed in any order.

15.3.4.1.4 Arbitration

The EMIF looks at all the commands stored in the command FIFO to schedule commands to the external memory. All commands with the same MConnID on a particular L3 interface complete in order. The EMIF does not ensure ordering between commands with different MConnIDs or between commands from two L3 interfaces. For more information about L3 interconnect terms (MConnID, MCMD, MADDR, etc.) see Section 13.2, *L3 Interconnect*.

However, the EMIF does maintain data coherency. Therefore, the EMIF blocks a command, regardless of priority or the L3 interface, if that command is to the same block address (2048 bytes) as an older command that is not complete. Thus, the EMIF may have one pending read or write for each MConnID. Among all pending reads, the EMIF selects all reads that have their corresponding SDRAM banks already open. Similarly, among all pending writes, the EMIF selects all writes that have their corresponding SDRAM banks already open. Accesses to memory mapped registers are treated as accesses that have open banks.

As a result of this reordering, the EMIF may now have several pending reads and writes that have their corresponding banks open. The EMIF then selects the highest priority read from pending reads, and the highest priority write from pending writes. Commands from the low-latency L3 interface have a higher priority over the commands from the system L3 interface. If two or more commands have the highest priority, the EMIF selects the oldest command. As a result, the EMIF may now have the next read and a write command. If the return command FIFO and the read data FIFO have space and the external bus conflict is resolved, the EMIF performs the final read command before the final write command. If the return command FIFO has space but the read data FIFO is full, the EMIF performs the final write command before the final read command. Resolution of external bus conflict means all the SDRAM command-to-command counters are satisfied and the read-to-write or write-to-read turnaround time is met.

The EMIF does not support tag interleaving. In other words, for an L3 interface, the EMIF completes executing an L3 command before it switches to another command. The EMIF can, however, interleave execution between commands from two L3 interfaces.

The data coherency inside the EMIF is ensured only in a single level of L3 infrastructure. For example, if a write from a secondary L3 bus segment is blocked by a bridge element, the read from a tertiary bus can still beat the write to the EMIF. In such a case, to confirm that a write from master A has landed before a read from master B is performed, master A must wait for the write status from the EMIF before indicating to master B that the data is ready to be read. If master A does not use the L3 wait status, it must do the following:

1. Perform the required write.
2. Perform a dummy write to the EMIF_MOD_ID_REV register.
3. Perform a dummy read to the EMIF_MOD_ID_REV register.
4. Indicate to master B that the data is ready to be read after completion of read in Step 3. The completion of read in Step 3 ensures that the previous writes were done.

Apart from reads and writes, the EMIF must also open and close SDRAM banks and maintain the refresh counts for an SDRAM. The priority of SDRAM commands with respect to refresh levels are:

1. SDRAM refresh request when refresh-must level is reached (highest priority)
2. L3 request for a read without a higher priority write
3. SDRAM refresh request when refresh-need level is reached
4. L3 request for a write
5. SDRAM activate commands
6. SDRAM deactivate commands
7. SDRAM deep power-down request
8. SDRAM refresh request when refresh-may level is reached
9. SDRAM self-refresh or SDRAM power-down request (lowest priority)

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While performing the previous scheduling algorithm, the EMIF may encounter two conditions:

- A continuous stream of high-priority commands can block lower priority commands.
- A continuous stream of SDRAM commands to a row in an open bank can block commands to another row in the same bank.

In addition to this scheduling, the highest priority condition is a reset command. If this condition occurs, the EMIF abandons what it is doing and begins its start-up sequence. In this case, commands and data stored in the FIFOs are lost. The EMIF also starts its start-up sequence whenever the EMIF_SDRAM_CONFIG register is written and the EMIF_SDRAM_REF_CTRL[31] REG_INITREF_DIS bit is set to 0. In this case, commands and data stored in the FIFOs are not lost. The EMIF ensures that in-flight read or write transactions to the SDRAM are complete before starting the initialization sequence.

All the accesses to an SDRAM are pipelined to maximize use of the external bus. All of these are done while fulfilling the access timing requirements of an SDRAM.

15.3.4.2 Clock Management

The EMIF can gate EMIF_FCLK. There is an internal mechanism that can stop EMIF_FCLK automatically.

EMIF_FCLK can be stopped only after the SDRAM is put into self-refresh mode and the power-idle protocol on the L3 bus completes.

The EMIF waits for the DLL lock before performing any memory access.

The EMIF_FCLK frequency can be changed only after putting the external SDRAM in self-refresh mode.

EMIFi_FCLK frequency is equal to half of the DDR_PHY_CLK frequency. DDR_PHY_CLK is equal to half of the PHY_ROOT_CLK frequency.

15.3.4.3 Software Reset

The EMIF does not support a software reset.

The EMIF supports global warm reset mode, during which the EMIF keeps the SDRAM content. Upon a request from the PRCM module indicating a need to enter global warm reset mode, the EMIF does the following:

1. Completes the ongoing access and then puts the SDRAM in self-refresh mode
2. Clears all its FIFO contents and deasserts the sys_SCmdAccept and sys_SDataAccept ports

When the global warm reset must terminate:

1. The PRCM block deasserts its request signal to the EMIF.
2. The EMIF exits self-refresh mode when it receives host accesses from the MPU to the external memory.

15.3.4.4 System Power Management

15.3.4.4.1 Read Idle Window

The EMIF_READ_IDLE_CTRL register can force idle time between consecutive reads to allow the DDR PHY to recalibrate the DLL delays during gradual voltage and frequency change.

The EMIF_READ_IDLE_CTRL[8:0] REG_READ_IDLE_INTERVAL bit field determines the maximum interval ((REG_READ_IDLE_INTERVAL + 1) * 64 EMIF_FCLK clock cycles) between read idle detections or force read idle time. A value of 0 disables the read idle function.

The EMIF_READ_IDLE_CTRL[19:16] REG_READ_IDLE_LEN bit field determines the minimum size of idle window for the read idle detection and the force read idle time. The EMIF introduces idle time only if it does not see at least (REG_READ_IDLE_LEN + 1) * 2 number of idle EMIF_FCLK cycles in REG_READ_IDLE_INTERVAL. Any command other than a read command is considered idle for this purpose. Force read idle occurs when the data bus is busy transferring read data and the read idle interval expires without seeing a read idle length pause in the reads.

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15.3.4.4.2 LPDDR2-SDRAM Power-Down Mode

The EMIF supports power-down mode for low power. The EMIF automatically puts the SDRAM into power-down mode after it is idle for EMIF_PWR_MGMT_CTRL[15:12] REG_PD_TIM number of EMIF_FCLK cycles and the EMIF_PWR_MGMT_CTRL[10:8] REG_LP_MODE bit field is set to 0x4. In power-down mode, the EMIF does not stop the clocks to the SDRAM. The EMIF maintains lpddr2i_ckej[1:0] (where i = 1 or 2 and j = 0 or 1) low to maintain the power-down mode.

When the SDRAM is in power-down mode, the EMIF services register accesses normally. The EMIF also services LPDDR2-NVM accesses normally, provided it is not in power-down mode (in the case the SDRAMs are connected to the same EMIF through two different CSs).

If the LPDDR2-SDRAM is in power-down mode and one of the following occurs, the EMIF brings SDRAM out of power-down mode:

1. EMIF_PWR_MGMT_CTRL[10:8] REG_LP_MODE bit field is changed from 0x4 to some other value.
2. An SDRAM access is requested.
3. The refresh-must level is reached.

For LPDDR2-SDRAM, the EMIF module:

1. Drives lpddr2i_ckej[1:0] (where i = 1 or 2 and j = 0 or 1) high
2. Waits for EMIF_SDRAM_TIM_2[30:28] REG_T_XP + 1 cycles
3. Enters its idle mode and can issue any commands

15.3.4.4.3 LPDDR2-SDRAM Deep Power-Down Mode

For ultimate power savings, the EMIF supports deep power-down mode for LPDDR2-SDRAM.

The SDRAM can be forced into deep power-down mode through software by setting the EMIF_PWR_MGMT_CTRL[11] REG_DPD_EN bit to 0x1. In this case the EMIF continues normal operation until all SDRAM access requests are serviced. At this point the EMIF issues a deep power-down command. The EMIF then maintains plpddr2i_ckej[1:0] (where i = 1 or 2 and j = 0 or 1) low to maintain deep power-down mode. In deep power-down mode, the EMIF automatically stops the clocks to the SDRAM.

Setting the EMIF_PWR_MGMT_CTRL[11] REG_DPD_EN bit to 1 overrides the setting of the EMIF_PWR_MGMT_CTRL[10:8] REG_LP_MODE bit field. Therefore, if the SDRAM is in self-refresh or power-down mode, and the EMIF_PWR_MGMT_CTRL[11] REG_DPD_EN bit is set to 1, the EMIF exits those modes and goes into deep power-down mode.

When the SDRAM is in deep power-down mode, the EMIF services register accesses normally. The EMIF also services LPDDR2-NVM accesses normally, provided it is not in power-down mode (in the case of an SDRAM and NVM, memories are connected to the same EMIF through two different CSs).

If the EMIF_PWR_MGMT_CTRL[11] REG_DPD_EN bit is set to 0x0, the EMIF brings the SDRAM out of deep power-down mode.

For LPDDR2-SDRAM, the EMIF controller:

1. Drives lpddr2i_ckej[1:0] (where i = 1 or 2 and j = 0 or 1) high
2. Issues a RESET command to LPDDR2 (MRW)
3. Enters its idle mode and can issue any commands
4. Software must perform initialization, as specified in Section 15.3.4.13, *LPDDR2-SDRAM Initialization*.

15.3.4.4.4 LPDDR2-NVM Power-Down Mode

The EMIF supports power-down mode for LPDDR2-NVM. The EMIF automatically puts the LPDDR2-NVM into power down after the EMIF is idle for EMIF_PWR_MGMT_CTRL[15:12] REG_PD_TIM number of EMIF_FCLK cycles and the EMIF_PWR_MGMT_CTRL[10:8] REG_LP_MODE bit field is set to 0x4. The EMIF maintains lpddr2i_ckej[1:0] (where i = 1 or 2 and j = 0 or 1) low to maintain the power-down mode.

When LPDDR2-NVM is in power-down mode, the EMIF services register accesses normally. The EMIF also services SDRAM accesses normally, provided it is not in self-refresh or power-down mode (in the case of NVMs, memories are connected to the same EMIF through two different CSs).

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When the LPDDR2-NVM is in power-down mode and the EMIF_PWR_MGMT_CTRL[10:8] REG_LP_MODE bit field is changed from 0x4 to some other value, or an LPDDR2-NVM access is requested, the EMIF brings the LPDDR2-NVM out of power-down mode.

For LPDDR2-NVM, the EMIF module:

1. Drives lpddr2i_ckej[1:0] (where i = 1 or 2 and j = 0 or 1) high
2. Waits for EMIF_SDRAM_TIM_2[30:28] REG_T_XP + 1 cycles
3. Enters its idle mode and can issue any commands

15.3.4.4.5 LPDDR2-SDRAM Self-Refresh Mode

The EMIF supports self-refresh mode for low power. The EMIF automatically puts the SDRAM into self-refresh mode after the EMIF is idle for EMIF_PWR_MGMT_CTRL[3:0] REG_CS_TIM number of EMIF_FCLK cycles and the EMIF_PWR_MGMT_CTRL[10:8] REG_LP_MODE bit field is set to 0x2. In self-refresh mode, the EMIF automatically stops the clocks to the SDRAM. The EMIF maintains lpddr2i_ckej[1:0] (where i = 1 or 2 and j = 0 or 1) low to maintain self-refresh mode.

When the SDRAM is in self-refresh mode, the EMIF services register accesses normally. The EMIF also services LPDDR2-NVM accesses normally, provided it is not in power-down mode (in the case of an SDRAM and NVM, memories are connected to the same EMIF through two different CSs).

If the LPDDR2-SDRAM is in self-refresh mode and one of the following occurs, the EMIF brings SDRAM out of self-refresh mode:

1. The EMIF_PWR_MGMT_CTRL[10:8] REG_LP_MODE bit field is changed from 0x2 to some other value.
2. An SDRAM access is requested.
3. EMIF_SDRAM_TIM_2[2:0] REG_T_CKE + 1 cycles have elapsed since the SELF-REFRESH command was issued.

For LPDDR2-SDRAM, the EMIF:

1. Enables clocks
2. Drives lpddr2i_ckej[1:0] (i = 1 or 2 and j = 0 or 1) high
3. Waits for EMIF_SDRAM_TIM_2[24:16] REG_T_XSNR + 1 cycles
4. Starts an auto-refresh cycle in the next cycle
5. Enters its idle mode and can issue any commands

15.3.4.4.6 Save and Restore

The EMIF supports the save-and-restore mechanism to switch off power to the EMIF.

For more information about the off-mode sequence and restoration of power to the EMIF sequence, see Chapter 3, *Power, Reset, and Clock Management*.

15.3.4.4.7 Retention Mode

EMIF supports full-retention mode.

15.3.4.5 Interrupt Requests

The EMIF sources two interrupts: one for the system L3 interface and the other for the low-latency L3 interface. The pulse and level interrupt signals for a particular interface are sourced from the same raw interrupt internal to the module.

The EMIF sets the EMIF_IRQSTATUS_RAW_SYS[0] REG_RAW_SYS/EMIF_IRQSTATUS_RAW_LL[0] REG_RAW_LL bit (depending on which interface sent the command having an error) to 1, if an access request to an unsupported MAddrSpace is received. If such an error occurs, it is due to bad programming of the DMM. For more information about addressing, see Section 15.2, *Dynamic Memory Manager*.

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The interrupts can be cleared by writing 1 to the corresponding bits in the EMIF_IRQSTATUS_RAW_SYS/EMIF_IRQSTATUS_RAW_LL or the EMIF_IRQSTATUS_SYS/EMIF_IRQSTATUS_LL registers.

Table 15-98 lists the event flags and their mask that can cause module interrupts.

Table 15-98. Events

Event Flag	Event Mask	Description
EMIF_IRQSTATUS_RAW_SYS[1] REG_TA_SYS / EMIF_IRQSTATUS_SYS[1] REG_TA_SYS	EMIF_IRQENABLE_SET_SYS[1] REG_EN_TA_SYS / EMIF_IRQENABLE_CLR_SYS[1] REG_EN_TA_SYS	System L3 interrupt for SDRAM temperature alert
EMIF_IRQSTATUS_RAW_LL[1] REG_TA_LL / EMIF_IRQSTATUS_LL[1] REG_TA_LL	EMIF_IRQENABLE_SET_LL[1] REG_EN_TA_LL / EMIF_IRQENABLE_CLR_LL[1] REG_EN_TA_LL	Low-latency L3 interrupt for SDRAM temperature alert
EMIF_IRQSTATUS_RAW_SYS[0] REG_ERR_SYS / EMIF_IRQSTATUS_SYS[0] REG_ERR_SYS	EMIF_IRQENABLE_SET_SYS[0] REG_EN_ERR_SYS / EMIF_IRQENABLE_CLR_SYS[0] REG_EN_ERR_SYS	System L3 interrupt for command or address error
EMIF_IRQSTATUS_RAW_LL[0] REG_ERR_LL / EMIF_IRQSTATUS_LL[0] REG_ERR_LL	EMIF_IRQENABLE_SET_LL[0] REG_EN_ERR_LL / EMIF_IRQENABLE_CLR_LL[0] REG_EN_ERR_LL	Low-latency L3 interrupt for command or address error

15.3.4.6 SDRAM Output Impedance Calibration

The EMIF supports automatic output impedance calibration. The ZQ calibration can be enabled per CS by setting the EMIF_ZQ_CONFIG[31] REG_ZQ_CS1EN and EMIF_ZQ_CONFIG[30] REG_ZQ_CS0EN bits. The EMIF supports three types of ZQ calibration commands:

- ZQINIT: ZQ calibration command during initialization
- ZQCS: ZQ calibration short command
- ZQCL: ZQ calibration long command

The EMIF issues a ZQCS command each time the EMIF_ZQ_CONFIG[15:0] REG_ZQ_REFINTERVAL bit field expires. In other words, the REG_ZQ_REFINTERVAL defines the interval between ZQCS commands. When a ZQCS command is issued, the EMIF waits and blocks any other command for (EMIF_SDRAM_TIM_3[20:15] REG_ZQ_ZQCS + 1) number of DDR clock cycles.

If the EMIF_ZQ_CONFIG[28] REG_ZQ_SFEXITEN bit field is set to 1, the EMIF issues a ZQCL command every time it exits self-refresh, active power-down, and precharge power-down modes. When a ZQCL command is issued, the EMIF waits and blocks any other command for (EMIF_ZQ_CONFIG[17:16] REG_ZQ_ZQCL_MULT + 1) × (EMIF_SDRAM_TIM_3[20:15] REG_ZQ_ZQCS + 1) number of DDR clock cycles.

If a separate calibration resistor is used per device, the ZQ calibration can be performed simultaneously over both CSs. To enable ZQ calibration to be performed simultaneously over both CSs, the EMIF_ZQ_CONFIG[27] REG_ZQ_DUALCALEN bit must be set to 1. If REG_ZQ_DUALCALEN is set to 0, the EMIF performs ZQ calibration per CS serially.

15.3.4.7 SDRAM Temperature Monitoring

The EMIF supports automatic temperature monitoring to facilitate the software update of the refresh rate according to the temperature changes of the LPDDR2. Temperature monitoring can be enabled per CS by setting the EMIF_TEMP_ALERT_CONFIG[31] REG_TA_CS1EN and EMIF_TEMP_ALERT_CONFIG[30] REG_TA_CS0EN bits.

The EMIF polls the temperature of the LPDDR2 (issues an MRR command to Mode Register 4) every time the EMIF_TEMP_ALERT_CONFIG[21:0] REG_TA_REFINTERVAL bit field expires. In other words, REG_TA_REFINTERVAL defines the interval between temperature alert polls. If the EMIF sees a 1 on bit 7 of the read data value from the MRR, which indicates the temperature has changed, the

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EMIF_IRQSTATUS_SYS[1] REG_TA_SYS bit (for L3 interconnect) or EMIF_IRQSTATUS_LL[1] REG_TA_LL bit (for low-latency L3) connected LPDDR2-NVM is set and the module sends an interrupt on the system and low-latency interrupt lines, respectively. When the interrupt is received, software updates the EMIF_SDRAM_REF_CTRL[15:0] REG_REFRESH_RATE bit field to the required value as per the temperature change.

If the EMIF_TEMP_ALERT_CONFIG[28] REG_TA_SFEXITEN bit is set to 1, the EMIF polls for temperature change every time it exits self-refresh, active power-down, and precharge power-down modes.

Because the EMIF is performing an MRR, it needs information about how the LPDDR2 is connected. The EMIF_TEMP_ALERT_CONFIG[27:26] REG_TA_DEVWDT and EMIF_TEMP_ALERT_CONFIG[25:24] REG_TA_DEVCNT bit fields provide the necessary information to the EMIF for MRR data compare. For example, if REG_TA_DEVWDT is set to 0, which indicates 8-bit devices are used, and if REG_TA_DEVCNT is set to 2, which indicates four devices are used to form a 32-bit bus, the mask used for checking is 4'b1111; that is, the EMIF expects data on each byte lane on a 32-bit bus.

15.3.4.8 SDRAM Refresh Scheduling

The EMIF uses two counters to schedule AUTO REFRESH commands: a 13-bit decrementing refresh interval counter and a 4-bit refresh backlog counter. The interval counter is used to define the rate at which connected SDRAM devices are refreshed. It is loaded with the value of the EMIF_SDRAM_REF_CTRL[15:0] REG_REFRESH_RATE bit field at reset (only the 13 LSBs are taken). The interval counter decrements by 1 each cycle until it reaches 0, at which point it reloads from the EMIF_SDRAM_REF_CTRL[15:0] REG_REFRESH_RATE bit field and restarts decrementing. The counter also reloads and restarts decrementing whenever the EMIF_SDRAM_REF_CTRL[15:0] REG_REFRESH_RATE bit field is updated.

The refresh backlog counter records the number of outstanding AUTO REFRESH commands the EMIF has. The backlog counter increments by 1 each time the interval counter reloads (unless it has reached its maximum value of 15). The backlog counter decrements by 1 each time the EMIF issues an AUTO REFRESH command (unless it is already 0). For the range of values that the backlog counter can take, there are four levels of urgency with which the EMIF must perform an auto refresh cycle (in which it issues AUTO REFRESH commands):

1. Refresh-may level is reached when the backlog count is greater than 0, which indicates there is a refresh backlog; therefore, if the EMIF is not busy and none of the SDRAM banks are open, the EMIF must perform an auto refresh cycle.
2. Refresh-release level is reached when the backlog count is greater than 4, which indicates the refresh backlog is getting bigger; therefore, if the EMIF is not busy it must perform an auto refresh cycle even if any of the banks are open.
3. Refresh-need level is reached when the backlog count is greater than 5, which indicates the refresh backlog is getting bigger and the EMIF must raise the priority of performing an auto refresh cycle above that of servicing new memory write requests. The EMIF starts servicing new memory accesses after the refresh-release level is cleared.
4. Refresh-must level is reached when the backlog count is greater than 7, which indicates the refresh backlog is becoming excessive and the EMIF must perform an auto refresh cycle before servicing any new memory access requests. The EMIF starts servicing new memory accesses after the refresh-release level is cleared.

The refresh counters do not operate when SDRAM is in self-refresh mode.

The EMIF issues AUTO REFRESH commands within auto refresh cycles. An auto refresh cycle consists of issuing an AUTO REFRESH command and waiting T_RFC (see EMIF_SDRAM_TIM_3) cycles before rechecking the refresh levels. If the refresh-release level is not reached, the EMIF starts another auto refresh cycle; otherwise, it returns to idle mode where it can issue any command.The EMIF ensures that no more than eight AUTO REFRESH commands are issued in any rolling tREFBW (= 4 * 8 * tRFC) window.

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15.3.4.8.1 Performance Counters Description

The EMIF_PERF_CNT_1 and EMIF_PERF_CNT_2 registers can be used to monitor or calculate the EMIF bandwidth and efficiency. These counters can count events such as total SDRAM accesses, SDRAM activates, reads, writes, etc. Each counter counts events independent of the other counters. In addition to the ability to count events, the counters can also filter the events from a particular master or address space. The events to be counted and the filter enabling can be configured using the EMIF_PERF_CNT_CFG register. The filter value to be used can be configured using the EMIF_PERF_CNT_SEL register. Each counter can be configured independently.

Table 15-178 lists all the events that can be counted and whether a filter can be applied to a particular event. A filter can be applied to an event if the following bits for Performance Counter 1 and Performance Counter 2 can be set equal to 0x1 for that event:

- Performance Counter 1: EMIF_PERF_CNT_CFG[15] REG_CNTR1_MCONNID_EN and EMIF_PERF_CNT_CFG[14] REG_CNTR1_REGION_EN
- Performance Counter 2: EMIF_PERF_CNT_CFG[31] REG_CNTR2_MCONNID_EN and EMIF_PERF_CNT_CFG[30] REG_CNTR2_REGION_EN

15.3.4.8.2 Performance Counters General Examples

15.3.4.8.2.1 PERF_CNT_1 General Example for Counting Write Accesses

The Performance Counter 1 register must count all write accesses from the dual Cortex-M3 MPU subsystem:

- To enable counting writes, the EMIF_PERF_CNT_CFG[3:0] REG_CNTR1_CFG bit field must be set to 0x3.
- The EMIF_PERF_CNT_SEL[15:8] REG_MCONNID1 bit field must be set to 0x44. The values programmed into the REG_MCONNIDx bit fields are those in Table 28-20, in Chapter 28, *On-Chip Debug Support*, left-shifted by 2 bits.
- To enable filtering, the EMIF_PERF_CNT_CFG[15] REG_CNTR1_MCONNID_EN bit must be set to 0x1.

With this configuration, Counter 1 counts every write made to the EMIF from master 0x44 to any address space. This does not include accesses from other masters and does not include commands other than writes.

15.3.4.8.2.2 PERF_CNT_2 General Example for Counting Total Access

The Performance Counter 2 register must count total accesses to SDRAM regardless of the masters or address space.

- To enable counting all SDRAM accesses, the EMIF_PERF_CNT_CFG[19:16] REG_CNTR2_CFG bit field must be set to 0x0.
- To disable filtering, the EMIF_PERF_CNT_CFG[31] REG_CNTR2_MCONNID_EN and the EMIF_PERF_CNT_CFG[30] REG_CNTR2_REGION_EN bits must be set to 0x0.

With this configuration, Counter 2 counts every access made to the EMIF. This includes all accesses from all masters and to any address space.

15.3.4.8.2.3 PERF_CNT_3 General Example for Counting all Read Accesses

The Performance Counter 1 register must count all read accesses from the dual Cortex-M3 MPU subsystem to address space 0x0.

- To enable counting reads, the EMIF_PERF_CNT_CFG[3:0] REG_CNTR1_CFG bit field must be set to 0x2.
- The EMIF_PERF_CNT_SEL[15:8] REG_MCONNID1 and EMIF_PERF_CNT_SEL[1:0] REG_REGION_SEL1 bit fields must be set to 0x44 and 0x0, respectively.
- To enable filtering, the EMIF_PERF_CNT_CFG[15] REG_CNTR1_MCONNID_EN and EMIF_PERF_CNT_CFG[14] REG_CNTR1_REGION_EN bits must be set to 0x1.

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With this configuration, Counter 1 counts every read made to the EMIF from master 0x44 to address space 0x0. This does not include accesses from other masters or accesses to other address space and does not include commands other than reads.

15.3.4.9 EMIF Access Cycles

By default, the EMIF keeps the SDRAM CSs active. To direct a command to one of the SDRAMs, the EMIF deasserts the CS to the other SDRAMs for the duration of the command. If the EMIF_SDRAM_CONFIG[3] REG_EBANK bit in the SDRAM configuration register is set to 0, CS1 is always driven high except during initialization and for REFRESH, POWER DOWN, SELF-REFRESH, and DEEP POWER-DOWN commands.

The EMIF always performs burst accesses to the SDRAM. Multiple SDRAM bursts may be needed to service a single L3 burst request. Table 15-99 through Table 15-103 show a few examples of how EMIF accesses SDRAM for a linear incrementing transaction type. T0, T1, etc. are clock cycles. R0 is read starting at column 0, R8 is read starting at column 8, and R16 is read starting at column 16. D0-1 is the data from column 0 and 1, D2-3 is the data from column 2 and 3, and so on.

Table 15-99. 64-Byte Linear Read Starting at Address 0x0

T0	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11
R0				R8							
				D0-1	D2-3	D4-5	D6-7	D8-9	D10-11	D12-13	D14-15

Table 15-100. 64-Byte Linear Read Starting at Address 0x8 (LPDDR2-S2)

T0	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13	T14
R2			R8				R16							
				D2-3	D4-5	D6-7	D8-9	D10-11	D12-13	D14-15	D16-17	Unused	Unused	Unused

Table 15-101. 64-Byte Linear Read Starting at Address 0x8 (LPDDR2-S4)

T0	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13	T14	T15
R2				R8				R16							
				D2-3	D4-5	D6-7	Unused	D8-9	D10-11	D12-13	D14-15	D16-17	Unused	Unused	Unused

Table 15-102. 64-Byte Linear Read Starting at Address 0x10

T0	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13
R4		R8				R16							
				D4-5	D6-7	D8-9	D10-11	D12-13	D14-15	D16-17	D18-19	Unused	Unused

Table 15-103. 64-Byte Linear Read Starting at Address 0x18

T0	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13
R6		R8				R16							
				D6-7	Unused	D8-9	D10-11	D12-13	D14-15	D16-17	D18-19	D20-21	Unused

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The EMIF uses the unused data phases in the preceding figures by issuing successive read commands if there are reads to open banks pending in the command FIFO.

The write data conversion from SDR to DDR is done outside the EMIF.

15.3.4.9.1 SDRAM Read

A read access to an SDRAM is initiated with a READ command. The EMIF provides the internal bank address and the column address on pad_ca_o with the READ command. The EMIF registers the first read data from lpddr2i_dj (where i = 1 or 2 and j = 0 or 1) after (read_latency + 3) DDR clock cycles. Read latency is programmed in the EMIF_DDR_PHY_CTRL_1 register.

15.3.4.9.2 SDRAM Write

A write access to an SDRAM is initiated with a WRITE command. The EMIF provides the internal bank address and the column address on pad_ca_o with the WRITE command.

The EMIF delays the write data by the appropriate write latency minus 1. Subsequent data words are provided on lpddr2i_dj (where i = 1 or 2 and j = 0 or 1) along with the appropriate data mask on lpddr2i_dmj (where i = 1 or 2 and j = 0 or 1) on each successive clock cycle. The DDR PHY then adds one more clock cycle delay to the write data to appropriately center the write data to the outgoing DQS.

15.3.4.10 Turnaround Time

Table 15-104 lists the turnaround time the EMIF introduces on the data bus for various back-to-back accesses. The EMIF takes advantage of the CAS latencies and packs the commands as close as possible on the control bus to introduce the following turnaround time on the data bus.

Table 15-104. Turnaround Time

Previous Access	Next Access	Turnaround Time (Number of DDR Clock Cycles)
SDRAM read	SDRAM read to the same CS	0
SDRAM read	SDRAM read to a different CS	2
SDRAM read	SDRAM write	2
SDRAM write	SDRAM write	0
SDRAM write	SDRAM read	2

15.3.4.11 SDRAM Address Mapping

The EMIF interleaves the internal banks for SDRAM connected to both CSs (see Table 15-105 for the SDRAM addressing space), according to the DMM (for more information, see Section 15.2, *Dynamic Memory Manager*). From the system point of view, the external SDRAM is seen as one block of SDRAM. If two external 64-MB devices are used, a 128-MB memory block is observed. If two external 32-MB devices are used, a 64-MB block is observed.

Table 15-105. SDRAM Addressing Space

Module Name	Base Address	Size
EMIF1 | EMIF2-CS0-SDRAM[1]	0x8000 0000	0 to 1GB, programmable in DMM (see Section 15.2, *Dynamic Memory Manager*)

[1] The addressing space is interleaved on two LPDDR memory controllers (EMIF1, EMIF2), each activating their CS0 line. These CSs can address 64, 128, 256, 512, 1024, or 2048MBs. Interleaving occurs at 128-byte granularity. Both memories must be of the same kind (SDRAM or NVM). EMIF1-CS0 base address is always 0x8000 0000 at reset, and occupies a 1-GB address space at reset (interleaving disabled at reset).

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Table 15-105. SDRAM Addressing Space (continued)

Module Name	Base Address	Size
EMIF1| EMIF2-CS1-SDRAM[2]	0xC000 0000	0 to 1GB, programmable in DMM (see Section 15.2, *Dynamic Memory Manager*)

[2] The addressing space is interleaved on two LPDDR memory controllers (EMIF1, EMIF2), each activating its CS1 line. These CSs are programmable to 64, 128, 256, 512, or 1024MBs. Interleaving occurs at 128-byte granularity. EMIF1-CS1 and EMIF2-CS1 are disabled at reset. Their base address is programmable to achieve a continuous address space with the respective CS0, regardless of the programmed address range. EMIF1-CS1 is disabled if the EMIF1-CS0 memory density is set to 2048MB (2GB) when interleaving is disabled, or if the EMIF1-CS0 + EMIF2-CS0 memory density is set to 1024MB (1GB) when interleaving is enabled.

When addressing SDRAM, if the EMIF_SDRAM_CONFIG[28:27] REG_IBANK_POS bit field is set to 0, the EMIF uses the following three bit fields to determine the mapping from the source address to the SDRAM row, column, bank, and CS:

- EMIF_SDRAM_CONFIG[6:4] REG_IBANK
- EMIF_SDRAM_CONFIG[3] REG_EBANK
- EMIF_SDRAM_CONFIG[2:0] REG_PAGESIZE

If the EMIF_SDRAM_CONFIG[28:27] REG_IBANK_POS bit field is set to 1, 2, or 3, the EMIF uses the folloiwing four bit fields to determine the mapping from the source address to the SDRAM row, column, bank, and CS:

- EMIF_SDRAM_CONFIG[6:4] REG_IBANK
- EMIF_SDRAM_CONFIG[3] REG_EBANK
- EMIF_SDRAM_CONFIG[2:0] REG_PAGESIZE
- EMIF_SDRAM_CONFIG[9:7] REG_ROWSIZE

In all cases the EMIF considers its SDRAM address space to be a single logical block, regardless of the number of physical devices or whether the devices are mapped across one or two EMIF CSs.

For EMIF_SDRAM_CONFIG[28:27] REG_IBANK_POS = 0, Table 15-106 and Table 15-107 list which source address bits (MAddr) map to the SDRAM row, column, bank, and CS bits for all combinations of REG_IBANK, REG_EBANK, and REG_PAGESIZE.

For EMIF_SDRAM_CONFIG[28:27] REG_IBANK_POS != 0, Table 15-109 and Table 15-110 show which source address bits (MAddr) map to the SDRAM row, column, bank, and CS bits for all combinations of REG_IBANK, REG_EBANK, REG_PAGESIZE, and REG_ROWSIZE.

The tables also list the maximum size of the resulting SDRAM space.

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Table 15-106. L3 Address to SDRAM Address Mapping for 16-Bit SDRAM (EMIF_SDRAM_CONFIG[28:27] REG_IBANK_POS = 0)

Reach (MBytes)	EMIF_SDRAM_CONFIG [3] REG_EBANK	EMIF_SDRAM_CONFIG [6:4] REG_IBANK	EMIF_SDRAM_CONFIG [2:0] REG_PAGESIZE	MAddr															
				31	30	29	28	27	26	25	[24:16]	15	14	13	12	11	10	9	[8:1]
32	0	0	0	–							Row								Col
64	1	0	0	–							Row							CS	Col
64	0	1	0	–							Row							Bank	Col
128	1	1	0	–						Row							CS	Bank	Col
128	0	2	0	–						Row							Bank		Col
256	1	2	0	–					Row							CS	Bank		Col
256	0	3	0	–					Row							Bank			Col
512	1	3	0	–				Row							CS	Bank			Col
64	0	0	1	–							Row							Col	
128	1	0	1	–						Row							CS	Col	
128	0	1	1	–						Row							Bank	Col	
256	1	1	1	–					Row							CS	Bank	Col	
256	0	2	1	–					Row							Bank		Col	
512	1	2	1	–				Row							CS	Bank		Col	
512	0	3	1	–				Row							Bank			Col	
1024	1	3	1	–			Row							CS	Bank			Col	
128	0	0	2	–						Row								Col	
256	1	0	2	–					Row							CS		Col	
256	0	1	2	–					Row							Bank		Col	
512	1	1	2	–				Row							CS	Bank		Col	
512	0	2	2	–				Row							Bank			Col	
1024	1	2	2	–			Row							CS	Bank			Col	
1024	0	3	2	–			Row							Bank				Col	
2048	1	3	2	–		Row							CS	Bank				Col	
256	0	0	3	–					Row							Col			
512	1	0	3	–				Row							CS	Col			
512	0	1	3	–				Row							Bank	Col			

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Table 15-106. L3 Address to SDRAM Address Mapping for 16-Bit SDRAM (EMIF_SDRAM_CONFIG[28:27] REG_IBANK_POS = 0) (continued)

Reach (MBytes)	EMIF_SDRAM_CONFIG [3] REG_EBANK	EMIF_SDRAM_CONFIG [6:4] REG_IBANK	EMIF_SDRAM_CONFIG [2:0] REG_PAGESIZE	MAddr															
				31	30	29	28	27	26	25	[24:16]	15	14	13	12	11	10	9	[8:1]
1024	1	1	3	–		Row								CS	Bank	Col			
1024	0	2	3	–		Row								Bank		Col			
2048	1	2	3	–	Row								CS	Bank		Col			
2048	0	3	3	–	Row								Bank			Col			

Table 15-107. L3 Address to SDRAM Address Mapping for 32-Bit SDRAM (EMIF_SDRAM_CONFIG[28:27] REG_IBANK_POS = 0)

Reach (Mbytes)	EMIF_SDRAM_CONFIG[3] REG_EBANK	EMIF_SDRAM_CONFIG[6:4] REG_IBANK	EMIF_SDRAM_CONFIG[2:0] REG_PAGESIZE	MAddr														
				31	30	29	28	27	26	25:17	16	15	14	13	12	11	10	9:2
64	0	0	0	-						row								col
128	1	0	0	-						row							cs	col
128	0	1	0	-						row							bank	col
256	1	1	0	-						row						cs	bank	col
256	0	2	0	-						row						bank		col
512	1	2	0	-						row					cs	bank		col
512	0	3	0	-						row					bank			col
1024	1	3	0	-						row				cs	bank			col
128	0	0	1	-						row							col	
256	1	0	1	-						row						cs	col	
256	0	1	1	-						row						bank	col	
512	1	1	1	-						row					cs	bank	col	
512	0	2	1	-						row					bank		col	
1024	1	2	1	-						row				cs	bank		col	
1024	0	3	1	-						row				bank			col	

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Table 15-107. L3 Address to SDRAM Address Mapping for 32-Bit SDRAM (EMIF_SDRAM_CONFIG[28:27] REG_IBANK_POS = 0) (continued)

Reach (Mbytes)	EMIF_SDRAM_CONFIG[3] REG_EBANK	EMIF_SDRAM_CONFIG[6:4] REG_IBANK	EMIF_SDRAM_CONFIG[2:0] REG_PAGESIZE	MAddr														
				31	30	29	28	27	26	25:17	16	15	14	13	12	11	10	9:2
2048	1	3	1	-	row								cs	bank			col	
256	0	0	2	-					row							col		
512	1	0	2	-				row							cs	col		
512	0	1	2	-				row							bank	col		
1024	1	1	2	-			row							cs	bank	col		
1024	0	2	2	-			row							bank		col		
2048	1	2	2	-	row								cs	bank		col		
2048	0	3	2	-	row								bank			col		
4096	1	3	2	row								cs	bank			col		
512	0	0	3	-				row							col			
1024	1	0	3	-			row							cs	col			
1024	0	1	3	-			row							bank	col			
2048	1	1	3	-	row								cs	bank	col			
2048	0	2	3	-	row								bank		col			
4096	1	2	3	row								cs	bank		col			
4096	0	3	3	row								bank			col			

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For EMIF_SDRAM_CONFIG[28:27] REG_IBANK_POS = 0, the effect of the address-mapping scheme is that as the source address increments across SDRAM page boundaries, the EMIF moves onto the same page in the next bank in the current device (lpddr2i_cs1[0]n, where i = 1 or 2). This movement along the banks of the current device continues until the page is accessed in all banks in the current device. The EMIF then proceeds to the same page in the next device (if EMIF_SDRAM_CONFIG[3] REG_EBANK = 1, lpddr2i_cs1[1]n, where i = 1 or 2) and proceeds through the same page in all its banks before moving to the next page in the first device (lpddr2i_cs1[0]n, where i = 1 or 2). The EMIF exploits this movement across internal banks and CSs while remaining on the same page to maximize the number of open SDRAM banks within the overall SDRAM space.

Thus, the EMIF can keep a maximum of 16 banks (eight internal banks across two CSs) open at a time, and can interleave among all of them.

Table 15-108 through Table 15-110 list the L3 address to SDRAM address mapping. In each case, there are x bits for bank, followed by y bits for row, followed by z bits for CS, followed by s bits for bank, and t bits for col in MAddr[31:N] (x, y, z, s, and t are given depending on the value of the EMIF_SDRAM_CONFIG bit field).

Table 15-108. L3 Address to SDRAM Address Mapping for EMIF_SDRAM_CONFIG[28:27] REG_IBANK_POS = 1 and EMIF_SDRAM_CONFIG_2[27] REG_EBANK_POS = 0

MAddr[31:N]				
Bank Address	**Row Address**	**Chip-Select**	**Bank Address**	**Column Address**
Number of bits defined by EMIF_SDRAM_CONFIG [6] REG_IBANK	**Number of bits defined by EMIF_SDRAM_CONFIG [9:7] REG_ROWSIZE**	**Number of bits defined by EMIF_SDRAM_CONFIG [3] REG_EBANK**	**Number of bits defined by EMIF_SDRAM_CONFIG [5:3] REG_IBANK**	**Number of bits defined by EMIF_SDRAM_CONFIG [2:0] REG_PAGESIZE**
= 0: 0 bit	= 0: 9 bits	= 0: 0 bit	= 0: 0 bit	= 0: 8 bits
= 1: 0 bit	= 1: 10 bits	= 1: 1 bit	= 1: 1 bit	= 1: 9 bits
	= 2: 11 bits		= 2: 2 bits	= 2: 10 bits
	= 3: 12 bits		= 3: 2 bits	= 3: 11 bits
	= 4: 13 bits			
	= 5: 14 bits			
	= 6: 15 bits			
	= 7: 16 bits			

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NOTE: N = 1 for 16-bit SDRAM, and N = 2 for 32-bit SDRAM.

The REG_IBANK bit field is listed twice because it gives the number of bank bits depending on their place in the MAddr.

For EMIF_SDRAM_CONFIG[28:27] REG_IBANK_POS = 1, the EMIF interleaves banks the same as for EMIF_SDRAM_CONFIG[28:27] REG_IBANK_POS = 0, but the interleaving of banks within a device (per CS) is limited to four banks. Thus, the EMIF can keep a maximum of 16 banks (eight internal banks across two CSs) open at a time, but can interleave among only 8 of them.

Table 15-109. L3 Address to SDRAM Address Mapping for EMIF_SDRAM_CONFIG[28:27] REG_IBANK_POS = 2 and EMIF_SDRAM_CONFIG_2[27] REG_EBANK_POS = 0

MAddr[31:N]				
Bank Address	**Row Address**	**Chip-Select**	**Bank Address**	**Column Address**
Number of bits defined by EMIF_SDRAM_CONFIG [6:5] REG_IBANK	**Number of bits defined by EMIF_SDRAM_CONFIG [9:7] REG_ROWSIZE**	**Number of bits defined by EMIF_SDRAM_CONFIG [3] REG_EBANK**	**Number of bits defined by EMIF_SDRAM_CONFIG [4] REG_IBANK**	**Number of bits defined by EMIF_SDRAM_CONFIG [2:0] REG_PAGESIZE**
= 0: 0 bit	= 0: 9 bits	= 0: 0 bit	= 0: 0 bit	= 0: 8 bits
= 1: 0 bit	= 1: 10 bits	= 1: 1 bit	= 1: 1 bit	= 1: 9 bits
= 2: 1 bit	= 2: 11 bits			= 2: 10 bits
= 3: 2 bits	= 3: 12 bits			= 3: 11 bits
	= 4: 13 bits			
	= 5: 14 bits			
	= 6: 15 bits			
	= 7: 16 bits			

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NOTE: N = 1 for 16-bit SDRAM, and N = 2 for 32-bit SDRAM.

For EMIF_SDRAM_CONFIG[28:27] REG_IBANK_POS = 2, the EMIF interleaves banks the same as for EMIF_SDRAM_CONFIG[28:27] REG_IBANK_POS = 0, but the interleaving of banks within a device (per CS) is limited to two banks. Thus, the EMIF can keep a maximum of 16 banks (eight internal banks across two CSs) open at a time, but can interleave among only 4 of them.

Table 15-110. L3 Address to SDRAM Address Mapping for EMIF_SDRAM_CONFIG[28:27] REG_IBANK_POS = 3 and EMIF_SDRAM_CONFIG_2[27] REG_EBANK_POS = 0

MAddr[31:N]			
Bank Address	**Row Address**	**Chip-Select**	**Column Address**
Number of bits defined by EMIF_SDRAM_CONFIG[6:4] REG_IBANK	**Number of bits defined by EMIF_SDRAM_CONFIG[9:7] REG_ROWSIZE**	**Number of bits defined by EMIF_SDRAM_CONFIG[3] REG_EBANK**	**Number of bits defined by EMIF_SDRAM_CONFIG[2:0] REG_PAGESIZE**
= 0: 0 bit	= 0: 9 bits	= 0: 0 bit	= 0: 8 bits
= 1: 1 bit	= 1: 10 bits	= 1: 1 bit	= 1: 9 bits
= 2: 2 bits	= 2: 11 bits		= 2: 10 bits
= 3: 3 bits	= 3: 12 bits		= 3: 11 bits
	= 4: 13 bits		
	= 5: 14 bits		
	= 6: 15 bits		
	= 7: 16 bits		

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NOTE: N = 1 for 16-bit SDRAM, and N = 2 for 32-bit SDRAM.

For EMIF_SDRAM_CONFIG[28:27] REG_IBANK_POS = 3, the EMIF cannot interleave banks within a device (per CS). However, it can interleave banks between the two CSs. Thus, the EMIF can keep a maximum of 16 banks (eight internal banks across two CSs) open at a time, but can interleave among only 2 of them.

Because the EMIF interleave among a fewer number of banks when EMIF_SDRAM_CONFIG[28:27] REG_IBANK_POS != 0, these cases are lower in performance than the EMIF_SDRAM_CONFIG[28:27] REG_IBANK_POS = 0 case. Thus, these cases are recommended to be used only with partial array self-refresh where performance can be traded off for power savings.

Table 15-111. L3 Address to SDRAM Address Mapping for EMIF_SDRAM_CONFIG[28:27] REG_IBANK_POS = 1 and EMIF_SDRAM_CONFIG_2[27] REG_EBANK_POS = 1

MAddr[31:N]				
Chip-Select	**Bank Address**	**Row Address**	**Bank Address**	**Column Address**
Number of bits defined by EMIF_SDRAM_CONFIG[3] REG_EBANK	Number of bits defined by EMIF_SDRAM_CONFIG[6:4] REG_IBANK	Number of bits defined by EMIF_SDRAM_CONFIG[9:7] REG_ROWSIZE	Number of bits defined by EMIF_SDRAM_CONFIG[6:4] REG_IBANK	Number of bits defined by EMIF_SDRAM_CONFIG[2:0] REG_PAGESIZE
= 0: 0 bit	= 0: 0 bit	= 0: 9 bits	= 0: 0 bit	= 0: 8 bits
= 1: 1 bit	= 1: 0 bit	= 1: 10 bits	= 1: 1 bit	= 1: 9 bits
	= 2: 0 bit	= 2: 11 bits	= 2: 2 bits	= 2: 10 bits
	= 3: 1 bit	= 3: 12 bits	= 3: 2 bits	= 3: 11 bits
		= 4: 13 bits		
		= 5: 14 bits		
		= 6: 15 bits		
		= 7: 16 bits		

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NOTE: N = 1 for 16-bit SDRAM, and N = 2 for 32-bit SDRAM.

The interleaving of banks within a device (per chip-select) is limited to four banks. The EMIF cannot interleave banks between the two chip-selects. Thus, the EMIF can keep a maximum of 16 banks (8 internal banks across two chip-selects) open at a time, but can interleave among only 4 of them.

Table 15-112. L3 Address to SDRAM Address Mapping for EMIF_SDRAM_CONFIG[28:27] REG_IBANK_POS = 2 and EMIF_SDRAM_CONFIG_2[27] REG_EBANK_POS = 1

MAddr[31:N]				
Chip-Select	**Bank Address**	**Row Address**	**Bank Address**	**Column Address**
Number of bits defined by EMIF_SDRAM_CONFIG[3] REG_EBANK	Number of bits defined by EMIF_SDRAM_CONFIG[6:4] REG_IBANK	Number of bits defined by EMIF_SDRAM_CONFIG [9:7] REG_ROWSIZE	Number of bits defined by EMIF_SDRAM_CONFIG [6:4] REG_IBANK	Number of bits defined by EMIF_SDRAM_CONFIG[2:0] REG_PAGESIZE
= 0: 0 bit	= 0: 0 bit	= 0: 9 bits	= 0: 0 bit	= 0: 8 bits
= 1: 1 bit	= 1: 0 bit	= 1: 10 bits	= 1: 1 bit	= 1: 9 bits
	= 2: 1 bit	= 2: 11 bits	= 2: 1 bit	= 2: 10 bits
	= 3: 2 bits	= 3: 12 bits	= 3: 1 bit	= 3: 11 bits
		= 4: 13 bits		
		= 5: 14 bits		
		= 6: 15 bits		
		= 7: 16 bits		

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NOTE: N = 1 for 16-bit SDRAM, and N = 2 for 32-bit SDRAM.

The interleaving of banks within a device (per chip-select) is limited to two banks. The EMIF cannot interleave banks between the two chip-selects. Thus, the EMIF can keep a maximum of 16 banks (8 internal banks across two chip-selects) open at a time, but can interleave among only 2 of them.

Table 15-113. L3 Address to SDRAM Address Mapping for EMIF_SDRAM_CONFIG[28:27] REG_IBANK_POS = 3 and EMIF_SDRAM_CONFIG_2[27] REG_EBANK_POS = 1

MAddr[31:N]			
Chip-Select	**Bank Address**	**Row Address**	**Column Address**
Number of bits defined by EMIF_SDRAM_CONFIG[3] REG_EBANK	Number of bits defined by EMIF_SDRAM_CONFIG[6:4] REG_IBANK	Number of bits defined by EMIF_SDRAM_CONFIG[9:7] REG_ROWSIZE	Number of bits defined by EMIF_SDRAM_CONFIG[2:0] REG_PAGESIZE
= 0: 0 bit	= 0: 0 bit	= 0: 9 bits	= 0: 8 bits
= 1: 1 bit	= 1: 1 bit	= 1: 10 bits	= 1: 9 bits
	= 2: 2 bits	= 2: 11 bits	= 2: 10 bits
	= 3: 3 bits	= 3: 12 bits	= 3: 11 bits
		= 4: 13 bits	
		= 5: 14 bits	
		= 6: 15 bits	
		= 7: 16 bits	

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NOTE: N = 1 for 16-bit SDRAM, and N = 2 for 32-bit SDRAM.

The EMIF cannot interleave banks within a device (per chip-select) or between the two chip-selects. Thus, the EMIF can keep a maximum of 16 banks (8 internal banks across two chip-selects) open at a time, but cannot interleave among them.

Because the EMIF interleaves among fewer banks when REG_IBANK_POS != 0 or REG_EBANK_POS = 1, these cases are lower in performance than the REG_IBANK_POS = 0 case. Thus, these cases are recommended to be used only along with partial array self-refresh, where performance can be traded for power savings.

15.3.4.12 NVM Address Mapping

NVMs are always decoded CSs (bank, row, column) and cannot be interleaved.

15.3.4.13 LPDDR2 SDRAM Initialization

When coming out of reset if the EMIF_SDRAM_CONFIG[31:29] REG_SDRAM_TYPE bit field is equal to 4 or 5, the EMIF performs an LPDDR2 initialization sequence as follows:

1. Drives lpddr2i_ckej[1:0] (where i = 1 or 2 and j = 0 or 1) high and starts to issue NOP commands continuously.
2. After 16 SDRAM refresh rate intervals, issues a PRECHARGE-ALL command. The SDRAM refresh rate is defined in the EMIF_SDRAM_REF_CTRL[15:0] REG_REFRESH_RATE bit field.
3. Issues a RESET command.
4. Software initializes LPDDR2 using the EMIF_LPDDR2_MODE_REG_CFG and EMIF_LPDDR2_MODE_REG_DATA registers. Software must enable refreshes by writing 1 in the EMIF_LPDDR2_MODE_REG_CFG[30] REG_REFRESH_EN bit during the last MRW command.

The EMIF also performs the initialization sequence whenever the EMIF_SDRAM_CONFIG register is written and the LPDDR2 initialization was not performed previously because the SDRAM_REF_CTRL[31] REG_INITREF_DIS bit was set to 0. Once the EMIF performs initialization, rewriting the SDRAM configuration register does not cause reinitialization.

NOTE: The values of the different bit fields in the EMIF_SDRAM_CONFIG and EMIF_SDRAM_CONFIG_2 registers are fixed by the control module at reset. These values must be modified by the header feature in the ROM code configuration or by the initial boot image running from an external XIP booting memory or internal RAM (see Section 27.4.8, *Image Format*). They must not be modified during run time, because they reflect the used hardware LPDDR2 SDRAM and/or NVM memory configurations.

The EMIF does not perform any transactions until the LPDDR2 initialization sequence completes.

When the EMIF comes out of reset, the delay time in Step 2 resulting from the 16 refresh rate intervals + 8 cycles is approximately 16 × EMIF_SDRAM_REF_CTRL[15:0] REG_REFRESH_RATE / input frequency.

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15.3.5 EMIF Programming Guide

15.3.5.1 EMIF Low-Level Programming Models

This section describers the low-level hardware programming sequences for the configuration and use of the EMIF module.

The following programming sequences are double, because there are two EMIF modules (EMIF1 and EMIF2) with the same register mapping but different register addresses.

15.3.5.1.1 Global Initialization

Table 15-114. Global Initialization of Surrounding Modules

Surrounding Modules	Comments
PRCM	The module interface and functional clocks must be enabled. See Chapter 3, *Power, Reset, and Clock Management*.
Interrupt submodule of the MPU	The interrupt requests from the EMIF must be enabled (unmasked). See Chapter 17, *Interrupt Controllers*.
DMM	The EMIF is a slave to the DMM. The DMM must be enabled and configured for communication with LPDDR2 memories. See Section 15.2, *Dynamic Memory Manager*.

15.3.5.1.1.1 EMIF Module Global Initialization

This procedure initializes the EMIF after a power-on reset (POR). It works only with LPDDR2 SDRAM or NVM types. The unused bits in all registers must be written with zeros. The values of the shadow registers are loaded in their corresponding registers when the signal SidleAck is asserted.

NOTE: The values of the different bit fields in the EMIF_SDRAM_CONFIG and EMIF_SDRAM_CONFIG_2 registers are fixed by the control module at reset. These values must be modified by the header feature in the ROM code configuration or by the initial boot image running from an external XIP booting memory or internal RAM (see Section 27.4.8, *Image Format)*. They must not be modified during run time, because they reflect the used hardware LPDDR2 SDRAM and/or NVM memory configurations.

Table 15-115. EMIF Global Initialization

Step	Register/Bit Field/Programming Model	Value
Disable the automatic power management mode.	EMIF_PWR_MGMT_CTRL[10:8] REG_LP_MODE	0x0
Write the shadow register of the EMIF_PWR_MGMT_CTRL with the same value.	EMIF_PWR_MGMT_CTRL_SHDW	EMIF_PWR_MGMT_CTRL
Configure the DDR PHY physical layer to the SDRAM. (Read Latency for the read data from SDRAM in number of DDR clock cycles)	EMIF_DDR_PHY_CTRL_1	0x--------
Write the shadow register of the EMIF_DDR_PHY_CTRL_1 with the same value.	EMIF_DDR_PHY_CTRL_1_SHDW	EMIF_DDR_PHY_CTRL 1
Configure the DDR PHY physical layer to the SDRAM parameters.	EMIF_DDR_PHY_CTRL_2	0x--------
Write the shadow register of the EMIF_SDRAM_REF_CTRL with the same value.	EMIF_SDRAM_REF_CTRL_SHDW	EMIF_SDRAM_REF_CTRL
Define the CS to be used and the mode register address.	EMIF_LPDDR2_MODE_REG_CFG	0x-00000–
Configure the system and low-latency L3 threshold maxima and the priority counter of an old command.	EMIF_L3_CONFIG	0x0-0-00–
Configure the performance counter configuration register.	EMIF_PERF_CNT_CFG	0x-00--00-

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Table 15-115. EMIF Global Initialization (continued)

Step	Register/Bit Field/Programming Model	Value
Configure the performance counter master region select register.	EMIF_PERF_CNT_SEL	0x--0---0-
Define timings and clock parameters.	EMIF Timing Initialization	
Configure the SDRAM output impedance calibration parameters.	EMIF Output Impedance Calibration Mode	
Configure the temperature alert parameters.	EMIF Temperature Monitoring Mode	
Enable system L3 interrupt for command or address error and/or for temperature alert.	EMIF_IRQENABLE_SET_SYS[1:0]	0x3
Enable low-latency L3 interrupt.	EMIF_IRQENABLE_SET_LL[1:0]	0x3
Specify the dummy-data to be written to the memory for refresh cycles.	EMIF_LPDDR2_MODE_REG_DATA	0x000000–
Clear all eventual previous indications of treated interrupts; write the four registers:	EMIF_IRQSTATUS_SYS, EMIF_IRQSTATUS_LL, EMIF_IRQSTATUS_RAW_SYS, EMIF_IRQSTATUS_RAW_LL	0x0000003

Table 15-116. Subprocess Call Summary for Main Sequence – EMIF Global Initialization

Subprocess Name	Cross-Reference
EMIF Timing Initialization	Table 15-117 *EMIF Timing Initialization*
EMIF Output Impedance Calibration Mode	Table 15-118 *EMIF Output Impedance Calibration Mode*
EMIF Temperature Monitoring Mode	Table 15-126 *EMIF Temperature Monitoring Mode*

15.3.5.1.1.2 Subsequence – EMIF Timing Initialization

Table 15-117. Subsequence – EMIF Timing Initialization

Step	Register/Bit Field/Programming Model	Value
Configure the time after which the EMIF being in Idle mode will put the SDRAM in power-saving mode.	EMIF_PWR_MGMT_CTRL[3:0] REG_CS_TIM	0x-
Write the shadow register of the EMIF_PWR_MGMT_CTRL with the same value.	EMIF_PWR_MGMT_CTRL_SHDW	EMIF_PWR_MGMT_CTRL
Configure the LPDDR2-NVM memory timings: 1) Minimum number of DDR clock cycles from power-down exit to any command 2) Minimum number of DDR clock cycles from last write to read 3) Minimum number of DDR clock cycles from preactive to activate 4) Minimum number of DDR clock cycles from last write transfer to activate 5) Minimum number of DDR clock cycles from activate to activate for a different bank 6) Minimum number of DDR clock cycles from activate to read or write	EMIF_LPDDR2_NVM_TIM	0x--------
Write the shadow register of the EMIF_LPDDR2_NVM_TIM with the same value.	EMIF_LPDDR2_NVM_TIM_SHDW	EMIF_LPDDR2_NVM_TIM
Define the rate at which the connected SDRAM devicesare refreshed.	EMIF_SDRAM_REF_CTRL[15:0] REG_REFRESH_RATE	0x----
Write the shadow register of the EMIF_SDRAM_REF_CTRL with the same value.	EMIF_SDRAM_REF_CTRL_SHDW	EMIF_SDRAM_REF_CTRL
Define the timings and clock parameters: 1) Minimum number of DDR clock cycles for which LPDDR2 must remain in self-refresh mode	EMIF_SDRAM_TIM_3	0x0000----

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Table 15-117. Subsequence – EMIF Timing Initialization (continued)

Step	Register/Bit Field/Programming Model	Value
2) Number of DDR clock cycles for a ZQCS command 3) Number of DDR clock that satisfies t DQSCKmax for LPDDR2 4) Minimum number of DDR clock cycles from refresh or load mode to refresh or activate 5) Maximum number of reg_refresh_rate intervals from activate to precharge command		
Write the shadow register of the EMIF_SDRAM_TIM_3.	EMIF_SDRAM_TIM_3_SHDW	EMIF_SDRAM_TIM_3
Define minimum number of DDR clock cycles from power-down exit to any command other than a read command.	EMIF_SDRAM_TIM_2[30:28]REG_T_XP	0x-
Write the shadow register of the EMIF_SDRAM_TIM_2.	EMIF_SDRAM_TIM_2_SHDW	EMIF_SDRAM_TIM_2
Determine the minimum size of the read idle window for read idle detection and the force read idle time.	EMIF_READ_IDLE_CTRL[19:16] REG_READ_IDLE_LEN	0x-
Determine the maximum interval between read idle detections or force.	EMIF_READ_IDLE_CTRL[8:0] REG_READ_IDLE_INTERVAL	0x—
Write the shadow register of the EMIF_READ_IDLE_CTRL with the same value.	EMIF_READ_IDLE_CTRL_SHDW	EMIF_READ_IDLE_CTRL
Configure the temperature alert parameters.	EMIF_TEMP_ALERT_CONFIG	0x--------
Specify the data to be written to the memory.	EMIF_LPDDR2_MODE_REG_DATA	0x000000–

15.3.5.1.2 Operational Modes Configuration

15.3.5.1.2.1 EMIF Output Impedance Calibration Mode

Table 15-118. EMIF Output Impedance Calibration Mode

Step	Register/Bit Field/Programming Model	Value
Determine whether CS1 or CS0 will be used for automatic output impedance calibration (Option 1).	EMIF_ZQ_CONFIG[31:30] REG_ZQ_CS1/0EN	0x-
Determine whether CS1 and CS 0 will be used for automatic output impedance calibration simultaneously (Option 2).	EMIF_ZQ_CONFIG[29] REG_ZQ_DUALCALEN	0x-
Define the interval (number of refresh periods) between ZQCS commands.	EMIF_ZQ_CONFIG[15:0] REG_ZQ_REFINTERVAL	0x----
Define the number of ZQCL intervals that build the ZQINIT interval.	EMIF_ZQ_CONFIG[19:18] REG_ZQ_ZQINIT_MULT	0x-
Define the number of ZQCS intervals that build the ZQCL interval.	EMIF_ZQ_CONFIG[17:16] REG_ZQ_ZQCL_MULT	0x-
Enable the issuing of ZQ-Long command on self-refresh, active power-down, and precharge power-down exit.	EMIF_ZQ_CONFIG[28] REG_ZQ_SFEXITEN	0x1

15.3.5.1.2.2 EMIF Read

Table 15-119. EMIF Read

Step	Register/Bit Field/Programming Model	Value
Define the read latency of the memory.	EMIF_DDR_PHY_CTRL_1[3:0] REG_READ_LATENCY	0x-

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Table 15-119. EMIF Read (continued)

Step	Register/Bit Field/Programming Model	Value
Choose CS0 or CS1 to issue the mode register command.	EMIF_LPDDR2_MODE_REG_CFG[31] REG_CS	0x-
Write the memory address.	EMIF_LPDDR2_MODE_REG_CFG[7:0] REG_ADDRESS	0x----
Initiate read command by reading the register.	EMIF_LPDDR2_MODE_REG_DATA[7:0]	Configure the SDRAM output impedance calibration parameters 0x-00-----

15.3.5.1.2.3 EMIF Write

Table 15-120. EMIF Write

Step	Register/Bit Field/Programming Model	Value
Choose CS0 or CS1 to issue mode register command.	EMIF_LPDDR2_MODE_REG_CFG[31] REG_CS	0x-
Write the memory address.	EMIF_LPDDR2_MODE_REG_CFG[7:0] REG_ADDRESS	0x----
Define the minimum number of DDR clock cycles from last write transfer to precharge.	EMIF_SDRAM_TIM_1[20:17] REG_T_WR	0x-
Supply the data byte to be written and initiate write command by writing the register.	EMIF_LPDDR2_MODE_REG_DATA[7:0] REG_VALUE_0	0x–

15.3.5.1.2.4 EMIF SDRAM Refresh

Table 15-121. EMIF SDRAM Refresh

Step	Register/Bit Field/Programming Model	Value
Define the minimum number of DDR clock cycles from refresh or load mode to refresh or activate.	EMIF_SDRAM_TIM_3[12:4] REG_T_RFC	0x----
Write the shadow register of EMIF_SDRAM_TIM_3.	EMIF_SDRAM_TIM_3_SHDW	EMIF_SDRAM_TIM_3
Define the rate at which the connected SDRAM devices are refreshed.	EMIF_SDRAM_REF_CTRL[15:0] REG_REFRESH_RATE	0x----
Disable the SDRAM-DDR1/2/3 refresh.	EMIF_SDRAM_REF_CTRL[31] REG_INITREF_DIS	0x1
Write the shadow register of EMIF_SDRAM_REF_CTRL.	EMIF_SDRAM_REF_CTRL _SHDW	EMIF_SDRAM_REF_CTRL
Choose CS0 or CS1 to issue mode register command.	EMIF_LPDDR2_MODE_REG_CFG[31]	0x-
Enable refresh for SDRAM-LPDDR2 memory.	EMIF_LPDDR2_MODE_REG_CFG[30]	0x1
Dummy write to start the LPDDR2 refresh cycles.	EMIF_LPDDR2_MODE_REG_DATA	0x00000000

15.3.5.1.2.5 EMIF SDRAM Self-Refresh

Table 15-122. EMIF SDRAM Self-Refresh

Step	Register/Bit Field/Programming Model	Value
Define minimum number of DDR clock cycles from self-refresh exit to any command other than a read command.	EMIF_SDRAM_TIM_2[24:16] REG_T_XSNR	0x—
Write the shadow register of EMIF_SDRAM_TIM_2.	EMIF_SDRAM_TIM_2_SHDW	EMIF_SDRAM_TIM_ 2

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Table 15-122. EMIF SDRAM Self-Refresh (continued)

Step	Register/Bit Field/Programming Model	Value
Enable self-refresh mode.	EMIF_PWR_MGMT_CTRL[10:8] REG_LP_MODE	0x2

15.3.5.1.2.6 EMIF LPDDR2 (SDRAM or NVM) Power-Down Mode

Table 15-123. EMIF SDRAM Power-Down Mode

Step	Register/Bit Field/Programming Model	Value
Define minimum number of DDR clock cycles from power-down exit to any command other than a read command.	EMIF_SDRAM_TIM_2[30:28] REG_T_XP	0x-
Write the shadow register of EMIF_SDRAM_TIM_2.	EMIF_SDRAM_TIM_2_SHDW	EMIF_SDRAM_TIM_2
Define the number of DDR clock cycles after which the external memory will be put in power-saving mode when the EMIF enters idle mode.	EMIF_PWR_MGMT_CTRL[3:0] REG_CS_TIM	0x-
Enable (enter) power-down mode.	EMIF_PWR_MGMT_CTRL[10:8] REG_LP_MODE	0x4

15.3.5.1.2.7 EMIF LPDDR2-SDRAM Deep Power-Down Mode

Table 15-124. EMIF LPDDR2-SDRAM Deep Power-Down Mode

Step	Register/Bit Field/Programming Model	Value
Define minimum number of DDR clock cycles from power-down exit to any command other than a read command.	EMIF_SDRAM_TIM_2[30:28] REG_T_XP	0x-
Write the shadow register of EMIF_SDRAM_TIM_2.	EMIF_SDRAM_TIM_2_SHDW	EMIF_SDRAM_TIM_2
Define the number of DDR clock cycles after which the external memory will be put in power-saving mode when the EMIF enters idle mode.	EMIF_PWR_MGMT_CTRL[3:0] REG_CS_TIM	0x-
Enable (enter) deep power-down mode.	EMIF_PWR_MGMT_CTRL[11] REG_DPD_EN	0x1

15.3.5.1.2.8 EMIF Global Warm Reset (Software Reset)

Table 15-125. EMIF Global Warm Reset (Software Reset)

Step	Register/Bit Field/Programming Model	Value
IF: External request for reset	Input signal EMIFi_GLOBAL_RST	Asserted (see the programming model in the PRCM chapter)
Follow the sequence in Section 15.3.5.1.2.5 *EMIF SDRAM Self-Refresh Sequence*.	EMIF_PWR_MGMT_CTRL[10:8] REG_LP_MODE	0x2
ELSE:	Input signal EMIFi_GLOBAL_RST	Deasserted (see the programming model in the PRCM chapter)
Disable (exit) self-refresh mode when not needed.	EMIF_PWR_MGMT_CTRL[10:8] REG_LP_MODE	0x0
ENDIF		

15.3.5.1.2.9 EMIF Temperature Monitoring Mode

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Table 15-126. EMIF Temperature Monitoring Mode

Step	Register/Bit Field/Programming Model	Value
Determine whether CS1 or CS0 will be used for temperature alert polling.	EMIF_TEMP_ALERT_CONFIG[31:30] REG_TA_CS1/0EN	0x-
Define the interval (number of refresh periods) between temperature alert polls.	EMIF_TEMP_ALERT_CONFIG[21:0] REG_TA_REFINTERVAL	0x------
Define how wide the physical memory device will be.	EMIF_TEMP_ALERT_CONFIG[27:26] REG_TA_DEVWDT	0x-
Define which external byte lanes will contain a device for temperature monitoring (which devices to be polled).	EMIF_TEMP_ALERT_CONFIG[25:24] REG_TA_DEVCNT	0x-
Enable system L3 interrupt for SDRAM temperature alert.	EMIF_IRQENABLE_SET_SYS[1] REG_EN_TA_SYS	0x1
Enable low-latency L3 interrupt for SDRAM temperature alert.	EMIF_IRQENABLE_SET_LL[1] REG_EN_TA_LL	0x1
Enable the issuing of a temperature alert poll on self-refresh exit (poll for temperature change every time EMIF exits self-refresh, active power-down, and precharge power-down modes).	EMIF_TEMP_ALERT_CONFIG[28] REG_TA_SFEXITEN	0x1

15.3.5.1.3 EMIF Events Servicing

15.3.5.1.3.1 Interrupt Servicing

This section describes event servicing (interrupt treatment) of the EMIF module.

The following Interrupt mechanism is double, because there are two EMIF modules with different register addresses and two Interrupt lines, EMIF1_IRQ and EMIF2_IRQ.

Table 15-127. EMIF Event Servicing

Step	Registe/Bit Field/Programming Model	Value
Clear all eventual previous indications of treated interrupts, and write the four registers:	EMIF_IRQSTATUS_SYS, EMIF_IRQSTATUS_LL, EMIF_IRQSTATUS_RAW_SYS, EMIF_IRQSTATUS_RAW_LL	0x0000003
Enable the system L3 interrupts.	EMIF_IRQENABLE_SET_SYS	0x0000003
Enable the low-latency L3 interrupts.	EMIF_IRQENABLE_SET_LL	0x0000003
Wait until an event occurs.		
Read the status registers:	EMIF_IRQSTATUS_SYS, EMIF_IRQSTATUS_LL, EMIF_IRQSTATUS_RAW_SYS, EMIF_IRQSTATUS_RAW_LL	
IF: the EMIF_IRQSTATUS_SYS[0] = 1		
Read the error log register and determine the addressing mode, command type, and connection ID of the first errored transaction:	EMIF_L3_ERR_LOG	
Start the interrupt handler for system L3 – Command/address error.	INTC of the MPU	
ELSE IF: the EMIF_IRQSTATUS_SYS[1] = 1		
Read the error log register and determine the addressing mode, command type, and connection ID of the first errored transaction:	EMIF_L3_ERR_LOG	
Start the interrupt handler for system L3 – Temperature alert.	INTC of the MPU	
Update the REFRESH_RATE to the required value as per the temperature change.	EMIF_SDRAM_REF_CTRL[15:0] REG_REFRESH_RATE	0x----
ELSE IF: the EMIF_IRQSTATUS_RAW_SYS[0] = 1		

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Table 15-127. EMIF Event Servicing (continued)

Step	Registe/Bit Field/Programming Model	Value
Read the error log register and determine the addressing mode, command type, and connection ID of the first errored transaction:	EMIF_L3_ERR_LOG	
Start the interrupt handler for raw system L3 – Command/address error.	INTC of the MPU	
ELSE IF: the EMIF_IRQSTATUS_RAW_SYS[1] = 1		
Read the error log register and determine the addressing mode, command type, and connection ID of the first errored transaction:	EMIF_L3_ERR_LOG	
Start the interrupt handler for raw system L3 – Temperature alert	INTC of the MPU	
Update the REFRESH_RATE to the required value as per the temperature change.	EMIF_SDRAM_REF_CTRL[15:0] REG_REFRESH_RATE	0x----
ELSE IF: the EMIF_IRQSTATUS_LL[0] = 1		
Read the error log register and determine the addressing mode, command type, and connection ID of the first errored transaction:	EMIF_L3_ERR_LOG	
Start the interrupt handler for low-latency L3 – Command/address error.	INTC of the MPU	
ELSE IF: the EMIF_IRQSTATUS_LL[1] =1		
Read the error log register and determine the addressing mode, command type, and connection ID of the first errored transaction:	EMIF_L3_ERR_LOG	
Start the interrupt handler for low-latency L3 – Temperature alert.	INTC of the MPU	
Update the REFRESH_RATE to the required value as per the temperature change.	EMIF_SDRAM_REF_CTRL[15:0] REG_REFRESH_RATE	0x----
ELSE IF: The EMIF_IRQSTATUS_RAW_LL[0] = 1		
Read the error log register and determine the addressing mode, command type, and connection ID of the first errored transaction:	EMIF_L3_ERR_LOG	
Start the interrupt handler for raw low-latency L3 – Command/address error	INTC of the MPU	
ELSE: The EMIF_IRQSTATUS_RAW_LL[1] = 1		
Read the error log register and determine the addressing mode, command type, and connection ID of the first errored transaction:	EMIF_L3_ERR_LOG	
Start the interrupt handler for raw low-latency L3 – Temperature alert.	INTC of the MPU	
Update the REFRESH_RATE to the required value as per the temperature change.	EMIF_SDRAM_REF_CTRL[15:0] REG_REFRESH_RATE	0x----
ENDIF		
Wait until the termination of the corresponding interrupt handler.	IINTC of the MPU	
IF: Address/command error was treated		
Clear the LSB in the relevant IRQ status registers, SYS or LL; write both registers:	EMIF_IRQSTATUS_SYS[0] REG_ERR_SYS and EMIF_IRQSTATUS_RAW_SYS[0] REG_ERR_SYS, or EMIF_IRQSTATUS_LL[0] REG_ERR_LL and EMIF_IRQSTATUS_RAW_LL[0] REG_ERR_LL	0x1
Disable the corresponding interrupt if needed; write:	EMIF_IRQENABLE_CLR_SYS[0] REG_EN_ERR_SYS or EMIF_IRQENABLE_CLR_LL[0] REG_EN_ERR_LL	0x1
ELSE: (Temperature alert proceeded)		

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Table 15-127. EMIF Event Servicing (continued)

Step	Registe/Bit Field/Programming Model	Value
Clear the corresponding bit in the relevant IRQ status registers, SYS or LL; write both registers:	EMIF_IRQSTATUS_SYS[1] REG_TA_SYS and EMIF_IRQSTATUS_RAW_SYS[1] REG_TA_SYS, or EMIF_IRQSTATUS_LL[1] REG_TA_LL and EMIF_IRQSTATUS_RAW_LL[1] REG_TA_LL	0x1
Disable the corresponding interrupt if needed; write:	EMIF_IRQENABLE_CLR_SYS[1] REG_EN_TA_SYS or EMIF_IRQENABLE_CLR_LL[1] REG_EN_TA_LL	0x1
ENDIF		

15.3.6 EMIF Register Manual

Table 15-128 lists the EMIF instance.

15.3.6.1 EMIF Instance Summary

Table 15-128. EMIF Instance Summary

Module Name	Base Address	Size
EMIF1	0x4C00 0000	16MB
EMIF2	0x4D00 0000	16MB

15.3.6.2 EMIF Registers

Table 15-129 summarizes the EMIF register mapping.

15.3.6.2.1 EMIF Register Summary

Table 15-129. EMIF Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	EMIF1 L3 Physical Address	EMIF2 L3 Physical Address
EMIF_MOD_ID_REV	R	32	0x0000 0000	0x4C00 0000	0x4D00 0000
EMIF_STATUS	R	32	0x0000 0004	0x4C00 0004	0x4D00 0004
EMIF_SDRAM_CONFIG	RW	32	0x0000 0008	0x4C00 0008	0x4D00 0008
EMIF_SDRAM_CONFIG_2	RW	32	0x0000 000C	0x4C00 000C	0x4D00 000C
EMIF_SDRAM_REF_CTRL	RW	32	0x0000 0010	0x4C00 0010	0x4D00 0010
EMIF_SDRAM_REF_CTRL_SHDW	RW	32	0x0000 0014	0x4C00 0014	0x4D00 0014
EMIF_SDRAM_TIM_1	RW	32	0x0000 0018	0x4C00 0018	0x4D00 0018
EMIF_SDRAM_TIM_1_SHDW	RW	32	0x0000 001C	0x4C00 001C	0x4D00 001C
EMIF_SDRAM_TIM_2	RW	32	0x0000 0020	0x4C00 0020	0x4D00 0020
EMIF_SDRAM_TIM_2_SHDW	RW	32	0x0000 0024	0x4C00 0024	0x4D00 0024
EMIF_SDRAM_TIM_3	RW	32	0x0000 0028	0x4C00 0028	0x4D00 0028
EMIF_SDRAM_TIM_3_SHDW	RW	32	0x0000 002C	0x4C00 002C	0x4D00 002C

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Table 15-129. EMIF Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	EMIF1 L3 Physical Address	EMIF2 L3 Physical Address
EMIF_LPDDR2_NVM_TIM	RW	32	0x0000 0030	0x4C00 0030	0x4D00 0030
EMIF_LPDDR2_NVM_TIM_SHDW	RW	32	0x0000 0034	0x4C00 0034	0x4D00 0034
EMIF_PWR_MGMT_CTRL	RW	32	0x0000 0038	0x4C00 0038	0x4D00 0038
EMIF_PWR_MGMT_CTRL_SHDW	RW	32	0x0000 003C	0x4C00 003C	0x4D00 003C
EMIF_LPDDR2_MODE_REG_DATA	RW	32	0x0000 0040	0x4C00 0040	0x4D00 0040
EMIF_LPDDR2_MODE_REG_CFG	RW	32	0x0000 0050	0x4C00 0050	0x4D00 0050
EMIF_L3_CONFIG	RW	32	0x0000 0054	0x4C00 0054	0x4D00 0054
EMIF_L3_CFG_VAL_1	R	32	0x0000 0058	0x4C00 0058	0x4D00 0058
EMIF_L3_CFG_VAL_2	R	32	0x0000 005C	0x4C00 005C	0x4D00 005C
EMIF_PERF_CNT_1	R	32	0x0000 0080	0x4C00 0080	0x4D00 0080
EMIF_PERF_CNT_2	R	32	0x0000 0084	0x4C00 0084	0x4D00 0084
EMIF_PERF_CNT_CFG	RW	32	0x0000 0088	0x4C00 0088	0x4D00 0088
EMIF_PERF_CNT_SEL	RW	32	0x0000 008C	0x4C00 008C	0x4D00 008C
EMIF_PERF_CNT_TIM	R	32	0x0000 0090	0x4C00 0090	0x4D00 0090
EMIF_READ_IDLE_CTRL	RW	32	0x0000 0090	0x4C00 0098	0x4D00 0098
EMIF_READ_IDLE_CTRL_SHDW	RW	32	0x0000 0090	0x4C00 009C	0x4D00 009C
EMIF_IRQSTATUS_RAW_SYS	RW	32	0x0000 00A4	0x4C00 00A4	0x4D00 00A4
EMIF_IRQSTATUS_RAW_LL	RW	32	0x0000 00A8	0x4C00 00A8	0x4D00 00A8
EMIF_IRQSTATUS_SYS	RW	32	0x0000 00AC	0x4C00 00AC	0x4D00 00AC
EMIF_IRQSTATUS_LL	RW	32	0x0000 00B0	0x4C00 00B0	0x4D00 00B0
EMIF_IRQENABLE_SET_SYS	RW	32	0x0000 00B4	0x4C00 00B4	0x4D00 00B4
EMIF_IRQENABLE_SET_LL	RW	32	0x0000 00B8	0x4C00 00B8	0x4D00 00B8
EMIF_IRQENABLE_CLR_SYS	RW	32	0x0000 00BC	0x4C00 00BC	0x4D00 00BC
EMIF_IRQENABLE_CLR_LL	RW	32	0x0000 00C0	0x4C00 00C0	0x4D00 00C0
EMIF_ZQ_CONFIG	RW	32	0x0000 00C8	0x4C00 00C8	0x4D00 00C8
EMIF_TEMP_ALERT_CONFIG	RW	32	0x0000 00CC	0x4C00 00CC	0x4D00 00CC
EMIF_L3_ERR_LOG	R	32	0x0000 00D0	0x4C00 00D0	0x4D00 00D0
EMIF_DDR_PHY_CTRL_1	RW	32	0x0000 00E4	0x4C00 00E4	0x4D00 00E4

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Table 15-129. EMIF Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	EMIF1 L3 Physical Address	EMIF2 L3 Physical Address
EMIF_DDR_PHY_CTRL_1_SHDW	RW	32	0x0000 00E8	0x4C00 00E8	0x4D00 00E8
EMIF_DDR_PHY_CTRL_2	RW	32	0x0000 00EC	0x4C00 00EC	0x4D00 00EC

NOTE: The values of the different bit fields in the EMIF_SDRAM_CONFIG and EMIF_SDRAM_CONFIG2 registers are fixed by the control module at reset. These values must be modified by the header feature in the ROM code configuration or by the initial boot image running from an external XIP booting memory or internal RAM (see Section 27.4.8, *Image Format*). They must not be modified during run time, because they reflect the used hardware LPDDR2 SDRAM and/or NVM memory configurations.

15.3.6.2.2 EMIF Register Description

Table 15-130 through Table 15-213 describe the individual EMIF registers.

Table 15-130. EMIF_MOD_ID_REV

Address Offset	0x0000 0000		
Physical Address	0x4C00 0000 0x4D00 0000	**Instance**	EMIF1 EMIF2
Description	Revision number register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

Bits	Field Name	Description	Type	Reset
31:0	RESERVED	Reserved for future use	R	0x---- ---- (1)

(1) TI internal data

Table 15-131. Register Call Summary for Register EMIF_MOD_ID_REV

EMIF Controller
- Arbitration: [0] [1]
- EMIF Register Summary: [2]

Table 15-132. EMIF_STATUS

Address Offset	0x0000 0004		
Physical Address	0x4C00 0004 0x4D00 0004	**Instance**	EMIF1 EMIF2
Description	SDRAM Status Register (STATUS)		
Type	R		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REG_BE	REG_DUAL_CLK_MODE	REG_FAST_INIT	RESERVED																										REG_PHY_DLL_READY	RESERVED	

Bits	Field Name	Description	Type	Reset
31	REG_BE	Big endian mode select for 8 and 16-bit devices, set to 1 for big endian or 0 for little endian operation.	R	0
30	REG_DUAL_CLK_MODE	Dual Clock mode. Defines whether the L3_clk and EMIF_FCLK clock are asynchronous. L3_clk and EMIF_FCLK clock are asynchronous, if set to 1.	R	1
29	REG_FAST_INIT	Fast Init. Defines whether the EMIF fast initialization mode has been enabled. Fast initialization is enabled if set to 1.	R	0
28:3	RESERVED	Reserved	R	0x0000000
2	REG_PHY_DLL_READY	DDR PHY Ready. Reflects the value on the phy_ready port (active high) that defines whether the DDR PHY is ready for normal operation. The DDR PHY is ready for normal operation, if set to 1.	R	1
1:0	RESERVED	Reserved	R	0x0

Table 15-133. Register Call Summary for Register EMIF_STATUS

EMIF Controller

- EMIF Register Summary: [0]

Table 15-134. EMIF_SDRAM_CONFIG

Address Offset	0x0000 0008		
Physical Address	0x4C00 0008 0x4D00 0008	**Instance**	EMIF1 EMIF2
Description	SDRAM Config Register. A write to this register will cause the EMIF to start the SDRAM initialization sequence if it was not performed previously because EMIF_SDRAM_REF_CTRL[31] REG_INITREF_DIS was a zero.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REG_SDRAM_TYPE			REG_IBANK_POS		RESERVED			REG_DDR2_DDQS	RESERVED		REG_DDR_DISABLE_DLL	RESERVED				REG_NARROW_MODE		REG_CL			REG_ROWSIZE			REG_IBANK			REG_EBANK		REG_PAGESIZE		

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Bits	Field Name	Description	Type	Reset
31:29	REG_SDRAM_TYPE	SDRAM Type selection. Set to 4 for LPDDR2-S4, Set to 5 for LPDDR2-S2 All other value are reserved.	RW	0x- (1)
28:27	REG_IBANK_POS	Internal bank position. Set to 0 to assign internal bank address bits from L3 address as shown in Table 15-106 and Table 15-107. Set to 1, 2, or 3 to assign internal bank address bits from L3 address as shown in Table 15-108, Table 15-109, and Table 15-110.	RW	0x- (1)
26:24	RESERVED	RESERVED	RW	0x0
23	REG_DDR2_DDQS	DDR2 differential DQS enable. Set to 0 for single-ended DQS. Set to 1 for differential DQS. This bit is only for DDR2 mode, because the device supports LPDDR2; this bit is don't care.	RW	0x- (1)
22:21	RESERVED	RESERVED	RW	0x- (1)
20	REG_DDR_DISABLE_DLL	Disable DLL select. Set to 1 to disable DLL inside SDRAM.	RW	0x- (1)
19:16	RESERVED	RESERVED	RW	0x0
15:14	REG_NARROW_MODE	SDRAM data bus width. Set to 0 for 32-bit and set to 1 for 16-bit. All other values are reserved.	RW	0x- (2)
13:10	REG_CL	CAS Latency. The value of this field defines the CAS latency to be used when accessing connected SDRAM devices. Value of 3, 4, 5, 6, 7, and 8 (CAS latency of 3, 4, 5, 6, 7, and 8) are supported for LPDDR2-SDRAM. All other values are reserved.	RW	0x- (2)

(1) Value fixed by the control module at reset
(2) Value fixed by the control module at reset

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Bits	Field Name	Description	Type	Reset
9:7	REG_ROWSIZE	Row Size. Defines the number of row address bits of connected SDRAM devices. Set to 0 for 9 row bits, Set to 1 for 10 row bits, Set to 2 for 11 row bits, Set to 3 for 12 row bits, Set to 4 for 13 row bits, Set to 5 for 14 row bits, Set to 6 for 15 row bits, Set to 7 for 16 row bits. This field is only used when EMIF_SDRAM_CONFIG[28:27] REG_IBANK_POS field is set to 1, 2, or 3 or REG_EBANK_POS field in EMIF_SDRAM_CONFIG_2 register is set to 1.	RW	0x- (3)
6:4	REG_IBANK	Internal Bank setup. Defines number of banks inside connected SDRAM devices. Set to 0 for 1 bank, Set to 1 for 2 banks, Set to 2 for 4 banks, Set to 3 for 8 banks. All other values are reserved.	RW	0x- (3)
3	REG_EBANK	External chip select setup. Defines whether SDRAM accesses will use 1 or 2 chip select lines. Set to 0 to use pad_cs_o_n[0] only. Set to 1 to use pad_cs_o_n[1:0]. This bit will automatically be set to 0 if EMIF_SDRAM_CONFIG_2[30] REG_CS1NVMEN field is set to 1.	RW	0x- (3)
2:0	REG_PAGESIZE	Page Size. Defines the internal page size of connected SDRAM devices. Set to 0 for 256-word page (8 column bits), Set to 1 for 512-word page (9 column bits), Set to 2 for 1024-word page (10 column bits), Set to 3 for 2048-word page (11 column bits). All other values are reserved.	RW	0x- (3)

(3) Value fixed by the control module at reset

Table 15-135. Register Call Summary for Register EMIF_SDRAM_CONFIG

EMIF Controller

- Arbitration: [0]
- EMIF Access Cycles: [1]
- SDRAM Address Mapping: [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23] [24] [25] [26] [27] [28] [29] [30] [31] [32] [33] [34] [35] [36] [37] [38] [39] [40] [41] [42] [43] [44] [45] [46] [47] [48] [49] [50] [51] [52] [53] [54] [55] [56]
- LPDDR2 SDRAM Initialization: [57] [58] [59]
- Global Initialization: [60]
- EMIF Register Summary: [61] [62] [63]
- EMIF Register Description: [64]

Table 15-136. EMIF_SDRAM_CONFIG_2

Address Offset	0x0000 000C
Physical Address	0x4C00 000C 0x4D00 000C
Description	
Type	RW

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	REG_CS1NVMEN	RESERVED		REG_EBANK_POS	RESERVED																					REG_RDBNUM		RESERVED			REG_RDBSIZE	

Bits	Field Name	Description	Type	Reset
31	RESERVED		R	0
30	REG_CS1NVMEN	CS1 LPDDR2-NVM enable. Set to 1 if LPDDR2-NVM is connected to CS1. This bit will automatically be set to 0 if reg_sdram_type field in the SDRAM Config register is not set to LPDDR2.	RW	0x-(1)
29:28	RESERVED		R	0x0
27	REG_EBANK_POS	External bank position. Set to 0 to assign external bank address bits from lower OCP address as shown in tables. Set to 1 to assign external bank address bits from higher OCP address bits as shown in tables.	RW	0
26:6	RESERVED		R	0x000000
5:4	REG_RDBNUM	Row Buffer setup. Defines number of row buffers inside connected LPDDR2-NVM devices. Set to 0 for 1 row buffer, set to 1 for 2 row buffers, set to 2 for 4 row buffers, and set to 3 for 8 row buffers. All other values are reserved.	RW	0x-(1)
3	RESERVED		R	0
2:0	REG_RDBSIZE	Row Data Buffer Size. Defines the row data buffer size of connected LPDDR2-NVM devices. Set to 0 for 32 bytes, set to 1 for 64 bytes, set to 2 for 128 bytes, set to 3 for 256 bytes, set to 4 for 512 bytes, set to 5 for 1024 bytes, set to 6 for 2048 bytes, and set to 7 for 4096 bytes.	RW	0x-(1)

(1) Value fixed by the control module at reset

Table 15-137. Register Call Summary for Register EMIF_SDRAM_CONFIG_2

EMIF Controller

- LPDDR2 SDRAM Initialization: [0]
- Global Initialization: [1]
- EMIF Register Summary: [2]
- EMIF Register Description: [3] [4]

Table 15-138. EMIF_SDRAM_REF_CTRL

Address Offset	0x0000 0010		
Physical Address	0x4C00 0010 0x4D00 0010	**Instance**	EMIF1 EMIF2
Description	SDRAM Refresh Control Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REG_INITREF_DIS								RESERVED								REG_REFRESH_RATE															

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Bits	Field Name	Description	Type	Reset
31	REG_INITREF_DIS	Initialization and Refresh disable. When set to 1, EMIF will disable SDRAM initialization and refreshes, but will carry out SDRAM write/read transactions.	RW	0
30:16	RESERVED	Reserved	R	0
15:0	REG_REFRESH_RATE	Refresh Rate. Value in this field is used to define the rate at which connected SDRAM devices will be refreshed. SDRAM refresh rate = DDR clock rate/reg_refresh_rate. To avoid lock-up situations, the programmer must not program reg_refresh_rate < (6 × reg_t_rfc).	RW	0x0000

Table 15-139. Register Call Summary for Register EMIF_SDRAM_REF_CTRL

EMIF Controller

- Arbitration: [0]
- SDRAM Temperature Monitoring: [1]
- SDRAM Refresh Scheduling: [2] [3] [4]
- LPDDR2 SDRAM Initialization: [5] [6]
- Global Initialization: [7] [8] [9] [10] [11]
- Operational Modes Configuration: [12] [13] [14] [15] [16]
- EMIF Events Servicing: [17] [18] [19] [20]
- EMIF Register Summary: [21]
- EMIF Register Description: [22] [23] [24]

Table 15-140. EMIF_SDRAM_REF_CTRL_SHDW

Address Offset	0x0000 0014		
Physical Address	0x4C00 0014 0x4D00 0014	**Instance**	EMIF1 EMIF2
Description	SDRAM Refresh Control Shadow Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																REG_REFRESH_RATE_SHDW															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x0000
15:0	REG_REFRESH_RATE_SHDW	Shadow field for REG_REFRESH_RATE. This field is loaded into EMIF_SDRAM_REF_CTRL[15:0] REG_REFRESH_RATE field when SIdleAck is asserted. This register is not auto corrected when the value is invalid.	RW	0x0000

Table 15-141. Register Call Summary for Register EMIF_SDRAM_REF_CTRL_SHDW

EMIF Controller

- Global Initialization: [0] [1]
- EMIF Register Summary: [2]

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Table 15-142. EMIF_SDRAM_TIM_1

Address Offset	0x0000 0018		
Physical Address	0x4C00 0018 0x4D00 0018	**Instance**	EMIF1 EMIF2
Description	SDRAM Timing 1 Register. If this register is byte written, care must be taken that all the fields are written before performing any accesses to the SDRAM.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			REG_T_RP					REG_T_RCD				REG_T_WR				REG_T_RAS				REG_T_RC						REG_T_RRD			REG_T_WTR		

Bits	Field Name	Description	Type	Reset
31:29	RESERVED	Reserved	R	0x0
28:25	REG_T_RP	Minimum number of DDR clock cycles from Precharge to Activate or Refresh, minus one.	RW	0x0
24:21	REG_T_RCD	Minimum number of DDR clock cycles from Activate to Read or Write, minus one.	RW	0x0
20:17	REG_T_WR	Minimum number of DDR clock cycles from last Write transfer to Precharge, minus one.	RW	0x0
16:12	REG_T_RAS	Minimum number of DDR clock cycles from Activate to Precharge, minus one. reg_t_ras value needs to be bigger than or equal to reg_t_rcd value.	RW	0x0
11:6	REG_T_RC	Minimum number of DDR clock cycles from Activate to Activate, minus one.	RW	000010
5:3	REG_T_RRD	Minimum number of DDR clock cycles from Activate to Activate for a different bank, minus one. For an 8-bank, this field must be equal to ((tFAW/(4*tCK))-1).	RW	100
2:0	REG_T_WTR	Minimum number of DDR clock cycles from last Write to Read, minus one.	RW	11

Table 15-143. Register Call Summary for Register EMIF_SDRAM_TIM_1

EMIF Controller

- Operational Modes Configuration: [0]
- EMIF Register Summary: [1]
- EMIF Register Description: [2] [3] [4] [5] [6] [7] [8]

Table 15-144. EMIF_SDRAM_TIM_1_SHDW

Address Offset	0x0000 001C		
Physical Address	0x4C00 001C 0x4D00 001C	**Instance**	EMIF1 EMIF2
Description	SDRAM Timing 1 Shadow Register		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			REG_T_RP_SHDW					REG_T_RCD_SHDW				REG_T_WR_SHDW				REG_T_RAS_SHDW				REG_T_RC_SHDW				REG_T_RRD_SHDW				REG_T_WTR_SHDW			

Bits	Field Name	Description	Type	Reset
31:29	RESERVED	Reserved	R	0x0
28:25	REG_T_RP_SHDW	Shadow field for REG_T_RP. This field is loaded into EMIF_SDRAM_TIM_1[28:25] REG_T_RP field when SIdleAck is asserted.	RW	0x0
24:21	REG_T_RCD_SHDW	Shadow field for REG_T_RCD. This field is loaded into EMIF_SDRAM_TIM_1[24:21] REG_T_RCD field when SIdleAck is asserted.	RW	0x0
20:17	REG_T_WR_SHDW	Shadow field for REG_T_WR. This field is loaded into EMIF_SDRAM_TIM_1[20:17] REG_T_WR field when SIdleAck is asserted.	RW	0x0
16:12	REG_T_RAS_SHDW	Shadow field for REG_T_RAS. This field is loaded into EMIF_SDRAM_TIM_1[16:12] REG_T_RAS field when SIdleAck is asserted.	RW	0x00
11:6	REG_T_RC_SHDW	Shadow field for REG_T_RC. This field is loaded into EMIF_SDRAM_TIM_1[11:6] REG_T_RC field when SIdleAck is asserted.	RW	000010
5:3	REG_T_RRD_SHDW	Shadow field for REG_T_RRD. This field is loaded into EMIF_SDRAM_TIM_1[5:3] REG_T_RRD field when SIdleAck is asserted.	RW	0x4
2:0	REG_T_WTR_SHDW	Shadow field for REG_T_WTR. This field is loaded into EMIF_SDRAM_TIM_1[2:0] REG_T_WTR field when SIdleAck is asserted.	RW	0x3

Table 15-145. Register Call Summary for Register EMIF_SDRAM_TIM_1_SHDW

EMIF Controller

- EMIF Register Summary: [0]

Table 15-146. EMIF_SDRAM_TIM_2

Address Offset	0x0000 0020		
Physical Address	0x4C00 0020 0x4D00 0020	**Instance**	EMIF1 EMIF2
Description	SDRAM Timing 2 Register. If this register is byte written, care must be taken that all the fields are written before performing any accesses to the SDRAM.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		REG_T_XP			RESERVED			REG_T_XSNR								REG_T_XSRD										REG_T_RTP				REG_T_CKE			

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Bits	Field Name	Description	Type	Reset
31	RESERVED	Reserved	R	0
30:28	REG_T_XP	Minimum number of DDR clock cycles from power-down exit to any command other than a read command, minus one.	RW	0x2
27:25	RESERVED	reserved	R	0x0
24:16	REG_T_XSNR	Minimum number of DDR clock cycles from Self-Refresh exit to any command other than a Read command, minus one. REG_T_XSNR and REG_T_XSRD must be programmed with the same value.	RW	0x0A
15:6	REG_T_XSRD	Minimum number of DDR clock cycles from Self-Refresh exit to a Read command, minus one. REG_T_XSNR and REG_T_XSRD must be programmed with the same value.	RW	0000001010
5:3	REG_T_RTP	Minimum number of DDR clock cycles for the last read command to a Precharge command, minus one.	RW	001
2:0	REG_T_CKE	Minimum number of DDR clock cycles between pad_cke_o changes, minus one.	RW	010

Table 15-147. Register Call Summary for Register EMIF_SDRAM_TIM_2

EMIF Controller

- LPDDR2-SDRAM Power-Down Mode: [0]
- LPDDR2-NVM Power-Down Mode: [1]
- LPDDR2-SDRAM Self-Refresh Mode: [2] [3]
- Global Initialization: [4] [5] [6]
- Operational Modes Configuration: [7] [8] [9] [10] [11] [12] [13] [14]
- EMIF Register Summary: [15]
- EMIF Register Description: [16] [17] [18] [19] [20]

Table 15-148. EMIF_SDRAM_TIM_2_SHDW

Address Offset	0x0000 0024		
Physical Address	0x4C00 0024 0x4D00 0024	**Instance**	EMIF1 EMIF2
Description	SDRAM Timing 2 Shadow Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				REG_T_XP_SHDW				RESERVED								REG_T_XSNR_SHDW								REG_T_XSRD_SHDW								REG_T_RTP_SHDW				REG_T_CKE_SHDW			

Bits	Field Name	Description	Type	Reset
31	RESERVED	Reserved	R	0
30:28	REG_T_XP_SHDW	Shadow field for REG_T_XP. This field is loaded into EMIF_SDRAM_TIM_2[30:28] REG_T_XP field when SIdleAck is asserted.	RW	0x2
27:25	RESERVED	Reserved	RW	0x0
24:16	REG_T_XSNR_SHDW	Shadow field for REG_T_XSNR. This field is loaded into EMIF_SDRAM_TIM_2[24:16] REG_T_XSNR field when SIdleAck is asserted.	RW	0x0A

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Bits	Field Name	Description	Type	Reset
15:6	REG_T_XSRD_SHDW	Shadow field for REG_T_XSRD. This field is loaded into EMIF_SDRAM_TIM_2[15:6] REG_T_XSRD field when SIdleAck is asserted.	RW	0000001010
5:3	REG_T_RTP_SHDW	Shadow field for REG_T_RTP. This field is loaded into EMIF_SDRAM_TIM_2[5:3] REG_T_RTP field when SIdleAck is asserted.	RW	0x1
2:0	REG_T_CKE_SHDW	Shadow field for REG_T_CKE. This field is loaded into EMIF_SDRAM_TIM_2[2:0] REG_T_CKE field when SIdleAck is asserted.	RW	0x2

Table 15-149. Register Call Summary for Register EMIF_SDRAM_TIM_2_SHDW

EMIF Controller

- Global Initialization: [0]
- Operational Modes Configuration: [1] [2] [3]
- EMIF Register Summary: [4]

Table 15-150. EMIF_SDRAM_TIM_3

Address Offset	0x0000 0028		
Physical Address	0x4C00 0028 0x4D00 0028	**Instance**	EMIF1 EMIF2
Description	SDRAM Timing 3 Register. If this register is byte written, care must be taken that all the fields are written before performing any accesses to the SDRAM.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								REG_T_CKESR			REG_ZQ_ZQCS					REG_T_TDQSCKMAX		RESERVED						REG_T_RFC							
																												REG_T_RAS_MAX			

Bits	Field Name	Description	Type	Reset
31:24	RESERVED	Reserved	R	0x0
23:21	REG_T_CKESR	Minimum number of DDR clock cycles for which LPDDR2 must remain in Self Refresh, minus one.	RW	0x2
20:15	REG_ZQ_ZQCS	Number of DDR clock cycles for a ZQCS command, minus one.	RW	0x08
14:13	REG_T_TDQSCKMAX	Number of DDR clock that satisfies tDQSCKmax for LPDDR2, minus one.	RW	01
12:4	REG_T_RFC	Minimum number of DDR clock cycles from Refresh or Load Mode to Refresh or Activate, minus one.	RW	0x115
3:0	REG_T_RAS_MAX	Maximum number of reg_refresh_rate intervals from Activate to Precharge command. This field must be equal to ((tRASmax / tREFI)-1) rounded down to the next lower integer. Value for REG_T_RAS_MAX can be calculated as follows: If tRASmax = 120 us and tREFI = 15.7 us, then REG_T_RAS_MAX = ((120/15.7)-1) = 6.64. Round down to the next lower integer. Therefore, the programmed value must be 6.	RW	0x1

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Table 15-151. Register Call Summary for Register EMIF_SDRAM_TIM_3

EMIF Controller

- SDRAM Output Impedance Calibration: [0] [1]
- SDRAM Refresh Scheduling: [2]
- Global Initialization: [3] [4] [5]
- Operational Modes Configuration: [6] [7] [8]
- EMIF Register Summary: [9]
- EMIF Register Description: [10] [11] [12] [13] [14] [15]

Table 15-152. EMIF_SDRAM_TIM_3_SHDW

Address Offset	0x0000 002C		
Physical Address	0x4C00 002C 0x4D00 002C	**Instance**	EMIF1 EMIF2
Description	SDRAM Timing 3 Shadow Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								REG_T_CKESR_SHDW			REG_ZQ_ZQCS_SHDW						REG_T_TDQSCKMAX_SHDW		REG_T_RFC_SHDW									REG_T_RAS_MAX_SHDW			

Bits	Field Name	Description	Type	Reset
31:24	RESERVED	Reserved	R	0x0
23:21	REG_T_CKESR_SHDW	Shadow field for reg_t_ckesr. This field is loaded into reg_t_ckesr field in EMIF_SDRAM_TIM_3 register when SIdleAck is asserted.	RW	0x2
20:15	REG_ZQ_ZQCS_SHDW	Shadow field for reg_zq_zqcs. This field is loaded into reg_zq_zqcs field in EMIF_SDRAM_TIM_3 register when SIdleAck is asserted.	RW	0x08
14:13	REG_T_TDQSCKMAX_SHDW	Shadow field for REG_T_TDQSCKMAX. This field is loaded into EMIF_SDRAM_TIM_3[14:13] REG_T_TDQSCKMAX field when SIdleAck is asserted.	RW	0x1
12:4	REG_T_RFC_SHDW	Shadow field for REG_T_RFC. This field is loaded into EMIF_SDRAM_TIM_3[12:4] REG_T_RFC when SIdleAck is asserted.	RW	0x115
3:0	REG_T_RAS_MAX_SHDW	Shadow field for REG_T_RAS_MAX. This field is loaded into EMIF_SDRAM_TIM_3[3:0] REG_T_RAS_MAX field when SIdleAck is asserted.	RW	0x1

Table 15-153. Register Call Summary for Register EMIF_SDRAM_TIM_3_SHDW

EMIF Controller

- Global Initialization: [0]
- Operational Modes Configuration: [1]
- EMIF Register Summary: [2]

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Table 15-154. EMIF_LPDDR2_NVM_TIM

Address Offset	0x0000 0030		
Physical Address	0x4C00 0030 0x4D00 0030	**Instance**	EMIF1 EMIF2
Description	LPDDR2-NVM Timing Register. If this register is byte written, care must be taken that all the fields are written before performing any accesses to the LPDDR2-NVM.		
Type	RW		

31	30 29 28	27	26 25 24	23 22 21 20	19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
RESERVED	REG_NVM_T_XP	RESERVED	REG_NVM_T_WTR	REG_NVM_T_RP	REG_NVM_T_WRA	REG_NVM_T_RRD	REG_NVM_T_RCDMIN

Bits	Field Name	Description	Type	Reset
31	RESERVED	Reserved	R	0
30:28	REG_NVM_T_XP	Minimum number of DDR clock cycles from power-down exit to any command minus one.	RW	0x1
27	RESERVED	Reserved	R	0
26:24	REG_NVM_T_WTR	Minimum number of DDR clock cycles from last Write to Read, minus one.	RW	0x1
23:20	REG_NVM_T_RP	Minimum number of DDR clock cycles from Preactive to Activate, minus one.	RW	0x2
19:16	REG_NVM_T_WRA	Minimum number of DDR clock cycles from last Write transfer to Activate, minus one.	RW	0x2
15:8	REG_NVM_T_RRD	Minimum number of DDR clock cycles from Activate to Activate for a different bank, minus one.	RW	0x0C
7:0	REG_NVM_T_RCDMIN	Minimum number of DDR clock cycles from Activate to Read or Write, minus one.	RW	0x0C

Table 15-155. Register Call Summary for Register EMIF_LPDDR2_NVM_TIM

EMIF Controller

- Global Initialization: [0] [1] [2]
- EMIF Register Summary: [3]
- EMIF Register Description: [4] [5] [6] [7] [8] [9]

Table 15-156. EMIF_LPDDR2_NVM_TIM_SHDW

Address Offset	0x0000 0034		
Physical Address	0x4C00 0034 0x4D00 0034	**Instance**	EMIF1 EMIF2
Description	LPDDR2-NVM Timing Shadow Register		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	REG_NVM_T_XP_SHDW			RESERVED	REG_NVM_T_WTR_SHDW			REG_NVM_T_RP_SHDW				REG_NVM_T_WRA_SHDW				REG_NVM_T_RRD_SHDW								REG_NVM_T_RCDMIN_SHDW							

Bits	Field Name	Description	Type	Reset
31	RESERVED	Reserved	R	0
30:28	REG_NVM_T_XP_SHDW	Shadow field for REG_NVM_T_XP. This field is loaded into EMIF_LPDDR2_NVM_TIM[30:28] REG_NVM_T_XP field when SIdleAck is asserted.	RW	0x0
27	RESERVED	Reserved	R	0
26:24	REG_NVM_T_WTR_SHDW	Shadow field for REG_NVM_T_WTR. This field is loaded into EMIF_LPDDR2_NVM_TIM[26:24] REG_NVM_T_WTR field when SIdleAck is asserted.	RW	0x0
23:20	REG_NVM_T_RP_SHDW	Shadow field for REG_NVM_T_RP. This field is loaded into EMIF_LPDDR2_NVM_TIM[23:20] REG_NVM_T_RP field when SIdleAck is asserted.	RW	0x0
19:16	REG_NVM_T_WRA_SHDW	Shadow field for REG_NVM_T_WRA. This field is loaded into EMIF_LPDDR2_NVM_TIM[19:16] REG_NVM_T_WRA field when SIdleAck is asserted.	RW	0x0
15:8	REG_NVM_T_RRD_SHDW	Shadow field for REG_NVM_T_RRD. This field is loaded into EMIF_LPDDR2_NVM_TIM[15:8] REG_NVM_T_RRD field when SIdleAck is asserted.	RW	0x00
7:0	REG_NVM_T_RCDMIN_SHDW	Shadow field for . This field is loaded into EMIF_LPDDR2_NVM_TIM[7:0] REG_NVM_T_RCDMIN field when SIdleAck is asserted.	RW	0x00

Table 15-157. Register Call Summary for Register EMIF_LPDDR2_NVM_TIM_SHDW

EMIF Controller

- Global Initialization: [0]
- EMIF Register Summary: [1]

Table 15-158. EMIF_PWR_MGMT_CTRL

Address Offset	0x0000 0038		
Physical Address	0x4C00 0038 0x4D00 0038	**Instance**	EMIF1 EMIF2
Description	Power Management Control Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																REG_PD_TIM				REG_DPD_EN	REG_LP_MODE			REG_SR_TIM				REG_CS_TIM			

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Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	REG_PD_TIM	Power Mangement timer for Power-Down. The EMIF will put the external SDRAM in Power-Down mode after the EMIF is idle for these number of DDR clock cycles and if reg_lp_mode field is set to 4. Set to 0 to immediately enter Power-Down mode. Set to 1 for 16 clocks, set to 2 for 32 clocks, set to 3 for 64 clocks, set to 4 for 128 clocks, set to 5 for 256 clocks, set to 6 for 512 clocks, set to 7 for 1024 clocks, set to 8 for 2048 clocks, set to 9 for 4096 clocks, set to 10 for 8192 clocks, set to 11 for 16384 clocks, set to 12 for 32768 clocks, set to 13 for 65536 clocks, set to 14 for 131072 clocks, and set to 15 for 262144 clocks.	RW	0x0
11	REG_DPD_EN	Deep Power Down enable. Set to 0 for normal operation. Set to 1 to enter deep power-down mode. This mode will override the reg_lp_mode field setting.	RW	0
10:8	REG_LP_MODE	Automatic Power Management enable Set to 1: Reserved Set to 2: Self-refresh mode Set to 4: Power-down mode All other values will disable automatic power management.	RW	0x0
7:4	REG_SR_TIM	Power Mangement timer for Self Refresh. The EMIF will put the external SDRAM in Self Refresh mode after the EMIF is idle for these number of DDR clock cycles and if reg_lp_mode field is set to 2. Set to 0 to immediately enter Self Refresh mode. Set to 1 for 16 clocks, set to 2 for 32 clocks, set to 3 for 64 clocks, set to 4 for 128 clocks, set to 5 for 256 clocks, set to 6 for 512 clocks, set to 7 for 1024 clocks, set to 8 for 2048 clocks, set to 9 for 4096 clocks, set to 10 for 8192 clocks, set to 11 for 16384 clocks, set to 12 for 32768 clocks, set to 13 for 65536 clocks, set to 14 for 131072 clocks, and set to 15 for 262144 clocks.	RW	0x0
3:0	REG_CS_TIM	Power Mangement timer for Clock Stop. The EMIF will put the external SDRAM in Clock Stop mode after the EMIF is idle for these number of DDR clock cycles and if reg_lp_mode field is set to 1. Set to 0 to immediately enter Clock Stop mode. Set to 1 for 16 clocks, set to 2 for 32 clocks, set to 3 for 64 clocks, set to 4 for 128 clocks, set to 5 for 256 clocks, set to 6 for 512 clocks, set to 7 for 1024 clocks, set to 8 for 2048 clocks, set to 9 for 4096 clocks, set to 10 for 8192 clocks, set to 11 for 16384 clocks, set to 12 for 32768 clocks, set to 13 for 65536 clocks, set to 14 for 131072 clocks, and set to 15 for 262144 clocks.	RW	0x0

Table 15-159. Register Call Summary for Register EMIF_PWR_MGMT_CTRL

EMIF Controller

- LPDDR2-SDRAM Power-Down Mode: [0] [1] [2]
- LPDDR2-SDRAM Deep Power-Down Mode: [3] [4] [5] [6] [7]
- LPDDR2-NVM Power-Down Mode: [8] [9] [10]
- LPDDR2-SDRAM Self-Refresh Mode: [11] [12] [13]
- Global Initialization: [14] [15] [16] [17] [18] [19]
- Operational Modes Configuration: [20] [21] [22] [23] [24] [25] [26]
- EMIF Register Summary: [27]

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Table 15-160. EMIF_PWR_MGMT_CTRL_SHDW

Address Offset	0x0000 003C		
Physical Address	0x4C00 003C 0x4D00 003C	**Instance**	EMIF1 EMIF2
Description	Power Management Control Shadow Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																REG_PD_TIM_SHDW				RESERVED				REG_SR_TIM_SHDW				REG_CS_TIM_SHDW			

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	RO	0x0
15 :12	REG_PD_TIM_SHDW	Shadow field for reg_pd_tim. This field is loaded into reg_pd_tim field in Power Management Control register when SIdleAck is asserted.	RW	0x0
11:8	RESERVED	Reserved	RO	0x0
7:4	REG_SR_TIM_SHDW	Shadow field for reg_sr_tim. This field is loaded into reg_sr_tim field in Power Management Control register when SIdleAck is asserted.	RW	0x0
3:0	REG_CS_TIM_SHDW	Shadow field for reg_cs_tim. This field is loaded into reg_cs_tim field in Power Management Control register when SIdleAck is asserted.	RW	0x0

Table 15-161. Register Call Summary for Register EMIF_PWR_MGMT_CTRL_SHDW

EMIF Controller

- Global Initialization: [0] [1]
- EMIF Register Summary: [2]

Table 15-162. EMIF_LPDDR2_MODE_REG_DATA

Address Offset	0x0000 0040		
Physical Address	0x4C00 0040 0x4D00 0040	**Instance**	EMIF1 EMIF2
Description	LPDDR2 Mode Reg Data Register A write to this register will cause a Mode Register write command to be sent to the LPDDR2 device with write data as specified in the REG_VALUE_0 field. The address and chip select are taken from the LPDDR2_MODE_REG_CFG register. A read to this register will cause a Mode Register read command to be sent to the LPDDR2 device. The address and chip select are taken from the LPDDR2_MODE_REG_CFG register. The read data will appear in REG_VALUE_0 field.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								REG_VALUE_0							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Reserved for future use.	R	0x0000000
7:0	REG_VALUE_0	Mode register value.	RW	0x00

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Table 15-163. Register Call Summary for Register EMIF_LPDDR2_MODE_REG_DATA

EMIF Controller

- LPDDR2 SDRAM Initialization: [0]
- Global Initialization: [1] [2]
- Operational Modes Configuration: [3] [4] [5]
- EMIF Register Summary: [6]

Table 15-164. EMIF_LPDDR2_MODE_REG_CFG

Address Offset	0x0000 0050		
Physical Address	0x4C00 0050 0x4D00 0050	**Instance**	EMIF1 EMIF2
Description	LPDDR2 Mode Reg Config Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REG_CS	REG_REFRESH_EN	RESERVED																						REG_ADDRESS							

Bits	Field Name	Description	Type	Reset
31	REG_CS	Chip select to issue mode register command. Set to 0 for CS0 and set to 1 for CS1.	RW	0
30	REG_REFRESH_EN	Refresh Enable after MRW write. If a Mode Data register write occurs with this bit set to 1, the refresh operations will commence.	RW	0x0
29:8	RESERVED	Reserved	R	0x000000
7:0	REG_ADDRESS	Mode register address.	RW	0x00

Table 15-165. Register Call Summary for Register EMIF_LPDDR2_MODE_REG_CFG

EMIF Controller

- LPDDR2 SDRAM Initialization: [0] [1]
- Global Initialization: [2]
- Operational Modes Configuration: [3] [4] [5] [6] [7] [8]
- EMIF Register Summary: [9]

Table 15-166. EMIF_L3_CONFIG

Address Offset	0x0000 0054		
Physical Address	0x4C00 0054 0x4D00 0054	**Instance**	EMIF1 EMIF2
Description	Config Register		
Type	RW		

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31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
RESERVED	REG_SYS_THRESH_MAX	RESERVED	REG_LL_THRESH_MAX	RESERVED	REG_PR_OLD_COUNT

Bits	Field Name	Description	Type	Reset
31:28	RESERVED	Reserved for future use.	R	0x0
27:24	REG_SYS_THRESH_MAX	System L3 Threshold Maximum. The number of commands the system interface can consume in the command FIFO. The value is used to determine when to stop future request, writing a zero will reserve no space for the associated interface. In the event the value is set to zero and a request is seen for that interface, the command FIFO will assume a value of 1. Since the low-latency interface has effectively a higher priority, the only way for the system interface to use all command FIFO entries is to set the REG_LL_THRESH_MAX to zero.	RW	0x7
23:20	REG_MPU_THRESH_MAX	MPU Interface Threshold Maximum. The number of commands the MPU interface can consume in the command FIFO. The value is used to determine when to stop future request, writing a zero will reserve no space for the associated interface. In the event the value is set to zero and a request is seen for that interface, the command FIFO will assume a value of 1.	RW	0x7
19:16	REG_LL_THRESH_MAX	Low-latency L3 Threshold Maximum. The number of commands the low latency interface can consume in the command FIFO. The value is used to determine when to stop future request, writing a zero will reserve no space for the associated interface. In the event the value is set to zero and a request is seen for that interface, the command FIFO will assume a value of 1.	RW	0x7
15:8	RESERVED	Reserved for future use.	R	0x0
7:0	RESERVED	Although this field is reserved, it is still read writable. Values written have no effect on operation of the EMIF4D3.	RW	0xFF

Table 15-167. Register Call Summary for Register EMIF_L3_CONFIG

EMIF Controller

- FIFO Description: [0] [1] [2] [3] [4] [5] [6] [7]
- Global Initialization: [8]
- EMIF Register Summary: [9]

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Table 15-168. EMIF_L3_CFG_VAL_1

Address Offset	0x0000 0058		
Physical Address	0x4C00 0058 0x4D00 0058	**Instance**	EMIF1 EMIF2
Description	Config Value 1 Register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REG_SYS_BUS_WIDTH								REG_LL_BUS_WIDTH								RESERVED								REG_WR_FIFO_DEPTH								REG_CMD_FIFO_DEPTH							

Bits	Field Name	Description	Type	Reset
31:30	REG_SYS_BUS_WIDTH	System L3 data bus width 0 = 32-bit wide, 1 = 64-bit wide, 2 = 128-bit wide, 3 = Reserved	R	0x2
29:28	REG_LL_BUS_WIDTH	Low-latency L3 data bus width 0 = 32-bit wide, 1 = 64-bit wide, 2 = 128-bit wide, 3 = Reserved	R	0x1
27:16	RESERVED	Reserved for future use.	R	0x000
15:8	REG_WR_FIFO_DEPTH	Write Data FIFO depth	R	0x19
7:0	REG_CMD_FIFO_DEPTH	Command FIFO depth	R	0x0A

Table 15-169. Register Call Summary for Register EMIF_L3_CFG_VAL_1

EMIF Controller

- EMIF Register Summary: [0]

Table 15-170. EMIF_L3_CFG_VAL_2

Address Offset	0x0000 005C		
Physical Address	0x4C00 005C 0x4D00 005C	**Instance**	EMIF1 EMIF2
Description	Config Value 2 Register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								REG_RREG_FIFO_DEPTH								REG_RSD_FIFO_DEPTH								REG_RCMD_FIFO_DEPTH							

Bits	Field Name	Description	Type	Reset
31:24	RESERVED	Reserved	R	0x00
23:16	REG_RREG_FIFO_DEPTH	Register Read Data FIFO depth	R	0x04
15:8	REG_RSD_FIFO_DEPTH	SDRAM Read Data FIFO depth	R	0x27
7:0	REG_RCMD_FIFO_DEPTH	Read Command FIFO depth	R	0x27

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Table 15-171. Register Call Summary for Register EMIF_L3_CFG_VAL_2

EMIF Controller

- EMIF Register Summary: [0]

Table 15-172. EMIF_PERF_CNT_1

Address Offset	0x0000 0080		
Physical Address	0x4C00 0080 0x4D00 0080	**Instance**	EMIF1 EMIF2
Description	Performance Counter 1 Register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REG_COUNTER1																															

Bits	Field Name	Description	Type	Reset
31:0	REG_COUNTER1	32-bit counter that can be configured as specified in the Performance Counter Config Register and Performance Counter Master Region Select Register.	R	0x0000 0000

Table 15-173. Register Call Summary for Register EMIF_PERF_CNT_1

EMIF Controller

- Performance Counters Description: [0]
- EMIF Register Summary: [1]

Table 15-174. EMIF_PERF_CNT_2

Address Offset	0x0000 0084		
Physical Address	0x4C00 0084 0x4D00 0084	**Instance**	EMIF1 EMIF2
Description	Performance Counter 2 Register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REG_COUNTER2																															

Bits	Field Name	Description	Type	Reset
31:0	REG_COUNTER2	32-bit counter that can be configured as specified in the Performance Counter Config Register and Performance Counter Master Region Select Register.	R	0x0000 0000

Table 15-175. Register Call Summary for Register EMIF_PERF_CNT_2

EMIF Controller

- Performance Counters Description: [0]
- EMIF Register Summary: [1]

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Table 15-176. EMIF_PERF_CNT_CFG

Address Offset	0x0000 0088		
Physical Address	0x4C00 0088 0x4D00 0088	**Instance**	EMIF1 EMIF2
Description	Performance Counter Config Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REG_CNTR2_MCONNID_EN	REG_CNTR2_REGION_EN	RESERVED										REG_CNTR2_CFG				REG_CNTR1_MCONNID_EN	REG_CNTR1_REGION_EN	RESERVED										REG_CNTR1_CFG			

Bits	Field Name	Description	Type	Reset
31	REG_CNTR2_MCONNID_EN	MConnID filter enable for Performance Counter 2 register.	RW	0
30	REG_CNTR2_REGION_EN	Chip Select filter enable for Performance Counter 2 register.	RW	0
29:20	RESERVED	Reserved for future use	R	0x000
19:16	REG_CNTR2_CFG	Filter configuration for Performance Counter 2. Refer to Table 15-178 for details.	RW	0x1
15	REG_CNTR1_MCONNID_EN	MConnID filter enable for Performance Counter 1 register.	RW	0
14	REG_CNTR1_REGION_EN	Chip Select filter enable for Performance Counter 1 register.	RW	0
13:4	RESERVED	Reserved for future use	R	0x000
3:0	REG_CNTR1_CFG	Filter configuration for Performance Counter 1. Refer to Table 15-178 for details.	RW	0x0

Table 15-177. Register Call Summary for Register EMIF_PERF_CNT_CFG

EMIF Controller

- Performance Counters Description: [0] [1] [2] [3] [4]
- Performance Counters General Examples: [5] [6] [7] [8] [9] [10] [11] [12]
- Global Initialization: [13]
- EMIF Register Summary: [14]

Table 15-178. Performance Counter Filter Configuration

CNTRn_CFG	CNTRn_REGION_EN	CNTRn_MCONNID_EN	Description
0x0	0x0	0x0 or 0x1	Count total SDRAM accesses
0x1	0x0	0x0 or 0x1	Count total SDRAM activates
0x2	0x0 or 0x1	0x0 or 0x1	Count total reads
0x3	0x0 or 0x1	0x0 or 0x1	Count total writes
0x4	0x0	0x0	Count number of EMIF_FCLK clock cycles L3 Command FIFO is full
0x5	0x0	0x0	Count number of EMIF_FCLK clock cycles L3 Write Data FIFO is full
0x6	0x0	0x0	Count number of EMIF_FCLK clock cycles L3 Read Data FIFO is full

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Table 15-178. Performance Counter Filter Configuration (continued)

CNTRn_CFG	CNTRn_REGION_EN	CNTRn_MCONNID_EN	Description
0x7	0x0	0x0	Count number of EMIF_FCLK clock cycles L3 Return Command FIFO is full
0x8	0x0 or 0x1	0x0 or 0x1	Count number of priotity elevations
0x9	0x0	0x0	Count number of EMIF_FCLK clock cycles that a command was pending
0xA	0x0	0x0	Count number of EMIF_FCLK clock cycles for which the memory data bus was transferring data.
0xB - 0xF	0x0	0x0	Reserved for future use.

NOTE: When MReqDebug is set to a 1 for a particular L3 command, the performance counters will not be incremented for that particular command if the CNTRn_CFG values are equal 0x0, 0x1, 0x2, 0x3, or 0xA.

Table 15-178 shows the possible filter configurations for the two performance counters. These filter configurations can be used in conjunction with a L3 master ID and/or an external chip select to obtain performance statistics for a particular L3 master and/or an external chip select.

The EMIF clock frequency is half the DDR speed.

Table 15-179. EMIF_PERF_CNT_SEL

Address Offset	0x0000 008C		
Physical Address	0x4C00 008C 0x4D00 008C	**Instance**	EMIF1 EMIF2
Description	Performance Counter Master Region Select Register		
Type	RW		

31 30 29 28 27 26 25 24	23 22 21 20 19 18	17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2	1 0
REG_MCONNID2	RESERVED	REG_REGION_SEL2	REG_MCONNID1	RESERVED	REG_REGION_SEL1

Bits	Field Name	Description	Type	Reset
31:24	REG_MCONNID2	MConnID for Performance Counter 2 register.	RW	0x00
23:18	RESERVED	Reserved for future use.	R	0x00
17:16	REG_REGION_SEL2	MAddrSpace for Performance Counter 2 register.	RW	0x0
15:8	REG_MCONNID1	MConnID for Performance Counter 1 register.	RW	0x00
7:2	RESERVED	Reserved for future use.	R	0x00
1:0	REG_REGION_SEL1	MAddrSpace for Performance Counter 1 register.	RW	0x0

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Table 15-180. Register Call Summary for Register EMIF_PERF_CNT_SEL

EMIF Controller

- Performance Counters Description: [0]
- Performance Counters General Examples: [1] [2] [3]
- Global Initialization: [4]
- EMIF Register Summary: [5]

NOTE: The values programmed into the REG_MCONNIDx fields are those in Table 28-27, ConnID Mapping (Debug View), in Chapter 28, On-Chip Debug Support, left shifted by 2 bits. For example, to monitor accesses from the dual Cortex-M3 MPU subsystem (ConnID = 0x11), the value 0x44 is programmed into the REG_MCONNIDx field.

Table 15-181. EMIF_PERF_CNT_TIM

Address Offset	0x0000 0090		
Physical Address	0x4C00 0090 0x4D00 0090	**Instance**	EMIF1 EMIF2
Description	Performance Counter Time Register. This is a free running counter.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REG_TOTAL_TIME																															

Bits	Field Name	Description	Type	Reset
31:0	REG_TOTAL_TIME	32-bit counter that continuously counts number for EMIF_FCLK clock cycles elapsed after EMIF is brought out of reset.	R	0x0000 0000

Table 15-182. Register Call Summary for Register EMIF_PERF_CNT_TIM

EMIF Controller

- EMIF Register Summary: [0]

Table 15-183. EMIF_READ_IDLE_CTRL

Address Offset	0x0000 0098		
Physical Address	0x4C00 0098 0x4D00 0098	**Instance**	EMIF1 EMIF2
Description	Read Idle Control Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												REG_READ_IDLE_LEN				RESERVED								REG_READ_IDLE_INTERVAL							

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Bits	Field Name	Description	Type	Reset
31:20	RESERVED	Reserved for future use.	R	0x0
19:16	REG_READ_IDLE_LEN	The Read Idle Length field determines the minimum required size that a read idle window must be to be detected or generated. The actual read idle length will be (REG_READ_IDLE_LEN+1)*2 EMIF_FCLK clocks. The value programmed should be (the required read idle length minus one) divided by two.	RW	0x5
15:9	RESERVED	Reserved for future use.	R	0x0
8:0	REG_READ_IDLE_INTERVAL	The Read Idle Interval field determines the maximum interval between successive read idle events. The actual interval between read idle events is (REG_READ_IDLE_INTERVAL+1)*64 EMIF_FCLK clocks. The value programmed should be (the required max interval divided by sixty four) minus one. A value of 0 disables the read idle function.	RW	0x0

Table 15-184. Register Call Summary for Register EMIF_READ_IDLE_CTRL

EMIF Controller

- Read Idle Window: [0] [1] [2]
- Global Initialization: [3] [4] [5] [6]
- EMIF Register Summary: [7]
- EMIF Register Description: [8] [9]

Table 15-185. EMIF_READ_IDLE_CTRL_SHDW

Address Offset	0x0000 009C		
Physical Address	0x4C00 009C 0x4D00 009C	**Instance**	EMIF1 EMIF2
Description	Read Idle Control Shadow Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												REG_READ_IDLE_LEN_SHDW				RESERVED								REG_READ_IDLE_INTERVAL_SHDW							

Bits	Field Name	Description	Type	Reset
31:20	RESERVED	Reserved for future use.	R	0x0
19:16	REG_READ_IDLE_LEN_SHDW	Shadow field for REG_READ_IDLE_LEN. This field is loaded into EMIF_READ_IDLE_CTRL[19:16] REG_READ_IDLE_LEN field when SIdleAck is asserted.	RW	0x5
15:9	RESERVED	Reserved for future use.	R	0x0
8:0	REG_READ_IDLE_INTERVAL_SHDW	Shadow field for REG_READ_IDLE_INTERVAL. This field is loaded into EMIF_READ_IDLE_CTRL[8:0] REG_READ_IDLE_INTERVAL field when SIdleAck is asserted.	RW	0x0

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Table 15-186. Register Call Summary for Register EMIF_READ_IDLE_CTRL_SHDW

EMIF Controller

- Global Initialization: [0]
- EMIF Register Summary: [1]

Table 15-187. EMIF_IRQSTATUS_RAW_SYS

Address Offset	0x0000 00A4		
Physical Address	0x4C00 00A4 0x4D00 00A4	**Instance**	EMIF1 EMIF2
Description	System L3 Interrupt Raw Status Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													REG_DNV_SYS	REG_TA_SYS	REG_ERR_SYS

Bits	Field Name	Description	Type	Reset
31:3	RESERVED	Reserved for future use.	R	0x0000 0000
2	REG_DNV_SYS	Raw status of system L3 interrupt for LPDDR2 NVM data not valid. Write 1 to set the (raw) status, typically for debug. Writing 0 has no effect.	RW	0
1	REG_TA_SYS	Raw status of system L3 interrupt for SDRAM temperature alert. Write 1 to set the (raw) status, mostly for debug. Writing a 0 has no effect.	RW	0
0	REG_ERR_SYS	Raw status of system L3 interrupt for command or address error. Write 1 to set the (raw) status, mostly for debug. Writing a 0 has no effect.	RW	0

Table 15-188. Register Call Summary for Register EMIF_IRQSTATUS_RAW_SYS

EMIF Controller

- Interrupt Requests: [0] [1] [2] [3]
- Global Initialization: [4]
- EMIF Events Servicing: [5] [6] [7] [8] [9] [10]
- EMIF Register Summary: [11]

Table 15-189. EMIF_IRQSTATUS_RAW_LL

Address Offset	0x0000 00A8		
Physical Address	0x4C00 00A8 0x4D00 00A8	**Instance**	EMIF1 EMIF2
Description	Low-Latency L3 Interrupt Raw Status Register		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													REG_DNV_LL	REG_TA_LL	REG_ERR_LL

Bits	Field Name	Description	Type	Reset
31:3	RESERVED	Reserved for future use.	R	0x0000 0000
2	REG_DNV_LL	Raw status of low-latency L3 interrupt for LPDDR2 NVM data not valid. Write 1 to set the (raw) status, typically for debug. Writing 0 has no effect.	RW	0
1	REG_TA_LL	Raw status of low-latency L3 interrupt or SDRAM temperature alert. Write 1 to set the (raw) status, mostly for debug. Writing a 0 has no effect.	RW	0
0	REG_ERR_LL	Raw status of low-latency L3 interrupt for command or address error. Write 1 to set the (raw) status, mostly for debug. Writing a 0 has no effect.	RW	0

Table 15-190. Register Call Summary for Register EMIF_IRQSTATUS_RAW_LL

EMIF Controller

- Interrupt Requests: [0] [1] [2] [3]
- Global Initialization: [4]
- EMIF Events Servicing: [5] [6] [7] [8] [9] [10]
- EMIF Register Summary: [11]

Table 15-191. EMIF_IRQSTATUS_SYS

Address Offset	0x0000 00AC		
Physical Address	0x4C00 00AC 0x4D00 00AC	**Instance**	EMIF1 EMIF2
Description	System L3 Interrupt Status Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													REG_DNV_SYS	REG_TA_SYS	REG_ERR_SYS

Bits	Field Name	Description	Type	Reset
31:3	RESERVED	Reserved for future use.	R	0x0000 0000
2	REG_DNV_SYS	Enabled status of system L3 interrupt for LPDDR2 NVM data not valid. Write 1 to clear the status after interrupt is serviced (raw status is cleared; that is, even if not enabled). Writing 0 has no effect.	RW	0
1	REG_TA_SYS	Enabled status of system L3 interrupt for SDRAM temperature alert. Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, that is, even if not enabled). Writing a 0 has no effect.	RW	0

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Bits	Field Name	Description	Type	Reset
0	REG_ERR_SYS	Enabled status of system L3 interrupt interrupt for command or address error. Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, that is, even if not enabled). Writing a 0 has no effect.	RW	0

Table 15-192. Register Call Summary for Register EMIF_IRQSTATUS_SYS

EMIF Controller

- Interrupt Requests: [0] [1] [2]
- SDRAM Temperature Monitoring: [3]
- Global Initialization: [4]
- EMIF Events Servicing: [5] [6] [7] [8] [9] [10]
- EMIF Register Summary: [11]

Table 15-193. EMIF_IRQSTATUS_LL

Address Offset	0x0000 00B0		
Physical Address	0x4C00 00B0 0x4D00 00B0	**Instance**	EMIF1 EMIF2
Description	Low-Latency L3 Interrupt Status Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													REG_DNV_LL	REG_TA_LL	REG_ERR_LL

Bits	Field Name	Description	Type	Reset
31:3	RESERVED	Reserved for future use.	R	0x0000 0000
2	REG_DNV_LL	Enabled status of low-latency L3 interrupt for LPDDR2 NVM data not valid. Write 1 to clear the status after interrupt is serviced (raw status is cleared; that is, even if not enabled). Writing 0 has no effect.	RW W1toClr	0
1	REG_TA_LL	Enabled status of low-latency L3 interrupt for SDRAM temperature alert. Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, that is, even if not enabled). Writing a 0 has no effect.	RW W1toClr	0
0	REG_ERR_LL	Enabled status of low-latency L3 interrupt for command or address error. Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, that is, even if not enabled). Writing a 0 has no effect.	RW W1toClr	0

Table 15-194. Register Call Summary for Register EMIF_IRQSTATUS_LL

EMIF Controller

- Interrupt Requests: [0] [1] [2]
- SDRAM Temperature Monitoring: [3]
- Global Initialization: [4]
- EMIF Events Servicing: [5] [6] [7] [8] [9] [10]
- EMIF Register Summary: [11]

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Table 15-195. EMIF_IRQENABLE_SET_SYS

Address Offset	0x0000 00B4		
Physical Address	0x4C00 00B4 0x4D00 00B4	**Instance**	EMIF1 EMIF2
Description	System L3 Interrupt Enable Set Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													REG_EN_DNV_SYS	REG_EN_TA_SYS	REG_EN_ERR_SYS

Bits	Field Name	Description	Type	Reset
31:3	RESERVED	Reserved for future use.	R	0x0000 0000
2	REG_EN_DNV_SYS	Enable set for system L3 interrupt for LPDDR2 NVM data not valid. Writing 1 enables the interrupt and sets this bit and the corresponding Interrupt-enable clear register. Writing 0 has no effect.	RW W1toSet	0
1	REG_EN_TA_SYS	Enable set for system L3 interrupt for SDRAM temperature alert. . Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect.	RW W1toSet	0
0	REG_EN_ERR_SYS	Enable set for system L3 interrupt for command or address error. Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect.	RW W1toSet	0

Table 15-196. Register Call Summary for Register EMIF_IRQENABLE_SET_SYS

EMIF Controller

- Interrupt Requests: [0] [1]
- Global Initialization: [2]
- Operational Modes Configuration: [3]
- EMIF Events Servicing: [4]
- EMIF Register Summary: [5]

Table 15-197. EMIF_IRQENABLE_SET_LL

Address Offset	0x0000 00B8		
Physical Address	0x4C00 00B8 0x4D00 00B8	**Instance**	EMIF1 EMIF2
Description	Low-Latency L3 Interrupt Enable Set Register		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													REG_EN_DNV_LL	REG_EN_TA_LL	REG_EN_ERR_LL

Bits	Field Name	Description	Type	Reset
31:3	RESERVED	Reserved for future use.	R	0x0000 0000
2	REG_EN_DNV_LL	Enable set for low-latency L3 interrupt for LPDDR2 NVM data not valid. Writing 1 enables the interrupt and sets this bit and the corresponding Interrupt-enable clear register. Writing a 0 has no effect.	RW W1toSet	0
1	REG_EN_TA_LL	Enable set for low-latency L3 interrupt for SDRAM temperature alert. Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect.	RW W1toSet	0
0	REG_EN_ERR_LL	Enable set for low-latency L3 interrupt for command or address error. Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect.	RW W1toSet	0

Table 15-198. Register Call Summary for Register EMIF_IRQENABLE_SET_LL

EMIF Controller

- Interrupt Requests: [0] [1]
- Global Initialization: [2]
- Operational Modes Configuration: [3]
- EMIF Events Servicing: [4]
- EMIF Register Summary: [5]

Table 15-199. EMIF_IRQENABLE_CLR_SYS

Address Offset	0x0000 00BC		
Physical Address	0x4C00 00BC 0x4D00 00BC	**Instance**	EMIF1 EMIF2
Description	System L3 Interrupt Enable Clear Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													REG_EN_DNV_SYS	REG_EN_TA_SYS	REG_EN_ERR_SYS

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Bits	Field Name	Description	Type	Reset
31:3	RESERVED	Reserved for future use	R	0x0000 0000
2	REG_EN_DNV_SYS	Enable clear for system OCP interrupt for LPDDR2 NVM data not valid. Writing 1 disables the interrupt and clears this bit and the corresponding interrupt-enable set register. Writing 0 has no effect.	RW W1toClr	0
1	REG_EN_TA_SYS	Enable clear for system L3 interrupt for SDRAM temperature alert. Writing a 1 will disable the interrupt, and clear this bit as well as the corresponding Interrupt Enable Set Register. Writing a 0 has no effect.	RW W1toClr	0
0	REG_EN_ERR_SYS	Enable clear for system L3 interrupt for command or address error. Writing a 1 will disable the interrupt, and clear this bit as well as the corresponding Interrupt Enable Set Register. Writing a 0 has no effect.	RW W1toClr	0

Table 15-200. Register Call Summary for Register EMIF_IRQENABLE_CLR_SYS

EMIF Controller

- Interrupt Requests: [0] [1]
- EMIF Events Servicing: [2] [3]
- EMIF Register Summary: [4]

Table 15-201. EMIF_IRQENABLE_CLR_LL

Address Offset	0x0000 00C0		
Physical Address	0x4C00 00C0 0x4D00 00C0	**Instance**	EMIF1 EMIF2
Description	Low-Latency L3 Interrupt Enable Clear Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													REG_EN_DNV_LL	REG_EN_TA_LL	REG_EN_ERR_LL

Bits	Field Name	Description	Type	Reset
31:3	RESERVED	Reserved for future use.	R	0x0000 0000
2	REG_EN_DNV_LL	Enable clear for low-latency OCP interrupt for LPDDR2 NVM data not valid. Writing 1 disables the interrupt and clears this bit and the corresponding interrupt enable set register. Writing 0 has no effect.	RW W1toClr	0
1	REG_EN_TA_LL	Enable clear for low-latency L3 interrupt for SDRAM temperature alert. Writing a 1 will disable the interrupt, and clear this bit as well as the corresponding Interrupt Enable Set Register. Writing a 0 has no effect.	RW W1toClr	0
0	REG_EN_ERR_LL	Enable clear for low-latency L3 interrupt for command or address error. Writing a 1 will disable the interrupt, and clear this bit as well as the corresponding Interrupt Enable Set Register. Writing a 0 has no effect.	RW W1toClr	0

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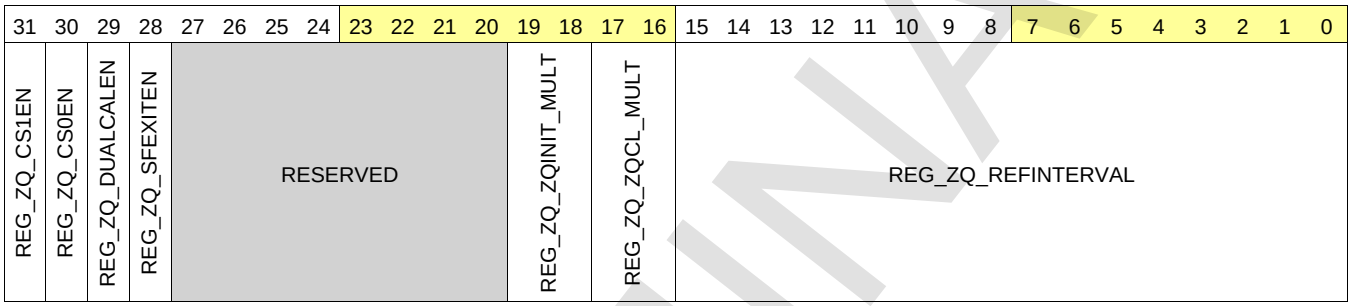
Table 15-202. Register Call Summary for Register EMIF_IRQENABLE_CLR_LL

EMIF Controller

- Interrupt Requests: [0] [1]
- EMIF Events Servicing: [2] [3]
- EMIF Register Summary: [4]

Table 15-203. EMIF_ZQ_CONFIG

Address Offset	0x0000 00C8		
Physical Address	0x4C00 00C8 0x4D00 00C8	**Instance**	EMIF1 EMIF2
Description	SDRAM Output Impedance Calibration Config Register		
Type	RW		



Bits	Field Name	Description	Type	Reset
31	REG_ZQ_CS1EN	Writing a 1 enables ZQ calibration for CS1.	RW	0x0
30	REG_ZQ_CS0EN	Writing a 1 enables ZQ calibration for CS0.	RW	0x0
29	REG_ZQ_DUALCALEN	ZQ Dual Calibration enable. Allows both ranks to be ZQ calibrated simultaneously. Setting this bit requires both chip selects to have a separate calibration resistor per device.	RW	0x0
28	REG_ZQ_SFEXITEN	ZQCL on Self-Refresh, Active Power-Down, and Precharge Power-Down exit enable. Writing a 1 enables the issuing of ZQCL on Self-Refresh, Active Power-Down, and Precharge Power-Down exit.	RW	0x0
27:20	RESERVED	Reserved	R	0x00
19:18	REG_ZQ_ZQINIT_MULT	Indicates the number of ZQCL intervals that make up a ZQINIT interval, minus one..	RW	0x0
17:16	REG_ZQ_ZQCL_MULT	Indicates the number of ZQCS intervals that make up a ZQCL interval, minus one. ZQCS interval is defined by reg_zq_zqcs in EMIF_SDRAM_TIM_3.	RW	0x0
15:0	REG_ZQ_REFINTERVAL	Number of refresh periods between ZQCS commands. This field supports between one refresh period to 256 ms between ZQCS calibration commands. Refresh period is defined by reg_refresh_rate in EMIF_SDRAM_REF_CTRL register.	RW	0x0000

Table 15-204. Register Call Summary for Register EMIF_ZQ_CONFIG

EMIF Controller

- SDRAM Output Impedance Calibration: [0] [1] [2] [3] [4] [5]
- Operational Modes Configuration: [6] [7] [8] [9] [10] [11]
- EMIF Register Summary: [12]

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Table 15-205. EMIF_TEMP_ALERT_CONFIG

Address Offset	0x0000 00CC		
Physical Address	0x4C00 00CC 0x4D00 00CC	**Instance**	EMIF1 EMIF2
Description	Temperature Alert Config Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REG_TA_CS1EN	REG_TA_CS0EN	RESERVED	REG_TA_SFEXITEN	REG_TA_DEVWDT		REG_TA_DEVCNT		RESERVED		REG_TA_REFINTERVAL																					

Bits	Field Name	Description	Type	Reset
31	REG_TA_CS1EN	Writing a 1 enables temperature alert polling for CS1.	RW	0x0
30	REG_TA_CS0EN	Writing a 1 enables temperature alert polling for CS0.	RW	0x0
29	RESERVED	Reserved	R	0x0
28	REG_TA_SFEXITEN	Temperature Alert Poll on Self-Refresh, Active Power-Down, and Precharge Power-Down exit enable. Writing a 1 enables the issuing of a temperature alert poll on Self-Refresh exit.	RW	0x0
27:26	REG_TA_DEVWDT	This field indicates how wide a physical device is. It is used in conjunction with the reg_ta_devcnt register to determine which byte lanes contain the temperature alert info. A value of 0 = eight bit wide, 1 = sixteen bit wide, 2 = thirty two bit wide. All others are reserved. If this field is set to 1 and the reg_ta_devcnt field is set to one the byte mask for checking will be 4'b0101.	RW	0x0
25:24	REG_TA_DEVCNT	This field indicates which external byte lanes contain a device for temperature monitoring. A value of 0 = one device, 1 = two devices, 2 = four devices. All other reserved.	RW	0x0
23:22	RESERVED	Reserved	R	0x0
21:0	REG_TA_REFINTERVAL	Number of refresh periods between temperature alert polls. This field supports between one refresh period to 10 seconds between temperature alert polls. Refresh period is defined by reg_refresh_rate in SDRAM Refresh Control register.	RW	0x000000

Table 15-206. Register Call Summary for Register EMIF_TEMP_ALERT_CONFIG

EMIF Controller

- SDRAM Temperature Monitoring: [0] [1] [2] [3] [4] [5]
- Global Initialization: [6]
- Operational Modes Configuration: [7] [8] [9] [10] [11]
- EMIF Register Summary: [12]

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Table 15-207. EMIF_L3_ERR_LOG

Address Offset	0x0000 00D0		
Physical Address	0x4C00 00D0 0x4D00 00D0	**Instance**	EMIF1 EMIF2
Description	Error Log Register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																REG_MADDRSPACE		REG_MBURSTSEQ			REG_MCMD			REG_MCONNID							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved for future use.	R	0x0000
15:14	REG_MADDRSPACE	Address space of the first errored transaction. 0x0: SDRAM 0x1: LPDDR2-NVM 0x2: reserved 0x3: internal registers	R	0x0
13:11	REG_MBURSTSEQ	Addressing mode of the first errored transaction. (see Chapter 13, *Interconnect* for more information)	R	0x0
10:8	REG_MCMD	Command type of the first errored transaction. (see Chapter 13, *Interconnect* for more information)	R	0x0
7:0	REG_MCONNID	Connection ID of the first errored transaction.	R	0x00

Table 15-208. Register Call Summary for Register EMIF_L3_ERR_LOG

EMIF Controller

- EMIF Events Servicing: [0] [1] [2] [3] [4] [5] [6] [7]
- EMIF Register Summary: [8]

Table 15-209. EMIF_DDR_PHY_CTRL_1

Address Offset	0x0000 00E4		
Physical Address	0x4C00 00E4 0x4D00 00E4	**Instance**	EMIF1 EMIF2
Description	DDR PHY Control 1 Register. This register is used to control the DDR PHY. The bit field definitions are DDR PHY specific.		
Type	RW		

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31 30	29 28 27 26	25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
DLL_MASTER_SENSITIVITY	REG_PHY_FREEZE_DELAY_CODE_POSTAMBLE	REG_PHY_FREEZE_DELAY_CODE_PREAMBLE	REG_DLL_MASTER_SW_CODE_CTRL	REG_DLL_SLAVE_DLY_CTRL	REG_READ_LATENCY

Bits	Field Name	Description	Type	Reset
31:30	DLL_MASTER_SENSITIVITY	This field defines the level of sensitivity of the DLL master: the lower the value, the more sensitive the DLL is to PVT variation. The recommended setting is 0x2.	RW	0x0
29:26	REG_PHY_FREEZE_DELAY_CODE_POSTAMBLE	Postamble time respected by the DATA PHY freezing the DLL slave code after reads	RW	0x0
25:22	REG_PHY_FREEZE_DELAY_CODE_PREAMBLE	Preamble time respected by the DATA PHY before freezing the DLL slave code during reads	RW	0x0
21:12	REG_DLL_MASTER_SW_CODE_CTRL	DLL delay code when in software override mode	RW	0x1FF
11:4	REG_DLL_SLAVE_DLY_CTRL	DLL slave delay ratio control	RW	0xFF
3:0	REG_READ_LATENCY	This field defines the read latency for the read data from SDRAM in number of DDR clock cycles. This field is used by the EMIF as well as the PHY. The EMIF will expect the first read data to arrive (reg_read_latency + 3) DDR clock cycles from the read command. The reg_read_latency must be set to RL + tDQSCKmax (the actual value programmed in the EMIF registers, including the minus 1). See the LPDDR SDRAM standard.	RW	0x0

Table 15-210. Register Call Summary for Register EMIF_DDR_PHY_CTRL_1

EMIF Controller

- SDRAM Read: [0]
- Global Initialization: [1] [2]
- Operational Modes Configuration: [3]
- EMIF Register Summary: [4]
- EMIF Register Description: [5] [6]

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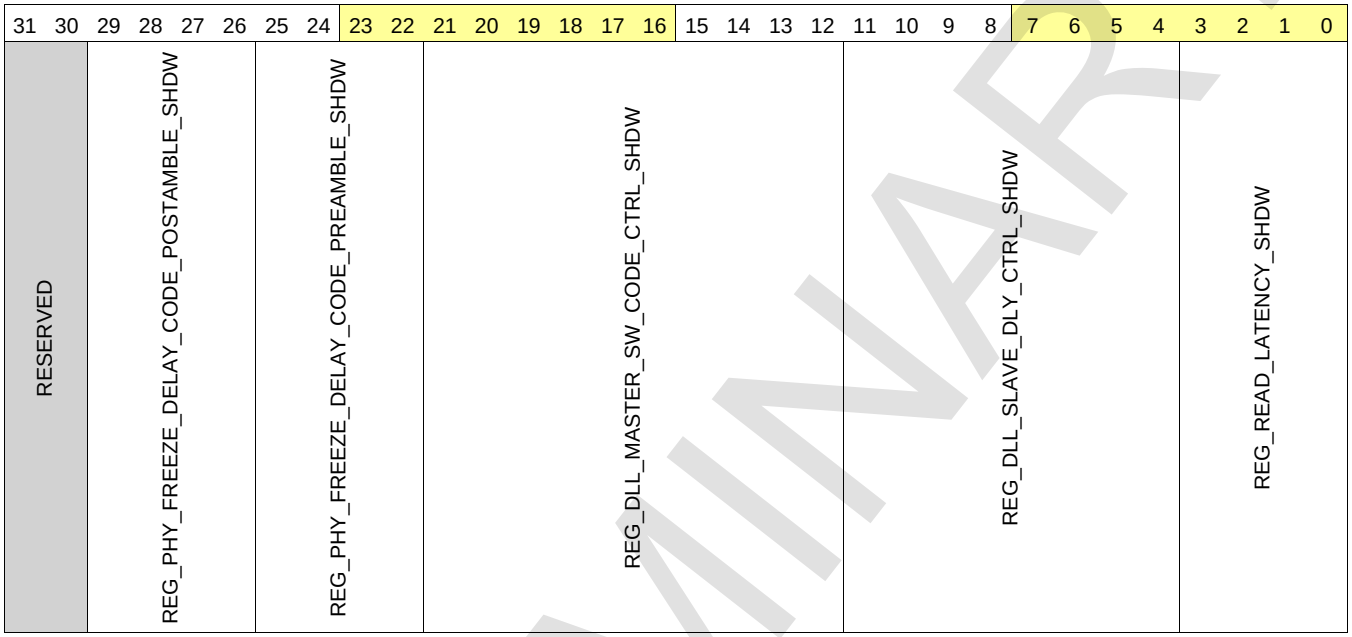
Table 15-211. EMIF_DDR_PHY_CTRL_1_SHDW

Address Offset	0x0000 00E8		
Physical Address	0x4C00 00E8 0x4D00 00E8	**Instance**	EMIF1 EMIF2
Description	DDR PHY Control 1 Shadow Register. Shadow field for EMIF_DDR_PHY_CTRL_1.		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:30	RESERVED	Reserved	RW	0x0
29:26	REG_PHY_FREEZE_DELAY_CODE_POSTAMBLE_SHDW	Shadow field for REG_PHY_FREEZE_DELAY_CODE_POSTAMBLE	RW	0x0
25:22	REG_PHY_FREEZE_DELAY_CODE_PREAMBLE_SHDW	Shadow field for REG_PHY_FREEZE_DELAY_CODE_PREAMBLE	RW	0x0
21:12	REG_DLL_MASTER_SW_CODE_CTRL_SHDW	Shadow field for REG_DLL_MASTER_SW_CODE_CTRL	RW	0x1FF
11:4	REG_DLL_SLAVE_DLY_CTRL_SHDW	Shadow field for REG_DLL_SLAVE_DLY_CTRL	RW	0xFF
3:0	REG_READ_LATENCY_SHDW	Shadow field for REG_READ_LATENCY. This field is loaded into EMIF_DDR_PHY_CTRL_1[3:0] REG_READ_LATENCY field when SIdleAck is asserted.	RW	0x0

Table 15-212. Register Call Summary for Register EMIF_DDR_PHY_CTRL_1_SHDW

EMIF Controller

- Global Initialization: [0]
- EMIF Register Summary: [1]

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Table 15-213. EMIF_DDR_PHY_CTRL_2

Address Offset	0x0000 00EC		
Physical Address	0x4C00 00EC 0x4D00 00EC	**Instance**	EMIF1 EMIF2
Description	DDR PHY Control 2 Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REG_DDR_PHY_CTRL_2																															

Bits	Field Name	Description	Type	Reset
31:0	REG_DDR_PHY_CTRL_2	This register is used to control the DDR PHY. The bit field definitions are DDR PHY specific.	RW	0x0000 0000

Table 15-214. Register Call Summary for Register EMIF_DDR_PHY_CTRL_2

EMIF Controller

- Global Initialization: [0]
- EMIF Register Summary: [1]

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15.4 General-Purpose Memory Controller

15.4.1 GPMC Overview

The general-purpose memory controller (GPMC) is an unified memory controller dedicated to interfacing external memory devices:

- Asynchronous SRAM-like memories and application-specific integrated circuit (ASIC) devices
- Asynchronous, synchronous, and page mode (only available in non-muxed mode) burst NOR flash devices
- NAND Flash
- Pseudo-SRAM devices

15.4.2 GPMC Environment

This section describes the GPMC application fields from an environment point of view (external connections). It describes GPMC connectivity options, and gives three possible interfaces.

15.4.2.1 GPMC Modes

This section shows three GPMC external connections options:

- Figure 15-50 shows a connection between the GPMC and a 16-bit synchronous address/data-multiplexed (or AAD-multiplexed, but this protocol use less address pins) external memory device (Figure 15-50).
- Figure 15-50 shows a connection between the GPMC and a 16-bit synchronous nonmultiplexed external memory device (Figure 15-51).
- Figure 15-52 shows a connection between the GPMC and a 16-bit NAND device (Figure 15-52).

NOTE: The device does not provide the A0 byte address line required for random-byte addressable 8-bit wide device interfacing (for multiplexed and nonmultiplexed protocol). Hence, an 8-bit device must be connected to the D[7:0] / gpmc_ad[7:0] data bus (rather than D[15:8] / gpmc_ad[15:8]) of the GPMC controller. This limits the use of 8-bit wide device interfacing to byte-alias access.

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Figure 15-50. GPMC to 16-Bit Address/Data-Multiplexed Memory

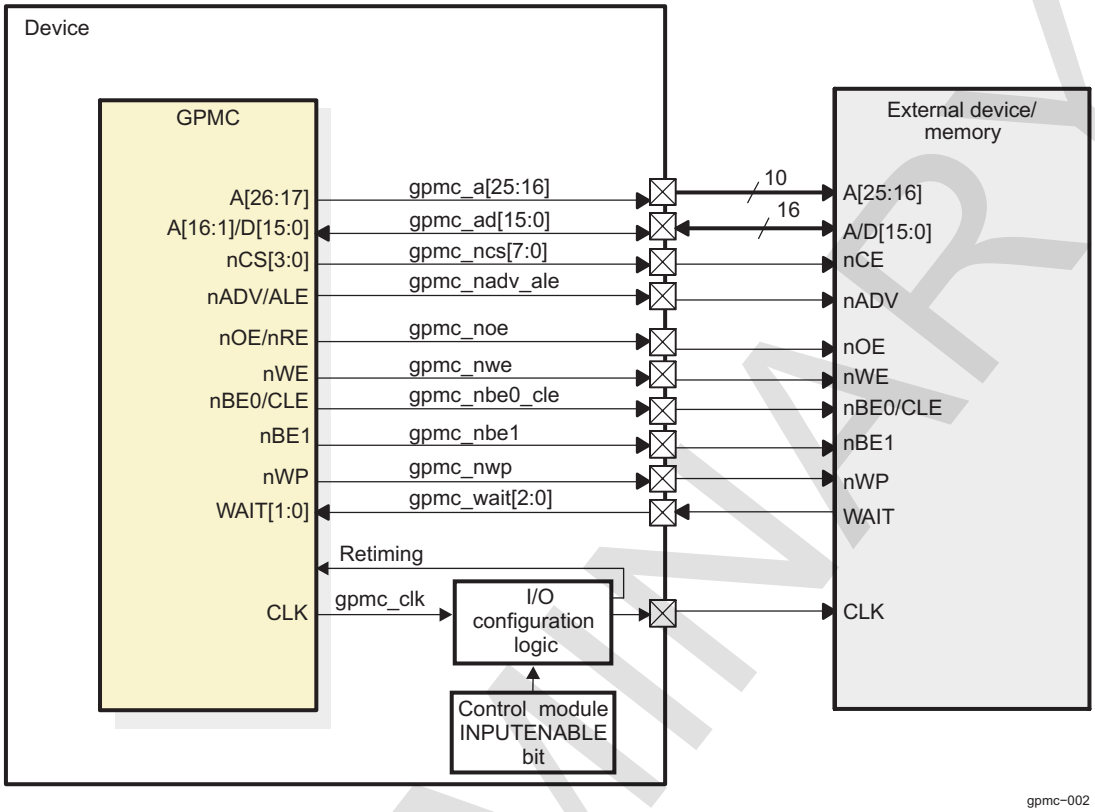

Figure 15-51. GPMC to 16-Bit Nonmultiplexed Memory

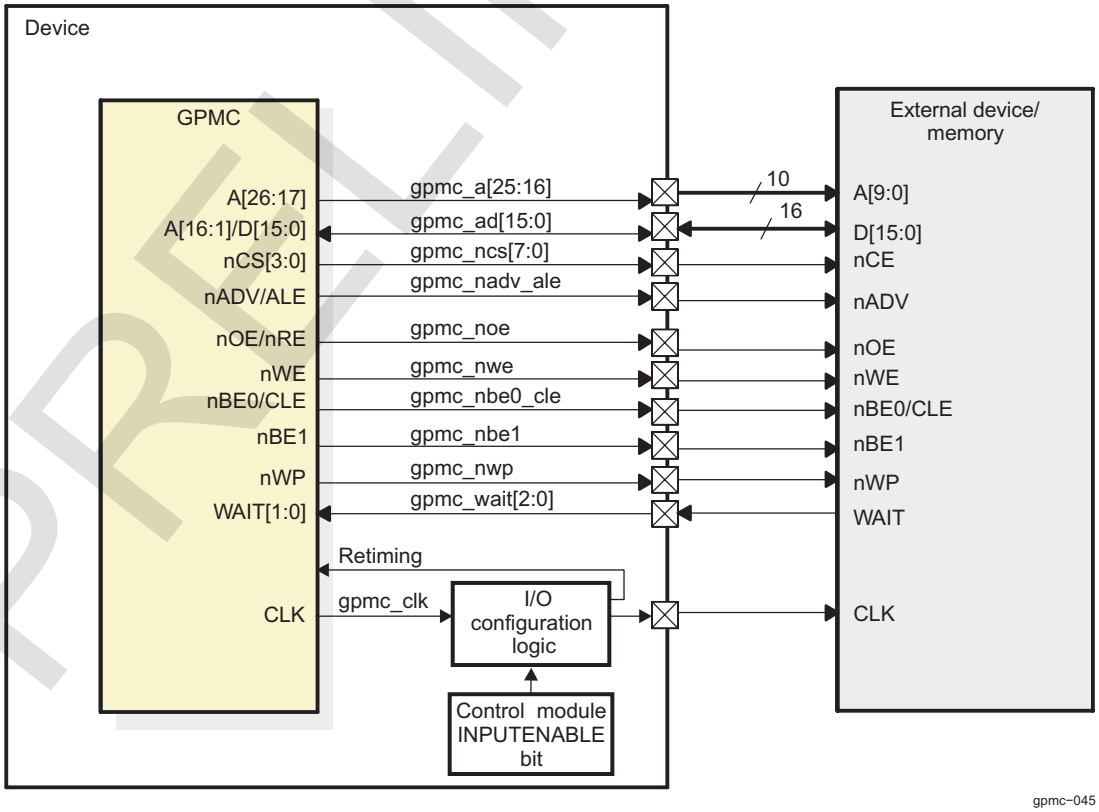

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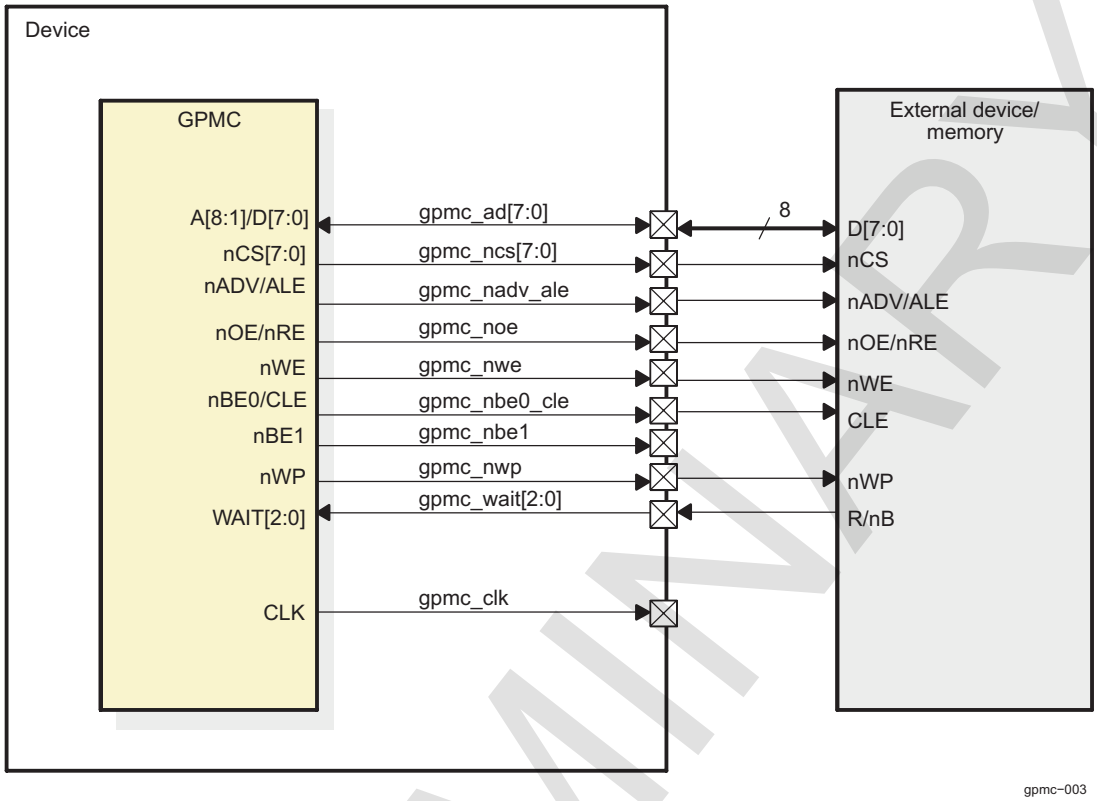
Figure 15-52. GPMC to 8-Bit NAND Device



15.4.2.2 GPMC Signals

Table 15-215 lists the GPMC subsystem I/O pins.

Table 15-215. GPMC I/O Description

Pin Name	I/O	Description
gpmc_a[25:16]	O	Address
gpmc_ad[15:0]	I/O	Data
gpmc_ncs[7:0]	O	Chip-selects (active low)
gpmc_clk	O[(1)]	Clock generated for the external memory or device
gpmc_nadv_ale	O	Address valid (active low). Also used as address latch enable (active high) for NAND protocol memories.
gpmc_noe_nre	O	Output enable (active low). Also used as read enable (active low) for NAND protocol memories.
gpmc_nwe	O	Write enable (active low)
gpmc_nbe0_cle	O	Lower-byte enable (active low). Also used as command latch enable for NAND protocol memories.
gpmc_nbe1	O	Upper-byte enable (active low).
gpmc_nwp	O	Write protect (active low)
gpmc_wait[2:0]	I	External wait signal for NOR and NAND protocol memories. The wait signals can be mapped on any of the chip-select.
gpmc_io_dir	O	gpmc_ad[15:0] signal direction control: Low during transmit (for write access: data OUT from GPMC to memory), High during receive (for read access: data IN from memory to GPMC)

(1) This output signal is also used as retiming input (the INPUTENABLE bit in the corresponding pad configuration register must be set to 1).

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Table 15-216 shows the use of address and data GPMC controller pins based on the type of external device.

Table 15-216. GPMC Pin Multiplexing Options

GPMC Pin	Multiplexed Address Data 16-Bit Device	Nonmultiplexed Address Data 16-Bit Device With LIMITED-ADDRESS Bit Enabled	16-Bit NAND Device	8-Bit NAND Device
gpmc_a[25]	A26	A10	Not used	Not used
gpmc_a[24]	A25	A9	Not used	Not used
gpmc_a[23]	A24	A8	Not used	Not used
gpmc_a[22]	A23	A7	Not used	Not used
gpmc_a[21]	A22	A6	Not used	Not used
gpmc_a[20]	A21	A5	Not used	Not used
gpmc_a[19]	A20	A4	Not used	Not used
gpmc_a[18]	A19	A3	Not used	Not used
gpmc_a[17]	A18	A2	Not used	Not used
gpmc_a[16]	A17	A1	Not used	Not used
gpmc_ad[15]	A16/D15	D15	D15	Not used
gpmc_ad[14]	A15/D14	D14	D14	Not used
gpmc_ad[13]	A14/D13	D13	D13	Not used
gpmc_ad[12]	A13/D12	D12	D12	Not used
gpmc_ad[11]	A12/D11	D11	D11	Not used
gpmc_ad[10]	A11/D10	D10	D10	Not used
gpmc_ad[9]	A10/D9	D9	D9	Not used
gpmc_ad[8]	A9/D8	D8	D8	Not used
gpmc_ad[7]	A8/D7	D7	D7	D7
gpmc_ad[6]	A7/D6	D6	D6	D6
gpmc_ad[5]	A6/D5	D5	D5	D5
gpmc_ad[4}	A5/D4	D4	D4	D4
gpmc_ad[3]	A4/D3	D3	D3	D3
gpmc_ad[2]	A3/D2	D2	D2	D2
gpmc_ad[1]	A2/D1	D1	D1	D1
gpmc_ad[0]	A1/D0	D0	D0	D0

When using non-multiplexed memories, it is recommended to enable GPMC_CONFIG[1] LIMITEDADDRESS. This bit forces A[26:11] to 1 on the GPMC I/O side. Thus, only 2Kbytes of memory address space is accessible regardless of the memory size.

With all device types, the GPMC does not drive unnecessary address lines. They stay at their reset value of 0x00.

Address mapping supports address/data-multiplexed 16-bit wide devices:

- The NOR flash memory controller still supports non-multiplexed address and data memory devices.
- Multiplexing mode can be selected through the GPMC_CONFIG1_i[9:8] MUXADDDATA bit field (i = 0 to 7).
- Asynchronous page mode is not supported for multiplexed address and data devices.

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NOTE: The numbering for A (address) is starting from 1 instead of 0 such as D (data) because the A0 signal is handled within the GPMC but is not driven to any pad. The signal is only relevant to 8-bit accesses and this configuration is not recommended. If such a memory or device is connected, only every second word in the memory is accessible, that is, each 16-bit aligned 8-bit word is mapped but not the non-16-bit aligned ones. Any access to a non-aligned one will actually result in accessing the associated aligned one, at address A1 instead of address A.

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15.4.3 GPMC Integration

This section describes module integration in the device, including information about clocks, resets, and hardware requests.

- No STANDBY hardware handshake
- No wake-up request
- One system direct memory access (sDMA) request
- One interrupt request to the Cortex-A9 MPU Interrupt Controller (MA_IRQ) and to DSP subsystem (D_IRQ)
- One clock for functional and interface domains

Figure 15-53 shows GPMC integration.

Figure 15-53. GPMC Integration

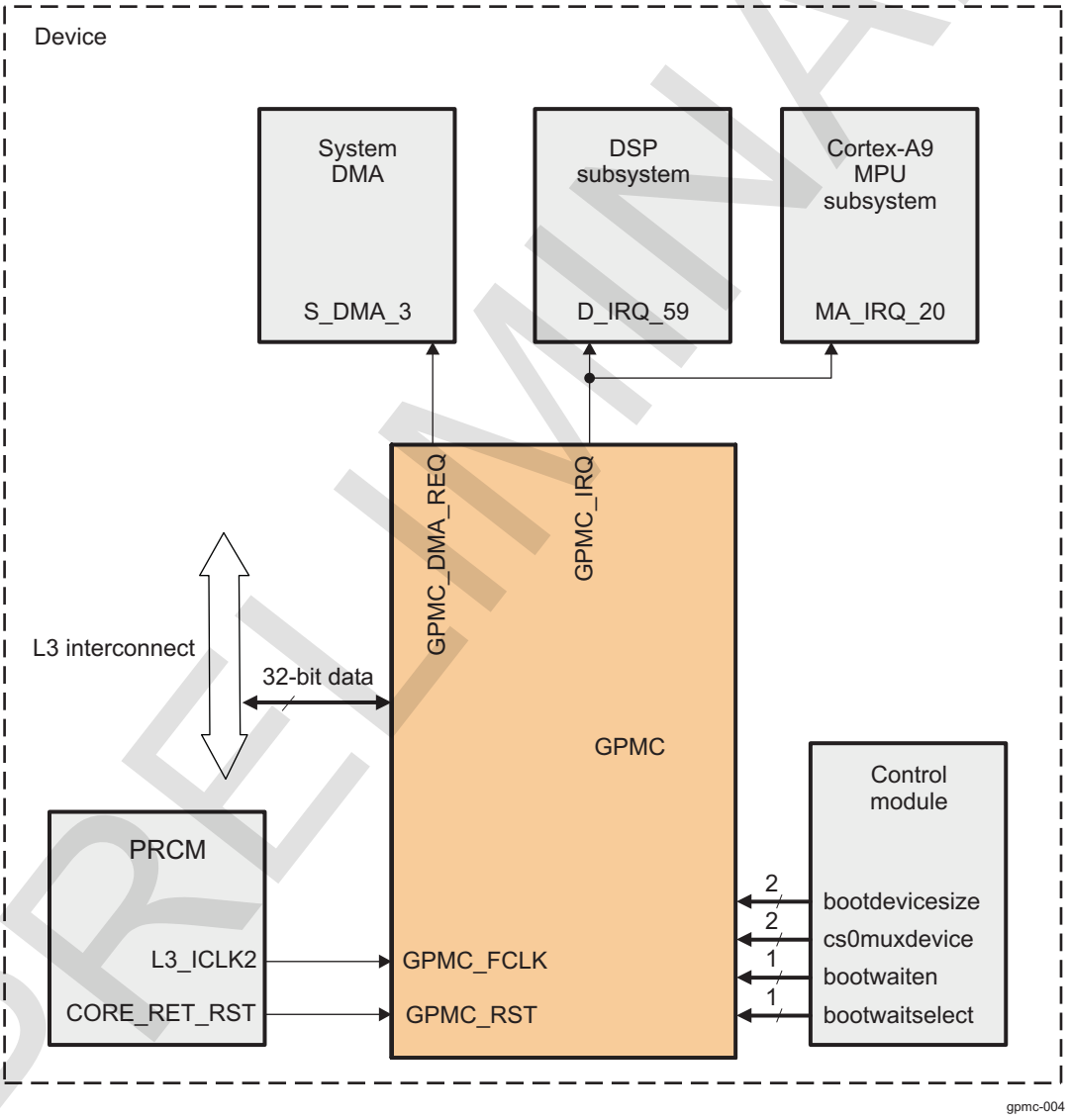

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Table 15-217, Table 15-218 and Table 15-219 summarize the integration of the module in the device.

Table 15-217. GPMC Integration Attributes

Module Instance	Attributes		
	Power Domain	Wake-up Capability	Interconnect
GPMC	PD_CORE	No	L3

NOTE:

- For information about operation performance point (OPP) configuration description, seeSection 3.1.1.1.2, *Module Level Clock Management* in Chapter 3, *Power, Reset, and Clock Management*.

Table 15-218. GPMC Clocks and Resets

Clocks				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
GPMC	GPMC_FCLK	L3_ICLK2	PRCM	Functional clock
Resets				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
GPMC	GPMC_RST	CORE_RET_RST	PRCM	GPMC reset

NOTE: For clock description, see Section 15.4.4.2, *GPMC Clock Configuration*.

Table 15-219. GPMC Hardware Requests

Interrupt Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
GPMC	GPMC_IRQ	D_IRQ_59	DSP	GPMC interrupt to DSP subsystem
	GPMC_IRQ	MA_IRQ_20	Cortex-A9	GPMC interrupt to Cortex-A9 MPU subsystem
DMA Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
GPMC	GPMC_DMA_REQ	S_DMA_3	sDMA	GPMC request from Prefetch Engine to sDMA

NOTE:

- For interrupt source description, see Section 15.4.4.5, *GPMC Interrupt Requests*.
- For DMA source description, see Section 15.4.4.6, *GPMC DMA Requests*.

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15.4.4 GPMC Functional Description

The GPMC basic programming model offers maximum flexibility to support various access protocols for each of the eight configurable chip-selects. Use optimal chip-select settings, based on the characteristics of the external device:

- Different protocols can be selected to support generic asynchronous or synchronous random-access devices (NOR flash, SRAM) or to support specific NAND devices.
- The address and the data bus can be multiplexed on the same external bus.
- Read and write access can be independently defined as asynchronous or synchronous.
- System requests (byte, 16-bit word, burst) are performed through single or multiple accesses. External access profiles (single, multiple with optimized burst length, native- or emulated-wrap) are based on external device characteristics (supported protocol, bus width, data buffer size, native-wrap support).
- System burst read or write requests are synchronous-burst (multiple-read or multiple-write). When neither burst nor page mode is supported by external memory or ASIC devices, system burst read or write requests are translated to successive single synchronous or asynchronous accesses (single reads or single writes). 8-bit wide devices are supported only in single synchronous or single asynchronous read or write mode.
- To simulate a programmable internal-wait state, an external wait pin can be monitored to dynamically control external access at the beginning (initial access time) of and during a burst access.

Each control signal is controlled independently for each chip-select. The internal functional clock of the GPMC (GPMC_FCLK) is used as a time reference to specify the following:

- Read- and write-access duration
- Most GPMC external interface control-signal assertion and deassertion times
- Data-capture time during read access
- External wait-pin monitoring time
- Duration of idle time between accesses, when required

15.4.4.1 GPMC Block Diagram

Figure 15-54 shows the GPMC functional block diagram. The GPMC consists of six blocks:

- L3 interconnect port interface
- Address decoder, GPMC configuration, and chip-select configuration register file
- Access engine
- Prefetch and write-posting engine
- Error correction code engine (ECC)
- External device/memory port interface

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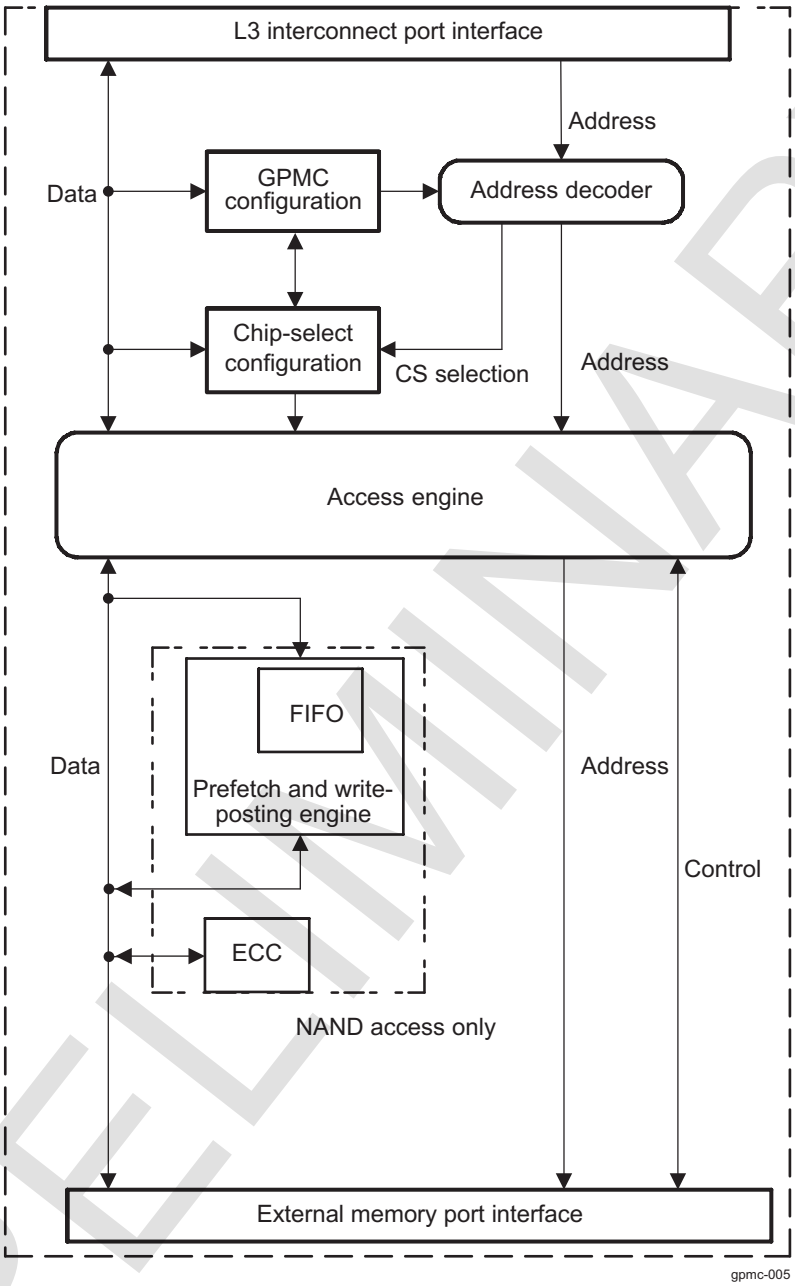
Figure 15-54. GPMC Block Diagram



The GPMC can access various external devices through the L3 Interconnect. The flexible programming model allows a wide range of attached device types and access schemes.

Based on the programmed configuration bit fields stored in the GPMC registers, the GPMC is able to generate all control signals timing depending on the attached device and access type.

Given the chip-select decoding and its associated configuration registers, the GPMC selects the appropriate device type control signals timing.

15.4.4.2 GPMC Clock Configuration

Table 15-220 describes the GPMC clocks.

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Table 15-220. GPMC Clocks

Signal	I/O [1]	Description
GPMC_FCLK	I	Functional and interface clock
gpmc_clk	O	External clock provided to synchronous external memory devices.

(1) I = Input; O = Output

The gpmc_clk is generated by the GPMC from the internal GPMC_FCLK clock. The source of the GPMC_FCLK is described in Table 15-218. The gpmc_clk is configured via the GPMC_CONFIG1_i[1:0] GPMCFCLKDIVIDER field (for i = 0 to 7) as shown in Table 15-221.

Table 15-221. gpmc_clk Configuration

Source Clock	GPMC_CONFIG1_i[1:0] GPMCFCLKDIVIDER	gpmc_clk Generated Clock Provided to External Memory Device
GPMC_FCLK	00	GPMC_FCLK
	01	GPMC_FCLK/2
	10	GPMC_FCLK/3
	11	GPMC_FCLK/4

15.4.4.3 GPMC Software Reset

The GPMC can be reset by software through the GPMC_SYSCONFIG[1] SOFTRESET bit. Setting the bit to 1 enables an active software reset that is functionally equivalent to a hardware reset. Hardware and software resets initialize all GPMC registers and the finite state-machine (FSM) immediately and unconditionally. The GPMC_SYSSTATUS[0] RESETDONE bit indicates that the software reset is complete when its value is 1. The software must ensure that the software reset completes before doing GPMC operations.

15.4.4.4 GPMC Power Management

GPMC power is supplied by the CORE power domain, and GPMC power management complies with system power-management guidelines.

Table 15-222 describes power-management features available for the GPMC module.

NOTE:

- For information about source clock gating and sleep/wake-up transitions description, see Section 3.1.1.1, *Clock Management*, in Chapter 3, *Power, Reset, and Clock Management*.
- For descriptions of EnaWakeUp, IdleMode, ClockActivity, and StandbyMode features, see Section 3.6, *Clock Management Functional Description*, in Chapter 3, *Power, Reset, and Clock Management*.

Table 15-222. GPMC Local Power Management Features

Feature	Registers	Description
Clock Auto Gating	GPMC_SYSCONFIG[0] AUTOIDLE bit	This bit allows a local power optimization inside the module, by gating the GPMC_FCLK clock upon the internal activity.
Slave Idle Modes	GPMC_SYSCONFIG[4:3] SIDLEMODE bit field	Force-idle, No-idle and Smart-idle wakeup modes are available
Clock Activity	N/A	Feature not available
Master Standby Modes	N/A	Feature not available
Global Wake-up Enable	N/A	Feature not available
Wake-up Sources Enable	N/A	Feature not available

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15.4.4.5 GPMC Interrupt Requests

The GPMC generates one interrupt event as shown in Figure 15-53 :

- The interrupt request goes from GPMC (GPMC_IRQ) to the Cortex-A9 MPU subsystem : MA_IRQ_20 and to the DSP susbsystem : D_IRQ_59.

Table 15-223 lists the event flags, and their mask, that can cause module interrupts.

Table 15-223. GPMC Interrupt Events

Event Flag	Event Mask	Sensitivity	Map to	Description
GPMC_IRQSTATUS[10] WAIT2EDGE DETECTIONSTATUS	GPMC_IRQENABLE[10] WAIT2EDGE DETECTIONENABLE	Edge	D_IRQ_59 and MA_IRQ_20	Wait2 edge detection interrupt: Triggered if a rising or falling edge is detected on the gpmc_wait2 signal. The rising or falling edge detection of Wait2 is selected through GPMC_CONFIG[10] WAIT2PINPOLARITY
GPMC_IRQSTATUS[9] WAIT1EDGE DETECTIONSTATUS	GPMC_IRQENABLE[9] WAIT1EDGE DETECTIONENABLE	Edge	D_IRQ_59 and MA_IRQ_20	Wait1 edge detection interrupt: Triggered if a rising or falling edge is detected on the gpmc_wait1 signal. The rising or falling edge detection of Wait1 is selected through GPMC_CONFIG[9] WAIT1PINPOLARITY
GPMC_IRQSTATUS[8] WAIT0EDGE DETECTIONSTATUS	GPMC_IRQENABLE[8] WAIT0EDGE DETECTIONENABLE	Edge	D_IRQ_59 and MA_IRQ_20	Wait0 edge detection interrupt: Triggered if a rising or falling edge is detected on the gpmc_wait0 signal. The rising or falling edge detection of Wait0 is selected through GPMC_CONFIG[8] WAIT0PINPOLARITY
GPMC_IRQSTATUS[1] TERMINAL COUNTSTATUS	GPMC_IRQENABLE[1] TERMINAL COUNTENABLE	Level	D_IRQ_59 and MA_IRQ_20	Terminal count event: Triggered on prefetch process completion, that is when the number of currently remaining data to be requested reaches zero
GPMC_IRQSTATUS[0] FIFOEVENTSTATUS	GPMC_IRQENABLE[0] FIFOEVENTENABLE	Level	D_IRQ_59 and MA_IRQ_20	FIFO event interrupt: Indicates FIFO levels availability for in Write-Posting mode and prefetch mode. GPMC_PREFETCH_CONFIG1[2] DMAMODE shall be set to 0.

15.4.4.6 GPMC DMA Requests

The GPMC generates one DMA event as shown in Figure 15-53 :

- From GPMC (GPMC_DMA_REQ) to the system DMA (sDMA) : S_DMA_3.

15.4.4.7 L3 Interconnect Interface

The GPMC L3 interconnect interface is a pipelined interface including an 16 x 32-bit word write buffer.

Any system host can issue external access requests through the GPMC.

The device system can issue the following requests through this interface:

- One 8-bit / 16-bit / 32-bit interconnect access (read/write)
- Two incrementing 32-bit interconnect accesses (read/write)
- Two wrapped 32-bit interconnect accesses (read/write)
- Four incrementing 32-bit interconnect accesses (read/write)
- Four wrapped 32-bit interconnect accesses (read/write)
- Eight incrementing 32-bit interconnect accesses (read/write)
- Eight wrapped 32-bit interconnect accesses (read/write)

Only linear burst transactions are supported; interleaved burst transactions are not supported. Only power-of-two-length precise bursts 2 x 32, 4 x 32, 8 x 32 or 16 x 32 with the burst base address aligned on the total burst size are supported (this limitation applies to incrementing bursts only).

This interface also provides one interrupt and one DMA request line, for specific event control.

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It is recommended to program the ATTACHEDDEVICEPAGELENGTH field (GPMC_CONFIG1_i[24:23]) according to the effective attached device page length and to enable WRAPBURST bit (GPMC_CONFIG1_i[31]) if the attached device supports wrapping burst.

However, it is possible to emulate wrapping burst on a non-wrapping memory by providing relevant addresses within the page or splitting transactions. Bursts larger than the memory page length are chopped into multiple bursts transactions. Due to the alignment requirements, a page boundary is never crossed.

15.4.4.8 GPMC Address and Data Bus

The current application supports GPMC connection to NAND devices and to address/data-multiplexed memories or devices. Connection to address/data-nonmultiplexed memories or devices is supported with a limited address range of 2 Kbytes.

Depending on the GPMC configuration of each chip-select, address and data bus lines that are not required for a particular access protocol are not updated (changed from current value) and are not sampled when input (input data bus).

- When the GPMC_CONFIG[1] LIMITEDADDRESS bit is set to 1, A26-A11 are not modified during an external memory access. This limits the memory address space to 2K-byte regardless of the memory size.
- For address/data-multiplexed and AAD-multiplexed NOR devices, the address is multiplexed on the data bus.
- 8-bit wide NOR devices do not use GPMC I/O: gpmc_ad[15:8] for data (they are used for address if needed).
- 16-bit wide NAND devices do not use GPMC I/O: gpmc_a[25:16].
- 8-bit wide NAND devices do not use GPMC I/O: gpmc_a[25:16] and GPMC I/O: gpmc_ad[15:8].

CAUTION

Before accessing a chip-select configured with a nonmultiplexed protocol, set the LIMITEDADDRESS bit control.

15.4.4.8.1 GPMC I/O Configuration Setting

NOTE: In this section and next sections, the i in GPMC_CONFIGx_i stands for the GPMC chip-select i where i = 0 to 7.

To select a NAND device, program the following register fields:

- GPMC_CONFIG1_i[11:10] DEVICETYPE field = 0b10
- GPMC_CONFIG1_i[9:8] MUXADDDATA bit = 0b00

To select an address/data-multiplexed device, program the following register fields:

- GPMC_CONFIG1_i[11:10] DEVICETYPE field = 0b00
- GPMC_CONFIG1_i[9:8] MUXADDDATA bit = 0b10

To select an address/address/data-multiplexed device, program the following register fields:

- GPMC_CONFIG1_i[11:10] DEVICETYPE field = 0b00
- GPMC_CONFIG1_i[9:8] MUXADDDATA bit = 0b01

To select an address/data-nonmultiplexed device (limited to a 2K-byte address range), program the following register fields:

- GPMC_CONFIG1_i[11:10] DEVICETYPE field = 0b00
- GPMC_CONFIG1_i[9:8] MUXADDDATA bit = 0b00
- GPMC_CONFIG[1] LIMITEDADDRESS bit = 1

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NOTE: The GPMC_CONFIG[1] LIMITEDADDRESS bit only applies to address/data-nonmultiplexed devices; it has no effect on other device types (NAND, address/data-multiplexed).

15.4.4.8.2 GPMC CS0 Default Configuration at IC Reset

To ensure a correct external boot with a GPMC access from IC reset time on CS0, several external pins are sampled:

- The sys_boot[4:0] pins (device boundary) define the sequence of interfaces and devices to use for booting.
- The sys_boot[5] pin defines which group of booting sequences is preferred: memory booting (sys_boot[5] = 0) or peripheral booting (sys_boot[5] = 1).
- Additional pins are used to configure reset values in the GPMC_CONFIG1_i register (where i = 0) as detailed below and in Table 15-224:
  - The *bootdevicesize* input pin (at the GPMC boundary) defines the size of the attached device on chip-select 0 and is used to configure the GPMC_CONFIG1_i[13:12] DEVICESIZE bits (where i = 0). The BOOT_DEVICE_TYPE signal is propagated from the system control module (SCM). Its value is fixed for the device at 0x1 at IC reset, which means that only 16-bit memories are supported for booting.
  - The *cs0muxdevice* input pin (at the GPMC boundary) selects whether the attached device to chip-select 0 is an address/data-multiplexed device or not. The input pin is used to configure the GPMC_CONFIG1_i[9:8] MUXADDDATA bit (where i = 0). The CS0_MUX_DEVICE signal is propagated from the SCM. Its value is fixed for the device at 0x2 at IC reset, which means that only address/data-multiplexed memories are supported for booting (that is, in a standalone way from memories connected to CS0).
  - The *bootwaiten* input pin (at the GPMC boundary) enables the monitoring on chip-select 0 of the WAIT pin at IC reset release time for read accesses. The input pin is used to configure the GPMC_CONFIG1_i[22] WAITREADMONITORING bit (where i = 0). The BOOT_WAIT_ENABLE signal is propagated from the system control module (SCM). When sys_boot[5:0] = 0b11 1111, the BOOT_WAIT_ENABLE signal is activated, causing the wait pin to be monitored for read accesses.
  - The *bootwaitselect* input pin selects the WAIT signal at IC reset release time between WAIT0 input pin, WAIT1 input pin or WAIT2 input pin. At IC reset release time, these three pins have different polarity.

Table 15-224. Boot Control Interface Input Signals Description

Signal Name	Width	Description
bootdevicesize	2	Size of the device attached on CS0 0b00: 8-bit 0b01: 16-bit 0b10: Reserved 0b11: Reserved
cs0muxdevice	2	Multiplexing mode of the device on CS0 0b00: Nonmultiplexed device on CS0 0b01: AAD-multiplexed device on CS0 (address-address-data) 0b10: Address/Data-multiplexed device on CS0 0b11: Reserved
bootwaiten	1	Wait monitoring on CS0 at IC reset release time for read accesses 0: Wait pin is not monitored 1: Wait pin is monitored
bootwaitselect	1	Selection of the wait pin 0: WAIT0 intput pin 1: WAIT1 intput pin 2: WAIT2 intput pin

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CAUTION

Using the internal boot code, the entire CS0 configuration can be modified before the first CS0 access. This modification of internal boot code is necessary for two external devices:

- NAND device attached to CS0
- Nonmultiplexed 2 Kbytes address range device attached to CS0

At reset time, the IC may boot from the internal ROM.

Reset values of the timing control parameters are defined to cope with direct boot on address and data multiplexed NOR Flash device, on non-multiplexed NOR Flash device or on any asynchronous device with large timing margins assuming a low GPMC_FCLK frequency (for example, 19.2Mhz) at boot time.

For a multiplexed access, the address 16 low-order bits are presented onto gpmc_ad[15:0] while the high-order bits are presented both onto gpmc_a[26:16]. If the external chip interface to the memories uses a 16-bit data bus, the high-order address bits are sampled on the address bus.

The reset values of timing parameters used at boot time are:

- CSONTIME = 1
- CSRDOFFTIME = 16
- ADVONTIME = 4
- ADVRDOFFTIME = 5
- OEONTIME = 6
- OEOFFTIME = 16
- RDACCESSTIME = 15
- RDCYCLETIME = 17

For an AAD-multiplexed access, all address bits are passed onto the data bus using two nADV rising edge. The first rising edge latches the address MSB down to bit 17 while the second rising edge latches address bits 16 down to 1. This configuration is only used for 16-bit memories.

The reset values of these timing parameters used at boot time are:

- ADVAADMUXONTIME = 1
- ADVAADMUXRDOFFTIME = 2
- OEAADMUXONTIME = 1
- OEAADMUXRDOFFTIME = 3

15.4.4.9 Address Decoder and Chip-Select Configuration

Addresses are decoded accordingly with the address request of the chip-select and the content of the chip-select base address register file, which includes a set of global GPMC configuration registers and eight sets of chip-select configuration registers.

The GPMC configuration register file is memory-mapped and can be read or written with byte, 16-bit word, or 32-bit word accesses. The register file should be configured as a noncacheable, nonbufferable region to prevent any desynchronization between host execution (write request) and the completion of register configuration (write completed with register updated). Section 15.4.7,*GPMC Register Manual* provides the GPMC register locations. For the map of GPMC memory locations, see Chapter 2 , *Memory Mapping*.

After the chip-select is configured, the access engine accesses the external device, drives the external interface control signals, and applies the interface protocol based on user-defined timing parameters and settings.

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15.4.4.9.1 Chip-Select Base Address and Region Size

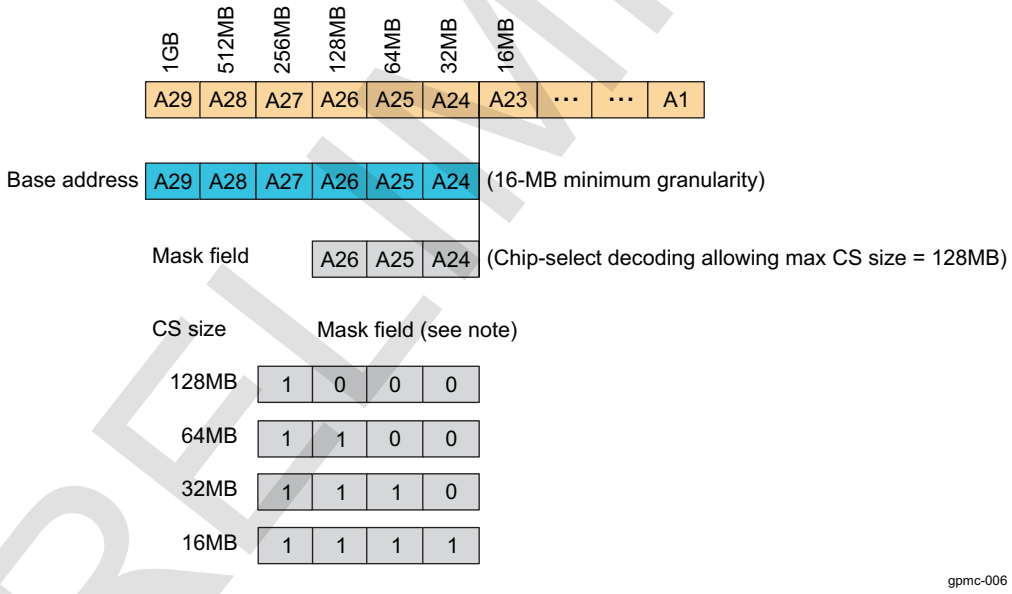
Any external memory or ASIC device attached to the GPMC external interface can be accessed by any device system host within the GPMC 1 Gbyte contiguous address space. For details, see Chapter 2, *Memory Mapping*.

The GPMC 1G byte address space can be divided into a maximum of eight chip-select regions with programmable base address and programmable CS size. The CS size is programmable from 16M bytes to 128M bytes (must be a power-of-2) and is defined by the mask field. Attached memory smaller than the programmed CS region size is accessed through the entire CS region (aliasing).

Each chip-select has a 6-bit base address encoding and a 4-bit decoding mask, which must be programmed according to the following rules:

- The programmed chip-select region base address must be aligned on the chip-select region size address boundary and is limited to a power-of-2 address value. During access decoding, the register base address value is used for address comparison with the address-bit line mapping as described in Figure 15-55 (with A0 as the device system byte-address line). Base address is programmed through the GPMC_CONFIG7_i[5:0] BASEADDRESS bit field
- The register mask is used to exclude some address lines from the decoding. A register mask bit field set to 0 suppresses the associated address line from the address comparison (incoming address bit line is don't care). The register mask value must be limited to the subsequent value, based on the desired chip-select region size. Any other value has an undefined result. When multiple chip-select regions with overlapping addresses are enabled concurrently, access to these chip-select regions is cancelled and a GPMC access error is posted. The mask field is programmed through the GPMC_CONFIG7_i[11:8] MASKADDRESS bit field.

Figure 15-55. Chip-Select Address Mapping and Decoding Mask



Chip-select configuration (base and mask address or any protocol and timing settings) must be performed while the associated chip-select is disabled through the GPMC_CONFIG7_i[6] CSVALID bit (where i stands for the GPMC chip-select value, i = 0 to 7). In addition, a chip-select configuration can only be disabled if there is no ongoing access to that chip-select. This requires activity monitoring of the prefetch or write-posting engine if the engine is active on the chip-select. Also, the write buffer state must be monitored to wait for any posted write completion to the chip-select.

Any access attempted to a nonvalid GPMC address region (CSVALID disabled or address decoding outside a valid chip-select region) is not propagated to the external interface and a GPMC access error is posted. In case of chip-selects overlapping, an error is generated and no access will occur on either chip-select.

Chip-select 0 is the only chip-select region enabled after either a power-up or a GPMC reset.

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CAUTION

Although the GPMC interface can drive up to 4 chip-selects, the frequency specified for this interface is for a specific load. If this load is exceeded, the maximum frequency cannot be reached. One solution is to implement a board with buffers, to allow the slowest device to maintain the total load on the lines.

15.4.4.9.2 Access Protocol

15.4.4.9.2.1 Supported Devices

The access protocol of each chip-select can be independently specified through the GPMC_CONFIG1_i[11:10] DEVICETYPE parameter (where i = 0 to 7) for:

- Random-access synchronous or asynchronous memory like NOR flash, SRAM
- NAND flash asynchronous devices

NOTE: For more information about the NAND flash GPMC basic programming model and NAND support, see Section 15.4.4.13, *NAND Device Basic Programming Model*, and Section 15.4.4.13.1, *NAND Memory Device in Byte or Word 16 Stream Mode*.

15.4.4.9.2.2 Access Size Adaptation and Device Width

Each chip-select can be independently configured through the GPMC_CONFIG1_i[13:12] DEVICESIZE field (i = 0 to 7) to interface with a 16-bit wide device or an 8-bit wide device. System requests with data width greater than the external device data bus width are split into successive accesses according to both the external device data-bus width and little-endian data organization.

NOTE: The device does not provide the A0 byte address line required for random-byte addressable 8-bit wide device interfacing (for both multiplexed and nonmultiplexed protocol). It limits the use of 8-bit wide device interfacing to byte-alias accesses. This limitation is not applicable to NAND device interfacing (8-bit wide or 16-bit wide devices).

15.4.4.9.2.3 Address/Data-Multiplexing Interface

For random synchronous or asynchronous memory interfacing (DEVICETYPE = 0b00), an address- and data-multiplexing protocol can be selected through the GPMC_CONFIG1_i[9:8] MUXADDDATA bit field (i = 0 to 7). The nADV signal must be used as the external device address latch control signal. For the associated chip-select configuration, nADV assertion and deassertion time and nOE assertion time must be set to the appropriate value to meet the address latch setup/hold time requirements of the external device. See Section 15.4.3, *GPMC Integration*.

NOTE: This address/data-multiplexing interface is not applicable to NAND device interfacing. NAND devices require a specific address, command, and data multiplexing protocol. See Section 15.4.4.13, *NAND Device Basic Programming Model*.

15.4.4.9.3 External Signals

15.4.4.9.3.1 WAIT Pin Monitoring Control

GPMC access time can be dynamically controlled using an external gpmc_wait pin when the external device access time is not deterministic and cannot be defined and controlled only using the GPMC internal RDACCESSTIME, WRACCESSTIME and PAGEBURSTACCESSTIME wait state generator.

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The GPMC features three input wait pins: gpmc_wait2, gpmc_wait1 and gpmc_wait0. These pins allow control of external devices with different wait-pin polarity. They also allow the overlap of wait-pin assertion from different devices without affecting access to devices for which the wait pin is not asserted.

- The GPMC_CONFIG1_i[17:16] WAITPINSELECT field (i = 0 to 7) selects which input gpmc_wait pin is used for the device attached to the corresponding chip-select.
- The polarity of the wait pin is defined through the WAITxPINPOLARITY bit of the GPMC_CONFIG register. A wait pin configured to be active low means that low level on the WAIT signal indicates that the data is not ready and that the data bus is invalid. When WAIT is inactive, data is valid.

The GPMC access engine can be configured per CS to monitor the wait pin of the external memory device or not, based on the access type: read or write.

- The GPMC_CONFIG1_i[22] WAITREADMONITORING bit defines whether the wait pin should be monitored during read accesses or not.
- The GPMC_CONFIG1_i[21] WAITWRITEMONITORING bit defines whether the wait pin should be monitored during write accesses or not.

The GPMC access engine can be configured to monitor the wait pin of the external memory device asynchronously or synchronously with the GPMC_CLK clock, depending on the access type: synchronous or asynchronous (the GPMC_CONFIG1_i[29] READTYPE and GPMC_CONFIG1_i[27] WRITETYPE bits).

15.4.4.9.3.1.1 Wait Monitoring During an Asynchronous Read Access

When wait-pin monitoring is enabled for read accesses (WAITREADMONITORING), the effective access time is a logical AND combination of the RDACCESSTIME timing completion and the wait-deasserted state.

During asynchronous read accesses with wait-pin monitoring enabled, the wait pin must be at a valid level (asserted or deasserted) for at least two GPMC clock cycles before RDACCESSTIME completes, to ensure correct dynamic access-time control through wait-pin monitoring. The advance pipelining of the two GPMC clock cycles is the result of the internal synchronization requirements for the WAIT signal.

In this context, RDACCESSTIME is used as a WAIT invalid timing window and is set to such a value that the wait pin is at a valid state two GPMC clock cycles before RDACCESSTIME completes.

Similarly, during a multiple-access cycle (for example, asynchronous read page mode), the effective access time is a logical AND combination of PAGEBURSTACCESSTIME timing completion and the wait-deasserted state. Wait-monitoring pipelining is also applicable to multiple accesses (access within a page).

- WAIT monitored as active freezes the CYCLETIME counter. For an access within a page, when the CYCLETIME counter is by definition in a lock state, WAIT monitored as asserted extends the current access time in the page. Control signals are kept in their current state. The data bus is considered invalid, and no data are captured during this clock cycle.
- WAIT monitored as inactive unfreezes the CYCLETIME counter. For an access within a page, when the CYCLETIME counter is by definition in a lock state, WAIT monitored as inactive completes the current access time and starts the next access phase in the page. The data bus is considered valid, and data are captured during this clock cycle. In case of a single access or if this was the last access in a multiple-access cycle, all signals are controlled according to their related control timing value and according to the CYCLETIME counter status.

When a delay larger than two GPMC clocks must be observed between wait-pin deactivation time and data valid time (including the required GPMC and the device data setup time), an extra delay can be added between wait-pin deassertion time detection and effective data-capture time and the effective unlock of the CYCLETIME counter. This extra delay can be programmed in the GPMC_CONFIG1_i[19:18] WAITMONITORINGTIME field (i = 0 to 7).

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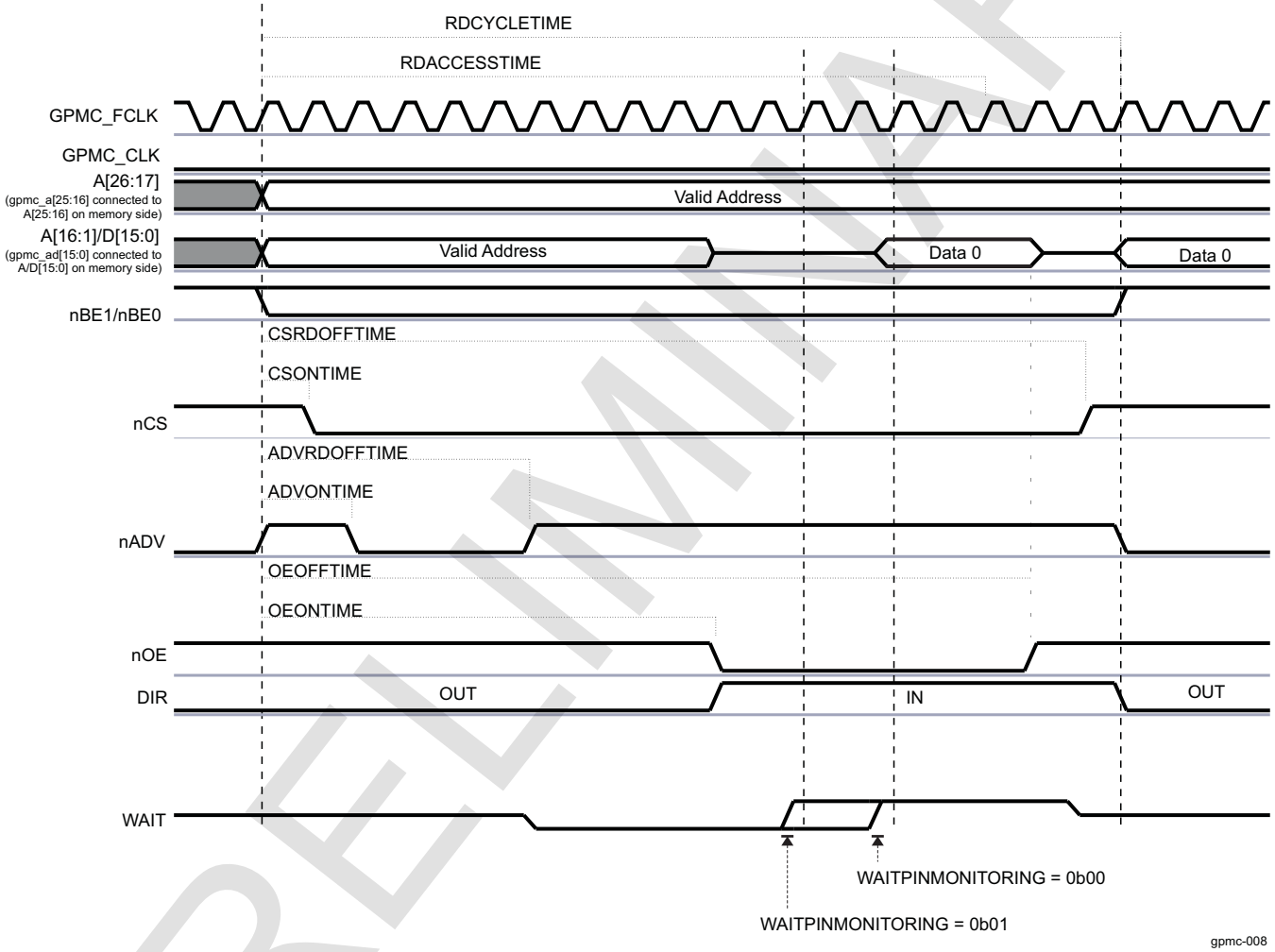
NOTE:

- The WAITMONITORINGTIME parameter does not delay the wait-pin active or inactive detection, nor does it modify the two GPMC clocks pipelined detection delay.
- This extra delay is expressed as a number of GPMC_CLK clock cycles, even though the access is defined as asynchronous, and no GPMC_CLK clock is provided to the external device. Still, GPMCFCLKDIVIDER is used as a divider for the GPMC clock, so it must be programmed to define the correct WAITMONITORINGTIME delay.

Figure 15-56 shows wait behavior during an asynchronous single read access.

Figure 15-56. Wait Behavior During an Asynchronous Single Read Access (GPMCFCLKDivider = 1)



NOTE: The WAIT signal is active low. GPMC_CONFIG1_i[19:18] WAITMONITORINGTIME = 0b00, or 0b01.

15.4.4.9.3.1.2 Wait Monitoring During an Asynchronous Write Access

When wait-pin monitoring is enabled for write accesses (GPMC_CONFIG1_i[21] WAITWRITEMONITORING bit = 0x1), the WAIT-invalid timing window is defined by the WRACCESSTIME field. WRACCESSTIME must be set so that the wait pin is at a valid state two GPMC clock cycles before WRACCESSTIME completes. The advance pipelining of the two GPMC clock cycles is the result of the internal synchronization requirements for the WAIT signal.

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- WAIT monitored as active freezes the CYCLETIME counter. This informs the GPMC that the data bus is not captured by the external device. The control signals are kept in their current state. The data bus still drives the data.
- WAIT monitored as inactive unfreezes the CYCLETIME counter. This informs that the data bus is correctly captured by the external device. All signals, including the data bus, are controlled according to their related control timing value and to the CYCLETIME counter status.

When a delay larger than two GPMC clock cycles must be observed between wait-pin deassertion time and the effective data write into the external device (including the required GPMC data setup time and the device data setup time), an extra delay can be added between wait-pin deassertion time detection and effective data write time into the external device and the effective unfreezing of the CYCLETIME counter. This extra delay can be programmed in the GPMC_CONFIG1_i[19:18] WAITMONITORINGTIME fields (i = 0 to 7).

NOTE:

- The WAITMONITORINGTIME parameter does not delay the wait-pin assertion or deassertion detection, nor does it modify the two GPMC clock cycles pipelined detection delay.
- This extra delay is expressed as a number of GPMC_CLK clock cycles, even though the access is defined as asynchronous, and even though no clock is provided to the external device. Still, GPMC_CONFIG1_i[1:0] GPMCFCLKDIVIDER is used as a divider for the GPMC clock and so it must be programmed to define the correct WAITMONITORINGTIME delay.

15.4.4.9.3.1.3 Wait Monitoring During a Synchronous Read Access

During synchronous accesses with wait-pin monitoring enabled, the wait pin is captured synchronously with GPMC_CLK, using the rising edge of this clock.

The WAIT signal can be programmed to apply to the same clock cycle it is captured in. Alternatively, it can be sampled one or two GPMC_CLK cycles ahead of the clock cycle it applies to. This pipelining is applicable to the entire burst access, and to all data phase in the burst access. This WAIT pipelining depth is programmed in the GPMC_CONFIG1_i[19:18] WAITMONITORINGTIME field (where i = 0 to 7), and is expressed as a number of GPMC_CLK clock cycles.

In synchronous mode, when wait-pin monitoring is enabled (GPMC_CONFIG1_i[22] WAITREADMONITORING bit), the effective access time is a logical AND combination of the RDACCESSTIME timing completion and the WAIT deasserted-state detection.

Depending on the programmed WAITMONITORINGTIME value, the wait pin should be at a valid level, either asserted or deasserted:

- In the same clock cycle the data is valid if WAITMONITORINGTIME = 0 (at RDACCESSTIME completion)
- In the WAITMONITORINGTIME x (GPMCFCLKDIVIDER + 1) GPMC_FCLK clock cycles before RDACCESSTIME completion if WAITMONITORINGTIME not equal to 0

Similarly, during a multiple-access cycle (burst mode), the effective access time is a logical AND combination of PAGEBURSTACCESSTIME timing completion and the wait-inactive state. The Wait pipelining depth programming applies to the whole burst access.

- WAIT monitored as active freezes the CYCLETIME counter. For an access within a burst (when the CYCLETIME counter is by definition in a lock state), WAIT monitored as active extends the current access time in the burst. Control signals are kept in their current state. The data bus is considered invalid, and no data are captured during this clock cycle.
- WAIT monitored as inactive unfreezes the CYCLETIME counter. For an access within a burst (when the CYCLETIME counter is by definition in lock state), WAIT monitored as inactive completes the current access time and starts the next access phase in the burst. The data bus is considered valid, and data are captured during this clock cycle. In a single access or if this was the last access in a multiple-access cycle, all signals are controlled according to their relative control timing value and the CYCLETIME counter status.

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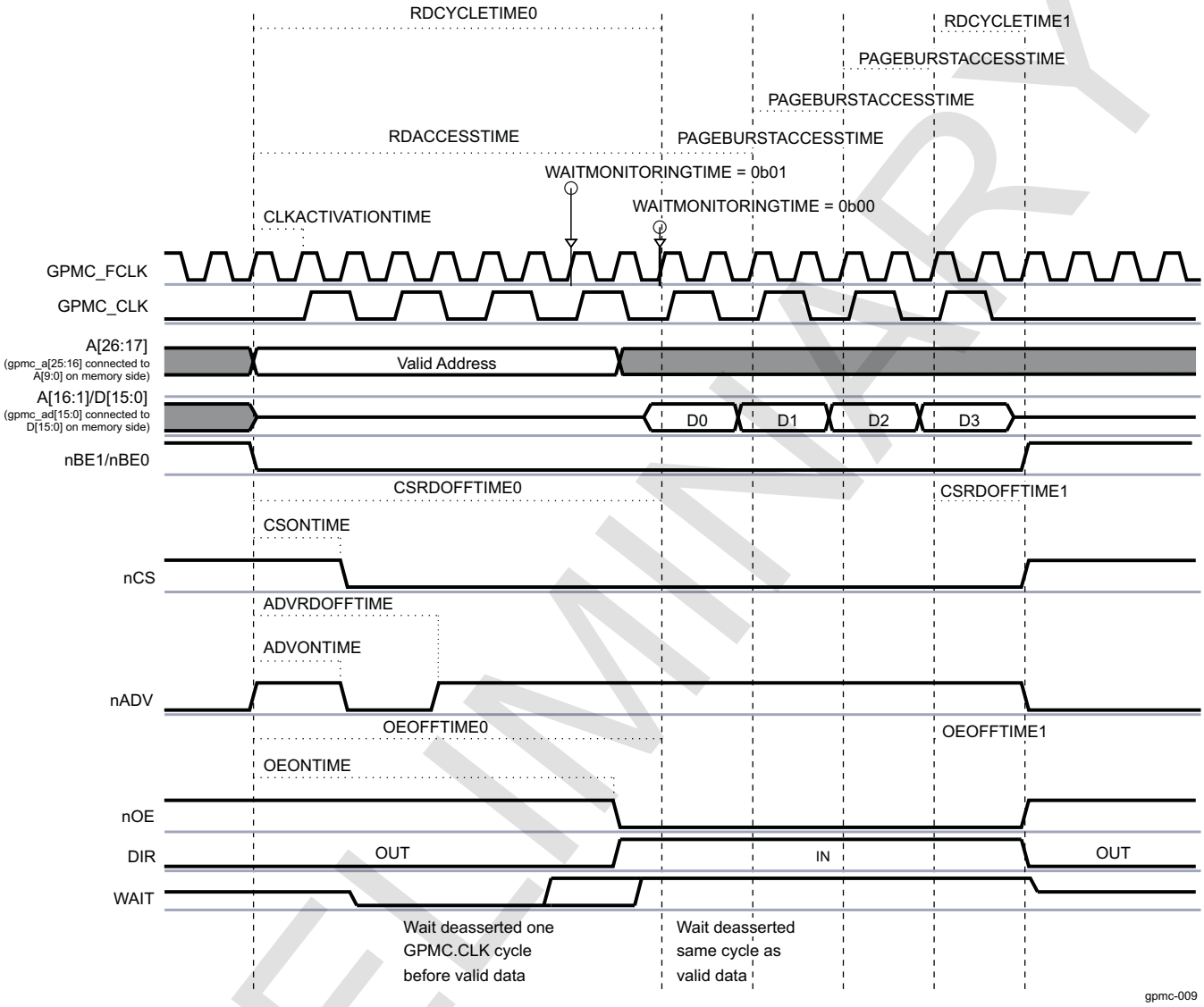
Figure 15-57 shows wait behavior during a synchronous read burst access.

Figure 15-57. Wait Behavior During a Synchronous Read Burst Access



NOTE: The WAIT signal is active low. WAITMONITORINGTIME = 00, 01.

15.4.4.9.3.1.4 Wait Monitoring During a Synchronous Write Access

During synchronous accesses with wait-pin monitoring enabled (the WAITWRITEMONITORING bit), the wait pin is captured synchronously with GPMC_CLK, using the rising edge of this clock.

If enabled, external wait-pin monitoring can be used in combination with WRACCESSTIME to delay the effective memory device GPMC_CLK capture edge.

Wait-monitoring pipelining depth is similar to synchronous read access:

- At WRACCESSTIME completion if WAITMONITORINGTIME = 0
- In the WAITMONITORINGTIME x (GPMCFCLKDIVIDER + 1) GPMC_FCLK cycles before WRACCESSTIME completion if WAITMONITORINGTIME not equal to 0.

Wait-monitoring pipelining definition applies to whole burst accesses:

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- WAIT monitored as active freezes the CYCLETIME counter. For accesses within a burst, when the CYCLETIME counter is by definition in a lock state, WAIT monitored as active indicates that the data bus is not being captured by the external device. Control signals are kept in their current state. The data bus is kept in its current state.
- WAIT monitored as inactive unfreezes the CYCLETIME counter. For accesses within a burst, when the CYCLETIME counter is by definition in a lock state, WAIT monitored as inactive indicates the effective data capture of the bus by the external device and starts the next access of the burst. In case of a single access or if this was the last access in a multiple access cycle, all signals, including the data bus, are controlled according to their related control timing value and the CYCLETIME counter status.

NOTE: Wait monitoring is supported for all configurations except for GPMC_CONFIG1_i[19:18] WAITMONITORINGTIME = 0x0 (where i = 0 to 7) for write bursts with a clock divider of 1 or 2 (GPMC_CONFIG1_i[1:0] GPMCFCLKDIVIDER field equal to 0x0 or 0x1 respectively).

15.4.4.9.3.1.5 WAIT with NAND Device

For details about the use of the wait pin for communication with a NAND flash external device, see Section 15.4.4.13.2, *NAND Device-Ready Pin*.

15.4.4.9.3.1.6 Idle Cycle Control Between Successive Accesses

15.4.4.9.3.1.6.1 Bus Turnaround (BUSTURNAROUND)

To prevent data-bus contention, an access that follows a read access to a slow memory/device must be delayed (in other words, control the nCS/nOE de-assertion to data bus in high-impedance delay).

The bus turnaround is a time-out counter starting after nCS or nOE de-assertion time, whichever occurs first, and delays the next access start-cycle time. The counter is programmed through the GPMC_CONFIG6_i[3:0] BUSTURNAROUND bit field (where i = 0 to 7).

After a read access to a chip-select with a non zero BUSTURNAROUND, the next access is delayed until the BUSTURNAROUND delay completes, if the next access is one of the following:

- A write access to any chip-select (same or different from the chip-select data was read from)
- A read access to a different chip-select from the chip-select data was read access from
- A read or write access to a chip-select associated with an address/data-multiplexed device

NOTE: Bus keeping starts after bus turnaround completion so that DIR changes from IN to OUT after bus turnaround. The bus will not have enough time to go into high-impedance even though it could be driven with the same value before bus turnaround timing.

BUSTURNAROUND delay runs in parallel with GPMC_CONFIG6_i[3:0] CYCLE2CYCLEDELAY delays. It should be noted that BUSTURNAROUND is a timing parameter for the ending chip-select access while CYCLE2CYCLEDELAY is a timing parameter for the following chip-select access. The effective minimum delay between successive accesses is driven by these delay timing parameters and by the access type of the following access. See Figure 15-58 to Figure 15-60.

Another way to prevent bus contention is to define an earlier nCS or nOE deassertion time for slow devices or to extend the value of RDCYCLETIME. Doing this prevents bus contention, but affects all accesses of this specific chip-select.

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Figure 15-58. Read to Read for an Address-Data Multiplexed Device, on Different CS, without Bus Turnaround (nCS0 attached to a fast device)

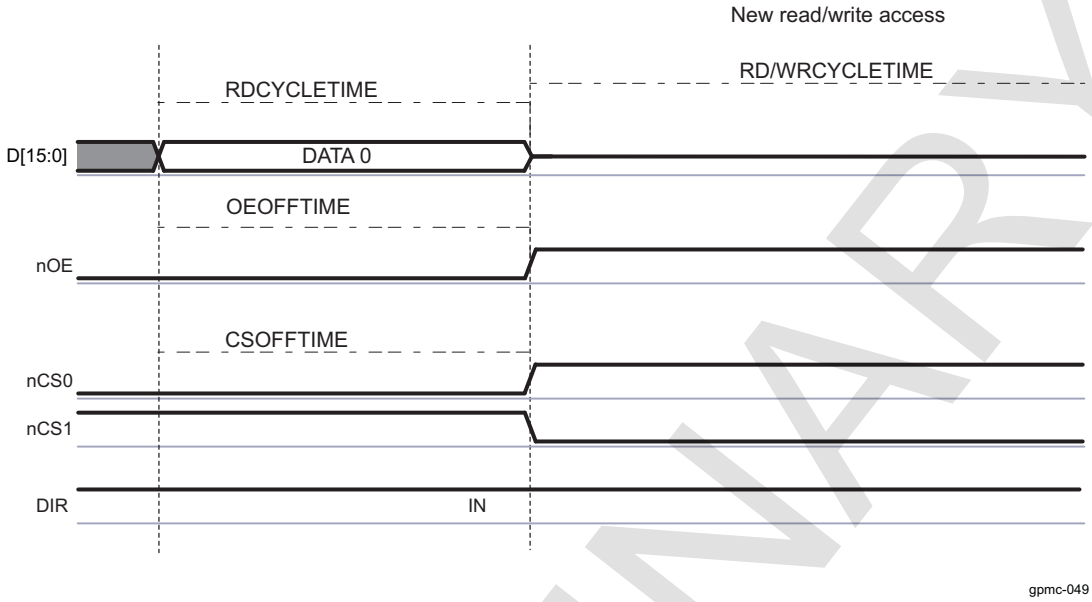

Figure 15-59. Read to Read / Write for an Address-Data Multiplexed Device, on Different CS, with Bus Turnaround

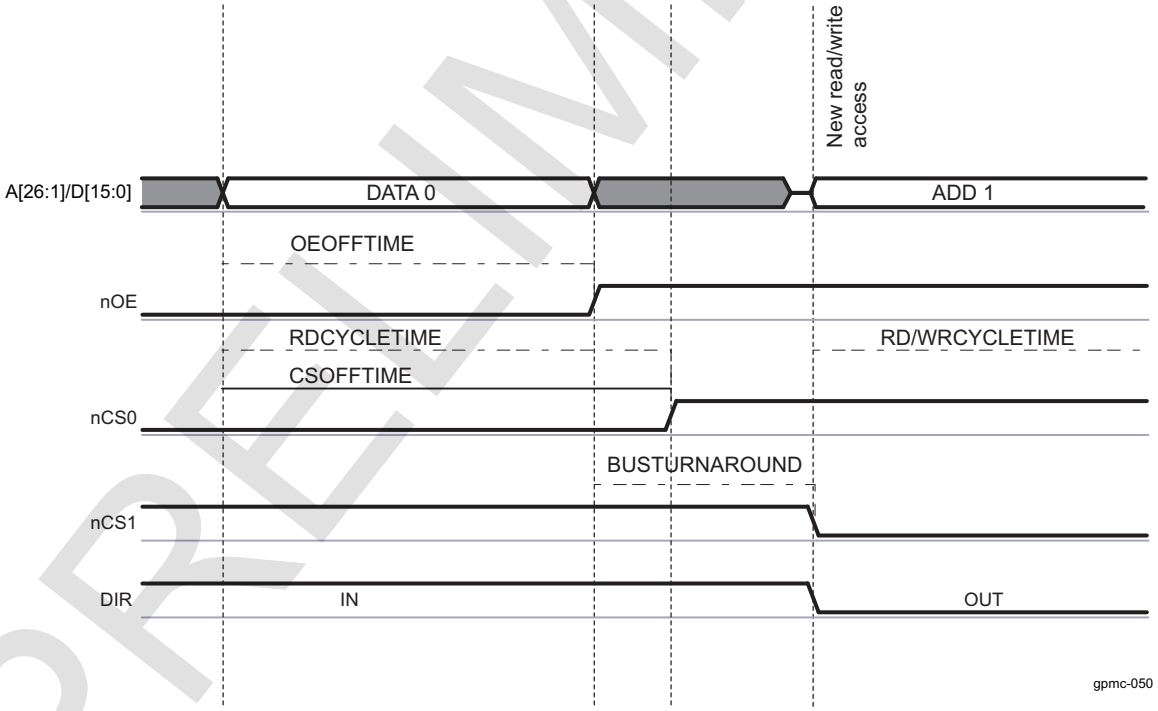

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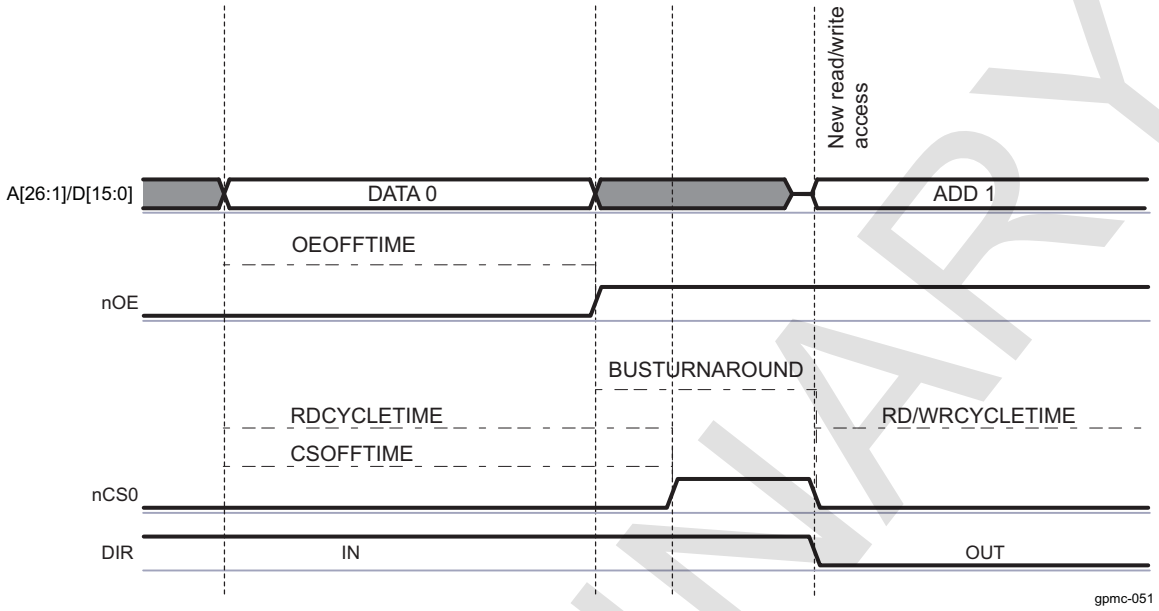
Figure 15-60. Read to Read / Write for a Address-Data or AAD-multiplexed device, on the Same CS, with Bus Turnaround



15.4.4.9.3.1.6.2 Idle Cycles Between Accesses to Same Chip-Select (CYCLE2CYCLESAMECSEN, CYCLE2CYCLEDELAY)

Some devices require a minimum chip-select signal inactive time between accesses. The GPMC_CONFIG6_i[7] CYCLE2CYCLESAMECSEN bit (i = 0 to 7) enables insertion of a minimum number of GPMC_FCLK cycles, defined by the GPMC_CONFIG6_i[11:8] CYCLE2CYCLEDELAY field, between successive accesses of any type (read or write) to the same chip-select.

If CYCLE2CYCLESAMECSEN is enabled, any subsequent access to the same chip-select is delayed until its CYCLE2CYCLEDELAY completes. The CYCLE2CYCLEDELAY counter starts when CSRDOFFTIME/CSWROFFTIME completes.

The same applies to successive accesses occurring during 32-bit word or burst accesses split into successive single accesses when the single-access mode is used (GPMC_CONFIG1_i[30] READMULTIPLE = 0 or GPMC_CONFIG1_i[28] WRITEMULTIPLE = 0).

All control signals (CS, ADV#/ALE, BE0#/CLE, WE#, and GPMC.CLK) are kept inactive (ADV#/ALE, BE0#/CLE, and GPMC.CLK at low level; and CS, OE#/RE, and WE at high level) during the idle GPMC.FCLK cycles. This prevents back-to-back accesses to the same chip-select without idle cycles between accesses.

15.4.4.9.3.1.6.3 Idle Cycles Between Accesses to Different Chip-Select (CYCLE2CYCLEDIFFCSEN, CYCLE2CYCLEDELAY)

Because of the pipelined behavior of the system, successive accesses to different chip-selects can occur back-to-back with no idle cycles between accesses. Depending on the control signals (nCS, nADV/ALE, nBE0/CLE, nOE/RE, nWE) assertion and de-assertion timing parameters and on the IC timing parameters, some control signals assertion times may overlap between the successive accesses to different CS. Similarly, some control signals (WE, OE/RE) may not respect required transition times.

To work around the overlapping and to observe the required control-signal transitions, a minimum of CYCLE2CYCLEDELAY inactive cycles is inserted between the access being initiated to this chip-select and the previous access ending for a different chip-select. This applies to any type of access (read or write).

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If GPMC_CONFIG6_i[6] CYCLE2CYCLEDIFFCSEN is enabled, the chip-select access is delayed until CYCLE2CYCLEDELAY cycles have expired since the end of a previous access to a different chip-select. CYCLE2CYCLEDELAY count starts at CSRDOFFTIME/CSWROFFTIME completion. All control signals are kept inactive during the idle GPMC_FCLK cycles.

NOTE: CYCLE2CYCLESAMECSEN and CYCLE2CYCLEDIFFCSEN should be set in GPMC_CONFIG6_i registers to respectively get idle cycles inserted between accesses on this chip-select and after accesses to a different chip-select.

The CYCLE2CYCLEDELAY delay runs in parallel with the BUSTURNAROUND delay. It should be noted that BUSTURNAROUND is a timing parameter defined for the ending chip-select access, whereas CYCLE2CYCLEDELAY is a timing parameter defined for the starting chip-select access. The effective minimum delay between successive accesses is based on the larger delay timing parameter and on access type combination, since bus turnaround does not apply to all access types. See Section 15.4.4.9.3.1.6.1, *Bus Turnaround (BUSTURNAROUND)* for more details on bus turnaround.

Table 15-225 describes the configuration required for idle cycle insertion.

Table 15-225. Idle Cycle Insertion Configuration

1st Access Type	BUSTURN AROUND Timing Parameter	Second Access Type	Chip-Select	Add/Data Multiplexed	CYCLE2 CYCLE SAMECSEN Parameter	CYCLE2 CYCLE DIFFCSEN Parameter	Idle Cycle Insertion Between the Two Accesses
R/W	= 0	R/W	Any	Any	0	x	No idle cycles are inserted if the two accesses are well pipelined.
R	0	R	Same	Nonmuxed	x	0	No idle cycles are inserted if the two accesses are well pipelined.
R	0	R	Different	Nonmuxed	0	0	BUSTURNAROUND cycles are inserted.
R	0	R/W	Any	Muxed	0	0	BUSTURNAROUND cycles are inserted.
R	0	W	Any	Any	0	0	BUSTURNAROUND cycles are inserted.
W	0	R/W	Any	Any	0	0	No idle cycles are inserted if the two accesses are well pipelined.
R/W	= 0	R/W	Same	Any	1	x	CYCLE2CYCLEDELAY cycles are inserted.
R/W	= 0	R/W	Different	Any	x	1	CYCLE2CYCLEDELAY cycles are inserted.
R/W	0	R/W	Same	Any	1	x	CYCLE2CYCLEDELAY cycles are inserted. If BTA idle cycles already apply on these two back-to-back accesses, the effective delay is max (BUSTURNAROUND, CYCLE2CYCLEDELAY).
R/W	0	R/W	Different	Any	x	1	CYCLE2CYCLEDELAY cycles are inserted. If BTA idle cycles already apply on these two back-to-back accesses, the effective delay is maximum (BUSTURNAROUND, CYCLE2CYCLEDELAY).

15.4.4.9.3.1.7 Slow Device Support (TIMEPARAGRANULARITY Parameter)

All access-timing parameters can be multiplied by 2 by setting the GPMC_CONFIG1_i[4] TIMEPARAGRANULARITY bit (where i stands for the GPMC chip-select value, i = 0 to 7). Increasing all access timing parameters allows support of slow devices.

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15.4.4.9.3.2 gpmc_io_dir Pin

The gpmc_io_dir pin is used to control I/O direction on the GPMC data bus gpmc_ad[15:0]. Depending on top-level pad multiplexing, this signal can be output and used externally to the device, if required.

The gpmc_io_dir pin is low during transmit (OUT) and high during receive (IN).

For write accesses, the gpmc_io_dir pin stays OUT from start-cycle time to end-cycle time.

For read accesses, the gpmc_io_dir pin goes from OUT to IN at nOE assertion time and stays IN until:

- BUSTURNAROUND is enabled:
  - The gpmc_io_dir pin goes from IN to OUT at end-cycle time plus programmable bus turnaround time.
- BUSTURNAROUND is disabled:
  - After an asynchronous read access, the gpmc_io_dir pin goes from IN to OUT at RDACCESSTIME + 1 GPMC_FCLK cycle or when RDCYCLETIME completes, whichever occurs last.
  - After a synchronous read access, the gpmc_io_dir pin goes from IN to OUT at RDACCESSTIME + 2 GPMC_FCLK cycles or when RDCYCLETIME completes, whichever occurs last.

Because of the bus-keeping feature of the GPMC, after a read or write access and with no other accesses pending, the default value of the gpmc_io_dir pin is OUT (see Section 15.4.4.10.10, *Bus Keeping Support*).

In nonmultiplexed devices, the gpmc_io_dir pin stays IN between two successive read accesses to prevent unnecessary toggling (nonmultiplexed 16-bit wide devices support is limited to 2 Kbytes).

15.4.4.9.3.3 Reset

No reset signal is sent to the external memory device by the GPMC. For more information about external-device reset, see Chapter 3, *Power, Reset, and Clock Management*.

The PRCM module provides an input pin, global_rst_n, to the GPMC:

- The global_rst_n pin is activated during device warm reset and cold reset.
- The global_rst_n pin initializes the internal state-machine and the internal configuration registers.

15.4.4.9.3.4 Write Protect Signal (nWP)

When connected to the attached memory device, the write protect signal can enable or disable the lockdown function of the attached memory.

The gpmc_nwp output pin value is controlled through the GPMC_CONFIG[4] WRITEPROTECT bit, which is common to all CS.

15.4.4.9.3.5 Byte Enable (nBE1/nBE0)

Byte enable signals (nBE1/nBE0) are:

- Valid (asserted or nonasserted according to the incoming system request) from access start to access completion for asynchronous and synchronous single accesses
- Asserted low from access start to access completion for asynchronous and synchronous multiple read accesses
- Valid (asserted or nonasserted, according to the incoming system request) synchronously to each written data for synchronous multiple write accesses

15.4.4.9.4 Error Handling

When an error occurs in the GPMC, the error information is stored in the GPMC_ERR_TYPE register and the address of the illegal access is stored in the GPMC_ERR_ADDRESS register. The GPMC only keeps the first error abort information until the GPMC_ERR_TYPE register is reset. Subsequent accesses that cause errors are not logged until the error is cleared by hardware with the GPMC_ERR_TYPE[0] ERRORVALID bit.

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- ERRORNOTSUPPADD occurs when an incoming system request address decoding does not match any valid chip-select region, or if two chip-select regions are defined as overlapped, or if a register file access is tried outside the valid address range of 1 Kbyte.
- ERRORNOTSUPPMCMD occurs when an unsupported command request is decoded at the L3 interconnect interface.
- ERRORTIMEOUT: A time-out mechanism prevents the system from hanging. The start value of the 9-bit time-out counter is defined in the GPMC_TIMEOUT_CONTROL register and enabled with the GPMC_TIMEOUT_CONTROL[0] TIMEOUTENABLE bit. When enabled, the counter starts at start-cycle time until it reaches 0 and data is not responded to from memory, then a time-out error occurs. When data are sent from memory, this counter is reset to its start value. With multiple accesses (asynchronous page mode or synchronous burst mode), the counter is reset to its start value for each data access within the burst.

The GPMC does not generate interrupts on these errors. True abort to the MPU or interrupt generation is handled at interconnect level.

15.4.4.10 Timing Setting

The GPMC offers the maximum flexibility to support various access protocols. Most of the timing parameters of the protocol access used by the GPMC to communicate with attached memories or devices are programmable on a chip-select basis. Assertion and deassertion times of control signals are defined to match the attached memory or device timing specifications and to get maximum performance during accesses. For more information on GPMC_CLK and GPMC_FCLK see Section 15.4.4.10.6, *GPMC_CLK*.

NOTE: In the following sections, the start access time refer to the time at which the access begins.

15.4.4.10.1 Read Cycle Time and Write Cycle Time (RDCYCLETIME / WRCYCLETIME)

The GPMC_CONFIG5_i[4:0] RDCYCLETIME and GPMC_CONFIG5_i[12:8] WRCYCLETIME fields (i = 0 to 7) define the address bus and byte enables valid times for read and write accesses. To ensure a correct duty cycle of GPMC_CLK between accesses, RDCYCLETIME and WRCYCLETIME are expressed in GPMC_FCLK cycles and must be multiples of the GPMC_CLK cycle. RDCYCLETIME and WRCYCLETIME bit fields can be set with a granularity of 1 or 2 throught GPMC_CONFIG1_i[4] TIMEPARAGRANULARITY.

When either RDCYCLETIME or WRCYCLETIME completes, if they are not already deasserted, all control signals (nCS, nADV/ALE, nOE/RE, nWE, and BE0/CLE) are deasserted to their reset values, regardless of their deassertion time parameters.

An exception to this forced deassertion occurs when a pipelined request to the same chip-select or to a different chip-select is pending. In such a case, it is not necessary to deassert a control signal with deassertion time parameters equal to the cycle-time parameter. This exception to forced deassertion prevents any unnecessary glitches. This requirement also applies to BE signals, thus avoiding an unnecessary BE glitch transition when pipelining requests.

NOTE: All control signals (CS, ADV#/ALE, BE0#/CLE, WE#, and GPMC.CLK) are kept inactive (ADV#/ALE, BE0#/CLE, and GPMC.CLK at low level; and CS, OE#/RE, and WE at high level) during the idle GPMC.FCLK cycles.

If no inactive cycles are required between successive accesses to the same or to a different chip-select (GPMC_CONFIG6_i[7] CYCLE2CYCLESAMECSEN = 0 or GPMC_CONFIG6_i[6] CYCLE2CYCLEDIFFCSEN = 0, where i = 0 to 7), and if assertion-time parameters associated with the pipelined access are equal to 0, asserted control signals (nCS, nADV/ALE, nBE0/CLE, nWE, and nOE/RE) are kept asserted. This applies to any read/write to read/write access combination.

If inactive cycles are inserted between successive accesses, that is, CYCLE2CYCLESAMECSEN = 1 or CYCLE2CYCLEDIFFCSEN = 1, the control signals are forced to their respective default reset values for the number of GPMC_FCLK cycles defined in CYCLE2CYCLEDELAY.

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15.4.4.10.2 nCS: Chip-Select Signal Control Assertion/Deassertion Time (CSONTIME / CSRDOFFTIME / CSWROFFTIME / CSEXTRADELAY)

The GPMC_CONFIG2_i[3:0] CSONTIME field (where i = 0 to 7) defines the nCS signal-assertion time relative to the start access time. It is common for read and write accesses.

GPMC_CONFIG2_i[12:8] CSRDOFFTIME (read access) and GPMC_CONFIG2_i[20:16] CSWROFFTIME (write access) bit fields define the nCS signal deassertion time relative to start access time.

CSONTIME, CSRDOFFTIME and CSWROFFTIME parameters are applicable to synchronous and asynchronous modes. CSONTIME can be used to control an address and byte enable setup time before chip-select assertion. CSRDOFFTIME and CSWROFFTIME can be used to control an address and byte enable hold time after chip-select deassertion.

nCS signal transitions as controlled through CSONTIME, CSRDOFFTIME, and CSWROFFTIME can be delayed by half a GPMC_FCLK period by enabling the GPMC_CONFIG2_i[7] CSEXTRADELAY bit. This half of a GPMC_FCLK period provides more granularity on the nCS assertion and deassertion time to guarantee proper setup and hold time relative to GPMC_CLK. CSEXTRADELAY is especially useful in configurations where GPMC_CLK and GPMC_FCLK have the same frequency, but can be used for all GPMC configurations. If enabled, CSEXTRADELAY applies to all parameters controlling nCS transitions.

The CSEXTRADELAY bit must be used carefully to avoid control-signal overlap between successive accesses to different chip-selects. This implies the need to program the RDCYCLETIME and WRCYCLETIME bit fields to be greater than the nCS signal-deassertion time, including the extra half-GPMC_FCLK-period delay.

15.4.4.10.3 nADV/ALE: Address Valid/Address Latch Enable Signal Control Assertion/Deassertion Time (ADVONTIME / ADVRDOFFTIME / ADVWROFFTIME / ADVEXTRADELAY/ADVAADMUXONTIME/ADVAADMUXRDOFFTIME/ADVAADMUXWROFFTIME)

The GPMC_CONFIG3_i[3:0] ADVONTIME field (where i = 0 to 7) defines the nADV/ALE signal-assertion time relative to start access time. It is common to read and write accesses.

GPMC_CONFIG3_i[12:8] ADVRDOFFTIME (read access) and GPMC_CONFIG3_i[20:16] ADVWROFFTIME (write access) bit fields define the nADV/ALE signal-deassertion time relative to start access time.

ADVONTIME can be used to control an address and byte enable valid setup time control before nADV/ALE assertion. ADVRDOFFTIME and ADVWROFFTIME can be used to control an address and byte enable valid hold time control after nADV/ALE de-assertion. ADVRDOFFTIME and ADVWROFFTIME are applicable to both synchronous and asynchronous modes.

nADV/ALE signal transitions as controlled through ADVONTIME, ADVRDOFFTIME, and ADVWROFFTIME can be delayed by half a GPMC_FCLK period by enabling the GPMC_CONFIG3_i[7] ADVEXTRADELAY bit. This half of a GPMC_FCLK period provides more granularity on nADV/ALE assertion and deassertion time to guarantee proper setup and hold time relative to GPMC_CLK. The ADVEXTRADELAY configuration parameter is especially useful in configurations where GPMC_CLK and GPMC_FCLK have the same frequency, but can be used for all GPMC configurations. If enabled, ADVEXTRADELAY applies to all parameters controlling nADV/ALE transitions.

ADVEXTRADELAY must be used carefully to avoid control-signal overlap between successive accesses to different chip-selects. This implies the need to program the RDCYCLETIME and WRCYCLETIME bit fields to be greater than nADV/ALE signal-deassertion time, including the extra half-GPMC_FCLK-period delay.

GPMC_CONFIG3_i[6:4] ADVAADMUXONTIME, GPMC_CONFIG3_i[26:24] ADVAADMUXRDOFFTIME, and GPMC_CONFIG3_i[30:28] ADVAADMUXWROFFTIME parameters have the same functions as ADVONTIME, ADVRDOFFTIME, and ADVWROFFTIME, but apply to the first address phase in the AAD-multiplexed protocol. It is the user responsibility to make sure ADVAADMUXxxOFFTIME is programmed to a value lower than or equal to ADVxxOFFTIME. Functionality in AAD-mux mode is undefined if the settings do not comply with this requirement. ADVAADMUXxxOFFTIME can be programmed to the same value as ADVONTIME if no high nADV pulse is needed between the two AAD-mux address phases, which is the typical case in synchronous mode. In this configuration, nADV is kept low until it reaches the correct ADVxxOFFTIME.

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See Section 15.4.4.13, *NAND Access Description* for more details on ADVONTIME, ADVRDOFFTIME, ADVWROFFTIME, and ADVAADMUXRDOFFTIME, ADVAADMUXWROFFTIME usage for CLE and ALE (Command / Address Latch Enable) usage for a NAND Flash interface.

15.4.4.10.4 nOE/nRE: Output Enable / Read Enable Signal Control Assertion / Deassertion Time (OEONTIME / OEOFFTIME / OEEXTRADELAY / OEAADMUXONTIME / OEAADMUXOFFTIME)

The GPMC_CONFIG4_i[3:0] OEONTIME field (where i = 0 to 7) defines the nOE/nRE signal assertion time relative to start access time. It is applicable only to read accesses.

The GPMC_CONFIG4_i[12:8] OEOFFTIME field defines the nOE/nRE signal deassertion time relative to start access time. It is applicable only to read accesses. nOE/nRE is not asserted during a write cycle.

OEONTIME, OEOFFTIME, OEAADMUXONTIME and OEAADMUXOFFTIME parameters are applicable to synchronous and asynchronous modes. OEONTIME can be used to control an address and byte enable valid setup time control before nOE/nRE assertion. OEOFFTIME can be used to control an address and byte enable valid hold time control after nOE/nRE assertion.

OEAADMUXONTIME and OEAADMUXOFFTIME parameters have the same functions as OEONTIME and OEOFFTIME, but apply to the first OE assertion in the AAD-multiplexed protocol for a read phase, or to the only OE assertion for a write phase. It is the user responsibility to make sure OEAADMUXOFFTIME is programmed to a value lower than OEONTIME. Functionality in AAD-mux mode is undefined if the settings do not comply with this requirement. OEAADMUXOFFTIME shall never be equal to OEONTIME because the AAD-mux protocol requires a second address phase with the nOE signal deasserted before nOE can be asserted again to define a read command.

The nOE/RE signal transitions as controlled through OEONTIME, OEOFFTIME, OEAADMUXONTIME and OEAADMUXOFFTIME can be delayed by half a GPMC_FCLK period by enabling the GPMC_CONFIG4_i[7] OEEXTRADELAY bit. This half of a GPMC_FCLK period provides more granularity on nOE/RE assertion and deassertion time to guaranty proper setup and hold time relative to GPMC_CLK. If enabled, OEEXTRADELAY applies to all parameters controlling nOE/nRE transitions.

OEEXTRADELAY must be used carefully, to avoid control-signal overlap between successive accesses to different chip-selects. This implies the need to program RDCYCLETIME and WRCYCLETIME to be greater than nOE/RE signal-deassertion time, including the extra half-GPMC_FCLK-period delay.

NOTE: When the GPMC generates a read access to an address-/data-multiplexed device, it drives the address bus until nOE assertion time.

15.4.4.10.5 nWE: Write Enable Signal Control Assertion / Deassertion Time (WEONTIME / WEOFFTIME / WEEXTRADELAY)

The GPMC_CONFIG4_i[19:16] WEONTIME field (where i = 0 to 7) defines the nWE signal-assertion time relative to start access time. The GPMC_CONFIG4_i[28:24] WEOFFTIME field defines the nWE signal-deassertion time relative to start access time. These bit fields only apply to write accesses. nWE is not asserted during a read cycle.

WEONTIME can be used to control an address and byte enable valid setup time control before nWE assertion. WEOFFTIME can be used to control an address and byte enable valid hold time control after nWE assertion.

nWE signal transitions as controlled through WEONTIME, and WEOFFTIME can be delayed by half a GPMC_FCLK period by enabling the GPMC_CONFIG4_i[23] WEEXTRADELAY bit. This half of a GPMC_FCLK period provides more granularity on nWE assertion and deassertion time to guaranty proper setup and hold time relative to GPMC_CLK. If enabled, WEEXTRADELAY applies to all parameters controlling nWE transitions.

The WEEXTRADELAY bit must be used carefully to avoid control-signal overlap between successive accesses to different chip-selects. This implies the need to program the WRCYCLETIME bit field to be greater than the nWE signal-deassertion time, including the extra half-GPMC_FCLK-period delay.

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15.4.4.10.6 GPMC_CLK

GPMC_CLK is the external clock provided to the attached synchronous memory or device.

- The GPMC_CLK clock frequency is the GPMC_FCLK functional clock frequency divided by 1, 2, 3, or 4, depending on the GPMC_CONFIG1_i[1:0] GPMCFCLKDIVIDER bit field (where i = 0 to 7), with a guaranteed 50-percent duty cycle.
- The GPMC_CLK clock is only activated when the access in progress is defined as synchronous (read or write access).
- The GPMC_CONFIG1_i[26:25] CLKACTIVATIONTIME field (i = 0 to 7) defines the number of GPMC_FCLK cycles from start access time to GPMC_CLK activation.
- The GPMC_CLK clock is stopped when cycle time completes and is asserted low between accesses.
- The GPMC_CLK clock is kept low when access is defined as asynchronous.

CAUTION

When cycle time completes, the GPMC_CLK may be high because of the GPMCFCLKDIVIDER bit field. To ensure correct stoppage of the GPMC_CLK clock within the 50-percent required duty cycle, it is the user's responsibility to extend the RDCYCLETIME or WRCYCLETIME value.

NOTE: To ensure a correct external clock cycle, the following rules must be applied:

- (RDCYCLETIME CLKACTIVATIONTIME) must be a multiple of (GPMCFCLKDIVIDER + 1).
- The PAGEBURSTACCESSTIME value must be a multiple of (GPMCFCLKDIVIDER + 1).

15.4.4.10.7 GPMC_CLK and Control Signals Setup and Hold

Control-signal transition (assertion and deassertion) setup and hold values with respect to the GPMC_CLK edge can be controlled in the following ways:

- For the GPMC_CLK signal, the GPMC_CONFIG1_i[26:25] CLKACTIVATIONTIME field (i = 0 to 7) allows setup and hold control of control-signal assertion time.
- The use of a divided GPMC_CLK allows setup and hold control of control-signal assertion and deassertion times.
- When GPMC_CLK runs at the GPMC_FCLK frequency so that GPMC_CLK edge and control-signal transitions refer to the same GPMC_FCLK edge, the control-signal transitions can be delayed by half of a GPMC_FCLK period to provide minimum setup and hold times. This half-GPMC_FCLK delay is enabled with the CSEXTRADELAY, ADVEXTRADELAY, OEEXTRADELAY, or WEEXTRADELAY parameter. This delay must be used carefully to prevent control-signal overlap between successive accesses to different chip-selects. This implies that the RDCYCLETIME and WRCYCLETIME are greater than the last control-signal deassertion time, including the extra half-GPMC_FCLK cycle.

15.4.4.10.8 Access Time (RDACCESSTIME / WRACCESSTIME)

The read access time and write access time durations can be programmed independently through GPMC_CONFIG5_i[20:16] RDACCESSTIME and GPMC_CONFIG6_i[28:24] WRACCESSTIME (i = 0 to 7). This allows nOE and GPMC data capture timing parameters to be independent of nWE and memory device data capture timing parameters. RDACCESSTIME and WRACCESSTIME bit fields can be set with a granularity of 1 or 2 throught GPMC_CONFIG1_i[4] TIMEPARAGRANULARITY.

15.4.4.10.8.1 Access Time on Read Access

In asynchronous read mode, for single and paged accesses, GPMC_CONFIG5_i[20:16] RDACCESSTIME field (i = 0 to 7) defines the number of GPMC_FCLK cycles from start access time to the GPMC_FCLK rising edge used for the first data capture. RDACCESSTIME must be programmed to the rounded greater value (in GPMC_FCLK cycles) of the read access time of the attached memory device.

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In synchronous read mode, for single or burst accesses, RDACCESSTIME defines the number of GPMC_FCLK cycles from start access time to the GPMC_FCLK rising edge corresponding to the GPMC_CLK rising edge used for the first data capture.

GPMC_CLK which is sent to the memory device for synchronization with the GPMC controller, is internally retimed to correctly latch the returned data. GPMC_CONFIG5_i[4:0] RDCYCLETIME must be greater than RDACCESSTIME in order to let the GPMC latch the last return data using the internally retimed GPMC_CLK.

The external WAIT signal can be used in conjunction with RDACCESSTIME to control the effective GPMC data-capture GPMC_FCLK edge on read access in both asynchronous mode and synchronous mode. For details about wait monitoring, see Section 15.4.4.9.3.1, *Chip-Select Base Address and Region Size*.

15.4.4.10.8.2 Access Time on Write Access

In asynchronous write mode, the GPMC_CONFIG6_i[28:24] WRACCESSTIME timing parameter is not used to define the effective write access time. Instead, it is used as a WAIT invalid timing window, and must be set to a correct value so that the gpmc_wait pin is at a valid state two GPMC_CLK cycles before WRACCESSTIME completes. For details about wait monitoring, see Section 15.4.4.9.3.1, *Chip-Select Base Address and Region Size*.

In synchronous write mode , for single or burst accesses, WRACCESSTIME defines the number of GPMC_FCLK cycles from start access time to the GPMC_CLK rising edge used by the memory device for the first data capture.

The external WAIT signal can be used in conjunction with WRACCESSTIME to control the effective memory device data capture GPMC_CLK edge for a synchronous write access. For details about wait monitoring, see Section 15.4.4.9.3.1, *Chip-Select Base Address and Region Size*.

15.4.4.10.9 Page Burst Access Time (PAGEBURSTACCESSTIME)

GPMC_CONFIG5_i[27:24] PAGEBURSTACCESSTIME bit field (i = 0 to 7) can be set with a granularity of 1 or 2 throught GPMC_CONFIG1_i[4] TIMEPARAGRANULARITY.

15.4.4.10.9.1 Page Burst Access Time on Read Access

In asynchronous page read mode, the delay between successive word captures in a page is controlled through the PAGEBURSTACCESSTIME bit field. The PAGEBURSTACCESSTIME parameter must be programmed to the rounded greater value (in GPMC_FCLK cycles) of the read access time of the attached device.

In synchronous burst read mode, the delay between successive word captures in a burst is controlled through the PAGEBURSTACCESSTIME field.

The external WAIT signal can be used in conjunction with PAGEBURSTACCESSTIME to control the effective GPMC data capture GPMC_FCLK edge on read access. For details about wait monitoring, see Section 15.4.4.9.3.1, *Chip-Select Base Address and Region Size*.

15.4.4.10.9.2 Page Burst Access Time on Write Access

Asynchronous page write mode is not supported. PAGEBURSTACCESSTIME is irrelevant in this case.

In synchronous burst write mode, PAGEBURSTACCESSTIME controls the delay between successive memory device word captures in a burst.

The external WAIT signal can be used in conjunction with PAGEBURSTACCESSTIME to control the effective memory-device data capture GPMC_CLK edge in synchronous write mode. For details about wait monitoring, see Section 15.4.4.9.3.1, *Chip-Select Base Address and Region Size*.

15.4.4.10.10 Bus Keeping Support

At the end-cycle time of a read access, if no other access is pending, the GPMC drives the bus with the last data read after RDCYCLETIME completion time to prevent bus floating and reduce power consumption.

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After a write access, if no other access is pending, the GPMC keeps driving the data bus after WRCYCLETIME completes with the same data to prevent bus floating and power consumption.

15.4.4.11 NOR Access Description

For each chip-select configuration, the read access can be specified as either asynchronous or synchronous access through the GPMC_CONFIG1_i[29] READTYPE bit (i = 0 to 7). For each chip-select configuration, the write access can be specified as either synchronous or asynchronous access through the GPMC_CONFIG1_i[27] WRITETYPE bit (i = 0 to 7).

Asynchronous and synchronous read and write access time and related control signals are controlled through timing parameters that refer to GPMC_FCLK. The primary difference of synchronous mode is the availability of a configurable clock interface (GPMC_CLK) to control the external device. Synchronous mode also affects data-capture and wait-pin monitoring schemes in read access.

For details about asynchronous and synchronous access, see the descriptions of GPMC_CLK, RdAccessTime, WrAccessTime, and wait-pin monitoring.

For more information about timing-parameter settings, see the sample timing diagrams in this chapter.

NOTE: The address bus and nBE[1:0] are fixed for the duration of a synchronous burst read access, but they are updated for each beat of an asynchronous page-read access.

15.4.4.11.1 Asynchronous Access Description

This section describes:

- Asynchronous single-read operation on an address/data multiplexed device
- Asynchronous single write operation on an address/data-multiplexed device
- Asynchronous single read operation on an AAD-multiplexed device
- Asynchronous single write operation on an AAD-multiplexed device
- Asynchronous multiple (page) read operation on a non-multiplexed device

In asynchronous operations GPMC_CLK is not provided outside the GPMC and is kept low.

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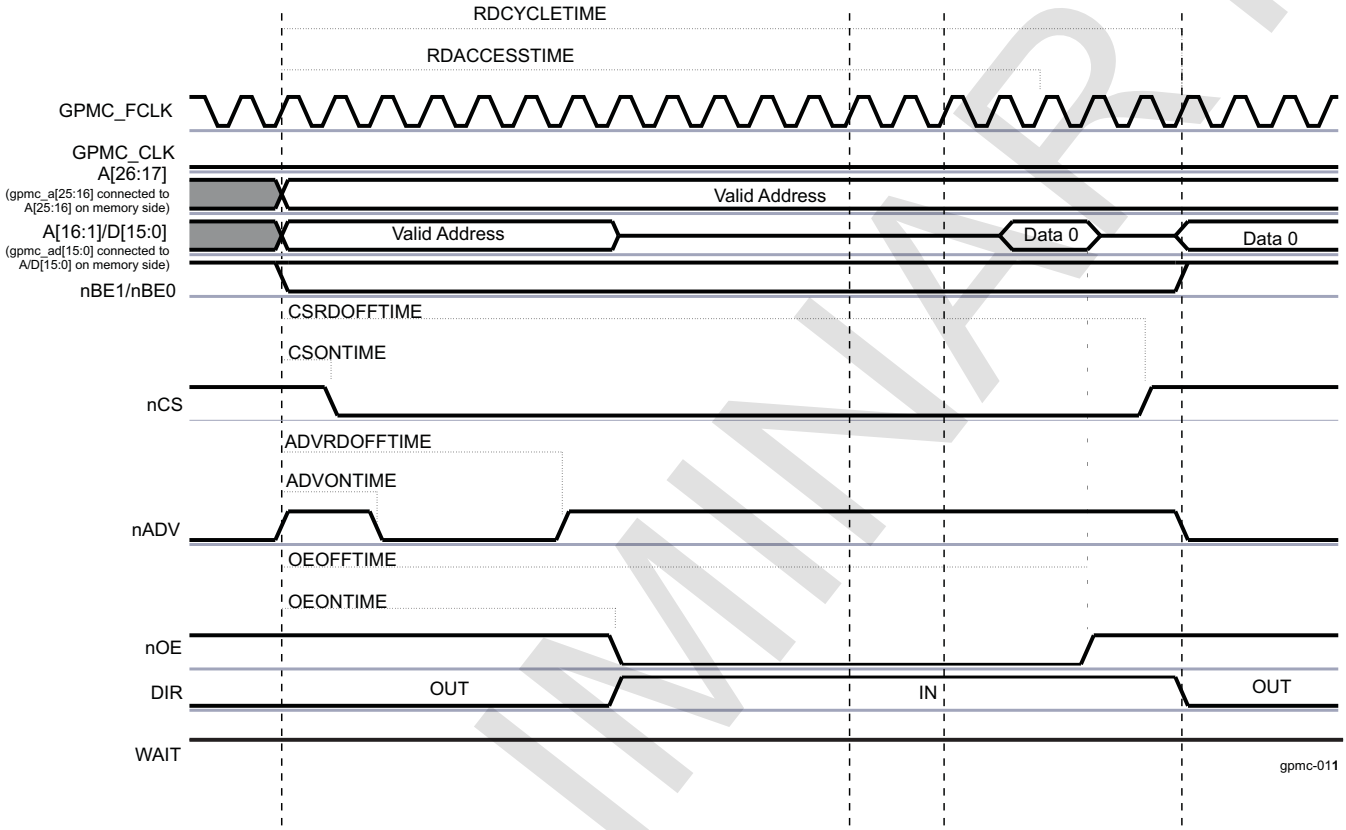
15.4.4.11.1.1 Access on Address/Data Multiplexed Devices

15.4.4.11.1.1.1 Asynchronous Single-Read Operation on an Address/Data Multiplexed Device

Figure 15-61 shows an asynchronous single read operation on an address/data-multiplexed device.

Figure 15-61. Asynchronous Single Read on an Address/Data-Multiplexed Device



See Section 15.4.5.6.1, *GPMC Timing Parameters Formulas* for formulas to calculate timing parameters.

Table 15-257 lists the timing bit fields to set up in order to configure the GPMC in asynchronous single read mode.

When the GPMC generates a read access to an address/data-multiplexed device, it drives the address bus until nOE assertion time. For details, see Section 15.4.4.9.2.3, *Address/Data-Multiplexing Interface*.

Address bits (A[16:1] from a GPMC perspective, A[15:0] from an external device perspective) are placed on the address/data bus, and the remaining address bits gpmc_a[25:16] are placed on the address bus. The address phase ends at nOE assertion, when the DIR signal goes from OUT to IN.

- Chip-select signal nCS:
  - nCS assertion time is controlled by the GPMC_CONFIG2_i[3:0] CSONTIME field. It controls the address setup time to nCS assertion.
  - nCS deassertion time is controlled by the GPMC_CONFIG2_i[12:8] CSRDOFFTIME field. It controls the address hold time from nCS deassertion.
- Address valid signal nADV:
  - nADV assertion time is controlled by the GPMC_CONFIG3_i[3:0] ADVONTIME field.
  - nADV deassertion time is controlled by the GPMC_CONFIG3_i[12:8] ADVRDOFFTIME field.
- Output enable signal nOE:
  - nOE assertion indicates a read cycle.
  - nOE assertion time is controlled by the GPMC_CONFIG4_i[3:0] OEONTIME field.

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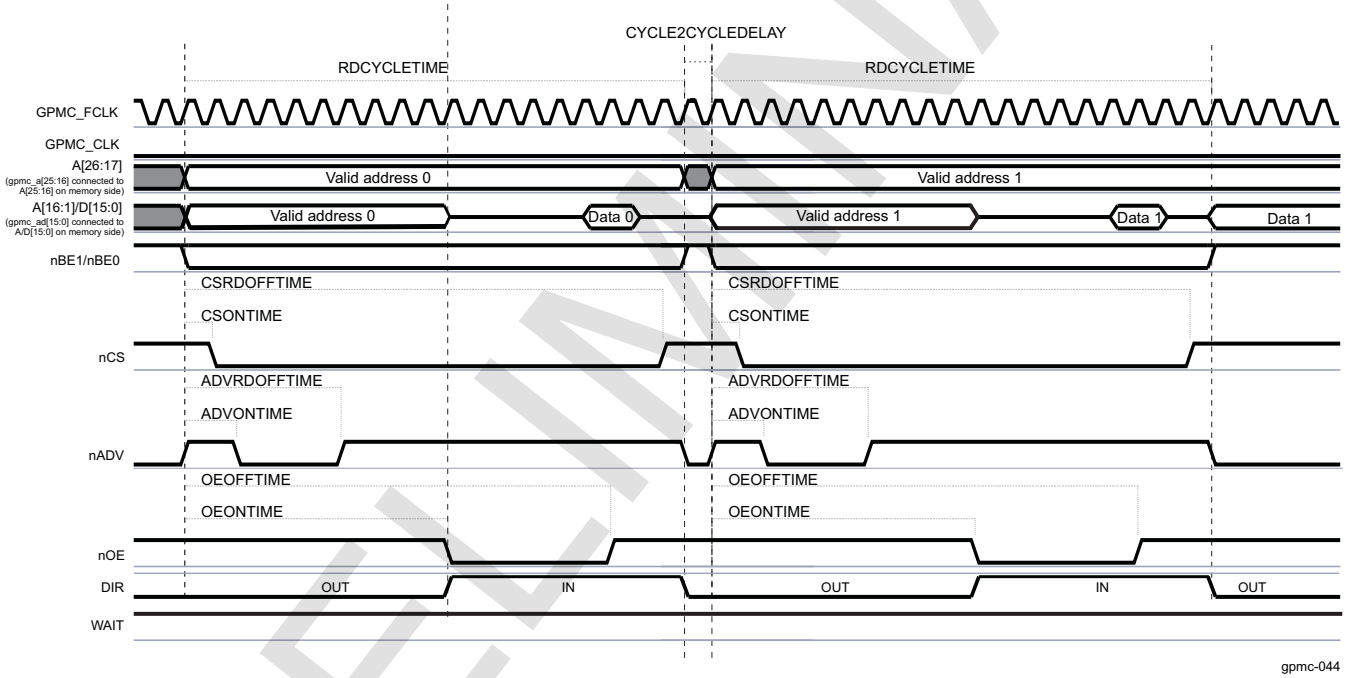
  - nOE deassertion time is controlled by the GPMC_CONFIG4_i[12:8] OEOFFTIME field.
- Read data is latched when RDACCESSTIME completes. Access time is defined in the GPMC_CONFIG5_i[20:16] RDACCESSTIME field.
- Direction signal DIR: DIR goes from OUT to IN at the same time that nOE is asserted.
- The end of the access is defined by the GPMC_CONFIG5_i[4:0] RDCYCLETIME parameter.

In the GPMC, when a 16-bit wide device is attached to the controller, a 32-bit word write access is split into two 16-bit word write accesses. For more information about GPMC access size and type adaptation, see Section 15.4.4.11.5, *System Burst Versus External Device Burst Support*.

Between two successive accesses, if an nCS pulse is needed:

- The GPMC_CONFIG6_i[11:8] CYCLE2CYCLEDELAY field can be programmed with GPMC_CONFIG6_i[7] CYCLE2CYCLESAMECSEN enabled.
- The CSWROFFTIME and CSONTIME parameters also allow a chip-select pulse, but this affects all other types of access.

Figure 15-62. Two Asynchronous Single Read Accesses on an Address/Data Multiplexed Device (32-bit read split into 2 x 16-bit read)



15.4.4.11.1.1.2 Asynchronous Single Write Operation on an Address/Data-Multiplexed Device

Figure 15-63 shows an asynchronous single write operation on an address/data-multiplexed device.

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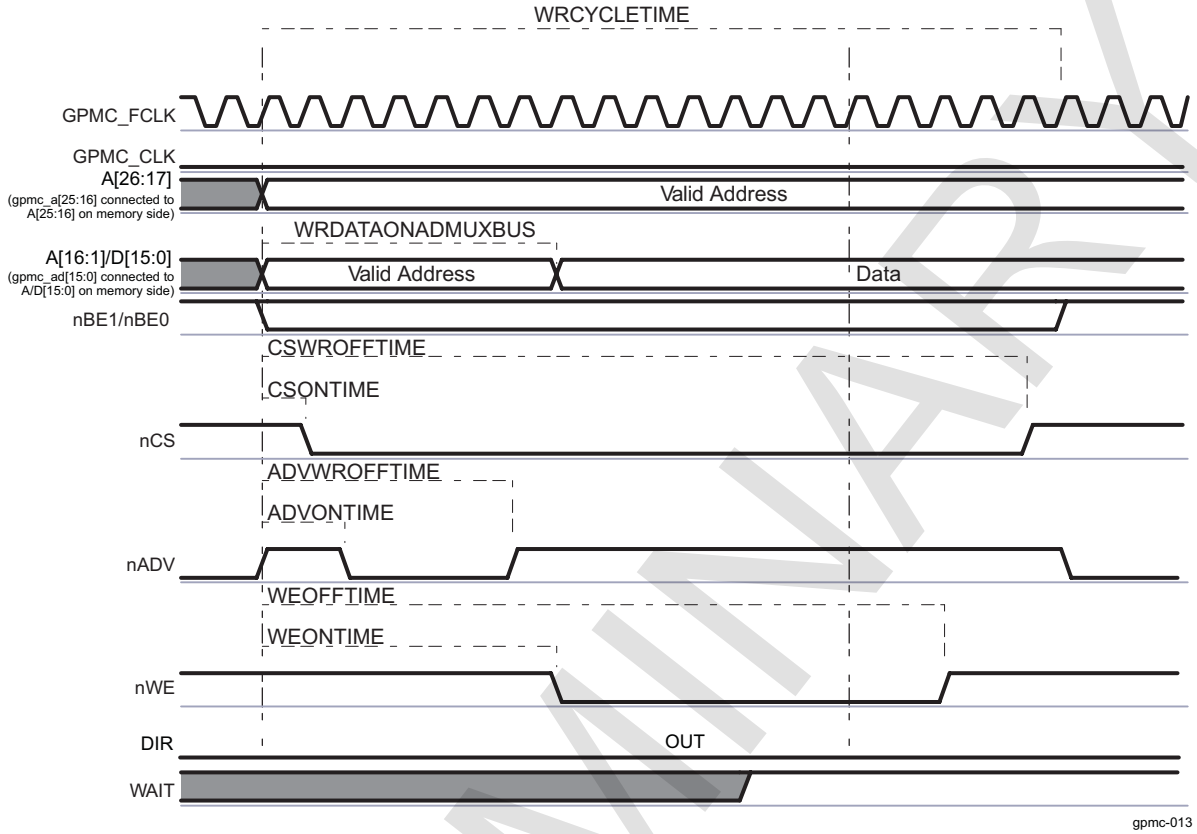
Figure 15-63. Asynchronous Single Write on an Address/Data-Multiplexed Device



See Section 15.4.5.6.1, *GPMC Timing Parameterss Formulas* for formulas to calculate timing parameters.

Table 15-257 lists the timing bit fields to set up in order to configure the GPMC in asynchronous single write mode.

When the GPMC generates a write access to an address/data-multiplexed device, it drives the address bus until nWE assertion time. For more information, see Section 15.4.4.9.2.3, *Address/Data-Multiplexing Interface*.

The nCS, and nADV signals are controlled in the same way as for asynchronous single read operation on an address/data-multiplexed device.

- Write enable signal nWE:
  - nWE assertion indicates a write cycle.
  - nWE assertion time is controlled by the GPMC_CONFIG4_i[19:16] WEONTIME field.
  - nWE deassertion time is controlled by the GPMC_CONFIG4_i[28:24] WEOFFTIME field.
- Direction signal DIR: DIR signal is OUT during the entire access.
- The end of the access is defined by the GPMC_CONFIG5_i[12:8] WRCYCLETIME parameter.

Address bits A[16:1] (GPMC point of view) are placed on the address/data bus at the start of cycle time, and the remaining address bits A[26:17] are placed on the address bus.

Data is driven on the address/data bus at a GPMC_CONFIG6_i[19:16] WRDATAONADMUXBUS time.

NOTE: Write multiple access in asynchronous mode is not supported. If WRITEMULTIPLE is enabled with WRITETYPE as asynchronous, the GPMC processes single asynchronous accesses.

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After a write operation, if no other access (read or write) is pending, the data bus keeps its previous value. See Section 15.4.4.10.10, *Bus Keeping Support*.

15.4.4.11.1.1.3 Asynchronous Multiple (Page) Write Operation on an Address/Data-Multiplexed Device

Write multiple (page) access in asynchronous mode is not supported for address/data-multiplexed devices.

If GPMC_CONFIG1_i[28] WRITEMULTIPLE is enabled (0x1) with GPMC_CONFIG1_i[27] WRITETYPE as asynchronous (0x0), the GPMC processes single asynchronous accesses.

For accesses on non-multiplexed devices refer to Section 15.4.4.11.3, *Asynchronous and Synchronous Accesses in Nonmultiplexed Mode*.

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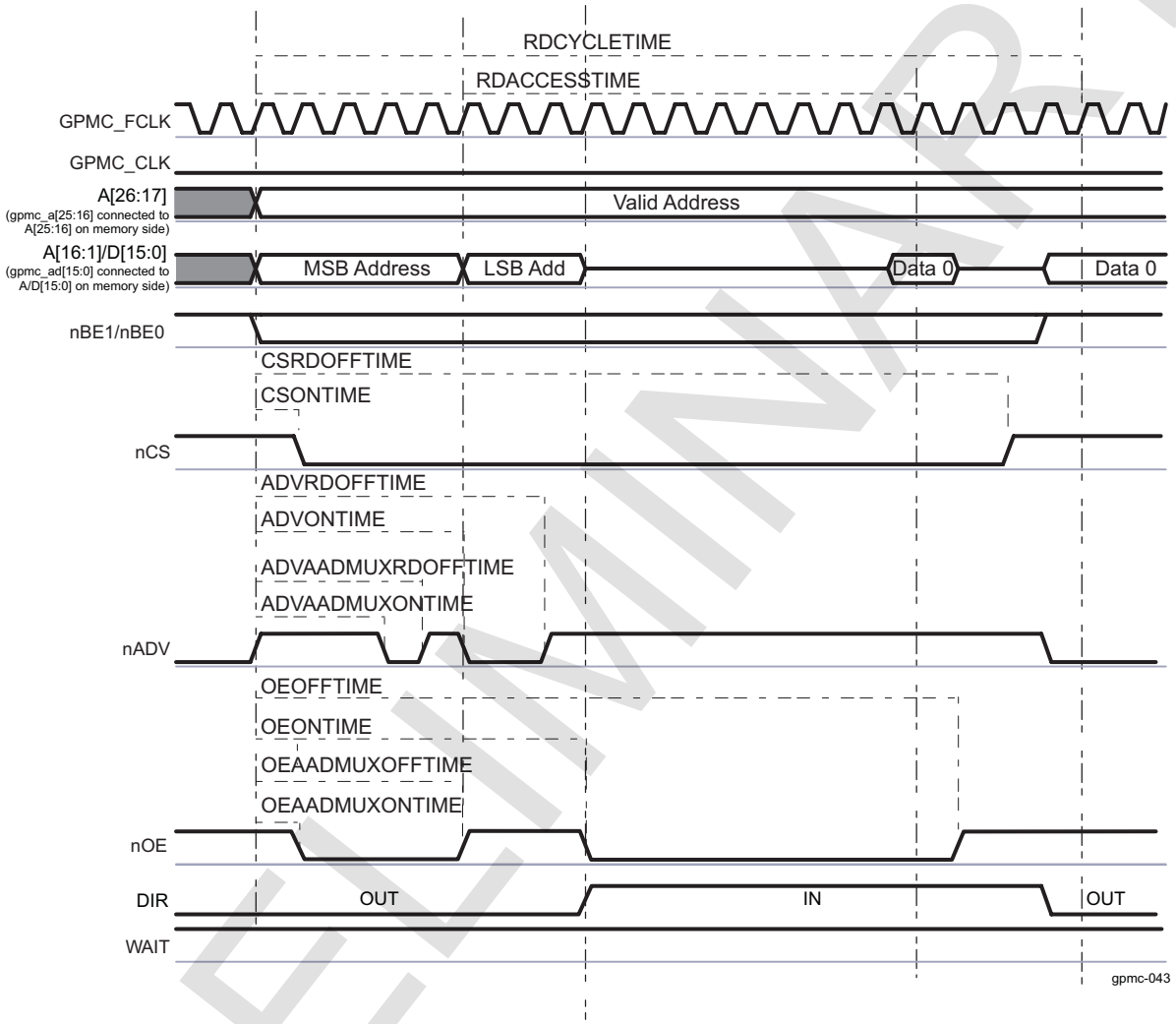
15.4.4.11.1.2 Access on Address/Address/Data Multiplexed Devices

15.4.4.11.1.2.1 Asynchronous Single Read Operation on an AAD-Multiplexed Device

Figure 15-64 shows an asynchronous single read operation on an AAD-multiplexed device.

Figure 15-64. Asynchronous Single Read on an AAD-Multiplexed Device



See Section 15.4.5.6.1, *GPMC Timing Parameterss Formulas* for formulas to calculate timing parameters.

Table 15-257 lists the timing bit fields to set up in order to configure the GPMC in asynchronous single write mode.

When the GPMC generates a read access to an AAD-multiplexed device, all address bits are driven onto the address/data bus in two separate phases. The first phase is used for the MSB address and is qualified with nOE driven low. The first address phase ends at the first nOE deassertion time. The second phase for LSB address is qualified with nOE driven high. The second address phase ends at the second nOE assertion time, when the DIR signal goes from OUT to IN.

The nCS, and DIR signals are controlled in the same way as for asynchronous single read operation on an address/data-multiplexed device.

- Address valid signal nADV. nADV is asserted and deasserted twice during a read transaction:
  - nADV first assertion time is controlled by the GPMC_CONFIG3_i[6:4] ADVAADMUXONTIME field.
  - nADV first deassertion time is controlled by the GPMC_CONFIG3_i[26:24] ADVAADMUXRDOFFTIME field.

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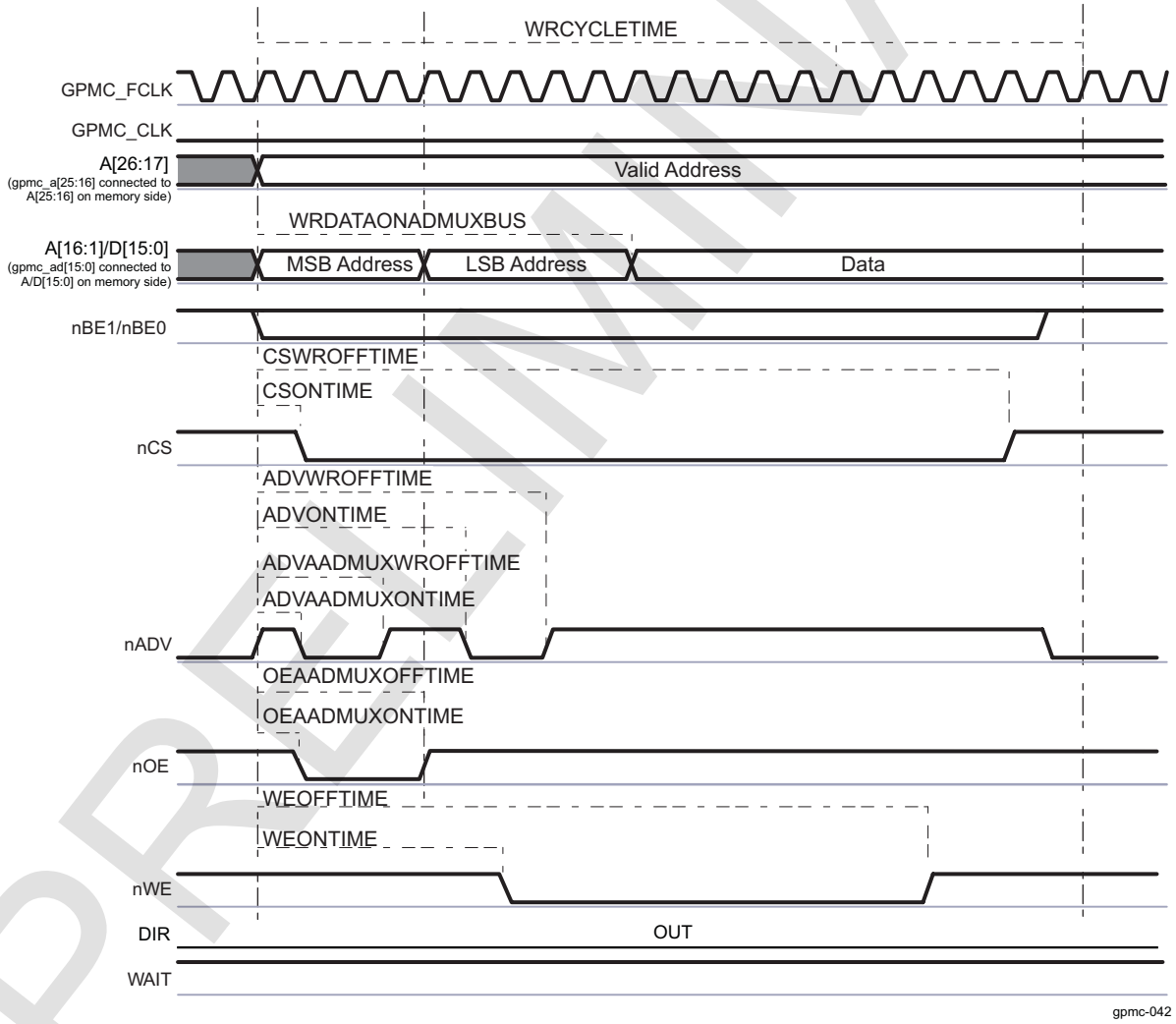
  - nADV second assertion time is controlled by the GPMC_CONFIG3_i[3:0] ADVONTIME field.
  - nADV second deassertion time is controlled by the GPMC_CONFIG3_i[12:8] ADVRDOFFTIME field.
- Output Enable signal nOE. nOE is asserted and deasserted twice during a read transaction (nOE second assertion indicates a read cycle):
  - nOE first assertion time is controlled by the GPMC_CONFIG4_i[6:4] OEAADMUXONTIME field.
  - nOE first deassertion time is controlled by the GPMC_CONFIG3_i[15:13] OEAADMUXOFFTIME field.
  - nOE second assertion time is controlled by the GPMC_CONFIG4_i[3:0] OEONTIME field.
  - nOE second deassertion time is controlled by the GPMC_CONFIG4_i[12:8] OEOFFTIME field.

15.4.4.11.1.2.2 Asynchronous Single Write Operation on an AAD-Multiplexed Device

Figure 15-65 shows an asynchronous single write operation on an AAD-multiplexed device.

Figure 15-65. Asynchronous Single Write on an AAD-Multiplexed Device



See Section 15.4.5.6.1, *GPMC Timing Parameterss Formulas* for formulas to calculate timing parameters.

Table 15-257 lists the timing bit fields to set up in order to configure the GPMC in asynchronous single write mode.

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When the GPMC generates a write access to an AAD-multiplexed device, all address bits are driven onto the address/data bus in two separate phases. The first phase is used for the MSB address and is qualified with nOE driven low. The second phase for LSB address is qualified with nOE driven high. The address phase ends at nWE assertion time.

The nCS, nWE, and DIR signals are controlled in the same way as for asynchronous single write operation on an address/data-multiplexed device. See Table 15-248.

- Address valid signal nADV is asserted and deasserted twice during a write transaction:
  - nADV first assertion time is controlled by the GPMC_CONFIG3_i[6:4] ADVAADMUXONTIME field.
  - nADV first deassertion time is controlled by the GPMC_CONFIG3_i[30:28] ADVAADMUXWROFFTIME field.
  - nADV second assertion time is controlled by the GPMC_CONFIG3_i[3:0] ADVONTIME field.
  - nADV second deassertion time is controlled by the GPMC_CONFIG3_i[20:16] ADVWROFFTIME field.
- Output Enable signal nOE is asserted during the address phase of a write transaction:
  - nOE assertion time is controlled by the GPMC_CONFIG4_i[6:4] OEAADMUXONTIME field.
  - nOE deassertion time is controlled by the GPMC_CONFIG3_i[15:13] OEAADMUXOFFTIME field.

The address bits for the first address phase are driven onto the data bus until nOE deassertion. Data is driven onto the address/data bus at the clock edge defined by the GPMC_CONFIG6_i[19:16] WRDATAONADMUXBUS parameter.

15.4.4.11.1.2.3 Asynchronous Multiple (Page) Read Operation on an AAD-Multiplexed Device

Write multiple (page) access in asynchronous mode is not supported for AAD-multiplexed devices.

If GPMC_CONFIG1_i[28] WRITEMULTIPLE is enabled (0x1) with GPMC_CONFIG1_i[27] WRITETYPE as asynchronous (0x0), the GPMC processes single asynchronous accesses.

For accesses on non-multiplexed devices refer to Section 15.4.4.11.3, *Asynchronous and Synchronous Accessed in Nonmultiplexed Mode*.

15.4.4.11.2 Synchronous Access Description

This section details read and write synchronous accesses on address/data multiplexed. All information in this section can be applied to any type of memory - non-multiplexed, address and data multiplexed or AAD-multiplexed - with a difference limited to the address phase. For accesses on non-multiplexed devices refer to Section 15.4.4.11.3, *Asynchronus and Synchronus Accessed in Nonmultiplexed Mode*.

In synchronous operations:

- The GPMC_CLK clock is provided outside the GPMC when accessing the memory device.
- The GPMC_CLK clock is derived from the GPMC_FCLK clock using the GPMC_CONFIG1_i[1:0] GPMCFCLKDIVIDER field. In the following section i stands for the chip-select number, i = 0 to 7.
- The GPMC_CONFIG1_i[26:25] CLKACTIVATIONTIME field specifies that the GPMC_CLK is provided outside the GPMC 0, 1, or 2 GPMC_FCLK cycles after start access time until RDCYCLETIME or WRCYCLETIME completion.

15.4.4.11.2.1 Synchronous Single Read

Figure 15-66 and Figure 15-67 show a synchronous single-read operation with GPMCFCLKDIVIDER equal to 0 and 1, respectively.

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Figure 15-66. Synchronous Single Read (GPMCFCLKDIVIDER = 0)

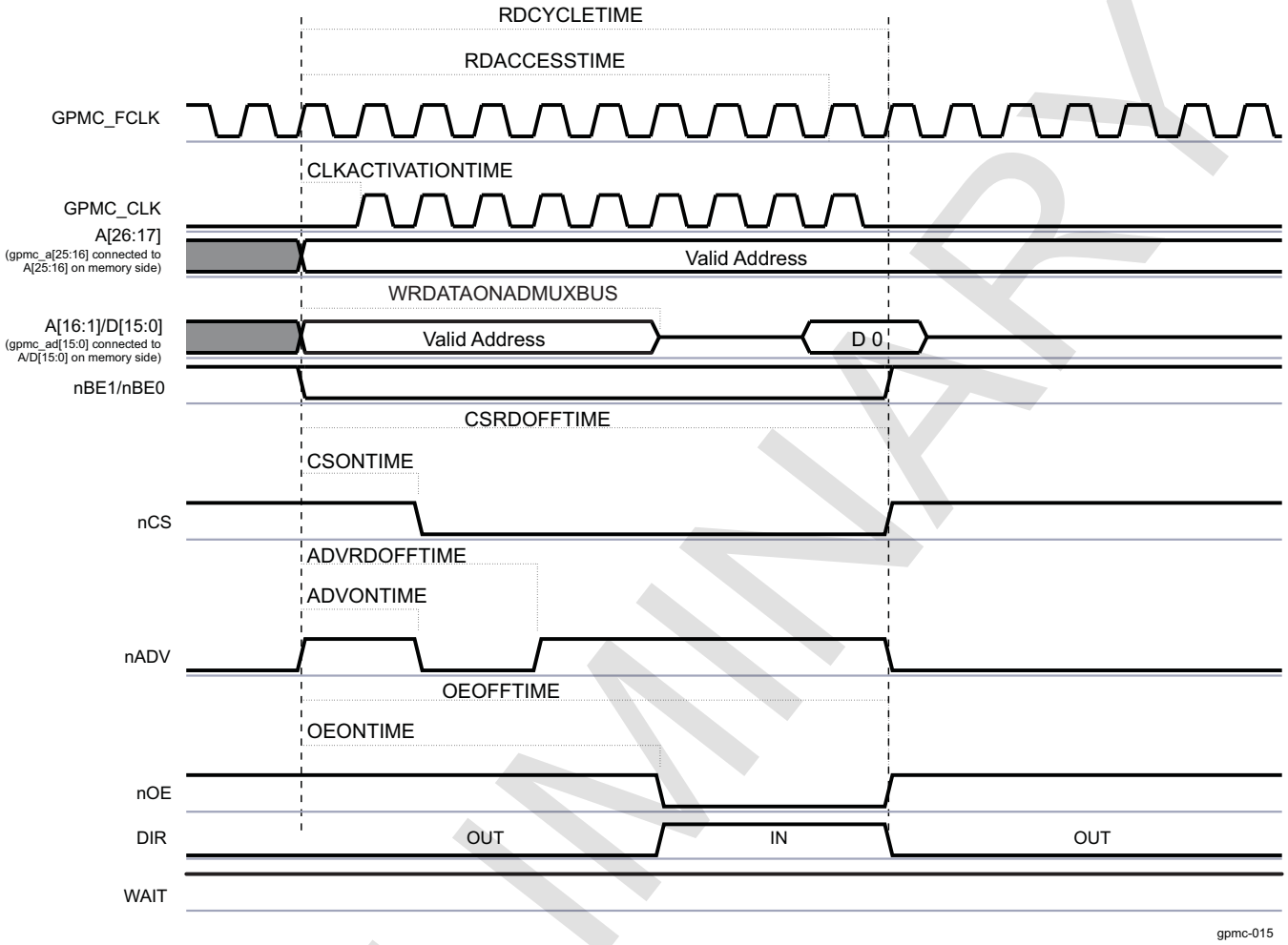

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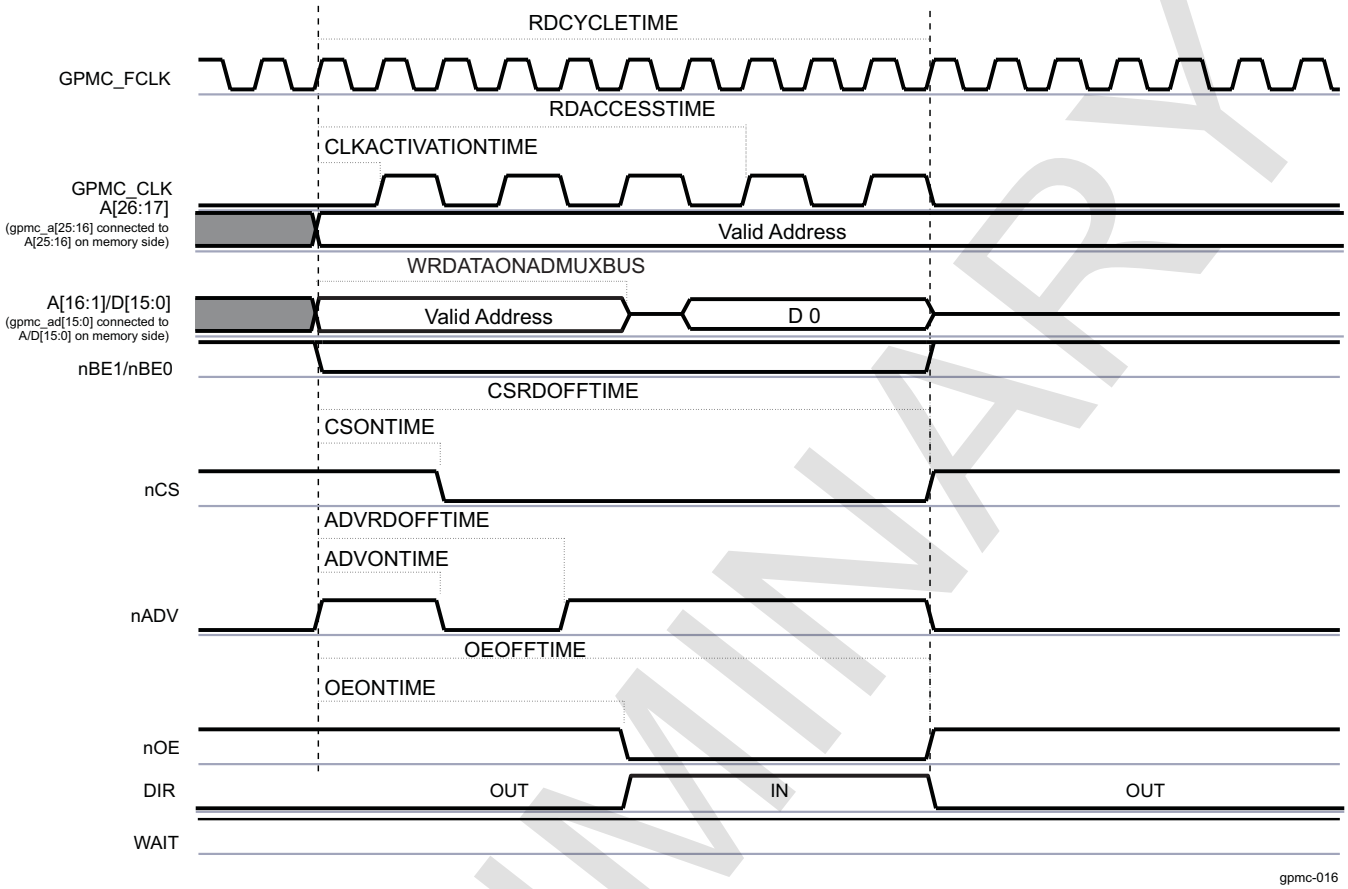
Figure 15-67. Synchronous Single Read (GPMCFCLKDIVIDER = 1)



See Section 15.4.5.6.1, *GPMC Timing Parameterss Formulas* for formulas to calculate timing parameters.

Table 15-257 lists the timing bit fields to set up in order to configure the GPMC in asynchronous single read mode.

When the GPMC generates a read access to an address/data-multiplexed device, it drives the address bus until nOE assertion time. For details, see Section 15.4.4.9.2.3, *Address/Data-Multiplexing Interface*.

- Chip-select signal nCS:
  - nCS assertion time is controlled by the GPMC_CONFIG2_i[3:0] CSONTIME field and ensures address setup time to nCS assertion.
  - nCS deassertion time is controlled by the GPMC_CONFIG2_i[12:8] CSRDOFFTIME field and ensures address hold time to nCS deassertion.
- Address valid signal nADV:
  - nADV assertion time is controlled by the GPMC_CONFIG3_i[3:0] ADVONTIME field.
  - nADV deassertion time is controlled by the GPMC_CONFIG3_i[12:8] ADVRDOFFTIME field.
- Output enable signal nOE:
  - nOE assertion indicates a read cycle.
  - nOE assertion time is controlled by the GPMC_CONFIG4_i[3:0] OEONTIME field.
  - nOE deassertion time is controlled by the GPMC_CONFIG4_i[12:8] OEOFFTIME field.
- Initial latency for the first read data is controlled by GPMC_CONFIG5_i[20:16] RDACCESSTIME or by monitoring the WAIT signal.
- Total access time (GPMC_CONFIG5_i[4:0] RDCYCLETIME) corresponds to RDACCESSTIME plus the address hold time from nCS deassertion, plus time from RDACCESSTIME to CSRDOFFTIME.
- Direction signal DIR: DIR goes from OUT to IN at the same time as nOE assertion.

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When the GPMC generates a write access to an AAD-multiplexed device, all address bits are driven onto the address/data bus in two separate phases. The first phase is used for the MSB address and is qualified with nOE driven low. The second phase for LSB address is qualified with nOE driven high. The address phase ends at nWE assertion time.

The nCS, and DIR signals are controlled in the same way as for synchronous single read operation on an address/data-multiplexed device.

- Address valid signal nADV is asserted and deasserted twice during a read transaction:
  - nADV first assertion time is controlled by the GPMC_CONFIG3_i[6:4] ADVAADMUXONTIME field.
  - nADV first deassertion time is controlled by the GPMC_CONFIG3_i[26:24] ADVAADMUXRDOFFTIME field.
  - nADV second assertion time is controlled by the GPMC_CONFIG3_i[3:0] ADVONTIME field.
  - nADV second deassertion time is controlled by the GPMC_CONFIG3_i[12:8] ADVRDOFFTIME field.
- Output Enable signal nOE is asserted and deasserted twice during a read transaction (nOE second assertion indicates a read cycle):
  - nOE first assertion time is controlled by the GPMC_CONFIG4_i[6:4] OEAADMUXONTIME field.
  - nOE first deassertion time is controlled by the GPMC_CONFIG3_i[15:13] OEAADMUXOFFTIME field.
  - nOE second assertion time is controlled by the GPMC_CONFIG4_i[3:0] OEONTIME field.
  - nOE second deassertion time is controlled by the GPMC_CONFIG4_i[12:8] OEOFFTIME field.

After a read operation, if no other access (read or write) is pending, the data bus is driven with the previous read value. See Section 15.4.4.10.10, *Bus Keeping Support*.

15.4.4.11.2.2 Synchronous Multiple (Burst) Read (4-, 8-, 16-Word16 Burst With Wraparound Capability)

Figure 15-68 and Figure 15-69 show a synchronous multiple read operation with GPMCFCLKDivider equal to 0 and 1, respectively.

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Figure 15-68. Synchronous Multiple (Burst) Read (GPMCFCLKDIVIDER = 0)

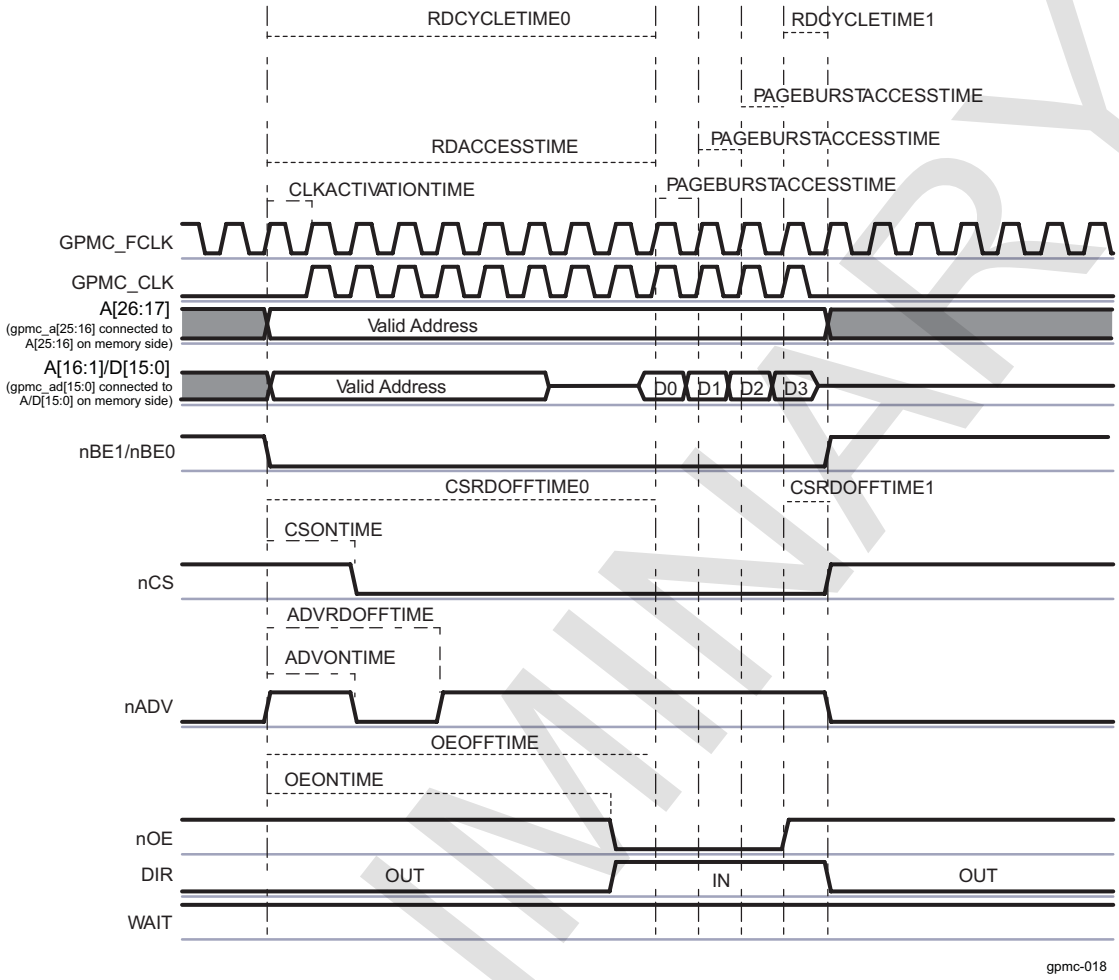

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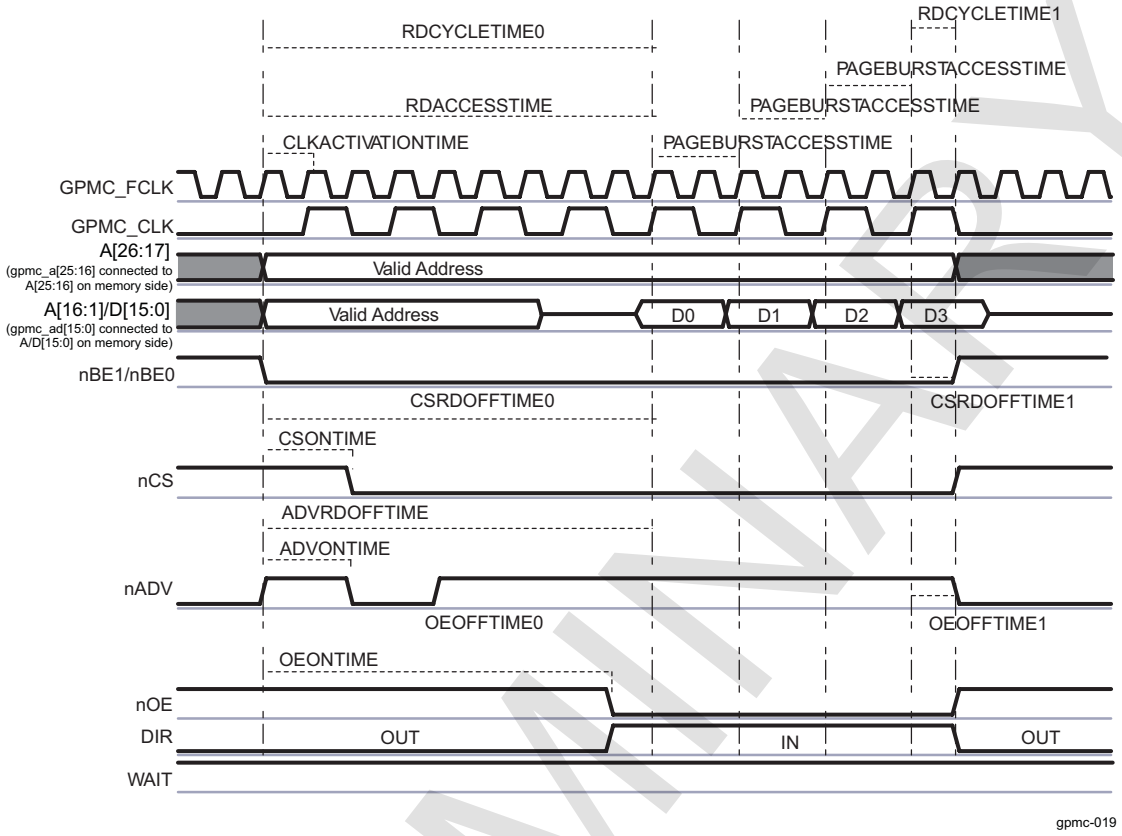
Figure 15-69. Synchronous Multiple (Burst) Read (GPMCFCLKDIVIDER = 1)



When GPMC_CONFIG5_i[20:16] RDACCESSTIME completes, control-signal timings are frozen during the multiple data transactions, corresponding to GPMC_CONFIG5_i[27:24] PAGEBURSTACCESSTIME multiplied by the number of remaining data transactions.

The nCS, nADV, nOE and DIR signals are controlled in the same way as for synchronous single read operation. See Table 15-243.

Initial latency for the first read data is controlled by RDACCESSTIME or by monitoring the WAIT signal. Successive read data are provided by the memory device each one or two GPMC_CLK cycles. The PAGEBURSTACCESSTIME parameter must be set accordingly with GPMC_CONFIG1_i[1:0] GPMCFCLKDIVIDER and the memory-device internal configuration. Depending on the device page length, the GPMC checks device page crossing during a new burst request and purposely insert initial latency (of RDACCESSTIME) when required.

Total access time GPMC_CONFIG5_i[4:0] RDCYCLETIME corresponds to RDACCESSTIME plus the address hold time from nCS deassertion. In Figure 15-69, RDCYCLETIME programmed value equals to RDCYCLETIME0 + RDCYCLETIME1.

After a read operation, if no other access (read or write) is pending, the data bus is driven with the previous read value. See Section 15.4.4.10.10, *Bus Keeping Support*.

Burst wraparound is enabled through the GPMC_CONFIG1_i[31] WRAPBURST bit and allows a 4-, 8-, or 16-Word16 linear burst access to wrap within its burst-length boundary through GPMC_CONFIG1_i[24:23] ATTACHEDDEVICEPAGELENGTH.

15.4.4.11.2.3 Synchronous Single Write

Burst write mode is used for synchronous single or burst accesses.

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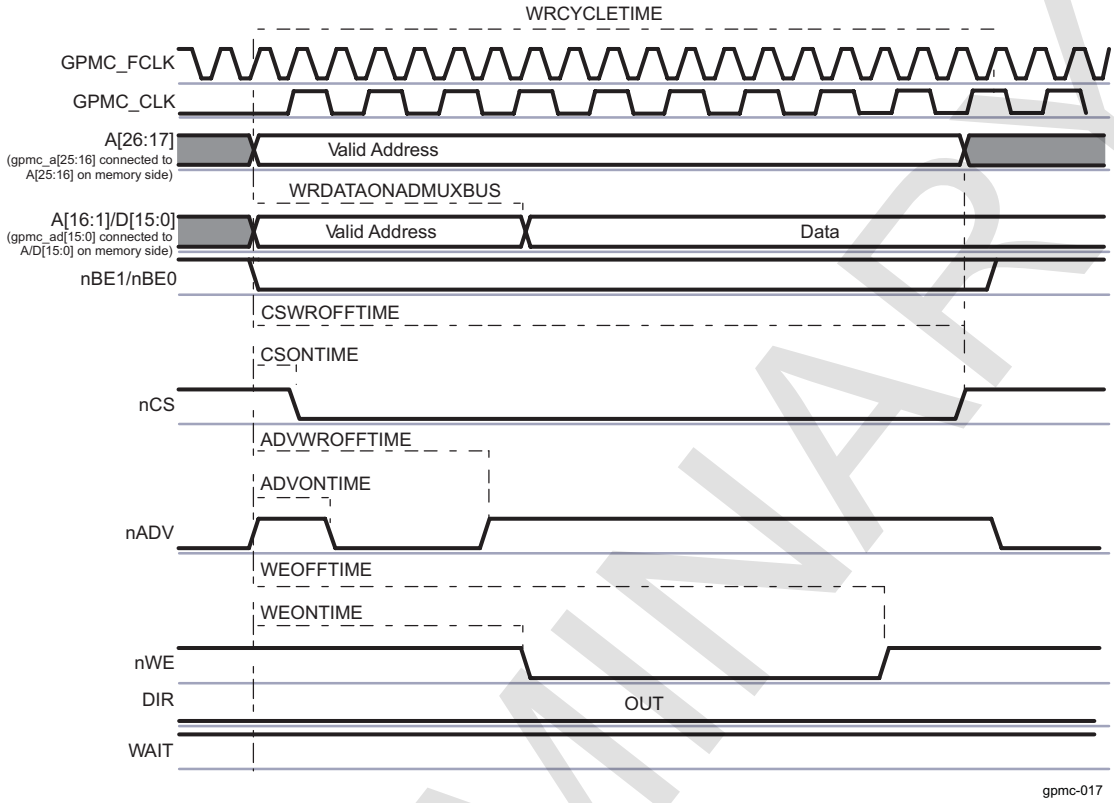
Figure 15-70. Synchronous Single Write on an Address/Data-Multiplexed Device



When the GPMC generates a write access to an address/data-multiplexed device, it drives the data bus (with address bits A[16:1]) until GPMC_CONFIG6_i[19:16] WRDATAONADMUXBUS time. First data of the burst is driven on the address/data bus at WRDATAONADMUXBUS time.

15.4.4.11.2.4 Synchronous Multiple (Burst) Write

Synchronous burst write mode provides synchronous single or consecutive accesses.

Figure 15-71 shows a synchronous burst write access when the chip-select is configured in address/data-multiplexed mode.

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Figure 15-71. Synchronous Multiple Write (Burst Write) in Address/Data-Multiplexed Mode

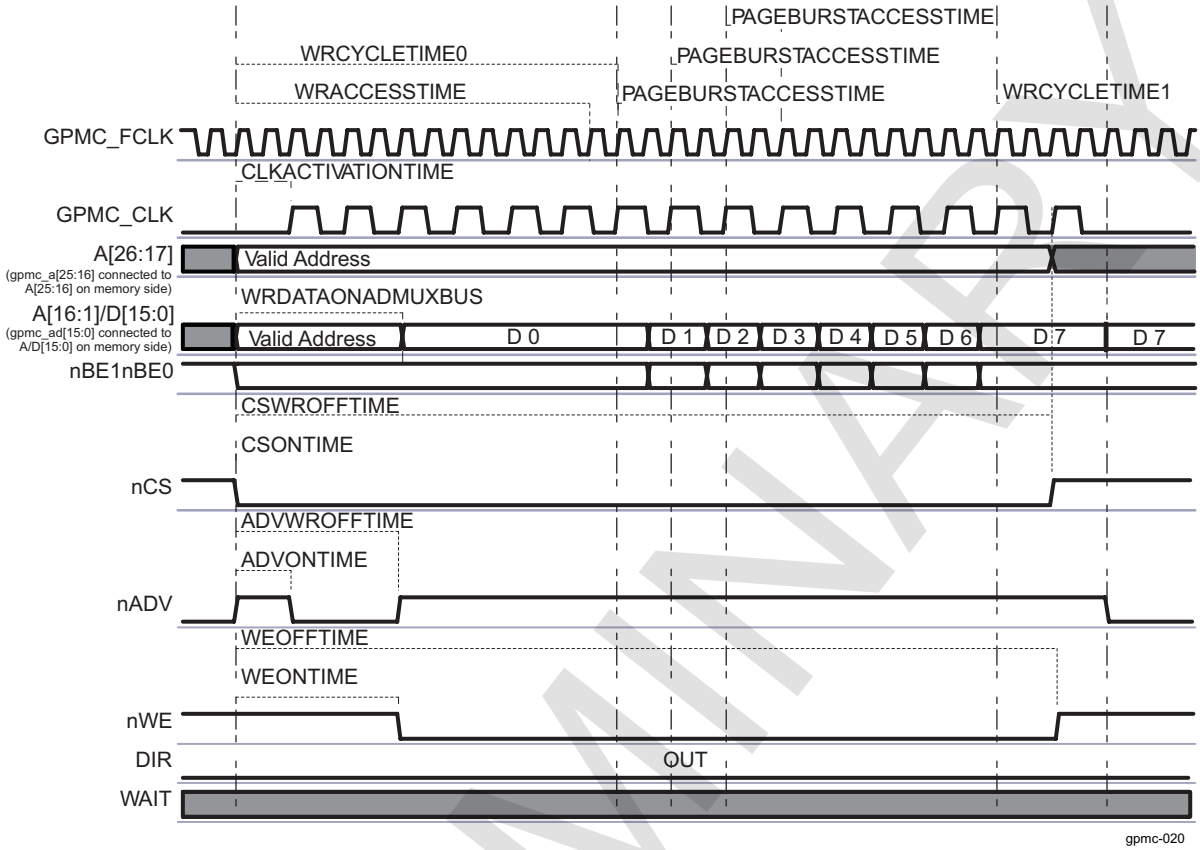

Figure 15-72 shows the same synchronous burst write access when the chip-select is configured in address/address/data-multiplexed (AAD-multiplexed) mode.

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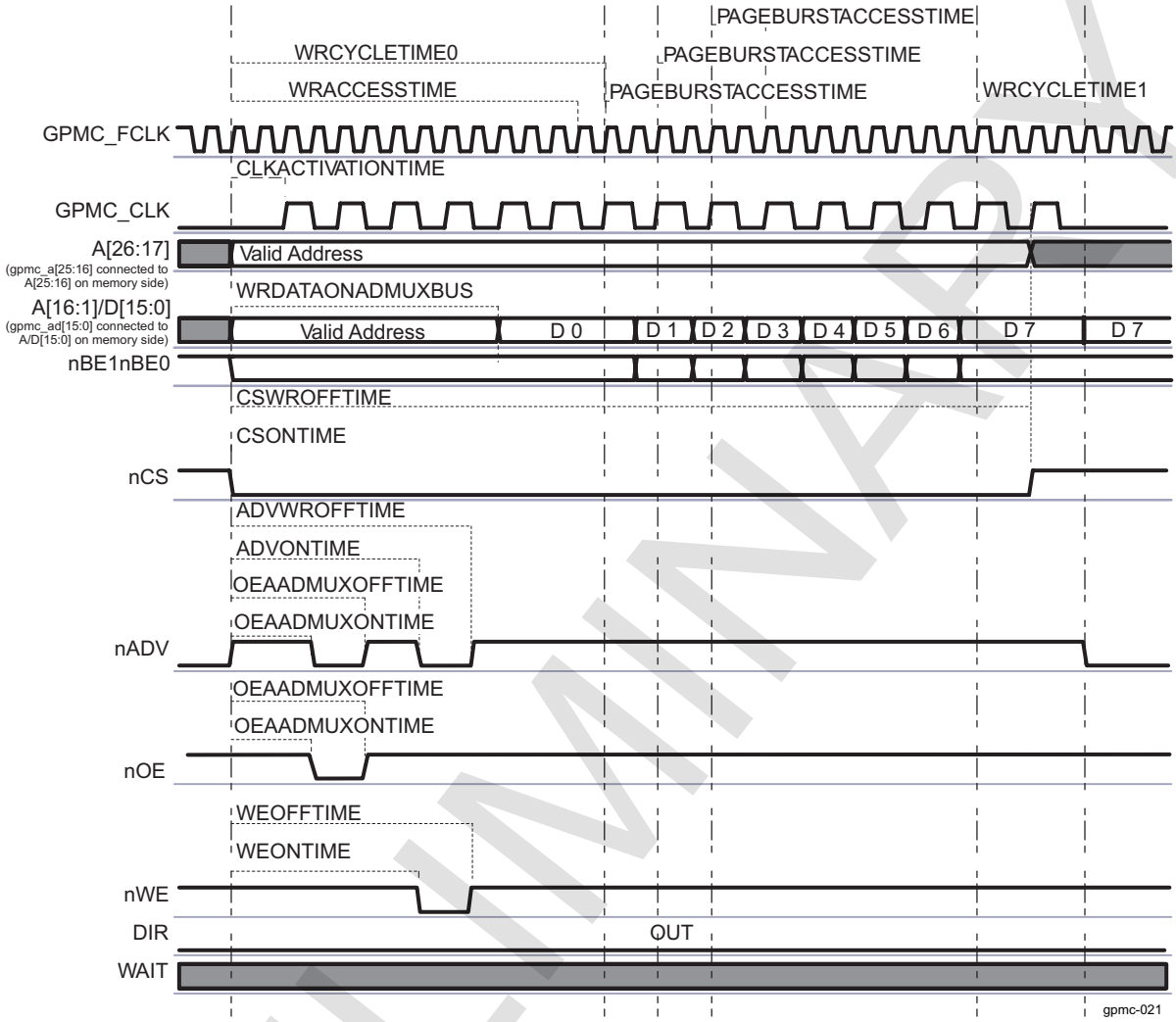
Figure 15-72. Synchronous Multiple Write (Burst Write) in Address/Address/Data-Multiplexed Mode



The first data of the burst is driven on the A/D bus at GPMC_CONFIG6_i[19:16] WRDATAONADMUXBUS.

When WRACCESSTIME completes, control-signal timings are frozen during the multiple data transactions, corresponding to the GPMC_CONFIG5_i[27:24] PAGEBURSTACCESSTIME multiplied by the number of remaining data transactions.

When the GPMC generates a read access to an address/data-multiplexed device, it drives the address bus until nOE assertion time. For details, see Section 15.4.4.9.2.3, *Address/Data-Multiplexing Interface*.

- Chip-select signal nCS:
  - nCS assertion time is controlled by the GPMC_CONFIG2_i[3:0] CSONTIME field (i = 0 to 7) and ensures address setup time to nCS assertion.
  - nCS deassertion time controlled by the GPMC_CONFIG2_i[20:16] CSWROFFTIME field and ensures address hold time to nCS deassertion.
- Address valid signal nADV:
  - nADV assertion time is controlled by the GPMC_CONFIG3_i[3:0] ADVONTIME field.
  - nADV deassertion time is controlled by the GPMC_CONFIG3_i[20:16] ADVWROFFTIME field.
- Write enable signal nWE:
  - nWE assertion indicates a read cycle.
  - nWE assertion time is controlled by the GPMC_CONFIG4_i[19:16] WEONTIME field.

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– nWE deassertion time is controlled by the GPMC_CONFIG4_i[28:24] WEOFFTIME field.

NOTE: The nWE falling edge must not be used to control the time when the burst first data is driven in the address/data bus because some new devices require the nWE signal at low during the address phase.

- Direction signal DIR is OUT during the entire access.

When the GPMC generates a write access to an AAD-multiplexed device, all address bits are driven onto the address/data bus in two separate phases. The first phase is used for the MSB address and is qualified with nOE driven low. The second phase for LSB address is qualified with nOE driven high. The address phase ends at nWE assertion time.

The nCS, and DIR signals are controlled as detailled above.

- Address valid signal nADV is asserted and deasserted twice during a read transaction:
  - nADV first assertion time is controlled by the GPMC_CONFIG3_i[6:4] ADVAADMUXONTIME field.
  - nADV first deassertion time is controlled by the GPMC_CONFIG3_i[26:24] ADVAADMUXRDOFFTIME field.
  - nADV second assertion time is controlled by the GPMC_CONFIG3_i[3:0] ADVONTIME field.
  - nADV second deassertion time is controlled by the GPMC_CONFIG3_i[12:8] ADVRDOFFTIME field.
- Output Enable signal nOE is asserted and deasserted twice during a read transaction (nOE second assertion indicates a read cycle):
  - nOE first assertion time is controlled by the GPMC_CONFIG4_i[6:4] OEAADMUXONTIME field.
  - nOE first deassertion time is controlled by the GPMC_CONFIG4_i[15:13] OEAADMUXOFFTIME field.
  - nOE second assertion time is controlled by the GPMC_CONFIG4_i[3:0] OEONTIME field.
  - nOE second deassertion time is controlled by the GPMC_CONFIG4_i[12:8] OEOFFTIME field.

First write data is driven by the GPMC at GPMC_CONFIG6_i[19:16] WRDATAONADMUXBUS, when in address/data mux configuration. The next write data of the burst is driven on the bus at WRACCESSTIME + 1 during GPMC_CONFIG5_i[27:24] PAGEBURSTACCESSTIME GPMC_FCLK cycles. The last data of the synchronous burst write is driven until GPMC_CONFIG5_i[12:8] WRCYCLETIME completes.

- WRACCESSTIME is defined in the GPMC_CONFIG6_i[28:24] register.
- The PAGEBURSTACCESSTIME parameter must be set accordingly with GPMCFCLKDIVIDER and the memory-device internal configuration.

Total access time GPMC_CONFIG5_i[12:8] WRCYCLETIME corresponds to WRACCESSTIME plus the address hold time from nCS deassertion. In Figure 15-71, the WRCYCLETIME programmed value equals WRCYCLETIME0 + WRCYCLETIME1. WRCYCLETIME0 and WRCYCLETIME1 delays are not actual parameters and are only a graphical representation of the full WRCYCLETIME value.

After a write operation, if no other access (read or write) is pending, the data bus keeps the previous value. See Section 15.4.4.10.10, *Bus Keeping Support*.

15.4.4.11.3 Asynchronous and Synchronous Accesses in Nonmultiplexed Mode

Page mode is only available in non-muxed mode. The non-muxed mode is described in this section even though its use is very limited (address space limited to 2 KBytes).

- Asynchronous single read operation on a nonmultiplexed device
- Asynchronous single write operation on a nonmultiplexed device
- Asynchronous multiple (page mode) read operation on a nonmultiplexed device
- Synchronous operations on a nonmultiplexed device

15.4.4.11.3.1 Asynchronous Single Read Operation on a Nonmultiplexed Device

Figure 15-73 shows an asynchronous single read operation on a nonmultiplexed device.

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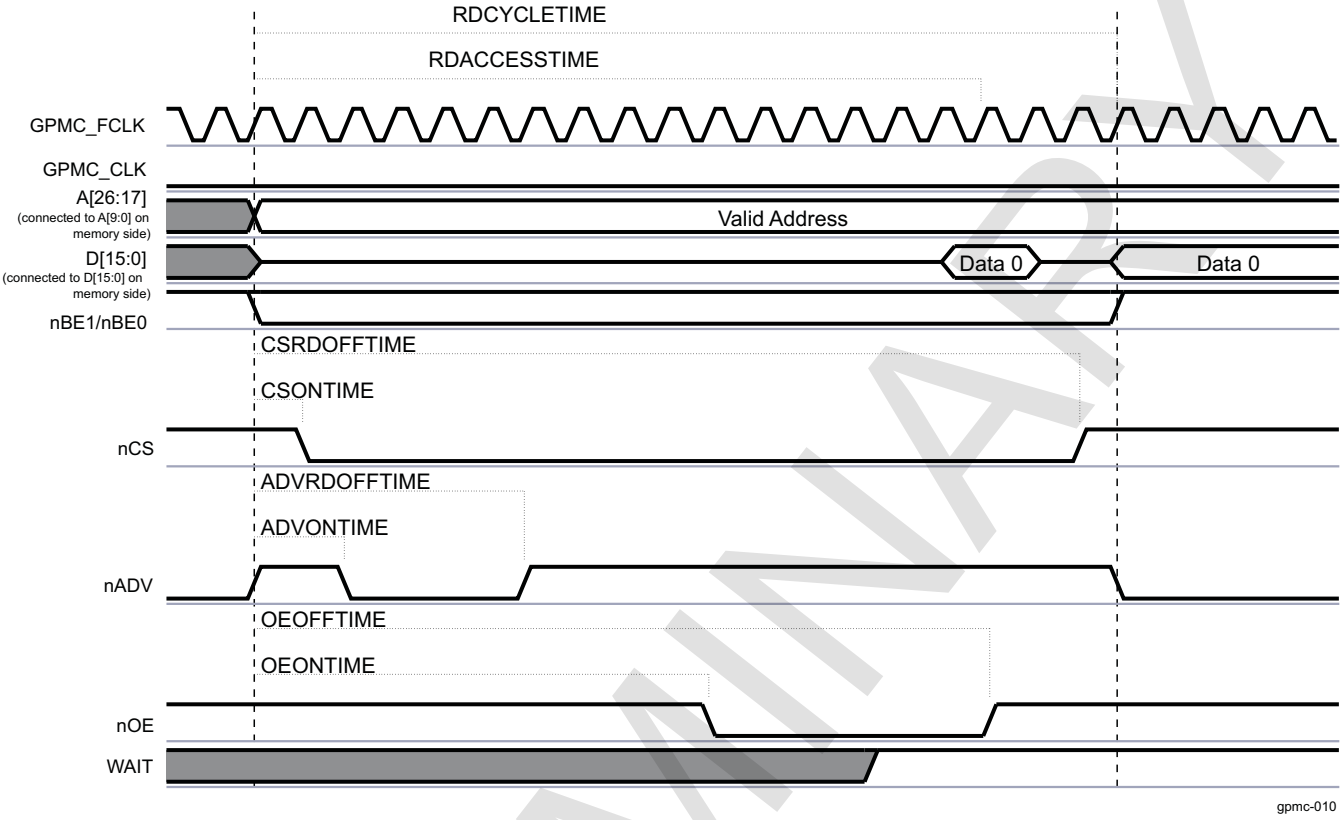
Figure 15-73. Asynchronous Single Read on an Address/Data-Nonmultiplexed Device



The 10-bit address is driven onto the address bus A[10:1] and the 16-bit data is driven onto the data bus D[15:0].

Read data is latched at GPMC_CONFIG1_5[20:16] RDACCESSTIME completion time. The end of the access is defined by the GPMC_CONFIG1_5[4:0] RDCYCLETIME parameter.

Set GPMC_CONFIG[1] LIMITEDADDRESS to 0x1 (A26-A11 are not modified during an external memory access).

nCS, nADV, nOE and DIR signals are controlled in the same way as address/data multiplexed accesses, see Table 15-248.

15.4.4.11.3.2 Asynchronous Single Write Operation on a Nonmultiplexed Device

Figure 15-74 shows an asynchronous single write operation on a nonmultiplexed device.

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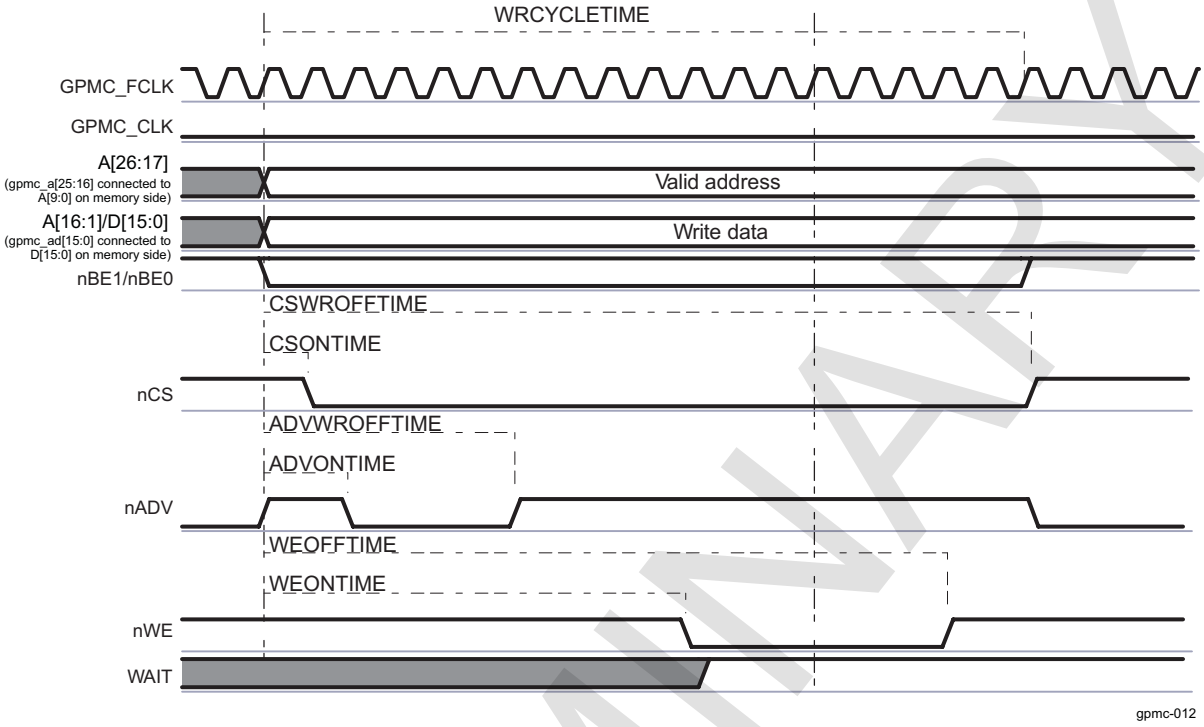
Figure 15-74. Asynchronous Single Write on an Address/Data-Nonmultiplexed Device



The 10-bit address is driven onto the address bus A[10:1] and the 16-bit data is driven onto the data bus D[15:0].

Set GPMC_CONFIG[1] LIMITEDADDRESS to 0x1 (A26-A11 are not modified during an external memory access).

nCS, nADV, nWE and DIR signals are controlled in the same way as address/data multiplexed accesses, see Table 15-248.

15.4.4.11.3.3 Asynchronous Multiple (Page Mode) Read Operation on a Nonmultiplexed Device

Figure 15-75 shows an asynchronous multiple read operation on a Nonmultiplexed Device, in which two word32 host read accesses to the GPMC are split into one multiple (page mode of 4 word16) read access to the attached device.

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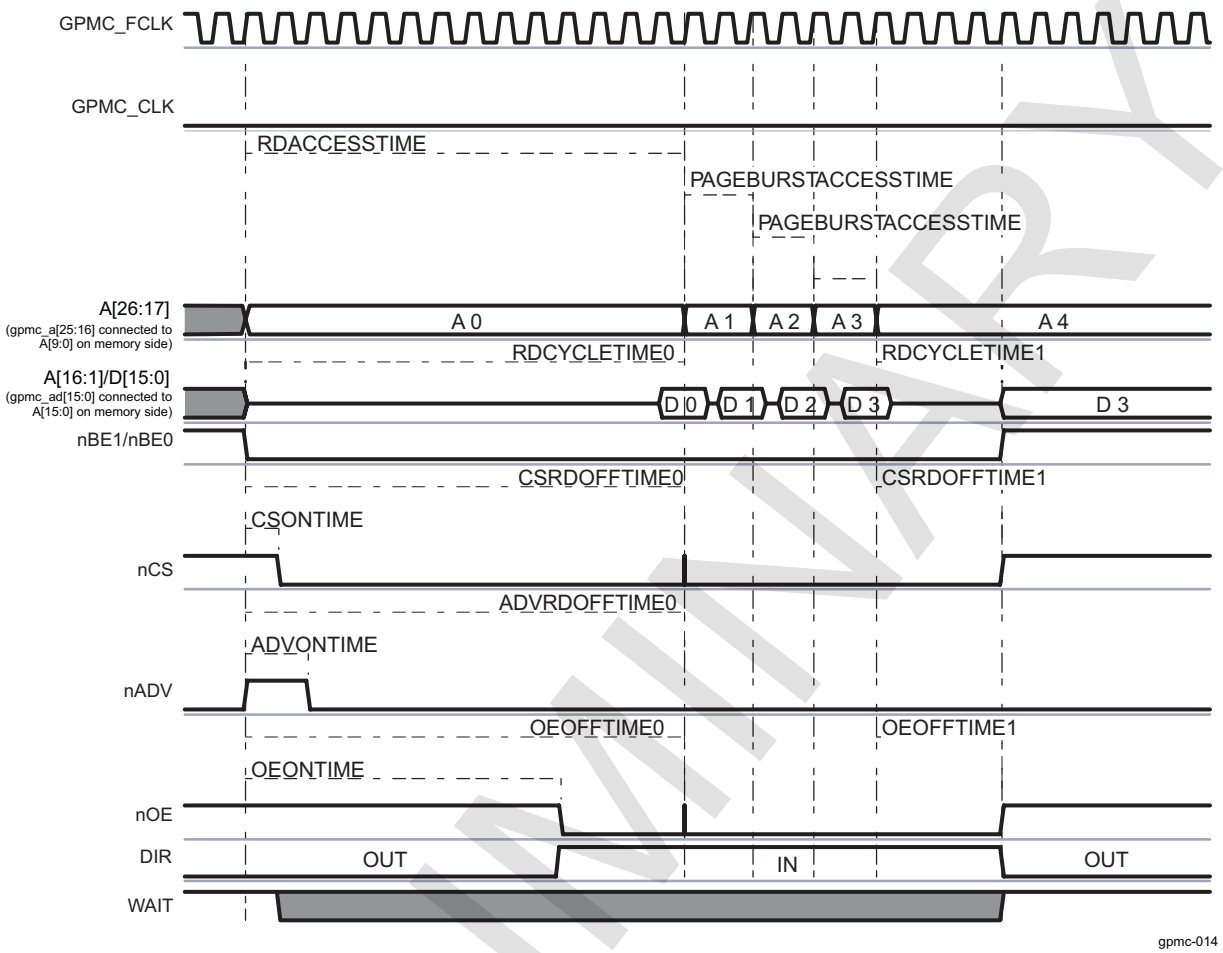
Figure 15-75. Asynchronous Multiple (Page Mode) Read



NOTE: The WAIT signal is active low.

nCS, nADV, nOE and DIR signals are controlled in the same way as address/data multiplexed accesses, see Table 15-248.

When RDACCESSTIME completes, control-signal timings are frozen during the multiple data transactions, corresponding to PAGEBURSTACCESSTIME multiplied by the number of remaining data transactions.

Read data is latched at GPMC_CONFIG5_i[20:16] RDACCESSTIME completion time (i = 0 to 7). The end of the access is defined by the GPMC_CONFIG5_i[4:0] RDCYCLETIME parameter.

Set GPMC_CONFIG[1] LIMITEDADDRESS to 0x1 (A26-A11 are not modified during an external memory access).

During consecutive accesses, the GPMC increments the address after each data read completes.

Delay between successive read data in the page is controlled by the GPMC_CONFIG5_i[27:24] PAGEBURSTACCESSTIME parameter. Depending on the device page length, the GPMC can control device page crossing during a burst request and insert initial RDACCESSTIME latency. Note that page crossing is only possible with a new burst access, meaning a new initial access phase is initiated.

Total access time RDCYCLETIME corresponds to RDACCESSTIME plus the address hold time starting from the nCS deassertion.

- The read cycle time is defined in the GPMC_CONFIG5_i[4:0] RDCYCLETIME field.
- In Figure 15-75, the RDCYCLETIME programmed value equals RDCYCLETIME0 (before paged accesses) + RDCYCLETIME1 (after paged accesses).

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15.4.4.11.3.4 Synchronous Operations on a Nonmultiplexed Device

All information for this section is equivalent to similar operations for address/data- or AAD-multiplexed accesses. The only difference resides in the address phase. See Section 15.4.5.3, *GPMC Configuration in NOR Mode*.

15.4.4.11.4 Page and Burst Support

Each chip-select can be configured to process system single or burst requests into successive single accesses or asynchronous page/synchronous burst accesses, with appropriate access size adaptation.

Depending on the external device page or burst capability, read and write accesses can be independently configured through the GPMC. The GPMC_CONFIG1_i[30] READMULTIPLE and GPMC_CONFIG1_i[28] WRITMULTIPLE bits (i = 0 to 7) are associated with the READTYPE and WRITETYPE parameters.

NOTE:

- Asynchronous write page mode is not supported.
- 8-bit wide device support is limited to nonburstable devices (READMULTIPLE and WRITEMULTIPLE are ignored).
- Not applicable to NAND device interfacing.

15.4.4.11.5 System Burst Versus External Device Burst Support

The device system can issue the following requests to the GPMC:

- Byte, 16-bit word, 32-bit word requests (byte enable controlled). This is always a single request from the interconnect point of view.
- Incrementing fixed-length bursts of two words, four words, and eight words
- Wrapped (critical word access first) fixed-length burst of two, four, or eight words

To process a system request with the optimal protocol, the READMULTIPLE (and READTYPE) and WRITEMULTIPLE (and WRITETYPE) parameters must be set according to the burstable capability (synchronous or asynchronous) of the attached device.

The GPMC access engine issues only fixed-length burst. The maximum length that can be issued is defined per CS by the GPMC_CONFIG1_i[24:23] ATTACHEDDEVICEPAGELENGTH field (i = 0 to 7). When the ATTACHEDDEVICEPAGELENGTH value is less than the system burst request length (including the appropriate access size adaptation according to the device width), the GPMC splits the system burst request into multiple bursts. Within the specified 4-, 8-, or 16-word value, the ATTACHEDDEVICEPAGELENGTH field value must correspond to the maximum-length burst supported by the memory device configured in fixed-length burst mode (as opposed to continuous burst mode).

To get optimal performance from memory devices that natively support 16 Word16-length-wrapping burst capability (critical word access first), the ATTACHEDDEVICEPAGELENGTH parameter must be set to 16 words and the GPMC_CONFIG1_i[31] WRAPBURST bit (i = 0 to 7) must be set to 1. Similarly DEVICEPAGELENGTH is set to 4 and 8 for memories supporting respectively 4 and 8 Word16-length-wrapping burst.

When the memory device does not offer (or is not configured to offer) native 16 Word16-length-wrapping burst, the WRAPBURST parameter must be cleared, and the GPMC access engine emulates the wrapping burst by issuing the appropriate burst sequences according to the ATTACHEDDEVICEPAGELENGTH value.

When the memory device does not support native-wrapping burst, there is usually no difference in behavior between a fixed burst length mode and a continuous burst mode configuration (except for a potential power increase from a memory-speculative data prefetch in a continuous burst read). However, even though continuous burst mode is compatible with GPMC behavior, because the GPMC access engine issues only fixed-length burst and does not benefit from continuous burst mode, it is best to configure the memory device in fixed-length burst mode.

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The memory device maximum-length burst (configured in fixed-length burst wrap or nonwrap mode) usually corresponds to the memory device data buffer size. Memory devices with a minimum of 16 half-word buffers are the most appropriate (especially with wrap support), but memory devices with smaller buffer size (4 or 8) are also supported, assuming that the GPMC_CONFIG1_i[24:23] ATTACHEDDEVICEPAGELENGTH field is set accordingly to 4 or 8 words.

The device system issues only requests with addresses or starting addresses for nonwrapping burst requests; that is, the request size boundary is aligned. In case of an eight-word-wrapping burst, the wrapping address always occurs on the eight-words boundary. As a consequence, all words requested must be available from the memory data buffer when the buffer size is equal to or greater than the ATTACHEDDEVICEPAGELENGTH value. This usually means that data can be read from or written to the buffer at a constant rate (number of cycles between data) without wait states between data accesses. If the memory does not behave this way (nonzero wait state burstable memory), wait-pin monitoring must be enabled to dynamically control data-access completion within the burst.

NOTE: When the system burst request length is less than the ATTACHEDDEVICEPAGELENGTH value, the GPMC proceeds with the required accesses.

15.4.4.12 pSRAM Access Specificities

pSRAM devices are SRAM-pin-compatible low-power memories that contain a self-refreshed DRAM memory array. The GPMC_CONFIG1_i[11:10] DEVICETYPE field (i = 0 to 7) must be set to 0b00.

The pSRAM devices uses the NOR protocol. It support the following operations:

- Asynchronous single read
- Asynchronous page read
- Asynchronous single write
- Synchronous single read and write
- Synchronous burst read
- Synchronous burst write (not supported by NOR Flash memory)

pSRAM devices must be powered up and initialized in a predefined manner according to the specifications of the attached device.

pSRAM devices can be programmed to use either mode: fixed or variable latency. pSRAM devices can either automatically schedule autorefresh operations, which force the GPMC to use its WAIT signal capability when read or write operations occur during an internal self-refresh operation, or pSRAM devices automatically include the autorefresh operation in the access time. These devices do not require additional WAIT signal capability or a minimum nCS high pulse width between consecutive accesses to ensure that the correct internal refresh operation is scheduled.

15.4.4.13 NAND Access Description

NAND (8-bit and 16-bit) memory devices using a standard NAND asynchronous address/data-multiplexing scheme can be supported on any chip-select with the appropriate asynchronous configuration settings.

As for any other type of memory compatible with the GPMC interface, accesses to a chip-select allocated to a NAND device can be interleaved with accesses to chip-selects allocated to other external devices. This interleaved capability limits the system to *chip enable don't care* NAND devices since the chip-select allocated to the NAND device has to be deasserted if accesses to other chip-selects are requested.

15.4.4.13.1 NAND Memory Device in Byte or 16-bit Word Stream Mode

NAND devices require correct command and address programming before data array read or write accesses. The GPMC does not include specific hardware to translate a random address system request into a NAND-specific multiphase access. In that sense, GPMC NAND support, as opposed to random memory-map device support, is data-stream-oriented (byte or 16-bit word).

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The GPMC NAND programming model relies on a software driver for address and command formatting with the correct data address pointer value according to the block and page structure. Because of NAND structure and protocol interface diversity, the GPMC does not support automatic command and address phase programming, and software drivers must access the NAND device ID to ensure that correct command and address formatting are used for the identified device.

NAND device data read and write accesses are achieved through an asynchronous read or write access. The associated chip-select signal timing control must be programmed according to the NAND device timing specification.

Any chip-select region can be qualified as a NAND region to constrain the nADV/ALE signal as Address Latch Enable (ALE active high, default state value at low) during address program access, and the nBE0/CLE signal as Command Latch Enable (CLE active high, default state value at low) during command program access. GPMC address lines are not used (the previous value is not changed) during NAND access.

15.4.4.13.1.1 Chip-Select Configuration for NAND Interfacing in Byte or Word Stream Mode

The GPMC_CONFIG7_i register (where i = 0 to 7) associated with a NAND device region interfaced in byte or word stream mode can be initialized with a minimum size of 16 Mbytes, because any address location in the chip-select memory region can be used to access a NAND data array. The NAND Flash protocol specifies an address sequence where address bits are passed through the data bus in a series of write accesses with the ALE pin asserted. After this address phase, all operations are streamed and the system requests address is irrelevant.

CAUTION

To allow correct command, address, and data-access controls, the GPMC_CONFIG1_i register associated with a NAND device region must be initialized in asynchronous read and write modes with the parameters shown in Table 15-226. Failure to comply with these settings corrupts the NAND interface protocol.

Table 15-226. Chip-Select Configuration for NAND Interfacing

Bit Field	Register	Value	Comments
WRAPBURST	GPMC_CONFIG1_i[31] (1)	0	No wrap
READMULTIPLE	GPMC_CONFIG1_i[30]	0	Single access
READTYPE	GPMC_CONFIG1_i[29]	0	Asynchronous mode
WRITEMULTIPLE	GPMC_CONFIG1_i[28]	0	Single access
WRITETYPE	GPMC_CONFIG1_i[27]	0	Asynchronous mode
CLKACTIVATIONTIME	GPMC_CONFIG1_i[26:25]	0b00	
ATTACHEDDEVICEPAGELENGTH	GPMC_CONFIG1_i[24:23]	Don't care	Single-access mode
WAITREADMONITORING	GPMC_CONFIG1_i[22]	0	Wait not monitored by GPMC access engine
WAITWRITEMONITORING	GPMC_CONFIG1_i[21]	0	Wait not monitored by GPMC access engine
WAITMONITORINGTIME	GPMC_CONFIG1_i[19:18]	Don't care	Wait not monitored by GPMC access engine
WAITPINSELECT	GPMC_CONFIG1_i[17:16]		Select which wait is monitored by edge detectors
DEVICESIZE	GPMC_CONFIG1_i[13:12]	0b00 or 0b01	8- or 16-bit interface
DEVICETYPE	GPMC_CONFIG1_i[11:10]	0b10	NAND device in stream mode
MUXADDDATA	GPMC_CONFIG1_i[9:8]	0b00	Nonmultiplexed mode

(1) i = 0 to 7

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Table 15-226. Chip-Select Configuration for NAND Interfacing (continued)

Bit Field	Register	Value	Comments
TIMEPARAGRANULARITY	GPMC_CONFIG1_i[4]	0	Timing achieved with best GPMC clock granularity
GPMCFCLKDIVIDER	GPMC_CONFIG1_i[1:0]	Don't care	Asynchronous mode

The GPMC_CONFIG1_i to GPMC_CONFIG4_i register (where i = 0 to 7) associated with a NAND device region must be initialized with the correct control-signal timing value according to the NAND device timing parameters.

15.4.4.13.1.2 NAND Device Command and Address Phase Control

NAND devices require multiple address programming phases. The MPU software driver is responsible for issuing the correct number of command and address program accesses, according to the device command set and the device address-mapping scheme.

NAND device-command and address-phase programming is achieved through write requests to the GPMC_NAND_COMMAND_i and GPMC_NAND_ADDRESS_i register locations (i = 0 to 7) with the correct command and address values. These locations are mapped in the associated chip-select register region. The associated chip-select signal timing control must be programmed according to the NAND device timing specification.

Command and address values are not latched during the access and cannot be read back at the register location.

- Only write accesses must be issued to these locations, but the GPMC does not discard any read access. Accessing a NAND device with nOE and CLE or ALE asserted (read access) can produce undefined results.
- Write accesses to the GPMC_NAND_COMMAND_i register location and to the GPMC_NAND_ADDRESS_i register location must be posted for faster operations (i = 0 to 7). The GPMC_CONFIG[0] NANDFORCEPOSTEDWRITE bit enables write accesses to these locations as posted, even if they are defined as nonposted.

A write buffer is used to store write transaction information before the external device is accessed:

- Up to eight consecutive posted write accesses can be accepted and stored in the write buffer.
- For nonposted write, the pipeline is one deep.
- An GPMC_STATUS[0] EMPTYWRITEBUFFERSTATUS bit stores the empty status of the write buffer.

GPMC_NAND_COMMAND_i and GPMC_NAND_ADDRESS_i (i = 0 to 7) are 32-bit word locations, which means any 32-bit word or 16-bit word access is split into 4- or 2-byte accesses if an 8-bit wide NAND device is attached. For multiple-command phase or multiple-address phase, the software driver can use 32-bit word or 16-bit word access to these registers, but it must account for the splitting and little-endian ordering scheme. When only one byte command or address phase is required, only byte write access to GPMC_NAND_COMMAND_i and GPMC_NAND_ADDRESS_i can be used, and any of the four byte locations of the registers are valid.

The same applies to a GPMC_NAND_COMMAND_i and a GPMC_NAND_ADDRESS_i (i = 0 to 7) 32-bit word write access to a 16-bit wide NAND device (split into two 16-bit word accesses). In the case of a 16-bit word write access, the MSByte of the 16-bit word value must be set according to the NAND device requirement (usually 0). Either 16-bit word location or any one of the four byte locations of the registers is valid.

15.4.4.13.1.3 Command Latch Cycle

Writing data at the GPMC_NAND_COMMAND_i location (i = 0 to 7) places the data as the NAND command value on the bus, using a regular asynchronous write access.

- nCE is controlled by the CSONTIME and CSWROFFTIME timing parameters.
- CLE is controlled by the ADVONTIME and ADVWROFFTIME timing parameters.

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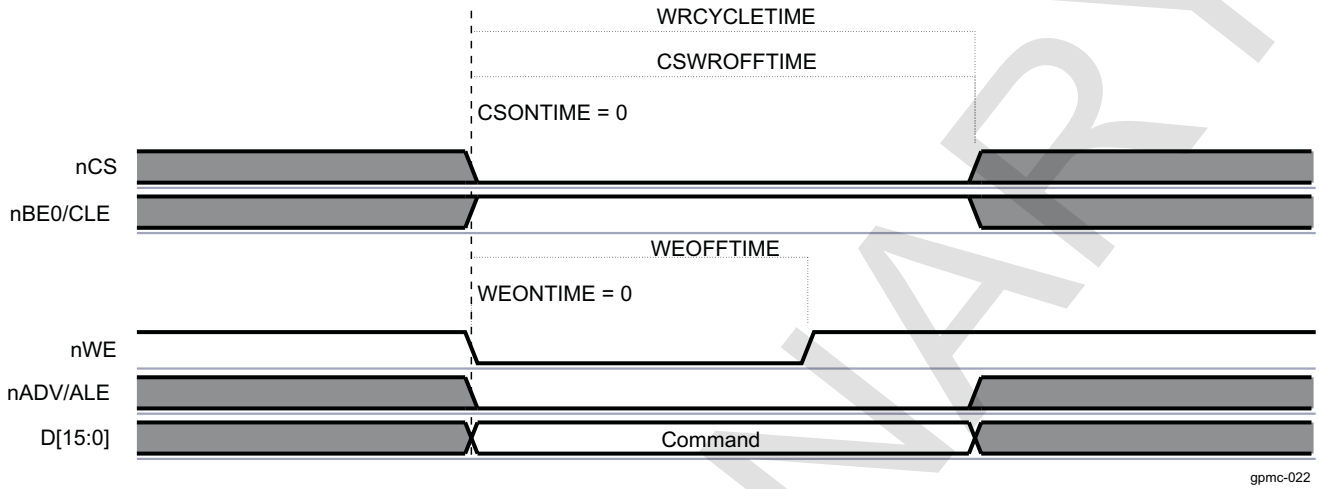
- nWE is controlled by the WEONTIME and WEOFFTIME timing parameters.
- ALE and nRE (nOE) are maintained inactive.

Figure 15-76 shows the NAND command latch cycle.

Figure 15-76. NAND Command Latch Cycle



NOTE: CLE is shared with the nBE0 output signal and has an inverted polarity from BE0. The NAND qualifier deals with this. During the asynchronous NAND data access cycle, nBE0 (also nBE1) must not toggle, because it is shared with CLE.

NAND Flash memories do not use byte enable signals at all.

15.4.4.13.1.4 Address Latch Cycle

Writing data at the GPMC_NAND_ADDRESS_i location (i = 0 to 7) places the data as the NAND partial address value on the bus, using a regular asynchronous write access.

- nCS is controlled by the CSONTIME and CSWROFFTIME timing parameters.
- ALE is controlled by the ADVONTIME and ADVWROFFTIME timing parameters.
- nWE is controlled by the WEONTIME and WEOFFTIME timing parameters.
- CLE and nRE (nOE) are maintained inactive.

Figure 15-77 shows the NAND address latch cycle.

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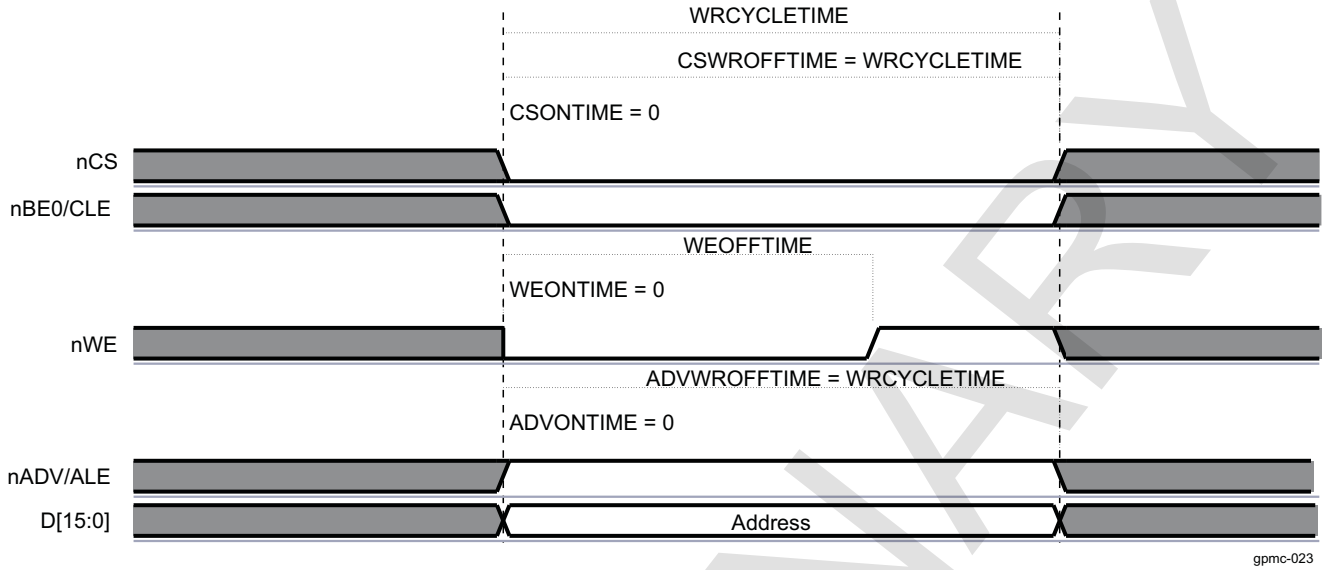
Figure 15-77. NAND Address Latch Cycle



NOTE: ALE is shared with the nADV output signal and has an inverted polarity from ADV. The NAND qualifier deals with this. During the asynchronous NAND data access cycle, ALE is kept stable.

15.4.4.13.1.5 NAND Device Data Read and Write Phase Control in Stream Mode

NAND device data read and write accesses are achieved through a read or write request to the chip-select-associated memory region at any address location in the region or through a read or write request to the GPMC_NAND_DATA_i location (i = 0 to 7) mapped in the chip-select-associated control register region. GPMC_NAND_DATA_i is not a true register, but an address location to enable nRE or nWE signal control. The associated chip-select signal timing control must be programmed according to the NAND device timing specification.

Reading data from the GPMC_NAND_DATA_i location or from any location in the associated chip-select memory region activates an asynchronous read access.

- nCS is controlled by the CSONTIME and CSRDOFFTIME timing parameters.
- nRE is controlled by the OEONTIME and OEOFFTIME timing parameters.
- To take advantage of nRE high-to-data invalid minimum timing value, the RDACCESSTIME can be set so that data are effectively captured after nRE deassertion. This allows optimization of NAND read access cycle time completion. For optimal timing parameter settings, see the NAND device and the device IC timing parameters.

ALE, CLE, and nWE are maintained inactive.

Figure 15-78 shows the NAND data read cycle.

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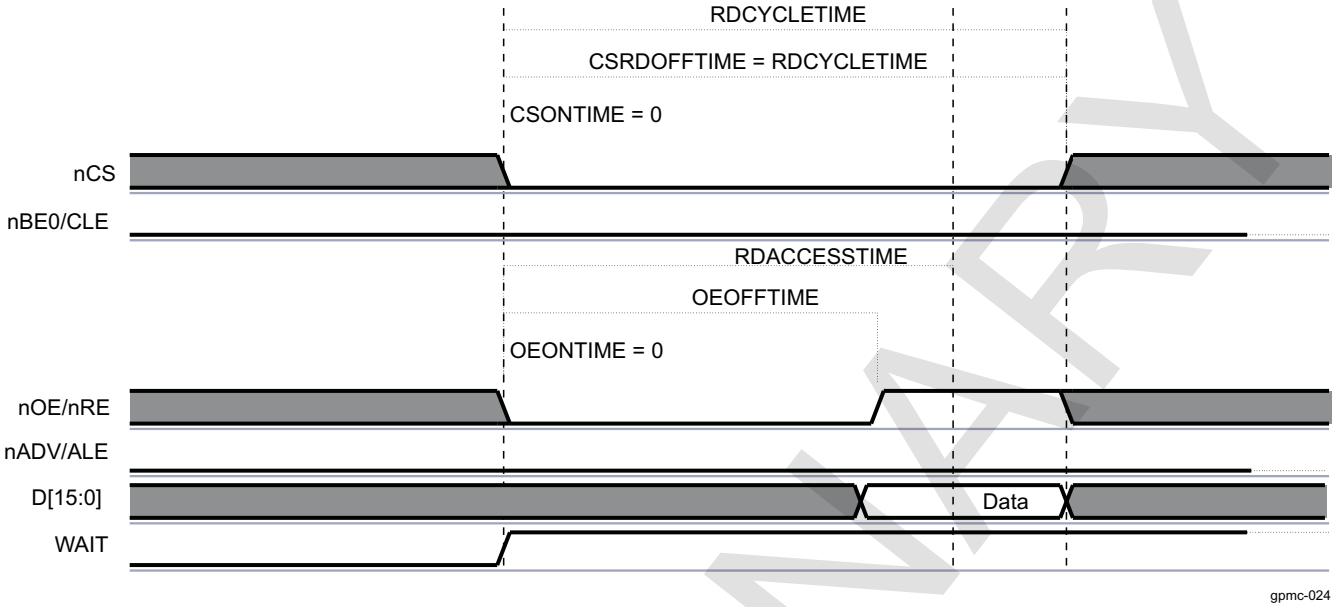
Figure 15-78. NAND Data Read Cycle

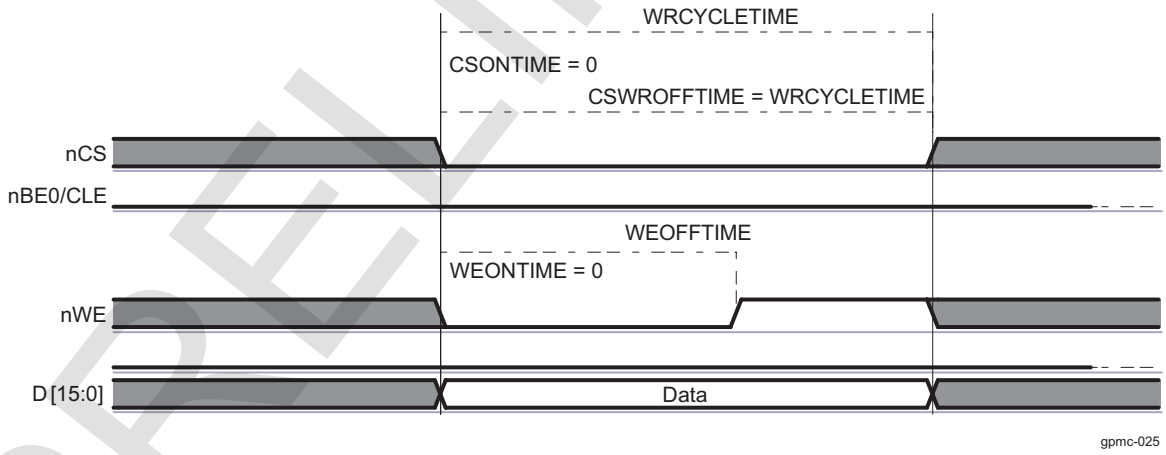


Writing data to the GPMC_NAND_DATA_i location or to any location in the associated chip-select memory region activates an asynchronous write access.

- nCS is controlled by the CSONTIME and CSWROFFTIME timing parameters.
- nWE is controlled by the WEONTIME and WEOFFTIME timing parameters.
- ALE, CLE, and nRE (nOE) are maintained inactive.

Figure 15-79 shows the NAND data write cycle.

Figure 15-79. NAND Data Write Cycle



15.4.4.13.1.6 NAND Device General Chip-Select Timing Control Requirement

For most NAND devices, read data access time is dominated by nCS-to-data-valid timing and has faster nRE-to-data-valid timing. Successive accesses with nCS deassertions between accesses are affected by this timing constraint. Because accesses to a NAND device can be interleaved with other chip-select accesses, there is no certainty that nCS always stays low between two accesses to the same chip-select. Moreover, an nCS deassertion time between the same chip-select NAND accesses is likely to be required as follows: the nCS deassertion requires programming CYCLETIME and RDACCESSTIME according to the nCS-to-data-valid critical timing.

To get full performance from NAND read and write accesses, the prefetch engine can dynamically reduce

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RDCYCLETIME, WRCYCLETIME, RDACCESSTIME, WRACCESSTIME, CSRDOFFTIME, CSWROFFTIME, ADVRDOFFTIME, ADVWROFFTIME, OEOFFTIME, and WEOFFTIME on back-to-back NAND accesses (to the same memory) and suppress the minimum nCS high pulse width between accesses. For more information about optimal prefetch engine access, see Section 15.4.4.13.4, *Prefetch and Write-Posting Engine*.

Some NAND devices require minimum write-to-read idle time, especially for device-status read accesses following status-read command programming (write access). If such write-to-read transactions are used, a minimum nCS high pulse width must be set. For this, CYCLE2CYCLESAMECSEN and CYCLE2CYCLEDELAY must be set according to the appropriate timing requirement to prevent any timing violation.

NAND devices usually have an important nRE high to data bus in tristate mode. This requires a bus turnaround setting (BUSTURNAROUND = 1), so that the next access to a different chip-select is delayed until the BUSTURNAROUND delay completes. Back-to-back NAND read accesses to the same NAND Flash are not affected by the programmed bus turnaround delay.

15.4.4.13.1.7 Read and Write Access Size Adaptation

15.4.4.13.1.7.1 8-bit wide NAND Device

Host 16-bit word and 32-bit word read and write access requests to a chip-select associated with an 8-bit wide NAND device are split into successive read and write byte accesses to the NAND memory device. Byte access is ordered according to little-endian organization. A NAND 8-bit wide device must be interfaced on the D0D7 interface bus lane. GPMC data accesses are justified on this bus lane when the chip-select is associated with an 8-bit wide NAND device.

15.4.4.13.1.7.2 16-bit wide NAND Device

Host 32-bit word read and write access requests to a chip-select associated with a 16-bit wide NAND device are split into successive read and write 16-bit word accesses to the NAND memory device. 16-bit word access is ordered according to little-endian organization.

Host byte read and write access requests to a 16-bit wide NAND device are completed as 16-bit accesses on the device itself, because there is no byte-addressing capability on 16-bit wide NAND devices. This means that the NAND device address pointer is incremented on a 16-bit word basis and not on a byte basis. For a read access, only the requested byte is given back to the host, but the remaining byte is not stored or saved by the GPMC, and the next byte or 16-bit word read access gets the next 16-bit word NAND location. For a write access, the invalid byte part of the 16-bit word is driven to FF, and the next byte or 16-bit word write access programs the next 16-bit word NAND location.

Generally, byte access to a 16-bit wide NAND device should be avoided, especially when ECC calculation is enabled. 8-bit or 16-bit ECC-based computations are corrupted by a byte read to a 16-bit wide NAND device, because the nonrequested byte is considered invalid on a read access (not captured on the external data bus; FF is fed to the ECC engine) and is set to FF on a write access.

Host requests (read/write) issued in the chip-select memory region are translated in successive single or split accesses (read/write) to the attached device. Therefore, incrementing 32-bit burst requests are translated in multiple 32-bit sequential accesses following the access adaptation of the 32-bit to 8- or 16-bit device.

15.4.4.13.2 NAND Device-Ready Pin

The NAND memory device provides a ready pin to indicate data availability after a block/page opening and to indicate that data programming is complete. The ready pin can be connected to one of the WAIT GPMC input pins; data read accesses must not be tried when the ready pin is sampled inactive (device is not ready) even if the associated chip-select WAITREADMONITORING bit field is set. The duration of the NAND device busy state after the block/page opening is so long (up to 50 micro second) that accesses occurring when the ready pin is sampled inactive can stall GPMC access and eventually cause a system time-out.

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NOTE: If a read access to a NAND flash is done using the wait monitoring mode, the device is blocked during a page opening, and so is the GPMC. If the correct settings are used, other chip-selects can be used while the memory processes the page opening command.

To avoid a time-out caused by a block/page opening delay in NAND flash, disable the wait pin monitoring for read and write accesses (that is, set the GPMC_CONFIG1_i[21] WAITWRITEMONITORING and GPMC_CONFIG1_i[22] WAITREADMONITORING bits to 0, where i = 0 to 7), and use one of the following methods instead:

- Use software to poll the WAITnSTATUS bit (n = 0 to 3) of the GPMC_STATUS register.
- Configure an interrupt that is generated on the WAIT signal change (through the GPMC_IRQENABLE register bits[11:8]).

Even if the READWAITMONITORING bit is not set, the external memory nR/B pin status is captured in the programmed WAIT bit in the GPMC_STATUS register.

The READWAITMONITORING bit method must be used for other memories than NAND flash, if they require the use of a WAIT signal.

15.4.4.13.2.1 Ready Pin Monitored by Software Polling

The ready signal state can be monitored through the GPMC_STATUS WAITxSTATUS bit (x = 0 or 1). The software must monitor the ready pin only when the signal is declared valid. Refer to the NAND device timing parameters to set the correct software temporization to monitor ready only after the invalid window is complete from the last read command written to the NAND device.

15.4.4.13.2.2 Ready Pin Monitored by Hardware Interrupt

Each gpmc_wait input pin can generate an interrupt when a wait-to-no-wait transition is detected. Depending on whether the GPMC_CONFIG WAITxPINPOLARITY bits (x = 0 or 1) is active low or active high, the wait-to-no-wait transition is a low-to-high external WAIT signal transition or a high-to-low external WAIT signal transition, respectively.

The wait transition pin detector must be cleared before any transition detection. This is done by writing 1 to the WAITxEDGEDETECTIONSTATUS bit (x = 0 or 3) of the GPMC_IRQSTATUS register according to the gpmc_wait pin used for the NAND device-ready signal monitoring. To detect a wait-to-no-wait transition, the transition detector requires a wait active time detection of a minimum of two GPMC_FCLK cycles. Software must incorporate precautions to clear the wait transition pin detector before wait (busy) time completes.

A wait-to-no-wait transition detection can issue a GPMC interrupt if the WAITxEDGEDETECTIONENABLE bit in the GPMC_IRQENABLE register is set and if the WAITxEDGEDETECTIONSTATUS bit field in the GPMC_IRQSTATUS register is set.

The WAITMONITORINGTIME field does not affect wait-to-no-wait transition time detection.

It is also possible to poll the WAITxEDGEDETECTIONSTATUS bit field in the GPMC_IRQSTATUS register according to the gpmc_wait pin used for the NAND device ready signal monitoring.

15.4.4.13.3 ECC Calculator

The General Purpose Memory Controller includes an Error Code Correction (ECC) calculator circuitry that enables on the fly ECC calculation during data read or data program (that is, write) operations. The page size supported by the ECC calculator in one calculation/context is 512 bytes.

The user can choose from two different algorithms with different error correction capabilities through the GPMC_ECC_CONFIG[16] ECCALGORITHM bit:

1. Hamming code for 1-bit error code correction on 8- or 16-bit NAND Flash organized with page size greater than 512 bytes
2. BCH (Bose-Chaudhurl-Hocquenghem) code for 4- to 16-bit error correction

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The GPMC does not directly handle the error code correction itself. During writes, the GPMC computes parity bits. During reads, the GPMC provides enough information for the processor to correct errors without reading the data buffer all over again.

The Hamming code ECC is based on a 2-dimensional (row and column) bit parity accumulation. This parity accumulation is either accomplished on the programmed number of bytes or 16-bit words read from the memory device, or written to the memory device in stream mode.

Because the ECC engine includes only one accumulation context, it can be allocated to only one chip-select at a time through the GPMC_ECC_CONFIG[3:1] ECCCS bit field. Even if two CS use different ECC algorithms, one the Hamming code and the other a BCH code, they must define separate ECC contexts because some of the ECC registers are common to all types of algorithms.

15.4.4.13.3.1 Hamming Code

All references to Error Code Correction (ECC) in this subsection refer to the 1-bit error correction Hamming code.

The ECC is based on a two-dimensional (row and column) bit parity accumulation known as Hamming Code. The parity accumulation is done for a programmed number of bytes or 16-bit word read from the memory device or written to the memory device in stream mode.

There is no automatic error detection or correction, and it is the software NAND driver responsibility to read the multiple ECC calculation results, compare them to the expected code value, and take the appropriate corrective actions according to the error handling strategy (ECC storage in spare byte, error correction on read, block invalidation).

The ECC engine includes a single accumulation context. It can be allocated to a single designated chip-select at a time and parallel computations on different chip-selects are not possible. Since it is allocated to a single chip-select, the ECC computation is not affected by interleaved GPMC accesses to other chip-selects and devices. The ECC accumulation is sequentially processed in the order of data read from or written to the memory on the designated chip-select. The ECC engine does not differentiate read accesses from write accesses and does not differentiate data from command or status information. It is the software responsibility to make sure only relevant data are passed to the NAND flash memory while the ECC computation engine is active.

The starting NAND page location must be programmed first, followed by an ECC accumulation context reset with an ECC enabling, if required. The NAND device accesses discussed in the following sections must be limited to data read or write until the specified number of ECC calculations is completed.

15.4.4.13.3.1.1 ECC Result Register and ECC Computation Accumulation Size

The GPMC includes up to nine ECC result registers (GPMC_ECCj_RESULT, j = 1 to 9) to store ECC computation results when the specified number of bytes or 16-bit words has been computed.

The ECC result registers are used sequentially; one ECC result is stored in one ECC result register on the list, the next ECC result is stored in the next ECC result register on the list, and so forth, until the last ECC computation. The GPMC_ECCj_RESULT register value is valid only when the programmed number of bytes or 16-bit words has been accumulated, which means that the same number of bytes or 16-bit words has been read from or written to the NAND device in sequence.

The GPMC_ECC_CONTROL[3:0] ECCPOINTER field must be set to the correct value to select the ECC result register to be used first in the list for the incoming ECC computation process. The ECCPointer can be read to determine which ECC register is used in the next ECC result storage for the ongoing ECC computation. The GPMC_ECCj_RESULT register value (j = 1 to 9) can be considered valid when ECCPOINTER equals j + 1. When GPMC_ECCj_RESULT (where j = 9) is updated, ECCPOINTER is frozen at 10, and ECC computing is stopped (ECCENABLE = 0).

The ECC accumulator must be reset before any ECC computation accumulation process. The GPMC_ECC_CONTROL[8] ECCCLEAR bit must be set to 1 (nonpersistent bit) to clear the accumulator and all ECC result registers.

For each ECC result (each GPMC_ECCj_RESULT register, j = 1 to 9), the number of bytes or 16-bit words used for ECC computing accumulation can be selected from between two programmable values.

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The ECCjRESULTSIZE bits (j = 1 to 9) in the GPMC_ECC_SIZE_CONFIG register select which programmable size value (ECCSIZE0 or ECCSIZE1) must be used for this ECC result (stored in GPMC_ECCj_RESULT).

The ECCSIZE0 and ECCSIZE1 fields allow selection of the number of bytes or 16-bit words used for ECC computation accumulation. Any even values from 2 to 512 are allowed.

Flexibility in the number of ECCs computed and the number of bytes or 16-bit words used in the successive ECC computations enables different NAND page error-correction strategies. Usually based on 256 or 512 bytes and on 128 or 256 16-bit word, the number of ECC results required is a function of the NAND device page size. Specific ECC accumulation size can be used when computing the ECC on the NAND spare byte.

For example, with a 2 Kbyte data page 8-bit wide NAND device, eight ECCs accumulated on 256 bytes can be computed and added to one extra ECC computed on the 24 spare bytes area where the eight ECC results used for comparison and correction with the computed data page ECC are stored. The GPMC then provides nine GPMC_ECCj_RESULT registers (j= 1 to 9) to store the results. In this case, ECCSIZE0 is set to 256, and ECCSIZE1 is set to 24; the ECC[1:8]RESULTSIZE bits are set to 0, and the ECC9RESULTSIZE bit is set to 1.

15.4.4.13.3.1.2 ECC Enabling

The GPMC_ECC_CONFIG[3:1] ECCCS field selects the allocated chip-select. The GPMC_ECC_CONFIG[0] ECCENABLE bit enables ECC computation on the next detected read or write access to the selected chip-select.

The ECCPOINTER, ECCCLEAR, ECCSIZE, ECCjRESULTSIZE (where j = 1 to 9), ECC16B, and ECCCS fields must not be changed or cleared while an ECC computation is in progress.

The ECC accumulator and ECC result register must not be changed or cleared while an ECC computation is in progress.

Table 15-227 describes the ECC enable settings.

Table 15-227. ECC Enable Settings

Bit Field	Register	Value	Comments
ECCCS	GPMC_ECC_CONFIG	0-3	Selects the chip-select where ECC is computed
ECC16B	GPMC_ECC_CONFIG	0/1	Selects column number for ECC calculation
ECCCLEAR	GPMC_ECC_CONTROL	0-7	Clears all ECC result registers
ECCPOINTER	GPMC_ECC_CONTROL	0-7	A write to this bit field selects the ECC result register where the first ECC computation is stored. Set to 1 by default.
ECCSIZE1	GPMC_ECC_SIZE_CONFIG	0x00-0xFF	Defines ECCSIZE1
ECCSIZE0	GPMC_ECC_SIZE_CONFIG	0x00-0xFF	Defines ECCSIZE0
ECCjRESULTSIZE (j from 1 to 9)	GPMC_ECC_SIZE_CONFIG	0/1	Selects the size of ECCn result register
ECCENABLE	GPMC_ECC_CONFIG	1	Enables the ECC computation

15.4.4.13.3.1.3 ECC Computation

The ECC algorithm is a multiple parity bit accumulation computed on the odd and even bit streams extracted from the byte or Word 16 streams. The parity accumulation is split into row and column accumulations, as shown in Figure 15-80 and Figure 15-81. The intermediate row and column parities are used to compute the upper level row and column parities. Only the final computation of each parity bit is used for ECC comparison and correction.

P1o = bit7 XOR bit5 XOR bit3 XOR bit1 on each byte of the data stream
P1e = bit6 XOR bit4 XOR bit2 XOR bit0 on each byte of the data stream

P2o = bit7 XOR bit6 XOR bit3 XOR bit2 on each byte of the data stream
P2e = bit5 XOR bit4 XOR bit1 XOR bit0 on each byte of the data stream

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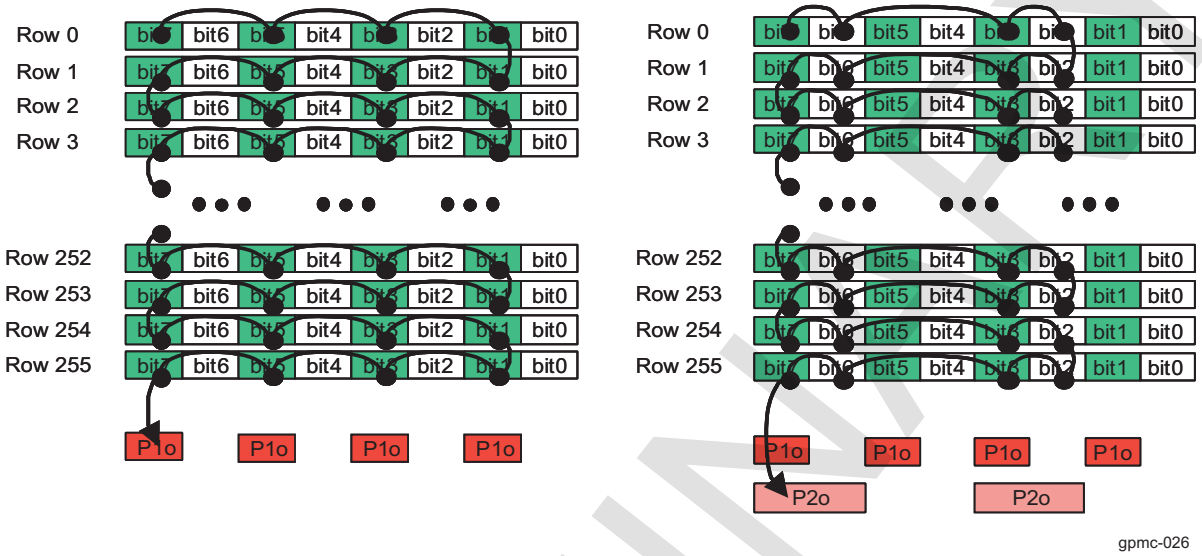
P4o = bit7 XOR bit6 XOR bit5 XOR bit4 on each byte of the data stream
P4e = bit3 XOR bit2 XOR bit1 XOR bit0 on each byte of the data stream

Each column parity bit is XORed with the previous accumulated value.

Figure 15-80. Hamming Code Accumulation Algorithm (1/2)

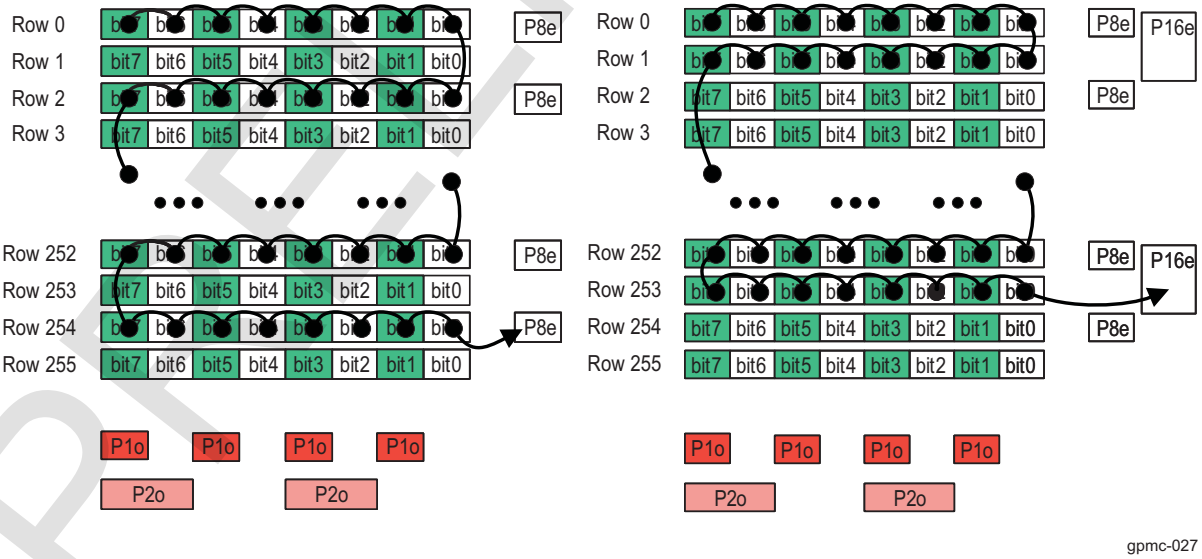


For line parities, the bits of each new data are XORed together, and line parity bits are computed as described below:

P8e = row0 XOR row2 XOR row4 XOR ... XOR row254
P8o = row1 XOR row3 XOR row5 XOR ... XOR row255

P16e = row0 XOR row1 XOR row4 XOR row5 XOR ... XOR row252 XOR row 253
P16o = row2 XOR row3 XOR row6 XOR row7 XOR ... XOR row254 XOR row 255

Figure 15-81. Hamming Code Accumulation Algorithm (2/2)



Unused parity bits in the result registers are set to 0.

Figure 15-82 shows ECC computation for a 256-byte data stream (read or write). The result includes six column parity bits (P1o-P2o-P4o for odd parities, and P1e-P2e-P4e for even parities) and sixteen row parity bits (P8o-P16o-P32o--P1024o for odd parities, and P8e-P16e-P32e--P1024e for even parities).

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Figure 15-82. ECC Computation for a 256-Byte Data Stream (Read or Write)

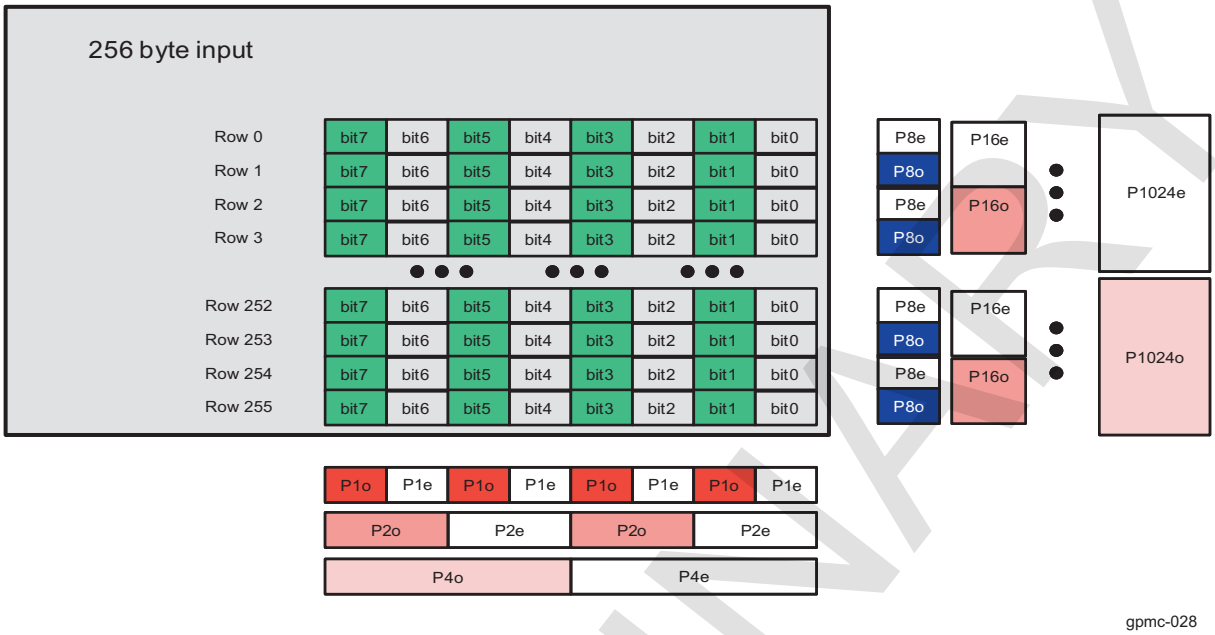
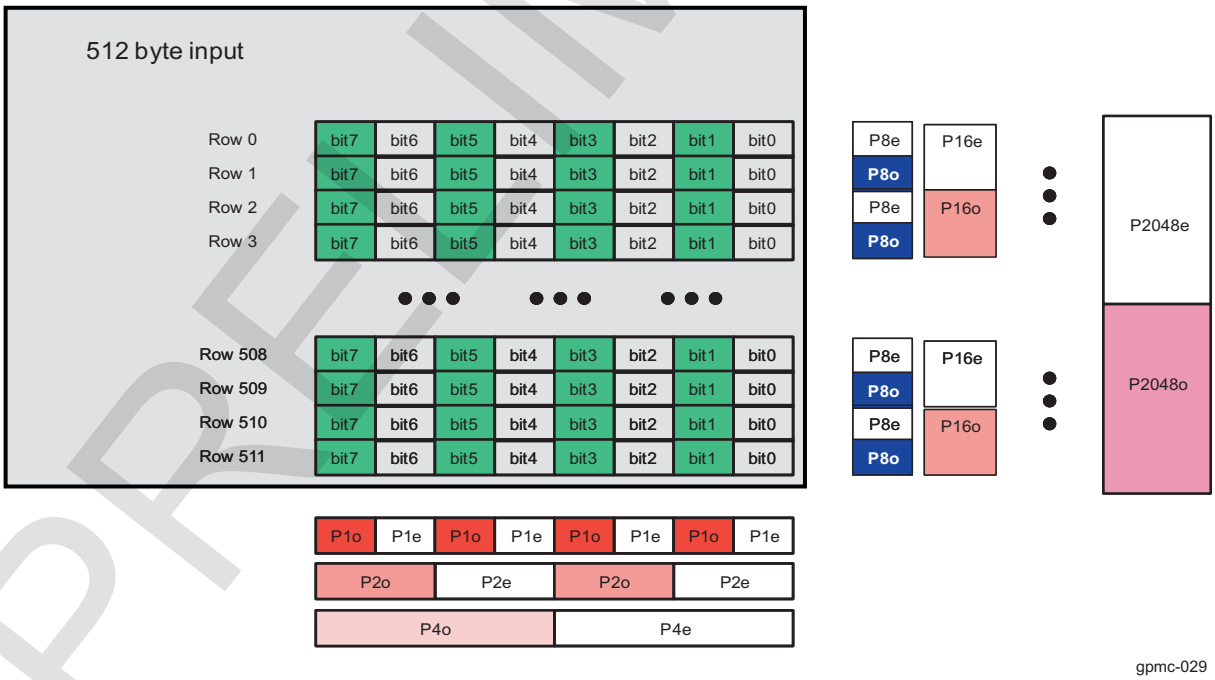


Figure 15-83 shows ECC computation for a 512-byte data stream (read or write). The result includes six column parity bits (P1o-P2o-P4o for odd parities, and P1e-P2e-P4e for even parities) and eighteen row parity bits (P8o-P16o-P32o--P1024o- - P2048o for odd parities, and P8e-P16e-P32e--P1024e- P2048e for even parities).

Figure 15-83. ECC Computation for a 512-Byte Data Stream (Read or Write)



For a 2 Kbytes page, four 512 bytes ECC calculations plus one for the spare area are required. Results are stored in the GPMC_ECCj_RESULT registers (j = 1 to 9).

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15.4.4.13.3.1.4 ECC Comparison and Correction

To detect an error, the computed ECC result must be XORed with the parity value stored in the spare area of the accessed page.

- If the result of this logical XOR is all 0s, no error is detected and the read data is correct.
- If every second bit in the parity result is a 1, one bit is corrupted and is located at bit address (P2048o, P1024o, P512o, P256o, P128o, P64o, P32o, P16o, P8o, P4o, P2o, P1o). The software must correct the corresponding bit.
- If only one bit in the parity result is 1, it is an ECC error and the read data is correct.

15.4.4.13.3.1.5 ECC Calculation Based on 8-Bit Word

The 8-bit based ECC computation is used for 8-bit wide NAND device interfacing.

The 8-bit based ECC computation can be used for 16-bit wide NAND device interfacing to get backward compatibility on the error-handling strategy used with 8-bit wide NAND devices. In this case, the 16-bit wide data read from or written to the NAND device is fragmented into 2 bytes. According to little-endian access, the least significant bit (LSB) of the 16-bit wide data is ordered first in the byte stream used for 8-bit based ECC computation.

15.4.4.13.3.1.6 ECC Calculation Based on 16-Bit Word

ECC computation based on a 16-bit word is used for 16-bit wide NAND device interfacing. This ECC computation is not supported when interfacing an 8-bit wide NAND device, and the GPMC_ECC_CONFIG[7] ECC16B bit must be set to 0 when interfacing an 8-bit wide NAND device.

The parity computation based on 16-bit words affects the row and column parity mapping. The main difference is that the odd and even parity bits P8o and P8e are computed on rows for an 8-bit based ECC while there are computed on columns for a 16-bit based ECC. Figure 15-84 and Figure 15-85 show a 128 Word 16 ECC computation scheme and a 256 16-bit word ECC computation scheme.

Figure 15-84. 128 Word16 ECC Computation

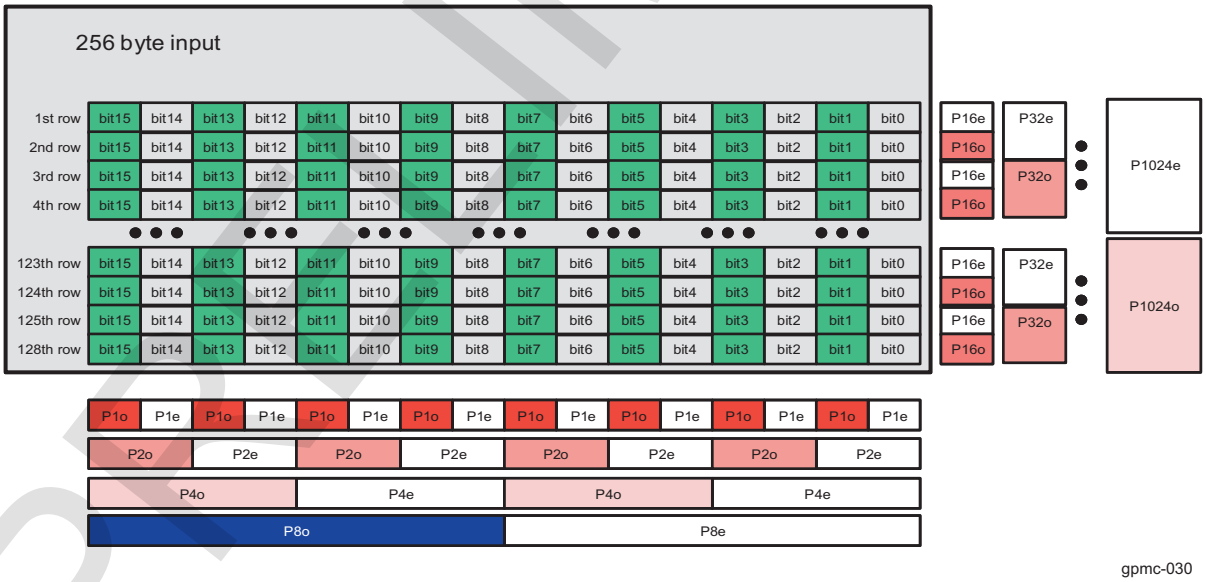

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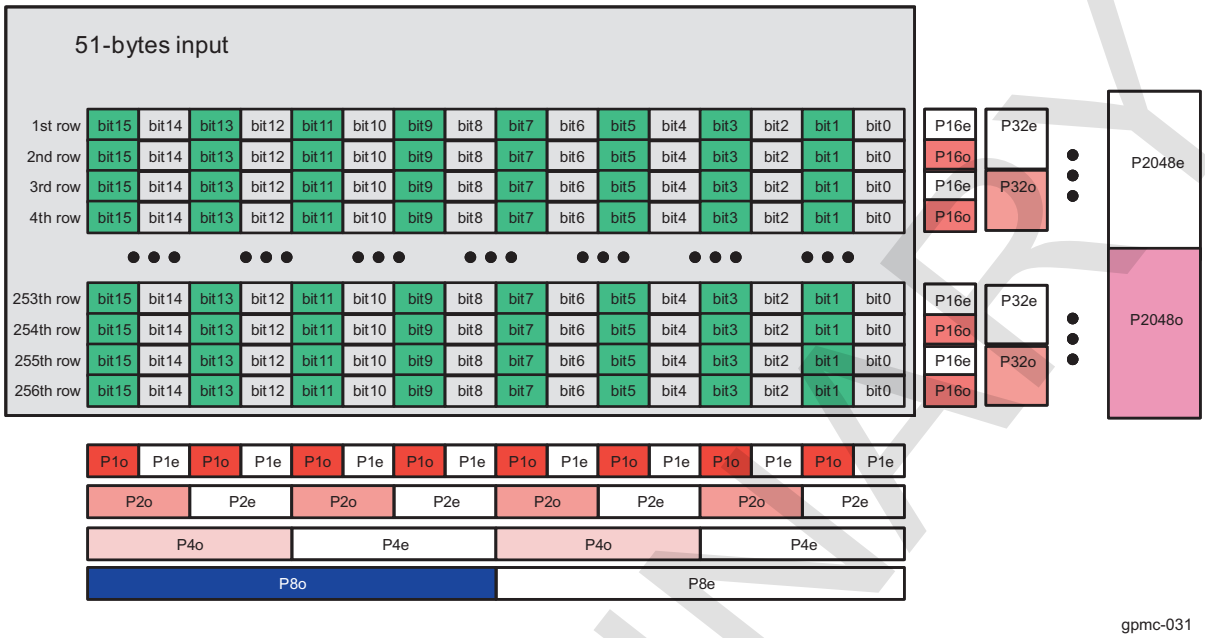
Figure 15-85. 256 Word16 ECC Computation



15.4.4.13.3.2 BCH Code (Bose-Chaudhurl-Hocquenghem)

All references to Error Code Correction (ECC) in this subsection refer to the 4- to 16-bit error correction BCH code.

15.4.4.13.3.2.1 Requirements

1. Read and write accesses to a NAND flash take place by whole pages, in a predetermined sequence: first the data byte page itself, then some spare bytes, including the BCH ECC (and other information). The NAND IC can cache a full page, including spares, for read and write accesses.
   Typical page write sequence:
   - Sequential write to NAND cache of main data + spare data, for a page. ECC is calculated on the fly. Calculated ECC may be inserted on the fly in the spares, or replaced by dummy accesses.
   - When the calculated ECC is replaced by dummy accesses, it must be written to the cache in a second, separate phase. The ECC module is disabled during that time.
   - NAND writes its cache line (page) to the array.

   Typical page read sequence:
   - Sequential read of a page. ECC is calculated on the fly.
   - ECC module buffers status determines the presence of errors.
2. Accesses to several memories may be interleaved by the GPMC, but only one of those memories can be a NAND using the BCH engine at a time; in other words, only one BCH calculation (for example, for a single page) can be on-going at any time. Note also that the sequential nature of NAND accesses guarantees that the data is always written / read out in the same order. BCH-relevant accesses are selected by the GPMCs chip-select.
3. Each page may hold up to 4 Kbytes of data, spare bytes not included. This means up to 8 x 512-byte BCH messages. Since all the data is written / read out first, followed by the BCH ECC, this means that the BCH engine must be able to hold 8 104-bit remainders or syndromes (or smaller, 52-bit ones) at the same time.
   The BCH module has the capacity to store all remainders internally. After the page start, an internal counter is used to detect the 512-byte sector boundaries. On those boundaries, the current remainder is stored and the divider reset for the next calculation. At the end of the page, the BCH module contains all remainders.
4. NAND access cycles hold 8 or 16 bits of data each (1 or 2 bytes); Each NAND cycle takes at least 4

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cycles of the GPMCs internal clock. This means the NAND flash timing parameters must define a RDCYCLETIME and a WRCYCLETIME of at least 4 clock cycles after optimization when using the BCH calculator.

5. The spare area is assumed to be large enough to hold the BCH ECC, that is, to have at least a message of 13 bytes available per 512-byte sector of data. The zone of unused spare area by the ECC may or may not be protected by the same ECC scheme, by extending the BCH message beyond 512 bytes (maximum codeword is 1023-byte long, ECC included, which leaves a lot of space to cover some spares bytes).

15.4.4.13.3.2.2 Memory-Mapping of the BCH Codeword

BCH encoding considers a block of data to protect as a polynomial message M(x). In our standard case, 512 bytes of data (that is, 2^{12} bits = 4096 bits) are seen as a polynomial of degree 2^{12} - 1 = 4095, with parameters ranging from M0 to M4095. For 512 bytes of data, 52 bits are required for 4-bit error correction, and 104 bits are required for 8-bit error correction and 207 bits are required for 16-bit error correction. The ECC is a remainder polynomial R(x) of degree 103 (or 51, depending on the selected mode). The complete codeword C(x) is the concatenation of M(x) and R(x) as shown in Table 15-228.

Table 15-228. Flattened BCH Codeword Mapping (512 Bytes + 104 Bits)

	Message M(x)			ECC R(x)		
Bit number	M4095	...	M0	R103	...	R0

If the message is extended by the addition of spare bytes to be protected by the same ECC, the principle is still valid. For example, a 3-byte extension of the message gives a polynomial message M(x) of degree ((512 + 3) * 8) - 1 = 4119, for a total of 3+13 = 16 spare bytes of spare, all protected as part of the same codeword.

The message and the ECC bits are manipulated and mapped in the GPMC byte-oriented system. The ECC bits are stored in GPMC_BCH_RESULT0_i, GPMC_BCH_RESULT1_i, GPMC_BCH_RESULT2_i, and GPMC_BCH_RESULT3_i (where i = 0 to 7).

15.4.4.13.3.2.2.1 Memory-Mapping of the Data Message

The data message mapping shall follow the following rules:

- Bit endianness within a byte is little-endian, that is, the bytes LS bit is also the lowest-degree polynomial parameter: a byte b7-b0 (with b0 the LS bit) represents a segment of polynomial b7 * $x^{(7+i)}$ + b6 * $x^{(6+i)}$ + ... + b0 * x^{i}
- The message is mapped in the NAND starting with the highest-order parameters, that is, in the lowest addresses of a NAND page.
- Byte endianness within the NANDs 16-bit words is big endian. This means that the same message mapped in 8- and 16-bit memories has the same content at the same byte address.

NOTE: The BCH module has no visibility over actual addresses. The most important point is the sequence of data word the BCH sees. However, the NAND page is always scanned incrementally in read and write accesses, and this produces the mapping patterns described below.

The following tables represent the mapping of the same 512-byte vector (typically a BCH message) in the NANDs memory space. Note that the byte 'address' is only an offset modulo 512 (0x200), since the same page may contain several contiguous 512-byte sectors (BCH blocks). The LSB and MSB are respectively the bits M0 and M(2^{12}-1) of the codeword mapping given above. In both cases the data vectors are aligned, that is, their boundaries coincide with the RAMs data word boundaries.

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Table 15-229. Aligned Message Byte Mapping in 8-bit NAND

Byte offset	8-bit word
0x000	(msb) Byte 511 (0x1FF)
0x001	Byte 510 (0x1FE)
...	...
0x1FF	Byte 0 (0x0) (lsb)

Table 15-230. Aligned Message Byte Mapping in 16-bit NAND

Byte offset	16-bit words MSB	16-bit words LSB
0x000	Byte 510 (0x1FE)	(msb) Byte 511 (0x1FF)
0x002	Byte 508 (0x1FC)	Byte 509 (0x1FD)
...	...	...
0x1FE	Byte 0 (0x0)	(lsb) Byte 1 (0x1)

The following tables show the mapping in memory of arbitrarily-sized messages, starting on access (byte or 16-bit word) boundaries for more clarity. Note that message may actually start and stop on arbitrary nibbles. A nibble is a 4-bit entity. The unused nibbles are not discarded, and they can still be used by the BCH module, but as part of the next message section (for example, on another sectors ECC).

Table 15-231. Aligned Nibble Mapping of Message in 8-bit NAND

Byte offset	8-bit word	
	4-bit most significant Nibble	4-bit less significant Nibble
1	(msb) Nibble S-1	Nibble S-2
2	Nibble S-3	Nibble S-4
...	...	...
S/2 - 2	Nibble 3	Nibble 2
S/2 - 1	Nibble 1	Nibble 0 (lsb)

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Table 15-232. Misaligned Nibble Mapping of Message in 8-bit NAND

Byte offset	8-bit word	
	4-bit most significant Nibble	4-bit less significant Nibble
1	(msb) Nibble S-1	Nibble S-2
2	Nibble S-3	Nibble S-4
...	...	...
(S+1)/2 - 2	Nibble 2	Nibble 1
(S+1)/2 - 1	Nibble 0 (lsb)	

Table 15-233. Aligned Nibble Mapping of Message in 16-bit NAND

Byte offset	16-bit word			
	4-bit most significant Nibble		4-bit less significant Nibble	
0	Nibble S-3	Nibble S-4	(msb) Nibble S-1	Nibble S-2
2	Nibble S-7	Nibble S-8	Nibble S-5	Nibble S-6
...	...		...	
S/2 - 4	Nibble 5	Nibble 4	Nibble 7	Nibble 6
S/2 - 2	Nibble 1	Nibble 0 (lsb)	Nibble 3	Nibble 2

Table 15-234. Misaligned Nibble Mapping of Message in 16-bit NAND (1 Unused Nibble)

Byte offset	16-bit word			
	4-bit most significant Nibble		4-bit less significant Nibble	
0	Nibble S-3	Nibble S-4	(msb) Nibble S-1	Nibble S-2
2	Nibble S-7	Nibble S-8	Nibble S-5	Nibble S-6
...	...		...	
(S+1)/2 - 4	Nibble 4	Nibble 3	Nibble 6	Nibble 5
(S+1)/2 - 2	Nibble 0 (lsb)		Nibble 2	Nibble 1

Table 15-235. Misaligned Nibble Mapping of Message in 16-bit NAND (2 Unused Nibbles)

Byte offset	16-bit word			
	4-bit most significant Nibble		4-bit less significant Nibble	
0	Nibble S-3	Nibble S-4	(msb) Nibble S-1	Nibble S-2
2	Nibble S-7	Nibble S-8	Nibble S-5	Nibble S-6
...	...		...	
(S+2)/2 - 4	Nibble 3	Nibble 2	Nibble 5	Nibble 4
(S+2)/2 - 2			Nibble 1	Nibble 0 (lsb)

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Table 15-236. Misaligned Nibble Mapping of Message in 16-bit NAND (3 Unused Nibbles)

Byte offset	16-bit word			
	4-bit most significant Nibble		4-bit less significant Nibble	
0	Nibble S-3	Nibble S-4	(msb) Nibble S-1	Nibble S-2
2	Nibble S-7	Nibble S-8	Nibble S-5	Nibble S-6
...	...		...	
(S+3)/2 - 4	Nibble 2	Nibble 1	Nibble 4	Nibble 3
(S+3)/2 - 2			Nibble 0 (lsb)	

Note that many other cases exist than the ones represented above, for example, where the message does not start on a word boundary.

15.4.4.13.3.2.2.2 Memory-Mapping of the ECC

The ECC (or remainder) is presented by the BCH module as a single 104-bit (or 52-bit), little-endian vector. It is up to the software to fetch those 13 bytes (or 6 bytes) from the modules interface, then store them to the NANDs spare area (page write) or to an intermediate buffer for comparison with the stored ECC (page read). There are no constraints on the ECC mapping inside the spare area: it is a softwarecontrolled operation.

However, it is advised to maintain a coherence in the respective formats of the message or the ECC remainder once they have been read out of the NAND. The error correction algorithm works from the complete codeword (concatenated message and remainder) once an error as been detected. The creation of this codeword should be made as straightforward as possible.

There are cases where the same NAND access contains both data and the ECC protecting that data. This is the case when the data/ECC boundary (which can be on any nibble) does not coincide with an access boundary. The ECC is calculated on-the-fly following the write. In that case, the write must also contain part of the ECC because it is impossible to insert the ECC on-the-fly. Instead:

- During the initial page write (BCH encoding), the ECC is replaced by dummy bits. The BCH encoder is by definition turned OFF during the ECC section, so the BCH result is unmodified.
- During a second phase, the ECC is written to the correct location, next to the actual data.
- The completed line buffer is then written to the NAND array.

15.4.4.13.3.2.2.3 Wrapping Modes

For a given wrapping mode, the module automatically goes through a specific number of sections, as data is being fed into the module. For each section, the BCH core can be enabled (in which case the data is fed to the BCH divider) or not (in which case the BCH simply counts to the end of the section). When enabled, the data is added to the ongoing calculation for a given sector number (for example, number 0).

Wrapping modes are described below. To get a better understanding and see the real-life read and write sequences implemented with each mode, see Section 15.4.4.13.3.2.3, *Supported NAND Page Mappings and ECC Schemes*.

For each mode:

- a sequence describes the mode in pseudo-language, with for each section the size and the buffer used for ECC processing (if ON). The programmable lengths are size, size0 and size1.
- a checksum condition is given. If the checksum condition is not respected for a given mode, the modules behavior is unpredictable. S is the number of sectors in the page; size0 and size1 are the section sizes programmed for the mode, in nibbles.

Note that wrapping modes 8, 9, 10, and 11 insert a 1-nibble padding where the BCH processing is OFF. This is intended for t = 4 ECC, where ECC is 6 bytes long and the ECC area is expected to include (at least) 1 unused nibble to remain byte-aligned.

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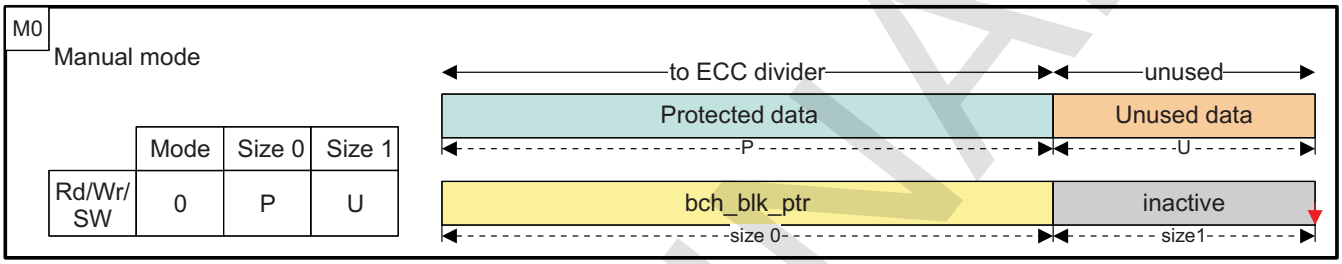
15.4.4.13.3.2.2.4 Manual Mode (0x0)

This mode is intended for short sequences, added manually to a given buffer through the software data port input. A complete page may be built out of several such sequences.

To process an arbitrary sequence of 4-bit nibbles, accesses to the software data port shall be made, containing the appropriate data. If the sequence end does not coincide with an access boundary (for example, to process 5 nibbles = 20 bits in 16-bit access mode) and those nibbles need to be skipped, a number of unused nibbles shall be programmed in size1 (in the same example: 5 nibbles to process + 3 to discard = 8 nibbles = exactly 2 x 16-bit accesses: we must program size0 = 5, size1 = 3).

NOTE: In the following figures size and size0 are the same parameter.

Figure 15-86. Manual Mode Sequence and Mapping



Section processing sequence:

- One time with buffer
  - size0 nibbles of data, processing ON
  - size1 nibbles of unused data, processing OFF

Checksum: size0 + size1 nibbles must fit in a whole number of accesses.

In the following sections, S is the number of sectors in the page.

15.4.4.13.3.2.2.5 Mode 0x1

Page processing sequence:

- Repeat with buffer 0 to S-1
  - 512-byte data, processing ON
- Repeat with buffer 0 to S-1
  - size0 nibbles spare, processing ON
  - size1 nibbles spare, processing OFF

Checksum: Spare area size (nibbles) = S - (size0 + size1)

15.4.4.13.3.2.2.6 Mode 0xA (10)

Page processing sequence:

- Repeat with buffer 0 to S-1
  - 512-byte data, processing ON
- Repeat with buffer 0 to S-1
  - size0 nibbles spare, processing ON
  - 1 nibble pad spare, processing OFF
  - size1 nibbles spare, processing OFF

Checksum: Spare area size (nibbles) = S - (size0 + 1 + size1)

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15.4.4.13.3.2.2.7 Mode 0x2

Page processing sequence:

- Repeat with buffer 0 to S-1
  - 512-byte data, processing ON
- Repeat with buffer 0 to S-1
  - size0 nibbles spare, processing OFF
  - size1 nibbles spare, processing ON

Checksum: Spare area size (nibbles) = S - (size0 + size1)

15.4.4.13.3.2.2.8 Mode 0x3

Page processing sequence:

- Repeat with buffer 0 to S-1
  - 512-byte data, processing ON
- One time with buffer 0
  - size0 nibbles spare, processing ON
- Repeat with buffer 0 to S-1
  - size1 nibbles spare, processing ON

Checksum: Spare area size (nibbles) = size0 + (S - size1)

15.4.4.13.3.2.2.9 Mode 0x7

Page processing sequence:

- Repeat with buffer 0 to S-1
  - 512-byte data, processing ON
- One time with buffer 0
  - size0 nibbles spare, processing ON
- Repeat S times (no buffer used)
  - size1 nibbles spare, processing OFF

Checksum: Spare area size (nibbles) = size0 + (S - size1)

15.4.4.13.3.2.2.10 Mode 0x8

Page processing sequence:

- Repeat with buffer 0 to S-1
  - 512-byte data, processing ON
- One time with buffer 0
  - size0 nibbles spare, processing ON
- Repeat with buffer 0 to S-1
  - 1 nibble padding spare, processing OFF
  - size1 nibbles spare, processing ON

Checksum: Spare area size (nibbles) = size0 + (S - (1+size1))

15.4.4.13.3.2.2.11 Mode 0x4

Page processing sequence:

- Repeat with buffer 0 to S-1
  - 512-byte data, processing ON
- One time (no buffer used)

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  - size0 nibbles spare, processing OFF
- Repeat with buffer 0 to S-1
  - size1 nibbles spare, processing ON

Checksum: Spare area size (nibbles) = size0 + (S - size1)

15.4.4.13.3.2.2.12 Mode 0x9

Page processing sequence:

- Repeat with buffer 0 to S-1
  - 512-byte data, processing ON
- One time (no buffer used)
  - size0 nibbles spare, processing OFF
- Repeat with buffer 0 to S-1
  - 1 nibble padding spare, processing OFF
  - size1 nibbles spare, processing ON

Checksum: Spare area size (nibbles) = size0 + (S - (1+size1))

15.4.4.13.3.2.2.13 Mode 0x5

Page processing sequence:

- Repeat with buffer 0 to S-1
  - 512-byte data, processing ON
- Repeat with buffer 0 to S-1
  - size0 nibbles spare, processing ON
- Repeat with buffer 0 to S-1
  - size1 nibbles spare, processing ON

Checksum: Spare area size (nibbles) = S - (size0 + size1)

15.4.4.13.3.2.2.14 Mode 0xB (11)

Page processing sequence:

- Repeat with buffer 0 to S-1
  - 512-byte data, processing ON
- Repeat with buffer 0 to S-1
  - size0 nibbles spare, processing ON
- Repeat with buffer 0 to S-1
  - 1 nibble padding spare, processing OFF
  - size1 nibbles spare, processing ON

Checksum: Spare area size (nibbles) = S - (size0 + 1 + size1)

15.4.4.13.3.2.2.15 Mode 0x6

Page processing sequence:

- Repeat with buffer 0 to S-1
  - 512-byte data, processing ON
- Repeat with buffer 0 to S-1
  - size0 nibbles spare, processing ON
- Repeat S times (no buffer used)
  - size1 nibbles spare, processing OFF

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Checksum: Spare area size (nibbles) = S - (size0 + size1)

15.4.4.13.3.2.3 Supported NAND Page Mappings and ECC Schemes

The following rules apply throughout the entire mapping description:

- Main data area (sectors) size is hardcoded to 512 bytes.
- Spare area size is programmable.
- All page sections (of main area data bytes, protected spare bytes, unprotected spare bytes, and ECC) are defined as explained in Section 15.4.4.13.3.2.2.1, *Memory-Mapping of the Data Message*.

Each one of the following sections shows a NAND page mapping example (per-sector spare mappings, pooled spare mapping, per-sector spare mapping, with ECC separated at the end of the page).

In the mapping diagrams, sections that belong to the same BCH codeword have the same color (blue or green); unprotected sections are not covered (orange) by the BCH scheme.

Below each mapping diagram, a write (encoding) and read (decoding: syndrome generation) sequence is given, with the number of the active buffers at each point in time (yellow). In the inactive zones (grey), no computing is taking place but the data counter is still active.

In Figure 15-87 to Figure 15-89, tables on the left summarize the mode, size0, size1 parameters to program for respectively write and read processing of a page, with the given mapping, where :

- P is the size of spare byte section Protected by the ECC (in nibbles)
- U is the size of spare byte section Unprotected by the ECC (in nibbles)
- E is the size of the ECC itself (in nibbles)
- S is the number of Sectors per page (2 in the current diagrams)

Each time the processing of a BCH block is complete (ECC calculation for write/encoding, syndrome generation for read/decoding, indicated by red arrows), the update pointer is pulsed. Note that the processing for block 0 can be the first or the last to complete, depending on the NAND page mapping and operation (read or write). All examples show a page size of 1kByte + spares, that is, S = 2 sectors of 512 bytes. The same principles can be extended to larger pages by adding more sectors.

The actual BCH codeword size is used during the error location work to restrict the search range: by definition, errors can only happen in the codeword that was actually written to the NAND, and not in the mathematical codeword of $n = 2^{13} - 1 = 8191$ bits. That codeword (higher-order bits) is all-zero and implicit during computations.

The actual BCH codeword size depends on the mode, on the programmed sizes and on the sector number (all sizes in nibbles):

- Spares mapped and protected per sector (below: see M1-M2-M3-M9-M10):
  - all sectors: (512) + P + E
- Spares pooled and protected by sector 0 (below: see M5-M6):
  - sector 0 codeword: (512) + P + E
  - other sectors: (512) + E
- Unprotected spares (below: see M4-M7-M8-M11-M12):
  - all codewords (512) + E

15.4.4.13.3.2.3.1 Per-Sector Spare Mappings

In these schemes, each 512-byte sector of the main area has its own dedicated section of the spare area. The spare area of each sector is composed of :

- ECC, which must be located after the data it protects
- other data, which may or may not be protected by the sectors ECC

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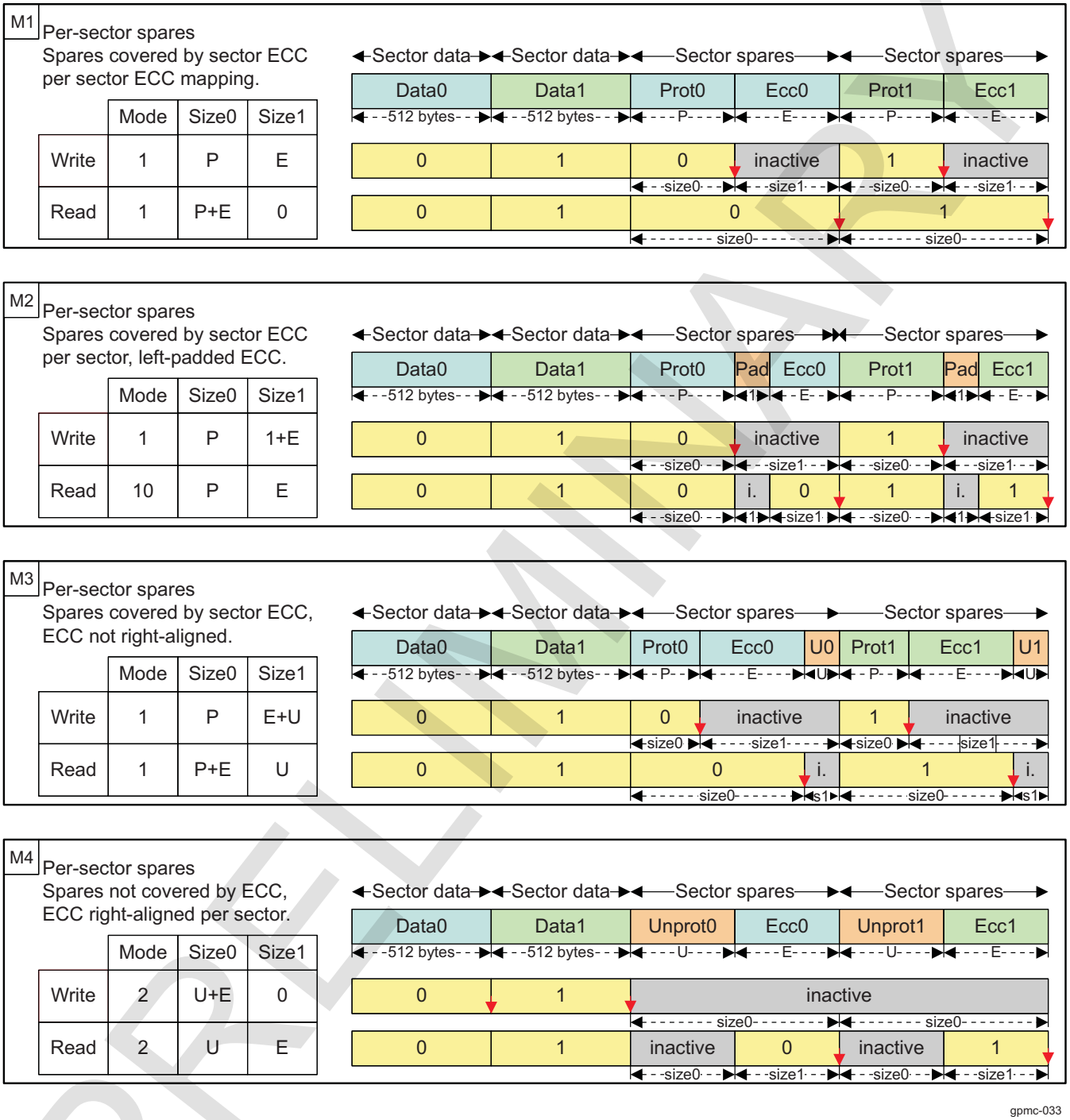
Figure 15-87. NAND Page Mapping and ECC: Per-Sector Schemes



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15.4.4.13.3.2.3.2 Pooled Spare Mapping

In the schemes below, the spare area is pooled for the page.

- The ECC of each sector is aligned at the end of the spare area.
- The non-ECC spare data may or may not be covered by the ECC of sector 0

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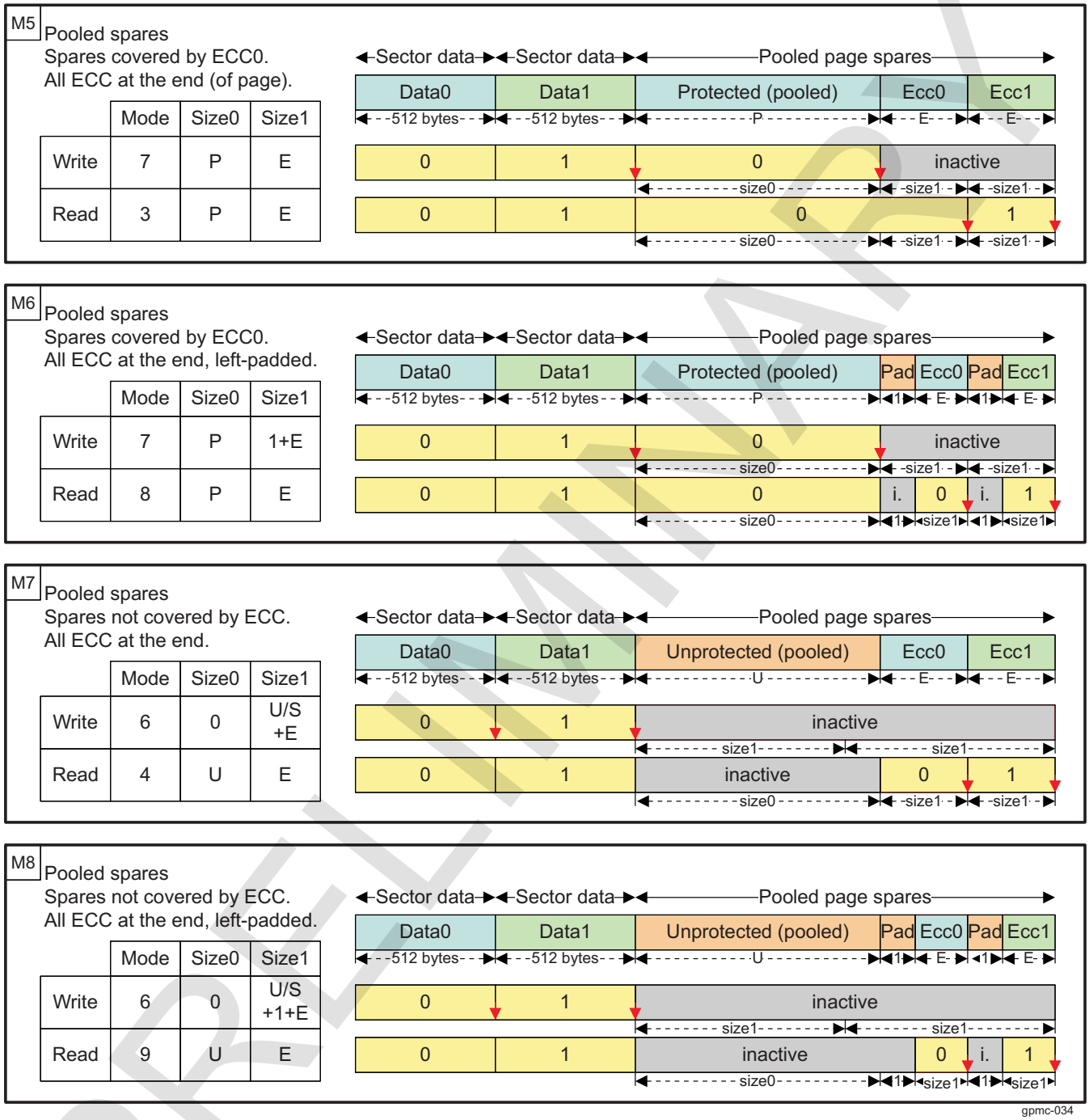
Figure 15-88. NAND Page Mapping and ECC: Pooled Spare Schemes



15.4.4.13.3.2.3.3 Per-Sector Spare Mapping, with ECC Separated at the End of the Page

In these schemes, each 512-byte sector of the main area is associated with 2 sections of the spare area.

- ECC section, all aligned at the end of the page
- other data section, aligned before the ECCs, each of which may or may not be protected by its sectors ECC

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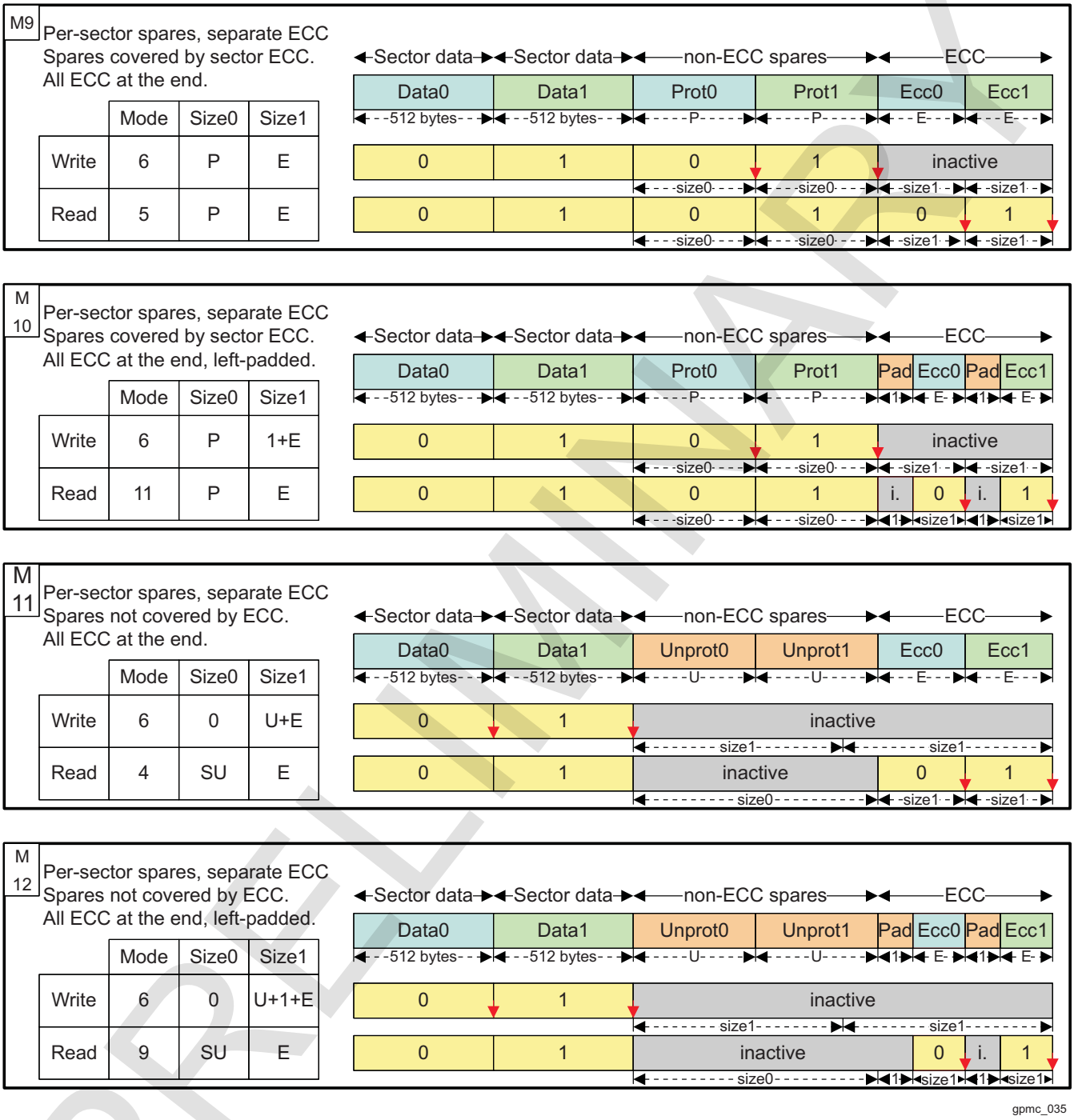
Figure 15-89. NAND Page Mapping and ECC: Per-Sector Schemes, with Separate ECC



15.4.4.13.4 Prefetch and Write-Posting Engine

NAND device data access cycles are usually much slower than the MPU system frequency; such NAND read or write accesses issued by the processor will impact the overall system performance, especially considering long read or write sequences required for NAND page loading or programming. To minimize this effect on system performance, the GPMC includes a prefetch and write-posting engine, which can be used to read from or write to any chip-select location in a buffered manner.

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The prefetch and write-posting engine is a simplified embedded-access requester that presents requests to the access engine on a user-defined chip-select target. The access engine interleaves these requests with any request coming from the L3 interface; as a default the prefetch and write-posting engine has the lowest priority.

The prefetch and write-posting engine is dedicated to data-stream access (as opposed to random data access); thus, it is primarily dedicated to NAND support. The engine does not include an address generator; the request is limited to chip-select target identification. It includes a 64-byte FIFO associated with a DMA request synchronization line, for optimal DMA-based use.

The prefetch and write-posting engine uses an embedded 64 bytes (32 16-bit word) FIFO to prefetch data from the NAND device in read mode (prefetch mode) or to store host data to be programmed into the NAND device in write mode (write-posting mode). The FIFO draining and filling (read and write) can be controlled either by the MPU through interrupt synchronization (an interrupt is triggered whenever a programmable threshold is reached) or the sDMA through DMA request synchronization, with a programmable request byte size in both prefetch or posting mode.

The prefetch and write-posting engine includes a single memory pool. Therefore, only one mode, read or write, can be used at any given time. In other words, the prefetch and write-posting engine is a single-context engine that can be allocated to only one chip-select at a time for a read prefetch or a write-posting process.

The engine does not support atomic command and address phase programming and is limited to linear memory read or write access. In consequence, it is limited to NAND data-stream access. The engine relies on the MPU NAND software driver to control block and page opening with the correct data address pointer initialization, before the engine can read from or write to the NAND memory device.

Once started, the engine data reads and writes sequencing is solely based on FIFO location availability and until the total programmed number of bytes is read or written.

Any host-concurrent accesses to a different chip-select are correctly interleaved with ongoing engine accesses. The engine has the lowest priority access so that host accesses to a different chip-select do not suffer a large latency.

A round-robin arbitration scheme can be enabled to ensure minimum bandwidth to the prefetch and write-posting engine in the case of back-to-back direct memory requests to a different chip-select. If the GPMC_PREFETCH_CONFIG1[23] PFPWENROUNDROBIN bit is enabled, the arbitration grants the prefetch and write posting engine access to the GPMC bus for a number of requests programmed in the GPMC_PREFETCH_CONFIG1[19:16] PFPWWEIGHTEDPRIO field.

The prefetch/write-posting engine read or write request is routed to the access engine with the chip-select destination ID. After the required arbitration phase, the access engine processes the request as a single access with the data access size equal to the device size specified in the corresponding chip-select configuration.

NOTE: The destination chip-select configuration must be set to the NAND protocol-compatible configuration for which address lines are not used (the address bus is not changed from its current value). Selecting a different chip-select configuration can produce undefined behavior.

15.4.4.13.4.1 General Facts About the Engine Configuration

The engine can be configured only if the GPMC_PREFETCH_CONTROL[0] STARTENGINE bit is deasserted.

The engine must be correctly configured in prefetch or write-posting mode and must be linked to a NAND chip-select before it can be started. The chip-select is linked using the GPMC_PREFETCH_CONFIG1[26:24] ENGINECSSELECTOR field.

In both prefetch and write-posting modes, the engine respectively uses byte or 16-bit word access requests for an 8- or 16-bit-wide NAND device attached to the linked chip-select. The FIFOTHRESHOLD and TRANSFERCOUNT fields must be programmed accordingly as a number of bytes.

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When the GPMC_PREFETCH_CONFIG1[7] ENABLEENGINE bit is set, the FIFO entry on the L3 interconnect port side is accessible at any address in the associated chip-select memory region. When the ENABLEENGINE bit is set, any host access to this chip-select is rerouted to the FIFO input. Directly accessing the NAND device linked to this chip-select from the host is still possible through the GPMC_NAND_COMMAND_i, GPMC_NAND_ADDRESS_i, and GPMC_NAND_DATA_i registers (where i = 0 to 7).

The FIFO entry on the L3 interconnect port can be accessed with byte, 16-bit word, or 32-bit word access size, according to little-endian format, even though the FIFO input is 32 bits wide.

The FIFO control is made easier through the use of interrupts or DMA requests associated with the FIFOTHRESHOLD bit field. The GPMC_PREFETCH_STATUS[30:24] FIFOPOINTER field monitors the number of available bytes to be read in prefetch mode or the number of free empty slots which can be written in write-posting mode. The GPMC_PREFETCH_STATUS[13:0] COUNTVALUE field monitors the number of remaining bytes to be read or written by the engine according to the TRANSFERCOUNT value. The FIFOPOINTER and COUNTVALUE bit fields are always expressed as a number of bytes even if a 16-bit wide NAND device is attached to the linked chip-select.

In prefetch mode, when the FIFOPOINTER equals 0, that is, the FIFO is empty, a host read access receives the byte last read from the FIFO as its response. In case of 32-bit word or 16-bit word read accesses, the last byte read from the FIFO is copied the required number of times to fit the requested word size. In write-posting mode, when the FIFOPOINTER equals 0, that is, the FIFO is full, a host write overwrites the last FIFO byte location. There is no underflow or overflow error reporting in the GPMC.

15.4.4.13.4.2 Prefetch Mode

The prefetch mode is selected when the GPMC_PREFETCH_CONFIG1[0] ACCESSMODE bit is cleared.

The MPU NAND software driver must issue the block and page opening (READ) command with the correct data address pointer initialization before the engine can be started to read from the NAND memory device. The engine is started by asserting the GPMC_PREFETCH_CONTROL[0] STARTENGINE bit. The STARTENGINE bit automatically clears when the prefetch process completes.

If required, the ECC calculator engine must be initialized (that is, reset, configured, and enabled) before the prefetch engine is started, so that the ECC is correctly computed on all data read by the prefetch engine.

When the GPMC_PREFETCH_CONFIG1[3] SYNCHROMODE bit is cleared, the prefetch engine starts requesting data as soon as the STARTENGINE bit is set. If using this configuration, the host must monitor the NAND device-ready pin so that it only sets the STARTENGINE bit when the NAND device is in a ready state, meaning data is valid for prefetching.

When the SYNCHROMODE bit is set, the prefetch engine starts requesting data when an active to inactive wait signal transition is detected. The transition detector must be cleared before any transition detection; see Section 15.4.4.13.2.2, *Ready Pin Monitored by Hardware Interrupt*. The GPMC_PREFETCH_CONFIG1[5:4] WAITPINSELECTOR field selects which gpmc_wait pin edge detector triggers the prefetch engine in this synchronized mode.

If the STARTENGINE bit is set after the NAND address phase (page opening command), the engine is effectively started only after the actual NAND address phase completion. To prevent GPMC stall during this NAND address phase, set the STARTENGINE bit field before NAND address phase completion when in synchronized mode. The prefetch engine will start when an active to inactive wait signal transition is detected. The STARTENGINE bit is automatically cleared on prefetch process completion.

The prefetch engine issues a read request to fill the FIFO with the amount of data specified by GPMC_PREFETCH_CONFIG2[13:0] TRANSFERCOUNT field.

Table 15-237. Prefetch Mode Configuration

Bit Field	Register	Value	Comments
STARTENGINE	GPMC_PREFETCH_CONTROL[0]	0	Prefetch engine can be configured only if STARTENGINE is set to 0.
ENGINECSSELECTOR	GPMC_PREFETCH_CONFIG1[26:24]	0 to 3	Selects the chip-select associated with a NAND device where the prefetch engine is active.

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Table 15-237. Prefetch Mode Configuration (continued)

Bit Field	Register	Value	Comments
ACCESSMODE	GPMC_PREFETCH_CONFIG1[0]	0	Selects prefetch mode
FIFOTHRESHOLD	GPMC_PREFETCH_CONFIG1[14:8]		Selects the maximum number of bytes read or written by the host on DMA or interrupt request
TRANSFERCOUNT	GPMC_PREFETCH_CONFIG2[13:0]		Selects the number of bytes to be read or written by the engine to the selected chip-select
SYNCHROMODE	GPMC_PREFETCH_CONFIG1[3]	0/1	Selects when the engine starts the access to the chip-select
WAITPINSELECT	GPMC_PREFETCH_CONFIG1[17:16]	0 to 1	Selects wait pin edge detector (if GPMC_PREFETCH_CONFIG1[3] SYNCHROMODE = 0x1)
ENABLEOPTIMIZEDACCESS	GPMC_PREFETCH_CONFIG1[27]	0/1	See Section 15.4.4.13.4.6, *Optimizing NAND Access Using the Prefetch and Write-Posting Engine*.
CYCLEOPTIMIZATION	GPMC_PREFETCH_CONFIG1[30:28]		Number of clock cycle removed to timing parameters
ENABLEENGINE	GPMC_PREFETCH_CONFIG1[7]	1	Engine enabled
STARTENGINE	GPMC_PREFETCH_CONTROL[0]	1	Starts the prefetch engine

15.4.4.13.4.3 FIFO Control in Prefetch Mode

The FIFO can be drained directly by the MPU or by an sDMA channel.

In MPU draining mode, the FIFO status can be monitored through the GPMC_PREFETCH_STATUS[30:24] FIFOPOINTER field or through the GPMC_PREFETCH_STATUS[16] FIFOTHRESHOLDSTATUS bit. The FIFOPOINTER indicates the current number of available data to be read; FIFOTHRESHOLDSTATUS set to 1 indicates that at least FIFOTHRESHOLD bytes are available from the FIFO.

An interrupt can be triggered by the GPMC if the GPMC_IRQENABLE[0] FIFOEVENTENABLE bit is set. The FIFO interrupt event is logged, and the GPMC_IRQSTATUS[0] FIFOEVENTSTATUS bit is set. To clear the interrupt, the MPU must read all the available bytes, or at least enough bytes to get below the programmed FIFO threshold, and the FIFOEVENTSTATUS bit must be cleared to enable further interrupt events. The FIFOEVENTSTATUS bit must always be reset prior to asserting the FIFOEVENTENABLE bit to clear any out-of-date logged interrupt event. This interrupt generation must be enabled after enabling the STARTENGINE bit.

Prefetch completion can be monitored through the GPMC_PREFETCH_STATUS[13:0] COUNTVALUE field. COUNTVALUE indicates the number of currently remaining data to be requested according to the TRANSFERCOUNT value. An interrupt can be triggered by the GPMC when the prefetch process is complete (that is, COUNTVALUE equals 0) if the GPMC_IRQENABLE[1] TERMINALCOUNTEVENTENABLE bit is set. At prefetch completion, the TERMINALCOUNT interrupt event is also logged, and the GPMC_IRQSTATUS[1] TERMINALCOUNTSTATUS bit is set. To clear the interrupt, the MPU must clear the TERMINALCOUNTSTATUS bit. The TERMINALCOUNTSTATUS bit must always be cleared prior to asserting the TERMINALCOUNTEVENTENABLE bit to clear any out-of-date logged interrupt event.

NOTE: The COUNTVALUE value is only valid when the prefetch engine is active (started), and an interrupt is only triggered when COUNTVALUE reaches 0, that is, when the prefetch engine automatically goes from an active to an inactive state.

The number of bytes to be prefetched (programmed in TRANSFERCOUNT) must be a multiple of the

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programmed FIFOTHRESHOLD to trigger the correct number of interrupts allowing a deterministic and transparent FIFO control. If this guideline is respected, the number of ISR accesses is always required and the FIFO is always empty after the last interrupt is trigerred. In other cases, the TERMINALCOUNT interrupt must be used to read the remaining bytes in the FIFO (the number of remaining bytes being lower than the FIFOTHRESHOLD value).

In DMA draining mode, the GPMC_PREFETCH_CONFIG1[2] DMAMODE bit must be set so that the GPMC issues a DMA hardware request when at least FIFOTHRESHOLD bytes are ready to be read from the FIFO. The DMA channel owning this DMA request must be programmed so that the number of bytes programmed in FIFOTHRESHOLD is read from the FIFO during the DMA request process. The DMA request is kept active until this number of bytes has effectively been read from the FIFO, and no other DMA request can be issued until the ongoing active request is complete.

In prefetch mode, the TERMINALCOUNT event is also a source of DMA requests if the number of bytes to be prefetched is not a multiple of FIFOTHRESHOLD, the remaining bytes in the FIFO can be read by the DMA channel using the last DMA request. This assumes that the number of remaining bytes to be read is known and controlled through the DMA channel programming model.

Any potentially active DMA request is cleared when the prefetch engine goes from inactive to active prefetch (the STARTENGINE bit is set to 1). The associated DMA channel must always be enabled by the MPU after setting the STARTENGINE bit so that the out-of-date active DMA request does not trigger spurious DMA transfers.

15.4.4.13.4.4 Write-Posting Mode

The write-posting mode is selected when the GPMC_PREFETCH_CONFIG1[0] ACCESSMODE bit is set.

The MPU NAND software driver must issue the correct address pointer initialization command (page program) before the engine can start writing data into the NAND memory device. The engine starts when the GPMC_PREFETCH_CONTROL[0] STARTENGINE bit is set to 1. The STARTENGINE bit clears automatically when posting completes. When all data have been written to the NAND memory device, the MPU NAND software driver must issue the second cycle program command and monitor the status for programming process completion (adding ECC handling, if required).

If used, the ECC calculator engine must be started (configured, reset, and enabled) before the posting engine is started so that the ECC parities are properly calculated on all data written by the prefetch engine to the associated chip-select.

In write-posting mode, the GPMC_PREFETCH_CONFIG1[3] SYNCHROMODE bit must be cleared so that posting starts as soon as the STARTENGINE bit is set and the FIFO is not empty.

If the STARTENGINE bit is set after the NAND address phase (page program command), the STARTENGINE setting is effective only after the actual NAND command completion. To prevent GPMC stall during this NAND command phase, set the STARTENGINE bit field before the NAND address completion and ensure that the associated DMA channel is enabled after the NAND address phase.

The posting engine issues a write request when valid data are available from the FIFO and until the programmed GPMC_PREFETCH_CONFIG2[13:0] TRANSFERCOUNT accesses have been completed.

The STARTENGINE bit clears automatically when posting completes. When all data have been written to the NAND memory device, the MPU NAND software driver must issue the second cycle program command and monitor the status for programming process completion. The closing program command phase must only be issued when the full NAND page has been written into the NAND flash write buffer, including the spare area data and the ECC parities, if used.

Table 15-238. Write-Posting Mode Configuration

Bit Field	Register	Value	Comments
STARTENGINE	GPMC_PREFETCH_CONTROL[0]	0	Write-posting engine can be configured only if STARTENGINE is set to 0.
ENGINECSSELECTOR	GPMC_PREFETCH_CONFIG1[26:24]	0 to 3	Selects the chip-select associated with a NAND device where the prefetch engine is active
ACCESSMODE	GPMC_PREFETCH_CONFIG1[0]	1	Selects write-posting mode

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Table 15-238. Write-Posting Mode Configuration (continued)

Bit Field	Register	Value	Comments
FIFOTHRESHOLD	GPMC_PREFETCH_CONFIG1[14:8]		Selects the maximum number of bytes read or written by the host on DMA or interrupt request
TRANSFERCOUNT	GPMC_PREFETCH_CONFIG2[13:0]		Selects the number of bytes to be read or written by the engine from/to the selected chip-select
SYNCHROMODE	GPMC_PREFETCH_CONFIG1[3]	0	Engine starts the access to chip-select as soon as STARTENGINE is set.
ENABLEOPTIMIZEDACCESS	GPMC_PREFETCH_CONFIG1[27]	0/1	See Section 15.4.4.13.4.6, *Optimizing NAND Access Using the Prefetch and Write-Posting Engine*.
CYCLEOPTIMIZATION	GPMC_PREFETCH_CONFIG1[30:28]		
ENABLEENGINE	GPMC_PREFETCH_CONFIG1[7]	1	Engine enabled
STARTENGINE	GPMC_PREFETCH_CONTROL[0]	1	Starts the prefetch engine

15.4.4.13.4.5 FIFO Control in Write-Posting Mode

The FIFO can be filled directly by the MPU or by an sDMA channel.

In MPU filling mode, the FIFO status can be monitored through the FIFOPOINTER or through the GPMC_PREFETCH_STATUS[16] FIFOTHRESHOLDSTATUS bit. FIFOPOINTER indicates the current number of available free byte places in the FIFO, and the FIFOTHRESHOLDSTATUS bit, when set, indicates that at least FIFOTHRESHOLD free byte places are available in the FIFO.

An interrupt can be issued by the GPMC if the GPMC_IRQENABLE[0] FIFOEVENTENABLE bit is set. When the interrupt is fired, the GPMC_IRQSTATUS[0] FIFOEVENTSTATUS bit is set. To clear the interrupt, the MPU must write enough bytes to fill the FIFO, or enough bytes to get below the programmed threshold, and the FIFOEVENTSTATUS bit must be cleared to get further interrupt events. The FIFOEVENTSTATUS bit must always be cleared prior to asserting the FIFOEVENTENABLE bit to clear any out-of-date logged interrupt event. This interrupt must be enabled after enabling the STARTENGINE bit.

The posting completion can be monitored through the GPMC_PREFETCH_STATUS[13:0] COUNTVALUE field. COUNTVALUE indicates the current number of remaining data to be written based on the TRANSFERCOUNT value. An interrupt is issued by the GPMC when the write-posting process completes (that is, COUNTVALUE equal to 0) if the GPMC_IRQENABLE[1] TERMINALCOUNTEVENTENABLE bit is set. When the interrupt is fired, the GPMC_IRQSTATUS[1] TERMINALCOUNTSTATUS bit is set. To clear the interrupt, the MPU must clear the TERMINALCOUNTSTATUS bit. The TERMINALCOUNTSTATUS bit must always be cleared prior to asserting the TERMINALCOUNTEVENTENABLE bit to clear any out-of-date logged interrupt event.

NOTE: The COUNTVALUE value is only valid if the write-posting engine is active and started, and an interrupt is only issued when COUNTVALUE reaches 0, that is, when the posting engine automatically goes from active to inactive.

In DMA filling mode, the DMAMode bit field in the GPMC_PREFETCH_CONFIG1[2] DMAMODE bit must be set so that the GPMC issues a DMA hardware request when at least FIFOTHRESHOLD bytes-free places are available in the FIFO. The DMA channel owning this DMA request must be programmed so that a number of bytes equal to the value programmed in the FIFOTHRESHOLD bit field are written into the FIFO during the DMA access. The DMA request remains active until the associated number of bytes has effectively been written into the FIFO, and no other DMA request can be issued until the ongoing active request has been completed.

Any potentially active DMA request is cleared when the prefetch engine goes from inactive to active prefetch (STARTENGINE set to 1). The associated DMA channel must always be enabled by the MPU after setting the STARTENGINE bit so that an out-of-date active DMA request does not trigger spurious DMA transfers.

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In write-posting mode, the DMA or the MPU fill the FIFO with no consideration to the associated byte enables. Any byte stored in the FIFO is written into the memory device.

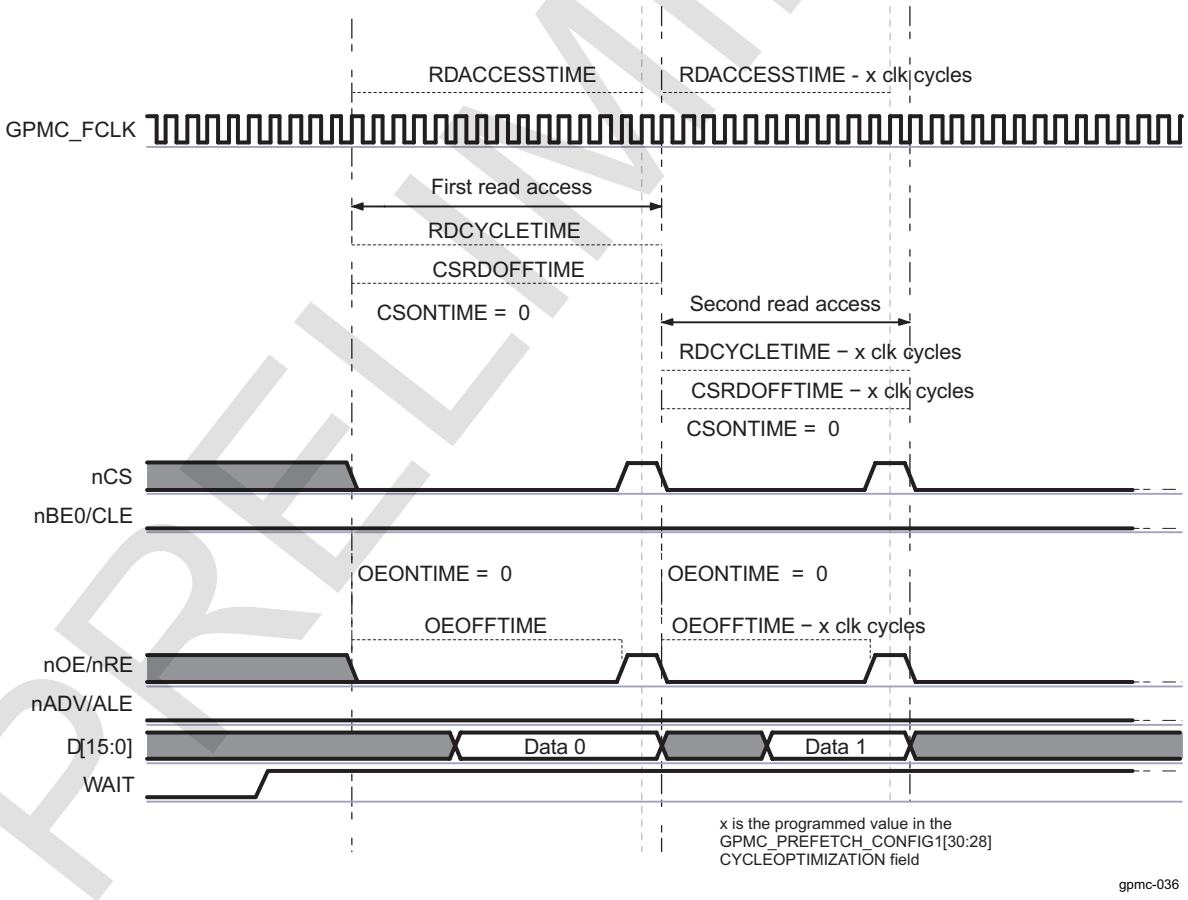
15.4.4.13.4.6 Optimizing NAND Access Using the Prefetch and Write-Posting Engine

Access time to a NAND memory device can be optimized for back-to-back accesses if the associated nCS signal is not deasserted between accesses. The GPMC access engine can track prefetch engine accesses to optimize the access timing parameter programmed for the allocated chip-select, if no accesses to other chip-selects (that is, interleaved accesses) occur. Similarly, the access engine also eliminates the CYCLE2CYCLEDELAY even if CYCLE2CYCLESAMECSEN is set. This capability is limited to the prefetch and write-posting engine accesses, and MPU accesses to a NAND memory device (through the defined chip-select memory region or through the GPMC_NAND_DATA_i location, i = 0 to 7) are never optimized.

The GPMC_PREFETCH_CONFIG1[27] ENABLEOPTIMIZEDACCESS bit must be set to enable optimized accesses. To optimize access time, the GPMC_PREFETCH_CONFIG1[30:28] CYCLEOPTIMIZATION field defines the number of GPMC_FCLK cycles to be suppressed from the RDCYCLETIME, WRCYCLETIME, RDACCESSTIME, WRACCESSTIME, CSOFFTIME, ADVOFFTIME, OEOFFTIME, and WEOFFTIME timing parameters.

Figure 15-90 highlights that, in the case of back-to-back accesses to the NAND flash through the prefetch engine, CYCLE2CYCLESAMECSEN is forced to 0 when using optimized accesses. The first access uses the regular timing settings for this chip-select. All accesses after this one use settings reduced by x clock cycles, x being defined by the GPMC_PREFETCH_CONFIG1[30:28] CYCLEOPTIMIZATION field.

Figure 15-90. NAND Read Cycle Optimization Timing Description



15.4.4.13.4.7 Interleaved Accesses Between Prefetch and Write-Posting Engine and Other Chip-Selects

Any on-going read or write access from the prefetch and write-posting engine is completed before an

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access to any other chip-select can be initiated. As a default, the arbiter uses a fixed-priority algorithm, and the prefetch and write-posting engine has the lowest priority. The maximum latency added to access starting time in this case equals the RDCYCLETIME or WRCYCLETIME (optimized or not) plus the requested BUSTURNAROUND delay for bus turnaround completion programmed for the chip-select to which the NAND device is connected to.

Alternatively, a round-robin arbitration can be used to prioritize accesses to the external bus. This arbitration scheme is enabled by setting the GPMC_PREFETCH_CONFIG1[23] PFPWENROUNDROBIN bit. When a request to another chip-select is received while the prefetch and write-posting engine is active, priority is given to the new request. The request processed thereafter is the prefetch and write-posting engine request, even if another interconnect request is passed in the mean time. The engine keeps control of the bus for an additional number of requests programmed in the GPMC_PREFETCH_CONFIG1[19:16] PFPWWEIGHTEDPRIO bit field. Control is then passed to the direct interconnect request.

As an example, the round-robin arbitration scheme is selected with PFPWWEIGHTEDPRIO set to 0x2. Considering the prefetch and write-posting engine and the interconnect interface are always requesting access to the external interface, the GPMC grants priority to the direct interconnect access for one request. The GPMC then grants priority to the engine for three requests, and finnaly back to the direct interconnect access, until the arbiter is reset when one of the two initiators stops initiating requests.

15.4.5 GPMC Basic Programming Model

15.4.5.1 GPMC High-Level Programming Model Overview

The goal of the basic high-level programming model is to introduce a top down approach to users that need to configure the GPMC module.

Figure 15-91, Table 15-239, Table 15-240 and Table 15-241 show a programming model top level diagram for the GPMC, and the description of each step. Each block of the diagram is detailled in one of the following subsections through a set of registers to configure.

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Figure 15-91. Programming Model Top Level Diagram

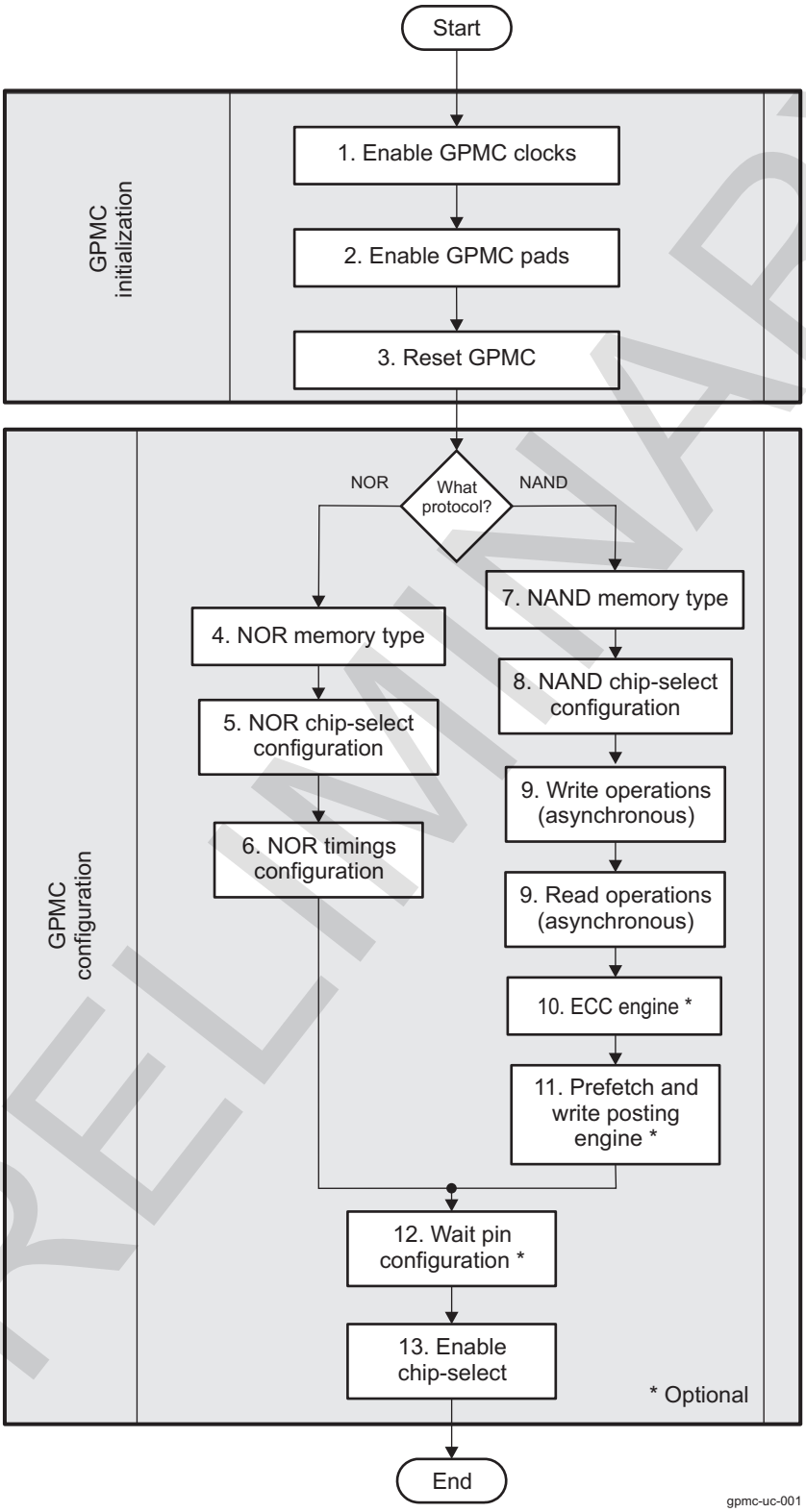

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Table 15-239. GPMC Initialization

Step	Description
Enable GPMC clocks	Module interface and functional clocks must be enabled. See Chapter 3, *Power, Reset, and Clock Management*.
Enable GPMC pads	Module-specific pad muxing and configuration must be set in the control module. See Chapter 18, *Control Module*.
Reset GPMC	See Table 15-242

Table 15-240. GPMC Configuration in NOR Mode

Step	Description
NOR Memory Type	See Table 15-243
NOR Chip-Select Configuration	See Table 15-244
NOR Timings Configuration	See Table 15-245
Wait Pin Configuration	See Table 15-253
Enable Chip-Select	See Table 15-254

Table 15-241. GPMC Configuration in NAND Mode

Step	Description
NAND Memory Type	See Table 15-248
NAND Chip-Select Configuration	See Table 15-249
Write Operations (Asynchronous)	See Table 15-250
Read Operations (Asynchronous)	See Table 15-250
ECC Engine	See Table 15-251
Prefetch and Write-Posting Engine	See Table 15-252
Wait Pin Configuration	See Table 15-253
Enable Chip-Select	See Table 15-254

15.4.5.2 GPMC Initialization

Table 15-270 describes the settings required to prepare the GPMC, that is enabling its clock, its pads, and proceeding to a GPMC reset.

Table 15-242. Reset GPMC

Sub-process Name	Register / Bit Field	Value
Start a software reset	GPMC_SYSCONFIG[1] SOFTRESET	0x1
Wait until	GPMC_SYSSTATUS[0] RESETDONE =	0x1

15.4.5.3 GPMC Configuration in NOR Mode

This section gives a generic configuration for parameters related to the NOR memory connected to the GPMC.

Table 15-243. NOR Memory Type

Sub-process Name	Register / Bit Field	Value
Set the NOR protocol	GPMC_CONFIG1_i[11:10] DEVICETYPE	0x0
Set a device size	GPMC_CONFIG1_i[13:12] DEVICESIZE	x
Select an address and data multiplexing protocol	GPMC_CONFIG1_i[9] MUXADDDATA	x
Set the attached device page length	GPMC_CONFIG1_i[24:23] ATTACHEDDEVICEPAGELENGTH	x
Set the wrapping burst capabilities	GPMC_CONFIG1_i[31] WRAPBURST	x

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Table 15-243. NOR Memory Type (continued)

Sub-process Name	Register / Bit Field	Value
Select a timing signals latencies factor	GPMC_CONFIG1_i[4] TIMEPARAGRANULARITY	x
Select an output clock frequency (1)	GPMC_CONFIG1_i[1:0] GPMCFCLKDIVIDER	x
Choose an output clock activation time (1)	GPMC_CONFIG1_i[26:25] CLKACTIVATIONTIME	x
Set a single or multiple access for read operations (1)	GPMC_CONFIG1_i[30] READMULTIPLE	x
Set a synchronous or asynchronous mode for read operations	GPMC_CONFIG1_i[29] READTYPE	x
Set a single or multiple access for write operations	GPMC_CONFIG1_i[28] WRITEMULTIPLE	x
Set a synchronous or asynchronous mode for write operations	GPMC_CONFIG1_i[27] WRITETYPE	x

(1) Only applies to synchronous configurations (or non-multiplexed async for the multiple access one).

Table 15-244. NOR Chip-Select Configuration

Sub-process Name	Register / Bit Field	Value
Select the chip-select base address	GPMC_CONFIG7_i[5:0] BASEADDRESS	x
Select the chip-select mask address	GPMC_CONFIG7_i[11:8] MASKADDRESS	x

Table 15-245. NOR Timings Configuration

Sub-process Name	Register / Bit Field	Value
Configure adequate timing parameters in various memory modes	See Section 15.4.5.6, *GPMC Timing Parameters*	

Table 15-246. Wait Pin Configuration

Sub-process Name	Register / Bit Field	Value
Enable or disable wait pin monitoring for read operations	GPMC_CONFIG1_i[22] WAITREADMONITORING	x
Enable or disable wait pin monitoring for write operations	GPMC_CONFIG1_i[21] WAITWRITEMONITORING	x
Select a wait pin monitoring time	GPMC_CONFIG1_i[19:18] WAITMONITORINGTIME	x
Choose the input wait pin for the chip-select	GPMC_CONFIG1_i[17:16] WAITPINSELECT	x

Table 15-247. Enable Chip-Select

Sub-process Name	Register / Bit Field	Value
When all parameters are configured, enable the chip-select	GPMC_CONFIG7_i[6] CSVALID	x

15.4.5.4 GPMC Configuration in NAND Mode

This section gives a generic configuration for parameters related to the NAND memory connected to the GPMC.

Table 15-248. NAND Memory Type

Sub-process Name	Register / Bit Field	Value
Set the NAND protocol	GPMC_CONFIG1_i[11:10] DEVICETYPE	0x2
Set a device size	GPMC_CONFIG1_i[13:12] DEVICESIZE	x
Set the address and data multiplexing protocol to non-multiplexed attached device	GPMC_CONFIG1_i[9] MUXADDDATA	0x0
Select a timing signals latencies factor	GPMC_CONFIG1_i[4] TIMEPARAGRANULARITY	x
Set a synchronous or asynchronous mode and a single or multiple access for read and write operations	See Section 15.4.5.5, *Set Memory Access*	x

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Table 15-249. NAND Chip-Select Configuration

Sub-process Name	Register / Bit Field	Value
Select the chip-select base address	GPMC_CONFIG7_i[5:0] BASEADDRESS	x
Select the chip-select minimum granularity (16M bytes)	GPMC_CONFIG7_i[11:8] MASKADDRESS	x

Table 15-250. Asynchronous Read and Write Operations

Sub-process Name	Register / Bit Field	Value
Configure adequate timing parameters in asynchronous modes	See Section 15.4.5.6, *GPMC Timing Parameters*	

Table 15-251. ECC Engine

Sub-process Name	Register / Bit Field	Value
Select the ECC result register where the first ECC computation is stored (Only applies to Hamming)	GPMC_ECC_CONTROL[3:0] ECCPOINTER	x (1)
Clear all ECC result registers	GPMC_ECC_CONTROL[8] ECCCLEAR	Write '1' to clear.
Define ECCSIZE0 and ECCSIZE1	GPMC_ECC_SIZE_CONFIG[19:12] ECCSIZE0 and [29:22] ECCSIZE1	x (2)
Select the size of each of the 9 result registers (size specified by ECCSIZE0 or ECCSIZE1)	GPMC_ECC_SIZE_CONFIG[j-1] ECCjRESULTSIZE where j = 1 to 9	x
Select the chip-select where ECC is computed	GPMC_ECC_CONFIG[3:1] ECCCS	x
Select the Hamming code or BCH code ECC algorithm in use	GPMC_ECC_CONFIG[16] ECCALGORITHM	x
Select word size for ECC calculation	GPMC_ECC_CONFIG[7] ECC16B	x
If the BCH code is used, Set an error correction capability and Select a number of sectors to process	GPMC_ECC_CONFIG[13:12] ECCBCHTSEL and GPMC_ECC_CONFIG[6:4] ECCTOPSECTOR	x
Enable the ECC computation	GPMC_ECC_CONFIG[0] ECCENABLE	0x1

(1) This parameter depends on the numbers of sectors in a page.
(2) Depends on the size of each sector in the NAND page.

Table 15-252. Prefetch and Write-Posting Engine

Sub-process Name	Register / Bit Field	Value
Disable the engine before configuration	GPMC_PREFETCH_CONTROL[0] STARTENGINE	0x0
Select the chip-select associated with a NAND device where the prefetch engine is active	GPMC_PREFETCH_CONFIG1[26:24] ENGINECSSELECTOR	x
Select access direction through prefetch engine, read or write.	GPMC_PREFETCH_CONFIG1[0] ACCESSMODE	x
Select the threshold used to issue a DMA request	GPMC_PREFETCH_CONFIG1[14:8] FIFOTHRESHOLD	x
Select either DMA synchronized mode or software manual mode.	GPMC_PREFETCH_CONFIG1[2] DMAMODE	x
Select if the engine immediately starts accessing the memory upon STARTENGINE assertion or if hardware synchronization based on a WAIT signal is used.	GPMC_PREFETCH_CONFIG1[3] SYNCHROMODE	x
Select which wait pin edge detector should start the engine in synchronized mode	GPMC_PREFETCH_CONFIG1[5:4] WAITPINSELECTOR	x
Enter a number of clock cycles removed to timing parameters (For all back-to-back accesses to the NAND flash but not the first one)	GPMC_PREFETCH_CONFIG1[30:28] CYCLEOPTIMIZATION	x
Enable the prefetch postwite engine	GPMC_PREFETCH_CONFIG1[7] ENABLEENGINE	0x1
Select the number of bytes to be read or written by the engine to the selected chip-select	GPMC_PREFETCH_CONFIG2[13:0] TRANSFERCOUNT	x
Start the prefetch engine	GPMC_PREFETCH_CONTROL[0] STARTENGINE	0x1

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Table 15-253. Wait Pin Configuration

Sub-process Name	Register / Bit Field	Value
Selects when the engine starts the access to CS	GPMC_PREFETCH_CONFIG1[3] SYNCHROMODE	x
Select which wait pin edge detector should start the engine in synchronized mode	GPMC_PREFETCH_CONFIG1[5:4] WAITPINSELECTOR	x

Table 15-254. Enable Chip-Select

Sub-process Name	Register / Bit Field	Value
When all parameters are configured, enable the chip-select	GPMC_CONFIG7_i[6] CSVALID	x

15.4.5.5 Set Memory Access

This section details the bit field to configure to set the GPMC in various memory modes.

Table 15-255. Mode Parameters Check List Table

Register	Bit	Bit field name	Asynchronous				Synchronous			
			Single Read Access	Single Write Access	Multiple Read (Page) Access	Multiple Write (Page) Access	Single Read Access	Single Write Access	Multiple Read (Burst) Access	Multiple Write (Burst) Access
GPMC_CONFIG1_i	30	READMULTIPLE	0x0	-	0x1 (1)	N/S	0x0	-	0x1	-
GPMC_CONFIG1_i	29	READTYPE	0x0	-	0x0 (1)	N/S	0x1	-	0x1	-
GPMC_CONFIG1_i	28	WRITEMULTIPLE	-	0x0	- (1)	N/S	-	0x0	-	0x1
GPMC_CONFIG1_i	27	WRITETYPE	-	0x0	- (1)	N/S	-	0x1	-	0x1

(1) Multiple read is not supported in address/data- and AAD-multiplexed modes. Multiple read is supported in Nonmultiplexed mode.

Table 15-256. Access Type Parameters Check List Table

Register	Bit	Bit field name	Access Type		
			Non-mux	Address /Data Mux	AAD-mux
GPMC_CONFIG1_i	9:8	MUXADDDATA	0x0	0x2	0x1
GPMC_CONFIG	1	LIMITEDADDRESS (1)	0x1	0x0	0x0

(1) This parameter applies to all chip-selects. There is no per-CS configuration for this parameter.

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15.4.5.6 GPMC Timing Parameters

Figure 15-92 shows a programming model diagram for the NOR interfacing timing parameters.

Figure 15-92. NOR Interfacing Timing Parameters Diagram

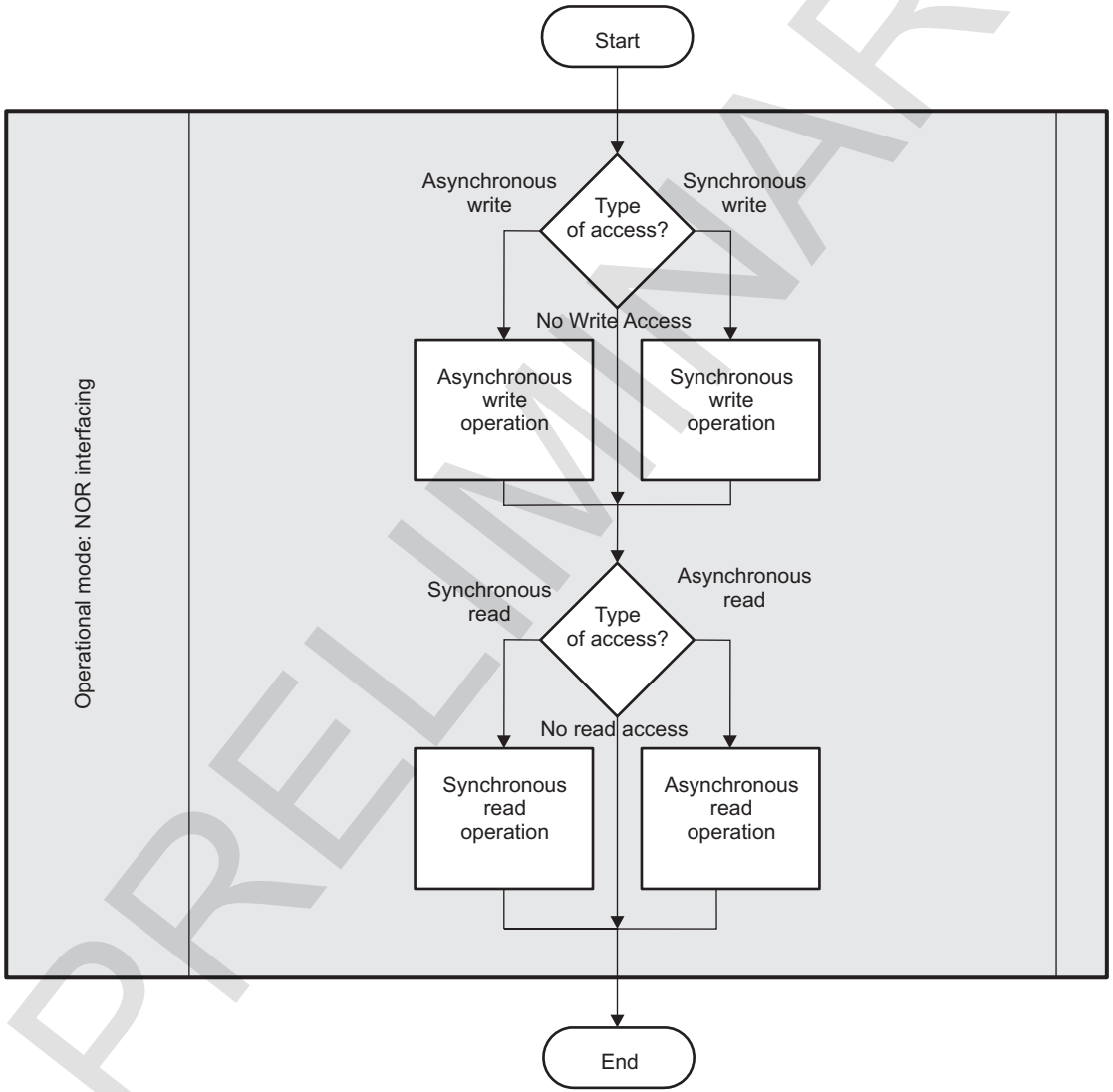

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Table 15-257 lists bit fields to configure adequate timing parameter in various memory modes.

Table 15-257. Timing Parameters

			Asynchronous			Synchronous				Access Type		
Register	Bit	Bit field name	Single Read Access	Single Write Access	Multiple Read (Page) access	Single Read Access	Single Write Access	Multiple Read (Burst) Access	Multiple Write (Burst) Access	Non-multiplexed	Address /Data-multiplexed	AAD-multiplexed
GPMC_CONFIG1_i	9	MUXADDDATA	y	y	y	y	y	y	y	y	y	y
GPMC_CONFIG1_i	29	READTYPE	y		y	y		y		y	y	y
GPMC_CONFIG1_i	30	READMULTIPLE	y		y	y		y		y	y	y
GPMC_CONFIG1_i	27	WRITETYPE		y			y		y	y	y	y
GPMC_CONFIG1_i	28	WRITEMULTIPLE		y			y		y	y	y	y
GPMC_CONFIG1_i	31	WRAPBURST						y	y	y	y	y
GPMC_CONFIG1_i	26:25	CLKACTIVATIONTIME				y	y	y	y	y	y	y
GPMC_CONFIG1_i	19:18	WAITMONITORINGTIME	y	y	y	y	y	y	y	y	y	y
GPMC_CONFIG1_i	4	TIMEPARAGRANULARITY	y	y	y	y	y	y	y	y	y	y
GPMC_CONFIG2_i	20:16	CSWROFFTIME		y			y		y	y	y	y
GPMC_CONFIG2_i	12:8	CSRDOFFTIME	y		y	y		y		y	y	y
GPMC_CONFIG2_i	7	CSEXTRADELAY	y	y	y	y	y	y	y	y	y	y
GPMC_CONFIG2_i	3:0	CSONTIME	y	y	y	y	y	y	y	y	y	y
GPMC_CONFIG3_i	30:28	ADVAADMUXWROFFTIME		y			y		y			y
GPMC_CONFIG3_i	30:29	ADVAADMUXRDOFFTIME	y		y	y		y				y
GPMC_CONFIG3_i	6:4	ADVAADMUXONTIME	y	y	y	y	y	y	y			y
GPMC_CONFIG3_i	20:16	ADVWROFFTIME		y			y		y	y	y	y
GPMC_CONFIG3_i	12:8	ADVRDOFFTIME	y		y	y		y		y	y	y
GPMC_CONFIG3_i	7	ADVEXTRADELAY	y	y	y	y	y	y	y	y	y	y
GPMC_CONFIG3_i	3:0	ADVONTIME	y	y	y	y	y	y	y	y	y	y
GPMC_CONFIG4_i	15:13	OEAADMUXOFFTIME	y	y	y	y	y	y	y			y
GPMC_CONFIG4_i	6:4	OEAADMUXONTIME	y	y	y	y	y	y	y			y
GPMC_CONFIG4_i	28:24	WEOFFTIME		y			y		y	y	y	y
GPMC_CONFIG4_i	23	WEEXTRADELAY		y			y		y	y	y	y
GPMC_CONFIG4_i	19:16	WEONTIME		y			y		y	y	y	y
GPMC_CONFIG4_i	12:8	OEOFFTIME	y		y	y		y		y	y	y
GPMC_CONFIG4_i	7	OEEXTRADELAY	y		y	y		y		y	y	y
GPMC_CONFIG4_i	3:0	OEONTIME	y		y	y		y		y	y	y
GPMC_CONFIG5_i	27:24	PAGEBURSTACCESSTIME			y			y	y	y	y	y

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Table 15-257. Timing Parameters (continued)

			Asynchronous			Synchronous			Access Type		
GPMC_CONFIG5_i	20:16	RDACCESSTIME	y		y	y			y	y	y
GPMC_CONFIG5_i	12:8	WRCYCLETIME		y			y	y	y	y	y
GPMC_CONFIG5_i	4:0	RDCYCLETIME	y		y	y			y	y	y
GPMC_CONFIG6_i	28:24	WRACCESSTIME		y			y	y	y	y	y
GPMC_CONFIG6_i	19:16	WRDATAONADMUXBUS		y			y	y		y	y
GPMC_CONFIG6_i	11:8	CYCLE2CYCLEDELAY	y	y	y	y	y	y	y	y	y	y
GPMC_CONFIG6_i	7	CYCLE2CYCLESAMECSEN	y	y	y	y	y	y	y	y	y	y
GPMC_CONFIG6_i	6	CYCLE2CYCLEDIFFCSEN	y	y	y	y	y	y	y	y	y	y
GPMC_CONFIG6_i	3:0	BUSTURNAROUND	y	y	y	y	y	y	y	y	y	y
GPMC_CONFIG7_i	6	CSVALID	y	y	y	y	y	y	y	y	y	y

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15.4.5.6.1 GPMC Timing Parameters Formulas

This section intends to help the user to calculate the GPMC timing bit fields values. Formulas are not listed exhaustively.

The section details:

- NAND Flash Interface Timing Parameters Formulas
- Synchronous NOR Flash Timing Parameters Formulas
- Asynchronous NOR Flash Timing Parameters Formulas

15.4.5.6.1.1 NAND Flash Interface Timing Parameters Formulas

This section lists formulas to use in order to calculate NAND timing parameters. This is the case when GPMC_CONFIG1_i[11:10] DEVICETYPE = 0x2. Table 15-258 details NAND timing parameters.

Table 15-258. NAND Formulas Description Table

Configuration Parameter	Unit	Description
A	ns	Pulse duration - gpmc_nwe valid time
B	ns	Delay time - gpmc_ncs valid to gpmc_nwe valid
C	ns	Delay time - gpmc_nbe0_cle/gpmc_nadv_ale high to gpmc_nwe valid
D	ns	Delay time - gpmc_ad[15:0] valid to gpmc_nwe valid
E	ns	Delay time - gpmc_nwe invalid to gpmc_ad[15:0] invalid
F	ns	Delay time - gpmc_nwe invalid to gpmc_nbe0_cle/gpmc_nadv_ale invalid
G	ns	Delay time - gpmc_nwe invalid to gpmc_ncs invalid
H	ns	Cycle time - Write cycle time
I	ns	Delay time - gpmc_ncs valid to gpmc_noe valid
J	ns	Setup time - gpmc_ad[15:0] valid to gpmc_noe invalid
K	ns	Pulse duration - gpmc_noe valid time
L	ns	Cycle time - Read cycle time
M	ns	Delay time - gpmc_noe invalid to gpmc_ncs invalid

The configuration parameters are calculated through the following formulas.

A = (WEOffTime - WEOnTime) * (TimeParaGranularity + 1) * GPMC_FCLK period

B = ((WEOnTime - CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (WEExtraDelay - CSExtraDelay)) * GPMC_FCLK period

C = ((WEOnTime - ADVOnTime) * (TimeParaGranularity + 1) + 0.5 * (WEExtraDelay - ADVExtraDelay)) * GPMC_FCLK period

D = (WEOnTime * (TimeParaGranularity + 1) + 0.5 * WEExtraDelay) * GPMC_FCLK period

E = (WrCycleTime - WEOffTime * (TimeParaGranularity + 1) - 0.5 * WEExtraDelay) * GPMC_FCLK period

F = (ADVWrOffTime - WEOffTime * (TimeParaGranularity + 1) + 0.5 * (ADVExtraDelay - WEExtraDelay) * GPMC_FCLK period

G = (CSWrOffTime - WEOffTime * (TimeParaGranularity + 1) + 0.5 * (CSExtraDelay - WEExtraDelay) * GPMC_FCLK period

H = WrCycleTime * (1 + TimeParaGranularity) * GPMC_FCLK period

I = ((OEOnTime - CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (OEExtraDelay - CSExtraDelay)) * GPMC_FCLK period

J = ((AccessTime - OEOffTime) * (TimeParaGranularity + 1) - 0.5 * OEExtraDelay)) * GPMC_FCLK period

K = (OEOffTime - OEOnTime) * (1 + TimeParaGranularity) * GPMC_FCLK period

L = RdCycleTime * (1 + TimeParaGranularity) * GPMC_FCLK period

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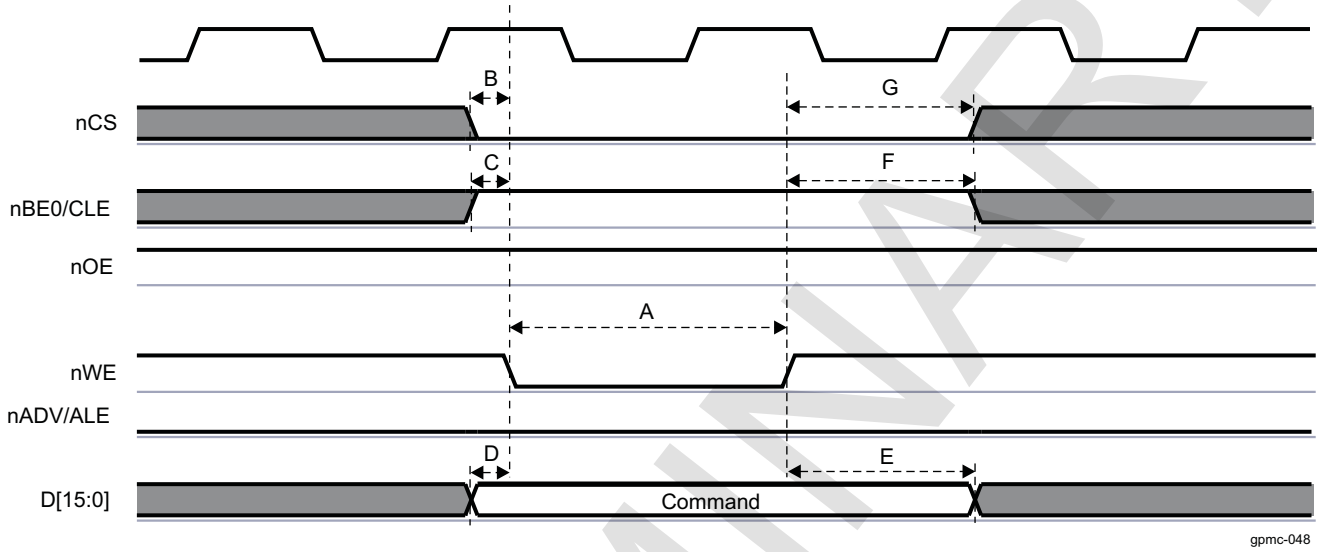
M = (CSRdOffTime - OEOffTime * (TimeParaGranularity + 1) + 0.5 * (CSExtraDelay - OEExtraDelay) * GPMC_FCLK period

Figure 15-93 shows a command latch cycle timing simplified example where formulas are associated with signal waves.

Figure 15-93. NAND Command Latch Cycle Timing Simplified Example



15.4.5.6.1.2 Synchronous NOR Flash Timing Parameters Formulas

This section lists all formulas to use in order to calculate synchronous NOR timing parameters. This is the case when GPMC_CONFIG1_i[11:10] DEVICETYPE = 0x0 and when READTYPE or WRITETYPE are set to synchronous mode.

Table 15-259. Synchronous NOR Formulas Description Table

Configuration Parameter	Unit	Description
A	ns	Pulse duration - gpmc_ncs low
B	ns	Delay time - address bus valid to gpmc_clk first edge
		Delay time - gpmc_nbe0_cle/gpmc_nbe1 valid to gpmc_clk first edge
C	ns	Pulse duration - gpmc_nbe0_cle/gpmc_nbe1 low
D	ns	Delay time - gpmc_clk rising edge to gpmc_nbe0_cle/gpmc_nbe1 invalid
		Delay time - gpmc_clk rising edge to gpmc_nadv_ale invalid
E	ns	Delay time - gpmc_clk rising edge to gpmc_ncs invalid
		Delay time - gpmc_clk rising edge to gpmc_noe invalid
F	ns	Delay time - gpmc_clk rising edge to gpmc_ncs transition
G	ns	Delay time - gpmc_clk rising edge to gpmc_nadv_ale transition
H	ns	Delay time - gpmc_clk rising edge to gpmc_noe transition
I	ns	Delay time - gpmc_clk rising edge to gpmc_nwe transition
J	ns	Delay time - gpmc_clk rising edge to gpmc_ad data bus transition
		Delay time - gpmc_clk rising edge to gpmc_nbe0_cle/gpmc_nbe1 transition
K	ns	Pulse duration - gpmc_nadv_ale low
L	ns	Delay time - gpmc_wait invalid to first data latching gpmc_clk edge

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The configuration parameters are calculated through the following formulas.

1. For single read accesses:
   A = (CSRDOFFTIME - CSONTIME) * (TIMEPARAGRANULARITY + 1) * GPMC_FCLK period
   C = RDCYCLETIME * (TIMEPARAGRANULARITY + 1) * GPMC_FCLK period
   D = (RDCYCLETIME - ACCESSTIME) * GPMC_FCLK period
   E = (CSRDOFFTIME - ACCESSTIME) * GPMC_FCLK period
2. For burst read accesses (where n is the page burst access number):
   A = (CSRDOFFTIME - CSONTIME + (n - 1) * PAGEBURSTACCESSTIME) * (TIMEPARAGRANULARITY + 1) * GPMC_FCLK period
   C = (RDCYCLETIME + (n - 1) * PAGEBURSTACCESSTIME) * (TIMEPARAGRANULARITY + 1) * GPMC_FCLK period
   D = (RDCYCLETIME - (ACCESSTIME + (n - 1) * PAGEBURSTACCESSTIME) * GPMC_FCLK period
   E = (CSRDOFFTIME - (ACCESSTIME + (n - 1) * PAGEBURSTACCESSTIME) * GPMC_FCLK period
3. For burst write accesses (where n is the page burst access number):
   A = (CSWROFFTIME - CSONTIME + (n - 1) * PAGEBURSTACCESSTIME) * (TIMEPARAGRANULARITY + 1) * GPMC_FCLK period
   C = (WRCYCLETIME + (n - 1) * PAGEBURSTACCESSTIME) * (TIMEPARAGRANULARITY + 1) * GPMC_FCLK period
   D = (WRCYCLETIME - (ACCESSTIME + (n - 1) * PAGEBURSTACCESSTIME) * GPMC_FCLK period
   E = (CSWROFFTIME - (ACCESSTIME + (n - 1) * PAGEBURSTACCESSTIME) * GPMC_FCLK period
4. For all accesses:
   For nCS falling edge (CS activated):
   - Case where GPMC_CONFIG1_i[1:0] GPMCFCLKDIVIDER = 0x0:
     F = 0.5 * CSEXTRADELAY * GPMC_FCLK period
   - Case where GPMCFCLKDIVIDER = 0x1:
     F = 0.5 * CSEXTRADELAY * GPMC_FCLK period, when (CLKACTIVATIONTIME and CSONTIME are odd) or (CLKACTIVATIONTIME and CSONTIME are even)
     F = (1 + 0.5 * CSEXTRADELAY) * GPMC_FCLK period otherwise.
   - Case where GPMCFCLKDIVIDER = 0x2:
     F = 0.5 * CSEXTRADELAY * GPMC_FCLK period, when (CSONTIME - CLKACTIVATIONTIME) is a multiple of 3
     F = (1 + 0.5 * CSEXTRADELAY) * GPMC_FCLK period, when (CSONTIME - CLKACTIVATIONTIME - 1) is a multiple of 3
     F = (2 + 0.5 * CSEXTRADELAY) * GPMC_FCLK period, when (CSONTIME - CLKACTIVATIONTIME - 2) is a multiple of 3

   For nCS rising edge (CS desactivated) in reading mode:
   - Case where GPMC_CONFIG1_i[1:0] GPMCFCLKDIVIDER = 0x0:
     F = 0.5 * CSEXTRADELAY * GPMC_FCLK period
   - Case where GPMCFCLKDIVIDER = 0x1:
     F = 0.5 * CSEXTRADELAY * GPMC_FCLK period, when (CLKACTIVATIONTIME and CSRDOFFTIME are odd) or (CLKACTIVATIONTIME and CSRDOFFTIME are even)
     F = (1 + 0.5 * CSEXTRADELAY) * GPMC_FCLK period otherwise.
   - Case where GPMCFCLKDIVIDER = 0x2:
     F = 0.5 * CSEXTRADELAY * GPMC_FCLK period, when (CSRDOFFTIME - CLKACTIVATIONTIME) is a multiple of 3
     F = (1 + 0.5 * CSEXTRADELAY) * GPMC_FCLK period, when (CSRDOFFTIME - CLKACTIVATIONTIME - 1) is a multiple of 3
     F = (2 + 0.5 * CSEXTRADELAY) * GPMC_FCLK period, when (CSRDOFFTIME - CLKACTIVATIONTIME - 2) is a multiple of 3

   For nCS rising edge (CS desactivated) in writing mode:
   - Case where GPMC_CONFIG1_i[1:0] GPMCFCLKDIVIDER = 0x0:
     F = 0.5 * CSEXTRADELAY * GPMC_FCLK period
   - Case where GPMCFCLKDIVIDER = 0x1:
     F = 0.5 * CSEXTRADELAY * GPMC_FCLK period, when (CLKACTIVATIONTIME and CSWROFFTIME are odd) or (CLKACTIVATIONTIME and CSWROFFTIME are even)
     F = (1 + 0.5 * CSEXTRADELAY) * GPMC_FCLK period otherwise.

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- Case where GPMCFCLKDIVIDER = 0x2:
  F = 0.5 * CSEXTRADELAY * GPMC_FCLK period, when (CSWROFFTIME - CLKACTIVATIONTIME) is a multiple of 3
  F = (1 + 0.5 * CSEXTRADELAY) * GPMC_FCLK period, when (CSWROFFTIME - CLKACTIVATIONTIME - 1) is a multiple of 3
  F = (2 + 0.5 * CSEXTRADELAY) * GPMC_FCLK period, when (CSWROFFTIME - CLKACTIVATIONTIME - 2) is a multiple of 3

For nADV falling edge (nADV activated):

- Case where GPMC_CONFIG1_i[1:0] GPMCFCLKDIVIDER = 0x0:
  G = 0.5 * ADVEXTRADELAY * GPMC_FCLK period
- Case where GPMCFCLKDIVIDER = 0x1:
  G = 0.5 * ADVEXTRADELAY * GPMC_FCLK period, when (CLKACTIVATIONTIME and ADVONTIME are odd) or (CLKACTIVATIONTIME and ADVONTIME are even)
  G = (1 + 0.5 * ADVEXTRADELAY) * GPMC_FCLK period otherwise.
- Case where GPMCFCLKDIVIDER = 0x2:
  G = 0.5 * ADVEXTRADELAY * GPMC_FCLK period, when (ADVONTIME - CLKACTIVATIONTIME) is a multiple of 3
  G = (1 + 0.5 * ADVEXTRADELAY) * GPMC_FCLK period, when (ADVONTIME - CLKACTIVATIONTIME - 1) is a multiple of 3
  G = (2 + 0.5 * ADVEXTRADELAY) * GPMC_FCLK period, when (ADVONTIME - CLKACTIVATIONTIME - 2) is a multiple of 3

For nADV rising edge (nADV desactivated) in reading mode:

- Case where GPMC_CONFIG1_i[1:0] GPMCFCLKDIVIDER = 0x0:
  G = 0.5 * ADVEXTRADELAY * GPMC_FCLK period
- Case where GPMCFCLKDIVIDER = 0x1:
  G = 0.5 * ADVEXTRADELAY * GPMC_FCLK period, when (CLKACTIVATIONTIME and ADVRDOFFTIME are odd) or (CLKACTIVATIONTIME and ADVRDOFFTIME are even)
  G = (1 + 0.5 * ADVEXTRADELAY) * GPMC_FCLK period otherwise.
- Case where GPMCFCLKDIVIDER = 0x2:
  G = 0.5 * ADVEXTRADELAY * GPMC_FCLK period, when (ADVRDOFFTIME - CLKACTIVATIONTIME) is a multiple of 3
  G = (1 + 0.5 * ADVEXTRADELAY) * GPMC_FCLK period, when (ADVRDOFFTIME - CLKACTIVATIONTIME - 1) is a multiple of 3
  G = (2 + 0.5 * ADVEXTRADELAY) * GPMC_FCLK period, when (ADVRDOFFTIME - CLKACTIVATIONTIME - 2) is a multiple of 3

For nADV rising edge (nADV desactivated) in writing mode:

- Case where GPMC_CONFIG1_i[1:0] GPMCFCLKDIVIDER = 0x0:
  G = 0.5 * ADVEXTRADELAY * GPMC_FCLK period
- Case where GPMCFCLKDIVIDER = 0x1:
  G = 0.5 * ADVEXTRADELAY * GPMC_FCLK period, when (CLKACTIVATIONTIME and ADVWROFFTIME are odd) or (CLKACTIVATIONTIME and ADVWROFFTIME are even)
  G = (1 + 0.5 * ADVEXTRADELAY) * GPMC_FCLK period otherwise.
- Case where GPMCFCLKDIVIDER = 0x2:
  G = 0.5 * ADVEXTRADELAY * GPMC_FCLK period, when (ADVWROFFTIME - CLKACTIVATIONTIME) is a multiple of 3
  G = (1 + 0.5 * ADVEXTRADELAY) * GPMC_FCLK period, when (ADVWROFFTIME - CLKACTIVATIONTIME - 1) is a multiple of 3
  G = (2 + 0.5 * ADVEXTRADELAY) * GPMC_FCLK period, when (ADVWROFFTIME - CLKACTIVATIONTIME - 2) is a multiple of 3

For nOE falling edge (nOE activated):

- Case where GPMC_CONFIG1_i[1:0] GPMCFCLKDIVIDER = 0x0:
  H = 0.5 * OEEXTRADELAY * GPMC_FCLK period
- Case where GPMCFCLKDIVIDER = 0x1:
  H = 0.5 * OEEXTRADELAY * GPMC_FCLK period, when (CLKACTIVATIONTIME and OEONTIME are odd) or (CLKACTIVATIONTIME and OEONTIME are even)
  H = (1 + 0.5 * OEEXTRADELAY) * GPMC_FCLK period otherwise.

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- Case where GPMCFCLKDIVIDER = 0x2:
  H = 0.5 * OEEXTRADELAY * GPMC_FCLK period, when (OEONTIME - CLKACTIVATIONTIME) is a multiple of 3
  H = (1 + 0.5 * OEEXTRADELAY) * GPMC_FCLK period, when (OEONTIME - CLKACTIVATIONTIME - 1) is a multiple of 3
  H = (2 + 0.5 * OEEXTRADELAY) * GPMC_FCLK period, when (OEONTIME - CLKACTIVATIONTIME - 2) is a multiple of 3

For nOE rising edge (nOE desactivated):

- Case where GPMC_CONFIG1_i[1:0] GPMCFCLKDIVIDER = 0x0:
  H = 0.5 * OEEXTRADELAY * GPMC_FCLK period
- Case where GPMCFCLKDIVIDER = 0x1:
  H = 0.5 * OEEXTRADELAY * GPMC_FCLK period, when (CLKACTIVATIONTIME and OEOFFTIME are odd) or (CLKACTIVATIONTIME and OEOFFTIME are even)
  H = (1 + 0.5 * OEEXTRADELAY) * GPMC_FCLK period otherwise.
- Case where GPMCFCLKDIVIDER = 0x2:
  H = 0.5 * OEEXTRADELAY * GPMC_FCLK period, when (OEOFFTIME - CLKACTIVATIONTIME) is a multiple of 3
  H = (1 + 0.5 * OEEXTRADELAY) * GPMC_FCLK period, when (OEOFFTIME - CLKACTIVATIONTIME - 1) is a multiple of 3
  H = (2 + 0.5 * OEEXTRADELAY) * GPMC_FCLK period, when (OEOFFTIME - CLKACTIVATIONTIME - 2) is a multiple of 3

For nWE falling edge (nWE activated):

- Case where GPMC_CONFIG1_i[1:0] GPMCFCLKDIVIDER = 0x0:
  I = 0.5 * WEEXTRADELAY * GPMC_FCLK period
- Case where GPMCFCLKDIVIDER = 0x1:
  I = 0.5 * WEEXTRADELAY * GPMC_FCLK period, when (CLKACTIVATIONTIME and WEONTIME are odd) or (CLKACTIVATIONTIME and WEONTIME are even)
  I = (1 + 0.5 * WEEXTRADELAY) * GPMC_FCLK period otherwise.
- Case where GPMCFCLKDIVIDER = 0x2:
  I = 0.5 * WEEXTRADELAY * GPMC_FCLK period, when (WEONTIME - CLKACTIVATIONTIME) is a multiple of 3
  I = (1 + 0.5 * WEEXTRADELAY) * GPMC_FCLK period, when (WEONTIME - CLKACTIVATIONTIME - 1) is a multiple of 3
  I = (2 + 0.5 * WEEXTRADELAY) * GPMC_FCLK period, when (WEONTIME - CLKACTIVATIONTIME - 2) is a multiple of 3

For nWE rising edge (nWE desactivated):

- Case where GPMC_CONFIG1_i[1:0] GPMCFCLKDIVIDER = 0x0:
  I = 0.5 * WEEXTRADELAY * GPMC_FCLK period
- Case where GPMCFCLKDIVIDER = 0x1:
  I = 0.5 * WEEXTRADELAY * GPMC_FCLK period, when (CLKACTIVATIONTIME and WEOFFTIME are odd) or (CLKACTIVATIONTIME and WEOFFTIME are even)
  I = (1 + 0.5 * WEEXTRADELAY) * GPMC_FCLK period otherwise.
- Case where GPMCFCLKDIVIDER = 0x2:
  I = 0.5 * WEEXTRADELAY * GPMC_FCLK period, when (WEOFFTIME - CLKACTIVATIONTIME) is a multiple of 3
  I = (1 + 0.5 * WEEXTRADELAY) * GPMC_FCLK period, when (WEOFFTIME - CLKACTIVATIONTIME - 1) is a multiple of 3
  I = (2 + 0.5 * WEEXTRADELAY) * GPMC_FCLK period, when (WEOFFTIME - CLKACTIVATIONTIME - 2) is a multiple of 3

For gpmc_nadv low pulse duration:

- Read operation:
  K = (ADVRDOFFTIME - ADVONTIME) * (TIMEPARAGRANULARITY + 1) * GPMC_FCLK period
- Write operation:
  K = (ADVWROFFTIME - ADVONTIME) * (TIMEPARAGRANULARITY + 1) * GPMC_FCLK period

For gpmc_wait invalid to first data latching gpmc_clk edge:

- L = WAITMONITORINGTIME * (GPMCFCLKDIVIDER + 1) * GPMC_FCLK period + GPMC_CLK

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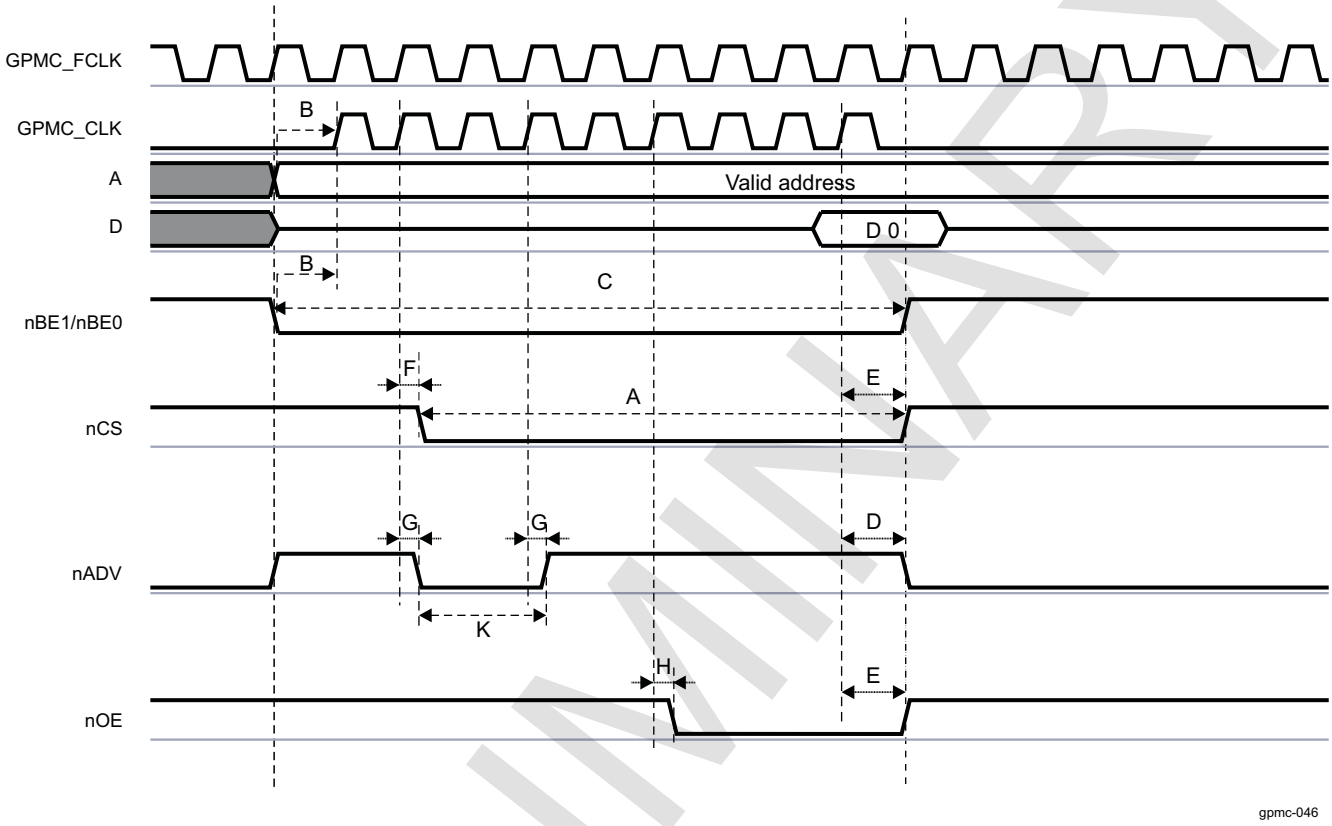
period

Figure 15-94 shows a synchronous NOR single read simplified example where formulas are associated with signal waves.

Figure 15-94. Synchronous NOR Single Read Simplified Example



15.4.5.6.1.3 Asynchronous NOR Flash Timing Parameters Formulas

This section lists all formulas to use in order to calculate asynchronous NOR timing parameters. This is the case when GPMC_CONFIG1_i[11:10] DEVICETYPE = 0x0 and when READTYPE or WRITETYPE are set to asynchronous mode.

Table 15-260. Asynchronous NOR Formulas Description Table

Configuration Parameter	Unit	Description
A	ns	Pulse duration - gpmc_ncs low
B	ns	Delay time - gpmc_ncs valid to gpmc_nadv_ale invalid
C	ns	Delay time - gpmc_ncs valid to gpmc_noe invalid (single read)
D	ns	Pulse duration - address bus valid - 2nd, 3rd and 4th accesses
E	ns	Delay time - gpmc_ncs valid to gpmc_nwe valid
F	ns	Delay time - gpmc_ncs valid to gpmc_nwe invalid
G	ns	Address invalid duration between 2 successive R/W accesses
H	ns	Setup time - read data valid before gpmc_noe high
I	ns	Delay time - gpmc_ncs valid to gpmc_noe invalid (burst read)
J	ns	Delay time - address bus valid to gpmc_ncs valid
		Delay time - data bus valid to gpmc_ncs valid
		Delay time - gpmc_nbe0_cle/gpmc_nbe1 valid to gpmc_ncs valid
K	ns	Delay time - gpmc_ncs valid to gpmc_nadv_ale valid

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Table 15-260. Asynchronous NOR Formulas Description Table (continued)

Configuration Parameter	Unit	Description
L	ns	Delay time - gpmc_ncs valid to gpmc_noe valid
M	ns	Delay time - gpmc_ncs valid to first data latching edge
N	ns	Pulse duration - gpmc_nbe0_cle/gpmc_nbe1 valid time
O	ns	Delay time - gpmc_ncs valid to gpmc_nadv_ale valid

The configuration parameters are calculated through the following formulas. Note that these formulas are not exhaustive.

- gpmc_ncs low pulse:
  For single read: A = (CSRDOFFTIME - CSONTIME) * (TIMEPARAGRANULARITY + 1) * GPMC_FCLK period
  For burst read: A = (CSRDOFFTIME - CSONTIME + (N - 1) * PAGEBURSTACCESSTIME) * (TIMEPARAGRANULARITY + 1) * GPMC_FCLK period, where N = page burst access number
  For single write: A = (CSWROFFTIME - CSONTIME) * (TIMEPARAGRANULARITY + 1) * GPMC_FCLK period
  For burst write: A = (CSWROFFTIME - CSONTIME + (N - 1) * PAGEBURSTACCESSTIME) * (TIMEPARAGRANULARITY + 1) * GPMC_FCLK period, where N = page burst access number
- gpmc_ncs valid to gpmc_nadv_ale invalid delay:
  For reading: B = ((ADVRDOFFTIME - CSONTIME) * (TIMEPARAGRANULARITY + 1) + 0.5 * (ADVEXTRADELAY - CSEXTRADELAY)) * GPMC_FCLK period
  For writing: B = ((ADVWROFFTIME - CSONTIME) * (TIMEPARAGRANULARITY + 1) + 0.5 * (ADVEXTRADELAY - CSEXTRADELAY)) * GPMC_FCLK period
- C = ((OEOFFTIME - CSONTIME) * (TIMEPARAGRANULARITY + 1) + 0.5 * (OEEXTRADELAY - CSEXTRADELAY)) * GPMC_FCLK period
- D = PAGEBURSTACCESSTIME * (TIMEPARAGRANULARITY + 1) * GPMC_FCLK period
- E = ((WEONTIME - CSONTIME) * (TIMEPARAGRANULARITY + 1) + 0.5 * (WEEXTRADELAY - CSEXTRADELAY)) * GPMC_FCLK period
- F = ((WEOFFTIME - CSONTIME) * (TIMEPARAGRANULARITY + 1) + 0.5 * (WEEXTRADELAY - CSEXTRADELAY)) * GPMC_FCLK period
- G = CYCLE2CYCLEDELAY * GPMC_FCLK period
- H = ((OEOFFTIME - ACCESSTIME) * (TIMEPARAGRANULARITY + 1) + 0.5 * OEEXTRADELAY) * GPMC_FCLK period
- I = ((OEOFFTIME + (N - 1) * PAGEBURSTACCESSTIME - CSONTIME) * (TIMEPARAGRANULARITY + 1) + 0.5 * (OEEXTRADELAY - CSEXTRADELAY)) * GPMC_FCLK period, where N = page burst access number
- J = (CSONTIME * (TIMEPARAGRANULARITY + 1) + 0.5 * CSEXTRADELAY) * GPMC_FCLK period
- K = ((ADVONTIME - CSONTIME) * (TIMEPARAGRANULARITY + 1) + 0.5 * (ADVEXTRADELAY - CSEXTRADELAY)) * GPMC_FCLK period
- L = ((OEONTIME - CSONTIME) * (TIMEPARAGRANULARITY + 1) + 0.5 * (OEEXTRADELAY - CSEXTRADELAY)) * GPMC_FCLK period
- M = ((ACCESSTIME - CSONTIME) * (TIMEPARAGRANULARITY + 1) - 0.5 * CSEXTRADELAY) * GPMC_FCLK period
- gpmc_nbe0_cle/gpmc_nbe1 pulse:
  For single read: N = RDCYCLETIME * (TIMEPARAGRANULARITY + 1) * GPMC_FCLK period
  For burst read: N = (RDCYCLETIME + (N - 1) * PAGEBURSTACCESSTIME) * (TIMEPARAGRANULARITY + 1) * GPMC_FCLK period, where N = page burst access number
  For burst write: N = (WRCYCLETIME + (N - 1) * PAGEBURSTACCESSTIME) * (TIMEPARAGRANULARITY + 1) * GPMC_FCLK period, where N = page burst access number
- O = ((WRCYCLETIME + (N - 1) * PAGEBURSTACCESSTIME - CSONTIME) * (TIMEPARAGRANULARITY + 1) + 0.5 * (ADVEXTRADELAY - CSEXTRADELAY)) * GPMC_FCLK period

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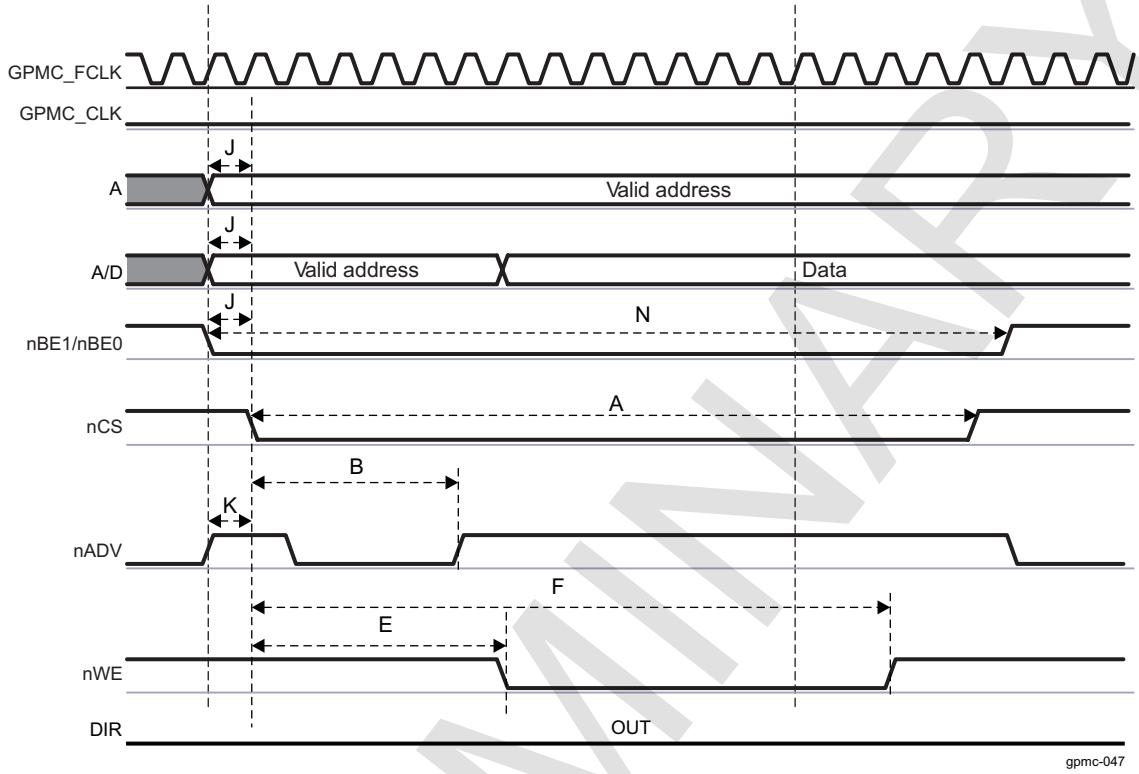
Figure 15-95 shows an asynchronous NOR single write simplified example where formulas are associated with signal waves.

Figure 15-95. Asynchronous NOR Single Write Simplified Example



NOTE: Write multiple access is not supported in asynchronous mode. If WRITEMULTIPLE is enabled with WRITETYPE as asynchronous, the GPMC processes single asynchronous accesses.

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15.4.6 GPMC Use Cases And Tips

15.4.6.1 How to Set GPMC Timing Parameters for Typical Accesses

15.4.6.1.1 External Memory Attached to the GPMC Module

As discussed in the introduction to this chapter, the GPMC module supports the following external memory types:

- Asynchronous or synchronous, 8-bit or 16-bit-width memory or device
- 16-bit address/data-multiplexed or not multiplexed NOR flash device
- 8- or 16-bit NAND flash device

The following examples show how to calculate GPMC timing parameters by showing a typical parameter setup for the access to be performed.

The example is based on a 512-Mb multiplexed NOR flash memory with the following characteristics:

- Type: NOR flash (address/data-multiplexed mode)
- Size: 512M bits
- Data Bus: 16 bits wide
- Speed: 104 MHz clock frequency
- Read access time: 80 ns

15.4.6.1.2 Typical GPMC Setup

Table 15-261 lists some of the I/Os of the GPMC module.

Table 15-261. GPMC Signals

Signal Name	I/0	Description
GPMC_FCLK	Internal	Functional and interface clock. Acts as the time reference.
gpmc_clk	O	External clock provided to the external device for synchronous operations
gpmc_a[25:16]	O	Address
gpmc_ad[15: 0]	I/O	Data-multiplexed with addresses A[16:1] on memory side
gpmc_ncsx	O	Chip-select (where x = 0, or 1)
gpmc_nadv_ale	O	Address valid enable
gpmc_noe_nre	O	Output enable (read access only)
gpmc_nwe	O	Write enable (write access only)
gpmc_wait[2:0]	I	Ready signal from memory device. Indicates when valid burst data is ready to be read

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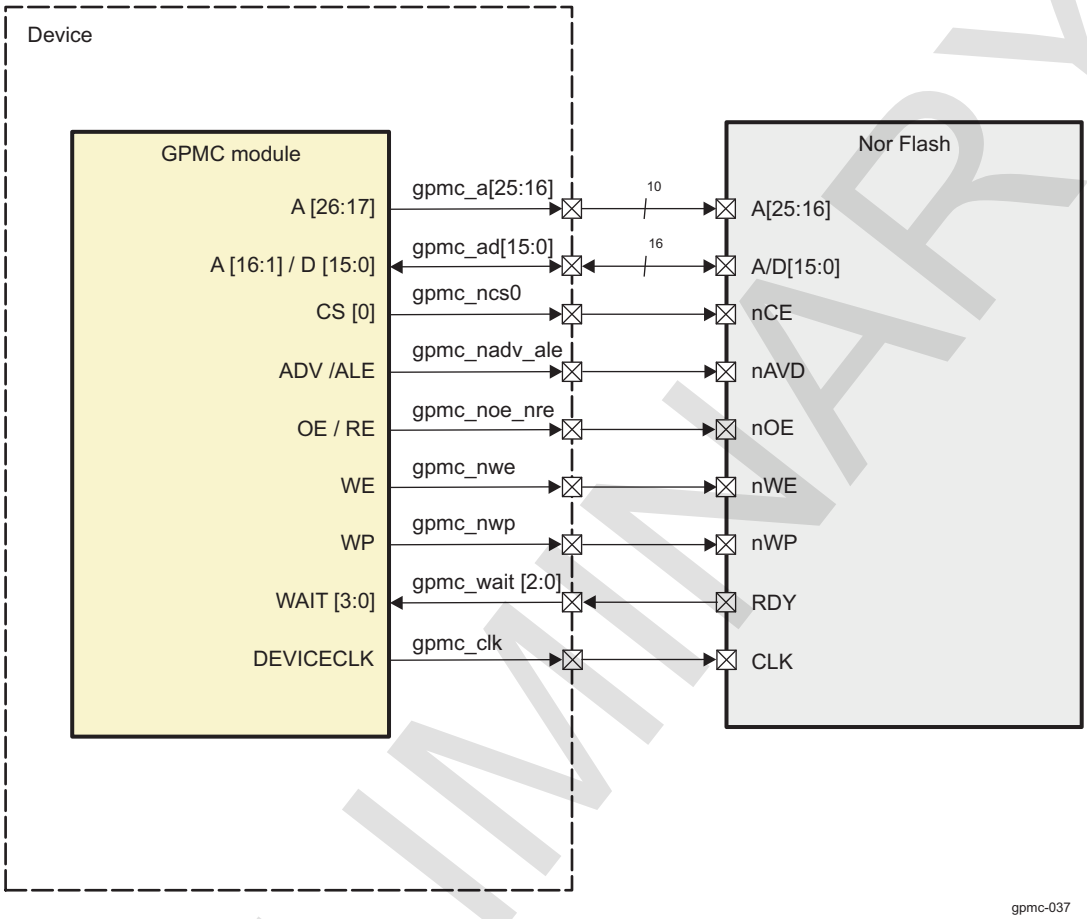
Figure 15-96 shows the typical connection between the GPMC module and an attached NOR Flash memory.

Figure 15-96. GPMC Connection to an External NOR Flash Memory



The following sections demonstrate how to calculate GPMC parameters for three access types:

- Synchronous burst read
- Asynchronous read
- Asynchronous single write

15.4.6.1.2.1 GPMC Configuration for Synchronous Burst Read Access

The clock runs at 104 MHz (f = 104 MHz; T = 9, 615 ns).

Table 15-262 shows the timing parameters (on the memory side) that determine the parameters on the GPMC side.

Table 15-263 shows how to calculate timings for the GPMC using the memory parameters.

Figure 15-97 shows the synchronous burst read access.

Table 15-262. Useful Timing Parameters on the Memory Side

AC Read Characteristics on the Memory Side	Description	Duration (ns)
tCES	nCS setup time to clock	0
tACS	Address setup time to clock	3
tIACC	Synchronous access time	80

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Table 15-262. Useful Timing Parameters on the Memory Side (continued)

AC Read Characteristics on the Memory Side	Description	Duration (ns)
tBACC	Burst access time valid clock to output delay	5,2
tCEZ	Chip-select to High-Z	7
tOEZ	Output enable to High-Z	7
tAVC	nADV setup time	6
tAVD	nAVD pulse	6
tACH	Address hold time from clock	3

The following terms, which describe the timing interface between the controller and its attached device, are used to calculate the timing parameters on the GPMC side:

- Read Access time (GPMC side): Time required to activate the clock + read access time requested on the memory side + data setup time required for optimal capture of a burst of data
- Data setup time (GPMC side): Ensures a good capture of a burst of data (as opposed to taking a burst of data out). One word of data is processed in one clock cycle (T = 9,615 ns). The read access time between 2 bursts of data is tBACC = 5,2 ns. Therefore, data setup time is a clock period - tBACC = 4,415 ns of data setup.
- Access completion (GPMC side): (Different from page burst access time) Time required between the last burst access and access completion: nCS/nOE hold time (nCS and nOE must be released at the end of an access. These signals are held to allow the access to complete).
- Read cycle time (GPMC side): Read Access time + access completion
- Write cycle time for burst access: Not supported for NOR flash memory

Table 15-263. Calculating GPMC Timing Parameters

Parameter Name on GPMC Side	Formula	Duration (ns)	Number of Clock Cycles (F = 104 MHz)	GPMC Register Configurations
GPMC FCLK Divider	-	-	-	GPMCFCLKDIVIDER = 0x0
ClkActivation Time	min (tCES, tACS)	3	1	CLKACTIVATIONTIME = 0x1
RdAccessTime	roundmax (ClkActivationTime + tIACC + DataSetupTime)	94,03: (9,615 + 80 + 4,415)	10 : roundmax (94,03 / 9,615)	ACCESSTIME = 0x0A
PageBurst AccessTime	roundmax (tBACC)	roundmax (5,2)	1	PAGEBURSTACCESSTIME = 0x1
RdCycleTime	AccessTime + max (tCEZ, tOEZ)	101, 03: (94, 03 + 7)	11	RDCYCLETIME = 0x0B
CsOnTime	tCES	0	0	CSONTIME = 0x0
CsReadOffTime	RdCycleTime	-	11	CSRDOFFTIME = 0x0B
AdvOnTime	tAVC (1)	0	0	ADVONTIME = 0x0
AdvRdOffTime	tAVD + tAVC (2)	12	2	ADVRDOFFTIME = 0x02
OeOnTime (3)	(ClkActivationTime + tACH) OeOnTime (ClkActivationTime + tIACC)	-	3 for instance.	OEONTIME = 0x3
OeOffTime	RdCycleTime	-	11	OEOFFTIME = 0x0B

(1) The external clock provided to the NOR flash is not yet available.
(2) AdvRdOffTime - AdvOnTime = tAVD; thus, AdvRdOffTime = tAVD + AdvOnTime = tAVD + tAVC.
(3) OeOnTime must guarantee that addresses are available. It must not exceed the availability of the first burst of data.

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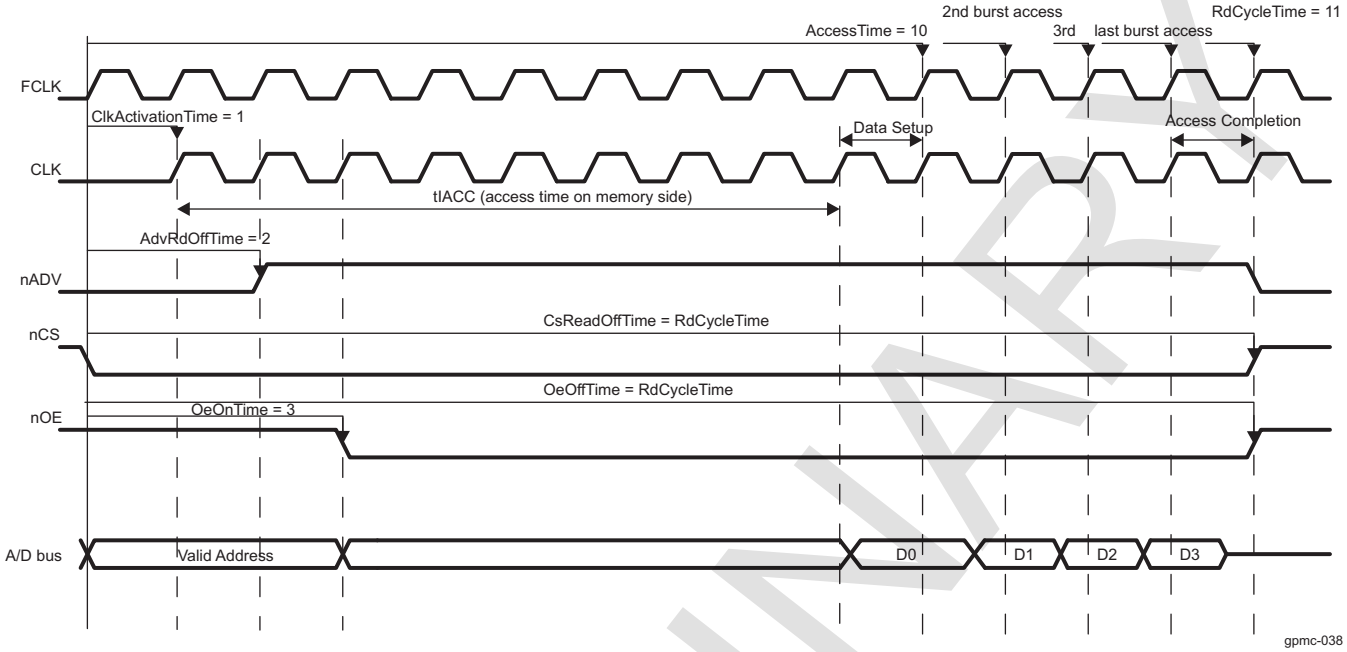
Figure 15-97. Synchronous Burst Read Access (Timing Parameters in Clock Cycles)



15.4.6.1.2.2 GPMC Configuration for Asynchronous Read Access

The clock runs at 104 MHz (f = 104 MHz; T = 9, 615 ns).

Table 15-264 shows the timing parameters (on the memory side) that determine the parameters on the GPMC side.

Table 15-265 shows how to calculate timings for the GPMC using the memory parameters.

Figure 15-98 shows the asynchronous read access.

Table 15-264. AC Characteristics for Asynchronous Read Access

AC Read Characteristics on the Memory Side	Description	Duration (ns)
tCE	Read Access time from nCS low	80
tAAVDS	Address setup time to rising edge of nADV	3
tAVDP	nADV low time	6
tCAS	nCS setup time to nADV	0
tOE	Output enable to output valid	6
tOEZ	Output enable to High-Z	7

Use the following formula to calculate the RdCycleTime parameter for this typical access:

RdCycleTime = RdAccessTime + AccessCompletion = RdAccessTime + 1 clock cycle + tOEZ:

- First, on the memory side, the external memory makes the data available to the output bus. This is the memory-side read access time defined in Table 15-264: the number of clock cycles between the address capture (nADV rising edge) and the data valid on the output bus.

  The GPMC requires some hold time to allow the data to be captured correctly and the access to be finished.
- To read the data correctly, the GPMC must be configure to meet the data setup time requirement of the memory; the GPMC module captures the data on the next rising edge. This is access time on the GPMC side.
- There must also be a data hold time for correctly reading the data (checking that there is no nOE/nCS

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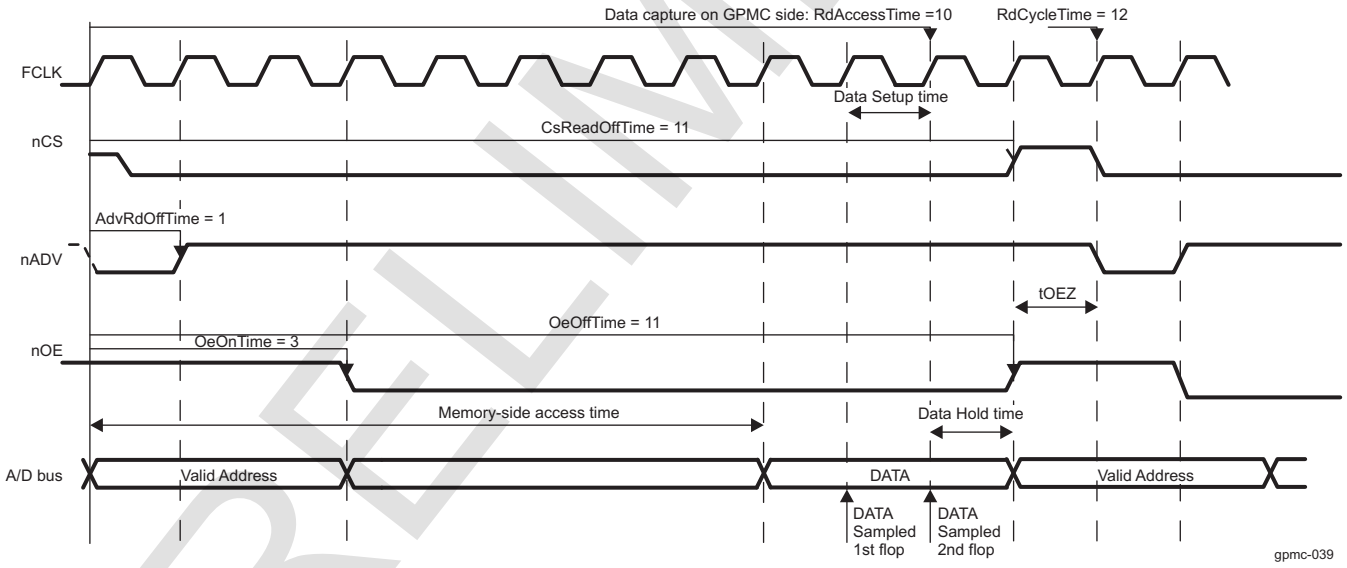
deassertion while reading the data). This data hold time is 1 clock cycle (that is, AccessTime + 1).

- To complete the access, nOE/nCS signals are driven to High-Z. AccessTime + 1 + tOEZ is the read cycle time.
- Addresses can now be relatched and a new read cycle begun.

Table 15-265. GPMC Timing Parameters for Asynchronous Read Access

Parameter Name on GPMC side	Formula	Duration (ns)	Number of Clock Cycles (F = 104 MHz)	GPMC Register Configurations
ClkActivationTime	n/a (asynchronous mode)			
AccessTime	round max (tCE)	80	10	ACCESSTIME = 0x0A
PageBurstAccess Time	n/a (single access)			
RdCycleTime	AccessTime + 1cycle + tOEZ	96, 615	12	RDCYCLETIME = 0x0C
CsOnTime	tCAS	0	0	CSONTIME = 0x0
CsReadOffTime	AccessTime + 1 cycle	89, 615	11	CSRDOFFTIME = 0x0B
AdvOnTime	tAAVDS	3	1	ADVONTIME = 0X1
AdvRdOffTime	tAAVDS + tAVDP	9	1	ADVRDOFFTIME = 0x01
OeOnTime	OeOnTime = AdvRdOffTime (multiplexed mode)	-	3 for instance	OEONTIME = 0x3
OeOffTime	AccessTime + 1cycle	89, 615	11	OEOFFTIME = 0x0B

Figure 15-98. Asynchronous Single Read Access (Timing Parameters in Clock Cycles)



15.4.6.1.2.3 GPMC Configuration for Asynchronous Single Write Access

The clock runs at 104 MHz: (f = 104 MHz; T = 9, 615 ns).

Table 15-267 shows how to calculate timings for the GPMC using the memory parameters.

Table 15-266 shows the timing parameters (on the memory side) that determine the parameters on the GPMC side.

Figure 15-99 shows the synchronous burst write access.

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Table 15-266. AC Characteristics for Asynchronous Single Write (Memory Side)

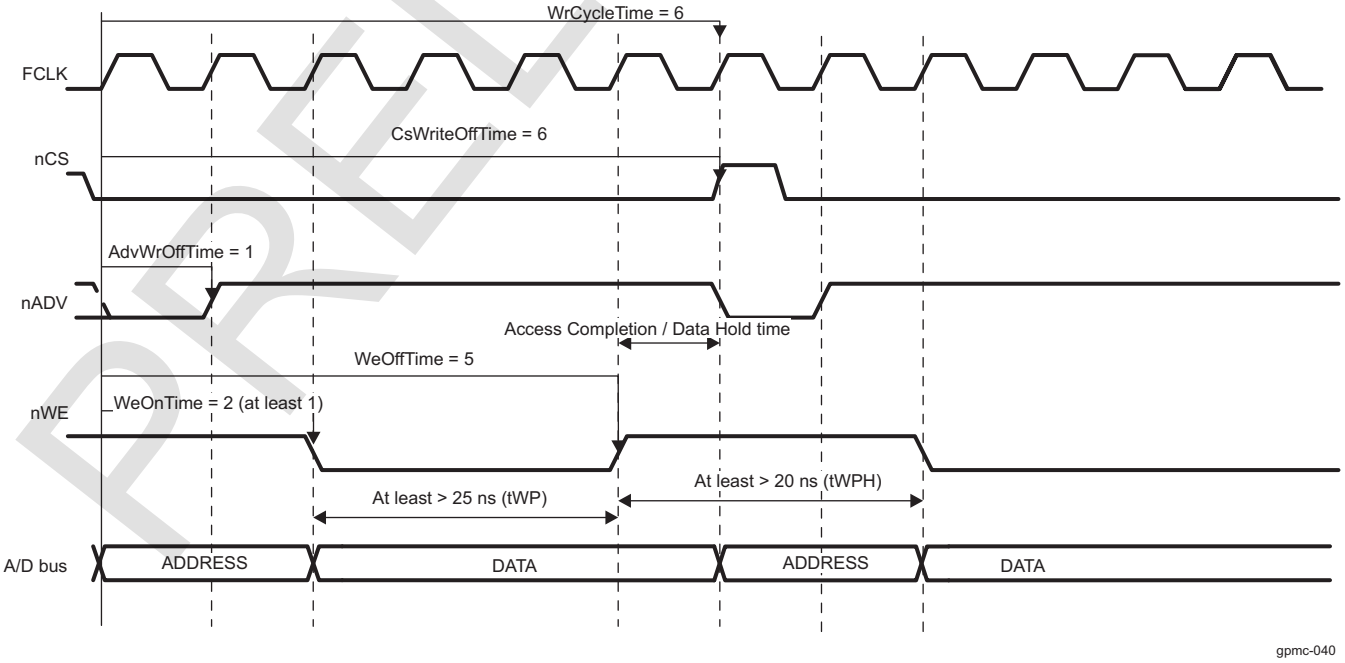
AC Characteristics on the Memory Side	Description	Duration (ns)
tWC	Write cycle time	60
tAVDP	nADV low time	6
tWP	Write pulse width	25
tWPH	Write pulse width high	20
tCS	nCS setup time to nWE	3
tCAS	nCS setup time to nADV	0
tAVSC	nADV setup time	3

For asynchronous single write access, write cycle time is WrCycleTime = WeOffTime + AccessCompletion = WeOffTime + 1. For the AccesCompletion, the GPMC requires 1 cycle of data hold time (nCS deassertion).

Table 15-267. GPMC Timing parameters for Asynchronous Single Write

Parameter Name on GPMC side	Formula	Duration (ns)	Number of Clock Cycles (F = 104 MHz)	GPMC Registers Configuration
ClkActivationTime	n/a (asynchronous mode)			
AccessTime	Applicable only to WAITMONITORING (the value is the same as for read access)			
PageBurstAccessTime	n/a (single access)			
WrCycleTime	WeOffTime + AccessCompletion	57, 615	6	WRCYCLETIME = 0x06
CsOnTime	tCAS	0	0	CSONTIME = 0x0
CsWrOffTime	WeOffTime + 1	57, 615	6	CSWROFFTIME = 0x06
AdvOnTime	tAVSC	3	1	ADVONTIME = 0x1
AdvWrOffTime	tAVSC + tAVDP	9	1	ADVWROFFTIME = 0x01
WeOnTime	tCS	3	1	WEONTIME = 0x1
WeOffTime	tCS + tWP + tWPH	48	5	WEOFFTIME = 0x05

Figure 15-99. Asynchronous Single Write Access (Timing Parameters in Clock Cycles)



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15.4.6.2 How to choose a suitable memory to use with the GPMC

This section is intended to help the user select a suitable memory device to interface with the GPMC controller.

15.4.6.2.1 Supported Memories or Devices

NAND flash and NOR flash architectures are the two flash technologies. The GPMC supports various types of external memory or device, basically any one that supports NAND or NOR protocols:

- 8- and 16-bit width asynchronous or synchronous memory or device (8-bit: non burst device only)
- 16-bit address and data multiplexed NOR flash devices (pSRAM, OneNAND™, ...)
- 8- and 16-bit NAND flash device

NOTE: Non-multiplexed NOR flash devices are supported by the GPMC but their usage is highly limited. As only ten address pins are available on the GPMC interface, the maximum device size supported is 2KB.

15.4.6.2.1.1 Memory Pin Multiplexing

This section highlights the interfacing differences of the GPMC supported memories.

Table 15-268. Supported memories interfaces

Function	16-bit Address/Data muxed pSRAM or NOR Flash [1]	OneNAND	16-bit NAND	8-bit NAND
gpmc_a[25]	A26			
gpmc_a[24]	A25			
gpmc_a[23]	A24			
gpmc_a[22]	A23			
gpmc_a[21]	A22			
gpmc_a[20]	A21			
gpmc_a[19]	A20			
gpmc_a[18]	A19			
gpmc_a[17]	A18			
gpmc_a[16]	A17			
gpmc_ad[15]	D15 or A16		IO15	
gpmc_ad[14]	D14 or A15		IO14	
gpmc_ad[13]	D13 or A14		IO13	
gpmc_ad[12]	D12 or A13		IO12	
gpmc_ad[11]	D11 or A12		IO11	
gpmc_ad[10]	D10 or A11		IO10	
gpmc_ad[9]	D9 or A10		IO9	
gpmc_ad[8]	D8 or A9		IO8	
gpmc_ad[7]	D7 or A8		IO7	
gpmc_ad[6]	D6 or A7		IO6	
gpmc_ad[5]	D5 or A6		IO5	
gpmc_ad[4]	D4 or A5		IO4	
gpmc_ad[3]	D3 or A4		IO3	
gpmc_ad[2]	D2 or A3		IO2	
gpmc_ad[1]	D1 or A2		IO1	
gpmc_ad[0]	D0 or A1		IO0	
gpmc_clk	CLK			

[1] Addresses seen from the device side. When interfacing to the external IC, A1 is connected to the memory A0, A2 to the memory A1, and so on...

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Table 15-268. Supported memories interfaces (continued)

Function	16-bit Address/Data muxed pSRAM or NOR Flash [1]	OneNAND	16-bit NAND	8-bit NAND
gpmc_ncs0	nCS0 (Chip Select)		nCE0 (Chip Enable)	
gpmc_ncs1	nCS1		nCE1	
gpmc_ncs2	nCS2		nCE2	
gpmc_ncs3	nCS3		nCE3	
gpmc_ncs4	nCS4		nCE4	
gpmc_ncs5	nCS5		nCE5	
gpmc_ncs6	nCS6		nCE6	
gpmc_ncs7	nCS7		nCE7	
gpmc_nadv_ale	nADV (Address Valid)		ALE (Address Latch Enable)	
gpmc_noe	nOE (Output Enable)		nRE (Read Enable)	
gpmc_nwe	nWE (Write Enable)		nWE (Write Enable)	
gpmc_nbe0_cle	nBE0 (Byte Enable)		CLE (Command Latch Enable)	
gpmc_nbe1	nBE1			
gpmc_nwp	nWP (Write Protect)		nWP (Write Protect)	
gpmc_wait0	WAIT0		R/nB0 (Ready/Busy)	
gpmc_wait1	WAIT1		R/nB1	
gpmc_wait2	WAIT2		R/nB2	

15.4.6.2.1.2 NAND Interface Protocol

NAND flash architecture, introduced in 1989, is a flash technology. NAND is a page-oriented memory device, that is, read and write accesses are done by pages. NAND achieves great density by sharing common areas of the storage transistor, which creates strings of serially connected transistors (in NOR devices, each transistor stands alone). Thanks to its high density NAND is best suited to devices requiring high capacity data storage, such as pictures, music, or data files. NAND non-volatility, makes of it a good storage solution for many applications where mobility, low power, and speed are key factors. Low pin count and simple interface are other advantages of NAND.

Table 15-269 summarizes the NAND interface signals level applied to external device or memories.

Table 15-269. NAND Interface Bus Operations Summary

Bus operation	CLE	ALE	nCE	nWE [1]	nRE [1]	nWP
Read (cmd input)	H	L	L	RE	H	x
Read (add input)	L	H	L	RE	H	x
Write (cmd input)	H	L	L	RE	H	H
Write (add input)	L	H	L	RE	H	H
Data input	L	L	L	RE	H	H
Data output	L	L	L	H	FE	x
Busy (during read)	x	x	H [2]	H [2]	H [2]	x
Busy (during program)	x	x	x	x	x	H
Busy (during erase)	x	x	x	x	x	H
Write protect	x	x	x	x	x	L
Stand-by	x	x	H	x	x	H/L [3]

(1) RE stands for rising edge, FE stands for falling edge
(2) Can be either nCE high, or WE and nRE high.
(3) nWP should be biased to CMOS high or CMOS low for standby

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15.4.6.2.1.3 NOR Interface Protocol

NOR flash architecture, introduced in 1988, is a flash technology. Unlike NAND which is a sequential access device, NOR is directly addressable, that is, is designed to be a random access device. NOR is best suited to devices used to store and run code or firmware, usually in small capacities. While NOR has fast read capabilities it has slow write and erase functions compared to NAND architecture.

Table 15-270 summarizes the NOR interface signals level applied to external device or memories.

Table 15-270. NOR Interface Bus Operations Summary

Bus operation	CLK	nADV	nCS	nOE	nWE	WAIT	DQ[15:0]
Read (asynchronous)	x	L	L	L	H	Asserted	Output
Read (synchronous)	Running	L	L	L	H	Driven	Output
Read (burst suspend)	Halted	x	L	H	H	Active	Output
Write	x	L	L	H	L	Asserted	Input
Output disable	x	x	L	H	H	Asserted	High-Z
Standby	x	x	H	x	x	High-Z	High-Z

15.4.6.2.1.4 Other Technologies

Other supported device type interact with the GPMC through the NOR interface protocol.

OneNAND™ is a high density and low-power memory device. OneNAND™ is based on single- or multi-level-cell NAND core with SRAM and logic, and interfaces as a synchronous NOR Flash, plus has synchronous write capability. It reads faster than conventional NAND and write faster than conventionnal NOR flash. Hence, it is appropriate for both mass storage and code storage.

pSRAM stands for pseudo-static random access memory. pSRAM is a low-power memory device for mobile applications. pSRAM is based on the DRAM cell with internal refresh and address control features, and interfaces as a synchronous NOR Flash, plus has synchronous write capability.

15.4.6.2.1.5 Supported Protocols

The GPMC supports the following interface protocols when communicating with external memory or external devices:

- Asynchronous read/write access
- Asynchronous read page access (4-8-16 Word16)
- Synchronous read/write access
- Synchronous read burst access without wrap capability (4-8-16 Word16)
- Synchronous read burst access with wrap capability (4-8-16 Word16)

15.4.6.2.2 GPMC Features and Settings

This section lists GPMC features and settings:

- Supported device type: up to four NAND or NOR protocol external memories or devices
- Operating Voltage: 1.8V;
- Maximum GPMC addressing capability: 1 GByte divided into eight chip-selects
- Maximum supported memory size: 256 MBytes (must be a power-of-2)
- Minimum supported memory size: 16 MBytes (must be a power-of-2). Aliasing occurs when addressing smaller memories.
- Data path to external memory or device: 8- and 16-bit wide
- Burst and page access: burst of 4-8-16 Word16
- Supports bus keeping
- Supports bus turn around

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15.4.7 GPMC Register Manual

This section provides information about the GPMC instance in this product. Table 15-272 provides a summary of the GPMC registers. The remaining parts of this section describe the registers within the module instance.

15.4.7.1 GPMC Register Summary

Table 15-271. GPMC Instance Summary

Module Name	Base Address	Size
GPMC	0x5000 0000	32 Mbytes

Table 15-272. GPMC Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	GPMC L3 Physical Address
GPMC_REVISION	R	32	0x0000 0000	0x5000 0000
GPMC_SYSCONFIG	RW	32	0x0000 0010	0x5000 0010
GPMC_SYSSTATUS	R	32	0x0000 0014	0x5000 0014
GPMC_IRQSTATUS	RW	32	0x0000 0018	0x5000 0018
GPMC_IRQENABLE	RW	32	0x0000 001C	0x5000 001C
GPMC_TIMEOUT_CONTROL	RW	32	0x0000 0040	0x5000 0040
GPMC_ERR_ADDRESS	RW	32	0x0000 0044	0x5000 0044
GPMC_ERR_TYPE	RW	32	0x0000 0048	0x5000 0048
GPMC_CONFIG	RW	32	0x0000 0050	0x5000 0050
GPMC_STATUS	RW	32	0x0000 0054	0x5000 0054
GPMC_CONFIG1_i (1)	RW	32	0x0000 0060 + (0x0000 0030 * i)	0x5000 0060 + (0x0000 0030 * i)
GPMC_CONFIG2_i (1)	RW	32	0x0000 0064 + (0x0000 0030 * i)	0x5000 0064 + (0x0000 0030 * i)
GPMC_CONFIG3_i (1)	RW	32	0x0000 0068 + (0x0000 0030 * i)	0x5000 0068 + (0x0000 0030 * i)
GPMC_CONFIG4_i (1)	RW	32	0x0000 006C + (0x0000 0030 * i)	0x5000 006C + (0x0000 0030 * i)
GPMC_CONFIG5_i (1)	RW	32	0x0000 0070 + (0x0000 0030 * i)	0x5000 0070 + (0x0000 0030 * i)
GPMC_CONFIG6_i (1)	RW	32	0x0000 0074 + (0x0000 0030 * i)	0x5000 0074 + (0x0000 0030 * i)
GPMC_CONFIG7_i (1)	RW	32	0x0000 0078 + (0x0000 0030 * i)	0x5000 0078 + (0x0000 0030 * i)
GPMC_NAND_COMMAND_i (1)	W	32	0x0000 007C + (0x0000 0030 * i)	0x5000 007C + (0x0000 0030 * i)
GPMC_NAND_ADDRESS_i (1)	W	32	0x0000 0080 + (0x0000 0030 * i)	0x5000 0080 + (0x0000 0030 * i)
GPMC_NAND_DATA_i (1)	RW	32	0x0000 0084 + (0x0000 0030 * i)	0x5000 0084 + (0x0000 0030 * i)
GPMC_PREFETCH_CONFIG1	RW	32	0x0000 01E0	0x5000 01E0
GPMC_PREFETCH_CONFIG2	RW	32	0x0000 01E4	0x5000 01E4
GPMC_PREFETCH_CONTROL	RW	32	0x0000 01EC	0x5000 01EC
GPMC_PREFETCH_STATUS	RW	32	0x0000 01F0	0x5000 01F0
GPMC_ECC_CONFIG	RW	32	0x0000 01F4	0x5000 01F4
GPMC_ECC_CONTROL	RW	32	0x0000 01F8	0x5000 01F8
GPMC_ECC_SIZE_CONFIG	RW	32	0x0000 01FC	0x5000 01FC
GPMC_ECCj_RESULT (2)	RW	32	0x0000 0200 + (0x0000 0004 * j)	0x5000 0200 + (0x0000 0004 * j)
GPMC_BCH_RESULT0_i (1)	RW	32	0x0000 0240 + (0x0000 0010 * i)	0x5000 0240 + (0x0000 0010 * i)
GPMC_BCH_RESULT1_i (1)	RW	32	0x0000 0244 + (0x0000 0010 * i)	0x5000 0244 + (0x0000 0010 * i)
GPMC_BCH_RESULT2_i (1)	RW	32	0x0000 0248 + (0x0000 0010 * i)	0x5000 0248 + (0x0000 0010 * i)
GPMC_BCH_RESULT3_i (1)	RW	32	0x0000 024C + (0x0000 0010 * i)	0x5000 024C + (0x0000 0010 * i)
GPMC_BCH_RESULT4_i (1)	RW	32	0x0000 0300 + (0x0000 0010 * i)	0x5000 0300 + (0x0000 0010 * i)
GPMC_BCH_RESULT5_i (1)	RW	32	0x0000 0304 + (0x0000 0010 * i)	0x5000 0304 + (0x0000 0010 * i)
GPMC_BCH_RESULT6_i (1)	RW	32	0x0000 0308 + (0x0000 0010 * i)	0x5000 0308 + (0x0000 0010 * i)
GPMC_BCH_SWDATA	RW	32	0x0000 02D0	0x5000 02D0

(1) i = 0 to 7 for GPMC
(2) j = 0 to 8 for GPMC

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15.4.7.2 GPMC Register Descriptions

NOTE: All GPMC registers are aligned to 32-bit address boundaries. All register file accesses, except to GPMC_NAND_DATA_i register, are little endian. If the GPMC_NAND_DATA_i register location is accessed, the endianness is access-dependent.

In the whole section i corresponds to the chip-select number, i = 0 to 7.

Table 15-273. GPMC_REVISION

Address Offset	0x0000 0000		
Physical Address	0x5000 0000	**Instance**	GPMC
Description	This register contains the IP revision code.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP revision	R	TI internal data

Table 15-274. Register Call Summary for Register GPMC_REVISION

General-Purpose Memory Controller
- GPMC Register Summary: [0]

Table 15-275. GPMC_SYSCONFIG

Address Offset	0x0000 0010		
Physical Address	0x5000 0010	**Instance**	GPMC
Description	This register controls the various parameters of the Interconnect.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																											SIDLEMODE		RESERVED	SOFTRESET	AUTOIDLE

Bits	Field Name	Description	Type	Reset
31:5	RESERVED	Write 0s for future compatibility. Reads return 0s.	RW	0x0000000
4:3	SIDLEMODE	0x0: Force-idle. An idle request is acknowledged unconditionally 0x1: No-idle. An idle request is never acknowledged 0x2: Smart-idle. Acknowledgment to an idle request is given based on the internal activity of the module 0x3: Do not use	RW	0x0
2	RESERVED	Write 0 for future compatibility Reads returns 0	RW	0x0
1	SOFTRESET	Software reset. Set this bit to 1 triggers a module reset. This bit is automatically reset by hardware. During reads, it always returns 0. 0x0: Normal mode 0x1: The module is reset	RW	0x0

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Bits	Field Name	Description	Type	Reset
0	AUTOIDLE	Internal Interface clock gating strategy 0x0: Interface clock is free-running 0x1: Automatic Interface clock gating strategy is applied, based on the Interconnect activity	RW	0x0

Table 15-276. Register Call Summary for Register GPMC_SYSCONFIG

General-Purpose Memory Controller
- GPMC Software Reset: [0]
- GPMC Power Management: [1] [2]
- GPMC Initialization: [3]
- GPMC Register Summary: [4]

Table 15-277. GPMC_SYSSTATUS

Address Offset	0x0000 0014		
Physical Address	0x5000 0014	**Instance**	GPMC
Description	This register provides status information about the module, excluding the interrupt status information		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RESERVED							RESETDONE

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Reads returns 0	R	0x000000
7:1	RESERVED	Reads returns 0 (reserved for Interconnect-socket status information)	R	0x00
0	RESETDONE	Internal reset monitoring 0x0: Internal module reset in ongoing 0x1: Reset completed	R	0x-

Table 15-278. Register Call Summary for Register GPMC_SYSSTATUS

General-Purpose Memory Controller
- GPMC Software Reset: [0]
- GPMC Initialization: [1]
- GPMC Register Summary: [2]

Table 15-279. GPMC_IRQSTATUS

Address Offset	0x0000 0018		
Physical Address	0x5000 0018	**Instance**	GPMC
Description	This interrupt status register regroups all the status of the module internal events that can generate an interrupt.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																					WAIT2EDGEDETECTIONSTATUS	WAIT1EDGEDETECTIONSTATUS	WAIT0EDGEDETECTIONSTATUS	RESERVED						TERMINALCOUNTSTATUS	FIFOEVENTSTATUS

Bits	Field Name	Description	Type	Reset
31:11	RESERVED	Write 0s for future compatibility. Read returns 0s.	RW	0x000000
10	WAIT2EDGEDETECTIONSTATUS	Status of the Wait2 Edge Detection interrupt Read 0x0: A transition on WAIT2 input pin has not been detected Write 0x0: WAIT2EDGEDETECTIONSTATUS bit unchanged Read 0x1: A transition on WAIT2 input pin has been detected Write 0x1: WAIT2EDGEDETECTIONSTATUS bit is reset	RW	0x0
9	WAIT1EDGEDETECTIONSTATUS	Status of the Wait1 Edge Detection interrupt Read 0x0: A transition on WAIT1 input pin has not been detected Write 0x0: WAIT1EDGEDETECTIONSTATUS bit unchanged Read 0x1: A transition on WAIT1 input pin has been detected Write 0x1: WAIT1EDGEDETECTIONSTATUS bit is reset	RW	0x0
8	WAIT0EDGEDETECTIONSTATUS	Status of the Wait0 Edge Detection interrupt Read 0x0: A transition on WAIT0 input pin has not been detected Write 0x0: WAIT0EDGEDETECTIONSTATUS bit unchanged Read 0x1: A transition on WAIT0 input pin has been detected Write 0x1: WAIT0EDGEDETECTIONSTATUS bit is reset	RW	0x0
7:2	RESERVED	Write 0s for future compatibility. Read returns 0s.	RW	0x00
1	TERMINALCOUNTSTATUS	Status of the TerminalCountEvent interrupt Read 0x0: Indicates that CountValue is greater than 0 Write 0x0: TERMINALCOUNTSTATUS bit unchanged Read 0x1: Indicates that CountValue is equal to 0 Write 0x1: TERMINALCOUNTSTATUS bit is reset	RW	0x0
0	FIFOEVENTSTATUS	Status of the FIFOEvent interrupt Read 0x0: Indicates than less than GPMC_PREFETCH_STATUS[16] FIFOTHRESHOLDSTATUS bytes are available in prefetch mode and less than FIFOTHRESHOLD bytes free places are available in write-posting mode. Write 0x0: FIFOEVENTSTATUS bit unchanged Read 0x1: Indicates than at least GPMC_PREFETCH_STATUS[16] FIFOTHRESHOLDSTATUS bytes are available in prefetch mode and at least FIFOTHRESHOLD bytes free places are available in write-posting mode. Write 0x1: FIFOEVENTSTATUS bit is reset	RW	0x0

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Table 15-280. Register Call Summary for Register GPMC_IRQSTATUS

General-Purpose Memory Controller

- GPMC Interrupt Requests: [0] [1] [2] [3] [4]
- NAND Device-Ready Pin: [5] [6] [7]
- Prefetch and Write-Posting Engine: [8] [9] [10] [11]
- GPMC Register Summary: [12]

Table 15-281. GPMC_IRQENABLE

Address Offset	0x0000 001C		
Physical Address	0x5000 001C	**Instance**	GPMC
Description	The interrupt enable register allows to mask/unmask the module internal sources of interrupt, on a event-by-event basis.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																					WAIT2EDGEDETECTIONENABLE	WAIT1EDGEDETECTIONENABLE	WAIT0EDGEDETECTIONENABLE	RESERVED						TERMINALCOUNTEVENTENABLE	FIFOEVENTENABLE

Bits	Field Name	Description	Type	Reset
31:11	RESERVED	Write 0s for future compatibility. Read returns 0s.	RW	0x000000
10	WAIT2EDGEDETECTION ENABLE	Enables the Wait2 Edge Detection interrupt 0x0: Wait2EdgeDetection interrupt is masked 0x1: Wait2EdgeDetection event generates an interrupt if occurs	RW	0
9	WAIT1EDGEDETECTION ENABLE	Enables the Wait1 Edge Detection interrupt 0x0: Wait1EdgeDetection interrupt is masked 0x1: Wait1EdgeDetection event generates an interrupt if occurs	RW	0x0
8	WAIT0EDGEDETECTION ENABLE	Enables the Wait0 Edge Detection interrupt 0x0: Wait0EdgeDetection interrupt is masked 0x1: Wait0EdgeDetection event generates an interrupt if occurs	RW	0x0
7:2	RESERVED	Write 0s for future compatibility. Read returns 0s.	RW	0x00
1	TERMINALCOUNTEVENT ENABLE	Enables TerminalCountEvent interrupt issuing in prefetch or write-posting mode 0x0: TerminalCountEvent interrupt is masked 0x1: TerminalCountEvent interrupt is not masked	RW	0x0
0	FIFOEVENTENABLE	Enables the FIFOEvent interrupt 0x0: FIFOEvent interrupt is masked 0x1: FIFOEvent interrupt is not masked	RW	0x0

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Table 15-282. Register Call Summary for Register GPMC_IRQENABLE

General-Purpose Memory Controller

- GPMC Interrupt Requests: [0] [1] [2] [3] [4]
- NAND Device-Ready Pin: [5] [6]
- Prefetch and Write-Posting Engine: [7] [8] [9] [10]
- GPMC Register Summary: [11]

Table 15-283. GPMC_TIMEOUT_CONTROL

Address Offset	0x0000 0040		
Physical Address	0x5000 0040	**Instance**	GPMC
Description	The GPMC_TIMEOUT_CONTROL register allows the user to set the start value of the timeout counter		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																TIMEOUTSTARTVALUE								RESERVED							TIMEOUTENABLE

Bits	Field Name	Description	Type	Reset
31:13	RESERVED	Write 0s for future compatibility. Read returns 0s.	RW	0x00000
12:4	TIMEOUTSTARTVALUE	Start value of the time-out counter 0x000: Zero GPMC_FCLK cycle 0x001: One GPMC_FCLK cycle ... 0x1FF: 511 GPMC_FCLK cycles	RW	0x1FF
3:1	RESERVED	Write 0s for future compatibility. Read returns 0s.	RW	0x0
0	TIMEOUTENABLE	Enable bit of the TimeOut feature 0x0: TimeOut feature is disabled 0x1: TimeOut feature is enabled	RW	0x0

Table 15-284. Register Call Summary for Register GPMC_TIMEOUT_CONTROL

General-Purpose Memory Controller

- Error Handling: [0] [1]
- GPMC Register Summary: [2]
- GPMC Register Descriptions: [3]

Table 15-285. GPMC_ERR_ADDRESS

Address Offset	0x0000 0044		
Physical Address	0x5000 0044	**Instance**	GPMC
Description	The GPMC_ERR_ADDRESS register stores the address of the illegal access when an error occurs		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								ILLEGALADD																							

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Bits	Field Name	Description	Type	Reset
31	RESERVED	Write 0s for future compatibility. Read returns 0.	RW	0x0
30:0	ILLEGALADD	Address of illegal access A30: 0 for memory region, 1 for GPMC register region A29-A0: 1 GBytes max	R	0x00000000

Table 15-286. Register Call Summary for Register GPMC_ERR_ADDRESS

General-Purpose Memory Controller

- Error Handling: [0]
- GPMC Register Summary: [1]
- GPMC Register Descriptions: [2]

Table 15-287. GPMC_ERR_TYPE

Address Offset	0x0000 0048		
Physical Address	0x5000 0048	**Instance**	GPMC
Description	The GPMC_ERR_TYPE register stores the type of error when an error occurs		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																					ILLEGALMCMD			RESERVED			ERRORNOTSUPPADD	ERRORNOTSUPPMCMD	ERRORTIMEOUT	RESERVED	ERRORVALID

Bits	Field Name	Description	Type	Reset
31:11	RESERVED	Write 0s for future compatibility. Read returns 0s.	RW	0x000000
10:8	ILLEGALMCMD	System Command of the transaction that caused the error	R	0x0
7:5	RESERVED	Write 0s for future compatibility. Read returns 0s.	RW	0x0
4	ERRORNOTSUPPADD	Not supported Address error 0x0: No error occurs 0x1: The error is due to a non supported Address	R	0x0
3	ERRORNOTSUPPMCMD	Not supported Command error 0x0: No error occurs 0x1: The error is due to a non supported Command	R	0x0
2	ERRORTIMEOUT	Time-out error 0x0: No error occurs 0x1: The error is due to a time out	R	0x0
1	RESERVED	Write 0s for future compatibility. Read returns 0.	RW	0x0
0	ERRORVALID	Error validity status - Must be explicitly cleared with a write 1 transaction 0x0: All error fields no longer valid 0x1: Error detected and logged in the other error fields	RW	0x0

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Table 15-288. Register Call Summary for Register GPMC_ERR_TYPE

General-Purpose Memory Controller

- Error Handling: [0] [1] [2]
- GPMC Register Summary: [3]
- GPMC Register Descriptions: [4]

Table 15-289. GPMC_CONFIG

Address Offset	0x0000 0050		
Physical Address	0x5000 0050	**Instance**	GPMC
Description	The configuration register allows global configuration of the GPMC		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																					WAIT2PINPOLARITY	WAIT1PINPOLARITY	WAIT0PINPOLARITY	RESERVED			WRITEPROTECT	RESERVED		LIMITEDADDRESS	NANDFORCEPOSTEDWRITE

Bits	Field Name	Description	Type	Reset
31:11	RESERVED	Write 0s for future compatibility. Read returns 0s.	RW	0x1
10	WAIT2PINPOLARITY	Selects the polarity of input pin WAIT2 0x0: WAIT2 active low 0x1: WAIT2 active high	RW	0x0
9	WAIT1PINPOLARITY	Selects the polarity of input pin WAIT1 0x0: WAIT1 active low 0x1: WAIT1 active high	RW	0x1
8	WAIT0PINPOLARITY	Selects the polarity of input pin WAIT0 0x0: WAIT0 active low 0x1: WAIT0 active high	RW	0x0
7:5	RESERVED	Write 0s for future compatibility. Read returns 0s.	RW	0x0
4	WRITEPROTECT	Controls the WP output pin level 0x0: WP output pin is low 0x1: WP output pin is high	RW	0x0
3:2	RESERVED	Write 0s for future compatibility. Read returns 0s.	RW	0x0
1	LIMITEDADDRESS	Limited Address device support 0x0: No effect 0x1: A26-A11 are not modified during an external memory access.	RW	0x0
0	NANDFORCEPOSTEDWRITE	Enables the Force Posted Write feature to NAND Cmd/Add/Data location 0x0: Disables Force Posted Write 0x1: Enables Force Posted Write	RW	0x0

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Table 15-290. Register Call Summary for Register GPMC_CONFIG

General-Purpose Memory Controller

- GPMC Signals: [0]
- GPMC Interrupt Requests: [1] [2] [3]
- GPMC Address and Data Bus: [4]
- GPMC I/O Configuration Setting: [5] [6]
- External Signals: [7] [8]
- Asynchronous and Synchronous Accesses in Nonmultiplexed Mode: [9] [10] [11] [12] [13]
- NAND Memory Device in Byte or 16-bit Word Stream Mode: [14]
- NAND Device-Ready Pin: [15]
- Set Memory Access: [16]
- GPMC Register Summary: [17]

Table 15-291. GPMC_STATUS

Address Offset	0x0000 0054		
Physical Address	0x5000 0054	**Instance**	GPMC
Description	The status register provides global status bits of the GPMC		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																					WAIT2STATUS	WAIT1STATUS	WAIT0STATUS	RESERVED							EMPTYWRITEBUFFERSTATUS

Bits	Field Name	Description	Type	Reset
31:11	RESERVED	Write 0s for future compatibility. Read returns 0s.	RW	0x000000
10	WAIT2STATUS	Is a copy of input pin WAIT2. (Reset value is WAIT2 input pin sampled at IC reset) 0x0: WAIT2 asserted (inactive state) 0x1: WAIT2 deasserted	R	0x-
9	WAIT1STATUS	Is a copy of input pin WAIT1. (Reset value is WAIT1 input pin sampled at IC reset) 0x0: WAIT1 asserted (inactive state) 0x1: WAIT1 deasserted	R	0x-
8	WAIT0STATUS	Is a copy of input pin WAIT0. (Reset value is WAIT0 input pin sampled at IC reset) 0x0: WAIT0 asserted (inactive state) 0x1: WAIT0 deasserted	R	0x-
7:1	RESERVED	Write 0s for future compatibility. Reads returns 0	RW	0x00
0	EMPTYWRITEBUFFERSTATUS	Stores the empty status of the write buffer 0x0: Write Buffer is not empty 0x1: Write Buffer is empty	R	0x1

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Table 15-292. Register Call Summary for Register GPMC_STATUS

General-Purpose Memory Controller

- NAND Memory Device in Byte or 16-bit Word Stream Mode: [0]
- NAND Device-Ready Pin: [1] [2] [3]
- GPMC Register Summary: [4]

Table 15-293. GPMC_CONFIG1_i

Address Offset	0x0000 0060 + (0x0000 0030 * i)	**Index**	i = 0 to 7
Physical Address	0x5000 0060 + (0x0000 0030 * i)	**Instance**	GPMC
Description	The configuration register 1 sets signal control parameters per chip-select		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WRAPBURST	READMULTIPLE	READTYPE	WRITEMULTIPLE	WRITETYPE	CLKACTIVATIONTIME			ATTACHEDDEVICEPAGELENGTH		WAITREADMONITORING	WAITWRITEMONITORING	RESERVED		WAITMONITORINGTIME		WAITPINSELECT		RESERVED		DEVICESIZE		DEVICETYPE		MUXADDDATA		RESERVED			TIMEPARAGRANULARITY	RESERVED			GPMCFCLKDIVIDER		

Bits	Field Name	Description	Type	Reset
31	WRAPBURST	Enables the wrapping burst capability. Must be set if the attached device is configured in wrapping burst 0x0: Synchronous wrapping burst not supported 0x1: Synchronous wrapping burst supported	RW	0x0
30	READMULTIPLE	Selects the read single or multiple access 0x0: Single access 0x1: Multiple access (burst if synchronous, page if asynchronous)	RW	0x0
29	READTYPE	Selects the read mode operation 0x0: Read Asynchronous 0x1: Read Synchronous	RW	0x0
28	WRITEMULTIPLE	Selects the write single or multiple access 0x0: Single access 0x1: Multiple access (burst if synchronous, considered as single if asynchronous)	RW	0x0
27	WRITETYPE	Selects the write mode operation 0x0: Write Asynchronous 0x1: Write Synchronous	RW	0x0
26:25	CLKACTIVATIONTIME	Output GPMC_CLK activation time 0x0: First rising edge of GPMC_CLK at start access time 0x1: First rising edge of GPMC_CLK one GPMC_FCLK cycle after start access time 0x2: First rising edge of GPMC_CLK two GPMC_FCLK cycles after start access time 0x3: Reserved	RW	0x0

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Bits	Field Name	Description	Type	Reset
24:23	ATTACHEDDEVICEPAGE LENGTH	Specifies the attached device page (burst) length 0x0: 4 Words 0x1: 8 Words 0x2: 16 Words 0x3: Reserved (1 Word = Interface size)	RW	0x0
22	WAITREADMONITORING	Selects the Wait monitoring configuration for Read accesses (Reset value is *bootwaiten* input pin sampled at IC reset) 0x0: Wait pin is not monitored for read accesses 0x1: Wait pin is monitored for read accesses	RW	0x-
21	WAITWRITEMONITORING	Selects the Wait monitoring configuration for Write accesses 0x0: Wait pin is not monitored for write accesses 0x1: Wait pin is monitored for write accesses	RW	0x0
20	RESERVED	Write 0s for future compatibility. Read returns 0.	RW	0x0
19:18	WAITMONITORINGTIME	Selects input pin Wait monitoring time 0x0: Wait pin is monitored with valid data 0x1: Wait pin is monitored one GPMC_CLK cycle before valid data 0x2: Wait pin is monitored two GPMC_CLK cycle before valid data 0x3: Reserved	RW	0x0
17:16	WAITPINSELECT	Selects the input WAIT pin for this chip-select (Reset value is *bootwaitselect* input pin sampled at IC reset for CS0 and 0 for CS1-7) 0x0: Wait input pin is WAIT0 0x1: Wait input pin is WAIT1 0x2: Wait input pin is WAIT2 0x3: Reserved	RW	0x-
15:14	RESERVED	Write 0s for future compatibility. Reads returns 0	RW	0x0
13:12	DEVICESIZE	Selects the device size attached (Reset value is *bootdevicesize* input pin sampled at IC reset for CS0 and 0x1 for CS1 to CS7) 0x0: 8 bit 0x1: 16 bit 0x2: Reserved 0x3: Reserved	RW	0x-
11:10	DEVICETYPE	Selects the attached device type 0x0: NOR Flash like, asynchronous and synchronous devices 0x1: Reserved 0x2: NAND Flash like devices, stream mode 0x3: Reserved	RW	0x0
9:8	MUXADDDATA	Enables the address and data multiplexed protocol (Reset value is *cs0muxdevice* input pin sampled at IC reset for CS0 and 0 for CS1-CS7) 0x0: Non-multiplexed attached device 0x1: AAD-mux protocol device 0x2: Address and data multiplexed attached device 0x3: Reserved	RW	0x-
7:5	RESERVED	Write 0s for future compatibility. Read returns 0s.	RW	0x0

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Bits	Field Name	Description	Type	Reset
4	TIMEPARAGRANULARITY	Signals timing latencies scalar factor (RD/WRCYCLETIME, RD/WRACCESSTIME, PAGEBURSTACCESSTIME, CSONTIME, CSRD/WROFFTIME, ADVONTIME, ADVRD/WROFFTIME, OEONTIME, OEOFFTIME, WEONTIME, WEOFFTIME, CYCLE2CYCLEDELAY, BUSTURNAROUND, TIMEOUTSTARTVALUE, WRDATAONADMUXBUS) 0x0: x1 latencies 0x1: x2 latencies	RW	0x0
3:2	RESERVED	Write 0s for future compatibility. Read returns 0s.	RW	0x0
1:0	GPMCFCLKDIVIDER	Divides the GPMC_FCLK clock 0x0: GPMC_CLK frequency = GPMC_FCLK frequency 0x1: GPMC_CLK frequency = GPMC_FCLK frequency / 2 0x2: GPMC_CLK frequency = GPMC_FCLK frequency / 3 0x3: GPMC_CLK frequency = GPMC_FCLK frequency /4	RW	0x0

Table 15-294. Register Call Summary for Register GPMC_CONFIG1_i

General-Purpose Memory Controller

- GPMC Signals: [0]
- GPMC Clock Configuration: [1] [2]
- L3 Interconnect Interface: [3] [4]
- GPMC I/O Configuration Setting: [5] [6] [7] [8] [9] [10] [11] [12]
- GPMC CS0 Default Configuration at IC Reset: [13] [14] [15] [16]
- Access Protocol: [17] [18] [19]
- External Signals: [20] [21] [22] [23] [24] [25] [26] [27] [28] [29] [30] [31] [32] [33] [34] [35] [36]
- Read Cycle Time and Write Cycle Time (RDCYCLETIME / WRCYCLETIME): [37]
- GPMC_CLK: [38] [39]
- GPMC_CLK and Control Signals Setup and Hold: [40]
- Access Time (RDACCESSTIME / WRACCESSTIME): [41]
- Page Burst Access Time (PAGEBURSTACCESSTIME): [42]
- NOR Access Description: [43] [44]
- Asynchronous Access Description: [45] [46] [47] [48]
- Synchronous Access Description: [49] [50] [51] [52] [53]
- Page and Burst Support: [54] [55]
- System Burst Versus External Device Burst Support: [56] [57] [58]
- pSRAM Access Specificities: [59]
- NAND Memory Device in Byte or 16-bit Word Stream Mode: [60] [61] [62] [63] [64] [65] [66] [67] [68] [69] [70] [71] [72] [73] [74] [75] [76] [77]
- NAND Device-Ready Pin: [78] [79]
- GPMC Configuration in NOR Mode: [80] [81] [82] [83] [84] [85] [86] [87] [88] [89] [90] [91] [92] [93] [94] [95]
- GPMC Configuration in NAND mode: [96] [97] [98] [99]
- Set Memory Access: [100] [101] [102] [103] [104]
- GPMC Timing Parameters: [105] [106] [107] [108] [109] [110] [111] [112] [113]
- GPMC Timing Parameters Formulas: [114] [115] [116] [117] [118] [119] [120] [121] [122] [123] [124] [125] [126]
- GPMC Register Summary: [127]

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Table 15-295. GPMC_CONFIG2_i

Address Offset	0x0000 0064 + (0x0000 0030 * i)	**Index**	i = 0 to 7
Physical Address	0x5000 0064 + (0x0000 0030 * i)	**Instance**	GPMC
Description	CS signal timing parameter configuration		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								CSWROFFTIME								RESERVED			CSRDOFFTIME					CSEXTRADELAY	RESERVED					CSONTIME			

Bits	Field Name	Description	Type	Reset
31:21	RESERVED	Write 0s for future compatibility. Reads returns 0	RW	0x000
20:16	CSWROFFTIME	CS i de-assertion time from start cycle time for write accesses 0x00: 0 GPMC_FCLK cycle 0x01: 1 GPMC_FCLK cycle ... 0x1F: 31 GPMC_FCLK cycles	RW	0x10
15:13	RESERVED	Write 0s for future compatibility. Read returns 0s.	RW	0x0
12:8	CSRDOFFTIME	CS i de-assertion time from start cycle time for read accesses 0x00: 0 GPMC_FCLK cycle 0x01: 1 GPMC_FCLK cycle ... 0x1F: 31 GPMC_FCLK cycles	RW	0x10
7	CSEXTRADELAY	CS i Add Extra Half GPMC_FCLK cycle 0x0: CS i Timing control signal is not delayed 0x1: CS i Timing control signal is delayed of half GPMC_FCLK clock cycle	RW	0x0
6:4	RESERVED	Write 0s for future compatibility. Read returns 0s.	RW	0x0
3:0	CSONTIME	CS i assertion time from start cycle time 0x0: 0 GPMC_FCLK cycle 0x1: 1 GPMC_FCLK cycle ... 0xF: 15 GPMC_FCLK cycles	RW	0x1

Table 15-296. Register Call Summary for Register GPMC_CONFIG2_i

General-Purpose Memory Controller

- nCS: Chip-Select Signal Control Assertion/Deassertion Time (CSONTIME / CSRDOFFTIME / CSWROFFTIME / CSEXTRADELAY): [0] [1] [2] [3]
- Asynchronous Access Description: [4] [5]
- Synchronous Access Description: [6] [7] [8] [9]
- GPMC Timing Parameters: [10] [11] [12] [13]
- GPMC Register Summary: [14]

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Table 15-297. GPMC_CONFIG3_i

Address Offset	0x0000 0068 + (0x0000 0030 * i)	**Index**	i = 0 to 7
Physical Address	0x5000 0068 + (0x0000 0030 * i)	**Instance**	GPMC
Description	nADV signal timing parameter configuration		
Type	RW		

31	30 29 28	27	26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7	6 5 4	3 2 1 0
RESERVED	ADVAADMUXWROFFTIME	RESERVED	ADVAADMUXRDOFFTIME	RESERVED	ADVWROFFTIME	RESERVED	ADVRDOFFTIME	ADVEXTRADELAY	ADVAADMUXONTIME	ADVONTIME

Bits	Field Name	Description	Type	Reset
31	RESERVED	Write 0s for future compatibility. Read returns 0s.	RW	0x0
30:28	ADVAADMUXWROFFTIME	nADV de-assertion for first address phase when using the AAD-mux protocol 0x0: 0 GPMC_FCLK cycle 0x1: 1 GPMC_FCLK cycle ... 0x7: 7 GPMC_FCLK cycles	RW	0x2
27	RESERVED	Write 0s for future compatibility. Read returns 0s.	RW	0x0
26:24	ADVAADMUXRDOFFTIME	nADV assertion for first address phase when using the AAD-mux protocol 0x0: 0 GPMC_FCLK cycle 0x1: 1 GPMC_FCLK cycle ... 0x7: 7 GPMC_FCLK cycles	RW	0x2
23:21	RESERVED	Write 0s for future compatibility. Read returns 0s.	RW	0x0
20:16	ADVWROFFTIME	nADV de-assertion time from start cycle time for write accesses 0x00: 0 GPMC_FCLK cycle 0x01: 1 GPMC_FCLK cycle ... 0x1F: 31 GPMC_FCLK cycles	RW	0x02
15:13	RESERVED	Write 0s for future compatibility. Read returns 0s.	RW	0x0
12:8	ADVRDOFFTIME	nADV de-assertion time from start cycle time for read accesses 0x00: 0 GPMC_FCLK cycle 0x01: 1 GPMC_FCLK cycle ... 0x1F: 31 GPMC_FCLK cycles	RW	0x02
7	ADVEXTRADELAY	nADV Add Extra Half GPMC_FCLK cycle 0x0: nADV Timing control signal is not delayed 0x1: nADV Timing control signal is delayed of half GPMC_FCLK clock cycle	RW	0x0
6:4	ADVAADMUXONTIME	nADV assertion for first address phase when using the AAD-mux protocol 0x0: 0 GPMC_FCLK cycle 0x1: 1 GPMC_FCLK cycle ... 0x7: 7 GPMC_FCLK cycles	RW	0x1
3:0	ADVONTIME	nADV assertion time from start cycle time 0x0: 0 GPMC_FCLK cycle 0x1: 1 GPMC_FCLK cycle ... 0xF: 15 GPMC_FCLK cycles	RW	0x1

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Table 15-298. Register Call Summary for Register GPMC_CONFIG3_i

General-Purpose Memory Controller

- nADV/ALE: Address Valid/Address Latch Enable Signal Control Assertion/Deassertion Time (ADVONTIME / ADVRDOFFTIME / ADVWROFFTIME / ADVEXTRADELAY/ADVAADMUXONTIME/ADVAADMUXRDOFFTIME/ADVAADMUXWROFFTIME): [0] [1] [2] [3] [4] [5] [6]
- Asynchronous Access Description: [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18]
- Synchronous Access Description: [19] [20] [21] [22] [23] [24] [25] [26] [27] [28] [29] [30] [31]
- GPMC Timing Parameters: [32] [33] [34] [35] [36] [37] [38]
- GPMC Register Summary: [39]

Table 15-299. GPMC_CONFIG4_i

Address Offset	0x0000 006C + (0x0000 0030 * i)	**Index**	i = 0 to 7
Physical Address	0x5000 006C + (0x0000 0030 * i)	**Instance**	GPMC
Description	nWE and nOE signals timing parameter configuration		
Type	RW		

31 30 29	28 27 26 25 24	23	22 21 20	19 18 17 16	15 14 13	12 11 10 9 8	7	6 5 4	3 2 1 0
RESERVED	WEOFFTIME	WEEXTRADELAY	RESERVED	WEONTIME	OEAADMUXOFFTIME	OEOFFTIME	OEEXTRADELAY	OEAADMUXONTIME	OEONTIME

Bits	Field Name	Description	Type	Reset
31:29	RESERVED	Write 0s for future compatibility. Read returns 0s.	RW	0x3
28:24	WEOFFTIME	nWE de-assertion time from start cycle time 0x00: 0 GPMC_FCLK cycle 0x01: 1 GPMC_FCLK cycle ... 0x1F: 31 GPMC_FCLK cycles	RW	0x10
23	WEEXTRADELAY	nWE Add Extra Half GPMC_FCLK cycle 0x0: nWE Timing control signal is not delayed 0x1: nWE Timing control signal is delayed of half GPMC_FCLK clock cycle	RW	0x0
22:20	RESERVED	Write 0s for future compatibility. Read returns 0s.	RW	0x0
19:16	WEONTIME	nWE assertion time from start cycle time 0x0: 0 GPMC_FCLK cycle 0x1: 1 GPMC_FCLK cycle ... 0xF: 15 GPMC_FCLK cycles	RW	0x5
15:13	OEAADMUX OFFTIME	nOE de-assertion time for the first address phase in an AAD-mux access 0x0: 0 GPMC_FCLK cycle 0x1: 1 GPMC_FCLK cycle ... 0x7: 7 GPMC_FCLK cycles	RW	0x3
12:8	OEOFFTIME	nOE de-assertion time from start cycle time 0x00: 0 GPMC_FCLK cycle 0x01: 1 GPMC_FCLK cycle ... 0x1F: 31 GPMC_FCLK cycles	RW	0x10
7	OEEXTRADELAY	nOE Add Extra Half GPMC_FCLK cycle 0x0: nOE Timing control signal is not delayed 0x1: nOE Timing control signal is delayed of half GPMC_FCLK clock cycle	RW	0x0

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Bits	Field Name	Description	Type	Reset
6:4	OEAADMUX ONTIME	nOE assertion time for the first address phase in an AAD-mux access 0x0: 0 GPMC_FCLK cycle 0x1: 1 GPMC_FCLK cycle ... 0x7: 7 GPMC_FCLK cycles	RW	0x1
3:0	OEONTIME	nOE assertion time from start cycle time 0x0: 0 GPMC_FCLK cycle 0x1: 1 GPMC_FCLK cycle ... 0xF: 15 GPMC_FCLK cycles	RW	0x6

Table 15-300. Register Call Summary for Register GPMC_CONFIG4_i

General-Purpose Memory Controller

- nOE/nRE: Output Enable / Read Enable Signal Control Assertion / Deassertion Time (OEONTIME / OEOFFTIME / OEEXTRADELAY / OEAADMUXONTIME / OEAADMUXOFFTIME): [0] [1] [2]
- nWE: Write Enable Signal Control Assertion / Deassertion Time (WEONTIME / WEOFFTIME / WEEXTRADELAY): [3] [4] [5]
- Asynchronous Access Description: [6] [7] [8] [9] [10] [11] [12] [13]
- Synchronous Access Description: [14] [15] [16] [17] [18] [19] [20] [21] [22] [23] [24]
- NAND Memory Device in Byte or 16-bit Word Stream Mode: [25]
- GPMC Timing Parameters: [26] [27] [28] [29] [30] [31] [32] [33]
- GPMC Register Summary: [34]

Table 15-301. GPMC_CONFIG5_i

Address Offset	0x0000 0070 + (0x0000 0030 * i)	**Index**	i = 0 to 7
Physical Address	0x5000 0070 + (0x0000 0030 * i)	**Instance**	GPMC
Description	RdAccessTime and CycleTime timing parameters configuration		
Type	RW		

31 30 29 28	27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
RESERVED	PAGEBURSTACCESSTIME	RESERVED / RDACCESSTIME	RESERVED / WRCYCLETIME	RESERVED / RDCYCLETIME

Bits	Field Name	Description	Type	Reset
31:28	RESERVED	Write 0s for future compatibility. Read returns 0s.	RW	0x0
27:24	PAGEBURSTACCESSTIME	Delay between successive words in a multiple access 0x0: 0 GPMC_FCLK cycle 0x1: 1 GPMC_FCLK cycle ... 0xF: 15 GPMC_FCLK cycles	RW	0x1
23:21	RESERVED	Write 0s for future compatibility. Read returns 0s.	RW	0x0
20:16	RDACCESSTIME	Delay between start cycle time and first data valid 0x00: 0 GPMC_FCLK cycle 0x01: 1 GPMC_FCLK cycle ... 0x1F: 31 GPMC_FCLK cycles	RW	0x0F
15:13	RESERVED	Write 0s for future compatibility. Reads returns 0	RW	0x0

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Bits	Field Name	Description	Type	Reset
12:8	WRCYCLETIME	Total write cycle time 0x00: 0 GPMC_FCLK cycle 0x01: 1 GPMC_FCLK cycle ... 0x1F: 31 GPMC_FCLK cycles	RW	0x11
7:5	RESERVED	Write 0s for future compatibility. Read returns 0s.	RW	0x0
4:0	RDCYCLETIME	Total read cycle time 0x00: 0 GPMC_FCLK cycle 0x01: 1 GPMC_FCLK cycle ... 0x1F: 31 GPMC_FCLK cycles	RW	0x11

Table 15-302. Register Call Summary for Register GPMC_CONFIG5_i

General-Purpose Memory Controller

- Read Cycle Time and Write Cycle Time (RDCYCLETIME / WRCYCLETIME): [0] [1]
- Access Time (RDACCESSTIME / WRACCESSTIME): [2] [3] [4]
- Page Burst Access Time (PAGEBURSTACCESSTIME): [5]
- Asynchronous Access Description: [6] [7] [8]
- Synchronous Access Description: [9] [10] [11] [12] [13] [14] [15] [16] [17]
- Asynchronous and Synchronous Accesses in Nonmultiplexed Mode: [18] [19] [20] [21]
- GPMC Timing Parameters: [22] [23] [24] [25]
- GPMC Register Summary: [26]

Table 15-303. GPMC_CONFIG6_i

Address Offset	0x0000 0074 + (0x0000 0030 * i)	**Index**	i = 0 to7
Physical Address	0x5000 0074 + (0x0000 0030 * i)	**Instance**	GPMC
Description	WrAccessTime, WrDataOnADmuxBus, Cycle2Cycle and BusTurnAround parameters configuration		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			RESERVED					WRACCESSTIME								RESERVED								WRDATAONADMUXBUS				CYCLE2CYCLEDELAY				CYCLE2CYCLESAMECSEN	CYCLE2CYCLEDIFFCSEN	RESERVED		BUSTURNAROUND			

Bits	Field Name	Description	Type	Reset
31	RESERVED	TI Internal use - Do not modify.	RW	0x1
30:29	RESERVED	Write 0s for future compatibility. Read returns 0s.	RW	0x0
28:24	WRACCESSTIME	Delay from start access time to the GPMC_FCLK rising edge corresponding the the GPMC_CLK rising edge used by the attached memory for the first data capture 0x00: 0 GPMC_FCLK cycle 0x01: 1 GPMC_FCLK cycle ... 0x1F: 31 GPMC_FCLK cycles	RW	0x0F
23:20	RESERVED	Write 0s for future compatibility. Read returns 0s.	RW	0x0
19:16	WRDATAONADMUXBUS	Specifies on which GPMC_FCLK rising edge the first data of the synchronous burst write is driven in the add/data mux bus	RW	0x7
15:12	RESERVED	Write 0s for future compatibility. Read returns 0s.	RW	0x0

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Bits	Field Name	Description	Type	Reset
11:8	CYCLE2CYCLEDELAY	Chip-select high pulse delay between successive accesses 0x0: 0 GPMC_FCLK cycle 0x1: 1 GPMC_FCLK cycle ... 0xF: 15 GPMC_FCLK cycles	RW	0x0
7	CYCLE2CYCLESAMECSEN	Add CYCLE2CYCLEDELAY between successive accesses to the same CS (any access type) 0x0: No delay between the two accesses 0x1: Add CYCLE2CYCLEDELAY	RW	0x0
6	CYCLE2CYCLEDIFFCSEN	Add CYCLE2CYCLEDELAY between successive accesses to a different CS (any access type) 0x0: No delay between the two accesses 0x1: Add CYCLE2CYCLEDELAY	RW	0x0
5:4	RESERVED	Write 0s for future compatibility. Reads returns 0	RW	0x0
3:0	BUSTURNAROUND	Bus turn around latency between successive accesses to the same CS (read to write) or to a different CS (read to read and read to write) 0x0: 0 GPMC_FCLK cycle 0x1: 1 GPMC_FCLK cycle ... 0xF: 15 GPMC_FCLK cycles	RW	0x0

Table 15-304. Register Call Summary for Register GPMC_CONFIG6_i

General-Purpose Memory Controller

- External Signals: [0] [1] [2] [3] [4] [5]
- Read Cycle Time and Write Cycle Time (RDCYCLETIME / WRCYCLETIME): [6] [7]
- Access Time (RDACCESSTIME / WRACCESSTIME): [8] [9]
- Asynchronous Access Description: [10] [11] [12] [13]
- Synchronous Access Description: [14] [15] [16] [17]
- GPMC Timing Parameters: [18] [19] [20] [21] [22] [23]
- GPMC Register Summary: [24]

Table 15-305. GPMC_CONFIG7_i

Address Offset	0x0000 0078 + (0x0000 0030 * i)	**Index**	i = 0 to 7
Physical Address	0x5000 0078 + (0x0000 0030 * i)	**Instance**	GPMC
Description	CS address mapping configuration		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				MASKADDRESS				RESERVED	CSVALID	BASEADDRESS					

Bits	Field Name	Description	Type	Reset
31:12	RESERVED	Write 0s for future compatibility. Read returns 0s.	RW	0x00000
11:8	MASKADDRESS	CS mask address. 0x1000: Chip-select size of 128 Mbytes 0x1100: Chip-select size of 64 Mbytes 0x1110: Chip-select size of 32 Mbytes 0x1111: Chip-select size of 16 Mbytes Other values must be avoided as they create holes in the chip-select address space.	RW	0xF

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Bits	Field Name	Description	Type	Reset
7	RESERVED	Write 0s for future compatibility. Read returns 0.	RW	0x0
6	CSVALID	CS enable 0x0: CS disabled 0x1: CS enabled	RW	See (1)
5:0	BASEADDRESS	CSi base address where i = 0 to 7 (16M bytes minimum granularity) bits [5:0] corresponds to A29, A28, A27, A26, A25, and A24. See Figure 15-55	RW	0x00

(1) Reset value is 0x1 for CS0 and 0x0 for CS1 to CS7

Table 15-306. Register Call Summary for Register GPMC_CONFIG7_i

General-Purpose Memory Controller
- Chip-Select Base Address and Region Size: [0] [1] [2]
- NAND Memory Device in Byte or 16-bit Word Stream Mode: [3]
- GPMC Configuration in NOR Mode: [4] [5] [6]
- GPMC Configuration in NAND mode: [7] [8] [9]
- GPMC Timing Parameters: [10]
- GPMC Register Summary: [11]

Table 15-307. GPMC_NAND_COMMAND_i

Address Offset	0x0000 007C + (0x0000 0030 * i)	**Index**	i = 0 to 7
Physical Address	0x5000 007C + (0x0000 0030 * i)	**Instance**	GPMC
Description	This register is not a true register, just an address location.		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPMC_NAND_COMMAND																															

Bits	Field Name	Description	Type	Reset
31:0	GPMC_NAND_COMMAND	This register is not a true register, just an address location. Writing data at the GPMC_NAND_COMMAND_i location places the data as the NAND command value on the bus, using a regular asynchronous write access.	W	n/a

Table 15-308. Register Call Summary for Register GPMC_NAND_COMMAND_i

General-Purpose Memory Controller
- NAND Memory Device in Byte or 16-bit Word Stream Mode: [0] [1] [2] [3] [4] [5]
- Prefetch and Write-Posting Engine: [6]
- GPMC Register Summary: [7]
- GPMC Register Descriptions: [8]

Table 15-309. GPMC_NAND_ADDRESS_i

Address Offset	0x0000 0080 + (0x0000 0030 * i)	**Index**	i = 0 to 7
Physical Address	0x5000 0080 + (0x0000 0030 * i)	**Instance**	GPMC
Description	This register is not a true register, just an address location.		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPMC_NAND_ADDRESS																															

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Bits	Field Name	Description	Type	Reset
31:0	GPMC_NAND_ADDRESS	This register is not a true register, just an address location. Writing data at the GPMC_NAND_ADDRESS_i location places the data as the NAND partial address value on the bus, using a regular asynchronous write access.	W	n/a

Table 15-310. Register Call Summary for Register GPMC_NAND_ADDRESS_i

General-Purpose Memory Controller

- NAND Memory Device in Byte or 16-bit Word Stream Mode: [0] [1] [2] [3] [4] [5]
- Prefetch and Write-Posting Engine: [6]
- GPMC Register Summary: [7]
- GPMC Register Descriptions: [8]

Table 15-311. GPMC_NAND_DATA_i

Address Offset	0x0000 0084 + (0x0000 0030 * i)	**Index**	i = 0 to 7
Physical Address	0x5000 0084 + (0x0000 0030 * i)	**Instance**	GPMC
Description	This register is not a true register, just an address location.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPMC_NAND_DATA																															

Bits	Field Name	Description	Type	Reset
31:0	GPMC_NAND_DATA	This register is not a true register, just an address location. Reading data from the GPMC_NAND_DATA_i location or from any location in the associated chip-select memory region activates an asynchronous read access.	W	n/a

Table 15-312. Register Call Summary for Register GPMC_NAND_DATA_i

General-Purpose Memory Controller

- NAND Memory Device in Byte or 16-bit Word Stream Mode: [0] [1] [2] [3]
- Prefetch and Write-Posting Engine: [4] [5]
- GPMC Register Summary: [6]
- GPMC Register Descriptions: [7] [8] [9]

Table 15-313. GPMC_PREFETCH_CONFIG1

Address Offset	0x0000 01E0		
Physical Address	0x5000 01E0	**Instance**	GPMC
Description	Prefetch engine configuration 1		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	CYCLEOPTIMIZATION			ENABLEOPTIMIZEDACCESS	ENGINECSSELECTOR			PFPWENROUNDROBIN	RESERVED			PFPWWEIGHTEDPRIO				RESERVED	FIFOTHRESHOLD							ENABLEENGINE	RESERVED	WAITPINSELECTOR		SYNCHROMODE	DMAMODE	RESERVED	ACCESSMODE

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Bits	Field Name	Description	Type	Reset
31	RESERVED	Write 0s for future compatibility. Read returns 0.	RW	0x0
30:28	CYCLEOPTIMIZATION	Define the number of GPMC_FCLK cycles to be subtracted from RDCYCLETIME, WRCYCLETIME, ACCESSTIME, CSRDOFFTIME, CSWROFFTIME, ADVRDOFFTIME, ADVWROFFTIME, OEOFFTIME, WEOFFTIME 0x0: 0 GPMC_FCLK cycle 0x1: 1 GPMC_FCLK cycle ... 0x7: 7 GPMC_FCLK cycles	RW	0x0
27	ENABLEOPTIMIZEDACCESS	Enables access cycle optimization 0x0: Access cycle optimization is disabled 0x1: Access cycle optimization is enabled	RW	0x0
26:24	ENGINECSSELECTOR	Selects the CS where Prefetch Postwrite engine is active 0x0: CS0 0x1: CS1 0x2: CS2 0x3: CS3 0x4: CS4 0x5: CS5 0x6: CS6 0x7: CS7	RW	0x0
23	PFPWENROUNDROBIN	Enables the PFPW RoundRobin arbitration 0x0: Prefetch Postwrite engine round robin arbitration is disabled 0x1: Prefetch Postwrite engine round robin arbitration is enabled	RW	0x0
22:20	RESERVED	Write 0s for future compatibility. Read returns 0s.	RW	0x0
19:16	PFPWWEIGHTEDPRIO	When an arbitration occurs between a DMA and a PFPW engine access, the DMA is always serviced. If the PFPWEnRoundRobin is enabled, 0x0: the next access is granted to the PFPW engine, 0x1: the two next accesses are granted to the PFPW engine, ..., 0xF: the 16 next accesses are granted to the PFPW engine.	RW	0x0
15	RESERVED	Write 0s for future compatibility. Read returns 0.	RW	0x0
14:8	FIFOTHRESHOLD	Selects the maximum number of bytes read from the FIFO or written to the FIFO by the host on a DMA or interrupt request 0x00: 0 byte 0x01: 1 byte ... 0x40: 64 bytes	RW	0x40
7	ENABLEENGINE	Enables the Prefetch Postwite engine 0x0: Prefetch Postwrite engine is disabled 0x1: Prefetch Postwrite engine is enabled	RW	0x0
6	RESERVED	Write 0s for future compatibility. Read returns 0.	RW	0x0
5:4	WAITPINSELECTOR	Select which wait pin edge detector should start the engine in synchronized mode 0x0: Selects Wait0 EdgeDetection 0x1: Selects Wait1 EdgeDetection 0x2: Selects Wait2 EdgeDetection 0x3: Reserved	RW	0x0

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Bits	Field Name	Description	Type	Reset
3	SYNCHROMODE	Selects when the engine starts the access to CS 0x0: Engine starts the access to CS as soon as STARTENGINE is set 0x1: Engine starts the access to CS as soon as STARTENGINE is set AND wait to non wait edge detection on the selected wait pin	RW	0x0
2	DMAMODE	Selects interrupt synchronization or DMA request synchronization 0x0: Interrupt synchronization is enabled. Only interrupt line will be activated on FIFO threshold crossing. 0x1: DMA request synchronization is enabled. A DMA request protocol is used.	RW	0x0
1	RESERVED	Write 0s for future compatibility. Read returns 0.	RW	0x0
0	ACCESSMODE	Selects prefetch read or write-posting accesses 0x0: Prefetch read mode 0x1: Write-posting mode	RW	0x0

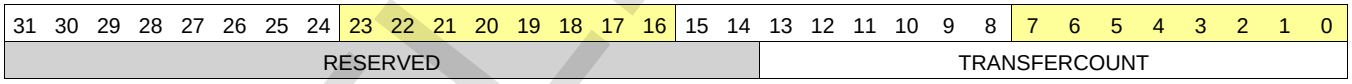
Table 15-314. Register Call Summary for Register GPMC_PREFETCH_CONFIG1

General-Purpose Memory Controller

- GPMC Interrupt Requests: [0]
- Prefetch and Write-Posting Engine: [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23] [24] [25] [26] [27] [28] [29] [30] [31] [32]
- GPMC Configuration in NAND mode: [33] [34] [35] [36] [37] [38] [39] [40] [41] [42]
- GPMC Register Summary: [43]

Table 15-315. GPMC_PREFETCH_CONFIG2

Address Offset	0x0000 01E4		
Physical Address	0x5000 01E4	**Instance**	GPMC
Description	Prefetch engine configuration 2		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:14	RESERVED	Write 0s for future compatibility. Read returns 0s.	RW	0x00000
13:0	TRANSFERCOUNT	Selects the number of bytes to be read or written by the engine to the selected CS 0x0000: 0 byte 0x0001: 1 byte ... 0x2000: 8 Kbytes	RW	0x0000

Table 15-316. Register Call Summary for Register GPMC_PREFETCH_CONFIG2

General-Purpose Memory Controller

- Prefetch and Write-Posting Engine: [0] [1] [2] [3]
- GPMC Configuration in NAND mode: [4]
- GPMC Register Summary: [5]

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Table 15-317. GPMC_PREFETCH_CONTROL

Address Offset	0x0000 01EC		
Physical Address	0x5000 01EC	**Instance**	GPMC
Description	Prefetch engine control		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															STARTENGINE

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Write 0s for future compatibility. Read returns 0s.	RW	0x00000000
0	STARTENGINE	Resets the FIFO pointer and starts the engine Read 0x0: Engine is stopped Write 0x0 stops the engine Read 0x1: Engine is running Write 0x1 resets the FIFO pointer to 0x0 in prefetch mode and 0x40 in postwrite mode and starts the engine	RW	0x0

Table 15-318. Register Call Summary for Register GPMC_PREFETCH_CONTROL

General-Purpose Memory Controller

- Prefetch and Write-Posting Engine: [0] [1] [2] [3] [4] [5] [6]
- GPMC Configuration in NAND mode: [7] [8]
- GPMC Register Summary: [9]

Table 15-319. GPMC_PREFETCH_STATUS

Address Offset	0x0000 01F0		
Physical Address	0x5000 01F0	**Instance**	GPMC
Description	Prefetch engine status		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							FIFOPOINTER								RESERVED	FIFOTHRESHOLDSTATUS	RESERVED															COUNTVALUE	

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Bits	Field Name	Description	Type	Reset
31	RESERVED	Write 0s for future compatibility. Read returns 0.	RW	0x0
30:24	FIFOPOINTER	Number of available bytes to be read or number of free empty byte places to be written 0x00: 0 byte available to be read or 0 free empty place to be written ... 0x40: 64 bytes available to be read or 64 empty places to be written	R	0x00
23:17	RESERVED	Write 0s for future compatibility. Read returns 0s.	RW	0x00
16	FIFOTHRESHOLDSTATUS	Set when FIFOPointer exceeds FIFOThreshold value 0x0: FIFOPointer smaller or equal to FIFOThreshold. Writing to this bit has no effect 0x1: FIFOPointer greater than FIFOThreshold. Writing to this bit has no effect	R	0x0
15:14	RESERVED	Write 0s for future compatibility. Read returns 0s.	RW	0x0
13:0	COUNTVALUE	Number of remaining bytes to be read or to be written by the engine according to the TransferCount value 0x0000: 0 byte remaining to be read or to be written 0x0001: 1 byte remaining to be read or to be written ... 0x2000: 8 Kbytes remaining to be read or to be written	R	0x0000

Table 15-320. Register Call Summary for Register GPMC_PREFETCH_STATUS

General-Purpose Memory Controller

- Prefetch and Write-Posting Engine: [0] [1] [2] [3] [4] [5] [6]
- GPMC Register Summary: [7]
- GPMC Register Descriptions: [8] [9]

Table 15-321. GPMC_ECC_CONFIG

Address Offset	0x0000 01F4		
Physical Address	0x5000 01F4	**Instance**	GPMC
Description	ECC configuration		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															ECCALGORITHM	RESERVED		ECCBCHTSEL		ECCWRAPMODE				ECC16B	ECCTOPSECTOR			ECCCS			ECCENABLE

Bits	Field Name	Description	Type	Reset
31:17	RESERVED	Write 0s for future compatibility. Read returns 0s.	RW	0x0000
16	ECCALGORITHM	ECC algorithm used 0x0: Hamming code 0x1: BCH code	RW	0x0
15:14	RESERVED	Write 0s for future compatibility. Read returns 0s.	RW	0x0
13:12	ECCBCHTSEL	Error correction capability used for BCH 0x0: Up to 4 bits error correction (t = 4) 0x1: Up to 8 bits error correction (t = 8) 0x2: Up to 16 bits error correction (t = 16) 0x3: Reserved	RW	0x1

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Bits	Field Name	Description	Type	Reset
11:8	ECCWRAPMODE	Spare area organization definition for the BCH algorithm. See the BCH syndrome/parity calculator module functional specification for more details	RW	0x0
7	ECC16B	Selects an ECC calculated on 16 columns 0x0: ECC calculated on 8 columns 0x1: ECC calculated on 16 columns	RW	0x0
6:4	ECCTOPSECTOR	Number of sectors to process with the BCH algorithm 0x0: 1 sector (512kB page) 0x1: 2 sectors ... 0x3: 4 sectors (2kB page) ... 0x7: 8 sectors (4kB page)	RW	0x3
3:1	ECCCS	Selects the CS where ECC is computed 0x0: Chip-select 0 0x1: Chip-select 1 0x2: Chip-select 2 0x3: Chip-select 3 Other: Reserved	RW	0x0
0	ECCENABLE	Enables the ECC feature 0x0: ECC disabled 0x1: ECC enabled	RW	0x0

Table 15-322. Register Call Summary for Register GPMC_ECC_CONFIG

General-Purpose Memory Controller

- ECC Calculator: [0] [1] [2] [3] [4] [5] [6] [7]
- GPMC Configuration in NAND mode: [8] [9] [10] [11] [12] [13]
- GPMC Register Summary: [14]
- GPMC Register Descriptions: [15] [16] [17]

Table 15-323. GPMC_ECC_CONTROL

Address Offset	0x0000 01F8		
Physical Address	0x5000 01F8	**Instance**	GPMC
Description	ECC control		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							ECCCLEAR	RESERVED				ECCPOINTER			

Bits	Field Name	Description	Type	Reset
31:9	RESERVED	Write 0s for future compatibility. Read returns 0s.	RW	0x000000
8	ECCCLEAR	Clear all ECC result registers Reads returns 0 Write 0x1 to this field clear all ECC result registers Write 0x0 is ignored	RW	0x0
7:4	RESERVED	Write 0s for future compatibility. Read returns 0s.	RW	0x0

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Bits	Field Name	Description	Type	Reset
3:0	ECCPOINTER	Selects ECC result register (Reads to this field give the dynamic position of the ECC pointer - Writes to this field select the ECC result register where the first ECC computation will be stored); Other enums: writing other values disables the ECC engine (ECCENABLE bit of GPMC_ECC_CONFIG set to 0) 0x0: Writing 0x0 disables the ECC engine (ECCENABLE bit of GPMC_ECC_CONFIG set to 0) 0x1: ECC result register 1 selected 0x2: ECC result register 2 selected 0x3: ECC result register 3 selected 0x4: ECC result register 4 selected 0x5: ECC result register 5 selected 0x6: ECC result register 6 selected 0x7: ECC result register 7 selected 0x8: ECC result register 8 selected 0x9: ECC result register 9 selected	RW	0x0

Table 15-324. Register Call Summary for Register GPMC_ECC_CONTROL

General-Purpose Memory Controller

- ECC Calculator: [0] [1] [2] [3]
- GPMC Configuration in NAND mode: [4] [5]
- GPMC Register Summary: [6]

Table 15-325. GPMC_ECC_SIZE_CONFIG

Address Offset	0x0000 01FC		
Physical Address	0x5000 01FC	**Instance**	GPMC
Description	ECC size		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								ECCSIZE1								RESERVED				ECCSIZE0				RESERVED								ECC9RESULTSIZE	ECC8RESULTSIZE	ECC7RESULTSIZE	ECC6RESULTSIZE	ECC5RESULTSIZE	ECC4RESULTSIZE	ECC3RESULTSIZE	ECC2RESULTSIZE	ECC1RESULTSIZE

Bits	Field Name	Description	Type	Reset
31:30	RESERVED	Write 0s for future compatibility. Read returns 0s.	RW	0x0
29:22	ECCSIZE1	Defines ECC size 1 0x00: 2 Bytes 0x01: 4 Bytes 0x02: 6 Bytes 0x03: 8 Bytes ... 0xFF: 512 Bytes	RW	0xFF
21:20	RESERVED	Write 0s for future compatibility. Read returns 0s.	RW	0x0
19:12	ECCSIZE0	Defines ECC size 0 0x00: 2 Bytes 0x01: 4 Bytes 0x02: 6 Bytes 0x03: 8 Bytes ... 0xFF: 512 Bytes	RW	0xFF

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Bits	Field Name	Description	Type	Reset
11:9	RESERVED	Write 0s for future compatibility. Read returns 0s.	RW	0x0
8	ECC9RESULTSIZE	Selects ECC size for ECC 9 result register 0x0: ECCSIZE0 selected 0x1: ECCSIZE1 selected	RW	0x0
7	ECC8RESULTSIZE	Selects ECC size for ECC 8 result register 0x0: ECCSIZE0 selected 0x1: ECCSIZE1 selected	RW	0x0
6	ECC7RESULTSIZE	Selects ECC size for ECC 7 result register 0x0: ECCSIZE0 selected 0x1: ECCSIZE1 selected	RW	0x0
5	ECC6RESULTSIZE	Selects ECC size for ECC 6 result register 0x0: ECCSIZE0 selected 0x1: ECCSIZE1 selected	RW	0x0
4	ECC5RESULTSIZE	Selects ECC size for ECC 5 result register 0x0: ECCSIZE0 selected 0x1: ECCSIZE1 selected	RW	0x0
3	ECC4RESULTSIZE	Selects ECC size for ECC 4 result register 0x0: ECCSIZE0 selected 0x1: ECCSIZE1 selected	RW	0x0
2	ECC3RESULTSIZE	Selects ECC size for ECC 3 result register 0x0: ECCSIZE0 selected 0x1: ECCSIZE1 selected	RW	0x0
1	ECC2RESULTSIZE	Selects ECC size for ECC 2 result register 0x0: ECCSIZE0 selected 0x1: ECCSIZE1 selected	RW	0x0
0	ECC1RESULTSIZE	Selects ECC size for ECC 1 result register 0x0: ECCSIZE0 selected 0x1: ECCSIZE1 selected	RW	0x0

Table 15-326. Register Call Summary for Register GPMC_ECC_SIZE_CONFIG

General-Purpose Memory Controller

- ECC Calculator: [0] [1] [2] [3]
- GPMC Configuration in NAND mode: [4] [5]
- GPMC Register Summary: [6]

Table 15-327. GPMC_ECCj_RESULT

Address Offset	0x0000 0200 + (0x0000 0004 * (j - 1))	**Index**	j = 1 to 9
Physical Address	0x5000 0200 + (0x0000 0004 * j)	**Instance**	GPMC
Description	ECC result register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				P2048o	P1024o	P512o	P256o	P128o	P64o	P32o	P16o	P8o	P4o	P2o	P1o	RESERVED				P2048e	P1024e	P512e	P256e	P128e	P64e	P32e	P16e	P8e	P4e	P2e	P1e

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Bits	Field Name	Description	Type	Reset
31:28	RESERVED	Write 0s for future compatibility. Read returns 0s.	RW	0x0
27	P2048o	Odd row parity bit 2048, only used for ECC computed on 512 Bytes	R	0x0
26	P1024o	Odd row parity bit 1024	R	0x0
25	P512o	Odd row parity bit 512	R	0x0
24	P256o	Odd row parity bit 256	R	0x0
23	P128o	Odd row parity bit 128	R	0x0
22	P64o	Odd row parity bit 64	R	0x0
21	P32o	Odd row parity bit 32	R	0x0
20	P16o	Odd row parity bit 16	R	0x0
19	P8o	Odd row parity bit 8	R	0x0
18	P4o	Odd Column Parity bit 4	R	0x0
17	P2o	Odd Column Parity bit 2	R	0x0
16	P1o	Odd Column Parity bit 1	R	0x0
15:12	RESERVED	Write 0s for future compatibility. Read returns 0s.	RW	0x0
11	P2048e	Even row parity bit 2048, only used for ECC computed on 512 Bytes	R	0x0
10	P1024e	Even row parity bit 1024	R	0x0
9	P512e	Even row parity bit 512	R	0x0
8	P256e	Even row parity bit 256	R	0x0
7	P128e	Even row parity bit 128	R	0x0
6	P64e	Even row parity bit 64	R	0x0
5	P32e	Even row parity bit 32	R	0x0
4	P16e	Even row parity bit 16	R	0x0
3	P8e	Even row parity bit 8	R	0x0
2	P4e	Even column parity bit 4	R	0x0
1	P2e	Even column parity bit 2	R	0x0
0	P1e	Even column parity bit 1	R	0x0

Table 15-328. Register Call Summary for Register GPMC_ECCj_RESULT

General-Purpose Memory Controller
- ECC Calculator: [0] [1] [2] [3] [4] [5] [6] [7]
- GPMC Register Summary: [8]

Table 15-329. GPMC_BCH_RESULT0_i

Address Offset	0x0000 0240 + (0x0000 0010 * i)	**Index**	i = 0 to 7
Physical Address	0x5000 0240 + (0x0000 0010 * i)	**Instance**	GPMC
Description	BCH ECC result (bits 0 to 31)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BCH_RESULT_0																															

Bits	Field Name	Description	Type	Reset
31:0	BCH_RESULT_0	BCH ECC result (bits 0 to 31)	RW	0x00000000

Table 15-330. Register Call Summary for Register GPMC_BCH_RESULT0_i

General-Purpose Memory Controller
- ECC Calculator: [0]
- GPMC Register Summary: [1]

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Table 15-331. GPMC_BCH_RESULT1_i

Address Offset	0x0000 0244 + (0x0000 0010 * i)	**Index**	i = 0 to 7
Physical Address	0x5000 0244 + (0x0000 0010 * i)	**Instance**	GPMC
Description	BCH ECC result (bits 32 to 63)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BCH_RESULT_1																															

Bits	Field Name	Description	Type	Reset
31:0	BCH_RESULT_1	BCH ECC result (bits 32 to 63)	RW	0x00000000

Table 15-332. Register Call Summary for Register GPMC_BCH_RESULT1_i

General-Purpose Memory Controller

- ECC Calculator: [0]
- GPMC Register Summary: [1]

Table 15-333. GPMC_BCH_RESULT2_i

Address Offset	0x0000 0248 + (0x0000 0010 * i)	**Index**	i = 0 to 7
Physical Address	0x5000 0248 + (0x0000 0010 * i)	**Instance**	GPMC
Description	BCH ECC result (bits 64 to 95)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BCH_RESULT_2																															

Bits	Field Name	Description	Type	Reset
31:0	BCH_RESULT_2	BCH ECC result (bits 64 to 95)	RW	0x00000000

Table 15-334. Register Call Summary for Register GPMC_BCH_RESULT2_i

General-Purpose Memory Controller

- ECC Calculator: [0]
- GPMC Register Summary: [1]

Table 15-335. GPMC_BCH_RESULT3_i

Address Offset	0x0000 024C + (0x0000 0010 * i)	**Index**	i = 0 to 7
Physical Address	0x5000 024C + (0x0000 0010 * i)	**Instance**	GPMC
Description	BCH ECC result (bits 96 to 127)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BCH_RESULT_3																															

Bits	Field Name	Description	Type	Reset
31:0	BCH_RESULT_3	BCH ECC result (bits 96 to 127)	RW	0x00000000

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Table 15-336. Register Call Summary for Register GPMC_BCH_RESULT3_i

General-Purpose Memory Controller

- ECC Calculator: [0]
- GPMC Register Summary: [1]

Table 15-337. GPMC_BCH_RESULT4_i

Address Offset	0x0000 0300 + (0x0000 0010 * i)	**Index**	i = 0 to 7
Physical Address	0x5000 0300 + (0x0000 0010 * i)	**Instance**	GPMC
Description	BCH ECC result (bits 128 to 159)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BCH_RESULT_4																															

Bits	Field Name	Description	Type	Reset
31:0	BCH_RESULT_4	BCH ECC result (bits 128 to 159)	RW	0x00000000

Table 15-338. Register Call Summary for Register GPMC_BCH_RESULT4_i

General-Purpose Memory Controller

- GPMC Register Summary: [0]

Table 15-339. GPMC_BCH_RESULT5_i

Address Offset	0x0000 0304 + (0x0000 0010 * i)	**Index**	i = 0 to 7
Physical Address	0x5000 0304 + (0x0000 0010 * i)	**Instance**	GPMC
Description	BCH ECC result (bits 160 to 191)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BCH_RESULT_5																															

Bits	Field Name	Description	Type	Reset
31:0	BCH_RESULT_5	BCH ECC result (bits 160 to 191)	RW	0x00000000

Table 15-340. Register Call Summary for Register GPMC_BCH_RESULT5_i

General-Purpose Memory Controller

- GPMC Register Summary: [0]

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Table 15-341. GPMC_BCH_RESULT6_i

Address Offset	0x0000 0308 + (0x0000 0010 * i)	**Index**	i = 0 to 7
Physical Address	0x5000 0308 + (0x0000 0010 * i)	**Instance**	GPMC
Description	BCH ECC result (bits 192 to 207)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																BCH_RESULT_6															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Write 0s for future compatibility. Read returns 0s.	R	0x0000
15:0	BCH_RESULT_6	BCH ECC result (bits 192 to 207)	RW	0x0000

Table 15-342. Register Call Summary for Register GPMC_BCH_RESULT6_i

General-Purpose Memory Controller

- GPMC Register Summary: [0]

Table 15-343. GPMC_BCH_SWDATA

Address Offset	0x0000 02D0		
Physical Address	0x5000 02D0	**Instance**	GPMC
Description	This register is used to directly pass data to the BCH ECC calculator without accessing the actual NAND flash interface.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																BCH_DATA															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Write 0s for future compatibility. Read returns 0s.	R	0x0000
15:0	BCH_DATA	Data to be included in the BCH calculation. Only bits 0 to 7 are taken into account if the calculator is configured to use 8 bits data (GPMC_ECC_CONFIG[7] ECC16B = 0)	RW	0x0000

Table 15-344. Register Call Summary for Register GPMC_BCH_SWDATA

General-Purpose Memory Controller

- GPMC Register Summary: [0]

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15.5 Error Location Module

15.5.1 Error Location Module Overview

Non-managed NAND flash memories can be dense and nonvolatile in their own nature, but error-prone. When reading from NAND flash memories, some level of error-correction is required. In the case of NAND modules with no internal correction capability, sometimes referred to as *bare NANDs*, the correction process is delegated to the memory controller.

The general-purpose memory controller (GPMC) probes data read from an external NAND flash and uses this to compute checksum-like information, called syndrome polynomials, on a per-block basis. Each syndrome polynomial gives a status of the read operations for a full block, including 512 bytes of data, parity bits, and an optional spare-area data field, with a maximum block size of 1023 bytes. Computation is based on a Bose-ChaudhurI-Hocquenghem (BCH) algorithm. The error-location module (ELM) extracts error addresses from these syndrome polynomials.

Based on the syndrome polynomial value, the ELM can detect errors, compute the number of errors, and give the location of each error bit. The actual data is not required to complete the error-correction algorithm. Errors can be reported anywhere in the NAND flash block, including in the parity bits.

The maximum acceptable number of errors that can be corrected depends on a programmable configuration parameter. 4-, 8-, and 16-bit error-correction levels are supported. The ELM relies on a static and fixed definition of the generator polynomial for each error-correction level that corresponds to the generator polynomials defined in the GPMC (there are three fixed polynomial for the three correction error levels). A larger number of errors than the programmed error-correction level may be detected, but the ELM cannot correct them all. The offending block is then tagged as *uncorrectable* in the associated computation exit status register. If the computation is successful, that is, if the number of errors detected does not exceed the maximum value authorized for the chosen correction capability, the exit status register contains the information on the number of detected errors.

When the error-location process completes, an interrupt is triggered to inform the central processing unit (CPU) that its status can be checked. The number of detected errors and their locations in the NAND block can be retrieved from the module through register accesses.

15.5.1.1 ELM Features

The ELM has the following features:

- 4, 8, and 16 bits per 512-byte block error-location based on BCH algorithms
- Eight simultaneous processing contexts
- Page-based and continuous modes
- Interrupt generation on error-location process completion:
  - When the full page has been processed in page mode
  - For each syndrome polynomial in continuous mode

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15.5.2 ELM Integration

The ELM extracts error addresses from generated syndrome polynomials.

The ELM is used with the GPMC. Syndrome polynomials generated on-the-fly when reading a NAND flash page and stored in GPMC registers are passed to the ELM. The microprocessor unit (MPU) can then correct the data block by flipping the bits to which the ELM error-location outputs point.

Figure 15-100 shows the integration of the ELM subsystem in the device.

Figure 15-100. ELM Integration

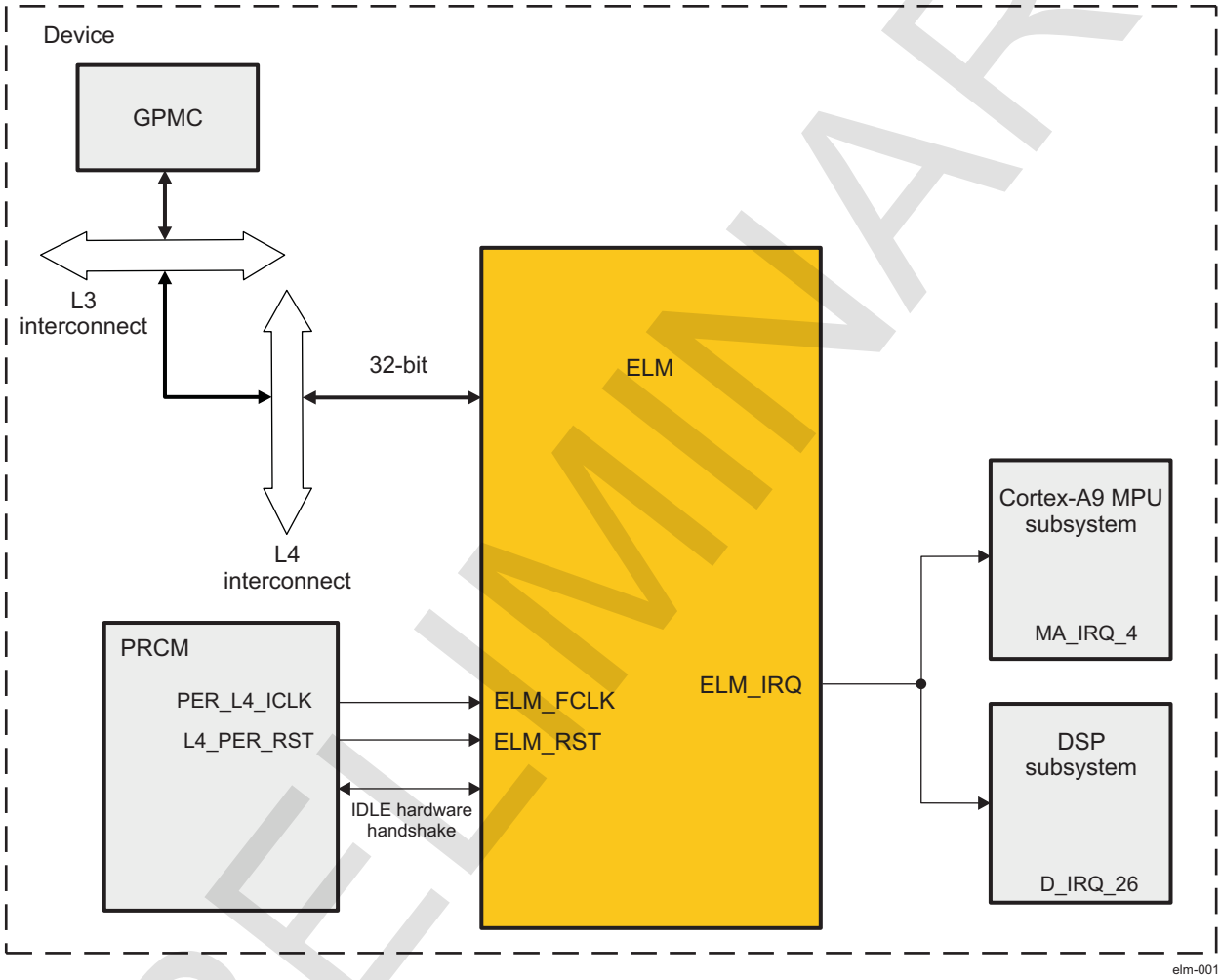

Table 15-345. Integration Attributes

Module Instance	Attributes		
	Power Domain	Wake-Up Capability	Interconnect
ELM	PD_L4_PER	No	NA

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Table 15-346. Clocks and Resets

Clocks				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
ELM	ELM_FCLK	PER_L4_ICLK	PRCM	Functional clock For information about PRCM clock gating and management, see Section 3.6.8, *CD_L4_PER Clock Domain* in Chapter 3, *Power, Reset, and Clock Management*.
Resets				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
ELM	ELM_RST	L4_PER_RST	PRCM	Power domain hardware reset For information about PRCM reset sources and distribution, see Section 3.5.4, *Reset Domains* inChapter 3, *Power, Reset, and Clock Management*.

Table 15-347. Hardware Requests

Interrupt Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
ELM	ELM_IRQ	MA_IRQ_4	Cortex-A9	BCH error-location module interrupt For information about Cortex-A9 interrupt control, see Section 17.3.2, *Interrupt Requests to Cortex-A9 MPU INTC*.
		D_IRQ_26	DSP	BCH error-location module interrupt For information about DSP interrupt control, see , *Interrupts Requests*.

15.5.3 ELM Functional Description

The ELM is designed around the error-location engine, which handles the computation based on the input syndrome polynomials.

The ELM maps the error-location engine to a standard interconnect interface by using a set of registers to control inputs and outputs.

15.5.3.1 ELM Software Reset

To perform a software reset, write a 1 to the ELM_SYSCONFIG[1] SOFTRESET bit. The ELM_SYSSTATUS[0] RESETDONE bit indicates that the software reset is complete when its value is 1. When the software reset completes, the ELM_SYSCONFIG[1] SOFTRESET bit is automatically reset.

15.5.3.2 ELM Power Management

Table 15-348 describes the power-management features available to the ELM module.

NOTE:

- For information about source clock gating and sleep/wake-up transitions description, see the Section 3.6.8, *CD_L4_PER Clock Domain* in Chapter 3, *Power, Reset, and Clock Management*.
- For a general description of EnaWakeUp, IdleMode, ClockActivity, and StandbyMode features, see Section 3.6 *Clock Management* in Chapter 3, *Power, Reset, and Clock Management*

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Table 15-348. Local Power Management Features

Feature	Registers	Description
Clock autogating	ELM_SYSCONFIG[0] AUTOGATING bit	This bit allows a local power optimization inside the module by gating the ELM_FCLK clock upon the interface activity.
Slave idle modes	ELM_SYSCONFIG[4:3] SIDLEMODE bit field	Force-idle, No-idle, and Smart-idle modes are available.
Clock activity	ELM_SYSCONFIG[8] CLOCKACTIVITY bit	The clock can be switched-off or maintained during the wake-up period.
Master Standby modes	N/A	
Global Wake-up Enable	N/A	
Wake-up Sources Enable	N/A	

CAUTION

The PRCM module has no hardware means of reading CLOCKACTIVITY settings. Thus, software must ensure consistent programming between the ELM CLOCKACTIVITY and ELM clock PRCM control bits. For a description of the ClockActivity feature, see Chapter 3, *Power, Reset, and Clock Management*.

15.5.3.3 ELM Interrupt Requests

Table 15-349 lists the event flags, and their masks, that can cause module interrupts.

Table 15-349. Events

Event Flag	Event Mask	Map to	Description
ELM_IRQSTATUS[8] PAGE_VALID	ELM_IRQENABLE[8] PAGE_MASK	ELM_IRQ	Page interrupt
ELM_IRQSTATUS[7] LOC_VALID_7	ELM_IRQENABLE[7] LOCATION_MASK_7	ELM_IRQ	Error-location interrupt for syndrome polynomial 7
ELM_IRQSTATUS[6] LOC_VALID_6	ELM_IRQENABLE[6] LOCATION_MASK_6	ELM_IRQ	Error-location interrupt for syndrome polynomial 6
ELM_IRQSTATUS[5] LOC_VALID_5	ELM_IRQENABLE[5] LOCATION_MASK_5	ELM_IRQ	Error-location interrupt for syndrome polynomial 5
ELM_IRQSTATUS[4] LOC_VALID_4	ELM_IRQENABLE[4] LOCATION_MASK_4	ELM_IRQ	Error-location interrupt for syndrome polynomial 4
ELM_IRQSTATUS[3] LOC_VALID_3	ELM_IRQENABLE[3] LOCATION_MASK_3	ELM_IRQ	Error-location interrupt for syndrome polynomial 3
ELM_IRQSTATUS[2] LOC_VALID_2	ELM_IRQENABLE[2] LOCATION_MASK_2	ELM_IRQ	Error-location interrupt for syndrome polynomial 2
ELM_IRQSTATUS[1] LOC_VALID_1	ELM_IRQENABLE[1] LOCATION_MASK_1	ELM_IRQ	Error-location interrupt for syndrome polynomial 1
ELM_IRQSTATUS[0] LOC_VALID_0	ELM_IRQENABLE[0] LOCATION_MASK_0	ELM_IRQ	Error-location interrupt for syndrome polynomial 0

15.5.3.4 Processing Initialization

ELM_LOCATION_CONFIG global setting parameters must be set before using the error-location engine. The ELM_LOCATION_CONFIG[1:0] ECC_BCH_LEVEL bit defines the error-correction level used (4-,8-, or 16-bit error-correction). The ELM_LOCATION_CONFIG[26:16] ECC_SIZE bit field defines the maximum buffer length beyond which the engine processing no longer looks for errors.

The CPU can choose to use the ELM in continuous mode or page mode. If all ELM_PAGE_CTRL[i] SECTOR_i bits are reset (i is the syndrome polynomial number, i = 0 to 7), continuous mode is used. In any other case, page mode is implicitly selected.

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- Continuous mode: Each syndrome polynomial is processed independently – results for a syndrome can be retrieved and acknowledged at any time, whatever the status of the other seven processing contexts.
- Page mode: Syndrome polynomials are grouped into atomic entities – only one page can be processed at any given time, even if all eight contexts are not used for this page. Unused contexts are lost and cannot be affected to any other processing. The full page must be acknowledged and cleared before moving to the next page.

For completion interrupts to be generated correctly, all ELM_IRQENABLE[i] LOCATION_MASK_i bits (i = 0 to 7) must be forced to 0 when in page mode, and set to 1 in continuous mode. Additionally, the ELM_IRQENABLE[8] PAGE_MASK bit must be set to 1 when in page mode.

The CPU initiates error-location processing by writing a syndrome polynomial into one of the eight possible register sets. Each of these register sets includes seven registers: ELM_SYNDROME_FRAGMENT_0_i to ELM_SYNDROME_FRAGMENT_6_i. The first six registers can be written in any order, but ELM_SYNDROME_FRAGMENT_6_i must be written last because it includes the validity bit, which instructs the ELM that this syndrome polynomial must be processed (the ELM_SYNDROME_FRAGMENT_6_i[16] SYNDROME_VALID bit).

As soon as one validity bit is asserted (ELM_SYNDROME_FRAGMENT_6_i[16] SYNDROME_VALID = 0x1, with i = 0 to 7), error-location processing can start for the corresponding syndrome polynomial. The associated ELM_LOCATION_STATUS_i and ELM_ERROR_LOCATION_0_i to ELM_ERROR_LOCATION_15_i registers are not reset (i = 0 to 7). The software must not consider them until the corresponding ELM_IRQSTATUS[i] LOC_VALID_i bit is set.

15.5.3.5 Processing Sequence

While the error-location engine is busy processing one syndrome polynomial, further syndrome polynomials can be written. They are processed when the current processing completes.

The engine completes early when:

- No error is detected; that is, when the ELM_LOCATION_STATUS_i[8] ECC_CORRECTABLE bit is set to 1 and the ELM_LOCATION_STATUS_i[4:0] ECC_NB_ERRORS bit field is set to 0x0.
- Too many errors are detected; that is, when the ELM_LOCATION_STATUS_i[8] ECC_CORRECTABLE bit is set to 0 while the ELM_LOCATION_STATUS_i[4:0] ECC_NB_ERRORS bit field is set with the value output by the error-location engine. The reported number of errors is not ensured if ECC_CORRECTABLE is 0.

If the engine completes early, the associated error-location registers ELM_ERROR_LOCATION_0_i to ELM_ERROR_LOCATION_15_i are not updated (i = 0 to 7).

In all other cases, the engine goes through the entire error-location process. Each time an error-location is found, it is logged in the associated ECC_ERROR_LOCATION bit field. The first error detected is logged in the ELM_ERROR_LOCATION_0_i[12:0] ECC_ERROR_LOCATION bit field; the second in the ELM_ERROR_LOCATION_1_i[12:0] ECC_ERROR_LOCATION bit field, and so on.

Table 15-350. ELM_LOCATION_STATUS_i Value Decoding Table

ECC_CORRECTABLE Value	ECC_NB_ERRORS Value	Status	Number of Errors Detected	Action Required
1	0	OK	0	None
1	≠ 0	OK	ECC_NB_ERRORS	Correct the data buffer read based on the ELM_ERROR_LOCATION_0_i to ELM_ERROR_LOCATION_15_i results.
0	Any	Failed	Unknown	Software-dependant

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15.5.3.6 Processing Completion

When the processing for a given syndrome polynomial completes, its ELM_SYNDROME_FRAGMENT_6_i[16] SYNDROME_VALID bit is reset. It must not be set again until the exit status registers, ELM_LOCATION_STATUS_i (i = 0 to 7), for this processing are checked. Failure to comply with this rule leads to potential loss of the first polynomial process data output.

The error-location engine signals the process completion to the ELM. When this event is detected, the corresponding ELM_IRQSTATUS[i] LOC_VALID_i bit is set (i = 0 to 7). The processing-exit status is available from the associated ELM_LOCATION_STATUS_i register, and error locations are stored in order in the ECC_ERROR_LOCATION fields. The software must only read valid error-location registers based on the number of errors detected and located.

Immediately after the error-location engine completes, a new syndrome polynomial can be processed, if any is available, as reported by the ELM_SYNDROME_FRAGMENT_6_i[16] SYNDROME_VALID validity bit, depending on the configured error-correction level. If several syndrome polynomials are available, a round-robin arbitration is used to select one for processing.

In continuous mode (that is, all bits in ELM_PAGE_CTRL are reset), an interrupt is triggered whenever a ELM_IRQSTATUS[i] LOC_VALID_i bit is asserted. The CPU must read the ELM_IRQSTATUS register to determine which polynomial is processed and retrieve the exit status and error locations (ELM_LOCATION_STATUS_i and ELM_ERROR_LOCATION_0_i to ELM_ERROR_LOCATION_15_i). When done, the CPU must clear the corresponding ELM_IRQSTATUS[i] LOC_VALID_i bit by writing it to 1. Other status bits must be written to 0 so that other interrupts are not unintentionally cleared. When using this mode, the ELM_IRQSTATUS[8] PAGE_VALID interrupt is never triggered.

In page mode, the module does not trigger interrupts for the processing completion of each polynomial because the ELM_IRQENABLE[i] LOCATION_MASK_i bits are cleared. A page is defined using the ELM_PAGE_CTRL register. Each SECTOR_i bit set means the corresponding polynomial i is part of the page processing. A page is fully processed when all tagged polynomials have been processed, as logged in the ELM_IRQSTATUS[i] LOC_VALID_i bit fields. The module triggers an ELM_IRQSTATUS[8] PAGE_VALID interrupt whenever it detects that the full page has been processed. To make sure the next page can be correctly processed, all status bits in the ELM_IRQSTATUS register must be cleared by using a single atomic-write access.

NOTE: Do not modify page setting parameters in the ELM_PAGE_CTRL register unless the engine is idle, no polynomial input is valid, and all interrupts have been cleared.

Because no polynomial-level interrupt is triggered in page mode, polynomials cleared in the ELM_PAGE_CTRL[i] SECTOR_i bit fields (i = 0 to 7) are processed as usual, but are essentially ignored. The CPU must manually poll the ELM_IRQSTATUS bits to check for their status.

15.5.4 ELM Basic Programming Model

15.5.4.1 ELM Low Level Programming Model

15.5.4.1.1 Processing Initialization

Table 15-351. ELM Processing Initialization

Step	Register/ Bit Field / Programming Model	Value
Resets the module	ELM_SYSCONFIG[1] SOFTRESET	0x1
Wait until reset is done.	ELM_SYSSTATUS[0] RESETDONE	0x1
Configure the slave interface power management.	ELM_SYSCONFIG[4:3] SIDLEMODE	Set value
Defines the error-correction level used	ELM_LOCATION_CONFIG[1:0] ECC_BCH_LEVEL	Set value
Defines the maximum buffer length	ELM_LOCATION_CONFIG[26:16] ECC_SIZE	Set value
Sets the ELM in continuous mode or page mode	ELM_PAGE_CTRL	Set value
If continuous mode is used	All ELM_PAGE_CTRL[i] SECTOR_i (i = 0 to 7)	0x0
Enables interrupt for syndrome polynomial i	ELM_IRQENABLE[i] LOCATION_MASK_i	0x1

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Table 15-351. ELM Processing Initialization (continued)

Step	Register/ Bit Field / Programming Model	Value
else (page mode is used)	One syndrome polynomial i is set ELM_PAGE_CTRL[i] SECTOR_i (i = 0 to 7)	0x1
Disable all interrupts for syndrome polynomial and enable PAGE_MASK interrupt.	All ELM_IRQENABLE[i] LOCATION_MASK_i = 0x0 and ELM_IRQENABLE[8] PAGE_MASK = 0x1	Set value
endif		Set value
Set the input syndrome polynomial i.	ELM_SYNDROME_FRAGMENT_0_i	Set value
	ELM_SYNDROME_FRAGMENT_1_i	Set value
	ELM_SYNDROME_FRAGMENT_5_i	Set value
	ELM_SYNDROME_FRAGMENT_6_i	Set value
Initiates the computation process	ELM_SYNDROME_FRAGMENT_6_i[16] SYNDROME_VALID	0x1

15.5.4.1.2 Read Results

The engine goes through the entire error-location process and results can be read. Table 15-352 and Table 15-353 describe the processing completion for continuous and page modes, respectively.

Table 15-352. ELM Processing Completion for Continuous Mode

Step	Register/ Bit Field / Programming Model	Value
Wait until process is complete for syndrome polynomial i: Wait until the ELM_IRQ interrupt is generated, or poll the status register.		
Read for which i the error-location process is complete.	ELM_IRQSTATUS[i] LOC_VALID_i	0x1
if the process fails (too many errors)	ELM_LOCATION_STATUS_i[8] ECC_CORRECTABLE	0x0
It is software dependant.		
else (process successful, the engine completes)	ELM_LOCATION_STATUS_i[8] ECC_CORRECTABLE	0x1
Read the number of errors.	ELM_LOCATION_STATUS_i[4:0] ECC_NB_ERRORS	
Read the error-location bit addresses for syndrome polynomial i of the ECC_NB_ERRORS first registers. It is the software responsibility to correct errors in the data buffer.	ELM_ERROR_LOCATION_0_i[12:0] ECC_ERROR_LOCATION	
	ELM_ERROR_LOCATION_1_i[12:0] ECC_ERROR_LOCATION	
	...	
	ELM_ERROR_LOCATION_15_i[12:0] ECC_ERROR_LOCATION	
endif		
Clear the corresponding i interrupt.	ELM_IRQSTATUS[i] LOC_VALID_i	0x1

A new syndrome polynomial can be processed after the end of processing (ELM_SYNDROME_FRAGMENT_6_i[16] SYNDROME_VALID = 0x0) and after the exit status register check (ELM_LOCATION_STATUS_i).

Table 15-353. ELM Processing Completion for Page Mode

Step	Register/ Bit Field / Programming Model	Value
Wait until process is complete for syndrome polynomial i: Wait until the ELM_IRQ interrupt is generated, or poll the status register.		
Wait for page completed interrupt: All error locations are valid.	ELM_IRQSTATUS[8] PAGE_VALID	0x1
Repeat the following actions the necessary number of times. That is, once for each valid defined block in the page.		

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Table 15-353. ELM Processing Completion for Page Mode (continued)

Step	Register/ Bit Field / Programming Model	Value
Read the process exit status.	ELM_LOCATION_STATUS_i[8] ECC_CORRECTABLE	
if the process fails (too many errors)	ELM_LOCATION_STATUS_i[8] ECC_CORRECTABLE	0x0
It is software dependant.		
else (process successful, the engine completes)	ELM_LOCATION_STATUS_i[8] ECC_CORRECTABLE	0x1
Read the number of errors.	ELM_LOCATION_STATUS_i[4:0] ECC_NB_ERRORS	
Read the error-location bit addresses for syndrome polynomial i of the ECC_NB_ERRORS first registers.	ELM_ERROR_LOCATION_0_i[12:0] ECC_ERROR_LOCATION	
	ELM_ERROR_LOCATION_1_i[12:0] ECC_ERROR_LOCATION	
	...	
	ELM_ERROR_LOCATION_15_i[12:0] ECC_ERROR_LOCATION	
endif		
End Repeat		
Clear the ELM_IRQSTATUS register.	ELM_IRQSTATUS	0x1FF

Next page can be correctly processed after a page is fully processed, when all tagged polynomials have been processed (ELM_IRQSTATUS[i] LOC_VALID_i = 0x1 for all syndrome polynomials i used in the page).

15.5.4.2 Use Case: ELM Used in Continuous Mode

In this example, the ELM module is programmed for an 8-bit error-correction capability in continuous mode. After reading a 528-byte NAND flash sector (512B data plus 16B spare area) with a 16-bit interface, a non-zero polynomial syndrome is reported from the GPMC (Polynomial syndrome 0 is used in the ELM):

- P = 0x0A16ABE115E44F767BFB0D0980

Table 15-354. Use Case: Continuous Mode

Step	Register/ Bit Field / Programming Model	Value
Resets the module	ELM_SYSCONFIG[1] SOFTRESET	0x1
Wait until reset is done.	ELM_SYSSTATUS[0] RESETDONE	0x1
Configure the slave interface power management: Smart idle is used.	ELM_SYSCONFIG[4:3] SIDLEMODE	0x2
Defines the error-correction level used: 8 bits	ELM_LOCATION_CONFIG[1:0] ECC_BCH_LEVEL	0x1
Defines the maximum buffer length: 528 bytes (2x528 = 1056)	ELM_LOCATION_CONFIG[26:16] ECC_SIZE	0x420
Sets the ELM in continuous mode	ELM_PAGE_CTRL	0
Enables interrupt for syndrome polynomial 0	ELM_IRQENABLE[0] LOCATION_MASK_0	0x1
Set the input syndrome polynomial 0.	ELM_SYNDROME_FRAGMENT_0_i (i=0)	0xFB0D0980
	ELM_SYNDROME_FRAGMENT_1_i (i=0)	0xE44F767B
	ELM_SYNDROME_FRAGMENT_2_i (i=0)	0x16ABE115
	ELM_SYNDROME_FRAGMENT_3_i (i=0)	0x0000000A
Initiates the computation process	ELM_SYNDROME_FRAGMENT_6_i[16] SYNDROME_VALID (i=0)	0x1
Wait until process is complete for syndrome polynomial 0: IRQ_ELM is generated or poll the status register.		
Read that error-location process is complete for syndrome polynomial 0.	ELM_IRQSTATUS[0] LOC_VALID_0	0x1
Read the process exit status: All errors were successfully located.	ELM_LOCATION_STATUS_i[8] ECC_CORRECTABLE (i=0)	0x1

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Table 15-354. Use Case: Continuous Mode (continued)

Step	Register/ Bit Field / Programming Model	Value
Read the number of errors: Four errors detected.	ELM_LOCATION_STATUS_i[4:0] ECC_NB_ERRORS (i=0)	0x4
Read the error-location bit addresses for syndrome polynomial 0 of the 4 first registers: Errors are located in the data buffer at decimal addresses 431, 1062, 1909, 3452.	ELM_ERROR_LOCATION_0_i (i=0)	0x1AF
	ELM_ERROR_LOCATION_1_i (i=0)	0x426
	ELM_ERROR_LOCATION_2_i (i=0)	0x775
	ELM_ERROR_LOCATION_3_i (i=0)	0xD7C
Clear the corresponding interrupt for polynomial 0.	ELM_IRQSTATUS[0] LOC_VALID_0	0x1

The NAND flash data in the sector are seen as a polynomial of degree 4223 (number of bits in a 528 byte buffer minus 1), with each data bit being a coefficient in the polynomial. When reading from a NAND flash using the GPMC module, computation of the polynomial syndrome assumes that the first NAND word read at address 0x0 contains the highest-order coefficient in the message. Furthermore, in the 16-bit NAND word, bits are ordered from bit 7 to bit 0, then from bit 15 to bit 8. Based on this convention, an address table of the data buffer can be built. NAND memory addresses in Table 15-355 are given in decimal format.

Table 15-355. 16-bit NAND Sector Buffer Address Map

NAND Memory Address	Message bit addresses in the memory word															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	4215	4214	4213	4212	4211	4210	4209	4208	4223	4222	4221	4220	4219	4218	4217	4216
1	4175	4174	4173	4172	4171	4170	4169	4168	4183	4182	4181	4180	4179	4178	4177	4176
...																
47	3463	3462	3461	3460	3459	3458	3457	3456	3471	3470	3469	3468	3467	3466	3465	3464
48	3447	3446	3445	3444	3443	3442	3441	3440	3455	3454	3453	3452	3451	3450	3449	3448
49	3431	3430	3429	3428	3427	3426	3425	3424	3439	3438	3437	3436	3435	3434	3433	3432
50	3415	3414	3413	3412	3411	3410	3409	3408	3423	3422	3421	3420	3419	3418	3417	3416
...																
255	135	134	133	132	131	130	129	128	143	142	141	140	139	138	137	136
256	119	118	117	116	115	114	113	112	127	126	125	124	123	122	121	120
257	103	102	101	100	99	98	97	96	111	110	109	108	107	106	105	104
258	87	86	85	84	83	82	81	80	95	94	93	92	91	90	89	88
259	71	70	69	68	67	66	65	64	79	78	77	76	75	74	73	72
260	55	54	53	52	51	50	49	48	63	62	61	60	59	58	57	56
261	39	38	37	36	35	34	33	32	47	46	45	44	43	42	41	40
262	23	22	21	20	19	18	17	16	31	30	29	28	27	26	25	24
263	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8

The table can now be used to determine which bits in the buffer were incorrect and must be flipped. In this example, the first bit to be flipped is bit 4 from the 49th byte read from memory. It is up to the processor to correctly map this word to the copied buffer and to flip this bit. The same process must be repeated for all detected errors.

15.5.4.3 Use Case: ELM Used in Page Mode

In this example, the ELM module is programmed for an 16-bit error-correction capability in page mode. After reading a 528-byte NAND flash sector (512B data plus 16B spare area) with a 16-bit interface, four non-zero polynomial syndromes are reported from the GPMC (Polynomial syndrome 0, 1, 2, and 3 are used in the ELM):

- P0 = 0xE8B0 12ADDB5A318E05BE B0693DB28330B5CC A329AA05E0B718EF
- P1 = 0xBAD0 49A0D932C22E6669 0948DF08BE093336 79C6BA10E5F935EB

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- P2 = 0x69D9 B86ABCD5EC3697FA A6498FEE54556EA0 1579EF7D60BA3189
- P3 = 0x0

Table 15-356. Use Case: Page Mode

Step	Register/ Bit Field / Programming Model	Value
Resets the module	ELM_SYSCONFIG[1] SOFTRESET	0x1
Wait until reset is done.	ELM_SYSSTATUS[0] RESETDONE	0x1
Configure the slave interface power management: Smart idle is used.	ELM_SYSCONFIG[4:3] SIDLEMODE	0x2
Defines the error-correction level used: 16 bits	ELM_LOCATION_CONFIG[1:0] ECC_BCH_LEVEL	0x2
Defines the maximum buffer length: 528 bytes	ELM_LOCATION_CONFIG[26:16] ECC_SIZE	0x420
Sets the ELM in page mode (4 blocks in a page)	ELM_PAGE_CTRL[0] SECTOR_0	0x1
	ELM_PAGE_CTRL[1] SECTOR_1	0x1
	ELM_PAGE_CTRL[2] SECTOR_2	0x1
	ELM_PAGE_CTRL[3] SECTOR_3	0x1
Disable all interrupts for syndrome polynomial and enable PAGE_MASK interrupt.	ELM_IRQENABLE	0x100
Set the input syndrome polynomial 0.	ELM_SYNDROME_FRAGMENT_0_i (i=0)	0xE0B718EF
	ELM_SYNDROME_FRAGMENT_1_i (i=0)	0xA329AA05
	ELM_SYNDROME_FRAGMENT_2_i (i=0)	0x8330B5CC
	ELM_SYNDROME_FRAGMENT_3_i (i=0)	0xB0693DB2
	ELM_SYNDROME_FRAGMENT_4_i (i=0)	0x318E05BE
	ELM_SYNDROME_FRAGMENT_5_i (i=0)	0x12ADDB5A
	ELM_SYNDROME_FRAGMENT_6_i (i=0)	0xE8B0
Set the input syndrome polynomial 1.	ELM_SYNDROME_FRAGMENT_0_i (i=1)	0xE5F935EB
	ELM_SYNDROME_FRAGMENT_1_i (i=1)	0x79C6BA10
	ELM_SYNDROME_FRAGMENT_2_i (i=1)	0xBE093336
	ELM_SYNDROME_FRAGMENT_3_i (i=1)	0x0948DF08
	ELM_SYNDROME_FRAGMENT_4_i (i=1)	0xC22E6669
	ELM_SYNDROME_FRAGMENT_5_i (i=1)	0x49A0D932
	ELM_SYNDROME_FRAGMENT_6_i (i=1)	0xBAD0
Set the input syndrome polynomial 2.	ELM_SYNDROME_FRAGMENT_0_i (i=2)	0x60BA3189
	ELM_SYNDROME_FRAGMENT_1_i (i=2)	0x1579EF7D
	ELM_SYNDROME_FRAGMENT_2_i (i=2)	0x54556EA0
	ELM_SYNDROME_FRAGMENT_3_i (i=2)	0xA6498FEE
	ELM_SYNDROME_FRAGMENT_4_i (i=2)	0xEC3697FA
	ELM_SYNDROME_FRAGMENT_5_i (i=2)	0xB86ABCD5
	ELM_SYNDROME_FRAGMENT_6_i (i=2)	0x69D9
Set the input syndrome polynomial 3.	ELM_SYNDROME_FRAGMENT_0_i (i=3)	0x0
	ELM_SYNDROME_FRAGMENT_1_i (i=3)	0x0
	ELM_SYNDROME_FRAGMENT_2_i (i=3)	0x0
	ELM_SYNDROME_FRAGMENT_3_i (i=3)	0x0
	ELM_SYNDROME_FRAGMENT_4_i (i=3)	0x0
	ELM_SYNDROME_FRAGMENT_5_i (i=3)	0x0
	ELM_SYNDROME_FRAGMENT_6_i (i=3)	0x0
Initiates the computation process for syndrome polynomial 0	ELM_SYNDROME_FRAGMENT_6_i[16] SYNDROME_VALID (i=0)	0x1
Initiates the computation process for syndrome polynomial 1	ELM_SYNDROME_FRAGMENT_6_i[16] SYNDROME_VALID (i=1)	0x1
Initiates the computation process for syndrome polynomial 2	ELM_SYNDROME_FRAGMENT_6_i[16] SYNDROME_VALID (i=2)	0x1

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Table 15-356. Use Case: Page Mode (continued)

Step	Register/ Bit Field / Programming Model	Value
Initiates the computation process for syndrome polynomial 3	ELM_SYNDROME_FRAGMENT_6_i[16] SYNDROME_VALID (i=3)	0x1
Wait until process is complete for syndrome polynomial 0, 1, 2, and 3: Wait until the ELM_IRQ interrupt is generated or poll the status register.		
Wait for page completed interrupt: All error locations are valid.	ELM_IRQSTATUS[8] PAGE_VALID	0x1
Read the process exit status for syndrome polynomial 0: All errors were successfully located.	ELM_LOCATION_STATUS_i[8] ECC_CORRECTABLE (i=0)	0x1
Read the process exit status for syndrome polynomial 1: All errors were successfully located.	ELM_LOCATION_STATUS_i[8] ECC_CORRECTABLE (i=1)	0x1
Read the process exit status for syndrome polynomial 2: All errors were successfully located.	ELM_LOCATION_STATUS_i[8] ECC_CORRECTABLE (i=2)	0x1
Read the process exit status for syndrome polynomial 3: All errors were successfully located.	ELM_LOCATION_STATUS_i[8] ECC_CORRECTABLE (i=3)	0x1
Read the number of errors for syndrome polynomial 0: 4 errors detected.	ELM_LOCATION_STATUS_i[4:0] ECC_NB_ERRORS (i=0)	0x4
Read the number of errors for syndrome polynomial 1: 2 errors detected.	ELM_LOCATION_STATUS_i[4:0] ECC_NB_ERRORS (i=1)	0x2
Read the number of errors for syndrome polynomial 2: 1 error detected.	ELM_LOCATION_STATUS_i[4:0] ECC_NB_ERRORS (i=2)	0x1
Read the number of errors for syndrome polynomial 3: 0 errors detected.	ELM_LOCATION_STATUS_i[4:0] ECC_NB_ERRORS (i=3)	0x0
Read the error-location bit addresses for syndrome polynomial 0 of the 4 first registers:	ELM_ERROR_LOCATION_0_i (i=0)	0x1FE
	ELM_ERROR_LOCATION_1_i (i=0)	0x617
	ELM_ERROR_LOCATION_2_i (i=0)	0x650
	ELM_ERROR_LOCATION_3_i (i=0)	0xA83
Read the error-location bit addresses for syndrome polynomial 1 of the 2 first registers:	ELM_ERROR_LOCATION_0_i (i=1)	0x4
	ELM_ERROR_LOCATION_1_i (i=1)	0x1036
Read the errors location bit addresses for syndrome polynomial 2 of the first registers:	ELM_ERROR_LOCATION_0_i (i=1)	0x3E8
Clear the ELM_IRQSTATUS register.	ELM_IRQSTATUS	0x1FF

15.5.5 ELM Register Manual

15.5.5.1 ELM Instance Summary

Table 15-357. ELM Instance Summary

Module Name	Base Address	Size
ELM	0x4807 8000	4KB

15.5.5.2 ELM Registers

15.5.5.2.1 ELM Register Summary

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Table 15-358. ELM Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	ELM L3 Physical Address
ELM_REVISION	R	32	0x0000 0000	0x4807 8000
ELM_SYSCONFIG	RW	32	0x0000 0010	0x4807 8010
ELM_SYSSTATUS	R	32	0x0000 0014	0x4807 8014
ELM_IRQSTATUS	RW	32	0x0000 0018	0x4807 8018
ELM_IRQENABLE	RW	32	0x0000 001C	0x4807 801C
ELM_LOCATION_CONFIG	RW	32	0x0000 0020	0x4807 8020
ELM_PAGE_CTRL	RW	32	0x0000 0080	0x4807 8080
ELM_SYNDROME_FRAGMENT_0_i (1)	RW	32	0x0000 0400 + (0x40 * i)	0x4807 8400 + (0x40 * i)
ELM_SYNDROME_FRAGMENT_1_i (1)	RW	32	0x0000 0404 + (0x40 * i)	0x4807 8404 + (0x40 * i)
ELM_SYNDROME_FRAGMENT_2_i (1)	RW	32	0x0000 0408 + (0x40 * i)	0x4807 8408 + (0x40 * i)
ELM_SYNDROME_FRAGMENT_3_i (1)	RW	32	0x0000 040C + (0x40 * i)	0x4807 840C + (0x40 * i)
ELM_SYNDROME_FRAGMENT_4_i (1)	RW	32	0x0000 0410 + (0x40 * i)	0x4807 8410 + (0x40 * i)
ELM_SYNDROME_FRAGMENT_5_i (1)	RW	32	0x0000 0414 + (0x40 * i)	0x4807 8414 + (0x40 * i)
ELM_SYNDROME_FRAGMENT_6_i (1)	RW	32	0x0000 0418 + (0x40 * i)	0x4807 8418 + (0x40 * i)
ELM_LOCATION_STATUS_i (1)	R	32	0x0000 0800 + (0x100 * i)	0x4807 8800 + (0x100 * i)
ELM_ERROR_LOCATION_0_i (1)	R	32	0x0000 0880 + (0x100 * i)	0x4807 8880 + (0x100 * i)
ELM_ERROR_LOCATION_1_i (1)	R	32	0x0000 0884 + (0x100 * i)	0x4807 8884 + (0x100 * i)
ELM_ERROR_LOCATION_2_i (1)	R	32	0x0000 0888 + (0x100 * i)	0x4807 8888 + (0x100 * i)
ELM_ERROR_LOCATION_3_i (1)	R	32	0x0000 088C + (0x100 * i)	0x4807 888C + (0x100 * i)
ELM_ERROR_LOCATION_4_i (1)	R	32	0x0000 0890 + (0x100 * i)	0x4807 8890 + (0x100 * i)
ELM_ERROR_LOCATION_5_i (1)	R	32	0x0000 0894 + (0x100 * i)	0x4807 8894 + (0x100 * i)
ELM_ERROR_LOCATION_6_i (1)	R	32	0x0000 0898 + (0x100 * i)	0x4807 8898 + (0x100 * i)
ELM_ERROR_LOCATION_7_i (1)	R	32	0x0000 089C + (0x100 * i)	0x4807 889C + (0x100 * i)
ELM_ERROR_LOCATION_8_i (1)	R	32	0x0000 08A0 + (0x100 * i)	0x4807 88A0 + (0x100 * i)
ELM_ERROR_LOCATION_9_i (1)	R	32	0x0000 08A4 + (0x100 * i)	0x4807 88A4 + (0x100 * i)
ELM_ERROR_LOCATION_10_i (1)	R	32	0x0000 08A8 + (0x100 * i)	0x4807 88A8 + (0x100 * i)
ELM_ERROR_LOCATION_11_i (1)	R	32	0x0000 08AC + (0x100 * i)	0x4807 88AC + (0x100 * i)
ELM_ERROR_LOCATION_12_i (1)	R	32	0x0000 08B0 + (0x100 * i)	0x4807 88B0 + (0x100 * i)
ELM_ERROR_LOCATION_13_i (1)	R	32	0x0000 08B4 + (0x100 * i)	0x4807 88B4 + (0x100 * i)
ELM_ERROR_LOCATION_14_i (1)	R	32	0x0000 08B8 + (0x100 * i)	0x4807 88B8 + (0x100 * i)
ELM_ERROR_LOCATION_15_i (1)	R	32	0x0000 08BC + (0x100 * i)	0x4807 88BC + (0x100 * i)

(1) i = 0 to 7 for ELM

15.5.5.2.2 ELM Register Description

Table 15-359. ELM_REVISION

Address Offset	0x0000 0000		
Physical Address	0x4807 8000	**Instance**	ELM
Description	This register contains the IP revision code. (A write or reset of to this register has no effect.)		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

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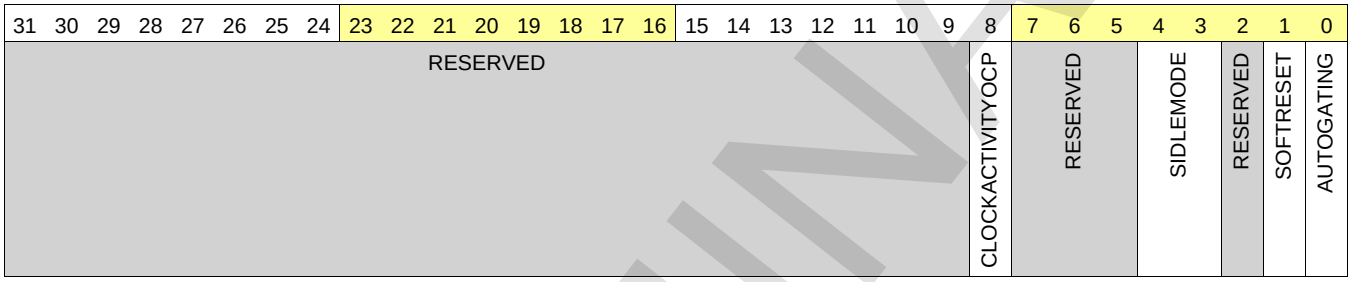
Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP Revision	R	TI internal data

Table 15-360. Register Call Summary for Register ELM_REVISION

Error Location Module
- ELM Register Summary: [0]

Table 15-361. ELM_SYSCONFIG

Address Offset	0x0000 0010		
Physical Address	0x4807 8010	**Instance**	ELM
Description	This register allows controlling various parameters of the OCP interface.		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:9	RESERVED	Reserved	R	0x000000
8	CLOCKACTIVITYOCP	OCP Clock activity when module is in IDLE mode (during wake up mode period) 0x0: OCP Clock can be switch-off 0x1: OCP Clock is maintained during wake up period	RW	0
7:5	RESERVED	Reserved	R	0x0
4:3	SIDLEMODE	Slave interface power management (IDLE req/ack control) 0x0: FORCE Idle. IDLE request is acknowledged unconditionally and immediately (Default *Dumb* mode for safety) 0x1: NO idle. IDLE request is never acknowledged. 0x2: SMART Idle. The acknowledgment to an IDLE request is given based on the internal activity. 0x3: Reserved - do not use	RW	0x2
2	RESERVED	Reserved	R	0
1	SOFTRESET	Module software reset This bit is automatically reset by hardware (During reads, it always returns 0.) It has same effect as the OCP hardware reset. 0x0: Normal mode 0x1: Start soft reset sequence.	RW	0
0	AUTOGATING	Internal OCP clock gating strategy (no module visible impact other than saving power) 0x0: OCP clock is free-running 0x1: Automatic internal OCP clock gating strategy is applied based on the OCP interface activity.	RW	1

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Table 15-362. Register Call Summary for Register ELM_SYSCONFIG

Error Location Module

- ELM Software Reset: [0] [1]
- ELM Power Management: [2] [3] [4]
- Processing Initialization: [5] [6]
- Use Case: ELM Used in Continuous Mode: [7] [8]
- Use Case: ELM Used in Page Mode: [9] [10]
- ELM Register Summary: [11]

Table 15-363. ELM_SYSSTATUS

Address Offset	0x0000 0014		
Physical Address	0x4807 8014	**Instance**	ELM
Description	Internal reset monitoring (OCP domain) Undefined since: From hardware perspective, the reset state is 0. From software user perspective, when the accessible module is 1.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															RESETDONE

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	RESETDONE	Internal reset monitoring (OCP domain) Undefined since: From hardware perspective, the reset state is 0. From software user perspective, when the accessible module is 1. Read 0x0: Reset is on-going Read 0x1: Reset is done (completed)	R	1

Table 15-364. Register Call Summary for Register ELM_SYSSTATUS

Error Location Module

- ELM Software Reset: [0]
- Processing Initialization: [1]
- Use Case: ELM Used in Continuous Mode: [2]
- Use Case: ELM Used in Page Mode: [3]
- ELM Register Summary: [4]

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Table 15-365. ELM_IRQSTATUS

Address Offset	0x0000 0018		
Physical Address	0x4807 8018	**Instance**	ELM
Description	Interrupt status. This register doubles as a status register for the error-location processes.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							PAGE_VALID	LOC_VALID_7	LOC_VALID_6	LOC_VALID_5	LOC_VALID_4	LOC_VALID_3	LOC_VALID_2	LOC_VALID_1	LOC_VALID_0

Bits	Field Name	Description	Type	Reset
31:9	RESERVED	Reserved	R	0x000000
8	PAGE_VALID	Error-location status for a full page, based on the mask definition Read 0x0: Error locations invalid for all polynomials enabled in the ECC_INTERRUPT_MASK register Read 0x1: All error locations valid Write 0x0: No effect Write 0x1: Clear interrupt	RW	0
7	LOC_VALID_7	Error-location status for syndrome polynomial 7 Read 0x0: No syndrome processed or process in progress Read 0x1: Error-location process completed Write 0x0: No effect Write 0x1: Clear interrupt	RW W1toClr	0
6	LOC_VALID_6	Error-location status for syndrome polynomial 6	RW W1toClr	0
5	LOC_VALID_5	Error-location status for syndrome polynomial 5	RW W1toClr	0
4	LOC_VALID_4	Error-location status for syndrome polynomial 4	RW W1toClr	0
3	LOC_VALID_3	Error-location status for syndrome polynomial 3	RW W1toClr	0
2	LOC_VALID_2	Error-location status for syndrome polynomial 2	RW W1toClr	0
1	LOC_VALID_1	Error-location status for syndrome polynomial 1	RW W1toClr	0
0	LOC_VALID_0	Error-location status for syndrome polynomial 0	RW W1toClr	0

Table 15-366. Register Call Summary for Register ELM_IRQSTATUS

Error Location Module

- ELM Interrupt Requests: [0] [1] [2] [3] [4] [5] [6] [7] [8]
- Processing Initialization: [9]
- Processing Completion: [10] [11] [12] [13] [14] [15] [16] [17] [18]
- Read Results: [19] [20] [21] [22] [23] [24]
- Use Case: ELM Used in Continuous Mode: [25] [26]
- Use Case: ELM Used in Page Mode: [27] [28] [29]
- ELM Register Summary: [30]

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Table 15-367. ELM_IRQENABLE

Address Offset	0x0000 001C		
Physical Address	0x4807 801C	**Instance**	ELM
Description	Interrupt enable		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							PAGE_MASK	LOCATION_MASK_7	LOCATION_MASK_6	LOCATION_MASK_5	LOCATION_MASK_4	LOCATION_MASK_3	LOCATION_MASK_2	LOCATION_MASK_1	LOCATION_MASK_0

Bits	Field Name	Description	Type	Reset
31:9	RESERVED	Reserved	R	0x000000
8	PAGE_MASK	Page interrupt mask bit 0: Disable interrupt 1: Enable interrupt	RW	0
7	LOCATION_MASK_7	Error-location interrupt mask bit for syndrome polynomial 7	RW	0
6	LOCATION_MASK_6	Error-location interrupt mask bit for syndrome polynomial 6	RW	0
5	LOCATION_MASK_5	Error-location interrupt mask bit for syndrome polynomial 5	RW	0
4	LOCATION_MASK_4	Error-location interrupt mask bit for syndrome polynomial 4	RW	0
3	LOCATION_MASK_3	Error-location interrupt mask bit for syndrome polynomial 3	RW	0
2	LOCATION_MASK_2	Error-location interrupt mask bit for syndrome polynomial 2	RW	0
1	LOCATION_MASK_1	Error-location interrupt mask bit for syndrome polynomial 1	RW	0
0	LOCATION_MASK_0	Error-location interrupt mask bit for syndrome polynomial 0 0: Disable interrupt 1: Enable interrupt	RW	0

Table 15-368. Register Call Summary for Register ELM_IRQENABLE

Error Location Module

- ELM Interrupt Requests: [0] [1] [2] [3] [4] [5] [6] [7] [8]
- Processing Initialization: [9] [10]
- Processing Completion: [11]
- Processing Initialization: [12] [13] [14]
- Use Case: ELM Used in Continuous Mode: [15]
- Use Case: ELM Used in Page Mode: [16]
- ELM Register Summary: [17]

Table 15-369. ELM_LOCATION_CONFIG

Address Offset	0x0000 0020		
Physical Address	0x4807 8020	**Instance**	ELM
Description	ECC algorithm parameters		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								ECC_SIZE								RESERVED															ECC_BCH_LEVEL

Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Reserved	R	0x00
26:16	ECC_SIZE	Maximum size of the buffers for which the error-location engine is used, in number of nibbles (4-bits entities)	RW	0x000
15:2	RESERVED	Reserved	R	0x0000
1:0	ECC_BCH_LEVEL	Error correction level 0x0: 4 bits 0x1: 8 bits 0x2: 16 bits 0x3: Reserved	RW	0x0

Table 15-370. Register Call Summary for Register ELM_LOCATION_CONFIG

Error Location Module

- Processing Initialization: [0] [1] [2]
- Processing Initialization: [3] [4]
- Use Case: ELM Used in Continuous Mode: [5] [6]
- Use Case: ELM Used in Page Mode: [7] [8]
- ELM Register Summary: [9]

Table 15-371. ELM_PAGE_CTRL

Address Offset	0x0000 0080		
Physical Address	0x4807 8080	**Instance**	ELM
Description	Page definition		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								SECTOR_7	SECTOR_6	SECTOR_5	SECTOR_4	SECTOR_3	SECTOR_2	SECTOR_1	SECTOR_0

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Reserved	R	0x000000
7	SECTOR_7	Set to 1 if syndrome polynomial 7 is part of the page in page mode. Must be 0 in continuous mode.	RW	0
6	SECTOR_6	Set to 1 if syndrome polynomial 6 is part of the page in page mode. Must be 0 in continuous mode.	RW	0
5	SECTOR_5	Set to 1 if syndrome polynomial 5 is part of the page in page mode. Must be 0 in continuous mode.	RW	0
4	SECTOR_4	Set to 1 if syndrome polynomial 4 is part of the page in page mode. Must be 0 in continuous mode.	RW	0
3	SECTOR_3	Set to 1 if syndrome polynomial 3 is part of the page in page mode. Must be 0 in continuous mode.	RW	0
2	SECTOR_2	Set to 1 if syndrome polynomial 2 is part of the page in page mode. Must be 0 in continuous mode.	RW	0

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Bits	Field Name	Description	Type	Reset
1	SECTOR_1	Set to 1 if syndrome polynomial 1 is part of the page in page mode. Must be 0 in continuous mode.	RW	0
0	SECTOR_0	Set to 1 if syndrome polynomial 0 is part of the page in page mode. Must be 0 in continuous mode.	RW	0

Table 15-372. Register Call Summary for Register ELM_PAGE_CTRL

Error Location Module

- Processing Initialization: [0]
- Processing Completion: [1] [2] [3] [4]
- Processing Initialization: [5] [6] [7]
- Use Case: ELM Used in Continuous Mode: [8]
- Use Case: ELM Used in Page Mode: [9] [10] [11] [12]
- ELM Register Summary: [13]

Table 15-373. ELM_SYNDROME_FRAGMENT_0_i

Address Offset	0x0000 0400 + (0x40 * i)	**Index**	i = 0 to 7
Physical Address	0x4807 8400 + (0x40 * i)	**Instance**	ELM
Description	Input syndrome polynomial bits 0 to 31.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SYNDROME_0																															

Bits	Field Name	Description	Type	Reset
31:0	SYNDROME_0	Syndrome bits 0 to 31	RW	0x0000 0000

Table 15-374. Register Call Summary for Register ELM_SYNDROME_FRAGMENT_0_i

Error Location Module

- Processing Initialization: [0]
- Processing Initialization: [1]
- Use Case: ELM Used in Continuous Mode: [2]
- Use Case: ELM Used in Page Mode: [3] [4] [5] [6]
- ELM Register Summary: [7]

Table 15-375. ELM_SYNDROME_FRAGMENT_1_i

Address Offset	0x0000 0404 + (0x40 * i)	**Index**	i = 0 to 7
Physical Address	0x4807 8404 + (0x40 * i)	**Instance**	ELM
Description	Input syndrome polynomial bits 32 to 63.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SYNDROME_1																															

Bits	Field Name	Description	Type	Reset
31:0	SYNDROME_1	Syndrome bits 32 to 63	RW	0x0000 0000

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Table 15-376. Register Call Summary for Register ELM_SYNDROME_FRAGMENT_1_i

Error Location Module

- Processing Initialization: [0]
- Use Case: ELM Used in Continuous Mode: [1]
- Use Case: ELM Used in Page Mode: [2] [3] [4] [5]
- ELM Register Summary: [6]

Table 15-377. ELM_SYNDROME_FRAGMENT_2_i

Address Offset	0x0000 0408 + (0x40 * i)	**Index**	i = 0 to 7
Physical Address	0x4807 8408 + (0x40 * i)	**Instance**	ELM
Description	Input syndrome polynomial bits 64 to 95.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SYNDROME_2																															

Bits	Field Name	Description	Type	Reset
31:0	SYNDROME_2	Syndrome bits 64 to 95	RW	0x0000 0000

Table 15-378. Register Call Summary for Register ELM_SYNDROME_FRAGMENT_2_i

Error Location Module

- Use Case: ELM Used in Continuous Mode: [0]
- Use Case: ELM Used in Page Mode: [1] [2] [3] [4]
- ELM Register Summary: [5]

Table 15-379. ELM_SYNDROME_FRAGMENT_3_i

Address Offset	0x0000 040C + (0x40 * i)	**Index**	i = 0 to 7
Physical Address	0x4807 840C + (0x40 * i)	**Instance**	ELM
Description	Input syndrome polynomial bits 96 to 127		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SYNDROME_3																															

Bits	Field Name	Description	Type	Reset
31:0	SYNDROME_3	Syndrome bits 96 to 127	RW	0x0000 0000

Table 15-380. Register Call Summary for Register ELM_SYNDROME_FRAGMENT_3_i

Error Location Module

- Use Case: ELM Used in Continuous Mode: [0]
- Use Case: ELM Used in Page Mode: [1] [2] [3] [4]
- ELM Register Summary: [5]

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Table 15-381. ELM_SYNDROME_FRAGMENT_4_i

Address Offset	0x0000 0410 + (0x40 * i)	**Index**	i = 0 to 7
Physical Address	0x4807 8410 + (0x40 * i)	**Instance**	ELM
Description	Input syndrome polynomial bits 128 to 159.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SYNDROME_4																															

Bits	Field Name	Description	Type	Reset
31:0	SYNDROME_4	Syndrome bits 128 to 159	RW	0x0000 0000

Table 15-382. Register Call Summary for Register ELM_SYNDROME_FRAGMENT_4_i

Error Location Module

- Use Case: ELM Used in Page Mode: [0] [1] [2] [3]
- ELM Register Summary: [4]

Table 15-383. ELM_SYNDROME_FRAGMENT_5_i

Address Offset	0x0000 0414 + (0x40 * i)	**Index**	i = 0 to 7
Physical Address	0x4807 8414 + (0x40 * i)	**Instance**	ELM
Description	Input syndrome polynomial bits 160 to 191.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SYNDROME_5																															

Bits	Field Name	Description	Type	Reset
31:0	SYNDROME_5	Syndrome bits 160 to 191	RW	0x0000 0000

Table 15-384. Register Call Summary for Register ELM_SYNDROME_FRAGMENT_5_i

Error Location Module

- Processing Initialization: [0]
- Use Case: ELM Used in Page Mode: [1] [2] [3] [4]
- ELM Register Summary: [5]

Table 15-385. ELM_SYNDROME_FRAGMENT_6_i

Address Offset	0x0000 0418 + (0x40 * i)	**Index**	i = 0 to 7
Physical Address	0x4807 8418 + (0x40 * i)	**Instance**	ELM
Description	Input syndrome polynomial bits 192 to 207.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															SYNDROME_VALID	SYNDROME_6															

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Bits	Field Name	Description	Type	Reset
31:17	RESERVED	Reserved	R	0x0000
16	SYNDROME_VALID	Syndrome valid bit 0x0: This syndrome polynomial should not be processed. 0x1: This syndrome polynomial must be processed.	RW	0
15:0	SYNDROME_6	Syndrome bits 192 to 207	RW	0x0000

Table 15-386. Register Call Summary for Register ELM_SYNDROME_FRAGMENT_6_i

Error Location Module

- Processing Initialization: [0] [1] [2] [3]
- Processing Completion: [4] [5]
- Processing Initialization: [6] [7]
- Read Results: [8]
- Use Case: ELM Used in Continuous Mode: [9]
- Use Case: ELM Used in Page Mode: [10] [11] [12] [13] [14] [15] [16] [17]
- ELM Register Summary: [18]

Table 15-387. ELM_LOCATION_STATUS_i

Address Offset	0x0000 0800 + (0x100 * i)	**Index**	i = 0 to 7
Physical Address	0x4807 8800 + (0x100 * i)	**Instance**	ELM
Description	Exit status for the syndrome polynomial processing		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							ECC_CORRECTABLE	RESERVED						ECC_NB_ERRORS	

Bits	Field Name	Description	Type	Reset
31:9	RESERVED	Reserved	R	0x000000
8	ECC_CORRECTABLE	Error-location process exit status 0x0: ECC error-location process failed. Number of errors and error locations are invalid. 0x1: All errors were successfully located. Number of errors and error locations are valid.	R	0
7:5	RESERVED	Reserved	R	0x0
4:0	ECC_NB_ERRORS	Number of errors detected and located	R	0x00

Table 15-388. Register Call Summary for Register ELM_LOCATION_STATUS_i

Error Location Module

- Processing Initialization: [0]
- Processing Sequence: [1] [2] [3] [4]
- Processing Completion: [5] [6] [7]
- Read Results: [8] [9] [10] [11] [12] [13] [14] [15]
- Use Case: ELM Used in Continuous Mode: [16] [17]
- Use Case: ELM Used in Page Mode: [18] [19] [20] [21] [22] [23] [24] [25]
- ELM Register Summary: [26]

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Table 15-389. ELM_ERROR_LOCATION_0_i

Address Offset	0x0000 0880 + (0x100 * i)	**Index**	i = 0 to 7
Physical Address	0x4807 8880 + (0x100 * i)	**Instance**	ELM
Description	Error-location register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								ECC_ERROR_LOCATION							

Bits	Field Name	Description	Type	Reset
31:13	RESERVED	Reserved	R	0x00000
12:0	ECC_ERROR_LOCATION	Error-location bit address	R	0x0000

Table 15-390. Register Call Summary for Register ELM_ERROR_LOCATION_0_i

Error Location Module

- Processing Initialization: [0]
- Processing Sequence: [1] [2] [3]
- Processing Completion: [4]
- Read Results: [5] [6]
- Use Case: ELM Used in Continuous Mode: [7]
- Use Case: ELM Used in Page Mode: [8] [9] [10]
- ELM Register Summary: [11]

Table 15-391. ELM_ERROR_LOCATION_1_i

Address Offset	0x0000 0884 + (0x100 * i)	**Index**	i = 0 to 7
Physical Address	0x4807 8884 + (0x100 * i)	**Instance**	ELM
Description	Error-location register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								ECC_ERROR_LOCATION							

Bits	Field Name	Description	Type	Reset
31:13	RESERVED	Reserved	R	0x00000
12:0	ECC_ERROR_LOCATION	Error-location bit address	R	0x0000

Table 15-392. Register Call Summary for Register ELM_ERROR_LOCATION_1_i

Error Location Module

- Processing Sequence: [0]
- Read Results: [1] [2]
- Use Case: ELM Used in Continuous Mode: [3]
- Use Case: ELM Used in Page Mode: [4] [5]
- ELM Register Summary: [6]

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Table 15-393. ELM_ERROR_LOCATION_2_i

Address Offset	0x0000 0888 + (0x100 * i)	**Index**	i = 0 to 7
Physical Address	0x4807 8888 + (0x100 * i)	**Instance**	ELM
Description	Error-location register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								ECC_ERROR_LOCATION							

Bits	Field Name	Description	Type	Reset
31:13	RESERVED	Reserved	R	0x00000
12:0	ECC_ERROR_LOCATION	Error-location bit address	R	0x0000

Table 15-394. Register Call Summary for Register ELM_ERROR_LOCATION_2_i

Error Location Module

- Use Case: ELM Used in Continuous Mode: [0]
- Use Case: ELM Used in Page Mode: [1]
- ELM Register Summary: [2]

Table 15-395. ELM_ERROR_LOCATION_3_i

Address Offset	0x0000 088C + (0x100 * i)	**Index**	i = 0 to 7
Physical Address	0x4807 888C + (0x100 * i)	**Instance**	ELM
Description	Error-location register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								ECC_ERROR_LOCATION							

Bits	Field Name	Description	Type	Reset
31:13	RESERVED	Reserved	R	0x00000
12:0	ECC_ERROR_LOCATION	Error-location bit address	R	0x0000

Table 15-396. Register Call Summary for Register ELM_ERROR_LOCATION_3_i

Error Location Module

- Use Case: ELM Used in Continuous Mode: [0]
- Use Case: ELM Used in Page Mode: [1]
- ELM Register Summary: [2]

Table 15-397. ELM_ERROR_LOCATION_4_i

Address Offset	0x0000 0890 + (0x100 * i)	**Index**	i = 0 to 7
Physical Address	0x4807 8890 + (0x100 * i)	**Instance**	ELM
Description	Error-location register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								ECC_ERROR_LOCATION							

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Bits	Field Name	Description	Type	Reset
31:13	RESERVED	Reserved	R	0x00000
12:0	ECC_ERROR_LOCATION	Error-location bit address	R	0x0000

Table 15-398. Register Call Summary for Register ELM_ERROR_LOCATION_4_i

Error Location Module

- ELM Register Summary: [0]

Table 15-399. ELM_ERROR_LOCATION_5_i

Address Offset	0x0000 0894 + (0x100 * i)	**Index**	i = 0 to 7
Physical Address	0x4807 8894 + (0x100 * i)	**Instance**	ELM
Description	Error-location register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								ECC_ERROR_LOCATION							

Bits	Field Name	Description	Type	Reset
31:13	RESERVED	Reserved	R	0x00000
12:0	ECC_ERROR_LOCATION	Error-location bit address	R	0x0000

Table 15-400. Register Call Summary for Register ELM_ERROR_LOCATION_5_i

Error Location Module

- ELM Register Summary: [0]

Table 15-401. ELM_ERROR_LOCATION_6_i

Address Offset	0x0000 0898 + (0x100 * i)	**Index**	i = 0 to 7
Physical Address	0x4807 8898 + (0x100 * i)	**Instance**	ELM
Description	Error-location register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								ECC_ERROR_LOCATION							

Bits	Field Name	Description	Type	Reset
31:13	RESERVED	Reserved	R	0x00000
12:0	ECC_ERROR_LOCATION	Error-location bit address	R	0x0000

Table 15-402. Register Call Summary for Register ELM_ERROR_LOCATION_6_i

Error Location Module

- ELM Register Summary: [0]

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Table 15-403. ELM_ERROR_LOCATION_7_i

Address Offset	0x0000 089C + (0x100 * i)	**Index**	i = 0 to 7
Physical Address	0x4807 889C + (0x100 * i)	**Instance**	ELM
Description	Error-location register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								ECC_ERROR_LOCATION							

Bits	Field Name	Description	Type	Reset
31:13	RESERVED	Reserved	R	0x00000
12:0	ECC_ERROR_LOCATION	Error-location bit address	R	0x0000

Table 15-404. Register Call Summary for Register ELM_ERROR_LOCATION_7_i

Error Location Module

- ELM Register Summary: [0]

Table 15-405. ELM_ERROR_LOCATION_8_i

Address Offset	0x0000 08A0 + (0x100 * i)	**Index**	i = 0 to 7
Physical Address	0x4807 88A0 + (0x100 * i)	**Instance**	ELM
Description	Error-location register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								ECC_ERROR_LOCATION							

Bits	Field Name	Description	Type	Reset
31:13	RESERVED	Reserved	R	0x00000
12:0	ECC_ERROR_LOCATION	Error-location bit address	R	0x0000

Table 15-406. Register Call Summary for Register ELM_ERROR_LOCATION_8_i

Error Location Module

- ELM Register Summary: [0]

Table 15-407. ELM_ERROR_LOCATION_9_i

Address Offset	0x0000 08A4 + (0x100 * i)	**Index**	i = 0 to 7
Physical Address	0x4807 88A4 + (0x100 * i)	**Instance**	ELM
Description	Error-location register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								ECC_ERROR_LOCATION							

Bits	Field Name	Description	Type	Reset
31:13	RESERVED	Reserved	R	0x00000
12:0	ECC_ERROR_LOCATION	Error-location bit address	R	0x0000

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Table 15-408. Register Call Summary for Register ELM_ERROR_LOCATION_9_i

Error Location Module

- ELM Register Summary: [0]

Table 15-409. ELM_ERROR_LOCATION_10_i

Address Offset	0x0000 08A8 + (0x100 * i)	**Index**	i = 0 to 7
Physical Address	0x4807 88A8 + (0x100 * i)	**Instance**	ELM
Description	Error-location register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								ECC_ERROR_LOCATION							

Bits	Field Name	Description	Type	Reset
31:13	RESERVED	Reserved	R	0x00000
12:0	ECC_ERROR_LOCATION	Error-location bit address	R	0x0000

Table 15-410. Register Call Summary for Register ELM_ERROR_LOCATION_10_i

Error Location Module

- ELM Register Summary: [0]

Table 15-411. ELM_ERROR_LOCATION_11_i

Address Offset	0x0000 08AC + (0x100 * i)	**Index**	i = 0 to 7
Physical Address	0x4807 88AC + (0x100 * i)	**Instance**	ELM
Description	Error-location register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								ECC_ERROR_LOCATION							

Bits	Field Name	Description	Type	Reset
31:13	RESERVED	Reserved	R	0x00000
12:0	ECC_ERROR_LOCATION	Error-location bit address	R	0x0000

Table 15-412. Register Call Summary for Register ELM_ERROR_LOCATION_11_i

Error Location Module

- ELM Register Summary: [0]

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Table 15-413. ELM_ERROR_LOCATION_12_i

Address Offset	0x0000 08B0 + (0x100 * i)	**Index**	i = 0 to 7
Physical Address	0x4807 88B0 + (0x100 * i)	**Instance**	ELM
Description	Error-location register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								ECC_ERROR_LOCATION							

Bits	Field Name	Description	Type	Reset
31:13	RESERVED	Reserved	R	0x00000
12:0	ECC_ERROR_LOCATION	Error-location bit address	R	0x0000

Table 15-414. Register Call Summary for Register ELM_ERROR_LOCATION_12_i

Error Location Module

- ELM Register Summary: [0]

Table 15-415. ELM_ERROR_LOCATION_13_i

Address Offset	0x0000 08B4 + (0x100 * i)	**Index**	i = 0 to 7
Physical Address	0x4807 88B4 + (0x100 * i)	**Instance**	ELM
Description	Error-location register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								ECC_ERROR_LOCATION							

Bits	Field Name	Description	Type	Reset
31:13	RESERVED	Reserved	R	0x00000
12:0	ECC_ERROR_LOCATION	Error-location bit address	R	0x0000

Table 15-416. Register Call Summary for Register ELM_ERROR_LOCATION_13_i

Error Location Module

- ELM Register Summary: [0]

Table 15-417. ELM_ERROR_LOCATION_14_i

Address Offset	0x0000 08B8 + (0x100 * i)	**Index**	i = 0 to 7
Physical Address	0x4807 88B8 + (0x100 * i)	**Instance**	ELM
Description	Error-location register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								ECC_ERROR_LOCATION							

Bits	Field Name	Description	Type	Reset
31:13	RESERVED	Reserved	R	0x00000
12:0	ECC_ERROR_LOCATION	Error-location bit address	R	0x0000

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Table 15-418. Register Call Summary for Register ELM_ERROR_LOCATION_14_i

Error Location Module

- ELM Register Summary: [0]

Table 15-419. ELM_ERROR_LOCATION_15_i

Address Offset	0x0000 08BC + (0x100 * i)	**Index**	i = 0 to 7
Physical Address	0x4807 88BC + (0x100 * i)	**Instance**	ELM
Description	Error-location register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								ECC_ERROR_LOCATION							

Bits	Field Name	Description	Type	Reset
31:13	RESERVED	Reserved	R	0x00000
12:0	ECC_ERROR_LOCATION	Error-location bit address	R	0x0000

Table 15-420. Register Call Summary for Register ELM_ERROR_LOCATION_15_i

Error Location Module

- Processing Initialization: [0]
- Processing Sequence: [1] [2]
- Processing Completion: [3]
- Read Results: [4] [5]
- ELM Register Summary: [6]

15.6 On-Chip Memory (OCM) Subsystem

15.6.1 OCM Subsystem Overview

There are three on-chip memories in the device.

- A 4K-byte SAR read-only memory (ROM)
- A 8K-byte SAR random-access memory (RAM)
- A 56K-byte L3 static random-access memory (L3 OCM_RAM)

There are other on-chip memories located inside other subsystems (Cortex-A9 MPU, DSP IVA-HD, ABE, Cortex-M3 MPU) that are not described in the following sections. Refer to each subsystem chapter for more details.

15.6.2 OCM Subsystem Integration

Figure 15-101 shows the integration of the OCM subsystem to the device.

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Figure 15-101. OCM Subsystem Integration to the Device

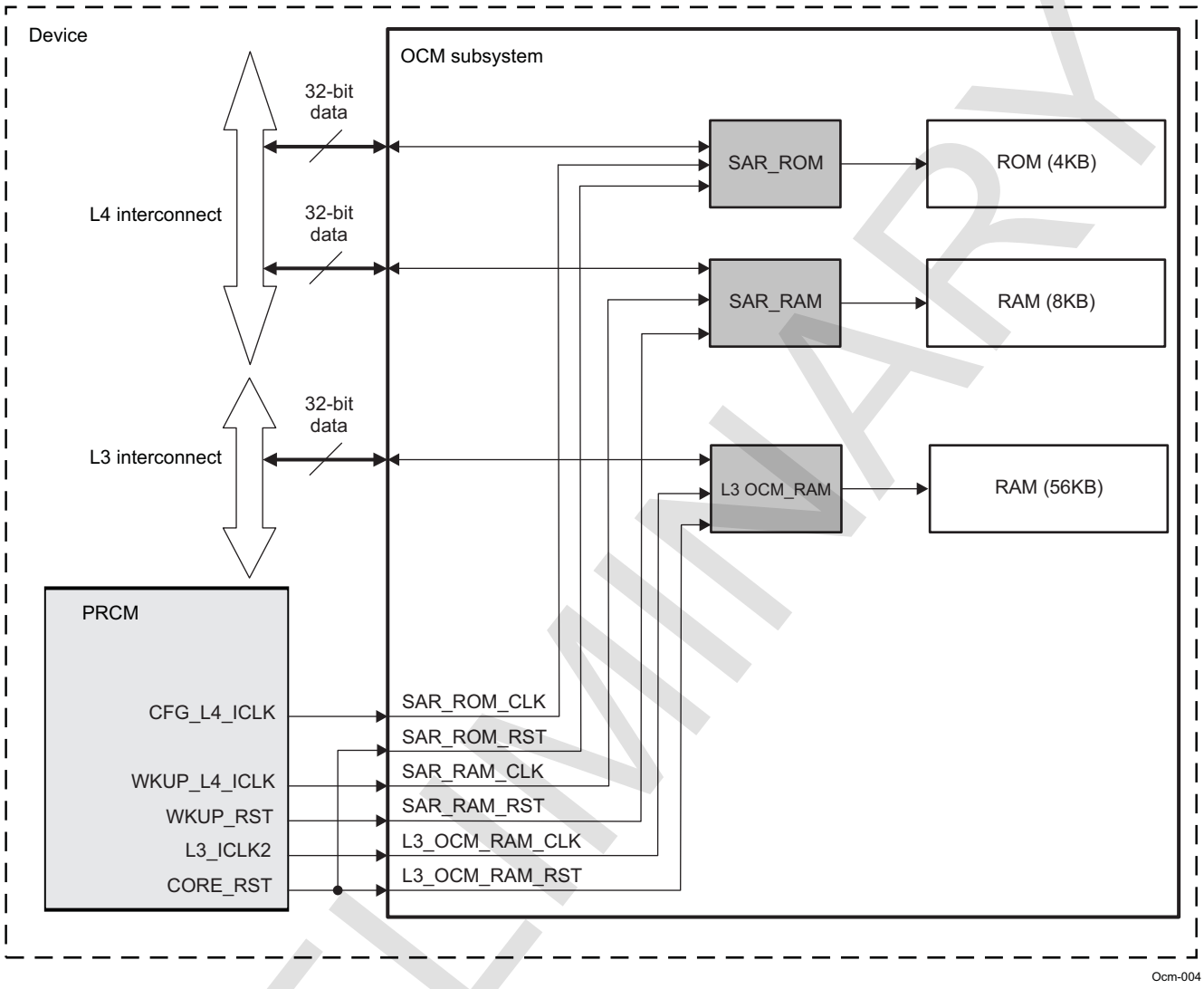

Table 15-421 through Table 15-422 summarize the integration of the module in the device.

Table 15-421. Integration Attributes

Module Instance	Attributes		
	Power Domain	Wake-Up Capability	Interconnect
L3 OCM_RAM	PD_CORE	No	NA
SAR_RAM	PD_WKUP	No	NA
SAR_ROM	PD_CORE	No	NA

Table 15-422. Clocks and Resets

Clocks				
Module Instance	Destination Signal Name	Source Signal Name	Source	Description
L3 OCM_RAM	L3 OCM_RAM_CLK	L3_ICLK2	PRCM	L3 OCM_RAM Clock For information about PRCM clock gating and management, see the *CORE Power Domain Clocks Controls* section in Chapter 3, *Power, Reset, and Clock Management*.

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Table 15-422. Clocks and Resets (continued)

SAR_RAM	SAR_RAM_CLK	WKUP_L4_ICLK	PRCM	SAR RAM clock For information about PRCM clock gating and management, see the *Wake-Up Power Domain Clocks Controls* section in Chapter 3, *Power, Reset, and Clock Management*.
SAR_ROM	SAR_ROM_CLK	CFG_L4_ICLK	PRCM	SAR ROM clock For information about PRCM clock gating and management, see the *CORE Power Domain Clocks Controls* section in Chapter 3, *Power, Reset, and Clock Management*.
		Resets		
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
L3 OCM_RAM	L3 OCM_RAM_RST	CORE_RST	PRCM	L3 OCM_RAM reset signal For information about PRCM reset sources and distribution, see the *CORE Power Domain Reset Description* section in Chapter 3, *Power, Reset, and Clock Management*.
SAR_RAM	SAR_RAM_RST	WKUP_RST	PRCM	SAR RAM reset signal For information about PRCM reset sources and distribution, see the *WAKE-UP Power Domain Reset Description* section in Chapter 3, *Power, Reset, and Clock Management*.
SAR_ROM	SAR_ROM_RST	CORE_RST	PRCM	SAR ROM reset signal For information about PRCM reset sources and distribution, see the *CORE Power Domain Reset Description* section in Chapter 3, *Power, Reset, and Clock Management*.

15.6.3 OCM Subsystem Functional Description

15.6.3.1 SAR ROM

This on-chip ROM contains 4K bytes of memory and a linked list of descriptors used by the system DMA (sDMA) during the restore context operation (when device transitions from OFF to ON modes).

The device-embedded SAR ROM has the following characteristics:

- 4K-bytes ROM
- 32-bit access per cycle
- Support for single and burst access transactions

  The memory space of the embedded ROM starts at 0x4A05 E000 and ends at 0x4A05 FFFF (8K bytes are reserved, but only 4K bytes are used).

15.6.3.2 SAR RAM

The on-chip SAR RAM contains 8K bytes and is mapped as 4 blocks with irregular region sizes. This memory content is preserved when the device goes into OFF mode (as long as the wake-up voltage domain remains supplied). It is used as context-saving memory to be written by the software, so that the sDMA restores its saved content when the device transitions from OFF to ON mode. Locations not used by the sDMA can be used as a scratch-pad memory by the software. It is mapped on the wake-up voltage domain.

The device-embedded SAR RAM has the following characteristics:

- Support for single-access transactions
  - Operates at full L4-PER interconnect clock frequency
  - 32-bit access per cycle

The SAR RAM space is at the following location:

- SAR space 1 (4KB): Starts at 0x4A32 6000 and ends at 0x4A32 6FFF

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- SAR space 2 (1KB): Starts at 0x4A32 7000 and ends at 0x4A32 73FF
- SAR space 3 (2KB): Starts at 0x4A32 8000 and ends at 0x4A32 87FF
- SAR space 4 (1KB): Starts at 0x4A32 9000 and ends at 0x4A32 93FF

15.6.3.3 L3 OCM_RAM

The on-chip L3 OCM_RAM contains 56K bytes of RAM, partitioning is defined by the L3 firewall logic.

The device-embedded L3 OCM_RAM has the following characteristics:

- Support for single and burst access transactions:
  - Operates at full L3 interconnect clock frequency
  - Fully pipelined, one 32-bit access per cycle
- Restricted access support based on:
  - A region-based partitioning (refer to L3 firewall description)
  - The module owner of the access, with respect to its read and write permissions to that region
  - The transaction attributes of the access, with respect to the region permission properties. See Section 13.2, *L3 Interconnect* for details.

The memory space of the embedded RAM starts at 0x4030 0000 and ends at 0x4030 DFFF.

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sDMA

This chapter describes the system direct memory access (sDMA) module.

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16.3 sDMA Module Integration 3344
16.4 sDMA Functional Description 3349
16.5 sDMA Basic Programming Model 3383
16.6 sDMA Register Manual 3392

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16.1 sDMA Module Overview

The system direct memory access (sDMA) module, also called DMA4, performs high-performance data transfers between memories and peripheral devices without microprocessor unit (MPU) or digital signal processor (DSP) support during transfer. A DMA transfer is programmed through a logical DMA channel, which allows the transfer to be optimally tailored to the requirements of the application.

The DMA controller includes the following main features:

- Data transfer support in either direction between:
  - Memory and memory
  - Memory and peripheral device
- 32 logical DMA channels supporting:
  - Multiple concurrent transfers
  - Independent transfer profile for each channel
  - 8-bit, 16-bit, or 32-bit data element transfer size
  - Software-triggered or hardware-synchronized transfers
  - Flexible source and destination address generation
  - Burst read and write
  - Chained multiple-channel transfers
  - Endianism conversion
  - Draining
  - Linked-list support for descriptor types 1, 2, and 3
- First-come, first-serve DMA scheduling with fixed priority
- Up to 127 DMA requests
- Constant fill
- Transparent copy
- Four programmable interrupt request output lines
- FIFO depth: 256 × 64-bit
- Data buffering
- FIFO budget allocation
- Power-management support
- Auto-idle power-saving support
- Implementation of retention flip-flops (RFFs) to support dynamic power switching (DPS) between system power modes without MPU involvement. For more information about DPS, see Section 3.1.2.3, *Dynamic Power Switching*, in Chapter 3, *Power, Reset and Clock Management*.

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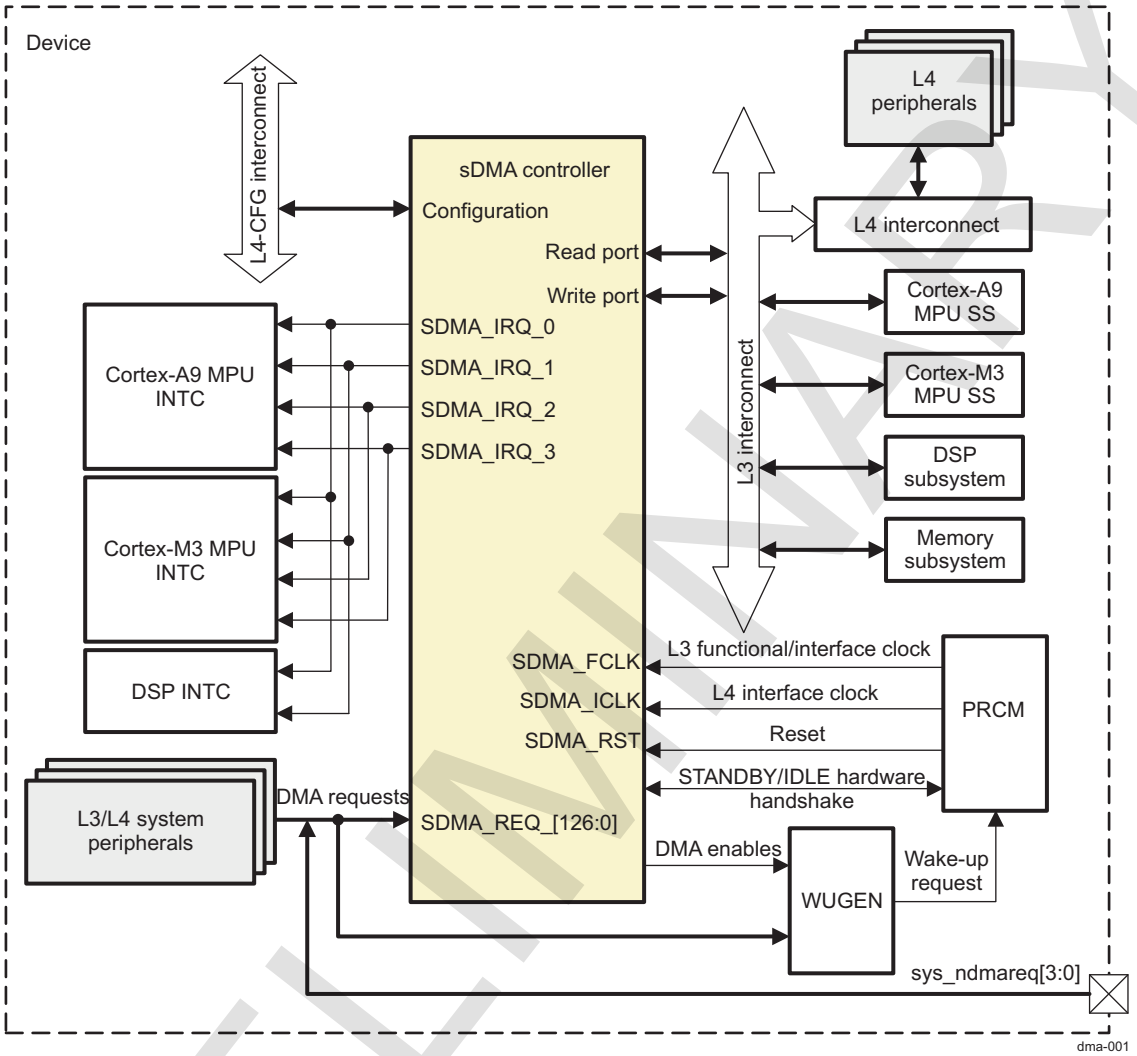
Figure 16-1 shows an overview of the sDMA module.

Figure 16-1. sDMA Overview



The sDMA module has three ports: one read, one write, and one configuration port, and provides multiple logical channel support. A dynamically allocated FIFO queue memory pool provides buffering between the read and write ports, which are multithreaded (two threads for the write port and four threads for the read port); this means that each transaction is flagged by a thread ID (0, 1, 2, or 3) in the request direction and in the response direction. This allows the read port to have four outstanding requests at a time. The write port has two threads budget available.

The MPU (or DSP) configures the sDMA through the L4-CFG interconnect.

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16.2 sDMA Controller Environment

The sDMA controller supports external DMA requests through the sys_ndmareq[3:0] pins (see Table 16-1). A logical channel can be configured to respond to an external synchronization request.

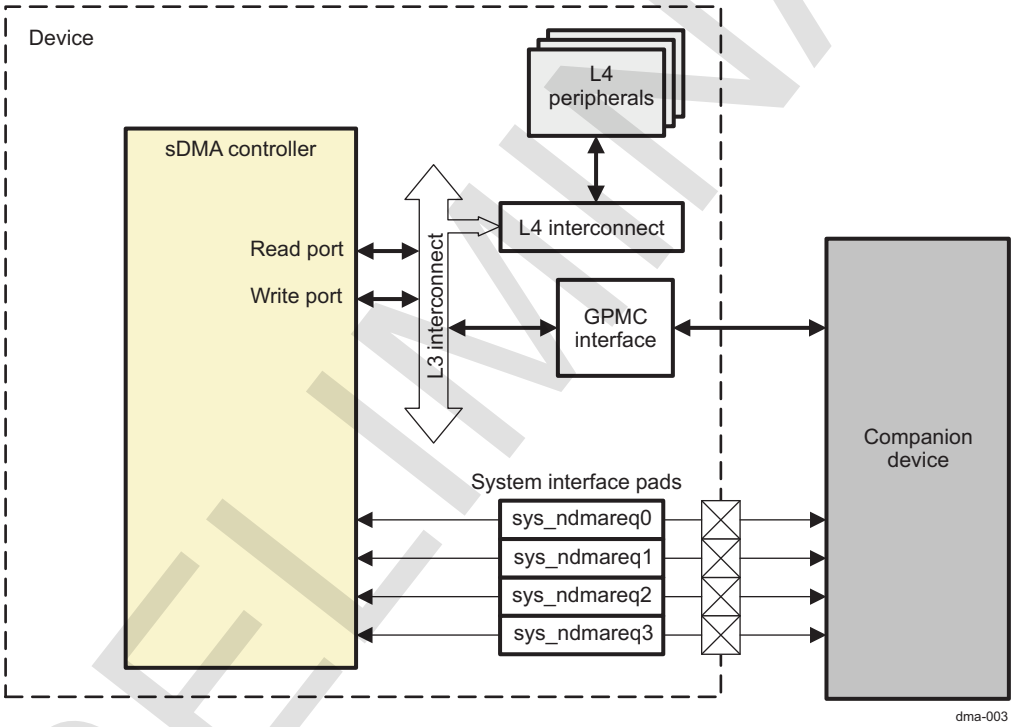
Table 16-1. External sDMA Request Signals

Signal Name	I/O [1]	Description
sys_ndmareq0	I	External DMA request 0 (system expansion)
sys_ndmareq1	I	External DMA request 1 (system expansion)
sys_ndmareq2	I	External DMA request 2 (system expansion)
sys_ndmareq3	I	External DMA request 3 (system expansion)

(1) I = Input, O = Output

Figure 16-2 shows an example of how to use the external hardware DMA request pins in the sDMA environment.

Figure 16-2. Example of External DMA Requests Use



An external device can use the external DMA request pins to start a logical channel transfer over the general-purpose memory controller (GPMC) interface. The transfer can be a memory-to-memory transfer in which the source memory is in the external device.

By default, the external DMA request signals are not available on external pins after a cold reset. For more information about multiplexing out the four signal lines to pins, see Chapter 18, *Control Module*.

All 127 DMA request lines are transition-sensitive.

For a transition-sensitive DMA request (see Figure 16-3), the line must be maintained low (asserted) until the first DMA access is complete, after which the line must be maintained high (deasserted) for greater than one clock cycle (DMA_L3_ICLK):

- When the deassertion time is less than one clock cycle, the sDMA may not detect the deassertion.
- When the channel is enabled one cycle after a DMA request is disabled, the channel detects the DMA request and starts the corresponding transfer.
- When the channel is enabled two cycles after the DMA request is disabled, the channel does not

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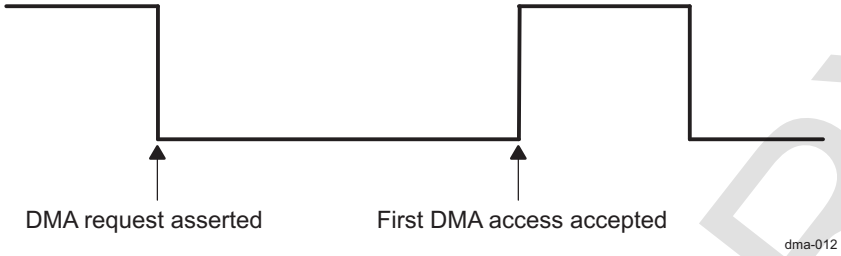
detect the DMA request.

Figure 16-3. Transition-Sensitive DMA Request Scheme



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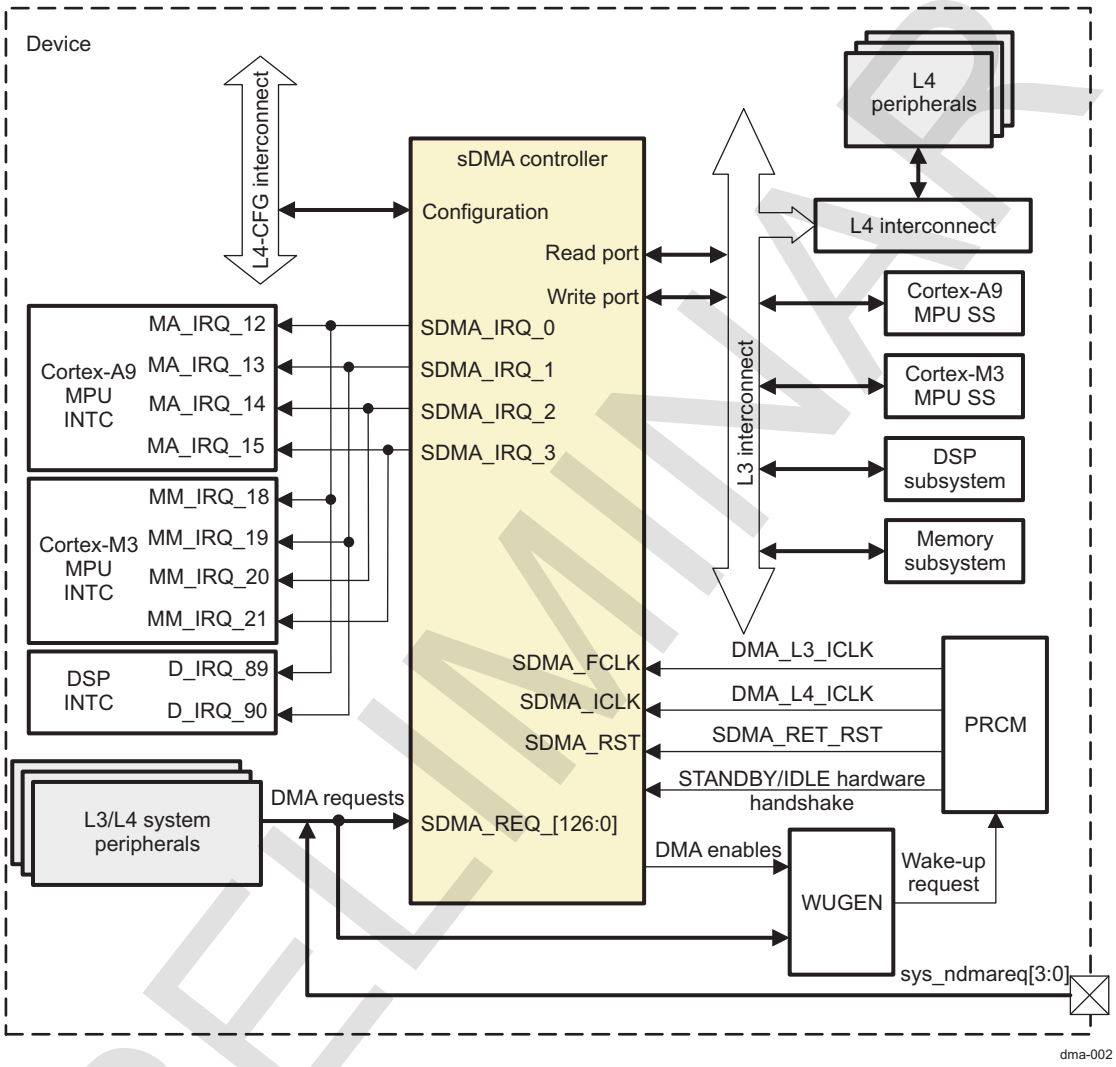
16.3 sDMA Module Integration

This section describes the integration of the module in the device, including information about clocks, resets, and hardware requests.

Figure 16-4 shows the sDMA controller integration.

Figure 16-4. sDMA Controller Integration



NOTE: For more information about the wake-up generator (WUGEN), the STANDBY/IDLE hardware handshake, and the wake-up request, see Section 3.1.1.1, *Clock Management* , in Chapter 3, *Power, Reset, and Clock Management*.

Table 16-2 through Table 16-4 summarize the integration of the module in the device.

Table 16-2. Integration Attributes

Module Instance	Attributes	
	Power Domain	Interconnect
sDMA	PD_CORE	L3 and L4-CFG

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Table 16-3. Clocks and Resets

Clocks				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
sDMA	SDMA_FCLK	DMA_L3_ICLK	PRCM	Functional clock for all internal logic and for the two master read and write ports. For information about the power, reset, and clock management (PRCM) clock gating and management, see Chapter 3, *Power, Reset, and Clock Management*.
	SDMA_ICLK	DMA_L4_ICLK		Interface clock. It supports the configuration port. For information about PRCM clock gating and management, see Chapter 3, *Power, Reset, and Clock Management*.
Resets				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
sDMA	SDMA_RST	SDMA_RET_RST	PRCM	Hardware reset. It initializes all internal logic of the sDMA module, all global registers, and some of the per-channel registers, implemented in flip-flops. However, all remaining per-channel registers are memory-based, and, therefore, are not reset (have undefined values). Thus, when programming a channel for the first time, all bits that have undefined reset values must be configured before enabling the channel. For information about PRCM reset sources and distribution, see Chapter 3, *Power, Reset, and Clock Management*.

Table 16-4. Hardware Requests

Interrupt Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
sDMA	SDMA_IRQ_0	MA_IRQ_12	Cortex™-A9 MPU INTC	sDMA interrupt request 0. For information about the Cortex-A9 MPU INTC, see Section 17.3.2.
	SDMA_IRQ_1	MA_IRQ_13	Cortex-A9 MPU INTC	sDMA interrupt request 1
	SDMA_IRQ_2	MA_IRQ_14	Cortex-A9 MPU INTC	sDMA interrupt request 2
	SDMA_IRQ_3	MA_IRQ_15	Cortex-A9 MPU INTC	sDMA interrupt request 3
	SDMA_IRQ_0	MM_IRQ_18	Cortex™-M3 MPU INTC	sDMA interrupt request 0. For information about the Cortex-M3 MPU INTC, see Section 17.3.3.
	SDMA_IRQ_1	MM_IRQ_19	Cortex-M3 MPU INTC	sDMA interrupt request 1
	SDMA_IRQ_2	MM_IRQ_20	Cortex-M3 MPU INTC	sDMA interrupt request 2
	SDMA_IRQ_3	MM_IRQ_21	Cortex-M3 MPU INTC	sDMA interrupt request 3
	SDMA_IRQ_0	D_IRQ_89	DSP INTC	sDMA interrupt request 0. For information about the DSP INTC, see .
	SDMA_IRQ_1	D_IRQ_90	DSP INTC	sDMA interrupt request 1

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NOTE: For a description of the interrupt source, see Section 16.4.2, *sDMA Controller Interrupt Requests*.

16.3.1 DMA Requests to the sDMA Controller

Table 16-5 lists the sDMA controller request mapping.

Table 16-5. sDMA Controller Request Mapping

DMA Request Line	Source	Description
S_DMA_0	Reserved	Reserved
S_DMA_1	sys_dma_req0	External DMA request 0 (system expansion)
S_DMA_2	sys_dma_req1	External DMA request 1 (system expansion)
S_DMA_3	GPMC_DMA	GPMC data transmit request from prefetch engine
S_DMA_4	Reserved	Reserved
S_DMA_5	DSS_DISPC_DMA	Frame update request
S_DMA_6	sys_dma_req2	External DMA request 2 (system expansion)
S_DMA_7	MCASP1_AXEVT	McASP1 transmit request
S_DMA_8	ISS_DMA0	Imaging subsystem request 0
S_DMA_9	ISS_DMA1	Imaging subsystem request 1
S_DMA_10	Reserved	Reserved
S_DMA_11	ISS_DMA2	Imaging subsystem request 2
S_DMA_12	ISS_DMA3	Imaging subsystem request 3
S_DMA_13	DSS_RFBI_DMA	Display subsystem RFBI request
S_DMA_14	SPI3_DMA_TX0	McSPI3 transmit request channel 0
S_DMA_15	SPI3_DMA_RX0	McSPI3 receive request channel 0
S_DMA_16	MCBSP2_DMA_TX	McBSP2 transmit request
S_DMA_17	MCBSP2_DMA_RX	McBSP2 receive request
S_DMA_18	MCBSP3_DMA_TX	McBSP3 transmit request
S_DMA_19	MCBSP3_DMA_RX	McBSP3 receive request
S_DMA_20	C2C_SSCM_GPO0	C2C GPO line 0
S_DMA_21	C2C_SSCM_GPO1	C2C GPO line 1
S_DMA_22	SPI3_DMA_TX1	McSPI3 transmit request channel 1
S_DMA_23	SPI3_DMA_RX1	McSPI3 receive request channel 1
S_DMA_24	I2C3_DMA_TX	I2C3 transmit request
S_DMA_25	I2C3_DMA_RX	I2C3 receive request
S_DMA_26	I2C1_DMA_TX	I2C1 transmit request
S_DMA_27	I2C1_DMA_RX	I2C1 receive request
S_DMA_28	I2C2_DMA_TX	I2C2 transmit request
S_DMA_29	I2C2_DMA_RX	I2C2 receive request
S_DMA_30	MCBSP4_DMA_TX	McBSP4 transmit request
S_DMA_31	MCBSP4_DMA_RX	McBSP4 receive request
S_DMA_32	MCBSP1_DMA_TX	McBSP1 transmit request
S_DMA_33	MCBSP1_DMA_RX	McBSP1 receive request
S_DMA_34	SPI1_DMA_TX0	McSPI1 transmit request channel 0
S_DMA_35	SPI1_DMA_RX0	McSPI1 receive request channel 0
S_DMA_36	SPI1_DMA_TX1	McSPI1 transmit request channel 1
S_DMA_37	SPI1_DMA_RX1	McSPI1 receive request channel 1
S_DMA_38	SPI1_DMA_TX2	McSPI1 transmit request channel 2
S_DMA_39	SPI1_DMA_RX2	McSPI1 receive request channel 2

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Table 16-5. sDMA Controller Request Mapping (continued)

DMA Request Line	Source	Description
S_DMA_40	SPI1_DMA_TX3	McSPI1 transmit request channel 3
S_DMA_41	SPI1_DMA_RX3	McSPI1 receive request channel 3
S_DMA_42	SPI2_DMA_TX0	McSPI2 transmit request channel 0
S_DMA_43	SPI2_DMA_RX0	McSPI2 receive request channel 0
S_DMA_44	SPI2_DMA_TX1	McSPI2 transmit request channel 1
S_DMA_45	SPI2_DMA_RX1	McSPI2 receive request channel 1
S_DMA_46	MMC2_DMA_TX	MMC2 transmit request
S_DMA_47	MMC2_DMA_RX	MMC2 receive request
S_DMA_48	UART1_DMA_TX	UART1 transmit request
S_DMA_49	UART1_DMA_RX	UART1 receive request
S_DMA_50	UART2_DMA_TX	UART2 transmit request
S_DMA_51	UART2_DMA_RX	UART2 receive request
S_DMA_52	UART3_DMA_TX	UART3 transmit request
S_DMA_53	UART3_DMA_RX	UART3 receive request
S_DMA_54	UART4_DMA_TX	UART4 transmit request
S_DMA_55	UART4_DMA_RX	UART4 receive request
S_DMA_56	MMC4_DMA_TX	MMC4 transmit request
S_DMA_57	MMC4_DMA_RX	MMC4 receive request
S_DMA_58	MMC5_DMA_TX	MMC5 transmit request
S_DMA_59	MMC5_DMA_RX	MMC5 receive request
S_DMA_60	MMC1_DMA_TX	MMC1 transmit request
S_DMA_61	MMC1_DMA_RX	MMC1 receive request
S_DMA_62	Reserved	Reserved
S_DMA_63	sys_dma_req3	External DMA request 3 (system expansion)
S_DMA_64	MCPDM_DMA_UP	McPDM uplink request
S_DMA_65	MCPDM_DMA_DOWN	McPDM downlink request
S_DMA_66	DMIC_DMA	DMIC DMA request
S_DMA_67	C2C_SSCM_GPO2	C2C GPO line 2
S_DMA_68	C2C_SSCM_GPO3	C2C GPO line 3
S_DMA_69	SPI4_DMA_TX0	McSPI4 transmit request channel 0
S_DMA_70	SPI4_DMA_RX0	McSPI4 receive request channel 0
S_DMA_71	DSS_DSI1_DMA0	Display subsystem DSI1 request 0
S_DMA_72	DSS_DSI1_DMA1	Display subsystem DSI1 request 1
S_DMA_73	DSS_DSI1_DMA2	Display subsystem DSI1 request 2
S_DMA_74	DSS_DSI1_DMA3	Display subsystem DSI1 request 3
S_DMA_75	DSS_HDMI_DMA	Display subsystem HDMI audio request
S_DMA_76	MMC3_DMA_TX	MMC3 transmit request
S_DMA_77	MMC3_DMA_RX	MMC3 receive request
S_DMA_78	Reserved	Reserved
S_DMA_79	Reserved	Reserved
S_DMA_80	DSS_DSI2_DMA0	Display subsystem DSI2 request 0
S_DMA_81	DSS_DSI2_DMA1	Display subsystem DSI2 request 1
S_DMA_82	DSS_DSI2_DMA2	Display subsystem DSI2 request 2
S_DMA_83	DSS_DSI2_DMA3	Display subsystem DSI2 request 3
S_DMA_84	SLIMBUS1_DMA_TX0	SLIMBUS1 transmit request channel 0
S_DMA_85	SLIMBUS1_DMA_TX1	SLIMBUS1 transmit request channel 1
S_DMA_86	SLIMBUS1_DMA_TX2	SLIMBUS1 transmit request channel 2

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Table 16-5. sDMA Controller Request Mapping (continued)

DMA Request Line	Source	Description
S_DMA_87	SLIMBUS1_DMA_TX3	SLIMBUS1 transmit request channel 3
S_DMA_88	SLIMBUS1_DMA_RX0	SLIMBUS1 receive request channel 0
S_DMA_89	SLIMBUS1_DMA_RX1	SLIMBUS1 receive request channel 1
S_DMA_90	SLIMBUS1_DMA_RX2	SLIMBUS1 receive request channel 2
S_DMA_91	SLIMBUS1_DMA_RX3	SLIMBUS1 receive request channel 3
S_DMA_92	SLIMBUS2_DMA_TX0	SLIMBUS2 transmit request channel 0
S_DMA_93	SLIMBUS2_DMA_TX1	SLIMBUS2 transmit request channel 1
S_DMA_94	SLIMBUS2_DMA_TX2	SLIMBUS2 transmit request channel 2
S_DMA_95	SLIMBUS2_DMA_TX3	SLIMBUS2 transmit request channel 3
S_DMA_96	SLIMBUS2_DMA_RX0	SLIMBUS2 receive request channel 0
S_DMA_97	SLIMBUS2_DMA_RX1	SLIMBUS2 receive request channel 1
S_DMA_98	SLIMBUS2_DMA_RX2	SLIMBUS2 receive request channel 2
S_DMA_99	SLIMBUS2_DMA_RX3	SLIMBUS2 receive request channel 3
S_DMA_100	ABE_DMA0	Audio back-end – request FIFO 0
S_DMA_101	ABE_DMA1	Audio back-end – request FIFO 1
S_DMA_102	ABE_DMA2	Audio back-end – request FIFO 2
S_DMA_103	ABE_DMA3	Audio back-end – request FIFO 3
S_DMA_104	ABE_DMA4	Audio back-end – request FIFO 4
S_DMA_105	ABE_DMA5	Audio back-end – request FIFO 5
S_DMA_106	ABE_DMA6	Audio back-end – request FIFO 6
S_DMA_107	ABE_DMA7	Audio back-end – request FIFO 7
S_DMA_108	Reserved	Reserved
S_DMA_109	Reserved	Reserved
S_DMA_110	Reserved	Reserved
S_DMA_111	Reserved	Reserved
S_DMA_112	Reserved	Reserved
S_DMA_113	Reserved	Reserved
S_DMA_114	Reserved	Reserved
S_DMA_115	Reserved	Reserved
S_DMA_116	Reserved	Reserved
S_DMA_117	Reserved	Reserved
S_DMA_118	Reserved	Reserved
S_DMA_119	Reserved	Reserved
S_DMA_120	Reserved	Reserved
S_DMA_121	Reserved	Reserved
S_DMA_122	Reserved	Reserved
S_DMA_123	I2C4_DMA_TX	I2C4 transmit request
S_DMA_124	I2C4_DMA_RX	I2C4 receive request
S_DMA_125	Reserved	Reserved
S_DMA_126	Reserved	Reserved

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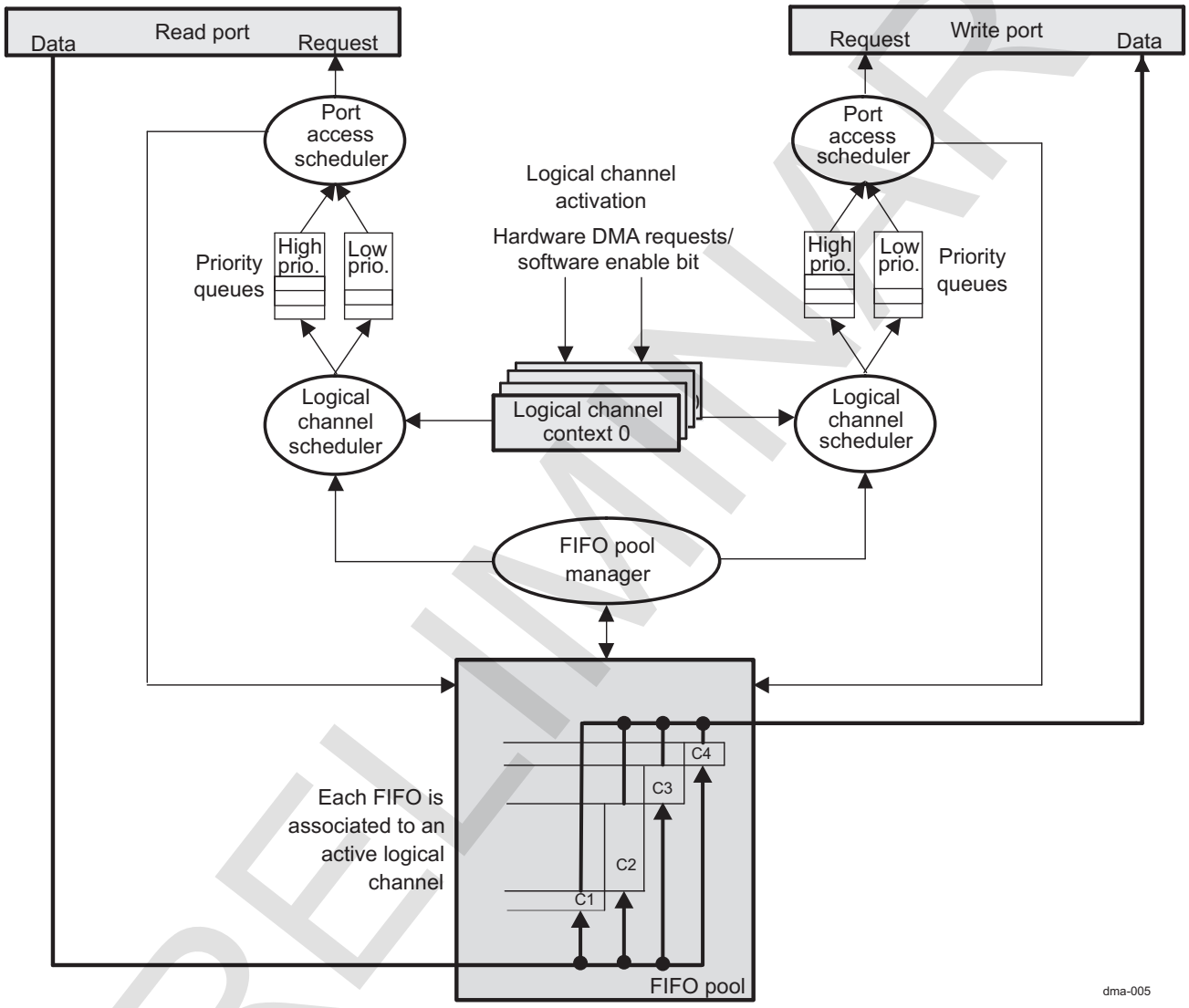
16.4 sDMA Functional Description

The sDMA module provides high-performance data transfers between memories and peripheral devices with low processor use. A DMA transfer is programmed through a logical DMA channel, which allows the transfer to be optimally tailored to the requirements of the application.

Figure 16-5 shows the sDMA controller top-level block diagram.

Figure 16-5. sDMA Controller Top-Level Block Diagram



16.4.1 sDMA Controller Power Management

Table 16-6 describes power-management features available for the sDMA controller.

NOTE:

- For information about source clock gating and sleep/wake-up transitions, see Section 3.1.1.1, *Clock Management*, in Chapter 3, *Power, Reset, and Clock Management*.
- For a description of the EnaWakeUp, IdleMode, ClockActivity, and StandbyMode features, see Section 3.1.1.1.2, *Module Level Clock Management*, in Chapter 3, *Power, Reset, and Clock Management*.

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Table 16-6. Local Power-Management Features

Feature	Registers	Description
Clock auto gating	DMA4_OCP_SYSCONFIG[0] AUTOIDLE bit	This bit allows local power optimization inside the module by gating the SDMA_ICLK clock upon the interface activity.
Slave idle modes	DMA4_OCP_SYSCONFIG[4:3] SIDLEMODE bit field	Force-idle, no-idle, and smart-idle modes are available.
Clock activity	DMA4_OCP_SYSCONFIG[9:8] CLOCKACTIVITY bit field	For configuration details, see Table 16-7.
Master standby modes	DMA4_OCP_SYSCONFIG[13:12] MIDLEMODE bit field	Force-standby, no-standby, and smart-standby modes are available.
Global wake-up enable	N/A	Feature not available
Wake-up sources enable	N/A	Feature not available

Table 16-7. Clock Activity Settings

SDMA_CLOCKACTIVITY Values	Clock State When Module is in IDLE State	
	SDMA_ICLK	SDMA_FCLK
00	Off	Off
10	Off	On
01	On	Off
11	On	On

CAUTION

Because the PRCM module cannot read CLOCKACTIVITY settings through hardware, software must ensure consistent programming between the SDMA_CLOCKACTIVITY and sDMA clock PRCM control bits. For a description of the ClockActivity feature, see Section 3.1.1.1.2, *Module Level Clock Management*, in Chapter 3, *Power, Reset, and Clock Management*.

16.4.2 sDMA Controller Interrupt Requests

DMA4 has four interrupt lines (Lj, where j = 0, 1, 2, 3). Each logical channel can request an interrupt over any line. The attachment of a channel interrupt event to one of these four external lines is programmable. Software determines whether it attaches a channel interrupt to a single IRQ line or to multiple IRQ lines.

There are two different registers per interrupt line:

- The DMA4_IRQSTATUS_Lj CH_31_0_Lj field shows the status of the different sources of interrupt. If the DMA4_IRQENABLE_Lj bit is 1, channel *i* is the source of interrupt in line *j*. In contrast to the DMA4_CSRi registers, the DMA4_IRQSTATUS_Lj registers are updated regardless of the corresponding bits in the DMA4_IRQENABLE_Lj registers.
- The DMA4_IRQENABLE_Lj CH_31_0_Lj_EN field masks/unmasks the channel interrupt. If the DMA4_IRQENABLE_Lj bit is set to 0, channel interrupt *i* of the line *j* is masked.

Each logical channel can generate a number of different interrupt events when enabled (that is, set to 1) in the DMA4_CICRi register. Each status bit is updated in the DMA4_CSRi register only when the corresponding enable bit is enabled in the DMA4_CICRi register.

To determine an interrupt source when an interrupt rises on an interrupt line L*j*:

- Identify the channel (LCH*i*) generating the interrupt.

  Read DMA4_IRQSTATUS_Lj.LCH*i* (LCH0 to LCH31). If LCH*i* = 1, channel *i* is the originator of the interrupt.
- Identify the interrupt event.

  Read the LCH*i* DMA4_CSRi. For example, if the drop event (the DMA4_CSRi[1] DROP bit) is 1, a

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request collision will occur.

The interrupt event status bit in the DMA4_CSRi register is immediately reset after it is written to 1.

The interrupt status bit in the DMA4_IRQSTATUS_Lj register is cleared after it is written to 1.

16.4.2.1 Interrupt Generation

The sDMA module has four interrupt request output lines, SDMA_IRQ_0 to SDMA_IRQ_3. One or more logical channels can be programmed to generate an interrupt request on any of these lines when any one of the maskable DMA events listed in Table 16-8 occurs.

Table 16-8. Logical DMA Channel Events

Event	Description
End of packet	A packet transfer completed.
End of block	A block transfer completed.
End of frame	A frame transfer completed.
End of super block	A super block transfer completed.
Half of frame	Half of the current frame transferred.
Start of last frame	The first element of the last frame transferred.
Transaction error	A transaction error is returned by the interconnect in either the read or write port.
Address error	An attempt was made to perform a DMA access to an address not aligned on an ES boundary. Condition to occur: if DMA4_CEN[23:0] CHANNEL_ELMNT_NBR = 0x000000 or DMA4_CFN[15:0] CHANNEL_FRAME_NBR = 0x0000 or DMA4_CSDP[1:0] DATA_TYPE = 0x3.
Supervisor transaction error	An error occurred, for example, when an unauthorized initiator (that is not a supervisor) tries to use a supervisor transfer.
Drain end	Drain is completed (DMA4_CCRi[10] WR_ACTIVE becomes 0).
Drop error	A drop event interrupt is generated when a DMA request is being serviced while a second one is asserted and a third one arrives before the second DMA request is serviced.

The logical DMA channels that generate an interrupt on a particular IRQ output are specified through the DMA4_IRQENABLE_Lj register (where *j* is the IRQ number: 0, 1, 2, or 3). The events that generate an interrupt for a particular channel can be configured through the channel DMA4_CICRi register.

When an interrupt is detected, the logical DMA channel generating the event can first be identified by reading the DMA4_IRQSTATUS_Lj register. The event causing the interrupt then can be identified by reading the interrupt status via the relevant DMA channel DMA4_CSRi register.

16.4.3 Logical Channel Transfer Overview

As Figure 16-5 shows, the sDMA module has one read port and one write port operating independently of one another. Buffering is provided between the read and write ports through a FIFO queue memory pool that is shared dynamically between the active logical channels.

- Logical channel synchronization

  A logical channel is described as hardware-synchronized when the DMA transfers are triggered by DMA requests from a hardware device. Alternatively, a logical channel is described as nonsynchronized when the DMA transfer is triggered by software.
- Logical channel activation

  A logical channel becomes active as follows:
  - For hardware-synchronized transfers, when the logical channel is enabled and the hardware DMA request line is asserted
  - For software-triggered (nonsynchronized) transfers, as soon as software enables the logical channel
- Logical channel transfer composition

  A DMA transfer is divided automatically into a number of transactions. Depending on the logical channel context configured, the transfer size, start address alignment, addressing mode, and

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configured maximum burst size, each transaction can be a single access or a burst of accesses.

- Logical channel scheduling

  When several logical channels are active at the same time, schedulers manage the read and write ports. The scheduling of logical channel transfers is similar for both read and write ports. When a logical channel becomes active, it is added to the tail of a scheduling queue. If more than one logical channel becomes active at the same time, the one with the lower number is queued first. This mechanism provides a first-come, first-serve scheduling scheme between the concurrently active logical channels.

  In addition, each read and write port has a high-priority queue and a low-priority queue. The priority bits (WRITE_PRIORITY and READ_ PRIORITY) in the logical channel DMA4_CCRi register determine whether a logical channel is queued as high or low priority. A software-configurable 8-bit priority counter gives weighting to the priority write queue. For every N (1 to 255) schedules from the priority write queue, one is scheduled from the regular write queue. A channel that is scheduled goes to the end of the queue after it completes its turn on the port. The relative weighting of the scheduling of the high-priority queue to the low priority queue is programmable from 1:1 to 1:256 through the DMA global channel register using the DMA4_GCR[23:16] ARBITRATION_RATE bit field.

  NOTE: The DMA4_GCR[23:16] ARBITRATION_RATE bit field does not depend on the DMA4_GCR[13:12] HI_THREAD_RESERVED bit field. The ARBITRATION_ RATE bit field depends on the DMA4_CCRi[26] WRITE_PRIORITY bit and the DMA4_CCRi[6] READ_PRIORITY bit.

- Read/write port access scheduling policy

  When either the read or write port becomes available, the port access scheduler selects the next logical channel for which to perform a DMA transaction from either the high- or low-priority queue.

  When the current DMA transaction (single or burst access) is complete and the full DMA transfer is not finished, the logical channel returns to the tail of the queue. Because the port access scheduling is on a per-transaction basis, a logical channel can be queued repeatedly this way several times during its block transfer.

The sDMA module can have up to four outstanding read transactions and two outstanding write transactions in the system interconnect; four read and two write thread IDs exist. For an arbitration cycle to occur, these two conditions must be met:

- At least one channel is requesting
- At least one free thread ID is available

On an arbitration cycle, the scheduler grants the highest priority channel that has an active request, allocates the thread ID, and tags this thread as busy. At a given time, a channel cannot be allocated for more than one thread ID.

NOTE: If more than one channel is active, each channel is given a thread ID for the current service only, not for the whole channel transfer.

When only one channel is enabled, only one thread is allocated for the channel. In such a situation the channel can have maximum of four outstanding commands (without getting the responses) without rescheduling the channel at the end of each transaction. Each command can be either single access (8-bit, 16-bit or 32-bit) or burst access (2 × M, 4 × M, 8 × M or 16 × M, where M can be 8, 16, or 32 bits).

When nonburst alignment is at the beginning of the transfer, the channel is rescheduled for each smaller access until burst-aligned. When the end of the transfer is not burst-aligned, the channel is rescheduled for each of the remaining smaller accesses.

For a logical channel transfer completion, when the last access is written to the destination, the logical channel becomes inactive. If enabled, an interrupt request is generated (see Section 16.4.2.1, *Interrupt Generation*).

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16.4.4 FIFO Queue Memory Pool

A FIFO queue memory pool provides buffering between the read and write ports. The hardware allocates the space dynamically to a number of FIFO queues, and each queue is associated with an active logical channel.

To avoid a memory pool overflow, if there are fewer entries in the FIFO queue memory pool than are required for the maximum configured source burst size of the next logical channel to be scheduled, the logical channel is returned to the tail of the queue, and the port access scheduler continues to search the queue until it finds a logical channel that can be scheduled.

The maximum FIFO depth that can be allocated to each individual logical channel can be limited globally through the DMA4_GCR[7:0] MAX_CHANNEL_FIFO_DEPTH bit field. This value should be configured to allow a fair allocation of the memory pool between the active channels.

A logical channel is scheduled if it has not yet reached its allocation limit, even if the access to be performed will exceed this limit. This means that the effective number of entries used by a particular logical channel is limited to the configured maximum entries per channel + channel maximum configured burst size (in words) 1.

16.4.5 Addressing Modes

A DMA transfer block consists of a number of frames (FN). Each frame consists of a number of elements (EN), and each element can have a size of 8, 16, or 32 bits (ES), as follows:

transfer block size = FN × EN × ES

The FN, EN, and ES are common for the source and destination. However, the way in which the data is represented (addressing profile/mode) is independently programmable for the source and destination devices, using one of these four addressing modes:

- Constant: The address remains the same for consecutive element accesses.
- Post-increment: The address increases by the ES, even across consecutive frames.
- Single-index: The address increases by the ES plus the element index (EI) value minus 1 (even across consecutive frames).
- Double-index: The address increases by the ES plus the EI value minus 1 within a frame. When a full frame is transferred, the address increases by the ES plus the frame index (FI) value minus 1.

The ES, EI, and FI values are expressed in bytes. The EI and FI values can be positive or negative.

When calculating the EI and FI values, it is critical to note that, after an element is accessed, the logical channel address pointer equals the address of the last byte (highest address) of the accessed element. The correct value for the EI or FI must be such that, when added to the logical channel address pointer, it results in the address of the first byte (lowest address) of the next element to be accessed.

The EI and FI values must be configured so that the address of each element in the transfer is aligned on an ES boundary.

Consequently, the single-index addressing mode with EI = 1 or double-index addressing mode with EI = 1 and FI = 1 is equivalent to post-increment addressing.

NOTE: The source and destination start addresses must also be aligned on an ES boundary.

When the address of an element to be accessed is not aligned on an ES boundary, the transfer is stopped and a misaligned address error interrupt occurs, if enabled (see Section 16.4.2.1, *Interrupt Generation*).

The DMA4_CFNi register configures the FN in a block.

The DMA4_CENi register configures the EN.

The DMA4_CSDPi register configures the ES.

The DMA4_CSSAi and DMA4_CDSAi registers configure the source and destination start addresses.

The DMA4_CCRi register configures the source and destination addressing modes.

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The DMA4_CSEIi, DMA4_CSFIi, DMA4_CDEIi, and DMA4_CDFIi registers configure the source EI, source FI, destination EI, and destination FI, respectively.

The addressing profiles are expressed as equations as follows:

Equation 1. Constant addressing:

$$A(n + 1) = A(n)$$

Note: Constant addressing mode with DMA4 to/from DDR memory is not supported on the OMAP4460 device.
To fill DDR memory with a single value, the constant fill feature of DMA4 must be used instead of a constant addressing mode transfer.

Equation 2. Post-increment addressing:

$$A(n + 1) = A(n) + ES$$

Equation 3. Single-indexed addressing:

$$A(n + 1) = A(n) + ES + (EI\ 1)$$

Equation 4. Double-indexed addressing:

When not at the end of a frame or transfer (that is, when the element counter ≠ 0):

$$A(n + 1) = A(n) + ES + (EI\ 1)$$

When at the end of a frame but not at the end of the transfer (that is, when the element counter = 0 and the frame counter ≠ 0):

$$A(n + 1) = A(n) + ES + (FI\ 1)$$

Calculate the element and frame index as follows:

Equation 5. Element index

$$EI = [(Stride\ EI\ 1) * ES] + 1$$

Equation 6. Frame index

$$FI = [(Stride\ FI\ 1) * ES] + 1$$

where:

A(n): Byte address of the element *n* within the transfer.

ES is in bytes, ES{1, 2, 4}.

EI is in bytes, specified in a configuration register, 32768 EI 32767.

Stride EI: The difference in the number of elements between the start of the current element *n* to the start of next element, *n+1*.

Element counter: A counter that is (re)initiated with the number of elements per frame or per transfer. Decreased by 1 for each element transferred. The initial value is configured in the register DMA channel element number, DMA4_CENi.

FI is in bytes, specified in a configuration register, 2147483648 FI 2147483647.

Stride FI: The difference in the number of elements between the start of the last element of the current frame and the beginning of the first element of the next frame.

Frame counter: A counter that is (re)initiated with the FN per transfer. Decreased by 1 for each frame transferred. The initial value is configured in the register DMA channel frame number, DMA4_CFNi.

Figure 16-6 shows how a stride EI and FI are defined. When handling complex configurations, using strides can make it easier to calculate EI and FI because you can calculate in elements instead of bytes. (This approach is used in the 90-degree clockwise image rotation example shown in Figure 16-10.) The double-index addressing example shown in Figure 16-6 uses ES = 4, EN = 2, EI = 5, FI = 5, and FN = 2.

Figure 16-6 through Figure 16-9 show examples of addressing mode configurations. Table 16-9 lists parameter values for the examples.

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Figure 16-6. Example Showing Double-Index Addressing, Elements, Frames, and Strides

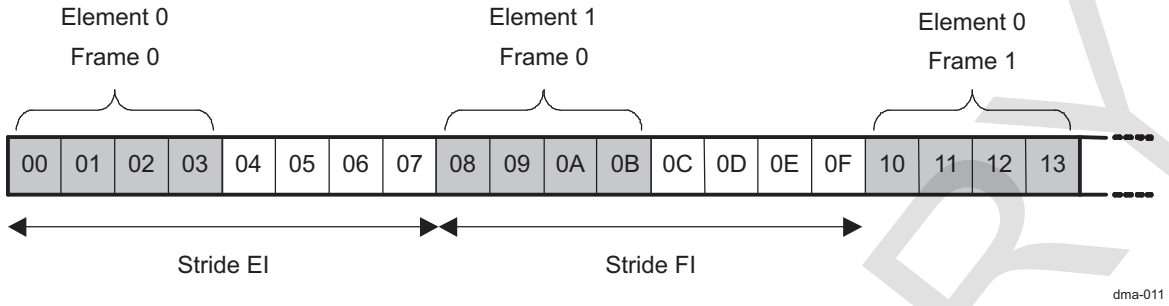

Figure 16-7. Addressing Mode Example (a)

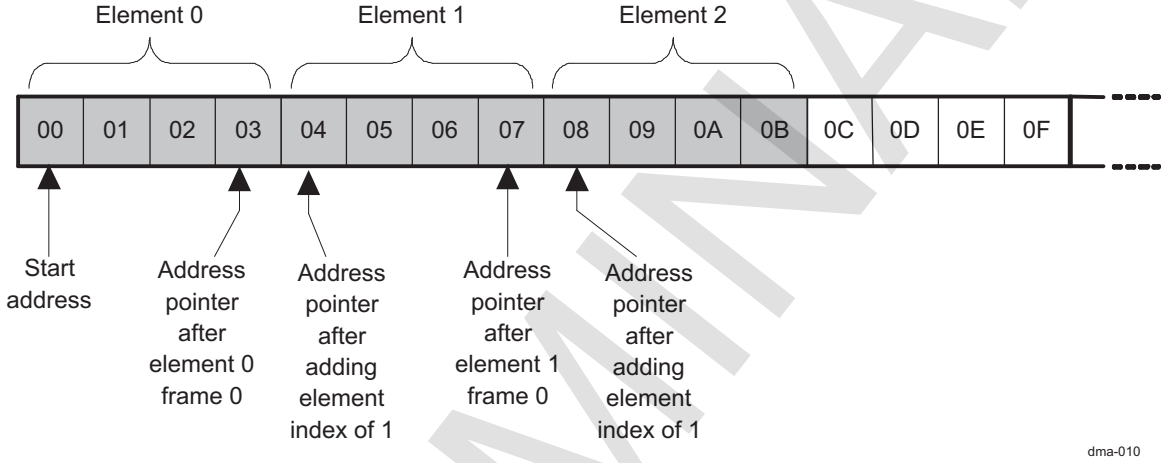

Figure 16-8. Addressing Mode Example (b)

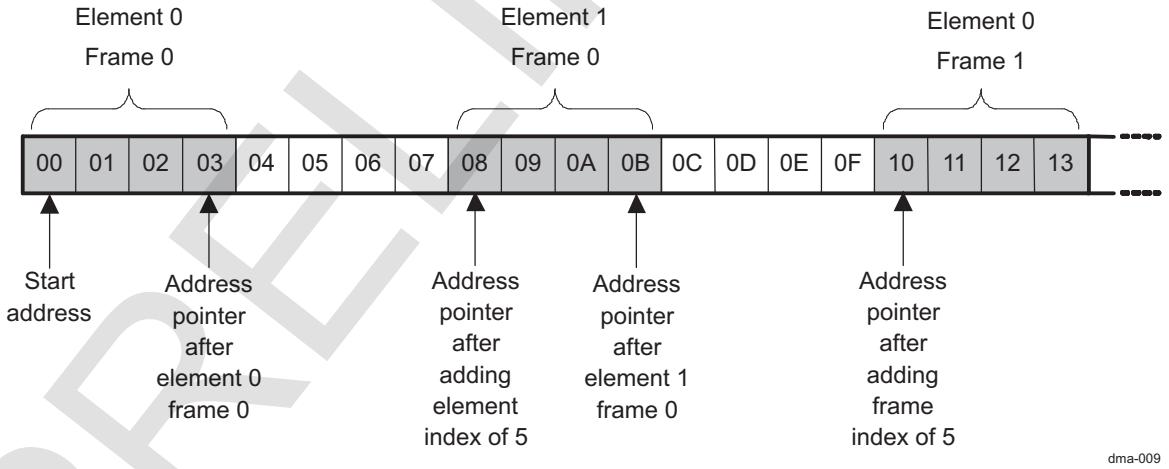

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Figure 16-9. Addressing Mode Example (c)

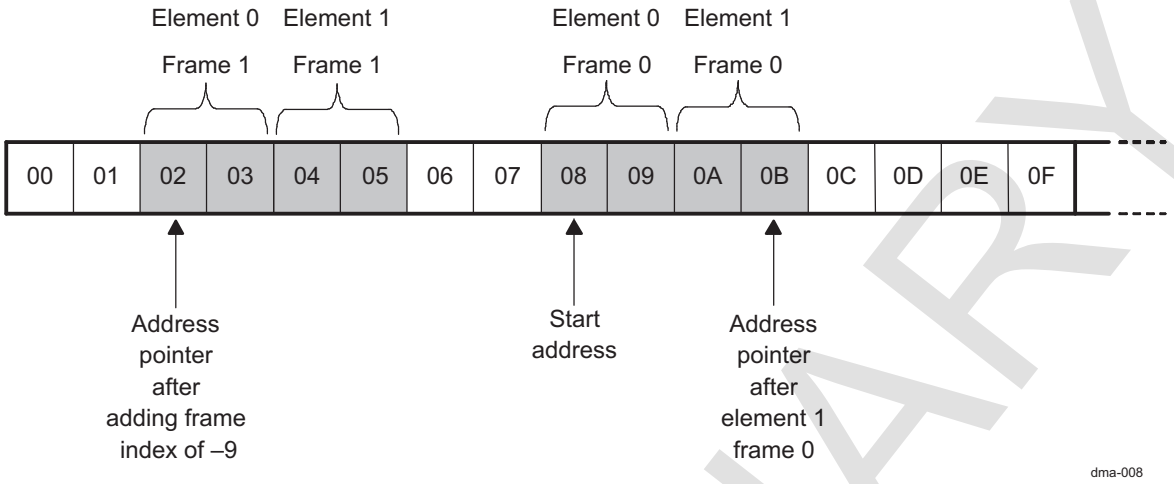

Table 16-9. Parameter Values for Addressing Mode Examples (a), (b), and (c)

Parameter	Example (a)	Example (b)	Example (c)
Addressing mode	Single index (or post-increment)	Double index	Double index
Start address	0	0	8
ES	4 (32-bit)	4 (32-bit)	2 (16-bit)
EN	3	2	2
EI	1	5	1
FN	1	2	2
Frame index	N/A	5	-9

Double indexing can occur on source (read) or destination (write). Equations for rotation of xx degrees on destination are obtained by taking equations for rotation of (360 – xx) degrees on source, and swapping the width (x) and height (y) of the image in them. The opposite is also true. Table 16-10 lists the equations for 90-, 180-, and 270-degree rotations.

Table 16-10. Equations for Rotation

		90° Rotation	180° Rotation	270° Rotation
Double indexing on destination (write)	Base address	ES*(y–1)	ES*(x*y–1)	ES*y*(x–1)
	EI	ES*(y–1) + 1	1–2*ES	1–ES*(y + 1)
	FI	1 ES*[(x–1)*y + 2]	1–2*ES	1+ES*(x–1)*y
Double indexing on source (read)	Base address	ES*x*(y–1)	ES*(x*y–1)	ES*(x–1)
	EI	1–ES*(x + 1)	1–2*ES	ES*(x–1) + 1
	FI	1+ES*(y–1)*x	1–2*ES	1 ES*[(y–1)*x + 2]

Table 16-11 and Figure 16-10 show the configuration required to perform a 90-degree clockwise rotation of a 240 × 160 pixel, 32-bit image. The EI, frame size, and FI values are configured so that the image is rotated line-by-line starting at the left end of the top line.

NOTE: The FI value for the destination is negative so that the first pixel of each subsequent line of the source image is written to the correct location at the destination.

Equation 5 and Equation 6 calculate the destination, FI and EI. The example assumes that the image lines are stored at consecutive addresses in memory, meaning that both EI and FI on the source side are 1.

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Rotations:

Section 16.5.7, *90-Degree Clockwise Image Rotation*, describes how to program an example of a 90-degree clockwise image rotation.

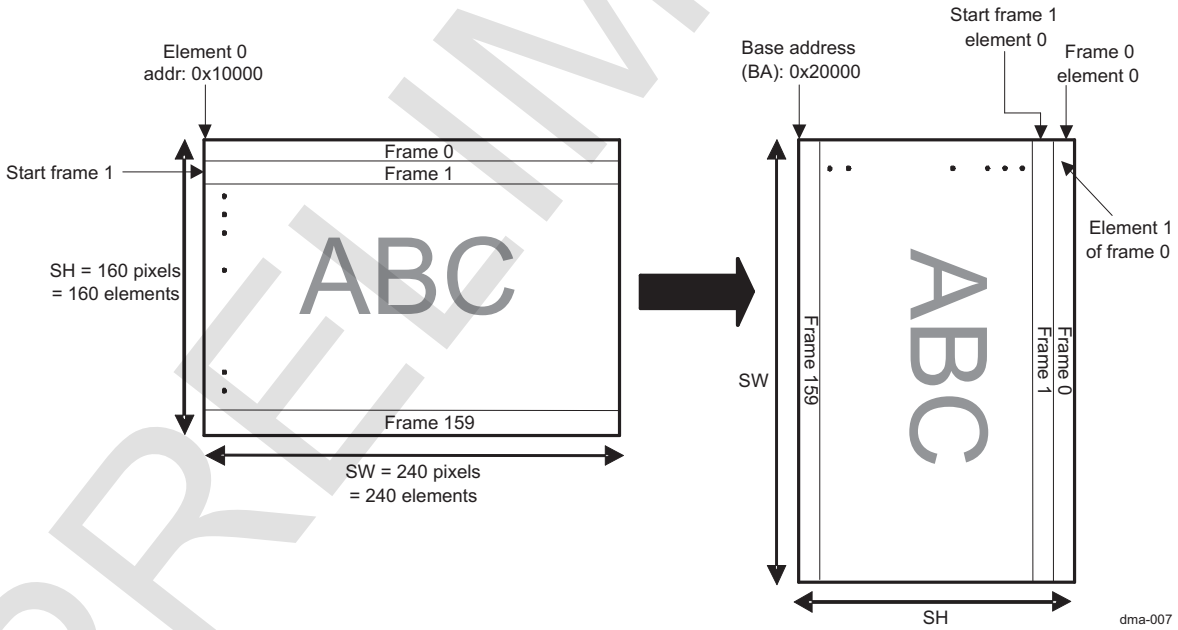
Observe that:

- One pixel = one element
- One line = one DMA frame
- Pixel size = element size = ES

Table 16-11. Example Parameter Values for a 90-Degree Clockwise Image Rotation

Parameter	Source Value	Destination Value
Bits per pixel	32	32
ES	4	4
Image width	SW	SH
Image height	SH	SW
Stride elements (stride EI)	1 element	SH
Stride frames (stride FI)	1 element	–[(SW-1)*SH + 1] = 38,241 elements
Start address	0x100000	0x200000 + (SH 1) x ES = 0x20027C
EN	SW	SW
EI	[(Stride EI 1) * ES] + 1 = 1	[(Stride EI 1) * ES] + 1 = 637
FN	SH	SH
FI	[(Stride FI 1) * ES] + 1= 1	[(Stride FI 1) * ES] + 1 = 152,967

Figure 16-10. Example of a 90-Degree Clockwise Image Rotation



16.4.6 Packed Accesses

To pack data means to group data to match the bus size, thus optimizing a transfer. When the logical channel ES is less than the DMA module read/write port size, and the addressing profile supports it (post-increment mode or single- or double-index mode with EI = 1), the number of elements to transfer in each read/write port access can be maximized by specifying that the source or destination is packed through the channel DMA4_CSDPi register. Thus:

- For a read/write port size of 32 bits, the source or destination can be configured as packed for transfer ESs of 8 bits (four elements per access) and 16 bits (two elements per access).

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- For a read/write port size of 64 bits, the source or destination can be configured as packed for transfer ESs of 8 bits (eight elements per access), 16 bits (four elements per access), and 32 bits (two elements per access).

Depending on the start address and transfer length, the first or last packed access can be only partially filled. This is indicated to the source or destination using the byte-enable signals.

16.4.7 Burst Transactions

Transfer performance can be improved so that the source or destination and addressing profile supports it. This can be achieved by configuring the logical channel to perform burst transactions consisting of multiple instead of single accesses. The channel can be programmed to use burst sizes equal to 16, 32, or 64 bytes through the DMA4_CSDPi register, with the read burst size programmable independently of the write burst size. Typically, the optimal burst size is 64 bytes (16 accesses for a 32-bit read/write port size or 8 accesses for a 64-bit read/write port size).

To obtain the maximum benefit from burst transactions, the source and destination start addresses must be aligned with the burst size. If this is not the case, the start of the transfer can consist of a number of smaller (single or burst) transactions until the first burst size boundary is reached.

Similarly, if the end of the transfer is not aligned on a burst size boundary, the final part of the transfer can consist of a number of smaller transactions.

NOTE: If post-incrementing is used, data must be packed to DMA data-port width, to use burst.

16.4.8 Endianism Conversion

The source and destination are each specified as little-endian or big-endian through the DMA4_CSDPi register for the particular logical channel. If the endianism of the source and destination differ, and if the logical channel ES is less than the sDMA module read/write port size, an endianism conversion is applied to the data before it is written to the destination.

When transferring data between a source and a destination with different endianism, it is important to specify an ES that equals the type of data being transferred to preserve the correct data image at the destination.

In the system, endianism conversion can be performed in more than one place. It is possible to instruct the source and/or destination to lock the endianism (that is, to not perform a conversion) through the logical DMA channel DMA4_CSDPi register.

NOTE: Because the device is little-endian by construction, the sDMA endianism registers must never be set to big-endian.

If sDMA is used to execute endian conversion by the setting source and destination to different endianism values, it is important to consider that the L3 interconnect also executes endian conversion if the sDMA and the source or destination have a different data bus width.

16.4.9 Transfer Synchronization

A logical channel can be programmed for software-triggered or hardware synchronized transfers.

16.4.9.1 Software Synchronization

A transfer is software-triggered when the logical channel is set up and started by software. To specify a software-triggered transfer, set the channel DMA DMA4_CCRi[4:0] and DMA4_CCRi[20:19] bit fields to 0. The transfer starts as soon as the DMA DMA4_CCRi[7] bit is set (when it enters the scheduling process).

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16.4.9.2 Hardware Synchronization

A transfer is hardware-synchronized if the logical channel activation is driven by hardware requests from the source or destination target. A hardware-synchronized transfer is specified by configuring the DMA request line number in the channel DMA4_CCRi register to a value that corresponds to the DMA request line from the source or destination that generates the DMA requests. The DMA request numbers to be configured are specified in the DMA request mapping (see Table 16-8).

Specify the DMA request number in the DMA4_CCRi[4:0] SYNCHRO_CONTROL and DMA4_CCRi[20:19] SYNCHRO_CONTROL_UPPER bit fields. After the DMA4_CCRi[7] ENABLE bit is set, the logical channel becomes enabled but not activated (it does not enter the scheduling process), which means that channel registers are not updated until the first DMA request is received.

NOTE: The channel synchronization control registers are 1-based. For example, to enable the S_DMA_1 request, the DMA4_CCRi[4:0] SYNCHRO_CONTROL bit field must be set to 0x2 (DMA request number + 1).

NOTE: A DMA request line must not be shared between concurrently enabled DMA channels. However, a DMA request line can be shared among several chained logical channels.

For hardware synchronization, the amount of data to be transferred for each assertion of the DMA request line is configured through the frame synchronization (FS) and block synchronization (BS) bits in the logical channel DMA4_CCRi register and the DMA4_CCRi[5] FS and DMA4_CCRi[18] BS bits, respectively.

The amount of data can be any of the following:

- A single element transfer: A complete element defined by data type. For example, 8/16/32 bits are transferred in response to a DMA request.
- A full frame: A complete frame of several elements is transferred in response to a DMA request.
- A full block (a full channel transfer): A complete block of several frames is transferred in response to a DMA request.
- A full packet (a full channel transfer): A complete packet of several elements is transferred in response to a DMA request.

Packets allow the size of each part of the full DMA transfer to be configured independently of the organization of the data to be transferred (typically a number of elements). This can be useful when the source or destination has a buffer (such as a FIFO queue) with a size unrelated to the frame size of the transfer. The packet size then can be set to the size of the buffer.

Packet transfer must be used only where the source or destination is addressed in constant addressing mode, because FI registers are reused to specify the packet size.

To support the burst mode, the logical channel must also be configured in target-port packed access mode.

The packet size is configured based on the DMA4_CCRi[24] SEL_SRC_DST_SYNC bit through either the channel DMA4_CDFIi register (source synchronized) or the DMA4_CSFIi register (destination synchronized).

When the logical channel transfer block is not an exact multiple of the packet size, the final packet consists of the remaining elements in the transfer, using burst or single accesses to complete the block transfer.

The maximum transfer size, regardless of the packet size, is always as follows:

Block_size = Number_of_Frame_in_Block * Number_of_Element_in_Frame * Element_Size

- Synchronized at the source

  The DMA module optimizes the transfer with respect to the number and size of burst transactions for the given source and destination addressing profiles and configured maximum burst sizes. When writing to the destination is slower than reading from the source, data is buffered in the channel FIFO queue. If the transfer is packet-synchronized at the source, the end-of-packet interrupt is disabled (see Section 16.4.13, *Reprogramming an Active Channel*).

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For a source synchronized transfer, buffering can be enabled or disabled by setting the DMA4_CCRi[25] BUFFERING_DISABLE bit. For a packet source synchronization with buffering disabled and the packed/burst across the packet boundary, the last packed/burst write transaction is split in optimized smaller accesses to complete the packet transfer size. However, for a packet source synchronized transfer with buffering enabled and with the packed/burst across the packet boundary, the DMA module waits for the next DMA request(s) to read enough data to issue an atomic packed/burst write transaction (assuming that the address is packed/burst aligned).

NOTE: Buffering is not performed between frames, even if it is enabled. If the packed/burst is across the frame boundary, the last packed/burst write transaction is split in optimized smaller accesses to complete the frame transfer size.

- Synchronized at the destination

  The performance of a hardware-synchronized transfer can be improved by using the prefetch mode, enabled through the channel DMA4_CCRi[23] PREFETCH bit. Data is prefetched on the read port side before the DMA request received and buffered in the FIFO queue. Up to a full transfer block can be prefetched, although this can be limited by the specified maximum channel FIFO queue depth (see Section 16.4.4, *FIFO Queue Memory Pool*).

  Buffering disable is not allowed for a destination-synchronized transfer.

NOTE: Behavior is undefined when prefetch is enabled and a transfer is synchronized to the source.

Regardless of whether buffering is enabled, the last transaction in the frame or in the block is write nonposted (WNP) even if the write mode is specified as write last nonposted (WLNP; the DMA4_CSDPi[17:16] WRITE_MODE bit field = 0x2). However, in a packet synchronization mode, the last transaction of each packet in the transfer is WNP only if the buffering disable is on (even if the write mode is specified as WLNP).

Regardless of whether buffering is enabled, the packet interrupt is not generated in the packet source synchronized mode.

CAUTION

The DMA4_CCRi[25] BUFFERING_DISABLE bit must be filled with an allowed value, as specified in Table 16-12.

Table 16-12. Buffering Disable

	BUFFERING_DISABLE (0: Buffering enable, 1: Buffering disable)	
Destination synchronized	0	Allowed
	1	Not allowed
Source synchronized	0	Allowed
	1	Allowed

- Synchronized transfer monitoring using CDAC (DMA4_CDACi):

  Context is restored only when the channel becomes active on a DMA request (not at software enable). The channel is software-enabled first, and then a DMA request is asserted followed by the first context restore.

  The CDAC register is writable; thus, the CDAC can be initialized to monitor the transfer and determine whether the transfer is started (for more information, see Section 16.5.4, *Synchronized Transfer Monitoring Using CDAC*).

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NOTE: For 16-bit transactions, start reading from or writing to the LSByte first to enable the register update. This is not an issue for 32-bit read-write transactions.

16.4.10 Thread Budget Allocation

When several concurrent channels are latency critical and hardware synchronized, a specific latency cannot be ensured until the target is served. This situation occurs when the number of concurrent channels is greater than the number of available threads.

NOTE: Four threads are available on the read port, and two threads are available on the write port.

For a hardware-synchronized transfer (memory to peripheral), a minimum bandwidth for a latency-critical transfer must be ensured to avoid collisions between two hardware requests.

Because it is latency critical, the software user is responsible for the following:

- Programming the synchronized channel as a high-priority channel
- Reserving one or several threads for high-priority channels

The proposed implementation is as follows (see Section 16.5.5, *Concurrent Software and Hardware Synchronization*):

Prevent the regular channel queue from exceeding more than a programmable (3, 2, or 1) number of threads on the read port and no more than one thread on the write port. This number can be set in the global register DMA4_GCR[13:12] .

The thread reservation is programmable for maximum use of thread resources for concurrent, low-priority channel transfer. Programmability can also allow a partial throughput control by limiting in software the number of concurrent outstanding requests that break the pipelining.

Depending on the DMA4_GCR [13:12] value, the following threadID on the read/write ports are allocated for a high-priority channel:

Read port priority thread reservation:

- DMA4_GCR[13:12] = 0x0 = No ThreadID is reserved for high-priority channels.
- DMA4_GCR[13:12] = 0x1 = Read ThreadID 0 is reserved for high-priority channels.
- DMA4_GCR[13:12] = 0x2 = Read ThreadID 0 and Read ThreadID 1 are reserved for high-priority channels.
- DMA4_GCR[13:12] = 0x3 = Read ThreadID 0, Read ThreadID 1, and Read ThreadID 2 are reserved for high-priority channels.

Write port priority thread reservation:

- DMA4_GCR[13:12] = 0x0 = No ThreadID is reserved for high-priority channels
- DMA4_GCR[13:12] = 0x1 = Write ThreadID 0 is reserved for high-priority channels.
- DMA4_GCR[13:12] = 0x2 = Write ThreadID 0 is reserved for high-priority channels.
- DMA4_GCR[13:12] = 0x3 = Write ThreadID 0 is reserved for high-priority channels.

Regardless of whether the enabled channels are high priority, only the setting of the DMA4_GCR[13:12] value forces the thread reservation to these values. Set the appropriate value to avoid losing threads using only regular channels.

To have an independent read and write priority context, a per-channel bit (DMA4_CCRi[26]) is added for write priority, and the previous priority bit becomes read priority bit (DMA4_CCRi[6]).

NOTE: The device has one priority bit per logical channel, not one priority bit per port.

16.4.11 FIFO Budget Allocation

To avoid fully occupying the FIFO with a high-priority transfer while low-priority channels wait in the

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arbitration queue, two separate FIFO budgets are specified: one for high-priority channels and one for low-priority channels. This is defined in the DMA4_GCR register, allowing the user to share the FIFO budget between the low- and high-priority channels. The amount of the FIFO allocated by the low- and high-priority channels is fixed by the value set in the DMA4_GCR[15:14] HI_LO_FIFO_BUDGET field. The maximum channel FIFO depth is limited by the HI_LO_FIFO_BUDGET field as follows:

If the channel is low priority:

- When HI_LO_FIFO_BUDGET = 0x1, then low priority cannot exceed 75 percent of the total FIFO.
- When HI_LO_FIFO_BUDGET = 0x2, then low priority cannot exceed 25 percent of the total FIFO.
- When HI_LO_FIFO_BUDGET = 0x3, then low priority cannot exceed 50 percent of the total FIFO.

If channel is high priority

- When HI_LO_FIFO_BUDGET = 0x1, then high priority cannot exceed 25 percent of the total FIFO.
- When HI_LO_FIFO_BUDGET = 0x2, then high priority cannot exceed 75 percent of the total FIFO.
- When HI_LO_FIFO_BUDGET = 0x3, then high priority cannot exceed 50 percent of the total FIFO.

The user must perform the following equation:

- For a high-priority channel: (Per_Channel_Maximum FIFO Depth + 1) x Number of High Channel = High Budget FIFO
- For a low-priority channel: (Per_Channel_Maximum FIFO Depth + 1) x Number of Low Channel = Low Budget FIFO

NOTE: Ensure that *Number of High Channel* means *Number of Active High-Priority Channel* and that *Number of Low Channel* means *Number of Active Low-Priority Channel*.

16.4.12 Chained Logical Channel Transfers

Chaining multiple logical channels permits transfers consisting of multiple parts to be executed without repeated software intervention. This results in better performance than the alternative of software setting up and starting each transfer separately. Each part of a chained transfer can have the data addressed in a different manner that permits the programming of a variety of complex transfers. For example:

- Interlaced video data with one logical channel configured to transfer the even lines and another logical channel configured to transfer the odd lines
- Protocol headers with a separate DMA4 channel configured to transfer each field in the header

Channels can be chained through each channel DMA4_CLNK_CTRLi register. When the transfer for the first channel completes, the next channel in the chain is enabled. The number of channels in the chain that are configured for hardware-synchronized transfers is flexible (although typically it may be all, none, or simply the first one). The DMA request line number must be set to 0 to specify that any or all of the channels in a chain are software-triggered or nonsynchronized.

The last channel in a chain can be chained to the first channel to create a continuously looping chain. The continuously looping transfer can be stopped on the fly at a specific channel by disabling the DMA4_CLNK_CTRLi[15] ENABLE_LNK bit. The looping transfer stops after the specified channel transfer is complete.

NOTE: A DMA request line must not be shared between concurrently enabled DMA channels. However, a DMA request line can be shared between several chained logical channels.

For more information about the programming model, see Section 16.5, *sDMA Basic Programming Model*.

16.4.13 Reprogramming an Active Channel

A currently active logical DMA channel can be disabled through the DMA4_CCRi[7] ENABLE bit. When an ongoing transaction is complete and the read-active and write-active bits in the DMA4_CCRi register (DMA4_CCRi[9] RD_ACTIVE and DMA4_CCRi[10] WR_ACTIVE) are reset, the channel can be reprogrammed for a new transfer.

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16.4.14 Packet Synchronization

A packet transfer notion is related to the behavior of some peripherals, which have certain buffering capability and requires to transfer the buffer content once an element number threshold is reached (a hardware DMA request is generated). To associate a frame synchronization to each DMA request is possible, but this limits the maximum transfer size. Indeed the maximum transfer size is proportional to the FIFO depth of the peripheral:

maximum_transfer_size =peripheral_FIFO_depth x number_of_frame_in_block

The packet synchronization allows to dissociate the transfer size from the FIFO depth of the peripheral. Only Constant addressing mode is allowed on a read port or a write port if source target or destination target is packet synchronized respectively.

Example:

Consider a camera interface with a FIFO_depth of 128 words and a FIFO_element_number_threshold of 128, and a picture to transfer with a size 320 lines by 240 columns. If frame synchronization is associated with each DMA request then the maximum transfer size that can be performed is $128x2^{16}$ words. In this case, a frame is 128-word long, which does not fit the size of a line, and it is not possible to generate an interrupt at the end of line. However, by introducing the packet transfer notion, which is related to the peripheral FIFO behavior/structure, the maximum transfer size (maximum_transfer_size = 2^{24} x 2^{16} words) is independent of both peripheral_FIFO_depth and FIFO_element_number_threshold. This allows a long-enough transfer within one channel context and rotation operation on a large image format.

The main features of DMA Packet transfer are as follows:

- DMA Packet_Data_Size for each DMA Request: The Peripheral_element_number_threshold (the number of elements in a packet) shares the DMA4_CSFIi and DMA4_CDFIi configuration registers. If the peripheral is the source target, the addressing mode is constant, and the DMA4_CSFIi[15:0] bit field is used to specify the packet data size in the DMA4_CSFIi register. The user must set the DMA.SDMA4_CCRi[24] SEL_SRC_DST_SYNC bit to 1. If the peripheral is the destination target, the addressing mode is constant, the DMA4_CDFIi[15:0], is used to specify the packet data size (PKT_ELNT_NBR), and the bit field [31:16] is unused. To specify the packet data size in the DMA4_CDFIi register, the user must set the DMA4_CCRi[24] SEL_SRC_DST_SYNC bit to 0.

  NOTE: The packet size can be a submultiple or non-submultiple of a frame size. If DMA Packet_Data_Size is aligned on the DMA channel block data size boundary, then DMA transfers the last data in the channel block boundary and stops at the block boundary for the last packet DMA Request. If the Packet_Data_size is not aligned on the block boundary, the remaining data smaller than a packet size are transferred using burst or single accesses to complete the block.

- DMA Packet_Data_Transfer does not affect DMA channel capabilities in term of packing and bursting.

  The packet synchronization mode is active when DMA4_CCRi[5] FS = DMA4_CCRi[18] BS = 1. Then:

  – If DMA4_CCRi[24] SEL_SRC_DST_SYNC = 0, the DMA4_CDFIi[15:0] bit field gives the number of elements in the packet and the DMA4_CDFIi[31:16] bit field is unused for the packet size.

  – If DMA4_CCRi[24] SEL_SRC_DST_SYNC = 1, the DMA4_CSFIi[15:0] bit field gives the number of element in the packet and the DMA4_CSFIi[31:16] bit field is unused for the packet size.

  NOTE: The maximum transfer size, regardless of the packet size, is always:

  Block_size = Number_of_Frame_in_Block x Number_of_Element_in_Frame x Element_Size.

  If DMA channel packet/burst access is across the packet boundary, the DMA hardware automatically splits this packing/burst access into multiple smaller accesses that are aligned on the packet boundary. Otherwise, the DMA transfers data as a usual packing/burst access.

16.4.15 Graphics Acceleration Support

The sDMA supports two graphic acceleration features: transparent copy and constant fill.

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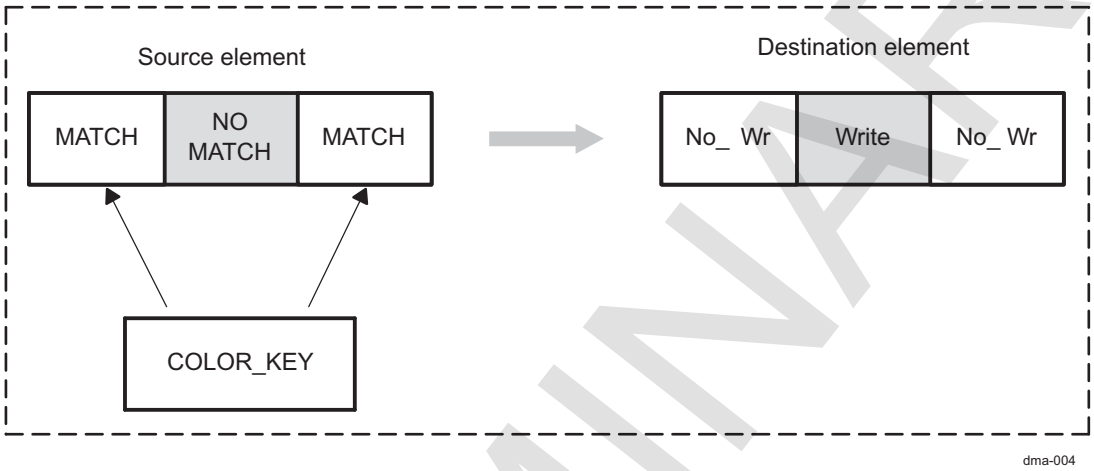
Only one of these features can be enabled at a time through the DMA4_CCRi register for the particular logical DMA channel.

The transparent copy feature enables specification of a particular color through the DMA4_COLORi register so that when it is recognized in the data from the source, it is not copied to the corresponding location in the destination but instead leaves the data in the corresponding location in the destination as it is.

Figure 16-11 shows the 2-D graphic transparent color block diagram.

Figure 16-11. 2-D Graphic Transparent Color Block Diagram



The constant fill feature provides the ability to specify a particular color through the DMA4_COLORi register for every specified location in the destination. In this case, the transfer consists only of writing to the destination without reading from a source.

Both features support 8, 16, and 24 bpp, depending on what is specified as the DMA transfer ES through the DMA4_CSDPi register. An ES of 32 bits corresponds to 24 bpp. During a 32-bit (24 bpp) transfer, the 8 most-significant bits (MSBs) ([31:24]) are 0. Both features are compatible with packed and burst transactions.

16.4.16 Supervisor Modes

A logical DMA channel can be configured to operate in supervisor mode through the DMA4_CCRi[22] SUPERVISOR bit. This must be done using supervisor access. Once a channel is configured in supervisor mode, the channel configuration is protected from nonsupervisor accesses. All DMA transactions on a supervisor channel are supervisor transactions.

16.4.17 Posted and Nonposted Writes

A logical channel can be configured in its DMA4_CSDPi[17:16] bits to use one of three write access handshake modes for the destination:

- Nonposted write: Each write must complete before transfer can continue or complete.
- Posted write: Transfer continues without waiting for each write to complete (may improve performance with slow devices).
- Posted with final write nonposted: Transfer continues without waiting for each write to complete, but final write completes before transfer can complete.

16.4.18 Disabling a Channel During Transfer

When a channel is disabled during a transfer, the channel undergoes an abort, unless it is hardware-source-synchronized with buffering enabled (DMA4_CCRi[25] BUFFERING_DISABLE = 0). If this is the case, the FIFO is drained to prevent the loss of data. For more information about this feature, see Section 16.4.19, *FIFO Draining Mechanism*.

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16.4.19 FIFO Draining Mechanism

When a source-synchronized channel is disabled during a transfer, the current hardware request (element/packet/frame/block) service completes and the channel DMA4_CCRi[9] RD_ACTIVE bit is set to 0, which means the channel is not active on the read port. The remaining data in the corresponding disabled channel FIFO is drained onto the write port and transferred to the programmed destination as in normal transfer.

At the end of the draining the DMA4_CCRi[10] WR_ACTIVE bit is set to 0 (channel is no longer active on the write port) and if the DMA4_CICRi[12] DRAIN_END_IE is set to 1, the DMA4_CSRi[12] DRAIN_END status bit is updated and an interrupt is generated.

Once a channel is disabled during a transfer, it must wait for the DMA4_CCRi[9] RD_ACTIVE and DMA4_CCRi[10] WR_ACTIVE bits to become 0 before being reenabled for a new transfer. The FIFO drain for a channel occurs only in the following cases:

- If the channel is a source synchronized channel and DMA4_CCRi[25] BUFFERING_DISABLE = 0 and
- If the channel is not a solid fill channel and
- If the channel is not a transparent and copy channel and
- If the channel is a hardware, synchronized channel

NOTE: For a self-linked or chain-linked channel, the user must disable the DMA4_CLNK_CTRLi[15] ENABLE_LINK bit before disabling the channel.

In all other cases, the channel undergoes an abort.

16.4.20 Linked List

16.4.20.1 Overview

The sDMA supports the logical transfer-descriptor loader feature. A transfer descriptor represents a set of values that maps to a set of logical channel configuration registers.

A logical channel transfer descriptor can be loaded by DMA from memories, and then successive transfer descriptors can be autonomously loaded based on a linked-list scheme. This enables DMA4 scatter-gather transfers with minimum MPU support by removing successive channel configuration processing and associated interrupt handling overheads. It also optimizes DMA4 channel resources by enabling efficient transfer serialization on a single logical channel versus concurrent (multiple) logical channel use.

Different types of transfer descriptors are supported (full or partial logical channel configuration registers are set). This optimizes the memory size required for storing a long linked list, because parameter changes are limited to only a few logical channel configuration registers.

16.4.20.2 Link-List Transfer Profile

A linked-list transfer can be seen as a super-block transfer (where the block is composed of FN frames and each frame includes EN elements). The block size (FN x EN x ES) can be changed in the linked list by loading an updated transfer descriptor.

The end of the super block is signaled in the last descriptor associated with the last block. Generally, for a given link-list transfer, the logical channel is set at the beginning of the transfer and the logical channel configurations for the subsequent blocks are slightly changed. Thus, the descriptor can be limited to an update of only few parameters, such as FN or EN. This assumes that the content of unmodified registers is preserved when a new descriptor is loaded.

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A transfer descriptor is composed of a set of channel configuration register values with the addition of the next-descriptor pointer register (DMA4_CNDPi) and a channel-descriptor parameter register (DMA4_CDPi) . The next-descriptor pointer is the 32-bit address pointer from where the next transfer descriptor is to be loaded. The next-descriptor pointer is mapped depending on the descriptor type (1, 2, or 3).

16.4.20.3 Descriptors

A transfer descriptor is a set of values that maps to a set of logical channel configuration registers. The descriptor contains the parameters associated with a transfer profile (transfer size, source or destination addresses, etc). Four different types of transfer descriptors are supported to optimize the memory size required to store a long linked list and to minimize MPU use to create and maintain the descriptor list.

A transfer descriptor is a list of 32-bit values. A descriptor must be 32-bit aligned in memory. Only the 30 least-significant bits (LSBs) of the next-descriptor address pointer are updated from the descriptor, and the DMA4 forces the 2 LSBs to 0 on generation of the pointer address. The descriptor size is variable, depending on the descriptor type and the Nxt_Dv and Nxt_Sv bit fields.

Transfer descriptor bit mapping is the same as DMA4 logical-channel configuration register bit mapping, with the following exceptions:

- Src_Element_index and Dst_Element_index are concatenated in the same 32-bit location.
- DMA4_CICRi (interrupt event mask)
- CFN (frame number)
- Bit fields:
  - P: Corresponds to the PAUSE_LINK_LIST bit:
    - When set to 1 in the descriptor, the channel is suspended when the descriptor load completes.
    - The user must not set the PAUSE_LINK_LIST bit through the configuration port. Otherwise, behavior is undefined.
    - When set to 0 (through the configuration port) after pause, the linked-list channel resumes its transfer (descriptor load or data load).
  - B: Corresponds to the end-of-block enable bit (BLOCK_IE) of the DMA4_CICRi register; valid only for type 3. This value is don't care for descriptor types 1 and 2, where DMA4_CICRi is fully specified.
  - Nxt_Dv, Nxt_Sv: Mapped in the DMA4_CDPi register. They indicate one of the following possibilities:
    - Next descriptor contains an updated destination or source address.
    - Next descriptor does not update the source or destination address, but increments the last source or destination address (from the end of the last transfer).
    - The next source address and/or destination address are the last valid ones in the configuration memory. This means that the corresponding location in the configuration memory is not updated (assuming that they were initialized at least once in the past). This is also called wrapping addressing.
  - Next_Descriptor_Type: Specifies the next descriptor type that corresponds to the NEXT_DESCRIPTOR_TYPE bit field in the DMA4_CDPi register

16.4.20.3.1 Type 1

A type 1 descriptor includes the overall channel configuration register value to be loaded (global registers are not part of the type 1 descriptor). This descriptor is used primarily when major changes are required:

- Channel read or write access profiles must be modified; for example, bursting and packing (included in the DMA4_CSDPi register)
- Attach a new DMA request to the same channel or change the priority or access privilege (included in the DMA4_CCRi register)
- Enable solid or transparent color fill (included in the DMA4_CCRi and DMA4_COLORi registers)
- Enable a channel link (included in the DMA4_CLNK_CTRLi register)

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Table 16-13 shows a type 1 descriptor.

Table 16-13. Type 1

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Ptr+ 0x2C	CCR																															
Ptr+ 0x28	CLNK_CTRL																															
Ptr+ 0x24	CSDP																															
Ptr+ 0x20	COLOR																															
Ptr+ 0x1C	Src_Frame_index/Src_Packet_size																															
Ptr+ 0x18	Dst_Frame_index/Dst_Packet_size																															
Ptr+ 0x14	Src_Element_index																Dst_Element_index															
Ptr+ 0x10	CICR (interrupt events mask)																CFN frame number															
Ptr+ 0xC	Destination_Start_Address																															
Ptr+ 0x8	Source_Start_Address																															
Ptr+ 0x4	N_type			B	Dv			Sv									Element_number															
Ptr	Next_descriptor_address_pointer																														Rsv	P

16.4.20.3.2 Type 2

A type 2 descriptor includes the overall logical channel transfer address register and transfer format register to be loaded. This descriptor enables 2D addressing linked-list transfer (for example, a multimedia application where 2D objects are moved in a link). Table 16-14 shows a type 2 descriptor with source and destination address updates. Table 16-15 shows a type 2 descriptor with one source or destination address update.

Table 16-14. Type 2 With Source and Destination Address Updates

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Ptr+ 0x1C	Src_Frame_index/Src_Packet_size																															
Ptr+ 0x18	Dst_Frame_index/Dst_Packet_size																															
Ptr+ 0x14	Src_Element_index																Dst_Element_index															
Ptr+ 0x10	CICR (interrupt events Mask)																CFN frame number															
Ptr+ 0xC	Destination_Start_Address																															
Ptr+ 0x8	Source_Start_Address																															
Ptr+ 0x4	N_type			B	Dv			Sv									Element_number															
Ptr	Next_descriptor_address_pointer																														Rsv	P

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Table 16-15. Type 2 With Source or Destination Address Update

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Ptr+ 0x18	Src_Frame_index/Src_Packet_size																															
Ptr+ 0x14	Dst_Frame_index/Dst_Packet_size																															
Ptr+ 0x10	Src_Element_index																Dst_Element_index															
Ptr+ 0xC	CICR (interrupt events Mask)																CFN frame number															
Ptr+ 0x8	Source_Start_Address or Destination_Start_Address																															
Ptr+ 0x4	N_type			B		Dv		Sv		Element_number																						
Ptr	Next_descriptor_address_pointer																														Rsv	P

16.4.20.3.3 Type 3

A type 3 descriptor is limited to a few logical channel transfer address registers and transfer format registers to be loaded. This descriptor enables simple 1D addressing link transfer (for example, scatter-gather or ping-pong memory movement using a linked list). Table 16-16 shows a type 3 descriptor with source and destination address updates. Table 16-17 shows a type 3 descriptor with one source or address destination update.

Table 16-16. Type 3 With Source and Destination Address Updates

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Ptr+ 0xC	Destination_Start_Address																															
Ptr+ 0x8	Source_Start_Address																															
Ptr+ 0x4	N_type			B		Dv		Sv		Element_number																						
Ptr	Next_descriptor_address_pointer																														Rsv	P

Table 16-17. Type 3 With Source or Destination Address Update

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Ptr+ 0x8	Source_Start_Address or Destination_Start_Address																															
Ptr+ 0x4	N_type			B		Dv		Sv		Element_number																						
Ptr	Next_descriptor_address_pointer																														Rsv	P

16.4.20.4 Linked-List Control and Monitoring

16.4.20.4.1 Transfer Mode Setting

Four descriptor types are available in DMA4_CDPi[9:8] TRANSFER_MODE to distinguish the different transfer modes:

- DMA4_CDPi[9:8] TRANSFER_MODE = 00: The current channel is using normal mode.
- DMA4_CDPi[9:8] TRANSFER_MODE = 01: The current channel is using link-list channel mode for a type 1, 2, or 3 descriptor.

The reset value is normal mode (DMA4_CDPi[9:8] TRANSFER_MODE = 0).

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16.4.20.4.2 Starting a Linked List

Like a nonlinked-list transfer, a link transfer starts under host control by enabling the associated logical channel (set the DMA4_CCRi[7] ENABLE bit to 1). The DMA4_CDPi[10] FAST bit sets the start mode of the link-list transfer:

In nonfast-start mode, the logical channel configuration is fully initialized so that the transfer can start without descriptor loading.

In fast-start mode, the descriptor pointer and other inputs are given. The channel starts by loading the descriptor and then starts the data transfer phase.

16.4.20.4.3 Monitoring a Linked-List Progression

In addition to the DMA4_CCENi (remaining elements) and DMA4_CCFNi (remaining frames) registers that are used to monitor the transfer progress, a per-channel register, DMA4_CCDNi (channel current active descriptor number), monitors which descriptor in the list is active. The user must initialize the DMA4_CCDNi register to 0 during the initial configuration. When the DMA4_CCDNi register is updated, the DMA4_CCFNi and the DMA4_CCENi registers are updated. The user must also initialize the DMA4_CCFNi and DMA4_CCENi registers to 0xFFFF and to 0xFFFFFF, respectively, to track the effective transfer start of synchronized transfer.

16.4.20.4.4 Interrupt During Linked-List Execution

Any logical channel source of interrupt can be triggered during a linked-list execution, if the interrupt source is enabled during the initial configuration in CICR. The DMA4_CICRi register can also be updated during the linked-list execution if descriptor types 1 and 2 are used.

The use of an interrupt event in a link execution can be difficult, because the link can progress in parallel with interrupt service routine (ISR) execution. This makes it difficult to synchronize them unless system assumptions are used. The most appropriate synchronization model is to get an interrupt-only on linked-list completion, when the last transfer block is complete. This prevents the interrupt from occurring during the link execution. An end-of-super-block interrupt event available in the DMA4_CICRi and DMA4_CSRi registers can be enabled at initial configuration or when using descriptor types 1 and 2. To prevent the use of descriptor type 1 or 2 to update BLOCK_IE (full DMA4_CICRi update), a dedicated BLOCK_IE bit field is also available in a type 3 descriptor.

16.4.20.4.5 Pause a Linked List

When the channel is suspended, it remains enabled.

The pause behaves differently, depending on the transfer mode:

- Normal transfer mode: If the user sets the DMA4_CDPi[7] PAUSE_LINK_LIST bit to 1, the channel completes the current read and write transactions and then suspends the channel. The channel can be resumed by setting the channel DMA4_CDPi[7] PAUSE_LINK_LIST bit to 0.
- Linked-list type 1, 2, or 3 mode: The user must not set the DMA4_CDPi[7] PAUSE_LINK_LIST bit through the configuration port; otherwise, transfer behavior is undefined.

  A PAUSE_LINK_LIST bit (P) is set to 1 in the descriptor.

  – The channel is suspended after the descriptor load, translation, and configuration memory update are complete.
  – The linked list can be resumed by resetting the DMA4_CDPi[7] PAUSE_LINK_LIST bit (through the configuration port).

16.4.20.4.6 Stop a Linked List (Abort or Drain)

The channel can be stopped for a drain or an abort. These cases are exclusive.

16.4.20.4.6.1 Drain

- Drain conditions:

  A channel is a drain candidate if it is a hardware-source-synchronized transfer with DMA4_CCRi[25]

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BUFFERING_DISABLE = 0 and should not be doing any of the graphics operation (transparent copy or solid-color fill).

- Drain trigger:

  A drain candidate channel is drained if it is disabled (DMA4_CCRi[7] ENABLE = 0) or if it receives a transaction error on the read port.

- Drain behavior with a type 1, 2, or 3 descriptor. Drain trigger can occur in two situations:
  - During descriptor loading: Any ongoing current transaction is complete and the channel is aborted.
  - During data loading: The read is completed at the boundary of the request (element/frame/packet/block boundary), the FIFO is drained to the destination, and then a DRAIN_END interrupt can be asserted.

16.4.20.4.6.2 Abort

- Abort condition:

  A channel is an abort candidate if it is software-synchronized, hardware-destination-synchronized, solid color-fill, transparent-color fill, or hardware-source-synchronized with DMA4_CCRi[25] BUFFERING_DISABLE = 1.

- Abort trigger:

  A channel is an abort candidate if it is disabled (DMA4_CCRi[7] ENABLE = 0), if it receives a transaction error on the read or write port, or if there is a MISALIGNMENT_ERROR.

- Abort behavior with a type 1, 2, or 3 descriptor:

  If an abort trigger occurs, the channel aborts immediately after completion of current read/write transactions and then the FIFO is cleaned up.

  In type 1, 2, or 3, if an abort trigger or drain trigger occurs during the descriptor load phase, the channel aborts.

16.4.20.4.7 Status Bit Behavior

This section describes the behavior of the DMA4_CSRi[6] SYNC, DMA4_CCRi[9] RD_ACTIVE and DMA4_CCRi[10] WR_ACTIVE status bits:

- For a hardware-synchronized channel in linked-list mode, the DMA4_CSRi[6] SYNC bit becomes active (DMA4_CSRi[6] SYNC = 1) when the first data load transaction is scheduled and remains active until the last data load transaction in the block (not super block) is descheduled (DMA4_CSRi[6] SYNC = 0). The SYNC bit is not active during the descriptor load phase.
- The DMA4_CCRi[9] RD_ACTIVE bit is active during the data load phase and the descriptor load phase. It becomes active when the first read transaction is scheduled. It becomes inactive:
  - When (during the descriptor load phase) the last descriptor write request is descheduled
  - When (during the data load phase) the last read transaction in the block (not super block) is descheduled for software-synchronized transfer or destination-synchronized transfer with prefetch enabled
  - When (during the data load phase) the last read transaction in the request (element/frame/packet/block sync) is descheduled for hardware-source-synchronized transfer or hardware-destination-synchronized transfer without prefetch
- The DMA4_CCRi[10] WR_ACTIVE bit is active only during the data load phase. It becomes active when the first write transaction is scheduled and becomes inactive:
  - Until the last write transaction in the block (not super block) is descheduled and the FIFO is cleaned up for software-synchronized transfer
  - Until the last write transaction in the request (element/frame/packet/block sync) is descheduled and the FIFO is cleaned up for hardware-source-synchronized transfer (with DMA4_CCRi[25] BUFFERING_DISABLE = 0) or hardware-destination-synchronized transfer.

16.4.20.4.8 Linked-List Channel Linking

Channel linking for inter- and intra-super blocks is supported for type 1, 2, and 3 descriptors.

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Assume that CHx and CHz are linked-list channels using generic descriptors. If CHx is composed of N descriptors and CHz is composed of M descriptors, then in nonfast mode:

CHx: CHx[Data1]- CHx[DES1] - . - CHx[DESN]-CHx[DataN + 1]

CHz: CHz[Data1]- CHz[DES1] - . - CHz[DESM]-CHz[DataM + 1]

It is possible to link CHx to CHz or CHx to itself after the completion of the CHx transfer (end of super block). To do this, the user must set the DMA4_CLNK_CTRLi[15] ENABLE_LNK bit to 1 and the DMA4_CLNK_CTRLi[4:0] NEXTLCH_ID bit to z (or to x for self linking) through the last descriptor using a type 1 descriptor. The sequence is:

CHx: CHx[Data1]- CHx[DES1] - . - CHx[DESN]-CHx[DataN+1] - CHz: CHz[Data1]- CHz[DES1] - . - CHz[DESM]-CHz[DataM+1]

It is also possible to link CHx to CHz during the CHx transfer and before the end of super block. The user must set the DMA4_CLNK_CTRLi[15] ENABLE_LNK bit to 1 and the DMA4_CLNK_CTRLi[4:0] NEXTLCH_ID bit to z through descriptor p (CHx[DESp]) using a type 1 descriptor. The sequence is:

CHx: CHx[Data1]- CHx[DES1] -.- CHx[DESp]-CHx[Data(p + 1)] - CHz[Data1]- CHz[DES1] - .

The user must continue the linking until channels CHx and CHz complete their super-block transfers; otherwise, the channels remain enabled.

NOTE: In channel linking, the head of a chain can be in fast mode or nonfast mode. All channels that are not in the head of the chain can be in nonfast mode only. In self-linking, the channel cannot be in fast mode.

NOTE: If channel CHx links to CHz in the middle of the superblock transfer (remember link bit can be set through Type-1 descriptor load), CHx is disabled after the corresponding data load and enables the channel CHz.

16.4.21 Auto-Restore Feature

The auto-restore feature is introduced mainly to accelerate the restore process, which otherwise is complex and time and resource consuming. In many system applications, it is required that the modem wake up and use only a few modules to wake up, without the intervention of the main MPU (Cortex-A9 MPU). The MPU still may be in off mode; however, some modules may need to come out of off mode. The sDMA can be used to restore the register contents of these modules. The auto-restore feature consists in saving the register data into a memory (SAR RAM in the WKUP domain) that remains powered even during off mode, and then in automatically retrieving data when returning from off mode.

The restore feature is enabled by default and cannot be disabled.

Figure 16-12 is an overview of the save-and-restore mechanism using SAR RAM and SAR ROM.

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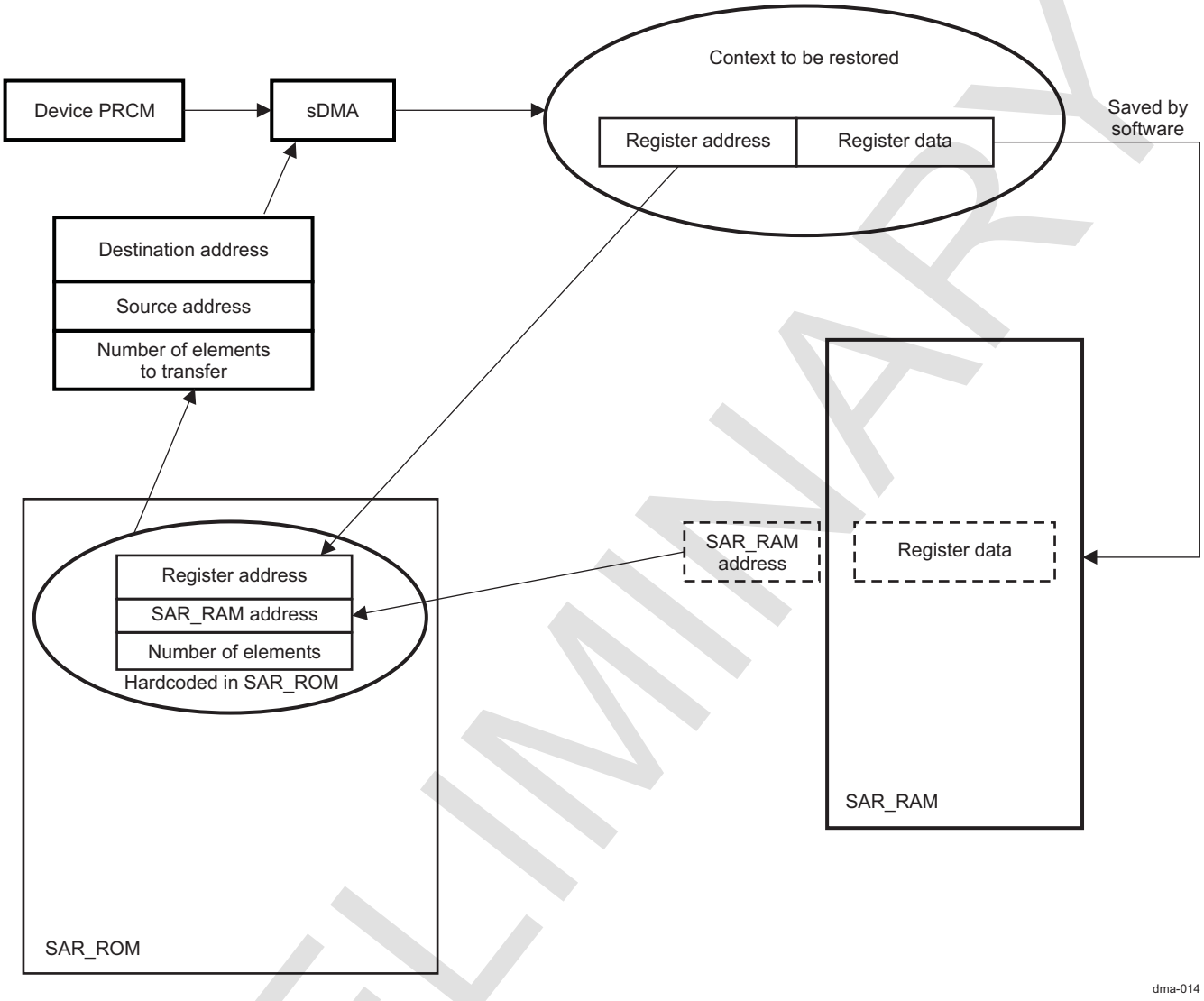
Figure 16-12. Overview of Save-and-Restore Mechanism Using SAR RAM and SAR ROM



16.4.21.1 Save Process

The save process is done entirely by software; the sDMA module normally is not involved. Software must save the data to be restored in a dedicated location in SAR RAM. To reduce the save sequence execution time, the sDMA can be used with linked-list descriptors. These save descriptors are symmetrical with regards to descriptors in the SAR ROM.

The register content to be saved can be the register value before going into off mode or a value that is required on wake up. This means that the restored register value can differ from the last value of the register before going into off mode.

The following registers are affected:

- CM1 and CM2 configuration

  Bits 0 of the CM_SHADOW_FREQ_CONFIG1 register and the CM_SHADOW_FREQ_CONFIG2 register are self-clearing and must be set at restore time. Thus, these data must always be overwritten in the SAR RAM.
- Because USBHOSTHS and USBTLL restore requires a particular sequencing, software must overwrite data read from the following registers implied in phase2a and phase 2b:
  - CM_L3INIT_HSUSBHOST_CLKCTRL_RESTORE

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– CM_L3INIT_HSUSBTLL_CLKCTRL_RESTORE
– CM_SDMA_STATICDEP_RESTORE

The USBHOSTHS and USBTLL modules must be put in a particular mode when saving (and restoring) their context. In the case of context saving, software must:

- Configure the L3INIT clock domain to SW_WKUP to ensure module transitions
- Disable both modules
- Assert the SAR_MODE pins
- Enable back both modules. Optional clocks must be kept gated
- Save both modules context
- Disable both modules
- Deassert SAR_MODE pins
- At this point, software may enable back both modules and get the L3INIT clock domain out from SW_WKUP state.

16.4.21.2 Restore Process

As explained earlier, every time modem wakes up, the MPU must not necessarily wake up. This needs an automated way of restore. For example, when mobile is in roaming, and not in active use, it needs to change base stations. For this task, the MPU need not wake up, only a few peripherals/subsystems need to be in ON mode. Before executing any task, we need to restore their register contents.

16.4.21.2.1 PRCM and sDMA interaction During Restore Phase

Restore is performed during three phases. At the end of each phase, the sDMA stops and waits for the PRCM to perform the next phase transfer. For more information, see Section 3.9.3.2, *Device Off Mode Wake-Up Sequences*, in Chapter 3, *Power, Reset, and Clock Management*.

16.4.21.2.2 sDMA Descriptors Description

The restore phase is done automatically by the sDMA. The sDMA gets the register address (destination address), number of elements to transfer, and the address of the data to transfer (Source address) from SAR ROM. As mentioned previously, the register data is stored in the SAR RAM.

The SAR ROM contains two types of descriptors the DMA-4 should use:

- Type-1 descriptors:

  Type-1 descriptors (48 bytes) are used at the beginning of each phase. In addition to the source and destination address and number of elements, these descriptors contain the required data that initializes the sDMA. Table 16-13 shows the Type-1 descriptor structure.
- Type-3 descriptors with source and destination address update:

  Type-3 descriptors (16 bytes) are used for subsequent sDMA transfers and mainly contain the source and destination address and number of elements. Table 16-16 shows the Type-3 descriptor structure.

  Figure 16-13 is an example of SAR ROM code (Type-3 descriptor).

Figure 16-13. Type-3 SAR ROM Code Example

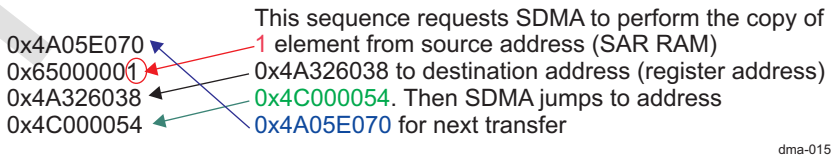

Figure 16-14 is an example of last DMA transfer (Type-3 descriptor). To indicate to the DMA that this is the last transfer, the next descriptor address must be set to 0xFFFFFFFC, as shown in the figure.

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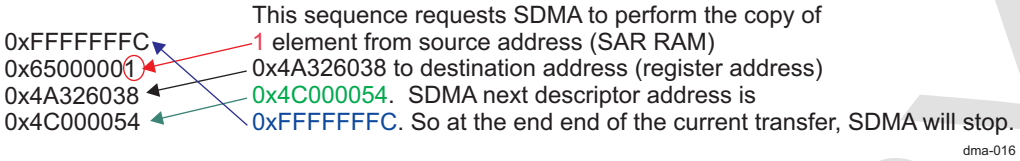
Figure 16-14. Type-3 SAR ROM Last Transfer Example



16.4.21.3 SAR RAM

The SAR RAM contains the data that needs to be maintained during off mode. The SAR RAM is split into three banks (see Table 16-18).

Table 16-18. SAR RAM Allocation

Access Mode	Bank	Address Range
Public	1 (SAR_RAM_1)	0x4A32_6000–0x4A32_6FFF (4KB)
Public, for I/O pad	2 (SAR_RAM_2)	0x4A32_7000–0x4A32_73FF (1KB)
Public	3 (SAR_RAM_3)	0x4A32_8000–0x4A32_87FF (2KB)

16.4.21.4 SAR ROM

The SAR ROM contains the list of registers that need to be saved before off mode and then restored after off mode, and where the register data is stored in SAR RAM. The SAR ROM start address is 0x4A05_E000.

When exiting off mode, PRCM automatically redirects the sDMA to address:

- 0x4A05_E000 for phase 1 (in SAR ROM)
- 0x4A05_E030 for phase 2a (in SAR ROM)
- 0x4A05_E060 for phase 2b (in SAR ROM)

The SAR ROM is built so that sDMA performs all the transfers for each phase. At the end of each phase, the sDMA stops. The PRCM module then requests to perform the next phase transfer, depending on the wake-up source.

Remarks:

- Phase 1 is always to happen; the restore mechanism is enabled by default and cannot be disabled.
- Phase 2 (2a and 2b) is to happen depending on the wake-up source from off mode. Phase 2 is not performed if C2C is the wake-up source, but it is performed for all other wake-up sources. Therefore, it is mandatory to fill the SAR RAM locations used for USB restore correctly, even if USB is not used, because the restore sequence will happen.
- The USB host restore is to be performed before the USB TLL restore.

NOTE: Some consecutive address registers cannot be saved/restored with burst. This is the case for:

- CLK1_DSS_BW_REGULATOR.L3_BW_R_BANDWIDTH and CLK1_DSS_BW_REGULATOR.L3_BW_R_WATERMARK registers
- CLK2_XXX_BW_REGULATOR.L3_BW_R_BANDWIDTH and CLK2_XXX_BW_REGULATOR.L3_BW_R_WATERMARK registers, where XXX = ISS, IVAHD, and SGX.

To avoid the failure of an sDMA transfer, the transfer of the previous registers is performed using a single sDMA transfer.

16.4.21.5 SAR RAM Memory Allocation Reserved for Save and Restore

The memory size of the SAR RAM reserved for the save-and-restore mechanism is:

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- 57 percent (2344 bytes) reserved for the SAR mechanism from SAR_RAM_1. The whole SAR_RAM_1 size is 4KB.
- 40 percent (408 bytes) reserved for the SAR mechanism from SAR_RAM_2. The whole SAR_RAM_2 size is 1KB.
- 51 percent (1052 bytes) reserved for the SAR mechanism from SAR_RAM_3. The whole SAR_RAM_3 size is 2KB.

The free part of the SAR RAM can be used by the user software to store any data that needs to be in always-on memory.

16.4.21.6 Register Mapping in SAR RAM

Table 16-19 describes the SAR_RAM_1 memory mapping.

Table 16-19. SAR_RAM_1 Memory Mapping

Order	Register Name	Register Start Address	Register End Address	Size	SAR_RAM_1 Address
1	EMIF1.EMIF_LPDDR2_NVM_CONFIG	0x4C00000C		4	0x4A326000
2	EMIF1.EMIF_SDRAM_CONFIG	0x4C000008		4	0x4A326004
3	EMIF1.EMIF_SDRAM_REF_CTRL	0x4C000010		4	0x4A326008
4	EMIF1.EMIF_SDRAM_REF_CTRL_SHDW	0x4C000014		4	0x4A32600C
5	EMIF1.EMIF_SDRAM_TIM_1	0x4C000018		4	0x4A326010
6	EMIF1.EMIF_SDRAM_TIM_1_SHDW	0x4C00001C		4	0x4A326014
7	EMIF1.EMIF_SDRAM_TIM_2	0x4C000020		4	0x4A326018
8	EMIF1.EMIF_SDRAM_TIM_2_SHDW	0x4C000024		4	0x4A32601C
9	EMIF1.EMIF_SDRAM_TIM_3	0x4C000028		4	0x4A326020
10	EMIF1.EMIF_SDRAM_TIM_3_SHDW	0x4C00002C		4	0x4A326024
11	EMIF1.EMIF_LPDDR2_NVM_TIM	0x4C000030		4	0x4A326028
12	EMIF1.EMIF_LPDDR2_NVM_TIM_SHDW	0x4C000034		4	0x4A32602C
13	EMIF1.EMIF_PWR_MGMT_CTRL	0x4C000038		4	0x4A326030
14	EMIF1.EMIF_PWR_MGMT_CTRL_SHDW	0x4C00003C		4	0x4A326034
15	EMIF1.EMIF_L3_CONFIG	0x4C000054		4	0x4A326038
16	EMIF1.EMIF_PERF_CNT_CFG	0x4C000088		4	0x4A32603C
17	EMIF1.EMIF_PERF_CNT_SEL	0x4C00008C		4	0x4A326040
18	EMIF1.EMIF_READ_IDLE_CTRL	0x4C000098		4	0x4A326044
19	EMIF1.EMIF_READ_IDLE_CTRL_SHDW	0x4C00009C		4	0x4A326048
20	EMIF1.EMIF_IRQENABLE_SET_SYS	0x4C0000B4		4	0x4A32604C
21	EMIF1.EMIF_IRQENABLE_SET_LL	0x4C0000B8		4	0x4A326050
22	EMIF1.EMIF_ZQ_CONFIG	0x4C0000C8		4	0x4A326054
23	EMIF1.EMIF_TEMP_ALERT_CONFIG	0x4C0000CC		4	0x4A326058
24	EMIF1.EMIF_DDR_PHY_CTRL_1	0x4C0000E4		4	0x4A32605C
25	EMIF1.EMIF_DDR_PHY_CTRL_1_SHDW	0x4C0000E8		4	0x4A326060
26	EMIF1.EMIF_DDR_PHY_CTRL_2	0x4C0000EC		4	0x4A326064
27	EMIF2.EMIF_LPDDR2_NVM_CONFIG	0x4D00000C		4	0x4A326068
28	EMIF2.EMIF_SDRAM_CONFIG	0x4D000008		4	0x4A32606C
29	EMIF2.EMIF_SDRAM_REF_CTRL	0x4D000010		4	0x4A326070
30	EMIF2.EMIF_SDRAM_REF_CTRL_SHDW	0x4D000014		4	0x4A326074
31	EMIF2.EMIF_SDRAM_TIM_1	0x4D000018		4	0x4A326078
32	EMIF2.EMIF_SDRAM_TIM_1_SHDW	0x4D00001C		4	0x4A32607C
33	EMIF2.EMIF_SDRAM_TIM_2	0x4D000020		4	0x4A326080
34	EMIF2.EMIF_SDRAM_TIM_2_SHDW	0x4D000024		4	0x4A326084
35	EMIF2.EMIF_SDRAM_TIM_3	0x4D000028		4	0x4A326088

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Table 16-19. SAR_RAM_1 Memory Mapping (continued)

Order	Register Name	Register Start Address	Register End Address	Size	SAR_RAM_1 Address
36	EMIF2.EMIF_SDRAM_TIM_3_SHDW	0x4D00002C		4	0x4A32608C
37	EMIF2.EMIF_LPDDR2_NVM_TIM	0x4D000030		4	0x4A326090
38	EMIF2.EMIF_LPDDR2_NVM_TIM_SHDW	0x4D000034		4	0x4A326094
39	EMIF2.EMIF_PWR_MGMT_CTRL	0x4D000038		4	0x4A326098
40	EMIF2.EMIF_PWR_MGMT_CTRL_SHDW	0x4D00003C		4	0x4A32609C
41	EMIF2.EMIF_L3_CONFIG	0x4D000054		4	0x4A3260A0
42	EMIF2.EMIF_PERF_CNT_CFG	0x4D000088		4	0x4A3260A4
43	EMIF2.EMIF_PERF_CNT_SEL	0x4D00008C		4	0x4A3260A8
44	EMIF2.EMIF_READ_IDLE_CTRL	0x4D000098		4	0x4A3260AC
45	EMIF2.EMIF_READ_IDLE_CTRL_SHDW	0x4D00009C		4	0x4A3260B0
46	EMIF2.EMIF_IRQENABLE_SET_SYS	0x4D0000B4		4	0x4A3260B4
47	EMIF2.EMIF_IRQENABLE_SET_LL	0x4D0000B8		4	0x4A3260B8
48	EMIF2.EMIF_ZQ_CONFIG	0x4D0000C8		4	0x4A3260BC
49	EMIF2.EMIF_TEMP_ALERT_CONFIG	0x4D0000CC		4	0x4A3260C0
50	EMIF2.EMIF_DDR_PHY_CTRL_1	0x4D0000E4		4	0x4A3260C4
51	EMIF2.EMIF_DDR_PHY_CTRL_1_SHDW	0x4D0000E8		4	0x4A3260C8
52	EMIF2.EMIF_DDR_PHY_CTRL_2	0x4D0000EC		4	0x4A3260CC
53	RESTORE_CM2. CM_MEMIF_CLKSTCTRL_RESTORE	0x4A009E0C		4	0x4A3260D0
54	RESTORE_CM1. CM_CLKSEL_CORE_RESTORE	0x4A004E00		4	0x4A3260D4
55	RESTORE_CM1. CM_DIV_M2_DPLL_CORE_RESTORE	0x4A004E04		4	0x4A3260D8
56	RESTORE_CM1. CM_DIV_M3_DPLL_CORE_RESTORE	0x4A004E08		4	0x4A3260DC
57	RESTORE_CM1. CM_DIV_M4_DPLL_CORE_RESTORE	0x4A004E0C		4	0x4A3260E0
58	RESTORE_CM1. CM_DIV_M5_DPLL_CORE_RESTORE	0x4A004E10		4	0x4A3260E4
59	RESTORE_CM1. CM_DIV_M6_DPLL_CORE_RESTORE	0x4A004E14		4	0x4A3260E8
60	RESTORE_CM1. CM_DIV_M7_DPLL_CORE_RESTORE	0x4A004E18		4	0x4A3260EC
61	RESTORE_CM1. CM_CLKSEL_DPLL_CORE_RESTORE	0x4A004E1C		4	0x4A3260F0
62	RESTORE_CM1. CM_SSC_DELTAMSTEP_DPLL_CORE_RESTORE	0x4A004E20		4	0x4A3260F4
63	RESTORE_CM1. CM_SSC_MODFREQDIV_DPLL_CORE_RESTORE	0x4A004E24		4	0x4A3260F8
64	RESTORE_CM1. CM_CLKMODE_DPLL_CORE_RESTORE	0x4A004E28		4	0x4A3260FC
65	RESTORE_CM1. CM_SHADOW_FREQ_CONFIG2_RESTORE	0x4A004E2C		4	0x4A326100
66	RESTORE_CM1. CM_SHADOW_FREQ_CONFIG1_RESTORE	0x4A004E30		4	0x4A326104
67	RESTORE_CM1. CM_AUTOIDLE_DPLL_CORE_RESTORE	0x4A004E34		4	0x4A326108
68	RESTORE_CM1. CM_MPU_CLKSTCTRL_RESTORE	0x4A004E38		4	0x4A326010C
69	RESTORE_CM1. CM_CM1_PROFILING_CLKCTRL_RESTORE	0x4A004E3C		4	0x4A3260110

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Table 16-19. SAR_RAM_1 Memory Mapping (continued)

Order	Register Name	Register Start Address	Register End Address	Size	SAR_RAM_1 Address
70	RESTORE_CM1. CM_DYN_DEP_PRESCAL_RESTORE	0x4A004E40		4	0x4A326114
71	RESTORE_CM2. CM_L3_1_CLKSTCTRL_RESTORE	0x4A009E00		4	0x4A326118
72	RESTORE_CM2. CM_L3_2_CLKSTCTRL_RESTORE	0x4A009E04		4	0x4A32611C
73	RESTORE_CM2. CM_L4CFG_CLKSTCTRL_RESTORE	0x4A009E08		4	0x4A326120
74	RESTORE_CM2. CM_MEMIF_CLKSTCTRL_RESTORE	0x4A009E0C		4	0x4A326124
75	RESTORE_CM2. CM_L4PER_CLKSTCTRL_RESTORE	0x4A009E10		4	0x4A326128
76	RESTORE_CM2. CM_L3INIT_CLKSTCTRL_RESTORE	0x4A009E14		4	0x4A32612C
77	RESTORE_CM2. CM_L3INSTR_L3_3_CLKCTRL_RESTORE	0x4A009E18		4	0x4A326130
78	RESTORE_CM2. CM_L3INSTR_L3_INSTR_CLKCTRL_RESTORE	0x4A009E1C		4	0x4A326134
79	RESTORE_CM2. CM_L3INSTR_OCP_WP1_CLKCTRL_RESTORE	0x4A009E20		4	0x4A326138
80	RESTORE_CM2. CM_CM2_PROFILING_CLKCTRL_RESTORE	0x4A009E24		4	0x4A32613C
81	RESTORE_CM2. CM_C2C_STATICDEP_RESTORE	0x4A009E28		4	0x4A326140
82	RESTORE_CM2. CM_L3_1_DYNAMICDEP_RESTORE	0x4A009E2C		4	0x4A326144
83	RESTORE_CM2. CM_L3_2_DYNAMICDEP_RESTORE	0x4A009E30		4	0x4A326148
84	RESTORE_CM2. CM_C2C_DYNAMICDEP_RESTORE	0x4A009E34		4	0x4A32614C
85	RESTORE_CM2. CM_L4CFG_DYNAMICDEP_RESTORE	0x4A009E38		4	0x4A326150
86	RESTORE_CM2. CM_L4PER_DYNAMICDEP_RESTORE	0x4A009E3C		4	0x4A326154
87	C2C. C2C_PORTCONFIG	0x5C00000C		4	0x4A326158
88	C2C. C2C_MIRRORMODE	0x5C000010		4	0x4A32615C
89	C2C. C2C_IRQ_ENABLE_SET_1	0x5C000028		4	0x4A326160
90	C2C. C2C_FCLK_FREQ	0x5C000040		4	0x4A326164
91	C2C. C2C_RX_MAX_FREQ	0x5C000044		4	0x4A326168
92	C2C. C2C_GENI_CONTROL	0x5C000070		4	0x4A32616C
93	C2C. C2C_GENI_MASK	0x5C000074		4	0x4A326170
94	C2C.C2C_GENO_INTERRUPT	0x5C000084		4	0x4A326174
95	C2C.C2C_GENO_LEVEL	0x5C000088		4	0x4A326178
98	SYSCTRL_PADCONF_CORE.CONTROL_PADCONF_GLOBAL	0x4A1005A0	0x4A1005DB	60	0x4A32617C
99	SYSCTRL_PADCONF_CORE.CONTROL_PBIASLITE	0x4A100600	0x4A100637	56	0x4A3261B8
100	SYSCTRL_PADCONF_CORE.CONTROL_LPDDR2IO1_0	0x4A100638	0x4A100657	32	0x4A3261F0
101	SYSCTRL_PADCONF_CORE.CONTROL_BUS_HOLD	0x4A100658		4	0x4A326210

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Table 16-19. SAR_RAM_1 Memory Mapping (continued)

Order	Register Name	Register Start Address	Register End Address	Size	SAR_RAM_1 Address
102	SYSCTRL_PADCONF_CORE.CONTROL_C2C	0x4A10065C		4	0x4A326214
103	SYSCTRL_PADCONF_CORE.CONTROL_EFUSE_1	0x4A100700		4	0x4A326218
104	SYSCTRL_PADCONF_CORE.CONTROL_EFUSE_2	0x4A100704		4	0x4A32621C
105	SYSCTRL_PADCONF_CORE.CONTROL_EFUSE_4	0x4A10070C		4	0x4A326220
106	CONTROL_HWOBS_CONTROL	0x4A002350		4	0x4A326224
246	DMM.DMM_LISA_MAP_0	0x4E000040		4	0x4A326228
247	DMM.DMM_LISA_MAP_1	0x4E000044		4	0x4A32622C
248	DMM.DMM_LISA_MAP_2	0x4E000048		4	0x4A326230
249	DMM.DMM_LISA_MAP_3	0x4E00004C		4	0x4A326234
250	DMM.DMM_LISA_LOCK	0x4E00001C		4	0x4A326238
251	DMM.DMM_TILER_OR0	0x4E000220		4	0x4A32623C
252	DMM.DMM_TILER_OR1	0x4E000224		4	0x4A326240
253	DMM.DMM_PAT_VIEW0	0x4E000420		4	0x4A326244
254	DMM.DMM_PAT_VIEW1	0x4E000424		4	0x4A326248
255	DMM.DMM_PAT_VIEW_MAP_0	0x4E000440		4	0x4A32624C
256	DMM.DMM_PAT_VIEW_MAP_1	0x4E000444		4	0x4A326250
257	DMM.DMM_PAT_VIEW_MAP_2	0x4E000448		4	0x4A326254
258	DMM.DMM_PAT_VIEW_MAP_3	0x4E00044C		4	0x4A326258
259	DMM.DMM_PAT_VIEW_MAP_BASE	0x4E000460		4	0x4A32625C
260	DMM.DMM_PAT_IRQENABLE_SET	0x4E0004A0		4	0x4A326260
261	DMM.DMM_PAT_DESCR_0	0x4E000500		4	0x4A326264
262	DMM.DMM_PAT_AREA_0	0x4E000504		4	0x4A326268
263	DMM.DMM_PAT_CTRL_0	0x4E000508		4	0x4A32626C
264	DMM.DMM_PAT_DATA_0	0x4E00050C		4	0x4A326270
265	DMM.DMM_PAT_DESCR_1	0x4E000510		4	0x4A326274
266	DMM.DMM_PAT_AREA_1	0x4E000514		4	0x4A326278
267	DMM.DMM_PAT_CTRL_1	0x4E000518		4	0x4A32627C
268	DMM.DMM_PAT_DATA_1	0x4E00051C		4	0x4A326280
269	DMM.DMM_PAT_DESCR_2	0x4E000520		4	0x4A326284
270	DMM.DMM_PAT_AREA_2	0x4E000524		4	0x4A326288
271	DMM.DMM_PAT_CTRL_2	0x4E000528		4	0x4A32628C
272	DMM.DMM_PAT_DATA_2	0x4E00052C		4	0x4A326290
273	DMM.DMM_PAT_DESCR_3	0x4E000530		4	0x4A326294
274	DMM.DMM_PAT_AREA_3	0x4E000534		4	0x4A326298
275	DMM.DMM_PAT_CTRL_3	0x4E000538		4	0x4A32629C
276	DMM.DMM_PAT_DATA_3	0x4E00053C		4	0x4A3262A0
277	DMM.DMM_PEG_PRIO0	0x4E000460		4	0x4A3262A4
278	DMM.DMM_PEG_PRIO1	0x4E000464		4	0x4A3262A8
279	DMM.DMM_PEG_PRIO_PAT	0x4E000640		4	0x4A3262AC
280	CLK1_FLAGMUX_CLK1.L3_FLAGMUX_MASK0	0x44000508		4	0x4A3262B0
281	CLK1_FLAGMUX_CLK1.L3_FLAGMUX_MASK1	0x44000510		4	0x4A3262B4
282	CLK1_DSS_BW_REGULATOR.L3_BW_R_BANDWIDTH	0x44000708		4	0x4A3262B8

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Table 16-19. SAR_RAM_1 Memory Mapping (continued)

Order	Register Name	Register Start Address	Register End Address	Size	SAR_RAM_1 Address
283	CLK1_DSS_BW_REGULATOR.L3_BW_R_WATERMARK	0x4400070C		4	0x4A3262BC
284	CLK1_RATE_ADAPT_RESP_32TO128_CLK1.L3_RA_CNF	0x44000808		4	0x4A3262C0
285	CLK2_FLAGMUX_CLK2.L3_FLAGMUX_MASK0	0x44801008		4	0x4A3262C4
286	CLK2_FLAGMUX_CLK2.L3_FLAGMUX_MASK1	0x44801010		4	0x4A3262C8
287	CLK2_RATE_ADAPT_RESP_32TO128_CLK2.L3_RA_CNF	0x44801208		4	0x4A3262CC
288	CLK2_ISS_BW_REGULATOR.L3_BW_R_BANDWIDTH	0x44801308		4	0x4A3262D0
289	CLK2_ISS_BW_REGULATOR.L3_BW_R_WATERMARK	0x4480130C		4	0x4A3262D4
290	CLK2_IVAHD_BW_REGULATOR.L3_BW_R_BANDWIDTH	0x44801408		4	0x4A3262D8
291	CCLK2_IVAHD_BW_REGULATOR.L3_BW_R_WATERMARK	0x4480140C		4	0x4A3262DC
292	CLK2_SGX_BW_REGULATOR.L3_BW_R_BANDWIDTH	0x44801508		4	0x4A3262E0
293	CLK2_SGX_BW_REGULATOR.L3_BW_R_WATERMARK	0x4480150C		4	0x4A3262E4
294	CLK3_FLAGMUX_CLK3.L3_FLAGMUX_MASK0	0x45000208		4	0x4A3262E8
295	CLK3_FLAGMUX_CLK3.L3_FLAGMUX_MASK1	0x45000210		4	0x4A3262EC
299	RESTORE_CM2.CM_L3INIT_USB_HOST_CLKCTRL_RESTORE	0x4A009E54		4	0x4A3262F0
300	RESTORE_CM2.CM_L3INIT_USB_TLL_CLKCTRL_RESTORE	0x4A009E58		4	0x4A3262F4
301	RESTORE_CM2.CM_SDMA_STATICDEP_RESTORE	0x4A009E5C		4	0x4A3262F8
303	USBTLLHS_config.USBTLL_SAR_CNTX_0	0x4A062400		4	0x4A3262FC
304	USBTLLHS_config.USBTLL_SAR_CNTX_1	0x4A062404		4	0x4A326300
305	USBTLLHS_config.USBTLL_SAR_CNTX_2	0x4A062408		4	0x4A326304
306	USBTLLHS_config.USBTLL_SAR_CNTX_3	0x4A06240C		4	0x4A326308
307	USBTLLHS_config.USBTLL_SAR_CNTX_4	0x4A062410		4	0x4A32630C
308	USBTLLHS_config.USBTLL_SAR_CNTX_5	0x4A062414		4	0x4A326310
309	USBTLLHS_config.USBTLL_SAR_CNTX_6	0x4A062418		4	0x4A326314
310	HSUSBHOST.UHH_SYSCONFIG	0x4A064010		4	0x4A326318
311	HSUSBHOST.UHH_HOSTCONFIG	0x4A064040		4	0x4A32631C
312	HSUSBHOST.UHH_SAR_CNTX_0	0x4A064100	0x4A0646FF	1536	0x4A326320
313	RESTORE_CM2.CM_L3INIT_HSUSBHOST_CLKCTRL_RESTORE	0x4A009E54		4	0x4A326920
314	RESTORE_CM2.CM_L3INIT_HSUSBTLL_CLKCTRL_RESTORE	0x4A009E58		4	0x4A326924
315	RESTORE_CM2.CM_SDMA_STATICDEP_RESTORE	0x4A009E5C		4	0x4A326928

Table 16-20 describes the SAR_RAM_2 memory mapping:

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Table 16-20. SAR_RAM_2 Memory Mapping

Order	Register Name	Register Start Address	Register End Address	Size	SAR RAM Address
96	SYSCTRL_PADCONF_CORE.CONTROL_CORE_PAD0_GPMC_AD0_PAD1_GPMC_AD1	0x4A100040	0x4A1001D7	408	0x4A327000
97	SYSCTRL_PADCONF_CORE.CONTROL_CORE_PAD0_CSI22_DY2	0x4A1001F4		4	0x4A327198

Table 16-21 describes the SAR_RAM_3 memory mapping:

Table 16-21. SAR_RAM_3 Memory Mapping

Order	Register Name	Register Start Address	Register End Address	Size	SAR RAM Address
140	MPUMA_FW.MRM_PERMISSION_REGION_LOW_0	0x4A20A088	0x4A20A0FF	120	0x4A32826C
141	PER_AP.L4_AP_PROT_GROUP_MEMBERS_3_L	0x48000218		4	0x4A3282E4
142	PER_AP.L4_AP_PROT_GROUP_MEMBERS_4_L	0x48000220		4	0x4A3282E8
143	PER_AP.L4_AP_PROT_GROUP_MEMBERS_5_L	0x48000228		4	0x4A3282EC
144	PER_AP.L4_AP_PROT_GROUP_MEMBERS_6_L	0x48000230		4	0x4A3282F0
145	PER_AP.L4_AP_PROT_GROUP_MEMBERS_7_L	0x48000238		4	0x4A3282F4
146	PER_AP.L4_AP_PROT_GROUP_ROLES_3	0x48000298	0x4800029F	8	0x4A3282F8
147	PER_AP.L4_AP_PROT_GROUP_ROLES_4	0x480002A0	0x480002A7	8	0x4A328300
148	PER_AP.L4_AP_PROT_GROUP_ROLES_5	0x480002A8	0x480002AF	8	0x4A328308
149	PER_AP.L4_AP_PROT_GROUP_ROLES_6	0x480002B0	0x480002B7	8	0x4A328310
150	PER_AP.L4_AP_PROT_GROUP_ROLES_7	0x480002B8	0x480002BF	8	0x4A328318
151	PER_AP.L4_AP_REGION_0_L	0x48000304		4	0x4A328320
152	PER_AP.L4_AP_REGION_3_L	0x4800031C		4	0x4A328324
153	PER_AP.L4_AP_REGION_5_L	0x4800032C		4	0x4A328328
154	PER_AP.L4_AP_REGION_7_L	0x4800033C		4	0x4A32832C
155	PER_AP.L4_AP_REGION_9_L	0x4800034C		4	0x4A328330
156	PER_AP.L4_AP_REGION_11_L	0x4800035C		4	0x4A328334
157	PER_AP.L4_AP_REGION_13_L	0x4800036C		4	0x4A328338
158	PER_AP.L4_AP_REGION_15_L	0x4800037C		4	0x4A32833C
159	PER_AP.L4_AP_REGION_17_L	0x4800038C		4	0x4A328340
160	PER_AP.L4_AP_REGION_19_L	0x4800039C		4	0x4A328344
161	PER_AP.L4_AP_REGION_21_L	0x480003AC		4	0x4A328348
162	PER_AP.L4_AP_REGION_23_L	0x480003BC		4	0x4A32834C
163	PER_AP.L4_AP_REGION_25_L	0x480003CC		4	0x4A328350
164	PER_AP.L4_AP_REGION_26_L	0x480003D4		4	0x4A328354
165	PER_AP.L4_AP_REGION_28_L	0x480003E4		4	0x4A328358
166	PER_AP.L4_AP_REGION_30_L	0x480003F4		4	0x4A32835C
167	PER_AP.L4_AP_REGION_32_L	0x48000404		4	0x4A328360
168	PER_AP.L4_AP_REGION_34_L	0x48000414		4	0x4A328364
169	PER_AP.L4_AP_REGION_37_L	0x4800042C		4	0x4A328368
170	PER_AP.L4_AP_REGION_39_L	0x4800043C		4	0x4A32836C
171	PER_AP.L4_AP_REGION_41_L	0x4800044C		4	0x4A328370
172	PER_AP.L4_AP_REGION_43_L	0x4800045C		4	0x4A328374

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Table 16-21. SAR_RAM_3 Memory Mapping (continued)

Order	Register Name	Register Start Address	Register End Address	Size	SAR RAM Address
173	PER_AP.L4_AP_REGION_45_L	0x4800046C		4	0x4A328378
174	PER_AP.L4_AP_REGION_47_L	0x4800047C		4	0x4A32837C
175	PER_AP.L4_AP_REGION_49_L	0x4800048C		4	0x4A328380
176	PER_AP.L4_AP_REGION_51_L	0x4800049C		4	0x4A328384
177	PER_AP.L4_AP_REGION_53_L	0x480004AC		4	0x4A328388
178	PER_AP.L4_AP_REGION_55_L	0x480004BC		4	0x4A32838C
179	PER_AP.L4_AP_REGION_57_L	0x480004CC		4	0x4A328390
180	PER_AP.L4_AP_REGION_59_L	0x480004DC		4	0x4A328394
181	PER_AP.L4_AP_REGION_61_L	0x480004EC		4	0x4A328398
182	PER_AP.L4_AP_REGION_63_L	0x480004FC		4	0x4A32839C
183	PER_AP.L4_AP_REGION_65_L	0x4800050C		4	0x4A3283A0
184	PER_AP.L4_AP_REGION_67_L	0x4800051C		4	0x4A3283A4
185	PER_AP.L4_AP_REGION_69_L	0x4800052C		4	0x4A3283A8
186	PER_AP.L4_AP_REGION_71_L	0x4800053C		4	0x4A3283AC
187	PER_AP.L4_AP_REGION_73_L	0x4800054C		4	0x4A3283B0
188	PER_AP.L4_AP_REGION_75_L	0x4800055C		4	0x4A3283B4
189	PER_AP.L4_AP_REGION_77_L	0x4800056C		4	0x4A3283B8
190	PER_AP.L4_AP_REGION_79_L	0x4800057C		4	0x4A3283BC
191	PER_AP.L4_AP_REGION_84_L	0x480005A4		4	0x4A3283C0
192	CFG_AP.L4_AP_PROT_GROUP_MEMBERS_6_L	0x4A000230		4	0x4A3283C4
193	CFG_AP.L4_AP_PROT_GROUP_MEMBERS_7_L	0x4A000238		4	0x4A3283C8
194	CFG_AP.L4_AP_PROT_GROUP_ROLES_6	0x4A0002B0	0x4A0002B7	8	0x4A3283CC
195	CFG_AP.L4_AP_PROT_GROUP_ROLES_7	0x4A0002B8	0x4A0002BF	8	0x4A3283D4
196	CFG_AP.L4_AP_REGION_0_L	0x4A000304		4	0x4A3283DC
197	CFG_AP.L4_AP_REGION_3_L	0x4A00031C		4	0x4A3283E0
198	CFG_AP.L4_AP_REGION_5_L	0x4A00032C		4	0x4A3283E4
199	CFG_AP.L4_AP_REGION_7_L	0x4A00033C		4	0x4A3283E8
200	CFG_AP.L4_AP_REGION_10_L	0x4A000354		4	0x4A3283EC
201	CFG_AP.L4_AP_REGION_11_L	0x4A00035C		4	0x4A3283F0
202	CFG_AP.L4_AP_REGION_13_L	0x4A00036C		4	0x4A3283F4
203	CFG_AP.L4_AP_REGION_15_L	0x4A00037C		4	0x4A3283F8
204	CFG_AP.L4_AP_REGION_17_L	0x4A00038C		4	0x4A3283FC
205	CFG_AP.L4_AP_REGION_21_L	0x4A0003AC		4	0x4A328400
206	CFG_AP.L4_AP_REGION_23_L	0x4A0003BC		4	0x4A328404
207	CFG_AP.L4_AP_REGION_25_L	0x4A0003CC		4	0x4A328408
208	CFG_AP.L4_AP_REGION_27_L	0x4A0003DC		4	0x4A32840C
209	CFG_AP.L4_AP_REGION_29_L	0x4A0003EC		4	0x4A328410
210	CFG_AP.L4_AP_REGION_31_L	0x4A0003FC		4	0x4A328414
211	CFG_AP.L4_AP_REGION_33_L	0x4A00040C		4	0x4A328418
212	CFG_AP.L4_AP_REGION_35_L	0x4A00041C		4	0x4A32841C
213	CFG_AP.L4_AP_REGION_37_L	0x4A00042C		4	0x4A328420
214	CFG_AP.L4_AP_REGION_39_L	0x4A00043C		4	0x4A328424
215	CFG_AP.L4_AP_REGION_41_L	0x4A00044C		4	0x4A328428
216	CFG_AP.L4_AP_REGION_43_L	0x4A00045C		4	0x4A32842C
217	CFG_AP.L4_AP_REGION_45_L	0x4A00046C		4	0x4A328430

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Table 16-21. SAR_RAM_3 Memory Mapping (continued)

Order	Register Name	Register Start Address	Register End Address	Size	SAR RAM Address
218	CFG_AP.L4_AP_REGION_47_L	0x4A00047C		4	0x4A328434
219	CFG_AP.L4_AP_REGION_49_L	0x4A00048C		4	0x4A328438
220	CFG_AP.L4_AP_REGION_51_L	0x4A00049C		4	0x4A32843C
221	CFG_AP.L4_AP_REGION_53_L	0x4A0004AC		4	0x4A328440
222	CFG_AP.L4_AP_REGION_55_L	0x4A0004BC		4	0x4A328444
223	CFG_AP.L4_AP_REGION_57_L	0x4A0004CC		4	0x4A328448
224	CFG_AP.L4_AP_REGION_59_L	0x4A0004DC		4	0x4A32844C
225	CFG_AP.L4_AP_REGION_61_L	0x4A0004EC		4	0x4A328450
226	CFG_AP.L4_AP_REGION_63_L	0x4A0004FC		4	0x4A328454
227	CFG_AP.L4_AP_REGION_65_L	0x4A00050C		4	0x4A328458
228	CFG_AP.L4_AP_REGION_67_L	0x4A00051C		4	0x4A32845C
229	CFG_AP.L4_AP_REGION_69_L	0x4A00052C		4	0x4A328460
230	CFG_AP.L4_AP_REGION_71_L	0x4A00053C		4	0x4A328464
231	CFG_AP.L4_AP_REGION_73_L	0x4A00054C		4	0x4A328468
232	CFG_AP.L4_AP_REGION_75_L	0x4A00055C		4	0x4A32846C
233	CFG_AP.L4_AP_REGION_77_L	0x4A00056C		4	0x4A328470
234	CFG_AP.L4_AP_REGION_78_L	0x4A000574		4	0x4A328474
235	CFG_AP.L4_AP_REGION_80_L	0x4A000584		4	0x4A328478
236	CFG_AP.L4_AP_REGION_82_L	0x4A000594		4	0x4A32847C
237	CFG_AP.L4_AP_REGION_84_L	0x4A0005A4		4	0x4A328480
238	CFG_AP.L4_AP_REGION_86_L	0x4A0005B4		4	0x4A328484
239	CFG_AP.L4_AP_REGION_88_L	0x4A0005C4		4	0x4A328488
240	CFG_AP.L4_AP_REGION_90_L	0x4A0005D4		4	0x4A32848C
241	CFG_AP.L4_AP_REGION_91_L	0x4A0005DC		4	0x4A328490
242	CFG_AP.L4_AP_REGION_92_L	0x4A0005E4		4	0x4A328494
243	CFG_AP.L4_AP_REGION_93_L	0x4A0005EC		4	0x4A328498
244	CFG_AP.L4_AP_REGION_94_L	0x4A0005F4		4	0x4A32849C
245	CFG_AP.L4_AP_REGION_95_L	0x4A0005FC		4	0x4A3284A0

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16.5 sDMA Basic Programming Model

16.5.1 Setup Configuration

After a hardware reset, program all fields in the logical channel registers to default values for any channels used, because most fields are undefined following reset.

Before programming any DMA transfers, the priority arbitration rate and the maximum FIFO depth must be configured through the DMA4_GCR register, and any required interrupts must be enabled through the DMA4_IRQENABLE_Lj registers and the logical channel DMA4_CICRi registers.

Software clears the DMA4_CSRi register and the IRQSTATUS bit for the different interrupt lines before enabling the channel.

16.5.2 Software-Triggered (Nonsynchronized) Transfer

To program a software-triggered DMA transfer:

1. Configure the transfer parameters in the logical DMA channel registers:
   - DMA4_CSDPi:
     - Transfer ES (8, 16, or 32 bits) in the DMA DMA4_CSDPi[1:0] bit field.
     - Read and write port access types (single/burst), DMA DMA4_CSDPi[8:7] and DMA4_CSDPi[15:14] bit fields
     - Source and destination endianism, DMA DMA4_CSDPi[21] and DMA4_CSDPi[19] bits
     - Write mode (posted or nonposted) and DMA DMA4_CSDPi[17:16] bit field
     - Source or destination packed or nonpacked (if the ES is less than the read/write port size), DMA DMA4_CSDPi[6] and DMA4_CSDPi[13] bits
   - DMA4_CENi: EN
   - DMA4_CFNi: FN per transfer block
   - DMA4_CSSAi and DMA4_CDSAi: Source and destination start address (aligned with transfer ES)
   - DMA4_CCRi:
     - Read and write port addressing modes, DMA DMA4_CCRi[13:12] and DMA4_CCRi[15:14] bit field
     - Priority bit for both read and write ports, DMA DMA4_CCRi[6] and DMA4_CCRi[26] bits
     - DMA request number (set to 0 for a software-triggered transfer) and DMA register bit fields DMA4_CCRi[4:0] = 0 and DMA4_CCRi[20:19] = 0
   - DMA4_CSEIi, DMA4_CSFIi, DMA4_CDEIi, and DMA4_CDFIi: Source and destination element and frame indexes (depending on addressing mode)
2. Start the transfer through the enable bit in the channel DMA4_CCRi register and DMA DMA4_CCRi[7] bit

The following example performs a DMA transfer on channel 10 of a 240*160 picture from RAM to RAM (0x80C00000 to 0x80F00000):

```
UWORD32 RegVal = 0;
DMA4_t *DMA4;
DMA4 = (DMA4_t
      *)malloc(sizeof(DMA4_t));
/* Init. parameters
      */
DMA4-DataType = 0x2; //
      DMA4_CSDPi[1:0]
DMA4-ReadPortAccessType = 0; //
      DMA4_CSDPi[8:7]
DMA4-WritePortAccessType = 0; //
      DMA4_CSDPi[15:14]
DMA4-SourceEndiansim = 0; //
      DMA4_CSDPi[21]
DMA4-DestinationEndianism = 0; //
```

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```
      DMA4_CSDPi[19]
DMA4-WriteMode = 0; //
      DMA4_CSDPi[17:16]
DMA4-SourcePacked = 0; //
      DMA4_CSDPi[6]
DMA4-DestinationPacked = 0; //
      DMA4_CSDPi[13]
DMA4-NumberOfElementPerFrame = 240; //
      DMA4_CENi
DMA4-NumberOfFramePerTransferBlock = 160; //
      DMA4_CFNi
DMA4-SourceStartAddress = 0x80C00000; //
      DMA4_CSSAi
DMA4-DestinationStartAddress = 0x80F00000; //
      DMA4_CDSAi
DMA4-SourceElementIndex = 1; //
      DMA4_CSEIi
DMA4-SourceFrameIndex = 1; //
      DMA4_CSFIi
DMA4-DestinationElementIndex = 1; //
      DMA4_CDEIi
DMA4-DestinationFrameIndex = 1; //
      DMA4_CDFIi
DMA4-ReadPortAccessMode = 1; //
      DMA4_CCRi[13:12]
DMA4-WritePortAccessMode = 1; //
      DMA4_CCRi[15:14]
DMA4-ReadPriority = 0; //
      DMA4_CCRi[6]
DMA4-WritePriority = 0; //
      DMA4_CCRi[23]
DMA4-ReadRequestNumber = 0; //
      DMA4_CCRi[4:0]
DMA4-WriteRequestNumber = 0; //
      DMA4_CCRi[20:19]
/* 1) Configure the transfer
      parameters in the logical DMA registers
      */
/*-------------------------------------------------------------------*/
/*
      a) Set the data type CSDP[1:0], the Read/Write Port access type
      CSDP[8:7]/[15:14], the Source/dest endianism CSDP[21]/CSDP[19], write
      mode CSDP[17:16], source/dest packed or non-packed
      CSDP[6]/CSDP[13]*/

// Read CSDP
RegVal =
      DMA4_CSDP_CH10;
// Build reg
RegVal = ((RegVal ~ 0x3)
      | DMA4-DataType );
RegVal = ((RegVal ~(0x3 7)) |
      (DMA4-ReadPortAccessType 7));
RegVal = ((RegVal ~(0x3 14)) |
      (DMA4-WritePortAccessType 14));
RegVal = ((RegVal ~(0x1 21)) |
      (DMA4-SourceEndiansim 21));
RegVal = ((RegVal ~(0x1 19)) |
      (DMA4-DestinationEndianism 19));
RegVal = ((RegVal ~(0x3 16)) |
      (DMA4-WriteMode 16));
RegVal = ((RegVal ~(0x1 6)) |
      (DMA4-SourcePacked 6));
RegVal = ((RegVal ~(0x1 13)) |
      (DMA4-DestinationPacked 13));
// Write CSDP
```

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```
DMA4_CSDP_CH10 = RegVal;
/* b) Set the number of
      element per frame CEN[23:0]*/
DMA4_CEN_CH10 =
      DMA4-NumberOfElementPerFrame;
/* c) Set the number of frame
      per block CFN[15:0]*/
DMA4_CFN_CH10 =
      DMA4-NumberOfFramePerTransferBlock;
/* d) Set the
      Source/dest start address index CSSA[31:0]/CDSA[31:0]*/

DMA4_CSSA_CH10 = DMA4-SourceStartAddress; // address start

DMA4_CDSA_CH10 = DMA4-DestinationStartAddress; // address dest

/* e) Set t1he Read Port addressing mode CCR[13:12], the
      Write Port addressing mode CCR[15:14], read/write priority
      CCR[6]/CCR[26], the current LCH CCR[20:19]=00 and CCR[4:0]=00000*/

// Read CCR
RegVal = DMA4_CCR_CH10;
//
      Build reg
RegVal = ((RegVal ~(0x3 12)) | (DMA4-ReadPortAccessMode
      12));
RegVal = ((RegVal ~(0x3 14)) | (DMA4-WritePortAccessMode
      14));
RegVal = ((RegVal ~(0x1 6)) | (DMA4-ReadPriority 6));

RegVal = ((RegVal ~(0x1 26)) | (DMA4-WritePriority 26));

RegVal= 0xFFCFFFE0 ;
// Write CCR
DMA4_CCR_CH10
      = RegVal;
/* f)- Set the source element index CSEI[15:0]*/

DMA4_CSEI_CH10 = DMA4-SourceElementIndex;
/* g)-
      Set the source frame index CSFI[15:0]*/
DMA4_CSFI_CH10 =
      DMA4-SourceFrameIndex ;
/* h)- Set the destination element
      index CDEI[15:0]*/
DMA4_CDEI_CH10 =
      DMA4-DestinationElementIndex;
/* i)- Set the destination
      frame index CDFI[31:0]*/
DMA4_CDFI_CH10 =
      DMA4-DestinationFrameIndex;
/* 2) Start the DMA transfer by
      Setting the enable bit CCR[7]=1 */

/*-------------------------------------------------------------*/

//write enable bit
DMA4_CCR_CH10 |= 1 7; /* start */
```

16.5.3 Hardware-Synchronized Transfer

To monitor a hardware synchronized DMA transfer, initialize the DMA4_CDACi register before the software enable.

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To configure an LCh to synchronize by element, packet, frame, or block, the frame synchronization DMA4_CCRi[5] FS bit and the block synchronization DMA4_CCRi[18] BS bit must be programmed. For all the following synchronized transfers (element, packet, and frame or block-synchronized transfers), the user must first set the DMA4_CCRi[24] SEL_SRC_DST_SYNC bit to 1 when the source triggers on the DMA request and set it the DMA4_CCRi[24] SEL_SRC_DST_SYNC bit to 0 when the destination triggers on the DMA request.

NOTE: The user must take care when setting the DMA4_CCRi[23] PREFETCH bit it is in conjunction with DMA4_CCRi[24] SEL_SRC_DST_SYNC bit.

- To configure an LCh to transfer one element per DMA request:
  1. Set the number of DMA request associated with the current LCH in the DMA4_CCRi[20:19] SYNCHRO_CONTROL_UPPER and DMA4_CCRi[4:0] SYNCHRO bit field.
  2. Set the data type, also referenced as element size (ES), in the DMA4_CSDPi[1:0] DATA_TYPE bit field.
  3. Set the Read Port access type (single or burst access) in the DMA4_CSDPi[8:7] SRC_BURST_EN bit field.
  4. Set the Write Port access type (single or burst access) in the DMA4_CSDPi[15:14] DST_BURST_EN bit field.
  5. Set the Read Port addressing mode in the DMA4_CCRi[13:12] SRC_AMODE bit field.
  6. Set the Write Port addressing mode in the DMA4_CCRi[15:14] DST_AMODE bit field.
  7. Set the Read start address in the DMA4_CSSAi[31:0] SRC_START_ADRS bit field.
  8. Set the Write start address in the DMA4_CDSAi[31:0] DST_START_ADRS bit field.
  9. Set both FS and BS to 0 in DMA4_CCRi[5] FS and DMA4_CCRi[18] BS.
  10. Set to 1 the channel enable bit DMA4_CCRi[7] EN.
- To configure an LCh to transfer one frame per DMA request:
  1. Set the number of DMA request associated to the current LCH in the DMA4_CCRi[20:19] SYNCHRO_CONTROL_UPPER and DMA4_CCRi[4:0] SYNCHRO bit field.
  2. Set the data type, also referenced as element size (ES), in the DMA4_CSDPi[1:0] DATA_TYPE bit field.
  3. Set the number of element per frame in the DMA4_CENi[23:0] CHANNEL_ELMNT_NBR bit field.
  4. Set the Read Port access type (single or burst access) in the DMA4_CSDPi[8:7] SRC_BURST_EN bit field.
  5. Set the Write Port access type (single or burst access) in the DMA4_CSDPi[15:14] DST_BURST_EN bit field.
  6. Set the Read Port addressing mode in the DMA4_CCRi[13:12] SRC_AMODE bit field.
  7. Set the Write Port addressing mode in the DMA4_CCRi[15:14] DST_AMODE bit field.
  8. Set the Read start address in the DMA4_CSSAi[31:0] SRC_START_ADRS bit field.
  9. Set the Write start address in the DMA4_CDSAi[31:0] DST_START_ADRS bit field.
  10. Set FS to 1 and BS to 0, respectively, in DMA4_CCRi[5] FS and DMA4_CCRi[18] BS.
  11. Set to 1 the channel enable bit DMA4_CCRi[7] EN.
- To configure an LCh to transfer one block per DMA request:
  1. Set the number of DMA request associated to the current LCH in the DMA4_CCRi[20:19] SYNCHRO_CONTROL_UPPER and DMA4_CCRi[4:0] SYNCHRO bit field.
  2. Set the data type, also referenced as element size (ES), in the DMA4_CSDPi[1:0] DATA_TYPE bit field.
  3. Set the number of element per frame in the DMA4_CENi[23:0] CHANNEL_ELMNT_NBR bit field.
  4. Set in the DMA4_CFNi[15:0] CHANNEL_FRAME_NBR bit field the number of frame (transfers), to take place before the LCH gets disabled.
  5. Set the Read Port access type (single or burst access) in the DMA4_CSDPi[8:7] SRC_BURST_EN

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bit field.

6. Set the Write Port access type (single or burst access) in the DMA4_CSDPi[15:14] DST_BURST_EN bit field.
7. Set the Read Port addressing mode in the DMA4_CCRi[13:12] SRC_AMODE bit field.
8. Set the Write Port addressing mode in the DMA4_CCRi[15:14] DST_AMODE bit field.
9. Set the Read start address in the DMA4_CSSAi[31:0] SRC_START_ADRS bit field.
10. Set the Write start address in the DMA4_CDSAi[31:0] DST_START_ADRS bit field.
11. Set FS to 0 and BS to 1, respectively, in DMA4_CCRi[5] FS and DMA4_CCRi[18] BS.
12. Set to 1 the channel enable bit DMA4_CCRi[7] EN.

- To configure an LCh to transfer one packet per DMA request:

1. Set the number of DMA request associated to the current LCH in the DMA4_CCRi[20:19] SYNCHRO_CONTROL_UPPER and DMA4_CCRi[4:0] SYNCHRO bit field.
2. Set the data type, also referenced as element size (ES), in the DMA4_CSDPi[1:0] DATA_TYPE bit field.
3. Set the number of elements per packet to transfer: If the packet requestor is in the source, set DMA4_CCRi [24] SEL_SRC_DST_SYNC to 1 and set the packet element number in the DMA4_CSFIi register and set the addressing mode of source to constant addressing in DMA4_CCRi[13:12] SRC_AMODE bit field; else, if the packet requestor is in the destination, set the DMA4_CCRi[24] SEL_SRC_DST_SYNC to 0 and set the packet element number in the DMA4_CDFIi register and set the addressing mode of destination to constant addressing in DMA4_CCRi[15:14] DST_AMODE bit field.
4. Set the number of elements per frame in the DMA4_CENi[23:0] CHANNEL_ELMNT_NBR bit field.
5. Set in the DMA4_CFNi[15:0] CHANNEL_FRAME_NBR bit field the number of frames (transfers), to take place before the LCH gets disabled.
6. Set the element number in the packet in the DMA4_CSFIi[15:0] PKT_ELNT_NBR, if constant addressing or post-incremented addressing modes are used in the source side. However, the number of element in the packet is set in the DMA4_CDFIi[15:0] PKT_ELNT_NBR if constant addressing mode is used in the destination side.
7. Set the Read Port access type (single or burst access) in the DMA4_CSDPi[8:7] SRC_BURST_EN bit field.
8. Set the Write Port access type (single or burst access) in the DMA4_CSDPi[15:14] DST_BURST_EN bit field.
9. Set the Read Port addressing mode in the DMA4_CCRi[13:12] SRC_AMODE bit field.
10. Set the Write Port addressing mode in the DMA4_CCRi[15:14] DST_AMODE bit field.
11. Set the Read start address in the DMA4_CSSAi[31:0] SRC_START_ADRS bit field.
12. Set the Write start address in the DMA4_CDSAi[31:0] DST_START_ADRS bit field.
13. Set FS to 1 and BS to 1, respectively, in DMA4_CCRi[5] FS and DMA4_CCRi[18] BS.
14. Set to 1 the channel enable bit DMA4_CCRi[7] EN.

NOTE: It is possible to stop a transfer by disabling the channel by resetting the DMA4_CCRi[7] ENABLE bit.

16.5.4 Synchronized Transfer Monitoring Using CDAC

The DMA4_CDACi register is writable and non-initialized (value undefined). It can be initialized to monitor a transfer by applying the following programming model:

1. Write 0 in the DMA4_CDACi register.
2. Enable the channel.
3. If a time-out occurs, read DMA4_CDACi register.
4. If DMA4_CDACi != 0 (it is the value configured in DMA4_CDACi):

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This indicates that the corresponding transfer has started. The user can then rely on DMA4_CCENi and DMA4_CCFNi element and frame counters.

Otherwise, if DMA4_CDACi = 0 (it is the value configured in the DMA4_CDACi):

This indicates that the corresponding transfer did not start.

16.5.5 Concurrent Software and Hardware Synchronization

This section describes thread allocation only; it does not describe the entire transfer. Because synchronized transfers are latency critical, you must allocate a thread at least on the synchronized target side.

Even for multiple concurrent channels, thread reservation ensures that when a hardware DMA request arrives, the read/write scheduler finds available thread(s) to initiate a channel schedule and issue a read/write transaction.

Consider six concurrent channels:

- Channels 0, 1, 2, and 3 are dedicated to memory-memory transfer; they are software triggered and not synchronized.
- Channel 4 is dedicated to memory-peripheral transfer, hardware triggered, and synchronized on the write side.
- Channel 5 is dedicated to peripheral-memory transfer, hardware triggered, and synchronized on the read side.

To perform thread reservation:

1. Allow thread reservation for priority channel 4 and channel 5:

   Reserve one thread (Read ThreadID 0) on the read port and one thread (Write ThreadID 0) on the write port: set the DMA4_GCR[13:12] HI_THREAD_RESERVED bit field to 0x1.
2. Specify channel priority:

   Channel 4 is a write high priority channel: set DMA4_CCRi[26] WRITE_PRIORITY = 1.

   Channel 5 is a read high priority channel: set DMA4_CCRi[6] READ_PRIORITY = 1.

16.5.6 Chained Transfer

A chained DMA transfer can be programmed as follows:

1. Configure the transfer parameters for each logical DMA channel in the chain as in step 1 for either the synchronized or non-synchronized transfers describe in Section 16.5.5, *Concurrent Software and Hardware Synchronization*.
2. For each channel in the chain, configure the DMA4_CLNK_CTRLi register as follows:
   - Next logical DMA channel number (for a looping chained transfer link last channel to first channel number), in the DMA4_CLNK_CTRLi[4:0] NEXTLCH_ID bit field.
   - Include the logical channel to the chain and enable link by setting the DMA4_CLNK_CTRLi[15] ENABLE_LNK bit.
   - For a non-looping chain, the last logical channel in the chain must have the DMA4_CLNK_CTRLi[15] ENABLE_LNK bit set to 0 to indicate the end of the chain.
3. Enable the transfer through the enable bit in the first logical channel DMA4_CCRi[7] ENABLE bit. All other channels in the chain must be disabled. Each channel is enabled automatically in turn when the previous logical channel transfer completes. A non-synchronized transfer starts immediately; a hardware-synchronized transfer starts when the DMA request line corresponding to the first DMA channel in the chain is asserted.

To stop a looping chained transfer, disable the DMA4_CLNK_CTRLi[15] ENABLE_LNK bit (by setting it to 0x0), of the final channel transfer.

In the RAM-to-RAM copy example, to copy in loop, it is possible to link channel 10 on itself. The following line can be added in the channel configuration:

```
/* g) Set link for loop */
DMA4_CLINK_CTRL_CH10 =
```


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```
0x0000800A;
```

16.5.7 90-Degree Clockwise Image Rotation

The 90-degree clockwise image rotation example described in Section 16.4.5, *Addressing Modes*, can be programmed as follows:

1. Configure the transfer parameters in the logical DMA channel registers:
   - DMA4_CSDPi:
     - Transfer ES = 32-bit (32 bpp), DMA4_CSDPi[1:0] DATA_TYPE bit field
     - Read and write port access types = maximum burst size supported by memory device, DMA4_CSDPi[8:7] SRC_BURST_EN and DMA4_CSDPi[15:14] DST_BURST_EN bit fields
     - Source and destination endianism, DMA4_CSDPi[21] SRC_ENDIAN and DMA4_CSDPi[19] DST_ENDIAN bits
     - Write mode = posted with last element nonposted, DMA4_CSDPi[17:16] WRITE_MODE bit field
     - Source and destination packed = Yes (although destination writes do not benefit because EI1), DMA4_CSDPi[6] SRC_PACKED and DMA4_CSDPi[13] DST_PACKED bits
   - DMA4_CENi: EN = 240
   - DMA4_CFNi: FN per transfer block = 160
   - DMA4_CSSAi: Source start address = 0x100000
   - DMA4_CDSAi: destination start address = 0x20013E
   - DMA4_CCRi:
     - Read and write port addressing modes = double-index addressing mode for both or post-increment addressing on source and double-index addressing on destination, DMA4_CCRi[13:12] SRC_AMODE and DMA4_CCRi[15:14] DST_AMODE bit fields
     - Low or high priority, DMA4_CCRi[6] READ_PRIORITY bit
     - DMA request number = 0 (for software-triggered transfer), DMA4_CCRi[4:0] SYNCHRO_CONTROL and DMA4_CCRi[20:19] SYNCHRO_CONTROL_UPPER bit fields
   - DMA4_CSEIi: Source EI = 1
   - DMA4_CSFIi: Source frame index = 1
   - DMA4_CDEIi: destination EI = 637
   - DMA4_CDFIi: destination frame index = 152967
2. Start the transfer through the enable bit in the channel DMA4_CCRi register.

The following parameters are used to perform this rotation from 0x80C00000 RAM address to 0x80F00000, with the same code used in Section 16.5.2, *Software-Triggered (Nonsynchronized) Transfer*:

```
/* Init. parameters */
DMA4-DataType = 0x2; //
      DMA4_CSDPi[1:0]
DMA4-ReadPortAccessType = 0x3; // DMA4_CSDPi[8:7]

DMA4-WritePortAccessType = 0x3; // DMA4_CSDPi[15:14]

DMA4-SourceEndiansim = 0; // DMA4_CSDPi[21]

DMA4-DestinationEndianism = 0; // DMA4_CSDPi[19]

DMA4-WriteMode = 0x2; // DMA4_CSDPi[17:16]
DMA4-SourcePacked
      = 0x1; // DMA4_CSDPi[6]
DMA4-DestinationPacked = 0x1; //
      DMA4_CSDPi[13]
DMA4-NumberOfElementPerFrame = 240; // DMA4_CENi

DMA4-NumberOfFramePerTransferBlock = 160; // DMA4_CFNi
```


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```
DMA4-SourceStartAddress = 0x80C00000; // DMA4_CSSAi

DMA4-DestinationStartAddress = 0x80F00000; // DMA4_CDSAi

DMA4-SourceElementIndex = 1; // DMA4_CSEIi

DMA4-SourceFrameIndex = 1; // DMA4_CSFIi

DMA4-DestinationElementIndex = 637; // DMA4_CDEIi

DMA4-DestinationFrameIndex = -152967; // DMA4_CDFIi

DMA4-ReadPortAccessMode = 0x3; // DMA4_CCRi[13:12]

DMA4-WritePortAccessMode = 0x3; // DMA4_CCRi[15:14]

DMA4-ReadPriority = 0; // DMA4_CCRi[6]
DMA4-WritePriority =
      0; // DMA4_CCRi[23]
DMA4-ReadRequestNumber = 0; // DMA4_CCRi[4:0]

DMA4-WriteRequestNumber = 0; // DMA4_CCRi[20:19]
```

16.5.8 Graphic Operations

- Transparent copy:
  1. Set the DMA4_CCRi[17] TRANSPARENT_COPY_ENABLE bit to 1
  2. Set the DMA4_CCRi[16] CONST_FILL_ENABLE bit to 0
  3. Set the value of the key color in the DMA4_COLORi[15:0] COLOR_KEY bit field

  To perform this graphic operation, the following lines can be added to the example of Section 16.5.2, *Software-Triggered (Nonsynchronized) Transfer*.

```
DMA4_CCR_CH10 = ~(0x1 16);
DMA4_CCR_CH10 |= 0x1 17;

DMA4_COLOR_CH10 = 0x00000003;
```

- Solid Color fill:
  1. Set the DMA4_CCRi[16] CONST_FILL_ENABLE bit to 1
  2. Set the DMA4_CCRi[17] TRANSPARENT_COPY_ENABLE bit to 0
  3. Set the value of key the color in the DMA4_COLORi[15:0] SOLID_COLOR bit field

  To perform this graphic operation, the following lines can be added to the example of Section 16.5.2, *Software-Triggered (Nonsynchronized) Transfer*.

```
DMA4_CCR_CH10 = ~(0x1 17);
DMA4_CCR_CH10 |= 0x1 16;

DMA4_COLOR_CH10 = 0x00000003;
```

16.5.9 Linked-List Programming Guidelines

- With the exception of the DMA4_CCRi[7] ENABLE bit and the DMA4_CDPi[7] PAUSE_LINK_LIST bit during a linked-list transfer (descriptor load phase or data load phase), avoid programming any register through the configuration port.
- Before enabling any linked-list transfer, ensure that all global registers and all registers in the descriptor are initialized. Some static channel registers (registers that are not updated by the descriptor to be loaded) must also be initialized correctly:
  - For type 2, the following registers must be initialized with consistent values:
    - All global registers
    - DMA4_CCRi
    - DMA4_CSDPi

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    - DMA4_CLNK_CTRLi
  - For type 3, the following registers must be initialized with consistent values:
    - All global registers
    - DMA4_CCRi
    - DMA4_CSDPi
    - DMA4_CLNK_CTRLi
    - DMA4_CICRi
    - DMA4_CFNi
- In case of a linked list with descriptor types 2 and 3, the content of the DMA4_CCRi register must not change during super-block life.
- The PAUSE_LINK_LIST bit must not be set in the initialization phase.

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16.6 sDMA Register Manual

16.6.1 sDMA Instance Summary

Table 16-22. sDMA Instance Summary

Module Name	Base Address	Size
sDMA	0x4A05 6000	4KB

16.6.2 sDMA Registers

16.6.2.1 sDMA Register Summary

Index *i* represents the logical channel number (where i = 0 to 31). The offset address for some registers is calculated from the channel *c* number. For example, the DMA4_CCR10 (channel 10) register has an offset address of 10 × 0x60 = 0x3C0, and thus a physical address of 0x4A05 6080 + 0x3C0 = 0x4A05 6440.

Index *j* represents the interrupt line number (where j = 0 to 3) The offset address for some registers is calculated from the channel *c* number. For example, the DMA4_IRQSTATUS_L3 (line 3) register has an offset address of 3 × 0x4 = 0xC, and thus a physical address of 0x4A05 6008 + 0xC = 0x4A05 6014.

Table 16-23. sDMA Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	sDMA L3 Base Address
DMA4_REVISION	R	32	0x0000 0000	0x4A05 6000
DMA4_IRQSTATUS_Lj (1)	RW	32	0x0000 0008 + (0x4 * j)	0x4A05 6008 + (0x4 * j)
DMA4_IRQENABLE_Lj (1)	RW	32	0x0000 0018 + (0x4 * j)	0x4A05 6018 + (0x4 * j)
DMA4_SYSSTATUS	R	32	0x0000 0028	0x4A05 6028
DMA4_OCP_SYSCONFIG	RW	32	0x0000 002C	0x4A05 602C
DMA4_CAPS_0	RW	32	0x0000 0064	0x4A05 6064
DMA4_CAPS_2	R	32	0x0000 006C	0x4A05 606C
DMA4_CAPS_3	R	32	0x0000 0070	0x4A05 6070
DMA4_CAPS_4	RW	32	0x0000 0074	0x4A05 6074
DMA4_GCR	RW	32	0x0000 0078	0x4A05 6078
DMA4_CCRi (2)	RW	32	0x0000 0080 + (0x60 * i)	0x4A05 6080 + (0x60 * i)
DMA4_CLNK_CTRLi (2)	RW	32	0x0000 0084 + (0x60 * i)	0x4A05 6084 + (0x60 * i)
DMA4_CICRi (2)	RW	32	0x0000 0088 + (0x60 * i)	0x4A05 6088 + (0x60 * i)
DMA4_CSRi (2)	RW	32	0x0000 008C + (0x60 * i)	0x4A05 608C + (0x60 * i)
DMA4_CSDPi (2)	RW	32	0x0000 0090 + (0x60 * i)	0x4A05 6090 + (0x60 * i)
DMA4_CENi (2)	RW	32	0x0000 0094 + (0x60 * i)	0x4A05 6094 + (0x60 * i)
DMA4_CFNi (2)	RW	32	0x0000 0098 + (0x60 * i)	0x4A05 6098 + (0x60 * i)
DMA4_CSSAi (2)	RW	32	0x0000 009C + (0x60 * i)	0x4A05 609C + (0x60 * i)

(1) j = 0 to 3
(2) i = 0 to 31

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Table 16-23. sDMA Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	sDMA L3 Base Address
DMA4_CDSAi [2]	RW	32	0x0000 00A0 + (0x60 * i)	0x4A05 60A0 + (0x60 * i)
DMA4_CSEIi [2]	RW	32	0x0000 00A4 + (0x60 * i)	0x4A05 60A4 + (0x60 * i)
DMA4_CSFIi [2]	RW	32	0x0000 00A8 + (0x60 * i)	0x4A05 60A8 + (0x60 * i)
DMA4_CDEIi [2]	RW	32	0x0000 00AC + (0x60 * i)	0x4A05 60AC + (0x60 * i)
DMA4_CDFIi [2]	RW	32	0x0000 00B0 + (0x60 * i)	0x4A05 60B0 + (0x60 * i)
DMA4_CSACi [2]	R	32	0x0000 00B4 + (0x60 * i)	0x4A05 60B4 + (0x60 * i)
DMA4_CDACi [2]	RW	32	0x0000 00B8 + (0x60 * i)	0x4A05 60B8 + (0x60 * i)
DMA4_CCENi [2]	RW	32	0x0000 00BC + (0x60 * i)	0x4A05 60BC + (0x60 * i)
DMA4_CCFNi [2]	RW	32	0x0000 00C0 + (0x60 * i)	0x4A05 60C0 + (0x60 * i)
DMA4_COLORi [3]	RW	32	0x0000 00C4 + (0x60 * i)	0x4A05 60C4 + (0x60 * i)
DMA4_CDPi [3]	RW	32	0x0000 00D0 + (0x60 * i)	0x4A05 60D0 + (0x60 * i)
DMA4_CNDPi [3]	RW	32	0x0000 00D4 + (0x60 * i)	0x4A05 60D4 + (0x60 * i)
DMA4_CCDNi [3]	RW	32	0x0000 00D8 + (0x60 * i)	0x4A05 60D8 + (0x60 * i)

[3] i = 0 to 31

16.6.2.2 sDMA Register Description

NOTE: Some registers have no reset value (marked with -) because of hardware implementation in memory. Software must ensure the correct programming of these registers, if needed.

Shadow registers are used to read run-time registers such as CCEN, CCFN, CDAC, and CSAC. Typically, when accessed in 8-bit or 16-bit access for two consecutive accesses, the value of the previous registers can change. A shadow register holds the entire value to let the next access recover the remaining 24 or 16 bits.

For non-32-bit transactions, start reading or writing from the LSByte first to enable the register update. There is no issue for 32-bit read-write transactions.

Table 16-24. DMA4_REVISION

Address Offset	0x0000 0000		
Physical Address	0x4A05 6000	**Instance**	sDMA
Description	This register contains the DMA revision code		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

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Bits	Field Name	Description	Type	Reset
31:0	REVISION	Reserved, Write 0's for future compatibility. Read returns 0	R	See(1)

(1) TI internal Data

Table 16-25. Register Call Summary for Register DMA4_REVISION

sDMA Register Manual
- sDMA Register Summary: [0]

Table 16-26. DMA4_IRQSTATUS_Lj

Address Offset	0x0000 0008 + (0x4 * j)	**Index**	j = 0 to 3
Physical Address	0x4A05 6008 + (0x4 * j)	**Instance**	sDMA
Description	The interrupt status register regroups all the status of the DMA4 channels that can generate an interrupt over line Lj.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CH_31_0_Lj																															

Bits	Field Name	Description	Type	Reset
31:0	CH_31_0_Lj	Channel 31 Interrupt on Lj: When an interrupt is seen on the line Lj the status of a interrupting channel i is read in the bit field i. Read 0x0: Channel Interrupt Lj false Write 0x0: Channel Interrupt Lj status bit unchanged Write 0x1: Channel Interrupt Lj status bit is reset Read 0x1: Channel Interrupt Lj true (pending)	RW	0x0000 0000

Table 16-27. Register Call Summary for Register DMA4_IRQSTATUS_Lj

sDMA Functional Description
- sDMA Controller Interrupt Requests: [0] [1] [2] [3]
- Interrupt Generation: [4]

sDMA Register Manual
- sDMA Register Summary: [5]

Table 16-28. DMA4_IRQENABLE_Lj

Address Offset	0x0000 0018 + (0x4 * j)	**Index**	j = 0 to 3
Physical Address	0x4A05 6018 + (0x4 * j)	**Instance**	sDMA
Description	The interrupt enable register allows to mask/unmask the module internal sources of interrupt, on line Lj		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CH_31_0_Lj_EN																															

Bits	Field Name	Description	Type	Reset
31:0	CH_31_0_Lj_EN	Channel Interrupt on Lj mask/unmask : to Mask/Unmask a channel i interrupt on Lj the user writes 0/1 on the bit field i. 0x0: Channel Interrupt Lj is masked 0x1: Channel Interrupt Lj generates an interrupt when it occurs	RW	0x0000 0000

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Table 16-29. Register Call Summary for Register DMA4_IRQENABLE_Lj

sDMA Functional Description • sDMA Controller Interrupt Requests: [0] [1] [2] [3] • Interrupt Generation: [4]
sDMA Basic Programming Model • Setup Configuration: [5]
sDMA Register Manual • sDMA Register Summary: [6]

Table 16-30. DMA4_SYSSTATUS

Address Offset	0x0000 0028		
Physical Address	0x4A05 6028	**Instance**	sDMA
Description	The register provides status information about the module excluding the interrupt status information (see interrupt status register)		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															RESETDONE

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved for module-specific status information	R	0x0000 0000
0	RESETDONE	Internal reset monitoring Read 0x0: Internal module reset is on-going Read 0x1: Reset completed	R	1

Table 16-31. Register Call Summary for Register DMA4_SYSSTATUS

sDMA Register Manual • sDMA Register Summary: [0]

Table 16-32. DMA4_OCP_SYSCONFIG

Address Offset	0x0000 002C		
Physical Address	0x4A05 602C	**Instance**	sDMA
Description	DMA system configuration register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																		MIDLEMODE		RESERVED		CLOCKACTIVITY		RESERVED		EMUFREE		SIDLEMODE		RESERVED	RESERVED	AUTOIDLE

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Bits	Field Name	Description	Type	Reset
31:14	RESERVED	Write 0's for future compatibility, Reads return 0	RW	0x00000
13:12	MIDLEMODE	Read write power management, standby/wait control 0x0: Force-standby: MStandby is asserted only when all the DMA channels are disabled 0x1: No-Standby: MStandby is never asserted 0x2: Smart-Standby: MStandby is asserted if at least one of the following two conditions is satisfied: 1. All the channels are disabled, OR 2. There is no non-synchronized channel enabled AND [if hardware synchronized channel is enabled, then no DMA request input is asserted and no requests are pending to be serviced]. 0x3: Reserved	RW	0x0
11:10	RESERVED	Reserved for clocks activities extension	RW	0x0
9:8	CLOCKACTIVITY	Clocks activities during wake-up Bit 8: Interface clock 0x0: Interface clock can be switched-off Bit 9: Functional clock 0x0: Functional clock can be switched-off	R	0x0
7:6	RESERVED	Write 0's for future compatibility. Read returns 0	RW	0x0
5	EMUFREE	Enable sensitivity to MSuspend 0x0: DMA4 freezes its internal logic upon MSuspend assertion 0x1: DMA4 ignores the MSuspend input	RW	0
4:3	SIDLEMODE	Configuration port power management, Idle req/ack control 0x0: Force-idle. An idle request is acknowledged unconditionally 0x1: No-idle. An idle request is never acknowledged 0x2: Smart-idle. Idle acknowledge is given by DMA4 if all of the conditions are true: 1. All the channels are disabled. 2. If hardware synchronized channel is enabled, then no DMA request input is asserted and no requests are pending to be serviced. 3. All transactions are completed on all the DMA ports. 4.No interrupts are pending to be serviced. 0x3: Reserved. Do not use	RW	0x0
2	RESERVED	Write 0's for future compatibility, Reads return 0	RW	0
1	RESERVED	Reserved for non-GP devices	RW	0
0	AUTOIDLE	Internal interface clock gating strategy 0x0: Interface clock is free running 0x1: Automatic interface clock gating strategy is applied, based on the interface activity.	RW	0

Table 16-33. Register Call Summary for Register DMA4_OCP_SYSCONFIG

sDMA Functional Description • sDMA Controller Power Management: [0] [1] [2] [3]
sDMA Register Manual • sDMA Register Summary: [4]

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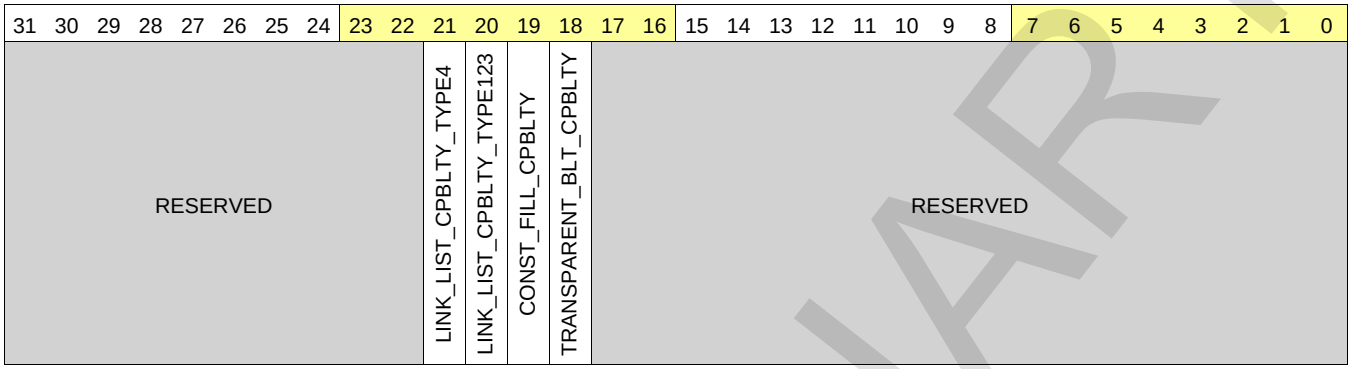
Table 16-34. DMA4_CAPS_0

Address Offset	0x0000 0064		
Physical Address	0x4A05 6064	**Instance**	sDMA
Description	DMA Capabilities Register 0 LSW		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:22	RESERVED	Write 0's for future compatibility. Read returns 0	RW	0x000
21	LINK_LIST_CPBLTY_TYPE4	Link List capability for type4 descriptor capability	R	0
20	LINK_LIST_CPBLTY_TYPE123	Link List capability for type123 descriptor capability	R	1
19	CONST_FILL_CPBLTY	Constant_Fill_Capability Read 0x0: No LCH supports constant fill copy Read 0x1: any LCH supports constant fill copy	R	1
18	TRANSPARENT_BLT_CPBLTY	Transparent_BLT_Capability Read 0x0: No LCH supports transparent BLT copy Read 0x1: any LCH supports transparent BLT copy	R	1
17:0	RESERVED	Write 0's for future compatibility. Read returns 0	RW	0x00000

Table 16-35. Register Call Summary for Register DMA4_CAPS_0

sDMA Register Manual

- sDMA Register Summary: [0]

Table 16-36. DMA4_CAPS_2

Address Offset	0x0000 006C		
Physical Address	0x4A05 606C	**Instance**	sDMA
Description	DMA Capabilities Register 2		
Type	R		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							SEPARATE_SRC_AND_DST_INDEX_CPBLTY	DST_DOUBLE_INDEX_ADRS_CPBLTY	DST_SINGLE_INDEX_ADRS_CPBLTY	DST_POST_INCRMNT_ADRS_CPBLTY	DST_CONST_ADRS_CPBLTY	SRC_DOUBLE_INDEX_ADRS_CPBLTY	SRC_SINGLE_INDEX_ADRS_CPBLTY	SRC_POST_INCREMENT_ADRS_CPBLTY	SRC_CONST_ADRS_CPBLTY

Bits	Field Name	Description	Type	Reset
31:9	RESERVED	Write 0's for future compatibility. Read returns 0	R	0x000000
8	SEPARATE_SRC_AND_DST_INDEX_CPBLTY	Separate_source/destination_index_capability Read 0x0: Does not support separate src/dst index for 2D addressing Read 0x1: Supports separate src/dest index for 2D addressing	R	1
7	DST_DOUBLE_INDEX_ADRS_CPBLTY	Destination_double_index_address_capability Read 0x0: Does not support double index address mode on the destination port Read 0x1: Supports double index address mode on the destination port	R	1
6	DST_SINGLE_INDEX_ADRS_CPBLTY	Destination_single_index_address_capability Read 0x0: Does not support single index address mode on the destination port Read 0x1: Supports single index address mode on the destination port	R	1
5	DST_POST_INCRMNT_ADRS_CPBLTY	Destination_post_increment_address_capability Read 0x0: Does not supports post-increment address mode in the destination port Read 0x1: Supports post-increment address mode in the destination port	R	1
4	DST_CONST_ADRS_CPBLTY	Destination_constant_address_capability Read 0x0: Does not supports constant address mode in the destination port Read 0x1: Supports constant address mode in the destination port	R	1
3	SRC_DOUBLE_INDEX_ADRS_CPBLTY	Source_double_index_address_capability Read 0x0: Does not support double index address mode on the source port Read 0x1: Supports double index address mode on the source port	R	1
2	SRC_SINGLE_INDEX_ADRS_CPBLTY	Source_single_index_address_capability Read 0x0: Does not support single index address mode on the source port Read 0x1: Supports single index address mode in the source port	R	1

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Bits	Field Name	Description	Type	Reset
1	SRC_POST_INCREMENT_ADRS_CPBLTY	Source_post_increment_address_capability Read 0x0: Does not supports post-increment address mode in the source port Read 0x1: Supports post-increment address mode in the source port	R	1
0	SRC_CONST_ADRS_CPBLTY	Source_constant_address_capability Read 0x0: Does not supports constant address mode in the source port Read 0x1: Supports constant address mode in the source port	R	1

Table 16-37. Register Call Summary for Register DMA4_CAPS_2

sDMA Register Manual
- sDMA Register Summary: [0]

Table 16-38. DMA4_CAPS_3

Address Offset	0x0000 0070		
Physical Address	0x4A05 6070	**Instance**	sDMA
Description	DMA Capabilities Register 3		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								BLOCK_SYNCHR_CPBLTY	PKT_SYNCHR_CPBLTY	CHANNEL_CHANINIG_CPBLTY	CHANNEL_INTERLEAVE_CPBLTY	RESERVED		FRAME_SYNCHR_CPBLTY	ELMNT_SYNCHR_CPBLTY

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Write 0's for future compatibility. Read returns 0	R	0x000000
7	BLOCK_SYNCHR_CPBLTY	Block_synchronization_capability Read 0x0: Does not support synchronization transfer on block boundary Read 0x1: Supports synchronization transfer on block boundary	R	1
6	PKT_SYNCHR_CPBLTY	Packet_synchronization_capability Read 0x0: Does not support synchronization transfer on packet boundary Read 0x1: Supports synchronization transfer on packet boundary	R	1
5	CHANNEL_CHANINIG_CPBLTY	Channel_Chaninig_capability Read 0x0: Does not support Channel Chaninig capability Read 0x1: Supports Channel Chaninig capability	R	1

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Bits	Field Name	Description	Type	Reset
4	CHANNEL_INTERLEAVE_CPBLTY	Channel_interleave_capability Read 0x0: Does not support Channel interleave capability Read 0x1: Supports Channel_interleave capability	R	1
3:2	RESERVED		R	0x0
1	FRAME_SYNCHR_CPBLTY	Frame_synchronization_capability Read 0x0: Does not support synchronization transfer on Frame boundary Read 0x1: Supports synchronization transfer on Frame boundary	R	1
0	ELMNT_SYNCHR_CPBLTY	Element_synchronization_capability Read 0x0: Does not support synchronization transfer on Element boundary Read 0x1: Supports synchronization transfer on Element boundary	R	1

Table 16-39. Register Call Summary for Register DMA4_CAPS_3

sDMA Register Manual
- sDMA Register Summary: [0]

Table 16-40. DMA4_CAPS_4

Address Offset	0x0000 0074		
Physical Address	0x4A05 6074	**Instance**	sDMA
Description	DMA Capabilities Register 4		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																	EOSB_INTERRUPT_CPBLTY	RESERVED	DRAIN_END_INTERRUPT_CPBLTY	MISALIGNED_ADRS_ERR_INTERRUPT_CPBLTY	SUPERVISOR_ERR_INTERRUPT_CPBLTY	RESERVED	TRANS_ERR_INTERRUPT_CPBLTY	PKT_INTERRUPT_CPBLTY	SYNC_STATUS_CPBLTY	BLOCK_INTERRUPT_CPBLTY	LAST_FRAME_INTERRUPT_CPBLTY	FRAME_INTERRUPT_CPBLTY	HALF_FRAME_INTERRUPT_CPBLTY	EVENT_DROP_INTERRUPT_CPBLTY	RESERVED

Bits	Field Name	Description	Type	Reset
31:15	RESERVED	Write 0's for future compatibility. Read returns 0.	RW	0x00000
14	EOSB_INTERRUPT_CPBLTY	End of Super Block detection capability.	R	1
13	RESERVED	Reserved for non-GP devices	R	1
12	DRAIN_END_INTERRUPT_CPBLTY	Drain End detection capability.	R	1
11	MISALIGNED_ADRS_ERR_INTERRUPT_CPBLTY	Misaligned error detection capability.	R	1

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Bits	Field Name	Description	Type	Reset
10	SUPERVISOR_ERR_INTERRUPT_CPBLTY	Supervisor error detection capability.	R	1
9	RESERVED	Reserved for non-GP devices	R	1
8	TRANS_ERR_INTERRUPT_CPBLTY	Transaction error detection capability.	R	1
7	PKT_INTERRUPT_CPBLTY	End of Packet detection capability. Read 0x0: Does not support end of packet interrupt generation capability Read 0x1: Supports end of packet interrupt generation capability	R	1
6	SYNC_STATUS_CPBLTY	Sync_status_capability Read 0x0: Does not support synchronized transfer status bit generation Read 0x1: Supports synchronized transfer status bit generation	R	1
5	BLOCK_INTERRUPT_CPBLTY	End of block detection capability. Read 0x0: Does not support end of block interrupt generation capability Read 0x1: Supports end of block interrupt generation capability	R	1
4	LAST_FRAME_INTERRUPT_CPBLTY	Start of last frame detection capability. Read 0x0: Does not support last frame interrupt generation capability Read 0x1: Supports last frame interrupt generation capability	R	1
3	FRAME_INTERRUPT_CPBLTY	End of frame detection capability. Read 0x0: Does not support end of frame interrupt generation capability Read 0x1: Supports end of frame interrupt generation capability	R	1
2	HALF_FRAME_INTERRUPT_CPBLTY	Detection capability of the half of frame end. Read 0x0: Does not support half of frame interrupt generation capability Read 0x1: Supports half of frame interrupt generation capability	R	1
1	EVENT_DROP_INTERRUPT_CPBLTY	Request collision detection capability. Read 0x0: Does not support event drop interrupt generation capability Read 0x1: Supports event drop interrupt generation capability	R	1
0	RESERVED	Write 0's for future compatibility. Read returns 0.	RW	0

Table 16-41. Register Call Summary for Register DMA4_CAPS_4

sDMA Register Manual

- sDMA Register Summary: [0]

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Table 16-42. DMA4_GCR

Address Offset	0x0000 0078		
Physical Address	0x4A05 6078	**Instance**	sDMA
Description	DMA4_GCR		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							CHANNEL_ID_GATE	ARBITRATION_RATE								HI_LO_FIFO_BUDGET		HI_THREAD_RESERVED		RESERVED				MAX_CHANNEL_FIFO_DEPTH							

Bits	Field Name	Description	Type	Reset
31:25	RESERVED	Write 0's for future compatibility. Read returns 0.	RW	0x00
24	CHANNEL_ID_GATE	Gates the Channel ID bus monitoring on both Read and Write ports 0x0: Gates the Channel ID qualifiers on both Read and Write Ports 0x1: Does not gate the Channel ID qualifiers on both Read and Write Ports	RW	0x0
23:16	ARBITRATION_RATE	Arbitration switching rate between prioritized and regular channel queues	RW	0x01
15:14	HI_LO_FIFO_BUDGET	Allow to have a separate Global FIFO budget for high and low priority channels. For Hi priority Channel: (Per_channel_Maximum FIFO depth + 1) x Number of active High priority Channel = High Budget FIFO For Low priority channel: (Per_channel_Maximum FIFO depth + 1) x Number of active Low priority Channel = Low Budget FIFO 0x0: no fixed budget for neither higher nor lower priority channel 0x1: 75% of FIFO for low priority and 25% for high priority channels 0x2: 25% of FIFO for low priority and 75% for high priority channels 0x3: 50% of FIFO for low priority and 50% for high priority channels	RW	0x0
13:12	HI_THREAD_RESERVED	Allow thread reservation for high priority channel on both read and write ports. 0x0: No ThreadID is reserved on the Read Port for high priority channels. No ThreadID is reserved on the Write Port for high priority channels. 0x1: Read Port ThreadID 0 is reserved for high priority channels. Write Port ThreadID 0 is reserved for high priority channels. 0x2: Read port ThreadID 0 and ThreadID 1 are reserved for high priority channels. Write Port ThreadID 0 is reserved for high priority channels. 0x3: Read PortThreadID 0, ThreadID 1 and ThreadID 2 are reserved for high priority channels. Write Port ThreadID 0 is reserved for high priority channels.	RW	0x0
11:8	RESERVED	Write 0's for future compatibility. Read returns 0.	RW	0x0

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Bits	Field Name	Description	Type	Reset
7:0	MAX_CHANNEL_FIFO_DEPTH	Maximum FIFO depth allocated to one logical channel. Maximum FIFO depth can not be 0x0. It should be at least 0x1 or greater. Note that If channel limit is less than destination burst size enough data will not be accumulated in the data FIFO and it will never be sent out on the WR port. The burst size should be less than the FIFO limit specified in this bit field.	RW	0x10

Table 16-43. Register Call Summary for Register DMA4_GCR

sDMA Functional Description
- Logical Channel Transfer Overview: [0] [1] [2]
- FIFO Queue Memory Pool: [3]
- Thread Budget Allocation: [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14]
- FIFO Budget Allocation: [15] [16]

sDMA Basic Programming Model
- Setup Configuration: [17]
- Concurrent Software and Hardware Synchronization: [18]

sDMA Register Manual
- sDMA Register Summary: [19]
- sDMA Register Description: [20]

Table 16-44. DMA4_CCRi

Address Offset	0x0000 0080 + (0x60 * i)	**index:**	i = 0 to 31
Physical Address	0x4A05 6080 + (0x60 * i)	**Instance**	sDMA
Description	Channel Control Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		RESERVED			WRITE_PRIORITY	BUFFERING_DISABLE	SEL_SRC_DST_SYNC	PREFETCH	SUPERVISOR	RESERVED	SYNCHRO_CONTROL_UPPER		BS	TRANSPARENT_COPY_ENABLE	CONST_FILL_ENABLE	DST_AMODE		SRC_AMODE		RESERVED	WR_ACTIVE	RD_ACTIVE	SUSPEND_SENSITIVE	ENABLE	READ_PRIORITY	FS	SYNCHRO_CONTROL			

Bits	Field Name	Description	Type	Reset
31:30	RESERVED	Write 0's for future compatibility. Read returns 0.	RW	0x0
29:27	RESERVED	Reserved for non-GP devices	RW	0x0
26	WRITE_PRIORITY	Channel priority on the Write side 0x0: Channel has low priority on the write side during the arbitration process. 0x1: Channel has high priority on write sided during the arbitration process.	RW	0

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Bits	Field Name	Description	Type	Reset
25	BUFFERING_DISABLE	This bit allows to disable the default buffering functionality when transfer is source synchronized. 0x0: Buffering is enabled across element/packet when source is synchronized to element, packet, frame or blocks. 0x1: Buffering is disabled across element/packet when source is synchronized to element, packet, frame or blocks.	RW	-
24	SEL_SRC_DST_SYNC	Specifies that element, packet, frame or block transfer (depending on CCR.bs and CCR.fs) is triggered by the source or the destination on the DMA request 0x0: Transfer is triggered by the destination. If synch on packet the packet element number is specified in the CDFI register. 0x1: Transfer is triggered by the source. If synchronized on packet the packet element number is specified in the CSFI register.	RW	-
23	PREFETCH	Enables the prefetch mode 0x0: Prefetch mode is disabled. When Sel_Src_Dst_Sync=1 transfers are buffered and pipelined between DMA requests. 0x1: Prefetch mode is enabled. Prefetch mode is active only when destination is synchronized. It is software user responsibility not to have at the same time Prefetch=1 when Sel_Src_Dst_Sync=1. This mode is not supported.	RW	0
22	SUPERVISOR	Enables the supervisor mode 0x0: Supervisor mode is disabled. 0x1: Supervisor mode is enabled.	RW	0
21	RESERVED	Reserved for non-GP devices	RW	0
20:19	SYNCHRO_CONTROL_UPPER	Channel Synchronization control upper (used in conjunction with the 5 bits of synchro channel DMA4_CCRi[4:0]) Used in conjunction, as 2 MSB, with the 5 bits of the synchro channel bit field.	RW	0b00
18	BS	Block synchronization This bit used in conjunction with the fs to see how the DMA request is serviced in a synchronized transfer.	RW	-
17	TRANSPARENT_COPY_ENABLE	Transparent copy enable 0x0: Transparent copy mode is disabled. 0x1: Transparent copy mode is enabled.	RW	-
16	CONST_FILL_ENABLE	Constant fill enable 0x0: Constant fill mode is disabled. 0x1: Constant fill mode is enabled.	RW	0
15:14	DST_AMODE	Selects the addressing mode on the Write Port of a channel. 0x0: Constant address mode 0x1: Post-incremented address mode 0x2: Single index address mode 0x3: Double index address mode	RW	0bxx
13:12	SRC_AMODE	Selects the addressing mode on the Read Port of a channel. 0x0: Constant address mode 0x1: Post-incremented address mode 0x2: Single index address mode 0x3: Double index address mode	RW	0bxx
11	RESERVED	Write 0s for future compatibility. Read returns 0.	RW	0

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Bits	Field Name	Description	Type	Reset
10	WR_ACTIVE	Indicates if the channel write context is active or not Read 0x0: Channel is not active on the write port. Read 0x1: Channel is currently active on the write port.	R	0
9	RD_ACTIVE	Indicates if the channel read context is active or not Read 0x0: Channel is not active on the read port. Read 0x1: Channel is currently active on the read port.	R	0
8	SUSPEND_SENSITIVE	Logical channel suspend enable bit 0x0: The channel ignores the MSuspend even if EMUFree is set to 0. 0x1: If EMUFree is set to 0 and MSuspend comes in then all current OCP services (single transaction or burst transaction as specified in the corresponding CSDP register) have to be completed before stopping processing any more transactions.	RW	0
7	ENABLE	Logical channel enable. It is SW responsibility to clear the CSR register and the IRQSTATUS bit for the different interrupt lines before enabling the channel. 0x0: The logical channel is disabled. 0x1: The logical channel is enabled.	RW	0
6	READ_PRIORITY	Channel priority on the read side 0x0: Channel has low priority on the read side during the arbitration process. 0x1: Channel has high priority on read sided during the arbitration process.	RW	0
5	FS	Frame synchronization This bit used in conjunction with the BS to see how the DMA request is serviced in a synchronized transfer FS = 0 and BS = 0: An element is transferred once a DMA request is made. FS = 0 and BS = 1: An entire block is transferred once a DMA request is made. FS = 1 and BS = 0: An entire frame is transferred once a DMA request is made. FS = 1 and BS = 1: A packet is transferred once a DMA request is made. All these different transfers can be interleaved on the port with other DMA requests.	RW	-
4:0	SYNCHRO_CONTROL	Channel synchronization control This bit field used in conjunction with the second_level_ synchro_control_upper (as 2 MSB) 0000000 : Is reserved for non synchronized LCH transfer xxxxxxx (from 1 to 127)There are 127 possible DMA request to assign to any LCH. **Note:** The channel synchronization control registers are 1-based. For example, to enable the S_DMA_1 request, DMA4_CCR[4:0] SYNCHRO_CONTROL must be set to 0x2 (DMA request number + 1).	RW	0b00000

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Table 16-45. Register Call Summary for Register DMA4_CCRi

sDMA Functional Description

- Interrupt Generation: [0]
- Logical Channel Transfer Overview: [1] [2] [3]
- Addressing Modes: [4]
- Software Synchronization: [5] [6] [7]
- Hardware Synchronization: [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19]
- Thread Budget Allocation: [20] [21]
- Reprogramming an Active Channel: [22] [23] [24] [25]
- Packet Synchronization: [26] [27] [28] [29] [30] [31]
- Graphics Acceleration Support: [32]
- Supervisor Modes: [33]
- Disabling a Channel During Transfer: [34]
- FIFO Draining Mechanism: [35] [36] [37] [38] [39]
- Type 1: [40] [41]
- Starting a Linked List: [42]
- Stop a Linked List (Abort or Drain): [43] [44] [45] [46]
- Status Bit Behavior: [47] [48] [49] [50] [51]

sDMA Basic Programming Model

- Software-Triggered (Nonsynchronized) Transfer: [52] [53] [54] [55] [56] [57] [58] [59] [60]
- Hardware-Synchronized Transfer: [61] [62] [63] [64] [65] [66] [67] [68] [69] [70] [71] [72] [73] [74] [75] [76] [77] [78] [79] [80] [81] [82] [83] [84] [85] [86] [87] [88] [89] [90] [91] [92] [93] [94] [95] [96] [97] [98] [99]
- Concurrent Software and Hardware Synchronization: [100] [101]
- Chained Transfer: [102]
- 90-Degree Clockwise Image Rotation: [103] [104] [105] [106] [107] [108] [109]
- Graphic Operations: [110] [111] [112] [113]
- Linked-List Programming Guidelines: [114] [115] [116] [117]

sDMA Register Manual

- sDMA Register Summary: [118]
- sDMA Register Description: [119]

Table 16-46. DMA4_CLNK_CTRLi

Address Offset	0x0000 0084 + (0x60 * i)	**index:**	i = 0 to 31
Physical Address	0x4A05 6084 + (0x60 * i)	**Instance**	sDMA
Description	Channel Link Control Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																ENABLE_LNK	RESERVED							NEXTLCH_ID							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Write 0's for future compatibility. Read returns 0.	RW	0x0000
15	ENABLE_LNK	Enables or disable the channel linking. 0x0: Channel linking mode is disabled When set on the fly to 0 the current channel will complete the transfer and stops the chain linking 0x1: Channel linking mode is enabled. The logical channel defined in the NextLCH_ID is enabled at the end of the current transfer	RW	0
14:5	RESERVED	Write 0's for future compatibility. Read returns 0.	RW	0x000

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Bits	Field Name	Description	Type	Reset
4:0	NEXTLCH_ID	Defines the NextLCh_ID, which is used to build logical channel chaining queue.	RW	0bxxxxx

Table 16-47. Register Call Summary for Register DMA4_CLNK_CTRLi

sDMA Functional Description • Chained Logical Channel Transfers: [0] [1] • FIFO Draining Mechanism: [2] • Type 1: [3] • Linked-List Channel Linking: [4] [5] [6] [7]
sDMA Basic Programming Model • Chained Transfer: [8] [9] [10] [11] [12] • Linked-List Programming Guidelines: [13] [14]
sDMA Register Manual • sDMA Register Summary: [15]

Table 16-48. DMA4_CICRi

Address Offset	0x0000 0088 + (0x60 * i)	**index:**	i = 0 to 31
Physical Address	0x4A05 6088 + (0x60 * i)	**Instance**	sDMA
Description	Channel Interrupt Control Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																SUPER_BLOCK_IE	RESERVED	DRAIN_IE	MISALIGNED_ERR_IE	SUPERVISOR_ERR_IE	RESERVED	TRANS_ERR_IE	PKT_IE	RESERVED	BLOCK_IE	LAST_IE	FRAME_IE	HALF_IE	DROP_IE	RESERVED	

Bits	Field Name	Description	Type	Reset
31:15	RESERVED	Write 0's for future compatibility. Read returns 0.	RW	0x00000
14	SUPER_BLOCK_IE	Enables the end of super block interrupt	RW	-
13	RESERVED	Reserved for non-GP devices	RW	1
12	DRAIN_IE	Enables the end of draining interrupt	RW	0
11	MISALIGNED_ERR_IE	Enables the address misaligned error event interrupt 0x0: Disables the misaligned address error event interrupt 0x1: Enables the misaligned address error event interrupt	RW	-
10	SUPERVISOR_ERR_IE	Enables the supervisor transaction error event interrupt 0x0: Disables the supervisor transaction error event interrupt 0x1: Enables the supervisor transaction error event interrupt	RW	1
9	RESERVED	Reserved for non-GP devices	RW	1
8	TRANS_ERR_IE	Enables the transaction error event interrupt 0x0: Disables the transaction error event interrupt 0x1: Enables the transaction error event interrupt	RW	-

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Bits	Field Name	Description	Type	Reset
7	PKT_IE	Enables the end of Packet interrupt 0x0: Disables the end of Packet transfer interrupt 0x1: Enables the end of Packet transfer interrupt	RW	-
6	RESERVED	Write 0's for future compatibility. Read returns 0.	RW	0
5	BLOCK_IE	Enables the end of block interrupt 0x0: Disables the end of block interrupt 0x1: Disables the end of block interrupt	RW	-
4	LAST_IE	Last frame interrupt enable (start of last frame) 0x0: Disables the last frame interrupt 0x1: Enables the last frame interrupt	RW	-
3	FRAME_IE	Frame interrupt enable (end of frame) 0x0: Disables the end of frame interrupt 0x1: Enables the end of frame interrupt	RW	-
2	HALF_IE	Enables or disables the half frame interrupt. 0x0: Disables the half frame interrupt 0x1: Enables the half frame interrupt	RW	-
1	DROP_IE	Synchronization event drop interrupt enable (request collision) 0x0: Disables the event drop interrupt 0x1: Enables the event drop interrupt	RW	0
0	RESERVED	Write 0's for future compatibility. Read returns 0.	RW	0

Table 16-49. Register Call Summary for Register DMA4_CICRi

sDMA Functional Description • sDMA Controller Interrupt Requests: [0] [1] • Interrupt Generation: [2] • FIFO Draining Mechanism: [3] • Descriptors: [4] [5] [6] • Interrupt During Linked-List Execution: [7] [8] [9]
sDMA Basic Programming Model • Setup Configuration: [10] • Linked-List Programming Guidelines: [11]
sDMA Register Manual • sDMA Register Summary: [12]

Table 16-50. DMA4_CSRi

Address Offset	0x0000 008C + (0x60 * i)	**index:**	i = 0 to 31
Physical Address	0x4A05 608C + (0x60 * i)	**Instance**	sDMA
Description	Channel Status Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															RESERVED	SUPER_BLOCK	RESERVED	DRAIN_END	MISALIGNED_ADRS_ERR	SUPERVISOR_ERR	RESERVED	TRANS_ERR	PKT	SYNC	BLOCK	LAST	FRAME	HALF	DROP	RESERVED

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Bits	Field Name	Description	Type	Reset
31:17	RESERVED	Write 0's for future compatibility. Read returns 0.	RW	0x0000
16:15	RESERVED	Reserved for debug (Monitor descriptor/data load phase), Write 0's for future compatibility, Read returns 0	RW	0x0
14	SUPER_BLOCK	End of Super block event	RW	0
13	RESERVED	Reserved for non-GP devices	RW	0
12	DRAIN_END	End of channel draining	RW	0
11	MISALIGNED_ADRS_ERR	Misaligned address error event Read 0x0: No address error Write 0x0: Status bit unchanged Write 0x1: Status bit is reset Read 0x1: An address error has been occurred	RW	0
10	SUPERVISOR_ERR	Supervisor transaction error event Read 0x0: No supervisor transaction error Write 0x0: Status bit unchanged Write 0x1: Status bit is reset Read 0x1: A supervisor transaction error has been occurred	RW	0
9	RESERVED	Reserved for non-GP devices	RW	0
8	TRANS_ERR	Transaction error event Read 0x0: No transaction error Write 0x0: Status bit unchanged Write 0x1: Status bit is reset Read 0x1: A transaction error has been occurred	RW	0
7	PKT	End of Packet transfer Read 0x0: The current packet transfer has not been finished Write 0x0: Status bit unchanged Write 0x1: Status bit is reset Read 0x1: The current packet has been transferred	RW	0
6	SYNC	Synchronization status of a channel. Read 0x0: Logical channel is not scheduled or servicing a non synchronized DMA request. Write 0x0: Status bit unchanged Write 0x1: Status bit is reset Read 0x1: Logical channel is servicing a synchronized DMA request	RW	0
5	BLOCK	End of block event Read 0x0: The current block transfer has not been finished Write 0x0: Status bit unchanged Write 0x1: Status bit is reset Read 0x1: The current block has been transferred	RW	0
4	LAST	Last frame (start of last frame) Read 0x0: The start of the last frame to transfer is not reached Write 0x0: Status bit unchanged Write 0x1: Status bit is reset Read 0x1: The start of the last frame to transfer is reached	RW	0

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Bits	Field Name	Description	Type	Reset
3	FRAME	End of frame event Read 0x0: The end of current transferred frame is not reached Write 0x0: Status bit unchanged Write 0x1: Status bit is reset Read 0x1: The end of current transferred frame is reached	RW	0
2	HALF	Half of frame event. Read 0x0: The half of current transferred frame is not reached Write 0x0: Status bit unchanged Write 0x1: Status bit is reset Read 0x1: The half of current transferred frame is reached	RW	0
1	DROP	Synchronization event drop occured during the transfer Read 0x0: No synchronization collision Write 0x0: Status bit unchanged Write 0x1: Status bit is reset Read 0x1: A synchronization collision has been occurred	RW	0
0	RESERVED	Write 0's for future compatibility. Read returns 0.	RW	0

Table 16-51. Register Call Summary for Register DMA4_CSRi

sDMA Functional Description • sDMA Controller Interrupt Requests: [0] [1] [2] [3] [4] • Interrupt Generation: [5] • FIFO Draining Mechanism: [6] • Interrupt During Linked-List Execution: [7] • Status Bit Behavior: [8] [9] [10] [11]
sDMA Basic Programming Model • Setup Configuration: [12]
sDMA Register Manual • sDMA Register Summary: [13]

Table 16-52. DMA4_CSDPi

Address Offset	0x0000 0090 + (0x60 * i)	**index:**	i = 0 to 31
Physical Address	0x4A05 6090 + (0x60 * i)	**Instance**	sDMA
Description	Channel Source Destination Parameters		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										SRC_ENDIAN	SRC_ENDIAN_LOCK	DST_ENDIAN	DST_ENDIAN_LOCK	WRITE_MODE		DST_BURST_EN		DST_PACKED	RESERVED					SRC_BURST_EN		SRC_PACKED	RESERVED				DATA_TYPE

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Bits	Field Name	Description	Type	Reset
31:22	RESERVED	Write 0's for future compatibility. Read returns 0.	RW	0x000
21	SRC_ENDIAN	Channel source endianness control 0x0: Source has Little Endian type 0x1: Source has Big Endian type	RW	-
20	SRC_ENDIAN_LOCK	Endianness Lock 0x0: Endianness adapt 0x1: Endianness lock	RW	-
19	DST_ENDIAN	Channel Destination endianness control 0x0: Destination has Little Endian type 0x1: Destination has Big Endian type	RW	-
18	DST_ENDIAN_LOCK	Endianness Lock 0x0: Endianness adapt 0x1: Endianness lock	RW	-
17:16	WRITE_MODE	Used to enable writing mode without posting or with posting 0x0: Write None Posted (WRNP) 0x1: Write (Posted) 0x2: All transaction are mapped on the Write command as posted except for the last transaction in the transfer mapped on a Write None Posted 0x3: Undefined	RW	0bxx
15:14	DST_BURST_EN	Used to enable bursting on the Write Port. Smaller burst size than the programmed burst size is also allowed 0x0: single access 0x1: 16 bytes or 4x32-bit / 2x64-bit burst access 0x2: 32 bytes or 8x32-bit / 4x64-bit burst access 0x3: 64 bytes or 16x32-bit / 8x64-bit burst access	RW	0b00
13	DST_PACKED	Destination receives packed data. 0x0: The destination target is non packed 0x1: The destination target is packed	RW	-
12:9	RESERVED	Write the reset value. Read returns reset value	RW	0x-
8:7	SRC_BURST_EN	Used to enable bursting on the Read Port. Smaller burst size than the programmed burst size is also allowed 0x0: single access 0x1: 16 bytes or 4x32-bit / 2x64-bit burst access 0x2: 32 bytes or 8x32-bit / 4x64-bit burst access 0x3: 64 bytes or 16x32-bit / 8x64-bit burst access	RW	0bxx
6	SRC_PACKED	Source provides packed data. 0x0: The source target is non packed 0x1: The source target is packed	RW	-
5:2	RESERVED	Write the reset value. Read returns reset value	RW	0x-
1:0	DATA_TYPE	Defines the type of the data moved in the channel. 0x0: 8 bits scalar 0x1: 16 bits scalar 0x2: 32 bits scalar 0x3: Reserved	RW	0bxx

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Table 16-53. Register Call Summary for Register DMA4_CSDPi

sDMA Functional Description • Addressing Modes: [0] • Packed Accesses: [1] • Burst Transactions: [2] • Endianism Conversion: [3] [4] • Hardware Synchronization: [5] • Graphics Acceleration Support: [6] • Posted and Nonposted Writes: [7] • Type 1: [8]
sDMA Basic Programming Model • Software-Triggered (Nonsynchronized) Transfer: [9] [10] [11] [12] [13] [14] [15] [16] [17] • Hardware-Synchronized Transfer: [18] [19] [20] [21] [22] [23] [24] [25] [26] [27] [28] [29] • 90-Degree Clockwise Image Rotation: [30] [31] [32] [33] [34] [35] [36] [37] [38] • Linked-List Programming Guidelines: [39] [40]
sDMA Register Manual • sDMA Register Summary: [41]

Table 16-54. DMA4_CENi

Address Offset	0x0000 0094 + (0x60 * i)	**index:**	i = 0 to 31
Physical Address	0x4A05 6094 + (0x60 * i)	**Instance**	sDMA
Description	Channel Element Number		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								CHANNEL_ELMNT_NBR																									

Bits	Field Name	Description	Type	Reset
31:24	RESERVED	Write 0's for future compatibility. Read returns 0.	RW	0x00
23:0	CHANNEL_ELMNT_NBR	Number of elements within a frame (unsigned) to transfer	RW	0x------

Table 16-55. Register Call Summary for Register DMA4_CENi

sDMA Functional Description • Addressing Modes: [0] [1]
sDMA Basic Programming Model • Software-Triggered (Nonsynchronized) Transfer: [2] • Hardware-Synchronized Transfer: [3] [4] [5] • 90-Degree Clockwise Image Rotation: [6]
sDMA Register Manual • sDMA Register Summary: [7]

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Table 16-56. DMA4_CFNi

Address Offset	0x0000 0098 + (0x60 * i)	**index:**	i = 0 to 31
Physical Address	0x4A05 6098 + (0x60 * i)	**Instance**	sDMA
Description	Channel Frame Number		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																CHANNEL_FRAME_NBR															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Write 0's for future compatibility. Read returns 0.	RW	0x0000
15:0	CHANNEL_FRAME_NBR	Number of frames within the block to be transferred (unsigned)	RW	0x----

Table 16-57. Register Call Summary for Register DMA4_CFNi

sDMA Functional Description • Addressing Modes: [0] [1]
sDMA Basic Programming Model • Software-Triggered (Nonsynchronized) Transfer: [2] • Hardware-Synchronized Transfer: [3] [4] • 90-Degree Clockwise Image Rotation: [5] • Linked-List Programming Guidelines: [6]
sDMA Register Manual • sDMA Register Summary: [7]

Table 16-58. DMA4_CSSAi

Address Offset	0x0000 009C + (0x60 * i)	**index:**	i = 0 to 31
Physical Address	0x4A05 609C + (0x60 * i)	**Instance**	sDMA
Description	Channel Source Start Address		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SRC_START_ADRS																															

Bits	Field Name	Description	Type	Reset
31:0	SRC_START_ADRS	32 bits of the source start address	RW	0x--------

Table 16-59. Register Call Summary for Register DMA4_CSSAi

sDMA Functional Description • Addressing Modes: [0]
sDMA Basic Programming Model • Software-Triggered (Nonsynchronized) Transfer: [1] • Hardware-Synchronized Transfer: [2] [3] [4] [5] • 90-Degree Clockwise Image Rotation: [6]
sDMA Register Manual • sDMA Register Summary: [7]

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Table 16-60. DMA4_CDSAi

Address Offset	0x0000 00A0 + (0x60 * i)	**index:**	i = 0 to 31
Physical Address	0x4A05 60A0 + (0x60 * i)	**Instance**	sDMA
Description	Channel Destination Start Address		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DST_START_ADRS																															

Bits	Field Name	Description	Type	Reset
31:0	DST_START_ADRS	32 bits of the destination start address	RW	0x--------

Table 16-61. Register Call Summary for Register DMA4_CDSAi

sDMA Functional Description • Addressing Modes: [0]
sDMA Basic Programming Model • Software-Triggered (Nonsynchronized) Transfer: [1] • Hardware-Synchronized Transfer: [2] [3] [4] [5] • 90-Degree Clockwise Image Rotation: [6]
sDMA Register Manual • sDMA Register Summary: [7]

Table 16-62. DMA4_CSEIi

Address Offset	0x0000 00A4 + (0x60 * i)	**index:**	i = 0 to 31
Physical Address	0x4A05 60A4 + (0x60 * i)	**Instance**	sDMA
Description	Channel Source Element Index (Signed)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																CHANNEL_SRC_ELMNT_INDEX															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Write 0's for future compatibility. Read returns 0.	RW	0x0000
15:0	CHANNEL_SRC_ELMNT_INDEX	Channel source element index	RW	0x----

Table 16-63. Register Call Summary for Register DMA4_CSEIi

sDMA Functional Description • Addressing Modes: [0]
sDMA Basic Programming Model • Software-Triggered (Nonsynchronized) Transfer: [1] • 90-Degree Clockwise Image Rotation: [2]
sDMA Register Manual • sDMA Register Summary: [3]

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Table 16-64. DMA4_CSFIi

Address Offset	0x0000 00A8 + (0x60 * i)	**index:**	i = 0 to 31
Physical Address	0x4A05 60A8 + (0x60 * i)	**Instance**	sDMA
Description	Channel Source Frame Index (Signed) or 16-bit Packet size		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CH_SRC_FRM_INDEX_OR_16BIT_PKT_ELNT_NBR																															

Bits	Field Name	Description	Type	Reset
31:0	CH_SRC_FRM_INDEX_OR_16BIT_PKT_ELNT_NBR	Channel source frame index value if source address is in double index mode. Or if fs=bs=1 and DMA_CCR[SEL_SRC_DST_SYNC] = 1; the bit field [15:0] gives the number of element in packet. The field [31:16] is unused for the packet size.	RW	0x--------

Table 16-65. Register Call Summary for Register DMA4_CSFIi

sDMA Functional Description
- Addressing Modes: [0]
- Hardware Synchronization: [1]
- Packet Synchronization: [2] [3] [4] [5] [6]

sDMA Basic Programming Model
- Software-Triggered (Nonsynchronized) Transfer: [7]
- Hardware-Synchronized Transfer: [8] [9]
- 90-Degree Clockwise Image Rotation: [10]

sDMA Register Manual
- sDMA Register Summary: [11]

Table 16-66. DMA4_CDEIi

Address Offset	0x0000 00AC + (0x60 * i)	**index:**	i = 0 to 31
Physical Address	0x4A05 60AC + (0x60 * i)	**Instance**	sDMA
Description	Channel Destination Element Index (Signed)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																CHANNEL_DST_ELMNT_INDEX															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Write 0's for future compatibility. Read returns 0.	RW	0x0000
15:0	CHANNEL_DST_ELMNT_INDEX	Channel destination element index	RW	0x----

Table 16-67. Register Call Summary for Register DMA4_CDEIi

sDMA Functional Description
- Addressing Modes: [0]

sDMA Basic Programming Model
- Software-Triggered (Nonsynchronized) Transfer: [1]
- 90-Degree Clockwise Image Rotation: [2]

sDMA Register Manual
- sDMA Register Summary: [3]

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Table 16-68. DMA4_CDFIi

Address Offset	0x0000 00B0 + (0x60 * i)	**index:**	i = 0 to 31
Physical Address	0x4A05 60B0 + (0x60 * i)	**Instance**	sDMA
Description	Channel Destination Frame Index (Signed) or 16-bit Packet size		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CH_DST_FRM_IDX_OR_16BIT_PKT_ELNT_NBR																															

Bits	Field Name	Description	Type	Reset
31:0	CH_DST_FRM_IDX_OR_16BIT_PKT_ELNT_NBR	Channel destination frame index value if destination address is in double index mode. Or if fs=bs=1 and DMA_CCR[SEL_SRC_DST_SYNC]=0; the bit field [15:0] gives the number of element in packet. The field [31:16] is unused for the packet size..	RW	0x--------

Table 16-69. Register Call Summary for Register DMA4_CDFIi

sDMA Functional Description
- Addressing Modes: [0]
- Hardware Synchronization: [1]
- Packet Synchronization: [2] [3] [4] [5] [6]

sDMA Basic Programming Model
- Software-Triggered (Nonsynchronized) Transfer: [7]
- Hardware-Synchronized Transfer: [8] [9]
- 90-Degree Clockwise Image Rotation: [10]

sDMA Register Manual
- sDMA Register Summary: [11]

Table 16-70. DMA4_CSACi

Address Offset	0x0000 00B4 + (0x60 * i)	**index:**	i = 0 to 31
Physical Address	0x4A05 60B4 + (0x60 * i)	**Instance**	sDMA
Description	Channel Source Address Value. User has to access this register only in 32-bit access. If accessed in 8-bit or 16bit data may be corrupted.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SRC_ELMNT_ADRS																															

Bits	Field Name	Description	Type	Reset
31:0	SRC_ELMNT_ADRS	Current source address counter value	R	0x--------

Table 16-71. Register Call Summary for Register DMA4_CSACi

sDMA Register Manual
- sDMA Register Summary: [0]

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Table 16-72. DMA4_CDACi

Address Offset	0x0000 00B8 + (0x60 * i)	**index:**	i = 0 to 31
Physical Address	0x4A05 60B8 + (0x60 * i)	**Instance**	sDMA
Description	Channel Destination Address Value. User has to access this register only in 32-bit access. If accessed in 8-bit or 16bit data may be corrupted.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DST_ELMNT_ADRS																															

Bits	Field Name	Description	Type	Reset
31:0	DST_ELMNT_ADRS	Current destination address counter value	RW	0x--------

Table 16-73. Register Call Summary for Register DMA4_CDACi

sDMA Functional Description • Hardware Synchronization: [0]
sDMA Basic Programming Model • Hardware-Synchronized Transfer: [1] • Synchronized Transfer Monitoring Using CDAC: [2] [3] [4] [5] [6] [7] [8]
sDMA Register Manual • sDMA Register Summary: [9]

Table 16-74. DMA4_CCENi

Address Offset	0x0000 00BC + (0x60 * i)	**index:**	i = 0 to 31
Physical Address	0x4A05 60BC + (0x60 * i)	**Instance**	sDMA
Description	Channel Current Transferred Element Number in the current frame. User has to access this register only in 32-bit access. If accessed in 8-bit or 16bit data may be corrupted.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								CURRENT_ELMNT_NBR																							

Bits	Field Name	Description	Type	Reset
31:24	RESERVED	Write 0's for future compatibility. Read returns 0.	RW	0x00
23:0	CURRENT_ELMNT_NBR	Channel current transferred element number in the current frame	RW	0x------

Table 16-75. Register Call Summary for Register DMA4_CCENi

sDMA Functional Description • Monitoring a Linked-List Progression: [0] [1] [2]
sDMA Basic Programming Model • Synchronized Transfer Monitoring Using CDAC: [3]
sDMA Register Manual • sDMA Register Summary: [4]

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Table 16-76. DMA4_CCFNi

Address Offset	0x0000 00C0 + (0x60 * i)	**index:**	i = 0 to 31
Physical Address	0x4A05 60C0 + (0x60 * i)	**Instance**	sDMA
Description	Channel Current Transferred Frame Number in the current transfer. User has to access this register only in 32-bit access. If accessed in 8-bit or 16bit data may be corrupted.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																CURRENT_FRAME_NBR															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Write 0's for future compatibility. Read returns 0.	RW	0x0000
15:0	CURRENT_FRAME_NBR	Channel current transferred frame number in the current transfer	RW	0x----

Table 16-77. Register Call Summary for Register DMA4_CCFNi

sDMA Functional Description
- Monitoring a Linked-List Progression: [0] [1] [2]

sDMA Basic Programming Model
- Synchronized Transfer Monitoring Using CDAC: [3]

sDMA Register Manual
- sDMA Register Summary: [4]

Table 16-78. DMA4_COLORi

Address Offset	0x0000 00C4 + (0x60 * i)	**index:**	i = 0 to 31
Physical Address	0x4A05 60C4 + (0x60 * i)	**Instance**	sDMA
Description	Channel DMA COLOR KEY /SOLID COLOR		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								CH_BLT_FRGRND_COLOR_OR_SOLID_COLOR_PTRN																									

Bits	Field Name	Description	Type	Reset
31:24	RESERVED	Write 0's for future compatibility. Read returns 0.	RW	0x–
23:0	CH_BLT_FRGRND_COLOR_OR_SOLID_COLOR_PTRN	Color key or solid color pattern: The pattern is replicated according to the data type. If the data-type is 8-bit the pattern is replicated 4 times to fill the register in order to enhance processing when data is packed at the graphic module input. The same reasoning for 16-bit data-type.	RW	0x------

Table 16-79. Register Call Summary for Register DMA4_COLORi

sDMA Functional Description
- Graphics Acceleration Support: [0] [1]
- Type 1: [2]

sDMA Basic Programming Model
- Graphic Operations: [3] [4]

sDMA Register Manual
- sDMA Register Summary: [5]

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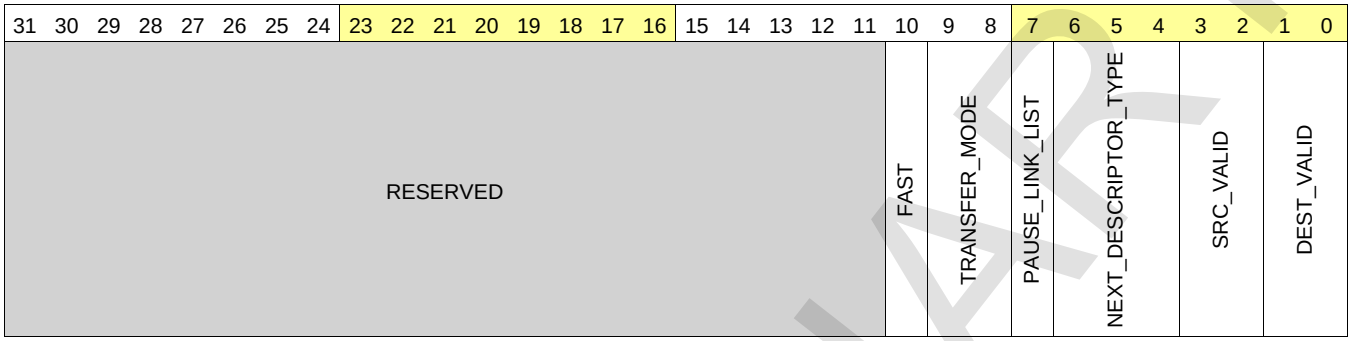
Table 16-80. DMA4_CDPi

Address Offset	0x0000 00D0 + (0x60 * i)	**index:**	i = 0 to 31
Physical Address	0x4A05 60D0 + (0x60 * i)	**Instance**	sDMA
Description	This register controls the various parameters of the link list mechanism		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:11	RESERVED	Write 0's for future compatibility, Reads return 0	RW	0x00000
10	FAST	Sets the fast-start mode for linked list descriptor types 1, 2 and 3 0x0: No fast-start mode 0x1: Fast-start mode is enabled.	RW	0x0
9:8	TRANSFER_MODE	Enable linked-list transfer mode 0x0: Normal transfer mode is used. 0x1: Linked-list channel mode for type 1, 2, or 3 descriptor is used. 0x2: Undefined 0x3: Undefined	RW	0x0
7	PAUSE_LINK_LIST	Suspend the linked-list transfer at completion of the current block transfer. 0x0: Linked list is active. 0x1: Linked list is suspended at the boundary of next descriptor loading.	RW	0x0
6:4	NEXT_DESCRIPTOR_TYPE	Next Descriptor Type 0x0: Undefined 0x1: Next descriptor is of type 1. 0x2: Next descriptor is of type 2. 0x3: Next descriptor is of type 3. 0x4: Undefined 0x5: Undefined 0x6: Undefined 0x7: Undefined	RW	0x-
3:2	SRC_VALID	Source address valid 0x0: The source address is not present in the next descriptor and continuous incrementing is enabled. 0x1: The source address must be reloaded in the next descriptor transfer. 0x2: The source start address is not present in the next descriptor. But will reload the one from configuration memory which belongs to the previous descriptor. 0x3: Undefined addressing mode	RW	0x-

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Bits	Field Name	Description	Type	Reset
1:0	DEST_VALID	Destination address valid 0x0: The destination address is not present in the next descriptor and continuous incrementing is enabled. 0x1: The destination address must be reloaded in the next descriptor transfer. 0x2: The destination start address is not present in the next descriptor. But will reload the one from configuration memory which belongs to the previous descriptor. 0x3: Undefined addressing mode	RW	0x-

Table 16-81. Register Call Summary for Register DMA4_CDPi

sDMA Functional Description • Link-List Transfer Profile: [0] • Descriptors: [1] [2] • Transfer Mode Setting: [3] [4] [5] [6] • Starting a Linked List: [7] • Pause a Linked List: [8] [9] [10] [11]
sDMA Basic Programming Model • Linked-List Programming Guidelines: [12]
sDMA Register Manual • sDMA Register Summary: [13]

Table 16-82. DMA4_CNDPi

Address Offset	0x0000 00D4 + (0x60 * i)	**index:**	i = 0 to 31
Physical Address	0x4A05 60D4 + (0x60 * i)	**Instance**	sDMA
Description	This register contains the Next descriptor Address Pointer for the link list Mechanism		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NEXT_DESCRIPTOR_POINTER																														RESERVED	

Bits	Field Name	Description	Type	Reset
31:2	NEXT_DESCRIPTOR_POINTER	This register contains the Next descriptor Address Pointer for the link list Mechanism	RW	0bxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
1:0	RESERVED	Write 0's for future compatibility, Reads return 0	RW	0x0

Table 16-83. Register Call Summary for Register DMA4_CNDPi

sDMA Functional Description • Link-List Transfer Profile: [0]
sDMA Register Manual • sDMA Register Summary: [1]

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Table 16-84. DMA4_CCDNi

Address Offset	0x0000 00D8 + (0x60 * i)	**index:**	i = 0 to 31
Physical Address	0x4A05 60D8 + (0x60 * i)	**Instance**	sDMA
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																CURRENT_DESCRIPTOR_NBR															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Write 0's for future compatibility, Reads return 0	RW	0x0000
15:0	CURRENT_DESCRIPTOR_NBR	This register when read contains the current active descriptor number in the link list. This register is Read/write to allow user initialization.	RW	0x----

Table 16-85. Register Call Summary for Register DMA4_CCDNi

sDMA Functional Description

- Monitoring a Linked-List Progression: [0] [1] [2]

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Interrupt Controllers

This chapter describes the interrupt controllers (INTCs) in the device.

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17.2 Interrupt Controllers Environment 3426
17.3 Interrupt Controller Integration 3427
17.4 Interrupt Controllers Functional Description 3433
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17.1 Interrupt Controllers Overview

The device provides three interrupt controller (INTC) modules, which handle interrupts at the device level:

- Cortex™-A9 microprocessor unit (MPU) subsystem interrupt controller (Cortex-A9 MPU INTC): This INTC module is a single functional unit that is integrated in the Cortex-A9 multiprocessor core alongside Cortex-A9 processors. It provides:
  - 128 hardware interrupt inputs
  - Generation of interrupts by software
  - Prioritization of interrupts
  - Masking of any interrupts
  - Distribution of the interrupts to the target Cortex-A9 processor(s)
  - Tracking the status of interrupts
  - Wake-up generator (WUGEN) module on external and local interrupts
- DSP subsystem interrupt controller (INTC): This module is a specific combination of WUGEN and the C64x+™ DSP INTC. It is used in the device but is not described in detail in this chapter. For detailed information about this module, see Chapter 5, *DSP Subsystem*.
- Cortex™-M3 MPU subsystem INTC (Cortex-M3 MPU INTC): This module is also called Nested Vectored Interrupt Controller (NVIC) and is integrated within each Cortex-M3 so the different interrupt lines are directly connected to each core. The interrupt mapping is the same for the two cores to facilitate parallel processing. The NVIC supports:
  - 64 external interrupts (in addition to 16 Cortex-M3 internal interrupts), which are dynamically prioritized with 16 levels of priority defined for each core
  - Low-latency exception and interrupt handling
  - Prioritization and handling of exceptions
  - Control of the local power management
  - Debug accesses to the processor core
  - WUGEN module on external interrupts, coming from device peripherals

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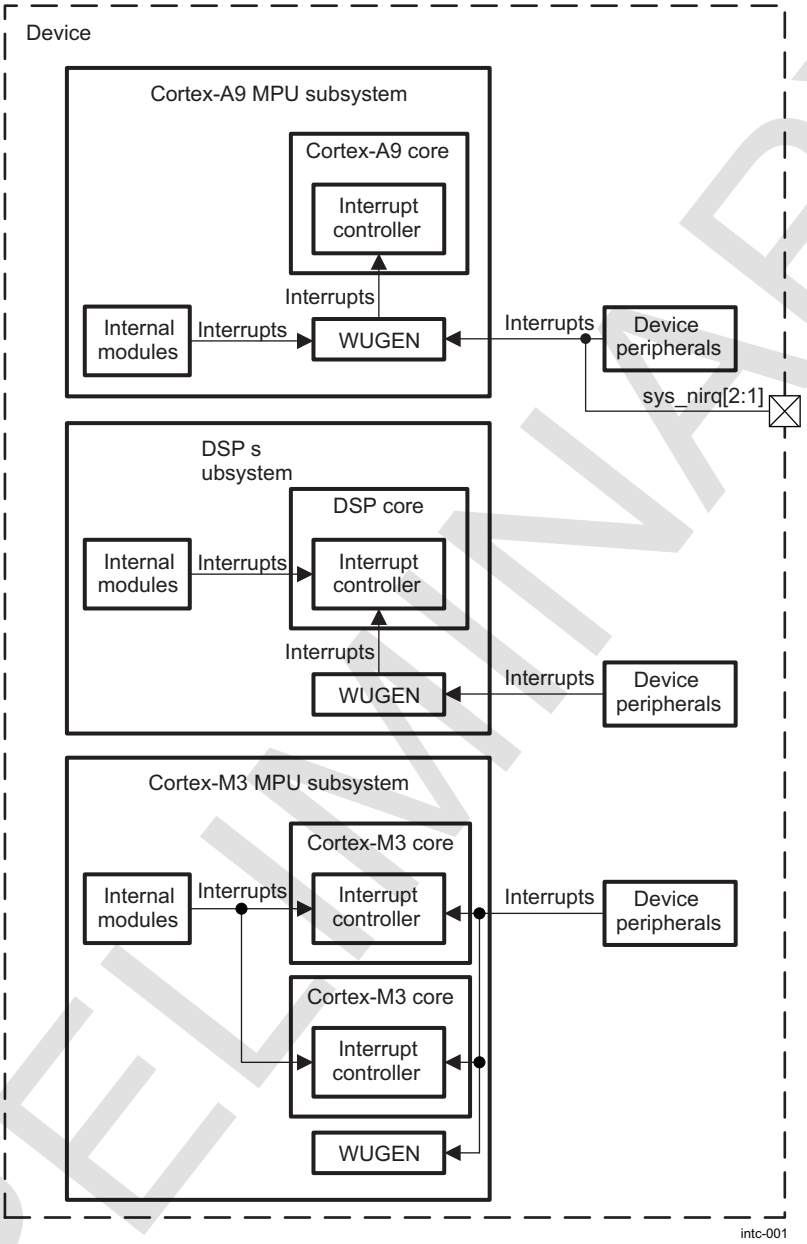
Figure 17-1 shows the internal interrupt scheme of the device.

Figure 17-1. Interrupt Controllers Overview



NOTE: For more information about the WUGEN module in the Cortex-A9 MPU subsystem (including integration, functional and register description), see Chapter 4, *Cortex-A9 MPU Subsystem*. For more information about the WUGEN module in the Cortex-M3 MPU subsystem (including integration, functional and register description), see Chapter 7, *Cortex-M3 MPU Subsystem*.

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17.2 Interrupt Controllers Environment

This section describes the INTC application fields from the environment point of view (external connections).

Figure 17-2 shows the relationship between the module and external interrupts.

Figure 17-2. Interrupts From External Devices

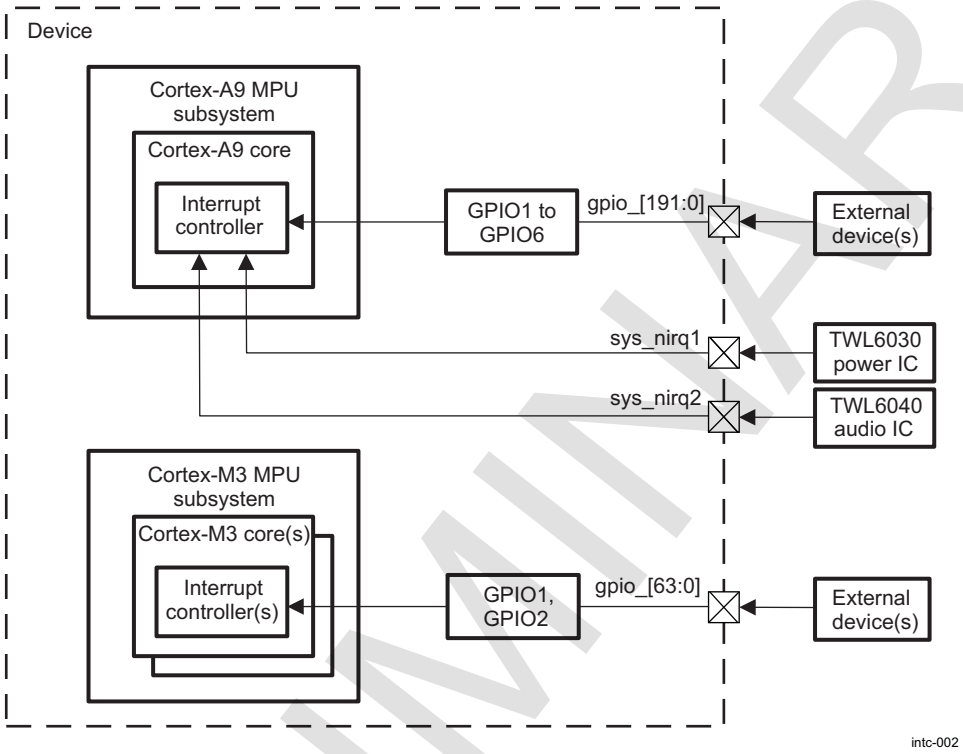

Table 17-1 describes the I/O signals that can be used by external devices to generate interrupts to the Cortex-A9 MPU INTC or Cortex-M3 MPU INTC.

Table 17-1. Interrupt Controllers I/O Signals

Signal Name	I/O [1]	Reset Value	Description	Cortex-A9 MPU INTC	Cortex-M3 MPU INTC
sys_nirq1	I	1	The TWL6030 power IC can use this pin to generate a system wake-up event to Cortex-A9 MPU INTC.	x	-
sys_nirq2	I	1	The TWL6040 audio IC can use this pin to generate a system wake-up event to Cortex-A9 MPU INTC.	x	-
gpio_[31:0]	I/O	-	External devices can use GPIO modules to generate interrupts to the Cortex-A9 MPU or Cortex-M3 MPU. There are six dedicated interrupt lines (for GPIO1 to GPIO6) to the Cortex-A9 MPU INTC and two dedicated interrupt lines (for GPIO1 and GPIO2) to the Cortex-M3 MPU INTC. Each GPIO module can generate a single interrupt whenever there is at least one event in any one of the configured 32 GPIO inputs. For more information about GPIO interrupt generation, see Chapter 25, *General-Purpose Interface*.	x	x
gpio_[63:32]	I/O	-		x	x
gpio_[95:64]	I/O	-		x	-
gpio_[127:96]	I/O	-		x	-
gpio_[159:128]	I/O	-		x	-
gpio_[191:160]	I/O	-		x	-

(1) I = Input, O = Output

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17.3 Interrupt Controller Integration

The Cortex-A9 MPU INTC is integrated inside the Cortex-A9 MPU core. For more information about Cortex-A9 MPU INTC integration, see Chapter 4, *Cortex-A9 MPU Subsystem Integration*.

The Cortex-M3 MPU INTC is integrated inside each Cortex-M3 MPU core. For more information about Cortex-M3 MPU INTC integration, see Chapter 7, *Dual Cortex-M3 MPU Subsystem Integration*.

17.3.1 Interrupt Mapping

NOTE: All device peripherals interrupts (external to the Cortex-A9 MPU, DSP, and Cortex-M3 MPU subsystems) are active-high, level-sensitive.

CAUTION

A single interrupt source can be physically mapped to multiple INTCs (Cortex-A9 MPU, DSP, and Cortex-M3 MPU subsystems). With multiple-mapped interrupts, it is strongly recommended to unmask each interrupt source in only one INTC at a time.

17.3.2 Interrupt Requests to Cortex-A9 MPU INTC

Table 17-2 lists the Cortex-A9 MPU INTC interrupt mapping.

Table 17-2. Cortex-A9 MPU INTC Interrupt Mapping

Interrupt Line (Destination)	Interrupt Line (Source)	Module Name	Description
MA_IRQ_0	L2_CACHE_IRQ	CORTEXA9	L2 cache controller interrupt(1)
MA_IRQ_1	CTI_IRQ_0	CORTEXA9	Cross-trigger module 0 (CTI0) interrupt(1)
MA_IRQ_2	CTI_IRQ_1	CORTEXA9	Cross-trigger module 1 (CTI1) interrupt(1)
MA_IRQ_3	Reserved	Reserved	Reserved
MA_IRQ_4	ELM_IRQ	ELM	Error location process completion(2)
MA_IRQ_5	CMU_IRQ_P	CMU	Cache management unit interrupt
MA_IRQ_6	Reserved	Reserved	Reserved
MA_IRQ_7	sys_nirq1	External	External interrupt 1 (active low)
MA_IRQ_8	Reserved	Reserved	Reserved
MA_IRQ_9	L3_DBG_IRQ	L3	L3 interconnect debug error
MA_IRQ_10	L3_APP_IRQ	L3	L3 interconnect application error
MA_IRQ_11	PRCM_MPU_IRQ	PRCM	PRCM interrupt
MA_IRQ_12	SDMA_IRQ_0	sDMA	sDMA interrupt 0(4)
MA_IRQ_13	SDMA_IRQ_1	sDMA	sDMA interrupt 1(4)
MA_IRQ_14	SDMA_IRQ_2	sDMA	sDMA interrupt 2(3)
MA_IRQ_15	SDMA_IRQ_3	sDMA	sDMA interrupt 3(3)
MA_IRQ_16	MCBSP4_IRQ	MCBSP4	MCBSP4 interrupt(2)
MA_IRQ_17	MCBSP1_IRQ	MCBSP1	MCBSP1 interrupt(2)
MA_IRQ_18	SR_MPU_IRQ	SR_MPU	SmartReflex MPU interrupt
MA_IRQ_19	SR_CORE_IRQ	SR_CORE	SmartReflex Core interrupt
MA_IRQ_20	GPMC_IRQ	GPMC	GPMC interrupt(2)
MA_IRQ_21	SGX_IRQ	SGX	2D/3D graphics module interrupt
MA_IRQ_22	MCBSP2_IRQ	MCBSP2	MCBSP2 interrupt(2)
MA_IRQ_23	MCBSP3_IRQ	MCBSP3	MCBSP3 interrupt(2)
MA_IRQ_24	ISS_IRQ5	Imaging subsystem	Imaging subsystem interrupt 5(3)

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Table 17-2. Cortex-A9 MPU INTC Interrupt Mapping (continued)

Interrupt Line (Destination)	Interrupt Line (Source)	Module Name	Description
MA_IRQ_25	DSS_DISPC_IRQ	Display controller	Display controller interrupt(4)
MA_IRQ_26	MAIL_U0_MPU_IRQ	MAILBOX	Mailbox user 0 interrupt
MA_IRQ_27	C2C_SSCM_IRQ0	C2C	C2C status interrupt(4)
MA_IRQ_28	DSP_MMU_IRQ	DSP	DSP MMU interrupt
MA_IRQ_29	GPIO1_MPU_IRQ	GPIO1	GPIO1 MPU interrupt(3)
MA_IRQ_30	GPIO2_MPU_IRQ	GPIO2	GPIO2 MPU interrupt(3)
MA_IRQ_31	GPIO3_MPU_IRQ	GPIO3	GPIO3 MPU interrupt
MA_IRQ_32	GPIO4_MPU_IRQ	GPIO4	GPIO4 MPU interrupt
MA_IRQ_33	GPIO5_MPU_IRQ	GPIO5	GPIO5 MPU interrupt
MA_IRQ_34	GPIO6_MPU_IRQ	GPIO6	GPIO6 MPU interrupt
MA_IRQ_35	Reserved	Reserved	Reserved
MA_IRQ_36	WDT3_IRQ	WDTIMER3	WDTIMER3 overflow
MA_IRQ_37	GPT1_IRQ	GPTIMER1	GPTIMER1 interrupt
MA_IRQ_38	GPT2_IRQ	GPTIMER2	GPTIMER2 interrupt
MA_IRQ_39	GPT3_IRQ	GPTIMER3	GPTIMER3 interrupt(3)
MA_IRQ_40	GPT4_IRQ	GPTIMER4	GPTIMER4 interrupt(3)
MA_IRQ_41	GPT5_IRQ	GPTIMER5	GPTIMER5 interrupt(2)
MA_IRQ_42	GPT6_IRQ	GPTIMER6	GPTIMER6 interrupt(2)
MA_IRQ_43	GPT7_IRQ	GPTIMER7	GPTIMER7 interrupt(2)
MA_IRQ_44	GPT8_IRQ	GPTIMER8	GPTIMER8 interrupt(2)
MA_IRQ_45	GPT9_IRQ	GPTIMER9	GPTIMER9 interrupt(3)
MA_IRQ_46	GPT10_IRQ	GPTIMER10	GPTIMER10 interrupt
MA_IRQ_47	GPT11_IRQ	GPTIMER11	GPTIMER11 interrupt(3)
MA_IRQ_48	MCSPI4_IRQ	MCSPI4	MCSPI4 interrupt
MA_IRQ_49	Reserved	Reserved	Reserved
MA_IRQ_50	Reserved	Reserved	Reserved
MA_IRQ_51	Reserved	Reserved	Reserved
MA_IRQ_52	Reserved	Reserved	Reserved
MA_IRQ_53	DSS_DSI1_IRQ	MIPI DSI1	Display Subsystem DSI1 interrupt(4)
MA_IRQ_54	Reserved	Reserved	Reserved
MA_IRQ_55	Reserved	Reserved	Reserved
MA_IRQ_56	I2C1_IRQ	I2C1	I2C1 interrupt(3)
MA_IRQ_57	I2C2_IRQ	I2C2	I2C2 interrupt(3)
MA_IRQ_58	HDQ_IRQ	HDQ	HDQ/1wire interrupt
MA_IRQ_59	MMC5_IRQ	HSMMC5	MMC5 interrupt(3)
MA_IRQ_60	Reserved	Reserved	Reserved
MA_IRQ_61	I2C3_IRQ	I2C3	I2C3 interrupt(3)
MA_IRQ_62	I2C4_IRQ	I2C4	I2C4 interrupt(3)
MA_IRQ_63	Reserved	Reserved	Reserved
MA_IRQ_64	Reserved	Reserved	Reserved
MA_IRQ_65	MCSPI1_IRQ	MCSPI1	MCSPI1 interrupt(4)
MA_IRQ_66	MCSPI2_IRQ	MCSPI2	MCSPI2 interrupt(3)
MA_IRQ_67	HSI_P1_MPU_IRQ	HSI	HSI Port 1 interrupt(3)
MA_IRQ_68	HSI_P2_MPU_IRQ	HSI	HSI Port 2 interrupt(3)
MA_IRQ_69	FDIF_IRQ_3	Face Detect	Face detect interrupt 3
MA_IRQ_70	UART4_IRQ	UART4	UART module 4 interrupt
MA_IRQ_71	HSI_DMA_MPU_IRQ	HSI	HSI DMA engine MPU request(3)

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Table 17-2. Cortex-A9 MPU INTC Interrupt Mapping (continued)

Interrupt Line (Destination)	Interrupt Line (Source)	Module Name	Description
MA_IRQ_72	UART1_IRQ	UART1	UART1 interrupt
MA_IRQ_73	UART2_IRQ	UART2	UART2 interrupt
MA_IRQ_74	UART3_IRQ	UART3	UART3 interrupt(4)
MA_IRQ_75	PBIAS_IRQ	PRCM	Merged interrupt for PBIASlite1 and 2
MA_IRQ_76	HSUSB_OHCI_IRQ	HSUSBHOST	HSUSB MP host interrupt OHCI controller
MA_IRQ_77	HSUSB_EHCI_IRQ	HSUSBHOST	HSUSB MP host interrupt EHCI controller(3)
MA_IRQ_78	HSUSB_TLL_IRQ	HSUSBTLL	HSUSB MP TLL interrupt(3)
MA_IRQ_79	Reserved	Reserved	Reserved
MA_IRQ_80	WDT2_IRQ	WDTIMER2	WDTIMER2 interrupt
MA_IRQ_81	Reserved	Reserved	Reserved
MA_IRQ_82	Reserved	Reserved	Reserved
MA_IRQ_83	MMC1_IRQ	HSMMC1	MMC1 interrupt(4)
MA_IRQ_84	DSS_DSI2_IRQ	MIPI DSI2	Display subsystem DSI2 interrupt(4)
MA_IRQ_85	Reserved	Reserved	Reserved
MA_IRQ_86	MMC2_IRQ	HSMMC2	MMC2 interrupt(4)
MA_IRQ_87	MPU_ICR_IRQ	ICR	ICR interrupt
MA_IRQ_88	C2C_SSCM_IRQ1	C2C	C2C GPI interrupt(4)
MA_IRQ_89	FSUSB_IRQ	FSUSB	FS-USB - host controller Interrupt(3)
MA_IRQ_90	FSUSB_SMI_IRQ	FSUSB	FS-USB - host controller SMI Interrupt(3)
MA_IRQ_91	MCSPI3_IRQ	MCSPI3	MCSPI3 interrupt
MA_IRQ_92	HSUSB_OTG_IRQ	HSUSBOTG	HSUSB OTG controller interrupt(3)
MA_IRQ_93	HSUSB_OTG_DMA_IRQ	HSUSBOTG	HSUSB OTG DMA interrupt(3)
MA_IRQ_94	MMC3_IRQ	HSMMC3	MMC3 interrupt(3)
MA_IRQ_95	Reserved	Reserved	Reserved
MA_IRQ_96	MMC4_IRQ	HSMMC4	MMC4 interrupt(3)
MA_IRQ_97	SLIMBUS1_IRQ	SLIMBUS1	SLIMBUS1 interrupt(2)
MA_IRQ_98	SLIMBUS2_IRQ	SLIMBUS2	SLIMBUS2 interrupt(2)
MA_IRQ_99	ABE_MPU_IRQ	ABE subsystem	Audio back-end interrupt
MA_IRQ_100	CORTEXM3_MMU_IRQ	CORTEXM3	Cortex-M3 MMU interrupt
MA_IRQ_101	DSS_HDMI_IRQ	HDMI	Display subsystem HDMI interrupt(4)
MA_IRQ_102	SR_IVA_IRQ	SR_IVA	SmartReflex IVA interrupt
MA_IRQ_103	IVAHD_IRQ2	IVAHD	Sync interrupt from ICONT2 (vDMA)(4)
MA_IRQ_104	IVAHD_IRQ1	IVAHD	Sync interrupt from ICONT1(4)
MA_IRQ_105	Reserved	Reserved	Reserved
MA_IRQ_106	Reserved	Reserved	Reserved
MA_IRQ_107	IVAHD_MAILBOX_IRQ_0	IVAHD	IVAHD mailbox interrupt 0
MA_IRQ_108	Reserved	Reserved	Reserved
MA_IRQ_109	MCASP1_AXINT	MCASP1	McASP1 transmit interrupt(2)
MA_IRQ_110	EMIF1_IRQ	EMIF1	EMIF1 interrupt
MA_IRQ_111	EMIF2_IRQ	EMIF2	EMIF2 interrupt
MA_IRQ_112	MCPDM_IRQ	MCPDM	MCPDM interrupt(2)
MA_IRQ_113	DMM_IRQ	DMM	DMM interrupt(3)
MA_IRQ_114	DMIC_IRQ	DMIC	DMIC interrupt(2)
MA_IRQ_115	Reserved	Reserved	Reserved
MA_IRQ_116	Reserved	Reserved	Reserved
MA_IRQ_117	Reserved	Reserved	Reserved
MA_IRQ_118	Reserved	Reserved	Reserved

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Table 17-2. Cortex-A9 MPU INTC Interrupt Mapping (continued)

Interrupt Line (Destination)	Interrupt Line (Source)	Module Name	Description
MA_IRQ_119	sys_nirq2	External	External interrupt 2 (active low)
MA_IRQ_120	KBD_CTL_IRQ	KEYBOARD	Keyboard controller interrupt
MA_IRQ_121	Reserved	Reserved	Reserved
MA_IRQ_122	Reserved	Reserved	Reserved
MA_IRQ_123	Reserved	Reserved	Reserved
MA_IRQ_124	Reserved	Reserved	Reserved
MA_IRQ_125	Reserved	Reserved	Reserved
MA_IRQ_126	THERMAL_ALERT	SYSCTRL_GENERAL_CORE	General CORE Control Module thermal sensor alert interrupt
MA_IRQ_127	Reserved	Reserved	Reserved

(1) Internally generated within the Cortex-A9 MPU subsystem
(2) Shared with DSP INTC
(3) Shared with Cortex-M3 MPU INTC
(4) Shared with DSP and Cortex-M3 MPU INTCs

NOTE: All Cortex-A9 MPU subsystem internal interrupts are active-high, level-sensitive.

17.3.3 Interrupt Requests to Cortex-M3 MPU INTC

Table 17-3 lists the Cortex-M3 MPU INTC interrupt mapping.

Table 17-3. Cortex-M3 MPU INTC Interrupt Mapping

Interrupt Line (Destination)	Interrupt Line (Source)	Module Name	Description
MM_IRQ_0	XLATE_MMU_FAULT	CORTEXM3	L2 cache MMU interrupt(1)
MM_IRQ_1	SHARED_CACHE_MMU_CPU_INT	CORTEXM3	Shared cache or MMU maintenance completed(1)
MM_IRQ_2	CTM_TIM_EVENT_1	CORTEXM3	CTM timer event (timer #1)(1)
MM_IRQ_3	HWSEM_M3_IRQ	CORTEXM3	Semaphore interrupt(1)
MM_IRQ_4	IC_NEMUINTR	CORTEXM3	ICECrusher™ (one to each core)(1)
MM_IRQ_5	IMP_FAULT	CORTEXM3	Imprecise fault (from interconnect)(1)
MM_IRQ_6	CTM_TIM_EVENT_2	CORTEXM3	CTM timer event (timer #2)(1)
MM_IRQ_7	DSS_DISPC_IRQ	Display controller	Display controller interrupt(4)
MM_IRQ_8	DSS_DSI1_IRQ	MIPI DSI1	Display subsystem DSI1 interrupt(4)
MM_IRQ_9	DSS_DSI2_IRQ	MIPI DSI2	Display subsystem DSI2 interrupt(4)
MM_IRQ_10	DSS_HDMI_IRQ	HDMI	Display subsystem HDMI interrupt(4)
MM_IRQ_11	ISS_IRQ0	Imaging subsystem	Imaging subsystem interrupt 0
MM_IRQ_12	ISS_IRQ1	Imaging subsystem	Imaging subsystem interrupt 1
MM_IRQ_13	ISS_IRQ2	Imaging subsystem	Imaging subsystem interrupt 2
MM_IRQ_14	ISS_IRQ3	Imaging subsystem	Imaging subsystem interrupt 3
MM_IRQ_15	ISS_IRQ4	Imaging subsystem	Imaging subsystem interrupt 4(2)
MM_IRQ_16	ISS_IRQ5	Imaging subsystem	Imaging subsystem interrupt 5(3)
MM_IRQ_17	FDIF_IRQ_1	Face detect	Face Detect interrupt 1
MM_IRQ_18	SDMA_IRQ_0	sDMA	sDMA interrupt 0(4)
MM_IRQ_19	SDMA_IRQ_1	sDMA	sDMA interrupt 1(4)
MM_IRQ_20	SDMA_IRQ_2	sDMA	sDMA interrupt 2(3)
MM_IRQ_21	SDMA_IRQ_3	sDMA	sDMA interrupt 3(3)

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Table 17-3. Cortex-M3 MPU INTC Interrupt Mapping (continued)

Interrupt Line (Destination)	Interrupt Line (Source)	Module Name	Description
MM_IRQ_22	IVAHD_MAILBOX_IRQ_2	IVAHD	IVAHD mailbox interrupt 2
MM_IRQ_23	IVAHD_IRQ2	IVAHD	Sync interrupt from ICONT2 (vDMA)(4)
MM_IRQ_24	IVAHD_IRQ1	IVAHD	Sync interrupt from ICONT1(4)
MM_IRQ_25	I2C1_IRQ	I2C1	I2C1 interrupt(3)
MM_IRQ_26	I2C2_IRQ	I2C2	I2C2 interrupt(3)
MM_IRQ_27	I2C3_IRQ	I2C3	I2C3 interrupt(3)
MM_IRQ_28	I2C4_IRQ	I2C4	I2C4 interrupt(3)
MM_IRQ_29	UART3_IRQ	UART3	UART3 interrupt(4)
MM_IRQ_30	Reserved	Reserved	Reserved
MM_IRQ_31	PRCM_M3_IRQ	PRCM	PRCM interrupt
MM_IRQ_32	Reserved	Reserved	Reserved
MM_IRQ_33	HSI_DMA_MPU_IRQ	HSI	HSI DMA engine MPU interrupt(3)
MM_IRQ_34	MAIL_U2_M3_IRQ	MAILBOX	Mailbox user 2 interrupt
MM_IRQ_35	GPIO1_MPU_IRQ	GPIO1	GPIO1 MPU interrupt(3)
MM_IRQ_36	GPIO2_MPU_IRQ	GPIO2	GPIO2 MPU interrupt(3)
MM_IRQ_37	GPT3_IRQ	GPTIMER3	GPTIMER3 interrupt(3)
MM_IRQ_38	GPT4_IRQ	GPTIMER4	GPTIMER4 interrupt(3)
MM_IRQ_39	GPT9_IRQ	GPTIMER9	GPTIMER9 interrupt(3)
MM_IRQ_40	GPT11_IRQ	GPTIMER11	GPTIMER11 interrupt(3)
MM_IRQ_41	MCSPI1_IRQ	MCSPI1	MCSPI1 interrupt(4)
MM_IRQ_42	MCSPI2_IRQ	MCSPI2	MCSPI2 interrupt(3)
MM_IRQ_43	Reserved	Reserved	Reserved
MM_IRQ_44	Reserved	Reserved	Reserved
MM_IRQ_45	Reserved	Reserved	Reserved
MM_IRQ_46	C2C_SSCM_IRQ0	C2C	C2C Status interrupt(4)
MM_IRQ_47	C2C_SSCM_IRQ1	C2C	C2C GPI interrupt(4)
MM_IRQ_48	DMM_IRQ	DMM	DMM interrupt(3)
MM_IRQ_49	Reserved	Reserved	Reserved
MM_IRQ_50	MMC1_IRQ	HSMMC1	MMC1 interrupt(4)
MM_IRQ_51	MMC2_IRQ	HSMMC2	MMC2 interrupt(4)
MM_IRQ_52	MMC3_IRQ	HSMMC3	MMC3 interrupt(3)
MM_IRQ_53	MMC4_IRQ	HSMMC4	MMC4 interrupt(3)
MM_IRQ_54	MMC5_IRQ	HSMMC5	MMC5 interrupt(3)
MM_IRQ_55	Reserved	Reserved	Reserved
MM_IRQ_56	FSUSB_SMI_IRQ	FSUSB	FS-USB – host controller SMI interrupt(3)
MM_IRQ_57	HSUSB_EHCI_IRQ	HSUSBHOST	HSUSB MP host interrupt EHCI controller(3)
MM_IRQ_58	HSUSB_TLL_IRQ	HSUSBTLL	HSUSB MP TLL interrupt(3)
MM_IRQ_59	FSUSB_IRQ	FSUSB	FS-USB – host controller Interrupt(3)
MM_IRQ_60	HSUSB_OTG_IRQ	HSUSBOTG	HSUSB OTG controller interrupt(3)
MM_IRQ_61	HSUSB_OTG_DMA_IRQ	HSUSBOTG	HSUSB OTG DMA interrupt(3)
MM_IRQ_62	HSI_P1_MPU_IRQ	HSI	HSI Port 1 interrupt(3)
MM_IRQ_63	HSI_P2_MPU_IRQ	HSI	HSI Port 2 interrupt(3)

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(1) Internally generated within the Cortex-M3 MPU subsystem
(2) Shared with DSP INTC
(3) Shared with Cortex-A9 MPU INTC
(4) Shared with DSP and Cortex-A9 MPU INTCs

NOTE: MM_IRQ_0 triggers exception 16 inside the Cortex-M3 core(s).

NOTE: All Cortex-M3 MPU subsystem internal interrupts are edge interrupts, except the one generated from the MMU (XLATE_MMU_FAULT), which is level interrupt.

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17.4 Interrupt Controllers Functional Description

17.4.1 Cortex-A9 MPU INTC Functional Description

Cortex-A9 MPU INTC is configured to have the following interrupt sources:

- Sixteen interprocessor interrupts (IPI): ID[15:0]
- Two private timer/watchdog interrupts: ID[30:29]
- Two legacy nFIQ nIRQ: one per CPU, bypasses the interrupt distributor logic and drives interrupt requests directly into the CPU, if used in legacy mode (otherwise, treated like other interrupts lines with ID28 and ID31, respectively)
- 128 hardware interrupts: ID[159:32] (rising-edge or high-level sensitive). The interrupt mapping of these interrupts is provided in Table 17-2, *Interrupt Requests to Cortex-A9 MPU INTC*.

CAUTION

Although the hardware interrupts can be configured to be rising-edge or high-level sensitive in the INTC, the device supports only active-high, level-sensitive configuration.

For more information about the functionality of the Cortex-A9 MPU INTC, see the *ARM Cortex-A9 MP Core Technical Reference Manual* .

17.4.2 Cortex-M3 MPU INTC Functional Description

The Cortex-M3 MPU INTC has the following configuration in the device:

- 64 hardware interrupts/16 levels of priority for each Cortex-M3 core. The interrupt mapping of these interrupts is provided in Table 17-3, *Interrupt Requests to Cortex-M3 MPU INTC*.
- The calibration register, which is used to reload the SYSTICK timer to generate a fixed interval, is not supported in the Cortex-M3 core within the Cortex-M3 MPU subsystem. The TENMS field is not available due to the different frequencies during voltage scaling.
- The SYSRESETREQ reset feature is not supported at the Cortex-M3 processor level. Writing to this bit has no effect.

For more information about the functionality of the Cortex-M3 MPU INTC, see *ARM Cortex-M3 Technical Reference Manual* .

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17.5 Interrupt Controllers Register Manual

17.5.1 Interrupt Controllers Instance Summary

For information about the Cortex-A9 MPU INTC and Cortex-M3 MPU INTC instances, see Chapter 4, *Cortex-A9 MPU Subsystem* and Chapter 7, *Dual Cortex-M3 Subsystem* .

17.5.2 Cortex-A9 MPU INTC Registers

For information about the Cortex-A9 MPU INTC registers and their description, see the *ARM Cortex-A9 MP Core Technical Reference Manual* .

17.5.3 Cortex-M3 MPU INTC Registers

For information about the Cortex-M3 MPU INTC registers and their description, see the *ARM Cortex-M3 Technical Reference Manual* .

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Control Module

This chapter describes the system control module for the device.

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18.4 Control Module Functional Description 3443
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18.1 Control Module Overview

The control module allows software control of the various static modes supported by the device. It is composed of two control submodules: general control module and device (padconfiguration) control module.

The general control module has the following features:

- General status and control
- Hardware observability input/output (I/O) multiplexing
- Standard eFuse logic

The device control module provides the following features:

- Pad functional I/O multiplexing
- Pad pullup/down configuration
- Pad groups associated signal integrity controls
- Complex I/O configuration
- Analog function control
- Device-specific eFuse registers

Both control submodules are split into two instances: the control core instance within the CORE power domain, and the control wake-up instance within the WKUP power domain. For more information about the four different control module instances, see Section 18.3, *Control Module Integration*.

Figure 18-1 is an overview of the control module.

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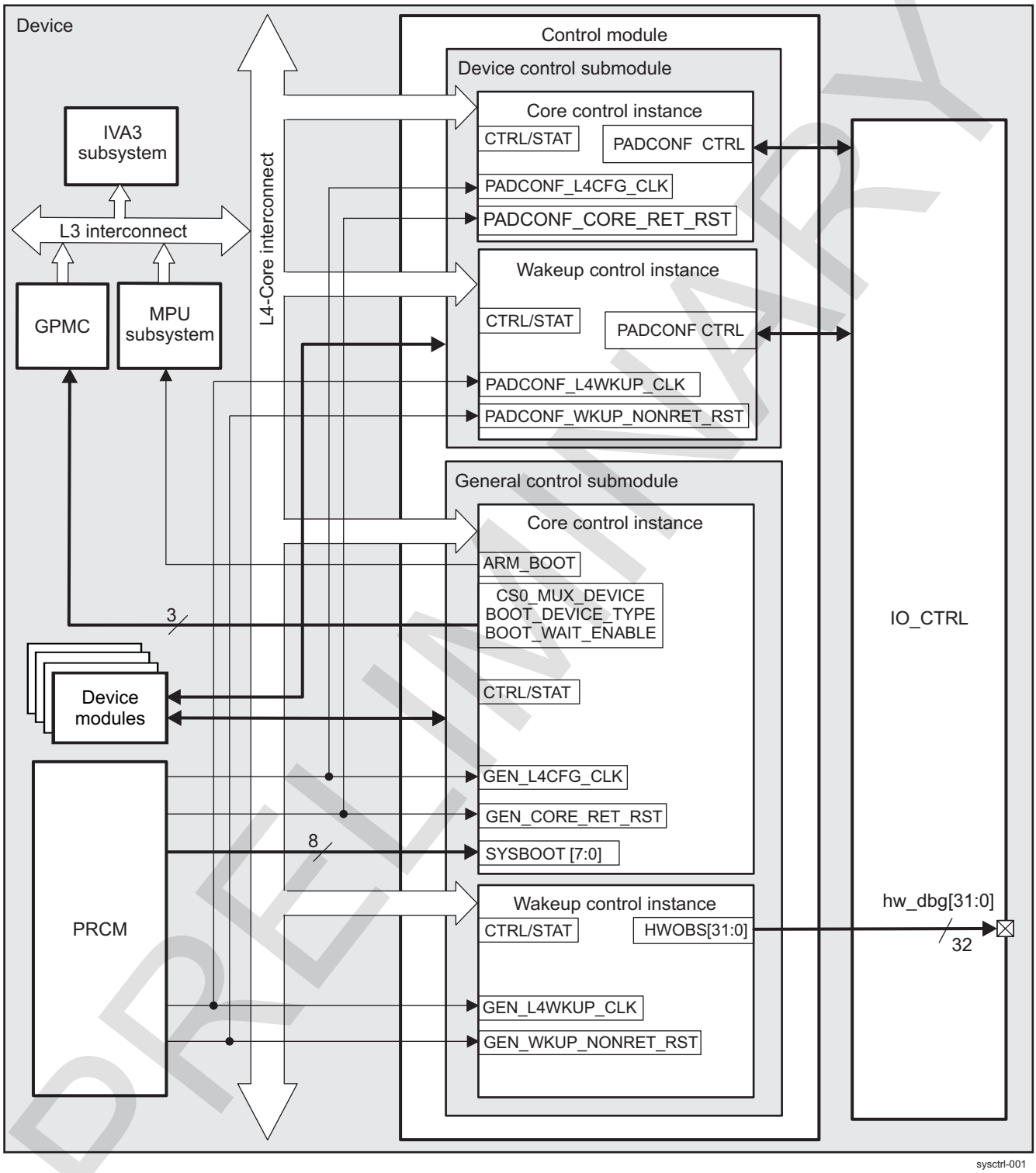
Figure 18-1. Control Module Overview



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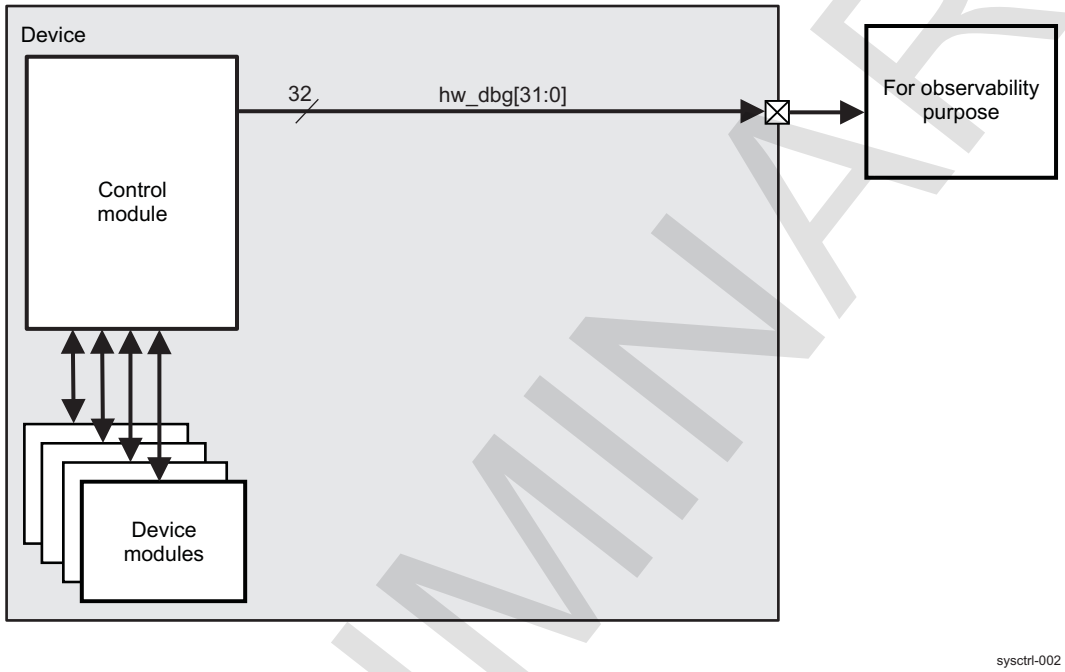
18.2 Control Module Environment

The control module controls the multiplexing of device internal module signals routed to the external pins (hw_dbg[31:0]) for hardware debug purposes. For more information, see Section 18.4.11, *Hardware Observability*, and Section 18.4.8, *PAD Functional Multiplexing and Configuration*. Using the correct pad configuration, the control module maps these pins at the device boundary to observe the internal signals from the power, reset, and clock management (PRCM) module, direct memory access (DMA) requests, and interrupts. Figure 18-2 is an overview of the control module environment.

Figure 18-2. Control Module Environment



18.2.1 Control Module Signals

Table 18-1 lists the control module hardware observability outputs configured to observe the debug signals of the device module. It describes the module signals and specifies their links to functions.

Table 18-1. Control Module I/O Description

Signal	I/O [1]	Description	Reset Value [2]
hw_dbg[31:0]	O	Internal hardware observability signals 0 to 31	HiZ

(1) I = Input; O = Output
(2) HiZ = High impedance

18.3 Control Module Integration

The control module of the device is on the L4-Core interconnect. It consists of four module instances:

- General core control module (SYSCTRL_GENERAL_CORE)
- General wakeup control module (SYSCTRL_GENERAL_WKUP)
- Device core control module (SYSCTRL_PADCONF_CORE)
- Device wakeup control module (SYSCTRL_PADCONF_WKUP)

For more information about the different control module instances, see Table 18-4.

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Each of these four module instances has an associated register set and shares one functional clock and one reset signal with the PRCM module. The exception is general core control module (SYSCTRL_GENERAL_CORE) which also receives a secondary functional clock, CORE_TS_FCLK. Table 18-2 describes the signals.

Table 18-2. Clocks and Resets

Clocks				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
SYSCTRL_GENERAL_WKUP	GEN_L4WKUP_CLK	WKUP_L4_ICLK2	PRCM	L4_WKUP interface/functional clock propagated to the general wakeup control module
SYSCTRL_GENERAL_CORE	GEN_L4CFG_CLK	CFG_L4_ICLK	PRCM	L4_CFG interface/functional clock propagated to the general core control module
	CORE_TS_FCLK	CORE_TS_FCLK	PRCM	Functional clock for the band gap state-machine instantiated in the general core control module
SYSCTRL_PADCONF_WKUP	PADCONF_L4WKUP_CLK	WKUP_L4_ICLK2	PRCM	L4_WKUP interface/functional clock propagated to the device wakeup control module
SYSCTRL_PADCONF_CORE	PADCONF_L4CFG_CLK	CFG_L4_ICLK	PRCM	L4_CFG interface/functional clock propagated to the device core control module
		Resets		
SYSCTRL_GENERAL_WKUP	GEN_WKUP_NONRET_RST	WKUP_PWRON_RST	PRCM	Internal power-on reset (POR) affecting the general wakeup control module
SYSCTRL_GENERAL_CORE	GEN_CORE_RET_RST	CORE_PWRON_RET_RST	PRCM	Internal POR affecting the general core control module
SYSCTRL_PADCONF_WKUP	PADCONF_WKUP_NONRET_RST	WKUP_PWRON_RST	PRCM	Internal POR affecting the device wakeup control module
SYSCTRL_PADCONF_CORE	PADCONF_CORE_RET_RST	CORE_PWRON_RET_RST	PRCM	Internal POR affecting the device core control module

Table 18-3. Hardware Requests

Interrupt Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
SYSCTRL_GENERAL_CORE	THERMAL_ALERT	MA_IRQ_126	CORTEX-A9 INTC	Interrupt generated by general core control module to CORTEX™-A9

NOTE: For a description of the interrupt sources, see Section 17.3.2,*Interrupt Requests to the Cortex-A9 MPU Interrupt Controller*.

The control module is reset by the internal POR, which is active low. The PRCM module provides a retention POR signal (CORE_PWRON_RET_RST) duplicated to both of the core control module instances, and a nonretention POR signal (WKUP_PWRON_RST) duplicated to each of the two wake-up control module instances in the control module. For more information, see , *Reset Domains*, in Chapter 3, *Power, Reset, and Clock Management*. The control module does not respond to a warm reset or to an L4-Core reset.

The main sequential logic within the system control module is accessible in a register file through the L4-Core interconnect. The PRCM module provides the CFG_L4_ICLK functional clock signal (L4_CFG clock domain) separately to each of the two core control submodules. In addition, an instantiated inside the general core control, the band gap state-machine receives its functional clock (CORE_TS_FCLK) from the PRCM module. For more information about this signal, see , *CM2 Clock Generator* in Chapter 3, *Power, Reset, and Clock Management*.

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The PRCM module also supplies the WKUP_L4_ICLK2 functional clock signal (L4_WKUP clock domain) to each of the two wake-up control module instances. For more information about this signal, see , *PRM Clock Source* in Chapter 3, *Power, Reset, and Clock Management*.

The PRCM module latches the sys_boot[7:0] pad signals at POR and exports them as vector to the SYSBOOT[7:0] input of the general core control module. It is scanned in the CONTROL_STATUS[7:0] SYS_BOOT bit field. For more information, see Section 27.2.4.2, *Booting Device Order Selection*, and Section 27.2.4.1, *Clock Source Selection.*

The thermal management subsystem inside the general core control module delivers one interrupt request (THERMAL_ALERT) to line MA_IRQ_126 of the MPU subsystem interrupt controller (INTC) (Cortex-A9 INTC), and delivers a thermal protection output signal (TSHUT) to the GPIO3 instance. For more information about the functional outputs of the thermal management control module, see Section 18.4.10.

The signal integration of the control module features:

- No IDLE hardware handshake
- No STANDBY hardware handshake
- No SAVE and RESTORE hardware handshake
- No wake-up request generation
- No DMA request generation
- One interrupt request (IRQ) – THERMAL_ALERT to the MPU subsystem
- A thermal shutdown protection signal (TSHUT) delivered to a GPIO3 input.
- Three functional clocks: two clocks in the CFG and one in the WKUP clock domains
- One retention and one nonretention internal power-on-based resets

Figure 18-3 shows the integration of the module in the device.

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Figure 18-3. Control Module Integration

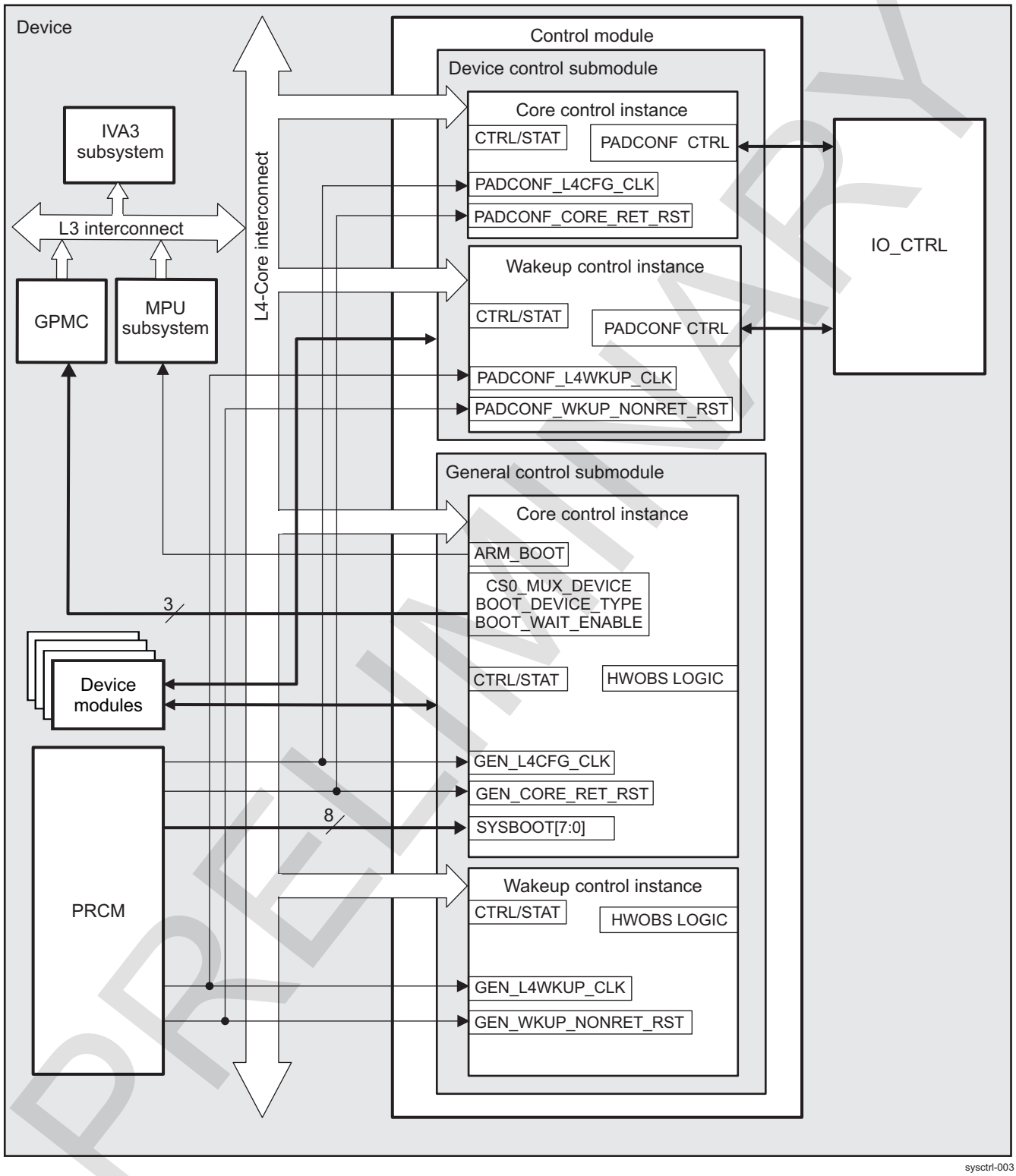

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Table 18-4 lists the integration attributes.

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Table 18-4. Integration Attributes

Module Instance	Attributes	
	Power Domain	Interconnect
SYSCTRL_GENERAL_WKUP	PD_WKUP	L4_WKUP
SYSCTRL_GENERAL_CORE	PD_CORE	L4_CFG
SYSCTRL_PADCONF_WKUP	PD_WKUP	L4_WKUP
SYSCTRL_PADCONF_CORE	PD_CORE	L4_CFG

Software sets the configuration registers to the desired values depending on the configuration of the requested device. Static device configuration registers can be set by software any time and are effective immediately.

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18.4 Control Module Functional Description

18.4.1 Control Module Block Diagram

The control module controls the settings of various device modules through the register configuration and internal signals. It also controls the pad configuration, pin functional multiplexing, and the routing of internal signals (such as PRCM signals or DMA requests) to output pins configured for hardware observability.

Figure 18-4 is the control module block diagram.

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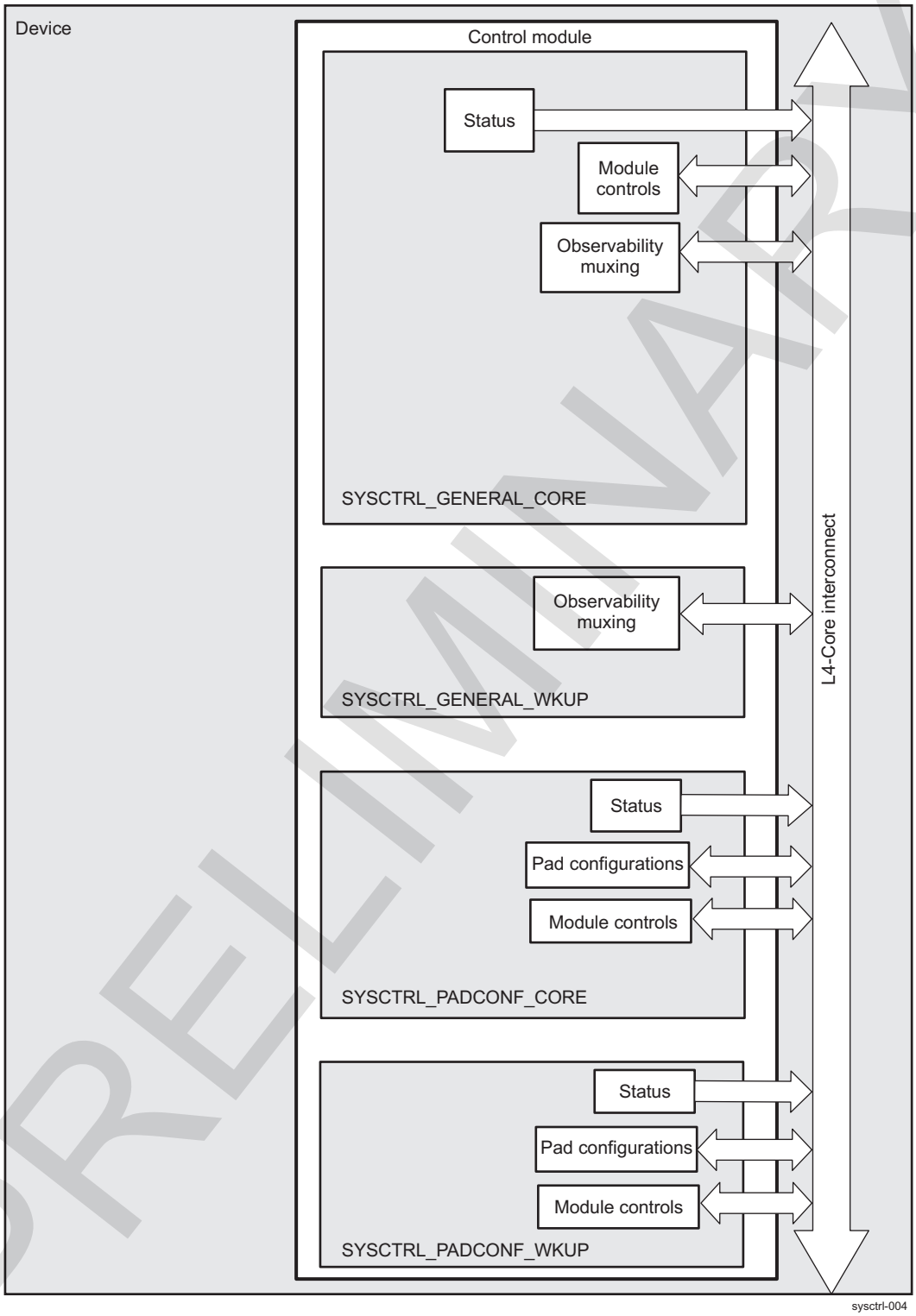
Figure 18-4. Control Module Block Diagram



The control submodules primarily implement a bank of registers accessible (read/write) by software and some read-only registers that provide status information.

The read/write registers in the general control module can be divided into the following classes:

- Hardware observability registers (32-bit read/write registers)

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- Status and configuration registers
- Boot registers
- eFuse ROM registers
- Miscellaneous functional registers

The read/write registers in the device(padconfiguration) control module can be divided into the following classes:

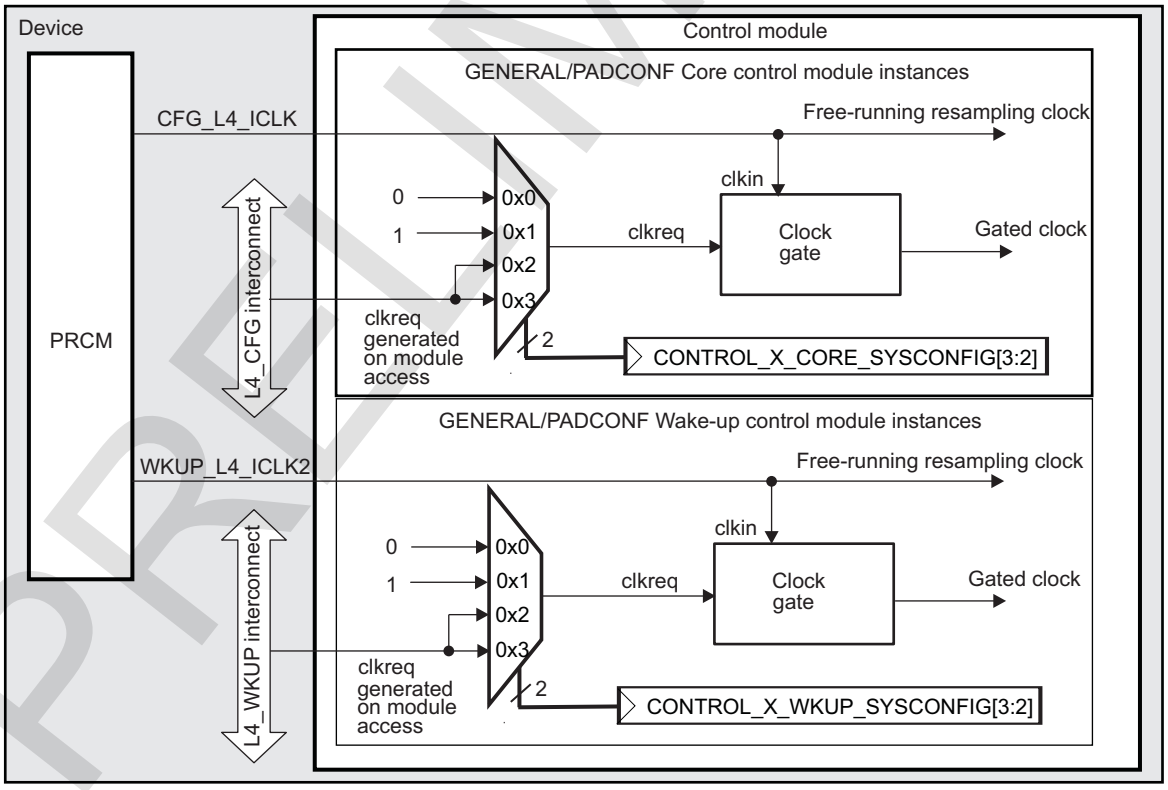
- Pad configuration registers (32-bit registers, one register for two pads)
- Pad groups (not individual per pad) associated registers for signal integrity parameters control (32-bit read/write registers)
- I/O cells associated specific control registers
- Device-specific status and configuration registers
- Miscellaneous functional registers

18.4.2 Control Module Clock Configuration

Figure 18-5 shows the distribution schema of the control module internal clock . Each CFG_L4_ICLK and WKUP_L4_ICLK2 source clock is internally distributed into two clock paths: the first path directly mirrors the source clock and is an always-running clock. It is used to synchronize and resample some of the module inputs. The other clock path can be internally gated within the module.

The CORE_TS_FCLK clock, which drives the general core control band gap state-machine, can also be locally gated through a dedicated bit in the CONTROL_TEMP_SENSOR register. For more information about the temperature module off mode, see Section 18.4.10, *Band Gap Voltage and Temperature Sensor*.

Figure 18-5. Control Module Internal Clock Paths



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The clock-gating strategy for L4 clocks is selected through the CONTROL_SYSCONFIG[3:2] IP_SYSCONFIG_IDLEMODE bit field available in each of the four control module instances. Table 18-5 describes the different possibilities for clock management. There are no PRCM software controls for the CFG_L4_ICLK and WKUP_L4_ICLK2 clocks in the control module. There are, however, clock activity status bits in the PRCM module.

The CORE_TS_FCLK has the following software controls: enable, status, and divider ratio, in the PRCM module. See , *Clock Domain Modes*, and , *CD_WKUP Clock Domain* , in Chapter 3, *Power, Reset, and Clock Management*.

Table 18-5. Internal Clock Gating Options

Feature	CONTROL_SYSCONFIG[3:2] IP_SYSCONFIG_IDLEMODE Value	Description
Local clock control	0b00	Clock is manually gated.
Local clock control	0b01	Clock is manually enabled.
Local clock autogating	0b10, 0b11	Clock is automatically gated when there is no access to the control module through the L4-interconnect.

18.4.3 Control Module Software Reset

The control module is not sensitive to software reset.

18.4.4 Control Module Power Management

18.4.4.1 Retention

The general core module and device core control module instances are fully built with retention flip-flops (RFFs) and are powered in the CORE power domain; thus, they can be in active or retention mode. The core instances lose their content when the CORE power domain is in off mode. In contrast to the core control instances, the control wake-up instances are always powered and active. For more information about the device low-power states, see, *Device Low-Power States*, in Chapter 3, *Power, Reset, and Clock Management*.

18.4.4.2 Power Management Protocols

The control module, which is slave on the L4 interconnect, does not support standby or idle mode protocols.

18.4.4.3 Save-and-Restore Mechanism

The control core module instances lose their contents when the CORE power domain is in off mode. To prevent this, before going to off mode, the core register context is copied by software into a dedicated SAR_RAM in the WKUP voltage domain. The save-and- restore (SAR) mechanism, controlled by the PRCM module, allows restoring registers to the value present before going to off mode. Thus, core domain registers have a correct configuration/state immediately after the core power is on again without requesting a software operation to reconfigure them.

Because the SAR mechanism is managed by software-accessible registers, no hardware-specific requirements exist. For more information about SAR, see , *Device Off State Management.*, in Chapter 3, *Power, Reset, and Clock Management*.

18.4.5 Hardware Requests

The control module does not generate DMA or wake-up requests. The general core control module generates one IRQ (THERMAL_ALERT) to the Cortex-A9 INTC (MA_IRQ_126 line). For more information, see Section 17.3.2, *Interrupt Requests to the Cortex-A9 MPU Interrupt Controller*.

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18.4.6 Control Module Initialization

The control module responds only to the internal POR and device type. At power-on, reset values for the registers define the *safe state* for the device. In the initialization mode, only modules to be used at boot time are associated with the pads. Other module inputs are internally tied and outputs pads are turned off. After POR, software must set the pad functional multiplexing and configuration registers to the desired values according to the requested device configuration. For more information, see Chapter 27, *Initialization*.

General-purpose (GP) devices include features that are inaccessible or unavailable. These inaccessible registers define the default or fixed device configuration or behavior.

The CONTROL_STATUS[7:0] SYS_BOOT boot field reflects the state of the sys_boot pins captured at POR in the PRCM module.

18.4.7 General Control Module Instances

18.4.7.1 General Core Control Module Instance

The SYSCTRL_GENERAL_CORE instance contains most of the control logic that provides the hardware observability features for different digital phase-locked loop (DPLL) clockout and DPLL-specific signals, DMA requests , IRQs, and other internal hardware signals. The general core control provides the system boot decoding logic and has control over the standard eFuse settings. The system configuration registers, specific function controls, and some peripheral control and status registers are also mapped there.

The register sets available within the SYSCTRL_GENERAL_CORE are:

- Observability control registers:
  - CONTROL_HWOBS_CONTROL
  - CONTROL_DEBOBS_FINAL_MUX_SEL
  - CONTROL_CONF_SDMA_REQ_SELx
  - CONTROL_CONF_CLK_SELx (where x = 0 to 2)
  - CONTROL_CONF_DPLL_X_SEL (where X = FREQLOCK, TINITZ, PHASELOCK, TENABLE, TENABLEDIV, BYPASSACK, IDLE)
- Part of the debug view channel selection registers: CONTROL_CORE_CONF_DEBUG_SEL_TST_X
- MMU address translation-related registers: CONTROL_CORTEX_M3_MMUADDRTRANSLTR and CONTROL_CORTEX_M3_MMUADDRLOGICTR
- Standard fuse registers: CONTROL_STD_FUSE_X
- Clock gating configuration register: CONTROL_GEN_CORE_SYSCONFIG
- Control status register: CONTROL_STATUS
- Peripheral control registers:
  - CONTROL_TEMP_SENSOR
  - CONTROL_BANDGAP_CTRL
  - CONTROL_BANDGAP_COUNTER
  - CONTROL_BANDGAP_THRESHOLD
  - CONTROL_TSHUT_THRESHOLD
  - CONTROL_BANDGAP_STATUS
  - CONTROL_DSS_CONTROL
  - CONTROL_USBOTGHS_CONTROL
  - CONTROL_LDOSRAM_MPU_VOLTAGE_CTRL
  - Etc.

18.4.7.2 General Wakeup Control Module Instance

The registers associated with this module are:

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- Clock gating configuration register: CONTROL_GEN_WKUP_SYSCONFIG
- Register with spare bits: CONTROL_OCPREG_SPARE
- Part of the debug view channel selection registers: CONTROL_WKUP_CONF_DEBUG_SEL_TST_X

18.4.7.3 Device Core Control Module Instance

The SYSCTRL_PADCONF_CORE instance provides the device-specific pad control features, such as pullup/down I/O configuration and pad functional multiplexing. Wake-up control/status features are also subjects of the device core control.

The registers associated with this module are:

- Clock gating configuration register: CONTROL_PADCONF_CORE_SYSCONFIG
- Different peripheral pad mode configuration and wake-up status/configuration registers:
  - CONTROL_CORE_PAD0_X_PAD1_Y
  - CONTROL_PADCONF_WAKEUPEVENTx
  - CONTROL_PADCONF_GLOBAL
  - CONTROL_SMARTxIO
  - CONTROL_C2CIO_PADCONF_0
  - Etc.
- Peripheral pad voltage-level control register: CONTROL_PADCONF_MODE
- Miscellaneous controls for different device interface modules: CONTROL_X registers, such as the CONTROL_EMIF register (including the CONTROL_EFUSE registers)

18.4.7.4 Device Wake-Up Control Module Instance

Configuration registers for all pads linked to the wake-up voltage domain are in the WKUP device control module. The registers instantiated are:

- Clock gating configuration register: CONTROL_PADCONF_WKUP_SYSCONFIG
- CONTROL_WKUP_PAD0_X_PAD1_Y registers for configuring FREF clock oscillator pads, reset signals, and power mode pad configurations

NOTE: SYSCTRL_PADCONF_X alias notifies a device control module instance.

Table 18-110 shows the memory size and base addresses assigned to the different control module instances

18.4.8 Pad Functional Multiplexing and Configuration

After POR, software must set the pad functional multiplexing and configuration registers to the desired values according to the requested device configuration. The configuration is controlled by pads or a group of pads. Each configurable pin has its own configuration register for pullup/down control and for assignment to a given module.

Two sets of 32-bit registers provide the pad functional multiplexing and configuration feature of the control module. The first set of registers (CONTROL_CORE_PAD0_X_PAD1_Y) configures the pads in the CORE power domain. The second set of registers (CONTROL_WKUP_PAD0_X_PAD1_Y) configures the pads in the WKUP power domain.

The pad configuration as defined in this module is used in the IO_CTRL logic along with the gating and protection features. The gating feature is implemented for the output pads. The protection feature is implemented for input lines. These features implement additional control and multiplexing capabilities hard-wired in the IO_CTRL logic and driven by the state and/or logic of the internal device.

The gating feature allows forcing an output pad to a fixed value (Z, pullup, pulldown, 1, 0) or to a given internal signal. Each gating command is defined with a logic equation and the output state or value to be set on the pad when the logic equation is "True."

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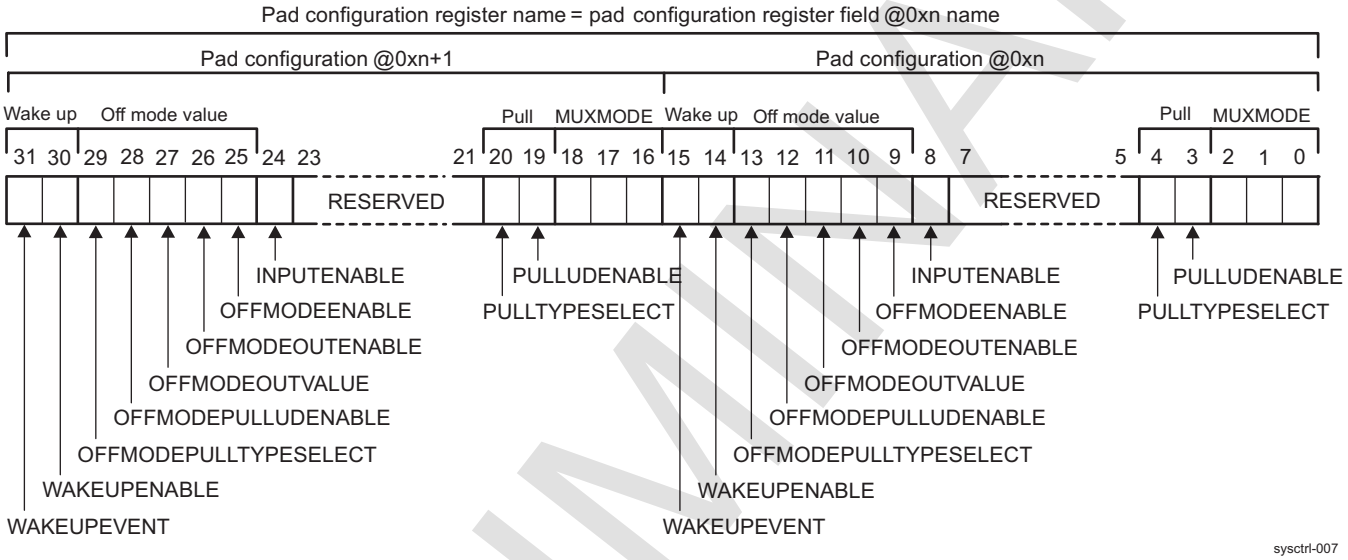
The protection feature provides control on each input line of the control module when no pad is assigned to this input (protected value). When POR is released, the value on the pad is driven by the default configuration of the control module. This configuration is usually aligned with the default value selected on the I/O cell. The protected value can be logical level (0 or 1) or a signal from a pad; it is selected when none of the pad_x.MuxMod selects a device input.

Each 32-bit pad configuration register controls two pads: the first pad is controlled by the 16 least-significant bits (LSBs), and the second pad is controlled by the 16 most-significant bits (MSBs); thus, one pad configuration register provides control for two different pins. After POR, software sets the pad functional multiplexing and configuration registers to the requested device pad configurations. Data written in these registers directly commands the multiplexing of the pad configuration logic. Figure 18-6 shows the 16-bit-wide pad configuration register field associated with each pin.

Figure 18-6. Pad Configuration Register Functionality



NOTE: These registers can be accessed using 8-, 16-, and 32-bit operations.

The functional bits of a pad configuration register field are divided into the following five fields:

- MUXMODE (3 bits) defines the multiplexing mode applied to the pin. A mode corresponds to the selection of the function mapped on the pin with seven (0 to 6) possible functional modes for each pin.
- PULL (2 bits) for combinational pullup/down configuration:
  - PULLTYPESELECT: Pullup/down type selection for the pin
  - PULLUDENABLE: Enables pullup/down feature for the pin
- INPUTENABLE (1 bit) drives an input enable signal to the I/O CTRL.
  - INPUTENABLE = 0: Input disable. Pin is configured only in output mode.
  - INPUTENABLE = 1: Input enable. Pin is configured in bidirectional mode.
- Off mode values (1 bit) override the pin state when the OFFMODEENABLE bit in CONTROL_CORE_PAD0_X_PAD1_Y is set and off mode is active. This feature allows having separate configurations (5 bits) for the pins when in off mode:
  - OFFMODEENABLE: Off mode pin state override control. Set to 1 to enable the feature and set to 0 to disable it.
  - OFFMODEOUTENABLE: Off mode output enable value. Set to 0 to enable the feature and set to 1 to disable it.
  - OFFMODEOUTVALUE: Off mode output value.
  - OFFMODEPULLUDENABLE: Off mode pullup/down feature enable
  - OFFMODEPULLTYPESELECT: Off mode pullup/down type selection

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- Wake-up bits (2 bits):
  - WAKEUPENABLE: Enable wake-up detection on input. It is also the off mode input enable value.
  - WAKEUPEVENT: Wake-up event status for the pin

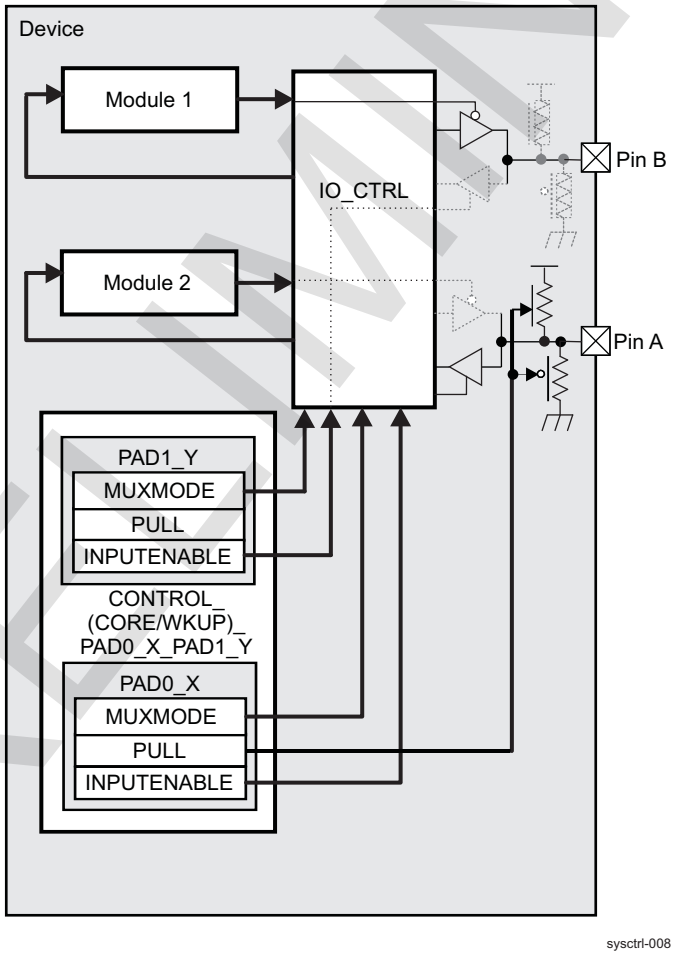
CAUTION

The OFFOUTENABLE and OFFOUTVALUE bits are functional only if the pad configuration supports output mode on at least one MUXMODE. For a pad that supports only the input feature, the OFFOUTENABLE and OFFOUTVALUE bits cannot be configured (they are don't care and read always returns 0).

NOTE: Because off-mode affects pads only in the CORE power domain, OFFMODE-related bits are not present in the pad configuration registers of the WKUP power domain .

Figure 18-7 shows the pad configuration functionality when off mode is inactive. For more information about off mode, see Section 18.4.8.4, *Off Mode PAD Control Overview*.

Figure 18-7. Pad Configuration Diagram



The I/O pads are controlled by software by:

- Writing to the CONTROL_(CORE/WKUP)_PAD0_X_PAD1_Y registers in the device control module for I/O and pullup/down configuration
- Writing to the GPIOi.GPIO_OE registers in the GPIO module for I/O configuration

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For more information about how to configure the I/O pads, see Section 18.5.1.2.5, *Pad Configuration Programming Points*.

For more information about the GPIO module, see Section 25.4.8, *General-Purpose Interface Data Input/Output Capabilities.*

NOTE: For the proper functioning of the following modules, the INPUTENABLE bit in the corresponding pad configuration register must be set to 1 for pads configured to drive output clocks:

- GPMC
- I2Ci
- MMCi
- HSUSB HOST
- McPDM

NOTE: For a correct configuration of each pin direction (input, output, bidirectional), the CONTROL_(CORE/WKUP)_PAD0_X_PAD1_Y and GPIOi.GPIO_OE registers must be written.

NOTE: Software INPUTENABLE controls are not available for the lpddr21_x, lpddr22_x, usbb1_hsic_x, and usbb2_hsic_x pads. Once their buffers are enabled they are always bidirectional. For more information, see Section 18.4.12.9.2, *High-Speed I/O Buffers With Impedance, Slew Rate, and Weak Driver Settings*.

Table 18-6 lists the bit directions of the CONTROL_(CORE/WKUP)_PAD0_X_PAD1_Y registers.

Table 18-6. Bit Meanings for CONTROL_(CORE/WKUP)_PAD0_X_PAD1_Y Registers

Pad Configuration Bit	Bit Meaning	
	0	1
PULLUDENABLE	Not activated	Activated
PULLTYPESELECT	Pulldown	Pullup
INPUTENABLE	Input enable signal is inactive.	Input enable signal is active.
OFFMODEENABLE	Off mode values are invalid.	Off mode values are valid.
OFFMODEOUTENABLE	Output	Input
OFFMODEOUTVALUE	Low	High
OFFMODEPULLUDENABLE	Not activated	Activated
OFFMODEPULLTYPESELECT	Pulldown	Pullup
WAKEUPENABLE	Disable I/O wake-up function.	Enable I/O wake-up function.
WAKEUPEVENT	Wake-up event is not detected.	Wake-up event is detected.
MUXMODE bits	See Table 18-7, *Mode Selection*.	See Table 18-7, *Mode Selection*.

18.4.8.1 Mode Selection

Table 18-7 lists the multiplexing modes and settings.

Table 18-7. Mode Selection

MUXMODE	Selected Mode
0b000	Primary mode = Mode 0
0b001	Mode 1
0b010	Mode 2
0b011	Mode 3

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Table 18-7. Mode Selection (continued)

MUXMODE	Selected Mode
0b100	Mode 4
0b101	Mode 5
0b110	Mode 6
0b111	Safe mode = Mode 7

The MUXMODE field in the CONTROL_CORE_PAD0_X_PAD1_Y and CONTROL_WKUP_PAD0_X_PAD1_Y registers defines the multiplexing mode applied to the pad. Modes are referred to by their decimal (from 0 to 7) or binary (from 0b000 to 0b111) representation. Functional modes are defined from 0b000 to 0b110; mode 0b111 is referred to as the safe mode.

For most pads, the reset value for the MUXMODE field in the CONTROL_CORE_PAD0_X_PAD1_Y and CONTROL_WKUP_PAD0_X_PAD1_Y registers is 0b111. The exceptions are pads to be used at boot time to transfer data from selected peripherals to the external flash memory.

Mode 0 is the primary mode. When mode 0 is set, the function mapped to the pin corresponds to the name of the pin.

Modes 1–6 are possible modes for alternate functions. On each pin, some modes are used effectively for alternate functions, while other modes are unused and correspond to no functional configuration.

Safe mode (Mode 7) avoids any risk of electrical contention by configuring the pin as an input with no functional interface mapped to it. Safe mode is used mainly as the default mode for all pins containing no mandatory interface at the release of POR.

NOTE: When a pad is set into a mux mode that is not defined by pin multiplexing, the pad is actually set undriven (HiZ) with potential pullup/down.

For more information about the configurable mode on each pin, see Table 18-10 and Table 18-9.

NOTE: Pad names are signal names available in mode 0.

18.4.8.2 Pull Selection

There is no automatic gating control to ensure that internal weak pulldown/pullup resistors on a pad are disconnected whenever pad is configured as output. If a pad is always configured in output mode, it is recommended for user software to disable any internal pull resistor tied to it, to avoid unnecessary consumption.

Table 18-8. Pull Selection

PULL		Pin Behavior
PULLTYPESELECT	PULLUDENABLE	
0b0	0b0	Pulldown selected but not activated
0b0	0b1	Pulldown selected and activated
0b1	0b0	Pullup selected but not activated
0b1	0b1	Pullup selected and activated

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For more information about the pull available on each pin, see Table 18-10 and Table 18-9.

NOTE: Software controls for internal active mode pullups and pulldowns on the lpddr21_x and lpddr22_x pads are available in the CONTROL_LPDDR2IO1_0 through CONTROL_LPDDR2IO1_2 and CONTROL_LPDDR2IO2_0 through CONTROL_LPDDR2IO2_2 registers, respectively.

Software controls for internal active mode pullups and pulldowns on the usbb1_hsic_x and usbb2_hsic_x pads are available in the CONTROL_USBB_HSIC register.

For more information, see Section 18.4.12.9.2, *High-Speed I/O Buffers With Impedance, Slew Rate, and Weak Driver Settings*.

18.4.8.2.1 Generic Pad Configuration Bit Fields vs I/O Cell Mapping

Figure 18-8 provides a generic view of the relations between the pad configuration controls and I/O cell functions for a pad configured in active mode.

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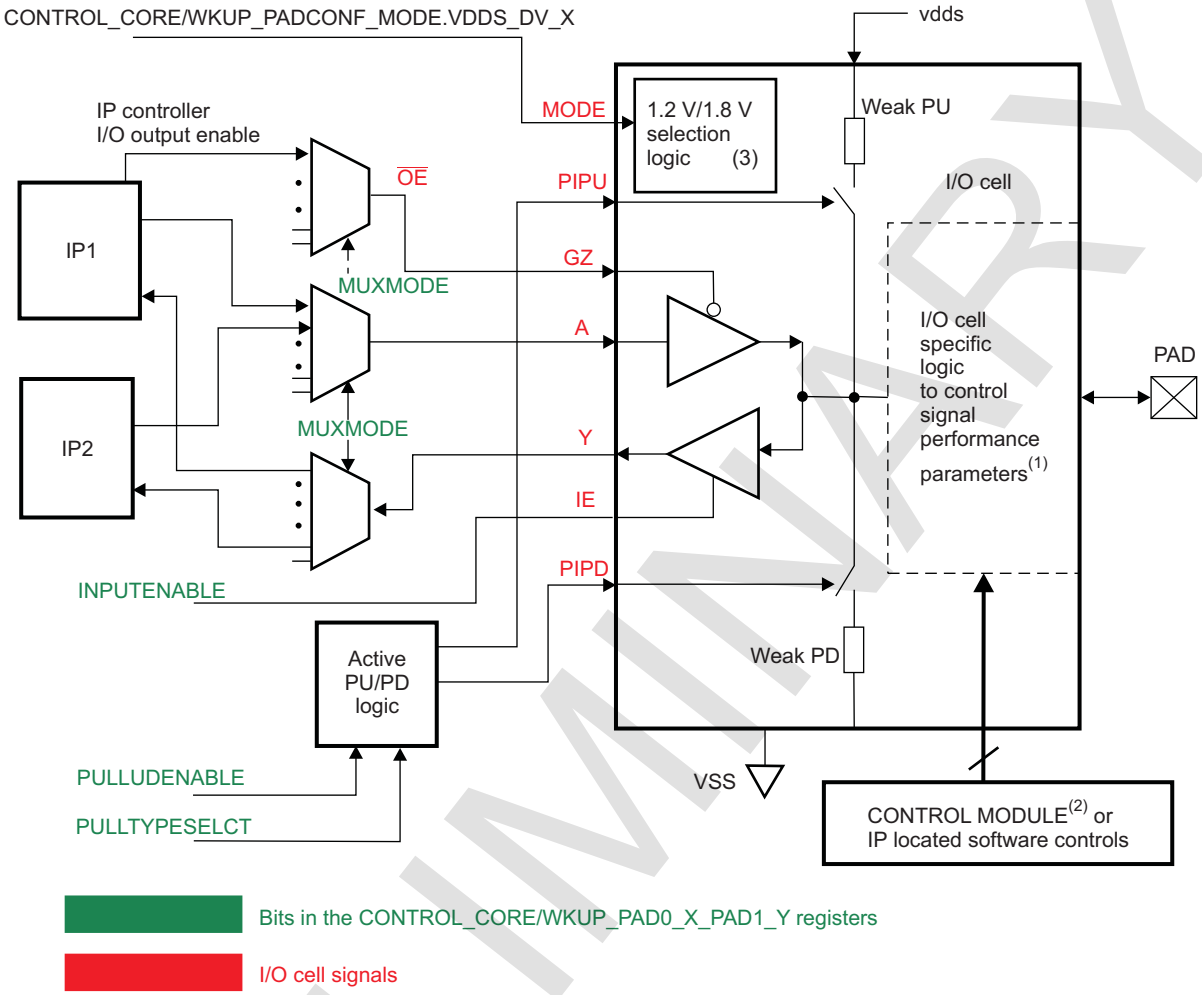
Figure 18-8. Active Mode Pad Configuration Bit Fields vs I/O Cell Mapping



(1) Section 18.4.12.9, *Signal Integrity Parameter Control Registers With Pad Group Assignment*, summarizes the I/O cell signal performance settings. For more information about the controlled I/O cell electrical parameters and interdependency considerations, see the device data manual.

(2) For information about the mapping of software controls in the control module versus different device pads, see Section 18.4.12.9.9, *Device Interfaces Signal Group Controls Mapping*. For more information about interface-specific signal parameter settings, see the device data manual.

(3) The CONTROL_CORE/WKUP_PADCONF_MODE.VDDS_DV_x bit is available for each I/O that is part of the dual-voltage domain group x. For more information about 1.2-V/1.8-V dual-voltage domain I/Os, see the device data manual. For more information about peripheral dual-voltage software controls versus pad group mapping, see Section 18.4.12.10, *Dual-Voltage-Supplied Peripheral Controls*.

NOTE: Dynamic switching between 1.2-V and 1.8-V voltage modes on dual-voltage peripheral I/Os is not allowed.

18.4.8.3 Pad Multiplexing Register Fields

Table 18-10 and Table 18-9 provide for each pad configuration register field the address offset and associated signal name for each multiplexing mode (as set by the MUXMODE bit field). Mode 0 is always defined. Modes with no signal name are undefined for the given pad. For more information about default padconfiguration settings (POR values) for pads in the CORE power domain, seeSection 18.6.7, *SYSCTRL_PADCONF_CORE Register Description;* for pads in the WKUP power domain, see Section 18.6.9, *SYSCTRL_PADCONF_WKUP Register Description.*

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NOTE:

- Table 18-9 lists the pad configuration registers instantiated in the WKUP power domain that drive the pads in the WKUP power domain. Table 18-10 lists the pad configuration registers instantiated in the CORE power domain that drive the pads in the CORE power domain.
- In Table 18-10 and Table 18-9, an empty cell indicates that the mode or pull is not available for this pin.

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Table 18-9. Device Wake-Up Control Module Pad Configuration Register Fields

SYSCTRL_PADCONF_WKUP.[Register name]	Address Offset	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
CONTROL_WKUP_PAD0_GPIO_WK0_PAD1_GPIO_WK1[15:0]	0x040	reserved			gpio_wk0	c2c_pwkup		hw_dbg1	safe_mode
CONTROL_WKUP_PAD0_GPIO_WK0_PAD1_GPIO_WK1[31:16]	0x040	reserved			gpio_wk1			hw_dbg2	safe_mode
CONTROL_WKUP_PAD0_GPIO_WK2_PAD1_GPIO_WK3[15:0]	0x044	reserved			gpio_wk2			hw_dbg3	safe_mode
CONTROL_WKUP_PAD0_GPIO_WK2_PAD1_GPIO_WK3[31:16]	0x044	reserved			gpio_wk3			hw_dbg4	safe_mode
CONTROL_WKUP_PAD0_GPIO_WK4_PAD1_SR_SCL[15:0]	0x048	reserved			gpio_wk4			hw_dbg5	safe_mode
CONTROL_WKUP_PAD0_GPIO_WK4_PAD1_SR_SCL[31:16]	0x048	sr_scl							
CONTROL_WKUP_PAD0_SR_SDA_PAD1_FREF_XTAL_IN[15:0]	0x04C	sr_sda							
CONTROL_WKUP_PAD0_SR_SDA_PAD1_FREF_XTAL_IN[31:16]	0x04C	fref_xtal_in				c2c_ wakereqin			
CONTROL_WKUP_PAD0_FREF_SLICER_IN_PAD1_FREF_CLK_IOREQ[15:0]	0x050	fref_slicer_in			gpi_wk5	c2c_ wakereqin			safe_mode
CONTROL_WKUP_PAD0_FREF_SLICER_IN_PAD1_FREF_CLK_IOREQ[31:16]	0x050	fref_clk_ioreq							
CONTROL_WKUP_PAD0_FREF_CLK0_OUT_PAD1_FREF_CLK3_REQ[15:0]	0x054	fref_clk0_out	fref_clk1_req	Reserved	gpio_wk6		sdmmc2_ dat7	hw_dbg6	safe_mode
CONTROL_WKUP_PAD0_FREF_CLK0_OUT_PAD1_FREF_CLK3_REQ[31:16]	0x054	fref_clk3_req	fref_clk1_req	Reserved	gpio_wk30	c2c_ wakereqin	sdmmc2_ dat4	hw_dbg7	safe_mode
CONTROL_WKUP_PAD0_FREF_CLK3_OUT_PAD1_FREF_CLK4_REQ[15:0]	0x058	fref_clk3_out	fref_clk2_req	Reserved	gpio_wk31	c2c_ wakereqout	sdmmc2_ dat5	hw_dbg8	safe_mode
CONTROL_WKUP_PAD0_FREF_CLK3_OUT_PAD1_FREF_CLK4_REQ[31:16]	0x058	fref_clk4_req	fref_clk5_out		gpio_wk7		sdmmc2_ dat6	hw_dbg9	

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Table 18-9. Device Wake-Up Control Module Pad Configuration Register Fields (continued)

SYSCTRL_PADCONF_WKUP.[Register name]	Address Offset	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
CONTROL_WKUP_PAD0_FREF_CLK4_OUT_PAD1_SYS_32K[15:0]	0x05C	fref_clk4_out			gpio_wk8			hw_dbg10	
CONTROL_WKUP_PAD0_FREF_CLK4_OUT_PAD1_SYS_32K[31:16]	0x05C	sys_32k							
CONTROL_WKUP_PAD0_SYS_NRESPWRON_PAD1_SYS_NRESWARM[15:0]	0x060	sys_nrespwron							
CONTROL_WKUP_PAD0_SYS_NRESPWRON_PAD1_SYS_NRESWARM[31:16]	0x060	sys_nreswarm							
CONTROL_WKUP_PAD0_SYS_PWR_REQ_PAD1_SYS_PWRON_RESET_OUT[15:0]	0x064	sys_pwr_req							
CONTROL_WKUP_PAD0_SYS_PWR_REQ_PAD1_SYS_PWRON_RESET_OUT[31:16]	0x064	sys_pwron_reset_out			gpio_wk29		hw_dbg0	hw_dbg11	
CONTROL_WKUP_PAD0_SYS_BOOT6_PAD1_SYS_BOOT7[15:0]	0x068	sys_boot6	dpm_emu18		gpio_wk9	c2c_wakereqout		hw_dbg12	safe_mode
CONTROL_WKUP_PAD0_SYS_BOOT6_PAD1_SYS_BOOT7[31:16]	0x068	sys_boot7	dpm_emu19		gpio_wk10			hw_dbg13	safe_mode
CONTROL_WKUP_PAD0_JTAG_NTRST_PAD1_JTAG_TCK[15:0]	0x06C	jtag_ntrst							
CONTROL_WKUP_PAD0_JTAG_NTRST_PAD1_JTAG_TCK[31:16]	0x06C	jtag_tck							safe_mode
CONTROL_WKUP_PAD0_JTAG_RTCK_PAD1_JTAG_TMS_TMSC[15:0]	0x070	jtag_rtck							
CONTROL_WKUP_PAD0_JTAG_RTCK_PAD1_JTAG_TMS_TMSC[31:16]	0x070	jtag_tms_tmsc							safe_mode
CONTROL_WKUP_PAD0_JTAG_TDI_PAD1_JTAG_TDO[15:0]	0x074	jtag_tdi							

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Table 18-9. Device Wake-Up Control Module Pad Configuration Register Fields (continued)

SYSCTRL_PADCONF_WKUP.[Register name]	Address Offset	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
CONTROL_WKUP_PAD0_JTAG_TDI_PAD1_JTAG_TDO[31:16]	0x074	jtag_tdo							

Table 18-10. Device Core Control Module Pad Configuration Register Fields

SYSCTRL_PADCONF_CORE.[Register Name]	Address Offset	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
CONTROL_CORE_PAD0_GPMC_AD0_PAD1_GPMC_AD1[15:0]	0x040	gpmc_ad0	sdmmc2_dat0						
CONTROL_CORE_PAD0_GPMC_AD0_PAD1_GPMC_AD1[31:16]	0x040	gpmc_ad1	sdmmc2_dat1						
CONTROL_CORE_PAD0_GPMC_AD2_PAD1_GPMC_AD3[15:0]	0x044	gpmc_ad2	sdmmc2_dat2						
CONTROL_CORE_PAD0_GPMC_AD2_PAD1_GPMC_AD3[31:16]	0x044	gpmc_ad3	sdmmc2_dat3						
CONTROL_CORE_PAD0_GPMC_AD4_PAD1_GPMC_AD5[15:0]	0x048	gpmc_ad4	sdmmc2_dat4	sdmmc2_dir_dat0					
CONTROL_CORE_PAD0_GPMC_AD4_PAD1_GPMC_AD5[31:16]	0x048	gpmc_ad5	sdmmc2_dat5	sdmmc2_dir_dat1					
CONTROL_CORE_PAD0_GPMC_AD6_PAD1_GPMC_AD7[15:0]	0x04C	gpmc_ad6	sdmmc2_dat6	sdmmc2_dir_cmd					
CONTROL_CORE_PAD0_GPMC_AD6_PAD1_GPMC_AD7[31:16]	0x04C	gpmc_ad7	sdmmc2_dat7	sdmmc2_clk_fdbk					
CONTROL_CORE_PAD0_GPMC_AD8_PAD1_GPMC_AD9[15:0]	0x050	gpmc_ad8	kpd_row0	c2c_data15	gpio_32		sdmmc1_dat0		
CONTROL_CORE_PAD0_GPMC_AD8_PAD1_GPMC_AD9[31:16]	0x050	gpmc_ad9	kpd_row1	c2c_data14	gpio_33		sdmmc1_dat1		
CONTROL_CORE_PAD0_GPMC_AD10_PAD1_GPMC_AD11[15:0]	0x054	gpmc_ad10	kpd_row2	c2c_data13	gpio_34		sdmmc1_dat2		

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Table 18-10. Device Core Control Module Pad Configuration Register Fields (continued)

SYSCTRL_PADCONF_CORE.[Register Name]	Address Offset	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
CONTROL_CORE_PAD0_GPMC_AD10_PAD1_GPMC_AD11[31:16]	0x054	gpmc_ad11	kpd_row3	c2c_ data12	gpio_35		sdmmc1_ dat3		
CONTROL_CORE_PAD0_GPMC_AD12_PAD1_GPMC_AD13[15:0]	0x058	gpmc_ad12	kpd_col0	c2c_ data11	gpio_36		sdmmc1_ dat4		
CONTROL_CORE_PAD0_GPMC_AD12_PAD1_GPMC_AD13[31:16]	0x058	gpmc_ad13	kpd_col1	c2c_ data10	gpio_37		sdmmc1_ dat5		
CONTROL_CORE_PAD0_GPMC_AD14_PAD1_GPMC_AD15[15:0]	0x05C	gpmc_ad14	kpd_col2	c2c_ data9	gpio_38		sdmmc1_ dat6		
CONTROL_CORE_PAD0_GPMC_AD14_PAD1_GPMC_AD15[31:16]	0x05C	gpmc_ad15	kpd_col3	c2c_ data8	gpio_39		sdmmc1_ dat7		
CONTROL_CORE_PAD0_GPMC_A16_PAD1_GPMC_A17[15:0]	0x060	gpmc_a16	kpd_row4	c2c_ datain0	gpio_40	venc_ 656_data0			safe_mode
CONTROL_CORE_PAD0_GPMC_A16_PAD1_GPMC_A17[31:16]	0x060	gpmc_a17	kpd_row5	c2c_ datain1	gpio_41	venc_ 656_data1			safe_mode
CONTROL_CORE_PAD0_GPMC_A18_PAD1_GPMC_A19[15:0]	0x064	gpmc_a18	kpd_row6	c2c_ datain2	gpio_42	venc_ 656_data2			safe_mode
CONTROL_CORE_PAD0_GPMC_A18_PAD1_GPMC_A19[31:16]	0x064	gpmc_a19	kpd_row7	c2c_ datain3	gpio_43	venc_ 656_data3			safe_mode
CONTROL_CORE_PAD0_GPMC_A20_PAD1_GPMC_A21[15:0]	0x068	gpmc_a20	kpd_col4	c2c_ datain4	gpio_44	venc_ 656_data4			safe_mode
CONTROL_CORE_PAD0_GPMC_A20_PAD1_GPMC_A21[31:16]	0x068	gpmc_a21	kpd_col5	c2c_ datain5	gpio_45	venc_ 656_data5			safe_mode
CONTROL_CORE_PAD0_GPMC_A22_PAD1_GPMC_A23[15:0]	0x06C	gpmc_a22	kpd_col6	c2c_ datain6	gpio_46	venc_ 656_data6			safe_mode
CONTROL_CORE_PAD0_GPMC_A22_PAD1_GPMC_A23[31:16]	0x06C	gpmc_a23	kpd_col7	c2c_ datain7	gpio_47	venc_ 656_data7			safe_mode
CONTROL_CORE_PAD0_GPMC_A24_PAD1_GPMC_A25[15:0]	0x070	gpmc_a24	kpd_col8	c2c_ clkout0	gpio_48				safe_mode

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Table 18-10. Device Core Control Module Pad Configuration Register Fields (continued)

SYSCTRL_PADCONF_CORE.[Register Name]	Address Offset	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
CONTROL_CORE_PAD0_GPMC_A24_PAD1_GPMC_A25[31:16]	0x070	gpmc_a25		c2c_ clkout1	gpio_49				safe_mode
CONTROL_CORE_PAD0_GPMC_NCS0_PAD1_GPMC_NCS1[15:0]	0x074	gpmc_ncs0			gpio_50	sys_ndmareq0			
CONTROL_CORE_PAD0_GPMC_NCS0_PAD1_GPMC_NCS1[31:16]	0x074	gpmc_ncs1		c2c_ dataout6	gpio_51				safe_mode
CONTROL_CORE_PAD0_GPMC_NCS2_PAD1_GPMC_NCS3[15:0]	0x078	gpmc_ncs2	kpd_row8	c2c_ dataout7	gpio_52				safe_mode
CONTROL_CORE_PAD0_GPMC_NCS2_PAD1_GPMC_NCS3[31:16]	0x078	gpmc_ncs3	gpmc_dir	c2c_ dataout4	gpio_53				safe_mode
CONTROL_CORE_PAD0_GPMC_NWP_PAD1_GPMC_CLK[15:0]	0x07C	gpmc_nwp	dsi1_te0		gpio_54	sys_ndmareq1			
CONTROL_CORE_PAD0_GPMC_NWP_PAD1_GPMC_CLK[31:16]	0x07C	gpmc_clk			gpio_55	sys_ndmareq2	sdmmc1_ cmd		
CONTROL_CORE_PAD0_GPMC_NADV_ALE_PAD1_GPMC_NOE[15:0]	0x080	gpmc_nadv_ale	dsi1_te1		gpio_56	sys_ndmareq3	sdmmc1_ clk		
CONTROL_CORE_PAD0_GPMC_NADV_ALE_PAD1_GPMC_NOE[31:16]	0x080	gpmc_noe	sdmmc2_ clk						
CONTROL_CORE_PAD0_GPMC_NWE_PAD1_GPMC_NBE0_CLE[15:0]	0x084	gpmc_nwe	sdmmc2_ cmd						
CONTROL_CORE_PAD0_GPMC_NWE_PAD1_GPMC_NBE0_CLE[31:16]	0x084	gpmc_nbe0_cle	dsi2_te0		gpio_59				
CONTROL_CORE_PAD0_GPMC_NBE1_PAD1_GPMC_WAIT0[15:0]	0x088	gpmc_nbe1		c2c_ dataout5	gpio_60				safe_mode
CONTROL_CORE_PAD0_GPMC_NBE1_PAD1_GPMC_WAIT0[31:16]	0x088	gpmc_wait0	dsi2_te1		gpio_61				
CONTROL_CORE_PAD0_GPMC_WAIT1_PAD1_GPMC_WAIT2[15:0]	0x08C	gpmc_wait1		c2c_ dataout2	gpio_62				safe_mode

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Table 18-10. Device Core Control Module Pad Configuration Register Fields (continued)

SYSCTRL_PADCONF_CORE.[Register Name]	Address Offset	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
CONTROL_CORE_PAD0_GPMC_WAIT1_PAD1_GPMC_WAIT2[31:16]	0x08C	gpmc_wait2	usbc1_icusb_txen	c2c_dataout3	gpio_100	sys_ndmareq0			safe_mode
CONTROL_CORE_PAD0_GPMC_NCS4_PAD1_GPMC_NCS5[15:0]	0x090	gpmc_ncs4	dsi1_te0	c2c_clkin0	gpio_101	sys_ndmareq1			safe_mode
CONTROL_CORE_PAD0_GPMC_NCS4_PAD1_GPMC_NCS5[31:16]	0x090	gpmc_ncs5	dsi1_te1	c2c_clkin1	gpio_102	sys_ndmareq2			safe_mode
CONTROL_CORE_PAD0_GPMC_NCS6_PAD1_GPMC_NCS7[15:0]	0x094	gpmc_ncs6	dsi2_te0	c2c_dataout0	gpio_103	sys_ndmareq3			safe_mode
CONTROL_CORE_PAD0_GPMC_NCS6_PAD1_GPMC_NCS7[31:16]	0x094	gpmc_ncs7	dsi2_te1	c2c_dataout1	gpio_104				safe_mode
CONTROL_CORE_PAD0_GPIO63_PAD1_GPIO64[15:0]	0x098	Reserved			gpio_63				safe_mode
CONTROL_CORE_PAD0_GPIO63_PAD1_GPIO64[31:16]	0x098	Reserved			gpio_64				safe_mode
CONTROL_CORE_PAD0_GPIO65_PAD1_GPIO66[15:0]	0x09C	Reserved			gpio_65				safe_mode
CONTROL_CORE_PAD0_GPIO65_PAD1_GPIO66[31:16]	0x09C	Reserved			gpio_66				safe_mode
CONTROL_CORE_PAD0_CSI21_DX0_PAD1_CSI21_DY0[15:0]	0x0A0	csi21_dx0			gpi_67				safe_mode
CONTROL_CORE_PAD0_CSI21_DX0_PAD1_CSI21_DY0[31:16]	0x0A0	csi21_dy0			gpi_68				safe_mode
CONTROL_CORE_PAD0_CSI21_DX1_PAD1_CSI21_DY1[15:0]	0x0A4	csi21_dx1			gpi_69				safe_mode
CONTROL_CORE_PAD0_CSI21_DX1_PAD1_CSI21_DY1[31:16]	0x0A4	csi21_dy1			gpi_70				safe_mode
CONTROL_CORE_PAD0_CSI21_DX2_PAD1_CSI21_DY2[15:0]	0x0A8	csi21_dx2			gpi_71				safe_mode
CONTROL_CORE_PAD0_CSI21_DX2_PAD1_CSI21_DY2[31:16]	0x0A8	csi21_dy2			gpi_72				safe_mode

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Table 18-10. Device Core Control Module Pad Configuration Register Fields (continued)

SYSCTRL_PADCONF_CORE.[Register Name]	Address Offset	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
CONTROL_CORE_PAD0_CSI21_DX3_PAD1_CSI21_DY3[15:0]	0x0AC	csi21_dx3	cam2_d7		gpi_73				safe_mode
CONTROL_CORE_PAD0_CSI21_DX3_PAD1_CSI21_DY3[31:16]	0x0AC	csi21_dy3	cam2_d6		gpi_74				safe_mode
CONTROL_CORE_PAD0_CSI21_DX4_PAD1_CSI21_DY4[15:0]	0x0B0	csi21_dx4	cam2_d5		gpi_75				safe_mode
CONTROL_CORE_PAD0_CSI21_DX4_PAD1_CSI21_DY4[31:16]	0x0B0	csi21_dy4	cam2_d4		gpi_76				safe_mode
CONTROL_CORE_PAD0_CSI22_DX0_PAD1_CSI22_DY0[15:0]	0x0B4	csi22_dx0	cam2_d3	cam2_d12	gpi_77				safe_mode
CONTROL_CORE_PAD0_CSI22_DX0_PAD1_CSI22_DY0[31:16]	0x0B4	csi22_dy0	cam2_d2	cam2_d13	gpi_78				safe_mode
CONTROL_CORE_PAD0_CSI22_DX1_PAD1_CSI22_DY1[15:0]	0x0B8	csi22_dx1	cam2_d1	cam2_d14	gpi_79				safe_mode
CONTROL_CORE_PAD0_CSI22_DX1_PAD1_CSI22_DY1[31:16]	0x0B8	csi22_dy1	cam2_d0	cam2_d15	gpi_80				safe_mode
CONTROL_CORE_PAD0_CAM_SHUTTER_PAD1_CAM_STROBE[15:0]	0x0BC	cam_ shutter		cam2_hs	gpio_81				safe_mode
CONTROL_CORE_PAD0_CAM_SHUTTER_PAD1_CAM_STROBE[31:16]	0x0BC	cam_ strobe		cam2_vs	gpio_82				safe_mode
CONTROL_CORE_PAD0_CAM_GLOBALRESET_PAD1_USBB1_ULPITLL_CLK[15:0]	0x0C0	cam_ globalreset		cam2_pclk	gpio_83				safe_mode
CONTROL_CORE_PAD0_CAM_GLOBALRESET_PAD1_USBB1_ULPITLL_CLK[31:16]	0x0C0	usbb1_ ulpitll_clk	hsi1_cawake		gpio_84	usbb1_ ulpiphy_clk		hw_dbg20	safe_mode
CONTROL_CORE_PAD0_USBB1_ULPITLL_STP_PAD1_USBB1_ULPITLL_DIR[15:0]	0x0C4	usbb1_ ulpitll_stp	hsi1_cadata	mcbsp4_clkr	gpio_85	usbb1_ ulpiphy_stp	usbb1_ mm_rxdp	hw_dbg21	safe_mode
CONTROL_CORE_PAD0_USBB1_ULPITLL_STP_PAD1_USBB1_ULPITLL_DIR[31:16]	0x0C4	usbb1_ ulpitll_dir	hsi1_caflag	mcbsp4_fsr	gpio_86	usbb1_ ulpiphy_dir		hw_dbg22	safe_mode

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Table 18-10. Device Core Control Module Pad Configuration Register Fields (continued)

SYSCTRL_PADCONF_CORE.[Register Name]	Address Offset	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
CONTROL_CORE_PAD0_USBB1_ULPITLL_NXT_PAD1_USBB1_ULPITLL_DAT0[15:0]	0x0C8	usbb1_ulpitll_nxt	hsi1_acready	mcbsp4_fsx	gpio_87	usbb1_ulpiphy_nxt	usbb1_mm_rxdm	hw_dbg23	safe_mode
CONTROL_CORE_PAD0_USBB1_ULPITLL_NXT_PAD1_USBB1_ULPITLL_DAT0[31:16]	0x0C8	usbb1_ulpitll_dat0	hsi1_acwake	mcbsp4_clkx	gpio_88	usbb1_ulpiphy_dat0	usbb1_mm_txen	hw_dbg24	safe_mode
CONTROL_CORE_PAD0_USBB1_ULPITLL_DAT1_PAD1_USBB1_ULPITLL_DAT2[15:0]	0x0CC	usbb1_ulpitll_dat1	hsi1_acdata	mcbsp4_dx	gpio_89	usbb1_ulpiphy_dat1	usbb1_mm_txdat	hw_dbg25	safe_mode
CONTROL_CORE_PAD0_USBB1_ULPITLL_DAT1_PAD1_USBB1_ULPITLL_DAT2[31:16]	0x0CC	usbb1_ulpitll_dat2	hsi1_acflag	mcbsp4_dr	gpio_90	usbb1_ulpiphy_dat2	usbb1_mm_txse0	hw_dbg26	safe_mode
CONTROL_CORE_PAD0_USBB1_ULPITLL_DAT3_PAD1_USBB1_ULPITLL_DAT4[15:0]	0x0D0	usbb1_ulpitll_dat3	hsi1_caready		gpio_91	usbb1_ulpiphy_dat3	usbb1_mm_rxrcv	hw_dbg27	safe_mode
CONTROL_CORE_PAD0_USBB1_ULPITLL_DAT3_PAD1_USBB1_ULPITLL_DAT4[31:16]	0x0D0	usbb1_ulpitll_dat4	dmtimer8_pwm_evt	abe_mcbsp3_dr	gpio_92	usbb1_ulpiphy_dat4		hw_dbg28	safe_mode
CONTROL_CORE_PAD0_USBB1_ULPITLL_DAT5_PAD1_USBB1_ULPITLL_DAT6[15:0]	0x0D4	usbb1_ulpitll_dat5	dmtimer9_pwm_evt	abe_mcbsp3_dx	gpio_93	usbb1_ulpiphy_dat5		hw_dbg29	safe_mode
CONTROL_CORE_PAD0_USBB1_ULPITLL_DAT5_PAD1_USBB1_ULPITLL_DAT6[31:16]	0x0D4	usbb1_ulpitll_dat6	dmtimer10_pwm_evt	abe_mcbsp3_clkx	gpio_94	usbb1_ulpiphy_dat6	abe_dmic_din3	hw_dbg30	safe_mode
CONTROL_CORE_PAD0_USBB1_ULPITLL_DAT7_PAD1_USBB1_HSIC_DATA[15:0]	0x0D8	usbb1_ulpitll_dat7	dmtimer11_pwm_evt	abe_mcbsp3_fsx	gpio_95	usbb1_ulpiphy_dat7	abe_dmic_clk3	hw_dbg31	safe_mode
CONTROL_CORE_PAD0_USBB1_ULPITLL_DAT7_PAD1_USBB1_HSIC_DATA[31:16]	0x0D8	usbb1_hsic_data			gpio_96				safe_mode
CONTROL_CORE_PAD0_USBB1_HSIC_STROBE_PAD1_USBC1_ICUSB_DP[15:0]	0x0DC	usbb1_hsic_strobe			gpio_97				safe_mode

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Table 18-10. Device Core Control Module Pad Configuration Register Fields (continued)

SYSCTRL_PADCONF_CORE.[Register Name]	Address Offset	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
CONTROL_CORE_PAD0_USBB1_HSIC_STROBE_PAD1_USBC1_ICUSB_DP[31:16]	0x0DC	usbc1_ icusb_dp			gpio_98				safe_mode
CONTROL_CORE_PAD0_USBC1_ICUSB_DM_PAD1_SDMMC1_CLK[15:0]	0x0E0	usbc1_ icusb_dm			gpio_99				safe_mode
CONTROL_CORE_PAD0_USBC1_ICUSB_DM_PAD1_SDMMC1_CLK[31:16]	0x0E0	sdmmc1_ clk		dpm_emu19	gpio_100				safe_mode
CONTROL_CORE_PAD0_SDMMC1_CMD_PAD1_SDMMC1_DAT0[15:0]	0x0E4	sdmmc1_ cmd		uart1_rx	gpio_101				safe_mode
CONTROL_CORE_PAD0_SDMMC1_CMD_PAD1_SDMMC1_DAT0[31:16]	0x0E4	sdmmc1_ dat0		dpm_emu18	gpio_102				safe_mode
CONTROL_CORE_PAD0_SDMMC1_DAT1_PAD1_SDMMC1_DAT2[15:0]	0x0E8	sdmmc1_ dat1		dpm_emu17	gpio_103				safe_mode
CONTROL_CORE_PAD0_SDMMC1_DAT1_PAD1_SDMMC1_DAT2[31:16]	0x0E8	sdmmc1_ dat2		dpm_emu16	gpio_104	jtag_ tms_tmsc			safe_mode
CONTROL_CORE_PAD0_SDMMC1_DAT3_PAD1_SDMMC1_DAT4[15:0]	0x0EC	sdmmc1_ dat3		dpm_emu15	gpio_105	jtag_tck			safe_mode
CONTROL_CORE_PAD0_SDMMC1_DAT3_PAD1_SDMMC1_DAT4[31:16]	0x0EC	sdmmc1_ dat4			gpio_106				safe_mode
CONTROL_CORE_PAD0_SDMMC1_DAT5_PAD1_SDMMC1_DAT6[15:0]	0x0F0	sdmmc1_ dat5			gpio_107				safe_mode
CONTROL_CORE_PAD0_SDMMC1_DAT5_PAD1_SDMMC1_DAT6[31:16]	0x0F0	sdmmc1_ dat6			gpio_108				safe_mode
CONTROL_CORE_PAD0_SDMMC1_DAT7_PAD1_ABE_MCBSP2_CLKX[15:0]	0x0F4	sdmmc1_ dat7			gpio_109				safe_mode
CONTROL_CORE_PAD0_SDMMC1_DAT7_PAD1_ABE_MCBSP2_CLKX[31:16]	0x0F4	abe_ mcbsp2_clkx	mcspi2_clk	abe_ mcasp_ahclkx	gpio_110	usbb2_ mm_rxdm			safe_mode
CONTROL_CORE_PAD0_ABE_MCBSP2_DR_PAD1_ABE_MCBSP2_DX[15:0]	0x0F8	abe_ mcbsp2_dr	mcspi2_ somi	abe_ mcasp_axr	gpio_111	usbb2_ mm_rxdp			safe_mode

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Table 18-10. Device Core Control Module Pad Configuration Register Fields (continued)

SYSCTRL_PADCONF_CORE.[Register Name]	Address Offset	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
CONTROL_CORE_PAD0_ABE_MCBSP2_DR_PAD1_ABE_MCBSP2_DX[31:16]	0x0F8	abe_ mcbsp2_dx	mcspi2_ simo	abe_ mcasp_amute	gpio_112	usbb2_ mm_rxrcv			safe_mode
CONTROL_CORE_PAD0_ABE_MCBSP2_FSX_PAD1_ABE_MCBSP1_CLKX[15:0]	0x0FC	abe_ mcbsp2_fsx	mcspi2_ cs0	abe_ mcasp_afsx	gpio_113	usbb2_ mm_txen			safe_mode
CONTROL_CORE_PAD0_ABE_MCBSP2_FSX_PAD1_ABE_MCBSP1_CLKX[31:16]	0x0FC	abe_ mcbsp1_clkx	abe_ slimbus1_clock		gpio_114				safe_mode
CONTROL_CORE_PAD0_ABE_MCBSP1_DR_PAD1_ABE_MCBSP1_DX[15:0]	0x100	abe_ mcbsp1_dr	abe_ slimbus1_ data		gpio_115				safe_mode
CONTROL_CORE_PAD0_ABE_MCBSP1_DR_PAD1_ABE_MCBSP1_DX[31:16]	0x100	abe_ mcbsp1_dx	sdmmc3_ dat2	abe_ mcasp_aclkx	gpio_116				safe_mode
CONTROL_CORE_PAD0_ABE_MCBSP1_FSX_PAD1_ABE_PDM_UL_DATA[15:0]	0x104	abe_ mcbsp1_fsx	sdmmc3_ dat3	abe_ mcasp_amutein	gpio_117				safe_mode
CONTROL_CORE_PAD0_ABE_MCBSP1_FSX_PAD1_ABE_PDM_UL_DATA[31:16]	0x104	abe_ pdm_ul_data	abe_ mcbsp3_dr						safe_mode
CONTROL_CORE_PAD0_ABE_PDM_DL_DATA_PAD1_ABE_PDM_FRAME[15:0]	0x108	abe_ pdm_dl_data	abe_ mcbsp3_dx						safe_mode
CONTROL_CORE_PAD0_ABE_PDM_DL_DATA_PAD1_ABE_PDM_FRAME[31:16]	0x108	abe_ pdm_frame	abe_ mcbsp3_clkx						safe_mode
CONTROL_CORE_PAD0_ABE_PDM_LB_CLK_PAD1_ABE_CLKS[15:0]	0x10C	abe_ pdm_lb_clk	abe_ mcbsp3_fsx						safe_mode
CONTROL_CORE_PAD0_ABE_PDM_LB_CLK_PAD1_ABE_CLKS[31:16]	0x10C	abe_clks			gpio_118				safe_mode
CONTROL_CORE_PAD0_ABE_DMIC_CLK1_PAD1_ABE_DMIC_DIN1[15:0]	0x110	abe_ dmic_clk1			gpio_119	usbb2_ mm_txse0	uart4_cts		safe_mode
CONTROL_CORE_PAD0_ABE_DMIC_CLK1_PAD1_ABE_DMIC_DIN1[31:16]	0x110	abe_ dmic_din1			gpio_120	usbb2_ mm_txdat	uart4_rts		safe_mode
CONTROL_CORE_PAD0_ABE_DMIC_DIN2_PAD1_ABE_DMIC_DIN3[15:0]	0x114	abe_ dmic_din2	slimbus2_ clock	abe_ mcasp_axr	gpio_121		dmtimer11_ pwm_evt		safe_mode

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Table 18-10. Device Core Control Module Pad Configuration Register Fields (continued)

SYSCTRL_PADCONF_CORE.[Register Name]	Address Offset	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
CONTROL_CORE_PAD0_ABE_DMIC_DIN2_PAD1_ABE_DMIC_DIN3[31:16]	0x114	abe_ dmic_din3	slimbus2_ data	abe_ dmic_clk2	gpio_122		dmtimer9_ pwm_evt		safe_mode
CONTROL_CORE_PAD0_UART2_CTS_PAD1_UART2_RTS[15:0]	0x118	uart2_cts	sdmmc3_ clk		gpio_123				safe_mode
CONTROL_CORE_PAD0_UART2_CTS_PAD1_UART2_RTS[31:16]	0x118	uart2_rts	sdmmc3_ cmd		gpio_124				safe_mode
CONTROL_CORE_PAD0_UART2_RX_PAD1_UART2_TX[15:0]	0x11C	uart2_rx	sdmmc3_ dat0		gpio_125				safe_mode
CONTROL_CORE_PAD0_UART2_RX_PAD1_UART2_TX[31:16]	0x11C	uart2_tx	sdmmc3_ dat1		gpio_126				safe_mode
CONTROL_CORE_PAD0_HDQ_SIO_PAD1_I2C1_SCL[15:0]	0x120	hdq_sio	i2c3_sccb	i2c2_sccb	gpio_127				safe_mode
CONTROL_CORE_PAD0_HDQ_SIO_PAD1_I2C1_SCL[31:16]	0x120	i2c1_scl							
CONTROL_CORE_PAD0_I2C1_SDA_PAD1_I2C2_SCL[15:0]	0x124	i2c1_sda							
CONTROL_CORE_PAD0_I2C1_SDA_PAD1_I2C2_SCL[31:16]	0x124	i2c2_scl	uart1_rx		gpio_128				safe_mode
CONTROL_CORE_PAD0_I2C2_SDA_PAD1_I2C3_SCL[15:0]	0x128	i2c2_sda	uart1_tx		gpio_129				safe_mode
CONTROL_CORE_PAD0_I2C2_SDA_PAD1_I2C3_SCL[31:16]	0x128	i2c3_scl			gpio_130				safe_mode
CONTROL_CORE_PAD0_I2C3_SDA_PAD1_I2C4_SCL[15:0]	0x12C	i2c3_sda			gpio_131				safe_mode
CONTROL_CORE_PAD0_I2C3_SDA_PAD1_I2C4_SCL[31:16]	0x12C	i2c4_scl			gpio_132				safe_mode
CONTROL_CORE_PAD0_I2C4_SDA_PAD1_MCSPI1_CLK[15:0]	0x130	i2c4_sda			gpio_133				safe_mode

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Table 18-10. Device Core Control Module Pad Configuration Register Fields (continued)

SYSCTRL_PADCONF_CORE.[Register Name]	Address Offset	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
CONTROL_CORE_PAD0_I2C4_SDA_PAD1_MCSPI1_CLK[31:16]	0x130	mcspi1_clk			gpio_134				safe_mode
CONTROL_CORE_PAD0_MCSPI1_SOMI_PAD1_MCSPI1_SIMO[15:0]	0x134	mcspi1_somi			gpio_135				safe_mode
CONTROL_CORE_PAD0_MCSPI1_SOMI_PAD1_MCSPI1_SIMO[31:16]	0x134	mcspi1_simo			gpio_136				safe_mode
CONTROL_CORE_PAD0_MCSPI1_CS0_PAD1_MCSPI1_CS1[15:0]	0x138	mcspi1_cs0			gpio_137				safe_mode
CONTROL_CORE_PAD0_MCSPI1_CS0_PAD1_MCSPI1_CS1[31:16]	0x138	mcspi1_cs1	uart1_rx		gpio_138				safe_mode
CONTROL_CORE_PAD0_MCSPI1_CS2_PAD1_MCSPI1_CS3[15:0]	0x13C	mcspi1_cs2	uart1_cts	slimbus2_clock	gpio_139				safe_mode
CONTROL_CORE_PAD0_MCSPI1_CS2_PAD1_MCSPI1_CS3[31:16]	0x13C	mcspi1_cs3	uart1_rts	slimbus2_data	gpio_140				safe_mode
CONTROL_CORE_PAD0_UART3_CTS_RCTX_PAD1_UART3_RTS_SD[15:0]	0x140	uart3_cts_rctx	uart1_tx		gpio_141				safe_mode
CONTROL_CORE_PAD0_UART3_CTS_RCTX_PAD1_UART3_RTS_SD[31:16]	0x140	uart3_rts_sd		cam_globalreset	gpio_142				safe_mode
CONTROL_CORE_PAD0_UART3_RX_IRRX_PAD1_UART3_TX_IRTX[15:0]	0x144	uart3_rx_irrx	dmtimer8_pwm_evt	cam_shutter	gpio_143				safe_mode
CONTROL_CORE_PAD0_UART3_RX_IRRX_PAD1_UART3_TX_IRTX[31:16]	0x144	uart3_tx_irtx	dmtimer9_pwm_evt	cam_strobe	gpio_144				safe_mode
CONTROL_CORE_PAD0_SDMMC5_CLK_PAD1_SDMMC5_CMD[15:0]	0x148	sdmmc5_clk	mcspi2_clk	usbc1_icusb_dp	gpio_145		sdmmc2_clk		safe_mode
CONTROL_CORE_PAD0_SDMMC5_CLK_PAD1_SDMMC5_CMD[31:16]	0x148	sdmmc5_cmd	mcspi2_simo	usbc1_icusb_dm	gpio_146		sdmmc2_cmd		safe_mode
CONTROL_CORE_PAD0_SDMMC5_DAT0_PAD1_SDMMC5_DAT1[15:0]	0x14C	sdmmc5_dat0	mcspi2_somi	usbc1_icusb_rcv	gpio_147		sdmmc2_dat0		safe_mode

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Table 18-10. Device Core Control Module Pad Configuration Register Fields (continued)

SYSCTRL_PADCONF_CORE.[Register Name]	Address Offset	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
CONTROL_CORE_PAD0_SDMMC5_DAT0_PAD1_SDMMC5_DAT1[31:16]	0x14C	sdmmc5_dat1		usbc1_icusb_txen	gpio_148		sdmmc2_dat1		safe_mode
CONTROL_CORE_PAD0_SDMMC5_DAT2_PAD1_SDMMC5_DAT3[15:0]	0x150	sdmmc5_dat2	mcspi2_cs1		gpio_149		sdmmc2_dat2		safe_mode
CONTROL_CORE_PAD0_SDMMC5_DAT2_PAD1_SDMMC5_DAT3[31:16]	0x150	sdmmc5_dat3	mcspi2_cs0		gpio_150		sdmmc2_dat3		safe_mode
CONTROL_CORE_PAD0_MCSPI4_CLK_PAD1_MCSPI4_SIMO[15:0]	0x154	mcspi4_clk	sdmmc4_clk	kpd_col6	gpio_151				safe_mode
CONTROL_CORE_PAD0_MCSPI4_CLK_PAD1_MCSPI4_SIMO[31:16]	0x154	mcspi4_simo	sdmmc4_cmd	kpd_col7	gpio_152				safe_mode
CONTROL_CORE_PAD0_MCSPI4_SOMI_PAD1_MCSPI4_CS0[15:0]	0x158	mcspi4_somi	sdmmc4_dat0	kpd_row6	gpio_153				safe_mode
CONTROL_CORE_PAD0_MCSPI4_SOMI_PAD1_MCSPI4_CS0[31:16]	0x158	mcspi4_cs0	sdmmc4_dat3	kpd_row7	gpio_154				safe_mode
CONTROL_CORE_PAD0_UART4_RX_PAD1_UART4_TX[15:0]	0x15C	uart4_rx	sdmmc4_dat2	kpd_row8	gpio_155				safe_mode
CONTROL_CORE_PAD0_UART4_RX_PAD1_UART4_TX[31:16]	0x15C	uart4_tx	sdmmc4_dat1	kpd_col8	gpio_156				safe_mode
CONTROL_CORE_PAD0_USBB2_ULPITLL_CLK_PAD1_USBB2_ULPITLL_STP[15:0]	0x160	usbb2_ulpitll_clk	usbb2_ulpiphy_clk	sdmmc4_cmd	gpio_157	hsi2_cawake			safe_mode
CONTROL_CORE_PAD0_USBB2_ULPITLL_CLK_PAD1_USBB2_ULPITLL_STP[31:16]	0x160	usbb2_ulpitll_stp	usbb2_ulpiphy_stp	sdmmc4_clk	gpio_158	hsi2_cadata	dispc2_data23		safe_mode
CONTROL_CORE_PAD0_USBB2_ULPITLL_DIR_PAD1_USBB2_ULPITLL_NXT[15:0]	0x164	usbb2_ulpitll_dir	usbb2_ulpiphy_dir	sdmmc4_dat0	gpio_159	hsi2_caflag	dispc2_data22		safe_mode
CONTROL_CORE_PAD0_USBB2_ULPITLL_DIR_PAD1_USBB2_ULPITLL_NXT[31:16]	0x164	usbb2_ulpitll_nxt	usbb2_ulpiphy_nxt	sdmmc4_dat1	gpio_160	hsi2_acready	dispc2_data21		safe_mode

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Table 18-10. Device Core Control Module Pad Configuration Register Fields (continued)

SYSCTRL_PADCONF_CORE.[Register Name]	Address Offset	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
CONTROL_CORE_PAD0_USBB2_ULPITLL_DAT0_PAD1_USBB2_ULPITLL_DAT1[15:0]	0x168	usbb2_ulpitll_dat0	usbb2_ulpiphy_dat0	sdmmc4_dat2	gpio_161	hsi2_acwake	dispc2_data20	usbb2_mm_txen	safe_mode
CONTROL_CORE_PAD0_USBB2_ULPITLL_DAT0_PAD1_USBB2_ULPITLL_DAT1[31:16]	0x168	usbb2_ulpitll_dat1	usbb2_ulpiphy_dat1	sdmmc4_dat3	gpio_162	hsi2_acdata	dispc2_data19	usbb2_mm_txdat	safe_mode
CONTROL_CORE_PAD0_USBB2_ULPITLL_DAT2_PAD1_USBB2_ULPITLL_DAT3[15:0]	0x16C	usbb2_ulpitll_dat2	usbb2_ulpiphy_dat2	sdmmc3_dat2	gpio_163	hsi2_acflag	dispc2_data18	usbb2_mm_txse0	safe_mode
CONTROL_CORE_PAD0_USBB2_ULPITLL_DAT2_PAD1_USBB2_ULPITLL_DAT3[31:16]	0x16C	usbb2_ulpitll_dat3	usbb2_ulpiphy_dat3	sdmmc3_dat1	gpio_164	hsi2_caready	dispc2_data15	rfbi_data15	safe_mode
CONTROL_CORE_PAD0_USBB2_ULPITLL_DAT4_PAD1_USBB2_ULPITLL_DAT5[15:0]	0x170	usbb2_ulpitll_dat4	usbb2_ulpiphy_dat4	sdmmc3_dat0	gpio_165	mcspi3_somi	dispc2_data14	rfbi_data14	safe_mode
CONTROL_CORE_PAD0_USBB2_ULPITLL_DAT4_PAD1_USBB2_ULPITLL_DAT5[31:16]	0x170	usbb2_ulpitll_dat5	usbb2_ulpiphy_dat5	sdmmc3_dat3	gpio_166	mcspi3_cs0	dispc2_data13	rfbi_data13	safe_mode
CONTROL_CORE_PAD0_USBB2_ULPITLL_DAT6_PAD1_USBB2_ULPITLL_DAT7[15:0]	0x174	usbb2_ulpitll_dat6	usbb2_ulpiphy_dat6	sdmmc3_cmd	gpio_167	mcspi3_simo	dispc2_data12	rfbi_data12	safe_mode
CONTROL_CORE_PAD0_USBB2_ULPITLL_DAT6_PAD1_USBB2_ULPITLL_DAT7[31:16]	0x174	usbb2_ulpitll_dat7	usbb2_ulpiphy_dat7	sdmmc3_clk	gpio_168	mcspi3_clk	dispc2_data11	rfbi_data11	safe_mode
CONTROL_CORE_PAD0_USBB2_HSIC_DATA_PAD1_USBB2_HSIC_STROBE[15:0]	0x178	usbb2_hsic_data			gpio_169				safe_mode
CONTROL_CORE_PAD0_USBB2_HSIC_DATA_PAD1_USBB2_HSIC_STROBE[31:16]	0x178	usbb2_hsic_strobe			gpio_170				safe_mode
CONTROL_CORE_PAD0_KPD_COL3_PAD1_KPD_COL4[15:0]	0x17C	kpd_col3	kpd_col0	cam2_d0	gpio_171				safe_mode

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Table 18-10. Device Core Control Module Pad Configuration Register Fields (continued)

SYSCTRL_PADCONF_CORE.[Register Name]	Address Offset	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
CONTROL_CORE_PAD0_KPD_COL3_PAD1_KPD_COL4[31:16]	0x17C	kpd_col4	kpd_col1	cam2_d1	gpio_172				safe_mode
CONTROL_CORE_PAD0_KPD_COL5_PAD1_KPD_COL0[15:0]	0x180	kpd_col5	kpd_col2	cam2_d2	gpio_173				safe_mode
CONTROL_CORE_PAD0_KPD_COL5_PAD1_KPD_COL0[31:16]	0x180	kpd_col0	kpd_col3	cam2_d3	gpio_174				safe_mode
CONTROL_CORE_PAD0_KPD_COL1_PAD1_KPD_COL2[15:0]	0x184	kpd_col1	kpd_col4	cam2_d8	gpio_0				safe_mode
CONTROL_CORE_PAD0_KPD_COL1_PAD1_KPD_COL2[31:16]	0x184	kpd_col2	kpd_col5	cam2_d10	gpio_1				safe_mode
CONTROL_CORE_PAD0_KPD_ROW3_PAD1_KPD_ROW4[15:0]	0x188	kpd_row3	kpd_row0	cam2_d4	gpio_175				safe_mode
CONTROL_CORE_PAD0_KPD_ROW3_PAD1_KPD_ROW4[31:16]	0x188	kpd_row4	kpd_row1	cam2_d5	gpio_176				safe_mode
CONTROL_CORE_PAD0_KPD_ROW5_PAD1_KPD_ROW0[15:0]	0x18C	kpd_row5	kpd_row2	cam2_d6	gpio_177				safe_mode
CONTROL_CORE_PAD0_KPD_ROW5_PAD1_KPD_ROW0[31:16]	0x18C	kpd_row0	kpd_row3	cam2_d7	gpio_178				safe_mode
CONTROL_CORE_PAD0_KPD_ROW1_PAD1_KPD_ROW2[15:0]	0x190	kpd_row1	kpd_row4	cam2_d9	gpio_2				safe_mode
CONTROL_CORE_PAD0_KPD_ROW1_PAD1_KPD_ROW2[31:16]	0x190	kpd_row2	kpd_row5	cam2_d11	gpio_3				safe_mode
CONTROL_CORE_PAD0_USBA0_OTG_CE_PAD1_USBA0_OTG_DP[15:0]	0x194	usba0_otg_ce							
CONTROL_CORE_PAD0_USBA0_OTG_CE_PAD1_USBA0_OTG_DP[31:16]	0x194	usba0_otg_dp	uart3_rx_irrx	uart2_rx					safe_mode
CONTROL_CORE_PAD0_USBA0_OTG_DM_PAD1_FREF_CLK1_OUT[15:0]	0x198	usba0_otg_dm	uart3_tx_irtx	uart2_tx					safe_mode

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Table 18-10. Device Core Control Module Pad Configuration Register Fields (continued)

SYSCTRL_PADCONF_CORE.[Register Name]	Address Offset	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
CONTROL_CORE_PAD0_USBA0_OTG_DM_PAD1_FREF_CLK1_OUT[31:16]	0x198	fref_clk1_out			gpio_181				safe_mode
CONTROL_CORE_PAD0_FREF_CLK2_OUT_PAD1_SYS_NIRQ1[15:0]	0x19C	fref_clk2_out			gpio_182				safe_mode
CONTROL_CORE_PAD0_FREF_CLK2_OUT_PAD1_SYS_NIRQ1[31:16]	0x19C	sys_nirq1							safe_mode
CONTROL_CORE_PAD0_SYS_NIRQ2_PAD1_SYS_BOOT0[15:0]	0x1A0	sys_nirq2			gpio_183				safe_mode
CONTROL_CORE_PAD0_SYS_NIRQ2_PAD1_SYS_BOOT0[31:16]	0x1A0	sys_boot0			gpio_184				safe_mode
CONTROL_CORE_PAD0_SYS_BOOT1_PAD1_SYS_BOOT2[15:0]	0x1A4	sys_boot1			gpio_185				safe_mode
CONTROL_CORE_PAD0_SYS_BOOT1_PAD1_SYS_BOOT2[31:16]	0x1A4	sys_boot2			gpio_186				safe_mode
CONTROL_CORE_PAD0_SYS_BOOT3_PAD1_SYS_BOOT4[15:0]	0x1A8	sys_boot3			gpio_187				safe_mode
CONTROL_CORE_PAD0_SYS_BOOT3_PAD1_SYS_BOOT4[31:16]	0x1A8	sys_boot4			gpio_188				safe_mode
CONTROL_CORE_PAD0_SYS_BOOT5_PAD1_DPM_EMU0[15:0]	0x1AC	sys_boot5			gpio_189				safe_mode
CONTROL_CORE_PAD0_SYS_BOOT5_PAD1_DPM_EMU0[31:16]	0x1AC	dpm_emu0			gpio_11			hw_dbg0	safe_mode
CONTROL_CORE_PAD0_DPM_EMU1_PAD1_DPM_EMU2[15:0]	0x1B0	dpm_emu1			gpio_12			hw_dbg1	safe_mode
CONTROL_CORE_PAD0_DPM_EMU1_PAD1_DPM_EMU2[31:16]	0x1B0	dpm_emu2	usba0_ulpiphy_clk		gpio_13		dispc2_fid	hw_dbg2	safe_mode
CONTROL_CORE_PAD0_DPM_EMU3_PAD1_DPM_EMU4[15:0]	0x1B4	dpm_emu3	usba0_ulpiphy_stp		gpio_14	rfbi_data10	dispc2_data10	hw_dbg3	safe_mode

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Table 18-10. Device Core Control Module Pad Configuration Register Fields (continued)

SYSCTRL_PADCONF_CORE.[Register Name]	Address Offset	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
CONTROL_CORE_PAD0_DPM_EMU3_PAD1_DPM_EMU4[31:16]	0x1B4	dpm_emu4	usba0_ulpiphy_dir		gpio_15	rfbi_data9	dispc2_data9	hw_dbg4	safe_mode
CONTROL_CORE_PAD0_DPM_EMU5_PAD1_DPM_EMU6[15:0]	0x1B8	dpm_emu5	usba0_ulpiphy_nxt		gpio_16	rfbi_te_vsync0	dispc2_data16	hw_dbg5	safe_mode
CONTROL_CORE_PAD0_DPM_EMU5_PAD1_DPM_EMU6[31:16]	0x1B8	dpm_emu6	usba0_ulpiphy_dat0	uart3_tx_irtx	gpio_17	rfbi_hsync0	dispc2_data17	hw_dbg6	safe_mode
CONTROL_CORE_PAD0_DPM_EMU7_PAD1_DPM_EMU8[15:0]	0x1BC	dpm_emu7	usba0_ulpiphy_dat1	uart3_rx_irrx	gpio_18	rfbi_cs0	dispc2_hsync	hw_dbg7	safe_mode
CONTROL_CORE_PAD0_DPM_EMU7_PAD1_DPM_EMU8[31:16]	0x1BC	dpm_emu8	usba0_ulpiphy_dat2	uart3_rts_sd	gpio_19	rfbi_re	dispc2_pclk	hw_dbg8	safe_mode
CONTROL_CORE_PAD0_DPM_EMU9_PAD1_DPM_EMU10[15:0]	0x1C0	dpm_emu9	usba0_ulpiphy_dat3	uart3_cts_rctx	gpio_20	rfbi_we	dispc2_vsync	hw_dbg9	safe_mode
CONTROL_CORE_PAD0_DPM_EMU9_PAD1_DPM_EMU10[31:16]	0x1C0	dpm_emu10	usba0_ulpiphy_dat4		gpio_21	rfbi_a0	dispc2_de	hw_dbg10	safe_mode
CONTROL_CORE_PAD0_DPM_EMU11_PAD1_DPM_EMU12[15:0]	0x1C4	dpm_emu11	usba0_ulpiphy_dat5		gpio_22	rfbi_data8	dispc2_data8	hw_dbg11	safe_mode
CONTROL_CORE_PAD0_DPM_EMU11_PAD1_DPM_EMU12[31:16]	0x1C4	dpm_emu12	usba0_ulpiphy_dat6		gpio_23	rfbi_data7	dispc2_data7	hw_dbg12	safe_mode
CONTROL_CORE_PAD0_DPM_EMU13_PAD1_DPM_EMU14[15:0]	0x1C8	dpm_emu13	usba0_ulpiphy_dat7		gpio_24	rfbi_data6	dispc2_data6	hw_dbg13	safe_mode
CONTROL_CORE_PAD0_DPM_EMU13_PAD1_DPM_EMU14[31:16]	0x1C8	dpm_emu14	Reserved	uart1_rx	gpio_25	rfbi_data5	dispc2_data5	hw_dbg14	safe_mode
CONTROL_CORE_PAD0_DPM_EMU15_PAD1_DPM_EMU16[15:0]	0x1CC	dpm_emu15	Reserved		gpio_26	rfbi_data4	dispc2_data4	hw_dbg15	safe_mode
CONTROL_CORE_PAD0_DPM_EMU15_PAD1_DPM_EMU16[31:16]	0x1CC	dpm_emu16	dmtimer8_pwm_evt	dsi1_te0	gpio_27	rfbi_data3	dispc2_data3	hw_dbg16	safe_mode
CONTROL_CORE_PAD0_DPM_EMU17_PAD1_DPM_EMU18[15:0]	0x1D0	dpm_emu17	dmtimer9_pwm_evt	dsi1_te1	gpio_28	rfbi_data2	dispc2_data2	hw_dbg17	safe_mode

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Table 18-10. Device Core Control Module Pad Configuration Register Fields (continued)

SYSCTRL_PADCONF_CORE.[Register Name]	Address Offset	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
CONTROL_CORE_PAD0_DPM_EMU17_PAD1_DPM_EMU18[31:16]	0x1D0	dpm_emu18	dmtimer10_pwm_evt	dsi2_te0	gpio_190	rfbi_data1	dispc2_data1	hw_dbg18	safe_mode
CONTROL_CORE_PAD0_DPM_EMU19_PAD1_CSI22_DX2[15:0]	0x1D4	dpm_emu19	dmtimer11_pwm_evt	dsi2_te1	gpio_191	rfbi_data0	dispc2_data0	hw_dbg19	safe_mode
CONTROL_CORE_PAD0_DPM_EMU19_PAD1_CSI22_DX2[31:16]	0x1D4	csi22_dx2		cam2_fid					safe_mode
CONTROL_CORE_PAD0_CSI22_DY2[15:0]	0x1F4	csi22_dy2		cam2_wen					safe_mode

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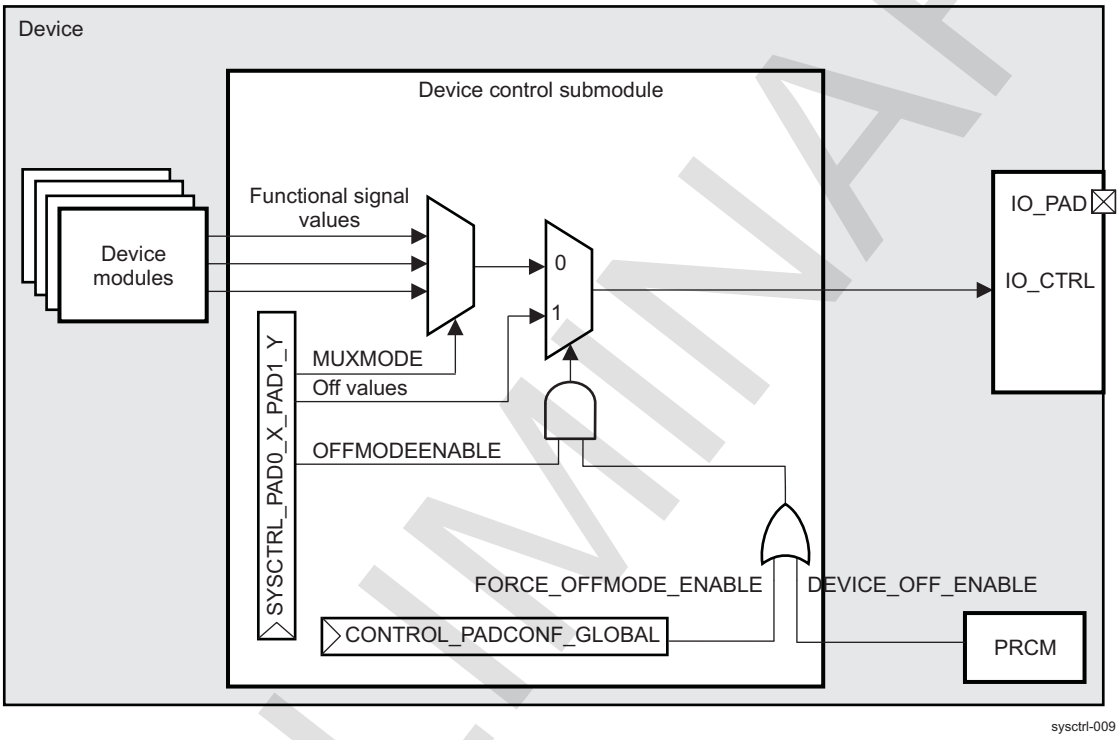
18.4.8.4 Off Mode Pad Control Overview

When off mode is selected, which is true when PRM_DEVICE_OFF_CTRL[0] DEVICE_OFF_ENABLE from the PRCM module = 0b1 or CONTROL_PADCONF_GLOBAL[31] FORCE_OFFMODE_ENABLE = 0b1 (force bit to test the value of off mode), the off mode values field CONTROL_CORE_PAD0_X_PAD1_Y[27,11] OFFMODEOUTVALUE overrides the pad state when the CONTROL_CORE_PAD0_X_PAD1_Y[25,9] OFFMODEENABLE bit is set.

The CONTROL_CORE_PAD0_X_PAD1_Y[26,10] OFFMODEOUTENABLE bit is active low.

Figure 18-9 shows the off mode pad control.

Figure 18-9. Off Mode Pad Control Overview



If off mode is active and the OFFMODEENABLE bit field is set to 0 (disable the off mode override feature), the pad keeps the AND value of the configuration (input/output, pullup/down) it had before going into off mode:

- For an input, the pad is isolated and the pull remains active.
- For an output, the value is latched before going into off mode, to drive the same value in off mode.

NOTE: Software controls for internal off-mode pullups and pulldowns on the usbb1_hsic_x and usbb2_hsic_x pads are available in the CONTROL_USBB_HSIC register.

No internal off-mode pullups and pulldowns are available for the lpddr21_x and lpddr22_x pads of the device.

For more information, see Section 18.4.12.9.2, *High-Speed I/O Buffers With Impedance, Slew Rate, and Weak Driver Settings*.

18.4.8.4.1 Wake-Up Event Detection

In off mode, wake-up event detection can also be enabled on an input pad. The pad wake-up event is latched in the CONTROL_CORE_PAD0_X_PAD1_Y[31,15] and CONTROL_WKUP_PAD0_X_PAD1_Y[31,15] WAKEUPEVENT bits.

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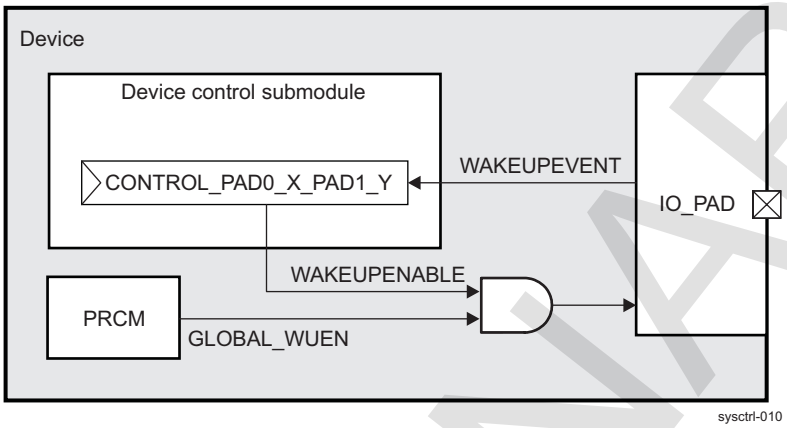
The off mode I/O pads wake-up scheme is enabled by setting the PRM_IO_PMCTRL[16] GLOBAL_WUEN bit from the PRCM module. The wake-up scheme status is transmitted by the WKUP_ENABLE signal. The wake-up event detection capability of each I/O pad of the device is individually enabled or disabled by writing the CONTROL_CORE_PAD0_X_PAD1_Y[30,14] and CONTROL_WKUP_PAD0_X_PAD1_Y[30,14] WAKEUPENABLE bits.

Figure 18-10. Wake-Up Event Detection Overview



NOTE: When wake-up detection is enabled for a pad, the pad must be configured as input to avoid contention between the device output buffer and an external driver. If this pin is already configured as an input in active mode, hardware automatically retains the same input state; no software action is required.

If this pin is configured as an output in active mode, the off override function must be enabled to set the pin as an input during off mode: in the CONTROL_(CORE/WKUP)_PAD0_X_PAD1_Y register, set the OFFMODEENABLE bit to 0x1 to enable the off override function and set the OFFMODEOUTENABLE bit to 0x1 to switch this pin to input mode.

NOTE: Regardless of whether the INPUTENABLE bit is set high or low during active mode, to enable wake-up detection for a pad, user software must set the WAKEUPENABLE bit to 0x1. It is recommended to apply pullup/down resistors at the pad to avoid spurious wake-up detection. User software can optionally enable the pad off-mode internal pullup/down resistors through the appropriate setting of the OFFMODEPULLUDENABLE and OFFMODEPULLTYPESELECT bits in the corresponding pad configuration register.

The CONTROL_PADCONF_WAKEUPEVENT_0 through CONTROL_PADCONF_WAKEUPEVENT_6 registers are dedicated 32-bit registers for a separate capture of the WAKEUPEVENT from different pads. Duplication of the CONTROL_CORE_PAD0_X_PAD1_Y[31,15] and CONTROL_WKUP_PAD0_X_PAD1_Y[31,15] wake-up event bits inside these seven additional registers helps reduce the software latency in identifying which pad has triggered a wake-up event.

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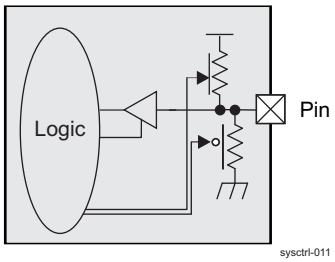
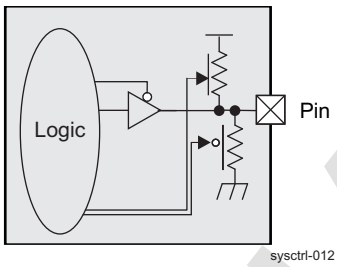
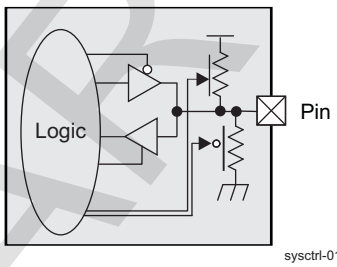
18.4.8.4.2 I/O Power Optimization

To optimize I/O power, it is important to avoid unconnected or incorrectly pulled pins. According to the type of pins, the way to reduce power consumption can differ. Table 18-11 shows the three available pin (or ball) types.

Table 18-11. Pin Types

Input	Output	Bidirectional
		

The configuration differs according to the I/O cell types. The following advice can be useful to avoid extra current leakage:

- For input pins, use a pullup/down when possible.
- For output pins, check existing pulls to avoid conflicts.
- For bidirectional pins, reconfigure the pin as an output driving 0 when possible.

NOTE: If the pad is always configured in output mode, it is recommended for software to disable the internal pull by programming the I/O pad configuration register of the corresponding control module.

NOTE: If a device pad is left unconnected, but power is supplied to the I/O, or the pad is used only as an output during the lifetime of the application, it is recommended to keep its corresponding pad configuration bit CONTROL_CORE /WKUP_PAD0_X_PAD1_Y.INPUTENABLE set to 0b0. This keeps the input buffer disabled and reduces static current consumption.

Some I/O configurations involve modifications during the software setup of I/Os and sometimes require several hardware updates.

Figure 18-11 shows how to optimize the power consumption of pads.

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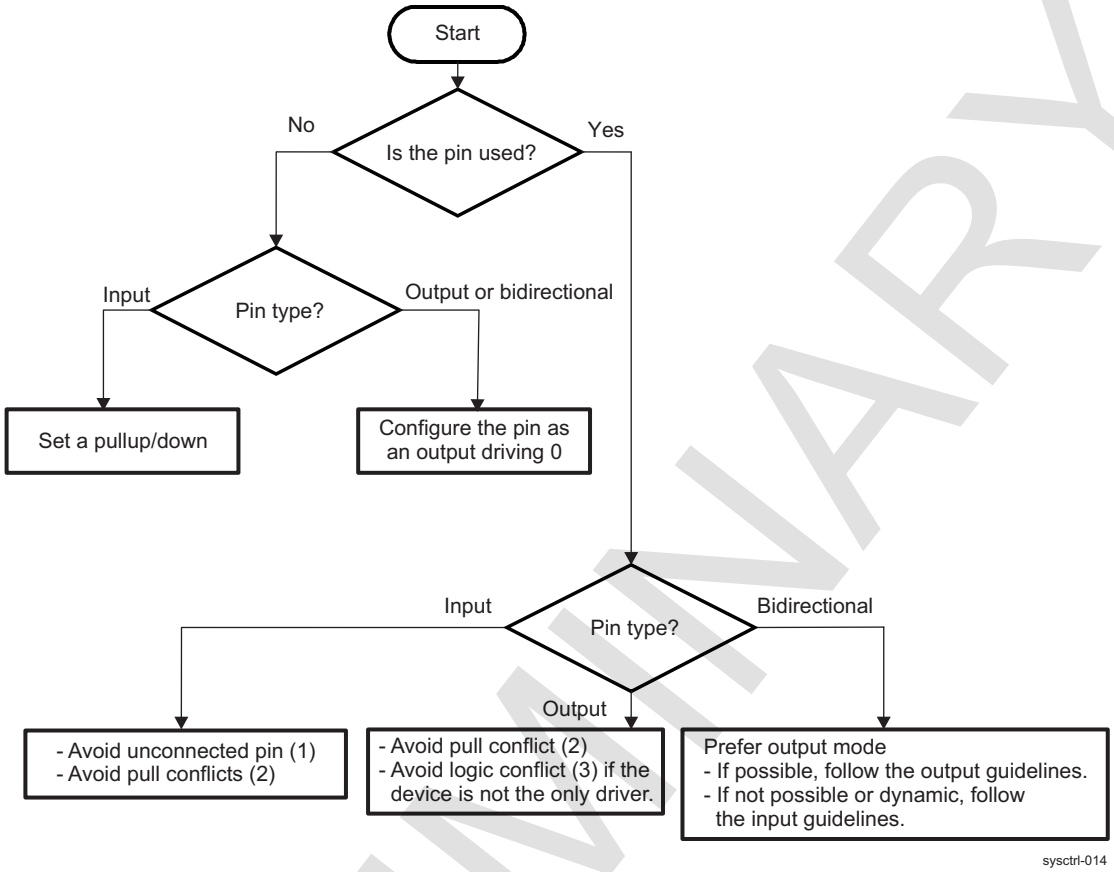
Figure 18-11. I/O Power Optimization Flow Chart



The following notes explain more about the pin configuration.

- To avoid unconnected pins, the configuration depends on its use:
  - If the pin is not driven externally, a pullup/down is required.
  - Otherwise, a pullup/down is not necessary.
- Pull conflicts occur when different pulls are on the same line. To configure the pin correctly, avoid having external and internal pulls together.
- Logic conflicts consist in different electrical levels at the same time on the same line. This can occur when several devices are connected to the same line. The two possible cases are:
  - If no external device drives the line, configure the pin to drive 0.
  - If another device drives the line, the same value must be driven or the pin must be disconnected (high-impedance state [HiZ]).

NOTE: It is advised to use HiZ logical state on the device or on the external component when the line is driven by both components.

18.4.9 Extended-Drain I/O and PBIAS Cell

The device primarily supports 1.8-V I/O voltage on its interfaces, with the exception of the MMC/SD/SDIO1 interface, which supports 1.8-V and 3.0-V voltages. The need for embedded extended-drain I/Os on the MMC/SD/SDIO1 interface imposes the use of embedded PBIAS cell MMC1_PBIAS to provide a 1.8-V or 3.0-V reference.

A second PBIAS cell (PBIAS1) is integrated in the device. One of its associated extended-drain I/O cells operates the signals of the gpio_wk0 through gpio_wk2 I/Os.

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A separate extended-drain I/O cell (USBC1_ICUSB extended-drain I/O cell) is shared between usbc1_icusb_dp and usbc1_icusb_dm (MUXMODE = 0x0), and between the gpio98 and gpio99 (MUXMODE = 0x3) pads. The USBC1_ICUSB I/O cell and the gpiowk_0–gpiowk_2 extended-drain I/O cells are biased by the same PBIAS1 output voltage.

NOTE: With the appropriate PBIAS cell configuration, the different I/Os muxed on the sdmmc1, usbc1_icusb, and gpio_wk0 through gpio_wk2 pads can operate at 1.8-V or 3.0-V power supply.

The MMC1_PBIAS cell and its associated MMC1 extended-drain I/O is software-controlled by bits in the CONTROL_PBIASLITE and CONTROL_MMC1 registers of the device core control module. PBIAS1 and associated GPIO_WKx and USBC1_ICUSB_x I/Os are software-controlled by bits in the CONTROL_PBIASLITE, CONTROL_MMC1, and CONTROL_GPIOWK registers.

Figure 18-12 shows the functional block diagram with the connections between the PBIAS cells and the extended-drain I/O cells.

Figure 18-12. Functional Block Diagram

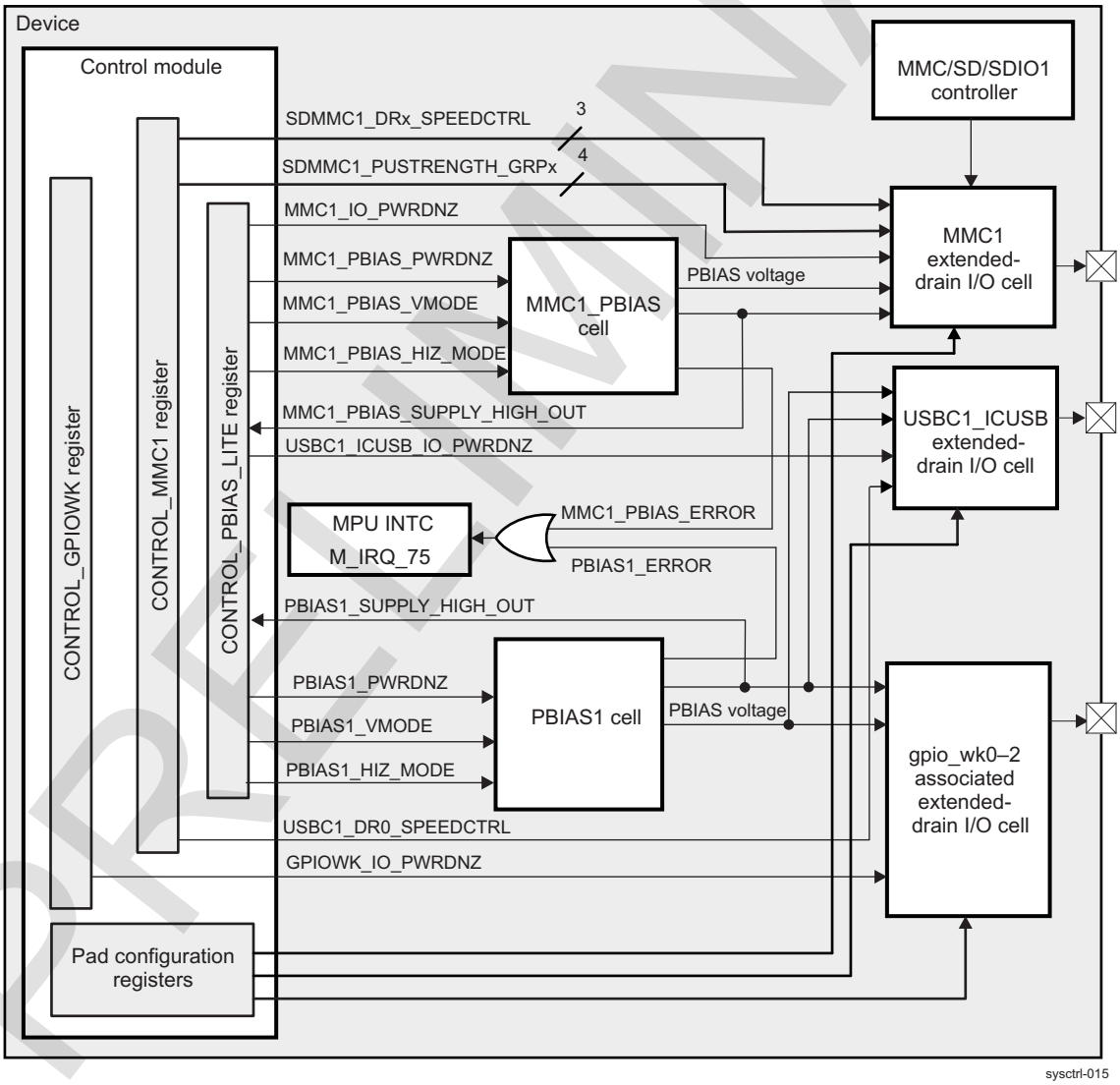

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Table 18-12. PBIAS Cell and Extended-Drain I/O Pin CONTROL_PBIAS_LITE Bit Control

Control Signals for Different PBIAS and Extended-Drain I/O Cells	Description
MMC1_PBIAS_PWRDNZ	Protects the MMC1_PBIAS cell when the SDMMC1_VDDS supply voltage is not stable. Software must keep this signal to 0b0 whenever this voltage ramps up/down or changes. When this bit is set to 0, the PBIAS output voltage is equal to SDMMC1_VDDS voltage and the PBIAS supply detector is disabled.
MMC1_PBIAS_VMODE	Sets the SDMMC1_VDDS voltage level (MMC1_PBIAS side) according to which MMC1_PBIAS cell generates appropriate biasing levels for the MMC1 extended-drain I/O. The default state of this bit is HIGH, indicating that the voltage level SDMMC1_VDDS is 3.0 V.
MMC1_PBIAS_HIZ_MODE	When MMC1_PBIAS_HIZ_MODE is set to 1, the PBIAS output is in high impedance. MMC1_PBIAS_ERROR is automatically set to 1 when MMC1_PBIAS_HIZ_MODE = 1. When MMC1_PBIAS_HIZ_MODE = 0, MMC1_PBIAS cell is in normal operation mode.
MMC1_PBIAS_SUPPLY_HIGH_OUT	Output from the internal MMC1_PBIAS voltage supply detector, which indicates whether the SDMMC1_VDDS supply is 3.0 V or 1.8 V
MMC1_PBIAS_ERROR	Indicates whether the software-programmed MMC1_PBIAS_VMODE level matches the MMC1_PBIAS_SUPPLY_HI_OUT output signal during normal operation
MMC1_IO_PWRDNZ	Protects the MMC1 I/O extended-drain cell when the SDMMC1_VDDS voltage is not stable. Software must keep this signal to 0b0 whenever the SDMMC1_VDDS supply voltage ramps up/down or changes. When this bit is at 0, the pad is floating.
SDMMC1_DRx_SPEEDCTRL, x = (0…2)	Speed control signals for three different SDMMC1 pad groups identified within the MMC1 I/O cell
SDMMC1_PUSTRENGTH_GRPx, x = (0…3)	Pullup strength controls for four different SDMMC1 pad groups identified within the MMC1 I/O cell
PBIAS1_PWRDNZ	Protects the PBIAS1 cell when the SIM_VDDS supply voltage is not stable. Software must keep the PWRDNZ signal to 0b0 whenever this supply voltage ramps up/down or changes. When this bit is at 0, the PBIAS1 output voltage is equal to SIM_VDDS voltage and the PBIAS supply detector is disabled.
PBIAS1_VMODE	Sets the SIM_VDDS voltage level (PBIAS1 side) according to which PBIAS1 cell generates appropriate biasing levels for the GPIOWK0GPIOWK2 and USBC1_ICUSB associated extended-drain I/Os. The default state of this bit is HIGH, indicating that the voltage level SIM_VDDS is 3.0 V.
PBIAS1_HIZ_MODE	When PBIAS1_HIZ_MODE is set to 1, the PBIAS1 output is in HIGH impedance. PBIAS1_ERROR is automatically set to 1 when PBIAS1_HIZ_MODE = 1. When PBIAS1_HIZ_MODE = 0, PBIAS1 is in normal operation mode.
PBIAS1_SUPPLY_HIGH_OUT	Output from the internal PBIAS1 voltage supply detector, which indicates whether the SIM_VDDS supply is 3.0 V or 1.8 V
PBIAS1_ERROR	Indicates whether the software-programmed PBIAS1_VMODE level matches the PBIAS1_SUPPLY_HI_OUT output signal during normal operation
GPIOWK_IO_PWRDNZ	Protects the GPIOWK0GPIOWK2 associated extended-drain I/O cell when the SIM_VDDS voltage is not stable Software must keep this signal to 0b0 whenever the SIM_VDDS supply voltage ramps up/down or changes. When this bit is set to 0, the pad is floating.
PAD_GPIO_WK1_LOW	This signal must be set to 0b0 to disable the strong pulldown available after reset on the gpio_wk1 pad. This is to ensure normal use of the gpio_wk1 pad.
0.22 PAD_GPIO_WK2_LOW	This signal must be set to 0b0 to disable the strong pulldown available after reset on the gpio_wk2 pad. This is to ensure normal use of the gpio_wk2 pad.
0.23 USBC1_ICUSB_IO_PWRDNZ	Protects the USBC1_ICUSB extended-drain I/O cell when the SIM_VDDS voltage is not stable. Software must keep this signal to 0b0 whenever the SIM_VDDS supply voltage ramps up/down or changes. When this bit is at 0, the pad is floating.
0.24 USBC1_DR0_SPEEDCTRL	Speed controls for the ICUSB pads associated with the USBC1_ICUSB associated I/O cell

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NOTE: When HIZ_MODE = 1, the PBIAS output (the pbias_mmc1 pin) must be tied to a defined external potential to avoid stress on transistors.

Table 18-13 lists the power supplies for PBIAS and the extended-drain I/O cells.

Table 18-13. Power Supplies

Name	Description
VDD2	Core voltage supply
SDMMC1_VDDS	MMC1 I/O cell supply voltage nominal 1.8 V/3.0 V
SIM_VDDS	USBC1_ICUSB and GPIOWK I/O cell supply voltage nominal 1.8 V/3.0 V
VDDS	1.8-V supply for the input buffer

18.4.9.1 PBIAS Cell

The MMC1_PBIAS cell provides a bias for the MMC/SD/SDIO1 extended-drain I/O cell used with high voltage for the MMC/SD/SDIO1 interface. This PBIAS cell provides a voltage reference (PBIAS voltage) for biasing extended-drain in the MMC/SD/SDIO1 cell. In addition to generating the bias voltage, the cell can detect the supply voltage (SDMMC1_VDDS) value (1.8 V or 3.0 V) and update, with its status, the CONTROL_PBIASLITE[24] MMC1_PBIASLITE_SUPPLY_HI_OUT bit. However, this is possible when the voltage reaches its steady state (the internal PBIAS voltage detector is enabled only when the MMC1_PBIAS_PWRDNZ signal is set to 0b1).

The PBIAS1 cell provides a reference voltage for biasing the gpiowk0gpiowk2 associated extended-drain I/O cell and the USBC1_ICUSB extended-drain I/O cell. In addition to generating the bias voltage, the cell can detect the supply voltage (SIM_VDDS) value (1.8 V or 3.0 V) and update, with its status, the CONTROL_PBIASLITE[30] PBIASLITE1_SUPPLY_HI_OUT bit. However, this is possible when voltage reaches its steady state (the internal PBIAS voltage detector is enabled only when the PBIAS1_PWRDNZ signal is set to 0b1).

CAUTION

A PBIAS cell lets the peripheral associated with its corresponding extended-drain I/O cells support 1.8-V and 3.0-V voltages. A PBIAS cell is not part of a peripheral, but part of the device I/Os to which this peripheral is internally connected. These device I/Os are not exclusive to one peripheral; through I/O multiplexing they can be connected to other internal signals. It is necessary to configure the PBIAS to enable the I/Os, regardless of how I/O multiplexing is configured for these device I/Os. In other words, independently of which signal is internally connected to a device I/O powered by SDMMC1_VDDS or SIM_VDDS, the corresponding PBIAS must be configured.

18.4.9.2 Extended-Drain I/O

The following MMC/SD/SDIO1 interface signals (selected when MuxMode = 0) use the device I/Os associated with the MMC1 extended-drain I/O cell:

- sdmmc1_clk
- sdmmc1_cmd
- sdmmc1_dati (where i = 0 to 7)

The MMC1 I/O cell is powered externally through the vdds_sdmmc1 pad.

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NOTE: The MMC1 I/O cell-associated device I/Os are also shared with other signals. gpio100gpio109, etc. are available when MuxMode is different than 0x0. If signals other than sdmmc1_x are selected , the MMC1 I/O cell must also be configured.

For more information about signal multiplexing, see Table 18-10.

For general-purpose (GP) device I/Os, which are part of the associated extended-drain cell of the GPIOWK pad , Muxmode = 3, Muxmode = 4 (gpio_wk0 pad only), and Muxmode = 6 are functional.

With Muxmode set to 0x3, the following signals are present:

- gpio_wk0
- gpio_wk1
- gpio_wk2

With Muxmode set to 0x4, the input signal (c2c_pwkup) is selected on the gpio_wk0 pad.

With Muxmode set to 0x6, the output signals (hw_dbg1, hw_dbg2, and hw_dbg3) are present at the gpio_wk0, gpio_wk1, and gpio_wk2 pads, respectively.

This PBIAS1 associated extended-drain I/O cell is externally powered through the vdds_sim pad.

NOTE: The GPIOWK-associated I/O cell must be properly configured when the gpio_wk0 through gpio_wk2 pads are used. For more information about signal multiplexing, see Table 18-10.

The following USBC1_ICUSB interface signals (selected through MuxMode = 0) use the device I/Os associated with the USBC1_ICUSB extended-drain I/O cell:

- usbc1_icusb_dp
- usbc1_icusb_dm

The USBC1_ICUSB I/O cell uses the same external power supply voltage as the GPIOWK cell (vdds_sim pad).

NOTE: The USBC1_ICUSB I/O cell associated device I/Os are also shared with the gpio_98 and gpio_99 signals when MuxMode = 0x3. The USBC1IC_ICUSB cell must be configured to allow for gpio_98 and gpio_99 operation. For more information about signal multiplexing, see Table 18-10.

Figure 18-13 shows the extended-drain I/O cells.

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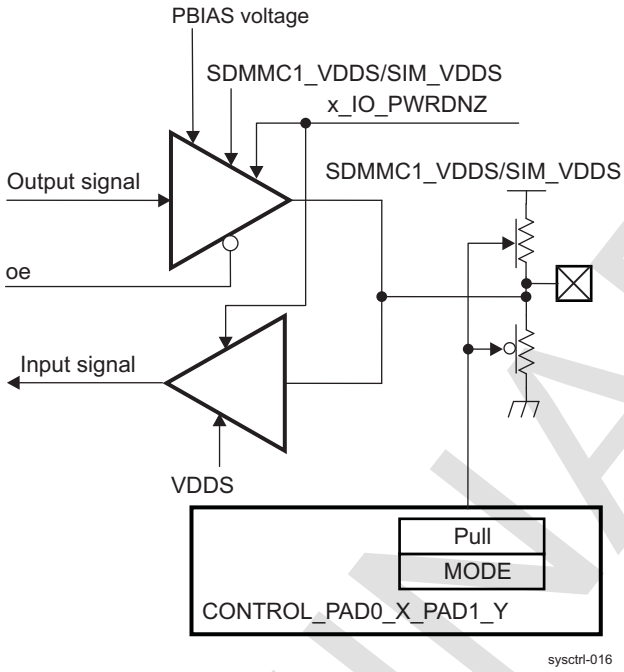
Figure 18-13. Extended-Drain I/O



The extended-drain I/O cells have the following I/O signals:

- The output signal, input signal, and oe, which comes from the selected I/O module with the correctly configured MUXMODE field within the corresponding CONTROL_CORE_PAD0_X_PAD1_Y or CONTROL_WKUP_PAD0_X_PAD1_Y register

NOTE: Extended-drain I/Os are muxed I/Os with mode and pullup/down configurations programmable in the control module.

- The PBIAS voltage is a voltage reference for biasing the extended-drain in the MMC1, USBC1_ICSUB, and GPIOWK I/O cells.
- The PWRDNZ signals are used to protect the I/O cells when the SDMMC1_VDDS/SIM_VDDS voltage is not stable.

CAUTION

Software must keep the PWRDNZ-related signals to 0b0 whenever the SDMMC1_VDDS or SIM_VDDS signal ramps up/down or changes. When it is set to 0, the pad is floating (the pad may not reflect the state of the output signal, and the input signal may not reflect the state of the pad).

- CONTROL_PBIASLITE[24] MMC1_PBIASLITE_SUPPLY_HI_OUT is a status bit on the SDMMC1_VDDS value and is used to inform the MMC1 I/O cell about the value of the SDMMC1_VDDS signal.
- CONTROL_PBIASLITE[30] PBIASLITE1_SUPPLY_HI_OUT is a status bit on the SIM_VDDS value and is used to inform the gpiowk0 through gpiowk2 associated I/O cell and USBC1_ICUSB I/O cell about the value of the SIM_VDDS signal.

For more information about the software configurations of the extended drain I/Os and PBIAS cells, see Section 18.5.1.2.2, *Extended-Drain I/Os and PBIAS Cells Programming Guide.*

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NOTE: The device can be supplied by an external power IC. TI provides such a global solution to its customers with the TWL60xx power IC.

If the device is associated with the TWL60xx power IC, before using an extended-drain I/O interface, software must program the TWL60xx to enable VMMC1 (for the MMC/SD/SDIO1 or muxed I/O modules) or VSIM (for the GPIOWK0, GPIOWK2 , USBC1_ICUSB, or muxed I/Os) and the LDO to provide 1.8-V/3.0-V voltage. This is done by software through the inter-integrated circuit (I^2C™) interface that links the device and the TWL60xx IC.

CAUTION

The power supply voltage generated from the companion power IC and applied on the vdds_sdmmc1 or vdds_sim device pins must be programmed according to the recommendations for the currently selected I/O module power supply range.

If the application does not want the I/O interface to run at 3.0 V, software users must then assert the VMODE signal to low for 1.8-V activity: in this case, the PBIAS is connected to ground.

Table 18-14 lists the control signal with the corresponding control bits from the CONTROL_PBIASLITE, CONTROL_MMC1, and CONTROL_GPIOWK registers to configure the PBIAS and the extended-drain I/O cells. These signals can be controlled by software.

Table 18-14. PBIAS/Extended-Drain I/O Cells Control Signals

Control Signals for Different PBIAS and Extended-Drain I/O Cells	Bits Used for PBIAS Cell and I/O Cell Configurations for Different I/O Modules	Reset Value
MMC1_PBIAS_PWRDNZ	CONTROL_PBIASLITE[22] MMC1_PBIASLITE_PWRDNZ	0
MMC1_PBIAS_VMODE	CONTROL_PBIASLITE[21] MMC1_PBIASLITE_VMODE	1
MMC1_PBIAS_HIZ_MODE	CONTROL_PBIASLITE[25] MMC1_PBIASLITE_HIZ_MODE	0
MMC1_PBIAS_SUPPLY_HIGH_OUT	CONTROL_PBIASLITE[24] MMC1_PBIASLITE_SUPPLY_HI_OUT	0
MMC1_PBIAS_ERROR	CONTROL_PBIASLITE[23] MMC1_PBIASLITE_VMODE_ERROR	0
MMC1_IO_PWRDNZ	CONTROL_PBIASLITE[26] MMC1_PWRDNZ	0
SDMMC1_DRx_SPEEDCTRL, x = (0…2)	CONTROL_MMC1[27] SDMMC1_DR0_SPEEDCTRL	0
	CONTROL_MMC1[26] SDMMC1_DR1_SPEEDCTRL	0
	CONTROL_MMC1[25] SDMMC1_DR2_SPEEDCTRL	0
SDMMC1_PUSTRENGTH_GRPx, x = (0…3)	CONTROL_MMC1[31] SDMMC1_PUSTRENGTH_GRP0	1
	CONTROL_MMC1[30] SDMMC1_PUSTRENGTH_GRP1	0
	CONTROL_MMC1[29] SDMMC1_PUSTRENGTH_GRP2	1
	CONTROL_MMC1[28] SDMMC1_PUSTRENGTH_GRP3	1
PBIAS1_PWRDNZ	CONTROL_PBIASLITE[28] PBIASLITE1_PWRDNZ	0
PBIAS1_VMODE	CONTROL_PBIASLITE[27] PBIASLITE1_VMODE	1
PBIAS1_HIZ_MODE	CONTROL_PBIASLITE[31] PBIASLITE1_HIZ_MODE	0
PBIAS1_SUPPLY_HIGH_OUT	CONTROL_PBIASLITE[30] PBIASLITE1_SUPPLY_HI_OUT	0
PBIAS1_ERROR	CONTROL_PBIASLITE[29] PBIASLITE1_VMODE_ERROR	0
GPIOWK_IO_PWRDNZ	CONTROL_GPIOWK[28] GPIOWK_IO_PWRDNZ	0
PAD_GPIO_WK1_LOW	CONTROL_GPIOWK[31] PAD_GPIO_WK1_LOW	1
PAD_GPIO_WK2_LOW	CONTROL_GPIOWK[29] PAD_GPIO_WK2_LOW	1
USBC1_ICUSB_IO_PWRDNZ	CONTROL_PBIASLITE[20] USBC1_ICUSB_PWRDNZ	0
USBC1_DR0_SPEEDCTRL	CONTROL_MMC1[24] USBC1_DR0_SPEEDCTRL	0

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The two PBIAS cells support two ranges of I/O SDMMC1_VDDS/SIM_VDDS: 1.8 V, typical for low-voltage applications, and 3.0 V, typical for high-voltage applications. For each supply voltage range, the cell generates suitable bias voltage (PBIAS) for extended-drain PMOS devices.

CAUTION

The PBIAS cell must be programmed according to peripheral power supply voltage. See Table 18-15.

Table 18-15. Voltage Configuration[1]

PBIASLITEVMODE Configuration	SDMMC1_VDDS/SIM_VDDS Voltage	Type of Operation
1.8 V	1.8 V	Normal 1.8-V operation
1.8 V	3.0 V	Damaging configuration[2]
3.0 V	1.8 V	Degraded functionality[2]
3.0 V	3.0 V	Normal 3.0-V operation

(1) For damaging configuration, hardware system protection is provided to prevent deterioration of the associated extended-drain I/Os.

(2) These modes must not be used.

The PBIAS output voltage is the same as SDMMC1_VDDS/SIM_VDDS voltage when the corresponding PWRDNZ bit is low. Once the SDMMC1_VDDS / SIM_VDDS supply is stable, software can release the PWRNDZ (setting it high). This starts the PBIAS cell work to generate the PBIAS voltage. During the completion process the corresponding I/Os cannot be used to transmit data. If VMODE is set correctly (compared with supply detector output and found to be the same), then PBIAS output voltage is generated based on the value of VMODE.

NOTE: In the case of a damaging configuration, hardware system protection prevents deterioration of the associated extended-drain I/Os.

CAUTION

The following requirements are critical for an extended-drain I/O cell:

- The VMODE bit must be defined before the PWRNDZ bit is made high (cell is brought out of power-down mode).
- The default state of VMODE bit is high (indicates 3.0-V operation).
- The PWRNDZ bit must be kept low whenever the SDMMC1_VDDS/SIM_VDDS supply ramps up/down or changes. This can be damaging.
- Supply detector is disabled when PWRDNZ = 0, and in this case, supply detector output (SUPPLY_HI_OUT) is initialized to 0.

18.4.9.3 PBIAS Error Generation

If VMODE and supply detector outputs are unequal, it takes 4 µs for the comparator to process the inputs and generate the VMODE_ERROR flag.

Table 18-16 summarizes the generation of the PBIAS error signals (MMC1_PBIAS_ERROR of the MMC1_PBIAS cell, and PBIAS1_ERROR of the PBIAS1 cell), which depend on the various CONTROL_PBIASLITE bit combinations. The shaded row in the table indicates a condition that could cause a reliability issue if not detected. To prevent this reliability issue, the PBIAS voltage is tied to SDMMC1_VDDS/SIM_VDDS when the PBIAS error signal is high. This disables the I/Os.

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CAUTION

Although asserting VMODE_ERROR to 1 ensures that PBIAS voltage is equal to SDMMC1_VDDS/SIM_VDDS, this does not completely protect the I/O cells. It is recommended that all the I/Os are powered down, setting the PWRDNZ mode bits of the corresponding I/O cells to 0b0 by software as soon as VMODE_ERROR = 0b1.

Table 18-16. PBIAS Error Signal Truth Table

VMODE	PWRDNZ	HIZ_MODE	SUPPLY_HI_OUT	VMODE_ERROR
0	0	X	0	0
0	1	0	0	0
0	1	0	1	1
X	1	1	X	1
1	0	X	0	0
1	1	0	0	1
1	1	0	1	0

NOTE: VMODE_ERROR = 0b1: VMODE level is not the same as SUPPLY_HI_OUT, or HiZ mode is selected.

VMODE_ERROR = 0b0: VMODE level is the same as SUPPLY_HI_OUT, or VMODE is not considered (PWRDNZ = 0b0).

The MMC1_PBIAS_ERROR and PBIAS1_ERROR signals are ORed and the outputs are mapped to the microprocessor unit (MPU) subsystem INTC. The interrupt line MA_IRQ_75 is activated upon error occurrence. For more information about the Cortex™-A9 MPU INTC registers and their description, see the *ARM Cortex-A9 Technical Reference Manual* .

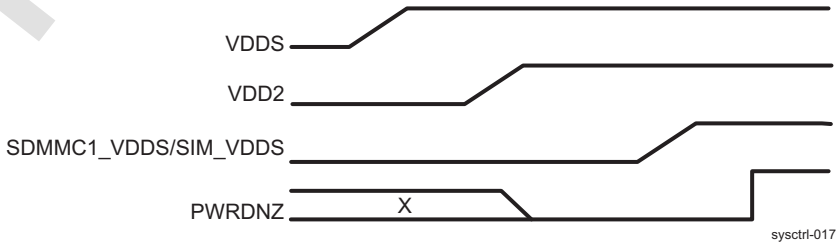
The CONTROL_PBIASLITE[29] PBIASLITE1_VMODE_ERROR and CONTROL_PBIASLITE[23] MMC1_PBIASLITE_VMODE_ERROR bits also indicate whether this kind of error occurs.

18.4.9.4 Critical Timing Requirements

It is critical that the PBIAS and I/O cell-related PWRDNZ bits are deasserted (made 1 from 0) only after SDMMC1_VDDS/SIM_VDDS power supply voltage is stable in the device. The cells support only the case where the 1.8-V input buffer supply voltage VDDS ramps up before VDD2 (core voltage). This power-up sequence is automatically provided upon POR by hardware in the device. Take care to ensure that the externally provided SDMMC1_VDDS/SIM_VDDS voltage (1.8 V/ 3 V) is powered up only after VDD2 and VDDS reach their steady state.

Figure 18-14 shows the only possible power-up sequence, as well as the expected behavior of PWRNDZ mode-related bits with regard to supplying voltage ramp up.

Figure 18-14. VDDS Ramps Up Before VDD2



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18.4.10 Band Gap Voltage and Temperature Sensor

The device supplies a voltage reference and a temperature sensor feature that are gathered in the band gap voltage and temperature sensor (VBGAPTS) module. The band gap provides current and voltage reference for its internal circuits and other analog IP blocks. The analog-to-digital converter (ADC) produces an output value that is proportional to the silicon temperature.

The main features of the VBGAPTS module are:

- A constant voltage reference output of 0.5 V
- Five constant current reference outputs of 1µA
- Analog supply is a nominal 1.8 V.
- Small ADC with 10-bit digital output
- Off mode compatible

A small finite state-machine (FSM) (band gap FSM) is instantiated inside the general core control module to help the VBGAPTS cell accomplish different measurement modes (see Section 18.4.10.2, *Temperature Sensor*) . In addition, two programmable comparator blocks inside the general core control module post-process the converted data and provide the following outputs:

- Thermal alert programmable comparator output
- Thermal shutdown programmable comparator output

Figure 18-15 shows the functional block diagram of the band gap and the temperature sensor module.

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Figure 18-15. Functional Block Diagram

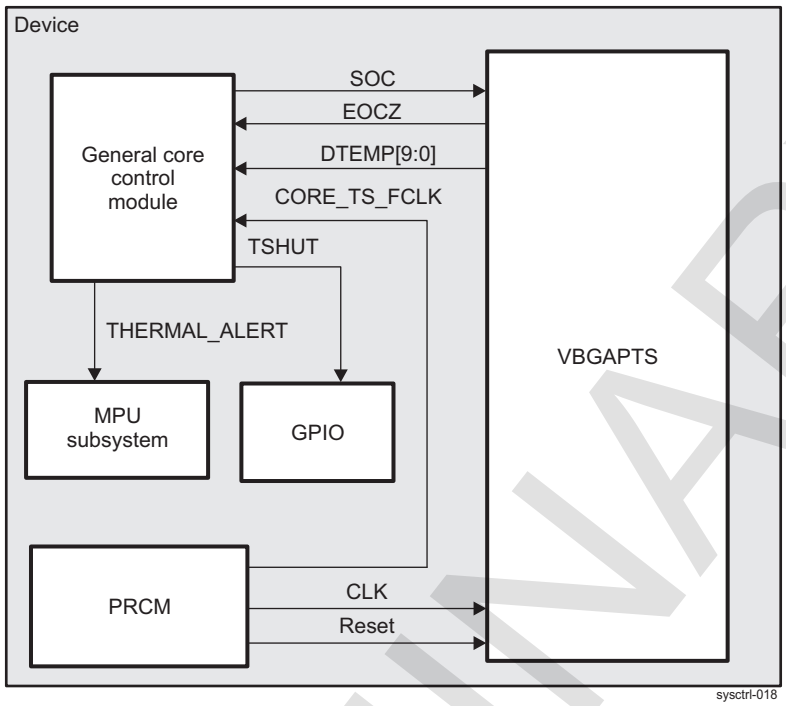

Table 18-17 describes the I/O signals, some of which (SOC, EOCZ, DTEMP[9:0]) build the interface between the VBGAPTS module and the bandgap state-machine of the general core control module.

Table 18-17. Band Gap Voltage and Temperature Sensor Signal Description

Pin	I/O (1)	Description
SOC	I	Start of Conversion signal. A transition to high starts a new ADC conversion cycle.
EOCZ	O	End of Conversion signal. When low, the signal indicates that the value of DTEMP[9:0] is valid.
DTEMP[9:0]	O	Temperature data from the temperature sensor. This value is valid when EOCZ is low.
CLRZ	I	When low, the temperature sensor is in reset mode. This signal must be low when OFFMODE is high.
CLK	I	Functional clock in the range (1–2 MHz) from the WKUP power domain used by the temperature sensor during temperature conversion

(1) I = Input, O = Output

All the configuration signals of the VBGAPTS temperature conversion logic are available through the CONTROL_TEMP_SENSOR register.

The bandgap state-machine of the general core control module is driven by a dedicated clock (CORE_TS_FCLK) that shares a common PRCM clock source with the VBGAPTS CLK. For more information about the thermal management clocks, see Chapter 3, *Power, Reset, and Clock Management*.

NOTE: The VBGAPTS functional clock delivered on CLK input is used only for the temperature sensor. When ADC is not converting, this clock can be switched off (CLK = 0). In this case, DTEMP[9:0] retains the temperature code obtained at the previous conversion.

NOTE: User software must ensure that the CONTROL_BANDGAP_STATUS[3] CLEAN_STOP bit read-only flag is high before switching off the VBGAPTS cell (CLK) and the bandgap state (CORE_TS_FCLK) clocks by programming the CONTROL_TEMP_SENSOR[13] BGAP_TEMPSOFF bit to 1. Status CLEAN_STOP = 1 indicates that the band gap state-machine is in IDLE state, and clocks can be safely switched off.

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Table 18-18 describes the functional outputs of the two post-processing comparator blocks integrated in the general core control module.

Table 18-18. General Core Control Thermal Logic Outputs Description

Functional Output	Description
THERMAL_ALERT	General core control module thermal alert output, mapped as an interrupt in the MPU subsystem. It is used by software to implement a thermal management policy of the device.
TSHUT	General core control module thermal shutdown comparator output, mapped on a GPIO input. This overheat protection signal is low during normal operation and goes high during a thermal shutdown event.

The configuration bits of the thermal post-processing logic are in several registers of the general core control module. For more information, see Section 18.4.10.2.3, *Thermal Data Post-Processing*.

18.4.10.1 Band Gap Voltage Reference

The band gap voltage reference feature provides several constant voltage and current references for its internal circuits and for other analog modules.

The voltage reference signal is a 0.5-V output. This output is used internally by the module and is exported for external modules or tests.

The current reference signals consist of five lines, each of which generates a 1-µA current with a 1.8-V voltage. These lines can be used to bias other modules.

18.4.10.2 Temperature Sensor

The temperature sensor feature is used to convert the temperature of the device into a decimal value coded on 10 bits. An internal ADC, which is part of the device embedded bandgap cell, is used for conversion.

For more information about the thermal sensor operating parameters (temperature range, accuracy, etc.), see the *Temperature Sensor* section in the device data manual.

For more information about the device operating junction temperature ranges under different conditions, see the *Recommended Operating Conditions* section in the device data manual.

NOTE: The temperature measured at the temperature sensor location is lower than the temperature of the hottest spot on the device die. This difference, defined also as the temperature offset between the on-die hottest spot temperature and the temperature registered by the on-die thermal sensor, depends on a number of factors, such as the current system power dissipation, device cooling conditions, etc.

CAUTION

User software must always take care to program thermal thresholds (thermal alert or TSHUT event points) at levels that do not exceed the device hottest spot maximal-allowed temperature minus the device temperature sensor offset estimated at current conditions.

The thermal alert interrupt events are described in Section 18.4.10.2.4, *Thermal Alert Functionality Comparators*.

The TSHUT signal is connected internally to a GPIO controller pin. For more information, see Chapter 25, *General-Purpose Interface*.

The bandgap state-machine offers two operating modes for the temperature sensor: single conversion mode and repeated single conversion mode.

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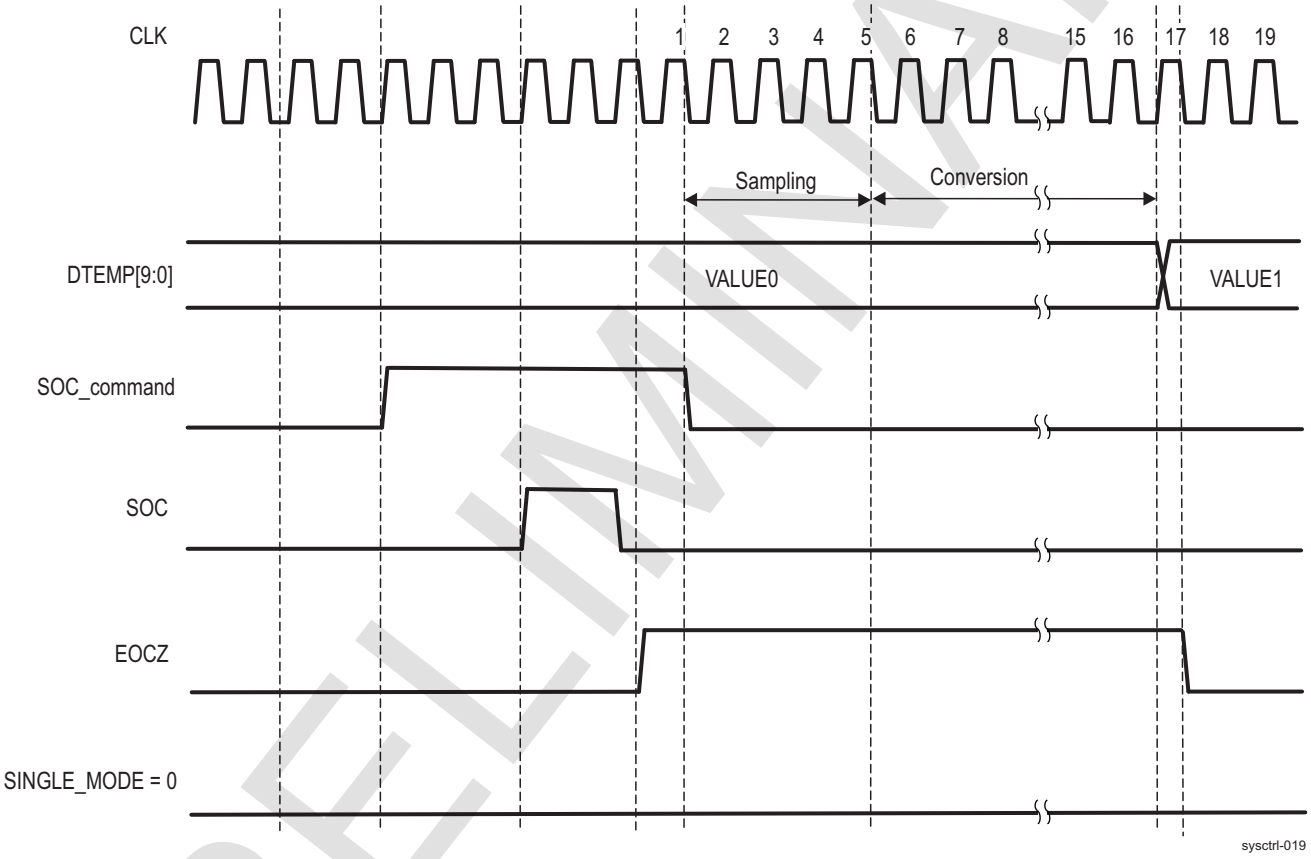
18.4.10.2.1 Single Conversion Mode

When the ADC is idle (CONTROL_TEMP_SENSOR[10] BGAP_TEMP_SENSOR_EOCZ = 0) and the CONTROL_BANDGAP_CTRL[31] SINGLE_MODE bit is set to 0, it is possible to ask for a single temperature conversion. To initiate a new conversion, the start of conversion bit (CONTROL_TEMP_SENSOR[11] BGAP_TEMP_SENSOR_SOC) must be asserted and maintained high until the end of conversion flag (CONTROL_TEMP_SENSOR[10] BGAP_TEMP_SENSOR_EOCZ) goes high, after which the SOC signal must be made low by setting the CONTROL_TEMP_SENSOR[11] BGAP_TEMP_SENSOR_SOC bit to 0. Conversion completion is indicated by a negative edge of EOCZ (the CONTROL_TEMP_SENSOR[10] BGAP_TEMP_SENSOR_EOCZ bit).

Figure 18-16 shows the timing sequence of a single temperature conversion. As can be seen in the figure, a single temperature conversion is performed by ADC for 17 band gap clock cycles.

Figure 18-16. Single Conversion Mode



18.4.10.2.2 Repeated Single Conversion Mode

A continuous temperature measurement on the device is performed as a sequence of single ADC conversions automatically initiated at regular intervals. A 24-bit counter inside the general core control module adds flexibility to program the delay between two consecutive SOC pulses generated from the band gap state-machine.

Two scenarios for ADC to work in a repeated single conversion mode are:

- Fixed-delay repeated single conversions
- Programmable-delay repeated single conversions

18.4.10.2.2.1 Fixed-Delay Repeated Single Conversions

The fixed-delay repeated single conversions scenario follows the sequence:

When the ADC is idle (CONTROL_TEMP_SENSOR[10] BGAP_TEMP_SENSOR_EOCZ = 0), and

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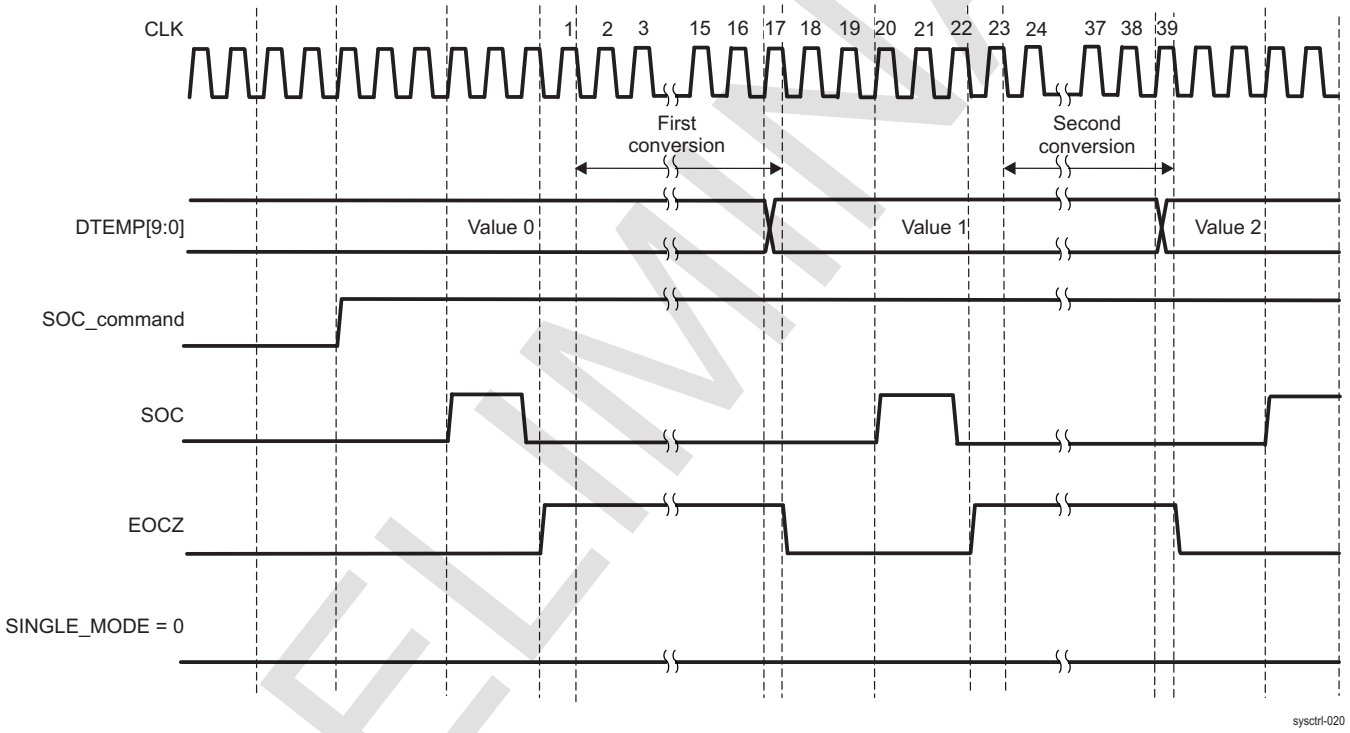
CONTROL_BANDGAP_CTRL[31] SINGLE_MODE = 0, the bandgap state-machine can be forced to generate a series of SOC pulses if the CONTROL_TEMP_SENSOR[11] BGAP_TEMP_SENSOR_SOC bit is asserted high and continuously maintained in this state during the required temperature monitoring period. The user software must deassert the CONTROL_TEMP_SENSOR[11] BGAP_TEMP_SENSOR_SOC bit to 0 when the CONTROL_TEMP_SENSOR[10] BGAP_TEMP_SENSOR_EOCZ status bit is set high for the last temperature measurement.

As described in Section 18.4.10.2.1, *Single Conversion Mode*, valid data on the DTEMP[9:0] bus upon single conversion completion is indicated by a negative edge of the EOCZ signal. For the software, CONTROL_TEMP_SENSOR[10] BGAP_TEMP_SENSOR_EOCZ = 0 signals that the temperature data CONTROL_TEMP_SENSOR[7:0] BGAP_TEMP_SENSOR_DTEMP bit field is updated.

Figure 18-17 shows the timing sequence for fixed-delay repeated single mode.

In this case, there is no flexibility to control delay between two consecutive SOC pulses, because with CONTROL_BANDGAP_CTRL[31] SINGLE_MODE = 0 band gap counter logic is disabled .The delay is fixed to 22 bandgap functional clock cycles.

Figure 18-17. Fixed-Delay Repeated Single Conversions



18.4.10.2.2.2 Programmable-Delay Repeated Single Conversions

In the programmable-delay repeated single conversions mode the bandgap state-machine uses a 24-bit incremental counter (part of the thermal post-processing logic of the general core control module) to generate a series of SOC pulses with a programmable delay between them.

The programmable-delay repeated single conversions scenario follows this sequence:

Before enabling this mode, the user must write the desired delay value as the number of bandgap CLK cycles in the CONTROL_BGAP_COUNTER[23:0] COUNTER bit field. When the ADC is idle (CONTROL_TEMP_SENSOR[10] BGAP_TEMP_SENSOR_EOCZ = 0) and CONTROL_TEMP_SENSOR[11] BGAP_TEMP_SENSOR_SOC = 0, the user must assert CONTROL_BANDGAP_CTRL[31] SINGLE_MODE = 1 to enable programmable-delay repeated single conversions.

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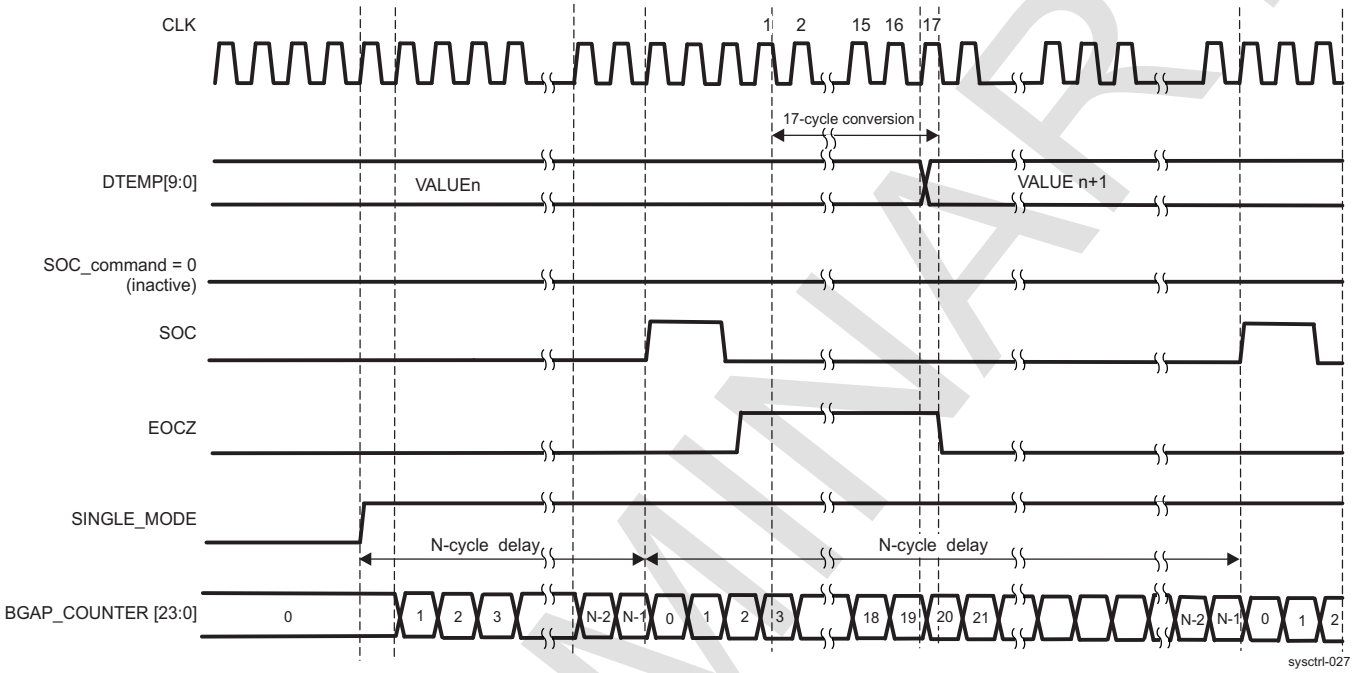
NOTE: The programmable-delay repeated single conversions require that software keeps CONTROL_TEMP_SENSOR[11] BGAP_TEMP_SENSOR_SOC = 0 during the measurement sequence.

Figure 18-18 shows the timing sequence for a programmable-delay repeated single mode.

Figure 18-18. Programmable-Delay Repeated Single Conversions



As Figure 18-18 shows, the initial SOC pulse of a sequence is generated N-cycles after assertion of the SINGLE_MODE bit, when BGAP_COUNTER reaches N-1. The N-cycle period is repeated for consecutive SOC insertions until the sequence is stopped in software by deasserting the CONTROL_BANDGAP_CTRL[31] SINGLE_MODE bit to 0.

The signal synchronization described in Section 18.4.10.2.1, *Single Conversion Mode*, applies to each single conversion in a measurement series. The general core control module sends the SOC pulses at regular programmable intervals defined through the value of the BGAP_COUNTER bit field and registers the temperature when EOCZ is asserted low. Software must populate the correct value based on the band gap frequency and monitoring frequency, knowing that the band gap, regardless of the clock frequency, delivers its temperature after 17 clock cycles.

Table 18-19 provides examples for programming SOC pulse generation periods based on minimal (1 MHz) and maximal (2 MHz) band gap clock frequency.

Table 18-19. Bandgap Counter Programming Examples

	Monitoring Period				
Bandgap Clock	**10 ms**	**20 ms**	**50 ms**	**100 ms**	**500 ms**
1 MHz – 1000 ns	10,000 cycles	20,000 cycles	50,000 cycles	100,000 cycles	200,000 cycles
2 MHz – 500 ns	20,000 cycles	40,000 cycles	100,000 cycles	200,000 cycles	1,000,000 cycles

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18.4.10.2.3 Thermal Data Post-Processing Logic

A thermal data post-processing logic with dedicated registers is implemented in the general core control module. The registered ADC value is passed in parallel to the inputs of four comparators (two sets of two comparators). In each set, the temperature data is compared to high- and low-temperature thresholds defined in software, to handle the hysteresis effect when temperature decreases. The two comparator sets provide different thermal management functions.

Figure 18-19 shows the thermal management schema in the device.

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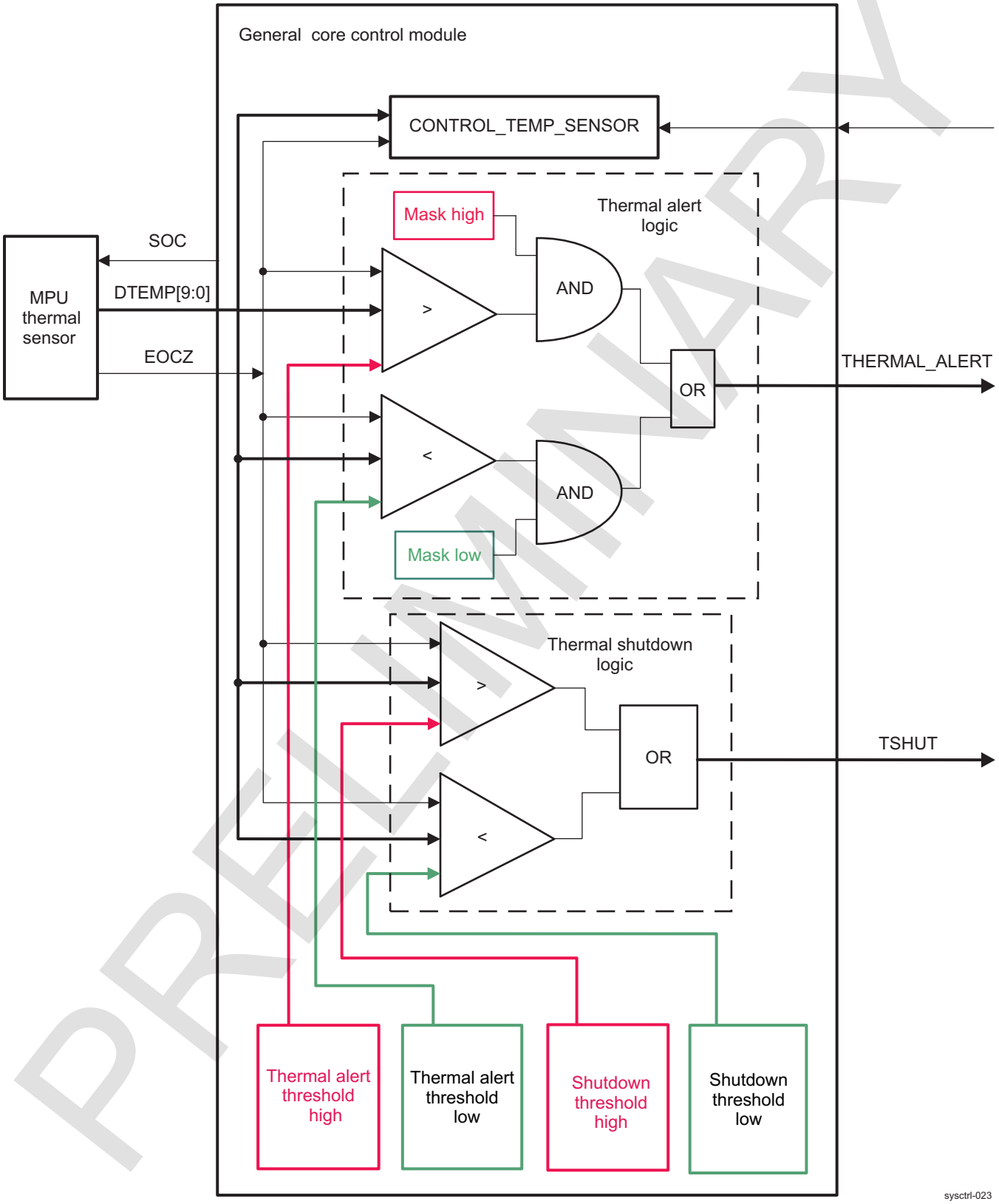
Figure 18-19. Thermal Management Schema



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NOTE: The software settings of the comparator blocks must be applied before starting a single or repeated-single measurement sequence.

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18.4.10.2.4 Thermal Alert Functionality Comparators

The first set of comparators provides a thermal alert function output. The high- and low-temperature thresholds for this function are configurable through the 10-bit CONTROL_BANDGAP_THRESHOLD[25:16] T_HOT and CONTROL_BANDGAP_THRESHOLD[9:0] T_COLD bit fields, respectively. Thermal alert logic in the general core control module provides the capability to mask (active low) comparator outputs for hot and cold events through the CONTROL_BANDGAP_CTRL[1] MASK_HOT and CONTROL_BANDGAP_CTRL[0] MASK_COLD bits. Figure 18-20 shows the functional logic of these 2 bits to mask comparator outputs for hot and cold thermal alert events. The masked HOT and COLD point monitoring signals are then ORed in the THERMAL_ALERT signal, which delivers an interrupt to the MPU subsystem on the MA_IRQ_126 input (see Section 18.3, *Control Module Integration*). It can be used by software to implement a thermal management policy of the device. For more information about this interrupt, see Section 17.3.2,*Interrupt Requests to the Cortex-A9 MPU Interrupt Controller*.

The nonmasked outputs of the thermal alert logic comparators are individually registered in the CONTROL_BANDGAP_STATUS[1] HOT_FLAG and CONTROL_BANDGAP_STATUS[0] COLD_FLAG read-only (RO) bits. The masked ORed event (that is, the THERMAL_ALERT signal) is mapped to the CONTROL_BANDGAP_STATUS[2] BGAP_ALERT RO bit. Figure 18-20 shows the behavior of the thermal alert logic.

NOTE: The thermal processing logic of the general core control module generates an interrupt event to the MPU subsystem whenever the registered temperature of on-die thermal sensor crosses a software-configurable threshold.

CAUTION

Users must take care to program the value of the CONTROL_BANDGAP_THRESHOLD[25:16] T_HOT bit field such that its corresponding temperature value does not exceed the maximal-allowed on-die temperature minus the temperature sensor offset estimated for the current conditions. For more information about the sensed temperature value constraints, see Section 18.4.10.2, *Temperature Sensor*.

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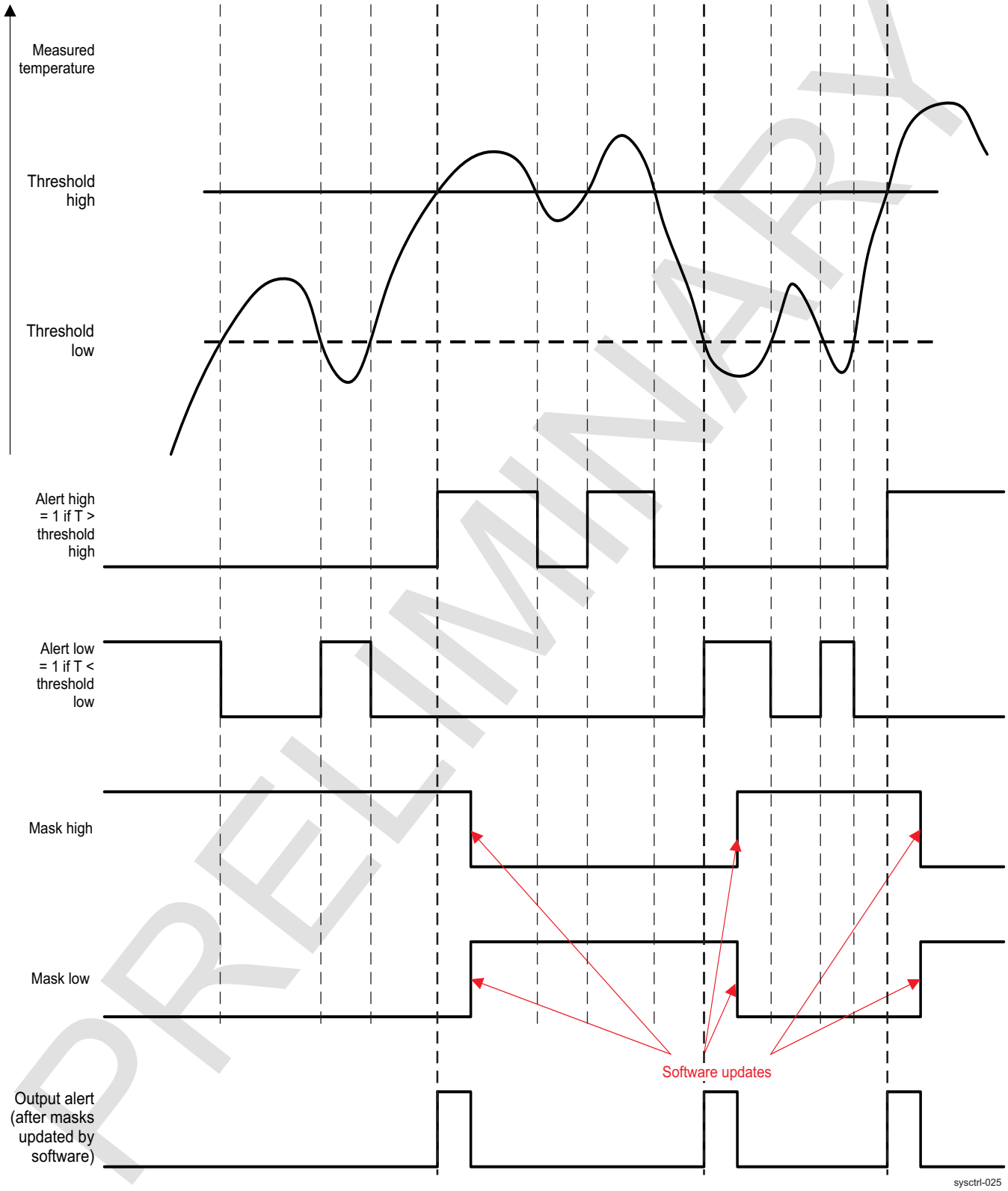
Figure 18-20. Thermal Alert Generation Signals



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18.4.10.2.5 Thermal Shutdown Functionality Comparators

The second set of two comparators in the general core control module is responsible for the thermal shutdown protection of the device. Two 10-bit fields (CONTROL_TSHUT_THRESHOLD[25:16] TSHUT_HOT and CONTROL_TSHUT_THRESHOLD[9:0] TSHUT_COLD) define the high- and low-threshold code values, respectively. The default value of the TSHUT_HOT bit field corresponds to the maximum allowed on the device die temperature (123°C). When the maximal temperature (TSHUT_HOT) is reached, TSHUT output is activated. The TSHUT output of the general core control module is tied internally to a GPIO3 module input pin (see Section 18.3, *Control Module Integration*). Its main purpose is to indicate that the maximum junction temperature of the die is reached, which is true when the temperature measured by the on-die sensor (at sensor location), satisfies the condition:

$T_{sensor_location_max_tshut}$, °C = $T_{max_allowed_hottest_spot}$, °C – $\Delta T_{estimated_temp_offset}$, °C

To prevent device malfunction or permanent damage to the device, software must take immediate action to reduce power dissipation by warm-resetting the device or freezing most internal activities.

CAUTION

User software must always provide that the temperature corresponding to the programmed value of the CONTROL_TSHUT_THRESHOLD[25:16] TSHUT_HOT bit field does not exceed the described $T_{sensor_location_max_tshut}$ limit value. For more information about the sensed temperature value constraints, see Section 18.4.10.2, *Temperature Sensor*.

For more information about thermal-related GPIO interrupts, see Chapter 25, *General-Purpose Interface*.

To deactivate TSHUT output, the temperature ADC-encoded value must go below the value of TSHUT_COLD threshold.

CAUTION

In case of a thermal shutdown event (T_{shut_hot}, °C value exceeded), users must take care to software-trigger a warm reset on the device upon a GPIO-generated TSHUT interrupt event. The device has no hardware mechanism to automatically generate a thermal-shutdown warm reset.

Figure 18-21 shows the behavior of the TSHUT logic.

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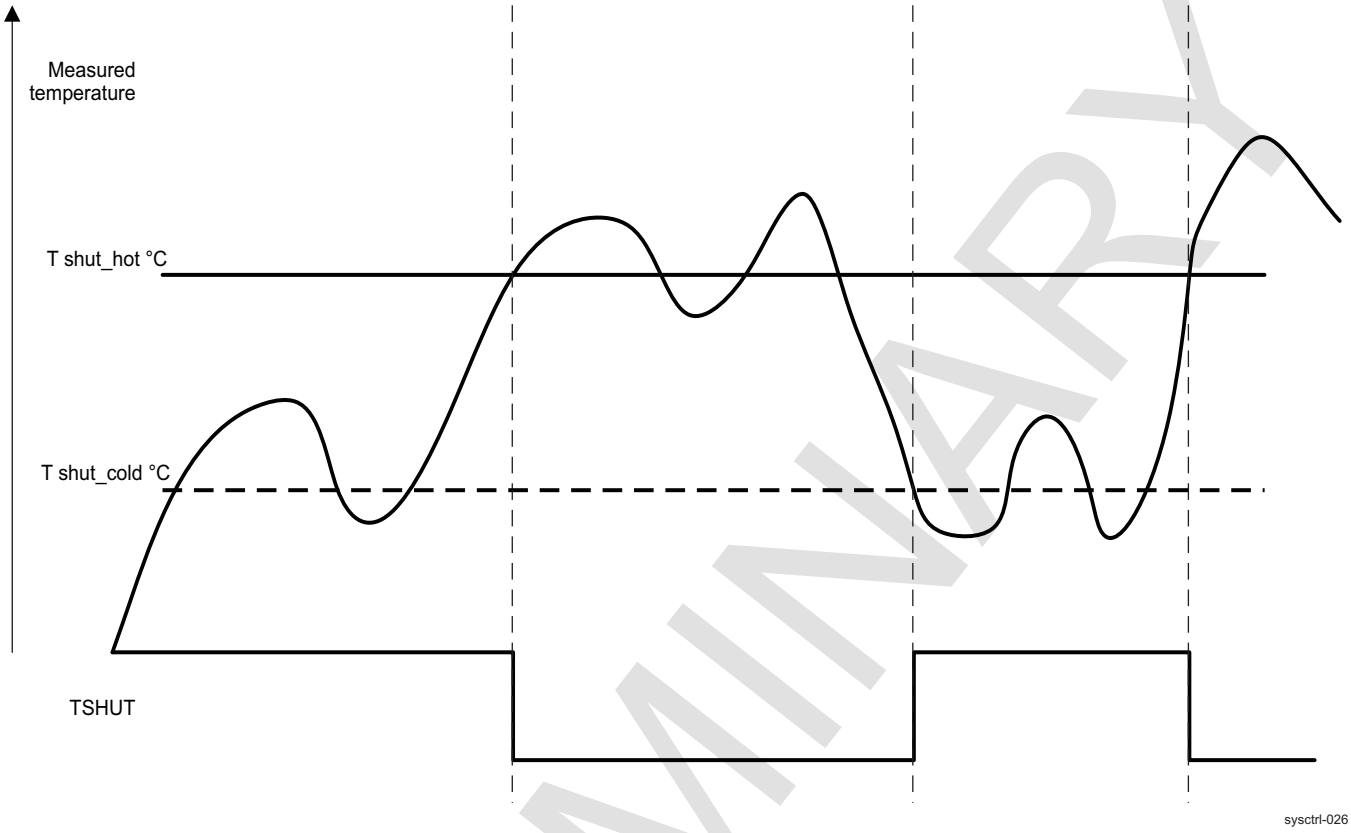
Figure 18-21. Thermal Alert Generation Signals



18.4.10.2.6 ADC Codes Versus Temperature

Table 18-20 gives the temperature range that corresponds to each value of the CONTROL_TEMP_SENSOR[9:0] BGAP_TEMP_SENSOR_DTEMP bit field.

Table 18-20. ADC Code Versus Temperature

ADC Code	Temperature °C		ADC Code	Temperature °C		ADC Code	Temperature °C		ADC Code	Temperature °C	
	From	To		From	To		From	To		From	To
530	–40–	–40	631	1.4	1.8	732	44.2	44.6	833	86.2	86.6
531	–40	–40	632	1.8	2.4	733	44.6	45	834	86.6	87
532	–40	–40	633	2.4	2.8	734	45	45.6	835	87	87.6
533	–40	–40	634	2.8	3.2	735	45.6	46	836	87.6	88
534	–40	–39.6	635	3.2	3.6	736	46	46.4	837	88	88.4
535	–39.6	–39.2	636	3.6	4	737	46.4	46.8	838	88.4	88.8
536	–39.2	–38.8	637	4	4.4	738	46.8	47.2	839	88.8	89.2
537	–38.8	–38.4	638	4.4	4.8	739	47.2	47.6	840	89.2	89.6
538	–38.4	–38	639	4.8	5.4	740	47.6	48	841	89.6	90
539	–38	–37.6	640	5.4	5.8	741	48	48.4	842	90	90.4
540	–37.6	–37	641	5.8	6.2	742	48.4	48.8	843	90.4	90.8
541	–37	–36.6	642	6.2	6.6	743	48.8	49.2	844	90.8	91.2
542	–36.6	–36.2	643	6.6	7	744	49.2	49.8	845	91.2	91.6
543	–36.2	–35.8	644	7	7.4	745	49.8	50.2	846	91.6	92
544	–35.8	–35.4	645	7.4	7.8	746	50.2	50.6	847	92	92.4

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Table 18-20. ADC Code Versus Temperature (continued)

ADC Code	Temperature ˚C		ADC Code	Temperature ˚C		ADC Code	Temperature ˚C		ADC Code	Temperature ˚C	
	From	To		From	To		From	To		From	To
545	–35.4	–35	646	7.8	8.2	747	50.6	51	848	92.4	92.8
546	–35	–34.6	647	8.2	8.8	748	51	51.4	849	92.8	93.2
547	–34.6	–34	648	8.8	9.2	749	51.4	51.8	850	93.2	93.6
548	–34	–33.6	649	9.2	9.6	750	51.8	52.2	851	93.6	94
549	–33.6	–33.2	650	9.6	10	751	52.2	52.6	852	94	94.4
550	–33.2	–32.8	651	10	10.4	752	52.6	53	853	94.4	94.8
551	–32.8	–32.4	652	10.4	10.8	753	53	53.4	854	94.8	95.2
552	–32.4	–32	653	10.8	11.2	754	53.4	54	855	95.2	95.8
553	–32	–31.6	654	11.2	11.6	755	54	54.4	856	95.8	96.2
554	–31.6	–31	655	11.6	12.2	756	54.4	54.8	857	96.2	96.6
555	–31	–30.6	656	12.2	12.6	757	54.8	55.2	858	96.6	97
556	–30.6	–30.2	657	12.6	13	758	55.2	55.6	859	97	97.4
557	–30.2	–29.8	658	13	13.4	759	55.6	56	860	97.4	97.8
558	–29.8	–29.4	659	13.4	13.8	760	56	56.4	861	97.8	98.2
559	–29.4	–29	660	13.8	14.2	761	56.4	56.8	862	98.2	98.6
560	–29	–28.4	661	14.2	14.6	762	56.8	57.2	863	98.6	99
561	–28.4	–28	662	14.6	15	763	57.2	57.6	864	99	99.4
562	–28	–27.6	663	15	15.6	764	57.6	58	865	99.4	99.8
563	–27.6	–27.2	664	15.6	16	765	58	58.4	866	99.8	100.2
564	–27.2	–26.8	665	16	16.4	766	58.4	59	867	100.2	100.6
565	–26.8	–26.4	666	16.4	16.8	767	59	59.4	868	100.6	101
566	–26.4	–26	667	16.8	17.2	768	59.4	59.8	869	101	101.4
567	–26	–25.4	668	17.2	17.6	769	59.8	60.2	870	101.4	101.8
568	–25.4	–25	669	17.6	18	770	60.2	60.6	871	101.8	102.2
569	–25	–24.6	670	18	18.4	771	60.6	61	872	102.2	102.6
570	–24.6	–24.2	671	18.4	19	772	61	61.4	873	102.6	103
571	–24.2	-23.8	672	19	19.4	773	61.4	61.8	874	103	103.4
572	-23.8	–23.4	673	19.4	19.8	774	61.8	62.2	875	103.4	103.8
573	-23.4	–23	674	19.8	20.2	775	62.2	62.6	876	103.8	104.2
574	–23	–22.4	675	20.2	20.6	776	62.6	63	877	104.2	104.6
575	–22.4	–22	676	20.6	21	777	63	63.6	878	104.6	105
576	–22	–21.6	677	21	21.4	778	63.6	64	879	105	105.4
577	–21.6	–21.2	678	21.4	21.8	779	64	64.4	880	105.4	105.8
578	–21.2	-20.8	679	21.8	22.4	780	64.4	64.8	881	105.8	106.4
579	–20.8	–20.4	680	22.4	22.8	781	64.8	65.2	882	106.4	106.8
580	–20.4	–20	681	22.8	23.2	782	65.2	65.6	883	106.8	107.2
581	–20	–19.4	682	23.2	23.6	783	65.6	66	884	107.2	107.6
582	–19.4	–19	683	23.6	24	784	66	66.4	885	107.6	108
583	–19	–18.6	684	24	24.4	785	66.4	66.8	886	108	108.4
584	–18.6	–18.2	685	24.4	24.8	786	66.8	67.2	887	108.4	108.8
585	–18.2	-17.8	686	24.8	25.2	787	67.2	67.6	888	108.8	109.2
586	–17.8	-17.4	687	25.2	25.6	788	67.6	68	889	109.2	109.6
587	–17.4	–17	688	25.6	26.2	789	68	68.4	890	109.6	110
588	–17	–16.4	689	26.2	26.6	790	68.4	69	891	110	110.4
589	–16.4	–16	690	26.6	27	791	69	69.4	892	110.4	110.8
590	–16	–15.6	691	27	27.4	792	69.4	69.8	893	110.8	111.2

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Table 18-20. ADC Code Versus Temperature (continued)

ADC Code	Temperature ˚C		ADC Code	Temperature ˚C		ADC Code	Temperature ˚C		ADC Code	Temperature ˚C	
	From	To		From	To		From	To		From	To
591	–15.6	–15.2	692	27.4	27.8	793	69.8	70.2	894	111.2	111.6
592	–15.2	–14.8	693	27.8	28.2	794	70.2	70.6	895	111.6	112
593	–14.8	–14.4	694	28.2	28.6	795	70.6	71	896	112	112.4
594	–14.4	–14	695	28.6	29	796	71	71.4	897	112.4	112.8
595	–14	–13.4	696	29	29.6	797	71.4	71.8	898	112.8	113.2
596	–13.4	–13	697	29.6	30	798	71.8	72.2	899	113.2	113.6
597	–13	–12.6	698	30	30.4	799	72.2	72.6	900	113.6	114
598	–12.6	–12.2	699	30.4	30.8	800	72.6	73	901	114	114.4
599	–12.2	–11.8	700	30.8	31.2	801	73	73.4	902	114.4	114.8
600	–11.8	–11.4	701	31.2	31.6	802	73.4	73.8	903	114.8	115.2
601	–11.4	–11	702	31.6	32	803	73.8	74.4	904	115.2	115.6
602	–11	–10.4	703	32	32.4	804	74.4	74.8	905	115.6	116
603	–10.4	–10	704	32.4	32.8	805	74.8	75.2	906	116	116.4
604	–10	–9.6	705	32.8	33.4	806	75.2	75.6	907	116.4	116.8
605	–9.6	–9.2	706	33.4	33.8	807	75.6	76	908	116.8	117.2
606	–9.2	–8.8	707	33.8	34.2	808	76	76.4	909	117.2	117.6
607	–8.8	–8.4	708	34.2	34.6	809	76.4	76.8	910	117.6	118
608	–8.4	–8	709	34.6	35	810	76.8	77.2	911	118	118.4
609	–8	–7.4	710	35	35.4	811	77.2	77.6	912	118.4	118.8
610	–7.4	–7	711	35.4	35.8	812	77.6	78	913	118.8	119.2
611	–7	–6.6	712	35.8	36.2	813	78	78.4	914	119.2	119.6
612	–6.6	–6.2	713	36.2	36.6	814	78.4	78.8	915	119.6	120
613	–6.2	–5.8	714	36.6	37	815	78.8	79.2	916	120	120.4
614	–5.8	–5.4	715	37	37.6	816	79.2	79.6	917	120.4	120.8
615	–5.4	–5	716	37.6	38	817	79.6	80	918	120.8	121.2
616	–5	–4.6	717	38	38.4	818	80	80.6	919	121.2	121.6
617	–4.6	–4	718	38.4	38.8	819	80.6	81	920	121.6	122
618	–4	–3.6	719	38.8	39.2	820	81	81.4	921	122	122.4
619	–3.6	–3.2	720	39.2	39.6	821	81.4	81.8	922	122.4	122.8
620	–3.2	–2.8	721	39.6	40	822	81.8	82.2	923	122.8	123.2
621	–2.8	–2.4	722	40	40.4	823	82.2	82.6	924	Outside range of operation	Outside range of operation
622	–2.4	–2	723	40.4	40.8	824	82.6	83	925	Outside range of operation	Outside range of operation
623	–2	–1.6	724	40.8	41.4	825	83	83.4	926	Outside range of operation	Outside range of operation
624	–1.6	–1	725	41.4	41.8	826	83.4	83.8	927	Outside range of operation	Outside range of operation
625	–1	–0.6	726	41.8	42.2	827	83.8	84.2	928	Outside range of operation	Outside range of operation
626	–0.6	–0.2	727	42.2	42.6	828	84.2	84.6	929	Outside range of operation	Outside range of operation

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Table 18-20. ADC Code Versus Temperature (continued)

ADC Code	Temperature °C		ADC Code	Temperature °C		ADC Code	Temperature °C		ADC Code	Temperature °C	
	From	To		From	To		From	To		From	To
627	–0.2	0.2	728	42.6	43	829	84.6	85	930	Outside range of operation	Outside range of operation
628	0.2	0.6	729	43	43.4	830	85	85.4	931	Outside range of operation	Outside range of operation
629	0.6	1	730	43.4	43.8	831	85.4	85.8	932	Outside range of operation	Outside range of operation
630	1	1.4	731	43.8	44.2	832	85.8	86.2		Outside range of operation	

NOTE: ADC code values in the subranges 0–529 and 933–1023 are reserved for future use.

18.4.11 Hardware Observability

18.4.11.1 Device Internal Signals Observability Overview

The general control module provides observability features covering different module internal signals related to:

- Power and reset management protocol inside different power domains
- Power domain states/transition indication
- Interrupt requests by different modules
- DMA requests by different modules
- Clocks and clock management

The associated signal multiplexing function is controlled through the hardware observability I/O multiplexing registers (32-bit read/write registers). The selected observable signals are multiplexed between the general control module CORE and/or WKUP power domain and are output on the po_hw_dbg[31:0] observability bus at the boundaries of the general wake-up control module. The po_hw_dbg[31:0] observability outputs are then exported to the device control module logic to be further multiplexed as their corresponding hw_dbg[31:0] signals on the different pads of the WKUP or CORE power domain of the device control module (see Section 18.4.11.4, *Observability Signals Multiplexing at Device Control Module Level)*.

NOTE: Each signal po_hw_dbg_i (where i = 0 to 31) of the general control wakeup po_hw_dbg[31:0] bus is propagated by device control module-level logic as its corresponding hw_dbgi output signal at the device boundary (where i = 0 to 31) for the device CORE power domain pads and where i = 0 to 13 for the device WKUP power domain pads (with the constraint that hw_dbg0 and hw_dbg11 are multiplexed on the same WKUP power domain pad) described in Section 18.4.11.4, *Observability Signals Multiplexing at Device Control Module Level*.

Figure 18-22 is an overview of observability multiplexing, which minimizes the number of signals exchanged at the device boundary.

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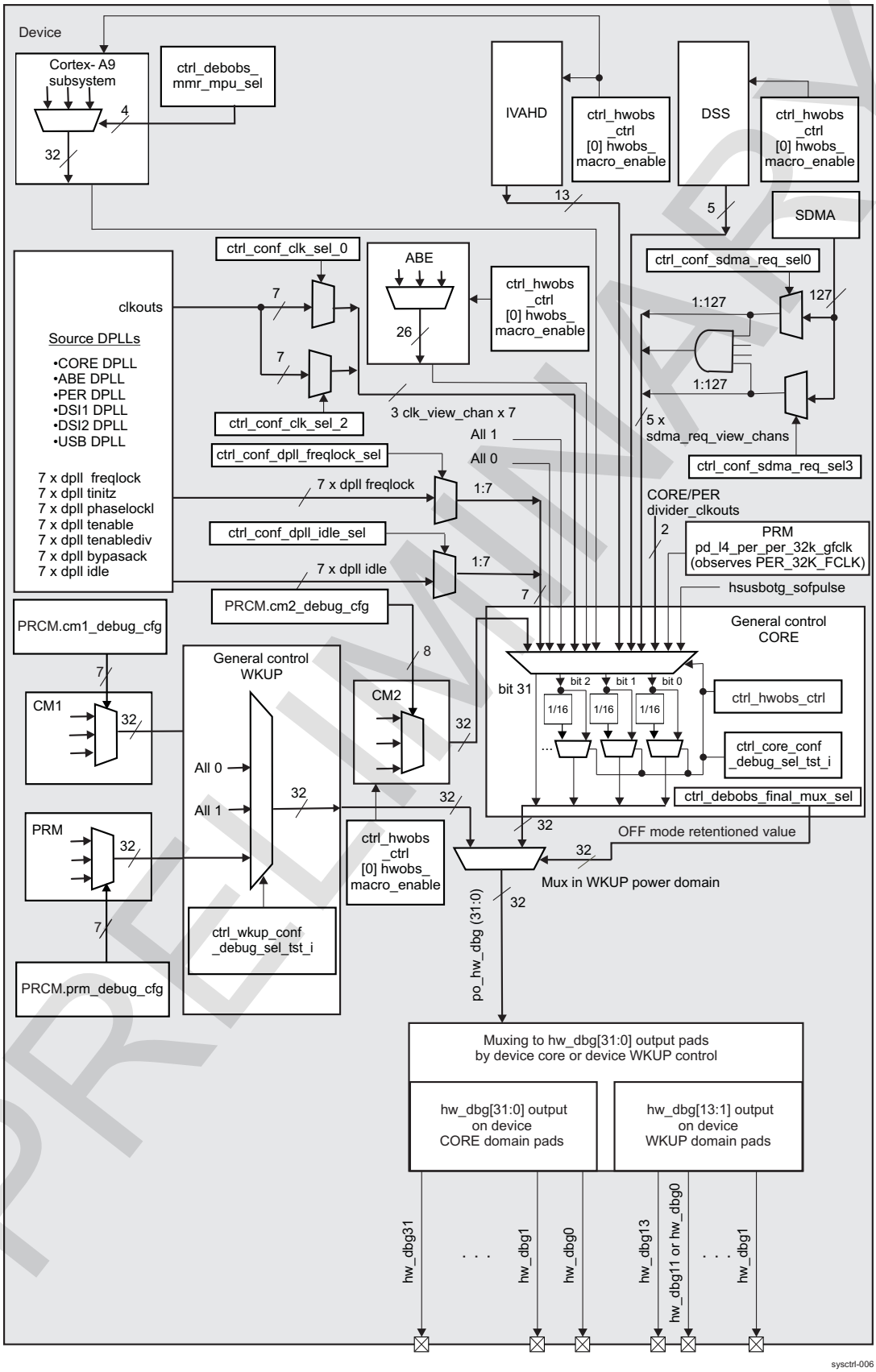
Figure 18-22. Overview of the Hardware Observability Functionality



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18.4.11.2 Observability Gating Capabilities

The programmer has the option to gate all 32 signals of the observability bus simultaneously at the observability paths of the CORE and WKUP power domains , keeping them tied to 1 (CONTROL_HWOBS_CONTROL[1] HWOBS_ALL_ONE_MODE = 0b1) or keeping them tied to 0 (CONTROL_HWOBS_CONTROL[2] HWOBS_ALL_ZERO_MODE = 0b1). This can be useful to check the path from hardware observability to external pads. These two bits must be set to 0 to enable the observability feature for all observability pads.

Additionally, the CONTROL_HWOBS_CONTROL[0] HWOBS_MACRO_ENABLE bit provides the gating feature only to observability signals muxed in the CORE power domain that come from the following modules (identified in the so-called MACRO group):

- CORTEX-A9 MPU subsystem
-
- IVA-HD
- Display subsystem
- CM2
- ABE

When CONTROL_HWOBS_CONTROL[0] HWOBS_MACRO_ENABLE = 0b0, the observability outputs associated with the MACRO group are gated and forced to 0b0.

NOTE: Do not set the observability gating bits CONTROL_HWOBS_CONTROL[1] HWOBS_ALL_ONE_MODE and CONTROL_HWOBS_CONTROL[2] HWOBS_ALL_ZERO_MODE simultaneously to 1 to avoid undefined states of the observability bus.

The clock frequency of the hw_dbg0, hw_dbg1, and hw_dbg2 signals can be optionally divided by 1, 2, 4, 8, or 16 through programming dedicated bit fields in CONTROL_HWOBS_CONTROL.

Assignment of dividers to the hw_dbg0, hw_dbg1, and hw_dbg2 signals applies only in the CORE power domain, as follows:

- [7:3] HWOBS_CLKDIV_SEL for hw_dbg0
- [13:9] HWOBS_CLKDIV_SEL_1 for hw_dbg1
- [18:14] HWOBS_CLKDIV_SEL_2 for hw_dbg2

NOTE: Only the CORE power domain signals hw_dbg0, hw_dbg1, and hw_dbg2 pass through the CONTROL_HWOBS_CONTROL programmable dividers. These dividers are not available to the corresponding po_hw_dbg(0), po_hw_dbg(1), and po_hw_dbg(2) lines in the WKUP power domain.

NOTE: To enable observability over the po_hw_dbg(0), po_hw_dbg(1), and po_hw_dbg(2) bus lines, the HWOBS_CLKDIV_SEL, HWOBS_CLKDIV_SEL_1, and HWOBS_CLKDIV_SEL_2 bit fields in the CONTROL_HWOBS_CONTROL register must be set different than 0. The default value (0) is not sufficient to see the observability value at the hw_dbg0, hw_dbg1, and hw_dbg2 pins.

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NOTE: The hw_dbg0, hw_dbg1, and hw_dbg2 frequency division and ability to gate the MACRO group observability signals (hw_dbg i, configurable in the CONTROL_HWOBS_CONTROL register) are limited to the hardware observability signals hw_dbg i (where i = 0 to 31) multiplexed and propagated in the CORE power domain (CONTROL_DEBOBS_FINAL_MUX_SEL[i] SELECT = 0b1).

These options do not apply to the hardware observability signals, hw_dbg i (where i = 0 to 31), which are muxed in the WKUP power domain (CONTROL_DEBOBS_FINAL_MUX_SEL[i] SELECT = 0x0).

18.4.11.3 Observability Signals Multiplexing at General Core/Wake-Up Control Level

Most of the observability multiplexers (MACRO group modules/DPLLs/sDMA associated) are configurable in the General Core Control Module, which is part of the switchable CORE power domain. Signal multiplexers are also instantiated in the general wakeup control module (CM1/PRM dedicated), which is part of the WKUP power domain. The CONTROL_DEBOBS_FINAL_MUX_SEL[31:0] SELECT bit field, instantiated in the CORE power domain, selects a signal to be observed between the outputs at the CORE and WKUP multiplexing levels. A bit from this register set to 1 selects to route a signal from the CORE power domain to a certain po_hw_dbgn (where n = 0…31) line, and when the bit is set to 0, selects to route a signal from the WKUP power domain to the same line. The output of this top-level multiplexing is further passed to the padconfiguration muxing I/O level within device control module boundaries.

NOTE: Although the CONTROL_DEBOBS_FINAL_MUX_SEL observability control register is in the CORE power domain, its value is retentioned before the device goes into off mode. Thus, the preserved value is used to control the final observability muxer in the WKUP power domain, even when the PD_CORE supply in the device is switched off. Because the hw_dbg i signals, which are propagated in the CORE power domain, are not available in off mode, the value of CONTROL_DEBOBS_FINAL_MUX_SEL[i] SELECT = 0b1 (where i = 0 to 31) in this case means that the hw_dbg i signal is not available at output.

The module and view-channel selection/reduction layer in the CORE domain is configured through the 4-bit field MODE in the 32 × 32-bit registers CONTROL_CORE_CONF_DEBUG_SEL_TST_0 through CONTROL_CORE_CONF_DEBUG_SEL_TST_31. The following modules can be selected as source of observability signals: Cortex-A9 MPU subsystem, IVA-HD, display subsystem , CM2, and ABE (MACRO signal sources).

Some of the CONTROL_CORE_CONF_DEBUG_SEL_TST registers are responsible for selection of sDMA view channels, different DPLL clock view channels, and other signal view channels.

- 3 x DPLL clockout signal view channels
- 7 x DPLL (other than clkout signal) view channels
- 5 x sDMA signal view channels
- 3 x additional clockout view channels monitoring the hwobs_coredivider_clkout3, hwobs_perdivider_clkout4, and hwobs_pd_l4_per_per32k_gfclk signals.

Table 18-21 summarizes the internal signals multiplexing schema for each of the 32 CONTROL_CORE_CONF_DEBUG_SEL_TST registers.

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Table 18-21. CORE Power Domain Observability Signals Multiplexing

REG_NAME	REG_ID	REG_OFFSET	REG_RESET	INPUT0	INPUT1	INPUT2	INPUT3	INPUT4	INPUT5	INPUT6	INPUT7	INPUT8	INPUT9	INPUT10	INPUT11	INPUT12
Reg Name	Reg	Reg	Mode value upon POR	Mode 0x0	Mode 0x1	Mode 0x2	Mode 0x3	Mode 0x4	Mode 0x5	Mode 0x6	Mode 0x7	Mode 0x8	Mode 0x9	Mode 0xA	Mode 0xB	Mode 0xC
CONTROL_CORE_CONF_DEBUG_SEL_TST_0	0	0x0480	0x0	hwobs_int_mpu(0)	clk_view_0	Reserved	Reserved	This information is not available in the public domain.	hwobs_int_cm2(0)	hwobs_int_ivahd(0)	Reserved	hwobs_int_abe(0)	This information is not available in the public domain.	Reserved	Reserved	This information is not available in the public domain.
CONTROL_CORE_CONF_DEBUG_SEL_TST_1	1	0x0484	0x0	hwobs_int_mpu(1)	clk_view_1	Reserved	Reserved	Reserved	hwobs_int_cm2(1)	hwobs_int_ivahd(1)	Reserved	hwobs_int_abe(1)	This information is not available in the public domain.	Reserved	Reserved	N/A
CONTROL_CORE_CONF_DEBUG_SEL_TST_2	2	0x0488	0x0	hwobs_int_mpu(2)	clk_view_2	Reserved	Reserved	Reserved	hwobs_int_cm2(2)	hwobs_int_ivahd(2)	Reserved	hwobs_int_abe(2)	This information is not available in the public domain.	Reserved	Reserved	N/A
CONTROL_CORE_CONF_DEBUG_SEL_TST_3	3	0x048C	0x0	hwobs_int_mpu(3)	dpll_freqlock	Reserved	Reserved	Reserved	hwobs_int_cm2(3)	hwobs_int_ivahd(3)	Reserved	hwobs_int_abe(3)	This information is not available in the public domain.	Reserved	Reserved	N/A
CONTROL_CORE_CONF_DEBUG_SEL_TST_4	4	0x0490	0x0	hwobs_int_mpu(4)	dpll_tinitz	Reserved	Reserved	Reserved	hwobs_int_cm2(4)	hwobs_int_ivahd(4)	Reserved	hwobs_int_abe(4)	This information is not available in the public domain.	Reserved	Reserved	N/A

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Table 18-21. CORE Power Domain Observability Signals Multiplexing (continued)

REG_NAME	REG_ID	REG_OFFSET	REG_RESET	INPUT0	INPUT1	INPUT2	INPUT3	INPUT4	INPUT5	INPUT6	INPUT7	INPUT8	INPUT9	INPUT10	INPUT11	INPUT12
CONTROL_CORE_CONF_DEBUG_SEL_TST_5	5	0x0494	0x0	hwobs_int_mpu(5)	dpll_phaselock	Reserved	Reserved	Reserved	hwobs_int_cm2(5)	hwobs_int_ivahd(5)	Reserved	hwobs_int_abe(5)	This information is not available in the public domain.	Reserved	Reserved	N/A
CONTROL_CORE_CONF_DEBUG_SEL_TST_6	6	0x0498	0x0	hwobs_int_mpu(6)	Reserved	Reserved	Reserved	Reserved	hwobs_int_cm2(6)	hwobs_int_ivahd(6)	Reserved	hwobs_int_abe(6)	This information is not available in the public domain.	Reserved	Reserved	N/A
CONTROL_CORE_CONF_DEBUG_SEL_TST_7	7	0x049C	0x0	hwobs_int_mpu(7)	dpll_tenable	sdma_req_view_0	Reserved	Reserved	hwobs_int_cm2(7)	hwobs_int_ivahd(7)	Reserved	hwobs_int_abe(7)	This information is not available in the public domain.	Reserved	Reserved	N/A
CONTROL_CORE_CONF_DEBUG_SEL_TST_8	8	0x04A0	0x0	hwobs_int_mpu(8)	dpll_tenablediv	sdma_req_view_1	Reserved	Reserved	hwobs_int_cm2(8)	hwobs_int_ivahd(8)	Reserved	hwobs_int_abe(8)	This information is not available in the public domain.	Reserved	Reserved	N/A
CONTROL_CORE_CONF_DEBUG_SEL_TST_9	9	0x04A4	0x0	hwobs_int_mpu(9)	dpll_bypassack	sdma_req_view_2	Reserved	Reserved	hwobs_int_cm2(9)	hwobs_int_ivahd(9)	Reserved	hwobs_int_abe(9)	This information is not available in the public domain.	Reserved	hwobs_dssvenctvdetgp[1]	N/A
CONTROL_CORE_CONF_DEBUG_SEL_TST_10	10	0x04A8	0x0	hwobs_int_mpu(10)	dpll_idle	sdma_req_view_3	Reserved	Reserved	hwobs_int_cm2(10)	hwobs_int_ivahd(10)	Reserved	hwobs_int_abe(10)	This information is not available in the public domain.	Reserved	hwobs_dssdacpwrdndaczcvbs_y[1]	N/A

(1) The (VDAC) function is not supported.

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Table 18-21. CORE Power Domain Observability Signals Multiplexing (continued)

REG_NAME	REG_ID	REG_OFFSET	REG_RESET	INPUT0	INPUT1	INPUT2	INPUT3	INPUT4	INPUT5	INPUT6	INPUT7	INPUT8	INPUT9	INPUT10	INPUT11	INPUT12
CONTROL_CORE_CONF_DEBUG_SEL_TST_11	11	0x04AC	0x0	hwobs_int_mpu(11)	hwobs_hsusbotg_sofpulse	sdma_req_view_all	Reserved	Reserved	hwobs_int_cm2(11)	hwobs_int_ivahd(11)	Reserved	hwobs_int_abe(11)	This information is not available in the public domain.	Reserved	hwobs_dssdacpwrdndaczchroma[1]	N/A
CONTROL_CORE_CONF_DEBUG_SEL_TST_12	12	0x04B0	0x0	hwobs_int_mpu(12)	Reserved	hwobs_corediviider_clkout3	Reserved	Reserved	hwobs_int_cm2(12)	hwobs_int_ivahd(12)	Reserved	hwobs_int_abe(12)	This information is not available in the public domain.	Reserved	hwobs_dssdacpwrdndaccvbs[1]	N/A
CONTROL_CORE_CONF_DEBUG_SEL_TST_13	13	0x04B4	0x0	hwobs_int_mpu(13)	Reserved	hwobs_perdiviider_clkout4	Reserved	Reserved	hwobs_int_cm2(13)	hwobs_int_ivahd(13)	Reserved	hwobs_int_abe(13)	This information is not available in the public domain.	Reserved	hwobs_dssdacpwrdnbgz[1]	N/A
CONTROL_CORE_CONF_DEBUG_SEL_TST_14	14	0x04B8	0x0	hwobs_int_mpu(14)	Reserved	hwobs_pd_l4_per_per32k_gfclk	Reserved	Reserved	hwobs_int_cm2(14)	hwobs_int_ivahd(14)	Reserved	hwobs_int_abe(14)	This information is not available in the public domain.	Reserved	Reserved	N/A
CONTROL_CORE_CONF_DEBUG_SEL_TST_15	15	0x04BC	0x0	hwobs_int_mpu(15)	Reserved	0	Reserved	Reserved	hwobs_int_cm2(15)	hwobs_int_ivahd(15)	Reserved	hwobs_int_abe(15)	This information is not available in the public domain.	Reserved	Reserved	N/A
CONTROL_CORE_CONF_DEBUG_SEL_TST_16	16	0x04C0	0x0	hwobs_int_mpu(16)	Reserved	0	Reserved	Reserved	hwobs_int_cm2(16)	hwobs_int_ivahd(16)	Reserved	hwobs_int_abe(16)	This information is not available in the public domain.	Reserved	Reserved	N/A

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Table 18-21. CORE Power Domain Observability Signals Multiplexing (continued)

REG_NAME	REG_ID	REG_OFFSET	REG_RESET	INPUT0	INPUT1	INPUT2	INPUT3	INPUT4	INPUT5	INPUT6	INPUT7	INPUT8	INPUT9	INPUT10	INPUT11	INPUT12
CONTROL_CORE_CONF_DEBUG_SEL_TST_17	17	0x04C4	0x0	hwobs_int_mpu(17)	Reserved	0	Reserved	Reserved	hwobs_int_cm2(17)	hwobs_int_ivahd(17)	Reserved	hwobs_int_abe(17)	This information is not available in the public domain.	Reserved	Reserved	N/A
CONTROL_CORE_CONF_DEBUG_SEL_TST_18	18	0x04C8	0x0	hwobs_int_mpu(18)	Reserved	0	Reserved	Reserved	hwobs_int_cm2(18)	hwobs_int_ivahd(18)	Reserved	hwobs_int_abe(18)	This information is not available in the public domain.	Reserved	Reserved	N/A
CONTROL_CORE_CONF_DEBUG_SEL_TST_19	19	0x04CC	0x0	hwobs_int_mpu(19)	Reserved	0	Reserved	Reserved	hwobs_int_cm2(19)	hwobs_int_ivahd(19)	Reserved	hwobs_int_abe(19)	This information is not available in the public domain.	Reserved	Reserved	N/A
CONTROL_CORE_CONF_DEBUG_SEL_TST_20	20	0x04D0	0x0	hwobs_int_mpu(20)	Reserved	0	Reserved	Reserved	hwobs_int_cm2(20)	hwobs_int_ivahd(20)	Reserved	hwobs_int_abe(20)	This information is not available in the public domain.	Reserved	Reserved	N/A
CONTROL_CORE_CONF_DEBUG_SEL_TST_21	21	0x04D4	0x0	hwobs_int_mpu(21)	Reserved	0	Reserved	Reserved	hwobs_int_cm2(21)	hwobs_int_ivahd(21)	Reserved	hwobs_int_abe(21)	This information is not available in the public domain.	Reserved	N/A	N/A
CONTROL_CORE_CONF_DEBUG_SEL_TST_22	22	0x04D8	0x0	hwobs_int_mpu(22)	Reserved	0	Reserved	Reserved	hwobs_int_cm2(22)	hwobs_int_ivahd(22)	Reserved	hwobs_int_abe(22)	This information is not available in the public domain.	Reserved	N/A	N/A

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Table 18-21. CORE Power Domain Observability Signals Multiplexing (continued)

REG_NAME	REG_ID	REG_OFFSET	REG_RESET	INPUT0	INPUT1	INPUT2	INPUT3	INPUT4	INPUT5	INPUT6	INPUT7	INPUT8	INPUT9	INPUT10	INPUT11	INPUT12
CONTROL_CORE_CONF_DEBUG_SEL_TST_23	23	0x04DC	0x0	hwobs_int_mpu(23)	Reserved	0	Reserved	Reserved	hwobs_int_cm2(23)	hwobs_int_ivahd(23)	Reserved	hwobs_int_abe(23)	This information is not available in the public domain.	Reserved	N/A	N/A
CONTROL_CORE_CONF_DEBUG_SEL_TST_24	24	0x04E0	0x0	hwobs_int_mpu(24)	Reserved	0	Reserved	Reserved	hwobs_int_cm2(24)	hwobs_int_ivahd(24)	Reserved	hwobs_int_abe(24)	This information is not available in the public domain.	Reserved	N/A	N/A
CONTROL_CORE_CONF_DEBUG_SEL_TST_25	25	0x04E4	0x0	hwobs_int_mpu(25)	Reserved	0	Reserved	Reserved	hwobs_int_cm2(25)	hwobs_int_ivahd(25)	Reserved	hwobs_int_abe(25)	This information is not available in the public domain.	Reserved	N/A	N/A
CONTROL_CORE_CONF_DEBUG_SEL_TST_26	26	0x04E8	0x0	hwobs_int_mpu(26)	Reserved	0	Reserved	0	hwobs_int_cm2(26)	hwobs_int_ivahd(26)	Reserved	hwobs_int_abe(26)	This information is not available in the public domain.	Reserved	N/A	N/A
CONTROL_CORE_CONF_DEBUG_SEL_TST_27	27	0x04EC	0x0	hwobs_int_mpu(27)	Reserved	0	Reserved	0	hwobs_int_cm2(27)	hwobs_int_ivahd(27)	Reserved	hwobs_int_abe(27)	This information is not available in the public domain.	Reserved	0	sdma_req_view_0
CONTROL_CORE_CONF_DEBUG_SEL_TST_28	28	0x04F0	0x0	hwobs_int_mpu(28)	Reserved	0	Reserved	0	hwobs_int_cm2(28)	hwobs_int_ivahd(28)	Reserved	hwobs_int_abe(28)	This information is not available in the public domain.	Reserved	0	sdma_req_view_1

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Table 18-21. CORE Power Domain Observability Signals Multiplexing (continued)

REG_NAME	REG_ID	REG_OFFSET	REG_RESET	INPUT0	INPUT1	INPUT2	INPUT3	INPUT4	INPUT5	INPUT6	INPUT7	INPUT8	INPUT9	INPUT10	INPUT11	INPUT12
CONTROL_CORE_CONF_DEBUG_SEL_TST_29	29	0x04F4	0x0	hwobs_int_mpu(29)	Reserved	0	Reserved	0	hwobs_int_cm2(29)	hwobs_int_ivahd(29)	Reserved	hwobs_int_abe(29)	This information is not available in the public domain.	Reserved	0	sdma_req_view_2
CONTROL_CORE_CONF_DEBUG_SEL_TST_30	30	0x04F8	0x0	hwobs_int_mpu(30)	Reserved	0	Reserved	0	hwobs_int_cm2(30)	hwobs_int_ivahd(30)	Reserved	hwobs_int_abe(30)	This information is not available in the public domain.	Reserved	0	sdma_req_view_3
CONTROL_CORE_CONF_DEBUG_SEL_TST_31	31	0x04FC	0x0	hwobs_int_mpu(31)	Reserved	0	Reserved	0	hwobs_int_cm2(31)	hwobs_int_ivahd(31)	Reserved	hwobs_int_abe(31)	This information is not available in the public domain.	Reserved	0	sdma_req_view_all

A third 1:N selection layer is applied over several signals to route them one-at-a-time to a certain view channel output:

- The CONTROL_CONF_CLK_SEL0[2:0] MULT through CONTROL_CONF_CLK_SEL2[2:0] MULT bit fields control the multiplexing of DPLL CLKOUT signals over three parallel DPLL clockout view channels. The signal source of a certain view channel can be selected to be one of six DPLLs in the device:
  - CORE DPLL
  - ABE DPLL
  - PER DPLL
  - DSI1 DPLL
  - DSI2 DPLL
  - USB DPLL
- The register bit fields associated with the seven different DPLL signal view channels are summarized in Table 18-22. Again, the 3-bit MULT bit field in each of the seven registers makes it possible to choose the source of the DPLL signal to be one of the following device DPLLs:
  - CORE DPLL
  - ABE DPLL
  - PER DPLL
  - DSI1 DPLL

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  - DSI2 DPLL
  - USB DPLL

- There are four independent sDMA request view channels, each of which has a dedicated register (CONTROL_CONF_SDMA_REQ_SEL0 through CONTROL_CONF_SDMA_REQ_SEL3) with a 7-bit MULT bit field to select one from 127 possible sDMA request signals for observation purposes. For more information, see Chapter 16, *sDMA Controller*. The fifth channel, sdma_req_view_all, is acquired by applying logical AND reduction over the four currently selected sDMA view channel output signals.
- The General Core observability logic input (hwobs_pd_l4_per_per32k_gfclk) is tied to the PRM output observability signal (pd_l4_per_per_32k_gfclk). The pd_l4_per_per_32k_gfclk signal corresponds to the hardware gated in the L4_PER clock domain clock (PER_32K_FCLK), which is directly sourced by the SCRM clock (32K_FCLK). For more information, see Section 3.6.3.1, *PRM Clock Source*, in Chapter 3, *Power, Reset, and Clock Management*. The PER_32K_FCLK and 32K_FCLK clocks are also multiplexed for observability in the WKUP domain when the PRCM.PRM_DEBUG_CFG[6:0] bit field is set to 0x6C. The observable signals are devfsm_l0.clk and gat_per_32k_gfclk_l0.clkGated, respectively. For more information, see Table 18-41, *PRM Observable Signals*.
- The General Core observability logic input, hwobs_coredivider_clkout3, is tied to the Core DPLL observability output, CLK_FUNC_1_0_3, which is a direct (nongated, nondivided) version of the CORE DPLL clock output , CLKOUTX2_M3. For more information, see Section 3.6.3.5, *DPLL_CORE Description*, in Chapter 3, *Power, Reset, and Clock Management*.
- The General Core observability logic input, hwobs_perdivider_clkout4, is tied to the Core DPLL observability output, CLK_FUNC_1_0_4, which is a direct (nongated, nondivided) version of the PER DPLL clock output, CLKOUTX2_M4. For more information, see Section 3.6.3.4, *DPLL_PER Description*, in Chapter 3, *Power, Reset, and Clock Management*.

Table 18-22 lists the DPLL signal observability controls.

Table 18-22. DPLL Signal Observability Controls

Feature	Type	Register/Bit Field/Observability Control	Description
Different domain DPLL freqlock observability	Control	CONTROL_CONF_DPLL_FREQLOCK_SEL[2:0] MULT	Selects DPLL freqlock view channel (1:8)
Different domain DPLL phaselock observability	Control	CONTROL_CONF_DPLL_PHASELOCK_SEL[2:0] MULT	Selects DPLL phaselock view channel (1:8)
Different domain DPLL tinitz observability	Control	CONTROL_CONF_DPLL_TINITZ_SEL[2:0] MULT	Selects to observe DPLL tinitzview channel (1:8)
Different domain DPLL tenable observability	Control	CONTROL_CONF_DPLL_TENABLE_SEL[2:0] MULT	Selects to observe DPLL tenableview channel (1:8)
Different domain DPLL tenablediv observability	Control	CONTROL_CONF_DPLL_TENABLEDIV_SEL[2:0] MULT	Selects to observe DPLL tenabledivview channel (1:8)
Different domain DPLL bypassack observability	Control	CONTROL_CONF_DPLL_BYPASSACK_SEL[2:0] MULT	Selects to observe DPLL bypassackview channel (1:8)
Different domain DPLL idle observability	Control	CONTROL_CONF_DPLL_IDLE_SEL[2:0] MULT	Selects to observe DPLL idleview channel (1:8)

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NOTE: Features configured in the following registers are limited to hardware observability signals, hw_dbg i (where i = 0 to 31), multiplexed and propagated in the CORE power domain (CONTROL_DEBOBS_FINAL_MUX_SEL[i] SELECT = 0b1):

- CONTROL_CORE_CONF_DEBUG_SEL_TST_0 through CONTROL_CORE_CONF_DEBUG_SEL_TST_31
- CONTROL_CONF_CLK_SEL0[2:0] MULT through CONTROL_CONF_CLK_SEL2[2:0] MULT
- CONTROL_CONF_SDMA_REQ_SEL0 through CONTROL_CONF_SDMA_REQ_SEL3
- CONTROL_CONF_DPLL_FREQLOCK_SEL
- CONTROL_CONF_DPLL_TINITZ_SEL
- CONTROL_CONF_DPLL_PHASELOCK_SEL
- CONTROL_CONF_DPLL_TENABLE_SEL
- CONTROL_CONF_DPLL_TENABLEDIV_SEL
- CONTROL_CONF_DPLL_BYPASSACK_SEL
- CONTROL_CONF_DPLL_IDLE_SEL

These options are not applicable to hardware observability signals, hw_dbg i (where i = 0 to 31), which at the general control module level are muxed in the WKUP power domain (CONTROL_DEBOBS_FINAL_MUX_SEL[i] SELECT = 0b0).

The CONTROL_WKUP_CONF_DEBUG_SEL_TST_i[0] MODE bit (where i = 0…31) provides the option to choose between observation of power and reset manager signals in the device or observation of signals related to CM1. If CONTROL_WKUP_CONF_DEBUG_SEL_TST_i[0] =0b1, the hwobs_int_prm_i signal is selected. Otherwise, the hwobs_int_cm1_i signal is output.

NOTE: The CM1 and PRM observable signals are multiplexed in the WKUP power domain.

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18.4.11.4 Observability Signals Multiplexing at Device Control Module Level

The pads used for the hardware debug must be properly configured by selecting the hardware debug function (hw_dbgn) of the pad.

18.4.11.4.1 Observability Signals Muxed on Pads in Core Power Domain

To map the hw_dbg0 through hw_dbg19 signals to their associated external device pads in the CORE power domain, set the related MUXMODE bit fields within the CONTROL_CORE_PAD0_SYS_BOOT5_PAD1_DPM_EMU0 through CONTROL_CORE_PAD0_DPM_EMU19_PAD1_CSI22_DX2 padconfiguration registers to 0b110 (Mode 6). To make the remaining signals (hw_dbg20 through the hw_dbg31) available at their corresponding device pads in the CORE power domain, set the MUXMODE bit fields within the CONTROL_CORE_PAD0_CAM_GLOBALRESET_PAD1_USBB1_ULPITLL_CLK through CONTROL_CORE_PAD0_USBB1_ULPITLL_DAT7_PAD1_USBB1_HSIC_DATA padconfiguration registers to 0b110 (Mode 6).

For more information, see Table 18-10, *Device Core Control Module Pad Configuration Register Fields*.

For more information about hardware observability configuration, see Table 18-109, *ACTIVE PADS Configuration Points*.

NOTE: The hw_dbg i signals (where i = 0 to 31), which are multiplexed and propagated in the CORE power domain, are not visible when the device is set in off mode (PD_CORE supply switched off).

18.4.11.4.2 Observability Signals Muxed on Pads in WKUP Power Domain

To have hw_dbg1 through hw_dbg13 signals multiplexed on the WKUP power domain pads, set MuxMode = 0x6 in the following SYSCTRL_PADCONF_WKUP registers:

- CONTROL_WKUP_PAD0_GPIO_WK0_PAD1_GPIO_WK1 through CONTROL_WKUP_PAD0_GPIO_WK2_PAD1_GPIO_WK3[31:16] to have the hw_dbg1–hw_dbg4 signals output on the gpio_wk0–gpio_wk3 device pads, respectively
- CONTROL_WKUP_PAD0_GPIO_WK4_PAD1_SR_SCL[15:0] to have the hw_dbg5 signal output on the gpio_wk4 device pad
- CONTROL_WKUP_PAD0_FREF_CLK0_OUT_PAD1_FREF_CLK3_REQ through CONTROL_WKUP_PAD0_FREF_CLK3_OUT_PAD1_FREF_CLK4_REQ to have the hw_dbg6–hw_dbg9 signal output on the fref_clk0_out, fref_clk3_req, fref_clk3_out, and fref_clk4_req device pads, respectively
- CONTROL_WKUP_PAD0_FREF_CLK4_OUT_PAD1_SYS_32K[15:0] to have the hw_dbg10 signal output on the fref_clk4_out device pad
- CONTROL_WKUP_PAD0_SYS_PWR_REQ_PAD1_SYS_PWRON_RESET_OUT[31:16] to have the hw_dbg11 signal output on the sys_pwron_reset_out device pad
- CONTROL_WKUP_PAD0_SYS_BOOT6_PAD1_SYS_BOOT7 to have the hw_dbg12 and hw_dbg13 signals output on the sys_boot6 and sys_boot7 device pads, respectively

The hw_dbg0 signal is available on the sys_pwron_reset_out pad in WKUP domain, through setting MuxMode=0x5 in theCONTROL_WKUP_PAD0_SYS_PWR_REQ_PAD1_SYS_PWRON_RESET_OUT[31:16] register. Because hw_dbg11 (MuxMode=0x6) and hw_dbg0 (MuxMode=0x5) are muxed on the same pad - sys_pwron_reset_out, user should make choice between the two observable signals in WKUP domain

See Table 18-9, *Device Wakeup Control Module Pad Configuration Register Fields* for more information.

See Table 18-109, *ACTIVE PADS Configuration Points*, for more details on hardware observability configuration.

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NOTE: If multiplexed on corresponding device pads in the WKUP power domain, the hw_dbg i signals (where i = 0 to 31), which are multiplexed and propagated in the WKUP power domain, can be observed even if the device goes into off mode.

18.4.11.5 Observability Signals Sourced at Module Level

Observable signals coming from within different device subsystems are mapped to general core control and general wakeup control observability inputs. Additional multiplexing is also implemented inside some of the observable modules (see Figure 18-22, *Overview of the Hardware Observability Functionality)*.

18.4.11.5.1 Dual Cortex-A9 Subsystem Observable Signals

Table 18-23 through Table 18-31 list the Cortex-A9 MPU subsystem observable signals available in 12 functional multiplexing modes. The mode is selected at the general core control module level by programming the CONTROL_DEBOBS_MMR_MPU[3:0] SELECT bit field. The SELECT values in range (0xC–0xF) are reserved for future use.

Table 18-23. Observability Signals Multiplexing at Cortex-A9 MPU Subsystem Level – Mode 0

CONTROL_DEBOBS_MMR_MPU[3:0] SELECT = 0b0000			
SYSCTRL_GENERAL_CORE Observability Inputs Tied to Signals Inside Cortex-A9 MPU Subsystem	**Cortex-A9 MPU Subsystem Observable Signals Mapped to SYSCTRL_GENERAL_CORE Observability Inputs**	**Signal Description**	**Logical Value Meaning**
hwobs_int_mpu[31:24]	Intr[7:0]	hwobs_int_mpu(31) down to hwobs_int_mpu(24)correspond to Cortex-A9 MPU subsystem interrupt requests on linesMA_IRQ_7 down to MA_IRQ_0. For more information, see Section 17.3.2, *Interrupt Requests to the Cortex-A9 MPU Interrupt Controller*.	–
hwobs_int_mpu[23]	mpu_rstn	MPU warm reset	–
hwobs_int_mpu[22]	mpu_pwron_rstn	MPU power-on reset	–
hwobs_int_mpu[21:15]	Reserved	-	–
hwobs_int_mpu[14]	CPU0 Standby	Standby request asserted from CPU0 L1STBY ctrl to the local PRM wrapper	
hwobs_int_mpu[13]	CPU1 Standby	Standby request asserted from CPU1 L1STBY ctrl to the local PRM wrapper	
hwobs_int_mpu[12]	DPLLPhaseLock	Module in phase lock condition	Active high
hwobs_int_mpu[11]	DPLL Clock / 16	MPU DPLL clock divided by 16	
hwobs_int_mpu[10]	DPLLFreqLock	Module in freqlock condition	
hwobs_int_mpu[9]	PRESETN	Debug reset	
hwobs_int_mpu[8]	ATRESETN	Trace reset	
hwobs_int_mpu[7]	DPLLInitZ	–	
hwobs_int_mpu[6:5]	Reserved	–	
hwobs_int_mpu[4]	nCPURESET[0]	Cortex-A9 CPU reset (per CPU0)	
hwobs_int_mpu[3]	PIDPLLIDLE	Observes PLL to Idle mode setting. Sets CLKOUT to the bypass mode clock as selected by ULOWCLKEN.	
hwobs_int_mpu[2]	PROFILING_EVENT2PRM[2:0]	Output to PRM for profiling local CPU0 power status	See Table 18-27 for signal descriptions.
hwobs_int_mpu[1]			
hwobs_int_mpu[0]			

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Table 18-24. Observability Signals Multiplexing at Cortex-A9 MPU Subsystem Level – Mode 1

CONTROL_DEBOBS_MMR_MPU[3:0] SELECT = 0b0001			
SYSCTRL_GENERAL_CORE Observability Inputs Tied to Signals Inside Cortex-A9 MPU Subsystem	**Cortex-A9 MPU Subsystem Observable Signals Mapped to SYSCTRL_GENERAL_CORE Observability Inputs**	**Signal Description**	**Logical Value Meaning**
hwobs_int_mpu[31:10]	Reserved	–	–
hwobs_int_mpu[9]	WDTRESET	Watchdog status reset	–
hwobs_int_mpu[8]	aclk_abe_final_phase	Last Aclk pulse in period of the abe_clk generated at MPU subsystem level, used for ABE interface	–
hwobs_int_mpu[7]	aclk_l3_final_phase	Last Aclk pulse in period of the l3_clk generated at MPU subsystem level, used for L3 interface	–
hwobs_int_mpu[6:5]	Reserved	–	–
hwobs_int_mpu[4]	nCPURESET[1]	Cortex-A9 CPU Reset (per CPU1)	
hwobs_int_mpu[3]	ARM_FCLK / 16	Cortex-A9 CPU0/CPU1 input clock divided by 16	
hwobs_int_mpu[2]	PROFILING_EVENT2PRM[5:3]	Output to PRM for profiling local CPU0 power status	See Table 18-27 for signal descriptions.
hwobs_int_mpu[1]			
hwobs_int_mpu[0]			

Table 18-25. Observability Signals Multiplexing at Cortex-A9 MPU Subsystem Level – Mode 2

CONTROL_DEBOBS_MMR_MPU[3:0] SELECT = 0b0010			
SYSCTRL_GENERAL_CORE Observability Inputs tied to Signals Inside Cortex-A9 MPU Subsystem	**Cortex-A9 MPU Subsystem Observable Signals Mapped to SYSCTRL_GENERAL_CORE Observability Inputs**	**Signal Description**	**Logical Value Meaning**
hwobs_int_mpu[27]	top_mstandby_0	Standby handshake to local PRCM (CPU0)	–
hwobs_int_mpu[26]	top_mwait_0	Standby wake-up handshake for CPU0	
hwobs_int_mpu[25]	top_mwakeup_0	Wake-up request from CPU0	
hwobs_int_mpu[24]	top_mstandby_1	Standby handshake to local PRCM (CPU1)	
hwobs_int_mpu[23]	top_mwait_1	Standby wake-up handshake for CPU1	–
hwobs_int_mpu[22]	top_mwakeup_1	Wake-up request from CPU1	
hwobs_int_mpu[21]	MSTANDBY	Global MStandby handshake to global PRCM	
hwobs_int_mpu[20]	MWAIT	Global MWait handshake to global PRCM	
hwobs_int_mpu[19]	MWAKEUP	Global Mwakeup handshake to global PRCM	
hwobs_int_mpu[18]	EMUASSERTNRESET[0]	Command for assertion of a local reset to CPU Core0	
hwobs_int_mpu[17:8]	Reserved	–	–
hwobs_int_mpu[7]	DPLLInitZ	MPU subsystem DPLL initialization	
hwobs_int_mpu[6]	Aclk / 8	Aclk is equal to ARM_FCLK / 2; thus, clock with frequency ARM_FCLK / 16 is observed.	

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Table 18-25. Observability Signals Multiplexing at Cortex-A9 MPU Subsystem Level – Mode 2 (continued)

CONTROL_DEBOBS_MMR_MPU[3:0] SELECT = 0b0010			
SYSCTRL_GENERAL_CORE Observability Inputs tied to Signals Inside Cortex-A9 MPU Subsystem	**Cortex-A9 MPU Subsystem Observable Signals Mapped to SYSCTRL_GENERAL_CORE Observability Inputs**	**Signal Description**	**Logical Value Meaning**
hwobs_int_mpu[5]	Aclk / 8	Aclk is equal to ARM_FCLK / 2; thus, clock with frequency ARM_FCLK / 16 is observed.	
hwobs_int_mpu[4]	L2_Cache_Ctrl_IDLE	IDLE state of L2-cache controller	
hwobs_int_mpu[3]	ARM_FCLK / 16	Cortex-A9 CPU0/CPU1 input clock divided by 16	
hwobs_int_mpu[2]	PROFILING_EVENT2PRM[8:6]	Output to PRM for profiling local CPU1 power status	See Table 18-27 for signal descriptions.
hwobs_int_mpu[1]			
hwobs_int_mpu[0]			

Table 18-26. Observability Signals Multiplexing at Cortex-A9 MPU Subsystem Level - Mode 3

CONTROL_DEBOBS_MMR_MPU[3:0] SELECT = 0b0011			
SYSCTRL_GENERAL_CORE Observability Inputs Tied to Signals Inside Cortex-A9 MPU Subsystem	**Cortex-A9 MPU Subsystem Observable Signals Mapped to SYSCTRL_GENERAL_CORE Observability Inputs**	**Signal Description**	**Logical Value Meaning**
hwobs_int_mpu[31:16]	Intr[31:16]	hwobs_int_mpu(31) down to hwobs_int_mpu(16) correspond to Cortex-A9 MPU subsystem interrupt requests on line :MA_IRQ_31 down to MA_IRQ_16. For more information, see Section 17.3.2, *Interrupt Requests to the Cortex-A9 MPU Interrupt Controller*.	–
hwobs_int_mpu[15:8]	Intr[15:8]	hwobs_int_mpu(15) down to hwobs_int_mpu(8) correspond to Cortex-A9 MPU subsystem interrupt requests on lines MA_IRQ_15 down to MA_IRQ_8. For more information, see Section 17.3.2, *Interrupt Requests to the Cortex-A9 MPU Interrupt Controller*.	–
hwobs_int_mpu[7]	DPLLInitZ	MPU subsystem DPLL Initialization	–
hwobs_int_mpu[6]	PODPLLBYPASSACK	Bypass status signal	1 o/p clock in bypass
hwobs_int_mpu[5]	PIDPLLTENABLEDIV	Core RegM2/N2 load enable (L-H)	–
hwobs_int_mpu[4]	PIDPLLTENABLE	Core RegM2/N2 load enable (L-H)	–
hwobs_int_mpu[3]	ARM_FCLK / 16	Cortex-A9 CPU0/CPU1 input clock divided by 16.	–
hwobs_int_mpu[2]	PROFILING_EVENT2PRM[11:9]	Output to PRM for profiling local CPU1 power status	See Table 18-27 for signal descriptions.
hwobs_int_mpu[1]			
hwobs_int_mpu[0]			

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The POPROFILING_EVENT2PRM bus signals, observable in modes 0, 1, 2, and 3, monitor the power states of the CPU. There are 6 status bits per Cortex-A9 CPU0 and CPU1, respectively. Table 18-27 describes the encoding of the status bits.

POPROFILING_EVENT2PRM[5:0] are the status bits for CPU0, and POPROFILING_EVENT2PRM[11:6] are the status bits for CPU1.

Table 18-27. CPU0/CPU1 PM Profiling Bus Observable Signals Description

Bit Position (CPU0)	Bit Position (CPU1)	Descriptions
5	11	**Memory in transition** 1'b0 : Memory array power transition complete 1'b1 : Memory array power transition in progress
4:3	10:9	**Memory (L1) State** 2'b00 : OFF 2'b01 : RETENTION 2'b10: Reserved 2'b11: ON
2	8	**Logic in transition** 1'b0 : Power state transition complete 1'b1 : Power state transition in progress
1:0	7:6	**Power State** 2'b00 : Power Domain is OFF. 2'b01 : Power Domain is RETENTION. 2'b10:Power Domain is ON-INACTIVE. 2'b11: Power Domain is ON-ACTIVE.

Table 18-28. Observability Signals Multiplexing at Cortex-A9 MPU Subsystem Level – Mode 4

CONTROL_DEBOBS_MMR_MPU[3:0] SELECT = 0b0100			
SYSCTRL_GENERAL_CORE Observability Inputs Tied to Signals Inside Cortex-A9 MPU Subsystem	**Cortex-A9 MPU Subsystem Observable Signals Mapped to SYSCTRL_GENERAL_CORE Observability Inputs**	**Signal Description**	**Logical Value Meaning**
hwobs_int_mpu[31:24]	Intr[55:48]	hwobs_int_mpu(31) down to hwobs_int_mpu(24) correspond to Cortex-A9 MPU subsystem interrupt requests on lines MA_IRQ_55 down to MA_IRQ_48. For more information, see Section 17.3.2, *Interrupt Requests to the Cortex-A9 MPU Interrupt Controller*.	–
hwobs_int_mpu[23:16]	Intr[47:40]	hwobs_int_mpu(23) down to hwobs_int_mpu(16) correspond to Cortex-A9 MPU subsystem interrupt requests on lines MA_IRQ_47 down to MA_IRQ_40. For more information, see Section 17.3.2, *Interrupt Requests to the Cortex-A9 MPU Interrupt Controller*.	–
hwobs_int_mpu[15:8]	Intr[39:32]	hwobs_int_mpu(15) down to hwobs_int_mpu(8) correspond to Cortex-A9 MPU subsystem interrupt requests on lines MA_IRQ_39 down to MA_IRQ_32. For more information, see Section 17.3.2, *Interrupt Requests to the Cortex-A9 MPU Interrupt Controller*.	–

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Table 18-28. Observability Signals Multiplexing at Cortex-A9 MPU Subsystem Level – Mode 4 (continued)

CONTROL_DEBOBS_MMR_MPU[3:0] SELECT = 0b0100			
SYSCTRL_GENERAL_CORE Observability Inputs Tied to Signals Inside Cortex-A9 MPU Subsystem	**Cortex-A9 MPU Subsystem Observable Signals Mapped to SYSCTRL_GENERAL_CORE Observability Inputs**	**Signal Description**	**Logical Value Meaning**
hwobs_int_mpu[7]	PIDPLLIDLE	Observes PLL to Idle mode setting. Sets CLKOUT to the bypass mode clock as selected by ULOWCLKEN	1: MPU subsystem DPLL is set to idle mode.
hwobs_int_mpu[6]	DPLLRWRCK	–	–
hwobs_int_mpu[5]	DPLLCLKOUT	MPU subsystem DPLL clockout	–
hwobs_int_mpu[4]	EMUASSERTNRESET[1]	Command for assertion of a local reset to CPU Core1	–
hwobs_int_mpu[3]	ARM_FCLK / 16	Cortex-A9 CPU0 / CPU1 input clock divided by 16	–
hwobs_int_mpu[2]	LPRM_EMU_i/f CPU0[2:0]	Latch Reset Bus Ack	–
hwobs_int_mpu[1]		Force Active Ack	
hwobs_int_mpu[0]		InhibitSleep Ack	

Table 18-29. Observability Signals Multiplexing at Cortex-A9 MPU Subsystem Level – Mode 5

CONTROL_DEBOBS_MMR_MPU[3:0] SELECT = 0b0101			
SYSCTRL_GENERAL_CORE Observability Inputs Tied to Signals Inside Cortex-A9 MPU Subsystem	**Cortex-A9 MPU Subsystem Observable Signals Mapped to SYSCTRL_GENERAL_CORE Observability Inputs**	**Signal Description**	**Logical Value Meaning**
hwobs_int_mpu[31:16]	Intr[79:64]	hwobs_int_mpu(31) down to hwobs_int_mpu(16) correspond to Cortex-A9 MPU subsystem interrupt requests on lines MA_IRQ_79 down to MA_IRQ_64 For more information, see Section 17.3.2, *Interrupt Requests to the Cortex-A9 MPU Interrupt Controller*.	–
hwobs_int_mpu[15:8]	Intr[63:56]	hwobs_int_mpu(15) down to hwobs_int_mpu(8) correspond to Cortex-A9 MPU subsystem interrupt requests on lines MA_IRQ_63 down to MA_IRQ_56 For more information, see Section 17.3.2, *Interrupt Requests to the Cortex-A9 MPU Interrupt Controller*.	–
hwobs_int_mpu[7:4]	Reserved	–	–
hwobs_int_mpu[3]	ARM_FCLK / 16	Cortex-A9 CPU0 / CPU1 input clock divided by 16	–
hwobs_int_mpu[2]	LPRM_EMU_i/f CPU0[5:3]	CPU0 EMUWAITINRESET	–
hwobs_int_mpu[1]		CPU0 EMURELEASEFROMWIR	–
hwobs_int_mpu[0]		CPU0 EMUBLOCKRESET	–

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Table 18-30. Observability Signals Multiplexing at Cortex-A9 MPU Subsystem Level – Mode 6

CONTROL_DEBOBS_MMR_MPU[3:0] SELECT = 0b0110			
SYSCTRL_GENERAL_CORE Observability Inputs Tied to Signals Inside Cortex-A9 MPU Subsystem	**Cortex-A9 MPU Subsystem Observable Signals Mapped to SYSCTRL_GENERAL_CORE Observability Inputs**	**Signal Description**	**Logical Value Meaning**
hwobs_int_mpu[31:24]	Intr[103:96]	hwobs_int_mpu(31) down to hwobs_int_mpu(24) correspond to Cortex-A9 MPU subsystem interrupt requests on lines MA_IRQ_103 down to MA_IRQ_96 For more information, see Section 17.3.2, *Interrupt Requests to the Cortex-A9 MPU Interrupt Controller*.	–
hwobs_int_mpu[23:16]	Intr[95:88]	hwobs_int_mpu(23) down to hwobs_int_mpu(16) correspond to Cortex-A9 MPU subsystem interrupt requests on line :MA_IRQ_95 down to MA_IRQ_88 For more information, see Section 17.3.2, *Interrupt Requests to the Cortex-A9 MPU Interrupt Controller*.	–
hwobs_int_mpu[15:8]	Intr[87:80]	hwobs_int_mpu(15) down to hwobs_int_mpu(8) correspond to Cortex-A9 MPU subsystem interrupt requests on lines MA_IRQ_87 down to MA_IRQ_80 For more information, see Section 17.3.2, *Interrupt Requests to the Cortex-A9 MPU Interrupt Controller*.	–
hwobs_int_mpu[7:5]	Reserved	–	–
hwobs_int_mpu[4]	DPLLBYPASS	MPU DPLL bypass command	–
hwobs_int_mpu[3]	ARM_FCLK / 16	Cortex-A9 CPU0 / CPU1 input clock divided by 16	–
hwobs_int_mpu[2]	LPRM_EMU_i/f CPU1[2:0]	Latch Reset Bus Ack	–
hwobs_int_mpu[1]		Force Active Ack	–
hwobs_int_mpu[0]		InhibitSleep Ack	–

Table 18-31. Observability Signals Multiplexing at Cortex-A9 MPU Subsystem Level – Mode 7

CONTROL_DEBOBS_MMR_MPU[3:0] SELECT = 0b0111			
SYSCTRL_GENERAL_CORE Observability Inputs Tied to Signals Inside Cortex-A9 MPU Subsystem	**Cortex-A9 MPU Subsystem Observable Signals Mapped to SYSCTRL_GENERAL_CORE Observability Inputs**	**Signal Description**	**Logical Value Meaning**
hwobs_int_mpu[31:16]	Intr[127: 112]	hwobs_int_mpu(31) down to hwobs_int_mpu(16) correspond to Cortex-A9 MPU subsystem interrupt requests on lines MA_IRQ_127 down to MA_IRQ_112 For more information, see Section 17.3.2, *Interrupt Requests to the Cortex-A9 MPU Interrupt Controller*.	–

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Table 18-31. Observability Signals Multiplexing at Cortex-A9 MPU Subsystem Level – Mode 7 (continued)

CONTROL_DEBOBS_MMR_MPU[3:0] SELECT = 0b0111			
SYSCTRL_GENERAL_CORE Observability Inputs Tied to Signals Inside Cortex-A9 MPU Subsystem	**Cortex-A9 MPU Subsystem Observable Signals Mapped to SYSCTRL_GENERAL_CORE Observability Inputs**	**Signal Description**	**Logical Value Meaning**
hwobs_int_mpu[15:8]	Intr[111: 104]	hwobs_int_mpu(15) down to hwobs_int_mpu(8) correspond to Cortex-A9 MPU subsystem interrupt requests on lines MA_IRQ_111 down to MA_IRQ_104 For more information, see Section 17.3.2, *Interrupt Requests to the Cortex-A9 MPU Interrupt Controller*.	–
hwobs_int_mpu[7:4]	Reserved	–	–
hwobs_int_mpu[3]	ARM_FCLK / 16	Cortex-A9 CPU0 / CPU1 input clock divided by 16	–
hwobs_int_mpu[2]	LPRM_EMU_i/f CPU1[5:3]	CPU1 EMUWAITINRESET	–
hwobs_int_mpu[1]		CPU1 EMURELEASEFROMWIR	–
hwobs_int_mpu[0]		CPU1 EMUBLOCKRESET	–

Table 18-32. Observability Signals Multiplexing at Cortex-A9 MPU Subsystem Level – Mode 8

CONTROL_DEBOBS_MMR_MPU[3:0] SELECT = 0b1000			
SYSCTRL_GENERAL_CORE observability inputs tied to signals inside Cortex-A9 MPU subsystem	**Cortex-A9 MPU subsystem observable signals mapped to SYSCTRL_GENERAL_CORE observability inputs**	**Signal Description**	**Logical Value Meaning**
hwobs_int_mpu[31:7]	Reserved	-	-
hwobs_int_mpu[6]	clkrst_emifclk_gated_hw	Copy of emifclk (ARM_FCLK / 2 or ARM_FCLK / 4 depending on EMIF_DIV_MODE input) which is gated by memory adapter hwdbgout.	-
hwobs_int_mpu[5:4]	Reserved	-	-
hwobs_int_mpu[3]	ARM_FCLK / 16	Cortex-A9 CPU0 / CPU1 input clock divided by 16.	-
hwobs_int_mpu[2:0]	Reserved	-	-

Table 18-33. Observability Signals Multiplexing at Cortex-A9 MPU Subsystem Level – Mode 9

CONTROL_DEBOBS_MMR_MPU[3:0] SELECT = 0b1001			
SYSCTRL_GENERAL_CORE Observability Inputs Tied to Signals Inside Cortex-A9 MPU Subsystem	**Cortex-A9 MPU Subsystem Observable Signals Mapped to SYSCTRL_GENERAL_CORE Observability Inputs**	**Signal Description**	**Logical Value Meaning**
hwobs_int_mpu[31:11]	Reserved	–	–
hwobs_int_mpu[10]	clkrst_emifclk_gated_hw	Copy of emifclk (ARM_FCLK / 2 or ARM_FCLK / 4, depending on EMIF_DIV_MODE input), which is gated by memory adapter hwdbgout	–

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Table 18-33. Observability Signals Multiplexing at Cortex-A9 MPU Subsystem Level – Mode 9 (continued)

CONTROL_DEBOBS_MMR_MPU[3:0] SELECT = 0b1001			
SYSCTRL_GENERAL_CORE Observability Inputs Tied to Signals Inside Cortex-A9 MPU Subsystem	**Cortex-A9 MPU Subsystem Observable Signals Mapped to SYSCTRL_GENERAL_CORE Observability Inputs**	**Signal Description**	**Logical Value Meaning**
hwobs_int_mpu[9:4]	Reserved	–	–
hwobs_int_mpu[3]	ARM_FCLK / 16	Cortex-A9 CPU0/CPU1 input clock divided by 16	–
hwobs_int_mpu[2:0]	Reserved	–	–

Table 18-34. Observability Signals Multiplexing at Cortex-A9 MPU Subsystem Level – Mode 10

CONTROL_DEBOBS_MMR_MPU[3:0] SELECT = 0b1010			
SYSCTRL_GENERAL_CORE Observability Inputs Tied to Signals Inside Cortex-A9 MPU Subsystem	**Cortex-A9 MPU Subsystem Observable Signals Mapped to SYSCTRL_GENERAL_CORE Observability Inputs**	**Signal Description**	**Logical Value Meaning**
hwobs_int_mpu[31:12]	Reserved	–	–
hwobs_int_mpu[11]	clkrst_emifclk_gated_hw	Copy of emifclk (ARM_FCLK / 2 or ARM_FCLK / 4, depending on EMIF_DIV_MODE input), which is gated by memory adapter hwdbgout	–
hwobs_int_mpu[10:4]	Reserved	–	–
hwobs_int_mpu[3]	ARM_FCLK / 16	Cortex-A9 CPU0 / CPU1 input clock divided by 16	–
hwobs_int_mpu[2:0]	Reserved	–	–

Table 18-35. Observability Signals Multiplexing at Cortex-A9 MPU Subsystem Level – Mode 11

CONTROL_DEBOBS_MMR_MPU[3:0] SELECT = 0b1011			
SYSCTRL_GENERAL_CORE Observability Inputs Tied to Signals Inside Cortex-A9 MPU Subsystem	**Cortex-A9 MPU Subsystem Observable Signals Mapped to SYSCTRL_GENERAL_CORE Observability Inputs**	**Signal Description**	**Logical Value Meaning**
hwobs_int_mpu[31:4]	Reserved	–	–
hwobs_int_mpu[3]	ARM_FCLK / 16	Cortex-A9 CPU0 / CPU1 input clock divided by 16	–
hwobs_int_mpu[2:0]	Reserved	–	–

18.4.11.5.2 IVA-HD Subsystem Observable Signals

Table 18-36 lists the full set of 13 IVA-HD observable signals from inside the IVA-HD subsystem. No observability signal multiplexing is implemented at the IVA-HD level.

Table 18-36. Observability Signals at IVA-HD Subsystem Level

SYSCTRL_GENERAL_CORE Observability Inputs Tied to Signals Inside IVA-HD Subsystem	**IVA-HD Subsystem Observable Signals Mapped to SYSCTRL_GENERAL_CORE Observability Inputs**	**Signal Description**	**Logical Value Meaning**
hwobs_int_ivahd[31:13]	unused	General control module IVA-HD inputs tied to low	Tied to low

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Table 18-36. Observability Signals at IVA-HD Subsystem Level (continued)

SYSCTRL_GENERAL_CORE Observability Inputs Tied to Signals Inside IVA-HD Subsystem	IVA-HD Subsystem Observable Signals Mapped to SYSCTRL_GENERAL_CORE Observability Inputs	Signal Description	Logical Value Meaning
hwobs_int_ivahd[12]	MAILBOX_poidleack[1]	Mailbox idle acknowledge (idle domain 0)	–
hwobs_int_ivahd[11]	IVAHD_INTC_poidleack[1]	IVA-HD local interconnect idle acknowledge (idle domain 0)	–
hwobs_int_ivahd[10]	SMSET_poidleack[1]	SMSET idle acknowledge (idle domain 0)	–
hwobs_int_ivahd[9]	MSGIF_poidleack[1]	MSGIF idle acknowledge (idle domain 0)	–
hwobs_int_ivahd[8]	ECD3_poidleack[1]	ECD3 idle acknowledge (idle domain 0)	–
hwobs_int_ivahd[7]	MC3_poidleack[1]	MC3 idle acknowledge (idle domain 0)	–
hwobs_int_ivahd[6]	IPE3_poidleack[1]	iPE3 idle acknowledge (idle domain 0)	–
hwobs_int_ivahd[5]	CALC3_poidleack[1]	CALC3 idle acknowledge (idle domain 0)	–
hwobs_int_ivahd[4]	ILF3_poidleack[1]	iLF3 idle acknowledge s (idle domain 0)	–
hwobs_int_ivahd[3]	IME3_poidleack[1]	iME3 idle acknowledge (idle domain 0)	–
hwobs_int_ivahd[2]	VDMA_poidleack[1]	vDMA idle acknowledge (idle domain 0)	–
hwobs_int_ivahd[1]	ICONT2_poidleack[1]	ICONT2 idle acknowledge (idle domain 0)	–
hwobs_int_ivahd[0]	ICONT1_poidleack[1]	ICONT1 idle acknowledge (idle domain 0)	–

18.4.11.5.3 Display Subsystem Observable Signals

The display subsystem observable signals described in Table 18-37 are directly mapped to th display subsystem observability inputs of the SYSCTRL_GENERAL_CORE module, and no additional multiplexing is performed inside the display subsystem wrapper.

Table 18-37. Observability Signals at Display Subsystem Level

SYSCTRL_GENERAL_CORE Observability Inputs Tied to Signals Inside Display Subsystem	Display Subsystem Observable Signals Mapped to SYSCTRL_GENERAL_CORE Observability Inputs	Signal Description	Logical Value Meaning
hwobs_dssvenctvdetgp	DSS_VENC_TVDETGP	Display subsystem VENC tvdetgp	Active high pulse to detect the TV connection
hwobs_dssdacpwrdndaczcvbs_y	DSS_DAC_PWR_DNDACZCVBS/Y	Display subsystem DAC pwrdn dac zcvbs_y – Power down for DAC Y	0: DAC Y put in power-down mode 1: DAC Y put in ACTIVE state
hwobs_dssdacpwrdndaczchroma	DSS_DAC_PWR_DNDACZCHROMA	Display subsystem DAC pwrdn dac zchroma – Power down for DAC CHROMA	0: DAC CHROMA put in power-down mode 1: DAC CHROMA put in ACTIVE state
hwobs_dssdacpwrdndaccvbs	DSS_DAC_PWR_DNDACCVBS	Display subsystem DAC pwrdn dac zcvbs – Power down for DAC CVBS	0: DAC CVBS put in power-down mode 1: DAC CVBS put in ACTIVE state

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Table 18-37. Observability Signals at Display Subsystem Level (continued)

SYSCTRL_GENERAL_CORE Observability Inputs Tied to Signals Inside Display Subsystem	Display Subsystem Observable Signals Mapped to SYSCTRL_GENERAL_CORE Observability Inputs	Signal Description	Logical Value Meaning
hwobs_dssdacpwrdnbgz	DSS_DAC_PWR_DNBGZ	Display subsystem DAC pwrdn bgz – Band gap power down for DAC	0: DAC Bandgap put in power-down mode 1: DAC Bandgap put in ACTIVE state

NOTE: The (VDAC) function is not supported.

18.4.11.5.4 DSP Subsystem Observable Signals

This information is not available in the public domain.

18.4.11.5.5 ABE Subsystem Observable Signals

The audio backend (ABE) observable signals described in Table 18-38 are directly mapped to the ABE dedicated observability inputs, hwobs_int_abe[31:0] of the SYSCTRL_GENERAL_CORE module, and no additional multiplexing is performed inside the ABE.

Table 18-38. Observability Signals at ABE Subsystem Level

SYSCTRL_GENERAL_CORE Observability Inputs Tied to Signals Inside Cortex-A9 MPU subsystem	SYSCTRL_GENERAL_CORE Observability Inputs Tied to Signals Inside Cortex-A9 MPU Subsystem	Signal Description	Logical Value Meaning
hwobs_int_abe[31:26]	–	–	–
hwobs_int_abe[25:24]	OPP_DIV	OPP DIVIDER bits [1:0]	–
hwobs_int_abe[23]	AESS_to_MPU_IRQ	IRQ sent from AESS to MCU. SeeChapter 12, *ABE*.	–
hwobs_int_abe[22]	AESS_to_DSPSS_IRQ	IRQ sent from AESS to DSP. See , *Interrupt Requests,* and Chapter 12, *ABE*.	–
hwobs_int_abe[21]	Reserved	–	–
hwobs_int_abe[20]	GPT_WDT_PWM_INP	PWM received from the GPTIMER or watchdog (OR)	–
hwobs_int_abe[19]	AESS_DMAREQ_ALL	(Logical OR with all DMA requests out)	High while outcoming DMA requests from audio engine have not been acknowledged by the host
hwobs_int_abe[18]	AESS_DMAREQ_PER	(Logical OR with all DMA requests coming from the peripheral)	High when incoming DMA requests from audio engine are still to be served
hwobs_int_abe[17]	AESS_IDLEPO	PO_IDLE AESS output	High when the audio engine executes a wait until an activation of the PI_WAKEUP pin is done
hwobs_int_abe[16:0]	RESERVED	–	–

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18.4.11.5.6 USBOTGHS Subsystem Observable Signals

One of the General Wakeup Control observability inputs can be mapped to the USBOTGHS start-of-frame signal (hsusbotg_sofpulse) by setting CONTROL_CORE_CONF_DEBUG_SEL_TST_11[3:0] MODE =0x1.

18.4.11.5.7 CM2 Subsystem Observable Signals

The SYSCTRL_GENERAL_CORE observability inputs hwobs_int_cm2(i), (where i = 0…31) are mapped to the signals debugcm2(i), (where i = 0…31) coming out of the PRCM submodule, clock manager 2 (CM2).

Local multiplexing controls at the CM2 level are in the CM2_DEBUG_CFG register. The CM2 observability output signals are driven on the debugcm2(0) through debugcm2(7) lines. A certain mux set is selected by programming the CM2_DEBUG_CFG[7:0] SEL0 bit field. The remaining debugcm2(8) through debugcm2(31) lines are reserved for future use. For more information about the CM2 observability source select field, see Section 3.11.30.1, *INTRCONN_SOCKET_CM2 Register Summary*, in Chapter 3, *Power, Reset, and Clock Management*.

Table 18-39 provides different details about the signals inside the CM 2 that can be monitored on device hw_dbg pins.

Table 18-39. CM2 Observable Signals

Byte	0x00	Type	AutoPRCM Signal Identifier	B#	Info +	Info +	Info +	Comments
Bit	7:0		Reserved					SPARE
Byte	0x01	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	7:0		Reserved					SPARE
Byte	0x02	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	7:0		Reserved					SPARE
Byte	0x03	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	7:0		Reserved					SPARE
Byte	0x04	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	7:0		Reserved					SPARE
Byte	0x5	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	7:0		Reserved					SPARE
Byte	0x6	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	7:0		Reserved					SPARE
Byte	0x7	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	7:0		Reserved					SPARE
Byte	0x8	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	7:0		Reserved					SPARE
Byte	0x9	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	7:0		Reserved					SPARE
Byte	0xa	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	7:0		Reserved					SPARE
Byte	0xb	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	7:0		Reserved					SPARE
Byte	0xc	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	7:0		Reserved					SPARE
Byte	0xd	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	7:0		Reserved					SPARE
Byte	0xe	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	7:0		Reserved					SPARE
Byte	0xf	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	7:0		Reserved					SPARE

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Table 18-39. CM2 Observable Signals (continued)

Byte	0x10	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	ifsm_ccptx_ccpt_stby_I0.MStandby				Input	
Bit	1	Internal	ifsm_ccptx_ccpt_stby_I0.init_Wait				Output	
Bit	2	Internal	ifsm_ccptx_ccpt_stby_I0.module_mwakeup	0			Input	
Bit	7:3		Reserved					
Byte	0x11	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	ifsm_deiss_mststdby_p_I0.MStandby				Input	
Bit	1	Internal	ifsm_deiss_mststdby_p_I0.init_Wait				Output	
Bit	2	Internal	ifsm_deiss_mststdby_p_I0.module_mwakeup	0			Input	
Bit	3	Internal	ifsm_dss_dss_stdby_pm_I0.MStandby				Input	
Bit	4	Internal	ifsm_dss_dss_stdby_pm_I0.init_Wait				Output	
Bit	5	Internal	ifsm_dss_dss_stdby_pm_I0.module_mwakeup	0			Input	
Bit	7:6		Reserved					
Byte	0x12	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	ifsm_cortex_m3_pm_master_I0.MStandby				Input	
Bit	1	Internal	ifsm_cortex_m3_pm_master_I0.init_Wait				Output	
Bit	2	Internal	ifsm_cortex_m3_pm_master_I0.module_mwakeup	0			Input	
Bit	3	Internal	ifsm_emac_mstandbyp_I0.MStandby				Input	
Bit	4	Internal	ifsm_emac_mstandbyp_I0.init_Wait				Output	
Bit	5	Internal	ifsm_emac_mstandbyp_I0.module_mwakeup	0			Input	
Bit	7:6		Reserved					
Byte	0x13	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	ifsm_fdif_standby_prot_I0.MStandby				Input	
Bit	1	Internal	ifsm_fdif_standby_prot_I0.init_Wait				Output	
Bit	2	Internal	ifsm_fdif_standby_prot_I0.module_mwakeup	0			Input	
Bit	3	Internal	ifsm_gfx_stby_prot_I0.MStandby				Input	
Bit	4	Internal	ifsm_gfx_stby_prot_I0.init_Wait				Output	
Bit	5	Internal	ifsm_gfx_stby_prot_I0.module_mwakeup	0			Input	
Bit	7:6		Reserved					
Byte	0x14	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	ifsm_hsi_hsi_standby_I0.MStandby				Input	
Bit	1	Internal	ifsm_hsi_hsi_standby_I0.init_Wait				Output	
Bit	2	Internal	ifsm_hsi_hsi_standby_I0.module_mwakeup	0			Input	
Bit	3	Internal	ifsm_iss_standby_iss_I0.MStandby				Input	
Bit	4	Internal	ifsm_iss_standby_iss_I0.init_Wait				Output	
Bit	5	Internal	ifsm_iss_standby_iss_I0.module_mwakeup	0			Input	
Bit	7:6		Reserved					
Byte	0x15	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	ifsm_ivahd_master_I0.MStandby				Input	
Bit	1	Internal	ifsm_ivahd_master_I0.init_Wait				Output	
Bit	2	Internal	ifsm_ivahd_master_I0.module_mwakeup	0			Input	
Bit	3	Internal	ifsm_mmc1_stby_prot_I0.MStandby				Input	
Bit	4	Internal	ifsm_mmc1_stby_prot_I0.init_Wait				Output	
Bit	5	Internal	ifsm_mmc1_stby_prot_I0.module_mwakeup	0			Input	
Bit	7:6		Reserved					
Byte	0x16	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	ifsm_mmc2_stby_prot_I0.MStandby				Input	
Bit	1	Internal	ifsm_mmc2_stby_prot_I0.init_Wait				Output	

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Table 18-39. CM2 Observable Signals (continued)

Bit	2	Internal	ifsm_mmc2_stby_prot_I0.module_mwakeup	0			Input	
Bit	7:3		Reserved					
Byte	0x17	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	7:0		Reserved					
Byte	0x18	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	ifsm_sad2d_sad2d_stby_I0.MStandby				Input	
Bit	1	Internal	ifsm_sad2d_sad2d_stby_I0.init_Wait				Output	
Bit	2	Internal	ifsm_sad2d_sad2d_stby_I0.module_mwakeup	0			Input	
Bit	7:3		Reserved					
Byte	0x19	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	ifsm_sdma_stby_prot_I0.MStandby				Input	
Bit	1	Internal	ifsm_sdma_stby_prot_I0.init_Wait				Output	
Bit	2	Internal	ifsm_sdma_stby_prot_I0.module_mwakeup	0			Input	
Bit	3	Internal	ifsm_tppss_cppidma_stdby_prm_I0.MStandby				Input	
Bit	4	Internal	ifsm_tppss_cppidma_stdby_prm_I0.init_Wait				Output	
Bit	5	Internal	ifsm_tppss_cppidma_stdby_prm_I0.module_mwakeup	0			Input	
Bit	7:6		Reserved					
Byte	0x1a	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	2:0		reserved					
Bit	3	Internal	ifsm_usb_host_fs_standby_prot_I0.MStandby				Input	
Bit	4	Internal	ifsm_usb_host_fs_standby_prot_I0.init_Wait				Output	
Bit	5	Internal	ifsm_usb_host_fs_standby_prot_I0.module_mwakeup	0			Input	
Bit	7:6		Reserved					
Byte	0x1b	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	ifsm_usb_host_usbhosths_intrconn_masterif_pwr_I0.MStandby				Input	
Bit	1	Internal	ifsm_usb_host_usbhosths_intrconn_masterif_pwr_I0.init_Wait				Output	
Bit	2	Internal	ifsm_usb_host_usbhosths_intrconn_masterif_pwr_I0.module_mwakeup	0			Input	
Bit	3	Internal	ifsm_usb_otg_usbotghs_intrconn_master_I0.MStandby				Input	
Bit	4	Internal	ifsm_usb_otg_usbotghs_intrconn_master_I0.init_Wait				Output	
Bit	5	Internal	ifsm_usb_otg_usbotghs_intrconn_master_I0.module_mwakeup	0			Input	
Bit	7:6		Reserved					
Byte	0x1c	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	ifsm_xhpi_hpi_stby_I0.MStandby				Input	
Bit	1	Internal	ifsm_xhpi_hpi_stby_I0.init_Wait				Output	
Bit	2	Internal	ifsm_xhpi_hpi_stby_I0.module_mwakeup	0			Input	
Bit	3	Internal	tfsm_adc_adc_idle_I0.idleReq				Output	
Bit	4	Internal	tfsm_adc_adc_idle_I0.SidleAck	1			Input	
Bit	5	Internal	tfsm_adc_adc_idle_I0.module_swakeup	0			Input	
Bit	6	Internal	tfsm_adc_adc_idle_I0.fclken_IP				Output	
Bit	7		Reserved					
Byte	0x1d	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	7:0		Reserved					
Byte	0x1e	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	tfsm_ccptx_ccpt_idle_I0.idleReq				Output	
Bit	1	Internal	tfsm_ccptx_ccpt_idle_I0.SidleAck	1			Input	
Bit	2	Internal	tfsm_ccptx_ccpt_idle_I0.module_swakeup	0			Input	

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Table 18-39. CM2 Observable Signals (continued)

Bit	3	Internal	tfsm_ccptx_ccpt_idle_I0.fclken_IP				Output	
Bit	4	Internal	tfsm_cm2_profiling_I0.idleReq				Output	
Bit	5	Internal	tfsm_cm2_profiling_I0.SidleAck	1			Input	
Bit	6	Internal	tfsm_cm2_profiling_I0.module_swakeup	0			Input	
Bit	7	Internal	tfsm_cm2_profiling_I0.fclken_IP				Output	
Byte	0x1f	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	7:0		Reserved					
Byte	0x20	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	tfsm_deiss_slvidle_p_I0.idleReq				Output	
Bit	1	Internal	tfsm_deiss_slvidle_p_I0.SidleAck	1			Input	
Bit	2	Internal	tfsm_deiss_slvidle_p_I0.module_swakeup	0			Input	
Bit	3	Internal	tfsm_deiss_slvidle_p_I0.fclken_IP				Output	
Bit	7:4		Reserved					
Byte	0x21	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	tfsm_dmm_idle_prot_I0.idleReq				Output	
Bit	1	Internal	tfsm_dmm_idle_prot_I0.SidleAck	1			Input	
Bit	2	Internal	tfsm_dmm_idle_prot_I0.module_swakeup	0			Input	
Bit	3	Internal	tfsm_dmm_idle_prot_I0.fclken_IP				Output	
Bit	4	Internal	tfsm_dmtimer10_dmtimer_dmc1ms_power_I0.idleReq				Output	
Bit	5	Internal	tfsm_dmtimer10_dmtimer_dmc1ms_power_I0.SidleAck	1			Input	
Bit	6	Internal	tfsm_dmtimer10_dmtimer_dmc1ms_power_I0.module_swakeup	0			Input	
Bit	7	Internal	tfsm_dmtimer10_dmtimer_dmc1ms_power_I0.fclken_IP				Output	
Byte	0x22	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	tfsm_dmtimer11_dmtimer_dmc_power_I0.idleReq				Output	
Bit	1	Internal	tfsm_dmtimer11_dmtimer_dmc_power_I0.SidleAck	1			Input	
Bit	2	Internal	tfsm_dmtimer11_dmtimer_dmc_power_I0.module_swakeup	0			Input	
Bit	3	Internal	tfsm_dmtimer11_dmtimer_dmc_power_I0.fclken_IP				Output	
Bit	4	Internal	tfsm_dmtimer2_dmtimer_dmc1ms_power_I0.idleReq				Output	
Bit	5	Internal	tfsm_dmtimer2_dmtimer_dmc1ms_power_I0.SidleAck	1			Input	
Bit	6	Internal	tfsm_dmtimer2_dmtimer_dmc1ms_power_I0.module_swakeup	0			Input	
Bit	7	Internal	tfsm_dmtimer2_dmtimer_dmc1ms_power_I0.fclken_IP				Output	
Byte	0x23	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	tfsm_dmtimer3_dmtimer_dmc_power_I0.idleReq				Output	
Bit	1	Internal	tfsm_dmtimer3_dmtimer_dmc_power_I0.SidleAck	1			Input	
Bit	2	Internal	tfsm_dmtimer3_dmtimer_dmc_power_I0.module_swakeup	0			Input	
Bit	3	Internal	tfsm_dmtimer3_dmtimer_dmc_power_I0.fclken_IP				Output	
Bit	4	Internal	tfsm_dmtimer4_dmtimer_dmc_power_I0.idleReq				Output	
Bit	5	Internal	tfsm_dmtimer4_dmtimer_dmc_power_I0.SidleAck	1			Input	
Bit	6	Internal	tfsm_dmtimer4_dmtimer_dmc_power_I0.module_swakeup	0			Input	
Bit	7	Internal	tfsm_dmtimer4_dmtimer_dmc_power_I0.fclken_IP				Output	
Byte	0x24	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	tfsm_dmtimer9_dmtimer_dmc_power_I0.idleReq				Output	
Bit	1	Internal	tfsm_dmtimer9_dmtimer_dmc_power_I0.SidleAck	1			Input	
Bit	2	Internal	tfsm_dmtimer9_dmtimer_dmc_power_I0.module_swakeup	0			Input	
Bit	3	Internal	tfsm_dmtimer9_dmtimer_dmc_power_I0.fclken_IP				Output	
Bit	7:4		Reserved					

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Table 18-39. CM2 Observable Signals (continued)

Byte	0x25	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	tfsm_dss_dss_idle_pm_I0.idleReq				Output	
Bit	1	Internal	tfsm_dss_dss_idle_pm_I0.SidleAck	1			Input	
Bit	2	Internal	tfsm_dss_dss_idle_pm_I0.module_swakeup	0			Input	
Bit	3	Internal	tfsm_dss_dss_idle_pm_I0.module_swakeup	1			Input	
Bit	4	Internal	tfsm_dss_dss_idle_pm_I0.module_swakeup	2			Input	
Bit	5	Internal	tfsm_dss_dss_idle_pm_I0.module_swakeup	3			Input	
Bit	6	Internal	tfsm_dss_dss_idle_pm_I0.module_swakeup	4			Input	
Bit	7	Internal	tfsm_dss_dss_idle_pm_I0.fclken_IP				Output	
Byte	0x26	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	tfsm_cortex_m3_pm_slave_I0.idleReq				Output	
Bit	1	Internal	tfsm_cortex_m3_pm_slave_I0.SidleAck	1			Input	
Bit	2	Internal	tfsm_cortex_m3_pm_slave_I0.module_swakeup	0			Input	
Bit	3	Internal	tfsm_cortex_m3_pm_slave_I0.fclken_IP				Output	
Bit	4	Internal	tfsm_elm_idle_I0.idleReq				Output	
Bit	5	Internal	tfsm_elm_idle_I0.SidleAck	1			Input	
Bit	6	Internal	tfsm_elm_idle_I0.module_swakeup	0			Input	
Bit	7	Internal	tfsm_elm_idle_I0.fclken_IP				Output	
Byte	0x27	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	tfsm_emac_slv0p_I0.idleReq				Output	
Bit	1	Internal	tfsm_emac_slv0p_I0.SidleAck	1			Input	
Bit	2	Internal	tfsm_emac_slv0p_I0.module_swakeup	0			Input	
Bit	3	Internal	tfsm_emac_slv0p_I0.fclken_IP				Output	
Bit	4	Internal	tfsm_emif1_l3idleprm_I0.idleReq				Output	
Bit	5	Internal	tfsm_emif1_l3idleprm_I0.SidleAck	1			Input	
Bit	6	Internal	tfsm_emif1_l3idleprm_I0.module_swakeup	0			Input	
Bit	7	Internal	tfsm_emif1_l3idleprm_I0.fclken_IP				Output	
Byte	0x28	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	tfsm_emif2_l3idleprm_I0.idleReq				Output	
Bit	1	Internal	tfsm_emif2_l3idleprm_I0.SidleAck	1			Input	
Bit	2	Internal	tfsm_emif2_l3idleprm_I0.module_swakeup	0			Input	
Bit	3	Internal	tfsm_emif2_l3idleprm_I0.fclken_IP				Output	
Bit	7:4		Reserved					
Byte	0x29	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	tfsm_emif_h1_l3idleprm_I0.idleReq				Output	
Bit	1	Internal	tfsm_emif_h1_l3idleprm_I0.SidleAck	1			Input	
Bit	2	Internal	tfsm_emif_h1_l3idleprm_I0.module_swakeup	0			Input	
Bit	3	Internal	tfsm_emif_h1_l3idleprm_I0.fclken_IP				Output	
Bit	4	Internal	tfsm_emif_h2_l3idleprm_I0.idleReq				Output	
Bit	5	Internal	tfsm_emif_h2_l3idleprm_I0.SidleAck	1			Input	
Bit	6	Internal	tfsm_emif_h2_l3idleprm_I0.module_swakeup	0			Input	
Bit	7	Internal	tfsm_emif_h2_l3idleprm_I0.fclken_IP				Output	
Byte	0x2a	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	tfsm_fdif_idle_prot_I0.idleReq				Output	
Bit	1	Internal	tfsm_fdif_idle_prot_I0.SidleAck	1			Input	
Bit	2	Internal	tfsm_fdif_idle_prot_I0.module_swakeup	0			Input	
Bit	3	Internal	tfsm_fdif_idle_prot_I0.fclken_IP				Output	
Bit	4	Internal	tfsm_gfx_idle_prot_I0.idleReq				Output	

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Table 18-39. CM2 Observable Signals (continued)

Bit	5	Internal	tfsm_gfx_idle_prot_I0.SidleAck	1			Input	
Bit	6	Internal	tfsm_gfx_idle_prot_I0.module_swakeup	0			Input	
Bit	7	Internal	tfsm_gfx_idle_prot_I0.fclken_IP				Output	
Byte	0x2b	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	tfsm_gpio2_gpio_v2_power_I0.idleReq				Output	
Bit	1	Internal	tfsm_gpio2_gpio_v2_power_I0.SidleAck	1			Input	
Bit	2	Internal	tfsm_gpio2_gpio_v2_power_I0.module_swakeup	0			Input	
Bit	3	Internal	tfsm_gpio2_gpio_v2_power_I0.module_swakeup	1			Input	
Bit	4	Internal	tfsm_gpio2_gpio_v2_power_I0.fclken_IP				Output	
Bit	7:5		Reserved					
Byte	0x2c	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	tfsm_gpio3_gpio_v2_power_I0.idleReq				Output	
Bit	1	Internal	tfsm_gpio3_gpio_v2_power_I0.SidleAck	1			Input	
Bit	2	Internal	tfsm_gpio3_gpio_v2_power_I0.module_swakeup	0			Input	
Bit	3	Internal	tfsm_gpio3_gpio_v2_power_I0.module_swakeup	1			Input	
Bit	4	Internal	tfsm_gpio3_gpio_v2_power_I0.fclken_IP				Output	
Bit	7:5		Reserved					
Byte	0x2d	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	tfsm_gpio4_gpio_v2_power_I0.idleReq				Output	
Bit	1	Internal	tfsm_gpio4_gpio_v2_power_I0.SidleAck	1			Input	
Bit	2	Internal	tfsm_gpio4_gpio_v2_power_I0.module_swakeup	0			Input	
Bit	3	Internal	tfsm_gpio4_gpio_v2_power_I0.module_swakeup	1			Input	
Bit	4	Internal	tfsm_gpio4_gpio_v2_power_I0.fclken_IP				Output	
Bit	7:5		Reserved					
Byte	0x2e	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	tfsm_gpio5_gpio_v2_power_I0.idleReq				Output	
Bit	1	Internal	tfsm_gpio5_gpio_v2_power_I0.SidleAck	1			Input	
Bit	2	Internal	tfsm_gpio5_gpio_v2_power_I0.module_swakeup	0			Input	
Bit	3	Internal	tfsm_gpio5_gpio_v2_power_I0.module_swakeup	1			Input	
Bit	4	Internal	tfsm_gpio5_gpio_v2_power_I0.fclken_IP				Output	
Bit	7:5		Reserved					
Byte	0x2f	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	tfsm_gpio6_gpio_v2_power_I0.idleReq				Output	
Bit	1	Internal	tfsm_gpio6_gpio_v2_power_I0.SidleAck	1			Input	
Bit	2	Internal	tfsm_gpio6_gpio_v2_power_I0.module_swakeup	0			Input	
Bit	3	Internal	tfsm_gpio6_gpio_v2_power_I0.module_swakeup	1			Input	
Bit	4	Internal	tfsm_gpio6_gpio_v2_power_I0.fclken_IP				Output	
Bit	7:5		Reserved					
Byte	0x30	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	tfsm_gpmc_idle_I0.idleReq				Output	
Bit	1	Internal	tfsm_gpmc_idle_I0.SidleAck	1			Input	
Bit	2	Internal	tfsm_gpmc_idle_I0.module_swakeup	0			Input	
Bit	3	Internal	tfsm_gpmc_idle_I0.fclken_IP				Output	
Bit	4	Internal	tfsm_hdq1w_hdq1w_idle_I0.idleReq				Output	
Bit	5	Internal	tfsm_hdq1w_hdq1w_idle_I0.SidleAck	1			Input	
Bit	6	Internal	tfsm_hdq1w_hdq1w_idle_I0.module_swakeup	0			Input	
Bit	7	Internal	tfsm_hdq1w_hdq1w_idle_I0.fclken_IP				Output	
Byte	0x31	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments

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Table 18-39. CM2 Observable Signals (continued)

Bit	0	Internal	tfsm_hecc1_hecc_cfg_idle_I0.idleReq				Output	
Bit	1	Internal	tfsm_hecc1_hecc_cfg_idle_I0.SidleAck	1			Input	
Bit	2	Internal	tfsm_hecc1_hecc_cfg_idle_I0.module_swakeup	0			Input	
Bit	3	Internal	tfsm_hecc1_hecc_cfg_idle_I0.fclken_IP				Output	
Bit	4	Internal	tfsm_hecc2_hecc_cfg_idle_I0.idleReq				Output	
Bit	5	Internal	tfsm_hecc2_hecc_cfg_idle_I0.SidleAck	1			Input	
Bit	6	Internal	tfsm_hecc2_hecc_cfg_idle_I0.module_swakeup	0			Input	
Bit	7	Internal	tfsm_hecc2_hecc_cfg_idle_I0.fclken_IP				Output	
Byte	0x32	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	tfsm_hsi_hsi_idle_I0.idleReq				Output	
Bit	1	Internal	tfsm_hsi_hsi_idle_I0.SidleAck	1			Input	
Bit	2	Internal	tfsm_hsi_hsi_idle_I0.module_swakeup	0			Input	
Bit	3	Internal	tfsm_hsi_hsi_idle_I0.module_swakeup	1			Input	
Bit	4	Internal	tfsm_hsi_hsi_idle_I0.module_swakeup	2			Input	
Bit	5	Internal	tfsm_hsi_hsi_idle_I0.fclken_IP				Output	
Bit	7:6		Reserved					
Byte	0x33	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	tfsm_hw_sem_hwsem_idle_I0.idleReq				Output	
Bit	1	Internal	tfsm_hw_sem_hwsem_idle_I0.SidleAck	1			Input	
Bit	2	Internal	tfsm_hw_sem_hwsem_idle_I0.module_swakeup	0			Input	
Bit	3	Internal	tfsm_hw_sem_hwsem_idle_I0.fclken_IP				Output	
Bit	7:4		Reserved					
Byte	0x34	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	tfsm_i2c1_mshsi2cintrconn_power_I0.idleReq				Output	
Bit	1	Internal	tfsm_i2c1_mshsi2cintrconn_power_I0.SidleAck	1			Input	
Bit	2	Internal	tfsm_i2c1_mshsi2cintrconn_power_I0.module_swakeup	0			Input	
Bit	3	Internal	tfsm_i2c1_mshsi2cintrconn_power_I0.module_swakeup	1			Input	
Bit	4	Internal	tfsm_i2c1_mshsi2cintrconn_power_I0.fclken_IP				Output	
Bit	7:5		Reserved					
Byte	0x35	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	tfsm_i2c2_mshsi2cintrconn_power_I0.idleReq				Output	
Bit	1	Internal	tfsm_i2c2_mshsi2cintrconn_power_I0.SidleAck	1			Input	
Bit	2	Internal	tfsm_i2c2_mshsi2cintrconn_power_I0.module_swakeup	0			Input	
Bit	3	Internal	tfsm_i2c2_mshsi2cintrconn_power_I0.module_swakeup	1			Input	
Bit	4	Internal	tfsm_i2c2_mshsi2cintrconn_power_I0.fclken_IP				Output	
Bit	7:5		Reserved					
Byte	0x36	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	tfsm_i2c3_mshsi2cintrconn_power_I0.idleReq				Output	
Bit	1	Internal	tfsm_i2c3_mshsi2cintrconn_power_I0.SidleAck	1			Input	
Bit	2	Internal	tfsm_i2c3_mshsi2cintrconn_power_I0.module_swakeup	0			Input	
Bit	3	Internal	tfsm_i2c3_mshsi2cintrconn_power_I0.module_swakeup	1			Input	
Bit	4	Internal	tfsm_i2c3_mshsi2cintrconn_power_I0.fclken_IP				Output	
Bit	7:5		Reserved					
Byte	0x37	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	tfsm_i2c4_mshsi2cintrconn_power_I0.idleReq				Output	
Bit	1	Internal	tfsm_i2c4_mshsi2cintrconn_power_I0.SidleAck	1			Input	
Bit	2	Internal	tfsm_i2c4_mshsi2cintrconn_power_I0.module_swakeup	0			Input	
Bit	3	Internal	tfsm_i2c4_mshsi2cintrconn_power_I0.module_swakeup	1			Input	

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Table 18-39. CM2 Observable Signals (continued)

Bit	4	Internal	tfsm_i2c4_mshsi2cintrconn_power_I0.fclken_IP				Output	
Bit	7:5		Reserved					
Byte	0x38	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	tfsm_i2c5_mshsi2cintrconn_power_I0.idleReq				Output	
Bit	1	Internal	tfsm_i2c5_mshsi2cintrconn_power_I0.SidleAck	1			Input	
Bit	2	Internal	tfsm_i2c5_mshsi2cintrconn_power_I0.module_swakeup	0			Input	
Bit	3	Internal	tfsm_i2c5_mshsi2cintrconn_power_I0.module_swakeup	1			Input	
Bit	4	Internal	tfsm_i2c5_mshsi2cintrconn_power_I0.fclken_IP				Output	
Bit	7:5		Reserved					
Byte	0x39	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	tfsm_iss_idle_iss_I0.idleReq				Output	
Bit	1	Internal	tfsm_iss_idle_iss_I0.SidleAck	1			Input	
Bit	2	Internal	tfsm_iss_idle_iss_I0.module_swakeup	0			Input	
Bit	3	Internal	tfsm_iss_idle_iss_I0.fclken_IP				Output	
Bit	4	Internal	tfsm_ivahd_idle0_I0.idleReq				Output	
Bit	5	Internal	tfsm_ivahd_idle0_I0.SidleAck	1			Input	
Bit	6	Internal	tfsm_ivahd_idle0_I0.module_swakeup	0			Input	
Bit	7	Internal	tfsm_ivahd_idle0_I0.fclken_IP				Output	
Byte	0x3a	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	tfsm_l3_instr_interconnect_idle_prot_I0.idleReq				Output	
Bit	1	Internal	tfsm_l3_instr_interconnect_idle_prot_I0.SidleAck	1			Input	
Bit	2	Internal	tfsm_l3_instr_interconnect_idle_prot_I0.module_swakeup	0			Input	
Bit	3	Internal	tfsm_l3_instr_interconnect_idle_prot_I0.fclken_IP				Output	
Bit	4	Internal	tfsm_l3_interconnect_1_idle_prot_I0.idleReq				Output	
Bit	5	Internal	tfsm_l3_interconnect_1_idle_prot_I0.SidleAck	1			Input	
Bit	6	Internal	tfsm_l3_interconnect_1_idle_prot_I0.module_swakeup	0			Input	
Bit	7	Internal	tfsm_l3_interconnect_1_idle_prot_I0.fclken_IP				Output	
Byte	0x3b	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	tfsm_l3_interconnect_2_idle_prot_I0.idleReq				Output	
Bit	1	Internal	tfsm_l3_interconnect_2_idle_prot_I0.SidleAck	1			Input	
Bit	2	Internal	tfsm_l3_interconnect_2_idle_prot_I0.module_swakeup	0			Input	
Bit	3	Internal	tfsm_l3_interconnect_2_idle_prot_I0.fclken_IP				Output	
Bit	4	Internal	tfsm_l3_interconnect_3_idle_prot_I0.idleReq				Output	
Bit	5	Internal	tfsm_l3_interconnect_3_idle_prot_I0.SidleAck	1			Input	
Bit	6	Internal	tfsm_l3_interconnect_3_idle_prot_I0.module_swakeup	0			Input	
Bit	7	Internal	tfsm_l3_interconnect_3_idle_prot_I0.fclken_IP				Output	
Byte	0x3c	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	tfsm_l4_cfg_interconnect_idle_prot_I0.idleReq				Output	
Bit	1	Internal	tfsm_l4_cfg_interconnect_idle_prot_I0.SidleAck	1			Input	
Bit	2	Internal	tfsm_l4_cfg_interconnect_idle_prot_I0.module_swakeup	0			Input	
Bit	3	Internal	tfsm_l4_cfg_interconnect_idle_prot_I0.fclken_IP				Output	
Bit	4	Internal	tfsm_l4_per_interconnect_idle_prot_I0.idleReq				Output	
Bit	5	Internal	tfsm_l4_per_interconnect_idle_prot_I0.SidleAck	1			Input	
Bit	6	Internal	tfsm_l4_per_interconnect_idle_prot_I0.module_swakeup	0			Input	
Bit	7	Internal	tfsm_l4_per_interconnect_idle_prot_I0.fclken_IP				Output	
Byte	0x3d	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	tfsm_mailbox_mbx_idle_I0.idleReq				Output	
Bit	1	Internal	tfsm_mailbox_mbx_idle_I0.SidleAck	1			Input	

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Table 18-39. CM2 Observable Signals (continued)

Bit	2	Internal	tfsm_mailbox_mbx_idle_I0.module_swakeup	0			Input	
Bit	3	Internal	tfsm_mailbox_mbx_idle_I0.fclken_IP				Output	
Bit	7:4		Reserved					
Byte	0x3e	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	7:0		Reserved					
Byte	0x3f	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	7:0		Reserved					
Byte	0x40	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	tfsm_mcbsp4_mcbsplp_power_I0.idleReq				Output	
Bit	1	Internal	tfsm_mcbsp4_mcbsplp_power_I0.SidleAck	1			Input	
Bit	2	Internal	tfsm_mcbsp4_mcbsplp_power_I0.module_swakeup	0			Input	
Bit	3	Internal	tfsm_mcbsp4_mcbsplp_power_I0.fclken_IP				Output	
Bit	4	Internal	tfsm_mcspi1_spi_power_I0.idleReq				Output	
Bit	5	Internal	tfsm_mcspi1_spi_power_I0.SidleAck	1			Input	
Bit	6	Internal	tfsm_mcspi1_spi_power_I0.module_swakeup	0			Input	
Bit	7	Internal	tfsm_mcspi1_spi_power_I0.fclken_IP				Output	
Byte	0x41	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	tfsm_mcspi2_spi_power_I0.idleReq				Output	
Bit	1	Internal	tfsm_mcspi2_spi_power_I0.SidleAck	1			Input	
Bit	2	Internal	tfsm_mcspi2_spi_power_I0.module_swakeup	0			Input	
Bit	3	Internal	tfsm_mcspi2_spi_power_I0.fclken_IP				Output	
Bit	4	Internal	tfsm_mcspi3_spi_power_I0.idleReq				Output	
Bit	5	Internal	tfsm_mcspi3_spi_power_I0.SidleAck	1			Input	
Bit	6	Internal	tfsm_mcspi3_spi_power_I0.module_swakeup	0			Input	
Bit	7	Internal	tfsm_mcspi3_spi_power_I0.fclken_IP				Output	
Byte	0x42	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	tfsm_mcspi4_spi_power_I0.idleReq				Output	
Bit	1	Internal	tfsm_mcspi4_spi_power_I0.SidleAck	1			Input	
Bit	2	Internal	tfsm_mcspi4_spi_power_I0.module_swakeup	0			Input	
Bit	3	Internal	tfsm_mcspi4_spi_power_I0.fclken_IP				Output	
Bit	7:4		Reserved					
Byte	0x43	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	tfsm_mmc1_idle_prot_I0.idleReq				Output	
Bit	1	Internal	tfsm_mmc1_idle_prot_I0.SidleAck	1			Input	
Bit	2	Internal	tfsm_mmc1_idle_prot_I0.module_swakeup	0			Input	
Bit	3	Internal	tfsm_mmc1_idle_prot_I0.fclken_IP				Output	
Bit	4	Internal	tfsm_mmc2_idle_prot_I0.idleReq				Output	
Bit	5	Internal	tfsm_mmc2_idle_prot_I0.SidleAck	1			Input	
Bit	6	Internal	tfsm_mmc2_idle_prot_I0.module_swakeup	0			Input	
Bit	7	Internal	tfsm_mmc2_idle_prot_I0.fclken_IP				Output	
Byte	0x44	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	3:0		Reserved					
Bit	4	Internal	tfsm_mmc_sd3_mmchs_idle_I0.idleReq				Output	
Bit	5	Internal	tfsm_mmc_sd3_mmchs_idle_I0.SidleAck	1			Input	
Bit	6	Internal	tfsm_mmc_sd3_mmchs_idle_I0.module_swakeup	0			Input	
Bit	7	Internal	tfsm_mmc_sd3_mmchs_idle_I0.fclken_IP				Output	
Byte	0x45	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	tfsm_mmc_sd4_mmchs_idle_I0.idleReq				Output	

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Table 18-39. CM2 Observable Signals (continued)

Bit	1	Internal	tfsm_mmc_sd4_mmchs_idle_I0.SidleAck	1			Input	
Bit	2	Internal	tfsm_mmc_sd4_mmchs_idle_I0.module_swakeup	0			Input	
Bit	3	Internal	tfsm_mmc_sd4_mmchs_idle_I0.fclken_IP				Output	
Bit	4	Internal	tfsm_mmc_sd5_mmchs_idle_I0.idleReq				Output	
Bit	5	Internal	tfsm_mmc_sd5_mmchs_idle_I0.SidleAck	1			Input	
Bit	6	Internal	tfsm_mmc_sd5_mmchs_idle_I0.module_swakeup	0			Input	
Bit	7	Internal	tfsm_mmc_sd5_mmchs_idle_I0.fclken_IP				Output	
Byte	0x46	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	tfsm_modem_icr_idle_prot_I0.idleReq				Output	
Bit	1	Internal	tfsm_modem_icr_idle_prot_I0.SidleAck	1			Input	
Bit	2	Internal	tfsm_modem_icr_idle_prot_I0.module_swakeup	0			Input	
Bit	3	Internal	tfsm_modem_icr_idle_prot_I0.fclken_IP				Output	
Bit	4	Internal	tfsm_modem_intc_idle_prot_I0.idleReq				Output	
Bit	5	Internal	tfsm_modem_intc_idle_prot_I0.SidleAck	1			Input	
Bit	6	Internal	tfsm_modem_intc_idle_prot_I0.module_swakeup	0			Input	
Bit	7	Internal	tfsm_modem_intc_idle_prot_I0.fclken_IP				Output	
Byte	0x47	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	3:0		Reserved					
Bit	4	Internal	tfsm_ocmc_ram_ocmcram_idle_I0.idleReq				Output	
Bit	5	Internal	tfsm_ocmc_ram_ocmcram_idle_I0.SidleAck	1			Input	
Bit	6	Internal	tfsm_ocmc_ram_ocmcram_idle_I0.module_swakeup	0			Input	
Bit	7	Internal	tfsm_ocmc_ram_ocmcram_idle_I0.fclken_IP				Output	
Byte	0x48	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	tfsm_ocp_wp1_idle_prot_I0.idleReq				Output	
Bit	1	Internal	tfsm_ocp_wp1_idle_prot_I0.SidleAck	1			Input	
Bit	2	Internal	tfsm_ocp_wp1_idle_prot_I0.module_swakeup	0			Input	
Bit	3	Internal	tfsm_ocp_wp1_idle_prot_I0.fclken_IP				Output	
Bit	7:4		Reserved					
Byte	0x49	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	7:4		Reserved					
Byte	0x4a	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	3:0		Reserved					
Bit	4	Internal	tfsm_sad2d_d2d_idle_I0.idleReq				Output	
Bit	5	Internal	tfsm_sad2d_d2d_idle_I0.SidleAck	1			Input	
Bit	6	Internal	tfsm_sad2d_d2d_idle_I0.module_swakeup	0			Input	
Bit	7	Internal	tfsm_sad2d_d2d_idle_I0.fclken_IP				Output	
Byte	0x4b	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	7:0		Reserved					
Byte	0x4c	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	3:0		Reserved					
Bit	4	Internal	tfsm_sdma_idle_prot_I0.idleReq				Output	
Bit	5	Internal	tfsm_sdma_idle_prot_I0.SidleAck	1			Input	
Bit	6	Internal	tfsm_sdma_idle_prot_I0.module_swakeup	0			Input	
Bit	7	Internal	tfsm_sdma_idle_prot_I0.fclken_IP				Output	
Byte	0x4d	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	3:0		Reserved					
Bit	4	Internal	tfsm_sl2_idle1_I0.idleReq				Output	
Bit	5	Internal	tfsm_sl2_idle1_I0.SidleAck	1			Input	

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Table 18-39. CM2 Observable Signals (continued)

Bit	6	Internal	tfsm_sl2_idle1_I0.module_swakeup	0			Input	
Bit	7	Internal	tfsm_sl2_idle1_I0.fclken_IP				Output	
Byte	0x4e	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	tfsm_slimbus2_slimbus_power_I0.idleReq				Output	
Bit	1	Internal	tfsm_slimbus2_slimbus_power_I0.SidleAck	1			Input	
Bit	2	Internal	tfsm_slimbus2_slimbus_power_I0.module_swakeup	0			Input	
Bit	3	Internal	tfsm_slimbus2_slimbus_power_I0.module_swakeup	1			Input	
Bit	4	Internal	tfsm_slimbus2_slimbus_power_I0.fclken_IP				Output	
Bit	7:5		Reserved					
Byte	0x4f	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	tfsm_smartreflex_core_sr_idle_I0.idleReq				Output	
Bit	1	Internal	tfsm_smartreflex_core_sr_idle_I0.SidleAck	1			Input	
Bit	2	Internal	tfsm_smartreflex_core_sr_idle_I0.module_swakeup	0			Input	
Bit	3	Internal	tfsm_smartreflex_core_sr_idle_I0.fclken_IP				Output	
Bit	4	Internal	tfsm_smartreflex_iva_sr_idle_I0.idleReq				Output	
Bit	5	Internal	tfsm_smartreflex_iva_sr_idle_I0.SidleAck	1			Input	
Bit	6	Internal	tfsm_smartreflex_iva_sr_idle_I0.module_swakeup	0			Input	
Bit	7	Internal	tfsm_smartreflex_iva_sr_idle_I0.fclken_IP				Output	
Byte	0x50	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	tfsm_smartreflex_mpu_sr_idle_I0.idleReq				Output	
Bit	1	Internal	tfsm_smartreflex_mpu_sr_idle_I0.SidleAck	1			Input	
Bit	2	Internal	tfsm_smartreflex_mpu_sr_idle_I0.module_swakeup	0			Input	
Bit	3	Internal	tfsm_smartreflex_mpu_sr_idle_I0.fclken_IP				Output	
Bit	4	Internal	tfsm_tppss_tppss_slave_prm_I0.idleReq				Output	
Bit	5	Internal	tfsm_tppss_tppss_slave_prm_I0.SidleAck	1			Input	
Bit	6	Internal	tfsm_tppss_tppss_slave_prm_I0.module_swakeup	0			Input	
Bit	7	Internal	tfsm_tppss_tppss_slave_prm_I0.fclken_IP				Output	
Byte	0x51	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	tfsm_uart1_uartirdacirintrconn_power_I0.idleReq				Output	
Bit	1	Internal	tfsm_uart1_uartirdacirintrconn_power_I0.SidleAck	1			Input	
Bit	2	Internal	tfsm_uart1_uartirdacirintrconn_power_I0.module_swakeup	0			Input	
Bit	3	Internal	tfsm_uart1_uartirdacirintrconn_power_I0.fclken_IP				Output	
Bit	4	Internal	tfsm_uart2_uartirdacirintrconn_power_I0.idleReq				Output	
Bit	5	Internal	tfsm_uart2_uartirdacirintrconn_power_I0.SidleAck	1			Input	
Bit	6	Internal	tfsm_uart2_uartirdacirintrconn_power_I0.module_swakeup	0			Input	
Bit	7	Internal	tfsm_uart2_uartirdacirintrconn_power_I0.fclken_IP				Output	
Byte	0x52	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	tfsm_uart3_uartirdacirintrconn_power_I0.idleReq				Output	
Bit	1	Internal	tfsm_uart3_uartirdacirintrconn_power_I0.SidleAck	1			Input	
Bit	2	Internal	tfsm_uart3_uartirdacirintrconn_power_I0.module_swakeup	0			Input	
Bit	3	Internal	tfsm_uart3_uartirdacirintrconn_power_I0.fclken_IP				Output	
Bit	4	Internal	tfsm_uart4_uartirdacirintrconn_power_I0.idleReq				Output	
Bit	5	Internal	tfsm_uart4_uartirdacirintrconn_power_I0.SidleAck	1			Input	
Bit	6	Internal	tfsm_uart4_uartirdacirintrconn_power_I0.module_swakeup	0			Input	
Bit	7	Internal	tfsm_uart4_uartirdacirintrconn_power_I0.fclken_IP				Output	
Byte	0x53	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	3:0		Reserved					
Bit	4	Internal	tfsm_usb_host_fs_idle_prot_I0.idleReq				Output	

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Table 18-39. CM2 Observable Signals (continued)

Bit	5	Internal	tfsm_usb_host_fs_idle_prot_I0.SidleAck	1			Input	
Bit	6	Internal	tfsm_usb_host_fs_idle_prot_I0.module_swakeup	0			Input	
Bit	7	Internal	tfsm_usb_host_fs_idle_prot_I0.fclken_IP				Output	
Byte	0x54	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	tfsm_usb_host_usbhosths_intrconn_regif_pwr_I0.idleReq				Output	
Bit	1	Internal	tfsm_usb_host_usbhosths_intrconn_regif_pwr_I0.SidleAck	1			Input	
Bit	2	Internal	tfsm_usb_host_usbhosths_intrconn_regif_pwr_I0.module_swakeup	0			Input	
Bit	3	Internal	tfsm_usb_host_usbhosths_intrconn_regif_pwr_I0.fclken_IP				Output	
Bit	4	Internal	tfsm_usb_otg_usbotghs_intrconn_slave_I0.idleReq				Output	
Bit	5	Internal	tfsm_usb_otg_usbotghs_intrconn_slave_I0.SidleAck	1			Input	
Bit	6	Internal	tfsm_usb_otg_usbotghs_intrconn_slave_I0.module_swakeup	0			Input	
Bit	7	Internal	tfsm_usb_otg_usbotghs_intrconn_slave_I0.fclken_IP				Output	
Byte	0x55	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	tfsm_usb_tll_usb_tll_power_I0.idleReq				Output	
Bit	1	Internal	tfsm_usb_tll_usb_tll_power_I0.SidleAck	1			Input	
Bit	2	Internal	tfsm_usb_tll_usb_tll_power_I0.module_swakeup	0			Input	
Bit	3	Internal	tfsm_usb_tll_usb_tll_power_I0.fclken_IP				Output	
Bit	4	Internal	tfsm_usbphyintrconn2scp_idle_prot_I0.idleReq				Output	
Bit	5	Internal	tfsm_usbphyintrconn2scp_idle_prot_I0.SidleAck	1			Input	
Bit	6	Internal	tfsm_usbphyintrconn2scp_idle_prot_I0.module_swakeup	0			Input	
Bit	7	Internal	tfsm_usbphyintrconn2scp_idle_prot_I0.fclken_IP				Output	
Byte	0x56	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	tfsm_xhpi_hpi_idle_I0.idleReq				Output	
Bit	1	Internal	tfsm_xhpi_hpi_idle_I0.SidleAck	1			Input	
Bit	2	Internal	tfsm_xhpi_hpi_idle_I0.module_swakeup	0			Input	
Bit	3	Internal	tfsm_xhpi_hpi_idle_I0.fclken_IP				Output	
Bit	7:4		Reserved					
Byte	0x57	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	dpllsctrl_dpll_per_I0.DPLLCtrlState	0	LSB		Output	
Bit	1	Internal	dpllsctrl_dpll_per_I0.DPLLCtrlState	1			Output	
Bit	2	Internal	dpllsctrl_dpll_per_I0.DPLLCtrlState	2			Output	
Bit	3	Internal	dpllsctrl_dpll_per_I0.DPLLCtrlState	3			Output	
Bit	4	Internal	dpllsctrl_dpll_per_I0.DPLLCtrlState	4			Output	
Bit	5	Internal	dpllsctrl_dpll_per_I0.DPLLCtrlState	5			Output	
Bit	6	Internal	dpllsctrl_dpll_per_I0.DPLLCtrlState	6			Output	
Bit	7	Internal	dpllsctrl_dpll_per_I0.DPLLCtrlState	7	MSB		Output	
Byte	0x58	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	dpllsctrl_dpll_per_I0.freqChgReqAck				Input	
Bit	1	Internal	dpllsctrl_dpll_per_I0.freqChgReq				Output	
Bit	2	Internal	dpllsctrl_dpll_per_I0.freqChgReqAck2				Output	
Bit	3	Internal	dpllsctrl_dpll_per_I0.freqChgReq2				Input	
Bit	4	Internal	dpllsctrl_dpll_per_I0.bypass				Input	
Bit	5	Internal	dpllsctrl_dpll_per_I0.freqlock				Input	
Bit	6	Internal	dpllsctrl_dpll_per_I0.lossref				Input	
Bit	7	Internal	dpllsctrl_dpll_per_I0.tinitz				Output	
Byte	0x59	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments

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Table 18-39. CM2 Observable Signals (continued)

Bit	0	Internal	dpllsctrl_dpll_per_I0.tenable				Output	
Bit	1	Internal	dpllsctrl_dpll_per_I0.tenablediv				Output	
Bit	2	Internal	dpllsctrl_dpll_per_I0.idle				Output	
Bit	3	Internal	dpllsctrl_dpll_per_I0.lowcurrstdby				Output	
Bit	4	Internal	dpllsctrl_dpll_per_I0.dpll_ticopwdn				Input	
Bit	5	Internal	dpllsctrl_dpll_per_I0.dpll_ldopwdn				Input	
Bit	6	Internal	dpllsctrl_dpll_per_I0.ulowclken	0			Output	
Bit	7	Internal	dpllsctrl_dpll_per_I0.dpll_clkbypselacksel	0			Input	
Byte	0x5a	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	dpllsctrl_dpll_per_I0.clkinpIsRunning				Input	
Bit	1	Internal	dpllsctrl_dpll_per_I0.clkinpToBeGated				Output	
Bit	2	Internal	dpllsctrl_dpll_per_I0.clkinplowIsRunning				Input	
Bit	3	Internal	dpllsctrl_dpll_per_I0.clkinplowToBeGated				Output	
Bit	7:4		Reserved					
Byte	0x5b	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	7:0		Reserved					
Byte	0x5c	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	7:0		Reserved					
Byte	0x5d	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	7:0		Reserved					
Byte	0x5e	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	dpllsctrl_dpll_usb_I0.DPLLCtrlState	0	LSB		Output	
Bit	1	Internal	dpllsctrl_dpll_usb_I0.DPLLCtrlState	1			Output	
Bit	2	Internal	dpllsctrl_dpll_usb_I0.DPLLCtrlState	2			Output	
Bit	3	Internal	dpllsctrl_dpll_usb_I0.DPLLCtrlState	3			Output	
Bit	4	Internal	dpllsctrl_dpll_usb_I0.DPLLCtrlState	4			Output	
Bit	5	Internal	dpllsctrl_dpll_usb_I0.DPLLCtrlState	5			Output	
Bit	6	Internal	dpllsctrl_dpll_usb_I0.DPLLCtrlState	6			Output	
Bit	7	Internal	dpllsctrl_dpll_usb_I0.DPLLCtrlState	7	MSB		Output	
Byte	0x5f	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	dpllsctrl_dpll_usb_I0.freqChgReqAck				Input	
Bit	1	Internal	dpllsctrl_dpll_usb_I0.freqChgReq				Output	
Bit	2	Internal	dpllsctrl_dpll_usb_I0.freqChgReqAck2				Output	
Bit	3	Internal	dpllsctrl_dpll_usb_I0.freqChgReq2				Input	
Bit	4	Internal	dpllsctrl_dpll_usb_I0.bypass				Input	
Bit	5	Internal	dpllsctrl_dpll_usb_I0.freqlock				Input	
Bit	6	Internal	dpllsctrl_dpll_usb_I0.lossref				Input	
Bit	7	Internal	dpllsctrl_dpll_usb_I0.tinitz				Output	
Byte	0x60	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	dpllsctrl_dpll_usb_I0.tenable				Output	
Bit	1	Internal	dpllsctrl_dpll_usb_I0.tenablediv				Output	
Bit	2	Internal	dpllsctrl_dpll_usb_I0.idle				Output	
Bit	3	Internal	dpllsctrl_dpll_usb_I0.dpll_ticopwdn				Input	
Bit	4	Internal	dpllsctrl_dpll_usb_I0.dpll_ldopwdn				Input	
Bit	5	Internal	dpllsctrl_dpll_usb_I0.ulowclken	0			Output	
Bit	6	Internal	dpllsctrl_dpll_usb_I0.dpll_clkbypselacksel	0			Input	
Bit	7	Internal	dpllsctrl_dpll_usb_I0.clkinpIsRunning				Input	
Byte	0x61	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments

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Table 18-39. CM2 Observable Signals (continued)

Bit	0	Internal	dpllsctrl_dpll_usb_I0.clkinpToBeGated				Output	
Bit	1	Internal	dpllsctrl_dpll_usb_I0.clkinplowIsRunning				Input	
Bit	2	Internal	dpllsctrl_dpll_usb_I0.clkinplowToBeGated				Output	
Bit	3	Internal	mutegen_ccptx_I0.dyn_domain_mute				Output	
Bit	4	Internal	mutegen_ccptx_I0.static_domain_mute				Output	
Bit	5	Internal	mutegen_ccptx_I0.public_active	0			Input	
Bit	7:6		Reserved					
Byte	0x62	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	7:0		Reserved					
Byte	0x63	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	mutegen_deiss_I0.dyn_domain_mute				Output	
Bit	1	Internal	mutegen_deiss_I0.static_domain_mute				Output	
Bit	2	Internal	mutegen_deiss_I0.public_active	0			Input	
Bit	3	Internal	mutegen_dss_I0.dyn_domain_mute				Output	
Bit	4	Internal	mutegen_dss_I0.static_domain_mute				Output	
Bit	5	Internal	mutegen_dss_I0.public_active	0			Input	
Bit	7:6		reserved					
Byte	0x64	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	mutegen_cortex_m3_to_l3_interconnect_2_I0.dyn_domain_mute				Output	
Bit	1	Internal	mutegen_cortex_m3_to_l3_interconnect_2_I0.static_domain_mute				Output	
Bit	2	Internal	mutegen_cortex_m3_to_l3_interconnect_2_I0.public_active	0			Input	
Bit	3	Internal	mutegen_emac_I0.dyn_domain_mute				Output	
Bit	4	Internal	mutegen_emac_I0.static_domain_mute				Output	
Bit	5	Internal	mutegen_emac_I0.public_active	0			Input	
Bit	7:6		Reserved					
Byte	0x65	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	mutegen_fdif_I0.dyn_domain_mute				Output	
Bit	1	Internal	mutegen_fdif_I0.static_domain_mute				Output	
Bit	2	Internal	mutegen_fdif_I0.public_active	0			Input	
Bit	3	Internal	mutegen_gfx_I0.dyn_domain_mute				Output	
Bit	4	Internal	mutegen_gfx_I0.static_domain_mute				Output	
Bit	5	Internal	mutegen_gfx_I0.public_active	0			Input	
Bit	7:6		Reserved					
Byte	0x66	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	mutegen_hsi_I0.dyn_domain_mute				Output	
Bit	1	Internal	mutegen_hsi_I0.static_domain_mute				Output	
Bit	2	Internal	mutegen_hsi_I0.public_active	0			Input	
Bit	3	Internal	mutegen_iss_I0.dyn_domain_mute				Output	
Bit	4	Internal	mutegen_iss_I0.static_domain_mute				Output	
Bit	5	Internal	mutegen_iss_I0.public_active	0			Input	
Bit	7:6		Reserved					
Byte	0x67	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	mutegen_ivahd_I0.dyn_domain_mute				Output	
Bit	1	Internal	mutegen_ivahd_I0.static_domain_mute				Output	
Bit	2	Internal	mutegen_ivahd_I0.public_active	0			Input	
Bit	3	Internal	mutegen_l3_interconnect_1_all_ta_to_dmm_I0.dyn_domain_mute				Output	

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Table 18-39. CM2 Observable Signals (continued)

Bit	4	Internal	mutegen_l3_interconnect_1_all_ta_to_dmm_I0.static_domain_mute				Output	
Bit	5	Internal	mutegen_l3_interconnect_1_all_ta_to_dmm_I0.public_active	0			Input	
Bit	7:6		Reserved					
Byte	0x68	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	mutegen_l3_interconnect_1_to_dmm_I0.dyn_domain_mute				Output	
Bit	1	Internal	mutegen_l3_interconnect_1_to_dmm_I0.static_domain_mute				Output	
Bit	2	Internal	mutegen_l3_interconnect_1_to_dmm_I0.public_active	0			Input	
Bit	3	Internal	mutegen_l3_interconnect_1_to_l3_interconnect_2_I0.dyn_domain_mute				Output	
Bit	4	Internal	mutegen_l3_interconnect_1_to_l3_interconnect_2_I0.static_domain_mute				Output	
Bit	5	Internal	mutegen_l3_interconnect_1_to_l3_interconnect_2_I0.public_active	0			Input	
Bit	7:6		Reserved					
Byte	0x69	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	mutegen_l3_interconnect_1_to_l4_audio_interconnect_I0.dyn_domain_mute				Output	
Bit	1	Internal	mutegen_l3_interconnect_1_to_l4_audio_interconnect_I0.static_domain_mute				Output	
Bit	2	Internal	mutegen_l3_interconnect_1_to_l4_audio_interconnect_I0.public_active	0			Input	
Bit	3	Internal	mutegen_l3_interconnect_1_to_l4_cfg_interconnect_I0.dyn_domain_mute				Output	
Bit	4	Internal	mutegen_l3_interconnect_1_to_l4_cfg_interconnect_I0.static_domain_mute				Output	
Bit	5	Internal	mutegen_l3_interconnect_1_to_l4_cfg_interconnect_I0.public_active	0			Input	
Bit	7:6		Reserved					
Byte	0x6a	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	7:0		Reserved					
Byte	0x6b	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	mutegen_l3_interconnect_2_to_dss_I0.dyn_domain_mute				Output	
Bit	1	Internal	mutegen_l3_interconnect_2_to_dss_I0.static_domain_mute				Output	
Bit	2	Internal	mutegen_l3_interconnect_2_to_dss_I0.public_active	0			Input	
Bit	3	Internal	mutegen_l3_interconnect_2_to_cortex_m3_I0.dyn_domain_mute				Output	
Bit	4	Internal	mutegen_l3_interconnect_2_to_cortex_m3_I0.static_domain_mute				Output	
Bit	5	Internal	mutegen_l3_interconnect_2_to_cortex_m3_I0.public_active	0			Input	
Bit	7:6		Reserved					
Byte	0x6c	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	mutegen_l3_interconnect_2_to_gfx_I0.dyn_domain_mute				Output	
Bit	1	Internal	mutegen_l3_interconnect_2_to_gfx_I0.static_domain_mute				Output	
Bit	2	Internal	mutegen_l3_interconnect_2_to_gfx_I0.public_active	0			Input	
Bit	3	Internal	mutegen_l3_interconnect_2_to_ivahd_I0.dyn_domain_mute				Output	
Bit	4	Internal	mutegen_l3_interconnect_2_to_ivahd_I0.static_domain_mute				Output	

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Table 18-39. CM2 Observable Signals (continued)

Bit	5	Internal	mutegen_l3_interconnect_2_to_ivahd_l0.public_active	0			Input	
Bit	7:6		Reserved					
Byte	0x6d	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	mutegen_l3_interconnect_2_to_l3_interconnect_1_l0.dyn_domain_mute				Output	
Bit	1	Internal	mutegen_l3_interconnect_2_to_l3_interconnect_1_l0.static_domain_mute				Output	
Bit	2	Internal	mutegen_l3_interconnect_2_to_l3_interconnect_1_l0.public_active	0			Input	
Bit	3	Internal	mutegen_l3_interconnect_2_to_l4_per_interconnect_l0.dyn_domain_mute				Output	
Bit	4	Internal	mutegen_l3_interconnect_2_to_l4_per_interconnect_l0.static_domain_mute				Output	
Bit	5	Internal	mutegen_l3_interconnect_2_to_l4_per_interconnect_l0.public_active	0			Input	
Bit	7:6		Reserved					
Byte	0x6e	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	2:0		reserved					
Bit	3	Internal	mutegen_l3_interconnect_2_to_sad2d_l0.dyn_domain_mute				Output	
Bit	4	Internal	mutegen_l3_interconnect_2_to_sad2d_l0.static_domain_mute				Output	
Bit	5	Internal	mutegen_l3_interconnect_2_to_sad2d_l0.public_active	0			Input	
Bit	7:6		Reserved					
Byte	0x6f	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	2:0		Reserved					
Bit	3	Internal	mutegen_l3_interconnect_2_to_sl2_l0.dyn_domain_mute				Output	
Bit	4	Internal	mutegen_l3_interconnect_2_to_sl2_l0.static_domain_mute				Output	
Bit	5	Internal	mutegen_l3_interconnect_2_to_sl2_l0.public_active	0			Input	
Bit	7:6		Reserved					
Byte	0x70	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	mutegen_l3_interconnect_2_to_tppss_l0.dyn_domain_mute				Output	
Bit	1	Internal	mutegen_l3_interconnect_2_to_tppss_l0.static_domain_mute				Output	
Bit	2	Internal	mutegen_l3_interconnect_2_to_tppss_l0.public_active	0			Input	
Bit	3	Internal	mutegen_l4_cfg_interconnect_all_ta_to_l3_interconnect_2_l0.dyn_domain_mute				Output	
Bit	4	Internal	mutegen_l4_cfg_interconnect_all_ta_to_l3_interconnect_2_l0.static_domain_mute				Output	
Bit	5	Internal	mutegen_l4_cfg_interconnect_all_ta_to_l3_interconnect_2_l0.public_active	0			Input	
Bit	7:6		Reserved					
Byte	0x71	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	mutegen_l4_cfg_interconnect_all_ta_to_l3_interconnect_2_l1.dyn_domain_mute				Output	
Bit	1	Internal	mutegen_l4_cfg_interconnect_all_ta_to_l3_interconnect_2_l1.static_domain_mute				Output	
Bit	2	Internal	mutegen_l4_cfg_interconnect_all_ta_to_l3_interconnect_2_l1.public_active	0			Input	
Bit	3	Internal	mutegen_l4_cfg_interconnect_all_ta_to_l3_interconnect_2_l2.dyn_domain_mute				Output	

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Table 18-39. CM2 Observable Signals (continued)

Bit	4	Internal	mutegen_l4_cfg_interconnect_all_ta_to_l3_interconnect_2_I2.static_domain_mute				Output	
Bit	5	Internal	mutegen_l4_cfg_interconnect_all_ta_to_l3_interconnect_2_I2.public_active	0			Input	
Bit	7:6		Reserved					
Byte	0x72	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	mutegen_l4_cfg_interconnect_all_ta_to_l3_interconnect_2_I3.dyn_domain_mute				Output	
Bit	1	Internal	mutegen_l4_cfg_interconnect_all_ta_to_l3_interconnect_2_I3.static_domain_mute				Output	
Bit	2	Internal	mutegen_l4_cfg_interconnect_all_ta_to_l3_interconnect_2_I3.public_active	0			Input	
Bit	3	Internal	mutegen_l4_cfg_interconnect_all_ta_to_l3_interconnect_2_I4.dyn_domain_mute				Output	
Bit	4	Internal	mutegen_l4_cfg_interconnect_all_ta_to_l3_interconnect_2_I4.static_domain_mute				Output	
Bit	5	Internal	mutegen_l4_cfg_interconnect_all_ta_to_l3_interconnect_2_I4.public_active	0			Input	
Bit	7:6		Reserved					
Byte	0x73	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	mutegen_l4_cfg_interconnect_all_ta_to_l3_interconnect_2_I5.dyn_domain_mute				Output	
Bit	1	Internal	mutegen_l4_cfg_interconnect_all_ta_to_l3_interconnect_2_I5.static_domain_mute				Output	
Bit	2	Internal	mutegen_l4_cfg_interconnect_all_ta_to_l3_interconnect_2_I5.public_active	0			Input	
Bit	3	Internal	mutegen_l4_cfg_interconnect_all_ta_to_l3_interconnect_2_I6.dyn_domain_mute				Output	
Bit	4	Internal	mutegen_l4_cfg_interconnect_all_ta_to_l3_interconnect_2_I6.static_domain_mute				Output	
Bit	5	Internal	mutegen_l4_cfg_interconnect_all_ta_to_l3_interconnect_2_I6.public_active	0			Input	
Bit	7:6		Reserved					
Byte	0x74	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	mutegen_l4_cfg_interconnect_all_ta_to_l3_interconnect_2_I7.dyn_domain_mute				Output	
Bit	1	Internal	mutegen_l4_cfg_interconnect_all_ta_to_l3_interconnect_2_I7.static_domain_mute				Output	
Bit	2	Internal	mutegen_l4_cfg_interconnect_all_ta_to_l3_interconnect_2_I7.public_active	0			Input	
Bit	3	Internal	mutegen_l4_cfg_interconnect_all_ta_to_l3_interconnect_2_I8.dyn_domain_mute				Output	
Bit	4	Internal	mutegen_l4_cfg_interconnect_all_ta_to_l3_interconnect_2_I8.static_domain_mute				Output	
Bit	5	Internal	mutegen_l4_cfg_interconnect_all_ta_to_l3_interconnect_2_I8.public_active	0			Input	
Bit	7:6		Reserved					
Byte	0x75	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	mutegen_l4_cfg_interconnect_all_ta_to_l3_interconnect_2_I9.dyn_domain_mute				Output	
Bit	1	Internal	mutegen_l4_cfg_interconnect_all_ta_to_l3_interconnect_2_I9.static_domain_mute				Output	
Bit	2	Internal	mutegen_l4_cfg_interconnect_all_ta_to_l3_interconnect_2_I9.public_active	0			Input	
Bit	3	Internal	mutegen_l4_cfg_interconnect_all_ta_to_modem_icr_I0.dyn_domain_mute				Output	

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Table 18-39. CM2 Observable Signals (continued)

Bit	4	Internal	mutegen_l4_cfg_interconnect_all_ta_to_modem_icr_I0.static_domain_mute				Output	
Bit	5	Internal	mutegen_l4_cfg_interconnect_all_ta_to_modem_icr_I0.public_active	0			Input	
Bit	7:6		Reserved					
Byte	0x76	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	mutegen_l4_cfg_interconnect_to_ccptx_I0.dyn_domain_mute				Output	
Bit	1	Internal	mutegen_l4_cfg_interconnect_to_ccptx_I0.static_domain_mute				Output	
Bit	2	Internal	mutegen_l4_cfg_interconnect_to_ccptx_I0.public_active	0			Input	
Bit	7:3		Reserved					
Byte	0x77	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	mutegen_l4_cfg_interconnect_to_deiss_I0.dyn_domain_mute				Output	
Bit	1	Internal	mutegen_l4_cfg_interconnect_to_deiss_I0.static_domain_mute				Output	
Bit	2	Internal	mutegen_l4_cfg_interconnect_to_deiss_I0.public_active	0			Input	
Bit	3	Internal	mutegen_l4_cfg_interconnect_to_emac_I0.dyn_domain_mute				Output	
Bit	4	Internal	mutegen_l4_cfg_interconnect_to_emac_I0.static_domain_mute				Output	
Bit	5	Internal	mutegen_l4_cfg_interconnect_to_emac_I0.public_active	0			Input	
Bit	7:6		Reserved					
Byte	0x78	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	mutegen_l4_cfg_interconnect_to_emif_fw_I0.dyn_domain_mute				Output	
Bit	1	Internal	mutegen_l4_cfg_interconnect_to_emif_fw_I0.static_domain_mute				Output	
Bit	2	Internal	mutegen_l4_cfg_interconnect_to_emif_fw_I0.public_active	0			Input	
Bit	3	Internal	mutegen_l4_cfg_interconnect_to_hsi_I0.dyn_domain_mute				Output	
Bit	4	Internal	mutegen_l4_cfg_interconnect_to_hsi_I0.static_domain_mute				Output	
Bit	5	Internal	mutegen_l4_cfg_interconnect_to_hsi_I0.public_active	0			Input	
Bit	7:6		Reserved					
Byte	0x79	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	mutegen_l4_cfg_interconnect_to_l3_interconnect_1_I0.dyn_domain_mute				Output	
Bit	1	Internal	mutegen_l4_cfg_interconnect_to_l3_interconnect_1_I0.static_domain_mute				Output	
Bit	2	Internal	mutegen_l4_cfg_interconnect_to_l3_interconnect_1_I0.public_active	0			Input	
Bit	3	Internal	mutegen_l4_cfg_interconnect_to_l3_interconnect_2_I0.dyn_domain_mute				Output	
Bit	4	Internal	mutegen_l4_cfg_interconnect_to_l3_interconnect_2_I0.static_domain_mute				Output	
Bit	5	Internal	mutegen_l4_cfg_interconnect_to_l3_interconnect_2_I0.public_active	0			Input	
Bit	7:6		Reserved					
Byte	0x7a	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	mutegen_l4_cfg_interconnect_to_modem_icr_I0.dyn_domain_mute				Output	
Bit	1	Internal	mutegen_l4_cfg_interconnect_to_modem_icr_I0.static_domain_mute				Output	

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Table 18-39. CM2 Observable Signals (continued)

Bit	2	Internal	mutegen_l4_cfg_interconnect_to_modem_icr_I0.public_active	0			Input	
Bit	3	Internal	mutegen_l4_cfg_interconnect_to_modem_intc_I0.dyn_domain_mute				Output	
Bit	4	Internal	mutegen_l4_cfg_interconnect_to_modem_intc_I0.static_domain_mute				Output	
Bit	5	Internal	mutegen_l4_cfg_interconnect_to_modem_intc_I0.public_active	0			Input	
Bit	7:6		Reserved					
Byte	0x7b	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	7:0		Reserved					
Byte	0x7c	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	mutegen_l4_cfg_interconnect_to_sad2d_fw_I0.dyn_domain_mute				Output	
	1	Internal	mutegen_l4_cfg_interconnect_to_sad2d_fw_I0.static_domain_mute				Output	
	2	Internal	mutegen_l4_cfg_interconnect_to_sad2d_fw_I0.public_active				Input	
Bit	7:3		Reserved					
Byte	0x7d	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	mutegen_l4_cfg_interconnect_to_sdma_I0.dyn_domain_mute				Output	
Bit	1	Internal	mutegen_l4_cfg_interconnect_to_sdma_I0.static_domain_mute				Output	
Bit	2	Internal	mutegen_l4_cfg_interconnect_to_sdma_I0.public_active	0			Input	
Bit	3	Internal	mutegen_l4_cfg_interconnect_to_smartreflex_core_I0.dyn_domain_mute				Output	
Bit	4	Internal	mutegen_l4_cfg_interconnect_to_smartreflex_core_I0.static_domain_mute				Output	
Bit	5	Internal	mutegen_l4_cfg_interconnect_to_smartreflex_core_I0.public_active	0			Input	
Bit	7:6		Reserved					
Byte	0x7e	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	mutegen_l4_cfg_interconnect_to_smartreflex_iva_I0.dyn_domain_mute				Output	
Bit	1	Internal	mutegen_l4_cfg_interconnect_to_smartreflex_iva_I0.static_domain_mute				Output	
Bit	2	Internal	mutegen_l4_cfg_interconnect_to_smartreflex_iva_I0.public_active	0			Input	
Bit	3	Internal	mutegen_l4_cfg_interconnect_to_smartreflex_mpu_I0.dyn_domain_mute				Output	
Bit	4	Internal	mutegen_l4_cfg_interconnect_to_smartreflex_mpu_I0.static_domain_mute				Output	
Bit	5	Internal	mutegen_l4_cfg_interconnect_to_smartreflex_mpu_I0.public_active	0			Input	
Bit	7:6		Reserved					
Byte	0x7f	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	mutegen_l4_cfg_interconnect_to_dspss_I0.dyn_domain_mute				Output	
Bit	1	Internal	mutegen_l4_cfg_interconnect_to_dspss_I0.static_domain_mute				Output	
Bit	2	Internal	mutegen_l4_cfg_interconnect_to_dspss_I0.public_active	0			Input	
Bit	3	Internal	mutegen_l4_cfg_interconnect_to_tppss_I0.dyn_domain_mute				Output	

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Table 18-39. CM2 Observable Signals (continued)

Bit	4	Internal	mutegen_l4_cfg_interconnect_to_tppss_I0.static_domain_mute				Output	
Bit	5	Internal	mutegen_l4_cfg_interconnect_to_tppss_I0.public_active	0			Input	
Bit	7:6		Reserved					
Byte	0x80	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	2:0		Reserved					
Bit	3	Internal	mutegen_l4_cfg_interconnect_to_usb_host_I0.dyn_domain_mute				Output	
Bit	4	Internal	mutegen_l4_cfg_interconnect_to_usb_host_I0.static_domain_mute				Output	
Bit	5	Internal	mutegen_l4_cfg_interconnect_to_usb_host_I0.public_active	0			Input	
Bit	7:6		Reserved					
Byte	0x81	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	mutegen_l4_cfg_interconnect_to_usb_host_fs_I0.dyn_domain_mute				Output	
Bit	1	Internal	mutegen_l4_cfg_interconnect_to_usb_host_fs_I0.static_domain_mute				Output	
Bit	2	Internal	mutegen_l4_cfg_interconnect_to_usb_host_fs_I0.public_active	0			Input	
Bit	3	Internal	mutegen_l4_cfg_interconnect_to_usb_otg_I0.dyn_domain_mute				Output	
Bit	4	Internal	mutegen_l4_cfg_interconnect_to_usb_otg_I0.static_domain_mute				Output	
Bit	5	Internal	mutegen_l4_cfg_interconnect_to_usb_otg_I0.public_active	0			Input	
Bit	7:6		Reserved					
Byte	0x82	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	mutegen_l4_cfg_interconnect_to_usb_tll_I0.dyn_domain_mute				Output	
Bit	1	Internal	mutegen_l4_cfg_interconnect_to_usb_tll_I0.static_domain_mute				Output	
Bit	2	Internal	mutegen_l4_cfg_interconnect_to_usb_tll_I0.public_active	0			Input	
Bit	3	Internal	mutegen_l4_cfg_interconnect_to_usbphyintrconn2scp_I0.dyn_domain_mute				Output	
Bit	4	Internal	mutegen_l4_cfg_interconnect_to_usbphyintrconn2scp_I0.static_domain_mute				Output	
Bit	5	Internal	mutegen_l4_cfg_interconnect_to_usbphyintrconn2scp_I0.public_active	0			Input	
Bit	7:6		Reserved					
Byte	0x83	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	mutegen_l4_cfg_interconnect_to_wkup_l4_interconnect_I0.dyn_domain_mute				Output	
Bit	1	Internal	mutegen_l4_cfg_interconnect_to_wkup_l4_interconnect_I0.static_domain_mute				Output	
Bit	2	Internal	mutegen_l4_cfg_interconnect_to_wkup_l4_interconnect_I0.public_active	0			Input	
Bit	3	Internal	mutegen_l4_cfg_interconnect_to_xhpi_I0.dyn_domain_mute				Output	
Bit	4	Internal	mutegen_l4_cfg_interconnect_to_xhpi_I0.static_domain_mute				Output	
Bit	5	Internal	mutegen_l4_cfg_interconnect_to_xhpi_I0.public_active	0			Input	
Bit	7:6		Reserved					
Byte	0x84	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	7:0		Reserved					

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Table 18-39. CM2 Observable Signals (continued)

Byte	0x85	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	mutegen_l4_per_interconnect_to_dss_I0.dyn_domain_mute				Output	
Bit	1	Internal	mutegen_l4_per_interconnect_to_dss_I0.static_domain_mute				Output	
Bit	2	Internal	mutegen_l4_per_interconnect_to_dss_I0.public_active	0			Input	
Bit	3	Internal	mutegen_l4_per_interconnect_to_mmc1_I0.dyn_domain_mute				Output	
Bit	4	Internal	mutegen_l4_per_interconnect_to_mmc1_I0.static_domain_mute				Output	
Bit	5	Internal	mutegen_l4_per_interconnect_to_mmc1_I0.public_active	0			Input	
Bit	7:6		Reserved					
Byte	0x86	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	mutegen_l4_per_interconnect_to_mmc2_I0.dyn_domain_mute				Output	
Bit	1	Internal	mutegen_l4_per_interconnect_to_mmc2_I0.static_domain_mute				Output	
Bit	2	Internal	mutegen_l4_per_interconnect_to_mmc2_I0.public_active	0			Input	
Bit	7:3		Reserved					
Byte	0x87	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	mutegen_l4_per_interconnect_to_pkaeip29_I0.dyn_domain_mute				Output	
Bit	1	Internal	mutegen_l4_per_interconnect_to_pkaeip29_I0.static_domain_mute				Output	
Bit	2	Internal	mutegen_l4_per_interconnect_to_pkaeip29_I0.public_active	0			Input	
Bit	3	Internal	mutegen_l4_per_interconnect_to_rng_I0.dyn_domain_mute				Output	
Bit	4	Internal	mutegen_l4_per_interconnect_to_rng_I0.static_domain_mute				Output	
Bit	5	Internal	mutegen_l4_per_interconnect_to_rng_I0.public_active	0			Input	
Bit	7:6		Reserved					
Byte	0x88	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	mutegen_mmc1_I0.dyn_domain_mute				Output	
Bit	1	Internal	mutegen_mmc1_I0.static_domain_mute				Output	
Bit	2	Internal	mutegen_mmc1_I0.public_active	0			Input	
Bit	3	Internal	mutegen_mmc2_I0.dyn_domain_mute				Output	
Bit	4	Internal	mutegen_mmc2_I0.static_domain_mute				Output	
Bit	5	Internal	mutegen_mmc2_I0.public_active	0			Input	
Bit	7:6		Reserved					
Byte	0x89	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	mutegen_mmc6_I0.dyn_domain_mute				Output	
Bit	1	Internal	mutegen_mmc6_I0.static_domain_mute				Output	
Bit	2	Internal	mutegen_mmc6_I0.public_active	0			Input	
Bit	3	Internal	mutegen_p1500_I0.dyn_domain_mute				Output	
Bit	4	Internal	mutegen_p1500_I0.static_domain_mute				Output	
Bit	5	Internal	mutegen_p1500_I0.public_active	0			Input	
Bit	7:6		Reserved					
Byte	0x8a	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	mutegen_pciess_I0.dyn_domain_mute				Output	
Bit	1	Internal	mutegen_pciess_I0.static_domain_mute				Output	
Bit	2	Internal	mutegen_pciess_I0.public_active	0			Input	

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Table 18-39. CM2 Observable Signals (continued)

Bit	3	Internal	mutegen_sad2d_I0.dyn_domain_mute				Output	
Bit	4	Internal	mutegen_sad2d_I0.static_domain_mute				Output	
Bit	5	Internal	mutegen_sad2d_I0.public_active	0			Input	
Bit	7:6		Reserved					
Byte	0x8b	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	mutegen_sad2d_fw_to_l3_interconnect_2_I0.dyn_domain_mute				Output	
Bit	1	Internal	mutegen_sad2d_fw_to_l3_interconnect_2_I0.static_domain_mute				Output	
Bit	2	Internal	mutegen_sad2d_fw_to_l3_interconnect_2_I0.public_active	0			Input	
Bit	3	Internal	mutegen_sad2d_to_emif_fw_I0.dyn_domain_mute				Output	
Bit	4	Internal	mutegen_sad2d_to_emif_fw_I0.static_domain_mute				Output	
Bit	5	Internal	mutegen_sad2d_to_emif_fw_I0.public_active	0			Input	
Bit	7:6		Reserved					
Byte	0x8c	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	2:0		reserved					
Bit	3	Internal	mutegen_sdma_I0.dyn_domain_mute				Output	
Bit	4	Internal	mutegen_sdma_I0.static_domain_mute				Output	
Bit	5	Internal	mutegen_sdma_I0.public_active	0			Input	
Bit	7:6		Reserved					
Byte	0x8d	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	mutegen_sdma_write_port_I0.dyn_domain_mute				Output	
Bit	1	Internal	mutegen_sdma_write_port_I0.static_domain_mute				Output	
Bit	2	Internal	mutegen_sdma_write_port_I0.public_active	0			Input	
Bit	3	Internal	mutegen_tppss_I0.dyn_domain_mute				Output	
Bit	4	Internal	mutegen_tppss_I0.static_domain_mute				Output	
Bit	5	Internal	mutegen_tppss_I0.public_active	0			Input	
Bit	7:6		Reserved					
Byte	0x8e	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	2:0		reserved					
Bit	3	Internal	mutegen_usb_host_I0.dyn_domain_mute				Output	
Bit	4	Internal	mutegen_usb_host_I0.static_domain_mute				Output	
Bit	5	Internal	mutegen_usb_host_I0.public_active	0			Input	
Bit	7:6		Reserved					
Byte	0x8f	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	mutegen_usb_host_fs_I0.dyn_domain_mute				Output	
Bit	1	Internal	mutegen_usb_host_fs_I0.static_domain_mute				Output	
Bit	2	Internal	mutegen_usb_host_fs_I0.public_active	0			Input	
Bit	3	Internal	mutegen_usb_otg_I0.dyn_domain_mute				Output	
Bit	4	Internal	mutegen_usb_otg_I0.static_domain_mute				Output	
Bit	5	Internal	mutegen_usb_otg_I0.public_active	0			Input	
Bit	7:6		Reserved					
Byte	0x90	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	mutegen_xhpi_I0.dyn_domain_mute				Output	
Bit	1	Internal	mutegen_xhpi_I0.static_domain_mute				Output	
Bit	2	Internal	mutegen_xhpi_I0.public_active	0			Input	
Bit	7:3		Reserved					
Byte	0x91	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	cmfsm_always_on_core_l4_ao_I0.domain_is_on				Input	

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Table 18-39. CM2 Observable Signals (continued)

Bit	1	Internal	cmfsm_always_on_core_l4_ao_l0.domain_wakeup				Input	
Bit	2	Internal	cmfsm_always_on_core_l4_ao_l0.domain_wkup_ack				Output	
Bit	3	Internal	cmfsm_always_on_core_l4_ao_l0.fsm_state	0	LSB		Output	ACT2INACT2 = "101"
Bit	4	Internal	cmfsm_always_on_core_l4_ao_l0.fsm_state	1			Output	ACTIVE = "011", ACT2INACT1 = "111",
Bit	5	Internal	cmfsm_always_on_core_l4_ao_l0.fsm_state	2	MSB		Output	INACTIVE = "000", INACT2ACT = "001",
Bit	7:6		Reserved					
Byte	0x92	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	cmfsm_cam_iss_l0.domain_is_on				Input	
Bit	1	Internal	cmfsm_cam_iss_l0.domain_wakeup				Input	
Bit	2	Internal	cmfsm_cam_iss_l0.domain_wkup_ack				Output	
Bit	3	Internal	cmfsm_cam_iss_l0.fsm_state	0	LSB		Output	ACT2INACT2 = "101"
Bit	4	Internal	cmfsm_cam_iss_l0.fsm_state	1			Output	ACTIVE = "011", ACT2INACT1 = "111",
Bit	5	Internal	cmfsm_cam_iss_l0.fsm_state	2	MSB		Output	INACTIVE = "000", INACT2ACT = "001",
Bit	7:6		Reserved					
Byte	0x93	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	ctsbuf_ff_cm2_per_cortex_m3_clk_l0.y			clock	Output	PER_cortex_m3_CLK (dpll_per_clkoutm6)
Bit	1	Internal	cmfsm_core_cortex_m3_l0.domain_is_on				Input	
Bit	2	Internal	cmfsm_core_cortex_m3_l0.domain_wakeup				Input	
Bit	3	Internal	cmfsm_core_cortex_m3_l0.domain_wkup_ack				Output	
Bit	4	Internal	cmfsm_core_cortex_m3_l0.fsm_state	0	LSB		Output	ACT2INACT2 = "101"
Bit	5	Internal	cmfsm_core_cortex_m3_l0.fsm_state	1			Output	ACTIVE = "011", ACT2INACT1 = "111",
Bit	6	Internal	cmfsm_core_cortex_m3_l0.fsm_state	2	MSB		Output	INACTIVE = "000", INACT2ACT = "001",
Bit	7		Reserved					
Byte	0x94	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	cmfsm_core_l3_1_l0.domain_is_on				Input	
Bit	1	Internal	cmfsm_core_l3_1_l0.domain_wakeup				Input	
Bit	2	Internal	cmfsm_core_l3_1_l0.domain_wkup_ack				Output	
Bit	3	Internal	cmfsm_core_l3_1_l0.fsm_state	0	LSB		Output	ACT2INACT2 = 101
Bit	4	Internal	cmfsm_core_l3_1_l0.fsm_state	1			Output	ACTIVE = 011, ACT2INACT1 = 111
Bit	5	Internal	cmfsm_core_l3_1_l0.fsm_state	2	MSB		Output	INACTIVE = 000, INACT2ACT = 001
Bit	7:6		Reserved					
Byte	0x95	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	cmfsm_core_l3_2_l0.domain_is_on				Input	
Bit	1	Internal	cmfsm_core_l3_2_l0.domain_wakeup				Input	
Bit	2	Internal	cmfsm_core_l3_2_l0.domain_wkup_ack				Output	

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Table 18-39. CM2 Observable Signals (continued)

Bit	3	Internal	cmfsm_core_l3_2_l0.fsm_state	0	LSB		Output	ACT2INACT2 = 101
Bit	4	Internal	cmfsm_core_l3_2_l0.fsm_state	1			Output	ACTIVE = 011, ACT2INACT1 = 111
Bit	5	Internal	cmfsm_core_l3_2_l0.fsm_state	2	MSB		Output	INACTIVE = 000, INACT2ACT = 001
Bit	7:6		Reserved					
Byte	0x96	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	cmfsm_core_l3_dma_l0.domain_is_on				Input	
Bit	1	Internal	cmfsm_core_l3_dma_l0.domain_wakeup				Input	
Bit	2	Internal	cmfsm_core_l3_dma_l0.domain_wkup_ack				Output	
Bit	3	Internal	cmfsm_core_l3_dma_l0.fsm_state	0	LSB		Output	ACT2INACT2 = 101
Bit	4	Internal	cmfsm_core_l3_dma_l0.fsm_state	1			Output	ACTIVE = 011, ACT2INACT1 = 111
Bit	5	Internal	cmfsm_core_l3_dma_l0.fsm_state	2	MSB		Output	INACTIVE = 000, INACT2ACT = 001
Bit	7:6		Reserved					
Byte	0x97	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	cmfsm_core_l3_emif_l0.domain_is_on				Input	
Bit	1	Internal	cmfsm_core_l3_emif_l0.domain_wakeup				Input	
Bit	2	Internal	cmfsm_core_l3_emif_l0.domain_wkup_ack				Output	
Bit	3	Internal	cmfsm_core_l3_emif_l0.fsm_state	0	LSB		Output	ACT2INACT2 = 101
Bit	4	Internal	cmfsm_core_l3_emif_l0.fsm_state	1			Output	ACTIVE = 011, ACT2INACT1 = 111
Bit	5	Internal	cmfsm_core_l3_emif_l0.fsm_state	2	MSB		Output	INACTIVE = 000, INACT2ACT = 001
Bit	7:6		Reserved					
Byte	0x98	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	ctsbuf_ff_cm2_per_abe_x1_gfclk_l0.y			clock	Output	PER_ABE_X1_GFCLK (dpll_abe_clkoutm2)
Bit	1	Internal	cmfsm_core_l3_instr_l0.domain_is_on				Input	
Bit	2	Internal	cmfsm_core_l3_instr_l0.domain_wakeup				Input	
Bit	3	Internal	cmfsm_core_l3_instr_l0.domain_wkup_ack				Output	
Bit	4	Internal	cmfsm_core_l3_instr_l0.fsm_state	0	LSB		Output	ACT2INACT2 = 101
Bit	5	Internal	cmfsm_core_l3_instr_l0.fsm_state	1			Output	ACTIVE = 011, ACT2INACT1 = 111
Bit	6	Internal	cmfsm_core_l3_instr_l0.fsm_state	2	MSB		Output	INACTIVE = 000, INACT2ACT = 001
Bit	7		Reserved					
Byte	0x99	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	cmfsm_core_l3x2_d2d_l0.domain_is_on				Input	
Bit	1	Internal	cmfsm_core_l3x2_d2d_l0.domain_wakeup				Input	
Bit	2	Internal	cmfsm_core_l3x2_d2d_l0.domain_wkup_ack				Output	
Bit	3	Internal	cmfsm_core_l3x2_d2d_l0.fsm_state	0	LSB		Output	ACT2INACT2 = 101
Bit	4	Internal	cmfsm_core_l3x2_d2d_l0.fsm_state	1			Output	ACTIVE = 011, ACT2INACT1 = 111
Bit	5	Internal	cmfsm_core_l3x2_d2d_l0.fsm_state	2	MSB		Output	INACTIVE = 000, INACT2ACT = 001
Bit	7:6		Reserved					
Byte	0x9a	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	ctsbuf_ff_cm2_func_192m_clk_l0.y			clock	Output	FUNC_192M (dpll_per_clkoutm2x2)

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Table 18-39. CM2 Observable Signals (continued)

Bit	1	Internal	cmfsm_core_l4_cfg_l0.domain_is_on				Input	
Bit	2	Internal	cmfsm_core_l4_cfg_l0.domain_wakeup				Input	
Bit	3	Internal	cmfsm_core_l4_cfg_l0.domain_wkup_ack				Output	
Bit	4	Internal	cmfsm_core_l4_cfg_l0.fsm_state	0	LSB		Output	ACT2INACT2 = 101
Bit	5	Internal	cmfsm_core_l4_cfg_l0.fsm_state	1			Output	ACTIVE = 011, ACT2INACT1 = 111
Bit	6	Internal	cmfsm_core_l4_cfg_l0.fsm_state	2	MSB		Output	INACTIVE = 000, INACT2ACT = 001
Bit	7		Reserved					
Byte	0x9b	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	7:0		Reserved					
Byte	0x9c	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	ctsbuf_ff_cm2_func_128m_clk_l0.y			clock	Output	FUNC_128M (dpll_per_clkoutm4)
Bit	1	Internal	cmfsm_dss_l3_dss_l0.domain_is_on				Input	
Bit	2	Internal	cmfsm_dss_l3_dss_l0.domain_wakeup				Input	
Bit	3	Internal	cmfsm_dss_l3_dss_l0.domain_wkup_ack				Output	
Bit	4	Internal	cmfsm_dss_l3_dss_l0.fsm_state	0	LSB		Output	ACT2INACT2 = 101
Bit	5	Internal	cmfsm_dss_l3_dss_l0.fsm_state	1			Output	ACTIVE = 011, ACT2INACT1 = 111
Bit	6	Internal	cmfsm_dss_l3_dss_l0.fsm_state	2	MSB		Output	INACTIVE = 000, INACT2ACT = 001
Bit	7		Reserved					
Byte	0x9d	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	ctsbuf_ff_cm2_core_sgx_gfclk_l0.y			clock	Output	CORE_SGX_GFCLK (dpll_core_clkoutm7)
Bit	1	Internal	cmfsm_gfx_l3_gfx_l0.domain_is_on				Input	
Bit	2	Internal	cmfsm_gfx_l3_gfx_l0.domain_wakeup				Input	
Bit	3	Internal	cmfsm_gfx_l3_gfx_l0.domain_wkup_ack				Output	
Bit	4	Internal	cmfsm_gfx_l3_gfx_l0.fsm_state	0	LSB		Output	ACT2INACT2 = 101
Bit	5	Internal	cmfsm_gfx_l3_gfx_l0.fsm_state	1			Output	ACTIVE = 011, ACT2INACT1 = 111
Bit	6	Internal	cmfsm_gfx_l3_gfx_l0.fsm_state	2	MSB		Output	INACTIVE = 000, INACT2ACT = 001
Bit	7		Reserved					
Byte	0x9e	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	cmfsm_ivahd_ivahd_root_l0.domain_is_on				Input	
Bit	1	Internal	cmfsm_ivahd_ivahd_root_l0.domain_wakeup				Input	
Bit	2	Internal	cmfsm_ivahd_ivahd_root_l0.domain_wkup_ack				Output	
Bit	3	Internal	cmfsm_ivahd_ivahd_root_l0.fsm_state	0	LSB		Output	ACT2INACT2 = 101
Bit	4	Internal	cmfsm_ivahd_ivahd_root_l0.fsm_state	1			Output	ACTIVE = 011, ACT2INACT1 = 111
Bit	5	Internal	cmfsm_ivahd_ivahd_root_l0.fsm_state	2	MSB		Output	INACTIVE = 000, INACT2ACT = 001
Bit	7:6		Reserved					
Byte	0x9f	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	cmfsm_l3_init_l3_init_l0.domain_is_on				Input	
Bit	1	Internal	cmfsm_l3_init_l3_init_l0.domain_wakeup				Input	
Bit	2	Internal	cmfsm_l3_init_l3_init_l0.domain_wkup_ack				Output	
Bit	3	Internal	cmfsm_l3_init_l3_init_l0.fsm_state	0	LSB		Output	ACT2INACT2 = 101

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Table 18-39. CM2 Observable Signals (continued)

Bit	4	Internal	cmfsm_l3_init_l3_init_I0.fsm_state	1			Output	ACTIVE = 011, ACT2INACT1 = 111
Bit	5	Internal	cmfsm_l3_init_l3_init_I0.fsm_state	2	MSB		Output	INACTIVE = 000, INACT2ACT = 001
Bit	7:6		Reserved					
Byte	0xa0	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	ctsbuf_ff_cm2_l4_iclk_p2p_i_i_I0.y			clock	Output	L4_ICLK
Bit	1	Internal	cmfsm_l4_per_l4_per_I0.domain_is_on				Input	
Bit	2	Internal	cmfsm_l4_per_l4_per_I0.domain_wakeup				Input	
Bit	3	Internal	cmfsm_l4_per_l4_per_I0.domain_wkup_ack				Output	
Bit	4	Internal	cmfsm_l4_per_l4_per_I0.fsm_state	0	LSB		Output	ACT2INACT2 = 101
Bit	5	Internal	cmfsm_l4_per_l4_per_I0.fsm_state	1			Output	ACTIVE = 011, ACT2INACT1 = 111
Bit	6	Internal	cmfsm_l4_per_l4_per_I0.fsm_state	2	MSB		Output	INACTIVE = 000, INACT2ACT = 001
Bit	7		Reserved					
Byte	0xa1	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	5:0		Reserved					
Bit	6	Internal	gcg_cam_phy_ctrl_gclk_I0.clk_is_gated				Output	
Bit	7	Internal	gcg_cam_phy_ctrl_gclk_I0.clk_is_running				Output	
Byte	0xa2	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	gcg_cm2_profiling_l4_giclk_I0.clk_is_gated				Output	
Bit	1	Internal	gcg_cm2_profiling_l4_giclk_I0.clk_is_running				Output	
Bit	2	Internal	gcg_core_alwon_32k_gfclk_I0.clk_is_gated				Output	
Bit	3	Internal	gcg_core_alwon_32k_gfclk_I0.clk_is_running				Output	
Bit	4	Internal	gcg_core_cortex_m3_clk_I0.clk_is_gated				Output	
Bit	5	Internal	gcg_core_cortex_m3_clk_I0.clk_is_running				Output	
Bit	7:6		Reserved					
Byte	0xa3	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	gcg_dss_fclk_I0.clk_is_gated				Output	
Bit	1	Internal	gcg_dss_fclk_I0.clk_is_running				Output	
Bit	2	Internal	gcg_cortex_m3_gclk_I0.clk_is_gated				Output	
Bit	3	Internal	gcg_cortex_m3_gclk_I0.clk_is_running				Output	
Bit	4	Internal	gcg_fdif_fclk_pwadded_I0.clk_is_gated				Output	
Bit	5	Internal	gcg_fdif_fclk_pwadded_I0.clk_is_running				Output	
Bit	6	Internal	gcg_fdif_gfclk_I0.clk_is_gated				Output	
Bit	7	Internal	gcg_fdif_gfclk_I0.clk_is_running				Output	
Byte	0xa4	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	gcg_func_128m_clk_I0.clk_is_gated				Output	
Bit	1	Internal	gcg_func_128m_clk_I0.clk_is_running				Output	
Bit	2	Internal	gcg_func_12m_fclk_pwadded_I0.clk_is_gated				Output	
Bit	3	Internal	gcg_func_12m_fclk_pwadded_I0.clk_is_running				Output	
Bit	4	Internal	gcg_func_192m_clk_I0.clk_is_gated				Output	
Bit	5	Internal	gcg_func_192m_clk_I0.clk_is_running				Output	
Bit	6	Internal	gcg_func_24mc_fclk_pwadded_I0.clk_is_gated				Output	
Bit	7	Internal	gcg_func_24mc_fclk_pwadded_I0.clk_is_running				Output	
Byte	0xa5	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	gcg_func_48m_fclk_pwadded_I0.clk_is_gated				Output	
Bit	1	Internal	gcg_func_48m_fclk_pwadded_I0.clk_is_running				Output	
Bit	2	Internal	gcg_func_48mc_fclk_pwadded_I0.clk_is_gated				Output	

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Table 18-39. CM2 Observable Signals (continued)

Bit	3	Internal	gcg_func_48mc_fclk_pwadded_I0.clk_is_running				Output	
Bit	4	Internal	gcg_func_64m_fclk_pwadded_I0.clk_is_gated				Output	
Bit	5	Internal	gcg_func_64m_fclk_pwadded_I0.clk_is_running				Output	
Bit	6	Internal	gcg_func_96m_alwon_clk_I0.clk_is_gated				Output	
Bit	7	Internal	gcg_func_96m_alwon_clk_I0.clk_is_running				Output	
Byte	0xa6	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	gcg_func_96m_fclk_pwadded_I0.clk_is_gated				Output	
Bit	1	Internal	gcg_func_96m_fclk_pwadded_I0.clk_is_running				Output	
Bit	3:2		Reserved					
Bit	4	Internal	gcg_hsi_fclk_pwadded_I0.clk_is_gated				Output	
Bit	5	Internal	gcg_hsi_fclk_pwadded_I0.clk_is_running				Output	
Bit	6	Internal	gcg_hsic_p1_480m_gfclk_I0.clk_is_gated				Output	
Bit	7	Internal	gcg_hsic_p1_480m_gfclk_I0.clk_is_running				Output	
Byte	0xa7	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	gcg_hsic_p1_gfclk_I0.clk_is_gated				Output	
Bit	1	Internal	gcg_hsic_p1_gfclk_I0.clk_is_running				Output	
Bit	2	Internal	gcg_hsic_p2_480m_gfclk_I0.clk_is_gated				Output	
Bit	3	Internal	gcg_hsic_p2_480m_gfclk_I0.clk_is_running				Output	
Bit	4	Internal	gcg_hsic_p2_gfclk_I0.clk_is_gated				Output	
Bit	5	Internal	gcg_hsic_p2_gfclk_I0.clk_is_running				Output	
Bit	6	Internal	gcg_init_480m_gfclk_I0.clk_is_gated				Output	
Bit	7	Internal	gcg_init_480m_gfclk_I0.clk_is_running				Output	
Byte	0xa8	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	gcg_init_48m_gfclk_I0.clk_is_gated				Output	
Bit	1	Internal	gcg_init_48m_gfclk_I0.clk_is_running				Output	
Bit	2	Internal	gcg_init_48mc_gfclk_I0.clk_is_gated				Output	
Bit	3	Internal	gcg_init_48mc_gfclk_I0.clk_is_running				Output	
Bit	4	Internal	gcg_init_60m_fclk_pwadded_I0.clk_is_gated				Output	
Bit	5	Internal	gcg_init_60m_fclk_pwadded_I0.clk_is_running				Output	
Bit	6	Internal	gcg_init_60m_p1_gfclk_I0.clk_is_gated				Output	
Bit	7	Internal	gcg_init_60m_p1_gfclk_I0.clk_is_running				Output	
Byte	0xa9	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	gcg_init_60m_p2_gfclk_I0.clk_is_gated				Output	
Bit	1	Internal	gcg_init_60m_p2_gfclk_I0.clk_is_running				Output	
Bit	2	Internal	gcg_init_960m_gfclk_I0.clk_is_gated				Output	
Bit	3	Internal	gcg_init_960m_gfclk_I0.clk_is_running				Output	
Bit	4	Internal	gcg_init_96m_gfclk_I0.clk_is_gated				Output	
Bit	5	Internal	gcg_init_96m_gfclk_I0.clk_is_running				Output	
Bit	6	Internal	gcg_init_hsi_gfclk_I0.clk_is_gated				Output	
Bit	7	Internal	gcg_init_hsi_gfclk_I0.clk_is_running				Output	
Byte	0xaa	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	gcg_iss_gclk_I0.clk_is_gated				Output	
Bit	1	Internal	gcg_iss_gclk_I0.clk_is_running				Output	
Bit	2	Internal	gcg_l3_gfx_giclk_I0.clk_is_gated				Output	
Bit	3	Internal	gcg_l3_gfx_giclk_I0.clk_is_running				Output	
Bit	4	Internal	gcg_l4_ao_iclk_I0.clk_is_gated				Output	
Bit	5	Internal	gcg_l4_ao_iclk_I0.clk_is_running				Output	
Bit	7:6		Reserved					

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Table 18-39. CM2 Observable Signals (continued)

Byte	0xab	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	gcg_l4_d2d_giclk_I0.clk_is_gated				Output	
Bit	1	Internal	gcg_l4_d2d_giclk_I0.clk_is_running				Output	
Bit	2	Internal	gcg_l4_d2d_giclk_I1.clk_is_gated				Output	
Bit	3	Internal	gcg_l4_d2d_giclk_I1.clk_is_running				Output	
Bit	4	Internal	gcg_l4_dss_giclk_I0.clk_is_gated				Output	
Bit	5	Internal	gcg_l4_dss_giclk_I0.clk_is_running				Output	
Bit	6	Internal	gcg_per_32k_gfclk_I0.clk_is_gated				Output	
Bit	7	Internal	gcg_per_32k_gfclk_I0.clk_is_running				Output	
Byte	0xac	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	gcg_per_48m_gfclk_I0.clk_is_gated				Output	
Bit	1	Internal	gcg_per_48m_gfclk_I0.clk_is_running				Output	
Bit	2	Internal	gcg_per_96m_gfclk_I0.clk_is_gated				Output	
Bit	3	Internal	gcg_per_96m_gfclk_I0.clk_is_running				Output	
Bit	4	Internal	gcg_per_abe_24m_fclk_pwadded_I0.clk_is_gated				Output	
Bit	5	Internal	gcg_per_abe_24m_fclk_pwadded_I0.clk_is_running				Output	
Bit	6	Internal	gcg_per_abe_nc_fclk_pwadded_I0.clk_is_gated				Output	
Bit	7	Internal	gcg_per_abe_nc_fclk_pwadded_I0.clk_is_running				Output	
Byte	0xad	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	gcg_per_dpll_alwon_clk_I0.clk_is_gated				Output	
Bit	1	Internal	gcg_per_dpll_alwon_clk_I0.clk_is_running				Output	
Bit	2	Internal	gcg_per_dpll_scrm_clk_I0.clk_is_gated				Output	
Bit	3	Internal	gcg_per_dpll_scrm_clk_I0.clk_is_running				Output	
Bit	4	Internal	gcg_per_cortex_m3_clk_I0.clk_is_gated				Output	
Bit	5	Internal	gcg_per_cortex_m3_clk_I0.clk_is_running				Output	
Bit	6	Internal	gcg_per_sgx_fclk_I0.clk_is_gated				Output	
Bit	7	Internal	gcg_per_sgx_fclk_I0.clk_is_running				Output	
Byte	0xae	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	gcg_per_sys_gfclk_I0.clk_is_gated				Output	
Bit	1	Internal	gcg_per_sys_gfclk_I0.clk_is_running				Output	
Bit	2	Internal	gcg_sr_core_sysclk_I0.clk_is_gated				Output	
Bit	3	Internal	gcg_sr_core_sysclk_I0.clk_is_running				Output	
Bit	4	Internal	gcg_sr_iva_sysclk_I0.clk_is_gated				Output	
Bit	5	Internal	gcg_sr_iva_sysclk_I0.clk_is_running				Output	
Bit	6	Internal	gcg_sr_mpu_sysclk_I0.clk_is_gated				Output	
Bit	7	Internal	gcg_sr_mpu_sysclk_I0.clk_is_running				Output	
Byte	0xaf	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	gcg_tll_ch0_gfclk_I0.clk_is_gated				Output	
Bit	1	Internal	gcg_tll_ch0_gfclk_I0.clk_is_running				Output	
Bit	2	Internal	gcg_tll_ch1_gfclk_I0.clk_is_gated				Output	
Bit	3	Internal	gcg_tll_ch1_gfclk_I0.clk_is_running				Output	
Bit	7:4		Reserved					
Byte	0xb0	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	1:0		Reserved					
Bit	2	Internal	gcg_usb_dpll_clk_I0.clk_is_gated				Output	
Bit	3	Internal	gcg_usb_dpll_clk_I0.clk_is_running				Output	
Bit	4	Internal	gcg_utmi_p3_gfclk_I0.clk_is_gated				Output	
Bit	5	Internal	gcg_utmi_p3_gfclk_I0.clk_is_running				Output	

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Table 18-39. CM2 Observable Signals (continued)

Bit	6	Internal	gcg_utmi_root_gfclk_I0.clk_is_gated				Output	
Bit	7	Internal	gcg_utmi_root_gfclk_I0.clk_is_running				Output	
Byte	0xb1	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	gat_cam_phy_ctrl_gclk_I0.clkCtrl				Input	
Bit	1	Internal	gat_cm2_profiling_l4_giclk_I0.clkCtrl				Input	
Bit	2	Internal	gat_cortex_m3_clk_mux_pwadded0_I0.clkCtrl				Input	
Bit	3	Internal	gat_cortex_m3_clk_mux_pwadded1_I0.clkCtrl				Input	
Bit	4	Internal	gat_fdif_fclk_pwadded_I0.clkCtrl				Input	
Bit	5	Internal	gat_fdif_gfclk_I0.clkCtrl				Input	
Bit	6	Internal	gat_func_12m_fclk_pwadded_I0.clkCtrl				Input	
Bit	7	Internal	gat_func_24mc_fclk_pwadded_I0.clkCtrl				Input	
Byte	0xb2	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	gat_func_48m_fclk_pwadded_I0.clkCtrl				Input	
Bit	1	Internal	gat_func_48mc_fclk_pwadded_I0.clkCtrl				Input	
Bit	2	Internal	gat_func_64m_fclk_pwadded_I0.clkCtrl				Input	
Bit	3	Internal	gat_func_96m_fclk_pwadded_I0.clkCtrl				Input	
Bit	4		Reserved					
Bit	5	Internal	gat_hsi_fclk_pwadded_I0.clkCtrl				Input	
Bit	6	Internal	gat_hsmmc1_fclk_pwadded0_I0.clkCtrl				Input	
Bit	7	Internal	gat_hsmmc1_fclk_pwadded1_I0.clkCtrl				Input	
Byte	0xb3	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	gat_hsmmc2_fclk_pwadded0_I0.clkCtrl				Input	
Bit	1	Internal	gat_hsmmc2_fclk_pwadded1_I0.clkCtrl				Input	
Bit	3:2		Reserved					
Bit	4	Internal	gat_init_48m_gfclk_I0.clkCtrl				Input	
Bit	5	Internal	gat_init_48mc_gfclk_I0.clkCtrl				Input	
Bit	6	Internal	gat_init_96m_gfclk_I0.clkCtrl				Input	
Bit	7	Internal	gat_init_hsi_gfclk_I0.clkCtrl				Input	
Byte	0xb4	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	gat_l3_1_giclk_I0.clkCtrl				Input	
Bit	1	Internal	gat_l3_2_giclk_I0.clkCtrl				Input	
Bit	2	Internal	gat_l3_d2d_giclk_I0.clkCtrl				Input	
Bit	3	Internal	gat_l3_dma_giclk_I0.clkCtrl				Input	
Bit	4	Internal	gat_l3_dss_giclk_I0.clkCtrl				Input	
Bit	5	Internal	gat_l3_emif_giclk_I0.clkCtrl				Input	
Bit	6	Internal	gat_l3_eintrconn_giclk_I0.clkCtrl				Input	
Bit	7	Internal	gat_l3_gfx_giclk_I0.clkCtrl				Input	
Byte	0xb5	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	gat_l3_init_giclk_I0.clkCtrl				Input	
Bit	1	Internal	gat_l3_instr_giclk_I0.clkCtrl				Input	
Bit	2		Reserved					
Bit	3	Internal	gat_l4_ao_iclk_I0.clkCtrl				Input	
Bit	4		Reserved					
Bit	5	Internal	gat_l4_cfg_giclk_I0.clkCtrl				Input	
Bit	6	Internal	gat_l4_d2d_giclk_I0.clkCtrl				Input	
Bit	7	Internal	gat_l4_init_giclk_I0.clkCtrl				Input	
Byte	0xb6	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	gat_l4_per_giclk_I0.clkCtrl				Input	

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Table 18-39. CM2 Observable Signals (continued)

Bit	5:1		Reserved					
Bit	6	Internal	gat_mcbsp4_sync_mux_pwadded0_I0.clkCtrl				Input	
Bit	7	Internal	gat_mcbsp4_sync_mux_pwadded1_I0.clkCtrl				Input	
Byte	0xb7	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	gat_per_48m_gfclk_I0.clkCtrl				Input	
Bit	1	Internal	gat_per_96m_gfclk_I0.clkCtrl				Input	
Bit	2	Internal	gat_per_abe_24m_fclk_pwadded_I0.clkCtrl				Input	
Bit	3	Internal	gat_per_abe_nc_fclk_pwadded_I0.clkCtrl				Input	
Bit	4	Internal	gat_sgx_clk_mux_pwadded0_I0.clkCtrl				Input	
Bit	5	Internal	gat_sgx_clk_mux_pwadded1_I0.clkCtrl				input	
Bit	7:6		reserved					
Byte	0xb8	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	External	dllready	0			input	
Bit	1	External	dllready	1			Input	
Bit	2	External	dllready	2			Input	
Bit	3	External	dllready	3			Input	
Bit	4	External	dllready	4			Input	
Bit	5	External	dllready	5			Input	
Bit	6	External	dllready	6			Input	
Bit	7	External	dllready	7			Input	
Byte	0xb9	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	emiffsm_I0.state	0	LSB		Output	
Bit	1	Internal	emiffsm_I0.state	1			Output	
Bit	2	Internal	emiffsm_I0.state	2	MSB		Output	
Bit	3	Internal	emiffsm_I0.clockStable				Output	
Bit	4	External	forceactive_cortex_m3_cpu1				Input	
Bit	5	External	forceactive_cortex_m3_cpu2				Input	
Bit	6	External	inhibitsleep_cortex_m3_cpu1				Input	
Bit	7	External	inhibitsleep_cortex_m3_cpu2				Input	
Byte	0xba	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	cortex_m3_emu_custom.emu_clkstate_cortex_m3				Output	
Bit	1	Internal	prcm_emu_ctrl_clk_cortex_m3_cpu1_st.ackfsm_state	0	LSB		Output	FORCEACKSTATE = 11, BOTHACK = 10
Bit	2	Internal	prcm_emu_ctrl_clk_cortex_m3_cpu1_st.ackfsm_state	1	MSB		Output	ACKOFF = 01, INHIBACK = 00
Bit	3	Internal	prcm_emu_ctrl_clk_cortex_m3_cpu1_st.fsm_state	0	LSB		Output	FORCEON = 010
Bit	4	Internal	prcm_emu_ctrl_clk_cortex_m3_cpu1_st.fsm_state	1			Output	SLEEPDESIREDSTATE = 111, SLEEP2NORMAL = 101

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Table 18-39. CM2 Observable Signals (continued)

Bit	5	Internal	prcm_emu_ctrl_clk_cortex_m3_cpu1_st.fsm_state	2	MSB		Output	NORMAL = 000, TOSLEEPD = 001
Bit	7:6		Reserved					
Byte	0xbb	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	prcm_emu_ctrl_clk_cortex_m3_cpu2_st.ackfsm_state	0	LSB		Output	FORCEACKSTATE = 11, BOTHACK = 10
Bit	1	Internal	prcm_emu_ctrl_clk_cortex_m3_cpu2_st.ackfsm_state	1	MSB		Output	ACKOFF = 01, INHIBACK = 00
Bit	2	Internal	prcm_emu_ctrl_clk_cortex_m3_cpu2_st.fsm_state	0	LSB		Output	FORCEON = 010
Bit	3	Internal	prcm_emu_ctrl_clk_cortex_m3_cpu2_st.fsm_state	1			Output	SLEEPDESIREDSTATE = 111,SLEEP2NORMAL = 101
Bit	4	Internal	prcm_emu_ctrl_clk_cortex_m3_cpu2_st.fsm_state	2	MSB		Output	NORMAL = 000, TOSLEEPD = 001
Bit	7:5		Reserved					
Byte	0xbc	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	prcm_emu_ctrl_cortex_m3_clk_I0.ackfsm_state	0	LSB		Output	FORCEACKSTATE = 11, BOTHACK = 10
Bit	1	Internal	prcm_emu_ctrl_cortex_m3_clk_I0.ackfsm_state	1	MSB		Output	ACKOFF = 01, INHIBACK = 00
Bit	2	Internal	prcm_emu_ctrl_cortex_m3_clk_I0.fsm_state	0	LSB		Output	FORCEON = 010
Bit	3	Internal	prcm_emu_ctrl_cortex_m3_clk_I0.fsm_state	1			Output	SLEEPDESIREDSTATE = 111,SLEEP2NORMAL = 101
Bit	4	Internal	prcm_emu_ctrl_cortex_m3_clk_I0.fsm_state	2	MSB		Output	NORMAL = 000, TOSLEEPD = 001
Bit	5	Internal	gat_l3_dss_giclk_I0.clkGated			clock	Output	L3_DSS_GICLK
Bit	6	Internal	gat_l3_init_giclk_I0.clkGated			clock	Output	L3_INIT_GICLK
Bit	7		Reserved					
Byte	0xbd	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	gat_l3_gfx_giclk_I0.clkGated			clock	Output	L3_GFX_GICLK
Bit	1	Internal	gat_l3_emif_giclk_I0.clkGated			clock	Output	L3_EMIF_GICLK
Bit	2	Internal	gat_l3_d2d_giclk_I0.clkGated			clock	Output	L3_D2D_GICLK
Bit	3	Internal	gat_l3_1_giclk_I0.clkGated			clock	Output	L3_1_GICLK
Bit	4	Internal	gat_l3_2_giclk_I0.clkGated			clock	Output	L3_2_GICLK
Bit	5	Internal	gat_l3_instr_giclk_I0.clkGated			clock	Output	L3_INSTR_GICLK
Bit	6	Internal	gat_l3_dma_giclk_I0.clkGated			clock	Output	L3_DMA_GICLK
Bit	7	Internal	gat_l4_init_giclk_I0.clkGated			clock	Output	L4_INIT_GICLK
Byte	0xbe	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	gat_l4_per_giclk_I0.clkGated			clock	Output	L4_PER_GICLK
Bit	1		Reserved					
Bit	2	Internal	gat_l4_ao_iclk_I0.clkGated			clock	Output	L4_AO_ICLK
Bit	3	Internal	gat_l4_d2d_giclk_I0.clkGated			clock	Output	L4_D2D_GICLK
Bit	4	Internal	gat_l4_cfg_giclk_I0.clkGated			clock	Output	L4_CFG_GICLK
Bit	5	Internal	gat_cm2_profiling_l4_giclk_I0.clkGated			clock	Output	CM2_PROFILING_L4_GICLK
Bit	6		Reserved					
Bit	7	Internal	gat_cam_phy_ctrl_gclk_I0.clkGated			clock	Output	CAM_PHY_CTRL_GCLK
Byte	0xbf	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments

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Table 18-39. CM2 Observable Signals (continued)

Bit	0	Internal	gat_init_96m_gfclk_I0.clkGated			clock	Output	INIT_96M_GFCLK
Bit	1	Internal	gat_per_96m_gfclk_I0.clkGated			clock	Output	PER_96M_GFCLK
Bit	2	Internal	gat_init_hsi_gfclk_I0.clkGated			clock	Output	INIT_HSI_GFCLK
Bit	3	Internal	gat_per_48m_gfclk_I0.clkGated			clock	Output	PER_48M_GFCLK
Bit	4	Internal	gat_init_48m_gfclk_I0.clkGated			clock	Output	INIT_48M_GFCLK
Bit	5	Internal	dg1_func_12m_fclk_I0.div_bus			clock	Output	FUNC_12M_GFCLK
Bit	6	Internal	dg1_func_24mc_fclk_I0.div_bus			clock	Output	PER_24MC_GFCLK
Bit	7		Reserved					
Byte	0xc0	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	gat_init_48mc_gfclk_I0.clkGated			clock	Output	INIT_48MC_GFCLK
Bit	1	Internal	gat_init_48mc_gfclk_I0.clkGated			clock	Output	HDMI_PHY_48MHZ_GFCLK
Bit	2	Internal	gat_fdif_gfclk_I0.clkGated			clock	Output	FDIF_GFCLK
Bit	3	Internal	mux_hsmmc2_fclk_I0.clk_out			clock	Output	INIT_HSMMC2_GFCLK
Bit	4	Internal	mux_hsmmc1_fclk_I0.clk_out			clock	Output	INIT_HSMMC1_GFCLK
Bit	5		Reserved					
Bit	6	Internal	mux_cortex_m3_clk_mux_I0.clk_out			clock	Output	cortex_m3_ISS_CLK
Bit	7	Internal	mux_sgx_clk_mux_I0.clk_out			clock	Output	SGX_GFCLK
Byte	0xc1	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	dg1_per_abe_24m_fclk_I0.div_bus			clock	Output	PER_ABE_24M_GFCLK
Bit	1	Internal	mux_per_mcbsp4_gfclk_I0.clk_out			clock	Output	PER_MCBSP4_GFCLK
Bit	2		Reserved					
Bit	3		Reserved					
Bit	4	External	pd_dss_l4_dss_giclk_ien			clock	Output	L4_DSS_GICLK_IEN
Bit	5		Reserved					
Bit	6	External	pd_core_l4_d2d_giclk_ien			clock	Output	L4_D2D_GICLK_IEN
Bit	7	External	pd_core_l4_1_giclk_ien			clock	Output	L4_1_GICLK_IEN
Byte	0xc2	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	External	pd_core_l4_2_giclk_ien			clock	Output	L4_2_GICLK_IEN
Bit	1	External	pd_core_l4_instr_giclk_ien			clock	Output	L4_INSTR_GICLK_IEN
Bit	2	External	pd_core_l4_dma_giclk_ien			clock	Output	L4_DMA_GICLK_IEN
Bit	3	External	pd_core_l4_emif_giclk_ien			clock	Output	L4_EMIF_GICLK_IEN
Bit	4	External	pd_l3_init_l4_init_giclk_ien			clock	Output	L4_INIT_GICLK_IEN
Bit	5	Internal	spare_cm2_I0.cm2_emac_50mh_clk_in			clock	Input	EMAC_50MHZ_CLK
Bit	6	Internal	freezegen_cam_iss_I0.freeze_Public				Output	
Bit	7	Internal	freezegen_core_cortex_m3_I0.freeze_Public				Output	
Byte	0xc3	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	freezegen_core_l3_dma_I0.freeze_Public				Output	
Bit	1	Internal	freezegen_core_l3x2_d2d_I0.freeze_Public				Output	
Bit	2	Internal	freezegen_dss_l3_dss_I0.freeze_Public				Output	

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Table 18-39. CM2 Observable Signals (continued)

Bit	3	Internal	freezegen_gfx_l3_gfx_l0.freeze_Public				Output	
Bit	4	Internal	freezegen_ivahd_ivahd_root_l0.freeze_Public				Output	
Bit	5	Internal	freezegen_l3_init_l3_init_l0.freeze_Public				Output	
Bit	6		Reserved					
Bit	7		Reserved					

18.4.11.5.8 CM1 Subsystem Observable Signals

The General Wakeup Control observability inputs hwobs_int_cm1(i) , (where i = 0…31) are mapped to the signals debugcm1(i), (where i = 0…31) coming out of the PRCM submodule clock manager 1 (CM1).

Local multiplexing controls at the CM1 level are in the CM1_DEBUG_CFG register. The CM1 observability output signals are driven on the debugcm1(0) through debugcm1(7) lines. A certain mux set is selected by programming the CM1_DEBUG_CFG[6:0] SEL0 bit field. The remaining debugcm1(8) through debugcm1(31) lines are reserved for future use. For more information about the CM1 observability source select field, see Section 3.11.22.1, *INTRCONN_SOCKET_CM1 Register Summary* in Chapter 3, *Power, Reset, and Clock Management*.

Table 18-40provides different details about the signals inside CM1 that can be monitored on device hw_dbg pins.

Table 18-40. CM1 Observable Signals

Byte	0x00	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	External	cortex_a9_cm1_profiling_event	0			Input	CPU0_MStandby
Bit	1	External	cortex_a9_cm1_profiling_event	2			Input	CPU0_MWait
Bit	2	External	cortex_a9_cm1_profiling_event	4			Input	CPU1_MStandby
Bit	3	External	cortex_a9_cm1_profiling_event	6			Input	CPU1_MWait
Bit	4	External	cortex_a9_cm1_profiling_event	1			Input	CPU0_MWakeup
Bit	5	External	cortex_a9_cm1_profiling_event	5			Input	CPU1_MWakeup
Bit	6	External	cortex_a9_cm1_profiling_event	3			Input	
Bit	7	External	cortex_a9_cm1_profiling_event	7			Input	
Byte	0x01	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	ckctrl_emif_l0.ckctrl_mpudpll				Input	
Bit	1	Internal	ckctrl_emif_l0.ckstat_mpudpll				output	
Bit	2	Internal	ckctrl_emif_l0.ckctrl_icg1				output	
Bit	3	Internal	ckctrl_emif_l0.ckstat_icg1				Input	
Bit	4	Internal	ckctrl_emif_l0.ckctrl_icg2				output	
Bit	5	Internal	ckctrl_emif_l0.ckstat_icg2				Input	
Bit	6	Internal	ckctrl_emif_l0.emif_clk_sel				output	
Bit	7		Reserved					
Byte	0x02	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments

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Table 18-40. CM1 Observable Signals (continued)

Byte	0x00	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	ckctrl_emif_I0.ckctrl_l3emif				Input	
Bit	1	Internal	ckctrl_emif_I0.ckstat_l3emif				output	
Bit	2	Internal	ckctrl_emif_I0.ckctrl_icg3				output	
Bit	3	Internal	ckctrl_emif_I0.ckstat_icg3				Input	
Bit	4	Internal	ckctrl_emif_I0.ckctrl_icg4				output	
Bit	5	Internal	ckctrl_emif_I0.ckstat_icg4				Input	
Bit	6	Internal	ckctrl_emif_I0.emif_clk_sel				output	
Bit	7		Reserved					
Byte	0x03	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	mpu_dcc_fsm_I0.dbgstate	0			output	
Bit	1	Internal	mpu_dcc_fsm_I0.dbgstate	1			output	
Bit	2	Internal	mpu_dcc_fsm_I0.dbgstate	2			output	
Bit	3	Internal	mpu_dcc_fsm_I0.dbgstate	3			output	
Bit	4	Internal	ckctrl_emif_I0.ckctrl_icg1				output	
Bit	5	Internal	mpu_dcc_fsm_I0.mpu_clkoutenack				Input	
Bit	6	Internal	mpu_dcc_fsm_I0.mpu_clkouthifenack				Input	
Bit	7	Internal	mpu_dcc_fsm_I0.mpu_dcc_ckstat				Input	
Byte	0x04	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	7:0		Reserved					SPARE
Byte	0x5	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	7:0		Reserved					SPARE
Byte	0x6	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	7:0		Reserved					SPARE
Byte	0x7	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	7:0		Reserved					SPARE
Byte	0x8	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	7:0		Reserved					SPARE
Byte	0x9	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	7:0		Reserved					SPARE
Byte	0xa	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	7:0		Reserved					SPARE
Byte	0xb	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	7:0		Reserved					SPARE
Byte	0xc	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	7:0		Reserved					SPARE
Byte	0xd	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	7:0		Reserved					SPARE

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Table 18-40. CM1 Observable Signals (continued)

Byte	0x00	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Byte	0xe	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	7:0		Reserved					SPARE
Byte	0xf	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	7:0		Reserved					SPARE
Byte	0x10	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	ifsm_aess_standby_prot_I0.MStandby				Input	
Bit	1	Internal	ifsm_aess_standby_prot_I0.init_Wait				output	
Bit	2	Internal	ifsm_aess_standby_prot_I0.module_mwakeup	0			Input	
Bit	7:3		Reserved					
Byte	0x11	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	ifsm_dspss_stdby_prot_I0.MStandby				Input	
Bit	1	Internal	ifsm_dspss_stdby_prot_I0.init_Wait				output	
Bit	2	Internal	ifsm_dspss_stdby_prot_I0.module_mwakeup	0			Input	
Bit	3	Internal	tfsm_aess_idle_prot_I0.idleReq				output	
Bit	4	Internal	tfsm_aess_idle_prot_I0.SidleAck	1			Input	
Bit	5	Internal	tfsm_aess_idle_prot_I0.module_swakeup	0			Input	
Bit	6	Internal	tfsm_aess_idle_prot_I0.fclken_IP				output	
Bit	7		Reserved					
Byte	0x12	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	tfsm_cm1_profiling_I0.idleReq				output	
Bit	1	Internal	tfsm_cm1_profiling_I0.SidleAck	1			Input	
Bit	2	Internal	tfsm_cm1_profiling_I0.module_swakeup	0			Input	
Bit	3	Internal	tfsm_cm1_profiling_I0.fclken_IP				output	
Bit	7:4		Reserved					
Byte	0x13	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	tfsm_dmic_idle_prot_I0.idleReq				output	
Bit	1	Internal	tfsm_dmic_idle_prot_I0.SidleAck	1			Input	
Bit	2	Internal	tfsm_dmic_idle_prot_I0.module_swakeup	0			Input	
Bit	3	Internal	tfsm_dmic_idle_prot_I0.module_swakeup	1			Input	
Bit	4	Internal	tfsm_dmic_idle_prot_I0.fclken_IP				output	
Bit	7:5		Reserved					
Byte	0x14	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	tfsm_l4_audio_interconnect_idle_prot_I0.idleReq				output	

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Table 18-40. CM1 Observable Signals (continued)

Byte	0x00	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	1	Internal	tfsm_l4_audio_interconnect_idle_prot_I0.SidleAck	1			Input	
Bit	2	Internal	tfsm_l4_audio_interconnect_idle_prot_I0.module_swakeup	0			Input	
Bit	3	Internal	tfsm_l4_audio_interconnect_idle_prot_I0.fclken_IP				output	
Bit	7:4		Reserved					
Byte	0x15	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	tfsm_mcasp_cfgidle_p_cfg_I0.idleReq				output	
Bit	1	Internal	tfsm_mcasp_cfgidle_p_cfg_I0.SidleAck	1			Input	
Bit	2	Internal	tfsm_mcasp_cfgidle_p_cfg_I0.module_swakeup	0			Input	
Bit	3	Internal	tfsm_mcasp_cfgidle_p_cfg_I0.module_swakeup	1			Input	
Bit	4	Internal	tfsm_mcasp_cfgidle_p_cfg_I0.fclken_IP				output	
Bit	7:5		Reserved					
Byte	0x16	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	tfsm_mcbsp1_mcbsplp_power_I0.idleReq				output	
Bit	1	Internal	tfsm_mcbsp1_mcbsplp_power_I0.SidleAck	1			Input	
Bit	2	Internal	tfsm_mcbsp1_mcbsplp_power_I0.module_swakeup	0			Input	
Bit	3	Internal	tfsm_mcbsp1_mcbsplp_power_I0.fclken_IP				output	
Bit	4	Internal	tfsm_mcbsp2_mcbsplp_power_I0.idleReq				output	
Bit	5	Internal	tfsm_mcbsp2_mcbsplp_power_I0.SidleAck	1			Input	
Bit	6	Internal	tfsm_mcbsp2_mcbsplp_power_I0.module_swakeup	0			Input	
Bit	7	Internal	tfsm_mcbsp2_mcbsplp_power_I0.fclken_IP				output	
Byte	0x17	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	tfsm_mcbsp3_mcbsplp_power_I0.idleReq				output	
Bit	1	Internal	tfsm_mcbsp3_mcbsplp_power_I0.SidleAck	1			Input	
Bit	2	Internal	tfsm_mcbsp3_mcbsplp_power_I0.module_swakeup	0			Input	
Bit	3	Internal	tfsm_mcbsp3_mcbsplp_power_I0.fclken_IP				output	
Bit	7:4		Reserved					
Byte	0x18	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	tfsm_pdm_idle_prot_I0.idleReq				output	
Bit	1	Internal	tfsm_pdm_idle_prot_I0.SidleAck	1			Input	
Bit	2	Internal	tfsm_pdm_idle_prot_I0.module_swakeup	0			Input	
Bit	3	Internal	tfsm_pdm_idle_prot_I0.module_swakeup	1			Input	

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Table 18-40. CM1 Observable Signals (continued)

Byte	0x00	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	4	Internal	tfsm_pdm_idle_prot_I0.fclken_IP				output	
Bit	7:5		Reserved					
Byte	0x19	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	tfsm_slimbus_slimbus_power_I0.idleReq				output	
Bit	1	Internal	tfsm_slimbus_slimbus_power_I0.SidleAck	1			Input	
Bit	2	Internal	tfsm_slimbus_slimbus_power_I0.module_swakeup	0			Input	
Bit	3	Internal	tfsm_slimbus_slimbus_power_I0.module_swakeup	1			Input	
Bit	4	Internal	tfsm_slimbus_slimbus_power_I0.fclken_IP				output	
Bit	7:5		Reserved					
Byte	0x1a	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	tfsm_dspss_idle_prot_I0.idleReq				output	
Bit	1	Internal	tfsm_dspss_idle_prot_I0.SidleAck	1			Input	
Bit	2	Internal	tfsm_dspss_idle_prot_I0.module_swakeup	0			Input	
Bit	3	Internal	tfsm_dspss_idle_prot_I0.fclken_IP				output	
Bit	4	Internal	tfsm_timer5_dmtimer_dmc_power_I0.idleReq				output	
Bit	5	Internal	tfsm_timer5_dmtimer_dmc_power_I0.SidleAck	1			Input	
Bit	6	Internal	tfsm_timer5_dmtimer_dmc_power_I0.module_swakeup	0			Input	
Bit	7	Internal	tfsm_timer5_dmtimer_dmc_power_I0.fclken_IP				output	
Byte	0x1b	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	tfsm_timer6_dmtimer_dmc_power_I0.idleReq				output	
Bit	1	Internal	tfsm_timer6_dmtimer_dmc_power_I0.SidleAck	1			Input	
Bit	2	Internal	tfsm_timer6_dmtimer_dmc_power_I0.module_swakeup	0			Input	
Bit	3	Internal	tfsm_timer6_dmtimer_dmc_power_I0.fclken_IP				output	
Bit	4	Internal	tfsm_timer7_dmtimer_dmc_power_I0.idleReq				output	
Bit	5	Internal	tfsm_timer7_dmtimer_dmc_power_I0.SidleAck	1			Input	
Bit	6	Internal	tfsm_timer7_dmtimer_dmc_power_I0.module_swakeup	0			Input	
Bit	7	Internal	tfsm_timer7_dmtimer_dmc_power_I0.fclken_IP				output	
Byte	0x1c	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	tfsm_timer8_dmtimer_dmc_power_I0.idleReq				output	
Bit	1	Internal	tfsm_timer8_dmtimer_dmc_power_I0.SidleAck	1			Input	

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Table 18-40. CM1 Observable Signals (continued)

Byte	0x00	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	2	Internal	tfsm_timer8_dmtimer_dmc_power_I0.module_swakeup	0			Input	
Bit	3	Internal	tfsm_timer8_dmtimer_dmc_power_I0.fclken_IP				output	
Bit	4	Internal	tfsm_wdt3_watchdog_power_I0.idleReq				output	
Bit	5	Internal	tfsm_wdt3_watchdog_power_I0.SidleAck	1			Input	
Bit	6	Internal	tfsm_wdt3_watchdog_power_I0.module_swakeup	0			Input	
Bit	7	Internal	tfsm_wdt3_watchdog_power_I0.fclken_IP				output	
Byte	0x1d	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	dpllsctrl_dpll_abe_I0.DPLLCtrlState	0	LSB		output	
Bit	1	Internal	dpllsctrl_dpll_abe_I0.DPLLCtrlState	1			output	
Bit	2	Internal	dpllsctrl_dpll_abe_I0.DPLLCtrlState	2			output	
Bit	3	Internal	dpllsctrl_dpll_abe_I0.DPLLCtrlState	3			output	
Bit	4	Internal	dpllsctrl_dpll_abe_I0.DPLLCtrlState	4			output	
Bit	5	Internal	dpllsctrl_dpll_abe_I0.DPLLCtrlState	5			output	
Bit	6	Internal	dpllsctrl_dpll_abe_I0.DPLLCtrlState	6			output	
Bit	7	Internal	dpllsctrl_dpll_abe_I0.DPLLCtrlState	7	MSB		output	
Byte	0x1e	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	dpllsctrl_dpll_abe_I0.freqChgReqAck				Input	
Bit	1	Internal	dpllsctrl_dpll_abe_I0.freqChgReq				output	
Bit	2	Internal	dpllsctrl_dpll_abe_I0.freqChgReqAck2				output	
Bit	3	Internal	dpllsctrl_dpll_abe_I0.freqChgReq2				Input	
Bit	4	Internal	dpllsctrl_dpll_abe_I0.bypass				Input	
Bit	5	Internal	dpllsctrl_dpll_abe_I0.freqlock				Input	
Bit	6	Internal	dpllsctrl_dpll_abe_I0.lossref				Input	
Bit	7	Internal	dpllsctrl_dpll_abe_I0.tinitz				output	
Byte	0x1f	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	dpllsctrl_dpll_abe_I0.tenable				output	
Bit	1	Internal	dpllsctrl_dpll_abe_I0.tenablediv				output	
Bit	2	Internal	dpllsctrl_dpll_abe_I0.idle				output	
Bit	3	Internal	dpllsctrl_dpll_abe_I0.lowcurrstdby				output	

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Table 18-40. CM1 Observable Signals (continued)

Byte	0x00	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	4	Internal	dpllsctrl_dpll_abe_I0.dpll_ticopwdn				Input	
Bit	5	Internal	dpllsctrl_dpll_abe_I0.dpll_ldopwdn				Input	
Bit	6	Internal	dpllsctrl_dpll_abe_I0.clkinpIsRunning				Input	
Bit	7	Internal	dpllsctrl_dpll_abe_I0.clkinpToBeGated				output	
Byte	0x20	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	dpllsctrl_dpll_abe_I0.clkinplowIsRunning				Input	
Bit	1	Internal	dpllsctrl_dpll_abe_I0.clkinplowToBeGated				output	
Bit	7:2		Reserved					
Byte	0x21	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	dpllsctrl_dpll_core_I0.DPLLCtrlState	0	LSB		output	
Bit	1	Internal	dpllsctrl_dpll_core_I0.DPLLCtrlState	1			output	
Bit	2	Internal	dpllsctrl_dpll_core_I0.DPLLCtrlState	2			output	
Bit	3	Internal	dpllsctrl_dpll_core_I0.DPLLCtrlState	3			output	
Bit	4	Internal	dpllsctrl_dpll_core_I0.DPLLCtrlState	4			output	
Bit	5	Internal	dpllsctrl_dpll_core_I0.DPLLCtrlState	5			output	
Bit	6	Internal	dpllsctrl_dpll_core_I0.DPLLCtrlState	6			output	
Bit	7	Internal	dpllsctrl_dpll_core_I0.DPLLCtrlState	7	MSB		output	
Byte	0x22	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	dpllsctrl_dpll_core_I0.stopCondBus	0			Input	
Bit	1	Internal	dpllsctrl_dpll_core_I0.stopCondBus	1			Input	
Bit	2	Internal	dpllsctrl_dpll_core_I0.stopCondBus	2			Input	
Bit	3	Internal	dpllsctrl_dpll_core_I0.stopCondBus	3			Input	
Bit	4	Internal	dpllsctrl_dpll_core_I0.stopCondBus	4			Input	
Bit	5	Internal	dpllsctrl_dpll_core_I0.stopCondBus	5			Input	
Bit	6	Internal	dpllsctrl_dpll_core_I0.stopCondBus	6			Input	
Bit	7	Internal	dpllsctrl_dpll_core_I0.stopCondBus	7			Input	
Byte	0x23	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	dpllsctrl_dpll_core_I0.bypassCondBus	0			Input	
Bit	1	Internal	dpllsctrl_dpll_core_I0.bypassCondBus	1			Input	
Bit	2	Internal	dpllsctrl_dpll_core_I0.bypassCondBus	2			Input	

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Table 18-40. CM1 Observable Signals (continued)

Byte	0x00	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	3	Internal	dpllsctrl_dpll_core_I0.bypassCondBus	3			Input	
Bit	4	Internal	dpllsctrl_dpll_core_I0.bypassCondBus	4			Input	
Bit	5	Internal	dpllsctrl_dpll_core_I0.bypassCondBus	5			Input	
Bit	6	Internal	dpllsctrl_dpll_core_I0.bypassCondBus	6			Input	
Bit	7	Internal	dpllsctrl_dpll_core_I0.bypassCondBus	7			Input	
Byte	0x24	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	dpllsctrl_dpll_core_I0.freqChgReqAck				Input	
Bit	1	Internal	dpllsctrl_dpll_core_I0.freqChgReq				output	
Bit	2	Internal	dpllsctrl_dpll_core_I0.freqChgReqAck2				output	
Bit	3	Internal	dpllsctrl_dpll_core_I0.freqChgReq2				Input	
Bit	4	Internal	dpllsctrl_dpll_core_I0.bypass				Input	
Bit	5	Internal	dpllsctrl_dpll_core_I0.freqlock				Input	
Bit	6	Internal	dpllsctrl_dpll_core_I0.lossref				Input	
Bit	7	Internal	dpllsctrl_dpll_core_I0.tinitz				output	
Byte	0x25	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	dpllsctrl_dpll_core_I0.tenable				output	
Bit	1	Internal	dpllsctrl_dpll_core_I0.tenablediv				output	
Bit	2	Internal	dpllsctrl_dpll_core_I0.idle				output	
Bit	3	Internal	dpllsctrl_dpll_core_I0.lowcurrstdby				output	
Bit	4	Internal	dpllsctrl_dpll_core_I0.dpll_ticopwdn				Input	
Bit	5	Internal	dpllsctrl_dpll_core_I0.dpll_ldopwdn				Input	
Bit	6	Internal	dpllsctrl_dpll_core_I0.ulowclken	0			output	
Bit	7	Internal	dpllsctrl_dpll_core_I0.dpll_clkbypselacksel	0			Input	
Byte	0x26	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	dpllsctrl_dpll_core_I0.clkinpIsRunning				Input	
Bit	1	Internal	dpllsctrl_dpll_core_I0.clkinpToBeGated				output	
Bit	2	Internal	dpllsctrl_dpll_core_I0.clkinplowIsRunning				Input	
Bit	3	Internal	dpllsctrl_dpll_core_I0.clkinplowToBeGated				output	
Bit	7:4		Reserved					
Byte	0x27	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments

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Table 18-40. CM1 Observable Signals (continued)

Byte	0x00	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	dpllsctrl_dpll_iva_I0.DPLLCtrlState	0	LSB		output	
Bit	1	Internal	dpllsctrl_dpll_iva_I0.DPLLCtrlState	1			output	
Bit	2	Internal	dpllsctrl_dpll_iva_I0.DPLLCtrlState	2			output	
Bit	3	Internal	dpllsctrl_dpll_iva_I0.DPLLCtrlState	3			output	
Bit	4	Internal	dpllsctrl_dpll_iva_I0.DPLLCtrlState	4			output	
Bit	5	Internal	dpllsctrl_dpll_iva_I0.DPLLCtrlState	5			output	
Bit	6	Internal	dpllsctrl_dpll_iva_I0.DPLLCtrlState	6			output	
Bit	7	Internal	dpllsctrl_dpll_iva_I0.DPLLCtrlState	7	MSB		output	
Byte	0x28	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	dpllsctrl_dpll_iva_I0.freqChgReqAck				Input	
Bit	1	Internal	dpllsctrl_dpll_iva_I0.freqChgReq				output	
Bit	2	Internal	dpllsctrl_dpll_iva_I0.freqChgReqAck2				output	
Bit	3	Internal	dpllsctrl_dpll_iva_I0.freqChgReq2				Input	
Bit	4	Internal	dpllsctrl_dpll_iva_I0.bypass				Input	
Bit	5	Internal	dpllsctrl_dpll_iva_I0.freqlock				Input	
Bit	6	Internal	dpllsctrl_dpll_iva_I0.lossref				Input	
Bit	7	Internal	dpllsctrl_dpll_iva_I0.tinitz				output	
Byte	0x29	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	dpllsctrl_dpll_iva_I0.tenable				output	
Bit	1	Internal	dpllsctrl_dpll_iva_I0.tenablediv				output	
Bit	2	Internal	dpllsctrl_dpll_iva_I0.idle				output	
Bit	3	Internal	dpllsctrl_dpll_iva_I0.lowcurrstdby				output	
Bit	4	Internal	dpllsctrl_dpll_iva_I0.dpll_ticopwdn				Input	
Bit	5	Internal	dpllsctrl_dpll_iva_I0.dpll_ldopwdn				Input	
Bit	6	Internal	dpllsctrl_dpll_iva_I0.clkinpIsRunning				Input	
Bit	7	Internal	dpllsctrl_dpll_iva_I0.clkinpToBeGated				output	
Byte	0x2a	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	dpllsctrl_dpll_iva_I0.clkinplowIsRunning				Input	
Bit	1	Internal	dpllsctrl_dpll_iva_I0.clkinplowToBeGated				output	
Bit	7:2		Reserved					

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Table 18-40. CM1 Observable Signals (continued)

Byte	0x00	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Byte	0x2b	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	dpllsctrl_dpll_mpu_I0.DPLLCtrlState	0	LSB		output	
Bit	1	Internal	dpllsctrl_dpll_mpu_I0.DPLLCtrlState	1			output	
Bit	2	Internal	dpllsctrl_dpll_mpu_I0.DPLLCtrlState	2			output	
Bit	3	Internal	dpllsctrl_dpll_mpu_I0.DPLLCtrlState	3			output	
Bit	4	Internal	dpllsctrl_dpll_mpu_I0.DPLLCtrlState	4			output	
Bit	5	Internal	dpllsctrl_dpll_mpu_I0.DPLLCtrlState	5			output	
Bit	6	Internal	dpllsctrl_dpll_mpu_I0.DPLLCtrlState	6			output	
Bit	7	Internal	dpllsctrl_dpll_mpu_I0.DPLLCtrlState	7	MSB		output	
Byte	0x2c	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	dpllsctrl_dpll_mpu_I0.freqChgReqAck				Input	
Bit	1	Internal	dpllsctrl_dpll_mpu_I0.freqChgReq				output	
Bit	2	Internal	dpllsctrl_dpll_mpu_I0.freqChgReqAck2				output	
Bit	3	Internal	dpllsctrl_dpll_mpu_I0.freqChgReq2				Input	
Bit	4	Internal	dpllsctrl_dpll_mpu_I0.bypass				Input	
Bit	5	Internal	dpllsctrl_dpll_mpu_I0.freqlock				Input	
Bit	6	Internal	dpllsctrl_dpll_mpu_I0.lossref				Input	
Bit	7	Internal	dpllsctrl_dpll_mpu_I0.tinitz				output	
Byte	0x2d	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	dpllsctrl_dpll_mpu_I0.tenable				output	
Bit	1	Internal	dpllsctrl_dpll_mpu_I0.tenablediv				output	
Bit	2	Internal	dpllsctrl_dpll_mpu_I0.idle				output	
Bit	3	Internal	dpllsctrl_dpll_mpu_I0.lowcurrstdby				output	
Bit	4	Internal	dpllsctrl_dpll_mpu_I0.dpll_ticopwdn				Input	
Bit	5	Internal	dpllsctrl_dpll_mpu_I0.dpll_ldopwdn				Input	
Bit	6	Internal	dpllsctrl_dpll_mpu_I0.clkinpIsRunning				Input	
Bit	7	Internal	dpllsctrl_dpll_mpu_I0.clkinpToBeGated				output	
Byte	0x2e	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	dpllsctrl_dpll_mpu_I0.clkinplowIsRunning				Input	
Bit	1	Internal	dpllsctrl_dpll_mpu_I0.clkinplowToBeGated				output	

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Table 18-40. CM1 Observable Signals (continued)

Byte	0x00	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	7:2		Reserved					
Byte	0x2f	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	7:0		Reserved					
Byte	0x30	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	ctsbuf_ff_cm1_func_96m_alwon_clk_I0.y			clock	output	FUNC_96M_ALWON_CLK (dpll_per_clkoutm2)
Bit	1	Internal	mutegen_dspss_to_ivahd_I0.dyn_domain_mute				output	
Bit	2	Internal	mutegen_dspss_to_ivahd_I0.static_domain_mute				output	
Bit	3	Internal	mutegen_dspss_to_ivahd_I0.public_active	0			Input	
Bit	4	Internal	mutegen_dspss_to_l3_interconnect_1_I0.dyn_domain_mute				output	
Bit	5	Internal	mutegen_dspss_to_l3_interconnect_1_I0.static_domain_mute				output	
Bit	6	Internal	mutegen_dspss_to_l3_interconnect_1_I0.public_active	0			Input	
Bit	7		Reserved					
Byte	0x31	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	mutegen_dspss_to_l4_audio_interconnect_I0.dyn_domain_mute				output	
Bit	1	Internal	mutegen_dspss_to_l4_audio_interconnect_I0.static_domain_mute				output	
Bit	2	Internal	mutegen_dspss_to_l4_audio_interconnect_I0.public_active	0			Input	
Bit	3	Internal	mutegen_dspss_to_sl2_I0.dyn_domain_mute				output	
Bit	4	Internal	mutegen_dspss_to_sl2_I0.static_domain_mute				output	
Bit	5	Internal	mutegen_dspss_to_sl2_I0.public_active	0			Input	
Bit	7:6		Reserved					
Byte	0x32	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	gat_l3_iclk_I0.clkGated			clock	output	L3_ICLK
Bit	1	Internal	cmfsm_audio_interconn_abe_I0.domain_is_on				Input	
Bit	2	Internal	cmfsm_audio_interconn_abe_I0.domain_wakeup				Input	
Bit	3	Internal	cmfsm_audio_interconn_abe_I0.domain_wkup_ack				output	
Bit	4	Internal	cmfsm_audio_interconn_abe_I0.fsm_state	0	LSB		output	ACT2INACT2 = "101"
Bit	5	Internal	cmfsm_audio_interconn_abe_I0.fsm_state	1			output	ACTIVE = "011", ACT2INACT1 = "111",
Bit	6	Internal	cmfsm_audio_interconn_abe_I0.fsm_state	2	MSB		output	INACTIVE = "000", INACT2ACT = "001",
Bit	7		Reserved					
Byte	0x33	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	ctsbuf_ff_cm1_core_dpll_hs_clk_I0.y			clock	output	CORE_DPLL_HS_CLK (dpll_abe_clkoutm3)
Bit	1	Internal	cmfsm_core_cm1_I0.domain_is_on				Input	

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Table 18-40. CM1 Observable Signals (continued)

Byte	0x00	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	2	Internal	cmfsm_core_cm1_I0.domain_wakeup				Input	
Bit	3	Internal	cmfsm_core_cm1_I0.domain_wkup_ack				output	
Bit	4	Internal	cmfsm_core_cm1_I0.fsm_state	0	LSB		output	ACT2INACT2 = "101"
Bit	5	Internal	cmfsm_core_cm1_I0.fsm_state	1			output	ACTIVE = "011", ACT2INACT1 = "111",
Bit	6	Internal	cmfsm_core_cm1_I0.fsm_state	2	MSB		output	INACTIVE = "000", INACT2ACT = "001",
Bit	7		Reserved					
Byte	0x34	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	gat_l4_root_clk_I0.clkGated			clock	output	L4_ROOT_CLK
Bit	1	Internal	cmfsm_mpu_mpu_dpll_I0.domain_is_on				Input	
Bit	2	Internal	cmfsm_mpu_mpu_dpll_I0.domain_wakeup				Input	
Bit	3	Internal	cmfsm_mpu_mpu_dpll_I0.domain_wkup_ack				output	
Bit	4	Internal	cmfsm_mpu_mpu_dpll_I0.fsm_state	0	LSB		output	ACT2INACT2 = "101"
Bit	5	Internal	cmfsm_mpu_mpu_dpll_I0.fsm_state	1			output	ACTIVE = "011", ACT2INACT1 = "111",
Bit	6	Internal	cmfsm_mpu_mpu_dpll_I0.fsm_state	2	MSB		output	INACTIVE = "000", INACT2ACT = "001",
Bit	7		Reserved					
Byte	0x35	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	cmfsm_dspss_dspss_root_I0.domain_is_on				Input	
Bit	1	Internal	cmfsm_dspss_dspss_root_I0.domain_wakeup				Input	
Bit	2	Internal	cmfsm_dspss_dspss_root_I0.domain_wkup_ack				output	
Bit	3	Internal	cmfsm_dspss_dspss_root_I0.fsm_state	0	LSB		output	ACT2INACT2 = "101"
Bit	4	Internal	cmfsm_dspss_dspss_root_I0.fsm_state	1			output	ACTIVE = "011", ACT2INACT1 = "111",
Bit	5	Internal	cmfsm_dspss_dspss_root_I0.fsm_state	2	MSB		output	INACTIVE = "000", INACT2ACT = "001",
Bit	6	Internal	gcg_abe_24m_fclk_pwadded_I0.clk_is_gated				output	
Bit	7	Internal	gcg_abe_24m_fclk_pwadded_I0.clk_is_running				output	
Byte	0x36	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	gcg_abe_alwon_32k_clk_I0.clk_is_gated				output	
Bit	1	Internal	gcg_abe_alwon_32k_clk_I0.clk_is_running				output	
Bit	2	Internal	gcg_abe_clk_pwadded_I0.clk_is_gated				output	
Bit	3	Internal	gcg_abe_clk_pwadded_I0.clk_is_running				output	
Bit	4	Internal	gcg_abe_sysclk_I0.clk_is_gated				output	

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Table 18-40. CM1 Observable Signals (continued)

Byte	0x00	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	5	Internal	gcg_abe_sysclk_I0.clk_is_running				output	
Bit	6	Internal	gcg_adll_clk_div_pwadded_I0.clk_is_gated				output	
Bit	7	Internal	gcg_adll_clk_div_pwadded_I0.clk_is_running				output	
Byte	0x37	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	gcg_aess_fclk_pwadded_I0.clk_is_gated				output	
Bit	1	Internal	gcg_aess_fclk_pwadded_I0.clk_is_running				output	
Bit	2	Internal	gcg_async_dll_x2_clk_I0.clk_is_gated				output	
Bit	3	Internal	gcg_async_dll_x2_clk_I0.clk_is_running				output	
Bit	4	Internal	gcg_async_phy1_clk_I0.clk_is_gated				output	
Bit	5	Internal	gcg_async_phy1_clk_I0.clk_is_running				output	
Bit	6	Internal	gcg_async_phy2_clk_I0.clk_is_gated				output	
Bit	7	Internal	gcg_async_phy2_clk_I0.clk_is_running				output	
Byte	0x38	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	gcg_cm1_profiling_l3_giclk_I0.clk_is_gated				output	
Bit	1	Internal	gcg_cm1_profiling_l3_giclk_I0.clk_is_running				output	
Bit	2	Internal	gcg_cm1_profiling_l4_giclk_I0.clk_is_gated				output	
Bit	3	Internal	gcg_cm1_profiling_l4_giclk_I0.clk_is_running				output	
Bit	4	Internal	gcg_core_clk_I0.clk_is_gated				output	
Bit	5	Internal	gcg_core_clk_I0.clk_is_running				output	
Bit	6	Internal	gcg_core_dpll_hs_clk_I0.clk_is_gated				output	
Bit	7	Internal	gcg_core_dpll_hs_clk_I0.clk_is_running				output	
Byte	0x39	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	gcg_core_dpll_scrm_clk_I0.clk_is_gated				output	
Bit	1	Internal	gcg_core_dpll_scrm_clk_I0.clk_is_running				output	
Bit	2	Internal	gcg_core_sgx_gfclk_I0.clk_is_gated				output	
Bit	3	Internal	gcg_core_sgx_gfclk_I0.clk_is_running				output	
Bit	4	Internal	gcg_core_x2_clk_I0.clk_is_gated				output	
Bit	5	Internal	gcg_core_x2_clk_I0.clk_is_running				output	
Bit	6	Internal	gcg_div_core_pwadded_I0.clk_is_gated				output	

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Table 18-40. CM1 Observable Signals (continued)

Byte	0x00	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	7	Internal	gcg_div_core_pwadded_I0.clk_is_running				output	
Byte	0x3a	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	gcg_div_iva_hs_clk_pwadded_I0.clk_is_gated				output	
Bit	1	Internal	gcg_div_iva_hs_clk_pwadded_I0.clk_is_running				output	
Bit	2	Internal	gcg_div_mpu_hs_clk_pwadded_I0.clk_is_gated				output	
Bit	3	Internal	gcg_div_mpu_hs_clk_pwadded_I0.clk_is_running				output	
Bit	4	Internal	gcg_dll_clk_div_pwadded_I0.clk_is_gated				output	
Bit	5	Internal	gcg_dll_clk_div_pwadded_I0.clk_is_running				output	
Bit	6	Internal	gcg_dll_x2_clk_I0.clk_is_gated				output	
Bit	7	Internal	gcg_dll_x2_clk_I0.clk_is_running				output	
Byte	0x3b	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	gcg_dpll_abe_x2_clk_I0.clk_is_gated				output	
Bit	1	Internal	gcg_dpll_abe_x2_clk_I0.clk_is_running				output	
Bit	2	Internal	gcg_emac_50mhz_clk_I0.clk_is_gated				output	
Bit	3	Internal	gcg_emac_50mhz_clk_I0.clk_is_running				output	
Bit	4	Internal	gcg_func_24m_clk_pwadded_I0.clk_is_gated				output	
Bit	5	Internal	gcg_func_24m_clk_pwadded_I0.clk_is_running				output	
Bit	6	Internal	gcg_ivahd_root_clk_I0.clk_is_gated				output	
Bit	7	Internal	gcg_ivahd_root_clk_I0.clk_is_running				output	
Byte	0x3c	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	gcg_l3_d2d_giclk_I0.clk_is_gated				output	
Bit	1	Internal	gcg_l3_d2d_giclk_I0.clk_is_running				output	
Bit	2	Internal	gcg_l3_div_pwadded_I0.clk_is_gated				output	
Bit	3	Internal	gcg_l3_div_pwadded_I0.clk_is_running				output	
Bit	4	Internal	gcg_l3_iclk_I0.clk_is_gated				output	
Bit	5	Internal	gcg_l3_iclk_I0.clk_is_running				output	
Bit	6	Internal	gcg_l4_1_giclk_I0.clk_is_gated				output	
Bit	7	Internal	gcg_l4_1_giclk_I0.clk_is_running				output	
Byte	0x3d	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	gcg_l4_2_giclk_I0.clk_is_gated				output	

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Table 18-40. CM1 Observable Signals (continued)

Byte	0x00	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	1	Internal	gcg_l4_2_giclk_I0.clk_is_running				output	
Bit	2	Internal	gcg_l4_cfg_giclk_I0.clk_is_gated				output	
Bit	3	Internal	gcg_l4_cfg_giclk_I0.clk_is_running				output	
Bit	4	Internal	gcg_l4_div_pwadded_I0.clk_is_gated				output	
Bit	5	Internal	gcg_l4_div_pwadded_I0.clk_is_running				output	
Bit	6	Internal	gcg_l4_dma_giclk_I0.clk_is_gated				output	
Bit	7	Internal	gcg_l4_dma_giclk_I0.clk_is_running				output	
Byte	0x3e	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	gcg_l4_emif_giclk_I0.clk_is_gated				output	
Bit	1	Internal	gcg_l4_emif_giclk_I0.clk_is_running				output	
Bit	2	Internal	gcg_l4_iclk_I0.clk_is_gated				output	
Bit	3	Internal	gcg_l4_iclk_I0.clk_is_running				output	
Bit	4	Internal	gcg_l4_init_giclk_I0.clk_is_gated				output	
Bit	5	Internal	gcg_l4_init_giclk_I0.clk_is_running				output	
Bit	6	Internal	gcg_l4_init_giclk_I1.clk_is_gated				output	
Bit	7	Internal	gcg_l4_init_giclk_I1.clk_is_running				output	
Byte	0x3f	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	gcg_l4_instr_giclk_I0.clk_is_gated				output	
Bit	1	Internal	gcg_l4_instr_giclk_I0.clk_is_running				output	
Bit	2	Internal	gcg_l4_per_giclk_I0.clk_is_gated				output	
Bit	3	Internal	gcg_l4_per_giclk_I0.clk_is_running				output	
Bit	4	Internal	gcg_l4_root_clk_I0.clk_is_gated				output	
Bit	5	Internal	gcg_l4_root_clk_I0.clk_is_running				output	
Bit	7:6		Reserved					
Byte	0x40	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	1:0		resreved					
Bit	2	Internal	gcg_lp_clk_div_pwadded_I0.clk_is_gated				output	
Bit	3	Internal	gcg_lp_clk_div_pwadded_I0.clk_is_running				output	
Bit	4	Internal	gcg_mpu_dpll_alwon_clk_I0.clk_is_gated				output	
Bit	5	Internal	gcg_mpu_dpll_alwon_clk_I0.clk_is_running				output	

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Table 18-40. CM1 Observable Signals (continued)

Byte	0x00	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	6	Internal	gcg_mpu_dpll_clk_I0.clk_is_gated				output	
Bit	7	Internal	gcg_mpu_dpll_clk_I0.clk_is_running				output	
Byte	0x41	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	gcg_mpu_dpll_hs_clk_I0.clk_is_gated				output	
Bit	1	Internal	gcg_mpu_dpll_hs_clk_I0.clk_is_running				output	
Bit	2	Internal	gcg_interconn_abe_giclk_I0.clk_is_gated				output	
Bit	3	Internal	gcg_interconn_abe_giclk_I0.clk_is_running				output	
Bit	4	Internal	gcg_interconn_abe_iclk_pwadded_I0.clk_is_gated				output	
Bit	5	Internal	gcg_interconn_abe_iclk_pwadded_I0.clk_is_running				output	
Bit	6	Internal	gcg_pad_gclks_I0.clk_is_gated				output	
Bit	7	Internal	gcg_pad_gclks_I0.clk_is_running				output	
Byte	0x42	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	gcg_per_abe_x1_gfclk_I0.clk_is_gated				output	
Bit	1	Internal	gcg_per_abe_x1_gfclk_I0.clk_is_running				output	
Bit	2	Internal	gcg_per_hs_clk_div_pwadded_I0.clk_is_gated				output	
Bit	3	Internal	gcg_per_hs_clk_div_pwadded_I0.clk_is_running				output	
Bit	4	Internal	gcg_phy_root_clk_I0.clk_is_gated				output	
Bit	5	Internal	gcg_phy_root_clk_I0.clk_is_running				output	
Bit	6	Internal	gcg_slimbus_gclks_I0.clk_is_gated				output	
Bit	7	Internal	gcg_slimbus_gclks_I0.clk_is_running				output	
Byte	0x43	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	gcg_dspss_dpll_alwon_clk_I0.clk_is_gated				output	
Bit	1	Internal	gcg_dspss_dpll_alwon_clk_I0.clk_is_running				output	
Bit	2	Internal	gcg_dspss_root_clk_I0.clk_is_gated				output	
Bit	3	Internal	gcg_dspss_root_clk_I0.clk_is_running				output	
Bit	4	Internal	gcg_usb_hs_clk_div_pwadded_I0.clk_is_gated				output	
Bit	5	Internal	gcg_usb_hs_clk_div_pwadded_I0.clk_is_running				output	
Bit	6	Internal	gat_adll_clk_div_pwadded_I0.clkCtrl				Input	
Bit	7	Internal	gat_cm1_profiling_l3_giclk_I0.clkCtrl				Input	
Byte	0x44	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments

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Table 18-40. CM1 Observable Signals (continued)

Byte	0x00	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	gat_cm1_profiling_l4_giclk_I0.clkCtrl				Input	
Bit	1	Internal	gat_core_clk_I0.clkCtrl				Input	
Bit	2	Internal	gat_core_cortex_m3_clk_I0.clkCtrl				Input	
Bit	3	Internal	gat_core_hsd_byp_clk_mux_pwadded0_I0.clkCtrl				Input	
Bit	4	Internal	gat_core_hsd_byp_clk_mux_pwadded1_I0.clkCtrl				Input	
Bit	5	Internal	gat_div_core_pwadded_I0.clkCtrl				Input	
Bit	6	Internal	gat_div_iva_hs_clk_pwadded_I0.clkCtrl				Input	
Bit	7	Internal	gat_div_mpu_hs_clk_pwadded_I0.clkCtrl				Input	
Byte	0x45	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	gat_dll_clk_div_pwadded_I0.clkCtrl				Input	
Bit	1	Internal	gat_func_24m_clk_pwadded_I0.clkCtrl				Input	
Bit	2	Internal	gat_iva_hsd_byp_clk_mux_pwadded0_I0.clkCtrl				Input	
Bit	3	Internal	gat_iva_hsd_byp_clk_mux_pwadded1_I0.clkCtrl				Input	
Bit	4	Internal	gat_l3_div_pwadded_I0.clkCtrl				Input	
Bit	5	Internal	gat_l3_iclk_I0.clkCtrl				Input	
Bit	6	Internal	gat_l3x2_d2d_giclk_I0.clkCtrl				Input	
Bit	7	Internal	gat_l4_div_pwadded_I0.clkCtrl				Input	
Byte	0x46	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	gat_l4_iclk_I0.clkCtrl				Input	
Bit	1	Internal	gat_l4_root_clk_I0.clkCtrl				Input	
Bit	2	Internal	gat_mpu_dpll_hs_clk_I0.clkCtrl				Input	
Bit	3	Internal	gat_per_hs_clk_div_pwadded_I0.clkCtrl				Input	
Bit	4	Internal	gat_per_hsd_byp_clk_mux_pwadded0_I0.clkCtrl				Input	
Bit	5	Internal	gat_per_hsd_byp_clk_mux_pwadded1_I0.clkCtrl				Input	
Bit	6	Internal	gat_usb_hs_clk_div_pwadded_I0.clkCtrl				Input	
Bit	7		Reserved					
Byte	0x47	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	External	forceactive_cortex_m3_cpu1				Input	
Bit	1	External	forceactive_cortex_m3_cpu2				Input	
Bit	2	External	forceactive_ivahd_seq1				Input	

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Table 18-40. CM1 Observable Signals (continued)

Byte	0x00	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	3	External	forceactive_ivahd_seq2				Input	
Bit	4	External	forceactive_mpu				Input	
Bit	5	External	forceactive_dspss				Input	
Bit	6	External	inhibitsleep_cortex_m3_cpu1				Input	
Bit	7	External	inhibitsleep_cortex_m3_cpu2				Input	
Byte	0x48	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	External	inhibitsleep_ivahd_seq1				Input	
Bit	1	External	inhibitsleep_ivahd_seq2				Input	
Bit	2	External	inhibitsleep_mpu				Input	
Bit	3	External	inhibitsleep_dspss				Input	
Bit	4	Internal	ckctrl_emif_I0.ckstat_mpudpll				output	emu_clkstate_mpu
Bit	5	Internal	ivahd_emu_custom.emu_clkstate_ivahd				output	
Bit	6	Internal	dspss_emu_custom.emu_clkstate_dspss				output	
Bit	7		Reserved					
Byte	0x49	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	emu_ivahd_root_ctrl_clk_I0.ackfsm_state	0	LSB		output	FORCEACKSTATE = "11", BOTHACK = "10"
Bit	1	Internal	emu_ivahd_root_ctrl_clk_I0.ackfsm_state	1	MSB		output	ACKOFF = "01", INHIBACK = "00",
Bit	2	Internal	emu_ivahd_root_ctrl_clk_I0.fsm_state	0	LSB		output	FORCEON = "010"
Bit	3	Internal	emu_ivahd_root_ctrl_clk_I0.fsm_state	1			output	SLEEPDESIREDSTATE = "111",SLEEP2NORMAL = "101",
Bit	4	Internal	emu_ivahd_root_ctrl_clk_I0.fsm_state	2	MSB		output	NORMAL = "000",TOSLEEPD = "001",
Bit	7:5		Reserved					
Byte	0x4a	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	emu_mpu_ctrl_clk_I0.ackfsm_state	0	LSB		output	FORCEACKSTATE = "11", BOTHACK = "10"
Bit	1	Internal	emu_mpu_ctrl_clk_I0.ackfsm_state	1	MSB		output	ACKOFF = "01", INHIBACK = "00",
Bit	2	Internal	emu_mpu_ctrl_clk_I0.fsm_state	0	LSB		output	FORCEON = "010"
Bit	3	Internal	emu_mpu_ctrl_clk_I0.fsm_state	1			output	SLEEPDESIREDSTATE = "111",SLEEP2NORMAL = "101",
Bit	4	Internal	emu_mpu_ctrl_clk_I0.fsm_state	2	MSB		output	NORMAL = "000",TOSLEEPD = "001",
Bit	7:5		Reserved					

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Table 18-40. CM1 Observable Signals (continued)

Byte	0x00	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Byte	0x4b	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	emu_dspss_root_ctrl_clk_I0.ackfsm_state	0	LSB		output	FORCEACKSTATE = "11", BOTHACK = "10"
Bit	1	Internal	emu_dspss_root_ctrl_clk_I0.ackfsm_state	1	MSB		output	ACKOFF = "01", INHIBACK = "00",
Bit	2	Internal	emu_dspss_root_ctrl_clk_I0.fsm_state	0	LSB		output	FORCEON = "010"
Bit	3	Internal	emu_dspss_root_ctrl_clk_I0.fsm_state	1			output	SLEEPDESIREDSTATE = "111",SLEEP2NORMAL = "101",
Bit	4	Internal	emu_dspss_root_ctrl_clk_I0.fsm_state	2	MSB		output	NORMAL = "000",TOSLEEPD = "001",
Bit	7:5		Reserved					
Byte	0x4c	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	prcm_emu_ctrl_clk_ivahd_seq1_st.ackfsm_state	0	LSB		output	FORCEACKSTATE = "11", BOTHACK = "10"
Bit	1	Internal	prcm_emu_ctrl_clk_ivahd_seq1_st.ackfsm_state	1	MSB		output	ACKOFF = "01", INHIBACK = "00",
Bit	2	Internal	prcm_emu_ctrl_clk_ivahd_seq1_st.fsm_state	0	LSB		output	FORCEON = "010"
Bit	3	Internal	prcm_emu_ctrl_clk_ivahd_seq1_st.fsm_state	1			output	SLEEPDESIREDSTATE = "111",SLEEP2NORMAL = "101",
Bit	4	Internal	prcm_emu_ctrl_clk_ivahd_seq1_st.fsm_state	2	MSB		output	NORMAL = "000",TOSLEEPD = "001",
Bit	7:5		Reserved					
Byte	0x4d	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	prcm_emu_ctrl_clk_ivahd_seq2_st.ackfsm_state	0	LSB		output	FORCEACKSTATE = "11", BOTHACK = "10"
Bit	1	Internal	prcm_emu_ctrl_clk_ivahd_seq2_st.ackfsm_state	1	MSB		output	ACKOFF = "01", INHIBACK = "00",
Bit	2	Internal	prcm_emu_ctrl_clk_ivahd_seq2_st.fsm_state	0	LSB		output	FORCEON = "010"
Bit	3	Internal	prcm_emu_ctrl_clk_ivahd_seq2_st.fsm_state	1			output	SLEEPDESIREDSTATE = "111",SLEEP2NORMAL = "101",
Bit	4	Internal	prcm_emu_ctrl_clk_ivahd_seq2_st.fsm_state	2	MSB		output	NORMAL = "000",TOSLEEPD = "001",
Bit	7:5		Reserved					
Byte	0x4e	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	prcm_emu_ctrl_clk_ivahd_dspss_I0.ackfsm_state	0	LSB		output	FORCEACKSTATE = "11", BOTHACK = "10"
Bit	1	Internal	prcm_emu_ctrl_clk_ivahd_dspss_I0.ackfsm_state	1	MSB		output	ACKOFF = "01", INHIBACK = "00",
Bit	2	Internal	prcm_emu_ctrl_clk_ivahd_dspss_I0.fsm_state	0	LSB		output	FORCEON = "010"
Bit	3	Internal	prcm_emu_ctrl_clk_ivahd_dspss_I0.fsm_state	1			output	SLEEPDESIREDSTATE = "111",SLEEP2NORMAL = "101",

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Table 18-40. CM1 Observable Signals (continued)

Byte	0x00	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	4	Internal	prcm_emu_ctrl_clk_ivahd_dspss_I0.fsm_state	2	MSB		output	NORMAL = "000",TOSLEEPD = "001",
Bit	7:5		Reserved					
Byte	0x4f	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	prcm_emu_ctrl_l4_iclk_I0.ackfsm_state	0	LSB		output	FORCEACKSTATE = "11", BOTHACK = "10"
Bit	1	Internal	prcm_emu_ctrl_l4_iclk_I0.ackfsm_state	1	MSB		output	ACKOFF = "01", INHIBACK = "00",
Bit	2	Internal	prcm_emu_ctrl_l4_iclk_I0.fsm_state	0	LSB		output	FORCEON = "010"
Bit	3	Internal	prcm_emu_ctrl_l4_iclk_I0.fsm_state	1			output	SLEEPDESIREDSTATE = "111",SLEEP2NORMAL = "101",
Bit	4	Internal	prcm_emu_ctrl_l4_iclk_I0.fsm_state	2	MSB		output	NORMAL = "000",TOSLEEPD = "001",
Bit	7:5		Reserved					
Byte	0x50	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	prcm_emu_ctrl_l4_root_clk_I0.ackfsm_state	0	LSB		output	FORCEACKSTATE = "11", BOTHACK = "10"
Bit	1	Internal	prcm_emu_ctrl_l4_root_clk_I0.ackfsm_state	1	MSB		output	ACKOFF = "01", INHIBACK = "00",
Bit	2	Internal	prcm_emu_ctrl_l4_root_clk_I0.fsm_state	0	LSB		output	FORCEON = "010"
Bit	3	Internal	prcm_emu_ctrl_l4_root_clk_I0.fsm_state	1			output	SLEEPDESIREDSTATE = "111",SLEEP2NORMAL = "101",
Bit	4	Internal	prcm_emu_ctrl_l4_root_clk_I0.fsm_state	2	MSB		output	NORMAL = "000",TOSLEEPD = "001",
Bit	5	Internal	ctsbuf_ff_cm1_core_x2_clk_I0.y			clock	output	CORE_X2_CLK
Bit	6	Internal	gat_dll_clk_div_pwadded_I0.clkGated			clock	output	DLL_CLK
Bit	7	Internal	gat_mpu_dpll_hs_clk_I0.clkGated			clock	output	MPU_DPLL_HS_CLK
Byte	0x51	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	ctsbuf_ff_cm1_div_iva_hs_clk_I0.y			clock	output	IVA_DPLL_HS_CLK
Bit	1	Internal	gat_core_cortex_m3_clk_I0.clkGated			clock	output	CORE_CORTEX_M3_CLK
Bit	2	Internal	gat_l3x2_d2d_giclk_I0.clkGated			clock	output	L3X2_D2D_GICLK
Bit	3	Internal	shp_l3_d2d_giclk_I0.clkEnabling			clock	output	L3_D2D_GICLK_IEN
Bit	4	Internal	gat_l3_iclk_I0.clkGated			clock	output	L3_ICLK
Bit	5	Internal	gat_cm1_profiling_l3_giclk_I0.clkGated			clock	output	CM1_PROFILING_L3_GICLK
Bit	6	Internal	gat_l4_root_clk_I0.clkGated			clock	output	L4_ROOT_CLK
Bit	7	Internal	gat_cm1_profiling_l4_giclk_I0.clkGated			clock	output	CM1_PROFILING_L4_GICLK

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Table 18-40. CM1 Observable Signals (continued)

Byte	0x00	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Byte	0x52	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	gat_l4_iclk_I0.clkGated			clock	output	L4_ICLK
Bit	1	Internal	dg1_adll_clk_div_I0.div_bus			clock	output	ASYNC_DLL_CLK
Bit	2	Internal	dg1_func_24m_clk_I0.div_bus			clock	output	FUNC_24M_GFCLK
Bit	3	Internal	mux_per_hsd_byp_clk_mux_I0.clk_out			clock	output	PER_HSD_BYP_CLK
Bit	4	Internal	dg1_per_hs_clk_div_I0.div_bus			clock	output	PER_DPLL_HS_CLK
Bit	5	Internal	dg1_usb_hs_clk_div_I0.div_bus			clock	output	USB_DPLL_HS_CLK
Bit	6	Internal	mux_core_hsd_byp_clk_mux_I0.clk_out			clock	output	CORE_PHY_HSD_BYP_CLK
Bit	7	Internal	mux_iva_hsd_byp_clk_mux_I0.clk_out			clock	output	IVA_HSD_BYP_CLK
Byte	0x53	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	spare_cm1_I0.cm1_dss_fclk_in			clock	Input	DSS_FCLK
Bit	1	Internal	freezegen_mpu_mpu_dpll_I0.freeze_Public				output	
Bit	2	Internal	freezegen_dspss_dspss_root_I0.freeze_Public				output	
Bit	7:3		Reserved					

18.4.11.5.9 PRM Subsystem Observable Signals

The General Wakeup Control observability inputs hwobs_int_prm(i), (where i = 0…31) are mapped to the signals debugprm(i),(where i = 0…31) coming out from the power reset manager (PRM) submodule.

Local multiplexing controls at the PRM level are in the PRM_DEBUG_CFG register. The PRM observability output signals are driven on the debugprm(0) through debugprm(7) lines. A certain mux set is selected by programming the PRM_DEBUG_CFG[6:0] SEL0 bit field. The remaining debugprm(8) through debugprm(31) lines are reserved for future use. For more information about the PRM observability source select field, see Section 3.11.2.1, *INTRCONN_SOCKET_PRM Register Summary* in Chapter 3, *Power, Reset, and Clock Management*.

Table 18-41 provides different details about the signals inside the PRM that can be monitored on device hw_dbg pins.

Table 18-41. PRM Observable Signals

Byte	0x00	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	devfsm_I0.osc_clk_out			clock	Input	
Bit	1	Internal	prcm_dev_sysclk_gcg_I0.clk_activity_ctrl				output	
Bit	2	Internal	bgap_stabilization_custom.bgap_is_on				output	
Bit	3	Internal	prcm_dev_merger_I0.pmDomainIsIdle				output	devfsm_I0.device_is_lp
Bit	4	Internal	vfsm_custom_I0.device_in_off_mode				output	
Bit	5	Internal	ldo_custom_I0.bgap_aipoff				output	

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Table 18-41. PRM Observable Signals (continued)

Byte	0x00	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	6	Internal	temporary_device_I1.ls_vddcore_off				output	
Bit	7	Internal	temporary_device_I1.ls_vddcore_wkup_en				output	
Byte	0x01	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	ldo_custom_I0.wkupldosleep				output	
Bit	1	Internal	iocntl_I0.fsm_state	0	LSB		output	
Bit	2	Internal	iocntl_I0.fsm_state	1			output	
Bit	3	Internal	iocntl_I0.fsm_state	2			output	
Bit	4	Internal	iocntl_I0.fsm_state	3			output	
Bit	5	Internal	iocntl_I0.fsm_state	4	MSB		output	
Bit	6	Internal	vdd_status_custom_I0.device_is_on				output	all_vdd_is_on
Bit	7	Internal	device_sarfsm_I0.sar_restore_start				output	
Byte	0x02	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	init_off_cond_custom_I0.init_off_cond				output	
Bit	1	Internal	vfsm_iva_I0.go_off_mode				output	
Bit	2	Internal	bgap_aipoff_custom.go_ls_off_mode				output	
Bit	3	Internal	gpcon_vdd_I0.gp_is_on				output	
Bit	4	Internal	gpcon_vdd_I0.gp_ack				output	
Bit	5	Internal	device_in_off_transition_custom_I0.device_in_off_transition				output	
Bit	6	Internal	vfsm_custom_I0.device_in_off_mode				output	
Bit	7	Internal	bgap_stabilization_custom.bgap_is_on				output	
Byte	0x03	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	vfsm_custom_I0.volt_mpu_domain_dep				output	
Bit	1	Internal	vfsm_custom_I0.volt_iva_domain_dep				output	
Bit	2	Internal	vfsm_custom_I0.volt_core_domain_dep				output	
Bit	3	Internal	vfsm_custom_I0.volt_mpu_domain_wakeup				output	
Bit	4	Internal	vfsm_custom_I0.volt_iva_domain_wakeup				output	
Bit	5	Internal	vfsm_custom_I0.volt_core_domain_wakeup				output	
Bit	7:6		Reserved					

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Table 18-41. PRM Observable Signals (continued)

Byte	0x00	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Byte	0x04	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	vsldo_mpu_I0.sram_vok				output	
Bit	1	Internal	vsldo_mpu_custom.all_sram_off_or_ret				output	
Bit	2	Internal	vsldo_mpu_custom.all_sram_off_or_ret_req				output	
Bit	3	Internal	pscon_override_custom_I0.pscon_mpu_sramvok				output	
Bit	4	Internal	vdd_status_custom_I0.vdd_mpu_domain_is_on				output	
Bit	5	Internal	vdd_status_custom_I0.vdd_iva_domain_is_on				output	
Bit	6	Internal	vdd_status_custom_I0.vdd_core_domain_is_on				output	
Bit	7		Reserved					
Byte	0x05	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	vsldo_iva_I0.sram_vok				output	
Bit	1	Internal	vsldo_iva_custom.all_sram_off_or_ret				output	
Bit	2	Internal	vsldo_iva_custom.all_sram_off_or_ret_req				output	
Bit	3	Internal	pscon_override_custom_I0.pscon_ivahd_sramvok				output	
Bit	4	Internal	pscon_override_custom_I0.pscon_dspss_sramvok				output	
Bit	5	Internal	pscon_override_custom_I0.pscon_audio_sramvok				output	
Bit	7:6		Reserved					
Byte	0x06	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	vsldo_core_I0.sram_vok				output	
Bit	1	Internal	vsldo_core_custom.all_sram_off_or_ret				output	
Bit	2	Internal	vsldo_core_custom.all_sram_off_or_ret_req				output	
Bit	3	Internal	pscon_override_custom_I0.pscon_core_sramvok				output	
Bit	4	Internal	pscon_override_custom_I0.pscon_dss_sramvok				output	
Bit	5	Internal	pscon_override_custom_I0.pscon_gfx_sramvok				output	
Bit	6	Internal	pscon_override_custom_I0.pscon_cam_sramvok				output	
Bit	7	Internal	pscon_override_custom_I0.pscon_l4_per_sramvok				output	
Byte	0x07	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	device_sarfsm_I0.sar_override				output	

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Table 18-41. PRM Observable Signals (continued)

Byte	0x00	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	1	Internal	device_sarfsm_I0.sar_inhibit_frequpdate				output	
Bit	2	Internal	device_sarfsm_I0.sar_stall_reset				output	
Bit	3	Internal	device_sarfsm_I0.sar_sdma_mwakeup				output	
Bit	4	Internal	device_sarfsm_I0.sar_deviceOffWkupAct st				output	
Bit	5	Internal	device_sarfsm_I0.sar_sdma_rst_n				output	
Bit	6	Internal	device_sarfsm_I0.sdma_mstandby				input	
Bit	7	Internal	device_sarfsm_I0.io_nready				input	
Byte	0x08	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	External	cortex_a9_prm_profiling_event	0			input	cortex_a9_cpu0_powerStateSt(0)
Bit	1	External	cortex_a9_prm_profiling_event	1			input	cortex_a9_cpu0_powerStateSt(1)
Bit	2	External	cortex_a9_prm_profiling_event	2			input	cortex_a9_cpu0_logicStateSt
Bit	3	External	cortex_a9_prm_profiling_event	3			input	cortex_a9_cpu0_l1_membankst(0)
Bit	4	External	cortex_a9_prm_profiling_event	4			input	cortex_a9_cpu0_l1_membankst(1)
Bit	5	External	cortex_a9_prm_profiling_event	5			input	cortex_a9_cpu0_inTransition
Bit	7:6		Reserved					SPARE
Byte	0x09	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	External	cortex_a9_prm_profiling_event	6			input	cortex_a9_cpu1_powerStateSt(0)
Bit	1	External	cortex_a9_prm_profiling_event	7			input	cortex_a9_cpu1_powerStateSt(1)
Bit	2	External	cortex_a9_prm_profiling_event	8			input	cortex_a9_cpu1_logicStateSt
Bit	3	External	cortex_a9_prm_profiling_event	9			input	cortex_a9_cpu1_l1_membankst(0)
Bit	4	External	cortex_a9_prm_profiling_event	10			input	cortex_a9_cpu1_l1_membankst(1)
Bit	5	External	cortex_a9_prm_profiling_event	11			input	cortex_a9_cpu1_inTransition
Bit	7:6		Reserved					SPARE
Byte	0x0a	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	7:0		Reserved					SPARE
Byte	0x0b	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	7:0		Reserved					SPARE
Byte	0x0c	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	7:0		Reserved					SPARE
Byte	0x0d	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments

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Table 18-41. PRM Observable Signals (continued)

Byte	0x00	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	7:0		Reserved					SPARE
Byte	0x0e	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	7:0		Reserved					SPARE
Byte	0x0f	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	7:0		Reserved					SPARE
Byte	0x10	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	emu_custom1.dbg_mstandby				output	ifsm_debug_logic_debugss_stby_I0.MStandby
Bit	1	Internal	ifsm_debug_logic_debugss_stby_I0.init_Wait				output	
Bit	2	Internal	ifsm_debug_logic_debugss_stby_I0.module_mwakeup	0			input	
Bit	3	Internal	tfsm_debug_logic_debugss_idle_I0.idleReq				output	
Bit	4	Internal	tfsm_debug_logic_debugss_idle_I0.SidleAck	1			input	
Bit	5	Internal	tfsm_debug_logic_debugss_idle_I0.module_swakeup	0			input	
Bit	6	Internal	tfsm_debug_logic_debugss_idle_I0.fclken_IP				output	
Bit	7		Reserved					
Byte	0x11	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	tfsm_gpio1_gpio_v2_power_I0.idleReq				output	
Bit	1	Internal	tfsm_gpio1_gpio_v2_power_I0.SidleAck	1			input	
Bit	2	Internal	tfsm_gpio1_gpio_v2_power_I0.module_swakeup	0			input	
Bit	3	Internal	tfsm_gpio1_gpio_v2_power_I0.module_swakeup	1			input	
Bit	4	Internal	tfsm_gpio1_gpio_v2_power_I0.fclken_IP				output	
Bit	7:5		Reserved					
Byte	0x12	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	tfsm_keyboard_kbdinterconn_power_I0.idleReq				output	
Bit	1	Internal	tfsm_keyboard_kbdinterconn_power_I0.SidleAck	1			input	
Bit	2	Internal	tfsm_keyboard_kbdinterconn_power_I0.module_swakeup	0			input	
Bit	3	Internal	tfsm_keyboard_kbdinterconn_power_I0.fclken_IP				output	
Bit	4	Internal	tfsm_prm_profiling_I0.idleReq				output	
Bit	5	Internal	tfsm_prm_profiling_I0.SidleAck	1			input	
Bit	6	Internal	tfsm_prm_profiling_I0.module_swakeup	0			input	
Bit	7	Internal	tfsm_prm_profiling_I0.fclken_IP				output	

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Table 18-41. PRM Observable Signals (continued)

Byte	0x00	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Byte	0x13	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	tfsm_rtc_slvp_I0.idleReq				output	
Bit	1	Internal	tfsm_rtc_slvp_I0.SidleAck	1			input	
Bit	2	Internal	tfsm_rtc_slvp_I0.module_swakeup	0			input	
Bit	3	Internal	tfsm_rtc_slvp_I0.fclken_IP				output	
Bit	4	Internal	tfsm_sar_ram_sar_ram_idle_I0.idleReq				output	
Bit	5	Internal	tfsm_sar_ram_sar_ram_idle_I0.SidleAck	1			input	
Bit	6	Internal	tfsm_sar_ram_sar_ram_idle_I0.module_swakeup	0			input	
Bit	7	Internal	tfsm_sar_ram_sar_ram_idle_I0.fclken_IP				output	
Byte	0x14	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	tfsm_synctimer_synctimer32k_power_I0.idleReq				output	
Bit	1	Internal	tfsm_synctimer_synctimer32k_power_I0.SidleAck	1			input	
Bit	2	Internal	tfsm_synctimer_synctimer32k_power_I0.module_swakeup	0			input	
Bit	3	Internal	tfsm_synctimer_synctimer32k_power_I0.fclken_IP				output	
Bit	7:4		Reserved					
Byte	0x15	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	tfsm_timer1_dmtimer_dmc1ms_power_I0.idleReq				output	
Bit	1	Internal	tfsm_timer1_dmtimer_dmc1ms_power_I0.SidleAck	1			input	
Bit	2	Internal	tfsm_timer1_dmtimer_dmc1ms_power_I0.module_swakeup	0			input	
Bit	3	Internal	tfsm_timer1_dmtimer_dmc1ms_power_I0.fclken_IP				output	
Bit	7:4		Reserved					
Byte	0x16	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	3:0		Reserved					
Bit	4	Internal	tfsm_wdt2_watchdoginterconn2_power_I0.idleReq				output	
Bit	5	Internal	tfsm_wdt2_watchdoginterconn2_power_I0.SidleAck	1			input	
Bit	6	Internal	tfsm_wdt2_watchdoginterconn2_power_I0.module_swakeup	0			input	
Bit	7	Internal	tfsm_wdt2_watchdoginterconn2_power_I0.fclken_IP				output	
Byte	0x17	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	tfsm_wkup_l4_interconnect_idle_prot_I0.idleReq				output	

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Table 18-41. PRM Observable Signals (continued)

Byte	0x00	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	1	Internal	tfsm_wkup_l4_interconnect_idle_prot_I0.SidleAck	1			input	
Bit	2	Internal	tfsm_wkup_l4_interconnect_idle_prot_I0.module_swakeup	0			input	
Bit	3	Internal	tfsm_wkup_l4_interconnect_idle_prot_I0.fclken_IP				output	
Bit	4	Internal	mutegen_debug_logic_to_l3_interconnect_2_I0.dyn_domain_mute				output	
Bit	5	Internal	mutegen_debug_logic_to_l3_interconnect_2_I0.static_domain_mute				output	
Bit	6	Internal	mutegen_debug_logic_to_l3_interconnect_2_I0.public_active	0			input	
Bit	7		Reserved					
Byte	0x18	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	cmfsm_emu_emu_sys_I0.domain_is_on				input	
Bit	1	Internal	cmfsm_emu_emu_sys_I0.domain_wakeup				input	
Bit	2	Internal	cmfsm_emu_emu_sys_I0.domain_wkup_ack				output	
Bit	3	Internal	cmfsm_emu_emu_sys_I0.fsm_state	0	LSB		output	ACT2INACT2 = "101"
Bit	4	Internal	cmfsm_emu_emu_sys_I0.fsm_state	1			output	ACTIVE = "011", ACT2INACT1 = "111",
Bit	5	Internal	cmfsm_emu_emu_sys_I0.fsm_state	2	MSB		output	INACTIVE = "000", INACT2ACT = "001",
Bit	7:6		Reserved					
Byte	0x19	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	mux_l4_wkup_clk_mux_I0.clk_out			clock	output	L4_WKUP_ICLK
Bit	1	Internal	cmfsm_wkup_l4_wkup_I0.domain_is_on				input	
Bit	2	Internal	cmfsm_wkup_l4_wkup_I0.domain_wakeup				input	
Bit	3	Internal	cmfsm_wkup_l4_wkup_I0.domain_wkup_ack				output	
Bit	4	Internal	cmfsm_wkup_l4_wkup_I0.fsm_state	0	LSB		output	ACT2INACT2 = "101"
Bit	5	Internal	cmfsm_wkup_l4_wkup_I0.fsm_state	1			output	ACTIVE = "011", ACT2INACT1 = "111",
Bit	6	Internal	cmfsm_wkup_l4_wkup_I0.fsm_state	2	MSB		output	INACTIVE = "000", INACT2ACT = "001",
Bit	7	Internal	cm2prm_core_cm1_I0.pmDomainIsIdle				output	
Byte	0x1a	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	gcg_cm1_sys_clk_I0.clk_is_gated				output	
Bit	1	Internal	gcg_cm1_sys_clk_I0.clk_is_running				output	
Bit	2	Internal	gcg_core_dpll_alwon_clk_I0.clk_is_gated				output	

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Table 18-41. PRM Observable Signals (continued)

Byte	0x00	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	3	Internal	gcg_core_dpll_alwon_clk_I0.clk_is_running				output	
Bit	4	Internal	gcg_core_dpll_emu_clk_I0.clk_is_gated				output	
Bit	5	Internal	gcg_core_dpll_emu_clk_I0.clk_is_running				output	
Bit	6	Internal	gcg_dss_alwon_sys_clk_I0.clk_is_gated				output	
Bit	7	Internal	gcg_dss_alwon_sys_clk_I0.clk_is_running				output	
Byte	0x1b	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	gcg_emu_sys_clk_I0.clk_is_gated				output	
Bit	1	Internal	gcg_emu_sys_clk_I0.clk_is_running				output	
Bit	2	Internal	gcg_emu_sys_clk_gate_I0.clk_is_gated				output	
Bit	3	Internal	gcg_emu_sys_clk_gate_I0.clk_is_running				output	
Bit	4	Internal	gcg_l4_wkup_gclk_I0.clk_is_gated				output	
Bit	5	Internal	gcg_l4_wkup_gclk_I0.clk_is_running				output	
Bit	6	Internal	gcg_l4_wkup_giclk_I0.clk_is_gated				output	
Bit	7	Internal	gcg_l4_wkup_giclk_I0.clk_is_running				output	
Byte	0x1c	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	gcg_l4_wkup_profiling_gclk_I0.clk_is_gated				output	
Bit	1	Internal	gcg_l4_wkup_profiling_gclk_I0.clk_is_running				output	
Bit	2	Internal	gcg_std_efuse_sys_clk_I0.clk_is_gated				output	
Bit	3	Internal	gcg_std_efuse_sys_clk_I0.clk_is_running				output	
Bit	4	Internal	gcg_syc_clk_div_pwadded_I0.clk_is_gated				output	
Bit	5	Internal	gcg_syc_clk_div_pwadded_I0.clk_is_running				output	
Bit	7:6		Reserved					
Byte	0x1d	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	1:0		Reserved					
Bit	2	Internal	gcg_wkup_32k_gfclk_I0.clk_is_gated				output	
Bit	3	Internal	gcg_wkup_32k_gfclk_I0.clk_is_running				output	
Bit	4	Internal	prcm_dev_sysclk_gcg_I0.clk_is_gated				output	
Bit	5	Internal	prcm_dev_sysclk_gcg_I0.clk_is_running				output	

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Table 18-41. PRM Observable Signals (continued)

Byte	0x00	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	6	Internal	gat_abe_alwon_32k_clk_I0.clkCtrl				input	
Bit	7	Internal	gat_abe_dpll_bypass_clk_mux_pwadded0_I0.clkCtrl				input	
Byte	0x1e	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	gat_abe_dpll_bypass_clk_mux_pwadded1_I0.clkCtrl				input	
Bit	1	Internal	gat_abe_dpll_refclk_mux_pwadded0_I0.clkCtrl				input	
Bit	2	Internal	gat_abe_dpll_refclk_mux_pwadded1_I0.clkCtrl				input	
Bit	3	Internal	gat_abe_sysclk_I0.clkCtrl				input	
Bit	4	Internal	gat_cm1_sys_clk_I0.clkCtrl				input	
Bit	5	Internal	gat_cm2_dm10_mux_pwadded0_I0.clkCtrl				input	
Bit	6	Internal	gat_cm2_dm10_mux_pwadded1_I0.clkCtrl				input	
Bit	7	Internal	gat_cm2_dm11_mux_pwadded0_I0.clkCtrl				input	
Byte	0x1f	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	gat_cm2_dm11_mux_pwadded1_I0.clkCtrl				input	
Bit	1	Internal	gat_cm2_dm2_mux_pwadded0_I0.clkCtrl				input	
Bit	2	Internal	gat_cm2_dm2_mux_pwadded1_I0.clkCtrl				input	
Bit	3	Internal	gat_cm2_dm3_mux_pwadded0_I0.clkCtrl				input	
Bit	4	Internal	gat_cm2_dm3_mux_pwadded1_I0.clkCtrl				input	
Bit	5	Internal	gat_cm2_dm4_mux_pwadded0_I0.clkCtrl				input	
Bit	6	Internal	gat_cm2_dm4_mux_pwadded1_I0.clkCtrl				input	
Bit	7	Internal	gat_cm2_dm9_mux_pwadded0_I0.clkCtrl				input	
Byte	0x20	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	gat_cm2_dm9_mux_pwadded1_I0.clkCtrl				input	
Bit	1	Internal	gat_core_alwon_32k_gfclk_I0.clkCtrl				input	
Bit	2	Internal	gat_core_dpll_alwon_clk_I0.clkCtrl				input	
Bit	3		Reserved					
Bit	4	Internal	gat_dmt1_clk_mux_pwadded0_I0.clkCtrl				input	
Bit	5	Internal	gat_dmt1_clk_mux_pwadded1_I0.clkCtrl				input	
Bit	6	Internal	gat_dss_alwon_sys_clk_I0.clkCtrl				input	

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Table 18-41. PRM Observable Signals (continued)

Byte	0x00	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	7	Internal	gat_emu_sys_clk_I0.clkCtrl				input	
Byte	0x21	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	gat_l4_wkup_clk_mux_pwadded0_I0.clkCtrl				input	
Bit	1	Internal	gat_l4_wkup_clk_mux_pwadded1_I0.clkCtrl				input	
Bit	2	Internal	gat_l4_wkup_gclk_I0.clkCtrl				input	
Bit	3	Internal	gat_l4_wkup_giclk_I0.clkCtrl				input	
Bit	4	Internal	gat_l4_wkup_profiling_gclk_I0.clkCtrl				input	
Bit	5	Internal	gat_mpu_dpll_alwon_clk_I0.clkCtrl				input	
Bit	6	Internal	gat_per_32k_gfclk_I0.clkCtrl				input	
Bit	7	Internal	gat_per_dpll_alwon_clk_I0.clkCtrl				input	
Byte	0x22	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	gat_per_sys_gfclk_I0.clkCtrl				input	
Bit	1	Internal	gat_sr_core_sysclk_I0.clkCtrl				input	
Bit	2	Internal	gat_sr_iva_sysclk_I0.clkCtrl				input	
Bit	3	Internal	gat_sr_mpu_sysclk_I0.clkCtrl				input	
Bit	4	Internal	gat_std_efuse_sys_clk_I0.clkCtrl				input	
Bit	5	Internal	gat_syc_clk_div_pwadded_I0.clkCtrl				input	
Bit	6	Internal	gat_dspss_dpll_alwon_clk_I0.clkCtrl				input	
Bit	7	Internal	gat_unipro_dpll_clk_I0.clkCtrl				input	
Byte	0x23	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	gat_usb_dpll_clk_I0.clkCtrl				input	
Bit	2:1		Reserved					
Bit	3	Internal	gat_wkup_32k_gfclk_I0.clkCtrl				input	
Bit	7:4		Reserved					
Byte	0x24	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	pmfsm_audio_I0.done			act like	output	
Bit	1	Internal	pmfsm_audio_I0.fsm_state	0	LSB		output	INACTIVE2ONISO = "11010", INACTIVE2ONNOISO = "11011", INACTIVE2ONRST = "11100", UPDATE2OFF = "11101", UPDATE2RETL = "11110", UPDATE2RETH = "11111"

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Table 18-41. PRM Observable Signals (continued)

Byte	0x00	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	2	Internal	pmfsm_audio_I0.fsm_state	1			output	RETL2ONNOISO = "10100", RETH2ONNOISO = "10101", OFF2ONRST = "10110", RETL2ONRST = "10111", RETH2ONRST = "11000", INACTIVE2ON = "11001",
Bit	3	Internal	pmfsm_audio_I0.fsm_state	2			output	RETL2ON = "01110", RETH2ON = "01111", OFF2ONISO = "10000", RETL2ONISO = "10001", RETH2ONISO = "10010", OFF2ONNOISO = "10011",
Bit	4	Internal	pmfsm_audio_I0.fsm_state	3			output	ON2OFF = "00111", ON2RETL = "01000", ON2RETH = "01001", OFFSTATE = "01010", RETL = "01011", RETH = "01100", OFF2ON = "01101",
Bit	5	Internal	pmfsm_audio_I0.fsm_state	4	MSB		output	RESET = "00000", CHANGEMEM = "00001", ONSTATE = "00010", STATEUPDATE = "00011", INACTIVE = "00100", ON2INACT = "00101", INACT2ON = "00110",
Bit	7:6		Reserved					
Byte	0x25	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	pmfsm_cam_I0.done			act like	output	
Bit	1	Internal	pmfsm_cam_I0.fsm_state	0	LSB		output	INACTIVE2ONISO = "11010", INACTIVE2ONNOISO = "11011", INACTIVE2ONRST = "11100", UPDATE2OFF = "11101", UPDATE2RETL = "11110", UPDATE2RETH = "11111"
Bit	2	Internal	pmfsm_cam_I0.fsm_state	1			output	RETL2ONNOISO = "10100", RETH2ONNOISO = "10101", OFF2ONRST = "10110", RETL2ONRST = "10111", RETH2ONRST = "11000", INACTIVE2ON = "11001",
Bit	3	Internal	pmfsm_cam_I0.fsm_state	2			output	RETL2ON = "01110", RETH2ON = "01111", OFF2ONISO = "10000", RETL2ONISO = "10001", RETH2ONISO = "10010", OFF2ONNOISO = "10011",
Bit	4	Internal	pmfsm_cam_I0.fsm_state	3			output	ON2OFF = "00111", ON2RETL = "01000", ON2RETH = "01001", OFFSTATE = "01010", RETL = "01011", RETH = "01100", OFF2ON = "01101",
Bit	5	Internal	pmfsm_cam_I0.fsm_state	4	MSB		output	RESET = "00000", CHANGEMEM = "00001", ONSTATE = "00010", STATEUPDATE = "00011", INACTIVE = "00100", ON2INACT = "00101", INACT2ON = "00110",
Bit	7:6		Reserved					
Byte	0x26	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	pmfsm_core_I0.done			act like	output	
Bit	1	Internal	pmfsm_core_I0.fsm_state	0	LSB		output	INACTIVE2ONISO = "11010", INACTIVE2ONNOISO = "11011", INACTIVE2ONRST = "11100", UPDATE2OFF = "11101", UPDATE2RETL = "11110", UPDATE2RETH = "11111"
Bit	2	Internal	pmfsm_core_I0.fsm_state	1			output	RETL2ONNOISO = "10100", RETH2ONNOISO = "10101", OFF2ONRST = "10110", RETL2ONRST = "10111", RETH2ONRST = "11000", INACTIVE2ON = "11001",
Bit	3	Internal	pmfsm_core_I0.fsm_state	2			output	RETL2ON = "01110", RETH2ON = "01111", OFF2ONISO = "10000", RETL2ONISO = "10001", RETH2ONISO = "10010", OFF2ONNOISO = "10011",

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Table 18-41. PRM Observable Signals (continued)

Byte	0x00	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	4	Internal	pmfsm_core_I0.fsm_state	3			output	ON2OFF = "00111", ON2RETL = "01000", ON2RETH = "01001", OFFSTATE = "01010", RETL = "01011", RETH = "01100", OFF2ON = "01101",
Bit	5	Internal	pmfsm_core_I0.fsm_state	4	MSB		output	RESET = "00000", CHANGEMEM = "00001", ONSTATE = "00010", STATEUPDATE = "00011", INACTIVE = "00100", ON2INACT = "00101", INACT2ON = "00110",
Bit	7:6		Reserved					
Byte	0x27	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	7:0		Reserved					
Byte	0x28	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	pmfsm_dss_I0.done			act like	output	
Bit	1	Internal	pmfsm_dss_I0.fsm_state	0	LSB		output	INACTIVE2ONISO = "11010", INACTIVE2ONNOISO = "11011", INACTIVE2ONRST = "11100", UPDATE2OFF = "11101", UPDATE2RETL = "11110", UPDATE2RETH = "11111"
Bit	2	Internal	pmfsm_dss_I0.fsm_state	1			output	RETL2ONNOISO = "10100", RETH2ONNOISO = "10101", OFF2ONRST = "10110", RETL2ONRST = "10111", RETH2ONRST = "11000", INACTIVE2ON = "11001",
Bit	3	Internal	pmfsm_dss_I0.fsm_state	2			output	RETL2ON = "01110", RETH2ON = "01111", OFF2ONISO = "10000", RETL2ONISO = "10001", RETH2ONISO = "10010", OFF2ONNOISO = "10011",
Bit	4	Internal	pmfsm_dss_I0.fsm_state	3			output	ON2OFF = "00111", ON2RETL = "01000", ON2RETH = "01001", OFFSTATE = "01010", RETL = "01011", RETH = "01100", OFF2ON = "01101",
Bit	5	Internal	pmfsm_dss_I0.fsm_state	4	MSB		output	RESET = "00000", CHANGEMEM = "00001", ONSTATE = "00010", STATEUPDATE = "00011", INACTIVE = "00100", ON2INACT = "00101", INACT2ON = "00110",
Bit	7:6		Reserved					
Byte	0x29	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	pmfsm_emu_I0.done			act like	output	
Bit	1	Internal	pmfsm_emu_I0.fsm_state	0	LSB		output	INACTIVE2ONISO = "11010", INACTIVE2ONNOISO = "11011", INACTIVE2ONRST = "11100", UPDATE2OFF = "11101", UPDATE2RETL = "11110", UPDATE2RETH = "11111"
Bit	2	Internal	pmfsm_emu_I0.fsm_state	1			output	RETL2ONNOISO = "10100", RETH2ONNOISO = "10101", OFF2ONRST = "10110", RETL2ONRST = "10111", RETH2ONRST = "11000", INACTIVE2ON = "11001",
Bit	3	Internal	pmfsm_emu_I0.fsm_state	2			output	RETL2ON = "01110", RETH2ON = "01111", OFF2ONISO = "10000", RETL2ONISO = "10001", RETH2ONISO = "10010", OFF2ONNOISO = "10011",
Bit	4	Internal	pmfsm_emu_I0.fsm_state	3			output	ON2OFF = "00111", ON2RETL = "01000", ON2RETH = "01001", OFFSTATE = "01010", RETL = "01011", RETH = "01100", OFF2ON = "01101",

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Table 18-41. PRM Observable Signals (continued)

Byte	0x00	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	5	Internal	pmfsm_emu_I0.fsm_state	4	MSB		output	RESET = "00000", CHANGEMEM = "00001", ONSTATE = "00010", STATEUPDATE = "00011", INACTIVE = "00100", ON2INACT = "00101", INACT2ON = "00110",
Bit	7:6		Reserved					
Byte	0x2a	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	pmfsm_gfx_I0.done			active like	output	
Bit	1	Internal	pmfsm_gfx_I0.fsm_state	0	LSB		output	INACTIVE2ONISO = "11010", INACTIVE2ONNOISO = "11011", INACTIVE2ONRST = "11100", UPDATE2OFF = "11101", UPDATE2RETL = "11110", UPDATE2RETH = "11111"
Bit	2	Internal	pmfsm_gfx_I0.fsm_state	1			output	RETL2ONNOISO = "10100", RETH2ONNOISO = "10101", OFF2ONRST = "10110", RETL2ONRST = "10111", RETH2ONRST = "11000", INACTIVE2ON = "11001",
Bit	3	Internal	pmfsm_gfx_I0.fsm_state	2			output	RETL2ON = "01110", RETH2ON = "01111", OFF2ONISO = "10000", RETL2ONISO = "10001", RETH2ONISO = "10010", OFF2ONNOISO = "10011",
Bit	4	Internal	pmfsm_gfx_I0.fsm_state	3			output	ON2OFF = "00111", ON2RETL = "01000", ON2RETH = "01001", OFFSTATE = "01010", RETL = "01011", RETH = "01100", OFF2ON = "01101",
Bit	5	Internal	pmfsm_gfx_I0.fsm_state	4	MSB		output	RESET = "00000", CHANGEMEM = "00001", ONSTATE = "00010", STATEUPDATE = "00011", INACTIVE = "00100", ON2INACT = "00101", INACT2ON = "00110",
Bit	7:6		Reserved					
Byte	0x2b	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	pmfsm_ivahd_I0.done			active like	output	
Bit	1	Internal	pmfsm_ivahd_I0.fsm_state	0	LSB		output	INACTIVE2ONISO = "11010", INACTIVE2ONNOISO = "11011", INACTIVE2ONRST = "11100", UPDATE2OFF = "11101", UPDATE2RETL = "11110", UPDATE2RETH = "11111"
Bit	2	Internal	pmfsm_ivahd_I0.fsm_state	1			output	RETL2ONNOISO = "10100", RETH2ONNOISO = "10101", OFF2ONRST = "10110", RETL2ONRST = "10111", RETH2ONRST = "11000", INACTIVE2ON = "11001",
Bit	3	Internal	pmfsm_ivahd_I0.fsm_state	2			output	RETL2ON = "01110", RETH2ON = "01111", OFF2ONISO = "10000", RETL2ONISO = "10001", RETH2ONISO = "10010", OFF2ONNOISO = "10011",
Bit	4	Internal	pmfsm_ivahd_I0.fsm_state	3			output	ON2OFF = "00111", ON2RETL = "01000", ON2RETH = "01001", OFFSTATE = "01010", RETL = "01011", RETH = "01100", OFF2ON = "01101",
Bit	5	Internal	pmfsm_ivahd_I0.fsm_state	4	MSB		output	RESET = "00000", CHANGEMEM = "00001", ONSTATE = "00010", STATEUPDATE = "00011", INACTIVE = "00100", ON2INACT = "00101", INACT2ON = "00110",
Bit	7:6		Reserved					
Byte	0x2c	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments

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Table 18-41. PRM Observable Signals (continued)

Byte	0x00	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	pmfsm_l3_init_I0.done			act like	output	
Bit	1	Internal	pmfsm_l3_init_I0.fsm_state	0	LSB		output	INACTIVE2ONISO = "11010", INACTIVE2ONNOISO = "11011", INACTIVE2ONRST = "11100", UPDATE2OFF = "11101", UPDATE2RETL = "11110", UPDATE2RETH = "11111"
Bit	2	Internal	pmfsm_l3_init_I0.fsm_state	1			output	RETL2ONNOISO = "10100", RETH2ONNOISO = "10101", OFF2ONRST = "10110", RETL2ONRST = "10111", RETH2ONRST = "11000", INACTIVE2ON = "11001",
Bit	3	Internal	pmfsm_l3_init_I0.fsm_state	2			output	RETL2ON = "01110", RETH2ON = "01111", OFF2ONISO = "10000", RETL2ONISO = "10001", RETH2ONISO = "10010", OFF2ONNOISO = "10011",
Bit	4	Internal	pmfsm_l3_init_I0.fsm_state	3			output	ON2OFF = "00111", ON2RETL = "01000", ON2RETH = "01001", OFFSTATE = "01010", RETL = "01011", RETH = "01100", OFF2ON = "01101",
Bit	5	Internal	pmfsm_l3_init_I0.fsm_state	4	MSB		output	RESET = "00000", CHANGEMEM = "00001", ONSTATE = "00010", STATEUPDATE = "00011", INACTIVE = "00100", ON2INACT = "00101", INACT2ON = "00110",
Bit	7:6		Reserved					
Byte	0x2d	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	pmfsm_l4_per_I0.done			act like	output	
Bit	1	Internal	pmfsm_l4_per_I0.fsm_state	0	LSB		output	INACTIVE2ONISO = "11010", INACTIVE2ONNOISO = "11011", INACTIVE2ONRST = "11100", UPDATE2OFF = "11101", UPDATE2RETL = "11110", UPDATE2RETH = "11111"
Bit	2	Internal	pmfsm_l4_per_I0.fsm_state	1			output	RETL2ONNOISO = "10100", RETH2ONNOISO = "10101", OFF2ONRST = "10110", RETL2ONRST = "10111", RETH2ONRST = "11000", INACTIVE2ON = "11001",
Bit	3	Internal	pmfsm_l4_per_I0.fsm_state	2			output	RETL2ON = "01110", RETH2ON = "01111", OFF2ONISO = "10000", RETL2ONISO = "10001", RETH2ONISO = "10010", OFF2ONNOISO = "10011",
Bit	4	Internal	pmfsm_l4_per_I0.fsm_state	3			output	ON2OFF = "00111", ON2RETL = "01000", ON2RETH = "01001", OFFSTATE = "01010", RETL = "01011", RETH = "01100", OFF2ON = "01101",
Bit	5	Internal	pmfsm_l4_per_I0.fsm_state	4	MSB		output	RESET = "00000", CHANGEMEM = "00001", ONSTATE = "00010", STATEUPDATE = "00011", INACTIVE = "00100", ON2INACT = "00101", INACT2ON = "00110",
Bit	7:6		Reserved					
Byte	0x2e	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	pmfsm_mpu_I0.done			act like	output	
Bit	1	Internal	pmfsm_mpu_I0.fsm_state	0	LSB		output	INACTIVE2ONISO = "11010", INACTIVE2ONNOISO = "11011", INACTIVE2ONRST = "11100", UPDATE2OFF = "11101", UPDATE2RETL = "11110", UPDATE2RETH = "11111"

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Table 18-41. PRM Observable Signals (continued)

Byte	0x00	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	2	Internal	pmfsm_mpu_I0.fsm_state	1			output	RETL2ONNOISO = "10100", RETH2ONNOISO = "10101", OFF2ONRST = "10110", RETL2ONRST = "10111", RETH2ONRST = "11000", INACTIVE2ON = "11001",
Bit	3	Internal	pmfsm_mpu_I0.fsm_state	2			output	RETL2ON = "01110", RETH2ON = "01111", OFF2ONISO = "10000", RETL2ONISO = "10001", RETH2ONISO = "10010", OFF2ONNOISO = "10011",
Bit	4	Internal	pmfsm_mpu_I0.fsm_state	3			output	ON2OFF = "00111", ON2RETL = "01000", ON2RETH = "01001", OFFSTATE = "01010", RETL = "01011", RETH = "01100", OFF2ON = "01101",
Bit	5	Internal	pmfsm_mpu_I0.fsm_state	4	MSB		output	RESET = "00000", CHANGEMEM = "00001", ONSTATE = "00010", STATEUPDATE = "00011", INACTIVE = "00100", ON2INACT = "00101", INACT2ON = "00110",
Bit	7:6		Reserved					
Byte	0x2f	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	pmfsm_dspss_I0.done			act like	output	
Bit	1	Internal	pmfsm_dspss_I0.fsm_state	0	LSB		output	INACTIVE2ONISO = "11010", INACTIVE2ONNOISO = "11011", INACTIVE2ONRST = "11100", UPDATE2OFF = "11101", UPDATE2RETL = "11110", UPDATE2RETH = "11111"
Bit	2	Internal	pmfsm_dspss_I0.fsm_state	1			output	RETL2ONNOISO = "10100", RETH2ONNOISO = "10101", OFF2ONRST = "10110", RETL2ONRST = "10111", RETH2ONRST = "11000", INACTIVE2ON = "11001",
Bit	3	Internal	pmfsm_dspss_I0.fsm_state	2			output	RETL2ON = "01110", RETH2ON = "01111", OFF2ONISO = "10000", RETL2ONISO = "10001", RETH2ONISO = "10010", OFF2ONNOISO = "10011",
Bit	4	Internal	pmfsm_dspss_I0.fsm_state	3			output	ON2OFF = "00111", ON2RETL = "01000", ON2RETH = "01001", OFFSTATE = "01010", RETL = "01011", RETH = "01100", OFF2ON = "01101",
Bit	5	Internal	pmfsm_dspss_I0.fsm_state	4	MSB		output	RESET = "00000", CHANGEMEM = "00001", ONSTATE = "00010", STATEUPDATE = "00011", INACTIVE = "00100", ON2INACT = "00101", INACT2ON = "00110",
Bit	6	Internal	pscon_audio_I0.pgoodout	0			input	
Bit	7	Internal	pscon_audio_I0.ret				output	
Byte	0x30	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	pscon_cam_I0.pgoodout	0			input	
Bit	1	Internal	pscon_core_I0.pgoodout	0			input	
Bit	2	Internal	pscon_core_I0.ret				output	
Bit	3		Reserved					
Bit	4	Internal	pscon_dss_I0.pgoodout	0			input	
Bit	5	Internal	pscon_dss_I0.ret				output	

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Table 18-41. PRM Observable Signals (continued)

Byte	0x00	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	6	Internal	pscon_emu_I0.pgoodout	0			input	
Bit	7	Internal	pscon_gfx_I0.pgoodout	0			input	
Byte	0x31	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	pscon_ivahd_I0.pgoodout	0			input	
Bit	1	Internal	pscon_ivahd_I0.ret				output	
Bit	2	Internal	pscon_l3_init_I0.pgoodout	0			input	
Bit	3	Internal	pscon_l3_init_I0.ret				output	
Bit	4	Internal	pscon_l4_per_I0.pgoodout	0			input	
Bit	5	Internal	pscon_l4_per_I0.ret				output	
Bit	6	Internal	pscon_mpu_I0.pgoodout	0			input	
Bit	7	Internal	pscon_mpu_I0.ret				output	
Byte	0x32	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	pscon_std_efuse_I0.pgoodout	0			input	
Bit	1	Internal	pscon_dspss_I0.pgoodout	0			input	
Bit	2	Internal	pscon_dspss_I0.ret				output	
Bit	3	Internal	wkupctrl_always_on_core_l4_ao_I0.domain_wakeup				output	
Bit	4	Internal	wkupctrl_always_on_core_l4_ao_I0.domain_wkup_ack				input	
Bit	5	Internal	wkupctrl_audio_interconn_abe_I0.domain_wakeup				output	
Bit	6	Internal	wkupctrl_audio_interconn_abe_I0.domain_wkup_ack				input	
Bit	7		Reserved					
Byte	0x33	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	wkupctrl_cam_iss_I0.domain_wakeup				output	
Bit	1	Internal	wkupctrl_cam_iss_I0.domain_wkup_ack				input	
Bit	2	Internal	wkupctrl_core_cm1_I0.domain_wakeup				output	
Bit	3	Internal	wkupctrl_core_cm1_I0.domain_wkup_ack				input	
Bit	4	Internal	wkupctrl_core_cortex_m3_I0.domain_wakeup				output	
Bit	5	Internal	wkupctrl_core_cortex_m3_I0.domain_wkup_ack				input	
Bit	6	Internal	wkupctrl_core_l3_1_I0.domain_wakeup				output	

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Table 18-41. PRM Observable Signals (continued)

Byte	0x00	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	7	Internal	wkupctrl_core_l3_1_I0.domain_wkup_ack				input	
Byte	0x34	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	wkupctrl_core_l3_2_I0.domain_wakeup				output	
Bit	1	Internal	wkupctrl_core_l3_2_I0.domain_wkup_ack				input	
Bit	2	Internal	wkupctrl_core_l3_dma_I0.domain_wakeup				output	
Bit	3	Internal	wkupctrl_core_l3_dma_I0.domain_wkup_ack				input	
Bit	4	Internal	wkupctrl_core_l3_emif_I0.domain_wakeup				output	
Bit	5	Internal	wkupctrl_core_l3_emif_I0.domain_wkup_ack				input	
Bit	6	Internal	wkupctrl_core_l3_instr_I0.domain_wakeup				output	
Bit	7	Internal	wkupctrl_core_l3_instr_I0.domain_wkup_ack				input	
Byte	0x35	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	wkupctrl_core_l3x2_d2d_I0.domain_wakeup				output	
Bit	1	Internal	wkupctrl_core_l3x2_d2d_I0.domain_wkup_ack				input	
Bit	2	Internal	wkupctrl_core_l4_cfg_I0.domain_wakeup				output	
Bit	3	Internal	wkupctrl_core_l4_cfg_I0.domain_wkup_ack				input	
Bit	5:4		Reserved					
Bit	6	Internal	wkupctrl_dss_l3_dss_I0.domain_wakeup				output	
Bit	7	Internal	wkupctrl_dss_l3_dss_I0.domain_wkup_ack				input	
Byte	0x36	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	wkupctrl_emu_emu_sys_I0.domain_wakeup				output	
Bit	1	Internal	wkupctrl_emu_emu_sys_I0.domain_wkup_ack				input	
Bit	2	Internal	wkupctrl_gfx_l3_gfx_I0.domain_wakeup				output	
Bit	3	Internal	wkupctrl_gfx_l3_gfx_I0.domain_wkup_ack				input	
Bit	4	Internal	wkupctrl_ivahd_ivahd_root_I0.domain_wakeup				output	
Bit	5	Internal	wkupctrl_ivahd_ivahd_root_I0.domain_wkup_ack				input	
Bit	6	Internal	wkupctrl_l3_init_l3_init_I0.domain_wakeup				output	
Bit	7	Internal	wkupctrl_l3_init_l3_init_I0.domain_wkup_ack				input	
Byte	0x37	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments

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Table 18-41. PRM Observable Signals (continued)

Byte	0x00	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	wkupctrl_l4_per_l4_per_l0.domain_wakeup				output	
Bit	1	Internal	wkupctrl_l4_per_l4_per_l0.domain_wkup_ack				input	
Bit	3:2		Reserved					
Bit	4	Internal	wkupctrl_mpu_mpu_dpll_l0.domain_wakeup				output	
Bit	5	Internal	wkupctrl_mpu_mpu_dpll_l0.domain_wkup_ack				input	
Bit	6	Internal	wkupctrl_dspss_dspss_root_l0.domain_wakeup				output	
Bit	7	Internal	wkupctrl_dspss_dspss_root_l0.domain_wkup_ack				input	
Byte	0x38	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	wkupctrl_wkup_l4_wkup_l0.domain_wakeup				output	
Bit	1	Internal	wkupctrl_wkup_l4_wkup_l0.domain_wkup_ack				input	
Bit	2	Internal	inv_glbl_sw_rst_custom.ro_rst_globalcold_sw_n				output	
Bit	3	External	icepickpor_rst_n				input	
Bit	4	External	sys_pwron_arst_n				input	
Bit	5	Internal	inv_glbl_sw_rst_custom.ro_rst_globalwarm_sw_n				output	
Bit	6	External	icepick_rst_n				input	
Bit	7		reset					
Byte	0x39	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	External	mpu_wdt_rst_n				input	
Bit	1		Reserved					
Bit	2	External	sys_warmin_arst_n				input	
Bit	3	External	c2c_warm_rst				input	
Bit	4	External	audio_pwron_rst_n				output	
Bit	5	External	audio_rst_n				output	
Bit	6	External	always_on_cm1_pwron_rst_n				output	
Bit	7	External	always_on_cm1_rst_n				output	
Byte	0x3a	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	External	always_on_core_pwron_rst				output	
Bit	1	External	always_on_core_rst_n				output	
Bit	2	External	always_on_iva_rst_n				output	

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Table 18-41. PRM Observable Signals (continued)

Byte	0x00	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	3	External	always_on_mpu_rst_n				output	
Bit	4	External	cam_rst_n				output	
Bit	5	External	cm2_pwron_ret_rst_n				output	
Bit	6	External	cm2_ret_rst_n				output	
Bit	7	External	core_pwron_ret_rst_n				output	
Byte	0x3b	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	External	core_ret_rst_n				output	
Bit	1	External	core_rst_n				output	
Bit	2		Reserved					
Bit	3	External	dll_rst_n				output	
Bit	4	External	dpll_iva_pwron_rst				output	
Bit	5	External	dpll_l3_init_pwron_ret_rst				output	
Bit	6	External	dpll_mpu_pwron_rst				output	
Bit	7	External	dss_ret_rst_n				output	
Byte	0x3c	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	External	dss_rst_n				output	
Bit	1	External	cortex_m3_pwron_rst_n				output	
Bit	2	External	cortex_m3_ret_rst_n				output	
Bit	3	External	cortex_m3_rst1_n				output	
Bit	4	External	cortex_m3_rst2_n				output	
Bit	5	External	cortex_m3_rst3_n				output	
Bit	6	External	emif_ddr_phy_pwron_rst_n				output	
Bit	7	External	emu_early_pwron_rst_n				output	
Byte	0x3d	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	External	emu_pwron_rst_n				output	
Bit	1	External	emu_rst_n				output	
Bit	2	External	gfx_rst_n				output	
Bit	3	External	ivahd_pwron_rst_n				output	

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Table 18-41. PRM Observable Signals (continued)

Byte	0x00	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	4	External	ivahd_rst_n				output	
Bit	5	External	ivahd_seq1_rst_n				output	
Bit	6	External	ivahd_seq2_rst_n				output	
Bit	7	External	l3_init_pwron_rst_n				output	
Byte	0x3e	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	External	l3_init_ret_rst_n				output	
Bit	1	External	l3_init_rst_n				output	
Bit	2	External	l4_per_pwron_ret_rst_n				output	
Bit	3	External	l4_per_ret_rst_n				output	
Bit	4	External	l4_per_rst_n				output	
Bit	5	External	mpu_pwron_rst_n				output	
Bit	6	External	mpu_rst_n				output	
Bit	7	External	sdma_ret_rst_n				output	
Byte	0x3f	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	External	std_efuse_pwron_rst_n				output	
Bit	1	External	dspss_dsp_rst_n				output	
Bit	2	External	dspss_pwron_rst_n				output	
Bit	3	External	dspss_ret_rst_n				output	
Bit	4	External	dspss_sys_rst_n				output	
Bit	5	External	wkup_pwron_rst_n				output	
Bit	6	External	wkup_rst_n				output	
Bit	7	External	wkup_sys_pwron_rst_n				output	
Byte	0x40	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	External	cortex_m3_rstdone				input	
Bit	1	External	mpu_pwron_rstdone				input	
Bit	2	External	dspss_rstdone				input	
Bit	3:4		Reserved					
Bit	5	Internal	memlog_mpu_l2_destroyed_I0.logStatus				output	

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Table 18-41. PRM Observable Signals (continued)

Byte	0x00	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	6	Internal	memlog_mpu_l2_notaccessible_I0.logStatus				output	
Bit	7	Internal	memlog_mpu_ram_destroyed_I0.logStatus				output	
Byte	0x41	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	memlog_mpu_ram_notaccessible_I0.logStatus				output	
Bit	1	Internal	rstactst_audio_rstactst_I0.logStatus				output	
Bit	2	Internal	rstactst_cam_rstactst_I0.logStatus				output	
Bit	3	Internal	rstactst_core_rstactst_I0.logStatus				output	
Bit	4		Reserved					
Bit	5	Internal	rstactst_dss_rstactst_I0.logStatus				output	
Bit	6	Internal	rstactst_emu_rstactst_I0.logStatus				output	
Bit	7	Internal	rstactst_gfx_rstactst_I0.logStatus				output	
Byte	0x42	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	rstactst_ivahd_rstactst_I0.logStatus				output	
Bit	1	Internal	rstactst_l3_init_rstactst_I0.logStatus				output	
Bit	2	Internal	rstactst_l4_per_rstactst_I0.logStatus				output	
Bit	3	Internal	rstactst_mpu_rstactst_I0.logStatus				output	
Bit	4	Internal	rstactst_dspss_rstactst_I0.logStatus				output	
Bit	5	Internal	rstactst_globalwarm_rstactst_I0.logStatus				output	
Bit	7:6		Reserved					
Byte	0x43	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	rstactst_globalcold_rstactst_I0.logStatus				output	
Bit	1	Internal	glblrstmngr_I0.warmrst_fsm_state	0	LSB		output	WAITWARMIN = "101", WAITCLOCKSTABLE = "110", FREQUPDATE = "111"
Bit	2	Internal	glblrstmngr_I0.warmrst_fsm_state	1			output	WAITEMIFIDLE = "011", WAITNOPENDINGRST = "100",
Bit	3	Internal	glblrstmngr_I0.warmrst_fsm_state	2			output	RESET = "000", INIT = "001", WAIT16CLK = "010",
Bit	4	Internal	glblrstmngr_I0.warmrst_fsm_state	3	MSB		output	RESET = "000", INIT = "001", WAIT16CLK = "010",
Bit	5	External	debug_logic_debugss_stby_mstandby				input	
Bit	6	External	forceactive_cortex_m3_cpu1				input	
Bit	7	External	forceactive_cortex_m3_cpu2				input	

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Table 18-41. PRM Observable Signals (continued)

Byte	0x00	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Byte	0x44	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	External	forceactive_ivahd_seq1				input	
Bit	1	External	forceactive_ivahd_seq2				input	
Bit	2	External	forceactive_mpu				input	
Bit	3	External	forceactive_dspss				input	
Bit	4	External	inhibitsleep_cortex_m3_cpu1				input	
Bit	5	External	inhibitsleep_cortex_m3_cpu2				input	
Bit	6	External	inhibitsleep_ivahd_seq1				input	
Bit	7	External	inhibitsleep_ivahd_seq2				input	
Byte	0x45	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	External	inhibitsleep_mpu				input	
Bit	1	External	inhibitsleep_dspss				input	
Bit	2	External	waitinreset_cortex_m3_cpu1				input	
Bit	3	External	waitinreset_cortex_m3_cpu2				input	
Bit	4	External	waitinreset_ivahd_seq1				input	
Bit	5	External	waitinreset_ivahd_seq2				input	
Bit	6	External	waitinreset_mpu				input	
Bit	7	External	waitinreset_dspss				input	
Byte	0x46	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	emupst_core_I0.powerState				output	
Bit	1	Internal	emupst_ivahd_I0.powerState				output	
Bit	2	Internal	emupst_mpu_I0.powerState				output	
Bit	3	Internal	emupst_dspss_I0.powerState				output	
Bit	7:4		Reserved					
Byte	0x47	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	emupwr_core_I0.ackfsm_state	0	LSB		output	FORCEACKSTATE = "11", BOTHACK = "10"
Bit	1	Internal	emupwr_core_I0.ackfsm_state	1	MSB		output	ACKOFF = "01", INHIBACK = "00",

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Table 18-41. PRM Observable Signals (continued)

Byte	0x00	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	2	Internal	emupwr_core_I0.fsm_state	0	LSB		output	OFF2EMUONRST = "01111", RETL2EMUONRST = "10000", RETH2EMUONRST = "10001", EMUON2ONINACT = "10010"
Bit	3	Internal	emupwr_core_I0.fsm_state	1			output	OFF2EMUONNOISO = "01100", RETL2EMUONNOISO = "01101", RETH2EMUONNOISO = "01110",
Bit	4	Internal	emupwr_core_I0.fsm_state	2			output	RETH2EMUONISO = "01000", EMUON2OFF = "01001", EMUON2RETL = "01010", EMUON2RETH = "01011",
Bit	5	Internal	emupwr_core_I0.fsm_state	3			output	RETL2EMUON = "00100", RETH2EMUON = "00101", OFF2EMUONISO = "00110", RETL2EMUONISO = "00111",
Bit	6	Internal	emupwr_core_I0.fsm_state	4	MSB		output	NORMAL = "00000", SLEEPDESIREDSTATE = "00001", FORCEON = "00010", OFF2EMUON = "00011",
Bit	7		Reserved					
Byte	0x48	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	emupwr_ivahd_I0.ackfsm_state	0	LSB		output	FORCEACKSTATE = "11", BOTHACK = "10"
Bit	1	Internal	emupwr_ivahd_I0.ackfsm_state	1	MSB		output	ACKOFF = "01", INHIBACK = "00",
Bit	2	Internal	emupwr_ivahd_I0.fsm_state	0	LSB		output	OFF2EMUONRST = "01111", RETL2EMUONRST = "10000", RETH2EMUONRST = "10001", EMUON2ONINACT = "10010"
Bit	3	Internal	emupwr_ivahd_I0.fsm_state	1			output	OFF2EMUONNOISO = "01100", RETL2EMUONNOISO = "01101", RETH2EMUONNOISO = "01110",
Bit	4	Internal	emupwr_ivahd_I0.fsm_state	2			output	RETH2EMUONISO = "01000", EMUON2OFF = "01001", EMUON2RETL = "01010", EMUON2RETH = "01011",
Bit	5	Internal	emupwr_ivahd_I0.fsm_state	3			output	RETL2EMUON = "00100", RETH2EMUON = "00101", OFF2EMUONISO = "00110", RETL2EMUONISO = "00111",
Bit	6	Internal	emupwr_ivahd_I0.fsm_state	4	MSB		output	NORMAL = "00000", SLEEPDESIREDSTATE = "00001", FORCEON = "00010", OFF2EMUON = "00011",
Bit	7		Reserved					
Byte	0x49	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	emupwr_mpu_I0.ackfsm_state	0	LSB		output	FORCEACKSTATE = "11", BOTHACK = "10"
Bit	1	Internal	emupwr_mpu_I0.ackfsm_state	1	MSB		output	ACKOFF = "01", INHIBACK = "00",
Bit	2	Internal	emupwr_mpu_I0.fsm_state	0	LSB		output	OFF2EMUONRST = "01111", RETL2EMUONRST = "10000", RETH2EMUONRST = "10001", EMUON2ONINACT = "10010"
Bit	3	Internal	emupwr_mpu_I0.fsm_state	1			output	OFF2EMUONNOISO = "01100", RETL2EMUONNOISO = "01101", RETH2EMUONNOISO = "01110",
Bit	4	Internal	emupwr_mpu_I0.fsm_state	2			output	RETH2EMUONISO = "01000", EMUON2OFF = "01001", EMUON2RETL = "01010", EMUON2RETH = "01011",

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Table 18-41. PRM Observable Signals (continued)

Byte	0x00	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	5	Internal	emupwr_mpu_I0.fsm_state	3			output	RETL2EMUON = "00100", RETH2EMUON = "00101", OFF2EMUONISO = "00110", RETL2EMUONISO = "00111",
Bit	6	Internal	emupwr_mpu_I0.fsm_state	4	MSB		output	NORMAL = "00000", SLEEPDESIREDSTATE = "00001", FORCEON = "00010", OFF2EMUON = "00011",
Bit	7		Reserved					
Byte	0x4a	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	emupwr_dspss_I0.ackfsm_state	0	LSB		output	FORCEACKSTATE = "11", BOTHACK = "10"
Bit	1	Internal	emupwr_dspss_I0.ackfsm_state	1	MSB		output	ACKOFF = "01", INHIBACK = "00",
Bit	2	Internal	emupwr_dspss_I0.fsm_state	0	LSB		output	OFF2EMUONRST = "01111", RETL2EMUONRST = "10000", RETH2EMUONRST = "10001", EMUON2ONINACT = "10010"
Bit	3	Internal	emupwr_dspss_I0.fsm_state	1			output	OFF2EMUONNOISO = "01100", RETL2EMUONNOISO = "01101", RETH2EMUONNOISO = "01110",
Bit	4	Internal	emupwr_dspss_I0.fsm_state	2			output	RETH2EMUONISO = "01000", EMUON2OFF = "01001", EMUON2RETL = "01010", EMUON2RETH = "01011",
Bit	5	Internal	emupwr_dspss_I0.fsm_state	3			output	RETL2EMUON = "00100", RETH2EMUON = "00101", OFF2EMUONISO = "00110", RETL2EMUONISO = "00111",
Bit	6	Internal	emupwr_dspss_I0.fsm_state	4	MSB		output	NORMAL = "00000", SLEEPDESIREDSTATE = "00001", FORCEON = "00010", OFF2EMUON = "00011",
Bit	7		Reserved					
Byte	0x4b	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	prcm_emu_ctrl_cm1_sysclk_I0.ackfsm_state	0	LSB		output	FORCEACKSTATE = "11", BOTHACK = "10"
Bit	1	Internal	prcm_emu_ctrl_cm1_sysclk_I0.ackfsm_state	1	MSB		output	ACKOFF = "01", INHIBACK = "00",
Bit	2	Internal	prcm_emu_ctrl_cm1_sysclk_I0.fsm_state	0	LSB		output	FORCEON = "010"
Bit	3	Internal	prcm_emu_ctrl_cm1_sysclk_I0.fsm_state	1			output	SLEEPDESIREDSTATE = "111",SLEEP2NORMAL = "101",
Bit	4	Internal	prcm_emu_ctrl_cm1_sysclk_I0.fsm_state	2	MSB		output	NORMAL = "000",TOSLEEPD = "001",
Bit	7:5		Reserved					
Byte	0x4c	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	prcm_emu_ctrl_per_dpll_alwon_clk_I0.ackfsm_state	0	LSB		output	FORCEACKSTATE = "11", BOTHACK = "10"
Bit	1	Internal	prcm_emu_ctrl_per_dpll_alwon_clk_I0.ackfsm_state	1	MSB		output	ACKOFF = "01", INHIBACK = "00",
Bit	2	Internal	prcm_emu_ctrl_per_dpll_alwon_clk_I0.fsm_state	0	LSB		output	FORCEON = "010"
Bit	3	Internal	prcm_emu_ctrl_per_dpll_alwon_clk_I0.fsm_state	1			output	SLEEPDESIREDSTATE = "111",SLEEP2NORMAL = "101",
Bit	4	Internal	prcm_emu_ctrl_per_dpll_alwon_clk_I0.fsm_state	2	MSB		output	NORMAL = "000",TOSLEEPD = "001",
Bit	7:5		Reserved					

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Table 18-41. PRM Observable Signals (continued)

Byte	0x00	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Byte	0x4d	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	emu_clkfsm_I0.dpll1_stop				input	
Bit	1	Internal	emu_clkfsm_I0.dpll2_stop				input	
Bit	2	Internal	emu_clkfsm_I0.stm_fsm_state	0	LSB		output	DPLL1 = "11", DPLL2 = "10"
Bit	3	Internal	emu_clkfsm_I0.stm_fsm_state	1	MSB		output	SLEEP = "00", SYS = "01",
Bit	4	Internal	emu_clkfsm_I0.trace_fsm_state	0	LSB		output	DPLL1 = "11", DPLL2 = "10"
Bit	5	Internal	emu_clkfsm_I0.trace_fsm_state	1	MSB		output	SLEEP = "00", SYS = "01",
Bit	6	Internal	emu_clkfsm_I0.dbg_fsm_state	0	LSB		output	DPLL1 = "11", DPLL2 = "10"
Bit	7	Internal	emu_clkfsm_I0.dbg_fsm_state	1	MSB		output	SLEEP = "00", SYS = "01",
Byte	0x4e	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	emu_clkfsm_I0.fsm_state	0	LSB		output	CLKST = "110"
Bit	1	Internal	emu_clkfsm_I0.fsm_state	1			output	CLKCG = "011", CLKCR = "010",
Bit	2	Internal	emu_clkfsm_I0.fsm_state	2	MSB		output	SLEEP = "000", MUX = "001",
Bit	3	External	globalwkupen				output	
Bit	4	External	ioswakeup				input	
Bit	5	External	modem_sleep				input	
Bit	6	Internal	sysclkreq_custom.emu_clkreq				output	
Bit	7	Internal	prcm_dev_sysclk_gcg_I0.clk_activity_ctrl				output	
Byte	0x4f	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	devfsm_I0.sys_clk_on				output	
Bit	1	Internal	sysclkreq_custom.allsysclkisgated				input	
Bit	2	Internal	devfsm_I0.power_req				output	
Bit	3	Internal	devfsm_I0.power_req_ack				input	
Bit	4	Internal	devfsm_I0.wkupldo_volt_ok				output	
Bit	5	Internal	bgap_stabilization_custom.bgap_is_on				output	
Bit	7:6		Reserved					
Byte	0x50	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	devfsm_I0.osc_clk_out			clock	input	

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Table 18-41. PRM Observable Signals (continued)

Byte	0x00	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	1	Internal	devfsm_I0.clk			clock	input	
Bit	2	Internal	devfsm_I0.device_is_on				output	
Bit	3	Internal	prcm_dev_merger_I0.pmDomainIsIdle				output	devfsm_I0.device_is_lp
Bit	7:4		Reserved					
Byte	0x51	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	ldo_custom_I0.wkupldosleep				output	
Bit	1	Internal	ldo_custom_I0.wkupldoemuon				output	
Bit	2	Internal	ldo_custom_I0.bgap_aipoff				output	
Bit	3	Internal	ldo_custom_I0.vsldo_wkup_dftrtaon				output	
Bit	4	Internal	ldo_custom_I0.vsldo_wkup_dftrtagood				output	
Bit	5	Internal	vfsm_custom_I0.device_in_off_mode				output	
Bit	6	Internal	vsldo_mpu_custom.global_aipoff				input	
Bit	7		Reserved					
Byte	0x52	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	vfsm_core_I0.volt_domain_is_on				output	
Bit	1	Internal	vfsm_core_I0.volt_domain_is_good				output	
Bit	2	Internal	vfsm_core_I0.volt_domain_is_lp				output	
Bit	3	Internal	vfsm_core_I0.volt_domain_is_sleep				output	
Bit	4	Internal	vfsm_core_I0.volt_domain_is_ret				output	
Bit	5	Internal	vfsm_core_I0.go_off_mode				output	
Bit	6	Internal	vfsm_core_I0.err_rstn				output	
Bit	7	Internal	vfsm_core_I0.volt_off_rst_n				output	
Byte	0x53	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	vfsm_iva_I0.volt_domain_is_on				output	
Bit	1	Internal	vfsm_iva_I0.volt_domain_is_good				output	
Bit	2	Internal	vfsm_iva_I0.volt_domain_is_lp				output	
Bit	3	Internal	vfsm_iva_I0.volt_domain_is_sleep				output	
Bit	4	Internal	vfsm_iva_I0.volt_domain_is_ret				output	

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Table 18-41. PRM Observable Signals (continued)

Byte	0x00	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	5	Internal	vfsm_iva_I0.go_off_mode				output	
Bit	6	Internal	vfsm_iva_I0.err_rstn				output	
Bit	7	Internal	vfsm_iva_I0.volt_off_rst_n				output	
Byte	0x54	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	vfsm_mpu_I0.volt_domain_is_on				output	
Bit	1	Internal	vfsm_mpu_I0.volt_domain_is_good				output	
Bit	2	Internal	vfsm_mpu_I0.volt_domain_is_lp				output	
Bit	3	Internal	vfsm_mpu_I0.volt_domain_is_sleep				output	
Bit	4	Internal	vfsm_mpu_I0.volt_domain_is_ret				output	
Bit	5	Internal	vfsm_mpu_I0.go_off_mode				output	
Bit	6	Internal	vfsm_mpu_I0.err_rstn				output	
Bit	7	Internal	vfsm_mpu_I0.volt_off_rst_n				output	
Byte	0x55	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	vsldo_core_I0.AIPOFF				output	
Bit	1	Internal	vsldo_core_I0.ABBOFF				output	
Bit	2	Internal	vsldo_core_I0.SRAMALLRET				output	
Bit	4:3		Reserved					
Bit	5	Internal	vsldo_core_I0.sram_vok				output	
Bit	7:6		Reserved					
Byte	0x56	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	vsldo_iva_I0.AIPOFF				output	
Bit	1	Internal	vsldo_iva_I0.ABBOFF				output	
Bit	2	Internal	vsldo_iva_I0.SRAMALLRET				output	
Bit	4:3		Reserved					
Bit	5	Internal	vsldo_iva_I0.sram_vok				output	
Bit	7:6		Reserved					
Byte	0x57	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	vsldo_mpu_I0.AIPOFF				output	
Bit	1	Internal	vsldo_mpu_I0.ABBOFF				output	

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Table 18-41. PRM Observable Signals (continued)

Byte	0x00	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	2	Internal	vsldo_mpu_I0.SRAMALLRET				output	
Bit	4:3		Reserved					
Bit	5	Internal	vsldo_mpu_I0.sram_vok				output	
Bit	7:6		Reserved					
Byte	0x58	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	vbbldo_iva_I0.AIPOFF				output	
Bit	1	Internal	vbbldo_iva_I0.VBYPASSZ				output	
Bit	2	Internal	vbbldo_iva_I0.BBSEL				output	
Bit	3	Internal	vbbldo_iva_I0.sleep_and_vddc_settled				input	
Bit	4	Internal	vbbldo_mpu_I0.AIPOFF				output	
Bit	5	Internal	vbbldo_mpu_I0.VBYPASSZ				output	
Bit	6	Internal	vbbldo_mpu_I0.BBSEL				output	
Bit	7	Internal	vbbldo_mpu_I0.sleep_and_vddc_settled				input	
Byte	0x59	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	temporary_device_I1.ls_vddcore_en				output	
Bit	1	Internal	temporary_device_I1.ls_vddcore_off				output	
Bit	2	Internal	temporary_device_I1.ls_vddiva_en				output	
Bit	3	Internal	temporary_device_I1.ls_vddiva_off				output	
Bit	4	Internal	temporary_device_I1.ls_vddmpu_en				output	
Bit	5	Internal	temporary_device_I1.ls_vddmpu_off				output	
Bit	6	Internal	temporary_device_I1.ls_vddcore_wkup_en				output	
Bit	7	Internal	temporary_device_I1.ls_vddcore_emu_en				output	
Byte	0x5a	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	temporary_device_I1.ls_vddmodem_off				output	
Bit	7:1		Reserved					
Byte	0x5b	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	iocntl_I0.io_off_mode				output	
Bit	1	Internal	iocntl_I0.io_isoovr				output	
Bit	2	Internal	iocntl_I0.io_isobypass				output	

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Table 18-41. PRM Observable Signals (continued)

Byte	0x00	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	3	Internal	iocntl_I0.io_iso_clk				output	
Bit	4	Internal	iocntl_I0.io_iso_clk_ack				input	
Bit	5	Internal	iocntl_I0.io_iso				output	
Bit	6	Internal	iocntl_I0.io_iso_ack				input	
Bit	7	Internal	iocntl_I0.io_wuclk				output	
Byte	0x5c	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	iocntl_I0.io_wuclk_ack				input	
Bit	1	Internal	iocntl_I0.io_nready				output	
Bit	2	Internal	iocntl_I0.io_iso_active				output	
Bit	3	Internal	iocntl_I0.fsm_state	0	LSB		output	EMIF2ON_INIT2 = "11110", EMIF2ON_INIT3 = "11100", EMIF2ON_INIT4 = "11000"
Bit	4	Internal	iocntl_I0.fsm_state	1			output	ISOEMIF_INIT6 = "01010", ISOEMIF = "11010", ISOEMIF_EXTEND = "01111", EMIF2ON_INIT1 = "01110",
Bit	5	Internal	iocntl_I0.fsm_state	2			output	ISOEMIF_INIT2 = "01100", ISOEMIF_INIT3 = "01000", ISOEMIF_INIT4 = "01001", ISOEMIF_INIT5 = "01011",
Bit	6	Internal	iocntl_I0.fsm_state	3			output	ISOALL_INIT3 = "00110", ISOALL_INIT4 = "00111", ISOALL_ACTIVE = "00101", ISOEMIF_INIT1 = "00100",
Bit	7	Internal	iocntl_I0.fsm_state	4	MSB		output	INIT = "00000", ONSTATE = "00001", ISOALL_INIT1 = "00011", ISOALL_INIT2 = "00010",
Byte	0x5d	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	device_sarfsm_I0.sar_restore_start				output	
Bit	1	Internal	device_sarfsm_I0.sar_restore_io				output	
Bit	2	Internal	device_sarfsm_I0.sar_restore_ioemif				output	
Bit	3	Internal	device_sarfsm_I0.fsm_state	0	LSB		output	SAR2B_RESTORE = "11010", SAR2B_RESET = "01111", SAR2B_IO = "01110"
Bit	4	Internal	device_sarfsm_I0.fsm_state	1			output	SAR2A_RESTORE = "01001", SAR2A_RESET = "01011", SAR2B_START = "01010",
Bit	5	Internal	device_sarfsm_I0.fsm_state	2			output	SAR1_IO = "00101", SAR1_RESET = "00100", SAR1_END = "01100", SAR2A_START = "01000",
Bit	6	Internal	device_sarfsm_I0.fsm_state	3			output	SAR1_BLOCKRST = "00010", SAR1_START = "00110", SAR1_RESTORE = "00111",
Bit	7	Internal	device_sarfsm_I0.fsm_state	4	MSB		output	SAR_IDLE = "00000", INITOFF_MODE = "00001", OFF_MODE = "00011",
Byte	0x5e	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	vproc_core_I0.srfreqerror	0			input	

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Table 18-41. PRM Observable Signals (continued)

Byte	0x00	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	1	Internal	vproc_core_I0.srfreqerror	1			input	
Bit	2	Internal	vproc_core_I0.srfreqerror	2			input	
Bit	3	Internal	vproc_core_I0.srfreqerror	3			input	
Bit	4	Internal	vproc_core_I0.srfreqerror	4			input	
Bit	5	Internal	vproc_core_I0.srfreqerror	5			input	
Bit	6	Internal	vproc_core_I0.srfreqerror	6			input	
Bit	7	Internal	vproc_core_I0.srfreqerror	7			input	
Byte	0x5f	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	vproc_core_I0.srupdateclk				input	
Bit	1	Internal	vproc_core_I0.srinterruptz				input	
Bit	2	Internal	vproc_core_I0.vpirqclr				output	
Bit	7:3		Reserved					
Byte	0x60	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	vproc_iva_I0.srfreqerror	0			input	
Bit	1	Internal	vproc_iva_I0.srfreqerror	1			input	
Bit	2	Internal	vproc_iva_I0.srfreqerror	2			input	
Bit	3	Internal	vproc_iva_I0.srfreqerror	3			input	
Bit	4	Internal	vproc_iva_I0.srfreqerror	4			input	
Bit	5	Internal	vproc_iva_I0.srfreqerror	5			input	
Bit	6	Internal	vproc_iva_I0.srfreqerror	6			input	
Bit	7	Internal	vproc_iva_I0.srfreqerror	7			input	
Byte	0x61	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	vproc_iva_I0.srupdateclk				input	
Bit	1	Internal	vproc_iva_I0.srinterruptz				input	
Bit	2	Internal	vproc_iva_I0.vpirqclr				output	
Bit	7:3		Reserved					
Byte	0x62	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	vproc_mpu_I0.srfreqerror	0			input	

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Table 18-41. PRM Observable Signals (continued)

Byte	0x00	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	1	Internal	vproc_mpu_I0.srfreqerror	1			input	
Bit	2	Internal	vproc_mpu_I0.srfreqerror	2			input	
Bit	3	Internal	vproc_mpu_I0.srfreqerror	3			input	
Bit	4	Internal	vproc_mpu_I0.srfreqerror	4			input	
Bit	5	Internal	vproc_mpu_I0.srfreqerror	5			input	
Bit	6	Internal	vproc_mpu_I0.srfreqerror	6			input	
Bit	7	Internal	vproc_mpu_I0.srfreqerror	7			input	
Byte	0x63	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	vproc_mpu_I0.srupdateclk				input	
Bit	1	Internal	vproc_mpu_I0.srinterruptz				input	
Bit	2	Internal	vproc_mpu_I0.vpirqclr				output	
Bit	7:3		Reserved					
Byte	0x64	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	temporary_scrm_I0.scrm_2_prm_o	32			output	alt_sysclk
Bit	1	Internal	temporary_scrm_I0.scrm_2_prm_o	33			output	ape_clk32k
Bit	2	Internal	temporary_scrm_I0.scrm_2_prm_o	34			output	ape_sysclk
Bit	3	Internal	temporary_scrm_I0.scrm_2_prm_o	35			output	mdm_clk32k
Bit	4	Internal	temporary_scrm_I0.scrm_2_prm_o	36			output	mdm_sysclk
Bit	5	Internal	temporary_scrm_I0.scrm_2_prm_o	37			output	d2d_clk32k
Bit	6	Internal	temporary_scrm_I0.scrm_2_prm_o	38			output	d2d_sysClk
Bit	7	Internal	temporary_scrm_I0.scrm_2_prm_o	39			output	ape_clkreq
Byte	0x65	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	temporary_scrm_I0.scrm_2_prm_o	40			output	mdm_clkreq
Bit	1	Internal	temporary_scrm_I0.scrm_2_prm_o	41			output	d2d_clkreq
Bit	2	Internal	temporary_scrm_I0.scrm_2_prm_o	42			output	src_bypass
Bit	3	Internal	temporary_scrm_I0.scrm_2_prm_o	43			output	src_pwrdn
Bit	4	Internal	temporary_scrm_I0.scrm_2_prm_o	44			output	src_sysclk_good
Bit	5	Internal	temporary_scrm_I0.scrm_2_prm_o	45			output	slicer_bypass

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Table 18-41. PRM Observable Signals (continued)

Byte	0x00	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	6	Internal	temporary_scrm_I0.scrm_2_prm_o	46			output	slicer_pwrdn
Bit	7	Internal	temporary_scrm_I0.scrm_2_prm_o	47			output	scrm_dft_cnt_bypass
Byte	0x66	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	temporary_scrm_I0.scrm_2_prm_o	48			output	aux_clk_muxout(4)
Bit	1	Internal	temporary_scrm_I0.scrm_2_prm_o	49			output	alt_sysclk
Bit	2	Internal	temporary_scrm_I0.scrm_2_prm_o	50			output	sysclk
Bit	3	Internal	temporary_scrm_I0.scrm_2_prm_o	51			output	state of pwr_req_sm state-machine
Bit	4	Internal	temporary_scrm_I0.scrm_2_prm_o	52			output	state of pwr_req_sm state-machine
Bit	5	Internal	temporary_scrm_I0.scrm_2_prm_o	53			output	state of pwr_req_sm state-machine
Bit	6	Internal	temporary_scrm_I0.scrm_2_prm_o	54			output	mdm_pwr_req_ack
Bit	7	Internal	temporary_scrm_I0.scrm_2_prm_o	55			output	mdm_pwr_req
Byte	0x67	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	temporary_scrm_I0.scrm_2_prm_o	56			output	ape_pwr_req_ack
Bit	1	Internal	temporary_scrm_I0.scrm_2_prm_o	57			output	ape_pwr_req
Bit	2	Internal	temporary_scrm_I0.scrm_2_prm_o	58			output	clk_is_gated_d2d_sysclk
Bit	3	Internal	temporary_scrm_I0.scrm_2_prm_o	59			output	clk_is_gated_mdm_sysclk
Bit	4	Internal	temporary_scrm_I0.scrm_2_prm_o	60			output	clk_is_gated_ape_sysclk
Bit	5	Internal	temporary_scrm_I0.scrm_2_prm_o	61			output	clk_is_running_sysclk
Bit	6	Internal	temporary_scrm_I0.scrm_2_prm_o	62			output	ape_allsysclkgated
Bit	7	Internal	temporary_scrm_I0.scrm_2_prm_o	63			output	sysclk_clkok
Byte	0x68	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	temporary_scrm_I0.scrm_2_prm_o	64			output	warmrst_out_na
Bit	1	Internal	temporary_scrm_I0.scrm_2_prm_o	65			output	ape_por_na
Bit	2	Internal	temporary_scrm_I0.scrm_2_prm_o	66			output	ape_warmrst_out_na
Bit	3	Internal	temporary_scrm_I0.scrm_2_prm_o	67			output	mdm_por_na
Bit	4	Internal	temporary_scrm_I0.scrm_2_prm_o	68			output	mdm_warmrst_out_na
Bit	5	Internal	temporary_scrm_I0.scrm_2_prm_o	69			output	d2d_por_na

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Table 18-41. PRM Observable Signals (continued)

Byte	0x00	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	6	Internal	temporary_scrm_l0.scrm_2_prm_o	70			output	d2d_warmrst_out_na
Bit	7	Internal	temporary_scrm_l0.scrm_2_prm_o	71			output	por_out_na
Byte	0x69	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	temporary_scrm_l0.scrm_2_prm_o	72			output	warmrst_in_na
Bit	1	Internal	temporary_scrm_l0.scrm_2_prm_o	73			output	ape_warmrst_in_na
Bit	2	Internal	temporary_scrm_l0.scrm_2_prm_o	74			output	mdm_warmrst_in_na
Bit	3	Internal	temporary_scrm_l0.scrm_2_prm_o	75			output	d2d_warmrst_in_na
Bit	4	Internal	temporary_scrm_l0.scrm_2_prm_o	76			output	d2d_clk32k_is_not_running
Bit	5	Internal	temporary_scrm_l0.scrm_2_prm_o	77			output	mdm_clk32k_is_not_running
Bit	6	Internal	temporary_scrm_l0.scrm_2_prm_o	78			output	ape_clk32k_is_not_running
Bit	7	Internal	temporary_scrm_l0.scrm_2_prm_o	79			output	aux_sysclk_4_is_not_running
Byte	0x6a	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	temporary_scrm_l0.scrm_2_prm_o	80			output	i_d2d_unnaturalreset
Bit	1	Internal	temporary_scrm_l0.scrm_2_prm_o	81			output	i_d2d_inreset
Bit	2	Internal	temporary_scrm_l0.scrm_2_prm_o	82			output	i_d2d_latchresetbusack
Bit	3	Internal	temporary_scrm_l0.scrm_2_prm_o	83			output	d2d_latchresetbus
Bit	4	Internal	temporary_scrm_l0.scrm_2_prm_o	84			output	d2d_assertnreset
Bit	5	Internal	temporary_scrm_l0.scrm_2_prm_o	85			output	d2d_blockreset
Bit	6	Internal	temporary_scrm_l0.scrm_2_prm_o	86			output	d2d_releasefromwir
Bit	7	Internal	temporary_scrm_l0.scrm_2_prm_o	87			output	d2d_waitinreset
Byte	0x6b	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	temporary_scrm_l0.scrm_2_prm_o	88			output	d2d_warminrstsrc_fltrd
Bit	1	Internal	temporary_scrm_l0.scrm_2_prm_o	89			output	mdm_warminrstsrc_fltrd
Bit	2	Internal	temporary_scrm_l0.scrm_2_prm_o	90			output	ape_warminrstsrc_fltrd
Bit	3	Internal	temporary_scrm_l0.scrm_2_prm_o	91			output	ext_warminrstsrc_fltrd
Bit	4	Internal	temporary_scrm_l0.scrm_2_prm_o	92			output	d2d_warmrst_in_na_s
Bit	5	Internal	temporary_scrm_l0.scrm_2_prm_o	93			output	mdm_warmrst_in_na_s

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Table 18-41. PRM Observable Signals (continued)

Byte	0x00	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	6	Internal	temporary_scrm_I0.scrm_2_prm_o	94			output	ape_warmrst_in_na_s
Bit	7	Internal	temporary_scrm_I0.scrm_2_prm_o	95			output	ext_warmrst_in_na_s
Byte	0x6c	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	devfsm_I0.osc_clk_out			clock	input	SYS_CLK
Bit	1	Internal	devfsm_I0.clk			clock	input	32K_FCLK
Bit	2	Internal	gat_per_32k_gfclk_I0.clkGated			clock	output	PER_32K_FCLK
Bit	3	Internal	gat_wkup_32k_gfclk_I0.clkGated			clock	output	WKUP_32K_FCLK
Bit	4	Internal	gat_abe_alwon_32k_clk_I0.clkGated			clock	output	ABE_ALWON_32K_CLK
Bit	5	Internal	gat_per_sys_gfclk_I0.clkGated			clock	output	PER_SYS_GFCLK
Bit	6	Internal	gat_std_efuse_sys_clk_I0.clkGated			clock	output	STD_EFUSE_SYS_CLK
Bit	7	Internal	gat_core_dpll_alwon_clk_I0.clkGated			clock	output	CORE_DPLL_ALWON_CLK
Byte	0x6d	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	gat_per_dpll_alwon_clk_I0.clkGated			clock	output	PER_DPLL_ALWON_CLK
Bit	1		Reserved					
Bit	2	Internal	gat_mpu_dpll_alwon_clk_I0.clkGated			clock	output	MPU_DPLL_ALWON_CLK
Bit	3	Internal	mux_abe_dpll_refclk_mux_I0.clk_out			clock	output	ABE_DPLL_ALWON_CLK
Bit	4		Reserved					
Bit	5	Internal	gat_l4_wkup_profiling_gclk_I0.clkGated			clock	output	L4_WKUP_PROFILING_GCLK
Bit	6	Internal	gat_l4_wkup_gclk_I0.clkGated			clock	output	L4_WKUP_GCLK
Bit	7	Internal	gat_cm1_sys_clk_I0.clkGated			clock	output	CM1_SYS_CLK
Byte	0x6e	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	gat_l4_wkup_giclk_I0.clkGated			clock	output	L4_WKUP_GICLK
Bit	1	Internal	gat_sr_core_sysclk_I0.clkGated			clock	output	SR_CORE_SYSCLK
Bit	2	Internal	gat_sr_mpu_sysclk_I0.clkGated			clock	output	SR_MPU_SYSCLK
Bit	3	Internal	gat_sr_iva_sysclk_I0.clkGated			clock	output	SR_IVA_SYSCLK
Bit	4	Internal	ctsbuf_ff_prm_l4_wkup_iclk_p2p_i_I0.y			clock	output	L4_WKUP_ICLK
Bit	5		Reserved					
Bit	6	Internal	gat_dss_alwon_sys_clk_I0.clkGated			clock	output	DSS_ALWON_SYS_CLK
Bit	7	Internal	gat_abe_sysclk_I0.clkGated			clock	output	ABE_SYSCLK

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Table 18-41. PRM Observable Signals (continued)

Byte	0x00	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Byte	0x6f	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	gat_dspss_dpll_alwon_clk_I0.clkGated			clock	output	dspss_DPLL_ALWON_CLK
Bit	1	Internal	gat_emu_sys_clk_I0.clkGated			clock	output	EMU_SYS_CLK
Bit	2	Internal	gat_usb_dpll_clk_I0.clkGated			clock	output	USB_DPLL_CLK
Bit	3	Internal	gat_abe_dpll_bypass_clk_mux_pwadded0_I0.clkGated			clock	output	ABE_DPLL_BYPASS_CLK
Bit	4	Internal	mux_cm2_dm2_mux_I0.clk_out			clock	output	DMT2_GFCLK
Bit	5	Internal	mux_cm2_dm3_mux_I0.clk_out			clock	output	DMT3_GFCLK
Bit	6	Internal	mux_cm2_dm4_mux_I0.clk_out			clock	output	DMT4_GFCLK
Bit	7	Internal	mux_cm2_dm9_mux_I0.clk_out			clock	output	DMT9_GFCLK
Byte	0x70	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	mux_cm2_dm10_mux_I0.clk_out			clock	output	DMT10_GFCLK
Bit	1	Internal	mux_cm2_dm11_mux_I0.clk_out			clock	output	DMT11_GFCLK
Bit	2	Internal	mux_dmt1_clk_mux_I0.clk_out			clock	output	DMT1_GCLK
Bit	3		Reserved					
Bit	4	Internal	cirq_cortex_m3_I0.prm2Irq				output	
Bit	5		Reserved					
Bit	6	Internal	cirq_dspss_I0.prm2Irq				output	
Bit	7		Reserved					
Byte	0x71	Type	AutoPRCM signal identifier	B#	Info +	Info +	Info +	Comments
Bit	0	Internal	rstbdvcn_I0.eFuseAutoLoad_done_pulse				output	
Bit	1	Internal	rstbdvcn_I0.eFuseAutoLoad_done_one_pulse				output	
Bit	2	Internal	rstbdvcn_I0.eFuseAutoLoad_n_s				output	
Bit	3	Internal	rstbdvcn_I0.prmDeviceType	0	LSB		output	
Bit	4	Internal	rstbdvcn_I0.prmDeviceType	1			output	
Bit	5	Internal	rstbdvcn_I0.prmDeviceType	2	MSB		output	
Bit	7:6		Reserved					

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18.4.11.5.10 PRCM FSM State Observable Signals Description

Some of the observable signals encode the different PRCM finite state-machine (FSM) states. Each state corresponds to a combination of FSM output signal values. The states of the different FSMs associated with the SAR RAM, DPLLs, EMIF, I/O controller, power manager, global reset manager warm reset generator, and clock managers, along with their corresponding output signal values (except for DPLL Ctrl outputs) are described in Table 18-42 through Table 18-48.

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Table 18-42. SAR FSM State Description

	FSM State		Output Values									
device_sarfsm_I0.fsm_state	**Name**	**Value**	sar_deviceOffWkupActst	sar_restore_cndp	sar_restore_start	sar_override	sar_inhibit_frequpdate	sar_stall_reset	sar_sdma_mwakeup	sar_restore_ioemif	sar_restore_io	sar_sdma_rst_n
	SAR_IDLE	00000	0	0	0	0	0	0	0	1	1	1
	INITOFF_MODE	00001	0	Previous value	previous value	0	Previous value	Previous value	0	0	0	Previous value
	OFF_MODE	00011	0	restore_phase1_cndp	0	0	Previous value	1	0	0	0	0
	SAR1_BLOCKRST	00010	0	Previous value	0	1	Previous value	1	0	0	0	0
	SAR1_START	00110	1	Previous value	1	1	glblWarmRstActSt	1	1	0	0	1
	SAR1_RESTORE	00111	1	Previous value	1	1	Previous value	1	0	0	0	1
	SAR1_IO	00101	1	Previous value	1	1	Previous value	1	0	1	0	1
	SAR1_RESET	00100	0	Previous value	1	0	Previous value	1	0	1	0	0
	SAR1_END	01100	0	Previous value	1	0	0	1	0	1	0	0
	SAR2A_START	01000	0	restore_phase2a_cndp	1	0	Previous value	1	1	1	0	1
	SAR2A_RESTORE	01001	0	Previous value	1	0	Previous value	1	0	1	0	1
	SAR2A_RESET	01011	0	Previous value	1	0	Previous value	1	0	1	0	0
	SAR2B_START	01010	0	restore_phase2b_cndp	1	0	Previous value	1	1	1	0	1
	SAR2B_RESTORE	11010	0	Previous value	1	0	Previous value	1	0	1	0	1
	SAR2B_RESET	01111	0	Previous value	0	0	Previous value	1	0	1	0	0
	SAR2B_IO	01110	0	Previous value	0	0	Previous value	1	0	1	1	1

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Table 18-43. DPLLCtrl FSM State Description

	Name	Value		Mode
dpllsctrl_dpll. DPLLCtrlState		0x00	00000000	None
	MLPS0	0x11	00010001	LPS
	MLPS1	0x12	00010010	LPS
	MLPS2	0x13	00010011	LPS
	GoToLPS	0x14	00010100	LPS
	setIdle	0x15	00010101	LPS
	LPStopCmd	0x16	00010110	LPS
	LPStopState	0x1F	00011111	LPS
	MLPS0	0x91	10010001	LPS
	MLPS1	0x92	10010010	LPS
	MLPS2	0x93	10010011	LPS
	GoToLPS	0x94	10010100	LPS
	setIdle	0x95	10010101	LPS
	LPStopCmd	0x96	10010110	LPS
	LPStopState	0x9F	10011111	LPS
	MFRS0	0x21	00100001	FRS
	MFRS1	0x22	00100010	FRS
	MFRS2	0x23	00100011	FRS
	GoToFRS	0x24	00100100	FRS
	FRStopCmd	0x26	00100110	FRS
	FRStopState	0x2F	00101111	FRS
	MFRS0	0xA1	10100001	FRS
	MFRS1	0xA2	10100010	FRS
	MFRS2	0xA3	10100011	FRS
	GoToFRS	0xA4	10100100	FRS
	setIdle	0xA5	10100101	FRS
	FRStopCmd	0xA6	10100110	FRS
	FRStopState	0xAF	10101111	FRS
	waitM0	0x41	01000001	MNB
	GoToMNB	0x42	01000010	MNB
	MNBypassState	0x4F	01001111	MNB
	MLPB0	0x51	01010001	LPB
	MLPB1	0x52	01010010	LPB
	MLPB2	0x53	01010011	LPB

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Table 18-43. DPLLCtrl FSM State Description (continued)

	Name	Value		Mode
dpllsctrl_dpll. DPLLCtrlState	wait3clkinp	0x54	01010100	LPB
	GoToLPB	0x55	01010101	LPB
	LPBypassState	0x5F	01011111	LPB
	MLPB0	0xD1	11010001	LPB
	MLPB1	0xD2	11010010	LPB
	MLPB2	0xD3	11010011	LPB
	wait3clkinp	0xD4	11010100	LPB
	GoToLPB	0xD5	11010101	LPB
	LPBypassState	0xDF	11011111	LPB
	MFRB0	0x61	01100001	FRB
	MFRB1	0x62	01100010	FRB
	MFRB2	0x63	01100011	FRB
	wait3clkinp	0x64	01100100	FRB
	GoToFRB	0x65	01100101	FRB
	FRBypassState	0x6F	01101111	FRB
	MFRB0	0xE1	11100001	FRB
	MFRB1	0xE2	11100010	FRB
	MFRB2	0xE3	11100011	FRB
	wait3clkinp	0xE4	11100100	FRB
	GoToFRB	0xE5	11100101	FRB
	FRBypassState	0xEF	11101111	FRB
	PL3.5	0x71	01110001	Lock
	PL4	0x72	01110010	Lock
	GoToLock	0x73	01110011	Lock
	LockState	0x7F	01111111	Lock

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Table 18-44. EMIF FSM State Description

	FSM State		Output Values				
emiffsm_I0.state	Name	Value	forceIdleReq	copyShadow	dll_reset_enable	clear_frequpdate	freq_update_idle
	START	000	0	0	0	0	1
	REQIDLE	001	1	0	0	0	0
	UPLOADSHADOW1	010	1	1	ro_shadow_dll_reset	0	0
	UPLOADSHADOW2	011	1	1	ro_shadow_dll_reset	0	0
	SHADOWCOPIED	100	1	1	ro_shadow_dll_reset	0	0
	WAITDLLREADY	101	1	0	0	dllReady and warmrstdata_n	0
	CLEAR_EXITIDLE	110	0	0	0	0	0

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Table 18-45. I/O Controller FSM State Description

	FSM State		Output Values									
iocntl_I0.fsm_state	Name	Value	io_nready	io_iso_active	io_is_on	io_off_mode	io_iso_clk	io_iso	io_isoovr	io_isobypass	io_protect	wkup_chain_en
	INIT	00000	Previous value	0	0	Previous value	0	0	0	0	0	0
	ONSTATE	00001	0	0	1	0	0	0	0	0	0	0
	ISOALL_INIT1	00011	1	0	0	1	Previous value	Previous value	Pervious value	0	1	1
	ISOALL_INIT2	00010	1	0	0	Previous value	1	Previous value	Previous value	0	1	1
	ISOALL_INIT3	00110	1	0	0	Previous value	Previous value	1	Previous value	0	1	1
	ISOALL_INIT4	00111	1	0	0	Previous value	0	Previous value	Previous value	0	1	1
	ISOALL_ACTIVE	00101	1	1	0	Previous value	Previous value	Previous value	Previous value	0	0	1
	ISOEMIF_INIT1	00100	1	1	0	0	Previous value	Previous value	Previous value	0	0	1
	ISOEMIF_INIT2	01100	1	1	0	Previous value	Previous value	Previous value	1	0	0	1
	ISOEMIF_INIT3	01000	1	1	0	Previous value	1	Previous value	Previous value	0	0	1
	ISOEMIF_INIT4	01001	1	1	0	Previous value	Previous value	0	Previous value	0	0	1
	ISOEMIF_INIT5	01011	1	1	0	Previous value	Previous value	Previous value	Previous value	0	0	1
	ISOEMIF_INIT6	01010	1	1	0	Previous value	0	Previous value	Previous value	0	0	1
	ISOEMIF	11010	1	0	0	Previous value	Previous value	Previous value	Previous value	0	0	0
	ISOEMIF_EXTEND	01111	0	0	0	Previous value	Previous value	Previous value	Previous value	0	0	0
	EMIF2ON_INIT1	01110	Previous value	0	0	Previous value	Previous value	Previous value	Previous value	1	0	0
	EMIF2ON_INIT2	11110	Previous value	0	0	Previous value	1	Previous value	Previous value	1	0	0
	EMIF2ON_INIT3	11100	Previous value	0	0	Previous value	Previous value	Previous value	0	1	0	0
	EMIF2ON_INIT4	11000	Previous value	0	0	Previous value	0	Previous value	Previous value	1	0	0

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Table 18-46. PM FSM State Description

	FSM State		Output Values											
pmfsm.fsm_state	Name	Value	sleep	domain_isolation	PM_off_reset	PM_ret_reset	PM_reset	intransition	domain_is_on	domain_is_retention	domain_is_off	domain_is_inactive	powerrequest	power_ok
	RESET	00000	0	0	PMRST_VAL	PMRST_VAL	PMRST_VAL	1	0	0	0	0	1	1
	CHANGEMEM	00001	0	0	1	1	1	1	1	0	0	0	Previous value	Previous value
	ONSTATE	00010	0	0	1	1	1	0	1	0	0	0	1	Previous value
	STATEUPDATE	00011	0	0	1	1	1	1	1	0	0	0	Previous value	Previous value
	INACTIVE	00100	0	0	1	1	1	0	0	0	0	1	Previous value	Previous value
	ON2INACT	00101	0	0	1	1	1	1	0	0	0	0	Previous value	Previous value
	INACT2ON	00110	0	0	1	1	1	1	1	0	0	0	Previous value	Previous value
	ON2OFF	00111	1	0	1	1	1	1	0	0	0	0	0	Previous value
	ON2RETL	01000	1	0	1	1	1	1	0	0	0	0	0	Previous value
	ON2RETH	01001	0	0	1	1	1	1	0	0	0	0	0	Previous value
	OFFSTATE	01010	1	1	1	0	0	0	0	0	1	0	Previous value	0
	RETL	01011	1	1	1	1	0	0	0	1	1	0	Previous value	0
	RETH	01100	0	0	1	1	1	0	0	1	0	0	Previous value	Previous value
	OFF2ON	01101	0	1	0	0	0	1	0	0	0	0	Previous value	0
	RETL2ON	01110	0	1	1	1	0	1	0	0	0	0	Previous value	0
	RETH2ON	01111	0	0	1	1	1	1	0	0	0	0	Previous value	Previous value
	OFF2ONISO	10000	0	1	0	0	0	1	0	0	0	0	Previous value	1
	RETL2ONISO	10001	0	1	1	1	0	1	0	0	0	0	Previous value	1
	RETH2ONISO	10010	0	0	1	1	1	1	0	0	0	0	Previous value	1

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Table 18-46. PM FSM State Description (continued)

	FSM State		Output Values											
pmfsm.fsm_state	OFF2ONNOISO	10011	0	0	0	0	0	1	0	0	0	0	Previous value	Previous value
	RETL2ONNOISO	10100	0	0	1	1	0	1	0	0	0	0	Previous value	Previous value
	RETH2ONNOISO	10101	0	0	1	1	1	1	0	0	0	0	Previous value	Previous value
	OFF2ONRST	10110	0	0	0	0	0	1	0	0	0	0	Previous value	Previous value
	RETL2ONRST	10111	0	0	1	1	0	1	0	0	0	0	Previous value	Previous value
	RETH2ONRST	11000	0	0	1	1	1	1	0	0	0	0	Previous value	Previous value
	INACTIVE2ON	11001	0	0	1	1	1	1	0	0	0	0	Previous value	Previous value
	INACTIVE2ONISO	11010	0	0	1	1	1	1	0	0	0	0	Previous value	1
	INACTIVE2ONNOISO	11011	0	0	1	1	1	1	0	0	0	0	Previous value	Previous value
	INACTIVE2ONRST	11100	0	0	1	1	1	1	0	0	0	0	Previous value	Previous value
	UPDATE2OFF	11101	1	Previous value	1	1	Previous value	1	0	0	0	0	0	Previous value
	UPDATE2RETL	11110	1	0	1	1	1	1	0	0	0	0	0	Previous value
	UPDATE2RETH	11111	0	0	1	1	1	1	0	0	0	0	0	Previous value

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Table 18-47. Warm Reset FSM State Description

	FSM State		Output Values					
glblrstmngr_l0.warmrst_fsm_state	Name	Value	glblWarmRst_n	Reserved	glblWarmRstNoWarmIn_n	glblWarmRstActSrc_n	emifForceIdleReq	warmRstBlockAck
	RESET	000	0		1	1	0	0
	INIT	001	1		1	1	0	0
	WAIT16CLK	010	1		1	0	1	0
	WAITEMIFIDLE	011	1		1	0	1	0
	WAITNOPENDINGRST	100	warm_in_s_n and not pending_warm_rst_log		not pending_warm_rst_log	0	1	0
	WAITWARMIN	101	warm_in_s_n and not pending_warm_rst_log		1	0	1	0
	WAITCLOCKSTABLE	110	1		1	1	1	0
	FREQUPDATE	111	1		1	1	0	1

Table 18-48. CM FSM State Description

	FSM State		Output Values			
cmfsm.fsm_state	Name	Value	domain_idle_req	domain_nReady	domain_is_idle	domain_is_noton_ack
	INACTIVE	000	1	1	1	1
	INACT2ACT	001	0	1	0	0
	ACTIVE	011	0	0	0	0
	ACT2INACT1	111	1	1	0	0
	ACT2INACT2	101	1	1	1	0

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18.4.11.5.11 DPLL Clockview Channel Observable Signals Multiplexing

Table 18-49 describes the multiplexing of the different DPLL clock outputs for each of the three available clk_view_0, clk_view_1, and clk_view_2 channels.

Table 18-49. Different DPLL Observable Clock Output Signals

SYSCTRL_GENERAL_CORE Observability Inputs Tied to Signals Inside Different Module DPLLs	Different DPLL Observable Signals Mapped to SYSCTRL_GENERAL_CORE Observability Inputs	Signal Description	DPLL CLKOUT Selection Per clk_view channel i CONTROL_CONF_CLK_SELi [2:0] MULT Value (where i = 0…2]
hwobs_coredpll_clkout	DPLL_TESTCLKOUT	CORE DPLL	0x0
hwobs_abedpll_clkout	PODPLLTESTCLKOUT	ABE DPLL	0x1
hwobs_perdpll_clkout	DPLL_TESTCLKOUT	PERIPH DPLL	0x2
hwobs_dsi1dpll_clkout	PODPLLTESTCLKOUT	DSI1 DPLL	0x3
hwobs_dsi2dpll_clkout	DPLL_TESTCLKOUT	DSI2 DPLL	0x4
reserved	Reserved	–	0x5
hwobs_usbdpll_clkout	PODPLLTESTCLKOUT	USB DPLL	0x6
reserved	Rreserved	–	0x7

18.4.11.5.12 Other CORE DPLL Observable Signals

Table 18-50 describes the mapping of CORE DPLL observability signals (other than CLKOUT) to the SYSCTRL_GENERAL_CORE DPLL observing inputs. The selection of CORE DPLL as the source of the additional DPLL signals is done at the SYSCTRL_GENERAL_CORE level by setting bit field MULT = 0x0 inside each of the eight registers (CONTROL_CONF_DPLL_FREQLOCK_SEL through CONTROL_CONF_DPLL_IDLE_SEL).

Table 18-50. Other CORE DPLL Observability Signals

SYSCTRL_GENERAL_CORE Observability Inputs Tied to CORE DPLL Observable Signals	Other CORE DPLL Observable Signals Mapped to SYSCTRL_GENERAL_CORE Observability Inputs	Signal Description	Logical Value Meaning
hwobs_coredpll_freqlock	COREdpll_freqlock	CORE DPLL frequency lock check	–
hwobs_coredpll_tinitz	COREdpll_tinitz	Check CORE DPLL status, lock/relock time	–
hwobs_coredpll_phaselock	COREdpll_phaselock	CORE DPLL phase lock check	–
hwobs_coredpll_tenable	COREdpll_tenable	CORE DPLL core RegM/N load enable input	–
hwobs_coredpll_tenablediv	COREdpll_tenablediv	CORE DPLL core RegM2/N2 load enable input	–
hwobs_coredpll_bypassack	COREdpll_bypassack	CORE DPLL bypass status signal	–
hwobs_coredpll_idle	COREdpll_idle	CORE DPLL idle mode input	–

18.4.11.5.13 Other ABE DPLL Observable Signals

Table 18-51 describes the mapping of CORE DPLL observability signals (other than CLKOUT) to the SYSCTRL_GENERAL_CORE DPLL observing inputs. The selection of ABE DPLL as the source of the additional DPLL signals is done at the SYSCTRL_GENERAL_CORE level by setting bit field MULT = 0x1 inside each of the eight registers (CONTROL_CONF_DPLL_FREQLOCK_SEL through CONTROL_CONF_DPLL_IDLE_SEL).

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Table 18-51. Other ABE DPLL Observability Signals

SYSCTRL_GENERAL_CORE Observability Inputs Tied to ABE DPLL Observable Signals	Other ABE DPLL Observable Signals Mapped to SYSCTRL_GENERAL_CORE Observability Inputs	Signal Description	Logical Value Meaning
hwobs_abedpll_freqlock	dspdpll_freqlock	ABE DPLL frequency lock check	–
hwobs_abedpll_tinitz	dspdpll_tinitz	Check ABE DPLL status, lock/relock time.	–
hwobs_abedpll_phaselock	dspDpllPhaseLock	dspDPLL phase lock check	–
hwobs_abedpll_tenable	dspDpllPhaseLock	dspDPLL phase lock check	–
hwobs_abedpll_tenablediv	dspDpllPhaseLock	dspDPLL phase lock check	–
hwobs_abedpll_bypassack	dspDpllPhaseLock	dspDPLL phase lock check	–
hwobs_abedpll_idle	dspDpllPhaseLock	dspDPLL phase lock check	–

18.4.11.5.14 Other PERIPH DPLL Observable Signals

Table 18-52 describes the mapping of CORE DPLL observability signals (other than CLKOUT) to the SYSCTRL_GENERAL_CORE DPLL observing inputs. The selection of PERIPH DPLL as the source of the additional DPLL signals is done at the YSCTRL_GENERAL_CORE level by setting bit field MULT = 0x2 inside each of the eight registers (CONTROL_CONF_DPLL_FREQLOCK_SEL through CONTROL_CONF_DPLL_IDLE_SEL).

Table 18-52. Other PERIPH DPLL Observability Signals

SYSCTRL_GENERAL_CORE Observability Inputs Tied to PERIPH DPLL Observable Signals	Other PERIPH DPLL Observable Signals Mapped to SYSCTRL_GENERAL_CORE Observability Inputs	Signal Description	Logical Value Meaning
hwobs_perdpll_freqlock	PERIPHdpll_freqlock	PERIPH DPLL frequency lock check	–
hwobs_perdpll_tinitz	PERIPHdpll_tinitz	Check PERIPH DPLL status, lock/relock time.	–
hwobs_perdpll_phaselock	PERIPHDpllPhaseLock	PERIPH DPLL phase lock check	–
hwobs_perdpll_tenable	dspDpllPhaseLock	dspDPLL phase lock check	–
hwobs_perdpll_tenablediv	dspDpllPhaseLock	dspDPLL phase lock check	–
hwobs_perdpll_bypassack	dspDpllPhaseLock	dspDPLL phase lock check	–
hwobs_perdpll_idle	PERIPHDpllPhaseLock	PERIPH DPLL phase lock check	–

18.4.11.5.15 Other DSI1 DPLL Observable Signals

Table 18-53 describes the mapping of CORE DPLL observability signals (other than CLKOUT) to the SYSCTRL_GENERAL_CORE DPLL observing inputs. The selection of DSI1 DPLL as the source of the additional DPLL signals is done at the SYSCTRL_GENERAL_CORE level by setting bit field MULT = 0x3 inside each of the eight registers (CONTROL_CONF_DPLL_FREQLOCK_SEL through CONTROL_CONF_DPLL_IDLE_SEL).

Table 18-53. Other DSI1 DPLL Observability Signals

SYSCTRL_GENERAL_CORE Observability Inputs Tied to DSI1 DPLL Observable Signals	Other DSI1 DPLL Observable Signals Mapped to SYSCTRL_GENERAL_CORE Observability Inputs	Signal Description	Logical Value Meaning
hwobs_dsi1dpll_freqlock	dspdpll_freqlock	dspDPLL frequency lock check	–
hwobs_dsi1dpll_tinitz	dspdpll_tinitz	Check dspDPLL status, lock/relock time.	–

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Table 18-53. Other DSI1 DPLL Observability Signals (continued)

SYSCTRL_GENERAL_CORE Observability Inputs Tied to DSI1 DPLL Observable Signals	Other DSI1 DPLL Observable Signals Mapped to SYSCTRL_GENERAL_CORE Observability Inputs	Signal Description	Logical Value Meaning
hwobs_dsi1dpll_phaselock	dspDpllPhaseLock	dspDPLL phase lock check	–
hwobs_dsi1dpll_tenable	dspDpllPhaseLock	dspDPLL phase lock check	–
hwobs_dsi1dpll_tenablediv	dspDpllPhaseLock	dspDPLL phase lock check	–
hwobs_dsi1dpll_bypassack	dspDpllPhaseLock	dspDPLL phase lock check	–
hwobs_dsi1dpll_idle	dspDpllPhaseLock	dspDPLL phase lock check	–

18.4.11.5.16 Other DSI2 DPLL Observable Signals

Table 18-54 describes the mapping of CORE DPLL observability signals (other than CLKOUT) to the SYSCTRL_GENERAL_CORE DPLL observing inputs. The selection of DSI2 DPLL as the source of the additional DPLL signals is done at the SYSCTRL_GENERAL_CORE level by setting bit field MULT = 0x4 inside each of the eight registers (CONTROL_CONF_DPLL_FREQLOCK_SEL through CONTROL_CONF_DPLL_IDLE_SEL).

Table 18-54. Other DSI2 DPLL Observability Signals

SYSCTRL_GENERAL_CORE Observability Inputs Tied to DSI2 DPLL Observable Signals	Other DSI2 DPLL Observable Signals Mapped to SYSCTRL_GENERAL_CORE Observability Inputs	Signal Description	Logical Value Meaning
hwobs_dsi2dpll_freqlock	PERIPHdpll_freqlock	PERIPH DPLL frequency lock check	–
hwobs_dsi2dpll_tinitz	PERIPHdpll_tinitz	Check PERIPH DPLL status, lock/relock time.	–
hwobs_dsi2dpll_phaselock	PERIPHDpllPhaseLock	PERIPH DPLL phase lock check	–
hwobs_dsi2dpll_tenable	dspDpllPhaseLock	dspDPLL phase lock check	–
hwobs_dsi2dpll_tenablediv	dspDpllPhaseLock	dspDPLL phase lock check	–
hwobs_dsi2dpll_bypassack	dspDpllPhaseLock	dspDPLL phase lock check	–
hwobs_dsi2dpll_idle	PERIPHDpllPhaseLock	PERIPH DPLL phase lock check	–

18.4.11.5.17 Other USB DPLL Observable Signals

Table 18-55 shows mapping of (other than CLKOUT) CORE dpll observability signals to the SYSCTRL_GENERAL_CORE dpll observing inputs. The selection of USB DPLL as the source of the additional DPLL signals is done at SYSCTRL_GENERAL_CORE level through setting bit field MULT=0x6 inside all of the eight registers - CONTROL_CONF_DPLL_FREQLOCK_SEL through CONTROL_CONF_DPLL_IDLE_SEL.

Table 18-55. Other USB DPLL Observability Signals

SYSCTRL_GENERAL_CORE Observability Inputs Tied to USB DPLL Observable Signals	Other USB DPLL Observable Signals Mapped to SYSCTRL_GENERAL_CORE Observability inputs	Signal Description	Logical Value Meaning
hwobs_usbdpll_freqlock	dspdpll_freqlock	dspDPLL frequency lock check	–
hwobs_usbdpll_tinitz	dspdpll_tinitz	Vheck dspDPLL status, lock/relock time.	–
hwobs_usbdpll_phaselock	dspDpllPhaseLock	dspDPLL phase lock check	–
hwobs_usbdpll_tenable	dspDpllPhaseLock	dspDPLL phase lock check	–

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Table 18-55. Other USB DPLL Observability Signals (continued)

SYSCTRL_GENERAL_CORE Observability Inputs Tied to USB DPLL Observable Signals	Other USB DPLL Observable Signals Mapped to SYSCTRL_GENERAL_CORE Observability inputs	Signal Description	Logical Value Meaning
hwobs_usbdpll_tenablediv	dspDpllPhaseLock	dspDPLL phase lock check	–
hwobs_usbdpll_bypassack	dspDpllPhaseLock	dspDPLL phase lock check	–
hwobs_usbdpll_idle	dspDpllPhaseLock	dspDPLL phase lock check	–

18.4.12 Functional Register Description

18.4.12.1 DSP Boot Register

This information is not available in the public domain.

18.4.12.1.1 PBIASLITE Control Register

Table 18-56 describes the CONTROL_PBIASLITE register, which controls some settings of PBIASLITE cells for the MMC I/O interface.

Table 18-56. PBIAS Control Register

Physical Address	Register Name	Description	Access
0x4A10 0600	CONTROL_PBIASLITE	Control settings for PBIAS cell	RW

18.4.12.2 Temperature Sensor Control Registers

Table 18-57 describes the CONTROL_TEMP_SENSOR registers of the general core control module, which control the temperature sensor, band gap state-machine, and thermal post-processing logic.

Table 18-57. Temperature Sensor Register

Physical Address	Register Name	Description	Access
0x4A00 232C	CONTROL_TEMP_SENSOR	Temperature sensor control register	R/W
0x4A00 2378	CONTROL_BANDGAP_CTRL	Mode selection and mask hot/cold event register	R/W
0x4A00 237C	CONTROL_BANDGAP_COUNTER	Band gap delay counter register	R/W
0x4A00 2380	CONTROL_BANDGAP_THRESHOLD	Band gap thermal alert threshold register	R/W
0x4A00 2384	CONTROL_TSHUT_THRESHOLD	Tshut threshold register	R/W
0x4A00 2388	CONTROL_BANDGAP_STATUS	Thermal alert and band gap idle events status register	RO

18.4.12.2.1 CSI Receiver Control Register

To enable the physical layer of the camera receiver, the programmer manipulates the bits within the CONTROL_CAMERA_RX register.

Table 18-58. CSI Receiver Control Register

Physical Address	Register Name	Description	Access
0x4A10 0608	CONTROL_CAMERA_RX	Module dedicated configurations	RW

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18.4.12.3 Protection Status Registers

Table 18-59 lists the status registers.

Table 18-59. Protection Status Registers

Physical Address	Register Name	Description	Access
0x4A00 22D0	CONTROL_SEC_ERR_STATUS_FUNC	Protection firewall error status register	Public (R)
0x4A00 22D4	CONTROL_SEC_ERR_STATUS_DEBUG	Protection firewall error status register debug	Public (RW)

These registers do not depend on the device type.

The CONTROL_PROT_ERR_STATUS_FUNC can be read in public mode, but cannot be written.

The CONTROL_PROT_ERR_STATUS_DEBUG register is both read and write accessible in GP devices.

These bits are cleared when the L3 and L4 firewall embedded-error log registers are cleared. All bits in these registers reflect internal events in the device related to the device protection.

On a specific event (signal rising edge), the corresponding bit is set. On a rising edge, the input signal must stay high for at least two interface clock periods to be recognized. Software must clear each bit after reviewing the events.

When a protection violation occurs, the following bits are set:

- In application mode
  - CONTROL_SEC_ERR_STATUS_FUNC[01] = L3RAM protection violation
  - CONTROL_SEC_ERR_STATUS_FUNC[02] = GPMC protection violation
  - CONTROL_SEC_ERR_STATUS_FUNC[03] = EMIF protection violation
  - CONTROL_SEC_ERR_STATUS_FUNC[04] = IVA-HD protection violation
  - CONTROL_SEC_ERR_STATUS_FUNC[05] = Dual Cortex™-M3 protection violation
  - CONTROL_SEC_ERR_STATUS_FUNC[06] = SL2 protection violation
  - CONTROL_SEC_ERR_STATUS_FUNC[12] = C2C protection violation
  - CONTROL_SEC_ERR_STATUS_FUNC[13] = SGX protection violation
  - CONTROL_SEC_ERR_STATUS_FUNC[14] = DSS protection violation
  - CONTROL_SEC_ERR_STATUS_FUNC[15] = ISS protection violation
  - CONTROL_SEC_ERR_STATUS_FUNC[16] = L4_PER protection violation
  - CONTROL_SEC_ERR_STATUS_FUNC[17] = L4_CFG protection violation
  - CONTROL_SEC_ERR_STATUS_FUNC[18] = DEBUGSS protection violation
  - CONTROL_SEC_ERR_STATUS_FUNC[19] = L4 AudioBE protection violation
  - CONTROL_SEC_ERR_STATUS_FUNC[20] = C2C INIT protection violation
- In debug mode:
  - CONTROL_SEC_ERR_STATUS_DEBUG[01] = L3RAM protection violation
  - CONTROL_SEC_ERR_STATUS_DEBUG[02] = GPMC protection violation
  - CONTROL_SEC_ERR_STATUS_DEBUG[03] = EMIF protection violation
  - CONTROL_SEC_ERR_STATUS_DEBUG[04] = IVA-HD protection violation
  - CONTROL_SEC_ERR_STATUS_DEBUG[05] = Dual Cortex-M3 protection violation
  - CONTROL_SEC_ERR_STATUS_DEBUG[06] = SL2 protection violation
  - CONTROL_SEC_ERR_STATUS_DEBUG[12] = C2C protection violation
  - CONTROL_SEC_ERR_STATUS_DEBUG[13] = SGX protection violation
  - CONTROL_SEC_ERR_STATUS_DEBUG[14] = DSS protection violation
  - CONTROL_SEC_ERR_STATUS_DEBUG[15] = ISS protection violation
  - CONTROL_SEC_ERR_STATUS_DEBUG[16] = L4_PER protection violation

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- CONTROL_SEC_ERR_STATUS_DEBUG[17] = L4_CFG protection violation
- CONTROL_SEC_ERR_STATUS_DEBUG[18] = DEBUGSS protection violation
- CONTROL_SEC_ERR_STATUS_DEBUG[19] = L4 AudioBE protection violation
- CONTROL_SEC_ERR_STATUS_DEBUG[20] = C2C INIT protection violation

For more information about L4 firewall protection-violation report mechanisms , see , *Firewall Error Logging in the Control Module*. For more information about L3 firewall protection-violation report mechanisms, see , *L3 Interconnect Error Analysis.*

18.4.12.4 Protection SDRAM Configuration Registers

Table 18-60, *Protection SDRAM Configuration Registers for EMIF1 and EMIF2*, lists the protection SDRAM configuration registers for EMIF1 and EMIF2 that are part of the general wakeup control module. Upon POR, their values are exported as reset values of the EMIF1 and EMIF2 registers (EMIF_SDRAM_CONFIG and EMIF_SDRAM_CONFIG_2, respectively).

Table 18-60. Protection SDRAM Configuration Registers for EMIF1 and EMIF2

Physical Address	Register Name	Description	Access
0x4A30C110	CONTROL_WKUP_PROT_EMIF1_SDRAM_CONFIG_REG	Protection SDRAM configuration register 1, defining bit field reset values of the EMIF1.EMIF_SDRAM_CONFIG register	RW
0x4A30C114	CONTROL_WKUP_PROT_EMIF1_SDRAM_CONFIG2_REG	Protection SDRAM configuration register 2, defining bit field reset values of the EMIF1.EMIF_SDRAM_CONFIG_2 register	RW
0x4A30C118	CONTROL_WKUP_PROT_EMIF2_SDRAM_CONFIG_REG	Protection SDRAM configuration register 1, defining bit field reset values of the EMIF2.EMIF_SDRAM_CONFIG register	RW
0x4A30C11C	CONTROL_WKUP_PROT_EMIF2_SDRAM_CONFIG2_REG	Protection SDRAM configuration register 2, defining bit field reset values of the EMIF2.EMIF_SDRAM_CONFIG_2 register	RW

18.4.12.5 Register Controls for the LPDDR2IO1/LPDDR2IO2 I/O Buffer Modes

Global LPDDR2IO1/LPDDR2IO2 (EMIF1 and EMIF2 associated) phycmd0 and phydata0–phydata3 I/O buffer controls are part of the SYSCTRL_GENERAL_CORE.CONTROL_GEN_CORE_ OCPREG_SPARE register. Their functionality is as follows:

- Programming the OCPREG_SPARE[1] and OCPREG_SPARE[3] bits to high brings the PWRDN signal to the I/O buffers driven by the emif1/emif2phydata0 through emif/emif2phydata3 components, respectively, to low; as a consequence, power-down mode for these I/O buffers is activated.

  The PWRDN software controls do not affect the emif1/emif2phycmd0 components.
- Programming the OCPREG_SPARE[0] and OCPREG_SPARE[2] bits to high enables the low-voltage CMOS buffer logic for the emif1/emif2phydata0-emif1/emif2phydata3 and emif1/emif2phycmd0 components, respectively. Programming the OCPREG_SPARE[0] and OCPREG_SPARE[2] bits to low enables a true differential comparator.
- Upon POR, the value of the register is 0x0. The PWRDN signal is high (power-down mode is inactive) and CMOSEN is low at the pads (differential comparator enable).

CAUTION

The bits in CONTROL_GEN_CORE_OCPREG_SPARE must not be updated.

Table 18-61 lists the register used to control the described EMIF1 and EMIF2 features.

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Table 18-61. LPDDR2IO Buffer Control Register

Physical Address	Register Name	Description	Access
0x4A0023FC	CONTROL_GEN_CORE_OCPREG_SPARE	The lower 4 bits of this register are assigned to control the power-down mode and enable the LVCMOS buffers associated with the EMIF1 and EMIF2 PHY components.	RW

18.4.12.6 EMIF DLL Master/Slave Specific Registers

18.4.12.6.1 EMIF DLL Slaves Individual Offset Compensation

Delays used to time the DQS signals of the LPDDR2 interface vary for the different DDR PHY DLL slaves associated with an EMIF controller instance. An individual offset compensation is provided for each of the four DLL slaves to achieve symmetrical timings.

Two 32-bit registers (CONTROL_EMIF1_OFFSET and CONTROL_EMIF2_OFFSET) in the general core control module are dedicated to hold four signed-offset programmable values for the EMIF1 and EMIF2 PHY DLL slaves, respectively. The following programming points apply to these registers:

- Offset is stored as 2s complement 8-bit value, ranging from –128 to +127.
- Reset value is 0 (that is, by default, no offset is applied).
- The programmed values are saved and restored during an off mode transition.

The slave delay ratio value also has a single software control for all DLLs associated with an EMIF instance (the EMIF1.EMIF_DDR_PHY_CTRL_1[11:4] REG_DLL_SLAVE_DLY_CTRL bit field in the EMIF1 address space and EMIF2.EMIF_DDR_PHY_CTRL_1[11:4] REG_DLL_SLAVE_DLY_CTRL bit field in the EMIF2 address space). For more information , see Chapter 15, *Memory Subsystem.*

The control sent to each DLL slave is the EMIF1/EMIF2 control (REG_DLL_SLAVE_DLY_CTRL) and the local signed offset, which is stored in the DLL slave corresponding bit field in the CONTROL_EMIF1_OFFSET/ CONTROL_EMIF2_OFFSET registers. DLL Slave Delay Control Schema shows the DLL slave delay control schema.

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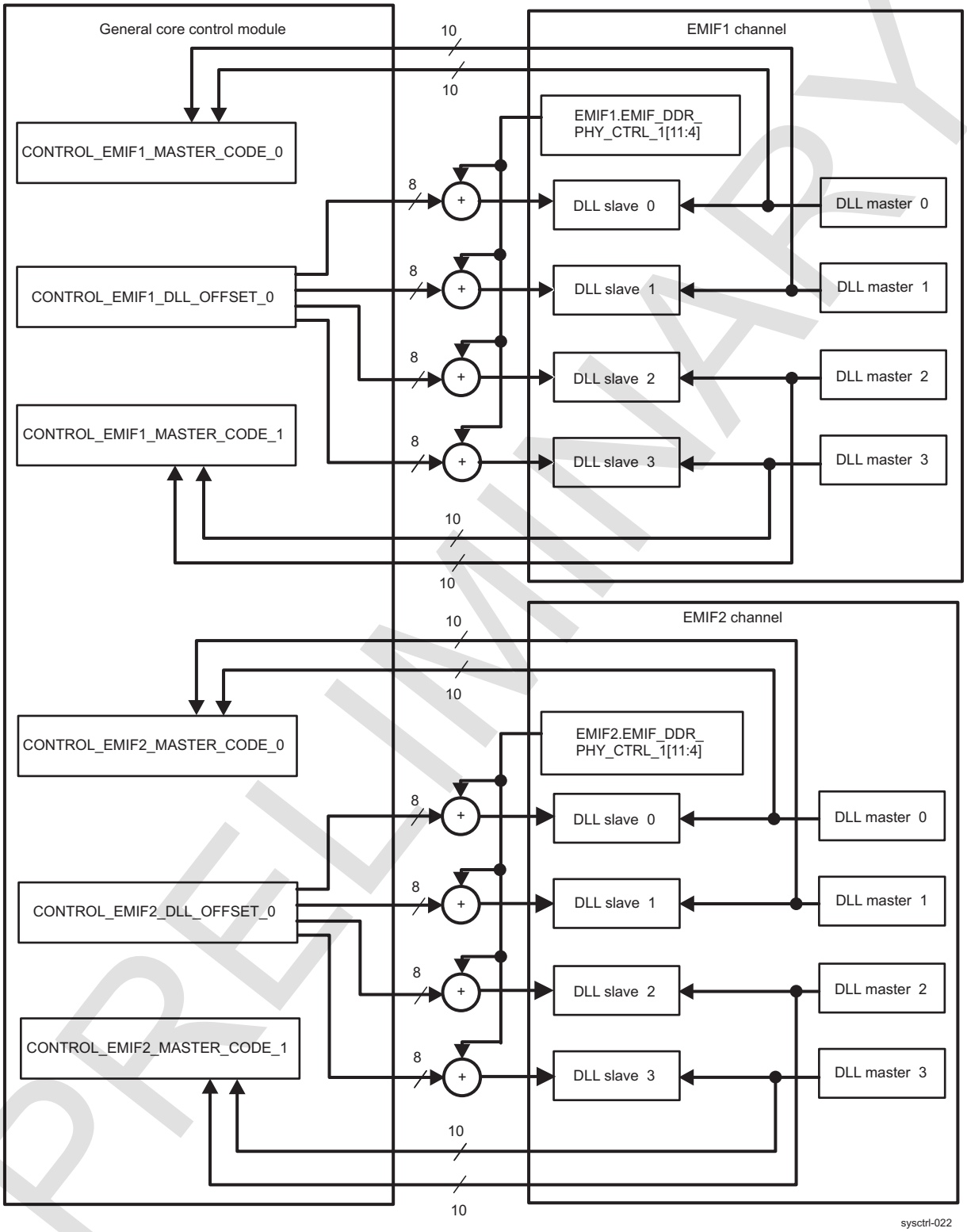
Figure 18-23. DLL Slave Delay Control Schema



Because the adders work in saturation mode, there is no wrap-around on either end of the spectrum:

- Any value higher than 0xFF saturates to 0xFF.
- Any value lower than 0x00 saturates to 0x00.

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Table 18-62 describes the control registers in general core control module dedicated to store delay offsets individually for the four DDR PHY DLL slaves.

Table 18-62. EMIF DLL Slave Offset Compensation Registers

Physical Address	Register Name	Description	Access
0x4A00 2360	CONTROL_EMIF1_OFFSET	EMIF1 slaves individual DLL offset controls	R/W
0x4A00 2364	CONTROL_EMIF2_OFFSET	EMIF2 slaves individual DLL offset controls	R/W

18.4.12.6.2 EMIF DLL Master Code Monitoring Registers

As can be seen in Figure 18-23, two read-only (RO) registers are provided in the general core control module to monitor DLL master codes for each of the EMIF1 and EMIF2 instances.

The 40 EMIF1 DLL master code monitoring signals are distributed as 20 read-only bits in the CONTROL_EMIF1_MASTER_CODE_0 register and 20 read-only bits in the CONTROL_EMIF1_MASTER_CODE_1 register, respectively.

Similarly, the 40 EMIF2 DLL master code monitoring signals are distributed as 20 read-only bits in the CONTROL_EMIF2_MASTER_CODE_0 register and 20 read-only bits in the CONTROL_EMIF2_MASTER_CODE_1 register, respectively.

Table 18-63 lists the control registers in general core control module dedicated to monitor the master code for the four DDR PHY DLLs.

Table 18-63. EMIF DLL Master Code-Monitoring Registers

Physical Address	Register Name	Description	Access
0x4A00 2368	CONTROL_EMIF1_MASTER_CODE_0	EMIF1 Master 0, 1 code	RO
0x4A00 236C	CONTROL_EMIF1_MASTER_CODE_1	EMIF1 Master 2, 3 code	RO
0x4A00 2370	CONTROL_EMIF2_MASTER_CODE_0	EMIF2 Master 0, 1 code	RO
0x4A00 2374	CONTROL_EMIF2_MASTER_CODE_1	EMIF2 Master 2, 3 code	RO

18.4.12.7 EMIF Read Pipeline Control Register

The EMIF1 and EMIF2 instances have dedicated control bits in the device core control module register (CONTROL_EMIF) to enable the EMIF read pipeline.

Table 18-64. EMIF Read Pipeline Control Register

Physical Address	Register Name	Description	Access
0x4A10 0694	CONTROL_EMIF	EMIF1, EMIF2 read pipeline enable	R/W

18.4.12.8 Force MPU Write Nonposted Transactions Control Register

At the top level, software can force all writes from the MPU subsystem to the L3 interconnect to be nonposted, regardless of the attributes of the transactions coming from the Cortex-A9 CPU. When active-high bit FORCEWRNP = 1, only nonposted write commands are sent to the L3 interconnect. This bit must remain stable for the entire transfer and must not change in between the transfer.

Table 18-65 describes the general core control module register with FORCEWRNP control.

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Table 18-65. Force MPU Write Nonposted Transactions Control Register

Physical Address	Register Name	Description	Access
0x4A00 03C0	CONTROL_FORCEWRNP	Forces only nonposted write commands from the MPU subsystem to the L3 interconnect	R/W

18.4.12.9 Signal Integrity Parameter Control Registers With Pad Group Assignment

18.4.12.9.1 Signal Integrity Parameter Controls Overview

Most of the I/O cells associated with the device pads can be configured to deliver their carried signals to the targeted sink with maximum signal integrity. Configuration of these I/Os is done by pad group assignment and not individually per pad.

The different I/O-specific requirements determine the use of different types of I/O cells for the device I/Os. Software controls associated with the signal integrity parameters are implemented at the SYSCTRL_PADCONF_CORE and SYSCTRL_PADCONF_WKUP level.

The following types of I/O cells associated with pad groups can be identified:

- LPDDR2 high-speed I/O cells with impedance(I), slew rate(SR), and weak driver (WD) settings
- High-speed I/O cells with far-end load (LB) settings
- Low -speed I/O cells with combined slew rate (SC) and load versus transmission line (TL) length (LB) settings
- Two types of I/O cells with mode (MB) controls and load compensation (LB) settings
- I/O cells with control (DS0) of the impedance mode
- C2C I/O cells with LB0 control adjustable according to interface requirement/voltage mode
- I/O cells with pullup strength (PUSTRENGTH) and speed controls
- I2Cx I/O cells with pullup resistance vers capacitance load settings
- JTAG I/O cells with bus-holder enable control

NOTE: I/Os are non-failsafe, which means that voltage must never be applied at a pad before the internal I/O supply voltage VDDS is powered.

The pad group-assigned signal integrity controls are provided through the registers described in Table 18-66.

Table 18-66. Signal Integrity Parameter Control Registers

Physical Address	Register Name	Description	Access
0x4A10 05A8	CONTROL_SMART1IO_PADCONF_0	Signal integrity pad group assignment control register	R/W
0x4A10 05AC	CONTROL_SMART1IO_PADCONF_1	Signal integrity pad group assignment control register	R/W
0x4A10 05B0	CONTROL_SMART2IO_PADCONF_0	Signal integrity pad group assignment control register	R/W
0x4A10 05B4	CONTROL_SMART2IO_PADCONF_1	Signal integrity pad group assignment control register	R/W
0x4A10 05B8	CONTROL_SMART3IO_PADCONF_0	Signal integrity pad group assignment control register	R/W
0x4A10 05BC	CONTROL_SMART3IO_PADCONF_1	Signal integrity pad group assignment control register	R/W
0x4A10 05C0	CONTROL_SMART3IO_PADCONF_2	Signal integrity pad group assignment control register	R/W

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Table 18-66. Signal Integrity Parameter Control Registers (continued)

Physical Address	Register Name	Description	Access
0x4A10 05C4	CONTROL_USBB_HSIC	Signal integrity pad group assignment control register	R/W
0x4A10 05C8	CONTROL_SMART3IO_PADCONF_3	Signal integrity pad group assignment control register	R/W
0x4A10 05CC	CONTROL_SMART2IO_PADCONF_2	Signal integrity pad group assignment control register	R/W
0x4A10 05D0	CONTROL_SMART1IO_PADCONF_2	Signal integrity pad group assignment control register	R/W
0x4A10 05D4	CONTROL_SMART1IO_PADCONF_3	Signal integrity pad group assignment control register	R/W
0x4A10 05D8	CONTROL_C2CIO_PADCONF_0	Signal integrity pad group assignment control register	R/W
0x4A10 0604	CONTROL_I2C_0	Signal integrity pad group assignment control register	R/W
0x4A10 0628	CONTROL_MMC1	Signal integrity pad group assignment control register	R/W
0x4A10 0638	CONTROL_LPDDR2IO1_0	Signal integrity pad group assignment control register	R/W
0x4A10 063C	CONTROL_LPDDR2IO1_1	Signal integrity pad group assignment control register	R/W
0x4A10 0640	CONTROL_LPDDR2IO1_2	Signal integrity pad group assignment control register	R/W
0x4A10 0644	CONTROL_LPDDR2IO1_3	Signal integrity pad group assignment control register	R/W
0x4A10 0648	CONTROL_LPDDR2IO2_0	Signal integrity pad group assignment control register	R/W
0x4A10 064C	CONTROL_LPDDR2IO2_1	Signal integrity pad group assignment control register	R/W
0x4A10 0650	CONTROL_LPDDR2IO2_2	Signal integrity pad group assignment control register	R/W
0x4A10 0654	CONTROL_LPDDR2IO2_3	Signal integrity pad group assignment control register	R/W
0x4A31 E5A0	CONTROL_SMART1NOPMIO_PADCONF_0	Signal integrity pad group assignment control register	R/W
0x4A31 E5A4	CONTROL_SMART1NOPMIO_PADCONF_1	Signal integrity pad group assignment control register	R/W
0x4A31 E5B0	CONTROL_SMART3NOPMIO_PADCONF_0	Signal integrity pad group assignment control register	R/W
0x4A31 E5B4	CONTROL_SMART3NOPMIO_PADCONF_1	Signal integrity pad group assignment control register	R/W
0x4A31 E604	CONTROL_I2C_2	Signal integrity pad group assignment control register	R/W
0x4A31 E608	CONTROL_JTAG	Signal integrity pad group assignment control register	R/W

18.4.12.9.2 High-Speed I/O Buffers With Impedance, Slew Rate, and Weak Driver Settings

The LPDDR2IO (EMIF) buffers are based on high-speed unterminated logic and require excellent driver impedance control to achieve optimal timing–EMI trade-offs. A specific type of device I/O cell with programmable features is used to meet this requirement. These I/O cells also support the high-speed interchip (HSIC) interface.

Three types of software-configurable I/O cells are integrated to support high-speed unterminated logic:

- Single-ended I/O cells
- Two-pad differential I/O cells

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- Vref generation cell

Two-pad differential I/O cells are provided with a differential receiver and complementary transmitter. They are used to support the LPDDR2 clock pads (lpddr21_ck, lpddr21_nck, lpddr22_ck, lpddr22_nck) and LPDDR2 strobe pads (lpddr21_dqsi, lpddr21_ndqsi, lpddr22_dqsi, and lpddr22_ndqsi ,where i = 0 to 3).

A Vref-generation cell is integrated in the device to supply a Vref-based receiver.

These I/O cells are integrated with the following controls in the SYSCTRL_PADCONF_CORE module:

- Driver output impedance (I) controls
- SR controls
- WD controls to support LPDDR2/HSIC interface and avoid floating pad
- Process-only impedance compensation using 5-bit binary coded schema separately for pullup p1:5 and pulldown n1:5 impedance
- Internal and external reference voltage source selection for the Vref generation cell
- Vref cell decoupling capacitor selection

Programmable bits for impedance and SR control are provided when the I/Os are set to operate in driver mode (outputs).

The bits I[2:0] are used to program the desired impedance value of the driver.

The drive strengths corresponding to the I[2:0] value are aliased as Drv i (where i = 5 to 12) in the CONTROL_LPDDR2IO1_x and CONTROL_LPDDR2IO2_x, (where x = 0 to 2) register tables in Section 18.6.7, *SYSCTRL_PADCONF_CORE Register Description*.

CAUTION

To ensure the best performance of the LPDDR2 I/Os, it is strongly recommended for user software to always set the impedance controlling bits (I) in the CONTROL_LPDDR2IO1_x and CONTROL_LPDDR2IO2_x registers (where x = 0 to 2) to 0x7, which corresponds to Drv12 mode.

For more information about LPDDR2 I/O-specific driver output impedance (respectively, corresponding drive strength) parameter, see the *Electrical Characteristics/DC Electrical Characteristics/LPDDR2 DC Electrical Characteristics* section in the device data manual.

User software can program the slew rate (turn-on time) of the output signal using the control bits SR[1:0] in the CONTROL_LPDDR2IO1_x and CONTROL_LPDDR2IO2_x (where x = 0 to 2) registers.

For more information about the LPDDR2 I/O slew rate parameter control, SR[1:0], see the *Electrical Characteristics/DC Electrical Characteristics/LPDDR2 DC Electrical Characteristics* section in the device data manual.

Weak pullup/down or a keeper on pad is enabled through the wd0 and wd1 bits. The weak pullup/down option is used to define the pad state (high or low) when no signal is driving the pad. The weak keeper option is used to maintain the previous output value when nothing is driving the pad. Table 18-67 describes the WD controls.

NOTE: The WD[1:0] bit field controls play the role of the PULLTYPESELECT and PULLUDENABLE bits within the standard pad configuration registers, and provides the keeper function to the I/Os with the state WD = 0b11. For LPDDR2 I/Os, the WD controls do not apply during off mode.

Similar to the lpddr1_x and lpddr2_x pads, the usbb1_hsic_data/strobe and usbb2_hsic_data/strobe pads also have weak driver software controls for active-mode internal weak pullups and pulldowns. They are in the CONTROL_USBB_HSIC register.

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In contrast to the LPDDR2 I/Os, the usbb1_hsic and usbb2_hsic pads are also provided with bits in the same register to select weak pullup/down and keeper function during off mode. For a given usbbx_hsic_data/strobe pad (where x = 1, 2) the associated bit to allow an off mode-specific pullup/pulldown/keeper setting is OFFMODE_WD_ENABLE. The off mode option is defined through the OFFMODE_WD[1:0] bit field in the CONTROL_USBB_HSIC register..

Table 18-67. Weak Driver PUPD/Latch Mode

WD1	WD0	Operation
0	0	Pull logic disabled
0	1	Weak pullup enabled
1	0	Weak pulldown enabled
1	1	Weak keeper enabled

The following sequence is required to program the off-mode pullup/pulldown /latch (keeper) feature of the usbb1_hsic_data/usbb2_hsic_data and usbb1_hsic_strobe/usbb2_hsic_strobe pads:

1. Program the desired values for USBB1_HSIC_DATA_OFFMODE_WD/ USBB2_HSIC_DATA_OFFMODE_WD and USBB1_HSIC_STROBE_OFFMODE_WD/ USBB2_HSIC_STROBE_OFFMODE_WD in the CONTROL_USBB_HSIC register.
2. For an off-mode pullup/pulldown configuration different than the active-mode pullup/pulldown configuration, set the USBB1_HSIC_DATA_OFFMODE_WD_ENABLE/USBB2_HSIC_DATA_ OFFMODE_WD_ENABLE and USBB1_HSIC_STROBE_OFFMODE_WD_ENABLE/USBB2_HSIC_ STROBE_OFFMODE_WD_ENABLE bits to 1.

   If USBB1_HSIC_DATA_OFFMODE_WD_ENABLE/USBB2_HSIC_DATA_OFFMODE_WD_ENABLE is set to 0, the applied value of the pullup/pulldown after the device goes to off mode will be same as the value of the active pullup/pulldown (that is, in this case, the value of the OFFMODE PU/PD bit field is disregarded).

   If, for example, USBB1_HSIC_DATA_OFFMODE_WD/USBB2_HSIC_DATA_OFFMODE_WD is programmed with the same setting as USBB1_HSIC_DATA_WD/USBB2_HSIC_DATA_WD, then the value of USBB1_HSIC_DATA_OFFMODE_WD_ENABLE/USBB2_HSIC_DATA_OFFMODE_WD_ ENABLE does not matter.

   Therefore, USBB1_HSIC_DATA_OFFMODE_WD_ENABLE/USBB2_HSIC_DATA_OFFMODE_WD_ENABLE and USBB1_HSIC_STROBE_OFFMODE_WD_ENABLE/USBB2_HSIC_STROBE_OFFMODE_WD_ ENABLE apply only to off-mode pullup/pulldown selection.

The eFuse impedance compensation settings are exported upon POR to 10 bits in the CONTROL_EFUSE_2 register of the device control module as follows:

CONTROL_EFUSE_2[23] LPDDR2_PTV_N1 through CONTROL_EFUSE_2[19] LPDDR2_PTV_N5 (pulldown impedance trimming)

CONTROL_EFUSE_2[18] LPDDR2_PTV_P1 through CONTROL_EFUSE_2[14] LPDDR2_PTV_P5 (pullup impedance trimming)

CAUTION

Do not override the eFuse impedance compensation settings in the CONTROL_EFUSE_2 register.

NOTE: There is no software control (INPUTENABLE) for the input buffer of the high-speed unterminated logic I/Os associated with the lpddr21_x, lpddr22_x, usbb1_hsic_data/strobe, and usbb2_hsic_data/strobe pads. If the CMOS buffer is enabled, it is always bidirectional (that is, the input buffer is always enabled).

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Internal LPDDR2IO Vref-based receivers use the output voltage of LPDDR2-associated voltage reference cells. The voltage drive selection bit fields of the LPDDR2 voltage reference cells are in the CONTROL_LPDDR2IO1_3 and CONTROL_LPDDR2IO2_3 registers. Individual VREF_TAP[1:0] control bits set the output drive capability for each of the pads (where x = 1, 2):

- lpddr2x_vref_ca_int
- lpddr2x_vref_ca
- lpddr2x_vref_dq0_int–lpddr2x_vref_dq3_int
- lpddr2x_vref_dq

Table 18-68, *LPDDR2 Internal Reference Configuration*, lists the possible options for internal reference voltage drive selection.

Table 18-68. LPDDR2 Internal Reference Configuration

VREF_TAP1	VREF_TAP0	Description
0	0	Pad/bias2 Connected to internal reference VDDS/2, for 2-µA current load
0	1	Pad/bias2 Connected to internal reference VDDS/2, for 4-µA current load
1	0	Pad/bias2 Connected to internal reference VDDS/2, for 6-µA current load
1	1	Pad/bias2 Connected to internal reference VDDS/2, for 8-µA current load

When the internal Vref generator is turned on, it supplies voltage reference to the Vref-based receivers associated with th LPDDR2IO DQ and CA interface lines.

In Vref-based receiver mode, the LPDDR2 I/O cell receiver is a true differential comparator with pad connected to the positive terminal and VREF tied to the negative terminal. The Vref-based receiver allows the improvement of speed performance at VDDS = 1.2-V I/O voltage supply.

Setting bit CONTROL_LPDDR2IOx_3[0] LPDDR2x_INT_VREF_AUTO_EN_DQ = 0b1 or CONTROL_LPDDR2IOx_3[1] LPDDR2x_INT_VREF_AUTO_EN_CA = 0b1 (where x = 1, 2) enables the automatic shut off or switch-on of the internal Vref cell generators associated with the LPDDR2x interface, the DQ and CA lines, respectively.

If user software sets the manual control bit CONTROL_LPDDR2IOx_3[2] LPDDR2x_INT_VREF_EN_DQ = 0b1 or CONTROL_LPDDR2IOx_3[3] LPDDR2x_INT_VREF_EN_CA = 0b1, internal Vref cell generators are enabled, regardless of the state of the LPDDR2x_INT_VREF_AUTO_EN_DQ/LPDDR2x_INT_VREF_AUTO_EN_CA bits. Thus, automatic control over LPDDR2 Vref cell generators can always be overridden in the context of enabling the Vref generator.

If the Vref cell generator is enabled, the following pads (where x = 1, 2) act as outputs and can be used to supply reference voltage to external devices:

- lpddr2x_vref_ca_int
- lpddr2x_vref_ca
- lpddr2x_vref_dq0_int–lpddr2x_vref_dq3_int
- lpddr2x_vref_dq (where x = 1, 2)

CAUTION

While using the Vref cell in internal reference mode, nothing else must drive the pad externally, although the pad can be connected to supply a Vref signal to other devices.

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When the internal Vref cell generators are disabled and bypassed, which is provided when the bits LPDDR2x_INT_VREF_EN_DQ/CA = 0b0 and LPDDR2x_INT_VREF_AUTO_EN_DQ/CA = 0b0, the following pads (where x = 1, 2) act as inputs that can supply voltage reference to Vref-based receivers from external sources:

- lpddr2x_vref_ca_int
- lpddr2x_vref_ca
- lpddr2x_vref_dq0_int–lpddr2x_vref_dq3_int
- lpddr2x_vref_dq

NOTE: The LPDDR2x_INT_VREF_EN_DQ and LPDDR2x_INT_VREF_AUTO_EN_DQ controls determine the direction of the lpddr2x_vref_dq0_int–lpddr2x_vref_dq3_int and lpddr2x_vref_dq pads. Similarly, the LPDDR2x_INT_VREF_EN_CA and LPDDR2x_INT_VREF_AUTO_EN_CA controls determine the direction of the lpddr2x_vref_ca_int and lpddr2x_vref_ca pads.

Table 18-69 provides different combinations of Vref cell control types, the state of the Vref cell, and the associated voltage reference pad direction.

Table 18-69. LPDDR2 Vref Cells State Description

LPDDR2x_INT_VREF_EN_DQ/CA (Manual Control Bits)	LPDDR2x_INT_VREF_AUTO_EN_DQ/CA (AUTO Control Bits)	Type of Control	Vref Cell State	Voltage Reference Pad Direction
1	x	Manual	Enabled	O
0	1	AUTO	Automatically enabled/disabled	O
0	0	–	Disabled and bypassed	I

According to the noise environment, the user can choose to filter the reference voltage, which is supplied at the internal VREF node (receiver comparators Vref input), by the Vref cell generator or by an external source. Two coupling capacitors, internal to the LPDDR2 Vref cell, are available at the internal VREF node, and are configurable as specified in Table 18-70.

Table 18-70. LPDDR2 Vref Cell Decoupling Cap Selection

VREF_CCAP0	VREF_CCAP1	Capacitor
0	0	No capacitor connected
0	1	Capacitor between internal reference node and VDDS
1	0	Capacitor between internal reference node and VSS
1	1	Capacitor between internal reference node and VDDS as well as internal reference node and VSS

Individual VREF_CCAP0 and VREF_CCAP1 control bits in the CONTROL_LPDDR2IO1_3 and CONTROL_LPDDR2IO2_3 registers set the internal coupling capacitor connection at the internal VREF node for each of the following pads (where x = 1, 2):

- lpddr2x_vref_ca_int
- lpddr2x_vref_ca
- lpddr2x_vref_dq0_int–lpddr2x_vref_dq3_int
- lpddr2x_vref_dq

18.4.12.9.3 Low-Speed I/Os Combined Slew Rate vs TL Length and Load Settings

The low-speed I/O cells slew modes are selectable through the slew mode control SC[1:0] bit field. These settings act like coarse settings for the signal performance behavior of the low-speed I/Os.

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The low-speed I/O cells far-end capacitance load can be selected according to the transmission line (TL) length settings by modifying load bits LB[1] and LB[0] appropriately. These settings fine-tune the signal performance.

The pads featuring low-speed I/O cells require different SC[1:0] and LB[1:0] bit field settings to achieve optimal electrical performance for the multiplexed interface. This behavior may depend on various factors:

- Section 18.4.12.9.9, *Device Interfaces Signal Group Controls Mapping*, describes the different interfaces that have SC[1:0] and LB[1:0] controls and their pad corresponding software control registers.
- The *Electrical Characteristics/DC Electrical Characteristics* section of the device data manual provides more information about the specific SC[1:0] and LB[1:0] bit field settings applicable to these interfaces multiplexed to low-speed I/O pads.

18.4.12.9.4 I/Os With Combined Mode and Load Settings

There are two subtypes (conditionally described as type 1 and type 2 throughout this chapter) of device I/Os, with combined mode and load settings, that differ primarily in typical output impedance and mode-specific performance. Type 1 I/Os feature a lower typical output impedance than type 2.

Both I/Os have an output buffer with an internal pad voltage SR control mechanism. Each of the type 1 and type 2 corresponding I/O cells is controlled from two mode bits (MB0 and MB1) and a dedicated bit (LB0) for load compensation. LB0 programs the CLoad for the I/O cell associated pads. The table also lists the load bit settings.

The pads featuring type 1 and type 2 I/O cells with combined mode and load settings require different MB[1:0] and LB0 bit field settings to achieve optimal electrical performance for the multiplexed interface. This behavior may depend on various factors:

- Section 18.4.12.9.9, *Device Interfaces Signal Group Controls Mapping*, describes the different interfaces that have type 1 and type 2 MB and LB0 controls and the type 1 and type 2 I/O cell pad corresponding software control registers.
- The *Electrical Characteristics/DC Electrical Characteristics* section the device data manual provides more information about the specific MB[1:0] and LB0 bit field settings applicable to these interfaces multiplexed to type 1 and type 2 I/O pads with combined mode and load controls.

A process-only compensation using a 4-bit binary-coded schema is used separately for pullup/down output parameter variations.

For type 1 I/Os, only mode 2 does not use such compensation.

For type 2 I/Os, only mode 1 and mode 2 use eFuse process-only compensation to reduce the spread in timing parameters.

The I/Os with combined mode and load controls share the same compensation settings with the I/Os with driver output impedance (DS) settings and with the C2CI/O buffers. They are exported from eFuse upon POR to the following bits in the CONTROL_EFUSE_2 register:

CONTROL_EFUSE_2[31] EFUSE_SMART2TEST_P0 through CONTROL_EFUSE_2[28] EFUSE_SMART2TEST_P3 (pullup output parameters trimming)

CONTROL_EFUSE_2[27] EFUSE_SMART2TEST_N0 through CONTROL_EFUSE_2[24] EFUSE_SMART2TEST_N3 (pulldown output parameters trimming)

CAUTION

Do not override the SMART2TEST_P/SMART2TEST_N eFuse compensation settings in the CONTROL_EFUSE_2 register.

18.4.12.9.5 I/O Cells With Configurable Impedance Mode

The impedance mode at which this type of I/O cell operates is selected by setting a single bit drive strength control, DS0, as follows:

- DS0 = 1 selects mode 1, corresponding to 25-Ω impedance mode

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- DS0 = 0 selects mode 2, corresponding to 50-Ω impedance mode

The pads featuring I/O cell with configurable impedance mode require different DS0 bit settings to achieve optimal electrical performance for the multiplexed interface. This behavior may depend on various factors:

- Section 18.4.12.9.9, *Device Interfaces Signal Group Controls Mapping*, describes the different interfaces that have DS0 impedance mode control and the pad corresponding software control registers.
- The *Electrical Characteristics/DC Electrical Characteristics* section of the device data manual provides more information about the specific DS0 bit settings applicable to these interfaces multiplexed to I/O pads with configurable impedance mode.

A process-only compensation using 4-bit binary coded schema is used separately for pullup/down output parameter variations. Only MODE1 and MODE2 use eFuse process-only compensation to reduce spread in timing parameters. The I/Os with DS0 impedance mode control share the same compensation settings with the I/Os with combined mode and load controls (both type 1 and type 2) and with the C2CI/O buffers. They are exported from eFuse upon POR to the following bits in the CONTROL_EFUSE_2 register:

CONTROL_EFUSE_2[31] EFUSE_SMART2TEST_P0 through CONTROL_EFUSE_2[28] EFUSE_SMART2TEST_P3 (pullup output parameters trimming)

CONTROL_EFUSE_2[27] EFUSE_SMART2TEST_N0 through CONTROL_EFUSE_2[24] EFUSE_SMART2TEST_N3 (pulldown output parameters trimming)

18.4.12.9.6 C2CI/O Cells With Load Setting Adjustable According to Interface Requirement Voltage Mode

To configure this type of I/O cell for different interfaces multiplexed on it, the user must manipulate in software a single bit, LB0, depending on type of multiplexed interface (C2C, GPMC, or SDMMC2) of the pad and the selected I/O voltage supply mode. Like LPDDR2IO, this I/O cell is provided with selectable LVCMOS and Vref-based receiver option. A vref pad is provided to supply reference voltage to the receiver in the 1.2-V mode. To save power at lower frequency operation, the LVCMOS receiver can be selected, and 2 bits, for each of the two C2C pad groups, are used to enable/disable the LVCMOS receiver (CMOSEN_C2C_FRM_CTRL) manually in the CONTROL_C2CIO_PADCONF_0 register.

The pads featuring C2C I/O cells with load setting adjustable according to interface requirement/voltage mode require different LB0 bit settings to achieve optimal electrical performance for the multiplexed interface. This behavior may depend on various factors:

- Section 18.4.12.9.9, *Device Interfaces Signal Group Controls Mapping*, describes the different interfaces that have the interface type versus voltage mode control (LB0) and the pad corresponding software control registers.
- The *Electrical Characteristics/DC Electrical Characteristics* section of the device data manual provides more information about the specific LB0 bit settings applicable to these interfaces multiplexed to I/O pads with configurable impedance mode.

NOTE: No bits are assigned to control the output drive capability of the internal C2C Vref generator (at the c2c_vref pad). It is fixed to a 2-µA current load.

If 1.2-V voltage mode is selected, the user can choose to have the LVCMOS receiver or Vref-based receiver on the C2C I/O cell pads. For the description of the dual-voltage mode settings of the C2C I/O cell pads, see Section 18.4.12.10, *Dual Voltage-Supplied Peripheral Controls*.

In Vref-based receiver mode, the C2C I/O cell receiver is a true differential comparator with pad connected to the positive terminal and VREF tied to the negative terminal. The Vref-based receiver allows the improvement of speed performance at VDDS = 1.2-V I/O voltage supply.

NOTE: The Vref-based receiver is not supported in 1.8-V mode. In this mode, the LVCMOS receiver is the only option.

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NOTE: While at VDDS = 1.2 V, the LVCMOS receiver is supported for all C2C I/O cell pads. The Vref-based receiver is supported on only some of these pads.

The CONTROL_C2CIO_PADCONF_0[12] CMOSEN_C2C_0_FRM_CTRL and CONTROL_C2CIO_PADCONF_0[11] CMOSEN_C2C_1_FRM_CTRL bits, each related to a separate group of pads, are dedicated to select Vref-based receiver mode or LVCMOS receiver mode when VDDS = 1.2 V is selected in the CONTROL_CORE_PADCONF_MODE register.

CMOSEN_C2C_0_FRM_CTRL = 1 enables the 1.2-V mode LVCMOS receiver, and CMOSEN_C2C_0_FRM_CTRL = 0 enables the 1.2-V Vref-based receiver for the following pads:

- gpmc_ad8–gpmc_ad15
- gpmc_ncs4
- gpmc_ncs5

CMOSEN_C2C_1_FRM_CTRL = 1 enables the 1.2-V mode LVCMOS receiver and CMOSEN_C2C_1_FRM_CTRL= 0 enables the 1.2-V Vref-based receiver for the following pads:

- gpmc_a16–gpmc_a23

NOTE: The Vref-based receiver in 1.2-V mode is not supported for the following C2C I/O cell pads:

- gpmc_ad0–gpmc_ad7
- gpmc_a24
- gpmc_a25
- gpmc_ncs0–gpmc_ncs3
- gpmc_clk
- gpmc_nadv_ale
- gpmc_noe
- gpmc_nwe
- gpmc_nbe0_cle
- gpmc_nbe1
- gpmc_wait1
- gpmc_wait2
- gpmc_ncs6
- gpmc_ncs7

When the internal Vref generator is turned on, it supplies voltage reference to the Vref-based receivers supported for some C2C I/O cell pads and can also be used to drive external modules with 1.2-V reference. In this case, the c2c_vref device pad outputs voltage of the internal C2C Vref cell.

Setting bit CONTROL_C2CIO_PADCONF_0[7] C2C_INT_VREF_AUTO_EN = 0b1 enables the automatic shut off or switch-on of the internal Vref cell generator.

If user software sets the manual control bit CONTROL_C2CIO_PADCONF_0[8] C2C_INT_VREF_EN = 0b1, the internal Vref cell generator is enabled, regardless of the state of the CONTROL_C2CIO_PADCONF_0[7] C2C_INT_VREF_AUTO_EN bit. Thus, automatic control over the C2C Vref cell generator can always be overridden in the context of enabling the Vref generator.

If the Vref cell generator is enabled, the c2c_vref pad acts as output and can be used to supply reference voltage to external devices.

NOTE: At VDDS = 1.8-V voltage mode, the internal reference generator is shut off and the internal Vref cell reference node is connected to 0.

For the description of the dual-voltage mode settings of the C2C I/O cell pads, see Section 18.4.12.10, *Dual Voltage-Supplied Peripheral Controls*.

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CAUTION

While using the Vref cell in internal reference mode, nothing else must drive the pad externally, although the pad can be connected to supply the Vref signal to other devices.

When the internal Vref cell generator is disabled and bypassed, which is provided when bits CONTROL_C2CIO_PADCONF_0[8] C2C_INT_VREF_EN = 0b0 and CONTROL_C2CIO_PADCONF_0[7] C2C_INT_VREF_AUTO_EN = 0b0, the c2c_vref pad acts as input that can supply voltage reference to the Vref-based receivers from external sources.

Table 18-71 provides different combinations of Vref cell control types, the state of the Vref cell, and the associated voltage reference pad direction.

Table 18-71. C2C Vref Cell State Description

C2C_INT_VREF_EN (Manual Control Bits)	C2C_INT_VREF_AUTO_EN (AUTO Control Bits)	Type of Control	Vref Cell State	Voltage Reference Pad Direction
1	x	Manual	Enabled	O
0	1	AUTO	Automatically enabled/disabled	O
0	0	–	Disabled and bypassed	I

CAUTION

The c2c_vref pad must be externally driven only in 1.2-V voltage mode.

According to the noise environment, the user can select to filter the reference voltage, which is supplied at the internal VREF node (receiver comparators Vref input) by the Vref cell generator or by an external source. Two coupling capacitors, internal to the C2C Vref cell, are available at the internal VREF node, which is configurable as specified in Table 18-72.

Table 18-72. C2C Vref Cell Decoupling Cap Selection

VREF_CCAP0	VREF_CCAP1	Capacitor
0	0	No capacitor connected
0	1	Capacitor between internal reference node and VDDS
1	0	Capacitor between internal reference node and VSS
1	1	Capacitor between internal reference node and VDDS as well as internal reference node and VSS

A process-only compensation using a 4-bit binary-coded schema is used separately for pullup/down output parameter variations. The C2CI/O buffers share the same compensation settings with the I/Os with combined mode and load controls (both with 25- and 50-Ω output) and I/Os with driver output impedance (DS) settings. They are exported from eFuse upon POR to the following bits in the CONTROL_EFUSE_2 register:

CONTROL_EFUSE_2[31] EFUSE_SMART2TEST_P0 through CONTROL_EFUSE_2[28] EFUSE_SMART2TEST_P3 (pullup output parameters trimming)

CONTROL_EFUSE_2[27] EFUSE_SMART2TEST_N0 through CONTROL_EFUSE_2[24] EFUSE_SMART2TEST_N3 (pulldown output parameters trimming)

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18.4.12.9.7 SDMMC1 Pullup Strength Control

The SDMMC1_PUSTRENGTH_GRPi (where i = 1 to 3) control bits are added in the CONTROL_MMC1 register to program the pullup strength for the MMC/SD/SDIO1 I/Os group.

- Section 18.4.12.9.9, *Device Interfaces Signal Group Controls Mapping*, describes the different interfaces that have the pullup strength control and the pad corresponding software control registers.
- The *Electrical Characteristics/DC Electrical Characteristics* section of the device data manual provides more information about the specific pullup strength settings applicable to these interfaces multiplexed to I/O pads with configurable pullup strength.

18.4.12.9.8 I2Cx I/Os Group Pullupresx Controls and Load Range Settings

The I2Cx buffer contains internal pullup resistors for F/S and HS modes. LB[1:0] bits are used to select an appropriate pullup resistor for a given load range.

The active high GLFENB[0] bit is implemented for I^2C receivers to enable glitch-free operation.

NOTE: The pullup versus load settings applicable to I2Cx FS mode also apply to I2Cx standard speed mode.

The type of the pullup resistor (external or internal) for a certain I2Cx I/O group (where x = 1 to 4) is selected through the I2Cx_SCL_PULLUPRESX and I2Cx_SDA_PULLUPRESX bits. Internal pullups are activated when I2Cx_SCL_PULLUPRESX / I2Cx_SDA_PULLUPRESX =0b0.

I^2C functionality is not ensured if the weak internal pullup or pulldown is activated on any of the I/Os connected to the bus.

NOTE: The user must set PULLUDENABLE = 0b0 in the I2Cx padconf registers (disable internal weak pullup resistors on i2cx pads) to ensure the full I/O cell performance capabilities of the I^2C.

The I^2C pads require different LB[1:0] and GLFENB[0] bit field settings to achieve optimal electrical performance for the multiplexed (in MuxMode = 0x0) I^2C signals. This behavior may depend on various factors:

- Section 18.4.12.9.9, *Device Interfaces Signal Group Controls Mapping*, describes the I^2C pads and their corresponding software control registers.
- The *Electrical Characteristics/DC Electrical Characteristics/I^2C DC Electrical Characteristics* section of the device data manual provides more information about the specific LB[1:0] and GLFENB[0] bit settings applicable to I^2C I/O pads.

18.4.12.9.9 Device Interfaces Signal Group Controls Mapping

Table 18-73 through Table 18-100 describe the mapping of the signal integrity control bit fields in the different signal integrity control registers described in Table 18-66.

NOTE: The same I/O cell and I/O cell controls assigned to a pad signal available when Muxmode = 0 are shared between signals available on the same pad when Muxmode is selected different than 0. For more information, see Section 18.4.8.3, *Pad Multiplexing Register Fields*.

Table 18-73. EMIF (LPDDR2IO) Signal Group Parameter Controls to Different Interface I/O Pads Mapping

EMIF (LPDDR2IO) Interface I/O Controls		
Bit Fields for Pad Group Controls	**Pads (Muxmode = 0) in Group**	**Type of I/O Group-Associated Control Bit Fields**
CONTROL_LPDDR2IO1_0[31:30] LPDDR2IO1_GR4_SR	lpddr21_dq24– lpddr21_dq31; lpddr21_dm3	HS I/O buffers with impedance (I), slew rate(SR), and weak driver settings (WD)

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Table 18-73. EMIF (LPDDR2IO) Signal Group Parameter Controls to Different Interface I/O Pads Mapping (continued)

EMIF (LPDDR2IO) Interface I/O Controls		
Bit Fields for Pad Group Controls	**Pads (Muxmode = 0) in Group**	**Type of I/O Group-Associated Control Bit Fields**
CONTROL_LPDDR2IO1_0[29:27] LPDDR2IO1_GR4_I CONTROL_LPDDR2IO1_0[26:25] LPDDR2IO1_GR4_WD		(See Section 18.4.12.9.2 for more information.)
CONTROL_LPDDR2IO1_0[23:22] LPDDR2IO1_GR3_SR CONTROL_LPDDR2IO1_0[21:19] LPDDR2IO1_GR3_I CONTROL_LPDDR2IO1_0[18:17] LPDDR2IO1_GR3_WD	lpddr21_dq16–lpddr21_dq23; lpddr21_dm2	
CONTROL_LPDDR2IO1_0[15:14] LPDDR2IO1_GR2_SR CONTROL_LPDDR2IO1_0[13:11] LPDDR2IO1_GR2_I CONTROL_LPDDR2IO1_0[10:9] LPDDR2IO1_GR2_WD	lpddr21_dq8– lpddr21_dq15; lpddr21_dm1	
CONTROL_LPDDR2IO1_0[7:6] LPDDR2IO1_GR1_SR CONTROL_LPDDR2IO1_0[5:3] LPDDR2IO1_GR1_I CONTROL_LPDDR2IO1_0[2:1] LPDDR2IO1_GR1_WD	lpddr21_dq0–lpddr21_dq7; lpddr21_dm0	
CONTROL_LPDDR2IO1_1[31:30] LPDDR2IO1_GR8_SR CONTROL_LPDDR2IO1_1[29:27] LPDDR2IO1_GR8_I CONTROL_LPDDR2IO1_1[26:25] LPDDR2IO1_GR8_WD	lpddr21_dqs2; lpddr21_ndqs2	
CONTROL_LPDDR2IO1_1[23:22] LPDDR2IO1_GR7_SR CONTROL_LPDDR2IO1_1[21:19] LPDDR2IO1_GR7_I CONTROL_LPDDR2IO1_1[18:17] LPDDR2IO1_GR7_WD	lpddr21_dqs1; lpddr21_ndqs1	
CONTROL_LPDDR2IO1_1[15:14] LPDDR2IO1_GR6_SR CONTROL_LPDDR2IO1_1[13:11] LPDDR2IO1_GR6_I CONTROL_LPDDR2IO1_1[10:9] LPDDR2IO1_GR6_WD	lpddr21_dqs0; lpddr21_ndqs0	
CONTROL_LPDDR2IO1_1[7:6] LPDDR2IO1_GR5_SR CONTROL_LPDDR2IO1_1[5:3] LPDDR2IO1_GR5_I CONTROL_LPDDR2IO1_1[2:1] LPDDR2IO1_GR5_WD	lpddr21_ca0–lpddr21_ca9	
CONTROL_LPDDR2IO1_2[31:30] LPDDR2IO1_GR11_SR CONTROL_LPDDR2IO1_2[29:27] LPDDR2IO1_GR11_I CONTROL_LPDDR2IO1_2[26:25] LPDDR2IO1_GR11_WD	lpddr21_ncs0; lpddr21_ncs1; lpddr21_cke0; lpddr21_cke1	

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Table 18-73. EMIF (LPDDR2IO) Signal Group Parameter Controls to Different Interface I/O Pads Mapping (continued)

EMIF (LPDDR2IO) Interface I/O Controls		
Bit Fields for Pad Group Controls	**Pads (Muxmode = 0) in Group**	**Type of I/O Group-Associated Control Bit Fields**
CONTROL_LPDDR2IO1_2[23:22] LPDDR2IO1_GR10_SR CONTROL_LPDDR2IO1_2[21:19] LPDDR2IO1_GR10_I CONTROL_LPDDR2IO1_2[18:17] LPDDR2IO1_GR10_WD	lpddr21_ck; lpddr21_nck	HS I/O buffers with impedance (I), slew rate(SR), and weak driver settings (WD) (See Section 18.4.12.9.2 for more information.)
CONTROL_LPDDR2IO1_2[15:14] LPDDR2IO1_GR9_SR	lpddr21_dqs3; lpddr21_ndqs3	
CONTROL_LPDDR2IO1_2[13:11] LPDDR2IO1_GR9_I		
CONTROL_LPDDR2IO1_2[10:9] LPDDR2IO1_GR9_WD		
CONTROL_LPDDR2IO2_0[31:30] LPDDR2IO2_GR4_SR CONTROL_LPDDR2IO2_0[29:27] LPDDR2IO2_GR4_I CONTROL_LPDDR2IO2_0[26:25] LPDDR2IO2_GR4_WD	lpddr22_dq24–lpddr22_dq31; lpddr22_dm3	
CONTROL_LPDDR2IO2_0[23:22] LPDDR2IO2_GR3_SR CONTROL_LPDDR2IO2_0[21:19] LPDDR2IO2_GR3_I CONTROL_LPDDR2IO2_0[18:17] LPDDR2IO2_GR3_WD	lpddr22_dq16–lpddr22_dq23; lpddr22_dm2	
CONTROL_LPDDR2IO2_0[15:14] LPDDR2IO2_GR2_SR CONTROL_LPDDR2IO2_0[13:11] LPDDR2IO2_GR2_I CONTROL_LPDDR2IO2_0[10:9] LPDDR2IO2_GR2_WD	lpddr22_dq8–lpddr22_dq15; lpddr22_dm1	
CONTROL_LPDDR2IO2_0[7:6] LPDDR2IO2_GR1_SR CONTROL_LPDDR2IO2_0[5:3] LPDDR2IO2_GR1_I CONTROL_LPDDR2IO2_0[2:1] LPDDR2IO2_GR1_WD	lpddr22_dq0–lpddr22_dq7; lpddr22_dm0	
CONTROL_LPDDR2IO2_1[31:30] LPDDR2IO2_GR8_SR CONTROL_LPDDR2IO2_1[29:27] LPDDR2IO2_GR8_I CONTROL_LPDDR2IO2_1[26:25] LPDDR2IO2_GR8_WD	lpddr22_dqs2; lpddr22_ndqs2	
CONTROL_LPDDR2IO2_1[23:22] LPDDR2IO2_GR7_SR CONTROL_LPDDR2IO2_1[21:19] LPDDR2IO2_GR7_I CONTROL_LPDDR2IO2_1[18:17] LPDDR2IO2_GR7_WD	lpddr22_dqs1; lpddr22_ndqs1	
CONTROL_LPDDR2IO2_1[15:14] LPDDR2IO2_GR6_SR CONTROL_LPDDR2IO2_1[13:11] LPDDR2IO2_GR6_I	lpddr22_dqs0; lpddr22_ndqs0	

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Table 18-73. EMIF (LPDDR2IO) Signal Group Parameter Controls to Different Interface I/O Pads Mapping (continued)

EMIF (LPDDR2IO) Interface I/O Controls		
Bit Fields for Pad Group Controls	**Pads (Muxmode = 0) in Group**	**Type of I/O Group-Associated Control Bit Fields**
CONTROL_LPDDR2IO2_1[10:9] LPDDR2IO2_GR6_WD		
CONTROL_LPDDR2IO2_1[7:6] LPDDR2IO2_GR5_SR CONTROL_LPDDR2IO2_1[5:3] LPDDR2IO2_GR5_I CONTROL_LPDDR2IO2_1[2:1] LPDDR2IO2_GR5_WD	lpddr22_ca0–lpddr22_ca9	
CONTROL_LPDDR2IO2_2[31:30] LPDDR2IO2_GR11_SR CONTROL_LPDDR2IO2_2[29:27] LPDDR2IO2_GR11_I CONTROL_LPDDR2IO2_2[26:25] LPDDR2IO2_GR11_WD	lpddr22_ncs0; lpddr22_ncs1; lpddr22_cke0; lpddr22_cke1	HS I/O buffers with impedance (I), slew rate(SR), and weak driver settings (WD) (See Section 18.4.12.9.2 for more information.)
CONTROL_LPDDR2IO2_2[23:22] LPDDR2IO2_GR10_SR CONTROL_LPDDR2IO2_2[21:19] LPDDR2IO2_GR10_I CONTROL_LPDDR2IO2_2[18:17] LPDDR2IO2_GR10_WD	lpddr22_ck; lpddr22_nck	
CONTROL_LPDDR2IO2_2[15:14] LPDDR2IO2_GR9_SR CONTROL_LPDDR2IO2_2[13:11] LPDDR2IO2_GR9_I CONTROL_LPDDR2IO2_2[10:9] LPDDR2IO2_GR9_WD	lpddr22_dqs3; lpddr22_ndqs3	

Table 18-74. GPMC I/O Signal Group Parameter Controls to Different Interface I/O Pads Mapping

GPMC interface I/O Controls		
Bit Fields for Pad Group Controls	**Pads (Muxmode = 0) in Group**	**Type of I/O Group-Associated Control Bit Fields**
CONTROL_C2CIO_PADCONF_0[13] SDMMC2_DR0_LB0	gpmc_ad0–gpmc_ad7; gpmc_noe; gpmc_nwe	C2CIO cell I/Os with single-LB0 control (See Section 18.4.12.9.6 for more information.)
CONTROL_C2CIO_PADCONF_0[28] GPIO_DR0_LB0	gpmc_ad8–gpmc_ad11	
CONTROL_C2CIO_PADCONF_0[15] KPD_DR4_LB0	gpmc_ad12–gpmc_ad15	
CONTROL_C2CIO_PADCONF_0[27] GPIO_DR1_LB0	gpmc_a16–gpmc_a19	
CONTROL_C2CIO_PADCONF_0[14] KPD_DR5_LB0	gpmc_a20–gpmc_a23	
CONTROL_C2CIO_PADCONF_0[26] GPIO_DR2_LB0	gpmc_a24 ; gpmc_nbe0_cle	
CONTROL_C2CIO_PADCONF_0[17] GPMC_DR8_LB0	gpmc_a25	C2CIO cell I/Os with single-LB0 control (See Section 18.4.12.9.6 for more information.)
CONTROL_C2CIO_PADCONF_0[25] GPMC_DR0_LB0	gpmc_ncs0	
CONTROL_C2CIO_PADCONF_0[31] C2C_DR0_LB0	gpmc_ncs1	

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Table 18-74. GPMC I/O Signal Group Parameter Controls to Different Interface I/O Pads Mapping (continued)

GPMC interface I/O Controls		
Bit Fields for Pad Group Controls	**Pads (Muxmode = 0) in Group**	**Type of I/O Group-Associated Control Bit Fields**
CONTROL_C2CIO_PADCONF_0[16] GPMC_DR9_LB0	gpmc_ncs2	
CONTROL_C2CIO_PADCONF_0[23] GPMC_DR10_LB0	gpmc_ncs3	
CONTROL_SMART3IO_PADCONF_1[13:12] GPMC_DR1_MB; CONTROL_SMART3IO_PADCONF_2[8] GPMC_DR1_LB	gpmc_nwp	Type 2 I/Os with MB[1:0] + LB[0] settings (for more information, see Section 18.4.12.9.4, *I/Os With Combined Mode and Load Settings*)
CONTROL_C2CIO_PADCONF_0[24] GPMC_DR11_LB0	gpmc_nadv_ale	C2CIO cell I/Os with single-LB0 control (See Section 18.4.12.9.6 for more information.)
CONTROL_C2CIO_PADCONF_0[20] GPMC_DR5_LB0	gpmc_clk	
CONTROL_C2CIO_PADCONF_0[21] GPMC_DR4_LB0	gpmc_nbe1	
CONTROL_SMART1IO_PADCONF_0[17:16] GPMC_DR3_SC CONTROL_SMART1IO_PADCONF_1[17:16] GPMC_DR3_LB	gpmc_wait0	Low speed I/Os LB[1: 0] + SC[1:0] controls (See Section 18.4.12.9.3 for more information.)
CONTROL_C2CIO_PADCONF_0[22] GPMC_DR2_LB0	gpmc_wait1	C2CIO cell I/Os with single-LB0 control (See Section 18.4.12.9.6 for more information.)
CONTROL_C2CIO_PADCONF_0[19] GPMC_DR6_LB0	gpmc_wait2	
CONTROL_C2CIO_PADCONF_0[18] GPMC_DR7_LB0	gpmc_ncs4, gpmc_ncs5	
CONTROL_C2CIO_PADCONF_0[30] C2C_DR1_LB0	gpmc_ncs6	
CONTROL_C2CIO_PADCONF_0[29] C2C_DR2_LB0	gpmc_ncs7	

Table 18-75. CAMERA I/O Signal Group Parameter Controls to Different Interface I/O Pads Mapping

CAMERA Interface I/O Controls		
Bit Fields for Pad Group Controls	**Pads (Muxmode = 0) in Group**	**Type of I/O Group-Associated Control Bit Fields**
CONTROL_SMART1IO_PADCONF_0[29:28] CAM_DR0_SC CONTROL_SMART1IO_PADCONF_1[29:28] CAM_DR0_LB	cam_shutter; cam_strobe; cam_globalreset	Low speed I/Os LB[1: 0]+SC[1:0] controls, (See Section 18.4.12.9.3 for more information.)

Table 18-76. USBB1 I/O Signal Group Parameter Controls to Different Interface I/O Pads Mapping

USBB1 Interface I/O Controls		
Bit Fields for Pad Group Controls	**Pads (Muxmode = 0) in Group**	**Type of I/O Group-Associated Control Bit Fields**
CONTROL_SMART2IO_PADCONF_2[11] USBB1_DR0_DS	usbb1_ulpitll_clk	I/O cell with single-bit drive strength (DS) control for driver output impedance (See Section 18.4.12.9.5 for more information.)

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Table 18-76. USBB1 I/O Signal Group Parameter Controls to Different Interface I/O Pads Mapping (continued)

USBB1 Interface I/O Controls		
Bit Fields for Pad Group Controls	**Pads (Muxmode = 0) in Group**	**Type of I/O Group-Associated Control Bit Fields**
CONTROL_SMART3IO_PADCONF_1[21:20] HSI_DR0_MB CONTROL_SMART3IO_PADCONF_2[10] HSI_DR0_LB	usbb1_ulpitll_stp	Type 1 I/Os with MB[1:0] + LB[0] settings (for more information, see Section 18.4.12.9.4, *I/Os With Combined Mode and Load Settings*)
CONTROL_SMART3IO_PADCONF_1[1:0] USBB1_DR2_MB CONTROL_SMART3IO_PADCONF_2[4] USBB1_DR2_LB	usbb1_ulpitll_dir	
CONTROL_SMART3IO_PADCONF_0[21:20] HSI_DR1_MB CONTROL_SMART3IO_PADCONF_2[26] HSI_DR1_LB	usbb1_ulpitll_nxt; usbb1_ulpitll_dat0	
CONTROL_SMART3IO_PADCONF_0[19:18] HSI_DR2_MB CONTROL_SMART3IO_PADCONF_2[25] HSI_DR2_LB	usbb1_ulpitll_dat1; usbb1_ulpitll_dat2	
CONTROL_SMART3IO_PADCONF_0[17:16] HSI_DR3_MB CONTROL_SMART3IO_PADCONF_2[24] HSI_DR3_LB	usbb1_ulpitll_dat3	
CONTROL_SMART3IO_PADCONF_0[29:28] GPIO_DR3_MB CONTROL_SMART3IO_PADCONF_2[30] GPIO_DR3_LB	usbb1_ulpitll_dat4; usbb1_ulpitll_dat5	
CONTROL_SMART3IO_PADCONF_0[27:26] GPIO_DR4_MB CONTROL_SMART3IO_PADCONF_2[29] GPIO_DR4_LB	usbb1_ulpitll_dat6; usbb1_ulpitll_dat7	
CONTROL_USBB _HSIC[26:25] USBB1_DR1_SR CONTROL_USBB _HSIC[24:22] USBB1_DR1_I CONTROL_USBB _HSIC[21:20] USBB1_HSIC_DATA_WD CONTROL_USBB _HSIC[13] USBB1_HSIC_DATA_OFFMODE_WD_ENABLE CONTROL_USBB _HSIC[12:11] USBB1_HSIC_DATA_OFFMODE_WD CONTROL_USBB _HSIC[19:18] USBB1_HSIC_STROBE_WD CONTROL_USBB _HSIC[10] USBB1_HSIC_STROBE_OFFMODE_WD_ENABLE CONTROL_USBB _HSIC[9:8] USBB1_HSIC_STROBE_OFFMODE_WD	usbb1_hsic _data; usbb1_hsic_strobe	HS I/O buffers with impedance (I), slew rate(SR), and weak driver (WD) settings (See Section 18.4.12.9.2 for more information.)

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Table 18-77. USBB2 I/O Signal Group Parameter Controls to Different Interface I/O Pads Mapping

USBB2 Interface I/O Controls		
Bit Fields for Pad Group Controls	**Pads(Muxmode = 0) in Group**	**Type of I/O Group-Associated Control Bit Fields**
CONTROL_SMART2IO_PADCONF_2[12] USBB2_DR0_DS	usbb2_ulpitll_clk	I/O cell with single-bit drive strength (DS) control for driver output impedance (See Section 18.4.12.9.5 for more information.)
CONTROL_SMART2IO_PADCONF_2[23] SDMMC4_DR0_DS	usbb2_ulpitll_stp; usbb2_ulpitll_dir	
CONTROL_SMART2IO_PADCONF_2[27] HSI2_DR0_DS	usbb2_ulpitll_nxt; usbb2_ulpitll_dat0	
CONTROL_SMART2IO_PADCONF_2[22] SDMMC4_DR1_DS	usbb2_ulpitll_dat1	
CONTROL_SMART2IO_PADCONF_2[26] HSI2_DR1_DS	usbb2_ulpitll_dat2	
CONTROL_SMART2IO_PADCONF_2[25] HSI2_DR2_DS	usbb2_ulpitll_dat3	
CONTROL_SMART2IO_PADCONF_2[24] SDMMC3_DR0_DS	usbb2_ulpitll_dat4	
CONTROL_SMART2IO_PADCONF_2[20] SPI3_DR1_DS	usbb2_ulpitll_dat5	
CONTROL_SMART2IO_PADCONF_2[21] SPI3_DR0_DS	usbb2_ulpitll_dat6; usbb2_ulpitll_dat7	
CONTROL_USBB _HSIC[31:30] USBB2_DR1_SR CONTROL_USBB _HSIC[29:27] USBB2_DR1_I CONTROL_USBB _HSIC[17:16] USBB2_HSIC_DATA_WD CONTROL_USBB _HSI [7] USBB2_HSIC_DATA_OFFMODE_WD_ENABLE CONTROL_USBB _HSIC[6:5] USBB2_HSIC_DATA_OFFMODE_WD CONTROL_USBB _HSIC[15:14] USBB2_HSIC_STROBE_WD CONTROL_USBB _HSIC[4] USBB2_HSIC_STROBE_OFFMODE_WD_ENABLE CONTROL_USBB _HSIC[3:2] USBB2_HSIC_STROBE_OFFMODE_WD	usbb2_hsic _data; usbb2_hsic_strobe	HS I/O buffers with impedance (I), slew rate(SR), and weak driver (WD) settings (See Section 18.4.12.9.2 for more information.)

Table 18-78. USBC1 I/O Signal Group Parameter Controls to Different Interface I/O Pads Mapping

USBC1 Interface I/O Controls		
Bit Fields for Pad Group Controls	**Pads (Muxmode = 0) in Group**	**Type of I/O Group-Associated Control Bit Fields**
CONTROL_PBIASLITE[20] USBC1_ICUSB_PWRDNZ	usbc1_icusb_dp; usbc1_icusb_dm	Power-down mode for gpio_wk pads associated extended-drain I/O cell + speed control. PUSTRENGTH control is hardware tied to 0 – (50k–110k).
CONTROL_MMC1[24] USBC1_DR0_SPEEDCTRL		Speed control for the usbc1 I/Os. See Table 18-14 for more information.

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Table 18-79. KEYPAD I/O Signal Group Parameter Controls to Different Interface I/O Pads Mapping

KEYPAD Interface I/O Controls		
Bit Fields for Pad Group Controls	**Pads (Muxmode = 0) in Group**	**Type of I/O Group-Associated Control Bit Fields**
CONTROL_SMART1IO_PADCONF_2[31:30] KPD_DR0_SC CONTROL_SMART1IO_PADCONF_3[31:30] KPD_DR0_LB	kpd_col3; kpd_col4; kpd_col5	Low speed I/Os LB[1: 0] + SC[1:0] controls (See Section 18.4.12.9.3 for more information.)
CONTROL_SMART1IO_PADCONF_2[29:28] KPD_DR1_SC CONTROL_SMART1IO_PADCONF_3[29:28] KPD_DR1_LB	kpd_col0; kpd_col1; kpd_col2	
CONTROL_SMART1IO_PADCONF_2[27:26] KPD_DR2_SC CONTROL_SMART1IO_PADCONF_3[27:26] KPD_DR2_LB	kpd_row3; kpd_row4; kpd_row5	
CONTROL_SMART1IO_PADCONF_2[25:24] KPD_DR3_SC CONTROL_SMART1IO_PADCONF_3[25:24] KPD_DR3_LB	kpd_row0; kpd_row1; kpd_row2	

Table 18-80. HDQ I/O Signal Group Parameter Controls to Different Interface I/O Pads Mapping

HDQ Interface I/O Controls		
Bit Fields for Pad Group Controls	**Pads (Muxmode = 0) in Group**	**Type of I/O Group-Associated Control Bit Fields**
CONTROL_SMART1IO_PADCONF_2[23:22] HDQ_DR0_SC CONTROL_SMART1IO_PADCONF_3[23:22] HDQ_DR0_LB	hdq_sio	Low speed I/Os LB[1: 0] + SC[1:0] controls (See Section 18.4.12.9.3 for more information.)

Table 18-81. GPIO Signal Group Parameter Controls to Different Interface I/O Pads Mapping

GPIO Interface I/O Controls		
Bit Fields for Pad Group Controls	**Signals (Muxmode = 3) in Group**	**Type of I/O Group-Associated Control Bit Fields**
CONTROL_SMART1NOPMIO_PADCONF_0 [13:12] GPIOWK4_DR0_SC CONTROL_SMART1NOPMIO_PADCONF_1 [13:12] GPIOWK4_DR0_LB	gpio_wk4	Low speed I/Os LB[1: 0] + SC[1:0] controls (See Section 18.4.12.9.3 for more information.)
CONTROL_SMART1IO_PADCONF_0[13:12] GPIO_63_64_DR0_SC CONTROL_SMART1IO_PADCONF_1[13:12] GPIO_63_64_DR0_LB	gpio_63 - gpio_64	Low speed I/Os LB[1: 0] + SC[1:0] controls (See Section 18.4.12.9.3 for more information.)

Table 18-82. SDMMC1 Signal Group Parameter Controls to Different Interface I/O Pads Mapping

SDMMC1 Interface I/O Controls		
Bit Fields for Pad Group Controls	**Pads (Muxmode = 0) in Group**	**Type of I/O Group-Associated Control Bit Fields**
CONTROL_MMC1[31] SDMMC1_PUSTRENGTH_GRP0	sdmmc1_clk	Pad pullup strength control. See Section 18.4.12.9.7 , Section 18.4.9.2 and Section 18.5.1.2.2 for more details.
CONTROL_MMC1[27] SDMMC1_DR0_SPEEDCTRL		Pad speed control. See Section 18.4.9.2 and Section 18.5.1.2.2 for more details.

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Table 18-82. SDMMC1 Signal Group Parameter Controls to Different Interface I/O Pads Mapping (continued)

SDMMC1 Interface I/O Controls		
Bit Fields for Pad Group Controls	**Pads (Muxmode = 0) in Group**	**Type of I/O Group-Associated Control Bit Fields**
CONTROL_MMC1[30] SDMMC1_PUSTRENGTH_GRP1	sdmmc1_cmd	Pad pullup strength control. For more information, see Section 18.4.12.9.7 , Section 18.4.9.2, and Section 18.5.1.2.2.
CONTROL_MMC1[27] SDMMC1_DR0_SPEEDCTRL		Pad speed control. For more information, see Section 18.4.9.2 and Section 18.5.1.2.2.
CONTROL_MMC1[29] SDMMC1_PUSTRENGTH_GRP2	sdmmc1_dat0; sdmmc1_dat1	Pad pullup strength control. For more information, see Section 18.4.12.9.7 , Section 18.4.9.2, and Section 18.5.1.2.2 .
CONTROL_MMC1[27] SDMMC1_DR0_SPEEDCTRL		Pad speed control. For more information, see Section 18.4.9.2 and Section 18.5.1.2.2.
CONTROL_MMC1[29] SDMMC1_PUSTRENGTH_GRP2	sdmmc1_dat2; sdmmc1_dat3	Pad pullup strength control. For more information, see Section 18.4.12.9.7 , Section 18.4.9.2, and Section 18.5.1.2.2.
CONTROL_MMC1[25] SDMMC1_DR2_SPEEDCTRL		Pad speed control. For more information, see Section 18.4.9.2 and Section 18.5.1.2.2.
CONTROL_MMC1[28] SDMMC1_PUSTRENGTH_GRP3	sdmmc1_dat4 - sdmmc1_dat7	Pad pullup strength control. For more information, see Section 18.4.12.9.7 , Section 18.4.9.2, and Section 18.5.1.2.2.
CONTROL_MMC1[26] SDMMC1_DR1_SPEEDCTRL		Pad speed control. For more information, see Section 18.4.9.2 and Section 18.5.1.2.2.

Table 18-83. SDMMC5 Signal Group Parameter Controls to Different Interface I/O Pads Mapping

SDMMC5 Interface I/O Controls		
Bit Fields for Pad Group Controls	**Pads (Muxmode=0) in Group**	**Type of I/O Group-Associated Control Bit Fields**
CONTROL_SMART3IO_PADCONF_1[31:30] SPI2_DR1_MB CONTROL_SMART3IO_PADCONF_2[15] SPI2_DR1_LB	sdmmc5_clk; sdmmc5_cmd; sdmmc5_dat0	Type 2 I/Os with MB[1:0] + LB[0] settings (for more information, see Section 18.4.12.9.4, *I/Os With Combined Mode and Load Settings*)
CONTROL_SMART3IO_PADCONF_1[29:28] SPI2_DR2_MB CONTROL_SMART3IO_PADCONF_2[14] SPI2_DR2_LB	sdmmc5_dat1	Type 2 I/Os with MB[1:0] + LB[0] settings (for more information, see Section 18.4.12.9.4, *I/Os With Combined Mode and Load Settings*)
CONTROL_SMART3IO_PADCONF_0[25:24] GPIO_DR5_MB CONTROL_SMART3IO_PADCONF_2[28] GPIO_DR5_LB	sdmmc5_dat2	Type 2 I/Os with MB[1:0] + LB[0] settings (for more information, see Section 18.4.12.9.4, *I/Os With Combined Mode and Load Settings*)
CONTROL_SMART3IO_PADCONF_0[23:22] GPIO_DR6_MB CONTROL_SMART3IO_PADCONF_2[27] GPIO_DR6_LB	sdmmc5_dat3	Type 2 I/Os with MB[1:0] + LB[0] settings (for more information, see Section 18.4.12.9.4, *I/Os With Combined Mode and Load Settings*)

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Table 18-84. ABE McBSP1 Signal Group Parameter Controls to Different Interface I/O Pads Mapping

McBSP1 Interface I/O Controls		
Bit Fields for Pad Group Controls	**Pads (Muxmode = 0) in Group**	**Type of I/O Group-Associated Control Bit Fields**
CONTROL_SMART3IO_PADCONF_3[31:30] SLIMBUS1_DR0_MB CONTROL_SMART3IO_PADCONF_3[19] SLIMBUS1_DR0_LB	abe_mcbsp1_clkx	Type 2 I/Os with MB[1:0] + LB[0] settings (for more information, see Section 18.4.12.9.4, *I/Os With Combined Mode and Load Settings*)
CONTROL_SMART3IO_PADCONF_3[29:28] SLIMBUS1_DR1_MB CONTROL_SMART3IO_PADCONF_3[15] SLIMBUS1_DR1_LB	abe_mcbsp1_dr	
CONTROL_SMART3IO_PADCONF_0[9:8] SDMMC3_DR0_MB CONTROL_SMART3IO_PADCONF_2[5] SDMMC3_DR0_LB	abe_mcbsp1_dx; abe_mcbsp1_fsx	

Table 18-85. ABE McBSP2 Signal Group Parameter Controls to Different Interface I/O Pads Mapping

McBSP2 Interface I/O Controls		
Bit Fields for Pad Group Controls	**Pads (Muxmode = 0) in Group**	**Type of I/O Group-Associated Control Bit Fields**
CONTROL_SMART3IO_PADCONF_0[15:14] MCBSP2_DR0_MB; CONTROL_SMART3IO_PADCONF_2[23] MCBSP2_DR0_LB	abe_mcbsp2_clkx; abe_mcbsp2_dr; abe_mcbsp2_dx	Type 2 I/Os with MB[1:0] + LB[0] settings (for more information, see Section 18.4.12.9.4, *I/Os With Combined Mode and Load Settings*)
CONTROL_SMART3IO_PADCONF_0[1:0] SPI2_DR0_MB CONTROL_SMART3IO_PADCONF_2[16] SPI2_DR0_LB	abe_mcbsp2_fsx	Type 2 I/Os with MB[1:0] + LB[0] settings (for more information, see Section 18.4.12.9.4, *I/Os With Combined Mode and Load Settings*)

Table 18-86. ABE McPDM Signal Group Parameter Controls to Different Interface I/O Pads Mapping

McPDM Interface I/O Controls		
Bit Fields for Pad Group Controls	**Pads (Muxmode = 0) in Group**	**Type of I/O Group-Associated Control Bit Fields**
CONTROL_SMART3IO_PADCONF_1[7:6] PDM_DR0_MB CONTROL_SMART3IO_PADCONF_2[7] PDM_DR0_LB	abe_pdm_ul_data; abe_pdm_dl_data; abe_pdm_frame; abe_pdm_lb_clk	Type 2 I/Os with MB[1:0] + LB[0] settings (for more information, see Section 18.4.12.9.4, *I/Os With Combined Mode and Load Settings*)

Table 18-87. ABE DMIC Signal Group Parameter Controls to Different Interface I/O Pads Mapping

DMIC Interface I/O Controls		
Bit Fields for Pad Group Controls	**Pads (Muxmode = 0) in group**	**Type of I/O Group-Associated Control Bit Fields**
CONTROL_SMART3IO_PADCONF_0[31:30] DMIC_DR0_MB CONTROL_SMART3IO_PADCONF_2[31] DMIC_DR0_LB	abe_dmic_clk1; abe_dmic_din1	Type 2 I/Os with MB[1:0] + LB[0] settings (for more information, see Section 18.4.12.9.4, *I/Os With Combined Mode and Load Settings*)
CONTROL_SMART3IO_PADCONF_3[27:26] SLIMBUS2_DR0_MB CONTROL_SMART3IO_PADCONF_3[14] SLIMBUS2_DR0_LB	abe_dmic_din2	Type 2 I/Os with MB[1:0] + LB[0] settings (for more information, see Section 18.4.12.9.4, *I/Os With Combined Mode and Load Settings*)
CONTROL_SMART3IO_PADCONF_3[23:22] SLIMBUS2_DR2_MB CONTROL_SMART3IO_PADCONF_3[17] SLIMBUS2_DR2_LB	abe_dmic_din3	Type 2 I/Os with MB[1:0] + LB[0] settings (for more information, see Section 18.4.12.9.4, *I/Os With Combined Mode and Load Settings*)

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Table 18-88. ABE Shared Signal Group Parameter Controls to Different Interface I/O Pads Mapping

ABE Modules Shared I/O Controls		
Bit Fields for Pad Group Controls	**Pads (Muxmode = 0) in Group**	**Type of I/O Group-Associated Control Bit Fields**
CONTROL_SMART1IO_PADCONF_0[31:30] ABE_DR0_SC CONTROL_SMART1IO_PADCONF_1[31:30] ABE_DR0_LB	abe_clks	Low-speed I/Os LB[1: 0] + SC[1:0] controls (See Section 18.4.12.9.3 for more information.)

Table 18-89. UART2 Signal Group Parameter Controls to Different Interface I/O Pads Mapping

UART2 Interface I/O Controls		
Bit Fields for Pad Group Controls	**Pads (Muxmode = 0) in Group**	**Type of I/O Group-Associated Control Bit Fields**
CONTROL_SMART3IO_PADCONF_1[27:26] UART2_DR0_MB CONTROL_SMART3IO_PADCONF_2[13] UART2_DR0_LB	uart2_cts; uart2_rts; uart2_rx	Type 2 I/Os with MB[1:0] + LB[0] settings (for more information, see Section 18.4.12.9.4, *I/Os With Combined Mode and Load Settings*)
CONTROL_SMART3IO_PADCONF_1[25:24] UART2_DR1_MB CONTROL_SMART3IO_PADCONF_2[12] UART2_DR1_LB	uart2_tx	Type 2 I/Os with MB[1:0] + LB[0] settings (for more information, see Section 18.4.12.9.4, *I/Os With Combined Mode and Load Settings*)

Table 18-90. UART3 Signal Group Parameter Controls to Different Interface I/O Pads Mapping

UART3 Interface I/O Controls		
Bit Fields for Pad Group Controls	**Pads (Muxmode = 0) in Group**	**Type of I/O Group-Associated Control Bit Fields**
CONTROL_SMART1IO_PADCONF_0[7:6] UART3_DR0_SC CONTROL_SMART1IO_PADCONF_1[7:6] UART3_DR0_LB	uart3_cts_rctx;	Low-speed I/Os LB[1: 0] + SC[1:0] controls (See Section 18.4.12.9.3 for more information.)
CONTROL_SMART1IO_PADCONF_0[5:4] UART3_DR1_SC CONTROL_SMART1IO_PADCONF_1[5:4] UART3_DR1_LB	uart3_rts_sd; uart3_rx_irrx; uart3_tx_irtx	Low-speed I/Os LB[1: 0] + SC[1:0] controls (See Section 18.4.12.9.3 for more information.)

Table 18-91. UART4 Signal Group Parameter Controls to Different Interface I/O Pads Mapping

UART4 Interface I/O Controls		
Bit Fields for Pad Group Controls	**Pads (Muxmode = 0) in Group**	**Type of I/O Group-Associated Control Bit Fields**
CONTROL_SMART3IO_PADCONF_1[23:22] UART4_DR0_MB CONTROL_SMART3IO_PADCONF_2[11] UART4_DR0_LB	uart4_rx; uart4_tx;	Type 2 I/Os with MB[1:0] + LB[0] settings (for more information, see Section 18.4.12.9.4, *I/Os With Combined Mode and Load Settings*)

Table 18-92. McSPI1 Signal Group Parameter Controls to Different Interface I/O Pads Mapping

McSPI1 Interface I/O Controls		
Bit Fields for Pad Group Controls	**Pads (Muxmode = 0) in Group**	**Type of I/O Group-Associated Control Bit Fields**
CONTROL_SMART1IO_PADCONF_0[11:10] MCSPI1_DR0_SC CONTROL_SMART1IO_PADCONF_1[11:10] MCSPI1_DR0_LB	mcspi1_clk; mcspi1_somi; mcspi1_simo; mcspi1_cs0	Low-speed I/Os LB[1: 0] + SC[1:0] controls (See Section 18.4.12.9.3 for more information.)
CONTROL_SMART1IO_PADCONF_0[9:8] UART1_DR0_SC CONTROL_SMART1IO_PADCONF_1[9:8] UART1_DR0_LB	mcspi1_cs1	Low-speed I/Os LB[1: 0] + SC[1:0] controls (See Section 18.4.12.9.3 for more information.)

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Table 18-92. McSPI1 Signal Group Parameter Controls to Different Interface I/O Pads Mapping (continued)

McSPI1 Interface I/O Controls		
Bit Fields for Pad Group Controls	**Pads (Muxmode = 0) in Group**	**Type of I/O Group-Associated Control Bit Fields**
CONTROL_SMART3IO_PADCONF_3[25:24] SLIMBUS2_DR1_MB CONTROL_SMART3IO_PADCONF_3[18] SLIMBUS2_DR1_LB	mcspi1_cs2	Type 2 I/Os with MB[1:0] + LB[0] settings (for more information, see Section 18.4.12.9.4, *I/Os With Combined Mode and Load Settings*)
CONTROL_SMART3IO_PADCONF_3[21:20] SLIMBUS2_DR3_MB CONTROL_SMART3IO_PADCONF_3[16] SLIMBUS2_DR3_LB	mcspi1_cs3	Type 2 I/Os with MB[1:0] + LB[0] settings (for more information, see Section 18.4.12.9.4, *I/Os With Combined Mode and Load Settings*)

Table 18-93. McSPI4 Signal Group Parameter Controls to Different Interface I/O Pads Mapping

McSPI4 Interface I/O Controls		
Bit Fields for Pad Group Controls	**Pads (Muxmode = 0) in Group**	**Type of I/O Group-Associated Control Bit Fields**
CONTROL_SMART3IO_PADCONF_0[13:12] MCSPI4_DR0_MB CONTROL_SMART3IO_PADCONF_2[22] MCSPI4_DR0_LB	mcspi4_clk; mcspi4_simo; mcspi4_somi;	Type 2 I/Os with MB[1:0] + LB[0] settings (for more information, see Section 18.4.12.9.4, *I/Os With Combined Mode and Load Settings*)
CONTROL_SMART3IO_PADCONF_0[11:10] MCSPI4_DR1_MB CONTROL_SMART3IO_PADCONF_2[21] MCSPI4_DR1_LB	mcspi4_cs0	Type 2 I/Os with MB[1:0] + LB[0] settings (for more information, see Section 18.4.12.9.4, *I/Os With Combined Mode and Load Settings*)

Table 18-94. I2C1 Signal Group Parameter Controls to Different Interface I/O Pads Mapping

I2C1 Interface I/O Controls		
Bit Fields for Pad Group Controls	**Pads (Muxmode = 0) in Group**	**Type of I/O Group-Associated Control Bit Fields**
CONTROL_I2C_0[3] I2C1_SCL_GLFENB	i2c1_scl	Enable glitch-free operation for I^2C receiver. (See Section 18.4.12.9.8 for more information.)
CONTROL_I2C_0[2:1] I2C1_SCL_LOAD_BITS		LB[1:0] – load bit controls to select internal pullup resistor value . (See for more information.)
CONTROL_I2C_0[0] I2C1_SCL_PULLUPRESX		Bit to enable internal pullup resistor option. (See Section 18.4.12.9.8 for more information.)
CONTROL_I2C_0[19] I2C1_SDA_GLFENB	i2c1_sda	Enable glitch-free operation for I^2C receiver. (See Section 18.4.12.9.8 for more information.)
CONTROL_I2C_0[18:17] I2C1_SDA_LOAD_BITS		LB[1:0] – load bit controls to select internal pullup resistor value . (See for more information.)
CONTROL_I2C_0[16] I2C1_SDA_PULLUPRESX		Bit to enable internal pullup resistor option. (See Section 18.4.12.9.8 for more information.)

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Table 18-95. I2C2 Signal Group Parameter Controls to Different Interface I/O Pads Mapping

I2C2 Interface I/O Controls		
Bit Fields for Pad Group Controls	**Pads (Muxmode = 0) in Group**	**Type of I/O Group-Associated Control Bit Fields**
CONTROL_I2C_0[7] I2C2_SCL_GLFENB	i2c2_scl	Enable glitch-free operation for I^2C receiver. (See Section 18.4.12.9.8 for more information.)
CONTROL_I2C_0[6:5] I2C2_SCL_LOAD_BITS		LB[1:0] – load bit controls to select internal pullup resistor value . (See for more information.)
CONTROL_I2C_0[4] I2C2_SCL_PULLUPRESX		Bit to enable internal pullup resistor option. (See Section 18.4.12.9.8 for more information.)
CONTROL_I2C_0[23] I2C2_SDA_GLFENB	i2c2_sda	Enable glitch-free operation for I^2C receiver. (See Section 18.4.12.9.8 for more information.)
CONTROL_I2C_0[22:21] I2C2_SDA_LOAD_BITS		LB[1:0] – load bit controls to select internal pullup resistor value . (See for more information.)
CONTROL_I2C_0[20] I2C2_SDA_PULLUPRESX		Bit to enable internal pullup resistor option. (See Section 18.4.12.9.8 for more information.)

Table 18-96. I2C3 Signal Group Parameter Controls to Different Interface I/O Pads Mapping

I2C3 Interface I/O Controls		
Bit Fields for Pad Group Controls	**Pads (Muxmode = 0) in Group**	**Type of I/O Group-Associated Control Bit Fields**
CONTROL_I2C_0[11] I2C3_SCL_GLFENB	i2c3_scl	Enable glitch-free operation for I^2C receiver. (See Section 18.4.12.9.8 for more information.)
CONTROL_I2C_0[10:9] I2C3_SCL_LOAD_BITS		LB[1:0] - load bit controls to select internal pullup resistor value . (See for more information.)
CONTROL_I2C_0[8] I2C3_SCL_PULLUPRESX		Bit to enable internal pullup resistor option. (See Section 18.4.12.9.8 for more information.)
CONTROL_I2C_0[27] I2C3_SDA_GLFENB	i2c3_sda	Enable glitch-free operation for I^2C receiver. (See Section 18.4.12.9.8 for more information.)
CONTROL_I2C_0[26:25] I2C3_SDA_LOAD_BITS		LB[1:0] – load bit controls to select internal pullup resistor value. (See for more information.)
CONTROL_I2C_0[24] I2C3_SDA_PULLUPRESX		Bit to enable internal pullup resistor option. (See Section 18.4.12.9.8 for more information.)

Table 18-97. I2C4 Signal Group Parameter Controls to Different Interface I/O Pads Mapping

I2C4 Interface I/O Controls		
Bit Fields for Pad Group Controls	**Pads (Muxmode = 0) in Group**	**Type of I/O Group-Associated Control Bit Fields**
CONTROL_I2C_0[15] I2C4_SCL_GLFENB	i2c4_scl	Enable glitch-free operation for I^2C receiver. (See Section 18.4.12.9.8 for more information.)
CONTROL_I2C_0[14:13] I2C4_SCL_LOAD_BITS		LB[1:0] – load bit controls to select internal pullup resistor value . (See for more information.)
CONTROL_I2C_0[12] I2C4_SCL_PULLUPRESX		Bit to enable internal pullup resistor option. (See Section 18.4.12.9.8 for more information.)

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Table 18-97. I2C4 Signal Group Parameter Controls to Different Interface I/O Pads Mapping (continued)

I2C4 Interface I/O Controls		
Bit Fields for Pad Group Controls	**Pads (Muxmode = 0) in Group**	**Type of I/O Group-Associated Control Bit Fields**
CONTROL_I2C_0[31] I2C4_SDA_GLFENB	i2c4_sda	Enable glitch-free operation for I^2C receiver. (See Section 18.4.12.9.8 for more information.)
CONTROL_I2C_0[30:29] I2C4_SDA_LOAD_BITS		LB[1:0] – load bit controls to select internal pullup resistor value . (See for more information.)
CONTROL_I2C_0[28] I2C4_SDA_PULLUPRESX		Bit to enable internal pullup resistor option. (See Section 18.4.12.9.8 for more information.)

Table 18-98. SR Signal Group Parameter Controls to Different Interface I/O Pads Mapping

SR Interface I/O Controls		
Bit Fields for Pad Group Controls	**Pads (Muxmode = 0) in Group**	**Type of I/O Group-Associated Control Bit Fields**
CONTROL_I2C_2[31] SR_SCL_GLFENB	sr_scl	Enable glitch-free operation for SmartReflex™ I^2C receiver (See Section 18.4.12.9.8 for more information.)
CONTROL_I2C_2[30:29] SR_SCL_LOAD_BITS		LB[1:0] – load bit controls to select internal pullup resistor value (See for more information.)
CONTROL_I2C_2[28] SR_SCL_PULLUPRESX		Bit to enable internal pullup resistor option (See Section 18.4.12.9.8 for more information.)
CONTROL_I2C_2[27] SR_SDA_GLFENB	sr_sda	Enable glitch-free operation for SmartReflex I^2C receiver (See Section 18.4.12.9.8 for more information.)
CONTROL_I2C_2[26:25] SR_SDA_LOAD_BITS		LB[1:0] – load bit controls to select internal pullup resistor value (See for more information.)
CONTROL_I2C_2[24] SR_SDA_PULLUPRESX		Bit to enable internal pullup resistor option (See Section 18.4.12.9.8 for more information.)

Table 18-99. System Signals Group Parameter Controls to Different Interface I/O Pads Mapping

System Interface I/O Controls		
Bit Fields for Pad Group Controls	**Pads (Muxmode = 0) in Group**	**Type of I/O Group-Associated Control Bit Fields**
CONTROL_SMART1NOPMIO_PADCONF_0[31:30] FREF_DR0_SC CONTROL_SMART1NOPMIO_PADCONF_1[31:30] FREF_DR0_LB	fref_clk_ioreq	Low-speed I/Os LB[1: 0] + SC[1:0] controls (See Section 18.4.12.9.3 for more information.)
CONTROL_SMART3NOPMIO_PADCONF_0[31:30] FREF_DR1_MB CONTROL_SMART3NOPMIO_PADCONF_1[31] FREF_DR1_LB0	fref_clk0_out	Type 2 I/Os with MB[1:0] + LB[0] settings (for more information, see Section 18.4.12.9.4, *I/Os With Combined Mode and Load Settings*)
CONTROL_SMART3IO_PADCONF_1[5:4] FREF_DR2_MB CONTROL_SMART3IO_PADCONF_2[6] FREF_DR2_LB	fref_clk1_out	Type 2 I/Os with MB[1:0] + LB[0] settings (for more information, see Section 18.4.12.9.4, *I/Os With Combined Mode and Load Settings*)

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Table 18-99. System Signals Group Parameter Controls to Different Interface I/O Pads Mapping (continued)

System Interface I/O Controls		
Bit Fields for Pad Group Controls	**Pads (Muxmode = 0) in Group**	**Type of I/O Group-Associated Control Bit Fields**
CONTROL_SMART3IO_PADCONF_1[3:2] FREF_DR3_MB CONTROL_SMART3IO_PADCONF_2[9] FREF_DR3_LB	fref_clk2_out	Type 2 I/Os with MB[1:0] + LB[0] settings (for more information, see Section 18.4.12.9.4, *I/Os With Combined Mode and Load Settings*)
CONTROL_SMART3NOPMIO_PADCONF_0 [23:22] FREF_DR4_MB CONTROL_SMART3NOPMIO_PADCONF_1 [27] FREF_DR4_LB0	fref_clk3_req	Type 2 I/Os with MB[1:0] + LB[0] settings (for more information, see Section 18.4.12.9.4, *I/Os With Combined Mode and Load Settings*)
CONTROL_SMART3NOPMIO_PADCONF_0 [29:28] FREF_DR5_MB CONTROL_SMART3NOPMIO_PADCONF_1 [30] FREF_DR5_LB0	fref_clk3_out	Type 2 I/Os with MB[1:0] + LB[0] settings (for more information, see Section 18.4.12.9.4, *I/Os With Combined Mode and Load Settings*)
CONTROL_SMART3NOPMIO_PADCONF_0 [27:26] FREF_DR6_MB CONTROL_SMART3NOPMIO_PADCONF_1 [29] FREF_DR6_LB0	fref_clk4_req	Type 2 I/Os with MB[1:0] + LB[0] settings (for more information, see Section 18.4.12.9.4, *I/Os With Combined Mode and Load Settings*)
CONTROL_SMART3NOPMIO_PADCONF_0 [25:24] FREF_DR7_MB CONTROL_SMART3NOPMIO_PADCONF_1 [28] FREF_DR7_LB0	fref_clk4_out	Type 2 I/Os with MB[1:0] + LB[0] settings (for more information, see Section 18.4.12.9.4, *I/Os With Combined Mode and Load Settings*)
CONTROL_SMART1NOPMIO_PADCONF_0 [19:18] GPIO_DR7_SC CONTROL_SMART1NOPMIO_PADCONF_1 [19:18] GPIO_DR7_LB	sys_pwron_reset_out	Low-speed I/Os LB[1: 0] + SC[1:0] controls (See Section 18.4.12.9.3 for more information.)
CONTROL_SMART1IO_PADCONF_0[23:22] GPIO_DR8_SC CONTROL_SMART1IO_PADCONF_1[23:22] GPIO_DR8_LB	sys_nirq2	Low-speed I/Os LB[1: 0] + SC[1:0] controls (See Section 18.4.12.9.3 for more information.)
CONTROL_SMART1IO_PADCONF_0[21:20] GPIO_DR9_SC CONTROL_SMART1IO_PADCONF_1[21:20] GPIO_DR9_LB	sys_boot0 -sys_boot5	Low-speed I/Os LB[1: 0] + SC[1:0] controls (See Section 18.4.12.9.3 for more information.)
CONTROL_SMART1NOPMIO_PADCONF_0 [15:14] DPM_DR0_SC CONTROL_SMART1NOPMIO_PADCONF_1 [15:14] DPM_DR0_LB	sys_boot6; sys_boot7	Low-speed I/Os LB[1: 0] + SC[1:0] controls (See Section 18.4.12.9.3 for more information.)

Table 18-100. DPM Signals Group Parameter Controls to Different Interface I/O Pads Mapping

System Interface I/O Controls		
Bit Fields for Pad Group Controls	**Pads (Muxmode=0) in Group**	**Type of I/O Group-Associated Control Bit Fields**
CONTROL_SMART2IO_PADCONF_2[31] DPM_DR1_DS	dpm_emu0; dpm_emu1	I/O cell with single-bit drive strength (DS) control for driver output impedance (See Section 18.4.12.9.5 for more information.)

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Table 18-100. DPM Signals Group Parameter Controls to Different Interface I/O Pads Mapping (continued)

System Interface I/O Controls		
Bit Fields for Pad Group Controls	**Pads (Muxmode=0) in Group**	**Type of I/O Group-Associated Control Bit Fields**
CONTROL_SMART2IO_PADCONF_2[15] USBA0_DR0_DS	dpm_emu2	I/O cell with single-bit drive strength (DS) control for driver output impedance (See Section 18.4.12.9.5 for more information.)
CONTROL_SMART2IO_PADCONF_2[14] USBA0_DR1_DS	dpm_emu3–dpm_emu5	I/O cell with single-bit drive strength (DS) control for driver output impedance (See Section 18.4.12.9.5 for more information.)
CONTROL_SMART2IO_PADCONF_2[19] UART3_DR2_DS	dpm_emu6	I/O cell with single-bit drive strength (DS) control for driver output impedance (See Section 18.4.12.9.5 for more information.)
CONTROL_SMART2IO_PADCONF_2[18] UART3_DR3_DS	dpm_emu7	I/O cell with single-bit drive strength (DS) control for driver output impedance (See Section 18.4.12.9.5 for more information.)
CONTROL_SMART2IO_PADCONF_2[17] UART3_DR4_DS	dpm_emu8	I/O cell with single-bit drive strength (DS) control for driver output impedance (See Section 18.4.12.9.5 for more information.)
CONTROL_SMART2IO_PADCONF_2[16] UART3_DR5_DS	dpm_emu9	I/O cell with single-bit drive strength (DS) control for driver output impedance (See Section 18.4.12.9.5 for more information.)
CONTROL_SMART2IO_PADCONF_2[13] USBA_DR2_DS	dpm_emu10– dpm_emu13	I/O cell with single-bit drive strength (DS) control for driver output impedance (See Section 18.4.12.9.5 for more information.)
CONTROL_SMART2IO_PADCONF_2[28] GPIO_DR10_DS	dpm_emu14 ; dpm_emu15	I/O cell with single-bit drive strength (DS) control for driver output impedance (See Section 18.4.12.9.5 for more information.)
CONTROL_SMART2IO_PADCONF_2[30] DPM_DR2_DS	dpm_emu16; dpm_emu17	I/O cell with single-bit drive strength (DS) control for driver output impedance (See Section 18.4.12.9.5 for more information.)
CONTROL_SMART2IO_PADCONF_2[29] DPM_DR3_DS	dpm_emu18; dpm_emu19	I/O cell with single-bit drive strength (DS) control for driver output impedance (See Section 18.4.12.9.5 for more information.)

18.4.12.10 Dual Voltage-Supplied Peripheral Controls

Some of the peripheral I/Os have the option to be supplied with a 1.2-V or 1.8-V power supply (VDDS through device external pads). The power supply level to the dual-voltage I/Os of different peripherals is configurable through bit fields in the CONTROL_CORE_PADCONF_MODE register in the CORE domain (EMIF, GPMC, C2C,CAMERA,and SDMMC2 I/Os) and the CONTROL_WKUP_PADCONF_MODE register in the WKUP domain (EMIF and FREF generator). One control bit in these registers is dedicated to set dual-voltage per group of pads.

NOTE: Dynamic switching between 1.2-V and 1.8-V voltage modes on dual-voltage peripheral I/Os is not allowed.

Table 18-101 describes dual-voltage controls versus the mapping of different pads.

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Table 18-101. Dual-Voltage Peripheral Control Bits vs Pad Mapping

Dual-Voltage VDDS = 1.2-V/1.8-V Control Bits	Pads With Dual-Voltage Settings
CONTROL_CORE_PADCONF_MODE[22] VDDS_DV_SDMMC2	gpmc_ad0–gpmc_ad7
	gpmc_noe
	gpmc_nwe
CONTROL_CORE_PADCONF_MODE[25] VDDS_DV_C2C	gpmc_ad8–gpmc_ad15
	gpmc_a16–gpmc_a25
	gpmc_ncs1–gpmc_ncs3
	gpmc_nbe1
	gpmc_wait1
	gpmc_wait2
	gpmc_ncs4–gpmc_ncs7
	c2c_vref
CONTROL_CORE_PADCONF_MODE[23] VDDS_DV_GPMC0	gpmc_clk
	gpmc_nbe0_cle
CONTROL_CORE_PADCONF_MODE[20] VDDS_DV_GPMC1	gpmc_ncs0
	gpmc_nwp
	gpmc_nadv_ale
	gpmc_wait0
CONTROL_CORE_PADCONF_MODE[24] VDDS_DV_CAM	cam_globalreset
	cam_shutter
	cam_strobe
	i2c3_scl
	i2c3_sda
	fref_clk1_out
	fref_clk2_out
CONTROL_CORE_PADCONF_MODE[31] VDDS_DV_BANK0	usbb1_ulpitll_clk
	usbb1_ulpitll_stp
	usbb1_ulpitll_dir
	usbb1_ulpitll_nxt
	usbb1_ulpitll_dat0–usbb1_ulpitll_dat7
CONTROL_CORE_PADCONF_MODE[30] VDDS_DV_BANK1	abe_mcbsp2_clkx
	abe_mcbsp2_dr
	abe_mcbsp2_dx
	abe_mcbsp2_fsx
	abe_mcbsp1_clkx
	abe_mcbsp1_dr
	abe_mcbsp1_dx
	abe_mcbsp1_fsx
	uart2_cts
	uart2_rts
	uart2_rx
	uart2_tx
CONTROL_CORE_PADCONF_MODE[19] VDDS_DV_BANK2_SHARED0	abe_pdm_ul_data
	abe_pdm_dl_data
	abe_pdm_frame
	abe_pdm_lb_clk
	abe_clks

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Table 18-101. Dual-Voltage Peripheral Control Bits vs Pad Mapping (continued)

Dual-Voltage VDDS = 1.2-V/1.8-V Control Bits	Pads With Dual-Voltage Settings
	abe_dmic_clk1
	abe_dmic_din1
	abe_dmic_din2
	abe_dmic_din3
	i2c1_scl
	i2c1_sda
CONTROL_WKUP_PADCONF_MODE[30] VDDS_DV_BANK2_SHARED1	sr_scl
	sr_sda
CONTROL_CORE_PADCONF_MODE[29] VDDS_DV_BANK3	mcspi1_clk
	mcspi1_somi
	mcspi1_simo
	mcspi1_cs0–mcspi1_cs3
CONTROL_CORE_PADCONF_MODE[28] VDDS_DV_BANK4	sdmmc5_clk
	sdmmc5_cmd
	sdmmc5_dat0–sdmmc5_dat3
CONTROL_CORE_PADCONF_MODE[27] VDDS_DV_BANK5	mcspi4_clk
	mcspi4_simo
	mcspi_somi
	mcspi_cs0
	uart4_rx
	uart4_tx
	i2c4_scl
	i2c4_sda
CONTROL_CORE_PADCONF_MODE[26] VDDS_DV_BANK6	usbb2_ulpitll_clk
	usbb2_ulpitll_stp
	usbb2_ulpitll_dir
	usbb2_ulpitll_nxt
	usbb2_ulpitll_dat0–usbb2_ulpitll_dat7
CONTROL_CORE_PADCONF_MODE[21] VDDS_DV_BANK7	kpd_col0–kpd_col5
	kpd_row0–kpd_row5
CONTROL_WKUP_PADCONF_MODE[31] VDDS_DV_FREF	fref_clk3_req
	fref_clk3_out
	fref_clk4_req
	fref_clk4_out

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18.5 Control Module Programming Guide

18.5.1 Control Module Low-Level Programming Models

This section describes the low-level programming sequences for the configuration and use of the control module.

18.5.1.1 Global Initialization

18.5.1.1.1 Surrounding Modules Global Initialization

This section identifies the requirements for initializing the surrounding modules when the control module is to be used for the first time after a device reset. This initialization of surrounding modules is based on the environment and integration of the control module. For more information, see *Section 18.2, Control Module Environment*, and Section 18.3, *Control Module Integration*.

Table 18-102. Global Initialization of Surrounding Modules

Surrounding Modules	Comments
PRCM	The three clocks coming from the PRCM module (CFG_L4_ICLK , WKUP_L4_ICLK2 , and CORE_TS_FCLK) are not software-controlled by PRCM. For more information about the three clocks, see Section 3.6.3.2.4, *CM2 Clock Generator*, and Section 3.6.3.1, *PRM Clock Source*, in Chapter 3, *Power, Reset, and Clock Management*.
L4 interconnect	For information about the L4-CFG interconnect configuration, see Section 13.3, *L4 Interconnects*, in Chapter 13, *Interconnects*.

18.5.1.1.2 Control Module Global Initialization

18.5.1.1.2.1 Software Reset

The control module is not sensitive to a software reset.

18.5.1.1.2.2 Clock Gating Configuration

As described in Section 18.4.2, *Control Module Clock Configuration*, the programmer can choose a clock-gating strategy individually for each of the four control module instances. Table 18-103 explains the necessary steps.

Table 18-103. Configure Clock Gating for Different Control Module Instances

Step	Register/Bit Field/Programming Model	Value
Set clock gating for SYSCTRL_PADCONF_CORE.	CONTROL_PADCONF_CORE_SYSCONFIG[3:2]	0x-
Set clock gating for SYSCTRL_PADCONF_WKUP.	CONTROL_PADCONF_WKUP_SYSCONFIG[3:2]	0x-
Set clock gating for SYSCTRL_GENERAL_CORE.	CONTROL_GEN_CORE_SYSCONFIG[3:2] CONTROL_TEMP_SENSOR[13]	0x-
Set clock gating for SYSCTRL_GENERAL_WKUP.	CONTROL_GEN_WKUP_SYSCONFIG[3:2]	0x-

18.5.1.2 Operational Modes Configuration

18.5.1.2.1 Video Driver Configuration

This section provides information about all modules and features in the high-tier device.

For more information about the VDAC, see Section 10.6, *Video Encoder*.

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Table 18-104. Control Module AVDAC Configuration

Step	Register/Bit Field/Programming Model	Value
Video buffer is bypassed or not bypassed.	CONTROL_AVDAC[30] AVDAC_TVOUTBYPASS	0b-
Enable or disable ac coupling for TV output.	CONTROL_AVDAC[31] AVDAC_ACEN	0b-

NOTE: The (VDAC) function is not supported.

18.5.1.2.2 Extended-Drain I/Os and PBIAS Cells Programming Guide

This section describes the programming flow from 3.0 V to 1.8 V, and vice versa, when operating with the extended-drain I/Os and PBIAS cells.

Figure 18-24. Configuring PBIAS Cell to Operate in Different Modes, Interrupt Method

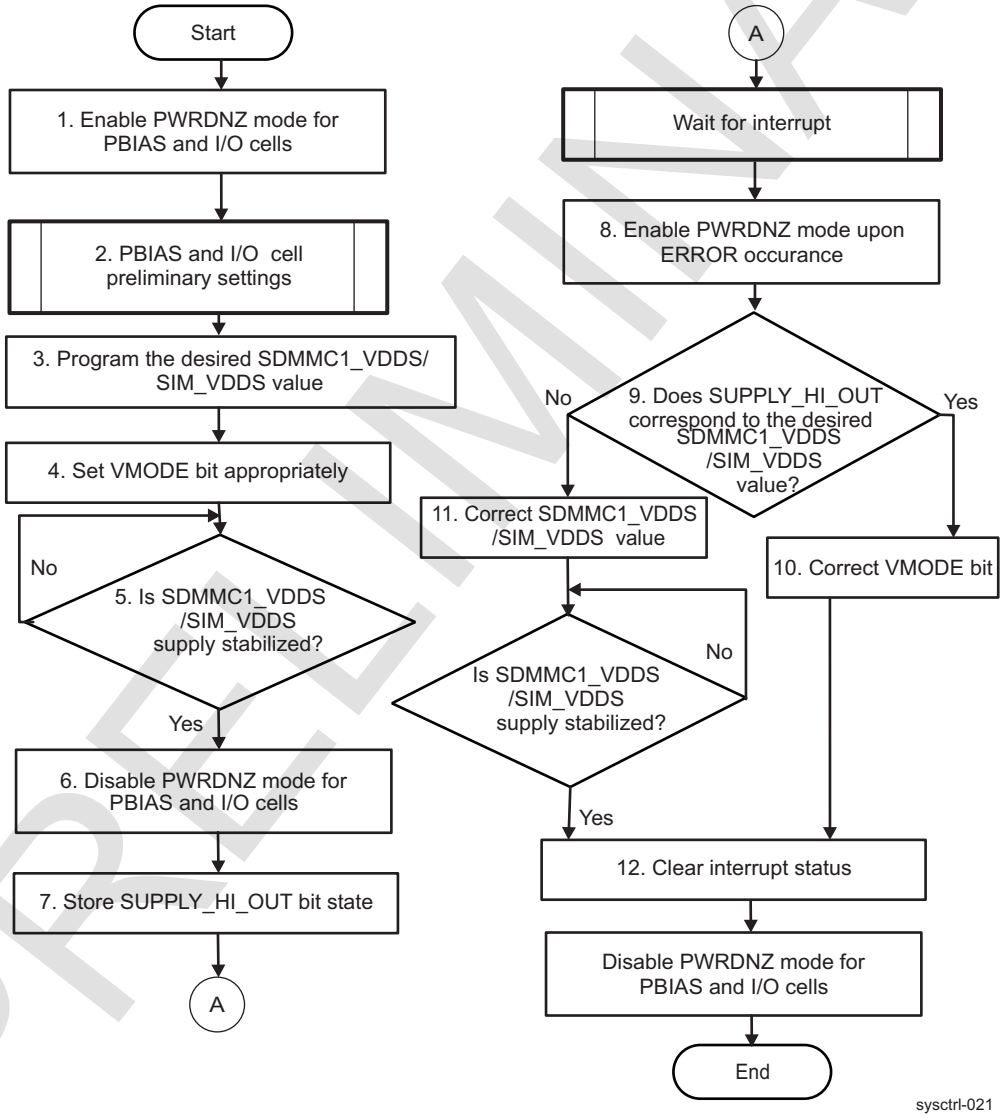

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Table 18-105. Register Settings for Configuring the MMC1_PBIAS and MMC1 I/O Cells

Procedure Name	Description	Register Settings
1. Enable PWRDNZ mode for MMC1_PBIAS cell and MMC/SD/SDIO1 I/O cell.	Software must keep MMC1_PBIAS cell and MMC1_IO cell PWRDNZ signals low whenever SDMMC1_VDDS ramps up/down or changes. This is for cell protection purposes.	1. Set CONTROL_PBIASLITE[22] MMC1_PBIASLITE_PWRDNZ = 0b0. 2. Set CONTROL_PBIASLITE[26] MMC1_PWRDNZ = 0b0.
2. Preliminary MMC1_PBIAS and MMC1 IO cell settings	Enable MMC1_PBIAS cell output and MMC1_PBIAS error associated interrupt. Select desired I/Os within the MMC1 I/O cell and set the corresponding pad configuration fields appropriately. Set the group speed and pullup strength controls for the MMC/SD/SDIO1 pads.	1. Set CONTROL_PBIASLITE[25]MMC1_PBIASLITE_HIZ_MODE = 0b0. 2. For information about setting the MA_IRQ_75 line associated interrupt request PBIAS_IRQ, see Chapter 17, *Interrupt Controller*. 3. For I/O multiplexing and pad configuration settings, see Section 18.5.1.2.5, *Pad Configuration Programming Points*. 4. Set the speed control bits for the MMC1 I/O cell pads: • CONTROL_MMC1[27] SDMMC1_DR0_SPEEDCTRL = 0b- • CONTROL_MMC1[26] SDMMC1_DR1_SPEEDCTRL = 0b- • CONTROL_MMC1[28] SDMMC1_DR2_SPEEDCTRL = 0b- 5. Set the pullup strength control bits for the MMC1 I/O cell pad groups: • CONTROL_MMC1[31] SDMMC1_PUSTRENGTH_GRP0=0b- • CONTROL_MMC1[30] SDMMC1_PUSTRENGTH_GRP1=0b- • CONTROL_MMC1[29] SDMMC1_PUSTRENGTH_GRP2=0b- • CONTROL_MMC1[28] SDMMC1_PUSTRENGTH_GRP3=0b-
3. Program the desired SDMMC1_VDDS voltage for MMC/SD/SDIO1 I/Os.	Program external power supply IC to generate appropriate SDMMC1_VDDS voltage:(3.0 V/ 1.8 V).	For more information about I^2C interface operation, see Section 23.1, *Multimaster High-Speed I^2C*.
4. Set VMODE bit appropriately.	PBIAS voltage generation is based on the value of VMODE, set according to externally applied SDMMC1_VDDS voltage.	Set CONTROL_PBIASLITE[21] MMC1_PBIASLITE_VMODE = 0b-(1).
5. Check whether the SDMMC1_VDDS supply is stabilized.	Check the state of the externally generated SDMMC1_VDDS voltage, which is provided through communication between the device and external power supply device over the I^2C interface.	For more information about I^2C interface settings, see Section 23.1, *Multimaster High-Speed I^2C.*
6. Disable PWRDNZ mode for MMC1_PBIAS and associated extended-drain MMC1 I/O cell.	This starts the MMC1_PBIAS cell work to generate the PBIAS voltage.	1. Set CONTROL_PBIASLITE[22] MMC1_PBIASLITE_PWRDNZ = 0b1. 2. Set CONTROL_PBIASLITE[26] MMC1_PWRDNZ = 0b1.
7. Store the state of the SUPPLY_HI_OUT bit.	Done as a preliminary step for error handling analysis. (Whenever PWRDNZ = 0b0 , SUPPLY_HI_OUT is unconditionally set to 0b0.)	Store CONTROL_PBIASLITE[24] MMC1_PBIASLITE_SUPPLY_HI_OUT bit in memory.
8.Enable PWRDNZ mode upon error occurrence.	It is recommended that all the I/Os are powered down (PWRDNZ = 0) as soon as VMODE_ERROR is high.	1. Set CONTROL_PBIASLITE[26] MMC1_PWRDNZ = 0b0 . 2. Set CONTROL_PBIASLITE[22]MMC1_PBIASLITE_PWRDNZ = 0b0.
9. Does SUPPLY_HI_OUT correspond to the desired SDMMC1_VDDS?	Test whether the error comes from incorrectly set value of SDMMC1_VDDS or incorrectly set VMODE bit.	Check the SUPPLY_HI_OUT bit stored in memory.
10. Correct VMODE bit.	If the level of SUPPLY_HI_OUT corresponds to the desired value of SDMMC1_VDDS, the correct the value of the VMODE bit	Modify the value of the CONTROL_PBIASLITE[21] MMC1_PBIASLITE_VMODE bit.
11. Correct SDMMC1_VDDS value.	If SUPPLY_HI_OUT is different from expected, correct and set SDMMC1_VDDS value over I^2C again.	For more information about I^2C interface settings, see Section 23.1, *Multimaster High-Speed I^2C* ,
12. Clear Interrupt status.	Clear the IRQ_MA_75 interrupt status flag.	For more information about setting the MA_IRQ_75 line associated interrupt request PBIAS_IRQ, see Chapter 17, *Interrupt Controller*.

(1) Must be set high when external MMC1_VDDS source is programmed to be 3.0 V, or low when the external MMC1_VDDS source is programmed to be 1.8 V. The reset default value corresponds to 3.0 V.

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Table 18-106. Register Settings for Configuring the PBIAS1 Cell, USBC1_ICUSB and gpio_wk0gpio_wk2 Associated I/O Cells

Procedure Name	Description	Register Settings
1. Enable PWRDNZ mode for PBIAS1 cell ,USBC1_ICUSB I/O cel,l and gpiowk0–gpiowk2 associated I/O cell.	Software must keep the PBIAS1 cell and the USBC1_ICUSB and gpiowk0 - gpiowk2 I/O cells associated with the PWRDNZ signals low whenever SIM_VDDS ramps up/down or changes. This is for cell protection purposes.	1. Set CONTROL_PBIASLITE[28] PBIASLITE1_PWRDNZ = 0b0. 2. Set CONTROL_PBIASLITE[20] USBC1_ICUSB_PWRDNZ = 0b0. 3. Set CONTROL_GPIOWK[28] GPIOWK_IO_PWRDNZ = 0b0.
2. Preliminary MMC1_PBIAS and MMC1 IO cell settings	Enable MMC1_PBIAS cell output and MMC1_PBIAS error associated interrupt. Select desired I/Os within the USBC1_ICUSB and GPIOWK I/O cells and set appropriately their corresponding pad configuration fields Set the speed and pulldown controls for the pads (if applicable).	1. Set CONTROL_PBIASLITE[31] PBIASLITE1_HIZ_MODE = 0b0. 2. For more information about setting MA_IRQ_75 line associated interrupt request PBIAS_IRQ, see Chapter 17, *Interrupt Controller*. 3. For the I/O multiplexing and pad configuration settings, see Section 18.5.1.2.5, *Pad Configuration Programming Points*. 4. Set the speed control bits for USBC1_ICUSB I/O cell pads CONTROL_MMC1[24] USBC1_DR0_SPEEDCTRL = 0b- (No speed ctrl available for GPIOWK associated I/O cell). 5. Disable strong pulldowns on the gpio_wk1 and gpio_wk2 pads available by default after reset: • CONTROL_GPIOWK[31] PAD_GPIO_WK1_LOW = 0b0 • CONTROL_GPIOWK[29] PAD_GPIO_WK2_LOW = 0b0
3. Program the desired voltage for SIM_VDDS for the USBC1_ICUSB/gpiowk0–gpiowk2 or (hw_dbg1–hw_dbg3 in WKUP domain) I/Os.	Program external power supply IC to generate appropriate SIM_VDDS voltage:(3.0 V/1.8 V)	For more information about I^2C interface operation, see Section 23.1, *Multimaster High-Speed I^2C* .
4. Set VMODE bit appropriately.	PBIAS voltage generation is based on the value of VMODE, set according to externally applied SIM_VDDS voltage.	Set CONTROL_PBIASLITE[27] PBIASLITE1_VMODE = 0b-. (1)
5. Check whether SIM_VDDS supply is stabilized.	Check the state of the externally generated SIM_VDDS voltage.This is provided through communication between the device and the companion power supply device over the I^2C interface.	For more information about I^2C interface setting, see Section 23.1, *Multimaster High-Speed I^2C* .
6. Disable PWRDNZ mode for PBIAS1 cell and its associated extended-drain USBC1_ICUSB and gpiowk0–gpiowk2 I/O cells.	This starts the PBIAS1 cell work to generate the PBIAS voltage.	1. Set CONTROL_PBIASLITE[28] PBIASLITE1_PWRDNZ = 0b1. 2. Set CONTROL_PBIASLITE[20] USBC1_ICUSB_PWRDNZ = 0b1. 3. Set CONTROL_GPIOWK[28] GPIOWK_IO_PWRDNZ = 0b1.
7. Store the state of the SUPPLY_HI_OUT bit.	Done as a preliminary step for error handling analysis. (Whenever PWRDNZ = 0b0 , SUPPLY_HI_OUT is unconditionally set to 0b0.)	Store the CONTROL_PBIASLITE[30] PBIASLITE1_SUPPLY_HI_OUT bit in memory.
8.Enable PWRDNZ mode upon error occurrence.	It is recommended that all the I/Os are powered down (PWRDNZ = 0) as soon as VMODE_ERROR is high.	1. Set CONTROL_PBIASLITE[28] PBIASLITE1_PWRDNZ = 0b0. 2. Set CONTROL_PBIASLITE[20] USBC1_ICUSB_PWRDNZ = 0b0. 3. Set CONTROL_GPIOWK[28] GPIOWK_IO_PWRDNZ = 0b0.
9. Does SUPPLY_HI_OUT correspond to the desired SIM_VDDS level?	Test whether the error comes from incorrectly set value of SIM_VDDS or incorrectly set VMODE bit.	Check the stored in memory SUPPLY_HI_OUT bit.
10. Correct VMODE bit.	If the level of SUPPLY_HI_OUT corresponds to the desired value for SIM_VDDS, the correct value of the VMODE bit.	Modify value of CONTROL_PBIASLITE[27] PBIASLITE1_VMODE.
11. Correct SIM_VDDS value.	If SUPPLY_HI_OUT is different than expected, correct and set SIM_VDDS value over I^2C again.	For more information about I^2C interface setting, see Section 23.1, *Multimaster High-Speed I^2C* .
12. Clear Interrupt status.	Clear the IRQ_MA_75 interrupt status flag.	For more information about setting MA_IRQ_75 line associated interrupt request PBIAS_IRQ, see Chapter 17, *Interrupt Controller*.

(1) Must be set high when the external SIM_VDDS source is programmed to be 3.0 V, or low when the external SIM_VDDS source is programmed to be 1.8 V. The reset default value corresponds to 3.0 V .

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18.5.1.2.3 Hardware Observability Settings

This section describes the procedures to control the hardware observability features of the device. To configure these features, the programmer must perform the steps listed in Table 18-107.

Table 18-107. Configure Hardware Observability Features

	Step	Register/Bit Field/Programming Model	Value
1.	Select the hwobs(0)/hwobs(1)/hwobs(2) signal frequency divider value (applies only to po_hw_dbg0, po_hw_dbg1, and po_hw_dbg2 bus signals propagated in the CORE power domain).	CONTROL_HWOBS_CONTROL[7:3] HWOBS_CLKDIV_SEL CONTROL_HWOBS_CONTROL[13:9] HWOBS_CLKDIV_SEL_1 CONTROL_HWOBS_CONTROL[18:14] HWOBS_CLKDIV_SEL_2	0x-(1)
2.	Enable/disable gating of hwobs and alternatively set all hwobs ports to 0 or 1.	.CONTROL_HWOBS_CONTROL[2] HWOBS_ALL_ZERO_MODE CONTROL_HWOBS_CONTROL[1] HWOBS_ALL_ONE_MODE	0x-(2)
3.	Enable/disable hwobs port gating only for signals coming from IPs identified in the MACRO group (applies only to po_hw_dbg bus signals propagated in the CORE power domain).	CONTROL_HWOBS_CONTROL[0] HWOBS_MACRO_ENABLE	0x- (3)
4.	Associate a certain hwobs channel to the CORE or WKUP power domain.	Configure each bit from the CONTROL_DEBOBS_FINAL_MUX_SEL[31:0] SELECT bit field appropriately for its corresponding hw_dbg channel.	0x-
5.	Choose the source of a signal or signal view channel in the CORE power domain.	Configure each CONTROL_CORE_CONF_DEBUG_SEL_TST_0[3:0] MODE through CONTROL_CORE_CONF_DEBUG_SEL_TST_31[3:0] MODE bit field appropriately for its corresponding hw_dbg channel.	0x-
6.	Choose the source of a signal within the WKUP power domain.	Configure each CONTROL_WKUP_CONF_DEBUG_SEL_TST_i[0] MODE bit, (where i = 0 to 31) appropriately for its corresponding hw_dbg channel i (where i = 0 to 31).	0x-
7.	Choose to associate a certain DPLL signal to a given DPLL signal view channel (applies only to po_hw_dbg bus signals propagated in the CORE power domain).	CONTROL_CONF_DPLL_FREQLOCK_SEL[2:0] MULT .CONTROL_CONF_DPLL_TINITZ_SEL[2:0] MULT CONTROL_CONF_DPLL_PHASELOCK_SEL[2:0] MULT CONTROL_CONF_DPLL_TENABLE_SEL[2:0] MULT CONTROL_CONF_DPLL_TENABLEDIV_SEL[2:0] MULT CONTROL_CONF_DPLL_BYPASSACK_SEL[2:0] MULT CONTROL_CONF_DPLL_IDLE_SEL[2:0] MULT	0x-
8.	Choose to associate a certain clockout signal to a given clockview channel (applies only to po_hw_dbg bus signals propagated in the CORE power domain).	CONTROL_CONF_CLK_SEL0[2:0] MULT through CONTROL_CONF_CLK_SEL2[2:0] MULT	0x-
9.	Choose to associate an sDMA signal to a given sDMA view channel (applies only to po_hw_dbg bus signals propagated in the CORE power domain).	CONTROL_CONF_SDMA_REQ_SEL0[6:0] MULT through CONTROL_CONF_SDMA_REQ_SEL3[6:0] MULT	0x-
10.	Set the appropriate pad configuration bit fields to associate the hw_dbgn pad function to output pins and configure additional output pad features.	For more information, see Section 18.4.11, *Hardware Observability*, and Section 18.4.8, *Pad Functional Multiplexing and Configuration*.	For more information, see Section 18.4.8, *PAD Functional Multiplexing and Configuration*.

(1) To configure the hwobs(0) channel to operate normally, the value of the HWOBS_CLKDIV_SEL, HWOBS_CLKDIV_SEL_1, or HWOBS_CLKDIV_SEL_2 bit must be set different than 0.

(2) Set both bits to 0 to enable hardware observability. Set only one bit to 1 to gate hwobs ports according to the output state required.

(3) The modules that belong to this group are: Cortex-A9 MPU subsystem, IVA-HD, display subsystem , CM2, and ABE.

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For more information about the different functions and registers associated with the hardware observability features, see Section 18.4.11, *Hardware Observability*.

18.5.1.2.4 Off Mode Preliminary Settings

This section describes configurations of pads to work in off mode. The following actions must be performed once, and remain valid for all device off - on transitions.

Table 18-108. Setting Pad Off Mode Through Padconfiguration Registers

Step	Register/Bit Field/Programming Model	Value
Set OFFMODEPULLTYPESELECT bit.	CONTROL_CORE_PAD0_X_PAD1_Y[29,13] – Select pullup/down type when pad in off mode.	0b-
Set OFFMODEPULLUDENABLE bit.	CONTROL_CORE_PAD0_X_PAD1_Y[28,12] – Enable/disable pullup/down feature when pad in off mode.	0b-
Set OFFMODEOUTVALUE bit.	CONTROL_CORE_PAD0_X_PAD1_Y[27,11] – Set off mode pad override value.	0b-
Set OFFMODEENABLE bit (enable/disable pad overriding capability in off mode).	CONTROL_CORE_PAD0_X_PAD1_Y[25,9] – Set pad to keep its previous state (it had before going to off mode) or force pad output to a certain override value (OFFMODEOUTVALUE) when pad in off mode.	0b-
Set OFFMODEOUTENABLE bit.	CONTROL_CORE_PAD0_X_PAD1_Y[26,10] – Enable/disable output in off mode.	0b-
Program a valid device ACTIVE pad configuration.	For more information about ACTIVE pad configuration, see Table 18-109.	
Set clock gating strategy.	. CONTROL_PADCONF_CORE_SYSCONFIG[3:2] IP_SYSCONFIG CONTROL_PADCONF_WKUP_SYSCONFIG[3:2] IP_SYSCONFIG	0x2,0x3
Enable/disable the wake-up detection capability(1).	CONTROL_CORE_PAD0_X_PAD1_Y[30,14]	0b-

(1) When the wake-up detection is enabled for a pad, this pad is configured as input. Therefore, be sure to write 0b1 in the OFFOUTENABLE bit to disable the output capability.

18.5.1.2.5 Pad Configuration Programming Points

This section describes through an example the configurations of pads necessary for working in active mode.

To configure the pad, ensure that the following steps are done:

1. Identify signals required on the interface based on the target application.

   Example: To configure the UART2 interface on balls, the required signals are uart2_tx, uart2_rts, uart2_cts, and uart2_rx.

2. Choose the pads used for those signals. Some signals may be available on several pads and/or may be multiplexed with other signals needed for another application. See Section 18.4.8.3, *Pad Multiplexing Register Fields.*

   Example: Unlike the UART2 interface signals, uart2_rx and uart2_tx, each of which is available on two pads, the uart2_cts and uart2_rts signals are available only on one pad each (MUXMODE = 0b000). The uart2_cts signal, however, is multiplexed with the MMC I/O signal sdmmc3_clk, and the uart2_rts signal is multiplexed with the MMC I/O signal sdmmc3_cmd on the same pad. Assume that the MMC I/O 3 interface is also required in the system. Therefore, for the MMC I/O interface signals, pads must be used where those signals are not multiplexed with a UART2 signal, if possible. In this case, the solution is to use sdmmc3_clk and sdmmc3_cmd on another two pads of the device (usbb2_ulpitll_dat7 and usbb2_ulpitll_dat6) configuring (MUXMODE = 0b010).

3. Identify the signal integrity parameter settings (drive strength, impedance, slew rate, pullup/pulldown strength, etc.) necessary for the pads associated I/O cells, listed in Section 18.4.12.9.9, *Device Interfaces Signal Group Controls Mapping*).

   For the register settings of the signal integrity parameters for the uart2_rx, uart2_tx, uart2_cts, and urat2_rts pads (this is the variant when the desired uart2 signals appear in MuxMode = 0x0), see Table 18-89.

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For the uart2_cts, uart2_rts, and uart2_rx pads, the following bit fields (Mode and Load bit group settings) must be set:

- CONTROL_SMART3IO_PADCONF_1[27:26] UART2_DR0_MB
- CONTROL_SMART3IO_PADCONF_2[13] UART2_DR0_LB

For the uart2_tx pad, the following bit fields (Mode and Load bit group settings) must be set:

- CONTROL_SMART3IO_PADCONF_1[25:24] UART2_DR1_MB
- CONTROL_SMART3IO_PADCONF_2[12] UART2_DR1_LB

For recommendations about the signal integrity parameter settings of the mentioned pad group, see the device data manual.

NOTE: To identify the signal-associated I/O cell signal parameter settings in Section 18.4.12.9.9, *Device Interfaces Signal Group Controls Mapping*, the user must search for the device pad name on which the desired signal is muxed, because the I/O cell settings are designated and listed on a per pad basis. This means that a signal name does not appear (unless MuxMode = 0x0) in Section 18.4.12.9.9, *Device Interfaces Signal Group Controls Mapping*, but only the pad on which the signal is muxed.

Pads that do not have software I/O cell signal integrity parameter controls are not listed in Section 18.4.12.9.9, *Device Interfaces Signal Group Controls Mapping*.

Assume the user application configures the sdmmc3_clk and sdmmc3_cmd signals on the usbb2_ulpitll_dat7 and usbb2_ulpitll_dat6 pads (MuxMode = 0x2). The I/O cell setting (single-bit group control – SPI3_DR0_DS of driver output impedance) listed in Table 18-77 also applies to the sdmmc3_clk and sdmmc3_cmd signals, which appear on the same pads, when MuxMode = 0x2.

In this case, the CONTROL_SMART2IO_PADCONF_2[21] SPI3_DR0_DS bit must be set to configure the I/O cell performance of sdmmc3_clk and sdmmc3_clk.

For recommendations about the mentioned pad group signal integrity parameter settings, see the device data manual.

4. Identify and program the peripheral dual-voltage settings, if they apply to the chosen pads:

   Table 18-101 lists the corresponding control bits of the pads in the CONTROL_CORE_PADCONF_MODE and CONTROL_WKUP_PADCONF_MODE registers. The identification of the I/O dual voltage domains/control bits for a signal must be made on a per-pad basis.

   All pads (uart2_cts, uart2_rts, uart2_rx, and uart2_tx) fall within the same dual-voltage domain (VDDS_DV_BANK1) and the I/O supply voltage (1.2 V/1.8 V) is configured by setting the CONTROL_CORE_PADCONF_MODE[30] VDDS_DV_BANK1 bit.

   As previously explained, the sdmmc3_clk and sdmmc3_cmd signals are muxed on the usbb2_ulpitll_dat7 and usbb2_ulpitll_dat6 pads. The dual-voltage control bit corresponding to these two pads is CONTROL_CORE_PADCONF_MODE[26] VDDS_DV_BANK6 (see Table 18-101).

   For more information about pad performance dependencies from I/O dual-voltage supply settings, see the device data manual.

5. Identify the pad configuration registers associated with the pads to be used in the application. See Section 18.4.8.3, *Pad Multiplexing Register Fields*.

   Example: Under the previous hypothesis, the pad configuration registers to program are:

   - uart2_rts: CONTROL_CORE_PAD0_UART2_CTS_PAD1_UART2_RTS[31:16]
   - uart2_cts: CONTROL_CORE_PAD0_UART2_CTS_PAD1_UART2_RTS[15:0]
   - uart2_tx: CONTROL_CORE_PAD0_UART2_RX_PAD1_UART2_TX[31:16]
   - uart2_rx: CONTROL_CORE_PAD0_UART2_RX_PAD1_UART2_TX[15:0]
   - sdmmc3_clk (MuxMode = 0x2): CONTROL_CORE_PAD0_USBB2_ULPITLL_DAT6_PAD1 _USBB2_ULPITLL_DAT7[31:16]
   - sdmmc3_cmd (MuxMode = 0x2): CONTROL_CORE_PAD0_USBB2_ULPITLL_DAT6_PAD1 _USBB2_ULPITLL_DAT7[15:0]

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Table 18-109. ACTIVE PADS Configuration Points

Step	Register/Bit Field/Programming Model	Value
1. Identify the interface signals and map them to the appropriate pads according to the application requirements and the device-specific pad I/O muxing capabilities. See Section 18.4.8.3, *Pad Multiplexing Register Fields*.	Define the list of I/O signal names: uart2_cts, uart2_rts, uart2_rx, uart2_tx, sdmmc3_clk, and sdmmc3_cmd Define the list of corresponding pads: uart2_cts, uart2_rts, uart2_rx, uart2_tx, usbb2_ulpitll_dat7, and usbb2_ulpitll_dat6	–
2. Identify the corresponding I/O cell signal integrity parameter controls for the pad (on a per-pad basis). See Section 18.4.12.9.9, *Device Interfaces Signal Group Controls Mapping*.	(uart2_cts, uart2_rts, uart2_rx pads) CONTROL_SMART3IO_PADCONF_1[27:26] UART2_DR0_MB CONTROL_SMART3IO_PADCONF_2[13] UART2_DR0_LB (uart2_tx pad) CONTROL_SMART3IO_PADCONF_1[25:24] UART2_DR1_MB CONTROL_SMART3IO_PADCONF_2[12] UART2_DR1_LB (usbb2_ulpitll_dat7, usbb2_ulpitll_dat6) CONTROL_SMART2IO_PADCONF_2[21] SPI3_DR0_DS	For more information about the recommended I/O settings, see the device data manual
3. Determine whether the pad is associated with a peripheral dual-voltage domain (see the device data manual). Identify its corresponding 1.2-V/1.8-V dual-voltage control bit in the CONTROL_CORE_PADCONF_MODE or CONTROL_WKUP_PADCONF_MODE register. See Table 18-101.	(uart2_cts, uart2_rts, uart2_rx, uart2_tx) CONTROL_CORE_PADCONF_MODE[30] VDDS_DV_BANK1 (usbb2_ulpitll_dat7, usbb2_ulpitll_dat6) CONTROL_CORE_PADCONF_MODE[26] VDDS_DV_BANK6	For more information about the I/O performance dependency on dual-voltage settings, see the device data manual.
4. Configure MUXMODE field in pad configuration registers associated with the pads used.	CONTROL_CORE_PAD0_UART2_CTS_PAD1_UART2_RTS[18:16] UART2_RTS_MUXMODE CONTROL_CORE_PAD0_UART2_CTS_PAD1_UART2_RTS[2:0] UART2_CTS_MUXMODE CONTROL_CORE_PAD0_UART2_RX_PAD1_UART2_TX[18:16] UART2_TX_MUXMODE CONTROL_CORE_PAD0_UART2_RX_PAD1_UART2_TX[2:0] UART2_RX_MUXMODE CONTROL_CORE_PAD0_USBB2_ULPITLL_DAT6_ PAD1_USBB2_ULPITLL_DAT7[18:16] USBB2_ULPITLL_DAT7_MUXMODE CONTROL_CORE_PAD0_USBB2_ULPITLL_DAT6_ PAD1 _USBB2_ULPITLL_DAT7[2:0] USBB2_ULPITLL_DAT6_MUXMODE	0b000 0b000 0b000 0b000 0b010 0b010
5. Select the type of the internal pullup/down resistor (1).	CONTROL_CORE_PAD0_UART2_RX_PAD1_UART2_TX[4] UART2_RX_PULLTYPESELECT CONTROL_CORE_PAD0_UART2_CTS_PAD1_UART2_RTS[2:0] UART2_CTS_PULLTYPESELECT	0b1 (pullup selected) 0b1 (pullup selected)
6. Enable/disable pullup/down feature of the pad (2).	CONTROL_CORE_PAD0_UART2_RX_PAD1_UART2_TX[3] UART2_RX_PULLUDENABLE CONTROL_CORE_PAD0_UART2_CTS_PAD1_UART2_RTS[3] UART2_CTS_PULLUDENABLE	0b1 (pull feature enabled) 0b1 (pull feature enabled)
7. Set the direction of the pin signal.(2)	CONTROL_CORE_PAD0_UART2_RX_PAD1_UART2_TX[8] UART2_RX_INPUTENABLE CONTROL_CORE_PAD0_UART2_CTS_PAD1_UART2_RTS[8] UART2_CTS_INPUTENABLE CONTROL_CORE_PAD0_UART2_RX_PAD1_UART2_TX[24] UART2_TX_INPUTENABLE CONTROL_CORE_PAD0_UART2_CTS_PAD1_UART2_RTS[24] UART2_RTS_INPUTENABLE CONTROL_CORE_PAD0_USBB2_ULPITLL_DAT6_ PAD1_USBB2_ULPITLL_DAT7[24] USBB2_ULPITLL_DAT7_INPUTENABLE (sdmmc3_clk) CONTROL_CORE_PAD0_USBB2_ULPITLL_DAT6_ PAD1 _USBB2_ULPITLL_DAT7[8] USBB2_ULPITLL_DAT6_INPUTENABLE (sdmmc3_cmd)	0b1 (input pin) 0b1 (input pin) 0b0 (output pin) 0b0 (output pin) 0b1 (input pin) 0b1 (input pin)

(1) It is recommended to use internal pullup/down resistor if pad is used as input and external pullup/down is not used.

(2) If the pad is configured in output mode, it is recommended for software to disable the internal pullup/pulldown associated with it.

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NOTE: The order for setting the previous pad configuration bits is not important.

NOTE: If a device pad is left unconnected, but power is supplied to the I/O, or the pad is used only as an output during the lifetime of the application, it is recommended to keep its corresponding pad configuration bit CONTROL_CORE /WKUP_PAD0_X_PAD1_Y.INPUTENABLE set to 0b0. This keeps the input buffer disabled and reduces static current consumption.

NOTE: I/Os are non-failsafe, which means that voltage must never be applied at a pad before the internal I/O supply voltage VDDS is powered.

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18.6 Control Module Register Manual

18.6.1 Control Module Instance Summary

Table 18-110 lists the base address and address space for the control module instances.

Table 18-110. Control Module Instance Summary

Module instance	Base Address	Size	Description
SYSCTRL_GENERAL_CORE	0x4A00 2000	4KB	Module
SYSCTRL_GENERAL_WKUP	0x4A30 C000	4KB	Module
SYSCTRL_PADCONF_CORE	0x4A10 0000	4KB	Module
SYSCTRL_PADCONF_WKUP	0x4A31 E000	4KB	Module

NOTE: All module registers are 8-, 16-, or 32-bit accessible through the L4 interconnect (little-endian encoding).

18.6.2 SYSCTRL_GENERAL_CORE Register Summary

Table 18-111. SYSCTRL_GENERAL_CORE Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	SYSCTRL_GENERAL_CORE Physical Address
CONTROL_GEN_CORE_REVISION	R	32	0x00000000	0x4A002000
CONTROL_GEN_CORE_HWINFO	R	32	0x00000004	0x4A002004
CONTROL_GEN_CORE_SYSCONFIG	RW	32	0x00000010	0x4A002010
CONTROL_STD_FUSE_DIE_ID_0	R	32	0x0000 0200	0x4A00 2200
CONTROL_ID_CODE	R	32	0x0000 0204	0x4A00 2204
CONTROL_STD_FUSE_DIE_ID_1	R	32	0x0000 0208	0x4A00 2208
CONTROL_STD_FUSE_DIE_ID_2	R	32	0x0000 020C	0x4A00 220C
CONTROL_STD_FUSE_DIE_ID_3	R	32	0x0000 0210	0x4A00 2210
CONTROL_STD_FUSE_PROD_ID_0	R	32	0x0000 0214	0x4A00 2214
CONTROL_STD_FUSE_PROD_ID_1	R	32	0x0000 0218	0x4A00 2218
CONTROL_STD_FUSE_USB_CONF	R	32	0x0000 021C	0x4A00 221C
CONTROL_STD_FUSE_CONF	R	32	0x0000 0220	0x4A00 2220
CONTROL_STD_FUSE_OPP_VDD_WKUP	R	32	0x0000 0228	0x4A00 2228
CONTROL_STD_FUSE_OPP_VDD_IVA_0	R	32	0x0000 022C	0x4A00 222C
CONTROL_STD_FUSE_OPP_VDD_IVA_1	R	32	0x0000 0230	0x4A00 2230
CONTROL_STD_FUSE_OPP_VDD_IVA_2	R	32	0x0000 0234	0x4A00 2234
CONTROL_STD_FUSE_OPP_VDD_IVA_3	R	32	0x0000 0238	0x4A00 2238
RESERVED	R	32	0x0000 023C	0x4A00 223C
CONTROL_STD_FUSE_OPP_VDD_MPU_0	R	32	0x0000 0240	0x4A00 2240
CONTROL_STD_FUSE_OPP_VDD_MPU_1	R	32	0x0000 0244	0x4A00 2244
CONTROL_STD_FUSE_OPP_VDD_MPU_2	R	32	0x0000 0248	0x4A00 2248
CONTROL_STD_FUSE_OPP_VDD_MPU_3	R	32	0x0000 024C	0x4A00 224C
RESERVED	R	32	0x0000 0250	0x4A00 2250
CONTROL_STD_FUSE_OPP_VDD_CORE_0	R	32	0x0000 0254	0x4A00 2254
CONTROL_STD_FUSE_OPP_VDD_CORE_1	R	32	0x0000 0258	0x4A00 2258
CONTROL_STD_FUSE_OPP_VDD_CORE_2	R	32	0x0000 025C	0x4A00 225C

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Table 18-111. SYSCTRL_GENERAL_CORE Register Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	SYSCTRL_GENERAL_CORE Physical Address
CONTROL_STD_FUSE_OPP_BGAP	R	32	0x0000 0260	0x4A00 2260
CONTROL_STD_FUSE_OPP_DPLL_0	R	32	0x0000 0264	0x4A00 2264
CONTROL_STD_FUSE_OPP_DPLL_1	R	32	0x0000 0268	0x4A00 2268
CONTROL_STATUS	R	32	0x0000 02C4	0x4A00 22C4
CONTROL_SEC_ERR_STATUS_FUNC	RW	32	0x0000 02D0	0x4A00 22D0
CONTROL_SEC_ERR_STATUS_DEBUG	RW	32	0x0000 02D4	0x4A00 22D4
RESERVED	R	32	0x0000 02D8	0x4A00 22D8
RESERVED	R	32	0x0000 02DC	0x4A00 22DC
CONTROL_DEV_CONF	RW	32	0x0000 0300	0x4A00 2300
RESERVED	RW	32	0x0000 0304	0x4A00 2304
CONTROL_LDOVBB_IVA_VOLTAGE_CTRL	RW	32	0x0000 0314	0x4A00 2314
CONTROL_LDOVBB_MPU_VOLTAGE_CTRL	RW	32	0x0000 0318	0x4A00 2318
CONTROL_LDOSRAM_IVA_VOLTAGE_CTRL	RW	32	0x0000 0320	0x4A00 2320
CONTROL_LDOSRAM_MPU_VOLTAGE_CTRL	RW	32	0x0000 0324	0x4A00 2324
CONTROL_LDOSRAM_CORE_VOLTAGE_CTRL	RW	32	0x0000 0328	0x4A00 2328
CONTROL_TEMP_SENSOR	RW	32	0x0000 032C	0x4A00 232C
CONTROL_DPLL_NWELL_TRIM_0	RW	32	0x0000 0330	0x4A00 2330
CONTROL_DPLL_NWELL_TRIM_1	RW	32	0x0000 0334	0x4A00 2334
RESERVED	RW	32	0x0000 0338	0x4A00 2338
CONTROL_USBOTGHS_CONTROL	RW	32	0x0000 033C	0x4A00 233C
CONTROL_DSS_CONTROL	RW	32	0x0000 0340	0x4A00 2340
RESERVED	RO	32	0x0000 0344	0x4A00 2344
CONTROL_CORTEX_M3_MMUADDRTRANSLTR	RW	32	0x0000 0348	0x4A00 2348
CONTROL_CORTEX_M3_MMUADDRLOGICTR	RW	32	0x0000 034C	0x4A00 234C
CONTROL_HWOBS_CONTROL	RW	32	0x0000 0350	0x4A00 2350
CONTROL_EMIF1_OFFSET	RW	32	0x0000 0360	0x4A00 2360
CONTROL_EMIF2_OFFSET	RW	32	0x0000 0364	0x4A00 2364
CONTROL_EMIF1_MASTER_CODE_0	RO	32	0x0000 0368	0x4A00 2368
CONTROL_EMIF1_MASTER_CODE_1	RO	32	0x0000 036C	0x4A00 236C
CONTROL_EMIF2_MASTER_CODE_0	RO	32	0x0000 0370	0x4A00 2370
CONTROL_EMIF2_MASTER_CODE_1	RO	32	0x0000 0374	0x4A00 2374
CONTROL_BANDGAP_CTRL	RW	32	0x0000 0378	0x4A00 2378
CONTROL_BANDGAP_COUNTER	RW	32	0x0000 037C	0x4A00 237C
CONTROL_BANDGAP_THRESHOLD	RW	32	0x0000 0380	0x4A00 2380
CONTROL_TSHUT_THRESHOLD	RW	32	0x0000 0384	0x4A00 2384
CONTROL_BANDGAP_STATUS	RO	32	0x0000 0388	0x4A00 2388
CONTROL_FORCEWRNP	RW	32	0x0000 03C0	0x4A00 23C0
CONTROL_GEN_CORE_OCPREG_SPARE	RW	32	0x0000 03FC	0x4A00 23FC
CONTROL_DEBOBS_FINAL_MUX_SEL	RW	32	0x0000 0400	0x4A00 2400
RESERVED	RO	32	0x0000 0404	0x4A00 2404
CONTROL_DEBOBS_MMR_MPU	RW	32	0x0000 0408	0x4A00 2408
RESERVED	RO	32	0x0000 0410	0x4A00 2410
RESERVED	RO	32	0x0000 0414	0x4A00 2414
RESERVED	RO	32	0x0000 0418	0x4A00 2418

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Table 18-111. SYSCTRL_GENERAL_CORE Register Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	SYSCTRL_GENERAL_CORE Physical Address
RESERVED	RO	32	0x0000 041C	0x4A00 241C
RESERVED	RO	32	0x0000 0420	0x4A00 2420
RESERVED	RO	32	0x0000 0424	0x4A00 2424
CONTROL_CONF_SDMA_REQ_SEL0	RW	32	0x0000 042C	0x4A00 242C
CONTROL_CONF_SDMA_REQ_SEL1	RW	32	0x0000 0430	0x4A00 2430
CONTROL_CONF_SDMA_REQ_SEL2	RW	32	0x0000 0434	0x4A00 2434
CONTROL_CONF_SDMA_REQ_SEL3	RW	32	0x0000 0438	0x4A00 2438
CONTROL_CONF_CLK_SEL0	RW	32	0x0000 0440	0x4A00 2440
CONTROL_CONF_CLK_SEL1	RW	32	0x0000 0444	0x4A00 2444
CONTROL_CONF_CLK_SEL2	RW	32	0x0000 0448	0x4A00 2448
CONTROL_CONF_DPLL_FREQLOCK_SEL	RW	32	0x0000 044C	0x4A00 244C
CONTROL_CONF_DPLL_TINITZ_SEL	RW	32	0x0000 0450	0x4A00 2450
CONTROL_CONF_DPLL_PHASELOCK_SEL	RW	32	0x0000 0454	0x4A00 2454
RESERVED	RW	32	0x0000 0458	0x4A00 2458
CONTROL_CONF_DPLL_TENABLE_SEL	RW	32	0x0000 045C	0x4A00 245C
CONTROL_CONF_DPLL_TENABLEDIV_SEL	RW	32	0x0000 0460	0x4A00 2460
CONTROL_CONF_DPLL_BYPASSACK_SEL	RW	32	0x0000 0464	0x4A00 2464
CONTROL_CONF_DPLL_IDLE_SEL	RW	32	0x0000 0468	0x4A00 2468
CONTROL_CORE_CONF_DEBUG_SEL_TST_0	RW	32	0x0000 0480	0x4A00 2480
CONTROL_CORE_CONF_DEBUG_SEL_TST_1	RW	32	0x0000 0484	0x4A00 2484
CONTROL_CORE_CONF_DEBUG_SEL_TST_2	RW	32	0x0000 0488	0x4A00 2488
CONTROL_CORE_CONF_DEBUG_SEL_TST_3	RW	32	0x0000 048C	0x4A00 248C
CONTROL_CORE_CONF_DEBUG_SEL_TST_4	RW	32	0x0000 0490	0x4A00 2490
CONTROL_CORE_CONF_DEBUG_SEL_TST_5	RW	32	0x0000 0494	0x4A00 2494
CONTROL_CORE_CONF_DEBUG_SEL_TST_6	RW	32	0x0000 0498	0x4A00 2498
CONTROL_CORE_CONF_DEBUG_SEL_TST_7	RW	32	0x0000 049C	0x4A00 249C
CONTROL_CORE_CONF_DEBUG_SEL_TST_8	RW	32	0x0000 04A0	0x4A00 24A0
CONTROL_CORE_CONF_DEBUG_SEL_TST_9	RW	32	0x0000 04A4	0x4A00 24A4
CONTROL_CORE_CONF_DEBUG_SEL_TST_10	RW	32	0x0000 04A8	0x4A00 24A8
CONTROL_CORE_CONF_DEBUG_SEL_TST_11	RW	32	0x0000 04AC	0x4A00 24AC
CONTROL_CORE_CONF_DEBUG_SEL_TST_12	RW	32	0x0000 04B0	0x4A00 24B0
CONTROL_CORE_CONF_DEBUG_SEL_TST_13	RW	32	0x0000 04B4	0x4A00 24B4
CONTROL_CORE_CONF_DEBUG_SEL_TST_14	RW	32	0x0000 04B8	0x4A00 24B8
CONTROL_CORE_CONF_DEBUG_SEL_TST_15	RW	32	0x0000 04BC	0x4A00 24BC
CONTROL_CORE_CONF_DEBUG_SEL_TST_16	RW	32	0x0000 04C0	0x4A00 24C0

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Table 18-111. SYSCTRL_GENERAL_CORE Register Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	SYSCTRL_GENERAL_CORE Physical Address
CONTROL_CORE_CONF_DEBUG_SEL_TST_17	RW	32	0x0000 04C4	0x4A00 24C4
CONTROL_CORE_CONF_DEBUG_SEL_TST_18	RW	32	0x0000 04C8	0x4A00 24C8
CONTROL_CORE_CONF_DEBUG_SEL_TST_19	RW	32	0x0000 04CC	0x4A00 24CC
CONTROL_CORE_CONF_DEBUG_SEL_TST_20	RW	32	0x0000 04D0	0x4A00 24D0
CONTROL_CORE_CONF_DEBUG_SEL_TST_21	RW	32	0x0000 04D4	0x4A00 24D4
CONTROL_CORE_CONF_DEBUG_SEL_TST_22	RW	32	0x0000 04D8	0x4A00 24D8
CONTROL_CORE_CONF_DEBUG_SEL_TST_23	RW	32	0x0000 04DC	0x4A00 24DC
CONTROL_CORE_CONF_DEBUG_SEL_TST_24	RW	32	0x0000 04E0	0x4A00 24E0
CONTROL_CORE_CONF_DEBUG_SEL_TST_25	RW	32	0x0000 04E4	0x4A00 24E4
CONTROL_CORE_CONF_DEBUG_SEL_TST_26	RW	32	0x0000 04E8	0x4A00 24E8
CONTROL_CORE_CONF_DEBUG_SEL_TST_27	RW	32	0x0000 04EC	0x4A00 24EC
CONTROL_CORE_CONF_DEBUG_SEL_TST_28	RW	32	0x0000 04F0	0x4A00 24F0
CONTROL_CORE_CONF_DEBUG_SEL_TST_29	RW	32	0x0000 04F4	0x4A00 24F4
CONTROL_CORE_CONF_DEBUG_SEL_TST_30	RW	32	0x0000 04F8	0x4A00 24F8
CONTROL_CORE_CONF_DEBUG_SEL_TST_31	RW	32	0x0000 04FC	0x4A00 24FC

18.6.3 SYSCTRL_GENERAL_CORE Register Description

Table 18-112. CONTROL_GEN_CORE_REVISION

Address Offset	0x0000 0000		
Physical Address	0x4A002000	**Instance**	SYSCTRL_GENERAL_CORE
Description	Control module instance revision identifier		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP Revision	R	See(1)

(1) TI internal data

Table 18-113. Register Call Summary for Register CONTROL_GEN_CORE_REVISION

Control Module Register Manual

- SYSCTRL_GENERAL_CORE Register Summary: [0]

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Table 18-114. CONTROL_GEN_CORE_HWINFO

Address Offset	0x0000 0004		
Physical Address	0x4A002004	**Instance**	SYSCTRL_GENERAL_CORE
Description	Information about the IP module hardware configuration		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IP_HWINFO																															

Bits	Field Name	Description	Type	Reset
31:0	IP_HWINFO	IP-module dependent	R	0x0000 0000

Table 18-115. Register Call Summary for Register CONTROL_GEN_CORE_HWINFO

Control Module Register Manual
- SYSCTRL_GENERAL_CORE Register Summary: [0]

Table 18-116. CONTROL_GEN_CORE_SYSCONFIG

Address Offset	0x0000 0010		
Physical Address	0x4A002010	**Instance**	SYSCTRL_GENERAL_CORE
Description	Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												IP_SYSCONFIG_IDLEMODE		RESERVED	

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0000000
3:2	IP_SYSCONFIG_IDLEMODE	Select the local clock-gating strategy 0x0: Clock is manually gated 0x1: Clock is manually enabled 0x2,0x3: Clock is automatically gated when there is no access to the Control Module through L4-interconnect	RW	0x2
1:0	RESERVED		R	0x0

Table 18-117. Register Call Summary for Register CONTROL_GEN_CORE_SYSCONFIG

Control Module Functional Description
- General Core Control Module Instance: [0]

Control Module Programming Guide
- Global Initialization: [1]

Control Module Register Manual
- SYSCTRL_GENERAL_CORE Register Summary: [2]

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Table 18-118. CONTROL_STD_FUSE_DIE_ID_0

Address Offset	0x0000 0200		
Physical Address	0x4A00 2200	**Instance**	SYSCTRL_GENERAL_CORE
Description	Die ID Register - Part 0. Access conditions. Read: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

Bits	Field Name	Description	Type	Reset
31:0	RESERVED	Reserved	R	Single identifier

Table 18-119. Register Call Summary for Register CONTROL_STD_FUSE_DIE_ID_0

Control Module Register Manual

- SYSCTRL_GENERAL_CORE Register Summary: [0]

Table 18-120. CONTROL_ID_CODE

Address Offset	0x0000 0204		
Physical Address	0x4A00 2204	**Instance**	SYSCTRL_GENERAL_CORE
Description	ID_CODE Key Register Access conditions. Read: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VERSION				RAMP_SYSTEM												TI_IDM															-

Bits	Field Name	Description	Type	Reset
31:28	VERSION	Revision number	R	0x-(1)
27:12	RAMP_SYSTEM	Ramp system number	R	0x-(1)
11:1	TI_IDM	Manufacturer identity(TI)	R	0x17
0	-	Always set to 1	R	0x1

(1) See Section 1.5, *Device Identification*.

Table 18-121. Register Call Summary for Register CONTROL_ID_CODE

Control Module Register Manual

- SYSCTRL_GENERAL_CORE Register Summary: [0]

Table 18-122. CONTROL_STD_FUSE_DIE_ID_1

Address Offset	0x0000 0208		
Physical Address	0x4A00 2208	**Instance**	SYSCTRL_GENERAL_CORE
Description	Die ID Register - Part 1. Access conditions. Read: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

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Bits	Field Name	Description	Type	Reset
31:0	RESERVED	Reserved	R	Single identifier

Table 18-123. Register Call Summary for Register CONTROL_STD_FUSE_DIE_ID_1

Control Module Register Manual
- SYSCTRL_GENERAL_CORE Register Summary: [0]

Table 18-124. CONTROL_STD_FUSE_DIE_ID_2

Address Offset	0x0000 020C		
Physical Address	0x4A00 220C	**Instance**	SYSCTRL_GENERAL_CORE
Description	Die ID Register - Part 2. Access conditions. Read: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

Bits	Field Name	Description	Type	Reset
31:0	RESERVED	Reserved	R	Single identifier

Table 18-125. Register Call Summary for Register CONTROL_STD_FUSE_DIE_ID_2

Control Module Register Manual
- SYSCTRL_GENERAL_CORE Register Summary: [0]

Table 18-126. CONTROL_STD_FUSE_DIE_ID_3

Address Offset	0x0000 0210		
Physical Address	0x4A00 2210	**Instance**	SYSCTRL_GENERAL_CORE
Description	Die ID Register - Part 3. Access conditions. Read: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

Bits	Field Name	Description	Type	Reset
31:0	RESERVED	Reserved	R	Single identifier

Table 18-127. Register Call Summary for Register CONTROL_STD_FUSE_DIE_ID_3

Control Module Register Manual
- SYSCTRL_GENERAL_CORE Register Summary: [0]

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Table 18-128. CONTROL_STD_FUSE_PROD_ID_0

Address Offset	0x0000 0214		
Physical Address	0x4A00 2214	**Instance**	SYSCTRL_GENERAL_CORE
Description	Prod ID Register - Part 0. This register shows the device type. Access conditions. Read: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								DEVICE_TYPE							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Reserved	R	0x-
7:0	DEVICE_TYPE	Define the device type 0xF0 = GP device Other values = Reserved	R	0x-

Table 18-129. Register Call Summary for Register CONTROL_STD_FUSE_PROD_ID_0

Control Module Register Manual

- SYSCTRL_GENERAL_CORE Register Summary: [0]

Table 18-130. CONTROL_STD_FUSE_PROD_ID_1

Address Offset	0x0000 0218		
Physical Address	0x4A00 2218	**Instance**	SYSCTRL_GENERAL_CORE
Description	Prod ID Register - Part 1.This register shows the device type. Access conditions. Read: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														SILICON_TYPE		RESERVED CONTROL_DSIPHY															

Bits	Field Name	Description	Type	Reset
31:18	RESERVED	Reserved	R	0x-
17:16	SILICON_TYPE	Define the silicon performance type [(1)]	R	0x-
15:0	RESERVED	Reserved	R	0x-

(1) For all available values, see Section 1.5, *OMAP4460 Family and Device Identification*, in Chapter 1, *Introduction*.

Table 18-131. Register Call Summary for Register CONTROL_STD_FUSE_PROD_ID_1

Control Module Register Manual

- SYSCTRL_GENERAL_CORE Register Summary: [0]

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Table 18-132. CONTROL_STD_FUSE_USB_CONF

Address Offset	0x0000 021C		
Physical Address	0x4A00 221C	**Instance**	SYSCTRL_GENERAL_CORE
Description	Standard Fuse conf [31:0]. Register shows part of the chip standard eFuse configuration. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
USB_PROD_ID																USB_VENDOR_ID															

Bits	Field Name	Description	Type	Reset
31:16	USB_PROD_ID	USB Product Identification	R	0x0000
15:0	USB_VENDOR_ID	USB Vendor Identification	R	0x0000

Table 18-133. Register Call Summary for Register CONTROL_STD_FUSE_USB_CONF

Control Module Register Manual

- SYSCTRL_GENERAL_CORE Register Summary: [0]

Table 18-134. CONTROL_STD_FUSE_CONF

Address Offset	0x0000 0220		
Physical Address	0x4A00 2220	**Instance**	SYSCTRL_GENERAL_CORE
	SYSCTRL_GENERAL_CORE		
Description	Standard fuse configuration register. The register shows part of the chip eFuse configuration on the L4 interface. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read only		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															STD_FUSE_FACE_DETECT_DISABLE	STD_FUSE_CRYPTO_DISABLE	STD_FUSE_MODEM3G_DISABLE	STD_FUSE_CH_SPEEDUP_DISABLE	STD_FUSE_ROM_HIDE	STD_FUSE_DPLL_CLK_TRIMMING_DISABLE	RESERVED	STD_FUSE_DSS_VENC_MVENAB	STD_FUSE_ISS_EFUSE1_EN	STD_FUSE_ISS_EFUSE2_EN	STD_FUSE_ISS_EFUSE3_EN	STD_FUSE_ISS_EFUSE4_EN	STD_FUSE_SGX540_3D_CLOCK_SOURCE	STD_FUSE_SGX540_3D_DISABLE	STD_FUSE_CORTEXA9_MPU_DISABLE	BSC_ACCESS_PROTECT	CUST_IEEE1500_DISABLE

Bits	Field Name	Description	Type	Reset
31:17	RESERVED	Reserved	R	0x000000
16	STD_FUSE_FACE_DETECT_DISABLE	Disables face detect Read 0x0: Enables face detect	R	0x[1]

[1] The POR value is exported from Fuse-ROM locations, which are programmed during the manufacturing process.

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Bits	Field Name	Description	Type	Reset
		Read 0x1: Disables face detect		
15	STD_FUSE_CRYPTO_DISABLE	Disables cryptographic modules	R	0x-
		Read 0x0: Enables cryptrographic modules		
		Read 0x1: Disables cryptrographic modules		
14	STD_FUSE_MODEM3G_DISABLE	Disables the 3G modem	R	0x-
		Read 0x0: Enables 3G modem		
		Read 0x1: Disables 3G modem		
13	STD_FUSE_CH_SPEEDUP_DISABLE	ROM code settings for configuration header block and speedup block. Only software access (no hardware access).	R	0x-
		Read 0x0: Enables CH and speedup		
		Read 0x1: Disables CH and speedup		
12	STD_FUSE_ROM_HIDE	MPU BOOT ROM space (4-KB ROM code protection)	R	0x-
		Read 0x0: BOOT ROM space is 128KB.		
		Read 0x1: BOOT ROM upper 4-KB region becomes reserved.		
11	STD_FUSE_DPLL_CLK_TRIMMING_DISABLE	Controls DPLLs	R	0x-
		Read 0x0: Enables DPLL trimming		
		Read 0x1: Disables DPLL trimming		
10	RESERVED	Reserved	R	0x-
9	STD_FUSE_DSS_VENC_MVENAB	Enables implementation-specific features. Controls DSS_VENC_MVENAB.	R	0x-
		Read 0x0: Disables DSS_VENC_MVENAB		
		Read 0x1: Enables DSS_VENC_MVENAB		
8	STD_FUSE_ISS_EFUSE1_EN	Enables implementation-specific features. Controls ISS.EFUSE1_EN. Sets to 1.	R	0x1
		Read 0x0: Disables ISS EFUSE1		
		Read 0x1: Enables ISS EFUSE1		
7	STD_FUSE_ISS_EFUSE2_EN	Enables implementation-specific features. Controls ISS.EFUSE2_EN. Sets to 0.	R	0x0
		Read 0x0: Disables ISS EFUSE2		
		Read 0x1: Enables ISS EFUSE2		
6	STD_FUSE_ISS_EFUSE3_EN	Enables implementation specific features. Controls ISS.EFUSE3_EN. Sets to 0.	R	0x0
		Read 0x0: Disables ISS EFUSE3		
		Read 0x1: Enables ISS EFUSE3		
5	STD_FUSE_ISS_EFUSE4_EN	Enables implementation-specific features. Controls ISS.EFUSE4_EN. Sets to 0.	R	0x0
		Read 0x0: Disables ISS EFUSE4		
		Read 0x1: Enables ISS EFUSE4		
4	STD_FUSE_SGX540_3D_CLOCK_SOURCE	Force 3D graphic engine clock source	R	0x-
3	STD_FUSE_SGX540_3D_DISABLE	Disable the 3D Gx engine (SGX540)	R	0x-
		Read 0x0: Enables SGX		
		Read 0x1: Disables SGX		
2	STD_FUSE_CORTEXA9_MPU_DISABLE	Configures Cortex-A9 MPU boot mode. It disables one Cortex-A9 core.	R	0x-
		Read 0x0: Boot SMP mode		
		Read 0x1: Boot IP mode		
1	BSC_ACCESS_PROTECT	Reserved for bsc_access protect	R	0x-

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Bits	Field Name	Description	Type	Reset
0	CUST_IEEE1500_DISABLE	Customer eFuse control/IEEE1500 access path disable	R	0x-

Table 18-135. Register Call Summary for Register CONTROL_STD_FUSE_CONF

Control Module Register Manual
- SYSCTRL_GENERAL_CORE Register Summary: [0]

Table 18-136. CONTROL_STD_FUSE_OPP_VDD_WKUP

Address Offset	0x0000 0228		
Physical Address	0x4A00 2228	**Instance**	SYSCTRL_GENERAL_CORE
Description	Standard Fuse OPP VDD_WKUP [31:0]. Register shows part of the chip standard eFuse configuration. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STD_FUSE_OPP_VDD_WKUP																															

Bits	Field Name	Description	Type	Reset
31:0	STD_FUSE_OPP_VDD_WKUP		R	0x0000 0000

Table 18-137. Register Call Summary for Register CONTROL_STD_FUSE_OPP_VDD_WKUP

Control Module Register Manual
- SYSCTRL_GENERAL_CORE Register Summary: [0]

Table 18-138. CONTROL_STD_FUSE_OPP_VDD_IVA_0

Address Offset	0x0000 022C		
Physical Address	0x4A00 222C	**Instance**	SYSCTRL_GENERAL_CORE
Description	Standard Fuse OPP VDD_IVA_0. Register shows part of the chip eFuse configuration on the L4 interface. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VDD_IVA_OPP100_SENN_REC								VDD_IVA_OPP50_SENP_GAIN				VDD_IVA_OPP50_SENN_GAIN				VDD_IVA_OPP50_SENP_REC								VDD_IVA_OPP50_SENN_REC							

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Bits	Field Name	Description	Type	Reset
31:24	VDD_IVA_OPP100_SENN_REC	Voltage domain VDD_IVA OPP100 [7:0] from Standard Fuse	R	0x00
23:20	VDD_IVA_OPP50_SENP_GAIN	Voltage domain VDD_IVA OPP50 [23:20] from Standard Fuse	R	0x0
19:16	VDD_IVA_OPP50_SENN_GAIN	Voltage domain VDD_IVA OPP50 [19:16] from Standard Fuse	R	0x0
15:8	VDD_IVA_OPP50_SENP_REC	Voltage domain VDD_IVA OPP50 [15:8] from Standard Fuse	R	0x00
7:0	VDD_IVA_OPP50_SENN_REC	Voltage domain VDD_IVA OPP50 [7:0] from Standard Fuse	R	0x00

Table 18-139. Register Call Summary for Register CONTROL_STD_FUSE_OPP_VDD_IVA_0

Control Module Register Manual
- SYSCTRL_GENERAL_CORE Register Summary: [0]

Table 18-140. CONTROL_STD_FUSE_OPP_VDD_IVA_1

Address Offset	0x0000 0230		
Physical Address	0x4A00 2230	**Instance**	SYSCTRL_GENERAL_CORE
Description	Standard Fuse OPP VDD_IVA_1. Register shows part of the chip eFuse configuration on the L4 interface. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
VDD_IVA_OPP_TURBO_SENP_REC	DD_IVA_OPP_TURBO_SENN_REC	VDD_IVA_OPP100_SENP_GAIN / VDD_IVA_OPP100_SENN_GAIN	VDD_IVA_OPP100_SENP_REC

Bits	Field Name	Description	Type	Reset
31:24	VDD_IVA_OPP_TURBO_SENP_REC	Voltage domain VDD_IVA OPP_TURBO [15:8] from Standard Fuse	R	0x00
23:16	VDD_IVA_OPP_TURBO_SENN_REC	Voltage domain VDD_IVA OPP_TURBO [7:0] from Standard Fuse	R	0x00
15:12	VDD_IVA_OPP100_SENP_GAIN	Voltage domain VDD_IVA OPP100 [23:20] from Standard Fuse	R	0x0
11:8	VDD_IVA_OPP100_SENN_GAIN	Voltage domain VDD_IVA OPP100 [19:16] from Standard Fuse	R	0x0
7:0	VDD_IVA_OPP100_SENP_REC	Voltage domain VDD_IVA OPP100 [15:8] from Standard Fuse	R	0x00

Table 18-141. Register Call Summary for Register CONTROL_STD_FUSE_OPP_VDD_IVA_1

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- SYSCTRL_GENERAL_CORE Register Summary: [0]

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Table 18-142. CONTROL_STD_FUSE_OPP_VDD_IVA_2

Address Offset	0x0000 0234		
Physical Address	0x4A00 2234	**Instance**	SYSCTRL_GENERAL_CORE
Description	Standard Fuse OPP VDD_IVA_2. Register shows part of the chip eFuse configuration on the L4 interface. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31 30 29 28	27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4	3 2 1 0
VDD_IVA_OPP_NITRO_SENP_GAIN	VDD_IVA_OPP_NITRO_SENN_GAIN	VDD_IVA_OPP_NITRO_SENP_REC	VDD_IVA_OPP_NITRO_SENN_REC	VDD_IVA_OPP_TURBO_SENP_GAIN	VDD_IVA_OPP_TURBO_SENN_GAIN

Bits	Field Name	Description	Type	Reset
31:28	VDD_IVA_OPP_NITRO_SENP_GAIN	Voltage domain VDD_IVA OPP_NITRO[23:20] from Standard Fuse	R	0x0
27:24	VDD_IVA_OPP_NITRO_SENN_GAIN	Voltage domain VDD_IVA OPP_NITRO[19:16] from Standard Fuse	R	0x0
23:16	VDD_IVA_OPP_NITRO_SENP_REC	Voltage domain VDD_IVA OPP_NITRO[15:8] from Standard Fuse	R	0x00
15:8	VDD_IVA_OPP_NITRO_SENN_REC	Voltage domain VDD_IVA OPP_NITRO[7:0] from Standard Fuse	R	0x00
7:4	VDD_IVA_OPP_TURBO_SENP_GAIN	Voltage domain VDD_IVA OPP_TURBO[23:20] from Standard Fuse	R	0x0
3:0	VDD_IVA_OPP_TURBO_SENN_GAIN	Voltage domain VDD_IVA OPP_TURBO[19:16] from Standard Fuse	R	0x0

Table 18-143. Register Call Summary for Register CONTROL_STD_FUSE_OPP_VDD_IVA_2

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- SYSCTRL_GENERAL_CORE Register Summary: [0]

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Table 18-144. CONTROL_STD_FUSE_OPP_VDD_IVA_3

Address Offset	0x0000 0238		
Physical Address	0x4A00 2238	**Instance**	SYSCTRL_GENERAL_CORE
Description	Standard Fuse OPP VDD_IVA_3. Register shows part of the chip eFuse configuration on the L4 interface. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31 30 29 28	27 26	25 24	23 22 21 20	19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
RESERVED	VDD_IVA_SR_SENN	VDD_IVA_SR_SENP	VDD_IVA_OPP_NITROSB_SENP_GAIN	VDD_IVA_OPP_NITROSB_SENN_GAIN	VDD_IVA_OPP_NITROSB_SENP_REC	VDD_IVA_OPP_NITROSB_SENN_REC

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:26	VDD_IVA_SR_SENN	VDD_IVA SmartReflex from Standard Fuse	R	0x0
25:24	VDD_IVA_SR_SENP	VDD_IVA SmartReflex from Standard Fuse	R	0x0
23:20	VDD_IVA_OPP_NTSB_SENP_GAIN	Voltage domain VDD_IVA OPP_NTSB[23:20] from Standard Fuse	R	0x0
19:16	VDD_IVA_OPP_NTSB_SENN_GAIN	Voltage domain VDD_IVA OPP_NTSB[19:16] from Standard Fuse	R	0x0
15:8	VDD_IVA_OPP_NTSB_SENP_REC	Voltage domain VDD_IVA OPP_NTSB[15:8] from Standard Fuse	R	0x00
7:0	VDD_IVA_OPP_NTSB_SENN_REC	Voltage domain VDD_IVA OPP_NTSB[7:0] from Standard Fuse	R	0x00

Table 18-145. Register Call Summary for Register CONTROL_STD_FUSE_OPP_VDD_IVA_3

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- SYSCTRL_GENERAL_CORE Register Summary: [0]

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Table 18-146. CONTROL_STD_FUSE_OPP_VDD_MPU_0

Address Offset	0x0000 0240		
Physical Address	0x4A00 2240	**Instance**	SYSCTRL_GENERAL_CORE
Description	Standard Fuse OPP VDD_MPU_0. Register shows part of the chip eFuse configuration on the L4 interface. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16		15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
VDD_MPU_OPP100_SENN_REC	VDD_MPU_OPP50_SENP_GAIN	VDD_MPU_OPP50_SENN_GAIN	VDD_MPU_OPP50_SENP_REC	VDD_MPU_OPP50_SENN_REC

Bits	Field Name	Description	Type	Reset
31:24	VDD_MPU_OPP100_SENN_REC	Voltage domain VDD_MPU OPP100[7:0] from Standard Fuse	R	0x00
23:20	VDD_MPU_OPP50_SENP_GAIN	Voltage domain VDD_MPU OPP50[23:20] from Standard Fuse	R	0x0
19:16	VDD_MPU_OPP50_SENN_GAIN	Voltage domain VDD_MPU OPP50[19:16] from Standard Fuse	R	0x0
15:8	VDD_MPU_OPP50_SENP_REC	Voltage domain VDD_MPU OPP50[15:8] from Standard Fuse	R	0x00
7:0	VDD_MPU_OPP50_SENN_REC	Voltage domain VDD_MPU OPP50[7:0] from Standard Fuse	R	0x00

Table 18-147. Register Call Summary for Register CONTROL_STD_FUSE_OPP_VDD_MPU_0

Control Module Register Manual

- SYSCTRL_GENERAL_CORE Register Summary: [0]

Table 18-148. CONTROL_STD_FUSE_OPP_VDD_MPU_1

Address Offset	0x0000 0244		
Physical Address	0x4A00 2244	**Instance**	SYSCTRL_GENERAL_CORE
Description	Standard Fuse OPP VDD_MPU_1. Register shows part of the chip eFuse configuration on the L4 interface. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

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31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
VDD_MPU_OPP_TURBO_SENP_REC	VDD_MPU_OPP_TURBO_SENN_REC	VDD_MPU_OPP100_SENP_GAIN / VDD_MPU_OPP100_SENN_GAIN	VDD_MPU_OPP100_SENP_REC

Bits	Field Name	Description	Type	Reset
31:24	VDD_MPU_OPP_TURBO_SENP_REC	Voltage domain VDD_MPU OPP_TURBO[15:8] from Standard Fuse	R	0x00
23:16	VDD_MPU_OPP_TURBO_SENN_REC	Voltage domain VDD_MPU OPP_TURBO[7:0] from Standard Fuse	R	0x00
15:12	VDD_MPU_OPP100_SENP_GAIN	Voltage domain VDD_MPU OPP100[23:20] from Standard Fuse	R	0x0
11:8	VDD_MPU_OPP100_SENN_GAIN	Voltage domain VDD_MPU OPP100[19:16] from Standard Fuse	R	0x0
7:0	VDD_MPU_OPP100_SENP_REC	Voltage domain VDD_MPU OPP100[15:8] from Standard Fuse	R	0x00

Table 18-149. Register Call Summary for Register CONTROL_STD_FUSE_OPP_VDD_MPU_1

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- SYSCTRL_GENERAL_CORE Register Summary: [0]

Table 18-150. CONTROL_STD_FUSE_OPP_VDD_MPU_2

Address Offset	0x0000 0248		
Physical Address	0x4A00 2248	**Instance**	SYSCTRL_GENERAL_CORE
Description	Standard Fuse OPP VDD_MPU_2. Register shows part of the chip eFuse configuration on the L4 interface. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31 30 29 28	27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4	3 2 1 0
VDD_MPU_OPP_NITRO_SENP_GAIN	VDD_MPU_OPP_NITRO_SENN_GAIN	VDD_MPU_OPP_NITRO_SENP_REC	VDD_MPU_OPP_NITRO_SENN_REC	VDD_MPU_OPP_TURBO_SENP_GAIN	VDD_MPU_OPP_TURBO_SENN_GAIN

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Bits	Field Name	Description	Type	Reset
31:28	VDD_MPU_OPP_NITRO_SENP_GAIN	Voltage domain VDD_MPU OPP_NITRO[23:20] from Standard Fuse	R	0x0
27:24	VDD_MPU_OPP_NITRO_SENN_GAIN	Voltage domain VDD_MPU OPP_NITRO[19:16] from Standard Fuse	R	0x0
23:16	VDD_MPU_OPP_NITRO_SENP_REC	Voltage domain VDD_MPU OPP_NITRO[15:8] from Standard Fuse	R	0x00
15:8	VDD_MPU_OPP_NITRO_SENN_REC	Voltage domain VDD_MPU OPP_NITRO[7:0] from Standard Fuse	R	0x00
7:4	VDD_MPU_OPP_TURBO_SENP_GAIN	Voltage domain VDD_MPU OPP_TURBO[23:20] from Standard Fuse	R	0x0
3:0	VDD_MPU_OPP_TURBO_SENN_GAIN	Voltage domain VDD_MPU OPP_TURBO[19:16] from Standard Fuse	R	0x0

Table 18-151. Register Call Summary for Register CONTROL_STD_FUSE_OPP_VDD_MPU_2

Control Module Register Manual

- SYSCTRL_GENERAL_CORE Register Summary: [0]

Table 18-152. CONTROL_STD_FUSE_OPP_VDD_MPU_3

Address Offset	0x0000 024C		
Physical Address	0x4A00 224C	**Instance**	SYSCTRL_GENERAL_CORE
Description	Standard Fuse OPP VDD_MPU_3. Register shows part of the chip eFuse configuration on the L4 interface. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31 30 29 28	27 26	25 24	23 22 21 20	19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
RESERVED	VDD_MPU_SR_SENN	VDD_MPU_SR_SENP	VDD_MPU_OPP_NITROSB_SENP_GAIN	VDD_MPU_OPP_NITROSB_SENN_GAIN	VDD_MPU_OPP_NITROSB_SENP_REC	VDD_MPU_OPP_NITROSB_SENN_REC

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:26	VDD_MPU_SR_SENN	VDD_MPU SmartReflex from Standard Fuse	R	0x0
25:24	VDD_MPU_SR_SENP	VDD_MPU SmartReflex from Standard Fuse	R	0x0
23:20	VDD_MPU_OPP_NTSB_SENP_GAIN	Voltage domain VDD_MPU OPP_NTSB[23:20] from Standard Fuse	R	0x0
19:16	VDD_MPU_OPP_NTSB_SENN_GAIN	Voltage domain VDD_MPU OPP_NTSB[19:16] from Standard Fuse	R	0x0
15:8	VDD_MPU_OPP_NTSB_SENP_REC	Voltage domain VDD_MPU OPP_NTSB[15:8] from Standard Fuse	R	0x00
7:0	VDD_MPU_OPP_NTSB_SENN_REC	Voltage domain VDD_MPU OPP_NTSB[7:0] from Standard Fuse	R	0x00

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Table 18-153. Register Call Summary for Register CONTROL_STD_FUSE_OPP_VDD_MPU_3

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- SYSCTRL_GENERAL_CORE Register Summary: [0]

Table 18-154. CONTROL_STD_FUSE_OPP_VDD_CORE_0

Address Offset	0x0000 0254		
Physical Address	0x4A00 2254	**Instance**	SYSCTRL_GENERAL_CORE
Description	Standard Fuse OPP VDD_CORE_0. Register shows part of the chip eFuse configuration on the L4 interface. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
VDD_CORE_OPP100_SENN_REC	VDD_CORE_OPP50_SENP_GAIN / VDD_CORE_OPP50_SENN_GAIN	VDD_CORE_OPP50_SENP_REC	VDD_CORE_OPP50_SENN_REC

Bits	Field Name	Description	Type	Reset
31:24	VDD_CORE_OPP100_SENN_REC	Voltage domain VDD_CORE OPP100[7:0] from Standard Fuse	R	0x00
23:20	VDD_CORE_OPP50_SENP_GAIN	Voltage domain VDD_CORE OPP50 23:20] from Standard Fuse	R	0x0
19:16	VDD_CORE_OPP50_SENN_GAIN	Voltage domain VDD_CORE OPP50[19:16] from Standard Fuse	R	0x0
15:8	VDD_CORE_OPP50_SENP_REC	Voltage domain VDD_CORE OPP50[15:8] from Standard Fuse	R	0x00
7:0	VDD_CORE_OPP50_SENN_REC	Voltage domain VDD_CORE OPP50[7:0] from Standard Fuse	R	0x00

Table 18-155. Register Call Summary for Register CONTROL_STD_FUSE_OPP_VDD_CORE_0

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- SYSCTRL_GENERAL_CORE Register Summary: [0]

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Table 18-156. CONTROL_STD_FUSE_OPP_VDD_CORE_1

Address Offset	0x0000 0258		
Physical Address	0x4A00 2258	**Instance**	SYSCTRL_GENERAL_CORE
Description	Standard Fuse OPP VDD_CORE_1. Register shows part of the chip eFuse configuration on the L4 interface. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
VDD_CORE_OPP119_SENP_REC	VDD_CORE_OPP119_SENN_REC	VDD_CORE_OPP100_SENP_GAIN, VDD_CORE_OPP100_SENN_GAIN	VDD_CORE_OPP100_SENP_REC

Bits	Field Name	Description	Type	Reset
31:24	VDD_CORE_OPP119_SENP_REC	Voltage domain VDD_CORE OPP119[15:8] from Standard Fuse (overdrive mode)	R	0x00
23:16	VDD_CORE_OPP119_SENN_REC	Voltage domain VDD_CORE OPP119[7:0] from Standard Fuse (overdrive mode)	R	0x00
15:12	VDD_CORE_OPP100_SENP_GAIN	Voltage domain VDD_CORE OPP100[23:20] from Standard Fuse	R	0x0
11:8	VDD_CORE_OPP100_SENN_GAIN	Voltage domain VDD_CORE OPP100[19:16] from Standard Fuse	R	0x0
7:0	VDD_CORE_OPP100_SENP_REC	Voltage domain VDD_CORE OPP100[15:8] from Standard Fuse	R	0x00

Table 18-157. Register Call Summary for Register CONTROL_STD_FUSE_OPP_VDD_CORE_1

Control Module Register Manual

- SYSCTRL_GENERAL_CORE Register Summary: [0]

Table 18-158. CONTROL_STD_FUSE_OPP_VDD_CORE_2

Address Offset	0x0000 025C		
Physical Address	0x4A00 225C	**Instance**	SYSCTRL_GENERAL_CORE
Description	Standard Fuse OPP VDD_CORE_2. Register shows part of the chip eFuse configuration on the L4 interface. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				VDD_CORE_SR_SENN		VDD_CORE_SR_SENP		VDD_CORE_OPP119_SENP_GAIN				VDD_CORE_OPP119_SENN_GAIN			

Bits	Field Name	Description	Type	Reset
31:12	RESERVED		R	0x00000
11:10	VDD_CORE_SR_SENN	VDD_CORE SmartReflex from Standard Fuse	R	0x0
9:8	VDD_CORE_SR_SENP	VDD_CORE SmartReflex from Standard Fuse	R	0x0
7:4	VDD_CORE_OPP119_SENP_GAIN	Voltage domain VDD_CORE OPP119[23:20] from Standard Fuse (overdrive mode)	R	0x0
3:0	VDD_CORE_OPP119_SENN_GAIN	Voltage domain VDD_CORE OPP119[19:16] from Standard Fuse (overdrive mode)	R	0x0

Table 18-159. Register Call Summary for Register CONTROL_STD_FUSE_OPP_VDD_CORE_2

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- SYSCTRL_GENERAL_CORE Register Summary: [0]

Table 18-160. CONTROL_STD_FUSE_OPP_BGAP

Address Offset	0x0000 0260		
Physical Address	0x4A00 2260	**Instance**	SYSCTRL_GENERAL_CORE
Description	Standard Fuse OPP BGAP. Register shows part of the chip standard eFuse configuration. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STD_FUSE_OPP_BGAP																															

Bits	Field Name	Description	Type	Reset
31:0	STD_FUSE_OPP_BGAP		R	0x0000 0000

Table 18-161. Register Call Summary for Register CONTROL_STD_FUSE_OPP_BGAP

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- SYSCTRL_GENERAL_CORE Register Summary: [0]

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Table 18-162. CONTROL_STD_FUSE_OPP_DPLL_0

Address Offset	0x0000 0264		
Physical Address	0x4A00 2264	**Instance**	SYSCTRL_GENERAL_CORE
Description	Standard Fuse OPP DPLL. Register shows part of the chip standard eFuse configuration. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STD_FUSE_OPP_DPLL_0																															

Bits	Field Name	Description	Type	Reset
31:0	STD_FUSE_OPP_DPLL_0		R	0x0000 0000

Table 18-163. Register Call Summary for Register CONTROL_STD_FUSE_OPP_DPLL_0

Control Module Register Manual

- SYSCTRL_GENERAL_CORE Register Summary: [0]

Table 18-164. CONTROL_STD_FUSE_OPP_DPLL_1

Address Offset	0x0000 0268		
Physical Address	0x4A00 2268	**Instance**	SYSCTRL_GENERAL_CORE
Description	Standard Fuse OPP DPLL. Register shows part of the chip standard eFuse configuration. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STD_FUSE_OPP_DPLL_1																															

Bits	Field Name	Description	Type	Reset
31:0	STD_FUSE_OPP_DPLL_1		R	0x0000 0000

Table 18-165. Register Call Summary for Register CONTROL_STD_FUSE_OPP_DPLL_1

Control Module Register Manual

- SYSCTRL_GENERAL_CORE Register Summary: [0]

Table 18-166. CONTROL_STATUS

Address Offset	0x0000 02C4		
Physical Address	0x4A00 22C4	**Instance**	SYSCTRL_GENERAL_CORE
Description	Control Module Status Register Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																			SYSCTRL_GENERAL_CONF		DEVICE_TYPE				SYS_BOOT							

Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000
12:11	SYSCTRL_GENERAL_CONF	Sysctrl_General_ IP configuration Read 0x1: SMP configuration	R	0x0
10:8	DEVICE_TYPE	Device type captured at reset time Device type value sampled at power-on reset. Read 0x3: General Purpose (GP)	R	0x0
7:0	SYS_BOOT	Sys.Boot pins state captured at reset time Sys.Boot pin values sampled at power-on reset	R	0x00

Table 18-167. Register Call Summary for Register CONTROL_STATUS

Control Module Integration • Control Module Integration: [0]
Control Module Functional Description • Control Module Initialization: [1] • General Core Control Module Instance: [2]
Control Module Register Manual • SYSCTRL_GENERAL_CORE Register Summary: [3]

Table 18-168. CONTROL_SEC_ERR_STATUS_FUNC

Address Offset	0x0000 02D0		
Physical Address	0x4A00 22D0	**Instance**	SYSCTRL_GENERAL_CORE
Description	Firewall Error Status functional Register Access conditions. Read Only		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											C2C_INIT_FW_ERROR	L4_AUDIOBE_FW_ERROR	DEBUGSS_FW_ERROR	L4_CONFIG_FW_ERROR	L4_PERIPH_FW_ERROR	ISS_FW_ERROR	DSS_FW_ERROR	SGX_FW_ERROR	C2C_FW_ERROR	RESERVED				SL2_FW_ERROR	DUAL_CORTEX_M3_FW_ERROR	IVAHD_FW_ERROR	EMIF_FW_ERROR	GPMC_FW_ERROR	L3RAM_FW_ERROR	RESERVED	

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Bits	Field Name	Description	Type	Reset
31:21	RESERVED		R	0x000
20	C2C_INIT_FW_ERROR	C2C init firewall. MID config: unused (reserved) 0x0: No error from firewall 0x1: Error from firewall	R	0
19	L4_AUDIOBE_FW_ERROR	L4 AudioBE firewall 0x0: No error from firewall 0x1: Error from firewall	R	0
18	DEBUGSS_FW_ERROR	DebugSS firewall 0x0: No error from firewall 0x1: Error from firewall	R	0
17	L4_CONFIG_FW_ERROR	L4 Config firewall 0x0: No error from firewall 0x1: Error from firewall	R	0
16	L4_PERIPH_FW_ERROR	L4 PER firewall 0x0: No error from firewall 0x1: Error from firewall	R	0
15	ISS_FW_ERROR	ISS firewall 0x0: No error from firewall 0x1: Error from firewall	R	0
14	DSS_FW_ERROR	DSS firewall 0x0: No error from firewall 0x1: Error from firewall	R	0
13	SGX_FW_ERROR	SGX firewall 0x0: No error from firewall 0x1: Error from firewall	R	0
12	C2C_FW_ERROR	C2C firewall. MID config: unused (reserved). 0x0: No error from firewall 0x1: Error from firewall	R	0
11: 7	RESERVED	Reserved	R	0
6	SL2_FW_ERROR	SL2 firewall 0x0: No error from firewall 0x1: Error from firewall	R	0
5	DUAL_CORTEX_M3_FW_ERROR	Dual Cortex M3 firewall 0x0: No error from firewall 0x1: Error from firewall	R	0
4	IVAHD_FW_ERROR	IVAHD firewall 0x0: No error from firewall 0x1: Error from firewall	R	0
3	EMIF_FW_ERROR	EMIF firewall 0x0: No error from firewall 0x1: Error from firewall	R	0
2	GPMC_FW_ERROR	GPMC firewall 0x0: No error from firewall 0x1: Error from firewall	R	0
1	L3RAM_FW_ERROR	L3RAM firewall 0x0: No error from firewall 0x1: Error from firewall	R	0
0	RESERVED	Reserved	R	0

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Table 18-169. Register Call Summary for Register CONTROL_SEC_ERR_STATUS_FUNC

Control Module Functional Description

- Protection Status Registers: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15]

Control Module Register Manual

- SYSCTRL_GENERAL_CORE Register Summary: [16]

Table 18-170. CONTROL_SEC_ERR_STATUS_DEBUG

Address Offset	0x0000 02D4		
Physical Address	0x4A00 22D4	**Instance**	SYSCTRL_GENERAL_CORE
Description	Error Status debug Register. Read All / Write All. Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											C2C_INIT_DBGFW_ERROR	L4_AUDIOBE_DBGFW_ERROR	DEBUGSS_DBGFW_ERROR	L4_CONFIG_DBGFW_ERROR	L4_PERIPH_DBGFW_ERROR	ISS_DBGFW_ERROR	DSS_DBGFW_ERROR	SGX_DBGFW_ERROR	C2C_DBGFW_ERROR	RESERVED				SL2_DBGFW_ERROR	DUAL_CORTEX_M3_DBGFW_ERROR	IVAHD_DBGFW_ERROR	EMIF_DBGFW_ERROR	GPMC_DBGFW_ERROR	L3RAM_DBGFW_ERROR	RESERVED	

Bits	Field Name	Description	Type	Reset
31:21	RESERVED		R	0x000
20	C2C_INIT_DBGFW_ERROR	C2C init debug firewall. MID config: unused (reserved) 0x0: No error from firewall 0x1: Error from firewall	R	0
19	L4_AUDIOBE_DBGFW_ERROR	L4 AudioBE debug firewall 0x0: No error from firewall 0x1: Error from firewall	R	0
18	DEBUGSS_DBGFW_ERROR	DebugSS debug firewall 0x0: No error from firewall 0x1: Error from firewall	R	0
17	L4_CONFIG_DBGFW_ERROR	L4 Config debug firewall 0x0: No error from firewall 0x1: Error from firewall	R	0
16	L4_PERIPH_DBGFW_ERROR	L4 PER debug firewall 0x0: No error from firewall 0x1: Error from firewall	R	0
15	ISS_DBGFW_ERROR	ISS debug firewall 0x0: No error from firewall 0x1: Error from firewall	R	0
14	DSS_DBGFW_ERROR	DSS debug firewall 0x0: No error from firewall 0x1: Error from firewall	R	0

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Bits	Field Name	Description	Type	Reset
13	SGX_DBGFW_ERROR	SGX debug firewall 0x0: No error from firewall 0x1: Error from firewall	R	0
12	C2C_DBGFW_ERROR	C2C debug firewall. MID config: unused (reserved). 0x0: No error from firewall 0x1: Error from firewall	R	0
11:7	RESERVED	Reserved	R	0
6	SL2_DBGFW_ERROR	SL2 debug firewall 0x0: No error from firewall 0x1: Error from firewall	R	0
5	DUAL_CORTEX_M3_ DBGFW_ERROR	Dual Cortex M3 debug firewall 0x0: No error from firewall 0x1: Error from firewall	R	0
4	IVAHD_DBGFW_ERROR	IVAHD debug firewall 0x0: No error from firewall 0x1: Error from firewall	R	0
3	EMIF_DBGFW_ERROR	EMIF debug firewall 0x0: No error from firewall 0x1: Error from firewall	R	0
2	GPMC_DBGFW_ERROR	GPMC debug firewall 0x0: No error from firewall 0x1: Error from firewall	R	0
1	L3RAM_DBGFW_ERROR	L3RAM debug firewall 0x0: No error from firewall 0x1: Error from firewall	R	0
0	RESERVED	Reserved	R	0

Table 18-171. Register Call Summary for Register CONTROL_SEC_ERR_STATUS_DEBUG

Control Module Functional Description • Protection Status Registers: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15]
Control Module Register Manual • SYSCTRL_GENERAL_CORE Register Summary: [16]

Table 18-172. CONTROL_DEV_CONF

Address Offset	0x0000 0300		
Physical Address	0x4A00 2300	**Instance**	SYSCTRL_GENERAL_CORE
Description	Device configuration register. Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DEV_CONF																															USBPHY_PD

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Bits	Field Name	Description	Type	Reset
31:1	DEV_CONF	Spare bits for device configuration.	RW	0x0000 0000
0	USBPHY_PD	Power down entire USB phy (data, common module and UTMI). controls USB2PHYCORE.PD pin. 0x0: Normal operation 0x1: Power down the USB PHY	RW	0

Table 18-173. Register Call Summary for Register CONTROL_DEV_CONF

Control Module Register Manual

- SYSCTRL_GENERAL_CORE Register Summary: [0]

Table 18-174. CONTROL_LDOVBB_IVA_VOLTAGE_CTRL

Address Offset	0x0000 0314		
Physical Address	0x4A00 2314	**Instance**	SYSCTRL_GENERAL_CORE
Description	IVA Voltage Body Bias LDO control register Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					RESERVED			RESERVED								RESERVED						LDOVBBIVA_FBB_MUX_CTRL			LDOVBBIVA_FBB_VSET_IN					LDOVBBIVA_FBB_VSET_OUT					

Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Reserved	R	0x00
26	RESERVED	Reserved	RW	0
25:21	RESERVED	Reserved	R	0x00
20:16	RESERVED	Reserved	RW	0x00
15:11	RESERVED	Reserved	R	0x00
10	LDOVBBIVA_FBB_MUX_CTRL	Override control of EFUSE Forward Body Bias voltage value 0x0: efuse value is used 0x1: override value is used	RW	0
9:5	LDOVBBIVA_FBB_VSET_IN	EFUSE Forward Body Bias voltage value	R	0x00
4:0	LDOVBBIVA_FBB_VSET_OUT	Override value for Forward Body Bias voltage	RW	0x00

Table 18-175. Register Call Summary for Register CONTROL_LDOVBB_IVA_VOLTAGE_CTRL

Control Module Register Manual

- SYSCTRL_GENERAL_CORE Register Summary: [0]

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Table 18-176. CONTROL_LDOVBB_MPU_VOLTAGE_CTRL

Address Offset	0x0000 0318		
Physical Address	0x4A00 2318	**Instance**	SYSCTRL_GENERAL_CORE
Description	MPU Voltage Body Bias LDO control register Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					RESERVED			RESERVED								RESERVED						LDOVBBMPU_FBB_MUX_CTRL			LDOVBBMPU_FBB_VSET_IN					LDOVBBMPU_FBB_VSET_OUT					

Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Reserved	R	0x00
26	RESERVED	Reserved	RW	0
25:21	RESERVED	Reserved	R	0x00
20:16	RESERVED	Reserved	RW	0x00
15:11	RESERVED	Reserved	R	0x00
10	LDOVBBMPU_FBB_MUX_CTRL	Override control of EFUSE Forward Body Bias voltage value 0x0: efuse value is used 0x1: override value is used	RW	0
9:5	LDOVBBMPU_FBB_VSET_IN	EFUSE Forward Body Bias voltage value	R	0x00
4:0	LDOVBBMPU_FBB_VSET_OUT	Override value for Forward Body Bias voltage	RW	0x00

Table 18-177. Register Call Summary for Register CONTROL_LDOVBB_MPU_VOLTAGE_CTRL

Control Module Register Manual
- SYSCTRL_GENERAL_CORE Register Summary: [0]

Table 18-178. CONTROL_LDOSRAM_IVA_VOLTAGE_CTRL

Address Offset	0x0000 0320		
Physical Address	0x4A00 2320	**Instance**	SYSCTRL_GENERAL_CORE
Description	IVA SRAM LDO control register Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					LDOSRAMIVA_RETMODE_MUX_CTRL	LDOSRAMIVA_RETMODE_VSET_IN					LDOSRAMIVA_RETMODE_VSET_OUT					RESERVED					LDOSRAMIVA_ACTMODE_MUX_CTRL	LDOSRAMIVA_ACTMODE_VSET_IN					LDOSRAMIVA_ACTMODE_VSET_OUT			

Bits	Field Name	Description	Type	Reset
31:27	RESERVED		R	0x00
26	LDOSRAMIVA_RETMODE_MUX_CTRL	Override control of EFUSE Retention Mode Voltage value 0x0: efuse value is used 0x1: override value is used	RW	0
25:21	LDOSRAMIVA_RETMODE_VSET_IN	EFUSE Retention Mode Voltage value (vset[9:5])	R	0x00
20:16	LDOSRAMIVA_RETMODE_VSET_OUT	Override value for Retention Mode Voltage	RW	0x00
15:11	RESERVED		R	0x00
10	LDOSRAMIVA_ACTMODE_MUX_CTRL	Override control of EFUSE Active Mode Voltage value 0x0: efuse value is used 0x1: override value is used	RW	0
9:5	LDOSRAMIVA_ACTMODE_VSET_IN	EFUSE Active Mode Voltage value (vset[4:0])	R	0x00
4:0	LDOSRAMIVA_ACTMODE_VSET_OUT	Override value for Active Mode Voltage value	RW	0x00

Table 18-179. Register Call Summary for Register CONTROL_LDOSRAM_IVA_VOLTAGE_CTRL

Control Module Register Manual

- SYSCTRL_GENERAL_CORE Register Summary: [0]

Table 18-180. CONTROL_LDOSRAM_MPU_VOLTAGE_CTRL

Address Offset	0x0000 0324		
Physical Address	0x4A00 2324	**Instance**	SYSCTRL_GENERAL_CORE
Description	MPU SRAM LDO control register Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					LDOSRAMMPU_RETMODE_MUX_CTRL	LDOSRAMMPU_RETMODE_VSET_IN					LDOSRAMMPU_RETMODE_VSET_OUT					RESERVED					LDOSRAMMPU_ACTMODE_MUX_CTRL	LDOSRAMMPU_ACTMODE_VSET_IN					LDOSRAMMPU_ACTMODE_VSET_OUT			

Bits	Field Name	Description	Type	Reset
31:27	RESERVED		R	0x00
26	LDOSRAMMPU_RETMODE_MUX_CTRL	Override control of EFUSE Retention Mode Voltage value 0x0: efuse value is used 0x1: override value is used	RW	0
25:21	LDOSRAMMPU_RETMODE_VSET_IN	EFUSE Retention Mode Voltage value (vset[9:5])	R	0x00
20:16	LDOSRAMMPU_RETMODE_VSET_OUT	Override value for Retention Mode Voltage	RW	0x00
15:11	RESERVED		R	0x00
10	LDOSRAMMPU_ACTMODE_MUX_CTRL	Override control of EFUSE Active Mode Voltage value 0x0: efuse value is used 0x1: override value is used	RW	0
9:5	LDOSRAMMPU_ACTMODE_VSET_IN	EFUSE Active Mode Voltage value (vset[4:0])	R	0x00
4:0	LDOSRAMMPU_ACTMODE_VSET_OUT	Override value for Active Mode Voltage value	RW	0x00

Table 18-181. Register Call Summary for Register CONTROL_LDOSRAM_MPU_VOLTAGE_CTRL

Control Module Functional Description
- General Core Control Module Instance: [0]

Control Module Register Manual
- SYSCTRL_GENERAL_CORE Register Summary: [1]

Table 18-182. CONTROL_LDOSRAM_CORE_VOLTAGE_CTRL

Address Offset	0x0000 0328		
Physical Address	0x4A00 2328	**Instance**	SYSCTRL_GENERAL_CORE
Description	Core SRAM LDO control register Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					LDOSRAMCORE_RETMODE_MUX_CTRL	LDOSRAMCORE_RETMODE_VSET_IN					LDOSRAMCORE_RETMODE_VSET_OUT					RESERVED					LDOSRAMCORE_ACTMODE_MUX_CTRL	LDOSRAMCORE_ACTMODE_VSET_IN					LDOSRAMCORE_ACTMODE_VSET_OUT			

Bits	Field Name	Description	Type	Reset
31:27	RESERVED		R	0x00
26	LDOSRAMCORE_RETMODE_MUX_CTRL	Override control of EFUSE Retention Mode Voltage value 0x0: efuse value is used 0x1: override value is used	RW	0
25:21	LDOSRAMCORE_RETMODE_VSET_IN	EFUSE Retention Mode Voltage value (vset[9:5])	R	0x00
20:16	LDOSRAMCORE_RETMODE_VSET_OUT	Override value for Retention Mode Voltage	RW	0x00
15:11	RESERVED		R	0x00
10	LDOSRAMCORE_ACTMODE_MUX_CTRL	Override control of EFUSE Active Mode Voltage value 0x0: efuse value is used 0x1: override value is used	RW	0
9:5	LDOSRAMCORE_ACTMODE_VSET_IN	EFUSE Active Mode Voltage value (vset[4:0])	R	0x00
4:0	LDOSRAMCORE_ACTMODE_VSET_OUT	Override value for Active Mode Voltage value	RW	0x00

Table 18-183. Register Call Summary for Register CONTROL_LDOSRAM_CORE_VOLTAGE_CTRL

Control Module Register Manual

- SYSCTRL_GENERAL_CORE Register Summary: [0]

Table 18-184. CONTROL_TEMP_SENSOR

Address Offset	0x0000 032C		
Physical Address	0x4A00 232C	**Instance**	SYSCTRL_GENERAL_CORE
Description	Control VBGAPTS temperature sensor and thermal comparator shutdown register Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																		BGAP_TEMPSOFF	RESERVED	BGAP_TEMP_SENSOR_SOC	BGAP_TEMP_SENSOR_EOCZ	BGAP_TEMP_SENSOR_DTEMP								

Bits	Field Name	Description	Type	Reset
31:14	RESERVED		R	0x00000
13	BGAP_TEMPSOFF	Temperature sensor and thermal shutdown mode. 0x0: Temperature sensor and thermal shutdown is active 0x1: Temperature sensor and thermal shutdown set in OFF mode	RW	0
12	RESERVED	Reserved	RW	0
11	BGAP_TEMP_SENSOR_SOC	ADC Start of Conversion. A transition to high starts a new ADC conversion cycle	RW	0
10	BGAP_TEMP_SENSOR_EOCZ	ADC End of Conversion. Active low, when CTRL_TEMP(5:0) is valid.	R	0
9:0	BGAP_TEMP_SENSOR_DTEMP	Temperature data from the ADC. Valid if EOCZ is low.	R	0x000

Table 18-185. Register Call Summary for Register CONTROL_TEMP_SENSOR

Control Module Functional Description
- Control Module Clock Configuration: [0]
- General Core Control Module Instance: [1]
- Band Gap Voltage and Temperature Sensor: [2] [3]
- Temperature Sensor: [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18]
- Temperature Sensor Control Registers: [19] [20]

Control Module Programming Guide
- Global Initialization: [21]

Control Module Register Manual
- SYSCTRL_GENERAL_CORE Register Summary: [22]

Table 18-186. CONTROL_DPLL_NWELL_TRIM_0

Address Offset	0x0000 0330		
Physical Address	0x4A00 2330	**Instance**	SYSCTRL_GENERAL_CORE
Description	Dpll trim (SW override) - Part 0 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		DPLL_ABE_NWELL_TRIM_MUX_CTRL						DPLL_ABE_NWELL_TRIM								DPLL_PER_NWELL_TRIM_MUX_CTRL								DPLL_PER_NWELL_TRIM							
RESERVED		DPLL_CORE_NWELL_TRIM_MUX_CTRL						DPLL_CORE_NWELL_TRIM								DPLL_IVA_NWELL_TRIM_MUX_CTRL								DPLL_IVA_NWELL_TRIM							
RESERVED		DPLL_MPU_NWELL_TRIM_MUX_CTRL						DPLL_MPU_NWELL_TRIM																							

Bits	Field Name	Description	Type	Reset
31:30	RESERVED		R	0x0
29	DPLL_ABE_NWELL_TRIM_MUX_CTRL	Software override selection over efuse values. 0x0: efuse value is used 0x1: override value is used	RW	0
28:24	DPLL_ABE_NWELL_TRIM	Software override value.	RW	0x00
23	DPLL_PER_NWELL_TRIM_MUX_CTRL	Software override selection over efuse values. 0x0: efuse value is used 0x1: override value is used	RW	0
22:18	DPLL_PER_NWELL_TRIM	Software override value.	RW	0x00
17	DPLL_CORE_NWELL_TRIM_MUX_CTRL	Software override selection over efuse values. 0x0: efuse value is used 0x1: override value is used	RW	0
16:12	DPLL_CORE_NWELL_TRIM	Software override value.	RW	0x00
11	DPLL_IVA_NWELL_TRIM_MUX_CTRL	Software override selection over efuse values. 0x0: efuse value is used 0x1: override value is used	RW	0
10:6	DPLL_IVA_NWELL_TRIM	Software override value.	RW	0x00
5	DPLL_MPU_NWELL_TRIM_MUX_CTRL	Software override selection over efuse values. 0x0: efuse value is used 0x1: override value is used	RW	0
4:0	DPLL_MPU_NWELL_TRIM	Software override value.	RW	0x00

Table 18-187. Register Call Summary for Register CONTROL_DPLL_NWELL_TRIM_0

Control Module Register Manual

- SYSCTRL_GENERAL_CORE Register Summary: [0]

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Table 18-188. CONTROL_DPLL_NWELL_TRIM_1

Address Offset	0x0000 0334		
Physical Address	0x4A00 2334	**Instance**	SYSCTRL_GENERAL_CORE
Description	Dpll trim (SW override) - Part 1 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								DPLL_USB_NWELL_TRIM_MUX_CTRL								RESERVED				DPLL_DSI2_NWELL_TRIM_MUX_CTRL						DPLL_DSI1_NWELL_TRIM_MUX_CTRL							
RESERVED								DPLL_USB_NWELL_TRIM												DPLL_DSI2_NWELL_TRIM				DPLL_DSI1_NWELL_TRIM							

Bits	Field Name	Description	Type	Reset
31:30	RESERVED		R	0x0
29:24	RESERVED	Reserved	RW	0x00
23	DPLL_USB_NWELL_TRIM_MUX_CTRL	Software override selection over efuse values. 0x0: efuse value is used 0x1: override value is used	RW	0
22:18	DPLL_USB_NWELL_TRIM	Software override value.	RW	0x00
17:12	RESERVED	Reserved	RW	0
11	DPLL_DSI2_NWELL_TRIM_MUX_CTRL	Software override selection over efuse values. 0x0: efuse value is used 0x1: override value is used	RW	0
10:6	DPLL_DSI2_NWELL_TRIM	Software override value.	RW	0x00
5	DPLL_DSI1_NWELL_TRIM_MUX_CTRL	Software override selection over efuse values. 0x0: efuse value is used 0x1: override value is used	RW	0
4:0	DPLL_DSI1_NWELL_TRIM	Software override value.	RW	0x00

Table 18-189. Register Call Summary for Register CONTROL_DPLL_NWELL_TRIM_1

Control Module Register Manual

- SYSCTRL_GENERAL_CORE Register Summary: [0]

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Table 18-190. CONTROL_USBOTGHS_CONTROL

Address Offset	0x0000 033C		
Physical Address	0x4A00 233C	**Instance**	SYSCTRL_GENERAL_CORE
Description	USBOTGHS software control Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							DISCHRGVBUS	CHRGVBUS	DRVVBUS	IDPULLUP	IDDIG	SESSEND	VBUSVALID	BVALID	AVALID

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	DISCHRGVBUS	USBOTGHS value for signal dischrgvbus (OTG_PD_VBUS). controls discharging of VBUS for completing SRP. Read 0x0: OTG transceiver does not discharge VBUS Read 0x1: OTG transceiver discharges VBUS	R	0
7	CHRGVBUS	USBOTGHS value for signal chrgvbus (OTG_PU_VBUS). controls charging of VBUS for initiating SRP. Read 0x0: OTG transceiver does not charge VBUS Read 0x1: OTG transceiver charges VBUS	R	0
6	DRVVBUS	USBOTGHS value for signal drvvbus (OTG_DRV_VBUS). controls the driving of 5V power on VBUS. Read 0x0: OTG transceiver does not drive VBUS Read 0x1: OTG transceiver drives VBUS	R	0
5	IDPULLUP	USBOTGHS value for signal Idpullup (OTG_PU_ID). Enables sampling of the ID pin of the USB connector. Read 0x0: OTG transceiver does not apply a pullup to ID Read 0x1: OTG transceiver applies a pullup to ID	R	0
4	IDDIG	Sets the USBOTGHS signal iddig (ID). Indicates the value of the ID pin of the USB connector. 0x0: ID pin is grounded 0x1: ID pin is high-impedance	RW	1
3	SESSEND	Sets the USBOTGHS signal sessend (BSESSEND). Indicates if VBUS is below the B-Device session end threshold. The threshold Vth is between 0.2V and 0.8V. 0x0: VBUS voltage is above VB_SESS_END 0x1: VBUS voltage is below VB_SESS_END	RW	1
2	VBUSVALID	Sets the USBOTGHS signal vbusvalid (VBUSVLD). Indicates if VBUS is above the threshold for normal operation. The threshold Vth is between 4.4V and 4.75V.	RW	0
1	BVALID	Sets the USBOTGHS signal bvalid (BSESSVLD). Signal is currently unconnected (reserved for future use). 0x0: VBUS voltage is below VB_SESS_VLD 0x1: VBUS voltage is above VB_SESS_VLD	RW	0

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Bits	Field Name	Description	Type	Reset
0	AVALID	Sets the USBOTGHS signal avalid (ASESSVLD). Indicates if VBUS is above the A-Device session valid threshold. The threshold Vth is between 0.8V and 2.0V. 0x0: VBUS voltage is below VA_SESS_VLD 0x1: VBUS voltage is above VA_SESS_VLD	RW	0

Table 18-191. Register Call Summary for Register CONTROL_USBOTGHS_CONTROL

Control Module Functional Description • General Core Control Module Instance: [0]
Control Module Register Manual • SYSCTRL_GENERAL_CORE Register Summary: [1]

Table 18-192. CONTROL_DSS_CONTROL

Address Offset	0x0000 0340		
Physical Address	0x4A00 2340	**Instance**	SYSCTRL_GENERAL_CORE
Description	DSS software control Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															DSS_MUX6_SELECT

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	DSS_MUX6_SELECT	Mux6 select value for DSS. 0x0: enables DSS_CLK as functional clock input for the DSI2 PHY bypass clock 0x1: enables PLL1_CLK4 as functional clock input for the DSI2 PHY bypass clock	RW	0

Table 18-193. Register Call Summary for Register CONTROL_DSS_CONTROL

Control Module Functional Description • General Core Control Module Instance: [0]
Control Module Register Manual • SYSCTRL_GENERAL_CORE Register Summary: [1]

Table 18-194. CONTROL_CORTEX_M3_MMUADDRTRANSLTR

Address Offset	0x0000 0348		
Physical Address	0x4A00 2348	**Instance**	SYSCTRL_GENERAL_CORE
Description	CORTEX_M3 reg Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								CORTEX_M3_MMUADDRTRANSLTR																									

Bits	Field Name	Description	Type	Reset
31:20	RESERVED		R	0x000
19:0	CORTEX_M3_MMUADDRTRANSLTR	Used to save the mmu address boot	RW	0x00000

Table 18-195. Register Call Summary for Register CONTROL_CORTEX_M3_MMUADDRTRANSLTR

Control Module Functional Description • General Core Control Module Instance: [0]
Control Module Register Manual • SYSCTRL_GENERAL_CORE Register Summary: [1]

Table 18-196. CONTROL_CORTEX_M3_MMUADDRLOGICTR

Address Offset	0x0000 034C		
Physical Address	0x4A00 234C	**Instance**	SYSCTRL_GENERAL_CORE
Description	Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								CORTEX_M3_MMUADDRLOGICTR																									

Bits	Field Name	Description	Type	Reset
31:20	RESERVED		R	0x000
19:0	CORTEX_M3_MMUADDRLOGICTR		RW	0x00000

Table 18-197. Register Call Summary for Register CONTROL_CORTEX_M3_MMUADDRLOGICTR

Control Module Functional Description • General Core Control Module Instance: [0]
Control Module Register Manual • SYSCTRL_GENERAL_CORE Register Summary: [1]

Table 18-198. CONTROL_HWOBS_CONTROL

Address Offset	0x0000 0350		
Physical Address	0x4A00 2350	**Instance**	SYSCTRL_GENERAL_CORE
Description	Hardware observability control. This register enables or disables hardware observability outputs (to save power primarily) Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							HWOBS_CLKOBS_GATE_ENABLE	HWOBS_CLKDIV_SEL						HWOBS_ALL_ZERO_MODE	HWOBS_ALL_ONE_MODE	HWOBS_MACRO_ENABLE

Bits	Field Name	Description	Type	Reset
31:19	RESERVED		R	0x000000
18:14	HWOBS_CLKDIV_SEL_2	Clock divider selection on po_hwobs(2). 0x1: output is not divided 0x2: output is divided by 2 0x4: output is divided by 4 0x8: output is divided by 8 0x10: output is divided by 16(1)	RW	0x00
13:9	HWOBS_CLKDIV_SEL_1	Clock divider selection on po_hwobs(1). 0x1: output is not divided 0x2: output is divided by 2 0x4: output is divided by 4 0x8: output is divided by 8 0x10: output is divided by 16(1)	RW	0x00
8	RESERVED		R	0x0
7:3	HWOBS_CLKDIV_SEL	Clock divider selection on po_hwobs(0). 0x1: output is not divided 0x2: output is divided by 2 0x4: output is divided by 4 0x8: output is divided by 8 0x10: output is divided by 16(1)	RW	0x00
2	HWOBS_ALL_ZERO_MODE	Used to gate observable signals. When set all outputs are set to zero (can be used to check the path from hardware observability to external pads). 0x0: Hardware observability ports are not gated 0x1: Hardware observability ports are all set to 0	RW	0
1	HWOBS_ALL_ONE_MODE	Used to gate observable signals. When set all outputs are set to one (can be used to check the path from hardware observability to external pads). 0x0: Hardware observability ports are not gated 0x1: Hardware observability ports are all set to 1	RW	0
0	HWOBS_MACRO_ENABLE	Used to gate observable signals coming from macros using the 32-bit HWOBS bus definition. When deasserted all outputs of the HWOBS busdef are set to zero. 0x0: Hardware observability ports from macros are gated and set to zero 0x1: Hardware observability ports from macros are not gated	RW	0

(1) The values different than 1, 2, 4, 8, and 16 are reserved.

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Table 18-199. Register Call Summary for Register CONTROL_HWOBS_CONTROL

Control Module Functional Description • General Core Control Module Instance: [0] • Observability Gating Capabilities: [1] [2] [3] [4] [5] [6] [7] [8] [9] [10]
Control Module Programming Guide • Operational Modes Configuration: [11] [12] [13] [14] [15] [16]
Control Module Register Manual • SYSCTRL_GENERAL_CORE Register Summary: [17]

Table 18-200. CONTROL_EMIF1_OFFSET

Address Offset	0x0000 0360		
Physical Address	0x4A00 2360	**Instance**	SYSCTRL_GENERAL_CORE
Description	emif1 offset Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
EMIF1_DLL_OFFSET_3	EMIF1_DLL_OFFSET_2	EMIF1_DLL_OFFSET_1	EMIF1_DLL_OFFSET_0

Bits	Field Name	Description	Type	Reset
31:24	EMIF1_DLL_OFFSET_3	8-bit signed offset value (-128 ... +127) for EMIF1 DLL Slave3 delay correction.	RW	0x00
23:16	EMIF1_DLL_OFFSET_2	8-bit signed offset value (-128 ... +127) for EMIF1 DLL Slave2 delay correction.	RW	0x00
15:8	EMIF1_DLL_OFFSET_1	8-bit signed offset value (-128 ... +127) for EMIF1 DLL Slave1 delay correction.	RW	0x00
7:0	EMIF1_DLL_OFFSET_0	8-bit signed offset value (-128 ... +127) for EMIF1 DLL Slave0 delay correction.	RW	0x00

Table 18-201. Register Call Summary for Register CONTROL_EMIF1_OFFSET

Control Module Functional Description • EMIF DLL Master/Slave Specific Registers: [0] [1] [2]
Control Module Register Manual • SYSCTRL_GENERAL_CORE Register Summary: [3]

Table 18-202. CONTROL_EMIF2_OFFSET

Address Offset	0x0000 0364		
Physical Address	0x4A00 2364	**Instance**	SYSCTRL_GENERAL_CORE
Description	emif2 offset Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
EMIF2_DLL_OFFSET_3	EMIF2_DLL_OFFSET_2	EMIF2_DLL_OFFSET_1	EMIF2_DLL_OFFSET_0

Bits	Field Name	Description	Type	Reset
31:24	EMIF2_DLL_OFFSET_3	8-bit signed offset value (-128 ... +127) for EMIF2 DLL Slave3 delay correction.	RW	0x00
23:16	EMIF2_DLL_OFFSET_2	8-bit signed offset value (-128 ... +127) for EMIF2 DLL Slave2 delay correction.	RW	0x00

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Bits	Field Name	Description	Type	Reset
15:8	EMIF2_DLL_OFFSET_1	8-bit signed offset value (-128 ... +127) for EMIF2 DLL Slave1 delay correction.	RW	0x00
7:0	EMIF2_DLL_OFFSET_0	8-bit signed offset value (-128 ... +127) for EMIF2 DLL Slave0 delay correction.	RW	0x00

Table 18-203. Register Call Summary for Register CONTROL_EMIF2_OFFSET

Control Module Functional Description
- EMIF DLL Master/Slave Specific Registers: [0] [1] [2]

Control Module Register Manual
- SYSCTRL_GENERAL_CORE Register Summary: [3]

Table 18-204. CONTROL_EMIF1_MASTER_CODE_0

Address Offset	0x0000 0368		
Physical Address	0x4A00 2368	**Instance**	SYSCTRL_GENERAL_CORE
Description	emif1 master code Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								EMIF1_MASTER_CODE_1								RESERVED								EMIF1_MASTER_CODE_0							

Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x00
25:16	EMIF1_MASTER_CODE_1	EMIF1 DLL Master1 code	R	0x000
15:10	RESERVED		R	0x00
9:0	EMIF1_MASTER_CODE_0	EMIF1 DLL Master0 code	R	0x000

Table 18-205. Register Call Summary for Register CONTROL_EMIF1_MASTER_CODE_0

Control Module Functional Description
- EMIF DLL Master/Slave Specific Registers: [0] [1]

Control Module Register Manual
- SYSCTRL_GENERAL_CORE Register Summary: [2]

Table 18-206. CONTROL_EMIF1_MASTER_CODE_1

Address Offset	0x0000 036C		
Physical Address	0x4A00 236C	**Instance**	SYSCTRL_GENERAL_CORE
Description	Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								EMIF1_MASTER_CODE_3								RESERVED								EMIF1_MASTER_CODE_2							

Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x00
25:16	EMIF1_MASTER_CODE_3	EMIF1 DLL Master3 code	R	0x000
15:10	RESERVED		R	0x00
9:0	EMIF1_MASTER_CODE_2	EMIF1 DLL Master2 code	R	0x000

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Table 18-207. Register Call Summary for Register CONTROL_EMIF1_MASTER_CODE_1

Control Module Functional Description • EMIF DLL Master/Slave Specific Registers: [0] [1]
Control Module Register Manual • SYSCTRL_GENERAL_CORE Register Summary: [2]

Table 18-208. CONTROL_EMIF2_MASTER_CODE_0

Address Offset	0x0000 0370		
Physical Address	0x4A00 2370	**Instance**	SYSCTRL_GENERAL_CORE
Description	emif2 master code Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								EMIF2_MASTER_CODE_1								RESERVED								EMIF2_MASTER_CODE_0							

Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x00
25:16	EMIF2_MASTER_CODE_1	EMIF2 DLL Master1 code	R	0x000
15:10	RESERVED		R	0x00
9:0	EMIF2_MASTER_CODE_0	EMIF2 DLL Master0 code	R	0x000

Table 18-209. Register Call Summary for Register CONTROL_EMIF2_MASTER_CODE_0

Control Module Functional Description • EMIF DLL Master/Slave Specific Registers: [0] [1]
Control Module Register Manual • SYSCTRL_GENERAL_CORE Register Summary: [2]

Table 18-210. CONTROL_EMIF2_MASTER_CODE_1

Address Offset	0x0000 0374		
Physical Address	0x4A00 2374	**Instance**	SYSCTRL_GENERAL_CORE
Description	Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								EMIF2_MASTER_CODE_3								RESERVED								EMIF2_MASTER_CODE_2							

Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x00
25:16	EMIF2_MASTER_CODE_3	EMIF2 DLL Master3 code	R	0x000
15:10	RESERVED		R	0x00
9:0	EMIF2_MASTER_CODE_2	EMIF2 DLL Master2 code	R	0x000

Table 18-211. Register Call Summary for Register CONTROL_EMIF2_MASTER_CODE_1

Control Module Functional Description • EMIF DLL Master/Slave Specific Registers: [0] [1]
Control Module Register Manual • SYSCTRL_GENERAL_CORE Register Summary: [2]

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Table 18-212. CONTROL_BANDGAP_CTRL

Address Offset	0x0000 0378		
Physical Address	0x4A00 2378	**Instance**	SYSCTRL_GENERAL_CORE
Description	bandgap control Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SINGLE_MODE	RESERVED																													MASK_HOT	MASK_COLD

Bits	Field Name	Description	Type	Reset
31	SINGLE_MODE	Toggles between single mode or continuous mode (repeated single mode) 0x0: Single mode selected 0x1: Continuous mode selected	RW	0
30:2	RESERVED		R	0x0000 0000
1	MASK_HOT	Mask for hot events 0x0: hot event is masked 0x1: hot event is enabled	RW	0
0	MASK_COLD	Mask for cold events 0x0: cold event is masked 0x1: cold event is enabled	RW	0

Table 18-213. Register Call Summary for Register CONTROL_BANDGAP_CTRL

Control Module Functional Description

- General Core Control Module Instance: [0]
- Temperature Sensor: [1] [2] [3] [4] [5] [6] [7]
- Temperature Sensor Control Registers: [8]

Control Module Register Manual

- SYSCTRL_GENERAL_CORE Register Summary: [9]

Table 18-214. CONTROL_BANDGAP_COUNTER

Address Offset	0x0000 037C		
Physical Address	0x4A00 237C	**Instance**	SYSCTRL_GENERAL_CORE
Description	bandgap counter Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								COUNTER																							

Bits	Field Name	Description	Type	Reset
31:24	RESERVED		R	0x00
23:0	COUNTER	Counter for continous mode	RW	0x000000

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Table 18-215. Register Call Summary for Register CONTROL_BANDGAP_COUNTER

Control Module Functional Description • General Core Control Module Instance: [0] • Temperature Sensor Control Registers: [1]
Control Module Register Manual • SYSCTRL_GENERAL_CORE Register Summary: [2]

Table 18-216. CONTROL_BANDGAP_THRESHOLD

Address Offset	0x0000 0380		
Physical Address	0x4A00 2380	**Instance**	SYSCTRL_GENERAL_CORE
Description	bandgap threshold Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								T_HOT								RESERVED								T_COLD							

Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x00
25:16	T_HOT	Threshold for hot temperature	RW	0x000
15:10	RESERVED		R	0x00
9:0	T_COLD	Threshold for cold temperature	RW	0x000

Table 18-217. Register Call Summary for Register CONTROL_BANDGAP_THRESHOLD

Control Module Functional Description • General Core Control Module Instance: [0] • Temperature Sensor: [1] [2] [3] • Temperature Sensor Control Registers: [4]
Control Module Register Manual • SYSCTRL_GENERAL_CORE Register Summary: [5]

Table 18-218. CONTROL_TSHUT_THRESHOLD

Address Offset	0x0000 0384		
Physical Address	0x4A00 2384	**Instance**	SYSCTRL_GENERAL_CORE
Description	bandgap tshut threshold Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TSHUT_HOT								RESERVED								TSHUT_COLD							

Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x00
25:16	TSHUT_HOT	Tshut Threshold for hot temperature. Code value must not exceed the device junction (hottest spot) maximal-allowed temperature minus the device temperature sensor offset estimated at current conditions. For more information, see Section 18.4.10.2, *Temperature Sensor*.	RW	0x000
15:10	RESERVED		R	0x00

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Bits	Field Name	Description	Type	Reset
9:0	TSHUT_COLD	Tshut Threshold for cold temperature	RW	0x000

Table 18-219. Register Call Summary for Register CONTROL_TSHUT_THRESHOLD

Control Module Functional Description
- General Core Control Module Instance: [0]
- Temperature Sensor: [1] [2] [3]
- Temperature Sensor Control Registers: [4]

Control Module Register Manual
- SYSCTRL_GENERAL_CORE Register Summary: [5]

Table 18-220. CONTROL_BANDGAP_STATUS

Address Offset	0x0000 0388		
Physical Address	0x4A00 2388	**Instance**	SYSCTRL_GENERAL_CORE
Description	bandgap status Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												CLEAN_STOP	BGAP_ALERT	HOT_FLAG	COLD_FLAG

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0000000
3	CLEAN_STOP	Show when clean stop	R	1
2	BGAP_ALERT	Show when hot or cold event	R	0
1	HOT_FLAG	Show when hot event	R	0
0	COLD_FLAG	Show when cold event	R	0

Table 18-221. Register Call Summary for Register CONTROL_BANDGAP_STATUS

Control Module Functional Description
- General Core Control Module Instance: [0]
- Band Gap Voltage and Temperature Sensor: [1]
- Temperature Sensor: [2] [3] [4]
- Temperature Sensor Control Registers: [5]

Control Module Register Manual
- SYSCTRL_GENERAL_CORE Register Summary: [6]

Table 18-222. CONTROL_FORCEWRNP

Address Offset	0x0000 03C0		
Physical Address	0x4A00 23C0	**Instance**	SYSCTRL_GENERAL_CORE
Description	Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															MPUFORCEWRNP

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	MPUFORCEWRNP	0x0: Non-posted write attribute is defined by Cortex-A9 CPU 0x1: Forces only non-posted write commands from MPUSS to the L3 interconnect	RW	0

Table 18-223. Register Call Summary for Register CONTROL_FORCEWRNP

Control Module Functional Description
• Force MPU Write Nonposted Transactions Control Register: [0]
Control Module Register Manual
• SYSCTRL_GENERAL_CORE Register Summary: [1]

Table 18-224. CONTROL_GEN_CORE_OCPREG_SPARE

Address Offset	0x0000 03FC		
Physical Address	0x4A00 23FC	**Instance**	SYSCTRL_GENERAL_CORE
Description	The lower 4-bits of this register are assigned to control PWRDN mode globally, and the LVCMOS buffers enable control of the EMIF1 and EMIF2 PHYs. Read: Unrestricted; Write: Unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OCPREG_SPARE																												OCPREG_SPARE3	OCPREG_SPARE2	OCPREG_SPARE1	OCPREG_SPARE0

Bits	Field Name	Description	Type	Reset
31:4	OCPREG_SPARE	Reserved	R	0x0000000
3	OCPREG_SPARE3	emif2phydata0–emif2phydata3 power-down mode control 0x0: Normal mode selected 0x1: Power-down mode selected	RW	0
2	OCPREG_SPARE2	emif2phycmd0, emif2phydata0–emif2phydata3 I/O LVCMOS buffers enable 0x0: Differential comparator is enabled. 0x1: Differential comparator is disabled.	RW	0
1	OCPREG_SPARE1	emif1phydata0–emif1phydata3 power-down mode control 0x0: Normal mode is selected. 0x1: Power-down mode is selected.	RW	0

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Bits	Field Name	Description	Type	Reset
0	OCPREG_SPARE0	emif1phycmd0, emif1phydata0–emif1phydata3 I/O LVCMOS buffers enable 0x0: LVCMOS buffers are enabled. 0x1: LVCMOS buffers are disabled.	RW	0

Table 18-225. Register Call Summary for Register CONTROL_GEN_CORE_OCPREG_SPARE

Control Module Functional Description
- Register Controls for the LPDDR2IO1/LPDDR2IO2 I/O Buffer Modes: [0] [1]

Control Module Register Manual
- SYSCTRL_GENERAL_CORE Register Summary: [2]

Table 18-226. CONTROL_DEBOBS_FINAL_MUX_SEL

Address Offset	0x0000 0400
Physical Address	0x4A00 2400 **Instance** SYSCTRL_GENERAL_CORE
Description	Final mux select signal. It selects between core and wkup signal (controls external observability logic). Access conditions. Read: unrestricted, Write: unrestricted
Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SELECT																															

Bits	Field Name	Description	Type	Reset
31:0	SELECT	The i-th (i=0..31) bit from this bit field controls the multiplexing between the core and the wake-up signals to be observed at i-th hw_dbg line. Ob0: Selects a signal from the WAKEUP domain 0b1: Select a signal from the CORE domain	RW	0x0000 0000

Table 18-227. Register Call Summary for Register CONTROL_DEBOBS_FINAL_MUX_SEL

Control Module Functional Description
- General Core Control Module Instance: [0]
- Observability Gating Capabilities: [1] [2]
- Observability Signals Multiplexing at General Core/Wake-Up Control Level: [3] [4] [5] [6] [7]

Control Module Programming Guide
- Operational Modes Configuration: [8]

Control Module Register Manual
- SYSCTRL_GENERAL_CORE Register Summary: [9]

Table 18-228. CONTROL_DEBOBS_MMR_MPU

Address Offset	0x0000 0408
Physical Address	0x4A00 2408 **Instance** SYSCTRL_GENERAL_CORE
Description	Dual Cortex-A9 register to control hardware observability muxing inside dual Cortex-A9 (controls external observability logic).
Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												SELECT			

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Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved. Read returns reset value.	R	0x0000 0000
3:0	SELECT	Control external observability logic	RW	0x0

Table 18-229. Register Call Summary for Register CONTROL_DEBOBS_MMR_MPU

Control Module Functional Description • Observability Signals Sourced at Module Level: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12]
Control Module Register Manual • SYSCTRL_GENERAL_CORE Register Summary: [13]

Table 18-230. CONTROL_CONF_SDMA_REQ_SEL0

Address Offset	0x0000 042C		
Physical Address	0x4A00 242C	**Instance**	SYSCTRL_GENERAL_CORE
Description	System DMA requests view channel 0 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								MULT							

Bits	Field Name	Description	Type	Reset
31:7	RESERVED		R	0x0000000
6:0	MULT	Select one of the following signals: 0x0: hwobs_sdma_dma_req_0 0x1: hwobs_sdma_dma_req_1 0x2: hwobs_sdma_dma_req_2 0x3: hwobs_sdma_dma_req_3 0x4: hwobs_sdma_dma_req_4 0x5: hwobs_sdma_dma_req_5 0x6: hwobs_sdma_dma_req_6 0x7: hwobs_sdma_dma_req_7 0x8: hwobs_sdma_dma_req_8 0x9: hwobs_sdma_dma_req_9 0xA: hwobs_sdma_dma_req_10 0xB: hwobs_sdma_dma_req_11 0xC: hwobs_sdma_dma_req_12 0xD: hwobs_sdma_dma_req_13 0xE: hwobs_sdma_dma_req_14 0xF: hwobs_sdma_dma_req_15 0x10: hwobs_sdma_dma_req_16 0x11: hwobs_sdma_dma_req_17 0x12: hwobs_sdma_dma_req_18 0x13: hwobs_sdma_dma_req_19 0x14: hwobs_sdma_dma_req_20 0x15: hwobs_sdma_dma_req_21 0x16: hwobs_sdma_dma_req_22 0x17: hwobs_sdma_dma_req_23 0x18: hwobs_sdma_dma_req_24 0x19: hwobs_sdma_dma_req_25 0x1A: hwobs_sdma_dma_req_26	RW	0x00

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Bits	Field Name	Description	Type	Reset
		0x1B: hwobs_sdma_dma_req_27		
		0x1C: hwobs_sdma_dma_req_28		
		0x1D: hwobs_sdma_dma_req_29		
		0x1E: hwobs_sdma_dma_req_30		
		0x1F: hwobs_sdma_dma_req_31		
		0x20: hwobs_sdma_dma_req_32		
		0x21: hwobs_sdma_dma_req_33		
		0x22: hwobs_sdma_dma_req_34		
		0x23: hwobs_sdma_dma_req_35		
		0x24: hwobs_sdma_dma_req_36		
		0x25: hwobs_sdma_dma_req_37		
		0x26: hwobs_sdma_dma_req_38		
		0x27: hwobs_sdma_dma_req_39		
		0x28: hwobs_sdma_dma_req_40		
		0x29: hwobs_sdma_dma_req_41		
		0x2A: hwobs_sdma_dma_req_42		
		0x2B: hwobs_sdma_dma_req_43		
		0x2C: hwobs_sdma_dma_req_44		
		0x2D: hwobs_sdma_dma_req_45		
		0x2E: hwobs_sdma_dma_req_46		
		0x2F: hwobs_sdma_dma_req_47		
		0x30: hwobs_sdma_dma_req_48		
		0x31: hwobs_sdma_dma_req_49		
		0x32: hwobs_sdma_dma_req_50		
		0x33: hwobs_sdma_dma_req_51		
		0x34: hwobs_sdma_dma_req_52		
		0x35: hwobs_sdma_dma_req_53		
		0x36: hwobs_sdma_dma_req_54		
		0x37: hwobs_sdma_dma_req_55		
		0x38: hwobs_sdma_dma_req_56		
		0x39: hwobs_sdma_dma_req_57		
		0x3A: hwobs_sdma_dma_req_58		
		0x3B: hwobs_sdma_dma_req_59		
		0x3C: hwobs_sdma_dma_req_60		
		0x3D: hwobs_sdma_dma_req_61		
		0x3E: hwobs_sdma_dma_req_62		
		0x3F: hwobs_sdma_dma_req_63		
		0x40: hwobs_sdma_dma_req_64		
		0x41: hwobs_sdma_dma_req_65		
		0x42: hwobs_sdma_dma_req_66		
		0x43: hwobs_sdma_dma_req_67		
		0x44: hwobs_sdma_dma_req_68		
		0x45: hwobs_sdma_dma_req_69		
		0x46: hwobs_sdma_dma_req_70		
		0x47: hwobs_sdma_dma_req_71		
		0x48: hwobs_sdma_dma_req_72		
		0x49: hwobs_sdma_dma_req_73		
		0x4A: hwobs_sdma_dma_req_74		
		0x4B: hwobs_sdma_dma_req_75		

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Bits	Field Name	Description	Type	Reset
		0x4C: hwobs_sdma_dma_req_76		
		0x4D: hwobs_sdma_dma_req_77		
		0x4E: hwobs_sdma_dma_req_78		
		0x4F: hwobs_sdma_dma_req_79		
		0x50: hwobs_sdma_dma_req_80		
		0x51: hwobs_sdma_dma_req_81		
		0x52: hwobs_sdma_dma_req_82		
		0x53: hwobs_sdma_dma_req_83		
		0x54: hwobs_sdma_dma_req_84		
		0x55: hwobs_sdma_dma_req_85		
		0x56: hwobs_sdma_dma_req_86		
		0x57: hwobs_sdma_dma_req_87		
		0x58: hwobs_sdma_dma_req_88		
		0x59: hwobs_sdma_dma_req_89		
		0x5A: hwobs_sdma_dma_req_90		
		0x5B: hwobs_sdma_dma_req_91		
		0x5C: hwobs_sdma_dma_req_92		
		0x5D: hwobs_sdma_dma_req_93		
		0x5E: hwobs_sdma_dma_req_94		
		0x5F: hwobs_sdma_dma_req_95		
		0x60: hwobs_sdma_dma_req_96		
		0x61: hwobs_sdma_dma_req_97		
		0x62: hwobs_sdma_dma_req_98		
		0x63: hwobs_sdma_dma_req_99		
		0x64: hwobs_sdma_dma_req_100		
		0x65: hwobs_sdma_dma_req_101		
		0x66: hwobs_sdma_dma_req_102		
		0x67: hwobs_sdma_dma_req_103		
		0x68: hwobs_sdma_dma_req_104		
		0x69: hwobs_sdma_dma_req_105		
		0x6A: hwobs_sdma_dma_req_106		
		0x6B: hwobs_sdma_dma_req_107		
		0x6C: hwobs_sdma_dma_req_108		
		0x6D: hwobs_sdma_dma_req_109		
		0x6E: hwobs_sdma_dma_req_110		
		0x6F: hwobs_sdma_dma_req_111		
		0x70: hwobs_sdma_dma_req_112		
		0x71: hwobs_sdma_dma_req_113		
		0x72: hwobs_sdma_dma_req_114		
		0x73: hwobs_sdma_dma_req_115		
		0x74: hwobs_sdma_dma_req_116		
		0x75: hwobs_sdma_dma_req_117		
		0x76: hwobs_sdma_dma_req_118		
		0x77: hwobs_sdma_dma_req_119		
		0x78: hwobs_sdma_dma_req_120		
		0x79: hwobs_sdma_dma_req_121		
		0x7A: hwobs_sdma_dma_req_122		
		0x7B: hwobs_sdma_dma_req_123		
		0x7C: hwobs_sdma_dma_req_124		

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Bits	Field Name	Description	Type	Reset
		0x7D: hwobs_sdma_dma_req_125 0x7E: hwobs_sdma_dma_req_126		

Table 18-231. Register Call Summary for Register CONTROL_CONF_SDMA_REQ_SEL0

Control Module Functional Description • Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0] [1]
Control Module Programming Guide • Operational Modes Configuration: [2]
Control Module Register Manual • SYSCTRL_GENERAL_CORE Register Summary: [3]

Table 18-232. CONTROL_CONF_SDMA_REQ_SEL1

Address Offset	0x0000 0430		
Physical Address	0x4A00 2430	**Instance**	SYSCTRL_GENERAL_CORE
Description	System DMA requests view channel 1 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								MULT							

Bits	Field Name	Description	Type	Reset
31:7	RESERVED		R	0x0000000
6:0	MULT	Select one of the following signals: 0x0: hwobs_sdma_dma_req_0 0x1: hwobs_sdma_dma_req_1 0x2: hwobs_sdma_dma_req_2 0x3: hwobs_sdma_dma_req_3 0x4: hwobs_sdma_dma_req_4 0x5: hwobs_sdma_dma_req_5 0x6: hwobs_sdma_dma_req_6 0x7: hwobs_sdma_dma_req_7 0x8: hwobs_sdma_dma_req_8 0x9: hwobs_sdma_dma_req_9 0xA: hwobs_sdma_dma_req_10 0xB: hwobs_sdma_dma_req_11 0xC: hwobs_sdma_dma_req_12 0xD: hwobs_sdma_dma_req_13 0xE: hwobs_sdma_dma_req_14 0xF: hwobs_sdma_dma_req_15 0x10: hwobs_sdma_dma_req_16 0x11: hwobs_sdma_dma_req_17 0x12: hwobs_sdma_dma_req_18 0x13: hwobs_sdma_dma_req_19 0x14: hwobs_sdma_dma_req_20 0x15: hwobs_sdma_dma_req_21 0x16: hwobs_sdma_dma_req_22 0x17: hwobs_sdma_dma_req_23 0x18: hwobs_sdma_dma_req_24	RW	0x01

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Bits	Field Name	Description	Type	Reset
		0x19: hwobs_sdma_dma_req_25		
		0x1A: hwobs_sdma_dma_req_26		
		0x1B: hwobs_sdma_dma_req_27		
		0x1C: hwobs_sdma_dma_req_28		
		0x1D: hwobs_sdma_dma_req_29		
		0x1E: hwobs_sdma_dma_req_30		
		0x1F: hwobs_sdma_dma_req_31		
		0x20: hwobs_sdma_dma_req_32		
		0x21: hwobs_sdma_dma_req_33		
		0x22: hwobs_sdma_dma_req_34		
		0x23: hwobs_sdma_dma_req_35		
		0x24: hwobs_sdma_dma_req_36		
		0x25: hwobs_sdma_dma_req_37		
		0x26: hwobs_sdma_dma_req_38		
		0x27: hwobs_sdma_dma_req_39		
		0x28: hwobs_sdma_dma_req_40		
		0x29: hwobs_sdma_dma_req_41		
		0x2A: hwobs_sdma_dma_req_42		
		0x2B: hwobs_sdma_dma_req_43		
		0x2C: hwobs_sdma_dma_req_44		
		0x2D: hwobs_sdma_dma_req_45		
		0x2E: hwobs_sdma_dma_req_46		
		0x2F: hwobs_sdma_dma_req_47		
		0x30: hwobs_sdma_dma_req_48		
		0x31: hwobs_sdma_dma_req_49		
		0x32: hwobs_sdma_dma_req_50		
		0x33: hwobs_sdma_dma_req_51		
		0x34: hwobs_sdma_dma_req_52		
		0x35: hwobs_sdma_dma_req_53		
		0x36: hwobs_sdma_dma_req_54		
		0x37: hwobs_sdma_dma_req_55		
		0x38: hwobs_sdma_dma_req_56		
		0x39: hwobs_sdma_dma_req_57		
		0x3A: hwobs_sdma_dma_req_58		
		0x3B: hwobs_sdma_dma_req_59		
		0x3C: hwobs_sdma_dma_req_60		
		0x3D: hwobs_sdma_dma_req_61		
		0x3E: hwobs_sdma_dma_req_62		
		0x3F: hwobs_sdma_dma_req_63		
		0x40: hwobs_sdma_dma_req_64		
		0x41: hwobs_sdma_dma_req_65		
		0x42: hwobs_sdma_dma_req_66		
		0x43: hwobs_sdma_dma_req_67		
		0x44: hwobs_sdma_dma_req_68		
		0x45: hwobs_sdma_dma_req_69		
		0x46: hwobs_sdma_dma_req_70		
		0x47: hwobs_sdma_dma_req_71		
		0x48: hwobs_sdma_dma_req_72		
		0x49: hwobs_sdma_dma_req_73		

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Bits	Field Name	Description	Type	Reset
		0x4A: hwobs_sdma_dma_req_74		
		0x4B: hwobs_sdma_dma_req_75		
		0x4C: hwobs_sdma_dma_req_76		
		0x4D: hwobs_sdma_dma_req_77		
		0x4E: hwobs_sdma_dma_req_78		
		0x4F: hwobs_sdma_dma_req_79		
		0x50: hwobs_sdma_dma_req_80		
		0x51: hwobs_sdma_dma_req_81		
		0x52: hwobs_sdma_dma_req_82		
		0x53: hwobs_sdma_dma_req_83		
		0x54: hwobs_sdma_dma_req_84		
		0x55: hwobs_sdma_dma_req_85		
		0x56: hwobs_sdma_dma_req_86		
		0x57: hwobs_sdma_dma_req_87		
		0x58: hwobs_sdma_dma_req_88		
		0x59: hwobs_sdma_dma_req_89		
		0x5A: hwobs_sdma_dma_req_90		
		0x5B: hwobs_sdma_dma_req_91		
		0x5C: hwobs_sdma_dma_req_92		
		0x5D: hwobs_sdma_dma_req_93		
		0x5E: hwobs_sdma_dma_req_94		
		0x5F: hwobs_sdma_dma_req_95		
		0x60: hwobs_sdma_dma_req_96		
		0x61: hwobs_sdma_dma_req_97		
		0x62: hwobs_sdma_dma_req_98		
		0x63: hwobs_sdma_dma_req_99		
		0x64: hwobs_sdma_dma_req_100		
		0x65: hwobs_sdma_dma_req_101		
		0x66: hwobs_sdma_dma_req_102		
		0x67: hwobs_sdma_dma_req_103		
		0x68: hwobs_sdma_dma_req_104		
		0x69: hwobs_sdma_dma_req_105		
		0x6A: hwobs_sdma_dma_req_106		
		0x6B: hwobs_sdma_dma_req_107		
		0x6C: hwobs_sdma_dma_req_108		
		0x6D: hwobs_sdma_dma_req_109		
		0x6E: hwobs_sdma_dma_req_110		
		0x6F: hwobs_sdma_dma_req_111		
		0x70: hwobs_sdma_dma_req_112		
		0x71: hwobs_sdma_dma_req_113		
		0x72: hwobs_sdma_dma_req_114		
		0x73: hwobs_sdma_dma_req_115		
		0x74: hwobs_sdma_dma_req_116		
		0x75: hwobs_sdma_dma_req_117		
		0x76: hwobs_sdma_dma_req_118		
		0x77: hwobs_sdma_dma_req_119		
		0x78: hwobs_sdma_dma_req_120		
		0x79: hwobs_sdma_dma_req_121		
		0x7A: hwobs_sdma_dma_req_122		

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Bits	Field Name	Description	Type	Reset
		0x7B: hwobs_sdma_dma_req_123		
		0x7C: hwobs_sdma_dma_req_124		
		0x7D: hwobs_sdma_dma_req_125		
		0x7E: hwobs_sdma_dma_req_126		

Table 18-233. Register Call Summary for Register CONTROL_CONF_SDMA_REQ_SEL1

Control Module Register Manual

- SYSCTRL_GENERAL_CORE Register Summary: [0]

Table 18-234. CONTROL_CONF_SDMA_REQ_SEL2

Address Offset	0x0000 0434		
Physical Address	0x4A00 2434	**Instance**	SYSCTRL_GENERAL_CORE
Description	System DMA requests view channel 2 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								MULT							

Bits	Field Name	Description	Type	Reset
31:7	RESERVED		R	0x0000000
6:0	MULT	Select one of the following signals:	RW	0x02
		0x0: hwobs_sdma_dma_req_0		
		0x1: hwobs_sdma_dma_req_1		
		0x2: hwobs_sdma_dma_req_2		
		0x3: hwobs_sdma_dma_req_3		
		0x4: hwobs_sdma_dma_req_4		
		0x5: hwobs_sdma_dma_req_5		
		0x6: hwobs_sdma_dma_req_6		
		0x7: hwobs_sdma_dma_req_7		
		0x8: hwobs_sdma_dma_req_8		
		0x9: hwobs_sdma_dma_req_9		
		0xA: hwobs_sdma_dma_req_10		
		0xB: hwobs_sdma_dma_req_11		
		0xC: hwobs_sdma_dma_req_12		
		0xD: hwobs_sdma_dma_req_13		
		0xE: hwobs_sdma_dma_req_14		
		0xF: hwobs_sdma_dma_req_15		
		0x10: hwobs_sdma_dma_req_16		
		0x11: hwobs_sdma_dma_req_17		
		0x12: hwobs_sdma_dma_req_18		
		0x13: hwobs_sdma_dma_req_19		
		0x14: hwobs_sdma_dma_req_20		
		0x15: hwobs_sdma_dma_req_21		
		0x16: hwobs_sdma_dma_req_22		
		0x17: hwobs_sdma_dma_req_23		
		0x18: hwobs_sdma_dma_req_24		
		0x19: hwobs_sdma_dma_req_25		

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Bits	Field Name	Description	Type	Reset
		0x1A: hwobs_sdma_dma_req_26		
		0x1B: hwobs_sdma_dma_req_27		
		0x1C: hwobs_sdma_dma_req_28		
		0x1D: hwobs_sdma_dma_req_29		
		0x1E: hwobs_sdma_dma_req_30		
		0x1F: hwobs_sdma_dma_req_31		
		0x20: hwobs_sdma_dma_req_32		
		0x21: hwobs_sdma_dma_req_33		
		0x22: hwobs_sdma_dma_req_34		
		0x23: hwobs_sdma_dma_req_35		
		0x24: hwobs_sdma_dma_req_36		
		0x25: hwobs_sdma_dma_req_37		
		0x26: hwobs_sdma_dma_req_38		
		0x27: hwobs_sdma_dma_req_39		
		0x28: hwobs_sdma_dma_req_40		
		0x29: hwobs_sdma_dma_req_41		
		0x2A: hwobs_sdma_dma_req_42		
		0x2B: hwobs_sdma_dma_req_43		
		0x2C: hwobs_sdma_dma_req_44		
		0x2D: hwobs_sdma_dma_req_45		
		0x2E: hwobs_sdma_dma_req_46		
		0x2F: hwobs_sdma_dma_req_47		
		0x30: hwobs_sdma_dma_req_48		
		0x31: hwobs_sdma_dma_req_49		
		0x32: hwobs_sdma_dma_req_50		
		0x33: hwobs_sdma_dma_req_51		
		0x34: hwobs_sdma_dma_req_52		
		0x35: hwobs_sdma_dma_req_53		
		0x36: hwobs_sdma_dma_req_54		
		0x37: hwobs_sdma_dma_req_55		
		0x38: hwobs_sdma_dma_req_56		
		0x39: hwobs_sdma_dma_req_57		
		0x3A: hwobs_sdma_dma_req_58		
		0x3B: hwobs_sdma_dma_req_59		
		0x3C: hwobs_sdma_dma_req_60		
		0x3D: hwobs_sdma_dma_req_61		
		0x3E: hwobs_sdma_dma_req_62		
		0x3F: hwobs_sdma_dma_req_63		
		0x40: hwobs_sdma_dma_req_64		
		0x41: hwobs_sdma_dma_req_65		
		0x42: hwobs_sdma_dma_req_66		
		0x43: hwobs_sdma_dma_req_67		
		0x44: hwobs_sdma_dma_req_68		
		0x45: hwobs_sdma_dma_req_69		
		0x46: hwobs_sdma_dma_req_70		
		0x47: hwobs_sdma_dma_req_71		
		0x48: hwobs_sdma_dma_req_72		
		0x49: hwobs_sdma_dma_req_73		
		0x4A: hwobs_sdma_dma_req_74		

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Bits	Field Name	Description	Type	Reset
		0x4B: hwobs_sdma_dma_req_75		
		0x4C: hwobs_sdma_dma_req_76		
		0x4D: hwobs_sdma_dma_req_77		
		0x4E: hwobs_sdma_dma_req_78		
		0x4F: hwobs_sdma_dma_req_79		
		0x50: hwobs_sdma_dma_req_80		
		0x51: hwobs_sdma_dma_req_81		
		0x52: hwobs_sdma_dma_req_82		
		0x53: hwobs_sdma_dma_req_83		
		0x54: hwobs_sdma_dma_req_84		
		0x55: hwobs_sdma_dma_req_85		
		0x56: hwobs_sdma_dma_req_86		
		0x57: hwobs_sdma_dma_req_87		
		0x58: hwobs_sdma_dma_req_88		
		0x59: hwobs_sdma_dma_req_89		
		0x5A: hwobs_sdma_dma_req_90		
		0x5B: hwobs_sdma_dma_req_91		
		0x5C: hwobs_sdma_dma_req_92		
		0x5D: hwobs_sdma_dma_req_93		
		0x5E: hwobs_sdma_dma_req_94		
		0x5F: hwobs_sdma_dma_req_95		
		0x60: hwobs_sdma_dma_req_96		
		0x61: hwobs_sdma_dma_req_97		
		0x62: hwobs_sdma_dma_req_98		
		0x63: hwobs_sdma_dma_req_99		
		0x64: hwobs_sdma_dma_req_100		
		0x65: hwobs_sdma_dma_req_101		
		0x66: hwobs_sdma_dma_req_102		
		0x67: hwobs_sdma_dma_req_103		
		0x68: hwobs_sdma_dma_req_104		
		0x69: hwobs_sdma_dma_req_105		
		0x6A: hwobs_sdma_dma_req_106		
		0x6B: hwobs_sdma_dma_req_107		
		0x6C: hwobs_sdma_dma_req_108		
		0x6D: hwobs_sdma_dma_req_109		
		0x6E: hwobs_sdma_dma_req_110		
		0x6F: hwobs_sdma_dma_req_111		
		0x70: hwobs_sdma_dma_req_112		
		0x71: hwobs_sdma_dma_req_113		
		0x72: hwobs_sdma_dma_req_114		
		0x73: hwobs_sdma_dma_req_115		
		0x74: hwobs_sdma_dma_req_116		
		0x75: hwobs_sdma_dma_req_117		
		0x76: hwobs_sdma_dma_req_118		
		0x77: hwobs_sdma_dma_req_119		
		0x78: hwobs_sdma_dma_req_120		
		0x79: hwobs_sdma_dma_req_121		
		0x7A: hwobs_sdma_dma_req_122		
		0x7B: hwobs_sdma_dma_req_123		

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Bits	Field Name	Description	Type	Reset
		0x7C: hwobs_sdma_dma_req_124		
		0x7D: hwobs_sdma_dma_req_125		
		0x7E: hwobs_sdma_dma_req_126		

Table 18-235. Register Call Summary for Register CONTROL_CONF_SDMA_REQ_SEL2

Control Module Register Manual

- SYSCTRL_GENERAL_CORE Register Summary: [0]

Table 18-236. CONTROL_CONF_SDMA_REQ_SEL3

Address Offset	0x0000 0438		
Physical Address	0x4A00 2438	**Instance**	SYSCTRL_GENERAL_CORE
Description	System DMA requests view channel 3 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								MULT							

Bits	Field Name	Description	Type	Reset
31:7	RESERVED		R	0x0000000
6:0	MULT	Select one of the following signals:	RW	0x03
		0x0: hwobs_sdma_dma_req_0		
		0x1: hwobs_sdma_dma_req_1		
		0x2: hwobs_sdma_dma_req_2		
		0x3: hwobs_sdma_dma_req_3		
		0x4: hwobs_sdma_dma_req_4		
		0x5: hwobs_sdma_dma_req_5		
		0x6: hwobs_sdma_dma_req_6		
		0x7: hwobs_sdma_dma_req_7		
		0x8: hwobs_sdma_dma_req_8		
		0x9: hwobs_sdma_dma_req_9		
		0xA: hwobs_sdma_dma_req_10		
		0xB: hwobs_sdma_dma_req_11		
		0xC: hwobs_sdma_dma_req_12		
		0xD: hwobs_sdma_dma_req_13		
		0xE: hwobs_sdma_dma_req_14		
		0xF: hwobs_sdma_dma_req_15		
		0x10: hwobs_sdma_dma_req_16		
		0x11: hwobs_sdma_dma_req_17		
		0x12: hwobs_sdma_dma_req_18		
		0x13: hwobs_sdma_dma_req_19		
		0x14: hwobs_sdma_dma_req_20		
		0x15: hwobs_sdma_dma_req_21		
		0x16: hwobs_sdma_dma_req_22		
		0x17: hwobs_sdma_dma_req_23		
		0x18: hwobs_sdma_dma_req_24		
		0x19: hwobs_sdma_dma_req_25		
		0x1A: hwobs_sdma_dma_req_26		

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Bits	Field Name	Description	Type	Reset
		0x1B: hwobs_sdma_dma_req_27		
		0x1C: hwobs_sdma_dma_req_28		
		0x1D: hwobs_sdma_dma_req_29		
		0x1E: hwobs_sdma_dma_req_30		
		0x1F: hwobs_sdma_dma_req_31		
		0x20: hwobs_sdma_dma_req_32		
		0x21: hwobs_sdma_dma_req_33		
		0x22: hwobs_sdma_dma_req_34		
		0x23: hwobs_sdma_dma_req_35		
		0x24: hwobs_sdma_dma_req_36		
		0x25: hwobs_sdma_dma_req_37		
		0x26: hwobs_sdma_dma_req_38		
		0x27: hwobs_sdma_dma_req_39		
		0x28: hwobs_sdma_dma_req_40		
		0x29: hwobs_sdma_dma_req_41		
		0x2A: hwobs_sdma_dma_req_42		
		0x2B: hwobs_sdma_dma_req_43		
		0x2C: hwobs_sdma_dma_req_44		
		0x2D: hwobs_sdma_dma_req_45		
		0x2E: hwobs_sdma_dma_req_46		
		0x2F: hwobs_sdma_dma_req_47		
		0x30: hwobs_sdma_dma_req_48		
		0x31: hwobs_sdma_dma_req_49		
		0x32: hwobs_sdma_dma_req_50		
		0x33: hwobs_sdma_dma_req_51		
		0x34: hwobs_sdma_dma_req_52		
		0x35: hwobs_sdma_dma_req_53		
		0x36: hwobs_sdma_dma_req_54		
		0x37: hwobs_sdma_dma_req_55		
		0x38: hwobs_sdma_dma_req_56		
		0x39: hwobs_sdma_dma_req_57		
		0x3A: hwobs_sdma_dma_req_58		
		0x3B: hwobs_sdma_dma_req_59		
		0x3C: hwobs_sdma_dma_req_60		
		0x3D: hwobs_sdma_dma_req_61		
		0x3E: hwobs_sdma_dma_req_62		
		0x3F: hwobs_sdma_dma_req_63		
		0x40: hwobs_sdma_dma_req_64		
		0x41: hwobs_sdma_dma_req_65		
		0x42: hwobs_sdma_dma_req_66		
		0x43: hwobs_sdma_dma_req_67		
		0x44: hwobs_sdma_dma_req_68		
		0x45: hwobs_sdma_dma_req_69		
		0x46: hwobs_sdma_dma_req_70		
		0x47: hwobs_sdma_dma_req_71		
		0x48: hwobs_sdma_dma_req_72		
		0x49: hwobs_sdma_dma_req_73		
		0x4A: hwobs_sdma_dma_req_74		
		0x4B: hwobs_sdma_dma_req_75		

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Bits	Field Name	Description	Type	Reset
		0x4C: hwobs_sdma_dma_req_76		
		0x4D: hwobs_sdma_dma_req_77		
		0x4E: hwobs_sdma_dma_req_78		
		0x4F: hwobs_sdma_dma_req_79		
		0x50: hwobs_sdma_dma_req_80		
		0x51: hwobs_sdma_dma_req_81		
		0x52: hwobs_sdma_dma_req_82		
		0x53: hwobs_sdma_dma_req_83		
		0x54: hwobs_sdma_dma_req_84		
		0x55: hwobs_sdma_dma_req_85		
		0x56: hwobs_sdma_dma_req_86		
		0x57: hwobs_sdma_dma_req_87		
		0x58: hwobs_sdma_dma_req_88		
		0x59: hwobs_sdma_dma_req_89		
		0x5A: hwobs_sdma_dma_req_90		
		0x5B: hwobs_sdma_dma_req_91		
		0x5C: hwobs_sdma_dma_req_92		
		0x5D: hwobs_sdma_dma_req_93		
		0x5E: hwobs_sdma_dma_req_94		
		0x5F: hwobs_sdma_dma_req_95		
		0x60: hwobs_sdma_dma_req_96		
		0x61: hwobs_sdma_dma_req_97		
		0x62: hwobs_sdma_dma_req_98		
		0x63: hwobs_sdma_dma_req_99		
		0x64: hwobs_sdma_dma_req_100		
		0x65: hwobs_sdma_dma_req_101		
		0x66: hwobs_sdma_dma_req_102		
		0x67: hwobs_sdma_dma_req_103		
		0x68: hwobs_sdma_dma_req_104		
		0x69: hwobs_sdma_dma_req_105		
		0x6A: hwobs_sdma_dma_req_106		
		0x6B: hwobs_sdma_dma_req_107		
		0x6C: hwobs_sdma_dma_req_108		
		0x6D: hwobs_sdma_dma_req_109		
		0x6E: hwobs_sdma_dma_req_110		
		0x6F: hwobs_sdma_dma_req_111		
		0x70: hwobs_sdma_dma_req_112		
		0x71: hwobs_sdma_dma_req_113		
		0x72: hwobs_sdma_dma_req_114		
		0x73: hwobs_sdma_dma_req_115		
		0x74: hwobs_sdma_dma_req_116		
		0x75: hwobs_sdma_dma_req_117		
		0x76: hwobs_sdma_dma_req_118		
		0x77: hwobs_sdma_dma_req_119		
		0x78: hwobs_sdma_dma_req_120		
		0x79: hwobs_sdma_dma_req_121		
		0x7A: hwobs_sdma_dma_req_122		
		0x7B: hwobs_sdma_dma_req_123		
		0x7C: hwobs_sdma_dma_req_124		

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Bits	Field Name	Description	Type	Reset
		0x7D: hwobs_sdma_dma_req_125 0x7E: hwobs_sdma_dma_req_126		

Table 18-237. Register Call Summary for Register CONTROL_CONF_SDMA_REQ_SEL3

Control Module Functional Description • Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0] [1]
Control Module Programming Guide • Operational Modes Configuration: [2]
Control Module Register Manual • SYSCTRL_GENERAL_CORE Register Summary: [3]

Table 18-238. CONTROL_CONF_CLK_SEL0

Address Offset	0x0000 0440		
Physical Address	0x4A00 2440	**Instance**	SYSCTRL_GENERAL_CORE
Description	clk view channel 0 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														MULT	

Bits	Field Name	Description	Type	Reset
31:3	RESERVED		R	0x0000 0000
2:0	MULT	Select one of the following signals: 0x0: hwobs_coredpll_clkout 0x1: hwobs_abedpll_clkout 0x2: hwobs_perdpll_clkout 0x3: hwobs_dsi1dpll_clkout 0x4: hwobs_dsi2dpll_clkout 0x5: reserved 0x6: hwobs_usbdpll_clkout 0x7: reserved	RW	0x0

Table 18-239. Register Call Summary for Register CONTROL_CONF_CLK_SEL0

Control Module Functional Description • Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0] [1]
Control Module Programming Guide • Operational Modes Configuration: [2]
Control Module Register Manual • SYSCTRL_GENERAL_CORE Register Summary: [3]

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Table 18-240. CONTROL_CONF_CLK_SEL1

Address Offset	0x0000 0444		
Physical Address	0x4A00 2444	**Instance**	SYSCTRL_GENERAL_CORE
Description	clk view channel 1 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													MULT		

Bits	Field Name	Description	Type	Reset
31:3	RESERVED		R	0x0000 0000
2:0	MULT	Select one of the following signals: 0x0: hwobs_coredpll_clkout 0x1: hwobs_abedpll_clkout 0x2: hwobs_perdpll_clkout 0x3: hwobs_dsi1dpll_clkout 0x4: hwobs_dsi2dpll_clkout 0x5: reserved 0x6: hwobs_usbdpll_clkout 0x7: reserved	RW	0x1

Table 18-241. Register Call Summary for Register CONTROL_CONF_CLK_SEL1

Control Module Register Manual

- SYSCTRL_GENERAL_CORE Register Summary: [0]

Table 18-242. CONTROL_CONF_CLK_SEL2

Address Offset	0x0000 0448		
Physical Address	0x4A00 2448	**Instance**	SYSCTRL_GENERAL_CORE
Description	clk view channel 2 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													MULT		

Bits	Field Name	Description	Type	Reset
31:3	RESERVED		R	0x0000 0000
2:0	MULT	Select one of the following signals: 0x0: hwobs_coredpll_clkout 0x1: hwobs_abedpll_clkout 0x2: hwobs_perdpll_clkout 0x3: hwobs_dsi1dpll_clkout 0x4: hwobs_dsi2dpll_clkout 0x5: reserved 0x6: hwobs_usbdpll_clkout 0x7: reserved	RW	0x2

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Table 18-243. Register Call Summary for Register CONTROL_CONF_CLK_SEL2

Control Module Functional Description • Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0] [1]
Control Module Programming Guide • Operational Modes Configuration: [2]
Control Module Register Manual • SYSCTRL_GENERAL_CORE Register Summary: [3]

Table 18-244. CONTROL_CONF_DPLL_FREQLOCK_SEL

Address Offset	0x0000 044C		
Physical Address	0x4A00 244C	**Instance**	SYSCTRL_GENERAL_CORE
Description	dpll_freqlock view Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														MULT	

Bits	Field Name	Description	Type	Reset
31:3	RESERVED		R	0x0000 0000
2:0	MULT	Select one of the following signals: 0x0: hwobs_coredpll_freqlock 0x1: hwobs_abedpll_freqlock 0x2: hwobs_perdpll_freqlock 0x3: hwobs_dsi1dpll_freqlock 0x4: hwobs_dsi2dpll_freqlock 0x5: reserved 0x6: hwobs_usbdpll_freqlock 0x7: reserved	RW	0x0

Table 18-245. Register Call Summary for Register CONTROL_CONF_DPLL_FREQLOCK_SEL

Control Module Functional Description • Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0] [1] • Observability Signals Sourced at Module Level: [2] [3] [4] [5] [6] [7]
Control Module Programming Guide • Operational Modes Configuration: [8]
Control Module Register Manual • SYSCTRL_GENERAL_CORE Register Summary: [9]

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Table 18-246. CONTROL_CONF_DPLL_TINITZ_SEL

Address Offset	0x0000 0450		
Physical Address	0x4A00 2450	**Instance**	SYSCTRL_GENERAL_CORE
Description	dpll_tinitz view Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														MULT	

Bits	Field Name	Description	Type	Reset
31:3	RESERVED		R	0x0000 0000
2:0	MULT	Select one of the following signals: 0x0: hwobs_coredpll_tinitz	RW	0x0

Table 18-247. Register Call Summary for Register CONTROL_CONF_DPLL_TINITZ_SEL

Control Module Functional Description • Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0] [1]
Control Module Programming Guide • Operational Modes Configuration: [2]
Control Module Register Manual • SYSCTRL_GENERAL_CORE Register Summary: [3]

Table 18-248. CONTROL_CONF_DPLL_PHASELOCK_SEL

Address Offset	0x0000 0454		
Physical Address	0x4A00 2454	**Instance**	SYSCTRL_GENERAL_CORE
Description	dpll_phaselock view Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														MULT	

Bits	Field Name	Description	Type	Reset
31:3	RESERVED		R	0x0000 0000
2:0	MULT	Select one of the following signals: 0x0: hwobs_coredpll_phaselock 0x1: hwobs_abedpll_phaselock 0x2: hwobs_perdpll_phaselock 0x3: hwobs_dsi1dpll_phaselock 0x4: hwobs_dsi2dpll_phaselock 0x5: reserved 0x6: hwobs_usbdpll_phaselock 0x7: reserved	RW	0x0

Table 18-249. Register Call Summary for Register CONTROL_CONF_DPLL_PHASELOCK_SEL

Control Module Functional Description • Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0] [1]
Control Module Programming Guide • Operational Modes Configuration: [2]

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Table 18-249. Register Call Summary for Register CONTROL_CONF_DPLL_PHASELOCK_SEL (continued)

Control Module Register Manual • SYSCTRL_GENERAL_CORE Register Summary: [3]

Table 18-250. CONTROL_CONF_DPLL_TENABLE_SEL

Address Offset	0x0000 045C		
Physical Address	0x4A00 245C	**Instance**	SYSCTRL_GENERAL_CORE
Description	dpll_tenable view Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														MULT	

Bits	Field Name	Description	Type	Reset
31:3	RESERVED		R	0x0000 0000
2:0	MULT	Select one of the following signals: 0x0: hwobs_coredpll_tenable 0x1: hwobs_abedpll_tenable 0x2: hwobs_perdpll_tenable 0x3: hwobs_dsi1dpll_tenable 0x4: hwobs_dsi2dpll_tenable 0x5: reserved 0x6: hwobs_usbdpll_tenable 0x7: reserved	RW	0x0

Table 18-251. Register Call Summary for Register CONTROL_CONF_DPLL_TENABLE_SEL

Control Module Functional Description • Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0] [1]
Control Module Programming Guide • Operational Modes Configuration: [2]
Control Module Register Manual • SYSCTRL_GENERAL_CORE Register Summary: [3]

Table 18-252. CONTROL_CONF_DPLL_TENABLEDIV_SEL

Address Offset	0x0000 0460		
Physical Address	0x4A00 2460	**Instance**	SYSCTRL_GENERAL_CORE
Description	dpll_tenablediv view Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														MULT	

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Bits	Field Name	Description	Type	Reset
31:3	RESERVED		R	0x0000 0000
2:0	MULT	Select one of the following signals: 0x0: hwobs_coredpll_tenablediv 0x1: hwobs_abedpll_tenablediv 0x2: hwobs_perdpll_tenablediv 0x3: hwobs_dsi1dpll_tenablediv 0x4: hwobs_dsi2dpll_tenablediv 0x5: reserved 0x6: hwobs_usbdpll_tenablediv 0x7: reserved	RW	0x0

Table 18-253. Register Call Summary for Register CONTROL_CONF_DPLL_TENABLEDIV_SEL

Control Module Functional Description • Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0] [1]
Control Module Programming Guide • Operational Modes Configuration: [2]
Control Module Register Manual • SYSCTRL_GENERAL_CORE Register Summary: [3]

Table 18-254. CONTROL_CONF_DPLL_BYPASSACK_SEL

Address Offset	0x0000 0464		
Physical Address	0x4A00 2464	**Instance**	SYSCTRL_GENERAL_CORE
Description	dpll_bypassack view Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														MULT	

Bits	Field Name	Description	Type	Reset
31:3	RESERVED		R	0x0000 0000
2:0	MULT	Select one of the following signals: 0x0: hwobs_coredpll_bypassack 0x1: hwobs_abedpll_bypassack 0x2: hwobs_perdpll_bypassack 0x3: hwobs_dsi1dpll_bypassack 0x4: hwobs_dsi2dpll_bypassack 0x5: reserved 0x6: hwobs_usbdpll_bypassack 0x7: reserved	RW	0x0

Table 18-255. Register Call Summary for Register CONTROL_CONF_DPLL_BYPASSACK_SEL

Control Module Functional Description • Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0] [1]
Control Module Programming Guide • Operational Modes Configuration: [2]
Control Module Register Manual • SYSCTRL_GENERAL_CORE Register Summary: [3]

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Table 18-256. CONTROL_CONF_DPLL_IDLE_SEL

Address Offset	0x0000 0468		
Physical Address	0x4A00 2468	**Instance**	SYSCTRL_GENERAL_CORE
Description	dpll_idle view Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													MULT		

Bits	Field Name	Description	Type	Reset
31:3	RESERVED		R	0x0000 0000
2:0	MULT	Select one of the following signals: 0x0: hwobs_coredpll_idle 0x1: hwobs_abedpll_idle 0x2: hwobs_perdpll_idle 0x3: hwobs_dsi1dpll_idle 0x4: hwobs_dsi2dpll_idle 0x5: reserved 0x6: hwobs_usbdpll_idle 0x7: reserved	RW	0x0

Table 18-257. Register Call Summary for Register CONTROL_CONF_DPLL_IDLE_SEL

Control Module Functional Description
- Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0] [1]
- Observability Signals Sourced at Module Level: [2] [3] [4] [5] [6] [7]

Control Module Programming Guide
- Operational Modes Configuration: [8]

Control Module Register Manual
- SYSCTRL_GENERAL_CORE Register Summary: [9]

Table 18-258. CONTROL_CORE_CONF_DEBUG_SEL_TST_0

Address Offset	0x0000 0480		
Physical Address	0x4A00 2480	**Instance**	SYSCTRL_GENERAL_CORE
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0000000
3:0	MODE	Select one of the following signals: 0x0: hwobs_int_mpu_0 0x1: clk_view_0 0x2: reserved 0x3: reserved 0x4: This information is not available in the public domain. 0x5: hwobs_int_cm2_0 0x6: hwobs_int_ivahd_0 0x7: reserved	RW	0x0

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Bits	Field Name	Description	Type	Reset
		0x8: hwobs_int_abe_0 0x9:This information is not available in the public domain. 0xA: reserved 0xB: reserved 0xC:This information is not available in the public domain.		

Table 18-259. Register Call Summary for Register CONTROL_CORE_CONF_DEBUG_SEL_TST_0

Control Module Functional Description • Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0] [1] [2]
Control Module Programming Guide • Operational Modes Configuration: [3]
Control Module Register Manual • SYSCTRL_GENERAL_CORE Register Summary: [4]

Table 18-260. CONTROL_CORE_CONF_DEBUG_SEL_TST_1

Address Offset	0x0000 0484		
Physical Address	0x4A00 2484	**Instance**	SYSCTRL_GENERAL_CORE
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												MODE			

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0000000
3:0	MODE	Select one of the following signals: 0x0: hwobs_int_mpu_1 0x1: clk_view_1 0x2: reserved 0x3: reserved 0x4: reserved 0x5: hwobs_int_cm2_1 0x6: hwobs_int_ivahd_1 0x7: reserved 0x8: hwobs_int_abe_1 0x9: This information is not available in the public domain. 0xA: reserved 0xB: reserved	RW	0x0

Table 18-261. Register Call Summary for Register CONTROL_CORE_CONF_DEBUG_SEL_TST_1

Control Module Functional Description • Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0]
Control Module Register Manual • SYSCTRL_GENERAL_CORE Register Summary: [1]

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Table 18-262. CONTROL_CORE_CONF_DEBUG_SEL_TST_2

Address Offset	0x0000 0488		
Physical Address	0x4A00 2488	**Instance**	SYSCTRL_GENERAL_CORE
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												MODE			

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0000000
3:0	MODE	Select one of the following signals: 0x0: hwobs_int_mpu_2 0x1: clk_view_2 0x2: reserved 0x3: reserved 0x4: reserved 0x5: hwobs_int_cm2_2 0x6: hwobs_int_ivahd_2 0x7: reserved 0x8: hwobs_int_abe_2 0x9: This information is not available in the public domain. 0xA: reserved 0xB: reserved	RW	0x0

Table 18-263. Register Call Summary for Register CONTROL_CORE_CONF_DEBUG_SEL_TST_2

Control Module Functional Description

- Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0]

Control Module Register Manual

- SYSCTRL_GENERAL_CORE Register Summary: [1]

Table 18-264. CONTROL_CORE_CONF_DEBUG_SEL_TST_3

Address Offset	0x0000 048C		
Physical Address	0x4A00 248C	**Instance**	SYSCTRL_GENERAL_CORE
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												MODE			

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0000000
3:0	MODE	Select one of the following signals: 0x0: hwobs_int_mpu_3 0x1: dpll_freqlock 0x2: reserved 0x3: reserved	RW	0x0

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Bits	Field Name	Description	Type	Reset
		0x4: reserved		
		0x5: hwobs_int_cm2_3		
		0x6: hwobs_int_ivahd_3		
		0x7: reserved		
		0x8: hwobs_int_abe_3		
		0x9: This information is not available in the public domain.		
		0xA: reserved		
		0xB: reserved		

Table 18-265. Register Call Summary for Register CONTROL_CORE_CONF_DEBUG_SEL_TST_3

Control Module Functional Description • Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0]
Control Module Register Manual • SYSCTRL_GENERAL_CORE Register Summary: [1]

Table 18-266. CONTROL_CORE_CONF_DEBUG_SEL_TST_4

Address Offset	0x0000 0490		
Physical Address	0x4A00 2490	**Instance**	SYSCTRL_GENERAL_CORE
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												MODE			

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0000000
3:0	MODE	Select one of the following signals:	RW	0x0
		0x0: hwobs_int_mpu_4		
		0x1: dpll_tinitz		
		0x2: reserved		
		0x3: reserved		
		0x4: reserved		
		0x5: hwobs_int_cm2_4		
		0x6: hwobs_int_ivahd_4		
		0x7: reserved		
		0x8: hwobs_int_abe_4		
		0x9: This information is not available in the public domain.		
		0xA: reserved		
		0xB: reserved		

Table 18-267. Register Call Summary for Register CONTROL_CORE_CONF_DEBUG_SEL_TST_4

Control Module Functional Description • Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0]
Control Module Register Manual • SYSCTRL_GENERAL_CORE Register Summary: [1]

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Table 18-268. CONTROL_CORE_CONF_DEBUG_SEL_TST_5

Address Offset	0x0000 0494		
Physical Address	0x4A00 2494	**Instance**	SYSCTRL_GENERAL_CORE
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												MODE			

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0000000
3:0	MODE	Select one of the following signals: 0x0: hwobs_int_mpu_5 0x1: dpll_phaselock 0x2: reserved 0x3: reserved 0x4: reserved 0x5: hwobs_int_cm2_5 0x6: hwobs_int_ivahd_5 0x7: reserved 0x8: hwobs_int_abe_5 0x9: This information is not available in the public domain. 0xA: reserved 0xB: reserved	RW	0x0

Table 18-269. Register Call Summary for Register CONTROL_CORE_CONF_DEBUG_SEL_TST_5

Control Module Functional Description

- Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0]

Control Module Register Manual

- SYSCTRL_GENERAL_CORE Register Summary: [1]

Table 18-270. CONTROL_CORE_CONF_DEBUG_SEL_TST_6

Address Offset	0x0000 0498		
Physical Address	0x4A00 2498	**Instance**	SYSCTRL_GENERAL_CORE
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												MODE			

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0000000
3:0	MODE	Select one of the following signals: 0x0: hwobs_int_mpu_6 0x1: reserved 0x2: reserved 0x3: reserved	RW	0x0

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Bits	Field Name	Description	Type	Reset
		0x4: reserved		
		0x5: hwobs_int_cm2_6		
		0x6: hwobs_int_ivahd_6		
		0x7: reserved		
		0x8: hwobs_int_abe_6		
		0x9: This information is not available in the public domain.		
		0xA: reserved		
		0xB: reserved		

Table 18-271. Register Call Summary for Register CONTROL_CORE_CONF_DEBUG_SEL_TST_6

Control Module Functional Description • Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0]
Control Module Register Manual • SYSCTRL_GENERAL_CORE Register Summary: [1]

Table 18-272. CONTROL_CORE_CONF_DEBUG_SEL_TST_7

Address Offset	0x0000 049C		
Physical Address	0x4A00 249C	**Instance**	SYSCTRL_GENERAL_CORE
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												MODE			

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0000000
3:0	MODE	Select one of the following signals:	RW	0x0
		0x0: hwobs_int_mpu_7		
		0x1: dpll_tenable		
		0x2: sdma_req_view_0		
		0x3: reserved		
		0x4: reserved		
		0x5: hwobs_int_cm2_7		
		0x6: hwobs_int_ivahd_7		
		0x7: reserved		
		0x8: hwobs_int_abe_7		
		0x9: This information is not available in the public domain.		
		0xA: reserved		
		0xB: reserved		

Table 18-273. Register Call Summary for Register CONTROL_CORE_CONF_DEBUG_SEL_TST_7

Control Module Functional Description • Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0]
Control Module Register Manual • SYSCTRL_GENERAL_CORE Register Summary: [1]

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Table 18-274. CONTROL_CORE_CONF_DEBUG_SEL_TST_8

Address Offset	0x0000 04A0		
Physical Address	0x4A00 24A0	**Instance**	SYSCTRL_GENERAL_CORE
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												MODE			

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0000000
3:0	MODE	Select one of the following signals: 0x0: hwobs_int_mpu_8 0x1: dpll_tenablediv 0x2: sdma_req_view_1 0x3: reserved 0x4: reserved 0x5: hwobs_int_cm2_8 0x6: hwobs_int_ivahd_8 0x7: reserved 0x8: hwobs_int_abe_8 0x9: This information is not available in the public domain. 0xA: reserved 0xB: reserved	RW	0x0

Table 18-275. Register Call Summary for Register CONTROL_CORE_CONF_DEBUG_SEL_TST_8

Control Module Functional Description

- Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0]

Control Module Register Manual

- SYSCTRL_GENERAL_CORE Register Summary: [1]

Table 18-276. CONTROL_CORE_CONF_DEBUG_SEL_TST_9

Address Offset	0x0000 04A4		
Physical Address	0x4A00 24A4	**Instance**	SYSCTRL_GENERAL_CORE
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												MODE			

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Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0000000
3:0	MODE	Select one of the following signals: 0x0: hwobs_int_mpu_9 0x1: dpll_bypassack 0x2: sdma_req_view_2 0x3: reserved 0x4: reserved 0x5: hwobs_int_cm2_9 0x6: hwobs_int_ivahd_9 0x7: reserved 0x8: hwobs_int_abe_9 0x9: This information is not available in the public domain. 0xA: reserved 0xB: hwobs_dssvenctvdetgp	RW	0x0

Table 18-277. Register Call Summary for Register CONTROL_CORE_CONF_DEBUG_SEL_TST_9

Control Module Functional Description
- Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0]

Control Module Register Manual
- SYSCTRL_GENERAL_CORE Register Summary: [1]

Table 18-278. CONTROL_CORE_CONF_DEBUG_SEL_TST_10

Address Offset	0x0000 04A8		
Physical Address	0x4A00 24A8	**Instance**	SYSCTRL_GENERAL_CORE
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												MODE			

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0000000
3:0	MODE	Select one of the following signals: 0x0: hwobs_int_mpu_10 0x1: dpll_idle 0x2: sdma_req_view_3 0x3: reserved 0x4: reserved 0x5: hwobs_int_cm2_10 0x6: hwobs_int_ivahd_10 0x7: reserved 0x8: hwobs_int_abe_10 0x9: This information is not available in the public domain. 0xA: reserved 0xB: hwobs_dssdacpwrdndaczcvbs_y	RW	0x0

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Table 18-279. Register Call Summary for Register CONTROL_CORE_CONF_DEBUG_SEL_TST_10

Control Module Functional Description • Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0]
Control Module Register Manual • SYSCTRL_GENERAL_CORE Register Summary: [1]

Table 18-280. CONTROL_CORE_CONF_DEBUG_SEL_TST_11

Address Offset	0x0000 04AC		
Physical Address	0x4A00 24AC	**Instance**	SYSCTRL_GENERAL_CORE
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												MODE			

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0000000
3:0	MODE	Select one of the following signals: 0x0: hwobs_int_mpu_11 0x1: hwobs_hsusbotg_sofpulse 0x2: sdma_req_view_all 0x3: reserved 0x4: reserved 0x5: hwobs_int_cm2_11 0x6: hwobs_int_ivahd_11 0x7: reserved 0x8: hwobs_int_abe_11 0x9: This information is not available in the public domain. 0xA: reserved 0xB: hwobs_dssdacpwrdndaczchroma	RW	0x0

Table 18-281. Register Call Summary for Register CONTROL_CORE_CONF_DEBUG_SEL_TST_11

Control Module Functional Description • Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0] • Observability Signals Sourced at Module Level: [1]
Control Module Register Manual • SYSCTRL_GENERAL_CORE Register Summary: [2]

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Table 18-282. CONTROL_CORE_CONF_DEBUG_SEL_TST_12

Address Offset	0x0000 04B0		
Physical Address	0x4A00 24B0	**Instance**	SYSCTRL_GENERAL_CORE
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												MODE			

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0000000
3:0	MODE	Select one of the following signals: 0x0: hwobs_int_mpu_12 0x1: reserved 0x2: hwobs_coredivider_clkout3 0x3: reserved 0x4: reserved 0x5: hwobs_int_cm2_12 0x6: hwobs_int_ivahd_12 0x7: reserved 0x8: hwobs_int_abe_12 0x9: This information is not available in the public domain. 0xA: reserved 0xB: hwobs_dssdacpwrdndaccvbs	RW	0x0

Table 18-283. Register Call Summary for Register CONTROL_CORE_CONF_DEBUG_SEL_TST_12

Control Module Functional Description

- Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0]

Control Module Register Manual

- SYSCTRL_GENERAL_CORE Register Summary: [1]

Table 18-284. CONTROL_CORE_CONF_DEBUG_SEL_TST_13

Address Offset	0x0000 04B4		
Physical Address	0x4A00 24B4	**Instance**	SYSCTRL_GENERAL_CORE
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												MODE			

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Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0000000
3:0	MODE	Select one of the following signals: 0x0: hwobs_int_mpu_13 0x1: reserved 0x2: hwobs_perdivider_clkout4 0x3: reserved 0x4: reserved 0x5: hwobs_int_cm2_13 0x6: hwobs_int_ivahd_13 0x7: reserved 0x8: hwobs_int_abe_13 0x9: This information is not available in the public domain. 0xA: reserved 0xB: hwobs_dssdacpwrdnbgz	RW	0x0

Table 18-285. Register Call Summary for Register CONTROL_CORE_CONF_DEBUG_SEL_TST_13

Control Module Functional Description

- Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0]

Control Module Register Manual

- SYSCTRL_GENERAL_CORE Register Summary: [1]

Table 18-286. CONTROL_CORE_CONF_DEBUG_SEL_TST_14

Address Offset	0x0000 04B8		
Physical Address	0x4A00 24B8	**Instance**	SYSCTRL_GENERAL_CORE
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												MODE			

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0000000
3:0	MODE	Select one of the following signals: 0x0: hwobs_int_mpu_14 0x1: reserved 0x2: hwobs_pd_l4_per_per32k_gfclk 0x3: reserved 0x4: reserved 0x5: hwobs_int_cm2_14 0x6: hwobs_int_ivahd_14 0x7: reserved 0x8: hwobs_int_abe_14 0x9: This information is not available in the public domain. 0xA: reserved 0xB: reserved	RW	0x0

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Table 18-287. Register Call Summary for Register CONTROL_CORE_CONF_DEBUG_SEL_TST_14

Control Module Functional Description • Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0]
Control Module Register Manual • SYSCTRL_GENERAL_CORE Register Summary: [1]

Table 18-288. CONTROL_CORE_CONF_DEBUG_SEL_TST_15

Address Offset	0x0000 04BC		
Physical Address	0x4A00 24BC	**Instance**	SYSCTRL_GENERAL_CORE
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												MODE			

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0000000
3:0	MODE	Select one of the following signals: 0x0: hwobs_int_mpu_15 0x1: reserved 0x2: 0 0x3: reserved 0x4: reserved 0x5: hwobs_int_cm2_15 0x6: hwobs_int_ivahd_15 0x7: reserved 0x8: hwobs_int_abe_15 0x9: This information is not available in the public domain. 0xA: reserved 0xB: reserved	RW	0x0

Table 18-289. Register Call Summary for Register CONTROL_CORE_CONF_DEBUG_SEL_TST_15

Control Module Functional Description • Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0]
Control Module Register Manual • SYSCTRL_GENERAL_CORE Register Summary: [1]

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Table 18-290. CONTROL_CORE_CONF_DEBUG_SEL_TST_16

Address Offset	0x0000 04C0		
Physical Address	0x4A00 24C0	**Instance**	SYSCTRL_GENERAL_CORE
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												MODE			

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0000000
3:0	MODE	Select one of the following signals: 0x0: hwobs_int_mpu_16 0x1: reserved 0x2: 0 0x3: reserved 0x4: reserved 0x5: hwobs_int_cm2_16 0x6: hwobs_int_ivahd_16 0x7: reserved 0x8: hwobs_int_abe_16 0x9: This information is not available in the public domain. 0xA: reserved 0xB: reserved	RW	0x0

Table 18-291. Register Call Summary for Register CONTROL_CORE_CONF_DEBUG_SEL_TST_16

Control Module Functional Description

- Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0]

Control Module Register Manual

- SYSCTRL_GENERAL_CORE Register Summary: [1]

Table 18-292. CONTROL_CORE_CONF_DEBUG_SEL_TST_17

Address Offset	0x0000 04C4		
Physical Address	0x4A00 24C4	**Instance**	SYSCTRL_GENERAL_CORE
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												MODE			

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Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0000000
3:0	MODE	Select one of the following signals: 0x0: hwobs_int_mpu_17 0x1: reserved 0x2: 0 0x3: reserved 0x4: reserved 0x5: hwobs_int_cm2_17 0x6: hwobs_int_ivahd_17 0x7: reserved 0x8: hwobs_int_abe_17 0x9: This information is not available in the public domain. 0xA: reserved 0xB: reserved	RW	0x0

Table 18-293. Register Call Summary for Register CONTROL_CORE_CONF_DEBUG_SEL_TST_17

Control Module Functional Description
- Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0]

Control Module Register Manual
- SYSCTRL_GENERAL_CORE Register Summary: [1]

Table 18-294. CONTROL_CORE_CONF_DEBUG_SEL_TST_18

Address Offset	0x0000 04C8		
Physical Address	0x4A00 24C8	**Instance**	SYSCTRL_GENERAL_CORE
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												MODE			

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0000000
3:0	MODE	Select one of the following signals: 0x0: hwobs_int_mpu_18 0x1: reserved 0x2: 0 0x3: reserved 0x4: reserved 0x5: hwobs_int_cm2_18 0x6: hwobs_int_ivahd_18 0x7: reserved 0x8: hwobs_int_abe_18 0x9: This information is not available in the public domain. 0xA: reserved 0xB: reserved	RW	0x0

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Table 18-295. Register Call Summary for Register CONTROL_CORE_CONF_DEBUG_SEL_TST_18

Control Module Functional Description
- Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0]

Control Module Register Manual
- SYSCTRL_GENERAL_CORE Register Summary: [1]

Table 18-296. CONTROL_CORE_CONF_DEBUG_SEL_TST_19

Address Offset	0x0000 04CC		
Physical Address	0x4A00 24CC	**Instance**	SYSCTRL_GENERAL_CORE
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												MODE			

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0000000
3:0	MODE	Select one of the following signals: 0x0: hwobs_int_mpu_19 0x1: reserved 0x2: 0 0x3: reserved 0x4: reserved 0x5: hwobs_int_cm2_19 0x6: hwobs_int_ivahd_19 0x7: reserved 0x8: hwobs_int_abe_19 0x9: This information is not available in the public domain. 0xA: reserved 0xB: reserved	RW	0x0

Table 18-297. Register Call Summary for Register CONTROL_CORE_CONF_DEBUG_SEL_TST_19

Control Module Functional Description
- Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0]

Control Module Register Manual
- SYSCTRL_GENERAL_CORE Register Summary: [1]

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Table 18-298. CONTROL_CORE_CONF_DEBUG_SEL_TST_20

Address Offset	0x0000 04D0		
Physical Address	0x4A00 24D0	**Instance**	SYSCTRL_GENERAL_CORE
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												MODE			

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0000000
3:0	MODE	Select one of the following signals: 0x0: hwobs_int_mpu_20 0x1: reserved 0x2: 0 0x3: reserved 0x4: reserved 0x5: hwobs_int_cm2_20 0x6: hwobs_int_ivahd_20 0x7: reserved 0x8: hwobs_int_abe_20 0x9: This information is not available in the public domain. 0xA: reserved 0xB: reserved	RW	0x0

Table 18-299. Register Call Summary for Register CONTROL_CORE_CONF_DEBUG_SEL_TST_20

Control Module Functional Description

- Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0]

Control Module Register Manual

- SYSCTRL_GENERAL_CORE Register Summary: [1]

Table 18-300. CONTROL_CORE_CONF_DEBUG_SEL_TST_21

Address Offset	0x0000 04D4		
Physical Address	0x4A00 24D4	**Instance**	SYSCTRL_GENERAL_CORE
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												MODE			

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Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0000000
3:0	MODE	Select one of the following signals: 0x0: hwobs_int_mpu_21 0x1: reserved 0x2: 0 0x3: reserved 0x4: reserved 0x5: hwobs_int_cm2_21 0x6: hwobs_int_ivahd_21 0x7: reserved 0x8: hwobs_int_abe_21 0x9: This information is not available in the public domain. 0xA: reserved	RW	0x0

Table 18-301. Register Call Summary for Register CONTROL_CORE_CONF_DEBUG_SEL_TST_21

Control Module Functional Description • Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0]
Control Module Register Manual • SYSCTRL_GENERAL_CORE Register Summary: [1]

Table 18-302. CONTROL_CORE_CONF_DEBUG_SEL_TST_22

Address Offset	0x0000 04D8		
Physical Address	0x4A00 24D8	**Instance**	SYSCTRL_GENERAL_CORE
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								MODE							

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0000000
3:0	MODE	Select one of the following signals: 0x0: hwobs_int_mpu_22 0x1: reserved 0x2: 0 0x3: reserved 0x4: reserved 0x5: hwobs_int_cm2_22 0x6: hwobs_int_ivahd_22 0x7:reserved 0x8: hwobs_int_abe_22 0x9: This information is not available in the public domain. 0xA: reserved	RW	0x0

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Table 18-303. Register Call Summary for Register CONTROL_CORE_CONF_DEBUG_SEL_TST_22

Control Module Functional Description • Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0]
Control Module Register Manual • SYSCTRL_GENERAL_CORE Register Summary: [1]

Table 18-304. CONTROL_CORE_CONF_DEBUG_SEL_TST_23

Address Offset	0x0000 04DC		
Physical Address	0x4A00 24DC	**Instance**	SYSCTRL_GENERAL_CORE
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												MODE			

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0000000
3:0	MODE	Select one of the following signals: 0x0: hwobs_int_mpu_23 0x1: reserved 0x2: 0 0x3: reserved 0x4: reserved 0x5: hwobs_int_cm2_23 0x6: hwobs_int_ivahd_23 0x7: reserved 0x8: hwobs_int_abe_23 0x9: This information is not available in the public domain. 0xA: reserved	RW	0x0

Table 18-305. Register Call Summary for Register CONTROL_CORE_CONF_DEBUG_SEL_TST_23

Control Module Functional Description • Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0]
Control Module Register Manual • SYSCTRL_GENERAL_CORE Register Summary: [1]

Table 18-306. CONTROL_CORE_CONF_DEBUG_SEL_TST_24

Address Offset	0x0000 04E0		
Physical Address	0x4A00 24E0	**Instance**	SYSCTRL_GENERAL_CORE
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												MODE			

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Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0000000
3:0	MODE	Select one of the following signals: 0x0: hwobs_int_mpu_24 0x1: reserved 0x2: 0 0x3: reserved 0x4: reserved 0x5: hwobs_int_cm2_24 0x6: hwobs_int_ivahd_24 0x7: reserved 0x8: hwobs_int_abe_24 0x9: This information is not available in the public domain. 0xA: reserved	RW	0x0

Table 18-307. Register Call Summary for Register CONTROL_CORE_CONF_DEBUG_SEL_TST_24

Control Module Functional Description • Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0]
Control Module Register Manual • SYSCTRL_GENERAL_CORE Register Summary: [1]

Table 18-308. CONTROL_CORE_CONF_DEBUG_SEL_TST_25

Address Offset	0x0000 04E4		
Physical Address	0x4A00 24E4	**Instance**	SYSCTRL_GENERAL_CORE
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												MODE			

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0000000
3:0	MODE	Select one of the following signals: 0x0: hwobs_int_mpu_25 0x1: reserved 0x2: 0 0x3: reserved 0x4: reserved 0x5: hwobs_int_cm2_25 0x6: hwobs_int_ivahd_25 0x7: reserved 0x8: hwobs_int_abe_25 0x9: This information is not available in the public domain. 0xA: reserved	RW	0x0

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Table 18-309. Register Call Summary for Register CONTROL_CORE_CONF_DEBUG_SEL_TST_25

Control Module Functional Description
- Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0]

Control Module Register Manual
- SYSCTRL_GENERAL_CORE Register Summary: [1]

Table 18-310. CONTROL_CORE_CONF_DEBUG_SEL_TST_26

Address Offset	0x0000 04E8		
Physical Address	0x4A00 24E8	**Instance**	SYSCTRL_GENERAL_CORE
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												MODE			

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0000000
3:0	MODE	Select one of the following signals: 0x0: hwobs_int_mpu_26 0x1: reserved 0x2: 0 0x3: reserved 0x4: 0 0x5: hwobs_int_cm2_26 0x6: hwobs_int_ivahd_26 0x7: reserved 0x8: hwobs_int_abe_26 0x9: This information is not available in the public domain. 0xA: reserved	RW	0x0

Table 18-311. Register Call Summary for Register CONTROL_CORE_CONF_DEBUG_SEL_TST_26

Control Module Functional Description
- Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0]

Control Module Register Manual
- SYSCTRL_GENERAL_CORE Register Summary: [1]

Table 18-312. CONTROL_CORE_CONF_DEBUG_SEL_TST_27

Address Offset	0x0000 04EC		
Physical Address	0x4A00 24EC	**Instance**	SYSCTRL_GENERAL_CORE
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												MODE			

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Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0000000
3:0	MODE	Select one of the following signals: 0x0: hwobs_int_mpu_27 0x1: reserved 0x2: 0 0x3: reserved 0x4: 0 0x5: hwobs_int_cm2_27 0x6: hwobs_int_ivahd_27 0x7: reserved 0x8: hwobs_int_abe_27 0x9: This information is not available in the public domain. 0xA: reserved 0xB: 0 0xC: sdma_req_view_0	RW	0x0

Table 18-313. Register Call Summary for Register CONTROL_CORE_CONF_DEBUG_SEL_TST_27

Control Module Functional Description • Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0]
Control Module Register Manual • SYSCTRL_GENERAL_CORE Register Summary: [1]

Table 18-314. CONTROL_CORE_CONF_DEBUG_SEL_TST_28

Address Offset	0x0000 04F0		
Physical Address	0x4A00 24F0	**Instance**	SYSCTRL_GENERAL_CORE
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												MODE			

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Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0000000
3:0	MODE	Select one of the following signals: 0x0: hwobs_int_mpu_28 0x1: reserved 0x2: 0 0x3: reserved 0x4: 0 0x5: hwobs_int_cm2_28 0x6: hwobs_int_ivahd_28 0x7: reserved 0x8: hwobs_int_abe_28 0x9: This information is not available in the public domain. 0xA: reserved 0xB: 0 0xC: sdma_req_view_1	RW	0x0

Table 18-315. Register Call Summary for Register CONTROL_CORE_CONF_DEBUG_SEL_TST_28

Control Module Functional Description • Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0]
Control Module Register Manual • SYSCTRL_GENERAL_CORE Register Summary: [1]

Table 18-316. CONTROL_CORE_CONF_DEBUG_SEL_TST_29

Address Offset	0x0000 04F4		
Physical Address	0x4A00 24F4	**Instance**	SYSCTRL_GENERAL_CORE
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												MODE			

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Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0000000
3:0	MODE	Select one of the following signals: 0x0: hwobs_int_mpu_29 0x1: reserved 0x2: 0 0x3: reserved 0x4: 0 0x5: hwobs_int_cm2_29 0x6: hwobs_int_ivahd_29 0x7: reserved 0x8: hwobs_int_abe_29 0x9: This information is not available in the public domain. 0xA: reserved 0xB: 0 0xC: sdma_req_view_2	RW	0x0

Table 18-317. Register Call Summary for Register CONTROL_CORE_CONF_DEBUG_SEL_TST_29

Control Module Functional Description • Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0]
Control Module Register Manual • SYSCTRL_GENERAL_CORE Register Summary: [1]

Table 18-318. CONTROL_CORE_CONF_DEBUG_SEL_TST_30

Address Offset	0x0000 04F8		
Physical Address	0x4A00 24F8	**Instance**	SYSCTRL_GENERAL_CORE
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												MODE			

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Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0000000
3:0	MODE	Select one of the following signals: 0x0: hwobs_int_mpu_30 0x1: reserved 0x2: 0 0x3: reserved 0x4: 0 0x5: hwobs_int_cm2_30 0x6: hwobs_int_ivahd_30 0x7: reserved 0x8: hwobs_int_abe_30 0x9: This information is not available in the public domain. 0xA: reserved 0xB: 0 0xC: sdma_req_view_3	RW	0x0

Table 18-319. Register Call Summary for Register CONTROL_CORE_CONF_DEBUG_SEL_TST_30

Control Module Functional Description • Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0]
Control Module Register Manual • SYSCTRL_GENERAL_CORE Register Summary: [1]

Table 18-320. CONTROL_CORE_CONF_DEBUG_SEL_TST_31

Address Offset	0x0000 04FC		
Physical Address	0x4A00 24FC	**Instance**	SYSCTRL_GENERAL_CORE
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												MODE			

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Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0000000
3:0	MODE	Select one of the following signals: 0x0: hwobs_int_mpu_31 0x1: reserved 0x2: 0 0x3: reserved 0x4: 0 0x5: hwobs_int_cm2_31 0x6: hwobs_int_ivahd_31 0x7: reserved 0x8: hwobs_int_abe_31 0x9: This information is not available in the public domain. 0xA: reserved 0xB: 0 0xC: sdma_req_view_all	RW	0x0

Table 18-321. Register Call Summary for Register CONTROL_CORE_CONF_DEBUG_SEL_TST_31

Control Module Functional Description • Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0] [1] [2]
Control Module Programming Guide • Operational Modes Configuration: [3]
Control Module Register Manual • SYSCTRL_GENERAL_CORE Register Summary: [4]

18.6.4 SYSCTRL_GENERAL_WKUP Register Summary

Table 18-322. SYSCTRL_GENERAL_WKUP Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	SYSCTRL_GENERAL_WKUP Physical Address
CONTROL_GEN_WKUP_REVISION	R	32	0x0000 0000	0x4A30 C000
CONTROL_GEN_WKUP_HWINFO	R	32	0x0000 0004	0x4A30 C004
CONTROL_GEN_WKUP_SYSCONFIG	RW	32	0x0000 0010	0x4A30 C010
RESERVED	RW	32	0x0000 0104	0x4A30 C104
RESERVED	RW	32	0x0000 0108	0x4A30 C108
CONTROL_OCPREG_SPARE	RW	32	0x0000 010C	0x4A30 C10C
CONTROL_WKUP_PROT_EMIF1_SDRAM_CONFIG_REG	RW	32	0x0000 0110	0x4A30 C110
CONTROL_WKUP_PROT_EMIF1_SDRAM_CONFIG2_REG	RW	32	0x0000 0114	0x4A30 C114
CONTROL_WKUP_PROT_EMIF2_SDRAM_CONFIG_REG	RW	32	0x0000 0118	0x4A30 C118
CONTROL_WKUP_PROT_EMIF2_SDRAM_CONFIG2_REG	RW	32	0x0000 011C	0x4A30 C11C
CONTROL_WKUP_CONF_DEBUG_SEL_TST_i (1)	RW	32	0x0000 0460 + (i*0x004)	0x4A30 C460 + (i*0x004)

(1) i = 0 to 31

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18.6.5 SYSCTRL_GENERAL_WKUP Register Description

Table 18-323. CONTROL_GEN_WKUP_REVISION

Address Offset	0x0000 0000		
Physical Address	0x4A30 C000	**Instance**	SYSCTRL_GENERAL_WKUP
Description	Control module revision identifier Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP Revision	R	See(1)

(1) TI internal data

Table 18-324. Register Call Summary for Register CONTROL_GEN_WKUP_REVISION

Control Module Register Manual
- SYSCTRL_GENERAL_WKUP Register Summary: [0]

Table 18-325. CONTROL_GEN_WKUP_HWINFO

Address Offset	0x0000 0004		
Physical Address	0x4A30 C004	**Instance**	SYSCTRL_GENERAL_WKUP
Description	Information about the IP module hardware configuration that is, typically the module HDL generics (if any). Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IP_HWINFO																															

Bits	Field Name	Description	Type	Reset
31:0	IP_HWINFO	IP-module dependent	R	0x0000 0000

Table 18-326. Register Call Summary for Register CONTROL_GEN_WKUP_HWINFO

Control Module Register Manual
- SYSCTRL_GENERAL_WKUP Register Summary: [0]

Table 18-327. CONTROL_GEN_WKUP_SYSCONFIG

Address Offset	0x0000 0010		
Physical Address	0x4A30 C010	**Instance**	SYSCTRL_GENERAL_WKUP
Description	Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												IP_SYSCONFIG_IDLEMODE		RESERVED	

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0000000
3:2	IP_SYSCONFIG_IDLEMODE	Select the local clock-gating strategy 0x0: Clock is manually gated 0x1: Clock is manually enabled 0x2,0x3: Clock is automatically gated when there is no access to the Control Module through L4-interconnect	RW	0x2
1:0	RESERVED		R	0x0

Table 18-328. Register Call Summary for Register CONTROL_GEN_WKUP_SYSCONFIG

Control Module Functional Description • General Wakeup Control Module Instance: [0]
Control Module Programming Guide • Global Initialization: [1]
Control Module Register Manual • SYSCTRL_GENERAL_WKUP Register Summary: [2]

Table 18-329. CONTROL_OCPREG_SPARE

Address Offset	0x0000 010C		
Physical Address	0x4A30 C10C	**Instance**	SYSCTRL_GENERAL_WKUP
Description	Spare Register Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OCPREG_SPARE31	OCPREG_SPARE30	OCPREG_SPARE29	OCPREG_SPARE28	OCPREG_SPARE27	OCPREG_SPARE26	OCPREG_SPARE25	OCPREG_SPARE24	OCPREG_SPARE23	OCPREG_SPARE22	OCPREG_SPARE21	OCPREG_SPARE20	OCPREG_SPARE19	OCPREG_SPARE18	OCPREG_SPARE17	OCPREG_SPARE16	OCPREG_SPARE15	OCPREG_SPARE14	OCPREG_SPARE13	OCPREG_SPARE12	OCPREG_SPARE11	OCPREG_SPARE10	OCPREG_SPARE9	OCPREG_SPARE8	OCPREG_SPARE7	OCPREG_SPARE6	OCPREG_SPARE5	OCPREG_SPARE4	OCPREG_SPARE3	OCPREG_SPARE2	OCPREG_SPARE1	RESERVED

Bits	Field Name	Description	Type	Reset
31	OCPREG_SPARE31	Spare register 31	RW	0
30	OCPREG_SPARE30	Spare register 30	RW	0
29	OCPREG_SPARE29	Spare register 29	RW	0
28	OCPREG_SPARE28	Spare register 28	RW	0
27	OCPREG_SPARE27	Spare register 27	RW	0
26	OCPREG_SPARE26	Spare register 26	RW	0

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Bits	Field Name	Description	Type	Reset
25	OCPREG_SPARE25	Spare register 25	RW	0
24	OCPREG_SPARE24	Spare register 24	RW	0
23	OCPREG_SPARE23	Spare register 23	RW	0
22	OCPREG_SPARE22	Spare register 22	RW	0
21	OCPREG_SPARE21	Spare register 21	RW	0
20	OCPREG_SPARE20	Spare register 20	RW	0
19	OCPREG_SPARE19	Spare register 19	RW	0
18	OCPREG_SPARE18	Spare register 18	RW	0
17	OCPREG_SPARE17	Spare register 17	RW	0
16	OCPREG_SPARE16	Spare register 16	RW	0
15	OCPREG_SPARE15	Spare register 15	RW	0
14	OCPREG_SPARE14	Spare register 14	RW	0
13	OCPREG_SPARE13	Spare register 13	RW	0
12	OCPREG_SPARE12	Spare register 12	RW	0
11	OCPREG_SPARE11	Spare register 11	RW	0
10	OCPREG_SPARE10	Spare register 10	RW	0
9	OCPREG_SPARE9	Spare register 9	RW	0
8	OCPREG_SPARE8	Spare register 8	RW	0
7	OCPREG_SPARE7	Spare register 7	RW	0
6	OCPREG_SPARE6	Spare register 6	RW	0
5	OCPREG_SPARE5	Spare register 5	RW	0
4	OCPREG_SPARE4	Spare register 4	RW	0
3	OCPREG_SPARE3	Spare register 3	RW	0
2	OCPREG_SPARE2	Spare register 2	RW	0
1	OCPREG_SPARE1	Spare register 1	RW	0
0	RESERVED	Reserved	RW	0

Table 18-330. Register Call Summary for Register CONTROL_OCPREG_SPARE

Control Module Functional Description • General Wakeup Control Module Instance: [0]
Control Module Register Manual • SYSCTRL_GENERAL_WKUP Register Summary: [1]

Table 18-331. CONTROL_WKUP_PROT_EMIF1_SDRAM_CONFIG_REG

Address Offset	0x0000 0100		
Physical Address	0x4A30 C110	**Instance**	SYSCTRL_GENERAL_WKUP
Description	Protection EMIF1 SDRAM configuration register 1 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31 30 29	28 27	26 25 24	23 22 21	20	19 18 17 16	15 14	13 12 11 10	9 8	7 6 5 4	3	2 1 0
EMIF1_SDRAM_TYPE	EMIF1_SDRAM_IBANK_POS	RESERVED	EMIF1_SDRAM_DDR2_DDQS	EMIF1_SDRAM_DDR_DISABLE_DLL	RESERVED	EMIF1_SDRAM_NARROW_MODE	EMIF1_SDRAM_CL	EMIF1_SDRAM_ROWSIZE	EMIF1_SDRAM_IBANK	EMIF1_SDRAM_EBANK	EMIF1_SDRAM_PAGESIZE

Bits	Field Name	Description	Type	Reset
31:29	EMIF1_SDRAM_TYPE	SDRAM type selection: Set to 0x4 for LPDDR2-S4. Set to 0x5 for LPDDR2-S2. All other values are reserved.	RW	0x4
28:27	EMIF1_SDRAM_IBANK_POS	Internal bank position: Set to 0x0 to assign internal bank address bits from the L3 address as shown in Table 15-99, *64-Byte Linear Read Starting at Address 0x0*, and Table 15-100, *64-Byte Linear Read Starting at Address 0x8 (LPDDR2-S2)*, in Chapter 15, *Memory Subsystem*. Set to 0x1, 0x2, or 0x3 to assign internal bank address bits from the L3 address as shown in Table 15-101, *64-Byte Linear Read Starting at Address 0x8 (LPDDR2-S4)*, Table 15-102, *64-Byte Linear Read Starting at Address 0x10*, and Table 15-103, *64-Byte Linear Read Starting at Address 0x18*, in Chapter 15, *Memory Subsystem*.	RW	0x0
26:24	RESERVED		R	0x0
23	EMIF1_SDRAM_DDR2_DDQS	DDR2 differential DQS enable: Set to 0 for single ended DQS. Set to 1 for differential DQS. This bit is only for DDR2 mode; because the device supports LPDDR2, this bit is don't care.	RW	0x1
22:21	RESERVED		R	0x0
20	EMIF1_SDRAM_DDR_DISABLE_DLL	Disable DLL select: Set to 0x0 to enable DLL inside SDRAM. Set to 0x1 to disable DLL inside SDRAM.	RW	0x0
19:16	RESERVED		R	0x0
15:14	EMIF1_SDRAM_NARROW_MODE	SDRAM data bus width: Set to 0x0 for 64-bit width. Set to 0x1 for 32-bit width. Set to 0x2 for 16-bit width. All other values are reserved.	RW	0x0

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Bits	Field Name	Description	Type	Reset
13:10	EMIF1_SDRAM_CL	CAS latency. The value of this field defines the CAS latency to be used when accessing connected SDRAM devices: Supported for LPDDR2-SDRAM: 0x1: CAS latency of 3 cycles 0x2: CAS latency of 4 cycles 0x3: CAS latency of 5 cycles 0x4: CAS latency of 6 cycles 0x5: CAS latency of 7 cycles 0x6: CAS latency of 8 cycles All other values are reserved.	RW	0x3
9:7	EMIF1_SDRAM_ROWSIZE	Row size. Defines the number of row address bits of connected SDRAM devices: Set to 0x0 for 9 row bits. Set to 0x1 for 10 row bits. Set to 0x2 for 11 row bits. Set to 0x3 for 12 row bits. Set to 0x4 for 13 row bits. Set to 0x5 for 14 row bits. Set to 0x6 for 15 row bits. Set to 0x7 for 16 row bits. This field is used only when the ibank_pos field in the SDRAM Config register is set to 0x1, 0x2, or 0x3.	RW	0x4
6:4	EMIF1_SDRAM_IBANK	Internal bank setup. Defines number of banks inside connected SDRAM devices: Set to 0x0 for 1 bank. Set to 0x1 for 2 banks. Set to 0x2 for 4 banks. Set to 0x3 for 8 banks. All other values are reserved.	RW	0x3
3	EMIF1_SDRAM_EBANK	External CS setup. Defines whether SDRAM accesses will use 1 or 2 CS lines. Set to 0 to use pad_cs_o_n[0] only: Set to 0x0 to use only pad_cs_o_n[0]. Set to 0x1 to use pad_cs_o_n[1:0]. This bit is automatically set to 0 if either the cs0nvmen or cs1nvmen field in the LPDDR2-NVM is set to 1.	RW	0x0
2:0	EMIF1_SDRAM_PAGESIZE	Page size. Defines the internal page size of the connected SDRAM devices: Set to 0x0 for 256-word page (8 column bits). Set to 0x1 for 512-word page (9 column bits). Set to 0x2 for 1024-word page (10 column bits). Set to 0x3 for 2048-word page (11 column bits). All other values are reserved.	RW	0x0

Table 18-332. Register Call Summary for Register CONTROL_WKUP_PROT_EMIF1_SDRAM_CONFIG_REG

Control Module Register Manual

- SYSCTRL_GENERAL_WKUP Register Summary: [0]

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Table 18-333. CONTROL_WKUP_PROT_EMIF1_SDRAM_CONFIG2_REG

Address Offset	0x0000 0114		
Physical Address	0x4A30 C114	**Instance**	SYSCTRL_GENERAL_WKUP
Description	Protection EMIF1 SDRAM configuration register 2 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	EMIF1_SDRAM_CS1NVMEN	RESERVED																								EMIF1_SDRAM_RDBNUM		RESERVED		EMIF1_SDRAM_RDBSIZE		

Bits	Field Name	Description	Type	Reset
31	RESERVED		R	0x0
30	EMIF1_SDRAM_CS1NVMEN	CS1 LPDDR2-NVM enable: Set to 0x1 if LPDDR2-NVM is connected to CS1. This bit is automatically set to 0x0 if the sdram_type field in the SDRAM Config register is not set to LPDDR2.	RW	0x1
29:6	RESERVED		R	0x000000
5:4	EMIF1_SDRAM_RDBNUM	Row buffer setup. Defines the number of row buffers inside the connected LPDDR2-NVM devices: Set to 0x0 for 1 row buffer. Set to 0x1 for 2 row buffers. Set to 0x2 for 4 row buffers. Set to 0x3 for 8 row buffers. All other values are reserved.	RW	0x1
3	RESERVED		R	0x0
2:0	EMIF1_SDRAM_RDBSIZE	Row data buffer size. Defines the row data buffer size of connected LPDDR2-NVM devices: Set to 0x0 for 32 bytes. Set to 0x1 for 64 bytes. Set to 0x2 for 128 bytes. Set to 0x3 for 256 bytes. Set to 0x4 for 512 bytes. Set to 0x5 for 1024 bytes. Set to 0x6 for 2048 bytes. Set to 0x7 for 4096 bytes.	RW	0x0

Table 18-334. Register Call Summary for Register CONTROL_WKUP_PROT_EMIF1_SDRAM_CONFIG2_REG

Control Module Register Manual

- SYSCTRL_GENERAL_WKUP Register Summary: [0]

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Table 18-335. CONTROL_WKUP_PROT_EMIF2_SDRAM_CONFIG_REG

Address Offset	0x0000 0118		
Physical Address	0x4A30 C118	**Instance**	SYSCTRL_GENERAL_WKUP
Description	Protection EMIF2 SDRAM configuration register 1 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EMIF2_SDRAM_TYPE								EMIF2_SDRAM_DDR2_DDQS			EMIF2_SDRAM_DDR_DISABLE_DLL					EMIF2_SDRAM_NARROW_MODE								EMIF2_SDRAM_IBANK				EMIF2_SDRAM_EBANK			
			EMIF2_SDRAM_IBANK_POS																	EMIF2_SDRAM_CL				EMIF2_SDRAM_ROWSIZE						EMIF2_SDRAM_PAGESIZE		
					RESERVED				RESERVED			RESERVED																				

Bits	Field Name	Description	Type	Reset
31:29	EMIF2_SDRAM_TYPE	SDRAM type selection: Set to 0x4 for LPDDR2-S4. Set to 0x5 for LPDDR2-S2. All other values are reserved.	RW	0x4
28:27	EMIF2_SDRAM_IBANK_POS	Internal bank position: Set to 0x0 to assign internal bank address bits from the L3 address as shown in Table 15-99, *64-Byte Linear Read Starting at Address 0x0*, and Table 15-100, *64-Byte Linear Read Starting at Address 0x8 (LPDDR2-S2)*, in Chapter 15, *Memory Subsystem*. Set to 0x1, 0x2, or 0x3 to assign internal bank address bits from the L3 address as shown in Table 15-101, *64-Byte Linear Read Starting at Address 0x8 (LPDDR2-S4)*, Table 15-102, *64-Byte Linear Read Starting at Address 0x10*, and Table 15-103, *64-Byte Linear Read Starting at Address 0x18*, in Chapter 15, *Memory Subsystem*.	RW	0x0
26:24	RESERVED		R	0x0
23	EMIF2_SDRAM_DDR2_DDQS	DDR2 differential DQS enable: Set to 0 for single ended DQS. Set to 1 for differential DQS. This bit is only for DDR2 mode; because the device supports LPDDR2, this bit is don't care.	RW	0x1
22:21	RESERVED		R	0x0
20	EMIF2_SDRAM_DDR_DISABLE_DLL	Disable DLL select: Set to 0x0 to enable DLL inside SDRAM. Set to 0x1 to disable DLL inside SDRAM.	RW	0x0
19:16	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
15:14	EMIF2_SDRAM_NARROW_MODE	SDRAM data bus width: Set to 0x0 for 64-bit width. Set to 0x1 for 32-bit width. Set to 0x2 for 16-bit width. All other values are reserved.	RW	0x0
13:10	EMIF2_SDRAM_CL	CAS latency. The value of this field defines the CAS latency to be used when accessing connected SDRAM devices: Supported for LPDDR2-SDRAM: 0x1: CAS latency of 3 cycles 0x2: CAS latency of 4 cycles 0x3: CAS latency of 5 cycles 0x4: CAS latency of 6 cycles 0x5: CAS latency of 7 cycles 0x6: CAS latency of 8 cycles All other values are reserved.	RW	0x3
9:7	EMIF2_SDRAM_ROWSIZE	Row size. Defines the number of row address bits of connected SDRAM devices: Set to 0x0 for 9 row bits. Set to 0x1 for 10 row bits. Set to 0x2 for 11 row bits. Set to 0x3 for 12 row bits. Set to 0x4 for 13 row bits. Set to 0x5 for 14 row bits. Set to 0x6 for 15 row bits. Set to 0x7 for 16 row bits. This field is used only when the ibank_pos field in the SDRAM Config register is set to 0x1, 0x2, or 0x3.	RW	0x4
6:4	EMIF2_SDRAM_IBANK	Internal bank setup. Defines number of banks inside connected SDRAM devices: Set to 0x0 for 1 bank. Set to 0x1 for 2 banks. Set to 0x2 for 4 banks. Set to 0x3 for 8 banks. All other values are reserved.	RW	0x3
3	EMIF2_SDRAM_EBANK	External CS setup. Defines whether SDRAM accesses will use 1 or 2 CS lines. Set to 0 to use pad_cs_o_n[0] only: Set to 0x0 to use only pad_cs_o_n[0]. Set to 0x1 to use pad_cs_o_n[1:0]. This bit is automatically set to 0 if either the cs0nvmen or cs1nvmen field in the LPDDR2-NVM is set to 1.	RW	0x0
2:0	EMIF2_SDRAM_PAGESIZE	Page size. Defines the internal page size of the connected SDRAM devices: Set to 0x0 for 256-word page (8 column bits). Set to 0x1 for 512-word page (9 column bits). Set to 0x2 for 1024-word page (10 column bits). Set to 0x3 for 2048-word page (11 column bits). All other values are reserved.	RW	0x0

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Table 18-336. Register Call Summary for Register CONTROL_WKUP_PROT_EMIF2_SDRAM_CONFIG_REG

Control Module Functional Description

- Protection SDRAM Configuration Registers: [0]

Control Module Register Manual

- SYSCTRL_GENERAL_WKUP Register Summary: [1]

Table 18-337. CONTROL_WKUP_PROT_EMIF2_SDRAM_CONFIG2_REG

Address Offset	0x0000 0114		
Physical Address	0x4A30 C11C	**Instance**	SYSCTRL_GENERAL_WKUP
Description	Protection EMIF1 SDRAM configuration register 2 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	EMIF2_SDRAM_CS1NVMEN	RESERVED																								EMIF2_SDRAM_RDBNUM		RESERVED		EMIF2_SDRAM_RDBSIZE		

Bits	Field Name	Description	Type	Reset
31	RESERVED		R	0x0
30	EMIF2_SDRAM_CS1NVMEN	CS1 LPDDR2-NVM enable: Set to 0x1 if LPDDR2-NVM is connected to CS1. This bit is automatically set to 0x0 if the sdram_type field in the SDRAM Config register is not set to LPDDR2.	RW	0x1
29:6	RESERVED		R	0x000000
5:4	EMIF2_SDRAM_RDBNUM	Row buffer setup. Defines the number of row buffers inside the connected LPDDR2-NVM devices: Set to 0x0 for 1 row buffer. Set to 0x1 for 2 row buffers. Set to 0x2 for 4 row buffers. Set to 0x3 for 8 row buffers. All other values are reserved.	RW	0x1
3	RESERVED		R	0x0
2:0	EMIF2_SDRAM_RDBSIZE	Row data buffer size. Defines the row data buffer size of connected LPDDR2-NVM devices: Set to 0x0 for 32 bytes. Set to 0x1 for 64 bytes. Set to 0x2 for 128 bytes. Set to 0x3 for 256 bytes. Set to 0x4 for 512 bytes. Set to 0x5 for 1024 bytes. Set to 0x6 for 2048 bytes. Set to 0x7 for 4096 bytes.	RW	0x0

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Table 18-338. Register Call Summary for Register CONTROL_WKUP_PROT_EMIF2_SDRAM_CONFIG2_REG

Control Module Functional Description • Protection SDRAM Configuration Registers: [0]
Control Module Register Manual • SYSCTRL_GENERAL_WKUP Register Summary: [1]

Table 18-339. CONTROL_WKUP_CONF_DEBUG_SEL_TST_i

Address Offset	0x0000 0460		
Physical Address	0x4A30 C460 + (i*0x004)	**Instance**	SYSCTRL_GENERAL_WKUP
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															MODE

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	MODE	Select one of the following signals: 0x0: hwobs_int_prm_i[1] 0x1: hwobs_int_cm1_i	RW	0

(1) i = 0 to 31

Table 18-340. Register Call Summary for Register CONTROL_WKUP_CONF_DEBUG_SEL_TST_i

Control Module Functional Description • Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0] [1]
Control Module Programming Guide • Operational Modes Configuration: [2]
Control Module Register Manual • SYSCTRL_GENERAL_WKUP Register Summary: [3]

18.6.6 SYSCTRL_PADCONF_CORE Register Summary

Table 18-341. SYSCTRL_PADCONF_CORE Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	SYSCTRL_PADCONF_CORE Physical Address
CONTROL_PADCONF_CORE_REVISION	R	32	0x00000000	0x4A10 0000
CONTROL_PADCONF_CORE_HWINFO	R	32	0x00000004	0x4A10 0004
CONTROL_PADCONF_CORE_SYSCONFIG	RW	32	0x00000010	0x4A10 0010
CONTROL_CORE_PAD0_GPMC_AD0_PAD1_GPMC_AD1	RW	32	0x00000040	0x4A10 0040
CONTROL_CORE_PAD0_GPMC_AD2_PAD1_GPMC_AD3	RW	32	0x00000044	0x4A10 0044
CONTROL_CORE_PAD0_GPMC_AD4_PAD1_GPMC_AD5	RW	32	0x00000048	0x4A10 0048

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Table 18-341. SYSCTRL_PADCONF_CORE Register Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	SYSCTRL_PADCONF_CORE Physical Address
CONTROL_CORE_PAD0_GPMC_AD6_PAD1_GPMC_AD7	RW	32	0x0000004C	0x4A10 004C
CONTROL_CORE_PAD0_GPMC_AD8_PAD1_GPMC_AD9	RW	32	0x00000050	0x4A10 0050
CONTROL_CORE_PAD0_GPMC_AD10_PAD1_GPMC_AD11	RW	32	0x00000054	0x4A10 0054
CONTROL_CORE_PAD0_GPMC_AD12_PAD1_GPMC_AD13	RW	32	0x00000058	0x4A10 0058
CONTROL_CORE_PAD0_GPMC_AD14_PAD1_GPMC_AD15	RW	32	0x0000005C	0x4A10 005C
CONTROL_CORE_PAD0_GPMC_A16_PAD1_GPMC_A17	RW	32	0x00000060	0x4A10 0060
CONTROL_CORE_PAD0_GPMC_A18_PAD1_GPMC_A19	RW	32	0x00000064	0x4A10 0064
CONTROL_CORE_PAD0_GPMC_A20_PAD1_GPMC_A21	RW	32	0x00000068	0x4A10 0068
CONTROL_CORE_PAD0_GPMC_A22_PAD1_GPMC_A23	RW	32	0x0000006C	0x4A10 006C
CONTROL_CORE_PAD0_GPMC_A24_PAD1_GPMC_A25	RW	32	0x00000070	0x4A10 0070
CONTROL_CORE_PAD0_GPMC_NCS0_PAD1_GPMC_NCS1	RW	32	0x00000074	0x4A10 0074
CONTROL_CORE_PAD0_GPMC_NCS2_PAD1_GPMC_NCS3	RW	32	0x00000078	0x4A10 0078
CONTROL_CORE_PAD0_GPMC_NWP_PAD1_GPMC_CLK	RW	32	0x0000007C	0x4A10 007C
CONTROL_CORE_PAD0_GPMC_NADV_ALE_PAD1_GPMC_NOE	RW	32	0x00000080	0x4A10 0080
CONTROL_CORE_PAD0_GPMC_NWE_PAD1_GPMC_NBE0_CLE	RW	32	0x00000084	0x4A10 0084
CONTROL_CORE_PAD0_GPMC_NBE1_PAD1_GPMC_WAIT0	RW	32	0x00000088	0x4A10 0088
CONTROL_CORE_PAD0_GPMC_WAIT1_PAD1_GPMC_WAIT2	RW	32	0x0000008C	0x4A10 008C
CONTROL_CORE_PAD0_GPMC_NCS4_PAD1_GPMC_NCS5	RW	32	0x00000090	0x4A10 0090
CONTROL_CORE_PAD0_GPMC_NCS6_PAD1_GPMC_NCS7	RW	32	0x00000094	0x4A10 0094
CONTROL_CORE_PAD0_GPIO63_PAD1_GPIO64	RW	32	0x00000098	0x4A10 0098
CONTROL_CORE_PAD0_GPIO65_PAD1_GPIO66	RW	32	0x0000009C	0x4A10 009C
CONTROL_CORE_PAD0_CSI21_DX0_PAD1_CSI21_DY0	RW	32	0x000000A0	0x4A10 00A0
CONTROL_CORE_PAD0_CSI21_DX1_PAD1_CSI21_DY1	RW	32	0x000000A4	0x4A10 00A4
CONTROL_CORE_PAD0_CSI21_DX2_PAD1_CSI21_DY2	RW	32	0x000000A8	0x4A10 00A8
CONTROL_CORE_PAD0_CSI21_DX3_PAD1_CSI21_DY3	RW	32	0x000000AC	0x4A10 00AC
CONTROL_CORE_PAD0_CSI21_DX4_PAD1_CSI21_DY4	RW	32	0x000000B0	0x4A10 00B0
CONTROL_CORE_PAD0_CSI22_DX0_PAD1_CSI22_DY0	RW	32	0x000000B4	0x4A10 00B4

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Table 18-341. SYSCTRL_PADCONF_CORE Register Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	SYSCTRL_PADCONF_CORE Physical Address
CONTROL_CORE_PAD0_CSI22_DX1_PAD1_CSI22_DY1	RW	32	0x000000B8	0x4A10 00B8
CONTROL_CORE_PAD0_CAM_SHUTTER_PAD1_CAM_STROBE	RW	32	0x000000BC	0x4A10 00BC
CONTROL_CORE_PAD0_CAM_GLOBALRESET_PAD1_USBB1_ULPITLL_CLK	RW	32	0x000000C0	0x4A10 00C0
CONTROL_CORE_PAD0_USBB1_ULPITLL_STP_PAD1_USBB1_ULPITLL_DIR	RW	32	0x000000C4	0x4A10 00C4
CONTROL_CORE_PAD0_USBB1_ULPITLL_NXT_PAD1_USBB1_ULPITLL_DAT0	RW	32	0x000000C8	0x4A10 00C8
CONTROL_CORE_PAD0_USBB1_ULPITLL_DAT1_PAD1_USBB1_ULPITLL_DAT2	RW	32	0x000000CC	0x4A10 00CC
CONTROL_CORE_PAD0_USBB1_ULPITLL_DAT3_PAD1_USBB1_ULPITLL_DAT4	RW	32	0x000000D0	0x4A10 00D0
CONTROL_CORE_PAD0_USBB1_ULPITLL_DAT5_PAD1_USBB1_ULPITLL_DAT6	RW	32	0x000000D4	0x4A10 00D4
CONTROL_CORE_PAD0_USBB1_ULPITLL_DAT7_PAD1_USBB1_HSIC_DATA	RW	32	0x000000D8	0x4A10 00D8
CONTROL_CORE_PAD0_USBB1_HSIC_STROBE_PAD1_USBC1_ICUSB_DP	RW	32	0x000000DC	0x4A10 00DC
CONTROL_CORE_PAD0_USBC1_ICUSB_DM_PAD1_SDMMC1_CLK	RW	32	0x000000E0	0x4A10 00E0
CONTROL_CORE_PAD0_SDMMC1_CMD_PAD1_SDMMC1_DAT0	RW	32	0x000000E4	0x4A10 00E4
CONTROL_CORE_PAD0_SDMMC1_DAT1_PAD1_SDMMC1_DAT2	RW	32	0x000000E8	0x4A10 00E8
CONTROL_CORE_PAD0_SDMMC1_DAT3_PAD1_SDMMC1_DAT4	RW	32	0x000000EC	0x4A10 00EC
CONTROL_CORE_PAD0_SDMMC1_DAT5_PAD1_SDMMC1_DAT6	RW	32	0x000000F0	0x4A10 00F0
CONTROL_CORE_PAD0_SDMMC1_DAT7_PAD1_ABE_MCBSP2_CLKX	RW	32	0x000000F4	0x4A10 00F4
CONTROL_CORE_PAD0_ABE_MCBSP2_DR_PAD1_ABE_MCBSP2_DX	RW	32	0x000000F8	0x4A10 00F8
CONTROL_CORE_PAD0_ABE_MCBSP2_FSX_PAD1_ABE_MCBSP1_CLKX	RW	32	0x000000FC	0x4A10 00FC
CONTROL_CORE_PAD0_ABE_MCBSP1_DR_PAD1_ABE_MCBSP1_DX	RW	32	0x00000100	0x4A10 0100
CONTROL_CORE_PAD0_ABE_MCBSP1_FSX_PAD1_ABE_PDM_UL_DATA	RW	32	0x00000104	0x4A10 0104
CONTROL_CORE_PAD0_ABE_PDM_DL_DATA_PAD1_ABE_PDM_FRAME	RW	32	0x00000108	0x4A10 0108
CONTROL_CORE_PAD0_ABE_PDM_LB_CLK_PAD1_ABE_CLKS	RW	32	0x0000010C	0x4A10 010C
CONTROL_CORE_PAD0_ABE_DMIC_CLK1_PAD1_ABE_DMIC_DIN1	RW	32	0x00000110	0x4A10 0110
CONTROL_CORE_PAD0_ABE_DMIC_DIN2_PAD1_ABE_DMIC_DIN3	RW	32	0x00000114	0x4A10 0114
CONTROL_CORE_PAD0_UART2_CTS_PAD1_UART2_RTS	RW	32	0x00000118	0x4A10 0118

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Table 18-341. SYSCTRL_PADCONF_CORE Register Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	SYSCTRL_PADCONF_CORE Physical Address
CONTROL_CORE_PAD0_UART2_RX_PAD1_UART2_TX	RW	32	0x0000011C	0x4A10 011C
CONTROL_CORE_PAD0_HDQ_SIO_PAD1_I2C1_SCL	RW	32	0x00000120	0x4A10 0120
CONTROL_CORE_PAD0_I2C1_SDA_PAD1_I2C2_SCL	RW	32	0x00000124	0x4A10 0124
CONTROL_CORE_PAD0_I2C2_SDA_PAD1_I2C3_SCL	RW	32	0x00000128	0x4A10 0128
CONTROL_CORE_PAD0_I2C3_SDA_PAD1_I2C4_SCL	RW	32	0x0000012C	0x4A10 012C
CONTROL_CORE_PAD0_I2C4_SDA_PAD1_MCSPI1_CLK	RW	32	0x00000130	0x4A10 0130
CONTROL_CORE_PAD0_MCSPI1_SOMI_PAD1_MCSPI1_SIMO	RW	32	0x00000134	0x4A10 0134
CONTROL_CORE_PAD0_MCSPI1_CS0_PAD1_MCSPI1_CS1	RW	32	0x00000138	0x4A10 0138
CONTROL_CORE_PAD0_MCSPI1_CS2_PAD1_MCSPI1_CS3	RW	32	0x0000013C	0x4A10 013C
CONTROL_CORE_PAD0_UART3_CTS_RCTX_PAD1_UART3_RTS_SD	RW	32	0x00000140	0x4A10 0140
CONTROL_CORE_PAD0_UART3_RX_IRRX_PAD1_UART3_TX_IRTX	RW	32	0x00000144	0x4A10 0144
CONTROL_CORE_PAD0_SDMMC5_CLK_PAD1_SDMMC5_CMD	RW	32	0x00000148	0x4A10 0148
CONTROL_CORE_PAD0_SDMMC5_DAT0_PAD1_SDMMC5_DAT1	RW	32	0x0000014C	0x4A10 014C
CONTROL_CORE_PAD0_SDMMC5_DAT2_PAD1_SDMMC5_DAT3	RW	32	0x00000150	0x4A10 0150
CONTROL_CORE_PAD0_MCSPI4_CLK_PAD1_MCSPI4_SIMO	RW	32	0x00000154	0x4A10 0154
CONTROL_CORE_PAD0_MCSPI4_SOMI_PAD1_MCSPI4_CS0	RW	32	0x00000158	0x4A10 0158
CONTROL_CORE_PAD0_UART4_RX_PAD1_UART4_TX	RW	32	0x0000015C	0x4A10 015C
CONTROL_CORE_PAD0_USBB2_ULPITLL_CLK_PAD1_USBB2_ULPITLL_STP	RW	32	0x00000160	0x4A10 0160
CONTROL_CORE_PAD0_USBB2_ULPITLL_DIR_PAD1_USBB2_ULPITLL_NXT	RW	32	0x00000164	0x4A10 0164
CONTROL_CORE_PAD0_USBB2_ULPITLL_DAT0_PAD1_USBB2_ULPITLL_DAT1	RW	32	0x00000168	0x4A10 0168
CONTROL_CORE_PAD0_USBB2_ULPITLL_DAT2_PAD1_USBB2_ULPITLL_DAT3	RW	32	0x0000016C	0x4A10 016C
CONTROL_CORE_PAD0_USBB2_ULPITLL_DAT4_PAD1_USBB2_ULPITLL_DAT5	RW	32	0x00000170	0x4A10 0170
CONTROL_CORE_PAD0_USBB2_ULPITLL_DAT6_PAD1_USBB2_ULPITLL_DAT7	RW	32	0x00000174	0x4A10 0174
CONTROL_CORE_PAD0_USBB2_HSIC_DATA_PAD1_USBB2_HSIC_STROBE	RW	32	0x00000178	0x4A10 0178
CONTROL_CORE_PAD0_KPD_COL3_PAD1_KPD_COL4	RW	32	0x0000017C	0x4A10 017C

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Table 18-341. SYSCTRL_PADCONF_CORE Register Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	SYSCTRL_PADCONF_CORE Physical Address
CONTROL_CORE_PAD0_KPD_COL5_PAD1_KPD_COL0	RW	32	0x00000180	0x4A10 0180
CONTROL_CORE_PAD0_KPD_COL1_PAD1_KPD_COL2	RW	32	0x00000184	0x4A10 0184
CONTROL_CORE_PAD0_KPD_ROW3_PAD1_KPD_ROW4	RW	32	0x00000188	0x4A10 0188
CONTROL_CORE_PAD0_KPD_ROW5_PAD1_KPD_ROW0	RW	32	0x0000018C	0x4A10 018C
CONTROL_CORE_PAD0_KPD_ROW1_PAD1_KPD_ROW2	RW	32	0x00000190	0x4A10 0190
CONTROL_CORE_PAD0_USBA0_OTG_CE_PAD1_USBA0_OTG_DP	RW	32	0x00000194	0x4A10 0194
CONTROL_CORE_PAD0_USBA0_OTG_DM_PAD1_FREF_CLK1_OUT	RW	32	0x00000198	0x4A10 0198
CONTROL_CORE_PAD0_FREF_CLK2_OUT_PAD1_SYS_NIRQ1	RW	32	0x0000019C	0x4A10 019C
CONTROL_CORE_PAD0_SYS_NIRQ2_PAD1_SYS_BOOT0	RW	32	0x000001A0	0x4A10 01A0
CONTROL_CORE_PAD0_SYS_BOOT1_PAD1_SYS_BOOT2	RW	32	0x000001A4	0x4A10 01A4
CONTROL_CORE_PAD0_SYS_BOOT3_PAD1_SYS_BOOT4	RW	32	0x000001A8	0x4A10 01A8
CONTROL_CORE_PAD0_SYS_BOOT5_PAD1_DPM_EMU0	RW	32	0x000001AC	0x4A10 01AC
CONTROL_CORE_PAD0_DPM_EMU1_PAD1_DPM_EMU2	RW	32	0x000001B0	0x4A10 01B0
CONTROL_CORE_PAD0_DPM_EMU3_PAD1_DPM_EMU4	RW	32	0x000001B4	0x4A10 01B4
CONTROL_CORE_PAD0_DPM_EMU5_PAD1_DPM_EMU6	RW	32	0x000001B8	0x4A10 01B8
CONTROL_CORE_PAD0_DPM_EMU7_PAD1_DPM_EMU8	RW	32	0x000001BC	0x4A10 01BC
CONTROL_CORE_PAD0_DPM_EMU9_PAD1_DPM_EMU10	RW	32	0x000001C0	0x4A10 01C0
CONTROL_CORE_PAD0_DPM_EMU11_PAD1_DPM_EMU12	RW	32	0x000001C4	0x4A10 01C4
CONTROL_CORE_PAD0_DPM_EMU13_PAD1_DPM_EMU14	RW	32	0x000001C8	0x4A10 01C8
CONTROL_CORE_PAD0_DPM_EMU15_PAD1_DPM_EMU16	RW	32	0x000001CC	0x4A10 01CC
CONTROL_CORE_PAD0_DPM_EMU17_PAD1_DPM_EMU18	RW	32	0x000001D0	0x4A10 01D0
CONTROL_CORE_PAD0_DPM_EMU19_PAD1_CSI22_DX2	RW	32	0x000001D4	0x4A10 01D4
CONTROL_PADCONF_WAKEUPEVENT_0	R	32	0x000001D8	0x4A10 01D8
CONTROL_PADCONF_WAKEUPEVENT_1	R	32	0x000001DC	0x4A10 01DC
CONTROL_PADCONF_WAKEUPEVENT_2	R	32	0x000001E0	0x4A10 01E0
CONTROL_PADCONF_WAKEUPEVENT_3	R	32	0x000001E4	0x4A10 01E4
CONTROL_PADCONF_WAKEUPEVENT_4	R	32	0x000001E8	0x4A10 01E8

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Table 18-341. SYSCTRL_PADCONF_CORE Register Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	SYSCTRL_PADCONF_CORE Physical Address
CONTROL_PADCONF_WAKEUPEVENT_5	R	32	0x000001EC	0x4A10 01EC
CONTROL_PADCONF_WAKEUPEVENT_6	R	32	0x000001F0	0x4A10 01F0
CONTROL_CORE_PAD0_CSI22_DY2	RW	32	0x0000 01F4	0x4A10 01F4
CONTROL_PADCONF_GLOBAL	RW	32	0x000005A0	0x4A10 05A0
CONTROL_CORE_PADCONF_MODE	RW	32	0x000005A4	0x4A10 05A4
CONTROL_SMART1IO_PADCONF_0	RW	32	0x000005A8	0x4A10 05A8
CONTROL_SMART1IO_PADCONF_1	RW	32	0x000005AC	0x4A10 05AC
CONTROL_SMART2IO_PADCONF_0	RW	32	0x000005B0	0x4A10 05B0
CONTROL_SMART2IO_PADCONF_1	RW	32	0x000005B4	0x4A10 05B4
CONTROL_SMART3IO_PADCONF_0	RW	32	0x000005B8	0x4A10 05B8
CONTROL_SMART3IO_PADCONF_1	RW	32	0x000005BC	0x4A10 05BC
CONTROL_SMART3IO_PADCONF_2	RW	32	0x000005C0	0x4A10 05C0
CONTROL_USBB_HSIC	RW	32	0x000005C4	0x4A10 05C4
CONTROL_SMART3IO_PADCONF_3	RW	32	0x000005C8	0x4A10 05C8
CONTROL_SMART2IO_PADCONF_2	RW	32	0x000005CC	0x4A10 05CC
CONTROL_SMART1IO_PADCONF_2	RW	32	0x000005D0	0x4A10 05D0
CONTROL_SMART1IO_PADCONF_3	RW	32	0x000005D4	0x4A10 05D4
CONTROL_C2CIO_PADCONF_0	RW	32	0x000005D8	0x4A10 05D8
CONTROL_PBIASLITE	RW	32	0x00000600	0x4A10 0600
CONTROL_I2C_0	RW	32	0x00000604	0x4A10 0604
CONTROL_CAMERA_RX	RW	32	0x00000608	0x4A10 0608
CONTROL_AVDAC (1)	RW	32	0x0000060C	0x4A10 060C
RESERVED	RW	32	0x00000610	0x4A10 0610
CONTROL_MMC2	RW	32	0x00000614	0x4A10 0614
CONTROL_DSIPHY	RW	32	0x00000618	0x4A10 0618
CONTROL_MCBSPLP	RW	32	0x0000061C	0x4A10 061C
CONTROL_USB2PHYCORE	RW	32	0x00000620	0x4A10 0620
RESERVED	RW	32	0x00000624	0x4A10 0624
CONTROL_MMC1	RW	32	0x00000628	0x4A10 0628
CONTROL_HSI	RW	32	0x0000062C	0x4A10 062C
CONTROL_USB	RW	32	0x00000630	0x4A10 0630
CONTROL_HDQ	RW	32	0x00000634	0x4A10 0634
CONTROL_LPDDR2IO1_0	RW	32	0x00000638	0x4A10 0638
CONTROL_LPDDR2IO1_1	RW	32	0x0000063C	0x4A10 063C
CONTROL_LPDDR2IO1_2	RW	32	0x00000640	0x4A10 0640
CONTROL_LPDDR2IO1_3	RW	32	0x00000644	0x4A10 0644
CONTROL_LPDDR2IO2_0	RW	32	0x00000648	0x4A10 0648
CONTROL_LPDDR2IO2_1	RW	32	0x0000064C	0x4A10 064C
CONTROL_LPDDR2IO2_2	RW	32	0x00000650	0x4A10 0650
CONTROL_LPDDR2IO2_3	RW	32	0x00000654	0x4A10 0654
CONTROL_BUS_HOLD	RW	32	0x00000658	0x4A10 0658
CONTROL_C2C	RW	32	0x0000065C	0x4A10 065C
CONTROL_CORE_CONTROL_SPARE_RW	RW	32	0x00000660	0x4A10 0660

(1) The video DAC (VDAC) function is not supported.

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Table 18-341. SYSCTRL_PADCONF_CORE Register Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	SYSCTRL_PADCONF_CORE Physical Address
CONTROL_CORE_CONTROL_SPARE_R	R	32	0x00000664	0x4A10 0664
CONTROL_CORE_CONTROL_SPARE_R_C0	RW	32	0x00000668	0x4A10 0668
CONTROL_CORE_CONTROL_SPARE_RW1	RW	32	0x0000066C	0x4A10 066C
CONTROL_CORE_CONTROL_SPARE_RW2	RW	32	0x00000670	0x4A10 0670
CONTROL_CORE_CONTROL_SPARE_RW3	RW	32	0x00000674	0x4A10 0674
CONTROL_CORE_CONTROL_SPARE_RW4	RW	32	0x00000678	0x4A10 0678
CONTROL_CORE_CONTROL_SPARE_RW5	RW	32	0x0000067C	0x4A10 067C
CONTROL_CORE_CONTROL_SPARE_RW6	RW	32	0x00000680	0x4A10 0680
CONTROL_CORE_CONTROL_SPARE_RW7	RW	32	0x00000684	0x4A10 0684
CONTROL_CORE_CONTROL_SPARE_RW8	RW	32	0x00000688	0x4A10 0688
CONTROL_CORE_CONTROL_SPARE_RW9	RW	32	0x0000068C	0x4A10 068C
CONTROL_CORE_CONTROL_SPARE_R1	R	32	0x00000690	0x4A10 0690
CONTROL_EMIF	RW	32	0x0000 0694	0x4A10 0694
CONTROL_EFUSE_1 (2)	RW	32	0x00000700	0x4A10 0700
CONTROL_EFUSE_2	RW	32	0x00000704	0x4A10 0704
CONTROL_EFUSE_3	R	32	0x00000708	0x4A10 0708
CONTROL_EFUSE_4	RW	32	0x0000070C	0x4A10 070C

(2) The video DAC (VDAC) function is not supported.

18.6.7 SYSCTRL_PADCONF_CORE Register Description

Table 18-342. CONTROL_PADCONF_CORE_REVISION

Address Offset	0x0000 0000		
Physical Address	0x4A10 0000	**Instance**	SYSCTRL_PADCONF_CORE
Description	Control module revision identifier Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP Revision	R	See (1)

(1) TI internal data

Table 18-343. Register Call Summary for Register CONTROL_PADCONF_CORE_REVISION

Control Module Register Manual

- SYSCTRL_PADCONF_CORE Register Summary: [0]

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Table 18-344. CONTROL_PADCONF_CORE_HWINFO

Address Offset	0x0000 0004		
Physical Address	0x4A10 0004	**Instance**	SYSCTRL_PADCONF_CORE
Description	Information about the IP module hardware configuration that is, typically the module HDL generics (if any). Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IP_HWINFO																															

Bits	Field Name	Description	Type	Reset
31:0	IP_HWINFO	IP-module dependent	R	0x0000 0000

Table 18-345. Register Call Summary for Register CONTROL_PADCONF_CORE_HWINFO

Control Module Register Manual
- SYSCTRL_PADCONF_CORE Register Summary: [0]

Table 18-346. CONTROL_PADCONF_CORE_SYSCONFIG

Address Offset	0x0000 0010		
Physical Address	0x4A10 0010	**Instance**	SYSCTRL_PADCONF_CORE
Description	Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												IP_SYSCONFIG_IDLEMODE		RESERVED	

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0000000
3:2	IP_SYSCONFIG_IDLEMODE	Select the local clock-gating strategy 0x0: Clock is manually gated 0x1: Clock is manually enabled 0x2,0x3: Clock is automatically gated when there is no access to the Control Module through L4-interconnect	RW	0x2
1:0	RESERVED		R	0x0

Table 18-347. Register Call Summary for Register CONTROL_PADCONF_CORE_SYSCONFIG

Control Module Functional Description
- Device Core Control Module Instance: [0]

Control Module Programming Guide
- Global Initialization: [1]
- Operational Modes Configuration: [2]

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Table 18-347. Register Call Summary for Register CONTROL_PADCONF_CORE_SYSCONFIG (continued)

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- SYSCTRL_PADCONF_CORE Register Summary: [3]

Table 18-348. CONTROL_CORE_PAD0_GPMC_AD0_PAD1_GPMC_AD1

Address Offset	0x0000 0040		
Physical Address	0x4A10 0040	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads gpmc_ad0 and gpmc_ad1 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPMC_AD1_WAKEUPEVENT	GPMC_AD1_WAKEUPENABLE	GPMC_AD1_OFFMODEPULLTYPESELECT	GPMC_AD1_OFFMODEPULLUDENABLE	GPMC_AD1_OFFMODEOUTVALUE	GPMC_AD1_OFFMODEOUTENABLE	GPMC_AD1_OFFMODEENABLE	GPMC_AD1_INPUTENABLE	RESERVED			GPMC_AD1_PULLTYPESELECT	GPMC_AD1_PULLUDENABLE	GPMC_AD1_MUXMODE			GPMC_AD0_WAKEUPEVENT	GPMC_AD0_WAKEUPENABLE	GPMC_AD0_OFFMODEPULLTYPESELECT	GPMC_AD0_OFFMODEPULLUDENABLE	GPMC_AD0_OFFMODEOUTVALUE	GPMC_AD0_OFFMODEOUTENABLE	GPMC_AD0_OFFMODEENABLE	GPMC_AD0_INPUTENABLE	RESERVED			GPMC_AD0_PULLTYPESELECT	GPMC_AD0_PULLUDENABLE	GPMC_AD0_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	GPMC_AD1_WAKEUPEVENT	Pad_x wake-up event status latched in the I/O Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	GPMC_AD1_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29	GPMC_AD1_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad gpmc_ad1 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
28	GPMC_AD1_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad gpmc_ad1 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	GPMC_AD1_OFFMODEOUTVALUE	OffMode mode output value for pad gpmc_ad1 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	GPMC_AD1_OFFMODEOUTENABLE	OffMode mode output enable value for pad gpmc_ad1. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0

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Bits	Field Name	Description	Type	Reset
25	GPMC_AD1_OFFMODEENABLE	OffMode mode override control for pad gpmc_ad1 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
24	GPMC_AD1_INPUTENABLE	Input enable value for pad gpmc_ad1 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	GPMC_AD1_PULLTYPESELECT	pullup/down selection for pad gpmc_ad1 0x0: pulldown selected 0x1: pullup selected	RW	1
19	GPMC_AD1_PULLUDENABLE	pullup/down enable for pad gpmc_ad1 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	GPMC_AD1_MUXMODE	Functional multiplexing selection for pad gpmc_ad1 0x0: Select gpmc_ad1 0x1: Select sdmmc2_dat1	RW	0x0
15	GPMC_AD0_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	GPMC_AD0_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	GPMC_AD0_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad gpmc_ad0 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
12	GPMC_AD0_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad gpmc_ad0 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	GPMC_AD0_OFFMODEOUTVALUE	OffMode mode output value for pad gpmc_ad0 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	GPMC_AD0_OFFMODEOUTENABLE	OffMode mode output enable value for pad gpmc_ad0. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	GPMC_AD0_OFFMODEENABLE	OffMode mode override control for pad gpmc_ad0 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	GPMC_AD0_INPUTENABLE	Input enable value for pad gpmc_ad0 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	GPMC_AD0_PULLTYPESELECT	pullup/down selection for pad gpmc_ad0 0x0: pulldown selected 0x1: pullup selected	RW	1

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Bits	Field Name	Description	Type	Reset
3	GPMC_AD0_PULLUDENABLE	pullup/down enable for pad gpmc_ad0 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	GPMC_AD0_MUXMODE	Functional multiplexing selection for pad gpmc_ad0 0x0: Select gpmc_ad0 0x1: Select sdmmc2_dat0	RW	0x0

Table 18-349. Register Call Summary for Register CONTROL_CORE_PAD0_GPMC_AD0_PAD1_GPMC_AD1

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- SYSCTRL_PADCONF_CORE Register Summary: [2]

Table 18-350. CONTROL_CORE_PAD0_GPMC_AD2_PAD1_GPMC_AD3

Address Offset	0x0000 0044		
Physical Address	0x4A10 0044	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads gpmc_ad2 and gpmc_ad3 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPMC_AD3_WAKEUPEVENT	GPMC_AD3_WAKEUPENABLE	GPMC_AD3_OFFMODEPULLTYPESELECT	GPMC_AD3_OFFMODEPULLUDENABLE	GPMC_AD3_OFFMODEOUTVALUE	GPMC_AD3_OFFMODEOUTENABLE	GPMC_AD3_OFFMODEENABLE	GPMC_AD3_INPUTENABLE	RESERVED			GPMC_AD3_PULLTYPESELECT	GPMC_AD3_PULLUDENABLE	GPMC_AD3_MUXMODE			GPMC_AD2_WAKEUPEVENT	GPMC_AD2_WAKEUPENABLE	GPMC_AD2_OFFMODEPULLTYPESELECT	GPMC_AD2_OFFMODEPULLUDENABLE	GPMC_AD2_OFFMODEOUTVALUE	GPMC_AD2_OFFMODEOUTENABLE	GPMC_AD2_OFFMODEENABLE	GPMC_AD2_INPUTENABLE	RESERVED			GPMC_AD2_PULLTYPESELECT	GPMC_AD2_PULLUDENABLE	GPMC_AD2_MUXMODE	

Bits	Field Name	Description	Type	Reset
31	GPMC_AD3_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	GPMC_AD3_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29	GPMC_AD3_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad gpmc_ad3 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0

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Bits	Field Name	Description	Type	Reset
28	GPMC_AD3_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad gpmc_ad3 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	GPMC_AD3_OFFMODEOUTVALUE	OffMode mode output value for pad gpmc_ad3 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	GPMC_AD3_OFFMODEOUTENABLE	OffMode mode output enable value for pad gpmc_ad3. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	GPMC_AD3_OFFMODEENABLE	OffMode mode override control for pad gpmc_ad3 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
24	GPMC_AD3_INPUTENABLE	Input enable value for pad gpmc_ad3 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	GPMC_AD3_PULLTYPESELECT	pullup/down selection for pad gpmc_ad3 0x0: pulldown selected 0x1: pullup selected	RW	1
19	GPMC_AD3_PULLUDENABLE	pullup/down enable for pad gpmc_ad3 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	GPMC_AD3_MUXMODE	Functional multiplexing selection for pad gpmc_ad3 0x0: Select gpmc_ad3 0x1: Select sdmmc2_dat3	RW	0x0
15	GPMC_AD2_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	GPMC_AD2_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	GPMC_AD2_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad gpmc_ad2 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
12	GPMC_AD2_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad gpmc_ad2 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	GPMC_AD2_OFFMODEOUTVALUE	OffMode mode output value for pad gpmc_ad2 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	GPMC_AD2_OFFMODEOUTENABLE	OffMode mode output enable value for pad gpmc_ad2. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0

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Bits	Field Name	Description	Type	Reset
9	GPMC_AD2_OFFMODEENABLE	OffMode mode override control for pad gpmc_ad2 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	GPMC_AD2_INPUTENABLE	Input enable value for pad gpmc_ad2 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	GPMC_AD2_PULLTYPESELECT	pullup/down selection for pad gpmc_ad2 0x0: pulldown selected 0x1: pullup selected	RW	1
3	GPMC_AD2_PULLUDENABLE	pullup/down enable for pad gpmc_ad2 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	GPMC_AD2_MUXMODE	Functional multiplexing selection for pad gpmc_ad2 0x0: Select gpmc_ad2 0x1: Select sdmmc2_dat2	RW	0x0

Table 18-351. Register Call Summary for Register CONTROL_CORE_PAD0_GPMC_AD2_PAD1_GPMC_AD3

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- SYSCTRL_PADCONF_CORE Register Summary: [2]

Table 18-352. CONTROL_CORE_PAD0_GPMC_AD4_PAD1_GPMC_AD5

Address Offset	0x0000 0048		
Physical Address	0x4A10 0048	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads gpmc_ad4 and gpmc_ad5 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPMC_AD5_WAKEUPEVENT	GPMC_AD5_WAKEUPENABLE	GPMC_AD5_OFFMODEPULLTYPESELECT	GPMC_AD5_OFFMODEPULLUDENABLE	GPMC_AD5_OFFMODEOUTVALUE	GPMC_AD5_OFFMODEOUTENABLE	GPMC_AD5_OFFMODEENABLE	GPMC_AD5_INPUTENABLE	RESERVED			GPMC_AD5_PULLTYPESELECT	GPMC_AD5_PULLUDENABLE	GPMC_AD5_MUXMODE			GPMC_AD4_WAKEUPEVENT	GPMC_AD4_WAKEUPENABLE	GPMC_AD4_OFFMODEPULLTYPESELECT	GPMC_AD4_OFFMODEPULLUDENABLE	GPMC_AD4_OFFMODEOUTVALUE	GPMC_AD4_OFFMODEOUTENABLE	GPMC_AD4_OFFMODEENABLE	GPMC_AD4_INPUTENABLE	RESERVED			GPMC_AD4_PULLTYPESELECT	GPMC_AD4_PULLUDENABLE	GPMC_AD4_MUXMODE		

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Bits	Field Name	Description	Type	Reset
31	GPMC_AD5_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	GPMC_AD5_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29	GPMC_AD5_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad gpmc_ad5 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
28	GPMC_AD5_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad gpmc_ad5 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	GPMC_AD5_OFFMODEOUTVALUE	OffMode mode output value for pad gpmc_ad5 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	GPMC_AD5_OFFMODEOUTENABLE	OffMode mode output enable value for pad gpmc_ad5. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	GPMC_AD5_OFFMODEENABLE	OffMode mode override control for pad gpmc_ad5 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
24	GPMC_AD5_INPUTENABLE	Input enable value for pad gpmc_ad5 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	GPMC_AD5_PULLTYPESELECT	pullup/down selection for pad gpmc_ad5 0x0: pulldown selected 0x1: pullup selected	RW	1
19	GPMC_AD5_PULLUDENABLE	pullup/down enable for pad gpmc_ad5 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	GPMC_AD5_MUXMODE	Functional multiplexing selection for pad gpmc_ad5 0x0: Select gpmc_ad5 0x1: Select sdmmc2_dat5 0x2: Select sdmmc2_dir_dat1	RW	0x0
15	GPMC_AD4_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	GPMC_AD4_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	GPMC_AD4_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad gpmc_ad4 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0

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Bits	Field Name	Description	Type	Reset
12	GPMC_AD4_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad gpmc_ad4 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	GPMC_AD4_OFFMODEOUTVALUE	OffMode mode output value for pad gpmc_ad4 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	GPMC_AD4_OFFMODEOUTENABLE	OffMode mode output enable value for pad gpmc_ad4. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	GPMC_AD4_OFFMODEENABLE	OffMode mode override control for pad gpmc_ad4 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	GPMC_AD4_INPUTENABLE	Input enable value for pad gpmc_ad4 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	GPMC_AD4_PULLTYPESELECT	pullup/down selection for pad gpmc_ad4 0x0: pulldown selected 0x1: pullup selected	RW	1
3	GPMC_AD4_PULLUDENABLE	pullup/down enable for pad gpmc_ad4 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	GPMC_AD4_MUXMODE	Functional multiplexing selection for pad gpmc_ad4 0x0: Select gpmc_ad4 0x1: Select sdmmc2_dat4 0x2: Select sdmmc2_dir_dat0	RW	0x0

Table 18-353. Register Call Summary for Register CONTROL_CORE_PAD0_GPMC_AD4_PAD1_GPMC_AD5

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- SYSCTRL_PADCONF_CORE Register Summary: [2]

Table 18-354. CONTROL_CORE_PAD0_GPMC_AD6_PAD1_GPMC_AD7

Address Offset	0x0000 004C		
Physical Address	0x4A10 004C	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads gpmc_ad6 and gpmc_ad7 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPMC_AD7_WAKEUPEVENT	GPMC_AD7_WAKEUPENABLE	GPMC_AD7_OFFMODEPULLTYPESELECT	GPMC_AD7_OFFMODEPULLUDENABLE	GPMC_AD7_OFFMODEOUTVALUE	GPMC_AD7_OFFMODEOUTENABLE	GPMC_AD7_OFFMODEENABLE	GPMC_AD7_INPUTENABLE	RESERVED			GPMC_AD7_PULLTYPESELECT	GPMC_AD7_PULLUDENABLE	GPMC_AD7_MUXMODE			GPMC_AD6_WAKEUPEVENT	GPMC_AD6_WAKEUPENABLE	GPMC_AD6_OFFMODEPULLTYPESELECT	GPMC_AD6_OFFMODEPULLUDENABLE	GPMC_AD6_OFFMODEOUTVALUE	GPMC_AD6_OFFMODEOUTENABLE	GPMC_AD6_OFFMODEENABLE	GPMC_AD6_INPUTENABLE	RESERVED			GPMC_AD6_PULLTYPESELECT	GPMC_AD6_PULLUDENABLE	GPMC_AD6_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	GPMC_AD7_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	GPMC_AD7_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29	GPMC_AD7_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad gpmc_ad7 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
28	GPMC_AD7_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad gpmc_ad7 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	GPMC_AD7_OFFMODEOUTVALUE	OffMode mode output value for pad gpmc_ad7 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	GPMC_AD7_OFFMODEOUTENABLE	OffMode mode output enable value for pad gpmc_ad7. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	GPMC_AD7_OFFMODEENABLE	OffMode mode override control for pad gpmc_ad7 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
24	GPMC_AD7_INPUTENABLE	Input enable value for pad gpmc_ad7 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	GPMC_AD7_PULLTYPESELECT	pullup/down selection for pad gpmc_ad7 0x0: pulldown selected 0x1: pullup selected	RW	1
19	GPMC_AD7_PULLUDENABLE	pullup/down enable for pad gpmc_ad7 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1

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Bits	Field Name	Description	Type	Reset
18:16	GPMC_AD7_MUXMODE	Functional multiplexing selection for pad gpmc_ad7 0x0: Select gpmc_ad7 0x1: Select sdmmc2_dat7 0x2: Select sdmmc2_clk_fdbk	RW	0x0
15	GPMC_AD6_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	GPMC_AD6_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	GPMC_AD6_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad gpmc_ad6 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
12	GPMC_AD6_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad gpmc_ad6 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	GPMC_AD6_OFFMODEOUTVALUE	OffMode mode output value for pad gpmc_ad6 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	GPMC_AD6_OFFMODEOUTENABLE	OffMode mode output enable value for pad gpmc_ad6. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	GPMC_AD6_OFFMODEENABLE	OffMode mode override control for pad gpmc_ad6 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	GPMC_AD6_INPUTENABLE	Input enable value for pad gpmc_ad6 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	GPMC_AD6_PULLTYPESELECT	pullup/down selection for pad gpmc_ad6 0x0: pulldown selected 0x1: pullup selected	RW	1
3	GPMC_AD6_PULLUDENABLE	pullup/down enable for pad gpmc_ad6 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	GPMC_AD6_MUXMODE	Functional multiplexing selection for pad gpmc_ad6 0x0: Select gpmc_ad6 0x1: Select sdmmc2_dat6 0x2: Select sdmmc2_dir_cmd	RW	0x0

Table 18-355. Register Call Summary for Register CONTROL_CORE_PAD0_GPMC_AD6_PAD1_GPMC_AD7

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- SYSCTRL_PADCONF_CORE Register Summary: [2]

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Table 18-356. CONTROL_CORE_PAD0_GPMC_AD8_PAD1_GPMC_AD9

Address Offset	0x0000 0050		
Physical Address	0x4A10 0050	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads gpmc_ad8 and gpmc_ad9 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPMC_AD9_WAKEUPEVENT	GPMC_AD9_WAKEUPENABLE	GPMC_AD9_OFFMODEPULLTYPESELECT	GPMC_AD9_OFFMODEPULLUDENABLE	GPMC_AD9_OFFMODEOUTVALUE	GPMC_AD9_OFFMODEOUTENABLE	GPMC_AD9_OFFMODEENABLE	GPMC_AD9_INPUTENABLE	RESERVED			GPMC_AD9_PULLTYPESELECT	GPMC_AD9_PULLUDENABLE	GPMC_AD9_MUXMODE			GPMC_AD8_WAKEUPEVENT	GPMC_AD8_WAKEUPENABLE	GPMC_AD8_OFFMODEPULLTYPESELECT	GPMC_AD8_OFFMODEPULLUDENABLE	GPMC_AD8_OFFMODEOUTVALUE	GPMC_AD8_OFFMODEOUTENABLE	GPMC_AD8_OFFMODEENABLE	GPMC_AD8_INPUTENABLE	RESERVED			GPMC_AD8_PULLTYPESELECT	GPMC_AD8_PULLUDENABLE	GPMC_AD8_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	GPMC_AD9_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	GPMC_AD9_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29	GPMC_AD9_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad gpmc_ad9 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
28	GPMC_AD9_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad gpmc_ad9 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	GPMC_AD9_OFFMODEOUTVALUE	OffMode mode output value for pad gpmc_ad9 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	GPMC_AD9_OFFMODEOUTENABLE	OffMode mode output enable value for pad gpmc_ad9. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	GPMC_AD9_OFFMODEENABLE	OffMode mode override control for pad gpmc_ad9 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
24	GPMC_AD9_INPUTENABLE	Input enable value for pad gpmc_ad9 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1

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Bits	Field Name	Description	Type	Reset
23:21	RESERVED		R	0x0
20	GPMC_AD9_PULLTYPESELECT	pullup/down selection for pad gpmc_ad9 0x0: pulldown selected 0x1: pullup selected	RW	1
19	GPMC_AD9_PULLUDENABLE	pullup/down enable for pad gpmc_ad9 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	GPMC_AD9_MUXMODE	Functional multiplexing selection for pad gpmc_ad9 0x0: Select gpmc_ad9 0x1: Select kpd_row1 0x2: Select c2c_data14 0x3: Select gpio_33 0x5: Select sdmmc1_dat1	RW	0x0
15	GPMC_AD8_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	GPMC_AD8_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	GPMC_AD8_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad gpmc_ad8 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
12	GPMC_AD8_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad gpmc_ad8 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	GPMC_AD8_OFFMODEOUTVALUE	OffMode mode output value for pad gpmc_ad8 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	GPMC_AD8_OFFMODEOUTENABLE	OffMode mode output enable value for pad gpmc_ad8. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	GPMC_AD8_OFFMODEENABLE	OffMode mode override control for pad gpmc_ad8 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	GPMC_AD8_INPUTENABLE	Input enable value for pad gpmc_ad8 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	GPMC_AD8_PULLTYPESELECT	pullup/down selection for pad gpmc_ad8 0x0: pulldown selected 0x1: pullup selected	RW	1
3	GPMC_AD8_PULLUDENABLE	pullup/down enable for pad gpmc_ad8 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1

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Bits	Field Name	Description	Type	Reset
2:0	GPMC_AD8_MUXMODE	Functional multiplexing selection for pad gpmc_ad8 0x0: Select gpmc_ad8 0x1: Select kpd_row0 0x2: Select c2c_data15 0x3: Select gpio_32 0x5: Select sdmmc1_dat0	RW	0x0

Table 18-357. Register Call Summary for Register CONTROL_CORE_PAD0_GPMC_AD8_PAD1_GPMC_AD9

Control Module Functional Description • Pad Multiplexing Register Fields: [0] [1]
Control Module Register Manual • SYSCTRL_PADCONF_CORE Register Summary: [2]

Table 18-358. CONTROL_CORE_PAD0_GPMC_AD10_PAD1_GPMC_AD11

Address Offset	0x0000 0054		
Physical Address	0x4A10 0054	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads gpmc_ad10 and gpmc_ad11 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPMC_AD11_WAKEUPEVENT	GPMC_AD11_WAKEUPENABLE	GPMC_AD11_OFFMODEPULLTYPESELECT	GPMC_AD11_OFFMODEPULLUDENABLE	GPMC_AD11_OFFMODEOUTVALUE	GPMC_AD11_OFFMODEOUTENABLE	GPMC_AD11_OFFMODEENABLE	GPMC_AD11_INPUTENABLE	RESERVED			GPMC_AD11_PULLTYPESELECT	GPMC_AD11_PULLUDENABLE	GPMC_AD11_MUXMODE			GPMC_AD10_WAKEUPEVENT	GPMC_AD10_WAKEUPENABLE	GPMC_AD10_OFFMODEPULLTYPESELECT	GPMC_AD10_OFFMODEPULLUDENABLE	GPMC_AD10_OFFMODEOUTVALUE	GPMC_AD10_OFFMODEOUTENABLE	GPMC_AD10_OFFMODEENABLE	GPMC_AD10_INPUTENABLE	RESERVED			GPMC_AD10_PULLTYPESELECT	GPMC_AD10_PULLUDENABLE	GPMC_AD10_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	GPMC_AD11_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	GPMC_AD11_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29	GPMC_AD11_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad gpmc_ad11 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0

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Bits	Field Name	Description	Type	Reset
28	GPMC_AD11_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad gpmc_ad11 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	GPMC_AD11_OFFMODEOUTV ALUE	OffMode mode output value for pad gpmc_ad11 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	GPMC_AD11_OFFMODEOUTE NABLE	OffMode mode output enable value for pad gpmc_ad11. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	GPMC_AD11_OFFMODEENABL E	OffMode mode override control for pad gpmc_ad11 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
24	GPMC_AD11_INPUTENABLE	Input enable value for pad gpmc_ad11 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	GPMC_AD11_PULLTYPESELE CT	pullup/down selection for pad gpmc_ad11 0x0: pulldown selected 0x1: pullup selected	RW	1
19	GPMC_AD11_PULLUDENABLE	pullup/down enable for pad gpmc_ad11 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	GPMC_AD11_MUXMODE	Functional multiplexing selection for pad gpmc_ad11 0x0: Select gpmc_ad11 0x1: Select kpd_row3 0x2: Select c2c_data12 0x3: Select gpio_35 0x5: Select sdmmc1_dat3	RW	0x0
15	GPMC_AD10_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	GPMC_AD10_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	GPMC_AD10_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad gpmc_ad10 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
12	GPMC_AD10_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad gpmc_ad10 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	GPMC_AD10_OFFMODEOUTV ALUE	OffMode mode output value for pad gpmc_ad10 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	GPMC_AD10_OFFMODEOUTE NABLE	OffMode mode output enable value for pad gpmc_ad10. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0

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Bits	Field Name	Description	Type	Reset
9	GPMC_AD10_OFFMODEENABLE	OffMode mode override control for pad gpmc_ad10 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	GPMC_AD10_INPUTENABLE	Input enable value for pad gpmc_ad10 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	GPMC_AD10_PULLTYPESELECT	pullup/down selection for pad gpmc_ad10 0x0: pulldown selected 0x1: pullup selected	RW	1
3	GPMC_AD10_PULLUDENABLE	pullup/down enable for pad gpmc_ad10 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	GPMC_AD10_MUXMODE	Functional multiplexing selection for pad gpmc_ad10 0x0: Select gpmc_ad10 0x1: Select kpd_row2 0x2: Select c2c_data13 0x3: Select gpio_34 0x5: Select sdmmc1_dat2	RW	0x0

Table 18-359. Register Call Summary for Register CONTROL_CORE_PAD0_GPMC_AD10_PAD1_GPMC_AD11

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- SYSCTRL_PADCONF_CORE Register Summary: [2]

Table 18-360. CONTROL_CORE_PAD0_GPMC_AD12_PAD1_GPMC_AD13

Address Offset	0x0000 0058		
Physical Address	0x4A10 0058	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads gpmc_ad12 and gpmc_ad13 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPMC_AD13_WAKEUPEVENT	GPMC_AD13_WAKEUPENABLE	GPMC_AD13_OFFMODEPULLTYPESELECT	GPMC_AD13_OFFMODEPULLUDENABLE	GPMC_AD13_OFFMODEOUTVALUE	GPMC_AD13_OFFMODEOUTENABLE	GPMC_AD13_OFFMODEENABLE	GPMC_AD13_INPUTENABLE	RESERVED			GPMC_AD13_PULLTYPESELECT	GPMC_AD13_PULLUDENABLE	GPMC_AD13_MUXMODE			GPMC_AD12_WAKEUPEVENT	GPMC_AD12_WAKEUPENABLE	GPMC_AD12_OFFMODEPULLTYPESELECT	GPMC_AD12_OFFMODEPULLUDENABLE	GPMC_AD12_OFFMODEOUTVALUE	GPMC_AD12_OFFMODEOUTENABLE	GPMC_AD12_OFFMODEENABLE	GPMC_AD12_INPUTENABLE	RESERVED			GPMC_AD12_PULLTYPESELECT	GPMC_AD12_PULLUDENABLE	GPMC_AD12_MUXMODE	

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Bits	Field Name	Description	Type	Reset
31	GPMC_AD13_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	GPMC_AD13_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29	GPMC_AD13_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad gpmc_ad13 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
28	GPMC_AD13_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad gpmc_ad13 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	GPMC_AD13_OFFMODEOUTV ALUE	OffMode mode output value for pad gpmc_ad13 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	GPMC_AD13_OFFMODEOUTE NABLE	OffMode mode output enable value for pad gpmc_ad13. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	GPMC_AD13_OFFMODEENABL E	OffMode mode override control for pad gpmc_ad13 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
24	GPMC_AD13_INPUTENABLE	Input enable value for pad gpmc_ad13 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	GPMC_AD13_PULLTYPESELE CT	pullup/down selection for pad gpmc_ad13 0x0: pulldown selected 0x1: pullup selected	RW	0
19	GPMC_AD13_PULLUDENABLE	pullup/down enable for pad gpmc_ad13 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	GPMC_AD13_MUXMODE	Functional multiplexing selection for pad gpmc_ad13 0x0: Select gpmc_ad13 0x1: Select kpd_col1 0x2: Select c2c_data10 0x3: Select gpio_37 0x5: Select sdmmc1_dat5	RW	0x0
15	GPMC_AD12_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	GPMC_AD12_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	GPMC_AD12_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad gpmc_ad12 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0

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Bits	Field Name	Description	Type	Reset
12	GPMC_AD12_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad gpmc_ad12 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	GPMC_AD12_OFFMODEOUTV ALUE	OffMode mode output value for pad gpmc_ad12 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	GPMC_AD12_OFFMODEOUTE NABLE	OffMode mode output enable value for pad gpmc_ad12. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	GPMC_AD12_OFFMODEENABL E	OffMode mode override control for pad gpmc_ad12 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	GPMC_AD12_INPUTENABLE	Input enable value for pad gpmc_ad12 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	GPMC_AD12_PULLTYPESELE CT	pullup/down selection for pad gpmc_ad12 0x0: pulldown selected 0x1: pullup selected	RW	0
3	GPMC_AD12_PULLUDENABLE	pullup/down enable for pad gpmc_ad12 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	GPMC_AD12_MUXMODE	Functional multiplexing selection for pad gpmc_ad12 0x0: Select gpmc_ad12 0x1: Select kpd_col0 0x2: Select c2c_data11 0x3: Select gpio_36 0x5: Select sdmmc1_dat4	RW	0x0

Table 18-361. Register Call Summary for Register CONTROL_CORE_PAD0_GPMC_AD12_PAD1_GPMC_AD13

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- SYSCTRL_PADCONF_CORE Register Summary: [2]

Table 18-362. CONTROL_CORE_PAD0_GPMC_AD14_PAD1_GPMC_AD15

Address Offset	0x0000 005C		
Physical Address	0x4A10 005C	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads gpmc_ad14 and gpmc_ad15 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPMC_AD15_WAKEUPEVENT	GPMC_AD15_WAKEUPENABLE	GPMC_AD15_OFFMODEPULLTYPESELECT	GPMC_AD15_OFFMODEPULLUDENABLE	GPMC_AD15_OFFMODEOUTVALUE	GPMC_AD15_OFFMODEOUTENABLE	GPMC_AD15_OFFMODEENABLE	GPMC_AD15_INPUTENABLE	RESERVED			GPMC_AD15_PULLTYPESELECT	GPMC_AD15_PULLUDENABLE	GPMC_AD15_MUXMODE			GPMC_AD14_WAKEUPEVENT	GPMC_AD14_WAKEUPENABLE	GPMC_AD14_OFFMODEPULLTYPESELECT	GPMC_AD14_OFFMODEPULLUDENABLE	GPMC_AD14_OFFMODEOUTVALUE	GPMC_AD14_OFFMODEOUTENABLE	GPMC_AD14_OFFMODEENABLE	GPMC_AD14_INPUTENABLE	RESERVED			GPMC_AD14_PULLTYPESELECT	GPMC_AD14_PULLUDENABLE	GPMC_AD14_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	GPMC_AD15_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	GPMC_AD15_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29	GPMC_AD15_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad gpmc_ad15 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
28	GPMC_AD15_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad gpmc_ad15 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	GPMC_AD15_OFFMODEOUTV ALUE	OffMode mode output value for pad gpmc_ad15 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	GPMC_AD15_OFFMODEOUTE NABLE	OffMode mode output enable value for pad gpmc_ad15. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	GPMC_AD15_OFFMODEENABL E	OffMode mode override control for pad gpmc_ad15 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
24	GPMC_AD15_INPUTENABLE	Input enable value for pad gpmc_ad15 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	GPMC_AD15_PULLTYPESELE CT	pullup/down selection for pad gpmc_ad15 0x0: pulldown selected 0x1: pullup selected	RW	0
19	GPMC_AD15_PULLUDENABLE	pullup/down enable for pad gpmc_ad15 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1

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Bits	Field Name	Description	Type	Reset
18:16	GPMC_AD15_MUXMODE	Functional multiplexing selection for pad gpmc_ad15 0x0: Select gpmc_ad15 0x1: Select kpd_col3 0x2: Select c2c_data8 0x3: Select gpio_39 0x5: Select sdmmc1_dat7	RW	0x0
15	GPMC_AD14_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	GPMC_AD14_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	GPMC_AD14_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad gpmc_ad14 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
12	GPMC_AD14_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad gpmc_ad14 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	GPMC_AD14_OFFMODEOUTV ALUE	OffMode mode output value for pad gpmc_ad14 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	GPMC_AD14_OFFMODEOUTE NABLE	OffMode mode output enable value for pad gpmc_ad14. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	GPMC_AD14_OFFMODEENABL E	OffMode mode override control for pad gpmc_ad14 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	GPMC_AD14_INPUTENABLE	Input enable value for pad gpmc_ad14 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	GPMC_AD14_PULLTYPESELE CT	pullup/down selection for pad gpmc_ad14 0x0: pulldown selected 0x1: pullup selected	RW	0
3	GPMC_AD14_PULLUDENABLE	pullup/down enable for pad gpmc_ad14 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	GPMC_AD14_MUXMODE	Functional multiplexing selection for pad gpmc_ad14 0x0: Select gpmc_ad14 0x1: Select kpd_col2 0x2: Select c2c_data9 0x3: Select gpio_38 0x5: Select sdmmc1_dat6	RW	0x0

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Table 18-363. Register Call Summary for Register CONTROL_CORE_PAD0_GPMC_AD14_PAD1_GPMC_AD15

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- SYSCTRL_PADCONF_CORE Register Summary: [2]

Table 18-364. CONTROL_CORE_PAD0_GPMC_A16_PAD1_GPMC_A17

Address Offset	0x0000 0060		
Physical Address	0x4A10 0060	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads gpmc_a16 and gpmc_a17 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPMC_A17_WAKEUPEVENT	GPMC_A17_WAKEUPENABLE	GPMC_A17_OFFMODEPULLTYPESELECT	GPMC_A17_OFFMODEPULLUDENABLE	GPMC_A17_OFFMODEOUTVALUE	GPMC_A17_OFFMODEOUTENABLE	GPMC_A17_OFFMODEENABLE	GPMC_A17_INPUTENABLE	RESERVED			GPMC_A17_PULLTYPESELECT	GPMC_A17_PULLUDENABLE	GPMC_A17_MUXMODE			GPMC_A16_WAKEUPEVENT	GPMC_A16_WAKEUPENABLE	GPMC_A16_OFFMODEPULLTYPESELECT	GPMC_A16_OFFMODEPULLUDENABLE	GPMC_A16_OFFMODEOUTVALUE	GPMC_A16_OFFMODEOUTENABLE	GPMC_A16_OFFMODEENABLE	GPMC_A16_INPUTENABLE	RESERVED			GPMC_A16_PULLTYPESELECT	GPMC_A16_PULLUDENABLE	GPMC_A16_MUXMODE	

Bits	Field Name	Description	Type	Reset
31	GPMC_A17_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	GPMC_A17_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29	GPMC_A17_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad gpmc_a17 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
28	GPMC_A17_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad gpmc_a17 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	GPMC_A17_OFFMODEOUTVALUE	OffMode mode output value for pad gpmc_a17 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	GPMC_A17_OFFMODEOUTENABLE	OffMode mode output enable value for pad gpmc_a17. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0

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Bits	Field Name	Description	Type	Reset
25	GPMC_A17_OFFMODEENABLE	OffMode mode override control for pad gpmc_a17 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
24	GPMC_A17_INPUTENABLE	Input enable value for pad gpmc_a17 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	GPMC_A17_PULLTYPESELECT	pullup/down selection for pad gpmc_a17 0x0: pulldown selected 0x1: pullup selected	RW	0
19	GPMC_A17_PULLUDENABLE	pullup/down enable for pad gpmc_a17 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	GPMC_A17_MUXMODE	Functional multiplexing selection for pad gpmc_a17 0x0: Select gpmc_a17 0x1: Select kpd_row5 0x2: Select c2c_datain1 0x3: Select gpio_41 0x4: Select venc_656_data1 0x7: Select safe_mode	RW	0x7
15	GPMC_A16_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	GPMC_A16_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	GPMC_A16_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad gpmc_a16 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
12	GPMC_A16_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad gpmc_a16 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	GPMC_A16_OFFMODEOUTVALUE	OffMode mode output value for pad gpmc_a16 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	GPMC_A16_OFFMODEOUTENABLE	OffMode mode output enable value for pad gpmc_a16. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	GPMC_A16_OFFMODEENABLE	OffMode mode override control for pad gpmc_a16 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	GPMC_A16_INPUTENABLE	Input enable value for pad gpmc_a16 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
4	GPMC_A16_PULLTYPESELECT	pullup/down selection for pad gpmc_a16 0x0: pulldown selected 0x1: pullup selected	RW	0
3	GPMC_A16_PULLUDENABLE	pullup/down enable for pad gpmc_a16 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	GPMC_A16_MUXMODE	Functional multiplexing selection for pad gpmc_a16 0x0: Select gpmc_a16 0x1: Select kpd_row4 0x2: Select c2c_datain0 0x3: Select gpio_40 0x4: Select venc_656_data0 0x7: Select safe_mode	RW	0x7

Table 18-365. Register Call Summary for Register CONTROL_CORE_PAD0_GPMC_A16_PAD1_GPMC_A17

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- SYSCTRL_PADCONF_CORE Register Summary: [2]

Table 18-366. CONTROL_CORE_PAD0_GPMC_A18_PAD1_GPMC_A19

Address Offset	0x0000 0064		
Physical Address	0x4A10 0064	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads gpmc_a18 and gpmc_a19 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPMC_A19_WAKEUPEVENT	GPMC_A19_WAKEUPENABLE	GPMC_A19_OFFMODEPULLTYPESELECT	GPMC_A19_OFFMODEPULLUDENABLE	GPMC_A19_OFFMODEOUTVALUE	GPMC_A19_OFFMODEOUTENABLE	GPMC_A19_OFFMODEENABLE	GPMC_A19_INPUTENABLE	RESERVED			GPMC_A19_PULLTYPESELECT	GPMC_A19_PULLUDENABLE	GPMC_A19_MUXMODE			GPMC_A18_WAKEUPEVENT	GPMC_A18_WAKEUPENABLE	GPMC_A18_OFFMODEPULLTYPESELECT	GPMC_A18_OFFMODEPULLUDENABLE	GPMC_A18_OFFMODEOUTVALUE	GPMC_A18_OFFMODEOUTENABLE	GPMC_A18_OFFMODEENABLE	GPMC_A18_INPUTENABLE	RESERVED			GPMC_A18_PULLTYPESELECT	GPMC_A18_PULLUDENABLE	GPMC_A18_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	GPMC_A19_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0

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Bits	Field Name	Description	Type	Reset
30	GPMC_A19_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29	GPMC_A19_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad gpmc_a19 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
28	GPMC_A19_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad gpmc_a19 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	GPMC_A19_OFFMODEOUTVALUE	OffMode mode output value for pad gpmc_a19 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	GPMC_A19_OFFMODEOUTENABLE	OffMode mode output enable value for pad gpmc_a19. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	GPMC_A19_OFFMODEENABLE	OffMode mode override control for pad gpmc_a19 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
24	GPMC_A19_INPUTENABLE	Input enable value for pad gpmc_a19 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	GPMC_A19_PULLTYPESELECT	pullup/down selection for pad gpmc_a19 0x0: pulldown selected 0x1: pullup selected	RW	0
19	GPMC_A19_PULLUDENABLE	pullup/down enable for pad gpmc_a19 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	GPMC_A19_MUXMODE	Functional multiplexing selection for pad gpmc_a19 0x0: Select gpmc_a19 0x1: Select kpd_row7 0x2: Select c2c_datain3 0x3: Select gpio_43 0x4: Select venc_656_data3 0x7: Select safe_mode	RW	0x7
15	GPMC_A18_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	GPMC_A18_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	GPMC_A18_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad gpmc_a18 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0

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Bits	Field Name	Description	Type	Reset
12	GPMC_A18_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad gpmc_a18 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	GPMC_A18_OFFMODEOUTVALUE	OffMode mode output value for pad gpmc_a18 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	GPMC_A18_OFFMODEOUTENABLE	OffMode mode output enable value for pad gpmc_a18. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	GPMC_A18_OFFMODEENABLE	OffMode mode override control for pad gpmc_a18 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	GPMC_A18_INPUTENABLE	Input enable value for pad gpmc_a18 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	GPMC_A18_PULLTYPESELECT	pullup/down selection for pad gpmc_a18 0x0: pulldown selected 0x1: pullup selected	RW	0
3	GPMC_A18_PULLUDENABLE	pullup/down enable for pad gpmc_a18 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	GPMC_A18_MUXMODE	Functional multiplexing selection for pad gpmc_a18 0x0: Select gpmc_a18 0x1: Select kpd_row6 0x2: Select c2c_datain2 0x3: Select gpio_42 0x4: Select venc_656_data2 0x7: Select safe_mode	RW	0x7

Table 18-367. Register Call Summary for Register CONTROL_CORE_PAD0_GPMC_A18_PAD1_GPMC_A19

Control Module Functional Description • Pad Multiplexing Register Fields: [0] [1]
Control Module Register Manual • SYSCTRL_PADCONF_CORE Register Summary: [2]

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Table 18-368. CONTROL_CORE_PAD0_GPMC_A20_PAD1_GPMC_A21

Address Offset	0x0000 0068		
Physical Address	0x4A10 0068	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads gpmc_a20 and gpmc_a21 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPMC_A21_WAKEUPEVENT	GPMC_A21_WAKEUPENABLE	GPMC_A21_OFFMODEPULLTYPESELECT	GPMC_A21_OFFMODEPULLUDENABLE	GPMC_A21_OFFMODEOUTVALUE	GPMC_A21_OFFMODEOUTENABLE	GPMC_A21_OFFMODEENABLE	GPMC_A21_INPUTENABLE	RESERVED			GPMC_A21_PULLTYPESELECT	GPMC_A21_PULLUDENABLE	GPMC_A21_MUXMODE			GPMC_A20_WAKEUPEVENT	GPMC_A20_WAKEUPENABLE	GPMC_A20_OFFMODEPULLTYPESELECT	GPMC_A20_OFFMODEPULLUDENABLE	GPMC_A20_OFFMODEOUTVALUE	GPMC_A20_OFFMODEOUTENABLE	GPMC_A20_OFFMODEENABLE	GPMC_A20_INPUTENABLE	RESERVED			GPMC_A20_PULLTYPESELECT	GPMC_A20_PULLUDENABLE	GPMC_A20_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	GPMC_A21_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	GPMC_A21_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29	GPMC_A21_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad gpmc_a21 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
28	GPMC_A21_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad gpmc_a21 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	GPMC_A21_OFFMODEOUTVALUE	OffMode mode output value for pad gpmc_a21 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	GPMC_A21_OFFMODEOUTENABLE	OffMode mode output enable value for pad gpmc_a21. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	GPMC_A21_OFFMODEENABLE	OffMode mode override control for pad gpmc_a21 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
24	GPMC_A21_INPUTENABLE	Input enable value for pad gpmc_a21 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1

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Bits	Field Name	Description	Type	Reset
23:21	RESERVED		R	0x0
20	GPMC_A21_PULLTYPESELECT	pullup/down selection for pad gpmc_a21 0x0: pulldown selected 0x1: pullup selected	RW	0
19	GPMC_A21_PULLUDENABLE	pullup/down enable for pad gpmc_a21 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	GPMC_A21_MUXMODE	Functional multiplexing selection for pad gpmc_a21 0x0: Select gpmc_a21 0x1: Select kpd_col5 0x2: Select c2c_datain5 0x3: Select gpio_45 0x4: Select venc_656_data5 0x7: Select safe_mode	RW	0x7
15	GPMC_A20_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	GPMC_A20_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	GPMC_A20_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad gpmc_a20 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
12	GPMC_A20_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad gpmc_a20 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	GPMC_A20_OFFMODEOUTVALUE	OffMode mode output value for pad gpmc_a20 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	GPMC_A20_OFFMODEOUTENABLE	OffMode mode output enable value for pad gpmc_a20. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	GPMC_A20_OFFMODEENABLE	OffMode mode override control for pad gpmc_a20 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	GPMC_A20_INPUTENABLE	Input enable value for pad gpmc_a20 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	GPMC_A20_PULLTYPESELECT	pullup/down selection for pad gpmc_a20 0x0: pulldown selected 0x1: pullup selected	RW	0
3	GPMC_A20_PULLUDENABLE	pullup/down enable for pad gpmc_a20 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1

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Bits	Field Name	Description	Type	Reset
2:0	GPMC_A20_MUXMODE	Functional multiplexing selection for pad gpmc_a20 0x0: Select gpmc_a20 0x1: Select kpd_col4 0x2: Select c2c_datain4 0x3: Select gpio_44 0x4: Select venc_656_data4 0x7: Select safe_mode	RW	0x7

Table 18-369. Register Call Summary for Register CONTROL_CORE_PAD0_GPMC_A20_PAD1_GPMC_A21

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- SYSCTRL_PADCONF_CORE Register Summary: [2]

Table 18-370. CONTROL_CORE_PAD0_GPMC_A22_PAD1_GPMC_A23

Address Offset	0x0000 006C		
Physical Address	0x4A10 006C	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads gpmc_a22 and gpmc_a23 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPMC_A23_WAKEUPEVENT	GPMC_A23_WAKEUPENABLE	GPMC_A23_OFFMODEPULLTYPESELECT	GPMC_A23_OFFMODEPULLUDENABLE	GPMC_A23_OFFMODEOUTVALUE	GPMC_A23_OFFMODEOUTENABLE	GPMC_A23_OFFMODEENABLE	GPMC_A23_INPUTENABLE	RESERVED			GPMC_A23_PULLTYPESELECT	GPMC_A23_PULLUDENABLE	GPMC_A23_MUXMODE			GPMC_A22_WAKEUPEVENT	GPMC_A22_WAKEUPENABLE	GPMC_A22_OFFMODEPULLTYPESELECT	GPMC_A22_OFFMODEPULLUDENABLE	GPMC_A22_OFFMODEOUTVALUE	GPMC_A22_OFFMODEOUTENABLE	GPMC_A22_OFFMODEENABLE	GPMC_A22_INPUTENABLE	RESERVED			GPMC_A22_PULLTYPESELECT	GPMC_A22_PULLUDENABLE	GPMC_A22_MUXMODE	

Bits	Field Name	Description	Type	Reset
31	GPMC_A23_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	GPMC_A23_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29	GPMC_A23_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad gpmc_a23 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0

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Bits	Field Name	Description	Type	Reset
28	GPMC_A23_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad gpmc_a23 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	GPMC_A23_OFFMODEOUTVALUE	OffMode mode output value for pad gpmc_a23 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	GPMC_A23_OFFMODEOUTENABLE	OffMode mode output enable value for pad gpmc_a23. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	GPMC_A23_OFFMODEENABLE	OffMode mode override control for pad gpmc_a23 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
24	GPMC_A23_INPUTENABLE	Input enable value for pad gpmc_a23 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	GPMC_A23_PULLTYPESELECT	pullup/down selection for pad gpmc_a23 0x0: pulldown selected 0x1: pullup selected	RW	0
19	GPMC_A23_PULLUDENABLE	pullup/down enable for pad gpmc_a23 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	GPMC_A23_MUXMODE	Functional multiplexing selection for pad gpmc_a23 0x0: Select gpmc_a23 0x1: Select kpd_col7 0x2: Select c2c_datain7 0x3: Select gpio_47 0x4: Select venc_656_data7 0x7: Select safe_mode	RW	0x7
15	GPMC_A22_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	GPMC_A22_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	GPMC_A22_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad gpmc_a22 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
12	GPMC_A22_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad gpmc_a22 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	GPMC_A22_OFFMODEOUTVALUE	OffMode mode output value for pad gpmc_a22 0x0: Set value at 0 0x1: Set value at 1	RW	0

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Bits	Field Name	Description	Type	Reset
10	GPMC_A22_OFFMODEOUTENABLE	OffMode mode output enable value for pad gpmc_a22. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	GPMC_A22_OFFMODEENABLE	OffMode mode override control for pad gpmc_a22 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	GPMC_A22_INPUTENABLE	Input enable value for pad gpmc_a22 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	GPMC_A22_PULLTYPESELECT	pullup/down selection for pad gpmc_a22 0x0: pulldown selected 0x1: pullup selected	RW	0
3	GPMC_A22_PULLUDENABLE	pullup/down enable for pad gpmc_a22 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	GPMC_A22_MUXMODE	Functional multiplexing selection for pad gpmc_a22 0x0: Select gpmc_a22 0x1: Select kpd_col6 0x2: Select c2c_datain6 0x3: Select gpio_46 0x4: Select venc_656_data6 0x7: Select safe_mode	RW	0x7

Table 18-371. Register Call Summary for Register CONTROL_CORE_PAD0_GPMC_A22_PAD1_GPMC_A23

Control Module Functional Description • Pad Multiplexing Register Fields: [0] [1]
Control Module Register Manual • SYSCTRL_PADCONF_CORE Register Summary: [2]

Table 18-372. CONTROL_CORE_PAD0_GPMC_A24_PAD1_GPMC_A25

Address Offset	0x0000 0070		
Physical Address	0x4A10 0070	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads gpmc_a24 and gpmc_a25 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPMC_A25_WAKEUPEVENT	GPMC_A25_WAKEUPENABLE	GPMC_A25_OFFMODEPULLTYPESELECT	GPMC_A25_OFFMODEPULLUDENABLE	GPMC_A25_OFFMODEOUTVALUE	GPMC_A25_OFFMODEOUTENABLE	GPMC_A25_OFFMODEENABLE	GPMC_A25_INPUTENABLE	RESERVED			GPMC_A25_PULLTYPESELECT	GPMC_A25_PULLUDENABLE	GPMC_A25_MUXMODE			GPMC_A24_WAKEUPEVENT	GPMC_A24_WAKEUPENABLE	GPMC_A24_OFFMODEPULLTYPESELECT	GPMC_A24_OFFMODEPULLUDENABLE	GPMC_A24_OFFMODEOUTVALUE	GPMC_A24_OFFMODEOUTENABLE	GPMC_A24_OFFMODEENABLE	GPMC_A24_INPUTENABLE	RESERVED			GPMC_A24_PULLTYPESELECT	GPMC_A24_PULLUDENABLE	GPMC_A24_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	GPMC_A25_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	GPMC_A25_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29	GPMC_A25_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad gpmc_a25 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
28	GPMC_A25_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad gpmc_a25 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	GPMC_A25_OFFMODEOUTVALUE	OffMode mode output value for pad gpmc_a25 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	GPMC_A25_OFFMODEOUTENABLE	OffMode mode output enable value for pad gpmc_a25. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	GPMC_A25_OFFMODEENABLE	OffMode mode override control for pad gpmc_a25 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
24	GPMC_A25_INPUTENABLE	Input enable value for pad gpmc_a25 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	GPMC_A25_PULLTYPESELECT	pullup/down selection for pad gpmc_a25 0x0: pulldown selected 0x1: pullup selected	RW	0
19	GPMC_A25_PULLUDENABLE	pullup/down enable for pad gpmc_a25 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1

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Bits	Field Name	Description	Type	Reset
18:16	GPMC_A25_MUXMODE	Functional multiplexing selection for pad gpmc_a25 0x0: Select gpmc_a25 0x2: Select c2c_clkout1 0x3: Select gpio_49 0x7: Select safe_mode	RW	0x7
15	GPMC_A24_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	GPMC_A24_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	GPMC_A24_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad gpmc_a24 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
12	GPMC_A24_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad gpmc_a24 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	GPMC_A24_OFFMODEOUTVALUE	OffMode mode output value for pad gpmc_a24 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	GPMC_A24_OFFMODEOUTENABLE	OffMode mode output enable value for pad gpmc_a24. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	GPMC_A24_OFFMODEENABLE	OffMode mode override control for pad gpmc_a24 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	GPMC_A24_INPUTENABLE	Input enable value for pad gpmc_a24 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	GPMC_A24_PULLTYPESELECT	pullup/down selection for pad gpmc_a24 0x0: pulldown selected 0x1: pullup selected	RW	0
3	GPMC_A24_PULLUDENABLE	pullup/down enable for pad gpmc_a24 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	GPMC_A24_MUXMODE	Functional multiplexing selection for pad gpmc_a24 0x0: Select gpmc_a24 0x1: Select kpd_col8 0x2: Select c2c_clkout0 0x3: Select gpio_48 0x7: Select safe_mode	RW	0x7

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Table 18-373. Register Call Summary for Register CONTROL_CORE_PAD0_GPMC_A24_PAD1_GPMC_A25

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- SYSCTRL_PADCONF_CORE Register Summary: [2]

Table 18-374. CONTROL_CORE_PAD0_GPMC_NCS0_PAD1_GPMC_NCS1

Address Offset	0x0000 0074		
Physical Address	0x4A10 0074	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads gpmc_ncs0 and gpmc_ncs1 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPMC_NCS1_WAKEUPEVENT	GPMC_NCS1_WAKEUPENABLE	GPMC_NCS1_OFFMODEPULLTYPESELECT	GPMC_NCS1_OFFMODEPULLUDENABLE	GPMC_NCS1_OFFMODEOUTVALUE	GPMC_NCS1_OFFMODEOUTENABLE	GPMC_NCS1_OFFMODEENABLE	GPMC_NCS1_INPUTENABLE	RESERVED			GPMC_NCS1_PULLTYPESELECT	GPMC_NCS1_PULLUDENABLE	GPMC_NCS1_MUXMODE			GPMC_NCS0_WAKEUPEVENT	GPMC_NCS0_WAKEUPENABLE	GPMC_NCS0_OFFMODEPULLTYPESELECT	GPMC_NCS0_OFFMODEPULLUDENABLE	GPMC_NCS0_OFFMODEOUTVALUE	GPMC_NCS0_OFFMODEOUTENABLE	GPMC_NCS0_OFFMODEENABLE	GPMC_NCS0_INPUTENABLE	RESERVED			GPMC_NCS0_PULLTYPESELECT	GPMC_NCS0_PULLUDENABLE	GPMC_NCS0_MUXMODE	

Bits	Field Name	Description	Type	Reset
31	GPMC_NCS1_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	GPMC_NCS1_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29	GPMC_NCS1_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad gpmc_ncs1 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
28	GPMC_NCS1_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad gpmc_ncs1 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	GPMC_NCS1_OFFMODEOUTVALUE	OffMode mode output value for pad gpmc_ncs1 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	GPMC_NCS1_OFFMODEOUTENABLE	OffMode mode output enable value for pad gpmc_ncs1. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0

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Bits	Field Name	Description	Type	Reset
25	GPMC_NCS1_OFFMODEENABLE	OffMode mode override control for pad gpmc_ncs1 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
24	GPMC_NCS1_INPUTENABLE	Input enable value for pad gpmc_ncs1 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	GPMC_NCS1_PULLTYPESELECT	pullup/down selection for pad gpmc_ncs1 0x0: pulldown selected 0x1: pullup selected	RW	1
19	GPMC_NCS1_PULLUDENABLE	pullup/down enable for pad gpmc_ncs1 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	GPMC_NCS1_MUXMODE	Functional multiplexing selection for pad gpmc_ncs1 0x0: Select gpmc_ncs1 0x2: Select c2c_dataout6 0x3: Select gpio_51 0x7: Select safe_mode	RW	0x7
15	GPMC_NCS0_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	GPMC_NCS0_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	GPMC_NCS0_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad gpmc_ncs0 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
12	GPMC_NCS0_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad gpmc_ncs0 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	GPMC_NCS0_OFFMODEOUTVALUE	OffMode mode output value for pad gpmc_ncs0 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	GPMC_NCS0_OFFMODEOUTENABLE	OffMode mode output enable value for pad gpmc_ncs0. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	GPMC_NCS0_OFFMODEENABLE	OffMode mode override control for pad gpmc_ncs0 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	GPMC_NCS0_INPUTENABLE	Input enable value for pad gpmc_ncs0 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
4	GPMC_NCS0_PULLTYPESELECT	pullup/down selection for pad gpmc_ncs0 0x0: pulldown selected 0x1: pullup selected	RW	1
3	GPMC_NCS0_PULLUDENABLE	pullup/down enable for pad gpmc_ncs0 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	GPMC_NCS0_MUXMODE	Functional multiplexing selection for pad gpmc_ncs0 0x0: Select gpmc_ncs0 0x3: Select gpio_50 0x4: Select sys_ndmareq0	RW	0x0

Table 18-375. Register Call Summary for Register CONTROL_CORE_PAD0_GPMC_NCS0_PAD1_GPMC_NCS1

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- SYSCTRL_PADCONF_CORE Register Summary: [2]

Table 18-376. CONTROL_CORE_PAD0_GPMC_NCS2_PAD1_GPMC_NCS3

Address Offset	0x0000 0078		
Physical Address	0x4A10 0078	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads gpmc_ncs2 and gpmc_ncs3 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPMC_NCS3_WAKEUPEVENT	GPMC_NCS3_WAKEUPENABLE	GPMC_NCS3_OFFMODEPULLTYPESELECT	GPMC_NCS3_OFFMODEPULLUDENABLE	GPMC_NCS3_OFFMODEOUTVALUE	GPMC_NCS3_OFFMODEOUTENABLE	GPMC_NCS3_OFFMODEENABLE	GPMC_NCS3_INPUTENABLE	RESERVED			GPMC_NCS3_PULLTYPESELECT	GPMC_NCS3_PULLUDENABLE	GPMC_NCS3_MUXMODE			GPMC_NCS2_WAKEUPEVENT	GPMC_NCS2_WAKEUPENABLE	GPMC_NCS2_OFFMODEPULLTYPESELECT	GPMC_NCS2_OFFMODEPULLUDENABLE	GPMC_NCS2_OFFMODEOUTVALUE	GPMC_NCS2_OFFMODEOUTENABLE	GPMC_NCS2_OFFMODEENABLE	GPMC_NCS2_INPUTENABLE	RESERVED			GPMC_NCS2_PULLTYPESELECT	GPMC_NCS2_PULLUDENABLE	GPMC_NCS2_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	GPMC_NCS3_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	GPMC_NCS3_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0

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Bits	Field Name	Description	Type	Reset
29	GPMC_NCS3_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad gpmc_ncs3 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
28	GPMC_NCS3_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad gpmc_ncs3 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	GPMC_NCS3_OFFMODEOUTV ALUE	OffMode mode output value for pad gpmc_ncs3 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	GPMC_NCS3_OFFMODEOUTE NABLE	OffMode mode output enable value for pad gpmc_ncs3. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	GPMC_NCS3_OFFMODEENAB LE	OffMode mode override control for pad gpmc_ncs3 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
24	GPMC_NCS3_INPUTENABLE	Input enable value for pad gpmc_ncs3 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	GPMC_NCS3_PULLTYPESELE CT	pullup/down selection for pad gpmc_ncs3 0x0: pulldown selected 0x1: pullup selected	RW	1
19	GPMC_NCS3_PULLUDENABLE	pullup/down enable for pad gpmc_ncs3 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	GPMC_NCS3_MUXMODE	Functional multiplexing selection for pad gpmc_ncs3 0x0: Select gpmc_ncs3 0x1: Select gpmc_dir 0x2: Select c2c_dataout4 0x3: Select gpio_53 0x7: Select safe_mode	RW	0x7
15	GPMC_NCS2_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	GPMC_NCS2_WAKEUPENABL E	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	GPMC_NCS2_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad gpmc_ncs2 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
12	GPMC_NCS2_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad gpmc_ncs2 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	GPMC_NCS2_OFFMODEOUTV ALUE	OffMode mode output value for pad gpmc_ncs2 0x0: Set value at 0 0x1: Set value at 1	RW	0

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Bits	Field Name	Description	Type	Reset
10	GPMC_NCS2_OFFMODEOUTENABLE	OffMode mode output enable value for pad gpmc_ncs2. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	GPMC_NCS2_OFFMODEENABLE	OffMode mode override control for pad gpmc_ncs2 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	GPMC_NCS2_INPUTENABLE	Input enable value for pad gpmc_ncs2 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	GPMC_NCS2_PULLTYPESELECT	pullup/down selection for pad gpmc_ncs2 0x0: pulldown selected 0x1: pullup selected	RW	1
3	GPMC_NCS2_PULLUDENABLE	pullup/down enable for pad gpmc_ncs2 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	GPMC_NCS2_MUXMODE	Functional multiplexing selection for pad gpmc_ncs2 0x0: Select gpmc_ncs2 0x1: Select kpd_row8 0x2: Select c2c_dataout7 0x3: Select gpio_52 0x7: Select safe_mode	RW	0x7

Table 18-377. Register Call Summary for Register CONTROL_CORE_PAD0_GPMC_NCS2_PAD1_GPMC_NCS3

Control Module Functional Description • Pad Multiplexing Register Fields: [0] [1]
Control Module Register Manual • SYSCTRL_PADCONF_CORE Register Summary: [2]

Table 18-378. CONTROL_CORE_PAD0_GPMC_NWP_PAD1_GPMC_CLK

Address Offset	0x0000 007C		
Physical Address	0x4A10 007C	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads gpmc_nwp and gpmc_clk Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPMC_CLK_WAKEUPEVENT	GPMC_CLK_WAKEUPENABLE	GPMC_CLK_OFFMODEPULLTYPESELECT	GPMC_CLK_OFFMODEPULLUDENABLE	GPMC_CLK_OFFMODEOUTVALUE	GPMC_CLK_OFFMODEOUTENABLE	GPMC_CLK_OFFMODEENABLE	GPMC_CLK_INPUTENABLE	RESERVED			GPMC_CLK_PULLTYPESELECT	GPMC_CLK_PULLUDENABLE	GPMC_CLK_MUXMODE			GPMC_NWP_WAKEUPEVENT	GPMC_NWP_WAKEUPENABLE	GPMC_NWP_OFFMODEPULLTYPESELECT	GPMC_NWP_OFFMODEPULLUDENABLE	GPMC_NWP_OFFMODEOUTVALUE	GPMC_NWP_OFFMODEOUTENABLE	GPMC_NWP_OFFMODEENABLE	GPMC_NWP_INPUTENABLE	RESERVED			GPMC_NWP_PULLTYPESELECT	GPMC_NWP_PULLUDENABLE	GPMC_NWP_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	GPMC_CLK_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	GPMC_CLK_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29	GPMC_CLK_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad gpmc_clk 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
28	GPMC_CLK_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad gpmc_clk 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	GPMC_CLK_OFFMODEOUTVALUE	OffMode mode output value for pad gpmc_clk 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	GPMC_CLK_OFFMODEOUTENABLE	OffMode mode output enable value for pad gpmc_clk. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	GPMC_CLK_OFFMODEENABLE	OffMode mode override control for pad gpmc_clk 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
24	GPMC_CLK_INPUTENABLE	Input enable value for pad gpmc_clk 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	GPMC_CLK_PULLTYPESELECT	pullup/down selection for pad gpmc_clk 0x0: pulldown selected 0x1: pullup selected	RW	0
19	GPMC_CLK_PULLUDENABLE	pullup/down enable for pad gpmc_clk 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1

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Bits	Field Name	Description	Type	Reset
18:16	GPMC_CLK_MUXMODE	Functional multiplexing selection for pad gpmc_clk 0x0: Select gpmc_clk 0x3: Select gpio_55 0x4: Select sys_ndmareq2 0x5: Select sdmmc1_cmd	RW	0x0
15	GPMC_NWP_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	GPMC_NWP_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	GPMC_NWP_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad gpmc_nwp 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
12	GPMC_NWP_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad gpmc_nwp 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	GPMC_NWP_OFFMODEOUTVALUE	OffMode mode output value for pad gpmc_nwp 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	GPMC_NWP_OFFMODEOUTENABLE	OffMode mode output enable value for pad gpmc_nwp. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	GPMC_NWP_OFFMODEENABLE	OffMode mode override control for pad gpmc_nwp 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	GPMC_NWP_INPUTENABLE	Input enable value for pad gpmc_nwp 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	GPMC_NWP_PULLTYPESELECT	pullup/down selection for pad gpmc_nwp 0x0: pulldown selected 0x1: pullup selected	RW	0
3	GPMC_NWP_PULLUDENABLE	pullup/down enable for pad gpmc_nwp 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	GPMC_NWP_MUXMODE	Functional multiplexing selection for pad gpmc_nwp 0x0: Select gpmc_nwp 0x1: Select dsi1_te0 0x3: Select gpio_54 0x4: Select sys_ndmareq1	RW	0x0

Table 18-379. Register Call Summary for Register CONTROL_CORE_PAD0_GPMC_NWP_PAD1_GPMC_CLK

Control Module Functional Description

- Pad Multiplexing Register Fields: [0] [1]

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Table 18-379. Register Call Summary for Register CONTROL_CORE_PAD0_GPMC_NWP_PAD1_GPMC_CLK (continued)

Control Module Register Manual

- SYSCTRL_PADCONF_CORE Register Summary: [2]

Table 18-380. CONTROL_CORE_PAD0_GPMC_NADV_ALE_PAD1_GPMC_NOE

Address Offset	0x0000 0080		
Physical Address	0x4A10 0080	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads gpmc_nadv_ale and gpmc_noe Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPMC_NOE_WAKEUPEVENT	GPMC_NOE_WAKEUPENABLE	GPMC_NOE_OFFMODEPULLTYPESELECT	GPMC_NOE_OFFMODEPULLUDENABLE	GPMC_NOE_OFFMODEOUTVALUE	GPMC_NOE_OFFMODEOUTENABLE	GPMC_NOE_OFFMODEENABLE	GPMC_NOE_INPUTENABLE	RESERVED			GPMC_NOE_PULLTYPESELECT	GPMC_NOE_PULLUDENABLE	GPMC_NOE_MUXMODE			GPMC_NADV_ALE_WAKEUPEVENT	GPMC_NADV_ALE_WAKEUPENABLE	GPMC_NADV_ALE_OFFMODEPULLTYPESELECT	GPMC_NADV_ALE_OFFMODEPULLUDENABLE	GPMC_NADV_ALE_OFFMODEOUTVALUE	GPMC_NADV_ALE_OFFMODEOUTENABLE	GPMC_NADV_ALE_OFFMODEENABLE	GPMC_NADV_ALE_INPUTENABLE	RESERVED			GPMC_NADV_ALE_PULLTYPESELECT	GPMC_NADV_ALE_PULLUDENABLE	GPMC_NADV_ALE_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	GPMC_NOE_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	GPMC_NOE_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29	GPMC_NOE_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad gpmc_noe 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
28	GPMC_NOE_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad gpmc_noe 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	GPMC_NOE_OFFMODEOUTVALUE	OffMode mode output value for pad gpmc_noe 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	GPMC_NOE_OFFMODEOUTENABLE	OffMode mode output enable value for pad gpmc_noe. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0

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Bits	Field Name	Description	Type	Reset
25	GPMC_NOE_OFFMODEENABLE	OffMode mode override control for pad gpmc_noe 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
24	GPMC_NOE_INPUTENABLE	Input enable value for pad gpmc_noe 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	GPMC_NOE_PULLTYPESELECT	pullup/down selection for pad gpmc_noe 0x0: pulldown selected 0x1: pullup selected	RW	1
19	GPMC_NOE_PULLUDENABLE	pullup/down enable for pad gpmc_noe 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	GPMC_NOE_MUXMODE	Functional multiplexing selection for pad gpmc_noe 0x0: Select gpmc_noe 0x1: Select sdmmc2_clk	RW	0x0
15	GPMC_NADV_ALE_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	GPMC_NADV_ALE_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	GPMC_NADV_ALE_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad gpmc_nadv_ale 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
12	GPMC_NADV_ALE_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad gpmc_nadv_ale 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	GPMC_NADV_ALE_OFFMODEOUTVALUE	OffMode mode output value for pad gpmc_nadv_ale 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	GPMC_NADV_ALE_OFFMODEOUTENABLE	OffMode mode output enable value for pad gpmc_nadv_ale. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	GPMC_NADV_ALE_OFFMODEENABLE	OffMode mode override control for pad gpmc_nadv_ale 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	GPMC_NADV_ALE_INPUTENABLE	Input enable value for pad gpmc_nadv_ale 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	GPMC_NADV_ALE_PULLTYPESELECT	pullup/down selection for pad gpmc_nadv_ale 0x0: pulldown selected 0x1: pullup selected	RW	0

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Bits	Field Name	Description	Type	Reset
3	GPMC_NADV_ALE_PULLUDENABLE	pullup/down enable for pad gpmc_nadv_ale 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	GPMC_NADV_ALE_MUXMODE	Functional multiplexing selection for pad gpmc_nadv_ale 0x0: Select gpmc_nadv_ale 0x1: Select dsi1_te1 0x3: Select gpio_56 0x4: Select sys_ndmareq3 0x5: Select sdmmc1_clk	RW	0x0

Table 18-381. Register Call Summary for Register CONTROL_CORE_PAD0_GPMC_NADV_ALE_PAD1_GPMC_NOE

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- SYSCTRL_PADCONF_CORE Register Summary: [2]

Table 18-382. CONTROL_CORE_PAD0_GPMC_NWE_PAD1_GPMC_NBE0_CLE

Address Offset	0x0000 0084		
Physical Address	0x4A10 0084	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads gpmc_nwe and gpmc_nbe0_cle Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPMC_NBE0_CLE_WAKEUPEVENT	GPMC_NBE0_CLE_WAKEUPENABLE	GPMC_NBE0_CLE_OFFMODEPULLTYPESELECT	GPMC_NBE0_CLE_OFFMODEPULLUDENABLE	GPMC_NBE0_CLE_OFFMODEOUTVALUE	GPMC_NBE0_CLE_OFFMODEOUTENABLE	GPMC_NBE0_CLE_OFFMODEENABLE	GPMC_NBE0_CLE_INPUTENABLE	RESERVED			GPMC_NBE0_CLE_PULLTYPESELECT	GPMC_NBE0_CLE_PULLUDENABLE	GPMC_NBE0_CLE_MUXMODE			GPMC_NWE_WAKEUPEVENT	GPMC_NWE_WAKEUPENABLE	GPMC_NWE_OFFMODEPULLTYPESELECT	GPMC_NWE_OFFMODEPULLUDENABLE	GPMC_NWE_OFFMODEOUTVALUE	GPMC_NWE_OFFMODEOUTENABLE	GPMC_NWE_OFFMODEENABLE	GPMC_NWE_INPUTENABLE	RESERVED			GPMC_NWE_PULLTYPESELECT	GPMC_NWE_PULLUDENABLE	GPMC_NWE_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	GPMC_NBE0_CLE_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	GPMC_NBE0_CLE_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0

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Bits	Field Name	Description	Type	Reset
29	GPMC_NBE0_CLE_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad gpmc_nbe0_cle 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
28	GPMC_NBE0_CLE_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad gpmc_nbe0_cle 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	GPMC_NBE0_CLE_OFFMODE OUTVALUE	OffMode mode output value for pad gpmc_nbe0_cle 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	GPMC_NBE0_CLE_OFFMODE OUTENABLE	OffMode mode output enable value for pad gpmc_nbe0_cle. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	GPMC_NBE0_CLE_OFFMODEE NABLE	OffMode mode override control for pad gpmc_nbe0_cle 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
24	GPMC_NBE0_CLE_INPUTENAB LE	Input enable value for pad gpmc_nbe0_cle 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	GPMC_NBE0_CLE_PULLTYPE SELECT	pullup/down selection for pad gpmc_nbe0_cle 0x0: pulldown selected 0x1: pullup selected	RW	0
19	GPMC_NBE0_CLE_PULLUDEN ABLE	pullup/down enable for pad gpmc_nbe0_cle 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	GPMC_NBE0_CLE_MUXMODE	Functional multiplexing selection for pad gpmc_nbe0_cle 0x0: Select gpmc_nbe0_cle 0x1: Select dsi2_te0 0x3: Select gpio_59	RW	0x0
15	GPMC_NWE_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	GPMC_NWE_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	GPMC_NWE_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad gpmc_nwe 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
12	GPMC_NWE_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad gpmc_nwe 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	GPMC_NWE_OFFMODEOUTVA LUE	OffMode mode output value for pad gpmc_nwe 0x0: Set value at 0 0x1: Set value at 1	RW	0

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Bits	Field Name	Description	Type	Reset
10	GPMC_NWE_OFFMODEOUTENABLE	OffMode mode output enable value for pad gpmc_nwe. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	GPMC_NWE_OFFMODEENABLE	OffMode mode override control for pad gpmc_nwe 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	GPMC_NWE_INPUTENABLE	Input enable value for pad gpmc_nwe 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	GPMC_NWE_PULLTYPESELECT	pullup/down selection for pad gpmc_nwe 0x0: pulldown selected 0x1: pullup selected	RW	1
3	GPMC_NWE_PULLUDENABLE	pullup/down enable for pad gpmc_nwe 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	GPMC_NWE_MUXMODE	Functional multiplexing selection for pad gpmc_nwe 0x0: Select gpmc_nwe 0x1: Select sdmmc2_cmd	RW	0x0

Table 18-383. Register Call Summary for Register CONTROL_CORE_PAD0_GPMC_NWE_PAD1_GPMC_NBE0_CLE

Control Module Functional Description • Pad Multiplexing Register Fields: [0] [1]
Control Module Register Manual • SYSCTRL_PADCONF_CORE Register Summary: [2]

Table 18-384. CONTROL_CORE_PAD0_GPMC_NBE1_PAD1_GPMC_WAIT0

Address Offset	0x0000 0088		
Physical Address	0x4A10 0088	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads gpmc_nbe1 and gpmc_wait0 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPMC_WAIT0_WAKEUPEVENT	GPMC_WAIT0_WAKEUPENABLE	GPMC_WAIT0_OFFMODEPULLTYPESELECT	GPMC_WAIT0_OFFMODEPULLUDENABLE	GPMC_WAIT0_OFFMODEOUTVALUE	GPMC_WAIT0_OFFMODEOUTENABLE	GPMC_WAIT0_OFFMODEENABLE	GPMC_WAIT0_INPUTENABLE	RESERVED			GPMC_WAIT0_PULLTYPESELECT	GPMC_WAIT0_PULLUDENABLE	GPMC_WAIT0_MUXMODE			GPMC_NBE1_WAKEUPEVENT	GPMC_NBE1_WAKEUPENABLE	GPMC_NBE1_OFFMODEPULLTYPESELECT	GPMC_NBE1_OFFMODEPULLUDENABLE	GPMC_NBE1_OFFMODEOUTVALUE	GPMC_NBE1_OFFMODEOUTENABLE	GPMC_NBE1_OFFMODEENABLE	GPMC_NBE1_INPUTENABLE	RESERVED			GPMC_NBE1_PULLTYPESELECT	GPMC_NBE1_PULLUDENABLE	GPMC_NBE1_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	GPMC_WAIT0_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	GPMC_WAIT0_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29	GPMC_WAIT0_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad gpmc_wait0 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
28	GPMC_WAIT0_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad gpmc_wait0 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	GPMC_WAIT0_OFFMODEOUTVALUE	OffMode mode output value for pad gpmc_wait0 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	GPMC_WAIT0_OFFMODEOUTENABLE	OffMode mode output enable value for pad gpmc_wait0. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	GPMC_WAIT0_OFFMODEENABLE	OffMode mode override control for pad gpmc_wait0 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
24	GPMC_WAIT0_INPUTENABLE	Input enable value for pad gpmc_wait0 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	GPMC_WAIT0_PULLTYPESELECT	pullup/down selection for pad gpmc_wait0 0x0: pulldown selected 0x1: pullup selected	RW	1
19	GPMC_WAIT0_PULLUDENABLE	pullup/down enable for pad gpmc_wait0 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1

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Bits	Field Name	Description	Type	Reset
18:16	GPMC_WAIT0_MUXMODE	Functional multiplexing selection for pad gpmc_wait0 0x0: Select gpmc_wait0 0x1: Select dsi2_te1 0x3: Select gpio_61	RW	0x0
15	GPMC_NBE1_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	GPMC_NBE1_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	GPMC_NBE1_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad gpmc_nbe1 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
12	GPMC_NBE1_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad gpmc_nbe1 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	GPMC_NBE1_OFFMODEOUTVALUE	OffMode mode output value for pad gpmc_nbe1 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	GPMC_NBE1_OFFMODEOUTENABLE	OffMode mode output enable value for pad gpmc_nbe1. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	GPMC_NBE1_OFFMODEENABLE	OffMode mode override control for pad gpmc_nbe1 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	GPMC_NBE1_INPUTENABLE	Input enable value for pad gpmc_nbe1 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	GPMC_NBE1_PULLTYPESELECT	pullup/down selection for pad gpmc_nbe1 0x0: pulldown selected 0x1: pullup selected	RW	0
3	GPMC_NBE1_PULLUDENABLE	pullup/down enable for pad gpmc_nbe1 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	GPMC_NBE1_MUXMODE	Functional multiplexing selection for pad gpmc_nbe1 0x0: Select gpmc_nbe1 0x2: Select c2c_dataout5 0x3: Select gpio_60 0x7: Select safe_mode	RW	0x7

Table 18-385. Register Call Summary for Register CONTROL_CORE_PAD0_GPMC_NBE1_PAD1_GPMC_WAIT0

Control Module Functional Description • Pad Multiplexing Register Fields: [0] [1]
Control Module Register Manual • SYSCTRL_PADCONF_CORE Register Summary: [2]

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Table 18-386. CONTROL_CORE_PAD0_GPMC_WAIT1_PAD1_GPMC_WAIT2

Address Offset	0x0000 008C		
Physical Address	0x4A10 008C	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads gpmc_wait1 and gpmc_wait2 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPMC_WAIT2_WAKEUPEVENT	GPMC_WAIT2_WAKEUPENABLE	GPMC_WAIT2_OFFMODEPULLTYPESELECT	GPMC_WAIT2_OFFMODEPULLUDENABLE	GPMC_WAIT2_OFFMODEOUTVALUE	GPMC_WAIT2_OFFMODEOUTENABLE	GPMC_WAIT2_OFFMODEENABLE	GPMC_WAIT2_INPUTENABLE	RESERVED			GPMC_WAIT2_PULLTYPESELECT	GPMC_WAIT2_PULLUDENABLE	GPMC_WAIT2_MUXMODE			GPMC_WAIT1_WAKEUPEVENT	GPMC_WAIT1_WAKEUPENABLE	GPMC_WAIT1_OFFMODEPULLTYPESELECT	GPMC_WAIT1_OFFMODEPULLUDENABLE	GPMC_WAIT1_OFFMODEOUTVALUE	GPMC_WAIT1_OFFMODEOUTENABLE	GPMC_WAIT1_OFFMODEENABLE	GPMC_WAIT1_INPUTENABLE	RESERVED			GPMC_WAIT1_PULLTYPESELECT	GPMC_WAIT1_PULLUDENABLE	GPMC_WAIT1_MUXMODE	

Bits	Field Name	Description	Type	Reset
31	GPMC_WAIT2_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	GPMC_WAIT2_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29	GPMC_WAIT2_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad gpmc_wait2 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
28	GPMC_WAIT2_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad gpmc_wait2 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	GPMC_WAIT2_OFFMODEOUTVALUE	OffMode mode output value for pad gpmc_wait2 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	GPMC_WAIT2_OFFMODEOUTENABLE	OffMode mode output enable value for pad gpmc_wait2. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	GPMC_WAIT2_OFFMODEENABLE	OffMode mode override control for pad gpmc_wait2 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0

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Bits	Field Name	Description	Type	Reset
24	GPMC_WAIT2_INPUTENABLE	Input enable value for pad gpmc_wait2 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	GPMC_WAIT2_PULLTYPESELECT	pullup/down selection for pad gpmc_wait2 0x0: pulldown selected 0x1: pullup selected	RW	0
19	GPMC_WAIT2_PULLUDENABLE	pullup/down enable for pad gpmc_wait2 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	GPMC_WAIT2_MUXMODE	Functional multiplexing selection for pad gpmc_wait2 0x0: Select gpmc_wait2 0x1: Select usbc1_icusb_txen 0x2: Select c2c_dataout3 0x3: Select gpio_100 0x4: Select sys_ndmareq0 0x7: Select safe_mode	RW	0x7
15	GPMC_WAIT1_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	GPMC_WAIT1_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	GPMC_WAIT1_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad gpmc_wait1 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
12	GPMC_WAIT1_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad gpmc_wait1 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	GPMC_WAIT1_OFFMODEOUTVALUE	OffMode mode output value for pad gpmc_wait1 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	GPMC_WAIT1_OFFMODEOUTENABLE	OffMode mode output enable value for pad gpmc_wait1. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	GPMC_WAIT1_OFFMODEENABLE	OffMode mode override control for pad gpmc_wait1 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	GPMC_WAIT1_INPUTENABLE	Input enable value for pad gpmc_wait1 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
4	GPMC_WAIT1_PULLTYPESELECT	pullup/down selection for pad gpmc_wait1 0x0: pulldown selected 0x1: pullup selected	RW	1
3	GPMC_WAIT1_PULLUDENABLE	pullup/down enable for pad gpmc_wait1 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	GPMC_WAIT1_MUXMODE	Functional multiplexing selection for pad gpmc_wait1 0x0: Select gpmc_wait1 0x2: Select c2c_dataout2 0x3: Select gpio_62 0x7: Select safe_mode	RW	0x7

Table 18-387. Register Call Summary for Register CONTROL_CORE_PAD0_GPMC_WAIT1_PAD1_GPMC_WAIT2

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- SYSCTRL_PADCONF_CORE Register Summary: [2]

Table 18-388. CONTROL_CORE_PAD0_GPMC_NCS4_PAD1_GPMC_NCS5

Address Offset	0x0000 0090		
Physical Address	0x4A10 0090	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads gpmc_ncs4 and gpmc_ncs5 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPMC_NCS5_WAKEUPEVENT	GPMC_NCS5_WAKEUPENABLE	GPMC_NCS5_OFFMODEPULLTYPESELECT	GPMC_NCS5_OFFMODEPULLUDENABLE	GPMC_NCS5_OFFMODEOUTVALUE	GPMC_NCS5_OFFMODEOUTENABLE	GPMC_NCS5_OFFMODEENABLE	GPMC_NCS5_INPUTENABLE	RESERVED			GPMC_NCS5_PULLTYPESELECT	GPMC_NCS5_PULLUDENABLE	GPMC_NCS5_MUXMODE			GPMC_NCS4_WAKEUPEVENT	GPMC_NCS4_WAKEUPENABLE	GPMC_NCS4_OFFMODEPULLTYPESELECT	GPMC_NCS4_OFFMODEPULLUDENABLE	GPMC_NCS4_OFFMODEOUTVALUE	GPMC_NCS4_OFFMODEOUTENABLE	GPMC_NCS4_OFFMODEENABLE	GPMC_NCS4_INPUTENABLE	RESERVED			GPMC_NCS4_PULLTYPESELECT	GPMC_NCS4_PULLUDENABLE	GPMC_NCS4_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	GPMC_NCS5_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	GPMC_NCS5_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0

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Bits	Field Name	Description	Type	Reset
29	GPMC_NCS5_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad gpmc_ncs5 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
28	GPMC_NCS5_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad gpmc_ncs5 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	GPMC_NCS5_OFFMODEOUTV ALUE	OffMode mode output value for pad gpmc_ncs5 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	GPMC_NCS5_OFFMODEOUTE NABLE	OffMode mode output enable value for pad gpmc_ncs5 . This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	GPMC_NCS5_OFFMODEENAB LE	OffMode mode override control for pad gpmc_ncs5 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
24	GPMC_NCS5_INPUTENABLE	Input enable value for pad gpmc_ncs5 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	GPMC_NCS5_PULLTYPESELE CT	pullup/down selection for pad gpmc_ncs5 0x0: pulldown selected 0x1: pullup selected	RW	0
19	GPMC_NCS5_PULLUDENABLE	pullup/down enable for pad gpmc_ncs5 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	GPMC_NCS5_MUXMODE	Functional multiplexing selection for pad gpmc_ncs5 0x0: Select gpmc_ncs5 0x1: Select dsi1_te1 0x2: Select c2c_clkin1 0x3: Select gpio_102 0x4: Select sys_ndmareq2 0x7: Select safe_mode	RW	0x7
15	GPMC_NCS4_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	GPMC_NCS4_WAKEUPENABL E	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0

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Bits	Field Name	Description	Type	Reset
13	GPMC_NCS4_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad gpmc_ncs4 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
12	GPMC_NCS4_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad gpmc_ncs4 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	GPMC_NCS4_OFFMODEOUTV ALUE	OffMode mode output value for pad gpmc_ncs4 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	GPMC_NCS4_OFFMODEOUTE NABLE	OffMode mode output enable value for pad gpmc_ncs4. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	GPMC_NCS4_OFFMODEENAB LE	OffMode mode override control for pad gpmc_ncs4 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	GPMC_NCS4_INPUTENABLE	Input enable value for pad gpmc_ncs4 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	GPMC_NCS4_PULLTYPESELE CT	pullup/down selection for pad gpmc_ncs4 0x0: pulldown selected 0x1: pullup selected	RW	0
3	GPMC_NCS4_PULLUDENABLE	pullup/down enable for pad gpmc_cs4 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	GPMC_NCS4_MUXMODE	Functional multiplexing selection for pad gpmc_ncs4 0x0: Select gpmc_ncs4 0x1: Select dsi1_te0 0x2: Select c2c_clkin0 0x3: Select gpio_101 0x4: Select sys_ndmareq1 0x7: Select safe_mode	RW	0x7

Table 18-389. Register Call Summary for Register CONTROL_CORE_PAD0_GPMC_NCS4_PAD1_GPMC_NCS5

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- SYSCTRL_PADCONF_CORE Register Summary: [2]

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Table 18-390. CONTROL_CORE_PAD0_GPMC_NCS6_PAD1_GPMC_NCS7

Address Offset	0x0000 0094		
Physical Address	0x4A10 0094	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads gpmc_ncs6 and gpmc_ncs7 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPMC_NCS7_WAKEUPEVENT	GPMC_NCS7_WAKEUPENABLE	GPMC_NCS7_OFFMODEPULLTYPESELECT	GPMC_NCS7_OFFMODEPULLUDENABLE	GPMC_NCS7_OFFMODEOUTVALUE	GPMC_NCS7_OFFMODEOUTENABLE	GPMC_NCS7_OFFMODEENABLE	GPMC_NCS7_INPUTENABLE	RESERVED			GPMC_NCS7_PULLTYPESELECT	GPMC_NCS7_PULLUDENABLE	GPMC_NCS7_MUXMODE			GPMC_NCS6_WAKEUPEVENT	GPMC_NCS6_WAKEUPENABLE	GPMC_NCS6_OFFMODEPULLTYPESELECT	GPMC_NCS6_OFFMODEPULLUDENABLE	GPMC_NCS6_OFFMODEOUTVALUE	GPMC_NCS6_OFFMODEOUTENABLE	GPMC_NCS6_OFFMODEENABLE	GPMC_NCS6_INPUTENABLE	RESERVED			GPMC_NCS6_PULLTYPESELECT	GPMC_NCS6_PULLUDENABLE	GPMC_NCS6_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	GPMC_NCS7_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	GPMC_NCS7_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29	GPMC_NCS7_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad gpmc_ncs7 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
28	GPMC_NCS7_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad gpmc_ncs7 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	GPMC_NCS7_OFFMODEOUTVALUE	OffMode mode output value for pad gpmc_ncs7 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	GPMC_NCS7_OFFMODEOUTENABLE	OffMode mode output enable value for pad gpmc_ncs7. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	GPMC_NCS7_OFFMODEENABLE	OffMode mode override control for pad gpmc_ncs7 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0

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Bits	Field Name	Description	Type	Reset
24	GPMC_NCS7_INPUTENABLE	Input enable value for pad gpmc_ncs7 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	GPMC_NCS7_PULLTYPESELECT	pullup/down selection for pad gpmc_ncs7 0x0: pulldown selected 0x1: pullup selected	RW	0
19	GPMC_NCS7_PULLUDENABLE	pullup/down enable for pad gpmc_ncs7 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	GPMC_NCS7_MUXMODE	Functional multiplexing selection for pad gpmc_ncs7 0x0: Select gpmc_ncs7 0x1: Select dsi2_te1 0x2: Select c2c_dataout1 0x3: Select gpio_104 0x7: Select safe_mode	RW	0x7
15	GPMC_NCS6_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	GPMC_NCS6_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	GPMC_NCS6_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad gpmc_ncs6 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
12	GPMC_NCS6_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad gpmc_ncs6 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	GPMC_NCS6_OFFMODEOUTVALUE	OffMode mode output value for pad gpmc_ncs6 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	GPMC_NCS6_OFFMODEOUTENABLE	OffMode mode output enable value for pad gpmc_ncs6. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	GPMC_NCS6_OFFMODEENABLE	OffMode mode override control for pad gpmc_ncs6 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	GPMC_NCS6_INPUTENABLE	Input enable value for pad gpmc_ncs6 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1

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Bits	Field Name	Description	Type	Reset
7:5	RESERVED		R	0x0
4	GPMC_NCS6_PULLTYPESELECT	pullup/down selection for pad gpmc_ncs6 0x0: pulldown selected 0x1: pullup selected	RW	0
3	GPMC_NCS6_PULLUDENABLE	pullup/down enable for pad gpmc_ncs6 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	GPMC_NCS6_MUXMODE	Functional multiplexing selection for pad gpmc_ncs6 0x0: Select gpmc_ncs6 0x1: Select dsi2_te0 0x2: Select c2c_dataout0 0x3: Select gpio_103 0x4: Select sys_ndmareq3 0x7: Select safe_mode	RW	0x7

Table 18-391. Register Call Summary for Register CONTROL_CORE_PAD0_GPMC_NCS6_PAD1_GPMC_NCS7

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- SYSCTRL_PADCONF_CORE Register Summary: [2]

Table 18-392. CONTROL_CORE_PAD0_GPIO63_PAD1_GPIO64

Address Offset	0x0000 0098		
Physical Address	0x4A10 0098	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads gpio63 and gpio64 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPIO64_WAKEUPEVENT	GPIO64_WAKEUPENABLE	GPIO64_OFFMODEPULLTYPESELECT	GPIO64_OFFMODEPULLUDENABLE	GPIO64_OFFMODEOUTVALUE	GPIO64_OFFMODEOUTENABLE	GPIO64_OFFMODEENABLE	GPIO64_INPUTENABLE	RESERVED			GPIO64_PULLTYPESELECT	GPIO64_PULLUDENABLE	GPIO64_MUXMODE			GPIO63_WAKEUPEVENT	GPIO63_WAKEUPENABLE	GPIO63_OFFMODEPULLTYPESELECT	GPIO63_OFFMODEPULLUDENABLE	GPIO63_OFFMODEOUTVALUE	GPIO63_OFFMODEOUTENABLE	GPIO63_OFFMODEENABLE	GPIO63_INPUTENABLE	RESERVED			GPIO63_PULLTYPESELECT	GPIO63_PULLUDENABLE	GPIO63_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	GPIO64_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0

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Bits	Field Name	Description	Type	Reset
30	GPIO64_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29	GPIO64_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad gpio64 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
28	GPIO64_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad gpio64 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	GPIO64_OFFMODEOUTVALUE	OffMode mode output value for pad gpio64 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	GPIO64_OFFMODEOUTENABLE	OffMode mode output enable value for pad gpio64. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	GPIO64_OFFMODEENABLE	OffMode mode override control for pad gpio64 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
24	GPIO64_INPUTENABLE	Input enable value for pad gpio64 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	GPIO64_PULLTYPESELECT	pullup/down selection for pad gpio64 0x0: pulldown selected 0x1: pullup selected	RW	1
19	GPIO64_PULLUDENABLE	pullup/down enable for pad gpio64 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	GPIO64_MUXMODE	Functional multiplexing selection for pad gpio64 0x0: Reserved 0x3: Select gpio_64 0x7: Select safe_mode	RW	0x7
15	GPIO63_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	GPIO63_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	GPIO63_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad gpio63 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
12	GPIO63_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad gpio63 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0

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Bits	Field Name	Description	Type	Reset
11	GPIO63_OFFMODEOUTVALUE	OffMode mode output value for pad gpio63 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	GPIO63_OFFMODEOUTENABLE	OffMode mode output enable value for pad gpio63. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	GPIO63_OFFMODEENABLE	OffMode mode override control for pad gpio63 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	GPIO63_INPUTENABLE	Input enable value for pad gpio63 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	GPIO63_PULLTYPESELECT	pullup/down selection for pad gpio63 0x0: pulldown selected 0x1: pullup selected	RW	0
3	GPIO63_PULLUDENABLE	pullup/down enable for pad gpio63 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	GPIO63_MUXMODE	Functional multiplexing selection for pad gpio63 0x0: Reserved 0x3: Select gpio_63 0x7: Select safe_mode	RW	0x7

Table 18-393. Register Call Summary for Register CONTROL_CORE_PAD0_GPIO63_PAD1_GPIO64

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- SYSCTRL_PADCONF_CORE Register Summary: [2]

Table 18-394. CONTROL_CORE_PAD0_GPIO65_PAD1_GPIO66

Address Offset	0x0000 009C		
Physical Address	0x4A10 009C	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads gpio65 and gpio66 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPIO66_WAKEUPEVENT	GPIO66_WAKEUPENABLE	GPIO66_OFFMODEPULLTYPESELECT	GPIO66_OFFMODEPULLUDENABLE	GPIO66_OFFMODEOUTVALUE	GPIO66_OFFMODEOUTENABLE	GPIO66_OFFMODEENABLE	GPIO66_INPUTENABLE	RESERVED			GPIO66_PULLTYPESELECT	GPIO66_PULLUDENABLE	GPIO66_MUXMODE			GPIO65_WAKEUPEVENT	GPIO65_WAKEUPENABLE	GPIO65_OFFMODEPULLTYPESELECT	GPIO65_OFFMODEPULLUDENABLE	GPIO65_OFFMODEOUTVALUE	GPIO65_OFFMODEOUTENABLE	GPIO65_OFFMODEENABLE	GPIO65_INPUTENABLE	RESERVED			GPIO65_PULLTYPESELECT	GPIO65_PULLUDENABLE	GPIO65_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	GPIO66_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	GPIO66_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29	GPIO66_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad gpio66 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
28	GPIO66_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad gpio66 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	GPIO66_OFFMODEOUTVALUE	OffMode mode output value for pad gpio66 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	GPIO66_OFFMODEOUTENABLE	OffMode mode output enable value for pad gpio66. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	GPIO66_OFFMODEENABLE	OffMode mode override control for pad gpio66 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
24	GPIO66_INPUTENABLE	Input enable value for pad gpio66 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	GPIO66_PULLTYPESELECT	pullup/down selection for pad gpio66 0x0: pulldown selected 0x1: pullup selected	RW	1
19	GPIO66_PULLUDENABLE	pullup/down enable for pad gpio66 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1

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Bits	Field Name	Description	Type	Reset
18:16	GPIO66_MUXMODE	Functional multiplexing selection for pad gpio66 0x0: Reserved 0x3: Select gpio_66 0x7: Select safe_mode	RW	0x7
15	GPIO65_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	GPIO65_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	GPIO65_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad gpio65 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
12	GPIO65_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad gpio65 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	GPIO65_OFFMODEOUTVALUE	OffMode mode output value for pad GPIO65 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	GPIO65_OFFMODEOUTENABLE	OffMode mode output enable value for pad gpio65. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	GPIO65_OFFMODEENABLE	OffMode mode override control for pad gpio65 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	GPIO65_INPUTENABLE	Input enable value for pad gpio65 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	GPIO65_PULLTYPESELECT	pullup/down selection for pad gpio65 0x0: pulldown selected 0x1: pullup selected	RW	1
3	GPIO65_PULLUDENABLE	pullup/down enable for pad gpio65 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	GPIO65_MUXMODE	Functional multiplexing selection for pad gpio65 0x0: Reserved 0x3: Select gpio_65 0x7: Select safe_mode	RW	0x7

Table 18-395. Register Call Summary for Register CONTROL_CORE_PAD0_GPIO65_PAD1_GPIO66

Control Module Functional Description • Pad Multiplexing Register Fields: [0] [1]
Control Module Register Manual • SYSCTRL_PADCONF_CORE Register Summary: [2]

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Table 18-396. CONTROL_CORE_PAD0_CSI21_DX0_PAD1_CSI21_DY0

Address Offset	0x0000 00A0		
Physical Address	0x4A10 00A0	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads csi21_dx0 and csi21_dy0 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CSI21_DY0_WAKEUPEVENT	CSI21_DY0_WAKEUPENABLE	RESERVED					CSI21_DY0_INPUTENABLE	RESERVED			CSI21_DY0_PULLTYPESELECT	CSI21_DY0_PULLUDENABLE	CSI21_DY0_MUXMODE			CSI21_DX0_WAKEUPEVENT	CSI21_DX0_WAKEUPENABLE	RESERVED					CSI21_DX0_INPUTENABLE	RESERVED			CSI21_DX0_PULLTYPESELECT	CSI21_DX0_PULLUDENABLE	CSI21_DX0_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	CSI21_DY0_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	CSI21_DY0_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x00
24	CSI21_DY0_INPUTENABLE	Input enable value for pad csi21_dy0 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	CSI21_DY0_PULLTYPESELECT	pullup/down selection for pad csi21_dy0 0x0: pulldown selected 0x1: pullup selected	RW	0
19	CSI21_DY0_PULLUDENABLE	pullup/down enable for pad csi21_dy0 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	CSI21_DY0_MUXMODE	Functional multiplexing selection for pad csi21_dy0 0x0: Select csi21_dy0 0x3: Select gpi_68 0x7: Select safe_mode	RW	0x7
15	CSI21_DX0_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	CSI21_DX0_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x00

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Bits	Field Name	Description	Type	Reset
8	CSI21_DX0_INPUTENABLE	Input enable value for pad csi21_dx0 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	CSI21_DX0_PULLTYPESELECT	pullup/down selection for pad csi21_dx0 0x0: pulldown selected 0x1: pullup selected	RW	0
3	CSI21_DX0_PULLUDENABLE	pullup/down enable for pad csi21_dx0 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	CSI21_DX0_MUXMODE	Functional multiplexing selection for pad csi21_dx0 0x0: Select csi21_dx0 0x3: Select gpi_67 0x7: Select safe_mode	RW	0x7

Table 18-397. Register Call Summary for Register CONTROL_CORE_PAD0_CSI21_DX0_PAD1_CSI21_DY0

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- SYSCTRL_PADCONF_CORE Register Summary: [2]

Table 18-398. CONTROL_CORE_PAD0_CSI21_DX1_PAD1_CSI21_DY1

Address Offset	0x0000 00A4		
Physical Address	0x4A10 00A4	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads csi21_dx1 and csi21_dy1 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CSI21_DY1_WAKEUPEVENT	CSI21_DY1_WAKEUPENABLE	RESERVED					CSI21_DY1_INPUTENABLE	RESERVED			CSI21_DY1_PULLTYPESELECT	CSI21_DY1_PULLUDENABLE	CSI21_DY1_MUXMODE			CSI21_DX1_WAKEUPEVENT	CSI21_DX1_WAKEUPENABLE	RESERVED				CSI21_DX1_INPUTENABLE	RESERVED			CSI21_DX1_PULLTYPESELECT	CSI21_DX1_PULLUDENABLE	CSI21_DX1_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	CSI21_DY1_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	CSI21_DY1_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x00

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Bits	Field Name	Description	Type	Reset
24	CSI21_DY1_INPUTENABLE	Input enable value for pad csi21_dy1 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	CSI21_DY1_PULLTYPESELECT	pullup/down selection for pad csi21_dy1 0x0: pulldown selected 0x1: pullup selected	RW	0
19	CSI21_DY1_PULLUDENABLE	pullup/down enable for pad csi21_dy1 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	CSI21_DY1_MUXMODE	Functional multiplexing selection for pad csi21_dy1 0x0: Select csi21_dy1 0x3: Select gpi_70 0x7: Select safe_mode	RW	0x7
15	CSI21_DX1_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	CSI21_DX1_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x00
8	CSI21_DX1_INPUTENABLE	Input enable value for pad csi21_dx1 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	CSI21_DX1_PULLTYPESELECT	pullup/down selection for pad csi21_dx1 0x0: pulldown selected 0x1: pullup selected	RW	0
3	CSI21_DX1_PULLUDENABLE	pullup/down enable for pad csi21_dx1 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	CSI21_DX1_MUXMODE	Functional multiplexing selection for pad csi21_dx1 0x0: Select csi21_dx1 0x3: Select gpi_69 0x7: Select safe_mode	RW	0x7

Table 18-399. Register Call Summary for Register CONTROL_CORE_PAD0_CSI21_DX1_PAD1_CSI21_DY1

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- SYSCTRL_PADCONF_CORE Register Summary: [2]

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Table 18-400. CONTROL_CORE_PAD0_CSI21_DX2_PAD1_CSI21_DY2

Address Offset	0x0000 00A8		
Physical Address	0x4A10 00A8	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads csi21_dx2 and csi21_dy2 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CSI21_DY2_WAKEUPEVENT	CSI21_DY2_WAKEUPENABLE	RESERVED					CSI21_DY2_INPUTENABLE	RESERVED			CSI21_DY2_PULLTYPESELECT	CSI21_DY2_PULLUDENABLE	CSI21_DY2_MUXMODE			CSI21_DX2_WAKEUPEVENT	CSI21_DX2_WAKEUPENABLE	RESERVED					CSI21_DX2_INPUTENABLE	RESERVED			CSI21_DX2_PULLTYPESELECT	CSI21_DX2_PULLUDENABLE	CSI21_DX2_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	CSI21_DY2_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	CSI21_DY2_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x00
24	CSI21_DY2_INPUTENABLE	Input enable value for pad csi21_dy2 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	CSI21_DY2_PULLTYPESELECT	pullup/down selection for pad csi21_dy2 0x0: pulldown selected 0x1: pullup selected	RW	0
19	CSI21_DY2_PULLUDENABLE	pullup/down enable for pad csi21_dy2 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	CSI21_DY2_MUXMODE	Functional multiplexing selection for pad csi21_dy2 0x0: Select csi21_dy2 0x3: Select gpi_72 0x7: Select safe_mode	RW	0x7
15	CSI21_DX2_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	CSI21_DX2_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x00

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Bits	Field Name	Description	Type	Reset
8	CSI21_DX2_INPUTENABLE	Input enable value for pad csi21_dx2 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	CSI21_DX2_PULLTYPESELECT	pullup/down selection for pad csi21_dx2 0x0: pulldown selected 0x1: pullup selected	RW	0
3	CSI21_DX2_PULLUDENABLE	pullup/down enable for pad csi21_dx2 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	CSI21_DX2_MUXMODE	Functional multiplexing selection for pad csi21_dx2 0x0: Select csi21_dx2 0x3: Select gpi_71 0x7: Select safe_mode	RW	0x7

Table 18-401. Register Call Summary for Register CONTROL_CORE_PAD0_CSI21_DX2_PAD1_CSI21_DY2

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- SYSCTRL_PADCONF_CORE Register Summary: [2]

Table 18-402. CONTROL_CORE_PAD0_CSI21_DX3_PAD1_CSI21_DY3

Address Offset	0x0000 00AC		
Physical Address	0x4A10 00AC	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads csi21_dx3 and csi21_dy3 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CSI21_DY3_WAKEUPEVENT	CSI21_DY3_WAKEUPENABLE	RESERVED					CSI21_DY3_INPUTENABLE	RESERVED			CSI21_DY3_PULLTYPESELECT	CSI21_DY3_PULLUDENABLE	CSI21_DY3_MUXMODE			CSI21_DX3_WAKEUPEVENT	CSI21_DX3_WAKEUPENABLE	RESERVED				CSI21_DX3_INPUTENABLE	RESERVED			CSI21_DX3_PULLTYPESELECT	CSI21_DX3_PULLUDENABLE	CSI21_DX3_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	CSI21_DY3_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	CSI21_DY3_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x00

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Bits	Field Name	Description	Type	Reset
24	CSI21_DY3_INPUTENABLE	Input enable value for pad csi21_dy3 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	CSI21_DY3_PULLTYPESELECT	pullup/down selection for pad csi21_dy3 0x0: pulldown selected 0x1: pullup selected	RW	0
19	CSI21_DY3_PULLUDENABLE	pullup/down enable for pad csi21_dy3 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	CSI21_DY3_MUXMODE	Functional multiplexing selection for pad csi21_dy3 0x0: Select csi21_dy3 0x1: Select cam2_d6 0x3: Select gpi_74 0x7: Select safe_mode	RW	0x7
15	CSI21_DX3_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	CSI21_DX3_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x00
8	CSI21_DX3_INPUTENABLE	Input enable value for pad csi21_dx3 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	CSI21_DX3_PULLTYPESELECT	pullup/down selection for pad csi21_dx3 0x0: pulldown selected 0x1: pullup selected	RW	0
3	CSI21_DX3_PULLUDENABLE	pullup/down enable for pad csi21_dx3 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	CSI21_DX3_MUXMODE	Functional multiplexing selection for pad csi21_dx3 0x0: Select csi21_dx3 0x1: Select cam2_d7 0x3: Select gpi_73 0x7: Select safe_mode	RW	0x7

Table 18-403. Register Call Summary for Register CONTROL_CORE_PAD0_CSI21_DX3_PAD1_CSI21_DY3

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- SYSCTRL_PADCONF_CORE Register Summary: [2]

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Table 18-404. CONTROL_CORE_PAD0_CSI21_DX4_PAD1_CSI21_DY4

Address Offset	0x0000 00B0		
Physical Address	0x4A10 00B0	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads csi21_dx4 and csi21_dy4 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CSI21_DY4_WAKEUPEVENT	CSI21_DY4_WAKEUPENABLE	RESERVED					CSI21_DY4_INPUTENABLE	RESERVED			CSI21_DY4_PULLTYPESELECT	CSI21_DY4_PULLUDENABLE	CSI21_DY4_MUXMODE			CSI21_DX4_WAKEUPEVENT	CSI21_DX4_WAKEUPENABLE	RESERVED					CSI21_DX4_INPUTENABLE	RESERVED					CSI21_DX4_PULLTYPESELECT	CSI21_DX4_PULLUDENABLE	CSI21_DX4_MUXMODE	

Bits	Field Name	Description	Type	Reset
31	CSI21_DY4_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	CSI21_DY4_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x00
24	CSI21_DY4_INPUTENABLE	Input enable value for pad csi21_dy4 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	CSI21_DY4_PULLTYPESELECT	pullup/down selection for pad csi21_dy4 0x0: pulldown selected 0x1: pullup selected	RW	0
19	CSI21_DY4_PULLUDENABLE	pullup/down enable for pad csi21_dy4 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	CSI21_DY4_MUXMODE	Functional multiplexing selection for pad csi21_dy4 0x0: Select csi21_dy4 0x1: Select cam2_d4 0x3: Select gpi_76 0x7: Select safe_mode	RW	0x7
15	CSI21_DX4_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	CSI21_DX4_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x00

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Bits	Field Name	Description	Type	Reset
8	CSI21_DX4_INPUTENABLE	Input enable value for pad csi21_dx4 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	CSI21_DX4_PULLTYPESELECT	pullup/down selection for pad csi21_dx4 0x0: pulldown selected 0x1: pullup selected	RW	0
3	CSI21_DX4_PULLUDENABLE	pullup/down enable for pad csi21_dx4 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	CSI21_DX4_MUXMODE	Functional multiplexing selection for pad csi21_dx4 0x0: Select csi21_dx4 0x1: Select cam2_d5 0x3: Select gpi_75 0x7: Select safe_mode	RW	0x7

Table 18-405. Register Call Summary for Register CONTROL_CORE_PAD0_CSI21_DX4_PAD1_CSI21_DY4

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- SYSCTRL_PADCONF_CORE Register Summary: [2]

Table 18-406. CONTROL_CORE_PAD0_CSI22_DX0_PAD1_CSI22_DY0

Address Offset	0x0000 00B4		
Physical Address	0x4A10 00B4	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads csi22_dx0 and csi22_dy0 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CSI22_DY0_WAKEUPEVENT	CSI22_DY0_WAKEUPENABLE	RESERVED					CSI22_DY0_INPUTENABLE	RESERVED			CSI22_DY0_PULLTYPESELECT	CSI22_DY0_PULLUDENABLE	CSI22_DY0_MUXMODE			CSI22_DX0_WAKEUPEVENT	CSI22_DX0_WAKEUPENABLE	RESERVED					CSI22_DX0_INPUTENABLE	RESERVED			CSI22_DX0_PULLTYPESELECT	CSI22_DX0_PULLUDENABLE	CSI22_DX0_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	CSI22_DY0_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	CSI22_DY0_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0

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Bits	Field Name	Description	Type	Reset
29:25	RESERVED		R	0x00
24	CSI22_DY0_INPUTENABLE	Input enable value for pad csi22_dy0 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	CSI22_DY0_PULLTYPESELECT	pullup/down selection for pad csi22_dy0 0x0: pulldown selected 0x1: pullup selected	RW	0
19	CSI22_DY0_PULLUDENABLE	pullup/down enable for pad csi22_dy0 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	CSI22_DY0_MUXMODE	Functional multiplexing selection for pad csi22_dy0 0x0: Select csi22_dy0 0x1: Select cam2_d2 0x2: Select cam2_d13 0x3: Select gpi_78 0x7: Select safe_mode	RW	0x7
15	CSI22_DX0_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	CSI22_DX0_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x00
8	CSI22_DX0_INPUTENABLE	Input enable value for pad csi22_dx0 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	CSI22_DX0_PULLTYPESELECT	pullup/down selection for pad csi22_dx0 0x0: pulldown selected 0x1: pullup selected	RW	0
3	CSI22_DX0_PULLUDENABLE	pullup/down enable for pad csi22_dx0 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	CSI22_DX0_MUXMODE	Functional multiplexing selection for pad csi22_dx0 0x0: Select csi22_dx0 0x1: Select cam2_d3 0x2: Select cam2_d12 0x3: Select gpi_77 0x7: Select safe_mode	RW	0x7

Table 18-407. Register Call Summary for Register CONTROL_CORE_PAD0_CSI22_DX0_PAD1_CSI22_DY0

Control Module Functional Description • Pad Multiplexing Register Fields: [0] [1]
Control Module Register Manual • SYSCTRL_PADCONF_CORE Register Summary: [2]

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Table 18-408. CONTROL_CORE_PAD0_CSI22_DX1_PAD1_CSI22_DY1

Address Offset	0x0000 00B8		
Physical Address	0x4A10 00B8	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads csi22_dx1 and csi22_dy1 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CSI22_DY1_WAKEUPEVENT	CSI22_DY1_WAKEUPENABLE	RESERVED					CSI22_DY1_INPUTENABLE	RESERVED			CSI22_DY1_PULLTYPESELECT	CSI22_DY1_PULLUDENABLE	CSI22_DY1_MUXMODE			CSI22_DX1_WAKEUPEVENT	CSI22_DX1_WAKEUPENABLE	RESERVED					CSI22_DX1_INPUTENABLE	RESERVED			CSI22_DX1_PULLTYPESELECT	CSI22_DX1_PULLUDENABLE	CSI22_DX1_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	CSI22_DY1_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	CSI22_DY1_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x00
24	CSI22_DY1_INPUTENABLE	Input enable value for pad csi22_dy1 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	CSI22_DY1_PULLTYPESELECT	pullup/down selection for pad csi22_dy1 0x0: pulldown selected 0x1: pullup selected	RW	0
19	CSI22_DY1_PULLUDENABLE	pullup/down enable for pad csi22_dy1 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	CSI22_DY1_MUXMODE	Functional multiplexing selection for pad csi22_dy1 0x0: Select csi22_dy1 0x1: Select cam2_d0 0x2: Select cam2_d15 0x3: Select gpi_80 0x7: Select safe_mode	RW	0x7
15	CSI22_DX1_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	CSI22_DX1_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0

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Bits	Field Name	Description	Type	Reset
13:9	RESERVED		R	0x00
8	CSI22_DX1_INPUTENABLE	Input enable value for pad csi22_dx1 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	CSI22_DX1_PULLTYPESELECT	pullup/down selection for pad csi22_dx1 0x0: pulldown selected 0x1: pullup selected	RW	0
3	CSI22_DX1_PULLUDENABLE	pullup/down enable for pad csi22_dx1 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	CSI22_DX1_MUXMODE	Functional multiplexing selection for pad csi22_dx1 0x0: Select csi22_dx1 0x1: Select cam2_d1 0x2: Select cam2_14 0x3: Select gpi_79 0x7: Select safe_mode	RW	0x7

Table 18-409. Register Call Summary for Register CONTROL_CORE_PAD0_CSI22_DX1_PAD1_CSI22_DY1

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- SYSCTRL_PADCONF_CORE Register Summary: [2]

Table 18-410. CONTROL_CORE_PAD0_CAM_SHUTTER_PAD1_CAM_STROBE

Address Offset	0x0000 00BC		
Physical Address	0x4A10 00BC	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads cam_shutter and cam_strobe Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAM_STROBE_WAKEUPEVENT	CAM_STROBE_WAKEUPENABLE	CAM_STROBE_OFFMODEPULLTYPESELECT	CAM_STROBE_OFFMODEPULLUDENABLE	CAM_STROBE_OFFMODEOUTVALUE	CAM_STROBE_OFFMODEOUTENABLE	CAM_STROBE_OFFMODEENABLE	CAM_STROBE_INPUTENABLE	RESERVED			CAM_STROBE_PULLTYPESELECT	CAM_STROBE_PULLUDENABLE	CAM_STROBE_MUXMODE			CAM_SHUTTER_WAKEUPEVENT	CAM_SHUTTER_WAKEUPENABLE	CAM_SHUTTER_OFFMODEPULLTYPESELECT	CAM_SHUTTER_OFFMODEPULLUDENABLE	CAM_SHUTTER_OFFMODEOUTVALUE	CAM_SHUTTER_OFFMODEOUTENABLE	CAM_SHUTTER_OFFMODEENABLE	CAM_SHUTTER_INPUTENABLE	RESERVED			CAM_SHUTTER_PULLTYPESELECT	CAM_SHUTTER_PULLUDENABLE	CAM_SHUTTER_MUXMODE		

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Bits	Field Name	Description	Type	Reset
31	CAM_STROBE_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	CAM_STROBE_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29	CAM_STROBE_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad cam_strobe 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
28	CAM_STROBE_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad cam_strobe 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	CAM_STROBE_OFFMODEOUTVALUE	OffMode mode output value for pad cam_strobe 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	CAM_STROBE_OFFMODEOUTENABLE	OffMode mode output enable value for pad cam_strobe. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	CAM_STROBE_OFFMODEENABLE	OffMode mode override control for pad cam_strobe 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
24	CAM_STROBE_INPUTENABLE	Input enable value for pad cam_strobe 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	CAM_STROBE_PULLTYPESELECT	pullup/down selection for pad cam_strobe 0x0: pulldown selected 0x1: pullup selected	RW	0
19	CAM_STROBE_PULLUDENABLE	pullup/down enable for pad cam_strobe 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	CAM_STROBE_MUXMODE	Functional multiplexing selection for pad cam_strobe 0x0: Select cam_strobe 0x2: Select cam2_vs 0x3: Select gpio_82 0x7: Select safe_mode	RW	0x7
15	CAM_SHUTTER_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	CAM_SHUTTER_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	CAM_SHUTTER_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad cam_shutter 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0

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Bits	Field Name	Description	Type	Reset
12	CAM_SHUTTER_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad cam_shutter 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	CAM_SHUTTER_ OFFMODEOUTVALUE	OffMode mode output value for pad cam_shutter 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	CAM_SHUTTER_ OFFMODEOUTENABLE	OffMode mode output enable value for pad cam_shutter. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	CAM_SHUTTER_ OFFMODEENABLE	OffMode mode override control for pad cam_shutter 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	CAM_SHUTTER_INPUTENABLE	Input enable value for pad cam_shutter 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	CAM_SHUTTER_ PULLTYPESELECT	pullup/down selection for pad cam_shutter 0x0: pulldown selected 0x1: pullup selected	RW	0
3	CAM_SHUTTER_ PULLUDENABLE	pullup/down enable for pad cam_shutter 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	CAM_SHUTTER_ MUXMODE	Functional multiplexing selection for pad cam_shutter 0x0: Select cam_shutter 0x2: Select cam2_hs 0x3: Select gpio_81 0x7: Select safe_mode	RW	0x7

Table 18-411. Register Call Summary for Register CONTROL_CORE_PAD0_CAM_SHUTTER_PAD1_CAM_STROBE

Control Module Functional Description • Pad Multiplexing Register Fields: [0] [1]
Control Module Register Manual • SYSCTRL_PADCONF_CORE Register Summary: [2]

Table 18-412. CONTROL_CORE_PAD0_CAM_GLOBALRESET_PAD1_USBB1_ULPITLL_CLK

Address Offset	0x0000 00C0		
Physical Address	0x4A10 00C0	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads cam_globalreset and usbb1_ulpitll_clk Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
USBB1_ULPITLL_CLK_WAKEUPEVENT	USBB1_ULPITLL_CLK_WAKEUPENABLE	USBB1_ULPITLL_CLK_OFFMODEPULLTYPESELECT	USBB1_ULPITLL_CLK_OFFMODEPULLUDENABLE	USBB1_ULPITLL_CLK_OFFMODEOUTVALUE	USBB1_ULPITLL_CLK_OFFMODEOUTENABLE	USBB1_ULPITLL_CLK_OFFMODEENABLE	USBB1_ULPITLL_CLK_INPUTENABLE	RESERVED			USBB1_ULPITLL_CLK_PULLTYPESELECT	USBB1_ULPITLL_CLK_PULLUDENABLE	USBB1_ULPITLL_CLK_MUXMODE			CAM_GLOBALRESET_WAKEUPEVENT	CAM_GLOBALRESET_WAKEUPENABLE	CAM_GLOBALRESET_OFFMODEPULLTYPESELECT	CAM_GLOBALRESET_OFFMODEPULLUDENABLE	CAM_GLOBALRESET_OFFMODEOUTVALUE	CAM_GLOBALRESET_OFFMODEOUTENABLE	CAM_GLOBALRESET_OFFMODEENABLE	CAM_GLOBALRESET_INPUTENABLE	RESERVED			CAM_GLOBALRESET_PULLTYPESELECT	CAM_GLOBALRESET_PULLUDENABLE	CAM_GLOBALRESET_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	USBB1_ULPITLL_CLK_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	USBB1_ULPITLL_CLK_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29	USBB1_ULPITLL_CLK_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad usbb1_ulpitll_clk 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
28	USBB1_ULPITLL_CLK_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad usbb1_ulpitll_clk 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	USBB1_ULPITLL_CLK_OFFMODEOUTVALUE	OffMode mode output value for pad usbb1_ulpitll_clk 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	USBB1_ULPITLL_CLK_OFFMODEOUTENABLE	OffMode mode output enable value for pad usbb1_ulpitll_clk. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	USBB1_ULPITLL_CLK_OFFMODEENABLE	OffMode mode override control for pad usbb1_ulpitll_clk 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
24	USBB1_ULPITLL_CLK_INPUTENABLE	Input enable value for pad usbb1_ulpitll_clk 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
20	USBB1_ULPITLL_CLK_PULLTYPESELECT	pullup/down selection for pad usbb1_ulpitll_clk 0x0: pulldown selected 0x1: pullup selected	RW	0
19	USBB1_ULPITLL_CLK_PULLUDENABLE	pullup/down enable for pad usbb1_ulpitll_clk 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	USBB1_ULPITLL_CLK_MUXMODE	Functional multiplexing selection for pad usbb1_ulpitll_clk 0x0: Select usbb1_ulpitll_clk 0x1: Select hsi1_cawake 0x3: Select gpio_84 0x4: Select usbb1_ulpiphy_clk 0x6: Select hw_dbg20 0x7: Select safe_mode	RW	0x7
15	CAM_GLOBALRESET_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	CAM_GLOBALRESET_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	CAM_GLOBALRESET_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad cam_globalreset 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
12	CAM_GLOBALRESET_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad cam_globalreset 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	CAM_GLOBALRESET_OFFMODEOUTVALUE	OffMode mode output value for pad cam_globalreset 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	CAM_GLOBALRESET_OFFMODEOUTENABLE	OffMode mode output enable value for pad cam_globalreset. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	CAM_GLOBALRESET_OFFMODEENABLE	OffMode mode override control for pad cam_globalreset 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	CAM_GLOBALRESET_INPUTENABLE	Input enable value for pad cam_globalreset 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	CAM_GLOBALRESET_PULLTYPESELECT	pullup/down selection for pad cam_globalreset 0x0: pulldown selected 0x1: pullup selected	RW	0
3	CAM_GLOBALRESET_PULLUDENABLE	pullup/down enable for pad cam_globalreset 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1

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Bits	Field Name	Description	Type	Reset
2:0	CAM_GLOBALRESET_ MUXMODE	Functional multiplexing selection for pad cam_globalreset 0x0: Select cam_globalreset 0x2: Select cam2_pclk 0x3: Select gpio_83 0x7: Select safe_mode	RW	0x7

Table 18-413. Register Call Summary for Register CONTROL_CORE_PAD0_CAM_GLOBALRESET_PAD1_USBB1_ULPITLL_CLK

Control Module Functional Description

- Pad Multiplexing Register Fields: [0] [1]
- Observability Signals Multiplexing at Device Control Module Level: [2]

Control Module Register Manual

- SYSCTRL_PADCONF_CORE Register Summary: [3]

Table 18-414. CONTROL_CORE_PAD0_USBB1_ULPITLL_STP_PAD1_USBB1_ULPITLL_DIR

Address Offset	0x0000 00C4		
Physical Address	0x4A10 00C4	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads usbb1_ulpitll_stp and usbb1_ulpitll_dir Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
USBB1_ULPITLL_DIR_WAKEUPEVENT	USBB1_ULPITLL_DIR_WAKEUPENABLE	USBB1_ULPITLL_DIR_OFFMODEPULLTYPESELECT	USBB1_ULPITLL_DIR_OFFMODEPULLUDENABLE	USBB1_ULPITLL_DIR_OFFMODEOUTVALUE	USBB1_ULPITLL_DIR_OFFMODEOUTENABLE	USBB1_ULPITLL_DIR_OFFMODEENABLE	USBB1_ULPITLL_DIR_INPUTENABLE	RESERVED			USBB1_ULPITLL_DIR_PULLTYPESELECT	USBB1_ULPITLL_DIR_PULLUDENABLE	USBB1_ULPITLL_DIR_MUXMODE			USBB1_ULPITLL_STP_WAKEUPEVENT	USBB1_ULPITLL_STP_WAKEUPENABLE	USBB1_ULPITLL_STP_OFFMODEPULLTYPESELECT	USBB1_ULPITLL_STP_OFFMODEPULLUDENABLE	USBB1_ULPITLL_STP_OFFMODEOUTVALUE	USBB1_ULPITLL_STP_OFFMODEOUTENABLE	USBB1_ULPITLL_STP_OFFMODEENABLE	USBB1_ULPITLL_STP_INPUTENABLE	RESERVED			USBB1_ULPITLL_STP_PULLTYPESELECT	USBB1_ULPITLL_STP_PULLUDENABLE	USBB1_ULPITLL_STP_MUXMODE	

Bits	Field Name	Description	Type	Reset
31	USBB1_ULPITLL_ DIR_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	USBB1_ULPITLL_ DIR_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0

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Bits	Field Name	Description	Type	Reset
29	USBB1_ULPITLL_DIR_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad usbb1_ulpitll_dir 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
28	USBB1_ULPITLL_DIR_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad usbb1_ulpitll_dir 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	USBB1_ULPITLL_DIR_OFFMODEOUTVALUE	OffMode mode output value for pad usbb1_ulpitll_dir 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	USBB1_ULPITLL_DIR_OFFMODEOUTENABLE	OffMode mode output enable value for pad usbb1_ulpitll_dir. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	USBB1_ULPITLL_DIR_OFFMODEENABLE	OffMode mode override control for pad usbb1_ulpitll_dir 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
24	USBB1_ULPITLL_DIR_INPUTENABLE	Input enable value for pad usbb1_ulpitll_dir 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	USBB1_ULPITLL_DIR_PULLTYPESELECT	pullup/down selection for pad usbb1_ulpitll_dir 0x0: pulldown selected 0x1: pullup selected	RW	0
19	USBB1_ULPITLL_DIR_PULLUDENABLE	pullup/down enable for pad usbb1_ulpitll_dir 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	USBB1_ULPITLL_DIR_MUXMODE	Functional multiplexing selection for pad usbb1_ulpitll_dir 0x0: Select usbb1_ulpitll_dir 0x1: Select hsi1_caflag 0x2: Select mcbsp4_fsr 0x3: Select gpio_86 0x4: Select usbb1_ulpiphy_dir 0x6: Select hw_dbg22 0x7: Select safe_mode	RW	0x7
15	USBB1_ULPITLL_STP_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	USBB1_ULPITLL_STP_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	USBB1_ULPITLL_STP_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad usbb1_ulpitll_stp 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0

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Bits	Field Name	Description	Type	Reset
12	USBB1_ULPITLL_STP_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad usbb1_ulpitll_stp 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	USBB1_ULPITLL_STP_OFFMODEOUTVALUE	OffMode mode output value for pad usbb1_ulpitll_stp 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	USBB1_ULPITLL_STP_OFFMODEOUTENABLE	OffMode mode output enable value for pad usbb1_ulpitll_stp. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	USBB1_ULPITLL_STP_OFFMODEENABLE	OffMode mode override control for pad usbb1_ulpitll_stp 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	USBB1_ULPITLL_STP_INPUTENABLE	Input enable value for pad usbb1_ulpitll_stp 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	USBB1_ULPITLL_STP_PULLTYPESELECT	pullup/down selection for pad usbb1_ulpitll_stp 0x0: pulldown selected 0x1: pullup selected	RW	1
3	USBB1_ULPITLL_STP_PULLUDENABLE	pullup/down enable for pad usbb1_ulpitll_stp 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	USBB1_ULPITLL_STP_MUXMODE	Functional multiplexing selection for pad usbb1_ulpitll_stp 0x0: Select usbb1_ulpitll_stp 0x1: Select hsi1_cadata 0x2: Select mcbsp4_clkr 0x3: Select gpio_85 0x4: Select usbb1_ulpiphy_stp 0x5: Select usbb1_mm_rxdp 0x6: Select hw_dbg21 0x7: Select safe_mode	RW	0x7

Table 18-415. Register Call Summary for Register CONTROL_CORE_PAD0_USBB1_ULPITLL_STP_PAD1_USBB1_ULPITLL_DIR

Control Module Functional Description • Pad Multiplexing Register Fields: [0] [1]
Control Module Register Manual • SYSCTRL_PADCONF_CORE Register Summary: [2]

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Table 18-416. CONTROL_CORE_PAD0_USBB1_ULPITLL_NXT_PAD1_USBB1_ULPITLL_DAT0

Address Offset	0x0000 00C8		
Physical Address	0x4A10 00C8	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads usbb1_ulpitll_nxt and usbb1_ulpitll_dat0 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
USBB1_ULPITLL_DAT0_WAKEUPEVENT	USBB1_ULPITLL_DAT0_WAKEUPENABLE	USBB1_ULPITLL_DAT0_OFFMODEPULLTYPESELECT	USBB1_ULPITLL_DAT0_OFFMODEPULLUDENABLE	USBB1_ULPITLL_DAT0_OFFMODEOUTVALUE	USBB1_ULPITLL_DAT0_OFFMODEOUTENABLE	USBB1_ULPITLL_DAT0_OFFMODEENABLE	USBB1_ULPITLL_DAT0_INPUTENABLE	RESERVED			USBB1_ULPITLL_DAT0_PULLTYPESELECT	USBB1_ULPITLL_DAT0_PULLUDENABLE	USBB1_ULPITLL_DAT0_MUXMODE			USBB1_ULPITLL_NXT_WAKEUPEVENT	USBB1_ULPITLL_NXT_WAKEUPENABLE	USBB1_ULPITLL_NXT_OFFMODEPULLTYPESELECT	USBB1_ULPITLL_NXT_OFFMODEPULLUDENABLE	USBB1_ULPITLL_NXT_OFFMODEOUTVALUE	USBB1_ULPITLL_NXT_OFFMODEOUTENABLE	USBB1_ULPITLL_NXT_OFFMODEENABLE	USBB1_ULPITLL_NXT_INPUTENABLE	RESERVED			USBB1_ULPITLL_NXT_PULLTYPESELECT	USBB1_ULPITLL_NXT_PULLUDENABLE	USBB1_ULPITLL_NXT_MUXMODE	

Bits	Field Name	Description	Type	Reset
31	USBB1_ULPITLL_DAT0_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	USBB1_ULPITLL_DAT0_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29	USBB1_ULPITLL_DAT0_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad usbb1_ulpitll_dat0 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
28	USBB1_ULPITLL_DAT0_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad usbb1_ulpitll_dat0 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	USBB1_ULPITLL_DAT0_OFFMODEOUTVALUE	OffMode mode output value for pad usbb1_ulpitll_dat0 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	USBB1_ULPITLL_DAT0_OFFMODEOUTENABLE	OffMode mode output enable value for pad usbb1_ulpitll_dat0. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0

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Bits	Field Name	Description	Type	Reset
25	USBB1_ULPITLL_ DAT0_OFFMODEENABLE	OffMode mode override control for pad usbb1_ulpitll_dat0 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
24	USBB1_ULPITLL_ DAT0_INPUTENABLE	Input enable value for pad usbb1_ulpitll_dat0 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	USBB1_ULPITLL_ DAT0_PULLTYPESELECT	pullup/down selection for pad usbb1_ulpitll_dat0 0x0: pulldown selected 0x1: pullup selected	RW	0
19	USBB1_ULPITLL_ DAT0_PULLUDENABLE	pullup/down enable for pad usbb1_ulpitll_dat0 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	USBB1_ULPITLL_ DAT0_MUXMODE	Functional multiplexing selection for pad usbb1_ulpitll_dat0 0x0: Select usbb1_ulpitll_dat0 0x1: Select hsi1_acwake 0x2: Select mcbsp4_clkx 0x3: Select gpio_88 0x4: Select usbb1_ulpiphy_dat0 0x5: Select usbb1_mm_txen 0x6: Select hw_dbg24 0x7: Select safe_mode	RW	0x7
15	USBB1_ULPITLL_ NXT_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	USBB1_ULPITLL_ NXT_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	USBB1_ULPITLL_ NXT_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad usbb1_ulpitll_nxt 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
12	USBB1_ULPITLL_ NXT_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad usbb1_ulpitll_nxt 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	USBB1_ULPITLL_ NXT_OFFMODEOUTVALUE	OffMode mode output value for pad usbb1_ulpitll_nxt 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	USBB1_ULPITLL_ NXT_OFFMODEOUTENABLE	OffMode mode output enable value for pad usbb1_ulpitll_nxt. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	USBB1_ULPITLL_ NXT_OFFMODEENABLE	OffMode mode override control for pad usbb1_ulpitll_nxt 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0

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Bits	Field Name	Description	Type	Reset
8	USBB1_ULPITLL_ NXT_INPUTENABLE	Input enable value for pad usbb1_ulpitll_nxt 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	USBB1_ULPITLL_ NXT_PULLTYPESELECT	pullup/down selection for pad usbb1_ulpitll_nxt 0x0: pulldown selected 0x1: pullup selected	RW	0
3	USBB1_ULPITLL_ NXT_PULLUDENABLE	pullup/down enable for pad usbb1_ulpitll_nxt 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	USBB1_ULPITLL_ NXT_MUXMODE	Functional multiplexing selection for pad usbb1_ulpitll_nxt 0x0: Select usbb1_ulpitll_nxt 0x1: Select hsi1_acready 0x2: Select mcbsp4_fsx 0x3: Select gpio_87 0x4: Select usbb1_ulpiphy_nxt 0x5: Select usbb1_mm_rxdm 0x6: Select hw_dbg23 0x7: Select safe_mode	RW	0x7

Table 18-417. Register Call Summary for Register CONTROL_CORE_PAD0_USBB1_ULPITLL_NXT_PAD1_USBB1_ULPITLL_DAT0

Control Module Functional Description • Pad Multiplexing Register Fields: [0] [1]
Control Module Register Manual • SYSCTRL_PADCONF_CORE Register Summary: [2]

Table 18-418. CONTROL_CORE_PAD0_USBB1_ULPITLL_DAT1_PAD1_USBB1_ULPITLL_DAT2

Address Offset	0x0000 00CC		
Physical Address	0x4A10 00CC	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads usbb1_ulpitll_dat1 and usbb1_ulpitll_dat2 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
USBB1_ULPITLL_DAT2_WAKEUPEVENT	USBB1_ULPITLL_DAT2_WAKEUPENABLE	USBB1_ULPITLL_DAT2_OFFMODEPULLTYPESELECT	USBB1_ULPITLL_DAT2_OFFMODEPULLUDENABLE	USBB1_ULPITLL_DAT2_OFFMODEOUTVALUE	USBB1_ULPITLL_DAT2_OFFMODEOUTENABLE	USBB1_ULPITLL_DAT2_OFFMODEENABLE	USBB1_ULPITLL_DAT2_INPUTENABLE	RESERVED			USBB1_ULPITLL_DAT2_PULLTYPESELECT	USBB1_ULPITLL_DAT2_PULLUDENABLE	USBB1_ULPITLL_DAT2_MUXMODE			USBB1_ULPITLL_DAT1_WAKEUPEVENT	USBB1_ULPITLL_DAT1_WAKEUPENABLE	USBB1_ULPITLL_DAT1_OFFMODEPULLTYPESELECT	USBB1_ULPITLL_DAT1_OFFMODEPULLUDENABLE	USBB1_ULPITLL_DAT1_OFFMODEOUTVALUE	USBB1_ULPITLL_DAT1_OFFMODEOUTENABLE	USBB1_ULPITLL_DAT1_OFFMODEENABLE	USBB1_ULPITLL_DAT1_INPUTENABLE	RESERVED			USBB1_ULPITLL_DAT1_PULLTYPESELECT	USBB1_ULPITLL_DAT1_PULLUDENABLE	USBB1_ULPITLL_DAT1_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	USBB1_ULPITLL_DAT2_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	USBB1_ULPITLL_DAT2_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29	USBB1_ULPITLL_DAT2_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad usbb1_ulpitll_dat2 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
28	USBB1_ULPITLL_DAT2_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad usbb1_ulpitll_dat2 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	USBB1_ULPITLL_DAT2_OFFMODEOUTVALUE	OffMode mode output value for pad usbb1_ulpitll_dat2 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	USBB1_ULPITLL_DAT2_OFFMODEOUTENABLE	OffMode mode output enable value for pad usbb1_ulpitll_dat2. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	USBB1_ULPITLL_DAT2_OFFMODEENABLE	OffMode mode override control for pad usbb1_ulpitll_dat2 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
24	USBB1_ULPITLL_DAT2_INPUTENABLE	Input enable value for pad usbb1_ulpitll_dat2 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
20	USBB1_ULPITLL_DAT2_PULLTYPESELECT	pullup/down selection for pad usbb1_ulpitll_dat2 0x0: pulldown selected 0x1: pullup selected	RW	0
19	USBB1_ULPITLL_DAT2_PULLUDENABLE	pullup/down enable for pad usbb1_ulpitll_dat2 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	USBB1_ULPITLL_DAT2_MUXMODE	Functional multiplexing selection for pad usbb1_ulpitll_dat2 0x0: Select usbb1_ulpitll_dat2 0x1: Select hsi1_acflag 0x2: Select mcbsp4_dr 0x3: Select gpio_90 0x4: Select usbb1_ulpiphy_dat2 0x5: Select usbb1_mm_txse0 0x6: Select hw_dbg26 0x7: Select safe_mode	RW	0x7
15	USBB1_ULPITLL_DAT1_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	USBB1_ULPITLL_DAT1_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	USBB1_ULPITLL_DAT1_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad usbb1_ulpitll_dat1 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
12	USBB1_ULPITLL_DAT1_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad usbb1_ulpitll_dat1 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	USBB1_ULPITLL_DAT1_OFFMODEOUTVALUE	OffMode mode output value for pad usbb1_ulpitll_dat1 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	USBB1_ULPITLL_DAT1_OFFMODEOUTENABLE	OffMode mode output enable value for pad usbb1_ulpitll_dat1. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	USBB1_ULPITLL_DAT1_OFFMODEENABLE	OffMode mode override control for pad usbb1_ulpitll_dat1 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	USBB1_ULPITLL_DAT1_INPUTENABLE	Input enable value for pad usbb1_ulpitll_dat1 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	USBB1_ULPITLL_DAT1_PULLTYPESELECT	pullup/down selection for pad usbb1_ulpitll_dat1 0x0: pulldown selected 0x1: pullup selected	RW	0

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Bits	Field Name	Description	Type	Reset
3	USBB1_ULPITLL_DAT1_PULLUDENABLE	pullup/down enable for pad usbb1_ulpitll_dat1 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	USBB1_ULPITLL_DAT1_MUXMODE	Functional multiplexing selection for pad usbb1_ulpitll_dat1 0x0: Select usbb1_ulpitll_dat1 0x1: Select hsi1_acdata 0x2: Select mcbsp4_dx 0x3: Select gpio_89 0x4: Select usbb1_ulpiphy_dat1 0x5: Select usbb1_mm_txdat 0x6: Select hw_dbg25 0x7: Select safe_mode	RW	0x7

Table 18-419. Register Call Summary for Register CONTROL_CORE_PAD0_USBB1_ULPITLL_DAT1_PAD1_USBB1_ULPITLL_DAT2

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- SYSCTRL_PADCONF_CORE Register Summary: [2]

Table 18-420. CONTROL_CORE_PAD0_USBB1_ULPITLL_DAT3_PAD1_USBB1_ULPITLL_DAT4

Address Offset	0x0000 00D0		
Physical Address	0x4A10 00D0	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads usbb1_ulpitll_dat3 and usbb1_ulpitll_dat4 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
USBB1_ULPITLL_DAT4_WAKEUPEVENT	USBB1_ULPITLL_DAT4_WAKEUPENABLE	USBB1_ULPITLL_DAT4_OFFMODEPULLTYPESELECT	USBB1_ULPITLL_DAT4_OFFMODEPULLUDENABLE	USBB1_ULPITLL_DAT4_OFFMODEOUTVALUE	USBB1_ULPITLL_DAT4_OFFMODEOUTENABLE	USBB1_ULPITLL_DAT4_OFFMODEENABLE	USBB1_ULPITLL_DAT4_INPUTENABLE	RESERVED			USBB1_ULPITLL_DAT4_PULLTYPESELECT	USBB1_ULPITLL_DAT4_PULLUDENABLE	USBB1_ULPITLL_DAT4_MUXMODE			USBB1_ULPITLL_DAT3_WAKEUPEVENT	USBB1_ULPITLL_DAT3_WAKEUPENABLE	USBB1_ULPITLL_DAT3_OFFMODEPULLTYPESELECT	USBB1_ULPITLL_DAT3_OFFMODEPULLUDENABLE	USBB1_ULPITLL_DAT3_OFFMODEOUTVALUE	USBB1_ULPITLL_DAT3_OFFMODEOUTENABLE	USBB1_ULPITLL_DAT3_OFFMODEENABLE	USBB1_ULPITLL_DAT3_INPUTENABLE	RESERVED			USBB1_ULPITLL_DAT3_PULLTYPESELECT	USBB1_ULPITLL_DAT3_PULLUDENABLE	USBB1_ULPITLL_DAT3_MUXMODE	

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Bits	Field Name	Description	Type	Reset
31	USBB1_ULPITLL_DAT4_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	USBB1_ULPITLL_DAT4_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29	USBB1_ULPITLL_DAT4_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad usbb1_ulpitll_dat4 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
28	USBB1_ULPITLL_DAT4_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad usbb1_ulpitll_dat4 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	USBB1_ULPITLL_DAT4_OFFMODEOUTVALUE	OffMode mode output value for pad usbb1_ulpitll_dat4 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	USBB1_ULPITLL_DAT4_OFFMODEOUTENABLE	OffMode mode output enable value for pad usbb1_ulpitll_dat4. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	USBB1_ULPITLL_DAT4_OFFMODEENABLE	OffMode mode override control for pad usbb1_ulpitll_dat4 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
24	USBB1_ULPITLL_DAT4_INPUTENABLE	Input enable value for pad usbb1_ulpitll_dat4 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	USBB1_ULPITLL_DAT4_PULLTYPESELECT	pullup/down selection for pad usbb1_ulpitll_dat4 0x0: pulldown selected 0x1: pullup selected	RW	0
19	USBB1_ULPITLL_DAT4_PULLUDENABLE	pullup/down enable for pad usbb1_ulpitll_dat4 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	USBB1_ULPITLL_DAT4_MUXMODE	Functional multiplexing selection for pad usbb1_ulpitll_dat4 0x0: Select usbb1_ulpitll_dat4 0x1: Select dmtimer8_pwm_evt 0x2: Select abe_mcbsp3_dr 0x3: Select gpio_92 0x4: Select usbb1_ulpiphy_dat4 0x6: Select hw_dbg28 0x7: Select safe_mode	RW	0x7
15	USBB1_ULPITLL_DAT3_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0

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Bits	Field Name	Description	Type	Reset
14	USBB1_ULPITLL_ DAT3_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	USBB1_ULPITLL_ DAT3_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad usbb1_ulpitll_dat3 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
12	USBB1_ULPITLL_ DAT3_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad usbb1_ulpitll_dat3 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	USBB1_ULPITLL_ DAT3_OFFMODEOUTVALUE	OffMode mode output value for pad usbb1_ulpitll_dat3 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	USBB1_ULPITLL_ DAT3_OFFMODEOUTENABLE	OffMode mode output enable value for pad usbb1_ulpitll_dat3. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	USBB1_ULPITLL_ DAT3_OFFMODEENABLE	OffMode mode override control for pad usbb1_ulpitll_dat3 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	USBB1_ULPITLL_ DAT3_INPUTENABLE	Input enable value for pad usbb1_ulpitll_dat3 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	USBB1_ULPITLL_ DAT3_PULLTYPESELECT	pullup/down selection for pad usbb1_ulpitll_dat3 0x0: pulldown selected 0x1: pullup selected	RW	0
3	USBB1_ULPITLL_ DAT3_PULLUDENABLE	pullup/down enable for pad usbb1_ulpitll_dat3 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	USBB1_ULPITLL_ DAT3_MUXMODE	Functional multiplexing selection for pad usbb1_ulpitll_dat3 0x0: Select usbb1_ulpitll_dat3 0x1: Select hsi1_caready 0x3: Select gpio_91 0x4: Select usbb1_ulpiphy_dat3 0x5: Select usbb1_mm_rxrcv 0x6: Select hw_dbg27 0x7: Select safe_mode	RW	0x7

Table 18-421. Register Call Summary for Register CONTROL_CORE_PAD0_USBB1_ULPITLL_DAT3_PAD1_USBB1_ULPITLL_DAT4

Control Module Functional Description

- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual

- SYSCTRL_PADCONF_CORE Register Summary: [2]

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Table 18-422. CONTROL_CORE_PAD0_USBB1_ULPITLL_DAT5_PAD1_USBB1_ULPITLL_DAT6

Address Offset	0x0000 00D4		
Physical Address	0x4A10 00D4	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads usbb1_ulpitll_dat5 and usbb1_ulpitll_dat6 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
USBB1_ULPITLL_DAT6_WAKEUPEVENT	USBB1_ULPITLL_DAT6_WAKEUPENABLE	USBB1_ULPITLL_DAT6_OFFMODEPULLTYPESELECT	USBB1_ULPITLL_DAT6_OFFMODEPULLUDENABLE	USBB1_ULPITLL_DAT6_OFFMODEOUTVALUE	USBB1_ULPITLL_DAT6_OFFMODEOUTENABLE	USBB1_ULPITLL_DAT6_OFFMODEENABLE	USBB1_ULPITLL_DAT6_INPUTENABLE	RESERVED			USBB1_ULPITLL_DAT6_PULLTYPESELECT	USBB1_ULPITLL_DAT6_PULLUDENABLE	USBB1_ULPITLL_DAT6_MUXMODE			USBB1_ULPITLL_DAT5_WAKEUPEVENT	USBB1_ULPITLL_DAT5_WAKEUPENABLE	USBB1_ULPITLL_DAT5_OFFMODEPULLTYPESELECT	USBB1_ULPITLL_DAT5_OFFMODEPULLUDENABLE	USBB1_ULPITLL_DAT5_OFFMODEOUTVALUE	USBB1_ULPITLL_DAT5_OFFMODEOUTENABLE	USBB1_ULPITLL_DAT5_OFFMODEENABLE	USBB1_ULPITLL_DAT5_INPUTENABLE	RESERVED			USBB1_ULPITLL_DAT5_PULLTYPESELECT	USBB1_ULPITLL_DAT5_PULLUDENABLE	USBB1_ULPITLL_DAT5_MUXMODE	

Bits	Field Name	Description	Type	Reset
31	USBB1_ULPITLL_DAT6_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	USBB1_ULPITLL_DAT6_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29	USBB1_ULPITLL_DAT6_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad usbb1_ulpitll_dat6 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
28	USBB1_ULPITLL_DAT6_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad usbb1_ulpitll_dat6 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	USBB1_ULPITLL_DAT6_OFFMODEOUTVALUE	OffMode mode output value for pad usbb1_ulpitll_dat6 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	USBB1_ULPITLL_DAT6_OFFMODEOUTENABLE	OffMode mode output enable value for pad usbb1_ulpitll_dat6. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0

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Bits	Field Name	Description	Type	Reset
25	USBB1_ULPITLL_DAT6_OFFMODEENABLE	OffMode mode override control for pad usbb1_ulpitll_dat6 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
24	USBB1_ULPITLL_DAT6_INPUTENABLE	Input enable value for pad usbb1_ulpitll_dat6 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	USBB1_ULPITLL_DAT6_PULLTYPESELECT	pullup/down selection for pad usbb1_ulpitll_dat6 0x0: pulldown selected 0x1: pullup selected	RW	0
19	USBB1_ULPITLL_DAT6_PULLUDENABLE	pullup/down enable for pad usbb1_ulpitll_dat6 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	USBB1_ULPITLL_DAT6_MUXMODE	Functional multiplexing selection for pad usbb1_ulpitll_dat6 0x0: Select usbb1_ulpitll_dat6 0x1: Select dmtimer10_pwm_evt 0x2: Select abe_mcbsp3_clkx 0x3: Select gpio_94 0x4: Select usbb1_ulpiphy_dat6 0x5: Select abe_dmic_din3 0x6: Select hw_dbg30 0x7: Select safe_mode	RW	0x7
15	USBB1_ULPITLL_DAT5_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	USBB1_ULPITLL_DAT5_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	USBB1_ULPITLL_DAT5_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad usbb1_ulpitll_dat5 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
12	USBB1_ULPITLL_DAT5_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad usbb1_ulpitll_dat5 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	USBB1_ULPITLL_DAT5_OFFMODEOUTVALUE	OffMode mode output value for pad usbb1_ulpitll_dat5 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	USBB1_ULPITLL_DAT5_OFFMODEOUTENABLE	OffMode mode output enable value for pad usbb1_ulpitll_dat5. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	USBB1_ULPITLL_DAT5_OFFMODEENABLE	OffMode mode override control for pad usbb1_ulpitll_dat5 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0

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Bits	Field Name	Description	Type	Reset
8	USBB1_ULPITLL_DAT5_INPUTENABLE	Input enable value for pad usbb1_ulpitll_dat5 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	USBB1_ULPITLL_DAT5_PULLTYPESELECT	pullup/down selection for pad usbb1_ulpitll_dat5 0x0: pulldown selected 0x1: pullup selected	RW	0
3	USBB1_ULPITLL_DAT5_PULLUDENABLE	pullup/down enable for pad usbb1_ulpitll_dat5 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	USBB1_ULPITLL_DAT5_MUXMODE	Functional multiplexing selection for pad usbb1_ulpitll_dat5 0x0: Select usbb1_ulpitll_dat5 0x1: Select dmtimer9_pwm_evt 0x2: Select abe_mcbsp3_dx 0x3: Select gpio_93 0x4: Select usbb1_ulpiphy_dat5 0x6: Select hw_dbg29 0x7: Select safe_mode	RW	0x7

Table 18-423. Register Call Summary for Register CONTROL_CORE_PAD0_USBB1_ULPITLL_DAT5_PAD1_USBB1_ULPITLL_DAT6

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- SYSCTRL_PADCONF_CORE Register Summary: [2]

Table 18-424. CONTROL_CORE_PAD0_USBB1_ULPITLL_DAT7_PAD1_USBB1_HSIC_DATA

Address Offset	0x0000 00D8		
Physical Address	0x4A10 00D8	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads usbb1_ulpitll_dat7 and usbb1_hsic_data Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
USBB1_HSIC_DATA_WAKEUPEVENT	USBB1_HSIC_DATA_WAKEUPENABLE	RESERVED		USBB1_HSIC_DATA_OFFMODEOUTVALUE	USBB1_HSIC_DATA_OFFMODEOUTENABLE	USBB1_HSIC_DATA_OFFMODEENABLE	RESERVED						USBB1_HSIC_DATA_MUXMODE			USBB1_ULPITLL_DAT7_WAKEUPEVENT	USBB1_ULPITLL_DAT7_WAKEUPENABLE	USBB1_ULPITLL_DAT7_OFFMODEPULLTYPESELECT	USBB1_ULPITLL_DAT7_OFFMODEPULLUDENABLE	USBB1_ULPITLL_DAT7_OFFMODEOUTVALUE	USBB1_ULPITLL_DAT7_OFFMODEOUTENABLE	USBB1_ULPITLL_DAT7_OFFMODEENABLE	USBB1_ULPITLL_DAT7_INPUTENABLE	RESERVED			USBB1_ULPITLL_DAT7_PULLTYPESELECT	USBB1_ULPITLL_DAT7_PULLUDENABLE	USBB1_ULPITLL_DAT7_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	USBB1_HSIC_DATA_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	USBB1_HSIC_DATA_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:28	RESERVED		R	0x0
27	USBB1_HSIC_DATA_OFFMODEOUTVALUE	OffMode mode output value for pad usbb1_hsic_data 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	USBB1_HSIC_DATA_OFFMODEOUTENABLE	OffMode mode output enable value for pad usbb1_hsic_data. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	USBB1_HSIC_DATA_OFFMODEENABLE	OffMode mode override control for pad usbb1_hsic_data 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
24:19	RESERVED		R	0x00
18:16	USBB1_HSIC_DATA_MUXMODE	Functional multiplexing selection for pad usbb1_hsic_data 0x0: Select usbb1_hsic_data 0x3: Select gpio_96 0x7: Select safe_mode	RW	0x7
15	USBB1_ULPITLL_DAT7_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	USBB1_ULPITLL_DAT7_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0

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Bits	Field Name	Description	Type	Reset
13	USBB1_ULPITLL_DAT7_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad usbb1_ulpitll_dat7 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
12	USBB1_ULPITLL_DAT7_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad usbb1_ulpitll_dat7 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	USBB1_ULPITLL_DAT7_OFFMODEOUTVALUE	OffMode mode output value for pad usbb1_ulpitll_dat7 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	USBB1_ULPITLL_DAT7_OFFMODEOUTENABLE	OffMode mode output enable value for pad usbb1_ulpitll_dat7. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	USBB1_ULPITLL_DAT7_OFFMODEENABLE	OffMode mode override control for pad usbb1_ulpitll_dat7 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	USBB1_ULPITLL_DAT7_INPUTENABLE	Input enable value for pad usbb1_ulpitll_dat7 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	USBB1_ULPITLL_DAT7_PULLTYPESELECT	pullup/down selection for pad usbb1_ulpitll_dat7 0x0: pulldown selected 0x1: pullup selected	RW	0
3	USBB1_ULPITLL_DAT7_PULLUDENABLE	pullup/down enable for pad usbb1_ulpitll_dat7 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	USBB1_ULPITLL_DAT7_MUXMODE	Functional multiplexing selection for pad usbb1_ulpitll_dat7 0x0: Select usbb1_ulpitll_dat7 0x1: Select dmtimer11_pwm_evt 0x2: Select abe_mcbsp3_fsx 0x3: Select gpio_95 0x4: Select usbb1_ulpiphy_dat7 0x5: Select abe_dmic_clk3 0x6: Select hw_dbg31 0x7: Select safe_mode	RW	0x7

Table 18-425. Register Call Summary for Register CONTROL_CORE_PAD0_USBB1_ULPITLL_DAT7_PAD1_USBB1_HSIC_DATA

Control Module Functional Description

- Pad Multiplexing Register Fields: [0] [1]
- Observability Signals Multiplexing at Device Control Module Level: [2]

Control Module Register Manual

- SYSCTRL_PADCONF_CORE Register Summary: [3]

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Table 18-426. CONTROL_CORE_PAD0_USBB1_HSIC_STROBE_PAD1_USBC1_ICUSB_DP

Address Offset	0x0000 00DC		
Physical Address	0x4A10 00DC	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads usbb1_hsic_strobe and usbc1_icusb_dp Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
USBC1_ICUSB_DP_WAKEUPEVENT	USBC1_ICUSB_DP_WAKEUPENABLE	USBC1_ICUSB_DP_OFFMODEPULLTYPESELECT	USBC1_ICUSB_DP_OFFMODEPULLUDENABLE	USBC1_ICUSB_DP_OFFMODEOUTVALUE	USBC1_ICUSB_DP_OFFMODEOUTENABLE	USBC1_ICUSB_DP_OFFMODEENABLE	USBC1_ICUSB_DP_INPUTENABLE	RESERVED			USBC1_ICUSB_DP_PULLTYPESELECT	USBC1_ICUSB_DP_PULLUDENABLE	USBC1_ICUSB_DP_MUXMODE			USBB1_HSIC_STROBE_WAKEUPEVENT	USBB1_HSIC_STROBE_WAKEUPENABLE	RESERVED		USBB1_HSIC_STROBE_OFFMODEOUTVALUE	USBB1_HSIC_STROBE_OFFMODEOUTENABLE	USBB1_HSIC_STROBE_OFFMODEENABLE	RESERVED						USBB1_HSIC_STROBE_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	USBC1_ICUSB_DP_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	USBC1_ICUSB_DP_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29	USBC1_ICUSB_DP_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad usbc1_icusb_dp 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
28	USBC1_ICUSB_DP_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad usbc1_icusb_dp 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	USBC1_ICUSB_DP_OFFMODEOUTVALUE	OffMode mode output value for pad usbc1_icusb_dp 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	USBC1_ICUSB_DP_OFFMODEOUTENABLE	OffMode mode output enable value for pad usbc1_icusb_dp. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	USBC1_ICUSB_DP_OFFMODEENABLE	OffMode mode override control for pad usbc1_icusb_dp 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0

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Bits	Field Name	Description	Type	Reset
24	USBC1_ICUSB_DP_INPUTENABLE	Input enable value for pad usbc1_icusb_dp 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	USBC1_ICUSB_DP_PULLTYPESELECT	pullup/down selection for pad usbc1_icusb_dp 0x0: pulldown selected 0x1: pullup selected	RW	0
19	USBC1_ICUSB_DP_PULLUDENABLE	pullup/down enable for pad usbc1_icusb_dp 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	USBC1_ICUSB_DP_MUXMODE	Functional multiplexing selection for pad usbc1_icusb_dp 0x0: Select usbc1_icusb_dp 0x3: Select gpio_98 0x7: Select safe_mode	RW	0x7
15	USBB1_HSIC_STROBE_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	USBB1_HSIC_STROBE_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:12	RESERVED		R	0x0
11	USBB1_HSIC_STROBE_OFFMODEOUTVALUE	OffMode mode output value for pad usbb1_hsic_strobe 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	USBB1_HSIC_STROBE_OFFMODEOUTENABLE	OffMode mode output enable value for pad usbb1_hsic_strobe. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	USBB1_HSIC_STROBE_OFFMODEENABLE	OffMode mode override control for pad usbb1_hsic_strobe 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8:3	RESERVED		R	0x00
2:0	USBB1_HSIC_STROBE_MUXMODE	Functional multiplexing selection for pad usbb1_hsic_strobe 0x0: Select usbb1_hsic_strobe 0x3: Select gpio_97 0x7: Select safe_mode	RW	0x7

Table 18-427. Register Call Summary for Register CONTROL_CORE_PAD0_USBB1_HSIC_STROBE_PAD1_USBC1_ICUSB_DP

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- SYSCTRL_PADCONF_CORE Register Summary: [2]

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Table 18-428. CONTROL_CORE_PAD0_USBC1_ICUSB_DM_PAD1_SDMMC1_CLK

Address Offset	0x0000 00E0		
Physical Address	0x4A10 00E0	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads usbc1_icusb_dm and sdmmc1_clk Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SDMMC1_CLK_WAKEUPEVENT	SDMMC1_CLK_WAKEUPENABLE	SDMMC1_CLK_OFFMODEPULLTYPESELECT	SDMMC1_CLK_OFFMODEPULLUDENABLE	SDMMC1_CLK_OFFMODEOUTVALUE	SDMMC1_CLK_OFFMODEOUTENABLE	SDMMC1_CLK_OFFMODEENABLE	SDMMC1_CLK_INPUTENABLE	RESERVED			SDMMC1_CLK_PULLTYPESELECT	SDMMC1_CLK_PULLUDENABLE	SDMMC1_CLK_MUXMODE			USBC1_ICUSB_DM_WAKEUPEVENT	USBC1_ICUSB_DM_WAKEUPENABLE	USBC1_ICUSB_DM_OFFMODEPULLTYPESELECT	USBC1_ICUSB_DM_OFFMODEPULLUDENABLE	USBC1_ICUSB_DM_OFFMODEOUTVALUE	USBC1_ICUSB_DM_OFFMODEOUTENABLE	USBC1_ICUSB_DM_OFFMODEENABLE	USBC1_ICUSB_DM_INPUTENABLE	RESERVED			USBC1_ICUSB_DM_PULLTYPESELECT	USBC1_ICUSB_DM_PULLUDENABLE	USBC1_ICUSB_DM_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	SDMMC1_CLK_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	SDMMC1_CLK_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29	SDMMC1_CLK_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad sdmmc1_clk 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
28	SDMMC1_CLK_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad sdmmc1_clk 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	SDMMC1_CLK_OFFMODEOUTVALUE	OffMode mode output value for pad sdmmc1_clk 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	SDMMC1_CLK_OFFMODEOUTENABLE	OffMode mode output enable value for pad sdmmc1_clk. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	SDMMC1_CLK_OFFMODEENABLE	OffMode mode override control for pad sdmmc1_clk 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0

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Bits	Field Name	Description	Type	Reset
24	SDMMC1_CLK_INPUTENABLE	Input enable value for pad sdmmc1_clk 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	SDMMC1_CLK_PULLTYPESELECT	pullup/down selection for pad sdmmc1_clk 0x0: pulldown selected 0x1: pullup selected	RW	0
19	SDMMC1_CLK_PULLUDENABLE	pullup/down enable for pad sdmmc1_clk 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	SDMMC1_CLK_MUXMODE	Functional multiplexing selection for pad sdmmc1_clk 0x0: Select sdmmc1_clk 0x2: Select dpm_emu19 0x3: Select gpio_100 0x7: Select safe_mode	RW	0x7
15	USBC1_ICUSB_DM_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	USBC1_ICUSB_DM_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	USBC1_ICUSB_DM_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad usbc1_icusb_dm 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
12	USBC1_ICUSB_DM_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad usbc1_icusb_dm 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	USBC1_ICUSB_DM_OFFMODEOUTVALUE	OffMode mode output value for pad usbc1_icusb_dm 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	USBC1_ICUSB_DM_OFFMODEOUTENABLE	OffMode mode output enable value for pad usbc1_icusb_dm. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	USBC1_ICUSB_DM_OFFMODEENABLE	OffMode mode override control for pad usbc1_icusb_dm 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	USBC1_ICUSB_DM_INPUTENABLE	Input enable value for pad usbc1_icusb_dm 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	USBC1_ICUSB_DM_PULLTYPESELECT	pullup/down selection for pad usbc1_icusb_dm 0x0: pulldown selected 0x1: pullup selected	RW	0

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Bits	Field Name	Description	Type	Reset
3	USBC1_ICUSB_DM_PULLUDENABLE	pullup/down enable for pad usbc1_icusb_dm 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	USBC1_ICUSB_DM_MUXMODE	Functional multiplexing selection for pad usbc1_icusb_dm 0x0: Select usbc1_icusb_dm 0x3: Select gpio_99 0x7: Select safe_mode	RW	0x7

Table 18-429. Register Call Summary for Register CONTROL_CORE_PAD0_USBC1_ICUSB_DM_PAD1_SDMMC1_CLK

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- SYSCTRL_PADCONF_CORE Register Summary: [2]

Table 18-430. CONTROL_CORE_PAD0_SDMMC1_CMD_PAD1_SDMMC1_DAT0

Address Offset	0x0000 00E4		
Physical Address	0x4A10 00E4	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads sdmmc1_cmd and sdmmc1_dat0 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SDMMC1_DAT0_WAKEUPEVENT	SDMMC1_DAT0_WAKEUPENABLE	SDMMC1_DAT0_OFFMODEPULLTYPESELECT	SDMMC1_DAT0_OFFMODEPULLUDENABLE	SDMMC1_DAT0_OFFMODEOUTVALUE	SDMMC1_DAT0_OFFMODEOUTENABLE	SDMMC1_DAT0_OFFMODEENABLE	SDMMC1_DAT0_INPUTENABLE	RESERVED			SDMMC1_DAT0_PULLTYPESELECT	SDMMC1_DAT0_PULLUDENABLE	SDMMC1_DAT0_MUXMODE			SDMMC1_CMD_WAKEUPEVENT	SDMMC1_CMD_WAKEUPENABLE	SDMMC1_CMD_OFFMODEPULLTYPESELECT	SDMMC1_CMD_OFFMODEPULLUDENABLE	SDMMC1_CMD_OFFMODEOUTVALUE	SDMMC1_CMD_OFFMODEOUTENABLE	SDMMC1_CMD_OFFMODEENABLE	SDMMC1_CMD_INPUTENABLE	RESERVED			SDMMC1_CMD_PULLTYPESELECT	SDMMC1_CMD_PULLUDENABLE	SDMMC1_CMD_MUXMODE	

Bits	Field Name	Description	Type	Reset
31	SDMMC1_DAT0_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	SDMMC1_DAT0_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29	SDMMC1_DAT0_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad sdmmc1_dat0 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0

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Bits	Field Name	Description	Type	Reset
28	SDMMC1_DAT0_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad sdmmc1_dat0 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	SDMMC1_DAT0_ OFFMODEOUTVALUE	OffMode mode output value for pad sdmmc1_dat0 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	SDMMC1_DAT0_ OFFMODEOUTENABLE	OffMode mode output enable value for pad sdmmc1_dat0. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	SDMMC1_DAT0_ OFFMODEENABLE	OffMode mode override control for pad sdmmc1_dat0 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
24	SDMMC1_DAT0_ INPUTENABLE	Input enable value for pad sdmmc1_dat0 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	SDMMC1_DAT0_ PULLTYPESELECT	pullup/down selection for pad sdmmc1_dat0 0x0: pulldown selected 0x1: pullup selected	RW	0
19	SDMMC1_DAT0_ PULLUDENABLE	pullup/down enable for pad sdmmc1_dat0 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	SDMMC1_DAT0_ MUXMODE	Functional multiplexing selection for pad sdmmc1_dat0 0x0: Select sdmmc1_dat0 0x2: Select dpm_emu18 0x3: Select gpio_102 0x7: Select safe_mode	RW	0x7
15	SDMMC1_CMD_ WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	SDMMC1_CMD_ WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	SDMMC1_CMD_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad sdmmc1_cmd 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
12	SDMMC1_CMD_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad sdmmc1_cmd 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	SDMMC1_CMD_ OFFMODEOUTVALUE	OffMode mode output value for pad sdmmc1_cmd 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	SDMMC1_CMD_ OFFMODEOUTENABLE	OffMode mode output enable value for pad sdmmc1_cmd. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0

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Bits	Field Name	Description	Type	Reset
9	SDMMC1_CMD_ OFFMODEENABLE	OffMode mode override control for pad sdmmc1_cmd 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	SDMMC1_CMD_ INPUTENABLE	Input enable value for pad sdmmc1_cmd 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	SDMMC1_CMD_ PULLTYPESELECT	pullup/down selection for pad sdmmc1_cmd 0x0: pulldown selected 0x1: pullup selected	RW	0
3	SDMMC1_CMD_ PULLUDENABLE	pullup/down enable for pad sdmmc1_cmd 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	SDMMC1_CMD_ MUXMODE	Functional multiplexing selection for pad sdmmc1_cmd 0x0: Select sdmmc1_cmd 0x2: Select uart1_rx 0x3: Select gpio_101 0x7: Select safe_mode	RW	0x7

Table 18-431. Register Call Summary for Register CONTROL_CORE_PAD0_SDMMC1_CMD_PAD1_SDMMC1_DAT0

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- SYSCTRL_PADCONF_CORE Register Summary: [2]

Table 18-432. CONTROL_CORE_PAD0_SDMMC1_DAT1_PAD1_SDMMC1_DAT2

Address Offset	0x0000 00E8		
Physical Address	0x4A10 00E8	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads sdmmc1_dat1 and sdmmc1_dat2 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SDMMC1_DAT2_WAKEUPEVENT	SDMMC1_DAT2_WAKEUPENABLE	SDMMC1_DAT2_OFFMODEPULLTYPESELECT	SDMMC1_DAT2_OFFMODEPULLUDENABLE	SDMMC1_DAT2_OFFMODEOUTVALUE	SDMMC1_DAT2_OFFMODEOUTENABLE	SDMMC1_DAT2_OFFMODEENABLE	SDMMC1_DAT2_INPUTENABLE	RESERVED			SDMMC1_DAT2_PULLTYPESELECT	SDMMC1_DAT2_PULLUDENABLE	SDMMC1_DAT2_MUXMODE			SDMMC1_DAT1_WAKEUPEVENT	SDMMC1_DAT1_WAKEUPENABLE	SDMMC1_DAT1_OFFMODEPULLTYPESELECT	SDMMC1_DAT1_OFFMODEPULLUDENABLE	SDMMC1_DAT1_OFFMODEOUTVALUE	SDMMC1_DAT1_OFFMODEOUTENABLE	SDMMC1_DAT1_OFFMODEENABLE	SDMMC1_DAT1_INPUTENABLE	RESERVED			SDMMC1_DAT1_PULLTYPESELECT	SDMMC1_DAT1_PULLUDENABLE	SDMMC1_DAT1_MUXMODE		

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Bits	Field Name	Description	Type	Reset
31	SDMMC1_DAT2_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	SDMMC1_DAT2_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29	SDMMC1_DAT2_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad sdmmc1_dat2 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
28	SDMMC1_DAT2_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad sdmmc1_dat2 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	SDMMC1_DAT2_OFFMODEOUTVALUE	OffMode mode output value for pad sdmmc1_dat2 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	SDMMC1_DAT2_OFFMODEOUTENABLE	OffMode mode output enable value for pad sdmmc1_dat2. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	SDMMC1_DAT2_OFFMODEENABLE	OffMode mode override control for pad sdmmc1_dat2 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
24	SDMMC1_DAT2_INPUTENABLE	Input enable value for pad sdmmc1_dat2 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	SDMMC1_DAT2_PULLTYPESELECT	pullup/down selection for pad sdmmc1_dat2 0x0: pulldown selected 0x1: pullup selected	RW	0
19	SDMMC1_DAT2_PULLUDENABLE	pullup/down enable for pad sdmmc1_dat2 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	SDMMC1_DAT2_MUXMODE	Functional multiplexing selection for pad sdmmc1_dat2 0x0: Select sdmmc1_dat2 0x2: Select dpm_emu16 0x3: Select gpio_104 0x4: Select jtag_tms_tmsc 0x7: Select safe_mode	RW	0x7
15	SDMMC1_DAT1_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	SDMMC1_DAT1_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0

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Bits	Field Name	Description	Type	Reset
13	SDMMC1_DAT1_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad sdmmc1_dat1 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
12	SDMMC1_DAT1_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad sdmmc1_dat1 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	SDMMC1_DAT1_ OFFMODEOUTVALUE	OffMode mode output value for pad sdmmc1_dat1 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	SDMMC1_DAT1_ OFFMODEOUTENABLE	OffMode mode output enable value for pad sdmmc1_dat1. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	SDMMC1_DAT1_ OFFMODEENABLE	OffMode mode override control for pad sdmmc1_dat1 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	SDMMC1_DAT1_ INPUTENABLE	Input enable value for pad sdmmc1_dat1 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	SDMMC1_DAT1_ PULLTYPESELECT	pullup/down selection for pad sdmmc1_dat1 0x0: pulldown selected 0x1: pullup selected	RW	0
3	SDMMC1_DAT1_ PULLUDENABLE	pullup/down enable for pad sdmmc1_dat1 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	SDMMC1_DAT1_ MUXMODE	Functional multiplexing selection for pad sdmmc1_dat1 0x0: Select sdmmc1_dat1 0x2: Select dpm_emu17 0x3: Select gpio_103 0x7: Select safe_mode	RW	0x7

Table 18-433. Register Call Summary for Register CONTROL_CORE_PAD0_SDMMC1_DAT1_PAD1_SDMMC1_DAT2

Control Module Functional Description

- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual

- SYSCTRL_PADCONF_CORE Register Summary: [2]

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Table 18-434. CONTROL_CORE_PAD0_SDMMC1_DAT3_PAD1_SDMMC1_DAT4

Address Offset	0x0000 00EC		
Physical Address	0x4A10 00EC	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads sdmmc1_dat3 and sdmmc1_dat4 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SDMMC1_DAT4_WAKEUPEVENT	SDMMC1_DAT4_WAKEUPENABLE	SDMMC1_DAT4_OFFMODEPULLTYPESELECT	SDMMC1_DAT4_OFFMODEPULLUDENABLE	SDMMC1_DAT4_OFFMODEOUTVALUE	SDMMC1_DAT4_OFFMODEOUTENABLE	SDMMC1_DAT4_OFFMODEENABLE	SDMMC1_DAT4_INPUTENABLE	RESERVED			SDMMC1_DAT4_PULLTYPESELECT	SDMMC1_DAT4_PULLUDENABLE	SDMMC1_DAT4_MUXMODE			SDMMC1_DAT3_WAKEUPEVENT	SDMMC1_DAT3_WAKEUPENABLE	SDMMC1_DAT3_OFFMODEPULLTYPESELECT	SDMMC1_DAT3_OFFMODEPULLUDENABLE	SDMMC1_DAT3_OFFMODEOUTVALUE	SDMMC1_DAT3_OFFMODEOUTENABLE	SDMMC1_DAT3_OFFMODEENABLE	SDMMC1_DAT3_INPUTENABLE	RESERVED			SDMMC1_DAT3_PULLTYPESELECT	SDMMC1_DAT3_PULLUDENABLE	SDMMC1_DAT3_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	SDMMC1_DAT4_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	SDMMC1_DAT4_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29	SDMMC1_DAT4_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad sdmmc1_dat4 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
28	SDMMC1_DAT4_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad sdmmc1_dat4 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	SDMMC1_DAT4_OFFMODEOUTVALUE	OffMode mode output value for pad sdmmc1_dat4 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	SDMMC1_DAT4_OFFMODEOUTENABLE	OffMode mode output enable value for pad sdmmc1_dat4. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	SDMMC1_DAT4_OFFMODEENABLE	OffMode mode override control for pad sdmmc1_dat4 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0

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Bits	Field Name	Description	Type	Reset
24	SDMMC1_DAT4_ INPUTENABLE	Input enable value for pad sdmmc1_dat4 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	SDMMC1_DAT4_ PULLTYPESELECT	pullup/down selection for pad sdmmc1_dat4 0x0: pulldown selected 0x1: pullup selected	RW	0
19	SDMMC1_DAT4_ PULLUDENABLE	pullup/down enable for pad sdmmc1_dat4 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	SDMMC1_DAT4_ MUXMODE	Functional multiplexing selection for pad sdmmc1_dat4 0x0: Select sdmmc1_dat4 0x3: Select gpio_106 0x7: Select safe_mode	RW	0x7
15	SDMMC1_DAT3_ WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	SDMMC1_DAT3_ WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	SDMMC1_DAT3_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad sdmmc1_dat3 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
12	SDMMC1_DAT3_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad sdmmc1_dat3 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	SDMMC1_DAT3_ OFFMODEOUTVALUE	OffMode mode output value for pad sdmmc1_dat3 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	SDMMC1_DAT3_ OFFMODEOUTENABLE	OffMode mode output enable value for pad sdmmc1_dat3. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	SDMMC1_DAT3_ OFFMODEENABLE	OffMode mode override control for pad sdmmc1_dat3 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	SDMMC1_DAT3_ INPUTENABLE	Input enable value for pad sdmmc1_dat3 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	SDMMC1_DAT3_ PULLTYPESELECT	pullup/down selection for pad sdmmc1_dat3 0x0: pulldown selected 0x1: pullup selected	RW	0
3	SDMMC1_DAT3_ PULLUDENABLE	pullup/down enable for pad sdmmc1_dat3 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1

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Bits	Field Name	Description	Type	Reset
2:0	SDMMC1_DAT3_ MUXMODE	Functional multiplexing selection for pad sdmmc1_dat3 0x0: Select sdmmc1_dat3 0x2: Select dpm_emu15 0x3: Select gpio_105 0x4: Select jtag_tck 0x7: Select safe_mode	RW	0x7

Table 18-435. Register Call Summary for Register CONTROL_CORE_PAD0_SDMMC1_DAT3_PAD1_SDMMC1_DAT4

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- SYSCTRL_PADCONF_CORE Register Summary: [2]

Table 18-436. CONTROL_CORE_PAD0_SDMMC1_DAT5_PAD1_SDMMC1_DAT6

Address Offset	0x0000 00F0		
Physical Address	0x4A10 00F0	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads sdmmc1_dat5 and sdmmc1_dat6 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SDMMC1_DAT6_WAKEUPEVENT	SDMMC1_DAT6_WAKEUPENABLE	SDMMC1_DAT6_OFFMODEPULLTYPESELECT	SDMMC1_DAT6_OFFMODEPULLUDENABLE	SDMMC1_DAT6_OFFMODEOUTVALUE	SDMMC1_DAT6_OFFMODEOUTENABLE	SDMMC1_DAT6_OFFMODEENABLE	SDMMC1_DAT6_INPUTENABLE	RESERVED			SDMMC1_DAT6_PULLTYPESELECT	SDMMC1_DAT6_PULLUDENABLE	SDMMC1_DAT6_MUXMODE			SDMMC1_DAT5_WAKEUPEVENT	SDMMC1_DAT5_WAKEUPENABLE	SDMMC1_DAT5_OFFMODEPULLTYPESELECT	SDMMC1_DAT5_OFFMODEPULLUDENABLE	SDMMC1_DAT5_OFFMODEOUTVALUE	SDMMC1_DAT5_OFFMODEOUTENABLE	SDMMC1_DAT5_OFFMODEENABLE	SDMMC1_DAT5_INPUTENABLE	RESERVED			SDMMC1_DAT5_PULLTYPESELECT	SDMMC1_DAT5_PULLUDENABLE	SDMMC1_DAT5_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	SDMMC1_DAT6_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	SDMMC1_DAT6_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29	SDMMC1_DAT6_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad sdmmc1_dat6 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0

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Bits	Field Name	Description	Type	Reset
28	SDMMC1_DAT6_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad sdmmc1_dat6 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	SDMMC1_DAT6_ OFFMODEOUTVALUE	OffMode mode output value for pad sdmmc1_dat6 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	SDMMC1_DAT6_ OFFMODEOUTENABLE	OffMode mode output enable value for pad sdmmc1_dat6. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	SDMMC1_DAT6_ OFFMODEENABLE	OffMode mode override control for pad sdmmc1_dat6 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
24	SDMMC1_DAT6_ INPUTENABLE	Input enable value for pad sdmmc1_dat6 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	SDMMC1_DAT6_ PULLTYPESELECT	pullup/down selection for pad sdmmc1_dat6 0x0: pulldown selected 0x1: pullup selected	RW	0
19	SDMMC1_DAT6_ PULLUDENABLE	pullup/down enable for pad sdmmc1_dat6 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	SDMMC1_DAT6_ MUXMODE	Functional multiplexing selection for pad sdmmc1_dat6 0x0: Select sdmmc1_dat6 0x3: Select gpio_108 0x7: Select safe_mode	RW	0x7
15	SDMMC1_DAT5_ WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	SDMMC1_DAT5_ WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	SDMMC1_DAT5_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad sdmmc1_dat5 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
12	SDMMC1_DAT5_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad sdmmc1_dat5 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	SDMMC1_DAT5_ OFFMODEOUTVALUE	OffMode mode output value for pad sdmmc1_dat5 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	SDMMC1_DAT5_ OFFMODEOUTENABLE	OffMode mode output enable value for pad sdmmc1_dat5. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0

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Bits	Field Name	Description	Type	Reset
9	SDMMC1_DAT5_ OFFMODEENABLE	OffMode mode override control for pad sdmmc1_dat5 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	SDMMC1_DAT5_ INPUTENABLE	Input enable value for pad sdmmc1_dat5 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	SDMMC1_DAT5_ PULLTYPESELECT	pullup/down selection for pad sdmmc1_dat5 0x0: pulldown selected 0x1: pullup selected	RW	0
3	SDMMC1_DAT5_ PULLUDENABLE	pullup/down enable for pad sdmmc1_dat5 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	SDMMC1_DAT5_ MUXMODE	Functional multiplexing selection for pad sdmmc1_dat5 0x0: Select sdmmc1_dat5 0x3: Select gpio_107 0x7: Select safe_mode	RW	0x7

Table 18-437. Register Call Summary for Register CONTROL_CORE_PAD0_SDMMC1_DAT5_PAD1_SDMMC1_DAT6

Control Module Functional Description • Pad Multiplexing Register Fields: [0] [1]
Control Module Register Manual • SYSCTRL_PADCONF_CORE Register Summary: [2]

Table 18-438. CONTROL_CORE_PAD0_SDMMC1_DAT7_PAD1_ABE_MCBSP2_CLKX

Address Offset	0x0000 00F4		
Physical Address	0x4A10 00F4	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads sdmmc1_dat7 and abe_mcbsp2_clkx Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ABE_MCBSP2_CLKX_WAKEUPEVENT	ABE_MCBSP2_CLKX_WAKEUPENABLE	ABE_MCBSP2_CLKX_OFFMODEPULLTYPESELECT	ABE_MCBSP2_CLKX_OFFMODEPULLUDENABLE	ABE_MCBSP2_CLKX_OFFMODEOUTVALUE	ABE_MCBSP2_CLKX_OFFMODEOUTENABLE	ABE_MCBSP2_CLKX_OFFMODEENABLE	ABE_MCBSP2_CLKX_INPUTENABLE	RESERVED			ABE_MCBSP2_CLKX_PULLTYPESELECT	ABE_MCBSP2_CLKX_PULLUDENABLE	ABE_MCBSP2_CLKX_MUXMODE			SDMMC1_DAT7_WAKEUPEVENT	SDMMC1_DAT7_WAKEUPENABLE	SDMMC1_DAT7_OFFMODEPULLTYPESELECT	SDMMC1_DAT7_OFFMODEPULLUDENABLE	SDMMC1_DAT7_OFFMODEOUTVALUE	SDMMC1_DAT7_OFFMODEOUTENABLE	SDMMC1_DAT7_OFFMODEENABLE	SDMMC1_DAT7_INPUTENABLE	RESERVED			SDMMC1_DAT7_PULLTYPESELECT	SDMMC1_DAT7_PULLUDENABLE	SDMMC1_DAT7_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	ABE_MCBSP2_CLKX_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	ABE_MCBSP2_CLKX_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29	ABE_MCBSP2_CLKX_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad abe_mcbsp2_clkx 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
28	ABE_MCBSP2_CLKX_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad abe_mcbsp2_clkx 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	ABE_MCBSP2_CLKX_OFFMODEOUTVALUE	OffMode mode output value for pad abe_mcbsp2_clkx 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	ABE_MCBSP2_CLKX_OFFMODEOUTENABLE	OffMode mode output enable value for pad abe_mcbsp2_clkx. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	ABE_MCBSP2_CLKX_OFFMODEENABLE	OffMode mode override control for pad abe_mcbsp2_clkx 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
24	ABE_MCBSP2_CLKX_INPUTENABLE	Input enable value for pad abe_mcbsp2_clkx 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
20	ABE_MCBSP2_CLKX_PULLTYPESELECT	pullup/down selection for pad abe_mcbsp2_clkx 0x0: pulldown selected 0x1: pullup selected	RW	0
19	ABE_MCBSP2_CLKX_PULLUDENABLE	pullup/down enable for pad abe_mcbsp2_clkx 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	ABE_MCBSP2_CLKX_MUXMODE	Functional multiplexing selection for pad abe_mcbsp2_clkx 0x0: Select abe_mcbsp2_clkx 0x1: Select mcspi2_clk 0x2: Select abe_mcasp_ahclkx 0x3: Select gpio_110 0x4: Select usbb2_mm_rxdm 0x7: Select safe_mode	RW	0x7
15	SDMMC1_DAT7_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	SDMMC1_DAT7_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	SDMMC1_DAT7_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad sdmmc1_dat7 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
12	SDMMC1_DAT7_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad sdmmc1_dat7 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	SDMMC1_DAT7_OFFMODEOUTVALUE	OffMode mode output value for pad sdmmc1_dat7 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	SDMMC1_DAT7_OFFMODEOUTENABLE	OffMode mode output enable value for pad sdmmc1_dat7. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	SDMMC1_DAT7_OFFMODEENABLE	OffMode mode override control for pad sdmmc1_dat7 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	SDMMC1_DAT7_INPUTENABLE	Input enable value for pad sdmmc1_dat7 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	SDMMC1_DAT7_PULLTYPESELECT	pullup/down selection for pad sdmmc1_dat7 0x0: pulldown selected 0x1: pullup selected	RW	0
3	SDMMC1_DAT7_PULLUDENABLE	pullup/down enable for pad sdmmc1_dat7 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1

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Bits	Field Name	Description	Type	Reset
2:0	SDMMC1_DAT7_ MUXMODE	Functional multiplexing selection for pad sdmmc1_dat7 0x0: Select sdmmc1_dat7 0x3: Select gpio_109 0x7: Select safe_mode	RW	0x7

Table 18-439. Register Call Summary for Register CONTROL_CORE_PAD0_SDMMC1_DAT7_PAD1_ABE_MCBSP2_CLKX

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- SYSCTRL_PADCONF_CORE Register Summary: [2]

Table 18-440. CONTROL_CORE_PAD0_ABE_MCBSP2_DR_PAD1_ABE_MCBSP2_DX

Address Offset	0x0000 00F8		
Physical Address	0x4A10 00F8	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads abe_mcbsp2_dr and abe_mcbsp2_dx Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ABE_MCBSP2_DX_WAKEUPEVENT	ABE_MCBSP2_DX_WAKEUPENABLE	ABE_MCBSP2_DX_OFFMODEPULLTYPESELECT	ABE_MCBSP2_DX_OFFMODEPULLUDENABLE	ABE_MCBSP2_DX_OFFMODEOUTVALUE	ABE_MCBSP2_DX_OFFMODEOUTENABLE	ABE_MCBSP2_DX_OFFMODEENABLE	ABE_MCBSP2_DX_INPUTENABLE	RESERVED			ABE_MCBSP2_DX_PULLTYPESELECT	ABE_MCBSP2_DX_PULLUDENABLE	ABE_MCBSP2_DX_MUXMODE			ABE_MCBSP2_DR_WAKEUPEVENT	ABE_MCBSP2_DR_WAKEUPENABLE	ABE_MCBSP2_DR_OFFMODEPULLTYPESELECT	ABE_MCBSP2_DR_OFFMODEPULLUDENABLE	ABE_MCBSP2_DR_OFFMODEOUTVALUE	ABE_MCBSP2_DR_OFFMODEOUTENABLE	ABE_MCBSP2_DR_OFFMODEENABLE	ABE_MCBSP2_DR_INPUTENABLE	RESERVED			ABE_MCBSP2_DR_PULLTYPESELECT	ABE_MCBSP2_DR_PULLUDENABLE	ABE_MCBSP2_DR_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	ABE_MCBSP2_DX_ WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	ABE_MCBSP2_DX_ WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29	ABE_MCBSP2_DX_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad abe_mcbsp2_dx 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0

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Bits	Field Name	Description	Type	Reset
28	ABE_MCBSP2_DX_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad abe_mcbsp2_dx 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	ABE_MCBSP2_DX_ OFFMODEOUTVALUE	OffMode mode output value for pad abe_mcbsp2_dx 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	ABE_MCBSP2_DX_ OFFMODEOUTENABLE	OffMode mode output enable value for pad abe_mcbsp2_dx. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	ABE_MCBSP2_DX_ OFFMODEENABLE	OffMode mode override control for pad abe_mcbsp2_dx 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
24	ABE_MCBSP2_DX_ INPUTENABLE	Input enable value for pad abe_mcbsp2_dx 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	ABE_MCBSP2_DX_ PULLTYPESELECT	pullup/down selection for pad abe_mcbsp2_dx 0x0: pulldown selected 0x1: pullup selected	RW	0
19	ABE_MCBSP2_DX_ PULLUDENABLE	pullup/down enable for pad abe_mcbsp2_dx 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	ABE_MCBSP2_DX_ MUXMODE	Functional multiplexing selection for pad abe_mcbsp2_dx 0x0: Select abe_mcbsp2_dx 0x1: Select mcspi2_simo 0x2: Select abe_mcasp_amute 0x3: Select gpio_112 0x4: Select usbb2_mm_rxrcv 0x7: Select safe_mode	RW	0x7
15	ABE_MCBSP2_DR_ WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	ABE_MCBSP2_DR_ WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	ABE_MCBSP2_DR_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad abe_mcbsp2_dr 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
12	ABE_MCBSP2_DR_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad abe_mcbsp2_dr 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	ABE_MCBSP2_DR_ OFFMODEOUTVALUE	OffMode mode output value for pad abe_mcbsp2_dr 0x0: Set value at 0 0x1: Set value at 1	RW	0

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Bits	Field Name	Description	Type	Reset
10	ABE_MCBSP2_DR_OFFMODEOUTENABLE	OffMode mode output enable value for pad abe_mcbsp2_dr. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	ABE_MCBSP2_DR_OFFMODEENABLE	OffMode mode override control for pad abe_mcbsp2_dr 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	ABE_MCBSP2_DR_INPUTENABLE	Input enable value for pad abe_mcbsp2_dr 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	ABE_MCBSP2_DR_PULLTYPESELECT	pullup/down selection for pad abe_mcbsp2_dr 0x0: pulldown selected 0x1: pullup selected	RW	0
3	ABE_MCBSP2_DR_PULLUDENABLE	pullup/down enable for pad abe_mcbsp2_dr 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	ABE_MCBSP2_DR_MUXMODE	Functional multiplexing selection for pad abe_mcbsp2_dr 0x0: Select abe_mcbsp2_dr 0x1: Select mcspi2_somi 0x2: Select abe_mcasp_axr 0x3: Select gpio_111 0x4: Select usbb2_mm_rxdp 0x7: Select safe_mode	RW	0x7

Table 18-441. Register Call Summary for Register CONTROL_CORE_PAD0_ABE_MCBSP2_DR_PAD1_ABE_MCBSP2_DX

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- SYSCTRL_PADCONF_CORE Register Summary: [2]

Table 18-442. CONTROL_CORE_PAD0_ABE_MCBSP2_FSX_PAD1_ABE_MCBSP1_CLKX

Address Offset	0x0000 00FC		
Physical Address	0x4A10 00FC	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads abe_mcbsp2_fsx and abe_mcbsp1_clkx Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ABE_MCBSP1_CLKX_WAKEUPEVENT	ABE_MCBSP1_CLKX_WAKEUPENABLE	ABE_MCBSP1_CLKX_OFFMODEPULLTYPESELECT	ABE_MCBSP1_CLKX_OFFMODEPULLUDENABLE	ABE_MCBSP1_CLKX_OFFMODEOUTVALUE	ABE_MCBSP1_CLKX_OFFMODEOUTENABLE	ABE_MCBSP1_CLKX_OFFMODEENABLE	ABE_MCBSP1_CLKX_INPUTENABLE	RESERVED			ABE_MCBSP1_CLKX_PULLTYPESELECT	ABE_MCBSP1_CLKX_PULLUDENABLE	ABE_MCBSP1_CLKX_MUXMODE			ABE_MCBSP2_FSX_WAKEUPEVENT	ABE_MCBSP2_FSX_WAKEUPENABLE	ABE_MCBSP2_FSX_OFFMODEPULLTYPESELECT	ABE_MCBSP2_FSX_OFFMODEPULLUDENABLE	ABE_MCBSP2_FSX_OFFMODEOUTVALUE	ABE_MCBSP2_FSX_OFFMODEOUTENABLE	ABE_MCBSP2_FSX_OFFMODEENABLE	ABE_MCBSP2_FSX_INPUTENABLE	RESERVED			ABE_MCBSP2_FSX_PULLTYPESELECT	ABE_MCBSP2_FSX_PULLUDENABLE	ABE_MCBSP2_FSX_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	ABE_MCBSP1_CLKX_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	ABE_MCBSP1_CLKX_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29	ABE_MCBSP1_CLKX_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad abe_mcbsp1_clkx 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
28	ABE_MCBSP1_CLKX_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad abe_mcbsp1_clkx 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	ABE_MCBSP1_CLKX_OFFMODEOUTVALUE	OffMode mode output value for pad abe_mcbsp1_clkx 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	ABE_MCBSP1_CLKX_OFFMODEOUTENABLE	OffMode mode output enable value for pad abe_mcbsp1_clkx. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	ABE_MCBSP1_CLKX_OFFMODEENABLE	OffMode mode override control for pad abe_mcbsp1_clkx 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
24	ABE_MCBSP1_CLKX_INPUTENABLE	Input enable value for pad abe_mcbsp1_clkx 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
20	ABE_MCBSP1_CLKX_ PULLTYPESELECT	pullup/down selection for pad abe_mcbsp1_clkx 0x0: pulldown selected 0x1: pullup selected	RW	0
19	ABE_MCBSP1_CLKX_ PULLUDENABLE	pullup/down enable for pad abe_mcbsp1_clkx 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	ABE_MCBSP1_CLKX_ MUXMODE	Functional multiplexing selection for pad abe_mcbsp1_clkx 0x0: Select abe_mcbsp1_clkx 0x1: Select abe_slimbus1_clock 0x3: Select gpio_114 0x7: Select safe_mode	RW	0x7
15	ABE_MCBSP2_FSX_ WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	ABE_MCBSP2_FSX_ WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	ABE_MCBSP2_FSX_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad abe_mcbsp2_fsx 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
12	ABE_MCBSP2_FSX_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad abe_mcbsp2_fsx 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	ABE_MCBSP2_FSX_ OFFMODEOUTVALUE	OffMode mode output value for pad abe_mcbsp2_fsx 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	ABE_MCBSP2_FSX_ OFFMODEOUTENABLE	OffMode mode output enable value for pad abe_mcbsp2_fsx. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	ABE_MCBSP2_FSX_ OFFMODEENABLE	OffMode mode override control for pad abe_mcbsp2_fsx 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	ABE_MCBSP2_FSX_ INPUTENABLE	Input enable value for pad abe_mcbsp2_fsx 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	ABE_MCBSP2_FSX_ PULLTYPESELECT	pullup/down selection for pad abe_mcbsp2_fsx 0x0: pulldown selected 0x1: pullup selected	RW	0
3	ABE_MCBSP2_FSX_ PULLUDENABLE	pullup/down enable for pad abe_mcbsp2_fsx 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1

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Bits	Field Name	Description	Type	Reset
2:0	ABE_MCBSP2_FSX_ MUXMODE	Functional multiplexing selection for pad abe_mcbsp2_fsx 0x0: Select abe_mcbsp2_fsx 0x1: Select mcspi2_cs0 0x2: Select abe_mcasp_afsx 0x3: Select gpio_113 0x4: Select usbb2_mm_txen 0x7: Select safe_mode	RW	0x7

Table 18-443. Register Call Summary for Register CONTROL_CORE_PAD0_ABE_MCBSP2_FSX_PAD1_ABE_MCBSP1_CLKX

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- SYSCTRL_PADCONF_CORE Register Summary: [2]

Table 18-444. CONTROL_CORE_PAD0_ABE_MCBSP1_DR_PAD1_ABE_MCBSP1_DX

Address Offset	0x0000 0100		
Physical Address	0x4A10 0100	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads abe_mcbsp1_dr and abe_mcbsp1_dx Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ABE_MCBSP1_DX_WAKEUPEVENT	ABE_MCBSP1_DX_WAKEUPENABLE	ABE_MCBSP1_DX_OFFMODEPULLTYPESELECT	ABE_MCBSP1_DX_OFFMODEPULLUDENABLE	ABE_MCBSP1_DX_OFFMODEOUTVALUE	ABE_MCBSP1_DX_OFFMODEOUTENABLE	ABE_MCBSP1_DX_OFFMODEENABLE	ABE_MCBSP1_DX_INPUTENABLE	RESERVED			ABE_MCBSP1_DX_PULLTYPESELECT	ABE_MCBSP1_DX_PULLUDENABLE	ABE_MCBSP1_DX_MUXMODE			ABE_MCBSP1_DR_WAKEUPEVENT	ABE_MCBSP1_DR_WAKEUPENABLE	ABE_MCBSP1_DR_OFFMODEPULLTYPESELECT	ABE_MCBSP1_DR_OFFMODEPULLUDENABLE	ABE_MCBSP1_DR_OFFMODEOUTVALUE	ABE_MCBSP1_DR_OFFMODEOUTENABLE	ABE_MCBSP1_DR_OFFMODEENABLE	ABE_MCBSP1_DR_INPUTENABLE	RESERVED			ABE_MCBSP1_DR_PULLTYPESELECT	ABE_MCBSP1_DR_PULLUDENABLE	ABE_MCBSP1_DR_MUXMODE	

Bits	Field Name	Description	Type	Reset
31	ABE_MCBSP1_DX_ WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	ABE_MCBSP1_DX_ WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0

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Bits	Field Name	Description	Type	Reset
29	ABE_MCBSP1_DX_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad abe_mcbsp1_dx 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
28	ABE_MCBSP1_DX_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad abe_mcbsp1_dx 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	ABE_MCBSP1_DX_OFFMODEOUTVALUE	OffMode mode output value for pad abe_mcbsp1_dx 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	ABE_MCBSP1_DX_OFFMODEOUTENABLE	OffMode mode output enable value for pad abe_mcbsp1_dx. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	ABE_MCBSP1_DX_OFFMODEENABLE	OffMode mode override control for pad abe_mcbsp1_dx 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
24	ABE_MCBSP1_DX_INPUTENABLE	Input enable value for pad abe_mcbsp1_dx 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	ABE_MCBSP1_DX_PULLTYPESELECT	pullup/down selection for pad abe_mcbsp1_dx 0x0: pulldown selected 0x1: pullup selected	RW	0
19	ABE_MCBSP1_DX_PULLUDENABLE	pullup/down enable for pad abe_mcbsp1_dx 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	ABE_MCBSP1_DX_MUXMODE	Functional multiplexing selection for pad abe_mcbsp1_dx 0x0: Select abe_mcbsp1_dx 0x1: Select sdmmc3_dat2 0x2: Select abe_mcasp_aclkx 0x3: Select gpio_116 0x7: Select safe_mode	RW	0x7
15	ABE_MCBSP1_DR_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	ABE_MCBSP1_DR_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	ABE_MCBSP1_DR_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad abe_mcbsp1_dr 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
12	ABE_MCBSP1_DR_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad abe_mcbsp1_dr 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0

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Bits	Field Name	Description	Type	Reset
11	ABE_MCBSP1_ DR_OFFMODEOUTVALUE	OffMode mode output value for pad abe_mcbsp1_dr 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	ABE_MCBSP1_ DR_OFFMODEOUTENABLE	OffMode mode output enable value for pad abe_mcbsp1_dr. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	ABE_MCBSP1_ DR_OFFMODEENABLE	OffMode mode override control for pad abe_mcbsp1_dr 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	ABE_MCBSP1_ DR_INPUTENABLE	Input enable value for pad abe_mcbsp1_dr 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	ABE_MCBSP1_ DR_PULLTYPESELECT	pullup/down selection for pad abe_mcbsp1_dr 0x0: pulldown selected 0x1: pullup selected	RW	0
3	ABE_MCBSP1_ DR_PULLUDENABLE	pullup/down enable for pad abe_mcbsp1_dr 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	ABE_MCBSP1_ DR_MUXMODE	Functional multiplexing selection for pad abe_mcbsp1_dr 0x0: Select abe_mcbsp1_dr 0x1: Select abe_slimbus1_data 0x3: Select gpio_115 0x7: Select safe_mode	RW	0x7

Table 18-445. Register Call Summary for Register CONTROL_CORE_PAD0_ABE_MCBSP1_DR_PAD1_ABE_MCBSP1_DX

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- SYSCTRL_PADCONF_CORE Register Summary: [2]

Table 18-446. CONTROL_CORE_PAD0_ABE_MCBSP1_FSX_PAD1_ABE_PDM_UL_DATA

Address Offset	0x0000 0104		
Physical Address	0x4A10 0104	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads abe_mcbsp1_fsx and abe_pdm_ul_data Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ABE_PDM_UL_DATA_WAKEUPEVENT	ABE_PDM_UL_DATA_WAKEUPENABLE	RESERVED					ABE_PDM_UL_DATA_INPUTENABLE	RESERVED			ABE_PDM_UL_DATA_PULLTYPESELECT	ABE_PDM_UL_DATA_PULLUDENABLE	ABE_PDM_UL_DATA_MUXMODE			ABE_MCBSP1_FSX_WAKEUPEVENT	ABE_MCBSP1_FSX_WAKEUPENABLE	ABE_MCBSP1_FSX_OFFMODEPULLTYPESELECT	ABE_MCBSP1_FSX_OFFMODEPULLUDENABLE	ABE_MCBSP1_FSX_OFFMODEOUTVALUE	ABE_MCBSP1_FSX_OFFMODEOUTENABLE	ABE_MCBSP1_FSX_OFFMODEENABLE	ABE_MCBSP1_FSX_INPUTENABLE	RESERVED			ABE_MCBSP1_FSX_PULLTYPESELECT	ABE_MCBSP1_FSX_PULLUDENABLE	ABE_MCBSP1_FSX_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	ABE_PDM_UL_DATA_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	ABE_PDM_UL_DATA_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x00
24	ABE_PDM_UL_DATA_INPUTENABLE	Input enable value for pad abe_pdm_ul_data 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	ABE_PDM_UL_DATA_PULLTYPESELECT	pullup/down selection for pad abe_pdm_ul_data 0x0: pulldown selected 0x1: pullup selected	RW	0
19	ABE_PDM_UL_DATA_PULLUDENABLE	pullup/down enable for pad abe_pdm_ul_data 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	ABE_PDM_UL_DATA_MUXMODE	Functional multiplexing selection for pad abe_pdm_ul_data 0x0: Select abe_pdm_ul_data 0x1: Select abe_mcbsp3_dr 0x7: Select safe_mode	RW	0x7
15	ABE_MCBSP1_FSX_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	ABE_MCBSP1_FSX_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0

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Bits	Field Name	Description	Type	Reset
13	ABE_MCBSP1_FSX_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad abe_mcbsp1_fsx 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
12	ABE_MCBSP1_FSX_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad abe_mcbsp1_fsx 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	ABE_MCBSP1_FSX_OFFMODEOUTVALUE	OffMode mode output value for pad abe_mcbsp1_fsx 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	ABE_MCBSP1_FSX_OFFMODEOUTENABLE	OffMode mode output enable value for pad abe_mcbsp1_fsx. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	ABE_MCBSP1_FSX_OFFMODEENABLE	OffMode mode override control for pad abe_mcbsp1_fsx 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	ABE_MCBSP1_FSX_INPUTENABLE	Input enable value for pad abe_mcbsp1_fsx 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	ABE_MCBSP1_FSX_PULLTYPESELECT	pullup/down selection for pad abe_mcbsp1_fsx 0x0: pulldown selected 0x1: pullup selected	RW	0
3	ABE_MCBSP1_FSX_PULLUDENABLE	pullup/down enable for pad abe_mcbsp1_fsx 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	ABE_MCBSP1_FSX_MUXMODE	Functional multiplexing selection for pad abe_mcbsp1_fsx 0x0: Select abe_mcbsp1_fsx 0x1: Select sdmmc3_dat3 0x2: Select abe_mcasp_amutein 0x3: Select gpio_117 0x7: Select safe_mode	RW	0x7

Table 18-447. Register Call Summary for Register CONTROL_CORE_PAD0_ABE_MCBSP1_FSX_PAD1_ABE_PDM_UL_DATA

Control Module Functional Description

- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual

- SYSCTRL_PADCONF_CORE Register Summary: [2]

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Table 18-448. CONTROL_CORE_PAD0_ABE_PDM_DL_DATA_PAD1_ABE_PDM_FRAME

Address Offset	0x0000 0108		
Physical Address	0x4A10 0108	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads abe_pdm_dl_data and abe_pdm_frame Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ABE_PDM_FRAME_WAKEUPEVENT	ABE_PDM_FRAME_WAKEUPENABLE	ABE_PDM_FRAME_OFFMODEPULLTYPESELECT	ABE_PDM_FRAME_OFFMODEPULLUDENABLE	ABE_PDM_FRAME_OFFMODEOUTVALUE	ABE_PDM_FRAME_OFFMODEOUTENABLE	ABE_PDM_FRAME_OFFMODEENABLE	ABE_PDM_FRAME_INPUTENABLE	RESERVED			ABE_PDM_FRAME_PULLTYPESELECT	ABE_PDM_FRAME_PULLUDENABLE	ABE_PDM_FRAME_MUXMODE			ABE_PDM_DL_DATA_WAKEUPEVENT	ABE_PDM_DL_DATA_WAKEUPENABLE	ABE_PDM_DL_DATA_OFFMODEPULLTYPESELECT	ABE_PDM_DL_DATA_OFFMODEPULLUDENABLE	ABE_PDM_DL_DATA_OFFMODEOUTVALUE	ABE_PDM_DL_DATA_OFFMODEOUTENABLE	ABE_PDM_DL_DATA_OFFMODEENABLE	ABE_PDM_DL_DATA_INPUTENABLE	RESERVED			ABE_PDM_DL_DATA_PULLTYPESELECT	ABE_PDM_DL_DATA_PULLUDENABLE	ABE_PDM_DL_DATA_MUXMODE	

Bits	Field Name	Description	Type	Reset
31	ABE_PDM_FRAME_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	ABE_PDM_FRAME_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29	ABE_PDM_FRAME_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad abe_pdm_frame 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
28	ABE_PDM_FRAME_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad abe_pdm_frame 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	ABE_PDM_FRAME_OFFMODEOUTVALUE	OffMode mode output value for pad abe_pdm_frame 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	ABE_PDM_FRAME_OFFMODEOUTENABLE	OffMode mode output enable value for pad abe_pdm_frame. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0

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Bits	Field Name	Description	Type	Reset
25	ABE_PDM_FRAME_OFFMODEENABLE	OffMode mode override control for pad abe_pdm_frame 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
24	ABE_PDM_FRAME_INPUTENABLE	Input enable value for pad abe_pdm_frame 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	ABE_PDM_FRAME_PULLTYPESELECT	pullup/down selection for pad abe_pdm_frame 0x0: pulldown selected 0x1: pullup selected	RW	0
19	ABE_PDM_FRAME_PULLUDENABLE	pullup/down enable for pad abe_pdm_frame 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	ABE_PDM_FRAME_MUXMODE	Functional multiplexing selection for pad abe_pdm_frame 0x0: Select abe_pdm_frame 0x1: Select abe_mcbsp3_clkx 0x7: Select safe_mode	RW	0x7
15	ABE_PDM_DL_DATA_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	ABE_PDM_DL_DATA_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	ABE_PDM_DL_DATA_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad abe_pdm_dl_data 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
12	ABE_PDM_DL_DATA_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad abe_pdm_dl_data 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	ABE_PDM_DL_DATA_OFFMODEOUTVALUE	OffMode mode output value for pad abe_pdm_dl_data 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	ABE_PDM_DL_DATA_OFFMODEOUTENABLE	OffMode mode output enable value for pad abe_pdm_dl_data. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	ABE_PDM_DL_DATA_OFFMODEENABLE	OffMode mode override control for pad abe_pdm_dl_data 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	ABE_PDM_DL_DATA_INPUTENABLE	Input enable value for pad abe_pdm_dl_data 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
4	ABE_PDM_DL_DATA_PULLTYPESELECT	pullup/down selection for pad abe_pdm_dl_data 0x0: pulldown selected 0x1: pullup selected	RW	0
3	ABE_PDM_DL_DATA_PULLUDENABLE	pullup/down enable for pad abe_pdm_dl_data 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	ABE_PDM_DL_DATA_MUXMODE	Functional multiplexing selection for pad abe_pdm_dl_data 0x0: Select abe_pdm_dl_data 0x1: Select abe_mcbsp3_dx 0x7: Select safe_mode	RW	0x7

Table 18-449. Register Call Summary for Register CONTROL_CORE_PAD0_ABE_PDM_DL_DATA_PAD1_ABE_PDM_FRAME

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- SYSCTRL_PADCONF_CORE Register Summary: [2]

Table 18-450. CONTROL_CORE_PAD0_ABE_PDM_LB_CLK_PAD1_ABE_CLKS

Address Offset	0x0000 010C		
Physical Address	0x4A10 010C	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads abe_pdm_lb_clk and abe_clks Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ABE_CLKS_WAKEUPEVENT	ABE_CLKS_WAKEUPENABLE	ABE_CLKS_OFFMODEPULLTYPESELECT	ABE_CLKS_OFFMODEPULLUDENABLE	ABE_CLKS_OFFMODEOUTVALUE	ABE_CLKS_OFFMODEOUTENABLE	ABE_CLKS_OFFMODEENABLE	ABE_CLKS_INPUTENABLE	RESERVED			ABE_CLKS_PULLTYPESELECT	ABE_CLKS_PULLUDENABLE	ABE_CLKS_MUXMODE			ABE_PDM_LB_CLK_WAKEUPEVENT	ABE_PDM_LB_CLK_WAKEUPENABLE	ABE_PDM_LB_CLK_OFFMODEPULLTYPESELECT	ABE_PDM_LB_CLK_OFFMODEPULLUDENABLE	ABE_PDM_LB_CLK_OFFMODEOUTVALUE	ABE_PDM_LB_CLK_OFFMODEOUTENABLE	ABE_PDM_LB_CLK_OFFMODEENABLE	ABE_PDM_LB_CLK_INPUTENABLE	RESERVED			ABE_PDM_LB_CLK_PULLTYPESELECT	ABE_PDM_LB_CLK_PULLUDENABLE	ABE_PDM_LB_CLK_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	ABE_CLKS_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0

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Bits	Field Name	Description	Type	Reset
30	ABE_CLKS_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29	ABE_CLKS_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad abe_clks 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
28	ABE_CLKS_OFFMODEPULLUD ENABLE	OffMode mode pullup/down enable for pad abe_clks 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	ABE_CLKS_OFFMODEOUTVAL UE	OffMode mode output value for pad abe_clks 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	ABE_CLKS_OFFMODEOUTENA BLE	OffMode mode output enable value for pad abe_clks. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	ABE_CLKS_OFFMODEENABLE	OffMode mode override control for pad abe_clks 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
24	ABE_CLKS_INPUTENABLE	Input enable value for pad abe_clks 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	ABE_CLKS_PULLTYPESELECT	pullup/down selection for pad abe_clks 0x0: pulldown selected 0x1: pullup selected	RW	0
19	ABE_CLKS_PULLUDENABLE	pullup/down enable for pad abe_clks 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	ABE_CLKS_MUXMODE	Functional multiplexing selection for pad abe_clks 0x0: Select abe_clks 0x3: Select gpio_118 0x7: Select safe_mode	RW	0x7
15	ABE_PDM_LB_ CLK_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	ABE_PDM_LB_ CLK_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	ABE_PDM_LB_ CLK_OFFMODEPULLTYPESEL ECT	OffMode mode pullup/down selection for pad abe_pdm_lb_clk 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
12	ABE_PDM_LB_CLK_OFFMODE PULLUDENABLE	OffMode mode pullup/down enable for pad abe_pdm_lb_clk 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0

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Bits	Field Name	Description	Type	Reset
11	ABE_PDM_LB_CLK_OFFMODE OUTVALUE	OffMode mode output value for pad abe_pdm_lb_clk 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	ABE_PDM_LB_CLK_OFFMODE OUTENABLE	OffMode mode output enable value for pad abe_pdm_lb_clk. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	ABE_PDM_LB_CLK_OFFMODE ENABLE	OffMode mode override control for pad abe_pdm_lb_clk 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	ABE_PDM_LB_CLK_INPUTENA BLE	Input enable value for pad abe_pdm_lb_clk 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	ABE_PDM_LB_CLK_PULLTYPE SELECT	pullup/down selection for pad abe_pdm_lb_clk 0x0: pulldown selected 0x1: pullup selected	RW	0
3	ABE_PDM_LB_CLK_PULLUDEN ABLE	pullup/down enable for pad abe_pdm_lb_clk 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	ABE_PDM_LB_CLK_MUXMODE	Functional multiplexing selection for pad abe_pdm_lb_clk 0x0: Select abe_pdm_lb_clk 0x1: Select abe_mcbsp3_fsx 0x7: Select safe_mode	RW	0x7

Table 18-451. Register Call Summary for Register CONTROL_CORE_PAD0_ABE_PDM_LB_CLK_PAD1_ABE_CLKS

Control Module Functional Description • Pad Multiplexing Register Fields: [0] [1]
Control Module Register Manual • SYSCTRL_PADCONF_CORE Register Summary: [2]

Table 18-452. CONTROL_CORE_PAD0_ABE_DMIC_CLK1_PAD1_ABE_DMIC_DIN1

Address Offset	0x0000 0110		
Physical Address	0x4A10 0110	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads abe_dmic_clk1 and abe_dmic_din1 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ABE_DMIC_DIN1_WAKEUPEVENT	ABE_DMIC_DIN1_WAKEUPENABLE	ABE_DMIC_DIN1_OFFMODEPULLTYPESELECT	ABE_DMIC_DIN1_OFFMODEPULLUDENABLE	ABE_DMIC_DIN1_OFFMODEOUTVALUE	ABE_DMIC_DIN1_OFFMODEOUTENABLE	ABE_DMIC_DIN1_OFFMODEENABLE	ABE_DMIC_DIN1_INPUTENABLE	RESERVED			ABE_DMIC_DIN1_PULLTYPESELECT	ABE_DMIC_DIN1_PULLUDENABLE	ABE_DMIC_DIN1_MUXMODE			ABE_DMIC_CLK1_WAKEUPEVENT	ABE_DMIC_CLK1_WAKEUPENABLE	ABE_DMIC_CLK1_OFFMODEPULLTYPESELECT	ABE_DMIC_CLK1_OFFMODEPULLUDENABLE	ABE_DMIC_CLK1_OFFMODEOUTVALUE	ABE_DMIC_CLK1_OFFMODEOUTENABLE	ABE_DMIC_CLK1_OFFMODEENABLE	ABE_DMIC_CLK1_INPUTENABLE	RESERVED			ABE_DMIC_CLK1_PULLTYPESELECT	ABE_DMIC_CLK1_PULLUDENABLE	ABE_DMIC_CLK1_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	ABE_DMIC_DIN1_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	ABE_DMIC_DIN1_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29	ABE_DMIC_DIN1_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad abe_dmic_din1 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
28	ABE_DMIC_DIN1_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad abe_dmic_din1 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	ABE_DMIC_DIN1_OFFMODEOUTVALUE	OffMode mode output value for pad abe_dmic_din1 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	ABE_DMIC_DIN1_OFFMODEOUTENABLE	OffMode mode output enable value for pad abe_dmic_din1. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	ABE_DMIC_DIN1_OFFMODEENABLE	OffMode mode override control for pad abe_dmic_din1 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
24	ABE_DMIC_DIN1_INPUTENABLE	Input enable value for pad abe_dmic_din1 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	ABE_DMIC_DIN1_PULLTYPESELECT	pullup/down selection for pad abe_dmic_din1 0x0: pulldown selected 0x1: pullup selected	RW	0

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Bits	Field Name	Description	Type	Reset
19	ABE_DMIC_DIN1_PULLUDENABLE	pullup/down enable for pad abe_dmic_din1 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	ABE_DMIC_DIN1_MUXMODE	Functional multiplexing selection for pad abe_dmic_din1 0x0: Select abe_dmic_din1 0x3: Select gpio_120 0x4: Select usbb2_mm_txdat 0x5: Select uart4_rts 0x7: Select safe_mode	RW	0x7
15	ABE_DMIC_CLK1_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	ABE_DMIC_CLK1_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	ABE_DMIC_CLK1_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad abe_dmic_clk1 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
12	ABE_DMIC_CLK1_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad abe_dmic_clk1 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	ABE_DMIC_CLK1_OFFMODEOUTVALUE	OffMode mode output value for pad abe_dmic_clk1 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	ABE_DMIC_CLK1_OFFMODEOUTENABLE	OffMode mode output enable value for pad abe_dmic_clk1. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	ABE_DMIC_CLK1_OFFMODEENABLE	OffMode mode override control for pad abe_dmic_clk1 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	ABE_DMIC_CLK1_INPUTENABLE	Input enable value for pad abe_dmic_clk1 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	ABE_DMIC_CLK1_PULLTYPESELECT	pullup/down selection for pad abe_dmic_clk1 0x0: pulldown selected 0x1: pullup selected	RW	0
3	ABE_DMIC_CLK1_PULLUDENABLE	pullup/down enable for pad abe_dmic_clk1 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1

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Bits	Field Name	Description	Type	Reset
2:0	ABE_DMIC_CLK1_MUXMODE	Functional multiplexing selection for pad abe_dmic_clk1 0x0: Select abe_dmic_clk1 0x3: Select gpio_119 0x4: Select usbb2_mm_txse0 0x5: Select uart4_cts 0x7: Select safe_mode	RW	0x7

Table 18-453. Register Call Summary for Register CONTROL_CORE_PAD0_ABE_DMIC_CLK1_PAD1_ABE_DMIC_DIN1

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- SYSCTRL_PADCONF_CORE Register Summary: [2]

Table 18-454. CONTROL_CORE_PAD0_ABE_DMIC_DIN2_PAD1_ABE_DMIC_DIN3

Address Offset	0x0000 0114		
Physical Address	0x4A10 0114	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads abe_dmic_din2 and abe_dmic_din3 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ABE_DMIC_DIN3_WAKEUPEVENT	ABE_DMIC_DIN3_WAKEUPENABLE	ABE_DMIC_DIN3_OFFMODEPULLTYPESELECT	ABE_DMIC_DIN3_OFFMODEPULLUDENABLE	ABE_DMIC_DIN3_OFFMODEOUTVALUE	ABE_DMIC_DIN3_OFFMODEOUTENABLE	ABE_DMIC_DIN3_OFFMODEENABLE	ABE_DMIC_DIN3_INPUTENABLE	RESERVED			ABE_DMIC_DIN3_PULLTYPESELECT	ABE_DMIC_DIN3_PULLUDENABLE	ABE_DMIC_DIN3_MUXMODE			ABE_DMIC_DIN2_WAKEUPEVENT	ABE_DMIC_DIN2_WAKEUPENABLE	ABE_DMIC_DIN2_OFFMODEPULLTYPESELECT	ABE_DMIC_DIN2_OFFMODEPULLUDENABLE	ABE_DMIC_DIN2_OFFMODEOUTVALUE	ABE_DMIC_DIN2_OFFMODEOUTENABLE	ABE_DMIC_DIN2_OFFMODEENABLE	ABE_DMIC_DIN2_INPUTENABLE	RESERVED			ABE_DMIC_DIN2_PULLTYPESELECT	ABE_DMIC_DIN2_PULLUDENABLE	ABE_DMIC_DIN2_MUXMODE	

Bits	Field Name	Description	Type	Reset
31	ABE_DMIC_DIN3_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	ABE_DMIC_DIN3_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29	ABE_DMIC_DIN3_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad abe_dmic_din3 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0

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Bits	Field Name	Description	Type	Reset
28	ABE_DMIC_DIN3_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad abe_dmic_din3 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	ABE_DMIC_DIN3_OFFMODEOUTVALUE	OffMode mode output value for pad abe_dmic_din3 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	ABE_DMIC_DIN3_OFFMODEOUTENABLE	OffMode mode output enable value for pad abe_dmic_din3. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	ABE_DMIC_DIN3_OFFMODEENABLE	OffMode mode override control for pad abe_dmic_din3 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
24	ABE_DMIC_DIN3_INPUTENABLE	Input enable value for pad abe_dmic_din3 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	ABE_DMIC_DIN3_PULLTYPESELECT	pullup/down selection for pad abe_dmic_din3 0x0: pulldown selected 0x1: pullup selected	RW	0
19	ABE_DMIC_DIN3_PULLUDENABLE	pullup/down enable for pad abe_dmic_din3 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	ABE_DMIC_DIN3_MUXMODE	Functional multiplexing selection for pad abe_dmic_din3 0x0: Select abe_dmic_din3 0x1: Select slimbus2_data 0x2: Select abe_dmic_clk2 0x3: Select gpio_122 0x5: Select dmtimer9_pwm_evt 0x7: Select safe_mode	RW	0x7
15	ABE_DMIC_DIN2_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	ABE_DMIC_DIN2_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	ABE_DMIC_DIN2_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad abe_dmic_din2 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
12	ABE_DMIC_DIN2_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad abe_dmic_din2 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	ABE_DMIC_DIN2_OFFMODEOUTVALUE	OffMode mode output value for pad abe_dmic_din2 0x0: Set value at 0 0x1: Set value at 1	RW	0

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Bits	Field Name	Description	Type	Reset
10	ABE_DMIC_DIN2_OFFMODEOUTENABLE	OffMode mode output enable value for pad abe_dmic_din2. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	ABE_DMIC_DIN2_OFFMODEENABLE	OffMode mode override control for pad abe_dmic_din2 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	ABE_DMIC_DIN2_INPUTENABLE	Input enable value for pad abe_dmic_din2 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	ABE_DMIC_DIN2_PULLTYPESELECT	pullup/down selection for pad abe_dmic_din2 0x0: pulldown selected 0x1: pullup selected	RW	0
3	ABE_DMIC_DIN2_PULLUDENABLE	pullup/down enable for pad abe_dmic_din2 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	ABE_DMIC_DIN2_MUXMODE	Functional multiplexing selection for pad abe_dmic_din2 0x0: Select abe_dmic_din2 0x1: Select slimbus2_clock 0x2: Select abe_mcasp_axr 0x3: Select gpio_121 0x5: Select dmtimer11_pwm_evt 0x7: Select safe_mode	RW	0x7

Table 18-455. Register Call Summary for Register CONTROL_CORE_PAD0_ABE_DMIC_DIN2_PAD1_ABE_DMIC_DIN3

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- SYSCTRL_PADCONF_CORE Register Summary: [2]

Table 18-456. CONTROL_CORE_PAD0_UART2_CTS_PAD1_UART2_RTS

Address Offset	0x0000 0118		
Physical Address	0x4A10 0118	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads uart2_cts and uart2_rts Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UART2_RTS_WAKEUPEVENT	UART2_RTS_WAKEUPENABLE	UART2_RTS_OFFMODEPULLTYPESELECT	UART2_RTS_OFFMODEPULLUDENABLE	UART2_RTS_OFFMODEOUTVALUE	UART2_RTS_OFFMODEOUTENABLE	UART2_RTS_OFFMODEENABLE	UART2_RTS_INPUTENABLE	RESERVED			UART2_RTS_PULLTYPESELECT	UART2_RTS_PULLUDENABLE	UART2_RTS_MUXMODE			UART2_CTS_WAKEUPEVENT	UART2_CTS_WAKEUPENABLE	UART2_CTS_OFFMODEPULLTYPESELECT	UART2_CTS_OFFMODEPULLUDENABLE	UART2_CTS_OFFMODEOUTVALUE	UART2_CTS_OFFMODEOUTENABLE	UART2_CTS_OFFMODEENABLE	UART2_CTS_INPUTENABLE	RESERVED			UART2_CTS_PULLTYPESELECT	UART2_CTS_PULLUDENABLE	UART2_CTS_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	UART2_RTS_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	UART2_RTS_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29	UART2_RTS_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad uart2_rts 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
28	UART2_RTS_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad uart2_rts 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	UART2_RTS_OFFMODEOUTVALUE	OffMode mode output value for pad uart2_rts 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	UART2_RTS_OFFMODEOUTENABLE	OffMode mode output enable value for pad uart2_rts. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	UART2_RTS_OFFMODEENABLE	OffMode mode override control for pad uart2_rts 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
24	UART2_RTS_INPUTENABLE	Input enable value for pad uart2_rts 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	UART2_RTS_PULLTYPESELECT	pullup/down selection for pad uart2_rts 0x0: pulldown selected 0x1: pullup selected	RW	1
19	UART2_RTS_PULLUDENABLE	pullup/down enable for pad uart2_rts 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1

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Bits	Field Name	Description	Type	Reset
18:16	UART2_RTS_MUXMODE	Functional multiplexing selection for pad uart2_rts 0x0: Select uart2_rts 0x1: Select sdmmc3_cmd 0x3: Select gpio_124 0x7: Select safe_mode	RW	0x7
15	UART2_CTS_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	UART2_CTS_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	UART2_CTS_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad uart2_cts 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
12	UART2_CTS_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad uart2_cts 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	UART2_CTS_OFFMODEOUTVALUE	OffMode mode output value for pad uart2_cts 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	UART2_CTS_OFFMODEOUTENABLE	OffMode mode output enable value for pad uart2_cts. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	UART2_CTS_OFFMODEENABLE	OffMode mode override control for pad uart2_cts 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	UART2_CTS_INPUTENABLE	Input enable value for pad uart2_cts 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	UART2_CTS_PULLTYPESELECT	pullup/down selection for pad uart2_cts 0x0: pulldown selected 0x1: pullup selected	RW	1
3	UART2_CTS_PULLUDENABLE	pullup/down enable for pad uart2_cts 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	UART2_CTS_MUXMODE	Functional multiplexing selection for pad uart2_cts 0x0: Select uart2_cts 0x1: Select sdmmc3_clk 0x3: Select gpio_123 0x7: Select safe_mode	RW	0x7

Table 18-457. Register Call Summary for Register CONTROL_CORE_PAD0_UART2_CTS_PAD1_UART2_RTS

Control Module Functional Description

- Pad Multiplexing Register Fields: [0] [1]

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Table 18-457. Register Call Summary for Register CONTROL_CORE_PAD0_UART2_CTS_PAD1_UART2_RTS (continued)

Control Module Programming Guide
• Operational Modes Configuration: [2] [3] [4] [5] [6] [7] [8] [9]
Control Module Register Manual
• SYSCTRL_PADCONF_CORE Register Summary: [10]

Table 18-458. CONTROL_CORE_PAD0_UART2_RX_PAD1_UART2_TX

Address Offset	0x0000 011C		
Physical Address	0x4A10 011C	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads uart2_rx and uart2_tx Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UART2_TX_WAKEUPEVENT	UART2_TX_WAKEUPENABLE	UART2_TX_OFFMODEPULLTYPESELECT	UART2_TX_OFFMODEPULLUDENABLE	UART2_TX_OFFMODEOUTVALUE	UART2_TX_OFFMODEOUTENABLE	UART2_TX_OFFMODEENABLE	UART2_TX_INPUTENABLE	RESERVED			UART2_TX_PULLTYPESELECT	UART2_TX_PULLUDENABLE	UART2_TX_MUXMODE			UART2_RX_WAKEUPEVENT	UART2_RX_WAKEUPENABLE	UART2_RX_OFFMODEPULLTYPESELECT	UART2_RX_OFFMODEPULLUDENABLE	UART2_RX_OFFMODEOUTVALUE	UART2_RX_OFFMODEOUTENABLE	UART2_RX_OFFMODEENABLE	UART2_RX_INPUTENABLE	RESERVED			UART2_RX_PULLTYPESELECT	UART2_RX_PULLUDENABLE	UART2_RX_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	UART2_TX_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	UART2_TX_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29	UART2_TX_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad uart2_tx 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
28	UART2_TX_OFFMODEPULLUD ENABLE	OffMode mode pullup/down enable for pad uart2_tx 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	UART2_TX_OFFMODEOUTVAL UE	OffMode mode output value for pad uart2_tx 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	UART2_TX_OFFMODEOUTENA BLE	OffMode mode output enable value for pad uart2_tx. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0

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Bits	Field Name	Description	Type	Reset
25	UART2_TX_OFFMODEENABLE	OffMode mode override control for pad uart2_tx 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
24	UART2_TX_INPUTENABLE	Input enable value for pad uart2_tx 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	UART2_TX_PULLTYPESELECT	pullup/down selection for pad uart2_tx 0x0: pulldown selected 0x1: pullup selected	RW	1
19	UART2_TX_PULLUDENABLE	pullup/down enable for pad uart2_tx 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	UART2_TX_MUXMODE	Functional multiplexing selection for pad uart2_tx 0x0: Select uart2_tx 0x1: Select sdmmc3_dat1 0x3: Select gpio_126 0x7: Select safe_mode	RW	0x7
15	UART2_RX_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	UART2_RX_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	UART2_RX_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad uart2_rx 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
12	UART2_RX_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad uart2_rx 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	UART2_RX_OFFMODEOUTVALUE	OffMode mode output value for pad uart2_rx 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	UART2_RX_OFFMODEOUTENABLE	OffMode mode output enable value for pad uart2_rx. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	UART2_RX_OFFMODEENABLE	OffMode mode override control for pad uart2_rx 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	UART2_RX_INPUTENABLE	Input enable value for pad uart2_rx 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
4	UART2_RX_PULLTYPESELECT	pullup/down selection for pad uart2_rx 0x0: pulldown selected 0x1: pullup selected	RW	1
3	UART2_RX_PULLUDENABLE	pullup/down enable for pad uart2_rx 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	UART2_RX_MUXMODE	Functional multiplexing selection for pad uart2_rx 0x0: Select uart2_rx 0x1: Select sdmmc3_dat0 0x3: Select gpio_125 0x7: Select safe_mode	RW	0x7

Table 18-459. Register Call Summary for Register CONTROL_CORE_PAD0_UART2_RX_PAD1_UART2_TX

Control Module Functional Description • Pad Multiplexing Register Fields: [0] [1]
Control Module Programming Guide • Operational Modes Configuration: [2] [3] [4] [5] [6] [7] [8] [9]
Control Module Register Manual • SYSCTRL_PADCONF_CORE Register Summary: [10]

Table 18-460. CONTROL_CORE_PAD0_HDQ_SIO_PAD1_I2C1_SCL

Address Offset	0x0000 0120		
Physical Address	0x4A10 0120	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads hdq_sio and i2c1_scl Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I2C1_SCL_WAKEUPEVENT	I2C1_SCL_WAKEUPENABLE	RESERVED					I2C1_SCL_INPUTENABLE	RESERVED			I2C1_SCL_PULLTYPESELECT	I2C1_SCL_PULLUDENABLE	RESERVED			HDQ_SIO_WAKEUPEVENT	HDQ_SIO_WAKEUPENABLE	HDQ_SIO_OFFMODEPULLTYPESELECT	HDQ_SIO_OFFMODEPULLUDENABLE	HDQ_SIO_OFFMODEOUTVALUE	HDQ_SIO_OFFMODEOUTENABLE	HDQ_SIO_OFFMODEENABLE	HDQ_SIO_INPUTENABLE	RESERVED			HDQ_SIO_PULLTYPESELECT	HDQ_SIO_PULLUDENABLE	HDQ_SIO_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	I2C1_SCL_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0

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Bits	Field Name	Description	Type	Reset
30	I2C1_SCL_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x00
24	I2C1_SCL_INPUTENABLE	Input enable value for pad i2c1_scl 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	I2C1_SCL_PULLTYPESELECT	pullup/down selection for pad i2c1_scl 0x0: pulldown selected 0x1: pullup selected	RW	0
19	I2C1_SCL_PULLUDENABLE	pullup/down enable for pad i2c1_scl 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	0
18:16	RESERVED		R	0x0
15	HDQ_SIO_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	HDQ_SIO_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	HDQ_SIO_OFFMODEPULLTYPESELECT	OffMode mode Pull-Up/Down selection for pad hdq_sio 0x0: Offmode Pull-Down selected 0x1: Offmode Pull-Up selected	RW	0x0
12	HDQ_SIO_OFFMODEPULLUDENABLE	OffMode mode Pull-Up/Down enable for pad hdq_sio 0x0: Offmode Pull-Up/Down disabled 0x1: Offmode Pull-Up/Down enabled	RW	0x0
11	HDQ_SIO_OFFMODEOUTVALUE	OffMode mode output value for pad hdq_sio 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	HDQ_SIO_OFFMODEOUTENABLE	OffMode mode output enable value for pad hdq_sio. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	HDQ_SIO_OFFMODEENABLE	OffMode mode override control for pad hdq_sio 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	HDQ_SIO_INPUTENABLE	Input enable value for pad hdq_sio 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	HDQ_SIO_PULLTYPESELECT	Pull-Up/Down selection for pad hdq_sio 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0x0

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Bits	Field Name	Description	Type	Reset
3				HDQ_SIO_PULLTYPESELECT for pad hdq_sio
		0x0: Pull-Up/Down disabled		
		0x1: Pull-Up/Down enabled		
2:0	HDQ_SIO_MUXMODE	Functional multiplexing selection for pad hdq_sio	RW	0x7
		0x0: Select hdq_sio		
		0x1: Select i2c3_sccb		
		0x2: Select i2c2_sccb		
		0x3: Select gpio_127		
		0x7: Select safe_mode		

Table 18-461. Register Call Summary for Register CONTROL_CORE_PAD0_HDQ_SIO_PAD1_I2C1_SCL

Control Module Functional Description • Pad Multiplexing Register Fields: [0] [1]
Control Module Register Manual • SYSCTRL_PADCONF_CORE Register Summary: [2]

Table 18-462. CONTROL_CORE_PAD0_I2C1_SDA_PAD1_I2C2_SCL

Address Offset	0x0000 0124		
Physical Address	0x4A10 0124	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads i2c1_sda and i2c2_scl Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I2C2_SCL_WAKEUPEVENT	I2C2_SCL_WAKEUPENABLE	I2C2_SCL_OFFMODEPULLTYPESELECT	I2C2_SCL_OFFMODEPULLUDENABLE	I2C2_SCL_OFFMODEOUTVALUE	I2C2_SCL_OFFMODEOUTENABLE	I2C2_SCL_OFFMODEENABLE	I2C2_SCL_INPUTENABLE	RESERVED			I2C2_SCL_PULLTYPESELECT	I2C2_SCL_PULLUDENABLE	I2C2_SCL_MUXMODE			I2C1_SDA_WAKEUPEVENT	I2C1_SDA_WAKEUPENABLE	RESERVED					I2C1_SDA_INPUTENABLE	RESERVED				I2C1_SDA_PULLTYPESELECT	I2C1_SDA_PULLUDENABLE	RESERVED		

Bits	Field Name	Description	Type	Reset
31	I2C2_SCL_WAKEUPEVENT	Pad_x wake-up event status latched in the IO	R	0
		Read 0x0: No wake-up event occurred		
		Read 0x1: A wake-up event occurred		
30	I2C2_SCL_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value)	RW	0
		0x0: wake-up detection is disabled		
		0x1: wake-up detection is enabled		

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Bits	Field Name	Description	Type	Reset
29	I2C2_SCL_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad i2c2_scl 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
28	I2C2_SCL_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad i2c2_scl 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	I2C2_SCL_OFFMODEOUTVALUE	OffMode mode output value for pad i2c2_scl 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	I2C2_SCL_OFFMODEOUTENABLE	OffMode mode output enable value for pad i2c2_scl. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	I2C2_SCL_OFFMODEENABLE	OffMode mode override control for pad i2c2_scl 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
24	I2C2_SCL_INPUTENABLE	Input enable value for pad i2c2_scl 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	I2C2_SCL_PULLTYPESELECT	pullup/down selection for pad i2c2_scl 0x0: pulldown selected 0x1: pullup selected	RW	1
19	I2C2_SCL_PULLUDENABLE	pullup/down enable for pad i2c2_scl 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	I2C2_SCL_MUXMODE	Functional multiplexing selection for pad i2c2_scl 0x0: Select i2c2_scl 0x1: Select uart1_rx 0x3: Select gpio_128 0x7: Select safe_mode	RW	0x7
15	I2C1_SDA_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	I2C1_SDA_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x00
8	I2C1_SDA_INPUTENABLE	Input enable value for pad i2c1_sda 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	I2C1_SDA_PULLTYPESELECT	pullup/down selection for pad i2c1_sda 0x0: pulldown selected 0x1: pullup selected	RW	1

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Bits	Field Name	Description	Type	Reset
3	I2C1_SDA_PULLUDENABLE	pullup/down enable for pad i2c1_sda 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	RESERVED		R	0x0

Table 18-463. Register Call Summary for Register CONTROL_CORE_PAD0_I2C1_SDA_PAD1_I2C2_SCL

Control Module Functional Description • Pad Multiplexing Register Fields: [0] [1]
Control Module Register Manual • SYSCTRL_PADCONF_CORE Register Summary: [2]

Table 18-464. CONTROL_CORE_PAD0_I2C2_SDA_PAD1_I2C3_SCL

Address Offset	0x0000 0128		
Physical Address	0x4A10 0128	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads i2c2_sda and i2c3_scl Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I2C3_SCL_WAKEUPEVENT	I2C3_SCL_WAKEUPENABLE	I2C3_SCL_OFFMODEPULLTYPESELECT	I2C3_SCL_OFFMODEPULLUDENABLE	I2C3_SCL_OFFMODEOUTVALUE	I2C3_SCL_OFFMODEOUTENABLE	I2C3_SCL_OFFMODEENABLE	I2C3_SCL_INPUTENABLE	RESERVED			I2C3_SCL_PULLTYPESELECT	I2C3_SCL_PULLUDENABLE	I2C3_SCL_MUXMODE			I2C2_SDA_WAKEUPEVENT	I2C2_SDA_WAKEUPENABLE	I2C2_SDA_OFFMODEPULLTYPESELECT	I2C2_SDA_OFFMODEPULLUDENABLE	I2C2_SDA_OFFMODEOUTVALUE	I2C2_SDA_OFFMODEOUTENABLE	I2C2_SDA_OFFMODEENABLE	I2C2_SDA_INPUTENABLE	RESERVED			I2C2_SDA_PULLTYPESELECT	I2C2_SDA_PULLUDENABLE	I2C2_SDA_MUXMODE	

Bits	Field Name	Description	Type	Reset
31	I2C3_SCL_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	I2C3_SCL_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29	I2C3_SCL_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad i2c3_scl 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
28	I2C3_SCL_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad i2c3_scl 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0

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Bits	Field Name	Description	Type	Reset
27	I2C3_SCL_OFFMODEOUTVALUE	OffMode mode output value for pad i2c3_scl 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	I2C3_SCL_OFFMODEOUTENABLE	OffMode mode output enable value for pad i2c3_scl. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	I2C3_SCL_OFFMODEENABLE	OffMode mode override control for pad i2c3_scl 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
24	I2C3_SCL_INPUTENABLE	Input enable value for pad i2c3_scl 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	I2C3_SCL_PULLTYPESELECT	pullup/down selection for pad i2c3_scl 0x0: pulldown selected 0x1: pullup selected	RW	1
19	I2C3_SCL_PULLUDENABLE	pullup/down enable for pad i2c3_scl 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	I2C3_SCL_MUXMODE	Functional multiplexing selection for pad i2c3_scl 0x0: Select i2c3_scl 0x3: Select gpio_130 0x7: Select safe_mode	RW	0x7
15	I2C2_SDA_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	I2C2_SDA_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	I2C2_SDA_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad i2c2_sda 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
12	I2C2_SDA_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad i2c2_sda 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	I2C2_SDA_OFFMODEOUTVALUE	OffMode mode output value for pad i2c2_sda 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	I2C2_SDA_OFFMODEOUTENABLE	OffMode mode output enable value for pad i2c2_sda. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	I2C2_SDA_OFFMODEENABLE	OffMode mode override control for pad i2c2_sda 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0

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Bits	Field Name	Description	Type	Reset
8	I2C2_SDA_INPUTENABLE	Input enable value for pad i2c2_sda 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	I2C2_SDA_PULLTYPESELECT	pullup/down selection for pad i2c2_sda 0x0: pulldown selected 0x1: pullup selected	RW	1
3	I2C2_SDA_PULLUDENABLE	pullup/down enable for pad i2c2_sda 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	I2C2_SDA_MUXMODE	Functional multiplexing selection for pad i2c2_sda 0x0: Select i2c2_sda 0x1: Select uart1_tx 0x3: Select gpio_129 0x7: Select safe_mode	RW	0x7

Table 18-465. Register Call Summary for Register CONTROL_CORE_PAD0_I2C2_SDA_PAD1_I2C3_SCL

Control Module Functional Description • Pad Multiplexing Register Fields: [0] [1]
Control Module Register Manual • SYSCTRL_PADCONF_CORE Register Summary: [2]

Table 18-466. CONTROL_CORE_PAD0_I2C3_SDA_PAD1_I2C4_SCL

Address Offset	0x0000 012C		
Physical Address	0x4A10 012C	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads i2c3_sda and i2c4_scl Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I2C4_SCL_WAKEUPEVENT	I2C4_SCL_WAKEUPENABLE	I2C4_SCL_OFFMODEPULLTYPESELECT	I2C4_SCL_OFFMODEPULLUDENABLE	I2C4_SCL_OFFMODEOUTVALUE	I2C4_SCL_OFFMODEOUTENABLE	I2C4_SCL_OFFMODEENABLE	I2C4_SCL_INPUTENABLE	RESERVED			I2C4_SCL_PULLTYPESELECT	I2C4_SCL_PULLUDENABLE	I2C4_SCL_MUXMODE			I2C3_SDA_WAKEUPEVENT	I2C3_SDA_WAKEUPENABLE	I2C3_SDA_OFFMODEPULLTYPESELECT	I2C3_SDA_OFFMODEPULLUDENABLE	I2C3_SDA_OFFMODEOUTVALUE	I2C3_SDA_OFFMODEOUTENABLE	I2C3_SDA_OFFMODEENABLE	I2C3_SDA_INPUTENABLE	RESERVED			I2C3_SDA_PULLTYPESELECT	I2C3_SDA_PULLUDENABLE	I2C3_SDA_MUXMODE	

Bits	Field Name	Description	Type	Reset
31	I2C4_SCL_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0

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Bits	Field Name	Description	Type	Reset
30	I2C4_SCL_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29	I2C4_SCL_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad i2c4_scl 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
28	I2C4_SCL_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad i2c4_scl 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	I2C4_SCL_OFFMODEOUTVALUE	OffMode mode output value for pad i2c4_scl 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	I2C4_SCL_OFFMODEOUTENABLE	OffMode mode output enable value for pad i2c4_scl. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	I2C4_SCL_OFFMODEENABLE	OffMode mode override control for pad i2c4_scl 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
24	I2C4_SCL_INPUTENABLE	Input enable value for pad i2c4_scl 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	I2C4_SCL_PULLTYPESELECT	pullup/down selection for pad i2c4_scl 0x0: pulldown selected 0x1: pullup selected	RW	1
19	I2C4_SCL_PULLUDENABLE	pullup/down enable for pad i2c4_scl 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	I2C4_SCL_MUXMODE	Functional multiplexing selection for pad i2c4_scl 0x0: Select i2c4_scl 0x3: Select gpio_132 0x7: Select safe_mode	RW	0x7
15	I2C3_SDA_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	I2C3_SDA_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	I2C3_SDA_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad i2c3_sda 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
12	I2C3_SDA_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad i2c3_sda 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0

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Bits	Field Name	Description	Type	Reset
11	I2C3_SDA_OFFMODEOUTVALUE	OffMode mode output value for pad i2c3_sda 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	I2C3_SDA_OFFMODEOUTENABLE	OffMode mode output enable value for pad i2c3_sda. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	I2C3_SDA_OFFMODEENABLE	OffMode mode override control for pad i2c3_sda 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	I2C3_SDA_INPUTENABLE	Input enable value for pad i2c3_sda 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	I2C3_SDA_PULLTYPESELECT	pullup/down selection for pad i2c3_sda 0x0: pulldown selected 0x1: pullup selected	RW	1
3	I2C3_SDA_PULLUDENABLE	pullup/down enable for pad i2c3_sda 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	I2C3_SDA_MUXMODE	Functional multiplexing selection for pad i2c3_sda 0x0: Select i2c3_sda 0x3: Select gpio_131 0x7: Select safe_mode	RW	0x7

Table 18-467. Register Call Summary for Register CONTROL_CORE_PAD0_I2C3_SDA_PAD1_I2C4_SCL

Control Module Functional Description • Pad Multiplexing Register Fields: [0] [1]
Control Module Register Manual • SYSCTRL_PADCONF_CORE Register Summary: [2]

Table 18-468. CONTROL_CORE_PAD0_I2C4_SDA_PAD1_MCSPI1_CLK

Address Offset	0x0000 0130		
Physical Address	0x4A10 0130	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads i2c4_sda and mcspi1_clk Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MCSPI1_CLK_WAKEUPEVENT	MCSPI1_CLK_WAKEUPENABLE	MCSPI1_CLK_OFFMODEPULLTYPESELECT	MCSPI1_CLK_OFFMODEPULLUDENABLE	MCSPI1_CLK_OFFMODEOUTVALUE	MCSPI1_CLK_OFFMODEOUTENABLE	MCSPI1_CLK_OFFMODEENABLE	MCSPI1_CLK_INPUTENABLE	RESERVED			MCSPI1_CLK_PULLTYPESELECT	MCSPI1_CLK_PULLUDENABLE	MCSPI1_CLK_MUXMODE			I2C4_SDA_WAKEUPEVENT	I2C4_SDA_WAKEUPENABLE	I2C4_SDA_OFFMODEPULLTYPESELECT	I2C4_SDA_OFFMODEPULLUDENABLE	I2C4_SDA_OFFMODEOUTVALUE	I2C4_SDA_OFFMODEOUTENABLE	I2C4_SDA_OFFMODEENABLE	I2C4_SDA_INPUTENABLE	RESERVED			I2C4_SDA_PULLTYPESELECT	I2C4_SDA_PULLUDENABLE	I2C4_SDA_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	MCSPI1_CLK_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	MCSPI1_CLK_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29	MCSPI1_CLK_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad mcspi1_clk 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
28	MCSPI1_CLK_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad mcspi1_clk 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	MCSPI1_CLK_OFFMODEOUTVALUE	OffMode mode output value for pad mcspi1_clk 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	MCSPI1_CLK_OFFMODEOUTENABLE	OffMode mode output enable value for pad mcspi1_clk. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	MCSPI1_CLK_OFFMODEENABLE	OffMode mode override control for pad mcspi1_clk 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
24	MCSPI1_CLK_INPUTENABLE	Input enable value for pad mcspi1_clk 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	MCSPI1_CLK_PULLTYPESELECT	pullup/down selection for pad mcspi1_clk 0x0: pulldown selected 0x1: pullup selected	RW	0
19	MCSPI1_CLK_PULLUDENABLE	pullup/down enable for pad mcspi1_clk 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1

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Bits	Field Name	Description	Type	Reset
18:16	MCSPI1_ CLK_MUXMODE	Functional multiplexing selection for pad mcspi1_clk 0x0: Select mcspi1_clk 0x3: Select gpio_134 0x7: Select safe_mode	RW	0x7
15	I2C4_ SDA_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	I2C4_SDA_ WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	I2C4_SDA_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad i2c4_sda 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
12	I2C4_SDA_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad i2c4_sda 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	I2C4_SDA_ OFFMODEOUTVALUE	OffMode mode output value for pad i2c4_sda 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	I2C4_SDA_ OFFMODEOUTENABLE	OffMode mode output enable value for pad i2c4_sda. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	I2C4_SDA_ OFFMODEENABLE	OffMode mode override control for pad i2c4_sda 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	I2C4_SDA_ INPUTENABLE	Input enable value for pad i2c4_sda 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	I2C4_SDA_ PULLTYPESELECT	pullup/down selection for pad i2c4_sda 0x0: pulldown selected 0x1: pullup selected	RW	1
3	I2C4_SDA_ PULLUDENABLE	pullup/down enable for pad i2c4_sda 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	I2C4_SDA_ MUXMODE	Functional multiplexing selection for pad i2c4_sda 0x0: Select i2c4_sda 0x3: Select gpio_133 0x7: Select safe_mode	RW	0x7

Table 18-469. Register Call Summary for Register CONTROL_CORE_PAD0_I2C4_SDA_PAD1_MCSPI1_CLK

Control Module Functional Description • Pad Multiplexing Register Fields: [0] [1]
Control Module Register Manual • SYSCTRL_PADCONF_CORE Register Summary: [2]

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Table 18-470. CONTROL_CORE_PAD0_MCSPI1_SOMI_PAD1_MCSPI1_SIMO

Address Offset	0x0000 0134		
Physical Address	0x4A10 0134	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads mcspi1_somi and mcspi1_simo Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MCSPI1_SIMO_WAKEUPEVENT	MCSPI1_SIMO_WAKEUPENABLE	MCSPI1_SIMO_OFFMODEPULLTYPESELECT	MCSPI1_SIMO_OFFMODEPULLUDENABLE	MCSPI1_SIMO_OFFMODEOUTVALUE	MCSPI1_SIMO_OFFMODEOUTENABLE	MCSPI1_SIMO_OFFMODEENABLE	MCSPI1_SIMO_INPUTENABLE	RESERVED			MCSPI1_SIMO_PULLTYPESELECT	MCSPI1_SIMO_PULLUDENABLE	MCSPI1_SIMO_MUXMODE			MCSPI1_SOMI_WAKEUPEVENT	MCSPI1_SOMI_WAKEUPENABLE	MCSPI1_SOMI_OFFMODEPULLTYPESELECT	MCSPI1_SOMI_OFFMODEPULLUDENABLE	MCSPI1_SOMI_OFFMODEOUTVALUE	MCSPI1_SOMI_OFFMODEOUTENABLE	MCSPI1_SOMI_OFFMODEENABLE	MCSPI1_SOMI_INPUTENABLE	RESERVED			MCSPI1_SOMI_PULLTYPESELECT	MCSPI1_SOMI_PULLUDENABLE	MCSPI1_SOMI_MUXMODE	

Bits	Field Name	Description	Type	Reset
31	MCSPI1_SIMO_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	MCSPI1_SIMO_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29	MCSPI1_SIMO_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad mcspi1_simo 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
28	MCSPI1_SIMO_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad mcspi1_simo 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	MCSPI1_SIMO_OFFMODEOUTVALUE	OffMode mode output value for pad mcspi1_simo 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	MCSPI1_SIMO_OFFMODEOUTENABLE	OffMode mode output enable value for pad mcspi1_simo. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	MCSPI1_SIMO_OFFMODEENABLE	OffMode mode override control for pad mcspi1_simo 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0

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Bits	Field Name	Description	Type	Reset
24	MCSPI1_SIMO_ INPUTENABLE	Input enable value for pad mcspi1_simo 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	MCSPI1_SIMO_ PULLTYPESELECT	pullup/down selection for pad mcspi1_simo 0x0: pulldown selected 0x1: pullup selected	RW	0
19	MCSPI1_SIMO_ PULLUDENABLE	pullup/down enable for pad mcspi1_simo 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	MCSPI1_ SIMO_MUXMODE	Functional multiplexing selection for pad mcspi1_simo 0x0: Select mcspi1_simo 0x3: Select gpio_136 0x7: Select safe_mode	RW	0x7
15	MCSPI1_ SOMI_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	MCSPI1_ SOMI_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	MCSPI1_ SOMI_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad mcspi1_somi 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
12	MCSPI1_ SOMI_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad mcspi1_somi 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	MCSPI1_ SOMI_OFFMODEOUTVALUE	OffMode mode output value for pad mcspi1_somi 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	MCSPI1_ SOMI_OFFMODEOUTENABLE	OffMode mode output enable value for pad mcspi1_somi. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	MCSPI1_ SOMI_OFFMODEENABLE	OffMode mode override control for pad mcspi1_somi 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	MCSPI1_SOMI_ INPUTENABLE	Input enable value for pad mcspi1_somi 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	MCSPI1_SOMI_ PULLTYPESELECT	pullup/down selection for pad mcspi1_somi 0x0: pulldown selected 0x1: pullup selected	RW	0
3	MCSPI1_SOMI_ PULLUDENABLE	pullup/down enable for pad mcspi1_somi 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1

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Bits	Field Name	Description	Type	Reset
2:0	MCSPI1_SOMI_MUXMODE	Functional multiplexing selection for pad mcspi1_somi 0x0: Select mcspi1_somi 0x3: Select gpio_135 0x7: Select safe_mode	RW	0x7

Table 18-471. Register Call Summary for Register CONTROL_CORE_PAD0_MCSPI1_SOMI_PAD1_MCSPI1_SIMO

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- SYSCTRL_PADCONF_CORE Register Summary: [2]

Table 18-472. CONTROL_CORE_PAD0_MCSPI1_CS0_PAD1_MCSPI1_CS1

Address Offset	0x0000 0138		
Physical Address	0x4A10 0138	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads mcspi1_cs0 and mcspi1_cs1 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MCSPI1_CS1_WAKEUPEVENT	MCSPI1_CS1_WAKEUPENABLE	MCSPI1_CS1_OFFMODEPULLTYPESELECT	MCSPI1_CS1_OFFMODEPULLUDENABLE	MCSPI1_CS1_OFFMODEOUTVALUE	MCSPI1_CS1_OFFMODEOUTENABLE	MCSPI1_CS1_OFFMODEENABLE	MCSPI1_CS1_INPUTENABLE	RESERVED			MCSPI1_CS1_PULLTYPESELECT	MCSPI1_CS1_PULLUDENABLE	MCSPI1_CS1_MUXMODE			MCSPI1_CS0_WAKEUPEVENT	MCSPI1_CS0_WAKEUPENABLE	MCSPI1_CS0_OFFMODEPULLTYPESELECT	MCSPI1_CS0_OFFMODEPULLUDENABLE	MCSPI1_CS0_OFFMODEOUTVALUE	MCSPI1_CS0_OFFMODEOUTENABLE	MCSPI1_CS0_OFFMODEENABLE	MCSPI1_CS0_INPUTENABLE	RESERVED			MCSPI1_CS0_PULLTYPESELECT	MCSPI1_CS0_PULLUDENABLE	MCSPI1_CS0_MUXMODE	

Bits	Field Name	Description	Type	Reset
31	MCSPI1_CS1_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	MCSPI1_CS1_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29	MCSPI1_CS1_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad mcspi1_cs1 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
28	MCSPI1_CS1_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad mcspi1_cs1 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0

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Bits	Field Name	Description	Type	Reset
27	MCSPI1_CS1_OFFMODEOUTVALUE	OffMode mode output value for pad mcspi1_cs1 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	MCSPI1_CS1_OFFMODEOUTENABLE	OffMode mode output enable value for pad mcspi1_cs1. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	MCSPI1_CS1_OFFMODEENABLE	OffMode mode override control for pad mcspi1_cs1 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
24	MCSPI1_CS1_INPUTENABLE	Input enable value for pad mcspi1_cs1 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	MCSPI1_CS1_PULLTYPESELECT	pullup/down selection for pad mcspi1_cs1 0x0: pulldown selected 0x1: pullup selected	RW	0
19	MCSPI1_CS1_PULLUDENABLE	pullup/down enable for pad mcspi1_cs1 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	MCSPI1_CS1_MUXMODE	Functional multiplexing selection for pad mcspi1_cs1 0x0: Select mcspi1_cs1 0x1: Select uart1_rx 0x3: Select gpio_138 0x7: Select safe_mode	RW	0x7
15	MCSPI1_CS0_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	MCSPI1_CS0_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	MCSPI1_CS0_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad mcspi1_cs0 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
12	MCSPI1_CS0_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad mcspi1_cs0 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	MCSPI1_CS0_OFFMODEOUTVALUE	OffMode mode output value for pad mcspi1_cs0 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	MCSPI1_CS0_OFFMODEOUTENABLE	OffMode mode output enable value for pad mcspi1_cs0. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0

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Bits	Field Name	Description	Type	Reset
9	MCSPI1_CS0_OFFMODEENABLE	OffMode mode override control for pad mcspi1_cs0 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	MCSPI1_CS0_INPUTENABLE	Input enable value for pad mcspi1_cs0 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	MCSPI1_CS0_PULLTYPESELECT	pullup/down selection for pad mcspi1_cs0 0x0: pulldown selected 0x1: pullup selected	RW	0
3	MCSPI1_CS0_PULLUDENABLE	pullup/down enable for pad mcspi1_cs0 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	MCSPI1_CS0_MUXMODE	Functional multiplexing selection for pad mcspi1_cs0 0x0: Select mcspi1_cs0 0x3: Select gpio_137 0x7: Select safe_mode	RW	0x7

Table 18-473. Register Call Summary for Register CONTROL_CORE_PAD0_MCSPI1_CS0_PAD1_MCSPI1_CS1

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- SYSCTRL_PADCONF_CORE Register Summary: [2]

Table 18-474. CONTROL_CORE_PAD0_MCSPI1_CS2_PAD1_MCSPI1_CS3

Address Offset	0x0000 013C		
Physical Address	0x4A10 013C	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads mcspi1_cs2 and mcspi1_cs3 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MCSPI1_CS3_WAKEUPEVENT	MCSPI1_CS3_WAKEUPENABLE	MCSPI1_CS3_OFFMODEPULLTYPESELECT	MCSPI1_CS3_OFFMODEPULLUDENABLE	MCSPI1_CS3_OFFMODEOUTVALUE	MCSPI1_CS3_OFFMODEOUTENABLE	MCSPI1_CS3_OFFMODEENABLE	MCSPI1_CS3_INPUTENABLE	RESERVED			MCSPI1_CS3_PULLTYPESELECT	MCSPI1_CS3_PULLUDENABLE	MCSPI1_CS3_MUXMODE			MCSPI1_CS2_WAKEUPEVENT	MCSPI1_CS2_WAKEUPENABLE	MCSPI1_CS2_OFFMODEPULLTYPESELECT	MCSPI1_CS2_OFFMODEPULLUDENABLE	MCSPI1_CS2_OFFMODEOUTVALUE	MCSPI1_CS2_OFFMODEOUTENABLE	MCSPI1_CS2_OFFMODEENABLE	MCSPI1_CS2_INPUTENABLE	RESERVED			MCSPI1_CS2_PULLTYPESELECT	MCSPI1_CS2_PULLUDENABLE	MCSPI1_CS2_MUXMODE	

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Bits	Field Name	Description	Type	Reset
31	MCSPI1_CS3_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	MCSPI1_CS3_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29	MCSPI1_CS3_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad mcspi1_cs3 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
28	MCSPI1_CS3_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad mcspi1_cs3 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	MCSPI1_CS3_OFFMODEOUTVALUE	OffMode mode output value for pad mcspi1_cs3 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	MCSPI1_CS3_OFFMODEOUTENABLE	OffMode mode output enable value for pad mcspi1_cs3. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	MCSPI1_CS3_OFFMODEENABLE	OffMode mode override control for pad mcspi1_cs3 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
24	MCSPI1_CS3_INPUTENABLE	Input enable value for pad mcspi1_cs3 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	MCSPI1_CS3_PULLTYPESELECT	pullup/down selection for pad mcspi1_cs3 0x0: pulldown selected 0x1: pullup selected	RW	1
19	MCSPI1_CS3_PULLUDENABLE	pullup/down enable for pad mcspi1_cs3 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	MCSPI1_CS3_MUXMODE	Functional multiplexing selection for pad mcspi1_cs3 0x0: Select mcspi1_cs3 0x1: Select uart1_rts 0x2: Select slimbus2_data 0x3: Select gpio_140 0x7: Select safe_mode	RW	0x7
15	MCSPI1_CS2_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	MCSPI1_CS2_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	MCSPI1_CS2_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad mcspi1_cs2 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0

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Bits	Field Name	Description	Type	Reset
12	MCSPI1_CS2_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad mcspi1_cs2 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	MCSPI1_CS2_OFFMODEOUTVALUE	OffMode mode output value for pad mcspi1_cs2 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	MCSPI1_CS2_OFFMODEOUTENABLE	OffMode mode output enable value for pad mcspi1_cs2. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	MCSPI1_CS2_OFFMODEENABLE	OffMode mode override control for pad mcspi1_cs2 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	MCSPI1_CS2_INPUTENABLE	Input enable value for pad mcspi1_cs2 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	MCSPI1_CS2_PULLTYPESELECT	pullup/down selection for pad mcspi1_cs2 0x0: pulldown selected 0x1: pullup selected	RW	1
3	MCSPI1_CS2_PULLUDENABLE	pullup/down enable for pad mcspi1_cs2 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	MCSPI1_CS2_MUXMODE	Functional multiplexing selection for pad mcspi1_cs2 0x0: Select mcspi1_cs2 0x1: Select uart1_cts 0x2: Select slimbus2_clock 0x3: Select gpio_139 0x7: Select safe_mode	RW	0x7

Table 18-475. Register Call Summary for Register CONTROL_CORE_PAD0_MCSPI1_CS2_PAD1_MCSPI1_CS3

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- SYSCTRL_PADCONF_CORE Register Summary: [2]

Table 18-476. CONTROL_CORE_PAD0_UART3_CTS_RCTX_PAD1_UART3_RTS_SD

Address Offset	0x0000 0140		
Physical Address	0x4A10 0140	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads uart3_cts_rctx and uart3_rts_sd Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UART3_RTS_SD_WAKEUPEVENT	UART3_RTS_SD_WAKEUPENABLE	UART3_RTS_SD_OFFMODEPULLTYPESELECT	UART3_RTS_SD_OFFMODEPULLUDENABLE	UART3_RTS_SD_OFFMODEOUTVALUE	UART3_RTS_SD_OFFMODEOUTENABLE	UART3_RTS_SD_OFFMODEENABLE	UART3_RTS_SD_INPUTENABLE	RESERVED			UART3_RTS_SD_PULLTYPESELECT	UART3_RTS_SD_PULLUDENABLE	UART3_RTS_SD_MUXMODE			UART3_CTS_RCTX_WAKEUPEVENT	UART3_CTS_RCTX_WAKEUPENABLE	UART3_CTS_RCTX_OFFMODEPULLTYPESELECT	UART3_CTS_RCTX_OFFMODEPULLUDENABLE	UART3_CTS_RCTX_OFFMODEOUTVALUE	UART3_CTS_RCTX_OFFMODEOUTENABLE	UART3_CTS_RCTX_OFFMODEENABLE	UART3_CTS_RCTX_INPUTENABLE	RESERVED			UART3_CTS_RCTX_PULLTYPESELECT	UART3_CTS_RCTX_PULLUDENABLE	UART3_CTS_RCTX_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	UART3_RTS_SD_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	UART3_RTS_SD_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29	UART3_RTS_SD_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad uart3_rts_sd 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
28	UART3_RTS_SD_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad uart3_rts_sd 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	UART3_RTS_SD_OFFMODEOUTVALUE	OffMode mode output value for pad uart3_rts_sd 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	UART3_RTS_SD_OFFMODEOUTENABLE	OffMode mode output enable value for pad uart3_rts_sd. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	UART3_RTS_SD_OFFMODEENABLE	OffMode mode override control for pad uart3_rts_sd 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
24	UART3_RTS_SD_INPUTENABLE	Input enable value for pad uart3_rts_sd 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	UART3_RTS_SD_PULLTYPESELECT	pullup/down selection for pad uart3_rts_sd 0x0: pulldown selected 0x1: pullup selected	RW	1

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Bits	Field Name	Description	Type	Reset
19	UART3_RTS_SD_PULLUDENABLE	pullup/down enable for pad uart3_rts_sd 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	UART3_RTS_SD_MUXMODE	Functional multiplexing selection for pad uart3_rts_sd 0x0: Select uart3_rts_sd 0x2: Select cam_globalreset 0x3: Select gpio_142 0x7: Select safe_mode	RW	0x7
15	UART3_CTS_RCTX_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	UART3_CTS_RCTX_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	UART3_CTS_RCTX_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad uart3_cts_rctx 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
12	UART3_CTS_RCTX_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad uart3_cts_rctx 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	UART3_CTS_RCTX_OFFMODEOUTVALUE	OffMode mode output value for pad uart3_cts_rctx 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	UART3_CTS_RCTX_OFFMODEOUTENABLE	OffMode mode output enable value for pad uart3_cts_rctx. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	UART3_CTS_RCTX_OFFMODEENABLE	OffMode mode override control for pad uart3_cts_rctx 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	UART3_CTS_RCTX_INPUTENABLE	Input enable value for pad uart3_cts_rctx 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	UART3_CTS_RCTX_PULLTYPESELECT	pullup/down selection for pad uart3_cts_rctx 0x0: pulldown selected 0x1: pullup selected	RW	1
3	UART3_CTS_RCTX_PULLUDENABLE	pullup/down enable for pad uart3_cts_rctx 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	UART3_CTS_RCTX_MUXMODE	Functional multiplexing selection for pad uart3_cts_rctx 0x0: Select uart3_cts_rctx 0x1: Select uart1_tx 0x3: Select gpio_141 0x7: Select safe_mode	RW	0x7

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Table 18-477. Register Call Summary for Register CONTROL_CORE_PAD0_UART3_CTS_RCTX_PAD1_UART3_RTS_SD

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- SYSCTRL_PADCONF_CORE Register Summary: [2]

Table 18-478. CONTROL_CORE_PAD0_UART3_RX_IRRX_PAD1_UART3_TX_IRTX

Address Offset	0x0000 0144		
Physical Address	0x4A10 0144	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads uart3_rx_irrx and uart3_tx_irtx Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UART3_TX_IRTX_WAKEUPEVENT	UART3_TX_IRTX_WAKEUPENABLE	UART3_TX_IRTX_OFFMODEPULLTYPESELECT	UART3_TX_IRTX_OFFMODEPULLUDENABLE	UART3_TX_IRTX_OFFMODEOUTVALUE	UART3_TX_IRTX_OFFMODEOUTENABLE	UART3_TX_IRTX_OFFMODEENABLE	UART3_TX_IRTX_INPUTENABLE	RESERVED			UART3_TX_IRTX_PULLTYPESELECT	UART3_TX_IRTX_PULLUDENABLE	UART3_TX_IRTX_MUXMODE			UART3_RX_IRRX_WAKEUPEVENT	UART3_RX_IRRX_WAKEUPENABLE	UART3_RX_IRRX_OFFMODEPULLTYPESELECT	UART3_RX_IRRX_OFFMODEPULLUDENABLE	UART3_RX_IRRX_OFFMODEOUTVALUE	UART3_RX_IRRX_OFFMODEOUTENABLE	UART3_RX_IRRX_OFFMODEENABLE	UART3_RX_IRRX_INPUTENABLE	RESERVED			UART3_RX_IRRX_PULLTYPESELECT	UART3_RX_IRRX_PULLUDENABLE	UART3_RX_IRRX_MUXMODE	

Bits	Field Name	Description	Type	Reset
31	UART3_TX_IRTX_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	UART3_TX_IRTX_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29	UART3_TX_IRTX_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad uart3_tx_irtx 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
28	UART3_TX_IRTX_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad uart3_tx_irtx 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	UART3_TX_IRTX_OFFMODEOUTVALUE	OffMode mode output value for pad uart3_tx_irtx 0x0: Set value at 0 0x1: Set value at 1	RW	0

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Bits	Field Name	Description	Type	Reset
26	UART3_TX_IRTX_OFFMODEOUTENABLE	OffMode mode output enable value for pad uart3_tx_irtx. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	UART3_TX_IRTX_OFFMODEENABLE	OffMode mode override control for pad uart3_tx_irtx 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
24	UART3_TX_IRTX_INPUTENABLE	Input enable value for pad uart3_tx_irtx 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	UART3_TX_IRTX_PULLTYPESELECT	pullup/down selection for pad uart3_tx_irtx 0x0: pulldown selected 0x1: pullup selected	RW	1
19	UART3_TX_IRTX_PULLUDENABLE	pullup/down enable for pad uart3_tx_irtx 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	UART3_TX_IRTX_MUXMODE	Functional multiplexing selection for pad uart3_tx_irtx 0x0: Select uart3_tx_irtx 0x1: Select dmtimer9_pwm_evt 0x2: Select cam_strobe 0x3: Select gpio_144 0x7: Select safe_mode	RW	0x7
15	UART3_RX_IRRX_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	UART3_RX_IRRX_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	UART3_RX_IRRX_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad uart3_rx_irrx 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
12	UART3_RX_IRRX_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad uart3_rx_irrx 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	UART3_RX_IRRX_OFFMODEOUTVALUE	OffMode mode output value for pad uart3_rx_irrx 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	UART3_RX_IRRX_OFFMODEOUTENABLE	OffMode mode output enable value for pad uart3_rx_irrx. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	UART3_RX_IRRX_OFFMODEENABLE	OffMode mode override control for pad uart3_rx_irrx 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0

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Bits	Field Name	Description	Type	Reset
8	UART3_RX_IRRX_INPUTENABLE	Input enable value for pad uart3_rx_irrx 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	UART3_RX_IRRX_PULLTYPESELECT	pullup/down selection for pad uart3_rx_irrx 0x0: pulldown selected 0x1: pullup selected	RW	1
3	UART3_RX_IRRX_PULLUDENABLE	pullup/down enable for pad uart3_rx_irrx 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	UART3_RX_IRRX_MUXMODE	Functional multiplexing selection for pad uart3_rx_irrx 0x0: Select uart3_rx_irrx 0x1: Select dmtimer8_pwm_evt 0x2: Select cam_shutter 0x3: Select gpio_143 0x7: Select safe_mode	RW	0x7

Table 18-479. Register Call Summary for Register CONTROL_CORE_PAD0_UART3_RX_IRRX_PAD1_UART3_TX_IRTX

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- SYSCTRL_PADCONF_CORE Register Summary: [2]

Table 18-480. CONTROL_CORE_PAD0_SDMMC5_CLK_PAD1_SDMMC5_CMD

Address Offset	0x0000 0148		
Physical Address	0x4A10 0148	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads sdmmc5_clk and sdmmc5_cmd Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SDMMC5_CMD_WAKEUPEVENT	SDMMC5_CMD_WAKEUPENABLE	SDMMC5_CMD_OFFMODEPULLTYPESELECT	SDMMC5_CMD_OFFMODEPULLUDENABLE	SDMMC5_CMD_OFFMODEOUTVALUE	SDMMC5_CMD_OFFMODEOUTENABLE	SDMMC5_CMD_OFFMODEENABLE	SDMMC5_CMD_INPUTENABLE	RESERVED			SDMMC5_CMD_PULLTYPESELECT	SDMMC5_CMD_PULLUDENABLE	SDMMC5_CMD_MUXMODE			SDMMC5_CLK_WAKEUPEVENT	SDMMC5_CLK_WAKEUPENABLE	SDMMC5_CLK_OFFMODEPULLTYPESELECT	SDMMC5_CLK_OFFMODEPULLUDENABLE	SDMMC5_CLK_OFFMODEOUTVALUE	SDMMC5_CLK_OFFMODEOUTENABLE	SDMMC5_CLK_OFFMODEENABLE	SDMMC5_CLK_INPUTENABLE	RESERVED			SDMMC5_CLK_PULLTYPESELECT	SDMMC5_CLK_PULLUDENABLE	SDMMC5_CLK_MUXMODE		

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Bits	Field Name	Description	Type	Reset
31	SDMMC5_CMD _WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	SDMMC5_CMD _WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29	SDMMC5_CMD_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad sdmmc5_cmd 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
28	SDMMC5_CMD_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad sdmmc5_cmd 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	SDMMC5_CMD_OFFMODEOUTVALUE	OffMode mode output value for pad sdmmc5_cmd 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	SDMMC5_CMD_OFFMODEOUTENABLE	OffMode mode output enable value for pad sdmmc5_cmd. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	SDMMC5_CMD_OFFMODEENABLE	OffMode mode override control for pad sdmmc5_cmd 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
24	SDMMC5_CMD_INPUTENABLE	Input enable value for pad sdmmc5_cmd 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	SDMMC5_CMD _PULLTYPESELECT	pullup/down selection for pad sdmmc5_cmd 0x0: pulldown selected 0x1: pullup selected	RW	1
19	SDMMC5_CMD _PULLUDENABLE	pullup/down enable for pad sdmmc5_cmd 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	SDMMC5_CMD_MUXMODE	Functional multiplexing selection for pad sdmmc5_cmd 0x0: Select sdmmc5_cmd 0x1: Select mcspi2_simo 0x2: Select usbc1_icusb_dm 0x3: Select gpio_146 0x5: Select sdmmc2_cmd 0x7: Select safe_mode	RW	0x7
15	SDMMC5_ CLK_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	SDMMC5_ CLK_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0

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Bits	Field Name	Description	Type	Reset
13	SDMMC5_CLK_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad sdmmc5_clk 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
12	SDMMC5_CLK_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad sdmmc5_clk 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	SDMMC5_CLK_OFFMODEOUTVALUE	OffMode mode output value for pad sdmmc5_clk 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	SDMMC5_CLK_OFFMODEOUTENABLE	OffMode mode output enable value for pad sdmmc5_clk. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	SDMMC5_CLK_OFFMODEENABLE	OffMode mode override control for pad sdmmc5_clk 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	SDMMC5_CLK_INPUTENABLE	Input enable value for pad sdmmc5_clk 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	SDMMC5_CLK_PULLTYPESELECT	pullup/down selection for pad sdmmc5_clk 0x0: pulldown selected 0x1: pullup selected	RW	0
3	SDMMC5_CLK_PULLUDENABLE	pullup/down enable for pad sdmmc5_clk 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	SDMMC5_CLK_MUXMODE	Functional multiplexing selection for pad sdmmc5_clk 0x0: Select sdmmc5_clk 0x1: Select mcspi2_clk 0x2: Select usbc1_icusb_dp 0x3: Select gpio_145 0x5: Select sdmmc2_clk 0x7: Select safe_mode	RW	0x7

Table 18-481. Register Call Summary for Register CONTROL_CORE_PAD0_SDMMC5_CLK_PAD1_SDMMC5_CMD

Control Module Functional Description • Pad Multiplexing Register Fields: [0] [1]
Control Module Register Manual • SYSCTRL_PADCONF_CORE Register Summary: [2]

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Table 18-482. CONTROL_CORE_PAD0_SDMMC5_DAT0_PAD1_SDMMC5_DAT1

Address Offset	0x0000 014C		
Physical Address	0x4A10 014C	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads sdmmc5_dat0 and sdmmc5_dat1 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SDMMC5_DAT1_WAKEUPEVENT	SDMMC5_DAT1_WAKEUPENABLE	SDMMC5_DAT1_OFFMODEPULLTYPESELECT	SDMMC5_DAT1_OFFMODEPULLUDENABLE	SDMMC5_DAT1_OFFMODEOUTVALUE	SDMMC5_DAT1_OFFMODEOUTENABLE	SDMMC5_DAT1_OFFMODEENABLE	SDMMC5_DAT1_INPUTENABLE	RESERVED			SDMMC5_DAT1_PULLTYPESELECT	SDMMC5_DAT1_PULLUDENABLE	SDMMC5_DAT1_MUXMODE			SDMMC5_DAT0_WAKEUPEVENT	SDMMC5_DAT0_WAKEUPENABLE	SDMMC5_DAT0_OFFMODEPULLTYPESELECT	SDMMC5_DAT0_OFFMODEPULLUDENABLE	SDMMC5_DAT0_OFFMODEOUTVALUE	SDMMC5_DAT0_OFFMODEOUTENABLE	SDMMC5_DAT0_OFFMODEENABLE	SDMMC5_DAT0_INPUTENABLE	RESERVED			SDMMC5_DAT0_PULLTYPESELECT	SDMMC5_DAT0_PULLUDENABLE	SDMMC5_DAT0_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	SDMMC5_DAT1_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	SDMMC5_DAT1_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29	SDMMC5_DAT1_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad sdmmc5_dat1 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
28	SDMMC5_DAT1_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad sdmmc5_dat1 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	SDMMC5_DAT1_OFFMODEOUTVALUE	OffMode mode output value for pad sdmmc5_dat1 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	SDMMC5_DAT1_OFFMODEOUTENABLE	OffMode mode output enable value for pad sdmmc5_dat1. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	SDMMC5_DAT1_OFFMODEENABLE	OffMode mode override control for pad sdmmc5_dat1 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0

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Bits	Field Name	Description	Type	Reset
24	SDMMC5_DAT1_ INPUTENABLE	Input enable value for pad sdmmc5_dat1 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	SDMMC5_DAT1_ PULLTYPESELECT	pullup/down selection for pad sdmmc5_dat1 0x0: pulldown selected 0x1: pullup selected	RW	1
19	SDMMC5_DAT1_ PULLUDENABLE	pullup/down enable for pad sdmmc5_dat1 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	SDMMC5_DAT1_ MUXMODE	Functional multiplexing selection for pad sdmmc5_dat1 0x0: Select sdmmc5_dat1 0x2: Select usbc1_icusb_txen 0x3: Select gpio_148 0x5: Select sdmmc2_dat1 0x7: Select safe_mode	RW	0x7
15	SDMMC5_DAT0_ WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	SDMMC5_DAT0_ WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	SDMMC5_DAT0_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad sdmmc5_dat0 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
12	SDMMC5_DAT0_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad sdmmc5_dat0 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	SDMMC5_DAT0_ OFFMODEOUTVALUE	OffMode mode output value for pad sdmmc5_dat0 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	SDMMC5_DAT0_ OFFMODEOUTENABLE	OffMode mode output enable value for pad sdmmc5_dat0. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	SDMMC5_DAT0_ OFFMODEENABLE	OffMode mode override control for pad sdmmc5_dat0 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	SDMMC5_DAT0_ INPUTENABLE	Input enable value for pad sdmmc5_dat0 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	SDMMC5_DAT0_ PULLTYPESELECT	pullup/down selection for pad sdmmc5_dat0 0x0: pulldown selected 0x1: pullup selected	RW	1

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Bits	Field Name	Description	Type	Reset
3	SDMMC5_DAT0_PULLUDENABLE	pullup/down enable for pad sdmmc5_dat0 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	SDMMC5_DAT0_MUXMODE	Functional multiplexing selection for pad sdmmc5_dat0 0x0: Select sdmmc5_dat0 0x1: Select mcspi2_somi 0x2: Select usbc1_icusb_rcv 0x3: Select gpio_147 0x5: sdmmc2_dat0 0x7: Select safe_mode	RW	0x7

Table 18-483. Register Call Summary for Register CONTROL_CORE_PAD0_SDMMC5_DAT0_PAD1_SDMMC5_DAT1

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- SYSCTRL_PADCONF_CORE Register Summary: [2]

Table 18-484. CONTROL_CORE_PAD0_SDMMC5_DAT2_PAD1_SDMMC5_DAT3

Address Offset	0x0000 0150		
Physical Address	0x4A10 0150	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads sdmmc5_dat2 and sdmmc5_dat3 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SDMMC5_DAT3_WAKEUPEVENT	SDMMC5_DAT3_WAKEUPENABLE	SDMMC5_DAT3_OFFMODEPULLTYPESELECT	SDMMC5_DAT3_OFFMODEPULLUDENABLE	SDMMC5_DAT3_OFFMODEOUTVALUE	SDMMC5_DAT3_OFFMODEOUTENABLE	SDMMC5_DAT3_OFFMODEENABLE	SDMMC5_DAT3_INPUTENABLE	RESERVED			SDMMC5_DAT3_PULLTYPESELECT	SDMMC5_DAT3_PULLUDENABLE	SDMMC5_DAT3_MUXMODE			SDMMC5_DAT2_WAKEUPEVENT	SDMMC5_DAT2_WAKEUPENABLE	SDMMC5_DAT2_OFFMODEPULLTYPESELECT	SDMMC5_DAT2_OFFMODEPULLUDENABLE	SDMMC5_DAT2_OFFMODEOUTVALUE	SDMMC5_DAT2_OFFMODEOUTENABLE	SDMMC5_DAT2_OFFMODEENABLE	SDMMC5_DAT2_INPUTENABLE	RESERVED			SDMMC5_DAT2_PULLTYPESELECT	SDMMC5_DAT2_PULLUDENABLE	SDMMC5_DAT2_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	SDMMC5_DAT3_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	SDMMC5_DAT3_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0

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Bits	Field Name	Description	Type	Reset
29	SDMMC5_DAT3_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad sdmmc5_dat3 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
28	SDMMC5_DAT3_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad sdmmc5_dat3 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	SDMMC5_DAT3_ OFFMODEOUTVALUE	OffMode mode output value for pad sdmmc5_dat3 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	SDMMC5_DAT3_ OFFMODEOUTENABLE	OffMode mode output enable value for pad sdmmc5_dat3. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	SDMMC5_DAT3_ OFFMODEENABLE	OffMode mode override control for pad sdmmc5_dat3 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
24	SDMMC5_DAT3_ INPUTENABLE	Input enable value for pad sdmmc5_dat3 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	SDMMC5_DAT3_ PULLTYPESELECT	pullup/down selection for pad sdmmc5_dat3 0x0: pulldown selected 0x1: pullup selected	RW	1
19	SDMMC5_DAT3_ PULLUDENABLE	pullup/down enable for pad sdmmc5_dat3 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	SDMMC5_DAT3_ MUXMODE	Functional multiplexing selection for pad sdmmc5_dat3 0x0: Select sdmmc5_dat3 0x1: Select mcspi2_cs0 0x3: Select gpio_150 0x5: Select sdmmc2_dat3 0x7: Select safe_mode	RW	0x7
15	SDMMC5_DAT2_ WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	SDMMC5_DAT2_ WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	SDMMC5_DAT2_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad sdmmc5_dat2 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
12	SDMMC5_DAT2_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad sdmmc5_dat2 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0

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Bits	Field Name	Description	Type	Reset
11	SDMMC5_DAT2_ OFFMODEOUTVALUE	OffMode mode output value for pad sdmmc5_dat2 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	SDMMC5_DAT2_ OFFMODEOUTENABLE	OffMode mode output enable value for pad sdmmc5_dat2. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	SDMMC5_DAT2_ OFFMODEENABLE	OffMode mode override control for pad sdmmc5_dat2 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	SDMMC5_DAT2_ INPUTENABLE	Input enable value for pad sdmmc5_dat2 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	SDMMC5_DAT2_ PULLTYPESELECT	pullup/down selection for pad sdmmc5_dat2 0x0: pulldown selected 0x1: pullup selected	RW	1
3	SDMMC5_DAT2_ PULLUDENABLE	pullup/down enable for pad sdmmc5_dat2 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	SDMMC5_DAT2_ MUXMODE	Functional multiplexing selection for pad sdmmc5_dat2 0x0: Select sdmmc5_dat2 0x1: Select mcspi2_cs1 0x3: Select gpio_149 0x5: Select sdmmc2_dat2 0x7: Select safe_mode	RW	0x7

Table 18-485. Register Call Summary for Register CONTROL_CORE_PAD0_SDMMC5_DAT2_PAD1_SDMMC5_DAT3

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- SYSCTRL_PADCONF_CORE Register Summary: [2]

Table 18-486. CONTROL_CORE_PAD0_MCSPI4_CLK_PAD1_MCSPI4_SIMO

Address Offset	0x0000 0154		
Physical Address	0x4A10 0154	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads mcspi4_clk and mcspi4_simo Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MCSPI4_SIMO_WAKEUPEVENT	MCSPI4_SIMO_WAKEUPENABLE	MCSPI4_SIMO_OFFMODEPULLTYPESELECT	MCSPI4_SIMO_OFFMODEPULLUDENABLE	MCSPI4_SIMO_OFFMODEOUTVALUE	MCSPI4_SIMO_OFFMODEOUTENABLE	MCSPI4_SIMO_OFFMODEENABLE	MCSPI4_SIMO_INPUTENABLE	RESERVED			MCSPI4_SIMO_PULLTYPESELECT	MCSPI4_SIMO_PULLUDENABLE	MCSPI4_SIMO_MUXMODE			MCSPI4_CLK_WAKEUPEVENT	MCSPI4_CLK_WAKEUPENABLE	MCSPI4_CLK_OFFMODEPULLTYPESELECT	MCSPI4_CLK_OFFMODEPULLUDENABLE	MCSPI4_CLK_OFFMODEOUTVALUE	MCSPI4_CLK_OFFMODEOUTENABLE	MCSPI4_CLK_OFFMODEENABLE	MCSPI4_CLK_INPUTENABLE	RESERVED			MCSPI4_CLK_PULLTYPESELECT	MCSPI4_CLK_PULLUDENABLE	MCSPI4_CLK_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	MCSPI4_SIMO_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	MCSPI4_SIMO_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29	MCSPI4_SIMO_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad mcspi4_simo 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
28	MCSPI4_SIMO_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad mcspi4_simo 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	MCSPI4_SIMO_OFFMODEOUTVALUE	OffMode mode output value for pad mcspi4_simo 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	MCSPI4_SIMO_OFFMODEOUTENABLE	OffMode mode output enable value for pad mcspi4_simo. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	MCSPI4_SIMO_OFFMODEENABLE	OffMode mode override control for pad mcspi4_simo 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
24	MCSPI4_SIMO_INPUTENABLE	Input enable value for pad mcspi4_simo 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	MCSPI4_SIMO_PULLTYPESELECT	pullup/down selection for pad mcspi4_simo 0x0: pulldown selected 0x1: pullup selected	RW	1

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Bits	Field Name	Description	Type	Reset
19	MCSPI4_SIMO_ PULLUDENABLE	pullup/down enable for pad mcspi4_simo 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	MCSPI4_SIMO_ MUXMODE	Functional multiplexing selection for pad mcspi4_simo 0x0: Select mcspi4_simo 0x1: Select sdmmc4_cmd 0x2: Select kpd_col7 0x3: Select gpio_152 0x7: Select safe_mode	RW	0x7
15	MCSPI4_CLK_ WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	MCSPI4_CLK_ WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	MCSPI4_CLK_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad mcspi4_clk 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
12	MCSPI4_CLK_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad mcspi4_clk 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	MCSPI4_CLK_ OFFMODEOUTVALUE	OffMode mode output value for pad mcspi4_clk 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	MCSPI4_CLK_ OFFMODEOUTENABLE	OffMode mode output enable value for pad mcspi4_clk. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	MCSPI4_CLK_ OFFMODEENABLE	OffMode mode override control for pad mcspi4_clk 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	MCSPI4_CLK_ INPUTENABLE	Input enable value for pad mcspi4_clk 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	MCSPI4_CLK_ PULLTYPESELECT	pullup/down selection for pad mcspi4_clk 0x0: pulldown selected 0x1: pullup selected	RW	0
3	MCSPI4_CLK_ PULLUDENABLE	pullup/down enable for pad mcspi4_clk 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	MCSPI4_CLK_ MUXMODE	Functional multiplexing selection for pad mcspi4_clk 0x0: Select mcspi4_clk 0x1: Select sdmmc4_clk 0x2: Select kpd_col6 0x3: Select gpio_151 0x7: Select safe_mode	RW	0x7

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Table 18-487. Register Call Summary for Register CONTROL_CORE_PAD0_MCSPI4_CLK_PAD1_MCSPI4_SIMO

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- SYSCTRL_PADCONF_CORE Register Summary: [2]

Table 18-488. CONTROL_CORE_PAD0_MCSPI4_SOMI_PAD1_MCSPI4_CS0

Address Offset	0x0000 0158		
Physical Address	0x4A10 0158	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads mcspi4_somi and mcspi4_cs0 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MCSPI4_CS0_WAKEUPEVENT	MCSPI4_CS0_WAKEUPENABLE	MCSPI4_CS0_OFFMODEPULLTYPESELECT	MCSPI4_CS0_OFFMODEPULLUDENABLE	MCSPI4_CS0_OFFMODEOUTVALUE	MCSPI4_CS0_OFFMODEOUTENABLE	MCSPI4_CS0_OFFMODEENABLE	MCSPI4_CS0_INPUTENABLE	RESERVED			MCSPI4_CS0_PULLTYPESELECT	MCSPI4_CS0_PULLUDENABLE	MCSPI4_CS0_MUXMODE			MCSPI4_SOMI_WAKEUPEVENT	MCSPI4_SOMI_WAKEUPENABLE	MCSPI4_SOMI_OFFMODEPULLTYPESELECT	MCSPI4_SOMI_OFFMODEPULLUDENABLE	MCSPI4_SOMI_OFFMODEOUTVALUE	MCSPI4_SOMI_OFFMODEOUTENABLE	MCSPI4_SOMI_OFFMODEENABLE	MCSPI4_SOMI_INPUTENABLE	RESERVED			MCSPI4_SOMI_PULLTYPESELECT	MCSPI4_SOMI_PULLUDENABLE	MCSPI4_SOMI_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	MCSPI4_CS0_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	MCSPI4_CS0_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29	MCSPI4_CS0_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad mcspi4_cs0 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
28	MCSPI4_CS0_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad mcspi4_cs0 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	MCSPI4_CS0_OFFMODEOUTVALUE	OffMode mode output value for pad mcspi4_cs0 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	MCSPI4_CS0_OFFMODEOUTENABLE	OffMode mode output enable value for pad mcspi4_cs0. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0

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Bits	Field Name	Description	Type	Reset
25	MCSPI4_CS0_OFFMODEENABLE	OffMode mode override control for pad mcspi4_cs0 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
24	MCSPI4_CS0_INPUTENABLE	Input enable value for pad mcspi4_cs0 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	MCSPI4_CS0_PULLTYPESELECT	pullup/down selection for pad mcspi4_cs0 0x0: pulldown selected 0x1: pullup selected	RW	1
19	MCSPI4_CS0_PULLUDENABLE	pullup/down enable for pad mcspi4_cs0 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	MCSPI4_CS0_MUXMODE	Functional multiplexing selection for pad mcspi4_cs0 0x0: Select mcspi4_cs0 0x1: Select sdmmc4_dat3 0x2: Select kpd_row7 0x3: Select gpio_154 0x7: Select safe_mode	RW	0x7
15	MCSPI4_SOMI_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	MCSPI4_SOMI_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	MCSPI4_SOMI_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad mcspi4_somi 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
12	MCSPI4_SOMI_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad mcspi4_somi 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	MCSPI4_SOMI_OFFMODEOUTVALUE	OffMode mode output value for pad mcspi4_somi 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	MCSPI4_SOMI_OFFMODEOUTENABLE	OffMode mode output enable value for pad mcspi4_somi. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	MCSPI4_SOMI_OFFMODEENABLE	OffMode mode override control for pad mcspi4_somi 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	MCSPI4_SOMI_INPUTENABLE	Input enable value for pad mcspi4_somi 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
4	MCSPI4_SOMI_ PULLTYPESELECT	pullup/down selection for pad mcspi4_somi 0x0: pulldown selected 0x1: pullup selected	RW	1
3	MCSPI4_SOMI_ PULLUDENABLE	pullup/down enable for pad mcspi4_somi 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	MCSPI4_SOMI_ MUXMODE	Functional multiplexing selection for pad mcspi4_somi 0x0: Select mcspi4_somi 0x1: Select sdmmc4_dat0 0x2: Select kpd_row6 0x3: Select gpio_153 0x7: Select safe_mode	RW	0x7

Table 18-489. Register Call Summary for Register CONTROL_CORE_PAD0_MCSPI4_SOMI_PAD1_MCSPI4_CS0

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- SYSCTRL_PADCONF_CORE Register Summary: [2]

Table 18-490. CONTROL_CORE_PAD0_UART4_RX_PAD1_UART4_TX

Address Offset	0x0000 015C		
Physical Address	0x4A10 015C	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads uart4_rx and uart4_tx Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UART4_TX_WAKEUPEVENT	UART4_TX_WAKEUPENABLE	UART4_TX_OFFMODEPULLTYPESELECT	UART4_TX_OFFMODEPULLUDENABLE	UART4_TX_OFFMODEOUTVALUE	UART4_TX_OFFMODEOUTENABLE	UART4_TX_OFFMODEENABLE	UART4_TX_INPUTENABLE	RESERVED			UART4_TX_PULLTYPESELECT	UART4_TX_PULLUDENABLE	UART4_TX_MUXMODE			UART4_RX_WAKEUPEVENT	UART4_RX_WAKEUPENABLE	UART4_RX_OFFMODEPULLTYPESELECT	UART4_RX_OFFMODEPULLUDENABLE	UART4_RX_OFFMODEOUTVALUE	UART4_RX_OFFMODEOUTENABLE	UART4_RX_OFFMODEENABLE	UART4_RX_INPUTENABLE	RESERVED			UART4_RX_PULLTYPESELECT	UART4_RX_PULLUDENABLE	UART4_RX_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	UART4_TX_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	UART4_TX_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0

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Bits	Field Name	Description	Type	Reset
29	UART4_TX_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad uart4_tx 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
28	UART4_TX_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad uart4_tx 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	UART4_TX_ OFFMODEOUTVALUE	OffMode mode output value for pad uart4_tx 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	UART4_TX_ OFFMODEOUTENABLE	OffMode mode output enable value for pad uart4_tx. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	UART4_TX_ OFFMODEENABLE	OffMode mode override control for pad uart4_tx 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
24	UART4_TX_ INPUTENABLE	Input enable value for pad uart4_tx 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	UART4_TX_ PULLTYPESELECT	pullup/down selection for pad uart4_tx 0x0: pulldown selected 0x1: pullup selected	RW	1
19	UART4_TX_ PULLUDENABLE	pullup/down enable for pad uart4_tx 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	UART4_TX_ MUXMODE	Functional multiplexing selection for pad uart4_tx 0x0: Select uart4_tx 0x1: Select sdmmc4_dat1 0x2: Select kpd_col8 0x3: Select gpio_156 0x7: Select safe_mode	RW	0x7
15	UART4_RX_ WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	UART4_RX_ WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	UART4_RX_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad uart4_rx 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
12	UART4_RX_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad uart4_rx 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	UART4_RX_ OFFMODEOUTVALUE	OffMode mode output value for pad uart4_rx 0x0: Set value at 0 0x1: Set value at 1	RW	0

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Bits	Field Name	Description	Type	Reset
10	UART4_RX_ OFFMODEOUTENABLE	OffMode mode output enable value for pad uart4_rx. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	UART4_RX_ OFFMODEENABLE	OffMode mode override control for pad uart4_rx 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	UART4_RX_INPUTENABLE	Input enable value for pad uart4_rx 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	UART4_RX_ PULLTYPESELECT	pullup/down selection for pad uart4_rx 0x0: pulldown selected 0x1: pullup selected	RW	1
3	UART4_RX_ PULLUDENABLE	pullup/down enable for pad uart4_rx 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	UART4_RX_ MUXMODE	Functional multiplexing selection for pad uart4_rx 0x0: Select uart4_rx 0x1: Select sdmmc4_dat2 0x2: Select kpd_row8 0x3: Select gpio_155 0x7: Select safe_mode	RW	0x7

Table 18-491. Register Call Summary for Register CONTROL_CORE_PAD0_UART4_RX_PAD1_UART4_TX

Control Module Functional Description • Pad Multiplexing Register Fields: [0] [1]
Control Module Register Manual • SYSCTRL_PADCONF_CORE Register Summary: [2]

Table 18-492. CONTROL_CORE_PAD0_USBB2_ULPITLL_CLK_PAD1_USBB2_ULPITLL_STP

Address Offset	0x0000 0160		
Physical Address	0x4A10 0160	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads usbb2_ulpitll_clk and usbb2_ulpitll_stp Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
USBB2_ULPITLL_STP_WAKEUPEVENT	USBB2_ULPITLL_STP_WAKEUPENABLE	USBB2_ULPITLL_STP_OFFMODEPULLTYPESELECT	USBB2_ULPITLL_STP_OFFMODEPULLUDENABLE	USBB2_ULPITLL_STP_OFFMODEOUTVALUE	USBB2_ULPITLL_STP_OFFMODEOUTENABLE	USBB2_ULPITLL_STP_OFFMODEENABLE	USBB2_ULPITLL_STP_INPUTENABLE	RESERVED			USBB2_ULPITLL_STP_PULLTYPESELECT	USBB2_ULPITLL_STP_PULLUDENABLE	USBB2_ULPITLL_STP_MUXMODE			USBB2_ULPITLL_CLK_WAKEUPEVENT	USBB2_ULPITLL_CLK_WAKEUPENABLE	USBB2_ULPITLL_CLK_OFFMODEPULLTYPESELECT	USBB2_ULPITLL_CLK_OFFMODEPULLUDENABLE	USBB2_ULPITLL_CLK_OFFMODEOUTVALUE	USBB2_ULPITLL_CLK_OFFMODEOUTENABLE	USBB2_ULPITLL_CLK_OFFMODEENABLE	USBB2_ULPITLL_CLK_INPUTENABLE	RESERVED			USBB2_ULPITLL_CLK_PULLTYPESELECT	USBB2_ULPITLL_CLK_PULLUDENABLE	USBB2_ULPITLL_CLK_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	USBB2_ULPITLL_STP_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	USBB2_ULPITLL_STP_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29	USBB2_ULPITLL_STP_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad usbb2_ulpitll_stp 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
28	USBB2_ULPITLL_STP_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad usbb2_ulpitll_stp 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	USBB2_ULPITLL_STP_OFFMODEOUTVALUE	OffMode mode output value for pad usbb2_ulpitll_stp 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	USBB2_ULPITLL_STP_OFFMODEOUTENABLE	OffMode mode output enable value for pad usbb2_ulpitll_stp. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	USBB2_ULPITLL_STP_OFFMODEENABLE	OffMode mode override control for pad usbb2_ulpitll_stp 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
24	USBB2_ULPITLL_STP_INPUTENABLE	Input enable value for pad usbb2_ulpitll_stp 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
20	USBB2_ULPITLL_ STP_PULLTYPESELECT	pullup/down selection for pad usbb2_ulpitll_stp 0x0: pulldown selected 0x1: pullup selected	RW	1
19	USBB2_ULPITLL_ STP_PULLUDENABLE	pullup/down enable for pad usbb2_ulpitll_stp 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	USBB2_ULPITLL_ STP_MUXMODE	Functional multiplexing selection for pad usbb2_ulpitll_stp 0x0: Select usbb2_ulpitll_stp 0x1: Select usbb2_ulpiphy_stp 0x2: Select sdmmc4_clk 0x3: Select gpio_158 0x4: Select hsi2_cadata 0x5: Select dispc2_data23 0x7: Select safe_mode	RW	0x7
15	USBB2_ULPITLL_ CLK_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	USBB2_ULPITLL_ CLK_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	USBB2_ULPITLL_ CLK_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad usbb2_ulpitll_clk 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
12	USBB2_ULPITLL_ CLK_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad usbb2_ulpitll_clk 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	USBB2_ULPITLL_ CLK_OFFMODEOUTVALUE	OffMode mode output value for pad usbb2_ulpitll_clk 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	USBB2_ULPITLL_ CLK_OFFMODEOUTENABLE	OffMode mode output enable value for pad usbb2_ulpitll_clk. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	USBB2_ULPITLL_ CLK_OFFMODEENABLE	OffMode mode override control for pad usbb2_ulpitll_clk 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	USBB2_ULPITLL_ CLK_INPUTENABLE	Input enable value for pad usbb2_ulpitll_clk 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	USBB2_ULPITLL_ CLK_PULLTYPESELECT	pullup/down selection for pad usbb2_ulpitll_clk 0x0: pulldown selected 0x1: pullup selected	RW	0
3	USBB2_ULPITLL_ CLK_PULLUDENABLE	pullup/down enable for pad usbb2_ulpitll_clk 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1

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Bits	Field Name	Description	Type	Reset
2:0	USBB2_ULPITLL_CLK_MUXMODE	Functional multiplexing selection for pad usbb2_ulpitll_clk 0x0: Select usbb2_ulpitll_clk 0x1: Select usbb2_ulpiphy_clk 0x2: Select sdmmc4_cmd 0x3: Select gpio_157 0x4: Select hsi2_cawake 0x7: Select safe_mode	RW	0x7

Table 18-493. Register Call Summary for Register CONTROL_CORE_PAD0_USBB2_ULPITLL_CLK_PAD1_USBB2_ULPITLL_STP

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- SYSCTRL_PADCONF_CORE Register Summary: [2]

Table 18-494. CONTROL_CORE_PAD0_USBB2_ULPITLL_DIR_PAD1_USBB2_ULPITLL_NXT

Address Offset	0x0000 0164		
Physical Address	0x4A10 0164	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads usbb2_ulpitll_dir and usbb2_ulpitll_nxt Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
USBB2_ULPITLL_NXT_WAKEUPEVENT	USBB2_ULPITLL_NXT_WAKEUPENABLE	USBB2_ULPITLL_NXT_OFFMODEPULLTYPESELECT	USBB2_ULPITLL_NXT_OFFMODEPULLUDENABLE	USBB2_ULPITLL_NXT_OFFMODEOUTVALUE	USBB2_ULPITLL_NXT_OFFMODEOUTENABLE	USBB2_ULPITLL_NXT_OFFMODEENABLE	USBB2_ULPITLL_NXT_INPUTENABLE	RESERVED			USBB2_ULPITLL_NXT_PULLTYPESELECT	USBB2_ULPITLL_NXT_PULLUDENABLE	USBB2_ULPITLL_NXT_MUXMODE			USBB2_ULPITLL_DIR_WAKEUPEVENT	USBB2_ULPITLL_DIR_WAKEUPENABLE	USBB2_ULPITLL_DIR_OFFMODEPULLTYPESELECT	USBB2_ULPITLL_DIR_OFFMODEPULLUDENABLE	USBB2_ULPITLL_DIR_OFFMODEOUTVALUE	USBB2_ULPITLL_DIR_OFFMODEOUTENABLE	USBB2_ULPITLL_DIR_OFFMODEENABLE	USBB2_ULPITLL_DIR_INPUTENABLE	RESERVED			USBB2_ULPITLL_DIR_PULLTYPESELECT	USBB2_ULPITLL_DIR_PULLUDENABLE	USBB2_ULPITLL_DIR_MUXMODE	

Bits	Field Name	Description	Type	Reset
31	USBB2_ULPITLL_NXT_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	USBB2_ULPITLL_NXT_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0

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Bits	Field Name	Description	Type	Reset
29	USBB2_ULPITLL_NXT_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad usbb2_ulpitll_nxt 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
28	USBB2_ULPITLL_NXT_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad usbb2_ulpitll_nxt 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	USBB2_ULPITLL_NXT_OFFMODEOUTVALUE	OffMode mode output value for pad usbb2_ulpitll_nxt 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	USBB2_ULPITLL_NXT_OFFMODEOUTENABLE	OffMode mode output enable value for pad usbb2_ulpitll_nxt. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	USBB2_ULPITLL_NXT_OFFMODEENABLE	OffMode mode override control for pad usbb2_ulpitll_nxt 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
24	USBB2_ULPITLL_NXT_INPUTENABLE	Input enable value for pad usbb2_ulpitll_nxt 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	USBB2_ULPITLL_NXT_PULLTYPESELECT	pullup/down selection for pad usbb2_ulpitll_nxt 0x0: pulldown selected 0x1: pullup selected	RW	1
19	USBB2_ULPITLL_NXT_PULLUDENABLE	pullup/down enable for pad usbb2_ulpitll_nxt 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	USBB2_ULPITLL_NXT_MUXMODE	Functional multiplexing selection for pad usbb2_ulpitll_nxt 0x0: Select usbb2_ulpitll_nxt 0x1: Select usbb2_ulpiphy_nxt 0x2: Select sdmmc4_dat1 0x3: Select gpio_160 0x4: Select hsi2_acready 0x5: Select dispc2_data21 0x7: Select safe_mode	RW	0x7
15	USBB2_ULPITLL_DIR_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	USBB2_ULPITLL_DIR_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	USBB2_ULPITLL_DIR_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad usbb2_ulpitll_dir 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0

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Bits	Field Name	Description	Type	Reset
12	USBB2_ULPITLL_DIR_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad usbb2_ulpitll_dir 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	USBB2_ULPITLL_DIR_OFFMODEOUTVALUE	OffMode mode output value for pad usbb2_ulpitll_dir 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	USBB2_ULPITLL_DIR_OFFMODEOUTENABLE	OffMode mode output enable value for pad usbb2_ulpitll_dir. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	USBB2_ULPITLL_DIR_OFFMODEENABLE	OffMode mode override control for pad usbb2_ulpitll_dir 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	USBB2_ULPITLL_DIR_INPUTENABLE	Input enable value for pad usbb2_ulpitll_dir 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	USBB2_ULPITLL_DIR_PULLTYPESELECT	pullup/down selection for pad usbb2_ulpitll_dir 0x0: pulldown selected 0x1: pullup selected	RW	1
3	USBB2_ULPITLL_DIR_PULLUDENABLE	pullup/down enable for pad usbb2_ulpitll_dir 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	USBB2_ULPITLL_DIR_MUXMODE	Functional multiplexing selection for pad usbb2_ulpitll_dir 0x0: Select usbb2_ulpitll_dir 0x1: Select usbb2_ulpiphy_dir 0x2: Select sdmmc4_dat0 0x3: Select gpio_159 0x4: Select hsi2_caflag 0x5: Select dispc2_data22 0x7: Select safe_mode	RW	0x7

Table 18-495. Register Call Summary for Register CONTROL_CORE_PAD0_USBB2_ULPITLL_DIR_PAD1_USBB2_ULPITLL_NXT

Control Module Functional Description • Pad Multiplexing Register Fields: [0] [1]
Control Module Register Manual • SYSCTRL_PADCONF_CORE Register Summary: [2]

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Table 18-496. CONTROL_CORE_PAD0_USBB2_ULPITLL_DAT0_PAD1_USBB2_ULPITLL_DAT1

Address Offset	0x0000 0168		
Physical Address	0x4A10 0168	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads usbb2_ulpitll_dat0 and usbb2_ulpitll_dat1 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
USBB2_ULPITLL_DAT1_WAKEUPEVENT	USBB2_ULPITLL_DAT1_WAKEUPENABLE	USBB2_ULPITLL_DAT1_OFFMODEPULLTYPESELECT	USBB2_ULPITLL_DAT1_OFFMODEPULLUDENABLE	USBB2_ULPITLL_DAT1_OFFMODEOUTVALUE	USBB2_ULPITLL_DAT1_OFFMODEOUTENABLE	USBB2_ULPITLL_DAT1_OFFMODEENABLE	USBB2_ULPITLL_DAT1_INPUTENABLE	RESERVED			USBB2_ULPITLL_DAT1_PULLTYPESELECT	USBB2_ULPITLL_DAT1_PULLUDENABLE	USBB2_ULPITLL_DAT1_MUXMODE			USBB2_ULPITLL_DAT0_WAKEUPEVENT	USBB2_ULPITLL_DAT0_WAKEUPENABLE	USBB2_ULPITLL_DAT0_OFFMODEPULLTYPESELECT	USBB2_ULPITLL_DAT0_OFFMODEPULLUDENABLE	USBB2_ULPITLL_DAT0_OFFMODEOUTVALUE	USBB2_ULPITLL_DAT0_OFFMODEOUTENABLE	USBB2_ULPITLL_DAT0_OFFMODEENABLE	USBB2_ULPITLL_DAT0_INPUTENABLE	RESERVED			USBB2_ULPITLL_DAT0_PULLTYPESELECT	USBB2_ULPITLL_DAT0_PULLUDENABLE	USBB2_ULPITLL_DAT0_MUXMODE	

Bits	Field Name	Description	Type	Reset
31	USBB2_ULPITLL_DAT1_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	USBB2_ULPITLL_DAT1_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29	USBB2_ULPITLL_DAT1_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad usbb2_ulpitll_dat1 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
28	USBB2_ULPITLL_DAT1_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad usbb2_ulpitll_dat1 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	USBB2_ULPITLL_DAT1_OFFMODEOUTVALUE	OffMode mode output value for pad usbb2_ulpitll_dat1 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	USBB2_ULPITLL_DAT1_OFFMODEOUTENABLE	OffMode mode output enable value for pad usbb2_ulpitll_dat1. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0

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Bits	Field Name	Description	Type	Reset
25	USBB2_ULPITLL_DAT1_OFFMODEENABLE	OffMode mode override control for pad usbb2_ulpitll_dat1 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
24	USBB2_ULPITLL_DAT1_INPUTENABLE	Input enable value for pad usbb2_ulpitll_dat1 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	USBB2_ULPITLL_DAT1_PULLTYPESELECT	pullup/down selection for pad usbb2_ulpitll_dat1 0x0: pulldown selected 0x1: pullup selected	RW	1
19	USBB2_ULPITLL_DAT1_PULLUDENABLE	pullup/down enable for pad usbb2_ulpitll_dat1 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	USBB2_ULPITLL_DAT1_MUXMODE	Functional multiplexing selection for pad usbb2_ulpitll_dat1 0x0: Select usbb2_ulpitll_dat1 0x1: Select usbb2_ulpiphy_dat1 0x2: Select sdmmc4_dat3 0x3: Select gpio_162 0x4: Select hsi2_acdata 0x5: Select dispc2_data19 0x6: Select usbb2_mm_txdat 0x7: Select safe_mode	RW	0x7
15	USBB2_ULPITLL_DAT0_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	USBB2_ULPITLL_DAT0_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	USBB2_ULPITLL_DAT0_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad usbb2_ulpitll_dat0 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
12	USBB2_ULPITLL_DAT0_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad usbb2_ulpitll_dat0 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	USBB2_ULPITLL_DAT0_OFFMODEOUTVALUE	OffMode mode output value for pad usbb2_ulpitll_dat0 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	USBB2_ULPITLL_DAT0_OFFMODEOUTENABLE	OffMode mode output enable value for pad usbb2_ulpitll_dat0. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	USBB2_ULPITLL_DAT0_OFFMODEENABLE	OffMode mode override control for pad usbb2_ulpitll_dat0 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0

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Bits	Field Name	Description	Type	Reset
8	USBB2_ULPITLL_ DAT0_INPUTENABLE	Input enable value for pad usbb2_ulpitll_dat0 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	USBB2_ULPITLL_ DAT0_PULLTYPESELECT	pullup/down selection for pad usbb2_ulpitll_dat0 0x0: pulldown selected 0x1: pullup selected	RW	1
3	USBB2_ULPITLL_ DAT0_PULLUDENABLE	pullup/down enable for pad usbb2_ulpitll_dat0 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	USBB2_ULPITLL_ DAT0_MUXMODE	Functional multiplexing selection for pad usbb2_ulpitll_dat0 0x0: Select usbb2_ulpitll_dat0 0x1: Select usbb2_ulpiphy_dat0 0x2: Select sdmmc4_dat2 0x3: Select gpio_161 0x4: Select hsi2_acwake 0x5: Select dispc2_data20 0x6: Select usbb2_mm_txen 0x7: Select safe_mode	RW	0x7

Table 18-497. Register Call Summary for Register CONTROL_CORE_PAD0_USBB2_ULPITLL_DAT0_PAD1_USBB2_ULPITLL_DAT1

Control Module Functional Description • Pad Multiplexing Register Fields: [0] [1]
Control Module Register Manual • SYSCTRL_PADCONF_CORE Register Summary: [2]

Table 18-498. CONTROL_CORE_PAD0_USBB2_ULPITLL_DAT2_PAD1_USBB2_ULPITLL_DAT3

Address Offset	0x0000 016C		
Physical Address	0x4A10 016C	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads usbb2_ulpitll_dat2 and usbb2_ulpitll_dat3 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
USBB2_ULPITLL_DAT3_WAKEUPEVENT	USBB2_ULPITLL_DAT3_WAKEUPENABLE	USBB2_ULPITLL_DAT3_OFFMODEPULLTYPESELECT	USBB2_ULPITLL_DAT3_OFFMODEPULLUDENABLE	USBB2_ULPITLL_DAT3_OFFMODEOUTVALUE	USBB2_ULPITLL_DAT3_OFFMODEOUTENABLE	USBB2_ULPITLL_DAT3_OFFMODEENABLE	USBB2_ULPITLL_DAT3_INPUTENABLE	RESERVED			USBB2_ULPITLL_DAT3_PULLTYPESELECT	USBB2_ULPITLL_DAT3_PULLUDENABLE	USBB2_ULPITLL_DAT3_MUXMODE			USBB2_ULPITLL_DAT2_WAKEUPEVENT	USBB2_ULPITLL_DAT2_WAKEUPENABLE	USBB2_ULPITLL_DAT2_OFFMODEPULLTYPESELECT	USBB2_ULPITLL_DAT2_OFFMODEPULLUDENABLE	USBB2_ULPITLL_DAT2_OFFMODEOUTVALUE	USBB2_ULPITLL_DAT2_OFFMODEOUTENABLE	USBB2_ULPITLL_DAT2_OFFMODEENABLE	USBB2_ULPITLL_DAT2_INPUTENABLE	RESERVED			USBB2_ULPITLL_DAT2_PULLTYPESELECT	USBB2_ULPITLL_DAT2_PULLUDENABLE	USBB2_ULPITLL_DAT2_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	USBB2_ULPITLL_DAT3_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	USBB2_ULPITLL_DAT3_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29	USBB2_ULPITLL_DAT3_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad usbb2_ulpitll_dat3 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
28	USBB2_ULPITLL_DAT3_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad usbb2_ulpitll_dat3 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	USBB2_ULPITLL_DAT3_OFFMODEOUTVALUE	OffMode mode output value for pad usbb2_ulpitll_dat3 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	USBB2_ULPITLL_DAT3_OFFMODEOUTENABLE	OffMode mode output enable value for pad usbb2_ulpitll_dat3. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	USBB2_ULPITLL_DAT3_OFFMODEENABLE	OffMode mode override control for pad usbb2_ulpitll_dat3 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
24	USBB2_ULPITLL_DAT3_INPUTENABLE	Input enable value for pad usbb2_ulpitll_dat3 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
20	USBB2_ULPITLL_ DAT3_PULLTYPESELECT	pullup/down selection for pad usbb2_ulpitll_dat3 0x0: pulldown selected 0x1: pullup selected	RW	1
19	USBB2_ULPITLL_ DAT3_PULLUDENABLE	pullup/down enable for pad usbb2_ulpitll_dat3 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	USBB2_ULPITLL_ DAT3_MUXMODE	Functional multiplexing selection for pad usbb2_ulpitll_dat3 0x0: Select usbb2_ulpitll_dat3 0x1: Select usbb2_ulpiphy_dat3 0x2: Select sdmmc3_dat1 0x3: Select gpio_164 0x4: Select hsi2_caready 0x5: Select dispc2_data15 0x6: Select rfbi_data15 0x7: Select safe_mode	RW	0x7
15	USBB2_ULPITLL_ DAT2_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	USBB2_ULPITLL_ DAT2_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	USBB2_ULPITLL_ DAT2_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad usbb2_ulpitll_dat2 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
12	USBB2_ULPITLL_ DAT2_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad usbb2_ulpitll_dat2 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	USBB2_ULPITLL_ DAT2_OFFMODEOUTVALUE	OffMode mode output value for pad usbb2_ulpitll_dat2 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	USBB2_ULPITLL_ DAT2_OFFMODEOUTENABLE	OffMode mode output enable value for pad usbb2_ulpitll_dat2. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	USBB2_ULPITLL_ DAT2_OFFMODEENABLE	OffMode mode override control for pad usbb2_ulpitll_dat2 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	USBB2_ULPITLL_ DAT2_INPUTENABLE	Input enable value for pad usbb2_ulpitll_dat2 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	USBB2_ULPITLL_ DAT2_PULLTYPESELECT	pullup/down selection for pad usbb2_ulpitll_dat2 0x0: pulldown selected 0x1: pullup selected	RW	0

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Bits	Field Name	Description	Type	Reset
3	USBB2_ULPITLL_DAT2_PULLUDENABLE	pullup/down enable for pad usbb2_ulpitll_dat2 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	USBB2_ULPITLL_DAT2_MUXMODE	Functional multiplexing selection for pad usbb2_ulpitll_dat2 0x0: Select usbb2_ulpitll_dat2 0x1: Select usbb2_ulpiphy_dat2 0x2: Select sdmmc3_dat2 0x3: Select gpio_163 0x4: Select hsi2_acflag 0x5: Select dispc2_data18 0x6: Select usbb2_mm_txse0 0x7: Select safe_mode	RW	0x7

Table 18-499. Register Call Summary for Register CONTROL_CORE_PAD0_USBB2_ULPITLL_DAT2_PAD1_USBB2_ULPITLL_DAT3

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- SYSCTRL_PADCONF_CORE Register Summary: [2]

Table 18-500. CONTROL_CORE_PAD0_USBB2_ULPITLL_DAT4_PAD1_USBB2_ULPITLL_DAT5

Address Offset	0x0000 0170		
Physical Address	0x4A10 0170	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads usbb2_ulpitll_dat4 and usbb2_ulpitll_dat5 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
USBB2_ULPITLL_DAT5_WAKEUPEVENT	USBB2_ULPITLL_DAT5_WAKEUPENABLE	USBB2_ULPITLL_DAT5_OFFMODEPULLTYPESELECT	USBB2_ULPITLL_DAT5_OFFMODEPULLUDENABLE	USBB2_ULPITLL_DAT5_OFFMODEOUTVALUE	USBB2_ULPITLL_DAT5_OFFMODEOUTENABLE	USBB2_ULPITLL_DAT5_OFFMODEENABLE	USBB2_ULPITLL_DAT5_INPUTENABLE	RESERVED			USBB2_ULPITLL_DAT5_PULLTYPESELECT	USBB2_ULPITLL_DAT5_PULLUDENABLE	USBB2_ULPITLL_DAT5_MUXMODE			USBB2_ULPITLL_DAT4_WAKEUPEVENT	USBB2_ULPITLL_DAT4_WAKEUPENABLE	USBB2_ULPITLL_DAT4_OFFMODEPULLTYPESELECT	USBB2_ULPITLL_DAT4_OFFMODEPULLUDENABLE	USBB2_ULPITLL_DAT4_OFFMODEOUTVALUE	USBB2_ULPITLL_DAT4_OFFMODEOUTENABLE	USBB2_ULPITLL_DAT4_OFFMODEENABLE	USBB2_ULPITLL_DAT4_INPUTENABLE	RESERVED			USBB2_ULPITLL_DAT4_PULLTYPESELECT	USBB2_ULPITLL_DAT4_PULLUDENABLE	USBB2_ULPITLL_DAT4_MUXMODE	

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Bits	Field Name	Description	Type	Reset
31	USBB2_ULPITLL_DAT5_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	USBB2_ULPITLL_DAT5_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29	USBB2_ULPITLL_DAT5_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad usbb2_ulpitll_dat5 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
28	USBB2_ULPITLL_DAT5_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad usbb2_ulpitll_dat5 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	USBB2_ULPITLL_DAT5_OFFMODEOUTVALUE	OffMode mode output value for pad usbb2_ulpitll_dat5 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	USBB2_ULPITLL_DAT5_OFFMODEOUTENABLE	OffMode mode output enable value for pad usbb2_ulpitll_dat5. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	USBB2_ULPITLL_DAT5_OFFMODEENABLE	OffMode mode override control for pad usbb2_ulpitll_dat5 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
24	USBB2_ULPITLL_DAT5_INPUTENABLE	Input enable value for pad usbb2_ulpitll_dat5 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	USBB2_ULPITLL_DAT5_PULLTYPESELECT	pullup/down selection for pad usbb2_ulpitll_dat5 0x0: pulldown selected 0x1: pullup selected	RW	1
19	USBB2_ULPITLL_DAT5_PULLUDENABLE	pullup/down enable for pad usbb2_ulpitll_dat5 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	USBB2_ULPITLL_DAT5_MUXMODE	Functional multiplexing selection for pad usbb2_ulpitll_dat5 0x0: Select usbb2_ulpitll_dat5 0x1: Select usbb2_ulpiphy_dat5 0x2: Select sdmmc3_dat3 0x3: Select gpio_166 0x4: Select mcspi3_cs0 0x5: Select dispc2_data13 0x6: Select rfbi_data13 0x7: Select safe_mode	RW	0x7
15	USBB2_ULPITLL_DAT4_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0

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Bits	Field Name	Description	Type	Reset
14	USBB2_ULPITLL_DAT4_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	USBB2_ULPITLL_DAT4_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad usbb2_ulpitll_dat4 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
12	USBB2_ULPITLL_DAT4_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad usbb2_ulpitll_dat4 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	USBB2_ULPITLL_DAT4_OFFMODEOUTVALUE	OffMode mode output value for pad usbb2_ulpitll_dat4 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	USBB2_ULPITLL_DAT4_OFFMODEOUTENABLE	OffMode mode output enable value for pad usbb2_ulpitll_dat4. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	USBB2_ULPITLL_DAT4_OFFMODEENABLE	OffMode mode override control for pad usbb2_ulpitll_dat4 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	USBB2_ULPITLL_DAT4_INPUTENABLE	Input enable value for pad usbb2_ulpitll_dat4 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	USBB2_ULPITLL_DAT4_PULLTYPESELECT	pullup/down selection for pad usbb2_ulpitll_dat4 0x0: pulldown selected 0x1: pullup selected	RW	1
3	USBB2_ULPITLL_DAT4_PULLUDENABLE	pullup/down enable for pad usbb2_ulpitll_dat4 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	USBB2_ULPITLL_DAT4_MUXMODE	Functional multiplexing selection for pad usbb2_ulpitll_dat4 0x0: Select usbb2_ulpitll_dat4 0x1: Select usbb2_ulpiphy_dat4 0x2: Select sdmmc3_dat0 0x3: Select gpio_165 0x4: Select mcspi3_somi 0x5: Select dispc2_data14 0x6: Select rfbi_data14 0x7: Select safe_mode	RW	0x7

Table 18-501. Register Call Summary for Register CONTROL_CORE_PAD0_USBB2_ULPITLL_DAT4_PAD1_USBB2_ULPITLL_DAT5

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- SYSCTRL_PADCONF_CORE Register Summary: [2]

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Table 18-502. CONTROL_CORE_PAD0_USBB2_ULPITLL_DAT6_PAD1_USBB2_ULPITLL_DAT7

Address Offset	0x0000 0174		
Physical Address	0x4A10 0174	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads usbb2_ulpitll_dat6 and usbb2_ulpitll_dat7 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
USBB2_ULPITLL_DAT7_WAKEUPEVENT	USBB2_ULPITLL_DAT7_WAKEUPENABLE	USBB2_ULPITLL_DAT7_OFFMODEPULLTYPESELECT	USBB2_ULPITLL_DAT7_OFFMODEPULLUDENABLE	USBB2_ULPITLL_DAT7_OFFMODEOUTVALUE	USBB2_ULPITLL_DAT7_OFFMODEOUTENABLE	USBB2_ULPITLL_DAT7_OFFMODEENABLE	USBB2_ULPITLL_DAT7_INPUTENABLE	RESERVED			USBB2_ULPITLL_DAT7_PULLTYPESELECT	USBB2_ULPITLL_DAT7_PULLUDENABLE	USBB2_ULPITLL_DAT7_MUXMODE			USBB2_ULPITLL_DAT6_WAKEUPEVENT	USBB2_ULPITLL_DAT6_WAKEUPENABLE	USBB2_ULPITLL_DAT6_OFFMODEPULLTYPESELECT	USBB2_ULPITLL_DAT6_OFFMODEPULLUDENABLE	USBB2_ULPITLL_DAT6_OFFMODEOUTVALUE	USBB2_ULPITLL_DAT6_OFFMODEOUTENABLE	USBB2_ULPITLL_DAT6_OFFMODEENABLE	USBB2_ULPITLL_DAT6_INPUTENABLE	RESERVED			USBB2_ULPITLL_DAT6_PULLTYPESELECT	USBB2_ULPITLL_DAT6_PULLUDENABLE	USBB2_ULPITLL_DAT6_MUXMODE	

Bits	Field Name	Description	Type	Reset
31	USBB2_ULPITLL_DAT7_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	USBB2_ULPITLL_DAT7_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29	USBB2_ULPITLL_DAT7_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad usbb2_ulpitll_dat7 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
28	USBB2_ULPITLL_DAT7_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad usbb2_ulpitll_dat7 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	USBB2_ULPITLL_DAT7_OFFMODEOUTVALUE	OffMode mode output value for pad usbb2_ulpitll_dat7 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	USBB2_ULPITLL_DAT7_OFFMODEOUTENABLE	OffMode mode output enable value for pad usbb2_ulpitll_dat7. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0

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Bits	Field Name	Description	Type	Reset
25	USBB2_ULPITLL_DAT7_OFFMODEENABLE	OffMode mode override control for pad usbb2_ulpitll_dat7 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
24	USBB2_ULPITLL_DAT7_INPUTENABLE	Input enable value for pad usbb2_ulpitll_dat7 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	USBB2_ULPITLL_DAT7_PULLTYPESELECT	pullup/down selection for pad usbb2_ulpitll_dat7 0x0: pulldown selected 0x1: pullup selected	RW	1
19	USBB2_ULPITLL_DAT7_PULLUDENABLE	pullup/down enable for pad usbb2_ulpitll_dat7 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	USBB2_ULPITLL_DAT7_MUXMODE	Functional multiplexing selection for pad usbb2_ulpitll_dat7 0x0: Select usbb2_ulpitll_dat7 0x1: Select usbb2_ulpiphy_dat7 0x2: Select sdmmc3_clk 0x3: Select gpio_168 0x4: Select mcspi3_clk 0x5: Select dispc2_data11 0x6: Select rfbi_data11 0x7: Select safe_mode	RW	0x7
15	USBB2_ULPITLL_DAT6_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	USBB2_ULPITLL_DAT6_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	USBB2_ULPITLL_DAT6_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad usbb2_ulpitll_dat6 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
12	USBB2_ULPITLL_DAT6_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad usbb2_ulpitll_dat6 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	USBB2_ULPITLL_DAT6_OFFMODEOUTVALUE	OffMode mode output value for pad usbb2_ulpitll_dat6 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	USBB2_ULPITLL_DAT6_OFFMODEOUTENABLE	OffMode mode output enable value for pad usbb2_ulpitll_dat6. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	USBB2_ULPITLL_DAT6_OFFMODEENABLE	OffMode mode override control for pad usbb2_ulpitll_dat6 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0

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Bits	Field Name	Description	Type	Reset
8	USBB2_ULPITLL_ DAT6_INPUTENABLE	Input enable value for pad usbb2_ulpitll_dat6 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	USBB2_ULPITLL_ DAT6_PULLTYPESELECT	pullup/down selection for pad usbb2_ulpitll_dat6 0x0: pulldown selected 0x1: pullup selected	RW	1
3	USBB2_ULPITLL_ DAT6_PULLUDENABLE	pullup/down enable for pad usbb2_ulpitll_dat6 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	USBB2_ULPITLL_ DAT6_MUXMODE	Functional multiplexing selection for pad usbb2_ulpitll_dat6 0x0: Select usbb2_ulpitll_dat6 0x1: Select usbb2_ulpiphy_dat6 0x2: Select sdmmc3_cmd 0x3: Select gpio_167 0x4: Select mcspi3_simo 0x5: Select dispc2_data12 0x6: Select rfbi_data12 0x7: Select safe_mode	RW	0x7

Table 18-503. Register Call Summary for Register CONTROL_CORE_PAD0_USBB2_ULPITLL_DAT6_PAD1_USBB2_ULPITLL_DAT7

Control Module Functional Description • Pad Multiplexing Register Fields: [0] [1]
Control Module Register Manual • SYSCTRL_PADCONF_CORE Register Summary: [2]

Table 18-504. CONTROL_CORE_PAD0_USBB2_HSIC_DATA_PAD1_USBB2_HSIC_STROBE

Address Offset	0x0000 0178		
Physical Address	0x4A10 0178	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads usbb2_hsic_data and usbb2_hsic_strobe Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
USBB2_HSIC_STROBE_WAKEUPEVENT	USBB2_HSIC_STROBE_WAKEUPENABLE	RESERVED		USBB2_HSIC_STROBE_OFFMODEOUTVALUE	USBB2_HSIC_STROBE_OFFMODEOUTENABLE	USBB2_HSIC_STROBE_OFFMODEENABLE	RESERVED						USBB2_HSIC_STROBE_MUXMODE			USBB2_HSIC_DATA_WAKEUPEVENT	USBB2_HSIC_DATA_WAKEUPENABLE	RESERVED		USBB2_HSIC_DATA_OFFMODEOUTVALUE	USBB2_HSIC_DATA_OFFMODEOUTENABLE	USBB2_HSIC_DATA_OFFMODEENABLE	RESERVED						USBB2_HSIC_DATA_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	USBB2_HSIC_STROBE_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	USBB2_HSIC_STROBE_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:28	RESERVED		R	0x0
27	USBB2_HSIC_STROBE_OFFMODEOUTVALUE	OffMode mode output value for pad usbb2_hsic_strobe 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	USBB2_HSIC_STROBE_OFFMODEOUTENABLE	OffMode mode output enable value for pad usbb2_hsic_strobe. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	USBB2_HSIC_STROBE_OFFMODEENABLE	OffMode mode override control for pad usbb2_hsic_strobe 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
24:19	RESERVED		R	0x00
18:16	USBB2_HSIC_STROBE_MUXMODE	Functional multiplexing selection for pad usbb2_hsic_strobe 0x0: Select usbb2_hsic_strobe 0x3: Select gpio_170 0x7: Select safe_mode	RW	0x7
15	USBB2_HSIC_DATA_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	USBB2_HSIC_DATA_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:12	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
11	USBB2_HSIC_DATA_OFFMODEOUTVALUE	OffMode mode output value for pad usbb2_hsic_data 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	USBB2_HSIC_DATA_OFFMODEOUTENABLE	OffMode mode output enable value for pad usbb2_hsic_data. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	USBB2_HSIC_DATA_OFFMODEENABLE	OffMode mode override control for pad usbb2_hsic_data 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8:3	RESERVED		R	0x00
2:0	USBB2_HSIC_DATA_MUXMODE	Functional multiplexing selection for pad usbb2_hsic_data 0x0: Select usbb2_hsic_data 0x3: Select gpio_169 0x7: Select safe_mode	RW	0x7

Table 18-505. Register Call Summary for Register CONTROL_CORE_PAD0_USBB2_HSIC_DATA_PAD1_USBB2_HSIC_STROBE

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- SYSCTRL_PADCONF_CORE Register Summary: [2]

Table 18-506. CONTROL_CORE_PAD0_KPD_COL3_PAD1_KPD_COL4

Address Offset	0x0000 017C		
Physical Address	0x4A10 017C	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads kpd_col3 and kpd_col4 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
KPD_COL4_WAKEUPEVENT	KPD_COL4_WAKEUPENABLE	KPD_COL4_OFFMODEPULLTYPESELECT	KPD_COL4_OFFMODEPULLUDENABLE	KPD_COL4_OFFMODEOUTVALUE	KPD_COL4_OFFMODEOUTENABLE	KPD_COL4_OFFMODEENABLE	KPD_COL4_INPUTENABLE	RESERVED			KPD_COL4_PULLTYPESELECT	KPD_COL4_PULLUDENABLE	KPD_COL4_MUXMODE			KPD_COL3_WAKEUPEVENT	KPD_COL3_WAKEUPENABLE	KPD_COL3_OFFMODEPULLTYPESELECT	KPD_COL3_OFFMODEPULLUDENABLE	KPD_COL3_OFFMODEOUTVALUE	KPD_COL3_OFFMODEOUTENABLE	KPD_COL3_OFFMODEENABLE	KPD_COL3_INPUTENABLE	RESERVED			KPD_COL3_PULLTYPESELECT	KPD_COL3_PULLUDENABLE	KPD_COL3_MUXMODE		

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Bits	Field Name	Description	Type	Reset
31	KPD_COL4_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	KPD_COL4_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29	KPD_COL4_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad kpd_col4 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
28	KPD_COL4_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad kpd_col4 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	KPD_COL4_OFFMODEOUTVALUE	OffMode mode output value for pad kpd_col4 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	KPD_COL4_OFFMODEOUTENABLE	OffMode mode output enable value for pad kpd_col4. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	KPD_COL4_OFFMODEENABLE	OffMode mode override control for pad kpd_col4 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
24	KPD_COL4_INPUTENABLE	Input enable value for pad kpd_col4 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	KPD_COL4_PULLTYPESELECT	pullup/down selection for pad kpd_col4 0x0: pulldown selected 0x1: pullup selected	RW	0
19	KPD_COL4_PULLUDENABLE	pullup/down enable for pad kpd_col4 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	KPD_COL4_MUXMODE	Functional multiplexing selection for pad kpd_col4 0x0: Select kpd_col4 0x1: Select kpd_col1 0x2: Select cam2_d1 0x3: Select gpio_172 0x7: Select safe_mode	RW	0x7
15	KPD_COL3_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0

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Bits	Field Name	Description	Type	Reset
14	KPD_COL3_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	KPD_COL3_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad kpd_col3 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
12	KPD_COL3_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad kpd_col3 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	KPD_COL3_ OFFMODEOUTVALUE	OffMode mode output value for pad kpd_col3 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	KPD_COL3_ OFFMODEOUTENABLE	OffMode mode output enable value for pad kpd_col3. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	KPD_COL3_ OFFMODEENABLE	OffMode mode override control for pad kpd_col3 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	KPD_COL3_ INPUTENABLE	Input enable value for pad kpd_col3 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	KPD_COL3_ PULLTYPESELECT	pullup/down selection for pad kpd_col3 0x0: pulldown selected 0x1: pullup selected	RW	0
3	KPD_COL3_ PULLUDENABLE	pullup/down enable for pad kpd_col3 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	KPD_COL3_ MUXMODE	Functional multiplexing selection for pad kpd_col3 0x0: Select kpd_col3 0x1: Select kpd_col0 0x2: Select cam2_d0 0x3: Select gpio_171 0x7: Select safe_mode	RW	0x7

Table 18-507. Register Call Summary for Register CONTROL_CORE_PAD0_KPD_COL3_PAD1_KPD_COL4

Control Module Functional Description • Pad Multiplexing Register Fields: [0] [1]
Control Module Register Manual • SYSCTRL_PADCONF_CORE Register Summary: [2]

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Table 18-508. CONTROL_CORE_PAD0_KPD_COL5_PAD1_KPD_COL0

Address Offset	0x0000 0180		
Physical Address	0x4A10 0180	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads kpd_col5 and kpd_col0 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
KPD_COL0_WAKEUPEVENT	KPD_COL0_WAKEUPENABLE	KPD_COL0_OFFMODEPULLTYPESELECT	KPD_COL0_OFFMODEPULLUDENABLE	KPD_COL0_OFFMODEOUTVALUE	KPD_COL0_OFFMODEOUTENABLE	KPD_COL0_OFFMODEENABLE	KPD_COL0_INPUTENABLE	RESERVED			KPD_COL0_PULLTYPESELECT	KPD_COL0_PULLUDENABLE	KPD_COL0_MUXMODE			KPD_COL5_WAKEUPEVENT	KPD_COL5_WAKEUPENABLE	KPD_COL5_OFFMODEPULLTYPESELECT	KPD_COL5_OFFMODEPULLUDENABLE	KPD_COL5_OFFMODEOUTVALUE	KPD_COL5_OFFMODEOUTENABLE	KPD_COL5_OFFMODEENABLE	KPD_COL5_INPUTENABLE	RESERVED			KPD_COL5_PULLTYPESELECT	KPD_COL5_PULLUDENABLE	KPD_COL5_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	KPD_COL0_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	KPD_COL0_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29	KPD_COL0_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad kpd_col0 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
28	KPD_COL0_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad kpd_col0 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	KPD_COL0_ OFFMODEOUTVALUE	OffMode mode output value for pad kpd_col0 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	KPD_COL0_ OFFMODEOUTENABLE	OffMode mode output enable value for pad kpd_col0. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	KPD_COL0_ OFFMODEENABLE	OffMode mode override control for pad kpd_col0 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0

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Bits	Field Name	Description	Type	Reset
24	KPD_COL0_INPUTENABLE	Input enable value for pad kpd_col0 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	KPD_COL0_PULLTYPESELECT	pullup/down selection for pad kpd_col0 0x0: pulldown selected 0x1: pullup selected	RW	0
19	KPD_COL0_PULLUDENABLE	pullup/down enable for pad kpd_col0 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	KPD_COL0_MUXMODE	Functional multiplexing selection for pad kpd_col0 0x0: Select kpd_col0 0x1: Select kpd_col3 0x2: Select cam2_d3 0x3: Select gpio_174 0x7: Select safe_mode	RW	0x7
15	KPD_COL5_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	KPD_COL5_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	KPD_COL5_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad kpd_col5 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
12	KPD_COL5_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad kpd_col5 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	KPD_COL5_ OFFMODEOUTVALUE	OffMode mode output value for pad kpd_col5 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	KPD_COL5_ OFFMODEOUTENABLE	OffMode mode output enable value for pad kpd_col5. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	KPD_COL5_ OFFMODEENABLE	OffMode mode override control for pad kpd_col5 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	KPD_COL5_ INPUTENABLE	Input enable value for pad kpd_col5 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
4	KPD_COL5_ PULLTYPESELECT	pullup/down selection for pad kpd_col5 0x0: pulldown selected 0x1: pullup selected	RW	0
3	KPD_COL5_ PULLUDENABLE	pullup/down enable for pad kpd_col5 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	KPD_COL5_ MUXMODE	Functional multiplexing selection for pad kpd_col5 0x0: Select kpd_col5 0x1: Select kpd_col2 0x2: Select cam2_d2 0x3: Select gpio_173 0x7: Select safe_mode	RW	0x7

Table 18-509. Register Call Summary for Register CONTROL_CORE_PAD0_KPD_COL5_PAD1_KPD_COL0

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- SYSCTRL_PADCONF_CORE Register Summary: [2]

Table 18-510. CONTROL_CORE_PAD0_KPD_COL1_PAD1_KPD_COL2

Address Offset	0x0000 0184		
Physical Address	0x4A10 0184	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads kpd_col1 and kpd_col2 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
KPD_COL2_WAKEUPEVENT	KPD_COL2_WAKEUPENABLE	KPD_COL2_OFFMODEPULLTYPESELECT	KPD_COL2_OFFMODEPULLUDENABLE	KPD_COL2_OFFMODEOUTVALUE	KPD_COL2_OFFMODEOUTENABLE	KPD_COL2_OFFMODEENABLE	KPD_COL2_INPUTENABLE	RESERVED			KPD_COL2_PULLTYPESELECT	KPD_COL2_PULLUDENABLE	KPD_COL2_MUXMODE			KPD_COL1_WAKEUPEVENT	KPD_COL1_WAKEUPENABLE	KPD_COL1_OFFMODEPULLTYPESELECT	KPD_COL1_OFFMODEPULLUDENABLE	KPD_COL1_OFFMODEOUTVALUE	KPD_COL1_OFFMODEOUTENABLE	KPD_COL1_OFFMODEENABLE	KPD_COL1_INPUTENABLE	RESERVED			KPD_COL1_PULLTYPESELECT	KPD_COL1_PULLUDENABLE	KPD_COL1_MUXMODE	

Bits	Field Name	Description	Type	Reset
31	KPD_COL2_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0

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Bits	Field Name	Description	Type	Reset
30	KPD_COL2_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29	KPD_COL2_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad kpd_col2 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
28	KPD_COL2_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad kpd_col2 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	KPD_COL2_ OFFMODEOUTVALUE	OffMode mode output value for pad kpd_col2 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	KPD_COL2_ OFFMODEOUTENABLE	OffMode mode output enable value for pad kpd_col2. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	KPD_COL2_ OFFMODEENABLE	OffMode mode override control for pad kpd_col2 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
24	KPD_COL2_ INPUTENABLE	Input enable value for pad kpd_col2 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	KPD_COL2_ PULLTYPESELECT	pullup/down selection for pad kpd_col2 0x0: pulldown selected 0x1: pullup selected	RW	0
19	KPD_COL2_ PULLUDENABLE	pullup/down enable for pad kpd_col2 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	KPD_COL2_ MUXMODE	Functional multiplexing selection for pad kpd_col2 0x0: Select kpd_col2 0x1: Select kpd_col5 0x2: Select cam2_d10 0x3: Select gpio_1 0x7: Select safe_mode	RW	0x7
15	KPD_COL1_ WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	KPD_COL1_ WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0

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Bits	Field Name	Description	Type	Reset
13	KPD_COL1_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad kpd_col1 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
12	KPD_COL1_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad kpd_col1 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	KPD_COL1_ OFFMODEOUTVALUE	OffMode mode output value for pad kpd_col1 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	KPD_COL1_ OFFMODEOUTENABLE	OffMode mode output enable value for pad kpd_col1. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	KPD_COL1_ OFFMODEENABLE	OffMode mode override control for pad kpd_col1 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	KPD_COL1_ INPUTENABLE	Input enable value for pad kpd_col1 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	KPD_COL1_ PULLTYPESELECT	pullup/down selection for pad kpd_col1 0x0: pulldown selected 0x1: pullup selected	RW	0
3	KPD_COL1_ PULLUDENABLE	pullup/down enable for pad kpd_col1 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	KPD_COL1_ MUXMODE	Functional multiplexing selection for pad kpd_col1 0x0: Select kpd_col1 0x1: Select kpd_col4 0x2: Select cam2_d8 0x3: Select gpio_0 0x7: Select safe_mode	RW	0x7

Table 18-511. Register Call Summary for Register CONTROL_CORE_PAD0_KPD_COL1_PAD1_KPD_COL2

Control Module Functional Description

- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual

- SYSCTRL_PADCONF_CORE Register Summary: [2]

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Table 18-512. CONTROL_CORE_PAD0_KPD_ROW3_PAD1_KPD_ROW4

Address Offset	0x0000 0188		
Physical Address	0x4A10 0188	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads kpd_row3 and kpd_row4 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
KPD_ROW4_WAKEUPEVENT	KPD_ROW4_WAKEUPEVENT	RESERVED					KPD_ROW4_WAKEUPEVENT	RESERVED			KPD_ROW4_WAKEUPEVENT	KPD_ROW4_WAKEUPEVENT	KPD_ROW4_WAKEUPEVENT			KPD_ROW3_WAKEUPEVENT	KPD_ROW3_WAKEUPENABLE	RESERVED					KPD_ROW3_INPUTENABLE	RESERVED			KPD_ROW3_PULLTYPESELECT	KPD_ROW3_PULLUDENABLE	KPD_ROW3_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	KPD_ROW4_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	KPD_ROW4_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29	KPD_ROW4_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad kpd_row4 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
28	KPD_ROW4_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad kpd_row4 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	KPD_ROW4_ OFFMODEOUTVALUE	OffMode mode output value for pad kpd_row4 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	KPD_ROW4_ OFFMODEOUTENABLE	OffMode mode output enable value for pad kpd_row4. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	KPD_ROW4_ OFFMODEENABLE	OffMode mode override control for pad kpd_row4 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
24	KPD_ROW4_ INPUTENABLE	Input enable value for pad kpd_row4 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1

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Bits	Field Name	Description	Type	Reset
23:21	RESERVED		R	0x0
20	KPD_ROW4_PULLTYPESELECT	pullup/down selection for pad kpd_row4 0x0: pulldown selected 0x1: pullup selected	RW	1
19	KPD_ROW4_PULLUDENABLE	pullup/down enable for pad kpd_row4 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	KPD_ROW4_MUXMODE	Functional multiplexing selection for pad kpd_row4 0x0: Select kpd_row4 0x1: Select kpd_row1 0x2: Select cam2_d5 0x3: Select gpio_176 0x7: Select safe_mode	RW	0x7
15	KPD_ROW3_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	KPD_ROW3_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	KPD_ROW3_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad kpd_row3 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
12	KPD_ROW3_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad kpd_row3 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	KPD_ROW3_OFFMODEOUTVALUE	OffMode mode output value for pad kpd_row3 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	KPD_ROW3_OFFMODEOUTENABLE	OffMode mode output enable value for pad kpd_row3. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	KPD_ROW3_OFFMODEENABLE	OffMode mode override control for pad kpd_row3 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	KPD_ROW3_INPUTENABLE	Input enable value for pad kpd_row3 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
4	KPD_ROW3_PULLTYPESELECT	pullup/down selection for pad kpd_row3 0x0: pulldown selected 0x1: pullup selected	RW	1
3	KPD_ROW3_PULLUDENABLE	pullup/down enable for pad kpd_row3 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	KPD_ROW3_MUXMODE	Functional multiplexing selection for pad kpd_row3 0x0: Select kpd_row3 0x1: Select kpd_row0 0x2: Select cam2_d4 0x3: Select gpio_175 0x7: Select safe_mode	RW	0x7

Table 18-513. Register Call Summary for Register CONTROL_CORE_PAD0_KPD_ROW3_PAD1_KPD_ROW4

Control Module Functional Description • Pad Multiplexing Register Fields: [0] [1]
Control Module Register Manual • SYSCTRL_PADCONF_CORE Register Summary: [2]

Table 18-514. CONTROL_CORE_PAD0_KPD_ROW5_PAD1_KPD_ROW0

Address Offset	0x0000 018C		
Physical Address	0x4A10 018C	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads kpd_row5 and kpd_row0 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
KPD_ROW0_WAKEUPEVENT	KPD_ROW0_WAKEUPENABLE	RESERVED					KPD_ROW0_INPUTENABLE	RESERVED			KPD_ROW0_PULLTYPESELECT	KPD_ROW0_PULLUDENABLE	KPD_ROW0_MUXMODE			KPD_ROW5_WAKEUPEVENT	KPD_ROW5_WAKEUPENABLE	RESERVED				KPD_ROW5_INPUTENABLE	RESERVED				KPD_ROW5_PULLTYPESELECT	KPD_ROW5_PULLUDENABLE	KPD_ROW5_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	KPD_ROW0_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	KPD_ROW0_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0

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Bits	Field Name	Description	Type	Reset
29	KPD_ROW0_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad kpd_row0	RW	0
		0x0: Offmode pulldown selected		
		0x1: Offmode pullup selected		
28	KPD_ROW0_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad kpd_row0	RW	0
		0x0: Offmode pullup/down disabled		
		0x1: Offmode pullup/down enabled		
27	KPD_ROW0_ OFFMODEOUTVALUE	OffMode mode output value for pad kpd_row0	RW	0
		0x0: Set value at 0.		
		0x1: Set value at 1.		
26	KPD_ROW0_ OFFMODEOUTENABLE	OffMode mode output enable value for pad kpd_row0. This is an active low signal.	RW	0
		0x0: Output enable		
		0x1: Output disable		
25	KPD_ROW0_ OFFMODEENABLE	OffMode mode override control for pad kpd_row0	RW	0
		0x0: I/O state keeps its previous state when off mode is active.		
		0x1: I/O state is forced to off mode value when off mode is active.		
24	KPD_ROW0_INPUTENABLE	Input enable value for pad kpd_row0	RW	1
		0x0: Input buffer of I/O cell is disabled		
		0x1: Input buffer of I/O cell is enabled		
23:21	RESERVED		R	0x0
20	KPD_ROW0_PULLTYPESELECT	pullup/down selection for pad kpd_row0	RW	1
		0x0: pulldown selected		
		0x1: pullup selected		
19	KPD_ROW0_PULLUDENABLE	pullup/down enable for pad kpd_row0	RW	1
		0x0: pullup/down disabled		
		0x1: pullup/down enabled		
18:16	KPD_ROW0_MUXMODE	Functional multiplexing selection for pad kpd_row0	RW	0x7
		0x0: Select kpd_row0		
		0x1: Select kpd_row3		
		0x2: Select cam2_d7		
		0x3: Select gpio_178		
		0x7: Select safe_mode		
15	KPD_ROW5_WAKEUPEVENT	Pad_x wake-up event status latched in the IO	R	0
		Read 0x0: No wake-up event occurred		
		Read 0x1: A wake-up event occurred		
14	KPD_ROW5_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value)	RW	0
		0x0: wake-up detection is disabled		
		0x1: wake-up detection is enabled		
13	KPD_ROW5_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad kpd_row5	RW	0
		0x0: Offmode pulldown selected		
		0x1: Offmode pullup selected		

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Bits	Field Name	Description	Type	Reset
12	KPD_ROW5_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad kpd_row5 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	KPD_ROW5_ OFFMODEOUTVALUE	OffMode mode output value for pad kpd_row5 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	KPD_ROW5_ OFFMODEOUTENABLE	OffMode mode output enable value for pad kpd_row5. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	KPD_ROW5_ OFFMODEENABLE	OffMode mode override control for pad kpd_row5 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	KPD_ROW5_INPUTENABLE	Input enable value for pad kpd_row5 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	KPD_ROW5_PULLTYPESELECT	pullup/down selection for pad kpd_row5 0x0: pulldown selected 0x1: pullup selected	RW	1
3	KPD_ROW5_PULLUDENABLE	pullup/down enable for pad kpd_row5 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	KPD_ROW5_MUXMODE	Functional multiplexing selection for pad kpd_row5 0x0: Select kpd_row5 0x1: Select kpd_row2 0x2: Select cam2_d6 0x3: Select gpio_177 0x7: Select safe_mode	RW	0x7

Table 18-515. Register Call Summary for Register CONTROL_CORE_PAD0_KPD_ROW5_PAD1_KPD_ROW0

Control Module Functional Description • Pad Multiplexing Register Fields: [0] [1]
Control Module Register Manual • SYSCTRL_PADCONF_CORE Register Summary: [2]

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Table 18-516. CONTROL_CORE_PAD0_KPD_ROW1_PAD1_KPD_ROW2

Address Offset	0x0000 0190		
Physical Address	0x4A10 0190	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads kpd_row1 and kpd_row2 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
KPD_ROW2_WAKEUPEVENT	KPD_ROW2_WAKEUPENABLE	RESERVED					KPD_ROW2_INPUTENABLE	RESERVED			KPD_ROW2_PULLTYPESELECT	KPD_ROW2_PULLUDENABLE	KPD_ROW2_MUXMODE			KPD_ROW1_WAKEUPEVENT	KPD_ROW1_WAKEUPENABLE	RESERVED					KPD_ROW1_INPUTENABLE	RESERVED			KPD_ROW1_PULLTYPESELECT	KPD_ROW1_PULLUDENABLE	KPD_ROW1_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	KPD_ROW2_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	KPD_ROW2_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29	KPD_ROW2_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad kpd_row2 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
28	KPD_ROW2_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad kpd_row2 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	KPD_ROW2_OFFMODEOUTVALUE	OffMode mode output value for pad kpd_row2 0x0: Set value at 0. 0x1: Set value at 1.	RW	0
26	KPD_ROW2_OFFMODEOUTENABLE	OffMode mode output enable value for pad kpd_row2. This is an active low signal. 0x0: Output enable 0x1: Output disable	RW	0
25	KPD_ROW2_OFFMODEENABLE	OffMode mode override control for pad kpd_row2 0x0: I/O state keeps its previous state when off mode is active. 0x1: I/O state is forced to off mode value when off mode is active.	RW	0
24	KPD_ROW2_INPUTENABLE	Input enable value for pad kpd_row2 0x0: Input buffee of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
20	KPD_ROW2_PULLTYPESELECT	pullup/down selection for pad kpd_row2 0x0: pulldown selected 0x1: pullup selected	RW	1
19	KPD_ROW2_PULLUDENABLE	pullup/down enable for pad kpd_row2 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	KPD_ROW2_MUXMODE	Functional multiplexing selection for pad kpd_row2 0x0: Select kpd_row2 0x1: Select kpd_row5 0x2: Select cam2_d11 0x3: Select gpio_3 0x7: Select safe_mode	RW	0x7
15	KPD_ROW1_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	KPD_ROW1_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	KPD_ROW1_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad kpd_row1 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
12	KPD_ROW1_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad kpd_row1 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	KPD_ROW1_OFFMODEOUTVALUE	OffMode mode output value for pad kpd_row1 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	KPD_ROW1_OFFMODEOUTENABLE	OffMode mode output enable value for pad kpd_row1. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	KPD_ROW1_OFFMODEENABLE	OffMode mode override control for pad kpd_row1 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	KPD_ROW1_INPUTENABLE	Input enable value for pad kpd_row1 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	KPD_ROW1_PULLTYPESELECT	pullup/down selection for pad kpd_row1 0x0: pulldown selected 0x1: pullup selected	RW	1

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Bits	Field Name	Description	Type	Reset
3	KPD_ROW1_PULLUDENABLE	pullup/down enable for pad kpd_row1 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	KPD_ROW1_MUXMODE	Functional multiplexing selection for pad kpd_row1 0x0: Select kpd_row1 0x1: Select kpd_row4 0x2: Select cam2_d9 0x3: Select gpio_2 0x7: Select safe_mode	RW	0x7

Table 18-517. Register Call Summary for Register CONTROL_CORE_PAD0_KPD_ROW1_PAD1_KPD_ROW2

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- SYSCTRL_PADCONF_CORE Register Summary: [2]

Table 18-518. CONTROL_CORE_PAD0_USBA0_OTG_CE_PAD1_USBA0_OTG_DP

Address Offset	0x0000 0194		
Physical Address	0x4A10 0194	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads usba0_otg_ce and usba0_otg_dp Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
USBA0_OTG_DP_WAKEUPEVENT	USBA0_OTG_DP_WAKEUPENABLE										USBA0_OTG_DP_PULLTYPESELECT	USBA0_OTG_DP_PULLUDENABLE	USBA0_OTG_DP_MUXMODE			RESERVED										USBA0_OTG_CE_PULLTYPESELECT	USBA0_OTG_CE_PULLUDENABLE	RESERVED		

Bits	Field Name	Description	Type	Reset
31	USBA0_OTG_DP_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0x0
30	USBA0_OTG_DP_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: Wake-up detection on low level 0x1: Wake-up detection on high level	RW	0x0
29:21	RESERVED		R	0x000

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Bits	Field Name	Description	Type	Reset
20	USBA0_OTG_DP_PULLTYPESELECT	Pullup/down selection for pad usba0_otg_dp 0x0: Pulldown selected 0x1: Pullup selected	RW	0
19	USBA0_OTG_DP_PULLUDENABLE	Pullup/down enable for pad usba0_otg_dp 0x0: Pullup/down disabled 0x1: Pullup/down enabled	RW	1
18:16	USBA0_OTG_DP_MUXMODE (1)	Functional multiplexing selection for pad usba0_otg_dp 0x0: Select usba0_otg_dp 0x1: Select uart3_rx_irrx 0x2: Select uart2_rx 0x7: Select safe_mode	RW	0x7
15:5	RESERVED		R	0x000
4	USBA0_OTG_CE_PULLTYPESELECT	Pullup/down selection for pad usba0_otg_ce 0x0: Pulldown selected 0x1: Pullup selected	RW	0
3	USBA0_OTG_CE_PULLUDENABLE	Pullup/down enable for pad usba0_otg_ce 0x0: Pullup/down disabled 0x1: Pullup/down enabled	RW	1
2:0	RESERVED		R	0x0

(1) When USBA0_OTG_DP_MUXMODE = 0, user software must ensure that CONTROL_USB2PHYCORE[29] USB2PHY_GPIOMODE = 0. When USBA0_OTG_DP_MUXMODE is different than 0, user software must ensure that CONTROL_USB2PHYCORE[29] USB2PHY_GPIOMODE = 1.

Table 18-519. Register Call Summary for Register CONTROL_CORE_PAD0_USBA0_OTG_CE_PAD1_USBA0_OTG_DP

Control Module Functional Description • Pad Multiplexing Register Fields: [0] [1]
Control Module Register Manual • SYSCTRL_PADCONF_CORE Register Summary: [2]

Table 18-520. CONTROL_CORE_PAD0_USBA0_OTG_DM_PAD1_FREF_CLK1_OUT

Address Offset	0x0000 0198		
Physical Address	0x4A10 0198	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads usba0_otg_dm and fref_clk1_out Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FREF_CLK1_OUT_WAKEUPEVENT	FREF_CLK1_OUT_WAKEUPENABLE	FREF_CLK1_OUT_OFFMODEPULLTYPESELECT	FREF_CLK1_OUT_OFFMODEPULLUDENABLE	FREF_CLK1_OUT_OFFMODEOUTVALUE	FREF_CLK1_OUT_OFFMODEOUTENABLE	FREF_CLK1_OUT_OFFMODEENABLE	FREF_CLK1_OUT_INPUTENABLE	RESERVED			FREF_CLK1_OUT_PULLTYPESELECT	FREF_CLK1_OUT_PULLUDENABLE	FREF_CLK1_OUT_MUXMODE			RESERVED										USBA0_OTG_DM_PULLTYPESELECT	USBA0_OTG_DM_PULLUDENABLE	USBA0_OTG_DM_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	FREF_CLK1_OUT_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	FREF_CLK1_OUT_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29	FREF_CLK1_OUT_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad fref_clk1_out 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
28	FREF_CLK1_OUT_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad fref_clk1_out 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	FREF_CLK1_OUT_OFFMODEOUTVALUE	OffMode mode output value for pad fref_clk1_out 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	FREF_CLK1_OUT_OFFMODEOUTENABLE	OffMode mode output enable value for pad fref_clk1_out. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	FREF_CLK1_OUT_OFFMODEENABLE	OffMode mode override control for pad fref_clk1_out 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
24	FREF_CLK1_OUT_INPUTENABLE	Input enable value for pad fref_clk1_out 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	FREF_CLK1_OUT_PULLTYPESELECT	pullup/down selection for pad fref_clk1_out 0x0: pulldown selected 0x1: pullup selected	RW	0

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Bits	Field Name	Description	Type	Reset
19	FREF_CLK1_OUT_PULLUDENABLE	pullup/down enable for pad fref_clk1_out 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	FREF_CLK1_OUT_MUXMODE	Functional multiplexing selection for pad fref_clk1_out 0x0: Select fref_clk1_out 0x3: Select gpio_181 0x7: Select safe_mode	RW	0x7
15:5	RESERVED		R	0x000
4	USBA0_OTG_DM_PULLTYPESELECT	pullup/down selection for pad usba0_otg_dm 0x0: pulldown selected 0x1: pullup selected	RW	0
3	USBA0_OTG_DM_PULLUDENABLE	pullup/down enable for pad usba0_otg_dm 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	USBA0_OTG_DM_MUXMODE (1)	Functional multiplexing selection for pad usba0_otg_dm 0x0: Select usba0_otg_dm 0x1: Select uart3_tx_irtx 0x2: Select uart2_tx 0x7: Select safe_mode	RW	0x7

(1) When USBA0_OTG_DM_MUXMODE = 0, user software must ensure that CONTROL_USB2PHYCORE[29] USB2PHY_GPIOMODE = 0. When USBA0_OTG_DM_MUXMODE is different than 0, user software must ensure that CONTROL_USB2PHYCORE[29] USB2PHY_GPIOMODE = 1.

Table 18-521. Register Call Summary for Register CONTROL_CORE_PAD0_USBA0_OTG_DM_PAD1_FREF_CLK1_OUT

Control Module Functional Description • Pad Multiplexing Register Fields: [0] [1]
Control Module Register Manual • SYSCTRL_PADCONF_CORE Register Summary: [2]

Table 18-522. CONTROL_CORE_PAD0_FREF_CLK2_OUT_PAD1_SYS_NIRQ1

Address Offset	0x0000 019C		
Physical Address	0x4A10 019C	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads fref_clk2_out and sys_nirq1 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SYS_NIRQ1_WAKEUPEVENT	SYS_NIRQ1_WAKEUPENABLE	RESERVED					SYS_NIRQ1_INPUTENABLE	RESERVED			SYS_NIRQ1_PULLTYPESELECT	SYS_NIRQ1_PULLUDENABLE	SYS_NIRQ1_MUXMODE			FREF_CLK2_OUT_WAKEUPEVENT	FREF_CLK2_OUT_WAKEUPENABLE	FREF_CLK2_OUT_OFFMODEPULLTYPESELECT	FREF_CLK2_OUT_OFFMODEPULLUDENABLE	FREF_CLK2_OUT_OFFMODEOUTVALUE	FREF_CLK2_OUT_OFFMODEOUTENABLE	FREF_CLK2_OUT_OFFMODEENABLE	FREF_CLK2_OUT_INPUTENABLE	RESERVED			FREF_CLK2_OUT_PULLTYPESELECT	FREF_CLK2_OUT_PULLUDENABLE	FREF_CLK2_OUT_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	SYS_NIRQ1_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	SYS_NIRQ1_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x00
24	SYS_NIRQ1_INPUTENABLE	Input enable value for pad sys_nirq1 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	SYS_NIRQ1_PULLTYPESELECT	pullup/down selection for pad sys_nirq1 0x0: pulldown selected 0x1: pullup selected	RW	1
19	SYS_NIRQ1_PULLUDENABLE	pullup/down enable for pad sys_nirq1 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	SYS_NIRQ1_MUXMODE	Functional multiplexing selection for pad sys_nirq1 0x0: Select sys_nirq1 0x7: Select safe_mode	RW	0x7
15	FREF_CLK2_OUT_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	FREF_CLK2_OUT_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	FREF_CLK2_OUT_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad fref_clk2_out 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0

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Bits	Field Name	Description	Type	Reset
12	FREF_CLK2_OUT_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad fref_clk2_out 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	FREF_CLK2_OUT_OFFMODEOUTVALUE	OffMode mode output value for pad fref_clk2_out 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	FREF_CLK2_OUT_OFFMODEOUTENABLE	OffMode mode output enable value for pad fref_clk2_out. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	FREF_CLK2_OUT_OFFMODEENABLE	OffMode mode override control for pad fref_clk2_out 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	FREF_CLK2_OUT_INPUTENABLE	Input enable value for pad fref_clk2_out 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	FREF_CLK2_OUT_PULLTYPESELECT	pullup/down selection for pad fref_clk2_out 0x0: pulldown selected 0x1: pullup selected	RW	0
3	FREF_CLK2_OUT_PULLUDENABLE	pullup/down enable for pad fref_clk2_out 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	FREF_CLK2_OUT_MUXMODE	Functional multiplexing selection for pad fref_clk2_out 0x0: Select fref_clk2_out 0x3: Select gpio_182 0x7: Select safe_mode	RW	0x7

Table 18-523. Register Call Summary for Register CONTROL_CORE_PAD0_FREF_CLK2_OUT_PAD1_SYS_NIRQ1

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- SYSCTRL_PADCONF_CORE Register Summary: [2]

Table 18-524. CONTROL_CORE_PAD0_SYS_NIRQ2_PAD1_SYS_BOOT0

Address Offset	0x0000 01A0		
Physical Address	0x4A10 01A0	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads sys_nirq2 and sys_boot0 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SYS_BOOT0_WAKEUPEVENT	SYS_BOOT0_WAKEUPENABLE	SYS_BOOT0_OFFMODEPULLTYPESELECT	SYS_BOOT0_OFFMODEPULLUDENABLE	SYS_BOOT0_OFFMODEOUTVALUE	SYS_BOOT0_OFFMODEOUTENABLE	SYS_BOOT0_OFFMODEENABLE	SYS_BOOT0_INPUTENABLE	RESERVED			SYS_BOOT0_PULLTYPESELECT	SYS_BOOT0_PULLUDENABLE	SYS_BOOT0_MUXMODE			SYS_NIRQ2_WAKEUPEVENT	SYS_NIRQ2_WAKEUPENABLE	SYS_NIRQ2_OFFMODEPULLTYPESELECT	SYS_NIRQ2_OFFMODEPULLUDENABLE	SYS_NIRQ2_OFFMODEOUTVALUE	SYS_NIRQ2_OFFMODEOUTENABLE	SYS_NIRQ2_OFFMODEENABLE	SYS_NIRQ2_INPUTENABLE	RESERVED			SYS_NIRQ2_PULLTYPESELECT	SYS_NIRQ2_PULLUDENABLE	SYS_NIRQ2_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	SYS_BOOT0_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	SYS_BOOT0_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29	SYS_BOOT0_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad sys_boot0 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
28	SYS_BOOT0_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad sys_boot0 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	SYS_BOOT0_ OFFMODEOUTVALUE	OffMode mode output value for pad sys_boot0 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	SYS_BOOT0_ OFFMODEOUTENABLE	OffMode mode output enable value for pad sys_boot0. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	SYS_BOOT0_OFFMODEENABLE	OffMode mode override control for pad sys_boot0 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
24	SYS_BOOT0_INPUTENABLE	Input enable value for pad sys_boot0 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	SYS_BOOT0_PULLTYPESELECT	pullup/down selection for pad sys_boot0 0x0: pulldown selected 0x1: pullup selected	RW	0
19	SYS_BOOT0_PULLUDENABLE	pullup/down enable for pad sys_boot0 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1

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Bits	Field Name	Description	Type	Reset
18:16	SYS_BOOT0_MUXMODE	Functional multiplexing selection for pad sys_boot0 0x0: Select sys_boot0 0x3: Select gpio_184 0x7: Select safe_mode	RW	0x0
15	SYS_NIRQ2_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	SYS_NIRQ2_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	SYS_NIRQ2_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad sys_nirq2 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
12	SYS_NIRQ2_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad sys_nirq2 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	SYS_NIRQ2_ OFFMODEOUTVALUE	OffMode mode output value for pad sys_nirq2 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	SYS_NIRQ2_ OFFMODEOUTENABLE	OffMode mode output enable value for pad sys_nirq2. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	SYS_NIRQ2_OFFMODEENABLE	OffMode mode override control for pad sys_nirq2 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	SYS_NIRQ2_INPUTENABLE	Input enable value for pad sys_nirq2 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	SYS_NIRQ2_PULLTYPESELECT	pullup/down selection for pad sys_nirq2 0x0: pulldown selected 0x1: pullup selected	RW	1
3	SYS_NIRQ2_PULLUDENABLE	pullup/down enable for pad sys_nirq2 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	SYS_NIRQ2_MUXMODE	Functional multiplexing selection for pad sys_nirq2 0x0: Select sys_nirq2 0x3: Select gpio_183 0x7: Select safe_mode	RW	0x7

Table 18-525. Register Call Summary for Register CONTROL_CORE_PAD0_SYS_NIRQ2_PAD1_SYS_BOOT0

Control Module Functional Description • Pad Multiplexing Register Fields: [0] [1]
Control Module Register Manual • SYSCTRL_PADCONF_CORE Register Summary: [2]

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Table 18-526. CONTROL_CORE_PAD0_SYS_BOOT1_PAD1_SYS_BOOT2

Address Offset	0x0000 01A4		
Physical Address	0x4A10 01A4	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads sys_boot1 and sys_boot2 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SYS_BOOT2_WAKEUPEVENT	SYS_BOOT2_WAKEUPENABLE	SYS_BOOT2_OFFMODEPULLTYPESELECT	SYS_BOOT2_OFFMODEPULLUDENABLE	SYS_BOOT2_OFFMODEOUTVALUE	SYS_BOOT2_OFFMODEOUTENABLE	SYS_BOOT2_OFFMODEENABLE	SYS_BOOT2_INPUTENABLE	RESERVED			SYS_BOOT2_PULLTYPESELECT	SYS_BOOT2_PULLUDENABLE	SYS_BOOT2_MUXMODE			SYS_BOOT1_WAKEUPEVENT	SYS_BOOT1_WAKEUPENABLE	SYS_BOOT1_OFFMODEPULLTYPESELECT	SYS_BOOT1_OFFMODEPULLUDENABLE	SYS_BOOT1_OFFMODEOUTVALUE	SYS_BOOT1_OFFMODEOUTENABLE	SYS_BOOT1_OFFMODEENABLE	SYS_BOOT1_INPUTENABLE	RESERVED			SYS_BOOT1_PULLTYPESELECT	SYS_BOOT1_PULLUDENABLE	SYS_BOOT1_MUXMODE	

Bits	Field Name	Description	Type	Reset
31	SYS_BOOT2_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	SYS_BOOT2_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29	SYS_BOOT2_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad sys_boot2 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
28	SYS_BOOT2_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad sys_boot2 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	SYS_BOOT2_ OFFMODEOUTVALUE	OffMode mode output value for pad sys_boot2 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	SYS_BOOT2_ OFFMODEOUTENABLE	OffMode mode output enable value for pad sys_boot2. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	SYS_BOOT2_OFFMODEENABLE	OffMode mode override control for pad sys_boot2 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
24	SYS_BOOT2_INPUTENABLE	Input enable value for pad sys_boot2 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1

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Bits	Field Name	Description	Type	Reset
23:21	RESERVED		R	0x0
20	SYS_BOOT2_PULLTYPESELECT	pullup/down selection for pad sys_boot2 0x0: pulldown selected 0x1: pullup selected	RW	0
19	SYS_BOOT2_PULLUDENABLE	pullup/down enable for pad sys_boot2 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	SYS_BOOT2_MUXMODE	Functional multiplexing selection for pad sys_boot2 0x0: Select sys_boot2 0x3: Select gpio_186 0x7: Select safe_mode	RW	0x0
15	SYS_BOOT1_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	SYS_BOOT1_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	SYS_BOOT1_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad sys_boot1 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
12	SYS_BOOT1_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad sys_boot1 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	SYS_BOOT1_OFFMODEOUTVALUE	OffMode mode output value for pad sys_boot1 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	SYS_BOOT1_OFFMODEOUTENABLE	OffMode mode output enable value for pad sys_boot1. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	SYS_BOOT1_OFFMODEENABLE	OffMode mode override control for pad sys_boot1 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	SYS_BOOT1_INPUTENABLE	Input enable value for pad sys_boot1 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	SYS_BOOT1_PULLTYPESELECT	pullup/down selection for pad sys_boot1 0x0: pulldown selected 0x1: pullup selected	RW	0
3	SYS_BOOT1_PULLUDENABLE	pullup/down enable for pad sys_boot1 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	SYS_BOOT1_MUXMODE	Functional multiplexing selection for pad sys_boot1 0x0: Select sys_boot1 0x3: Select gpio_185 0x7: Select safe_mode	RW	0x0

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Table 18-527. Register Call Summary for Register CONTROL_CORE_PAD0_SYS_BOOT1_PAD1_SYS_BOOT2

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- SYSCTRL_PADCONF_CORE Register Summary: [2]

Table 18-528. CONTROL_CORE_PAD0_SYS_BOOT3_PAD1_SYS_BOOT4

Address Offset	0x0000 01A8		
Physical Address	0x4A10 01A8	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads sys_boot3 and sys_boot4 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SYS_BOOT4_WAKEUPEVENT	SYS_BOOT4_WAKEUPENABLE	SYS_BOOT4_OFFMODEPULLTYPESELECT	SYS_BOOT4_OFFMODEPULLUDENABLE	SYS_BOOT4_OFFMODEOUTVALUE	SYS_BOOT4_OFFMODEOUTENABLE	SYS_BOOT4_OFFMODEENABLE	SYS_BOOT4_INPUTENABLE	RESERVED			SYS_BOOT4_PULLTYPESELECT	SYS_BOOT4_PULLUDENABLE	SYS_BOOT4_MUXMODE			SYS_BOOT3_WAKEUPEVENT	SYS_BOOT3_WAKEUPENABLE	SYS_BOOT3_OFFMODEPULLTYPESELECT	SYS_BOOT3_OFFMODEPULLUDENABLE	SYS_BOOT3_OFFMODEOUTVALUE	SYS_BOOT3_OFFMODEOUTENABLE	SYS_BOOT3_OFFMODEENABLE	SYS_BOOT3_INPUTENABLE	RESERVED			SYS_BOOT3_PULLTYPESELECT	SYS_BOOT3_PULLUDENABLE	SYS_BOOT3_MUXMODE	

Bits	Field Name	Description	Type	Reset
31	SYS_BOOT4_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	SYS_BOOT4_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29	SYS_BOOT4_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad sys_boot4 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
28	SYS_BOOT4_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad sys_boot4 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	SYS_BOOT4_OFFMODEOUTVALUE	OffMode mode output value for pad sys_boot4 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	SYS_BOOT4_OFFMODEOUTENABLE	OffMode mode output enable value for pad sys_boot4. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0

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Bits	Field Name	Description	Type	Reset
25	SYS_BOOT4_OFFMODEENABLE	OffMode mode override control for pad sys_boot4 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
24	SYS_BOOT4_INPUTENABLE	Input enable value for pad sys_boot4 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	SYS_BOOT4_PULLTYPESELECT	pullup/down selection for pad sys_boot4 0x0: pulldown selected 0x1: pullup selected	RW	0
19	SYS_BOOT4_PULLUDENABLE	pullup/down enable for pad sys_boot4 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	SYS_BOOT4_MUXMODE	Functional multiplexing selection for pad sys_boot4 0x0: Select sys_boot4 0x3: Select gpio_188 0x7: Select safe_mode	RW	0x0
15	SYS_BOOT3_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	SYS_BOOT3_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	SYS_BOOT3_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad sys_boot3 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
12	SYS_BOOT3_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad sys_boot3 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	SYS_BOOT3_OFFMODEOUTVALUE	OffMode mode output value for pad sys_boot3 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	SYS_BOOT3_OFFMODEOUTENABLE	OffMode mode output enable value for pad sys_boot3. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	SYS_BOOT3_OFFMODEENABLE	OffMode mode override control for pad sys_boot3 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	SYS_BOOT3_INPUTENABLE	Input enable value for pad sys_boot3 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	SYS_BOOT3_PULLTYPESELECT	pullup/down selection for pad sys_boot3 0x0: pulldown selected 0x1: pullup selected	RW	0

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Bits	Field Name	Description	Type	Reset
3	SYS_BOOT3_PULLUDENABLE	pullup/down enable for pad sys_boot3 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	SYS_BOOT3_MUXMODE	Functional multiplexing selection for pad sys_boot3 0x0: Select sys_boot3 0x3: Select gpio_187 0x7: Select safe_mode	RW	0x0

Table 18-529. Register Call Summary for Register CONTROL_CORE_PAD0_SYS_BOOT3_PAD1_SYS_BOOT4

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- SYSCTRL_PADCONF_CORE Register Summary: [2]

Table 18-530. CONTROL_CORE_PAD0_SYS_BOOT5_PAD1_DPM_EMU0

Address Offset	0x0000 01AC		
Physical Address	0x4A10 01AC	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads sys_boot5 and dpm_emu0 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DPM_EMU0_WAKEUPEVENT	DPM_EMU0_WAKEUPENABLE	DPM_EMU0_OFFMODEPULLTYPESELECT	DPM_EMU0_OFFMODEPULLUDENABLE	DPM_EMU0_OFFMODEOUTVALUE	DPM_EMU0_OFFMODEOUTENABLE	DPM_EMU0_OFFMODEENABLE	DPM_EMU0_INPUTENABLE	RESERVED			DPM_EMU0_PULLTYPESELECT	DPM_EMU0_PULLUDENABLE	DPM_EMU0_MUXMODE			SYS_BOOT5_WAKEUPEVENT	SYS_BOOT5_WAKEUPENABLE	SYS_BOOT5_OFFMODEPULLTYPESELECT	SYS_BOOT5_OFFMODEPULLUDENABLE	SYS_BOOT5_OFFMODEOUTVALUE	SYS_BOOT5_OFFMODEOUTENABLE	SYS_BOOT5_OFFMODEENABLE	SYS_BOOT5_INPUTENABLE	RESERVED			SYS_BOOT5_PULLTYPESELECT	SYS_BOOT5_PULLUDENABLE	SYS_BOOT5_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	DPM_EMU0_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	DPM_EMU0_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29	DPM_EMU0_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad dpm_emu0 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0

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Bits	Field Name	Description	Type	Reset
28	DPM_EMU0_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad dpm_emu0 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	DPM_EMU0_ OFFMODEOUTVALUE	OffMode mode output value for pad dpm_emu0 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	DPM_EMU0_ OFFMODEOUTENABLE	OffMode mode output enable value for pad dpm_emu0. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	DPM_EMU0_ OFFMODEENABLE	OffMode mode override control for pad dpm_emu0 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
24	DPM_EMU0_INPUTENABLE	Input enable value for pad dpm_emu0 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	DPM_EMU0_PULLTYPESELECT	pullup/down selection for pad dpm_emu0 0x0: pulldown selected 0x1: pullup selected	RW	1
19	DPM_EMU0_PULLUDENABLE	pullup/down enable for pad dpm_emu0 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	DPM_EMU0_MUXMODE	Functional multiplexing selection for pad dpm_emu0 0x0: Select dpm_emu0 0x3: Select gpio_11 0x6: Select hw_dbg0 0x7: Select safe_mode	RW	0x0
15	SYS_BOOT5_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	SYS_BOOT5_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	SYS_BOOT5_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad sys_boot5 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
12	SYS_BOOT5_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad sys_boot5 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	SYS_BOOT5_ OFFMODEOUTVALUE	OffMode mode output value for pad sys_boot5 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	SYS_BOOT5_ OFFMODEOUTENABLE	OffMode mode output enable value for pad sys_boot5. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0

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Bits	Field Name	Description	Type	Reset
9	SYS_BOOT5_OFFMODEENABLE	OffMode mode override control for pad sys_boot5 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	SYS_BOOT5_INPUTENABLE	Input enable value for pad sys_boot5 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	SYS_BOOT5_PULLTYPESELECT	pullup/down selection for pad sys_boot5 0x0: pulldown selected 0x1: pullup selected	RW	0
3	SYS_BOOT5_PULLUDENABLE	pullup/down enable for pad sys_boot5 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	SYS_BOOT5_MUXMODE	Functional multiplexing selection for pad sys_boot5 0x0: Select sys_boot5 0x3: Select gpio_189 0x7: Select safe_mode	RW	0x0

Table 18-531. Register Call Summary for Register CONTROL_CORE_PAD0_SYS_BOOT5_PAD1_DPM_EMU0

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]
- Observability Signals Multiplexing at Device Control Module Level: [2]

Control Module Register Manual
- SYSCTRL_PADCONF_CORE Register Summary: [3]

Table 18-532. CONTROL_CORE_PAD0_DPM_EMU1_PAD1_DPM_EMU2

Address Offset	0x0000 01B0		
Physical Address	0x4A10 01B0	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads dpm_emu1 and dpm_emu2 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DPM_EMU2_WAKEUPEVENT	DPM_EMU2_WAKEUPENABLE	DPM_EMU2_OFFMODEPULLTYPESELECT	DPM_EMU2_OFFMODEPULLUDENABLE	DPM_EMU2_OFFMODEOUTVALUE	DPM_EMU2_OFFMODEOUTENABLE	DPM_EMU2_OFFMODEENABLE	DPM_EMU2_INPUTENABLE	RESERVED			DPM_EMU2_PULLTYPESELECT	DPM_EMU2_PULLUDENABLE	DPM_EMU2_MUXMODE			DPM_EMU1_WAKEUPEVENT	DPM_EMU1_WAKEUPENABLE	DPM_EMU1_OFFMODEPULLTYPESELECT	DPM_EMU1_OFFMODEPULLUDENABLE	DPM_EMU1_OFFMODEOUTVALUE	DPM_EMU1_OFFMODEOUTENABLE	DPM_EMU1_OFFMODEENABLE	DPM_EMU1_INPUTENABLE	RESERVED			DPM_EMU1_PULLTYPESELECT	DPM_EMU1_PULLUDENABLE	DPM_EMU1_MUXMODE	

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Bits	Field Name	Description	Type	Reset
31	DPM_EMU2_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	DPM_EMU2_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29	DPM_EMU2_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad dpm_emu2 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
28	DPM_EMU2_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad dpm_emu2 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	DPM_EMU2_OFFMODEOUTVALUE	OffMode mode output value for pad dpm_emu2 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	DPM_EMU2_OFFMODEOUTENABLE	OffMode mode output enable value for pad dpm_emu2. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	DPM_EMU2_OFFMODEENABLE	OffMode mode override control for pad dpm_emu2 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
24	DPM_EMU2_INPUTENABLE	Input enable value for pad dpm_emu2 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	DPM_EMU2_PULLTYPESELECT	pullup/down selection for pad dpm_emu2 0x0: pulldown selected 0x1: pullup selected	RW	0
19	DPM_EMU2_PULLUDENABLE	pullup/down enable for pad dpm_emu2 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	DPM_EMU2_MUXMODE	Functional multiplexing selection for pad dpm_emu2 0x0: Select dpm_emu2 0x1: Select usba0_ulpiphy_clk 0x3: Select gpio_13 0x5: Select dispc2_fid 0x6: Select hw_dbg2 0x7: Select safe_mode	RW	0x7
15	DPM_EMU1_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	DPM_EMU1_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0

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Bits	Field Name	Description	Type	Reset
13	DPM_EMU1_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad dpm_emu1 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
12	DPM_EMU1_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad dpm_emu1 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	DPM_EMU1_ OFFMODEOUTVALUE	OffMode mode output value for pad dpm_emu1 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	DPM_EMU1_ OFFMODEOUTENABLE	OffMode mode output enable value for pad dpm_emu1. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	DPM_EMU1_ OFFMODEENABLE	OffMode mode override control for pad dpm_emu1 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	DPM_EMU1_INPUTENABLE	Input enable value for pad dpm_emu1 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	DPM_EMU1_ PULLTYPESELECT	pullup/down selection for pad dpm_emu1 0x0: pulldown selected 0x1: pullup selected	RW	1
3	DPM_EMU1_PULLUDENABLE	pullup/down enable for pad dpm_emu1 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	DPM_EMU1_MUXMODE	Functional multiplexing selection for pad dpm_emu1 0x0: Select dpm_emu1 0x3: Select gpio_12 0x6: Select hw_dbg1 0x7: Select safe_mode	RW	0x0

Table 18-533. Register Call Summary for Register CONTROL_CORE_PAD0_DPM_EMU1_PAD1_DPM_EMU2

Control Module Functional Description • Pad Multiplexing Register Fields: [0] [1]
Control Module Register Manual • SYSCTRL_PADCONF_CORE Register Summary: [2]

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Table 18-534. CONTROL_CORE_PAD0_DPM_EMU3_PAD1_DPM_EMU4

Address Offset	0x0000 01B4		
Physical Address	0x4A10 01B4	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads dpm_emu3 and dpm_emu4 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DPM_EMU4_WAKEUPEVENT	DPM_EMU4_WAKEUPENABLE	DPM_EMU4_OFFMODEPULLTYPESELECT	DPM_EMU4_OFFMODEPULLUDENABLE	DPM_EMU4_OFFMODEOUTVALUE	DPM_EMU4_OFFMODEOUTENABLE	DPM_EMU4_OFFMODEENABLE	DPM_EMU4_INPUTENABLE	RESERVED			DPM_EMU4_PULLTYPESELECT	DPM_EMU4_PULLUDENABLE	DPM_EMU4_MUXMODE			DPM_EMU3_WAKEUPEVENT	DPM_EMU3_WAKEUPENABLE	DPM_EMU3_OFFMODEPULLTYPESELECT	DPM_EMU3_OFFMODEPULLUDENABLE	DPM_EMU3_OFFMODEOUTVALUE	DPM_EMU3_OFFMODEOUTENABLE	DPM_EMU3_OFFMODEENABLE	DPM_EMU3_INPUTENABLE	RESERVED			DPM_EMU3_PULLTYPESELECT	DPM_EMU3_PULLUDENABLE	DPM_EMU3_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	DPM_EMU4_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	DPM_EMU4_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29	DPM_EMU4_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad dpm_emu4 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
28	DPM_EMU4_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad dpm_emu4 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	DPM_EMU4_ OFFMODEOUTVALUE	OffMode mode output value for pad dpm_emu4 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	DPM_EMU4_ OFFMODEOUTENABLE	OffMode mode output enable value for pad dpm_emu4. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	DPM_EMU4_OFFMODEENABLE	OffMode mode override control for pad dpm_emu4 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
24	DPM_EMU4_INPUTENABLE	Input enable value for pad dpm_emu4 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1

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Bits	Field Name	Description	Type	Reset
23:21	RESERVED		R	0x0
20	DPM_EMU4_PULLTYPESELECT	pullup/down selection for pad dpm_emu4 0x0: pulldown selected 0x1: pullup selected	RW	0
19	DPM_EMU4_PULLUDENABLE	pullup/down enable for pad dpm_emu4 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	DPM_EMU4_MUXMODE	Functional multiplexing selection for pad dpm_emu4 0x0: Select dpm_emu4 0x1: Select usba0_ulpiphy_dir 0x3: Select gpio_15 0x4: Select rfbi_data9 0x5: Select dispc2_data9 0x6: Select hw_dbg4 0x7: Select safe_mode	RW	0x7
15	DPM_EMU3_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	DPM_EMU3_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	DPM_EMU3_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad dpm_emu3 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
12	DPM_EMU3_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad dpm_emu3 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	DPM_EMU3_OFFMODEOUTVALUE	OffMode mode output value for pad dpm_emu3 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	DPM_EMU3_OFFMODEOUTENABLE	OffMode mode output enable value for pad dpm_emu3. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	DPM_EMU3_OFFMODEENABLE	OffMode mode override control for pad dpm_emu3 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	DPM_EMU3_INPUTENABLE	Input enable value for pad dpm_emu3 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	DPM_EMU3_PULLTYPESELECT	pullup/down selection for pad dpm_emu3 0x0: pulldown selected 0x1: pullup selected	RW	0
3	DPM_EMU3_PULLUDENABLE	pullup/down enable for pad dpm_emu3 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1

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Bits	Field Name	Description	Type	Reset
2:0	DPM_EMU3_MUXMODE	Functional multiplexing selection for pad dpm_emu3 0x0: Select dpm_emu3 0x1: Select usba0_ulpiphy_stp 0x3: Select gpio_14 0x4: Select rfbi_data10 0x5: Select dispc2_data10 0x6: Select hw_dbg3 0x7: Select safe_mode	RW	0x7

Table 18-535. Register Call Summary for Register CONTROL_CORE_PAD0_DPM_EMU3_PAD1_DPM_EMU4

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- SYSCTRL_PADCONF_CORE Register Summary: [2]

Table 18-536. CONTROL_CORE_PAD0_DPM_EMU5_PAD1_DPM_EMU6

Address Offset	0x0000 01B8		
Physical Address	0x4A10 01B8	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads dpm_emu5 and dpm_emu6 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DPM_EMU6_WAKEUPEVENT	DPM_EMU6_WAKEUPENABLE	DPM_EMU6_OFFMODEPULLTYPESELECT	DPM_EMU6_OFFMODEPULLUDENABLE	DPM_EMU6_OFFMODEOUTVALUE	DPM_EMU6_OFFMODEOUTENABLE	DPM_EMU6_OFFMODEENABLE	DPM_EMU6_INPUTENABLE	RESERVED			DPM_EMU6_PULLTYPESELECT	DPM_EMU6_PULLUDENABLE	DPM_EMU6_MUXMODE			DPM_EMU5_WAKEUPEVENT	DPM_EMU5_WAKEUPENABLE	DPM_EMU5_OFFMODEPULLTYPESELECT	DPM_EMU5_OFFMODEPULLUDENABLE	DPM_EMU5_OFFMODEOUTVALUE	DPM_EMU5_OFFMODEOUTENABLE	DPM_EMU5_OFFMODEENABLE	DPM_EMU5_INPUTENABLE	RESERVED			DPM_EMU5_PULLTYPESELECT	DPM_EMU5_PULLUDENABLE	DPM_EMU5_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	DPM_EMU6_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	DPM_EMU6_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29	DPM_EMU6_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad dpm_emu6 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0

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Bits	Field Name	Description	Type	Reset
28	DPM_EMU6_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad dpm_emu6 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	DPM_EMU6_ OFFMODEOUTVALUE	OffMode mode output value for pad dpm_emu6 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	DPM_EMU6_ OFFMODEOUTENABLE	OffMode mode output enable value for pad dpm_emu6. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	DPM_EMU6_ OFFMODEENABLE	OffMode mode override control for pad dpm_emu6 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
24	DPM_EMU6_INPUTENABLE	Input enable value for pad dpm_emu6 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	DPM_EMU6_PULLTYPESELECT	pullup/down selection for pad dpm_emu6 0x0: pulldown selected 0x1: pullup selected	RW	0
19	DPM_EMU6_PULLUDENABLE	pullup/down enable for pad dpm_emu6 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	DPM_EMU6_MUXMODE	Functional multiplexing selection for pad dpm_emu6 0x0: Select dpm_emu6 0x1: Select usba0_ulpiphy_dat0 0x2: Select uart3_tx_irtx 0x3: Select gpio_17 0x4: Select rfbi_hsync0 0x5: Select dispc2_data17 0x6: Select hw_dbg6 0x7: Select safe_mode	RW	0x7
15	DPM_EMU5_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	DPM_EMU5_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	DPM_EMU5_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad dpm_emu5 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
12	DPM_EMU5_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad dpm_emu5 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	DPM_EMU5_ OFFMODEOUTVALUE	OffMode mode output value for pad dpm_emu5 0x0: Set value at 0 0x1: Set value at 1	RW	0

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Bits	Field Name	Description	Type	Reset
10	DPM_EMU5_ OFFMODEOUTENABLE	OffMode mode output enable value for pad dpm_emu5. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	DPM_EMU5_ OFFMODEENABLE	OffMode mode override control for pad dpm_emu5 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	DPM_EMU5_INPUTENABLE	Input enable value for pad dpm_emu5 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	DPM_EMU5_PULLTYPESELECT	pullup/down selection for pad dpm_emu5 0x0: pulldown selected 0x1: pullup selected	RW	0
3	DPM_EMU5_PULLUDENABLE	pullup/down enable for pad dpm_emu5 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	DPM_EMU5_MUXMODE	Functional multiplexing selection for pad dpm_emu5 0x0: Select dpm_emu5 0x1: Select usba0_ulpiphy_nxt 0x3: Select gpio_16 0x4: Select rfbi_te_vsync0 0x5: Select dispc2_data16 0x6: Select hw_dbg5 0x7: Select safe_mode	RW	0x7

Table 18-537. Register Call Summary for Register CONTROL_CORE_PAD0_DPM_EMU5_PAD1_DPM_EMU6

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- SYSCTRL_PADCONF_CORE Register Summary: [2]

Table 18-538. CONTROL_CORE_PAD0_DPM_EMU7_PAD1_DPM_EMU8

Address Offset	0x0000 01BC		
Physical Address	0x4A10 01BC	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads dpm_emu7 and dpm_emu8 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DPM_EMU8_WAKEUPEVENT	DPM_EMU8_WAKEUPENABLE	DPM_EMU8_OFFMODEPULLTYPESELECT	DPM_EMU8_OFFMODEPULLUDENABLE	DPM_EMU8_OFFMODEOUTVALUE	DPM_EMU8_OFFMODEOUTENABLE	DPM_EMU8_OFFMODEENABLE	DPM_EMU8_INPUTENABLE	RESERVED			DPM_EMU8_PULLTYPESELECT	DPM_EMU8_PULLUDENABLE	DPM_EMU8_MUXMODE			DPM_EMU7_WAKEUPEVENT	DPM_EMU7_WAKEUPENABLE	DPM_EMU7_OFFMODEPULLTYPESELECT	DPM_EMU7_OFFMODEPULLUDENABLE	DPM_EMU7_OFFMODEOUTVALUE	DPM_EMU7_OFFMODEOUTENABLE	DPM_EMU7_OFFMODEENABLE	DPM_EMU7_INPUTENABLE	RESERVED			DPM_EMU7_PULLTYPESELECT	DPM_EMU7_PULLUDENABLE	DPM_EMU7_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	DPM_EMU8_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	DPM_EMU8_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29	DPM_EMU8_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad dpm_emu8 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
28	DPM_EMU8_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad dpm_emu8 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	DPM_EMU8_ OFFMODEOUTVALUE	OffMode mode output value for pad dpm_emu8 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	DPM_EMU8_ OFFMODEOUTENABLE	OffMode mode output enable value for pad dpm_emu8. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	DPM_EMU8_OFFMODEENABLE	OffMode mode override control for pad dpm_emu8 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
24	DPM_EMU8_INPUTENABLE	Input enable value for pad dpm_emu8 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	DPM_EMU8_PULLTYPESELECT	pullup/down selection for pad dpm_emu8 0x0: pulldown selected 0x1: pullup selected	RW	0
19	DPM_EMU8_PULLUDENABLE	pullup/down enable for pad dpm_emu8 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1

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Bits	Field Name	Description	Type	Reset
18:16	DPM_EMU8_MUXMODE	Functional multiplexing selection for pad dpm_emu8 0x0: Select dpm_emu8 0x1: Select usba0_ulpiphy_dat2 0x2: Select uart3_rts_sd 0x3: Select gpio_19 0x4: Select rfbi_re 0x5: Select dispc2_pclk 0x6: Select hw_dbg8 0x7: Select safe_mode	RW	0x7
15	DPM_EMU7_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	DPM_EMU7_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	DPM_EMU7_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad dpm_emu7 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
12	DPM_EMU7_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad dpm_emu7 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	DPM_EMU7_ OFFMODEOUTVALUE	OffMode mode output value for pad dpm_emu7 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	DPM_EMU7_ OFFMODEOUTENABLE	OffMode mode output enable value for pad dpm_emu7. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	DPM_EMU7_OFFMODEENABLE	OffMode mode override control for pad dpm_emu7 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	DPM_EMU7_INPUTENABLE	Input enable value for pad dpm_emu7 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	DPM_EMU7_PULLTYPESELECT	pullup/down selection for pad dpm_emu7 0x0: pulldown selected 0x1: pullup selected	RW	0
3	DPM_EMU7_PULLUDENABLE	pullup/down enable for pad dpm_emu7 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1

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Bits	Field Name	Description	Type	Reset
2:0	DPM_EMU7_MUXMODE	Functional multiplexing selection for pad dpm_emu7	RW	0x7
		0x0: Select dpm_emu7		
		0x1: Select usba0_ulpiphy_dat1		
		0x2: Select uart3_rx_irrx		
		0x3: Select gpio_18		
		0x4: Select rfbi_cs0		
		0x5: Select dispc2_hsync		
		0x6: Select hw_dbg7		
		0x7: Select safe_mode		

Table 18-539. Register Call Summary for Register CONTROL_CORE_PAD0_DPM_EMU7_PAD1_DPM_EMU8

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- SYSCTRL_PADCONF_CORE Register Summary: [2]

Table 18-540. CONTROL_CORE_PAD0_DPM_EMU9_PAD1_DPM_EMU10

Address Offset	0x0000 01C0		
Physical Address	0x4A10 01C0	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads dpm_emu9 and dpm_emu10 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DPM_EMU10_WAKEUPEVENT	DPM_EMU10_WAKEUPENABLE	DPM_EMU10_OFFMODEPULLTYPESELECT	DPM_EMU10_OFFMODEPULLUDENABLE	DPM_EMU10_OFFMODEOUTVALUE	DPM_EMU10_OFFMODEOUTENABLE	DPM_EMU10_OFFMODEENABLE	DPM_EMU10_INPUTENABLE	RESERVED			DPM_EMU10_PULLTYPESELECT	DPM_EMU10_PULLUDENABLE	DPM_EMU10_MUXMODE			DPM_EMU9_WAKEUPEVENT	DPM_EMU9_WAKEUPENABLE	DPM_EMU9_OFFMODEPULLTYPESELECT	DPM_EMU9_OFFMODEPULLUDENABLE	DPM_EMU9_OFFMODEOUTVALUE	DPM_EMU9_OFFMODEOUTENABLE	DPM_EMU9_OFFMODEENABLE	DPM_EMU9_INPUTENABLE	RESERVED			DPM_EMU9_PULLTYPESELECT	DPM_EMU9_PULLUDENABLE	DPM_EMU9_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	DPM_EMU10_WAKEUPEVENT	Pad_x wake-up event status latched in the IO	R	0
		Read 0x0: No wake-up event occurred		
		Read 0x1: A wake-up event occurred		
30	DPM_EMU10_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value)	RW	0
		0x0: wake-up detection is disabled		
		0x1: wake-up detection is enabled		

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Bits	Field Name	Description	Type	Reset
29	DPM_EMU10_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad dpm_emu10 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
28	DPM_EMU10_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad dpm_emu10 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	DPM_EMU10_ OFFMODEOUTVALUE	OffMode mode output value for pad dpm_emu10 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	DPM_EMU10_ OFFMODEOUTENABLE	OffMode mode output enable value for pad dpm_emu10. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	DPM_EMU10_ OFFMODEENABLE	OffMode mode override control for pad dpm_emu10 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
24	DPM_EMU10_INPUTENABLE	Input enable value for pad dpm_emu10 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	DPM_EMU10_PULLTYPESELECT	pullup/down selection for pad dpm_emu10 0x0: pulldown selected 0x1: pullup selected	RW	0
19	DPM_EMU10_PULLUDENABLE	pullup/down enable for pad dpm_emu10 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	DPM_EMU10_MUXMODE	Functional multiplexing selection for pad dpm_emu10 0x0: Select dpm_emu10 0x1: Select usba0_ulpiphy_dat4 0x3: Select gpio_21 0x4: Select rfbi_a0 0x5: Select dispc2_de 0x6: Select hw_dbg10 0x7: Select safe_mode	RW	0x7
15	DPM_EMU9_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	DPM_EMU9_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	DPM_EMU9_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad dpm_emu9 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
12	DPM_EMU9_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad dpm_emu9 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0

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Bits	Field Name	Description	Type	Reset
11	DPM_EMU9_ OFFMODEOUTVALUE	OffMode mode output value for pad dpm_emu9 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	DPM_EMU9_ OFFMODEOUTENABLE	OffMode mode output enable value for pad dpm_emu9. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	DPM_EMU9_ OFFMODEENABLE	OffMode mode override control for pad dpm_emu9 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	DPM_EMU9_INPUTENABLE	Input enable value for pad dpm_emu9 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	DPM_EMU9_PULLTYPESELECT	pullup/down selection for pad dpm_emu9 0x0: pulldown selected 0x1: pullup selected	RW	0
3	DPM_EMU9_PULLUDENABLE	pullup/down enable for pad dpm_emu9 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	DPM_EMU9_MUXMODE	Functional multiplexing selection for pad dpm_emu9 0x0: Select dpm_emu9 0x1: Select usba0_ulpiphy_dat3 0x2: Select uart3_cts_rctx 0x3: Select gpio_20 0x4: Select rfbi_we 0x5: Select dispc2_vsync 0x6: Select hw_dbg9 0x7: Select safe_mode	RW	0x7

Table 18-541. Register Call Summary for Register CONTROL_CORE_PAD0_DPM_EMU9_PAD1_DPM_EMU10

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- SYSCTRL_PADCONF_CORE Register Summary: [2]

Table 18-542. CONTROL_CORE_PAD0_DPM_EMU11_PAD1_DPM_EMU12

Address Offset	0x0000 01C4		
Physical Address	0x4A10 01C4	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads dpm_emu11 and dpm_emu12 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DPM_EMU12_WAKEUPEVENT	DPM_EMU12_WAKEUPENABLE	DPM_EMU12_OFFMODEPULLTYPESELECT	DPM_EMU12_OFFMODEPULLUDENABLE	DPM_EMU12_OFFMODEOUTVALUE	DPM_EMU12_OFFMODEOUTENABLE	DPM_EMU12_OFFMODEENABLE	DPM_EMU12_INPUTENABLE	RESERVED			DPM_EMU12_PULLTYPESELECT	DPM_EMU12_PULLUDENABLE	DPM_EMU12_MUXMODE			DPM_EMU11_WAKEUPEVENT	DPM_EMU11_WAKEUPENABLE	DPM_EMU11_OFFMODEPULLTYPESELECT	DPM_EMU11_OFFMODEPULLUDENABLE	DPM_EMU11_OFFMODEOUTVALUE	DPM_EMU11_OFFMODEOUTENABLE	DPM_EMU11_OFFMODEENABLE	DPM_EMU11_INPUTENABLE	RESERVED			DPM_EMU11_PULLTYPESELECT	DPM_EMU11_PULLUDENABLE	DPM_EMU11_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	DPM_EMU12_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	DPM_EMU12_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29	DPM_EMU12_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad dpm_emu12 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
28	DPM_EMU12_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad dpm_emu12 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	DPM_EMU12_ OFFMODEOUTVALUE	OffMode mode output value for pad dpm_emu12 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	DPM_EMU12_ OFFMODEOUTENABLE	OffMode mode output enable value for pad dpm_emu12. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	DPM_EMU12_ OFFMODEENABLE	OffMode mode override control for pad dpm_emu12 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
24	DPM_EMU12_INPUTENABLE	Input enable value for pad dpm_emu12 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	DPM_EMU12_PULLTYPESELECT	pullup/down selection for pad dpm_emu12 0x0: pulldown selected 0x1: pullup selected	RW	0

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Bits	Field Name	Description	Type	Reset
19	DPM_EMU12_PULLUDENABLE	pullup/down enable for pad dpm_emu12 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	DPM_EMU12_MUXMODE	Functional multiplexing selection for pad dpm_emu12 0x0: Select dpm_emu12 0x1: Select usba0_ulpiphy_dat6 0x3: Select gpio_23 0x4: Select rfbi_data7 0x5: Select dispc2_data7 0x6: Select hw_dbg12 0x7: Select safe_mode	RW	0x7
15	DPM_EMU11_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	DPM_EMU11_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	DPM_EMU11_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad dpm_emu11 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
12	DPM_EMU11_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad dpm_emu11 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	DPM_EMU11_ OFFMODEOUTVALUE	OffMode mode output value for pad dpm_emu11 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	DPM_EMU11_ OFFMODEOUTENABLE	OffMode mode output enable value for pad dpm_emu11. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	DPM_EMU11_ OFFMODEENABLE	OffMode mode override control for pad dpm_emu11 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	DPM_EMU11_INPUTENABLE	Input enable value for pad dpm_emu11 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	DPM_EMU11_PULLTYPESELECT	pullup/down selection for pad dpm_emu11 0x0: pulldown selected 0x1: pullup selected	RW	0
3	DPM_EMU11_PULLUDENABLE	pullup/down enable for pad dpm_emu11 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1

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Bits	Field Name	Description	Type	Reset
2:0	DPM_EMU11_MUXMODE	Functional multiplexing selection for pad dpm_emu11 0x0: Select dpm_emu11 0x1: Select usba0_ulpiphy_dat5 0x3: Select gpio_22 0x4: Select rfbi_data8 0x5: Select dispc2_data8 0x6: Select hw_dbg11 0x7: Select safe_mode	RW	0x7

Table 18-543. Register Call Summary for Register CONTROL_CORE_PAD0_DPM_EMU11_PAD1_DPM_EMU12

Control Module Functional Description • Pad Multiplexing Register Fields: [0] [1]
Control Module Register Manual • SYSCTRL_PADCONF_CORE Register Summary: [2]

Table 18-544. CONTROL_CORE_PAD0_DPM_EMU13_PAD1_DPM_EMU14

Address Offset	0x0000 01C8		
Physical Address	0x4A10 01C8	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads dpm_emu13 and dpm_emu14 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DPM_EMU14_WAKEUPEVENT	DPM_EMU14_WAKEUPENABLE	DPM_EMU14_OFFMODEPULLTYPESELECT	DPM_EMU14_OFFMODEPULLUDENABLE	DPM_EMU14_OFFMODEOUTVALUE	DPM_EMU14_OFFMODEOUTENABLE	DPM_EMU14_OFFMODEENABLE	DPM_EMU14_INPUTENABLE	RESERVED			DPM_EMU14_PULLTYPESELECT	DPM_EMU14_PULLUDENABLE	DPM_EMU14_MUXMODE			DPM_EMU13_WAKEUPEVENT	DPM_EMU13_WAKEUPENABLE	DPM_EMU13_OFFMODEPULLTYPESELECT	DPM_EMU13_OFFMODEPULLUDENABLE	DPM_EMU13_OFFMODEOUTVALUE	DPM_EMU13_OFFMODEOUTENABLE	DPM_EMU13_OFFMODEENABLE	DPM_EMU13_INPUTENABLE	RESERVED			DPM_EMU13_PULLTYPESELECT	DPM_EMU13_PULLUDENABLE	DPM_EMU13_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	DPM_EMU14_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	DPM_EMU14_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0

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Bits	Field Name	Description	Type	Reset
29	DPM_EMU14_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad dpm_emu14 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
28	DPM_EMU14_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad dpm_emu14 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	DPM_EMU14_ OFFMODEOUTVALUE	OffMode mode output value for pad dpm_emu14 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	DPM_EMU14_ OFFMODEOUTENABLE	OffMode mode output enable value for pad dpm_emu14. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	DPM_EMU14_ OFFMODEENABLE	OffMode mode override control for pad dpm_emu14 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
24	DPM_EMU14_INPUTENABLE	Input enable value for pad dpm_emu14 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	DPM_EMU14_PULLTYPESELECT	pullup/down selection for pad dpm_emu14 0x0: pulldown selected 0x1: pullup selected	RW	0
19	DPM_EMU14_PULLUDENABLE	pullup/down enable for pad dpm_emu14 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	DPM_EMU14_MUXMODE	Functional multiplexing selection for pad dpm_emu14 0x0: Select dpm_emu14 0x1: Reserved 0x2: Select uart1_rx 0x3: Select gpio_25 0x4: Select rfbi_data5 0x5: Select dispc2_data5 0x6: Select hw_dbg14 0x7: Select safe_mode	RW	0x7
15	DPM_EMU13_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	DPM_EMU13_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	DPM_EMU13_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad dpm_emu13 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0

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Bits	Field Name	Description	Type	Reset
12	DPM_EMU13_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad dpm_emu13 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	DPM_EMU13_ OFFMODEOUTVALUE	OffMode mode output value for pad dpm_emu13 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	DPM_EMU13_ OFFMODEOUTENABLE	OffMode mode output enable value for pad dpm_emu13. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	DPM_EMU13_ OFFMODEENABLE	OffMode mode override control for pad dpm_emu13 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	DPM_EMU13_INPUTENABLE	Input enable value for pad dpm_emu13 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	DPM_EMU13_PULLTYPESELECT	pullup/down selection for pad dpm_emu13 0x0: pulldown selected 0x1: pullup selected	RW	0
3	DPM_EMU13_PULLUDENABLE	pullup/down enable for pad dpm_emu13 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	DPM_EMU13_MUXMODE	Functional multiplexing selection for pad dpm_emu13 0x0: Select dpm_emu13 0x1: Select usba0_ulpiphy_dat7 0x3: Select gpio_24 0x4: Select rfbi_data6 0x5: Select dispc2_data6 0x6: Select hw_dbg13 0x7: Select safe_mode	RW	0x7

Table 18-545. Register Call Summary for Register CONTROL_CORE_PAD0_DPM_EMU13_PAD1_DPM_EMU14

Control Module Functional Description • Pad Multiplexing Register Fields: [0] [1]
Control Module Register Manual • SYSCTRL_PADCONF_CORE Register Summary: [2]

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Table 18-546. CONTROL_CORE_PAD0_DPM_EMU15_PAD1_DPM_EMU16

Address Offset	0x0000 01CC		
Physical Address	0x4A10 01CC	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads dpm_emu15 and dpm_emu16 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DPM_EMU16_WAKEUPEVENT	DPM_EMU16_WAKEUPENABLE	DPM_EMU16_OFFMODEPULLTYPESELECT	DPM_EMU16_OFFMODEPULLUDENABLE	DPM_EMU16_OFFMODEOUTVALUE	DPM_EMU16_OFFMODEOUTENABLE	DPM_EMU16_OFFMODEENABLE	DPM_EMU16_INPUTENABLE	RESERVED			DPM_EMU16_PULLTYPESELECT	DPM_EMU16_PULLUDENABLE	DPM_EMU16_MUXMODE			DPM_EMU15_WAKEUPEVENT	DPM_EMU15_WAKEUPENABLE	DPM_EMU15_OFFMODEPULLTYPESELECT	DPM_EMU15_OFFMODEPULLUDENABLE	DPM_EMU15_OFFMODEOUTVALUE	DPM_EMU15_OFFMODEOUTENABLE	DPM_EMU15_OFFMODEENABLE	DPM_EMU15_INPUTENABLE	RESERVED			DPM_EMU15_PULLTYPESELECT	DPM_EMU15_PULLUDENABLE	DPM_EMU15_MUXMODE	

Bits	Field Name	Description	Type	Reset
31	DPM_EMU16_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	DPM_EMU16_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29	DPM_EMU16_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad dpm_emu16 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
28	DPM_EMU16_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad dpm_emu16 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	DPM_EMU16_ OFFMODEOUTVALUE	OffMode mode output value for pad dpm_emu16 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	DPM_EMU16_ OFFMODEOUTENABLE	OffMode mode output enable value for pad dpm_emu16. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	DPM_EMU16_ OFFMODEENABLE	OffMode mode override control for pad dpm_emu16 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0

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Bits	Field Name	Description	Type	Reset
24	DPM_EMU16_INPUTENABLE	Input enable value for pad dpm_emu16 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	DPM_EMU16_PULLTYPESELECT	pullup/down selection for pad dpm_emu16 0x0: pulldown selected 0x1: pullup selected	RW	0
19	DPM_EMU16_PULLUDENABLE	pullup/down enable for pad dpm_emu16 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	DPM_EMU16_MUXMODE	Functional multiplexing selection for pad dpm_emu16 0x0: Select dpm_emu16 0x1: Select dmtimer8_pwm_evt 0x2: Select dsi1_te0 0x3: Select gpio_27 0x4: Select rfbi_data3 0x5: Select dispc2_data3 0x6: Select hw_dbg16 0x7: Select safe_mode	RW	0x7
15	DPM_EMU15_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	DPM_EMU15_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	DPM_EMU15_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad dpm_emu15 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
12	DPM_EMU15_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad dpm_emu15 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	DPM_EMU15_OFFMODEOUTVALUE	OffMode mode output value for pad dpm_emu15 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	DPM_EMU15_OFFMODEOUTENABLE	OffMode mode output enable value for pad dpm_emu15. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	DPM_EMU15_OFFMODEENABLE	OffMode mode override control for pad dpm_emu15 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	DPM_EMU15_INPUTENABLE	Input enable value for pad dpm_emu15 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
4	DPM_EMU15_PULLTYPESELECT	pullup/down selection for pad dpm_emu15 0x0: pulldown selected 0x1: pullup selected	RW	0
3	DPM_EMU15_PULLUDENABLE	pullup/down enable for pad dpm_emu15 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	DPM_EMU15_MUXMODE	Functional multiplexing selection for pad dpm_emu15 0x0: Select dpm_emu15 0x1: Reserved 0x3: Select gpio_26 0x4: Select rfbi_data4 0x5: Select dispc2_data4 0x6: Select hw_dbg15 0x7: Select safe_mode	RW	0x7

Table 18-547. Register Call Summary for Register CONTROL_CORE_PAD0_DPM_EMU15_PAD1_DPM_EMU16

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- SYSCTRL_PADCONF_CORE Register Summary: [2]

Table 18-548. CONTROL_CORE_PAD0_DPM_EMU17_PAD1_DPM_EMU18

Address Offset	0x0000 01D0		
Physical Address	0x4A10 01D0	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads dpm_emu17 and dpm_emu18 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DPM_EMU18_WAKEUPEVENT	DPM_EMU18_WAKEUPENABLE	DPM_EMU18_OFFMODEPULLTYPESELECT	DPM_EMU18_OFFMODEPULLUDENABLE	DPM_EMU18_OFFMODEOUTVALUE	DPM_EMU18_OFFMODEOUTENABLE	DPM_EMU18_OFFMODEENABLE	DPM_EMU18_INPUTENABLE	RESERVED			DPM_EMU18_PULLTYPESELECT	DPM_EMU18_PULLUDENABLE	DPM_EMU18_MUXMODE			DPM_EMU17_WAKEUPEVENT	DPM_EMU17_WAKEUPENABLE	DPM_EMU17_OFFMODEPULLTYPESELECT	DPM_EMU17_OFFMODEPULLUDENABLE	DPM_EMU17_OFFMODEOUTVALUE	DPM_EMU17_OFFMODEOUTENABLE	DPM_EMU17_OFFMODEENABLE	DPM_EMU17_INPUTENABLE	RESERVED			DPM_EMU17_PULLTYPESELECT	DPM_EMU17_PULLUDENABLE	DPM_EMU17_MUXMODE	

Bits	Field Name	Description	Type	Reset
31	DPM_EMU18_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0

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Bits	Field Name	Description	Type	Reset
30	DPM_EMU18_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29	DPM_EMU18_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad dpm_emu18 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
28	DPM_EMU18_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad dpm_emu18 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	DPM_EMU18_ OFFMODEOUTVALUE	OffMode mode output value for pad dpm_emu18 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	DPM_EMU18_ OFFMODEOUTENABLE	OffMode mode output enable value for pad dpm_emu18. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	DPM_EMU18_ OFFMODEENABLE	OffMode mode override control for pad dpm_emu18 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
24	DPM_EMU18_INPUTENABLE	Input enable value for pad dpm_emu18 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	DPM_EMU18_PULLTYPESELECT	pullup/down selection for pad dpm_emu18 0x0: pulldown selected 0x1: pullup selected	RW	0
19	DPM_EMU18_PULLUDENABLE	pullup/down enable for pad dpm_emu18 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	DPM_EMU18_MUXMODE	Functional multiplexing selection for pad dpm_emu18 0x0: Select dpm_emu18 0x1: Select dmtimer10_pwm_evt 0x2: Select dsi2_te0 0x3: Select gpio_190 0x4: Select rfbi_data1 0x5: Select dispc2_data1 0x6: Select hw_dbg18 0x7: Select safe_mode	RW	0x7
15	DPM_EMU17_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	DPM_EMU17_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0

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Bits	Field Name	Description	Type	Reset
13	DPM_EMU17_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad dpm_emu17 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
12	DPM_EMU17_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad dpm_emu17 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	DPM_EMU17_ OFFMODEOUTVALUE	OffMode mode output value for pad dpm_emu17 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	DPM_EMU17_ OFFMODEOUTENABLE	OffMode mode output enable value for pad dpm_emu17. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	DPM_EMU17_ OFFMODEENABLE	OffMode mode override control for pad dpm_emu17 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	DPM_EMU17_INPUTENABLE	Input enable value for pad dpm_emu17 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	DPM_EMU17_PULLTYPESELECT	pullup/down selection for pad dpm_emu17 0x0: pulldown selected 0x1: pullup selected	RW	0
3	DPM_EMU17_PULLUDENABLE	pullup/down enable for pad dpm_emu17 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	DPM_EMU17_MUXMODE	Functional multiplexing selection for pad dpm_emu17 0x0: Select dpm_emu17 0x1: Select dmtimer9_pwm_evt 0x2: Select dsi1_te1 0x3: Select gpio_28 0x4: Select rfbi_data2 0x5: Select dispc2_data2 0x6: Select hw_dbg17 0x7: Select safe_mode	RW	0x7

Table 18-549. Register Call Summary for Register CONTROL_CORE_PAD0_DPM_EMU17_PAD1_DPM_EMU18

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- SYSCTRL_PADCONF_CORE Register Summary: [2]

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Table 18-550. CONTROL_CORE_PAD0_DPM_EMU19_PAD1_CSI22_DX2

Address Offset	0x0000 01D4		
Physical Address	0x4A10 01D4	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads dpm_emu19 and csi22_dx2 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CSI22_DX2_WAKEUPEVENT	CSI22_DX2_WAKEUPENABLE	RESERVED					CSI22_DX2_INPUTENABLE	RESERVED			CSI22_DX2_PULLTYPESELECT	CSI22_DX2_PULLUDENABLE	CSI22_DX2_MUXMODE			DPM_EMU19_WAKEUPEVENT	DPM_EMU19_WAKEUPENABLE	DPM_EMU19_OFFMODEPULLTYPESELECT	DPM_EMU19_OFFMODEPULLUDENABLE	DPM_EMU19_OFFMODEOUTVALUE	DPM_EMU19_OFFMODEOUTENABLE	DPM_EMU19_OFFMODEENABLE	DPM_EMU19_INPUTENABLE	RESERVED			DPM_EMU19_PULLTYPESELECT	DPM_EMU19_PULLUDENABLE	DPM_EMU19_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	CSI22_DX2_WAKEUPEVENT	Pad_x wake-up event status latched in the I/O Read 0x1: A wake-up event occurred. Read 0x0: No wake-up event occurred.	R	0
30	CSI22_DX2_WAKEUPENABLE	Input pad wake-up enable (and off mode input enable value) 0x0: Wake-up detection on low level 0x1: Wake-up detection on high level	RW	0
29:25	RESERVED		R	0x00
24	CSI22_DX2_INPUTENABLE	Input enable value for pad csi22_dx2 0x0: Input buffer of IO cell is disabled. 0x1: Input buffer of IO cell is enabled.	RW	1
23:21	RESERVED		R	0x0
20	CSI22_DX2_PULLTYPESELECT	Pullup/down selection for pad csi22_dx2 0x0: Pulldown selected 0x1: Pullup selected	RW	0
19	CSI22_DX2_PULLUDENABLE	Pullup/down enable for pad csi22_dx2 0x0: Pullup/downdisabled 0x1: Pullup/down enabled	RW	1
18:16	CSI22_DX2_MUXMODE	Functional multiplexing selection for pad csi22_dx2 0x0: Select csi22_dx2 0x2: Select cam2_fid 0x7: Select safe_mode	R	0x7
15	DPM_EMU19_ WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred. Read 0x1: A wake-up event occurred.	R	0

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Bits	Field Name	Description	Type	Reset
14	DPM_EMU19_ WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: Wake-up detection is disabled. 0x1: Wake-up detection is enabled.	RW	0
13	DPM_EMU19_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad dpm_emu19 0x0: Off mode pulldown selected 0x1: Off mode pullup selected	RW	0
12	DPM_EMU19_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad dpm_emu19 0x0: Off mode pullup/down disabled 0x1: Off mode pullup/down enabled	RW	0
11	DPM_EMU19_ OFFMODEOUTVALUE	OffMode mode output value for pad dpm_emu19 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	DPM_EMU19_ OFFMODEOUTENABLE	OffMode mode output enable value for pad dpm_emu19. This is an active low signal. 0x0: Output enable 0x1: Output disable	RW	0
9	DPM_EMU19_OFFMODEENABLE	OffMode mode override control for pad dpm_emu19 0x0: I/O state keeps its previous state when off mode is active. 0x1: I/O state is forced to off mode value when off mode is active.	RW	0
8	DPM_EMU19_INPUTENABLE	Input enable value for pad dpm_emu19 0x0: Input buffer of I/O cell is disabled. 0x1: Input buffer of I/O cell is enabled.	RW	1
7:5	RESERVED		R	0x0
4	DPM_EMU19_PULLTYPESELECT	Pullup/down selection for pad dpm_emu19 0x0: Pulldown selected 0x1: Pullup selected	RW	0
3	DPM_EMU19_PULLUDENABLE	Pullup/down enable for pad dpm_emu19 0x0: Pullup/down disabled 0x1: Pullup/down enabled	RW	1
2:0	DPM_EMU19_MUXMODE	Functional multiplexing selection for pad dpm_emu19 0x0: Select dpm_emu19 0x1: Select dmtimer11_pwm_evt 0x2: Select dsi2_te1 0x3: Select gpio_191 0x4: Select rfbi_data0 0x5: Select dispc2_data0 0x6: Select hw_dbg19 0x7: Select safe_mode	RW	0x7

Table 18-551. Register Call Summary for Register CONTROL_CORE_PAD0_DPM_EMU19_PAD1_CSI22_DX2

Control Module Functional Description
- Observability Signals Multiplexing at Device Control Module Level: [0]

Control Module Register Manual
- SYSCTRL_PADCONF_CORE Register Summary: [1]

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Table 18-552. CONTROL_PADCONF_WAKEUPEVENT_0

Address Offset	0x0000 01D8		
Physical Address	0x4A10 01D8	**Instance**	SYSCTRL_PADCONF_CORE
Description	Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPMC_CLK_DUPLICATEWAKEUPEVENT	GPMC_NWP_DUPLICATEWAKEUPEVENT	GPMC_NCS3_DUPLICATEWAKEUPEVENT	GPMC_NCS2_DUPLICATEWAKEUPEVENT	GPMC_NCS1_DUPLICATEWAKEUPEVENT	GPMC_NCS0_DUPLICATEWAKEUPEVENT	GPMC_A25_DUPLICATEWAKEUPEVENT	GPMC_A24_DUPLICATEWAKEUPEVENT	GPMC_A23_DUPLICATEWAKEUPEVENT	GPMC_A22_DUPLICATEWAKEUPEVENT	GPMC_A21_DUPLICATEWAKEUPEVENT	GPMC_A20_DUPLICATEWAKEUPEVENT	GPMC_A19_DUPLICATEWAKEUPEVENT	GPMC_A18_DUPLICATEWAKEUPEVENT	GPMC_A17_DUPLICATEWAKEUPEVENT	GPMC_A16_DUPLICATEWAKEUPEVENT	GPMC_AD15_DUPLICATEWAKEUPEVENT	GPMC_AD14_DUPLICATEWAKEUPEVENT	GPMC_AD13_DUPLICATEWAKEUPEVENT	GPMC_AD12_DUPLICATEWAKEUPEVENT	GPMC_AD11_DUPLICATEWAKEUPEVENT	GPMC_AD10_DUPLICATEWAKEUPEVENT	GPMC_AD9_DUPLICATEWAKEUPEVENT	GPMC_AD8_DUPLICATEWAKEUPEVENT	GPMC_AD7_DUPLICATEWAKEUPEVENT	GPMC_AD6_DUPLICATEWAKEUPEVENT	GPMC_AD5_DUPLICATEWAKEUPEVENT	GPMC_AD4_DUPLICATEWAKEUPEVENT	GPMC_AD3_DUPLICATEWAKEUPEVENT	GPMC_AD2_DUPLICATEWAKEUPEVENT	GPMC_AD1_DUPLICATEWAKEUPEVENT	GPMC_AD0_DUPLICATEWAKEUPEVENT

Bits	Field Name	Description	Type	Reset
31	GPMC_CLK_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad gpmc_clk Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	GPMC_NWP_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad gpmc_nwp Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
29	GPMC_NCS3_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad gpmc_ncs3 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
28	GPMC_NCS2_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad gpmc_ncs2 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
27	GPMC_NCS1_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad gpmc_ncs1 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
26	GPMC_NCS0_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad gpmc_ncs0 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
25	GPMC_A25_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad gpmc_a25 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0

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Bits	Field Name	Description	Type	Reset
24	GPMC_A24_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad gpmc_a24 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
23	GPMC_A23_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad gpmc_a23 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
22	GPMC_A22_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad gpmc_a22 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
21	GPMC_A21_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad gpmc_a21 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
20	GPMC_A20_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad gpmc_a20 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
19	GPMC_A19_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad gpmc_a19 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
18	GPMC_A18_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad gpmc_a18 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
17	GPMC_A17_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad gpmc_a17 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
16	GPMC_A16_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad gpmc_a16 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
15	GPMC_AD15_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad gpmc_ad15 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	GPMC_AD14_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad gpmc_ad14 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
13	GPMC_AD13_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad gpmc_ad13 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
12	GPMC_AD12_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad gpmc_ad12 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0

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Bits	Field Name	Description	Type	Reset
11	GPMC_AD11_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad gpmc_ad11 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
10	GPMC_AD10_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad gpmc_ad10 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
9	GPMC_AD9_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad gpmc_ad9 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
8	GPMC_AD8_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad gpmc_ad8 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
7	GPMC_AD7_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad gpmc_ad7 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
6	GPMC_AD6_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad gpmc_ad6 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
5	GPMC_AD5_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad gpmc_ad5 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
4	GPMC_AD4_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad gpmc_ad4 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
3	GPMC_AD3_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad gpmc_ad3 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
2	GPMC_AD2_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad gpmc_ad2 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
1	GPMC_AD1_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad gpmc_ad1 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
0	GPMC_AD0_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad gpmc_ad0 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0

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Table 18-553. Register Call Summary for Register CONTROL_PADCONF_WAKEUPEVENT_0

Control Module Functional Description
- Off Mode Pad Control Overview: [0]

Control Module Register Manual
- SYSCTRL_PADCONF_CORE Register Summary: [1]

Table 18-554. CONTROL_PADCONF_WAKEUPEVENT_1

Address Offset	0x0000 01DC		
Physical Address	0x4A10 01DC	**Instance**	SYSCTRL_PADCONF_CORE
Description	Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAM_STROBE_DUPLICATEWAKEUPEVENT	CAM_SHUTTER_DUPLICATEWAKEUPEVENT	CSI22_DY1_DUPLICATEWAKEUPEVENT	CSI22_DX1_DUPLICATEWAKEUPEVENT	CSI22_DY0_DUPLICATEWAKEUPEVENT	CSI22_DX0_DUPLICATEWAKEUPEVENT	CSI21_DY4_DUPLICATEWAKEUPEVENT	CSI21_DX4_DUPLICATEWAKEUPEVENT	CSI21_DY3_DUPLICATEWAKEUPEVENT	CSI21_DX3_DUPLICATEWAKEUPEVENT	CSI21_DY2_DUPLICATEWAKEUPEVENT	CSI21_DX2_DUPLICATEWAKEUPEVENT	CSI21_DY1_DUPLICATEWAKEUPEVENT	CSI21_DX1_DUPLICATEWAKEUPEVENT	CSI21_DY0_DUPLICATEWAKEUPEVENT	CSI21_DX0_DUPLICATEWAKEUPEVENT	GPIO66_DUPLICATEWAKEUPEVENT	GPIO65_DUPLICATEWAKEUPEVENT	GPIO64_DUPLICATEWAKEUPEVENT	GPIO63_DUPLICATEWAKEUPEVENT	GPMC_NCS7_DUPLICATEWAKEUPEVENT	GPMC_NCS6_DUPLICATEWAKEUPEVENT	GPMC_NCS5_DUPLICATEWAKEUPEVENT	GPMC_NCS4_DUPLICATEWAKEUPEVENT	GPMC_WAIT2_DUPLICATEWAKEUPEVENT	GPMC_WAIT1_DUPLICATEWAKEUPEVENT	GPMC_WAIT0_DUPLICATEWAKEUPEVENT	GPMC_NBE1_DUPLICATEWAKEUPEVENT	GPMC_NBE0_CLE_DUPLICATEWAKEUPEVENT	GPMC_NWE_DUPLICATEWAKEUPEVENT	GPMC_NOE_DUPLICATEWAKEUPEVENT	GPMC_NADV_ALE_DUPLICATEWAKEUPEVENT

Bits	Field Name	Description	Type	Reset
31	CAM_STROBE_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad cam_strobe Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	CAM_SHUTTER_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad cam_shutter Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
29	CSI22_DY1_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad csi22_dy1 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
28	CSI22_DX1_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad csi22_dx1 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
27	CSI22_DY0_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad csi22_dy0 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0

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Bits	Field Name	Description	Type	Reset
26	CSI22_DX0_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad csi22_dx0 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
25	CSI21_DY4_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad csi21_dy4 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
24	CSI21_DX4_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad csi21_dx4 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
23	CSI21_DY3_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad csi21_dy3 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
22	CSI21_DX3_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad csi21_dx3 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
21	CSI21_DY2_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad csi21_dy2 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
20	CSI21_DX2_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad csi21_dx2 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
19	CSI21_DY1_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad csi21_dy1 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
18	CSI21_DX1_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad csi21_dx1 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
17	CSI21_DY0_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad csi21_dy0 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
16	CSI21_DX0_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad csi21_dx0 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
15	GPIO66_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad gpio66 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	GPIO65_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad gpio65 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0

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Bits	Field Name	Description	Type	Reset
13	GPIO64_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad gpio64 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
12	GPIO63_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad gpio63 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
11	GPMC_NCS7_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad gpmc_ncs7 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
10	GPMC_NCS6_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad gpmc_ncs6 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
9	GPMC_NCS5_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad gpmc_ncs5 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
8	GPMC_NCS4_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad gpmc_ncs4 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
7	GPMC_WAIT2_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad gpmc_wait2 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
6	GPMC_WAIT1_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad gpmc_wait1 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
5	GPMC_WAIT0_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad gpmc_wait0 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
4	GPMC_NBE1_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad gpmc_nbe1 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
3	GPMC_NBE0_CLE_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad gpmc_nbe0_cle Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
2	GPMC_NWE_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad gpmc_nwe Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
1	GPMC_NOE_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad gpmc_noe Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0

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Bits	Field Name	Description	Type	Reset
0	GPMC_NADV_ALE_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad gpmc_nadv_ale Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0

Table 18-555. Register Call Summary for Register CONTROL_PADCONF_WAKEUPEVENT_1

Control Module Register Manual

- SYSCTRL_PADCONF_CORE Register Summary: [0]

Table 18-556. CONTROL_PADCONF_WAKEUPEVENT_2

Address Offset	0x0000 01E0		
Physical Address	0x4A10 01E0	**Instance**	SYSCTRL_PADCONF_CORE
Description	Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ABE_MCBSP1_CLKX_DUPLICATEWAKEUPEVENT	ABE_MCBSP2_FSX_DUPLICATEWAKEUPEVENT	ABE_MCBSP2_DX_DUPLICATEWAKEUPEVENT	ABE_MCBSP2_DR_DUPLICATEWAKEUPEVENT	ABE_MCBSP2_CLKX_DUPLICATEWAKEUPEVENT	SDMMC1_DAT7_DUPLICATEWAKEUPEVENT	SDMMC1_DAT6_DUPLICATEWAKEUPEVENT	SDMMC1_DAT5_DUPLICATEWAKEUPEVENT	SDMMC1_DAT4_DUPLICATEWAKEUPEVENT	SDMMC1_DAT3_DUPLICATEWAKEUPEVENT	SDMMC1_DAT2_DUPLICATEWAKEUPEVENT	SDMMC1_DAT1_DUPLICATEWAKEUPEVENT	SDMMC1_DAT0_DUPLICATEWAKEUPEVENT	SDMMC1_CMD_DUPLICATEWAKEUPEVENT	SDMMC1_CLK_DUPLICATEWAKEUPEVENT	USBC1_ICUSB_DM_DUPLICATEWAKEUPEVENT	USBC1_ICUSB_DP_DUPLICATEWAKEUPEVENT	USBB1_HSIC_STROBE_DUPLICATEWAKEUPEVENT	USBB1_HSIC_DATA_DUPLICATEWAKEUPEVENT	USBB1_ULPITLL_DAT7_DUPLICATEWAKEUPEVENT	USBB1_ULPITLL_DAT6_DUPLICATEWAKEUPEVENT	USBB1_ULPITLL_DAT5_DUPLICATEWAKEUPEVENT	USBB1_ULPITLL_DAT4_DUPLICATEWAKEUPEVENT	USBB1_ULPITLL_DAT3_DUPLICATEWAKEUPEVENT	USBB1_ULPITLL_DAT2_DUPLICATEWAKEUPEVENT	USBB1_ULPITLL_DAT1_DUPLICATEWAKEUPEVENT	USBB1_ULPITLL_DAT0_DUPLICATEWAKEUPEVENT	USBB1_ULPITLL_NXT_DUPLICATEWAKEUPEVENT	USBB1_ULPITLL_DIR_DUPLICATEWAKEUPEVENT	USBB1_ULPITLL_STP_DUPLICATEWAKEUPEVENT	USBB1_ULPITLL_CLK_DUPLICATEWAKEUPEVENT	CAM_GLOBALRESET_DUPLICATEWAKEUPEVENT

Bits	Field Name	Description	Type	Reset
31	ABE_MCBSP1_CLKX_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad abe_mcbsp1_clkx Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	ABE_MCBSP2_FSX_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad abe_mcbsp2_fsx Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
29	ABE_MCBSP2_DX_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad abe_mcbsp2_dx Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
28	ABE_MCBSP2_DR_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad abe_mcbsp2_dr Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0

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Bits	Field Name	Description	Type	Reset
27	ABE_MCBSP2_CLKX_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad abe_mcbsp2_clkx Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
26	SDMMC1_DAT7_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad sdmmc1_dat7 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
25	SDMMC1_DAT6_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad sdmmc1_dat6 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
24	SDMMC1_DAT5_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad sdmmc1_dat5 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
23	SDMMC1_DAT4_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad sdmmc1_dat4 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
22	SDMMC1_DAT3_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad sdmmc1_dat3 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
21	SDMMC1_DAT2_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad sdmmc1_dat2 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
20	SDMMC1_DAT1_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad sdmmc1_dat1 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
19	SDMMC1_DAT0_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad sdmmc1_dat0 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
18	SDMMC1_CMD_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad sdmmc1_cmd Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
17	SDMMC1_CLK_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad sdmmc1_clk Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
16	USBC1_ICUSB_DM_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad usbc1_icusb_dm Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
15	USBC1_ICUSB_DP_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad usbc1_icusb_dp Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0

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Bits	Field Name	Description	Type	Reset
14	USBB1_HSIC_STROBE_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad usbb1_hsic_strobe Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
13	USBB1_HSIC_DATA_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad usbb1_hsic_data Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
12	USBB1_ULPITLL_DAT7_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad usbb1_ulpitll_dat7 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
11	USBB1_ULPITLL_DAT6_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad usbb1_ulpitll_dat6 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
10	USBB1_ULPITLL_DAT5_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad usbb1_ulpitll_dat5 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
9	USBB1_ULPITLL_DAT4_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad usbb1_ulpitll_dat4 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
8	USBB1_ULPITLL_DAT3_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad usbb1_ulpitll_dat3 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
7	USBB1_ULPITLL_DAT2_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad usbb1_ulpitll_dat2 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
6	USBB1_ULPITLL_DAT1_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad usbb1_ulpitll_dat1 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
5	USBB1_ULPITLL_DAT0_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad usbb1_ulpitll_dat0 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
4	USBB1_ULPITLL_NXT_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad usbb1_ulpitll_nxt Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
3	USBB1_ULPITLL_DIR_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad usbb1_ulpitll_dir Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
2	USBB1_ULPITLL_STP_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad usbb1_ulpitll_stp Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0

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Bits	Field Name	Description	Type	Reset
1	USBB1_ULPITLL_CLK_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad usbb1_ulpitll_clk Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
0	CAM_GLOBALRESET_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad cam_globalreset Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0

Table 18-557. Register Call Summary for Register CONTROL_PADCONF_WAKEUPEVENT_2

Control Module Register Manual

- SYSCTRL_PADCONF_CORE Register Summary: [0]

Table 18-558. CONTROL_PADCONF_WAKEUPEVENT_3

Address Offset	0x0000 01E4		
Physical Address	0x4A10 01E4	**Instance**	SYSCTRL_PADCONF_CORE
Description	Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MCSPI1_CS3_DUPLICATEWAKEUPEVENT	MCSPI1_CS2_DUPLICATEWAKEUPEVENT	MCSPI1_CS1_DUPLICATEWAKEUPEVENT	MCSPI1_CS0_DUPLICATEWAKEUPEVENT	MCSPI1_SIMO_DUPLICATEWAKEUPEVENT	MCSPI1_SOMI_DUPLICATEWAKEUPEVENT	MCSPI1_CLK_DUPLICATEWAKEUPEVENT	I2C4_SDA_DUPLICATEWAKEUPEVENT	I2C4_SCL_DUPLICATEWAKEUPEVENT	I2C3_SDA_DUPLICATEWAKEUPEVENT	I2C3_SCL_DUPLICATEWAKEUPEVENT	I2C2_SDA_DUPLICATEWAKEUPEVENT	I2C2_SCL_DUPLICATEWAKEUPEVENT	I2C1_SDA_DUPLICATEWAKEUPEVENT	I2C1_SCL_DUPLICATEWAKEUPEVENT	HDQ_SIO_DUPLICATEWAKEUPEVENT	UART2_TX_DUPLICATEWAKEUPEVENT	UART2_RX_DUPLICATEWAKEUPEVENT	UART2_RTS_DUPLICATEWAKEUPEVENT	UART2_CTS_DUPLICATEWAKEUPEVENT	ABE_DMIC_DIN3_DUPLICATEWAKEUPEVENT	ABE_DMIC_DIN2_DUPLICATEWAKEUPEVENT	ABE_DMIC_DIN1_DUPLICATEWAKEUPEVENT	ABE_DMIC_CLK1_DUPLICATEWAKEUPEVENT	ABE_CLKS_DUPLICATEWAKEUPEVENT	ABE_PDM_LB_CLK_DUPLICATEWAKEUPEVENT	ABE_PDM_FRAME_DUPLICATEWAKEUPEVENT	ABE_PDM_DL_DATA_DUPLICATEWAKEUPEVENT	ABE_PDM_UL_DATA_DUPLICATEWAKEUPEVENT	ABE_MCBSP1_FSX_DUPLICATEWAKEUPEVENT	ABE_MCBSP1_DX_DUPLICATEWAKEUPEVENT	ABE_MCBSP1_DR_DUPLICATEWAKEUPEVENT

Bits	Field Name	Description	Type	Reset
31	MCSPI1_CS3_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad mcspi1_cs3 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	MCSPI1_CS2_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad mcspi1_cs2 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
29	MCSPI1_CS1_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad mcspi1_cs1 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0

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Bits	Field Name	Description	Type	Reset
28	MCSPI1_CS0_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad mcspi1_cs0 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
27	MCSPI1_SIMO_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad mcspi1_simo Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
26	MCSPI1_SOMI_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad mcspi1_somi Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
25	MCSPI1_CLK_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad mcspi1_clk Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
24	I2C4_SDA_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad i2c4_sda Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
23	I2C4_SCL_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad i2c4_scl Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
22	I2C3_SDA_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad i2c3_sda Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
21	I2C3_SCL_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad i2c3_scl Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
20	I2C2_SDA_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad i2c2_sda Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
19	I2C2_SCL_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad i2c2_scl Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
18	I2C1_SDA_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad i2c1_sda Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
17	I2C1_SCL_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad i2c1_scl Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
16	HDQ_SIO_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad hdq_sio Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
15	UART2_TX_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad uart2_tx Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	UART2_RX_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad uart2_rx Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0

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Bits	Field Name	Description	Type	Reset
13	UART2_RTS_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad uart2_rts Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
12	UART2_CTS_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad uart2_cts Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
11	ABE_DMIC_DIN3_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad abe_dmic_din3 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
10	ABE_DMIC_DIN2_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad abe_dmic_din2 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
9	ABE_DMIC_DIN1_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad abe_dmic_din1 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
8	ABE_DMIC_CLK1_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad abe_dmic_clk1 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
7	ABE_CLKS_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad abe_clks Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
6	ABE_PDM_LB_CLK_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad abe_pdm_lb_clk Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
5	ABE_PDM_FRAME_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad abe_pdm_frame Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
4	ABE_PDM_DL_DATA_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad abe_pdm_dl_data Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
3	ABE_PDM_UL_DATA_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad abe_pdm_ul_data Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
2	ABE_MCBSP1_FSX_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad abe_mcbsp1_fsx Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
1	ABE_MCBSP1_DX_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad abe_mcbsp1_dx Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0

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Bits	Field Name	Description	Type	Reset
0	ABE_MCBSP1_DR_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad abe_mcbsp1_dr Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0

Table 18-559. Register Call Summary for Register CONTROL_PADCONF_WAKEUPEVENT_3

Control Module Register Manual

- SYSCTRL_PADCONF_CORE Register Summary: [0]

Table 18-560. CONTROL_PADCONF_WAKEUPEVENT_4

Address Offset	0x0000 01E8		
Physical Address	0x4A10 01E8	**Instance**	SYSCTRL_PADCONF_CORE
Description	Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
KPD_COL4_DUPLICATEWAKEUPEVENT	KPD_COL3_DUPLICATEWAKEUPEVENT	USBB2_HSIC_STROBE_DUPLICATEWAKEUPEVENT	USBB2_HSIC_DATA_DUPLICATEWAKEUPEVENT	USBB2_ULPITLL_DAT7_DUPLICATEWAKEUPEVENT	USBB2_ULPITLL_DAT6_DUPLICATEWAKEUPEVENT	USBB2_ULPITLL_DAT5_DUPLICATEWAKEUPEVENT	USBB2_ULPITLL_DAT4_DUPLICATEWAKEUPEVENT	USBB2_ULPITLL_DAT3_DUPLICATEWAKEUPEVENT	USBB2_ULPITLL_DAT2_DUPLICATEWAKEUPEVENT	USBB2_ULPITLL_DAT1_DUPLICATEWAKEUPEVENT	USBB2_ULPITLL_DAT0_DUPLICATEWAKEUPEVENT	USBB2_ULPITLL_NXT_DUPLICATEWAKEUPEVENT	USBB2_ULPITLL_DIR_DUPLICATEWAKEUPEVENT	USBB2_ULPITLL_STP_DUPLICATEWAKEUPEVENT	USBB2_ULPITLL_CLK_DUPLICATEWAKEUPEVENT	UART4_TX_DUPLICATEWAKEUPEVENT	UART4_RX_DUPLICATEWAKEUPEVENT	MCSPI4_CS0_DUPLICATEWAKEUPEVENT	MCSPI4_SOMI_DUPLICATEWAKEUPEVENT	MCSPI4_SIMO_DUPLICATEWAKEUPEVENT	MCSPI4_CLK_DUPLICATEWAKEUPEVENT	SDMMC5_DAT3_DUPLICATEWAKEUPEVENT	SDMMC5_DAT2_DUPLICATEWAKEUPEVENT	SDMMC5_DAT1_DUPLICATEWAKEUPEVENT	SDMMC5_DAT0_DUPLICATEWAKEUPEVENT	SDMMC5_CMD_DUPLICATEWAKEUPEVENT	SDMMC5_CLK_DUPLICATEWAKEUPEVENT	UART3_TX_IRTX_DUPLICATEWAKEUPEVENT	UART3_RX_IRRX_DUPLICATEWAKEUPEVENT	UART3_RTS_SD_DUPLICATEWAKEUPEVENT	UART3_CTS_RCTX_DUPLICATEWAKEUPEVENT

Bits	Field Name	Description	Type	Reset
31	KPD_COL4_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad kpd_col4 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	KPD_COL3_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad kpd_col3 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
29	USBB2_HSIC_STROBE_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad usbb2_hsic_strobe Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
28	USBB2_HSIC_DATA_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad usbb2_hsic_data Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0

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Bits	Field Name	Description	Type	Reset
27	USBB2_ULPITLL_DAT7_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad usbb2_ulpitll_dat7 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
26	USBB2_ULPITLL_DAT6_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad usbb2_ulpitll_dat6 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
25	USBB2_ULPITLL_DAT5_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad usbb2_ulpitll_dat5 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
24	USBB2_ULPITLL_DAT4_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad usbb2_ulpitll_dat4 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
23	USBB2_ULPITLL_DAT3_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad usbb2_ulpitll_dat3 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
22	USBB2_ULPITLL_DAT2_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad usbb2_ulpitll_dat2 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
21	USBB2_ULPITLL_DAT1_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad usbb2_ulpitll_dat1 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
20	USBB2_ULPITLL_DAT0_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad usbb2_ulpitll_dat0 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
19	USBB2_ULPITLL_NXT_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad usbb2_ulpitll_nxt Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
18	USBB2_ULPITLL_DIR_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad usbb2_ulpitll_dir Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
17	USBB2_ULPITLL_STP_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad usbb2_ulpitll_stp Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
16	USBB2_ULPITLL_CLK_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad usbb2_ulpitll_clk Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
15	UART4_TX_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad uart4_tx Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0

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Bits	Field Name	Description	Type	Reset
14	UART4_RX_ DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad uart4_rx Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
13	MCSPI4_CS0_ DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad mcspi4_cs0 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
12	MCSPI4_SOMI_ DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad mcspi4_somi Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
11	MCSPI4_SIMO_ DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad mcspi4_simo Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
10	MCSPI4_CLK_ DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad mcspi4_clk Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
9	SDMMC5_DAT3_ DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad sdmmc5_dat3 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
8	SDMMC5_DAT2_ DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad sdmmc5_dat2 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
7	SDMMC5_DAT1_ DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad sdmmc5_dat1 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
6	SDMMC5_DAT0_ DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad sdmmc5_dat0 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
5	SDMMC5_CMD_ DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad sdmmc5_cmd Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
4	SDMMC5_CLK_ DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad sdmmc5_clk Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
3	UART3_TX_IRTX_ DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad uart3_tx_irtx Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
2	UART3_RX_IRRX_ DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad uart3_rx_irrx Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0

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Bits	Field Name	Description	Type	Reset
1	UART3_RTS_SD_ DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad uart3_rts_sd Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
0	UART3_CTS_RCTX_ DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad uart3_cts_rctx Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0

Table 18-561. Register Call Summary for Register CONTROL_PADCONF_WAKEUPEVENT_4

Control Module Register Manual

- SYSCTRL_PADCONF_CORE Register Summary: [0]

Table 18-562. CONTROL_PADCONF_WAKEUPEVENT_5

Address Offset	0x0000 01EC		
Physical Address	0x4A10 01EC	**Instance**	SYSCTRL_PADCONF_CORE
Description	Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DPM_EMU10_DUPLICATEWAKEUPEVENT	DPM_EMU9_DUPLICATEWAKEUPEVENT	DPM_EMU8_DUPLICATEWAKEUPEVENT	DPM_EMU7_DUPLICATEWAKEUPEVENT	DPM_EMU6_DUPLICATEWAKEUPEVENT	DPM_EMU5_DUPLICATEWAKEUPEVENT	DPM_EMU4_DUPLICATEWAKEUPEVENT	DPM_EMU3_DUPLICATEWAKEUPEVENT	DPM_EMU2_DUPLICATEWAKEUPEVENT	DPM_EMU1_DUPLICATEWAKEUPEVENT	DPM_EMU0_DUPLICATEWAKEUPEVENT	SYS_BOOT5_DUPLICATEWAKEUPEVENT	SYS_BOOT4_DUPLICATEWAKEUPEVENT	SYS_BOOT3_DUPLICATEWAKEUPEVENT	SYS_BOOT2_DUPLICATEWAKEUPEVENT	SYS_BOOT1_DUPLICATEWAKEUPEVENT	SYS_BOOT0_DUPLICATEWAKEUPEVENT	SYS_NIRQ2_DUPLICATEWAKEUPEVENT	SYS_NIRQ1_DUPLICATEWAKEUPEVENT	FREF_CLK2_OUT_DUPLICATEWAKEUPEVENT	FREF_CLK1_OUT_DUPLICATEWAKEUPEVENT	USBA0_OTG_DP_DUPLICATEWAKEUPEVENT	KPD_ROW2_DUPLICATEWAKEUPEVENT	KPD_ROW1_DUPLICATEWAKEUPEVENT	KPD_ROW0_DUPLICATEWAKEUPEVENT	KPD_ROW5_DUPLICATEWAKEUPEVENT	KPD_ROW4_DUPLICATEWAKEUPEVENT	KPD_ROW3_DUPLICATEWAKEUPEVENT	KPD_COL2_DUPLICATEWAKEUPEVENT	KPD_COL1_DUPLICATEWAKEUPEVENT	KPD_COL0_DUPLICATEWAKEUPEVENT	KPD_COL5_DUPLICATEWAKEUPEVENT

Bits	Field Name	Description	Type	Reset
31	DPM_EMU10_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad dpm_emu10 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	DPM_EMU9_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad dpm_emu9 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
29	DPM_EMU8_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad dpm_emu8 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0

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Bits	Field Name	Description	Type	Reset
28	DPM_EMU7_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad dpm_emu7 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
27	DPM_EMU6_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad dpm_emu6 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
26	DPM_EMU5_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad dpm_emu5 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
25	DPM_EMU4_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad dpm_emu4 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
24	DPM_EMU3_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad dpm_emu3 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
23	DPM_EMU2_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad dpm_emu2 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
22	DPM_EMU1_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad dpm_emu1 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
21	DPM_EMU0_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad dpm_emu0 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
20	SYS_BOOT5_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad sys_boot5 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
19	SYS_BOOT4_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad sys_boot4 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
18	SYS_BOOT3_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad sys_boot3 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
17	SYS_BOOT2_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad sys_boot2 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
16	SYS_BOOT1_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad sys_boot1 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0

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Bits	Field Name	Description	Type	Reset
15	SYS_BOOT0_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad sys_boot0 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	SYS_NIRQ2_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad sys_nirq2 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
13	SYS_NIRQ1_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad sys_nirq1 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
12	FREF_CLK2_OUT_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad fref_clk2_out Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
11	FREF_CLK1_OUT_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad fref_clk1_out Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
10	USBA0_OTG_DP_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad usba0_otg_dp Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
9	KPD_ROW2_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad kpd_row2 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
8	KPD_ROW1_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad kpd_row1 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
7	KPD_ROW0_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad kpd_row0 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
6	KPD_ROW5_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad kpd_row5 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
5	KPD_ROW4_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad kpd_row4 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
4	KPD_ROW3_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad kpd_row3 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
3	KPD_COL2_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad kpd_col2 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
2	KPD_COL1_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad kpd_col1 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0

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Bits	Field Name	Description	Type	Reset
1	KPD_COL0_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad kpd_col0 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
0	KPD_COL5_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad kpd_col5 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0

Table 18-563. Register Call Summary for Register CONTROL_PADCONF_WAKEUPEVENT_5

Control Module Register Manual
- SYSCTRL_PADCONF_CORE Register Summary: [0]

Table 18-564. CONTROL_PADCONF_WAKEUPEVENT_6

Address Offset	0x0000 01F0		
Physical Address	0x4A10 01F0	**Instance**	SYSCTRL_PADCONF_CORE
Description	Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							DPM_EMU19_DUPLICATEWAKEUPEVENT	DPM_EMU18_DUPLICATEWAKEUPEVENT	DPM_EMU17_DUPLICATEWAKEUPEVENT	DPM_EMU16_DUPLICATEWAKEUPEVENT	DPM_EMU15_DUPLICATEWAKEUPEVENT	DPM_EMU14_DUPLICATEWAKEUPEVENT	DPM_EMU13_DUPLICATEWAKEUPEVENT	DPM_EMU12_DUPLICATEWAKEUPEVENT	DPM_EMU11_DUPLICATEWAKEUPEVENT

Bits	Field Name	Description	Type	Reset
31: 11	RESERVED		R	0x000000
10	CSI22_DY2_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad csi22_dy2 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
9	CSI22_DX2_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad csi22_dx2 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
8	DPM_EMU19_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad dpm_emu19 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0x000000
7	DPM_EMU18_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad dpm_emu18 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0

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Bits	Field Name	Description	Type	Reset
6	DPM_EMU17_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad dpm_emu17 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
5	DPM_EMU16_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad dpm_emu16 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
4	DPM_EMU15_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad dpm_emu15 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
3	DPM_EMU14_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad dpm_emu14 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
2	DPM_EMU13_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad dpm_emu13 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
1	DPM_EMU12_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad dpm_emu12 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
0	DPM_EMU11_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad dpm_emu11 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0

Table 18-565. Register Call Summary for Register CONTROL_PADCONF_WAKEUPEVENT_6

Control Module Functional Description • Off Mode Pad Control Overview: [0]
Control Module Register Manual • SYSCTRL_PADCONF_CORE Register Summary: [1]

Table 18-566. CONTROL_CORE_PAD0_CSI22_DY2

Address Offset	0x0000 01F4		
Physical Address	0x4A10 01F4	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pad csi22_dy2 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																CSI22_DY2_WAKEUPEVENT	CSI22_DY2_WAKEUPENABLE	RESERVED					CSI22_DY2_INPUTENABLE	RESERVED			CSI22_DY2_PULLTYPESELECT	CSI22_DY2_PULLUDENABLE	CSI22_DY2_MUXMODE		

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15	CSI22_DY2_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	CSI22_DY2_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection on low level 0x1: wake-up detection on high level	RW	0
13:9	RESERVED		R	0x00
8	CSI22_DY2_INPUTENABLE	Input enable value for pad csi22_dy2 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	CSI22_DY2_PULLTYPESELECT	Pull-Up/Down selection for pad csi22_dy2 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	CSI22_DY2_PULLUDENABLE	Pull-Up/Down enable for pad csi22_dy2 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	CSI22_DY2_MUXMODE	Functional multiplexing selection for pad csi22_dy2 0x0: Select csi22_dy2 0x2: Select cam2_wen 0x7: Select safe_mode	RW	0x7

Table 18-567. Register Call Summary for Register CONTROL_CORE_PAD0_CSI22_DY2

Control Module Register Manual

- SYSCTRL_PADCONF_CORE Register Summary: [0]

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Table 18-568. CONTROL_PADCONF_GLOBAL

Address Offset	0x0000 05A0		
Physical Address	0x4A10 05A0	**Instance**	SYSCTRL_PADCONF_CORE
Description	Global PAD control Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FORCE_OFFMODE_EN	RESERVED																														

Bits	Field Name	Description	Type	Reset
31	FORCE_OFFMODE_EN	Force offmode enable for PADs 0x0: Offmode is not forced active 0x1: Offmode is forced active	RW	0
30:0	RESERVED		R	0x0000 0000

Table 18-569. Register Call Summary for Register CONTROL_PADCONF_GLOBAL

Control Module Functional Description

- Device Core Control Module Instance: [0]
- Off Mode Pad Control Overview: [1]

Control Module Register Manual

- SYSCTRL_PADCONF_CORE Register Summary: [2]

Table 18-570. CONTROL_CORE_PADCONF_MODE

Address Offset	0x0000 05A4		
Physical Address	0x4A10 05A4	**Instance**	SYSCTRL_PADCONF_CORE
Description	PAD Voltage Mode control Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VDDS_DV_BANK0	VDDS_DV_BANK1	VDDS_DV_BANK3	VDDS_DV_BANK4	VDDS_DV_BANK5	VDDS_DV_BANK6	VDDS_DV_C2C	VDDS_DV_CAM	VDDS_DV_GPMC0	VDDS_DV_SDMMC2	VDDS_DV_BANK7	VDDS_DV_GPMC1	VDDS_DV_BANK2_SHARED0																			

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Bits	Field Name	Description	Type	Reset
31	VDDS_DV_BANK0	PAD Voltage level control for vdds_dv_bank0 0x0: VDDS = 1.8V 0x1: VDDS = 1.2V	RW	0
30	VDDS_DV_BANK1	PAD Voltage level control for vdds_dv_bank1 0x0: VDDS = 1.8V 0x1: VDDS = 1.2V	RW	0
29	VDDS_DV_BANK3	PAD Voltage level control for vdds_dv_bank3 0x0: VDDS = 1.8V 0x1: VDDS = 1.2V	RW	0
28	VDDS_DV_BANK4	PAD Voltage level control for vdds_dv_bank4 0x0: VDDS = 1.8V 0x1: VDDS = 1.2V	RW	0
27	VDDS_DV_BANK5	PAD Voltage level control for vdds_dv_bank5 0x0: VDDS = 1.8V 0x1: VDDS = 1.2V	RW	0
26	VDDS_DV_BANK6	PAD Voltage level control for vdds_dv_bank6 0x0: VDDS = 1.8V 0x1: VDDS = 1.2V	RW	0
25	VDDS_DV_C2C	PAD Voltage level control for vdds_dv_c2c 0x0: VDDS = 1.8V 0x1: VDDS = 1.2V	RW	0
24	VDDS_DV_CAM	PAD Voltage level control for vdds_dv_cam 0x0: VDDS = 1.8V 0x1: VDDS = 1.2V	RW	0
23	VDDS_DV_GPMC0	PAD Voltage level control for vdds_dv_gpmc0 0x0: VDDS = 1.8V 0x1: VDDS = 1.2V	RW	0
22	VDDS_DV_SDMMC2	PAD Voltage level control for vdds_dv_sdmmc2 0x0: VDDS = 1.8V 0x1: VDDS = 1.2V	RW	0
21	VDDS_DV_BANK7	PAD Voltage level control for vdds_dv_bank7 0x0: VDDS = 1.8V 0x1: VDDS = 1.2V	RW	0
20	VDDS_DV_GPMC1	PAD Voltage level control for vdds_dv_gpmc1 0x0: VDDS = 1.8V 0x1: VDDS = 1.2V	RW	0
19	VDDS_DV_BANK2_SHARED0	PAD Voltage level control for vdds_dv_bank2_shared0 0x0: VDDS = 1.8V 0x1: VDDS = 1.2V	RW	0
18:0	RESERVED		R	0x000000

Table 18-571. Register Call Summary for Register CONTROL_CORE_PADCONF_MODE

Control Module Functional Description
- Signal Integrity Parameter Control Registers With Pad Group Assignment: [0]
- Dual Voltage-Supplied Peripheral Controls: [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14]

Control Module Programming Guide
- Operational Modes Configuration: [15] [16] [17] [18] [19] [20]

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Table 18-571. Register Call Summary for Register CONTROL_CORE_PADCONF_MODE (continued)

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- SYSCTRL_PADCONF_CORE Register Summary: [21]

Table 18-572. CONTROL_SMART1IO_PADCONF_0

Address Offset	0x0000 05A8		
Physical Address	0x4A10 05A8	**Instance**	SYSCTRL_PADCONF_CORE
Description	SMART1 I/O control 0 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31 30	29 28	27 26 25 24	23 22	21 20	19 18	17 16	15 14	13 12	11 10	9 8	7 6	5 4	3 2 1 0
ABE_DR0_SC	CAM_DR0_SC	RESERVED	GPIO_DR8_SC	GPIO_DR9_SC	RESERVED	GPMC_DR3_SC	RESERVED	GPIO_63_64_DR0_SC	MCSPI1_DR0_SC	UART1_DR0_SC	UART3_DR0_SC	UART3_DR1_SC	RESERVED

Bits	Field Name	Description	Type	Reset
31:30	ABE_DR0_SC	Slew rate control for group abe_dr0. Refer to Section 18.4.12.9.3, section Low Speed I/Os Combined Slew Rate vs TL Length and Load Settings for more details on SR settings.	RW	0x0
29:28	CAM_DR0_SC	Slew rate control for group cam_dr0. Refer to Section 18.4.12.9.3, section Low Speed I/Os Combined Slew Rate vs TL Length and Load Settings for more details on SR settings.	RW	0x0
27:24	RESERVED	Reserved	RW	0x0
23:22	GPIO_DR8_SC	Slew rate control for group gpio_dr8. Refer to Section 18.4.12.9.3, section Low Speed I/Os Combined Slew Rate vs TL Length and Load Settings for more details on SR settings.	RW	0x0
21:20	GPIO_DR9_SC	Slew rate control for group gpio_dr9. Refer to Section 18.4.12.9.3, section Low Speed I/Os Combined Slew Rate vs TL Length and Load Settings for more details on SR settings.	RW	0x0
19:18	RESERVED	Reserved	RW	0x0
17:16	GPMC_DR3_SC	Slew rate control for group gpmc_dr3. Refer to Section 18.4.12.9.3, section Low Speed I/Os Combined Slew Rate vs TL Length and Load Settings for more details on SR settings.	RW	0x1
15:14	RESERVED	Reserved	RW	0x0
13:12	GPIO_63_64_DR0_SC	Slew rate control for group gpio_63_64_dr0. Refer to Section 18.4.12.9.3, section Low Speed I/Os Combined Slew Rate vs TL Length and Load Settings for more details on SR settings.	RW	0x0

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Bits	Field Name	Description	Type	Reset
11:10	MCSPI1_DR0_SC	Slew rate control for group mcspi1_dr0 Refer to Section 18.4.12.9.3, section Low Speed I/Os Combined Slew Rate vs TL Length and Load Settings for more details on SR settings.	RW	0x0
9:8	UART1_DR0_SC	Slew rate control for group uart1_dr0 Refer to Section 18.4.12.9.3, section Low Speed I/Os Combined Slew Rate vs TL Length and Load Settings for more details on SR settings.	RW	0x0
7:6	UART3_DR0_SC	Slew rate control for group uart3_dr0 Refer to Section 18.4.12.9.3, section Low Speed I/Os Combined Slew Rate vs TL Length and Load Settings for more details on SR settings.	RW	0x0
5:4	UART3_DR1_SC	Slew rate control for group uart3_dr1 Refer to Section 18.4.12.9.3, section Low Speed I/Os Combined Slew Rate vs TL Length and Load Settings for more details on SR settings.	RW	0x0
3:0	RESERVED	Reserved	RW	0x0

Table 18-573. Register Call Summary for Register CONTROL_SMART1IO_PADCONF_0

Control Module Functional Description

- Signal Integrity Parameter Control Registers With Pad Group Assignment: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10]

Control Module Register Manual

- SYSCTRL_PADCONF_CORE Register Summary: [11]

Table 18-574. CONTROL_SMART1IO_PADCONF_1

Address Offset	0x0000 05AC		
Physical Address	0x4A10 05AC	**Instance**	SYSCTRL_PADCONF_CORE
Description	SMART1 I/O control 1 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31 30	29 28	27 26 25 24	23 22	21 20	19 18	17 16	15 14	13 12	11 10	9 8	7 6	5 4	3 2 1 0
ABE_DR0_LB	CAM_DR0_LB	RESERVED	GPIO_DR8_LB	GPIO_DR9_LB	RESERVED	GPMC_DR3_LB	RESERVED	GPIO_63_64_DR0_LB	MCSPI1_DR0_LB	UART1_DR0_LB	UART3_DR0_LB	UART3_DR1_LB	RESERVED

Bits	Field Name	Description	Type	Reset
31:30	ABE_DR0_LB	Load control for group abe_dr0 0x0: TL Length= [2cm-20cm] / Farend(1) cap per TL= [1pF-10pF] 0x1: Dual TL Length= [20cm-40cm] / Farend cap per TL= [1pF-10pF] 0x2: TL Length = [2cm-20cm] / Farend cap per TL= [10pF-20pF] 0x3: Dual TL Length = [20cm-40cm] / Farend cap per TL= [10pF-20pF]	RW	0x0

(1) Far-end load is equivalent to CLoad, where CLoad is the total capacitance seen at the far end of the transmission line.

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Bits	Field Name	Description	Type	Reset
29:28	CAM_DR0_LB	Load control for group cam_dr0 0x0: TL Length= [2cm-20cm] / Farend cap per TL= [1pF-10pF] 0x1: Dual TL Length= [20cm-40cm] / Farend cap per TL= [1pF-10pF] 0x2: TL Length = [2cm-20cm] / Farend cap per TL= [10pF-20pF] 0x3: Dual TL Length = [20cm-40cm] / Farend cap per TL= [10pF-20pF]	RW	0x0
27:24	RESERVED	Reserved	RW	0x0
23:22	GPIO_DR8_LB	Load control for group gpio_dr8 0x0: TL Length= [2cm-20cm] / Farend cap per TL= [1pF-10pF] 0x1: Dual TL Length= [20cm-40cm] / Farend cap per TL= [1pF-10pF] 0x2: TL Length = [2cm-20cm] / Farend cap per TL= [10pF-20pF] 0x3: Dual TL Length = [20cm-40cm] / Farend cap per TL= [10pF-20pF]	RW	0x0
21:20	GPIO_DR9_LB	Load control for group gpio_dr9 0x0: TL Length= [2cm-20cm] / Farend cap per TL= [1pF-10pF] 0x1: Dual TL Length= [20cm-40cm] / Farend cap per TL= [1pF-10pF] 0x2: TL Length = [2cm-20cm] / Farend cap per TL= [10pF-20pF] 0x3: Dual TL Length = [20cm-40cm] / Farend cap per TL= [10pF-20pF]	RW	0x0
19:18	RESERVED	Reserved	RW	0x0
17:16	GPMC_DR3_LB	Load control for group gpmc_dr3 0x0: TL Length= [2cm-20cm] / Farend cap per TL= [1pF-10pF] 0x1: Dual TL Length= [20cm-40cm] / Farend cap per TL= [1pF-10pF] 0x2: TL Length = [2cm-20cm] / Farend cap per TL= [10pF-20pF] 0x3: Dual TL Length = [20cm-40cm] / Farend cap per TL= [10pF-20pF]	RW	0x0
15:14	RESERVED	Reserved	RW	0x0
13:12	GPIO_63_64_DR0_LB	Load control for group gpio_63_64_dr0 0x0: TL Length= [2cm-20cm] / Farend cap per TL= [1pF-10pF] 0x1: Dual TL Length= [20cm-40cm] / Farend cap per TL= [1pF-10pF] 0x2: TL Length = [2cm-20cm] / Farend cap per TL= [10pF-20pF] 0x3: Dual TL Length = [20cm-40cm] / Farend cap per TL= [10pF-20pF]	RW	0x0
11:10	MCSPI1_DR0_LB	Load control for group mcspi1_dr0 0x0: TL Length= [2cm-20cm] / Farend cap per TL= [1pF-10pF] 0x1: Dual TL Length= [20cm-40cm] / Farend cap per TL= [1pF-10pF] 0x2: TL Length = [2cm-20cm] / Farend cap per TL= [10pF-20pF] 0x3: Dual TL Length = [20cm-40cm] / Farend cap per TL= [10pF-20pF]	RW	0x0

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Bits	Field Name	Description	Type	Reset
9:8	UART1_DR0_LB	Load control for group uart1_dr0 0x0: TL Length= [2cm-20cm] / Farend cap per TL= [1pF-10pF] 0x1: Dual TL Length= [20cm-40cm] / Farend cap per TL= [1pF-10pF] 0x2: TL Length = [2cm-20cm] / Farend cap per TL= [10pF-20pF] 0x3: Dual TL Length = [20cm-40cm] / Farend cap per TL= [10pF-20pF]	RW	0x0
7:6	UART3_DR0_LB	Load control for group uart3_dr0 0x0: TL Length= [2cm-20cm] / Farend cap per TL= [1pF-10pF] 0x1: Dual TL Length= [20cm-40cm] / Farend cap per TL= [1pF-10pF] 0x2: TL Length = [2cm-20cm] / Farend cap per TL= [10pF-20pF] 0x3: Dual TL Length = [20cm-40cm] / Farend cap per TL= [10pF-20pF]	RW	0x0
5:4	UART3_DR1_LB	Load control for group uart3_dr1 0x0: TL Length= [2cm-20cm] / Farend cap per TL= [1pF-10pF] 0x1: Dual TL Length= [20cm-40cm] / Farend cap per TL= [1pF-10pF] 0x2: TL Length = [2cm-20cm] / Farend cap per TL= [10pF-20pF] 0x3: Dual TL Length = [20cm-40cm] / Farend cap per TL= [10pF-20pF]	RW	0x0
3:0	RESERVED	Reserved	RW	0x0

Table 18-575. Register Call Summary for Register CONTROL_SMART1IO_PADCONF_1

Control Module Functional Description • Signal Integrity Parameter Control Registers With Pad Group Assignment: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10]
Control Module Register Manual • SYSCTRL_PADCONF_CORE Register Summary: [11]

Table 18-576. CONTROL_SMART2IO_PADCONF_0

Address Offset	0x0000 05B0		
Physical Address	0x4A10 05B0	**Instance**	SYSCTRL_PADCONF_CORE
Description	SMART2 I/O control 0 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

Bits	Field Name	Description	Type	Reset
31:0	RESERVED		RW	0

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Table 18-577. Register Call Summary for Register CONTROL_SMART2IO_PADCONF_0

Control Module Functional Description
- Signal Integrity Parameter Control Registers With Pad Group Assignment: [0]

Control Module Register Manual
- SYSCTRL_PADCONF_CORE Register Summary: [1]

Table 18-578. CONTROL_SMART2IO_PADCONF_1

Address Offset	0x0000 05B4		
Physical Address	0x4A10 05B4	**Instance**	SYSCTRL_PADCONF_CORE
Description	SMART2 I/O control 1 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

Bits	Field Name	Description	Type	Reset
31:0	RESERVED		R	0x0000 0000

Table 18-579. Register Call Summary for Register CONTROL_SMART2IO_PADCONF_1

Control Module Functional Description
- Signal Integrity Parameter Control Registers With Pad Group Assignment: [0]

Control Module Register Manual
- SYSCTRL_PADCONF_CORE Register Summary: [1]

Table 18-580. CONTROL_SMART3IO_PADCONF_0

Address Offset	0x0000 05B8		
Physical Address	0x4A10 05B8	**Instance**	SYSCTRL_PADCONF_CORE
Description	SMART3 I/O control 0 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMIC_DR0_MB		GPIO_DR3_MB		GPIO_DR4_MB		GPIO_DR5_MB		GPIO_DR6_MB		HSI_DR1_MB		HSI_DR2_MB		HSI_DR3_MB		MCBSP2_DR0_MB		MCSPI4_DR0_MB		MCSPI4_DR1_MB		SDMMC3_DR0_MB		RESERVED						SPI2_DR0_MB	

Bits	Field Name	Description	Type	Reset
31:30	DMIC_DR0_MB	50-Ω output buffer mode control for group dmic_dr0. Refer to 50-Ω output buffer I/Os with combined Mode and Load Settings for more details on mode settings.	RW	0x2
29:28	GPIO_DR3_MB	25-Ω output buffer mode control for group gpio_dr3. Refer to I/Os with combined Mode and Load Settings for more details on mode settings.	RW	0x3

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Bits	Field Name	Description	Type	Reset
27:26	GPIO_DR4_MB	25-Ω output buffer mode control for group gpio_dr4. Refer to I/Os with combined Mode and Load Settings for more details on mode settings.	RW	0x3
25:24	GPIO_DR5_MB	50-Ω output buffer mode control for group gpio_dr5. Refer to 50-Ω output buffer I/Os with combined Mode and Load Settings for more details on mode settings.	RW	0x1
23:22	GPIO_DR6_MB	50-Ω output buffer mode control for group gpio_dr6. Refer to 50-Ω output buffer I/Os with combined Mode and Load Settings for more details on mode settings.	RW	0x1
21:20	HSI_DR1_MB	25-Ω output buffer mode control for group hsi_dr1. Refer to the I/Os with combined Mode and Load Settings for more information about mode settings.	RW	0x3
19:18	HSI_DR2_MB	25-Ω output buffer mode control for group hsi_dr2. Refer to the I/Os with combined Mode and Load Settings for more information about mode settings.	RW	0x3
17:16	HSI_DR3_MB	25-Ω output buffer mode control for group hsi_dr3. Refer to I/Os with combined Mode and Load Settings for more details on mode settings.	RW	0x3
15:14	MCBSP2_DR0_MB	50-Ω output buffer mode control for group mcbsp2_dr0. Refer to 50-Ω output buffer I/Os with combined Mode and Load Settings for more details on mode settings.	RW	0x1
13:12	MCSPI4_DR0_MB	50-Ω output buffer mode control for group mcspi4_dr0. Refer to 50-Ω output buffer I/Os with combined Mode and Load Settings for more details on mode settings.	RW	0x1
11:10	MCSPI4_DR1_MB	50-Ω output buffer mode control for group mcspi4_dr1. Refer to 50-Ω output buffer I/Os with combined Mode and Load Settings for more details on mode settings.	RW	0x1
9:8	SDMMC3_DR0_MB	50-Ω output buffer mode control for group sdmmc3_dr0. Refer to 50-Ω output buffer I/Os with combined Mode and Load Settings for more details on mode settings.	RW	0x1
7:2	RESERVED		R	0x00
1:0	SPI2_DR0_MB	50-Ω output buffer mode control for group spi2_dr0. Refer to 50-Ω output buffer I/Os with combined Mode and Load Settings for more details on mode settings.	RW	0x1

Table 18-581. Register Call Summary for Register CONTROL_SMART3IO_PADCONF_0

Control Module Functional Description

- Signal Integrity Parameter Control Registers With Pad Group Assignment: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13]

Control Module Register Manual

- SYSCTRL_PADCONF_CORE Register Summary: [14]

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Table 18-582. CONTROL_SMART3IO_PADCONF_1

Address Offset	0x0000 05BC		
Physical Address	0x4A10 05BC	**Instance**	SYSCTRL_PADCONF_CORE
Description	SMART3 I/O control 1 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31 30	29 28	27 26	25 24	23 22	21 20	19 18 17 16	15 14	13 12	11 10 9 8	7 6	5 4	3 2	1 0
SPI2_DR1_MB	SPI2_DR2_MB	UART2_DR0_MB	UART2_DR1_MB	UART4_DR0_MB	HSI_DR0_MB	RESERVED		GPMC_DR1_MB	RESERVED	PDM_DR0_MB	FREF_DR2_MB	FREF_DR3_MB	USBB1_DR2_MB

Bits	Field Name	Description	Type	Reset
31:30	SPI2_DR1_MB	50-Ω output buffer mode control for group spi2_dr1. Refer to 50-Ω output buffer I/Os with combined Mode and Load Settings for more details on mode settings.	RW	0x1
29:28	SPI2_DR2_MB	50-Ω output buffer mode control for group spi2_dr1. Refer to 50-Ω output buffer I/Os with combined Mode and Load Settings for more details on mode settings.	RW	0x1
27:26	UART2_DR0_MB	50-Ω output buffer mode control for group spi2_dr1. Refer to 50-Ω output buffer I/Os with combined Mode and Load Settings for more details on mode settings.	RW	0x1
25:24	UART2_DR1_MB	50-Ω output buffer mode control for group spi2_dr1. Refer to 50-Ω output buffer I/Os with combined Mode and Load Settings for more details on mode settings.	RW	0x1
23:22	UART4_DR0_MB	50-Ω output buffer mode control for group spi2_dr1. Refer to 50-Ω output buffer I/Os with combined Mode and Load Settings for more details on mode settings.	RW	0x1
21:20	HSI_DR0_MB	25-Ω output buffer mode control for group hsi_dr0. Refer to I/Os with combined Mode and Load Settings for more details on mode settings.	RW	0x3
19: 14	RESERVED		R	0x00
13:12	GPMC_DR1_MB	50-Ω output buffer mode control for group gpmc_dr1. Refer to 50-Ω output buffer I/Os with combined Mode and Load Settings for more details on mode settings.	RW	0x3
11:8	RESERVED		RW	0x0
7:6	PDM_DR0_MB	50-Ω output buffer mode control for group pdm_dr0. Refer to 50-Ω output buffer I/Os with combined Mode and Load Settings for more details on mode settings.	RW	0x1
5:4	FREF_DR2_MB	50-Ω output buffer mode control for group fref_dr2. Refer to 50-Ω output buffer I/Os with combined Mode and Load Settings for more details on mode settings.	RW	0x1
3:2	FREF_DR3_MB	50-Ω output buffer mode control for group fref_dr3. Refer to 50-Ω output buffer I/Os with combined Mode and Load Settings for more details on mode settings.	RW	0x1

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Bits	Field Name	Description	Type	Reset
1:0	USBB1_DR2_MB	25-Ω output buffer mode control for group usbb1_dr2. Refer to I/Os with combined Mode and Load Settings for more details on mode settings.	RW	0x3

Table 18-583. Register Call Summary for Register CONTROL_SMART3IO_PADCONF_1

Control Module Functional Description • Signal Integrity Parameter Control Registers With Pad Group Assignment: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11]
Control Module Programming Guide • Operational Modes Configuration: [12] [13] [14] [15]
Control Module Register Manual • SYSCTRL_PADCONF_CORE Register Summary: [16]

Table 18-584. CONTROL_SMART3IO_PADCONF_2

Address Offset	0x0000 05C0		
Physical Address	0x4A10 05C0	**Instance**	SYSCTRL_PADCONF_CORE
Description	SMART3 I/O control 2 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMIC_DR0_LB	GPIO_DR3_LB	GPIO_DR4_LB	GPIO_DR5_LB	GPIO_DR6_LB	HSI_DR1_LB	HSI_DR2_LB	HSI_DR3_LB	MCBSP2_DR0_LB	MCSPI4_DR0_LB	MCSPI4_DR1_LB	RESERVED		SLIMBUS2_DR0_LB	RESERVED	SPI2_DR0_LB	SPI2_DR1_LB	SPI2_DR2_LB	UART2_DR0_LB	UART2_DR1_LB	UART4_DR0_LB	HSI_DR0_LB	FREF_DR3_LB	GPMC_DR1_LB	PDM_DR0_LB	FREF_DR2_LB	SDMMC3_DR0_LB	USBB1_DR2_LB	RESERVED			

Bits	Field Name	Description	Type	Reset
31	DMIC_DR0_LB	50-Ω output buffer load control dmic_dr0_lb Refer to 50-Ω output buffer I/Os with combined Mode and Load Settings for more details on mode settings.	RW	0
30	GPIO_DR3_LB	25-Ω output buffer load control gpio_dr3_lb Refer to I/Os with combined Mode and Load Settings for more details on mode settings.	RW	1
29	GPIO_DR4_LB	25-Ω output buffer load control gpio_dr4_lb Refer to I/Os with combined Mode and Load Settings for more details on mode settings.	RW	1
28	GPIO_DR5_LB	50-Ω output buffer load control gpio_dr5_lb Refer to 50-Ω output buffer I/Os with combined Mode and Load Settings for more details on mode settings.	RW	0
27	GPIO_DR6_LB	50-Ω output buffer load control gpio_dr6_lb Refer to 50-Ω output buffer I/Os with combined Mode and Load Settings for more details on mode settings.	RW	0
26	HSI_DR1_LB	25-Ω output buffer load control hsi_dr1_lb Refer to I/Os with combined Mode and Load Settings for more details on mode settings.	RW	1

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Bits	Field Name	Description	Type	Reset
25	HSI_DR2_LB	25-Ω output buffer load control hsi_dr2_lb Refer to I/Os with combined Mode and Load Settings for more details on mode settings.	RW	1
24	HSI_DR3_LB	25-Ω output buffer load control hsi_dr3_lb Refer to I/Os with combined Mode and Load Settings for more details on mode settings.	RW	1
23	MCBSP2_DR0_LB	50-Ω output buffer load control mcbsp2_dr0_lb Refer to 50-Ω output buffer I/Os with combined Mode and Load Settings for more details on mode settings.	RW	0
22	MCSPI4_DR0_LB	50-Ω output buffer load control mcspi4_dr0_lb Refer to 50-Ω output buffer I/Os with combined Mode and Load Settings for more details on mode settings.	RW	0
21	MCSPI4_DR1_LB	50-Ω output buffer load control mcspi4_dr1_lb Refer to 50-Ω output buffer I/Os with combined Mode and Load Settings for more details on mode settings.	RW	0
20: 17	RESERVED		R	0x0
16	SPI2_DR0_LB	50-Ω output buffer load control spi2_dr0_lb Refer to 50-Ω output buffer I/Os with combined Mode and Load Settings for more details on mode settings.	RW	0
15	SPI2_DR1_LB	50-Ω output buffer load control spi2_dr1_lb Refer to 50-Ω output buffer I/Os with combined Mode and Load Settings for more details on mode settings.	RW	0
14	SPI2_DR2_LB	50-Ω output buffer load control spi2_dr2_lb Refer to 50-Ω output buffer I/Os with combined Mode and Load Settings for more details on mode settings.	RW	0
13	UART2_DR0_LB	50-Ω output buffer load control uart2_dr0_lb Refer to 50-Ω output buffer I/Os with combined Mode and Load Settings for more details on mode settings.	RW	0
12	UART2_DR1_LB	50-Ω output buffer load control uart2_dr1_lb Refer to 50-Ω output buffer I/Os with combined Mode and Load Settings for more details on mode settings.	RW	0
11	UART4_DR0_LB	50-Ω output buffer load control uart4_dr0_lb Refer to 50-Ω output buffer I/Os with combined Mode and Load Settings for more details on mode settings.	RW	0
10	HSI_DR0_LB	25-Ω output buffer load control hsi_dr0 Refer to I/Os with combined Mode and Load Settings for more details on mode settings.	RW	1
9	FREF_DR3_LB	50-Ω output buffer load control fref_dr3 Refer to 50-Ω output buffer I/Os with combined Mode and Load Settings for more details on mode settings.	RW	0
8	GPMC_DR1_LB	50-Ω output buffer load control gpmc_dr1 Refer to 50-Ω output buffer I/Os with combined Mode and Load Settings for more details on mode settings.	RW	1
7	PDM_DR0_LB	50-Ω output buffer load control pdm_dr0 Refer to 50-Ω output buffer I/Os with combined Mode and Load Settings for more details on mode settings.	RW	0

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Bits	Field Name	Description	Type	Reset
6	FREF_DR2_LB	50-Ω output buffer load control fref_dr2 Refer to 50-Ω output buffer I/Os with combined Mode and Load Settings for more details on mode settings.	RW	0
5	SDMMC3_DR0_LB	50-Ω output buffer load control sdmmc3_dr0 Refer to 50-Ω output buffer I/Os with combined Mode and Load Settings for more details on mode settings.	RW	0
4	USBB1_DR2_LB	25-Ω output buffer load control usbb1_dr2 Refer to I/Os with combined Mode and Load Settings for more details on mode settings.	RW	1
3:0	RESERVED		R	0x0

Table 18-585. Register Call Summary for Register CONTROL_SMART3IO_PADCONF_2

Control Module Functional Description

- Signal Integrity Parameter Control Registers With Pad Group Assignment: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23] [24]

Control Module Programming Guide

- Operational Modes Configuration: [25] [26] [27] [28]

Control Module Register Manual

- SYSCTRL_PADCONF_CORE Register Summary: [29]

Table 18-586. CONTROL_USBB_HSIC

Address Offset	0x0000 05C4		
Physical Address	0x4A10 05C4	**Instance**	SYSCTRL_PADCONF_CORE
Description	USBB HSIC control Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
USBB2_DR1_SR		USBB2_DR1_I		USBB1_DR1_SR		USBB1_DR1_I		USBB1_HSIC_DATA_WD				USBB1_HSIC_STROBE_WD				USBB2_HSIC_DATA_WD								USBB2_HSIC_STROBE_WD							
																		USBB1_HSIC_DATA_OFFMODE_WD_ENABLE													
																			USBB1_HSIC_DATA_OFFMODE_WD												
																					USBB1_HSIC_STROBE_OFFMODE_WD_ENABLE											
																						USBB1_HSIC_STROBE_OFFMODE_WD										
																								USBB2_HSIC_DATA_OFFMODE_WD_ENABLE									
																										USBB2_HSIC_DATA_OFFMODE_WD						
																												USBB2_HSIC_STROBE_OFFMODE_WD_ENABLE				

Bits	Field Name	Description	Type	Reset
31:30	USBB2_DR1_SR	usbb2 Slew Rate control sr1:sr0 0x0: Turn_on time 125ps for Drv8 0x1: Turn_on time 500ps for Drv8 0x2: Turn_on time 325ps for Drv8 0x3: Turn_on time 750ps for Drv8	RW	0x0
29:27	USBB2_DR1_I	usbb2 Impedence control i2:i0 0x0: for Drv5 0x1: for Drv6 0x2: for Drv7 0x3: for Drv8 0x4: for Drv9 0x5: for Drv10 0x6: for Drv11 0x7: Drv12	RW	0x6
26:25	USBB1_DR1_SR	usbb1 Slew Rate control sr1:sr0 0x0: Turn_on time 125ps for Drv8 0x1: Turn_on time 500ps for Drv8 0x2: Turn_on time 325ps for Drv8 0x3: Turn_on time 750ps for Drv8	RW	0x0
24:22	USBB1_DR1_I	usbb1 Impedence control i2:i0 0x0: for Drv5 0x1: for Drv6 0x2: for Drv7 0x3: for Drv8 0x4: for Drv9 0x5: for Drv10 0x6: for Drv11 0x7: Drv12	RW	0x6
21:20	USBB1_HSIC_DATA_WD	usbb1_hsic_data wd1:wd0 0x0: Pull logic disabled 0x1: pull up 0x2: pull down 0x3: Maintain the previous output value	RW	0x2
19:18	USBB1_HSIC_STROBE_WD	usbb1_hsic_strobe wd1:wd0 0x0: Pull logic disabled 0x1: pull up 0x2: pull down 0x3: Maintain the previous output value	RW	0x2
17:16	USBB2_HSIC_DATA_WD	usbb2_hsic_data wd1:wd0 0x0: Pull logic disabled 0x1: pull up 0x2: pull down 0x3: Maintain the previous output value	RW	0x2
15:14	USBB2_HSIC_STROBE_WD	usbb2_hsic_strobe wd1:wd0 0x0: Pull logic disabled 0x1: pull up 0x2: pull down 0x3: Maintain the previous output value	RW	0x2

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Bits	Field Name	Description	Type	Reset
13	USBB1_HSIC_DATA_OFFMODE_WD_ENABLE	usbb1_hsic_data_offmode_wd enable 0x0: offmode_wd1 0x1: offmode_wd1	RW	0
12:11	USBB1_HSIC_DATA_OFFMODE_WD	usbb1_hsic_data_offmode_wd1:wd0 0x0: Pull logic disabled 0x1: pull up 0x2: pull down 0x3: Maintain the previous output value	RW	0x0
10	USBB1_HSIC_STROBE_OFFMODE_WD_ENABLE	usbb1_hsic_strobe_offmode_wd enable 0x0: offmode_wd1 0x1: offmode_wd1	RW	0
9:8	USBB1_HSIC_STROBE_OFFMODE_WD	usbb1_hsic_strobe_offmode_wd1:wd0 0x0: Pull logic disabled 0x1: pull up 0x2: pull down 0x3: Maintain the previous output value	RW	0x0
7	USBB2_HSIC_DATA_OFFMODE_WD_ENABLE	usbb2_hsic_data_offmode_wd enable 0x0: offmode_wd1 0x1: offmode_wd1	RW	0
6:5	USBB2_HSIC_DATA_OFFMODE_WD	usbb2_hsic_data_offmode_wd1:wd0 0x0: Pull logic disabled 0x1: pull up 0x2: pull down 0x3: Maintain the previous output value	RW	0x0
4	USBB2_HSIC_STROBE_OFFMODE_WD_ENABLE	usbb2_hsic_strobe_offmode_wd enable 0x0: offmode_wd1 0x1: offmode_wd1	RW	0
3:2	USBB2_HSIC_STROBE_OFFMODE_WD	usbb2_hsic_strobe_offmode_wd1:wd0 0x0: Pull logic disabled 0x1: pull up 0x2: pull down 0x3: Maintain the previous output value	RW	0x0
1:0	RESERVED		R	0x0

Table 18-587. Register Call Summary for Register CONTROL_USBB_HSIC

Control Module Functional Description

- Pull Selection: [0]
- Off Mode Pad Control Overview: [1]
- Signal Integrity Parameter Control Registers With Pad Group Assignment: [2] [3] [4] [5]

Control Module Register Manual

- SYSCTRL_PADCONF_CORE Register Summary: [6]

Table 18-588. CONTROL_SMART3IO_PADCONF_3

Address Offset	0x0000 05C8		
Physical Address	0x4A10 05C8	**Instance**	SYSCTRL_PADCONF_CORE
Description	SMART3 IO control 3 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31 30	29 28	27 26	25 24	23 22	21 20	19	18	17	16	15 14	13 12 11 10 9 8	7 6 5 4 3 2 1 0
SLIMBUS1_DR0_MB	SLIMBUS1_DR1_MB	SLIMBUS2_DR0_MB	SLIMBUS2_DR1_MB	SLIMBUS2_DR2_MB	SLIMBUS2_DR3_MB	SLIMBUS1_DR0_LB	SLIMBUS2_DR1_LB	SLIMBUS2_DR2_LB	SLIMBUS2_DR3_LB	SLIMBUS1_DR1_LB SLIMBUS2_DR0_LB	RESERVED	

Bits	Field Name	Description	Type	Reset
31:30	SLIMBUS1_DR0_MB	50-Ω output buffer mode control for group slimbus1_dr0 Refer to 50-Ω output buffer I/Os with combined Mode and Load Settings for more details on mode settings.	RW	0x1
29:28	SLIMBUS1_DR1_MB	50-Ω output buffer mode control for group slimbus1_dr1 Refer to 50-Ω output buffer I/Os with combined Mode and Load Settings for more details on mode settings.	RW	0x1
27:26	SLIMBUS2_DR0_MB	50-Ω output buffer mode control for group slimbus2_dr0 Refer to 50-Ω output buffer I/Os with combined Mode and Load Settings for more details on mode settings.	RW	0x1
25:24	SLIMBUS2_DR1_MB	50-Ω output buffer mode control for group slimbus2_dr1 Refer to 50-Ω output buffer I/Os with combined Mode and Load Settings for more details on mode settings.	RW	0x1
23:22	SLIMBUS2_DR2_MB	50-Ω output buffer mode control for group slimbus2_dr2 Refer to 50-Ω output buffer I/Os with combined Mode and Load Settings for more details on mode settings.	RW	0x1
21:20	SLIMBUS2_DR3_MB	50-Ω output buffer mode control for group slimbus2_dr3 Refer to 50-Ω output buffer I/Os with combined Mode and Load Settings for more details on mode settings.	RW	0x1
19	SLIMBUS1_DR0_LB	50-Ω output buffer load control for group slimbus1_dr0 Refer to 50-Ω output buffer I/Os with combined Mode and Load Settings for more details on mode settings.	RW	0
18	SLIMBUS2_DR1_LB	50-Ω output buffer load control for group slimbus2_dr1 Refer to 50-Ω output buffer I/Os with combined Mode and Load Settings for more details on mode settings.	RW	0
17	SLIMBUS2_DR2_LB	50-Ω output buffer load control for group slimbus2_dr2 Refer to 50-Ω output buffer I/Os with combined Mode and Load Settings for more details on mode settings.	RW	0
16	SLIMBUS2_DR3_LB	50-Ω output buffer load control for group slimbus2_dr3 Refer to 50-Ω output buffer I/Os with combined Mode and Load Settings for more details on mode settings.	RW	0
15	SLIMBUS1_DR1_LB	50-Ω output buffer load control for group slimbus1_dr1 Refer to 50-Ω output buffer I/Os with combined Mode and Load Settings for more details on mode settings.	RW	0
14	SLIMBUS2_DR0_LB	50-Ω output buffer load control for group slimbus2_dr0 Refer to 50-Ω output buffer I/Os with combined Mode and Load Settings for more details on mode settings.	RW	0
13:0	RESERVED		R	0x0000

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Table 18-589. Register Call Summary for Register CONTROL_SMART3IO_PADCONF_3

Control Module Functional Description
• Signal Integrity Parameter Control Registers With Pad Group Assignment: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12]
Control Module Register Manual
• SYSCTRL_PADCONF_CORE Register Summary: [13]

Table 18-590. CONTROL_SMART2IO_PADCONF_2

Address Offset	0x0000 05CC		
Physical Address	0x4A10 05CC	**Instance**	SYSCTRL_PADCONF_CORE
Description	SMART2 IO control 2 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DPM_DR1_DS	DPM_DR2_DS	DPM_DR3_DS	GPIO_DR10_DS	HSI2_DR0_DS	HSI2_DR1_DS	HSI2_DR2_DS	SDMMC3_DR0_DS	SDMMC4_DR0_DS	SDMMC4_DR1_DS	SPI3_DR0_DS	SPI3_DR1_DS	UART3_DR2_DS	UART3_DR3_DS	UART3_DR4_DS	UART3_DR5_DS	USBA0_DR0_DS	USBA0_DR1_DS	USBA_DR2_DS	USBB2_DR0_DS	USBB1_DR0_DS	RESERVED										

Bits	Field Name	Description	Type	Reset
31	DPM_DR1_DS	Drive strength control bit for group dpm_dr1 0x0: 50 Ω 0x1: 25 Ω	RW	0
30	DPM_DR2_DS	Drive strength control bit for group dpm_dr2 0x0: 50 Ω 0x1: 25 Ω	RW	0
29	DPM_DR3_DS	Drive strength control bit for group dpm_dr3 0x0: 50 Ω 0x1: 25 Ω	RW	0
28	GPIO_DR10_DS	Drive strength control bit for group gpio_dr10 0x0: 50 Ω 0x1: 25 Ω	RW	0
27	HSI2_DR0_DS	Drive strength control bit for group hsi2_dr0 0x0: 50 Ω 0x1: 25 Ω	RW	0
26	HSI2_DR1_DS	Drive strength control bit for group hsi2_dr1 0x0: 50 Ω 0x1: 25 Ω	RW	0
25	HSI2_DR2_DS	Drive strength control bit for group hsi2_dr2 0x0: 50 Ω 0x1: 25 Ω	RW	0
24	SDMMC3_DR0_DS	Drive strength control bit for group sdmmc3_dr0 0x0: 50 Ω 0x1: 25 Ω	RW	0
23	SDMMC4_DR0_DS	Drive strength control bit for group sdmmc4_dr0 0x0: 50 Ω 0x1: 25 Ω	RW	0

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Bits	Field Name	Description	Type	Reset
22	SDMMC4_DR1_DS	Drive strength control bit for group sdmmc4_dr1 0x0: 50 Ω 0x1: 25 Ω	RW	0
21	SPI3_DR0_DS	Drive strength control bit for group spi3_dr0 0x0: 50 Ω 0x1: 25 Ω	RW	0
20	SPI3_DR1_DS	Drive strength control bit for group spi3_dr1 0x0: 50 Ω 0x1: 25 Ω	RW	0
19	UART3_DR2_DS	Drive strength control bit for group uart3_dr2 0x0: 50 Ω 0x1: 25 Ω	RW	0
18	UART3_DR3_DS	Drive strength control bit for group uart3_dr3 0x0: 50 Ω 0x1: 25 Ω	RW	0
17	UART3_DR4_DS	Drive strength control bit for group uart3_dr4 0x0: 50 Ω 0x1: 25 Ω	RW	0
16	UART3_DR5_DS	Drive strength control bit for group uart3_dr5 0x0: 50 Ω 0x1: 25 Ω	RW	0
15	USBA0_DR0_DS	Drive strength control bit for group usba0_dr0 0x0: 50 Ω 0x1: 25 Ω	RW	0
14	USBA0_DR1_DS	Drive strength control bit for group usba0_dr1 0x0: 50 Ω 0x1: 25 Ω	RW	0
13	USBA_DR2_DS	Drive strength control bit for group usba_dr2 0x0: 50 Ω 0x1: 25 Ω	RW	0
12	USBB2_DR0_DS	Drive strength control bit for group usbb2_dr0 0x0: 50 Ω 0x1: 25 Ω	RW	0
11	USBB1_DR0_DS	Drive strength control bit for group usbb1_dr0 0x0: 50 Ω 0x1: 25 Ω	RW	0
10:0	RESERVED		R	0x000

Table 18-591. Register Call Summary for Register CONTROL_SMART2IO_PADCONF_2

Control Module Functional Description • Signal Integrity Parameter Control Registers With Pad Group Assignment: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21]
Control Module Programming Guide • Operational Modes Configuration: [22] [23]
Control Module Register Manual • SYSCTRL_PADCONF_CORE Register Summary: [24]

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Table 18-592. CONTROL_SMART1IO_PADCONF_2

Address Offset	0x0000 05D0		
Physical Address	0x4A10 05D0	**Instance**	SYSCTRL_PADCONF_CORE
Description	SMART1 IO control 2 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31 30	29 28	27 26	25 24	23 22	21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
KPD_DR0_SC	KPD_DR1_SC	KPD_DR2_SC	KPD_DR3_SC	HDQ_DR0_SC	RESERVED		

Bits	Field Name	Description	Type	Reset
31:30	KPD_DR0_SC	Slew rate control for group kpd_dr0 Refer to Section 18.4.12.9.3, section Low Speed I/Os Combined Slew Rate vs TL Length and Load Settings for more details on SR settings.	RW	0x0
29:28	KPD_DR1_SC	Slew rate control for group kpd_dr1 Refer to Section 18.4.12.9.3, section Low Speed I/Os Combined Slew Rate vs TL Length and Load Settings for more details on SR settings.	RW	0x0
27:26	KPD_DR2_SC	Slew rate control for group kpd_dr2 Refer to Section 18.4.12.9.3, section Low Speed I/Os Combined Slew Rate vs TL Length and Load Settings for more details on SR settings.	RW	0x0
25:24	KPD_DR3_SC	Slew rate control for group kpd_dr3 Refer to Section 18.4.12.9.3, section Low Speed I/Os Combined Slew Rate vs TL Length and Load Settings for more details on SR settings.	RW	0x0
23:22	HDQ_DR0_SC	Slew rate control for group hdq_dr0 Refer to Section 18.4.12.9.3, section Low Speed I/Os Combined Slew Rate vs TL Length and Load Settings for more details on SR settings.	RW	0x0
21:0	RESERVED		R	0x000000

Table 18-593. Register Call Summary for Register CONTROL_SMART1IO_PADCONF_2

Control Module Functional Description

- Signal Integrity Parameter Control Registers With Pad Group Assignment: [0] [1] [2] [3] [4] [5]

Control Module Register Manual

- SYSCTRL_PADCONF_CORE Register Summary: [6]

Table 18-594. CONTROL_SMART1IO_PADCONF_3

Address Offset	0x0000 05D4		
Physical Address	0x4A10 05D4	**Instance**	SYSCTRL_PADCONF_CORE
Description	SMART1 IO control 3 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31 30	29 28	27 26	25 24	23 22	21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
KPD_DR0_LB	KPD_DR1_LB	KPD_DR2_LB	KPD_DR3_LB	HDQ_DR0_LB	RESERVED		

Bits	Field Name	Description	Type	Reset
31:30	KPD_DR0_LB	Load control for group kpd_dr0 0x0: TL Length= [2cm-20cm] / Farend[(1)] cap per TL= [1pF-10pF] 0x1: Dual TL Length= [20cm-40cm] / Farend cap per TL= [1pF-10pF] 0x2: TL Length = [2cm-20cm] / Farend cap per TL= [10pF-20pF] 0x3: Dual TL Length = [20cm-40cm] / Farend cap per TL= [10pF-20pF]	RW	0x0
29:28	KPD_DR1_LB	Load control for group kpd_dr1 0x0: TL Length= [2cm-20cm] / Farend cap per TL= [1pF-10pF] 0x1: Dual TL Length= [20cm-40cm] / Farend cap per TL= [1pF-10pF] 0x2: TL Length = [2cm-20cm] / Farend cap per TL= [10pF-20pF] 0x3: Dual TL Length = [20cm-40cm] / Farend cap per TL= [10pF-20pF]	RW	0x0
27:26	KPD_DR2_LB	Load control for group kpd_dr2 0x0: TL Length= [2cm-20cm] / Farend cap per TL= [1pF-10pF] 0x1: Dual TL Length= [20cm-40cm] / Farend cap per TL= [1pF-10pF] 0x2: TL Length = [2cm-20cm] / Farend cap per TL= [10pF-20pF] 0x3: Dual TL Length = [20cm-40cm] / Farend cap per TL= [10pF-20pF]	RW	0x0
25:24	KPD_DR3_LB	Load control for group kpd_dr3 0x0: TL Length= [2cm-20cm] / Farend cap per TL= [1pF-10pF] 0x1: Dual TL Length= [20cm-40cm] / Farend cap per TL= [1pF-10pF] 0x2: TL Length = [2cm-20cm] / Farend cap per TL= [10pF-20pF] 0x3: Dual TL Length = [20cm-40cm] / Farend cap per TL= [10pF-20pF]	RW	0x0
23:22	HDQ_DR0_LB	Load control for group hdq_dr0 0x0: TL Length= [2cm-20cm] / Farend cap per TL= [1pF-10pF] 0x1: Dual TL Length= [20cm-40cm] / Farend cap per TL= [1pF-10pF] 0x2: TL Length = [2cm-20cm] / Farend cap per TL= [10pF-20pF] 0x3: Dual TL Length = [20cm-40cm] / Farend cap per TL= [10pF-20pF]	RW	0x0
21:0	RESERVED		R	0x000000

(1) Far-end load is equivalent to CLoad, where CLoad is the total capacitance seen at the far end of the transmission line.

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Table 18-595. Register Call Summary for Register CONTROL_SMART1IO_PADCONF_3

Control Module Functional Description

- Signal Integrity Parameter Control Registers With Pad Group Assignment: [0] [1] [2] [3] [4] [5]

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- SYSCTRL_PADCONF_CORE Register Summary: [6]

Table 18-596. CONTROL_C2CIO_PADCONF_0

Address Offset	0x0000 05D8		
Physical Address	0x4A10 05D8	**Instance**	SYSCTRL_PADCONF_CORE
Description	C2C IO control 0 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2C_DR0_LB0	C2C_DR1_LB0	C2C_DR2_LB0	GPIO_DR0_LB0	GPIO_DR1_LB0	GPIO_DR2_LB0	GPMC_DR0_LB0	GPMC_DR11_LB0	GPMC_DR10_LB0	GPMC_DR2_LB0	GPMC_DR4_LB0	GPMC_DR5_LB0	GPMC_DR6_LB0	GPMC_DR7_LB0	GPMC_DR8_LB0	GPMC_DR9_LB0	KPD_DR4_LB0	KPD_DR5_LB0	SDMMC2_DR0_LB0	CMOSEN_C2C_0_FRM_CTRL	CMOSEN_C2C_1_FRM_CTRL	C2C_VREF_CCAP	C2C_INT_VREF_EN	C2C_INT_VREF_AUTO_EN	RESERVED						

Bits	Field Name	Description	Type	Reset
31	C2C_DR0_LB0	Mode selection bit for group c2c_dr0_LB0 0x0: sdmmc2 1.2V and 1.8V / gpmc 1.2V 0x1: c2c 1.2V and 1.8V / gpmc 1.8V	RW	0
30	C2C_DR1_LB0	Mode selection bit for group c2c_dr1_LB0 0x0: sdmmc2 1.2V and 1.8V / gpmc 1.2V 0x1: c2c 1.2V and 1.8V / gpmc 1.8V	RW	0
29	C2C_DR2_LB0	Mode selection bit for group c2c_dr2_LB0 0x0: sdmmc2 1.2V and 1.8V / gpmc 1.2V 0x1: c2c 1.2V and 1.8V / gpmc 1.8V	RW	0
28	GPIO_DR0_LB0	Mode selection bit for group gpio_dr0_LB0 0x0: sdmmc2 1.2V and 1.8V / gpmc 1.2V 0x1: c2c 1.2V and 1.8V / gpmc 1.8V	RW	0
27	GPIO_DR1_LB0	Mode selection bit for group gpio_dr1_LB0 0x0: sdmmc2 1.2V and 1.8V / gpmc 1.2V 0x1: c2c 1.2V and 1.8V / gpmc 1.8V	RW	0
26	GPIO_DR2_LB0	Mode selection bit for group gpio_dr2_LB0 0x0: sdmmc2 1.2V and 1.8V / gpmc 1.2V 0x1: c2c 1.2V and 1.8V / gpmc 1.8V	RW	0
25	GPMC_DR0_LB0	Mode selection bit for group gpmc_dr0_LB0 0x0: sdmmc2 1.2V and 1.8V / gpmc 1.2V 0x1: c2c 1.2V and 1.8V / gpmc 1.8V	RW	0
24	GPMC_DR11_LB0	Mode selection bit for group gpmc_dr11_LB0 0x0: sdmmc2 1.2V and 1.8V / gpmc 1.2V 0x1: c2c 1.2V and 1.8V / gpmc 1.8V	RW	0

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Bits	Field Name	Description	Type	Reset
23	GPMC_DR10_LB0	Mode selection bit for group gpmc_dr10_LB0 0x0: sdmmc2 1.2V and 1.8V / gpmc 1.2V 0x1: c2c 1.2V and 1.8V / gpmc 1.8V	RW	0
22	GPMC_DR2_LB0	Mode selection bit for group gpmc_dr2_LB0 0x0: sdmmc2 1.2V and 1.8V / gpmc 1.2V 0x1: c2c 1.2V and 1.8V / gpmc 1.8V	RW	0
21	GPMC_DR4_LB0	Mode selection bit for group gpmc_dr4_LB0 0x0: sdmmc2 1.2V and 1.8V / gpmc 1.2V 0x1: c2c 1.2V and 1.8V / gpmc 1.8V	RW	0
20	GPMC_DR5_LB0	Mode selection bit for group gpmc_dr5_LB0 0x0: sdmmc2 1.2V and 1.8V / gpmc 1.2V 0x1: c2c 1.2V and 1.8V / gpmc 1.8V	RW	0
19	GPMC_DR6_LB0	Mode selection bit for group gpmc_dr6_LB0 0x0: sdmmc2 1.2V and 1.8V / gpmc 1.2V 0x1: c2c 1.2V and 1.8V / gpmc 1.8V	RW	0
18	GPMC_DR7_LB0	Mode selection bit for group gpmc_dr7_LB0 0x0: sdmmc2 1.2V and 1.8V / gpmc 1.2V 0x1: c2c 1.2V and 1.8V / gpmc 1.8V	RW	0
17	GPMC_DR8_LB0	Mode selection bit for group gpmc_dr8_LB0 0x0: sdmmc2 1.2V and 1.8V / gpmc 1.2V 0x1: c2c 1.2V and 1.8V / gpmc 1.8V	RW	0
16	GPMC_DR9_LB0	Mode selection bit for group gpmc_dr9_LB0 0x0: sdmmc2 1.2V and 1.8V / gpmc 1.2V 0x1: c2c 1.2V and 1.8V / gpmc 1.8V	RW	0
15	KPD_DR4_LB0	Mode selection bit for group kpd_dr4_LB0 0x0: sdmmc2 1.2V and 1.8V / gpmc 1.2V 0x1: c2c 1.2V and 1.8V / gpmc 1.8V	RW	0
14	KPD_DR5_LB0	Mode selection bit for group kpd_dr5_LB0 0x0: sdmmc2 1.2V and 1.8V / gpmc 1.2V 0x1: c2c 1.2V and 1.8V / gpmc 1.8V	RW	0
13	SDMMC2_DR0_LB0	Mode selection bit for group sdmmc2_dr0_LB0 0x0: sdmmc2 1.2V and 1.8V / gpmc 1.2V 0x1: c2c 1.2V and 1.8V / gpmc 1.8V	RW	0
12	CMOSEN_C2C_0_FRM_CTRL	lvcmos receiver enable in 1.2V mode for group c2c_0 0x0: lvcmos rx disable 0x1: lvcmos rx enable	RW	1
11	CMOSEN_C2C_1_FRM_CTRL	lvcmos receiver enable in 1.2V mode for group c2c_1 0x0: lvcmos rx disable 0x1: lvcmos rx enable	RW	1
10:9	C2C_VREF_CCAP	Selection for coupling cap connection on ivref pad 0x0: No capacitor connected 0x1: Capacitor between BIAS2 and VSS 0x3: Capacitor between BIAS2 and VDDS as well as BIAS2 and VSS 0x2: Capacitor between BIAS2 and VDDS	RW	0x1
8	C2C_INT_VREF_EN	Internal VREF enable for C2C pads in manual mode (if both manual and auto mode is enabled then manual mode takes the priority) 0x0: Disabled 0x1: Enabled	RW	1

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Bits	Field Name	Description	Type	Reset
7	C2C_INT_VREF_AUTO_EN	Internal VREF enable for C2C pads in auto mode (if both manual and auto mode is enabled then manual mode takes the priority) 0x0: Disabled 0x1: Enabled	RW	1
6:0	RESERVED		R	0x00

Table 18-597. Register Call Summary for Register CONTROL_C2CIO_PADCONF_0

Control Module Functional Description

- Device Core Control Module Instance: [0]
- Signal Integrity Parameter Control Registers With Pad Group Assignment: [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23] [24] [25] [26] [27] [28]

Control Module Register Manual

- SYSCTRL_PADCONF_CORE Register Summary: [29]

Table 18-598. CONTROL_PBIASLITE

Address Offset	0x0000 0600		
Physical Address	0x4A10 0600	**Instance**	SYSCTRL_PADCONF_CORE
Description	PBIASLITE control Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PBIASLITE1_HIZ_MODE	PBIASLITE1_SUPPLY_HI_OUT	PBIASLITE1_VMODE_ERROR	PBIASLITE1_PWRDNZ	PBIASLITE1_VMODE	MMC1_PWRDNZ	MMC1_PBIASLITE_HIZ_MODE	MMC1_PBIASLITE_SUPPLY_HI_OUT	MMC1_PBIASLITE_VMODE_ERROR	MMC1_PBIASLITE_PWRDNZ	MMC1_PBIASLITE_VMODE	USBC1_ICUSB_PWRDNZ	RESERVED																			

Bits	Field Name	Description	Type	Reset
31	PBIASLITE1_HIZ_MODE	HIZ MODE of the PBIASLITE1 0x0: PBIAS1 is in normal operation mode. 0x1: PBIAS1 output is in high-impedance state.	RW	0
30	PBIASLITE1_SUPPLY_HI_OUT	SUPPLY_HI_OUT from PBIASLITE1 Read 0x0: SIM_VDDS = 1.8 V Read 0x1: SIM_VDDS = 3 V	R	0
29	PBIASLITE1_VMODE_ERROR	VMODE ERROR from PBIASLITE1 Read 0x0: VMODE level is the same as SUPPLY_HI_OUT. Read 0x1: VMODE level is not the same as SUPPLY_HI_OUT.	R	0

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Bits	Field Name	Description	Type	Reset
28	PBIASLITE1_PWRDNZ	PWRDNZ control to PBIASLITE1 This bit is used to protect the PBIAS1 cell (associated with the gpio_wk0-gpio_wk2 pads I/O cell) when SIM_VDDS is not stable. 0x0: Software must clear this bit when SIM_VDDS changes. 0x1: Software must set this bit only when SIM_VDDS is stable.	RW	0
27	PBIASLITE1_VMODE	VMODE control to PBIASLITE1 0x0: SIM_VDDS = 1.8 V 0x1: SIM_VDDS = 3 V	RW	1
26	MMC1_PWRDNZ	PWRDNZ control to MMC1 IO This bit is used to protect the MMC1 I/O cell when MMC1_VDDS is not stable. 0x0: Software must clear this bit when MMC1_VDDS changes. 0x1: Software must set this bit only when MMC1_VDDS is stable.	RW	0
25	MMC1_PBIASLITE_HIZ_MODE	HIZ_MODE from MMC1 PBIASLITE 0x0: PBIAS in normal operation mode 0x1: PBIAS output is in high impedence state	RW	0
24	MMC1_PBIASLITE_SUPPLY_HI_OUT	SUPPLY_HI_OUT from MMC1 PBIASLITE Read 0x0: MMC1_VDDS = 1.8V Read 0x1: MMC1_VDDS = 3V	R	0
23	MMC1_PBIASLITE_VMODE_ERROR	VMODE ERROR from MMC1 PBIASLITE Read 0x0: VMODE level is same as SUPPLY_HI_OUT Read 0x1: VMODE level is not same as SUPPLY_HI_OUT	R	0
22	MMC1_PBIASLITE_PWRDNZ	PWRDNZ control to MMC1 PBIASLITE This bit is used to protect the MMC1_PBIAS cell (MMC1 I/O cell associated) when MMC1_VDDS is not stable. 0x0: Software must clear this bit when MMC1_VDDS changes. 0x1: Software must set this bit only when MMC1_VDDS is stable.	RW	0
21	MMC1_PBIASLITE_VMODE	VMODE control to MMC1 PBIASLITE 0x0: MMC1_VDDS = 1.8V 0x1: MMC1_VDDS = 3V	RW	1
20	USBC1_ICUSB_PWRDNZ	PWRDNZ control to USBC1 IO This bit is used to protect the USBC1_ICUSB I/O cell when SIM_VDDS is not stable. 0x0: Software must clear this bit when SIM_VDDS changes. 0x1: Software must set this bit only when SIM_VDDS is stable.	RW	0
19:0	RESERVED		R	0x00000

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Table 18-599. Register Call Summary for Register CONTROL_PBIASLITE

Control Module Functional Description

- Extended-Drain I/O and PBIAS Cell: [0] [1]
- PBIAS Cell: [2] [3]
- Extended-Drain I/O: [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18]
- PBIAS Error Generation: [19] [20] [21]
- DSP Boot Register: [22] [23]
- Signal Integrity Parameter Control Registers With Pad Group Assignment: [24]

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- Operational Modes Configuration: [25] [26] [27] [28] [29] [30] [31] [32] [33] [34] [35] [36] [37] [38] [39] [40] [41] [42] [43] [44]

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- SYSCTRL_PADCONF_CORE Register Summary: [45]

Table 18-600. CONTROL_I2C_0

Address Offset	0x0000 0604		
Physical Address	0x4A10 0604	**Instance**	SYSCTRL_PADCONF_CORE
Description	I2C pads control 0 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I2C4_SDA_GLFENB	I2C4_SDA_LOAD_BITS		I2C4_SDA_PULLUPRESX	I2C3_SDA_GLFENB	I2C3_SDA_LOAD_BITS		I2C3_SDA_PULLUPRESX	I2C2_SDA_GLFENB	I2C2_SDA_LOAD_BITS		I2C2_SDA_PULLUPRESX	I2C1_SDA_GLFENB	I2C1_SDA_LOAD_BITS		I2C1_SDA_PULLUPRESX	I2C4_SCL_GLFENB	I2C4_SCL_LOAD_BITS		I2C4_SCL_PULLUPRESX	I2C3_SCL_GLFENB	I2C3_SCL_LOAD_BITS		I2C3_SCL_PULLUPRESX	I2C2_SCL_GLFENB	I2C2_SCL_LOAD_BITS		I2C2_SCL_PULLUPRESX	I2C1_SCL_GLFENB	I2C1_SCL_LOAD_BITS		I2C1_SCL_PULLUPRESX

Bits	Field Name	Description	Type	Reset
31	I2C4_SDA_GLFENB	Active_high glitch free operation enable pin for i2c4 receiver 0x0: Disable i2c4 glitch free operation 0x1: Enable i2c4 glitch free operation	RW	0
30:29	I2C4_SDA_LOAD_BITS	Internal Pull up resistor in Fast or Standard mode / High_speed mode for i2c4 0x0: 4.5 kΩ (5-15 pF) / 1.66 kΩ (5-12 pF) 0x1: 2.1 kΩ (15-50 pF) / 920 Ω (12-25 pF) 0x2: 860 Ω (50-150 pF) / 500 Ω (25-50 pF) 0x3: N.A / 300 Ω (50-80 pF)	RW	0x1
28	I2C4_SDA_PULLUPRESX	Active_low internal pull_up resistor enabled for i2c4 0x0: Enable Internal Pull up resistor 0x1: Disable Internal Pull up resisitor	RW	0
27	I2C3_SDA_GLFENB	Active_high glitch free operation enable pin for i2c3 receiver 0x0: Disable i2c4 glitch free operation 0x1: Enable i2c4 glitch free operation	RW	0

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Bits	Field Name	Description	Type	Reset
26:25	I2C3_SDA_LOAD_BITS	Internal Pull up resistor in Fast or Standard mode / High_speed mode for i2c3 0x0: 4.5 kΩ (5-15 pF) / 1.66 kΩ (5-12 pF) 0x1: 2.1 kΩ (15-50 pF) / 920 Ω (12-25 pF) 0x2: 860 Ω (50-150 pF) / 500 Ω (25-50 pF) 0x3: N.A / 300 Ω (50-80 pF)	RW	0x1
24	I2C3_SDA_PULLUPRESX	Active_low internal pull_up resistor enabled for i2c3 0x0: Enable Internal Pull up resistor 0x1: Disable Internal Pull up resisitor	RW	0
23	I2C2_SDA_GLFENB	Active_high glitch free operation enable pin for i2c2 receiver 0x0: Disable i2c4 glitch free operation 0x1: Enable i2c4 glitch free operation	RW	0
22:21	I2C2_SDA_LOAD_BITS	Internal Pull up resistor in Fast or Standard mode / High_speed mode for i2c2 0x0: 4.5 kΩ (5-15 pF) / 1.66 kΩ (5-12 pF) 0x1: 2.1 kΩ (15-50 pF) / 920 Ω (12-25 pF) 0x2: 860 Ω (50-150 pF) / 500 Ω (25-50 pF) 0x3: N.A / 300 Ω (50-80 pF)	RW	0x1
20	I2C2_SDA_PULLUPRESX	Active_low internal pull_up resistor enabled for i2c2 0x0: Enable Internal Pull up resistor 0x1: Disable Internal Pull up resisitor	RW	0
19	I2C1_SDA_GLFENB	Active_high glitch free operation enable pin for i2c1 receiver 0x0: Disable i2c4 glitch free operation 0x1: Enable i2c4 glitch free operation	RW	0
18:17	I2C1_SDA_LOAD_BITS	Internal Pull up resistor in Fast or Standard mode / High_speed mode for i2c1 0x0: 4.5 kΩ (5-15 pF) / 1.66 kΩ (5-12 pF) 0x1: 2.1 kΩ (15-50 pF) / 920 Ω (12-25 pF) 0x2: 860 Ω (50-150 pF) / 500 Ω (25-50 pF) 0x3: N.A / 300 Ω (50-80 pF)	RW	0x2
16	I2C1_SDA_PULLUPRESX	Active_low internal pull_up resistor enabled for i2c1 0x0: Enable Internal Pull up resistor 0x1: Disable Internal Pull up resisitor	RW	0
15	I2C4_SCL_GLFENB	Active_high glitch free operation enable pin for i2c4 receiver 0x0: Disable i2c4 glitch free operation 0x1: Enable i2c4 glitch free operation	RW	0
14:13	I2C4_SCL_LOAD_BITS	Internal Pull up resistor in Fast or Standard mode / High_speed mode for i2c4 0x0: 4.5 kΩ (5-15 pF) / 1.66 kΩ (5-12 pF) 0x1: 2.1 kΩ (15-50 pF) / 920 Ω (12-25 pF) 0x2: 860 Ω (50-150 pF) / 500 Ω (25-50 pF) 0x3: N.A / 300 Ω (50-80 pF)	RW	0x1
12	I2C4_SCL_PULLUPRESX	Active_low internal pull_up resistor enabled for i2c4 0x0: Enable Internal Pull up resistor 0x1: Disable Internal Pull up resisitor	RW	0
11	I2C3_SCL_GLFENB	Active_high glitch free operation enable pin for i2c3 receiver 0x0: Disable i2c4 glitch free operation 0x1: Enable i2c4 glitch free operation	RW	0

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Bits	Field Name	Description	Type	Reset
10:9	I2C3_SCL_LOAD_BITS	Internal Pull up resistor in Fast or Standard mode / High_speed mode for i2c3 0x0: 4.5 kΩ (5-15 pF) / 1.66 kΩ (5-12 pF) 0x1: 2.1 kΩ (15-50 pF) / 920 Ω (12-25 pF) 0x2: 860 Ω (50-150 pF) / 500 Ω (25-50 pF) 0x3: N.A / 300 Ω (50-80 pF)	RW	0x1
8	I2C3_SCL_PULLUPRESX	Active_low internal pull_up resistor enabled for i2c3 0x0: Enable Internal Pull up resistor 0x1: Disable Internal Pull up resisitor	RW	0
7	I2C2_SCL_GLFENB	Active_high glitch free operation enable pin for i2c2 receiver 0x0: Disable i2c4 glitch free operation 0x1: Enable i2c4 glitch free operation	RW	0
6:5	I2C2_SCL_LOAD_BITS	Internal Pull up resistor in Fast or Standard mode / High_speed mode for i2c2 0x0: 4.5 kΩ (5-15 pF) / 1.66 kΩ (5-12 pF) 0x1: 2.1 kΩ (15-50 pF) / 920 Ω (12-25 pF) 0x2: 860 Ω (50-150 pF) / 500 Ω (25-50 pF) 0x3: N.A / 300 Ω (50-80 pF)	RW	0x1
4	I2C2_SCL_PULLUPRESX	Active_low internal pull_up resistor enabled for i2c2 0x0: Enable Internal Pull up resistor 0x1: Disable Internal Pull up resisitor	RW	0
3	I2C1_SCL_GLFENB	Active_high glitch free operation enable pin for i2c1 receiver 0x0: Disable i2c4 glitch free operation 0x1: Enable i2c4 glitch free operation	RW	0
2:1	I2C1_SCL_LOAD_BITS	Internal Pull up resistor in Fast or Standard mode / High_speed mode for i2c1 0x0: 4.5 kΩ (5-15 pF) / 1.66 kΩ (5-12 pF) 0x1: 2.1 kΩ (15-50 pF) / 920 Ω (12-25 pF) 0x2: 860 Ω (50-150 pF) / 500 Ω (25-50 pF) 0x3: N.A / 300 Ω (50-80 pF)	RW	0x2
0	I2C1_SCL_PULLUPRESX	Active_low internal pull_up resistor enabled for i2c1 0x0: Enable Internal Pull up resistor 0x1: Disable Internal Pull up resisitor	RW	0

Table 18-601. Register Call Summary for Register CONTROL_I2C_0

Control Module Functional Description

- Signal Integrity Parameter Control Registers With Pad Group Assignment: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23] [24]

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- SYSCTRL_PADCONF_CORE Register Summary: [25]

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Table 18-602. CONTROL_CAMERA_RX

Address Offset	0x0000 0608		
Physical Address	0x4A10 0608	**Instance**	SYSCTRL_PADCONF_CORE
Description	CAMERA RX control Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	CAMERARX_CSI22_LANEENABLE				CAMERARX_CSI21_LANEENABLE			RESERVED		CAMERARX_CSI22_CTRLCLKEN	CAMERARX_CSI22_CAMMODE		CAMERARX_CSI21_CTRLCLKEN	CAMERARX_CSI21_CAMMODE		RESERVED															

Bits	Field Name	Description	Type	Reset
31	CAMERARX_CSI22_LANEENABLE2	CSI22 CAMERARX lane 2 enable (CSI22_DX2, CSI22_DY2) 0x0: Lane module disabled 0x1: Lane module enabled	RW	0x0
30	CAMERARX_CSI22_LANEENABLE1	CSI22 CAMERARX lane 1 enable (CSI22_DX1, CSI22_DY1) 0x0: Lane module disabled 0x1: Lane module enabled	RW	0x0
29	CAMERARX_CSI22_LANEENABLE0	CSI22 CAMERARX lane 0 enable (CSI22_DX0, CSI22_DY0) 0x0: Lane module disabled 0x1: Lane module enabled	RW	0x0
28	CAMERARX_CSI21_LANEENABLE4	CSI21 CAMERARX lane 4 enable (CSI21_DX4, CSI21_DY4) 0x0: Lane module disabled 0x1: Lane module enabled	RW	0X0
27	CAMERARX_CSI21_LANEENABLE3	CSI21 CAMERARX lane 3 enable (CSI21_DX3, CSI21_DY3) 0x0: Lane module disabled 0x1: Lane module enabled	RW	0X0
26	CAMERARX_CSI21_LANEENABLE2	CSI21 CAMERARX lane 2 enable (CSI21_DX2, CSI21_DY2) 0x0: Lane module disabled 0x1: Lane module enabled	RW	0X0
25	CAMERARX_CSI21_LANEENABLE1	CSI21 CAMERARX lane 1 enable (CSI21_DX1, CSI21_DY1) 0x0: Lane module disabled 0x1: Lane module enabled	RW	0X0
24	CAMERARX_CSI21_LANEENABLE0	CSI21 CAMERARX lane 0 enable (CSI21_DX0, CSI21_DY0) 0x0: Lane module disabled 0x1: Lane module enabled	RW	0X0

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Bits	Field Name	Description	Type	Reset
23:22	RESERVED		R	0x0
21	CAMERARX_CSI22_CTRLCLKEN	CSI22 CAMERARX clock enable control 0x0: Disable for CTRLCLK 0x1: Active high enable for CTRLCLK	RW	0
20:19	CAMERARX_CSI22_CAMMODE	CSI22 CAMERARX CAMMODE control 0x0: DPHY mode (CSI2 mode) 0x1: Data/Strobe Transmission Format (CCP2 mode) 0x2: Data/Clock Transmission Format (CCP2/CSI1 mode) 0x3: GPI mode (Parallel interface mode)	RW	0x3
18	CAMERARX_CSI21_CTRLCLKEN	CSI21 CAMERARX clock enable control 0x0: Disable for CTRLCLK 0x1: Active high enable for CTRLCLK	RW	0
17:16	CAMERARX_CSI21_CAMMODE	CSI21 CAMERARX CAMMODE control 0x0: DPHY mode (CSI2 mode) 0x1: Data/Strobe Transmission Format (CCP2 mode) 0x2: Data/Clock Transmission Format (CCP2/CSI1 mode) 0x3: GPI mode (Parallel interface mode)	RW	0x3
15:0	RESERVED		R	0x0000

Table 18-603. Register Call Summary for Register CONTROL_CAMERA_RX

Control Module Functional Description
- Temperature Sensor Control Registers: [0] [1]

Control Module Register Manual
- SYSCTRL_PADCONF_CORE Register Summary: [2]

Table 18-604. CONTROL_AVDAC

Address Offset	0x0000 060C		
Physical Address	0x4A10 060C	**Instance**	SYSCTRL_PADCONF_CORE
Description	AVDAC control Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AVDAC_ACEN	AVDAC_TVOUTBYPASS	AVDAC_INPUTINV	RESERVED																RESERVED					RESERVED							

Bits	Field Name	Description	Type	Reset
31	AVDAC_ACEN	AC coupling enable 0x0: AC coupling disable 0x1: AC coupling enable	RW	0

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Bits	Field Name	Description	Type	Reset
30	AVDAC_TVOUTBYPASS	TV OUT bypass signal 0x0: Video buffer is not bypassed 0x1: Video buffer is bypassed	RW	0
29	AVDAC_INPUTINV	Inversion control for DAC input data – din[9:0] 0x0: Data inversion is disabled. 0x1: Data inversion is enabled.	RW	0
28:13	RESERVED		RW	0x0000
12	RESERVED		RW (Write 1 to Clear)	0
11:0	RESERVED		R	0x000

Table 18-605. Register Call Summary for Register CONTROL_AVDAC

Control Module Programming Guide • Operational Modes Configuration: [0] [1]
Control Module Register Manual • SYSCTRL_PADCONF_CORE Register Summary: [2]

Table 18-606. CONTROL_MMC2

Address Offset	0x0000 0614		
Physical Address	0x4A10 0614	**Instance**	SYSCTRL_PADCONF_CORE
Description	MMC2 control Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MMC2_FEEDBACK_CLK_SEL	RESERVED																														

Bits	Field Name	Description	Type	Reset
31	MMC2_FEEDBACK_CLK_SEL	Feed_back clock select 0x0: Clock feed_back at PAD level 0x1: Clock feed_back at board level	RW	0
30:0	RESERVED		R	0x0000 0000

Table 18-607. Register Call Summary for Register CONTROL_MMC2

Control Module Register Manual • SYSCTRL_PADCONF_CORE Register Summary: [0]

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Table 18-608. CONTROL_DSIPHY

Address Offset	0x0000 0618		
Physical Address	0x4A10 0618	**Instance**	SYSCTRL_PADCONF_CORE
Description	DSIPHY control Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DSI2_LANEENABLE			DSI1_LANEENABLE					DSI2_PIPD								DSI1_PIPD								RESERVED							

Bits	Field Name	Description	Type	Reset
31:29	DSI2_LANEENABLE	DSI2 Lane Enable For each bit, the following settings are valid: 0x0: Lane module disabled 0x1: Lane module enabled [31] DSI2 lane 2 enable [30] DSI2 lane 1 enable [29] DSI2 lane 0 enable	RW	0x0
28:24	DSI1_LANEENABLE	DSI1 Lane Enable For each bit, the following settings are valid: 0x0: Lane module disabled 0x1: Lane module enabled [28] DSI1 lane 4 enable [27] DSI1 lane 3 enable [26] DSI1 lane 2 enable [25] DSI1 lane 1 enable [24] DSI1 lane 0 enable	RW	0x00
23:19	DSI2_PIPD	DSI2 PD Enable For each bit, the following settings are valid: 0x0: Pull down enabled 0x1: Pull down disabled [23] RESERVED (Unused) [22] RESERVED (Unused) [21] DSI2 lane 2 PD enable [20] DSI2 lane 1 PD enable [19] DSI2 lane 0 PD enable	RW	0x00
18:14	DSI1_PIPD	DSI1 PD Enable For each bit, the following settings are valid: 0x0: Pull down enabled 0x1: Pull down disabled [18]] DSI1 lane 4 PD enable [17]] DSI1 lane 3 PD enable [16]] DSI1 lane 2 PD enable [15]] DSI1 lane 1 PD enable [14]] DSI1 lane 0 PD enable	RW	0x00
13:0	RESERVED		R	0x0000

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Table 18-609. Register Call Summary for Register CONTROL_DSIPHY

Control Module Register Manual

- SYSCTRL_PADCONF_CORE Register Summary: [0]

Table 18-610. CONTROL_MCBSPLP

Address Offset	0x0000 061C		
Physical Address	0x4A10 061C	**Instance**	SYSCTRL_PADCONF_CORE
Description	McBSPLP control Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ALBCTRLRX_FSX	ALBCTRLRX_CLKX	RESERVED																													

Bits	Field Name	Description	Type	Reset
31	ALBCTRLRX_FSX	Analog loop_back control for FSX. This bit is programmable for only the McBSP4 instance. For the remaining three McBSP instances, this bit is hardwired to 1. 0x0: PIFSR is used 0x1: PIFSX is used instead of PIFSR 4pin mode	RW	0
30	ALBCTRLRX_CLKX	Analog loop_back control for CLKX. This bit is programmable for only the McBSP4 instance. For the remaining three McBSP instances, this bit is hardwired to 1. 0x0: PICLKR is used 0x1: PICLKX is used instead of PICLKR 4pin mode	RW	0
29:0	RESERVED		R	0x0000 0000

Table 18-611. Register Call Summary for Register CONTROL_MCBSPLP

Control Module Register Manual

- SYSCTRL_PADCONF_CORE Register Summary: [0]

Table 18-612. CONTROL_USB2PHYCORE

Address Offset	0x0000 0620		
Physical Address	0x4A10 0620	**Instance**	SYSCTRL_PADCONF_CORE
Description	USB2PHYCORE control Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
USB2PHY_AUTORESUME_EN	USB2PHY_DISCHGDET	USB2PHY_GPIOMODE	USB2PHY_CHG_DET_EXT_CTL	USB2PHY_RDM_PD_CHGDET_EN	USB2PHY_RDP_PU_CHGDET_EN	USB2PHY_CHG_VSRC_EN	USB2PHY_CHG_ISINK_EN	USB2PHY_CHG_DET_STATUS			USB2PHY_CHG_DET_DM_COMP	USB2PHY_CHG_DET_DP_COMP	USB2PHY_DATADET	USB2PHY_SINKONDP	USB2PHY_SRCONDM	USB2PHY_RESTARTCHGDET	USB2PHY_CHGDETDONE	USB2PHY_CHGDETECTED	USB2PHY_MCPCPUEN	USB2PHY_MCPCMODEEN	RESERVED	USB2PHY_UTMIRESETDONE	USB2PHY_TXBITSTUFFENABLE	USB2PHY_DATAPOLARITYN	USBDPLL_FREQLOCK	USB2PHY_RESETDONETCLK	RESERVED				
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0x1			R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0				

Bits	Field Name	Description	Type	Reset
31	USB2PHY_AUTORESUME_EN	Auto resume enable 0x0: Disable autoresume 0x1: Enable autoresume	RW	0
30	USB2PHY_DISCHGDET	Disable charger detect 0x0: Charger detect function enabled 0x1: Charger detect function disabled	RW	0x0
29	USB2PHY_GPIOMODE(1)	GPIO mode 0x0: USB mode enabled 0x1: GPIO mode enabled	RW	0
28	USB2PHY_CHG_DET_EXT_CTL	Charge detect external control 0x0: Charger detect internal state-machine used 0x1: Charge detect state-machine is bypassed	RW	0
27	USB2PHY_RDM_PD_CHGDET_EN	DM Pull down control 0x0: PD disabled 0x1: PD enabled	RW	0
26	USB2PHY_RDP_PU_CHGDET_EN	DP Pull up control 0x0: PU disabled 0x1: PU enabled	RW	0
25	USB2PHY_CHG_VSRC_EN	VSRC enable on DP line-Host charger case 0x0: Disable VSRC drive on DP 0x1: Drives VSRC 600 mV on DP line	RW	0
24	USB2PHY_CHG_ISINK_EN	ISINK enable on DM line-Host charger case 0x0: Disable the ISINK on DM 0x1: Enables the ISINK (100 A) on DM line	RW	0
23:21	USB2PHY_CHG_DET_STATUS	Status of charger detection Read 0x0: Wait state Read 0x1: No contact Read 0x2: PS/2 Read 0x3: Unknown error Read 0x4: Dedicated charger Read 0x5: HOST charger Read 0x6: PC Read 0x7: Interrupt	R	0x1

(1) When USBA0_OTG_DP_MUXMODE = 0 and USBA0_OTG_DM_MUXMODE = 0, user software must ensure that CONTROL_USB2PHYCORE[29] USB2PHY_GPIOMODE = 0. When USBA0_OTG_DP_MUXMODE is different than 0 and USBA0_OTG_DM_MUXMODE is different than 0, user software must ensure that CONTROL_USB2PHYCORE[29] USB2PHY_GPIOMODE = 1.

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Bits	Field Name	Description	Type	Reset
20	USB2PHY_CHG_DET_DM_COMP	Output of the comparator on DM during the resistor host detect protocol Read 0x0: DM line is below 0.75V to 0.95V Read 0x1: DM line is above 0.75V to 0.95V	R	0
19	USB2PHY_CHG_DET_DP_COMP	Output of the comparator on DP during the resistor host detect protocol Read 0x0: DP line is below 0.75V to 0.95V Read 0x1: DP line is above 0.75V to 0.95V	R	0X1
18	USB2PHY_DATADET	Output of the charger detect comparator Read 0x0: DM line is below 0.25V to 0.4V Read 0x1: DM line is above 0.25V to 0.4V	R	0
17	USB2PHY_SINKONDP	When 1 current sink is connected to DP instead of DM 0x0: Default value 0x1: Enables the ISINK on DP instead of DM	RW	0
16	USB2PHY_SRCONDM	When 1 voltage source is connected to DP instead of DM 0x0: Default value 0x1: Enable the VSRC on DM instead of DP	RW	0
15	USB2PHY_RESTARTCHGDET	restartchgdet = 1 for 1 msec cause the CD_START to reset 0x0: Default value 0x1: A high pulse of 1 msec causes the charger detect to restart on negative edge of restartchgdet	RW	0
14	USB2PHY_CHGDETDONE	Status indicates that charger detection protocol is over Read 0x0: Charger detection protocol is not over Read 0x1: Charger detection protocol is over	R	0
13	USB2PHY_CHGDETECTED	Output of the charger detection protocol Read 0x0: Charger not detected Read 0x1: Charger detected	R	0
12	USB2PHY_MCPCPUEN	MCPC Pull up enable 0x0: Disable the MCPC pull up 0x1: Enable the 4.7K to10K pull up on receive line DP when datapolarityn is 0 and DM when datapolarityn is 1	RW	0
11	USB2PHY_MCPCMODEEN	MCPC Mode enable 0x0: Disable MCPC mode 0x1: Enable MCPC mode	RW	0
10	RESERVED	Read returns reset value	R	0
9	USB2PHY_UTMIRESETDONE	UTMI FSM reset status Read 0x0: UTMI FSMs are in reset Read 0x1: UTMI FSMs are out of reset	R	0
8	USB2PHY_TXBITSTUFFENABLE	TX data bit stuff enable 0x0: DATAOUT [7 0x1: DATAOUT [7	RW	0
7	USB2PHY_DATAPOLARITYN	Data polarity 0x0: DP functionality is on DP and DM funcationality is on DM 0x1: DP functionality is on DM and DM functionality is on DP	RW	0
6	USBDPLL_FREQLOCK	Status from USB DPLL	R	0
5	USB2PHY_RESETDONETCLK	resetdonetclk status from USB2PHY	R	0
4:0	RESERVED		R	0x00

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Table 18-613. Register Call Summary for Register CONTROL_USB2PHYCORE

Control Module Register Manual

- SYSCTRL_PADCONF_CORE Register Summary: [0]

Table 18-614. CONTROL_MMC1

Address Offset	0x0000 0628		
Physical Address	0x4A10 0628	**Instance**	SYSCTRL_PADCONF_CORE
Description	MMC1 control Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SDMMC1_PUSTRENGTH_GRP0	SDMMC1_PUSTRENGTH_GRP1	SDMMC1_PUSTRENGTH_GRP2	SDMMC1_PUSTRENGTH_GRP3	SDMMC1_DR0_SPEEDCTRL	SDMMC1_DR1_SPEEDCTRL	SDMMC1_DR2_SPEEDCTRL	USBC1_DR0_SPEEDCTRL	USB_FD_CDEN	USBC1_ICUSB_DP_PDDIS	USBC1_ICUSB_DM_PDDIS	RESERVED																				

Bits	Field Name	Description	Type	Reset
31	SDMMC1_PUSTRENGTH_GRP0	Pullstrengh control for sdmmc1_pustrength_grp0 0x0: Pull up with 50 to 110 kΩ on MMC1 data pins 0x1: Pull up with 10 to 50 kΩ on MMC1 data pins	RW	1
30	SDMMC1_PUSTRENGTH_GRP1	Pullstrengh control for sdmmc1_pustrength_grp1 0x0: Pull up with 50 to 110 kΩ on MMC1 data pins 0x1: Pull up with 10 to 50 kΩ on MMC1 data pins	RW	0
29	SDMMC1_PUSTRENGTH_GRP2	Pullstrengh control for sdmmc1_pustrength_grp2 0x0: Pull up with 50 to 110 kΩ on MMC1 data pins 0x1: Pull up with 10 to 50 kΩ on MMC1 data pins	RW	1
28	SDMMC1_PUSTRENGTH_GRP3	Pullstrengh control for sdmmc1_pustrength_grp3 0x0: Pull up with 50 to 110 kΩ on MMC1 data pins 0x1: Pull up with 10 to 50 kΩ on MMC1 data pins	RW	1
27	SDMMC1_DR0_SPEEDCTRL	Speed control for group sdmmc1_dr0 0x0: FMAX = 26 MHz at 30 pF 0x1: FMAX = 65 MHz at 30 pF	RW	0
26	SDMMC1_DR1_SPEEDCTRL	Speed control for group sdmmc1_dr1 0x0: FMAX = 26 MHz at 30 pF 0x1: FMAX = 65 MHz at 30 pF	RW	0
25	SDMMC1_DR2_SPEEDCTRL	Speed control for group sdmmc1_dr2 0x0: FMAX = 26 MHz at 30 pF 0x1: FMAX = 65 MHz at 30 pF	RW	0
24	USBC1_DR0_SPEEDCTRL	Speed control for group usbc1_dr0 0x0: FMAX = 26 MHz at 30 pF 0x1: FMAX = 65 MHz at 30 pF	RW	0

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Bits	Field Name	Description	Type	Reset
23	USB_FD_CDEN	USB FD pull down select 0x0: select pull down from USB FD logic 0x1: select pull down from device control modules registers	RW	0
22	USBC1_ICUSB_DP_PDDIS	usbc1_icusb_dp pull down disable 0x0: usbc1_icusb_dp pull down disabled 0x1: usbc1_icusb_dp pull down enabled	RW	0
21	USBC1_ICUSB_DM_PDDIS	usbc1_icusb_dm pull dowm disable 0x0: usbc1_icusb_dm pull down disabled 0x1: usbc1_icusb_dm pull down enabled	RW	0
20:0	RESERVED		R	0x000000

Table 18-615. Register Call Summary for Register CONTROL_MMC1

Control Module Functional Description
- Extended-Drain I/O and PBIAS Cell: [0] [1]
- Extended-Drain I/O: [2] [3] [4] [5] [6] [7] [8] [9] [10]
- Signal Integrity Parameter Control Registers With Pad Group Assignment: [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23]

Control Module Programming Guide
- Operational Modes Configuration: [24] [25] [26] [27] [28] [29] [30] [31]

Control Module Register Manual
- SYSCTRL_PADCONF_CORE Register Summary: [32]

Table 18-616. CONTROL_HSI

Address Offset	0x0000 062C		
Physical Address	0x4A10 062C	**Instance**	SYSCTRL_PADCONF_CORE
Description	HSI control Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HSI1_CALLOOP_SEL	HSI1_CALMUX_SEL	HSI2_CALLOOP_SEL	HSI2_CALMUX_SEL	RESERVED																											

Bits	Field Name	Description	Type	Reset
31	HSI1_CALLOOP_SEL	hsi1 calibration loop select 0x0: Calibration mode 0x1: Enable Calibration mode	RW	0
30	HSI1_CALMUX_SEL	hsi1 calibration mux select 0x0: Calibration mode 0x1: Enable Calibration mode	RW	0
29	HSI2_CALLOOP_SEL	hsi2 calibration loop select 0x0: Calibration mode 0x1: Enable Calibration mode	RW	0

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Bits	Field Name	Description	Type	Reset
28	HSI2_CALMUX_SEL	hsi2 calibration mux select 0x0: Calibration mode 0x1: Enable Calibration mode	RW	0
27:0	RESERVED		R	0x0000000

Table 18-617. Register Call Summary for Register CONTROL_HSI

Control Module Register Manual
- SYSCTRL_PADCONF_CORE Register Summary: [0]

Table 18-618. CONTROL_USB

Address Offset	0x0000 0630		
Physical Address	0x4A10 0630	**Instance**	SYSCTRL_PADCONF_CORE
Description	USB control Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CARKIT_USBA0_ULPIPHY_DAT0_AUTO_EN	CARKIT_USBA0_ULPIPHY_DAT1_AUTO_EN	RESERVED																													

Bits	Field Name	Description	Type	Reset
31	CARKIT_USBA0_ULPIPHY_DAT0_AUTO_EN	carkit usba0 ulpiphy dat0 auto enable 0x0: Carkit Auto mode disabled 0x1: Carkit Auto mode enabled	RW	0
30	CARKIT_USBA0_ULPIPHY_DAT1_AUTO_EN	carkit usba0 ulpiphy dat1 auto enable 0x0: Carkit Auto mode disabled 0x1: Carkit Auto mode enabled	RW	0
29:0	RESERVED		R	0x0000 0000

Table 18-619. Register Call Summary for Register CONTROL_USB

Control Module Functional Description
- Signal Integrity Parameter Control Registers With Pad Group Assignment: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15]

Control Module Register Manual
- SYSCTRL_PADCONF_CORE Register Summary: [16]

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Table 18-620. CONTROL_HDQ

Address Offset	0x0000 0634		
Physical Address	0x4A10 0634	**Instance**	SYSCTRL_PADCONF_CORE
Description	HDQ control Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

Bits	Field Name	Description	Type	Reset
31:0	RESERVED		R	0x0000 0000

Table 18-621. Register Call Summary for Register CONTROL_HDQ

Control Module Register Manual

- SYSCTRL_PADCONF_CORE Register Summary: [0]

Table 18-622. CONTROL_LPDDR2IO1_0

Address Offset	0x0000 0638		
Physical Address	0x4A10 0638	**Instance**	SYSCTRL_PADCONF_CORE
Description	LPDDR2 1 I/O control 0 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LPDDR2IO1_GR4_SR		LPDDR2IO1_GR4_I			LPDDR2IO1_GR4_WD		RESERVED	LPDDR2IO1_GR3_SR		LPDDR2IO1_GR3_I			LPDDR2IO1_GR3_WD		RESERVED	LPDDR2IO1_GR2_SR		LPDDR2IO1_GR2_I			LPDDR2IO1_GR2_WD		RESERVED	LPDDR2IO1_GR1_SR		LPDDR2IO1_GR1_I			LPDDR2IO1_GR1_WD		RESERVED

Bits	Field Name	Description	Type	Reset
31:30	LPDDR2IO1_GR4_SR	Group 4 Slew Rate control sr1:sr0	RW	0x2
29:27	LPDDR2IO1_GR4_I	Group 4 Impedence control i2:i0 0x0: for Drv5 0x1: for Drv6 0x2: for Drv7 0x3: for Drv8 0x4: for Drv9 0x5: for Drv10 0x6: for Drv11 0x7: Drv12 (1)	RW	0x3
26:25	LPDDR2IO1_GR4_WD	Group 4 Weak driver control wd1:wd0 0x0: Pull logic disabled 0x1: pull up 0x2: pull down 0x3: Maintain the previous output value	RW	0x2

(1) To achieve the best LPDDR2IO performance, software must keep the impedance bit field at this value.

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Bits	Field Name	Description	Type	Reset
24	RESERVED		R	0
23:22	LPDDR2IO1_GR3_SR	Group 3 Slew Rate control sr1:sr0	RW	0x2
21:19	LPDDR2IO1_GR3_I	Group 3 Impedence control i2:i0 0x0: for Drv5 0x1: for Drv6 0x2: for Drv7 0x3: for Drv8 0x4: for Drv9 0x5: for Drv10 0x6: for Drv11 0x7: Drv12 (2)	RW	0x3
18:17	LPDDR2IO1_GR3_WD	Group 3 Weak driver control wd1:wd0 0x0: Pull logic disabled 0x1: pull up 0x2: pull down 0x3: Maintain the previous output value	RW	0x2
16	RESERVED		R	0
15:14	LPDDR2IO1_GR2_SR	Group 2 Slew Rate control sr1:sr0	RW	0x2
13:11	LPDDR2IO1_GR2_I	Group 2 Impedence control i2:i0 0x0: for Drv5 0x1: for Drv6 0x2: for Drv7 0x3: for Drv8 0x4: for Drv9 0x5: for Drv10 0x6: for Drv11 0x7: Drv12 (2)	RW	0x3
10:9	LPDDR2IO1_GR2_WD	Group 2 Weak driver control wd1:wd0 0x0: Pull logic disabled 0x1: pull up 0x2: pull down 0x3: Maintain the previous output value	RW	0x2
8	RESERVED		R	0
7:6	LPDDR2IO1_GR1_SR	Group 1 Slew Rate control sr1:sr0	RW	0x2
5:3	LPDDR2IO1_GR1_I	Group 1 Impedence control i2:i0 0x0: for Drv5 0x1: for Drv6 0x2: for Drv7 0x3: for Drv8 0x4: for Drv9 0x5: for Drv10 0x6: for Drv11 0x7: Drv12 (2)	RW	0x3
2:1	LPDDR2IO1_GR1_WD	Group 1 Weak driver control wd1:wd0 0x0: Pull logic disabled 0x1: pull up 0x2: pull down 0x3: Maintain the previous output value	RW	0x2

(2) To achieve the best LPDDR2IO performance, software must keep the impedance bit field at this value.

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Bits	Field Name	Description	Type	Reset
0	RESERVED		R	0

Table 18-623. Register Call Summary for Register CONTROL_LPDDR2IO1_0

Control Module Functional Description
- Pull Selection: [0]
- Signal Integrity Parameter Control Registers With Pad Group Assignment: [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13]

Control Module Register Manual
- SYSCTRL_PADCONF_CORE Register Summary: [14]

For more information about slew rate (turn-on time) settings, see Section 18.4.12.9.2, *High-Speed I/O Buffers With Impedance, Slew Rate, and Weak Driver Settings*.

Table 18-624. CONTROL_LPDDR2IO1_1

Address Offset	0x0000 063C		
Physical Address	0x4A10 063C	**Instance**	SYSCTRL_PADCONF_CORE
Description	LPDDR2 1 I/O control 1 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31 30	29 28 27	26 25	24	23 22	21 20 19	18 17	16	15 14	13 12 11	10 9	8	7 6	5 4 3	2 1	0
LPDDR2IO1_GR8_SR	LPDDR2IO1_GR8_I	LPDDR2IO1_GR8_WD	RESERVED	LPDDR2IO1_GR7_SR	LPDDR2IO1_GR7_I	LPDDR2IO1_GR7_WD	RESERVED	LPDDR2IO1_GR6_SR	LPDDR2IO1_GR6_I	LPDDR2IO1_GR6_WD	RESERVED	LPDDR2IO1_GR5_SR	LPDDR2IO1_GR5_I	LPDDR2IO1_GR5_WD	RESERVED

Bits	Field Name	Description	Type	Reset
31:30	LPDDR2IO1_GR8_SR	Group 8 Slew Rate control sr1:sr0	RW	0x2
29:27	LPDDR2IO1_GR8_I	Group 8 Impedence control i2:i0 0x0: for Drv5 0x1: for Drv6 0x2: for Drv7 0x3: for Drv8 0x4: for Drv9 0x5: for Drv10 0x6: for Drv11 0x7: Drv12(1)	RW	0x3
26:25	LPDDR2IO1_GR8_WD	Group 8 Weak driver control wd1:wd0 0x0: Pull logic disabled 0x1: pull up 0x2: pull down 0x3: Maintain the previous output value	RW	0x2
24	RESERVED		R	0
23:22	LPDDR2IO1_GR7_SR	Group 7 Slew Rate control sr1:sr0	RW	0x2

(1) To achieve the best LPDDR2IO performance, software must keep the impedance bit field at this value.

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Bits	Field Name	Description	Type	Reset
21:19	LPDDR2IO1_GR7_I	Group 7 Impedence control i2:i0 0x0: for Drv5 0x1: for Drv6 0x2: for Drv7 0x3: for Drv8 0x4: for Drv9 0x5: for Drv10 0x6: for Drv11 0x7: Drv12 (2)	RW	0x3
18:17	LPDDR2IO1_GR7_WD	Group 7 Weak driver control wd1:wd0 0x0: Pull logic disabled 0x1: pull up 0x2: pull down 0x3: Maintain the previous output value	RW	0x2
16	RESERVED		R	0
15:14	LPDDR2IO1_GR6_SR	Group 6 Slew Rate control sr1:sr0	RW	0x2
13:11	LPDDR2IO1_GR6_I	Group 6 Impedence control i2:i0 0x0: for Drv5 0x1: for Drv6 0x2: for Drv7 0x3: for Drv8 0x4: for Drv9 0x5: for Drv10 0x6: for Drv11 0x7: Drv12 (2)	RW	0x3
10:9	LPDDR2IO1_GR6_WD	Group 6 Weak driver control wd1:wd0 0x0: Pull logic disabled 0x1: pull up 0x2: pull down 0x3: Maintain the previous output value	RW	0x2
8	RESERVED		R	0
7:6	LPDDR2IO1_GR5_SR	Group 5 Slew Rate control sr1:sr0	RW	0x2
5:3	LPDDR2IO1_GR5_I	Group 5 Impedence control i2:i0 0x0: for Drv5 0x1: for Drv6 0x2: for Drv7 0x3: for Drv8 0x4: for Drv9 0x5: for Drv10 0x6: for Drv11 0x7: Drv12 (2)	RW	0x3
2:1	LPDDR2IO1_GR5_WD	Group 5 Weak driver control wd1:wd0 0x0: Pull logic disabled 0x1: pull up 0x2: pull down 0x3: Maintain the previous output value	RW	0x2
0	RESERVED		R	0

(2) To achieve the best LPDDR2IO performance, software must keep the impedance bit field at this value.

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Table 18-625. Register Call Summary for Register CONTROL_LPDDR2IO1_1

Control Module Functional Description
• Signal Integrity Parameter Control Registers With Pad Group Assignment: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12]
Control Module Register Manual
• SYSCTRL_PADCONF_CORE Register Summary: [13]

For more information about slew rate (turn-on time) settings, see Section 18.4.12.9.2, *High-Speed I/O Buffers With Impedance, Slew Rate, and Weak Driver Settings*.

Table 18-626. CONTROL_LPDDR2IO1_2

Address Offset	0x0000 0640		
Physical Address	0x4A10 0640	**Instance**	SYSCTRL_PADCONF_CORE
Description	LPDDR2 1 I/O control 2 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31 30	29 28 27	26 25	24	23 22	21 20 19	18 17	16	15 14	13 12 11	10 9	8	7 6 5 4 3 2 1 0
LPDDR2IO1_GR11_SR	LPDDR2IO1_GR11_I	LPDDR2IO1_GR11_WD	RESERVED	LPDDR2IO1_GR10_SR	LPDDR2IO1_GR10_I	LPDDR2IO1_GR10_WD	RESERVED	LPDDR2IO1_GR9_SR	LPDDR2IO1_GR9_I	LPDDR2IO1_GR9_WD	RESERVED	

Bits	Field Name	Description	Type	Reset
31:30	LPDDR2IO1_GR11_SR	Group 11 Slew Rate control sr1:sr0	RW	0x2
29:27	LPDDR2IO1_GR11_I	Group 11 Impedence control i2:i0 0x0: for Drv5 0x1: for Drv6 0x2: for Drv7 0x3: for Drv8 0x4: for Drv9 0x5: for Drv10 0x6: for Drv11 0x7: Drv12(1)	RW	0x3
26:25	LPDDR2IO1_GR11_WD	Group 11 Weak driver control wd1:wd0 0x0: Pull logic disabled 0x1: pull up 0x2: pull down 0x3: Maintain the previous output value	RW	0x2
24	RESERVED		R	0
23:22	LPDDR2IO1_GR10_SR	Group 10 Slew Rate control sr1:sr0	RW	0x2

(1) To achieve the best LPDDR2IO performance, software must keep the impedance bit field at this value.

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Bits	Field Name	Description	Type	Reset
21:19	LPDDR2IO1_GR10_I	Group 10 Impedence control i2:i0 0x0: for Drv5 0x1: for Drv6 0x2: for Drv7 0x3: for Drv8 0x4: for Drv9 0x5: for Drv10 0x6: for Drv11 0x7: Drv12 (2)	RW	0x3
18:17	LPDDR2IO1_GR10_WD	Group 10 Weak driver control wd1:wd0 0x0: Pull logic disabled 0x1: pull up 0x2: pull down 0x3: Maintain the previous output value	RW	0x2
16	RESERVED		R	0
15:14	LPDDR2IO1_GR9_SR	Group 9 Slew Rate control sr1:sr0	RW	0x2
13:11	LPDDR2IO1_GR9_I	Group 9 Impedence control i2:i0 0x0: for Drv5 0x1: for Drv6 0x2: for Drv7 0x3: for Drv8 0x4: for Drv9 0x5: for Drv10 0x6: for Drv11 0x7: Drv12 (2)	RW	0x3
10:9	LPDDR2IO1_GR9_WD	Group 9 Weak driver control wd1:wd0 0x0: Pull logic disabled 0x1: pull up 0x2: pull down 0x3: Maintain the previous output value	RW	0x2
8:0	RESERVED		R	0x000

(2) To achieve the best LPDDR2IO performance, software must keep the impedance bit field at this value.

Table 18-627. Register Call Summary for Register CONTROL_LPDDR2IO1_2

Control Module Functional Description • Pull Selection: [0] • Signal Integrity Parameter Control Registers With Pad Group Assignment: [1] [2] [3] [4] [5] [6] [7] [8] [9] [10]
Control Module Register Manual • SYSCTRL_PADCONF_CORE Register Summary: [11]

For more information about slew rate (turn-on time) settings, see Section 18.4.12.9.2, *High-Speed I/O Buffers With Impedance, Slew Rate, and Weak Driver Settings*.

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Table 18-628. CONTROL_LPDDR2IO1_3

Address Offset	0x0000 0644
Physical Address	0x4A10 0644 **Instance** SYSCTRL_PADCONF_CORE
Description	LPDDR2 1 I/O control 3 Access conditions. Read: unrestricted, Write: unrestricted
Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LPDDR21_VREF_CA_CCAP0	LPDDR21_VREF_CA_CCAP1	LPDDR21_VREF_CA_INT_CCAP0	LPDDR21_VREF_CA_INT_CCAP1	LPDDR21_VREF_CA_INT_TAP0	LPDDR21_VREF_CA_INT_TAP1	LPDDR21_VREF_CA_TAP0	LPDDR21_VREF_CA_TAP1	LPDDR21_VREF_DQ_INT0_CCAP0	LPDDR21_VREF_DQ_INT0_CCAP1	LPDDR21_VREF_DQ_INT0_TAP0	LPDDR21_VREF_DQ_INT0_TAP1	LPDDR21_VREF_DQ_INT1_CCAP0	LPDDR21_VREF_DQ_INT1_CCAP1	LPDDR21_VREF_DQ_INT1_TAP0	LPDDR21_VREF_DQ_INT1_TAP1	LPDDR21_VREF_DQ_CCAP0	LPDDR21_VREF_DQ_CCAP1	LPDDR21_VREF_DQ_TAP0	LPDDR21_VREF_DQ_TAP1	LPDDR21_VREF_DQ_INT2_CCAP0	LPDDR21_VREF_DQ_INT3_CCAP0	LPDDR21_VREF_DQ_INT2_CCAP1	LPDDR21_VREF_DQ_INT3_CCAP1	LPDDR21_VREF_DQ_INT2_TAP0	LPDDR21_VREF_DQ_INT3_TAP0	LPDDR21_VREF_DQ_INT2_TAP1	LPDDR21_VREF_DQ_INT3_TAP1	LPDDR21_INT_VREF_EN_CA	LPDDR21_INT_VREF_EN_DQ	LPDDR21_INT_VREF_AUTO_EN_CA	LPDDR21_INT_VREF_AUTO_EN_DQ

Bits	Field Name	Description	Type	Reset
31	LPDDR21_VREF_CA_CCAP0	Selection for coupling cap connection 0x0: Disabled 0x1: Enabled	RW	1
30	LPDDR21_VREF_CA_CCAP1	Selection for coupling cap connection 0x0: Disabled 0x1: Enabled	RW	0
29	LPDDR21_VREF_CA_INT_CCAP0	Selection for coupling cap connection 0x0: Disabled 0x1: Enabled	RW	1
28	LPDDR21_VREF_CA_INT_CCAP1	Selection for coupling cap connection 0x0: Disabled 0x1: Enabled	RW	0
27	LPDDR21_VREF_CA_INT_TAP0	Selection for internal reference voltage drive 0x0: Disabled 0x1: Enabled	RW	1
26	LPDDR21_VREF_CA_INT_TAP1	Selection for internal reference voltage drive 0x0: Disabled 0x1: Enabled	RW	1
25	LPDDR21_VREF_CA_TAP0	Selection for internal reference voltage drive 0x0: Disabled 0x1: Enabled	RW	1
24	LPDDR21_VREF_CA_TAP1	Selection for internal reference voltage drive 0x0: Disabled 0x1: Enabled	RW	1
23	LPDDR21_VREF_DQ_INT0_CCAP0	Selection for coupling cap connection 0x0: Disabled 0x1: Enabled	RW	1

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Bits	Field Name	Description	Type	Reset
22	LPDDR21_VREF_DQ_INT0_CCAP1	Selection for coupling cap connection 0x0: Disabled 0x1: Enabled	RW	0
21	LPDDR21_VREF_DQ_INT0_TAP0	Selection for internal reference voltage drive 0x0: Disabled 0x1: Enabled	RW	1
20	LPDDR21_VREF_DQ_INT0_TAP1	Selection for internal reference voltage drive 0x0: Disabled 0x1: Enabled	RW	1
19	LPDDR21_VREF_DQ_INT1_CCAP0	Selection for coupling cap connection 0x0: Disabled 0x1: Enabled	RW	1
18	LPDDR21_VREF_DQ_INT1_CCAP1	Selection for coupling cap connection 0x0: Disabled 0x1: Enabled	RW	0
17	LPDDR21_VREF_DQ_INT1_TAP0	Selection for internal reference voltage drive 0x0: Disabled 0x1: Enabled	RW	1
16	LPDDR21_VREF_DQ_INT1_TAP1	Selection for internal reference voltage drive 0x0: Disabled 0x1: Enabled	RW	1
15	LPDDR21_VREF_DQ_CCAP0	Selection for coupling cap connection 0x0: Disabled 0x1: Enabled	RW	1
14	LPDDR21_VREF_DQ_CCAP1	Selection for coupling cap connection 0x0: Disabled 0x1: Enabled	RW	0
13	LPDDR21_VREF_DQ_TAP0	Selection for internal reference voltage drive 0x0: Disabled 0x1: Enabled	RW	1
12	LPDDR21_VREF_DQ_TAP1	Selection for internal reference voltage drive 0x0: Disabled 0x1: Enabled	RW	1
11	LPDDR21_VREF_DQ_INT2_CCAP0	Selection for coupling cap connection 0x0: Disabled 0x1: Enabled	RW	1
10	LPDDR21_VREF_DQ_INT3_CCAP0	Selection for coupling cap connection 0x0: Disabled 0x1: Enabled	RW	1
9	LPDDR21_VREF_DQ_INT2_CCAP1	Selection for coupling cap connection 0x0: Disabled 0x1: Enabled	RW	0
8	LPDDR21_VREF_DQ_INT3_CCAP1	Selection for coupling cap connection 0x0: Disabled 0x1: Enabled	RW	0
7	LPDDR21_VREF_DQ_INT2_TAP0	Selection for internal reference voltage drive 0x0: Disabled 0x1: Enabled	RW	1

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Bits	Field Name	Description	Type	Reset
6	LPDDR21_VREF_DQ_INT3_TAP0	Selection for internal reference voltage drive 0x0: Disabled 0x1: Enabled	RW	1
5	LPDDR21_VREF_DQ_INT2_TAP1	Selection for internal reference voltage drive 0x0: Disabled 0x1: Enabled	RW	1
4	LPDDR21_VREF_DQ_INT3_TAP1	Selection for internal reference voltage drive 0x0: Disabled 0x1: Enabled	RW	1
3	LPDDR21_INT_VREF_EN_CA	Internal vref enable for CA in manual mode (if both manual and auto mode is enabled then manual mode takes the priority) 0x0: Disabled 0x1: Enabled	RW	1
2	LPDDR21_INT_VREF_EN_DQ	Internal vref enable for DQ in manual mode (if both manual and auto mode is enabled then manual mode takes the priority) 0x0: Disabled 0x1: Enabled	RW	1
1	LPDDR21_INT_VREF_AUTO_EN_CA	Internal vref enable for CA in auto mode (if both manual and auto mode is enabled then manual mode takes the priority) 0x0: Disabled 0x1: Enabled	RW	1
0	LPDDR21_INT_VREF_AUTO_EN_DQ	Internal vref enable for DQ in auto mode (if both manual and auto mode is enabled then manual mode takes the priority) 0x0: Disabled 0x1: Enabled	RW	1

Table 18-629. Register Call Summary for Register CONTROL_LPDDR2IO1_3

Control Module Functional Description
- Signal Integrity Parameter Control Registers With Pad Group Assignment: [0] [1] [2]

Control Module Register Manual
- SYSCTRL_PADCONF_CORE Register Summary: [3]

Table 18-630. CONTROL_LPDDR2IO2_0

Address Offset	0x0000 0648		
Physical Address	0x4A10 0648	**Instance**	SYSCTRL_PADCONF_CORE
Description	LPDDR2 2 I/O control 0 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LPDDR2IO2_GR4_SR					LPDDR2IO2_GR4_I						LPDDR2IO2_GR4_WD				RESERVED				LPDDR2IO2_GR3_SR													
LPDDR2IO2_GR3_I								LPDDR2IO2_GR3_WD								RESERVED								LPDDR2IO2_GR2_SR							
LPDDR2IO2_GR2_I								LPDDR2IO2_GR2_WD								RESERVED								LPDDR2IO2_GR1_SR							
LPDDR2IO2_GR1_I								LPDDR2IO2_GR1_WD								RESERVED															

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Bits	Field Name	Description	Type	Reset
31:30	LPDDR2IO2_GR4_SR	Group 4 Slew Rate control sr1:sr0	RW	0x2
29:27	LPDDR2IO2_GR4_I	Group 4 Impedence control i2:i0 0x0: for Drv5 0x1: for Drv6 0x2: for Drv7 0x3: for Drv8 0x4: for Drv9 0x5: for Drv10 0x6: for Drv11 0x7: Drv12(1)	RW	0x3
26:25	LPDDR2IO2_GR4_WD	Group 4 Weak driver control wd1:wd0 0x0: Pull logic disabled 0x1: pull up 0x2: pull down 0x3: Maintain the previous output value	RW	0x2
24	RESERVED		R	0
23:22	LPDDR2IO2_GR3_SR	Group 3 Slew Rate control sr1:sr0	RW	0x2
21:19	LPDDR2IO2_GR3_I	Group 3 Impedence control i2:i0 0x0: for Drv5 0x1: for Drv6 0x2: for Drv7 0x3: for Drv8 0x4: for Drv9 0x5: for Drv10 0x6: for Drv11 0x7: Drv12(1)	RW	0x3
18:17	LPDDR2IO2_GR3_WD	Group 3 Weak driver control wd1:wd0 0x0: Pull logic disabled 0x1: pull up 0x2: pull down 0x3: Maintain the previous output value	RW	0x2
16	RESERVED		R	0
15:14	LPDDR2IO2_GR2_SR	Group 2 Slew Rate control sr1:sr0	RW	0x2
13:11	LPDDR2IO2_GR2_I	Group 2 Impedence control i2:i0 0x0: for Drv5 0x1: for Drv6 0x2: for Drv7 0x3: for Drv8 0x4: for Drv9 0x5: for Drv10 0x6: for Drv11 0x7: Drv12(1)	RW	0x3
10:9	LPDDR2IO2_GR2_WD	Group 2 Weak driver control wd1:wd0 0x0: Pull logic disabled 0x1: pull up 0x2: pull down 0x3: Maintain the previous output value	RW	0x2

(1) To achieve the best LPDDR2IO performance, software must keep the impedance bit field at this value.

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Bits	Field Name	Description	Type	Reset
8	RESERVED		R	0
7:6	LPDDR2IO2_GR1_SR	Group 1 Slew Rate control sr1:sr0	RW	0x2
5:3	LPDDR2IO2_GR1_I	Group 1 Impedence control i2:i0 0x0: for Drv5 0x1: for Drv6 0x2: for Drv7 0x3: for Drv8 0x4: for Drv9 0x5: for Drv10 0x6: for Drv11 0x7: Drv12 (2)	RW	0x3
2:1	LPDDR2IO2_GR1_WD	Group 1 Weak driver control wd1:wd0 0x0: Pull logic disabled 0x1: pull up 0x2: pull down 0x3: Maintain the previous output value	RW	0x2
0	RESERVED		R	0

(2) To achieve the best LPDDR2IO performance, software must keep the impedance bit field at this value.

Table 18-631. Register Call Summary for Register CONTROL_LPDDR2IO2_0

Control Module Functional Description
- Pull Selection: [0]
- Signal Integrity Parameter Control Registers With Pad Group Assignment: [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13]

Control Module Register Manual
- SYSCTRL_PADCONF_CORE Register Summary: [14]

For more information about slew rate (turn-on time) settings, see Section 18.4.12.9.2, *High-Speed I/O Buffers With Impedance, Slew Rate, and Weak Driver Settings*.

Table 18-632. CONTROL_LPDDR2IO2_1

Address Offset	0x0000 064C		
Physical Address	0x4A10 064C	**Instance**	SYSCTRL_PADCONF_CORE
Description	LPDDR2 2 I/O control 1 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LPDDR2IO2_GR8_SR		LPDDR2IO2_GR8_I			LPDDR2IO2_GR8_WD		RESERVED	LPDDR2IO2_GR7_SR		LPDDR2IO2_GR7_I			LPDDR2IO2_GR7_WD		RESERVED	LPDDR2IO2_GR6_SR		LPDDR2IO2_GR6_I			LPDDR2IO2_GR6_WD		RESERVED	LPDDR2IO2_GR5_SR		LPDDR2IO2_GR5_I			LPDDR2IO2_GR5_WD		RESERVED

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Bits	Field Name	Description	Type	Reset
31:30	LPDDR2IO2_GR8_SR	Group 8 Slew Rate control sr1:sr0	RW	0x2
29:27	LPDDR2IO2_GR8_I	Group 8 Impedence control i2:i0 0x0: for Drv5 0x1: for Drv6 0x2: for Drv7 0x3: for Drv8 0x4: for Drv9 0x5: for Drv10 0x6: for Drv11 0x7: Drv12(1)	RW	0x3
26:25	LPDDR2IO2_GR8_WD	Group 8 Weak driver control wd1:wd0 0x0: Pull logic disabled 0x1: pull up 0x2: pull down 0x3: Maintain the previous output value	RW	0x2
24	RESERVED		R	0
23:22	LPDDR2IO2_GR7_SR	Group 7 Slew Rate control sr1:sr0	RW	0x2
21:19	LPDDR2IO2_GR7_I	Group 7 Impedence control i2:i0 0x0: for Drv5 0x1: for Drv6 0x2: for Drv7 0x3: for Drv8 0x4: for Drv9 0x5: for Drv10 0x6: for Drv11 0x7: Drv12(1)	RW	0x3
18:17	LPDDR2IO2_GR7_WD	Group 7 Weak driver control wd1:wd0 0x0: Pull logic disabled 0x1: pull up 0x2: pull down 0x3: Maintain the previous output value	RW	0x2
16	RESERVED		R	0
15:14	LPDDR2IO2_GR6_SR	Group 6 Slew Rate control sr1:sr0	RW	0x2
13:11	LPDDR2IO2_GR6_I	Group 6 Impedence control i2:i0 0x0: for Drv5 0x1: for Drv6 0x2: for Drv7 0x3: for Drv8 0x4: for Drv9 0x5: for Drv10 0x6: for Drv11 0x7: Drv12(1)	RW	0x3
10:9	LPDDR2IO2_GR6_WD	Group 6 Weak driver control wd1:wd0 0x0: Pull logic disabled 0x1: pull up 0x2: pull down 0x3: Maintain the previous output value	RW	0x2

(1) To achieve the best LPDDR2IO performance, software must keep the impedance bit field at this value.

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Bits	Field Name	Description	Type	Reset
8	RESERVED		R	0
7:6	LPDDR2IO2_GR5_SR	Group 5 Slew Rate control sr1:sr0	RW	0x2
5:3	LPDDR2IO2_GR5_I	Group 5 Impedence control i2:i0 0x0: for Drv5 0x1: for Drv6 0x2: for Drv7 0x3: for Drv8 0x4: for Drv9 0x5: for Drv10 0x6: for Drv11 0x7: Drv12(2)	RW	0x3
2:1	LPDDR2IO2_GR5_WD	Group 5 Weak driver control wd1:wd0 0x0: Pull logic disabled 0x1: pull up 0x2: pull down 0x3: Maintain the previous output value	RW	0x2
0	RESERVED		R	0

(2) To achieve the best LPDDR2IO performance, software must keep the impedance bit field at this value.

Table 18-633. Register Call Summary for Register CONTROL_LPDDR2IO2_1

Control Module Functional Description • Signal Integrity Parameter Control Registers With Pad Group Assignment: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12]
Control Module Register Manual • SYSCTRL_PADCONF_CORE Register Summary: [13]

For more information about slew rate (turn-on time) settings, see Section 18.4.12.9.2, *High-Speed I/O Buffers With Impedance, Slew Rate, and Weak Driver Settings*.

Table 18-634. CONTROL_LPDDR2IO2_2

Address Offset	0x0000 0650		
Physical Address	0x4A10 0650	**Instance**	SYSCTRL_PADCONF_CORE
Description	LPDDR2 2 I/O control 2 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LPDDR2IO2_GR11_SR		LPDDR2IO2_GR11_I			LPDDR2IO2_GR11_WD		RESERVED	LPDDR2IO2_GR10_SR		LPDDR2IO2_GR10_I			LPDDR2IO2_GR10_WD		RESERVED	LPDDR2IO2_GR9_SR		LPDDR2IO2_GR9_I			LPDDR2IO2_GR9_WD		RESERVED							

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Bits	Field Name	Description	Type	Reset
31:30	LPDDR2IO2_GR11_SR	Group 11 Slew Rate control sr1:sr0	RW	0x2
29:27	LPDDR2IO2_GR11_I	Group 11 Impedence control i2:i0 0x0: for Drv5 0x1: for Drv6 0x2: for Drv7 0x3: for Drv8 0x4: for Drv9 0x5: for Drv10 0x6: for Drv11 0x7: Drv12(1)	RW	0x3
26:25	LPDDR2IO2_GR11_WD	Group 11 Weak driver control wd1:wd0 0x0: Pull logic disabled 0x1: pull up 0x2: pull down 0x3: Maintain the previous output value	RW	0x2
24	RESERVED		R	0
23:22	LPDDR2IO2_GR10_SR	Group 10 Slew Rate control sr1:sr0	RW	0x2
21:19	LPDDR2IO2_GR10_I	Group 10 Impedence control i2:i0 0x0: for Drv5 0x1: for Drv6 0x2: for Drv7 0x3: for Drv8 0x4: for Drv9 0x5: for Drv10 0x6: for Drv11 0x7: Drv12(1)	RW	0x3
18:17	LPDDR2IO2_GR10_WD	Group 10 Weak driver control wd1:wd0 0x0: Pull logic disabled 0x1: pull up 0x2: pull down 0x3: Maintain the previous output value	RW	0x2
16	RESERVED		R	0
15:14	LPDDR2IO2_GR9_SR	Group 9 Slew Rate control sr1:sr0	RW	0x2
13:11	LPDDR2IO2_GR9_I	Group 9 Impedence control i2:i0 0x0: for Drv5 0x1: for Drv6 0x2: for Drv7 0x3: for Drv8 0x4: for Drv9 0x5: for Drv10 0x6: for Drv11 0x7: Drv12(1)	RW	0x3
10:9	LPDDR2IO2_GR9_WD	Group 9 Weak driver control wd1:wd0 0x0: Pull logic disabled 0x1: pull up 0x2: pull down 0x3: Maintain the previous output value	RW	0x2
8:0	RESERVED		R	0x000

(1) To achieve the best LPDDR2IO performance, software must keep the impedance bit field at this value.

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Table 18-635. Register Call Summary for Register CONTROL_LPDDR2IO2_2

Control Module Functional Description

- Pull Selection: [0]
- Signal Integrity Parameter Control Registers With Pad Group Assignment: [1] [2] [3] [4] [5] [6] [7] [8] [9] [10]

Control Module Register Manual

- SYSCTRL_PADCONF_CORE Register Summary: [11]

For more information about slew rate (turn-on time) settings, see Section 18.4.12.9.2, *High-Speed I/O Buffers With Impedance, Slew Rate, and Weak Driver Settings*.

Table 18-636. CONTROL_LPDDR2IO2_3

Address Offset	0x0000 0654		
Physical Address	0x4A10 0654	**Instance**	SYSCTRL_PADCONF_CORE
Description	LPDDR2 2 I/O control 3 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LPDDR22_VREF_CA_CCAP0	LPDDR22_VREF_CA_CCAP1	LPDDR22_VREF_CA_INT_CCAP0	LPDDR22_VREF_CA_INT_CCAP1	LPDDR22_VREF_CA_INT_TAP0	LPDDR22_VREF_CA_INT_TAP1	LPDDR22_VREF_CA_TAP0	LPDDR22_VREF_CA_TAP1	LPDDR22_VREF_DQ_INT0_CCAP0	LPDDR22_VREF_DQ_INT0_CCAP1	LPDDR22_VREF_DQ_INT0_TAP0	LPDDR22_VREF_DQ_INT0_TAP1	LPDDR22_VREF_DQ_INT1_CCAP0	LPDDR22_VREF_DQ_INT1_CCAP1	LPDDR22_VREF_DQ_INT1_TAP0	LPDDR22_VREF_DQ_INT1_TAP1	LPDDR22_VREF_DQ_CCAP0	LPDDR22_VREF_DQ_CCAP1	LPDDR22_VREF_DQ_TAP0	LPDDR22_VREF_DQ_TAP1	LPDDR22_VREF_DQ_INT2_CCAP0	LPDDR22_VREF_DQ_INT3_CCAP0	LPDDR22_VREF_DQ_INT2_CCAP1	LPDDR22_VREF_DQ_INT3_CCAP1	LPDDR22_VREF_DQ_INT2_TAP0	LPDDR22_VREF_DQ_INT3_TAP0	LPDDR22_VREF_DQ_INT2_TAP1	LPDDR22_VREF_DQ_INT3_TAP1	LPDDR22_INT_VREF_EN_CA	LPDDR22_INT_VREF_EN_DQ	LPDDR22_INT_VREF_AUTO_EN_CA	LPDDR22_INT_VREF_AUTO_EN_DQ

Bits	Field Name	Description	Type	Reset
31	LPDDR22_VREF_CA_CCAP0	Selection for coupling cap connection 0x0: Disabled 0x1: Enabled	RW	1
30	LPDDR22_VREF_CA_CCAP1	Selection for coupling cap connection 0x0: Disabled 0x1: Enabled	RW	0
29	LPDDR22_VREF_CA_INT_CCAP0	Selection for coupling cap connection 0x0: Disabled 0x1: Enabled	RW	1
28	LPDDR22_VREF_CA_INT_CCAP1	Selection for coupling cap connection 0x0: Disabled 0x1: Enabled	RW	0
27	LPDDR22_VREF_CA_INT_TAP0	Selection for internal reference voltage drive 0x0: Disabled 0x1: Enabled	RW	1
26	LPDDR22_VREF_CA_INT_TAP1	Selection for internal reference voltage drive 0x0: Disabled 0x1: Enabled	RW	1

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Bits	Field Name	Description	Type	Reset
25	LPDDR22_VREF_CA_TAP0	Selection for internal reference voltage drive 0x0: Disabled 0x1: Enabled	RW	1
24	LPDDR22_VREF_CA_TAP1	Selection for internal reference voltage drive 0x0: Disabled 0x1: Enabled	RW	1
23	LPDDR22_VREF_DQ_INT0_CCAP0	Selection for coupling cap connection 0x0: Disabled 0x1: Enabled	RW	1
22	LPDDR22_VREF_DQ_INT0_CCAP1	Selection for coupling cap connection 0x0: Disabled 0x1: Enabled	RW	0
21	LPDDR22_VREF_DQ_INT0_TAP0	Selection for internal reference voltage drive 0x0: Disabled 0x1: Enabled	RW	1
20	LPDDR22_VREF_DQ_INT0_TAP1	Selection for internal reference voltage drive 0x0: Disabled 0x1: Enabled	RW	1
19	LPDDR22_VREF_DQ_INT1_CCAP0	Selection for coupling cap connection 0x0: Disabled 0x1: Enabled	RW	1
18	LPDDR22_VREF_DQ_INT1_CCAP1	Selection for coupling cap connection 0x0: Disabled 0x1: Enabled	RW	0
17	LPDDR22_VREF_DQ_INT1_TAP0	Selection for internal reference voltage drive 0x0: Disabled 0x1: Enabled	RW	1
16	LPDDR22_VREF_DQ_INT1_TAP1	Selection for internal reference voltage drive 0x0: Disabled 0x1: Enabled	RW	1
15	LPDDR22_VREF_DQ_CCAP0	Selection for coupling cap connection 0x0: Disabled 0x1: Enabled	RW	1
14	LPDDR22_VREF_DQ_CCAP1	Selection for coupling cap connection 0x0: Disabled 0x1: Enabled	RW	0
13	LPDDR22_VREF_DQ_TAP0	Selection for internal reference voltage drive 0x0: Disabled 0x1: Enabled	RW	1
12	LPDDR22_VREF_DQ_TAP1	Selection for internal reference voltage drive 0x0: Disabled 0x1: Enabled	RW	1
11	LPDDR22_VREF_DQ_INT2_CCAP0	Selection for coupling cap connection 0x0: Disabled 0x1: Enabled	RW	1
10	LPDDR22_VREF_DQ_INT3_CCAP0	Selection for coupling cap connection 0x0: Disabled 0x1: Enabled	RW	1

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Bits	Field Name	Description	Type	Reset
9	LPDDR22_VREF_DQ_INT2_CCAP1	Selection for coupling cap connection 0x0: Disabled 0x1: Enabled	RW	0
8	LPDDR22_VREF_DQ_INT3_CCAP1	Selection for coupling cap connection 0x0: Disabled 0x1: Enabled	RW	0
7	LPDDR22_VREF_DQ_INT2_TAP0	Selection for internal reference voltage drive 0x0: Disabled 0x1: Enabled	RW	1
6	LPDDR22_VREF_DQ_INT3_TAP0	Selection for internal reference voltage drive 0x0: Disabled 0x1: Enabled	RW	1
5	LPDDR22_VREF_DQ_INT2_TAP1	Selection for internal reference voltage drive 0x0: Disabled 0x1: Enabled	RW	1
4	LPDDR22_VREF_DQ_INT3_TAP1	Selection for internal reference voltage drive 0x0: Disabled 0x1: Enabled	RW	1
3	LPDDR22_INT_VREF_EN_CA	Internal vref enable for CA in manual mode (if both manual and auto mode is enabled then manual mode takes the priority) 0x0: Disabled 0x1: Enabled	RW	1
2	LPDDR22_INT_VREF_EN_DQ	Internal vref enable for DQ in manual mode (if both manual and auto mode is enabled then manual mode takes the priority) 0x0: Disabled 0x1: Enabled	RW	1
1	LPDDR22_INT_VREF_AUTO_EN_CA	Internal vref enable for CA in auto mode (if both manual and auto mode is enabled then manual mode takes the priority) 0x0: Disabled 0x1: Enabled	RW	1
0	LPDDR22_INT_VREF_AUTO_EN_DQ	Internal vref enable for DQ in auto mode (if both manual and auto mode is enabled then manual mode takes the priority) 0x0: Disabled 0x1: Enabled	RW	1

Table 18-637. Register Call Summary for Register CONTROL_LPDDR2IO2_3

Control Module Functional Description

- Signal Integrity Parameter Control Registers With Pad Group Assignment: [0] [1] [2]

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- SYSCTRL_PADCONF_CORE Register Summary: [3]

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Table 18-638. CONTROL_BUS_HOLD

Address Offset	0x0000 0658		
Physical Address	0x4A10 0658	**Instance**	SYSCTRL_PADCONF_CORE
Description	BUS HOLD I/O controls Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

Bits	Field Name	Description	Type	Reset
31:0	RESERVED		R	0x0000 0000

Table 18-639. Register Call Summary for Register CONTROL_BUS_HOLD

Control Module Register Manual

- SYSCTRL_PADCONF_CORE Register Summary: [0]

Table 18-640. CONTROL_C2C

Address Offset	0x0000 065C		
Physical Address	0x4A10 065C	**Instance**	SYSCTRL_PADCONF_CORE
Description	C2C controls Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2C_SPARE																															

Bits	Field Name	Description	Type	Reset
31:0	C2C_SPARE	C2C spare register bits	RW	0x0000 0000

Table 18-641. Register Call Summary for Register CONTROL_C2C

Control Module Register Manual

- SYSCTRL_PADCONF_CORE Register Summary: [0]

Table 18-642. CONTROL_CORE_CONTROL_SPARE_RW

Address Offset	0x0000 0660		
Physical Address	0x4A10 0660	**Instance**	SYSCTRL_PADCONF_CORE
Description	CORE control spare RW Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CORE_CONTROL_SPARE_RW																															

Bits	Field Name	Description	Type	Reset
31:0	CORE_CONTROL_SPARE_RW	Core control spare register bits RW	RW	0x0000 0000

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Table 18-643. Register Call Summary for Register CONTROL_CORE_CONTROL_SPARE_RW

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- SYSCTRL_PADCONF_CORE Register Summary: [0]

Table 18-644. CONTROL_CORE_CONTROL_SPARE_R

Address Offset	0x0000 0664		
Physical Address	0x4A10 0664	**Instance**	SYSCTRL_PADCONF_CORE
Description	CORE control spare R Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CORE_CONTROL_SPARE_R																															

Bits	Field Name	Description	Type	Reset
31:0	CORE_CONTROL_SPARE_R	Core control spare register bits R	R	0x0000 0000

Table 18-645. Register Call Summary for Register CONTROL_CORE_CONTROL_SPARE_R

Control Module Register Manual

- SYSCTRL_PADCONF_CORE Register Summary: [0]

Table 18-646. CONTROL_CORE_CONTROL_SPARE_R_C0

Address Offset	0x0000 0668		
Physical Address	0x4A10 0668	**Instance**	SYSCTRL_PADCONF_CORE
Description	CORE control spare RC Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CORE_CONTROL_SPARE_R_C0	CORE_CONTROL_SPARE_R_C1	CORE_CONTROL_SPARE_R_C2	CORE_CONTROL_SPARE_R_C3	CORE_CONTROL_SPARE_R_C4	CORE_CONTROL_SPARE_R_C5	CORE_CONTROL_SPARE_R_C6	CORE_CONTROL_SPARE_R_C7	RESERVED																							

Bits	Field Name	Description	Type	Reset
31	CORE_CONTROL_SPARE_R_C0	Core control spare register bits RC	RW (Write 1 to Clear)	0
30	CORE_CONTROL_SPARE_R_C1	Core control spare register bits RC	RW (Write 1 to Clear)	0
29	CORE_CONTROL_SPARE_R_C2	Core control spare register bits RC	RW (Write 1 to Clear)	0

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Bits	Field Name	Description	Type	Reset
28	CORE_CONTROL_SPARE_R_C3	Core control spare register bits RC	RW (Write 1 to Clear)	0
27	CORE_CONTROL_SPARE_R_C4	Core control spare register bits RC	RW (Write 1 to Clear)	0
26	CORE_CONTROL_SPARE_R_C5	Core control spare register bits RC	RW (Write 1 to Clear)	0
25	CORE_CONTROL_SPARE_R_C6	Core control spare register bits RC	RW (Write 1 to Clear)	0
24	CORE_CONTROL_SPARE_R_C7	Core control spare register bits RC	RW (Write 1 to Clear)	0
23:0	RESERVED		R	0x000000

Table 18-647. Register Call Summary for Register CONTROL_CORE_CONTROL_SPARE_R_C0

Control Module Register Manual
- SYSCTRL_PADCONF_CORE Register Summary: [0]

Table 18-648. CONTROL_CORE_CONTROL_SPARE_RW1

Address Offset	0x0000 066C		
Physical Address	0x4A10 066C	**Instance**	SYSCTRL_PADCONF_CORE
Description	CORE control spare RW1 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CORE_CONTROL_SPARE_RW1																															

Bits	Field Name	Description	Type	Reset
31:0	CORE_CONTROL_SPARE_RW1	Core control spare register bits RW1	RW	0x0000 0000

Table 18-649. Register Call Summary for Register CONTROL_CORE_CONTROL_SPARE_RW1

Control Module Register Manual
- SYSCTRL_PADCONF_CORE Register Summary: [0]

Table 18-650. CONTROL_CORE_CONTROL_SPARE_RW2

Address Offset	0x0000 0670		
Physical Address	0x4A10 0670	**Instance**	SYSCTRL_PADCONF_CORE
Description	CORE control spare RW2 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CORE_CONTROL_SPARE_RW2																															

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Bits	Field Name	Description	Type	Reset
31:0	CORE_CONTROL_SPARE_RW2	Core control spare register bits RW2	RW	0x0000 0000

Table 18-651. Register Call Summary for Register CONTROL_CORE_CONTROL_SPARE_RW2

Control Module Register Manual

- SYSCTRL_PADCONF_CORE Register Summary: [0]

Table 18-652. CONTROL_CORE_CONTROL_SPARE_RW3

Address Offset	0x0000 0674		
Physical Address	0x4A10 0674	**Instance**	SYSCTRL_PADCONF_CORE
Description	CORE control spare RW3 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CORE_CONTROL_SPARE_RW3																															

Bits	Field Name	Description	Type	Reset
31:0	CORE_CONTROL_SPARE_RW3	Core control spare register bits RW3	RW	0x0000 0000

Table 18-653. Register Call Summary for Register CONTROL_CORE_CONTROL_SPARE_RW3

Control Module Register Manual

- SYSCTRL_PADCONF_CORE Register Summary: [0]

Table 18-654. CONTROL_CORE_CONTROL_SPARE_RW4

Address Offset	0x0000 0678		
Physical Address	0x4A10 0678	**Instance**	SYSCTRL_PADCONF_CORE
Description	CORE control spare RW4 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CORE_CONTROL_SPARE_RW4																															

Bits	Field Name	Description	Type	Reset
31:0	CORE_CONTROL_SPARE_RW4	Core control spare register bits RW4	RW	0x0000 0000

Table 18-655. Register Call Summary for Register CONTROL_CORE_CONTROL_SPARE_RW4

Control Module Register Manual

- SYSCTRL_PADCONF_CORE Register Summary: [0]

Table 18-656. CONTROL_CORE_CONTROL_SPARE_RW5

Address Offset	0x0000 067C		
Physical Address	0x4A10 067C	**Instance**	SYSCTRL_PADCONF_CORE
Description	CORE control spare RW5 Access conditions. Read: unrestricted, Write: unrestricted		

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Table 18-656. CONTROL_CORE_CONTROL_SPARE_RW5 (continued)

Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CORE_CONTROL_SPARE_RW5																															

Bits	Field Name	Description	Type	Reset
31:0	CORE_CONTROL_SPARE_RW5	Core control spare register bits RW5	RW	0x0000 0000

Table 18-657. Register Call Summary for Register CONTROL_CORE_CONTROL_SPARE_RW5

Control Module Register Manual

- SYSCTRL_PADCONF_CORE Register Summary: [0]

Table 18-658. CONTROL_CORE_CONTROL_SPARE_RW6

Address Offset	0x0000 0680		
Physical Address	0x4A10 0680	**Instance**	SYSCTRL_PADCONF_CORE
Description	CORE control spare RW6 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CORE_CONTROL_SPARE_RW6																															

Bits	Field Name	Description	Type	Reset
31:0	CORE_CONTROL_SPARE_RW6	Core control spare register bits RW6	RW	0x0000 0000

Table 18-659. Register Call Summary for Register CONTROL_CORE_CONTROL_SPARE_RW6

Control Module Register Manual

- SYSCTRL_PADCONF_CORE Register Summary: [0]

Table 18-660. CONTROL_CORE_CONTROL_SPARE_RW7

Address Offset	0x0000 0684		
Physical Address	0x4A10 0684	**Instance**	SYSCTRL_PADCONF_CORE
Description	CORE control spare RW7 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CORE_CONTROL_SPARE_RW7																															

Bits	Field Name	Description	Type	Reset
31:0	CORE_CONTROL_SPARE_RW7	Core control spare register bits RW7	RW	0x0000 0000

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Table 18-661. Register Call Summary for Register CONTROL_CORE_CONTROL_SPARE_RW7

Control Module Register Manual

- SYSCTRL_PADCONF_CORE Register Summary: [0]

Table 18-662. CONTROL_CORE_CONTROL_SPARE_RW8

Address Offset	0x0000 0688		
Physical Address	0x4A10 0688	**Instance**	SYSCTRL_PADCONF_CORE
Description	CORE control spare RW8 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CORE_CONTROL_SPARE_RW8																															

Bits	Field Name	Description	Type	Reset
31:0	CORE_CONTROL_SPARE_RW8	Core control spare register bits RW8	RW	0x0000 0000

Table 18-663. Register Call Summary for Register CONTROL_CORE_CONTROL_SPARE_RW8

Control Module Register Manual

- SYSCTRL_PADCONF_CORE Register Summary: [0]

Table 18-664. CONTROL_CORE_CONTROL_SPARE_RW9

Address Offset	0x0000 068C		
Physical Address	0x4A10 068C	**Instance**	SYSCTRL_PADCONF_CORE
Description	CORE control spare RW9 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CORE_CONTROL_SPARE_RW9																															

Bits	Field Name	Description	Type	Reset
31:0	CORE_CONTROL_SPARE_RW9	Core control spare register bits RW9	RW	0xFFFF FFFF

Table 18-665. Register Call Summary for Register CONTROL_CORE_CONTROL_SPARE_RW9

Control Module Register Manual

- SYSCTRL_PADCONF_CORE Register Summary: [0]

Table 18-666. CONTROL_CORE_CONTROL_SPARE_R1

Address Offset	0x0000 0690		
Physical Address	0x4A10 0690	**Instance**	SYSCTRL_PADCONF_CORE
Description	CORE control spare R1 Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CORE_CONTROL_SPARE_R1																															

Bits	Field Name	Description	Type	Reset
31:0	CORE_CONTROL_SPARE_R1	Core control spare register bits R1	R	0x0000 0000

Table 18-667. Register Call Summary for Register CONTROL_CORE_CONTROL_SPARE_R1

Control Module Register Manual
- SYSCTRL_PADCONF_CORE Register Summary: [0]

Table 18-668. CONTROL_EMIF

Address Offset	0x0000 0694		
Physical Address	0x4A10 0694	**Instance**	SYSCTRL_PADCONF_CORE
Description	EMIF control Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														EMIF2_RDPIPEN	EMIF1_RDPIPEN

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	EMIF2_RDPIPEN	EMIF2 read pipeline enable 0x0: Disabled 0x1: Enabled	RW	0
0	EMIF1_RDPIPEN	EMIF1 read pipeline enable 0x0: Disabled 0x1: Enabled	RW	0

Table 18-669. Register Call Summary for Register CONTROL_EMIF

Control Module Functional Description
- Device Core Control Module Instance: [0]
- EMIF Read Pipeline Control Register: [1] [2]

Control Module Register Manual
- SYSCTRL_PADCONF_CORE Register Summary: [3]

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Table 18-670. CONTROL_EFUSE_1

Address Offset	0x0000 0700		
Physical Address	0x4A10 0700	**Instance**	SYSCTRL_PADCONF_CORE
Description	EFUSE control 1 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	AVDAC_TRIM_BYTE3							AVDAC_TRIM_BYTE2								AVDAC_TRIM_BYTE1								AVDAC_TRIM_BYTE0							

Bits	Field Name	Description	Type	Reset
31	RESERVED		R	0
30:24	AVDAC_TRIM_BYTE3	AVDAC trim byte3 (Reset value exported from efuse) Note that reset is exported. Its value is = pi_avdac_trim_byte_3	RW	0x00
23:16	AVDAC_TRIM_BYTE2	AVDAC trim byte2 (Reset value exported from efuse) Note that reset is exported. Its value is = pi_avdac_trim_byte_2	RW	0x00
15:8	AVDAC_TRIM_BYTE1	AVDAC trim byte1 (Reset value exported from efuse) Note that reset is exported. Its value is = pi_avdac_trim_byte_1	RW	0x00
7:0	AVDAC_TRIM_BYTE0	AVDAC trim byte0 (Reset value exported from efuse) Note that reset is exported. Its value is = pi_avdac_trim_byte_0	RW	0x00

Table 18-671. Register Call Summary for Register CONTROL_EFUSE_1

Control Module Register Manual

- SYSCTRL_PADCONF_CORE Register Summary: [0]

Table 18-672. CONTROL_EFUSE_2

Address Offset	0x0000 0704		
Physical Address	0x4A10 0704	**Instance**	SYSCTRL_PADCONF_CORE
Description	EFUSE control 2 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EFUSE_SMART2TEST_P0	EFUSE_SMART2TEST_P1	EFUSE_SMART2TEST_P2	EFUSE_SMART2TEST_P3	EFUSE_SMART2TEST_N0	EFUSE_SMART2TEST_N1	EFUSE_SMART2TEST_N2	EFUSE_SMART2TEST_N3	LPDDR2_PTV_N1	LPDDR2_PTV_N2	LPDDR2_PTV_N3	LPDDR2_PTV_N4	LPDDR2_PTV_N5	LPDDR2_PTV_P1	LPDDR2_PTV_P2	LPDDR2_PTV_P3	LPDDR2_PTV_P4	LPDDR2_PTV_P5	RESERVED													

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Bits	Field Name	Description	Type	Reset
31	EFUSE_SMART2TEST_P0	Smart2/3/C2C I/O PMOS process compensation bit 0 (Reset value exported from efuse) Note that reset is exported. Its value is = pi_sr_p0	RW	0
30	EFUSE_SMART2TEST_P1	Smart2/3/C2C I/O PMOS process compensation bit 1 (Reset value exported from efuse) Note that reset is exported. Its value is = pi_sr_p1	RW	0
29	EFUSE_SMART2TEST_P2	Smart2/3/C2C I/O PMOS process compensation bit 2 (Reset value exported from efuse) Note that reset is exported. Its value is = pi_sr_p2	RW	0
28	EFUSE_SMART2TEST_P3	Smart2/3/C2C I/O PMOS process compensation bit 3 (Reset value exported from efuse) Note that reset is exported. Its value is = pi_sr_p3	RW	0
27	EFUSE_SMART2TEST_N0	Smart2/3/C2C I/O NMOS process compensation bit 0 (Reset value exported from efuse) Note that reset is exported. Its value is = pi_sr_n0	RW	0
26	EFUSE_SMART2TEST_N1	Smart2/3/C2C I/O NMOS process compensation bit 1(Reset value exported from efuse) Note that reset is exported. Its value is = pi_sr_n1	RW	0
25	EFUSE_SMART2TEST_N2	Smart2/3/C2C I/O NMOS process compensation bit 2 (Reset value exported from efuse) Note that reset is exported. Its value is = pi_sr_n2	RW	0
24	EFUSE_SMART2TEST_N3	Smart2/3/C2C I/O NMOS process compensation bit 3 (Reset value exported from efuse) Note that reset is exported. Its value is = pi_sr_n3	RW	0
23	LPDDR2_PTV_N1	LPDDR2IO NMOS PTV code bit 1 (Reset value exported from efuse) Note that reset is exported. Its value is = pi_lpddr2_n1	RW	0
22	LPDDR2_PTV_N2	LPDDR2IO NMOS PTV code bit 2 (Reset value exported from efuse) Note that reset is exported. Its value is = pi_lpddr2_n2	RW	0
21	LPDDR2_PTV_N3	LPDDR2IO NMOS PTV code bit 3 (Reset value exported from efuse) Note that reset is exported. Its value is = pi_lpddr2_n3	RW	0
20	LPDDR2_PTV_N4	LPDDR2IO NMOS PTV code bit 4 (Reset value exported from efuse) Note that reset is exported. Its value is = pi_lpddr2_n4	RW	0
19	LPDDR2_PTV_N5	LPDDR2IO NMOS PTV code bit 5 (Reset value exported from efuse) Note that reset is exported. Its value is = pi_lpddr2_n5	RW	0
18	LPDDR2_PTV_P1	LPDDR2IO PMOS PTV code bit 1 (Reset value exported from efuse) Note that reset is exported. Its value is = pi_lpddr2_p1	RW	0
17	LPDDR2_PTV_P2	LPDDR2IO PMOS PTV code bit 2 (Reset value exported from efuse) Note that reset is exported. Its value is = pi_lpddr2_p2	RW	0
16	LPDDR2_PTV_P3	LPDDR2IO PMOS PTV code bit 3 (Reset value exported from efuse) Note that reset is exported. Its value is = pi_lpddr2_p3	RW	0
15	LPDDR2_PTV_P4	LPDDR2IO PMOS PTV code bit 4 (Reset value exported from efuse) Note that reset is exported. Its value is = pi_lpddr2_p4	RW	0
14	LPDDR2_PTV_P5	LPDDR2IO PMOS PTV code bit 5 (Reset value exported from efuse) Note that reset is exported. Its value is = pi_lpddr2_p5	RW	0
13:0	RESERVED		R	0x0000

Table 18-673. Register Call Summary for Register CONTROL_EFUSE_2

Control Module Functional Description

- Signal Integrity Parameter Control Registers With Pad Group Assignment: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21]

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Table 18-673. Register Call Summary for Register CONTROL_EFUSE_2 (continued)

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- SYSCTRL_PADCONF_CORE Register Summary: [22]

Table 18-674. CONTROL_EFUSE_3

Address Offset	0x0000 0708		
Physical Address	0x4A10 0708	**Instance**	SYSCTRL_PADCONF_CORE
Description	EFUSE control 3 Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
STD_FUSE_SPARE_1	STD_FUSE_SPARE_2	STD_FUSE_SPARE_3	STD_FUSE_SPARE_4

Bits	Field Name	Description	Type	Reset
31:24	STD_FUSE_SPARE_1	std efuse spare bits (Read Only)	R	0x00
23:16	STD_FUSE_SPARE_2	std efuse spare bits (Read Only)	R	0x00
15:8	STD_FUSE_SPARE_3	std efuse spare bits (Read Only)	R	0x00
7:0	STD_FUSE_SPARE_4	std efuse spare bits (Read Only)	R	0x00

Table 18-675. Register Call Summary for Register CONTROL_EFUSE_3

Control Module Register Manual

- SYSCTRL_PADCONF_CORE Register Summary: [0]

Table 18-676. CONTROL_EFUSE_4

Address Offset	0x0000 070C		
Physical Address	0x4A10 070C	**Instance**	SYSCTRL_PADCONF_CORE
Description	EFUSE control 4 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
STD_FUSE_SPARE_5	STD_FUSE_SPARE_6	STD_FUSE_SPARE_7	STD_FUSE_SPARE_8

Bits	Field Name	Description	Type	Reset
31:24	STD_FUSE_SPARE_5	std efuse spare bits (RW) Note that reset is exported. Its value is = pi_std_fuse_spare5	RW	0x00
23:16	STD_FUSE_SPARE_6	std efuse spare bits (RW) Note that reset is exported. Its value is = pi_std_fuse_spare6	RW	0x00
15:8	STD_FUSE_SPARE_7	std efuse spare bits (RW) Note that reset is exported. Its value is = pi_std_fuse_spare7	RW	0x00
7:0	STD_FUSE_SPARE_8	std efuse spare bits (RW) Note that reset is exported. Its value is = pi_std_fuse_spare8	RW	0x00

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Table 18-677. Register Call Summary for Register CONTROL_EFUSE_4

Control Module Register Manual
• SYSCTRL_PADCONF_CORE Register Summary: [0]

18.6.8 SYSCTRL_PADCONF_WKUP Register Summary

Table 18-678. SYSCTRL_PADCONF_WKUP Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	SYSCTRL_PADCONF_WKUP Physical Address
CONTROL_PADCONF_WKUP_REVISION	R	32	0x0000 0000	0x4A31 E000
CONTROL_PADCONF_WKUP_HWINFO	R	32	0x0000 0004	0x4A31 E004
CONTROL_PADCONF_WKUP_SYSCONFIG	RW	32	0x0000 0010	0x4A31 E010
CONTROL_WKUP_PAD0_GPIO_WK0_PAD1_GPIO_WK1	RW	32	0x0000 0040	0x4A31 E040
CONTROL_WKUP_PAD0_GPIO_WK2_PAD1_GPIO_WK3	RW	32	0x0000 0044	0x4A31 E044
CONTROL_WKUP_PAD0_GPIO_WK4_PAD1_SR_SCL	RW	32	0x0000 0048	0x4A31 E048
CONTROL_WKUP_PAD0_SR_SDA_PAD1_FREF_XTAL_IN	RW	32	0x0000 004C	0x4A31 E04C
CONTROL_WKUP_PAD0_FREF_SLICER_IN_PAD1_FREF_CLK_IOREQ	RW	32	0x0000 0050	0x4A31 E050
CONTROL_WKUP_PAD0_FREF_CLK0_OUT_PAD1_FREF_CLK3_REQ	RW	32	0x0000 0054	0x4A31 E054
CONTROL_WKUP_PAD0_FREF_CLK3_OUT_PAD1_FREF_CLK4_REQ	RW	32	0x0000 0058	0x4A31 E058
CONTROL_WKUP_PAD0_FREF_CLK4_OUT_PAD1_SYS_32K	RW	32	0x0000 005C	0x4A31 E05C
CONTROL_WKUP_PAD0_SYS_NRESPWRON_PAD1_SYS_NRESWARM	RW	32	0x0000 0060	0x4A31 E060
CONTROL_WKUP_PAD0_SYS_PWR_REQ_PAD1_SYS_PWRON_RESET_OUT	RW	32	0x0000 0064	0x4A31 E064
CONTROL_WKUP_PAD0_SYS_BOOT6_PAD1_SYS_BOOT7	RW	32	0x0000 0068	0x4A31 E068
CONTROL_WKUP_PAD0_JTAG_NTRST_PAD1_JTAG_TCK	RW	32	0x0000 006C	0x4A31 E06C
CONTROL_WKUP_PAD0_JTAG_RTCK_PAD1_JTAG_TMS_TMSC	RW	32	0x0000 0070	0x4A31 E070
CONTROL_WKUP_PAD0_JTAG_TDI_PAD1_JTAG_TDO	RW	32	0x0000 0074	0x4A31 E074
CONTROL_WKUP_PADCONF_WAKEUPEVENT_0	R	32	0x0000 007C	0x4A31 E07C
CONTROL_SMART1NOPMIO_PADCONF_0	RW	32	0x0000 05A0	0x4A31 E5A0
CONTROL_SMART1NOPMIO_PADCONF_1	RW	32	0x0000 05A4	0x4A31 E5A4
CONTROL_WKUP_PADCONF_MODE	RW	32	0x0000 05A8	0x4A31 E5A8
CONTROL_XTAL_OSCILLATOR	RW	32	0x0000 05AC	0x4A31 E5AC
CONTROL_SMART3NOPMIO_PADCONF_0	RW	32	0x0000 05B0	0x4A31 E5B0

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Table 18-678. SYSCTRL_PADCONF_WKUP Register Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	SYSCTRL_PADCONF_WKUP Physical Address
CONTROL_SMART3NOPMIO_PADCONF_1	RW	32	0x0000 05B4	0x4A31 E5B4
CONTROL_GPIOWK	RW	32	0x0000 0600	0x4A31 E600
CONTROL_I2C_2	RW	32	0x0000 0604	0x4A31 E604
CONTROL_JTAG	RW	32	0x0000 0608	0x4A31 E608
CONTROL_SYS	RW	32	0x0000 060C	0x4A31 E60C
CONTROL_WKUP_CONTROL_SPARE_RW	RW	32	0x0000 0614	0x4A31 E614
CONTROL_WKUP_CONTROL_SPARE_R	R	32	0x0000 0618	0x4A31 E618
CONTROL_WKUP_CONTROL_SPARE_R_C0	RW	32	0x0000 061C	0x4A31 E61C
CONTROL_WKUP_CONTROL_SPARE_RW1	RW	32	0x0000 0620	0x4A31 E620
CONTROL_WKUP_CONTROL_SPARE_RW2	RW	32	0x0000 0624	0x4A31 E624
CONTROL_WKUP_CONTROL_SPARE_RW3	RW	32	0x0000 0628	0x4A31 E628
CONTROL_WKUP_CONTROL_SPARE_RW4	RW	32	0x0000 062C	0x4A31 E62C
CONTROL_WKUP_CONTROL_SPARE_RW5	RW	32	0x0000 0630	0x4A31 E630
CONTROL_WKUP_CONTROL_SPARE_RW6	RW	32	0x0000 0634	0x4A31 E634
CONTROL_WKUP_CONTROL_SPARE_RW7	RW	32	0x0000 0638	0x4A31 E638
CONTROL_WKUP_CONTROL_SPARE_RW8	RW	32	0x0000 063C	0x4A31 E63C
CONTROL_WKUP_CONTROL_SPARE_RW9	RW	32	0x0000 0640	0x4A31 E640
CONTROL_WKUP_CONTROL_SPARE_R1	R	32	0x0000 064C	0x4A31 E64C

18.6.9 SYSCTRL_PADCONF_WKUP Register Description

Table 18-679. CONTROL_PADCONF_WKUP_REVISION

Address Offset	0x0000 0000		
Physical Address	0x4A31 E000	**Instance**	SYSCTRL_PADCONF_WKUP
Description	Control module revision identifier Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP Revision	R	See(1)

(1) TI internal data

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Table 18-680. Register Call Summary for Register CONTROL_PADCONF_WKUP_REVISION

Control Module Register Manual

- SYSCTRL_PADCONF_WKUP Register Summary: [0]

Table 18-681. CONTROL_PADCONF_WKUP_HWINFO

Address Offset	0x0000 0004		
Physical Address	0x4A31 E004	**Instance**	SYSCTRL_PADCONF_WKUP
Description	Information about the IP module hardware configuration that is, typically the module HDL generics (if any). Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IP_HWINFO																															

Bits	Field Name	Description	Type	Reset
31:0	IP_HWINFO	IP-module dependent	R	0x0000 0000

Table 18-682. Register Call Summary for Register CONTROL_PADCONF_WKUP_HWINFO

Control Module Register Manual

- SYSCTRL_PADCONF_WKUP Register Summary: [0]

Table 18-683. CONTROL_PADCONF_WKUP_SYSCONFIG

Address Offset	0x0000 0010		
Physical Address	0x4A31 E010	**Instance**	SYSCTRL_PADCONF_WKUP
Description	Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												IP_SYSCONFIG_IDLEMODE		RESERVED	

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0000000
3:2	IP_SYSCONFIG_IDLEMODE	Select the local clock-gating strategy 0x0: Clock is manually gated 0x1: Clock is manually enabled 0x2,0x3: Clock is automatically gated when there is no access to the Control Module through L4-interconnect	RW	0x2
1:0	RESERVED		R	0x0

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Table 18-684. Register Call Summary for Register CONTROL_PADCONF_WKUP_SYSCONFIG

Control Module Functional Description • Device Wake-Up Control Module Instance: [0]
Control Module Programming Guide • Global Initialization: [1] • Operational Modes Configuration: [2]
Control Module Register Manual • SYSCTRL_PADCONF_WKUP Register Summary: [3]

Table 18-685. CONTROL_WKUP_PAD0_GPIO_WK0_PAD1_GPIO_WK1

Address Offset	0x0000 0040		
Physical Address	0x4A31 E040	**Instance**	SYSCTRL_PADCONF_WKUP
Description	Register control for Pads gpio_wk0 and gpio_wk1 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPIO_WK1_WAKEUPEVENT	GPIO_WK1_WAKEUPENABLE	RESERVED					GPIO_WK1_INPUTENABLE	RESERVED			GPIO_WK1_PULLTYPESELECT	GPIO_WK1_PULLUDENABLE	GPIO_WK1_MUXMODE			GPIO_WK0_WAKEUPEVENT	GPIO_WK0_WAKEUPENABLE	RESERVED					GPIO_WK0_INPUTENABLE	RESERVED			GPIO_WK0_PULLTYPESELECT	GPIO_WK0_PULLUDENABLE	GPIO_WK0_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	GPIO_WK1_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	GPIO_WK1_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x00
24	GPIO_WK1_INPUTENABLE	Input enable value for pad gpio_wk1 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	GPIO_WK1_PULLTYPESELECT	pullup/down selection for pad gpio_wk1 0x0: pulldown selected 0x1: pullup selected	RW	0
19	GPIO_WK1_PULLUDENABLE	pullup/down enable for pad gpio_wk1 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1

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Bits	Field Name	Description	Type	Reset
18:16	GPIO_WK1_MUXMODE	Functional multiplexing selection for pad gpio_wk1 0x0: Reserved 0x3: Select gpio_wk1 0x6: Select hw_dbg2 0x7: Select safe_mode	RW	0x7
15	GPIO_WK0_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	GPIO_WK0_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x00
8	GPIO_WK0_INPUTENABLE	Input enable value for pad gpio_wk0 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	GPIO_WK0_PULLTYPESELECT	pullup/down selection for pad gpio_wk0 0x0: pulldown selected 0x1: pullup selected	RW	0
3	GPIO_WK0_PULLUDENABLE	pullup/down enable for pad gpio_wk0 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	GPIO_WK0_MUXMODE	Functional multiplexing selection for pad gpio_wk0 0x0: Reserved 0x3: Select gpio_wk0 0x4: Select c2c_pwkup 0x6: Select hw_dbg1 0x7: Select safe_mode	RW	0x7

Table 18-686. Register Call Summary for Register CONTROL_WKUP_PAD0_GPIO_WK0_PAD1_GPIO_WK1

Control Module Functional Description • Pad Multiplexing Register Fields: [0] [1] • Observability Signals Multiplexing at Device Control Module Level: [2]
Control Module Register Manual • SYSCTRL_PADCONF_WKUP Register Summary: [3]

Table 18-687. CONTROL_WKUP_PAD0_GPIO_WK2_PAD1_GPIO_WK3

Address Offset	0x0000 0044		
Physical Address	0x4A31 E044	**Instance**	SYSCTRL_PADCONF_WKUP
Description	Register control for Pads gpio_wk2 and gpio_wk3 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPIO_WK3_WAKEUPEVENT	GPIO_WK3_WAKEUPENABLE	RESERVED					GPIO_WK3_INPUTENABLE	RESERVED			GPIO_WK3_PULLTYPESELECT	GPIO_WK3_PULLUDENABLE	GPIO_WK3_MUXMODE			GPIO_WK2_WAKEUPEVENT	GPIO_WK2_WAKEUPENABLE	RESERVED					GPIO_WK2_INPUTENABLE	RESERVED			GPIO_WK2_PULLTYPESELECT	GPIO_WK2_PULLUDENABLE	GPIO_WK2_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	GPIO_WK3_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	GPIO_WK3_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x00
24	GPIO_WK3_INPUTENABLE	Input enable value for pad gpio_wk3 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	GPIO_WK3_PULLTYPESELECT	pullup/down selection for pad gpio_wk3 0x0: pulldown selected 0x1: pullup selected	RW	1
19	GPIO_WK3_PULLUDENABLE	pullup/down enable for pad gpio_wk3 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	GPIO_WK3_MUXMODE	Functional multiplexing selection for pad gpio_wk3 0x0: Reserved 0x3: Select gpio_wk3 0x6: Select hw_dbg4 0x7: Select safe_mode	RW	0x7
15	GPIO_WK2_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	GPIO_WK2_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x00
8	GPIO_WK2_INPUTENABLE	Input enable value for pad gpio_wk2 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	GPIO_WK2_PULLTYPESELECT	pullup/down selection for pad gpio_wk2 0x0: pulldown selected 0x1: pullup selected	RW	0

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Bits	Field Name	Description	Type	Reset
3	GPIO_WK2_PULLUDENABLE	pullup/down enable for pad gpio_wk2 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	GPIO_WK2_MUXMODE	Functional multiplexing selection for pad gpio_wk2 0x0: Reserved 0x3: Select gpio_wk2 0x6: Select hw_dbg3 0x7: Select safe_mode	RW	0x7

Table 18-688. Register Call Summary for Register CONTROL_WKUP_PAD0_GPIO_WK2_PAD1_GPIO_WK3

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]
- Observability Signals Multiplexing at Device Control Module Level: [2]

Control Module Register Manual
- SYSCTRL_PADCONF_WKUP Register Summary: [3]

Table 18-689. CONTROL_WKUP_PAD0_GPIO_WK4_PAD1_SR_SCL

Address Offset	0x0000 0048		
Physical Address	0x4A31 E048	**Instance**	SYSCTRL_PADCONF_WKUP
Description	Register control for Pads gpio_wk4 and sr_scl Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SR_SCL_WAKEUPEVENT	SR_SCL_WAKEUPENABLE	RESERVED					SR_SCL_INPUTENABLE	RESERVED			SR_SCL_PULLTYPESELECT	SR_SCL_PULLUDENABLE	RESERVED			GPIO_WK4_WAKEUPEVENT	GPIO_WK4_WAKEUPENABLE	RESERVED					GPIO_WK4_INPUTENABLE	RESERVED			GPIO_WK4_PULLTYPESELECT	GPIO_WK4_PULLUDENABLE	GPIO_WK4_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	SR_SCL_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	SR_SCL_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x00
24	SR_SCL_INPUTENABLE	Input enable value for pad sr_scl 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
20	SR_SCL_PULLTYPESELECT	pullup/down selection for pad sr_scl 0x0: pulldown selected 0x1: pullup selected	RW	0
19	SR_SCL_PULLUDENABLE	pullup/down enable for pad sr_scl 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	0
18:16	RESERVED		R	0x0
15	GPIO_WK4_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	GPIO_WK4_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x00
8	GPIO_WK4_INPUTENABLE	Input enable value for pad gpio_wk4 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	GPIO_WK4_PULLTYPESELECT	pullup/down selection for pad gpio_wk4 0x0: pulldown selected 0x1: pullup selected	RW	0
3	GPIO_WK4_PULLUDENABLE	pullup/down enable for pad gpio_wk4 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	GPIO_WK4_MUXMODE	Functional multiplexing selection for pad gpio_wk4 0x0: Reserved 0x3: Select gpio_wk4 0x6: Select hw_dbg5 0x7: Select safe_mode	RW	0x7

Table 18-690. Register Call Summary for Register CONTROL_WKUP_PAD0_GPIO_WK4_PAD1_SR_SCL

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]
- Observability Signals Multiplexing at Device Control Module Level: [2]

Control Module Register Manual
- SYSCTRL_PADCONF_WKUP Register Summary: [3]

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Table 18-691. CONTROL_WKUP_PAD0_SR_SDA_PAD1_FREF_XTAL_IN

Address Offset	0x0000 004C		
Physical Address	0x4A31 E04C	**Instance**	SYSCTRL_PADCONF_WKUP
Description	Register control for Pads sr_sda and fref_xtal_in Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													FREF_XTAL_IN_MUXMODE			SR_SDA_WAKEUPEVENT	SR_SDA_WAKEUPENABLE	RESERVED					SR_SDA_INPUTENABLE	RESERVED			SR_SDA_PULLTYPESELECT	SR_SDA_PULLUDENABLE	RESERVED		

Bits	Field Name	Description	Type	Reset
31:19	RESERVED		R	0x0000
18:16	FREF_XTAL_IN_MUXMODE	Functional multiplexing selection for pad fref_xtal_in 0x0: Select fref_xtal_in 0x4: Select c2c_wakereqin	RW	0x0
15	SR_SDA_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	SR_SDA_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x00
8	SR_SDA_INPUTENABLE	Input enable value for pad sr_sda 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	SR_SDA_PULLTYPESELECT	pullup/down selection for pad sr_sda 0x0: pulldown selected 0x1: pullup selected	RW	0
3	SR_SDA_PULLUDENABLE	pullup/down enable for pad sr_sda 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	0
2:0	RESERVED		R	0x0

Table 18-692. Register Call Summary for Register CONTROL_WKUP_PAD0_SR_SDA_PAD1_FREF_XTAL_IN

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- SYSCTRL_PADCONF_WKUP Register Summary: [2]

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Table 18-693. CONTROL_WKUP_PAD0_FREF_SLICER_IN_PAD1_FREF_CLK_IOREQ

Address Offset	0x0000 0050		
Physical Address	0x4A31 E050	**Instance**	SYSCTRL_PADCONF_WKUP
Description	Register control for Pads fref_slicer_in and fref_clk_ioreq Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FREF_CLK_IOREQ_WAKEUPEVENT	FREF_CLK_IOREQ_WAKEUPENABLE	RESERVED					FREF_CLK_IOREQ_INPUTENABLE	RESERVED			FREF_CLK_IOREQ_PULLTYPESELECT	FREF_CLK_IOREQ_PULLUDENABLE	RESERVED																FREF_SLICER_IN_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	FREF_CLK_IOREQ_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	FREF_CLK_IOREQ_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x00
24	FREF_CLK_IOREQ_INPUTENABLE	Input enable value for pad fref_clk_ioreq 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	FREF_CLK_IOREQ_PULLTYPESELECT	pullup/down selection for pad fref_clk_ioreq 0x0: pulldown selected 0x1: pullup selected	RW	0
19	FREF_CLK_IOREQ_PULLUDENABLE	pullup/down enable for pad fref_clk_ioreq 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:3	RESERVED		R	0x0000
2:0	FREF_SLICER_IN_MUXMODE	Functional multiplexing selection for pad fref_slicer_in 0x0: Select fref_slicer_in 0x3: Select gpi_wk5 0x4: Select c2c_wakereqin 0x7: Select safe_mode	RW	0x0

Table 18-694. Register Call Summary for Register CONTROL_WKUP_PAD0_FREF_SLICER_IN_PAD1_FREF_CLK_IOREQ

Control Module Functional Description

- Pad Multiplexing Register Fields: [0] [1]

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Table 18-694. Register Call Summary for Register CONTROL_WKUP_PAD0_FREF_SLICER_IN_PAD1_FREF_CLK_IOREQ (continued)

Control Module Register Manual

- SYSCTRL_PADCONF_WKUP Register Summary: [2]

Table 18-695. CONTROL_WKUP_PAD0_FREF_CLK0_OUT_PAD1_FREF_CLK3_REQ

Address Offset	0x0000 0054		
Physical Address	0x4A31 E054	**Instance**	SYSCTRL_PADCONF_WKUP
Description	Register control for Pads fref_clk0_out and fref_clk3_req Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FREF_CLK3_REQ_WAKEUPEVENT	FREF_CLK3_REQ_WAKEUPENABLE	RESERVED					FREF_CLK3_REQ_INPUTENABLE	RESERVED			FREF_CLK3_REQ_PULLTYPESELECT	FREF_CLK3_REQ_PULLUDENABLE	FREF_CLK3_REQ_MUXMODE			FREF_CLK0_OUT_WAKEUPEVENT	FREF_CLK0_OUT_WAKEUPENABLE	RESERVED					FREF_CLK0_OUT_INPUTENABLE	RESERVED			FREF_CLK0_OUT_PULLTYPESELECT	FREF_CLK0_OUT_PULLUDENABLE	FREF_CLK0_OUT_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	FREF_CLK3_REQ_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	FREF_CLK3_REQ_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x00
24	FREF_CLK3_REQ_INPUTENABLE	Input enable value for pad fref_clk3_req 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	FREF_CLK3_REQ_PULLTYPESELECT	pullup/down selection for pad fref_clk3_req 0x0: pulldown selected 0x1: pullup selected	RW	0
19	FREF_CLK3_REQ_PULLUDENABLE	pullup/down enable for pad fref_clk3_req 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1

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Bits	Field Name	Description	Type	Reset
18:16	FREF_CLK3_REQ_MUXMODE	Functional multiplexing selection for pad fref_clk3_req 0x0: Select fref_clk3_req 0x1: Select fref_clk1_req 0x2: Reserved 0x3: Select gpio_wk30 0x4: Select c2c_wakereqin 0x5: Select sdmmc2_dat4 0x6: Select hw_dbg7 0x7: Select safe_mode	RW	0x7
15	FREF_CLK0_OUT_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	FREF_CLK0_OUT_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x00
8	FREF_CLK0_OUT_INPUTENABLE	Input enable value for pad fref_clk0_out 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	FREF_CLK0_OUT_PULLTYPESELECT	pullup/down selection for pad fref_clk0_out 0x0: pulldown selected 0x1: pullup selected	RW	0
3	FREF_CLK0_OUT_PULLUDENABLE	pullup/down enable for pad fref_clk0_out 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	FREF_CLK0_OUT_MUXMODE	Functional multiplexing selection for pad fref_clk0_out 0x0: Select fref_clk0_out 0x1: Select fref_clk1_req 0x2: Reserved 0x3: Select gpio_wk6 0x5: Select sdmmc2_dat7 0x6: Select hw_dbg6 0x7: Select safe_mode	RW	0x7

Table 18-696. Register Call Summary for Register CONTROL_WKUP_PAD0_FREF_CLK0_OUT_PAD1_FREF_CLK3_REQ

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]
- Observability Signals Multiplexing at Device Control Module Level: [2]

Control Module Register Manual
- SYSCTRL_PADCONF_WKUP Register Summary: [3]

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Table 18-697. CONTROL_WKUP_PAD0_FREF_CLK3_OUT_PAD1_FREF_CLK4_REQ

Address Offset	0x0000 0058		
Physical Address	0x4A31 E058	**Instance**	SYSCTRL_PADCONF_WKUP
Description	Register control for Pads fref_clk3_out and fref_clk4_req Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FREF_CLK4_REQ_WAKEUPEVENT	FREF_CLK4_REQ_WAKEUPENABLE	RESERVED					FREF_CLK4_REQ_INPUTENABLE	RESERVED			FREF_CLK4_REQ_PULLTYPESELECT	FREF_CLK4_REQ_PULLUDENABLE	FREF_CLK4_REQ_MUXMODE			FREF_CLK3_OUT_WAKEUPEVENT	FREF_CLK3_OUT_WAKEUPENABLE	RESERVED					FREF_CLK3_OUT_INPUTENABLE	RESERVED			FREF_CLK3_OUT_PULLTYPESELECT	FREF_CLK3_OUT_PULLUDENABLE			

Bits	Field Name	Description	Type	Reset
31	FREF_CLK4_REQ_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	FREF_CLK4_REQ_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x00
24	FREF_CLK4_REQ_INPUTENABLE	Input enable value for pad fref_clk4_req 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	FREF_CLK4_REQ_PULLTYPESELECT	pullup/down selection for pad fref_clk4_req 0x0: pulldown selected 0x1: pullup selected	RW	0
19	FREF_CLK4_REQ_PULLUDENABLE	pullup/down enable for pad fref_clk4_req 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	FREF_CLK4_REQ_MUXMODE	Functional multiplexing selection for pad fref_clk4_req 0x0: Select fref_clk4_req 0x1: Select fref_clk5_out 0x3: Select gpio_wk7 0x5: Select sdmmc2_dat6 0x6: Select hw_dbg9	RW	0x0
15	FREF_CLK3_OUT_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0

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Bits	Field Name	Description	Type	Reset
14	FREF_CLK3_OUT_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x00
8	FREF_CLK3_OUT_INPUTENABLE	Input enable value for pad fref_clk3_out 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	FREF_CLK3_OUT_PULLTYPESELECT	pullup/down selection for pad fref_clk3_out 0x0: pulldown selected 0x1: pullup selected	RW	0
3	FREF_CLK3_OUT_PULLUDENABLE	pullup/down enable for pad fref_clk3_out 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	FREF_CLK3_OUT_MUXMODE	Functional multiplexing selection for pad fref_clk3_out 0x0: Select fref_clk3_out 0x1: Select fref_clk2_req 0x2: Reserved 0x3: Select gpio_wk31 0x4: Select c2c_wakereqout 0x5: Select sdmmc2_dat5 0x6: Select hw_dbg8 0x7: Select safe_mode	RW	0x7

Table 18-698. Register Call Summary for Register CONTROL_WKUP_PAD0_FREF_CLK3_OUT_PAD1_FREF_CLK4_REQ

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]
- Observability Signals Multiplexing at Device Control Module Level: [2]

Control Module Register Manual
- SYSCTRL_PADCONF_WKUP Register Summary: [3]

Table 18-699. CONTROL_WKUP_PAD0_FREF_CLK4_OUT_PAD1_SYS_32K

Address Offset	0x0000 005C		
Physical Address	0x4A31 E05C	**Instance**	SYSCTRL_PADCONF_WKUP
Description	Register control for Pads fref_clk4_out and sys_32k Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SYS_32K_WAKEUPEVENT	SYS_32K_WAKEUPENABLE	RESERVED					SYS_32K_INPUTENABLE	RESERVED			SYS_32K_PULLTYPESELECT	SYS_32K_PULLUDENABLE	RESERVED			FREF_CLK4_OUT_WAKEUPEVENT	FREF_CLK4_OUT_WAKEUPENABLE	RESERVED					FREF_CLK4_OUT_INPUTENABLE	RESERVED			FREF_CLK4_OUT_PULLTYPESELECT	FREF_CLK4_OUT_PULLUDENABLE	FREF_CLK4_OUT_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	SYS_32K_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	SYS_32K_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x00
24	SYS_32K_INPUTENABLE	Input enable value for pad sys_32k 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	SYS_32K_PULLTYPESELECT	pullup/down selection for pad sys_32k 0x0: pulldown selected 0x1: pullup selected	RW	0
19	SYS_32K_PULLUDENABLE	pullup/down enable for pad sys_32k 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	0
18:16	RESERVED		R	0x0
15	FREF_CLK4_OUT_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	FREF_CLK4_OUT_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x00
8	FREF_CLK4_OUT_INPUTENABLE	Input enable value for pad fref_clk4_out 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	FREF_CLK4_OUT_PULLTYPESELECT	pullup/down selection for pad fref_clk4_out 0x0: pulldown selected 0x1: pullup selected	RW	0

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Bits	Field Name	Description	Type	Reset
3	FREF_CLK4_OUT_PULLUDENABLE	pullup/down enable for pad fref_clk4_out 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	FREF_CLK4_OUT_MUXMODE	Functional multiplexing selection for pad fref_clk4_out 0x0: Select fref_clk4_out 0x3: Select gpio_wk8 0x6: Select hw_dbg10	RW	0x0

Table 18-700. Register Call Summary for Register CONTROL_WKUP_PAD0_FREF_CLK4_OUT_PAD1_SYS_32K

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]
- Observability Signals Multiplexing at Device Control Module Level: [2]

Control Module Register Manual
- SYSCTRL_PADCONF_WKUP Register Summary: [3]

Table 18-701. CONTROL_WKUP_PAD0_SYS_NRESPWRON_PAD1_SYS_NRESWARM

Address Offset	0x0000 0060		
Physical Address	0x4A31 E060	**Instance**	SYSCTRL_PADCONF_WKUP
Description	Register control for Pads sys_nreswarm Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SYS_NRESWARM_WAKEUPEVENT	SYS_NRESWARM_WAKEUPENABLE	RESERVED																													

Bits	Field Name	Description	Type	Reset
31	SYS_NRESWARM_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	SYS_NRESWARM_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:0	RESERVED		R	0x0000000

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Table 18-702. Register Call Summary for Register CONTROL_WKUP_PAD0_SYS_NRESPWRON_PAD1_SYS_NRESWARM

Control Module Functional Description • Pad Multiplexing Register Fields: [0] [1]
Control Module Register Manual • SYSCTRL_PADCONF_WKUP Register Summary: [2]

Table 18-703. CONTROL_WKUP_PAD0_SYS_PWR_REQ_PAD1_SYS_PWRON_RESET_OUT

Address Offset	0x0000 0064		
Physical Address	0x4A31 E064	**Instance**	SYSCTRL_PADCONF_WKUP
Description	Register control for Pads sys_pwr_req and sys_pwron_reset_out Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SYS_PWRON_RESET_OUT_WAKEUPEVENT	SYS_PWRON_RESET_OUT_WAKEUPENABLE	RESERVED					SYS_PWRON_RESET_OUT_INPUTENABLE	RESERVED			SYS_PWRON_RESET_OUT_PULLTYPESELECT	SYS_PWRON_RESET_OUT_PULLUDENABLE	SYS_PWRON_RESET_OUT_MUXMODE			SYS_PWR_REQ_WAKEUPEVENT	SYS_PWR_REQ_WAKEUPENABLE	RESERVED					SYS_PWR_REQ_INPUTENABLE	RESERVED				SYS_PWR_REQ_PULLTYPESELECT	SYS_PWR_REQ_PULLUDENABLE	RESERVED		

Bits	Field Name	Description	Type	Reset
31	SYS_PWRON_RESET_OUT_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	SYS_PWRON_RESET_OUT_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x00
24	SYS_PWRON_RESET_OUT_INPUTENABLE	Input enable value for pad sys_pwron_reset_out 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	SYS_PWRON_RESET_OUT_PULLTYPESELECT	pullup/down selection for pad sys_pwron_reset_out 0x0: pulldown selected 0x1: pullup selected	RW	0
19	SYS_PWRON_RESET_OUT_PULLUDENABLE	pullup/down enable for pad sys_pwron_reset_out 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1

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Bits	Field Name	Description	Type	Reset
18:16	SYS_PWRON_ RESET_OUT_MUXMODE	Functional multiplexing selection for pad sys_pwron_reset_out 0x0: Select sys_pwron_reset_out 0x3: Select gpio_wk29 0x5: Select hw_dbg0 0x6: Select hw_dbg11	RW	0x0
15	SYS_PWR_ REQ_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	SYS_PWR_ REQ_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x00
8	SYS_PWR_ REQ_INPUTENABLE	Input enable value for pad sys_pwr_req 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	SYS_PWR_ REQ_PULLTYPESELECT	pullup/down selection for pad sys_pwr_req 0x0: pulldown selected 0x1: pullup selected	RW	1
3	SYS_PWR_ REQ_PULLUDENABLE	pullup/down enable for pad sys_pwr_req 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	RESERVED		R	0x0

Table 18-704. Register Call Summary for Register CONTROL_WKUP_PAD0_SYS_PWR_REQ_PAD1_SYS_PWRON_RESET_OUT

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]
- Observability Signals Multiplexing at Device Control Module Level: [2] [3]

Control Module Register Manual
- SYSCTRL_PADCONF_WKUP Register Summary: [4]

Table 18-705. CONTROL_WKUP_PAD0_SYS_BOOT6_PAD1_SYS_BOOT7

Address Offset	0x0000 0068		
Physical Address	0x4A31 E068	**Instance**	SYSCTRL_PADCONF_WKUP
Description	Register control for Pads sys_boot6 and sys_boot7 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SYS_BOOT7_WAKEUPEVENT	SYS_BOOT7_WAKEUPENABLE	RESERVED					SYS_BOOT7_INPUTENABLE	RESERVED			SYS_BOOT7_PULLTYPESELECT	SYS_BOOT7_PULLUDENABLE	SYS_BOOT7_MUXMODE			SYS_BOOT6_WAKEUPEVENT	SYS_BOOT6_WAKEUPENABLE	RESERVED					SYS_BOOT6_INPUTENABLE	RESERVED			SYS_BOOT6_PULLTYPESELECT	SYS_BOOT6_PULLUDENABLE	SYS_BOOT6_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	SYS_BOOT7_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	SYS_BOOT7_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x00
24	SYS_BOOT7_INPUTENABLE	Input enable value for pad sys_boot7 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	SYS_BOOT7_PULLTYPESELECT	pullup/down selection for pad sys_boot7 0x0: pulldown selected 0x1: pullup selected	RW	0
19	SYS_BOOT7_PULLUDENABLE	pullup/down enable for pad sys_boot7 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	0
18:16	SYS_BOOT7_MUXMODE	Functional multiplexing selection for pad sys_boot7 0x0: Select sys_boot7 0x1: Select dpm_emu19 0x3: Select gpio_wk10 0x6: Select hw_dbg13 0x7: Select safe_mode	RW	0x0
15	SYS_BOOT6_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	SYS_BOOT6_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x00
8	SYS_BOOT6_INPUTENABLE	Input enable value for pad sys_boot6 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
4	SYS_BOOT6_PULLTYPESELECT	pullup/down selection for pad sys_boot6 0x0: pulldown selected 0x1: pullup selected	RW	0
3	SYS_BOOT6_PULLUDENABLE	pullup/down enable for pad sys_boot6 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	0
2:0	SYS_BOOT6_MUXMODE	Functional multiplexing selection for pad sys_boot6 0x0: Select sys_boot6 0x1: Select dpm_emu18 0x3: Select gpio_wk9 0x4: Select c2c_wakereqout 0x6: Select hw_dbg12 0x7: Select safe_mode	RW	0x0

Table 18-706. Register Call Summary for Register CONTROL_WKUP_PAD0_SYS_BOOT6_PAD1_SYS_BOOT7

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]
- Observability Signals Multiplexing at Device Control Module Level: [2]

Control Module Register Manual
- SYSCTRL_PADCONF_WKUP Register Summary: [3]

Table 18-707. CONTROL_WKUP_PAD0_JTAG_NTRST_PAD1_JTAG_TCK

Address Offset	0x0000 006C		
Physical Address	0x4A31 E06C	**Instance**	SYSCTRL_PADCONF_WKUP
Description	Register control for Pads jtag_ntrst and jtag_tck Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
JTAG_TCK_WAKEUPEVENT	JTAG_TCK_WAKEUPENABLE	RESERVED					JTAG_TCK_INPUTENABLE	RESERVED			JTAG_TCK_PULLTYPESELECT	JTAG_TCK_PULLUDENABLE	JTAG_TCK_MUXMODE			JTAG_NTRST_WAKEUPEVENT	JTAG_NTRST_WAKEUPENABLE	RESERVED				JTAG_NTRST_INPUTENABLE	RESERVED			JTAG_NTRST_PULLTYPESELECT	JTAG_NTRST_PULLUDENABLE	RESERVED			

Bits	Field Name	Description	Type	Reset
31	JTAG_TCK_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	JTAG_TCK_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0

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Bits	Field Name	Description	Type	Reset
29:25	RESERVED		R	0x00
24	JTAG_TCK_INPUTENABLE	Input enable value for pad jtag_tck 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	JTAG_TCK_PULLTYPESELECT	pullup/down selection for pad jtag_tck 0x0: pulldown selected 0x1: pullup selected	RW	0
19	JTAG_TCK_PULLUDENABLE	pullup/down enable for pad jtag_tck 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	JTAG_TCK_MUXMODE	Functional multiplexing selection for pad jtag_tck 0x0: Select jtag_tck 0x7: Select safe_mode	RW	0x0
15	JTAG_NTRST_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	JTAG_NTRST_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x00
8	JTAG_NTRST_INPUTENABLE	Input enable value for pad jtag_ntrst 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	JTAG_NTRST_PULLTYPESELECT	pullup/down selection for pad jtag_ntrst 0x0: pulldown selected 0x1: pullup selected	RW	0
3	JTAG_NTRST_PULLUDENABLE	pullup/down enable for pad jtag_ntrst 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	RESERVED		R	0x0

Table 18-708. Register Call Summary for Register CONTROL_WKUP_PAD0_JTAG_NTRST_PAD1_JTAG_TCK

Control Module Functional Description • Pad Multiplexing Register Fields: [0] [1]
Control Module Register Manual • SYSCTRL_PADCONF_WKUP Register Summary: [2]

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Table 18-709. CONTROL_WKUP_PAD0_JTAG_RTCK_PAD1_JTAG_TMS_TMSC

Address Offset	0x0000 0070		
Physical Address	0x4A31 E070	**Instance**	SYSCTRL_PADCONF_WKUP
Description	Register control for Pads jtag_rtck and jtag_tms_tmsc Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
JTAG_TMS_TMSC_WAKEUPEVENT	JTAG_TMS_TMSC_WAKEUPENABLE	RESERVED					JTAG_TMS_TMSC_INPUTENABLE	RESERVED					JTAG_TMS_TMSC_MUXMODE			JTAG_RTCK_WAKEUPEVENT	JTAG_RTCK_WAKEUPENABLE	RESERVED						JTAG_RTCK_PULLTYPESELECT	JTAG_RTCK_PULLUDENABLE	RESERVED					

Bits	Field Name	Description	Type	Reset
31	JTAG_TMS_TMSC_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	JTAG_TMS_TMSC_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x00
24	JTAG_TMS_TMSC_INPUTENABLE	Input enable value for pad jtag_tms_tmsc 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
23:19	RESERVED		R	0x00
18:16	JTAG_TMS_TMSC_MUXMODE	Functional multiplexing selection for pad jtag_tms_tmsc 0x0: Select jtag_tms_tmsc 0x7: Select safe_mode	RW	0x0
15	JTAG_RTCK_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	JTAG_RTCK_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:5	RESERVED		R	0x000
4	JTAG_RTCK_PULLTYPESELECT	pullup/down selection for pad jtag_rtck 0x0: pulldown selected 0x1: pullup selected	RW	0
3	JTAG_RTCK_PULLUDENABLE	pullup/down enable for pad jtag_rtck 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1

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Bits	Field Name	Description	Type	Reset
2:0	RESERVED		R	0x0

Table 18-710. Register Call Summary for Register CONTROL_WKUP_PAD0_JTAG_RTCK_PAD1_JTAG_TMS_TMSC

Control Module Functional Description

- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual

- SYSCTRL_PADCONF_WKUP Register Summary: [2]

Table 18-711. CONTROL_WKUP_PAD0_JTAG_TDI_PAD1_JTAG_TDO

Address Offset	0x0000 0074		
Physical Address	0x4A31 E074	**Instance**	SYSCTRL_PADCONF_WKUP
Description	Register control for Pads jtag_tdi and jtag_tdo Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
JTAG_TDO_WAKEUPEVENT	JTAG_TDO_WAKEUPENABLE	RESERVED					JTAG_TDO_INPUTENABLE	RESERVED			JTAG_TDO_PULLTYPESELECT	JTAG_TDO_PULLUDENABLE	RESERVED			JTAG_TDI_WAKEUPEVENT	JTAG_TDI_WAKEUPENABLE	RESERVED					JTAG_TDI_INPUTENABLE	RESERVED			JTAG_TDI_PULLTYPESELECT	JTAG_TDI_PULLUDENABLE	RESERVED		

Bits	Field Name	Description	Type	Reset
31	JTAG_TDO_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	JTAG_TDO_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x000
24	JTAG_TDO_INPUTENABLE	Input enable value for pad jtag_tdo 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	0x1
23:21	RESERVED		R	0x000
20	JTAG_TDO_PULLTYPESELECT	pullup/down selection for pad jtag_tdo 0x0: pulldown selected 0x1: pullup selected	RW	1
19	JTAG_TDO_PULLUDENABLE	pullup/down enable for pad jtag_tdo 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
15	JTAG_TDI_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	JTAG_TDI_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x00
8	JTAG_TDI_INPUTENABLE	Input enable value for pad jtag_tdi 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	JTAG_TDI_PULLTYPESELECT	pullup/down selection for pad jtag_tdi 0x0: pulldown selected 0x1: pullup selected	RW	1
3	JTAG_TDI_PULLUDENABLE	pullup/down enable for pad jtag_tdi 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	RESERVED		R	0x0

Table 18-712. Register Call Summary for Register CONTROL_WKUP_PAD0_JTAG_TDI_PAD1_JTAG_TDO

Control Module Functional Description • Pad Multiplexing Register Fields: [0] [1]
Control Module Register Manual • SYSCTRL_PADCONF_WKUP Register Summary: [2]

Table 18-713. CONTROL_WKUP_PADCONF_WAKEUPEVENT_0

Address Offset	0x0000 007C		
Physical Address	0x4A31 E07C	**Instance**	SYSCTRL_PADCONF_WKUP
Description	Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							JTAG_TDO_DUPLICATEWAKEUPEVENT	JTAG_TDI_DUPLICATEWAKEUPEVENT	JTAG_TMS_TMSC_DUPLICATEWAKEUPEVENT	JTAG_RTCK_DUPLICATEWAKEUPEVENT	JTAG_TCK_DUPLICATEWAKEUPEVENT	JTAG_NTRST_DUPLICATEWAKEUPEVENT	SYS_BOOT7_DUPLICATEWAKEUPEVENT	SYS_BOOT6_DUPLICATEWAKEUPEVENT	SYS_PWRON_RESET_OUT_DUPLICATEWAKEUPEVENT	SYS_PWR_REQ_DUPLICATEWAKEUPEVENT	SYS_NRESWARM_DUPLICATEWAKEUPEVENT	SYS_32K_DUPLICATEWAKEUPEVENT	FREF_CLK4_OUT_DUPLICATEWAKEUPEVENT	FREF_CLK4_REQ_DUPLICATEWAKEUPEVENT	FREF_CLK3_OUT_DUPLICATEWAKEUPEVENT	FREF_CLK3_REQ_DUPLICATEWAKEUPEVENT	FREF_CLK0_OUT_DUPLICATEWAKEUPEVENT	FREF_CLK_IOREQ_DUPLICATEWAKEUPEVENT	SR_SDA_DUPLICATEWAKEUPEVENT	SR_SCL_DUPLICATEWAKEUPEVENT	GPIO_WK4_DUPLICATEWAKEUPEVENT	GPIO_WK3_DUPLICATEWAKEUPEVENT	GPIO_WK2_DUPLICATEWAKEUPEVENT	GPIO_WK1_DUPLICATEWAKEUPEVENT	GPIO_WK0_DUPLICATEWAKEUPEVENT

Bits	Field Name	Description	Type	Reset
31:25	RESERVED		R	0x00
24	JTAG_TDO_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad jtag_tdo Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
23	JTAG_TDI_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad jtag_tdi Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
22	JTAG_TMS_TMSC_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad jtag_tms_tmsc Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
21	JTAG_RTCK_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad jtag_rtck Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
20	JTAG_TCK_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad jtag_tck Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
19	JTAG_NTRST_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad jtag_ntrst Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
18	SYS_BOOT7_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad sys_boot7 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
17	SYS_BOOT6_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad sys_boot6 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0

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Bits	Field Name	Description	Type	Reset
16	SYS_PWRON_RESET_OUT_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad sys_pwron_reset_out Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
15	SYS_PWR_REQ_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad sys_pwr_req Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	SYS_NRESWARM_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad sys_nreswarm Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
13	SYS_32K_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad sys_32k Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
12	FREF_CLK4_OUT_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad fref_clk4_out Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
11	FREF_CLK4_REQ_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad fref_clk4_req Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
10	FREF_CLK3_OUT_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad fref_clk3_out Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
9	FREF_CLK3_REQ_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad fref_clk3_req Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
8	FREF_CLK0_OUT_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad fref_clk0_out Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
7	FREF_CLK_IOREQ_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad fref_clk_ioreq Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
6	SR_SDA_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad sr_sda Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
5	SR_SCL_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad sr_scl Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
4	GPIO_WK4_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad gpio_wk4 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
3	GPIO_WK3_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad gpio_wk3 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0

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Bits	Field Name	Description	Type	Reset
2	GPIO_WK2_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad gpio_wk2 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
1	GPIO_WK1_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad gpio_wk1 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
0	GPIO_WK0_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad gpio_wk0 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0

Table 18-714. Register Call Summary for Register CONTROL_WKUP_PADCONF_WAKEUPEVENT_0

Control Module Register Manual

- SYSCTRL_PADCONF_WKUP Register Summary: [0]

Table 18-715. CONTROL_SMART1NOPMIO_PADCONF_0

Address Offset	0x0000 05A0		
Physical Address	0x4A31 E5A0	**Instance**	SYSCTRL_PADCONF_WKUP
Description	SMART1 NOPM I/O control 0 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31 30	29 28 27 26 25 24	23 22 21 20	19 18	17 16	15 14	13 12	11 10 9 8	7 6 5 4 3 2 1 0
FREF_DR0_SC	RESERVED		GPIO_DR7_SC	RESERVED	DPM_DR0_SC	GPIOWK4_DR0_SC	RESERVED	

Bits	Field Name	Description	Type	Reset
31:30	FREF_DR0_SC	Slew rate control for group fref_dr0 Refer to Section 18.4.12.9.3, section Low Speed I/Os Combined Slew Rate vs TL Length and Load Settings for more details on SR settings.	RW	0x0
29:20	RESERVED		R	0x000
19:18	GPIO_DR7_SC	Slew rate control for group gpio_dr7 Refer to Section 18.4.12.9.3, section Low Speed I/Os Combined Slew Rate vs TL Length and Load Settings for more details on SR settings.	RW	0x0
17:16	RESERVED		R	0x0
15:14	DPM_DR0_SC	Slew rate control for group dpm_dr0 Refer to Section 18.4.12.9.3, section Low Speed I/Os Combined Slew Rate vs TL Length and Load Settings for more details on SR settings.	RW	0x0
13:12	GPIOWK4_DR0_SC	Slew rate control for group gpiowk4_dr0 Refer to Section 18.4.12.9.3, section Low Speed I/Os Combined Slew Rate vs TL Length and Load Settings for more details on SR settings.	RW	0x0
11:0	RESERVED	Reserved	R	0x000

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Table 18-716. Register Call Summary for Register CONTROL_SMART1NOPMIO_PADCONF_0

Control Module Functional Description

- Signal Integrity Parameter Control Registers With Pad Group Assignment: [0] [1] [2] [3] [4]

Control Module Register Manual

- SYSCTRL_PADCONF_WKUP Register Summary: [5]

Table 18-717. CONTROL_SMART1NOPMIO_PADCONF_1

Address Offset	0x0000 05A4		
Physical Address	0x4A31 E5A4	**Instance**	SYSCTRL_PADCONF_WKUP
Description	SMART1 NOPM I/O control 1 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FREF_DR0_LB								RESERVED								GPIO_DR7_LB				RESERVED				DPM_DR0_LB				GPIOWK4_DR0_LB				RESERVED							

Bits	Field Name	Description	Type	Reset
31:30	FREF_DR0_LB	Load control for group fref_dr0 0x0: TL Length= [2cm-20cm] / Farend[(1)] cap per TL= [1pF-10pF] 0x1: Dual TL Length= [20cm-40cm] / Farend cap per TL= [1pF-10pF] 0x2: TL Length = [2cm-20cm] / Farend cap per TL= [10pF-20pF] 0x3: Dual TL Length = [20cm-40cm] / Farend cap per TL= [10pF-20pF]	RW	0x0
29:20	RESERVED		R	0x000
19:18	GPIO_DR7_LB	Load control for group gpio_dr7 0x0: TL Length= [2cm-20cm] / Farend cap per TL= [1pF-10pF] 0x1: Dual TL Length= [20cm-40cm] / Farend cap per TL= [1pF-10pF] 0x2: TL Length = [2cm-20cm] / Farend cap per TL= [10pF-20pF] 0x3: Dual TL Length = [20cm-40cm] / Farend cap per TL= [10pF-20pF]	RW	0x0
17:16	RESERVED		R	0x0
15:14	DPM_DR0_LB	Load control for group dpm_dr0 0x0: TL Length= [2cm-20cm] / Farend cap per TL= [1pF-10pF] 0x1: Dual TL Length= [20cm-40cm] / Farend cap per TL= [1pF-10pF] 0x2: TL Length = [2cm-20cm] / Farend cap per TL= [10pF-20pF] 0x3: Dual TL Length = [20cm-40cm] / Farend cap per TL= [10pF-20pF]	RW	0x0

(1) Far-end load is equivalent to CLoad, where CLoad is the total capacitance seen at the far end of the transmission line.

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Bits	Field Name	Description	Type	Reset
13:12	GPIOWK4_DR0_LB	Load control for group gpiowk4_dr0 0x0: TL Length= [2cm-20cm] / Farend cap per TL= [1pF-10pF] 0x1: Dual TL Length= [20cm-40cm] / Farend cap per TL= [1pF-10pF] 0x2: TL Length = [2cm-20cm] / Farend cap per TL= [10pF-20pF] 0x3: Dual TL Length = [20cm-40cm] / Farend cap per TL= [10pF-20pF]	RW	0x0
11:0	RESERVED		R	0x000

Table 18-718. Register Call Summary for Register CONTROL_SMART1NOPMIO_PADCONF_1

Control Module Functional Description • Signal Integrity Parameter Control Registers With Pad Group Assignment: [0] [1] [2] [3] [4]
Control Module Register Manual • SYSCTRL_PADCONF_WKUP Register Summary: [5]

Table 18-719. CONTROL_WKUP_PADCONF_MODE

Address Offset	0x0000 05A8		
Physical Address	0x4A31 E5A8	**Instance**	SYSCTRL_PADCONF_WKUP
Description	PAD Voltage Mode control Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VDDS_DV_FREF	VDDS_DV_BANK2_SHARED1	RESERVED																													

Bits	Field Name	Description	Type	Reset
31	VDDS_DV_FREF	PAD Voltage level control for vdds_dv_fref 0x0: VDDS = 1.8V 0x1: VDDS = 1.2V	RW	0
30	VDDS_DV_BANK2_SHARED1	PAD Voltage level control for vdds_dv_bank2_shared1 0x0: VDDS = 1.8V 0x1: VDDS = 1.2V	RW	0
29:0	RESERVED		R	0x0000 0000

Table 18-720. Register Call Summary for Register CONTROL_WKUP_PADCONF_MODE

Control Module Functional Description • Dual Voltage-Supplied Peripheral Controls: [0] [1] [2]
Control Module Programming Guide • Operational Modes Configuration: [3] [4]

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Table 18-720. Register Call Summary for Register CONTROL_WKUP_PADCONF_MODE (continued)

Control Module Register Manual
- SYSCTRL_PADCONF_WKUP Register Summary: [5]

Table 18-721. CONTROL_XTAL_OSCILLATOR

Address Offset	0x0000 05AC		
Physical Address	0x4A31 E5AC	**Instance**	SYSCTRL_PADCONF_WKUP
Description	XTAL OSCILLATOR control Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OSCILLATOR_BOOST	OSCILLATOR_OS_OUT	RESERVED																													

Bits	Field Name	Description	Type	Reset
31	OSCILLATOR_BOOST	Fast startup control 0x0: Fast startup is disabled 0x1: Fast startup is enabled	RW	1
30	OSCILLATOR_OS_OUT	Oscillator output Read 0x0: low to high transition in BOOST mode Read 0x1: BOOST is disabled	R	0
29:0	RESERVED		R	0x0000 0000

Table 18-722. Register Call Summary for Register CONTROL_XTAL_OSCILLATOR

Control Module Register Manual
- SYSCTRL_PADCONF_WKUP Register Summary: [0]

Table 18-723. CONTROL_SMART3NOPMIO_PADCONF_0

Address Offset	0x0000 05B0		
Physical Address	0x4A31 E5B0	**Instance**	SYSCTRL_PADCONF_WKUP
Description	SMART3 NOPM IO control 0 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FREF_DR1_MB		FREF_DR5_MB		FREF_DR6_MB		FREF_DR7_MB		FREF_DR4_MB		RESERVED																					

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Bits	Field Name	Description	Type	Reset
31:30	FREF_DR1_MB	50-Ω output buffer mode control for group fref_dr1 Refer to 50-Ω output buffer I/Os with combined Mode and Load Settings for more details on mode settings.	RW	0x1
29:28	FREF_DR5_MB	50-Ω output buffer mode control for group fref_dr5 Refer to 50-Ω output buffer I/Os with combined Mode and Load Settings for more details on mode settings.	RW	0x1
27:26	FREF_DR6_MB	50-Ω output buffer mode control for group fref_dr6 Refer to 50-Ω output buffer I/Os with combined Mode and Load Settings for more details on mode settings.	RW	0x1
25:24	FREF_DR7_MB	50-Ω output buffer mode control for group Refer to 50-Ω output buffer I/Os with combined Mode and Load Settings for more details on mode settings.	RW	0x1
23:22	FREF_DR4_MB	50-Ω output buffer mode control for group fref_dr4 Refer to 50-Ω output buffer I/Os with combined Mode and Load Settings for more details on mode settings.	RW	0x1
21:0	RESERVED		R	0x000000

Table 18-724. Register Call Summary for Register CONTROL_SMART3NOPMIO_PADCONF_0

Control Module Functional Description

- Signal Integrity Parameter Control Registers With Pad Group Assignment: [0] [1] [2] [3] [4] [5]

Control Module Register Manual

- SYSCTRL_PADCONF_WKUP Register Summary: [6]

Table 18-725. CONTROL_SMART3NOPMIO_PADCONF_1

Address Offset	0x0000 05B4		
Physical Address	0x4A31 E5B4	**Instance**	SYSCTRL_PADCONF_WKUP
Description	SMART3 NOPM IO control 1 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FREF_DR1_LB0	FREF_DR5_LB0	FREF_DR6_LB0	FREF_DR7_LB0	FREF_DR4_LB0	RESERVED																										

Bits	Field Name	Description	Type	Reset
31	FREF_DR1_LB0	50-Ω output buffer load control for group fref_dr1 Refer to 50-Ω output buffer I/Os with combined Mode and Load Settings for more details on mode settings.	RW	0
30	FREF_DR5_LB0	50-Ω output buffer load control for group fref_dr5 Refer to 50-Ω output buffer I/Os with combined Mode and Load Settings for more details on mode settings.	RW	0
29	FREF_DR6_LB0	50-Ω output buffer load control for group fref_dr6 Refer to 50-Ω output buffer I/Os with combined Mode and Load Settings for more details on mode settings.	RW	0

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Bits	Field Name	Description	Type	Reset
28	FREF_DR7_LB0	50-Ω output buffer load control for group fref_dr7 Refer to 50-Ω output buffer I/Os with combined Mode and Load Settings for more details on mode settings.	RW	0
27	FREF_DR4_LB0	50-Ω output buffer load control for group fref_dr4 Refer to 50-Ω output buffer I/Os with combined Mode and Load Settings for more details on mode settings.	RW	0
26:0	RESERVED		R	0x0000000

Table 18-726. Register Call Summary for Register CONTROL_SMART3NOPMIO_PADCONF_1

Control Module Functional Description • Signal Integrity Parameter Control Registers With Pad Group Assignment: [0] [1] [2] [3] [4] [5]
Control Module Register Manual • SYSCTRL_PADCONF_WKUP Register Summary: [6]

Table 18-727. CONTROL_GPIOWK

Address Offset	0x600		
Physical Address	0x4A31 E600	**Instance**	SYSCTRL_PADCONF_WKUP
Description	GPIOWK pads I/O control Access conditions. Read: unrestricted; Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PAD_GPIO_WK1_LOW	Reserved	PAD_GPIO_WK2_LOW	GPIOWK_IO_PWRDNZ	Reserved																											

Bits	Field Name	Description		Type	Reset
31	PAD_GPIO_WK1_LOW	LOW enable for gpio_wk1 PAD		RW	1
		0:	Strong pulldown is disabled		
		1:	Strong Pull-down after reset release		
30	Reserved			RO Rreturns 0s	0
29	PAD_GPIO_WK2_LOW	LOW enable for gpio_wk2 PAD		RW	1
		0:	Strong Pull-down is disabled		
		1:	Strong Pull-down after reset release		

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Bits	Field Name	Description	Type	Reset
28	GPIOWK_IO_PWRDNZ	PWRDNZ control to gpiowk0-gpiowk2 IOs This bit is used to protect the gpio_wk0-gpio_wk2 pads associated I/O cell when SIM_VDDS is not stable. 0: Software must clear this bit when SIM_VDDS changes. 1: Software must set this bit only when SIM_VDDS is stable.	RW	0
27:0	Reserved		RO Rreturns 0s	0x0000000

Table 18-728. Register Call Summary for Register CONTROL_GPIOWK

Control Module Functional Description
- Extended-Drain I/O and PBIAS Cell: [0]
- Extended-Drain I/O: [1] [2] [3] [4]

Control Module Programming Guide
- Operational Modes Configuration: [5] [6] [7] [8] [9]

Control Module Register Manual
- SYSCTRL_PADCONF_WKUP Register Summary: [10]

Table 18-729. CONTROL_I2C_2

Address Offset	0x0000 0604		
Physical Address	0x4A31 E604	**Instance**	SYSCTRL_PADCONF_WKUP
Description	I2C pads control 2 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SR_SDA_GLFENB	SR_SDA_LOAD_BITS		SR_SDA_PULLUPRESX	SR_SCL_GLFENB	SR_SCL_LOAD_BITS		SR_SCL_PULLUPRESX	RESERVED																							

Bits	Field Name	Description	Type	Reset
31	SR_SDA_GLFENB	Active_high glitch free operation enable pin for sr i2c receiver 0x0: Disable i2c4 glitch free operation 0x1: Enable i2c4 glitch free operation	RW	0
30:29	SR_SDA_LOAD_BITS	Internal Pull up resistor in Fast or Standard mode / High_speed mode for sr i2c 0x0: 4.5 kΩ (5-15 pF) / 1.66 kΩ (5-12 pF) 0x1: 2.1 kΩ (15-50 pF) / 920 Ω (12-25 pF) 0x2: 860 Ω (50-150 pF) / 500 Ω (25-50 pF) 0x3: N.A / 300 Ω (50-80 pF)	RW	0x0

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Bits	Field Name	Description	Type	Reset
28	SR_SDA_PULLUPRESX	Active_low internal pull_up resistor enabled for sr i2c 0x0: Enable Internal Pull up resistor 0x1: Disable Internal Pull up resisitor	RW	0
27	SR_SCL_GLFENB	Active_high glitch free operation enable pin for sr i2c receiver 0x0: Disable i2c4 glitch free operation 0x1: Enable i2c4 glitch free operation	RW	0
26:25	SR_SCL_LOAD_BITS	Internal Pull up resistor in Fast or Standard mode / High_speed mode for sr i2c 0x0: 4.5 kΩ (5-15 pF) / 1.66 kΩ (5-12 pF) 0x1: 2.1 kΩ (15-50 pF) / 920 Ω (12-25 pF) 0x2: 860 Ω (50-150 pF) / 500 Ω (25-50 pF) 0x3: N.A / 300 Ω (50-80 pF)	RW	0x0
24	SR_SCL_PULLUPRESX	Active_low internal pull_up resistor enabled for sr i2c 0x0: Enable Internal Pull up resistor 0x1: Disable Internal Pull up resisitor	RW	0
23:0	RESERVED		R	0x000000

Table 18-730. Register Call Summary for Register CONTROL_I2C_2

Control Module Functional Description
- Signal Integrity Parameter Control Registers With Pad Group Assignment: [0] [1] [2] [3] [4] [5] [6]

Control Module Register Manual
- SYSCTRL_PADCONF_WKUP Register Summary: [7]

Table 18-731. CONTROL_JTAG

Address Offset	0x0000 0608		
Physical Address	0x4A31 E608	**Instance**	SYSCTRL_PADCONF_WKUP
Description	JTAG pads control Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
JTAG_NTRST_EN	JTAG_TCK_EN	JTAG_RTCK_EN	JTAG_TDI_EN	JTAG_TDO_EN	RESERVED																										

Bits	Field Name	Description	Type	Reset
31	JTAG_NTRST_EN	bus holder enable for jtag_ntrst PAD 0x0: Disable bus holder functionality 0x1: Enable bus holder functionality	RW	0
30	JTAG_TCK_EN	bus holder enable for jtag_tck PAD 0x0: Disable bus holder functionality 0x1: Enable bus holder functionality	RW	0
29	JTAG_RTCK_EN	bus holder enable for jtag_rtck PAD 0x0: Disable bus holder functionality 0x1: Enable bus holder functionality	RW	0

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Bits	Field Name	Description	Type	Reset
28	JTAG_TDI_EN	bus holder enable for jtag_tdi PAD 0x0: Disable bus holder functionality 0x1: Enable bus holder functionality	RW	0
27	JTAG_TDO_EN	bus holder enable for jtag_tdo PAD 0x0: Disable bus holder functionality 0x1: Enable bus holder functionality	RW	0
26:0	RESERVED		R	0x0000000

Table 18-732. Register Call Summary for Register CONTROL_JTAG

Control Module Functional Description • Signal Integrity Parameter Control Registers With Pad Group Assignment: [0]
Control Module Register Manual • SYSCTRL_PADCONF_WKUP Register Summary: [1]

Table 18-733. CONTROL_SYS

Address Offset	0x0000 060C		
Physical Address	0x4A31 E60C	**Instance**	SYSCTRL_PADCONF_WKUP
Description	SYS controls Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SYS_NRESWARM_PIPU	RESERVED																														

Bits	Field Name	Description	Type	Reset
31	SYS_NRESWARM_PIPU	Pull up enable for sys_nreswarm PAD 0x0: Enable pull up 0x1: Disable pull up	RW	0
30:0	RESERVED		R	0x0000 0000

Table 18-734. Register Call Summary for Register CONTROL_SYS

Control Module Register Manual • SYSCTRL_PADCONF_WKUP Register Summary: [0]

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Table 18-735. CONTROL_WKUP_CONTROL_SPARE_RW

Address Offset	0x0000 0614		
Physical Address	0x4A31 E614	**Instance**	SYSCTRL_PADCONF_WKUP
Description	Wake-up control spare RW Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WKUP_CONTROL_SPARE_RW																															

Bits	Field Name	Description	Type	Reset
31:0	WKUP_CONTROL_SPARE_RW	Wake-up control spare register bits RW	RW	0x0000 0000

Table 18-736. Register Call Summary for Register CONTROL_WKUP_CONTROL_SPARE_RW

Control Module Register Manual

- SYSCTRL_PADCONF_WKUP Register Summary: [0]

Table 18-737. CONTROL_WKUP_CONTROL_SPARE_R

Address Offset	0x0000 0618		
Physical Address	0x4A31 E618	**Instance**	SYSCTRL_PADCONF_WKUP
Description	Wake-up control spare R Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WKUP_CONTROL_SPARE_R																															

Bits	Field Name	Description	Type	Reset
31:0	WKUP_CONTROL_SPARE_R	Wake-up control spare register bits R	R	0x0000 0000

Table 18-738. Register Call Summary for Register CONTROL_WKUP_CONTROL_SPARE_R

Control Module Register Manual

- SYSCTRL_PADCONF_WKUP Register Summary: [0]

Table 18-739. CONTROL_WKUP_CONTROL_SPARE_R_C0

Address Offset	0x0000 061C		
Physical Address	0x4A31 E61C	**Instance**	SYSCTRL_PADCONF_WKUP
Description	Wake-up control spare RC Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WKUP_CONTROL_SPARE_R_C0	WKUP_CONTROL_SPARE_R_C1	WKUP_CONTROL_SPARE_R_C2	WKUP_CONTROL_SPARE_R_C3	WKUP_CONTROL_SPARE_R_C4	WKUP_CONTROL_SPARE_R_C5	WKUP_CONTROL_SPARE_R_C6	WKUP_CONTROL_SPARE_R_C7	RESERVED																									

Bits	Field Name	Description	Type	Reset
31	WKUP_CONTROL_SPARE_R_C0	Wake-up control spare register bits RC	RW (Write 1 to Clear)	0
30	WKUP_CONTROL_SPARE_R_C1	Wake-up control spare register bits RC	RW (Write 1 to Clear)	0
29	WKUP_CONTROL_SPARE_R_C2	Wake-up control spare register bits RC	RW (Write 1 to Clear)	0
28	WKUP_CONTROL_SPARE_R_C3	Wake-up control spare register bits RC	RW (Write 1 to Clear)	0
27	WKUP_CONTROL_SPARE_R_C4	Wake-up control spare register bits RC	RW (Write 1 to Clear)	0
26	WKUP_CONTROL_SPARE_R_C5	Wake-up control spare register bits RC	RW (Write 1 to Clear)	0
25	WKUP_CONTROL_SPARE_R_C6	Wake-up control spare register bits RC	RW (Write 1 to Clear)	0
24	WKUP_CONTROL_SPARE_R_C7	Wake-up control spare register bits RC	RW (Write 1 to Clear)	0
23:0	RESERVED		R	0x000000

Table 18-740. Register Call Summary for Register CONTROL_WKUP_CONTROL_SPARE_R_C0

Control Module Register Manual

- SYSCTRL_PADCONF_WKUP Register Summary: [0]

Table 18-741. CONTROL_WKUP_CONTROL_SPARE_RW1

Address Offset	0x0000 0620		
Physical Address	0x4A31 E620	**Instance**	SYSCTRL_PADCONF_WKUP
Description	WKUP control spare RW1 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WKUP_CONTROL_SPARE_RW1																															

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Bits	Field Name	Description	Type	Reset
31:0	WKUP_CONTROL_SPARE_RW1	wkup control spare register bits RW1	RW	0x0000 0000

Table 18-742. Register Call Summary for Register CONTROL_WKUP_CONTROL_SPARE_RW1

Control Module Register Manual
- SYSCTRL_PADCONF_WKUP Register Summary: [0]

Table 18-743. CONTROL_WKUP_CONTROL_SPARE_RW2

Address Offset	0x0000 0624		
Physical Address	0x4A31 E624	**Instance**	SYSCTRL_PADCONF_WKUP
Description	WKUP control spare RW2 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WKUP_CONTROL_SPARE_RW2																															

Bits	Field Name	Description	Type	Reset
31:0	WKUP_CONTROL_SPARE_RW2	wkup control spare register bits RW2	RW	0x0000 0000

Table 18-744. Register Call Summary for Register CONTROL_WKUP_CONTROL_SPARE_RW2

Control Module Register Manual
- SYSCTRL_PADCONF_WKUP Register Summary: [0]

Table 18-745. CONTROL_WKUP_CONTROL_SPARE_RW3

Address Offset	0x0000 0628		
Physical Address	0x4A31 E628	**Instance**	SYSCTRL_PADCONF_WKUP
Description	WKUP control spare RW3 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WKUP_CONTROL_SPARE_RW3																															

Bits	Field Name	Description	Type	Reset
31:0	WKUP_CONTROL_SPARE_RW3	wkup control spare register bits RW3	RW	0x0000 0000

Table 18-746. Register Call Summary for Register CONTROL_WKUP_CONTROL_SPARE_RW3

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- SYSCTRL_PADCONF_WKUP Register Summary: [0]

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Table 18-747. CONTROL_WKUP_CONTROL_SPARE_RW4

Address Offset	0x0000 062C		
Physical Address	0x4A31 E62C	**Instance**	SYSCTRL_PADCONF_WKUP
Description	WKUP control spare RW4 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WKUP_CONTROL_SPARE_RW4																															

Bits	Field Name	Description	Type	Reset
31:0	WKUP_CONTROL_SPARE_RW4	wkup control spare register bits RW4	RW	0x0000 0000

Table 18-748. Register Call Summary for Register CONTROL_WKUP_CONTROL_SPARE_RW4

Control Module Register Manual

- SYSCTRL_PADCONF_WKUP Register Summary: [0]

Table 18-749. CONTROL_WKUP_CONTROL_SPARE_RW5

Address Offset	0x0000 0630		
Physical Address	0x4A31 E630	**Instance**	SYSCTRL_PADCONF_WKUP
Description	WKUP control spare RW5 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WKUP_CONTROL_SPARE_RW5																															

Bits	Field Name	Description	Type	Reset
31:0	WKUP_CONTROL_SPARE_RW5	wkup control spare register bits RW5	RW	0x0000 0000

Table 18-750. Register Call Summary for Register CONTROL_WKUP_CONTROL_SPARE_RW5

Control Module Register Manual

- SYSCTRL_PADCONF_WKUP Register Summary: [0]

Table 18-751. CONTROL_WKUP_CONTROL_SPARE_RW6

Address Offset	0x0000 0634		
Physical Address	0x4A31 E634	**Instance**	SYSCTRL_PADCONF_WKUP
Description	WKUP control spare RW6 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WKUP_CONTROL_SPARE_RW6																															

Bits	Field Name	Description	Type	Reset
31:0	WKUP_CONTROL_SPARE_RW6	wkup control spare register bits RW6	RW	0x0000 0000

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Table 18-752. Register Call Summary for Register CONTROL_WKUP_CONTROL_SPARE_RW6

Control Module Register Manual

- SYSCTRL_PADCONF_WKUP Register Summary: [0]

Table 18-753. CONTROL_WKUP_CONTROL_SPARE_RW7

Address Offset	0x0000 0638		
Physical Address	0x4A31 E638	**Instance**	SYSCTRL_PADCONF_WKUP
Description	WKUP control spare RW7 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WKUP_CONTROL_SPARE_RW7																															

Bits	Field Name	Description	Type	Reset
31:0	WKUP_CONTROL_SPARE_RW7	wkup control spare register bits RW7	RW	0x0000 0000

Table 18-754. Register Call Summary for Register CONTROL_WKUP_CONTROL_SPARE_RW7

Control Module Register Manual

- SYSCTRL_PADCONF_WKUP Register Summary: [0]

Table 18-755. CONTROL_WKUP_CONTROL_SPARE_RW8

Address Offset	0x0000 063C		
Physical Address	0x4A31 E63C	**Instance**	SYSCTRL_PADCONF_WKUP
Description	WKUP control spare RW8 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WKUP_CONTROL_SPARE_RW8																															

Bits	Field Name	Description	Type	Reset
31:0	WKUP_CONTROL_SPARE_RW8	wkup control spare register bits RW8	RW	0x0000 0000

Table 18-756. Register Call Summary for Register CONTROL_WKUP_CONTROL_SPARE_RW8

Control Module Register Manual

- SYSCTRL_PADCONF_WKUP Register Summary: [0]

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Table 18-757. CONTROL_WKUP_CONTROL_SPARE_RW9

Address Offset	0x0000 0640		
Physical Address	0x4A31 E640	**Instance**	SYSCTRL_PADCONF_WKUP
Description	WKUP control spare RW9 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WKUP_CONTROL_SPARE_RW9																															

Bits	Field Name	Description	Type	Reset
31:0	WKUP_CONTROL_SPARE_RW9	wkup control spare register bits RW9	RW	0xFFFF FFFF

Table 18-758. Register Call Summary for Register CONTROL_WKUP_CONTROL_SPARE_RW9

Control Module Register Manual

- SYSCTRL_PADCONF_WKUP Register Summary: [0]

Table 18-759. CONTROL_WKUP_CONTROL_SPARE_R1

Address Offset	0x0000 064C		
Physical Address	0x4A31 E64C	**Instance**	SYSCTRL_PADCONF_WKUP
Description	WKUP control spare R1 Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WKUP_CONTROL_SPARE_R1																															

Bits	Field Name	Description	Type	Reset
31:0	WKUP_CONTROL_SPARE_R1	wkup control spare register bits R1	R	0x0000 0000

Table 18-760. Register Call Summary for Register CONTROL_WKUP_CONTROL_SPARE_R1

Control Module Register Manual

- SYSCTRL_PADCONF_WKUP Register Summary: [0]

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Mailbox

This chapter describes the Mailbox module in the device.

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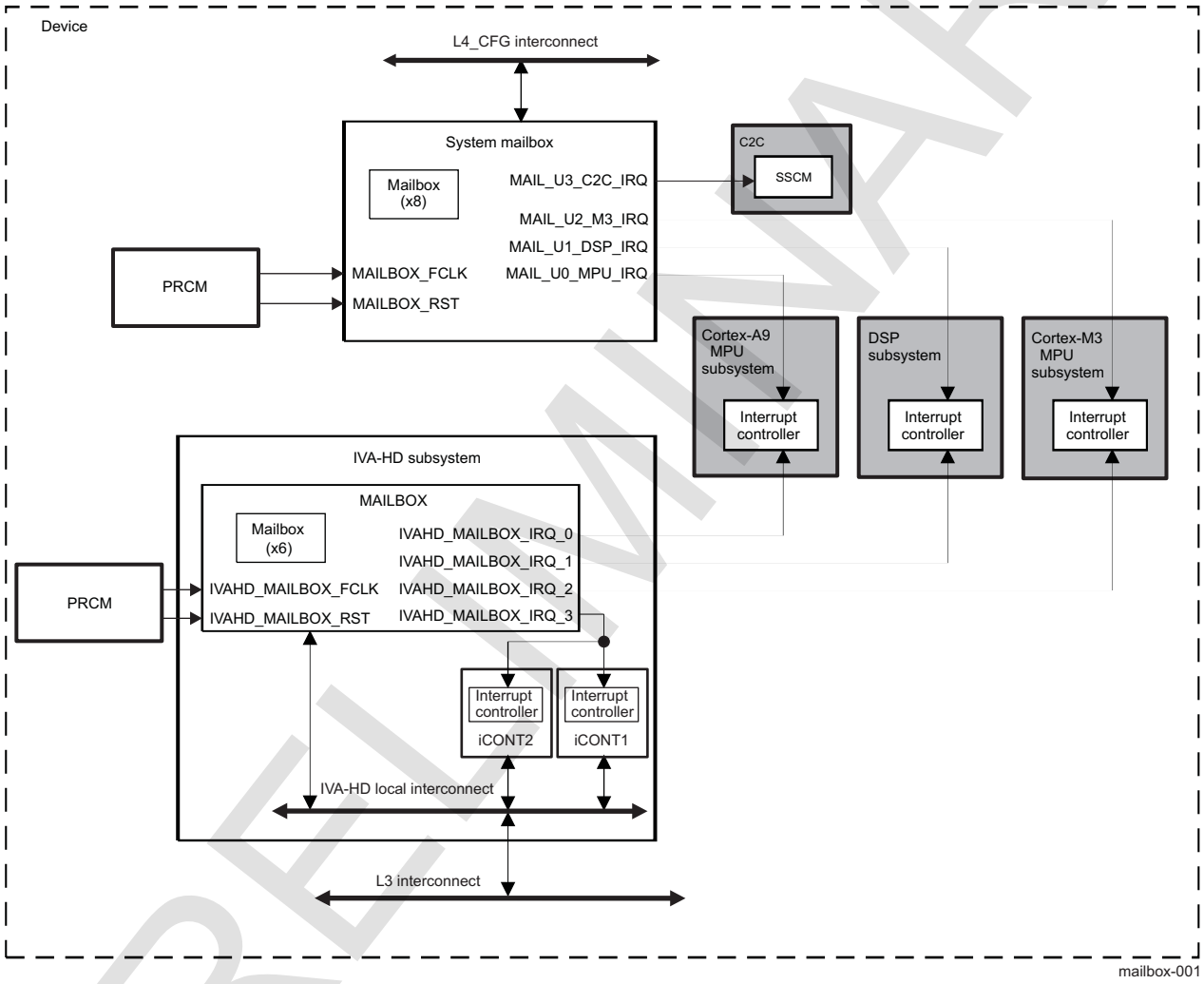
19.1 Mailbox Overview

Communication between the on-chip processors of the device uses a queued mailbox-interrupt mechanism.

The queued mailbox-interrupt mechanism allows the software to establish a communication channel between two processors through a set of registers and associated interrupt signals by sending and receiving messages (mailboxes).

Figure 19-1 shows an overview of the mailbox module.

Figure 19-1. Mailbox Overview



There are two mailbox module instances in the device:

- System mailbox - used for Cortex-A9 microprocessor unit (Cortex-A9 MPU), digital signal processor (DSP) and Cortex-M3 microprocessor unit (Cortex-M3 MPU) communications.
- IVA-HD mailbox - used for communication between one internal to the IVA-HD subsystem user (imaging controller 1 - iCONT1, or imaging controller 2 - iCONT2) and three external to the IVA-HD subsystem users (Cortex-A9 MPU, DSP and Cortex-M3 MPU). This communication is insured through three pairs of mailboxes.

The mailbox module includes the following features:

- Three users for the system mailbox instance (Cortex-A9 MPU, DSP and Cortex-M3 MPU)/four users for the IVA-HD mailbox instance (iCONT1/iCONT2, Cortex-A9 MPU, DSP and Cortex-M3 MPU)

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- Eight mailbox message queues for the system mailbox instance/six mailbox message queues for the IVA-HD mailbox instance
- Flexible assignment of receiver and sender for each mailbox through interrupt configuration
- Three interrupts (one per user) for the system mailbox instance/four interrupts (one per user) for the IVA-HD mailbox instance
- 32-bit message width
- Four-message FIFO depth for each message queue
- Message reception and queue-not-full notification using interrupts
- Support of 16-/32-bit addressing scheme
- Power management support

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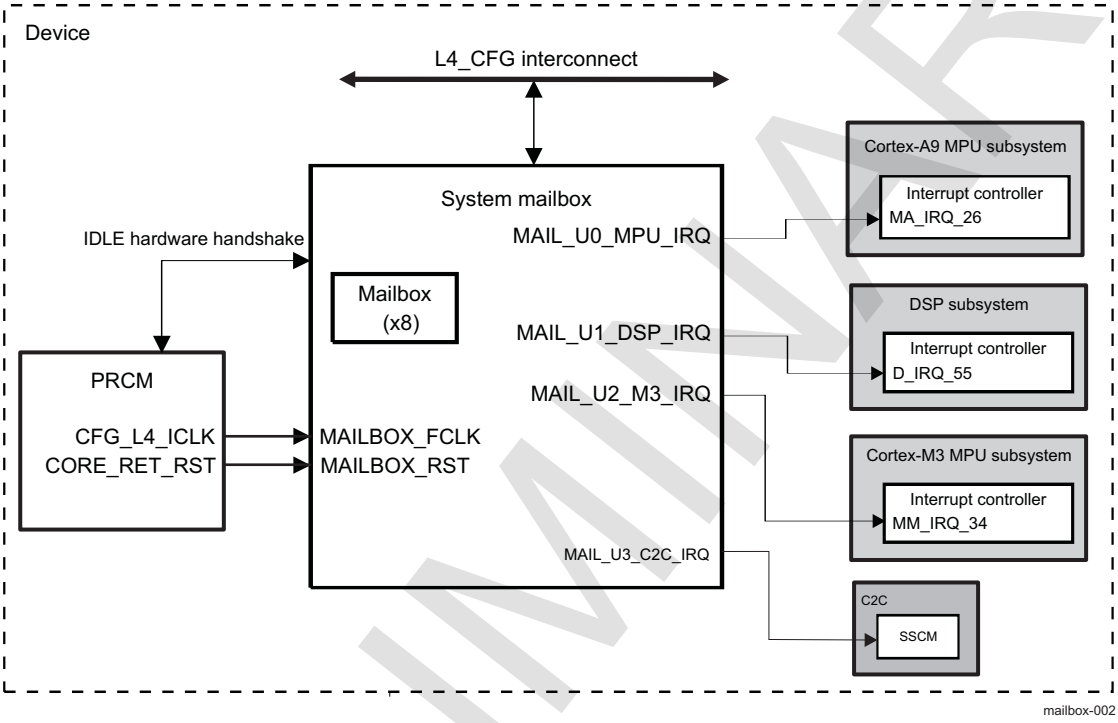
19.2 Mailbox Integration

This section describes the mailbox integration in the device, including information about clocks, resets, and hardware requests.

19.2.1 System Mailbox Integration

Figure 19-2 shows the system mailbox integration.

Figure 19-2. System Mailbox Integration



NOTE: For more information about the IDLE hardware handshake, see Section 3.1.1.1.2, *Module Level Clock Management*, in Chapter 3, *Power, Reset, and Clock Management*.

Table 19-1 through Table 19-3 summarize the system mailbox integration in the device.

Table 19-1. Integration Attributes

Module Instance	Attributes		
	Power Domain	Wake-Up Capability	Interconnect
SYSTEM_MAILBOX	PD_CORE	NA	L4_CFG

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Table 19-2. Clocks and Resets

Clocks				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
SYSTEM_MAILBOX	MAILBOX_FCLK	CFG_L4_ICLK	PRCM	System mailbox functional/interface clock. For information about PRCM clock gating and management, see Section 3.6.14, *CD_L4_CFG Clock Management*, in Chapter 3, *Power, Reset, and Clock Management*.
Resets				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
SYSTEM_MAILBOX	MAILBOX_RST	CORE_RET_RST	PRCM	System mailbox hardware reset. For information about PRCM reset sources and distribution, see Section 3.5.4, *Reset Domains*, in Chapter 3, *Power, Reset, and Clock Management*.

Table 19-3. Hardware Requests

Interrupt Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
SYSTEM_MAILBOX	MAIL_U0_MPU_IRQ	MA_IRQ_26	Cortex-A9	System mailbox user 0 interrupt request. For information about Cortex-A9 MPU interrupt mapping, see Section 17.3.2, *Interrupt Requests to the Cortex-A9 MPU Interrupt Controller*, in Chapter 17, *Interrupt Controllers*.
	MAIL_U1_DSP_IRQ	D_IRQ_55	DSP	System mailbox user 1 interrupt request. For information about DSP interrupt mapping, see see , *Interrupt Requests*, in Chapter 5, *DSP Subsystem*.
	MAIL_U2_M3_IRQ	MM_IRQ_34	Cortex-M3	System mailbox user 2 interrupt request. For information about Cortex-M3 MPU interrupt mapping, see Section 17.3.2, *Interrupt Requests to the Cortex-M3 MPU Interrupt Controller*, in Chapter 17, *Interrupt Controllers*.
	MAIL_U3_C2C_IRQ	C2C_SSCM_GPI_1	C2C INTC	Interrupt to the SSCM of C2C
No DMA Requests				

NOTE: For information about interrupt source description, see Section 19.3.4, *Interrupt Requests*.

19.2.2 IVA-HD Mailbox Integration

Figure 19-3 shows the IVA-HD mailbox integration.

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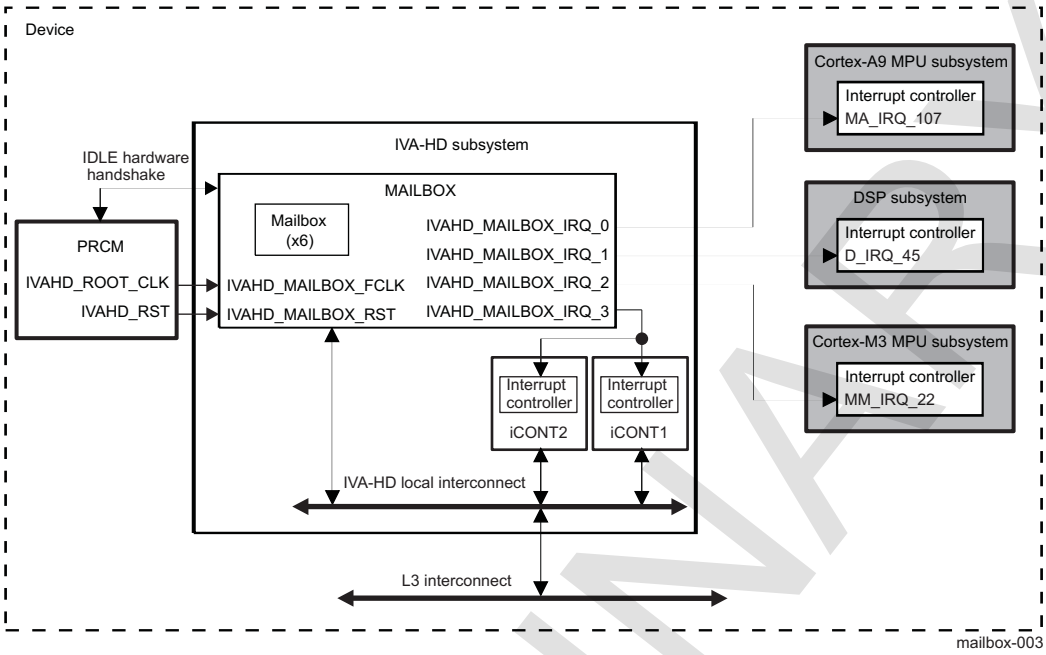
Figure 19-3. IVA-HD Mailbox Integration



NOTE: For more information about the IDLE hardware handshake, see Section 3.1.1.1.2, *Module Level Clock Management*, in Chapter 3, *Power, Reset, and Clock Management*.

NOTE: The two imaging controllers - iCONT1 and iCONT2, are mapped on a shared interrupt line. The choice between them is done by masking mailbox interrupt on iCONT1 or iCONT2. For more information, see , *IVA-HD Imaging Controller* in Chapter 6, *IVA-HD Subsystem*.

Table 19-4 through Table 19-6 summarize the IVA-HD mailbox integration in the device.

Table 19-4. Integration Attributes

Module Instance	Attributes		
	Power Domain	Wake-Up Capability	Interconnect
IVAHD_MAILBOX	PD_IVAHD	NA	IVA-HD local interconnect

Table 19-5. Clocks and Resets

Clocks				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
IVAHD_MAILBOX	IVAHD_MAILBOX_FCLK	IVAHD_CLK	PRCM	IVA-HD mailbox functional/interface clock.
Resets				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
IVAHD_MAILBOX	IVAHD_MAILBOX_RST	IVAHD_RST	PRCM	IVA-HD mailbox hardware reset.

Table 19-6. Hardware Requests

Interrupt Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**

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Table 19-6. Hardware Requests (continued)

IVAHD_MAILBOX	IVAHD_MAILBOX_IRQ_0	MA_IRQ_107	Cortex-A9	IVA-HD mailbox user 0 interrupt request
	IVAHD_MAILBOX_IRQ_1	D_IRQ_45	DSP	IVA-HD mailbox user 1 interrupt request
	IVAHD_MAILBOX_IRQ_2	MM_IRQ_22	Cortex-M3	IVA-HD mailbox user 2 interrupt request
	IVAHD_MAILBOX_IRQ_3	IRQ#11	iCONT1/iCONT2	IVA-HD mailbox user 3 interrupt request. For information about iCONT1/iCONT2 interrupt mapping, see , *iCONT*.
No DMA Requests				

NOTE: For information about interrupt source description, see Section 19.3.4, *Interrupt Requests*.

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19.3 Mailbox Functional Description

NOTE: In the mailbox functional description, *u* is the user number and *m* is the mailbox number as follows:

- for the system mailbox module instance, *u*=0 to 2 and *m*=0 to 7
- for the IVA-HD mailbox module instance, *u*=0 to 3 and *m*=0 to 5

The mailbox module provides a means of communication through message queues among the users (depending on the mailbox module instance). The individual mailbox modules (8 for the system mailbox instance, 6 for the IVA-HD mailbox instance), or FIFOs, can associate (or de-associate) with any of the processors using the MAILBOX_IRQENABLE_SET_u (or MAILBOX_IRQENABLE_CLR_u) register.

CAUTION

For the IVA-HD mailbox instance, communication is possible only if one of the users is iCONT1 or iCONT2.

The mailbox module includes the following user subsystems:

- User 0: Cortex-A9 MPU subsystem (u = 0)
- User 1: DSP subsystem (u = 1)
- User 2: Cortex-M3 MPU subsystem (u = 2)
- User 3:
  - IVA-HD subsystem (u = 3) - only available to the IVA-HD mailbox instance
  - Mailbox subsystem - only available to SSCM module of C2C interface

Each user has a dedicated interrupt signal from the corresponding mailbox module instance and dedicated interrupt enabling and status registers.
Each MAILBOX_IRQSTATUS_RAW_u/MAILBOX_IRQSTATUS_CLR_u interrupt status register corresponds to a particular user.

For the system mailbox instance, a user can query its interrupt status register through the L4_CFG interconnect.

For the IVA-HD mailbox instance, a user can query its interrupt status register as follows:

- Cortex-A9 MPU and Cortex-M3 MPU - through the L3 interconnect
- iCONT1/iCONT2 and DSP - private access (directly through the IVA-HD local interconnect)

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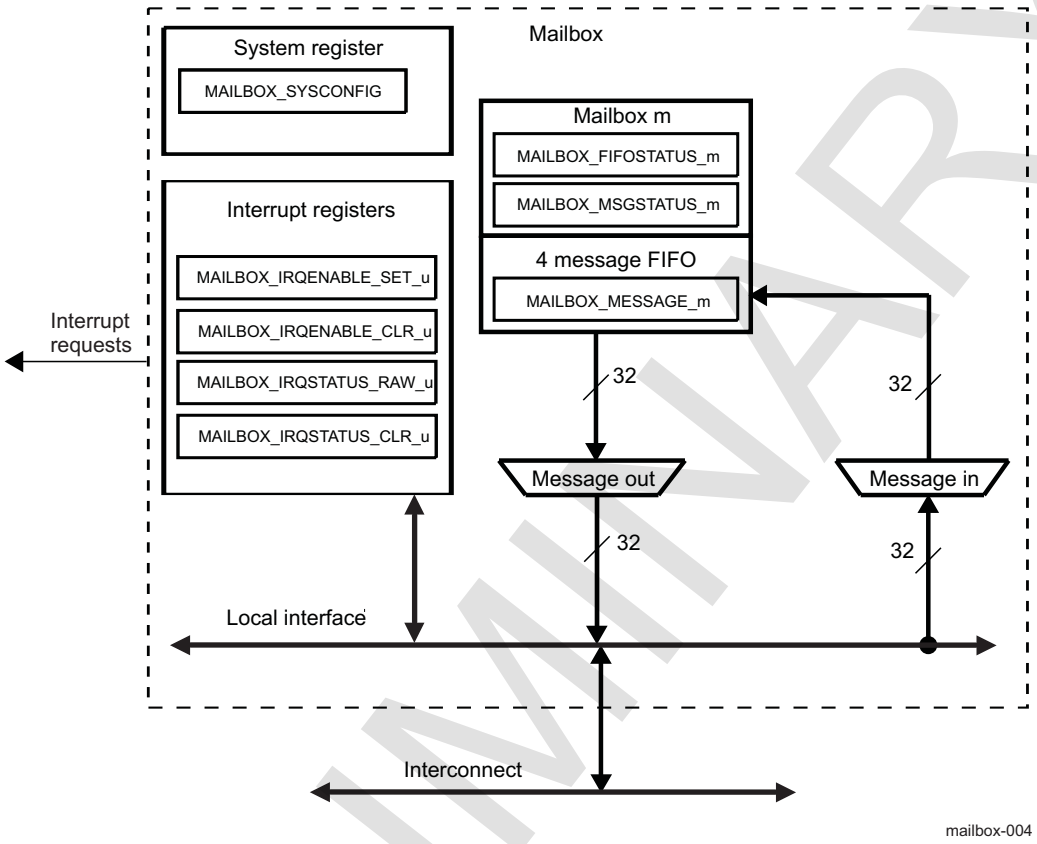
19.3.1 Mailbox Block Diagram

Figure 19-4 shows the mailbox block diagram.

Figure 19-4. Mailbox Block Diagram



NOTE: The interrupt requests and the interconnect depend on the mailbox module instance. For more information, see Section 19.2, *Mailbox Integration*.

19.3.2 Mailbox Software Reset

The mailbox module supports a software reset through the MAILBOX_SYSCONFIG[0] SOFTRESET bit. Setting this bit to 1 enables an active software reset that is functionally equivalent to a hardware reset. Reading the MAILBOX_SYSCONFIG[0] SOFTRESET bit gives the status of the software reset:

- Read 1: the software reset is on-going.
- Read 0: the software reset is complete.

The software must ensure that the software reset completes before doing mailbox operations.

19.3.3 Mailbox Power Management

Table 19-7 describes power-management features available for the mailbox module.

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NOTE:

- For information about source clock gating and sleep/wake-up transitions description, see Section 3.1.1.1.4, *Clock-Domain Level Clock Management*, in Chapter 3, *Power, Reset, and Clock Management*.
- For descriptions of EnaWakeUp, IdleMode, ClockActivity, and StandbyMode features, see Section 3.1.1.1.2, *Module-Level Clock Management*, in Chapter 3, *Power, Reset, and Clock Management*.

Table 19-7. Local Power Management Features

Feature	Registers	Description
Clock autogating	NA	Feature not available
Slave idle modes	MAILBOX_SYSCONFIG[3:2] SIDLEMODE bit field	Force-idle, no-idle and smart-idle modes are available
Clock activity	NA	Feature not available
Master standby modes	NA	Feature not available
Global wake-up enable	NA	Feature not available
Wake-up sources enable	NA	Feature not available

The mailbox module can be configured using the MAILBOX_SYSCONFIG[3:2] SIDLEMODE bit field to one of the following acknowledgment modes:

- Force-idle mode (SIDLEMODE = 0x0): The mailbox module immediately enters the idle state on receiving a low-power-mode request from the PRCM module. In this mode, the software must ensure that there are no asserted output interrupts before requesting this mode to go into the idle state.
- No-idle mode (SIDLEMODE = 0x1): The mailbox module never enters the idle state.
- Smart-idle mode (SIDLEMODE = 0x2): After receiving a low-power-mode request from the PRCM module, the mailbox module enters the idle state only after all asserted output interrupts are acknowledged.

19.3.4 Mailbox Interrupt Requests

An interrupt request allows the user of the mailbox to be notified when a message is received or when the message queue is not full. There is one interrupt per user.

NOTE: For more information about interrupt requests, see Section 19.2, *Mailbox Integration*.

Table 19-8 lists the event flags, and their mask, that can cause module interrupts.

Table 19-8. Interrupt Events

Non-Maskable Event Flag [1]	Maskable Event Flag	Event Mask Bit	Event Unmask Bit	Description
MAILBOX_IRQSTATUS_RAW_u[0+m*2] NEWMSGSTATUSUUMBm	MAILBOX_IRQSTATUS_CLR_u[0+m*2] NEWMSGSTATUSUUMBm	MAILBOX_IRQENABLE_CLR_u[0+m*2] NEWMSGSTATUSUUMBm	MAILBOX_IRQENABLE_SET_u[0+m*2] NEWMSGSTATUSUUMBm	Mailbox *m* receives a new message.
MAILBOX_IRQSTATUS_RAW_u[1+m*2] NOTFULLSTATUSUUMBm	MAILBOX_IRQSTATUS_CLR_u[1+m*2] NOTFULLSTATUSUUMBm	MAILBOX_IRQENABLE_CLR_u[1+m*2] NOTFULLSTATUSUUMBm	MAILBOX_IRQENABLE_SET_u[1+m*2] NOTFULLSTATUSUUMBm	Mailbox *m* message queue is not full.

(1) MAILBOX.MAILBOX_IRQSTATUS_RAW_u register is mostly used for debug purposes.

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CAUTION

Once an event generating the interrupt request has been processed by the software, it must be cleared by writing a logical 1 in the corresponding bit of the MAILBOX_IRQSTATUS_CLR_u register.

Writing a logical 1 in a bit of the MAILBOX_IRQSTATUS_CLR_u register will also clear to 0 the corresponding bit in the appropriate MAILBOX_IRQSTATUS_RAW_u register.

An event can generate an interrupt request when a logical 1 is written to the corresponding unmask bit in the MAILBOX_IRQENABLE_SET_u register. Events are reported in the appropriate MAILBOX_IRQSTATUS_CLR_u and MAILBOX_IRQSTATUS_RAW_u registers.

An event stops generating interrupt requests when a logical 1 is written to the corresponding mask bit in the MAILBOX_IRQENABLE_CLR_u register. Events are only reported in the appropriate MAILBOX_IRQSTATUS_RAW_u register.

In case of the MAILBOX_IRQSTATUS_RAW_u register, the event is reported in the corresponding bit even if the interrupt request generation is disabled for this event.

19.3.5 Mailbox Assignment

19.3.5.1 Description

To assign a receiver to a mailbox, set the new message interrupt enable bit corresponding to the desired mailbox in the MAILBOX_IRQENABLE_SET_u register. The receiver reads the MAILBOX_MESSAGE_m register to retrieve a message from the mailbox.

An alternate method for the receiver that does not use the interrupts is to poll the MAILBOX_FIFOSTATUS_m and/or MAILBOX_MSGSTATUS_m registers to know when to send or retrieve a message to or from the mailbox. This method does not require assigning a receiver to a mailbox. Because this method does not include the explicit assignment of the mailbox, the software must avoid having multiple receivers use the same mailbox, which can result in incoherency.

To assign a sender to a mailbox, set the queue-not-full interrupt enable bit of the desired mailbox in the MAILBOX_IRQENABLE_SET_u register, where *u* is the number of the sending user. However, direct allocation of a mailbox to a sender is not recommended because it can cause the sending processor to be constantly interrupted.

It is recommended that register polling be used to:

- Check the status of either the MAILBOX_FIFOSTATUS_m or MAILBOX_MSGSTATUS_m registers
- Write the message to the corresponding MAILBOX_MESSAGE_m register, if space is available.

The sender might use the queue-not-full interrupt when the initial mailbox status check indicates the mailbox is full. In this case, the sender can enable the queue-not-full interrupt for its mailbox in the appropriate MAILBOX_IRQENABLE_SET_u register. This allows the sender to be notified by interrupt only when a FIFO queue has at least one available entry.

Reading the MAILBOX_IRQSTATUS_CLR_u register determines the status of the new message and the queue-not-full interrupts for a particular user. Writing 1 to the corresponding bit in the MAILBOX_IRQSTATUS_CLR_u register acknowledges, and subsequently clears, an interrupt.

CAUTION

Assigning multiple senders or multiple receivers to the same mailbox is not recommended.

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19.3.6 Sending and Receiving Messages

19.3.6.1 Description

When a 32-bit message is written to the MAILBOX_MESSAGE_m register, the message is appended into the FIFO queue. This queue holds four messages. If the queue is full, the message is discarded.

Queue overflow can be avoided by first reading the MAILBOX_FIFOSTATUS_m register to check that the mailbox message queue is not full before writing a new message to it.

Reading the MAILBOX_MESSAGE_m register returns the message at the beginning of the FIFO queue and removes it from the queue. If the FIFO queue is empty when the MAILBOX_MESSAGE_m register is read, the value 0 is returned.

The new message interrupt is asserted when at least one message is in the mailbox message FIFO queue. To determine the number of messages in the mailbox message FIFO queue, read the MAILBOX_MSGSTATUS_m register.

19.3.7 16-Bit Register Access

19.3.7.1 Description

So that 16-bit processors can access the mailbox module, the module allows 16-bit register read and write access, with restrictions for the MAILBOX_MESSAGE_m registers. The 16-bit half-words are organized in little endian fashion; that is, the least-significant 16 bits are at the low address and the most-significant 16 bits are at the high address (low address + 0x02).

All mailbox module registers can be read or written to directly using individual 16-bit accesses with no restriction on interleaving, except the MAILBOX_MESSAGE_m registers, which must always be accessed by either single 32-bit accesses or two consecutive 16-bit accesses.

CAUTION

When using 16-bit accesses, it is critical to ensure that the mailbox used has only one assigned receiver and only one assigned sender.

When using 16-bit accesses to the MAILBOX_MESSAGE_m registers, the order of access must be the least-significant half-word first (low address) and the most-significant half-word last (high address). This requirement is because of the update operation by the message FIFO of the MAILBOX_MSGSTATUS_m registers. The update of the FIFO queue contents and the associated status registers and possible interrupt generation occurs only when the most-significant 16 bits of a MAILBOX_MESSAGE_m are accessed.

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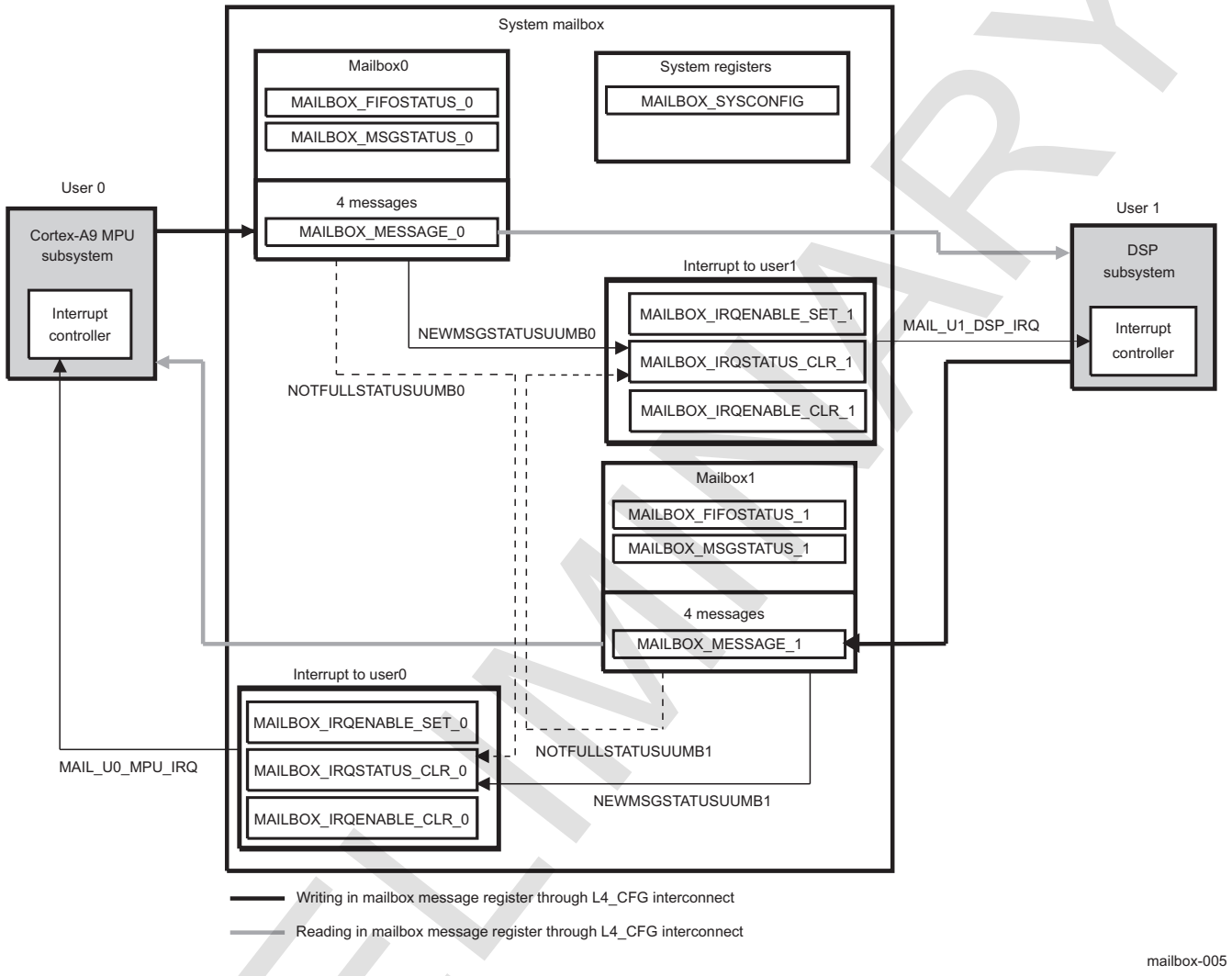
19.3.8 Example of Communication

Figure 19-5 shows an example of communication between Cortex-A9 MPU and DSP subsystems.

Figure 19-5. Example of Communication



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19.4 Mailbox Programming Guide

19.4.1 Mailbox Low-level Programming Models

This section covers the low-level hardware programming sequences for configuration and usage of the mailbox module.

19.4.1.1 Global Initialization

19.4.1.1.1 Surrounding Modules Global Initialization

This section identifies the requirements of initializing the surrounding modules when the mailbox module is to be used for the first time after a device reset. This initialization of surrounding modules is based on the integration of the mailbox.

See Section 19.2, *Mailbox Integration*, for further information.

Table 19-9. Global Initialization of Surrounding Modules for System Mailbox

Surrounding Modules	Comments
PRCM	Mailbox functional/interface clock must be enabled. For more information, see Section 3.6.14 , *CD_L4_CFG Clock Domain*, in Chapter 3, *Power, Reset, and Clock Management*.
Interrupt Controllers	Cortex-A9 MPU, or Cortex-M3 MPU, or DSP interrupt controller must be configured to enable the interrupt request generation to the Cortex-A9 MPU, or Cortex-M3 MPU, or DSP subsystem. For information about enabling interrupts in Cortex-A9 MPU INTC, see the *ARM Cortex™-A9 MPCore Technical Reference Manual* . For information about enabling interrupts in Cortex-M3 MPU INTC, see the *ARM Cortex™-M3 Technical Reference Manual* . For information about enabling interrupts in DSP INTC, see Chapter 5, *DSP Subsystem*.
Interconnect	For information about L4-CFG interconnect configuration, see Section 13.3, *L4 Interconnects,* in Chapter 13, *Interconnect*.

Table 19-10. Global Initialization of Surrounding Modules for IVA-HD Mailbox

Surrounding Modules	Comments
PRCM	Mailbox functional/interface clock must be enabled. For more information, see Chapter 3, *Power, Reset, and Clock Management*.
Interrupt Controllers	Cortex-A9 MPU, or Cortex-M3 MPU, or DSP, or iCONT1/iCONT2 interrupt controller must be configured to enable the interrupt request generation to the Cortex-A9 MPU, or Cortex-M3 MPU, or DSP, or IVA-HD subsystem. For information about enabling interrupts in Cortex-A9 MPU INTC, or Cortex-M3 MPU INTC, or DSP INTC, see Table 19-9, *Global Initialization of Surrounding Modules for System Mailbox*. For information about enabling interrupts in iCONT1/iCONT2, see , *iCONT* in Chapter 6, *IVA-HD Subsystem*.
Interconnect	For information about L3 interconnect configuration, see Section 13.2, *L3 Interconnects*, in Chapter 13, *Interconnect*.

19.4.1.1.2 Mailbox Global Initialization

19.4.1.1.2.1 Main Sequence - Mailbox Global Initialization

This procedure initializes the mailbox module after a power-on or software reset.

Table 19-11. Mailbox Global Initialization

Step	Register/ Bit Field / Programming Model	Value
Perform a software reset	MAILBOX_SYSCONFIG[0] SOFTRESET	0x1
Wait until reset is complete	MAILBOX_SYSCONFIG[0] SOFTRESET	= 0x0
Set idle mode configuration	MAILBOX_SYSCONFIG[3:2] SIDLEMODE	0x-

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19.4.1.2 Mailbox Operational Modes Configuration

19.4.1.2.1 Mailbox Processing modes

19.4.1.2.1.1 Main Sequence - Sending a Message (Polling Method)

Table 19-12. Sending a Message (Polling Method)

Step	Register/ Bit Field / Programming Model	Value
IF : Is FIFO full ?	MAILBOX_FIFOSTATUS_m[0] FIFOFULLMB	= 0x1
Wait until at least one message slot is available	MAILBOX_FIFOSTATUS_m[0] FIFOFULLMB	= 0x0
ELSE		
Write message	MAILBOX_MESSAGE_m[31:0] MESSAGEVALUEMBM	0x----
ENDIF		

19.4.1.2.1.2 Main Sequence - Sending a Message (Interupt Method)

Table 19-13. Sending a Message (Interupt Method)

Step	Register/ Bit Field / Programming Model	Value
IF : Is FIFO full ?	MAILBOX_FIFOSTATUS_m[0] FIFOFULLMB	= 0x1
Enable interrupt event	MAILBOX_IRQENABLE_SET_u[1+ m*2]	0x1
User (processor) can perform another task until interrupt occurs See Section 19.4.1.3.1 for interrupt handling in sending mode		
ELSE		
Write message	MAILBOX_MESSAGE_m[31:0] MESSAGEVALUEMBM	0x----
ENDIF		

19.4.1.2.1.3 Main Sequence - Receiving a Message (Polling Method)

Table 19-14. Receiving a Message (Polling Method)

Step	Register/ Bit Field / Programming Model	Value
IF : Number of messages is not equal to 0	MAILBOX_MSGSTATUS_m[2:0] NBOFMSGMB	!= 0x0
Read message	MAILBOX_MESSAGE_m[31:0] MESSAGEVALUEMBM	0x----
ENDIF		

19.4.1.2.1.4 Main Sequence - Receiving a Message (Interupt Method)

Table 19-15. Receiving a Message (Interupt Method)

Step	Register/ Bit Field / Programming Model	Value
Enable interrupt event	MAILBOX_IRQENABLE_SET_u[0 + m*2]	0x1
User (processor) can perform another task until interrupt occurs See Section 19.4.1.3.2 for interrupt handling in receiving mode		

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19.4.1.3 Mailbox Events Servicing

19.4.1.3.1 Events Servicing in Sending Mode

Table 19-16 describes the events servicing in sending mode.

Table 19-16. Events Servicing in Sending Mode

Step	Register/ Bit Field / Programming Model	Value
Read interrupt status bit	MAILBOX_IRQSTATUS_CLR_u[1 + m*2]	0x1
Write message	MAILBOX_MESSAGE_m[31:0] MESSAGEVALUEMBM	0x----
Write 1 to acknowledge interrupt	MAILBOX_IRQSTATUS_CLR_u[1 + m*2]	0x1

19.4.1.3.2 Events Servicing in Receiving Mode

Table 19-17 describes the events servicing in receiving mode.

Table 19-17. Events Servicing in Receiving Mode

Step	Register/ Bit Field / Programming Model	Value
Read interrupt status bit	MAILBOX_IRQSTATUS_CLR_u[0 + m*2]	0x1
IF : Number of messages is not equal to 0 ?	MAILBOX_MSGSTATUS_m[2:0] NBOFMSGMB	!= 0x0
Read message	MAILBOX_MESSAGE_m[31:0] MESSAGEVALUEMBM	0x----
ELSE		
Write 1 to acknowledge interrupt	MAILBOX_IRQSTATUS_CLR_u[0 + m*2]	0x1
ENDIF		

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19.5 Mailbox Register Manual

19.5.1 Mailbox Instance Summary

Table 19-18. System Mailbox Instance Summary

Module Name	Base Address L4_CFG Interconnect	Size
System Mailbox	0x4A0F 4000	4KB

Table 19-19. IVAHD Mailbox Instance Summary

Module Name	Base Address L3 Interconnect	Base Address DSP Subsystem Private Access	Base Address Private Access	Size
IVAHD Mailbox	0x5A05 A800	0x01E5 A800	0x008D A800	4KB

NOTE: Private access is an access that does not use the L3/L4 interconnects.

19.5.2 Mailbox Registers

19.5.2.1 Mailbox Register Summary

Table 19-20. System Mailbox Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	Physical Address L4_CFG Interconnect
MAILBOX_REVISION	R	32	0x0000 0000	0x4A0F 4000
MAILBOX_SYSCONFIG	RW	32	0x0000 0010	0x4A0F 4010
MAILBOX_MESSAGE_m (1)	RW	32	0x0000 0040 + (0x4 * m)	0x4A0F 4040 + (0x4 * m)
MAILBOX_FIFOSTATUS_m (1)	R	32	0x0000 0080 + (0x4 * m)	0x4A0F 4080 + (0x4 * m)
MAILBOX_MSGSTATUS_m (1)	R	32	0x0000 00C0 + (0x4 * m)	0x4A0F 40C0 + (0x4 * m)
MAILBOX_IRQSTATUS_RAW_u (2)	RW	32	0x0000 0100 + (0x10 * u)	0x4A0F 4100 + (0x10 * u)
MAILBOX_IRQSTATUS_CLR_u (2)	RW	32	0x0000 0104 + (0x10 * u)	0x4A0F 4104 + (0x10 * u)
MAILBOX_IRQENABLE_SET_u (2)	RW	32	0x0000 0108 + (0x10 * u)	0x4A0F 4108 + (0x10 * u)
MAILBOX_IRQENABLE_CLR_u (2)	RW	32	0x0000 010C + (0x10 * u)	0x4A0F 410C + (0x10 * u)
RESERVED			0x0000 0140	0x4A0F 4140

(1) m = 0 to 7
(2) u = 0 to 2

Table 19-21. IVAHD Mailbox Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	Physical Address L3 Interconnect	Physical Address DSP Private Access	Physical Address iCONT Private Access
MAILBOX_REVISION	R	32	0x0000 0000	0x5A05 A800	0x01E5 A800	0x008D A800
MAILBOX_SYSCONFIG	RW	32	0x0000 0010	0x5A05 A810	0x01E5 A810	0x008D A810
MAILBOX_MESSAGE_m (1)	RW	32	0x0000 0040 + (0x4 * m)	0x5A05 A840 + (0x4 * m)	0x01E5 A840 + (0x4 * m)	0x008D A840 + (0x4 * m)
MAILBOX_FIFOSTATUS_m (1)	R	32	0x0000 0080 + (0x4 * m)	0x5A05 A880 + (0x4 * m)	0x01E5 A880 + (0x4 * m)	0x008D A880 + (0x4 * m)

(1) m = 0 to 5

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Table 19-21. IVAHD Mailbox Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	Physical Address L3 Interconnect	Physical Address DSP Private Access	Physical Address iCONT Private Access
MAILBOX_MSGSTATUS_m [1]	R	32	0x0000 00C0 + (0x4 * m)	0x5A05 A8C0 + (0x4 * m)	0x01E5 A8C0 + (0x4 * m)	0x008D A8C0 + (0x4 * m)
MAILBOX_IRQSTATUS_RAW_u [2]	RW	32	0x0000 0100 + (0x10 * u)	0x5A05 A900 + (0x10 * u)	0x01E5 A900 + (0x10 * u)	0x008D A900 + (0x10 * u)
MAILBOX_IRQSTATUS_CLR_u [2]	RW	32	0x0000 0104 + (0x10 * u)	0x5A05 A904 + (0x10 * u)	0x01E5 A904 + (0x10 * u)	0x008D A904 + (0x10 * u)
MAILBOX_IRQENABLE_SET_u [2]	RW	32	0x0000 0108 + (0x10 * u)	0x5A05 A908 + (0x10 * u)	0x01E5 A908 + (0x10 * u)	0x008D A908 + (0x10 * u)
MAILBOX_IRQENABLE_CLR_u [2]	RW	32	0x0000 010C + (0x10 * u)	0x5A05 A90C + (0x10 * u)	0x01E5 A90C + (0x10 * u)	0x008D A90C + (0x10 * u)
RESERVED			0x0000 0140	0x5A05 A940	0x01E5 A940	0x008D A940

[2] u = 0 to 3

19.5.2.2 Mailbox Register Description

Table 19-22. MAILBOX_REVISION

Address Offset	0x0000 0000		
Physical Address	See Table 19-20	**Instance**	System Mailbox
	See Table 19-21	**Instance**	IVA-HD Mailbox
Description	This register contains the IP revision code		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP Revision	R	TI internal data

Table 19-23. Register Call Summary for Register MAILBOX_REVISION

Mailbox Register Manual

- Mailbox Register Summary: [0] [1]

Table 19-24. MAILBOX_SYSCONFIG

Address Offset	0x0000 0010		
Physical Address	See Table 19-20	**Instance**	System Mailbox
	See Table 19-21	**Instance**	IVA-HD Mailbox
Description	This register controls the various parameters of the communication interface		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												SIDLEMODE		RESERVED	SOFTRESET

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Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved	RW	0x0000000
3:2	SIDLEMODE	Idle Mode 0x0: Force-idle. An idle request is acknowledged unconditionally 0x1: No-idle. An idle request is never acknowledged 0x2: Smart-idle. Acknowledgement to an idle request is given based on the internal activity of the module based on the internal activity of the module 0x3: reserved do not use	RW	0x2
1	RESERVED	Reserved	RW	0
0	SOFTRESET	Softreset Read 0x0: Soft/Hard reset done Write 0x0: No action Read 0x1: Reset is ongoing Write 0x1: Start the soft reset sequence	RW	0

Table 19-25. Register Call Summary for Register MAILBOX_SYSCONFIG

Mailbox Functional Description • Mailbox Software Reset: [0] [1] • Mailbox Power Management: [2] [3]
Mailbox Programming Guide • Mailbox Global Initialization: [4] [5] [6]
Mailbox Register Manual • Mailbox Register Summary: [7] [8]

Table 19-26. MAILBOX_MESSAGE_m

Address Offset	0x0000 0040 + (0x4 * m)	**index:**	m = 0 to 7 (System Mailbox) or m = 0 to 5 (IVAHD Mailbox)
Physical Address	See Table 19-20	**Instance**	System Mailbox
	See Table 19-21	**Instance**	IVA-HD Mailbox
Description	The message register stores the next to be read message of the mailbox. Reads remove the message from the FIFO queue.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MESSAGEVALUEMBM																															

Bits	Field Name	Description	Type	Reset
31:0	MESSAGEVALUEMBM	Message in Mailbox	RW	0x0000 0000

Table 19-27. Register Call Summary for Register MAILBOX_MESSAGE_m

Mailbox Functional Description • Description: [0] [1] • Description: [2] [3] [4] • Description: [5] [6] [7] [8]
Mailbox Programming Guide • Mailbox Processing modes: [9] [10] [11] • Events Servicing in Sending Mode: [12] • Events Servicing in Receiving Mode: [13]

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Table 19-27. Register Call Summary for Register MAILBOX_MESSAGE_m (continued)

Mailbox Register Manual • Mailbox Register Summary: [14] [15]

Table 19-28. MAILBOX_FIFOSTATUS_m

Address Offset	0x0000 0080 + (0x4 * m)	**index:**	m = 0 to 7 (System Mailbox) or m = 0 to 5 (IVAHD Mailbox)
Physical Address	See Table 19-20	**Instance**	System Mailbox
	See Table 19-21	**Instance**	IVA-HD Mailbox
Description	The FIFO status register has the status related to the mailbox internal FIFO		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															FIFOFULLMBM

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reads returns 0	R	0x0000 0000
0	FIFOFULLMBM	Full flag for Mailbox Read 0x0: Mailbox FIFO is not full Read 0x1: Mailbox FIFO is full	R	0

Table 19-29. Register Call Summary for Register MAILBOX_FIFOSTATUS_m

Mailbox Functional Description • Description: [0] [1] • Description: [2]
Mailbox Programming Guide • Mailbox Processing modes: [3] [4] [5]
Mailbox Register Manual • Mailbox Register Summary: [6] [7]

Table 19-30. MAILBOX_MSGSTATUS_m

Address Offset	0x0000 00C0 + (0x4 * m)	**index:**	m = 0 to 7 (System Mailbox) or m = 0 to 5 (IVAHD Mailbox)
Physical Address	See Table 19-20	**Instance**	System Mailbox
	See Table 19-21	**Instance**	IVA-HD Mailbox
Description	The message status register has the status of the messages in the mailbox.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														NBOFMSGMBM	

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Bits	Field Name	Description	Type	Reset
31:3	RESERVED	Reserved. Read returns 0	R	0x0000 0000
2:0	NBOFMSGMBM	Number of unread messages in Mailbox Note: Limited to four messages per mailbox.	R	0x00

Table 19-31. Register Call Summary for Register MAILBOX_MSGSTATUS_m

Mailbox Functional Description • Description: [0] [1] • Description: [2] • Description: [3]
Mailbox Programming Guide • Mailbox Processing modes: [4] • Events Servicing in Receiving Mode: [5]
Mailbox Register Manual • Mailbox Register Summary: [6] [7]

Table 19-32. MAILBOX_IRQSTATUS_RAW_u

Address Offset	0x0000 0100 + (0x10 * u)	**index:**	u = 0 to 2 (System Mailbox) or u = 0 to 3 (IVA-HD Mailbox)
Physical Address	See Table 19-20	**Instance**	System Mailbox
	See Table 19-21	**Instance**	IVA-HD Mailbox
Description	The interrupt status register has the raw status for each event that may be responsible for the generation of an interrupt to the corresponding user - write 1 to a given bit sets this bit. This register is mainly used for debug purpose.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																NOTFULLSTATUSENUUMB7	NEWMSGSTATUSUUMB7	NOTFULLSTATUSUUMB6	NEWMSGSTATUSUUMB6	NOTFULLSTATUSUUMB5	NEWMSGSTATUSUUMB5	NOTFULLSTATUSUUMB4	NEWMSGSTATUSUUMB4	NOTFULLSTATUSUUMB3	NEWMSGSTATUSUUMB3	NOTFULLSTATUSUUMB2	NEWMSGSTATUSUUMB2	NOTFULLSTATUSUUMB1	NEWMSGSTATUSUUMB1	NOTFULLSTATUSUUMB0	NEWMSGSTATUSUUMB0

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Write 0's for future compatibility. Read returns 0.	RW	0
15	NOTFULLSTATUSENUUMB7	NotFull Status bit for User u, Mailbox 7 Read 0x0: No event pending (message queue full) Write 0x0: No action Read 0x1: Event pending (message queue not full) Write 0x1: Set the event (for debug)	RW	1
14	NEWMSGSTATUSUUMB7	NewMessage Status bit for User u, Mailbox 7 Read 0x0: No event (message) pending Write 0x0: No action Read 0x1: Event (message) pending Write 0x1: Set the event (for debug)	RW	0

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Bits	Field Name	Description	Type	Reset
13	NOTFULLSTATUSUUMB6	NotFull Status bit for User u, Mailbox 6 Read 0x0: No event pending (message queue full) Write 0x0: No action Read 0x1: Event pending (message queue not full) Write 0x1: Set the event (for debug)	RW	1
12	NEWMSGSTATUSUUMB6	NewMessage Status bit for User u, Mailbox 6 Read 0x0: No event (message) pending Write 0x0: No action Read 0x1: Event (message) pending Write 0x1: Set the event (for debug)	RW	0
11	NOTFULLSTATUSUUMB5	NotFull Status bit for User u, Mailbox 5 Read 0x0: No event pending (message queue full) Write 0x0: No action Read 0x1: Event pending (message queue not full) Write 0x1: Set the event (for debug)	RW	1
10	NEWMSGSTATUSUUMB5	NewMessage Status bit for User u, Mailbox 5 Read 0x0: No event (message) pending Write 0x0: No action Read 0x1: Event (message) pending Write 0x1: Set the event (for debug)	RW	0
9	NOTFULLSTATUSUUMB4	NotFull Status bit for User u, Mailbox 4 Read 0x0: No event pending (message queue full) Write 0x0: No action Read 0x1: Event pending (message queue not full) Write 0x1: Set the event (for debug)	RW	1
8	NEWMSGSTATUSUUMB4	NewMessage Status bit for User u, Mailbox 4 Read 0x0: No event (message) pending Write 0x0: No action Read 0x1: Event (message) pending Write 0x1: Set the event (for debug)	RW	0
7	NOTFULLSTATUSUUMB3	NotFull Status bit for User u, Mailbox 3 Read 0x0: No event pending (message queue full) Write 0x0: No action Read 0x1: Event pending (message queue not full) Write 0x1: Set the event (for debug)	RW	1
6	NEWMSGSTATUSUUMB3	NewMessage Status bit for User u, Mailbox 3 Read 0x0: No event (message) pending Write 0x0: No action Read 0x1: Event (message) pending Write 0x1: Set the event (for debug)	RW	0
5	NOTFULLSTATUSUUMB2	NotFull Status bit for User u, Mailbox 2 Read 0x0: No event pending (message queue full) Write 0x0: No action Read 0x1: Event pending (message queue not full) Write 0x1: Set the event (for debug)	RW	1

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Bits	Field Name	Description	Type	Reset
4	NEWMSGSTATUSUUMB2	NewMessage Status bit for User u, Mailbox 2 Read 0x0: No event (message) pending Write 0x0: No action Read 0x1: Event (message) pending Write 0x1: Set the event (for debug)	RW	0
3	NOTFULLSTATUSUUMB1	NotFull Status bit for User u, Mailbox 1 Read 0x0: No event pending (message queue full) Write 0x0: No action Read 0x1: Event pending (message queue not full) Write 0x1: Set the event (for debug)	RW	1
2	NEWMSGSTATUSUUMB1	NewMessage Status bit for User u, Mailbox 1 Read 0x0: No event (message) pending Write 0x0: No action Read 0x1: Event (message) pending Write 0x1: Set the event (for debug)	RW	0
1	NOTFULLSTATUSUUMB0	NotFull Status bit for User u, Mailbox 0 Read 0x0: No event pending (message queue full) Write 0x0: No action Read 0x1: Event pending (message queue not full) Write 0x1: Set the event (for debug)	RW	1
0	NEWMSGSTATUSUUMB0	NewMessage Status bit for User u, Mailbox 0 Read 0x0: No event (message) pending Write 0x0: No action Read 0x1: Event (message) pending Write 0x1: Set the event (for debug)	RW	0

Table 19-33. Register Call Summary for Register MAILBOX_IRQSTATUS_RAW_u

Mailbox Functional Description
- Mailbox Functional Description: [0]
- Mailbox Interrupt Requests: [1] [2] [3] [4] [5] [6]

Mailbox Register Manual
- Mailbox Register Summary: [7] [8]
- Mailbox Register Description: [9]

Table 19-34. MAILBOX_IRQSTATUS_CLR_u

Address Offset	0x0000 0104 + (0x10 * u)	**index:**	u = 0 to 2 (System Mailbox) or u = 0 to 3 (IVA-HD Mailbox)
Physical Address	See Table 19-20	**Instance**	System Mailbox
	See Table 19-21	**Instance**	IVA-HD Mailbox
Description	The interrupt status register has the status combined with irq-enable for each event that may be responsible for the generation of an interrupt to the corresponding user - write 1 to a given bit resets this bit		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																NOTFULLSTATUSENUUMB7	NEWMSGSTATUSENUUMB7	NOTFULLSTATUSENUUMB6	NEWMSGSTATUSENUUMB6	NOTFULLSTATUSENUUMB5	NEWMSGSTATUSENUUMB5	NOTFULLSTATUSENUUMB4	NEWMSGSTATUSENUUMB4	NOTFULLSTATUSENUUMB3	NEWMSGSTATUSENUUMB3	NOTFULLSTATUSENUUMB2	NEWMSGSTATUSENUUMB2	NOTFULLSTATUSENUUMB1	NEWMSGSTATUSENUUMB1	NOTFULLSTATUSENUUMB0	NEWMSGSTATUSENUUMB0

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Write 0's for future compatibility. Read returns 0.	RW	0
15	NOTFULLSTATUSENUUMB7	NotFull Status bit for User u, Mailbox 7 Read 0x0: No event pending (message queue full) Write 0x0: No action Read 0x1: Event pending (message queue not full) Write 0x1: Clear pending event, if any	RW	0
14	NEWMSGSTATUSENUUMB7	NewMessage Status bit for User u, Mailbox 7 Read 0x0: No event (message) pending Write 0x0: No action Read 0x1: Event (message) pending Write 0x1: Clear pending event, if any	RW	0
13	NOTFULLSTATUSENUUMB6	NotFull Status bit for User u, Mailbox 6 Read 0x0: No event pending (message queue full) Write 0x0: No action Read 0x1: Event pending (message queue not full) Write 0x1: Clear pending event, if any	RW	0
12	NEWMSGSTATUSENUUMB6	NewMessage Status bit for User u, Mailbox 6 Read 0x0: No event (message) pending Write 0x0: No action Read 0x1: Event (message) pending Write 0x1: Clear pending event, if any	RW	0
11	NOTFULLSTATUSENUUMB5	NotFull Status bit for User u, Mailbox 5 Read 0x0: No event pending (message queue full) Write 0x0: No action Read 0x1: Event pending (message queue not full) Write 0x1: Clear pending event, if any	RW	0
10	NEWMSGSTATUSENUUMB5	NewMessage Status bit for User u, Mailbox 5 Read 0x0: No event (message) pending Write 0x0: No action Read 0x1: Event (message) pending Write 0x1: Clear pending event, if any	RW	0
9	NOTFULLSTATUSENUUMB4	NotFull Status bit for User u, Mailbox 4 Read 0x0: No event pending (message queue full) Write 0x0: No action Read 0x1: Event pending (message queue not full) Write 0x1: Clear pending event, if any	RW	0

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Bits	Field Name	Description	Type	Reset
8	NEWMSGSTATUSENUUMB4	NewMessage Status bit for User u, Mailbox 4 Read 0x0: No event (message) pending Write 0x0: No action Read 0x1: Event (message) pending Write 0x1: Clear pending event, if any	RW	0
7	NOTFULLSTATUSENUUMB3	NotFull Status bit for User u, Mailbox 3 Read 0x0: No event pending (message queue full) Write 0x0: No action Read 0x1: Event pending (message queue not full) Write 0x1: Clear pending event, if any	RW	0
6	NEWMSGSTATUSENUUMB3	NewMessage Status bit for User u, Mailbox 3 Read 0x0: No event (message) pending Write 0x0: No action Read 0x1: Event (message) pending Write 0x1: Clear pending event, if any	RW	0
5	NOTFULLSTATUSENUUMB2	NotFull Status bit for User u, Mailbox 2 Read 0x0: No event pending (message queue full) Write 0x0: No action Read 0x1: Event pending (message queue not full) Write 0x1: Clear pending event, if any	RW	0
4	NEWMSGSTATUSENUUMB2	NewMessage Status bit for User u, Mailbox 2 Read 0x0: No event (message) pending Write 0x0: No action Read 0x1: Event (message) pending Write 0x1: Clear pending event, if any	RW	0
3	NOTFULLSTATUSENUUMB1	NotFull Status bit for User u, Mailbox 1 Read 0x0: No event pending (message queue full) Write 0x0: No action Read 0x1: Event pending (message queue not full) Write 0x1: Clear pending event, if any	RW	0
2	NEWMSGSTATUSENUUMB1	NewMessage Status bit for User u, Mailbox 1 Read 0x0: No event (message) pending Write 0x0: No action Read 0x1: Event (message) pending Write 0x1: Clear pending event, if any	RW	0
1	NOTFULLSTATUSENUUMB0	NotFull Status bit for User u, Mailbox 0 Read 0x0: No event pending (message queue full) Write 0x0: No action Read 0x1: Event pending (message queue not full) Write 0x1: Clear pending event, if any	RW	0
0	NEWMSGSTATUSENUUMB0	NewMessage Status bit for User u, Mailbox 0 Read 0x0: No event (message) pending Write 0x0: No action Read 0x1: Event (message) pending Write 0x1: Clear pending event, if any	RW	0

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Table 19-35. Register Call Summary for Register MAILBOX_IRQSTATUS_CLR_u

Mailbox Functional Description
- Mailbox Functional Description: [0]
- Mailbox Interrupt Requests: [1] [2] [3] [4] [5]
- Description: [6] [7]

Mailbox Programming Guide
- Events Servicing in Sending Mode: [8] [9]
- Events Servicing in Receiving Mode: [10] [11]

Mailbox Register Manual
- Mailbox Register Summary: [12] [13]
- Mailbox Register Description: [14]

Table 19-36. MAILBOX_IRQENABLE_SET_u

Address Offset	0x0000 0108 + (0x10 * u)	**index:**	u = 0 to 2 (System Mailbox) or u = 0 to 3 (IVA-HD Mailbox)
Physical Address	See Table 19-20	**Instance**	System Mailbox
	See Table 19-21	**Instance**	IVA-HD Mailbox
Description	The interrupt enable register enables to unmask the module internal source of interrupt to the corresponding user. This register is write 1 to set.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																NOTFULLENABLEUUMB7	NEWMSGENABLEUUMB7	NOTFULLENABLEUUMB6	NEWMSGENABLEUUMB6	NOTFULLENABLEUUMB5	NEWMSGENABLEUUMB5	NOTFULLENABLEUUMB4	NEWMSGENABLEUUMB4	NOTFULLENABLEUUMB3	NEWMSGENABLEUUMB3	NOTFULLENABLEUUMB2	NEWMSGENABLEUUMB2	NOTFULLENABLEUUMB1	NEWMSGENABLEUUMB1	NOTFULLENABLEUUMB0	NEWMSGENABLEUUMB0

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Write 0's for future compatibility. Read returns 0.	RW	0
15	NOTFULLENABLEUUMB7	NotFull Enable bit for User u, Mailbox 7 Read 0x0: Interupt disabled Write 0x0: No action Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW	0
14	NEWMSGENABLEUUMB7	NewMessage Enable bit for User u, Mailbox 7 Read 0x0: Interupt disabled Write 0x0: No action Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW	0
13	NOTFULLENABLEUUMB6	NotFull Enable bit for User u, Mailbox 6 Read 0x0: Interupt disabled Write 0x0: No action Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW	0

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Bits	Field Name	Description	Type	Reset
12	NEWMSGENABLEUUMB6	NewMessage Enable bit for User u, Mailbox 6 Read 0x0: Interupt disabled Write 0x0: No action Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW	0
11	NOTFULLENABLEUUMB5	NotFull Enable bit for User u, Mailbox 5 Read 0x0: Interupt disabled Write 0x0: No action Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW	0
10	NEWMSGENABLEUUMB5	NewMessage Enable bit for User u, Mailbox 5 Read 0x0: Interupt disabled Write 0x0: No action Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW	0
9	NOTFULLENABLEUUMB4	NotFull Enable bit for User u, Mailbox 4 Read 0x0: Interupt disabled Write 0x0: No action Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW	0
8	NEWMSGENABLEUUMB4	NewMessage Enable bit for User u, Mailbox 4 Read 0x0: Interupt disabled Write 0x0: No action Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW	0
7	NOTFULLENABLEUUMB3	NotFull Enable bit for User u, Mailbox 3 Read 0x0: Interupt disabled Write 0x0: No action Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW	0
6	NEWMSGENABLEUUMB3	NewMessage Enable bit for User u, Mailbox 3 Read 0x0: Interupt disabled Write 0x0: No action Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW	0
5	NOTFULLENABLEUUMB2	NotFull Enable bit for User u, Mailbox 2 Read 0x0: Interupt disabled Write 0x0: No action Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW	0
4	NEWMSGENABLEUUMB2	NewMessage Enable bit for User u, Mailbox 2 Read 0x0: Interupt disabled Write 0x0: No action Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW	0

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Bits	Field Name	Description	Type	Reset
3	NOTFULLENABLEUUMB1	NotFull Enable bit for User u, Mailbox 1 Read 0x0: Interupt disabled Write 0x0: No action Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW	0
2	NEWMSGENABLEUUMB1	NewMessage Enable bit for User u, Mailbox 1 Read 0x0: Interupt disabled Write 0x0: No action Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW	0
1	NOTFULLENABLEUUMB0	NotFull Enable bit for User u, Mailbox 0 Read 0x0: Interupt disabled Write 0x0: No action Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW	0
0	NEWMSGENABLEUUMB0	NewMessage Enable bit for User u, Mailbox 0 Read 0x0: Interupt disabled Write 0x0: No action Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW	0

Table 19-37. Register Call Summary for Register MAILBOX_IRQENABLE_SET_u

Mailbox Functional Description • Mailbox Functional Description: [0] • Mailbox Interrupt Requests: [1] [2] [3] • Description: [4] [5] [6]
Mailbox Programming Guide • Mailbox Processing modes: [7] [8]
Mailbox Register Manual • Mailbox Register Summary: [9] [10] • Mailbox Register Description: [11]

Table 19-38. MAILBOX_IRQENABLE_CLR_u

Address Offset	0x0000 010C + (0x10 * u)	**index:**	u = 0 to 2 (System Mailbox) or u = 0 to 3 (IVA-HD Mailbox)
Physical Address	See Table 19-20	**Instance**	System Mailbox
	See Table 19-21	**Instance**	IVA-HD Mailbox
Description	The interrupt enable register enables to mask the module internal source of interrupt to the corresponding user. This register is write 1 to clear.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																NOTFULLENABLEUUMB7	NEWMSGENABLEUUMB7	NOTFULLENABLEUUMB6	NEWMSGENABLEUUMB6	NOTFULLENABLEUUMB5	NEWMSGENABLEUUMB5	NOTFULLENABLEUUMB4	NEWMSGENABLEUUMB4	NOTFULLENABLEUUMB3	NEWMSGENABLEUUMB3	NOTFULLENABLEUUMB2	NEWMSGENABLEUUMB2	NOTFULLENABLEUUMB1	NEWMSGENABLEUUMB1	NOTFULLENABLEUUMB0	NEWMSGENABLEUUMB0

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Write 0's for future compatibility. Read returns 0.	RW	0
15	NOTFULLENABLEUUMB7	NotFull Enable bit for User u, Mailbox 7 Read 0x0: Interupt disabled Write 0x0: No action Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW	0
14	NEWMSGENABLEUUMB7	NewMessage Enable bit for User u, Mailbox 7 Read 0x0: Interupt disabled Write 0x0: No action Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW	0
13	NOTFULLENABLEUUMB6	NotFull Enable bit for User u, Mailbox 6 Read 0x0: Interupt disabled Write 0x0: No action Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW	0
12	NEWMSGENABLEUUMB6	NewMessage Enable bit for User u, Mailbox 6 Read 0x0: Interupt disabled Write 0x0: No action Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW	0
11	NOTFULLENABLEUUMB5	NotFull Enable bit for User u, Mailbox 5 Read 0x0: Interupt disabled Write 0x0: No action Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW	0
10	NEWMSGENABLEUUMB5	NewMessage Enable bit for User u, Mailbox 5 Read 0x0: Interupt disabled Write 0x0: No action Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW	0
9	NOTFULLENABLEUUMB4	NotFull Enable bit for User u, Mailbox 4 Read 0x0: Interupt disabled Write 0x0: No action Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW	0

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Bits	Field Name	Description	Type	Reset
8	NEWMSGENABLEUUMB4	NewMessage Enable bit for User u, Mailbox 4 Read 0x0: Interupt disabled Write 0x0: No action Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW	0
7	NOTFULLENABLEUUMB3	NotFull Enable bit for User u, Mailbox 3 Read 0x0: Interupt disabled Write 0x0: No action Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW	0
6	NEWMSGENABLEUUMB3	NewMessage Enable bit for User u, Mailbox 3 Read 0x0: Interupt disabled Write 0x0: No action Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW	0
5	NOTFULLENABLEUUMB2	NotFull Enable bit for User u, Mailbox 2 Read 0x0: Interupt disabled Write 0x0: No action Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW	0
4	NEWMSGENABLEUUMB2	NewMessage Enable bit for User u, Mailbox 2 Read 0x0: Interupt disabled Write 0x0: No action Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW	0
3	NOTFULLENABLEUUMB1	NotFull Enable bit for User u, Mailbox 1 Read 0x0: Interupt disabled Write 0x0: No action Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW	0
2	NEWMSGENABLEUUMB1	NewMessage Enable bit for User u, Mailbox 1 Read 0x0: Interupt disabled Write 0x0: No action Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW	0
1	NOTFULLENABLEUUMB0	NotFull Enable bit for User u, Mailbox 0 Read 0x0: Interupt disabled Write 0x0: No action Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW	0
0	NEWMSGENABLEUUMB0	NewMessage Enable bit for User u, Mailbox 0 Read 0x0: Interupt disabled Write 0x0: No action Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW	0

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Table 19-39. Register Call Summary for Register MAILBOX_IRQENABLE_CLR_u

Mailbox Functional Description • Mailbox Functional Description: [0] • Mailbox Interrupt Requests: [1] [2] [3]
Mailbox Register Manual • Mailbox Register Summary: [4] [5] • Mailbox Register Description: [6]

NOTE: For each interrupt status and enable register (MAILBOX_IRQSTATUS_RAW_u, MAILBOX_IRQSTATUS_CLR_u, MAILBOX_IRQENABLE_SET_u and MAILBOX_IRQENABLE_CLR_u), bits [15:12] have the given meaning only for the System Mailbox instance. For the IVA-HD Mailbox instance, these bits are considered as Reserved.

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Memory Management Units

This chapter describes the memory management units (MMUs).

Topic **Page**

20.1 MMU Overview **4164**
20.2 MMU Integration **4165**
20.3 MMU Functional Description **4168**
20.4 MMU Low-level Programming Models **4181**
20.5 MMU Register Manual **4185**

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20.1 MMU Overview

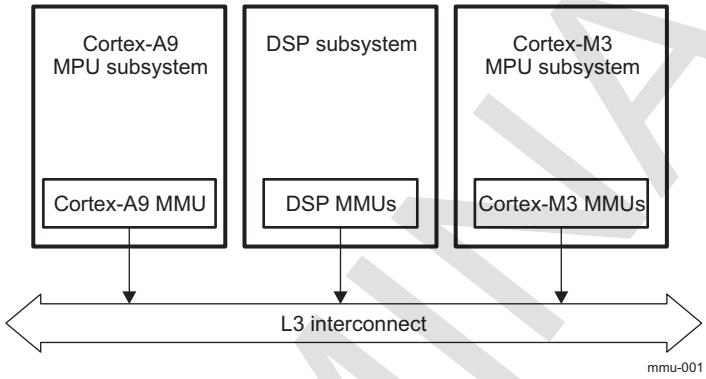
A memory management unit (MMU) is a hardware component responsible for handling accesses to memory requested by a processing unit. MMU functions include translation of virtual addresses to physical addresses (that is, virtual memory management) and cache control.

The device contains the following MMUs:

- In DSP - L1 Shared cache MMU and attribute MMU.
- In Dual Cortex-M3 MPU Subsystem - L1 Shared cache MMU and L2 MMU
- Cortex-A9 MMU

Figure 20-1 shows the MMU instances in the device.

Figure 20-1. Device MMU Instances



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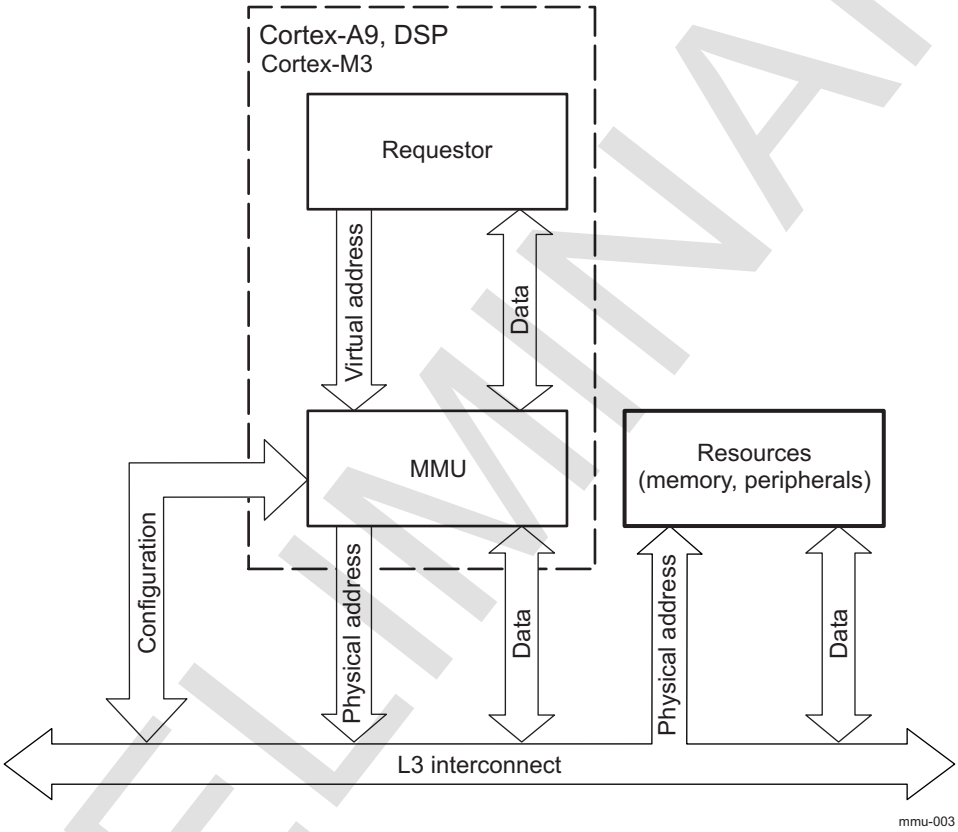
20.2 MMU Integration

This section describes module integration in the device, including information about clocks, resets, and hardware requests.

The MMU communicates accesses from the requestor (DSP, Cortex-M3 microprocessor unit (MPU), or Cortex-A9 MPU) to the L3 main interconnect, performing virtual to physical address translation. Although all MMUs are programmed (configured) through the L3 interconnect, the DSP MMU can be programmed both through the L3 interconnect or through the DSP local interconnect. DSP MMU and Cortex-M3 MMU error conditions are signaled as interrupts to the system main processor Cortex-A9 MPU.

Figure 20-2 shows typical MMU integration.

Figure 20-2. MMU Integration



NOTE: All MMUs are programmed through the L3 interconnect.

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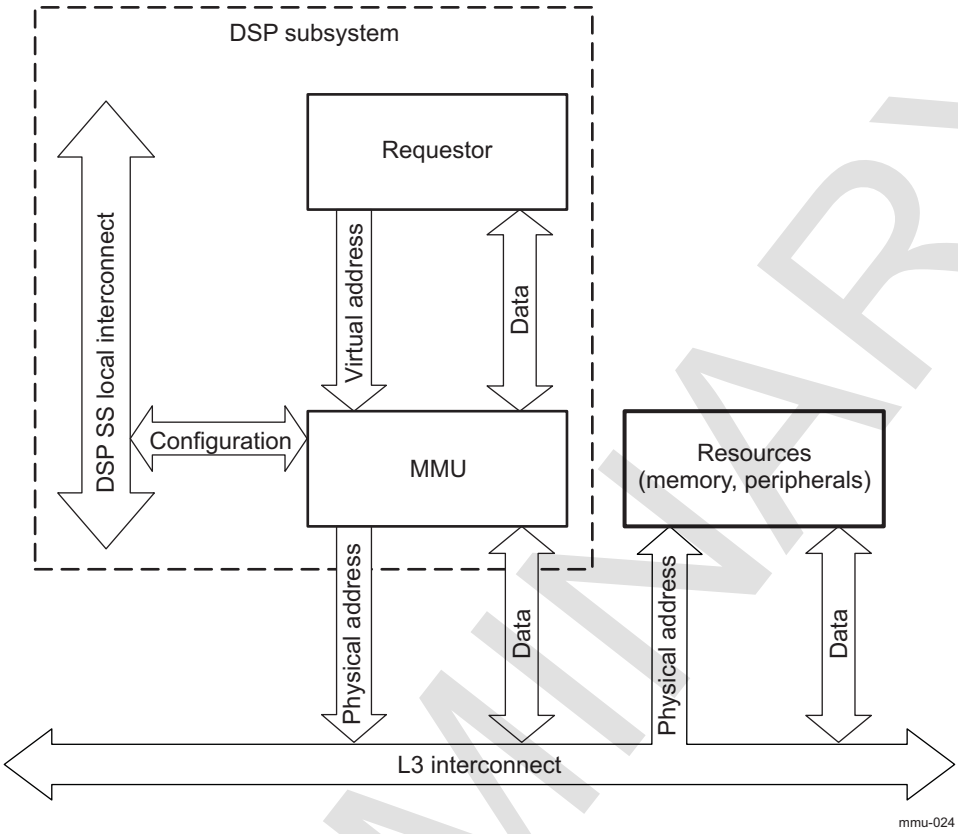
Figure 20-3. DSP MMU Integration



NOTE: The DSP MMU can be programmed from both the DSP local interconnect and from the L3 interconnect.

Table 20-1 through Table 20-3 summarize the MMU integration in the various modules of the device.

Table 20-1. Integration Attributes

Module Instance	Power Domain
CORTEXM3_L2MMU and CORTEXM3_SCACHE_MMU	PD_CORE
CORTEXA9_MMU	PD_MPU

Table 20-2. Clocks and Resets

Clocks				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
CORTEXA9_MMU	ARM_FCLK	MPU_DPLL_CLK	MPU DPLL	Internal clock in the Cortex-A9 MPU subsystem; supplies the MMU in Cortex-A9.
CORTEXM3_L2MMU and CORTEXM3_SCACHE_MMU	MPU_M3_CLK	MPU_M3_CLK	PRCM	External clock from the power, reset, and clock management (PRCM) module; supplies the shared cache MMU and L2 MMU in Cortex-M3.
Resets				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
CORTEXM3_L2MMU	CORTEXM3_PWRON_RST	CORTEXM3_PWRON_RST	PRCM	Power-on reset signal for the Cortex-M3 MPU subsystem
	CORTEXM3_RST3	CORTEXM3_RST3	PRCM	Reset signal to the L2 MMU

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Table 20-2. Clocks and Resets (continued)

CORTEXM3_SCACHE_MMU	CORTEXM3_RST3	CORTEXM3_RST3	PRCM	Reset signal for the shared cache MMU
	CORTEXM3_RET_RST	CORTEXM3_RET_RST	PRCM	Retention reset signal for the Cortex-M3 MPU subsystem
CORTEXA9_MMU	MPU_PWRON_RST	MPU_PWRON_RST	PRCM	Power-on reset signal to the MMU and the rest of the Cortex-A9 MPU subsystem
	MPU_RST	MPU_RST	PRCM	Reset signal to the MMU and the rest of the Cortex-A9 MPU subsystem

Table 20-3. Hardware Requests

		Interrupt Requests		
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
CORTEXM3_L2MMU	CORTEXM3_MMU_IRQ	MA_IRQ_100	MPU_INTC	Cortex-M3 MPU L2MMU interrupt to the main MPU subsystem
	XLATE_MMU_FAULT	MM_IRQ_0	CortexM3_INTC	Internal interrupt from the L2MMU to the Cortex-M3 interrupt controller (INTC)
CORTEXM3_SCACHE_MMU	SHARED_CACHE_MMU_CPU_INT	MM_IRQ_1	CortexM3_INTC	Internal interrupt from the shared cache MMU to the CortexM3 INTC

NOTE:

- For a description of the interrupt source, see Section 20.3.5, *Interrupt Requests*.

There are 5 MMU modules in the device:

- Shared cache MMU – there are two Share cache MMUs, one in the Cortex-M3 MPU and other in DSP subsystem. Refer to the corresponding chapters for more information.
- L2 MMUs – there are two L2 MMUs, one in the Cortex-M3 MPU and other in DSP subsystem. The L2 MMUs are directly operating with the L3 interconnect (shared device memory space). These L2 MMUs are described in this chapter.
- Cortex-A9 MMU – this MMU is located in the ARM Cortex-A9 processor. For information about this MMU, see the ARM® Cortex™-A9 MPCore Technical Reference Manual.

NOTE: There is PAT module in the Dynamic Memory Manager, which has similar to the MMU functionality. Refer to the DMM chapter, for more information.

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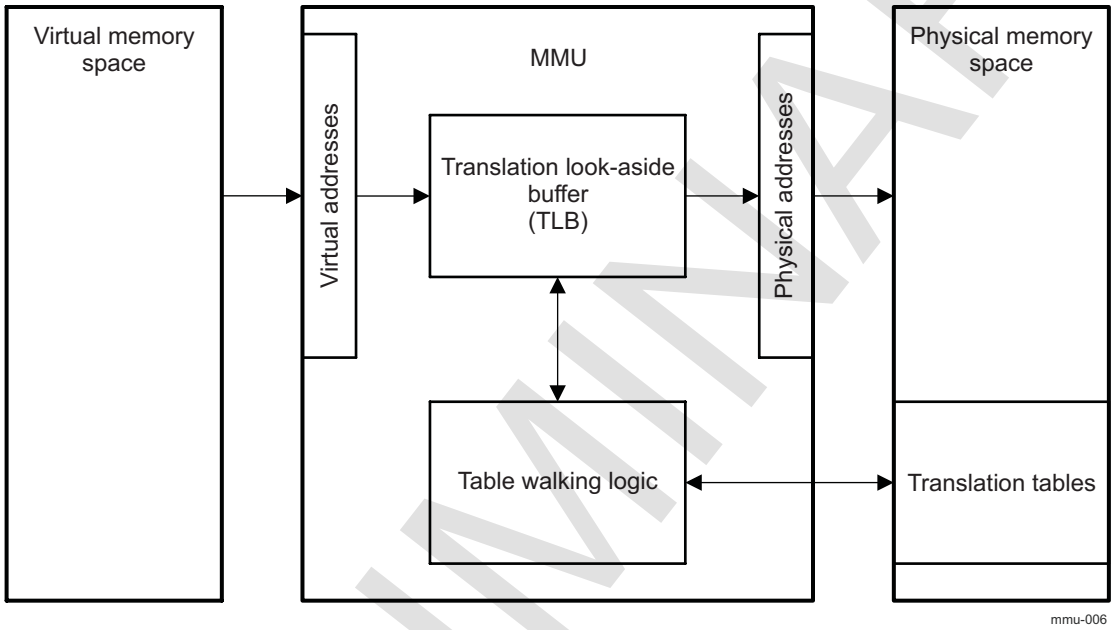
20.3 MMU Functional Description

20.3.1 MMU Block Diagram

The MMU manages the virtual to physical address translation for external addresses, as well as endianness conversion. The MMU can be programmed through the L3 interconnect. MMU programming is expected to be accomplished by the Cortex-A9 MPU, except for the DSP MMU, of which the configuration can be accomplished through the DSP local interconnect.

Figure 20-4 is the MMU block diagram.

Figure 20-4. MMU Block Diagram



Each table entry describes the translation of one contiguous memory region. For a description of the structure of these tables, see Section 20.3.1.2, *Translation Tables*.

Two major functional units exist in the MMU to provide address translation automatically based on the table entries:

- The table walker automatically retrieves the correct translation table entry for a requested translation. If two-level translation is used (for the translation of small memory pages), the table walker also automatically reads the required second-level translation table entry. The two-level translation is described later in the chapter.
- The translation look-aside buffer (TLB) stores recently used translation entries, acting like a cache of the translation table.

20.3.1.1 MMU Address Translation Process

Whenever an address translation is requested (that is, for every access with the MMU enabled), the MMU first checks whether the translation is contained in the TLB, which acts like a cache storing recent translations. The TLB can also be programmed manually to ensure that time-critical data can be translated without delay.

If the requested translation is not in the TLB, the table-walking logic retrieves this translation from the translation table(s), and then updates the TLB. The address translation is then performed. Figure 20-5 summarizes the process.

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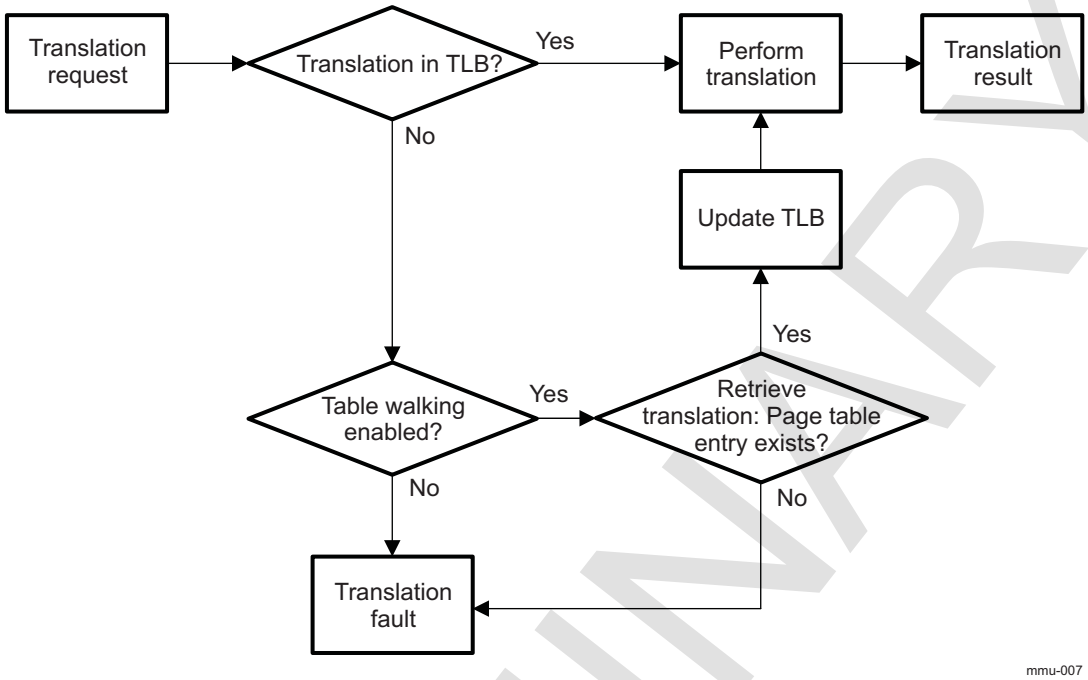
Figure 20-5. Translation Process



20.3.1.2 Translation Tables

The translation of virtual to physical addresses is based on entries in translation tables that define the following properties:

- Address translation, that is, the correspondence between virtual and physical addresses
- Size of the memory region the entry translates
- Endianness, data access size, and the mixed property of this memory region

The virtual addresses index the translation tables. Each virtual address corresponds to exactly one entry in the translation table.

20.3.1.2.1 Translation Table Hierarchy

When developing a table-based address translation scheme, one of the most important design parameters is the memory page size described by each translation table entry. MMU instances support 4KB and 64KB pages, a 1MB section, and a 16MB supersection. Using bigger page sizes means a smaller translation table.

Using a smaller page size greatly increases the efficiency of dynamic memory allocation and defragmentation. That is why many operating systems (OSs) can operate on memory blocks as small as 4KB; however, the smaller size implies a more complex table structure.

A quick calculation shows that using 4KB memory pages with one translation table would require one million entries to span the entire 4GB address range. The table itself would be 32MB, a size that is not feasible.

However, using bigger pages greatly reduces the functionality of the OS memory management. Implementing a two-level hierarchy reconciles these two requirements. Within this hierarchy, one first-level translation table describes the translation properties based on 1MB memory regions.

Each of the entries in this first-level translation table can specify the following:

- The translation properties for a big memory section. This memory section can be either 1MB (section) or 16MB (supersection). In this case, all translation parameters are specified in the first-level translation table entry.

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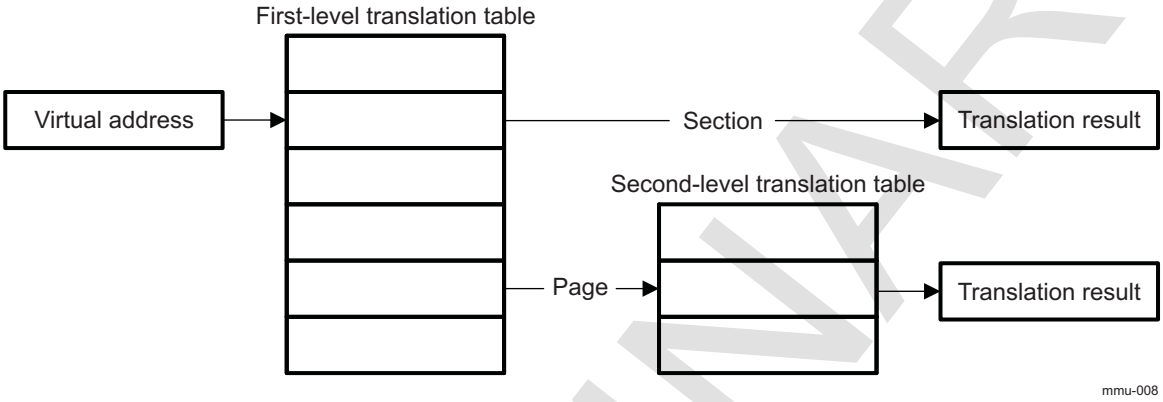
- A pointer to a second-level translation table that specifies individual translation properties based on smaller pages within the 1MB page of memory. These pages can be either 64KB (large page) or 4KB (small page). In this case, the actual translation parameters are specified in the second-level translation table entry. The first-level translation table entry specifies only the base address of the second-level translation table.

This hierarchical approach means that additional translation information for smaller pages must be provided only when the pages are actually used. Figure 20-6 shows the hierarchy.

Figure 20-6. Translation Hierarchy



The structure of the first and second-level translation tables and their entries are described in more detail in Section 20.3.1.2.2, *First-Level Translation Table*, and Section 20.3.1.2.3, *Two-Level Translation*.

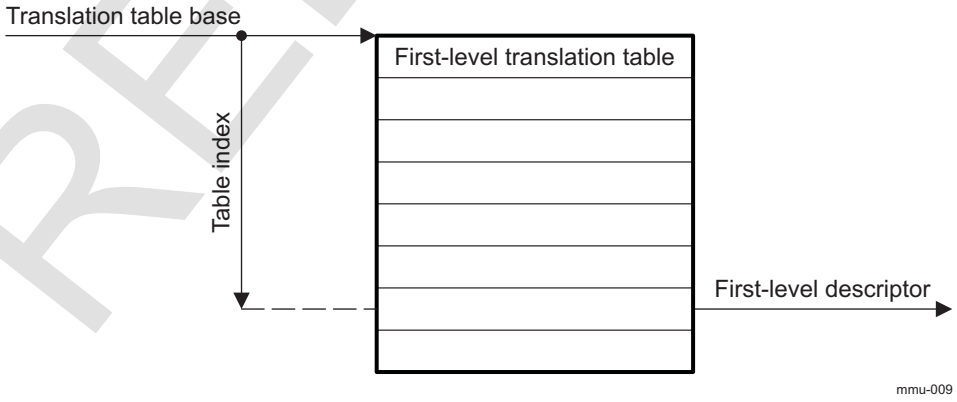
20.3.1.2.2 First-Level Translation Table

The first-level translation table describes the translation properties for 1MB sections. To describe a 4GB address range requires 4096 32-bit entries (so-called first-level descriptors).

The first-level translation table start address must be aligned on a multiple of the table size with a 128-byte minimum. Consequently, an alignment of at least 16K bytes is required for a complete 4096-entry table; that is, at least the last fourteen address bits must be zero.

The start address of the first-level translation table is specified by the so-called translation table base. The table is indexed by the upper 12-bits of the virtual address. Figure 20-7 shows this mechanism.

Figure 20-7. First-level Descriptor Address Calculation



To summarize, the translation table base and the translation table index together define the first-level descriptor address. Figure 20-8 outlines the precise mechanism used to calculate this address.

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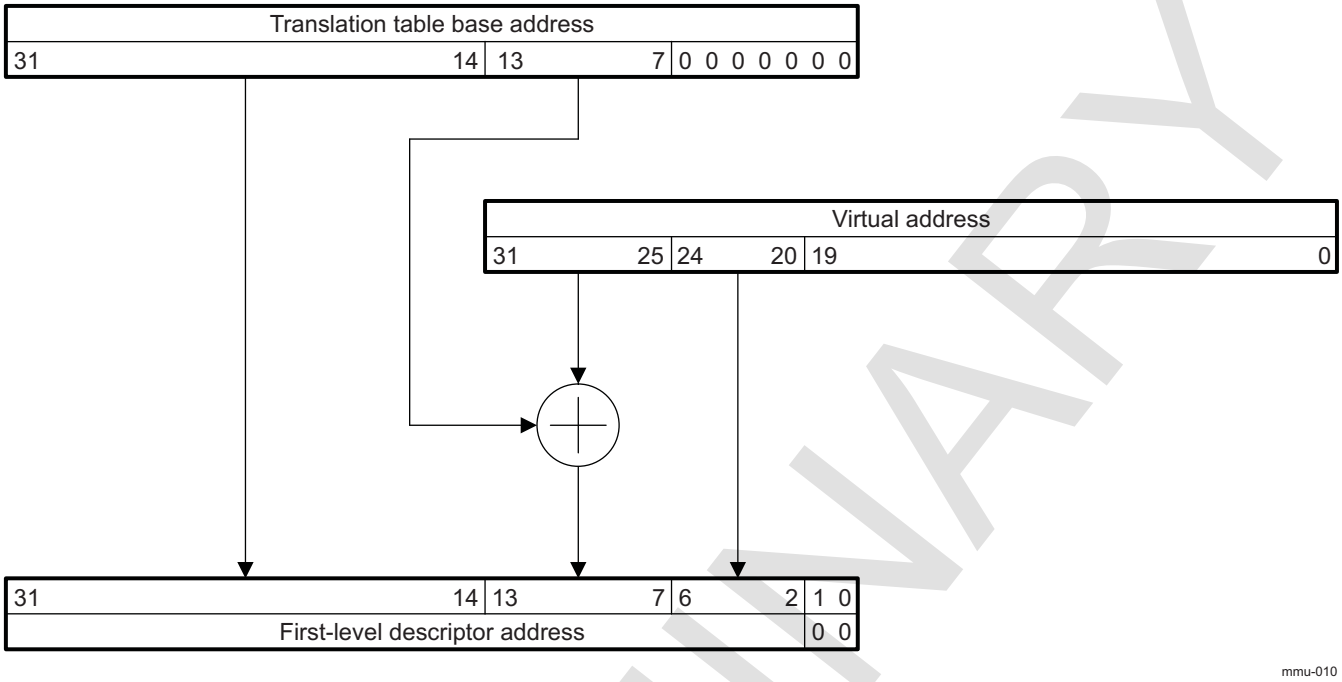
Figure 20-8. Detailed First-Level Descriptor Address Calculation



As an example of this mechanism, consider a translation table base address of 0x8000:0000 and a virtual address of 0x1234:5678. In this case, the first-level descriptor address is 0x8000:0000 + (0x123 2) = 0x8000:048C.

20.3.1.2.2.1 First-Level Descriptor Format

Each first-level descriptor provides either the complete address translation for 1MB or 16MB sections or provides a pointer to a second-level translation table for 4KB or 64KB pages. Table 20-4 shows the first-level descriptor format.

Table 20-4. First-Level Descriptor Format

First-Level Descriptor Format												
31:24	23:20	19	18	17	16	15	14:12	11:10	9:2	1	0	
X										0	0	Fault
Second-Level Translation Table Base Address									X	0	1	Page
Section Base Address		X	0	M	X	E (1)	X	ES	X	1	0	Section
Supersection Base Address	X		1	M	X	E	X	ES	X	1	0	Supersection
X										1	1	Fault

(1) See for endianness limitations.

M = Mixed region: 0 = Page-based endianness, 1 = Access-based endianness

E = Endianness: 0 = Little endian, 1 = Big endian (endianness is locked on little endian)

ES = Element Size: 00 = 8-bit, 01= 16-bit, 10 = 32-bit, 11 = No endianness conversion

X = Don't care

20.3.1.2.2.2 First-Level Page Descriptor Format

If a translation granularity smaller than 1MB is required, a two-level translation process is used. In this case, the first-level block descriptor specifies only the start address of a second-level translation table. The second-level translation table entries specify the actual translation properties.

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20.3.1.2.2.3 First-Level Section Descriptor Format

Each section descriptor in the first-level translation table specifies the complete translation properties for a 1MB section or a 16MB supersection.

NOTE: Supersection descriptors must be repeated 16 times, because each descriptor in the first-level translation table describes 1MB of memory. If an access points to a descriptor that is not initialized, the MMU will behave in an unpredictable way.

In addition to the address translation itself, three parameters are specified in the section descriptors:

- Endianness

  The *endianness* parameter specifies whether the memory section uses a big- or little-endian data format. This parameter is locked to little endian. See for more information.

- Element size

  The *element size* parameter can optionally specify the data access size (8, 16, or 32 bits) for all data items in the defined section.

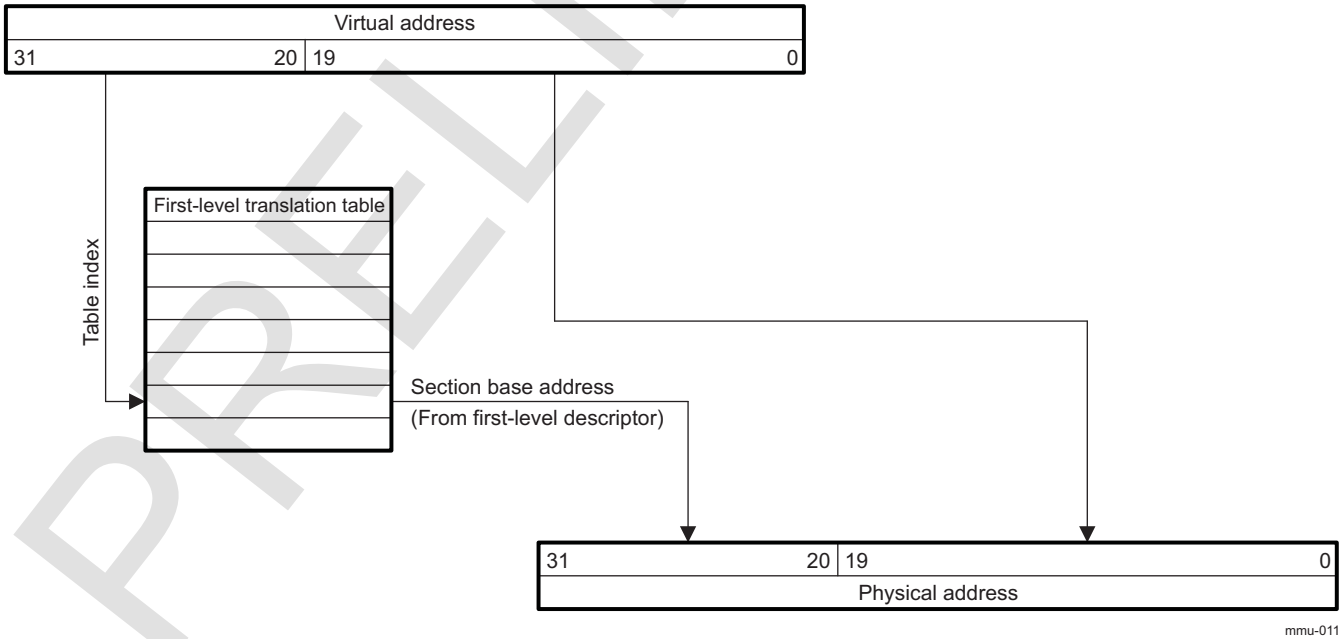
- Mixed region

  The *mixed region* parameter specifies whether the information about the data access size is detected from the access itself (access-based detection) or if the specified element size parameter is used (page-based detection). For example, the specified element size parameter can be used when several smaller sized accesses are packed into a bigger sized access, such as two 16-bit accesses packed into one 32-bit access. In this case, with no specified data access size, 32 bits would be the access size detected, leading to an incorrect result. To avoid this problem, specify the data access size for the memory section.

20.3.1.2.2.4 Section Translation Summary

Sections and supersections can be translated based solely on the information in the first-level translation table. Figure 20-9 summarizes the address translation process for a section.

Figure 20-9. Section Translation Summary



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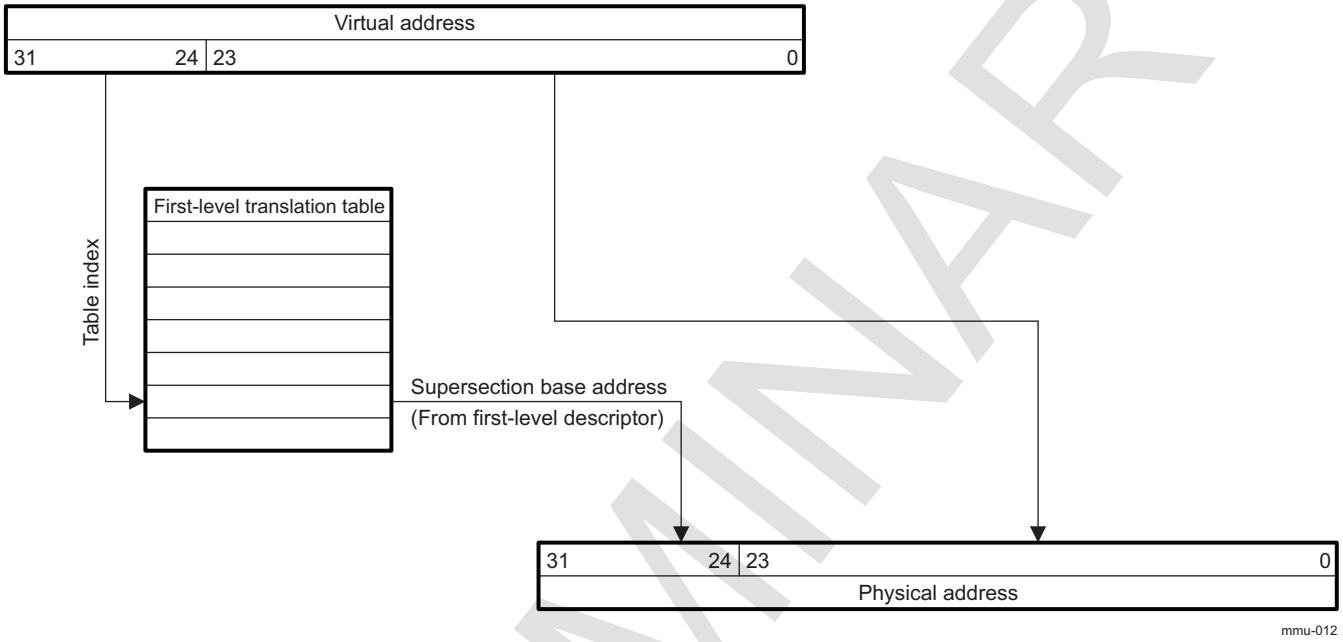
20.3.1.2.2.5 Supersection Translation Summary

The translation of a supersection is similar to the translation of a section. The difference is that for a supersection only bits 31 to 24 index into the first-level translation table. The last four bits of the table index are implicitly assumed to be zero as there are 16 identical consecutive entries for a supersection.

Figure 20-10 shows the translation mechanism for a supersection.

Figure 20-10. Supersection Translation Summary



20.3.1.2.3 Two-Level Translation

Two-level translation is used when fine-grain granularity is required, that is, when memory sections smaller than 1MB are needed. In this case, the first-level descriptor provides a pointer to the base address of a second-level translation table. This second-level table is indexed by bits 19 to 12 of the virtual address. Figure 20-11 shows this indexing mechanism.

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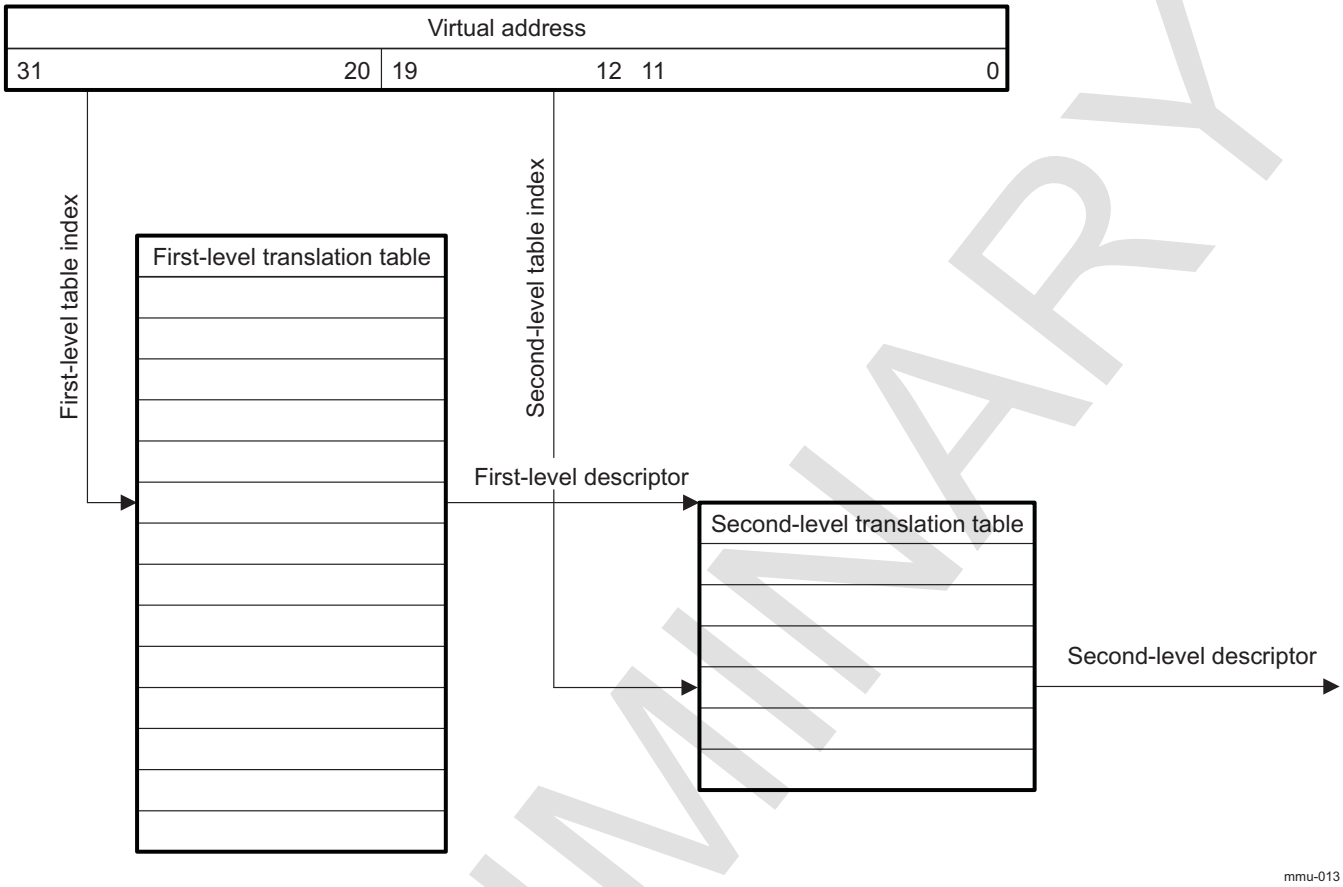
Figure 20-11. Two-Level Translation



Each second-level translation table describes the translation of 1MB of address space in pages of 64KB (large page) or 4KB (small page). It consists of 256 second-level descriptors describing 4KB each.

NOTE: In the case of a large page, the same descriptor must be repeated 16 times. If an access points to a descriptor that is not initialized, the MMU will behave in an unpredictable way.

20.3.1.2.3.1 Second-Level Descriptor Format

Similar to first-level section descriptors, second-level descriptors provide all of the necessary information for the translation of a large or small page. Table 20-5 shows the format of second-level descriptors. The translation parameters (endianness, element size, and mixed region) have the same meaning as those for sections.

Table 20-5. Second-Level Descriptor Format

Second-Level Descriptor Format										
31:16	15:12	11	10	9	8:6	5:4	3:2	1	0	
X								0	0	Fault
Large Page Base Address	X	M	X	E (1)	X	ES	X	0	1	Large Page
Small Page Base Address		M	X	E	X	ES	X	1	X	Small Page

(1) See for endianness limitations.

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M = Mixed region: 0 = Page-based endianness, 1 = Access-based endianness

E = Endianness: 0 = Little-endian, 1 = Big-endian (endianness is locked on little endian)

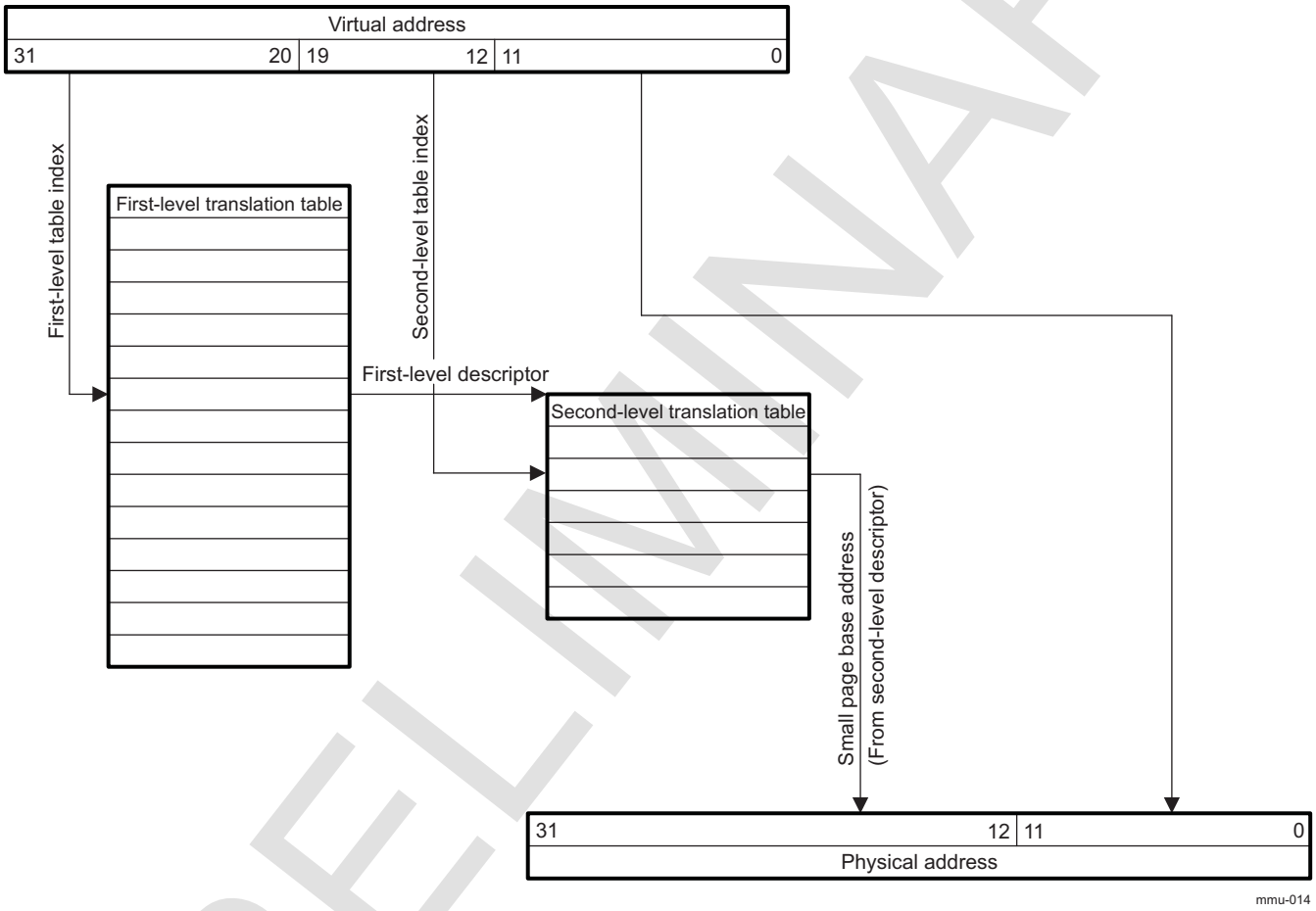
ES = Element Size: 00 = 8-bit, 01= 16-bit, 10 = 32-bit, 11 = No endianness conversion

X = Don't care

20.3.1.2.3.2 Small Page Translation Summary

Figure 20-12 summarizes the translation process for small pages.

Figure 20-12. Small Page Translation Summary



20.3.1.2.3.3 Large Page Translation Summary

The translation of a large page is similar to the translation of a small page. The difference is that, for a large page, only bits 19 to 16 index into the second-level translation table. The last four bits of the table index are implicitly assumed to be zero as there are 16 identical consecutive entries for a large page. This is shown in Figure 20-13.

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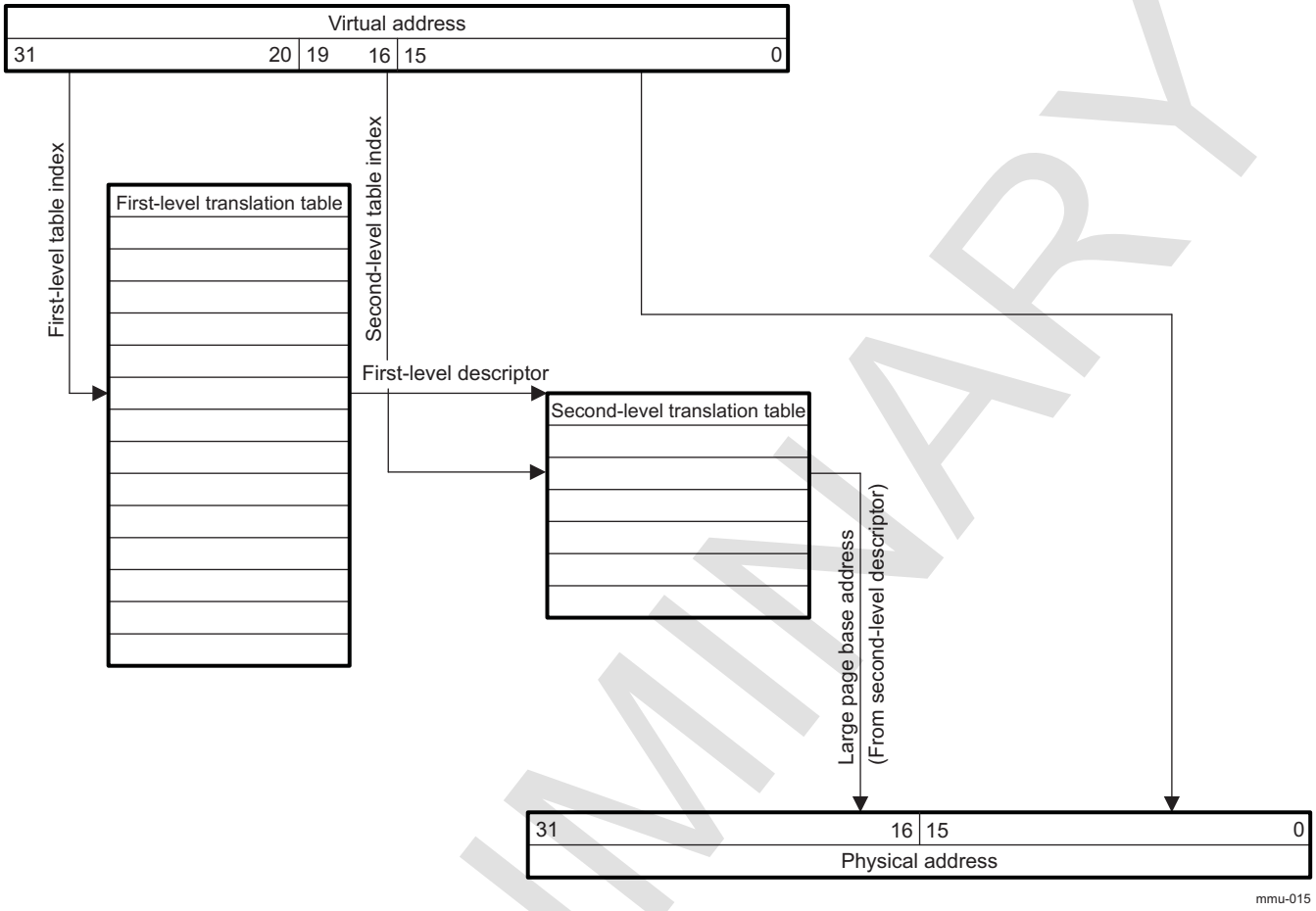
Figure 20-13. Large Page Translation Summary



20.3.1.3 Translation Lookaside Buffer

Translating virtual addresses to physical addresses is required for each memory access in systems using an MMU. To accelerate this translation process, a cache, or TLB, holds the result of recent translations.

For every translation, the MMU internal logic first checks whether the requested translation is already cached in the TLB. If the translation is cached, this translation is used; otherwise the translation is retrieved from the translation tables and the TLB is updated. If the TLB is full, one of its entries must be replaced. This entry is selected on a random basis.

The first *n* TLB entries, where *n Total Number N of TLB Entries*, can be protected (locked) against being overwritten by setting the TLB base pointer to *n*. When this mechanism is used, only unprotected entries can be overwritten. The victim pointer indicates the next TLB entry to be written. Figure 20-14 shows an example of the TLB with N TLB entries (ranging from 0 to N-1). The base pointer contains the value "3" protecting Entry 0, Entry 1, and Entry 2 and the victim pointer points to the next TLB entry to be updated.

NOTE: The last TLB entry (Entry N-1) always remains unprotected.

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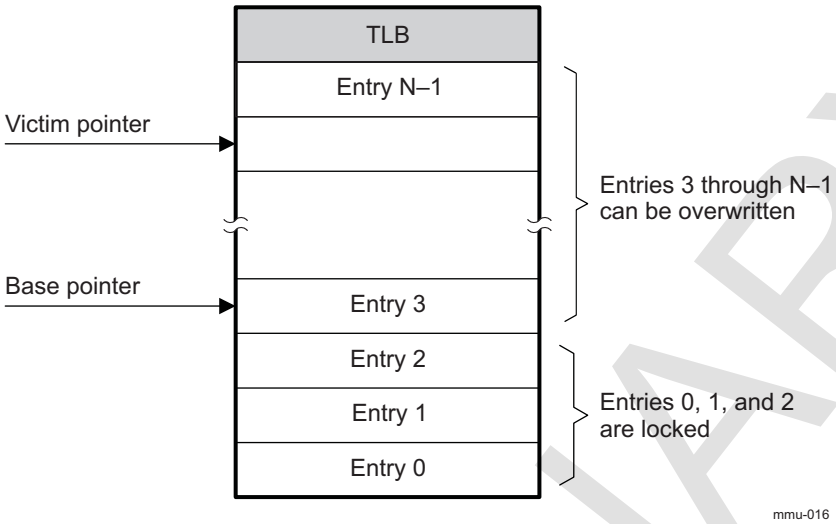
Figure 20-14. TLB Entry Lock Mechanism



The table walking logic automatically writes the TLB entries. The entries can also be manually written, which is done typically to ensure that the translation of time-critical data accesses is already present in the TLB so that they execute as fast as possible. The entries must be locked to prevent them from being overwritten.

20.3.1.3.1 TLB Entry Format

TLB entries consist of two parts:

- The CAM part contains the virtual address tag used to determine if a virtual address translation is in the TLB. The TLB acts like a fully associative cache addressed by the virtual address tag. The CAM part also contains the section/page size, as well as the preserved and the valid parameters. See the MMU_CAM register table for more details.
- The RAM part contains the address translation that belongs to the virtual address tag as well as the endianness, element size, and mixed parameters described in Section 20.3.1.2.2, *First-Level Translation Table*. See the MMU_RAM register table for more details.

The valid parameter specifies whether an entry is valid or not. The preserved parameter determines the behavior of an entry in the event of a TLB flush. If an entry is set as preserved, it is not deleted when a TLB is flushed, that is, when MMU_GFLUSH[0] GLOBALFLUSH is set to 1. Preserved entries must be deleted manually. Section 20.3.1.2.2 describes the procedure to delete TLB entries.

Figure 20-16 shows the TLB entry structure.

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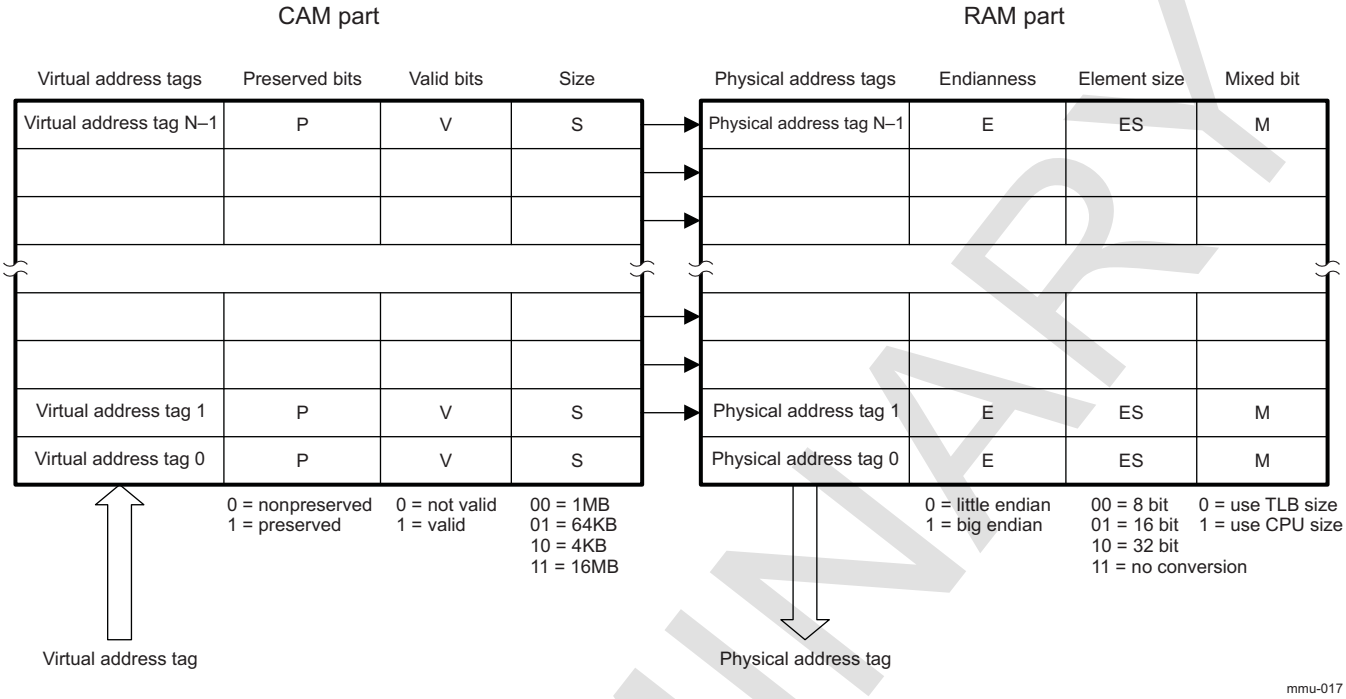
Figure 20-15. TLB Entry Structure



20.3.2 MMU Clock Configuration

There are two clock domains: The functional clock domain for the MMU, which is synchronous to the clock for the interconnect slave and master access ports; and the clock domain for the interconnect slave configuration port. As these clocks are matched, there is a single input clock with enables for each of the clock domains. If a clock domain should run at the same frequency as the input clock, that enable can be tied high.

Two clock enable signals exist, one to enable the interconnect data master and slave ports, and the other to enable the clock on the configuration L3 interconnect port. The clock signals are configured through the MMU_SYSCONFIG register. This is a system configuration register that controls the various parameters of the L3 interface.

20.3.3 MMU Software Reset

This section describes the software reset feature of the module. The MMU instances are reset together with their respective reset domains. See Table 20-2 for information about the reset domains of the different MMU instances.

To perform a software reset, write 1 in the MMU_SYSCONFIG[1] SOFTRESET bit. The MMU_SYSSTATUS[0] RESETDONE bit indicates that the software reset is complete when its value is 1. When the software reset completes, the MMU_SYSCONFIG[1] SOFTRESET bit is automatically reset. The software must ensure that the software reset completes before doing MMU operations. When an MMU instance is released from reset, its TLB is empty and the MMU is disabled.

20.3.4 MMU Power Management

As part of the device system-wide power management scheme, each MMU instance supports a communication protocol with the PRCM module that allows the PRCM module to request an MMU instance to enter a low-power state. When the MMU instance acknowledges a low-power mode request from the PRCM module, the clock to the instance is gated off at the PRCM clock generator. Because the clock is disabled at the source, the low-power mode offers lower power consumption than the internal clock gating method in the local power management.

Table 20-6 describes the power-management features available for the MMU modules.

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NOTE:

- For information about source clock gating and sleep/wake-up transitions description, see Section 3.1.1.1, *Clock Management*, in Chapter 3, *Power, Reset, and Clock Management*.
- For descriptions of EnaWakeUp, IdleMode, ClockActivity, and StandbyMode features, see Section 3.1.1.1.2, *Module Level Clock Management*, in Chapter 3, *Power, Reset, and Clock Management*.

Table 20-6. MMU Local Power Management Features

Feature	Register
Idle modes	MMU_SYSCONFIG[4:3] IDLEMODE
Clock activity	MMU_SYSCONFIG[9:8] CLOCKACTIVITY
Clock autogating	MMU_SYSCONFIG[0] AUTOIDLE

NOTE: The MMU_SYSCONFIG[9:8] CLOCKACTIVITY bits are read only.

20.3.5 MMU Interrupt Requests

Table 20-7 lists the event flags and their masks that can cause module interrupts.

Table 20-7. Events

Event Flag	Event Mask	Synchronous	Sensitivity	Map to	Description
MMU_IRQSTATUS[4] MULTIHITFAULT	MMU_IRQENABLE[4] MULTIHITFAULT	Yes	Level	M3_IRQ_0	Error in the L2 MMU due to multiple matches in the TLB
MMU_IRQSTATUS[3] TABLEWALKFAULT	MMU_IRQENABLE[3] TABLEWALKFAULT	Yes	Level	M3_IRQ_0	Error in the L2 MMU due to error response received during a Table Walk
MMU_IRQSTATUS[2] EMUMISS	MMU_IRQENABLE[2] EMUMISS				For more information about emulation and debug features, see Chapter 28, *On-Chip Debug Support*.
MMU_IRQSTATUS[1] TRANSLATIONFAULT	MMU_IRQENABLE[1] TRANSLATIONFAULT	Yes	Level	M3_IRQ_0	Error in the L2 MMU due to invalid descriptor in the translation tables (translation fault)
MMU_IRQSTATUS[0] TLBMISS	MMU_IRQENABLE[0] TLBMISS	Yes	Level	M3_IRQ_0	Error in L2 MMU due to unrecoverable TLB miss (hardware TWL disabled)

20.3.6 MMU Error Handling

Table 20-8 summarizes the intended operation for real and potential error conditions.

Table 20-8. Error Handling

Item	Condition	Action
1	Table-walk read has an error response.	Treat generally the same as a translation fault, but set the TableWalkFault interrupt status bit to aid in diagnosis
2	MMU is disabled during table-walk.	Not permitted; can result in loss of the current transaction but must not deadlock the MMU.
		Avoid this condition by first disabling the table-walk logic and then polling the TWLRunning bit to ensure that no table walk is pending
3	MMU is disabled during an address translation.	Not permitted; can result in access to an unintended location, but must not deadlock MMU.
		This condition should be avoided by ensuring that no accesses are pending.

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Table 20-8. Error Handling (continued)

Item	Condition	Action
4	TLB is accessed during an address translation or a table walk.	Reading permitted; write should be done with care to ensure that the TLB is self-consistent at all times that a translation can occur.
5	TLB is flushed during address translation or a table walk.	Permitted; the flush is processed first, followed by the TWL update.
6	MMU is disabled while an interrupt is pending.	Not permitted; all pending interrupts should be processed before disabling the MMU.

L3 Interconnect configuration port: Accesses to undecoded register addresses must not give an error response.

To protect against changes to the address translation between a READEX and the corresponding write or during a burst the following configuration operations are protected against writes during these processes:

- TLB update
- Global flush
- Flush entry
- MMU disable

The protection is implemented by stalling the configuration interconnect transaction until the write can proceed safely.

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20.4 MMU Low-level Programming Models

This section covers the low-level hardware programming sequences for configuration and usage of the module.

20.4.1 Global Initialization

20.4.1.1 Surrounding Modules Global Initialization

This section identifies the requirements of initializing the surrounding modules when the MMU module is to be used for the first time after a device reset. This initialization of surrounding modules is based on the integration and environment of the MMU. For more information, see Section Section 20.2, *MMU Module Integration* .

Table 20-9. Global Initialization of Surrounding Modules

Surrounding Modules	Comments
PRCM	Module interface and functional clocks must be enabled. For more information, see Chapter 3, *Power, Reset, and Clock Management*.
(optional) MPU INTC or DSP INTC or Cortex-M3 INTC	MPU, DSP, and Cortex-M3 interrupt controller configuration must be done to enable the interrupts from module.
Interconnect	For more information about the L3 interconnect configuration, see Section 13.2, *L3 Interconnect* .

NOTE: If the interrupt-based communication mode is used, the MPU, DSP, and Cortex-M3 interrupt controllers configurations are required.

20.4.1.2 MMU Global Initialization

20.4.1.2.1 Main Sequence—MMU Global Initialization

Figure 20-16 shows the procedure to initialize the MMU after a power-on or software reset.

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Figure 20-16. MMU Global Initialization

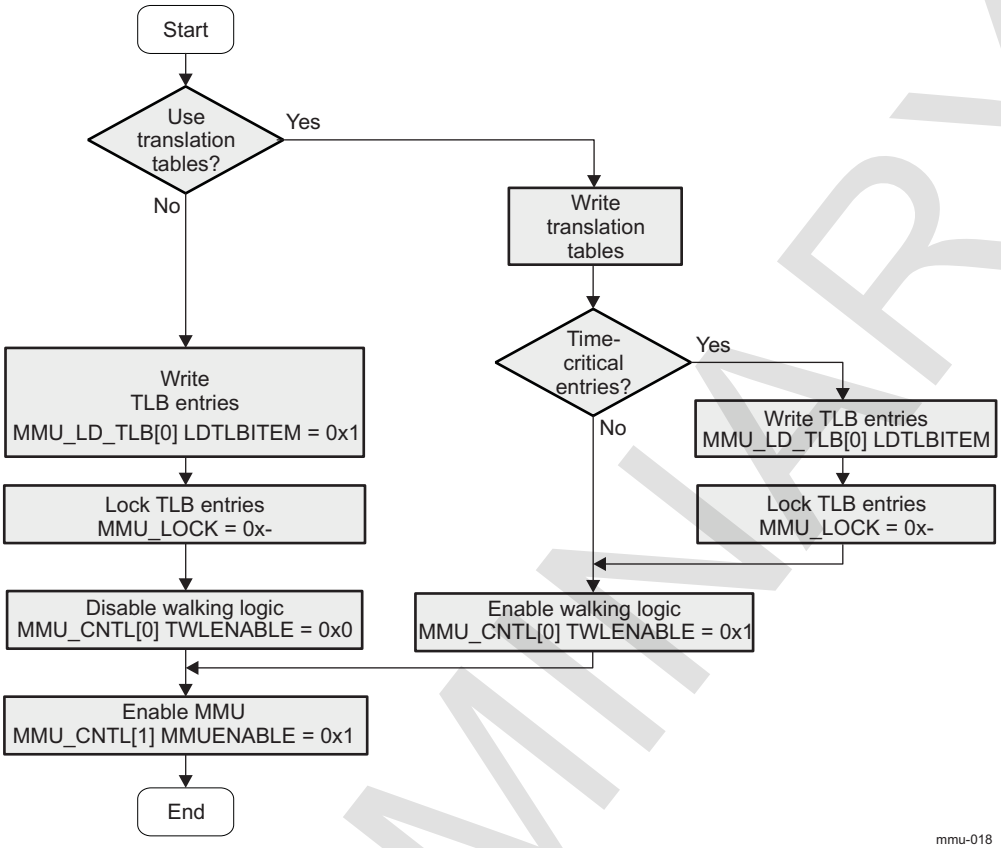

Table 20-10. Register Call Summary for Main Sequence—MMU Global Initialization

Register Name	Register Name	Register Name
MMU_LD_TLB	MMU_LOCK	MMU_CNTL

20.4.1.2.2 Subsequence—Configure a TLB entry

Table 20-11. Configure a TLB Entry

Step	Register / Bit Field / Programming Model	Value
Load the Virtual Address Tag	MMU_CAM[31:12] VATAG	0x-
Protect the TLB entry against flush	MMU_CAM[3] P	0x1
Validate the TLB entry	MMU_CAM[2] V	0x1
Define the page size	MMU_CAM[1:0] PAGESIZE	0x-

20.4.1.3 Operational Modes Configuration

20.4.1.3.1 Main Sequence—Writing TLB Entries Statically

Writing TLB entries statically avoids the need to write translation tables in memory and is commonly used for relatively small address spaces. This method ensures that the translation of time-critical data accesses execute as fast as possible with entries already present in the TLB. These entries must be locked to prevent them from being overwritten.

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Table 20-12. MMU Writing TLB Entries Statically

Step	Register/ Bit Field / Programming Model	Value
Execute software reset	MMU_SYSCONFIG[1] SOFTRESET	0x1
Wait for reset to complete	MMU_SYSSTATUS[0] RESETDONE	=0x1
Enable power saving via automatic interface clock gating	MMU_SYSCONFIG[0] AUTOIDLE	0x1
Configure TLB entries	See Table 20-11	
Load the physical Address of the page	MMU_RAM[31:12] PHYSICALADDRESS	0x-
Define the endianness of the page (little endian or big endian)	MMU_RAM[9] ENDIANNESS	0x-
Select the element size	MMU_RAM[8:7] ELEMENTSIZE	0x-
Define mixed page attribute	MMU_RAM[6] MIXED	0x-
Specify the TLB entry you want to write	MMU_LOCK[8:4] CURRENTVICTIM	0x-
Load the specified entry in the TLB	MMU_LD_TLB[0] LDTLBITEM	0x1
Enable multihit fault and TLB miss	MMU_IRQENABLE[4] MULTIHITFAULT	0x1
	MMU_IRQENABLE[0] TLBMISS	0x1
Enable memory translations	MMU_CNTL[1] MMUENABLE	0x1

20.4.1.3.2 Main Sequence—Protecting TLB Entries

The first *n* TLB entries (with *n* total number of TLB entries) can be protected from being overwritten with new translations. This is useful to ensure that certain commonly used or time-critical translations are always in the TLB and do not require retrieval using the table walking process.

Table 20-13. Protecting TLB Entries

Step	Registe/Bit Field/Programming Model	Value
Locks the TLB entries	MMU_LOCK[14:10] BASEVALUE	0x-

20.4.1.3.3 Main Sequence—Deleting TLB Entries

Two mechanisms exist to delete TLB entries. All unpreserved TLB entries, that is, TLB entries written with the preserved bit set to zero, can be deleted by invoking a TLB flush. The preserved bit should only be used on protected TLB entries, as it does not prevent replacement by the table walking logic.

Table 20-14. Deleting TLB Entries

Step	Registet / Bit Field / Programming Model	Value
Flush all nonprotected TLB entries	MMU_GFLUSH[0] GLOBALFLUSH	0x1
Flush all TLB entries specified by the CAM register	MMU_FLUSH_ENTRY[0] FLUSHENTRY	0x1

20.4.1.3.4 Main Sequence—Read TLB Entries

TLB entries can be read by the programmer to determine the TLB content at runtime.

Table 20-15. Read TLB Entries

Step	Register / Bit Field / Programming Model	Value
Set the current victim pointer	MMU_LOCK[8:4] CURRENTVICTIM	0x-
Read RAM parts of the TLB entry	MMU_READ_RAM	
Read CAM parts of the TLB entry	MMU_READ_CAM	

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20.5 MMU Register Manual

20.5.1 MMU Instance Summary

Table 20-16. MMU Instance Summary

Module Name	Base Address	Size
CORTEXM3_L2MMU	0x5508 2000	4KB
DSP_MMU	0x4A06 6000	4KB

20.5.2 MMU Registers

20.5.2.1 MMU Register Summary

Table 20-17. MMU Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	CORTEXM3_L2MMU Base Address	DSP_MMU Base Address
MMU_REVISION	R	32	0x0000 0000	0x5508 2000	0x4A06 6000
MMU_SYSCONFIG	RW	32	0x0000 0010	0x5508 2010	0x4A06 6010
MMU_SYSSTATUS	R	32	0x0000 0014	0x5508 2014	0x4A06 6014
MMU_IRQSTATUS	RW	32	0x0000 0018	0x5508 2018	0x4A06 6018
MMU_IRQENABLE	RW	32	0x0000 001C	0x5508 201C	0x4A06 601C
MMU_WALKING_ST	R	32	0x0000 0040	0x5508 2040	0x4A06 6040
MMU_CNTL	RW	32	0x0000 0044	0x5508 2044	0x4A06 6044
MMU_FAULT_AD	R	32	0x0000 0048	0x5508 2048	0x4A06 6048
MMU_TTB	RW	32	0x0000 004C	0x5508 204C	0x4A06 604C
MMU_LOCK	RW	32	0x0000 0050	0x5508 2050	0x4A06 6050
MMU_LD_TLB	RW	32	0x0000 0054	0x5508 2054	0x4A06 6054
MMU_CAM	RW	32	0x0000 0058	0x5508 2058	0x4A06 6058
MMU_RAM	RW	32	0x0000 005C	0x5508 205C	0x4A06 605C
MMU_GFLUSH	RW	32	0x0000 0060	0x5508 2060	0x4A06 6060
MMU_FLUSH_ENTRY	RW	32	0x0000 0064	0x5508 2064	0x4A06 6064
MMU_READ_CAM	R	32	0x0000 0068	0x5508 2068	0x4A06 6068
MMU_READ_RAM	R	32	0x0000 006C	0x5508 206C	0x4A06 606C
MMU_EMU_FAULT_AD	R	32	0x0000 0070	0x5508 2070	0x4A06 6070
MMU_FAULT_PC	R	32	0x0000 0080	0x5508 2080	0x4A06 6080
MMU_FAULT_STATUS	RW	32	0x0000 0084	0x5508 2084	0x4A06 6084
MMU_GP_REG	RW	32	0x0000 0088	0x5508 2088	N\A
DSPSS_MMU_GPR	RW	32	0x0000 0088	N/A	0x4A06 6088

NOTE: MMU_IRQENABLE, MMU_CNTL and MMU_TTB registers have retention capabilities. For more information about the device retention state management, see the PRCM chapter.

20.5.2.2 MMU Register Description

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Table 20-18. MMU_REVISION

Address Offset	0x0000 0000		
Physical Address	0x5508 2000	**Instance**	CORTEXM3_L2MMU
Description	This register contains the IP revision code		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP Revision	R	See (1)

(1) TI internal data

Table 20-19. Register Call Summary for Register MMU_REVISION

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- MMU Register Summary: [0]

Table 20-20. MMU_SYSCONFIG

Address Offset	0x0000 0010		
Physical Address	0x5508 2010	**Instance**	CORTEXM3_L2MMU
Description	This register controls the various parameters of the L3 interconnect interface		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						CLOCKACTIVITY		RESERVED			IDLEMODE		RESERVED	SOFTRESET	AUTOIDLE

Bits	Field Name	Description	Type	Reset
31:10	RESERVED	Write 0's for future compatibility Reads returns 0	R	0x000000
9:8	CLOCKACTIVITY	Clock activity during wake-up mode 00 Functional and Interconnect clocks can be switched off	R	0x0
7:5	RESERVED	Write 0's for future compatibility Reads returns 0	R	0x0
4:3	IDLEMODE	IdleMode 0x0: Force-idle. An idle request is acknowledged unconditionally 0x1: No-idle. An idle request is never acknowledged 0x2: Smart-idle. Acknowledgement to an idle request is given based on the internal activity of the module 0x3: reserved do not use	RW	0x0
2	RESERVED	Write 0's for future compatibility Reads returns 0	R	0
1	SOFTRESET	Software reset. This bit is automatically reset by the hardware. During reads, it always return 0 Read 0x0: always return 0 Write 0x0: no functional effect Write 0x1: The module is reset Read 0x1: never happens	RW	0

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Bits	Field Name	Description	Type	Reset
0	AUTOIDLE	Internal interconnect clock gating strategy 0x0: interconnect clock is free-running 0x1: Automatic interconnect clock gating strategy is applied, based on the interconnect interface activity	RW	0

Table 20-21. Register Call Summary for Register MMU_SYSCONFIG

MMU Functional Description • MMU Clock Configuration: [0] • MMU Software Reset: [1] [2] • MMU Power Management: [3] [4] [5] [6]
MMU Low-level Programming Models • Main Sequence—Writing TLB Entries Statically: [7] [8]
MMU Register Manual • MMU Register Summary: [9]

Table 20-22. MMU_SYSSTATUS

Address Offset	0x0000 0014		
Physical Address	0x5508 2014	**Instance**	CORTEXM3_L2MMU
Description	This register provides status information about the module, excluding the interrupt status information		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															RESETDONE

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reads returns 0	R	0x000000
0	RESETDONE	Internal reset monitoring Read 0x0: Internal module reset in on-going Read 0x1: Reset completed	R	-

Table 20-23. Register Call Summary for Register MMU_SYSSTATUS

MMU Functional Description • MMU Software Reset: [0]
MMU Low-level Programming Models • Main Sequence—Writing TLB Entries Statically: [1]
MMU Register Manual • MMU Register Summary: [2]

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Table 20-24. MMU_IRQSTATUS

Address Offset	0x0000 0018		
Physical Address	0x5508 2018	**Instance**	CORTEXM3_L2MMU
Description	This interrupt status register regroups all the status of the module internal events that can generate an interrupt.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																											MULTIHITFAULT	TABLEWALKFAULT	EMUMISS	TRANSLATIONFAULT	TLBMISS

Bits	Field Name	Description	Type	Reset
31:5	RESERVED	Write 0's for future compatibility read returns 0	R	0x0000000
4	MULTIHITFAULT	Error due to multiple matches in the TLB Read 0x0: MultiHitFault false Write 0x0: MultiHitFault status bit unchanged Write 0x1: MultiHitFault status bit is reset Read 0x1: MultiHitFault is true ("pending")	RW W1toClr	0
3	TABLEWALKFAULT	Error response received during a Table Walk Read 0x0: TableWalkFault false Write 0x0: TableWalkFault status bit unchanged Write 0x1: TableWalkFault status bit is reset Read 0x1: TableWalkFault is true ("pending")	RW W1toClr	0
2	EMUMISS	Unrecoverable TLB miss during debug (hardware TWL disabled) Read 0x0: EMUMiss false Write 0x0: EMUMiss status bit unchanged Write 0x1: EMUMiss status bit is reset Read 0x1: EMUMiss is true ("pending")	RW W1toClr	0
1	TRANSLATIONFAULT	Invalid descriptor in translation tables (translation fault) Read 0x0: TranslationFault false Write 0x0: TranslationFault status bit unchanged Write 0x1: TranslationFault status bit is reset Read 0x1: TranslationFault is true ("pending")	RW W1toClr	0
0	TLBMISS	Unrecoverable TLB miss (hardware TWL disabled) Read 0x0: TLBMiss false Write 0x0: TLBMiss status bit unchanged Write 0x1: TLBMiss status bit is reset Read 0x1: TLBMiss is true ("pending")	RW W1toClr	0

Table 20-25. Register Call Summary for Register MMU_IRQSTATUS

MMU Functional Description

- MMU Interrupt Requests: [0] [1] [2] [3] [4]

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- MMU Register Summary: [5]

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Table 20-26. MMU_IRQENABLE

Address Offset	0x0000 001C		
Physical Address	0x5508 201C	**Instance**	CORTEXM3_L2MMU
Description	The interrupt enable register allows to mask/unmask the module internal sources of interrupt, on a event-by-event basis.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																											MULTIHITFAULT	TABLEWALKFAULT	EMUMISS	TRANSLATIONFAULT	TLBMISS

Bits	Field Name	Description	Type	Reset
31:5	RESERVED	Write 0's for future compatibility Read returns 0	R	0x0000000
4	MULTIHITFAULT	Error due to multiple matches in the TLB 0x0: MultiHitFault is masked 0x1: MultiHitFault event generates an interrupt if occurs	RW	0
3	TABLEWALKFAULT	Error response received during a Table Walk 0x0: TableWalkFault is masked 0x1: TableWalkFault event generates an interrupt if occurs	RW	0
2	EMUMISS	Unrecoverable TLB miss during debug (hardware TWL disabled) 0x0: EMUMiss interrupt is masked 0x1: EMUMiss event generates an interrupt when it occurs	RW	0
1	TRANSLATIONFAULT	Invalid descriptor in translation tables (translation fault) 0x0: TranslationFault is masked 0x1: TranslationFault event generates an interrupt if occurs	RW	0
0	TLBMISS	Unrecoverable TLB miss (hardware TWL disabled) 0x0: TLBMiss interrupt is masked 0x1: TLBMiss event generates an interrupt when if occurs	RW	0

Table 20-27. Register Call Summary for Register MMU_IRQENABLE

MMU Functional Description
- MMU Interrupt Requests: [0] [1] [2] [3] [4]

MMU Low-level Programming Models
- Main Sequence—Writing TLB Entries Statically: [5] [6]

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- MMU Register Summary: [7] [8]

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Table 20-28. MMU_WALKING_ST

Address Offset	0x0000 0040		
Physical Address	0x5508 2040	**Instance**	CORTEXM3_L2MMU
Description	This register provides status information about the table walking logic		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															TWLRUNNING

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reads return 0	R	0x0000 0000
0	TWLRUNNING	Table Walking Logic is running Read 0x0: TWL Completed Read 0x1: TWL Running	R	0

Table 20-29. Register Call Summary for Register MMU_WALKING_ST

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- MMU Register Summary: [0]

Table 20-30. MMU_CNTL

Address Offset	0x0000 0044		
Physical Address	0x5508 2044	**Instance**	CORTEXM3_L2MMU
Description	This register programs the MMU features		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												EMUTLBUPDATE	TWLENABLE	MMUENABLE	RESERVED

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Write 0's for future compatibility Reads return 0	R	0x0000000
3	EMUTLBUPDATE	Enable TLB update on emulator table walk 0x0: Emulator TLB update disabled 0x1: Emulator TLB update enabled	RW	0
2	TWLENABLE	Table Walking Logic enable 0x0: TWL disabled 0x1: TWL enabled	RW	0
1	MMUENABLE	MMU enable 0x0: MMU disabled 0x1: MMU enabled	RW	0
0	RESERVED	Write 0's for future compatibility Reads return 0	R	0

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Table 20-31. Register Call Summary for Register MMU_CNTL

MMU Low-level Programming Models • Main Sequence—MMU Global Initialization: [0] • Main Sequence—Writing TLB Entries Statically: [1]
MMU Register Manual • MMU Register Summary: [2] [3]

Table 20-32. MMU_FAULT_AD

Address Offset	0x0000 0048		
Physical Address	0x5508 2048	**Instance**	CORTEXM3_L2MMU
Description	This register contains the virtual address that generated the interrupt		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FAULTADDRESS																															

Bits	Field Name	Description	Type	Reset
31:0	FAULTADDRESS	Virtual address of the access that generated a fault	R	0x0000 0000

Table 20-33. Register Call Summary for Register MMU_FAULT_AD

MMU Register Manual • MMU Register Summary: [0]

Table 20-34. MMU_TTB

Address Offset	0x0000 004C		
Physical Address	0x5508 204C	**Instance**	CORTEXM3_L2MMU
Description	This register contains the Translation Table Base address		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TTBADDRESS																								RESERVED							

Bits	Field Name	Description	Type	Reset
31:7	TTBADDRESS	Translation Table Base Address	RW	0x0000000
6:0	RESERVED	Write 0's for future compatibility Reads retiurn 0	R	0x00

Table 20-35. Register Call Summary for Register MMU_TTB

MMU Register Manual • MMU Register Summary: [0] [1]

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Table 20-36. MMU_LOCK

Address Offset	0x0000 0050		
Physical Address	0x5508 2050	**Instance**	CORTEXM3_L2MMU
Description	This register locks some of the TLB entries		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																BASEVALUE						RESERVED		CURRENTVICTIM						RESERVED	

Bits	Field Name	Description	Type	Reset
31:15	RESERVED	Write 0's for future compatibility Reads return 0	R	0x00000
14:10	BASEVALUE	Locked entries base value	RW	0x00
9	RESERVED	Write 0's for future compatibility Read returns 0	R	0
8:4	CURRENTVICTIM	Current entry to be updated either by the TWL or by the software Write value : TLB entry to be updated by software, Read value : TLB entry that will be updated by table walk logic	RW	0x00
3:0	RESERVED	Write 0's for future compatibility Reads return 0	R	0x0

Table 20-37. Register Call Summary for Register MMU_LOCK

MMU Low-level Programming Models

- Main Sequence—MMU Global Initialization: [0]
- Main Sequence—Writing TLB Entries Statically: [1]
- Main Sequence—Protecting TLB Entries: [2]
- Main Sequence—Read TLB Entries: [3]

MMU Register Manual

- MMU Register Summary: [4]

Table 20-38. MMU_LD_TLB

Address Offset	0x0000 0054		
Physical Address	0x5508 2054	**Instance**	CORTEXM3_L2MMU
Description	This register loads a TLB entry (CAM+RAM)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															LDTLBITEM

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Write 0's for future compatibility Reads return 0	RW	0x0000 0000
0	LDTLBITEM	Write (load) data in the TLB	RW	0
		Read 0x0: always return 0		
		Write 0x0: no functional effect		
		Write 0x1: load TLB data		
		Read 0x1: never happens		

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Table 20-39. Register Call Summary for Register MMU_LD_TLB

MMU Low-level Programming Models
- Main Sequence—MMU Global Initialization: [0]
- Main Sequence—Writing TLB Entries Statically: [1]

MMU Register Manual
- MMU Register Summary: [2]

Table 20-40. MMU_CAM

Address Offset	0x0000 0058		
Physical Address	0x5508 2058	**Instance**	CORTEXM3_L2MMU
Description	This register holds a CAM entry		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VATAG																RESERVED								P	V	PAGESIZE					

Bits	Field Name	Description	Type	Reset
31:12	VATAG	Virtual address tag	RW	0x00000
11:4	RESERVED	Write 0's for future compatibility Reads return 0	R	0x00
3	P	Preserved bit 0x0: TLB entry may be flushed 0x1: TLB entry is protected against flush	RW	0
2	V	Valid bit 0x0: TLB entry is invalid 0x1: TLB entry is valid	RW	0
1:0	PAGESIZE	Page size 0x0: Section (1MB) 0x1: Large page (64KB) 0x2: Small page (4KB) 0x3: Supersection (16MB)	RW	0x0

Table 20-41. Register Call Summary for Register MMU_CAM

MMU Functional Description
- TLB Entry Format: [0]

MMU Low-level Programming Models
- Subsequence—Configure a TLB entry: [1] [2] [3] [4]

MMU Register Manual
- MMU Register Summary: [5]
- MMU Register Description: [6]

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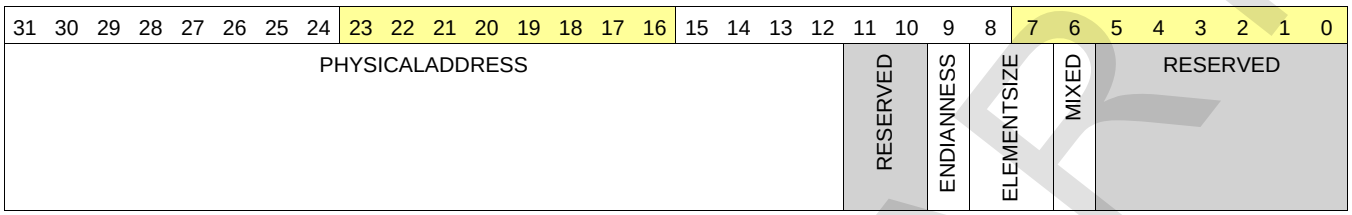
Table 20-42. MMU_RAM

Address Offset	0x0000 005C		
Physical Address	0x5508 205C	**Instance**	CORTEXM3_L2MMU
Description	This register holds a RAM entry		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:12	PHYSICALADDRESS	Physical address of the page	RW	0x00000
11:10	RESERVED	Write 0's for future compatibility Reads return 0	R	0x0
9	ENDIANNESS	Endianness of the page 0x0: Little Endian 0x1: Big endian	RW	0
8:7	ELEMENTSIZE	Element size of the page (8, 16, 32, no translation) 0x0: 8-bits 0x1: 16-bits 0x2: 32-bits 0x3: No translation	RW	0x0
6	MIXED	Mixed page attribute (use CPU element size) 0x0: Use TLB element size 0x1: Use CPU element size	RW	0
5:0	RESERVED	Write 0's for future compatibility Reads return 0	R	0x00

Table 20-43. Register Call Summary for Register MMU_RAM

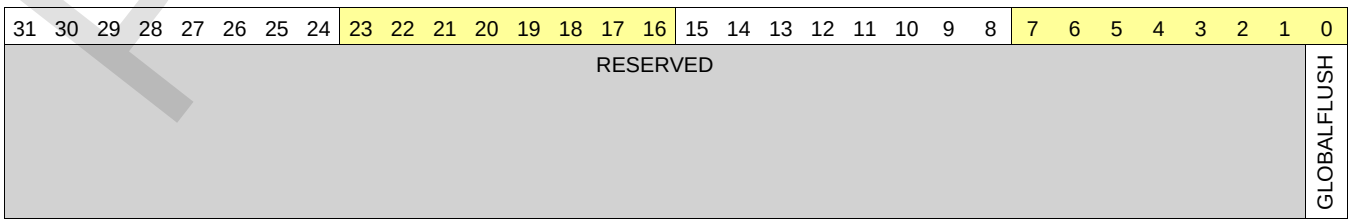
MMU Functional Description
- TLB Entry Format: [0]

MMU Low-level Programming Models
- Main Sequence—Writing TLB Entries Statically: [1] [2] [3] [4]

MMU Register Manual
- MMU Register Summary: [5]

Table 20-44. MMU_GFLUSH

Address Offset	0x0000 0060		
Physical Address	0x5508 2060	**Instance**	CORTEXM3_L2MMU
Description	This register flushes all the non-protected TLB entries		
Type	RW		



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Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Write 0's for future compatibility Reads return 0	RW	0x0000 0000
0	GLOBALFLUSH	Flush all the non-protected TLB entries when set Read 0x0: always return 0 Write 0x0: no functional effect Write 0x1: flush all the non-protected TLB entries Read 0x1: never happens	RW	0

Table 20-45. Register Call Summary for Register MMU_GFLUSH

MMU Functional Description • TLB Entry Format: [0]
MMU Low-level Programming Models • Main Sequence—Deleting TLB Entries: [1]
MMU Register Manual • MMU Register Summary: [2]

Table 20-46. MMU_FLUSH_ENTRY

Address Offset	0x0000 0064		
Physical Address	0x5508 2064	**Instance**	CORTEXM3_L2MMU
Description	This register flushes the entry pointed to by the CAM virtual address		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															FLUSHENTRY

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Write 0's for future compatibility Reads return 0	RW	0x0000 0000
0	FLUSHENTRY	Flush the TLB entry pointed by the virtual address (VATag) in MMU_CAM register, even if this entry is set protected Read 0x0: always return 0 Write 0x0: no functional effect Write 0x1: flush all the TLB entries specified by the CAM register Read 0x1: never happens	RW	0

Table 20-47. Register Call Summary for Register MMU_FLUSH_ENTRY

MMU Low-level Programming Models • Main Sequence—Deleting TLB Entries: [0]
MMU Register Manual • MMU Register Summary: [1]

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Table 20-48. MMU_READ_CAM

Address Offset	0x0000 0068		
Physical Address	0x5508 2068	**Instance**	CORTEXM3_L2MMU
Description	This register reads CAM data from a CAM entry		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VATAG																RESERVED								P	V	PAGESIZE					

Bits	Field Name	Description	Type	Reset
31:12	VATAG	Virtual address tag	R	0x00000
11:4	RESERVED	Reads return 0	R	0x00
3	P	Preserved bit Read 0x0: TLB entry may be flushed Read 0x1: TLB entry is protected against flush	R	0
2	V	Valid bit Read 0x0: TLB entry is invalid Read 0x1: TLB entry is valid	R	0
1:0	PAGESIZE	Page size Read 0x0: Section (1MB) Read 0x1: Large page (64KB) Read 0x2: Small page (4KB) Read 0x3: Supersection (16MB)	R	0x0

Table 20-49. Register Call Summary for Register MMU_READ_CAM

MMU Low-level Programming Models
- Main Sequence—Read TLB Entries: [0]

MMU Register Manual
- MMU Register Summary: [1]

Table 20-50. MMU_READ_RAM

Address Offset	0x0000 006C		
Physical Address	0x5508 206C	**Instance**	CORTEXM3_L2MMU
Description	This register reads RAM data from a RAM entry		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHYSICALADDRESS																				RESERVED		ENDIANNESS	ELEMENTSIZE		MIXED	RESERVED					

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Bits	Field Name	Description	Type	Reset
31:12	PHYSICALADDRESS	Physical address of the page	R	0x00000
11:10	RESERVED	Reads return 0	R	0x0
9	ENDIANNESS	Endianness of the page Read 0x0: Little Endian Read 0x1: Big endian	R	0
8:7	ELEMENTSIZE	Element size of the page (8, 16, 32, no translation) Read 0x0: 8-bits Read 0x1: 16-bits Read 0x2: 32-bits Read 0x3: No translation	R	0x0
6	MIXED	Mixed page attribute (use CPU element size) Read 0x0: Use TLB element size Read 0x1: Use CPU element size	R	0
5:0	RESERVED	Reads return 0	R	0x00

Table 20-51. Register Call Summary for Register MMU_READ_RAM

MMU Low-level Programming Models
- Main Sequence—Read TLB Entries: [0]

MMU Register Manual
- MMU Register Summary: [1]

Table 20-52. MMU_EMU_FAULT_AD

Address Offset	0x0000 0070		
Physical Address	0x5508 2070	**Instance**	CORTEXM3_L2MMU
Description	This register contains the last virtual address of a fault caused by the debugger		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EMUFAULTADDRESS																															

Bits	Field Name	Description	Type	Reset
31:0	EMUFAULTADDRESS	Virtual address of the last emulator access that generated a fault	R	0x0000 0000

Table 20-53. Register Call Summary for Register MMU_EMU_FAULT_AD

MMU Register Manual
- MMU Register Summary: [0]
- MMU Register Description: [1]

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Table 20-54. MMU_FAULT_PC

Address Offset	0x0000 0080	**Instance**	CORTEXM3_L2MMU DSP MMU
Physical Address	0x5508 2080		
Description	Capture first fault PC value, controlled by MMU_FAULT_STATUS[0] FAULTINDICATION. Notes: The address value is captured at MMU_EMU_FAULT_AD[31:0] EMUFAULTADDRESS. Data-Read-access : corresponding PC. Data-write-access : not perfect accuracy due to Posted-write. All this description is valid only for the DSP MMU. The Cortex-M3 L2 MMU always reads zero from this register.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PC																															

Bits	Field Name	Description	Type	Reset
31:0	PC	CPU program counter value where cause MMU fault	R	0x0000 0000

Table 20-55. Register Call Summary for Register MMU_FAULT_PC

MMU Register Manual

- MMU Register Summary: [0]

Table 20-56. MMU_FAULT_STATUS

Address Offset	0x0000 0084	**Instance**	CORTEXM3_L2MMU DSP MMU
Physical Address	0x5508 2084		
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								MMU_FAULT_TRANS_ID				RD_WR	MMU_FAULT_TYPE		FAULTINDICATION

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Bits	Field Name	Description	Type	Reset
31:8	RESERVED		R	0x000000
7:4	MMU_FAULT_TRANS_ID	Master ID who cause a fault Read 0x0: posted writes out of shared cache for Cortex-M3 MMU / eDMA read port 1 for DSP MMU Read 0x1: Cortex-M3 video and display control processor I/D bus access for Cortex-M3 MMU / eDMA read port 2 for DSP MMU Read 0x2: Cortex-M3 video and display control processor S bus access for Cortex-M3 MMU / eDMA write port 1 for DSP MMU Read 0x3: Cortex-M3 SIMCOP control processor I/D bus access for Cortex-M3 MMU / eDMA write port 2 for DSP MMU Read 0x4: Cortex-M3 SIMCOP control processor S bus access for Cortex-M3 MMU / shared cache Evictions/stores/Non-cacheable for DSP MMU Read 0x5: reserved for Cortex-M3 MMU / shared cache request for Program/Data for DSP MMU Read 0x6: reserved for Cortex-M3 MMU / shared cache request for DMA for DSP MMU Read 0x7: reserved (for both Cortex-M3 MMU and DSP MMU) Read 0x8: MMU hardware table walk (for both Cortex-M3 MMU and DSP MMU) Read 0x9 to 0xF: reserved (for both Cortex-M3 MMU and DSP MMU)	R	0x0
3	RD_WR	indicates read or write	R	0
2:1	MMU_FAULT_TYPE	MReq Type[1:0] Read 0x2: reserved for Cortex-M3 MMU / DMA address for DSP MMU Read 0x1: Fetch address Read 0x0: Data Load/Store	R	0x0
0	FAULTINDICATION	indicates a MMU fault	RW W1toClr	0

Table 20-57. Register Call Summary for Register MMU_FAULT_STATUS

MMU Register Manual

- MMU Register Summary: [0]
- MMU Register Description: [1]

Table 20-58. MMU_GP_REG

Address Offset	0x0000 0088	**Instance**	CORTEXM3_L2MMU
Physical Address	0x5508 2088		
Description	Bus-error back response enable register. For more information about the register usage, see section L2 MMU, part of the Dual Cortex-M3 MPU chapter.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															BUS_ERR_BACK_EN

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0
0	BUS_ERR_BACK_EN	Bus-error back response enable bit 0x0: Default behaviour for MMU page Faults 0x1: All MMU faults return bus-error back	RW	0x0

Table 20-59. Register Call Summary for Register MMU_GP_REG

MMU Register Manual
- MMU Register Summary: [0]

Table 20-60. DSPSS_MMU_GPR

Address Offset	0x0000 0088	**Instance**	DSP_MMU
Physical Address			
Description	This register controls the DSP MMU hardware debug output multiplexer. It also controls force-idle request generation. For more information about the use of this register, see Chapter 18, *Control Module*.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																FORCE_IDLE_REQ	RESERVED											HWDEBUG_MUX			

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x0000
15	FORCE_IDLE_REQ	Force-idle request to see existence of pending bus request. This bit must be used only for debug purposes, not in functional mode.	RW	0x0
14:4	RESERVED	Reserved	R	0x0
3:0	HWDEBUG_MUX	Control HWDEBUG output MUX	RW	0x0

Table 20-61. Register Call Summary for Register DSPSS_MMU_GPR

MMU Register Manual
- MMU Register Summary: [0]

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Spinlock

This chapter describes the Spinlock module of the device.

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21.1 Spinlock Overview **4202**
21.2 Spinlock Integration **4203**
21.3 Spinlock Functional Description **4204**
21.4 Spinlock Programming Guide **4207**
21.5 Spinlock Register Manual **4210**

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21.1 Spinlock Overview

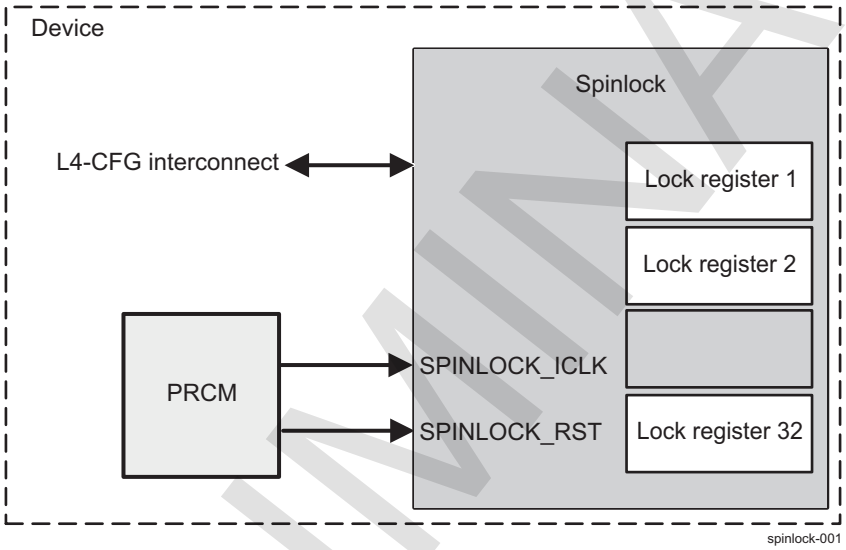
The Spinlock module provides hardware assistance for synchronizing the processes running on multiple processors in the device:

- Cortex-A9 microprocessor unit (MPU) subsystem
- Digital signal processor (DSP) subsystem
- Cortex-M3 MPU subsystem

The Spinlock module implements 32 spinlocks (or hardware semaphores), which provide an efficient way to perform a lock operation of a device resource using a single read-access, avoiding the need of a read-modify-write bus transfer that the programmable cores are not capable of.

Figure 21-1 shows the Spinlock module.

Figure 21-1. Spinlock Module



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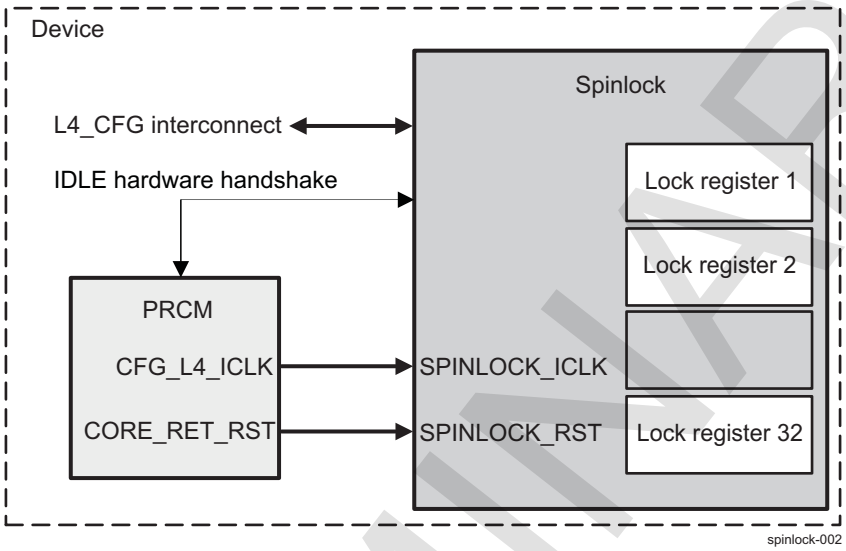
21.2 Spinlock Integration

This section describes module integration in the device, including information about clocks, resets, and hardware requests.

Figure 21-2 shows the Spinlock integration.

Figure 21-2. Spinlock Integration



NOTE: For more information about the IDLE hardware handshake and the wake-up request, see Section 3.1.1.1.2, *Module Level Clock Management*, Chapter 3, *Power, Reset, and Clock Management*.

Table 21-1 and Table 21-2 summarize the integration of the module in the device.

Table 21-1. Integration Attributes

Module Instance	Attributes	
	Power Domain	Interconnect
SPINLOCK	PD_CORE	L4_CFG

Table 21-2. Clocks and Resets

Clocks				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
SPINLOCK	SPINLOCK_ICLK	CFG_L4_ICLK	PRCM	Spinlock interface clock. This clock is used for all interface and functional operations.
Resets				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
SPINLOCK	SPINLOCK_RST	CORE_RET_RST	PRCM	Spinlock hardware reset. This reset is asynchronously applied to the Spinlock internal registers.

The Spinlock module does not support any interrupt and DMA requests.

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21.3 Spinlock Functional Description

21.3.1 Spinlock Software Reset

The Spinlock module can be reset by software through the SPINLOCK_SYSCONFIG[1] SOFTRESET bit. Setting this bit to 1 enables an active software reset that is functionally equivalent to a hardware reset. The SPINLOCK_SYSTATUS[0] RESETDONE bit can be polled to check the reset status (reading 1 indicates that reset sequence is done; reading 0 indicates that reset sequence is in progress). The software must ensure that the software reset completes before doing Spinlock operations.

21.3.2 Spinlock Power Management

Table 21-3 describes power-management features available to the Spinlock module.

NOTE:

- For information about source clock gating and sleep/wake-up transitions description, see Section 3.1.1.1.4, *Clock Domain Level Clock Management*, Chapter 3, *Power, Reset, and Clock Management*.
- For descriptions of EnaWakeUp, IdleMode, ClockActivity, and StandbyMode features, see Section 3.1.1.1.2, *Module Level Clock Management*, Chapter 3, *Power, Reset, and Clock Management*.

Table 21-3. Local Power Management Features

Feature	Registers	Description
Clock auto gating	SPINLOCK_SYSCONFIG[0] AUTOGATING bit	This bit indicates that the module uses an automatic internal interface clock gating strategy, based on interface activity.
Slave idle modes	SPINLOCK_SYSCONFIG[4:3] SIDLEMODE bit field	This bit field indicates that the module uses smart-idle mode.
Clock activity	SPINLOCK_SYSCONFIG[8] CLOCKACTIVITY bit	This bit indicates that the interface clock is not required by the module during idle mode and may be switched off.
Global wake-up enable	SPINLOCK_SYSCONFIG[2] ENAWAKEUP bit	This bit indicates that the wake-up generation feature (at module level) is disabled.

NOTE: All the local power management features are non-configurable (that is, their respective bits or bit fields are read-only).

CAUTION

The PRCM module has no hardware means of reading CLOCKACTIVITY settings. Thus, software must ensure consistent programming between the CLOCKACTIVITY bit and Spinlock clock PRCM control bits.

The Spinlock module is normally idle, except when processing a request from its slave interface port. The smart-idle mode acknowledges idle requests from the PRCM only when the module is prepared to go idle. The Spinlock module is always ready to go idle if it does not have any request that it is processing.

The Spinlock module uses retention flops to retain state including the Taken state of each lock register. This means that the module can be placed in retention at any time when it is not processing a request and it is known that the system will not need to access the module.

Software must ensure to only power off the Spinlock module when no locks would be lost. In general, the steps to powering down the Spinlock module are:

- Check that all masters which might use the Spinlock module are either:

  (a) Already powered off, or

  (b) Notified that Spinlock is not available and the notification is acknowledged.

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- If desired, check that no locks are currently held in the Spinlock module. The status of each bank of 32 locks can be read from the SPINLOCK_SYSTATUS register. If any locks are held, they are orphaned because they are not held by any master that is still active. Alternatively, you may decide to wait a timeout period to allow any active master to clean up its locks before powering down.
- The Spinlock module can now be powered off by writing the appropriate status to the PRCM.

In the case of powering off the whole system, these steps are unnecessary.

21.3.3 About Spinlocks

Spinlocks are present to solve the need for synchronization and mutual exclusion between heterogeneous processors and those not operating under a single, shared operating system. There is no alternative mechanism to accomplish these operations between processors in separate subsystems.

Spinlocks are not the best way to synchronize between tasks or threads on one CPU. Instead, spinlocks are for use in synchronization between different subsystems in the device that don't have any other means of hardware-based synchronization.

Spinlocks do not solve all system synchronization issues. They have limited applicability and should be used with care to implement higher level synchronization protocols.

A spinlock is appropriate for mutual exclusion for access to a shared data structure. It should be used only when:

1. The time to hold the lock is predictable and small (for example, a maximum hold time of less than 200 CPU cycles may be acceptable).
2. The locking task cannot be preempted, suspended, or interrupted while holding the lock (this would make the hold time large and unpredictable).
3. The lock is lightly contended, that is the chance of any other process (or processor) trying to acquire the lock while it is held is small.

If these conditions are met, then the locking code can retry a failed attempt to acquire the lock until success.

If the conditions are not met, then a spinlock is not a good candidate. One alternative is to use a spinlock for critical section control (engineered to meet the conditions) to implement a higher level semaphore that can support preemption, notification, timeout or other higher level properties.

21.3.4 Spinlock Functional Operation

The Spinlock module supports 32 spinlocks. It accepts only a single command at a time and processes the command fully before accepting the next command. A lock is requested by reading the SPINLOCK_LOCK_REG_i[0] TAKEN bit. There are two states: Taken (SPINLOCK_LOCK_REG_i[0] TAKEN = 1) or Not Taken (SPINLOCK_LOCK_REG_i[0] TAKEN = 0).

When the status of lock *i* (where i = 0 to 31) is Not Taken (free), a read from the SPINLOCK_LOCK_REG_i register returns 0 and sets the lock to Taken (locked). When the status of lock *i* is Taken, a read returns 1 and does not change the state of the lock.

A write to the SPINLOCK_LOCK_REG_i register does not change the state of lock, unless when writing 0 when the lock is in Taken state. By doing this, the requester frees the lock.

CAUTION

Only 32-bit reads and writes are supported.

Figure 21-3 shows the SPINLOCK_LOCK_REG_i register state diagram.

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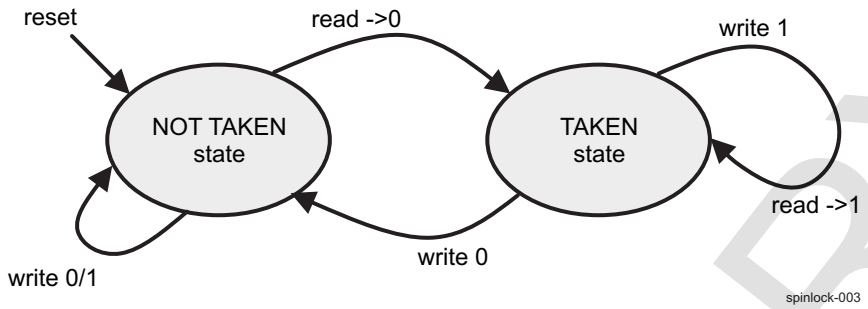
Figure 21-3. Lock Register State Diagram



NOTE:

- There is no support to ensure that a lock register is locked and unlocked by the same process. This must be ensured in software.
- There is no support to check that the same initiator that acquired the lock is the one that is freeing the lock.

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21.4 Spinlock Programming Guide

21.4.1 Spinlock Low-level Programming Models

This section covers the low-level hardware programming sequences for configuration and usage of the module.

21.4.1.1 Surrounding Modules Global Initialization

This procedure initializes the surrounding modules when the Spinlock module is used for the first time after a device reset.

Table 21-4. Global Initialization of Surrounding Modules

Surrounding Modules	Comments
PRCM	Spinlock interface clock must be enabled. For more information, see Section 3.6.14 , *CD_L4_CFG Clock Domain*, Chapter 3, *Power, Reset, and Clock Management*.
Interconnect	For more information about the L4-CFG interconnect configuration, see Section 13.3, *L4 Interconnects*.

21.4.1.2 Basic Spinlock Operations

The main spinlock operations are:

- Clear all the Taken spinlocks (only after a system bug recovery)
- Take a spinlock
- Release spinlock

21.4.1.2.1 Spinlocks Clearing After a System Bug Recovery

Module initialization (after reset) is not needed, except after system bug recovery. The following table presents the Spinlock initialization after a system bug recovery. Software should store 0 into each of the SPINLOCK_LOCK_REG_i registers at system startup to insure that all locks are initialized to Not Taken.

Table 21-5. Spinlock System Bug Recovery

Step	Register	Value
IF: SPINLOCK_SYSTATUS[0] IU0 = = 1?	SPINLOCK_SYSTATUS[0] IU0	
Free the 32 locks	SPINLOCK_LOCK_REG_i[0] TAKEN (i=0 to 31)	0x0
END		

21.4.1.2.2 Take and Release Spinlock

This procedure configures the take and release (free) operations for the Spinlock module. A spinlock should only be held with interrupts disabled. So, before attempting to obtain the spinlock, software should disable interrupts. Then it should read the SPINLOCK_LOCK_REG_i[0] TAKEN bit to attempt to obtain the lock. If it succeeds, it should proceed directly through the critical section then unlock and re-enable interrupts. If the acquisition attempt fails, the acquisition should be reattempted. To prevent unknown interrupt disabled time, interrupts should be re-enabled and then disabled before reattempting to acquire the lock. Figure 21-4 shows the described above procedure.

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Figure 21-4. Take and Release Spinlock

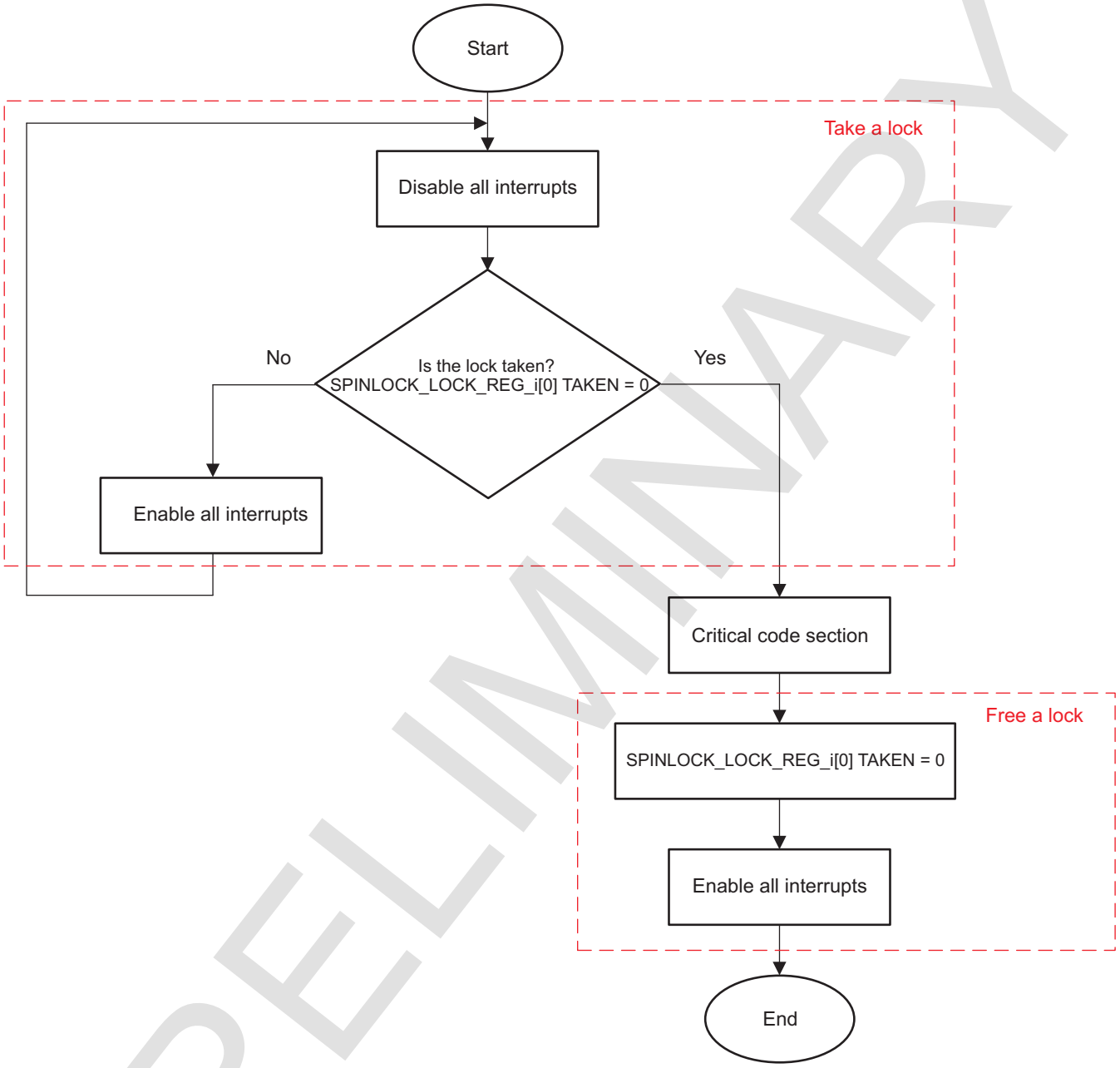

Table 21-6. Register Call Summary

Register Name
SPINLOCK_LOCK_REG_i[0] TAKEN

Table 21-7. Subprocess Call Summary

Subprocess Name	Cross Reference
Disable Interrupts	For information about disabling interrupts in Cortex-A9 MPU INTC, see the *ARMCortex-A9 MPCore Technical Reference Manual* . For information about disabling interrupts in Cortex-M3 MPU INTC, see the *ARMCortex-M3 Technical Reference Manual* . For information about disabling interrupts in DSP INTC, see Chapter 5, *DSP Subsystem*

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Table 21-7. Subprocess Call Summary (continued)

Subprocess Name	Cross Reference
Enable Interrupts	For information about enabling interrupts in Cortex-A9 MPU INTC, see the *ARM Cortex-A9 MPCore Technical Reference Manual* . For information about enabling interrupts in Cortex-M3 MPU INTC, see the *ARMCortex-M3 Technical Reference Manual* . For information about enabling interrupts in DSP INTC, see Chapter 5, *DSP Subsystem*

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21.5 Spinlock Register Manual

21.5.1 Spinlock Instance Summary

Table 21-8. Spinlock Instance Summary

Module Name	Base Address	Size
Spinlock	0x4A0F 6000	4K bytes

21.5.2 Spinlock Registers

21.5.2.1 Spinlock Register Summary

Table 21-9. Spinlock Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	Spinlock L4-CFG Base Address
SPINLOCK_REVISION	R	32	0x0000 0000	0x4A0F 6000
SPINLOCK_SYSCONFIG	RW	32	0x0000 0010	0x4A0F 6010
SPINLOCK_SYSTATUS	R	32	0x0000 0014	0x4A0F 6014
SPINLOCK_LOCK_REG_i [(1)]	RW	32	0x0000 0800 + (0x4 * i)	0x4A0F 6800 + (0x4 * i)

(1) i = 0 to 31

21.5.2.2 Spinlock Register Description

Table 21-10. SPINLOCK_REVISION

Address Offset	0x0000 0000		
Physical Address	0x4A0F 6000	**Instance**	Spinlock
Description	This register contains the IP revision code		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP revision	R	TI internal data

Table 21-11. Register Call Summary for Register SPINLOCK_REVISION

Spinlock Register Manual

- Spinlock Register Summary: [0]

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Table 21-12. SPINLOCK_SYSCONFIG

Address Offset	0x0000 0010		
Physical Address	0x4A0F 6010	**Instance**	Spinlock
Description	This register controls the various parameters of the L4-CFG interface. Note that most fields are read-only.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							CLOCKACTIVITY	RESERVED			SIDLEMODE		ENWAKEUP	SOFTRESET	AUTOGATING

Bits	Field Name	Description	Type	Reset
31:9	RESERVED	Reserved. Reads return 0.	R	0x000000
8	CLOCKACTIVITY	Indicates whether the module requires the interface clock when in IDLE mode. Read 0x0: Interface clock is not required by the module during IDLE mode and may be switched off. Read 0x1: Interface clock is required by the module, even during idle mode.	R	0
7:5	RESERVED	Reserved. Reads return 0.	R	0x0
4:3	SIDLEMODE	Slave interface power management (IDLE request/acknowledgement control). Read 0x0: Force-idle. IDLE request is acknowledged unconditionally and immediately. Read 0x1: No-idle. IDLE request is never acknowledged. Read 0x2: Smart-idle. IDLE request acknowledgement is based on the internal module activity. Read 0x3: Reserved. Do not use.	R	0x2
2	ENWAKEUP	Asynchronous wakeup gereration. Read 0x0: Wakeup generation is disabled. Read 0x1: Wakeup generation is enabled.	R	0
1	SOFTRESET	Module software reset. Write 0x0: No action Write 0x1: Start soft reset sequence	W	0
0	AUTOGATING	Internal interface clock gating strategy. Read 0x0: Interface clock is not gated when the L4-CFG interface is idle. Read 0x1: Automatic internal interface clock gating strategy is applied, based on the L4-CFG interface activity.	R	1

Table 21-13. Register Call Summary for Register SPINLOCK_SYSCONFIG

Spinlock Functional Description
- Spinlock Software Reset: [0]
- Spinlock Power Management: [1] [2] [3] [4]

Spinlock Register Manual
- Spinlock Register Summary: [5]

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Table 21-14. SPINLOCK_SYSTATUS

Address Offset	0x0000 0014		
Physical Address	0x4A0F 6014	**Instance**	Spinlock
Description	This register provides status information about this instance of the Spinlock module.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NUMLOCKS								RESERVED								IU7	IU6	IU5	IU4	IU3	IU2	IU1	IU0	RESERVED							RESETDONE

Bits	Field Name	Description	Type	Reset
31:24	NUMLOCKS	Number of lock registers implemeted. Read 0x1: This instance has 32 lock registers. Read 0x2: This instance has 64 lock registers. Read 0x4: This instance has 128 lock registers. Read 0x8: This instance has 256 lock registers.	R	0x01
23:16	RESERVED	Reserved. Reads return 0.	R	0x00
15	IU7	In-Use flag 7. Reads always return 0.	R	0
14	IU6	In-Use flag 6. Reads always return 0.	R	0
13	IU5	In-Use flag 5. Reads always return 0.	R	0
12	IU4	In-Use flag 4. Reads always return 0.	R	0
11	IU3	In-Use flag 3. Reads always return 0.	R	0
10	IU2	In-Use flag 2. Reads always return 0.	R	0
9	IU1	In-Use flag 1. Reads always return 0.	R	0
8	IU0	In-Use flag 0, covering lock registers 0 - 31. Read 0x0: All lock registers 0 31 are in the Not Taken state. Read 0x1: At least one of the lock registers 0 31 is in the Taken state.	R	0
7:1	RESERVED	Reserved. Reads return 0.	R	0x00
0	RESETDONE	Reset done status. Read 0x0: Reset in progress. Read 0x1: Reset is completed.	R	1

Table 21-15. Register Call Summary for Register SPINLOCK_SYSTATUS

Spinlock Functional Description
- Spinlock Software Reset: [0]
- Spinlock Power Management: [1]

Spinlock Programming Guide
- Spinlocks Clearing After a System Bug Recovery: [2] [3]

Spinlock Register Manual
- Spinlock Register Summary: [4]

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Table 21-16. SPINLOCK_LOCK_REG_i

Address Offset	0x0000 0800	**index**	i = 0 to 31
Physical Address	0x4A0F 6800 + (0x4 * i)	**Instance**	Spinlock
Description	This register contains the state of one lock.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															TAKEN

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved. Reads return 0. Writes are ignored.	R	0x0000 0000
0	TAKEN	Lock State Read 0x0: Lock was previously Not Taken (free). The requester is granted the lock. Write 0x0: Set the lock to Not Taken (free). Read 0x1: Lock was previously Taken. The requester is not granted the lock and must retry. Write 0x1: No update to the lock value.	RW	0

Table 21-17. Register Call Summary for Register SPINLOCK_LOCK_REG_i

Spinlock Functional Description
- Spinlock Functional Operation: [0] [1] [2] [3] [4] [5]

Spinlock Programming Guide
- Spinlocks Clearing After a System Bug Recovery: [6] [7]
- Take and Release Spinlock: [8] [9]

Spinlock Register Manual
- Spinlock Register Summary: [10]

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Timers

This chapter describes the timer modules for the device.

Topic **Page**

22.1 Timers Overview **4216**
22.2 General-Purpose Timers **4217**
22.3 Watchdog Timers **4273**
22.4 32-kHz Synchronized Timer **4301**

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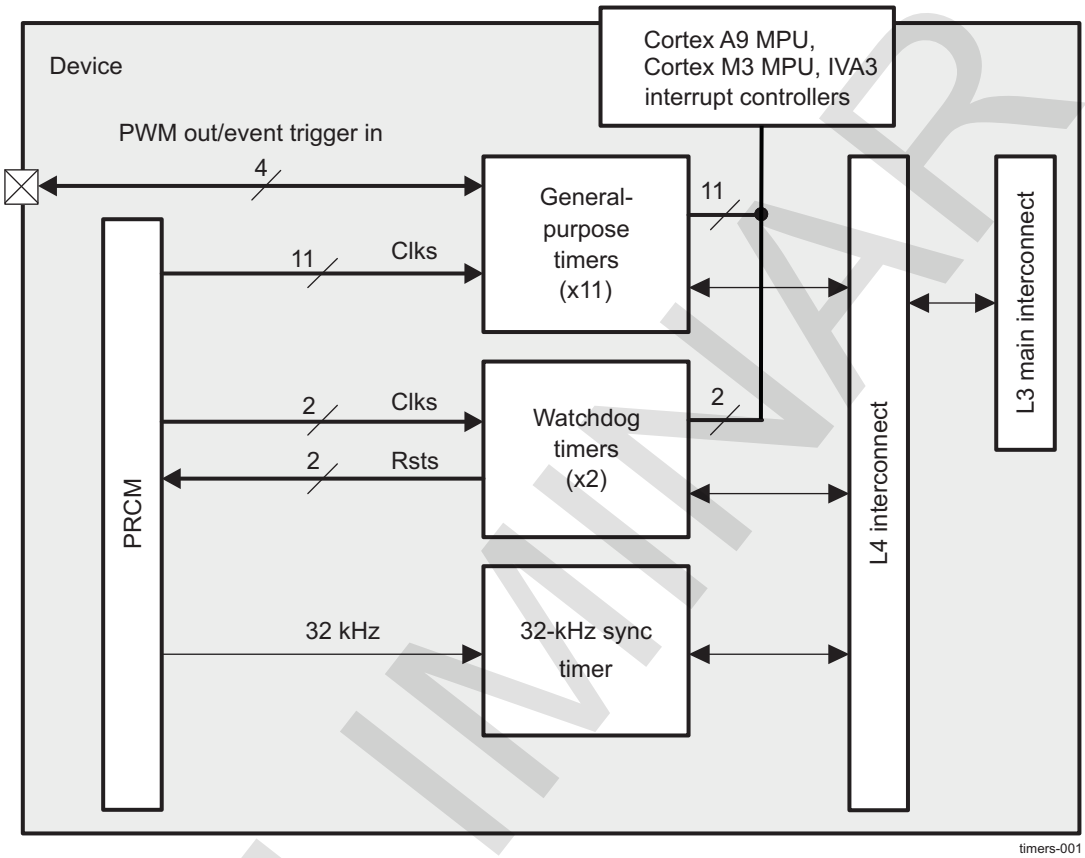
22.1 Timers Overview

The device includes several types of timers used by the system software, including 11 general-purpose (GP) timers , two watchdog timers, and a 32-kHz synchronized timer (sync timer). Figure 22-1 is a high-level block diagram of the device timers.

Figure 22-1. Timers



The two watchdog timers are clocked with 32-kHz clocks. The 32-kHz sync timer, which is reset only at power up, provides the operating system (OS) with a stable timing source that stores the relative time since the last power cycle of the product. Finally, 11 GP timers, which are useful simply as basic timers, are included to generate time-stamp-based interrupts to the system software or to use as a source of pulse-width modulation (PWM) signals.

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22.2 General-Purpose Timers

22.2.1 General-Purpose Timers Overview

The device has 11 general-purpose (GP) timers: GPTIMER1 through GPTIMER11.

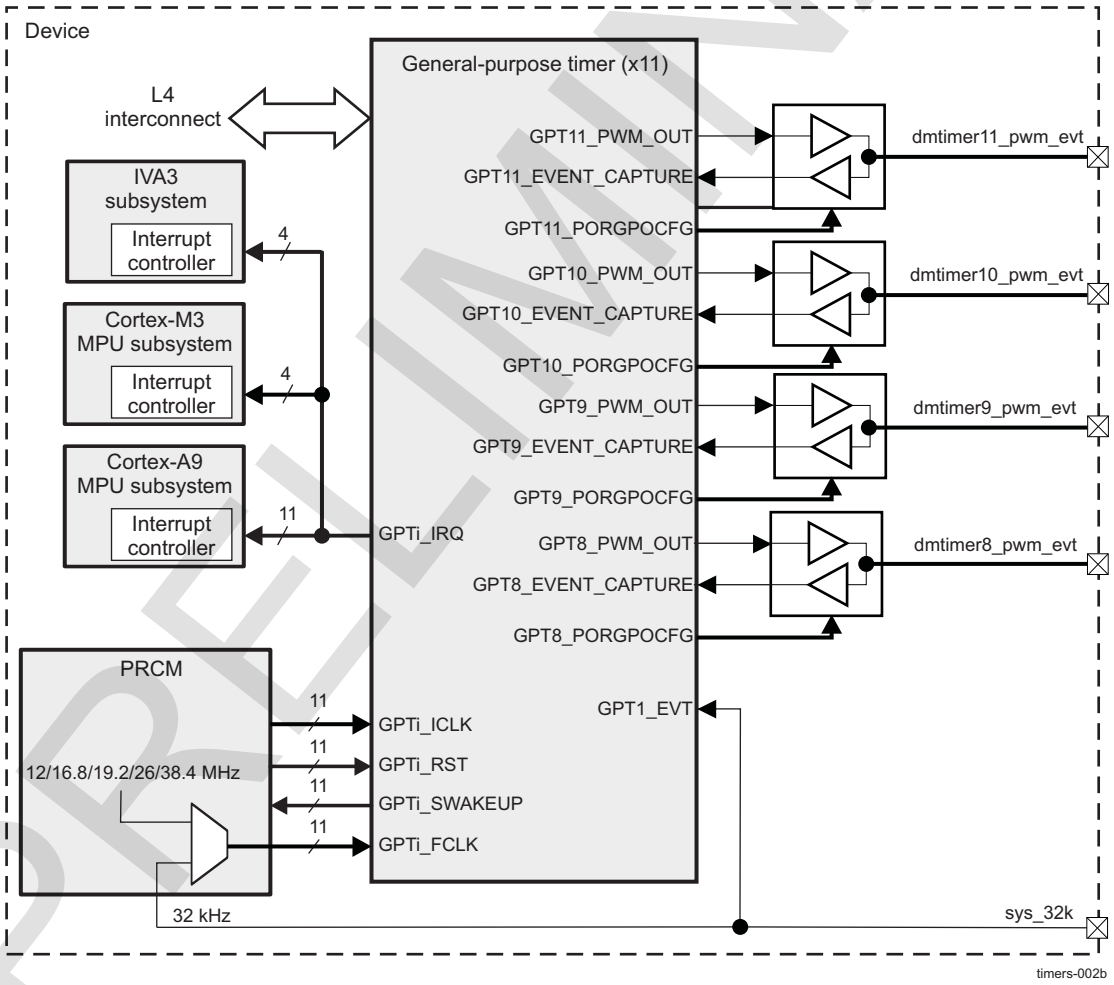
Each timer can be clocked from either the system clock (12, 16.8, 19.2, 26, or 38.4 MHz) or the 32-kHz clock. The selection of clock source is made at the power, reset, and clock management (PRCM) module level. For more information, see , *PRM Clock Source*.

GPTIMER1 has its GPT1_EVENT_CAPTURE pin tied to the 32-kHz clock and can be used to gauge the system clock input; it detects its frequency among 12, 16.8, 19.2, 26, or 38.4 MHz.

Each timer can provide an interrupt to the microprocessor unit (MPU) subsystem. In addition, GPTIMER5 through GPTIMER8 also have interrupts connected to the IVA3 subsystem.

GPTIMER1, GPTIMER2, and GPTIMER10 include specific functions to generate accurate tick interrupts to the operating system. GPTIMER8 through GPTIMER11 are connected to external pins by their PWM output or their event capture input pin (for external timer triggering). Figure 22-2 is an overview of the GP timers.

Figure 22-2. GP Timers Overview



22.2.1.1 GP Timer Features

The following are the main features of the GP timer controllers:

- L4 slave interface support:

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  - 32-bit data bus width
  - 32-/16-bit access supported
  - 8-bit access not supported
  - 10-bit address bus width
  - Burst mode not supported
  - Software-selectable nonposted or posted write/read internal resynchronization modes
- Interrupts generated on overflow, compare, and capture
- Free-running 32-bit upward counter
- Compare and capture modes
- Autoreload mode
- Start/stop mode
- Programmable divider clock source (2^n where n = [0:8])
- Dedicated input trigger for capture mode and dedicated output trigger/PWM signal
- Dedicated GP output signal for using the GPTi_GPOCFG signal
- On-the-fly read/write register (while counting)
- 1-ms tick with 32,768-Hz functional clock generated (only GPTIMER1, GPTIMER2, and GPTIMER10)

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22.2.2 GP Timer Environment

22.2.2.1 GP Timer External System Interface

Four of the 11 GP timers can send or receive stimulus to/from the external (off-chip) system. In the device; however, only GPTIMER8 through GPTIMER11 are configured to output a pulse-width modulation (PWM) pulse or receive an external event signal used as a trigger to capture the current timer count. GPTIMER1 is also configured to receive an event trigger input (GPT1_EVENT_CAPTURE) tied to the internal 32-kHz clock. This event signal gauges the system clock input; detecting its frequency among 12, 16.8, 19.2, 26, or 38.4 MHz.

Figure 22-3 shows the external system interface for the GP timers, and Table 22-1 describes the GP timer inputs and outputs.

NOTE: Software control must ensure that MUX mode is configured to select the dmtimerx_pwm_evt (where x = 8 to 11) signal on only one pad. Other pads on which the same signal is multiplexed must be configured in safe mode or non-dmtimer mode to avoid two different pads driving the same signal.

For more information about the configuration of the dmtimer8_pwm_evt through dmtimer11_pwm_evt I/O pads, see Section 18.4.8, *PAD Functional Multiplexing and Configuration*.

Figure 22-3. GP Timers External System Interface

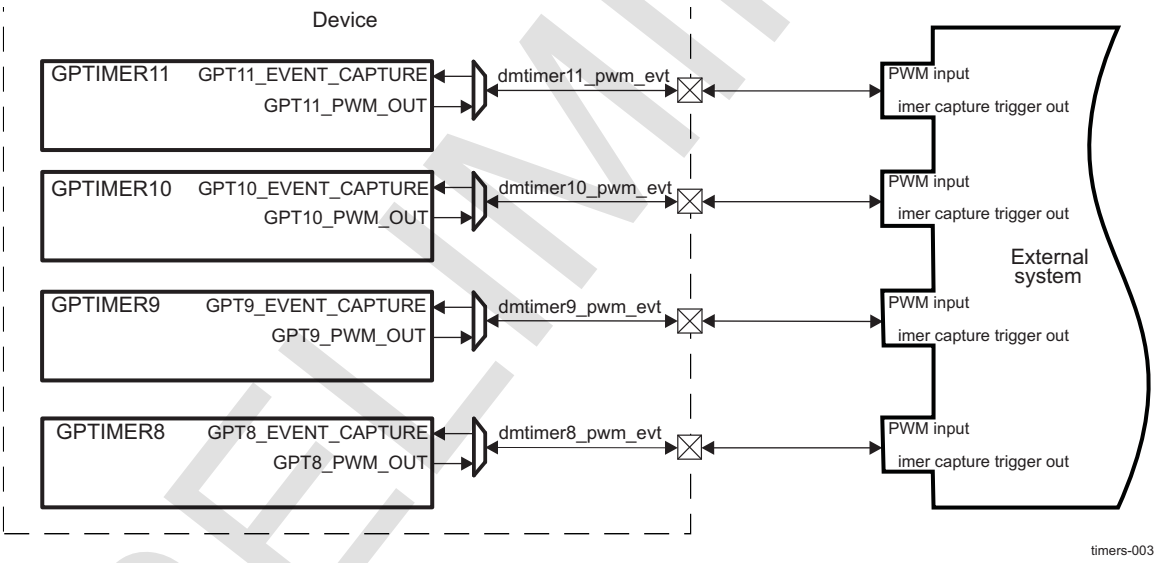

Table 22-1. Input/Output Description

Pin Name	Type [1]	Reset Value	Signal Name	Description
dmtimer8_pwm_evt	I/O	0	GPT8_EVENT_CAPTURE GPT8_PWM_OUT	GPTIMER8 trigger input/ PWM output
dmtimer9_pwm_evt	I/O	0	GPT9_EVENT_CAPTURE GPT9_PWM_OUT	GPTIMER9 trigger input/ PWM output
dmtimer10_pwm_evt	I/O	0	GPT10_EVENT_CAPTURE GPT10_PWM_OUT	GPTIMER10 trigger input/ PWM output
dmtimer11_pwm_evt	I/O	0	GPT11_EVENT_CAPTURE GPT11_PWM_OUT	GPTIMER11 trigger input/ PWM output

(1) When configured for that function; I = input, O = output

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NOTE: The event trigger input (GPTi_EVENT_CAPTURE) for GPTIMER2 through GPTIMER7 is internally tied low, and the PWM output (GPTi_PWM_OUT) is not connected.

NOTE: For GPTIMER8 through GPTIMER11, the GPTi_PORGPOCFG signal selects to connect the GPT pwm output or the GPT capture input to the dmtimerx_pwm_evt (where x = 8 to 11) pad at the top level. When the TCLR[14] GPO_CFG bit = 0b1 , the dmtimerx_pwm_evt functions as a capture input. When the TCLR[14] GPO_CFG bit = 0b0, the dmtimerx_pwm_evt functions as a pwm output (GPO_CFG = 0b0).

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22.2.3 GP Timer Integration

Figure 22-4 shows the integration of the GP timer in the device.

Figure 22-4. GP Timer Integration

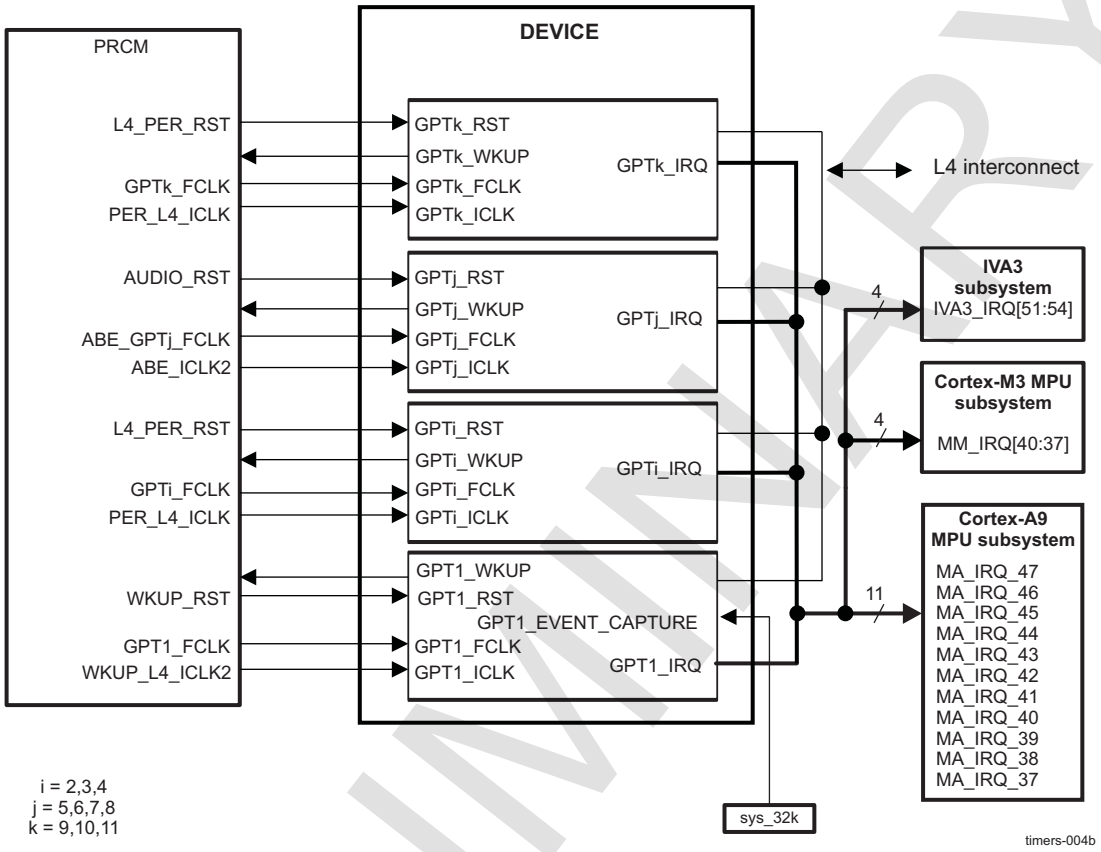

Table 22-2 through Table 22-4 summarize the integration of the module in the device.

Table 22-2. Integration Attributes

Module Instance	Attributes		
	Power Domain	Wake-Up Capability	Interconnect
GPTIMER1	PD_WKUP	Yes	L4_WKUP
GPTIMER2	PD_L4_PER	Yes	L4_PER
GPTIMER3	PD_L4_PER	Yes	L4_PER
GPTIMER4	PD_L4_PER	Yes	L4_PER
GPTIMER5	PD_AUDIO	Yes	L4_ABE
GPTIMER6	PD_AUDIO	Yes	L4_ABE
GPTIMER7	PD_AUDIO	Yes	L4_ABE
GPTIMER8	PD_AUDIO	Yes	L4_ABE
GPTIMER9	PD_L4_PER	Yes	L4_PER
GPTIMER10	PD_L4_PER	Yes	L4_PER
GPTIMER11	PD_L4_PER	Yes	L4_PER

Table 22-3. Clocks and Resets

	Clocks			
Module Instance	Destination Signal Name	Source Signal Name	Source	Description

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Table 22-3. Clocks and Resets (continued)

GPTIMER1	GPT1_FCLK	GPT1_FCLK	PRCM	GPTIMER1 functional clock
GPTIMER1	GPT1_ICLK	WKUP_L4_ICLK2	PRCM	GPTIMER1 interface Clock
GPTIMER2	GPT2_FCLK	GPT2_FCLK	PRCM	GPTIMER2 functional clock
GPTIMER2	GPT2_ICLK	PER_L4_ICLK	PRCM	GPTIMER2 interface Clock
GPTIMER3	GPT3_FCLK	GPT3_FCLK	PRCM	GPTIMER3 functional clock
GPTIMER3	GPT3_ICLK	PER_L4_ICLK	PRCM	GPTIMER3 interface Clock
GPTIMER4	GPT4_FCLK	GPT4_FCLK	PRCM	GPTIMER4 functional clock
GPTIMER4	GPT4_ICLK	PER_L4_ICLK	PRCM	GPTIMER4 interface Clock
GPTIMER5	GPT5_FCLK	ABE_GPT5_FCLK	PRCM	GPTIMER5 functional clock
GPTIMER5	GPT5_ICLK	ABE_ICLK2	PRCM	GPTIMER5 interface Clock
GPTIMER6	GPT6_FCLK	ABE_GPT6_FCLK	PRCM	GPTIMER6 functional clock
GPTIMER6	GPT6_ICLK	ABE_ICLK2	PRCM	GPTIMER6 interface Clock
GPTIMER7	GPT7_FCLK	ABE_GPT7_FCLK	PRCM	GPTIMER7 functional clock
GPTIMER7	GPT7_ICLK	ABE_ICLK2	PRCM	GPTIMER7 interface Clock
GPTIMER8	GPT8_FCLK	ABE_GPT8_FCLK	PRCM	GPTIMER8 functional clock
GPTIMER8	GPT8_ICLK	ABE_ICLK2	PRCM	GPTIMER8 interface Clock
GPTIMER9	GPT9_FCLK	GPT9_FCLK	PRCM	GPTIMER9 functional clock
GPTIMER9	GPT9_ICLK	PER_L4_ICLK	PRCM	GPTIMER9 interface Clock
GPTIMER10	GPT10_FCLK	GPT10_FCLK	PRCM	GPTIMER10 functional clock
GPTIMER10	GPT10_ICLK	PER_L4_ICLK	PRCM	GPTIMER10 interface Clock
GPTIMER11	GPT11_FCLK	GPT11_FCLK	PRCM	GPTIMER11 functional clock
GPTIMER11	GPT11_ICLK	PER_L4_ICLK	PRCM	GPTIMER11 interface Clock
		Resets		
GPTIMER1	GPT1_RST	WKUP_RST	PRM	Reset to GPTIMER1
GPTIMER2	GPT2_RST	L4_PER_RST	PRM	Reset to GPTIMER2
GPTIMER3	GPT3_RST	L4_PER_RST	PRM	Reset to GPTIMER3
GPTIMER4	GPT4_RST	L4_PER_RST	PRM	Reset to GPTIMER4
GPTIMER5	GPT5_RST	AUDIO_RST	PRM	Reset to GPTIMER5
GPTIMER6	GPT6_RST	AUDIO_RST	PRM	Reset to GPTIMER6
GPTIMER7	GPT7_RST	AUDIO_RST	PRM	Reset to GPTIMER7
GPTIMER8	GPT8_RST	AUDIO_RST	PRM	Reset to GPTIMER8
GPTIMER9	GPT9_RST	L4_PER_RST	PRM	Reset to GPTIMER9
GPTIMER10	GPT10_RST	L4_PER_RST	PRM	Reset to GPTIMER10
GPTIMER11	GPT11_RST	L4_PER_RST	PRM	Reset to GPTIMER11

Table 22-4. Hardware Requests

Interrupt Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
GPTIMER1	GPT1_IRQ	MA_IRQ_37	Cortex™-A9 MPU	GPTIMER1 interrupt to Cortex-A9 MPU
GPTIMER2	GPT2_IRQ	MA_IRQ_38	Cortex-A9™ MPU	GPTIMER2 interrupt to Cortex-A9 MPU
GPTIMER3	GPT3_IRQ	MA_IRQ_39	Cortex-A9 MPU	GPTIMER3 interrupt to Cortex-A9 MPU
	GPT3_IRQ	MM_IRQ_37	Cortex-M3™ MPU	GPTIMER3 interrupt to Cortex-M3 MPU
GPTIMER4	GPT4_IRQ	MA_IRQ_40	Cortex-A9 MPU	GPTIMER3 interrupt to Cortex-A9 MPU
	GPT4_IRQ	MM_IRQ_38	Cortex-M3 MPU	GPTIMER4 interrupt to Cortex-M3 MPU
GPTIMER5	GPT5_IRQ	D_IRQ_51	DSP	GPTIMER5 interrupt to DSP
	GPT5_IRQ	MA_IRQ_41	Cortex-A9 MPU	GPTIMER5 interrupt to Cortex-A9 MPU
GPTIMER6	GPT6_IRQ	D_IRQ_52	DSP	GPTIMER6 interrupt to DSP

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Table 22-4. Hardware Requests (continued)

	GPT6_IRQ	MA_IRQ_42	Cortex-A9 MPU	GPTIMER6 interrupt to Cortex-A9 MPU
GPTIMER7	GPT7_IRQ	D_IRQ_53	DSP	GPTIMER7 interrupt to DSP
	GPT7_IRQ	MA_IRQ_43	Cortex-A9 MPU	GPTIMER7 interrupt to Cortex-A9 MPU
GPTIMER8	GPT8_IRQ	D_IRQ_54	DSP	GPTIMER8 interrupt to DSP
	GPT8_IRQ	MA_IRQ_44	Cortex-A9 MPU	GPTIMER8 interrupt to Cortex-A9 MPU
GPTIMER9	GPT9_IRQ	MA_IRQ_45	Cortex-A9 MPU	GPTIMER3 interrupt to Cortex-A9 MPU
	GPT9_IRQ	MM_IRQ_39	Cortex-M3 MPU	GPTIMER9 interrupt to Cortex-M3 MPU
GPTIMER10	GPT10_IRQ	MA_IRQ_46	Cortex-A9 MPU	GPTIMER10 interrupt to Cortex-A9 MPU
GPTIMER11	GPT11_IRQ	MA_IRQ_47	Cortex-A9 MPU	GPTIMER3 interrupt to Cortex-A9 MPU
	GPT11_IRQ	MM_IRQ_40	Cortex-M3 MPU	GPTIMER11 interrupt to Cortex-M3 MPU
No DMA Requests				

NOTE: For the desctiption of the interrupt source description, see Section 22.2.4.5, *GP Timer Interrupts*.

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22.2.4 GP Timer Functional Description

Each GP timer contains a free-running upward counter with autoreload capability on overflow. The timer counter can be read and written on-the-fly (while counting). Each GP timer includes compare logic to allow an interrupt event on a programmable counter matching value. A dedicated output signal can be pulsed or toggled on either an overflow or a match event. This offers time-stamp trigger signaling or PWM signal sources. A dedicated input signal can be used to trigger an automatic timer counter capture or an interrupt event on a programmable input signal transition. A programmable clock divider (prescaler) allows reduction of the timer input clock frequency. All internal timer interrupt sources are merged into one module interrupt line and one wake-up line.

Each internal interrupt source can be independently enabled/disabled with a dedicated bit of the GPT_TIER register for the interrupt features, and a dedicated bit of the GPT_TWER register for the wake-up of GPTIMER1, GPTIMER2, and GPTIMER10. In addition, these timers have a mechanism implemented to generate an accurate tick interrupt.

For the other GP Timers, each internal interrupt source can be independently enabled/disabled through the GPT_IRQENABLE_SET and GPT_IRQENABLE_CLR register bit fields.

For each GP timer implemented in the device, there are two possible clock sources:

- 32-kHz clock
- System clock

Selection of the input clock source is done in the registers in the PRCM configuration (see Section 22.2.1, *GP Timer Overview*).

Each GP timer supports three functional modes:

- Timer mode
- Capture mode
- Compare mode

The capture and compare modes are disabled by default after core reset.

22.2.4.1 GP Timer Block Diagram

Figure 22-5 is a block diagram of the common GP timers, and Figure 22-6 is a block diagram of the GP timers with 1-ms tick generation module.

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Figure 22-5. Block Diagram of GPTIMER3 Through GPTIMER9, and GPTIMER11

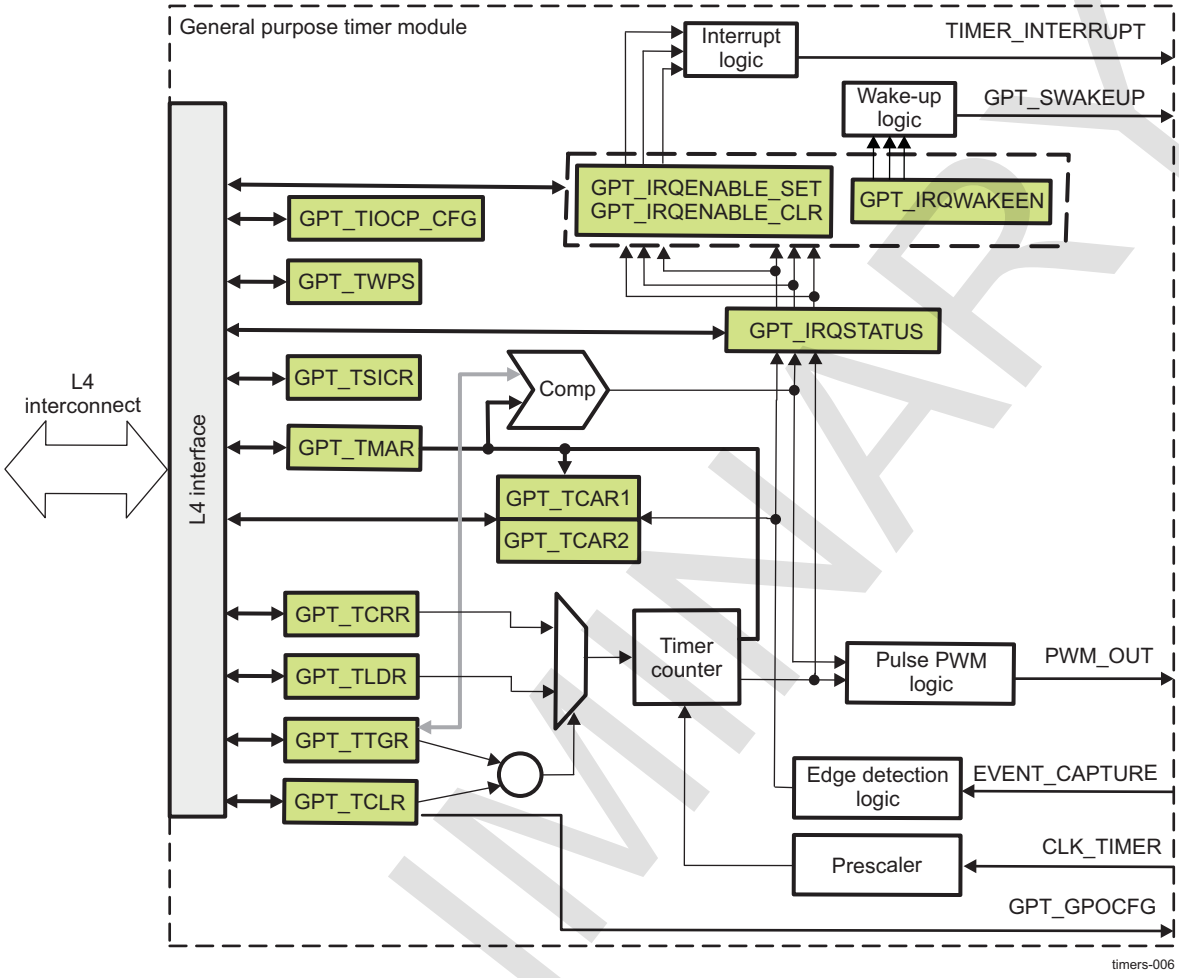

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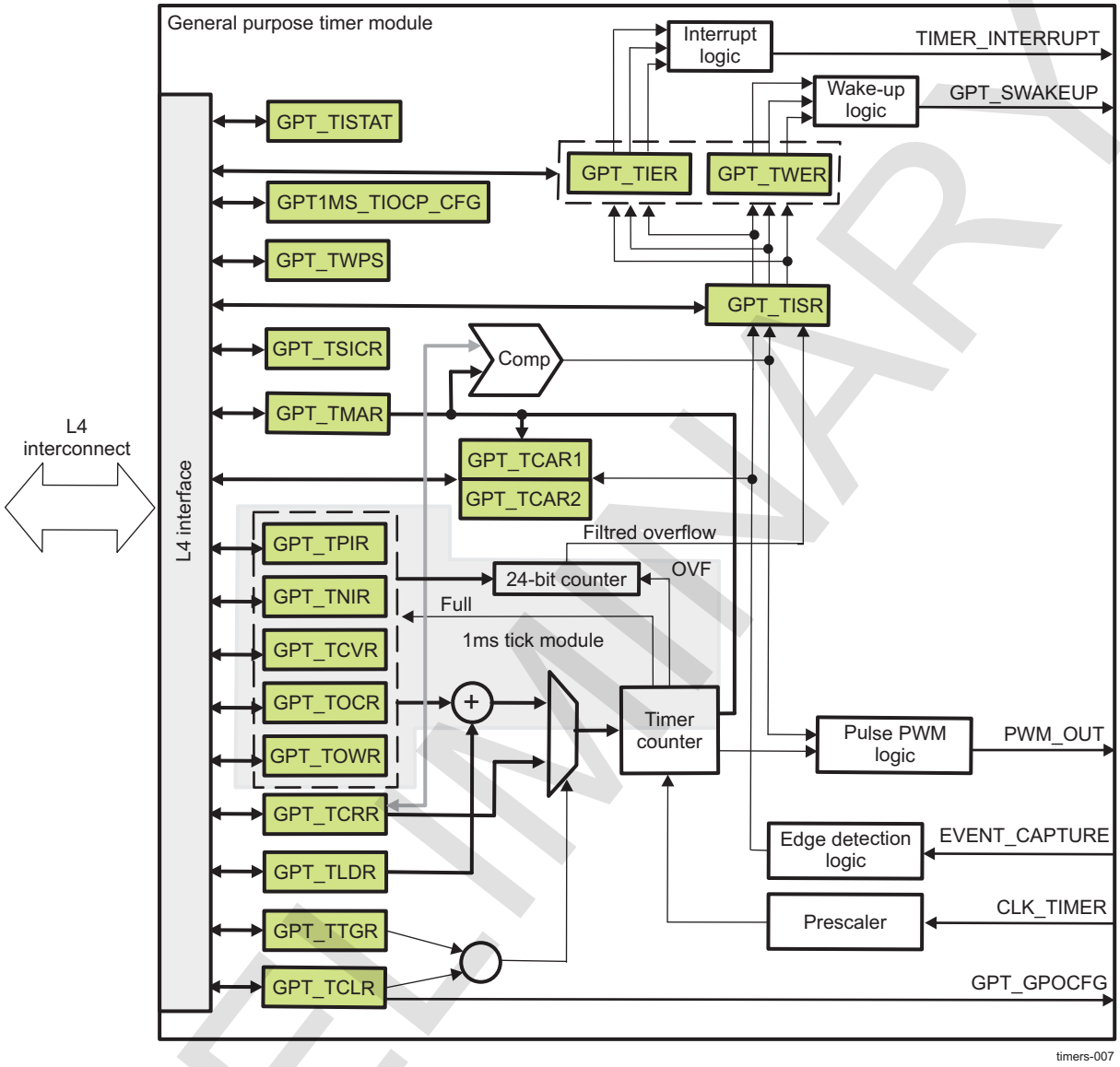
Figure 22-6. Block Diagram of GPTIMER1, GPTIMER2, and GPTIMER10



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22.2.4.2 GPTIMER1, GPTIMER2, and GPTIMER10 Power Management

The GP timer modules have an internal bit, GPT1MS_TIOCP_CFG[0] AUTOIDLE, that is used to apply an internal interface clock gating strategy.

At the PRCM module level, when all conditions to shut off the PRCM module functional or interface output clocks are met (see Section 3.1.1.1.4, *Clock Domain-Level Clock Management*), the PRCM module automatically launches a hardware handshake protocol to ensure the GP timer is ready to have its clocks switched off. Namely, the PRCM module asserts an IDLE request to the GP timer.

Although this handshake is a hardware function and is out of software control, the way the GP timer acknowledges the PRCM IDLE request is configurable through the GPT1MS_TIOCP_CFG[4:3] IDLEMODE bit field.

Table 22-7 lists the IDLEMODE settings and the related acknowledgment modes.

Table 22-5. IDLEMODE Settings

IDLEMODE Value	Selected Mode	Description
00	Force-idle	The GP timer unconditionally acknowledges the IDLE request from the PRCM module, regardless of its internal operations. This mode must be used carefully, because it does not prevent the loss of data when the clock is switched off.
01	No-idle	The GP timer never acknowledges an IDLE request from the PRCM module. This mode is safe from a module point of view, because it ensures that the clocks remain active. It is not efficient from a power-saving perspective, because it does not allow the PRCM output clock to be shut off and thus the power domain to be set to a lower power state.
10	Smart-idle	The GP timer acknowledges the IDLE request, basing its decision on its internal activity. The acknowledge signal is asserted only when all pending transactions and IRQ requests are treated. This is the best approach to efficient system power management.
11	Reserved	

When configured in smart-idle mode, the GP timer also offers an additional granularity on GPTi_FCLK and GPTi_ICLK gating. The GPT1MS_TIOCP_CFG[9:8] CLOCKACTIVITY bit field is used to determine which clock is shut down (GPTi_FCLK, GPTi_ICLK, neither, or both clocks).

The CLOCKACTIVITY setting is used internally to the GP timer to determine the part of the module on which the conditions to acknowledge the PRCM IDLE request are tested. For example, if GPTi_FCLK is not to be shut down on a PRCM IDLE request, the GP timer considers only GPTi_ICLK and associated pending activities before acknowledging the request.

Some GP timer features are associated with GPTi_ICLK and others are associated with GPTi_FCLK. Using the CLOCKACTIVITY setting along with the smart-idle mode ensures that the features associated with the clock that remains active are always enabled, even if the GP timer acknowledges an IDLE request.

Table 22-6 lists the CLOCKACTIVITY settings and associated features.

Table 22-6. CLOCKACTIVITY Settings

CLOCKACTIVITY Value	GPTi_ICLK Effects	GPTi_FCLK Effects	Description	Associated Features
00	OFF	OFF	GPTi_ICLK and GPTi_FCLK are considered for generating the acknowledge. This setting also means GPTi_FCLK and GPTi_ICLK are likely to be shut down on PRCM IDLE request.	The idle acknowledge signal is asserted when there are no pending activities on the functional clock domain (improved latency in assertion of idle acknowledge). The wake-up capability of the GP timer is disabled.
01	ON	OFF	GPTi_ICLK is not shut down on PRCM IDLE request; only GPTi_FCLK is affected.	

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Table 22-6. CLOCKACTIVITY Settings (continued)

CLOCKACTIVITY Value	GPTi_ICLK Effects	GPTi_FCLK Effects	Description	Associated Features
10	OFF	ON	GPTi_FCLK is not shut down on PRCM IDLE request; only GPTi_ICLK is affected.	The idle acknowledge signal is asserted when there are no pending activities on the interface clock domain, without evaluating the pending activities on the functional clock domain (the GP timer enters into sleep mode, and if a pending interrupt event is completed during idle mode, the wake-up signal is asserted). The wake-up signal is enabled.
11	ON	ON	None of the clocks are shut down. Therefore, the GP timer can potentially acknowledge the IDLE request without checking the internal functionalities linked to its clocks.	

CAUTION

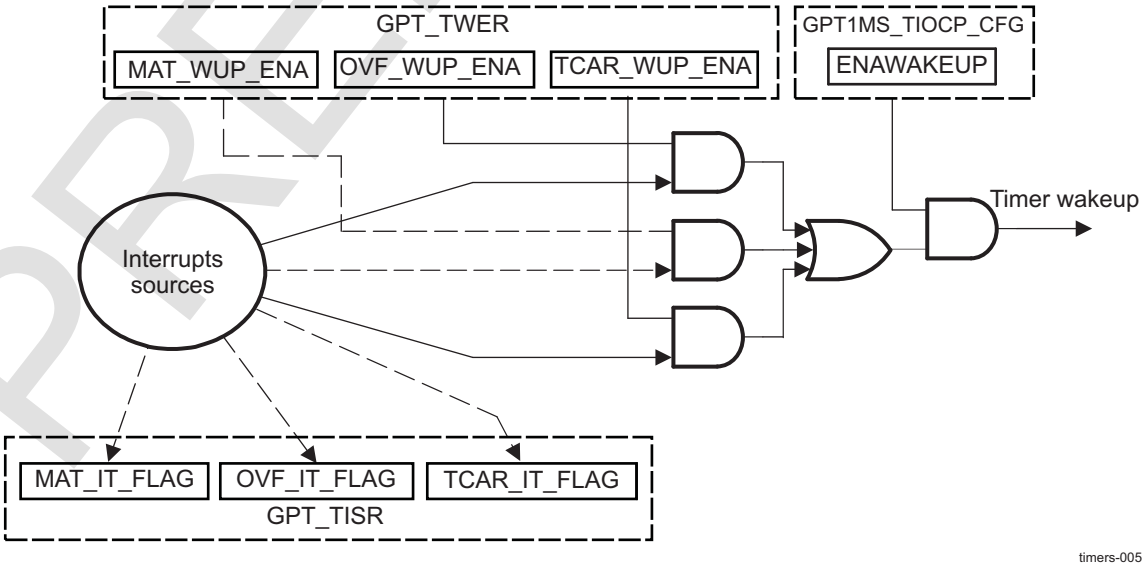
The PRCM module does not have any hardware means to read the CLOCKACTIVITY settings. The software must ensure consistent programming between the GP timer CLOCKACTIVITY and the PRCM module functional clock and interface clock control bits. If the GP timer is disabled in the CM_FCLKEN and CM_ICLKEN PRCM registers while CLOCKACTIVITY is set to 11, nothing prevents the PRCM module from asserting its IDLE request, which is acknowledged regardless of the features associated with the GP timer clocks. This can lead to unpredictable behavior.

22.2.4.2.1 Wake-Up Capability

If the GPT1MS_TIOCP_CFG[4:3] IDLEMODE bit field sets the smart-idle mode, the timer evaluates its internal capability to have the interface clock switched off. When there is no further internal activity (no pending interrupt sources: match, overflow, or timer capture events), the idle acknowledge signal is asserted and the timer enters sleep mode, ready to issue a wake-up request. This wake-up request is sent only if the GPT1MS_TIOCP_CFG[2] ENAWAKEUP bit enables the timer wake-up capability.

Figure 22-7 shows the wake-up request generation. For more information on the GP timer clock control, see Section 3.6, *Clock Management Functional Description* in Chapter 3, *Power, Reset and Clock Management*.

Figure 22-7. Wake-Up Request Generation



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For GPTIMER1, GPTIMER2, and GPTIMER10, the timer wake-up enable-register (GPT_TWER) allows masking the expected source of the wake-up event that generates a wake-up request. The GPT_TWER register is synchronously programmed with the interface clock before the PRCM module sends an idle mode request. The expected source of the wake-up event is an overflow (GPT_TCRR), a timer match (the compare result of GPT_TCRR and GPT_TMAR matches the counter value), and a timer capture (detection of an external pulse transition of the correct polarity on the GPT_EVENT_CAPTURE).

When the wake-up event is issued, the associated interrupt status bit is set in the timer status register (GPT_TISR). The pending wake-up event is reset when the set status bit is overwritten with 1.

NOTE: The status bit must be reset to re-enter idle mode.

22.2.4.3 Power Management of Other GP Timers

At the PRCM module level, when all conditions to shut off the PRCM module functional or interface output clocks are met (see Section 3.1.1.1.4, *Clock Domain Level Clock Management*), the PRCM module automatically launches a hardware handshake protocol to ensure the GP timer is ready to have its clocks switched off. Namely, the PRCM module asserts an IDLE request to the GP timer.

Although this handshake is a hardware function and is out of software control, the way the GP timer acknowledges the PRCM IDLE request is configurable through the GPT_TIOCP_CFG[3:2] IDLEMODE bit field.

Table 22-7 lists the IDLEMODE settings and the related acknowledgment modes.

Table 22-7. IDLEMODE Settings

IDLEMODE Value	Selected Mode	Description
00	Force-idle	The GP timer unconditionally acknowledges the IDLE request from the PRCM module, regardless of its internal operations. This mode must be used carefully, because it does not prevent the loss of data when the clock is switched off.
01	No-idle	The GP timer never acknowledges an IDLE request from the PRCM module. This mode is safe from a module point of view, because it ensures that the clocks remain active. It is not efficient from a power-saving perspective, however, because it does not allow the PRCM output clock to be shut off and thus the power domain to be set to a lower power state.
10	Smart-idle	The GP timer acknowledges the IDLE request, basing its decision on its internal activity. The acknowledge signal is asserted only when all pending transactions and IRQ requests are treated. This is the best approach to efficient system power management.
11	Reserved	

22.2.4.3.1 Wake-Up Capability

If the GPT_TIOCP_CFG[3:2] IDLEMODE bit field sets the smart-idle mode, the timer evaluates its internal capability to have the interface clock switched off. When there is no further internal activity (no pending interrupt sources: match, overflow, or timer capture events), the idle acknowledge signal is asserted and the timer enters sleep mode, ready to issue a wake-up request. This wake-up request is sent only if the GPT_IRQWAKEEN[2:0] bit field enables the timer wake-up capability.

Figure 22-8 shows the wake-up request generation. For more information on the GP timer clock control, see Section 3.6, *Clock Management Functional Description* in Chapter 3, *Power, Reset and Clock Management*.

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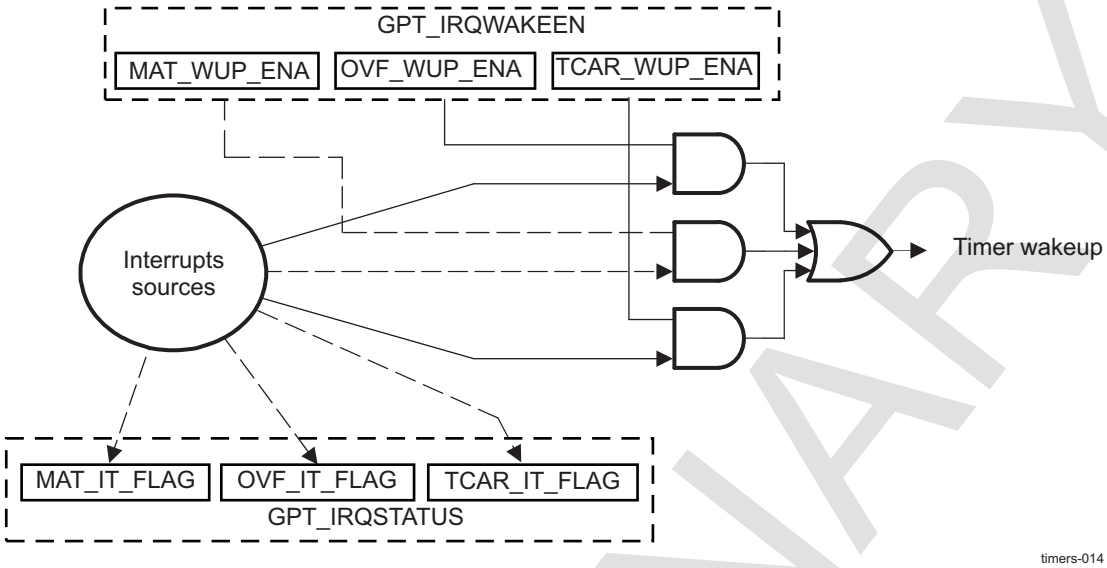
Figure 22-8. Wake-Up Request Generation



When the wake-up event is issued, the associated interrupt status bit is set in the timer status register (GPT_IRQSTATUS). The pending wake-up event is reset when the set status bit is overwritten with 1.

NOTE: The status bit must be reset to re-enter idle mode.

22.2.4.4 Software Reset

Two bit fields can generate a software reset of the GP timer:

- GPT1MS_TIOCP_CFG[1] SOFTRESET for GPTIMER1, GPTIMER2, and GPTIMER10, and GPT_TIOCP_CFG[0] SOFTRESET for other timers
- GPT_TSICR[1] SFT for all timers

For both bits, all read accesses return 0.

The GPT1MS_TIOCP_CFG[1] SOFTRESET/GPT_TIOCP_CFG[0] SOFTRESET bit allows resetting the functional and interface domains. The GPT_TSICR[1] SFT bit allows resetting the functional part of the GP timer.

Before accessing or using the GP timer, the local host must ensure that both internal resets are released by reading the GPT_TISTAT[0] RESETDONE (for GPTIMER1, GPTIMER2, and GPTIMER10), or the GPT_TIOCP_CFG[0] SOFTRESET bit (for other timers). This bit monitors the internal reset status.

22.2.4.5 GP Timer Interrupts

The timer can issue an overflow interrupt, a timer match interrupt, and a timer capture interrupt. Each internal interrupt source can be independently enabled/disabled in the interrupt-enable register (GPT_TIER for GPTIMER1, GPTIMER2, and GPTIMER10), or, for other timers, enable in the interrupt-enable register (GPT_IRQENABLE_SET) and disable in the interrupt disable register (GPT_IRQENABLE_CLR). When the interrupt event is issued, the associated interrupt status bit is set in the timer status register (GPT_TISR for GPTIMER1, GPTIMER2, and GPTIMER10, and GPT_IRQSTATUS for other timers).

22.2.4.6 Timer Mode Functionality

The timer is an upward counter that can be started and stopped at any time through the timer control register (GPT_TCLR[0] ST bit). The timer counter register (GPT_TCRR) can be loaded when stopped or on-the-fly (while counting). GPT_TCRR can be loaded directly by a GPT_TCRR write access with a new

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timer value. The GPT_TCRR register can also be loaded with the value held in the timer-load register GPT_TLDR by a trigger register (GPT_TTGR) write access. Loading of GPT_TCRR is done regardless of the GPT_TTGR written value. The timer counter register GPT_TCRR value can be read when stopped, or captured on-the-fly by a GPT_TCRR read access. The timer is stopped and the counter value is set to 0 when the module reset is asserted. The timer is maintained at stop after the reset is released.

In one-shot mode (the GPT_TCLR[1] AR bit set to 0), the counter is stopped after counting overflow occurs (the counter value remains at 0).

When the autoreload mode is enabled (the GPT_TCLR[1] AR bit set to 1), the GPT_TCRR register is reloaded with the timer-load register (GPT_TLDR) value after a counting overflow occurs.

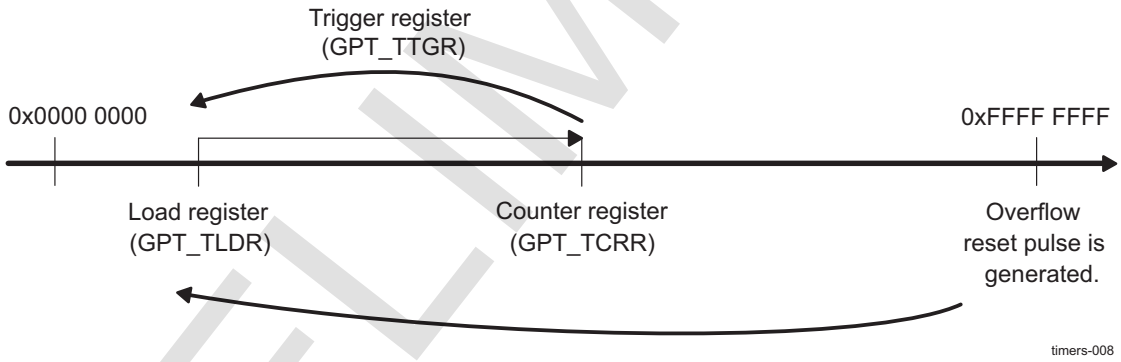
CAUTION

Do not put the overflow value (0xFFFF FFFF) in the GPT_TLDR register because it can lead to undesirable results.

An interrupt can be issued on overflow if the overflow interrupt-enable bit is set in the timer interrupt-enable register (GPT_TIER[1] OVF_IT_ENA bit set to 1 for GPTIMER1, GPTIMER2, and GPTIMER10, or GPT_IRQENABLE_SET[1] OVF_IT_FLAG bit set to 1 for other timers). A dedicated output pin (timer PWM) can be programmed in GPT_TCLR[12] through GPT_TCLR[11:10] (PT and TRG bits) to generate one positive pulse (prescaler duration) or to invert the current value (toggle mode) when an overflow occurs. The GPT_TCLR[12] PT bit selects pulse/toggle modulation (GPT_TCLR[11:10] TRG bit field selects trigger mode).

Figure 22-9 shows the GPT_TCRR timing value.

Figure 22-9. GPT_TCRR Timing Value



22.2.4.6.1 1-ms Tick Generation (Only GPTIMER1, GPTIMER2, and GPTIMER10)

The interrupt period is not exactly 1 ms because the timer input clock is 32,768 Hz. If the clock counts up to 32, it obtains a 0.977-ms period; if it counts up to 33, it obtains a 1.007-ms period. For large granularity, the error is cumulative and can generate important deviations from the standard value.

To minimize the error between a true 1-ms tick and the tick generated by the 32,768 Hz timer, the sequencing of periods less than 1 ms and periods greater than 1 ms must be shuffled. An additional 1-ms block is used to correct this error. See Figure 22-10.

In this implementation, the increment sequencing is automatically managed by the timer to minimize the error. The user must define only the value of the timer positive increment register (GPT_TPIR[31:0] POSITIVE_INC_VALUE bit field) and the timer negative increment register (GPT_TNIR[31:0] NEGATIVE_INC_VALUE bit field). An automatic adaptation mechanism is used to simplify the programming model.

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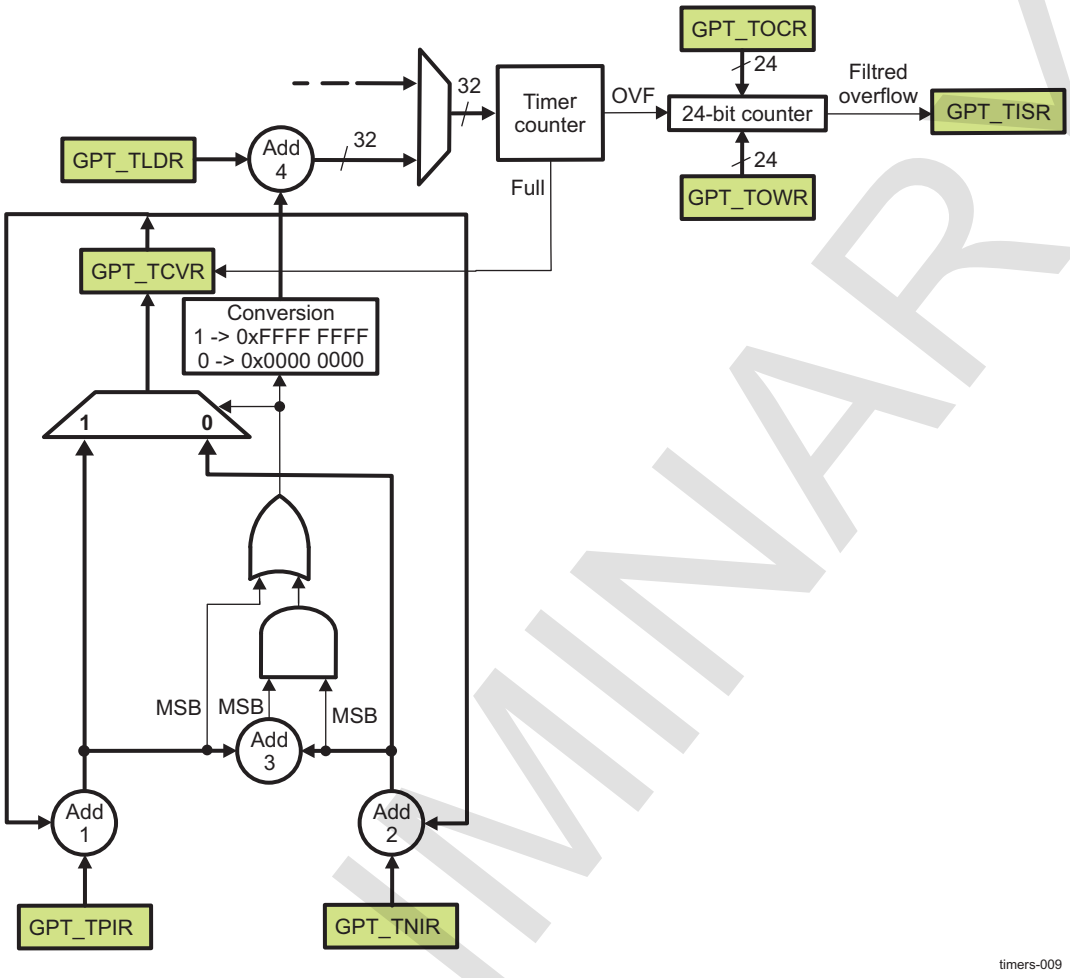
Figure 22-10. Block Diagram of the 1-ms Tick Module



The GPT_TPIR, GPT_TNIR, and GPT_TCVR registers and adders Add1, Add2, and Add3 are used to define whether the next value loaded in the timer counter register (GPT_TCRR[31:0] TIMER_COUNTER bit field) is the value of the GPT_TLDR[31:0] LOAD_VALUE bit field (period less than 1 ms) or the value of GPT_TLDR[31:0] LOAD_VALUE –1 (period greater than 1 ms).

Table 22-8 lists the value loaded in the GPT_TCRR register according to the sign of the result of Add1, Add2, and Add3.

MSB = 0: Positive value, MSB = 1: Negative value

Table 22-8. Value Loaded in GPT_TCRR to Generate 1-ms Tick

Add1 MSB	Add2 MSB	Add3 MSB	Value of GPT_TCRR Register
0	0	0	GPT_TLDR[31:0] LOAD_VALUE bit field
0	0	1	GPT_TLDR[31:0] LOAD_VALUE bit field
0	1	0	GPT_TLDR[31:0] LOAD_VALUE bit field
0	1	1	GPT_TLDR[31:0] LOAD_VALUE –1
1	0	0	N/A
1	0	1	N/A
1	1	0	GPT_TLDR[31:0] LOAD_VALUE –1
1	1	1	GPT_TLDR[31:0] LOAD_VALUE –1

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The values of the GPT_TPIR and GPT_TNIR registers are calculated using the following formula:

- Positive increment value = ((INTEGER[F_{clk} * T_{tick}] + 1) * 1e6) - (F_{clk} * T_{tick} * 1e6)
- Negative increment value = (INTEGER[F_{clk} * T_{tick}] * 1e6) - (F_{clk} * T_{tick} * 1e6)

NOTE: Fclk clock frequency (kHz)

Ttick tick period (ms)

The timer overflow counter register (GPT_TOCR) and the timer overflow wrapping register GPT_TOWR) are used to filter interrupts. When the timer overflows, it increments the 24-bit GPT_TOCR register. When the 24-bit GPT_TOCR register values match the value in the 24-bit GPT_TOWR register and the timer overflow is asserted, the GPT_TOCR register is reset and an interrupt is generated to the GPT_TISR register.

With the conversion block in reset state (the positive increment register, negative increment register, and counter value register are zeroed), the programming model and the behavior of GPTIMER1, GPTIMER2, and GPTIMER10 remain unchanged.

For 1-ms tick with a 32,768-Hz clock:

- GPT_TPIR[31:0] POSITIVE_INC_VALUE = 232000
- GPT_TNIR[31:0] NEGATIVE_INC_VALUE = –768000
- GPT_TLDR[31:0] LOAD_VALUE = 0xFFFF FFE0

NOTE: Any value of the tick period can be generated with the appropriate value of the GPT_TPIR, GPT_TNIR, and GPT_TLDR registers.

By default, the GPT_TPIR, GPT_TNIR, GPT_TCVR, GPT_TOCR, and GPT_TOWR registers and the associated logic are in reset mode (all 0s) and have no action on the programming model.

22.2.4.7 Capture Mode Functionality

When a transition is detected on the module input pin (EVENT_CAPTURE), the timer value in the GPT_TCRR register can be captured and saved in the GPT_TCAR1 or TCAR2 register function of the mode selected in the GPT_TCLR[13] CAPT_MODE bit. The edge detection circuitry monitors transitions on the input pin (EVENT_CAPTURE).

The rising edge, falling edge, or both, can be selected in the GPT_TCLR[9:8] TCM bit field to trigger the timer counter capture. The module sets the GPT_TISR[2] TCAR_IT_FLAG bit for GPTIMER1, GPTIMER2, or GPTIMER10, and the GPT_IRQSTATUS[2] TCAR_IT_FLAG bit for other timers, when an active edge is detected, and at the same time, the counter value GPT_TCRR is stored in timer capture register GPT_TCAR1 or GPT_TCAR2, as follows:

- If the GPT_TCLR[13] CAPT_MODE bit is 0, on the first enabled capture event, the value of the counter register is saved in the GPT_TCAR1 register, and all the next events are ignored (no update on the GPT_TCAR1 register and no interrupt triggering) until the detection logic is reset or the GPT_TISR[2] TCAR_IT_FLAG bit (or GPT_IRQSTATUS[2] TCAR_IT_FLAG, depending on the timer) is cleared by writing 1 to it.
- If the GPT_TCLR[13] CAPT_MODE bit is 1, on the first enabled capture event, the value of the counter register is saved in the GPT_TCAR1 register, and on the second enabled capture event, the value of the counter register is saved in the GPT_TCAR2 register. If a capture interrupt is enabled, the interrupt triggers on the second event capture. All other events are ignored (no update on GPT_TCAR1/GPT_TCAR2 and no interrupt triggering) until the detection logic is reset or GPT_TISR[2] TCAR_IT_FLAG bit (or GPT_IRQSTATUS[2] TCAR_IT_FLAG, depending on the timer) is cleared by writing 1 to it. This mechanism is useful for period calculation of a clock, if that clock is connected to the EVENT_CAPTURE input pin.

The edge detection logic is reset (a new capture is enabled) when the active capture interrupt is served. The GPT_TISR[2] TCAR_IT_FLAG bit or the GPT_IRQSTATUS[2] TCAR_IT_FLAG (previously 1) is cleared by writing 1 to it or when the edge detection mode bits (the GPT_TCLR[9:8] TCM bit field) are

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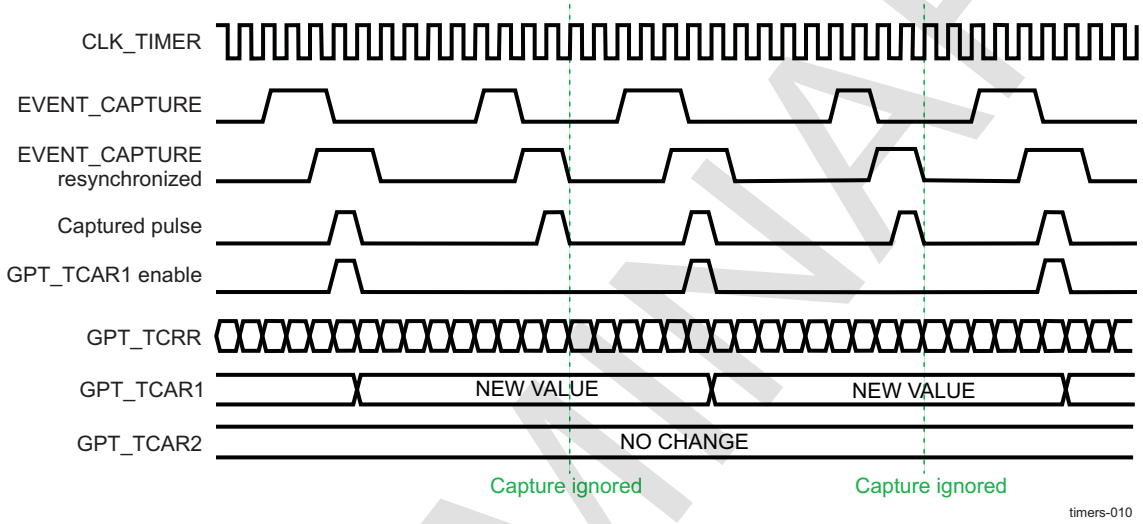
changed from no-capture mode detection to any other mode. The timer functional clock (input to prescaler) is used to sample the input pin (EVENT_CAPTURE). A negative or positive pulse input can be detected when the pulse time is greater than the functional clock period. An interrupt is issued on edge detection if the capture interrupt-enable bit is set in the GPT_TIER[2] TCAR_IT_ENA bit (for GPTIMER1, GPTIMER2, or GPTIMER10), or in the GPT_IRQENABLE_SET[2] TCAR_EN_FLAG bit (for other timers). See the examples in Figure 22-11 and Figure 22-12.

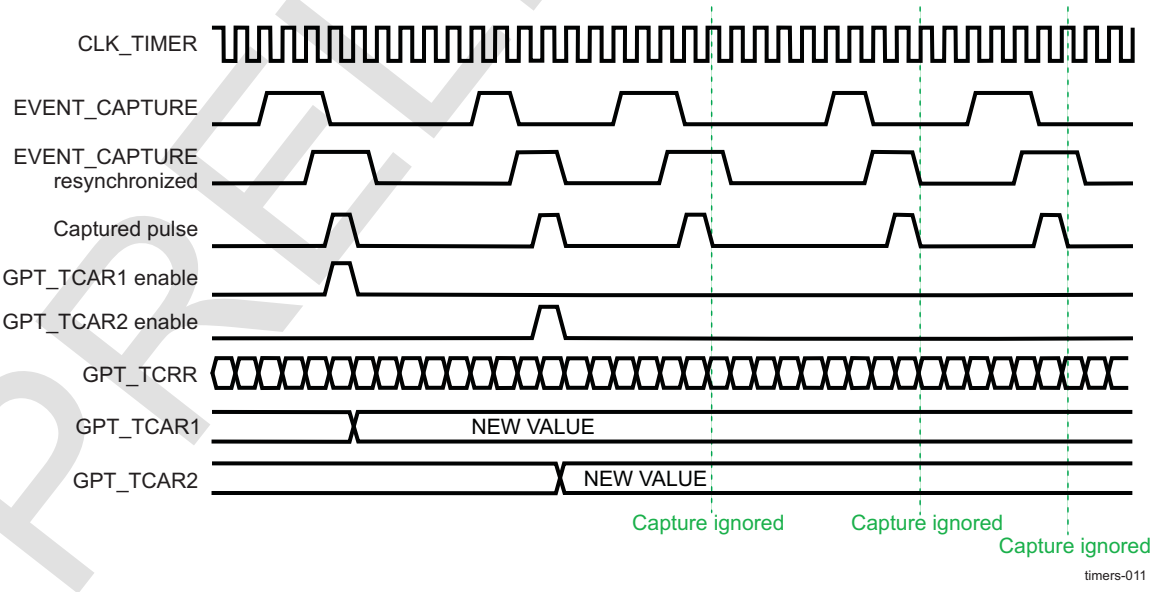
In Figure 22-11, the GPT_TCLR[9:8] TCM bit field value is 0b01, and GPT_TCLR[13] CAPT_MODE bit is 0. Only the rising edge of EVENT_CAPTURE triggers a capture in the GPT_TCAR1 and GPT_TCAR2 registers, and only the GPT_TCAR1 register updates.

Figure 22-11. Capture Wave Example for GPT_TCLR[13] CAPT_MODE = 0



In Figure 22-12, the value of the GPT_TCLR[9:8] TCM bit field is 0b01, and the GPT_TCLR[13] CAPT_MODE bit is 1. Only the rising edge of EVENT_CAPTURE triggers a capture in the GPT_TCAR1 register on the first enabled event, and the GPT_TCAR2 register updates on the second enabled event.

Figure 22-12. Capture Wave Example for GPT_TCLR[13] CAPT_MODE = 1



22.2.4.8 Compare Mode Functionality

When compare enable-register GPT_TCLR[6] CE bit is set to 1, the timer value (GPT_TCRR[31:0]

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TIMER_COUNTER bit field) is continuously compared to the value held in the timer match register (GPT_TMAR). The GPT_TMAR[31:0] COMPARE_VALUE bit field value can be loaded at any time (timer counting or stopped). When the GPT_TCRR and the GPT_TMAR values match, an interrupt is issued, if the GPT_TIER[0] MAT_IT_ENA (for GPTIMER1, GPTIMER2, and GPTIMER10), or GPT_IRQSTATUS_SET[0] MAT_EN_FLAG bit (for other timers) is set.

The right programming way is to write a compare value to the GPT_TMAR register before setting the GPT_TCLR[6] CE bit to prevent any unwanted interrupts due to a reset value matching effect.

The dedicated output pin (timer PWM) can be programmed in the GPT_TCLR[12] PT bit through the GPT_TCLR[11:10] TRG bit field to generate one positive pulse (timer clock duration) or to invert the current value (toggle mode) when an overflow or a match occurs.

22.2.4.9 Prescaler Functionality

A prescaler can be used to divide the timer counter input clock frequency. The prescaler is enabled when the GPT_TCLR[5] PRE bit is set. The GPT_TCLR[4:2] PTV bit field sets the second prescaler ratio. The prescaler counter is reset when the timer counter is stopped or reloaded on-the-fly.

Table 22-9 lists the prescaler/timer reload values versus contexts.

Table 22-9. Prescaler/Timer Reload Values Versus Contexts

Context	Prescaler	Timer Counter
Overflow (when autoreload is on)	Reset	GPT_TLDR[31:0]
GPT_TCRR write	Reset	GPT_TCRR[31:0]
GPT_TTGR write	Reset	GPT_TLDR[31:0]
Stop	Reset	Frozen

22.2.4.10 Pulse-Width Modulation

The timer can be configured to provide a programmable PWM output. The timer PWM output pin can be configured to toggle on an event. The GPT_TCLR[11:10] TRG bit field determines on which register value the PWM pin toggles. Either overflow alone or both overflow and match can be selected to toggle the timer PWM pin when a compare condition occurs.

CAUTION

In toggle mode, when GPT_TCLR[11:10] TRG = 0x2 (overflow and match), the first event that toggles the PWM line is an overflow event. If a match event occurs first; it does not toggle the PWM line (see Figure 22-14).

The GPT_TCLR[7] SCPWM bit can be programmed to set or clear the timer PWM output signal only while the counter is stopped or the trigger is off. This allows setting the output pin to a known state before modulation starts. Modulation synchronously stops when the GPT_TCLR[11:10] TRG bit field is cleared and overflow occurs. This allows fixing a deterministic state of the output pin when modulation stops.

In Figure 22-13, the internal overflow pulse is set each time (0xFFFF FFFF - GPT_TLDR[31:0] LOAD_VALUE + 1) the value is reached, and the internal match pulse is set when the counter reaches the GPT_TMAR register value. Depending on the value of the GPT_TCLR[12] PT bit and GPT_TCLR[11:10] TRG bit field, the timer provides pulse or PWM event on the output pin (timer PWM).

The GPT_TLDR and GPT_TMAR registers must keep values below the overflow value (0xFFFF FFFF) by at least two units. In case the PWM trigger events are both overflow and match, the difference between the values kept in the GPT_TMAR register and the value in theGPT_TLDR register must be at least two units. When match event is used, the compare mode GPT_TCLR[6] CE bit must be set.

In Figure 22-13, the GPT_TCLR[7] SCPWM bit is set to 0. In Figure 22-14, the GPT_TCLR[7] SCPWM bit is set to 1. To obtain the desired wave form, start the counter at 0xFFFF FFFE value (to ensure an overflow first) or adjust the line polarity (GPT_TCLR[7] SCPWM bit).

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Figure 22-13. Timing Diagram of PWM With GPT_TCLR[7] SCPWM Bit = 0

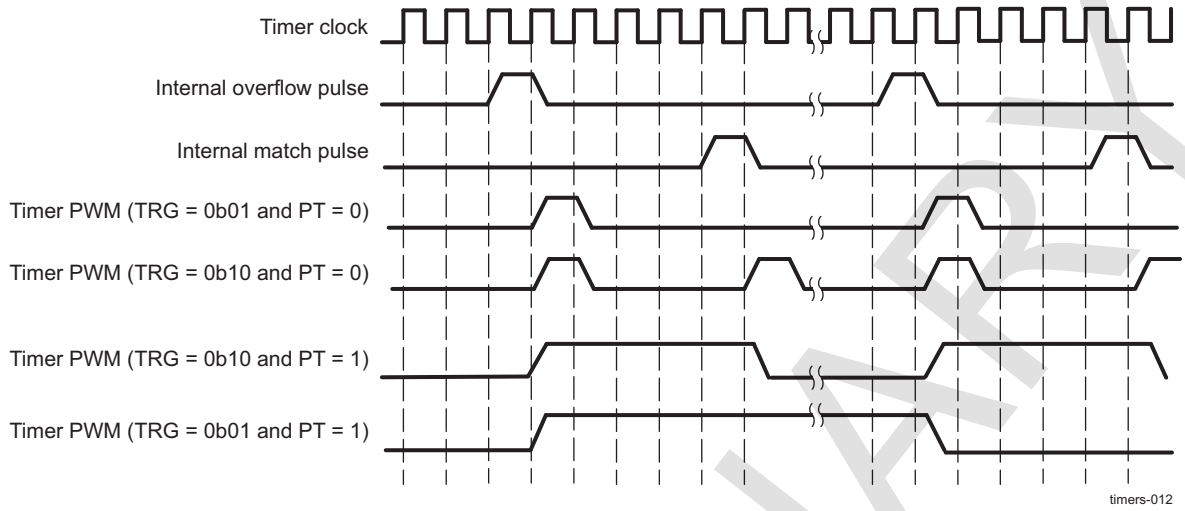
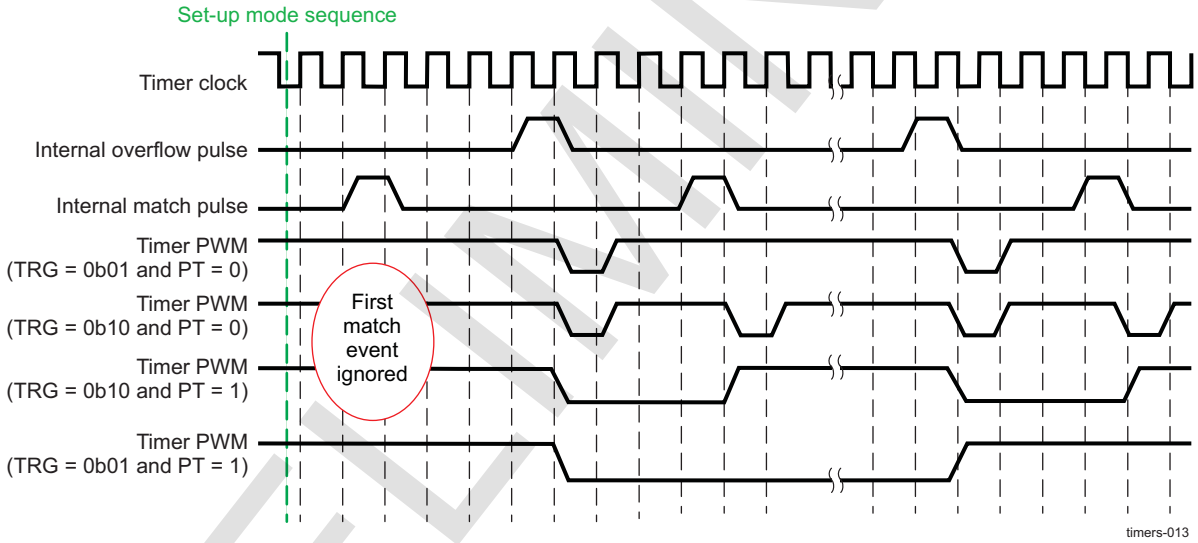


Figure 22-14. Timing Diagram of PWM With GPT_TCLR[7] SCPWM Bit = 1



22.2.4.11 Timer Counting Rate

The timer rate is defined by the following values:

- Value of the prescaler fields (the GPT_TCLR[5] PRE bit and the GPT_TCLR[4:2] PTV bit field)
- Value loaded into the timer-load register (GPT_TLDR)

Table 22-10 lists the prescaler clock ratio values.

Table 22-10. Prescaler Clock Ratio Values

GPT_TCLR[5] PRE	GPT_TCLR[4:2] PTV	Divisor (PS)
0	X	1
1	0	2
1	1	4
1	2	8
1	3	16
1	4	32

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Table 22-10. Prescaler Clock Ratio Values (continued)

GPT_TCLR[5] PRE	GPT_TCLR[4:2] PTV	Divisor (PS)
1	5	64
1	6	128
1	7	256

Thus, the timer overflow rate is expressed as:

OVF_Rate = (0xFFFF FFFF – GPT_TLDR + 1) * (timer-functional clock period) * PS

With (timer-functional clock period) = 1/(timer-functional clock frequency) and PS = $2^{(PTV + 1)}$ if prescaler is enabled, or PS = 1 if prescaler is disabled.

CAUTION

Internal resynchronization causes any write to the GPT_TCLR[1] ST bit to have some latency before the register is updated:

2.5 * functional clock cycles write_GPT_TCLR_latency 3.5 * functional clock cycles

Remember to consider this latency whenever the timer must be started or stopped by a software change to the GPT_TCLR[1] ST bit.

CAUTION

- In the non-PWM mode, GPT_TLDR must be maintained at less than or equal to 0xFFFF FFFE.
- In the PWM mode, GPT_TLDR must be maintained at less than or equal to 0xFFFF FFFD.

For example, with a timer clock input of 32 kHz and the GPT_TCLR[5] PRE bit set to 0, the timer output period is as listed in Table 22-11.

Table 22-11. Value and Corresponding Interrupt Period

GPT_TLDR[31:0] LOAD_VALUE	Interrupt Period
0x0000 0000	39 h
0xFFFF 0000	2.1 s
0xFFFF FFF0	524 µs
0xFFFF FFFE	65.5 µs

22.2.4.12 Timer Under Emulation

During emulation mode, the timer continues to run according to the value of the GPT1MS_TIOCP_CFG[5]/GPT_TIOCP_CFG[1] EMUFREE bit.

If the GPT1MS_TIOCP_CFG[5]/GPT_TIOCP_CFG[1] EMUFREE bit is set to 1, timer execution is not stopped in emulation mode and the interrupt is still generated when overflow or match is reached.

If the GPT1MS_TIOCP_CFG[5]/GPT_TIOCP_CFG[1] EMUFREE bit is set to 0, the prescaler and timer are frozen and both resume on exit from emulation mode. The asynchronous external input pin (dmtimer_i_pwm_evt, with i=[8:11]) is internally synchronized on two timer-clock rising edges.

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22.2.4.13 Accessing GP Timer Registers

All accesses are nonposted until software reconfiguration. All registers are 32 bits wide, accessible through the L4 interface with 16-bit or 32-bit access (read/write).

Any 16-bit write access must be least-significant bit (LSB) first, and the second write access must be most-significant bit (MSB) first. Write operations to the following GP timer registers can skip the MSB access if it is not necessary to update the 16 MSBs of the register:

- GPT_TIDR
- GPT_TIOCP_CFG
- GPT1MS_TIOCP_CFG
- GPT_IRQSTATUS_RAW
- GPT_IRQSTATUS
- GPT_IRQENABLE_SET
- GPT_IRQENABLE_CLR
- GPT_IRQWAKEEN
- GPT_TISR
- GPT_TIER
- GPT_TWER
- GPT_TSICR

Write operations to the following functional registers must be complete (the MSB must be written even if the MSB data is not used):

- GPT_TCLR
- GPT_TCRR
- GPT_TLDR
- GPT_TTGR
- GPT_TMAR
- GPT_TPIR
- GPT_TNIR
- GPT_TCVR
- GPT_TOCR
- GPT_TOWR

The following L4 synchronous registers are not affected by the posted/nonposted mode selection; the write/read operation is effective and acknowledged (command accepted) after one L4 clock cycle from command assertion:

- GPT_TIDR
- GPT_TIOCP_CFG
- GPT1MS_TIOCP_CFG
- GPT_TISTAT
- GPT_IRQSTATUS
- GPT_IRQSTATUS_RAW
- GPT_IRQENABLE_SET
- GPT_IRQENABLE_CLR
- GPT_IRQWAKEEN
- GPT_TWPS
- GPT_TSICR

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22.2.4.13.1 Writing to Timer Registers

The host uses the L4 interface to write to the following registers synchronously with the timer interface clock:

- GPT_TLDR
- GPT_TCRR
- GPT_TCLR
- GPT_TIOCP_CFG
- GPT1MS_TIOCP_CFG
- GPT_IRQSTATUS
- GPT_IRQENABLE_SET
- GPT_IRQENABLE_CLR
- GPT_IRQWAKEEN
- GPT_TTGR
- GPT_TSICR
- GPT_TMAR

GPTIMER1, GPTIMER2, and GPTIMER10 also have the following registers:

- GPT_TPIR
- GPT_TNIR
- GPT_TCVR
- GPT_TOCR
- GPT_TOWR
- GPT_TIER
- GPT_TISR
- GPT_TWER

In 16-bit access mode, the 16 LSBs must be written before writing to the 16 MSBs.

22.2.4.13.1.1 Write Posting Synchronization Mode

This mode is used if the GPT_TSICR[2] POSTED bit is set to 1.

This mode uses a posted write scheme to update any internal register (GPT_TCLR, GPT_TCRR, GPT_TLDR, GPT_TTGR, GPT_TMAR, and GPT_TPIR, GPT_TNIR, GPT_TCVR, GPT_TOCR, and GPT_TOWR for GPTIMER1, GPTIMER2, and GPTIMER10). Therefore, the write transaction is immediately acknowledged on the L4 interface, although the effective write operation occurs later due to a resynchronization in the timer clock domain. The advantage is that neither the interconnect nor the device that requested the write transaction are stalled.

For each register, a status bit is provided in the timer write-posted status register GPT_TWPS. In this mode, it is mandatory that the software checks this status bit prior to any write access. In case a write is attempted to a register with a previous access pending, the previous access is discarded without notice.

The timer module updates the timer counter register value synchronously with the L4 clock. Consequently, any read access to the timer counter register GPT_TCRR does not add any resynchronization latency; the current value is always available.

NOTE: Since the overflow IRQ is generated, when the TCRR value reaches 0xFFFF FFFF, and not when it changes its value to the value after overflow, one must wait a delay of (1 * PS * timer-functional clock period) before any read access to the timer counter register GPT_TCRR to ensure a correct reading of its content.

If a write access is pending for a register, reading from this register does not yield a correct result. Software synchronization must be used to avoid incorrect results.

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The drawback of this automatic update mechanism is that it assumes a given relationship between the timer interface frequency and the timer clock frequency.

Functional frequency range: freq(timer clock) < freq(L4 interface clock)/4.

22.2.4.13.1.2 Write Nonposting Synchronization Mode

This mode is used if the GPT_TSICR[2] POSTED bit is set to 0. It uses a nonposted write scheme to update any internal register. Therefore, the write transaction is not acknowledged on the L4 interface until the effective write operation occurs after the resynchronization in the timer functional clock domain. The drawback is that both the interconnect and the device that requested the write transaction are stalled during this period.

The same full resynchronization scheme is used for a read transaction, and the same stall period applies. A register read following a write to the same register is always coherent.

This mode is functional regardless of the ratio between the L4 interface frequency and the timer clock frequency.

22.2.4.13.2 Reading From Timer Counter Registers

In 16-bit access mode, reading the 16 LSBs from the timer counter registers (GPT_TCRR, GPT_TCAR1, and GPT_TCAR2) captures the current timer counter value. This must be followed by reading the 16 MSBs.

IVA3 subsystem 16-bit accesses can be interleaved with MPU subsystem 32-bit accesses.

NOTE: LSB/MSB accesses cannot be interleaved (that is, the sequence LSB register 1, LSB register 2, MSB register 1, MSB register 2 is not supported).

22.2.5 GP Timer Low-Level Programming Models

This section covers the low-level hardware programming sequences for configuration and usage of the module.

22.2.5.1 Global Initialization

22.2.5.1.1 Global Initialization of Surrounding Modules

This section identifies the requirements for initializing the surrounding modules when the GP timer module is to be used for the first time after a device reset. This initialization of surrounding modules is based on the integration and environment of the GP timer. For more information, see Section 22.2.3 *GP Timers Integration* and Section 22.2.2, *GP Timers Environment*.

Table 22-12. Global Initialization of Surrounding Modules

Surrounding Modules	Comments
PRCM	The module interface and functional clocks must be enabled. For more information about the module configuration, see Section 3.1.1.1.2, *Module Level Clock Management*, in Chapter 3, *Power, Reset, and Clock Management*.
Control Module	The module specific pad muxing must be set in the control module. For more information about the module configuration, see Section 18.4.8 *PAD Functional Multiplexing and Configuration,* in Chapter 18, *Control Module*.
MPU INTC	The MPU INTC configuration must be done to enable the interrupts from the GP timer module. See Section 4.4.3, *Interrupt Controller Registers*, in Section 4.4.3, *Cortex-A9 MPU Subsystem*.
DSP INTC	The DSP INTC configuration must be done to enable the interrupts from GP timer module. See , *INTC,* in Chapter 5, *DSP Subsystem*.

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22.2.5.1.2 GP Timer Module Global Initialization

22.2.5.1.2.1 Main Sequence – GP Timer Module Global Initialization

This section identifies the main steps for initializing the GP timer module when the module is to be used for the first time.

Table 22-13. GP Timer Module Global Initialization

Step	Register/Bit Field/Programming Model	Value
Execute software reset.	GPT_TIOCP_CFG[0]SOFTRESET(1) or GPT1MS_TIOCP_CFG[0] SOFTRESET(2)	0x1
Wait until reset release?	GPT_TIOCP_CFG[0] SOFTRESET(1) or GPT1MS_TIOCP_CFG[0] SOFTRESET(2)	0x0
Configure Idle mode.	GPT_TIOCP_CFG[3:2] IDLEMODE(1) or GPT1MS_TIOCP_CFG[4:3] IDLEMODE(2)	xx
Configure clock activity.	GPT1MS_TIOCP_CFG[9:8] CLOCKACTIVITY(2)	xx
Configure wake-up feature.	GPT1MS_TIOCP_CFG[2] ENAWAKEUP(2)	x
Enable wake-up interrupt events.	GPT_IRQWAKEEN[2:0](1) or GPT_TWER[2:0](2)	x
Select posted mode.	GPT_TSICR[2] POSTED	x

(1) Applies only to GPTIMER3 through GPTIMER9, and GPTIMER11
(2) Applies only to GPTIMER1, GPTIMER2, and GPTIMER10

22.2.5.2 Operational Mode Configuration

22.2.5.2.1 GP Timer Mode

22.2.5.2.1.1 Main Sequence – GP Timer Mode Configuration

Table 22-14. GP Timer Mode Configuration

Step	Register/Bit Field/Programming Model	Value
Select autoreload mode	GPT_TCLR[1] AR	x
Set prescale timer value.	GPT_TCLR[4:2] PTV	xxx
Enable prescaler.	GPT_TCLR[5] PRE	0x1
Enable overflow interrupt.	GPT_TIER[1] OVF_IT_ENA(1) or GPT_IRQENABLE_SET[1] OVF_EN_FLAG(2)	0x1
Load timer counter value.	GPT_TCRR	xxx
Load timer load value.	GPT_TLDR	xxx
Start the timer.	GPT_TCLR[0] ST	0x1

(1) Applies only to GPTIMER1, GPTIMER2, and GPTIMER10.
(2) Applies only to GPTIMER3 through GPTIMER 9, and GPTIMER11.

22.2.5.2.2 GP Timer Compare Mode

22.2.5.2.2.1 Main Sequence – GP Timer Compare Mode Configuration

Table 22-15. GP Timer Compare Mode Configuration

Step	Register/Bit Field/Programming Model	Value
Select autoreload mode.	GPT_TCLR[1] AR	x
Set prescale timer value.	GPT_TCLR[4:2] PTV	xxx
Enable prescaler.	GPT_TCLR[5] PRE	0x1

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Table 22-15. GP Timer Compare Mode Configuration (continued)

Step	Register/Bit Field/Programming Model	Value
Enable match interrupt.	GPT_TIER[0] MAT_IT_ENA[1] or GPT_IRQENABLE_SET[0] MAT_EN_FLAG[2]	0x1
Load timer counter value.	GPT_TCRR	xxx
Load timer compare value.	GPT_TMAR	xxx
Enable Compare mode.	GPT_TCLR[6] CE	0x1
Start the timer.	GPT_TCLR[0] ST	0x1

(1) Applies only to GPTIMER1, GPTIMER2, and GPTIMER10.
(2) Applies only to GPTIMER3 through GPTIMER9, and GPTIMER11.

22.2.5.2.3 GP Timer Capture Mode

22.2.5.2.3.1 Main Sequence – GP Timer Capture Mode Configuration

Table 22-16. GP Timer Capture Mode Configuration

Step	Register/Bit Field/Programming Model	Value
Initialize capture mode.	See Section 22.2.5.2.3.2.	
Enable capture interrupt.	GPT_TIER[2] TCAR_IT_ENA[1] or GPT_IRQENABLE_SET[2] TCAR_EN_FLAG[2]	0x1
Start the timer.	GPT_TCLR[0] ST	0x1
Detect event.	SeeSection 22.2.5.2.3.3.	

(1) Applies only to GPTIMER1, GPTIMER2, and GPTIMER10.
(2) Applies only to GPTIMER3 through GPTIMER9, and GPTIMER11.

22.2.5.2.3.2 Subsequence – Initialize Capture Mode

Table 22-17. Initialize Capture Mode

Step	Register/Bit Field/Programming Model	Value
Select autoreload mode.	GPT_TCLR[1] AR	x
Set prescale timer value.	GPT_TCLR[4:2] PTV	xxx
Enable prescaler.	GPT_TCLR[5] PRE	0x1
Select GPTx (where x = 8 to 11). Capture input at device pin dmtimerx_pwm_evt.	GPT_TCLR[14] GPO_CFG[1]	0x1
Select single or second event capture.	GPT_TCLR[13] CAPT_MODE	x
Select transition capture mode.	GPT_TCLR[9:8] TCM	xx

(1) Applies only to GPTIMER8 through GPTIMER11

22.2.5.2.3.3 Subsequence – Detect Event

Table 22-18. Detect Event

Step	Register/Bit Field/Programming Model	Value
Wait until event detected?	GPT_TISR[2] TCAR_IT_FLAG[1] or GPT_IRQSTATUS[2] TCAR_IT_FLAG[2]	= 0x1
Read Timer capture value.	GPT_TCAR1 and/or GPT_TCAR2	

(1) Applies only to GPTIMER1, GPTIMER2, and GPTIMER10.
(2) Applies only to GPTIMER3 through GPTIMER9, and GPTIMER11.

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Table 22-18. Detect Event (continued)

Step	Register/Bit Field/Programming Model	Value
Clear capture interrupt request.	GPT_TISR[2] TCAR_IT_FLAG(1) or GPT_IRQSTATUS[2] TCAR_IT_FLAG(2)	0x1

22.2.5.2.4 GP Timer PWM Mode

22.2.5.2.4.1 Main Sequence – GP Timer PWM Mode Configuration

Table 22-19. GP Timer PWM Mode Configuration

Step	Register/Bit Field/Programming Model	Value
Select autoreload mode.	GPT_TCLR[1] AR	x
Set prescale timer value.	GPT_TCLR[4:2] PTV	xxx
Enable prescaler.	GPT_TCLR[5] PRE	0x1
Select trigger output mode.	GPT_TCLR[11:10]TRG	xx
Select pulse or toggle modulation PWM mode.	GPT_TCLR[12] PT	x
Select GPTx (where x = 8 to 11) pwm output at device pin dmtimerx_pwm_evt.	GPT_TCLR[14] GPO_CFG(1)	0x0
Configure PWM output pin default value.	GPT_TCLR[7] SCPWM	x
Load timer load value.	GPT_TLDR	xxx
Load timer compare value.	GPT_TMAR	xxx
Enable compare.	GPT_TCLR[6] CE	0x1
Start the timer.	GPT_TCLR[0] ST	0x1

(1) Applies only to GPTIMER8 through GPTIMER11

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22.2.6 GP Timer Register Manual

22.2.6.1 GP Timer Instance Summary

Table 22-20 lists the base address and block size for the GP timer module instances.

Table 22-20. GP Timer Instance Summary

Module Name	Base Address L4 Interconnect	Base Address L3 Interconnect	Base Address Cortex-A9 Private Access	Base Address DSP Private Access	Size
GPTIMER2	0x4803 2000	-	-	-	4 KB
GPTIMER3	0x4803 4000	-	-	-	4 KB
GPTIMER4	0x4803 6000	-	-	-	4 KB
GPTIMER9	0x4803 E000	-	-	-	4 KB
GPTIMER10	0x4808 6000	-	-	-	4 KB
GPTIMER11	0x4808 8000	-	-	-	4 KB
GPTIMER5	-	0x4903 8000	0x4013 8000	0x01D3 8000	4 KB
GPTIMER6	-	0x4903 A000	0x4013 A000	0x01D3 A000	4 KB
GPTIMER7	-	0x4903 C000	0x4013 C000	0x01D3 C000	4 KB
GPTIMER8	-	0x4903 E000	0x4013 E000	0x01D3 E000	4 KB
GPTIMER1	0x4A31 8000	-	-	-	4 KB

NOTE: Private Access is an access which is not using the L3/L4 interconnects.

22.2.6.2 GP Timer Registers

22.2.6.2.1 GP Timer Register Summary

CAUTION

The GP timer registers are limited to 32-bit and 16-bit data accesses; 8-bit access is not allowed and can corrupt the register content.

Table 22-21 through Table 22-27 provide the register summary and associated offset addresses for the 11 GP timer internal registers.

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Table 22-21. GPTIMER1, GPTIMER2, and GPTIMER10 Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	GPTIMER1 Physical Address L4 Interconnect	GPTIMER2 Physical Address L4 Interconnect	GPTIMER10 Physical Address L4 Interconnect
GPT_TIDR	R	32	0x0000 0000	0x4A31 8000	0x4803 2000	0x4808 6000
GPT1MS_TIOCP_CFG	RW	32	0x0000 0010	0x4A31 8010	0x4803 2010	0x4808 6010
GPT_TISTAT	R	32	0x0000 0014	0x4A31 8014	0x4803 2014	0x4808 6014
GPT_TISR	RW	32	0x0000 0018	0x4A31 8018	0x4803 2018	0x4808 6018
GPT_TIER	RW	32	0x0000 001C	0x4A31 801C	0x4803 201C	0x4808 601C
GPT_TWER	RW	32	0x0000 0020	0x4A31 8020	0x4803 2020	0x4808 6020
GPT_TCLR	RW	32	0x0000 0024	0x4A31 8024	0x4803 2024	0x4808 6024
GPT_TCRR	RW	32	0x0000 0028	0x4A31 8028	0x4803 2028	0x4808 6028
GPT_TLDR	RW	32	0x0000 002C	0x4A31 802C	0x4803 202C	0x4808 602C
GPT_TTGR	RW	32	0x0000 0030	0x4A31 8030	0x4803 2030	0x4808 6030
GPT_TWPS	R	32	0x0000 0034	0x4A31 8034	0x4803 2034	0x4808 6034
GPT_TMAR	RW	32	0x0000 0038	0x4A31 8038	0x4803 2038	0x4808 6038
GPT_TCAR1	R	32	0x0000 003C	0x4A31 803C	0x4803 203C	0x4808 603C
GPT_TSICR	RW	32	0x0000 0040	0x4A31 8040	0x4803 2040	0x4808 6040
GPT_TCAR2	R	32	0x0000 0044	0x4A31 8044	0x4803 2044	0x4808 6044
GPT_TPIR	RW	32	0x0000 0048	0x4A31 8048	0x4803 2048	0x4808 6048
GPT_TNIR	RW	32	0x0000 004C	0x4A31 804C	0x4803 204C	0x4808 604C
GPT_TCVR	RW	32	0x0000 0050	0x4A31 8050	0x4803 2050	0x4808 6050
GPT_TOCR	RW	32	0x0000 0054	0x4A31 8054	0x4803 2054	0x4808 6054
GPT_TOWR	RW	32	0x0000 0058	0x4A31 8058	0x4803 2058	0x4808 6058

Table 22-22. GPTIMER3 and GPTIMER4 Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	GPTIMER3 Physical Address L4 Interconnect	GPTIMER4 Physical Address L4 Interconnect
GPT_TIDR	R	32	0x0000 0000	0x4803 4000	0x4803 6000
GPT_TIOCP_CFG	RW	32	0x0000 0010	0x4803 4010	0x4803 6010
RESERVED			0x0000 0020	0x4803 4020	0x4803 6020
GPT_IRQSTATUS_RAW	RW	32	0x0000 0024	0x4803 4024	0x4803 6024
GPT_IRQSTATUS	RW	32	0x0000 0028	0x4803 4028	0x4803 6028
GPT_IRQENABLE_SET	RW	32	0x0000 002C	0x4803 402C	0x4803 602C
GPT_IRQENABLE_CLR	RW	32	0x0000 0030	0x4803 4030	0x4803 6030
GPT_IRQWAKEEN	RW	32	0x0000 0034	0x4803 4034	0x4803 6034
GPT_TCLR	RW	32	0x0000 0038	0x4803 4038	0x4803 6038
GPT_TCRR	RW	32	0x0000 003C	0x4803 403C	0x4803 603C
GPT_TLDR	RW	32	0x0000 0040	0x4803 4040	0x4803 6040
GPT_TTGR	RW	32	0x0000 0044	0x4803 4044	0x4803 6044
GPT_TWPS	R	32	0x0000 0048	0x4803 4048	0x4803 6048
GPT_TMAR	RW	32	0x0000 004C	0x4803 404C	0x4803 604C
GPT_TCAR1	R	32	0x0000 0050	0x4803 4050	0x4803 6050
GPT_TSICR	RW	32	0x0000 0054	0x4803 4054	0x4803 6054
GPT_TCAR2	R	32	0x0000 0058	0x4803 4058	0x4803 6058

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Table 22-23. GPTIMER5 Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	GPTIMER5 Physical Address L3 Interconnect	GPTIMER5 Physical Address Cortex-A9 Private Access	GPTIMER5 Physical Address DSP Private Access
GPT_TIDR	R	32	0x0000 0000	0x4903 8000	0x4013 8000	0x01D3 8000
GPT_TIOCP_CFG	RW	32	0x0000 0010	0x4903 8010	0x4013 8010	0x01D3 8010
RESERVED			0x0000 0020	0x4903 8020	0x4013 8020	0x01D3 8020
GPT_IRQSTATUS_RAW	RW	32	0x0000 0024	0x4903 8024	0x4013 8024	0x01D3 8024
GPT_IRQSTATUS	RW	32	0x0000 0028	0x4903 8028	0x4013 8028	0x01D3 8028
GPT_IRQENABLE_SET	RW	32	0x0000 002C	0x4903 802C	0x4013 802C	0x01D3 802C
GPT_IRQENABLE_CLR	RW	32	0x0000 0030	0x4903 8030	0x4013 8030	0x01D3 8030
GPT_IRQWAKEEN	RW	32	0x0000 0034	0x4903 8034	0x4013 8034	0x01D3 8034
GPT_TCLR	RW	32	0x0000 0038	0x4903 8038	0x4013 8038	0x01D3 8038
GPT_TCRR	RW	32	0x0000 003C	0x4903 803C	0x4013 803C	0x01D3 803C
GPT_TLDR	RW	32	0x0000 0040	0x4903 8040	0x4013 8040	0x01D3 8040
GPT_TTGR	RW	32	0x0000 0044	0x4903 8044	0x4013 8044	0x01D3 8044
GPT_TWPS	R	32	0x0000 0048	0x4903 8048	0x4013 8048	0x01D3 8048
GPT_TMAR	RW	32	0x0000 004C	0x4903 804C	0x4013 804C	0x01D3 804C
GPT_TCAR1	R	32	0x0000 0050	0x4903 8050	0x4013 8050	0x01D3 8050
GPT_TSICR	RW	32	0x0000 0054	0x4903 8054	0x4013 8054	0x01D3 8054
GPT_TCAR2	R	32	0x0000 0058	0x4903 8058	0x4013 8058	0x01D3 8058

Table 22-24. GPTIMER6 Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	GPTIMER6 Physical Address L3 Interconnect	GPTIMER6 Physical Address Cortex-A9 Private Access	GPTIMER6 Physical Address DSP Private Access
GPT_TIDR	R	32	0x0000 0000	0x4903 A000	0x4013 A000	0x01D3 A000
GPT_TIOCP_CFG	RW	32	0x0000 0010	0x4903 A010	0x4013 A010	0x01D3 A010
RESERVED			0x0000 0020	0x4903 A020	0x4013 A020	0x01D3 A020
GPT_IRQSTATUS_RAW	RW	32	0x0000 0024	0x4903 A024	0x4013 A024	0x01D3 A024
GPT_IRQSTATUS	RW	32	0x0000 0028	0x4903 A028	0x4013 A028	0x01D3 A028
GPT_IRQENABLE_SET	RW	32	0x0000 002C	0x4903 A02C	0x4013 A02C	0x01D3 A02C
GPT_IRQENABLE_CLR	RW	32	0x0000 0030	0x4903 A030	0x4013 A030	0x01D3 A030
GPT_IRQWAKEEN	RW	32	0x0000 0034	0x4903 A034	0x4013 A034	0x01D3 A034
GPT_TCLR	RW	32	0x0000 0038	0x4903 A038	0x4013 A038	0x01D3 A038
GPT_TCRR	RW	32	0x0000 003C	0x4903 A03C	0x4013 A03C	0x01D3 A03C
GPT_TLDR	RW	32	0x0000 0040	0x4903 A040	0x4013 A040	0x01D3 A040
GPT_TTGR	RW	32	0x0000 0044	0x4903 A044	0x4013 A044	0x01D3 A044
GPT_TWPS	R	32	0x0000 0048	0x4903 A048	0x4013 A048	0x01D3 A048
GPT_TMAR	RW	32	0x0000 004C	0x4903 A04C	0x4013 A04C	0x01D3 A04C
GPT_TCAR1	R	32	0x0000 0050	0x4903 A050	0x4013 A050	0x01D3 A050
GPT_TSICR	RW	32	0x0000 0054	0x4903 A054	0x4013 A054	0x01D3 A054
GPT_TCAR2	R	32	0x0000 0058	0x4903 A058	0x4013 A058	0x01D3 A058

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Table 22-25. GPTIMER7 Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	GPTIMER7 Physical Address L3 Interconnect	GPTIMER7 Physical Address Cortex-A9 Private Access	GPTIMER7 Physical Address DSP Private Access
GPT_TIDR	R	32	0x0000 0000	0x4903 C000	0x4013 C000	0x01D3 C000
GPT_TIOCP_CFG	RW	32	0x0000 0010	0x4903 C010	0x4013 C010	0x01D3 C010
RESERVED			0x0000 0020	0x4903 C020	0x4013 C020	0x01D3 C020
GPT_IRQSTATUS_RAW	RW	32	0x0000 0024	0x4903 C024	0x4013 C024	0x01D3 C024
GPT_IRQSTATUS	RW	32	0x0000 0028	0x4903 C028	0x4013 C028	0x01D3 C028
GPT_IRQENABLE_SET	RW	32	0x0000 002C	0x4903 C02C	0x4013 C02C	0x01D3 C02C
GPT_IRQENABLE_CLR	RW	32	0x0000 0030	0x4903 C030	0x4013 C030	0x01D3 C030
GPT_IRQWAKEEN	RW	32	0x0000 0034	0x4903 C034	0x4013 C034	0x01D3 C034
GPT_TCLR	RW	32	0x0000 0038	0x4903 C038	0x4013 C038	0x01D3 C038
GPT_TCRR	RW	32	0x0000 003C	0x4903 C03C	0x4013 C03C	0x01D3 C03C
GPT_TLDR	RW	32	0x0000 0040	0x4903 C040	0x4013 C040	0x01D3 C040
GPT_TTGR	RW	32	0x0000 0044	0x4903 C044	0x4013 C044	0x01D3 C044
GPT_TWPS	R	32	0x0000 0048	0x4903 C048	0x4013 C048	0x01D3 C048
GPT_TMAR	RW	32	0x0000 004C	0x4903 C04C	0x4013 C04C	0x01D3 C04C
GPT_TCAR1	R	32	0x0000 0050	0x4903 C050	0x4013 C050	0x01D3 C050
GPT_TSICR	RW	32	0x0000 0054	0x4903 C054	0x4013 C054	0x01D3 C054
GPT_TCAR2	R	32	0x0000 0058	0x4903 C058	0x4013 C058	0x01D3 C058

Table 22-26. GPTIMER8 Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	GPTIMER8 Physical Address L3 Interconnect	GPTIMER8 Physical Address Cortex-A9 Private Access	GPTIMER8 Physical Address DSP Private Access
GPT_TIDR	R	32	0x0000 0000	0x4903 E000	0x4013 E000	0x01D3 E000
GPT_TIOCP_CFG	RW	32	0x0000 0010	0x4903 E010	0x4013 E010	0x01D3 E010
RESERVED			0x0000 0020	0x4903 E020	0x4013 E020	0x01D3 E020
GPT_IRQSTATUS_RAW	RW	32	0x0000 0024	0x4903 E024	0x4013 E024	0x01D3 E024
GPT_IRQSTATUS	RW	32	0x0000 0028	0x4903 E028	0x4013 E028	0x01D3 E028
GPT_IRQENABLE_SET	RW	32	0x0000 002C	0x4903 E02C	0x4013 E02C	0x01D3 E02C
GPT_IRQENABLE_CLR	RW	32	0x0000 0030	0x4903 E030	0x4013 E030	0x01D3 E030
GPT_IRQWAKEEN	RW	32	0x0000 0034	0x4903 E034	0x4013 E034	0x01D3 E034
GPT_TCLR	RW	32	0x0000 0038	0x4903 E038	0x4013 E038	0x01D3 E038
GPT_TCRR	RW	32	0x0000 003C	0x4903 E03C	0x4013 E03C	0x01D3 E03C
GPT_TLDR	RW	32	0x0000 0040	0x4903 E040	0x4013 E040	0x01D3 E040
GPT_TTGR	RW	32	0x0000 0044	0x4903 E044	0x4013 E044	0x01D3 E044
GPT_TWPS	R	32	0x0000 0048	0x4903 E048	0x4013 E048	0x01D3 E048
GPT_TMAR	RW	32	0x0000 004C	0x4903 E04C	0x4013 E04C	0x01D3 E04C
GPT_TCAR1	R	32	0x0000 0050	0x4903 E050	0x4013 E050	0x01D3 E050
GPT_TSICR	RW	32	0x0000 0054	0x4903 E054	0x4013 E054	0x01D3 E054
GPT_TCAR2	R	32	0x0000 0058	0x4903 E058	0x4013 E058	0x01D3 E058

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Table 22-27. GPTIMER9 and GPTIMER11 Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	GPTIMER9 Physical Address L4 Interconnect	GPTIMER11 Physical Address L4 Interconnect
GPT_TIDR	R	32	0x0000 0000	0x4803 E000	0x4808 8000
GPT_TIOCP_CFG	RW	32	0x0000 0010	0x4803 E010	0x4808 8010
RESERVED			0x0000 0020	0x4803 E020	0x4808 8020
GPT_IRQSTATUS_RAW	RW	32	0x0000 0024	0x4803 E024	0x4808 8024
GPT_IRQSTATUS	RW	32	0x0000 0028	0x4803 E028	0x4808 8028
GPT_IRQENABLE_SET	RW	32	0x0000 002C	0x4803 E02C	0x4808 802C
GPT_IRQENABLE_CLR	RW	32	0x0000 0030	0x4803 E030	0x4808 8030
GPT_IRQWAKEEN	RW	32	0x0000 0034	0x4803 E034	0x4808 8034
GPT_TCLR	RW	32	0x0000 0038	0x4803 E038	0x4808 8038
GPT_TCRR	RW	32	0x0000 003C	0x4803 E03C	0x4808 803C
GPT_TLDR	RW	32	0x0000 0040	0x4803 E040	0x4808 8040
GPT_TTGR	RW	32	0x0000 0044	0x4803 E044	0x4808 8044
GPT_TWPS	R	32	0x0000 0048	0x4803 E048	0x4808 8048
GPT_TMAR	RW	32	0x0000 004C	0x4803 E04C	0x4808 804C
GPT_TCAR1	R	32	0x0000 0050	0x4803 E050	0x4808 8050
GPT_TSICR	RW	32	0x0000 0054	0x4803 E054	0x4808 8054
GPT_TCAR2	R	32	0x0000 0058	0x4803 E058	0x4808 8058

22.2.6.2.2 GP Timer Register Description

Table 22-28. GPT_TIDR

Address Offset	0x0000 0000		
Physical Address	0x4A31 8000	**Instance**	GPTIMER1_L4
	0x4803 2000		GPTIMER2_L4
	0x4808 6000		GPTIMER10_L4
	0x4803 4000		GPTIMER3_L4
	0x4803 6000		GPTIMER4_L4
	0x4903 8000		GPTIMER5_L3
	0x4013 8000		GPTIMER5_CORTEX-A9
	0x01D3 8000		GPTIMER5_DSP
	0x4903 A000		GPTIMER6_L3
	0x4013 A000		GPTIMER6_CORTEX-A9
	0x01D3 A000		GPTIMER6_DSP
	0x4903 C000		GPTIMER7_L3
	0x4013 C000		GPTIMER7_CORTEX-A9
	0x01D3 C000		GPTIMER7_DSP
	0x4903 E000		GPTIMER8_L3
	0x4013 E000		GPTIMER8_CORTEX-A9
	0x01D3 E000		GPTIMER8_DSP
	0x4803 E000		GPTIMER9_L4
	0x4808 8000		GPTIMER11_L4
Description	This read-only register contains the revision number of the module. A write to this register has no effect. This register is used by software to track features, bugs, and compatibility.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31: 0	REVISION	IP Revision	R	0x– [1]

[1] TI internal data

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Table 22-29. Register Call Summary for Register GPT_TIDR

General-Purpose Timers

- Accessing GP Timer Registers: [0] [1]
- GP Timer Register Summary: [2] [3] [4] [5] [6] [7] [8]

Table 22-30. GPT_TIOCP_CFG

Address Offset	0x0000 0010		
Physical Address	0x4803 4010	**Instance**	GPTIMER3_L4
	0x4803 6010		GPTIMER4_L4
	0x4903 8010		GPTIMER5_L3
	0x4013 8010		GPTIMER5_CORTEX-A9
	0x01D3 8010		GPTIMER5_DSP
	0x4903 A010		GPTIMER6_L3
	0x4013 A010		GPTIMER6_CORTEX-A9
	0x01D3 A010		GPTIMER6_DSP
	0x4903 C010		GPTIMER7_L3
	0x4013 C010		GPTIMER7_CORTEX-A9
	0x01D3 C010		GPTIMER7_DSP
	0x4903 E010		GPTIMER8_L3
	0x4013 E010		GPTIMER8_CORTEX-A9
	0x01D3 E010		GPTIMER8_DSP
	0x4803 E010		GPTIMER9_L4
	0x4808 8010		GPTIMER11_L4
Description	This register controls the various parameters of the L4 interface.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												IDLEMODE		EMUFREE	SOFTRESET

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved	R	0x0000000
3:2	IDLEMODE	Power management, req/ack control 0x0: Force-idle mode: local target idle state follows (acknowledges) the system idle requests unconditionally, that is, regardless of the IP module internal requirements. Back-up mode, for debug only. 0x1: No-idle mode: local target never enters idle state. Back-up mode, for debug only. 0x2: Smart-idle mode: local target idle state eventually follows (acknowledges) the system idle requests, depending on the IP module internal requirements. IP module should not generate (IRQ- or DMA-request-related) wake-up events. 0x3: Smart-idle wake-up-capable mode: local target idle state eventually follows (acknowledges) the system idle requests, depending on the IP module internal requirements. IP module may generate (IRQ- or DMA-request-related) wake-up events when in idle state. Mode is only relevant if the appropriate IP module *swake-up* output(s) is (are) implemented.	RW	0x0
1	EMUFREE	Emulation mode 0x0: The timer is frozen in emulation mode (PINSUSPENDN signal active). 0x1: The timer runs free, regardless of PINSUSPENDN value.	RW	0

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Bits	Field Name	Description	Type	Reset
0	SOFTRESET	Software reset 0x0: Read 0: reset done, no pending action Write 0: No action 0x1: Read 1: initiate software reset Write 1: Reset ongoing	RW	0

Table 22-31. Register Call Summary for Register GPT_TIOCP_CFG

General-Purpose Timers

- Power Management of Other GP Timers: [0]
- Wake-Up Capability: [1]
- Software Reset: [2] [3] [4]
- Timer Under Emulation: [5] [6] [7]
- Accessing GP Timer Registers: [8] [9]
- Writing to Timer Registers: [10]
- GP Timer Module Global Initialization: [11] [12] [13]
- GP Timer Register Summary: [14] [15] [16] [17] [18] [19]

Table 22-32. GPT1MS_TIOCP_CFG

Address Offset	0x0000 0010		
Physical Address	0x4A31 8010 0x4803 2010 0x4808 6010	**Instance**	GPTIMER1_L4 GPTIMER2_L4 GPTIMER10_L4
Description	This register controls the various parameters of the OCP interface.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						CLOCKACTIVITY		RESERVED		EMUFREE		IDLEMODE		ENAWAKEUP	SOFTRESET	AUTOIDLE

Bits	Field Name	Description	Type	Reset
31:10	RESERVED	Reserved	R	0x000000
9:8	CLOCKACTIVITY	Clock activity 0x0: Functional clock can be switched-off ; L4 clock can be switched-off. 0x1: Functional clock can be switched-off ; L4 clock is maintained during wake-up period. 0x2: Functional clock is maintained during wake-up period; L4 clock can be switched-off. 0x3: Functional clock is maintained during wake-up period; L4 clock is maintained during wake-up period.	RW	0x0
7:6	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0
5	EMUFREE	Emulation mode 0x0: Timer counter frozen in emulation 0x1: Timer counter free-running in emulation	RW	0

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Bits	Field Name	Description	Type	Reset
4:3	IDLEMODE	Power management, req/ack control 0x0: Force-idle. An idle request is acknowledged unconditionally. 0x1: No-idle. An idle request is never acknowledged. 0x2: Smart-idle. Acknowledgment to an idle request is given based on the internal activity of the module. 0x3: Reserved, do not use.	RW	0x0
2	ENAWAKEUP	Wake-up feature global control 0x0: No wake-up line assertion in idle mode 0x1: Wake-up line assertion enabled in smart-idle mode.	RW	0
1	SOFTRESET	Software reset. This bit is automatically reset by the hardware. During reads, it always returns 0. 0x0: Normal mode 0x1: The module is reset.	RW	0
0	AUTOIDLE	Internal L4 clock gating strategy 0x0: L4 clock is free-running. 0x1: Automatic L4 clock gating strategy is applied, based on the L4 interface activity.	RW	0

Table 22-33. Register Call Summary for Register GPT1MS_TIOCP_CFG

General-Purpose Timers

- GPTIMER1, GPTIMER2, and GPTIMER10 Power Management: [0] [1] [2]
- Wake-Up Capability: [3] [4]
- Software Reset: [5] [6]
- Timer Under Emulation: [7] [8] [9]
- Accessing GP Timer Registers: [10] [11]
- Writing to Timer Registers: [12]
- GP Timer Module Global Initialization: [13] [14] [15] [16] [17]
- GP Timer Register Summary: [18]

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Table 22-34. GPT_IRQSTATUS_RAW

Address Offset	0x0000 0024		
Physical Address	0x4803 4024	**Instance**	GPTIMER3_L4
	0x4803 6024		GPTIMER4_L4
	0x4903 8024		GPTIMER5_L3
	0x4013 8024		GPTIMER5_CORTEX-A9
	0x01D3 8024		GPTIMER5_DSP
	0x4903 A024		GPTIMER6_L3
	0x4013 A024		GPTIMER6_CORTEX-A9
	0x01D3 A024		GPTIMER6_DSP
	0x4903 C024		GPTIMER7_L3
	0x4013 C024		GPTIMER7_CORTEX-A9
	0x01D3 C024		GPTIMER7_DSP
	0x4903 E024		GPTIMER8_L3
	0x4013 E024		GPTIMER8_CORTEX-A9
	0x01D3 E024		GPTIMER8_DSP
	0x4803 E024		GPTIMER9_L4
	0x4808 8024		GPTIMER11_L4
Description	Component interrupt-request status. Check the corresponding secondary status register. Raw status is set even if event is not enabled. Write 1 to set the (raw) status, mostly for debug.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													TCAR_IT_FLAG	OVF_IT_FLAG	MAT_IT_FLAG

Bits	Field Name	Description	Type	Reset
31:3	RESERVED	Reserved	R	0x0000 0000
2	TCAR_IT_FLAG	IRQ status for Capture Read 0: No event pending Write 0: No action Read 1: IRQ event pending Write 1: Trigger IRQ event by software.	RW	0
1	OVF_IT_FLAG	IRQ status for Overflow Read 0: No event pending Write 0: No action Read 1: IRQ event pending Write 1: Trigger IRQ event by software.	RW	0
0	MAT_IT_FLAG	IRQ status for Match Read 0: No event pending Write 0: No action Read 1: IRQ event pending Write 1: Trigger IRQ event by software	RW	0

Table 22-35. Register Call Summary for Register GPT_IRQSTATUS_RAW

General-Purpose Timers

- Accessing GP Timer Registers: [0] [1]
- GP Timer Register Summary: [2] [3] [4] [5] [6] [7]

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Table 22-36. GPT_IRQSTATUS

Address Offset	0x0000 0028		
Physical Address	0x4803 4028	**Instance**	GPTIMER3_L4
	0x4803 6028		GPTIMER4_L4
	0x4903 8028		GPTIMER5_L3
	0x4013 8028		GPTIMER5_CORTEX-A9
	0x01D3 8028		GPTIMER5_DSP
	0x4903 A028		GPTIMER6_L3
	0x4013 A028		GPTIMER6_CORTEX-A9
	0x01D3 A028		GPTIMER6_DSP
	0x4903 C028		GPTIMER7_L3
	0x4013 C028		GPTIMER7_CORTEX-A9
	0x01D3 C028		GPTIMER7_DSP
	0x4903 E028		GPTIMER8_L3
	0x4013 E028		GPTIMER8_CORTEX-A9
	0x01D3 E028		GPTIMER8_DSP
	0x4803 E028		GPTIMER9_L4
	0x4808 8028		GPTIMER11_L4
Description	Component interrupt-request status. Check the corresponding secondary status register. Enabled status is not set unless event is enabled. Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, that is, even if not enabled).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													TCAR_IT_FLAG	OVF_IT_FLAG	MAT_IT_FLAG

Bits	Field Name	Description	Type	Reset
31:3	RESERVED	Reserved	R	0x0000 0000
2	TCAR_IT_FLAG	IRQ status for capture Read 0: No event pending Write 0: No action Read 1: IRQ event pending Write 1: Clear any pending event.	RW	0
1	OVF_IT_FLAG	IRQ status for Overflow Read 0: No event pending Write 0: No action Read 1: IRQ event pending Write 1: Clear any pending event.	RW	0
0	MAT_IT_FLAG	IRQ status for Match Read 0: No event pending Write 0: No action Read 1: IRQ event pending Write 1: Clear any pending event.	RW	0

Table 22-37. Register Call Summary for Register GPT_IRQSTATUS

General-Purpose Timers

- Wake-Up Capability: [0]
- GP Timer Interrupts: [1]
- Capture Mode Functionality: [2] [3] [4] [5]
- Accessing GP Timer Registers: [6] [7]
- Writing to Timer Registers: [8]
- GP Timer Capture Mode: [9] [10]
- GP Timer Register Summary: [11] [12] [13] [14] [15] [16]

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Table 22-38. GPT_IRQENABLE_SET

Address Offset	0x0000 002C		
Physical Address	0x4803 402C	**Instance**	GPTIMER3_L4
	0x4803 602C		GPTIMER4_L4
	0x4903 802C		GPTIMER5_L3
	0x4013 802C		GPTIMER5_CORTEX-A9
	0x01D3 802C		GPTIMER5_DSP
	0x4903 A02C		GPTIMER6_L3
	0x4013 A02C		GPTIMER6_CORTEX-A9
	0x01D3 A02C		GPTIMER6_DSP
	0x4903 C02C		GPTIMER7_L3
	0x4013 C02C		GPTIMER7_CORTEX-A9
	0x01D3 C02C		GPTIMER7_DSP
	0x4903 E02C		GPTIMER8_L3
	0x4013 E02C		GPTIMER8_CORTEX-A9
	0x01D3 E02C		GPTIMER8_DSP
	0x4803 E02C		GPTIMER9_L4
	0x4808 802C		GPTIMER11_L4
Description	Component interrupt-request enable. Write 1 to set (enable interrupt). Readout equal to corresponding _CLR register.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													TCAR_EN_FLAG	OVF_EN_FLAG	MAT_EN_FLAG

Bits	Field Name	Description	Type	Reset
31:3	RESERVED	Reserved	R	0x0000 0000
2	TCAR_EN_FLAG	IRQ enable for Compare Read 0: IRQ event is disabled. Write 0: No action Read 1: IRQ event is enabled Write 1: Set IRQ enable.	RW	0
1	OVF_EN_FLAG	IRQ enable for Overflow Read 0: IRQ event is disabled. Write 0: No action Read 1: IRQ event is enabled. Write 1: Set IRQ enable.	RW	0
0	MAT_EN_FLAG	IRQ enable for Match Read 0: IRQ event is disabled. Write 0: No action Read 1: IRQ event is enabled. Write 1: Set IRQ enable.	RW	0

Table 22-39. Register Call Summary for Register GPT_IRQENABLE_SET

General-Purpose Timers

- GP Timer Functional Description: [0]
- GP Timer Interrupts: [1]
- Timer Mode Functionality: [2]
- Capture Mode Functionality: [3]
- Accessing GP Timer Registers: [4] [5]
- Writing to Timer Registers: [6]
- GP Timer Mode: [7]
- GP Timer Compare Mode: [8]
- GP Timer Capture Mode: [9]
- GP Timer Register Summary: [10] [11] [12] [13] [14] [15]

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Table 22-40. GPT_IRQENABLE_CLR

Address Offset	0x0000 0030		
Physical Address	0x4803 4030	**Instance**	GPTIMER3_L4
	0x4803 6030		GPTIMER4_L4
	0x4903 8030		GPTIMER5_L3
	0x4013 8030		GPTIMER5_CORTEX-A9
	0x01D3 8030		GPTIMER5_DSP
	0x4903 A030		GPTIMER6_L3
	0x4013 A030		GPTIMER6_CORTEX-A9
	0x01D3 A030		GPTIMER6_DSP
	0x4903 C030		GPTIMER7_L3
	0x4013 C030		GPTIMER7_CORTEX-A9
	0x01D3 C030		GPTIMER7_DSP
	0x4903 E030		GPTIMER8_L3
	0x4013 E030		GPTIMER8_CORTEX-A9
	0x01D3 E030		GPTIMER8_DSP
	0x4803 E030		GPTIMER9_L4
	0x4808 8030		GPTIMER11_L4
Description	Component interrupt-request enable. Write 1 to clear (disable interrupt). Readout equal to corresponding _SET register.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													TCAR_EN_FLAG	OVF_EN_FLAG	MAT_EN_FLAG

Bits	Field Name	Description	Type	Reset
31:3	RESERVED	Reserved	R	0x0000 0000
2	TCAR_EN_FLAG	IRQ enable for Compare Read 0: IRQ event is disabled. Write 0: No action Read 1: IRQ event is enabled. Write 1: Clear IRQ enable.	RW	0
1	OVF_EN_FLAG	IRQ enable for Overflow Read 0: IRQ event is disabled. Write 0: No action Read 1: IRQ event is enabled. Write 1: Clear IRQ enable.	RW	0
0	MAT_EN_FLAG	IRQ enable for Match Read 0: IRQ event is disabled. Write 0: No action Read 1: IRQ event is enabled. Write 1: Clear IRQ enable.	RW	0

Table 22-41. Register Call Summary for Register GPT_IRQENABLE_CLR

General-Purpose Timers

- GP Timer Functional Description: [0]
- GP Timer Interrupts: [1]
- Accessing GP Timer Registers: [2] [3]
- Writing to Timer Registers: [4]
- GP Timer Register Summary: [5] [6] [7] [8] [9] [10]

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Table 22-42. GPT_IRQWAKEEN

Address Offset	0x0000 0034		
Physical Address	0x4803 4034	**Instance**	GPTIMER3_L4
	0x4803 6034		GPTIMER4_L4
	0x4903 8034		GPTIMER5_L3
	0x4013 8034		GPTIMER5_CORTEX-A9
	0x01D3 8034		GPTIMER5_DSP
	0x4903 A034		GPTIMER6_L3
	0x4013 A034		GPTIMER6_CORTEX-A9
	0x01D3 A034		GPTIMER6_DSP
	0x4903 C034		GPTIMER7_L3
	0x4013 C034		GPTIMER7_CORTEX-A9
	0x01D3 C034		GPTIMER7_DSP
	0x4903 E034		GPTIMER8_L3
	0x4013 E034		GPTIMER8_CORTEX-A9
	0x01D3 E034		GPTIMER8_DSP
	0x4803 E034		GPTIMER9_L4
	0x4808 8034		GPTIMER11_L4
Description	Wake-up-enabled events taking place when module is idle should generate an asynchronous wake-up.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													TCAR_WUP_ENA	OVF_WUP_ENA	MAT_WUP_ENA

Bits	Field Name	Description	Type	Reset
31:3	RESERVED	Reserved	R	0x0000 0000
2	TCAR_WUP_ENA	Wake-up generation for Compare 0x0: Wake-up disabled 0x1: Wake-up enabled	RW	0
1	OVF_WUP_ENA	Wake-up generation for Overflow 0x0: Wake-up disabled 0x1: Wake-up enabled	RW	0
0	MAT_WUP_ENA	Wake-up generation for Match 0x0: Wake-up disabled 0x1: Wake-up enabled	RW	0

Table 22-43. Register Call Summary for Register GPT_IRQWAKEEN

General-Purpose Timers

- Wake-Up Capability: [0]
- Accessing GP Timer Registers: [1] [2]
- Writing to Timer Registers: [3]
- GP Timer Module Global Initialization: [4]
- GP Timer Register Summary: [5] [6] [7] [8] [9] [10]

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Table 22-44. GPT_TCLR

Address Offset	0x0000 0038		
Physical Address	0x4A31 8024	**Instance**	GPTIMER1_L4
	0x4803 2024		GPTIMER2_L4
	0x4808 6024		GPTIMER10_L4
	0x4803 4038		GPTIMER3_L4
	0x4803 6038		GPTIMER4_L4
	0x4903 8038		GPTIMER5_L3
	0x4013 8038		GPTIMER5_CORTEX-A9
	0x01D3 8038		GPTIMER5_DSP
	0x4903 A038		GPTIMER6_L3
	0x4013 A038		GPTIMER6_CORTEX-A9
	0x01D3 A038		GPTIMER6_DSP
	0x4903 C038		GPTIMER7_L3
	0x4013 C038		GPTIMER7_CORTEX-A9
	0x01D3 C038		GPTIMER7_DSP
	0x4903 E038		GPTIMER8_L3
	0x4013 E038		GPTIMER8_CORTEX-A9
	0x01D3 E038		GPTIMER8_DSP
	0x4803 E038		GPTIMER9_L4
	0x4808 8038		GPTIMER11_L4
Description	This register controls optional features specific to the timer functionality.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																	GPO_CFG	CAPT_MODE	PT	TRG		TCM		SCPWM	CE	PRE	PTV			AR	ST

Bits	Field Name	Description	Type	Reset
31:15	RESERVED	Reserved	R	0x00000
14	GPO_CFG	General-purpose output - this register directly drives the GPTi_PORGPOCFG output pin. For specific use of the GPO_CFG bit, see Section 22.2.2.1, *GP Timer External System Interface*. 0x0: GPTi_PORGPOCFG drives 0. 0x1: GPTi_PORGPOCFG drives 1.	RW	0
13	CAPT_MODE	Capture mode select bit (first/second) 0x0: Single capture: Capture the first enabled capture event in TCAR1. 0x1: Capture on second event: Capture the second enabled capture event in TCAR2.	RW	0
12	PT	Pulse or toggle mode on GPTi_PWM_out output pin 0x0: Pulse modulation 0x1: Toggle modulation	RW	0
11:10	TRG	Trigger output mode on GPTi_PWM_out output pin 0x0: No trigger 0x1: Trigger on overflow. 0x2: Trigger on overflow and match. 0x3: Reserved	RW	0x0

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Bits	Field Name	Description	Type	Reset
9:8	TCM	Transition capture mode on GPTi_EVENT_CAPTURE input pin (When the TCM field passed from (00) to any other combination, the TCAR_IT_FLAG and the edge detection logic are cleared.) 0x0: No capture 0x1: Capture on rising edges of GPTi_EVENT_CAPTURE pin 0x2: Capture on falling edges of GPTi_EVENT_CAPTURE pin 0x3: Capture on both edges of GPTi_EVENT_CAPTURE pin	RW	0x0
7	SCPWM	Pulse width modulation output pin default setting This bit must be set or clear while the timer is stopped or the trigger is off. 0x0: Clear the GPTi_PWM_out output pin and select positive pulse for pulse mode. 0x1: Set the GPTi_PWM_out output pin and select negative pulse for pulse mode.	RW	0
6	CE	Compare enable 0x0: Compare mode is disable. 0x1: Compare mode is enable.	RW	0
5	PRE	Prescaler enable 0x0: The TIMER clock input pin clocks the counter. 0x1: The divided input pin clocks the counter.	RW	0
4:2	PTV	Prescale clock timer value The timer counter is prescaled with the value $2^{(PTV+1)}$. Example: PTV = 3, counter increases value (if started) after 16 functional clock periods.	RW	0x0
1	AR	Autoreload mode 0x0: One shot timer 0x1: Autoreload timer	RW	0
0	ST	Start/stop timer control 0x0: Stop timer: Only the counter is frozen. If one-shot mode selected (AR =0), this bit is automatically reset by internal logic when the counter is overflowed. 0x1: Start timer	RW	0

Table 22-45. Register Call Summary for Register GPT_TCLR

General-Purpose Timers

- Timer Mode Functionality: [0] [1] [2] [3] [4] [5] [6]
- Capture Mode Functionality: [7] [8] [9] [10] [11] [12] [13] [14] [15]
- Compare Mode Functionality: [16] [17] [18] [19]
- Prescaler Functionality: [20] [21]
- Pulse-Width Modulation: [22] [23] [24] [25] [26] [27] [28] [29] [30] [31]
- Timer Counting Rate: [32] [33] [34] [35] [36] [37] [38]
- Accessing GP Timer Registers: [39]
- Writing to Timer Registers: [40] [41]
- GP Timer Mode: [42] [43] [44] [45]
- GP Timer Compare Mode: [46] [47] [48] [49] [50]
- GP Timer Capture Mode: [51] [52] [53] [54] [55] [56] [57]
- GP Timer PWM Mode: [58] [59] [60] [61] [62] [63] [64] [65] [66]
- GP Timer Register Summary: [67] [68] [69] [70] [71] [72] [73]
- GP Timer Register Description: [74] [75]

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Table 22-46. GPT_TCRR

Address Offset	0x0000 003C		
Physical Address	0x4A31 8028	**Instance**	GPTIMER1_L4
	0x4803 2028		GPTIMER2_L4
	0x4808 6028		GPTIMER10_L4
	0x4803 403C		GPTIMER3_L4
	0x4803 603C		GPTIMER4_L4
	0x4903 803C		GPTIMER5_L3
	0x4013 803C		GPTIMER5_CORTEX-A9
	0x01D3 803C		GPTIMER5_DSP
	0x4903 A03C		GPTIMER6_L3
	0x4013 A03C		GPTIMER6_CORTEX-A9
	0x01D3 A03C		GPTIMER6_DSP
	0x4903 C03C		GPTIMER7_L3
	0x4013 C03C		GPTIMER7_CORTEX-A9
	0x01D3 C03C		GPTIMER7_DSP
	0x4903 E03C		GPTIMER8_L3
	0x4013 E03C		GPTIMER8_CORTEX-A9
	0x01D3 E03C		GPTIMER8_DSP
	0x4803 E03C		GPTIMER9_L4
	0x4808 803C		GPTIMER11_L4
Description	This register holds the value of the internal counter.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TIMER_COUNTER																															

Bits	Field Name	Description	Type	Reset
31:0	TIMER_COUNTER	Value of TIMER counter	RW	0x0000 0000

Table 22-47. Register Call Summary for Register GPT_TCRR

General-Purpose Timers

- Wake-Up Capability: [0] [1]
- Timer Mode Functionality: [2] [3] [4] [5] [6] [7] [8] [9] [10]
- 1-ms Tick Generation (Only GPTIMER1, GPTIMER2, and GPTIMER10): [11] [12] [13]
- Capture Mode Functionality: [14] [15]
- Compare Mode Functionality: [16] [17]
- Prescaler Functionality: [18] [19]
- Accessing GP Timer Registers: [20]
- Writing to Timer Registers: [21] [22] [23] [24]
- Reading From Timer Counter Registers: [25]
- GP Timer Mode: [26]
- GP Timer Compare Mode: [27]
- GP Timer Register Summary: [28] [29] [30] [31] [32] [33] [34]
- GP Timer Register Description: [35] [36]

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Table 22-48. GPT_TLDR

Address Offset	0x0000 0040		
Physical Address	0x4A31 802C	**Instance**	GPTIMER1_L4
	0x4803 202C		GPTIMER2_L4
	0x4808 602C		GPTIMER10_L4
	0x4803 4040		GPTIMER3_L4
	0x4803 6040		GPTIMER4_L4
	0x4903 8040		GPTIMER5_L3
	0x4013 8040		GPTIMER5_CORTEX-A9
	0x01D3 8040		GPTIMER5_DSP
	0x4903 A040		GPTIMER6_L3
	0x4013 A040		GPTIMER6_CORTEX-A9
	0x01D3 A040		GPTIMER6_DSP
	0x4903 C040		GPTIMER7_L3
	0x4013 C040		GPTIMER7_CORTEX-A9
	0x01D3 C040		GPTIMER7_DSP
	0x4903 E040		GPTIMER8_L3
	0x4013 E040		GPTIMER8_CORTEX-A9
	0x01D3 E040		GPTIMER8_DSP
	0x4803 E040		GPTIMER9_L4
	0x4808 8040		GPTIMER11_L4
Description	This register holds the timer load value.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOAD_VALUE																															

Bits	Field Name	Description	Type	Reset
31:0	LOAD_VALUE	Timer counter value loaded on overflow in autoreload mode or on GPT_TTGR write access. LOAD_VALUE must be different than the timer overflow value (0xFFFF FFFF).	RW	0x0000 0000

Table 22-49. Register Call Summary for Register GPT_TLDR

General-Purpose Timers

- Timer Mode Functionality: [0] [1] [2]
- 1-ms Tick Generation (Only GPTIMER1, GPTIMER2, and GPTIMER10): [3] [4] [5] [6] [7] [8] [9] [10] [11] [12]
- Prescaler Functionality: [13] [14]
- Pulse-Width Modulation: [15] [16] [17]
- Timer Counting Rate: [18] [19] [20] [21] [22]
- Accessing GP Timer Registers: [23]
- Writing to Timer Registers: [24] [25]
- GP Timer Mode: [26]
- GP Timer PWM Mode: [27]
- GP Timer Register Summary: [28] [29] [30] [31] [32] [33] [34]
- GP Timer Register Description: [35] [36]

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Table 22-50. GPT_TTGR

Address Offset	0x0000 0044		
Physical Address	0x4A31 8030	**Instance**	GPTIMER1_L4
	0x4803 2030		GPTIMER2_L4
	0x4808 6030		GPTIMER10_L4
	0x4803 4044		GPTIMER3_L4
	0x4803 6044		GPTIMER4_L4
	0x4903 8044		GPTIMER5_L3
	0x4013 8044		GPTIMER5_CORTEX-A9
	0x01D3 8044		GPTIMER5_DSP
	0x4903 A044		GPTIMER6_L3
	0x4013 A044		GPTIMER6_CORTEX-A9
	0x01D3 A044		GPTIMER6_DSP
	0x4903 C044		GPTIMER7_L3
	0x4013 C044		GPTIMER7_CORTEX-A9
	0x01D3 C044		GPTIMER7_DSP
	0x4903 E044		GPTIMER8_L3
	0x4013 E044		GPTIMER8_CORTEX-A9
	0x01D3 E044		GPTIMER8_DSP
	0x4803 E044		GPTIMER9_L4
	0x4808 8044		GPTIMER11_L4
Description	The read value of this register is always 0xFFFF FFFF.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TTGR_VALUE																															

Bits	Field Name	Description	Type	Reset
31:0	TTGR_VALUE	Writing to the TTGR register causes the GPT_TCRR to be loaded from GPT_TLDR and the prescaler counter to be cleared. Reload is done regardless of the AR field value of the GPT_TCLR register.	RW Rreturns 1s	0xFFFF FFFF

Table 22-51. Register Call Summary for Register GPT_TTGR

General-Purpose Timers

- Timer Mode Functionality: [0] [1]
- Prescaler Functionality: [2]
- Accessing GP Timer Registers: [3]
- Writing to Timer Registers: [4] [5]
- GP Timer Register Summary: [6] [7] [8] [9] [10] [11] [12]
- GP Timer Register Description: [13] [14]

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Table 22-52. GPT_TWPS

Address Offset	0x0000 0048		
Physical Address	0x4A31 8034	**Instance**	GPTIMER1_L4
	0x4803 2034		GPTIMER2_L4
	0x4808 6034		GPTIMER10_L4
	0x4803 4048		GPTIMER3_L4
	0x4803 6048		GPTIMER4_L4
	0x4903 8048		GPTIMER5_L3
	0x4013 8048		GPTIMER5_CORTEX-A9
	0x01D3 8048		GPTIMER5_DSP
	0x4903 A048		GPTIMER6_L3
	0x4013 A048		GPTIMER6_CORTEX-A9
	0x01D3 A048		GPTIMER6_DSP
	0x4903 C048		GPTIMER7_L3
	0x4013 C048		GPTIMER7_CORTEX-A9
	0x01D3 C048		GPTIMER7_DSP
	0x4903 E048		GPTIMER8_L3
	0x4013 E048		GPTIMER8_CORTEX-A9
	0x01D3 E048		GPTIMER8_DSP
	0x4803 E048		GPTIMER9_L4
	0x4808 8048		GPTIMER11_L4
Description	This register contains the write posting bits for all writable functional registers.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																											W_PEND_TMAR	W_PEND_TTGR	W_PEND_TLDR	W_PEND_TCRR	W_PEND_TCLR

Bits	Field Name	Description	Type	Reset
31:5	RESERVED	Reserved	R	0x0000000
4	W_PEND_TMAR	When equal to 1, a write is pending to the GPT_TMAR register.	R	0
3	W_PEND_TTGR	When equal to 1, a write is pending to the GPT_TTGR register.	R	0
2	W_PEND_TLDR	When equal to 1, a write is pending to the GPT_TLDR register.	R	0
1	W_PEND_TCRR	When equal to 1, a write is pending to the GPT_TCRR register.	R	0
0	W_PEND_TCLR	When equal to 1, a write is pending to the GPT_TCLR register.	R	0

Table 22-53. Register Call Summary for Register GPT_TWPS

General-Purpose Timers

- Accessing GP Timer Registers: [0]
- Writing to Timer Registers: [1]
- GP Timer Register Summary: [2] [3] [4] [5] [6] [7] [8]

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Table 22-54. GPT_TMAR

Address Offset	0x0000 004C		
Physical Address	0x4A31 8038	**Instance**	GPTIMER1_L4
	0x4803 2038		GPTIMER2_L4
	0x4808 6038		GPTIMER10_L4
	0x4803 404C		GPTIMER3_L4
	0x4803 604C		GPTIMER4_L4
	0x4903 804C		GPTIMER5_L3
	0x4013 804C		GPTIMER5_CORTEX-A9
	0x01D3 804C		GPTIMER5_DSP
	0x4903 A04C		GPTIMER6_L3
	0x4013 A04C		GPTIMER6_CORTEX-A9
	0x01D3 A04C		GPTIMER6_DSP
	0x4903 C04C		GPTIMER7_L3
	0x4013 C04C		GPTIMER7_CORTEX-A9
	0x01D3 C04C		GPTIMER7_DSP
	0x4903 E04C		GPTIMER8_L3
	0x4013 E04C		GPTIMER8_CORTEX-A9
	0x01D3 E04C		GPTIMER8_DSP
	0x4803 E04C		GPTIMER9_L4
	0x4808 804C		GPTIMER11_L4
Description	The compare logic consists of a 32-bit-wide, read/write data TMAR register and logic to compare counter.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMPARE_VALUE																															

Bits	Field Name	Description	Type	Reset
31:0	COMPARE_VALUE	Value to be compared to the timer counter	RW	0x0000 0000

Table 22-55. Register Call Summary for Register GPT_TMAR

General-Purpose Timers

- Wake-Up Capability: [0]
- Compare Mode Functionality: [1] [2] [3] [4]
- Pulse-Width Modulation: [5] [6] [7]
- Accessing GP Timer Registers: [8]
- Writing to Timer Registers: [9] [10]
- GP Timer Compare Mode: [11]
- GP Timer PWM Mode: [12]
- GP Timer Register Summary: [13] [14] [15] [16] [17] [18] [19]
- GP Timer Register Description: [20]

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Table 22-56. GPT_TCAR1

Address Offset	0x0000 0050		
Physical Address	0x4A31 803C	**Instance**	GPTIMER1_L4
	0x4803 203C		GPTIMER2_L4
	0x4808 603C		GPTIMER10_L4
	0x4803 4050		GPTIMER3_L4
	0x4803 6050		GPTIMER4_L4
	0x4903 8050		GPTIMER5_L3
	0x4013 8050		GPTIMER5_CORTEX-A9
	0x01D3 8050		GPTIMER5_DSP
	0x4903 A050		GPTIMER6_L3
	0x4013 A050		GPTIMER6_CORTEX-A9
	0x01D3 A050		GPTIMER6_DSP
	0x4903 C050		GPTIMER7_L3
	0x4013 C050		GPTIMER7_CORTEX-A9
	0x01D3 C050		GPTIMER7_DSP
	0x4903 E050		GPTIMER8_L3
	0x4013 E050		GPTIMER8_CORTEX-A9
	0x01D3 E050		GPTIMER8_DSP
	0x4803 E050		GPTIMER9_L4
	0x4808 8050		GPTIMER11_L4
Description	This register holds the first captured value of the counter register.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPTURE_VALUE1																															

Bits	Field Name	Description	Type	Reset
31:0	CAPTURE_VALUE1	First timer counter value captured on an external event trigger	R	0x0000 0000

Table 22-57. Register Call Summary for Register GPT_TCAR1

General-Purpose Timers

- Capture Mode Functionality: [0] [1] [2] [3] [4] [5] [6] [7] [8]
- Reading From Timer Counter Registers: [9]
- GP Timer Capture Mode: [10]
- GP Timer Register Summary: [11] [12] [13] [14] [15] [16] [17]

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Table 22-58. GPT_TSICR

Address Offset	0x0000 0054		
Physical Address	0x4A31 8040	**Instance**	GPTIMER1_L4
	0x4803 2040		GPTIMER2_L4
	0x4808 6040		GPTIMER10_L4
	0x4803 4054		GPTIMER3_L4
	0x4803 6054		GPTIMER4_L4
	0x4903 8054		GPTIMER5_L3
	0x4013 8054		GPTIMER5_CORTEX-A9
	0x01D3 8054		GPTIMER5_DSP
	0x4903 A054		GPTIMER6_L3
	0x4013 A054		GPTIMER6_CORTEX-A9
	0x01D3 A054		GPTIMER6_DSP
	0x4903 C054		GPTIMER7_L3
	0x4013 C054		GPTIMER7_CORTEX-A9
	0x01D3 C054		GPTIMER7_DSP
	0x4903 E054		GPTIMER8_L3
	0x4013 E054		GPTIMER8_CORTEX-A9
	0x01D3 E054		GPTIMER8_DSP
	0x4803 E054		GPTIMER9_L4
	0x4808 8054		GPTIMER11_L4
Description	Timer synchronous interface control register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													POSTED	SFT	RESERVED

Bits	Field Name	Description	Type	Reset
31:3	RESERVED	Reserved	R	0x0000 0000
2	POSTED	Posted mode selection 0x0: Posted mode inactive: Delay the command accept output signal. 0x1: Posted mode active	RW	-
1	SFT	This bit resets all the functional part of the module. 0x0: Software reset is disabled. 0x1: Software reset is enabled.	RW	0
0	RESERVED	Reserved	R	0

Table 22-59. Register Call Summary for Register GPT_TSICR

General-Purpose Timers

- Software Reset: [0] [1]
- Accessing GP Timer Registers: [2] [3]
- Writing to Timer Registers: [4] [5] [6]
- GP Timer Module Global Initialization: [7]
- GP Timer Register Summary: [8] [9] [10] [11] [12] [13] [14]

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Table 22-60. GPT_TCAR2

Address Offset	0x0000 0058		
Physical Address	0x4A31 8044	**Instance**	GPTIMER1_L4
	0x4803 2044		GPTIMER2_L4
	0x4808 6044		GPTIMER10_L4
	0x4803 4058		GPTIMER3_L4
	0x4803 6058		GPTIMER4_L4
	0x4903 8058		GPTIMER5_L3
	0x4013 8058		GPTIMER5_CORTEX-A9
	0x01D3 8058		GPTIMER5_DSP
	0x4903 A058		GPTIMER6_L3
	0x4013 A058		GPTIMER6_CORTEX-A9
	0x01D3 A058		GPTIMER6_DSP
	0x4903 C058		GPTIMER7_L3
	0x4013 C058		GPTIMER7_CORTEX-A9
	0x01D3 C058		GPTIMER7_DSP
	0x4903 E058		GPTIMER8_L3
	0x4013 E058		GPTIMER8_CORTEX-A9
	0x01D3 E058		GPTIMER8_DSP
	0x4803 E058		GPTIMER9_L4
	0x4808 8058		GPTIMER11_L4
Description	This register holds the second captured value of the counter register.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPTURE_VALUE2																															

Bits	Field Name	Description	Type	Reset
31:0	CAPTURE_VALUE2	Second timer counter value captured on an external event trigger	R	0x0000 0000

Table 22-61. Register Call Summary for Register GPT_TCAR2

General-Purpose Timers

- Capture Mode Functionality: [0] [1] [2] [3] [4]
- Reading From Timer Counter Registers: [5]
- GP Timer Capture Mode: [6]
- GP Timer Register Summary: [7] [8] [9] [10] [11] [12] [13]

22.2.6.2.3 GPTIMER1, GPTIMER2 , and GPTIMER10 Register Description

Table 22-62. GPT_TISTAT

Address Offset	0x0000 0014		
Physical Address	0x4A31 8014	**Instance**	GPTIMER1_L4
	0x4803 2014		GPTIMER2_L4
	0x4808 6014		GPTIMER10_L4
Description	This register provides status information about the module, excluding interrupt status information.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															RESETDONE

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Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reads return 0.	R	0x0000 0000
0	RESETDONE	Internal reset monitoring Read 0x0: Internal module reset in ongoing. Read 0x1: Reset complete	R	-

Table 22-63. Register Call Summary for Register GPT_TISTAT

General-Purpose Timers

- Software Reset: [0]
- Accessing GP Timer Registers: [1]
- GP Timer Register Summary: [2]

Table 22-64. GPT_TISR

Address Offset	0x0000 0018		
Physical Address	0x4A31 8018 0x4803 2018 0x4808 6018	**Instance**	GPTIMER1_L4 GPTIMER2_L4 GPTIMER10_L4
Description	The timer status register is used to determine which of the timer events requested an interrupt.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													TCAR_IT_FLAG	OVF_IT_FLAG	MAT_IT_FLAG

Bits	Field Name	Description	Type	Reset
31:3	RESERVED	Reads return 0.	R	0x0000 0000
2	TCAR_IT_FLAG	Indicates when an external pulse transition of the correct polarity is detected on external pin GPTi_EVENT_CAPTURE 0x0: No capture interrupt request 0x1: Capture interrupt request	RW	0
1	OVF_IT_FLAG	TCRR overflow 0x0: No overflow interrupt request 0x1: Overflow interrupt pending	RW	0
0	MAT_IT_FLAG	The compare result of TCRR and TMAR 0x0: No compare interrupt request 0x1: Compare interrupt pending	RW	0

Table 22-65. Register Call Summary for Register GPT_TISR

General-Purpose Timers

- Wake-Up Capability: [0]
- GP Timer Interrupts: [1]
- 1-ms Tick Generation (Only GPTIMER1, GPTIMER2, and GPTIMER10): [2]
- Capture Mode Functionality: [3] [4] [5] [6]
- Accessing GP Timer Registers: [7]
- Writing to Timer Registers: [8]
- GP Timer Capture Mode: [9] [10]
- GP Timer Register Summary: [11]

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Table 22-66. GPT_TIER

Address Offset	0x0000 001C		
Physical Address	0x4A31 801C 0x4803 201C 0x4808 601C	**Instance**	GPTIMER1_L4 GPTIMER2_L4 GPTIMER10_L4
Description	This register controls (enable/disable) the interrupt events.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													TCAR_IT_ENA	OVF_IT_ENA	MAT_IT_ENA

Bits	Field Name	Description	Type	Reset
31:3	RESERVED	Reads return 0.	R	0x0000 0000
2	TCAR_IT_ENA	Capture interrupt enable 0x0: Disable capture interrupt. 0x1: Enable capture interrupt.	RW	0
1	OVF_IT_ENA	Overflow interrupt enable 0x0: Disable overflow interrupt. 0x1: Enable overflow interrupt.	RW	0
0	MAT_IT_ENA	Match interrupt enable 0x0: Disable match interrupt. 0x1: Enable match interrupt.	RW	0

Table 22-67. Register Call Summary for Register GPT_TIER

General-Purpose Timers

- GP Timer Functional Description: [0]
- GP Timer Interrupts: [1]
- Timer Mode Functionality: [2]
- Capture Mode Functionality: [3]
- Compare Mode Functionality: [4]
- Accessing GP Timer Registers: [5]
- Writing to Timer Registers: [6]
- GP Timer Mode: [7]
- GP Timer Compare Mode: [8]
- GP Timer Capture Mode: [9]
- GP Timer Register Summary: [10]

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Table 22-68. GPT_TWER

Address Offset	0x0000 0020		
Physical Address	0x4A31 8020 0x4803 2020 0x4808 6020	**Instance**	GPTIMER1_L4 GPTIMER2_L4 GPTIMER10_L4
Description	This register controls (enable/disable) the wake-up feature on specific interrupt events.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													TCAR_WUP_ENA	OVF_WUP_ENA	MAT_WUP_ENA

Bits	Field Name	Description	Type	Reset
31:3	RESERVED	Reads return 0	R	0x0000 0000
2	TCAR_WUP_ENA	Capture wake-up enable 0x0: Disable capture wake-up. 0x1: Enable capture wake-up.	RW	0
1	OVF_WUP_ENA	Overflow wake-up enable 0x0: Disable overflow wake-up. 0x1: Enable overflow wake-up.	RW	0
0	MAT_WUP_ENA	Match wake-up enable 0x0: Disable match wake-up. 0x1: Enable match wake-up.	RW	0

Table 22-69. Register Call Summary for Register GPT_TWER

General-Purpose Timers

- GP Timer Functional Description: [0]
- Wake-Up Capability: [1] [2]
- Accessing GP Timer Registers: [3]
- Writing to Timer Registers: [4]
- GP Timer Module Global Initialization: [5]
- GP Timer Register Summary: [6]

Table 22-70. GPT_TPIR

Address Offset	0x0000 0048		
Physical Address	0x4A31 8048 0x4803 2048 0x4808 6048	**Instance**	GPTIMER1_L4 GPTIMER2_L4 GPTIMER10_L4
Description	This register is used for 1-ms tick generation. The TPIR register holds the value of the positive increment. The value of this register is added to the value of TCVR to determine whether next value loaded in TCRR is the subperiod value or the overperiod value.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
POSITIVE_INC_VALUE																															

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Bits	Field Name	Description	Type	Reset
31:0	POSITIVE_INC_VALUE	Value of the positive increment	RW	0x0000 0000

Table 22-71. Register Call Summary for Register GPT_TPIR

General-Purpose Timers

- 1-ms Tick Generation (Only GPTIMER1, GPTIMER2, and GPTIMER10): [0] [1] [2] [3] [4] [5]
- Accessing GP Timer Registers: [6]
- Writing to Timer Registers: [7] [8]
- GP Timer Register Summary: [9]

Table 22-72. GPT_TNIR

Address Offset	0x0000 004C		
Physical Address	0x4A31 804C 0x4803 204C 0x4808 604C	**Instance**	GPTIMER1_L4 GPTIMER2_L4 GPTIMER10_L4
Description	This register is used for 1-ms tick generation. The TNIR register holds the value of the negative increment. The value of this register is added to the value of the TCVR to determine whether next value loaded in TCRR is the subperiod value or the overperiod value.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NEGATIVE_INV_VALUE																															

Bits	Field Name	Description	Type	Reset
31:0	NEGATIVE_INV_VALUE	Value of the negative increment	RW	0x0000 0000

Table 22-73. Register Call Summary for Register GPT_TNIR

General-Purpose Timers

- 1-ms Tick Generation (Only GPTIMER1, GPTIMER2, and GPTIMER10): [0] [1] [2] [3] [4] [5]
- Accessing GP Timer Registers: [6]
- Writing to Timer Registers: [7] [8]
- GP Timer Register Summary: [9]

Table 22-74. GPT_TCVR

Address Offset	0x0000 0050		
Physical Address	0x4A31 8050 0x4803 2050 0x4808 6050	**Instance**	GPTIMER1_L4 GPTIMER2_L4 GPTIMER10_L4
Description	This register is used for 1-ms tick generation. The TCVR register determines whether next value loaded in TCRR is the subperiod value or the overperiod value.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNTER_VALUE																															

Bits	Field Name	Description	Type	Reset
31:0	COUNTER_VALUE	Value of CVR counter	RW	0x0000 0000

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Table 22-75. Register Call Summary for Register GPT_TCVR

General-Purpose Timers

- 1-ms Tick Generation (Only GPTIMER1, GPTIMER2, and GPTIMER10): [0] [1]
- Accessing GP Timer Registers: [2]
- Writing to Timer Registers: [3] [4]
- GP Timer Register Summary: [5]

Table 22-76. GPT_TOCR

Address Offset	0x0000 0054		
Physical Address	0x4A31 8054 0x4803 2054 0x4808 6054	**Instance**	GPTIMER1_L4 GPTIMER2_L4 GPTIMER10_L4
Description	This register is used to mask the tick interrupt for a selected number of ticks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								OVF_COUNTER_VALUE																							

Bits	Field Name	Description	Type	Reset
31:24	RESERVED	Reads return 0.	R	0x00
23:0	OVF_COUNTER_VALUE	Number of overflow events	RW	0x000000

Table 22-77. Register Call Summary for Register GPT_TOCR

General-Purpose Timers

- 1-ms Tick Generation (Only GPTIMER1, GPTIMER2, and GPTIMER10): [0] [1] [2] [3] [4]
- Accessing GP Timer Registers: [5]
- Writing to Timer Registers: [6] [7]
- GP Timer Register Summary: [8]

Table 22-78. GPT_TOWR

Address Offset	0x0000 0058		
Physical Address	0x4A31 8058 0x4803 2058 0x4808 6058	**Instance**	GPTIMER1_L4 GPTIMER2_L4 GPTIMER10_L4
Description	This register holds the number of masked overflow interrupts.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								OVF_WRAPPING_VALUE																							

Bits	Field Name	Description	Type	Reset
31:24	RESERVED	Reads return 0.	R	0x00
23:0	OVF_WRAPPING_VALUE	Number of masked interrupts	RW	0x000000

Table 22-79. Register Call Summary for Register GPT_TOWR

General-Purpose Timers

- 1-ms Tick Generation (Only GPTIMER1, GPTIMER2, and GPTIMER10): [0] [1] [2]
- Accessing GP Timer Registers: [3]
- Writing to Timer Registers: [4] [5]
- GP Timer Register Summary: [6]

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22.3 Watchdog Timers

22.3.1 Watchdog Timers Overview

The device includes two instances of the 32-bit watchdog timer: WDT2 and WDT3. Figure 22-15 shows how each timer is connected in the device.

NOTE: WDTi (where i is the watchdog timer instance: i = 2 or 3) stands for the following:

- WDT2: Watchdog timer 2, also called MPU watchdog timer
- WDT3: Watchdog timer 3, also called IVA3 watchdog timer

Each watchdog timer is an upward counter capable of generating a pulse on the reset pin and an interrupt to the device system modules following an overflow condition. The MPU watchdog timer serves resets to the PRCM module (its interrupt outputs are unused), and the IVA3 watchdog timer serves watchdog interrupts to the MPU (its reset outputs are unused).

The watchdog timers can be accessed, loaded, and cleared by registers through the L4 interface. The MPU and IVA3 watchdog timers have the 32-kHz clock for their timer clock input.

The MPU watchdog timer directly generates a warm reset condition on overflow. The IVA3 watchdog timer generates an MPU interrupt condition on overflow, which can be used by the application software through the PRCM module to indirectly trigger a reset condition (that is, to the IVA3 subsystem).

The MPU watchdog timer connects to a single target agent port on the L4 interconnect.

Figure 22-15. Watchdog Timers Block Diagram

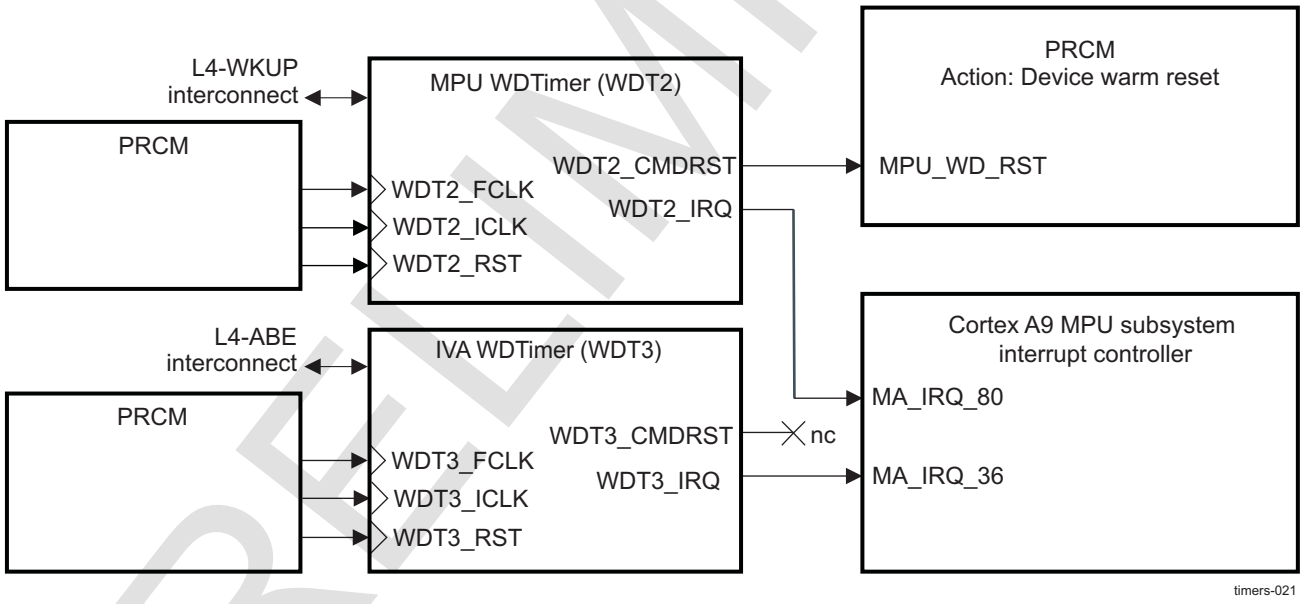

Table 22-80 lists the default state of the watchdog timers in the device.

Table 22-80. Watchdog Timers Default State

Timer	Default State	
MPU WDT2	Enabled	Not running
IVA3 WDT3	Enabled	Not running

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NOTE: The default state of the watchdog timers described in Table 22-80 is considered to be their state immediately after ROM code execution. For more information, see Chapter 27, *Initialization*.

22.3.1.1 Watchdog Timers Features

The main features of the watchdog timer controllers are:

- L4 slave interface support:
  - 32-bit data bus width
  - 32-/16-bit access supported
  - 8-bit access not supported
  - 11-bit address bus width
  - Burst mode not supported
  - Only posted write/read internal resynchronization mode supported
- Free-running 32-bit upward counter
- Programmable divider clock source (2^n where n = [0:7])
- On-the-fly read/write register (while counting)
- Subset programming model of the GP timer
- The watchdog timers are reset either on power-on or after a warm reset before they start counting.
- Reset or interrupt actions when a timer overflow condition occurs
- The watchdog timer generates a reset or an interrupt in its hardware integration (WDT2 or WDT3).

22.3.2 Watchdog Timer Environment

The watchdog timers are accessible through the L4 interface.

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22.3.3 Watchdog Timer Integration

Figure 22-16 shows the integration of the watchdog timers in the device.

Figure 22-16. Watchdog Timers Integration

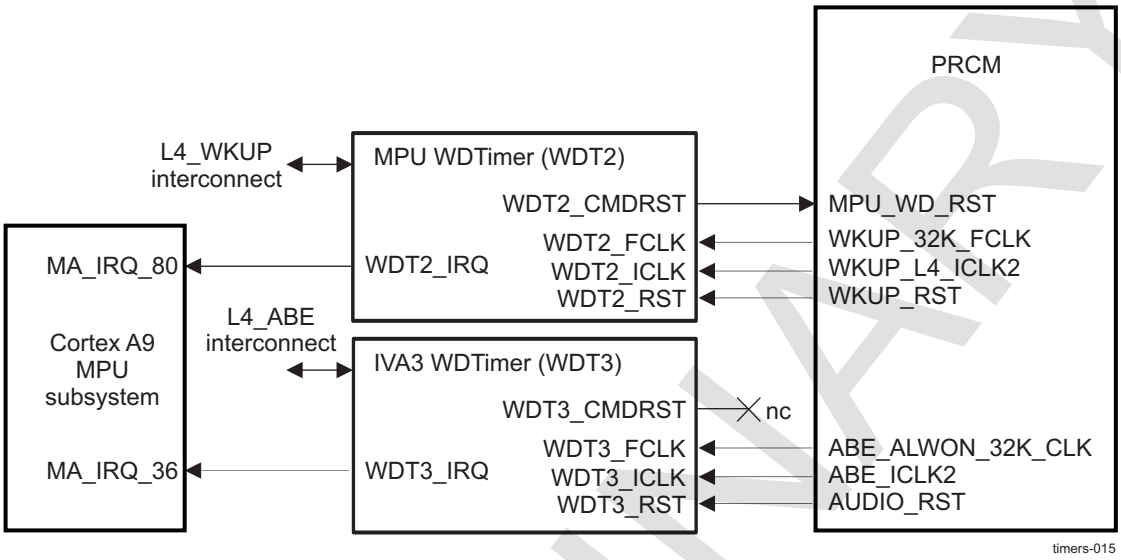

Table 22-81 through Table 22-83 summarize the integration of the module in the device.

Table 22-81. Integration Attributes

Module Instance	Attributes		
	Power Domain	Wake-Up Capability	Interconnect
WDT2	PD_WKUP	Yes	L4_WKUP
WDT3	PD_AUDIO	Yes	L4_ABE

Table 22-82. Clocks and Resets

Clocks				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
WDT2	WDT2_FCLK	WKUP_32K_FCLK	PRCM	WDT2 functional clock
WDT2	WDT2_ICLK	WKUP_L4_ICLK2	PRCM	WDT2 interface clock
WDT3	WDT3_FCLK	ABE_ALWON_32K_CLK	PRCM	WDT3 functional clock
WDT3	WDT3_ICLK	ABE_ICLK2	PRCM	WDT3 interface clock
Resets				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
WDT2	WDT2_RST	WKUP_RST	PRM	Reset to WDT2
WDT2	MPU_WDT_RST	WDT2_CMDRST	WDT2	Reset to PRCM
WDT3	WDT3_RST	AUDIO_RST	PRM	Reset to WDT3

NOTE: WDT2 is reset on power on or after a warm reset before it starts counting.

WDT3 is reset on power on or after a warm reset, and then it does not start counting.

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Table 22-83. Hardware Requests

Interrupt Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
WDT2	WDT2_IRQ	MA_IRQ_80	Cortex-A9 MPU	WDT2 interrupt to Cortex-A9 MPU
WDT3	WDT3_IRQ	MA_IRQ_36	Cortex-A9 MPU	IVA3 watchdog overflow
No DMA Requests				

NOTE:

- See Section 22.3.4.2, *Interrupts*, for interrupt source description.

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22.3.4 Watchdog Timers Functional Description

22.3.4.1 Power Management

There are two clock domains in the watchdog timers:

- Functional clock domain: WDTi_FCLK is the watchdog timer functional clock. It is used to clock the watchdog timer internal logic.
- Interface clock domain: WDTi_ICLK is the watchdog timer interface clock. It is used to synchronize the watchdog timer L4 port to the L4 interconnect. All accesses from the interconnect are synchronous to WDTi_ICLK.

Table 22-82 lists the source clocks for each watchdog timer in the device. For more information about clock control and domains, see Section 3.1.1.1, *Clock Management* in Chapter 3, *Power, Reset, and Clock Management*.

From a global system power-management perspective, when one or both of the watchdog timer clocks is no longer required, the watchdog timers can be deactivated at the PRCM module level in the corresponding registers.

At the PRCM module level, when the conditions to shut off the PRCM module functional or interface output clocks are met (for more information, see the , *Clock Domain Level Clock Management*), the PRCM module automatically launches a hardware handshake protocol to ensure the watchdog timer is ready to have its clocks switched off. Namely, the PRCM module asserts an IDLE request to the watchdog timer.

Although this handshake is a hardware function and out of software control, the way the watchdog timer acknowledges the PRCM IDLE request is configurable through the WDT_WDSC[4:3] IDLEMODE bit field. Table 22-84 lists the settings and related acknowledgment modes of the IDLEMODE bit field.

Table 22-84. IDLEMODE Settings

IDLEMODE Value	Selected Mode	Description
00	Force-idle	The watchdog timer unconditionally acknowledges the IDLE request from the PRCM module, regardless of its internal operations. This mode must be used carefully, because it does not prevent loss of data when the clock is switched off.
01	No-idle	The watchdog timer never acknowledges an IDLE request from the PRCM module. This mode is safe from a module point of view, because it ensures that the clocks remain active. It is not efficient from a power-saving perspective, however, because it does not allow the PRCM module output clock to be shut off and thus the power domain to be set to a lower power state.
10	Smart-idle	The watchdog timer acknowledges the IDLE request, basing its decision on its internal activity. The acknowledge signal is asserted only when all pending transactions and IRQ requests are treated. This is the best approach for efficient system power management.
11	Smart-idle wakeup-capable mode	The watchdog timer acknowledges the IDLE request, basing its decision on its internal activity. The timer generates (IRQ-request-related) wake-up events when in IDLE state if the WDT_WIRQWAKEEN[1:0] bits are set to 1.

22.3.4.1.1 Wake-Up Capability

If the WDT_WDSC[4:3] IDLEMODE bit field sets smart-idle wakeup-capable mode (= 0 × 3), the timer evaluates its internal capability to have the interface clock switched off. When there is no more internal activity (no pending interrupt sources: match, overflow, or timer capture events), the idle acknowledge signal is asserted and the timer enters into sleep mode, ready to issue a wake-up request. This wake-up request is sent only if the WDT_WIRQWAKEEN[0] OVF_WK_ENA and/or the WDT_WIRQWAKEEN[1] DLY_WK_ENA bits enable the overflow and/or the delay wake-up capability.

22.3.4.2 Interrupts

Table 22-85 list the event flags, and their masks, that cause module interrupts.

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Table 22-85. Watchdog Timer Events

Event Flag	Event Mask	Mapping	Comments
WDT_WIRQSTAT[0] EVENT_OVF	WDT_WIRQENSET/WDT_WIRQENCLR[0] OVF_IT_ENA	WDTi_IRQ	Watchdog timer overflow
WDT_WIRQSTAT[1] EVENT_DLY	WDT_WIRQENSET/WDT_WIRQENCLR[1] DLY_IT_ENA	WDTi_IRQ	Watchdog delay value reached

22.3.4.3 General Watchdog Timer Operation

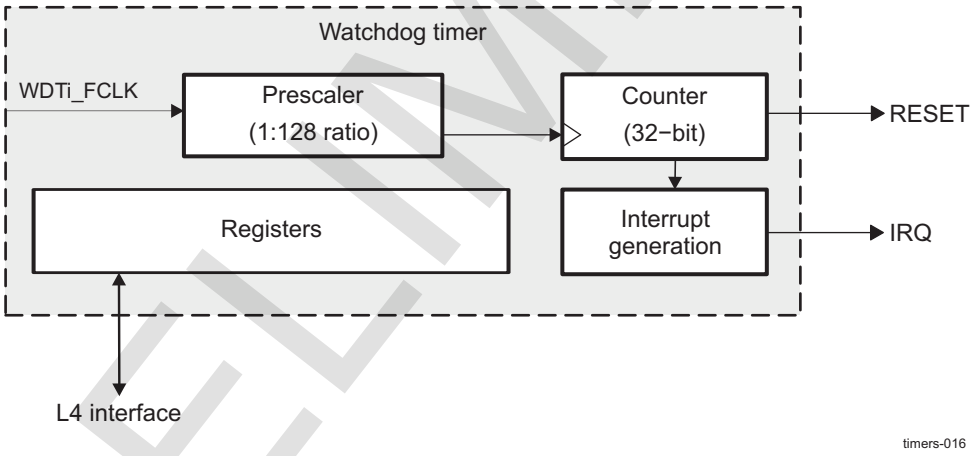
The watchdog timers are based on an upward 32-bit counter coupled with a prescaler. The counter overflow is signaled through two independent signals: a simple reset signal and an interrupt signal, both active low. The use of these signals depends on whether they are connected or not. For this information, see Figure 22-15. The interrupt generation mechanism is controlled through the WDT_WIRQENSET/WDT_WIRQENCLR and WDT_WIRQSTAT registers.

The prescaler ratio can be set from 1 to 128 by accessing the WDT_WCLR[4:2] PTV bit field and the WDT_WCLR[5] PRE bit of the watchdog control register (WDT_WCLR).

The current timer value can be accessed on-the-fly by reading the watchdog timer counter register (WDT_WCRR), modified by accessing the watchdog timer load register (WDT_WLDR) (no on-the-fly update), or reloaded by following a specific reload sequence on the watchdog timer trigger register (WDT_WTGR). A start/stop sequence applied to the watchdog timer start/stop register (WDT_WSPR) can start and stop the watchdog timers.

Figure 22-17 is a functional block diagram of the watchdog timer.

Figure 22-17. 32-Bit Watchdog Timer Functional Block Diagram



22.3.4.4 Reset Context

The watchdog timers are enabled after reset. Table 22-86 lists the default reset values of the two watchdog timer load registers (the WDT_WLDR) and prescaler ratios (the WDT_WCLR[4:2] PTV bit field). To get these values, software must read the corresponding WDT_WCLR[4:2] PTV bit field and the 32-bit register to retrieve the static configuration of the module.

Table 22-86. Count and Prescaler Default Reset Values

Timer	WDT_WLDR Reset Value	PTV Reset Value
MPU WDT (WDT2)	0xFFFB 0000	0
IVA3 WDT (WDT3)	0xFFFB 0000	0

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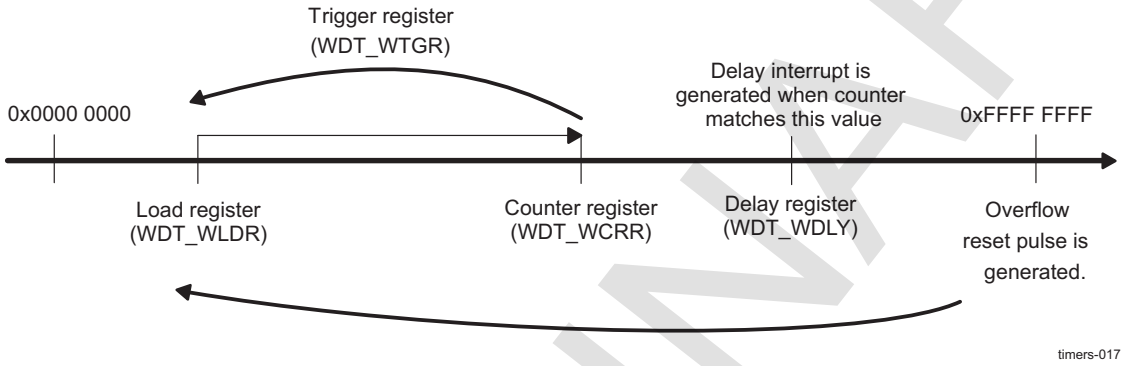
22.3.4.5 Overflow/Reset Generation

When the watchdog timer counter register (WDT_WCRR) overflows, an active-low reset pulse is generated to the PRCM module. This pulse is one prescaled timer clock cycle wide and occurs at the same time as the timer counter overflow.

After reset generation, the counter is automatically reloaded with the value stored in the watchdog load register (WDT_WLDR) and the prescaler is reset (the prescaler ratio remains unchanged). When the reset pulse output is generated, the timer counter begins incrementing again.

Figure 22-18 shows a general functional view of the watchdog timers.

Figure 22-18. Watchdog Timers General Functional View



22.3.4.6 Prescaler Value/Timer Reset Frequency

Each watchdog timer is composed of a prescaler stage and a timer counter.

The timer rate is defined by the following values:

- Value of the prescaler fields (the WDT_WCLR[5] PRE bit and the WDT_WCLR[4:2] PTV bit field)
- Value loaded into the timer load register (WDT_WLDR)

The prescaler stage is clocked with the timer clock and acts as a clock divider for the timer counter stage. The ratio is managed by accessing the ratio definition field (the WDT_WCLR[4:2] PTV bit field) and is enabled with the WDT_WCLR[5] PRE bit.

Table 22-87 lists the prescaler clock ratio values.

Table 22-87. Prescaler Clock Ratio Values

WDT_WCLR[5] PRE	WDT_WCLR[4:2] PTV	Clock Divider (PS)
0	X	1
1	0	1
1	1	2
1	2	4
1	3	8
1	4	16
1	5	32
1	6	64
1	7	128

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Thus the watchdog timer overflow rate is expressed as:

OVF_Rate = (0xFFFF FFFF – WDT_WLDR + 1) × (wd-functional clock period) × PS

where wd-functional clock period = 1/(wd-functional clock frequency) and PS = $2^{(PTV)}$

CAUTION

Internal resynchronization causes some latency in any software write to WDT_WSPR before WDT_WSPR is updated with the programmed value:

1.5 × functional clock cycles ≤ write_WDT_WSPR_latency ≤ 2.5 × functional clock cycles

Remember to consider this latency whenever the watchdog timer must be started or stopped.

For example, for a timer clock input of 32 kHz with a prescaler ratio value of 0x1 (clock divided by 2) and WDT_WCLR[5] PRE = 1 (clock divider enabled), the reset period is as listed in Table 22-88.

Table 22-88. Reset Period Examples

WDT_WLDR Value	Reset Period
0x0000 0000	74 h 56 min
0xFFFF 0000	4 s
0xFFFF FFF0	1 ms
0xFFFF FFFF	62.5 us

CAUTION

- Ensure that the reloaded value allows the correct operation of the application. When a watchdog timer is enabled, software must periodically trigger a reload before the counter overflows. Hence, the value of the WDT_WLDR[31:0] bit field must be chosen according to the ongoing activity preceding the watchdog reload.
- Due to design reasons, WDT_WLDR[31:0] = 0xFFFF FFFF is a special case, although such a value of WDT_WLDR is meaningless. When WDT_WLDR is programmed with the overflow value, a triggering event generates a reset/interrupt one functional clock cycle later, even if the watchdog timer is stopped.

Table 22-89 lists the default reset periods for the watchdog timers.

Table 22-89. Default Watchdog Timer Reset Periods

Watchdog Timers	Clock Source	Default Reset Period
MPU/IVA3 WDTs	32 kHz	10 s

22.3.4.7 Triggering a Timer Reload

To reload the timer counter and reset the prescaler before reaching overflow, a reload command is executed by accessing the watchdog timer trigger register (WDT_WTGR) using a specific reload sequence.

The specific reload sequence is performed whenever the written value on the WDT_WTGR register differs from its previous value. In this case, reload is executed in the same way as an overflow autoreload, but without the generation of a reset pulse.

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The timer counter is loaded with the value of the watchdog timer load register (the WDT_WLDR[31:0] TIMER_LOAD bit field), and the prescaler is reset.

22.3.4.8 Start/Stop Sequence for Watchdog Timers (Using the WDT_WSPR Register)

To start and stop a watchdog timer, access must be made through the start/stop register (WDT_WSPR) using a specific sequence.

To disable the timer, follow this sequence:

1. Write 0xXXXX AAAA in WDT_WSPR.
2. Write 0xXXXX 5555 in WDT_WSPR.

To enable the timer, follow this sequence:

1. Write 0xXXXX BBBB in WDT_WSPR.
2. Write 0xXXXX 4444 in WDT_WSPR.

All other write sequences on the WDT_WSPR register have no effect on the start/stop feature of the module.

22.3.4.9 Modifying Timer Count/Load Values and Prescaler Setting

To modify the timer counter value (the WDT_WCRR register), prescaler ratio (the WDT_WCLR[4:2] PTV bit field), delay configuration value (the WDT_WDLY[31:0] DLY_VALUE bit field), or the load value (the WDT_WLDR[31:0] TIMER_LOAD bit field), the watchdog timer must be disabled by using the start/stop sequence (the WDT_WSPR register).

After a write access, the load register value and prescaler ratio registers are updated immediately, but new values are considered only after the next consecutive counter overflow or after a new trigger command (the WDT_WTGR register).

22.3.4.10 Watchdog Counter Register Access Restriction (WDT_WCRR Register)

A 32-bit shadow register is implemented to read a coherent value of the WDT_WCRR register because the WDT_WCRR register is directly related to the timer counter value and is updated on the timer clock (WDT_FCLK). The shadow register is updated by a 16-bit LSB read command.

NOTE: Although the L4 clock (WDT_ICLK) is completely asynchronous with the timer clock (WDT_FCLK), some synchronization is performed to ensure that the value of the WDT_WCRR register is not read while it is being incremented.

When 32-bit read access is performed, the shadow register is not updated. Read access is performed directly from the accessed register.

To ensure that a coherent value is read inside WDT_WCRR, the first read access is to the lower 16 bits (offset = 0x08), followed by read access to the upper 16 bits (offset = 0x0A).

22.3.4.11 Watchdog Timer Interrupt Generation

When an interrupt source occurs, the interrupt status bit (the WDT_WIRQSTAT[0] EVENT_OVF or WDT_WIRQSTAT[1] EVENT_DLY bit) is set to 1. The output interrupt line (WDTi_IRQ) is asserted (active low) when status (the EVENT_xxx bit) and enable (the xxx_IT_ENA bit) flags are set to 1; the order is not relevant. Writing 1 to the enable bit (the status is already set at 1) also triggers the interrupt in the normal order (enable first, status next). The pending interrupt event is cleared when the set status bit is overwritten by a value of 1 by a write command in the WDT_WIRQSTAT register. Reading the WDT_WIRQSTAT register and writing the value back allows a fast interrupt acknowledge process.

The watchdog timer issues an overflow interrupt if this interrupt is enabled in the watchdog interrupt enable register (WDT_WIRQENSET[0] OVF_IT_ENA = 1). When the overflow occurs, the interrupt status bit (the WDT_WIRQSTAT[0] EVENT_OVF bit) is set to 1. The output interrupt line (WDT_IRQ) is asserted (active low) when status (EVENT_OVF) and enable (OVF_IT_ENA) flags are set to 1; the order is not relevant. This interrupt can be disabled by setting the WDT_WIRQENCLR[0] OVF_IT_ENA bit to 1.

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The watchdog can issue the delay interrupt if this interrupt is enabled in the interrupt enable register (WDT_WIRQENSET[1] DLY_IT_ENA = 1). When the counter is running and the counter value matches the value stored in the delay configuration register (WDT_WDLY), the corresponding interrupt status bit is set in the watchdog status register (WDT_WIRQSTAT) and the output interrupt line is asserted (active low) when the flag (EVENT_DLY) and enable (DLY_IT_ENA) bits are 1 in the WDT_WIRQSTAT and WDT_WIRQENSET registers, respectively; the order (normally enable, then flag), is not relevant. This interrupt can be disabled by setting the WDT_WIRQENCLR[1] DLY_IT_ENA bit to 1.

NOTE: Writing 0 to the WDT_WIRQSTAT[0] EVENT_OVF bit or the WDT_WIRQSTAT[1] EVENT_DLY bit has no effect.

The two clock domains are resynchronized because the interrupt event is generated on the functional clock domain (WDTi_FCLK) during the updating of the interrupt status register (WDT_WIRQSTAT).

The WDT_WDLY register is used to specify the value of the delay configuration register. The delay time to interrupt is the difference between the reload value stored in the counter load register (WDT_WLDR) and the programmed value in this register (WDT_WDLY).

Use the following formula to estimate the delay time:

Delay time period = (WDT_WDLY – WDT_WLDR + 1) × Timer clock period × Clock divider

Where:

- Timer clock period = 1/(Timer clock frequency)
- Clock divider = 2PTV

If the counter value (WDT_WCRR) reaches the programmed value (WDT_WDLY), the status bit (EVENT_DLY) gets set in the interrupt status register (WDT_WIRQSTAT), and an interrupt occurs if the corresponding enable bit is set in the interrupt enable register (WDT_WIRQENSET).

CAUTION

If the reload event occurs (after a triggering sequence or after a reset sequence) before reaching the programmed value (WDT_WDLY[31:0] WDLY_VALUE), no interrupt is generated.

Also, no interrupt is generated if the value programmed in the delay configuration register (WDT_WDLY) is less than the value stored in the counter load register (WDT_WLDR).

22.3.4.12 Watchdog Timers Under Emulation

During emulation mode, the watchdog timer can/cannot continue running, according to the value of the WDT_WDSC[5] EMUFREE bit of the system configuration register (WDT_WDSC).

- When EMUFREE is 1, watchdog timer execution is not stopped and a reset pulse is still generated when overflow is reached.
- When EMUFREE is 0, the counters (prescaler/timer) are frozen and incrementation restarts after exiting from emulation mode.

22.3.4.13 Accessing Watchdog Timer Registers

Posted/nonposted selection applies only to functional registers that require synchronization on/from the timer functional clock domain (WDTi_FCLK). For write/read operation, the following registers are affected:

- WDT_WCLR
- WDT_WCRR
- WDT_WLDR
- WDT_WTGR
- WDT_WDLY

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- WDT_WSPR

NOTE: To ensure completion of successive writes in a WDT2 or WDT3 functional clock domain register, user software must poll the appropriate WDT_WWPS status bit.

NOTE: To ensure coherent reading when a read transaction immediately follows a write access to a WDT2 or WDT3 functional clock domain register, user software must check the appropriate WDT_WWPS status bit.

The timer interface clock domain synchronous registers are not affected by the posted mode mechanism; the write/read operation is effective and acknowledged (command accepted) after one WDT_ICLK cycle from the command assertion. The timer interface clock domain synchronous registers are:

- WDT_WIDR
- WDT_WDSC
- WDT_WDST
- WDT_WIRQSTATRAW
- WDT_WIRQSTAT
- WDT_WIRQENSET
- WDT_WIRQENCLR
- WDT_WIRQWAKEEN
- WDT_WWPS

NOTE: Accesses to WDT2 and WDT3 functional clock domain synchronous registers are posted.

22.3.5 Watchdog Timer Low-Level Programming Model

This section covers the low-level hardware programming sequences for configuration and use of the module.

22.3.5.1 Global Initialization

22.3.5.1.1 Surrounding Modules Global Initialization

This section identifies the requirements for initializing the surrounding modules when the watchdog timer is to be used for the first time after a device reset. This initialization of surrounding modules is based on the integration and environment of the watchdog timer (see Table 22-90). For more information, see Section 22.3.2, *Watchdog Timer Environment*, and Section 22.3.3, *Watchdog Timer Integration.*

Table 22-90. Global Initialization of Surrounding Modules

Surrounding Modules	Comments
PRCM	The module interface and functional clocks must be enabled. for more information about the module configuration. For more information about the module configuration, see Section 3.1.1.1.2, *Module Level Clock Management*, in Chapter 3, *Power, Reset, and Clock Management*.
Control module	Module-specific pad muxing must be set in the control module. For more information about the module configuration, see Section 18.4.8, *PAD Functional Multiplexing and Configuration* in Chapter 18, *Control Module*.
MPU INTC	The MPU INTC configuration must be performed to enable the interrupts from the watchdog timer. See Section 4.4.3, *Interrupt Controller Registers* in Chapter 4, *Cortex-A9 MPU Subsystem*.

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22.3.5.1.2 Watchdog Timer Module Global Initialization

22.3.5.1.2.1 Main Sequence – Watchdog Timer Module Global Initialization

Table 22-91 lists the steps for initializing the watchdog timer module when the module is to be used for the first time.

Table 22-91. Watchdog Timer Module Global Initialization

Step	Register/Bit Field/Programming Model	Value
Execute software reset.	WDT_WDSC[1] SOFTRESET	0x1
Wait until reset release?	WDT_WDSC[1] SOFTRESET	0x0
Configure idle mode.	WDT_WDSC[4:3] IDLEMODE	xx
Enable delay wakeup.	WDT_WIRQWAKEEN[1] DLY_WK_ENA	0x1
Enable overflow wakeup.	WDT_WIRQWAKEEN[0] OVF_WK_ENA	0x1
Enable delay interrupt.	WDT_WIRQENSET[1] ENABLE_DLY	0x1
Enable overflow interrupt.	WDT_WIRQENSET[0] ENABLE_OVF	0x1

22.3.5.2 Operational Mode Configuration

22.3.5.2.1 Watchdog Timer Basic Configuration

22.3.5.2.1.1 Main Sequence – Watchdog Timer Basic Configuration

Table 22-92 lists the steps for the basic configuration of the watchdog timer.

Table 22-92. Watchdog Timer Basic Configuration

Step	Register/Bit Field/Programming Model	Value
Disable the watchdog timer.	See Section 22.3.5.2.1.2.	
Set prescaler value.	WDT_WCLR[4:2] PTV	xxx
Enable prescaler.	WDT_WCLR[5] PRE	0x1
Load delay configuration value.	WDT_WDLY	xxx
Load timer counter value.	WDT_WCRR	xxx
Enable the watchdog timer.	See Section 22.3.5.2.1.3.	

22.3.5.2.1.2 Subsequence – Disable the Watchdog Timer

Table 22-93 lists the steps to disable the watchdog timer.

Table 22-93. Disable the Watchdog Timer

Step	Register/Bit Field/Programming Model	Value
Write disable sequence Data1.	WDT_WSPR	0xXXXX AAAA
Write disable sequence Data2.	WDT_WSPR	0xXXXX 5555

22.3.5.2.1.3 Subsequence – Enable the Watchdog Timer

Table 22-94 lists the steps to enable the watchdog timer.

Table 22-94. Enable the Watchdog Timer

Step	Register/Bit Field/Programming Model	Value
Write enable sequence Data1.	WDT_WSPR	0xXXXX BBBB
Write enable sequence Data2.	WDT_WSPR	0xXXXX 4444

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22.3.6 Watchdog Timer Register Manual

22.3.6.1 Watchdog Timer Instance Summary

Table 22-95 lists the base address and address space for the watchdog timer module instances.

Table 22-95. Watchdog Timer Instance Summary

Module Name	Base Address L4 Interconnect	Base Address L3 Interconnect	Base Address Cortex-A9 Private Access	Base Address DSP Private Access	Size
WDTIMER2	0x4A31 4000	-	-	-	4KB
WDTIMER3	-	0x4903 0000	0x4013 0000	0x01D3 0000	4KB

NOTE: Private access is an access which is not using the L3/L4 interconnects.

22.3.6.2 Watchdog Timer Registers

22.3.6.2.1 Watchdog Timer Register Summary

CAUTION

The watchdog timers registers are limited to 32-bit and 16-bit data accesses; 8-bit access is not allowed and can corrupt register content.

Table 22-96 lists the WDTIMER2 registers.

Table 22-96. WDTIMER2 Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	Physical Address L4 Interconnect
WDT_WIDR	R	32	0x0000 0000	0x4A31 4000
WDT_WDSC	RW	32	0x0000 0010	0x4A31 4010
WDT_WDST	R	32	0x0000 0014	0x4A31 4014
WDT_WISR	RW	32	0x0000 0018	0x4A31 4018
WDT_WIER	RW	32	0x0000 001C	0x4A31 401C
WDT_WWER	RW	32	0x0000 0020	0x4A31 4020
WDT_WCLR	RW	32	0x0000 0024	0x4A31 4024
WDT_WCRR	RW	32	0x0000 0028	0x4A31 4028
WDT_WLDR	RW	32	0x0000 002C	0x4A31 402C
WDT_WTGR	RW	32	0x0000 0030	0x4A31 4030
WDT_WWPS	R	32	0x0000 0034	0x4A31 4034
WDT_WDLY	RW	32	0x0000 0044	0x4A31 4044
WDT_WSPR	RW	32	0x0000 0048	0x4A31 4048
RESERVED			0x0000 0050	0x4A31 4050
WDT_WIRQSTATRAW	RW	32	0x0000 0054	0x4A31 4054
WDT_WIRQSTAT	RW	32	0x0000 0058	0x4A31 4058
WDT_WIRQENSET	RW	32	0x0000 005C	0x4A31 405C
WDT_WIRQENCLR	RW	32	0x0000 0060	0x4A31 4060
WDT_WIRQWAKEEN	RW	32	0x0000 0064	0x4A31 4064

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Table 22-97 lists the WDTIMER3 registers.

Table 22-97. WDTIMER3 Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	Physical Address L3 Interconnect	Physical Address Cortex-A9 Private Access	Physical Address DSP Private Access
WDT_WIDR	R	32	0x0000 0000	0x4903 0000	0x4013 0000	0x01D3 0000
WDT_WDSC	RW	32	0x0000 0010	0x4903 0010	0x4013 0010	0x01D3 0010
WDT_WDST	R	32	0x0000 0014	0x4903 0014	0x4013 0014	0x01D3 0014
WDT_WISR	RW	32	0x0000 0018	0x4903 0018	0x4013 0018	0x01D3 0018
WDT_WIER	RW	32	0x0000 001C	0x4903 001C	0x4013 001C	0x01D3 001C
WDT_WWER	RW	32	0x0000 0020	0x4903 0020	0x4013 0020	0x01D3 0020
WDT_WCLR	RW	32	0x0000 0024	0x4903 0024	0x4013 0024	0x01D3 0024
WDT_WCRR	RW	32	0x0000 0028	0x4903 0028	0x4013 0028	0x01D3 0028
WDT_WLDR	RW	32	0x0000 002C	0x4903 002C	0x4013 002C	0x01D3 002C
WDT_WTGR	RW	32	0x0000 0030	0x4903 0030	0x4013 0030	0x01D3 0030
WDT_WWPS	R	32	0x0000 0034	0x4903 0034	0x4013 0034	0x01D3 0034
WDT_WDLY	RW	32	0x0000 0044	0x4903 0044	0x4013 0044	0x01D3 0044
WDT_WSPR	RW	32	0x0000 0048	0x4903 0048	0x4013 0048	0x01D3 0048
RESERVED			0x0000 0050	0x4903 0050	0x4013 0050	0x01D3 0050
WDT_WIRQSTATRAW	RW	32	0x0000 0054	0x4903 0054	0x4013 0054	0x01D3 0054
WDT_WIRQSTAT	RW	32	0x0000 0058	0x4903 0058	0x4013 0058	0x01D3 0058
WDT_WIRQENSET	RW	32	0x0000 005C	0x4903 005C	0x4013 005C	0x01D3 005C
WDT_WIRQENCLR	RW	32	0x0000 0060	0x4903 0060	0x4013 0060	0x01D3 0060
WDT_WIRQWAKEEN	RW	32	0x0000 0064	0x4903 0064	0x4013 0064	0x01D3 0064

NOTE:

- The WDT_WISR and WDT_WIRQSTATRAW registers have the same functionality. The WDT_WISR register is used for software backward compatibility.
- The WDT_WIER and WDT_WIRQENSET/WDT_WIRQENCLR registers have the same functionality. The WDT_WIER register is used for software backward compatibility.
- The WDT_WWER and WDT_WIRQWAKEEN registers have the same functionality. The WDT_WWER is used for software backward compatibility.
- The WDT_WIRQSTATRAW and WDT_WIRQSTAT registers give the same information when read. The WDT_WIRQSTATRAW register is used for debug.

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22.3.6.2.2 Watchdog Timer Register Description

through describe the watchdog timer registers.

Table 22-98. WDT_WIDR

Address Offset	0x0000 0000		
Physical Address	0x4A31 4000 0x4903 0000 0x4013 0000 0x01D3 0000	**Instance**	WDTIMER2_L4 WDTIMER3_L3 WDTIMER3_CORTEX-A9 WDTIMER3_DSP
Description	IP revision identifier		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP Revision	R	0x– [1]

[1] TI internal data

Table 22-99. Register Call Summary for Register WDT_WIDR

Watchdog Timers

- Accessing Watchdog Timer Registers: [0]
- Watchdog Timer Register Summary: [1] [2]

Table 22-100. WDT_WDSC

Address Offset	0x0000 0010		
Physical Address	0x4A31 4010 0x4903 0010 0x4013 0010 0x01D3 0010	**Instance**	WDTIMER2_L4 WDTIMER3_L3 WDTIMER3_CORTEX-A9 WDTIMER3_DSP
Description	This register controls the various parameters of the L4 interface.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																										EMUFREE	IDLEMODE	RESERVED	SOFTRESET	RESERVED	

Bits	Field Name	Description	Type	Reset
31:6	RESERVED	Write os for future compatibility. Reads return 0.	R	0x0000000
5	EMUFREE	Emulation mode 0x0: Timer counter frozen in emulation 0x1: Timer counter free-running in emulation	RW	0

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Bits	Field Name	Description	Type	Reset
4:3	IDLEMODE	Configuration of the local target state management mode. By definition, target can handle read/write transaction as long as it is out of IDLE state. 0x0: Force-idle mode: local target IDLE state follows (acknowledges) the system idle requests unconditionally, that is, regardless of the IP module internal requirements. Backup mode, for debug only. 0x1: No-idle mode: local target never enters IDLE state. Backup mode, for debug only. 0x2: Smart-idle mode: local target IDLE state eventually follows (acknowledges) the system idle requests, depending on the IP module internal requirements. IP module should not generate (IRQ- or DMA-request-related) wake-up events. 0x3: Smart-idle wake-up-capable mode: local target IDLE state eventually follows (acknowledges) the system idle requests, depending on the IP module internal requirements. IP module may generate (IRQ- or DMA-request-related) wake-up events when in IDLE state. Mode is relevant only if the appropriate IP module *swake-up* output(s) is (are) implemented.	RW	0x2
2	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0
1	SOFTRESET	Software reset. (Optional) Read 0x0: Reset done, no pending action Write 0x0: No action Write 0x1: Initiate software reset. Read 0x1: Reset (software or other) ongoing	RW	0
0	RESERVED	Write os for future compatibility. Reads return 0.	R	0

Table 22-101. Register Call Summary for Register WDT_WDSC

Watchdog Timers

- Power Management: [0]
- Wake-Up Capability: [1]
- Watchdog Timers Under Emulation: [2] [3]
- Accessing Watchdog Timer Registers: [4]
- Watchdog Timer Module Global Initialization: [5] [6] [7]
- Watchdog Timer Register Summary: [8] [9]

Table 22-102. WDT_WDST

Address Offset	0x0000 0014		
Physical Address	0x4A31 4014 0x4903 0014 0x4013 0014 0x01D3 0014	**Instance**	WDTIMER2_L4 WDTIMER3_L3 WDTIMER3_CORTEX-A9 WDTIMER3_DSP
Description	This register provides status information about the module.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															RESETDONE

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Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reads return 0.	R	0x0000 0000
0	RESETDONE	Internal module reset monitoring Read 0x0: Internal module reset is ongoing. Read 0x1: Reset completed	R	1

Table 22-103. Register Call Summary for Register WDT_WDST

Watchdog Timers
- Accessing Watchdog Timer Registers: [0]
- Watchdog Timer Register Summary: [1] [2]

Table 22-104. WDT_WISR

Address Offset	0x0000 0018		
Physical Address	0x4A31 4018 0x4903 0018 0x4013 0018 0x01D3 0018	**Instance**	WDTIMER2_L4 WDTIMER3_L3 WDTIMER3_CORTEX-A9 WDTIMER3_DSP
Description	This register shows which interrupt events are pending inside the module.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														DLY_IT_FLAG	OVF_IT_FLAG

Bits	Field Name	Description	Type	Reset
31:2	RESERVED	Reads return 0.	R	0x0000 0000
1	DLY_IT_FLAG	Pending delay interrupt status. Read 0x0: No delay interrupt pending Write 0x0: Status unchanged Write 0x1: Status bit cleared Read 0x1: Delay interrupt pending	RW W1toClr	0
0	OVF_IT_FLAG	Pending overflow interrupt status. Read 0x0: No overflow interrupt pending Write 0x0: Status unchanged Write 0x1: Status bit cleared Read 0x1: Overflow interrupt pending	RW W1toClr	0

Table 22-105. Register Call Summary for Register WDT_WISR

Watchdog Timers
- Watchdog Timer Register Summary: [0] [1] [2] [3]

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Table 22-106. WDT_WIER

Address Offset	0x0000 001C		
Physical Address	0x4A31 401C 0x4903 001C 0x4013 001C 0x01D3 001C	**Instance**	WDTIMER2_L4 WDTIMER3_L3 WDTIMER3_CORTEX-A9 WDTIMER3_DSP
Description	This register controls (enable/disable) the interrupt events.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														DLY_IT_ENA	OVF_IT_ENA

Bits	Field Name	Description	Type	Reset
31:2	RESERVED	Reads return 0.	R	0x0000 0000
1	DLY_IT_ENA	Delay interrupt enable/disable 0x0: Disable delay interrupt. 0x1: Enable delay interrupt.	RW	0
0	OVF_IT_ENA	Overflow interrupt enable/disable 0x0: Disable overflow interrupt. 0x1: Enable overflow interrupt.	RW	0

Table 22-107. Register Call Summary for Register WDT_WIER

Watchdog Timers

- Watchdog Timer Register Summary: [0] [1] [2] [3]

Table 22-108. WDT_WWER

Address Offset	0x0000 0020		
Physical Address	0x4A31 4020 0x4903 0020 0x4013 0020 0x01D3 0020	**Instance**	WDTIMER2_L4 WDTIMER3_L3 WDTIMER3_CORTEX-A9 WDTIMER3_DSP
Description	This register controls (enable/disable) the wake-up events.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														DLY_WK_ENA	OVF_WK_ENA

Bits	Field Name	Description	Type	Reset
31:2	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0000 0000
1	DLY_WK_ENA	Delay wake-up enable 0x0: Disable delay wakeup. 0x1: Enable delay wakeup.	RW	0

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Bits	Field Name	Description	Type	Reset
0	OVF_WK_ENA	Overflow wake-up enable 0x0: Disable overflow wakeup. 0x1: Enable overflow wakeup.	RW	0

Table 22-109. Register Call Summary for Register WDT_WWER

Watchdog Timers

- Watchdog Timer Register Summary: [0] [1] [2] [3]

Table 22-110. WDT_WCLR

Address Offset	0x0000 0024		
Physical Address	0x4A31 4024 0x4903 0024 0x4013 0024 0x01D3 0024	**Instance**	WDTIMER2_L4 WDTIMER3_L3 WDTIMER3_CORTEX-A9 WDTIMER3_DSP
Description	This register controls the prescaler stage of the counter.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								PRE	PTV				RESERVED		

Bits	Field Name	Description	Type	Reset
31:6	RESERVED	Reads return 0.	R	0x0000000
5	PRE	Prescaler enable/disable configuration 0x0: Prescaler disabled 0x1: Prescaler enabled	RW	1
4:2	PTV	Prescaler value The timer counter is prescaled with the value: 2**PTV. Example: PTV = 3 - counter increases value if started after 8 functional clock periods. On reset, it is loaded from PI_PTV_RESET_VALUE input port.	RW	0x0
1:0	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0

Table 22-111. Register Call Summary for Register WDT_WCLR

Watchdog Timers

- General Watchdog Timer Operation: [0] [1] [2]
- Reset Context: [3] [4]
- Prescaler Value/Timer Reset Frequency: [5] [6] [7] [8] [9] [10] [11]
- Modifying Timer Count/Load Values and Prescaler Setting: [12]
- Accessing Watchdog Timer Registers: [13]
- Watchdog Timer Basic Configuration: [14] [15]
- Watchdog Timer Register Summary: [16] [17]

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Table 22-112. WDT_WCRR

Address Offset	0x0000 0028		
Physical Address	0x4A31 4028 0x4903 0028 0x4013 0028 0x01D3 0028	**Instance**	WDTIMER2_L4 WDTIMER3_L3 WDTIMER3_CORTEX-A9 WDTIMER3_DSP
Description	This register holds the value of the internal counter.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TIMER_COUNTER																															

Bits	Field Name	Description	Type	Reset
31:0	TIMER_COUNTER	Value of the timer counter register	RW	0x0000 0000

Table 22-113. Register Call Summary for Register WDT_WCRR

Watchdog Timers

- General Watchdog Timer Operation: [0]
- Overflow/Reset Generation: [1]
- Modifying Timer Count/Load Values and Prescaler Setting: [2]
- Watchdog Counter Register Access Restriction (WDT_WCRR Register): [3] [4] [5] [6]
- Watchdog Timer Interrupt Generation: [7]
- Accessing Watchdog Timer Registers: [8]
- Watchdog Timer Basic Configuration: [9]
- Watchdog Timer Register Summary: [10] [11]

Table 22-114. WDT_WLDR

Address Offset	0x0000 002C		
Physical Address	0x4A31 402C 0x4903 002C 0x4013 002C 0x01D3 002C	**Instance**	WDTIMER2_L4 WDTIMER3_L3 WDTIMER3_CORTEX-A9 WDTIMER3_DSP
Description	This register holds the timer load value.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TIMER_LOAD																															

Bits	Field Name	Description	Type	Reset
31:0	TIMER_LOAD	Value of the timer load register	RW	0x0000 0000

Table 22-115. Register Call Summary for Register WDT_WLDR

Watchdog Timers

- General Watchdog Timer Operation: [0]
- Reset Context: [1] [2]
- Overflow/Reset Generation: [3]
- Prescaler Value/Timer Reset Frequency: [4] [5] [6] [7] [8] [9] [10]
- Triggering a Timer Reload: [11]
- Modifying Timer Count/Load Values and Prescaler Setting: [12]
- Watchdog Timer Interrupt Generation: [13] [14] [15]
- Accessing Watchdog Timer Registers: [16]
- Watchdog Timer Register Summary: [17] [18]

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Table 22-116. WDT_WTGR

Address Offset	0x0000 0030		
Physical Address	0x4A31 4030 0x4903 0030 0x4013 0030 0x01D3 0030	**Instance**	WDTIMER2_L4 WDTIMER3_L3 WDTIMER3_CORTEX-A9 WDTIMER3_DSP
Description	Writing a different value than the one already written in this register does a watchdog counter reload.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TTGR_VALUE																															

Bits	Field Name	Description	Type	Reset
31:0	TTGR_VALUE	Value of the trigger register	RW	0x0000 0000

Table 22-117. Register Call Summary for Register WDT_WTGR

Watchdog Timers

- General Watchdog Timer Operation: [0]
- Triggering a Timer Reload: [1] [2]
- Modifying Timer Count/Load Values and Prescaler Setting: [3]
- Accessing Watchdog Timer Registers: [4]
- Watchdog Timer Register Summary: [5] [6]

Table 22-118. WDT_WWPS

Address Offset	0x0000 0034		
Physical Address	0x4A31 4034 0x4903 0034 0x4013 0034 0x01D3 0034	**Instance**	WDTIMER2_L4 WDTIMER3_L3 WDTIMER3_CORTEX-A9 WDTIMER3_DSP
Description	This register contains the write posting bits for all writeable functional registers.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																										W_PEND_WDLY	W_PEND_WSPR	W_PEND_WTGR	W_PEND_WLDR	W_PEND_WCRR	W_PEND_WCLR

Bits	Field Name	Description	Type	Reset
31:6	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0000000
5	W_PEND_WDLY	Write pending for register WDLY Read 0x0: No register write pending Read 0x1: Register write pending	R	0
4	W_PEND_WSPR	Write pending for register WSPR Read 0x0: No register write pending Read 0x1: Register write pending	R	0
3	W_PEND_WTGR	Write pending for register WTGR Read 0x0: No register write pending Read 0x1: Register write pending	R	0

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Bits	Field Name	Description	Type	Reset
2	W_PEND_WLDR	Write pending for register WLDR Read 0x0: No register write pending Read 0x1: Register write pending	R	0
1	W_PEND_WCRR	Write pending for register WCRR Read 0x0: No register write pending Read 0x1: Register write pending	R	0
0	W_PEND_WCLR	Write pending for register WCLR Read 0x0: No register write pending Read 0x1: Register write pending	R	0

Table 22-119. Register Call Summary for Register WDT_WWPS

Watchdog Timers
- Accessing Watchdog Timer Registers: [0]
- Watchdog Timer Register Summary: [1] [2]

Table 22-120. WDT_WDLY

Address Offset	0x0000 0044		
Physical Address	0x4A31 4044 0x4903 0044 0x4013 0044 0x01D3 0044	**Instance**	WDTIMER2_L4 WDTIMER3_L3 WDTIMER3_CORTEX-A9 WDTIMER3_DSP
Description	This register holds the delay value that controls the internal pre-overflow event detection.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WDLY_VALUE																															

Bits	Field Name	Description	Type	Reset
31:0	WDLY_VALUE	Value of the delay register	RW	0x0000 0000

Table 22-121. Register Call Summary for Register WDT_WDLY

Watchdog Timers
- Modifying Timer Count/Load Values and Prescaler Setting: [0]
- Watchdog Timer Interrupt Generation: [1] [2] [3] [4] [5] [6] [7]
- Accessing Watchdog Timer Registers: [8]
- Watchdog Timer Basic Configuration: [9]
- Watchdog Timer Register Summary: [10] [11]

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Table 22-122. WDT_WSPR

Address Offset	0x0000 0048		
Physical Address	0x4A31 4048 0x4903 0048 0x4013 0048 0x01D3 0048	**Instance**	WDTIMER2_L4 WDTIMER3_L3 WDTIMER3_CORTEX-A9 WDTIMER3_DSP
Description	This register holds the start-stop value that controls the internal start-stop FSM.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WSPR_VALUE																															

Bits	Field Name	Description	Type	Reset
31:0	WSPR_VALUE	Value of the start-stop register	RW	0x0000 0000

Table 22-123. Register Call Summary for Register WDT_WSPR

Watchdog Timers

- General Watchdog Timer Operation: [0]
- Prescaler Value/Timer Reset Frequency: [1] [2]
- Start/Stop Sequence for Watchdog Timers (Using the WDT_WSPR Register): [3] [4] [5] [6] [7] [8]
- Modifying Timer Count/Load Values and Prescaler Setting: [9]
- Accessing Watchdog Timer Registers: [10]
- Watchdog Timer Basic Configuration: [11] [12] [13] [14]
- Watchdog Timer Register Summary: [15] [16]

Table 22-124. WDT_WIRQSTATRAW

Address Offset	0x0000 0054		
Physical Address	0x4A31 4054 0x4903 0054 0x4013 0054 0x01D3 0054	**Instance**	WDTIMER2_L4 WDTIMER3_L3 WDTIMER3_CORTEX-A9 WDTIMER3_DSP
Description	IRQ unmasked status, status set per-event raw interrupt status vector, line 0. Raw status is set even if event is not enabled. Write 1 to set the (raw) status, mostly for debug.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														EVENT_DLY	EVENT_OVF

Bits	Field Name	Description	Type	Reset
31:2	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0000 0000
1	EVENT_DLY	Settable raw status for delay event Read 0x0: No event pending Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending	RW W1toSet	0

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Bits	Field Name	Description	Type	Reset
0	EVENT_OVF	Settable raw status for overflow event Read 0x0: No event pending Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending	RW W1toSet	0

Table 22-125. Register Call Summary for Register WDT_WIRQSTATRAW

Watchdog Timers
- Accessing Watchdog Timer Registers: [0]
- Watchdog Timer Register Summary: [1] [2] [3] [4] [5]

Table 22-126. WDT_WIRQSTAT

Address Offset	0x0000 0058		
Physical Address	0x4A31 4058 0x4903 0058 0x4013 0058 0x01D3 0058	**Instance**	WDTIMER2_L4 WDTIMER3_L3 WDTIMER3_CORTEX-A9 WDTIMER3_DSP
Description	IRQ masked status, status clear per-event enabled interrupt status vector, line 0. Enabled status is not set unless event is enabled. Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, that is, even if not enabled).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														EVENT_DLY	EVENT_OVF

Bits	Field Name	Description	Type	Reset
31:2	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0000 0000
1	EVENT_DLY	Clearable, enabled status for delay event Read 0x0: No (enabled) event pending Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending	RW W1toClr	0
0	EVENT_OVF	Clearable, enabled status for overflow event Read 0x0: No (enabled) event pending Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending	RW W1toClr	0

Table 22-127. Register Call Summary for Register WDT_WIRQSTAT

Watchdog Timers
- Interrupts: [0] [1]
- General Watchdog Timer Operation: [2]
- Watchdog Timer Interrupt Generation: [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13]
- Accessing Watchdog Timer Registers: [14]
- Watchdog Timer Register Summary: [15] [16] [17]

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Table 22-128. WDT_WIRQENSET

Address Offset	0x0000 005C		
Physical Address	0x4A31 405C 0x4903 005C 0x4013 005C 0x01D3 005C	**Instance**	WDTIMER2_L4 WDTIMER3_L3 WDTIMER3_CORTEX-A9 WDTIMER3_DSP
Description	IRQ enable set per-event interrupt enable bit vector, line 0. Write 1 to set (enable interrupt). Readout equal to corresponding _CLR register.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														ENABLE_DLY	ENABLE_OVF

Bits	Field Name	Description	Type	Reset
31:2	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0000 0000
1	ENABLE_DLY	Enable for delay event Read 0x0: Interrupt disabled (masked) Write 0x0: No action Write 0x1: Enable interrupt. Read 0x1: Interrupt enabled	RW W1toSet	0
0	ENABLE_OVF	Enable for overflow event Read 0x0: Interrupt disabled (masked) Write 0x0: No action Write 0x1: Enable interrupt. Read 0x1: Interrupt enabled	RW W1toSet	0

Table 22-129. Register Call Summary for Register WDT_WIRQENSET

Watchdog Timers

- Interrupts: [0] [1]
- General Watchdog Timer Operation: [2]
- Watchdog Timer Interrupt Generation: [3] [4] [5] [6]
- Accessing Watchdog Timer Registers: [7]
- Watchdog Timer Module Global Initialization: [8] [9]
- Watchdog Timer Register Summary: [10] [11] [12]

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Table 22-130. WDT_WIRQENCLR

Address Offset	0x0000 0060		
Physical Address	0x4A31 4060 0x4903 0060 0x4013 0060 0x01D3 0060	**Instance**	WDTIMER2_L4 WDTIMER3_L3 WDTIMER3_CORTEX-A9 WDTIMER3_DSP
Description	IRQ enable clear per-event interrupt enable bit vector, line 0. Write 1 to clear (disable interrupt). Readout equal to corresponding _SET register.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														ENABLE_DLY	ENABLE_OVF

Bits	Field Name	Description	Type	Reset
31:2	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0000 0000
1	ENABLE_DLY	Enable for delay event Read 0x0: Interrupt disabled (masked) Write 0x0: No action Write 0x1: Disable interrupt. Read 0x1: Interrupt enabled	RW W1toClr	0
0	ENABLE_OVF	Enable for overflow event Read 0x0: Interrupt disabled (masked) Write 0x0: No action Write 0x1: Disable interrupt. Read 0x1: Interrupt enabled	RW W1toClr	0

Table 22-131. Register Call Summary for Register WDT_WIRQENCLR

Watchdog Timers

- Interrupts: [0] [1]
- General Watchdog Timer Operation: [2]
- Watchdog Timer Interrupt Generation: [3] [4]
- Accessing Watchdog Timer Registers: [5]
- Watchdog Timer Register Summary: [6] [7] [8]

Table 22-132. WDT_WIRQWAKEEN

Address Offset	0x0000 0064		
Physical Address	0x4A31 4064 0x4903 0064 0x4013 0064 0x01D3 0064	**Instance**	WDTIMER2_L4 WDTIMER3_L3 WDTIMER3_CORTEX-A9 WDTIMER3_DSP
Description	This register controls (enable/disable) the wake-up events.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														DLY_WK_ENA	OVF_WK_ENA

Bits	Field Name	Description	Type	Reset
31:2	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0000 0000
1	DLY_WK_ENA	Enable delay wake-up 0x0: Disable delay wakeup 0x1: Enable delay wakeup	RW	0
0	OVF_WK_ENA	Enable overflow wakeup 0x0: Disable overflow wakeup 0x1: Enable overflow wakeup	RW	0

Table 22-133. Register Call Summary for Register WDT_WIRQWAKEEN

Watchdog Timers

- Power Management: [0]
- Wake-Up Capability: [1] [2]
- Accessing Watchdog Timer Registers: [3]
- Watchdog Timer Module Global Initialization: [4] [5]
- Watchdog Timer Register Summary: [6] [7] [8]

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22.4 32-kHz Synchronized Timer

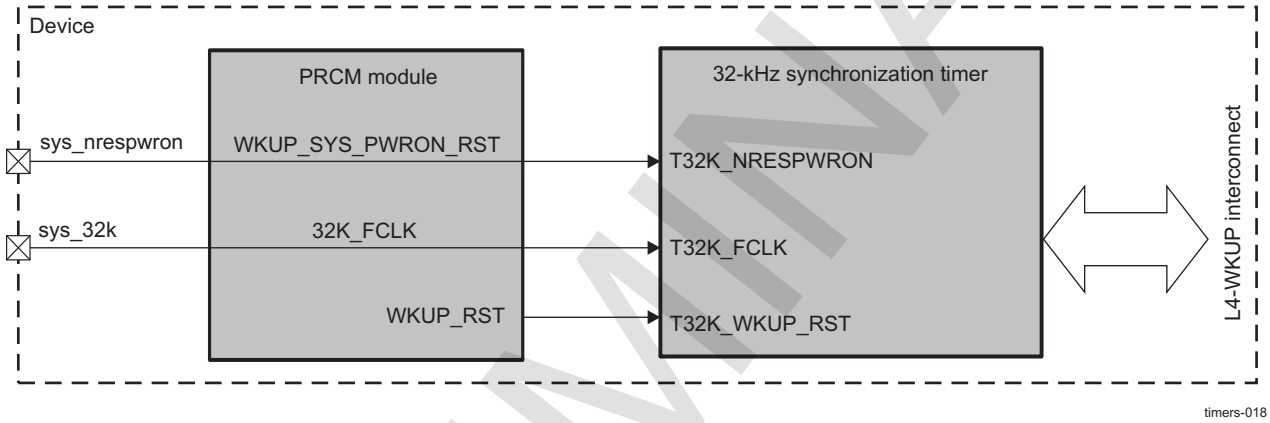
22.4.1 32-kHz Synchronized Timer Overview

The 32-kHz synchronized timer is a 32-bit counter clocked by the falling edge of the 32-kHz system clock. It is reset while the external asynchronous power-up reset (sys_nrespwron) primary input/output (I/O) is active (main device reset). When sys_nrespwron is released (on the rising edge of sys_nrespwron), after three 32-kHz clock periods, the counter starts counting up from the reset value of the counter register on the falling edge of the 32-kHz system clock. After reaching its highest value, the counter wraps back to 0 and starts counting again.

Figure 22-19 is the block diagram of the 32-kHz synchronized timer.

NOTE: sys_nrespwron is an active-low I/O.

Figure 22-19. 32-kHz Synchronized Timer Block Diagram



22.4.1.1 32-kHz Synchronized Timer Features

The main features of the 32-kHz synchronized timer controller are:

- L4 slave interface support:
  - 32-bit data bus width
  - 32-/16-bit access supported
  - 8-bit access not supported
  - 5-bit address bus width
  - Burst mode not supported
- Only read operations are supported on the module registers; no write operation is supported (no error/no action on write).
- Free-running 32-bit upward counter
- Start and keep counting after power-on reset
- Automatic roll over to 0; highest value reached: 0xFFFF FFFF
- On-the-fly read (while counting)

22.4.2 32-kHz Synchronized Timer Environment

The synchronized timer is accessible only through the L4 interface.

22.4.3 32-kHz Synchronized Timer Integration

Table 22-134 through Table 22-136 summarize the integration of the module in the device.

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Table 22-134. Integration Attributes

Module Instance	Attributes		
	Power Domain	Wake-Up Capability	Interconnect
32KTIMER	PD_WKUP	No	L4_WKUP

Table 22-135. Clocks and Resets

Clocks				
Module Instance	Destination Signal Name	Source Signal Name	Source	Description
32KTIMER	T32K_FCLK	32K_FCLK	PRCM	32KTIMER functional clock
32KTIMER	T32K_ICLK	WKUP_L4_ICLK2	PRCM	32KTIMER interface clock
Resets				
32KTIMER	T32K_NRESPWRON	WKUP_SYS_PWRON_RST	PRM	Reset to 32KTIMER
32KTIMER	T32K_WKUP_RST	WKUP_RST	PRM	Reset to 32KTIMER

Table 22-136. Hardware Requests

No Interrupt Requests
No DMA Requests

22.4.4 32-kHz Synchronized Timer Functional Description

The synchronized timer is a counter that starts on the rising edge of an external asynchronous signal (sys_nrespwron). When sys_nrespwron is released (on the rising edge of sys_nrespwron), the counter starts counting up from the reset value of the counter register on the falling edge of the 32-kHz system clock after three inverted 32-kHz clock periods. After reaching its highest value, the counter wraps back to 0 and starts counting again with no additional delay. When sys_nrespwron is released (on the rising edge of sys_nrespwron), after three inverted 32-kHz clock periods, the counter starts counting up from the reset value of the counter register on the falling edge of the 32-kHz system clock.

Figure 22-20 shows the reset synchronization timing diagram. After reaching its highest value, the counter wraps back to 0 and starts counting again without any extra delay.

Figure 22-20. Reset Resynchronization Timing Diagram

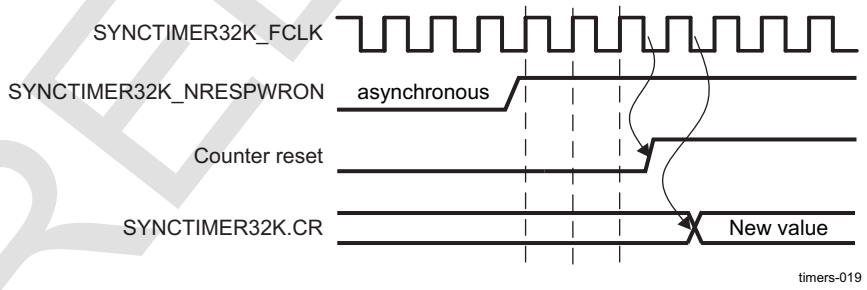

Figure 22-21 is the block diagram of the synchronized timer.

NOTE: sys_nrespwron is an active-low input.

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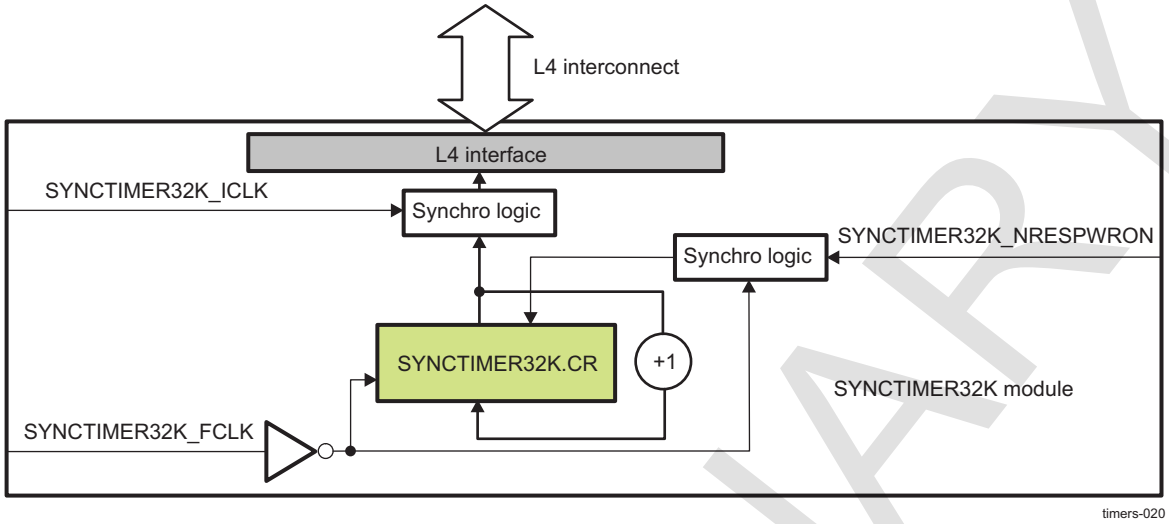
Figure 22-21. SYNCTIMER32K Block Diagram



The sync logic ensures the read transaction correctness by synchronizing the counter register read access on 32KSYNCNT_ICLK because the 32KSYNCNT_ICLK clock signal is completely asynchronous with S32KSYNCNT_FCLK. The sys_nrespwron input resets the counter register (32KSYNCNT_CR). The inverted 32KSYNCNT_FCLK clocks the sys_nrespwron reset signal.

22.4.4.1 Reading the 32-kHz Synchronized Timer

The counter register (32KSYNCNT_CR) is 32 bits wide. For correct count capture, it must be accessed as 16-bit LSB access first and 16-bit MSB access next. Internal synchronization logic allows reading of the counter value with 32KSYNCNT_ICLK while the counter is running. The time latency to read the synchronized counter register is one 32KSYNCNT_ICLK clock period.

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22.4.5 32KTimer Register Manual

Table 22-137 lists the base address and block size for the 32-kHz synchronized timer. It is memory mapped to the L4 peripheral bus memory space.

Table 22-137. 32KTimer Instance Summary

Module Name	Base Address L4 Interconnect	Size
32KTimer	0x4A30 4000	4KB

22.4.5.1 32KTimer Register Mapping Summary

CAUTION

The 32-kHz synchronized timer registers are limited to 32-bit and 16-bit data accesses; 8-bit access is not allowed and can corrupt the register content.

Table 22-138 lists the 32-kHz synchronized timer registers. through describe the register bits.

Table 22-138. 32KTimer Register Summary

Register Name	Type	Register Width (Bits)	Offset Address	Physical Address L4 Interconnect
32KSYNCNT_REV	R	32	0x0000	0x4A30 4000
32KSYNCNT_SYSCONFIG	R/W	32	0x0004	0x4A30 4004
32KSYNCNT_CR	R	32	0x0010	0x4A30 4010

22.4.5.2 32KTimer Register Description

Table 22-139. 32KSYNCNT_REV

Address Offset	0x0000
Physical Address	0x4A30 4000
Description	This register contains the sync counter IP revision code.
Type	R

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP Revision	R	0x-(1)

(1) TI internal data

Table 22-140. Register Call Summary for Register 32KSYNCNT_REV

32-kHz Synchronized Timer

- 32KTimer Register Mapping Summary: [0]

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Table 22-141. 32KSYNCNT_SYSCONFIG

Address Offset	0x0004
Physical Address	0x4A30 4004
Description	This register is used for IDLE modes only.
Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																											IDLEMODE		Reserved			

Bits	Field Name	Description		Type	Reset
31:5	Reserved	Reads return 0.		R	0x0
4:3	IDLEMODE	Power management REQ/ACK control		RW	0x0
		0x0:	Force idle. An idle request is acknowledged unconditionally.		
		0x1:	No-idle. An idle request is never acknowledged.		
		0x2:	Reserved		
		0x3:	Reserved		
2:0	Reserved	Reads return 0.		R	0x0

Table 22-142. Register Call Summary for Register 32KSYNCNT_SYSCONFIG

32-kHz Synchronized Timer

- 32KTimer Register Mapping Summary: [0]

Table 22-143. 32KSYNCNT_CR

Address Offset	0x0010
Physical Address	0x4A30 4010
Description	This register contains the 32-kHz sync counter value.
Type	R

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNTER_VALUE																															

Bits	Field Name	Description	Type	Reset
31:0	COUNTER_VALUE	Counter register value	R	0x00000003

Table 22-144. Register Call Summary for Register 32KSYNCNT_CR

32-kHz Synchronized Timer

- 32-kHz Synchronized Timer Functional Description: [0]
- Reading the 32-kHz Synchronized Timer: [1]
- 32KTimer Register Mapping Summary: [2]

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Serial Communication Interface

This chapter describes the features and operation of the device serial communication interface (SCI).

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23.3 UART/IrDA/CIR 4421
23.4 Multichannel Serial Port Interface 4529
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23.6 Multichannel PDM Controller 4709
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23.10 MIPI-HSI 4972
23.11 High-Speed Multiport USB Host Subsystem 5048
23.12 High-Speed USB OTG Controller 5171
23.13 Full-Speed USB Host Controller 5216

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23.1 Multimaster High-Speed I²C Controller

23.1.1 HS I²C Overview

The device contains four multimaster high-speed (HS) inter-integrated circuit (I²C™) controllers (I2Ci modules, where i = 1, 2, 3, 4), each of which provides an interface between a local host (LH), such as a digital signal processor (DSP), and any I²C-bus-compatible device that connects through the I²C serial bus. External components attached to the I²C bus can serially transmit and receive up to 8 bits of data to and from the LH device through the 2-wire I²C interface.

Each multimaster HS I²C controller can be configured to act like a slave or master I²C-compatible device. Moreover, each multimaster HS I²C controller can be configured in serial camera control bus (SCCB) mode (the SCCB is a serial bus developed by Omnivision Technologies, Inc.) to act as a master on a 2-wire SCCB bus. Only multimaster HS I²C controllers I2C2 and I2C3 can be configured in SCCB mode to act as a master device on a 3-wire SCCB bus.

The device contains a fifth master transmitter HS I²C interface (I2C5) in the power, reset, and clock management (PRCM) module to perform dynamic voltage control and power sequencing with an external power integrated circuit (IC).

Figure 23-1 shows the HS ***I²C*** controllers.

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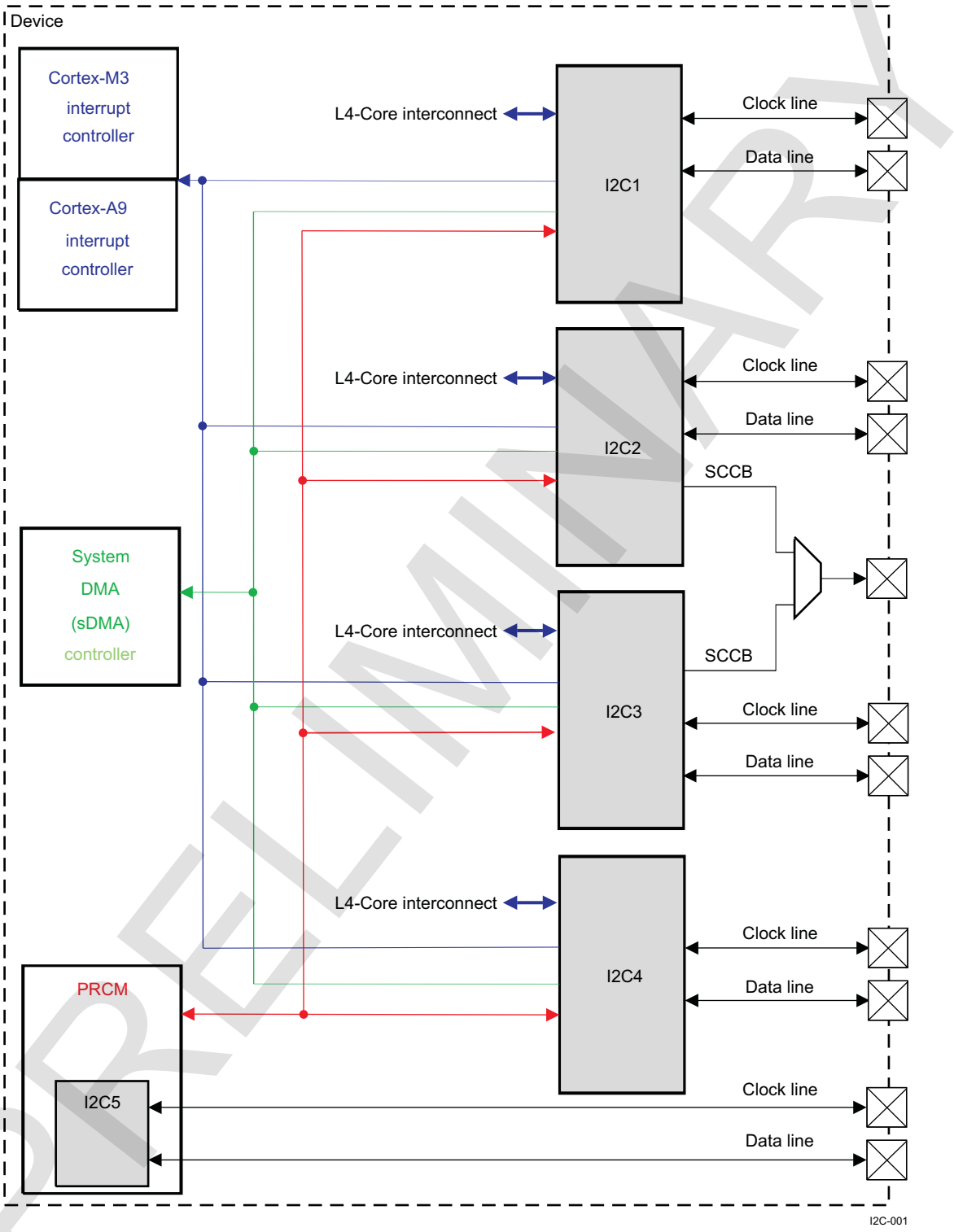
Figure 23-1. HS I²C Controllers



The four multimaster HS I²C controllers have the following features:

- Compliant with Philips I2C specification version 3.0
- Supports standard mode (up to 100 Kbps), fast mode (up to 400 Kbps), and fast mode+ (up to 1 Mbps)
- Supports HS mode for transfer up to 3.4 Mbps

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- Support for 3-wire/2-wire SCCB master mode for I2C2 and I2C3 modules, 2-wire SCCB master mode for I2C1 and I2C4 modules, up to 100 Kbps
- 7-bit and 10-bit device addressing modes
- General call
- Start/restart/stop
- Multimaster transmitter/slave receiver mode
- Multimaster receiver/slave transmitter mode
- Combined master transmit/receive and receive/transmit mode
- Built-in configurable FIFOs (8, 16, 32, 64 bytes) for buffered read or write
- Module enable/disable capability
- Programmable multislave channel (responds to four separate addresses)
- Programmable clock generation
- 8-bit-wide data access
- Open-core protocol (OCP) interface with LH application (OCP-IP 2.0 compliant)
- Designed for low power consumption
- Implement Auto Idle mechanism
- Implement Idle Request/Idle Acknowledge handshake mechanism
- Support for asynchronous wake-up mechanism
- Two direct memory access (DMA) channels
- Wide interrupt capability
- Supports OmniVision SCCB protocol
- Compliant with Highlander 0.8

The master transmitter HS I²C controller I2C5 has the following features:

- Support of HS and fast modes
- 7-bit addressing mode only
- Master transmitter mode only
- Start/restart/stop

NOTE: Before using HS I²C mode, determine that the target device supports this mode.

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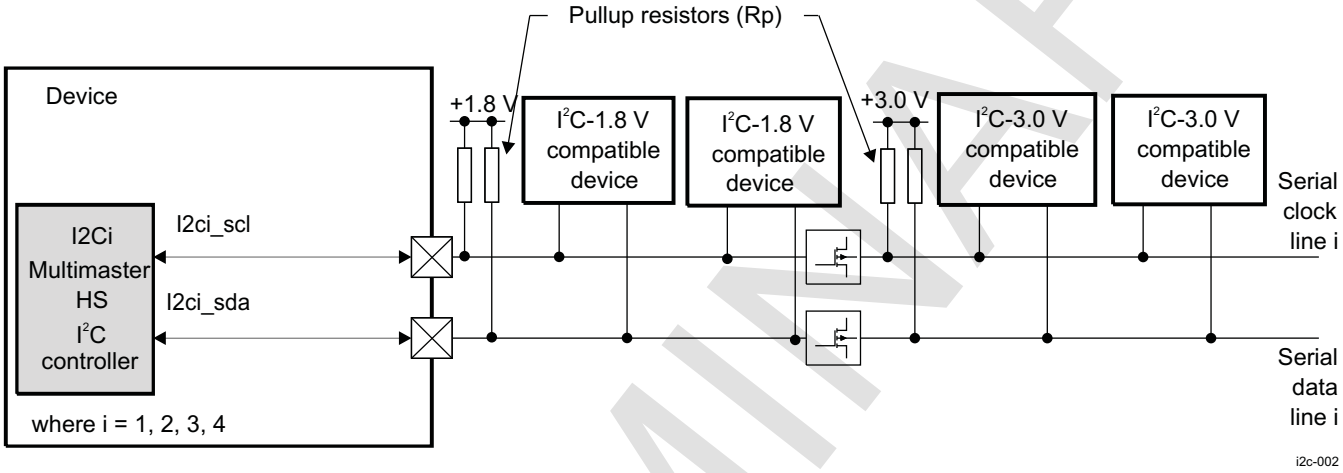
23.1.2 HS I²C Environment

This section describes the HS I²C application fields from an environment point of view (external connections). It describes HS I²C connectivity options, lists all possible interfaces, and describes the protocol and data format used in each case.

23.1.2.1 HS I²C in I²C Mode

Figure 23-2 shows the multimaster HS I²C controllers and their related connections with I²C-compliant devices in I²C mode.

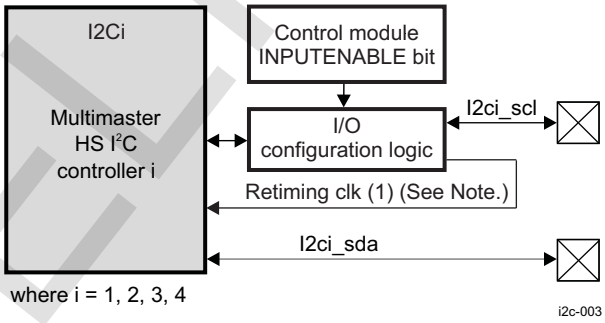
Figure 23-2. HS I²C and Typical Connections to I²C Devices



23.1.2.1.1 HS I²C Pins for Typical Connections in I²C Mode

Figure 23-3 shows the multimaster HS I²C controller pins used for typical connections with I²C devices.

Figure 23-3. HS I²C Interface Signals in I²C Mode



NOTE: In master mode, the clock signal (IP clk configured as output) is also used as retiming input (the INPUTENABLE bit in the corresponding pad configuration register must be set to 1).

23.1.2.1.2 HS I²C Interface Typical Connections

Table 23-1 lists the pins associated with the I²C interface.

Table 23-1. HS I²C Input/Output

Signal	I/O [1]	Description	Reset Value
i2ci_scl	I/O	I²C serial clock line[2]. Open-drain output buffer. Requires external pullup resistor (Rp).	1

[1] I = Input; O = Output

[2] This output signal is also used as retiming input (the INPUTENABLE bit in the corresponding pad configuration register must be set to 1).

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Table 23-1. HS I²C Input/Output (continued)

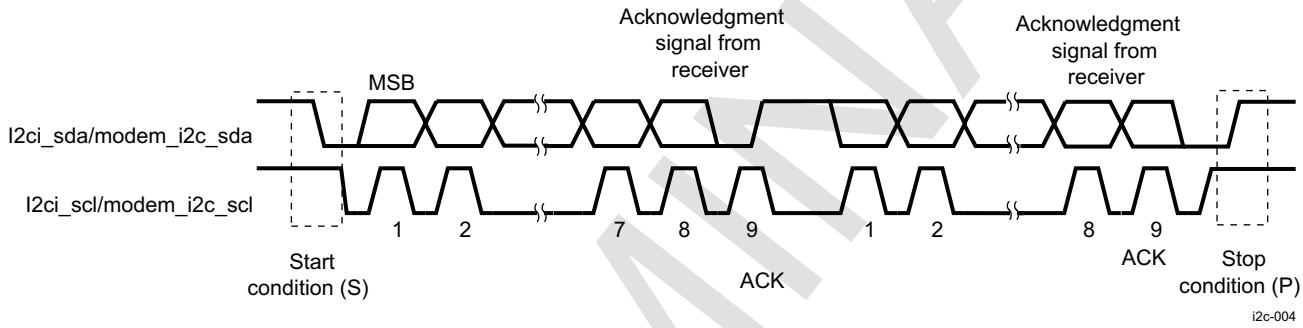
Signal	I/O [1]	Description	Reset Value
i2ci_sda	I/O	I²C serial data line. Open-drain output buffer. Requires external Rp.	1

23.1.2.1.3 HS I²C Typical Connection Protocol and Data Format

23.1.2.1.3.1 HS I²C Serial Data Format

The I²C controller operates in 8-bit word data format (byte write access supported for the last access). Each byte transmitted or received on the serial data line is 8 bits long. The number of bytes that can be transmitted or received is not restricted. The data is transferred with the most-significant bit (MSB) first. In receiver mode, each byte is followed by an acknowledge bit from the I²C. Figure 23-4 shows a typical I²C communication format.

Figure 23-4. HS I²C Data Transfer

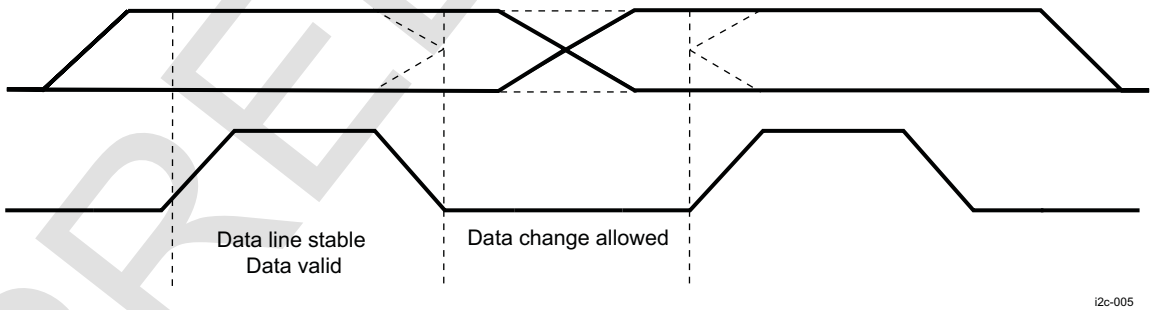


23.1.2.1.3.2 HS I²C Data Validity

The data on the serial data line (SDA) must be stable during the high period of the serial clock line. The high and low states of the data line can change only when the clock signal on the serial clock line (SCL) is low.

Figure 23-5 is an example of data validity requirements.

Figure 23-5. HS I²C Bit Transfer on the I²C Bus



23.1.2.1.3.3 HS I²C Start and Stop Conditions

The I²C module generates start (S) and stop (P) conditions when it is configured as a master.

- An S condition is a high-to-low transition on the serial data line while serial clock line is high.
- A P condition is a low-to-high transition on the serial data line while serial clock line is high.

The bus is considered busy after the S condition (the I2Ci.I2C_STAT[12] BB bit is 1 to indicate that the bus is busy) and free after the P condition (the I2Ci.I2C_STAT[12] BB bit is 0 to indicate that the bus is free).

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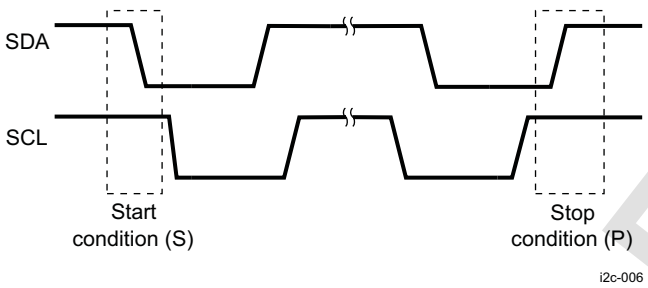
Figure 23-6 shows the waveforms that occur during an S and a P condition.

Figure 23-6. HS I²C S and P Condition Events



23.1.2.1.3.4 HS I²C Addressing

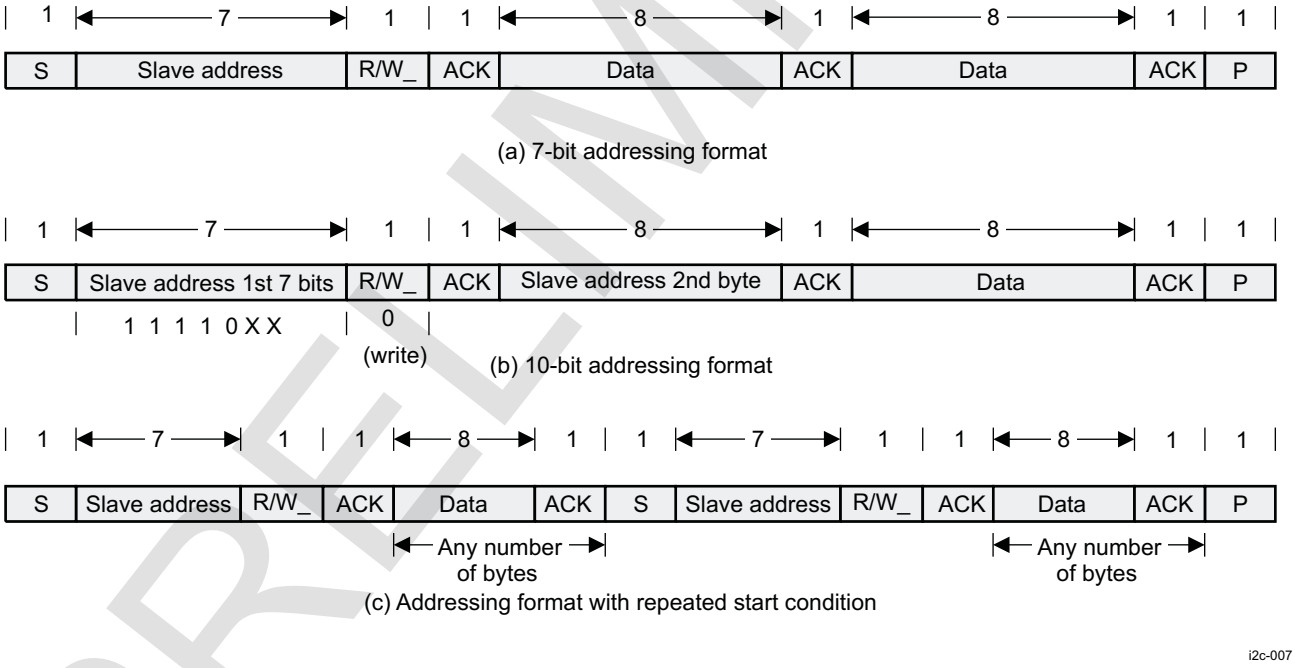
The I²C module supports two data formats in fast/standard (F/S) and HS modes:

- 7-bit/10-bit addressing format
- 7-bit/10-bit addressing format with repeated start (Sr) condition

23.1.2.1.3.4.1 Data Transfer Formats in F/S Mode

Figure 23-7 shows the I²C data transfer formats in F/S mode.

Figure 23-7. HS I²C Data Transfer Formats in F/S Mode



The first word after an S condition consists of 8 bits. In acknowledge mode, an extra dedicated acknowledgment bit is inserted after each byte.

In addressing formats with 7-bit addresses, the first byte is composed of 7 MSB slave address bits and 1 least-significant bit (LSB) R/W_ bit.

The LSB R/W_ bit of the address byte indicates the transmission direction of the data bytes that follow it. If R/W_ is 0, the master writes data to the selected slave; if it is 1, the master reads data from the slave.

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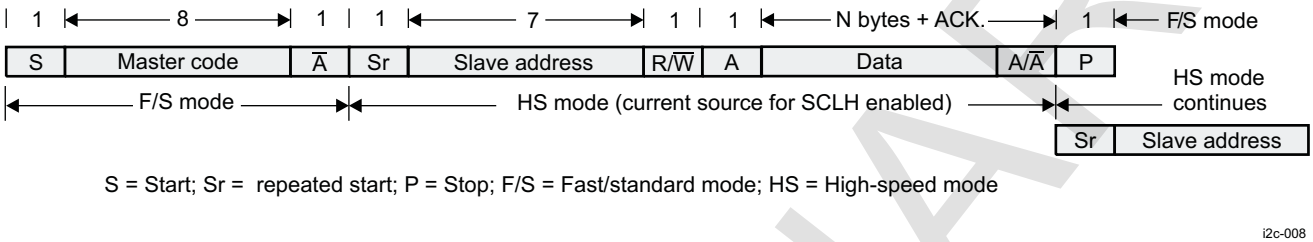
In addressing formats with 10-bit addresses, the structure of the first byte is 11110XXY, where XX is the 2 MSBs of the 10-bit addresses, and Y is the R/W_ bit. If the R/W_ bit is 0, the next byte contains the last 8 bits of the slave address. If the R/W_ bit is 1, the next byte contains data transmitted from the slave to the master.

23.1.2.1.3.4.2 Data Transfer Format in HS Mode

Figure 23-8 shows the I²C data transfer format in HS mode.

Figure 23-8. HS I²C Data Transfer in HS Mode



Each multimaster HS I²C controller can also operate in HS mode. In this case, after the S condition, the module, which is in F/S mode, writes the master code address (000001XXX, where XXX is the variable portion of the master code) on the bus. No device connected on the same bus acknowledges this address. The module switches the clock to the HS clock and after an Sr condition, and sends the slave address and the data, as shown in Figure 23-8.

23.1.2.1.3.5 HS I²C Master Transmitter

In master transmitter mode, data assembled in one of the previously described data formats is shifted out on the serial data line SDA in sync with the self-generated clock pulses on the serial clock line SCL. The clock pulses are inhibited and SCL is held low when the intervention of the processor is required (XUDF) after a byte is transmitted.

23.1.2.1.3.6 HS I²C Master Receiver

Master receiver mode can be entered only from master transmitter mode. With any of the address formats (a), (b), or (c) (see Figure 23-7), if R/W_ is high, the module enters master receiver mode after the slave address byte and bit R/W_ are transmitted. Serial data bits received on bus line SDAI are shifted in synchronization with the self-generated clock pulses on SCLI.

23.1.2.1.3.7 HS I²C Slave Transmitter

Slave transmitter mode can be entered only from slave receiver mode. With any of the address formats (a), (b), or (c) (see Figure 23-7), the slave transmitter is entered if the slave address byte is the same as its own address and bit R/W_ is transmitted, if R/W_ is high. The slave transmitter shifts the serial data out on the data line SDA in sync with the clock pulses that are generated by the master device. It does not generate the clock but it can hold clock line SCL low while intervention of the LH is required (XUDF).

23.1.2.1.3.8 HS I²C Slave Receiver

In this mode, serial data bits received on the bus line SDA are shifted-in in sync with the clock pulses on SCL that are generated by the master device. It does not generate the clock but it can hold clock line SCL low while intervention of the LH is required (ROVR) after a byte is received.

23.1.2.1.3.9 HS I²C Bus Arbitration

If two or more master transmitters start a transmission on the same bus almost simultaneously, an arbitration procedure is invoked. The arbitration procedure uses the data presented on the serial bus by the competing transmitters. When a transmitter senses that a high signal it has presented on the bus has

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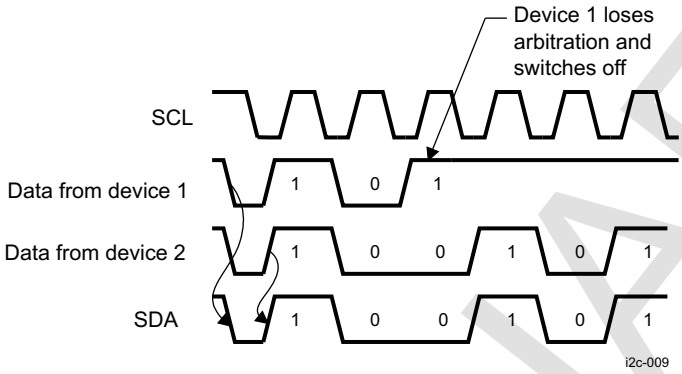
been overruled by a low signal, it switches to the slave receiver mode, sets the arbitration lost (AL) flag, and generates the arbitration lost interrupt. Figure 23-9 shows the arbitration procedure between two devices. The arbitration procedure gives priority to the device that transmits the serial data stream with the lowest binary value. If two or more devices send identical first bytes, arbitration continues on the subsequent bytes.

Figure 23-9. HS I²C Arbitration Between Master Transmitters



23.1.2.1.3.10 HS I²C Clock Generation and Synchronization

Under normal conditions, only one master device generates the clock signal, SCL. During the arbitration procedure, however, there are two or more master devices and the clock must be synchronized so that the data output can be compared. The wired-AND property of the clock line means that a device that first generates a low period of the clock line overrules the other devices. At this high/low transition, the clock generators of the other devices are forced to start generating their own low period. The clock line is then held low by the device with the longest low period, while the other devices that finish their low periods must wait for the clock line to be released before starting their high periods. A synchronized signal on the clock line is thus obtained, where the slowest device determines the length of the low period and the fastest device determines the length of the high period. If a device pulls down the clock line for a longer time, the result is that all clock generators must enter the WAIT-state. In this way a slave can slow down a fast master and the slow device can create enough time to store a received byte or prepare a byte to be transmitted (Clock Stretching).

NOTE: In case the SCL or SDA lines are stuck low, the Bus Clear operation is supported.

If the clock line (SCL) is stuck low, the preferred procedure is to reset the bus using the hardware reset signal if your I²C devices have hardware reset inputs. If the I²C devices do not have hardware reset inputs, cycle power to the devices to activate the mandatory internal power-on reset (POR) circuit.

If the data line (SDA) is stuck low, the master should send nine clock pulses. The device that held the bus low should release it sometime within those nine clocks. If not, then use the hardware reset or cycle power to clear the bus.

Figure 23-10 shows clock synchronization.

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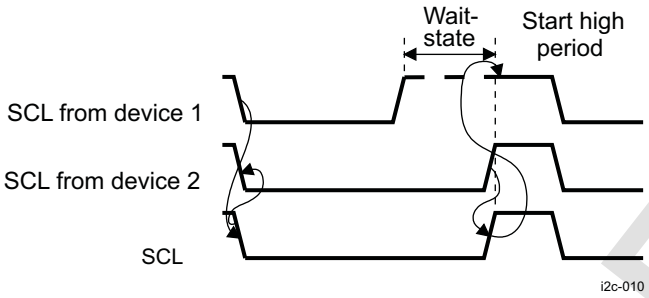
Figure 23-10. HS I²C Clock Generators Synchronization



23.1.2.1.3.11 HS I²C External Clock Configuration

Each multimaster HS I²C controller is clocked with an independent functional clock (I2Ci_FCLK) and an interface clock (I2Ci_ICLK) for interfacing with the L4_PER interconnect. These clocks are provided by the APE PRCM module for I2Ci (where i = 1, 2, 3, 4).

The SYS_CLK clock provided by the clock generator of the PRCM module is connected to the functional and interface clocks of the HS I²C controller I2C5. For detailed information about the module clocking, see Chapter 3, *Power, Reset, and Clock Management*.

The functional clock is processed by a prescaler block to produce the internal sampling clock. This clock is generated by the I²C prescaler block. The prescaler block consists of the I2Ci.I2C_PSC[7:0] PSC bit field (where i = 1, 2, 3, 4) that is used to divide down the functional clock to obtain an internal sampling clock with a frequency value of I2Ci_FCLK/(I2Ci.I2C_PSC[7:0] PSC bit field value + 1, where i = 1, 2, 3, 4).

NOTE: The I2Ci.I2C_PSC[7:0] PSC bit field (where i = 5) of I2C5 is not accessible by software.

23.1.2.2 HS I²C in SCCB Mode

The multimaster HS I²C controllers support the 2-wire SCCB protocol in master mode as listed in Figure 23-11. Only I2C2 and I2C3 support the 3-wire SCCB protocol in master mode.

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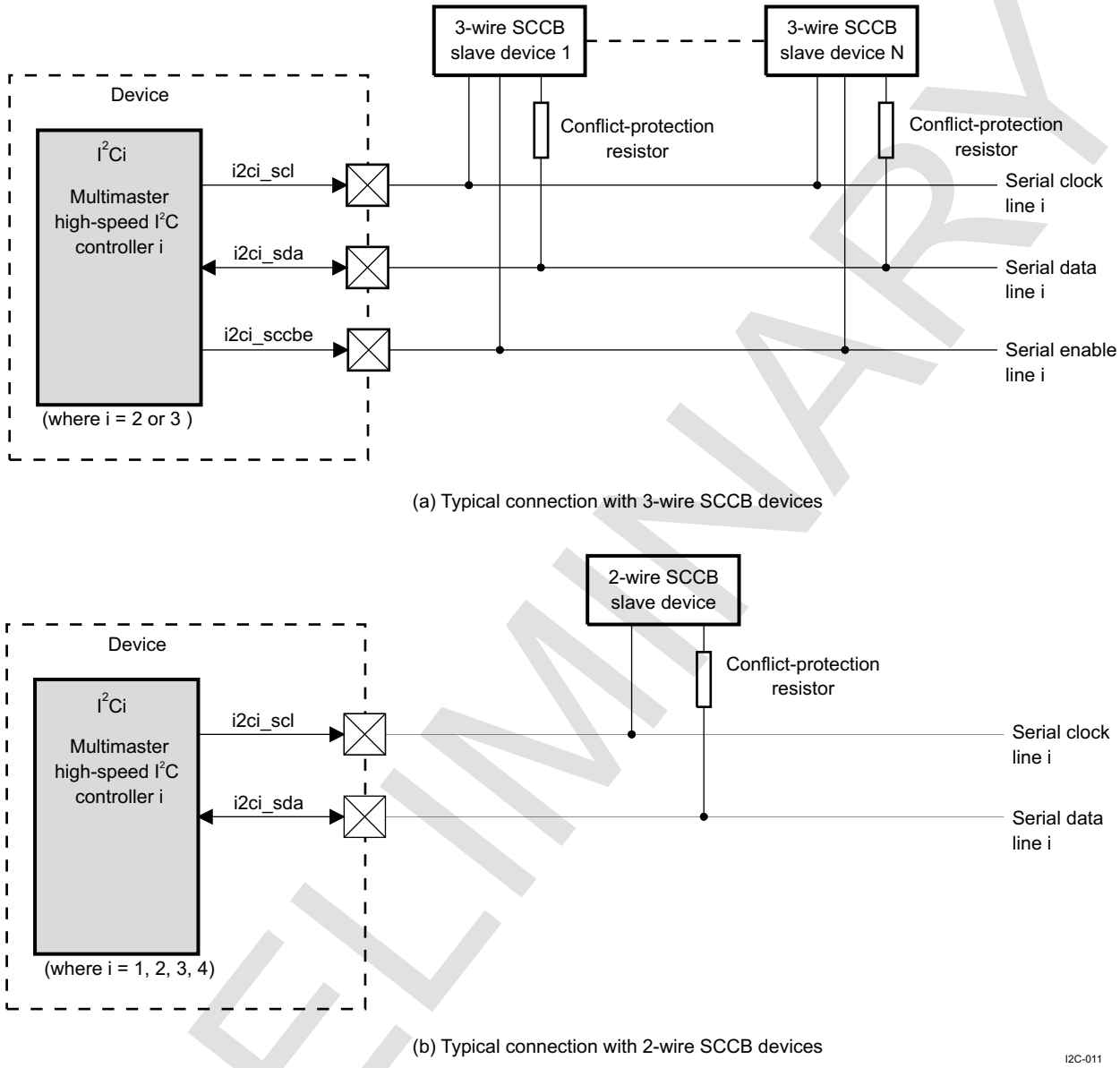
Figure 23-11. HS I²C and Typical Connections to SCCB Devices



NOTE: Only one 2-wire SCCB slave device can be connected to the 2-wire SCCB bus.

23.1.2.2.1 HS I²C Pins for Typical Connections in SCCB Mode

Figure 23-12 shows the multimaster HS I²C controller pins used for typical connections with 3-wire or 2-wire SCCB devices.

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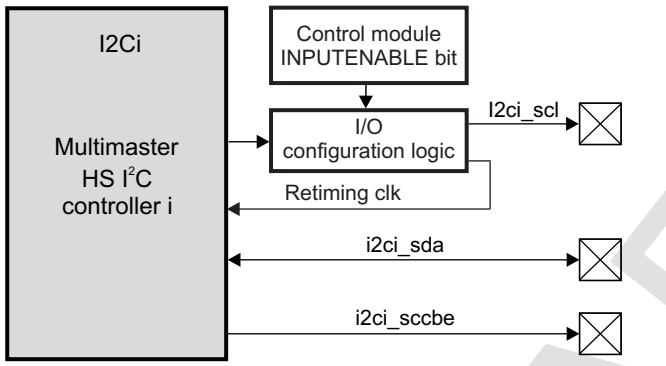
Figure 23-12. HS I²C Interface Signals in SCCB Mode



(where i = 1, 2, 3, 4 and i2ci_sccbe is not available for I2C1 and I2C4)

I2C-012

23.1.2.2.2 HS I²C SCCB Interface Typical Connections

Table 23-2 lists the pins associated with the SCCB interface.

Table 23-2. HS I²C Input/Output

Signal	I/O [1]	Description	Reset Value [2]	I2Ci.I2C_CON[15] I2C_EN bit = 0
i2ci_scl	O	SCCB serial clock line[3]. Standard CMOS output buffer.	Hi-Z	High
i2ci_sda	I/O(OD)	SCCB serial data line. Standard CMOS 3-state output buffer. Requires external conflict-protection resistor for each slave device connected to the bus.	Hi-Z	Hi-Z
i2ci_sccbe [4]	O	SCCB enable line. Standard CMOS output buffer.	High	High

(1) I = Input; O = Output; OD = Open Drain

(2) Hi-Z = High Impedance

(3) This output signal is also used as retiming input (the INPUTENABLE bit in the corresponding pad configuration register must be set to 1).

(4) This signal is used for the 3-wire SCCB protocol only.

NOTE: Because they share the same ball, the i2c2_sccbe and i2c3_sccbe signals are not available at the same time. For detailed information about pin configuration, see Chapter 18, *Control Module*.

I2C1 and I2C4 do not provide any i2c1_sccbe signal at the chip boundary of the device; thus, these modules do not support the 3-wire SCCB protocol.

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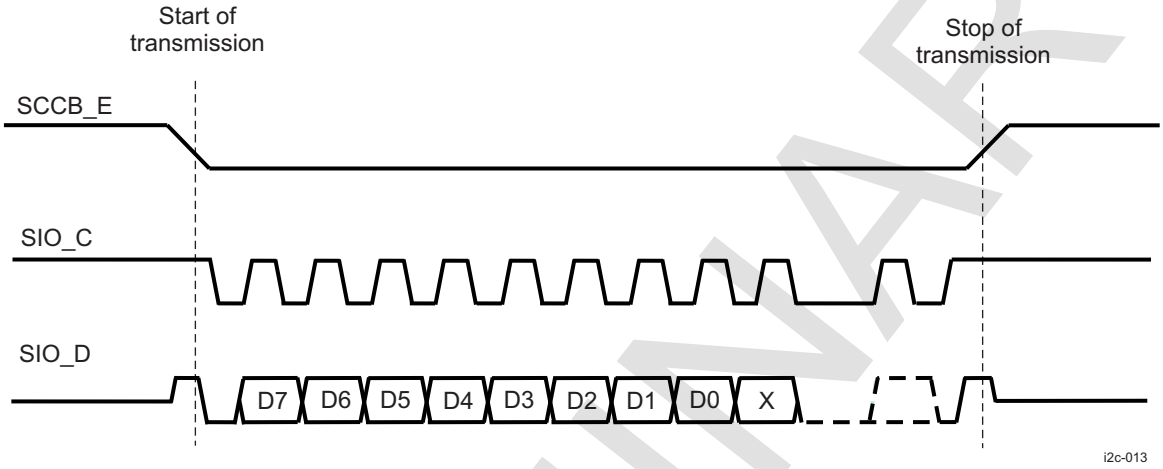
23.1.2.2.3 HS I²C SCCB Typical Connection Protocol and Data Format

23.1.2.2.3.1 HS I²C SCCB Data Format

If the module is configured in SCCB mode of operation, the data format of transmissions appears as shown in Figure 23-13. For SCCB protocol compatibility I²C provides one more signal, SCCB_E, which acts like a transaction enable signal.

Figure 23-13. HS I²C 3-wire SCCB Transmission Timing Diagram

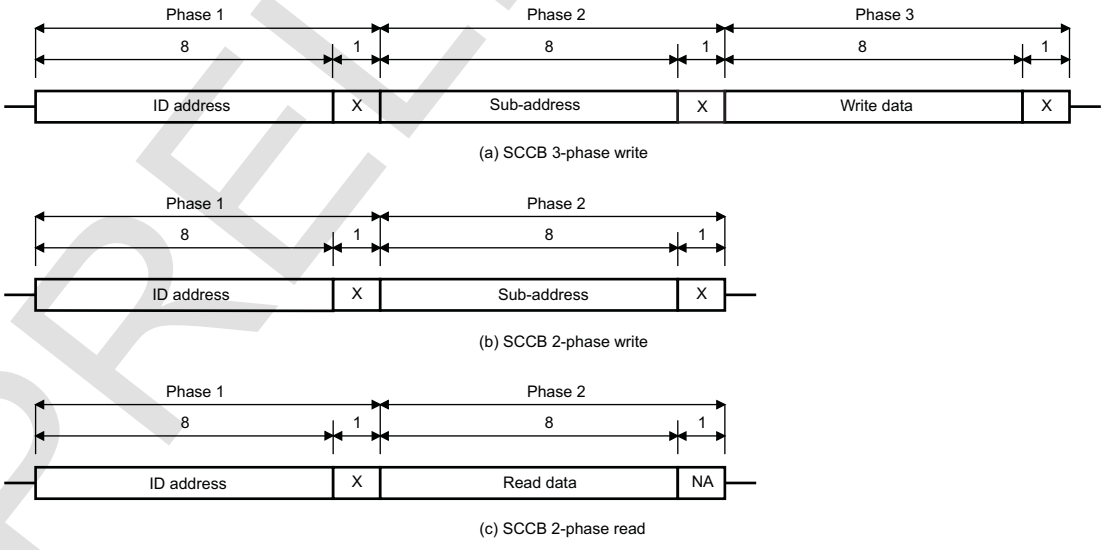


NOTE: When operating in 2-wire SCCB mode, the i2ci_sccbe signal is not used by the 2-wire SCCB-compliant slave device attached to the 2-wire SCCB bus.

23.1.2.2.3.2 HS I²C SCCB Transmission Data Formats

Figure 23-14 describes the data format of the three kinds of transmission.

Figure 23-14. HS I²C SCCB Transmission Data Formats



R/W: 0 = Write, 1 = Read

X: don't care

NA: ninth bit of a read phase. This bit must be set to 1 by the master device.

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The basic element of a data transmission is a phase. A phase contains 9 bits, which consist of an 8-bit sequential data transmission followed by a ninth bit. The ninth bit is a don't-care bit (X) or an NA bit, depending on whether the data transmission is a write or a read. The maximum number of phases that can be included in a transmission is three. The MSB is always asserted first for each phase.

A data transmission is one of three types:

- 3-phase write transmission:

  The 3-phase write transmission cycle (see (a) of Figure 23-14) is a full write operation in which the master can write 1 byte of data to a specific slave(s). The 7-bit slave address in the ID value identifies the specific slave that the master intends to access. The subaddress identifies the register location of the specified slave. The write data contains 8-bit data that the master intends to write over the content of this specific address. The ninth bit of each of the three phases is a don't-care bit (X bit).

- 2-phase write transmission:

  The 2-phase write transmission cycle is followed by a 2-phase read transmission cycle (see the following bullet). The purpose of issuing a 2-phase write transmission cycle (see (b) of Figure 23-14) is to identify the subaddress of some specific slave from which the master intends to read data for the following 2-phase read transmission cycle. The ninth bit of each phase is a don't-care bit (X bit).

- 2-phase read transmission:

  Either a 3-phase or a 2-phase write transmission cycle must be asserted ahead of a 2-phase read transmission cycle. The 2-phase read transmission cycle (see (c) of Figure 23-14) cannot identify the subaddress. The 2-phase write transmission cycle contains read data of 8 bits and a ninth don't-care bit or NA bit. The master must drive the NA bit at logical 1.

  In each transmission type, phase 1 (the 7-bit slave address of the ID value) is asserted by the master to identify the selected slave to which the data is read or written. Each slave has a unique 7-bit slave address. The 7-bit slave address of the ID value comprises 7 bits, from bit 7 to bit 1, that can identify up to 128 slaves. The eighth bit, bit 0, is the read/write selector bit that specifies the transmission direction of the current cycle. A logical 0 represents a write cycle and a logical 1 represents a read cycle. The ninth bit of phase 1 is a don't-care bit (X bit).

  Phase 2 (subaddress/read data) is asserted by the master (subaddress) or the slave(s) (read data). A phase 2 transmission asserted by the master identifies the subaddress of the slave(s) the master intends to access. A phase 2 transmission asserted by the slave(s) indicates the read data that the master will receive. The slave(s) recognize the subaddress of this read data according to the previous 3-phase or 2-phase write transmission cycle. The ninth bit is defined as a don't-care bit (X bit) when the master asserts phase 2. The ninth bit is defined as an NA bit when the slave(s) asserts the phase 2 transmission. The master is responsible for a logical 1 during the period of the NA bit.

  Phase 3 (write data) is asserted only by the master. This phase contains the data the master intends to write to the slave(s). Because the master asserts the transmission, the ninth bit of the phase 3 transmission is defined as a don't-care bit (X bit).

NOTE: A multimaster HS I²C controller configured in SCCB mode can perform two operations:

- Write a single byte to an SCCB slave device by using the 3-phase write transmission cycle
- Read a single byte from an SCCB slave device by using the 2-phase write transmission cycle followed by the 2-phase read transmission cycle

23.1.2.2.3.3 HS I²C Data Validity

The data validity is the same as described in Section 23.1.2.1.3.2, *HS I²C Data Validity*.

23.1.2.2.3.4 HS I²C S and P Conditions

The S and P conditions are the same as described in Section 23.1.2.1.3.3, *HS I²C Start and Stop Conditions*.

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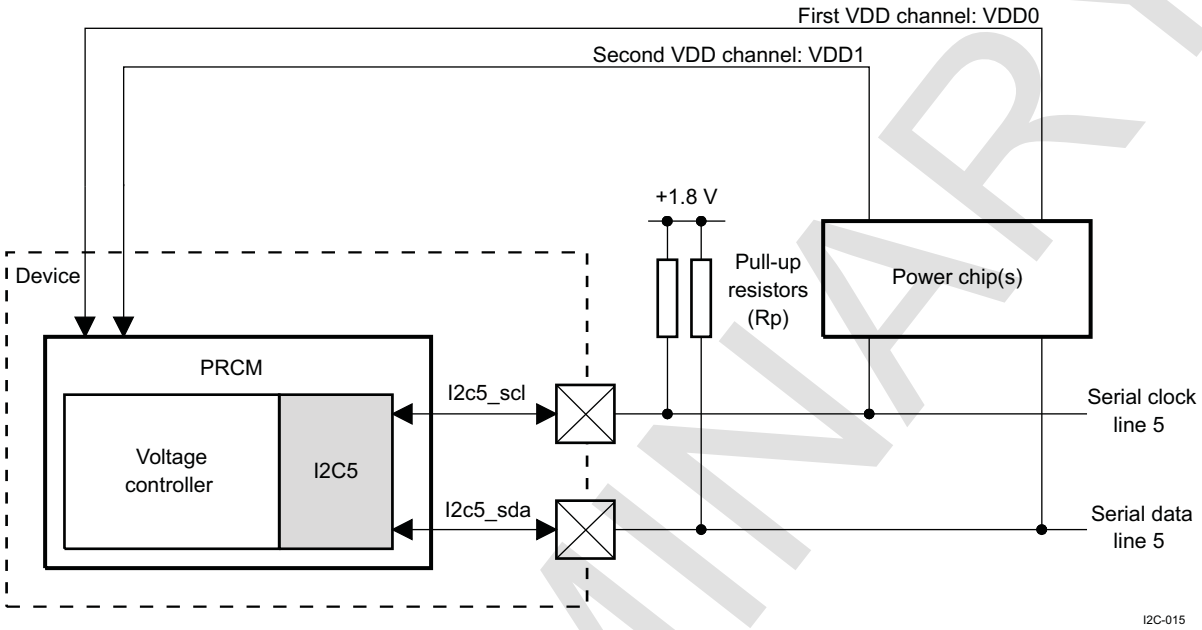
23.1.2.3 HS I²C for Communication With Power Chip(s)

Figure 23-15 shows a typical connection between the master transmitter HS I²C controller I2C5 of the device and external power chip(s).

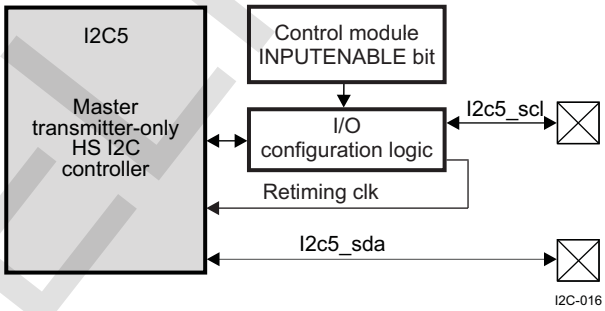
Figure 23-15. HS I²C and Typical Connection Between the HS I²C and Power Chip(s)



23.1.2.3.1 HS I²C I2C5 Pins for Typical Connections

Figure 23-16 shows the HS I²C controller I2C5 pins used for typical connections with power chips.

Figure 23-16. HS I²C I2C5 Interface Signals



23.1.2.3.2 HS I²C I2C5 Interface Typical Connections

The master transmitter HS I²C controller I2C5 interfaces between the device and external power chip(s) for voltage control. This module is always configured as an I²C master transmitter; it does not support the SCCB protocol.

Table 23-3 lists the pins associated with the I²C interface of the HS I²C controller I2C5 of the device.

Table 23-3. HS I²C Input/Output Description

Signal	I/O [1]	Description	Reset Value
i2c5_scl	I/O(OD)	I²C serial clock line[2]. Open-drain output buffer. Requires external Rp.	1

(1) I = Input; O = Output; OD = Open Drain

(2) This signal is also used as retiming input (the INPUTENABLE bit in the corresponding pad configuration register must be set to 1).

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Table 23-3. HS I²C Input/Output Description (continued)

Signal	I/O [1]	Description	Reset Value
i2c5_sda	I/O(OD)	I²C serial data line. Open-drain output buffer. Requires external Rp.	1

23.1.2.3.3 HS I²C Typical Connections Protocol and Data Format for I2C5

23.1.2.3.3.1 HS I²C Serial Data Format for I2C5

The serial data format is the same as described in Section 23.1.2.1.3.1, *HS I²C Serial Data Format*.

23.1.2.3.3.2 HS I²C Data Validity for I2C5

The data validity is the same as described in Section 23.1.2.1.3.2, *HS I²C Data Validity*.

23.1.2.3.3.3 HS I²C S and P Conditions for I2C5

The S and P conditions are the same as described in Section 23.1.2.1.3.3, *HS I²C Start and Stop Conditions*.

23.1.2.3.3.4 HS I²C Addressing for I2C5

The master transmitter HS I²C controller I2C5 supports only the 7-bit addressing mode. For each frame, the master writes the 8-bit value (DATA) in the register specified by the 8-bit register address (RA) of the slave addressed by the slave address (SA).

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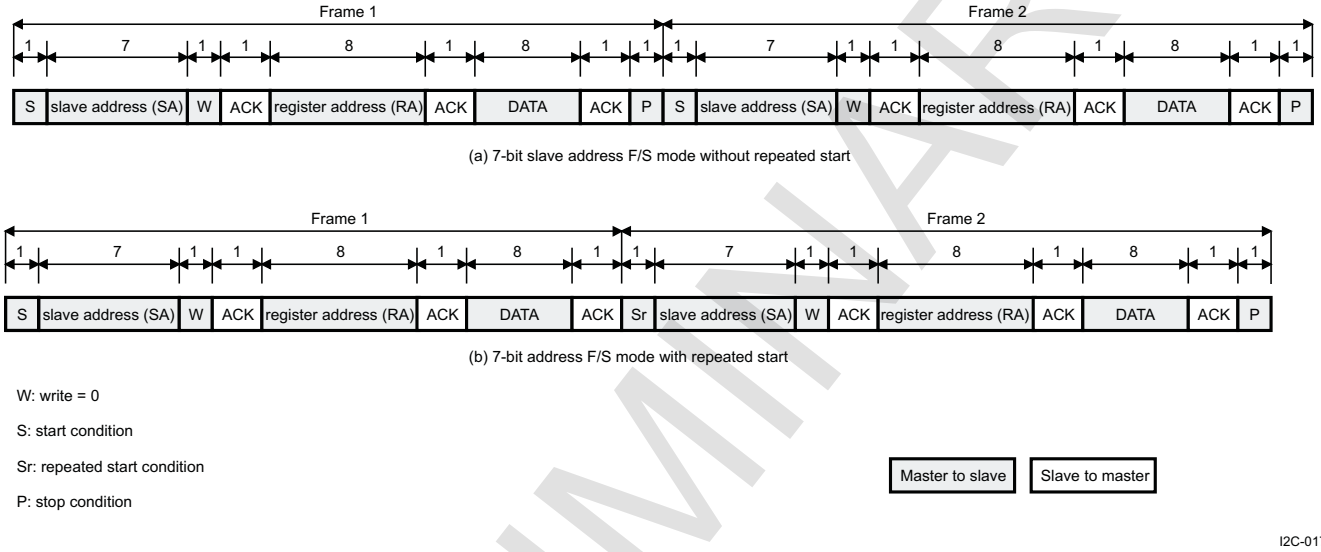
23.1.2.3.3.4.1 HS I²C Data Transfer Format in F/S Mode

Figure 23-17 shows the I²C data transfer format in F/S mode for I2C5.

Figure 23-17. HS I²C Data Transfer Format in F/S Mode for I2C5



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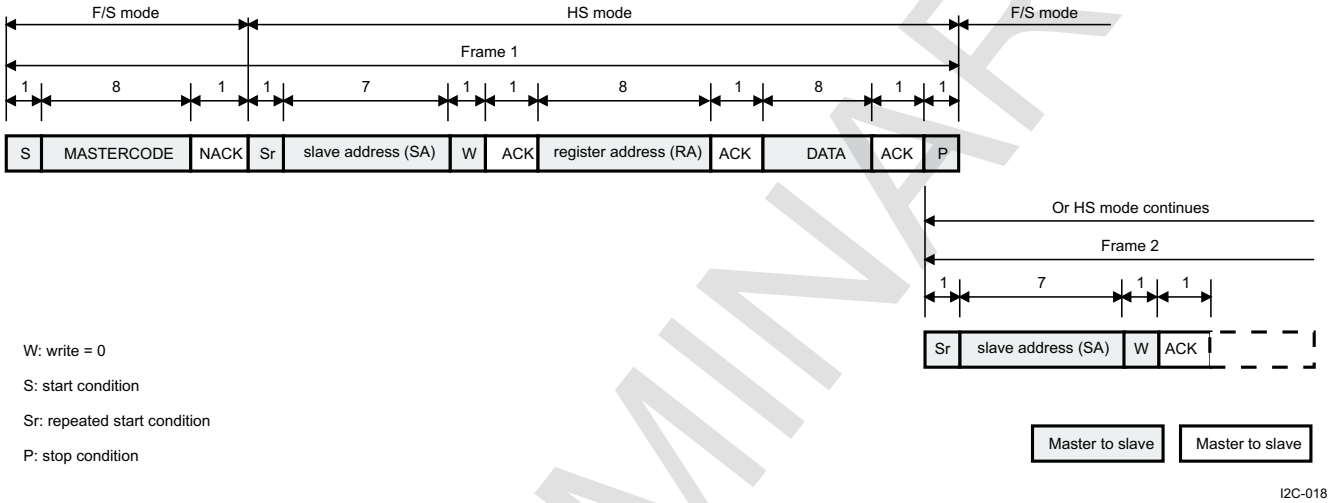
23.1.2.3.3.4.2 Data Transfer Format in HS Mode

Figure 23-18 shows the I²C data transfer format in HS mode for I2C5.

Figure 23-18. HS I²C Data Transfer Format in HS Mode for I2C5



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23.1.3 HS I²C Integration

This section describes module integration in the device, including information about clocks, resets, and hardware requests.

Figure 23-19 shows the integration of the four HS I²C controllers in the device.

Figure 23-19. HS I²C Integration

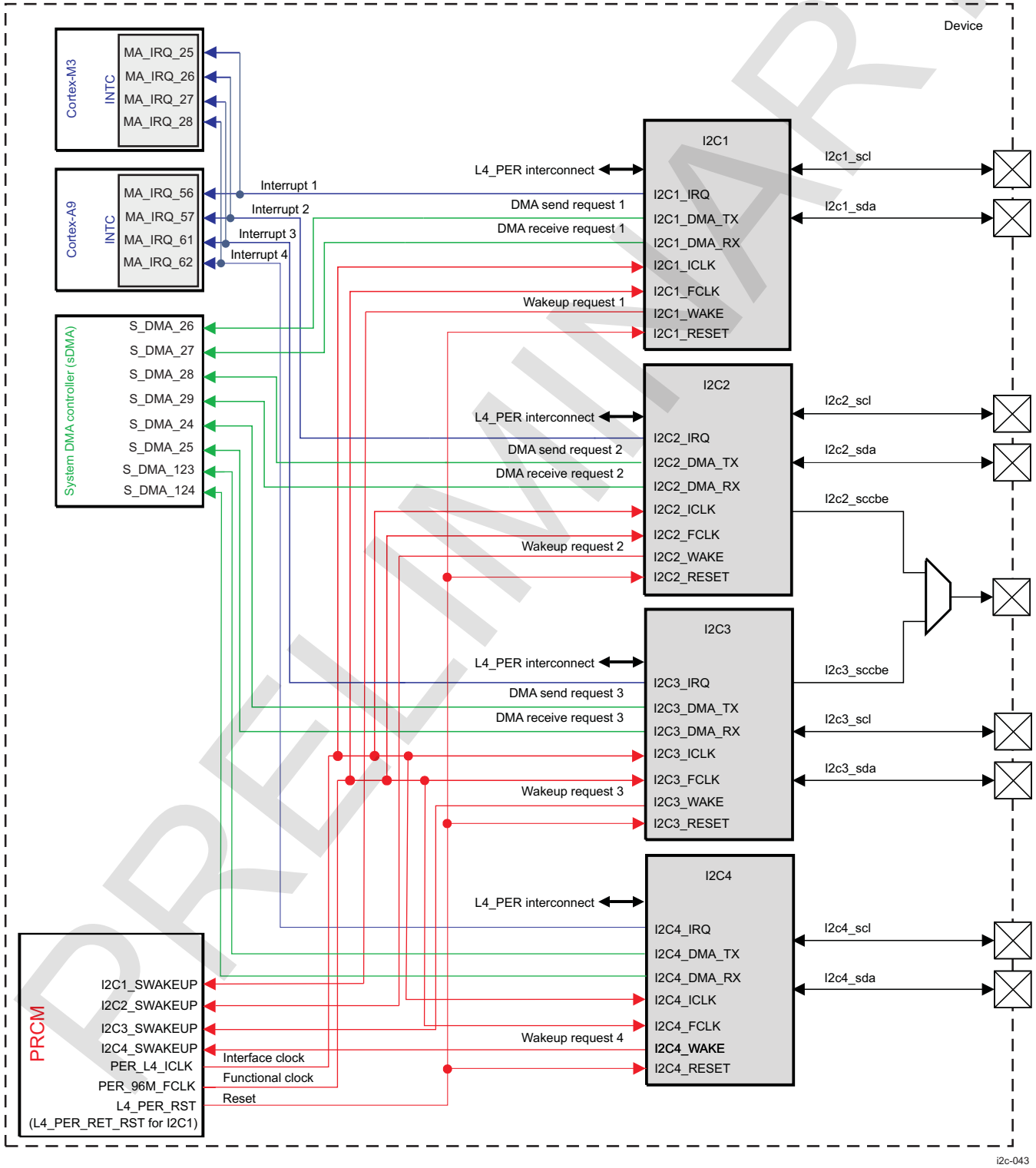

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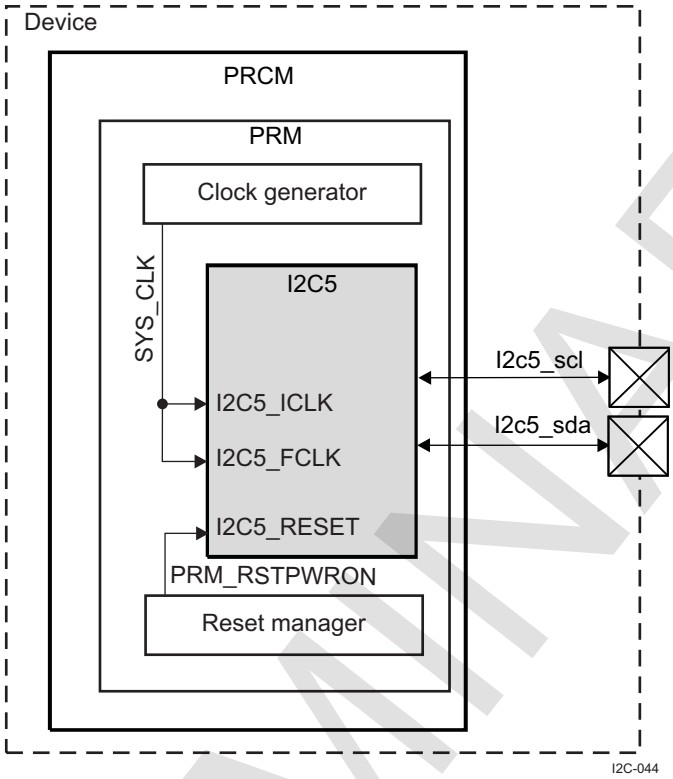
Figure 23-20 shows HS I²C integration of I2C5 inside the PRCM module.

Figure 23-20. HS I²C I2C5 Integration



NOTE: For more information about the IDLE hardware handshake and the wake-up request, see , *Power Management Functional Description*, in Chapter 3, *Power, Reset, and Clock Management*.

Table 23-4 through Table 23-6 summarize the integration of the module in the device.

Table 23-4. HS I²C Integration Attributes

Module Instance	Attributes	
	Power Domain	Interconnect
I2C1	PD_L4_PER	L4_PER
I2C2	PD_L4_PER	L4_PER
I2C3	PD_L4_PER	L4_PER
I2C4	PD_L4_PER	L4_PER

Table 23-5. HS I²C Clocks and Resets

	Clocks			
Module Instance	Destination Signal Name	Source Signal Name	Source	Description
I2C1	I2C1_ICLK	PER_L4_ICLK	PRCM	I2C1 interface clock
	I2C1_FCLK	PER_96M_FCLK	PRCM	I2C1 functional clock
I2C2	I2C2_ICLK	PER_L4_ICLK	PRCM	I2C2 interface clock
	I2C2_FCLK	PER_96M_FCLK	PRCM	I2C2 functional clock
I2C3	I2C3_ICLK	PER_L4_ICLK	PRCM	I2C3 interface clock
	I2C3_FCLK	PER_96M_FCLK	PRCM	I2C3 functional clock

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Table 23-5. HS I²C Clocks and Resets (continued)

I2C4	I2C4_ICLK	PER_L4_ICLK	PRCM	I2C4 interface clock
	I2C4_FCLK	PER_96M_FCLK	PRCM	I2C4 functional clock
Resets				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
I2C1	I2C1_RESET	L4_PER_RET_RST	PRCM	I2C1 reset
I2C2	I2C2_RESET	L4_PER_RST	PRCM	I2C2 reset
I2C3	I2C3_RESET	L4_PER_RST	PRCM	I2C3 reset
I2C4	I2C4_RESET	L4_PER_RST	PRCM	I2C4 reset

Table 23-6. HS I²C Hardware Requests

Interrupt Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
I2C1	I2C1_IRQ	MA_IRQ_56	Cortex™-A9 INTC	I2C1 interrupt request
	I2C1_IRQ	MM_IRQ_25	Cortex™-M3 INTC	I2C1 interrupt request
I2C2	I2C2_IRQ	MA_IRQ_57	Cortex-A9 INTC	I2C2 interrupt request
	I2C2_IRQ	MM_IRQ_26	Cortex-M3 INTC	I2C2 interrupt request
I2C3	I2C3_IRQ	MA_IRQ_61	Cortex-A9 INTC	I2C3 interrupt request
	I2C3_IRQ	MM_IRQ_27	Cortex-M3 INTC	I2C3 interrupt request
I2C4	I2C4_IRQ	MA_IRQ_62	Cortex-A9 INTC	I2C4 interrupt request
	I2C4_IRQ	MM_IRQ_28	Cortex-M3 INTC	I2C4 interrupt request
DMA Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
I2C1	I2C1_DMA_TX	S_DMA_26	sDMA	I2C1 DMA transmit request
	I2C1_DMA_RX	S_DMA_27	sDMA	I2C1 DMA receive request
I2C2	I2C2_DMA_TX	S_DMA_28	sDMA	I2C2 DMA transmit request
	I2C2_DMA_RX	S_DMA_29	sDMA	I2C2 DMA receive request
I2C3	I2C3_DMA_TX	S_DMA_24	sDMA	I2C3 DMA transmit request
	I2C3_DMA_RX	S_DMA_25	sDMA	I2C3 DMA receive request
I2C4	I2C4_DMA_TX	S_DMA_123	sDMA	I2C4 DMA transmit request
	I2C4_DMA_RX	S_DMA_124	sDMA	I2C4 DMA receive request

NOTE:

- For a description of interrupt source, see Table 23-12.
- For a description of DMA source, see Table 23-13.

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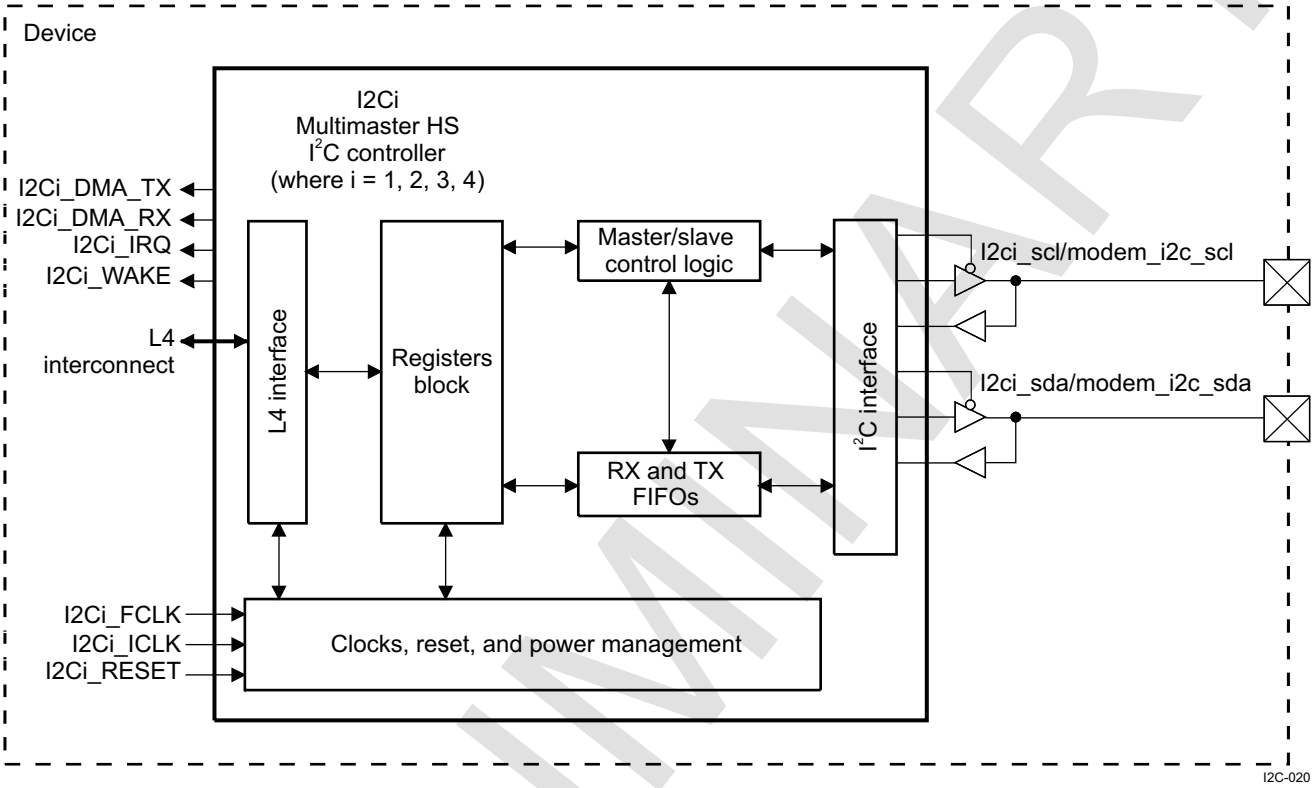
23.1.4 HS I²C Functional Description

23.1.4.1 HS I²C Block Diagram

Figure 23-21 is the multimaster I²C HS controller block diagram.

Figure 23-21. HS I²C Block Diagram



The five multimaster HS I²C controllers can be configured in F/S I²C mode, HS I²C mode, or SCCB mode. The operation mode is selected by configuring the I2Ci.I2C_CON[13:12] OPMODE bit field. Table 23-7 lists the available operation modes.

NOTE: The fifth master transmitter HS I²C interface (I2C5) in the PRCM module can also be configured in HS mode.

Table 23-7. HS I²C Operation Mode Selection

Operation Mode	Value of I2Ci.I2C_CON[13:12] OPMODE Bit Field
F/S I²C	0x0
HS I²C	0x1
SCCB	0x2
Reserved (not used)	0x3

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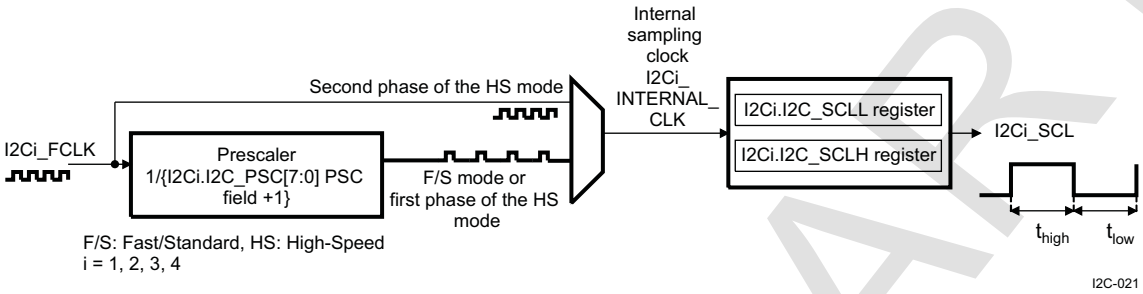
23.1.4.2 HS I²C Clocks

23.1.4.2.1 HS I²C Clocking

Figure 23-22 shows the I²C clock generation of the HS I²C controllers.

Figure 23-22. HS I²C Clock Generation



Each multimaster HS I²C controller uses the I2Ci_FCLK functional clock in the PRCM module. The internal sampling clock I2Ci_INTERNAL_CLK is generated by dividing the functional clock by the I2Ci.I2C_PSC[7:0] PSC bit field value + 1 in F/S mode, in SCCB mode, or in the first phase of HS mode; or by directly using the functional clock in the second phase of HS mode (prescaler is bypassed).

The low time of the I2Ci_SCL signal is determined by the I2Ci.I2C_SCLL[7:0] SCLL bit field in F/S mode, in SCCB mode, or in the first phase of HS mode; or by the I2Ci.I2C_SCLL[15:8] HSSCLL bit field in the second phase of HS mode.

The high time of the I2Ci_SCL signal is determined by the I2Ci.I2C_SCLH[7:0] SCLH bit field in F/S mode, in SCCB mode, or in the first phase of HS mode; or by the I2Ci.I2C_SCLH[15:8] HSSCLH bit field in the second phase of HS mode.

The low time of the I2C5 signal is determined by the PRM_VC_CFG_I2C_CLK[15:8] SCLL bit field in F/S mode or in the first phase of HS mode, or by the PRM_VC_CFG_I2C_CLK[31:24] HSSCLL bit field in the second phase of HS mode.

The high time of the I2C5 signal is determined by the PRM_VC_CFG_I2C_CLK[7:0] SCLH bit field in F/S mode or in the first phase of HS mode, or by the PRM_VC_CFG_I2C_CLK[23:16] HSSCLH bit field in the second phase of HS mode.

Table 23-8 lists the T_{LOW} and T_{HIGH} values in master mode only (in slave mode, the I²C controller does not generate the I²C clock).

Table 23-8. HS I²C T_{LOW} and T_{HIGH} Values of the I²C Clock

Mode	I²C Clock	t_{LOW}	t_{HIGH}	
			DFILTEREN bit = 0	DFILTEREN bit = 1
F/S, SCCB, or HS first phase	I2Ci_INTERNAL_CLK = I2Ci_FCLK / (I2Ci.I2C_PSC[7:0] PSC bit field + 1)	(I2Ci.I2C_SCLL[7:0] SCLL bit field value + 7) x I2Ci_INTERNAL_CLK period	(I2Ci.I2C_SCLH[7:0] SCLH bit field value + 5 + PROP_DELAY0) x I2Ci_INTERNAL_CLK period	(I2Ci.I2C_SCLH[7:0] SCLH bit field value + 5 + PROP_DELAY1) x I2Ci_INTERNAL_CLK period
HS second phase	I2Ci_FCLK	(I2Ci.I2C_SCLL[15:8] HSSCLL bit field value + 7) x I2Ci_FCLK period	(I2Ci.I2C_SCLH[15:8] HSSCLH bit field value + 5 + PROP_DELAY0) x I2Ci_FCLK period	(I2Ci.I2C_SCLH[15:8] HSSCLH bit field value + 5 + PROP_DELAY1) x I2Ci_FCLK period
F/S or HS first phase for I2C5	I2C5_FCLK	(PRM_VC_CFG_I2C_CLK[15:8] SCLL + 1) x I2C5_FCLK period	(PRM_VC_CFG_I2C_CLK[7:0] SCLH + 5 + PROP_DELAY0) x I2C5_FCLK period	(PRM_VC_CFG_I2C_CLK[7:0] SCLH + 5 + PROP_DELAY1) x I2C5_FCLK period

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Table 23-8. HS I²C T_{LOW} and T_{HIGH}Values of the I²C Clock (continued)

Mode	I²C Clock	t_{LOW}	t_{HIGH}	
			DFILTEREN bit = 0	DFILTEREN bit = 1
HS second phase for I2C5	I2C5_FCLK	(PRM_VC_CFG_I2C_CLK[31:24] HSSCLL + 1) x I2C5_FCLK period	(PRM_VC_CFG_I2C_CLK[23:16] HSSCLH + 5 + PROP_DELAY0) x I2C5_FCLK period	(PRM_VC_CFG_I2C_CLK[23:16] HSSCLH + 5 + PROP_DELAY1) x I2C5_FCLK period

NOTE: For HS mode, the I2Ci.I2C_SCLL[15:8] HSSCLL and I2Ci.I2C_SCLL[7:0] SCLL bit fields must be programmed (the first phase of an HS transaction is performed at F/S speed).

For HS mode, the I2Ci.I2C_SCLH[15:8] HSSCLH and I2Ci.I2C_SCLH[7:0] SCLH bit fields must be programmed (the first phase of an HS transaction is performed at F/S speed).

NOTE: The equations in Table 23-8 give the SCL timing values for SCLL/SCLH/HSSCLL/HSSCLH at HS I²C controller outputs. Actual T_{LOW} and T_{HIGH} periods may vary depending on the board (the load capacitance on the SCL signal). If necessary, any adjustments to the SCLL/SCLH/HSSCLL/HSSCLH values must be determined by measurements of actual SCL signal on the board

CAUTION

During active mode (the I2Ci.I2C_CON[15] I2C_EN bit is set to 1), make no changes to the I2Ci.I2C_SCLL and I2Ci.I2C_SCLH registers. Changes can result in unpredictable behavior.

NOTE: Each multimaster HS I²C controller can be used with an internal secondary pullup. This pullup is mandatory when the I²C controller is configured in HS mode for a bit rate of 3.4 Mbps, and the bus line capacitance exceeds 45 pF. Pullups can be programmed through:

- CONTROL_I2C_0[0] I2C1_SCL_PULLUPRESX bit or CONTROL_I2C_0[16] I2C1_SDA_PULLUPRESX bit for I2C1
- CONTROL_I2C_0[4] I2C2_SCL_PULLUPRESX bit or CONTROL_I2C_0[20] I2C2_SDA_PULLUPRESX bit for I2C2
- CONTROL_I2C_0[8] I2C3_SCL_PULLUPRESX bit or CONTROL_I2C_0[24] I2C3_SDA_PULLUPRESX bit for I2C3
- CONTROL_I2C_0[12] I2C4_SCL_PULLUPRESX bit or CONTROL_I2C_0[28] I2C4_SDA_PULLUPRESX bit for I2C4

The maximum bit rate specified by the SCCB specifications is 100 Kbps.

For more information see Section 18.4.12.9.8, *I2Cx I/Os Group Pullupresx Controls and Load Range Settings*.

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Table 23-9 lists the register values for obtaining the maximum I²C bit rates and the maximum period of the filtered spikes in F/S mode and HS mode.

Table 23-9. HS I²C Register Values for Maximum I²C Bit Rates in I²C F/S, I²C HS, and SCCB Modes[1]

	I²C Mode for I2Ci, where i = 1, 2, 3, 4				Description	SCCB Mode for I2Ci, where i = 2, 3		I²C Mode for I2C5 Fast and High-Speed Mode		
	Standard Mode	**Fast Mode**	**Fast Mode+**	**High-Speed Mode**						
I2Ci_FCLK frequency (MHz)	96					96		38.4		SYS_CLK clock frequency
I2Ci.I2C_PSC[7:0] PSC bit field value	**23**	**9**	**5**	**1**	Prescaler value for F/S and HS modes	**4**	Prescaler value for SCCB mode	Not accessible by software		
I2Ci_INTERNAL_CLK frequency (MHz)	4	9.6	19.2	96	19.2					
I2Ci.I2C_SCLL[7:0] SCLL bit field value	**13**	7	3	**113**	Value for F/S mode and first phase of HS mode	**89**	Value for SCCB mode	**PRM_VC_CFG_I2C_CLK[15:8] SCLL** (see Chapter 3, *Power, Reset, and Clock Management*)	43	Value for F/S mode and first phase of HS mode
I2Ci.I2C_SCLH[7:0] SCLH bit field value	**15**	**5**	4	**115**	Value for F/S mode and first phase of HS mode	**91**	Value for SCCB mode	**PRM_VC_CFG_I2C_CLK[7:0] SCLH** (see Chapter 3, *Power, Reset, and Clock Management*)	41	Value for F/S mode and first phase of HS mode
Maximum bit rate (Mbps)	0.1	0.4	1.0	0.4	F/S mode and first phase in HS mode maximum bit rate	0.1	SCCB mode maximum bit rate	Maximum bit rate (Mbps)	0.4	F/S mode and first phase in HS mode maximum bit rate
Maximum filter period (ns)	250	104	52	10		50		Maximum filter period (ns)	50	
I2Ci.I2C_SCLL[15:8] HSSCLL bit field value				**12**	Values for second phase of HS mode			**PRM_VC_CFG_I2C_CLK[31:24] HSSCLL** (see Chapter 3, *Power, Reset, and Clock Management*)	14	Values for second phase of HS mode
I2Ci.I2C_SCLH[15:8] HSSCLH bit field value				**5**	Values for second phase of HS mode			**PRM_VC_CFG_I2C_CLK[23:16] HSSCLH** (see Chapter 3, *Power, Reset, and Clock Management*)	0	Values for second phase of HS mode
HS mode maximum bit rate (Mbps)				3.31	HS mode maximum bit rate			HS mode maximum bit rate (Mbps)	3.2	HS mode maximum bit rate according to the corresponding SYS_CLK clock frequency
Maximum filter period (ns)				10					10	

[1] Programmable fields are in bold.

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NOTE: This table presents informative values only for the configuration parameters and the I2C bus performance obtained according to these values. The delays added by the analog pads are not considered in these figures.

NOTE: For I2Ci (where i = 1, 2, 3, 4)

I2Ci_INTERNAL_CLK freq = I2Ci_FCLK / (PSC + 1)

FS filter period = 1 / I2Ci_INTERNAL_CLK

HS filter period = 1 / I2Ci_FCLK freq

- If the DFILTEREN bit = 0:

  HS bit rate = I2Ci_FCLK freq / (HSSCLL+ 7 + HSSCLH + 5 + PROP_DELAY0)

  FS bit rate = I2Ci_INTERNAL_CLK / (SCLL + 7 + SCLH + 5 + PROP_DELAY0)
- If the DFILTEREN bit = 1:

  HS bit rate = I2Ci_FCLK freq / (HSSCLL+ 7 + HSSCLH + 5 + PROP_DELAY1)

  FS bit rate = I2Ci_INTERNAL_CLK / (SCLL + 7 + SCLH + 5 + PROP_DELAY1)

For I2C5 (SR):

I2C5_FCLK freq = SYS_CLK freq

HS/FS filter period = 1 / I2C5_FCLK freq

- If the DFILTEREN bit = 0:

  HS bit rate = I2C5_FCLK freq / (HSSCLL + 1 + HSSCLH + 5 + PROP_DELAY0)

  FS bit rate = I2C5_FCLK freq / (SCLL + 1 + SCLH + 5 + PROP_DELAY0)
- If the DFILTEREN bit = 1:

  HS bit rate = I2C5_FCLK freq / (HSSCLL + 1 + HSSCLH + 5 + PROP_DELAY1)

  FS bit rate = I2C5_FCLK freq / (SCLL + 1 + SCLH + 5 + PROP_DELAY1)

DFILTEREN refers to the VC_CFG_I2C_MODE[6] DFILTEREN bit. PROP_DELAYx (where x = 0 or 1) represents frequency-normalized I/O low-to-high propagation delay.

PROP_DELAY0 = 0 or 3 (values for bit rate maximum/minimum range)

PROP_DELAY1 = 1 or 4 (values for bit rate maximum/minimum range)

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23.1.4.2.2 HS I²C Automatic Blocking of the I²C Clock Feature (I²C Mode Only)

This feature offers the possibility for the LH to command the blocking of the I²C clock after the slave addressing phase, when the I²C controller is addressed by an external master device using a certain Own Address.

The release of the I²C clock can be performed independently for each Own Address (I2Ci.I2C_OA , where i = 1, 2, 3, 4 and I2Ci.I2C_OAx registers, where x = 1, 2, 3) by deasserting the corresponding bit in the I2Ci.I2C_SBLOCK register.

23.1.4.3 HS I²C Software Reset

Each multimaster HS I²C controller supports the software reset by accessing the I2Ci.I2C_SYSC[1] SRST bit (1: reset; 0: normal mode).

The software reset status can be checked by accessing the I2Ci.I2C_SYSS[0] RDONE bit (1: reset is done; 0: reset is ongoing).

To perform a software reset:

1. Ensure that the module is disabled (clear the I2Ci.I2C_CON[15] I2C_EN bit to 0).
2. Set the I2Ci.I2C_SYSC[1] SRST bit to 1.
3. Enable the module by setting I2Ci.I2C_CON[15] I2C_EN bit to 1.
4. Check the I2Ci.I2C_SYSS[0] RDONE bit until it is set to 1 to indicate the software reset is complete.

NOTE: The I2Ci.I2C_CON[15] I2C_EN bit can hold the functional clock domain of the multimaster HS I²C controller in reset after the device reset has been released. When the system bus reset is removed, this bit remains cleared. The functional part of the I²C controller is held in reset state while this bit is 0, and all configuration registers can be accessed.

The I2Ci.I2C_CON[15] I2C_EN bit must be set to 1 to enable the functional part of the I²C controller.

The I2Ci.I2C_SYSS[0] RDONE bit is asserted only after the module is enabled by setting the I2Ci.I2C_CON[15] I2C_EN bit to 1.

23.1.4.4 HS I²C Power Management

Table 23-10 describes power-management features available for the multimaster HS I²C controllers.

NOTE:

- For information about source clock gating and sleep/wake-up transitions description, see Section 3.1.1.1.2, *Module Level Clock Management*, in Chapter 3, *Power, Reset, and Clock Management*.
- For descriptions of EnaWakeUp, IdleMode, ClockActivity, and StandbyMode features, see Section 3.1.1.1.2, *Module Level Clock Management*, in Chapter 3, *Power, Reset, and Clock Management*.

Table 23-10. HS I²C Local Power-Management Features

Feature	Registers	Description
Clock auto gating	I2Ci.I2C_SYSC[0] AUTOIDLE	This bit allows a local power optimization inside the module
Slave idle modes	I2Ci.I2C_SYSC[4:3] IDLEMODE	Force-idle, no-idle, smart-idle, and smart-idle wake-up-capable modes are available.
Clock activity	I2Ci.I2C_SYSC[9:8] CLOCKACTIVITY	For configuration details, see Table 23-11.
Global wake-up enable	I2Ci.I2C_SYSC[2] ENAWAKEUP	This bit enables the wake-up feature at module level.

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NOTE: The voltage controllers, in which the HS I²C controller I2C5 are implemented, have no idle request/acknowledge mechanism. The idle modes for the voltage controllers are directly managed by the PRCM module.

Table 23-11. HS I²C Clock Activity Settings

I2Ci.I2C_SYSC[9:8] CLOCKACTIVITY	Clock State When Module is in IDLE State		Features Available/Unavailable When Module is in IDLE State
	I2Ci_ICLK	I2C_ FCLK	
00	OFF	OFF	Both clocks are disabled
10	OFF	ON	Interface clock is disabled; functional clock is enabled
01	ON	OFF	Functional clock is disabled; interface clock is enabled
11	ON	ON	Both clocks are enabled

CAUTION

The PRCM module has no hardware means of reading the settings of CLOCKACTIVITY. Thus, software must ensure consistent programming between the I2C CLOCKACTIVITY and I2C clock PRCM control bits. For a description of the ClockActivity feature, see Section 3.1.1.1.2, *Module Level Clock Management* in Chapter 3, *Power, Reset, and Clock Management*.

23.1.4.5 HS I²C Interrupt Requests

Table 23-12 lists the event flags, and their mask, that can cause module interrupts.

Table 23-12. HS I²C Events

Event Flag	Event Mask	Event Unmask	Map to	Description
I2Ci.I2C_IRQSTATUS[0] AL	I2Ci.I2C_IRQENABLE_SET[0] AL_IE	I2Ci.I2C_IRQENABLE_CLR[0] AL_IE	I2Ci_IRQ	Arbitration lost IRQ enabled status. This bit is automatically set by the hardware when it loses the Arbitration in master transmit mode, an interrupt is signaled to the MPU subsystem. During reads, it always returns 0.
I2Ci.I2C_IRQSTATUS[1] NACK	I2Ci.I2C_IRQENABLE_SET[1] NACK_IE	I2Ci.I2C_IRQENABLE_CLR[1] NACK_IE	I2Ci_IRQ	No acknowledgment IRQ enabled status. Bit is set when No Acknowledge has been received, an interrupt is signaled to MPU subsystem. Write 1 to clear this bit.
I2Ci.I2C_IRQSTATUS[2] ARDY	I2Ci.I2C_IRQENABLE_SET[2] ARDY_IE	I2Ci.I2C_IRQENABLE_CLR[2] ARDY_IE	I2Ci_IRQ	Register access ready IRQ enabled status. When set to 1 it indicates that previous access has been performed and registers are ready to be accessed again. An interrupt is signaled to MPU subsystem. Write 1 to clear.
I2Ci.I2C_IRQSTATUS[3] RRDY	I2Ci.I2C_IRQENABLE_SET[3] RRDY_IE	I2Ci.I2C_IRQENABLE_CLR[3] RRDY_IE	I2Ci_IRQ	Receive data ready IRQ enabled status. Set to 1 by core when receiver mode, a new data is able to be read. When set to 1 by core, an interrupt is signaled to MPU subsystem. Write 1 to clear.

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Table 23-12. HS I²C Events (continued)

Event Flag	Event Mask	Event Unmask	Map to	Description
I2Ci.I2C_IRQSTATUS[4] XRDY	I2Ci.I2C_IRQENABLE_SET[4] XRDY_IE	I2Ci.I2C_IRQENABLE_CLR[4] XRDY_IE	I2Ci_IRQ	Transmit data ready IRQ enabled status. Set to 1 by core when transmitter and when new data is requested. When set to 1 by core, an interrupt is signaled to MPU subsystem. Write 1 to clear.
I2Ci.I2C_IRQSTATUS[5] GC	I2Ci.I2C_IRQENABLE_SET[5] GC_IE	I2Ci.I2C_IRQENABLE_CLR[5] GC_IE	I2Ci_IRQ	General call IRQ enabled status. Set to 1 by core when General call address detected and interrupt signaled to MPU subsystem. Write 1 to clear.
I2Ci.I2C_IRQSTATUS[6] STC	I2Ci.I2C_IRQENABLE_SET[6] STC_IE	I2Ci.I2C_IRQENABLE_CLR[6] STC_IE	I2Ci_IRQ	Start Condition IRQ enabled status.
I2Ci.I2C_IRQSTATUS[7] AERR	I2Ci.I2C_IRQENABLE_SET[7] AERR_IE	I2Ci.I2C_IRQENABLE_CLR[7] AERR_IE	I2Ci_IRQ	Access Error IRQ enabled status.
I2Ci.I2C_IRQSTATUS[8] BF	I2Ci.I2C_IRQENABLE_SET[8] BF_IE	I2Ci.I2C_IRQENABLE_CLR[8] BF_IE	I2Ci_IRQ	Access Error IRQ enabled status.
I2Ci.I2C_IRQSTATUS[9] AAS	I2Ci.I2C_IRQENABLE_SET[9] AAS_IE	I2Ci.I2C_IRQENABLE_CLR[9] AAS_IE	I2Ci_IRQ	Address recognized as slave IRQ enabled status.
I2Ci.I2C_IRQSTATUS[10] XUDF	I2Ci.I2C_IRQENABLE_SET[10] XUDF_IE	I2Ci.I2C_IRQENABLE_CLR[10] XUDF_IE	I2Ci_IRQ	Transmit underflow enabled status. Writing into this bit has no effect.
I2Ci.I2C_IRQSTATUS[11] ROVR	I2Ci.I2C_IRQENABLE_SET[11] ROVR_IE	I2Ci.I2C_IRQENABLE_CLR[11] ROVR_IE	I2Ci_IRQ	Receive overrun enabled status. Writing into this bit has no effect.
I2Ci.I2C_IRQSTATUS[12] BB	I2Ci.I2C_IRQENABLE_SET[12] BB_IE	I2Ci.I2C_IRQENABLE_CLR[12] BB_IE	I2Ci_IRQ	Bus busy enabled status. Writing into this bit has no effect.
I2Ci.I2C_IRQSTATUS[13] RDR	I2Ci.I2C_IRQENABLE_SET[13] RDR_IE	I2Ci.I2C_IRQENABLE_CLR[13] RDR_IE	I2Ci_IRQ	Receive draining IRQ enabled status.
I2Ci.I2C_IRQSTATUS[14] XDR	I2Ci.I2C_IRQENABLE_SET[14] XDR_IE	I2Ci.I2C_IRQENABLE_CLR[14] XDR_IE	I2Ci_IRQ	Transmit draining IRQ enabled status.

23.1.4.6 HS I²C DMA Requests

Each multimaster HS I²C controller can generate two DMA requests to the system DMA (sDMA) controller. Table 23-13 lists the DMA requests with mapping on the sDMA controller. For information about DMA generation, see Section 23.1.4.8.3, *HS I²C FIFO DMA Mode (I²C Mode Only)*.

Table 23-13. HS I²C DMA Requests

Name	Source	Destination	Description
I2C1_DMA_TX	I2C1	S_DMA_26	I2C1 DMA write request to inform the sDMA to write new data in the I2C1.I2C_DATA[7:0] register
I2C1_DMA_RX	I2C1	S_DMA_27	I2C1 DMA read request to inform the sDMA to read the data in the I2C1.I2C_DATA[7:0] register
I2C2_DMA_TX	I2C2	S_DMA_28	I2C2 DMA write request to inform the sDMA to write new data in the I2C2.I2C_DATA[7:0] register
I2C2_DMA_RX	I2C2	S_DMA_29	I2C2 DMA read request to inform the sDMA to read the data in the I2C2.I2C_DATA[7:0] register
I2C3_DMA_TX	I2C3	S_DMA_24	I2C3 DMA write request to inform the sDMA to write new data in the I2C3.I2C_DATA[7:0] register

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Table 23-13. HS I²C DMA Requests (continued)

Name	Source	Destination	Description
I2C3_DMA_RX	I2C3	S_DMA_25	I2C3 DMA read request to inform the sDMA to read the data in the I2C3.I2C_DATA[7:0] register
I2C4_DMA_TX	I2C4	S_DMA_123	I2C4 DMA write request to inform the sDMA to write new data in the I2C4.I2C_DATA[7:0] register
I2C4_DMA_RX	I2C4	S_DMA_124	I2C4 DMA read request to inform the sDMA to read the data in the I2C4.I2C_DATA[7:0] register

NOTE: The HS I²C controller I2C5 does not generate any DMA requests.

23.1.4.7 HS I²C Programmable Multislave Channel Feature (I²C Mode Only)

This feature allows each multimaster HS I²C controller to be addressed using four separate Own Addresses configured in the I2Ci.I2C_OA and I2Ci.I2C_OAx registers (where x = 1, 2, 3). An additional register (I2Ci.I2C_ACTOA) is used to indicate to the LH which address is used by the external master to communicate with the I²C controller.

Each Own Address can be independently configured in 7-bit or 10-bit mode by setting the corresponding bit (I2Ci.I2C_CON[7] XOA, I2Ci.I2C_CON[6] XOA1, I2Ci.I2C_CON[5] XOA2, or I2Ci.I2C_CON[4] XOA3).

23.1.4.8 HS I²C FIFO Management

Each multimaster HS I²C controller implements two internal 8-bit FIFOs, the RX and TX FIFOs.

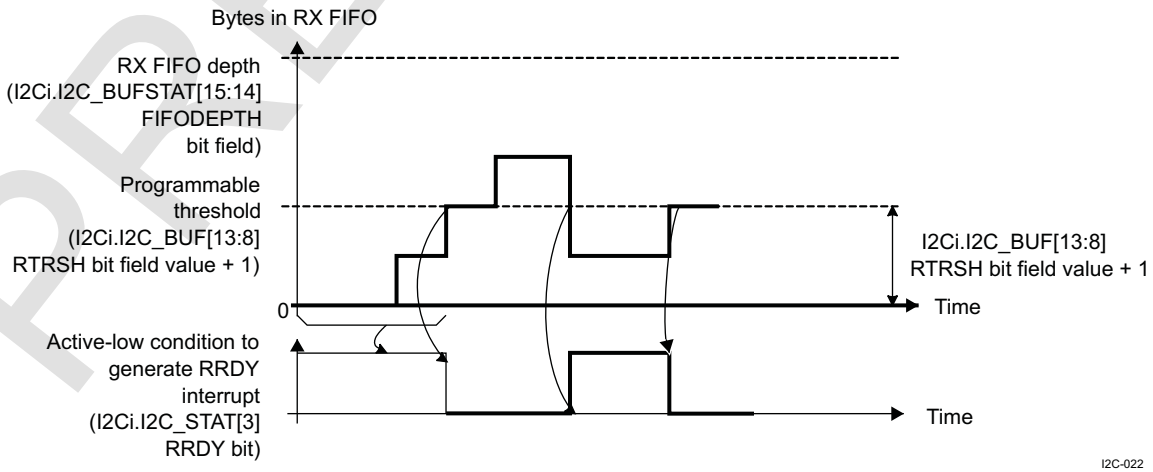
The depth of the RX and TX FIFOs can be checked by reading the I2Ci.I2C_BUFSTAT[15:14] FIFODEPTH bit field (0x0: 8 bytes, 0x1: 16 bytes, 0x2: 32 bytes, and 0x3: 64 bytes).

23.1.4.8.1 HS I²C FIFO Interrupt Mode

In first in first out (FIFO) interrupt mode (relevant interrupts enabled by the I2Ci.I2C_IE register), an interrupt signal informs the processor of the receiver and transmitter status. These interrupts are raised when the RX/TX FIFO thresholds (defined by the I2Ci.I2C_BUF[13:8] RTRSH bit field value + 1 for the RX FIFO or the I2Ci.I2C_BUF[5:0] TXTRSH bit field value + 1 for the TX FIFO) are reached; the interrupt signals instruct the LH to transfer data to the destination (from the I²C controller in receive mode and/or from any source to the I²C controller FIFO in transmit mode).

Figure 23-23 and Figure 23-24 show receive and transmit operations, respectively, from a FIFO management point of view.

Figure 23-23. HS I²C Receive FIFO Interrupt Request Generation



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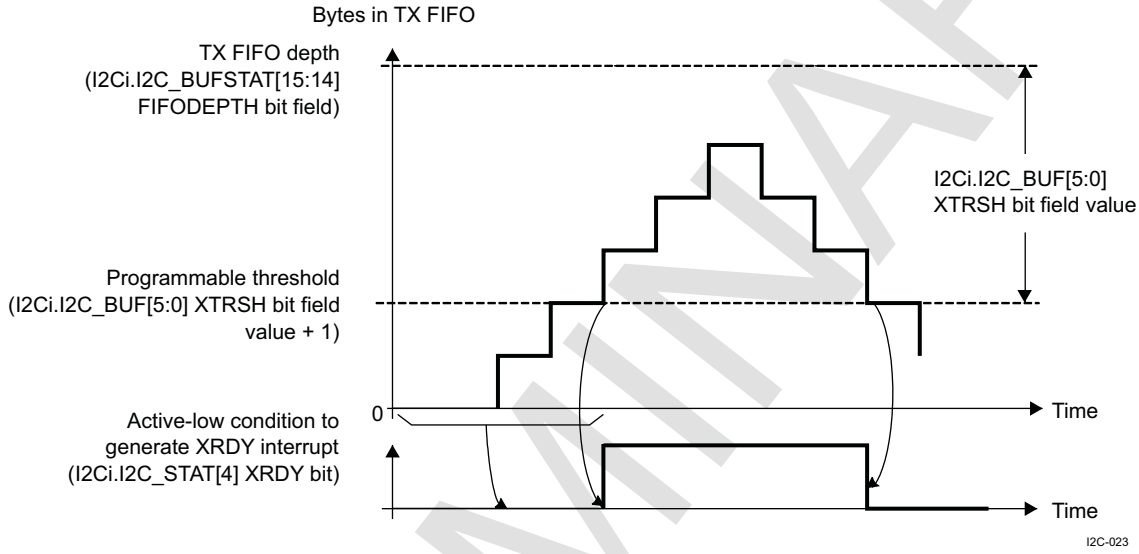
In Figure 23-23, the RRDY interrupt condition shows that the condition for generating an RRDY interrupt is achieved. The interrupt request is generated when this signal is active, and it can be cleared only by the LH by writing 1 in the I2Ci.I2C_STAT[3] RRDY bit. If the condition is still present after clearing the previous interrupt, another interrupt request is generated.

In receive mode, an RRDY interrupt is generated as soon as the FIFO reaches its receive threshold (I2Ci.I2C_BUF[13:8] RTRSH bit field value + 1). The interrupt can be deasserted only when the LH has handled enough bytes to make the number of bytes in the RX FIFO lower than the programmed threshold. For each interrupt, the LH can be configured to read a number of bytes equal to the value of the RX FIFO threshold.

Figure 23-24. HS I²C Transmit FIFO Interrupt Request Generation



In Figure 23-24, the XRDY interrupt condition shows that the condition for generating an XRDY interrupt is achieved. The interrupt request is generated when TX FIFO is empty or when the TX FIFO threshold is not reached, and the LH can clear the XRDY status bit by setting the I2Ci.I2C_STAT[4] XRDY bit to 1 after transmitting the configured number of bytes. If the condition is still present after clearing the previous interrupt, another interrupt request is generated.

In interrupt mode, the module offers two options for the LH application to handle the interrupts:

- When detecting an interrupt request (XRDY or RRDY type), the LH can write/read 1 data byte to/from the TX/RX FIFO and then clear the interrupt. The module reasserts the interrupt until the interrupt condition is not met.
- When detecting an interrupt request (XRDY or RRDY type), the LH can be programmed to write/read the amount of data bytes specified by the corresponding FIFO threshold (I2C_BUF[5:0] TXTRSH + 1 or I2C_BUF[5:0] RXTRSH + 1). In this case, the interrupt condition is cleared and the next interrupt is asserted again when the XRDY or RRDY condition is met again.

If the second-interrupt-serving approach is used, an additional mechanism (draining feature) is implemented for cases where the transfer length is not a multiple of the FIFO threshold value (see Section 23.1.4.8.4, *Draining Feature [I²C Mode Only]*).

NOTE: In slave transmit mode (the I2Ci.I2C_CON[10] MST bit is cleared and the I2Ci.I2C_CON[9] TRX bit is set to 1), the draining feature must not be used, because the transfer length is not known at configuration time, and the external master can end the transfer at any point by not acknowledging 1 data byte. If the draining feature is used in slave transmit mode, data can remain in the TX FIFO without being transmitted over the I²C bus. In this case, the TX FIFO must be cleared by setting the I2Ci.I2C_BUF[6] TXFIFO_CLR bit.

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NOTE: In SCCB mode, the RX and TX threshold values must be set to 1 by setting the I2Ci.I2C_BUF[13:8]RTRSH and I2Ci.I2C_BUF[5:0] TXTRSH fields to 0x0.

23.1.4.8.2 HS I²C FIFO Polling Mode

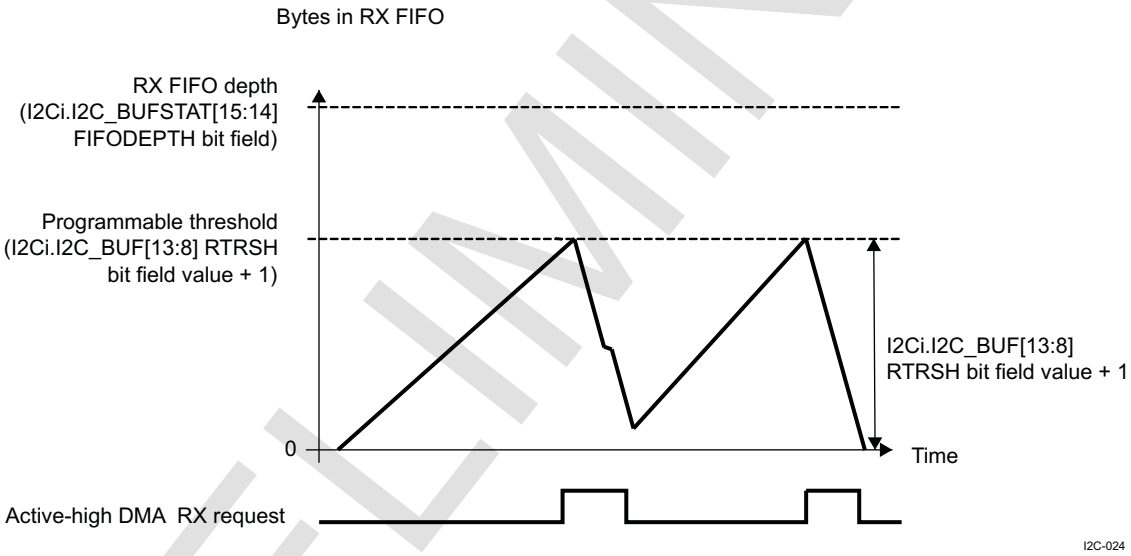
In FIFO polling mode (the I2Ci.I2C_IE[4] XRDY_IE and I2Ci.I2C_IE[3] RRDY_IE bits are disabled, and the I2Ci.I2C_BUF[15] RDMA_EN and I2Ci.I2C_BUF[7] XDMA_EN bits are disabled), the status of the module (receiver or transmitter) can be checked by polling the I2Ci.I2C_STAT[4] XRDY and the I2Ci.I2C_STAT[3] RRDY bits (the I2Ci.I2C_STAT[13] RDR and I2Ci.I2C_STAT[14] XDR bits can also be polled if the draining feature is enabled). The I2Ci.I2C_STAT[4] XRDY and I2Ci.I2C_STAT[3] RRDY bits accurately reflect the interrupt conditions described in the discussion of FIFO interrupt mode.

23.1.4.8.3 HS I²C FIFO DMA Mode (I²C Mode Only)

In receive mode, a DMA request is generated by the I2Ci_DMA_RX signal as soon as the RX FIFO exceeds its threshold level (the I2Ci.I2C_BUF[13:8] RTRSH bit field value + 1). This request is deasserted when the number of bytes defined by the threshold level is read by the DMA controller.

Figure 23-25 shows the DMA request generation in receive mode.

Figure 23-25. HS I²C Receive FIFO DMA Request Generation



In transmit mode, a DMA request is automatically asserted by the I2Ci_DMA_TX signal when the TX FIFO is empty. This request is deasserted when the number of bytes (the 2Ci.I2C_BUF[5:0] TXTRSH bit field value + 1) is written in the FIFO by the DMA controller. If an insufficient number of bytes is written, the sDMA request remains active. Figure 23-26 and Figure 23-27 show the DMA TX transfers with different values for the I2Ci.I2C_BUF[5:0] TXTRSH bit field.

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Figure 23-26. HS I²C Transmit FIFO Request Generation (High Threshold)

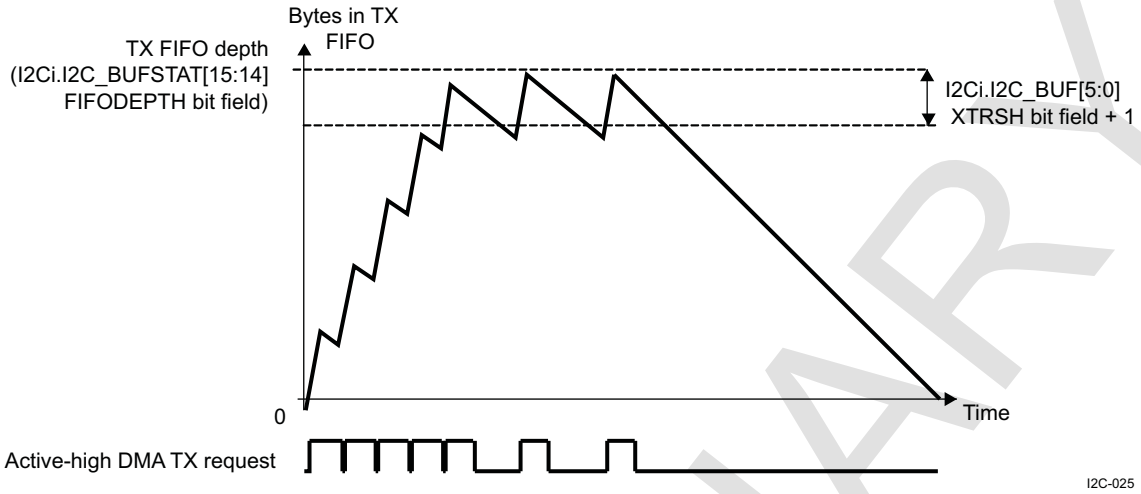
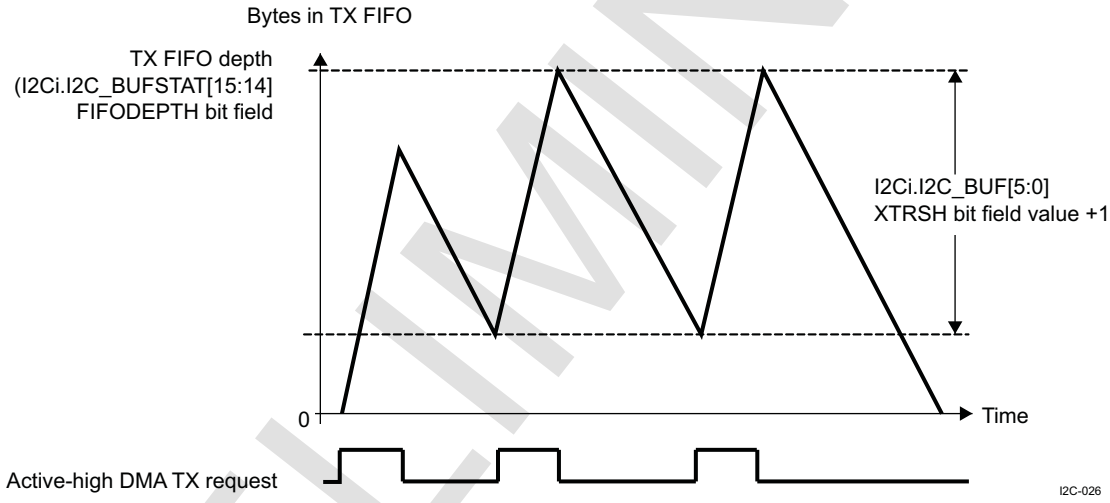


Figure 23-27. HS I²C Transmit FIFO Request Generation (Low Threshold)



NOTE: In SCCB mode, the RX and TX threshold values must be set to 1 by setting the I2Ci.I2C_BUF[13:8] RTRSH and I2Ci.I2C_BUF[5:0] XTRSH bit fields to 0x0.

The I²C module allows the user to clear the RX or TX FIFO by setting the I2Ci.I2C_BUF[14] RXFIFO_CLR and I2Ci.I2C_BUF[6] TXFIFO_CLR registers, respectively, which act like software reset for the FIFOs. In DMA mode, these bits also reset the DMA state-machines. The FIFO clearing feature can be used when the following conditions are met:

- The module is configured as a transmitter.
- The external receiver responds with a NACK in the middle of the transfer.
- Data in the TX FIFO is waiting to be transferred.

23.1.4.8.4 HS I²C Draining Feature (I²C Mode Only)

The draining feature is implemented to handle the end of a transfer whose length is not a multiple of the FIFO threshold values (the I2Ci.I2C_BUF[13:8] RTRSH bit field value + 1 for the RX threshold and I2Ci.I2C_BUF[5:0] TXTRSH field value + 1 for the TX threshold). It can also transfer the remaining number of bytes (because the threshold is not reached).

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This feature prevents the LH or the DMA controller from trying more FIFO accesses than necessary (for example, to generate at the end of a transfer a DMA RX request having fewer bytes in the FIFO than the configured DMA transfer length). Otherwise, an AERR interrupt is generated by the I2Ci.I2C_STAT[7] AERR bit.

The draining mechanism generates an interrupt using the I2Ci.I2C_STAT[13] RDR or I2Ci.I2C_STAT[14] XDR bit at the end of the transfer, informing the LH that it must check the amount of data left to be transferred (the I2Ci.I2C_BUFSTAT[13:8] RXSTAT or I2Ci.I2C_BUFSTAT[5:0] TXSTAT bit fields) and enable the draining feature of the DMA controller by reconfiguring the DMA transfer length according to this value (when the DMA mode is enabled) or perform only the required number of data accesses (when the DMA mode is disabled).

In receive mode (master or slave), if the RX FIFO threshold (the I2Ci.I2C_BUF[13:8] RTRSH bit field value + 1) is not reached, but the transfer ends on the I²C bus and data remains in the RX FIFO (less than the threshold), the receive draining interrupt (the I2Ci.I2C_STAT[13] RDR bit) is asserted to inform the LH that it can read the amount of data in the RX FIFO (the I2Ci.I2C_BUFSTAT[13:8] RXSTAT bit field). The LH performs a number of data read accesses equal to the I2Ci.I2C_BUFSTAT[13:8] RXSTAT bit field (interrupt or polling mode), or reconfigures the sDMA controller with the required value to drain the FIFO.

In master transmit mode, if the TX FIFO threshold (I2Ci.I2C_BUF[5:0] TXTRSH bit field value + 1) is not reached, but the amount of data remaining to be written in the TX FIFO is less than the threshold, the transmit draining interrupt (the I2Ci.I2C_STAT[14] XDR bit) is asserted to inform the LH that it can read the amount of data remaining to be written in the TX FIFO (the I2Ci.I2C_BUFSTAT[5:0] TXSTAT bit field). The LH must write the required number of data bytes specified by the I2Ci.I2C_BUFSTAT[5:0] TXSTAT bit field value or reconfigure the sDMA controller with the value required to transfer the last bytes to the FIFO.

In master mode, the LH can alternately not check the values of the I2Ci.I2C_BUFSTAT[5:0] TXSTAT and I2Ci.I2C_BUFSTAT[13:8] RXSTAT bit fields, the LH can obtain this information internally (by computing the I2Ci.I2C_CNT[15:0] DATACOUNT bit field value modulo I2Ci.I2C_BUF[13:8] RTRSH or I2Ci.I2C_BUF[5:0] TXTRSH).

By default, the draining feature is disabled; it can be enabled using the I2Ci.I2C_IE[14] XDR_IE or I2Ci.I2C_IE[13] RDR_IE bits (default disabled) only for transfers with lengths not equal to the threshold values (I2Ci.I2C_BUF[5:0] TXTRSH bit field value + 1 for the TX threshold or I2Ci.I2C_BUF[13:8] RTRSH bit field value + 1 for the RX threshold).

23.1.4.9 HS I²C Noise Filter

The noise filter is used to suppress any noise that is 50 ns or less in case of F/S operation modes and SCCB modes, and any noise that is 10 ns or less in case of HS mode operation. The noise filter is always one period of the I2Ci_INTERNAL_CLK clock. This way, for HS mode operation (prescaler bypassed), the filter suppresses spikes of less than 10.4 ns.

For SCCB modes (for example, I2Ci.I2C_PSC[7:0] PSC bit field = 4), the maximum width of suppressed spikes is 52 ns.

To ensure correct filtering, the prescaler must be programmed accordingly by the 2Ci.I2C_PSC[7:0] PSC bit field.

23.1.4.10 HS I²C Write and Read Operations in SCCB Mode

In SCCB mode, the multimaster HS I²C controller can write or read a single byte to or from the external SCCB device.

To write a single byte to the external SCCB device, the multimaster HS I²C controller must be configured in multimaster transmitter mode by setting the I2Ci.I2C_CON[10] MST and I2Ci.I2C_CON[9] TRX bits to 1. The external device slave address (7-bit address of the ID value) is set in the I2Ci.I2C_SA register; the register address (8-bit subaddress in the external SCCB device) is set in the I2Ci.I2C_OA0 register. The 8-bit data to be transmitted is written by the LH in the I2Ci.I2C_DATA register.

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To read a single byte from the external SCCB device, the multimaster HS I²C controller must be configured in multimaster receiver mode by setting the I2Ci.I2C_CON[10] MST bit to 1 and by clearing the I2Ci.I2C_CON[9] TRX bit to 0. The external device slave address (7-bit address of the ID value) is set in the I2Ci.I2C_SA register; the register address (8-bit subaddress in the external SCCB device) is set in the I2Ci.I2C_OA0 register. The 8-bit data received from the external SCCB device is read by the LH from the I2Ci.I2C_DATA register.

NOTE: In SCCB mode, the RX and TX thresholds must be set to 1 by configuring the I2Ci.I2C_BUF[13:8] RTRSH and I2Ci.I2C_BUF[5:0]XTRSH fields to 0x0.

23.1.4.11 HS I²C System Test Mode

A system test mode is available for multimaster HS I²C controller module testing. This mode is enabled by setting the I2Ci.I2C_SYSTEST[15] ST_EN bit to 1. When this bit is cleared to 0, the I²C controller is configured in normal operation mode.

In system test mode, the I2Ci_SYSTEST[13:12] TMODE bit field selects the type of test. Table 23-14 lists the tests available for the multimaster HS I²C controllers.

Table 23-14. HS I²C List of Tests

I2Ci.I2C_SYSTEST[13:12] TMODE	Test	Description
00	Functional mode	Normal operation mode
01	Reserved (not used)	
10	Test of i2ci_scl serial clock line	The i2ci_scl line is driven with a permanent clock as if mastered with the parameters set in the I2Ci.I2C_PSC, I2Ci.I2C_SCLL, and I2Ci.I2C_SCLH registers.
11	Loop-back mode + i2ci_scl/ i2ci_sda input/output	In master transmit mode only, data transmitted out of the I2Ci.I2C_DATA register (write action) is received in the same I2Ci.I2C_DATA register through an internal path through the FIFO buffers. The DMA and interrupt requests are normally generated if they are enabled. Moreover, the i2ci_scl, i2ci_sda, and i2ci_sccbe lines are controlled with the I2Ci.I2C_SYSTEST[4:0] bits..

NOTE: When the I2Ci.I2C_SYSTEST[13:12] TMODE bit field is set to 11, the I²C controller must be configured in I²C F/S (the I2Ci.I2C_CON[13:12] OPMODE set to 00) or I²C HS mode (the I2Ci.I2C_CON[13:12] OPMODE set to 01). The loop-back mode is not available in SCCB mode (the 2Ci.I2C_CON[13:12] OPMODE = b10).

NOTE: In normal operation mode (I2Ci.I2C_SYSTEST[15] ST_EN clear to 0), the I2Ci.I2C_SYSTEST[4:0] bits that control the i2ci_scl, i2ci_sda, and i2ci_sccbe lines in system test mode are read-only bits.

In system test mode (I2Ci.I2C_SYSTEST[15] ST_EN set to 1), the I2Ci.I2C_STAT[5:0] status bits can be set to 1 when the I2Ci.I2C_SYSTEST[11] SSB bit is set to 1. Clearing the I2Ci.I2C_SYSTEST[11] SSB bit to 0 does not clear the I2Ci.I2C_STAT[5:0] bits to 0. The I2Ci.I2C_STAT[5:0] bit field can be cleared to 0 only by writing 1 in the corresponding bits.

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23.1.5 HS I²C Programming Guide

23.1.5.1 HS I²C Low-Level Programming Models

23.1.5.1.1 HS I²C Programming Model in I²C Mode

This section describes the programming model of the multimaster HS I²C controllers configured in I²C mode.

23.1.5.1.1.1 Main Program

23.1.5.1.1.1.1 Configure the Module Before Enabling the I²C Controller

Before enabling the I²C controller, perform the following:

1. Enable the functional and interface clocks.
2. Program the prescaler to obtain an approximately 12-MHz internal sampling clock by programming the corresponding value in the I2Ci.I2C_PSC[7:0] PSC field. This value depends on the frequency of the functional clock (I2Ci_FCLK).
3. Program the I2Ci.I2C_SCLL[7:0] SCLL and I2Ci.I2C_SCLH[7:0] SCLH bit fields to obtain a bit rate of 100 Kbps, 400 Kbps or 1Mbps. These values depend on the internal sampling clock frequency (see Table 23-8).
4. (Optional) Program the I2Ci.I2C_SCLL[15:8] HSSCLL and I2Ci.I2C_SCLH[15:8] HSSCLH bit fields to obtain a bit rate of 400 Kbps or 3.4 Mbps (for the second phase of HS mode). These values depend on the internal sampling clock frequency (see Table 23-8).
5. (Optional) If a bit rate of 3.4 Mbps is used and the bus line capacitance exceeds 45 pF, see Section 18.4.8, *PAD Functional Multiplexing and Configuration.*
6. Configure the Own Address of the I2C controller by storing it in the I2Ci.I2C_OA register. Up to four Own Addresses can be programmed in the I2Ci.I2C_OAx registers (where x = 0, 1, 2, 3) for each I²C controller.

   NOTE: For a 10-bit address, set the corresponding expand Own Address bit in the I2Ci.I2C_CON register.

7. Set the TX threshold (in transmitter mode) and the RX threshold (in receiver mode) by setting the I2Ci.I2C_BUF[5:0] TXTRSH bit field to (TX threshold to 1) and the I2Ci.I2C_BUF[13:8]RTRSH bit field to (RX threshold to 1), where the TX and RX thresholds are greater than or equal to 1.
8. Take the I²C controller out of reset by setting the I2Ci.I2C_CON[15] I2C_EN bit to 1.

23.1.5.1.1.1.2 Initialize the I²C Controller

To initialize the I²C controller, perform the following steps:

1. Configure the I2Ci.I2C_CON register:
   - For master or slave mode, set the I2Ci.I2C_CON[10] MST bit (0: slave; 1: master).
   - For transmitter or receiver mode, set the I2Ci.I2C_CON[9] TRX bit (0: receiver; 1: transmitter).
2. If using an interrupt to transmit and receive data, set the corresponding bit in the I2Ci.I2C_IE register to 1 (the I2Ci.I2C_IE[4] XRDY_IE bit for the transmit interrupt, the I2Ci.I2C_IE[3] RRDY bit for the receive interrupt).
3. If using DMA to receive and transmit data, set the corresponding bit in the I2Ci.I2C_BUF register to 1 (the I2Ci.I2C_BUF[15] RDMA_EN bit for the receive DMA channel, the I2Ci.I2C_BUF[7] XDMA_EN bit for the transmit DMA channel).

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23.1.5.1.1.1.3 Configure Slave Address and the Data Control Register

In master mode, configure the slave address register by programming the I2Ci.I2C_SA[9:0] SA bit field and the number of data bytes (I²C data payload) associated with the transfer by programming the I2Ci.I2C_CNT[15:0] DCOUNT bit field.

NOTE: For a 10-bit address, set the I2Ci.I2C_CON[8] XSA bit to 1.

23.1.5.1.1.1.4 Initiate a Transfer

Poll the I2Ci.I2C_STAT[12] BB bit. If it is cleared to 0 (bus not busy), configure the I2Ci.I2C_CON[0] STT and I2Ci.I2C_CON[1] STP bits. To initiate a transfer, the I2Ci.I2C_CON[0] STT bit must be set to 1, and it is not mandatory to set the I2Ci.I2C_CON[1] STP bit to 1.

23.1.5.1.1.1.5 Receive Data

Poll the I2Ci.I2C_STAT[3] RRDY bit, or use the RRDY interrupt (the I2Ci.I2C_IE[3] RRDY_IE bit must be set to 1) or the DMA RX channel (the I2Ci.I2C_BUF[15] RDMA_EN bit must be set to 1) to read the receive data in the I2Ci.I2C_DATA register.

If the transfer length does not equal the RX FIFO threshold (I2Ci.I2C_BUF[13:8] RTRSH field + 1), use the draining feature (enable the RDR interrupt by setting the I2Ci.I2C_IE[13] RDR_IE bit to 1).

NOTE: In receive mode only, the I2Ci.I2C_STAT[11] ROVR (receive overrun) bit indicates whether the receiver has experienced overrun. An overrun condition occurs when the shift register and the RX FIFO are full. An overrun condition does not result in data loss; the I²C controller simply holds i2ci_scl to low to prevent other bytes from being received.

The I2Ci.I2C_STAT[7] AERR bit is set to 1 when a read access is performed in the I2Ci.I2C_DATA register while the RX FIFO is empty. The corresponding interrupt can be enabled by setting the I2Ci.I2C_IE[7] AERR_IE bit to 1.

23.1.5.1.1.1.6 Transmit Data

Poll the I2Ci.I2C_STAT[4] XRDY bit, or use the XRDY interrupt (the I2Ci.I2C_IE[4] XRDY_IE bit must be set to 1) or the DMA TX channel (the I2Ci.I2C_BUF[7] XDMA_EN bit must be set to 1) to write data to the I2Ci.I2C_DATA register.

If the transfer length does not equal the TX FIFO threshold (I2Ci.I2C_BUF[5:0] TXTRSH field + 1), use the draining feature (enable the XDR interrupt by setting the I2Ci.I2C_IE[14] XDR_IE bit to 1).

NOTE: In transmit mode only, the I2Ci.I2C_STAT[10] XUDF bit indicates whether the transmitter has experienced underflow.

In master transmit mode, underflow occurs when the shift register and the TX FIFO are empty and there are still some bytes to transmit (the value of the I2Ci.I2C_CNT[15:0] DCOUNT bit field is not 0).

In slave transmit mode, underflow occurs when the shift register and the TX FIFO are empty and the external I²C master device still requests data bytes to be read.

The I2Ci.I2C_STAT[7] AERR bit is set to 1 when a write access is performed in the I2Ci.I2C_DATA register while the TX FIFO is full. The corresponding interrupt can be enabled by setting the I2Ci.I2C_IE[7] AERR_IE bit to 1.

23.1.5.1.1.2 Interrupt Subroutine Sequence

1. Test for arbitration lost (the I2Ci.I2C_STAT[0] AL it) and resolve accordingly.
2. Test for no acknowledgment (the I2Ci.I2C_STAT[1] NACK bit) and resolve accordingly.
3. Test for register access ready (the I2Ci.I2C_STAT[2] ARDY bit) and resolve accordingly.

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4. Test for receive data ready (the I2Ci.I2C_STAT[3] RRDY bit) and resolve accordingly.
5. Test for transmit data ready (the I2Ci.I2C_STAT[4] XRDY bit) and resolve accordingly.
6. Test for general call (the I2Ci.I2C_STAT[5] GC bit) and resolve accordingly.
7. Test for start (S) condition (the I2Ci.I2C_STAT[6] STC bit) and resolve accordingly. For this test, the functional clock must be inactive.
8. Test for access error (the I2Ci.I2C_STAT[7] AERR bit) and resolve accordingly.
9. Test for bus free (the I2Ci.I2C_STAT[8] BF bit) and resolve accordingly.

23.1.5.1.1.3 Programming Flow Diagrams

Figure 23-28 through Figure 23-36 are procedure flow charts for programming the F/S and HS I²C modes.

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Figure 23-28. HS I²C Setup Procedure

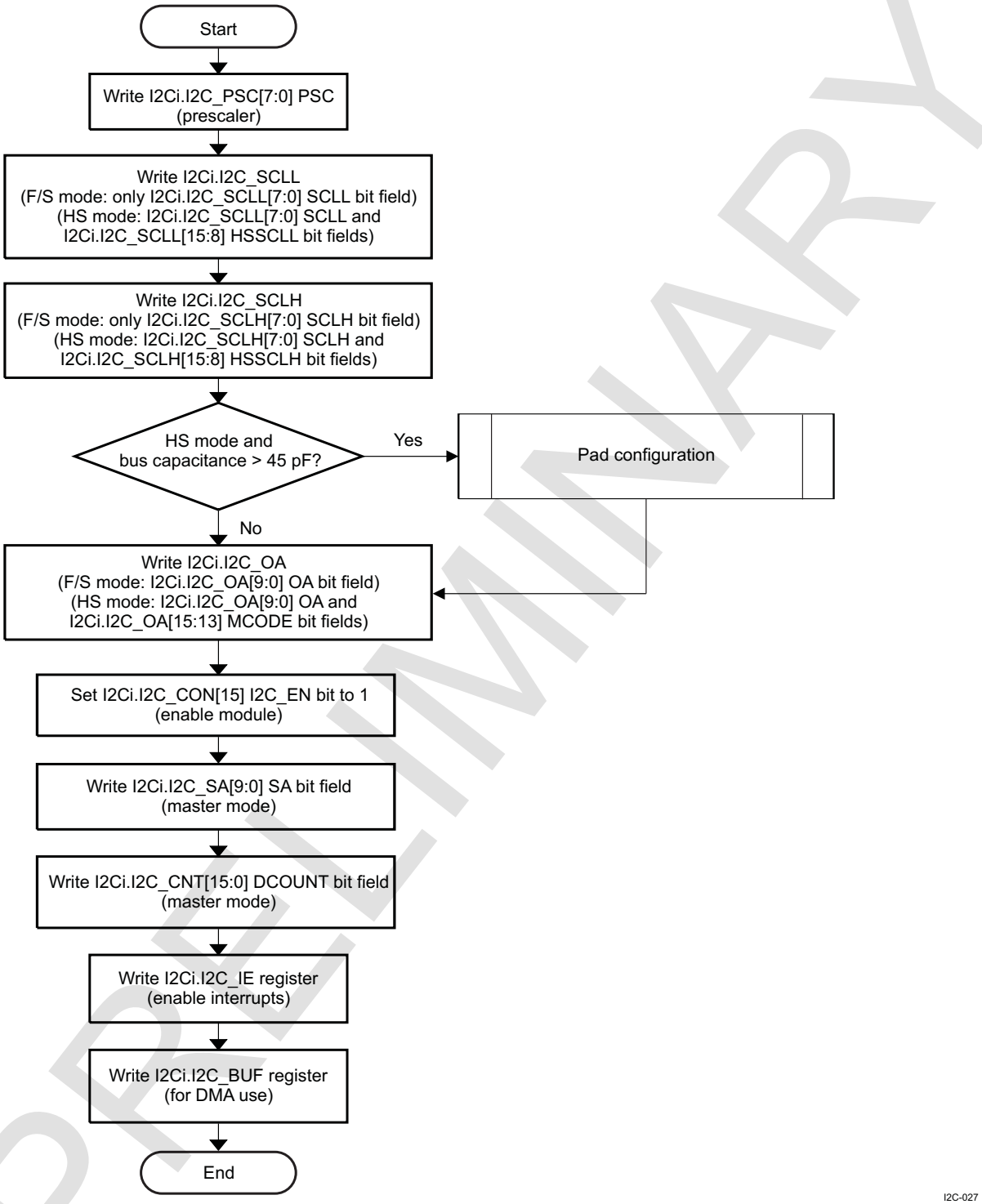

Table 23-15. HS I²C Subprocess call summary for Sequence - Setup Procedure

Register Name	Register Name
Pad configuration	Refer to Section 18.4.8 *PAD Functional Multiplexing and Configuration.*

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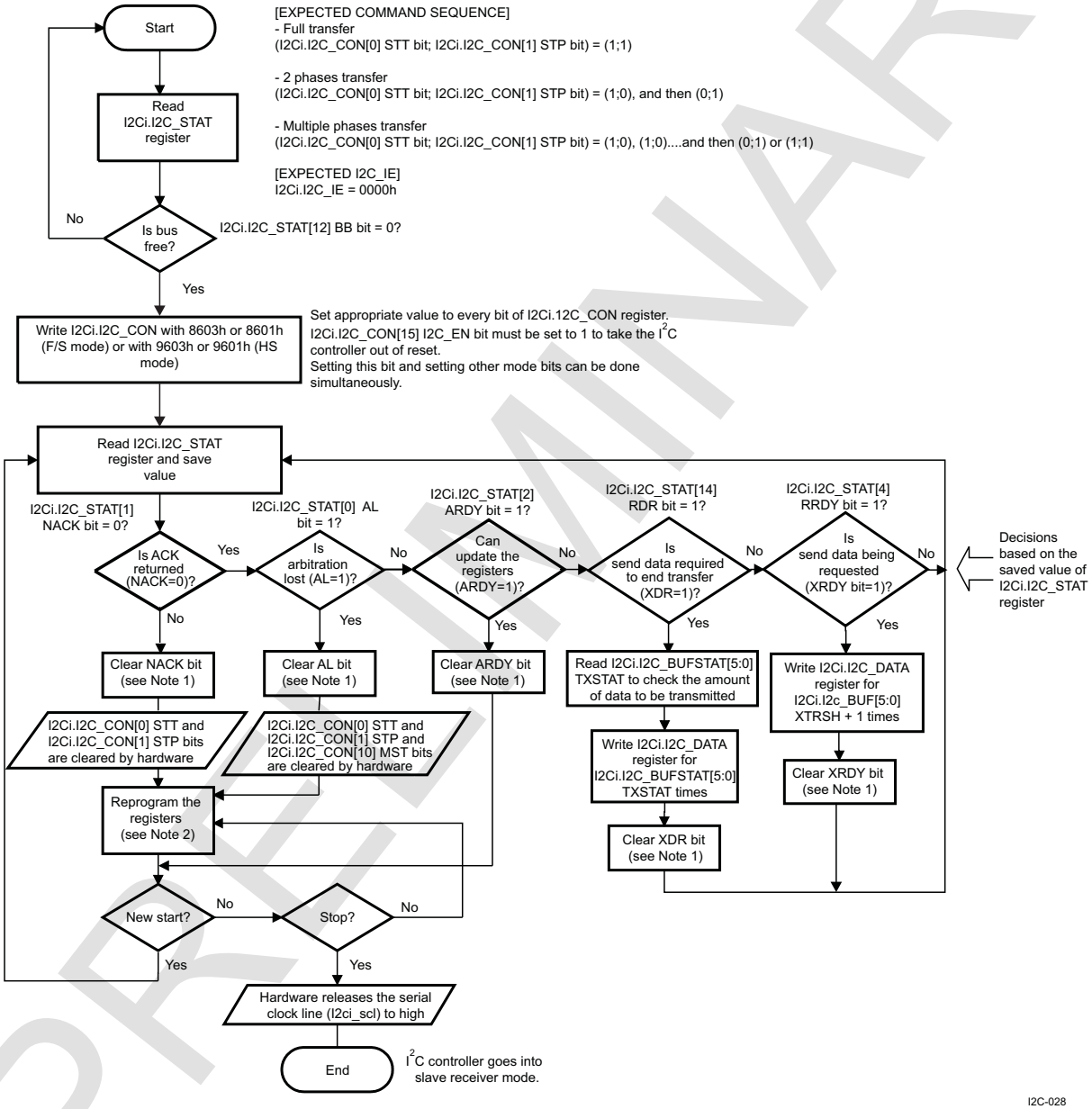
Table 23-16. HS I²C Register call summary for Sequence - Setup Procedure

Register Name	Register Name	Register Name
I2Ci.I2C_PSC (1)	I2Ci.I2C_CON (1)	I2Ci.I2C_BUF (1)
I2Ci.I2C_SCLL (1)	I2Ci.I2C_SA (1)	I2Ci.I2C_IE (1)
I2Ci.I2C_SCLH (1)	I2Ci.I2C_CNT (1)	I2Ci.I2C_OA (1)

(1) i = 1 to 4

Figure 23-29. HS I²C Master Transmitter Mode, Polling Method, in F/S and HS Modes



(1) The NACK, AL, ARDY, XDR, and XRDY bits are cleared by writing 1 to each corresponding bit in the I2Ci.I2C_STAT register.

(2) Reprogram the registers means: I2Ci.I2C_CON[11] STB and/or I2Ci.I2C_CON[10] MST bit and/or I2Ci.I2C_SA[9:0] SA register and/or I2Ci.I2C_CNT[15:0] DCOUNT register and/or I2Ci.I2C_CON[0] STT bit and/or I2Ci.I2C_CON[1] STP bit.

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Table 23-17. HS I²C Register call summary for Sequence - Master Transmitter Mode, Polling Method, in F/S and HS Modes

Register Name	Register Name	Register Name
I2Ci.I2C_STAT [1]	I2Ci.I2C_DATA [1]	I2Ci.I2C_CON [1]
I2Ci.I2C_BUFSTAT [1]	I2Ci.I2C_CON [1]	I2Ci.I2C_BUF [1]

[1] i = 1 to 4

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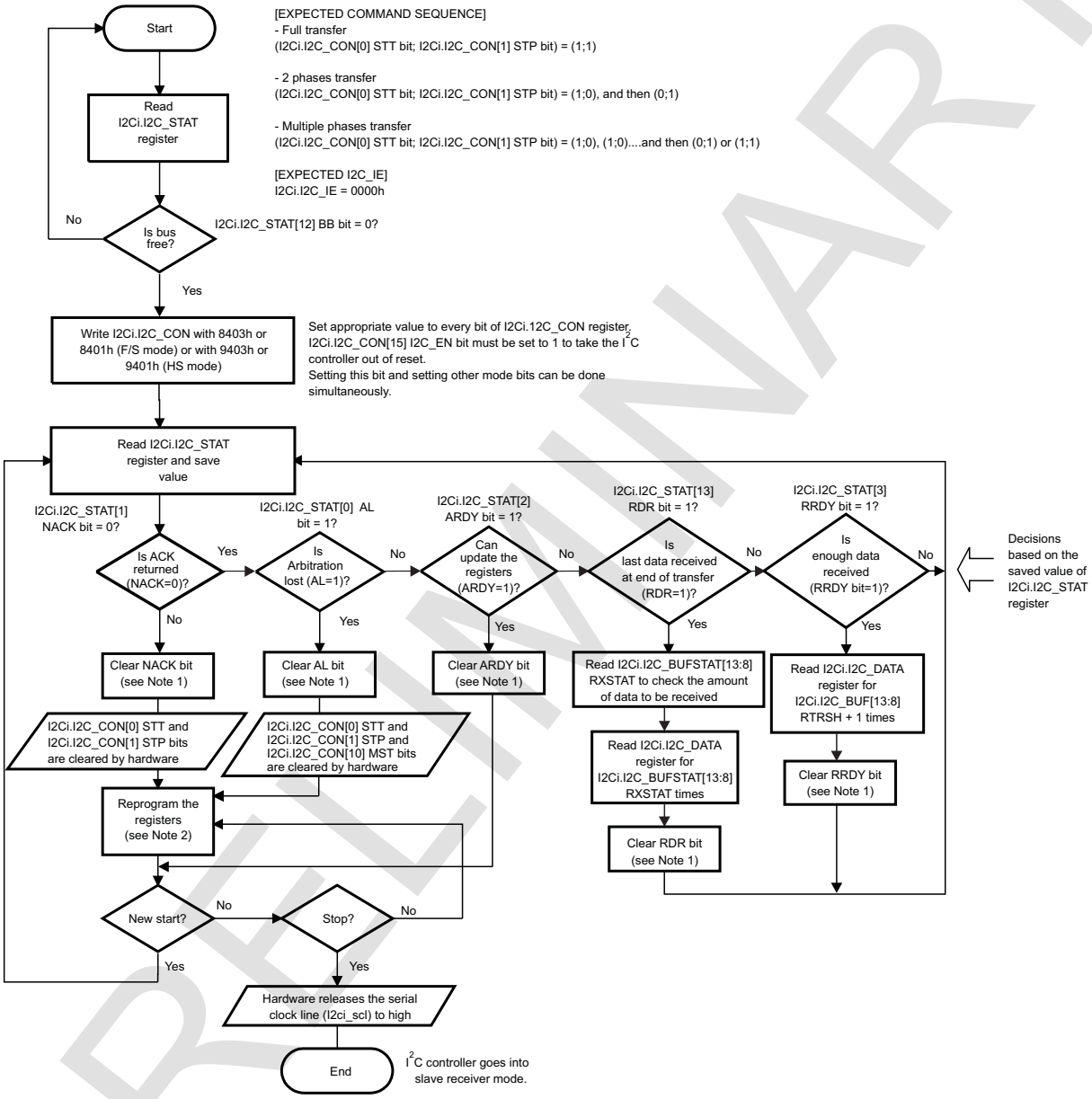
NOTE: In HS mode, the Sr condition and clock frequency switching are automatically generated by the multimaster HS I²C controller.

Figure 23-30. HS I²C Master Receiver Mode, Polling Method, in F/S and HS Modes



(1) The NACK, AL, ARDY, RDR, and RRDY bits are cleared by writing 1 to each corresponding bit in the I2Ci.I2C_STAT register.

(2) Reprogram registers means: I2Ci.I2C_CON[11] STB and/or I2Ci.I2C_CON[10] MST bit and/or I2Ci.I2C_SA[9:0] SA register and/or I2Ci.I2C_CNT[15:0] DCOUNT register and/or I2Ci.I2C_CON[0] STT bit and/or I2Ci.I2C_CON[1] STP bit.

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Table 23-18. HS I²C Register call summary for Sequence - Master Receiver Mode, Polling Method, in F/S and HS Modes

Register Name	Register Name	Register Name
I2Ci.I2C_STAT (1)	I2Ci.I2C_BUFSTAT (1)	I2Ci.I2C_BUF (1)
I2Ci.I2C_CON (1)	I2Ci.I2C_DATA (1)	

(1) i = 1 to 4

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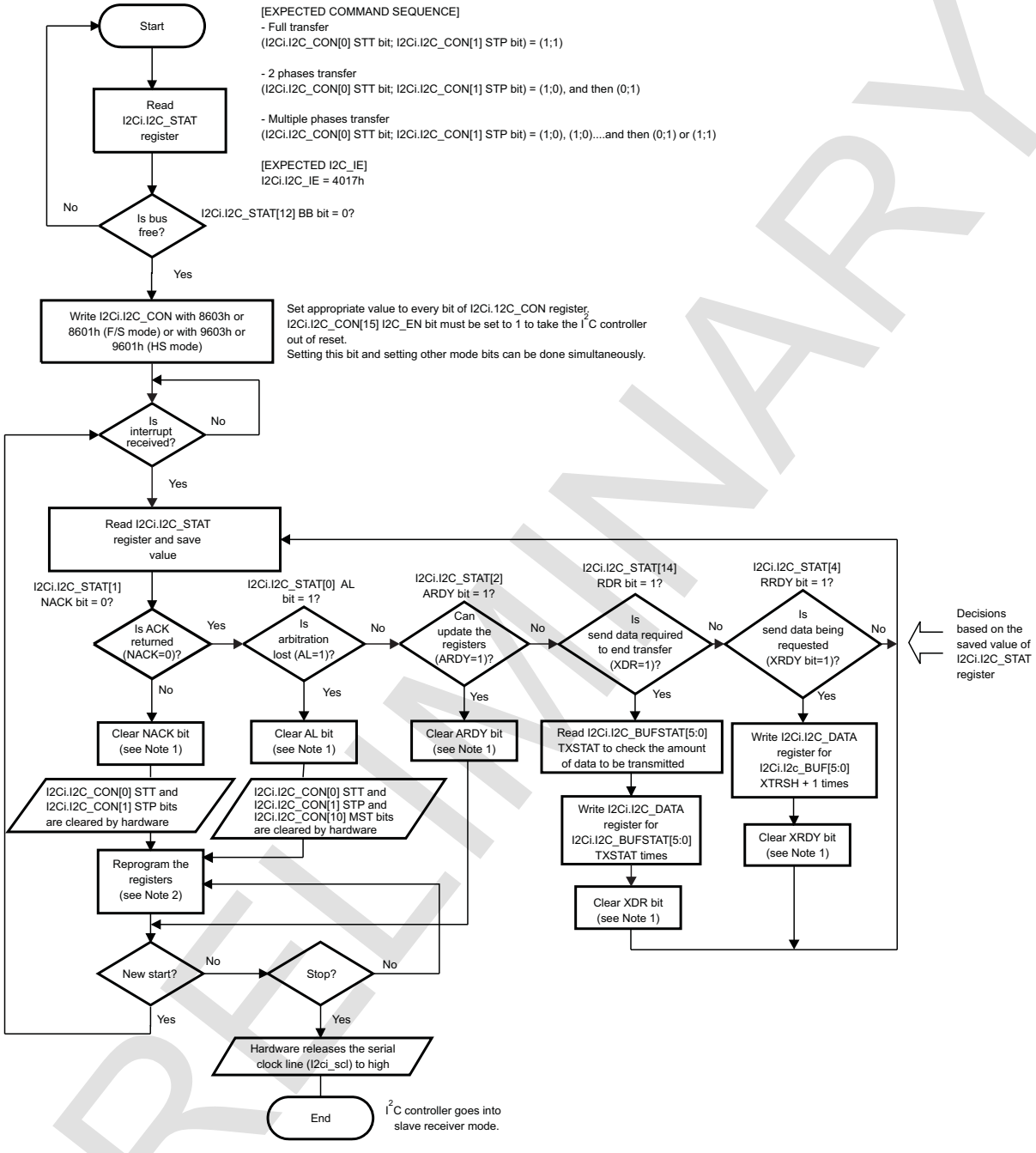
Figure 23-31. HS I²C Master Transmitter Mode, Interrupt Method, in F/S and HS Modes



(1) The NACK, AL, ARDY, XDR, and XRDY bits are cleared by writing 1 to each corresponding bit in the I2Ci.I2C_STAT register.

(2) Reprogram registers means: I2Ci.I2C_CON[11] STB and/or I2Ci.I2C_CON[10] MST bit and/or I2Ci.I2C_SA[9:0] SA register and/or I2Ci.I2C_CNT[15:0] DCOUNT register and/or I2Ci.I2C_CON[0] STT bit and/or I2Ci.I2C_CON[1] STP bit.

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Table 23-19. HS I²C Register call summary for Sequence - Master Transmitter Mode, Interrupt Method, in F/S and HS Modes

Register Name	Register Name	Register Name
I2Ci.I2C_STAT (1)	I2Ci.I2C_BUFSTAT (1)	I2Ci.I2C_BUF (1)
I2Ci.I2C_CON (1)	I2Ci.I2C_DATA (1)	

(1) i = 1 to 4

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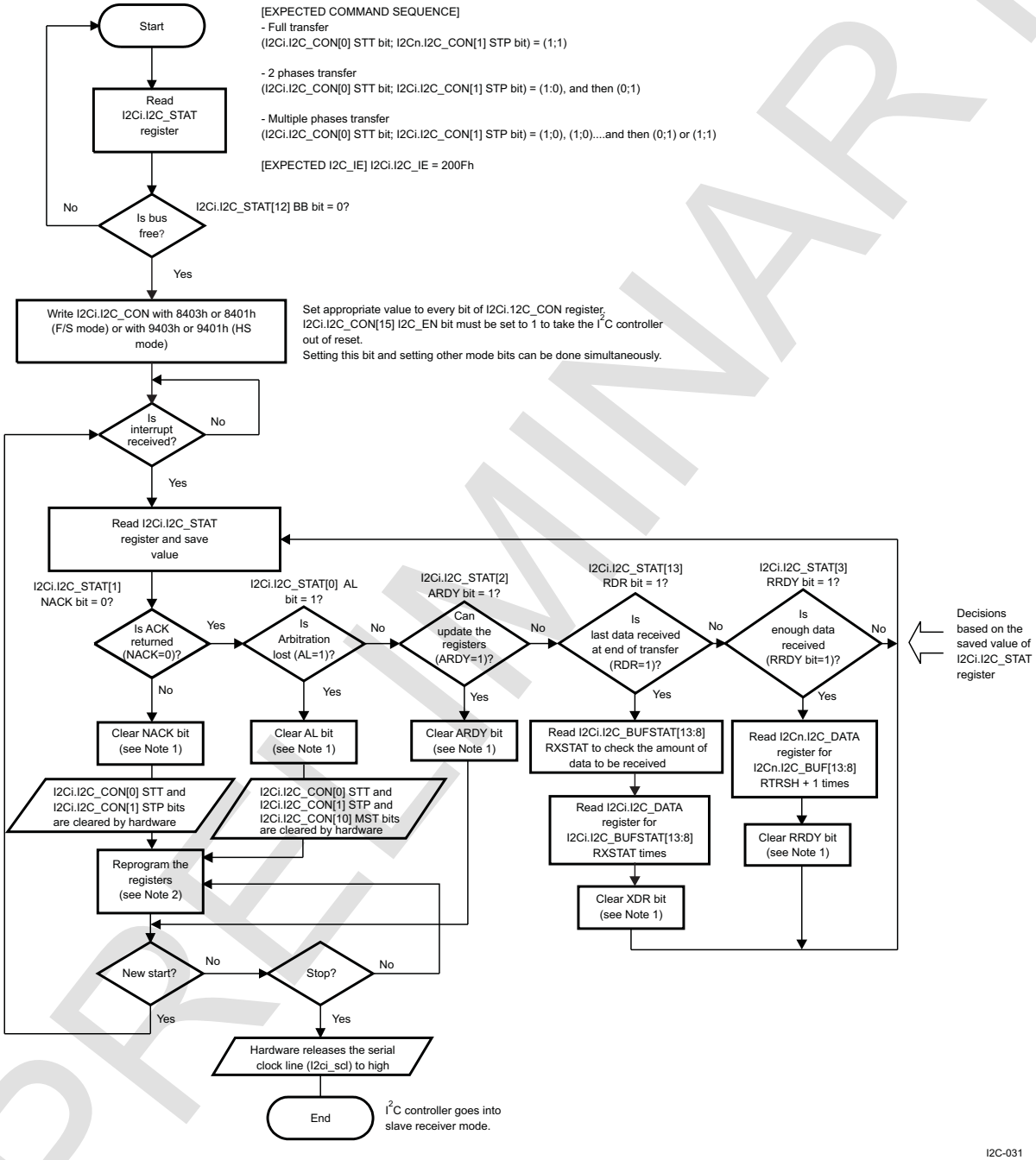
NOTE: In HS mode, the Sr condition and clock frequency switching are automatically generated by the multimaster HS I²C controller.

Figure 23-32. HS I²C Master Receiver Mode, Interrupt Method, in F/S and HS Modes



(1) The NACK, AL, ARDY, RDR, and RRDY bits are cleared by writing 1 to each corresponding bit in the I2Ci.I2C_STAT register.

(2) Reprogram registers means: I2Ci.I2C_CON[11] STB and/or I2Ci.I2C_CON[10] MST bit and/or I2Ci.I2C_SA[9:0] SA register and/or I2Ci.I2C_CNT[15:0] DCOUNT register and/or I2Ci.I2C_CON[0] STT bit and/or I2Ci.I2C_CON[1] STP bit.

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Table 23-20. HS I²C Register call summary for Sequence - Master Receiver Mode, Interrupt Method, in F/S and HS Modes

Register Name	Register Name	Register Name
I2Ci.I2C_STAT (1)	I2Ci.I2C_BUFSTAT (1)	I2Ci.I2C_BUF (1)
I2Ci.I2C_CON (1)	I2Ci.I2C_DATA (1)	

(1) i = 1 to 4

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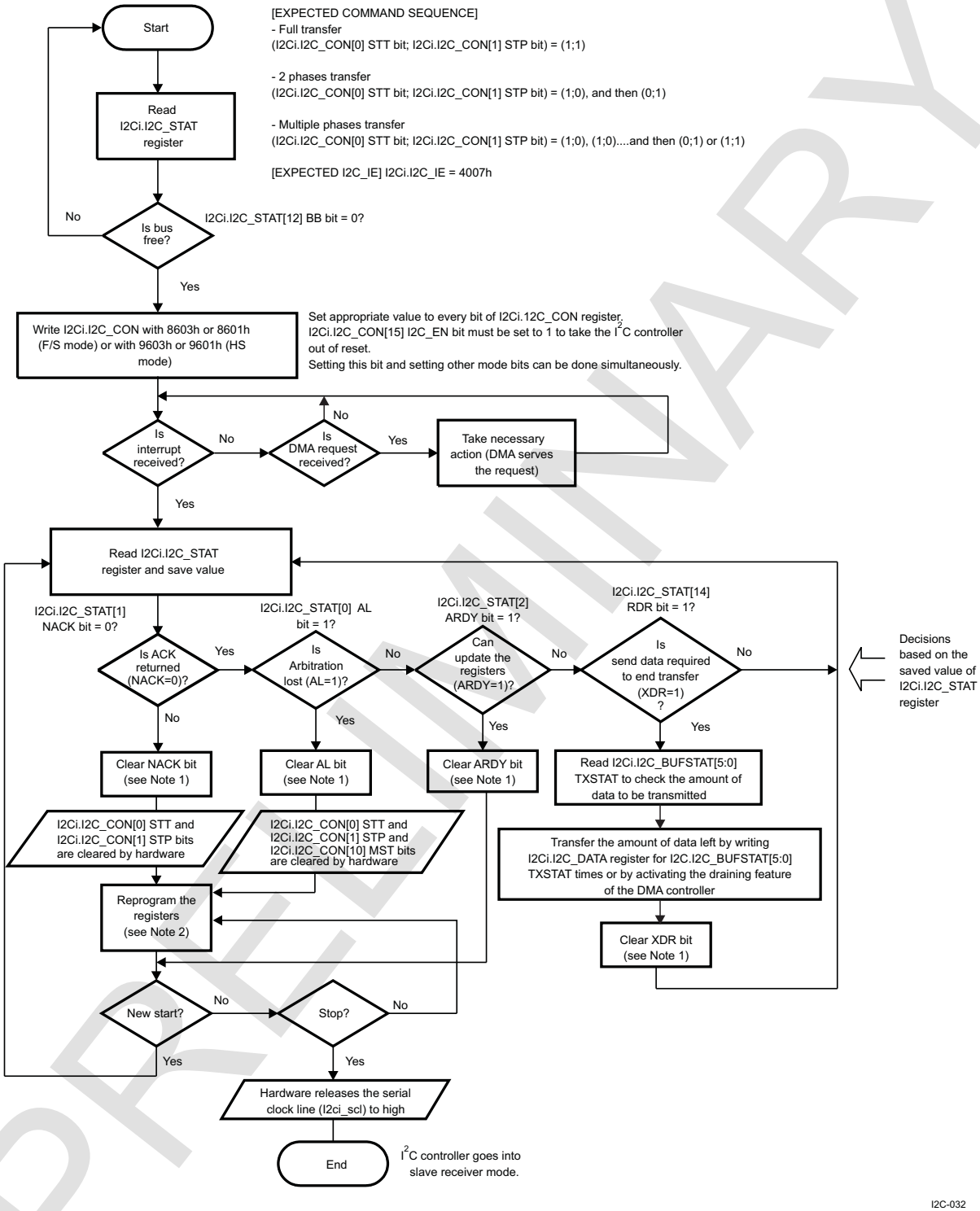
Figure 23-33. HS I²C Master Transmitter Mode, DMA Method in F/S and HS Modes



(1) The NACK, AL, ARDY, and XDR bits are cleared by writing 1 to each corresponding bit in the I2Ci.I2C_STAT register.

(2) Reprogram registers means: I2Ci.I2C_CON[11] STB and/or I2Ci.I2C_CON[10] MST bit and/or I2Ci.I2C_SA[9:0] SA register and/or I2Ci.I2C_CNT[15:0] DCOUNT register and/or I2Ci.I2C_CON[0] STT bit and/or I2Ci.I2C_CON[1] STP bit.

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Table 23-21. HS I²C Register call summary for Sequence - Master Transmitter Mode, DMA Method in F/S and HS Modes

Register Name	Register Name
I2Ci.I2C_STAT (1)	I2Ci.I2C_BUFSTAT (1)
I2Ci.I2C_CON (1)	I2Ci.I2C_DATA (1)

(1) i = 1 to 4

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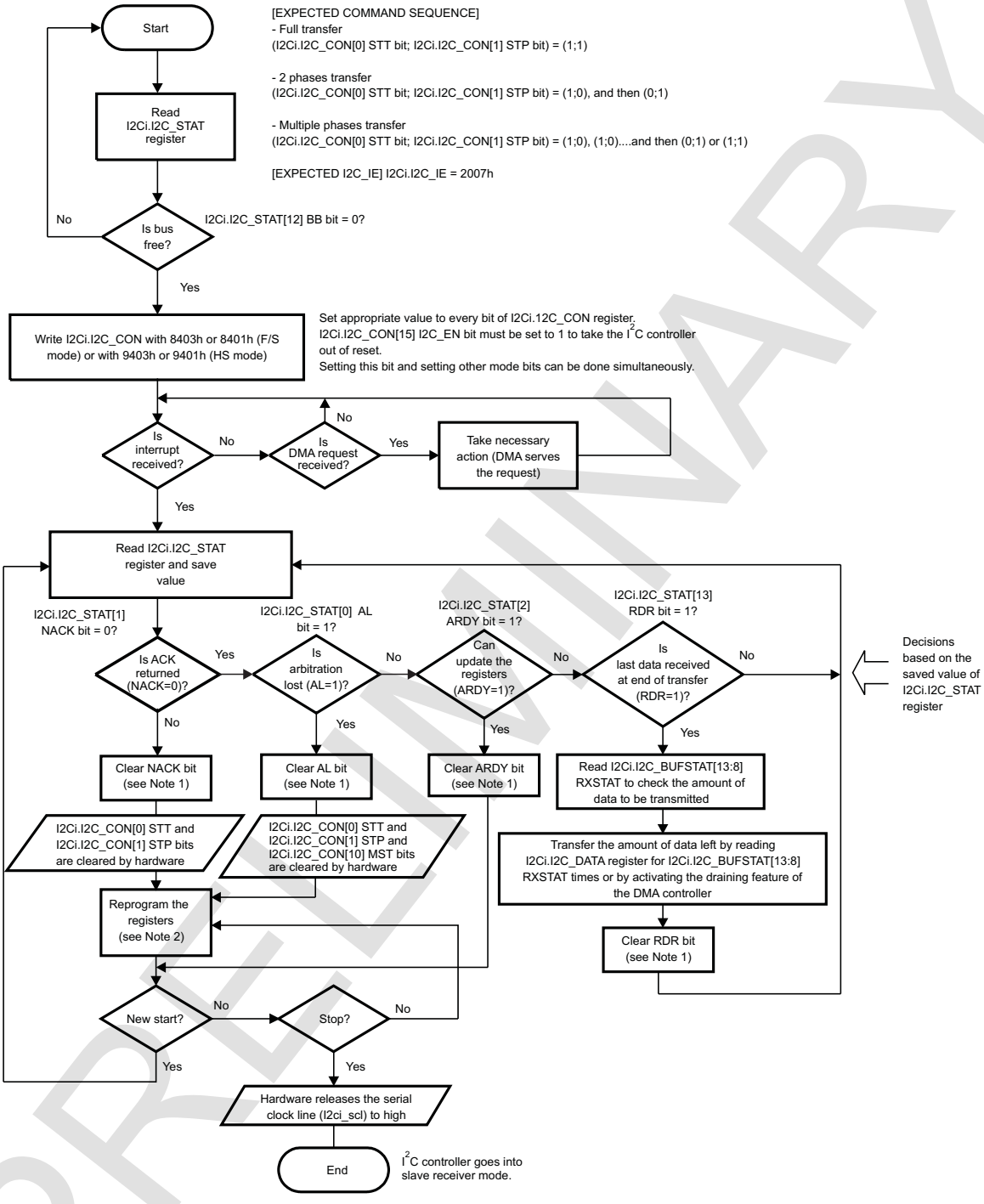
Figure 23-34. HS I²C Master Receiver Mode, DMA Method in F/S and HS Modes



(1) In HS mode, the Sr condition and clock frequency switching are automatically generated by the multimaster HS I²C controller.

(2) The NACK, AL, ARDY, and RDR bits are cleared by writing 1 to each corresponding bit in the I2Ci.I2C_STAT register.

(3) Reprogram registers means: I2Ci.I2C_CON[11] STB and/or I2Ci.I2C_CON[10] MST bit and/or I2Ci.I2C_SA[9:0] SA register and/or I2Ci.I2C_CNT[15:0] DCOUNT register and/or I2Ci.I2C_CON[0] STT bit and/or I2Ci.I2C_CON[1] STP bit.

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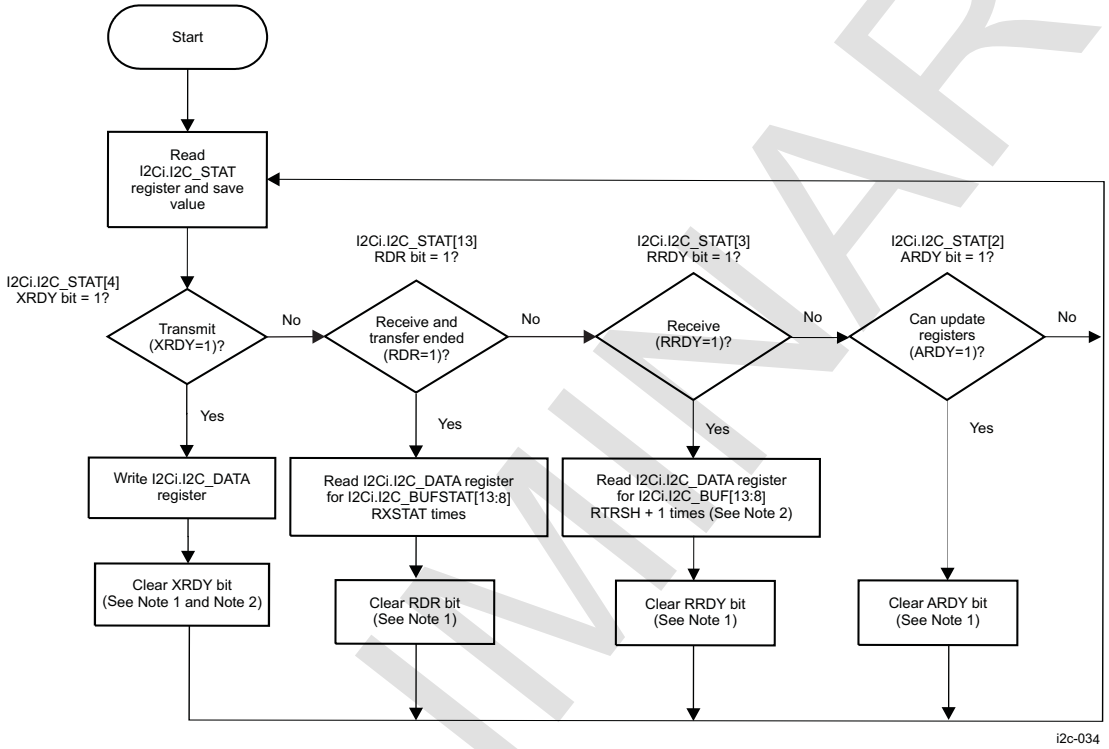
Table 23-22. HS I²C Register call summary for Sequence - Master Receiver Mode, DMA Method in F/S and HS Modes

Register Name	Register Name
I2Ci.I2C_STAT (1)	I2Ci.I2C_BUFSTAT (1)
I2Ci.I2C_CON (1)	I2Ci.I2C_DATA (1)

(1) i = 1 to 4

Figure 23-35. HS I²C Slave Transmitter/Receiver Mode, Polling



(1) The XRDY, RDR, RRDY, and ARDY bits are cleared by writing 1 to each corresponding bit in the I2Ci.I2C_STAT register.

(2) In slave transmitter mode, the amount of data requested by the external master I²C device is unknown; thus, the I2Ci.I2C_BUF[5:0] TXTRSH bit field must be configured to 0x0 (TX threshold = 1).

Table 23-23. HS I²C Register call summary for Sequence - Slave Transmitter/Receiver Mode, Polling

Register Name	Register Name
I2Ci.I2C_STAT (1)	I2Ci.I2C_BUFSTAT (1)
I2Ci.I2C_DATA (1)	I2Ci.I2C_BUF (1)

(1) i = 1 to 4

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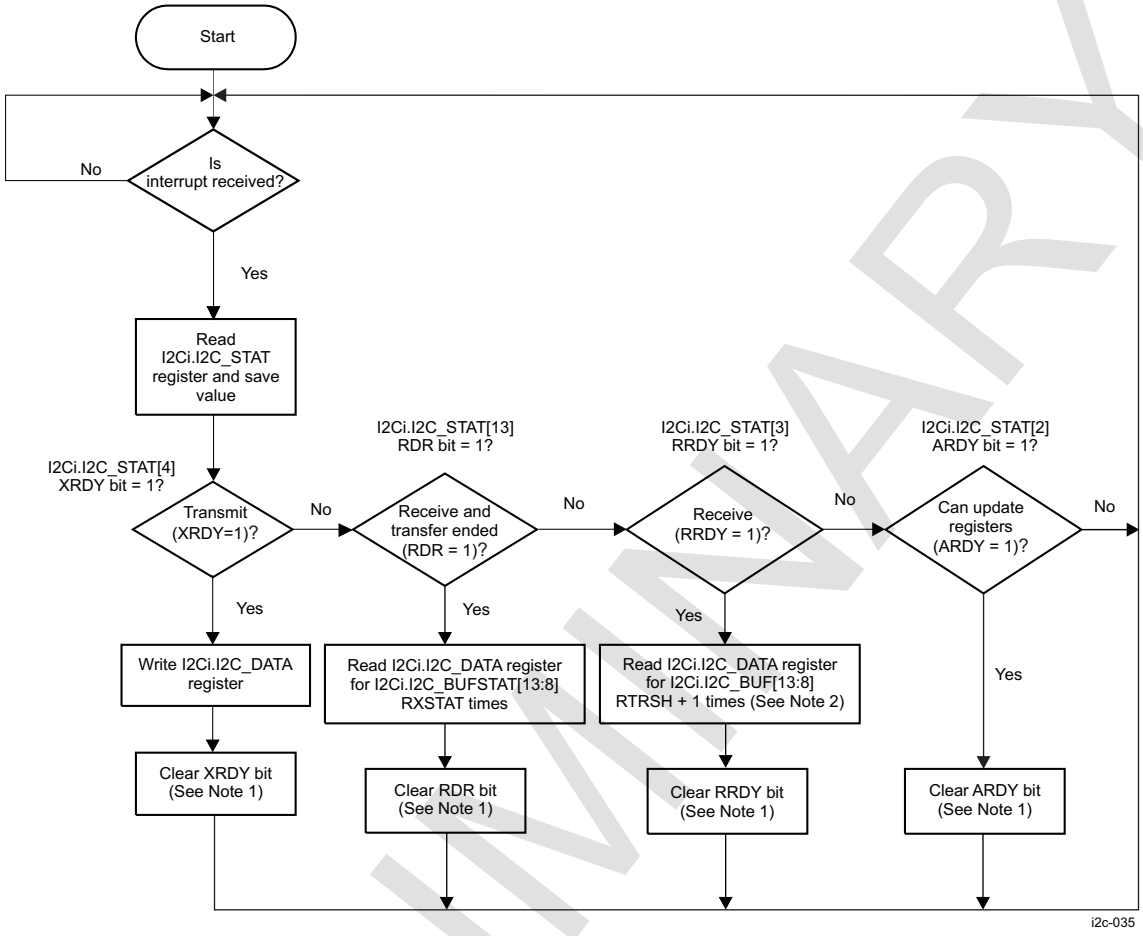
Figure 23-36. HS I²C Slave Transmitter/Receiver Mode, Interrupt



(1) The XRDY, RDR, RRDY, and ARDY bits are cleared by writing 1 to each corresponding bit in the I2Ci.I2C_STAT register.

(2) In slave transmitter mode, the amount of data requested by the external master I²C device is unknown; thus, the I2Ci.I2C_BUF[5:0] TXTRSH bit field must be configured to 0x0 (TX threshold = 1).

Table 23-24. HS I²C Register call summary for Sequence - Slave Transmitter/Receiver Mode, Interrupt

Register Name	Register Name
I2Ci.I2C_STAT (1)	I2Ci.I2C_BUFSTAT (1)
I2Ci.I2C_DATA (1)	I2Ci.I2C_BUF (1)

(1) i = 1 to 4

23.1.5.1.2 HS I²C (I2C5) Programming Model for Communication With Power Chips

This section describes the programming model of the master transmitter HS I²C controller (I2C5) for communication with one or more power chips. The HS I²C controller (I2C5) allowsthe two voltage Finite State Machines (FSMs) in the PRCM module of the device to be interfaced to external power chips through the I²C bus for dynamic voltage control of two power supplies and power sequencing. The primary programming tasks are to set up the configuration registers according to the external power supply chip(s) being used.

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23.1.5.1.2.1 Configure the Voltage Controller Registers

To use the voltage control function, the LH must configure the following registers in the voltage controller of the APE and 3G modem SS PRCM modules:

- The voltage configuration register address for each VDD channel in the PRCM.PRM_VC_VAL_SMPS_RA_VOL register
- The ON/ON-low-power-Retention/OFF command configuration register address for each VDD channel in the PRCM.PRM_VC_VAL_SMPS_RA_CMD register
- The set of ON/ON-low-power/Retention/OFF voltage/mode values in the APE PRCM.PRM_VC_VAL_CMD_VDD_CORE_L, APE PRCM.PRM_VC_VAL_CMD_VDD_IVA_L, and APE PRCM.PRM_VC_VAL_CMD_VDD_MPU_L registers, and 3G modem SS PRCM.PRM_VC_VAL_CMD_VDD_WGM_L register.
- The VDD channels configuration selection in the PRCM.PRM_VC_CFG_CHANNEL register

For more information about the voltage controller register configuration, see Chapter 3, *Power, Reset, and Clock Management*.

23.1.5.1.2.2 Configure the HS I²C Controller I2C5

At POR, the I2C5 is in HS mode (PRCM.PRM_VC_CFG_I2C_MODE[3] HSMODEEN bit). In HS mode, the LH must configure the master code value for the preamble I²C high-speed transmission by configuring the PRCM.PRM_VC_CFG_I2C_MODE[2:0] HSMCODE bit field. If the external power chips do not support the I²C HS mode, HS mode can be disabled and F/S mode enabled by clearing the PRCM.PRM_VC_CFG_I2C_MODE[3] HSMODEEN bit to 0.

By default, the Sr operation is enabled (PRCM.PRM_VC_CFG_I2C_MODE[4] SRMODEEN bit set to 1 at POR). In F/S mode, the Sr operation can be disabled by clearing the PRCM.PRM_VC_CFG_I2C_MODE[4] SRMODEEN bit to 0.

23.1.5.1.3 HS I²C Basic Programming Model in SCCB Mode

This section describes the programming model of the multimaster HS I²C controllers configured in SCCB mode.

23.1.5.1.3.1 Main Program

23.1.5.1.3.1.1 Configure the Module Before Enabling the I²C Controller

Before enabling the I²C controller, perform the following steps:

1. Enable the functional and interface clocks (see Table 23-7).
2. Program the prescaler to obtain an approximately 12-MHz internal sampling clock (I2Ci_INTERNAL_CLK) by programming the corresponding value in the I2Ci.I2C_PSC[7:0] PSC field. This value depends on the frequency of the functional clock (I2Ci_FCLK). Because this frequency is 96MHz, the I2Ci.I2C_PSC[7:0] PSC field value is 0x7.
3. Program the I2Ci.I2C_SCLL[7:0] SCLL and I2Ci.I2C_SCLH[7:0] SCLH fields to obtain a bit rate of 100K bps (maximum authorized bit rate in SCCB mode). This value depends on the internal sampling clock frequency (see Table 23-8).
4. Configure the 7-bit slave address (ID value) by storing it in the I2Ci.I2C_SA register.
5. Configure the 8-bit register address (subaddress) by storing it in the I2Ci.I2C_OA0 register.
6. Configure the I2Ci.I2C_BUF[13:8]RTRSH field to 0x0 (RX threshold to 1) and the I2Ci.I2C_BUF[5:0]XTRSH field to 0x0 (TX threshold to 1).
7. Take the I²C controller out of reset by setting the I2Ci.I2C_CON[15] I2C_EN bit to 1.

23.1.5.1.3.1.2 Initialize the I²C Controller

To initialize the I²C controller, perform the following steps:

1. Configure the I2Ci.I2C_CON register:

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- In SCCB mode, only the master mode is supported; set the I2Ci.I2C_CON[10] MST bit to 1.
- For transmitter mode (write to the external SCCB device register) or receiver mode (read from the external SCCB device register), set the I2Ci.I2C_CON[9] TRX bit (0: receiver, 1: transmitter).

2. If using an interrupt to transmit/receive data, set to 1 the corresponding bit in the I2Ci.I2C_IE register (the I2Ci.I2C_IE[4] XRDY_IE bit for the transmit interrupt, the I2Ci.I2C_IE[3] RRDY bit for the receive interrupt).

23.1.5.1.3.1.3 Initiate a Transfer

Poll the I2Ci.I2C_STAT[12] BB bit. If it is cleared to 0 (bus not busy), set the I2Ci.I2C_CON[0] STT bit to 1. Because a transfer allows the LH to write or read only a single byte to or from the external SCCB device, the transmission automatically stops at the end of the transfer. When the transfer is complete, the I2Ci.I2C_STAT[2] ARDY bit is set to 1. In SCCB mode, the I2Ci.I2C_CON[1] STP bit is not used.

23.1.5.1.3.1.4 Receive Data

Poll the I2Ci.I2C_STAT[3] RRDY bit, or use the RRDY interrupt (the I2Ci.I2C_IE[3] RRDY_IE bit must be set to 1) to read the receive data in the I2Ci.I2C_DATA register.

NOTE: In SCCB mode, the I2Ci.I2C_BUF[13:8] RTRSH field (RX threshold) must be set to a value of 0x0 (RX threshold = 1).

23.1.5.1.3.1.5 Transmit Data

Poll the I2Ci.I2C_STAT[4] XRDY bit, or use the XRDY interrupt (the I2Ci.I2C_IE[4] XRDY_IE bit must be set to 1) to write the data to the I2Ci.I2C_DATA register.

NOTE: In SCCB mode, the I2Ci.I2C_BUF[5:0] TXTRSH field (TX threshold) must be set to a value of 0x0 (TX threshold = 1).

23.1.5.1.3.2 Interrupt Subroutine Sequence

1. Test for register access ready (I2Ci.I2C_STAT[2] ARDY status bit) and resolve accordingly.
2. Test for receive data ready (I2Ci.I2C_STAT[3] RRDY status bit) and resolve accordingly.
3. Test for transmit data ready (I2Ci.I2C_STAT[4] XRDY status bit) and resolve accordingly.

23.1.5.1.3.3 Programming Flow Diagrams

Figure 23-37 through Figure 23-41 are procedure flowcharts for programming the SCCB mode.

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Figure 23-37. HS I²C SCCB Setup Procedure

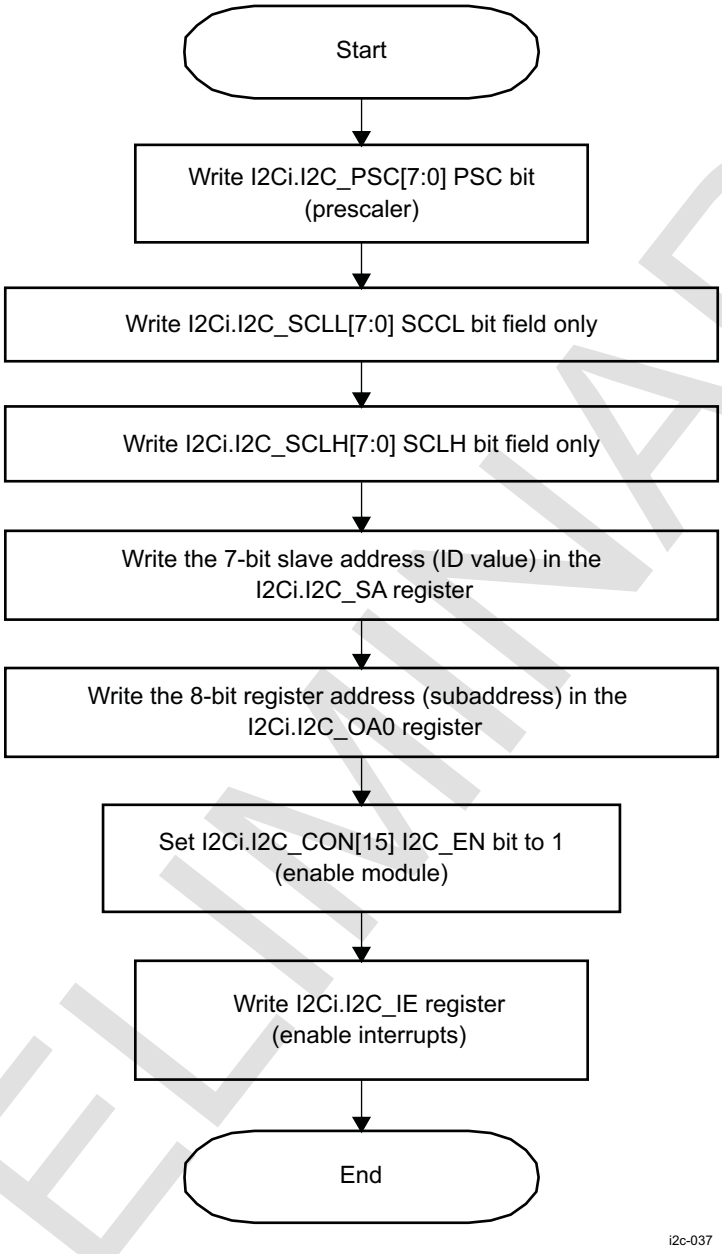

Table 23-25. HS I²C Register call summary for Sequence - SCCB Setup Procedure

Register Name	Register Name	Register Name
I2Ci.I2C_PSC (1)	I2Ci.I2C_SCLL (1)	I2Ci.I2C_SCLH (1)
I2Ci.I2C_SA (1)	I2Ci.I2C_OA0(1)	I2Ci.I2C_CON (1)
I2Ci.I2C_IE (1)		

(1) i = 1 to 4

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Figure 23-38. HS I²C SCCB Master Transmitter Mode, Polling

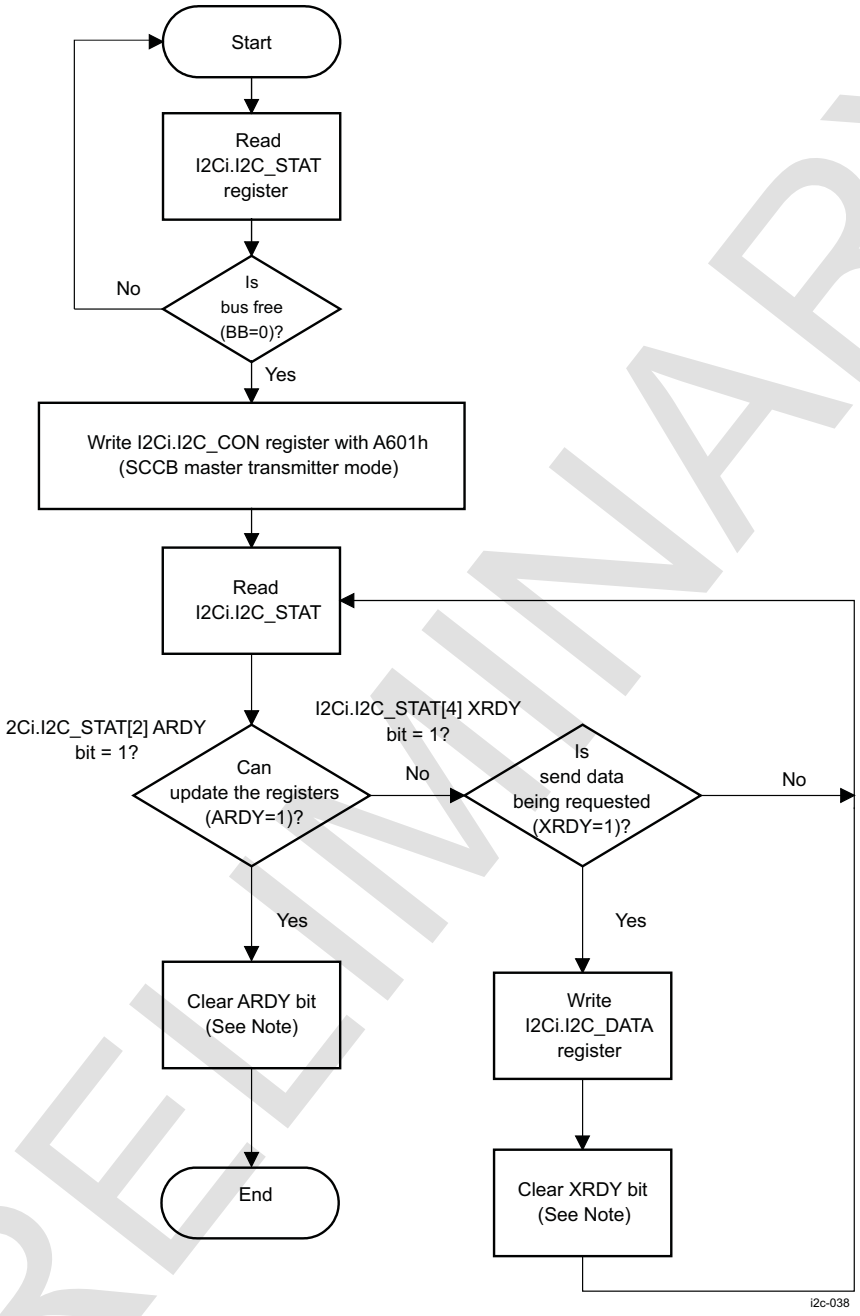

Table 23-26. HS I²C Register call summary for Sequence - SCCB Master Transmitter Mode, Polling

Register Name	Register Name
I2Ci.I2C_STAT (1)	I2Ci.I2C_SCLL (1)
I2Ci.I2C_CON (1)	I2Ci.I2C_DATA (1)

(1) i = 1 to 4

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NOTE: The XRDY and ARDY bits are cleared by writing 1 to the corresponding bit in the I2Ci.I2C_STAT register.

Figure 23-39. HS I²C SCCB Master Receiver Mode, Polling

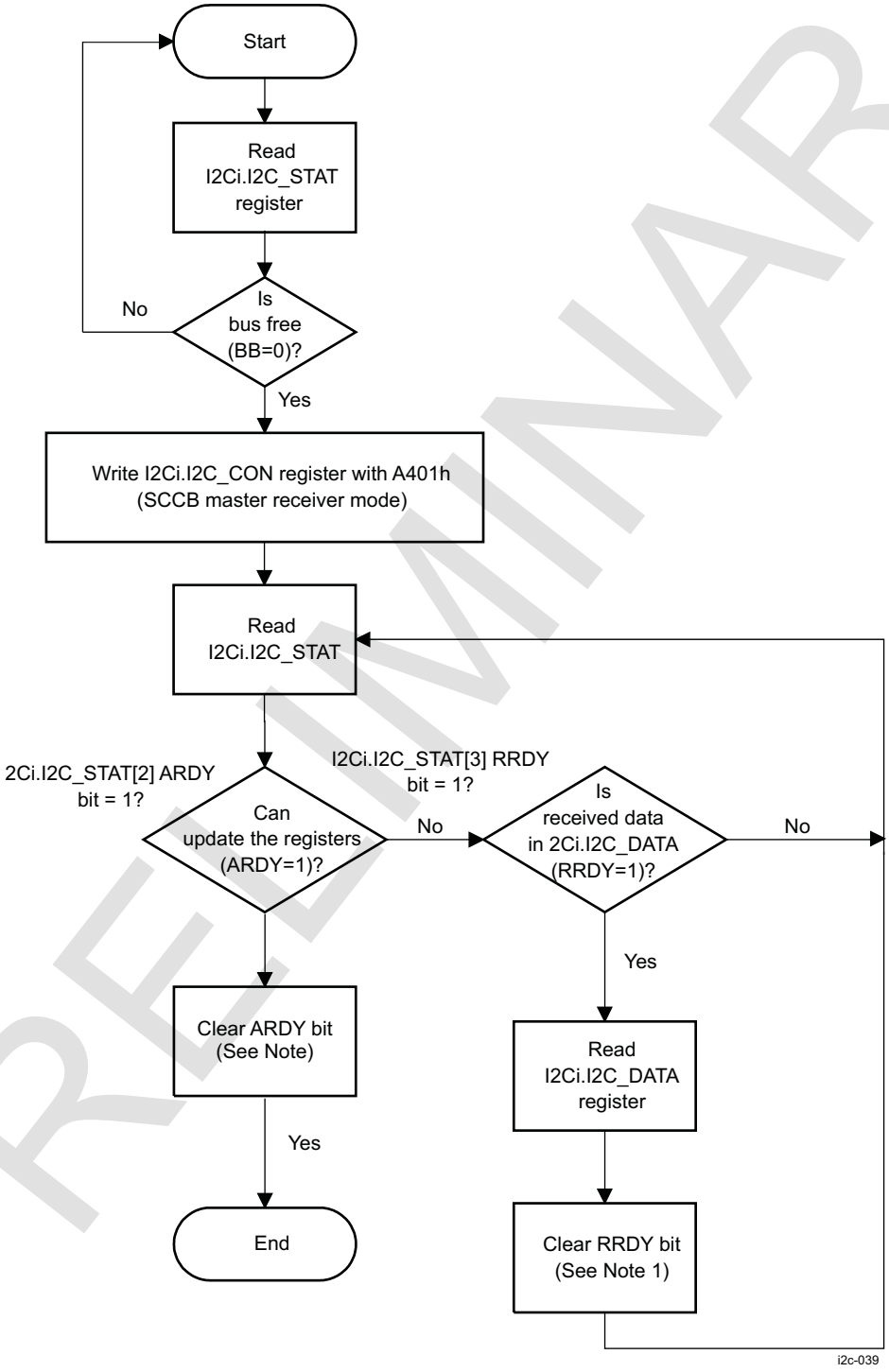

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Table 23-27. HS I²C Register call summary for Sequence - SCCB Master Receiver Mode, Polling

Register Name	Register Name
I2Ci.I2C_STAT (1)	I2Ci.I2C_SCLL (1)
I2Ci.I2C_CON (1)	I2Ci.I2C_DATA (1)

(1) i = 1 to 4

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NOTE: The RRDY and ARDY bits are cleared by writing 1 in the corresponding bit in the I2Ci.I2C_STAT register.

Figure 23-40. HS I²C SCCB Master Transmitter Mode, Interrupt

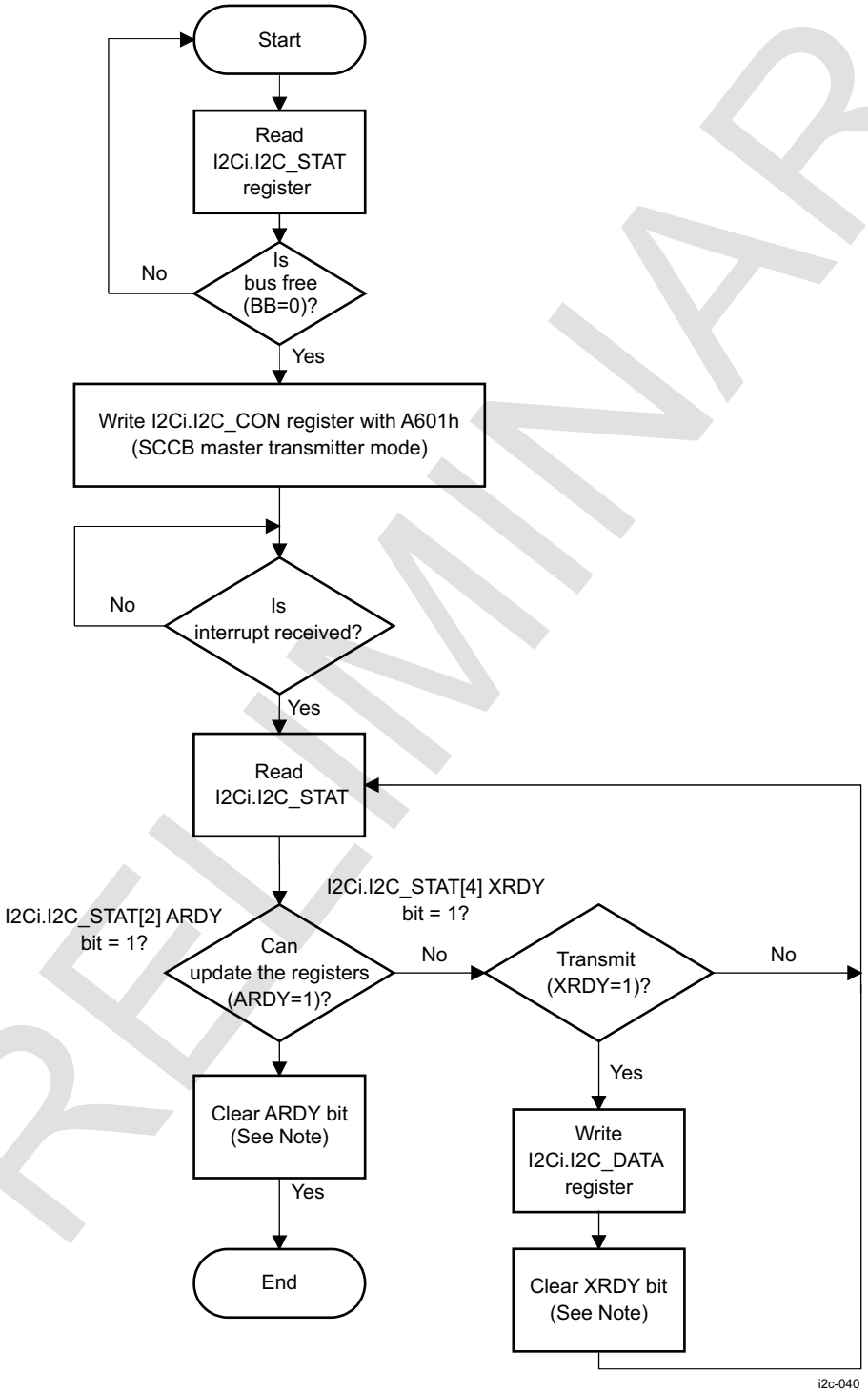

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Table 23-28. HS I²C Register call summary for Sequence - SCCB Master Transmitter Mode, Interrupt

Register Name	Register Name	Register Name
I2Ci.I2C_STAT (1)	I2Ci.I2C_DATA (1)	I2Ci.I2C_CON (1)

(1) i = 1 to 4

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NOTE: The XRDY and ARDY bits are cleared by writing 1 in the corresponding bit in the I2Ci.I2C_STAT register.

Figure 23-41. HS I²C SCCB Master Receiver Mode, Interrupt

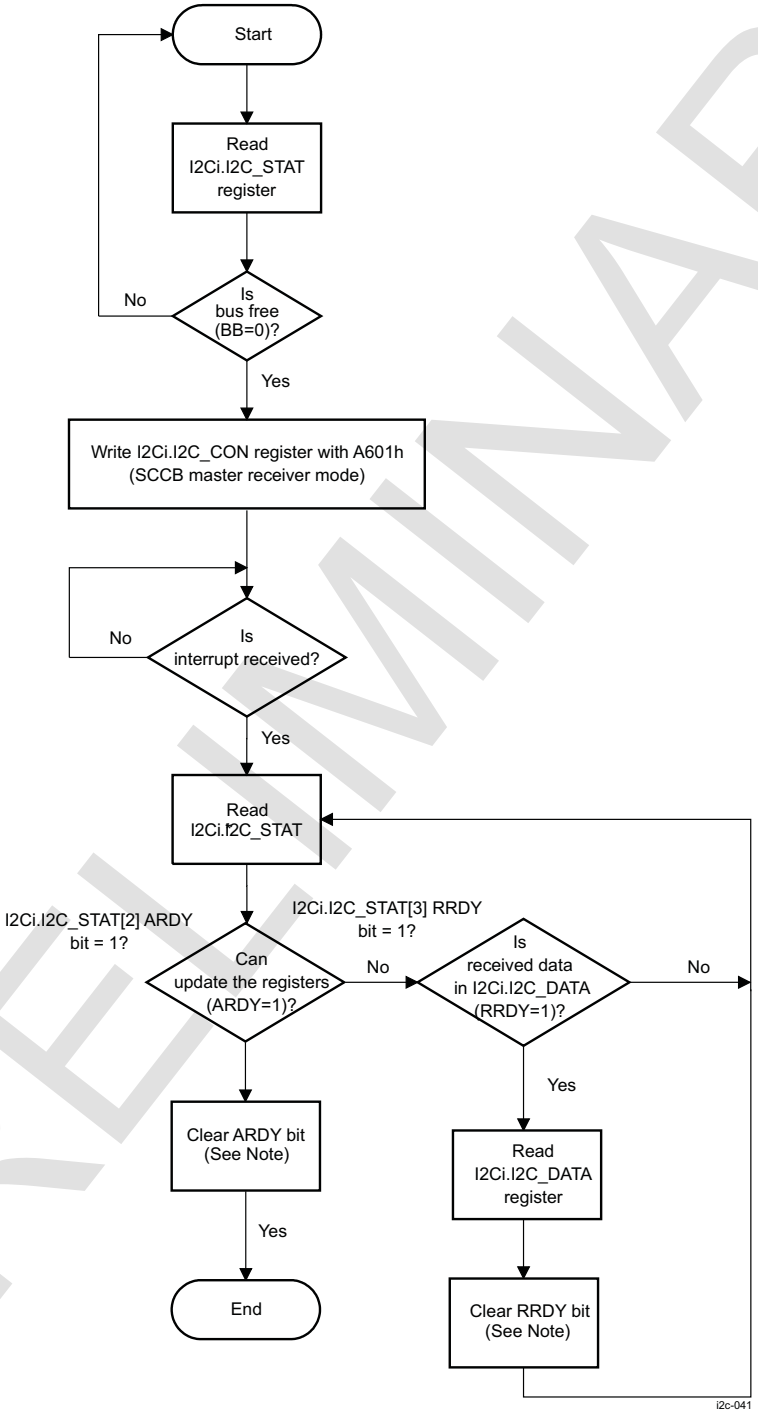

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Table 23-29. HS I²C Register call summary for Sequence - SCCB Master Receiver Mode, Interrupt

Register Name	Register Name	Register Name
I2Ci.I2C_STAT (1)	I2Ci.I2C_DATA (1)	I2Ci.I2C_CON (1)

(1) i = 1 to 4

NOTE: The RRDY and ARDY bits are cleared by writing 1 in the corresponding bit in the I2Ci.I2C_STAT register.

23.1.6 HS I²C Register Manual

23.1.6.1 HS I²C Instance Summary

Table 23-30. HS I²C Instance Summary

Module Name	Module Base Address	Size
I2C3	0x4806 0000	256 bytes
I2C1	0x4807 0000	256 bytes
I2C2	0x4807 2000	256 bytes
I2C4	0x4835 0000	256 bytes

23.1.6.2 HS I²C Registers

CAUTION

The HS I2C*i* registers are limited to 16 bit and 8 bit data accesses; 32–bit data access is not allowed and can corrupt register content.

NOTE: For register details about the master transmitter HS I2C controller I2C5, see Chapter 3, *Power, Reset, and Clock Management*.

23.1.6.2.1 HS I²C Register Summary

Table 23-31. HS I²C Registers Mapping Summary 1

Register Name	Type	Register Width (Bits)	Address Offset	I2C3 Physical Address	I2C1 Physical Address
I2C_REVNB_LO	R	16	0x0000 0000	0x4806 0000	0x4807 0000
I2C_REVNB_HI	R	16	0x0000 0004	0x4806 0004	0x4807 0004
I2C_SYSC	RW	16	0x0000 0010	0x4806 0010	0x4807 0010
RESERVED	W	16	0x0000 0020	0x4806 0020	0x4807 0020
I2C_IRQSTATUS_RAW	RW	16	0x0000 0024	0x4806 0024	0x4807 0024
I2C_IRQSTATUS	RW	16	0x0000 0028	0x4806 0028	0x4807 0028
I2C_IRQENABLE_SET	RW	16	0x0000 002C	0x4806 002C	0x4807 002C
I2C_IRQENABLE_CLR	RW	16	0x0000 0030	0x4806 0030	0x4807 0030
I2C_WE	RW	16	0x0000 0034	0x4806 0034	0x4807 0034
I2C_DMARXENABLE_SET	RW	16	0x0000 0038	0x4806 0038	0x4807 0038
I2C_DMATXENABLE_SET	RW	16	0x0000 003C	0x4806 003C	0x4807 003C
I2C_DMARXENABLE_CLR	RW	16	0x0000 0040	0x4806 0040	0x4807 0040
I2C_DMATXENABLE_CLR	RW	16	0x0000 0044	0x4806 0044	0x4807 0044

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Table 23-31. HS I²C Registers Mapping Summary 1 (continued)

Register Name	Type	Register Width (Bits)	Address Offset	I2C3 Physical Address	I2C1 Physical Address
I2C_DMARXWAKE_EN	RW	16	0x0000 0048	0x4806 0048	0x4807 0048
I2C_DMATXWAKE_EN	RW	16	0x0000 004C	0x4806 004C	0x4807 004C
I2C_IE	RW	16	0x0000 0084	0x4806 0084	0x4807 0084
I2C_STAT	RW	16	0x0000 0088	0x4806 0088	0x4807 0088
I2C_SYSS	RW	16	0x0000 0090	0x4806 0090	0x4807 0090
I2C_BUF	RW	16	0x0000 0094	0x4806 0094	0x4807 0094
I2C_CNT	RW	16	0x0000 0098	0x4806 0098	0x4807 0098
I2C_DATA	RW	16	0x0000 009C	0x4806 009C	0x4807 009C
I2C_CON	RW	16	0x0000 00A4	0x4806 00A4	0x4807 00A4
I2C_OA	RW	16	0x0000 00A8	0x4806 00A8	0x4807 00A8
I2C_SA	RW	16	0x0000 00AC	0x4806 00AC	0x4807 00AC
I2C_PSC	RW	16	0x0000 00B0	0x4806 00B0	0x4807 00B0
I2C_SCLL	RW	16	0x0000 00B4	0x4806 00B4	0x4807 00B4
I2C_SCLH	RW	16	0x0000 00B8	0x4806 00B8	0x4807 00B8
I2C_SYSTEST	RW	16	0x0000 00BC	0x4806 00BC	0x4807 00BC
I2C_BUFSTAT	R	16	0x0000 00C0	0x4806 00C0	0x4807 00C0
I2C_OA1	RW	16	0x0000 00C4	0x4806 00C4	0x4807 00C4
I2C_OA2	RW	16	0x0000 00C8	0x4806 00C8	0x4807 00C8
I2C_OA3	RW	16	0x0000 00CC	0x4806 00CC	0x4807 00CC
I2C_ACTOA	R	16	0x0000 00D0	0x4806 00D0	0x4807 00D0
I2C_SBLOCK	RW	16	0x0000 00D4	0x4806 00D4	0x4807 00D4

Table 23-32. HS I²C Registers Mapping Summary 2

Register Name	Type	Register Width (Bits)	Address Offset	I2C2 Physical Address	I2C4 Physical Address
I2C_REVNB_LO	R	16	0x0000 0000	0x4807 2000	0x4835 0000
I2C_REVNB_HI	R	16	0x0000 0004	0x4807 2004	0x4835 0004
I2C_SYSC	RW	16	0x0000 0010	0x4807 2010	0x4835 0010
RESERVED	W	16	0x0000 0020	0x4807 2020	0x4835 0020
I2C_IRQSTATUS_RAW	RW	16	0x0000 0024	0x4807 2024	0x4835 0024
I2C_IRQSTATUS	RW	16	0x0000 0028	0x4807 2028	0x4835 0028
I2C_IRQENABLE_SET	RW	16	0x0000 002C	0x4807 202C	0x4835 002C
I2C_IRQENABLE_CLR	RW	16	0x0000 0030	0x4807 2030	0x4835 0030
I2C_WE	RW	16	0x0000 0034	0x4807 2034	0x4835 0034
I2C_DMARXENABLE_SET	RW	16	0x0000 0038	0x4807 2038	0x4835 0038
I2C_DMATXENABLE_SET	RW	16	0x0000 003C	0x4807 203C	0x4835 003C
I2C_DMARXENABLE_CLR	RW	16	0x0000 0040	0x4807 2040	0x4835 0040
I2C_DMATXENABLE_CLR	RW	16	0x0000 0044	0x4807 2044	0x4835 0044
I2C_DMARXWAKE_EN	RW	16	0x0000 0048	0x4807 2048	0x4835 0048
I2C_DMATXWAKE_EN	RW	16	0x0000 004C	0x4807 204C	0x4835 004C
I2C_IE	RW	16	0x0000 0084	0x4807 2084	0x4835 0084
I2C_STAT	RW	16	0x0000 0088	0x4807 2088	0x4835 0088
I2C_SYSS	RW	16	0x0000 0090	0x4807 2090	0x4835 0090
I2C_BUF	RW	16	0x0000 0094	0x4807 2094	0x4835 0094
I2C_CNT	RW	16	0x0000 0098	0x4807 2098	0x4835 0098

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Table 23-32. HS I²C Registers Mapping Summary 2 (continued)

Register Name	Type	Register Width (Bits)	Address Offset	I2C2 Physical Address	I2C4 Physical Address
I2C_DATA	RW	16	0x0000 009C	0x4807 209C	0x4835 009C
I2C_CON	RW	16	0x0000 00A4	0x4807 20A4	0x4835 00A4
I2C_OA	RW	16	0x0000 00A8	0x4807 20A8	0x4835 00A8
I2C_SA	RW	16	0x0000 00AC	0x4807 20AC	0x4835 00AC
I2C_PSC	RW	16	0x0000 00B0	0x4807 20B0	0x4835 00B0
I2C_SCLL	RW	16	0x0000 00B4	0x4807 20B4	0x4835 00B4
I2C_SCLH	RW	16	0x0000 00B8	0x4807 20B8	0x4835 00B8
I2C_SYSTEST	RW	16	0x0000 00BC	0x4807 20BC	0x4835 00BC
I2C_BUFSTAT	R	16	0x0000 00C0	0x4807 20C0	0x4835 00C0
I2C_OA1	RW	16	0x0000 00C4	0x4807 20C4	0x4835 00C4
I2C_OA2	RW	16	0x0000 00C8	0x4807 20C8	0x4835 00C8
I2C_OA3	RW	16	0x0000 00CC	0x4807 20CC	0x4835 00CC
I2C_ACTOA	R	16	0x0000 00D0	0x4807 20D0	0x4835 00D0
I2C_SBLOCK	RW	16	0x0000 00D4	0x4807 20D4	0x4835 00D4

23.1.6.2.2 HS I²C Register Description

Table 23-33. I2C_REVNB_LO

Address Offset	0x0000 0000
Physical Address	0x4806 0000 0x4807 0000 0x4807 2000 0x4835 0000
Description	IP Revision Identifier (X.Y.R) Used by software to track features, bugs, and compatibility
Type	R

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP Revision	R	TI internal data

Table 23-34. Register Call Summary for Register I2C_REVNB_LO

Multimaster High-Speed I2C Controller

- HS I2C Register Summary: [0] [1]

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Table 23-35. I2C_REVNB_HI

Address Offset	0x0000 0004
Physical Address	0x4806 0004 0x4807 0004 0x4807 2004 0x4835 0004
Description	IP Revision Identifier (X.Y.R) Used by software to track features, bugs, and compatibility
Type	R

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP Revision	R	TI internal data

Table 23-36. Register Call Summary for Register I2C_REVNB_HI

Multimaster High-Speed I2C Controller

- HS I2C Register Summary: [0] [1]

Table 23-37. I2C_SYSC

Address Offset	0x0000 0010
Physical Address	0x4806 0010 0x4807 0010 0x4807 2010 0x4835 0010
Description	System Configuration register
Type	RW

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						CLKACTIVITY		RESERVED			IDLEMODE		ENAWAKEUP	SRST	AUTOIDLE

Bits	Field Name	Description	Type	Reset
15:10	RESERVED	Reserved.	R	0x00
9:8	CLKACTIVITY	Clock Activity selection bits 0x0: Both clocks can be cut off 0x1: Only OCP clock must be kept active; system clock can be cut off 0x3: Both clocks must be kept active 0x2: Only system clock must be kept active; OCP clock can be cut off	RW	0x0
7:5	RESERVED	Reads return 0.	R	0x0
4:3	IDLEMODE	Idle Mode selection bits 0x0: Force Idle mode 0x1: No Idle mode 0x3: smartidle_wakeup 0x2: Smart Idle mode	RW	0x0

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Bits	Field Name	Description	Type	Reset
2	ENAWAKEUP	Enable Wakeup control bit 0x0: Wakeup mechanism is disabled 0x1: Wakeup mechanism is enabled	RW	0
1	SRST	SoftReset bit 0x0: Normal mode 0x1: The module is reset	RW	0
0	AUTOIDLE	Autoidle bit 0x0: Auto Idle mechanism is disabled 0x1: Auto Idle mechanism is enabled	RW	1

Table 23-38. Register Call Summary for Register I2C_SYSC

Multimaster High-Speed I2C Controller

- HS I2C Software Reset: [0] [1]
- HS I2C Power Management: [2] [3] [4] [5] [6]
- HS I2C Register Summary: [7] [8]

Table 23-39. I2C_IRQSTATUS_RAW

Address Offset	0x0000 0024
Physical Address	0x4806 0024 0x4807 0024 0x4807 2024 0x4835 0024
Description	Per-event raw interrupt status vector
Type	RW

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	XDR	RDR	BB	ROVR	XUDF	AAS	BF	AERR	STC	GC	XRDY	RRDY	ARDY	NACK	AL

Bits	Field Name	Description	Type	Reset
15	RESERVED	Write 0s for future compatibility. Read returns 0.	RW	0
14	XDR	Transmit draining IRQ status. 0x0: Transmit draining inactive. 0x1: Transmit draining enabled.	RW	0
13	RDR	Receive draining IRQ status. 0x0: Receive draining inactive. 0x1: Receive draining enabled.	RW	0
12	BB	Bus busy status.Writing into this bit has no effect. Read 0x1: Bus is occupied. Read 0x0: Bus is free.	R	0
11	ROVR	Receive overrun status.Writing into this bit has no effect. Read 0x1: Receiver overrun. Read 0x0: Normal operation.	RW	0
10	XUDF	Transmit underflow status.Writing into this bit has no effect. Read 0x1: Transmit underflow. Read 0x0: Normal operation.	RW	0

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Bits	Field Name	Description	Type	Reset
9	AAS	Address recognized as slave IRQ status. 0x0: No action. 0x1: Address recognized.	RW	0
8	BF	Bus Free IRQ status. 0x0: No action. 0x1: Bus Free.	RW	0
7	AERR	Access Error IRQ status. 0x0: No action. 0x1: Access Error.	RW	0
6	STC	Start Condition IRQ status. 0x0: No action. 0x1: Start Condition detected.	RW	0
5	GC	General call IRQ status. Set to 1 by core when General call address detected and interrupt signaled to MPUSS. Write 1 to clear. 0x0: No general call detected. 0x1: General call address detected.	RW	0
4	XRDY	Transmit data ready IRQ status. Set to 1 by core when transmitter and when new data is requested. When set to 1 by core, an interrupt is signaled to MPUSS. Write 1 to clear. 0x0: Transmision ongoing. 0x1: Transmit data ready.	RW	0
3	RRDY	Receive data ready IRQ status. Set to 1 by core when receiver mode, a new data is able to be read. When set to 1 by core, an interrupt is signaled to MPUSS. Write 1 to clear. 0x0: No data available. 0x1: Receive data available.	RW	0
2	ARDY	Register access ready IRQ status. When set to 1 it indicates that previous access has been performed and registers are ready to be accessed again. An interrupt is signaled to MPUSS. Write 1 to clear. 0x0: Module busy. 0x1: Access ready.	RW	0
1	NACK	No acknowledgement IRQ status. Bit is set when No Acknowledge has been received, an interrupt is signaled to MPUSS. Write 1 to clear this bit. 0x0: Normal operation. 0x1: Not Acknowledge detected.	RW	0
0	AL	Arbitration lost IRQ status. This bit is automatically set by the hardware when it loses the Arbitration in master transmit mode, an interrupt is signaled to MPUSS. During reads, it always returns 0. 0x0: Normal operation. 0x1: Arbitration lost detected.	RW	0

Table 23-40. Register Call Summary for Register I2C_IRQSTATUS_RAW

Multimaster High-Speed I2C Controller

- HS I2C Register Summary: [0] [1]

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Table 23-41. I2C_IRQSTATUS

Address Offset	0x0000 0028
Physical Address	0x4806 0028 0x4807 0028 0x4807 2028 0x4835 0028
Description	Per-event enabled interrupt status vector
Type	RW

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	XDR	RDR	BB	ROVR	XUDF	AAS	BF	AERR	STC	GC	XRDY	RRDY	ARDY	NACK	AL

Bits	Field Name	Description	Type	Reset
15	RESERVED	Write 0s for future compatibility. Read returns 0.	RW	0
14	XDR	Transmit draining IRQ enabled status. 0x0: Transmit draining inactive. 0x1: Transmit draining enabled.	RW W1toClr	0
13	RDR	Receive draining IRQ enabled status. 0x0: Receive draining inactive. 0x1: Receive draining enabled.	RW W1toClr	0
12	BB	Bus busy enabled status.Writing into this bit has no effect. Read 0x1: Bus is occupied. Read 0x0: Bus is free.	R	0
11	ROVR	Receive overrun enabled status.Writing into this bit has no effect. Read 0x1: Receiver overrun. Read 0x0: Normal operation.	RW W1toClr	0
10	XUDF	Transmit underflow enabled status.Writing into this bit has no effect. Read 0x1: Transmit underflow. Read 0x0: Normal operation.	RW W1toClr	0
9	AAS	Address recognized as slave IRQ enabled status. 0x0: No action. 0x1: Address recognized.	RW W1toClr	0
8	BF	Bus Free IRQ enabled status. 0x0: No action. 0x1: Bus Free.	RW W1toClr	0
7	AERR	Access Error IRQ enabled status. 0x0: No action. 0x1: Access Error.	RW W1toClr	0
6	STC	Start Condition IRQ enabled status. 0x0: No action. 0x1: Start Condition detected.	RW W1toClr	0
5	GC	General call IRQ enabled status. Set to 1 by core when General call address detected and interrupt signaled to MPUSS. Write 1 to clear. 0x0: No general call detected. 0x1: General call address detected.	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
4	XRDY	Transmit data ready IRQ enabled status. Set to 1 by core when transmitter and when new data is requested. When set to 1 by core, an interrupt is signaled to MPUSS. Write 1 to clear. 0x0: Transmision ongoing. 0x1: Transmit data ready.	RW W1toClr	0
3	RRDY	Receive data ready IRQ enabled status. Set to 1 by core when receiver mode, a new data is able to be read. When set to 1 by core, an interrupt is signaled to MPUSS. Write 1 to clear. 0x0: No data available. 0x1: Receive data available.	RW W1toClr	0
2	ARDY	Register access ready IRQ enabled status. When set to 1 it indicates that previous access has been performed and registers are ready to be accessed again. An interrupt is signaled to MPUSS. Write 1 to clear. 0x0: Module busy. 0x1: Access ready.	RW W1toClr	0
1	NACK	No acknowledgement IRQ enabled status. Bit is set when No Acknowledge has been received, an interrupt is signaled to MPUSS. Write 1 to clear this bit. 0x0: Normal operation. 0x1: Not Acknowledge detected.	RW W1toClr	0
0	AL	Arbitration lost IRQ enabled status. This bit is automatically set by the hardware when it loses the Arbitration in master transmit mode, an interrupt is signaled to MPUSS. During reads, it always returns 0. 0x0: Normal operation. 0x1: Arbitration lost detected.	RW W1toClr	0

Table 23-42. Register Call Summary for Register I2C_IRQSTATUS

Multimaster High-Speed I2C Controller

- HS I2C Interrupt Requests: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14]
- HS I2C Register Summary: [15] [16]

Table 23-43. I2C_IRQENABLE_SET

Address Offset	0x0000 002C
Physical Address	0x4806 002C 0x4807 002C 0x4807 202C 0x4835 002C
Description	Per-event interrupt enable bit vector.
Type	RW

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	XDR_IE	RDR_IE	RESERVED	ROVR	XUDF	ASS_IE	BF_IE	AERR_IE	STC_IE	GC_IE	XRDY_IE	RRDY_IE	ARDY_IE	NACK_IE	AL_IE

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Bits	Field Name	Description	Type	Reset
15	RESERVED	Write 0s for future compatibility. Read returns 0.	RW	0
14	XDR_IE	Transmit Draining interrupt enable set. Mask or unmask the interrupt signaled by bit in I2C_STAT[XDR]. 0x0: Transmit Draining interrupt disabled 0x1: Transmit Draining interrupt enabled	RW	0
13	RDR_IE	Receive Draining interrupt enable set. Mask or unmask the interrupt signaled by bit in I2C_STAT[RDR]. 0x0: Receive Draining interrupt disabled 0x1: Receive Draining interrupt enabled	RW	0
12	RESERVED	reserved	R	0
11	ROVR	Receive overrun enable set. 0x0: Receive overrun interrupt disabled 0x1: Receive Draining interrupt enabled	RW	0
10	XUDF	Transmit underflow enable set. 0x0: Transmit underflow interrupt disabled 0x1: Transmit underflow interrupt enabled	RW	0
9	ASS_IE	Addressed as Slave interrupt enable set. Mask or unmask the interrupt signaled by bit in I2C_STAT[AAS]. 0x0: Addressed as Slave interrupt disabled 0x1: Addressed as Slave interrupt enabled	RW	0
8	BF_IE	Bus Free interrupt enable set. Mask or unmask the interrupt signaled by bit in I2C_STAT[BF]. 0x0: Bus Free interrupt disabled 0x1: Bus Free interrupt enabled	RW	0
7	AERR_IE	Access Error interrupt enable set. Mask or unmask the interrupt signaled by bit in I2C_STAT[AERR]. 0x0: Access Error interrupt disabled 0x1: Access Error interrupt enabled	RW	0
6	STC_IE	Start Condition interrupt enable set. Mask or unmask the interrupt signaled by bit in I2C_STAT[STC]. 0x0: Start Condition interrupt disabled 0x1: Start Condition interrupt enabled	RW	0
5	GC_IE	General call Interrupt enable set. Mask or unmask the interrupt signaled by bit in I2C_STAT[GC] 0x0: General call interrupt disabled 0x1: General call interrupt enabled	RW	0
4	XRDY_IE	Transmit data ready interrupt enable set. Mask or unmask the interrupt signaled by bit in I2C_STAT[XRDY] 0x0: Transmit data ready interrupt disabled 0x1: Transmit data ready interrupt enabled	RW	0
3	RRDY_IE	Receive data ready interrupt enable set. Mask or unmask the interrupt signaled by bit in I2C_STAT[RRDY] 0x0: Receive data ready interrupt disabled 0x1: Receive data ready interrupt enabled	RW	0
2	ARDY_IE	Register access ready interrupt enable set. Mask or unmask the interrupt signaled by bit in I2C_STAT[ARDY] 0x0: Register access ready interrupt disabled 0x1: Register access ready interrupt enabled	RW	0
1	NACK_IE	No acknowledgement interrupt enable set. Mask or unmask the interrupt signaled by bit in I2C_STAT[NACK] 0x0: Not Acknowledge interrupt disabled 0x1: Not Acknowledge interrupt enabled	RW	0

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Bits	Field Name	Description	Type	Reset
0	AL_IE	Arbitration lost interrupt enable set. Mask or unmask the interrupt signaled by bit in I2C_STAT[AL] 0x0: Arbitration lost interrupt disabled 0x1: Arbitration lost interrupt enabled	RW	0

Table 23-44. Register Call Summary for Register I2C_IRQENABLE_SET

Multimaster High-Speed I2C Controller

- HS I2C Interrupt Requests: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14]
- HS I2C Register Summary: [15] [16]

Table 23-45. I2C_IRQENABLE_CLR

Address Offset	0x0000 0030
Physical Address	0x4806 0030 0x4807 0030 0x4807 2030 0x4835 0030
Description	Per-event interrupt clear bit vector.
Type	RW

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	XDR_IE	RDR_IE	RESERVED	ROVR	XUDF	ASS_IE	BF_IE	AERR_IE	STC_IE	GC_IE	XRDY_IE	RRDY_IE	ARDY_IE	NACK_IE	AL_IE

Bits	Field Name	Description	Type	Reset
15	RESERVED	Write 0s for future compatibility. Read returns 0.	RW	0
14	XDR_IE	Transmit Draining interrupt enable clear. Mask or unmask the interrupt signaled by bit in I2C_STAT[XDR]. 0x0: Transmit Draining interrupt disabled 0x1: Transmit Draining interrupt enabled	RW	0
13	RDR_IE	Receive Draining interrupt enable clear. Mask or unmask the interrupt signaled by bit in I2C_STAT[RDR]. 0x0: Receive Draining interrupt disabled 0x1: Receive Draining interrupt enabled	RW	0
12	RESERVED	reserved	R	0
11	ROVR	Receive overrun enable clear. 0x0: Receive overrun interrupt disabled 0x1: Receive Draining interrupt enabled	RW	0
10	XUDF	Transmit underflow enable clear. 0x0: Transmit underflow interrupt disabled 0x1: Transmit underflow interrupt enabled	RW	0
9	ASS_IE	Addressed as Slave interrupt enable clear. Mask or unmask the interrupt signaled by bit in I2C_STAT[AAS]. 0x0: Addressed as Slave interrupt disabled 0x1: Addressed as Slave interrupt enabled	RW	0
8	BF_IE	Bus Free interrupt enable clear. Mask or unmask the interrupt signaled by bit in I2C_STAT[BF]. 0x0: Bus Free interrupt disabled 0x1: Bus Free interrupt enabled	RW	0

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Bits	Field Name	Description	Type	Reset
7	AERR_IE	Access Error interrupt enable clear. Mask or unmask the interrupt signaled by bit in I2C_STAT[AERR]. 0x0: Access Error interrupt disabled 0x1: Access Error interrupt enabled	RW	0
6	STC_IE	Start Condition interrupt enable clear. Mask or unmask the interrupt signaled by bit in I2C_STAT[STC]. 0x0: Start Condition interrupt disabled 0x1: Start Condition interrupt enabled	RW	0
5	GC_IE	General call Interrupt enable clear. Mask or unmask the interrupt signaled by bit in I2C_STAT[GC] 0x0: General call interrupt disabled 0x1: General call interrupt enabled	RW	0
4	XRDY_IE	Transmit data ready interrupt enable clear. Mask or unmask the interrupt signaled by bit in I2C_STAT[XRDY] 0x0: Transmit data ready interrupt disabled 0x1: Transmit data ready interrupt enabled	RW	0
3	RRDY_IE	Receive data ready interrupt enable clear. Mask or unmask the interrupt signaled by bit in I2C_STAT[RRDY] 0x0: Receive data ready interrupt disabled 0x1: Receive data ready interrupt enabled	RW	0
2	ARDY_IE	Register access ready interrupt enable clear. Mask or unmask the interrupt signaled by bit in I2C_STAT[ARDY] 0x0: Register access ready interrupt disabled 0x1: Register access ready interrupt enabled	RW	0
1	NACK_IE	No acknowledgement interrupt enable clear. Mask or unmask the interrupt signaled by bit in I2C_STAT[NACK] 0x0: Not Acknowledge interrupt disabled 0x1: Not Acknowledge interrupt enabled	RW	0
0	AL_IE	Arbitration lost interrupt enable clear. Mask or unmask the interrupt signaled by bit in I2C_STAT[AL] 0x0: Arbitration lost interrupt disabled 0x1: Arbitration lost interrupt enabled	RW	0

Table 23-46. Register Call Summary for Register I2C_IRQENABLE_CLR

Multimaster High-Speed I2C Controller

- HS I2C Interrupt Requests: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14]
- HS I2C Register Summary: [15] [16]

Table 23-47. I2C_WE

Address Offset	0x0000 0034
Physical Address	0x4806 0034 0x4807 0034 0x4807 2034 0x4835 0034
Description	I2C wakeup enable vector.
Type	RW

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	XDR	RDR	RESERVED	ROVR	XUDF	AAS	BF	RESERVED	STC	GC	RESERVED	DRDY	ARDY	NACK	AL

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Bits	Field Name	Description	Type	Reset
15	RESERVED	Reserved.	R	0
14	XDR	Transmit Draining wakeup set. 0x0: Transmit draining wakeup disabled 0x1: Transmit draining wakeup enabled	RW	0
13	RDR	Receive Draining wakeup set. 0x0: Receive draining wakeup disabled 0x1: Receive draining wakeup enabled	RW	0
12	RESERVED	Reserved.	R	0
11	ROVR	Receive overrun wakeup set. 0x0: Receive overrun wakeup disabled 0x1: Receive overrun wakeup enabled	RW	0
10	XUDF	Transmit underflow wakeup set. 0x0: Transmit underflow wakeup disabled 0x1: Transmit underflow wakeup enabled	RW	0
9	AAS	Address as slave IRQ wakeup set. 0x0: Addressed as slave wakeup disabled 0x1: Addressed as slave wakeup enabled	RW	0
8	BF	Bus Free IRQ wakeup set. 0x0: Bus Free wakeup disabled 0x1: Bus Free wakeup enabled	RW	0
7	RESERVED	Reserved.	R	0
6	STC	Start Condition IRQ wakeup set. 0x0: Start condition wakeup disabled 0x1: Start condition wakeup enabled	RW	0
5	GC	General call IRQ wakeup set. 0x0: General call wakeup disabled 0x1: General call wakeup enabled	RW	0
4	RESERVED	Reserved	R	0
3	DRDY	Receive/Transmit data ready IRQ wakeup set. 0x0: Transmit/receive data ready wakeup disabled 0x1: Transmit/receive data ready wakeup enabled	RW	0
2	ARDY	Register access ready IRQ wakeup set. 0x0: Register access ready wakeup disabled 0x1: Register access ready wakeup enabled	RW	0
1	NACK	No acknowledgment IRQ wakeup set. 0x0: Not Acknowledge wakeup disabled 0x1: Not Acknowledge wakeup enabled	RW	0
0	AL	Arbitration lost IRQ wakeup set. 0x0: Arbitration lost wakeup disabled 0x1: Arbitration lost wakeup enabled	RW	0

Table 23-48. Register Call Summary for Register I2C_WE

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- HS I2C Register Summary: [0] [1]

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Table 23-49. I2C_DMARXENABLE_SET

Address Offset	0x0000 0038
Physical Address	0x4806 0038 0x4807 0038 0x4807 2038 0x4835 0038
Description	Per-event DMA RX enable set.
Type	RW

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															DMARX_ENABLE_SET

Bits	Field Name	Description	Type	Reset
15:1	RESERVED	Reserved.	R	0x0000
0	DMARX_ENABLE_SET	Receive DMA channel enable set.	RW	0

Table 23-50. Register Call Summary for Register I2C_DMARXENABLE_SET

Multimaster High-Speed I2C Controller

- HS I2C Register Summary: [0] [1]

Table 23-51. I2C_DMATXENABLE_SET

Address Offset	0x0000 003C
Physical Address	0x4806 003C 0x4807 003C 0x4807 203C 0x4835 003C
Description	Per-event DMA TX enable set.
Type	RW

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															DMATX_ENABLE_SET

Bits	Field Name	Description	Type	Reset
15:1	RESERVED	Reserved.	R	0x0000
0	DMATX_ENABLE_SET	Transmit DMA channel enable set.	RW	0

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Table 23-52. Register Call Summary for Register I2C_DMATXENABLE_SET

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- HS I2C Register Summary: [0] [1]

Table 23-53. I2C_DMARXENABLE_CLR

Address Offset	0x0000 0040
Physical Address	0x4806 0040 0x4807 0040 0x4807 2040 0x4835 0040
Description	Per-event DMA RX enable clear.
Type	RW

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															DMARX_ENABLE_CLEAR

Bits	Field Name	Description	Type	Reset
15:1	RESERVED	Reserved.	R	0x0000
0	DMARX_ENABLE_CLEAR	Receive DMA channel enable clear.	RW	0

Table 23-54. Register Call Summary for Register I2C_DMARXENABLE_CLR

Multimaster High-Speed I2C Controller

- HS I2C Register Summary: [0] [1]

Table 23-55. I2C_DMATXENABLE_CLR

Address Offset	0x0000 0044
Physical Address	0x4806 0044 0x4807 0044 0x4807 2044 0x4835 0044
Description	Per-event DMA TX enable clear.
Type	RW

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															DMATX_ENABLE_CLEAR

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Bits	Field Name	Description	Type	Reset
15:1	RESERVED	Reserved.	R	0x0000
0	DMATX_ENABLE_CLEAR	Transmit DMA channel enable clear.	RW	0

Table 23-56. Register Call Summary for Register I2C_DMATXENABLE_CLR

Multimaster High-Speed I2C Controller

- HS I2C Register Summary: [0] [1]

Table 23-57. I2C_DMARXWAKE_EN

Address Offset	0x0000 0048
Physical Address	0x4806 0048 0x4807 0048 0x4807 2048 0x4835 0048
Description	Per-event DMA RX wakeup enable.
Type	RW

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	XDR	RDR	RESERVED	ROVR	XUDF	AAS	BF	RESERVED	STC	GC	RESERVED	DRDY	ARDY	NACK	AL

Bits	Field Name	Description	Type	Reset
15	RESERVED	Reserved.	R	0
14	XDR	Transmit Draining wakeup set. 0x0: Transmit draining wakeup disabled 0x1: Transmit draining wakeup enabled	RW	0
13	RDR	Receive Draining wakeup set. 0x0: Receive draining wakeup disabled 0x1: Receive draining wakeup enabled	RW	0
12	RESERVED	Reserved.	R	0
11	ROVR	Receive overrun wakeup set. 0x0: Receive overrun wakeup disabled 0x1: Receive overrun wakeup enabled	RW	0
10	XUDF	Transmit underflow wakeup set. 0x0: Transmit underflow wakeup disabled 0x1: Transmit underflow wakeup enabled	RW	0
9	AAS	Address as slave IRQ wakeup set. 0x0: Addressed as slave wakeup disabled 0x1: Addressed as slave wakeup enabled	RW	0
8	BF	Bus Free IRQ wakeup set. 0x0: Bus Free wakeup disabled 0x1: Bus Free wakeup enabled	RW	0
7	RESERVED	Reserved.	R	0
6	STC	Start Condition IRQ wakeup set. 0x0: Start condition wakeup disabled 0x1: Start condition wakeup enabled	RW	0

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Bits	Field Name	Description	Type	Reset
5	GC	General call IRQ wakeup set. 0x0: General call wakeup disabled 0x1: General call wakeup enabled	RW	0
4	RESERVED	Reserved	R	0
3	DRDY	Receive/Transmit data ready IRQ wakeup set. 0x0: Transmit/receive data ready wakeup disabled 0x1: Transmit/receive data ready wakeup enabled	RW	0
2	ARDY	Register access ready IRQ wakeup set. 0x0: Register access ready wakeup disabled 0x1: Register access ready wakeup enabled	RW	0
1	NACK	No acknowledgment IRQ wakeup set. 0x0: Not Acknowledge wakeup disabled 0x1: Not Acknowledge wakeup enabled	RW	0
0	AL	Arbitration lost IRQ wakeup set. 0x0: Arbitration lost wakeup disabled 0x1: Arbitration lost wakeup enabled	RW	0

Table 23-58. Register Call Summary for Register I2C_DMARXWAKE_EN

Multimaster High-Speed I2C Controller

- HS I2C Register Summary: [0] [1]

Table 23-59. I2C_DMATXWAKE_EN

Address Offset	0x0000 004C
Physical Address	0x4806 004C 0x4807 004C 0x4807 204C 0x4835 004C
Description	Per-event DMA TX wakeup enable.
Type	RW

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	XDR	RDR	RESERVED	ROVR	XUDF	AAS	BF	RESERVED	STC	GC	RESERVED	DRDY	ARDY	NACK	AL

Bits	Field Name	Description	Type	Reset
15	RESERVED	Reserved.	R	0
14	XDR	Transmit Draining wakeup set. 0x0: Transmit draining wakeup disabled 0x1: Transmit draining wakeup enabled	RW	0
13	RDR	Receive Draining wakeup set. 0x0: Receive draining wakeup disabled 0x1: Receive draining wakeup enabled	RW	0
12	RESERVED	Reserved.	R	0
11	ROVR	Receive overrun wakeup set. 0x0: Receive overrun wakeup disabled 0x1: Receive overrun wakeup enabled	RW	0

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Bits	Field Name	Description	Type	Reset
10	XUDF	Transmit underflow wakeup set. 0x0: Transmit underflow wakeup disabled 0x1: Transmit underflow wakeup enabled	RW	0
9	AAS	Address as slave IRQ wakeup set. 0x0: Addressed as slave wakeup disabled 0x1: Addressed as slave wakeup enabled	RW	0
8	BF	Bus Free IRQ wakeup set. 0x0: Bus Free wakeup disabled 0x1: Bus Free wakeup enabled	RW	0
7	RESERVED	Reserved.	R	0
6	STC	Start Condition IRQ wakeup set. 0x0: Start condition wakeup disabled 0x1: Start condition wakeup enabled	RW	0
5	GC	General call IRQ wakeup set. 0x0: General call wakeup disabled 0x1: General call wakeup enabled	RW	0
4	RESERVED	Reserved	R	0
3	DRDY	Receive/Transmit data ready IRQ wakeup set. 0x0: Transmit/receive data ready wakeup disabled 0x1: Transmit/receive data ready wakeup enabled	RW	0
2	ARDY	Register access ready IRQ wakeup set. 0x0: Register access ready wakeup disabled 0x1: Register access ready wakeup enabled	RW	0
1	NACK	No acknowledgment IRQ wakeup set. 0x0: Not Acknowledge wakeup disabled 0x1: Not Acknowledge wakeup enabled	RW	0
0	AL	Arbitration lost IRQ wakeup set. 0x0: Arbitration lost wakeup disabled 0x1: Arbitration lost wakeup enabled	RW	0

Table 23-60. Register Call Summary for Register I2C_DMATXWAKE_EN

Multimaster High-Speed I2C Controller

- HS I2C Register Summary: [0] [1]

Table 23-61. I2C_IE

Address Offset	0x0000 0084
Physical Address	0x4806 0084 0x4807 0084 0x4807 2084 0x4835 0084
Description	I2C interrupt enable vector (legacy).
Type	RW

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	XDR_IE	RDR_IE	RESERVED	ROVR	XUDF	ASS_IE	BF_IE	AERR_IE	STC_IE	GC_IE	XRDY_IE	RRDY_IE	ARDY_IE	NACK_IE	AL_IE

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Bits	Field Name	Description	Type	Reset
15	RESERVED	Write 0s for future compatibility. Read returns 0.	RW	0
14	XDR_IE	Transmit Draining interrupt enable. Mask or unmask the interrupt signaled by bit in I2C_STAT[XDR]. 0x0: Transmit Draining interrupt disabled 0x1: Transmit Draining interrupt enabled	RW	0
13	RDR_IE	Receive Draining interrupt enable. Mask or unmask the interrupt signaled by bit in I2C_STAT[RDR]. 0x0: Receive Draining interrupt disabled 0x1: Receive Draining interrupt enabled	RW	0
12	RESERVED	reserved	R	0
11	ROVR	Receive overrun enable set. 0x0: Receive overrun interrupt disabled 0x1: Receive Draining interrupt enabled	RW	0
10	XUDF	Transmit underflow enable set. 0x0: Transmit underflow interrupt disabled 0x1: Transmit underflow interrupt enabled	RW	0
9	ASS_IE	Addressed as Slave interrupt enable. Mask or unmask the interrupt signaled by bit in I2C_STAT[AAS]. 0x0: Addressed as Slave interrupt disabled 0x1: Addressed as Slave interrupt enabled	RW	0
8	BF_IE	Bus Free interrupt enable. Mask or unmask the interrupt signaled by bit in I2C_STAT[BF]. 0x0: Bus Free interrupt disabled 0x1: Bus Free interrupt enabled	RW	0
7	AERR_IE	Access Error interrupt enable. Mask or unmask the interrupt signaled by bit in I2C_STAT[AERR]. 0x0: Access Error interrupt disabled 0x1: Access Error interrupt enabled	RW	0
6	STC_IE	Start Condition interrupt enable. Mask or unmask the interrupt signaled by bit in I2C_STAT[STC]. 0x0: Start Condition interrupt disabled 0x1: Start Condition interrupt enabled	RW	0
5	GC_IE	General call Interrupt enable. Mask or unmask the interrupt signaled by bit in I2C_STAT[GC] 0x0: General call interrupt disabled 0x1: General call interrupt enabled	RW	0
4	XRDY_IE	Transmit data ready interrupt enable. Mask or unmask the interrupt signaled by bit in I2C_STAT[XRDY] 0x0: Transmit data ready interrupt disabled 0x1: Transmit data ready interrupt enabled	RW	0
3	RRDY_IE	Receive data ready interrupt enable. Mask or unmask the interrupt signaled by bit in I2C_STAT[RRDY] 0x0: Receive data ready interrupt disabled 0x1: Receive data ready interrupt enabled	RW	0
2	ARDY_IE	Register access ready interrupt enable. Mask or unmask the interrupt signaled by bit in I2C_STAT[ARDY] 0x0: Register access ready interrupt disabled 0x1: Register access ready interrupt enabled	RW	0
1	NACK_IE	No acknowledgement interrupt enable. Mask or unmask the interrupt signaled by bit in I2C_STAT[NACK] 0x0: Not Acknowledge interrupt disabled 0x1: Not Acknowledge interrupt enabled	RW	0

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Bits	Field Name	Description	Type	Reset
0	AL_IE	Arbitration lost interrupt enable. Mask or unmask the interrupt signaled by bit in I2C_STAT[AL] 0x0: Arbitration lost interrupt disabled 0x1: Arbitration lost interrupt enabled	RW	0

Table 23-62. Register Call Summary for Register I2C_IE

Multimaster High-Speed I2C Controller

- HS I2C FIFO Interrupt Mode: [0]
- HS I2C FIFO Polling Mode: [1] [2]
- HS I2C Draining Feature (I2C Mode Only): [3] [4]
- HS I2C Programming Model in I2C Mode: [5] [6] [7] [8] [9] [10] [11] [12] [13] [14]
- HS I2C Basic Programming Model in SCCB Mode: [15] [16] [17] [18] [19] [20]
- HS I2C Register Summary: [21] [22]

Table 23-63. I2C_STAT

Address Offset	0x0000 0088
Physical Address	0x4806 0088 0x4807 0088 0x4807 2088 0x4835 0088
Description	I2C interrupt status vector (legacy).
Type	RW

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	XDR	RDR	BB	ROVR	XUDF	AAS	BF	AERR	STC	GC	XRDY	RRDY	ARDY	NACK	AL

Bits	Field Name	Description	Type	Reset
15	RESERVED	Write 0s for future compatibility. Read returns 0.	RW	0
14	XDR	Transmit draining IRQ status. 0x0: Transmit draining inactive. 0x1: Transmit draining enabled.	RW W1toClr	0
13	RDR	Receive draining IRQ status. 0x0: Receive draining inactive. 0x1: Receive draining enabled.	RW W1toClr	0
12	BB	Bus busy status.Writing into this bit has no effect. Read 0x1: Bus is occupied. Read 0x0: Bus is free.	R	0
11	ROVR	Receive overrun status.Writing into this bit has no effect. Read 0x1: Receiver overrun. Read 0x0: Normal operation.	RW W1toClr	0
10	XUDF	Transmit underflow status.Writing into this bit has no effect. Read 0x1: Transmit underflow. Read 0x0: Normal operation.	RW W1toClr	0
9	AAS	Address recognized as slave IRQ status. 0x0: No action. 0x1: Address recognized.	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
8	BF	Bus Free IRQ status. 0x0: No action. 0x1: Bus Free.	RW W1toClr	0
7	AERR	Access Error IRQ status. 0x0: No action. 0x1: Access Error.	RW W1toClr	0
6	STC	Start Condition IRQ status. 0x0: No action. 0x1: Start Condition detected.	RW W1toClr	0
5	GC	General call IRQ status. Set to 1 by core when General call address detected and interrupt signaled to MPUSS. Write 1 to clear. 0x0: No general call detected. 0x1: General call address detected.	RW W1toClr	0
4	XRDY	Transmit data ready IRQ status. Set to 1 by core when transmitter and when new data is requested. When set to 1 by core, an interrupt is signaled to MPUSS. Write 1 to clear. 0x0: Transmision ongoing. 0x1: Transmit data ready.	RW W1toClr	0
3	RRDY	Receive data ready IRQ status. Set to 1 by core when receiver mode, a new data is able to be read. When set to 1 by core, an interrupt is signaled to MPUSS. Write 1 to clear. 0x0: No data available. 0x1: Receive data available.	RW W1toClr	0
2	ARDY	Register access ready IRQ status. When set to 1 it indicates that previous access has been performed and registers are ready to be accessed again. An interrupt is signaled to MPUSS. Write 1 to clear. 0x0: Module busy. 0x1: Access ready.	RW W1toClr	0
1	NACK	No acknowledgement IRQ status. Bit is set when No Acknowledge has been received, an interrupt is signaled to MPUSS. Write 1 to clear this bit. 0x0: Normal operation. 0x1: Not Acknowledge detected.	RW W1toClr	0
0	AL	Arbitration lost IRQ status. This bit is automatically set by the hardware when it loses the Arbitration in master transmit mode, an interrupt is signaled to MPUSS. During reads, it always returns 0. 0x0: Normal operation. 0x1: Arbitration lost detected.	RW W1toClr	0

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Table 23-64. Register Call Summary for Register I2C_STAT

Multimaster High-Speed I2C Controller

- HS I2C Typical Connection Protocol and Data Format: [0] [1]
- HS I2C FIFO Interrupt Mode: [2] [3]
- HS I2C FIFO Polling Mode: [4] [5] [6] [7] [8] [9]
- HS I2C Draining Feature (I2C Mode Only): [10] [11] [12] [13] [14]
- HS I2C System Test Mode: [15] [16] [17]
- HS I2C Programming Model in I2C Mode: [18] [19] [20] [21] [22] [23] [24] [25] [26] [27] [28] [29] [30] [31] [32] [33] [34] [35] [36] [37] [38] [39] [40] [41] [42] [43] [44] [45] [46] [47] [48] [49]
- HS I2C Basic Programming Model in SCCB Mode: [50] [51] [52] [53] [54] [55] [56] [57] [58] [59] [60] [61] [62] [63] [64]
- HS I2C Register Summary: [65] [66]
- HS I2C Register Description: [67] [68] [69] [70] [71] [72] [73] [74] [75] [76] [77] [78] [79] [80] [81] [82] [83] [84] [85] [86] [87] [88] [89] [90] [91] [92] [93] [94] [95] [96] [97] [98] [99] [100] [101] [102]

Table 23-65. I2C_SYSS

Address Offset	0x0000 0090
Physical Address	0x4806 0090 0x4807 0090 0x4807 2090 0x4835 0090
Description	System Status register
Type	RW

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															RDONE

Bits	Field Name	Description	Type	Reset
15:1	RESERVED	Reserved	R	0x0000
0	RDONE	Reset done bit Read 0x1: Reset completed Read 0x0: Internal module reset in ongoing	RW	1

Table 23-66. Register Call Summary for Register I2C_SYSS

Multimaster High-Speed I2C Controller

- HS I2C Software Reset: [0] [1] [2]
- HS I2C Register Summary: [3] [4]

Table 23-67. I2C_BUF

Address Offset	0x0000 0094
Physical Address	0x4806 0094 0x4807 0094 0x4807 2094 0x4835 0094
Description	Buffer Configuration register
Type	RW

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RDMA_EN	RXFIFO_CLR	RXTRSH						XDMA_EN	TXFIFO_CLR	TXTRSH					

Bits	Field Name	Description	Type	Reset
15	RDMA_EN	Receive DMA channel enable 0x0: Receive DMA channel disabled 0x1: Receive DMA channel enabled	RW	0
14	RXFIFO_CLR	Receive FIFO clear 0x0: Normal mode 0x1: Rx FIFO is reset	RW	0
13:8	RXTRSH	Threshold value for FIFO buffer in RX mode	RW	0x00
7	XDMA_EN	Transmit DMA channel enable 0x0: Transmit DMA channel disabled 0x1: Transmit DMA channel enabled	RW	0
6	TXFIFO_CLR	Transmit FIFO clear 0x0: Normal mode 0x1: Tx FIFO is reset	RW	0
5:0	TXTRSH	Threshold value for FIFO buffer in TX mode	RW	0x00

Table 23-68. Register Call Summary for Register I2C_BUF

Multimaster High-Speed I2C Controller

- HS I2C FIFO Interrupt Mode: [0] [1] [2] [3] [4] [5] [6] [7]
- HS I2C FIFO Polling Mode: [8] [9]
- HS I2C FIFO DMA Mode (I2C Mode Only): [10] [11] [12] [13] [14] [15] [16]
- HS I2C Draining Feature (I2C Mode Only): [17] [18] [19] [20] [21] [22] [23] [24]
- HS I2C Write and Read Operations in SCCB Mode: [25] [26]
- HS I2C Programming Model in I2C Mode: [27] [28] [29] [30] [31] [32] [33] [34] [35] [36] [37] [38] [39] [40] [41] [42] [43] [44]
- HS I2C Basic Programming Model in SCCB Mode: [45] [46] [47] [48]
- HS I2C Register Summary: [49] [50]

Table 23-69. I2C_CNT

Address Offset	0x0000 0098
Physical Address	0x4806 0098 0x4807 0098 0x4807 2098 0x4835 0098
Description	Data counter register
Type	RW

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DCOUNT															

Bits	Field Name	Description	Type	Reset
15:0	DCOUNT	Data count **Note:** Because the transfer length for DCOUNT = 0x0000 is 65536, the module does not allow the initiation of zero-data-byte transfers.	RW	0x0000

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Table 23-70. Register Call Summary for Register I2C_CNT

Multimaster High-Speed I2C Controller

- HS I2C Draining Feature (I2C Mode Only): [0]
- HS I2C Programming Model in I2C Mode: [1] [2] [3] [4] [5] [6] [7] [8] [9]
- HS I2C Register Summary: [10] [11]

Table 23-71. I2C_DATA

Address Offset	0x0000 009C
Physical Address	0x4806 009C 0x4807 009C 0x4807 209C 0x4835 009C
Description	Data access register
Type	RW

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								DATA							

Bits	Field Name	Description	Type	Reset
15:8	RESERVED	Reserved	R	0x00
7:0	DATA	Transmit/Receive data FIFO endpoint	RW	0x--

Table 23-72. Register Call Summary for Register I2C_DATA

Multimaster High-Speed I2C Controller

- HS I2C DMA Requests: [0] [1] [2] [3] [4] [5] [6] [7]
- HS I2C Write and Read Operations in SCCB Mode: [8] [9]
- HS I2C System Test Mode: [10] [11]
- HS I2C Programming Model in I2C Mode: [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23]
- HS I2C Basic Programming Model in SCCB Mode: [24] [25] [26] [27] [28] [29]
- HS I2C Register Summary: [30] [31]

Table 23-73. I2C_CON

Address Offset	0x0000 00A4
Physical Address	0x4806 00A4 0x4807 00A4 0x4807 20A4 0x4835 00A4
Description	I2C configuration register.
Type	RW

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I2C_EN	RESERVED	OPMODE		STB	MST	TRX	XSA	XOA0	XOA1	XOA2	XOA3	RESERVED		STP	STT

Bits	Field Name	Description	Type	Reset
15	I2C_EN	I2C module enable. 0x0: Controller in reset. FIFO are cleared and status bits are set to their default value 0x1: Module enabled	RW	0

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Bits	Field Name	Description	Type	Reset
14	RESERVED	Reserved	R	0
13:12	OPMODE	Operation mode selection. 0x0: I2C Fast/Standard mode. 0x1: I2C High Speed mode. 0x3: Reserved. 0x2: SCCB mode.	RW	0x0
11	STB	Start byte mode (master mode only). 0x0: Normal mode 0x1: Start byte mode	RW	0
10	MST	Master/slave mode. 0x0: Slave mode 0x1: Master mode	RW	0
9	TRX	Transmitter/Receiver mode (master mode only). 0x0: Receiver mode 0x1: Transmitter mode	RW	0
8	XSA	Expand Slave address. 0x0: 7-bit address mode 0x1: 10-bit address mode	RW	0
7	XOA0	Expand Own address 0. 0x0: 7-bit address mode 0x1: 10-bit address mode	RW	0
6	XOA1	Expand Own address 1. 0x0: 7-bit address mode 0x1: 10-bit address mode	RW	0
5	XOA2	Expand Own address 2. 0x0: 7-bit address mode 0x1: 10-bit address mode	RW	0
4	XOA3	Expand Own address 3. 0x0: 7-bit address mode 0x1: 10-bit address mode	RW	0
3:2	RESERVED	Reserved.	R	0x0
1	STP	Stop condition (master mode only). 0x0: No action or stop condition detected 0x1: Stop condition queried	RW	0
0	STT	Start condition (master mode only). 0x0: No action or start condition detected 0x1: Start condition queried	RW	0

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Table 23-74. Register Call Summary for Register I2C_CON

Multimaster High-Speed I2C Controller

- HS I2C SCCB Interface Typical Connections: [0]
- HS I2C Block Diagram: [1] [2]
- HS I2C Clocking: [3]
- HS I2C Software Reset: [4] [5] [6] [7] [8]
- HS I2C Programmable Multislave Channel Feature (I2C Mode Only): [9] [10] [11] [12]
- HS I2C FIFO Interrupt Mode: [13] [14]
- HS I2C Write and Read Operations in SCCB Mode: [15] [16] [17] [18]
- HS I2C System Test Mode: [19] [20] [21]
- HS I2C Programming Model in I2C Mode: [22] [23] [24] [25] [26] [27] [28] [29] [30] [31] [32] [33] [34] [35] [36] [37] [38] [39] [40] [41] [42] [43] [44] [45] [46] [47] [48] [49] [50] [51] [52] [53] [54] [55] [56] [57] [58] [59] [60] [61] [62] [63]
- HS I2C Basic Programming Model in SCCB Mode: [64] [65] [66] [67] [68] [69] [70] [71] [72] [73] [74]
- HS I2C Register Summary: [75] [76]

Table 23-75. I2C_OA

Address Offset	0x0000 00A8
Physical Address	0x4806 00A8 0x4807 00A8 0x4807 20A8 0x4835 00A8
Description	Own address register
Type	RW

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MCODE			RESERVED					OA							

Bits	Field Name	Description	Type	Reset
15:13	MCODE	Master Code	RW	0x0
12:10	RESERVED	Reserved	R	0x0
9:0	OA	Own address	RW	0x000

Table 23-76. Register Call Summary for Register I2C_OA

Multimaster High-Speed I2C Controller

- HS I2C Automatic Blocking of the I2C Clock Feature (I2C Mode Only): [0] [1]
- HS I2C Programmable Multislave Channel Feature (I2C Mode Only): [2] [3]
- HS I2C Write and Read Operations in SCCB Mode: [4] [5]
- HS I2C Programming Model in I2C Mode: [6] [7] [8]
- HS I2C Basic Programming Model in SCCB Mode: [9] [10]
- HS I2C Register Summary: [11] [12]

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Table 23-77. I2C_SA

Address Offset	0x0000 00AC
Physical Address	0x4806 00AC 0x4807 00AC 0x4807 20AC 0x4835 00AC
Description	Slave address register
Type	RW

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								SA							

Bits	Field Name	Description	Type	Reset
15:10	RESERVED	Reserved	R	0x00
9:0	SA	Slave address	RW	0x3FF

Table 23-78. Register Call Summary for Register I2C_SA

Multimaster High-Speed I2C Controller

- HS I2C Write and Read Operations in SCCB Mode: [0] [1]
- HS I2C Programming Model in I2C Mode: [2] [3] [4] [5] [6] [7] [8] [9]
- HS I2C Basic Programming Model in SCCB Mode: [10] [11]
- HS I2C Register Summary: [12] [13]

Table 23-79. I2C_PSC

Address Offset	0x0000 00B0
Physical Address	0x4806 00B0 0x4807 00B0 0x4807 20B0 0x4835 00B0
Description	I2C Clock Prescaler Register
Type	RW

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PSC							

Bits	Field Name	Description	Type	Reset
15:8	RESERVED	Reserved	R	0x00
7:0	PSC	Fast/Standard mode prescale sampling clock divider value 0x0: Divide by 1 0x1: Divide by 2 ..... 0xFF: Divide by 256	RW	0x00

Table 23-80. Register Call Summary for Register I2C_PSC

Multimaster High-Speed I2C Controller

- HS I2C Typical Connection Protocol and Data Format: [0] [1] [2]
- HS I2C Clocking: [3] [4] [5]
- HS I2C Noise Filter: [6] [7]
- HS I2C System Test Mode: [8]
- HS I2C Programming Model in I2C Mode: [9] [10]
- HS I2C Basic Programming Model in SCCB Mode: [11] [12] [13]
- HS I2C Register Summary: [14] [15]

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Table 23-81. I2C_SCLL

Address Offset	0x0000 00B4
Physical Address	0x4806 00B4 0x4807 00B4 0x4807 20B4 0x4835 00B4
Description	I2C SCL Low Time Register.
Type	RW

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HSSCLL								SCLL							

Bits	Field Name	Description	Type	Reset
15:8	HSSCLL	High Speed mode SCL low time	RW	0x00
7:0	SCLL	Fast/Standard mode SCL low time.	RW	0x00

Table 23-82. Register Call Summary for Register I2C_SCLL

Multimaster High-Speed I2C Controller

- HS I2C Clocking: [0] [1] [2] [3] [4] [5] [6] [7] [8]
- HS I2C System Test Mode: [9]
- HS I2C Programming Model in I2C Mode: [10] [11] [12]
- HS I2C Basic Programming Model in SCCB Mode: [13] [14] [15] [16]
- HS I2C Register Summary: [17] [18]

Table 23-83. I2C_SCLH

Address Offset	0x0000 00B8
Physical Address	0x4806 00B8 0x4807 00B8 0x4807 20B8 0x4835 00B8
Description	I2C SCL High Time Register.
Type	RW

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HSSCLH								SCLH							

Bits	Field Name	Description	Type	Reset
15:8	HSSCLH	High Speed mode SCL high time	RW	0x00
7:0	SCLH	Fast/Standard mode SCL high time.	RW	0x00

Table 23-84. Register Call Summary for Register I2C_SCLH

Multimaster High-Speed I2C Controller

- HS I2C Clocking: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10]
- HS I2C System Test Mode: [11]
- HS I2C Programming Model in I2C Mode: [12] [13] [14]
- HS I2C Basic Programming Model in SCCB Mode: [15] [16]
- HS I2C Register Summary: [17] [18]

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Table 23-85. I2C_SYSTEST

Address Offset	0x0000 00BC
Physical Address	0x4806 00BC 0x4807 00BC 0x4807 20BC 0x4835 00BC
Description	I2C System Test Register.
Type	RW

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ST_EN	FREE	TMODE		SSB	RESERVED		SCL_I_FUNC	SCL_O_FUNC	SDA_I_FUNC	SDA_O_FUNC	SCCB_E_O	SCL_I	SCL_O	SDA_I	SDA_O

Bits	Field Name	Description	Type	Reset
15	ST_EN	System test enable. 0x0: Normal mode. All others bits in register are read only 0x1: System test enabled. Permit other system test registers bits to be set	RW	0
14	FREE	Free running mode (on breakpoint) 0x0: Stop mode (on breakpoint condition). If Master mode, it stops after completion of the ongoing bit transfer. In slave mode, it stops during the phase transfer when 1 byte is completely transmitted/received. 0x1: Free running mode	RW	0
13:12	TMODE	Test mode select. 0x0: Functional mode (default) 0x1: Reserved 0x3: Loop back mode select + SDA/SCL IO mode select 0x2: Test of SCL counters (SCLL, SCLH, PSC). SCL provides a permanent clock with master mode.	RW	0x0
11	SSB	Set status bits from 0 to 14. 0x0: No action 0x1: Set interrupt status bits to 1	RW	0
10:9	RESERVED	Reserved	R	0x0
8	SCL_I_FUNC	SCL line input value (functional mode). Read 0x1: Read 1 from SCL line Read 0x0: Read 0 from SCL line	R	1
7	SCL_O_FUNC	SCL line output value (functional mode). Read 0x1: Driven 1 on SCL line Read 0x0: Driven 0 on SCL line	R	1
6	SDA_I_FUNC	SDA line input value (functional mode). Read 0x1: Read 1 from SDA line Read 0x0: Read 0 from SDA line	R	1
5	SDA_O_FUNC	SDA line output value (functional mode). Read 0x1: Driven 1 to SDA line Read 0x0: Driven 0 to SDA line	R	1
4	SCCB_E_O	SCCB_E line sense output value. 0x0: Write 0 to SCCBE line 0x1: Write 1 to SCCBE line	RW	0

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Bits	Field Name	Description	Type	Reset
3	SCL_I	SCL line sense input value Read 0x1: Read 1 from SCL line Read 0x0: Read 0 from SCL line	R	0
2	SCL_O	SCL line drive output value. 0x0: Write 0 to SCL line 0x1: Write 1 to SCL line	RW	0
1	SDA_I	SDA line sense input value. Read 0x1: Read 1 from SDA line Read 0x0: Read 0 from SDA line	R	0
0	SDA_O	SDA line drive output value. 0x0: Write 0 to SDA line 0x1: Write 1 to SDA line	RW	0

Table 23-86. Register Call Summary for Register I2C_SYSTEST

Multimaster High-Speed I2C Controller
- HS I2C System Test Mode: [0] [1] [2] [3] [4] [5] [6] [7] [8]
- HS I2C Register Summary: [9] [10]

Table 23-87. I2C_BUFSTAT

Address Offset	0x0000 00C0
Physical Address	0x4806 00C0 0x4807 00C0 0x4807 20C0 0x4835 00C0
Description	I2C Buffer Status Register.
Type	R

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIFODEPTH		RXSTAT						RESERVED		TXSTAT					

Bits	Field Name	Description	Type	Reset
15:14	FIFODEPTH	Internal FIFO buffers depth.	R	0x3
13:8	RXSTAT	RX Buffer Status	R	0x00
7:6	RESERVED	Reserved	R	0x0
5:0	TXSTAT	TX Buffer Status.	R	0x00

Table 23-88. Register Call Summary for Register I2C_BUFSTAT

Multimaster High-Speed I2C Controller
- HS I2C FIFO Management: [0]
- HS I2C Draining Feature (I2C Mode Only): [1] [2] [3] [4] [5] [6] [7] [8]
- HS I2C Programming Model in I2C Mode: [9] [10] [11] [12] [13] [14] [15] [16]
- HS I2C Register Summary: [17] [18]

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Table 23-89. I2C_OA1

Address Offset	0x0000 00C4
Physical Address	0x4806 00C4 0x4807 00C4 0x4807 20C4 0x4835 00C4
Description	I2C Own Address 1 Register
Type	RW

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								OA1							

Bits	Field Name	Description	Type	Reset
15:10	RESERVED	Reserved	R	0x00
9:0	OA1	Own address 1	RW	0x000

Table 23-90. Register Call Summary for Register I2C_OA1

Multimaster High-Speed I2C Controller

- HS I2C Register Summary: [0] [1]

Table 23-91. I2C_OA2

Address Offset	0x0000 00C8
Physical Address	0x4806 00C8 0x4807 00C8 0x4807 20C8 0x4835 00C8
Description	I2C Own Address 2 Register
Type	RW

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								OA2							

Bits	Field Name	Description	Type	Reset
15:10	RESERVED	Reserved	R	0x00
9:0	OA2	Own address 2	RW	0x000

Table 23-92. Register Call Summary for Register I2C_OA2

Multimaster High-Speed I2C Controller

- HS I2C Register Summary: [0] [1]

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Table 23-93. I2C_OA3

Address Offset	0x0000 00CC
Physical Address	0x4806 00CC 0x4807 00CC 0x4807 20CC 0x4835 00CC
Description	I2C Own Address 3 Register
Type	RW

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								OA3							

Bits	Field Name	Description	Type	Reset
15:10	RESERVED	Reserved	R	0x00
9:0	OA3	Own address 3	RW	0x000

Table 23-94. Register Call Summary for Register I2C_OA3

Multimaster High-Speed I2C Controller

- HS I2C Register Summary: [0] [1]

Table 23-95. I2C_ACTOA

Address Offset	0x0000 00D0
Physical Address	0x4806 00D0 0x4807 00D0 0x4807 20D0 0x4835 00D0
Description	I2C Active Own Address Register.
Type	R

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												OA3_ACT	OA2_ACT	OA1_ACT	OA0_ACT

Bits	Field Name	Description	Type	Reset
15:4	RESERVED	Reserved	R	0x000
3	OA3_ACT	Own Address 3 active. Read 0x1: Own Address active. Read 0x0: Own Address inactive.	R	0
2	OA2_ACT	Own Address 2 active. Read 0x1: Own Address active. Read 0x0: Own Address inactive.	R	0
1	OA1_ACT	Own Address 1 active. Read 0x1: Own Address active. Read 0x0: Own Address inactive.	R	0
0	OA0_ACT	Own Address 0 active. Read 0x1: Own Address active. Read 0x0: Own Address inactive.	R	0

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Table 23-96. Register Call Summary for Register I2C_ACTOA

Multimaster High-Speed I2C Controller

- HS I2C Programmable Multislave Channel Feature (I2C Mode Only): [0]
- HS I2C Register Summary: [1] [2]

Table 23-97. I2C_SBLOCK

Address Offset	0x0000 00D4
Physical Address	0x4806 00D4 0x4807 00D4 0x4807 20D4 0x4835 00D4
Description	I2C Clock Blocking Enable Register.
Type	RW

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												OA3_EN	OA2_EN	OA1_EN	OA0_EN

Bits	Field Name	Description	Type	Reset
15:4	RESERVED	Reserved	R	0x000
3	OA3_EN	Enable I2C Clock Blocking for Own Address 3. 0x0: I2C Clock Released. 0x1: I2C Clock Blocked.	RW	0
2	OA2_EN	Enable I2C Clock Blocking for Own Address 2. 0x0: I2C Clock Released. 0x1: I2C Clock Blocked.	RW	0
1	OA1_EN	Enable I2C Clock Blocking for Own Address 1. 0x0: I2C Clock Released. 0x1: I2C Clock Blocked.	RW	0
0	OA0_EN	Enable I2C Clock Blocking for Own Address 0. 0x0: I2C Clock Released. 0x1: I2C Clock Blocked.	RW	0

Table 23-98. Register Call Summary for Register I2C_SBLOCK

Multimaster High-Speed I2C Controller

- HS I2C Automatic Blocking of the I2C Clock Feature (I2C Mode Only): [0]
- HS I2C Register Summary: [1] [2]

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23.2 HDQ/1-Wire

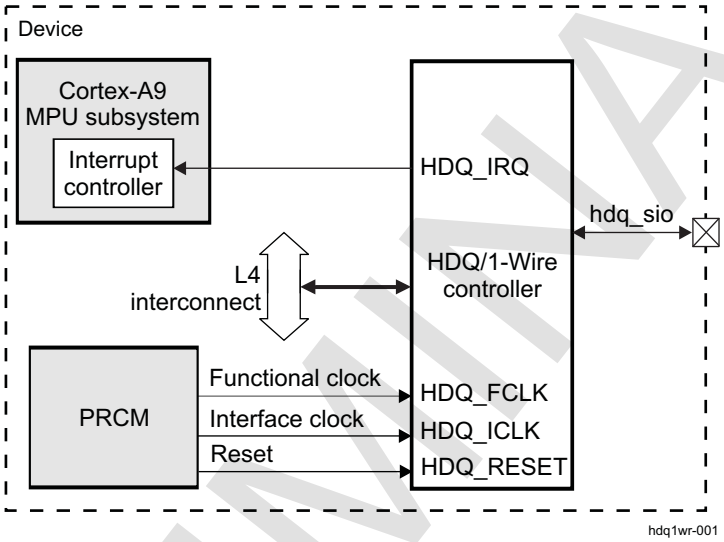
This section describes the HDQ™/ 1-Wire® interface for the device.

23.2.1 HDQ/1-Wire Overview

The HDQ/1-Wire module implements the hardware protocol of the master functions of the TI/Benchmarq HDQ and the Dallas Semiconductor 1-Wire® protocols. These protocols use a single wire for communication between the master (HDQ/1-Wire controller) and the slaves (HDQ/1-Wire external compliant devices).

Figure 23-42 shows the HDQ/1-Wire.

Figure 23-42. HDQ/1-Wire Overview



The HDQ/1-Wire has a generic L4 interface and is intended to be used in an interrupt-driven fashion. The 1-pin interface is implemented as an open-drain output at the device level.

The main features supported by the HDQ/1-Wire are the following:

- Benchmarq HDQ protocol
- Dallas Semiconductor 1-Wire protocol
- Power-down mode

The HDQ/1-Wire provides a communication rate of 5 Kbps over an address space of 128 bytes.

A typical application of the HDQ/1-Wire is the communication with battery monitor (gas gauge) integrated circuits.

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23.2.2 HDQ/1-Wire Environment

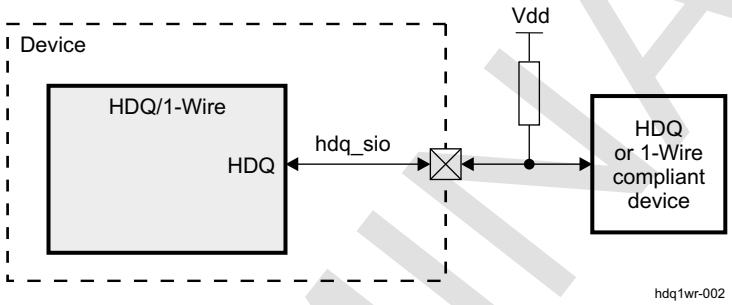
23.2.2.1 HDQ/1-Wire Functional Modes

The HDQ/1-Wire has two main modes: HDQ and 1-Wire. Each of these modes includes idle, active, and power-down submodes. Table 23-99 lists the HDQ/1-Wire functional modes, and Figure 23-43 shows an overview of a typical application.

Table 23-99. Functional Modes

Functions	Description
HDQ	Benchmarq HDQ protocol
1-Wire	Dallas Semiconductor 1-Wire protocol

Figure 23-43. HDQ/1-Wire Typical Application System Overview



An external pullup is required, because the two protocols use a return-to-1 mechanism (that is, after any command by any of the connected devices, the line is pulled to a logical high level).

The HDQ/1-Wire operates according to a command structure that is programmed into transmit command registers (as described in Section 23.2.5.1.2, *HDQ/1-Wire Low-level Programming Model*).

The 1-Wire mode runs at slower speeds than the capabilities of the mode.

Table 23-100 describes the external signal of the HDQ/1-Wire compliant module.

Table 23-100. I/O Description

Signal	I/O (1)	Description	Value at Reset
hdq_sio	I/O	Serial data input/output.Output is open drain type.	HiZ (pulled to 1 by pullup)

(1) I = Input; O = Output

23.2.2.2 HDQ and 1-Wire (SDQ) Protocols

23.2.2.2.1 HDQ Protocol Initialization (Default)

In HDQ mode, the firmware does not require the host to create an initialization pulse to the slave. However, the slave can be reset by using an initialization pulse (also referred to as a break pulse). The initialization pulse is generated by setting the HDQ_CTRL_STATUS[2] INITIALIZATION bit and then setting the HDQ_CTRL_STATUS[4] GO bit. The slave does not respond with a presence pulse as it does in the 1-Wire protocol.

The HDQ is a command-based protocol in which the host sends a command byte to the slave. The command directs the slave either to store the next eight bits of data received to a register specified by the command byte (write operation) or to output the eight bits of data from a register specified by the command byte (read operation). The master implementation is a simple byte engine. Sending of the ID, command/address, and data is controlled by firmware. The master engine provides only a single HDQ.HDQ_TX_DATA register.

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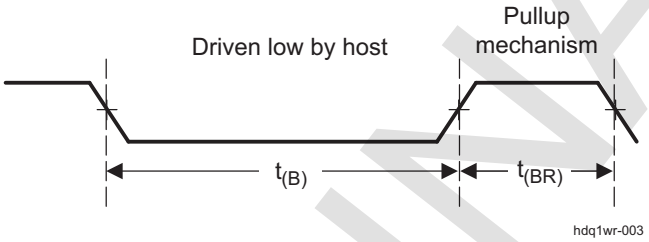
The command and data bytes consist of a stream of eight bits with a maximum transmission rate of 5 Kbps. The least-significant bit (LSB) of a command or data byte is transmitted first. If a communication time-out occurs between the host and the slave (for example, if the host waits longer than the specified time for the slave to respond, or if this is the first access command), then the host must send an initialization pulse (BREAK) before sending the command again.

The slave detects a break when the HDQ pin is driven to a logic-low state for a specified break time t(B) or greater. The HDQ pin then returns to its normal ready-high logic state for a specified break-recovery time t(BR). The slave is then ready for a command from the host processor. Figure 23-44 shows this behavior.

An interrupt condition indicates a TX-complete, an RX-complete, or a time-out condition. Reading the interrupt status register clears all interrupt conditions. Only one interrupt signal is sent to the microcontroller, and only one overall mask bit can enable or disable the interrupt. The interrupt conditions cannot be individually masked.

Figure 23-44. HDQ Break-Pulse Timing Diagram

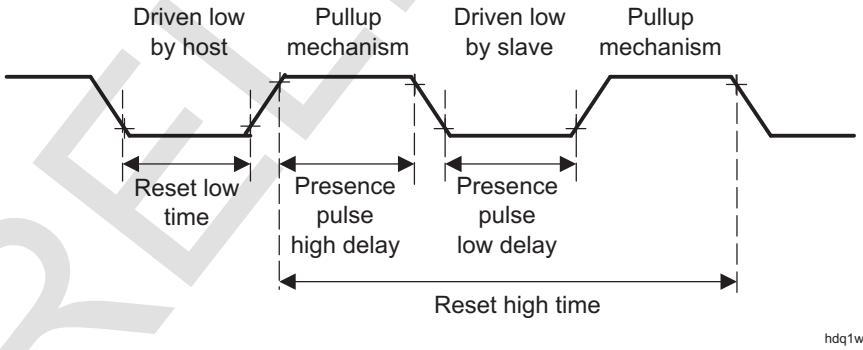


23.2.2.2.2 1-Wire (SDQ) Protocol Initialization

In 1-Wire (SDQ) protocol, the host first sends an initialization pulse (by pulling the line to a logic-low state) and then waits for the slave to respond with a presence pulse before enabling any communication sequence.

As for the initialization pulse, the presence pulse is a low-level pulse on the line initiated by the slave. The timing diagram in Figure 23-45 shows the 1-Wire (SDQ) reset sequence.

Figure 23-45. 1-Wire (SDQ) Reset Timing Diagram



The host drives the line to a logic-low state for a minimum of reset low time. Once the slave detects this pulse, it must drive the line to a logic-low state within the presence pulse high delay for a minimum period of presence pulse low time.

If the slave does not respond within this interval of time, a time-out event occurs and no transaction can be initiated. The host must initiate the reset sequence again before sending any command to the slave.

On the other hand, if the slave sends back its presence pulse within the specified time interval, the communication can be enabled after the reset high time.

23.2.2.2.3 Communication Sequence (HDQ and 1-Wire Protocols)

The description in this section applies to both protocols.

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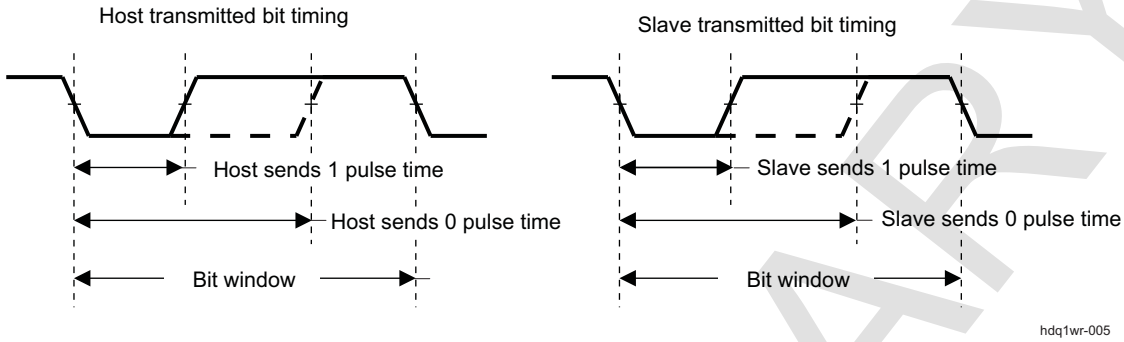
After a successful break pulse (HDQ mode) or initialization sequence (1-Wire protocol), the host and slave are ready for bit transmission. Each bit to transmit (either from the host to the slave or from the slave to the host) is preceded by a low-going edge on the line, as shown in Figure 23-46.

Figure 23-46. HDQ/1-Wire Transmitted Bit Timing



The return-to-1 data-bit frame consists of three distinct sections. The first section starts the transmission when either the slave or the host takes the line to a logic-low state. The next section is the actual data transmission in which the data must be valid during a specified period of time after the negative edge that starts the communication. The final section stops the transmission by returning the HDQ/1-Wire line to a logic-high state. Communication with an HDQ/1-Wire slave always occurs with the LSB being transmitted first.

The command byte of the HDQ/1-Wire protocols consists of eight contiguous valid command bits. The command byte contains two fields: R/W command and address. The R/W bit of the command byte determines whether the command is a read or a write, and the address field containing bits AD6-AD0 indicates the address to be read or written. Table 23-101 lists the command byte values.

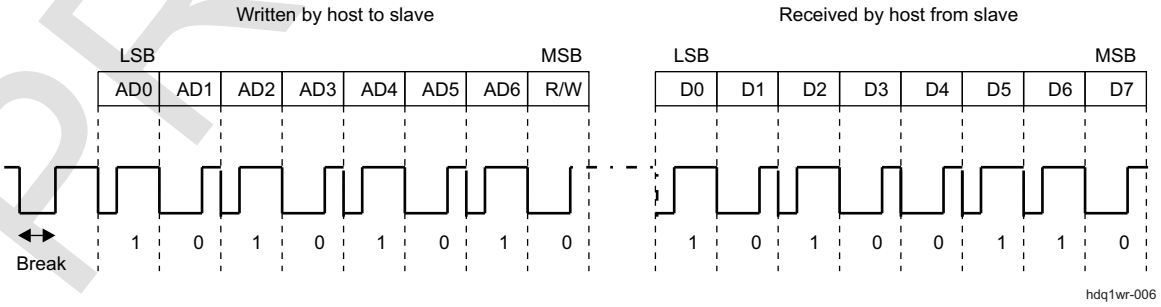
Table 23-101. HDQ/1-Wire Command Byte

7	6	5	4	3	2	1	0
R/W	AD6	AD5	AD4	AD3	AD2	AD1	AD0

R/W Indicates whether the command byte is a read or a write. A 1 indicates a write command; the following eight bits must be written to the register specified by the address field of the command byte. A 0 indicates that the command is a read. On a read command, the slave outputs the requested register contents.

AD6-AD0 Represent the seven bits labeled AD6-AD0 containing the address portion of the register to be accessed.
The communication sequence example in Figure 23-47 shows a read command at address 0x55; the received data is 0x65.

Figure 23-47. HDQ/1-Wire Communication Sequence



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23.2.3 HDQ/1-Wire Integration

Figure 23-48 shows HDQ/1-Wire integration in the device.

Figure 23-48. HDQ/1-Wire Integration

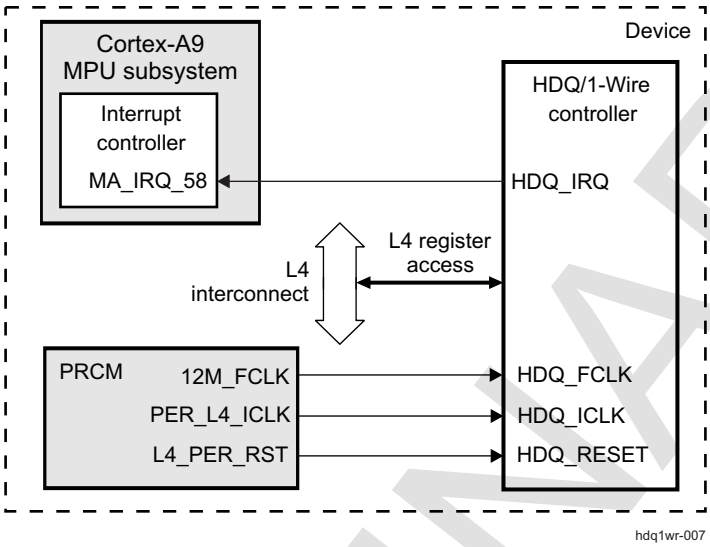

Table 23-102 through Table 23-104 summarize the integration of the module in the device.

Table 23-102. Integration Attributes

Module Instance	Attributes		
	Power Domain	Wake-Up Capability	Interconnect
HDQ/1-Wire	DPLL_PER	No	L4_PER

Table 23-103. Clocks and Resets

Clocks				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
HDQ/1-Wire	HDQ_ICLK	PER_L4_ICLK	PRCM	Interface clock
HDQ/1-Wire	HDQ_FCLK	12M_FCLK	PRCM	Functional clock
Resets				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
HDQ/1-Wire	HDQ_RESET	L4_PER_RST	PRCM	HDQ/1-wire reset signal

Table 23-104. Hardware Requests

Interrupt Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
HDQ/1-Wire	HDQ_IRQ	MA_IRQ_58	Cortex-A9	Interrupt to the Cortex A9 MPU subsystem interrupt controller (INTC).

NOTE: For the description of the interrupt source, see Section 17.4.1, *Cortex-A9 MPU INTC Functional Description*, in Chapter 17, *Interrupt Controllers*.

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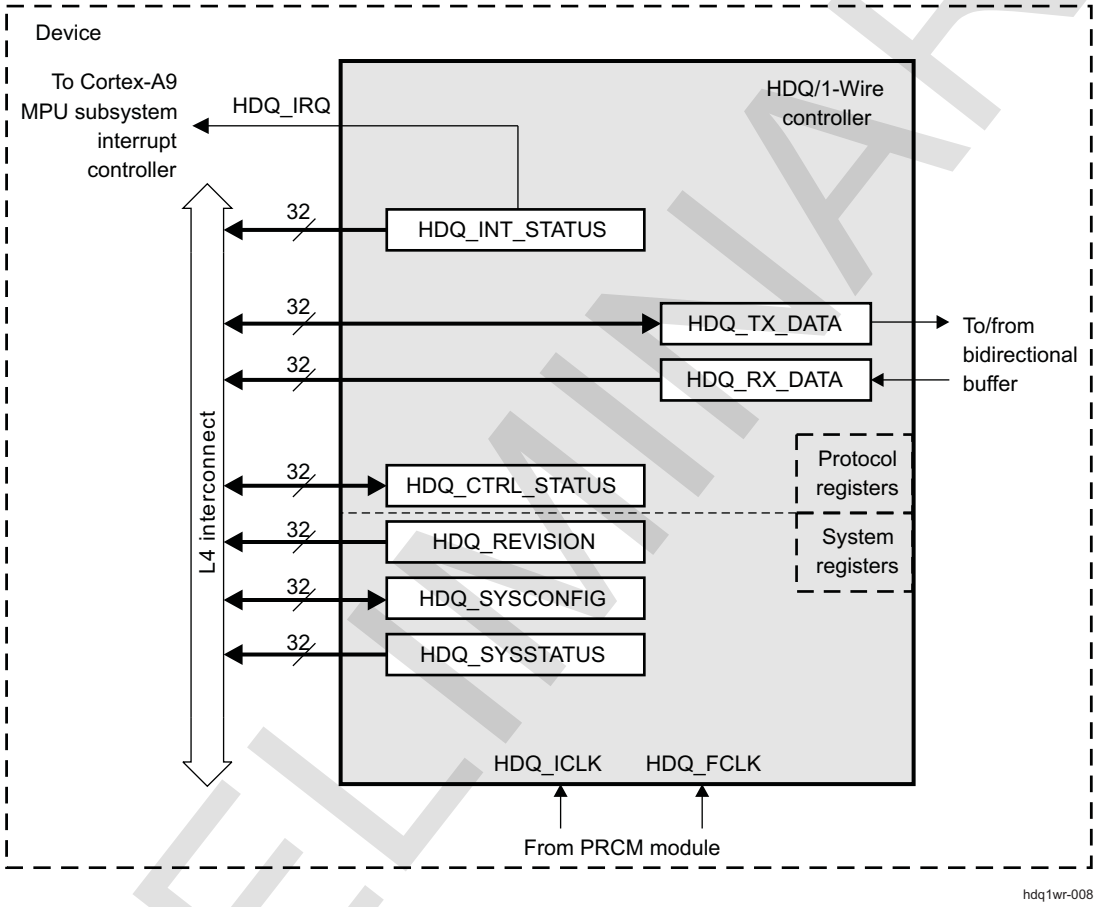
23.2.4 HDQ/1-Wire Functional Description

The HDQ/1-Wire works with HDQ and 1-Wire protocols. The protocols use a single wire to establish communication between the master and the slave. Both protocols use a return-to-1 mechanism; that is, after any command is driven, the line is pulled to a high level. This mechanism requires an external pullup.

23.2.4.1 HDQ/1-Wire Block Diagram

Figure 23-49 is the HDQ/1-Wire block diagram.

Figure 23-49. HDQ/1-Wire Block Diagram



The HDQ.HDQ_CTRL_STATUS[0] MODE bit allows selection between the HDQ and 1-Wire protocols. This bit is assumed static for design purposes. The configuration is in HDQ mode by default.

Figure 23-50 shows the protocol-dedicated register scheme.

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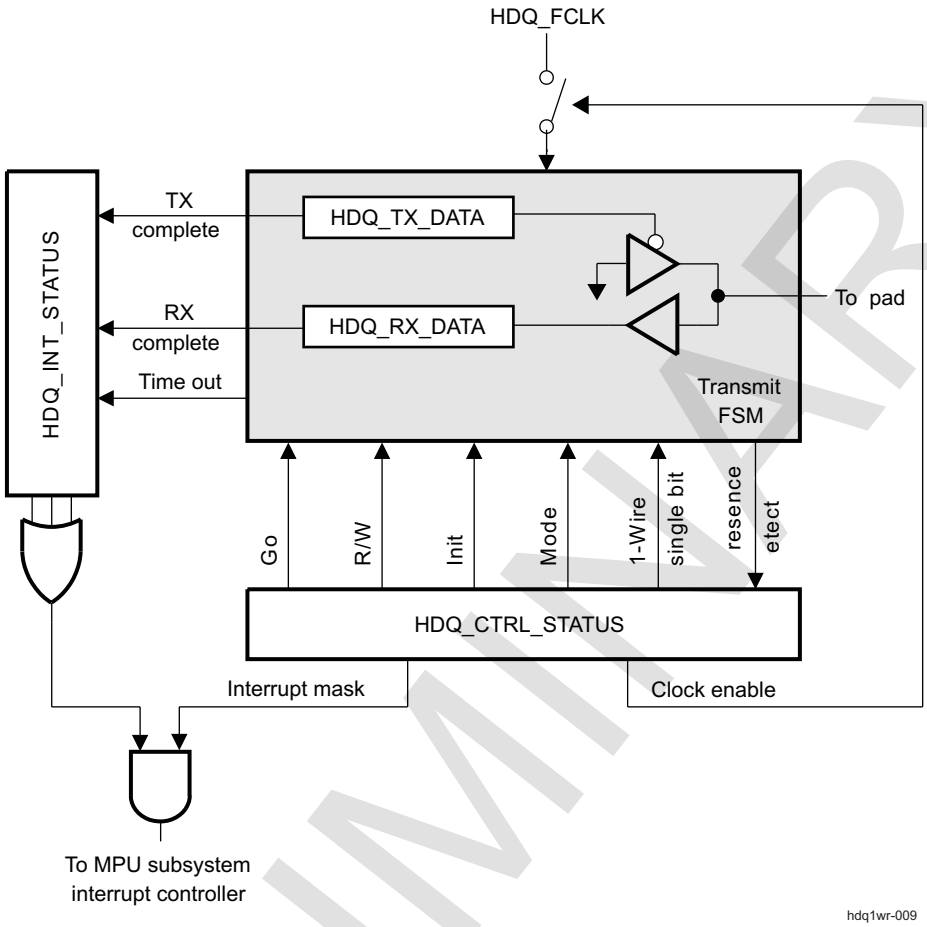
Figure 23-50. Protocol Registers Description



The receive and transmit operations of the HDQ/1-Wire module are performed with respect to the timing of the slower HDQ protocol. When the 1-Wire protocol is used, it runs at lower speed than its full capabilities, but is still able to meet the timing requirements and practical considerations.

23.2.4.2 HDQ/1-Wire Clocking Configuration

23.2.4.2.1 HDQ/1-Wire Clocks

The HDQ/1-Wire subsystem operates from two clocks: a functional clock (HDQ_FCLK) and an interface clock (HDQ_ICLK). When these clocks are set in the PRCM module, the following rule must be observed: HDQ_ICLK ≥ HDQ_FCLK.

- The HDQ_FCLK functional clock is a fixed clock provided by the PRCM module. It is used to clock the internal module logic.

  For more information about the clock, see Section 3.6.8, *CD_L4_PER Clock Domain*, in Chapter 3, *Power, Reset, and Clock Management*.

  When the HDQ/1-Wire no longer requires the HDQ_FCLK, the software can disable it at the PRCM level. The clock is effectively cut, provided the other modules that receive it do not require it either.

  For details about the PRCM register settings and clock configuration, see Section 3.6.8, *CD_L4_PER Clock Domain*, in Chapter 3, *Power, Reset, and Clock Management*.
- The HDQ_ICLK interface clock runs at L4 interconnect clock speed and is used to trigger access to the HDQ/1-Wire L4 interface.

  When the HDQ/1-Wire no longer requires the HDQ_ICLK (no transfer is in progress), the software can disable it at the PRCM level. The clock is effectively cut, provided the other modules that receive it do

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not require it either.

For more information, see Section 3.6.8, *CD_L4_PER Clock Domain*.

23.2.4.3 HDQ/1-Wire Hardware and Software Reset

Global reset of the module is done at the power, reset, and clock management (PRCM) module level (for more information, see Section 3.6.8, *CD_L4_PER Clock Domain*) or by setting the HDQ.HDQ_SYSCONFIG[1] SOFTRESET bit to 1. Setting this bit enables an active software reset functionality equivalent to a hardware reset. The HDQ_FCLK functional clock must be enabled from the PRCM level and locally through the HDQ_CTRL_STATUS[5] CLOCKENABLE bit (set to 1) for the software reset to complete.

23.2.4.4 HDQ/1-Wire Power Management

Table 23-105 describes power-management features available to the HDQ/1-Wire.

Table 23-105. Local Power-Management Features

Feature	Registers	Description
Clock auto gating	HDQ_SYSCONFIG [0] AUTOIDLE bit	Auto-idle mode
Slave idle modes	N/A	N/A
Clock enable	HDQ.HDQ_CTRL_STATUS[5] CLOCKENABLE bit	Power-down mode
Master standby modes	N/A	N/A
Global wake-up enable	N/A	N/A
Wake-up sources enable	N/A	N/A

23.2.4.4.1 Auto-Idle Mode

The HDQ/1-Wire provides an auto-idle function in its interconnect clock domain.

The interconnect clock auto-idle power-saving mode is enabled or disabled through the HDQ.HDQ_SYSCONFIG[0] AUTOIDLE bit. When this mode is enabled and there is no activity on the interconnect interface, the interconnect clock (HDQ_ICLK) is disabled inside the module, thereby reducing power consumption. When there is new activity on the interconnect interface, the interconnect clock is restarted with no latency penalty. This mode is disabled by default after a reset.

The auto-idle mode can be enabled in order to reduce power consumption.

23.2.4.4.2 Power-Down Mode

The HDQ/1-Wire also provides a power-saving function in its functional clock domain.

Setting the CLOCKENABLE bit in the control and status register (HDQ.HDQ_CTRL_STATUS[5] CLOCKENABLE bit) to 0 shuts off the functional clock (HDQ_FCLK) to the state-machine. The state-machine is reset when the functional clock is disabled; if any transaction is ongoing, it is aborted into the reset state.

Before shutting off the functional clock, the software must wait for transaction-complete interrupt. In write operation the software must check whether the interrupt was generated after address/command byte was sent or after data byte was sent. The functional clock must not be shut off after address/command byte is sent; otherwise, the data is not written to the slave.

The register values are not affected by disabling the functional clock.

CAUTION

There is no hardware mechanism to prevent cutting off the HDQ/1-Wire clocks while the module is performing a transfer. This would result in loss of data being transferred.

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23.2.4.5 HDQ Interrupt Requests

The HDQ/1-Wire can generate one interrupt:

- HDQ_IRQ: This is an interrupt to the MPU subsystem INTC. It is mapped on MA_IRQ_58. Table 23-106 lists the events that can generate this interrupt.

Table 23-106. Events

Event Flag	Event Mask	Sync	Sensitivity	Map to	Description
HDQ_INT_STATUS[2] TXCOMPLETE	HDQ_CTRL_STATUS[31] INTERRUPTMASK	Yes	Level	HDQ_IRQ	A write operation of one byte was completed.
HDQ_INT_STATUS[1] RXCOMPLETE	HDQ_CTRL_STATUS[31] INTERRUPTMASK	Yes	Level	HDQ_IRQ	A byte has been successfully read.
HDQ_INT_STATUS[0] TIMEOUT	HDQ_CTRL_STATUS[31] INTERRUPTMASK	Yes	Level	HDQ_IRQ	After a read command initiated by the host, the slave did not pull the line low within the specified time.

23.2.4.6 HDQ Mode (Default)

23.2.4.6.1 HDQ Mode Features

The HDQ mode supports the following:

- Benchmarq HDQ protocol
- Power-down mode

23.2.4.6.2 Description

In the HDQ mode, there is no need for the host to create an initialization pulse to the slave. However, the host can reset the slave by using an initialization pulse (also known as a break pulse). Setting the HDQ.HDQ_CTRL_STATUS[2] INITIALIZATION bit and then setting the HDQ_CTRL_STATUS[4] GO bit creates this pulse by pulling the line down for a defined duration. When the slave receives the pulse, it is ready for communication but does not respond with a presence pulse.

In a typical write operation, two bytes are sent to the slave. The first byte corresponds to the command/address byte, and the second byte corresponds to the data to be written.

In a typical read operation, the host sends a command/address byte and the slave returns a byte of data.

The master is implemented to send and receive bytes. Sending the command/address and data is controlled by the firmware. The master provides only a single data TX register.

The HDQ protocol is a return-to-1 protocol. Consequently, after a byte is sent to the slave (either command/address + data for a write, or just command/address for a read), the host pulls the line up. The line is set to the high-impedance state in the device and an external pullup brings it to a logical high level.

In the case of a read operation, the slave also drives the line to a logic-low state before sending the requested data.

If the host initiates a read and does not receive data within a specified interval of time (that is, the slave does not drive the line low within this interval), the HDQ.HDQ_INT_STATUS[0] TIMEOUT bit is set, thereby indicating a read failure. The TIMEOUT bit remains set until the host reads the interrupt status register (HDQ.HDQ_INT_STATUS).

An interrupt condition indicates either a TX-complete, an RX-complete, or a time-out on a transaction. The corresponding bit is set in the interrupt status register (HDQ.HDQ_INT_STATUS). This register is cleared as soon as it is read.

Only one interrupt signal is sent to the MPU, and only an overall mask can enable or disable the interrupts. These interrupts cannot be individually masked.

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23.2.4.6.3 Single-Bit Mode

In HDQ mode, the single-bit mode (HDQ.HDQ_CTRL_STATUS[7] ONE_WIRE_SINGLE_BIT bit set to 1) has no effect because the HDQ protocol supports only byte transfers.

23.2.4.6.4 Interrupt Conditions

The HDQ/1-Wire provides the following interrupt status:

- Transmission complete:

  A write operation of one byte was completed. Successful or failed completion is not indicated, because there is no acknowledgment from the slave in HDQ protocol. This interrupt condition is cleared by reading the interrupt status register (HDQ.HDQ_INT_STATUS).

- Read complete:

  In HDQ mode, the interrupt status indicates that a byte has been successfully read. This interrupt condition is cleared by reading the interrupt status register (HDQ.HDQ_INT_STATUS).

- Presence detect/time-out:

  In HDQ mode, the interrupt status indicates that after a read command initiated by the host, the slave did not pull the line low within the specified time. This interrupt condition is cleared by reading the interrupt status register (HDQ.HDQ_INT_STATUS).

  In HDQ mode, a time-out condition is also used to indicate the successful completion of a break pulse. That is, if the master has sent the break pulse, it is indicated with a time-out instead of a TX-complete.

Only one interrupt is generated to the MPU based on any of these interrupt conditions. A read operation on the interrupt status register clears all the interrupt status bits that were previously set.

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23.2.4.7 1-Wire Mode

23.2.4.7.1 1-Wire Mode Features

The 1-Wire mode supports the following:

- Dallas Semiconductor 1-Wire protocol
- Power-down mode
- Single-bit mode

23.2.4.7.2 Description

The 1-Wire mode requires an initialization pulse to be sent to the slave(s) connected on the interface. If a slave is present, it responds with a presence pulse.

The initialization pulse is sent when the HDQ.HDQ_CTRL_STATUS[2] INITIALIZATION bit is set and the HDQ_CTRL_STATUS[4] GO bit is set afterwards.

When the slave receives the initialization pulse, it sends back its presence pulse by pulling down the line for a defined duration. The module detects this low-level pulse and sets the HDQ.HDQ_CTRL_STATUS[3] PRESENCEDETECT bit.

In a similar way, if a presence pulse is not received from the slave after an initialization pulse is sent, the PRESENCEDETECT bit remains cleared.

Whether or not a presence pulse is detected after an initialization pulse is sent, the HDQ.HDQ_INT_STATUS[0] TIMEOUT bit is set and an interrupt condition is generated.

In 1-Wire mode, the generated interrupt condition means the maximum time allowed for receiving the response has elapsed and the software must check the PRESENCEDETECT bit to determine whether or not there was a presence pulse.

The INITIALIZATION bit is cleared at the end of the initialization pulse at the same time as the TIMEOUT bit is set. The TIMEOUT bit is cleared when the interrupt status register (HDQ.HDQ_INT_STATUS) is read.

For read operations, 1-Wire is a bit-by-bit protocol, which means the slave must be clocked by the host for each bit of the byte to read.

The line is pulled up at the end of the command/address byte. On the first read, the host creates a low-going edge to initiate a bit read. The line is then pulled up (pulled to the high-impedance state by the host and set to a high logical level by the external pullup) and the slave either drives the line low to transmit a 0, or does not drive the line to transmit a 1. This sequence is repeated for each bit to read.

The first bit the host receives is the LSB, and the last bit is the most-significant bit (MSB) in the receive data register (HDQ.HDQ_RX_DATA).

An interrupt condition indicates either a TX-complete, an RX-complete, or a time-out condition (that is, the time allowed for the slave to indicate its presence has elapsed). A read operation on the interrupt status register clears the interrupt conditions previously set. As in the HDQ mode, only one interrupt signal is sent to the MPU. Only an overall mask bit can enable or disable the interrupt (the interrupt conditions cannot be masked individually).

23.2.4.7.3 1-Wire Single-Bit Mode Operation

A single-bit mode can be entered by setting the appropriate bit in the control and status register (ONE_WIRE_SINGLE_BIT bit HDQ.HDQ_CTRL_STATUS[7]). In this mode, only one bit of data at a time is transferred between the master and the slave. After the bit is transferred, an interrupt is generated (that is, there is an RX-complete for a read operation and a TX-complete for a write operation). The ONE_WIRE_SINGLE_BIT bit is cleared by hardware after every single bit is received. Software must set this bit to re-enable reception in single-bit mode. Bit 0 of the RX register (HDQ.HDQ_RX_DATA) is updated each time a bit is received from the slave; bit 0 of the TX register (HDQ.HDQ_TX_DATA) contains the bit to be sent.

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23.2.4.7.4 Interrupt Conditions

The HDQ/1-Wire provides the following interrupt status:

- Transmission complete:

  A write operation of one byte was completed. Successful or failed completion is not indicated, because there is no acknowledgment from the slave in 1-Wire protocol. This interrupt condition is cleared by reading the interrupt status register (HDQ.HDQ_INT_STATUS).

- Read complete:

  In 1-Wire mode, the interrupt status indicates that a byte has been successfully read. This interrupt condition is cleared by reading the interrupt status register (HDQ.HDQ_INT_STATUS).

- Presence detect/time-out:

  In 1-Wire mode, the interrupt status indicates that it is now valid to check the PRESENCEDETECT bit. This interrupt condition is cleared by reading the interrupt status register (HDQ.HDQ_INT_STATUS).

Only one interrupt is generated to the MPU based on any of these interrupt conditions. A read operation on the interrupt status register clears all interrupt status bits that were previously set.

23.2.4.7.5 Status Flags

The presence-condition-detected status flag is contained in the HDQ.HDQ_CTRL_STATUS[3] PRESENCEDETECT bit. This is valid only in 1-Wire mode. The flag is updated when the HDQ.HDQ_INT_STATUS[0] TIMEOUT bit is set. Therefore, its correct value shows only after the interrupt is generated. The firmware must wait for the time-out condition; otherwise, the flag keeps its previous value and is undefined.

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23.2.5 HDQ/1-Wire Programming Models

This section describes the low-level hardware programming sequences for configuration and usage of the module. The basic protocol functions, such as slave initialization (reset), read-byte, and write-byte operations, are described. For a description of the functions, see the HDQ/1-Wire protocol documentation.

23.2.5.1 Global Initialization

23.2.5.1.1 Surrounding Modules Global Initialization

This section identifies the requirements for initializing the surrounding modules when the HDQ/1-Wire module is to be used for the first time after a device reset. This initialization of surrounding modules is based on the integration and environment of the HDQ/1-Wire. Refer to the HDQ/1-Wire Module Integration and Environment Sections for further information.

Table 23-107. Global Initialization of Surrounding Modules

Surrounding Modules	Comments
PRCM	Module interface and functional clocks must be enabled. The interface clock must not be slower than the functional clock (HDQ_ICLK ≥ HDQ_FCLK). For more information about the module configuration, see Chapter 3, *Power, Reset, and Clock Management*.
Control Module	Module specific pad muxing and pullup must be set in the control module. For more information about the module configuration, see Chapter 18, *Control Module*.
MPU INTC	MPU INTC configuration must be done to enable the interrupts from HDQ/1-Wire module. See Section 17.4.1, *Cortex-A9 MPU INTC Functional Description,* in Chapter 17, *Interrupt Controllers*.

23.2.5.1.2 HDQ/1-Wire Module Global Initialization

Table 23-108. HDQ/1-Wire Module Global Initialization

Step	Register/Bit Field/Programming Model	Value
Initiate software reset.	HDQ_SYSCONFIG[1] SOFTRESET	0x1
Disable power-down mode.	HDQ_CTRL_STATUS[5] CLOCKENABLE	0x1
Wait until reset complete?	HDQ_SYSSTATUS[0] RESETDONE	= 0x1
Disable power-down mode.	HDQ_CTRL_STATUS[5] CLOCKENABLE	0x1
Configure auto-idle mode.	HDQ_SYSCONFIG[0] AUTOIDLE	x

23.2.5.2 HDQ Operational Modes Configuration

23.2.5.2.1 Main Sequence – HDQ Write Operation Mode

Table 23-109. HDQ Mode Selection

Step	Register/Bit Field/Programming Model	Value
Select HDQ mode.	HDQ_CTRL_STATUS[0] MODE	0x0
Enable interrupt generation.	HDQ_CTRL_STATUS[6] INTERRUPTMASK	0x1
Initialize HDQ slave.	See Section 23.2.5.2.2.1	

Table 23-110. HDQ Write Operation Mode

Step	Register/Bit Field/Programming Model	Value
Write command/address or data value.	HDQ_TX_DATA[7:0]	0x–
Select write operation.	HDQ_CTRL_STATUS[1] DIR	0x0
Start operation.	HDQ_CTRL_STATUS[4] GO	0x1
Wait for interrupt.		

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Table 23-110. HDQ Write Operation Mode (continued)

Step	Register/Bit Field/Programming Model	Value
Reading HDQ_INT_STATUS clears interrupt conditions.	HDQ_INT_STATUS[2] TXCOMPLETE	0x1

23.2.5.2.2 Main Sequence - HDQ Read Operation Mode

23.2.5.2.2.1 Sub-sequence - Initialize HDQ Slave

Table 23-111. HDQ Read Operation Mode

Step	Register/Bit Field/ Programming Model	Value
Select read operation.	HDQ_CTRL_STATUS[1] DIR	0x1
Start operation.	HDQ_CTRL_STATUS[4] GO	0x1
Wait for interrupt.		
Read and store HDQ_INT_STATUS. Reading HDQ_INT_STATUS clears interrupt conditions.	HDQ_INT_STATUS	0x-
IF: Read operation successful?	HDQ_INT_STATUS[1] RXCOMPLETE HDQ_INT_STATUS[0] TIMEOUT	= 0x1 = 0x0
Get received data.	HDQ_RX_DATA[7:0]	0x-
ENDIF		

Table 23-112. Initialize HDQ Slave

Step	Register/Bit Field/Programming Model	Value
Send Initialization Pulse	HDQ_CTRL_STATUS[2] INITIALIZATION	0x1
Send Command	HDQ_CTRL_STATUS[4] GO	0x1

23.2.5.3 1-Wire Operational Modes Configuration

23.2.5.3.1 Main Sequence - 1-Wire Write Operation Mode

Table 23-113. 1-Wire Mode Selection

Step	Register/Bit Field/Programming Model	Value
Reset HDQ/1-Wire module.	See Section 23.2.5.1.2.	
Select 1-Wire mode.	HDQ_CTRL_STATUS[0] MODE	0x1
Enable interrupt generation.	HDQ_CTRL_STATUS[6] INTERRUPTMASK	0x1
Initialize 1-Wire slave, check for slave presence.	See Section 23.2.5.3.3.	

Table 23-114. 1-Wire Write Operation Mode

Step	Register/Bit Field/ Programming Model	Value
Write ID/command or data value.	HDQ_TX_DATA[7:0]	0x–
Select write operation.	HDQ_CTRL_STATUS[1] DIR	0x0
Start operation.	HDQ_CTRL_STATUS[4] GO	0x1
Wait for interrupt.		
Reading HDQ_INT_STATUS clears interrupt conditions.	HDQ_INT_STATUS[2] TXCOMPLETE	0x1

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23.2.5.3.2 Main Sequence - 1-Wire Read Operation Mode

Table 23-115. 1-Wire Read Operation Mode

Step	Register/Bit Field/Programming Model	Value
Select read operation.	HDQ_CTRL_STATUS[1] DIR	0x1
Start operation.	HDQ_CTRL_STATUS[4] GO	0x1
Wait for interrupt.		
Read and store HDQ_INT_STATUS. Reading HDQ_INT_STATUS clears interrupt conditions.	HDQ_INT_STATUS	0x–
IF: Read operation successful?	HDQ_INT_STATUS[1] RXCOMPLETE	= 0x1
Get received data.	HDQ_RX_DATA[7:0]	0x–
ENDIF		

23.2.5.3.3 Sub-sequence - Initialize 1-Wire Slave

Table 23-116. Initialize 1-Wire Slave

Step	Register/Bit Field/Programming Model	Value
Select sending initialization pulse operation.	HDQ_CTRL_STATUS[2] INITIALIZATION	0x1
Start operation.	HDQ_CTRL_STATUS[4] GO	0x1
Wait for interrupt.		
IF: Presence pulse detected?	HDQ_INT_STATUS[0] TIMEOUT HDQ_CTRL_STATUS[3] PRESENCEDETECT	= 0x1 = 0x1
Slave is present and initialized.		
ELSE		
Repeat initialization subsequence.		
ENDIF		

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23.2.6 HDQ/1-Wire Register Manual

23.2.6.1 HDQ/1-Wire Instance Summary

Table 23-117. HDQ/1-Wire Instance Summary

Module Name	Base Address	Size
HDQ/1-Wire	0x480B 2000	4KB

23.2.6.2 HDQ/1-Wire Registers

CAUTION

The following rules must be observed when accessing the module registers:

- A read from the HDQ_INT_STATUS register or the HDQ_RX_DATA register is not allowed unless the processor has been interrupted by the module.
- After the release of the GO bit in the HDQ_CTRL_STATUS register, no access to the HDQ_TX_DATA or HDQ_CTRL_STATUS register is allowed until the processor has been interrupted by the module.
- Polling of the HDQ_INT_STATUS register by software to determine whether an interrupt was generated is not allowed.

CAUTION

The HDQ/1-Wire registers are limited to 32-bit data accesses; 16-bit and 8-bit data accesses are not allowed and can corrupt register content.

23.2.6.2.1 HDQ/1-Wire Register Summary

Table 23-118. HDQ/1-Wire Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	HDQ/1-Wire L4 Base Address
HDQ_REVISION	R	32	0x0000 0000	0x480B 2000
HDQ_TX_DATA	RW	32	0x0000 0004	0x480B 2004
HDQ_RX_DATA	R	32	0x0000 0008	0x480B 2008
HDQ_CTRL_STATUS	RW	32	0x0000 000C	0x480B 200C
HDQ_INT_STATUS	R	32	0x0000 0010	0x480B 2010
HDQ_SYSCONFIG	RW	32	0x0000 0014	0x480B 2014
HDQ_SYSSTATUS	R	32	0x0000 0018	0x480B 2018

23.2.6.2.2 HDQ/1-Wire Register Description

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Table 23-119. HDQ_REVISION

Address Offset	0x0000 0000		
Physical Address	0x480B 2000	**Instance**	HDQ/1-Wire
Description	This register contains the IP revision code		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								REV							

Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP revision	R	TI internal data

Table 23-120. Register Call Summary for Register HDQ_REVISION

HDQ/1-Wire

- HDQ/1-Wire Register Summary: [0]

Table 23-121. HDQ_TX_DATA

Address Offset	0x0000 0004		
Physical Address	0x480B 2004	**Instance**	HDQ/1-Wire
Description	This register contains the data to be transmitted.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								TX_DATA							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Reads returns 0	R	0x000000
7:0	TX_DATA	Transmit data (used in both HDQ and 1-Wire modes)	RW	0x00

Table 23-122. Register Call Summary for Register HDQ_TX_DATA

HDQ/1-Wire

- HDQ Protocol Initialization (Default): [0]
- 1-Wire Single-Bit Mode Operation: [1]
- Main Sequence – HDQ Write Operation Mode: [2]
- Main Sequence - 1-Wire Write Operation Mode: [3]
- HDQ/1-Wire Registers: [4]
- HDQ/1-Wire Register Summary: [5]

Table 23-123. HDQ_RX_DATA

Address Offset	0x0000 0008		
Physical Address	0x480B 2008	**Instance**	HDQ/1-Wire
Description	This register contains the data to be received.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RX_DATA							

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Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Reads returns 0	R	0x000000
7:0	RX_DATA	Receive data (used in both HDQ and 1-Wire modes)	R	0x00

Table 23-124. Register Call Summary for Register HDQ_RX_DATA

HDQ/1-Wire

- Description: [0]
- 1-Wire Single-Bit Mode Operation: [1]
- Main Sequence - HDQ Read Operation Mode: [2]
- Main Sequence - 1-Wire Read Operation Mode: [3]
- HDQ/1-Wire Registers: [4]
- HDQ/1-Wire Register Summary: [5]

Table 23-125. HDQ_CTRL_STATUS

Address Offset	0x0000 000C		
Physical Address	0x480B 200C	**Instance**	HDQ/1-Wire
Description	This register provides status information about the module.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								ONE_WIRE_SINGLE_BIT	INTERRUPTMASK	CLOCKENABLE	GO	PRESENCEDETECT	INITIALIZATION	DIR	MODE

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Reads returns 0	RW	0x000000
7	ONE_WIRE_SINGLE_BIT	Single-bit mode for 1-Wire 0x0: Disabled 0x1: Enabled	RW	0
6	INTERRUPTMASK	Interrupt masking bit 0x0: Interrupts disable 0x1: Interrupts enable	RW	0
5	CLOCKENABLE	Power-down mode bit 0x0: Clock disable (power down) 0x1: Clock enable	RW	0
4	GO	Go bit. Write 1 to start the appropriate operation. Bit returns to 0 after the operation is complete.	RW	0
3	PRESENCEDETECT	Slave presence indicator. Actual only just after initialization time-out. Used in 1-Wire mode. Read-only flag. 0x0: No slave detected 0x1: Slave detected	R	0
2	INITIALIZATION	Write 1 to send initialization pulse. Bit returns to 0 after pulse is sent.	RW	0
1	DIR	DIR bit, determines if next command is read or write 0x0: Write 0x1: Read	RW	0
0	MODE	Mode selection bit 0x0: HDQ mode 0x1: 1-Wire mode	RW	0

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Table 23-126. Register Call Summary for Register HDQ_CTRL_STATUS

HDQ/1-Wire

- HDQ Protocol Initialization (Default): [0] [1]
- HDQ/1-Wire Block Diagram: [2]
- HDQ/1-Wire Hardware and Software Reset: [3]
- HDQ/1-Wire Power Management: [4]
- Power-Down Mode: [5]
- HDQ Interrupt Requests: [6] [7] [8]
- Description: [9] [10]
- Single-Bit Mode: [11]
- Description: [12] [13] [14]
- 1-Wire Single-Bit Mode Operation: [15]
- Status Flags: [16]
- HDQ/1-Wire Module Global Initialization: [17] [18]
- Main Sequence – HDQ Write Operation Mode: [19] [20] [21] [22]
- Main Sequence - HDQ Read Operation Mode: [23] [24] [25] [26]
- Main Sequence - 1-Wire Write Operation Mode: [27] [28] [29] [30]
- Main Sequence - 1-Wire Read Operation Mode: [31] [32]
- Sub-sequence - Initialize 1-Wire Slave: [33] [34] [35]
- HDQ/1-Wire Registers: [36] [37]
- HDQ/1-Wire Register Summary: [38]

Table 23-127. HDQ_INT_STATUS

Address Offset	0x0000 0010		
Physical Address	0x480B 2010	**Instance**	HDQ/1-Wire
Description	This register controls interrupts status		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													TXCOMPLETE	RXCOMPLETE	TIMEOUT

Bits	Field Name	Description	Type	Reset
31:3	RESERVED	Reads returns 0	R	0x0000 0000
2	TXCOMPLETE	TX-complete interrupt flag. Set to 1 if cause of interrupt. Set to 0 when register read.	R	0
1	RXCOMPLETE	Read-complete interrupt flag. Set to 1 if cause of interrupt. Set to 0 when register read.	R	0
0	TIMEOUT	Presence detect/timeout interrupt flag. In 1-Wire mode, set to 1 if slave's presence detected. In HDQ mode, set to 1 if timeout on read occurs. Set to 0 when register read.	R	0

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Table 23-128. Register Call Summary for Register HDQ_INT_STATUS

HDQ/1-Wire

- HDQ Interrupt Requests: [0] [1] [2]
- Description: [3] [4] [5]
- Interrupt Conditions: [6] [7] [8]
- Description: [9] [10]
- Interrupt Conditions: [11] [12] [13]
- Status Flags: [14]
- Main Sequence – HDQ Write Operation Mode: [15] [16]
- Main Sequence - HDQ Read Operation Mode: [17] [18] [19] [20] [21]
- Main Sequence - 1-Wire Write Operation Mode: [22] [23]
- Main Sequence - 1-Wire Read Operation Mode: [24] [25] [26] [27]
- Sub-sequence - Initialize 1-Wire Slave: [28]
- HDQ/1-Wire Registers: [29] [30]
- HDQ/1-Wire Register Summary: [31]

Table 23-129. HDQ_SYSCONFIG

Address Offset	0x0000 0014		
Physical Address	0x480B 2014	**Instance**	HDQ/1-Wire
Description	This register controls various bits		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														SOFTRESET	AUTOIDLE

Bits	Field Name	Description	Type	Reset
31:2	RESERVED	Reads returns 0	RW	0x0000 0000
1	SOFTRESET	Start soft reset sequence. 0x0: Disabled 0x1: Enabled	RW	0
0	AUTOIDLE	Interconnect idle. 0x0: Module clock is free-running. 0x1: Module is in power saving mode: Clock is running only when module is accessed or inside logic is in function to process events.	RW	0

Table 23-130. Register Call Summary for Register HDQ_SYSCONFIG

HDQ/1-Wire

- HDQ/1-Wire Hardware and Software Reset: [0]
- HDQ/1-Wire Power Management: [1]
- Auto-Idle Mode: [2]
- HDQ/1-Wire Module Global Initialization: [3] [4]
- HDQ/1-Wire Register Summary: [5]

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Table 23-131. HDQ_SYSSTATUS

Address Offset	0x0000 0018		
Physical Address	0x480B 2018	**Instance**	HDQ/1-Wire
Description	This register monitors the reset sequence.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															RESETDONE

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reads returns 0	R	0x0000 0000
0	RESETDONE	Reset monitoring. 0x0: The module is currently performing its reset. When the module is in power-down mode, set to 0 to indicate this fact. 0x1: The module has finished its reset.	R	1

Table 23-132. Register Call Summary for Register HDQ_SYSSTATUS

HDQ/1-Wire

- HDQ/1-Wire Module Global Initialization: [0]
- HDQ/1-Wire Register Summary: [1]

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23.3 UART/IrDA/CIR

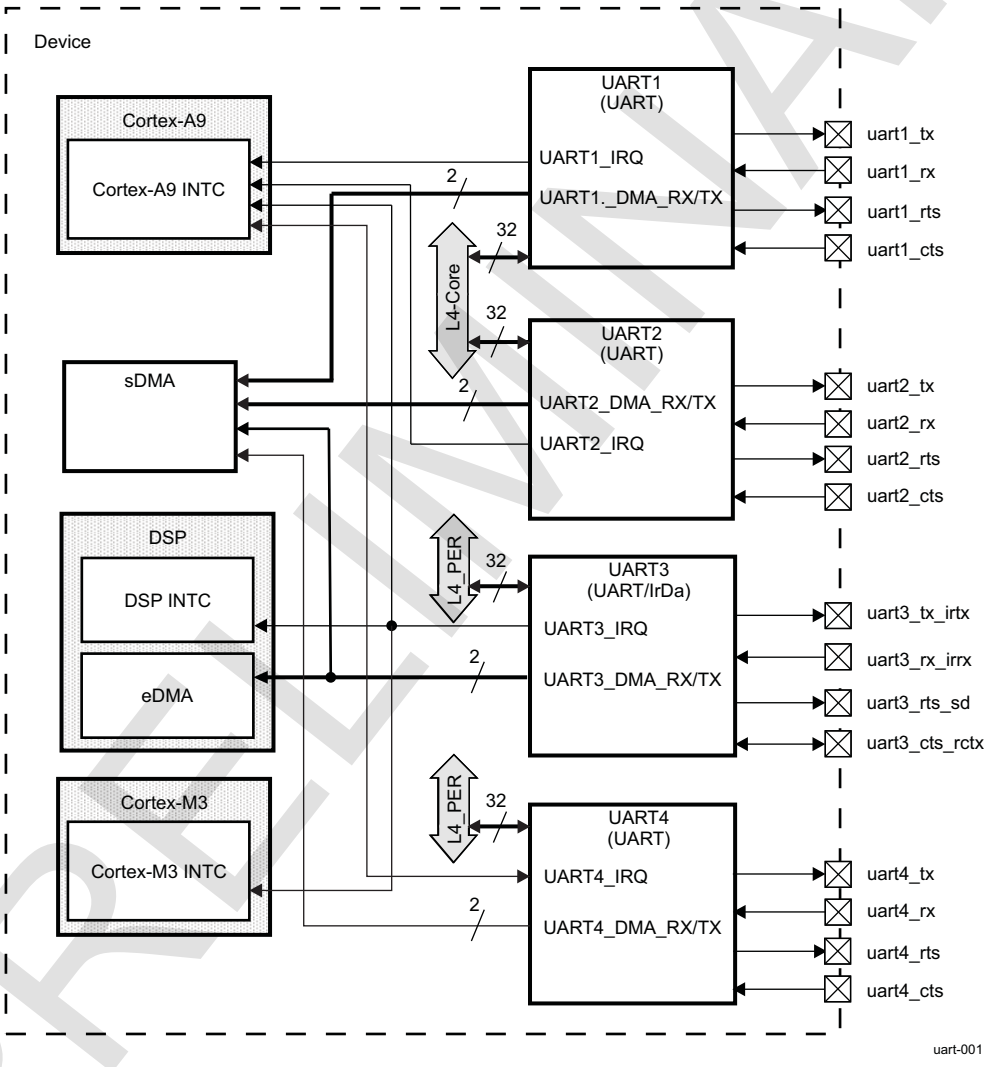
This chapter describes the function, operation, and configuration of the universal asynchronous receiver/transmitter (UART)/infrared data association (IrDA)/consumer infrared (CIR) module in the device.

23.3.1 UART/IrDA/CIR Overview

The device contains four UART devices controlled by the MPU (see Figure 23-51):

- Three UART-only modules (UART1, UART2, and UART4) are pinned out for use as UART devices only.
- UART3, which adds infrared communication support, is pinned out for use as a UART, IrDA, or CIR device, and can be programmed to any available operating mode.

Figure 23-51. UART Module



23.3.1.1 UART Features

The UARTs (UART1, UART2, UART3 when in UART mode, and UART4) include the following key features:

- 16C750 compatibility
- 64-byte FIFO buffer for receiver and 64-byte FIFO for transmitter
- Programmable interrupt trigger levels for FIFOs

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- Baud generation based on programmable divisors N (N = 1...16,384) operating from a fixed functional clock of 48 MHz

Oversampling is programmed by software as 16 or 13; thus, the baud rate computation is one of two options:

- Baud rate = (functional clock/16)/N
- Baud rate = (functional clock/13)/N

This software programming mode enables higher baud rates with the same error amount without changing the clock source:

- Break character detection and generation
- Configurable data format:
  - Data bit: 5, 6, 7, or 8 bits
  - Parity bit: Even, odd, none
  - Stop-bit: 1, 1.5, 2 bit(s)
- Flow control: Hardware (RTS/CTS) or software (XON/XOFF)

The UART clocks are connected to produce a baud rate of up to 3.6 Mbps. Table 23-133 lists the supported baud rates, the requested divisor, and the corresponding error versus the standard baud rate.

Table 23-133. UART Mode Baud Rates, Divisor Values, and Error Rates

Baud Rate	Oversampling	Divisor	Error (%)
300	16	10,000	0
600	16	5000	0
1200	16	2500	0
2400	16	1250	0
4800	16	625	0
9600	16	312	0.16
14,400	16	208	0.16
19,200	16	156	0.16
28,800	16	704	0.16
38,400	16	78	0.16
57,600	16	52	0.16
115,200	16	26	0.16
230,400	16	13	0.16
460,800	13	8	0.16
921,600	13	4	0.16
1,843,200	13	2	0.16
3,000,000	16	1	0
3,686,400	13	1	0.16

23.3.1.2 IrDA Features

The IrDA (UART3 only) includes the following key features:

- Support of IrDA 1.4 slow infrared (SIR), medium infrared (MIR), and fast infrared (FIR) communications:
  - Frame formatting: Addition of variable beginning-of-frame (xBOF) characters and end-of-frame (EOF) characters
  - Uplink/downlink cyclic redundancy check (CRC) generation/detection
  - Asynchronous transparency (automatic insertion of break character)
  - Eight-entry status FIFO (with selectable trigger levels) to monitor frame length and frame errors
  - Framing error, CRC error, illegal symbol (FIR), and abort pattern (SIR, MIR) detection

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Table 23-134 lists the supported baud rates, the requested divisor, and the corresponding error versus the standard baud rate.

Table 23-134. UART IrDA Mode Baud Rates, Divisor Values, and Error Rates

Baud Rate	IR Mode	Encoding	Divisor	Error (%)
2400	SIR	3/16	1250	0
9600	SIR	3/16	312	0.16
19,200	SIR	3/16	156	0.16
38,400	SIR	3/16	78	0.16
57,600	SIR	3/16	52	0.16
115,200	SIR	3/16	26	0.16
576,000	MIR	1/4	2	0
1,152,000	MIR	1/4	1	0
4,000,000	FIR	4 PPM(1)	1	0

(1) PPM = pulse-position modulation

23.3.1.3 CIR Features

The CIR mode uses a variable pulse-width modulation (PWM) technique (based on multiples of a programmable *t* period) to encompass the various formats of infrared encoding for remote-control applications. The CIR logic transmits data packets based on a user-definable frame structure and packet content.

The CIR (UART3 only) includes the following key features to provide CIR support for remote-control applications:

- Transmit mode only (Receive mode is not supported.)
- Free data format (supports any remote-control private standards)
- Selectable bit rate
- Configurable carrier frequency
- 1/2, 5/12, 1/3, or 1/4 carrier duty cycle

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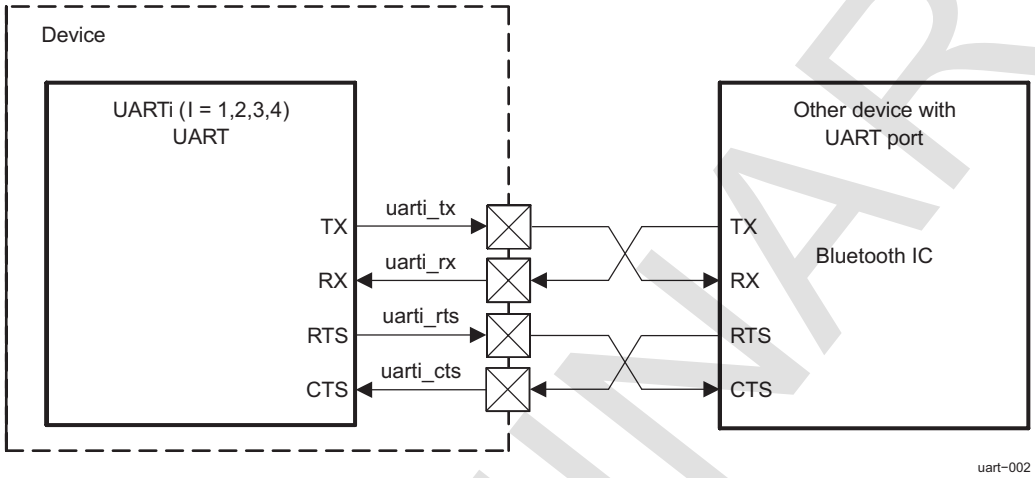
23.3.2 UART/IrDA/CIR Environment

This section describes the UART/IrDA/CIR connection with an external device.

23.3.2.1 System Using UART Communication With Hardware Handshake

Each UART instance can be easily connected to the UART port of an external IC (see Figure 23-52).

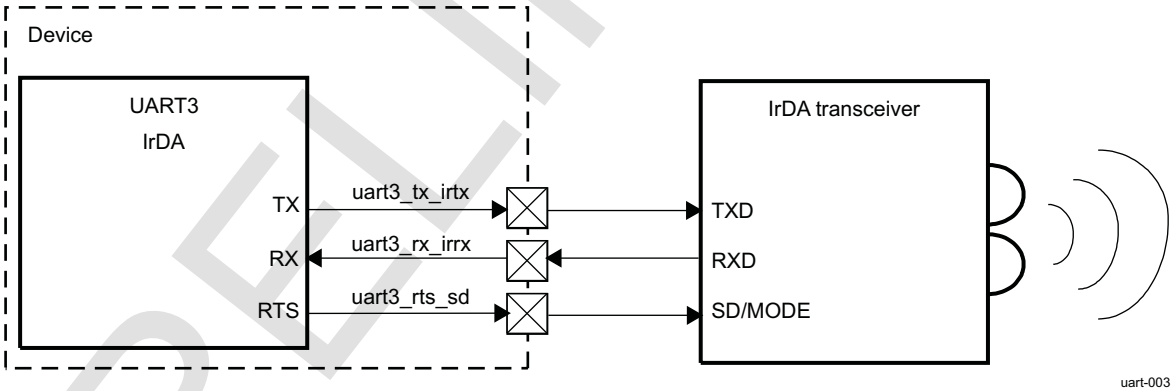
Figure 23-52. UART Mode Bus System Overview



23.3.2.2 System Using IrDA Communication Protocol

As Figure 23-53 shows, UART3 can be connected to an external infrared transceiver in the IrDA modes (FIR, SIR, and MIR).

Figure 23-53. IrDA System Overview



23.3.2.3 System Using CIR Communication Protocol With Remote Control

UART3 can be connected to an external infrared transceiver in CIR mode (see Figure 23-54).

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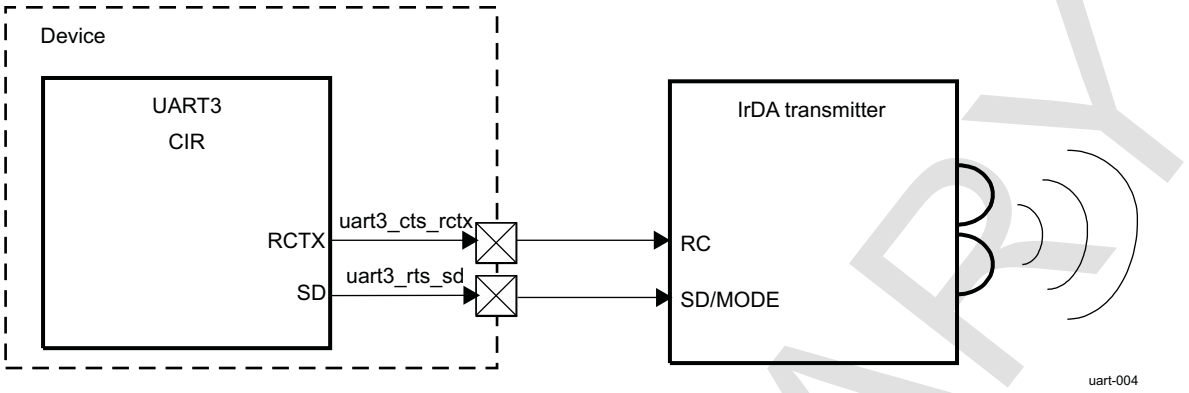
Figure 23-54. CIR System Overview



23.3.2.4 UART Interface

23.3.2.4.1 Description

Table 23-135 lists the UART interface input/output (I/O) signals.

Table 23-135. UART I/O Pins

Signal	I/O [1]	Description	Reset
UART Modem Signals			
uarti_rx	I	Serial data input	Unknown
uarti_tx	O	Serial data output Because this pin is active high in IrDA mode and the output is muxed, this pin is set to low on reset (when the UARTi.UART_MDR1[2:0] bit field is set to 0x7) and takes the defined inactive level of that signal corresponding to when and how the UARTi.UART_MDR1 register is programmed; that is, the output is 1 (inactive for UART modem modes) and 0 (inactive for IrDA modes).	1
uarti_cts	I	Clear to send Active-low modem status signal. Reading the UARTi.UART_MSR[4] NCTS_STS bit checks the condition of uarti_cts. Reading the UARTi.UART_MSR[0] CTS_STS bit checks a change of state of uarti_cts since the last read of the modem status register. The auto-nCTS mode uses uarti_cts to control the transmitter.	Unknown
uarti_rts	O	Request to send When active (low), the module is ready to receive data. Setting the UARTi.UART_MCR[1] RTS bit activates uarti_rts, which becomes inactive as the result of a module reset, loopback mode, or clearing the UARTi.UART_MCR[1] RTS bit. In auto-RTS mode, uarti_rts becomes inactive as a result of the receiver threshold logic.	1

(1) I = Input; O = Output

23.3.2.4.2 UART Protocol and Data Format

The UART device operates in three modes:

- UART 16x (= 230.4 kbps)
- UART 16x with autobauding (= 1200 bps and = 115.2 kbps)
- UART 13x (= 460.8 kbps)

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CAUTION

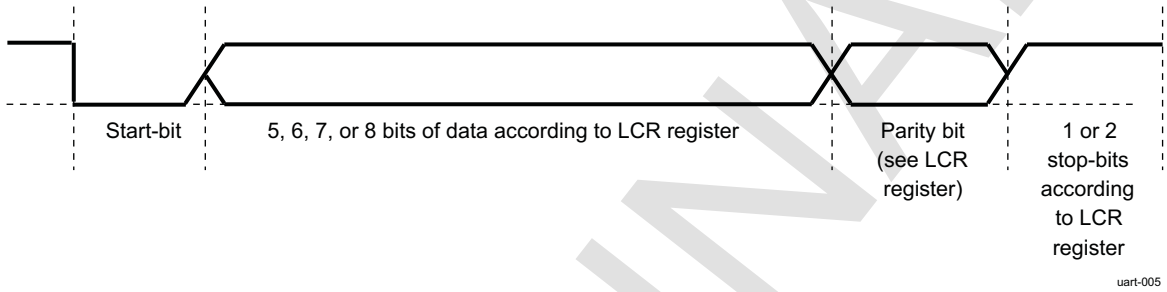
To be used as a UART, the operating mode must be programmed appropriately in the UARTi.UART_MDR1[2:0] MODE_SELECT bit field to select UART, IrDA, or CIR mode.

The UART uses a wired interface for serial communication with a remote device.

The UART is functionally compatible with the TL16C750 UART and earlier designs such as the TL16C550.

Figure 23-55 shows the UART frame data format.

Figure 23-55. UART Frame Data Format



23.3.2.5 IrDA Functional Interfaces

23.3.2.5.1 UART3 Interface Description

Table 23-136 lists the UART3 interface I/O signals.

Table 23-136. UART3 I/O Signals

Signal	I/O [1]	Description	Reset
IrDA Signals			
uart3_rx_irrx	I	Serial data input	Unknown
uart3_tx_irtx	O	Serial data output in IrDA modes (SIR, MIR, and FIR). In other modes, this pin is set to the reset value (inactive state).	0
uart3_rts_sd	O	SD mode is used to configure the transceivers. The SD pinout is an inverted value of the UART3.UART_ACREG[6] SD_MOD bit.	1

(1) I = Input; O = Output

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23.3.2.5.2 IrDA Protocol and Data Format

23.3.2.5.2.1 SIR Mode

In SIR mode, data is transferred between the MPU and peripheral devices at speeds of up to 115,200 baud. A SIR transmit frame begins with start flags (a single 0xC0, a multiple 0xC0, or a single 0xC0 preceded by a number of 0xFF flags), is followed by frame data and a CRC-16, and ends with a stop flag (0xC1).

The bit format for a single word uses 1 start-bit, 8 data bits, and 1 stop-bit, and is unaffected by the use and settings of the UART3.UART_LCR register.

The UART3.UART_BLR[6] XBOF_TYPE bit selects whether the 0xC0 or 0xFF start patterns are used when multiple start flags are required.

The SIR transmit state-machine attaches start flags, CRC-16, and stop flags, and checks the outgoing data to establish whether data transparency is required.

SIR transparency is carried out if the outgoing data between the start and stop flags contains 0xC0, 0xC1, or 0x7D. If one of these start flags is about to be transmitted, the SIR state-machine first sends an escape character (0x7D), then inverts the fifth bit of the real data to be sent and sends this data immediately after the 0x7D character.

The SIR receive state-machine recovers the receive clock, removes the start flags and any transparency from the incoming data, and determines the frame boundary with reception of the stop flag. The SIR state-machine also checks for errors such as a frame abort (0x7D character followed immediately by a 0xC1 stop flag without transparency), a CRC error, or a frame-length error. At the end of a frame reception, the MPU reads the line status register (UART3.UART_LSR) to find possible errors of the received frame.

NOTE: The module can transmit and receive data, but when the device is transmitting, the IR RX circuitry is automatically disabled by hardware. See the description of the UART3.UART_ACREG[5] DIS_IR_RX bit. This applies to all three modes: SIR, MIR, and FIR.

Infrared output in SIR mode can be 1.6-µs or 3/16 encoding, selected by the UART3.UART_ACREG[7] PULSE_TYPE bit. In 1.6-µs encoding, the infrared pulse width is 1.6 µs; and in 3/16th encoding, the infrared pulse width is 3/16th of a bit duration (1/baud rate).

For back-to-back frames, the transmitting device must send at least two start flags at the start of each frame.

NOTE: Reception supports variable-length stop-bits.

23.3.2.5.2.1.1 Frame Format

Figure 23-56 shows the IrDA SIR frame format.

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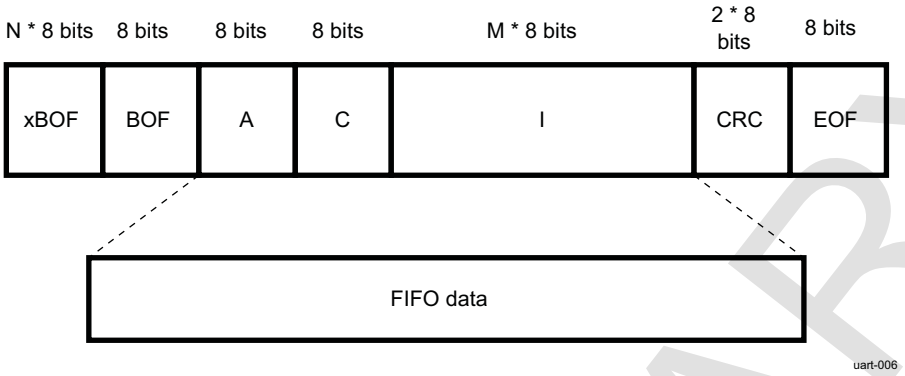
Figure 23-56. IrDA SIR Frame Format



The CRC is applied on the address (A), control (C), and information (I) bytes.

NOTE: The two words of CRC are written to the FIFO in reception.

23.3.2.5.2.1.2 Asynchronous Transparency

Before transmitting a byte, the UART IrDA controller examines each byte of the payload and the CRC field (between BOF and EOF). For each byte equal to 0xC0 (BOF), 0xC1 (EOF), or 0x7D (control escape), the controller performs certain tasks:

- In transmission:
  - Inserts a control escape (CE) byte preceding the byte
  - Complements bit 5 of the byte (that is, exclusive ORs the byte with 0x20)

  The byte sent for the CRC computation is the initial byte written in the TX FIFO (before the XOR with 0x20).
- In reception:

  For the A, C, I, CRC field:
  - Compares the byte with the CE byte; if they are not equal, sends the byte to the CRC detector and stores it in the RX FIFO.
  - If the byte is equal to the CE byte, discards the CE byte
  - Complements bit 5 of the byte following the CE
  - Sends the complemented byte to the CRC detector and stores it in the RX FIFO

23.3.2.5.2.1.3 Abort Sequence

The transmitter can prematurely close a frame (abort) by sending the sequence 0x7DC1. The abort pattern closes the frame without a CRC field or an ending flag.

When a 0x7D character that is followed immediately by a 0xC1 character is received without transparency, the receiver treats the frame as an aborted frame.

23.3.2.5.2.1.4 Pulse Shaping

The SIR mode supports the 3/16 and the 1.6-us pulse duration methods in receive and transmit. The UART3.UART_ACREG[7] PULSE_TYPE bit selects the pulse-width method in transmit mode.

23.3.2.5.2.1.5 Encoder

Serial data from the transmit state-machine are encoded to transmit data to the optoelectronics. While the TX FIFO output is high, the uart3_tx_irtx line is always low, and the counter used to form a pulse on uart3_tx_irtx is cleared continuously.

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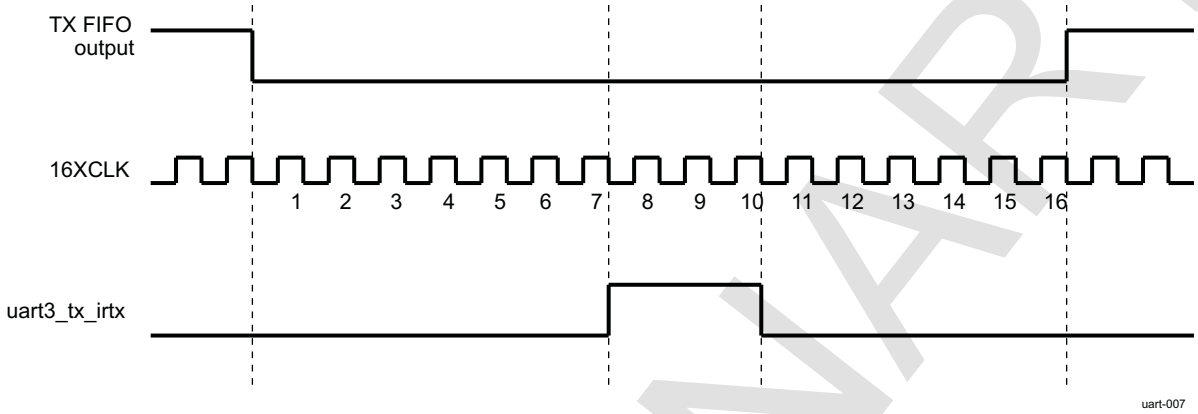
After the TX FIFO output resets to 0, uart3_tx_irtx rises on the falling edge of the seventh 16XCLK. On the falling edge of the tenth 16XCLK pulse, uart3_tx_irtx falls, creating a 3-clock-wide pulse. While the TX FIFO output stays low, a pulse is transmitted during the seventh to the tenth clock of each 16-clock bit cycle.

Figure 23-57 shows the IrDA SIR encoding mechanism.

Figure 23-57. IrDA SIR Encoding Mechanism

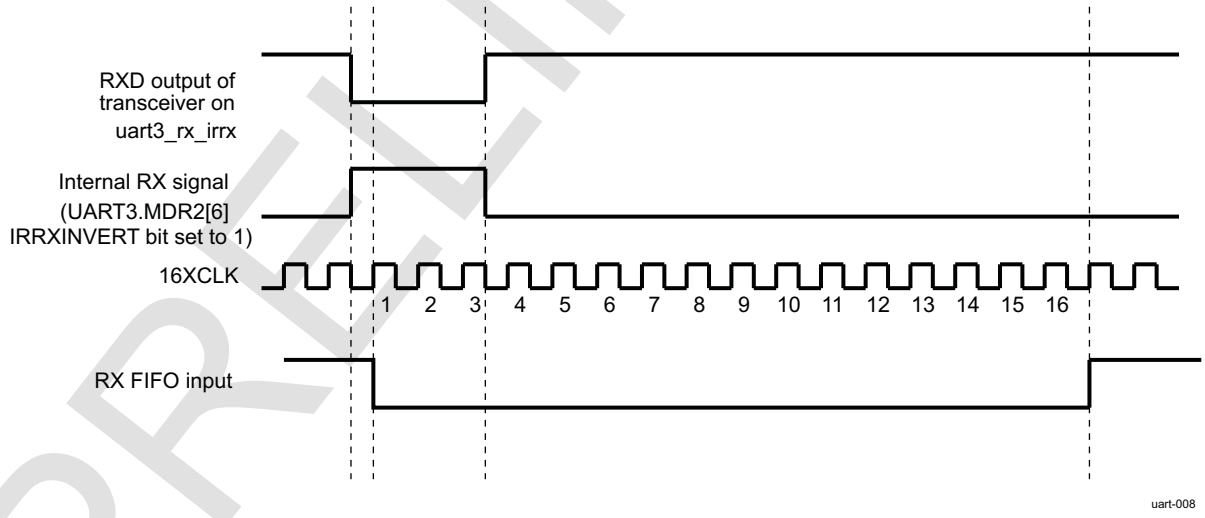


23.3.2.5.2.1.6 Decoder

After reset, the RX FIFO input is high and the 4-bit counter is cleared. When a rising edge is detected on RX, the RX FIFO input falls on the next rising edge of 16XCLK with sufficient setup time. The RX FIFO input stays low for 16 cycles (16XCLK) and then returns to high as required by the IrDA specification. As long as no pulses (rising edges) are detected on the RX, the RX FIFO input remains high.

Figure 23-58 shows the IrDA SIR decoding mechanism.

Figure 23-58. IrDA SIR Decoding Mechanism



The module can transmit and receive data, but when the device is transmitting, the IR RX circuitry is automatically disabled by hardware. The operation of the uart3_rx_irrx input can be disabled using the UART3.UART_ACREG[5] DIS_IR_RX bit. The UART3.UART_MDR2[6] IRRXINVERT bit can invert the signal from the transceiver (RXD) pin to the IR RX logic in the UART. This inversion is performed by default.

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23.3.2.5.2.1.7 IR Address Checking

In all IR modes, when address checking is enabled by setting the UART_EFR[1:0] bit field (see Table 23-137), only frames intended for the device are written to the RX FIFO. This is to avoid receiving frames not meant for this device in a multipoint infrared environment. To program two frame addresses that the UART3 receives in IrDA mode, use the UART3.UART_XON1_ADDR1[7:0] and UART3.UART_XON2_ADDR2[7:0] bit fields.

Table 23-137. UART_EFR[1:0] IR Address Checking Options

UART_EFR[1]	UART_EFR[0]	IR Address Checking
0	0	All address-checking operations disabled
0	1	Only address 1 checking enabled
1	0	Only address 2 checking enabled
1	1	All address-checking operations enabled

23.3.2.5.2.2 SIR Free-Format Mode

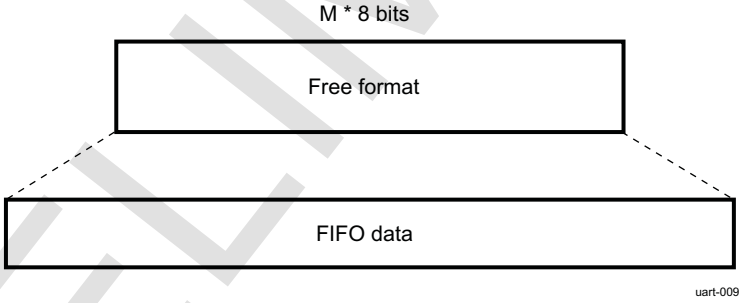
To allow complete software flexibility when transmitting and receiving infrared data packets, the SIR free-format (FF) mode is a subfunction of the existing SIR mode. In FF mode, all frames going to and from the FIFO buffers are untouched with respect to appending and removing control characters and CRC values.

The FF mode corresponds to a UART mode with a pulse modulation of 3/16 of baud rate pulse width.

For example, a normal SIR packet has BOF control and CRC error-checking data appended (transmitting) or removed (receiving) from the data going to and from the FIFOs.

Figure 23-59 shows SIR FF mode.

Figure 23-59. SIR FF Mode



In SIR FF mode, the MPU software must construct (that is, encode and decode) the entire FIFO data packet.

23.3.2.5.2.3 MIR Mode

In MIR mode, data is transferred between the MPU and the peripheral devices at 0.576 or 1.152 Mbps speed. A MIR transmit frame starts with at least two start flags followed by a frame data and a CRC-16, and ends with a stop flag (see Figure 23-60).

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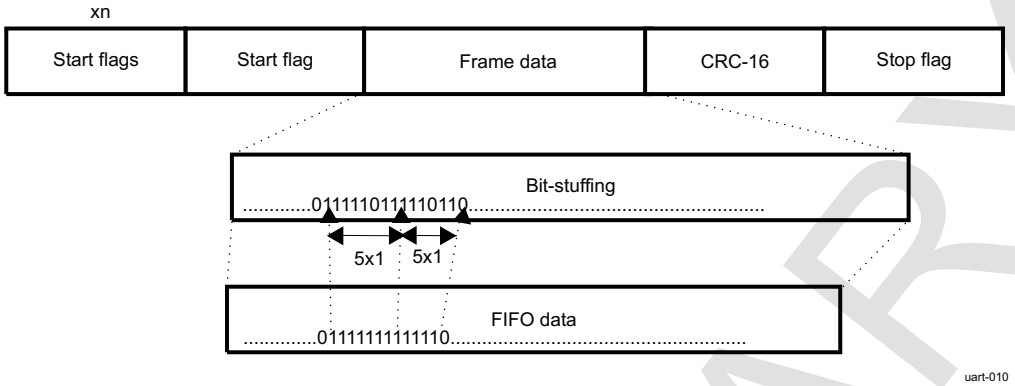
Figure 23-60. MIR Transmit Frame Format



On transmit, the MIR state-machine attaches start flags, a CRC-16, and stop flags, as in SIR mode. All fields are transmitted LSB of each byte first.

In MIR mode:

- The state-machine looks for consecutive 1s in the frame data and automatically inserts 0 after five consecutive 1s (this is called bit-stuffing).
- 0x7E is used for start and stop flags (unambiguously, not data, because of bit-stuffing).
- An abort sequence requires a minimum of seven consecutive 1s (unambiguously, not data, because of bit-stuffing).
- Back-to-back frames are allowed with three or more stop flags between them. If two consecutive frames are not back to back, the gap between the last stop flag of the first frame and the start flag of the second frame must be separated by at least seven bit durations.

On receive, the MIR receive state-machine recovers the receive clock, removes the start flags, destuffs the incoming data, and determines the frame boundary with reception of the stop flag. The state-machine also checks for errors such as frame abort, CRC error, and frame-length error. At the end of a frame reception, the MPU reads the line status register (UART3.UART_LSR) to detect errors of the received frame.

The module can transmit and receive data, but when the device is transmitting, the IR RX circuitry is automatically disabled by hardware.

23.3.2.5.2.3.1 MIR Encoder/Decoder

To meet the MIR baud rate tolerance of 0.1 percent with a 48-MHz clock input, a 42-41-42 encoding/decoding adjustment is performed. The reference start point is the first start flag, and the 42-41-42 cyclic pattern is repeated until the stop flag is sent or detected.

The jitter created this way is within MIR tolerances. The pulse width is not exactly 1/4, but it is within the tolerances defined by IrDA specifications.

Figure 23-61 shows the MIR baud rate adjustment mechanism.

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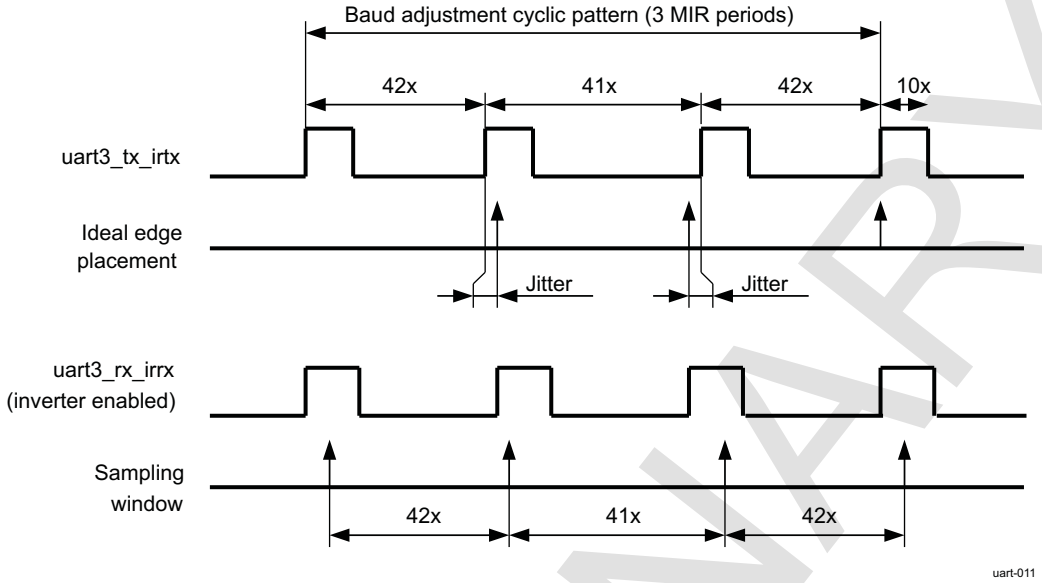
Figure 23-61. MIR Baud Rate Adjustment Mechanism

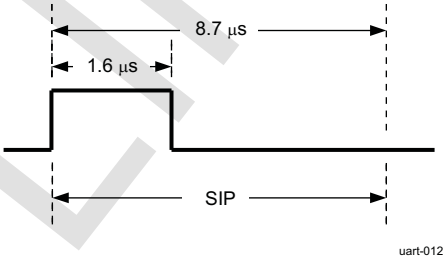


23.3.2.5.2.3.2 SIP Generation

In the MIR and FIR operation modes, the transmitter must send a serial infrared interaction pulse (SIP) at least once every 500 ms. The SIP informs slow devices (operating in SIR mode) that the medium is occupied.

Figure 23-62 shows the SIP.

Figure 23-62. SIP



23.3.2.5.2.4 FIR Mode

In FIR mode, data is transferred between the MPU and the peripheral devices at 4 Mbps. A FIR transmit frame starts with a preamble that is followed by a start flag, frame data, CRC-32, and ends with a stop flag.

Figure 23-63 shows the FIR transmit frame format.

Figure 23-63. FIR Transmit Frame Format

Preamble (16x)	Start flag	Frame data	CRC-32	Stop flag

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On transmit, the FIR transmit state-machine attaches the preamble, start flag, CRC-32, and stop flag. An abort sequence requires at least two transmissions of 0000. Back-to-back frames are allowed, but each frame must be complete.

The state-machine also encodes the transmit data into 4-PPM format (see Table 23-138) and generates the SIP (see Section 23.3.2.5.2.3.2, *SIP Generation*).

Table 23-138. 4-PPM Format

Data Bit Pair (Bin)	4-PPM Data Symbol (Bin)
00	1000
01	0100
10	0010
11	0001

The four symbols described in Table 23-138 are the legal, encoded data symbols. All other combinations are illegal for encoding data. Some of these illegal symbols are used in the definition of the preamble, start flag, and stop flag because they are unambiguously not data (see Table 23-139).

Table 23-139. FIR Preamble, Start Flag, and Stop Flag

Frame Part	Transmitted Frame (Bin)
Preamble	1000 0000 1010 1000 (16 repeated transmissions)
Start flag	0000 1100 0000 1100 0110 0000 0110 0000
Stop flag	0000 1100 0000 1100 0000 0110 0000 0110

All fields are transmitted the LSBs of each byte first (see Table 23-140).

Table 23-140. FIR Data Byte Transmission Order Example

Data Byte (Hex)	Data Byte Pair (Bin)	4-PPM Data Symbol (Bin)	Transmission Order
0x0B	00	1000	4
	00	1000	3
	10	0010	2
	11	0001	1

On receive, the FIR receive state-machine recovers the receive clock, removes the preamble and the start flag, decodes the 4-PPM incoming data, and determines the frame boundary with reception of the stop flag. The state-machine also checks for errors such as illegal symbol, CRC error, and frame-length error. At the end of a frame reception, the MPU reads the line status register (UART3.UART_LSR) to detect errors of the received frame.

The module can transmit and receive data, but when the device is transmitting, the IR RX circuitry is automatically disabled by hardware.

23.3.2.6 CIR Functional Interfaces

23.3.2.6.1 CIR Interface Description

Table 23-141 lists the CIR interface I/O signals.

Table 23-141. CIR I/O Signals

Signal	I/O [1]	Description	Reset
CIR Signals			
uart3_rx_irrx	I	Serial data input	Unknown
uart3_cts_rctx	O	Serial data output in CIR mode. In other modes, this pin is set to the reset value (inactive state).	0

(1) I = Input; O = Output

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Table 23-141. CIR I/O Signals (continued)

Signal	I/O [1]	Description	Reset
uart3_rts_sd	O	SD mode is used to configure the transceivers. The SD pinout is an inverted value of the UART3.UART_ACREG[6] SD_MOD bit.	1

23.3.2.6.2 CIR Protocol and Data Format

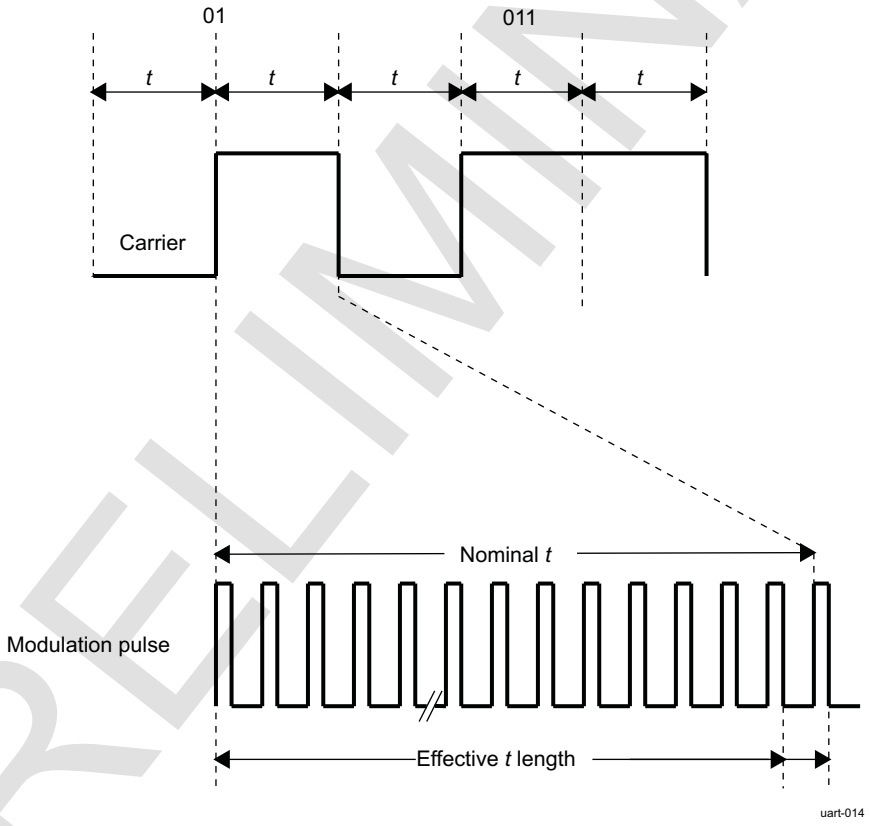
In CIR mode, the infrared operation functions as a programmable (universal) remote control.

CIR mode uses a variable PWM technique (based on multiples of a programmable *t* period) to encompass the various formats of infrared encoding for remote-control applications. The CIR logic transmits data packets based on user-defined frame structure and packet content.

23.3.2.6.2.1 Carrier Modulation

Each modulated pulse that constitutes a digit is a train of on/off pulses (see Figure 23-64).

Figure 23-64. CIR Pulse Modulation



23.3.2.6.2.2 Pulse Duty Cycle

The programmer can choose one of four duty cycles for modulation pulses by setting the appropriate value in the UART3.UART_MDR2[5:4] CIR_PULSE_MODE bit field (1/4, 1/3, 5/12, or 1/2).

Figure 23-65 shows the CIR modulation duty cycles.

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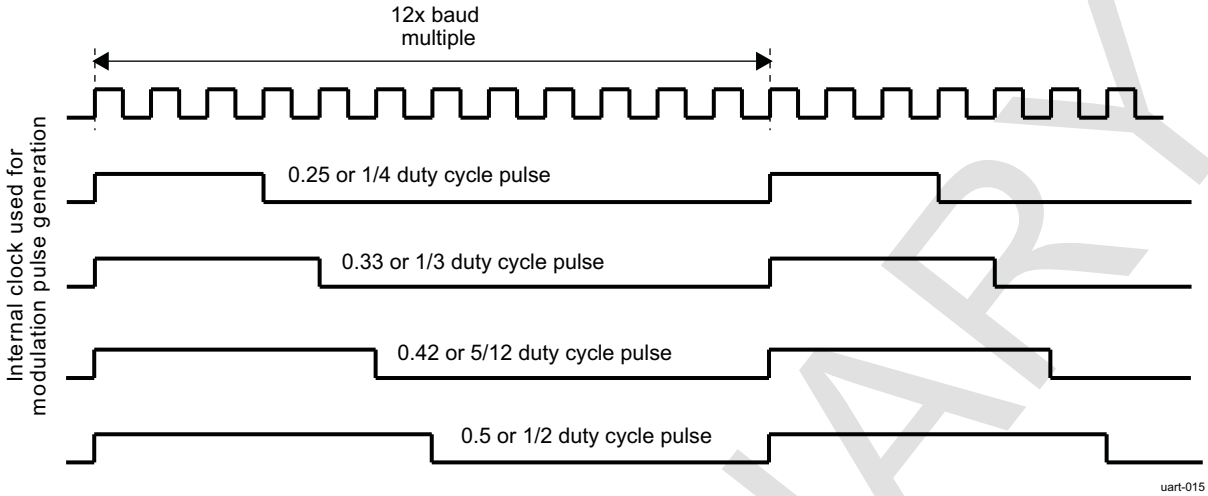
Figure 23-65. CIR Modulation Duty Cycle



The transmission logic ensures that all pulses are transmitted completely (no cutoff during transmission). While transmitting continuous bytes back-to-back, no delay is inserted between 2 transmitted bytes. Thus, software must handle the delay between consecutively transmitted bytes if the receiving end requires it.

23.3.2.6.2.3 Consumer IR Encoding/Decoding

There are two methods of encoding for remote-control applications:

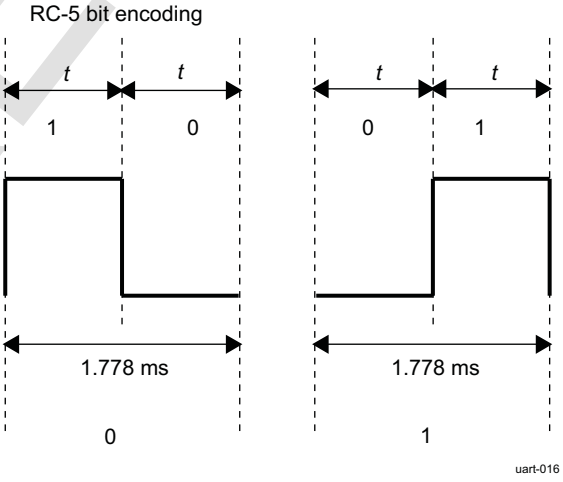
- Pulse duration encoding (time-extended bit forms): A variable pulse distance, or duration, in which the difference between logic 1 and logic 0 is the length of the pulse width
- Biphase encoding: The encoding of logic 0 and logic 1 is in the change of signal level from 1 to 0 or 0 to 1, respectively.

Japanese manufacturers favor pulse duration encoding; European manufacturers favor biphase encoding.

The CIR mode uses a completely flexible free-format encoding in which 1 is transmitted from the TX FIFO as a modulated pulse with duration *t*.

Similarly, 0 is transmitted as a blank duration T. The MPU constructs and deciphers the protocol of the data. For example, the RC-5 protocol using Manchester encoding can be emulated as using a 01 pair for 1 and a 10 pair for 0 (see Figure 23-66).

Figure 23-66. RC-5 Bit Encoding



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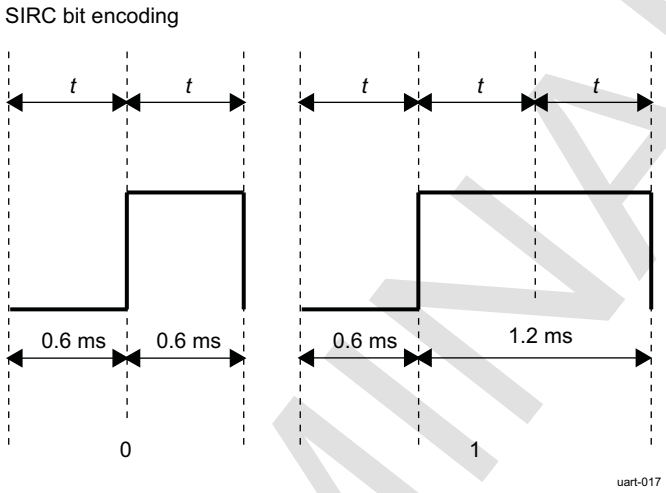
Because CIR mode logic does not impose a fixed format for infrared packets of data, the MPU software can define the format using simple data structures that are then modulated into an industry standard, such as RC-5 or SIRC. To send a sequence of 0101 in RC-5, the MPU software must write an 8-bit binary character of 10011001 to the data FIFO of the UART.

For SIRC, the modulation length (multiples of *t*) is used to distinguish between 1 and 0. The subsequent SIRC digits show the difference in encoding between this and, for example, RC-5. The pulse width is extended for one digit.

Figure 23-67 shows SIRC bit encoding.

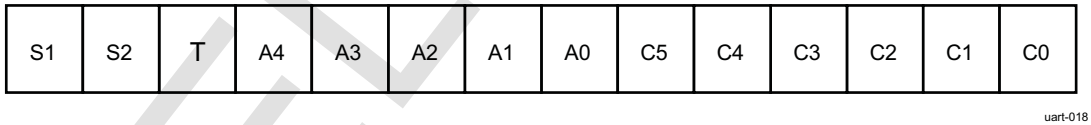
Figure 23-67. SIRC Bit Encoding



To construct comprehensive packets constituting remote-control commands, the MPU software must combine a number of 8-bit data characters in a sequence that follows one of the universally accepted formats.

Figure 23-68 shows a standard RC-5 frame as detected by UART3 in CIR mode (the SIRC format follows this). Each field in RC-5 can be considered as two *t* pulses (digital bits) from the TX FIFO.

Figure 23-68. RC-5 Standard Packet Format



Where:

S1, S2:	Start-bits (always 1)
T:	Toggle bit
A4..A0:	Address (or system) bits
C5..C0:	Command bits

The toggle bit T changes when a new command is transmitted to detect when the same key is pressed twice (effectively receiving the same data from the host consecutively). A brief delay in the transmission of the same command is detected by the use of the toggle bit because a code is sent while the MPU transmits characters to the UART for transmission. The address bits define the machine or device for which the infrared transmission is intended, and the command defines the operation.

To accommodate an extended RC-5 format, the S2 bit is replaced by an additional command bit (C6) that lets the command range increase to 7 bits. This format is known as the extended RC-5 format.

SIRC encoding uses the duration of modulation for mark and space; therefore, the duration of data bits in the standard frame length varies.

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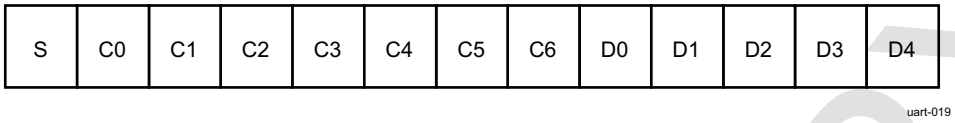
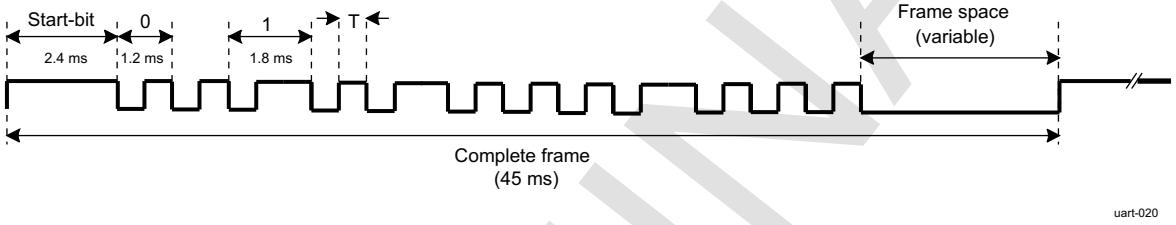
Figure 23-69 shows the packet format and bit encoding. As Figure 23-70 shows, 1 start-bit of 2.4 ms and control codes are followed by data that constitute the entire frame.

Figure 23-69. SIRC Packet Format



NOTE: The encoding must take a standard duration, but the contents of the data can vary. This implies that the control software for sending and receiving data packets must exercise a scheme of interpacket delay, where successive packets can be sent only after a real-time delay expires.

Figure 23-70. SIRC Bit Transmission Example



This document does not describe all encoding methods and techniques; the previous information discusses the considerations required to employ different encoding methods for different industry-standard protocols. See industry-standard documentation for specific methods of encoding and protocol use.

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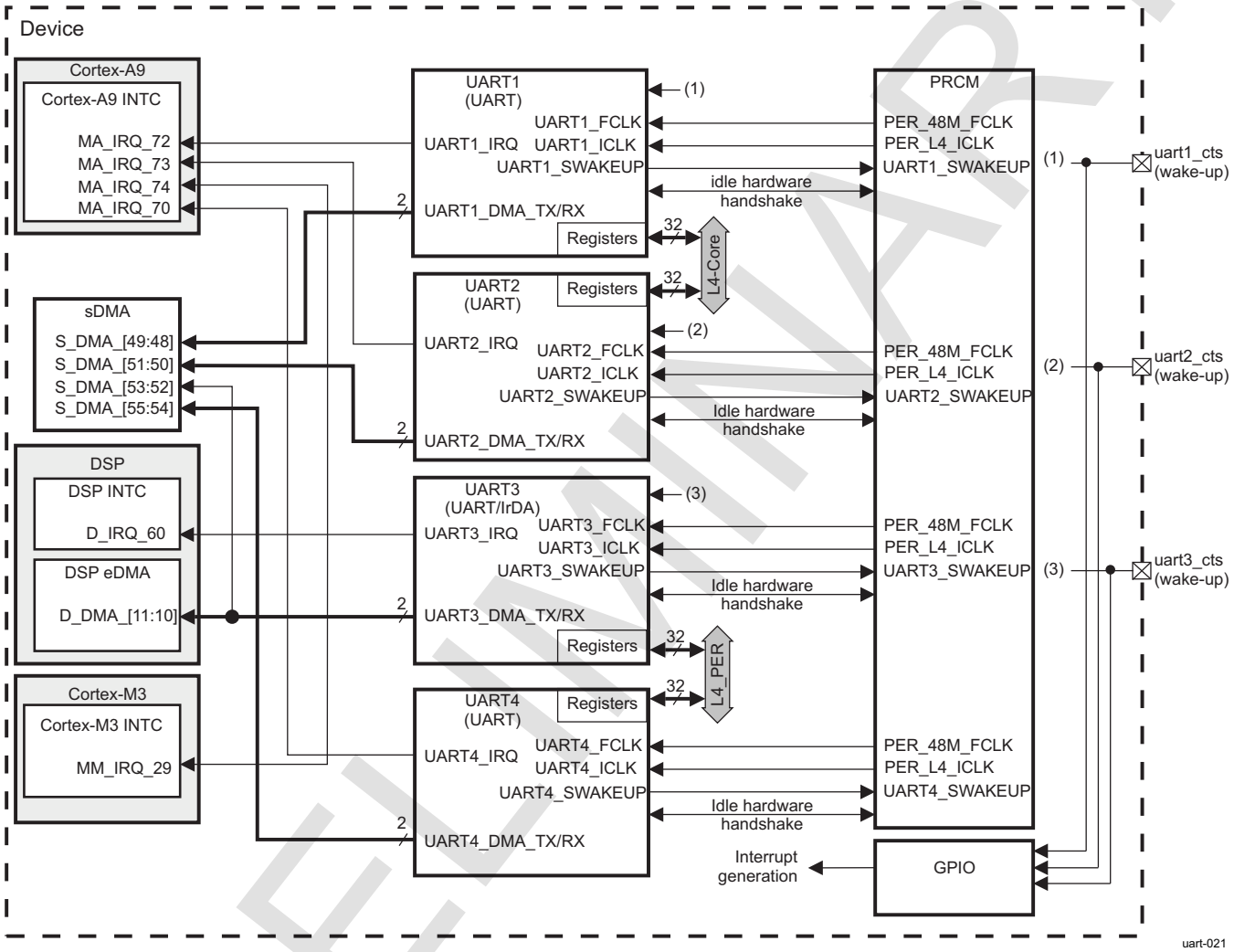
23.3.3 UART/IrDA/CIR Integration

This section describes module integration in the device, including information about clocks, resets, and hardware requests.

Figure 23-71 shows the device internal connections with related modules for UART functions.

Figure 23-71. UART/IrDA/CIR Integration



NOTE: For more information about the idle and standby hardware handshakes and the wake-up request, see Section 3.1.1.1.4, *Clock Domain-Level Clock Management*, in Chapter 3, *Power, Reset, and Clock Management*.

Table 23-142 through Table 23-144 summarize the integration of the module in the device.

Table 23-142. Integration Attributes

Module Instance	Attributes		
	Power Domain	Wake-Up Capability	Interconnect
UART1	PD_L4_PER	Yes	L4_PER
UART2	PD_L4_PER	Yes	L4_PER
UART3	PD_L4_PER	Yes	L4_PER
UART4	PD_L4_PER	Yes	L4_PER

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Table 23-143. Clocks and Resets

Clocks				
Module Instance	**Destination Signal**	**Source Signal**	**Source**	**Description**
UART1	UART1_ICLK	PER_L4_ICLK	PRCM	UART1 interface clock
	UART1_FCLK	PER_48M_FCLK	PRCM	UART1 functional clock
UART2	UART2_ICLK	PER_L4_ICLK	PRCM	UART2 interface clock
	UART2_FCLK	PER_48M_FCLK	PRCM	UART2 functional clock
UART3	UART3_ICLK	PER_L4_ICLK	PRCM	UART3 interface clock
	UART3_FCLK	PER_48M_FCLK	PRCM	UART3 functional clock
UART4	UART4_ICLK	PER_L4_ICLK	PRCM	UART4 interface clock
	UART4_FCLK	PER_48M_FCLK	PRCM	UART4 functional clock
Resets				
Module Instance	**Destination Signal**	**Source Signal**	**Source**	**Description**
UART1	UART1_RST	L4_PER_RST	PRCM	UART1 reset signal
UART2	UART2_RST	L4_PER_RST	PRCM	UART2 reset signal
UART3	UART3_RST	L4_PER_RST	PRCM	UART3 interface reset
UART4	UART4_RST	L4_PER_RST	PRCM	UART4 reset

Table 23-144. Hardware Requests

Interrupt Requests				
Module Instance	**Source Signal**	**Destination Signal**	**Destination**	**Description**
UART1	UART1_IRQ	MA_IRQ_72	Cortex-A9	UART module 1
UART2	UART2_IRQ	MA_IRQ_73	Cortex-A9	UART module 2
UART3	UART3_IRQ	D_IRQ_60	DSP	UART module 3 (also infrared)
	UART3_IRQ	MA_IRQ_74	Cortex-A9	UART module 3 (also infrared)
	UART3_IRQ	MM_IRQ_29	Cortex-M3	UART module 3 (also infrared)
UART4	UART4_IRQ	MA_IRQ_70	Cortex-A9	UART module 4
Direct Memory Access (DMA) Requests				
Module Instance	**Source Signal**	**Destination Signal**	**Destination**	**Description**
UART1	UART1_DMA_TX	S_DMA_48	sDMA	UART module 1 – transmit request
	UART1_DMA_RX	S_DMA_49	sDMA	UART module 1 – receive request
UART2	UART2_DMA_TX	S_DMA_50	sDMA	UART module 2 – transmit request
	UART2_DMA_RX	S_DMA_51	sDMA	UART module 2 – receive request
UART3	UART3_DMA_TX	S_DMA_52	sDMA	UART module 3 – transmit request (also infrared)
	UART3_DMA_RX	S_DMA_53	sDMA	UART module 3 – receive request (also infrared)
	UART3_DMA_TX	D_DMA_10	dDMA	UART module 3 – transmit request [0]
	UART3_DMA_RX	D_DMA_11	dDMA	UART module 3 – receive request [0]
UART4	UART4_DMA_TX	S_DMA_54	sDMA	UART module 4 – transmit request
	UART4_DMA_RX	S_DMA_55	sDMA	UART module 4 – receive request

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23.3.4 UART/IrDA/CIR Functional Description

23.3.4.1 Block Diagram

The UART/IrDA/CIR module can be divided into three main blocks:

- FIFO management
- Mode selection
- Protocol formatting

FIFO management is common to all functions and enables the transmission and reception of data from the host processor point of view.

There are two modes:

- Function mode: Routes the data to the chosen function (UART, IrDA, or CIR) and enables the mechanism corresponding to the chosen function
- Register mode: Enables conditional access to registers

For more information about mode configuration, see Section 23.3.4.7, *Mode Selection*.

Protocol formatting has three subcategories:

- Clock generation: The 48-MHz input clock generates all necessary clocks.
- Data formatting: Each function uses its own state-machine that is responsible for the transition between FIFO data and frame data associated with it.
- Interrupt management: Different interrupt types are generated depending on the chosen function:
  - UART mode interrupts: Seven interrupts prioritized in six different levels
  - IrDA mode interrupts: Eight interrupts. The interrupt line is activated when any interrupt is generated (there is no priority).
  - CIR mode interrupts: A subset of existing IrDA mode interrupts is used.

  In each mode, when an interrupt is generated, the UART_IIR register indicates the interrupt type.

In parallel with these functional blocks, a power-saving strategy exists for each function.

Figure 23-72 is the UART/IrDA/CIR block diagram.

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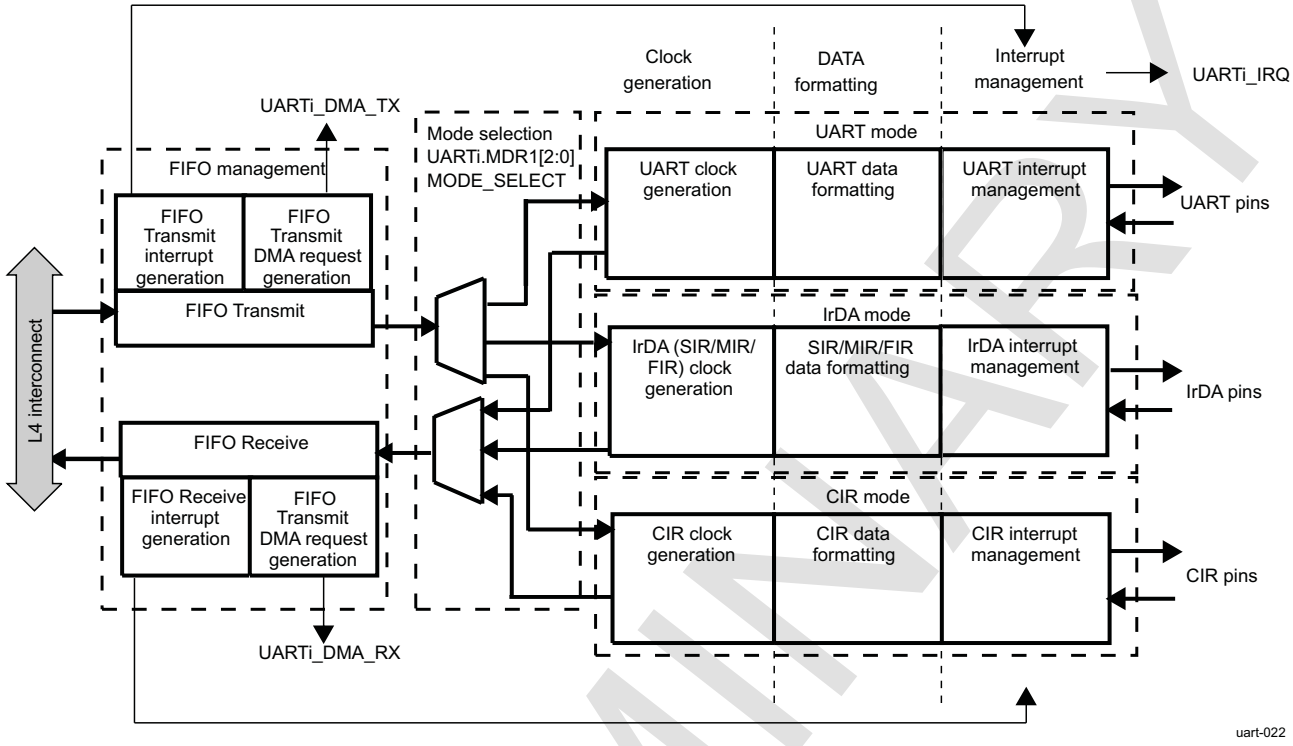
Figure 23-72. UART/IrDA/CIR Functional Specification Block Diagram



23.3.4.2 Clock Configuration

Each UART uses a 48-MHz functional clock for its logic and to generate external interface signals. Each UART uses an interface clock for register accesses. The PRCM module generates and controls all these clocks (for more information, see Section 3.6.4.4, *Clock Domain Module Attributes*, in Chapter 3, *Power, Reset, and Clock Management*).

The idle and wake-up processes use a handshake protocol between the PRCM and the UART (for a description of the protocol, see Section 3.1.1.1.2, *Module-Level Clock Managment*, in Chapter 3, *Power, Reset, and Clock Management*). The UARTi.UART_SYSC[4:3] IDLEMODE bit field controls UART idle mode.

23.3.4.3 Software Reset

The UARTi.UART_SYSC[1] SOFTRESET bit controls the software reset; setting this bit to 1 triggers a software reset functionally equivalent to hardware reset.

23.3.4.4 Power Management

23.3.4.4.1 UART Mode Power Management

23.3.4.4.1.1 Module Power Saving

In UART modes, sleep mode is enabled by setting the UARTi.UART_IER[4] SLEEP_MODE bit to 1 (when the UARTi.UART_EFR[4] ENHANCED_EN bit is set to 1).

Sleep mode is entered when all the following conditions exist:

- The serial data input line, uarti_rx, is idle.
- The TX FIFO and TX shift register are empty.
- The RX FIFO is empty.
- The only pending interrupts are THR interrupts.

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Sleep mode is a good way to lower UART power consumption, but this state can be achieved only when the UART is set to modem mode. Therefore, even if the UART has no key role functionally, it must be initialized in a functional mode to take advantage of sleep mode.

In sleep mode, the module clock and baud rate clock are stopped internally. Because most registers are clocked by these clocks, this greatly reduces power consumption. The module wakes up when a change is detected on the uarti_rx line, when data is written to the TX FIFO, and when there is a change in the state of the modem input pins.

An interrupt can be generated on a wake-up event by setting the UARTi.UART_SCR[4] RX_CTS_WU_EN bit to 1. To understand how to manage the interrupt, see Section 23.3.4.5.1.2, *Wake-Up Interrupt*.

NOTE: There must be no writing to the divisor latches, UARTi.UART_DLL and UARTi.UART_DLH, to set the baud clock (BCLK) while in sleep mode. It is advisable to disable sleep mode using the UARTi.UART_IER[4] SLEEP_MODE bit before writing to the UARTi.UART_DLL register or the UARTi.UART_DLH register.

23.3.4.4.1.2 System Power Saving

Sleep and auto-idle modes are embedded power-saving features. Power-reduction techniques can be applied at the system level by shutting down certain internal clock and power domains of the device.

The UART supports an idle req/idle ack handshaking protocol used at the system level to shut down the UART clocks in a clean and controlled manner and to switch the UART from interrupt-generation mode to wake-up generation mode for unmasked events (see the UARTi.UART_SYSC[2] ENAWAKEUP bit and the UARTi.UART_WER register).

For more information, see Section 3.1.1.1.2, *Module Level Clock Managment*, in Chapter 3, *Power, Reset, and Clock Management*.

23.3.4.4.2 IrDA Mode Power Management (UART3 Only)

23.3.4.4.2.1 Module Power Saving

In IrDA modes, sleep mode is enabled by setting the UART3.MDR[3] IR_SLEEP bit to 1.

Sleep mode is entered when all the following conditions exist:

- The serial data input line, uart3.rx_irrx, is idle.
- The TX FIFO and TX shift register are empty.
- The RX FIFO is empty.
- No interrupts are pending except THR interrupts.

The module wakes up when a change is detected on the uart3_rx_irrx line or when data is written to the TX FIFO.

23.3.4.4.2.2 System Power Saving

System power saving for the IrDA mode has the same function as for the UART mode (see Section 23.3.4.4.1.2, *System Power Saving*).

23.3.4.4.3 CIR Mode Power Management (UART3 Only)

23.3.4.4.3.1 Module Power Saving

Module power saving for the CIR mode has the same function as for the IrDA mode (see Section 23.3.4.4.2.1, *Module Power Saving*).

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23.3.4.4.3.2 System Power Saving

System power saving for the CIR mode has the same function as for the UART mode (see Section 23.3.4.4.1.2, *System Power Saving*).

23.3.4.4.4 Local Power Management

Table 23-145 describes power-management features available for the UART.

NOTE: For information about source clock gating and sleep/wake-up transitions description, see Section 3.1.1.1.2, *Module-Level Clock Managment*, in Chapter 3, *Power, Reset, and Clock Management*.

Table 23-145. Local Power-Management Features

Feature	Registers	Description
Clock autogating	UART_SYSC[0] AUTOIDLE	This bit allows local power optimization in the module by gating the UARTi_ICLK clock on interface activity or gating the UARTi_FCLK clock on internal activity.
Slave idle modes	UART_SYSC[4:3] IDLEMODE	Force-idle, no-idle, smart-idle, and smart-idle wakeup-capable modes are available
Clock activity	N/A	Feature not available
Master standby modes	N/A	Feature not available
Global wake-up enable	UART_SYSC[2] ENAWAKEUP	This bit enables the wake-up feature at module level.
Wake-Up sources enable	N/A	Feature not available

23.3.4.5 Interrupt Requests

23.3.4.5.1 UART Mode Interrupt Management

23.3.4.5.1.1 UART Interrupts

UART mode includes seven possible interrupts prioritized to six levels.

When an interrupt is generated, the interrupt identification register (UARTi.UART_IIR) sets the UARTi.UART_IIR[0] IT_PENDING bit to 0 to indicate that an interrupt is pending, and indicates the type of interrupt through the UARTi.UART_IIR[5:1] bit field. Table 23-146 summarizes the interrupt control functions.

Table 23-146. UART Mode Interrupts

UART_IIR[5:0]	Priority Level	Interrupt Type	Interrupt Source	Interrupt Reset Method
000001	None	None	None	None
000110	1	Receiver line status	OE, FE, PE, or BI errors occur in characters in the RX FIFO.	FE, PE, BI: Read the UART_RHR register. OE: Read the UART_LSR register.
001100	2	RX time-out	Stale data in RX FIFO	Read the UART_RHR register.
000100	2	RHR interrupt	DRDY (data ready) (FIFO disable)	Read the UART_RHR register until the interrupt condition disappears.
			RX FIFO above trigger level (FIFO enable)	
000010	3	THR interrupt	TFE (UART_THR empty) (FIFO disable)	Write to the UART_THR until the interrupt condition disappears.
			TX FIFO below trigger level (FIFO enable)	

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Table 23-146. UART Mode Interrupts (continued)

UART_IIR[5:0]	Priority Level	Interrupt Type	Interrupt Source	Interrupt Reset Method
000000	4	Modem status	See the UART_MSR register.	Read the UART_MSR register.
010000	5	XOFF interrupt/special character interrupt	Receive XOFF characters/special character	Receive XON character(s), if XOFF interrupt/read of the UART_IIR register, if special character interrupt.
100000	6	CTS, RTS	RTS pin or CTS pin change state from active (low) to inactive (high).	Read the UART_IIR register.

For the receiver-line status interrupt, the RX_FIFO_STS bit (UARTi.UART_LSR[7]) generates the interrupt.

For the XOFF interrupt, if an XOFF flow character detection caused the interrupt, the interrupt is cleared by an XON flow character detection. If special character detection caused the interrupt, the interrupt is cleared by a read of the UARTi.UART_IIR register.

23.3.4.5.1.2 Wake-Up Interrupt

Wake-up interrupt is a special interrupt that works differently from other interrupts. This interrupt is enabled when the UARTi.UART_SCR[4] RX_CTS_WU_EN bit is set to 1. The UARTi.UART_IIR register is not modified when this occurs; the UART3.UART_SSR[1] RX_CTS_WU_STS bit must be checked to detect a wake-up event.

When a wake-up interrupt occurs, it can be cleared only by resetting the UARTi.UART_SCR[4] RX_CTS_WU_EN bit. This bit must be reenabled (set to 1) after the current wake-up interrupt event is processed to detect the next incoming wake-up event.

23.3.4.5.2 IrDA Mode Interrupt Management

23.3.4.5.2.1 IrDA Interrupts

The IrDA function generates interrupts. All interrupts can be enabled and disabled by writing to the appropriate bit in the interrupt enable register (UART3.UART_IER). The interrupt status of the device can be checked by reading the interrupt identification register (UART3.UART_IIR).

UART, IrDA, and CIR modes have different interrupts in the UART/IrDA/CIR module and, therefore, different UART3.UART_IER and UART3.UART_IIR mappings, depending on the selected mode.

IrDA modes have eight possible interrupts (see Table 23-147). The interrupt line is activated when any interrupt is generated (there is no priority).

Table 23-147. IrDA Mode Interrupts

UART_IIR Bit	Interrupt Type	Interrupt Source	Interrupt Reset Method
0	RHR interrupt	DRDY (data ready) (FIFO disable) RX FIFO above trigger level (FIFO enable)	Read the UART_RHR register until the interrupt condition disappears.
1	THR interrupt	TFE (UART_THR empty) (FIFO disable) TX FIFO below trigger level (FIFO enable)	Write to the UART_THR until the interrupt condition disappears.
2	Last byte in RX FIFO	Last byte of frame in RX FIFO is available to be read at the RHR port.	Read the UART_RHR register.
3	RX overrun	Write to the UART_RHR register when the RX FIFO is full.	Read UART_RESUME register.

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Table 23-147. IrDA Mode Interrupts (continued)

UART_IIR Bit	Interrupt Type	Interrupt Source	Interrupt Reset Method
4	Status FIFO interrupt	Status FIFO triggers level reached.	Read STATUS FIFO.
5	TX status	1. UART_THR empty before EOF sent. Last bit of transmission of the IrDA frame occurred, but with an underrun error. OR 2. Transmission of the last bit of the IrDA frame completed successfully.	1. Read the UART_RESUME register. OR 2. Read the UART_IIR register.
6	Receiver line status interrupt	CRC, ABORT, or frame-length error is written into the STATUS FIFO.	Read the STATUS FIFO (read until empty - maximum of eight reads required).
7	Received EOF	Received end-of-frame	Read the UART_IIR register.

23.3.4.5.2.2 Wake-Up Interrupts

The wake-up interrupt for IrDA mode has the same function as that for UART mode (see Section 23.3.4.5.1.2, *Wake-Up Interrupt*).

CAUTION

Wake-Up interface implementation in this mode is based on the UARTi_SIDLEACK low-to-high transition instead of the UARTi_SIDLEACK state.

This does not ensure wake-up event generation as expected when configured in smart-idle mode, and the system wakes up for a short period.

23.3.4.5.3 CIR Mode Interrupt Management

23.3.4.5.3.1 CIR Interrupts

The CIR function generates interrupts that can be enabled and disabled by writing to the appropriate bit in the interrupt enable register (UART3.UART_IER). The interrupt status of the device can be checked by reading the interrupt identification register (UART3.UART_IIR).

UART, IrDA, and CIR modes have different interrupts in the UART/IrDA/CIR module and, therefore, different UART3.UART_IER and UART3.UART_IIR mappings, depending on the selected mode.

Table 23-148 lists the interrupt modes to be maintained. In CIR mode, the sole purpose of the UART3.UART_IIR[5] bit is to indicate that the last bit of infrared data was passed to the uart3_cts_rctx pin.

Table 23-148. CIR Mode Interrupts

UART_IIR Bit Number	Interrupt Type	Interrupt Source	Interrupt Reset Method
0	N/A for CIR mode	N/A for CIR mode	N/A for CIR mode
1	THR interrupt	TFE (UART_THR empty) (FIFO disable) TX FIFO below trigger level (FIFO enable)	Write to the UART_THR register until the interrupt condition disappears.
2	N/A for CIR mode	N/A for CIR mode	N/A for CIR mode
3	N/A for CIR mode	N/A for CIR mode	N/A for CIR mode
4	N/A for CIR mode	N/A for CIR mode	N/A for CIR mode

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Table 23-148. CIR Mode Interrupts (continued)

UART_IIR Bit Number	Interrupt Type	Interrupt Source	Interrupt Reset Method
5	TX status	Transmission of the last bit of the frame is complete successfully.	Read the UART_IIR register.
6	N/A for CIR mode	N/A for CIR mode	N/A for CIR mode
7	N/A for CIR mode	N/A for CIR mode	N/A for CIR mode

23.3.4.5.3.2 Wake-Up Interrupts

The wake-up interrupt for CIR mode has the same function as that for UART mode (see Section 23.3.4.5.1.2, *Wake-Up Interrupt*).

23.3.4.6 FIFO Management

The FIFO is accessed by reading and writing the UARTi.UART_RHR and UARTi.UART_THR registers. Parameters are controlled using the FIFO control register (UARTi.UART_FCR) and supplementary control register (UARTi.UART_SCR). Reading the UARTi.UART_SSR[0] TX_FIFO_FULL bit at 1 means the FIFO is full.

The UARTi.UART_TLR register controls the FIFO trigger level, which enables DMA and interrupt generation. After reset, transmit (TX) and receive (RX) FIFOs are disabled; thus, the trigger level is the default value of 1 byte. Figure 23-73 shows the FIFO management registers.

NOTE: Data in the UARTi.UART_RHR register is not overwritten when an overflow occurs.

NOTE: The UARTi.UART_SFLSR, UARTi.UART_SFREGL, and UARTi.UART_SFREGH status registers are used in IrDA mode only. For use, see Section 23.3.4.8.2.3, *IrDA Data Formatting*.

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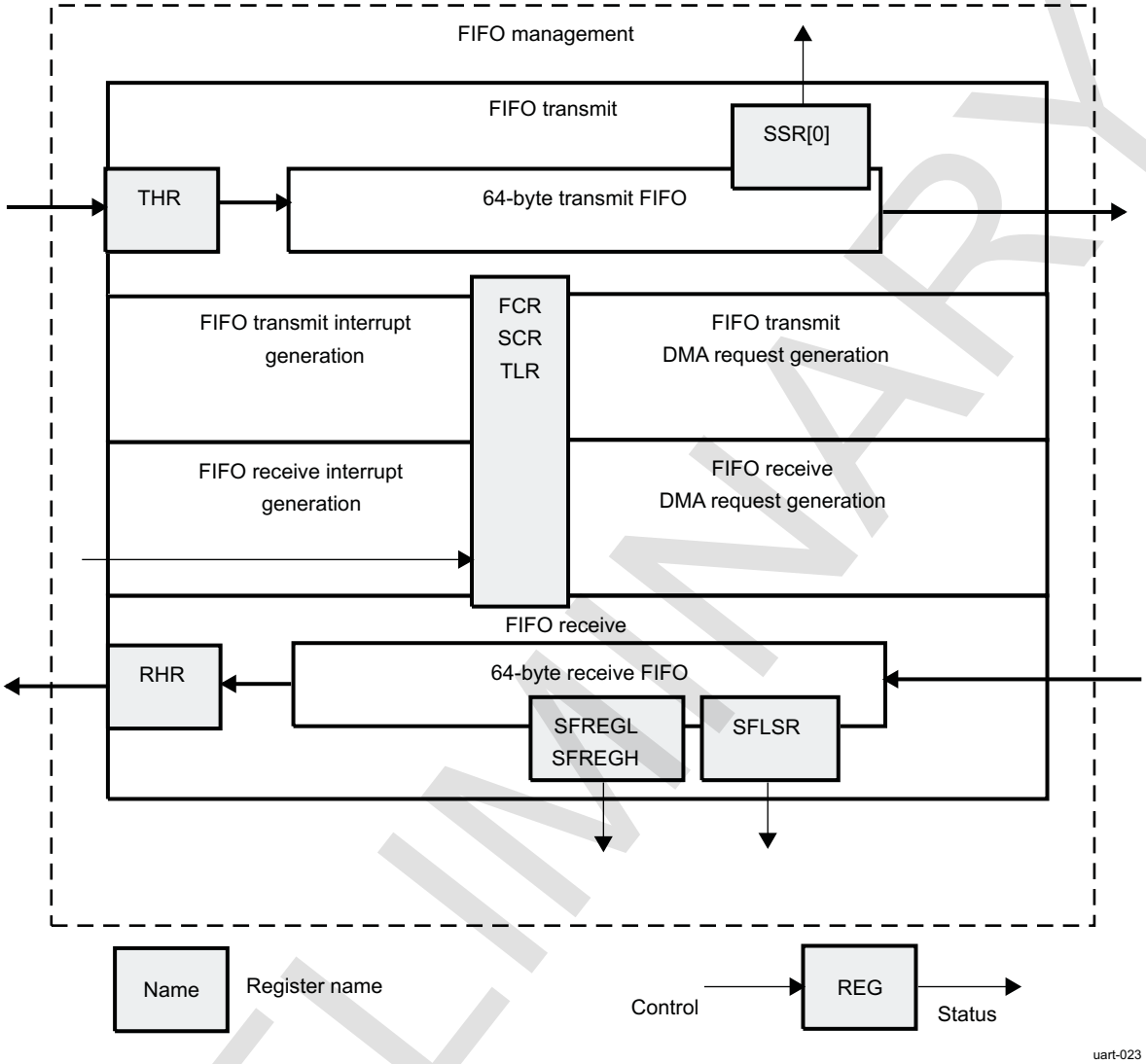
Figure 23-73. FIFO Management Registers



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23.3.4.6.1 FIFO Trigger

23.3.4.6.1.1 Transmit FIFO Trigger

Table 23-149 lists the TX FIFO trigger level settings.

Table 23-149. TX FIFO Trigger Level Setting Summary

UART_SCR[6]	UART_TLR[3:0]	TX FIFO Trigger Level
0	= 0x0	Defined by the UARTi.UART_FCR[5:4] TX_FIFO_TRIG bit field (8,16, 32, or 56 spaces)
0	!= 0x0	Defined by the UARTi.UART_TLR[3:0] TX_FIFO_TRIG_DMA bit field (from 4 to 60 spaces with a granularity of 4 spaces)
1	Value	Defined by the concatenated value of TX_FIFO_TRIG_DMA and TX_FIFO_TRIG (from 1 to 63 spaces with a granularity of 1 space) **Note:** The combination of TX_FIFO_TRIG_DMA = 0x0 and TX_FIFO_TRIG = 0x0 (all zeros) is not supported (minimum of one space required). All zeros result in unpredictable behavior.

23.3.4.6.1.2 Receive FIFO Trigger

Table 23-150 lists the RX FIFO trigger level settings.

Table 23-150. RX FIFO Trigger Level Setting Summary

UART_SCR[7]	UART_TLR[7:4]	RX FIFO Trigger Level
0	= 0x0	Defined by the UARTi.UART_FCR[7:6] RX_FIFO_TRIG bit field (8,16, 56, or 60 characters)
0	!= 0x0	Defined by the UARTi.UART_TLR[7:4] RX_FIFO_TRIG_DMA bit field (from 4 to 60 characters with a granularity of 4 characters)
1	Value	Defined by the concatenated value of RX_FIFO_TRIG_DMA and RX_FIFO_TRIG (from 1 to 63 characters with a granularity of 1 character) **Note:** The combination of RX_FIFO_TRIG_DMA = 0x0 and RX_FIFO_TRIG = 0x0 (all zeros) is not supported (minimum of one character required). All zeros result in unpredictable behavior.

The receive threshold is programmed using the UARTi.UART_TCR[7:4] RX_FIFO_TRIG_START and UARTi.UART_TCR[3:0] RX_FIFO_TRIG_HALT bit fields:

- Trigger levels from 0 to 60 bytes are available with a granularity of 4 (trigger level = 4 x [4-bit register value]).
- To ensure correct device operation, ensure that RX_FIFO_TRIG_HALT RX_FIFO_TRIG when auto-RTS is enabled.

  Delay = [4 + 16 x (1 + CHAR_LENGTH + Parity + Stop 0.5)] x Baud_rate + 4 x FCLK

  NOTE: The RTS signal is deasserted after the UART module receives the data over RX_FIFO_TRIG_HALT. Delay means how long the UART module takes to deassert the RTS signal after reaching RX_FIFO_TRIG_HALT.

- In FIFO interrupt mode with flow control, ensure that the trigger level to HALT transmission is greater than or equal to the RX FIFO trigger level (the UARTi.UART_TCR[7:4] RX_FIFO_TRIG_START bit field or the UARTi.UART_FCR[7:6] RX_FIFO_TRIG bit field); otherwise, FIFO operation stalls. In FIFO DMA mode with flow control, this concept does not exist, because a DMA request is sent when a byte is received.

23.3.4.6.2 FIFO Interrupt Mode

In FIFO interrupt mode (the FIFO control register UARTi.UART_FCR[0] FIFO_EN bit is set to 1 and

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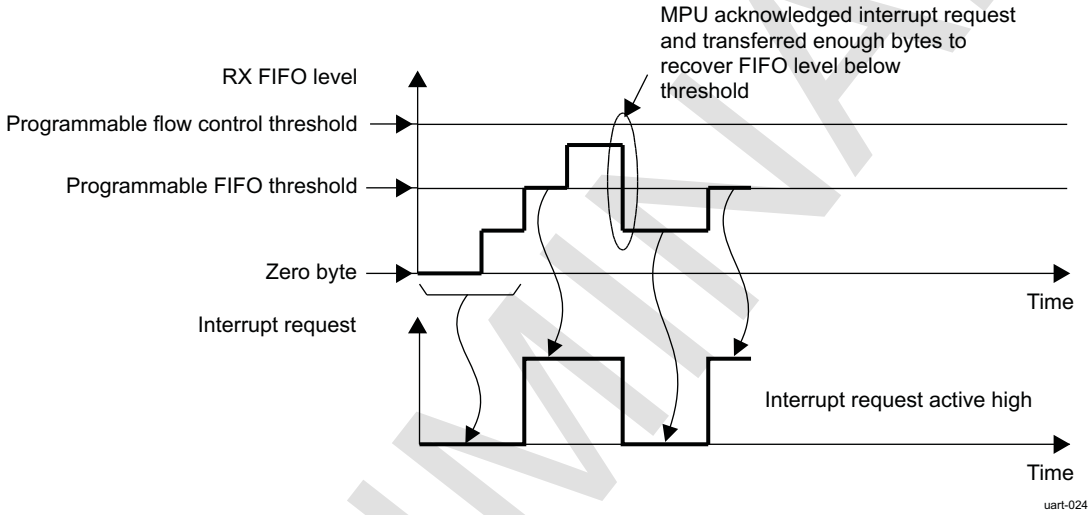
relevant interrupts are enabled by the UARTi.UART_IER register), an interrupt signal informs the processor of the status of the receiver and transmitter. These interrupts are raised when the RX/TX FIFO threshold (the UARTi.UART_TLR[7:4] RX_FIFO_TRIG_DMA and UARTi.UART_TLR[3:0] TX_FIFO_TRIG_DMA bit fields or the UARTi.UART_FCR[7:6] RX_FIFO_TRIG and UARTi.UART_FCR[5:4] TX_FIFO_TRIG bit fields, respectively) is reached.

The interrupt signals instruct the MPU to transfer data to the destination (from the UART in receive mode and/or from any source to the UART FIFO in transmit mode).

When UART flow control is enabled with interrupt capabilities, the UART flow control FIFO threshold (the UARTi.UART_TCR[3:0] RX_FIFO_TRIG_HALT bit field) must be greater than or equal to the RX FIFO threshold.

Figure 23-74 shows the generation of the RX FIFO interrupt request.

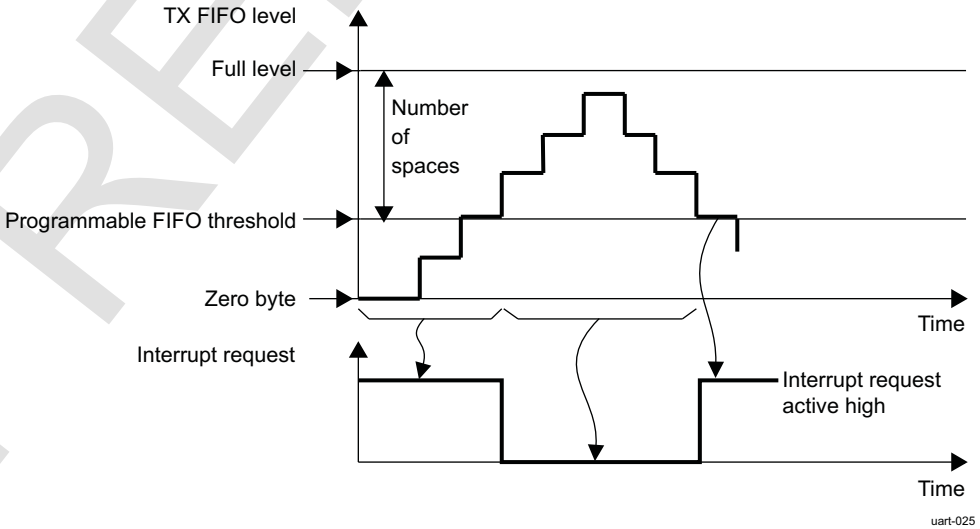
Figure 23-74. RX FIFO Interrupt Request Generation



In receive mode, no interrupt is generated until the RX FIFO reaches its threshold. Once low, the interrupt can be deasserted only when the MPU has handled enough bytes to put the FIFO level below threshold. The flow control threshold is set at a higher value than the FIFO threshold.

Figure 23-75 shows the generation of the TX FIFO interrupt request.

Figure 23-75. TX FIFO Interrupt Request Generation



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In transmit mode, an interrupt request is automatically asserted when the TX FIFO is empty. This request is deasserted when the TX FIFO crosses the threshold level. The interrupt line is deasserted until a sufficient number of elements is transmitted to go below the TX FIFO threshold.

23.3.4.6.3 FIFO Polled Mode Operation

In FIFO polled mode (the UARTi.UART_FCR[0] FIFO_EN bit is set to 0 and the relevant interrupts are disabled by the UARTi.UART_IER register), the status of the receiver and transmitter can be checked by polling the line status register (UARTi.UART_LSR).

This mode is an alternative to the FIFO interrupt mode of operation in which the status of the receiver and transmitter is automatically determined by sending interrupts to the MPU.

23.3.4.6.4 FIFO DMA Mode Operation

Although DMA operation includes four modes (DMA modes 0 through 3), the information in Table 23-144 assumes that mode 1 is used. (Mode 2 and mode 3 are legacy modes that use only one DMA request for each module.)

In mode 2, the remaining DMA request is used for RX. In mode 3, the remaining DMA request is used for TX.

DMA requests in mode 2 and mode 3 use the following signals:

- S_DMA_48
- S_DMA_50
- S_DMA_52/D_DMA_10
- S_DMA_54

The following signals are not used by the module in mode 2 and mode 3:

- S_DMA_49
- S_DMA_51
- S_DMA_53/D_DMA_11
- S_DMA_55

These signals can be selected as follows:

- When the UARTi.UART_SCR[0] DMA_MODE_CTL bit is set to 0, setting the UARTi.UART_FCR[3] DMA_MODE_CTL bit to 0 enables DMA mode 0. Setting the DMA_MODE_CTL bit to 1 enables DMA mode 1.
- When the DMA_MODE_CTL bit is set to 1, the UARTi.UART_FCR[2:1] DMA_MODE_2 bit field determines DMA mode 0 to mode 3 based on the supplementary control register (UART_SCR) description.

For example:

- If no DMA operation is desired, set the DMA_MODE_CTL bit to 1 and the DMA_MODE_2 bit field to 0x0. (The DMA_MODE bit is discarded.)
- If DMA mode 1 is desired, set the DMA_MODE_CTL bit to 0 and the DMA_MODE bit to 1, or set the DMA_MODE_CTL bit to 1 and the DMA_MODE_2 bit field to 01. (The DMA_MODE bit is discarded.)

If the FIFOs are disabled (the UARTi.UART_FCR[0] FIFO_EN bit is set to 0), the DMA occurs in single-character transfers.

When DMA mode 0 is programmed, the signals associated with DMA operation are not active.

Depending on UART_MDR3[2] SET_DMA_TX_THRESHOLD, the threshold can be programmed different ways:

- SET_TX_DMA_THRESHOLD = 1:

  The threshold value will be the value of the UART_TX_DMA_THRESHOLD register. If SET_TX_DMA_THRESHOLD + TX trigger spaces 64, then the default method of threshold is used: threshold value = TX FIFO size.

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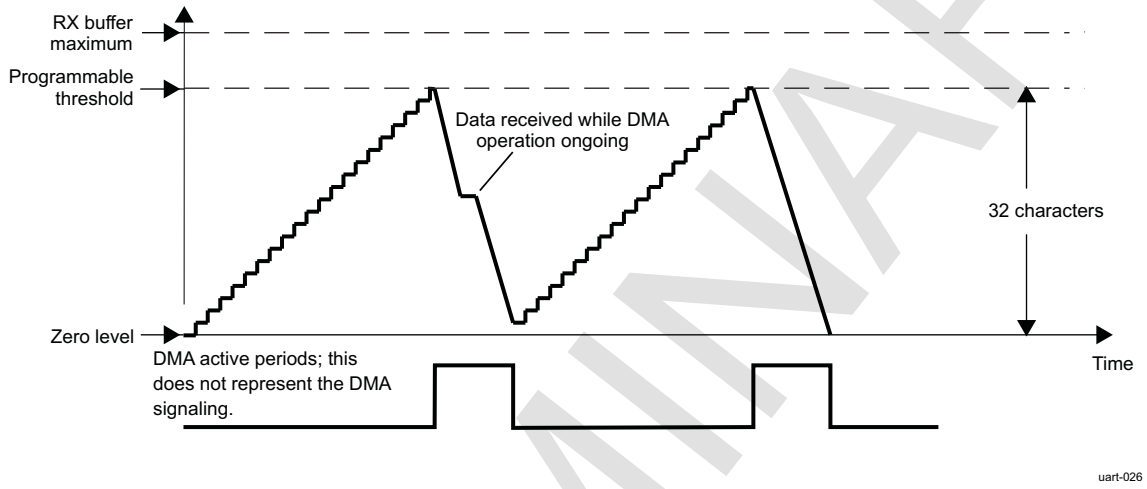
- SET_TX_DMA_THRESHOLD = 0:

  The threshold value = TX FIFO size TX trigger space. The TX DMA line is asserted if the TX FIFO level is lower then the threshold. It remains asserted until TX trigger spaces number of bytes are written into the FIFO. The DMA line is then deasserted and the FIFO level is compared with the threshold value.

23.3.4.6.4.1 DMA Transfers (DMA Mode 1, 2, or 3)

Figure 23-76 through Figure 23-79 show the supported DMA operations.

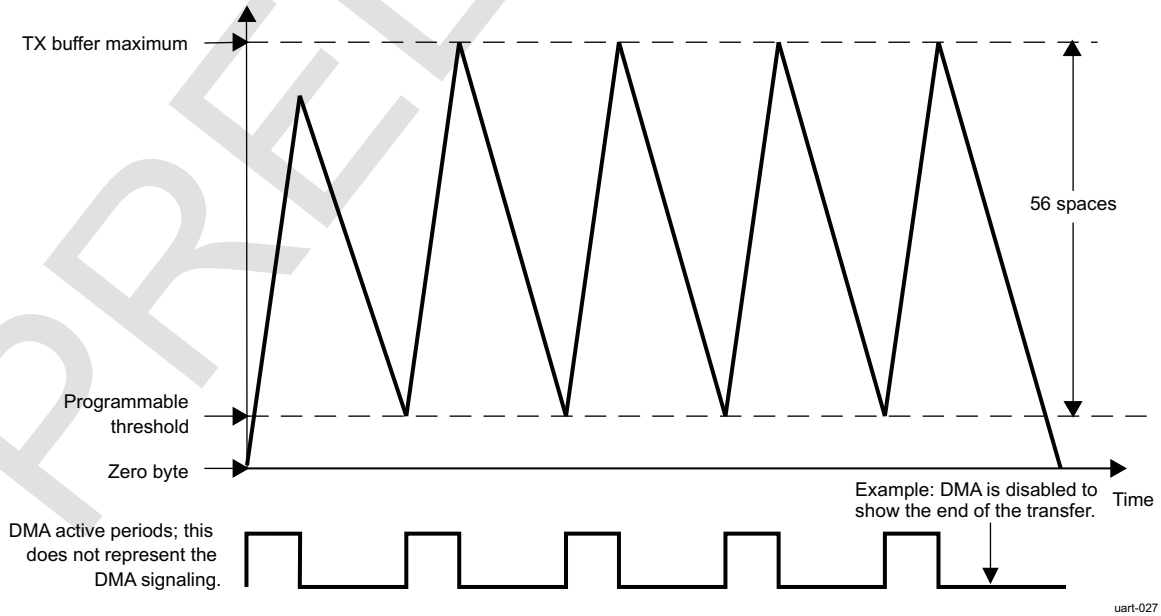
Figure 23-76. Receive FIFO DMA Request Generation (32 Characters)



In receive mode, a DMA request is generated when the RX FIFO reaches its threshold level defined in the trigger level register (UARTi.UART_TLR). This request is deasserted when the number of bytes defined by the threshold level is read by the sDMA.

In transmit mode, a DMA request is automatically asserted when the TX FIFO is empty. This request is deasserted when the number of bytes defined by the number of spaces in the UARTi.UART_TLR register is written by the sDMA. If an insufficient number of characters is written, the DMA request stays active.

Figure 23-77. Transmit FIFO DMA Request Generation (56 Spaces)



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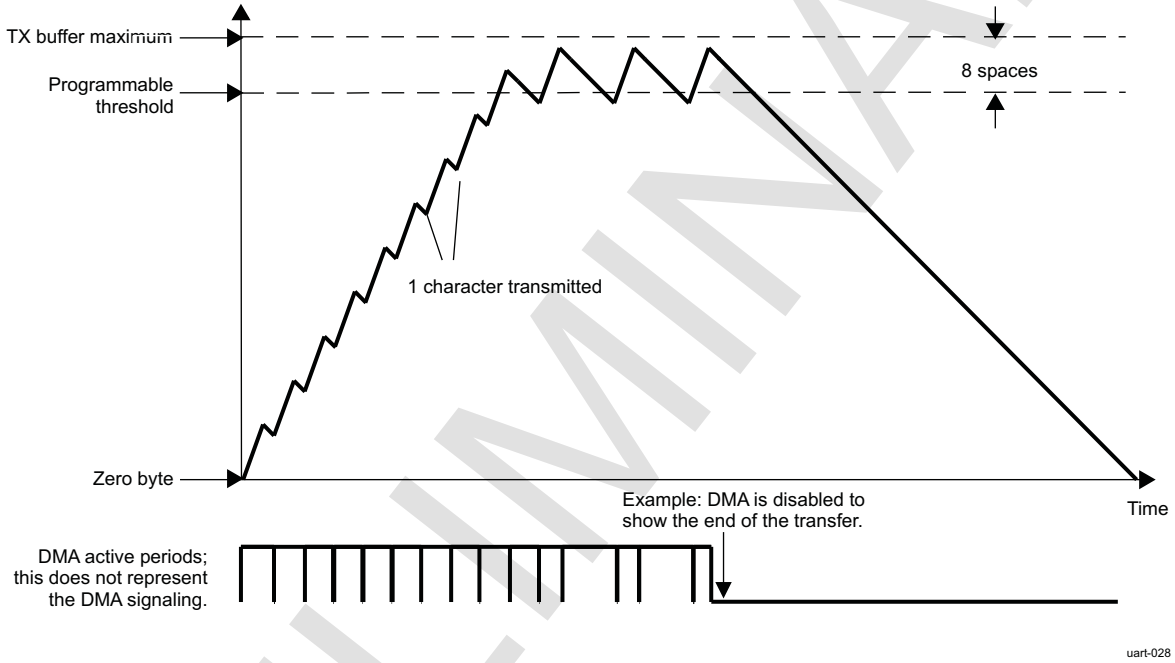
The DMA request is again asserted if the FIFO can receive the number of bytes defined by the UARTi.UART_TLR register.

The threshold can be programmed in a number of ways. Figure 23-77 shows a DMA transfer operating with a space setting of 56 that can arise from using the auto settings in the UARTi.UART_FCR[5:4] TX_FIFO_TRIG bit field or the UARTi.UART_TLR[3:0] TX_FIFO_TRIG_DMA bit field concatenated with the TX_FIFO_TRIG bit field.

The setting of 56 spaces in the UART/IrDA/CIR module must correlate with the settings of the sDMA so that the buffer does not overflow (program the DMA request size of the LH controller to equal the number of spaces in the UART/IrDA/CIR module).

Figure 23-78 shows an example with eight spaces to show the buffer level crossing the space threshold. The LH DMA controller settings must correspond to those of the UART/IrDA/CIR module.

Figure 23-78. Transmit FIFO DMA Request Generation (8 Spaces)



The next example shows the setting of one space that uses the DMA for each transfer of one character to the transmit buffer (see Figure 23-79). The buffer is filled faster than the baud rate at which data is transmitted to the TX pin. Eventually, the buffer is completely full and the DMA operations stop transferring data to the transmit buffer.

On two occasions, the buffer holds the maximum amount of data words; shortly after this, the DMA is disabled to show the slower transmission of the data words to the TX pin. Eventually, the buffer is emptied at the rate specified by the baud rate settings of the UARTi.UART_DLL and UARTi.UART_DLH registers.

The DMA settings must correspond to the system LH DMA controller settings to ensure correct operation of this logic.

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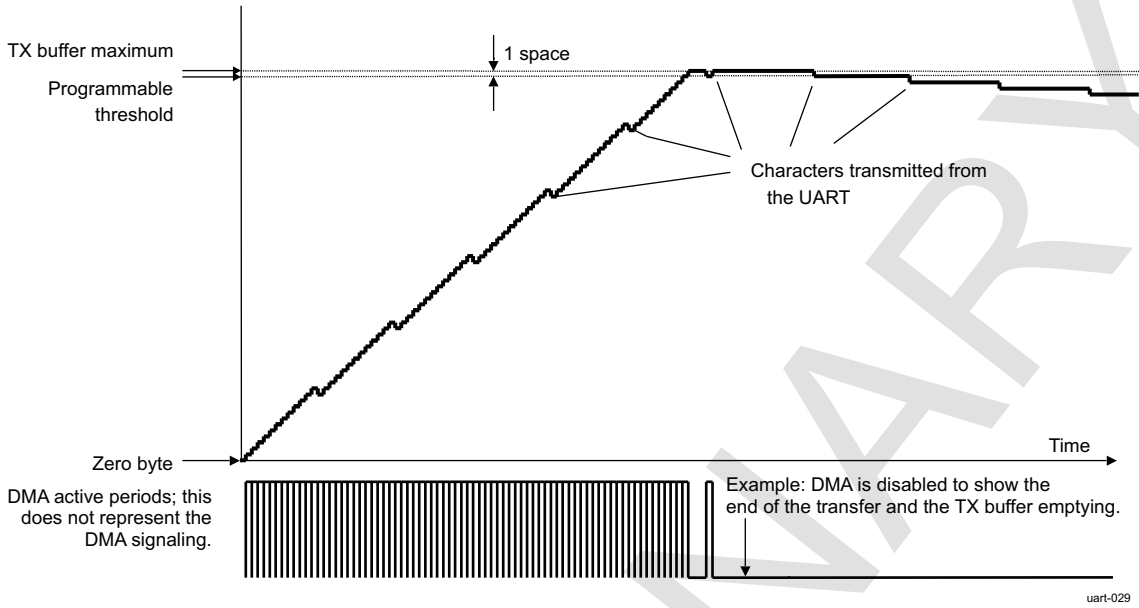
Figure 23-79. Transmit FIFO DMA Request Generation (1 Space)



The final example shows the setting of eight spaces, but setting the TX DMA threshold directly by setting the UART_MDR3[1] NONDEFAULT_FREQ bit and the UART_TX_DMA_THRESHOLD register (see Figure 23-80). In the example, UART_TX_DMA_THRESHOLD[2:0] TX_DMA_THRESHOLD = 3 and the trigger level is 8. The buffer is filled at a faster rate than the baud rate transmits data to the TX pin. The buffer is filled with 8 bytes and the DMA operations stop transferring data to the transmit buffer. When the buffer is emptied to the threshold level by transmission, the DMA operation activates again to fill the buffer with 8 bytes.

Eventually, the buffer is emptied at the rate specified by the baud rate settings of the UART_DLL and UART_DLH registers.

If the selected threshold level plus the trigger level exceed the maximum buffer size, the original TX DMA threshold method is used to prevent TX overrun, regardless of the value of the UART_MDR3[1] NONDEFAULT_FREQ bit.

The DMA settings must correspond to the settings of the system local host DMA controller to ensure the correct operation of this logic.

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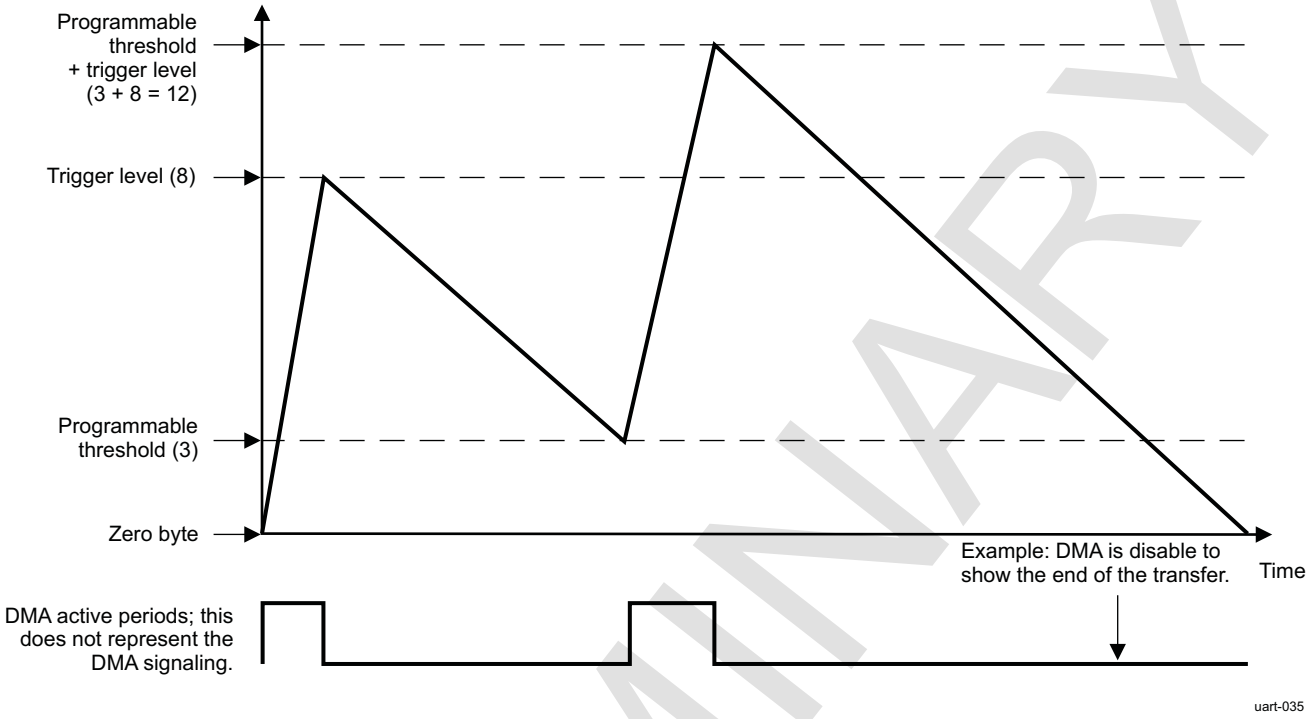
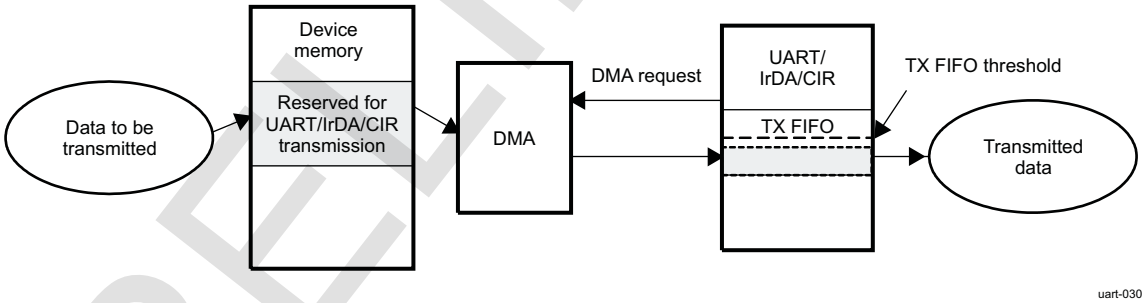
Figure 23-80. Transmit FIFO DMA Request Generation Using Direct TX DMA Threshold Programming. (Threshold = 3; Spaces = 8)



23.3.4.6.4.2 DMA Transmission

Figure 23-81 shows DMA transmission.

Figure 23-81. DMA Transmission



1. Data to be transmitted are put in the device memory reserved for UART/IrDA/CIR transmission by the DMA:
   (a) Until the TX FIFO trigger level is not reached, a DMA request is generated
   (b) An element (1 byte) is transferred from the SDRAM to the TX FIFO at each DMA request (DMA element synchronization).
2. Data in the TX FIFO are automatically transmitted.
3. The end of the transmission is signaled by the UARTi.UART_THR empty (TX FIFO empty).

NOTE: In IrDA mode, the transmission does not end immediately after the TX FIFO empties, at which point the last data byte, the CRC field, and the stop flag still must be transmitted; thus, the end of transmission occurs a few milliseconds after the UARTi.UART_THR register empties.

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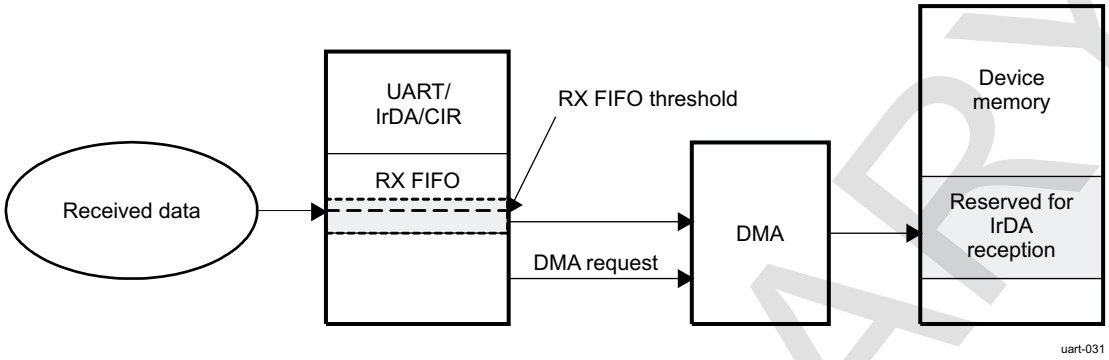
23.3.4.6.4.3 DMA Reception

Figure 23-82 shows DMA reception.

Figure 23-82. DMA Reception



1. Enable the reception.
2. Received data are put in the RX FIFO.
3. Data are transferred from the RX FIFO to the device memory by the DMA:
   (a) At each received byte, the RX FIFO trigger level (one character) is reached and a DMA request is generated.
   (b) An element (1 byte) is transferred from the RX FIFO to the SDRAM at each DMA request (DMA element synchronization).
4. The end of the reception is signaled by the EOF interrupt.

23.3.4.7 Mode Selection

23.3.4.7.1 Register Access Modes

23.3.4.7.1.1 Operational Mode and Configuration Modes

Register access depends on the register access mode, although register access modes are not correlated to functional mode selection. Three different modes are available:

- Operational mode
- Configuration mode A
- Configuration mode B

Operational mode is the selected mode when the function is active; serial data transfer can be performed in this mode.

Configuration mode A and configuration mode B are used during module initialization steps. These modes enable access to configuration registers, which are hidden in the operational mode. The modes are used when the module is inactive (no serial data transfer processed) and only for initialization or reconfiguration of the module.

The value of the UARTi.UART_LCR register determines the register access mode (see Table 23-151).

Table 23-151. UART/IrDA/CIR Register Access Mode Programming (Using UART_LCR)

Mode	Condition
Configuration mode A	UART_LCR[7] = 0x1 and UART_LCR[7:0] != 0xBF
Configuration mode B	UART_LCR[7] = 0x1 and UART_LCR[7:0] = 0xBF
Operational mode	UART_LCR[7] = 0x0

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23.3.4.7.1.2 Register Access Submode

In each access register mode (operational mode or configuration mode A/B), some register accesses are conditional on the programming of a submode (MSR_SPR, TCR_TLR, and XOFF). These registers are identified in Section 23.3.6, *UART/IrDA/CIR Register Manual*.

Table 23-152 through Table 23-154 summarize the register access submodes.

Table 23-152. Subconfiguration Mode A Summary

Mode	Condition
MSR_SPR	(UART_EFR[4] = 0x0 or UART_MCR[6] = 0x0)
TCR_TLR	UART_EFR[4] = 0x1 and UART_MCR[6] = 0x1

Table 23-153. Subconfiguration Mode B Summary

Mode	Condition
TCR_TLR	UART_EFR[4] = 0x1 and UART_MCR[6] = 0x1
XOFF	(UART_EFR[4] = 0x0 or UART_MCR[6] = 0x0)

Table 23-154. Suboperational Mode Summary

Mode	Condition
MSR_SPR	UART_EFR[4] = 0x0 or UART_MCR[6] = 0x0
TCR_TLR	UART_EFR[4] = 0x1 and UART_MCR[6] = 0x1

23.3.4.7.1.3 Registers Available for the Register Access Modes

Table 23-155 lists the names of the register bits in each access register mode. Gray shading indicates that the register does not depend on the register access mode (available in all modes).

Table 23-155. UART/IrDA/CIR Register Access Mode Overview

Address Offset	Registers					
	Configuration Mode A		Configuration Mode B		Operational Mode	
	Read	Write	Read	Write	Read	Write
0x000	UART_DLL	UART_DLL	UART_DLL	UART_DLL	UART_RHR	UART_THR
0x004	UART_DLH	UART_DLH	UART_DLH	UART_DLH	UART_IER	UART_IER
0x008	UART_IIR	UART_FCR	UART_EFR	UART_EFR	UART_IIR	UART_FCR
0x00C	UART_LCR	UART_LCR	UART_LCR	UART_LCR	UART_LCR	UART_LCR
0x010	UART_MCR	UART_MCR	UART_XON1_ADDR1	UART_XON1_ADDR1	UART_MCR	UART_MCR
0x014	UART_LSR	–	UART_XON2_ADDR2	UART_XON2_ADDR2	UART_LSR	–
0x018	UART_MSR (1)/UART_TCR (2)	UART_TCR (2)	UART_TCR (2)/UART_XOFF1 (3)	UART_TCR (2)/UART_XOFF1 (3)	UART_MSR (1)/UART_TCR (2)	UART_TCR (2)
0x01C	UART_SPR (1)/UART_TLR (2)	UART_SPR (1)/UART_TLR (2)	UART_TLR (2)/UART_XOFF2 (3)	UART_TLR (2)/UART_XOFF2 (3)	UART_SPR (1)/UART_TLR (2)	UART_SPR (1)/UART_TLR (2)
0x020	UART_MDR1	UART_MDR1	UART_MDR1	UART_MDR1	UART_MDR1	UART_MDR1
0x024	UART_MDR2	UART_MDR2	UART_MDR2	UART_MDR2	UART_MDR2	UART_MDR2
0x028	UART_SFLSR	UART_TXFLL	UART_SFLSR	UART_TXFLL	UART_SFLSR	UART_TXFLL

(1) MSR_SPR mode is active (see Section 23.3.4.7.1.2, *Register Access Submode*)
(2) TCR_TLR mode is active (see Section 23.3.4.7.1.2, *Register Access Submode*)
(3) XOFF mode is active (see Section 23.3.4.7.1.2, *Register Access Submode*)

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Table 23-155. UART/IrDA/CIR Register Access Mode Overview (continued)

Address Offset	Registers					
	Configuration Mode A		Configuration Mode B		Operational Mode	
	Read	Write	Read	Write	Read	Write
0x02C	UART_RESUME	UART_TXFLH	UART_RESUME	UART_TXFLH	UART_RESUME	UART_TXFLH
0x030	UART_SFREGL	UART_RXFLL	UART_SFREGL	UART_RXFLL	UART_SFREGL	UART_RXFLL
0x034	UART_SFREGH	UART_RXFLH	UART_SFREGH	UART_RXFLH	UART_SFREGH	UART_RXFLH
0x038	UART_UASR	–	UART_UASR	–	UART_BLR	UART_BLR
0x03C	–	–	–	–	UART_ACREG	UART_ACREG
0x040	UART_SCR	UART_SCR	UART_SCR	UART_SCR	UART_SCR	UART_SCR
0x044	UART_SSR	–	UART_SSR	–	UART_SSR	–
0x048	–	–	–	–	UART_EBLR	UART_EBLR
0x050	UART_MVR	–	UART_MVR	–	UART_MVR	–
0x054	UART_SYSC	UART_SYSC	UART_SYSC	UART_SYSC	UART_SYSC	UART_SYSC
0x058	UART_SYSS	–	UART_SYSS	–	UART_SYSS	–
0x05C	UART_WER	UART_WER	UART_WER	UART_WER	UART_WER	UART_WER
0x060	UART_CFPS	UART_CFPS	UART_CFPS	UART_CFPS	UART_CFPS	UART_CFPS
0x064	UART_RXFIFO_LVL	UART_RXFIFO_LVL	UART_RXFIFO_LVL	UART_RXFIFO_LVL	UART_RXFIFO_LVL	UART_RXFIFO_LVL
0x068	UART_TXFIFO_LVL	UART_TXFIFO_LVL	UART_TXFIFO_LVL	UART_TXFIFO_LVL	UART_TXFIFO_LVL	UART_TXFIFO_LVL
0x06C	UART_IER2	UART_IER2	UART_IER2	UART_IER2	UART_IER2	UART_IER2
0x070	UART_ISR2	UART_ISR2	UART_ISR2	UART_ISR2	UART_ISR2	UART_ISR2
0x074	UART_FREQ_SEL	UART_FREQ_SEL	UART_FREQ_SEL	UART_FREQ_SEL	UART_FREQ_SEL	UART_FREQ_SEL
0x080	UART_MDR3	UART_MDR3	UART_MDR3	UART_MDR3	UART_MDR3	UART_MDR3
0x084	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD

23.3.4.7.2 UART/IrDA (SIR, MIR, FIR)/CIR Mode Selection

To select a mode, set the UARTi.UART_MDR1[2:0] MODE_SELECT bit field (see Table 23-156).

Table 23-156. UART Mode Selection

Value	Mode
0x0:	UART 16x mode
0x1:	SIR mode (UART3 only)
0x2:	UART 16x auto-baud
0x3:	UART 13x mode
0x4:	MIR mode (UART3 only)
0x5:	FIR mode (UART3 only)
0x6:	CIR mode (UART3 only)

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MODE_SELECT is effective when the module is in operational mode (see Section 23.3.4.7.1, *Register Access Modes*).

23.3.4.7.2.1 Registers Available for the UART Function

Only the registers listed in Table 23-157 are used for the UART function.

Table 23-157. UART Mode Register Overview[1] [2]

Address Offset	Registers					
	Configuration Mode A		Configuration Mode B		Operational Mode	
	Read	Write	Read	Write	Read	Write
0x000	UART_DLL	UART_DLL	UART_DLL	UART_DLL	UART_RHR	UART_THR
0x004	UART_DLH	UART_DLH	UART_DLH	UART_DLH	UART_IER(UART)	UART_IER(UART)
0x008	UART_IIR	UART_FCR	UART_EFR[4]	UART_EFR[4]	UART_IIR(UART)	UART_FCR(UART)
0x00C	UART_LCR	UART_LCR	UART_LCR	UART_LCR	UART_LCR	UART_LCR
0x010	UART_MCR	UART_MCR	UART_XON1_ADDR1	UART_XON1_ADDR1	UART_MCR	UART_MCR
0x014	UART_LSR(UART)	–	UART_XON2_ADDR2	UART_XON2_ADDR2	UART_LSR(UART)	–
0x018	UART_MSR/UART_TCR	UART_TCR	UART_XOFF1/UART_TCR	UART_XOFF1/UART_TCR	UART_MSR/UART_TCR	UART_TCR
0x01C	UART_TLR/UART_SPR	UART_TLR/UART_SPR	UART_TLR/UART_XOFF2	UART_TLR/UART_XOFF2	UART_TLR/UART_SPR	UART_TLR/UART_SPR
0x020	UART_MDR1	UART_MDR1[2:0]	UART_MDR1[2:0]	UART_MDR1[2:0]	UART_MDR1[2:0]	UART_MDR1[2:0]
0x024	UART_MDR2	UART_MDR2	UART_MDR2	UART_MDR2	UART_MDR2	UART_MDR2
0x028	–	–	–	–	–	–
0x02C	–	–	–	–	–	–
0x030	–	–	–	–	–	–
0x034	–	–	–	–	–	–
0x038	UART_UASR	–	UART_UASR	–	–	–
0x03C	–	–	–	–	–	–
0x040	UART_SCR	UART_SCR	UART_SCR	UART_SCR	UART_SCR	UART_SCR
0x044	UART_SSR	–	UART_SSR	–	UART_SSR	–
0x048	–	–	–	–	–	–
0x050	UART_MVR	–	UART_MVR	–	UART_MVR	–
0x054	UART_SYSC	UART_SYSC	UART_SYSC	UART_SYSC	UART_SYSC	UART_SYSC
0x058	UART_SYSS	–	UART_SYSS	–	UART_SYSS	–
0x05C	UART_WER	UART_WER	UART_WER	UART_WER	UART_WER	UART_WER
0x060	–	–	–	–	–	–
0x064	UART_RXFIFO_LVL	UART_RXFIFO_LVL	UART_RXFIFO_LVL	UART_RXFIFO_LVL	UART_RXFIFO_LVL	UART_RXFIFO_LVL
0x068	UART_TXFIFO_LVL	UART_TXFIFO_LVL	UART_TXFIFO_LVL	UART_TXFIFO_LVL	UART_TXFIFO_LVL	UART_TXFIFO_LVL
0x06C	UART_IER2	UART_IER2	UART_IER2	UART_IER2	UART_IER2	UART_IER2
0x070	UART_ISR2	UART_ISR2	UART_ISR2	UART_ISR2	UART_ISR2	UART_ISR2
0x074	UART_FREQ_SEL	UART_FREQ_SEL	UART_FREQ_SEL	UART_FREQ_SEL	UART_FREQ_SEL	UART_FREQ_SEL
0x080	UART_MDR3	UART_MDR3	UART_MDR3	UART_MDR3	UART_MDR3	UART_MDR3

(1) REGISTER_NAME(UART) notation indicates that the register exists for other functions (IrDA or CIR), but fields have different meanings for other functions (described separately in Section 23.3.6, *UART/IrDA/CIR Register Manual*).

(2) REGISTER_NAME[m:n] notation indicates that only register bits numbered m to n apply to the UART function.

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Table 23-157. UART Mode Register Overview[1] [2] (continued)

Address Offset	Registers					
	Configuration Mode A		Configuration Mode B		Operational Mode	
	Read	Write	Read	Write	Read	Write
0x084	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD

23.3.4.7.2.2 Registers Available for the IrDA Function (UART3 Only)

Only the registers listed in Table 23-158 are used for the IrDA function.

Table 23-158. IrDA Mode Register Overview[1] [2]

Address Offset	Registers					
	Configuration Mode A		Configuration Mode B		Operational Mode	
	Read	Write	Read	Write	Read	Write
0x000	UART_DLL	UART_DLL	UART_DLL	UART_DLL	UART_RHR	UART_THR
0x004	UART_DLH	UART_DLH	UART_DLH	UART_DLH	UART_IER(IrDA)	UART_IER(IrDA)
0x008	UART_IIR	UART_FCR	UART_EFR[4]	UART_EFR[4]	UART_IIR(IrDA)	UART_FCR(IrDA)
0x00C	UART_LCR[7]	UART_LCR[7]	UART_LCR[7]	UART_LCR[7]	UART_LCR[7]	UART_LCR[7]
0x010	–	–	UART_XON1_ADDR1	UART_XON1_ADDR1	–	–
0x014	UART_LSR(IrDA)	–	UART_XON2_ADDR2	UART_XON2_ADDR2	UART_LSR(IrDA)	–
0x018	UART_MSR/UART_TCR	UART_TCR	UART_TCR	UART_TCR	UART_MSR/UART_TCR	UART_TCR
0x01C	UART_TLR/UART_SPR	UART_TLR/UART_SPR	UART_TLR	UART_TLR	UART_TLR/UART_SPR	UART_TLR/UART_SPR
0x020	UART_MDR1	UART_MDR1	UART_MDR1	UART_MDR1	UART_MDR1	UART_MDR1
0x024	UART_MDR2	UART_MDR2	UART_MDR2	UART_MDR2	UART_MDR2	UART_MDR2
0x028	UART_SFLSR	UART_TXFLL	UART_SFLSR	UART_TXFLL	UART_SFLSR	UART_TXFLL
0x02C	UART_RESUME	UART_TXFLH	UART_RESUME	UART_TXFLH	UART_RESUME	UART_TXFLH
0x030	UART_SFREGL	UART_RXFLL	UART_SFREGL	UART_RXFLL	UART_SFREGL	UART_RXFLL
0x034	UART_SFREGH	UART_RXFLH	UART_SFREGH	UART_RXFLH	UART_SFREGH	UART_RXFLH
0x038	–	–	–	–	UART_BLR	UART_BLR
0x03C	–	–	–	–	UART_ACREG	UART_ACREG
0x040	UART_SCR	UART_SCR	UART_SCR	UART_SCR	UART_SCR	UART_SCR
0x044	UART_SSR	–	UART_SSR	–	UART_SSR	–
0x048	–	–	–	–	UART_EBLR	UART_EBLR
0x050	UART_MVR	–	UART_MVR	–	UART_MVR	–
0x054	UART_SYSC	UART_SYSC	UART_SYSC	UART_SYSC	UART_SYSC	UART_SYSC
0x058	UART_SYSS	–	UART_SYSS	–	UART_SYSS	–
0x05C	UART_WER[6:4]	UART_WER[6:4]	UART_WER[6:4]	UART_WER[6:4]	UART_WER[6:4]	UART_WER[6:4]
0x060	–	–	–	–	–	–

(1) REGISTER_NAME(UART) notation indicates that the register exists for other functions (IrDA or CIR), but fields have different meanings for other functions (described separately in Section 23.3.6, *UART/IrDA/CIR Register Manual*).

(2) REGISTER_NAME[m:n] notation indicates that only register bits numbered m to n apply to the UART function.

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Table 23-158. IrDA Mode Register Overview[1] [2] (continued)

Address Offset	Registers					
	Configuration Mode A		Configuration Mode B		Operational Mode	
	Read	Write	Read	Write	Read	Write
0x064	UART_RXFIFO_LVL	UART_RXFIFO_LVL	UART_RXFIFO_LVL	UART_RXFIFO_LVL	UART_RXFIFO_LVL	UART_RXFIFO_LVL
0x068	UART_TXFIFO_LVL	UART_TXFIFO_LVL	UART_TXFIFO_LVL	UART_TXFIFO_LVL	UART_TXFIFO_LVL	UART_TXFIFO_LVL
0x06C	UART_IER2	UART_IER2	UART_IER2	UART_IER2	UART_IER2	UART_IER2
0x070	UART_ISR2	UART_ISR2	UART_ISR2	UART_ISR2	UART_ISR2	UART_ISR2
0x074	UART_FREQ_SEL	UART_FREQ_SEL	UART_FREQ_SEL	UART_FREQ_SEL	UART_FREQ_SEL	UART_FREQ_SEL
0x080	UART_MDR3	UART_MDR3	UART_MDR3	UART_MDR3	UART_MDR3	UART_MDR3
0x084	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD

23.3.4.7.2.3 Registers Available for the CIR Function (UART3 Only)

Only the registers listed in Table 23-159 are used for the CIR function.

Table 23-159. CIR Mode Register Overview[1] [2]

Address Offset	Registers					
	Configuration Mode A		Configuration Mode B		Operational Mode	
	Read	Write	Read	Write	Read	Write
0x000	UART_DLL	UART_DLL	UART_DLL	UART_DLL	–	UART_THR
0x004	UART_DLH	UART_DLH	UART_DLH	UART_DLH	UART_IER(CIR)	UART_IER(CIR)
0x008	UART_IIR	UART_FCR	UART_EFR	UART_EFR	UART_IIR(CIR)	UART_FCR(CIR)
0x00C	UART_LCR	UART_LCR[7]	UART_LCR[7]	UART_LCR[7]	UART_LCR[7]	UART_LCR[7]
0x010	–	–	–	–	–	–
0x014	UART_LSR(IrDA)	–	–	–	UART_LSR(IrDA)	–
0x018	UART_MSR/UART_TCR	UART_TCR	UART_TCR	UART_TCR	UART_MSR/UART_TCR	UART_TCR
0x01C	UART_TLR/UART_SPR	UART_TLR/UART_SPR	UART_TLR	UART_TLR	UART_TLR/UART_SPR	UART_TLR/UART_SPR
0x020	UART_MDR1[3:0]	UART_MDR1[3:0]	UART_MDR1[3:0]	UART_MDR1[3:0]	UART_MDR1[3:0]	UART_MDR1[3:0]
0x024	UART_MDR2	UART_MDR2	UART_MDR2	UART_MDR2	UART_MDR2	UART_MDR2
0x028	–	–	–	–	–	–
0x02C	UART_RESUME	–	UART_RESUME	–	UART_RESUME	–
0x030	–	–	–	–	–	–
0x034	–	–	–	–	–	–
0x038	–	–	–	–	–	–
0x03C	–	–	–	–	UART_ACREG	UART_ACREG
0x040	UART_SCR	UART_SCR	UART_SCR	UART_SCR	UART_SCR	UART_SCR
0x044	UART_SSR	–	UART_SSR	–	UART_SSR	–

(1) REGISTER_NAME(UART) notation indicates that the register exists for other functions (IrDA or CIR), but fields have different meanings for other functions (described separately in Section 23.3.6, *UART/IrDA/CIR Register Manual*).

(2) REGISTER_NAME[m:n] notation indicates that only register bits numbered m to n apply to the UART function.

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Table 23-159. CIR Mode Register Overview[1] [2] (continued)

Address Offset	Registers					
	Configuration Mode A		Configuration Mode B		Operational Mode	
	Read	Write	Read	Write	Read	Write
0x048	–	–	–	–	UART_EBLR	UART_EBLR
0x050	UART_MVR	–	UART_MVR	–	UART_MVR	–
0x054	UART_SYSC	UART_SYSC	UART_SYSC	UART_SYSC	UART_SYSC	UART_SYSC
0x058	UART_SYSS	–	UART_SYSS	–	UART_SYSS	–
0x05C	UART_WER[6:4]	UART_WER[6:4]	UART_WER[6:4]	UART_WER[6:4]	UART_WER[6:4]	UART_WER[6:4]
0x060	UART_CFPS	UART_CFPS	UART_CFPS	UART_CFPS	UART_CFPS	UART_CFPS
0x064	UART_RXFIFO_LVL	UART_RXFIFO_LVL	UART_RXFIFO_LVL	UART_RXFIFO_LVL	UART_RXFIFO_LVL	UART_RXFIFO_LVL
0x068	UART_TXFIFO_LVL	UART_TXFIFO_LVL	UART_TXFIFO_LVL	UART_TXFIFO_LVL	UART_TXFIFO_LVL	UART_TXFIFO_LVL
0x06C	UART_IER2	UART_IER2	UART_IER2	UART_IER2	UART_IER2	UART_IER2
0x070	UART_ISR2	UART_ISR2	UART_ISR2	UART_ISR2	UART_ISR2	UART_ISR2
0x074	UART_FREQ_SEL	UART_FREQ_SEL	UART_FREQ_SEL	UART_FREQ_SEL	UART_FREQ_SEL	UART_FREQ_SEL
0x080	UART_MDR3	UART_MDR3	UART_MDR3	UART_MDR3	UART_MDR3	UART_MDR3
0x084	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD

23.3.4.8 Protocol Formatting

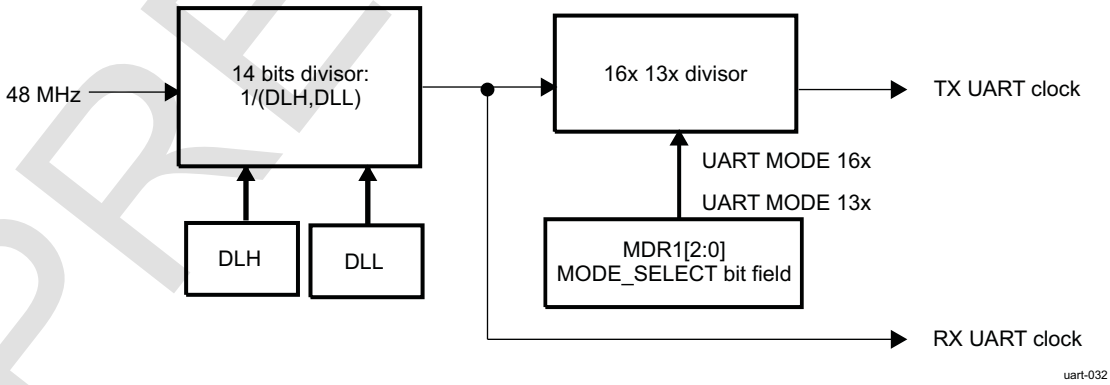
23.3.4.8.1 UART Mode

23.3.4.8.1.1 UART Clock Generation: Baud Rate Generation

The UART function contains a programmable baud generator and a set of fixed dividers that divide the 48-MHz clock input down to the expected baud rate.

Figure 23-83 shows the baud rate generator and associated controls.

Figure 23-83. Baud Rate Generation



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CAUTION

Before initializing or modifying clock parameter controls (UARTi.UART_DLH, UARTi.UART_DLL), MODE_SELECT = DISABLE (UARTi.UART_MDR1[2:0]) must be set to 0x7. Failure to observe this rule can result in unpredictable module behavior.

23.3.4.8.1.2 Choosing the Appropriate Divisor Value

Two divisor values are:

- UART 16x mode: Divisor value = Operating frequency/(16x baud rate)
- UART 13x mode: Divisor value = Operating frequency/(13x baud rate)

Table 23-160 describes the UART baud rate settings.

Table 23-160. UART Baud Rate Settings (48-MHz Clock)

Baud Rate	Baud Multiple	DLH,DLL (Decimal)	DLH,DLL (Hex)	Actual Baud Rate	Error (%)
0.3 kbps	16x	10000	0x27, 0x10	0.3 kbps	0
0.6 kbps	16x	5000	0x13, 0x88	0.6 kbps	0
1.2 kbps	16x	2500	0x09, 0xC4	1.2 kbps	0
2.4 kbps	16x	1250	0x04, 0xE2	2.4 kbps	0
4.8 kbps	16x	625	0x02, 0x71	4.8 kbps	0
9.6 kbps	16x	312	0x01, 0x38	9.6153 kbps	+0.16
14.4 kbps	16x	208	0x00, 0xD0	14.423 kbps	+0.16
19.2 kbps	16x	156	0x00, 0x9C	19.231 kbps	+0.16
28.8 kbps	16x	104	0x00, 0x68	28.846 kbps	+0.16
38.4 kbps	16x	78	0x00, 0x4E	38.462 kbps	+0.16
57.6 kbps	16x	52	0x00, 0x34	57.692 kbps	+0.16
115.2 kbps	16x	26	0x00, 0x1A	115.38 kbps	+0.16
230.4 kbps	16x	13	0x00, 0x0D	230.77 kbps	+0.16
460.8 kbps	13x	8	0x00, 0x08	461.54 kbps	+0.16
921.6 kbps	13x	4	0x00, 0x04	923.08 kbps	+0.16
1.843 Mbps	13x	2	0x00, 0x02	1.846 Mbps	+0.16
3.6884 Mbps	13x	1	0x00, 0x01	3.6923 Mbps	+0.16

23.3.4.8.1.3 UART Data Formatting

The UART can use hardware flow control to manage transmission and reception. Hardware flow control significantly reduces software overhead and increases system efficiency by automatically controlling serial data flow using the RTS output and CTS input signals.

The UART is enhanced with the autobauding function. In control mode, autobauding lets the speed, the number of bits per character, and the parity selected be set automatically.

23.3.4.8.1.3.1 Frame Formatting

When autobauding is not used, frame format attributes must be defined in the UARTi.UART_LCR register.

Character length is specified using the UARTi.UART_LCR[1:0] CHAR_LENGTH bit field.

The number of stop-bits is specified using the UARTi.UART_LCR[2] NB_STOP bit.

The parity bit is programmed using the UARTi.UART_LCR[5:3] PARITY_EN, PARITY_TYPE_1, and PARITY_TYPE_2 bit fields (see Table 23-161).

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Table 23-161. UART Parity Bit Encoding

PARITY_EN	PARITY_TYPE_1	PARITY_TYPE_2	Parity
0	N/A	N/A	No parity
1	0	0	Odd parity
1	1	0	Even parity
1	0	1	Forced 1
1	1	1	Forced 0

23.3.4.8.1.3.2 Hardware Flow Control

Hardware flow control is composed of auto-CTS and auto-RTS. Auto-CTS and auto-RTS can be enabled and disabled independently by programming the UARTi.UART_EFR[7:6] AUTO_CTS_EN and AUTO_RTS_EN bit fields, respectively.

With auto-CTS, uarti_cts must be active before the module can transmit data.

Auto-RTS activates the uarti_rts output only when there is enough room in the RX FIFO to receive data. It deactivates the uarti_rts output when the RX FIFO is sufficiently full. The HALT and RESTORE trigger levels in the UARTi.UART_TCR register determine the levels at which uarti_rts is activated and deactivated.

If auto-CTS and auto-RTS are enabled, data transmission does not occur unless the RX FIFO has empty space. Thus, overrun errors are eliminated during hardware flow control. If auto-CTS and auto-RTS are not enabled, overrun errors occur if the transmit data rate exceeds the RX FIFO latency.

- Auto-RTS:

  Auto-RTS data flow control originates in the receiver block. The RX FIFO trigger levels used in auto-RTS are stored in the UARTi.UART_TCR register. uarti_rts is active if the RX FIFO level is below the HALT trigger level in the UARTi.UART_TCR[3:0] RX_FIFO_TRIG_HALT bit field. When the RX FIFO HALT trigger level is reached, uarti_rts is deasserted. The sending device (for example, another UART) can send an additional byte after the trigger level is reached because it may not recognize the deassertion of RTS until it begins sending the additional byte.

  uarti_rts is automatically reasserted when the RX FIFO reaches the RESUME trigger level programmed by the UARTi.UART_TCR[7:4] RX_FIFO_TRIG_START bit field. This reassertion requests the sending device to resume transmission.

  In this case, uarti_rts is an active-low signal.

- Auto-CTS:

  The transmitter circuitry checks uarti_cts before sending the next data byte. When uarti_cts is active, the transmitter sends the next byte. To stop the transmitter from sending the next byte, uarti_cts must be deasserted before the middle of the last stop-bit currently sent.

  The auto-CTS function reduces interrupts to the host system. When auto-CTS flow control is enabled, the uarti_cts state changes do not have to trigger host interrupts because the device automatically controls its own transmitter. Without auto-CTS, the transmitter sends any data present in the transmit FIFO, and a receiver overrun error can result.

  In this case, uarti_cts is an active-low signal.

23.3.4.8.1.3.3 Software Flow Control

Software flow control is enabled through the enhanced feature register (UARTi.UART_EFR) and the modem control register (UARTi.UART_MCR). Different combinations of software flow control can be enabled by setting different combinations of the UARTi.UART_EFR[3:0] bit field (see Table 23-162).

Two other enhanced features relate to software flow control:

- XON any function (UARTi.UART_MCR[5]): Operation resumes after receiving any character after the XOFF character is recognized. If special character detect is enabled and special character is received after XOFF1, it does not resume transmission. The special character is stored in the RX FIFO.

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NOTE: The XON-any character is written into the RX FIFO even if it is a software flow character.

- Special character (UARTi.UART_EFR[5]): Incoming data is compared to XOFF2. When the special character is detected, the XOFF interrupt (UARTi.UART_IIR[4]) is set, but it does not halt transmission. The XOFF interrupt is cleared by a read of UARTi.UART_IIR. The special character is transferred to the RX FIFO. Special character does not work with XON2, XOFF2, or sequential XOFFs.

Table 23-162. UART_EFR[3:0] Software Flow Control Options

Bit 3	Bit 2	Bit 1	Bit 0	TX, RX Software Flow Controls
0	0	X	X	No transmit flow control
1	0	X	X	Transmit XON1, XOFF1
0	1	X	X	Transmit XON2, XOFF2
1	1	X	X	Transmit XON1, XON2: XOFF1, XOFF2(1)
X	X	0	0	No receive flow control
X	X	1	0	Receiver compares XON1, XOFF1
X	X	0	1	Receiver compares XON2, XOFF2
X	X	1	1	Receiver compares XON1, XON2: XOFF1, XOFF2(1)

(1) In these cases, the XON1 and XON2 characters or the XOFF1 and XOFF2 characters must be transmitted/received sequentially with XON1/XOFF1 followed by XON2/XOFF2.
XON1 is defined in the UARTi.UART_XON1_ADDR1[7:0] XON_WORD1 bit field. XON2 is defined in the UARTi.UART_XON2_ADDR2[7:0] XON_WORD2 bit field.
XOFF1 is defined in the UARTi.UART_XOFF1[7:0] XOFF_WORD1 bit field. XOFF2 is defined in the UARTi.UART_XOFF2[7:0] XOFF_WORD2 bit field.

23.3.4.8.1.3.3.1 Receive (RX)

When software flow control operation is enabled, the UART compares incoming data with XOFF1/2 programmed characters (in certain cases, XOFF1 and XOFF2 must be received sequentially). When the correct XOFF characters are received, transmission stops after transmission of the current character completes. Detection of XOFF also sets the UARTi.UART_IIR[4] bit (if enabled by UARTi.UART_IER[5]) and causes the interrupt line to go low.

To resume transmission, an XON1/2 character must be received (in certain cases, XON1 and XON2 must be received sequentially). When the correct XON characters are received, the UARTi.UART_IIR[4] bit is cleared and the XOFF interrupt disappears.

NOTE: When a parity, framing, or break error occurs while receiving a software flow control character, this character is treated as normal data and is written to the RX FIFO.

When XON-any and special character detect are disabled and software flow control is enabled, no valid XON or XOFF characters are written to the RX FIFO. For example, when UARTi.UART_EFR[1:0] = 0x2, if XON1 and XOFF1 characters are received, they are not written to the RX FIFO.

When pairs of software flow characters are programmed to be received sequentially (UARTi.UART_EFR[1:0] = 0x3), the software flow characters are not written to the RX FIFO if they are received sequentially. However, received XON1/XOFF1 characters must be written to the RX FIFO if the subsequent character is not XON2/XOFF2.

23.3.4.8.1.3.3.2 Transmit (TX)

Two XOFF1 characters are transmitted when the RX FIFO passes the trigger level programmed by UARTi.UART_TCR[3:0]. As soon as the RX FIFO reaches the trigger level programmed by UARTi.UART_TCR[7:4], two XON1 characters are sent, so the data transfer recovers.

NOTE: If software flow control is disabled after an XOFF character is sent, the module transmits XON characters automatically to enable normal transmission.

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The transmission of XOFF(s)/XON(s) follows the same protocol as transmission of an ordinary byte from the TX FIFO. This means that even if the word length is 5, 6, or 7 characters, the 5, 6, or 7 LSBs of XOFF1/2 and XON1/2 are transmitted. The 5, 6, or 7 bits of a character are seldom transmitted, but this function is included to maintain compatibility with earlier designs.

It is assumed that software flow control and hardware flow control are never enabled simultaneously.

23.3.4.8.1.3.4 Autobauding Modes

In autobauding mode, the UART can extract transfer characteristics (speed, length, and parity) from an "at" (AT) command (ASCII code). These characteristics are used to receive data after an AT and to send data.

The following AT commands are valid:

AT	DATA	CR
at	DATA	CR
A/		
a/		

A line break during the acquisition of the sequence AT is not recognized, and an echo function is not implemented in hardware.

A/ and a/ are not used to extract characteristics, but they must be recognized because of their special meaning. A/ or a/ is used to instruct the software to repeat the last received AT command; therefore, an a/ always follows an AT, and transfer characteristics are not expected to change between an AT and an a/.

When a valid AT is received, AT and all subsequent data, including the final CR (0x0D), are saved to the RX FIFO. The autobaud state-machine waits for the next valid AT command. If an a/ (A/) is received, the a/ (A/) is saved in the RX FIFO and the state-machine waits for the next valid AT command.

On the first successful detection of the baud rate, the UART activates an interrupt to signify that the AT (upper or lower case) sequence is detected. The UARTi.UART_UASR register reflects the correct settings for the baud rate detected. Interrupt activity can continue in this fashion when a subsequent character is received. Therefore, it is recommended that the software enable the RHR interrupt when using the autobaud mode.

The following settings are detected in autobaud mode with a module clock of 48 MHz:

- Speed:
  - 115.2K baud
  - 57.6K baud
  - 38.4K baud
  - 28.8K baud
  - 19.2K baud
  - 14.4K baud
  - 9.6K baud
  - 4.8K baud
  - 2.4K baud
  - 1.2K baud
- Length: 7 or 8 bits
- Parity: Odd, even, or space

NOTE: The combination of 7-bit character plus space parity is not supported.

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Autobauding mode is selected when the UARTi.UART_MDR1[2:0] MODE_SELECT bit field is set to 0x2. In UART autobauding mode, UARTi.UART_DLL, UARTi.UART_DLH, and UARTi.UART_LCR[5:0] bit field settings are not used; instead, UART_UASR is updated with the configuration detected by the autobauding logic.

UART_UASR Autobauding Status Register Use

This register is used to set up transmission according to the characteristics of the previous reception instead of the UARTi.UART_LCR, UARTi.UART_DLL, and UARTi.UART_DLH registers when the UART is in autobauding mode.

To reset the autobauding hardware (to start a new AT detection) or to set the UART in standard mode (no autobaud), the UARTi.UART_MDR1[2:0] MODE_ SELECT bit field must be set to reset state (0x7) and then to the UART in autobauding mode (0x2) or to the UART in standard mode (0x0).

Use limitation:

- Only 7- and 8-bit characters (5- and 6-bit not supported)
- 7-bit character with space parity not supported
- Baud rate between 1200 and 115,200 bps (10 possibilities)

23.3.4.8.1.3.5 Error Detection

When the UARTi.UART_LSR register is read, the UARTi.UART_LSR[4:2] bit field reflects the error bits (BI: break condition, FE: framing error, PE: parity error) of the character at the top of the RX FIFO (the next character to be read). Therefore, reading the UARTi.UART_LSR register and then reading the UARTi.UART_RHR register identifies errors in a character.

Reading the UARTi.UART_RHR register updates the BI, FE, and PE bits (see Table 23-146 for the UART mode interrupts).

The UARTi.UART_LSR[7] RX_FIFO_STS bit is set when there is an error in the RX FIFO and is cleared only when no errors remain in the RX FIFO.

NOTE: Reading the UARTi.UART_LSR register does not cause an increment of the RX FIFO read pointer. The RX FIFO read pointer is incremented by reading the UARTi.UART_RHR register.

Reading the UARTi.UART_LSR register clears the OE bit if it is set (see Table 23-146 for the UART mode interrupts).

23.3.4.8.1.3.6 Overrun During Receive

Overrun during receive occurs if the RX state-machine tries to write data into the RX FIFO when it is already full. When overrun occurs, the device interrupts the MPU with the UARTi.UART_IIR[5:1] IT_TYPE bit field set to 0x3 (receiver line status error) and discards the remaining portion of the frame.

Overrun also causes an internal flag to be set, which disables further reception. Before the next frame can be received, the MPU must:

- Reset the RX FIFO.
- Read the UARTi.UART_RESUME register, which clears the internal flag.

23.3.4.8.1.3.7 Time-Out and Break Conditions

23.3.4.8.1.3.7.1 Time-Out Counter

An RX idle condition is detected when the receiver line (uarti_rx) is high for a time that equals 4x the programmed word length + 12 bits. uarti_rx is sampled midway through each bit.

For sleep mode, the counter is reset when there is activity on uarti_rx.

For the time-out interrupt, the counter counts only when there is data in the RX FIFO, and the count is reset when there is activity on uarti_rx or when the UARTi.UART_RHR register is read.

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23.3.4.8.1.3.7.2 Break Condition

When a break condition occurs, uarti_tx is pulled low. A break condition is activated by setting the UARTi.UART_LCR[6] BREAK_EN bit. The break condition is not aligned on word stream (a break condition can occur in the middle of a character). The only way to send a break condition on a full character is:

1. Reset the TX FIFO (if enabled).
2. Wait for the transmit shift register to empty (the UARTi.UART_LSR[6] TX_SR_E bit is set to 1).
3. Take a guard time according to stop-bit definition.
4. Set the BREAK_EN bit to 1.

The break condition is asserted while the BREAK_EN bit is set to 1.

The time-out counter and break condition apply only to UART modem operation and not to IrDA/CIR mode operation.

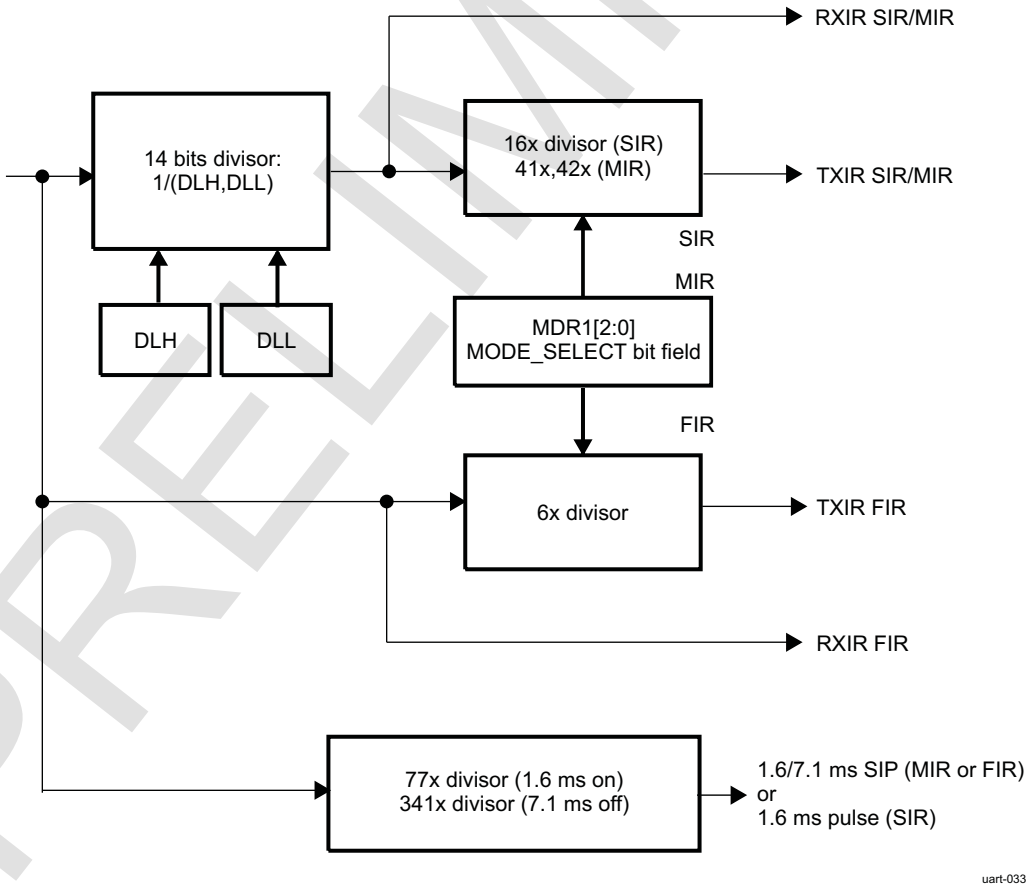
23.3.4.8.2 IrDA Mode (UART3 Only)

23.3.4.8.2.1 IrDA Clock Generation: Baud Generator

The IrDA function contains a programmable baud generator and a set of fixed dividers that divide the 48-MHz clock input down to the expected baud rate.

Figure 23-84 shows the baud rate generator and associated controls.

Figure 23-84. Baud Rate Generator



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CAUTION

Before initializing or modifying clock parameter controls (UARTi.UART_DLH, UARTi.UART_DLL), MODE_SELECT=DISABLE (UARTi.UART_MDR1[2:0]) must be set to 0x7). Failure to observe this rule can result in unpredictable module behavior.

23.3.4.8.2.2 Choosing the Appropriate Divisor Value

Three divisor values are:

- SIR mode: Divisor value = Operating frequency/(16x baud rate)
- MIR mode: Divisor value = Operating frequency/(41x/42x baud rate)
- FIR mode: Divisor value = None

Table 23-163 lists the IrDA baud rate settings.

Table 23-163. IrDA Baud Rate Settings

Baud Rate	IR Mode	Baud Multiple	Encoding	DLH, DLL (Decimal)	Actual Baud Rate	Error (%)	Source Jitter (%)	Pulse Duration
2.4 kbps	SIR	16x	3/16	1250	2.4 kbps	0	0	78.1 µs
9.6 kbps	SIR	16x	3/16	312	9.6153 kbps	+0.16	0	19.5 µs
19.2 kbps	SIR	16x	3/16	156	19.231 kbps	+0.16	0	9.75 µs
38.4 kbps	SIR	16x	3/16	78	38.462 kbps	+0.16	0	4.87 µs
57.6 kbps	SIR	16x	3/16	52	57.692 kbps	+0.16	0	3.25 µs
115.2 kbps	SIR	16x	3/16	26	115.38 kbps	+0.16	0	1.62 µs
0.576 Mbps	MIR	41x/42x	1/4	2	0.5756 Mbps(1)	0	+1.63/–0.80	416 ns
1.152 Mbps	MIR	41x/42x	1/4	1	1.1511 Mbps(1)	0	+1.63/–0.80	208 ns
4 Mbps	FIR	6x	4 PPM	–	4 Mbps	0	0	125 ns

(1) Average value

NOTE: Baud rate error and source jitter table values do not include 48-MHz reference clock error and jitter.

23.3.4.8.2.3 IrDA Data Formatting

The methods described in this section apply to all IrDA modes (SIR, MIR, and FIR).

23.3.4.8.2.3.1 IR RX Polarity Control

The UART3.UART_MDR2[6] IRRXINVERT bit provides the flexibility to invert the uart3_rx_irrx pin in the UART to ensure that the protocol at the output of the transceiver has the same polarity at module level. By default, the uart3_rx_irrx pin is inverted because most transceivers invert the IR receive pin.

23.3.4.8.2.3.2 IrDA Reception Control

The module can transmit and receive data, but when the device is transmitting, the IR RX circuitry is automatically disabled by hardware.

Operation of the uart3_rx_irrx input can be disabled by the UART3.UART_ACREG[5] DIS_IR_RX bit.

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23.3.4.8.2.3.3 IR Address Checking

In all IR modes, when address checking is enabled, only frames intended for the device are written to the RX FIFO. This restriction avoids receiving frames not meant for this device in a multipoint infrared environment. It is possible to program two frame addresses that the UART IrDA receives, with the UART3.UART_XON1_ADDR1[7:0] XON_WORD1 and UART3.UART_XON2_ADDR2[7:0] XON_WORD2 bit fields.

Setting the UART_EFR[0] bit to 1 selects address1 checking. Setting the UART_EFR[1] bit to 1 selects address2 checking. Setting the UART_EFR[1:0] bit field to 0 disables all address checking operations. If both bits are set, the incoming frame is checked for private and public addresses.

If address checking is disabled, all received frames write to the RX FIFO.

23.3.4.8.2.3.4 Frame Closing

A transmission frame can be terminated in two ways:

- Frame-length method: Set the UART3.UART_MDR1[7] FRAME_END_MODE bit to 0. The MPU writes the value of the frame length to the UART3.UART_TXFLH and UART3.UART_TXFLL registers. The device automatically attaches end flags to the frame when the number of bytes transmitted equals the value of the frame length.
- Set-EOT bit method: Set the FRAME_END_MODE bit to 1. The MPU writes 1 to the UART3.UART_ACREG[0] EOT bit just before it writes the last byte to the TX FIFO. When the MPU writes the last byte to the TX FIFO, the device internally sets the tag bit for that character in the TX FIFO. As the TX state-machine reads data from the TX FIFO, it uses this tag-bit information to attach end flags and correctly terminate the frame.

23.3.4.8.2.3.5 Store and Controlled Transmission

In store and controlled transmission (SCT) mode, the MPU starts writing data to the TX FIFO. Then, after writing a part of a frame (for a bigger frame) or an entire frame (a small frame; that is, a supervisory frame), the MPU writes 1 to the UART3.UART_ACREG[2] SCTX_EN bit (deferred TX start) to start transmission.

SCT mode is enabled by setting the UART3.UART_MDR1[5] SCT bit to 1. This transmission method differs from normal mode, in which data transmission starts immediately after data is written to the TX FIFO. SCT mode is useful for sending short frames without TX underrun.

23.3.4.8.2.3.6 Error Detection

When the UART3.UART_LSR register is read, the UART3.UART_LSR[4:2] bit field reflects the error bits [FL, CRC, ABORT] of the frame at the top of the STATUS FIFO (the next frame status to be read).

The error is triggered by an interrupt (for IrDA mode interrupts, see Table 23-147). The STATUS FIFO must be read until empty (a maximum of eight reads is required).

23.3.4.8.2.3.7 Underrun During Transmission

Underrun during transmission occurs when the TX FIFO is empty before the end of the frame is transmitted. When underrun occurs, the device closes the frame with end flags but attaches an incorrect CRC value. The receiving device detects a CRC error and discards the frame; it can then ask for a retransmission.

Underrun also causes an internal flag to be set, which disables additional transmissions. Before the next frame can be transmitted, the MPU must:

- Reset the TX FIFO.
- Read the UART3.UART_RESUME register, which clears the internal flag.

This function can be disabled by the UART3.UART_ACREG[4] DIS_TX_UNDERRUN bit, compensated by the extension of the stop-bit in transmission if the TX FIFO is empty.

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23.3.4.8.2.3.8 Overrun During Receive

Overrun during receive for the IrDA mode has the same function as that for the UART mode (see Section 23.3.4.8.1.3.6, *Overrun During Receive*).

23.3.4.8.2.3.9 Status FIFO

In IrDA modes, a status FIFO records the received frame status. When a complete frame is received, the length of the frame and the error bits associated with the frame are written to the status FIFO.

Reading the UART3.UART_SFREGH[3:0] MSB and UART3.UART_SFREGL[3:0] (LSB) bit fields obtains the frame length. The frame error status is read in the UART3.UART_SFLSR register. Reading the UART3.UART_SFLSR register increments the status FIFO read pointer. Because the status FIFO is eight entries deep, it can hold the status of eight frames.

The MPU uses the frame-length information to locate the frame boundary in the received frame data. The MPU can screen bad frames using the error status information and can later request the sender to resend only the bad frames.

This status FIFO can be used effectively in DMA mode because the MPU must be interrupted only when the programmed status FIFO trigger level is reached, not each time a frame is received.

23.3.4.8.2.4 SIR Mode Data Formatting

This section provides specific instructions for SIR mode programming.

23.3.4.8.2.4.1 Abort Sequence

The transmitter can prematurely close a frame (abort) by sending the sequence 0x7DC1. The abort pattern closes the frame without a CRC field or an ending flag.

A transmission frame can be aborted by setting the UART3.UART_ACREG[1] ABORT_EN bit to 1. When this bit is set to 1, 0x7D and 0xC1 are transmitted and the frame is not terminated with CRC or stop flags.

When a 0x7D character followed immediately by a 0xC1 character is received without transparency, the receiver treats a frame as an aborted frame.

CAUTION

When the TX FIFO is not empty and the UART3.UART_MDR1[5] SCT bit is set to 1, the UART IrDA starts a new transfer with data of a previous frame when the aborted frame is sent. Therefore, the TX FIFO must be reset before sending an aborted frame.

23.3.4.8.2.4.2 Pulse Shaping

SIR mode supports the 3/16 or the 1.6-µs pulse duration methods in receive and transmit. The UART3.UART_ACREG[7] PULSE_TYPE bit selects the pulse width method in the transmit mode.

23.3.4.8.2.4.3 SIR Free Format Programming

The SIR FF mode is selected by setting the module in the UART mode (UART3.UART_MDR1[2:0] MODE_SELECT = 0x0) and the UART3.UART_MDR2[3] UART_PULSE bit to 1 to allow pulse shaping.

Because the bit format stays the same, some UART mode configuration registers must be set at specific values:

- UART3.UART_LCR[1:0] CHAR_LENGTH bit field = 0x3 (8 data bits)
- UART3.UART_LCR[2] NB_STOP bit = 0x0 (1 stop-bit)
- UART3.UART_LCR[3] PARITY_EN bit = 0x0 (no parity)

The UART mode interrupts are used for the SIR FF mode, but many are not relevant (XOFF, RTS, CTS, modem status register, etc.).

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23.3.4.8.2.5 MIR and FIR Mode Data Formatting

This section describes common instructions for FIR and MIR mode programming.

At the end of a frame reception, the MPU reads the line status register (UART3.UART_LSR) to detect errors in the received frame.

When the UART3.UART_MDR1[6] SIP_MODE bit is set to 1, the TX state-machine always sends one SIP at the end of a transmission frame. However, when the SIP_MODE bit is set to 0, SIP transmission depends on the UART3.UART_ACREG[3] SEND_SIP bit.

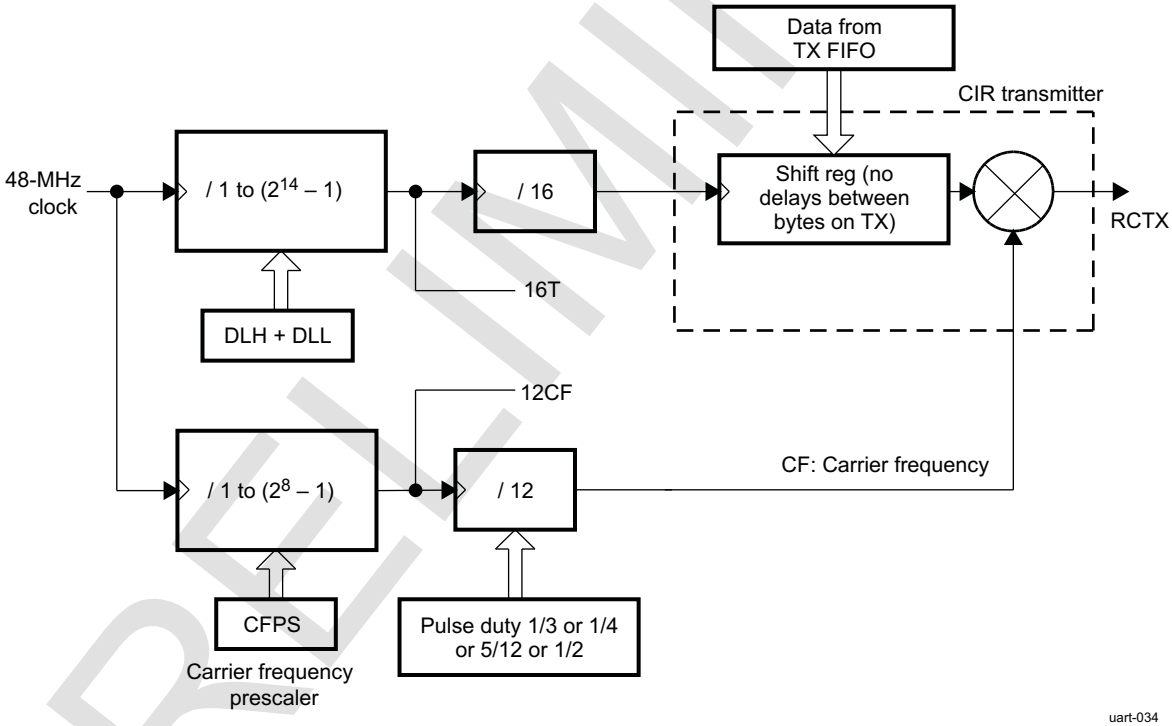
The MPU can set the SEND_SIP bit at least once every 500 ms. The advantage of this approach over the default approach is that the TX state-machine does not have to send the SIP at the end of each frame, thus reducing the overhead required.

23.3.4.8.3 CIR Mode (UART3 Only)

23.3.4.8.3.1 CIR Mode Clock Generation

Depending on the encoding method (variable pulse distance/biphase), the MPU must develop a data structure that combines 1 and 0 with a *t* period to encode the complete frame to transmit. This can then be transmitted to the infrared output with a modulation method, as shown in Figure 23-85.

Figure 23-85. CIR Mode Block Components



Based on the requested modulation frequency, the UART3.UART_CFPS register must be set with the correct dividing value to provide an accurate pulse frequency:

Dividing value = (FCLK/12)/MODfreq

Where:

FCLK = System clock frequency (48 MHz)

12 = Real value of baud multiple

MODfreq = Effective frequency of the modulation (MHz)

Example: For a targeted modulation frequency of 36 kHz, the value of UART_CFPS must be set to 0x7 (decimal), which provides a modulation frequency of 36.04 kHz.

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NOTE: The UART3.UART_CFPS register starts with a reset value of 105 (decimal), which translates to a frequency of 38.1 kHz.

The duty cycle of these pulses is user-defined by the pulse duty register bits in the UART3.UART_MDR2 register. Table 23-164 shows the duty cycle.

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Table 23-164. Duty Cycle

UART_MDR2[5:4]	Duty Cycle (High-Level)
00	1/4
01	1/3
10	5/12
11	1/2

23.3.4.8.3.2 CIR Data Formatting

The methods described in this section apply to all CIR modes.

23.3.4.8.3.2.1 IR RX Polarity Control

The IR RX polarity control for CIR mode has the same function as that for IrDA mode (see Section 23.3.4.8.2.3.1, *IR RX Polarity Control*).

23.3.4.8.3.2.2 CIR Transmission

In transmission, the MPU software must exercise an element of real-time control to transmit data packets, each of which must be emitted at a constant delay from the start-bits of each individual packet. Thus, when sending a series of packets, the packet-to-packet delay must respect a specific delay. Two methods can be used to control this delay:

- Filling the TX FIFO with a number of zero bits that are transmitted with a *t* period
- Using an external system timer to control the delay between each start-of-frame or between the end of a frame and the start of the next one. This can be performed by:
  - Controlling the start of the frame using the UART3.UART_MDR1[5] SCT bit and the UART3.UART_ACREG[2] SCTX_EN bit, depending on the timer status
  - Using the UART3.UART_IIR[5] TX_STATUS_IT interrupt bit to preload the next frame in the TX FIFO and to control the start of the timer (in case of control delay between the end of a frame and the start of the next frame)

23.3.5 UART/IrDA/CIR Basic Programming Model

23.3.5.1 UART Programming Model

23.3.5.1.1 Quick Start

This section describes the procedure for operating the UART with FIFO and DMA or interrupts. This three-part procedure ensures the quick start of the UART. It does not cover every UART feature.

The first programming model covers software reset of the UART. The second programming model describes FIFO and DMA configuration. The last programming model describes protocol, baud rate, and interrupt configuration.

NOTE: Each programming model can be used independently of the other two; for instance, reconfiguring the FIFOs and DMA settings only.

Each programming model can be executed starting from any UART register access mode (register modes, submodes, and other register dependencies). However, if the UART register access mode is known before executing the programming model, some steps that enable or restore register access are optional. For more information, see Section 23.3.4.7.1, *Register Access Modes*.

23.3.5.1.1.1 Software Reset

To clear the UART registers, perform the following steps:

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1. Initiate a software reset:
   Set the UARTi.UART_SYSC[1] SOFTRESET bit to 1.
2. Wait for the end of the reset operation:
   Poll the UARTi.UART_SYSS[0] RESETDONE bit until it equals 1.

23.3.5.1.1.2 FIFOs and DMA Settings

To enable and configure the receive and transmit FIFOs and program the DMA mode, perform the following steps:

1. Switch to register configuration mode B to access the UARTi.UART_EFR register:
   (a) Save the current UARTi.UART_LCR register value.
   (b) Set the UARTi.UART_LCR register value to 0x00BF.
2. Enable register submode TCR_TLR to access the UARTi.UART_TLR register (part 1 of 2):
   (a) Save the UARTi.UART_EFR[4] ENHANCED_EN value.
   (b) Set the UARTi.UART_EFR[4] ENHANCED_EN bit to 1.
3. Switch to register configuration mode A to access the UARTi.UART_MCR register:
   Set the UARTi.UART_LCR register value to 0x0080.
4. Enable register submode TCR_TLR to access the UARTi.UART_TLR register (part 2 of 2):
   (a) Save the UARTi.UART_MCR[6] TCR_TLR value.
   (b) Set the UARTi.UART_MCR[6] TCR_TLR bit to 1.
5. Enable the FIFO; load the new FIFO triggers (part 1 of 3) and the new DMA mode (part 1 of 2):
   Set the following bits to the desired values:
   - UARTi.UART_FCR[7:6] RX_FIFO_TRIG
   - UARTi.UART_FCR[5:4] TX_FIFO_TRIG
   - UARTi.UART_FCR[3] DMA_MODE
   - UARTi.UART_FCR[0] FIFO_ENABLE (0: Disable the FIFO; 1: Enable the FIFO)

   NOTE: The UARTi.UART_FCR register is not readable.
6. Switch to register configuration mode B to access the UARTi.UART_EFR register:
   Set the UARTi.UART_LCR register value to 0x00BF.
7. Load the new FIFO triggers (part 2 of 3):
   Set the following bits to the desired values:
   - UARTi.UART_TLR[7:4] RX_FIFO_TRIG_DMA
   - UARTi.UART_TLR[3:0] TX_FIFO_TRIG_DMA
8. Load the new FIFO triggers (part 3 of 3) and the new DMA mode (part 2 of 2):
   Set the following bits to the desired values:
   - UARTi.UART_SCR[7] RX_TRIG_GRANU1
   - UARTi.UART_SCR[6] TX_TRIG_GRANU1
   - UARTi.UART_SCR[2:1] DMA_MODE_2
   - UARTi.UART_SCR[0] DMA_MODE_CTL
9. Restore the UARTi.UART_EFR[4] ENHANCED_EN value saved in Step 2a.
10. Switch to register configuration mode A to access the UARTi.UART_MCR register:
    Set the UARTi.UART_LCR register value to 0x0080.
11. Restore the UARTi.UART_MCR[6] TCR_TLR value saved in Step 4a.
12. Restore the UARTi.UART_LCR value saved in Step 1a.

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Triggers are used to generate interrupt and DMA requests. See Section 23.3.4.6.1.1, *Transmit FIFO Trigger,* to choose the following values:

- UARTi.UART_FCR[5:4] TX_FIFO_TRIG
- UARTi.UART_TLR[3:0] TX_FIFO_TRIG_DMA
- UARTi.UART_SCR[6] TX_TRIG_GRANU1

Triggers are used to generate interrupt and DMA requests. See Section 23.3.4.6.1.2, *Receive FIFO Trigger*, to choose the following values:

- UARTi.UART_FCR[7:6] RX_FIFO_TRIG
- UARTi.UART_TLR[7:4] RX_FIFO_TRIG_DMA
- UARTi.UART_SCR[7] RX_TRIG_GRANU1

DMA mode enables DMA requests. See Section 23.3.4.6.4, *FIFO DMA Mode Operation*, to choose the following values:

- UARTi.UART_FCR[3] DMA_MODE
- UARTi.UART_SCR[2:1] DMA_MODE_2
- UARTi.UART_SCR[0] DMA_MODE_CTL

23.3.5.1.1.3 Protocol, Baud Rate, and Interrupt Settings

To program the protocol, baud rate, and interrupt settings, perform the following steps:

1. Disable UART to access the UARTi.UART_DLL and UARTi.UART_DLH registers:
   Set the UARTi.UART_MDR1[2:0] MODE_SELECT bit field to 0x7.
2. Switch to register configuration mode B to access the UARTi.UART_EFR register:
   Set the UARTi.UART_LCR register value to 0x00BF.
3. Enable access to the UARTi.UART_IER[7:4] bit field:
   (a) Save the UARTi.UART_EFR[4] ENHANCED_EN value.
   (b) Set the UARTi.UART_EFR[4] ENHANCED_EN bit to 1.
4. Switch to register operational mode to access the UARTi.UART_IER register:
   Set the UARTi.UART_LCR register value to 0x0000.
5. Clear the UARTi.UART_IER register (set the UARTi.UART_IER[4] SLEEP_MODE bit to 0 to change the UARTi.UART_DLL and UARTi.UART_DLH registers). Set the UARTi.UART_IER register value to 0x0000.
6. Switch to register configuration mode B to access the UARTi.UART_DLL and UARTi.UART_DLH registers:
   Set the UARTi.UART_LCR register value to 0x00BF.
7. Load the new divisor value:
   Set the UARTi.UART_DLL[7:0] CLOCK_LSB and UARTi.UART_DLH[5:0] CLOCK_MSB bit fields to the desired values.
8. Switch to register operational mode to access the UARTi.UART_IER register:
   Set the UARTi.UART_LCR register value to 0x0000.
9. Load the new interrupt configuration (0: Disable the interrupt; 1: Enable the interrupt):
   Set the following bits to the desired values:
   - UARTi.UART_IER[7] CTS_IT
   - UARTi.UART_IER[6] RTS_IT
   - UARTi.UART_IER[5] XOFF_IT
   - UARTi.UART_IER[4] SLEEP_MODE
   - UARTi.UART_IER[3] MODEM_STS_IT
   - UARTi.UART_IER[2] LINE_STS_IT
   - UARTi.UART_IER[1] THR_IT

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- UARTi.UART_IER[0] RHR_IT

10. Switch to register configuration mode B to access the UARTi.UART_EFR register:

    Set the UARTi.UART_LCR register value to 0x00BF.

11. Restore the UARTi.UART_EFR[4] ENHANCED_EN value saved in Step 3a.
12. Load the new protocol formatting (parity, stop-bit, character length) and switch to register operational mode:

    Set the UARTi.UART_LCR[7] DIV_EN bit to 0.

    Set the UARTi.UART_LCR[6] BREAK_EN bit to 0.

    Set the following bits to the desired values:

    - UARTi.UART_LCR[5] PARITY_TYPE_2
    - UARTi.UART_LCR[4] PARITY_TYPE_1
    - UARTi.UART_LCR[3] PARITY_EN
    - UARTi.UART_LCR[2] NB_STOP
    - UARTi.UART_LCR[1:0] CHAR_LENGTH

13. Load the new UART mode:

    Set the UARTi.UART_MDR1[2:0] MODE_SELECT bit field to the desired value.

See Section 23.3.4.8.1.2, *Choosing the Appropriate Divisor Value*, to choose the following values:

- UARTi.UART_DLL[7:0] CLOCK_LSB
- UARTi.UART_DLH[5:0] CLOCK_MSB
- UARTi.UART_MDR1[2:0] MODE_SELECT

See Section 23.3.4.8.1.3.1, *Frame Formatting*, to choose the following values:

- UARTi.UART_LCR[5] PARITY_TYPE_2
- UARTi.UART_LCR[4] PARITY_TYPE_1
- UARTi.UART_LCR[3] PARITY_EN
- UARTi.UART_LCR[2] NB_STOP
- UARTi.UART_LCR[1:0] CHAR_LENGTH

23.3.5.1.2 Hardware and Software Flow Control Configuration

This section describes the programming steps to enable and configure hardware and software flow control. Hardware and software flow control cannot be used at the same time.

NOTE: Each programming model can be executed starting from any UART register access mode (register modes, submodes, and other register dependencies). However, if the UART register access mode is known before executing the programming model, some steps that enable or restore register access are optional. For more information, see Section 23.3.4.7.1, *Register Access Modes*.

23.3.5.1.2.1 Hardware Flow Control Configuration

To enable and configure hardware flow control, perform the following steps:

1. Switch to register configuration mode A to access the UARTi.UART_MCR register:
   (a) Save the current UARTi.UART_LCR register value.
   (b) Set the UARTi.UART_LCR register value to 0x0080.
2. Enable register submode TCR_TLR to access the UARTi.UART_TCR register (part 1 of 2):
   (a) Save the UARTi.UART_MCR[6] TCR_TLR value.
   (b) Set the UARTi.UART_MCR[6] TCR_TLR bit to 1.
3. Switch to register configuration mode B to access the UARTi.UART_EFR register:

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Set the UARTi.UART_LCR register value to 0x00BF.

4. Enable register submode TCR_TLR to access the UARTi.UART_TCR register (part 2 of 2):
   (a) Save the UARTi.UART_EFR[4] ENHANCED_EN value.
   (b) Set the UARTi.UART_EFR[4] ENHANCED_EN bit to 1.
5. Load the new start and halt trigger values for hardware flow control:
   Set the following bits to the desired values:
   - UARTi.UART_TCR[7:4] AUTO_RTS_START
   - UARTi.UART_TCR[3:0] AUTO_RTS_HALT
6. Enable or disable receive and transmit hardware flow control mode and restore the UARTi.UART_EFR[4] ENHANCED_EN value saved in Step 4a.
   Set the following bits to the desired values:
   - UARTi.UART_EFR[7] AUTO_CTS_EN (0: Disable; 1: Enable)
   - UARTi.UART_EFR[6] AUTO_RTS_EN (0: Disable; 1: Enable)

   Restore the UARTi.UART_EFR[4] ENHANCED_EN bit to the saved value.
7. Switch to register configuration mode A to access the UARTi.UART_MCR register:
   Set the UARTi.UART_LCR register value to 0x0080.
8. Restore the UARTi.UART_MCR[6] TCR_TLR value saved in Step 2a.
9. Restore the UARTi.UART_LCR value saved in Step 1a.

See Section 23.3.4.8.1.3.2, *Hardware Flow Control*, to choose the following values:

- UARTi.UART_EFR[7] AUTO_CTS_EN
- UARTi.UART_EFR[6] AUTO_RTS_EN
- UARTi.UART_TCR[7:4] AUTO_RTS_START
- UARTi.UART_TCR[3:0] AUTO_RTS_HALT

23.3.5.1.2.2 Software Flow Control Configuration

To enable and configure software flow control, perform the following steps:

1. Switch to register configuration mode B to access the UARTi.UART_EFR register.
   (a) Save the current UARTi.UART_LCR register value.
   (b) Set the UARTi.UART_LCR register value to 0x00BF.
2. Enable register submode XOFF to access the UARTi.UART_XOFF1 and UARTi.UART_XOFF2 registers:
   (a) Save the UARTi.UART_EFR[4] ENHANCED_EN value.
   (b) Set the UARTi.UART_EFR[4] ENHANCED_EN bit to 0.
3. Load the new software flow control characters:
   Set the following bits to the desired values:
   - UARTi.UART_XON1_ADDR1[7:0] XON_WORD1
   - UARTi.UART_XON2_ADDR2[7:0] XON_WORD2
   - UARTi.UART_XOFF1[7:0] XOFF_WORD1
   - UARTi.UART_XOFF2[7:0] XOFF_WORD2
4. Enable access to the UARTi.UART_MCR[7:5] bit field and enable register submode TCR_TLR to access the UARTi.UART_TCR register (part 1 of 2):
   Set the UARTi.UART_EFR[4] ENHANCED_EN bit to 1.
5. Switch to register configuration mode A to access the UARTi.UART_MCR register:
   Set the UARTi.UART_LCR register value to 0x0080.
6. Enable register submode TCR_TLR to access the UARTi.UART_TCR register (part 2 of 2) and enable or disable XON any function:

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(a) Save the UARTi.UART_MCR[6] TCR_TLR value.

(b) Set the UARTi.UART_MCR[6] TCR_TLR bit to 1.

(c) Set the UARTi.UART_MCR[5] XON_EN bit to the desired value (0: Disable; 1: Enable).

7. Switch to register configuration mode B to access the UARTi.UART_EFR register:
   Set the UARTi.UART_LCR register value to 0x00BF.
8. Load the new start and halt trigger values for software flow control:
   Set the following bits to the desired values:
   - UARTi.UART_TCR[7:4] AUTO_RTS_START
   - UARTi.UART_TCR[3:0] AUTO_RTS_HALT
9. Enable or disable special character function and load the new software flow control mode and restore the UARTi.UART_EFR[4] ENHANCED_EN value saved in Step 2a:
   Set the following bits to the desired values:
   - UARTi.UART_EFR[5] SPEC_CHAR (0: Disable; 1: Enable)
   - UARTi.UART_EFR[3:0] SW_FLOW_CONTROL

   Restore the UARTi.UART_EFR[4] ENHANCED_EN bit to the saved value.
10. Switch to register configuration mode A to access the UARTi.UART_MCR register:
    Set the UARTi.UART_LCR register value to 0x0080.
11. Restore the UARTi.UART_MCR[6] TCR_TLR bit value saved in Step 6a.
12. Restore the UARTi.UART_LCR value saved in Step 1a.

See Section 23.3.4.8.1.3.3, *Software Flow Control*, to choose the following values:

- UARTi.UART_EFR[5] SPEC_CHAR
- UARTi.UART_EFR[3:0] SW_FLOW_CONTROL
- UARTi.UART_TCR[7:4] AUTO_RTS_START
- UARTi.UART_TCR[3:0] AUTO_RTS_HALT
- UARTi.UART_XON1_ADDR1[7:0] XON_WORD1
- UARTi.UART_XON2_ADDR2[7:0] XON_WORD2
- UARTi.UART_XOFF1[7:0] XOFF_WORD1
- UARTi.UART_XOFF2[7:0] XOFF_WORD2

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23.3.5.2 IrDA Programming Model (UART3 Only)

23.3.5.2.1 SIR Mode

23.3.5.2.1.1 Receive

The following programming model explains how to program the module to receive an IrDA frame with parity forced to 1, baud rate = 112.5KB, FIFOs disabled, 2 stop-bits, and 8-bit word length:

1. Disable the UART before accessing the UARTi.UART_DLL and UARTi.UART_DLH registers:
   Set the UARTi.UART_MDR1[2:0] MODE_SELECT bit field to 0x7.
2. Grant access to the UART_DLL and UART_DLH registers (the UART_LCR[7] DIV_EN bit = 1):
   UART3.UART_LCR = 0x80 (Data format is unaffected by the use and settings of the UART3.UART_LCR register in IrDA mode.)
3. Load the new baud rate (115.2 kbps):
   UART3.UART_DLL = 0x1A
   UART3.UART_DLH = 0x00
4. Set SIR mode:
   UART3.UART_MDR1[2:0] MODE_SELECT = 0x1
5. Disable access to the UART_DLL and UART_DLH registers and switch to register operational mode:
   UART3.UART_LCR = 0x00.
6. Optional: Enable the RHR interrupt:
   UART3.UART_IER[0] RHR_IT = 0x1

23.3.5.2.1.2 Transmit

The following programming model explains how to program the module to transmit an IrDA 6-byte frame with no parity, baud rate = 112.5 kbps, FIFOs disabled, 3/16 encoding, 2 stop-bits, and 7-bit word length:

1. Disable the UART before accessing the UARTi.UART_DLL and UARTi.UART_DLH registers:
   Set the UART_MDR1[2:0] MODE_SELECT bit field to 0x7.
2. Grant access to the UART_EFR register:
   UART3.UART_LCR = 0xBF
3. Enable the enhanced features (the UART_EFR[4] ENAHNCED_EN bit = 1):
   Set the UART3.UART_EFR register value to 0x10.
4. Grant access to the UART_DLL and UART_DLH registers (the UART_LCR[7] DIV_EN bit = 1):
   UART3.UART_LCR = 0x80 (Data format is unaffected by the use and settings of the UART3.UART_LCR register in IrDA mode.)
5. Load the new baud rate (115.2 kbps):
   UART3.UART_DLL = 0x1A
   UART3.UART_DLH = 0x00
6. Set SIR mode (the UART_MDR1[2:0] MODE_SELECT bit field = 0x1):
   UART3.UART_MDR1 = 0x01
7. Disable access to the UART_DLL and UART_DLH registers and switch to register operational mode:
   UART3.UART_LCR = 0x00.
8. Force DTR output to active:
   UART3.UART_MCR[0] DTR = 1
9. Optional: Enable the THR interrupt:
   UART3.UART_IER[1] THR_IT = 1
10. Set transmit frame length to 6 bytes:
    UART3.UART_TXFLL = 0x06
11. Set 7 starts of frame transmission:
    UART3.UART_EBLR = 0x08
12. Optional: Set SIR pulse width to be 1.6 us:
    UART3.UART_ACREG[7] PULSE_TYPE = 1
13. Load the UART_THR register with the data to be transmitted.

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23.3.5.2.2 MIR Mode

23.3.5.2.2.1 Receive

The following programming model explains how to program the module to receive an IrDA frame with no parity, baud rate = 1.152 Mpbs, and FIFOs disabled.

1. Disable the UART before accessing the UARTi.UART_DLL and UARTi.UART_DLH registers:
   Set the UARTi.UART_MDR1[2:0] MODE_SELECT bit field to 0x7.
2. Grant access to the UART_DLL and UART_DLH registers (UART_LCR[7] DIV_EN bit = 1):
   UART3.UART_LCR = 0x80 (Data format is unaffected by the use and settings of the UART3.UART_LCR register in IrDA mode.)
3. Load the new baud rate (1.152 Mpbs):
   UART3.UART_DLL = 0x01
   UART3.UART_DLH = 0x00
4. Set MIR mode:
   UART3.UART_MDR1[2:0] MODE_SELECT = 0x4
5. Disable access to the UART_DLL and UART_DLH registers and switch to register operational mode:
   UART3.UART_LCR = 0x00
6. Force DTR output to active (UART_MCR[0] DTR = 1):
   Force RTS output to active (UART_MCR[1] RTS = 1).
   UART3.UART_MCR = 0x3
7. Optional: Enable the RHR interrupt:
   UART3.UART_IER[0] RHR_IT = 1

23.3.5.2.2.2 Transmit

The following programming model explains how to program the module to transmit an IrDA 60-byte frame with no parity, baud rate = 1.152 Mpbs, and FIFOs disabled:

1. Disable the UART before accessing the UARTi.UART_DLL and UARTi.UART_DLH registers:
   Set the UARTi.UART_MDR1[2:0] MODE_SELECT bit field to 0x7.
2. Grant access to the UART_DLL and UART_DLH registers (UART_LCR[7] DIV_EN bit = 1):
   UART3.UART_LCR = 0x80 (Data format is unaffected by the use and settings of the UART3.UART_LCR register in IrDA mode.)
3. Load the new baud rate (1.152 Mpbs):
   UART3.UART_DLL = 0x01
   UART3.UART_DLH = 0x00
4. Set MIR mode:
   UART3.UART_MDR1[2:0] MODE_SELECT = 0x4
5. Disable access to the UART_DLL and UART_DLH registers and switch to register operational mode:
   UART3.UART_LCR = 0x00
6. Force DTR output to active:
   UART3.UART_MCR[0] DTR = 1
7. Optional: Enable the THR interrupt:
   UART3.UART_IER[1] THR_IT = 1
8. Set the frame length to 60 bytes:
   UART3.UART_TXFLL = 0x3C
9. Optional: Transmit eight additional starts of frame (MIR mode requires two starts):
   UART3.UART_EBLR = 0x08
10. SIP is sent at the end of transmission:
    UART3.UART_ACREG[3] = 1
11. Load the UART_THR register with the data to be transmitted.

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23.3.5.2.3 FIR Mode

23.3.5.2.3.1 Receive

The following programming model explains how to program the module to receive the IrDA frame with no parity, baud rate = 4 Mbps, FIFOs enabled, 8-bit word length.

1. Disable the UART before accessing the UART3.UART_DLL and UART3.UART_DLH registers:
   Set the UART3.UART_MDR1[2:0] MODE_SELECT bit field to 0x7.
2. Grant access to the UART_DLL and UART_DLH registers (UART_LCR[7] DIV_EN bit = 1):
   UART3.UART_LCR = 0x80 (Data format is unaffected by the use and settings of the UART3.UART_LCR register in IrDA mode.)
3. FIFO clear and enable:
   UART3.UART_FCR = 0x7 (TX/RX FIFO trigger: UART_FCR[7:6] and UART_FCR[5:4])
   UART3.UART_LCR[7] = 0
4. Set FIR mode:
   UART3.UART_MDR1[2:0] MODE_SELECT = 0x5
5. Set frame length:
   UART3.UART_RXFLL = 0xA (Data + CRC + STOP)
6. Disable access to the UART3.UART_DLL registers and UART3.UART_DLH and switch to register operational mode:
   UART3.UART_LCR[7] DIV_EN = 0x0
7. Optional: Enable the RHR interrupt:
   UART3.UART_IER[0] RHR_IT = 1

23.3.5.2.3.2 Transmit

The following programming model explains how to program the module to transmit an IrDA 4-byte frame with no parity, baud rate = 4 Mbps, FIFOs enabled, and 8-bit word length.

1. Disable the UART before accessing the UART3.UART_DLL and UART3.UART_DLH registers:
   Set the UART3.UART_MDR1[2:0] MODE_SELECT bit field to 0x7.
2. Grant access to EFR_REG:
   UART3.UART_LCR = 0xBF
3. Enable the enhanced features (EFR_REG[4] ENAHNCED_EN = 0x1):
   UART3.UART_EFR = 0x10
4. FIFO clear and enable:
   UART3.UART_FCR = 0x7 (TX/RX FIFO trigger: UART_FCR[7:6] and UART_FCR[5:4]).
   UART3.UART_LCR[7] = 0
5. Set FIR mode and enable auto-SIP mode:
   UART3.UART_MDR1 = 0x45
6. Set frame length:
   UART3.UART_TXFLL = 0x4
   UART3.UART_TXFLH = 0x0
   UART3.UART_RXFLL = 0xA (Data + CRC + STOP)
   UART3.UART_RXFLH = 0x0
7. Force DTR output to active:
   UART3.UART_MCR[0] DTR = 0x1
8. Optional: Enable the THR interrupt:
   UART3.UART_IER[1] THR_IT = 0x1
9. Optional: Transmit eight additional starts of frame (MIR mode requires two starts):
   UART3.UART_EBLR = 0x08
10. SIP is sent at the end of transmission:
    UART3.UART_ACREG[3] = 1
11. Load the UART_THR register with the data to be transmitted.

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23.3.6 UART/IrDA/CIR Register Manual

23.3.6.1 UART/IrDA/CIR Instance Summary

Table 23-165 shows the base address and address space for the UART/IrDA/CIR module instances.

Table 23-165. UART/IrDA/CIR Instance Summary

Module Name	Base Address	Size
UART1[(1)]	0x4806 A000	1KB
UART2[(1)]	0x4806 C000	1KB
UART3[(2)]	0x4802 0000	1KB
UART4[(1)]	0x4806 E000	1KB

(1) UART mode only
(2) UART, IrDA, or CIR mode

23.3.6.2 UART/IrDA/CIR Registers

23.3.6.2.1 UART/IrDA/CIR Register Summary

Table 23-166. UART/IrDA/CIR Register Mapping Summary (UART1 and UART2)

Register Name	Type	Register Width (Bits)	Address Offset	UART1 Base Address	UART2 Base Address
UART_THR	W	32	0x0000 0000	0x4806 A000	0x4806 C000
UART_RHR	R	32	0x0000 0000	0x4806 A000	0x4806 C000
UART_DLL	RW	32	0x0000 0000	0x4806 A000	0x4806 C000
UART_IER	RW	32	0x0000 0004	0x4806 A004	0x4806 C004
UART_IIR	R	32	0x0000 0008	0x4806 A008	0x4806 C008
UART_DLH	RW	32	0x0000 0004	0x4806 A004	0x4806 C004
UART_FCR	W	32	0x0000 0008	0x4806 A008	0x4806 C008
UART_EFR	RW	32	0x0000 0008	0x4806 A008	0x4806 C008
UART_LCR	RW	32	0x0000 000C	0x4806 A00C	0x4806 C00C
UART_XON1_ADDR1	RW	32	0x0000 0010	0x4806 A010	0x4806 C010
UART_MCR	RW	32	0x0000 0010	0x4806 A010	0x4806 C010
UART_LSR	R	32	0x0000 0014	0x4806 A014	0x4806 C014
UART_XON2_ADDR2	RW	32	0x0000 0014	0x4806 A014	0x4806 C014
UART_TCR	RW	32	0x0000 0018	0x4806 A018	0x4806 C018
UART_XOFF1	RW	32	0x0000 0018	0x4806 A018	0x4806 C018
UART_MSR	R	32	0x0000 0018	0x4806 A018	0x4806 C018
UART_SPR	RW	32	0x0000 001C	0x4806 A01C	0x4806 C01C
UART_TLR	RW	32	0x0000 001C	0x4806 A01C	0x4806 C01C
UART_XOFF2	RW	32	0x0000 001C	0x4806 A01C	0x4806 C01C
UART_MDR1	RW	32	0x0000 0020	0x4806 A020	0x4806 C020
UART_MDR2	RW	32	0x0000 0024	0x4806 A024	0x4806 C024
UART_SFLSR	R	32	0x0000 0028	0x4806 A028	0x4806 C028
UART_TXFLL	W	32	0x0000 0028	0x4806 A028	0x4806 C028
UART_RESUME	R	32	0x0000 002C	0x4806 A02C	0x4806 C02C
UART_TXFLH	W	32	0x0000 002C	0x4806 A02C	0x4806 C02C
UART_SFREGL	R	32	0x0000 0030	0x4806 A030	0x4806 C030
UART_RXFLL	W	32	0x0000 0030	0x4806 A030	0x4806 C030
UART_SFREGH	R	32	0x0000 0034	0x4806 A034	0x4806 C034
UART_RXFLH	W	32	0x0000 0034	0x4806 A034	0x4806 C034

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Table 23-166. UART/IrDA/CIR Register Mapping Summary (UART1 and UART2) (continued)

Register Name	Type	Register Width (Bits)	Address Offset	UART1 Base Address	UART2 Base Address
UART_BLR	RW	32	0x0000 0038	0x4806 A038	0x4806 C038
UART_UASR	R	32	0x0000 0038	0x4806 A038	0x4806 C038
UART_ACREG	RW	32	0x0000 003C	0x4806 A03C	0x4806 C03C
UART_SCR	RW	32	0x0000 0040	0x4806 A040	0x4806 C040
UART_SSR	R	32	0x0000 0044	0x4806 A044	0x4806 C044
UART_EBLR	RW	32	0x0000 0048	0x4806 A048	0x4806 C048
UART_MVR	R	32	0x0000 0050	0x4806 A050	0x4806 C050
UART_SYSC	RW	32	0x0000 0054	0x4806 A054	0x4806 C054
UART_SYSS	R	32	0x0000 0058	0x4806 A058	0x4806 C058
UART_WER	RW	32	0x0000 005C	0x4806 A05C	0x4806 C05C
UART_CFPS	RW	32	0x0000 0060	0x4806 A060	0x4806 C060
UART_RXFIFO_LVL	R	32	0x0000 0064	0x4806 A064	0x4806 C064
UART_TXFIFO_LVL	R	32	0x0000 0068	0x4806 A068	0x4806 C068
UART_IER2	RW	32	0x0000 006C	0x4806 A06C	0x4806 C06C
UART_ISR2	RW	32	0x0000 0070	0x4806 A070	0x4806 C070
UART_FREQ_SEL	RW	32	0x0000 0074	0x4806 A074	0x4806 C074
UART_MDR3	RW	32	0x0000 0080	0x4806 A080	0x4806 C080
UART_TX_DMA_THRESHOLD	RW	32	0x0000 0084	0x4806 A084	0x4806 C084

Table 23-167. UART/IrDA/CIR Register Mapping Summary (UART3 and UART4)

Register Name	Type	Register Width (Bits)	Address Offset	UART3 Base Address	UART4 Base Address
UART_THR	W	32	0x0000 0000	0x4802 0000	0x4806 E000
UART_RHR	R	32	0x0000 0000	0x4802 0000	0x4806 E000
UART_DLL	RW	32	0x0000 0000	0x4802 0000	0x4806 E000
UART_IER	RW	32	0x0000 0004	0x4802 0004	0x4806 E004
UART_IIR	R	32	0x0000 0008	0x4802 0008	0x4806 E008
UART_DLH	RW	32	0x0000 0004	0x4802 0004	0x4806 E004
UART_FCR	W	32	0x0000 0008	0x4802 0008	0x4806 E008
UART_EFR	RW	32	0x0000 0008	0x4802 0008	0x4806 E008
UART_LCR	RW	32	0x0000 000C	0x4802 000C	0x4806 E00C
UART_XON1_ADDR1	RW	32	0x0000 0010	0x4802 0010	0x4806 E010
UART_MCR	RW	32	0x0000 0010	0x4802 0010	0x4806 E010
UART_LSR	R	32	0x0000 0014	0x4802 0014	0x4806 E014
UART_XON2_ADDR2	RW	32	0x0000 0014	0x4802 0014	0x4806 E014
UART_TCR	RW	32	0x0000 0018	0x4802 0018	0x4806 E018
UART_XOFF1	RW	32	0x0000 0018	0x4802 0018	0x4806 E018
UART_MSR	R	32	0x0000 0018	0x4802 0018	0x4806 E018
UART_SPR	RW	32	0x0000 001C	0x4802 001C	0x4806 E01C
UART_TLR	RW	32	0x0000 001C	0x4802 001C	0x4806 E01C
UART_XOFF2	RW	32	0x0000 001C	0x4802 001C	0x4806 E01C
UART_MDR1	RW	32	0x0000 0020	0x4802 0020	0x4806 E020
UART_MDR2	RW	32	0x0000 0024	0x4802 0024	0x4806 E024
UART_SFLSR	R	32	0x0000 0028	0x4802 0028	0x4806 E028
UART_TXFLL	W	32	0x0000 0028	0x4802 0028	0x4806 E028
UART_RESUME	R	32	0x0000 002C	0x4802 002C	0x4806 E02C

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Table 23-167. UART/IrDA/CIR Register Mapping Summary (UART3 and UART4) (continued)

Register Name	Type	Register Width (Bits)	Address Offset	UART3 Base Address	UART4 Base Address
UART_TXFLH	W	32	0x0000 002C	0x4802 002C	0x4806 E02C
UART_SFREGL	R	32	0x0000 0030	0x4802 0030	0x4806 E030
UART_RXFLL	W	32	0x0000 0030	0x4802 0030	0x4806 E030
UART_SFREGH	R	32	0x0000 0034	0x4802 0034	0x4806 E034
UART_RXFLH	W	32	0x0000 0034	0x4802 0034	0x4806 E034
UART_BLR	RW	32	0x0000 0038	0x4802 0038	0x4806 E038
UART_UASR	R	32	0x0000 0038	0x4802 0038	0x4806 E038
UART_ACREG	RW	32	0x0000 003C	0x4802 003C	0x4806 E03C
UART_SCR	RW	32	0x0000 0040	0x4802 0040	0x4806 E040
UART_SSR	R	32	0x0000 0044	0x4802 0044	0x4806 E044
UART_EBLR	RW	32	0x0000 0048	0x4802 0048	0x4806 E048
UART_MVR	R	32	0x0000 0050	0x4802 0050	0x4806 E050
UART_SYSC	RW	32	0x0000 0054	0x4802 0054	0x4806 E054
UART_SYSS	R	32	0x0000 0058	0x4802 0058	0x4806 E058
UART_WER	RW	32	0x0000 005C	0x4802 005C	0x4806 E05C
UART_CFPS	RW	32	0x0000 0060	0x4802 0060	0x4806 E060
UART_RXFIFO_LVL	R	32	0x0000 0064	0x4802 0064	0x4806 E064
UART_TXFIFO_LVL	R	32	0x0000 0068	0x4802 0068	0x4806 E068
UART_IER2	RW	32	0x0000 006C	0x4802 006C	0x4806 E06C
UART_ISR2	RW	32	0x0000 0070	0x4802 0070	0x4806 E070
UART_FREQ_SEL	RW	32	0x0000 0074	0x4802 0074	0x4806 E074
UART_MDR3	RW	32	0x0000 0080	0x4802 0080	0x4806 E080
UART_TX_DMA_THRESHOLD	RW	32	0x0000 0084	0x4806 A084	0x4806 C084

23.3.6.2.2 UART/IrDA/CIR Registers

Table 23-168. UART_THR

Address Offset	0x0000 0000		
Physical Address	0x4806 A000 0x4806 C000 0x4802 0000 0x4806 E000	**Instance**	UART1 UART2 UART3 UART4
Description	The transmitter section consists of the transmit holding register (THR) and the transmit shift register. The THR is a 64-byte FIFO. The local host (LH) writes data to the THR. The data is placed in the transmit shift register where it is shifted out serially on the TX output. If the FIFO is disabled, location 0 of the FIFO stores the data.		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								THR							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Write has no effect.	W	0x000000
7:0	THR	Transmit holding register	W	0x-

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Table 23-169. Register Call Summary for Register UART_THR

UART/IrDA/CIR

- UART Mode Interrupt Management: [0] [1]
- IrDA Mode Interrupt Management: [2] [3] [4]
- CIR Mode Interrupt Management: [5] [6]
- FIFO Management: [7]
- FIFO DMA Mode Operation: [8] [9]
- Register Access Modes: [10]
- UART/IrDA (SIR, MIR, FIR)/CIR Mode Selection: [11] [12] [13]
- SIR Mode: [14]
- MIR Mode: [15]
- FIR Mode: [16]
- UART/IrDA/CIR Register Summary: [17] [18]

Table 23-170. UART_RHR

Address Offset	0x0000 0000		
Physical Address	0x4806 A000 0x4806 C000 0x4802 0000 0x4806 E000	**Instance**	UART1 UART2 UART3 UART4
Description	The receiver section consists of the receiver holding register (RHR) and the receiver shift register. The RHR is a 64-byte FIFO. The receiver shift register receives serial data from RX input. The data is converted to parallel data and moved to the RHR. If the FIFO is disabled, location 0 of the FIFO stores the single data character. **Note:** If an overflow occurs, the data in the RHR is not overwritten.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RHR							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Read returns 0	R	0x000000
7:0	RHR	Receive holding register	R	0x-

Table 23-171. Register Call Summary for Register UART_RHR

UART/IrDA/CIR

- UART Mode Interrupt Management: [0] [1] [2]
- IrDA Mode Interrupt Management: [3] [4] [5]
- FIFO Management: [6] [7]
- Register Access Modes: [8]
- UART/IrDA (SIR, MIR, FIR)/CIR Mode Selection: [9] [10]
- UART Mode: [11] [12] [13] [14]
- UART/IrDA/CIR Register Summary: [15] [16]

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Table 23-172. UART_DLL

Address Offset	0x0000 0000		
Physical Address	0x4806 A000 0x4806 C000 0x4802 0000 0x4806 E000	**Instance**	UART1 UART2 UART3 UART4
Description	This register, with UART_DLH, stores the 14-bit divisor for generation of the baud clock in the baud rate generator. DLH stores the most-significant part of the divisor. DLL stores the least-significant part of the divisor.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								CLOCK_LSB							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Read returns 0. Write has no effect.	RW	0x000000
7:0	CLOCK_LSB	Stores the 8-bit LSB divisor value	RW	0x00

Table 23-173. Register Call Summary for Register UART_DLL

UART/IrDA/CIR

- UART Mode Power Management: [0] [1]
- FIFO DMA Mode Operation: [2] [3]
- Register Access Modes: [4] [5] [6] [7]
- UART/IrDA (SIR, MIR, FIR)/CIR Mode Selection: [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19]
- UART Mode: [20] [21] [22]
- IrDA Mode (UART3 Only): [23]
- Quick Start: [24] [25] [26] [27] [28]
- SIR Mode: [29] [30] [31] [32] [33] [34] [35] [36]
- MIR Mode: [37] [38] [39] [40] [41] [42] [43] [44]
- FIR Mode: [45] [46] [47] [48]
- UART/IrDA/CIR Register Summary: [49] [50]
- UART/IrDA/CIR Registers: [51] [52]

Table 23-174. UART_IER

Address Offset	0x0000 0004		
Physical Address	0x4806 A004 0x4806 C004 0x4802 0004 0x4806 E004	**Instance**	UART1 UART2 UART3 UART4
Description	Interrupt enable register		
Type	RW		

UART Bit Field Details

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								CTS_IT	RTS_IT	XOFF_IT	SLEEP_MODE	MODEM_STS_IT	LINE_STS_IT	THR_IT	RHR_IT

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Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Read returns 0. Write has no effect.	RW	0x000000
7	CTS_IT	0x0: Disables the CTS* interrupt 0x1: Enables the CTS* interrupt	RW	0
6	RTS_IT	0x0: Disables the RTS* interrupt 0x1: Enables the RTS* interrupt	RW	0
5	XOFF_IT	0x0: Disables the XOFF interrupt 0x1: Enables the XOFF interrupt	RW	0
4	SLEEP_MODE	0x0: Disables sleep mode 0x1: Enables sleep mode (stop baud rate clock when the module is inactive)	RW	0
3	MODEM_STS_IT	0x0: Disables the modem status register interrupt 0x1: Enables the modem status register interrupt	RW	0
2	LINE_STS_IT	0x0: Disables the receiver line status interrupt 0x1: Enables the receiver line status interrupt	RW	0
1	THR_IT	0x0: Disables the THR interrupt 0x1: Enables the THR interrupt	RW	0
0	RHR_IT	0x0: Disables the RHR interrupt and time-out interrupt 0x1: Enables the RHR interrupt and time-out interrupt	RW	0

Table 23-175. Register Call Summary for Register UART_IER

UART/IrDA/CIR

- UART Mode Power Management: [0] [1]
- IrDA Mode Interrupt Management: [2] [3]
- CIR Mode Interrupt Management: [4] [5]
- FIFO Interrupt Mode: [6]
- FIFO Polled Mode Operation: [7]
- Register Access Modes: [8] [9]
- UART/IrDA (SIR, MIR, FIR)/CIR Mode Selection: [10] [11] [12] [13] [14] [15]
- UART Mode: [16]
- Quick Start: [17] [18] [19] [20] [21] [22] [23] [24] [25] [26] [27] [28] [29] [30]
- SIR Mode: [31] [32]
- MIR Mode: [33] [34]
- FIR Mode: [35] [36]
- UART/IrDA/CIR Register Summary: [37] [38]

IrDA Bit Field Details

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								EOF_IT	LINE_STS_IT	TX_STATUS_IT	STS_FIFO_TRIG_IT	RX_OVERRUN_IT	LAST_RX_BYTE_IT	THR_IT	RHR_IT

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Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Read returns 0. Write has no effect.	RW	0x000000
7	EOF_IT	0x0: Disables the received EOF interrupt 0x1: Enables the received EOF interrupt	RW	0
6	LINE_STS_IT	0x0: Disables the receiver line status interrupt 0x1: Enables the receiver line status interrupt	RW	0
5	TX_STATUS_IT	0x0: Disables the TX status interrupt 0x1: Enables the TX status interrupt	RW	0
4	STS_FIFO_TRIG_IT	0x0: Disables status FIFO trigger level interrupt 0x1: Enables status FIFO trigger level interrupt	RW	0
3	RX_OVERRUN_IT	0x0: Disables the RX overrun interrupt 0x1: Enables the RX overrun interrupt	RW	0
2	LAST_RX_BYTE_IT	0x0: Disables the last byte of frame in RX FIFO interrupt 0x1: Enables the last byte of frame in RX FIFO interrupt	RW	0
1	THR_IT	0x0: Disables the THR interrupt 0x1: Enables the THR interrupt	RW	0
0	RHR_IT	0x0: Disables the RHR interrupt and time-out interrupt 0x1: Enables the RHR interrupt and time-out interrupt	RW	0

CIR Bit Field Details

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RESERVED		TX_STATUS_IT	RESERVED	RX_OVERRUN_IT	RX_STOP_IT	THR_IT	RHR_IT

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Read returns 0. Write has no effect.	RW	0x000000
7:6	RESERVED	Not used in CIR mode	RW	0x0
5	TX_STATUS_IT	0x0: Disables the TX status interrupt 0x1: Enables the TX status interrupt	RW	0
4	RESERVED	Not used in CIR mode	RW	0
3	RX_OVERRUN_IT	0x0: Disables the RX overrun interrupt 0x1: Enables the RX overrun interrupt	RW	0
2	RX_STOP_IT	0x0: Disables the receive stop interrupt 0x1: Enables the receive stop interrupt	RW	0
1	THR_IT	0x0: Disables the THR interrupt 0x1: Enables the THR interrupt	RW	0
0	RHR_IT	0x0: Disables the RHR interrupt 0x1: Enables the RHR interrupt	RW	0

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Table 23-176. UART_IIR

Address Offset	0x0000 0008		
Physical Address	0x4806 A008 0x4806 C008 0x4802 0008 0x4806 E008	**Instance**	UART1 UART2 UART3 UART4
Description	Interrupt identification register. The IIR is a read-only register that provides the source of the interrupt in a prioritized manner.		
Type	R		

UART Bit Field Details

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								FCR_MIRROR		IT_TYPE					IT_PENDING

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Read returns 0. Write has no effect.	R	0x000000
7:6	FCR_MIRROR	Mirror the contents of UART_FCR[0] on both bits.	R	0x0
5:1	IT_TYPE	Read 0x0: Modem interrupt. Priority = 4 Read 0x1: THR interrupt. Priority = 3 Read 0x2: RHR interrupt. Priority = 2 Read 0x3: Receiver line status error. Priority = 3 Read 0x6: Rx time-out. Priority = 2 Read 0x8: XOFF/special character. Priority = 5 Read 0x10: CTS, RTS, DSR change state from active (low) to inactive (high) Priority = 6	R	0x00
0	IT_PENDING	Read 0x0: An interrupt is pending. Read 0x1: No interrupt is pending.	R	1

Table 23-177. Register Call Summary for Register UART_IIR

UART/IrDA/CIR

- Block Diagram: [0]
- UART Mode Interrupt Management: [1] [2] [3] [4] [5] [6] [7] [8]
- IrDA Mode Interrupt Management: [9] [10] [11] [12] [13]
- CIR Mode Interrupt Management: [14] [15] [16] [17] [18]
- Register Access Modes: [19] [20]
- UART/IrDA (SIR, MIR, FIR)/CIR Mode Selection: [21] [22] [23] [24] [25] [26]
- UART Mode: [27] [28] [29] [30] [31]
- CIR Mode (UART3 Only): [32]
- UART/IrDA/CIR Register Summary: [33] [34]
- UART/IrDA/CIR Registers: [35] [36] [37] [38] [39] [40] [41] [42]

IrDA Bit Field Details

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								EOF_IT	LINE_STS_IT	TX_STATUS_IT	STS_FIFO_IT	RX_OE_IT	RX_FIFO_LAST_BYTE_IT	THR_IT	RHR_IT

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Read returns 0. Write has no effect.	R	0x000000
7	EOF_IT	Read 0x0: Receive EOF interrupt inactive Read 0x1: Received EOF interrupt active	R	0
6	LINE_STS_IT	Read 0x0: Receiver line status interrupt inactive Read 0x1: Receiver line status interrupt active	R	0
5	TX_STATUS_IT	Read 0x0: TX status interrupt inactive Read 0x1: TX status interrupt active	R	0
4	STS_FIFO_IT	Read 0x0: Status FIFO trigger level interrupt inactive Read 0x1: Status FIFO trigger level interrupt active	R	0
3	RX_OE_IT	Read 0x0: RX overrun interrupt inactive Read 0x1: RX overrun interrupt active	R	0
2	RX_FIFO_LAST_BYTE_IT	Read 0x0: Last byte of frame in RX FIFO interrupt inactive Read 0x1: Last byte of frame in RX FIFO interrupt active	R	0
1	THR_IT	Read 0x0: THR interrupt inactive Read 0x1: THR interrupt active	R	0
0	RHR_IT	Read 0x0: RHR interrupt inactive Read 0x1: RHR interrupt active	R	1

CIR Bit Field Details

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RESERVED	TX_STATUS_IT	RESERVED	RX_OE_IT	RX_STOP_IT	THR_IT	RHR_IT

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Read returns 0. Write has no effect.	R	0x000000
7:6	RESERVED	Not used in CIR mode	R	0x0
5	TX_STATUS_IT	Read 0x0: TX status interrupt inactive Read 0x1: TX status interrupt active	R	0
4	RESERVED	Not used in CIR mode	R	0
3	RX_OE_IT	Read 0x0: RX overrun interrupt inactive Read 0x1: RX overrun interrupt active	R	0
2	RX_STOP_IT	Read 0x0: Receive stop interrupt inactive Read 0x1: Receive stop interrupt active	R	0

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Bits	Field Name	Description	Type	Reset
1	THR_IT	Read 0x0: THR interrupt inactive Read 0x1: THR interrupt active	R	0
0	RHR_IT	Read 0x0: RHR interrupt inactive Read 0x1: RHR interrupt active	R	0

Table 23-178. UART_DLH

Address Offset	0x0000 0004		
Physical Address	0x4806 A004 0x4806 C004 0x4802 0004 0x4806 E004	**Instance**	UART1 UART2 UART3 UART4
Description	This register, with UART_DLL, stores the 14-bit divisor for generating the baud clock in the baud rate generator. DLH stores the most-significant part of the divisor. DLL stores the least-significant part of the divisor.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RESERVED		CLOCK_MSB					

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Read returns 0. Write has no effect.	RW	0x000000
7:6	RESERVED	Read returns 0. Write has no effect.	RW	0x0
5:0	CLOCK_MSB	Stores the 6-bit MSB divisor value	RW	0x00

Table 23-179. Register Call Summary for Register UART_DLH

UART/IrDA/CIR

- UART Mode Power Management: [0] [1]
- FIFO DMA Mode Operation: [2] [3]
- Register Access Modes: [4] [5] [6] [7]
- UART/IrDA (SIR, MIR, FIR)/CIR Mode Selection: [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19]
- UART Mode: [20] [21] [22]
- IrDA Mode (UART3 Only): [23]
- Quick Start: [24] [25] [26] [27] [28]
- SIR Mode: [29] [30] [31] [32] [33] [34] [35] [36]
- MIR Mode: [37] [38] [39] [40] [41] [42] [43] [44]
- FIR Mode: [45] [46] [47] [48]
- UART/IrDA/CIR Register Summary: [49] [50]
- UART/IrDA/CIR Registers: [51] [52]

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Table 23-180. UART_FCR

Address Offset	0x0000 0008		
Physical Address	0x4806 A008 0x4806 C008 0x4802 0008 0x4806 E008	**Instance**	UART1 UART2 UART3 UART4
Description	FIFO control register **Notes:** Bits 4 and 5 can only be written to when UART_EFR[4] = 1. Bits 0 and 3 can be changed only when the baud clock is not running (DLL and DLH set to 0). See Table 23-149 for UART_FCR[5:4] setting restriction when UART_SCR[6] = 1. See Table 23-150 for UART_FCR[7:6] setting restriction when UART_SCR[7] = 1.		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RX_FIFO_TRIG		TX_FIFO_TRIG		DMA_MODE	TX_FIFO_CLEAR	RX_FIFO_CLEAR	FIFO_EN

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Write has no effect.	W	0x000000
7:6	RX_FIFO_TRIG	Sets the trigger level for the RX FIFO: If UART_SCR[7] = 0 and UART_TLR[7:4] = 0000: 00: 8 characters 01: 16 characters 10: 56 characters 11: 60 characters If UART_SCR[7] = 0 and UART_TLR[7:4] != 0000, RX_FIFO_TRIG is not considered. If UART_SCR[7] = 1, RX_FIFO_TRIG is 2 LSBs of the trigger level (1-63 on 6 bits) with the granularity 1.	W	0x0
5:4	TX_FIFO_TRIG	Sets the trigger level for the TX FIFO: If UART_SCR[6] = 0 and UART_TLR[3:0] = 0000: 00: 8 spaces 01: 16 spaces 10: 32 spaces 11: 56 spaces If UART_SCR[6] = 0 and UART_TLR[3:0] != 0000, TX_FIFO_TRIG is not considered. If UART_SCR[6] = 1, TX_FIFO_TRIG is 2 LSBs of the trigger level (1-63 on 6 bits) with the granularity 1	W	0x0
3	DMA_MODE	This register is considered if UART_SCR[0] = 0. Write 0x0: DMA_MODE 0 (No DMA) Write 0x1: DMA_MODE 1 (UART_nDMA_REQ[0] in TX, UART_nDMA_REQ[1] in RX)	W	0
2	TX_FIFO_CLEAR	Write 0x0: No change Write 0x1: Clears the TX FIFO and resets its counter logic to 0. Returns to 0 after clearing FIFO.	W	0
1	RX_FIFO_CLEAR	Write 0x0: No change Write 0x1: Clears the RX FIFO and resets its counter logic to 0. Returns to 0 after clearing FIFO.	W	0
0	FIFO_EN	Write 0x0: Disables the transmit and RX FIFOs. The transmit and receive holding registers are 1-byte FIFOs. Write 0x1: Enables the transmit and RX FIFOs. The transmit and receive holding registers are 64-byte FIFOs.	W	0

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Table 23-181. Register Call Summary for Register UART_FCR

UART/IrDA/CIR

- FIFO Management: [0]
- FIFO Trigger: [1] [2] [3]
- FIFO Interrupt Mode: [4] [5] [6]
- FIFO Polled Mode Operation: [7]
- FIFO DMA Mode Operation: [8] [9] [10] [11]
- Register Access Modes: [12] [13]
- UART/IrDA (SIR, MIR, FIR)/CIR Mode Selection: [14] [15] [16] [17] [18] [19]
- Quick Start: [20] [21] [22] [23] [24] [25] [26] [27]
- FIR Mode: [28] [29] [30] [31] [32] [33]
- UART/IrDA/CIR Register Summary: [34] [35]
- UART/IrDA/CIR Registers: [36] [37] [38] [39] [40] [41] [42] [43]

Table 23-182. UART_EFR

Address Offset	0x0000 0008		
Physical Address	0x4806 A008 0x4806 C008 0x4802 0008 0x4806 E008	**Instance**	UART1 UART2 UART3 UART4
Description	Enhanced feature register This register enables or disables enhanced features. Most of the enhanced functions apply only to UART modes, but UART_EFR[4] enables write accesses to UART_FCR[5:4], the TX trigger level, which is also used in IrDA modes.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								AUTO_CTS_EN	AUTO_RTS_EN	SPECIAL_CHAR_DETECT	ENHANCED_EN	SW_FLOW_CONTROL			

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Read returns 0. Write has no effect.	RW	0x000000
7	AUTO_CTS_EN	Auto-CTS enable bit 0x0: Normal operation 0x1: Auto-CTS flow control is enabled. Transmission is halted when the CTS* pin is high (inactive).	RW	0
6	AUTO_RTS_EN	Auto-RTS enable bit 0x0: Normal operation 0x1: Auto-RTS flow control is enabled. RTS* pin goes high (inactive) when the RX FIFO HALT trigger level, UART_TCR[3:0], is reached, and goes low (active) when the RX FIFO RESTORE transmission trigger level is reached.	RW	0
5	SPECIAL_CHAR_DETECT	0x0: Normal operation 0x1: Special character detect enable. Received data is compared with XOFF2 data. If a match occurs, the received data is transferred to the RX FIFO and the UART_IIR[4] bit is set to 1 to indicate that a special character was detected.	RW	0

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Bits	Field Name	Description	Type	Reset
4	ENHANCED_EN	Enhanced functions write enable bit 0x0: Disables writing to IER bits 4-7, UART_FCR bits 4-5, and MCR bits 5-7. 0x1: Enables writing to IER bits 4-7, UART_FCR bits 4-5, and MCR bits 5-7.	RW	0
3:0	SW_FLOW_CONTROL	Combinations of software flow control can be selected by programming bit 3 - bit 0. See Table 23-162.	RW	0x0

Table 23-183. Register Call Summary for Register UART_EFR

UART/IrDA/CIR

- IrDA Protocol and Data Format: [0] [1] [2]
- UART Mode Power Management: [3]
- Register Access Modes: [4] [5] [6] [7] [8] [9] [10] [11]
- UART/IrDA (SIR, MIR, FIR)/CIR Mode Selection: [12] [13] [14] [15] [16] [17]
- UART Mode: [18] [19] [20] [21] [22] [23]
- IrDA Mode (UART3 Only): [24] [25] [26]
- Quick Start: [27] [28] [29] [30] [31] [32] [33] [34] [35] [36]
- Hardware and Software Flow Control Configuration: [37] [38] [39] [40] [41] [42] [43] [44] [45] [46] [47] [48] [49] [50] [51] [52] [53] [54] [55] [56]
- SIR Mode: [57] [58] [59]
- FIR Mode: [60]
- UART/IrDA/CIR Register Summary: [61] [62]
- UART/IrDA/CIR Registers: [63] [64]

Table 23-184. UART_LCR

Address Offset	0x0000 000C		
Physical Address	0x4806 A00C 0x4806 C00C 0x4802 000C 0x4806 E00C	**Instance**	UART1 UART2 UART3 UART4
Description	Line control register LCR[6:0] define transmission and reception parameters. **Note:** When LCR[6] is set to 1, the TX line is forced to 0 and remains in this state as long as LCR[6] = 1.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								DIV_EN	BREAK_EN	PARITY_TYPE2	PARITY_TYPE1	PARITY_EN	NB_STOP	CHAR_LENGTH	

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Read returns 0. Write has no effect.	RW	0x000000
7	DIV_EN	0x0: Normal operating condition 0x1: Divisor latch enable. Allows access to DLL, DLH, and other registers (see Table 23-166 and Table 23-167).	RW	0
6	BREAK_EN	Break control bit 0x0: Normal operating condition 0x1: Forces the transmitter output to go low to alert the communication terminal	RW	0

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Bits	Field Name	Description	Type	Reset
5	PARITY_TYPE2	Selects the forced parity format (if UART_LCR[3] = 1). If UART_LCR[5] = 1 and UART_LCR[4] = 0, the parity bit is forced to 1 in the transmitted and received data. If UART_LCR[5] = 1 and UART_LCR[4] = 1, the parity bit is forced to 0 in the transmitted and received data.	RW	0
		UART_LCR[3] / UART_LCR[4] / UART_LCR[5] / Parity 0 / N/A / N/A / No parity 1 / 0 / 0 / Odd parity 1 / 1 / 0 / Even parity 1 / 0 / 1 / Forced 1 1 / 1 / 1 / Forced 0		
4	PARITY_TYPE1	0x0: Odd parity is generated (if UART_LCR[3] = 1). 0x1: Even parity is generated (if UART_LCR[3] = 1).	RW	0
3	PARITY_EN	0x0: No parity 0x1: A parity bit is generated during transmission and the receiver checks for received parity.	RW	0
2	NB_STOP	Specifies the number of stop-bits 0x0: 1 stop-bit (word length = 5, 6, 7, 8) 0x1: 1.5 stop-bits (word length = 5) 2 stop-bits (word length = 6, 7, 8)	RW	0
1:0	CHAR_LENGTH	Specifies the word length to be transmitted or received 0x0: 5 bits 0x1: 6 bits 0x2: 7 bits 0x3: 8 bits	RW	0x0

Table 23-185. Register Call Summary for Register UART_LCR

UART/IrDA/CIR

- IrDA Protocol and Data Format: [0]
- Register Access Modes: [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12]
- UART/IrDA (SIR, MIR, FIR)/CIR Mode Selection: [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23] [24] [25] [26] [27] [28] [29] [30]
- UART Mode: [31] [32] [33] [34] [35] [36] [37]
- IrDA Mode (UART3 Only): [38] [39] [40]
- Quick Start: [41] [42] [43] [44] [45] [46] [47] [48] [49] [50] [51] [52] [53] [54] [55] [56] [57] [58] [59] [60] [61] [62] [63]
- Hardware and Software Flow Control Configuration: [64] [65] [66] [67] [68] [69] [70] [71] [72] [73] [74]
- SIR Mode: [75] [76] [77] [78] [79] [80] [81] [82] [83]
- MIR Mode: [84] [85] [86] [87] [88] [89] [90] [91]
- FIR Mode: [92] [93] [94] [95] [96] [97] [98]
- UART/IrDA/CIR Register Summary: [99] [100]
- UART/IrDA/CIR Registers: [101] [102] [103] [104] [105] [106] [107] [108] [109] [110] [111]

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Table 23-186. UART_XON1_ADDR1

Address Offset	0x0000 0010		
Physical Address	0x4806 A010 0x4806 C010 0x4802 0010 0x4806 E010	**Instance**	UART1 UART2 UART3 UART4
Description	UART mode: XON1 character, IrDA mode: ADDR1 address		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								XON_WORD1							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Read returns 0. Write has no effect.	RW	0x000000
7:0	XON_WORD1	Stores the 8-bit XON1 character in UART modes and ADDR1 address 1 for IrDA modes	RW	0x00

Table 23-187. Register Call Summary for Register UART_XON1_ADDR1

UART/IrDA/CIR

- IrDA Protocol and Data Format: [0]
- Register Access Modes: [1] [2]
- UART/IrDA (SIR, MIR, FIR)/CIR Mode Selection: [3] [4] [5] [6]
- IrDA Mode (UART3 Only): [7]
- Hardware and Software Flow Control Configuration: [8] [9]
- UART/IrDA/CIR Register Summary: [10] [11]

Table 23-188. UART_MCR

Address Offset	0x0000 0010		
Physical Address	0x4806 A010 0x4806 C010 0x4802 0010 0x4806 E010	**Instance**	UART1 UART2 UART3 UART4
Description	Modem control register MCR[3:0] controls the interface with the modem, data set, or peripheral device that emulates the modem.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RESERVED	TCR_TLR	XON_EN	LOOPBACK_EN	CD_STS_CH	RI_STS_CH	RTS	DTR

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Read returns 0. Write has no effect.	RW	0x000000
7	RESERVED	Read returns 0. Write has no effect.	RW	0
6	TCR_TLR	0x0: No action 0x1: Enables access to the UART_TCR and UART_TLR registers	RW	0
5	XON_EN	0x0: Disable XON any function. 0x1: Enable XON any function.	RW	0

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Bits	Field Name	Description	Type	Reset
4	LOOPBACK_EN	0x0: Normal operating mode 0x1: Enable local loopback mode (internal). In this mode, the MCR[3:0] signals are looped back into the UART_MSR[7:4] bit field. The transmit output is looped back to the receive input internally.	RW	0
3	CD_STS_CH	0x0: In loopback, forces DCD* input high and IRQ outputs to inactive state 0x1: In loopback, forces DCD* input low and IRQ outputs to inactive state	RW	0
2	RI_STS_CH	0x0: In loopback, forces RI* input high 0x1: In loopback, forces RI* input low	RW	0
1	RTS	In loopback, controls the UART_MSR[4] bit. If auto-RTS is enabled, the RTS* output is controlled by hardware flow control. 0x0: Force RTS* output to inactive (high). 0x1: Force RTS* output to active (low).	RW	0
0	DTR	0x0: Force DTR* output to inactive (high). 0x1: Force DTR* output to active (low).	RW	0

Table 23-189. Register Call Summary for Register UART_MCR

UART/IrDA/CIR

- Description: [0] [1]
- Register Access Modes: [2] [3] [4] [5] [6] [7] [8] [9] [10] [11]
- UART/IrDA (SIR, MIR, FIR)/CIR Mode Selection: [12] [13] [14] [15]
- UART Mode: [16] [17]
- Quick Start: [18] [19] [20] [21] [22]
- Hardware and Software Flow Control Configuration: [23] [24] [25] [26] [27] [28] [29] [30] [31] [32] [33] [34]
- SIR Mode: [35]
- MIR Mode: [36] [37] [38] [39]
- FIR Mode: [40]
- UART/IrDA/CIR Register Summary: [41] [42]
- UART/IrDA/CIR Registers: [43] [44] [45] [46] [47] [48] [49] [50]

Table 23-190. UART_LSR

Address Offset	0x0000 0014		
Physical Address	0x4806 A014 0x4806 C014 0x4802 0014 0x4806 E014	**Instance**	UART1 UART2 UART3 UART4
Description	Line status register		
Type	R		

UART Bit Field Details

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RX_FIFO_STS	TX_SR_E	TX_FIFO_E	RX_BI	RX_FE	RX_PE	RX_OE	RX_FIFO_E

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Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Read returns 0.	R	0x000000
7	RX_FIFO_STS	Read 0x0: Normal operation Read 0x1: At least one parity error, framing error, or break indication in the RX FIFO. Bit 7 is cleared when no more errors are present in the RX FIFO.	R	0
6	TX_SR_E	Read 0x0: Transmitter hold (TX FIFO) and shift registers are not empty. Read 0x1: Transmitter hold (TX FIFO) and shift registers are empty.	R	1
5	TX_FIFO_E	Read 0x0: Transmit hold register (TX FIFO) is not empty. Read 0x1: Transmit hold register (TX FIFO) is empty. The transmission is not necessarily complete.	R	1
4	RX_BI	Read 0x0: No break condition Read 0x1: A break was detected while the data from the RX FIFO was received (for example, RX input was low for one character + 1 bit time frame).	R	0
3	RX_FE	Read 0x0: No framing error in data RX FIFO Read 0x1: Framing error occurred in data from RX FIFO (received data did not have a valid stop-bit).	R	0
2	RX_PE	Read 0x0: No parity error in data from RX FIFO Read 0x1: Parity error in data from RX FIFO	R	0
1	RX_OE	Read 0x0: No overrun error Read 0x1: Overrun error occurred. Set when the character in the receive shift register is not transferred to the RX FIFO. This occurs only when the RX FIFO is full.	R	0
0	RX_FIFO_E	Read 0x0: No data in the RX FIFO Read 0x1: At least one data character in the RX FIFO	R	0

Table 23-191. Register Call Summary for Register UART_LSR

UART/IrDA/CIR

- IrDA Protocol and Data Format: [0] [1] [2]
- UART Mode Interrupt Management: [3] [4]
- FIFO Polled Mode Operation: [5]
- Register Access Modes: [6] [7]
- UART/IrDA (SIR, MIR, FIR)/CIR Mode Selection: [8] [9] [10] [11] [12] [13]
- UART Mode: [14] [15] [16] [17] [18] [19] [20]
- IrDA Mode (UART3 Only): [21] [22] [23]
- UART/IrDA/CIR Register Summary: [24] [25]
- UART/IrDA/CIR Registers: [26]

IrDA Bit Field Details

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								THR_EMPTY	STS_FIFO_FULL	RX_LAST_BYTE	FRAME_TOO_LONG	ABORT	CRC	STS_FIFO_E	RX_FIFO_E

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Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Read returns 0.	R	0x000000
7	THR_EMPTY	Read 0x0: Transmit holding register (TX FIFO) is not empty. Read 0x1: Transmit hold register (TX FIFO) is empty. The transmission is not necessarily complete.	R	1
6	STS_FIFO_FULL	Read 0x0: Status FIFO not full Read 0x1: Status FIFO full	R	0
5	RX_LAST_BYTE	Read 0x0: The RX FIFO (RHR) does not contain the last byte of the frame to be read. Read 0x1: The RX FIFO (RHR) contains the last byte of the frame to be read. This bit is set only when the last byte of a frame is available to be read. It determines the frame boundary. It is cleared on a single read of the LSR register. See the note below.	R	0
4	FRAME_TOO_LONG	Read 0x0: No frame-too-long error in frame Read 0x1: Frame-too-long error in the frame at the top of the STATUS FIFO, (next character to be read). This bit is set to 1 when a frame exceeding the maximum length (set by RXFLH and RXFLL registers) is received. When this error is detected, current frame reception is terminated. Reception is stopped until the next START flag is detected.	R	0
3	ABORT	Read 0x0: No abort pattern error in frame Read 0x1: Abort pattern is received. SIR and MIR: Abort pattern FIR: Illegal symbol	R	0
2	CRC	Read 0x0: No CRC error in frame Read 0x1: CRC error in the frame at the top of the STATUS FIFO (next character to be read)	R	0
1	STS_FIFO_E	Read 0x0: Status FIFO not empty Read 0x1: Status FIFO empty	R	1
0	RX_FIFO_E	Read 0x0: No data in the RX FIFO Read 0x1: At least one data character in the RX FIFO	R	1

CIR Bit Field Details

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								THR_EMPTY	RESERVED	RX_STOP	RESERVED				RX_FIFO_E

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Read returns 0.	R	0x000000
7	THR_EMPTY	Read 0x0: Transmit holding register (TX FIFO) is not empty. Read 0x1: Transmit hold register (TX FIFO) is empty. The transmission is not necessarily complete.	R	1
6	RESERVED	Not used in CIR mode	R	0
5	RX_STOP	The RX_STOP is generated based on the value set in the BOF Length register (UART_EBLR). It is cleared on a single read of the UART_LSR register. Read 0x0: Reception is ongoing or waiting for a new frame. Read 0x1: Reception is complete.	R	0
4:1	RESERVED	Not used in CIR mode	R	0x0
0	RX_FIFO_E	Read 0x0: At least one data character in the RX FIFO	R	1

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Bits	Field Name	Description	Type	Reset
		Read 0x1: No data in the RX FIFO		

Table 23-192. UART_XON2_ADDR2

Address Offset	0x0000 0014		
Physical Address	0x4806 A014 0x4806 C014 0x4802 0014 0x4806 E014	**Instance**	UART1 UART2 UART3 UART4
Description	Stores the 8-bit XON2 character in UART moldes and ADDR2 address 2 for IrDA modes		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								XON_WORD2							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Read returns 0. Write has no effect.	RW	0x000000
7:0	XON_WORD2	Stores the 8-bit XON2 character in UART modes and ADDR2 address 2 for IrDA modes	RW	0x00

Table 23-193. Register Call Summary for Register UART_XON2_ADDR2

UART/IrDA/CIR

- IrDA Protocol and Data Format: [0]
- Register Access Modes: [1] [2]
- UART/IrDA (SIR, MIR, FIR)/CIR Mode Selection: [3] [4] [5] [6]
- IrDA Mode (UART3 Only): [7]
- Hardware and Software Flow Control Configuration: [8] [9]
- UART/IrDA/CIR Register Summary: [10] [11]

Table 23-194. UART_TCR

Address Offset	0x0000 0018		
Physical Address	0x4806 A018 0x4806 C018 0x4802 0018 0x4806 E018	**Instance**	UART1 UART2 UART3 UART4
Description	Transmission control register This register stores the RX FIFO threshold levels to start/stop transmission during hardware/software flow control. Notes: Trigger levels from 0 to 60 bytes are available with a granularity of 4. (Trigger level = 4 x [4-bit register value]) The programmer must ensure that UART_TCR[3:0] UART_TCR[7:4] when auto-RTS or software flow control is enabled to avoid a mis-operation of the device. In FIFO interrupt mode with flow control, the programmer must ensure that the trigger level to halt transmission is greater than or equal to the RX FIFO trigger level (UART_TLR[7:4] or UART_FCR[7:6]); otherwise, FIFO operation stalls. In FIFO DMA mode with flow control, this concept does not exist because a DMA request is sent each time a byte is received.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RX_FIFO_TRIG_START				RX_FIFO_TRIG_HALT			

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Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Read returns 0. Write has no effect.	RW	0x000000
7:4	RX_FIFO_TRIG_START	RX FIFO trigger level to RESTORE transmission (0 - 60)	RW	0x0
3:0	RX_FIFO_TRIG_HALT	RX FIFO trigger level to HALT transmission (0 - 60)	RW	0xF

Table 23-195. Register Call Summary for Register UART_TCR

UART/IrDA/CIR

- FIFO Trigger: [0] [1] [2]
- FIFO Interrupt Mode: [3]
- Register Access Modes: [4] [5] [6] [7] [8] [9]
- UART/IrDA (SIR, MIR, FIR)/CIR Mode Selection: [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23] [24] [25] [26] [27]
- UART Mode: [28] [29] [30] [31] [32] [33]
- Hardware and Software Flow Control Configuration: [34] [35] [36] [37] [38] [39] [40] [41] [42] [43] [44] [45]
- UART/IrDA/CIR Register Summary: [46] [47]
- UART/IrDA/CIR Registers: [48] [49] [50] [51]

Table 23-196. UART_XOFF1

Address Offset	0x0000 0018		
Physical Address	0x4806 A018 0x4806 C018 0x4802 0018 0x4806 E018	**Instance**	UART1 UART2 UART3 UART4
Description	UART mode XOFF1 character		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								XOFF_WORD1							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Read returns 0. Write has no effect.	RW	0x000000
7:0	XOFF_WORD1	Stores the 8-bit XOFF1 character used in UART modes	RW	0x00

Table 23-197. Register Call Summary for Register UART_XOFF1

UART/IrDA/CIR

- Register Access Modes: [0] [1]
- UART/IrDA (SIR, MIR, FIR)/CIR Mode Selection: [2] [3]
- Hardware and Software Flow Control Configuration: [4] [5] [6]
- UART/IrDA/CIR Register Summary: [7] [8]

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Table 23-198. UART_MSR

Address Offset	0x0000 0018		
Physical Address	0x4806 A018 0x4806 C018 0x4802 0018 0x4806 E018	**Instance**	UART1 UART2 UART3 UART4
Description	Modem status register. UART mode only. This register provides information about the current state of the control lines from the modem, data set, or peripheral device to the LH. It also indicates when a control input from the modem changes state.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								NCD_STS	NRI_STS	NDSR_STS	NCTS_STS	DCD_STS	RI_STS	DSR_STS	CTS_STS

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Read returns 0.	R	0x000000
7	NCD_STS	This bit is the complement of the DCD* input. In loopback mode, it is equivalent to UART_MCR[3].	R	-
6	NRI_STS	This bit is the complement of the RI* input. In loopback mode, it is equivalent to UART_MCR[2].	R	-
5	NDSR_STS	This bit is the complement of the DSR* input. In loopback mode, it is equivalent to UART_MCR[0].	R	-
4	NCTS_STS	This bit is the complement of the CTS* input. In loopback mode, it is equivalent to UART_MCR[1].	R	-
3	DCD_STS	Indicates that DCD* input (or UART_MCR[3] in loopback) changed. Cleared on a read.	R	0
2	RI_STS	Indicates that RI* input (or UART_MCR[2] in loopback) changed state from low to high. Cleared on a read.	R	0
1	DSR_STS	Read 0x1: Indicates that DSR* input (or UART_MCR[0] in loopback) changed state. Cleared on a read.	R	0
0	CTS_STS	Read 0x1: Indicates that CTS* input (or UART_MCR[1] in loopback) changed state. Cleared on a read.	R	0

Table 23-199. Register Call Summary for Register UART_MSR

UART/IrDA/CIR

- Description: [0] [1]
- UART Mode Interrupt Management: [2] [3]
- Register Access Modes: [4] [5]
- UART/IrDA (SIR, MIR, FIR)/CIR Mode Selection: [6] [7] [8] [9] [10] [11]
- UART/IrDA/CIR Register Summary: [12] [13]
- UART/IrDA/CIR Registers: [14] [15]

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Table 23-200. UART_SPR

Address Offset	0x0000 001C		
Physical Address	0x4806 A01C 0x4806 C01C 0x4802 001C 0x4806 E01C	**Instance**	UART1 UART2 UART3 UART4
Description	Scratchpad register This read/write register does not control the module. It is a scratchpad register to be used by the programmer to hold temporary data.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								SPR_WORD							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Read returns 0. Write has no effect.	RW	0x000000
7:0	SPR_WORD	Scratchpad register	RW	0x00

Table 23-201. Register Call Summary for Register UART_SPR

UART/IrDA/CIR

- Register Access Modes: [0] [1] [2] [3]
- UART/IrDA (SIR, MIR, FIR)/CIR Mode Selection: [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15]
- UART/IrDA/CIR Register Summary: [16] [17]

Table 23-202. UART_TLR

Address Offset	0x0000 001C		
Physical Address	0x4806 A01C 0x4806 C01C 0x4802 001C 0x4806 E01C	**Instance**	UART1 UART2 UART3 UART4
Description	Trigger level register This register stores the programmable transmit and RX FIFO trigger levels for DMA and IRQ generation.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RX_FIFO_TRIG_DMA				TX_FIFO_TRIG_DMA			

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Read returns 0. Write has no effect.	RW	0x000000
7:4	RX_FIFO_TRIG_DMA	Receive FIFO trigger level	RW	0x0
3:0	TX_FIFO_TRIG_DMA	Transmit FIFO trigger level	RW	0x0

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Table 23-203. Register Call Summary for Register UART_TLR

UART/IrDA/CIR

- FIFO Management: [0]
- FIFO Trigger: [1] [2] [3] [4]
- FIFO Interrupt Mode: [5] [6]
- FIFO DMA Mode Operation: [7] [8] [9] [10]
- Register Access Modes: [11] [12] [13] [14] [15] [16]
- UART/IrDA (SIR, MIR, FIR)/CIR Mode Selection: [17] [18] [19] [20] [21] [22] [23] [24] [25] [26] [27] [28] [29] [30] [31] [32] [33] [34]
- Quick Start: [35] [36] [37] [38] [39] [40]
- UART/IrDA/CIR Register Summary: [41] [42]
- UART/IrDA/CIR Registers: [43] [44] [45] [46] [47] [48]

Table 23-204. UART_XOFF2

Address Offset	0x0000 001C		
Physical Address	0x4806 A01C 0x4806 C01C 0x4802 001C 0x4806 E01C	**Instance**	UART1 UART2 UART3 UART4
Description	UART mode XOFF2 character		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								XOFF_WORD2							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Read returns 0. Write has no effect.	RW	0x000000
7:0	XOFF_WORD2	Stores the 8-bit XOFF2 character used in UART modes.	RW	0x00

Table 23-205. Register Call Summary for Register UART_XOFF2

UART/IrDA/CIR

- Register Access Modes: [0] [1]
- UART/IrDA (SIR, MIR, FIR)/CIR Mode Selection: [2] [3]
- Hardware and Software Flow Control Configuration: [4] [5] [6]
- UART/IrDA/CIR Register Summary: [7] [8]

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Table 23-206. UART_MDR1

Address Offset	0x0000 0020		
Physical Address	0x4806 A020 0x4806 C020 0x4802 0020 0x4806 E020	**Instance**	UART1 UART2 UART3 UART4
Description	Mode definition register 1 The mode of operation can be programmed by writing to MDR1[2:0] and therefore the MDR1 must be programmed on startup after configuration of the configuration registers (UART_DLL, UART_DLH, and UART_LCR). The value of MDR1[2:0] must not be changed again during normal operation. **Note:** If the module is disabled by setting the MODE_SELECT field to 111, interrupt requests can still be generated unless disabled through the interrupt enable register (IER). In this case, UART mode interrupts are visible. Reading the interrupt identification register (IIR) shows UART mode interrupt flags.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								FRAME_END_MODE	SIP_MODE	SCT	SET_TXIR	IR_SLEEP	MODE_SELECT		

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Read returns 0. Write has no effect.	RW	0x000000
7	FRAME_END_MODE	IrDA mode only 0x0: Frame-length method 0x1: Set EOT bit method	RW	0
6	SIP_MODE	MIR/FIR modes only 0x0: Manual SIP mode: SIP is generated with the control of ACREG[3]. 0x1: Automatic SIP mode: SIP is generated after each transmission.	RW	0
5	SCT	Store and control the transmission. 0x0: Starts the infrared transmission when a value is written to THR 0x1: Starts the infrared transmission with the control of ACREG[2]. **Note:** Before starting any transmission, there must be no reception ongoing.	RW	0
4	SET_TXIR	Used to configure the infrared transceiver 0x0: a) No action if MDR2[7] = 0 b) TXIR pin output is forced low if MDR2[7] = 1. 0x1: IRTX pin output is forced high (not dependent on MDR2[7] value).	RW	0
3	IR_SLEEP	0x0: IrDA/CIR sleep mode disabled 0x1: IrDA/CIR sleep mode enabled	RW	0
2:0	MODE_SELECT	0x0: UART 16x mode 0x1: SIR mode 0x2: UART 16x auto-baud 0x3: UART 13x mode 0x4: MIR mode 0x5: FIR mode	RW	0x7

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Bits	Field Name	Description	Type	Reset
		0x6: CIR mode		
		0x7: Disable (default state)		

Table 23-207. Register Call Summary for Register UART_MDR1

UART/IrDA/CIR

- Description: [0] [1]
- UART Protocol and Data Format: [2]
- Register Access Modes: [3] [4] [5] [6] [7] [8]
- UART/IrDA (SIR, MIR, FIR)/CIR Mode Selection: [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23] [24] [25] [26] [27]
- UART Mode: [28] [29] [30]
- IrDA Mode (UART3 Only): [31] [32] [33] [34] [35] [36]
- CIR Mode (UART3 Only): [37]
- Quick Start: [38] [39] [40]
- SIR Mode: [41] [42] [43] [44] [45]
- MIR Mode: [46] [47] [48] [49]
- FIR Mode: [50] [51] [52] [53]
- UART/IrDA/CIR Register Summary: [54] [55]
- UART/IrDA/CIR Registers: [56]

Table 23-208. UART_MDR2

Address Offset	0x0000 0024		
Physical Address	0x4806 A024 0x4806 C024 0x4802 0024 0x4806 E024	**Instance**	UART1 UART2 UART3 UART4
Description	Mode definition register 2 IR-IrDA and IR-CIR modes only. UART_MDR2[0] describes the status of the interrupt in UART_IIR[5]. The IRTX_UNDERRUN bit should be read after an UART_IIR[5] TX_STATUS_IT interrupt. The bits [2:1] of this register set the trigger level for the frame status FIFO (8 entries) and must be programmed before the mode is programmed in UART_MDR1[2:0]. **Note:** The UART_MDR2[6] gives the flexibility to invert the RX pin in the UART to ensure that the protocol at the input of the transceiver module has the same polarity at module level. By default, the RX pin is inverted because most transceivers invert the IR receive pin.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								SET_TXIR_ALT	IRRXINVERT	CIR_PULSE_MODE		UART_PULSE	STS_FIFO_TRIG		IRTX_UNDERRUN

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Read returns 0. Write has no effect.	RW	0x000000
7	SET_TXIR_ALT	Provide alternate function for MDR1[4] (SET_TXIR).	R	0
		0x0: Normal mode		
		0x1: Alternate mode for SET_TXIR		

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Bits	Field Name	Description	Type	Reset
6	IRRXINVERT	IR mode only (IrDA and CIR). Invert RX pin in the module before the voting or sampling system logic of the infrared block. This does not affect the RX path in UART modem modes. 0x0: Inversion is performed. 0x1: No inversion is performed.	RW	0
5:4	CIR_PULSE_MODE	CIR pulse modulation definition. Defines high level of the pulse width associated with a digit: 0x0: Pulse width of 3 from 12 cycles 0x1: Pulse width of 4 from 12 cycles 0x2: Pulse width of 5 from 12 cycles 0x3: Pulse width of 6 from 12 cycles	RW	0x0
3	UART_PULSE	UART mode only. Allows pulse shaping in UART mode. 0x0: Normal UART mode 0x1: UART mode with a pulse shaping	RW	0
2:1	STS_FIFO_TRIG	IR-IrDA mode only. Frame status FIFO threshold select: 0x0: 1 entry 0x1: 4 entries 0x2: 7 entries 0x3: 8 entries	RW	0x0
0	IRTX_UNDERRUN	IrDA transmission status interrupt. When the UART_IIR[5] interrupt occurs, the meaning of the interrupt is: Read 0x0: The last bit of the frame transmitted successfully without error. Read 0x1: An underrun occurred. The last bit of the frame was transmitted but with an underrun error. The bit is reset to 0 when the UART_RESUME register is read.	R	0

Table 23-209. Register Call Summary for Register UART_MDR2

UART/IrDA/CIR

- IrDA Protocol and Data Format: [0]
- CIR Protocol and Data Format: [1]
- Register Access Modes: [2] [3] [4] [5] [6] [7]
- UART/IrDA (SIR, MIR, FIR)/CIR Mode Selection: [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23] [24] [25]
- IrDA Mode (UART3 Only): [26] [27]
- CIR Mode (UART3 Only): [28] [29]
- UART/IrDA/CIR Register Summary: [30] [31]
- UART/IrDA/CIR Registers: [32] [33]

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Table 23-210. UART_SFLSR

Address Offset	0x0000 0028		
Physical Address	0x4806 A028 0x4806 C028 0x4802 0028 0x4806 E028	**Instance**	UART1 UART2 UART3 UART4
Description	Status FIFO line status register IrDA modes only. Reading this register effectively reads frame status information from the status FIFO (this register does not physically exist). Reading this register increments the status FIFO read pointer (SFREGL and SFREGH must be read first).		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RESERVED			OE_ERROR	FRAME_TOO_LONG_ERROR	ABORT_DETECT	CRC_ERROR	RESERVED

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Read returns 0.	R	0x000000
7:5	RESERVED	Read returns 0.	R	0x0
4	OE_ERROR	Read 0x1: Overrun error in RX FIFO when frame at top of RX FIFO was received **Note:** Top of RX FIFO = Next frame to be read from RX FIFO	R	-
3	FRAME_TOO_LONG_ERROR	Read 0x1: Frame-length too long error in frame at top of RX FIFO	R	-
2	ABORT_DETECT	Read 0x1: Abort pattern detected in frame at top of RX FIFO	R	-
1	CRC_ERROR	Read 0x1: CRC error in frame at top of RX FIFO	R	-
0	RESERVED		R	0

Table 23-211. Register Call Summary for Register UART_SFLSR

UART/IrDA/CIR

- FIFO Management: [0]
- Register Access Modes: [1] [2] [3]
- UART/IrDA (SIR, MIR, FIR)/CIR Mode Selection: [4] [5] [6]
- IrDA Mode (UART3 Only): [7] [8]
- UART/IrDA/CIR Register Summary: [9] [10]
- UART/IrDA/CIR Registers: [11] [12]

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Table 23-212. UART_TXFLL

Address Offset	0x0000 0028		
Physical Address	0x4806 A028 0x4806 C028 0x4802 0028 0x4806 E028	**Instance**	UART1 UART2 UART3 UART4
Description	Transmit frame length register low IrDA modes only. The UART_TXFLL and UART_TXFLH registers hold the 13-bit transmit frame length (expressed in bytes). UART_TXFLL holds the LSBs and UART_TXFLH holds the MSBs. The frame length value is used if the frame length method of frame closing is used.		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								TXFLL							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Write has no effect.	W	0x000000
7:0	TXFLL	LSB register used to specify the frame length	W	0x00

Table 23-213. Register Call Summary for Register UART_TXFLL

UART/IrDA/CIR

- Register Access Modes: [0] [1] [2]
- UART/IrDA (SIR, MIR, FIR)/CIR Mode Selection: [3] [4] [5]
- IrDA Mode (UART3 Only): [6]
- SIR Mode: [7]
- MIR Mode: [8]
- FIR Mode: [9]
- UART/IrDA/CIR Register Summary: [10] [11]
- UART/IrDA/CIR Registers: [12] [13] [14] [15]

Table 23-214. UART_RESUME

Address Offset	0x0000 002C		
Physical Address	0x4806 A02C 0x4806 C02C 0x4802 002C 0x4806 E02C	**Instance**	UART1 UART2 UART3 UART4
Description	IR-IrDA and IR-CIR modes only. This register is used to clear internal flags, which halt transmission/reception when an underrun/overrun error occurs. Reading this register resumes the halted operation. This register does not physically exist and reads always as 0x00.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RESUME							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Read returns 0.	R	0x000000
7:0	RESUME	Dummy read to restart the TX or RX	R	0x00

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Table 23-215. Register Call Summary for Register UART_RESUME

UART/IrDA/CIR

- IrDA Mode Interrupt Management: [0] [1]
- Register Access Modes: [2] [3] [4]
- UART/IrDA (SIR, MIR, FIR)/CIR Mode Selection: [5] [6] [7] [8] [9] [10]
- UART Mode: [11]
- IrDA Mode (UART3 Only): [12]
- UART/IrDA/CIR Register Summary: [13] [14]
- UART/IrDA/CIR Registers: [15]

Table 23-216. UART_TXFLH

Address Offset	0x0000 002C		
Physical Address	0x4806 A02C 0x4806 C02C 0x4802 002C 0x4806 E02C	**Instance**	UART1 UART2 UART3 UART4
Description	Transmit frame length register high IrDA modes only. The UART_TXFLL and UART_TXFLH registers hold the 13-bit transmit frame length (expressed in bytes). UART_TXFLL holds the LSBs and UART_TXFLH holds the MSBs. The frame length value is used if the frame length method of frame closing is used.		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RESERVED			TXFLH				

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Write has no effect.	W	0x000000
7:5	RESERVED	Write has no effect.	W	0x0
4:0	TXFLH	MSB register used to specify the frame length	W	0x00

Table 23-217. Register Call Summary for Register UART_TXFLH

UART/IrDA/CIR

- Register Access Modes: [0] [1] [2]
- UART/IrDA (SIR, MIR, FIR)/CIR Mode Selection: [3] [4] [5]
- IrDA Mode (UART3 Only): [6]
- FIR Mode: [7]
- UART/IrDA/CIR Register Summary: [8] [9]
- UART/IrDA/CIR Registers: [10] [11] [12] [13]

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Table 23-218. UART_SFREGL

Address Offset	0x0000 0030		
Physical Address	0x4806 A030 0x4806 C030 0x4802 0030 0x4806 E030	**Instance**	UART1 UART2 UART3 UART4
Description	Status FIFO register low IrDA modes only. The frame lengths of received frames are written into the status FIFO. This information can be read by reading the UART_SFREGL and UART_SFREGH registers (these registers do not physically exist). The LsBs are read from UART_SFREGL and the MSBs are read from UART_SFREGH. Reading these registers does not alter the status FIFO read pointer. These registers should be read before the pointer is incremented by reading the UART_SFLSR register.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								SFREGL							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Read returns 0.	R	0x000000
7:0	SFREGL	LSB part of the frame length	R	0x-

Table 23-219. Register Call Summary for Register UART_SFREGL

UART/IrDA/CIR

- FIFO Management: [0]
- Register Access Modes: [1] [2] [3]
- UART/IrDA (SIR, MIR, FIR)/CIR Mode Selection: [4] [5] [6]
- IrDA Mode (UART3 Only): [7]
- UART/IrDA/CIR Register Summary: [8] [9]
- UART/IrDA/CIR Registers: [10] [11] [12] [13]

Table 23-220. UART_RXFLL

Address Offset	0x0000 0030		
Physical Address	0x4806 A030 0x4806 C030 0x4802 0030 0x4806 E030	**Instance**	UART1 UART2 UART3 UART4
Description	Received frame length register low IrDA modes only. The UART_RXFLL and UART_RXFLH registers hold the 12-bit receive maximum frame length. UART_RXFLL holds the LSBs and UART_RXFLH holds the MSBs. If the intended maximum receive frame length is n bytes, program the UART_RXFLL and UART_RXFLH registers to be n + 3 in SIR or MIR modes and n + 6 in FIR mode (+3 and +6 are the result of frame format with CRC and stop flag; 2 bytes are associated with the FIR stop flag).		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RXFLL							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Write has no effect.	W	0x000000
7:0	RXFLL	LSB register used to specify the frame length in reception	W	0x00

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Table 23-221. Register Call Summary for Register UART_RXFLL

UART/IrDA/CIR

- Register Access Modes: [0] [1] [2]
- UART/IrDA (SIR, MIR, FIR)/CIR Mode Selection: [3] [4] [5]
- FIR Mode: [6] [7]
- UART/IrDA/CIR Register Summary: [8] [9]
- UART/IrDA/CIR Registers: [10] [11] [12] [13] [14] [15]

Table 23-222. UART_SFREGH

Address Offset	0x0000 0034		
Physical Address	0x4806 A034 0x4806 C034 0x4802 0034 0x4806 E034	**Instance**	UART1 UART2 UART3 UART4
Description	Status FIFO register high IrDA modes only. The frame lengths of received frames are written into the status FIFO. This information can be read by reading the UART_SFREGL and UART_SFREGH registers (these registers do not physically exist). The LSBs are read from UART_SFREGL and the MSBs are read from UART_SFREGH. Reading these registers does not alter the status FIFO read pointer. These registers should be read before the pointer is incremented by reading the UART_SFLSR register.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RESERVED				SFREGH			

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Read returns 0.	R	0x000000
7:4	RESERVED	Read returns 0.	R	0x0
3:0	SFREGH	MSB part of the frame length	R	0x-

Table 23-223. Register Call Summary for Register UART_SFREGH

UART/IrDA/CIR

- FIFO Management: [0]
- Register Access Modes: [1] [2] [3]
- UART/IrDA (SIR, MIR, FIR)/CIR Mode Selection: [4] [5] [6]
- IrDA Mode (UART3 Only): [7]
- UART/IrDA/CIR Register Summary: [8] [9]
- UART/IrDA/CIR Registers: [10] [11] [12] [13]

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Table 23-224. UART_RXFLH

Address Offset	0x0000 0034		
Physical Address	0x4806 A034 0x4806 C034 0x4802 0034 0x4806 E034	**Instance**	UART1 UART2 UART3 UART4
Description	Received frame length register high IrDA modes only. The UART_RXFLL and UART_RXFLH registers hold the 12-bit receive maximum frame length. UART_RXFLL holds the LSBs and UART_RXFLH holds the MSBs. If the intended maximum receive frame length is n bytes, program the UART_RXFLL and UART_RXFLH to be n + 3 in SIR or MIR modes and n + 6 in FIR mode (+3 and +6 are the result of frame format with CRC and stop flag; 2 bytes are associated with the FIR stop flag).		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RESERVED				RXFLH			

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Write has no effect.	W	0x000000
7:4	RESERVED	Write has no effect.	W	0x0
3:0	RXFLH	MSB register used to specify the frame length in reception	W	0x0

Table 23-225. Register Call Summary for Register UART_RXFLH

UART/IrDA/CIR

- Register Access Modes: [0] [1] [2]
- UART/IrDA (SIR, MIR, FIR)/CIR Mode Selection: [3] [4] [5]
- FIR Mode: [6]
- UART/IrDA/CIR Register Summary: [7] [8]
- UART/IrDA/CIR Registers: [9] [10] [11] [12] [13] [14]

Table 23-226. UART_BLR

Address Offset	0x0000 0038		
Physical Address	0x4806 A038 0x4806 C038 0x4802 0038 0x4806 E038	**Instance**	UART1 UART2 UART3 UART4
Description	BOF control register IrDA modes only. The UART_BLR[6] bit selects whether 0xC0 or 0xFF start patterns are to be used, when multiple start flags are required in SIR mode. If only one start flag is required, this is always 0xC0. If n start flags are required, (-1) 0xC0 or (-1) 0xFF flags are sent, followed by a single 0xC0 flag (immediately preceding the first data byte).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								STS_FIFO_RESET	XBOF_TYPE	RESERVED					

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Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Read returns 0. Write has no effect.	RW	0x000000
7	STS_FIFO_RESET	Status FIFO reset. This bit is self-clearing.	RW	0
6	XBOF_TYPE	SIR xBOF select 0x0: 0xFF 0x1: 0xC0	RW	1
5:0	RESERVED	Read returns 0.	R	0x00

Table 23-227. Register Call Summary for Register UART_BLR

UART/IrDA/CIR

- IrDA Protocol and Data Format: [0]
- Register Access Modes: [1] [2]
- UART/IrDA (SIR, MIR, FIR)/CIR Mode Selection: [3] [4]
- UART/IrDA/CIR Register Summary: [5] [6]
- UART/IrDA/CIR Registers: [7]

Table 23-228. UART_UASR

Address Offset	0x0000 0038		
Physical Address	0x4806 A038 0x4806 C038 0x4802 0038 0x4806 E038	**Instance**	UART1 UART2 UART3 UART4
Description	UART autobauding status register UART autobauding mode only. This status register returns the speed, the number of bits by characters, and the type of the parity in UART autobauding mode. In autobauding mode, the input frequency of the UART modem must be fixed to 48 MHz. Any other module clock frequency results in incorrect baud rate recognition. **Note:** When the UART is in autobauding mode, this register, instead of the LCR, DLL, and DLH registers, is used to set up transmission according to the characteristics of the previous reception. To reset the autobauding hardware (to start a new AT detection), set MDR1[2:0] to 111 (reset value), then set MDR1[2:1] to 010 (UART in autobaud mode). To set the UART to standard mode (no autobaud), set MDR1[2:1] to 000.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								PARITY_TYPE		BIT_BY_CHAR	SPEED				

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Read returns 0.	R	0x000000
7:6	PARITY_TYPE	Read 0x0: No parity identified Read 0x1: Parity space Read 0x2: Even parity Read 0x3: Odd parity	R	0x0
5	BIT_BY_CHAR	Read 0x0: 7-bit character identified Read 0x1: 8-bit character identified	R	0
4:0	SPEED	Used to report the speed identified Read 0x0: No speed identified Read 0x1: 115,200 baud Read 0x2: 57,600 baud	R	0x00

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Bits	Field Name	Description	Type	Reset
		Read 0x3: 38,400 baud		
		Read 0x4: 28,800 baud		
		Read 0x5: 19,200 baud		
		Read 0x6: 14,400 baud		
		Read 0x7: 9,600 baud		
		Read 0x8: 4,800 baud		
		Read 0x9: 2,400 baud		
		Read 0xA: 1,200 baud		

Table 23-229. Register Call Summary for Register UART_UASR

UART/IrDA/CIR

- Register Access Modes: [0] [1]
- UART/IrDA (SIR, MIR, FIR)/CIR Mode Selection: [2] [3]
- UART Mode: [4] [5] [6]
- UART/IrDA/CIR Register Summary: [7] [8]

Table 23-230. UART_ACREG

Address Offset	0x0000 003C		
Physical Address	0x4806 A03C 0x4806 C03C 0x4802 003C 0x4806 E03C	**Instance**	UART1 UART2 UART3 UART4
Description	Auxiliary control register. IR-IrDA and IR-CIR modes only.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								PULSE_TYPE	SD_MOD	DIS_IR_RX	DIS_TX_UNDERRUN	SEND_SIP	SCTX_EN	ABORT_EN	EOT_EN

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Read returns 0. Write has no effect.	RW	0x000000
7	PULSE_TYPE	SIR pulse width select	RW	0
		0x0: 3/16 of baud-rate pulse width		
		0x1: 1.6 µs		
6	SD_MOD	Primary output used to configure transceivers. Connected to the SD/MODE input pin of IrDA transceivers.	RW	0
		0x0: SD pin is set to high.		
		0x1: SD pin is set to low.		
5	DIS_IR_RX	0x0: Normal operation (RX input automatically disabled during transmit but enabled outside of transmit operation)	RW	0
		0x1: Disables RX input (permanent state - independent of transmit)		
4	DIS_TX_UNDERRUN	It is recommended to disable TX FIFO underrun capability by masking corresponding underrun interrupt. When disabling underrun by setting ACREG[4] = 1, garbage data is sent over TX line.	RW	0

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Bits	Field Name	Description	Type	Reset
		0x0: Long stop-bits cannot be transmitted; TX underrun is enabled. 0x1: Long stop-bits can be transmitted; TX underrun is disabled.		
3	SEND_SIP	MIR/FIR modes only. Send serial infrared interaction pulse (SIP). If this bit is set during an MIR/FIR transmission, the SIP is sent at the end of it. This bit is cleared automatically at the end of the SIP transmission. 0x0: No action 0x1: Send SIP pulse.	RW	0
2	SCTX_EN	Store and controlled TX start. When MDR1[5] = 1 and the LH writes 1 to this bit, the TX state-machine starts frame transmission. This bit is self-clearing.	RW	0
1	ABORT_EN	Frame abort. The LH can intentionally abort transmission of a frame by writing 1 to this bit. Neither the end flag nor the CRC bits are appended to the frame. If TX FIFO is not empty and MDR1[5] = 1, UART IrDA starts a new transfer with data of the previous frame when the abort frame is sent. Therefore, TX FIFO must be reset before sending an abort frame.	RW	0
0	EOT_EN	EOT (end of transmission) bit. The LH writes 1 to this bit just before it writes the last byte to the TX FIFO in set-EOT bit frame closing method. This bit is cleared automatically when the LH writes to the THR (TX FIFO).	RW	0

Table 23-231. Register Call Summary for Register UART_ACREG

UART/IrDA/CIR

- UART3 Interface Description: [0]
- IrDA Protocol and Data Format: [1] [2] [3] [4]
- CIR Interface Description: [5]
- Register Access Modes: [6] [7]
- UART/IrDA (SIR, MIR, FIR)/CIR Mode Selection: [8] [9] [10] [11]
- IrDA Mode (UART3 Only): [12] [13] [14] [15] [16] [17] [18]
- CIR Mode (UART3 Only): [19]
- SIR Mode: [20]
- MIR Mode: [21]
- FIR Mode: [22]
- UART/IrDA/CIR Register Summary: [23] [24]

Table 23-232. UART_SCR

Address Offset	0x0000 0040		
Physical Address	0x4806 A040 0x4806 C040 0x4802 0040 0x4806 E040	**Instance**	UART1 UART2 UART3 UART4
Description	Supplementary control register **Note:** Bit 4 enables the wake-up interrupt, but this interrupt is not mapped into the UART_IIR register. Therefore, when an interrupt occurs and there is no interrupt pending in the UART_IIR register, the SSR[1] bit must be checked. To clear the wake-up interrupt, bit UART_SCR[4] must be reset to 0.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RX_TRIG_GRANU1	TX_TRIG_GRANU1	DSR_IT	RX_CTS_DSR_WAKE_UP_ENABLE	TX_EMPTY_CTL_IT	DMA_MODE_2		DMA_MODE_CTL

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Read returns 0. Write has no effect.	RW	0x000000
7	RX_TRIG_GRANU1	0x0: Disables the granularity of 1 for trigger RX level 0x1: Enables the granularity of 1 for trigger RX level	RW	0
6	TX_TRIG_GRANU1	0x0: Disables the granularity of 1 for trigger TX level 0x1: Enables the granularity of 1 for trigger TX level	RW	0
5	DSR_IT	0x0: Disables DSR* interrupt 0x1: Enables DSR* interrupt	RW	0
4	RX_CTS_DSR_WAKE_UP_ENABLE	0x0: Disables the wake-up interrupt and clears SSR[1] 0x1: Waits for a falling edge of pins RX, CTS*, or DSR* to generate an interrupt	RW	0
3	TX_EMPTY_CTL_IT	0x0: Normal mode for THR interrupt (see UART mode interrupts table) 0x1: The THR interrupt is generated when TX FIFO and TX shift register are empty.	RW	0
2:1	DMA_MODE_2	Used to specify the DMA mode valid if the UART_SCR[0] bit = 1 0x0: DMA mode 0 (no DMA) 0x1: DMA mode 1 (UART_nDMA_REQ[0] in TX, UART_nDMA_REQ[1] in RX) 0x2: DMA mode 2 (UART_nDMA_REQ[0] in RX) 0x3: DMA mode 3 (UART_nDMA_REQ[0] in TX)	RW	0x0
0	DMA_MODE_CTL	0x0: The DMA_MODE is set with UART_FCR[3]. 0x1: The DMA_MODE is set with UART_SCR[2:1].	RW	0

Table 23-233. Register Call Summary for Register UART_SCR

UART/IrDA/CIR

- UART Mode Power Management: [0]
- UART Mode Interrupt Management: [1] [2]
- FIFO Management: [3]
- FIFO Trigger: [4] [5]
- FIFO DMA Mode Operation: [6] [7]
- Register Access Modes: [8] [9] [10] [11] [12] [13]
- UART/IrDA (SIR, MIR, FIR)/CIR Mode Selection: [14] [15] [16] [17] [18] [19] [20] [21] [22] [23] [24] [25] [26] [27] [28] [29] [30] [31]
- Quick Start: [32] [33] [34] [35] [36] [37] [38] [39]
- UART/IrDA/CIR Register Summary: [40] [41]
- UART/IrDA/CIR Registers: [42] [43] [44] [45] [46] [47] [48] [49] [50] [51] [52] [53] [54]

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Table 23-234. UART_SSR

Address Offset	0x0000 0044		
Physical Address	0x4806 A044 0x4806 C044 0x4802 0044 0x4806 E044	**Instance**	UART1 UART2 UART3 UART4
Description	Supplementary status register **Note:** Bit 1 is reset only when UART_SCR[4] is reset to 0.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RESERVED					DMA_COUNTER_RST	RX_CTS_DSR_WAKE_UP_STS	TX_FIFO_FULL

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Read returns 0.	R	0x000000
7:3	RESERVED	Read returns 0.	R	0x00
2	DMA_COUNTER_RST	0x0: The DMA counter will not be reset if the corresponding FIFO is reset (through FCR[1] or FCR[2]). 0x1: The DMA counter will be reset if corresponding FIFO is reset (through FCR[1] or FCR[2]).	RW	1
1	RX_CTS_DSR_WAKE_UP_STS	Read 0x0: No falling edge event on RX, CTS*, and DSR* Read 0x1: A falling edge occurred on RX, CTS*, or DSR*.	R	0
0	TX_FIFO_FULL	Read 0x0: TX FIFO is not full. Read 0x1: TX FIFO is full.	R	0

Table 23-235. Register Call Summary for Register UART_SSR

UART/IrDA/CIR

- UART Mode Interrupt Management: [0]
- FIFO Management: [1]
- Register Access Modes: [2] [3] [4]
- UART/IrDA (SIR, MIR, FIR)/CIR Mode Selection: [5] [6] [7] [8] [9] [10] [11] [12] [13]
- UART/IrDA/CIR Register Summary: [14] [15]

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Table 23-236. UART_EBLR

Address Offset	0x0000 0048		
Physical Address	0x4806 A048 0x4806 C048 0x4802 0048 0x4806 E048	**Instance**	UART1 UART2 UART3 UART4
Description	BOF length register IR-IrDA and IR-CIR modes only. In IR-IrDA SIR operation, this register specifies the number of BOF + xBOFs to transmit. Value set into this register must account for the BOF character; therefore, to send only one BOF with no XBOF, this register must be set to 1. To send one BOF with N XBOF, this register must be set to N + 1. The value 0 sends 1 BOF plus 255 XBOF. In IR-IrDA MIR mode, this register specifies the number of additional start flags (MIR protocol mandates a minimum of 2 start flags). In IR-CIR mode, this register specifies the number of consecutive 0s to be received before generating the RX_STOP interrupt (UART_IIR[2]). All received 0s are stored in the RX FIFO. When the register is set to 0, this feature is deactivated and always in reception state, which can be disabled by setting the ACREG[5] to 1. **Note:** If the RX_STOP interrupt occurs before a byte boundary, the remaining bits of the last byte are filled with 0s and passed into the RX FIFO.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								EBLR							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Read returns 0. Write has no effect.	RW	0x000000
7:0	EBLR	IR-IrDA mode: This register allows definition of up to 176 xBOFs, the maximum required by IrDA specification. IR-CIR mode: This register specifies the number of consecutive 0s to be received before generating the RX_STOP interrupt (UART_IIR[2]). 0x00: Feature disabled 0x01: Generate RX_STOP interrupt after receiving one zero bit. ... 0xFF: Generate RX_STOP interrupt after receiving 255 zero bits.	RW	0x00

Table 23-237. Register Call Summary for Register UART_EBLR

UART/IrDA/CIR

- Register Access Modes: [0] [1]
- UART/IrDA (SIR, MIR, FIR)/CIR Mode Selection: [2] [3] [4] [5]
- SIR Mode: [6]
- MIR Mode: [7]
- FIR Mode: [8]
- UART/IrDA/CIR Register Summary: [9] [10]
- UART/IrDA/CIR Registers: [11]

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Table 23-238. UART_MVR

Address Offset	0x0000 0050		
Physical Address	0x4806 A050 0x4806 C050 0x4802 0050 0x4806 E050	**Instance**	UART1 UART2 UART3 UART4
Description	Module version register The reset value is fixed by hardware and corresponds to the RTL revision of this module. A reset has no effect on the value returned.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REV																															

Bits	Field Name	Description	Type	Reset
31:0	REV	Revision number	R	0x-- TI internal data

Table 23-239. Register Call Summary for Register UART_MVR

UART/IrDA/CIR

- Register Access Modes: [0] [1] [2]
- UART/IrDA (SIR, MIR, FIR)/CIR Mode Selection: [3] [4] [5] [6] [7] [8] [9] [10] [11]
- UART/IrDA/CIR Register Summary: [12] [13]

Table 23-240. UART_SYSC

Address Offset	0x0000 0054		
Physical Address	0x4806 A054 0x4806 C054 0x4802 0054 0x4806 E054	**Instance**	UART1 UART2 UART3 UART4
Description	System configuration register The AUTOIDLE bit controls a power-saving technique to reduce the logic power consumption of the open-core protocol (OCP) interface. When the feature is enabled, the clock is gated off until an OCP command for this device is detected. When the software reset bit is set high, it causes a full device reset.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RESERVED			IDLEMODE		ENAWAKEUP	SOFTRESET	AUTOIDLE

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Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Read returns 0. Write has no effect.	RW	0x000000
7:5	RESERVED	Read returns 0.	R	0x0
4:3	IDLEMODE	Power management req/ack control ref: OCP Design Guidelines Version 1.1 0x0: Force-idle: Idle request is acknowledged unconditionally. 0x1: No-idle: Idle request is never acknowledged. 0x2: Smart-idle: Idle request is acknowledged based in module internal activity. 0x3: Smart-idle Wake-up: Acknowledgement to an idle request is given based in the internal activity of the module. The module is allowed to generate wake-up request.	RW	0x0
2	ENAWAKEUP	Wake-up feature control 0x0: Wakeup is disabled. 0x1: Wake-up capability is enabled.	RW	0
1	SOFTRESET	Software reset. Set this bit to 1 to trigger a module reset. This bit is automatically reset by the hardware. Read returns 0. 0x0: Normal mode 0x1: The module is reset.	RW	0
0	AUTOIDLE	Internal OCP clock gating strategy 0x0: Clock is running. 0x1: Automatic OCP clock gating strategy is applied, based on OCP interface activity	RW	0

Table 23-241. Register Call Summary for Register UART_SYSC

UART/IrDA/CIR

- Clock Configuration: [0]
- Software Reset: [1]
- UART Mode Power Management: [2]
- Local Power Management: [3] [4] [5]
- Register Access Modes: [6] [7] [8] [9] [10] [11]
- UART/IrDA (SIR, MIR, FIR)/CIR Mode Selection: [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23] [24] [25] [26] [27] [28] [29]
- Quick Start: [30]
- UART/IrDA/CIR Register Summary: [31] [32]

Table 23-242. UART_SYSS

Address Offset	0x0000 0058		
Physical Address	0x4806 A058 0x4806 C058 0x4802 0058 0x4806 E058	**Instance**	UART1 UART2 UART3 UART4
Description	System status register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RESERVED							RESETDONE

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Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Read returns 0.	R	0x000000
7:1	RESERVED	Read returns 0.	R	0x00
0	RESETDONE	Internal reset monitoring Read 0x0: Internal module reset is ongoing. Read 0x1: Reset complete	R	0

Table 23-243. Register Call Summary for Register UART_SYSS

UART/IrDA/CIR

- Register Access Modes: [0] [1] [2]
- UART/IrDA (SIR, MIR, FIR)/CIR Mode Selection: [3] [4] [5] [6] [7] [8] [9] [10] [11]
- Quick Start: [12]
- UART/IrDA/CIR Register Summary: [13] [14]

Table 23-244. UART_WER

Address Offset	0x0000 005C		
Physical Address	0x4806 A05C 0x4806 C05C 0x4802 005C 0x4806 E05C	**Instance**	UART1 UART2 UART3 UART4
Description	Wake-up enable register The UART wake-up enable register is used to mask and unmask a UART event that would subsequently notify the system. An event is any activity in the logic that could cause an interrupt and/or an activity that would require the system to wake up. Even if the wakeup is disabled for certain events, if these events are also an interrupt to the UART, the UART registers the interrupt.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								TX_WAKEUP_EN	EVENT_6_RECEIVER_LINE_STATUS_INTERRUPT	EVENT_5_RHR_INTERRUPT	EVENT_4_RX_ACTIVITY	EVENT_3_DCD_CD_ACTIVITY	EVENT_2_RI_ACTIVITY	EVENT_1_DSR_ACTIVITY	EVENT_0_CTS_ACTIVITY

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Read returns 0. Write has no effect.	RW	0x000000
7	TX_WAKEUP_EN	0x0: Event is not allowed to wake up the system. 0x1: Event can wake up the system: it can be THR_IT or TX_DMA request and/or TX_SATUS_IT.	RW	0
6	EVENT_6_RECEIVER_LINE_STATUS_INTERRUPT	0x0: Event is not allowed to wake up the system. 0x1: Event can wake up the system.	RW	1

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Bits	Field Name	Description	Type	Reset
5	EVENT_5_RHR_INTERRUPT	0x0: Event is not allowed to wake up the system. 0x1: Event can wake up the system.	RW	1
4	EVENT_4_RX_ACTIVITY	0x0: Event is not allowed to wake up the system. 0x1: Event can wake up the system.	RW	1
3	EVENT_3_DCD_CD_ACTIVITY	0x0: Event is not allowed to wake up the system 0x1: Event can wake up the system	RW	1
2	EVENT_2_RI_ACTIVITY	0x0: Event is not allowed to wake up the system. 0x1: Event can wake up the system.	RW	1
1	EVENT_1_DSR_ACTIVITY	0x0: Event is not allowed to wake up the system. 0x1: Event can wake up the system.	RW	1
0	EVENT_0_CTS_ACTIVITY	0x0: Event is not allowed to wake up the system. 0x1: Event can wake up the system.	RW	1

Table 23-245. Register Call Summary for Register UART_WER

UART/IrDA/CIR

- UART Mode Power Management: [0]
- Register Access Modes: [1] [2] [3] [4] [5] [6]
- UART/IrDA (SIR, MIR, FIR)/CIR Mode Selection: [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23] [24]
- UART/IrDA/CIR Register Summary: [25] [26]

Table 23-246. UART_CFPS

Address Offset	0x0000 0060		
Physical Address	0x4806 A060 0x4806 C060 0x4802 0060 0x4806 E060	**Instance**	UART1 UART2 UART3 UART4
Description	Carrier frequency prescaler Because the consumer IR works at modulation rates of 30 to 56.8 kHz, the 48-MHz clock must be prescaled before the clock can drive the IR logic. This register sets the divisor rate to give a range to accommodate the remote-control requirements in baud multiples of 12x. The value of the CFPS at reset is 0105 decimal, which equals 38.1 kHz output from starting conditions. The 48-MHz carrier is prescaled by the CFPS, which is then divided by the 12x baud multiple.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								CFPS							

Bits	Field Name	Description			Type	Reset
31:8	RESERVED	Read returns 0. Write has no effect.			RW	0x000000
7:0	CFPS	System clock frequency prescaler at (12x multiple). Examples for CFPS values:			RW	0x69
		Target Freq (kHz)	**CFPS (decimal)**	**Actual Freq (kHz)**		
		30	133	30.08		
		32.75	122	32.79		
		36	111	36.04		
		36.7	109	36.69		
		38*	105	38.1		
		40	100	40		
		56.8	70	57.14		
		*configured at reset to this value				
		Note: CFPS = 0 is not supported.				

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Table 23-247. Register Call Summary for Register UART_CFPS

UART/IrDA/CIR

- Register Access Modes: [0] [1] [2] [3] [4] [5]
- UART/IrDA (SIR, MIR, FIR)/CIR Mode Selection: [6] [7] [8] [9] [10] [11]
- CIR Mode (UART3 Only): [12] [13] [14]
- UART/IrDA/CIR Register Summary: [15] [16]

Table 23-248. UART_RXFIFO_LVL

Address Offset	0x0000 0064		
Physical Address	0x4806 A064 0x4806 C064 0x4802 0064 0x4806 E064	**Instance**	UART1 UART2 UART3 UART4
Description	Level of the RX FIFO		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RXFIFO_LVL							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Read returns 0.	R	0x000000
7:0	RXFIFO_LVL	Shows the number of received bytes in the RX FIFO	R	0x00

Table 23-249. Register Call Summary for Register UART_RXFIFO_LVL

UART/IrDA/CIR

- Register Access Modes: [0] [1] [2] [3] [4] [5]
- UART/IrDA (SIR, MIR, FIR)/CIR Mode Selection: [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23]
- UART/IrDA/CIR Register Summary: [24] [25]

Table 23-250. UART_TXFIFO_LVL

Address Offset	0x0000 0068		
Physical Address	0x4806 A068 0x4806 C068 0x4802 0068 0x4806 E068	**Instance**	UART1 UART2 UART3 UART4
Description	Level of the TX FIFO		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								TXFIFO_LVL							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Read returns 0.	R	0x000000
7:0	TXFIFO_LVL	Shows the number of written bytes in the TX FIFO	R	0x00

Table 23-251. Register Call Summary for Register UART_TXFIFO_LVL

UART/IrDA/CIR

- Register Access Modes: [0] [1] [2] [3] [4] [5]
- UART/IrDA (SIR, MIR, FIR)/CIR Mode Selection: [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23]
- UART/IrDA/CIR Register Summary: [24] [25]

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Table 23-252. UART_IER2

Address Offset	0x0000 006C		
Physical Address	0x4806 A06C 0x4806 C06C 0x4802 006C 0x4806 E06C	**Instance**	UART1 UART2 UART3 UART4
Description	Enables RX/TX FIFOs empty corresponding interrupts		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														EN_TXFIFO_EMPTY	EN_RXFIFO_EMPTY

Bits	Field Name	Description	Type	Reset
31:2	RESERVED	Read returns 0. Write has no effect.	RW	0x0000 0000
1	EN_TXFIFO_EMPTY	Enables TX FIFO empty corresponding interrupt 0x0: Enables EN_TXFIFO_EMPTY interrupt 0x1: Disables EN_TXFIFO_EMPTY interrupt	RW	0
0	EN_RXFIFO_EMPTY	Enables RX FIFO empty corresponding interrupt 0x0: Enables EN_RXFIFO_EMPTY interrupt 0x1: Disables EN_RXFIFO_EMPTY interrupt	RW	0

Table 23-253. Register Call Summary for Register UART_IER2

UART/IrDA/CIR

- Register Access Modes: [0] [1] [2] [3] [4] [5]
- UART/IrDA (SIR, MIR, FIR)/CIR Mode Selection: [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23]
- UART/IrDA/CIR Register Summary: [24] [25]

Table 23-254. UART_ISR2

Address Offset	0x0000 0070		
Physical Address	0x4806 A070 0x4806 C070 0x4802 0070 0x4806 E070	**Instance**	UART1 UART2 UART3 UART4
Description	Status of RX/TX FIFOs empty corresponding interrupts		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														TXFIFO_EMPTY_STS	RXFIFO_EMPTY_STS

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Bits	Field Name	Description	Type	Reset
31:2	RESERVED	Read returns 0. Write has no effect.	RW	0x0000 0000
1	TXFIFO_EMPTY_STS	Used to generate interrupt if the TX_FIFO is empty (software flow control) 0x0: TXFIFO_EMPTY interrupt not pending. 0x1: TXFIFO_EMPTY interrupt pending.	RW	1
0	RXFIFO_EMPTY_STS	Used to generate interrupt if the RX_FIFO is empty (software flow control) 0x0: RXFIFO_EMPTY interrupt not pending. 0x1: RXFIFO_EMPTY interrupt pending.	RW	1

Table 23-255. Register Call Summary for Register UART_ISR2

UART/IrDA/CIR
- Register Access Modes: [0] [1] [2] [3] [4] [5]
- UART/IrDA (SIR, MIR, FIR)/CIR Mode Selection: [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23]
- UART/IrDA/CIR Register Summary: [24] [25]

Table 23-256. UART_FREQ_SEL

Address Offset	0x0000 0074		
Physical Address	0x4806 A074 0x4806 C074 0x4802 0074 0x4806 E074	**Instance**	UART1 UART2 UART3 UART4
Description	Sample per bit selector		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								FREQ_SEL							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Read returns 0. Write has no effect.	RW	0x0000 0000
7:0	FREQ_SEL	Sets the sample per bit if nondefault frequency is used. MDR3[1] must be set to 1 after this value is set. Must be equal to or higher then 6.	RW	0x1A

Table 23-257. Register Call Summary for Register UART_FREQ_SEL

UART/IrDA/CIR
- Register Access Modes: [0] [1] [2] [3] [4] [5]
- UART/IrDA (SIR, MIR, FIR)/CIR Mode Selection: [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23]
- UART/IrDA/CIR Register Summary: [24] [25]

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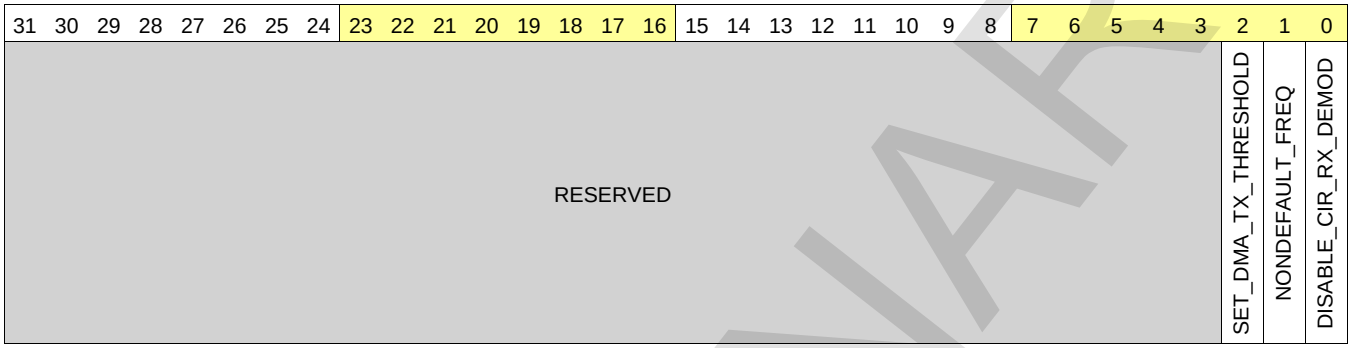
Table 23-258. UART_MDR3

Address Offset	0x0000 0080		
Physical Address	0x4806 A080 0x4806 C080 0x4802 0080 0x4806 E080	**Instance**	UART1 UART2 UART3 UART4
Description	Mode definition register 3		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:3	RESERVED	Read returns 0. Write has no effect.	RW	0x0000 0000
2	SET_DMA_TX_THRESHOLD	Enable to set different TXDMA threshold in UART_TX_DMA_THRESHOLD register.	RW	0
1	NONDEFAULT_FREQ	Used to enable the NONDEFAULT fclk frequencies. 0x0: Disables using NONDEFAULT fclk frequencies. 0x1: Enables using NONDEFAULT fclk frequencies (set FREQ_SEL and DLH/DLL).	RW	0
0	DISABLE_CIR_RX_DEMOD	Used to enable CIR RX demodulation. 0x0: Enables CIR RX demodulation. 0x1: Disables CIR RX demodulation.	RW	0

Table 23-259. Register Call Summary for Register UART_MDR3

UART/IrDA/CIR

- FIFO DMA Mode Operation: [0] [1] [2]
- Register Access Modes: [3] [4] [5] [6] [7] [8]
- UART/IrDA (SIR, MIR, FIR)/CIR Mode Selection: [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23] [24] [25] [26]
- UART/IrDA/CIR Register Summary: [27] [28]
- UART/IrDA/CIR Registers: [29]

Table 23-260. UART_TX_DMA_THRESHOLD

Address Offset	0x0000 0084		
Physical Address	0x4806 A084 0x4806 C084 0x4806 A084 0x4806 C084	**Instance**	UART1 UART2 UART3 UART4
Description	Use to manually set the TX DMA threshold level. UART_MDR3[2] SET_TX_DMA_THRESHOLD must be 1 and must be value + tx_trigger_level = 64 (TX FIFO size). If not, 64-tx_trigger_level will be used without modifying the value of this register.		
Type	RW		

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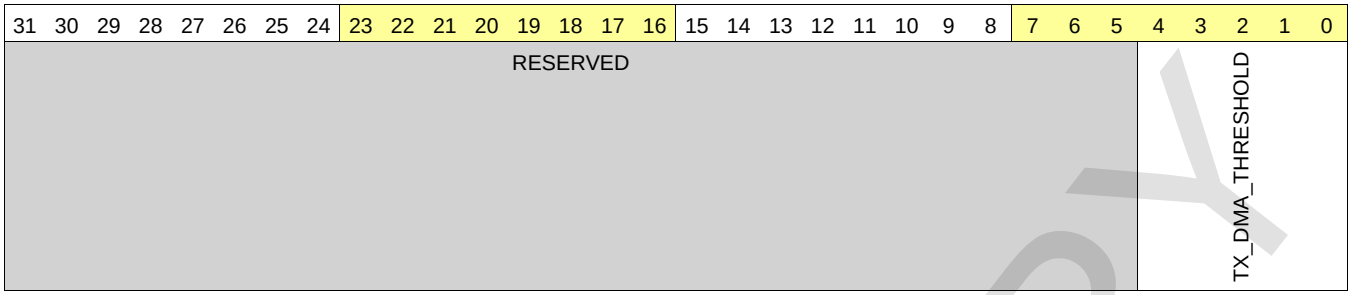

Bits	Field Name	Description	Type	Reset
31:5	RESERVED	Reserved	RW	0x0000000
4:0	TX_DMA_THRESHOLD	Used to manually set the TX DMA threshold level	RW	0x00

Table 23-261. Register Call Summary for Register UART_TX_DMA_THRESHOLD

UART/IrDA/CIR

- FIFO DMA Mode Operation: [0] [1] [2]
- Register Access Modes: [3] [4] [5] [6] [7] [8]
- UART/IrDA (SIR, MIR, FIR)/CIR Mode Selection: [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23] [24] [25] [26]
- UART/IrDA/CIR Register Summary: [27] [28]
- UART/IrDA/CIR Registers: [29]

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23.4 Multichannel Serial Port Interface

This section describes the four multichannel serial port interface (MCSPI) modules for the device.

23.4.1 MCSPI Overview

The MCSPI is a master/slave synchronous serial bus. The MCSPI has four separate modules (SPI1, SPI2, SPI3, and SPI4) in the device (see Figure 23-86). The MCSPI modules differ as follows: SPI1 supports up to four peripherals, SPI2 supports up to two peripherals, SPI3 and SPI4 support only one peripheral.

NOTE: In this chapter, *m = [1,4]* represents the module instance and *x* represents the channel in signal and register naming. The MCSPI has four instances, with each module instance having different channel numbers:

- SPI1: 4 channels (if *m = 1*, *x = 4*)
- SPI2: 2 channels (if *m = 2*, *x = 2*)
- SPI3: 1 channel (if *m = 3*, *x = 1*)
- SPI4: 1 channel (if *m = 4*, *x = 1*)

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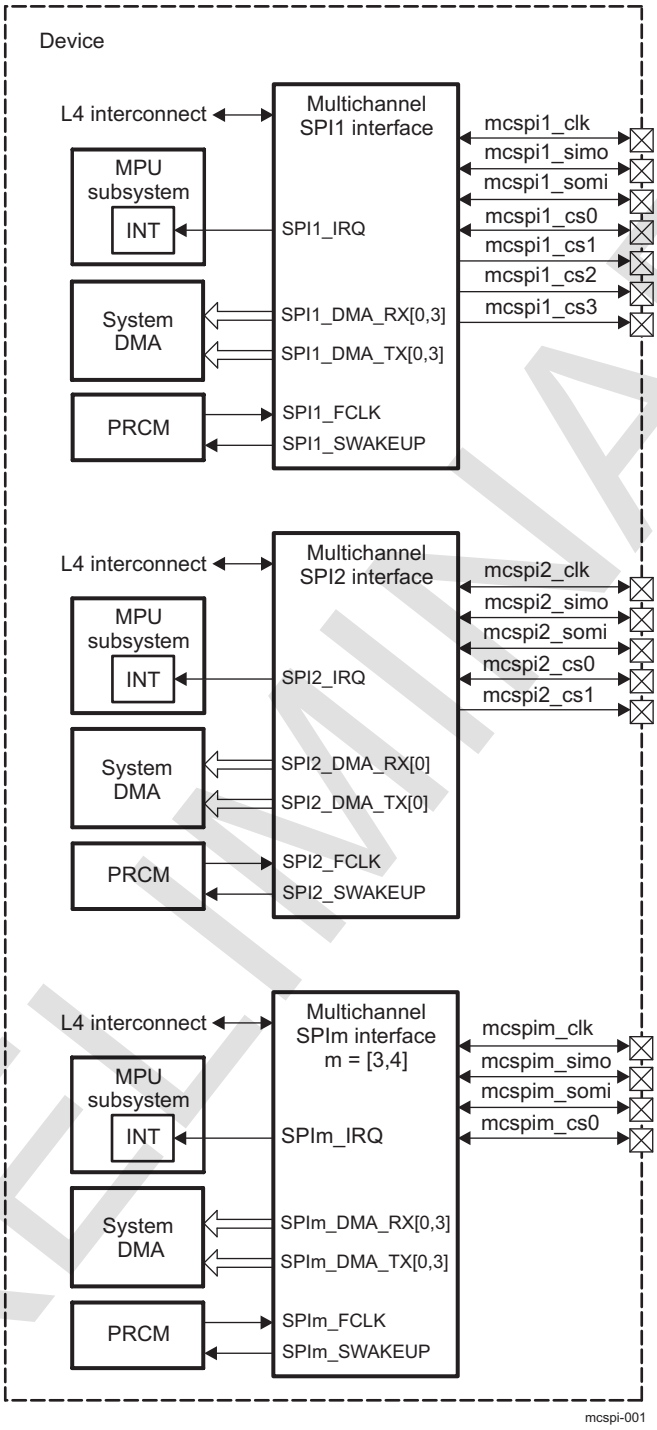
Figure 23-86. Multichannel Modules SPI1, SPI2, SPI3, and SPI4



The MCSPI instances include the following main features:

- Serial clock with programmable frequency, polarity, and phase for each channel
- Wide selection of SPI word lengths, ranging from 4 to 32 bits
- Up to four master channels, or single channel in slave mode
- Master multichannel mode:
  - Full duplex/half duplex
  - Transmit-only/receive-only/transmit-and-receive modes

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  - Flexible I/O port controls per channel
  - Two DMA requests (read/write) per channel
- Single interrupt line for multiple interrupt source events
- Power management through wake-up capabilities
- Enable the addition of a programmable start-bit for SPI transfer per channel (start-bit mode)
- Supports start-bit write command
- Supports start-bit pause and break sequence
- 64-byte built-in FIFO available for a single channel
- Force CS mode for continuous transfers

23.4.2 MCSPI Environment

Figure 23-87 shows a simplified overview of a typical application system using the MCSPI. This example is based on a TFS chip set, including a 2.2-inch color-active matrix thin-film transistor (TFT) liquid crystal display (LCD) with a light-emitting diode (LED) front light, a 4-wire resistive touch-screen panel, and LCD controllers. This chip set is associated with a touch-screen controller, powered by a power-management unit, and driven by the device. The MCSPI device interface is set to master mode; the touch-screen MCSPI controller interface operates in slave mode.

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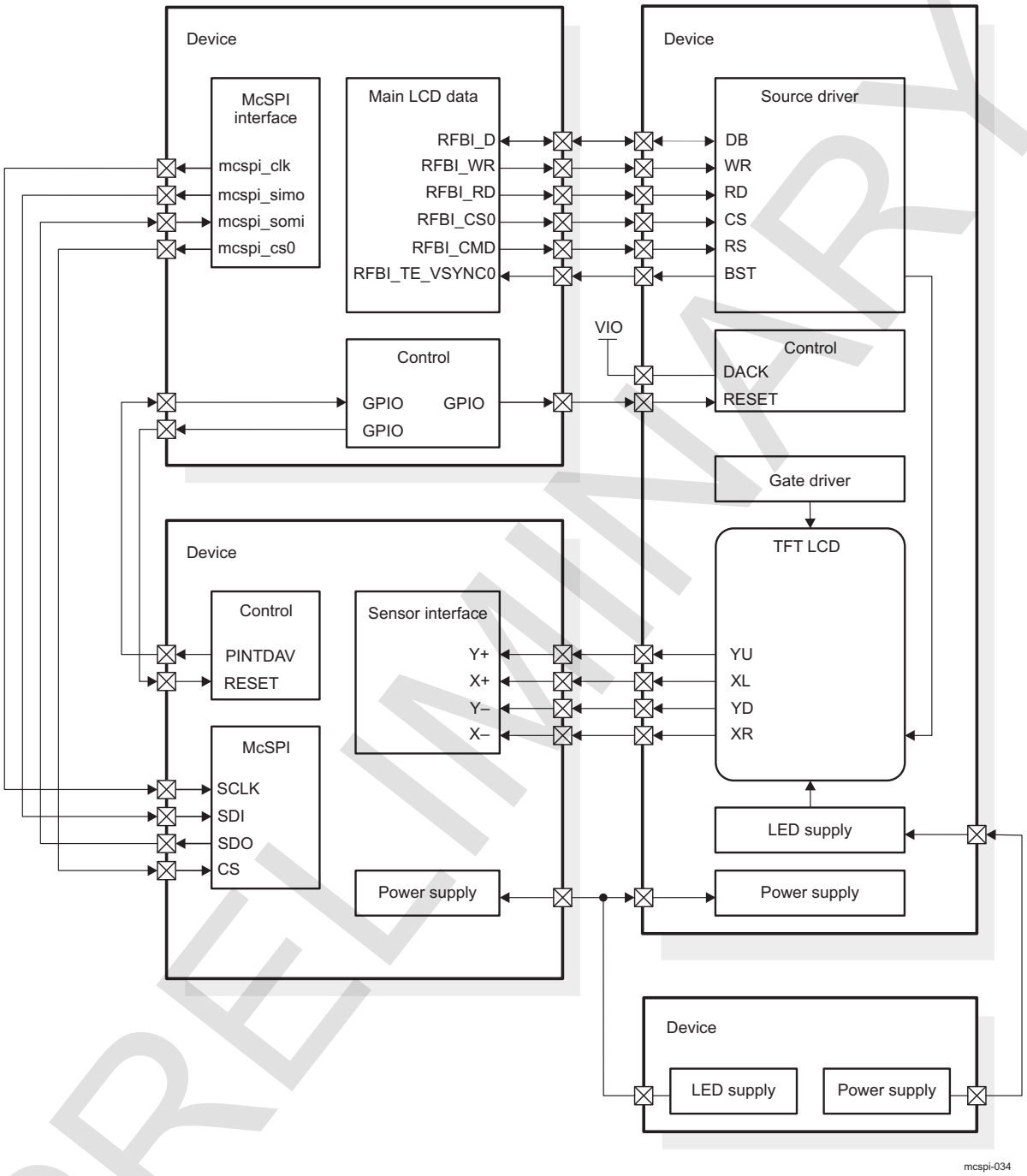
Figure 23-87. Typical Application Using the MCSPI



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23.4.2.1 MCSPI Interface

23.4.2.1.1 Basic MCSPI Pins for Master Mode

Figure 23-88 shows all of the MCSPI interface signals in master mode.

Figure 23-88. MCSPI Interface Signals in Master Mode

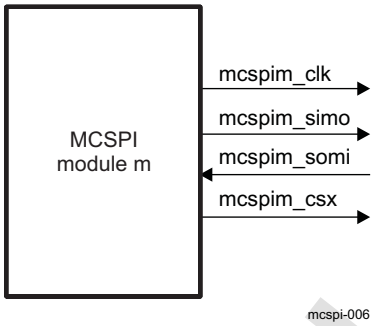

Table 23-262 describes the MCSPI I/O in master mode.

Table 23-262. MCSPI I/O Description (Master Mode)

Signal Name	I/O	Description	Reset [(1)]
mcspim_clk	O	SPIm module serial clock	Unknown
mcspim_simo	O	SPIm module serial data master out (slave input, master output)	Unknown
mcspim_somi	I	SPIm module serial data master input (slave output, master input)	–
mcspim_csx	O	SPIm module chip-select x output	Low

(1) After reset, the SPI modules are in slave mode by default. This paragraph implies that the MCSPI module is configured in slave mode. (See the MCSPI_MODULCTRL[2] MS bit in the module control register [MCSPI_MODULCTRL]).

23.4.2.1.2 Basic MCSPI Pins for Slave Mode

Figure 23-89 shows all of the MCSPI interface signals in slave mode.

Figure 23-89. MCSPI Interface Signals in Slave Mode

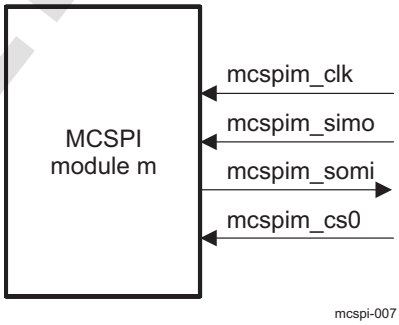

Table 23-263 describes the MCSPI I/O in slave mode.

Table 23-263. MCSPI I/O Description (Slave Mode)

Signal Name	I/O	Description	Reset [(1)]
mcspim_clk	I	SPIm module serial clock	Unknown

(1) After reset, the SPI modules are in slave mode by default. This paragraph implies that the MCSPI module is configured in slave mode. (See the MCSPI_MODULCTRL[2] MS bit in the module control register (MCSPI_MODULCTRL).)

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Table 23-263. MCSPI I/O Description (Slave Mode) (continued)

Signal Name	I/O	Description	Reset [1]
mcspim_simo	I	SPIm module serial data master out (slave input, master output)	Unknown
mcspim_somi	O	SPIm module serial data master input (slave output, master input)	–
mcspim_csx	I	SPIm module chip-select x output	Low

23.4.2.1.3 Multichannel SPI Protocol and Data Format

The synchronous SPI protocol allows a master device to initiate serial data transfers to a slave device. A slave select line (mcspim_csx) allows selection of an individual slave SPI device. Slave devices that are not selected do not interfere with SPI bus activities.

MCSPI offers the flexibility to modify the following parameters to adapt to the device features:

- Word length

  MCSPI supports any SPI word ranging from 4 bits to 32 bits long (the SPIm.MCSPI_CHxCONF[11:7] WL bit field).

  SPI word length can be changed between transmissions to allow the master device to communicate with peripheral slaves that have different requirements.
- SPI enable (mcspim_csx, for channel x of instance m)

  The polarity of the SPI enable signals is programmable (the SPIm.MCSPI_CHxCONF[6] EPOL bit). mcspim_csx signals can be active high or low.

  Assertion of the mcspim_csx signals is programmable and can be done manually or automatically. The manual assertion mode is available in single master mode only. mcspim_csx can be kept active between words with the SPIm.MCSPI_CHxCONF[20] FORCE bit.

  Two consecutive words for two different slave devices can go along with active mcspim_csx signals with different polarity.
- Programmable start-bit

  In start-bit mode a start-bit is added before the SPI word length to indicate how the next SPI word must be handled. The start-bit is enabled by setting the SPIm.MCSPI_CHxCONF[23] SBE bit to 1. The SPIm.MCSPI_CHxCONF[24] SBPOL bit defines the polarity of the start-bit.
- Programmable SPI clock
  - Bit rate

    In master mode, the baud rate of the SPI serial clock is programmable using the 48-MHz reference clock (from the PRCM module). Table 23-264 lists the spim_clk bit rates obtained for data transfer when programming the clock divider (the SPIm.MCSPI_CHxCONF[5:2] CLKD bit field).

Table 23-264. SPI Master Clock Rates

Divider	Clock Rate
1	48 MHz
2	24 MHz
4	12 MHz
8	6 MHz
16	3 MHz
32	1.5 MHz
64	750 kHz
128	375 kHz
256	~187 kHz
512	~93.7 kHz
1024	~46.8 kHz

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Table 23-264. SPI Master Clock Rates (continued)

Divider	Clock Rate
2048	~23.4 kHz
4096	~11.7 kHz

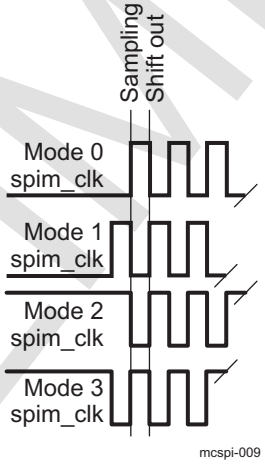
– Polarity and phase

The polarity (the SPIm.MCSPI_CHxCONF[1] POL bit) and the phase (the SPIm.MCSPI_CHxCONF[0] PHA bit) of the SPI serial clock (mcspim_clk) are configurable to offer four combinations. Software selects the right combination, depending on the device. See Table 23-265 and Figure 23-90.

Table 23-265. Phase and Polarity Combinations

Polarity (POL)	Phase (PHA)	SPI Mode	Comments
0	0	Mode 0	mcspim_clk is active high and sampling occurs on the rising edge.
0	1	Mode 1	mcspim_clk is active high and sampling occurs on the falling edge.
1	0	Mode 2	mcspim_clk is active low and sampling occurs on the falling edge.
1	1	Mode 3	mcspim_clk is active low and sampling occurs on the rising edge.

Figure 23-90. Phase and Polarity Combinations



23.4.2.1.3.1 Transfer Format

In master and slave modes, the MCSPI drives the data lines when spim_csx is asserted.

Each word is transmitted starting with the MSB.

This section explains the two cases of data transmission determined by the clock phase (PHA) and the type of data transmission using a start-bit (SBE) called the start-bit mode:

- Transmission in mode 0 and mode 2 (PHA = 0)

  When PHA = 0, the first bit of the SPI word to transmit (on the master or the slave data output pin) is valid one-half cycle of spim_clk after the assertion of spim_csx.

  Therefore, the first edge of the mcspim_clk line is used by the master to sample the first data bit sent by the slave. On the same edge, the first data bit sent by the master is sampled by the slave.

  On the next mcspim_clk edge, the received data bit is shifted into the receive shift register and a new data bit is transmitted on the serial data line.

  This process continues for a number of pulses on the spim_clk line defined by the SPI word length

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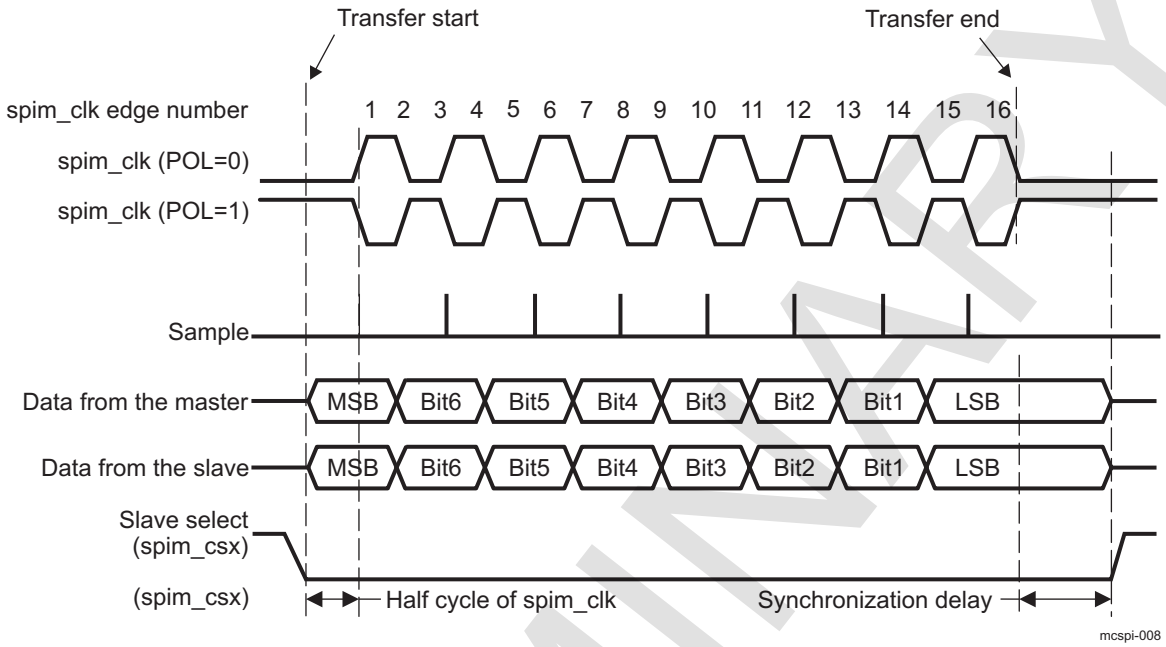
programmed in the master device, with data being latched on odd-numbered edges and shifted on even-numbered edges. See Figure 23-91.

Figure 23-91. Full-Duplex Transfer Format With PHA = 0



- Transmission in mode 1 and mode 3 (PHA = 1)

  When PHA = 1, the first bit of the SPI word to transmit (on the master or the slave data output pin) is valid on the following mcspim_clk edge (one-half cycle later). This is the sampling edge for the master and slave. A synchronization delay is added between the activation of mcspim_csx and the first mcspim_clk edge.

  The received data bit is shifted into the shift register on the third mcspim_clk edge.

  This process continues for a number of pulses on the mcspim_clk line defined by the SPI word length programmed in the master device, with data being latched on even-numbered edges and shifted on odd-numbered edges.

  NOTE: The minimum synchronization delay is one cycle of mcspim_clk, if the frequency of mcspim_clk equals the frequency of SPIm_FCLK (MCSPIm functional clock) in master mode. The minimum synchronization delay is one-half cycle of mcspim_clk, if the frequency of mcspim_clk is lower than the frequency of SPIm_FCLK in the master and slave modes.

- Transmission with a start-bit (SBE = 1)

  When the SPIm.MCSPI_CHxCONF[23] SBE bit is set to 1, a start-bit is added before the MSB to indicate whether the next SPI word must be handled as a command or as data.

  Figure 23-92 shows an example of a data transfer with an extra start-bit.

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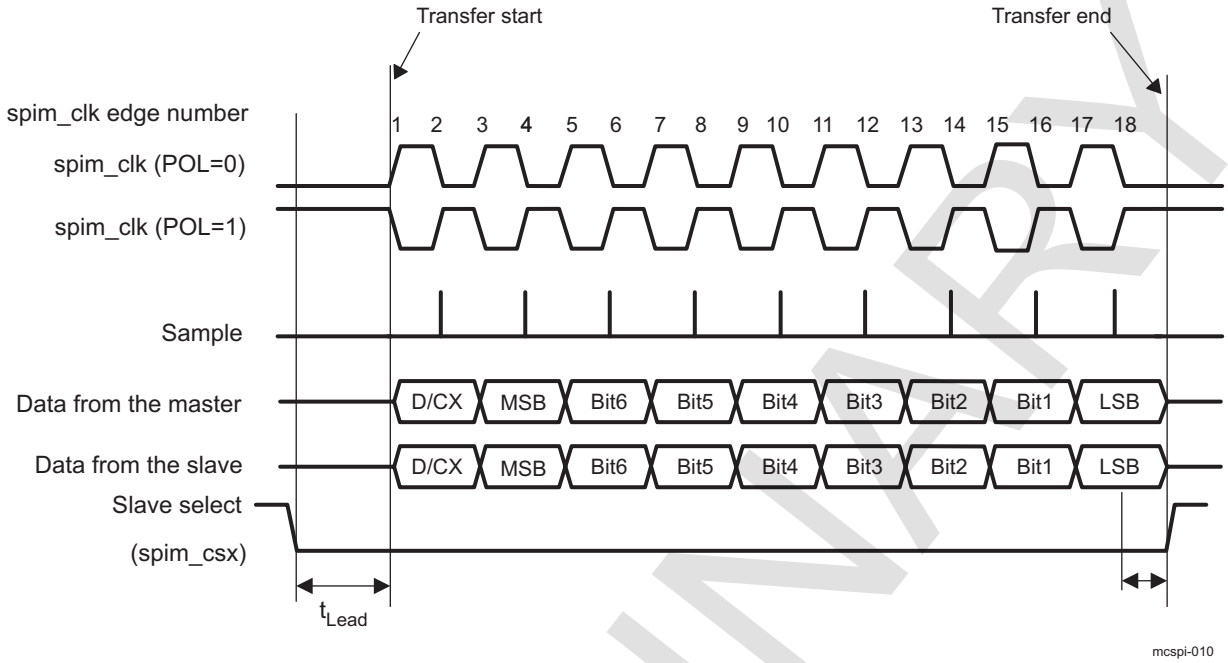
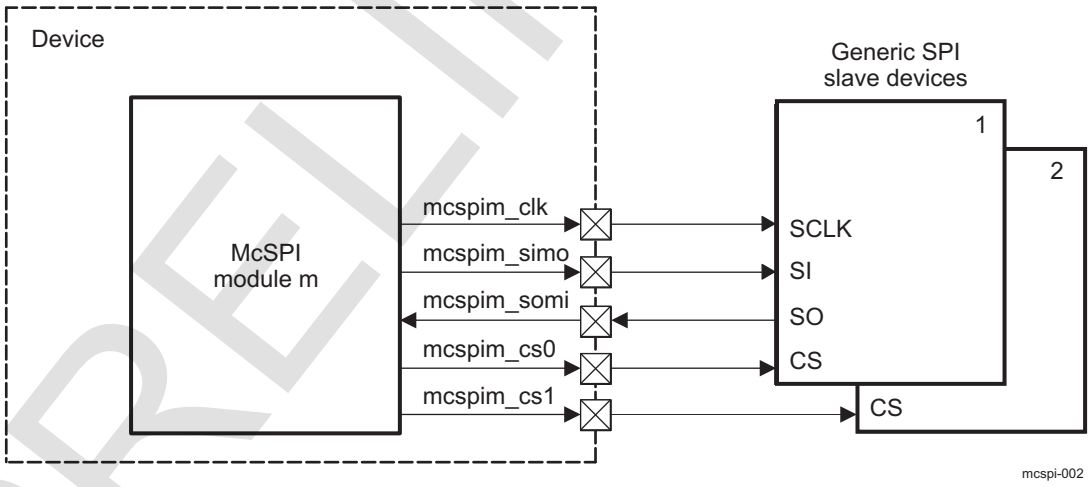
Figure 23-92. Extended SPI Transfer With a Start-Bit (SBE = 1)



23.4.2.2 SPI in Master Mode

Figure 23-93 shows a case in master mode (full-duplex) where the MCSPI module is connected with two slave devices.

Figure 23-93. MCSPI Master Mode (Full Duplex)



NOTE: In this case m = [1,3].

Figure 23-94 shows the master single mode, which can also be configured in receive-only mode.

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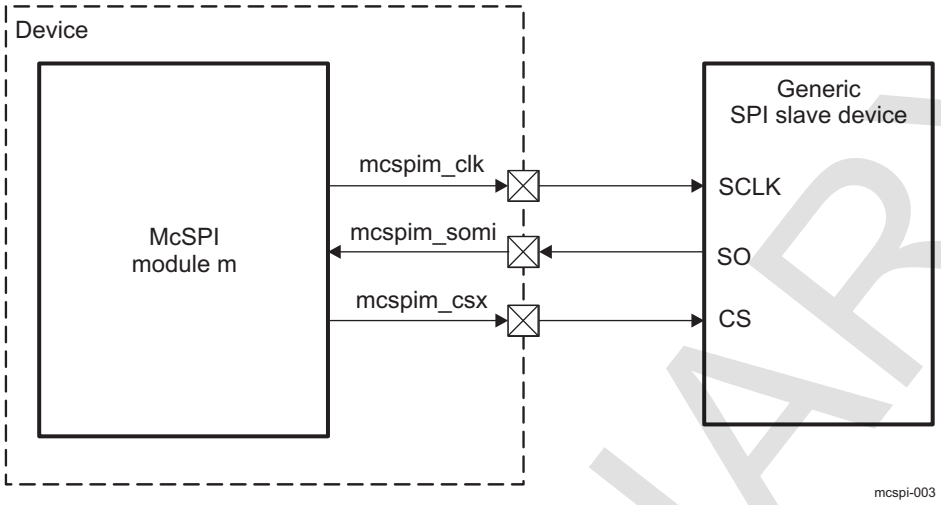
Figure 23-94. MCSPI Master Single Mode (Receive Only)



23.4.2.3 SPI in Slave Mode

Figure 23-95 shows a case in slave mode (full-duplex).

NOTE: Only channel 0 can be configured as slave, but the chip-enable signal can be connected to any mcspim_csx pin and then rerouted internally to channel 0 (the SPIm.MCSPI_CHxCONF[22:21] SPIENSLV bit field [where x = 0]). For more information, see Section 23.4.4.3, *Slave Mode*.

Figure 23-95. MCSPI Slave Mode (Full Duplex)

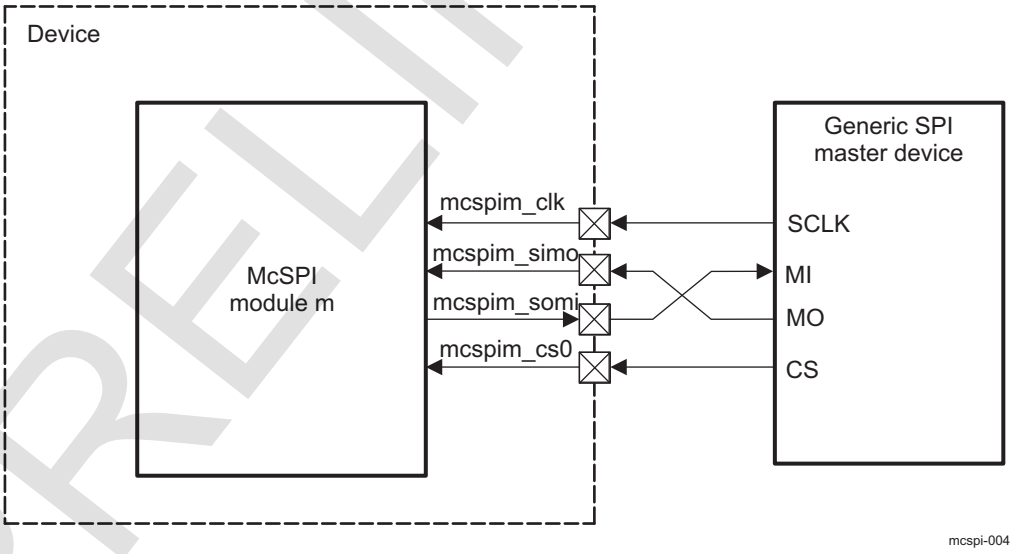


Figure 23-96 shows the slave single mode, which can also be configured in transmit-only mode.

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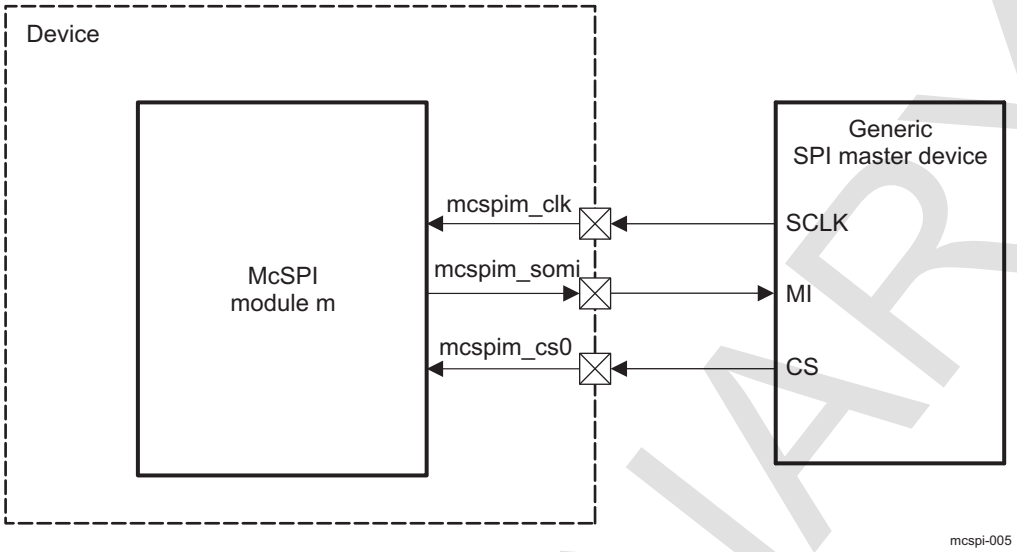
Figure 23-96. MCSPI Slave Single Mode (Transmit Only)

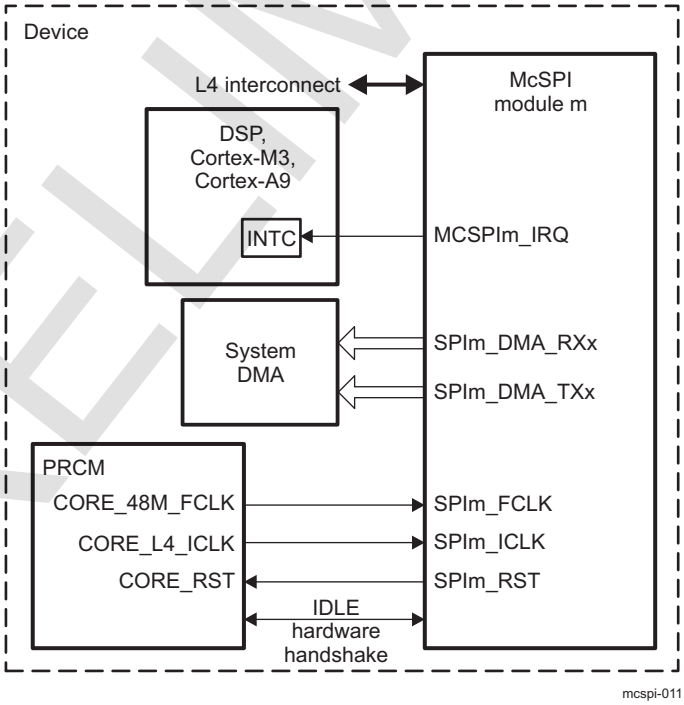


23.4.3 MCSPI Integration

This section describes module integration in the device, including information about clocks, resets, and hardware requests.

Figure 23-97 shows MCSPI integration.

Figure 23-97. MCSPI Integration



NOTE: For more information about the IDLE hardware handshake and the wake-up request, see Section 3.1.1.1.2, *Module-Level Clock Management*, in Chapter 3, *Power, Reset, and Clock Management*.

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NOTE: For the names of the signals going from the MCSPI and to the DSP, Cortex-M3, and Cortex-A9 INTC, see Table 23-268.

Table 23-266 through Table 23-268 summarize the integration of the module in the device.

Table 23-266. Integration Attributes

Module Instance	Attributes	
	Power Domain	Interconnect
MCSPI1	PD_L4_PER	L4_PER
MCSPI2	PD_L4_PER	L4_PER
MCSPI3	PD_L4_PER	L4_PER
MCSPI4	PD_L4_PER	L4_PER

Table 23-267. Clocks and Resets

Clocks				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
MCSPI1	SPI1_ICLK	PER_L4_ICLK	PRCM	Interface clock
	SPI1_FCLK	PER_48M_FCLK	PRCM	Functional clock
MCSPI2	SPI2_ICLK	PER_L4_ICLK	PRCM	Interface clock
	SPI2_FCLK	PER_48M_FCLK	PRCM	Functional clock
MCSPI3	SPI3_ICLK	PER_L4_ICLK	PRCM	Interface clock
	SPI3_FCLK	PER_48M_FCLK	PRCM	Functional clock
MCSPI4	SPI4_ICLK	PER_L4_ICLK	PRCM	Interface clock
	SPI4_FCLK	PER_48M_FCLK	PRCM	Functional clock
Resets				
MCSPI1	SPI1_RST	L4_PER_RST	PRCM	Reset from the PRCM module
MCSPI2	SPI2_RST	L4_PER_RST	PRCM	Reset from the PRCM module
MCSPI3	SPI3_RST	L4_PER_RST	PRCM	Reset from the PRCM module
MCSPI4	SPI4_RST	L4_PER_RST	PRCM	Reset from the PRCM module

Table 23-268. Hardware Requests

Interrupt Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
MCSPI1	SPI1_IRQ	D_IRQ_87	DSP INTC	Interrupt request to the DSP INTC
	SPI1_IRQ	MA_IRQ_65	Cortex-A9 INTC	Interrupt request to the Cortex-A9 INTC
	SPI1_IRQ	MM_IRQ_41	Cortex-M3 INTC	Interrupt request to the Cortex-M3 INTC
MCSPI2	SPI2_IRQ	MA_IRQ_66	Cortex-A9 INTC	Interrupt request to the Cortex-A9 INTC
	SPI2_IRQ	MM_IRQ_42	Cortex-M3 INTC	Interrupt request to the Cortex-M3 INTC
MCSPI3	SPI3_IRQ	MA_IRQ_91	Cortex-A9 INTC	Interrupt request to the Cortex-A9 INTC
MCSPI4	SPI4_IRQ	MA_IRQ_48	Cortex-A9 INTC	Interrupt request to the Cortex-A9 INTC
DMA Requests				
MCSPI1	SPI1_DMA_TX0	S_DMA_34	sDMA	Destination is system DMA.
	SPI1_DMA_RX0	S_DMA_35	sDMA	Destination is system DMA.
	SPI1_DMA_TX1	S_DMA_36	sDMA	Destination is system DMA.

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Table 23-268. Hardware Requests (continued)

	SPI1_DMA_RX1	S_DMA_37	sDMA	Destination is system DMA.
	SPI1_DMA_TX2	S_DMA_38	sDMA	Destination is system DMA.
	SPI1_DMA_RX2	S_DMA_39	sDMA	Destination is system DMA.
	SPI1_DMA_TX3	S_DMA_40	sDMA	Destination is system DMA.
	SPI1_DMA_RX3	S_DMA_41	sDMA	Destination is system DMA.
MCSPI2	SPI2_DMA_TX0	S_DMA_42	sDMA	Destination is system DMA.
	SPI2_DMA_RX0	S_DMA_43	sDMA	Destination is system DMA.
	SPI2_DMA_TX1	S_DMA_44	sDMA	Destination is system DMA.
	SPI2_DMA_RX1	S_DMA_45	sDMA	Destination is system DMA.
MCSPI3	SPI3_DMA_TX0	S_DMA_14	sDMA	Destination is system DMA.
	SPI3_DMA_RX0	S_DMA_15	sDMA	Destination is system DMA.
	SPI3_DMA_TX1	S_DMA_22	sDMA	Destination is system DMA.
	SPI3_DMA_RX1	S_DMA_23	sDMA	Destination is system DMA.
MCSPI4	SPI4_DMA_TX0	S_DMA_69	sDMA	Destination is system DMA.
	SPI4_DMA_RX0	S_DMA_70	sDMA	Destination is system DMA.

Table 23-269 lists the wake-up requests.

Table 23-269. Wake-Up Requests

Attributes	Wake Request	Name	Mapping	Comments
SPI1	1	spi1_cs0	SPI1_ SWAKEUP	Destination is the PRCM module.
SPI2	1	spi2_cs0	SPI2_ SWAKEUP	Destination is the PRCM module.
SPI3	1	spi3_cs0	SPI3_ SWAKEUP	Destination is the PRCM module.
SPI4	1	spi4_cs0	SPI4_ SWAKEUP	Destination is the PRCM module.

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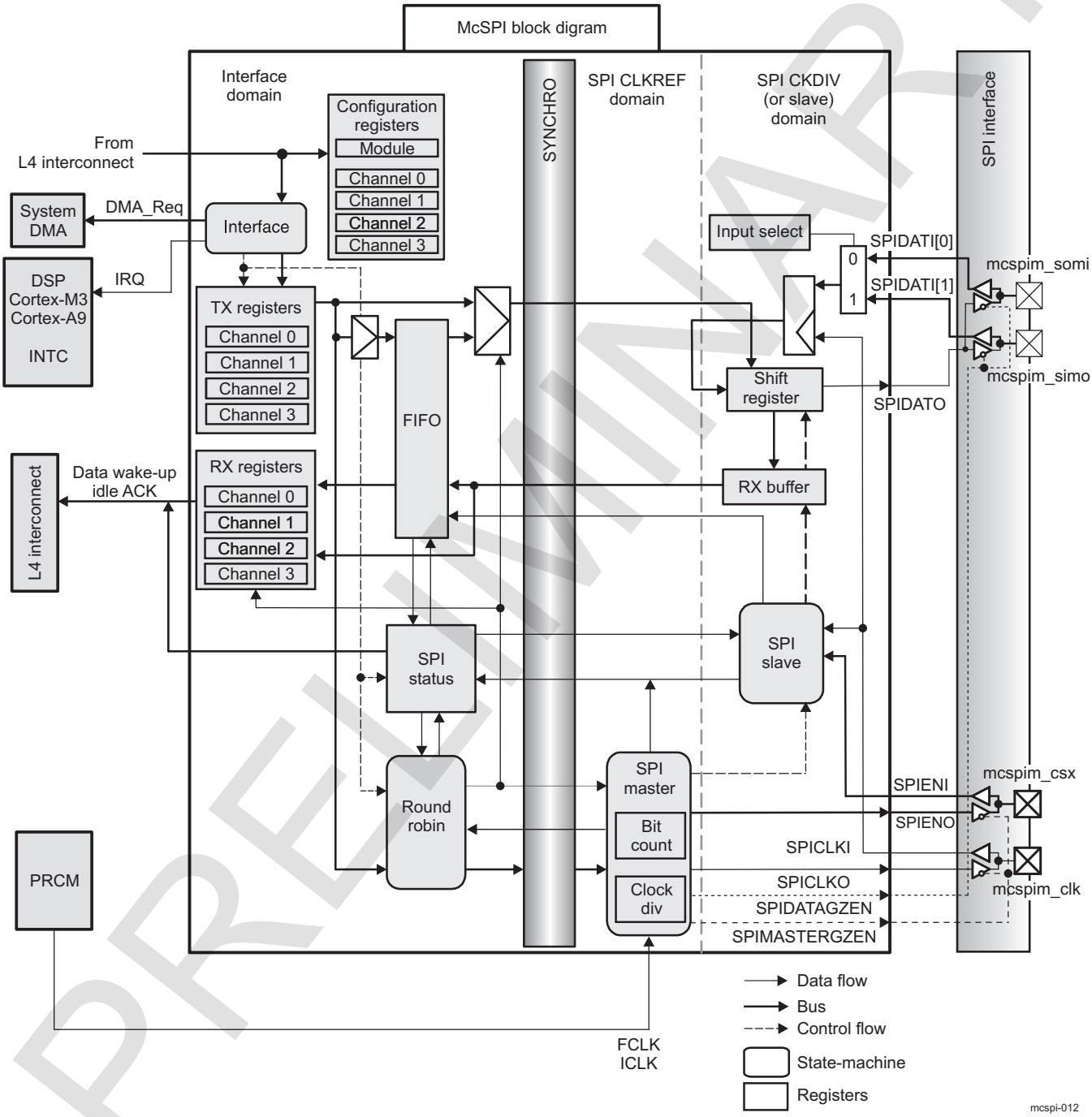
23.4.4 MCSPI Functional Description

23.4.4.1 MCSPI Block Diagram

Figure 23-98 shows the MCSPI module.

Figure 23-98. MCSPI Block Diagram



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23.4.4.2 Master Mode

23.4.4.2.1 Master Mode Features

The MCSPI master mode supports multichannel communication with up to four independent SPI communication channel contexts. The MCSPI initiates a data transfer on the data lines (mcspim_simo and mcspim_somi) and generates clock (mcspim_clk) and control (mcspim_csx) signals.

Connected to multiple external devices, the MCSPI exchanges data with one SPI device at a time through two main modes (available in slave mode):

- Two-data-pins interface mode (transmit-and-receive mode for full-duplex transmission)
- Single-data-pin interface mode (recommended for half-duplex transmission)

Two DMA request events (read and write) allow synchronized accesses of the DMA controller with the activity of MCSPI.

Three interrupt events can be used for data transmission and reception in master mode (for more information about interrupts, see Section 23.4.4.5.1, *Interrupt Events in Master Mode*).

23.4.4.2.2 Master Transmit-and-Receive Mode (Full Duplex)

In full-duplex transmission, data is transmitted (shifted out serially on mcspim_simo) and received (shifted in serially on mcspim_somi) simultaneously on separate data lines.

The master transmit-and-receive mode is programmable per channel (the SPIm.MCSPI_CHxCONF[13:12] TRM bit field).

Channel access to the shift registers for transmission/reception is based on the MCSPI_TXx transmitter register state, the MCSPI_RXx receiver register state, and round-robin arbitration.

Channels that meet the following rules are included in the round-robin list of active channels scheduled for transmission and/or reception. The arbiter skips channels that do not meet the rules and searches in the rotation for the next enabled channel.

- Rule 1: Only enabled channels (the SPIm.MCSPI_CHxCTRL[0] EN bit) can be scheduled for transmission and/or reception.
- Rule 2: If its MCSPI_TXx transmitter register is not empty (the SPIm.MCSPI_CHxSTAT[1] TXS bit), an enabled channel can be scheduled when the shift register is assigned. If the MCSPI_TXx register is empty when the shift register is assigned, the TXx_UNDERFLOW event is activated, and the next enabled channel with new data to transmit is scheduled (see also transmit-only mode).
- Rule 3: An enabled channel can be scheduled if its receive register is not full (the SPIm.MCSPI_CHxSTAT[0] RXS bit) when the shift register is assigned (see also receive-only mode). Therefore, the MCSPI_RXx register cannot be overwritten. The SPI1.MCSPI_IRQSTATUS[3] RX0_OVERFLOW bit is never set to this mode.

When SPI word transfer completes (the SPIm.MCSPI_CHxSTAT[2] EOT bit is set), the updated MCSPI_TXx register of the next scheduled channel is loaded into the shift register. The serialization (transmit-and-receive) starts depending on the channel communication configuration. When serialization completes, the received data transfers to the channel receive register.

The serial clock (mcspim_clk) synchronizes shifting and sampling of the information on the two serial data lines (mcspim_simo and mcspim_somi). Each time a bit transfers out from the master, 1 bit transfers in from the slave.

Figure 23-99 shows an example of a full-duplex system with a master device (MCSPI module *m*) on the left and a slave device on the right. After eight cycles of the serial clock mcspim_clk, WordA transfers from the master to the slave. At the same time, WordB transfers from the slave to the master.

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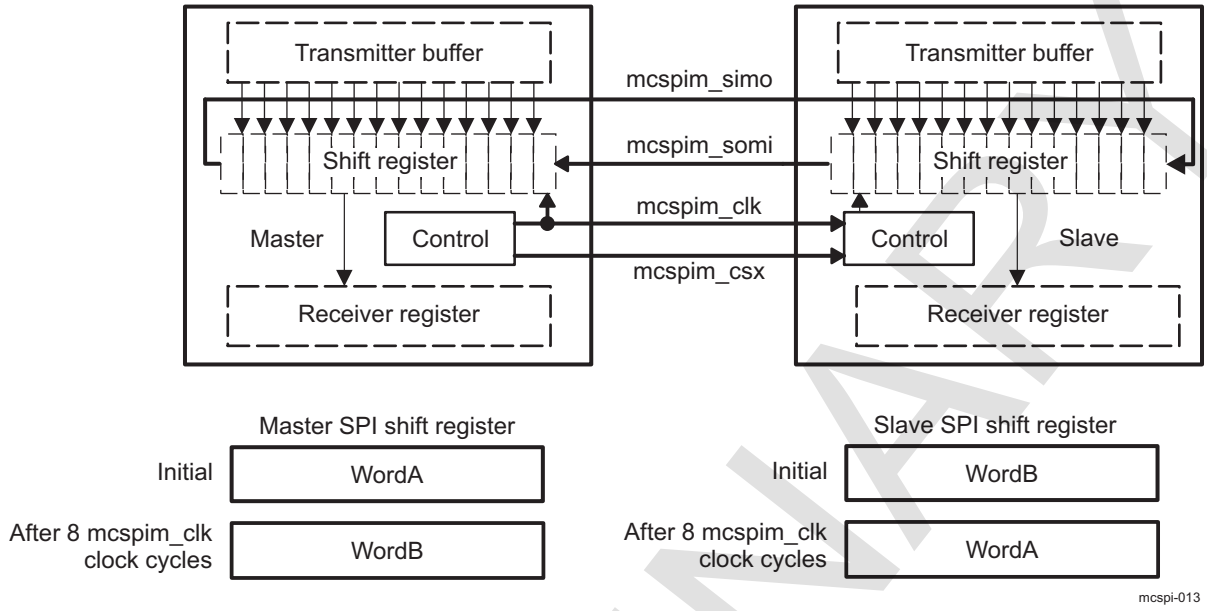
Figure 23-99. SPI Full-Duplex Transmission (Example)



23.4.4.2.3 Master Transmit-Only Mode (Half Duplex)

The master transmit-only mode prevents the MPU from reading the MCSPI_RXx register (minimizing data movement) when only transmission is meaningful.

The master transmit-only mode is programmable per channel (the SPIm.MCSPI_CHxCONF[13:12] TRM field). Transmission starts only after data is loaded into the MCSPI_TXx register.

Rule 1 and Rule 2, defined in Section 23.4.4.2.2, apply in this mode.

Rule 3, defined in Section 23.4.4.2.2, does not apply.

In master transmit-only mode, the MCSPI_RXx register state FULL does not prevent transmission and the MCSPI_RXx register is always overwritten with the new SPI word. This event is not significant when only transmission is meaningful. Thus, the RX0_OVERFLOW bit in the SPIm.MCSPI_IRQSTATUS register is never set in this mode.

The hardware automatically disables the RX_FULL interrupt and the DMA read requests.

The transfer status is given by the SPIm.MCSPI_CHxSTAT[2] EOT bit.

23.4.4.2.4 Master Receive-Only Mode (Half Duplex)

The master receive mode prevents the MPU from refilling the MCSPI_TXx register (minimizing data movement) when only reception is meaningful.

The master receive mode is programmable per channel (the SPIm.MCSPI_CHxCONF[13:12] TRM bit field).

The master receive-only mode enables channel scheduling only on the empty state of the MCSPI_RXx register.

Rule 1 and Rule 3, defined in Section 23.4.4.2.2, apply in this mode.

Rule 2, defined in Section 23.4.4.2.2, does not apply.

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In the master receive-only mode, software must write dummy data to the MCSPI_TXx register. Only one dummy write is enough to receive any number of words from the slave. Software should ensure that the MCSPI_TXx register is always full (the TXx_EMPTY bits of SPIm.MCSPI_IRQSTATUS) when receiving. The content of the MCSPI_TXx register is always loaded into the shift register when the shift register is assigned. After writing the dummy data to the MCSPI_TXx register, the TXx_EMPTY and TXx_UNDERFLOW bits in the SPIm.MCSPI_IRQSTATUS register are never set in receive-only mode.

The SPIm.MCSPI_CHxSTAT[2] EOT bit gives the status of serialization. The RXx_FULL bits of the SPIm.MCSPI_IRQSTATUS register are set when received data is loaded from the shift register to the corresponding MCSPI_RXx register. The SPIm.MCSPI_IRQSTATUS[3] RX0_OVERFLOW bit is never set in this mode.

23.4.4.2.5 Single-Channel Master Mode

When the MCSPI is configured as a master device with a single enabled channel, the assertion of the mcspim_csx signal can be controlled in two different ways:

- If the MCSPI_MODULCTRL[0] SINGLE bit is set to 0, mcspim_csx assertion and deassertion after each SPI word is automatically controlled by the MCSPI (see subsections of Section 23.4.4.2.1, *Master Mode Features*).
- If the MCSPI_MODULCTRL[0] SINGLE and MCSPI_CHxCONF[20] FORCE bits are set to ,: mcspim_csx assertion and deassertion is controlled by software (see Section 23.4.4.2.5.1, *Programming Tips When Switching to Another Channel*).

23.4.4.2.5.1 Programming Tips When Switching to Another Channel

When a single channel is enabled and data transfer is ongoing:

- Wait for completion of the SPI word transfer (wait until the SPIm.MCSPI_CHxSTAT[2] EOT bit is set to 1) before disabling the current channel and enabling a different channel.
- Disable the current channel, and then enable the other channel.

23.4.4.2.5.2 Force mcspim_csx Mode

Continuous transfers are allowed manually by keeping the mcspim_csx signal active for successive SPI words transfer. Several sequences (configuration/enable/disable of the channel) can be run without deactivating the mcspim_csx line. This mode is supported by all channels and any master sequence can be used (transmit-receive, transmit-only, receive-only).

Keeping the mcspim_csx active mode is supported when:

- A single channel is used (with the SPIm.MCSPI_MODULCTRL[0] SINGLE bit set to 1).
- Transfer parameters are loaded in the configuration register of the appropriate channel (SPIm.MCSPI_CHxCONF).

  The state of the mcspim_csx signal is programmable.

  – Writing 1 to the SPIm.MCSPI_CHxCONF[20] FORCE bit drives the mcspim_csx line high when the SPIm.MCSPI_CHxCONF[6] EPOL bit is set to 0. mcspim_csx is driven low when the SPIm.MCSPI_CHxCONF[6] EPOL bit is set to 1.

  – Writing 0 to the SPIm.MCSPI_CHxCONF[20] FORCE bit drives the mcspim_csx line low when the SPIm.MCSPI_CHxCONF[6] EPOL bit is set to 0. mcspim_csx is driven high when the SPIm.MCSPI_CHxCONF[6] EPOL bit is set to 1.
- A single channel is enabled (the SPIm.MCSPI_CHxCTRL[0] EN bit is set to 1). The first enabled channel activates the mcspim_csx line.

When the channel is enabled, the mcspim_csx signal activates with the programmed polarity. As in the multichannel master mode, the transfer start depends on the status of the MCSPI_TXx register (the SPIm.MCSPI_CHxSTAT[1] TXS bit), the status of the MCSPI_RXx register (the SPIm.MCSPI_CHxSTAT[1] RXS bit), and the defined mode (the SPIm.MCSPI_CHxCONF[13:12] TRM bit field) of the channel enabled.

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The SPIm.MCSPI_CHxSTAT[2] EOT bit gives the transfer status of each SPI word. The RXx_FULL bit in the SPIm.MCSPI_IRQSTATUS register is set when received data is loaded from the shift register to the MCSPI_RXx register.

A change in the configuration parameters is propagated directly on the SPI interface. If the mcspim_csx signal is activated, ensure that the configuration is changed only between SPI words to avoid corrupting the current transfer.

NOTE: To avoid data corruption, mcspim_csx polarity and mcspim_clk phase and mcspim_clk polarity must not be modified when the mcspim_csx signal is activated.

A delay between SPI words that requires the connected SPI slave device to switch from one configuration to another (for instance, from transmit-only to receive-only) must be handled by software.

At the end of the last SPI word, the channel must be deactivated (the SPIm.MCSPI_CHxCTRL[0] EN bit set to 0) and mcspim_csx can be forced to its INACTIVE state using the SPIm.MCSPI_CHxCONF[20] FORCE bit.

Figure 23-100 and Figure 23-101 show successive transfers with mcspim_csx maintained active low with a different configuration for each SPI word in single-data-pin and dual-data-pin interface modes, respectively.

Figure 23-100. Continuous Transfers With mcspim_csx Maintained Active (Single-Data-Pin Interface Mode)

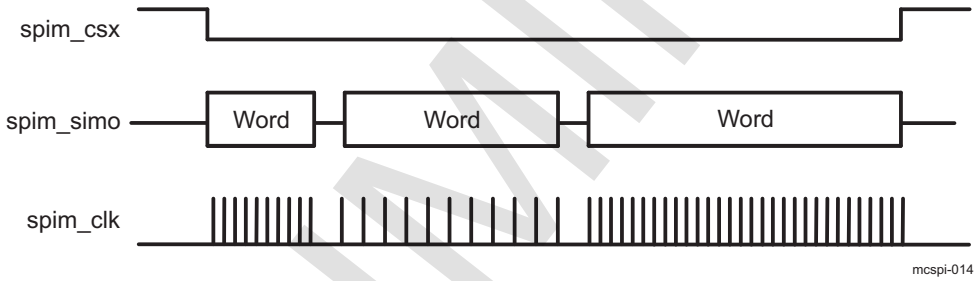
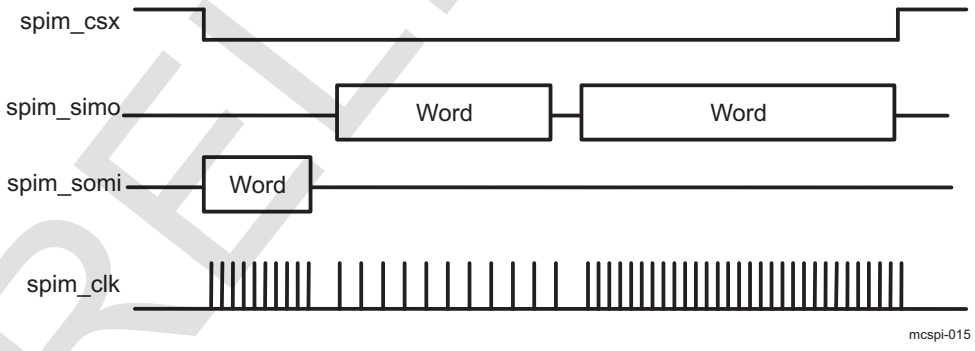


Figure 23-101. Continuous Transfers With mcspim_csx Maintained Active (Dual-Data-Pin Interface Mode)



NOTE: Turbo mode described in Section 23.4.4.2.5.3, *Turbo Mode*, maintains mcspim_csx in active mode when the following conditions are met:

- A single channel is explicitly used (the SPIm.MCSPI_MODULCTRL[0] SINGLE bit is set to 1).
- Turbo mode is enabled in the configuration of the channel (the SPIm.MCSPI_CHxCONF[19] TURBO bit is set to 1).

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23.4.4.2.5.3 Turbo Mode

Turbo mode improves the throughput of the SPI interface when a single channel is enabled by allowing transfers until the shift register and the MCSPI_RXx register are full. Turbo mode is time saving when a transfer exceeds two words. This mode is programmable per channel (through the SPI1.MCSPI_CHxCONF[9] TURBO bit).

When several channels are enabled, the TURBO bit has no effect and the channel access to the shift registers remains as previously described.

In turbo mode, Rule 1 and Rule 2 apply, but Rule 3 does not (see Section 23.4.4.2.2). An enabled channel can be scheduled if its receive register is full (the SPIm.MCSPI_CHxSTAT[0] RXS bit) at the time of the shift-register assignment until the shift register is full.

The MCSPI_RXx register cannot be overwritten in turbo mode. Consequently, the SPIm.MCSPI_IRQSTATUS[3] RX0_OVERFLOW bit is never set in this mode.

23.4.4.2.6 Start-Bit Mode

In start-bit mode, an extended bit is added before the SPI word to indicate whether the next SPI word must be handled as a command or as data. This feature is available only in master mode. Start-bit mode cannot be used at the same time as turbo mode and/or force mcspim_csx mode. In this case, only one channel can be used; round-robin arbitration is not possible.

This mode is programmable per channel by setting the SPIm.MCSPI_CHxCONF[23] SBE bit to 1. The polarity of the extended bit is programmable per channel. When the SPIm.MCSPI_CHxCONF[24] SBPOL bit is set to 0, the SPI word must be handled as a command. When the SPIm.MCSPI_CHxCONF[24] SBPOL bit is set to 1, the SPI word must be handled as data. Moreover, start-bit polarity can be changed dynamically during start-bit transfer without disabling the channel for reconfiguration; in this case, users must configure the SPIm.MCSPI_CHxCONF[24] SBPOL bit before writing the SPI word to be transmitted to the TX register.

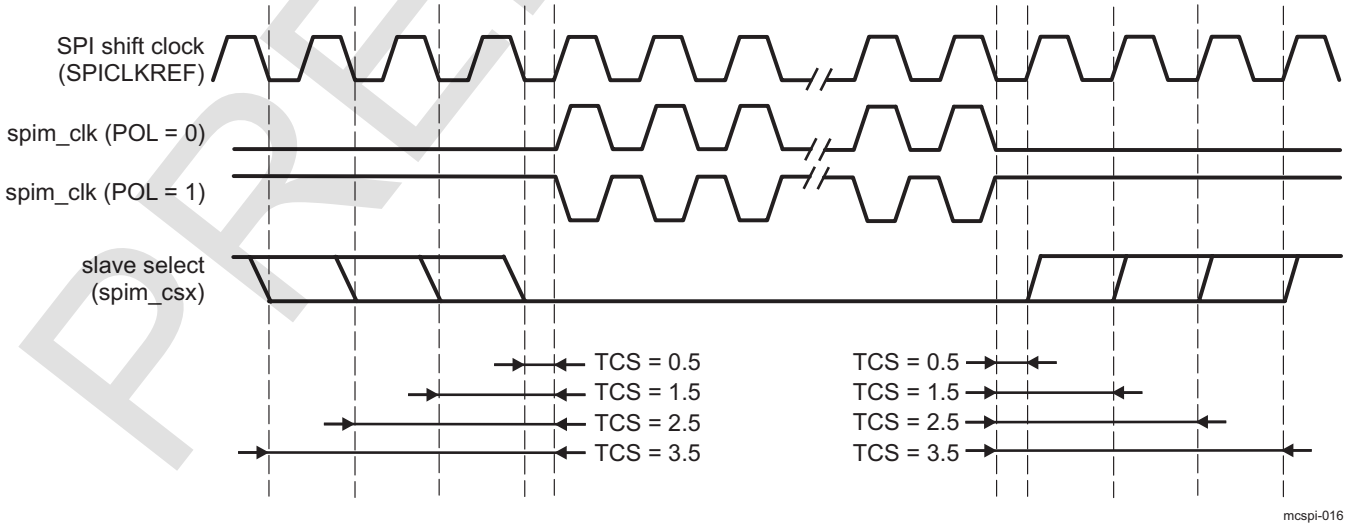
23.4.4.2.7 Chip-Select Timing Control

The chip-select (CS) timing control is available only in master mode with automatic CS generation (the MCSPI_MODULCTRL[0] SINGLE bit field set to 0) to add a programmable delay between CS assertion and first clock edge, or CS removal and last clock edge.

This mode is programmable per channel (the SPIm.MCSPI_CHxCONF TCS bit).

Figure 23-102 shows the CS SPIEN timing control.

Figure 23-102. CS SPIEN Timing Controls



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NOTE: Because of the design implementation for transfers using a clock divider ratio set to 1 (clock bypassed), a half cycle must be added to the value between CS assertion and the first clock edge with PHA = 1 or between CS removal and the last clock edge with PHA = 0.

23.4.4.2.8 Programmable SPI Clock (mcspim_clk)

In master mode, the baud rate of the SPI serial clock is programmable.

An internal reference clock, SPIm_FCLK, is used as input of a programmable divider (the SPIm.MCSPI_CHxCONF[5:2] CLKD bit field) to generate the bit rate of the serial output clock mcspim_clk. Table 23-270 summarizes the supported divisor values.

Table 23-270. SPI Master Clock Rates

Divider	Clock Rate
1	48 MHz
2	24 MHz
4	12 MHz
8	6 MHz
16	3 MHz
32	1.5 MHz
64	750 kHz
128	375 kHz
256	~187 kHz
512	~93.7 kHz
1024	~46.8 kHz
2048	~23.4 kHz
4096	~11.7 kHz
8192 and higher: Division not supported	–

23.4.4.2.8.1 Clock Ratio Granularity

By default, the clock division ratio is defined by the SPIm.MCSPI_CHxCONF[5:2] CLKD bit field with power-of-2 granularity leading to a clock division in the range 1 to 4096; in this case, the duty cycle is always 50 percent. With the SPIm.MCSPI_CHxCONF[29] CLKG bit, clock division granularity can be changed to one clock cycle; in that case the SPIm.MCSPI_CHxCTRL[15:8] EXTCLK bit field is concatenated with the SPIm.MCSPI_CHxCONF[5:2] CLKD bit field to give a 12-bit-wide division ratio in the range 1 to 4096.

When granularity is one clock cycle (the CLKG bit set to 1), for the odd value of the clock ratio, the clock high level lasts one clock cycle more than the low level, depending on th SPIm.MCSPI_CHxCONF[1] POL and SPIm.MCSPI_CHxCONF[0] PHA bits (see Table 23-271).

Table 23-271. CLKSPIO High/Low Time Computation

Clock Ratio Fratio	CLKSPIO High Time	CLKSPIO Low Time
1	Thigh_ref	Tlow_ref
Even >= 2	T_ref * (Fratio/2)	T_ref * (Fratio/2)
Odd >= (POL = PHA)	T_ref * (Fratio – 1)/2	T_ref * (Fratio + 1)/2
Odd >= (POL =! PHA)	T_ref * (Fratio + 1)/2	T_ref * (Fratio – 1)/2

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NOTE: Fratio = spi1_clk frequency (Fout) division ratio
Thigh = spi1_clk high time period
Tlow = spi1_clk low time period
T_ref = SPI1_FCLK period
Thigh_ref = SPI1_FCLK high time period
Tlow_ref = SPI1_FCLK low time period

If the CLKG bit is set to 1; Fratio = EXTCLK concatenated with CLKD + 1.

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For odd ratio values, the duty cycle is calculated as follows:

Duty_cycle = (1 – 1/Fratio)/2

Table 23-272 shows examples of clock granularity with a clock source frequency of 48 MHz.

Table 23-272. Clock Granularity Examples

EXTCLK	CLKD	CLKG	Fratio	PHA	POL	Thigh (ns)	Tlow (ns)	Tperiod (ns)	Duty Cycle	Fout (MHz)
X	0	0	1	X	X	10.4	10.4	20.8	50–50	48
X	1	0	2	X	X	20.8	20.8	41.6	50–50	24
X	2	0	4	X	X	41.6	41.6	83.2	50–50	12
X	3	0	8	X	X	83.2	83.2	166.4	50–50	6
0	0	1	1	X	X	10.4	10.4	20.8	50–50	48
0	1	1	2	X	X	20.8	20.8	41.6	50–50	24
0	2	1	3	1	0	41.6	20.8	62.4	66–33	16
0	2	1	3	1	1	20.8	41.6	62.4	33–66	16
0	3	1	4	X	X	41.6	41.6	83.2	50–50	12
5	0	1	81	1	0	852.8	832	1684.8	50.6–49.4	0.592
5	7	1	88	X	X	915.2	915.2	1830.4	50–50	0.545

23.4.4.3 Slave Mode

To select the MCSPI slave mode, set the SPIm.MCSPI_MODULCTRL[2] MS bit.

A MCSPI slave device can be connected to up to four external SPI master devices but handles transactions with one SPI master device at a time.

In slave mode, the MCSPI initiates data transfer on the data lines (mcspim_simo and mcspim_somi) when it is selected by an active control signal (mcspim_csx) and receives an SPI clock (mcspim_clk) from the external SPI master device. Only channel 0 can be configured as a slave. In slave mode, the MCSPI uses the edge of mcspim_csx to detect word length. For this reason, mcspim_csx must become inactive between each word.

The MCSPI does not support mcspim_csx active between SPI words. It uses the edge to detect word length.

23.4.4.3.1 Dedicated Resources

Only channel 0 can be enabled in slave mode. In this section register names such as SPI1.MCSPI_CHxCTRL stand for SPI1.MCSPI_CH0CTRL, where x = 0 (channel 0 control register).

Figure 23-103 shows an example of four slaves wired on a single master device.

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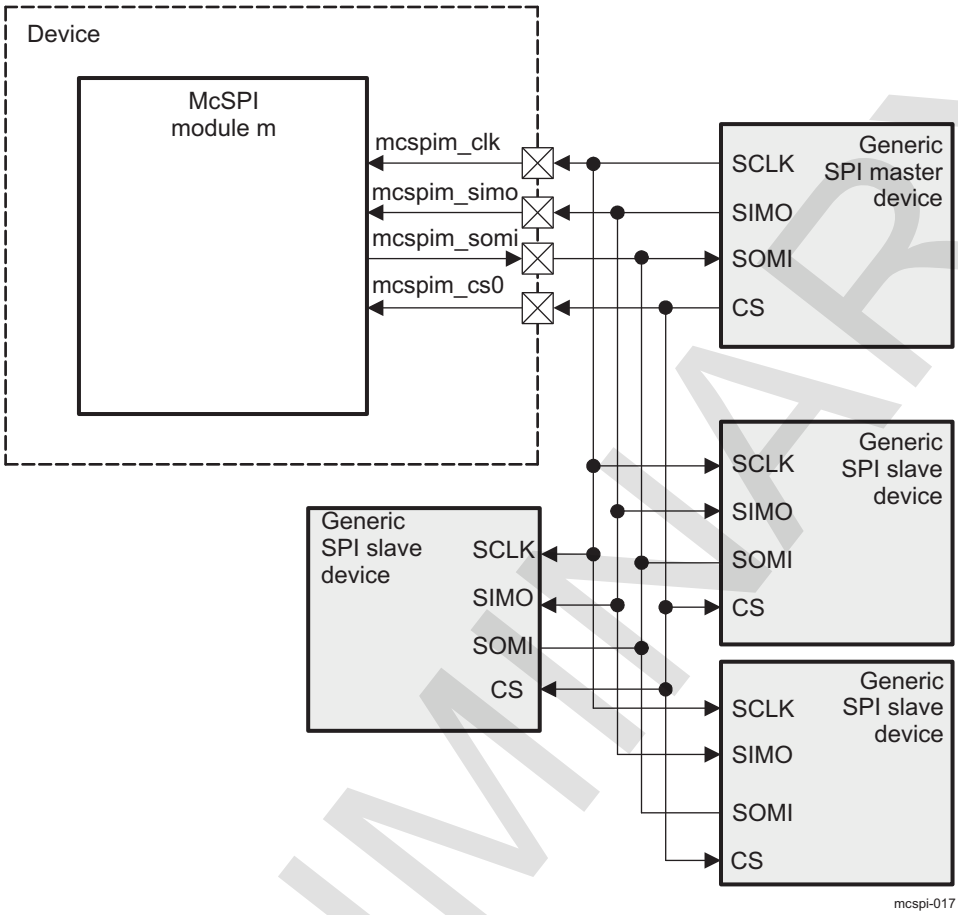
Figure 23-103. Example of MCSPI Slave With One Master and Multiple Slave Devices on Channel 0



The channel 0 in slave mode has the following resources:

- Its own channel enable, programmable with the SPIm.MCSPI_CHxCTRL[0] EN bit (where x = 0). This channel must be enabled before transmission and reception.
- For this mode, the slave-select signal can be detected on any one of the mcspim_csx ports. This is programmable with the SPIm.MCSPI_CHxCONF[22:21] SPIENSLV bit field (where x = 0).
- Its own transmitter register, SPIm.MCSPI_TXx (where x = 0), on top of the common transmit shift register. If the MCSPI_TXx register is empty, the SPIm.MCSPI_CHxSTAT[1] TXS bit (where x = 0) is set. If MCSPI is selected by an external master (the active signal on the mcspim_csx port assigned to channel 0), the MCSPI_TXx register content of channel 0 is always loaded into the shift register, whether its content is updated or not. The MCSPI_TXx register must be loaded before MCSPI is selected by a master.
- Its own receiver register, SPIm.MCSPI_RXx (where x = 0), on top of the common receive shift register. If the MCSPI_RXx register is full, the SPIm.MCSPI_CHxSTAT[0] RXS bit (where x = 0) is set.

NOTE: The MCSPI_TXx register and MCSPI_RXx registers of the other channels are not used. Reading from or writing to a channel register other than channel 0 has no effect.

- Its own communication configuration with the following parameters through the SPIm. MCSPI_CHxCONF register (where x = 0):
  - Transmit and receive modes, programmable with the TRM field
  - Interface mode (two data pins or single data pin) and data pins assignment, both programmable with the IS and DPE bits. (The SPIm modules are in slave mode after reset and must be properly configured for the modules to act in master mode.)

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– SPI word length, programmable with the WL bit
– mcspim_csx polarity, programmable with the EPOL bit
– mcspim_clk polarity, programmable with the POL bit
– mcspim_clk phase, programmable with the PHA bit

The mcspim_clk frequency of a transfer is controlled by the external SPI master connected to the MCSPI slave device. The SPIm.MCSPI_CHxCONF[5:2] CLKD bit field (where x = 0) is not used in slave mode.

NOTE: The configuration of the channel can be loaded in the SPIm.MCSPI_CHxCONF register (where x = 0) only when the channel is disabled.

- Two DMA request events, read and write, synchronize read/write accesses of the DMA controller with the activity of MCSPI. DMA requests are asserted using the SPIm.MCSPI_CHxCONF[15] DMAR bit (where x = 0) for reading and the SPIm.MCSPI_CHxCONF[14] DMAW bit (where x = 0) for writing.
- Four interrupt events (see Section 23.4.4.5.2, *Interrupt Events in Slave Mode*)

23.4.4.3.2 Slave Transmit-and-Receive Mode

The slave receive mode is programmable (set the SPIm.MCSPI_CHxCONF[13:12] TRM bit field [where x = 0] to 0x0).

In slave transmit-and-receive mode, the MCSPI_TXx register must be loaded before MCSPI is selected by an external SPI master device.

After a channel is enabled, transmission and reception proceed with interrupt and DMA request events.

The MCSPI_TXx register content is always loaded in the shift register whether it is updated or not. The event TXx_UNDERFLOW is activated accordingly and does not prevent transmission.

When an SPI word transfer completes (the SPIm.MCSPI_CHxSTAT0[2] EOT bit [where x = 0] set to 1), the received data is transferred to the channel receive register.

To use MCSPI as a slave transmit-only device, the RXx_FULL and RX0_OVERFLOW interrupts and DMA read requests must be disabled due to the MCSPI_RXx register state (see Section 23.4.4.5.2, *Interrupt Events in Slave Mode*).

23.4.4.3.3 Slave Transmit-Only Mode

The slave transmit-only mode is programmable (set the SPIm.MCSPI_CHxCONF[13:12] TRM bit field [where x = 0] to 0x2) and avoids the requirement for the MPU to read the MCSPI_RXx register (minimizing data movement) only when transmission is meaningful.

To use the MCSPI as a slave transmit-only device, the RXx_FULL and RX0_OVERFLOW interrupts and DMA read requests must be disabled due to the MCSPI_RXx register state.

When the SPI word transfer completes, the SPIm.MCSPI_CHxSTAT[2] EOT bit is set (where x = 0).

Figure 23-104 shows a half-duplex system with a master device on the left and a transmit-only slave device on the right. Each time a bit transfers out from the slave device, 1 bit transfers in the master. After eight cycles of the serial clock mcspim_clk, WordB transfers from the slave to the master.

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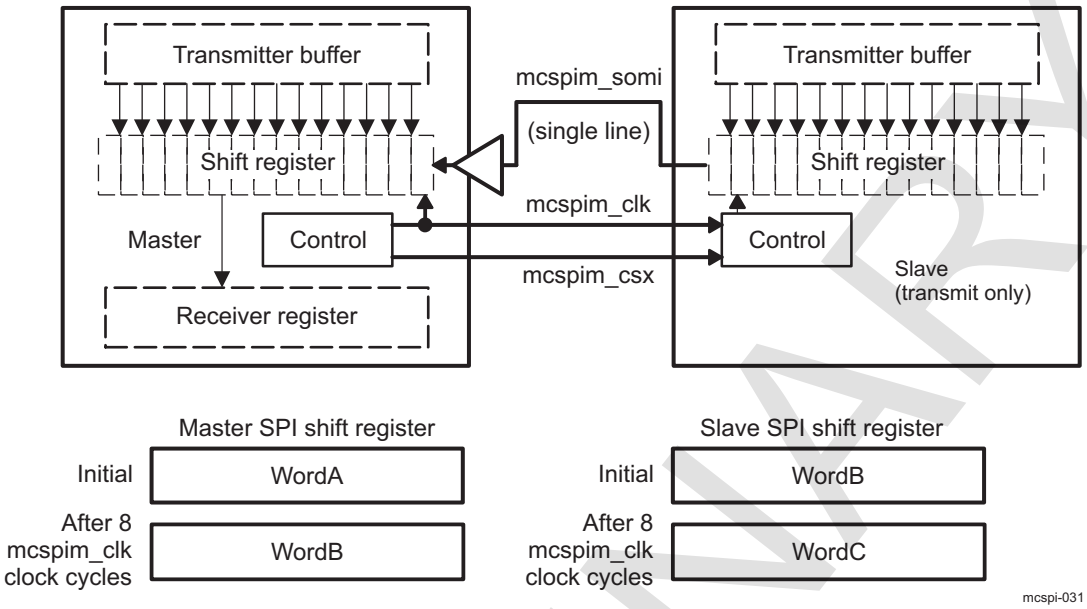
Figure 23-104. SPI Half-Duplex Transmission (Transmit-Only Slave)



23.4.4.3.4 Slave Receive-Only Mode

The slave receive mode is programmable (set the SPIm.MCSPI_CHxCONF[13:12] TRM bit field [where x = 0] to 0x1).

In receive-only mode, the MCSPI_TXx register must be loaded before the MCSPI is selected by an external SPI master device. The MCSPI_TXx register content is always loaded into the shift register whether it is updated or not. The TXx_UNDERFLOW event is activated accordingly and does not prevent transmission.

When an SPI word transfer completes (the SPIm.MCSPI_CHxSTAT0[2] EOT bit [where x = 0] is set to 1), the received data is transferred to the channel receive register.

To use the MCSPI as a slave receive-only device, the TXx_EMPTY and TXx_UNDERFLOW interrupts and the DMA write requests must be disabled due to the MCSPI_TXx register state.

For a full-duplex transmission, the serial clock (mcspim_clk) synchronizes shifting and sampling of the information on the single serial data line. For full duplex, two data lines are required. If mcspim_clk synchronizes on a single serial data line, the data line should be half-duplex.

Figure 23-105 shows an example of a half-duplex system with a master device on the left and a receive-only slave device on the right. Each time a bit transfers out from the master, 1 bit transfers in from the slave. After eight cycles of the serial clock mcspim_clk, Word A transfers from the master to the slave.

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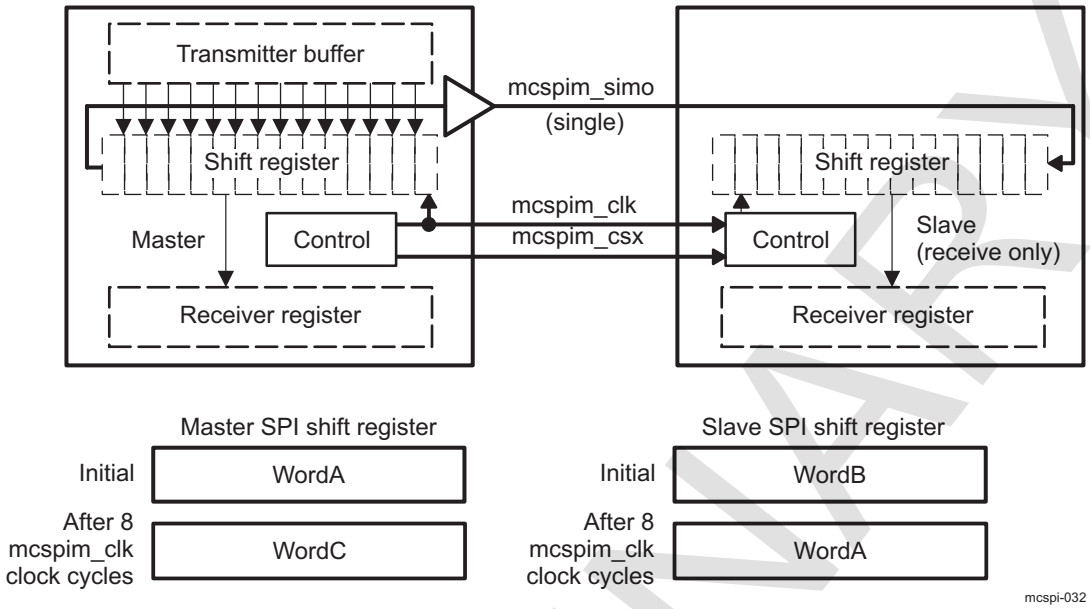
Figure 23-105. SPI Half-Duplex Transmission (Receive-Only Slave)



23.4.4.4 FIFO Buffer Management

The MCSPI controller has a built-in 64-byte buffer to unload the DMA or interrupt handler and improve data throughput.

This buffer can be used by only one channel at a time and is selected by setting the SPIm.MCSPI_CHxCONF[28] FFER or SPIm.MCSPI_CHxCONF[27] FFEW bits to 1. If several channels are selected and several FIFO enable bit fields are set to 1, the controller forces the buffer not to be used; the driver must set only one FIFO enable bit field.

The buffer can be used in the following modes:

- Master or slave mode
- Transmit-only, receive-only, or transmit-and-receive mode
- Single channel or turbo mode, or normal round-robin mode. In round-robin mode the buffer is used by only one channel.

  Every word length (SPIm.MCSPI_CHxCONF[11:7] WL) is supported.

In transmit-and-receive mode, the buffer can be used in transmit (see Figure 23-106) or receive (see Figure 23-107) directions, or in both directions. If only one direction is chosen in transmit-and-receive mode, the full buffer is used for this direction. In both directions, the buffer is split into two 32-byte buffers, one for each direction (see Figure 23-108).

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Figure 23-106. Buffer Used in Transmit Direction Only

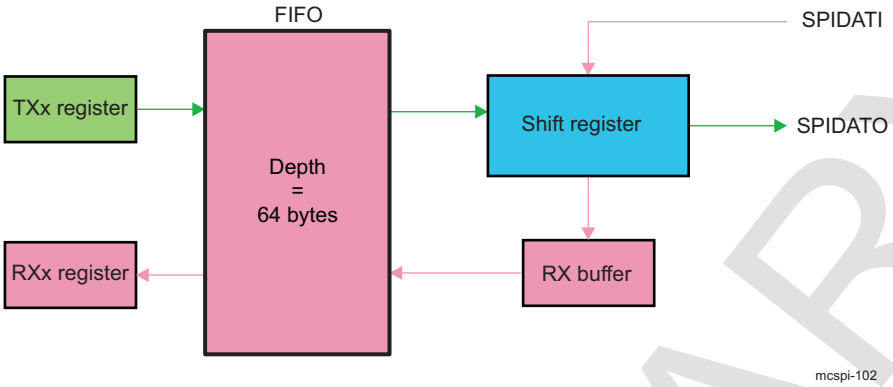


Figure 23-107. Buffer Used in Receive Direction Only

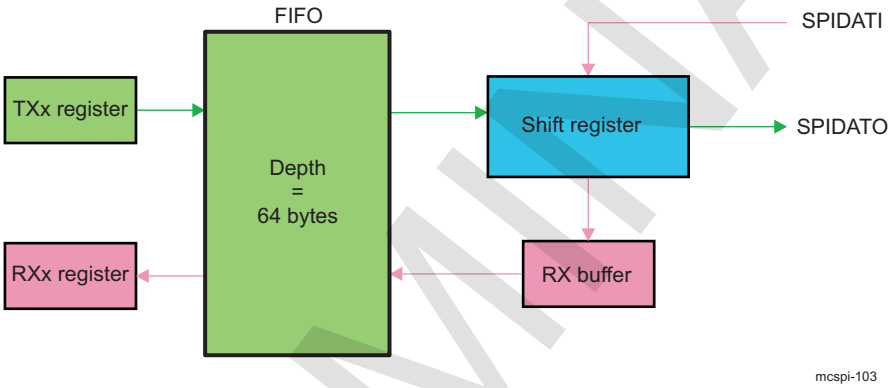
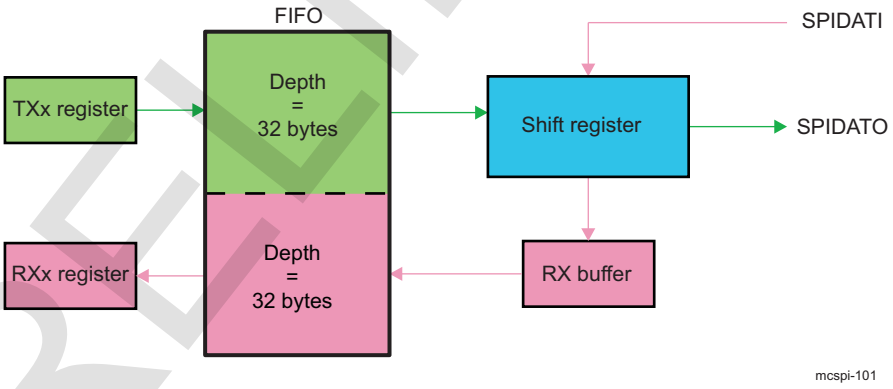


Figure 23-108. Buffer Used for Transmit and Receive Directions



Two levels (SPIm.MCSPI_XFERLEVEL[5:0] AEL and SPIm.MCSPI_XFERLEVEL[13:8] AFL) rule the buffer management. The granularity of these levels is 1 byte; it is not aligned with the SPI word length. The driver must set these values as a multiple of the SPI word length defined in WL. Table 23-273 shows the number of bytes written in the FIFO, depending on the word length.

Table 23-273. FIFO Writes, Word Length Relationship

SPI Word Length WL	3 <= WL<= 7	8 <= WL <= 15	16 <= WL <= 31
Number of byted written in the FIFO	1 byte	2 bytes	4 bytes

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The FIFO buffer pointers are reset when the corresponding channel is enabled or the FIFO configuration changes.

23.4.4.4.1 Buffer Almost Full

The MCSPI_XFERLEVEL[15:8] AFL bit field is needed when the buffer is used to receive an SPI word from a slave (the MCSPI_CHxCONF[28] FFER bit must be set to 1). It defines the almost-full buffer status. See Figure 23-109.

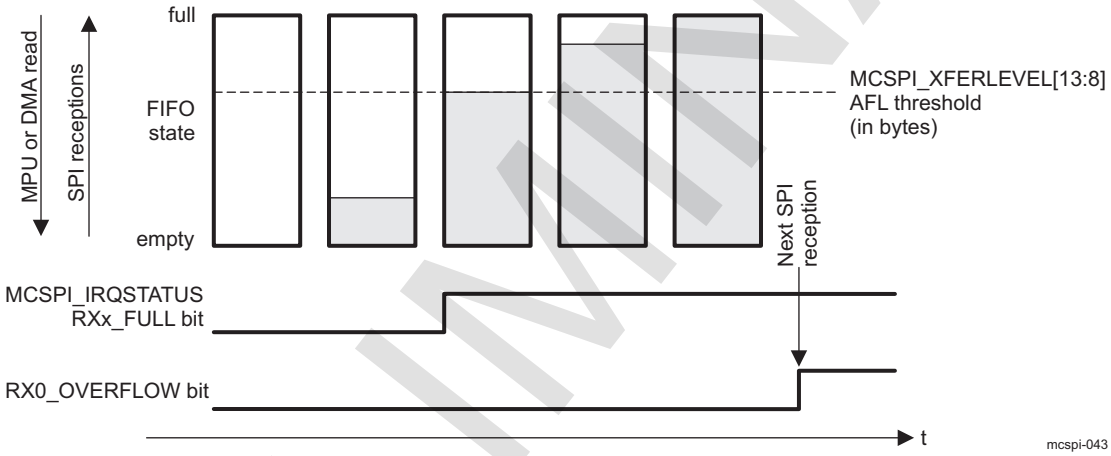
When the FIFO pointer reaches this level, an interrupt or a DMA request is sent to the MPU to enable the system to read AFL + 1 bytes from the receive register.

NOTE: AFL + 1 must correspond to a multiple value of the MCSPI_CHxCONF[11:7] WL bit field.

When DMA is used, the request is deasserted after the first receive register read.

No new request will be asserted again as long as the system has not performed the right number of read accesses.

Figure 23-109. Buffer Almost Full Level (AFL)



NOTE: The MCSPI_IRQSTATUS register bits are not available in DMA mode. In DMA mode, the SPIm_DMA_RXx request is asserted on the same conditions as the MCSPI_IRQSTATUS RXx_FULL flag.

23.4.4.4.2 Buffer Almost Empty

The MCSPI_XFERLEVEL[7:0] AEL bit field is needed when the buffer is used to transmit an SPI word to a slave (the MCSPI_CHxCONF[27] FFEW bit must be set to 1). It defines the almost-empty buffer status. See Figure 23-110.

When the FIFO pointer has not reached this level, an interrupt or a DMA request is sent to the MPU to enable the system to write AEL + 1 bytes to the transmit register.

NOTE: AEL + 1 must correspond to a multiple value of the MCSPI_CHxCONF[11:7] WL bit field.

When DMA is used, the request is deasserted after the first transmit register write.

No new request will be asserted again as long as the system has not performed the right number of write accesses.

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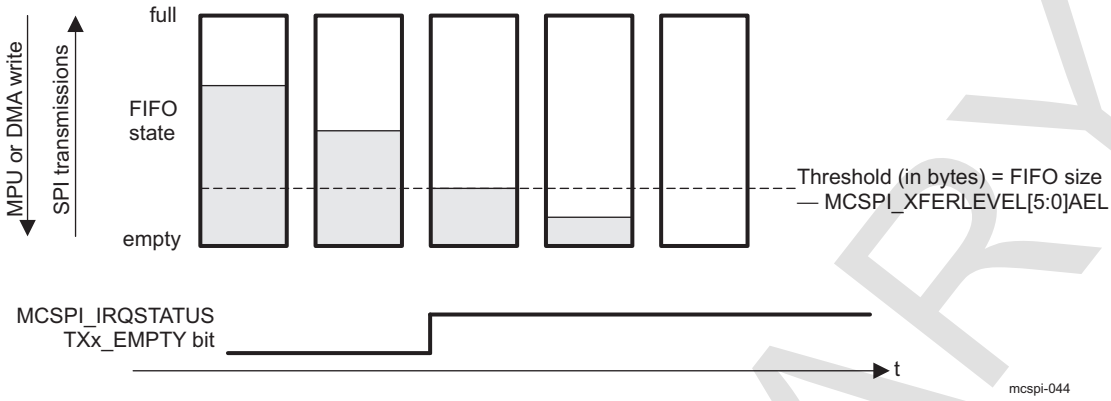
Figure 23-110. Buffer Almost Empty Level (AEL)



NOTE: The MCSPI_IRQSTATUS register bits are not available in DMA mode. In DMA mode, the SPIm_DMA_TXx request is asserted on the same conditions as the MCSPI_IRQSTATUS TXx_EMPTY flag.

23.4.4.4.3 End of Transfer Management

When the FIFO buffer is enabled for a channel, the user must previously configure in the MCSPI_XFERLEVEL register the AEL and AFL levels and especially the MCSPI_XFERLEVEL[31:16] WCNT bit field to define the number of SPI words to be transferred using the FIFO before enabling the channel.

This counter allows the controller to stop the transfer correctly after a defined number of SPI word transfers. If WNCT is set to 0x0000, the counter is not used and the user must stop the transfer manually by disabling the channel; in this case, the user does not know how many SPI transfers have been done. For received words, software must poll the CHxSTAT[5] RXFFE bit and read the MCSPI_RXx receive register to empty the FIFO buffer.

When the end-of-word count interrupt is generated (the MCSPI_IRQSTATUS[17] EOW bit is set), the user can disable the channel and poll the MCSPI_CHxSTAT[5] RXFFE bit to know it lasts SPI words in the FIFO buffer and read them.

No new request is asserted as long as the system has not performed the correct number of write accesses.

23.4.4.5 Interrupts

Each channel can issue interrupt events.

Each interrupt event has status bits in the SPIm.MCSPI_IRQSTATUS register (RXx_FULL, TXx_UNDERFLOW, TXx_EMPTY, …) (where x = 0, 3) that indicate whether service is required. Each status bit has an interrupt enable bit (a mask) in the SPIm.MCSPI_IRQENABLE register (RXx_FULL_ENABLE, TXx_UNDERFLOW_ENABLE, TXx_EMPTY_ENABLE, ...).

When an interrupt occurs and a mask is later applied on it, the interrupt line is not asserted again, even if the interrupt source is not serviced.

The MCSPI supports interrupt-driven and polling operations.

23.4.4.5.1 Interrupt Events in Master Mode

In master mode, the interrupt events related to the MCSPI_TXx register state are TXx_EMPTY and TXx_UNDERFLOW. The interrupt event related to the MCSPI_RXx register state is RXx_FULL.

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23.4.4.5.1.1 TXx_EMPTY

The TXx_EMPTY event is activated when a channel is enabled and its MCSPI_TXx register is empty (transient event). Enabling a channel automatically triggers this event, except in master receive-only mode (see Section 23.4.4.2.4, *Master Receive-Only Mode*). When the FIFO buffer is enabled (the MCSPI_CHxCONF[27] FFEW bit is set to 1), the MCSPI_IRQSTATUS TXx_EMPTY bit is set as soon as there is enough space in the buffer to write a number of bytes defined by the MCSPI_XFERLEVEL[5:0] AEL bit field.

The MCSPI_TXx register must be loaded with data to remove the source of the interrupt; the SPIm.MCSPI_IRQSTATUS TXx_EMPTY interrupt status bit must be cleared for interrupt line deassertion (if the event is enabled as the interrupt source).

When FIFO is enabled, no new TXx_EMPTY event will be asserted as soon as the MPU has not performed the number of writes into the MCSPI_TXx register defined by the MCSPI_XFERLEVEL[5:0] AEL bit field. The MPU must perform the right number of writes.

23.4.4.5.1.2 TXx_UNDERFLOW

The event TXx_UNDERFLOW is activated when the channel is enabled and if the MCSPI_TXx register or the FIFO is empty (not updated with new data) when an external master device starts a data transfer with the MCSPI (transmit and receive).

The TXx_UNDERFLOW is a harmless warning in master mode.

To avoid having a TXx_UNDERFLOW event at the beginning of a transmission, the event TXx_UNDERFLOW is not activated when no data has been loaded into the MCSPI_TXx register, because the channel has been enabled. To avoid having a TXx_UNDERFLOW event, the MCSPI_TXx register must seldom be loaded.

The SPIm.MCSPI_IRQSTATUS TXx_UNDERFLOW interrupt status bit must be cleared for interrupt line deassertion (if event enabled as the interrupt source).

23.4.4.5.1.3 RXx_ FULL

The RXx_FULL event is activated when channel is enabled and MCSPI_RXx register becomes filled (transient event). When the FIFO buffer is enabled (the MCSPI_CHxCONF[28] FFER bit is set to 1), RXx_ FULL is asserted as soon as the number of bytes holds in the FIFO to be read reaches the MCSPI_XFERLEVEL[13:8] AFL threshold.

The MCSPI_RXx register must be read to remove the source of the interrupt; the MCSPI_IRQSTATUS RXx_FULL interrupt status bit must be cleared for interrupt line deassertion (if the event is enabled as the interrupt source).

When FIFO is enabled, no new RXx_FULL event will be asserted as soon as the MPU has not performed AFL + 1 reads into MCSPI_RXx. The MPU must perform the right number of reads.

23.4.4.5.1.4 End Of Word Count

The MCSPI_IRQSTATUS[17] EOW event (end of word count) is activated when the channel is enabled and configured to use the built-in FIFO. This interrupt is raised when the controller performs the number of transfers defined in the MCSPI_XFERLEVEL[31:16] WCNT bit field. If WCNT is set to 0x0000, the counter is not enabled and this interrupt is not generated.

The end of word count interrupt also indicates that the SPI transfer is halted on the channel using the FIFO buffer as soon as MCSPI_XFERLEVEL[31:16] WCNT is not reloaded and the channel is not re-enabled.

The MCSPI_IRQSTATUS[17] EOW interrupt status bit must be cleared for interrupt line deassertion (if the event enabled as interrupt source).

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23.4.4.5.2 Interrupt Events in Slave Mode

In slave mode, the interrupt events related to the MCSPI_TXx register state are TXx_EMPTY and TXx_UNDERFLOW. The interrupt events related to the MCSPI_RXx register state are RXx_FULL and RX0_OVERFLOW (channels 1, 2, and 3 do not have a receiver overflow status bit). See the MCSPI_IRQSTATUS register.

23.4.4.5.2.1 TXx_EMPTY

The TXx_EMPTY event is activated when a channel is enabled and its MCSPI_TXx register is empty. Enabling the channel automatically raises this event. If the FIFO buffer is enabled (the MCSPI_CHxCONF[27] FFEW bit is set to 1), the TXx_EMPTY event will be asserted as soon as there is enough space in buffer to write a number of bytes defined by the MCSPI_XFERLEVEL[5:0] AEL bit field.

The MCSPI_TXx register must be loaded with data to remove the source of the interrupt; the SPIm.MCSPI_IRQSTATUS TXx_EMPTY interrupt status bit must be cleared for interrupt line deassertion (if the event is enabled as the interrupt source).

When FIFO is enabled, no new TXx_EMPTY event will be asserted as soon as the MPU has not performed the number of write into the MCSPI_TXx register defined by MCSPI_XFERLEVEL[5:0] AEL bit field. The MPU must perform the right number of writes.

23.4.4.5.2.2 TXx_UNDERFLOW

The TXx_UNDERFLOW event is activated when a channel is enabled and if the MCSPI_TXx register is empty (not updated with new data) when an external master device starts a data transfer with the MCSPI (transmit and receive).

When FIFO is enabled, the data emitted while the underflow event is raised is not the last data written in the FIFO but the next data in the FIFO (an old transmitted value or a dummy data in the FIFO has been reset).

TXx_UNDERFLOW indicates an error (data loss) in slave mode.

To avoid having a TXx_UNDERFLOW event at the beginning of a transmission, the TXx_UNDERFLOW event is not activated when no data has been loaded into the MCSPI_TXx register because the channel is enabled.

The SPIm.MCSPI_IRQSTATUS TXx_UNDERFLOW interrupt status bit must be cleared for interrupt line deassertion (if the event is enabled as the interrupt source).

23.4.4.5.2.3 RXx_FULL

The RXx_FULL event is activated when a channel is enabled and the MCSPI_RXx register is being filled (transient event). When the FIFO buffer is enabled (the MCSPI_CHxCONF[28] FFER bit is set to 1), RXx_FULL is asserted as soon as the number of bytes holds in the buffer to read defined by the MCSPI_XFERLEVEL[13:8] AFL bit field.

The MCSPI_RXx register must be read to remove the source of the interrupt; the SPIm.MCSPI_IRQSTATUS RXx_FULL interrupt status bit must be cleared for interrupt line deassertion (if the event is enabled as the interrupt source).

When FIFO is enabled, no new RXx_FULL event will be asserted as soon as the MPU has not performed AFL + 1 reads into MCSPI_RXx. The MPU must perform the correct number of reads.

23.4.4.5.2.4 RX0_OVERFLOW

The RX0_OVERFLOW event is activated in slave mode in either transmit-and-receive or receive-only mode, when a channel is enabled and the MCSPI_RXx register or FIFO is full when a new SPI word is received. The MCSPI_RXx register is always overwritten with the new SPI word. If the FIFO is enabled data within the FIFO are overwritten, it must be considered as corrupted. The RX0_OVERFLOW event should not appear in slave mode using the FIFO.

The RX0_OVERFLOW event indicates an error (data loss) in slave mode.

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The MCSPI_IRQSTATUS[3] RX0_OVERFLOW interrupt status bit must be cleared for interrupt line deassertion (if the event is enabled as the interrupt source).

23.4.4.5.2.5 End Of Word Count

The MCSPI_IRQSTATUS[17] EOW event (end of word count) is activated when the channel is enabled and configured to use the built-in FIFO. This interrupt is raised when the controller performs the number of transfer defined in the MCSPI_XFERLEVEL[31:16] WCNT bit field. If WCNT is set to 0x0000, the counter is not enabled and this interrupt is not generated.

The end of word count interrupt also indicates that the SPI transfer is halted on the channel using the FIFO buffer as soon as WCNT is not reloaded and the channel re-enabled.

The MCSPI_IRQSTATUS[17] EOW interrupt status bit must be cleared for interrupt line deassertion (if event enable as interrupt source).

23.4.4.5.3 Interrupt-Driven Operation

An interrupt enable bit in the SPIm.MCSPI_IRQENABLE register can be set to enable each event to generate interrupt requests when the corresponding event occurs. Status bits are automatically set by hardware logic conditions.

When an event occurs (the single interrupt line is asserted), the MPU must:

1. Read the SPIm.MCSPI_IRQSTATUS register to identify which event occurred.
2. Read the MCSPI_RXx register that corresponds to the event to remove the source of an RXx_FULL event or write into the MCSPI_TXx register that corresponds to the event to remove the source of a TXx_EMPTY event. No action is required to remove the source of the WKS (wake-up), TXx_ UNDERFLOW, and RX0_OVERFLOW events.
3. Set the corresponding bit of the SPIm.MCSPI_IRQSTATUS register to 1 to clear an interrupt status and then release the interrupt line.

The interrupt status bit must always be reset after channel enabling and before events are enabled as interrupt sources.

23.4.4.5.4 Polling

When the interrupt capability of an event is disabled in the SPIm.MCSPI_IRQENABLE register, the interrupt line is not asserted, but the status bits in the SPIm.MCSPI_IRQSTATUS register can be polled by software to detect when the corresponding event occurs.

Once the expected event occurs:

- RXx_FULL: To remove the source of the event, the MPU must read the corresponding MCSPI_RXx register.
- TXx_EMPTY: To remove the source of the event, the MPU must write into the corresponding MCSPI_TXx register.
- WKS (wake-up), TXx_UNDERFLOW, and RX0_OVERFLOW: No action is required to remove the source of the event.

To clear an interrupt, set the corresponding status bit of the SPIm.MCSPI_IRQSTATUS register to 1. This does not affect the interrupt line state.

23.4.4.6 DMA Requests

The sDMA controller module manages DMA accesses. The sDMA controller advantage is to reduce the MPU charge for data transfers.

Each MCSPI channel , if enabled, can issue DMA requests. There are two DMA request lines per MCSPI channel (one for read and one for write).

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The DMA read request line is asserted when the MCSPI channel is enabled and new data is available in the receive register of the MCSPI channel. A DMA read request can be individually masked with the SPI1.MCSPI_CHxCONF[15] DMAR bit. The DMA read request line is deasserted when reading of the MCSPI_RXx register of the MCSPI channel is complete.

The DMA write request line is asserted when the MCSPI channel is enabled and the MCSPI_TXx register of the MCSPI channel is empty. A DMA write request can be individually masked with the SPI1.MCSPI_CHxCONF[14] DMAW bit. The DMA write request line is deasserted when loading of the MCSPI_TXx register of the channel is complete.

23.4.4.7 Power Saving Management

Power consumption can be optimized by switching off internal clocks (interface and functional clock) when there is no activity. The MCSPI is compliant with the idle and wake-up system handshake protocol.

23.4.4.7.1 Normal Mode

In normal mode, internal SPI module clocks are automatically switched off (autogated) when there is no activity in slave or master mode.

Autogating of the module interface clock and functional clock occurs when the following conditions are met:

- The SPIm.MCSPI_SYSCONFIG[0] AUTOIDLE bit is set.
- In master mode, there is no data to transmit or receive in all channels.
- In slave mode, the MCSPI is not selected by the external master and there are no register accesses.

Autogating of the module interface clock and functional clock stops when the following conditions are met:

- In master mode, an internal access occurs.
- In slave mode, an internal access occurs or the MCSPI is selected by the external master.

23.4.4.7.2 Idle Mode

At the PRCM module level, when all conditions are met to shut off the CORE_48M_FCLK or CORE_L4_ICLK output clocks (for details, see Chapter 3, *Power, Reset, and Clock Management*), the PRCM module automatically launches a hardware handshake protocol to ensure that the MCSPI is ready to have its clocks switched off. Namely, the PRCM module asserts an idle request to the MCSPI.

Although this handshake is completely hardware-oriented and out of software control, the method in which the MCSPI module acknowledges the PRCM idle request is configurable through the MCSPI.SYSCONFIG[4:3] SIDLEMODE bit field.

The settings of the SIDLEMODE bit field and the related acknowledgment modes are:

- Force-idle mode (the SPIm.MCSPI_SYSCONFIG[4:3] SIDLEMODE bit field is set to 0x0): The MCSPI module acknowledges unconditionally the idle request from the PRCM module, regardless of its internal operations. This mode must be used carefully in this case because it does not prevent the loss of data when the clock is switched off.
- No-idle mode (the SIDLEMODE bit is set to 0x1): The MCSPI never acknowledges an idle request from the PRCM module and is safe from a module point of view because it ensures that the clocks remain active. However, it is not efficient to save power because it does not allow the PRCM output clock to be shut off and thus the power domain to be set to a lower power state.
- Smart-idle mode (the SIDLEMODE bit is set to 0x2): The MCSPI acknowledges the idle request, basing its decision on its internal activity. Namely, the acknowledge signal is asserted only when all pending transactions, IRQs, or DMA requests are treated. This is the best approach for efficient system power management.

When configured in smart-idle mode, the MCSPI also offers an additional granularity on the CORE_48M_FCLK and CORE_L4_ICLK gating. The SPIm.SYSCONFIG[9:8] CLOCKACTIVITY bit field determines which clock shuts down (the CORE_48M_FCLK, CORE_L4_ICLK, neither clock, or both clocks).

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The CLOCKACTIVITY setting is used internally to the MCSPI to determine on which part of the module the conditions to acknowledge the PRCM idle request are tested. For example, if CORE_48M_FCLK is not shut down on a PRCM idle request, the MCSPI considers only CORE_L4_ICLK and the associated pending activities before acknowledging the request.

Some MCSPI features are associated with CORE_L4_ICLK and others with CORE_48M_FCLK. Using the CLOCKACTIVITY bit field with the smart-idle mode ensures that the features associated with the clock that remains active are always enabled, even if the MCSPI acknowledges an idle request.

The CLOCKACTIVITY settings and the associated features are:

- CLOCKACTIVITY set to 00: ICLK off and FCLK off, ICLK and FCLK are considered for generating the acknowledge. This setting also means that FCLK and ICLK are likely to be shut down on a PRCM idle request.
- CLOCKACTIVITY set to 01: ICLK on and FCLK off, ICLK is not shut down on a PRCM idle request; only FCLK is concerned.
- CLOCKACTIVITY set to 10: ICLK off and FCLK on, FCLK is not shut down on a PRCM idle request; only ICLK is concerned.
- CLOCKACTIVITY set to 11: ICLK on and FCLK on, none of the clocks are shut down. This means the MCSPI can potentially acknowledge the idle request without checking the internal functions linked to its clocks.

CAUTION

The PRCM module does not have a hardware means of reading the CLOCKACTIVITY settings. Therefore, software must ensure consistent programming between CLOCKACTIVITY and the CORE_48M_FCLK and CORE_L4_ICLK control bits in the PRCM module. If the MCSPI is disabled in the CM_FCLKEN and CM_ICLKEN PRCM registers while CLOCKACTIVITY is set to 11, nothing prevents the PRCM module from asserting its idle request, which is acknowledged regardless of the features associated with the MCSPI clocks. This can lead to unpredictable behavior.

23.4.4.7.2.1 Wake-Up Event in Smart-Idle Mode

The module wake-up feature is enabled when the SPIm.MCSPI_SYSCONFIG[2] ENAWAKEUP and SPIm.MCSPI_WAKEUPENABLE[0] WKEN bits are set. Wake-up capability is relevant only when the module is configured in slave mode.

The module generates an asynchronous wakeup request to the system power manager to switch back the interface clock and the functional clock. A wake-up is requested when channel 0 is enabled and an asynchronous selection occurs on the mcspim.csx port associated with channel 0 (see the definition for the SPIm.MCSPI_CHxCONF[22:21] SPIENSLV bit field [where x = 0] in the register description table).

After the McSPI wake-up request, the system power manager must reactivate the interface clock:

- Before the beginning of the second SPI word serialization when the McSPI is in slave transmit-only mode or in slave transmit-and-receive mode
- Before the end of the second received SPI word in slave receive-only mode. To avoid data loss, the first received SPI word must be read from the SPIm.MCSPI_RXx register (where x = 0) before the completion of the second SPI word serialization.

Table 23-274 lists the supported cases in wake-up mode.

Table 23-274. Smart-Idle Mode and Wake-Up Capabilities

Mode	Interface Clock	SPI Clock Ref	Functionality	Wake-Up Event
Master	Must be maintained	Must be maintained	Full functionality, but the module does not generate a new interrupt or DMA request until the system exits wake-up mode	No wake-up event

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Table 23-274. Smart-Idle Mode and Wake-Up Capabilities (continued)

Mode	Interface Clock	SPI Clock Ref	Functionality	Wake-Up Event
Slave	Can be switched off	Can be switched off	An SPI word can be transmitted and/or received, but the module does not generate any new interrupts or DMA requests until the system exits wake-up mode.	The module asynchronously sends a wake-up request if an event on the mcspim_csx port associated with channel 0 is detected.

In wake-up mode, the interrupt and DMA request lines are no longer asserted.

Any access to the module in wake-up mode generates an error as long as the interface clock is alive.

23.4.4.7.2.2 Transitions From Smart-Idle Mode to Normal Mode

The MCSPI detects the end of the wake period through the idle and wake-up hardware handshake protocol.

The interrupt status register (the SPIm.MCSPI_IRQSTATUS[16] WKS bit) is updated with the event causing the wakeup; the wake-up event at the origin of the transition to the normal mode is converted to its corresponding interrupt when enabled by the SPIm.MCSPI_IRQENABLE[16] WKE bit or the DMA request.

Interrupts and wake-up events have independent enable and disable controls, accessible through the SPIm.MCSPI_IRQENABLE and SPIm.MCSPI_WAKEUPENABLE registers. Software must ensure the overall consistency.

The interrupt status register SPIm.MCSPI_IRQSTATUS is updated with the event causing the wake-up; the wake-up event at the origin of the transition to normal mode is converted to its corresponding interrupt request or DMA request. The module is fully operational.

23.4.4.7.2.3 Force-Idle Mode

Force-idle mode is enabled and exited as follows:

- Force-idle mode is enabled when the SPIm.MCSPI_SYSCONFIG[4:3] SIDLEMODE bit field is set to 0x0.
  - In force-idle mode, the MCSPI responds unconditionally to the idle request by deasserting unconditionally the interrupt and DMA request lines, if asserted. In addition, the wake-up capability is totally inhibited even if the SPIm.MCSPI_SYSCONFIG[2] ENAWAKEUP and SPIm.MCSPI_WAKEUPENABLE[0] WKEN bits are set.
  - The transition from normal mode to idle mode does not affect the interrupt event bits of the SPIm.MCSPI_IRQSTATUS register.
  - In force-idle mode, because the module must be disabled, the interrupt and DMA request lines are likely deasserted. The interface clock and SPI clock provided to the MCSPI can be switched off.
  - An idle request during an SPI data transfer can lead to an unexpected and unpredictable result. Software must avoid such a request.
- The module exits force-idle mode through the idle and wake-up hardware handshake protocol.

  The module is fully operational. The interrupt and DMA request lines are optionally asserted one clock cycle later.

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23.4.5 MCSPI Programming Guide

23.4.5.1 MCSPI Low-Level Programming Models

This section describes the low-level hardware programming sequences for the configuration and use of the MCSPI module.

23.4.5.1.1 Global Initialization

23.4.5.1.1.1 Surrounding Modules Global Initialization

This section identifies the requirements for initializing the surrounding modules when the I^2C module is to be used for the first time after a device reset. This initialization of surrounding modules is based on the integration and environment of the I^2C. For further information, see the *I^2C Module Integration* and *Environment* sections.

For more information, see Section 23.4.3.

Table 23-275 lists the information on the global initialization of the surrounding modules.

Table 23-275. Global Initialization of Surrounding Modules

Surrounding Modules	Comments
PRCM	MCSPI_FCLK functional clock must be enabled. See Section 3.1.1.1.2 , *Module Level Clock Management*, in Chapter 3, *Power, Reset, and Clock Management*.
L4 Interconnect	For information about L4-PER interconnect configuration, see Section 13.3, *L4 Interconnects*, in Chapter 13, *Interconnect*.
sDMA	DMA configuration must be done to enable the module DMA channel requests. See Chapter 16, *SDMA*.
MPU INTC	Cortex-A9 MPU, Cortex-M3 MPU, or DSP INTC must be configured to enable the interrupt request generation to the Cortex-A9 MPU or Cortex-M3 MPU, or in , *INTC*, in Chapter 5, *DSP Subsystem*.

23.4.5.1.2 MCSPI Global Initialization

23.4.5.1.2.1 Main Sequence – MCSPI Global Initialization

This procedure initializes the MCSPI module after a POR or software reset.

Table 23-276. MCSPI Global Initialization

Step	Register/Bit Field/Programming Model	Value
Perform a software reset.	SPIm.MCSPI_SYSCONFIG[1] SOFTRESET	0x1
Wait until reset is finished?	SPIm.MCSPI_SYSSTATUS[0] RESETDONE	=0x1

23.4.5.1.2 Operational Mode Configuration

23.4.5.1.2.1 MCSPI Operational Modes

The selection of the working mode is done with the SPIm.MCSPI_CHxCONF register. Table 23-277 through Table 23-279 list the possible operating modes and their configurations.

Table 23-277. MCSPI Receive Mode Initialization

Step	Register/Bit Field/Programming Model	Value
Set receive mode.	SPIm.MCSPI_CHxCONF[13:12] TRM	0x1
Set the word length.	SPIm.MCSPI_CHxCONF[11:7] WL	0x8
Clock initialization and channel enabling	SPIm.MCSPI_MODULCTRL[2] MS SPIm.MCSPI_CHxCTRL[0] EN	0x0 0x1

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Table 23-277. MCSPI Receive Mode Initialization (continued)

Step	Register/Bit Field/Programming Model	Value
Channels activated low during active state	SPIm.MCSPI_CHxCONF[6] EPOL	0x1
Clock held high during active state	SPIm.MCSPI_CHxCONF[1] POL	0x0
Data latched on odd-numbered edges of the SPI clock	SPIm.MCSPI_CHxCONF[0] PHA	0x0
Reset the status bits.	SPIm.MCSPI_IRQSTATUS	0x0

Table 23-278. MCSPI Transmit Mode Initialization

Step	Register/Bit Field/Programming Model	Value
Set transmit mode.	SPIm.MCSPI_CHxCONF[13:12] TRM	0x2
Set the word length.	SPIm.MCSPI_CHxCONF[11:7] WL	0x8
Clock initialization and channel enabling	SPIm.MCSPI_MODULCTRL[2] MS SPIm.MCSPI_CHxCTRL[0] EN	0x0 0x1
Channels activated low during active state	SPIm.MCSPI_CHxCONF[6] EPOL	0x1
Clock held high during active state	SPIm.MCSPI_CHxCONF[1] POL	0x0
Data latched on odd-numbered edges of the SPI clock	SPIm.MCSPI_CHxCONF[0] PHA	0x0
Reset the status bits.	SPIm.MCSPI_IRQSTATUS	0x0

Table 23-279. MCSPI Transmit-and-Receive Mode Initialization

Step	Register/Bit Field/Programming Model	Value
Set transmit and receive mode.	SPIm.MCSPI_CHxCONF[13:12] TRM	0x0
Set the word length.	SPIm.MCSPI_CHxCONF[11:7] WL	0x8
Clock initialization and channel enabling	SPIm.MCSPI_MODULCTRL[2] MS SPIm.MCSPI_CHxCTRL[0] EN	0x0 0x1
Channels activated low during active state	SPIm.MCSPI_CHxCONF[6] EPOL	0x1
Clock held high during active state	SPIm.MCSPI_CHxCONF[1] POL	0x0
Data latched on odd-numbered edges of the SPI clock	SPIm.MCSPI_CHxCONF[0] PHA	0x0
Reset the status bits.	SPIm.MCSPI_IRQSTATUS	0x0

23.4.5.1.2.1.1 Common Transfer Procedures Without FIFO – Polling Method

23.4.5.1.2.1.1.1 Receive-Only Procedure – Polling Method

Table 23-280 lists the receive-only procedure using the polling method. The MCSPI is acting as slave.

Table 23-280. Receive-Only Procedure – Polling Method

Step	Register/Bit Field/Programming Model	Value
Configure the channel according to the mode	See Table 23-277.	
Start the channel.	SPIm.MCSPI_CHxCTRL[0] EN	0x1
Wait until receive register is full?	SPIm.MCSPI_RXx	=0x1
Stop the channel.	SPIm.MCSPI_CHxCTRL[0] EN	0x0

23.4.5.1.2.1.1.2 Receive-Only Procedure – Interrupt Method

Table 23-281 lists the receive-only procedure using the interrupt method. The MCSPI is acting as slave.

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Table 23-281. Receive-Only Procedure – Interrupt Method

Step	Register/Bit Field/Programming Model	Value
Configure the channel according to the mode.	See Table 23-277.	
Start the channel.	SPIm.MCSPI_CHxCTRL[0] EN	0x1
Enable the interrupt for the receiver register.	SPIm.MCSPI_IRQENABLE[2] RX_FULL_ENABLE	0x1
Read the status register.	SPIm.MCSPI_IRQSTATUS[2] RX_FULL	0x0
Disable the interrupt.	SPIm.MCSPI_IRQENABLE[2] RX_FULL_ENABLE	0x0
Stop the channel.	SPIm.MCSPI_CHxCTRL[0] EN	0x0
Read the receiver register.	SPIm.MCSPI_RXx	xxxx

23.4.5.1.2.1.1.3 Transmit-Only Procedure – Polling Method

Table 23-282 lists the transmit-only procedure using the polling method. The MCSPI is acting as master.

Table 23-282. Transmit-Only Procedure – Polling Method

Step	Register/Bit Field/Programming Model	Value
Configure the channel according to the mode.	See Table 23-278	
Start the channel.	SPIm.MCSPI_CHxCTRL[0] EN	0x1
Wait until end of transfer?	SPIm.MCSPI_CHxSTAT[2:1]	=0x2
Stop the channel.	SPIm.MCSPI_CHxCTRL[0] EN	0x0

23.4.5.1.2.1.1.4 Transmit-and-Receive Procedure – Polling Method

Table 23-282 lists the transmit-and-receive procedure using the polling method. The MCSPI is acting as master and slave.

Table 23-283. Transmit-and-Receive Procedure – Polling Method

Step	Register/Bit Field/Programming Model	Value
Configure the channel according to the mode.	See Table 23-279.	
Start the channel.	SPIm.MCSPI_CHxCTRL[0] EN	0x1
Wait until transmit/receive word?	SPIm.MCSPI_CHxSTAT[2:0]	=0x3
Stop the channel.	SPIm.MCSPI_CHxCTRL[0] EN	0x0

23.4.5.1.3 Common Transfer Procedures With FIFO – Polling Method

When using FIFO the MCSPI module can start the transfer only after the first write request is released by writing the MCSPI_TXx register. The first write request can be managed by the IRQ routine or DMA handler. The end of transfer is more complex and depends on the transfer type. See Table 23-282 through Table 23-289.

23.4.5.1.3.1 Receive-Only Procedure With Word Count – Polling Method

Table 23-284. Receive-Only Procedure With Word Count – Polling Method

Step	Register/Bit Field/Programming Model	Value
Configure the channel according to the mode.	See Table 23-277.	
Start the channel.	SPIm.MCSPI_CHxCTRL[0] EN	0x1
Wait until end of word count?	SPIm.MCSPI_IRQSTATUS[17] EOW	=0x1
Stop the channel.	SPIm.MCSPI_CHxCTRL[0] EN	0x0
Read from the receiver register.	SPIm.MCSPI_RXx	xxxx

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23.4.5.1.3.2 Transmit-Only Procedure With and Without Word Count – Polling Method

Table 23-285. Transmit-Only Procedure Without Word Count – Polling Method

Step	Register/Bit Field/Programming Model	Value
Configure the channel according to the mode.	See Table 23-278.	
Start the channel.	SPIm.MCSPI_CHxCTRL[0] EN	0x1
Wait until end of word count?	SPIm.MCSPI_IRQSTATUS[17] EOW	=0x1
Wait until end of transfer?	SPIm.MCSPI_CHxSTAT[2] EOT SPIm.MCSPI_CHxSTAT[3] TXFFE	=0x1 =0x1
Stop the channel.	SPIm.MCSPI_CHxCTRL[0] EN	0x0

23.4.5.1.3.3 Transmit-Only Procedure With and Without Word Count – Interrupt Method

Table 23-286. Transmit-Only Procedure With Word Count – Interrupt Method

Step	Register/Bit Field/Programming Model	Value
Configure the channel according to the mode.	See Table 23-278.	
Start the channel.	SPIm.MCSPI_CHxCTRL[0] EN	0x1
Enable the interrupt for the transmit register.	SPIm.MCSPI_IRQENABLE[4] TX_EMPTY_ENABLE	0x1
End of word count.	SPIm.MCSPI_IRQSTATUS[17] EOW	=0x1
End of transfer	SPIm.MCSPI_CHxSTAT[2] EOT SPIm.MCSPI_CHxSTAT[3] TXFFE	=0x1 =0x1
Clear the interrupt.	SPIm.MCSPI_IRQENABLE[17] EOW_ENABLE	=0x0
Disable the interrupt for the transmit register.	SPIm.MCSPI_IRQENABLE[4] TX_EMPTY_ENABLE	0x0
Stop the channel.	SPIm.MCSPI_CHxCTRL[0] EN	0x0

23.4.5.1.3.4 Transmit-and-Receive Procedure With Word Count – Polling Method

Table 23-287. Transmit-and-Receive Procedure With Word Count – Polling Method

Step	Register/Bit Field/Programming Model	Value
Configure the channel according to the mode.	See Table 23-279.	
Start the channel.	SPIm.MCSPI_CHxCTRL[0] EN	0x1
Wait until end of word count?	SPIm.MCSPI_IRQSTATUS[17] EOW	=0x1
Stop the channel.	SPIm.MCSPI_CHxCTRL[0] EN	0x0
Read from the receiver register.	SPIm.MCSPI_RXx	xxxx

23.4.5.1.3.5 Transmit-and-Receive Procedure with Word Count – Interrupt Method

Table 23-288. Transmit-and-Receive Procedure With Word Count – Interrupt Method

Step	Register/Bit Field/Programming Model	Value
Configure the channel according to the mode.	See Table 23-279.	
Start the channel.	SPIm.MCSPI_CHxCTRL[0] EN	0x1
Enable the interrupt for the receiver register.	SPIm.MCSPI_IRQENABLE[2] RX_FULL_ENABLE	0x1
Enable the interrupt for the transmit register.	SPIm.MCSPI_IRQENABLE[4] TX_EMPTY_ENABLE	0x1
End of word count?	SPIm.MCSPI_IRQSTATUS[17] EOW	=0x1
Clear the interrupt.	SPIm.MCSPI_IRQENABLE[17] EOW_ENABLE	=0x0

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Table 23-288. Transmit-and-Receive Procedure With Word Count – Interrupt Method (continued)

Step	Register/Bit Field/Programming Model	Value
Disable the interrupt for the receiver register.	SPIm.MCSPI_IRQENABLE[4] TX_EMPTY_ENABLE	0x0
Disable the interrupt for the transmit register.	SPIm.MCSPI_IRQENABLE[2] RX_FULL_ENABLE	0x0
Stop the channel.	SPIm.MCSPI_CHxCTRL[0] EN	0x0
Read from the receiver register.	SPIm.MCSPI_RXx	xxxx

23.4.5.1.3.6 Transmit-and-Receive Procedure Without Word Count – Polling Method

Table 23-289. Transmit-and-Receive Procedure Without Word Count – Polling Method

Step	Register/Bit Field/Programming Model	Value
Configure the channel according to the mode.	See Table 23-279.	
Start the channel.	SPIm.MCSPI_CHxCTRL[0] EN	0x1
Wait until end of transfer?	SPIm.MCSPI_CHxSTAT[2] EOT SPIm.MCSPI_CHxSTAT[3] TXFFE	=0x1 =0x1
Stop the channel.	SPIm.MCSPI_CHxCTRL[0] EN	0x0
Read from the receiver register.	SPIm.MCSPI_RXx	xxxx

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23.4.6 MCSPI Register Manual

23.4.6.1 MCSPI Instance Summary

Table 23-290. MCSPI Instance Summary

Module Name	Base Address	Size
MCSPI1	0x4809 8000	4KB
MCSPI2	0x4809 A000	4KB
MCSPI3	0x480B 8000	4KB
MCSPI4	0x480B A000	4KB

23.4.6.2 MCSPI Registers

23.4.6.2.1 MCSPI Register Summary

Table 23-291 lists the MCSPI registers. Each register is 32 bits wide.

Table 23-291. MCSPI Register Summary

Register	Type	Offset Address	MCSPI1 L3 Physical Address	MCSPI2 L3 Physical Address	MCSPI3 L3 Physical Address	MCSPI4 L3 Physical Address
MCSPI_HL_REV	Rw	0x00	0x4809 8000	0x4809 A000	0x480B 8000	0x480B A000
MCSPI_HL_HWINFO	Rw	0x04	0x4809 8004	0x4809 A004	0x480B 8004	0x480B A004
MCSPI_HL_SYSCONFIG	Rw	0x10	0x4809 8010	0x4809 A010	0x480B 8010	0x480B A010
MCSPI_REVISION	R	0x100	0x4809 8100	0x4809 A100	0x480B 8100	0x480B A100
MCSPI_SYSCONFIG	RW	0x110	0x4809 8110	0x4809 A110	0x480B 8110	0x480B A110
MCSPI_SYSSTATUS	R	0x114	0x4809 8114	0x4809 A114	0x480B 8114	0x480B A114
MCSPI_IRQSTATUS	RW	0x118	0x4809 8118	0x4809 A118	0x480B 8118	0x480B A118
MCSPI_IRQENABLE	RW	0x1C	0x4809 811C	0x4809 A11C	0x480B 811C	0x480B A11C
MCSPI_WAKEUPENABLE	RW	0x120	0x4809 8120	0x4809 A120	0x480B 8120	0x480B A120
MCSPI_SYST	RW	0x124	0x4809 8124	0x4809 A124	0x480B 8124	0x480B A124
MCSPI_MODULCTRL	RW	0x128	0x4809 8128	0x4809 A128	0x480B 8128	0x480B A128
MCSPI_CHxCONF (1)	RW	0x12C + (0x14 * x)	0x4809 812C + (0x14 * x)	0x4809 A12C + (0x14 * x)	0x480B 812C + (0x14 * x)	0x480B A12C + (0x14 * x)
MCSPI_CHxSTAT (1)	R	0x130 + (0x14 * x)	0x4809 8130 + (0x14 * x)	0x4809 A130 + (0x14 * x)	0x480B 8130 + (0x14 * x)	0x480B A130 + (0x14 * x)
MCSPI_CHxCTRL (1)	RW	0x134 + (0x14 * x)	0x4809 8134 + (0x14 * x)	0x4809 A134 + (0x14 * x)	0x480B 8134 + (0x14 * x)	0x480B A134 + (0x14 * x)
MCSPI_TXx (1)	RW	0x138 + (0x14 * x)	0x4809 8138 + (0x14 * x)	0x4809 A138 + (0x14 * x)	0x480B 8138 + (0x14 * x)	0x480B A138 + (0x14 * x)
MCSPI_RXx (1)	R	0x13C + (0x14 * x)	0x4809 813C + (0x14 * x)	0x4809 A13C + (0x14 * x)	0x480B 813C + (0x14 * x)	0x480B A13C + (0x14 * x)
MCSPI_XFERLEVEL	RW	0x17C	0x4809 817C	0x4809 A17C	0x480B 817C	0x480B A17C

(1) x = 0 to 3 for MCSPI1
x = 0 to 1 for MCSPI2
x = 0 for MCSPI3
x = 0 for MCSPI4

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23.4.6.2.2 MCSPI Register Description

Table 23-292 through Table 23-324 describe the individual MCSPI register bits.

Table 23-292. MCSPI_HL_REV

Address Offset	0x00		
Physical Address	See Table 23-291.	**Instance**	MCSPI1 MCSPI2 MCSPI3 MCSPI4
Description	IP Revision Identifier (X.Y.R) Used by software to track features, bugs, and compatibility		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP Revision	R	TI internal data

Table 23-293. Register Call Summary for Register MCSPI_HL_REV

Multichannel Serial Port Interface (MCSPI)

- MCSPI Register Summary: [0]

Table 23-294. MCSPI_HL_HWINFO

Address Offset	0x04		
Physical Address	See Table 23-291.	**Instance**	MCSPI1 MCSPI2 MCSPI3 MCSPI4
Description	Information about the IP module's hardware configuration, that is, typically the module's HDL generics (if any). Actual field format and encoding is up to the module's designer to decide.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD																								RETMODE	FFNBYTE						USEFIFO

Bits	Field Name	Description	Type	Reset
31:7	RSVD	Reserved These bits are initialized to 0, and writes to them are ignored.	R	0x0000000
6	RETMODE	Retention Mode generic parameter. This bit field indicates whether the retention mode is supported using the pin PIRFFRET. 0x0: Retention mode disabled 0x1: Retention mode enabled	R	RETMODE

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Bits	Field Name	Description	Type	Reset
5:1	FFNBYTE	FIFO number of byte generic parameter This register defines the value of FFNBYTE generic parameter, only MSB bits from 8 down to 4 are taken into account. Read 0x1: FIFO 16 bytes depth Read 0x2: FIFO 32 bytes depth Read 0x4: FIFO 64 bytes depth Read 0x8: FIFO 128 bytes depth Read 0x10: FIFO 256 bytes depth	R	0x04
0	USEFIFO	Use of a FIFO enable: This bit indicates if a FIFO is integrated within controller design with its management. Read 0x0: FIFO not implemented in design Read 0x1: FIFO and its management implemented in design with depth defined by FFNBYTE generic	R	0

Table 23-295. Register Call Summary for Register MCSPI_HL_HWINFO

Multichannel Serial Port Interface (MCSPI)

- MCSPI Register Summary: [0]

Table 23-296. MCSPI_HL_SYSCONFIG

Address Offset	0x10		
Physical Address	See Table 23-291.	**Instance**	MCSPI1 MCSPI2 MCSPI3 MCSPI4
Description	Clock management configuration		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD																												IDLEMODE		FREEEMU	SOFTRESET

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Bits	Field Name	Description	Type	Reset
31:4	RSVD		R	0x0000000
3:2	IDLEMODE	Configuration of the local target state management mode. By definition, target can handle read/write transaction as long as it is out of IDLE state. 0x0: Force-idle mode: local target's IDLE state follows (acknowledges) the system's idle requests unconditionally, that is, regardless of the IP module's internal requirements. Backup mode, for debug only. 0x1: No-idle mode: local target never enters IDLE state. Backup mode, for debug only. 0x2: Smart-idle mode: local target's IDLE state eventually follows (acknowledges) the system's idle requests, depending on the IP module's internal requirements. IP module shall not generate (IRQ- or DMA-request-related) wake-up events. 0x3: Smart-idle wake-up-capable mode: local target's IDLE state eventually follows (acknowledges) the system's idle requests, depending on the IP module's internal requirements. IP module may generate (IRQ- or DMA-request-related) wake-up events when in IDLE state. Mode is relevant only if the appropriate IP module "swake-up" output(s) is (are) implemented.	RW	0x2
1	FREEEMU	Sensitivity to emulation (debug) suspend input signal. 0x0: IP module is sensitive to emulation suspend. 0x1: IP module is not sensitive to emulation suspend.	RW	0
0	SOFTRESET	Software reset. (Optional) Write 0x0: No action Read 0x0: Reset done, no pending action Read 0x1: Reset (software or other) ongoing Write 0x1: Initiate software reset	RW	0

Table 23-297. Register Call Summary for Register MCSPI_HL_SYSCONFIG

Multichannel Serial Port Interface (MCSPI)

- MCSPI Register Summary: [0]

Table 23-298. MCSPI_REVISION

Address Offset	0x100		
Physical Address	See Table 23-291.	**Instance**	MCSPI1 MCSPI2 MCSPI3 MCSPI4
Description	This register contains the revision number.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP revision	R	TI Internal data

Table 23-299. Register Call Summary for Register MCSPI_REVISION

Multichannel Serial Port Interface (MCSPI)

- MCSPI Register Summary: [0]

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Table 23-300. MCSPI_SYSCONFIG

Address Offset	0x110		
Physical Address	See Table 23-291	**Instance**	MCSPI1 MCSPI2 MCSPI3 MCSPI4
Description	This register allows controlling various parameters of the OCP interface.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						CLOCKACTIVITY		RESERVED			SIDLEMODE		ENAWAKEUP	SOFTRESET	AUTOIDLE

Bits	Field Name	Description	Type	Reset
31:10	RESERVED	Reads returns 0	RW	0x000000
9:8	CLOCKACTIVITY	Clocks activity during wake-up mode period 0x0: OCP and functional clocks may be switched off. 0x1: OCP clock is maintained. Functional clock may be switched off. 0x2: Functional clock is maintained. OCP clock may be switched off. 0x3: OCP and functional clocks are maintained.	RW	0x0
7:5	RESERVED	Reads returns 0	RW	0x0
4:3	SIDLEMODE	Power management 0x0: If an idle request is detected, the McSPI acknowledges it unconditionally and goes in inactive mode. Interrupt, DMA requests and wake-up lines are unconditionally deasserted and the module wake-up capability is deactivated even if the MCSPI_SYSCONFIG[EnaWakeUp] bit is set. 0x1: If an idle request is detected, the request is ignored and the module does not switch to wake-up mode, and keeps on behaving normally. 0x2: If an idle request is detected, the module will switch to wake-up mode based on its internal activity, and the wake-up capability can be used if the bit MCSPI_SYSCONFIG[EnaWakeUp] is set. 0x3: Reserved - do not use.	RW	0x2
2	ENAWAKEUP	Wake-up feature control 0x0: Wake-up capability is disabled. 0x1: Wake-up capability is enabled.	RW	1
1	SOFTRESET	Software reset. During reads it always returns 0. 0x0: (write) Normal mode 0x1: (write) Set this bit to 1 to trigger a module reset. The bit is automatically reset by the hardware.	RW	0
0	AUTOIDLE	Internal OCP clock-gating strategy 0x0: OCP clock is free-running. 0x1: Automatic OCP clock gating strategy is applied, based on the OCP interface activity.	RW	1

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Table 23-301. Register Call Summary for Register MCSPI_SYSCONFIG

Multichannel Serial Port Interface (MCSPI)

- Normal Mode: [0]
- Idle Mode: [1]
- Wake-Up Event in Smart-Idle Mode: [2]
- Force-Idle Mode: [3] [4]
- MCSPI Global Initialization: [5]
- MCSPI Register Summary: [6]
- MCSPI Register Description: [7] [8]

Table 23-302. MCSPI_SYSSTATUS

Address Offset	0x114		
Physical Address	See Table 23-291.	**Instance**	MCSPI1 MCSPI2 MCSPI3 MCSPI4
Description	This register provides status information about the module excluding the interrupt status information.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															RESETDONE

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved for module specific status information. Read returns 0.	R	0x0000 0000
0	RESETDONE	Internal reset monitoring Read 0x0: Internal module reset is ongoing Read 0x1: Reset completed	R	0

Table 23-303. Register Call Summary for Register MCSPI_SYSSTATUS

Multichannel Serial Port Interface (MCSPI)

- MCSPI Global Initialization: [0]
- MCSPI Register Summary: [1]

Table 23-304. MCSPI_IRQSTATUS

Address Offset	0x118		
Physical Address	See Table 23-291.	**Instance**	MCSPI1 MCSPI2 MCSPI3 MCSPI4
Description	The interrupt status regroups all the status of the module internal events that can generate an interrupt.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														EOW	WKS	RESERVED	RX3_FULL	TX3_UNDERFLOW	TX3_EMPTY	RESERVED	RX2_FULL	TX2_UNDERFLOW	TX2_EMPTY	RESERVED	RX1_FULL	TX1_UNDERFLOW	TX1_EMPTY	RX0_OVERFLOW	RX0_FULL	TX0_UNDERFLOW	TX0_EMPTY

Bits	Field Name	Description	Type	Reset
31:18	RESERVED	Reads returns 0	RW	0x0000
17	EOW	End of word count event when a channel is enabled using the FIFO buffer and the channel had sent the number of SPI word defined by MCSPI_XFERLEVEL[WCNT]. Write 0x0: w:Event status bit unchanged Read 0x0: r: Event false Read 0x1: r: Event is pending Write 0x1: w:Event status bit is reset	RW W1toClr	0
16	WKS	Wake-up event in slave mode when an active control signal is detected on the SPIEN line programmed in the field MCSPI_CH0CONF[SPIENSLV] Read 0x0: r: Event false Write 0x0: w:Event status bit unchanged Write 0x1: w:Event status bit is reset Read 0x1: r: Event is pending	RW W1toClr	0
15	RESERVED	Reads returns 0	RW	0
14	RX3_FULL	Receiver register is full or almost full. Only when Channel 3 is enabled Read 0x0: r: Event false Write 0x0: w:Event status bit unchanged Write 0x1: w:Event status bit is reset Read 0x1: r: Event is pending	RW W1toClr	0
13	TX3_UNDERFLOW	Transmitter register underflow. Only when Channel 3 is enabled. The transmitter register is empty (not updated by host or DMA with new data) before its time slot assignment. Exception: No TX_underflow event when no data has been loaded into the transmitter register since channel has been enabled. Read 0x0: r: Event false Write 0x0: w:Event status bit unchanged Write 0x1: w:Event status bit is reset Read 0x1: r: Event is pending	RW W1toClr	0
12	TX3_EMPTY	Transmitter register is empty or almost empty. Note: Enabling the channel automatically rises this event. Read 0x0: r: Event false Write 0x0: w:Event status bit unchanged Write 0x1: w:Event status bit is reset Read 0x1: r: Event is pending	RW W1toClr	0
11	RESERVED	Reads returns 0.	RW	0

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Bits	Field Name	Description	Type	Reset
10	RX2_FULL	Receiver register full or almost full. Channel 2 Read 0x0: r: Event false Write 0x0: w:Event status bit unchanged Write 0x1: w:Event status bit is reset Read 0x1: r: Event is pending	RW W1toClr	0
9	TX2_UNDERFLOW	Transmitter register underflow. Channel 2 Read 0x0: r: Event false Write 0x0: w:Event status bit unchanged Write 0x1: w:Event status bit is reset Read 0x1: r: Event is pending	RW W1toClr	0
8	TX2_EMPTY	Transmitter register empty or almost empty. Channel 2 Read 0x0: r: Event false Write 0x0: w:Event status bit unchanged Write 0x1: w:Event status bit is reset Read 0x1: r: Event is pending	RW W1toClr	0
7	RESERVED	Reads returns 0	RW	0
6	RX1_FULL	Receiver register full or almost full. Channel 1 Read 0x0: r: Event false Write 0x0: w:Event status bit unchanged Write 0x1: w:Event status bit is reset Read 0x1: r: Event is pending	RW W1toClr	0
5	TX1_UNDERFLOW	Transmitter register underflow. Channel 1 Read 0x0: r: Event false Write 0x0: w:Event status bit unchanged Write 0x1: w:Event status bit is reset Read 0x1: r: Event is pending	RW W1toClr	0
4	TX1_EMPTY	Transmitter register empty or almost empty. Channel 1 Read 0x0: r: Event false Write 0x0: w:Event status bit unchanged Write 0x1: w:Event status bit is reset Read 0x1: r: Event is pending	RW W1toClr	0
3	RX0_OVERFLOW	Receiver register overflow (slave mode only). Channel 0 Read 0x0: r: Event false Write 0x0: w:Event status bit unchanged Write 0x1: w:Event status bit is reset Read 0x1: r: Event is pending	RW W1toClr	0
2	RX0_FULL	Receiver register full or almost full. Channel 0 Read 0x0: r: Event false Write 0x0: w:Event status bit unchanged Write 0x1: w:Event status bit is reset Read 0x1: r: Event is pending	RW W1toClr	0
1	TX0_UNDERFLOW	Transmitter register underflow. Channel 0 Read 0x0: r: Event false Write 0x0: w:Event status bit unchanged Write 0x1: w:Event status bit is reset Read 0x1: r: Event is pending	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
0	TX0_EMPTY	Transmitter register empty or almost empty. Channel 0 Read 0x0: r: Event false Write 0x0: w:Event status bit unchanged Write 0x1: w:Event status bit is reset Read 0x1: r: Event is pending	RW W1toClr	0

Table 23-305. Register Call Summary for Register MCSPI_IRQSTATUS

Multichannel Serial Port Interface (MCSPI)

- Master Transmit-and-Receive Mode (Full Duplex): [0]
- Master Transmit-Only Mode (Half Duplex): [1]
- Master Receive-Only Mode (Half Duplex): [2] [3] [4] [5]
- Force mcspim_csx Mode: [6]
- Turbo Mode: [7]
- Buffer Almost Full: [8] [9]
- Buffer Almost Empty: [10] [11]
- End of Transfer Management: [12]
- Interrupts: [13]
- TXx_EMPTY: [14] [15]
- TXx_UNDERFLOW: [16]
- RXx_ FULL: [17]
- End Of Word Count: [18] [19]
- Interrupt Events in Slave Mode: [20]
- TXx_EMPTY: [21]
- TXx_UNDERFLOW: [22]
- RXx_FULL: [23]
- RX0_OVERFLOW: [24]
- End Of Word Count: [25] [26]
- Interrupt-Driven Operation: [27] [28]
- Polling: [29] [30]
- Transitions From Smart-Idle Mode to Normal Mode: [31] [32]
- Force-Idle Mode: [33]
- MCSPI Operational Modes: [34] [35] [36] [37]
- Receive-Only Procedure With Word Count- Polling Method: [38]
- Transmit-Only Procedure With and Without Word Count- Polling Method: [39]
- Transmit-Only Procedure With and Without Word Count- Interrupt Method: [40]
- Transmit and Receive Procedure with Word Count- Polling Method: [41]
- Transmit and Receive Procedure with Word Count - Interrupt Method: [42]
- MCSPI Register Summary: [43]
- MCSPI Register Description: [44] [45] [46]

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Table 23-306. MCSPI_IRQENABLE

Address Offset	0x11C		
Physical Address	See Table 23-291.	**Instance**	MCSPI1 MCSPI2 MCSPI3 MCSPI4
Description	This register allows enabling/disabling of the module internal sources of interrupt, on an event-by-event basis.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														EOW_ENABLE	WKE	RESERVED	RX3_FULL_ENABLE	TX3_UNDERFLOW_ENABLE	TX3_EMPTY_ENABLE	RESERVED	RX2_FULL_ENABLE	TX2_UNDERFLOW_ENABLE	TX2_EMPTY_ENABLE	RESERVED	RX1_FULL_ENABLE	TX1_UNDERFLOW_ENABLE	TX1_EMPTY_ENABLE	RX0_OVERFLOW_ENABLE	RX0_FULL_ENABLE	TX0_UNDERFLOW_ENABLE	TX0_EMPTY_ENABLE

Bits	Field Name	Description	Type	Reset
31:18	RESERVED	Reads return 0.	RW	0x0000
17	EOW_ENABLE	End of Word count Interrupt Enable. 0x0: Interrupt disabled 0x1: Interrupt enabled	RW	0
16	WKE	Wake-up event interrupt enable in slave mode when an active control signal is detected on the SPIEN line programmed in the MCSPI_CH0CONF[SPIENSLV] bit 0x0: Interrupt disabled 0x1: Interrupt enabled	RW	0
15	RESERVED	Reads returns 0.	RW	0
14	RX3_FULL_ENABLE	Receiver register Full Interrupt Enable. Channel 3 0x0: Interrupt disabled 0x1: Interrupt enabled	RW	0
13	TX3_UNDERFLOW_ENABLE	Transmitter register Underflow Interrupt Enable. Channel 3 0x0: Interrupt disabled 0x1: Interrupt enabled	RW	0
12	TX3_EMPTY_ENABLE	Transmitter register Empty Interrupt Enable. Channel 3 0x0: Interrupt disabled 0x1: Interrupt enabled	RW	0
11	RESERVED	Reads return 0.	RW	0
10	RX2_FULL_ENABLE	Receiver register Full Interrupt Enable. Channel 2 0x0: Interrupt disabled 0x1: Interrupt enabled	RW	0
9	TX2_UNDERFLOW_ENABLE	Transmitter register Underflow Interrupt Enable. Channel 2 0x0: Interrupt disabled 0x1: Interrupt enabled	RW	0

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Bits	Field Name	Description	Type	Reset
8	TX2_EMPTY_ENABLE	Transmitter register Empty Interrupt Enable. Channel 2 0x0: Interrupt disabled 0x1: Interrupt enabled	RW	0
7	RESERVED	Reads return 0.	RW	0
6	RX1_FULL_ENABLE	Receiver register Full Interrupt Enable. Channel 1 0x0: Interrupt disabled 0x1: Interrupt enabled	RW	0
5	TX1_UNDERFLOW_ENABLE	Transmitter register Underflow Interrupt Enable. Channel 1 0x0: Interrupt disabled 0x1: Interrupt enabled	RW	0
4	TX1_EMPTY_ENABLE	Transmitter register Empty Interrupt Enable. Channel 1 0x0: Interrupt disabled 0x1: Interrupt enabled	RW	0
3	RX0_OVERFLOW_ENABLE	Receiver register Overflow Interrupt Enable. Channel 0 0x0: Interrupt disabled 0x1: Interrupt enabled	RW	0
2	RX0_FULL_ENABLE	Receiver register Full Interrupt Enable. Channel 0 0x0: Interrupt disabled 0x1: Interrupt enabled	RW	0
1	TX0_UNDERFLOW_ENABLE	Transmitter register Underflow Interrupt Enable. Channel 0 0x0: Interrupt disabled 0x1: Interrupt enabled	RW	0
0	TX0_EMPTY_ENABLE	Transmitter register Empty Interrupt Enable. Channel 0 0x0: Interrupt disabled 0x1: Interrupt enabled	RW	0

Table 23-307. Register Call Summary for Register MCSPI_IRQENABLE

Multichannel Serial Port Interface (MCSPI)

- Interrupts: [0]
- Interrupt-Driven Operation: [1]
- Polling: [2]
- Transitions From Smart-Idle Mode to Normal Mode: [3] [4]
- MCSPI Operational Modes: [5] [6]
- Transmit-Only Procedure With and Without Word Count- Interrupt Method: [7] [8] [9]
- Transmit and Receive Procedure with Word Count - Interrupt Method: [10] [11] [12] [13] [14]
- MCSPI Register Summary: [15]

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Table 23-308. MCSPI_WAKEUPENABLE

Address Offset	0x120		
Physical Address	See Table 23-291.	**Instance**	MCSPI1 MCSPI2 MCSPI3 MCSPI4
Description	The wake-up enable register allows enabling and disabling of the module internal sources of wakeup on event-by-event basis.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															WKEN

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reads returns 0.	RW	0x0000 0000
0	WKEN	Wake-up functionality in slave mode when an active control signal is detected on the SPIEN line programmed in the MCSPI_CH0CONF[SPIENSLV] bit 0x0: The event is not allowed to wake-up the system, even if the global control bit MCSPI_SYSCONF[EnaWakeUp] is set. 0x1: The event is allowed to wake-up the system if the global control bit MCSPI_SYSCONF[EnaWakeUp] is set.	RW	0

Table 23-309. Register Call Summary for Register MCSPI_WAKEUPENABLE

Multichannel Serial Port Interface (MCSPI)

- Wake-Up Event in Smart-Idle Mode: [0]
- Transitions From Smart-Idle Mode to Normal Mode: [1]
- Force-Idle Mode: [2]
- MCSPI Register Summary: [3]

Table 23-310. MCSPI_SYST

Address Offset	0x124		
Physical Address	See Table 23-291.	**Instance**	MCSPI1 MCSPI2 MCSPI3 MCSPI4
Description	This register is used to check the correctness of the system interconnect either internally to peripheral bus, or externally to device I/O pads, when the module is configured in system test (SYSTEST) mode.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				SSB	SPIENDIR	SPIDATDIR1	SPIDATDIR0	WAKD	SPICLK	SPIDAT_1	SPIDAT_0	SPIEN_3	SPIEN_2	SPIEN_1	SPIEN_0

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Bits	Field Name	Description	Type	Reset
31:12	RESERVED	Reads returns 0.	RW	0x00000
11	SSB	Set status bit 0x0: No action. Writing 0 does not clear already set status bits. This bit must be cleared before trying to clear a status bit of the <MCSPI_IRQSTATUS> register. 0x1: Force to 1 all status bits of MCSPI_IRQSTATUS register. Writing 1 into this bit sets to 1 all status bits in the <MCSPI_IRQSTATUS> register.	RW	0
10	SPIENDIR	Set the direction of the SPIEN[3:0] lines and SPICLK line. 0x0: Output (as in master mode) 0x1: Input (as in slave mode)	RW	0
9	SPIDATDIR1	Set the direction of the SPIDAT[1]. 0x0: Output 0x1: Input	RW	0
8	SPIDATDIR0	Set the direction of the SPIDAT[0]. 0x0: Output 0x1: Input	RW	0
7	WAKD	SWAKEUP output (signal data value of internal signal to system). The signal is driven high or low according to the value written into this register bit. 0x0: The pin is driven low. 0x1: The pin is driven high.	RW	0
6	SPICLK	SPICLK line (signal data value) If MCSPI_SYST[SPIENDIR] = 1 (input mode direction), this bit returns the value on the CLKSPI line (high or low), and a write into this bit has no effect. If MCSPI_SYST[SPIENDIR] = 0 (output mode direction), the CLKSPI line is driven high or low according to the value written into this register.	RW	0
5	SPIDAT_1	SPIDAT[1] line (signal data value) If MCSPI_SYST[SPIDATDIR1] = 0 (output mode direction), the SPIDAT[1] line is driven high or low according to the value written into this register. If MCSPI_SYST[SPIDATDIR1] = 1 (input mode direction), this bit returns the value on the SPIDAT[1] line (high or low), and a write into this bit has no effect.	RW	0
4	SPIDAT_0	SPIDAT[0] line (signal data value) If MCSPI_SYST[SPIDATDIR0] = 0 (output mode direction), the SPIDAT[0] line is driven high or low according to the value written into this register. If MCSPI_SYST[SPIDATDIR0] = 1 (input mode direction), this bit returns the value on the SPIDAT[0] line (high or low), and a write into this bit has no effect.	RW	0
3	SPIEN_3	SPIEN[3] line (signal data value) If MCSPI_SYST[SPIENDIR] = 0 (output mode direction), the SPIENT[3] line is driven high or low according to the value written into this register. If MCSPI_SYST[SPIENDIR] = 1 (input mode direction), this bit returns the value on the SPIEN[3] line (high or low), and a write into this bit has no effect.	RW	0
2	SPIEN_2	SPIEN[2] line (signal data value) If MCSPI_SYST[SPIENDIR] = 0 (output mode direction), the SPIENT[2] line is driven high or low according to the value written into this register. If MCSPI_SYST[SPIENDIR] = 1 (input mode direction), this bit returns the value on the SPIEN[2] line (high or low), and a write into this bit has no effect.	RW	0

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Bits	Field Name	Description	Type	Reset
1	SPIEN_1	SPIEN[1] line (signal data value) If MCSPI_SYST[SPIENDIR] = 0 (output mode direction), the SPIENT[1] line is driven high or low according to the value written into this register. If MCSPI_SYST[SPIENDIR] = 1 (input mode direction), this bit returns the value on the SPIEN[1] line (high or low), and a write into this bit has no effect.	RW	0
0	SPIEN_0	SPIEN[0] line (signal data value) If MCSPI_SYST[SPIENDIR] = 0 (output mode direction), the SPIENT[0] line is driven high or low according to the value written into this register. If MCSPI_SYST[SPIENDIR] = 1 (input mode direction), this bit returns the value on the SPIEN[0] line (high or low), and a write into this bit has no effect.	RW	0

Table 23-311. Register Call Summary for Register MCSPI_SYST

Multichannel Serial Port Interface (MCSPI)

- MCSPI Register Summary: [0]
- MCSPI Register Description: [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14]

Table 23-312. MCSPI_MODULCTRL

Address Offset	0x128		
Physical Address	See Table 23-291.	**Instance**	MCSPI1 MCSPI2 MCSPI3 MCSPI4
Description	This register is dedicated to the configuration of the serial port interface.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							FDAA	MOA	INITDLY			SYSTEM_TEST	MS	PIN34	SINGLE

Bits	Field Name	Description	Type	Reset
31:9	RESERVED	Reads returns 0.	RW	0x000000
8	FDAA	FIFO DMA address 256-bit aligned This register is used when a FIFO is managed by the module and DMA connected to the controller provides only 256-bit aligned address. If this bit is set the enabled channel which uses the FIFO has its data managed through MCSPI_DAFTX and MCSPI_DAFRX registers instead of MCSPI_TX(i) and MCSPI_RX(i) registers. 0x0: FIFO data managed by MCSPI_TX(i) and MCSPI_RX(i) registers. 0x1: FIFO data managed by MCSPI_DAFTX and MCSPI_DAFRX registers.	RW	0
7	MOA	Multiple word OCP access: This register can only be used when a channel is enabled using a FIFO. It allows the system to perform multiple SPI word access for a single 32-bit OCP word access. This is possible for WL < 16. 0x0: Multiple word access disabled 0x1: Multiple word access enabled with FIFO	RW	0

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Bits	Field Name	Description	Type	Reset
6:4	INITDLY	Initial SPI delay for first transfer: This register is an option only available in SINGLE master mode. The controller waits for a delay to transmit the first SPI word after channel enabled and corresponding TX register filled. This delay is based on SPI output frequency clock. No clock output provided to the boundary and chip select is not active in 4-pin mode within this period. 0x0: No delay for first spi transfer. 0x1: The controller wait 4 SPI bus clock 0x2: The controller wait 8 SPI bus clock 0x3: The controller wait 16 SPI bus clock 0x4: The controller wait 32 SPI bus clock	RW	0x0
3	SYSTEM_TEST	Enables the system test mode 0x0: Functional mode 0x1: System test mode (SYSTEST)	RW	0
2	MS	Master/slave 0x0: Master - The module generates the SPICLK and SPIEN[3:0]. 0x1: Slave - The module receives the SPICLK and SPIEN[3:0].	RW	1
1	PIN34	Pin mode selection: This register is used to configure the SPI pin mode, in master or slave mode. If asserted the controller only use SIMO, SOMI, and SPICLK clock pin for SPI transfers. 0x0: SPIEN is used as a chip-select. 0x1: SPIEN is not used. In this mode all related options to chip-select have no meaning.	RW	0
0	SINGLE	Single channel/Multi Channel (master mode only) 0x0: More than one channel will be used in master mode. 0x1: Only one channel will be used in master mode. This bit must be set in Force SPIEN mode.	RW	0

Table 23-313. Register Call Summary for Register MCSPI_MODULCTRL

Multichannel Serial Port Interface (MCSPI)

- Single-Channel Master Mode: [0] [1]
- Force mcspim_csx Mode: [2] [3]
- Chip-Select Timing Control: [4]
- Slave Mode: [5]
- MCSPI Operational Modes: [6] [7] [8]
- MCSPI Register Summary: [9]
- MCSPI Register Description: [10] [11]

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Table 23-314. MCSPI_CHxCONF

Address Offset	0x12C + (0x14 * x)	**Index**	x= 0 to 3 for MCSPI1. x= 0 to 1 for MCSPI2 . x= 0 for MCSPI4 and MCSPI3.
Physical Address	See Table 23-291.	**Instance**	MCSPI1 MCSPI2 MCSPI3 MCSPI4
Description	This register is dedicated to the configuration of the channel 0		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		CLKG	FFER	FFEW	TCS0		SBPOL	SBE	SPIENSLV		FORCE	TURBO	IS	DPE1	DPE0	DMAR	DMAW	TRM		WL				EPOL	CLKD					POL	PHA

Bits	Field Name	Description	Type	Reset
31:30	RESERVED	Read returns 0.	R	0x0
29	CLKG	Clock divider granularity This register defines the granularity of channel clock divider: power of 2 or one clock cycle granularity. When this bit is set the register MCSPI_CHCTRL[EXTCLK] must be configured to reach a maximum of 4096 clock divider ratio. Then the clock divider ratio is a concatenation of MCSPI_CHCONF[CLKD] and MCSPI_CHCTRL[EXTCLK] values 0x0: Clock granularity of power of 2 0x1: One clock cycle granularity	RW	0
28	FFER	FIFO enabled for receive: Only one channel can have this bit field set. 0x0: The buffer is not used to receive data. 0x1: The buffer is used to receive data.	RW	0
27	FFEW	FIFO enabled for transmit: Only one channel can have this bit field set. 0x0: The buffer is not used to transmit data. 0x1: The buffer is used to transmit data.	RW	0
26:25	TCS0	Chip-select time control This 2-bit field defines the number of interface clock cycles between CS toggling and first or last edge of SPI clock. 0x0: 0.5 clock cycle 0x1: 1.5 clock cycles 0x2: 2.5 clock cycles 0x3: 3.5 clock cycles	RW	0x0
24	SBPOL	Start-bit polarity 0x0: Start-bit polarity is held to 0 during SPI transfer. 0x1: Start-bit polarity is held to 1 during SPI transfer.	RW	0
23	SBE	Start-bit enable for SPI transfer 0x0: Default SPI transfer length as specified by WL bit field 0x1: Start bit D/CX added before SPI transfer polarity is defined by MCSPI_CH0CONF[SBPOL]	RW	0

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Bits	Field Name	Description	Type	Reset
22:21	SPIENSLV	Channel 0 only and slave mode only: SPI slave select signal detection. Reserved bits for other cases. 0x0: Detection enabled only on SPIEN[0] 0x1: Detection enabled only on SPIEN[1] 0x2: Detection enabled only on SPIEN[2] 0x3: Detection enabled only on SPIEN[3]	RW	0x0
20	FORCE	Manual SPIEN assertion to keep SPIEN active between SPI words (single channel master mode only). 0x0: Writing 0 into this bit drives low the SPIEN line when MCSPI_CHCONF(i)[EPOL]=0, and drives it high when MCSPI_CHCONF(i)[EPOL]=1. 0x1: Writing 1 into this bit drives high the SPIEN line when MCSPI_CHCONF(i)[EPOL]=0, and drives it low when MCSPI_CHCONF(i)[EPOL]=1.	RW	0
19	TURBO	Turbo mode 0x0: Turbo is deactivated (recommended for single SPI word transfer). 0x1: Turbo is activated to maximize the throughput for multiple SPI words transfer.	RW	0
18	IS	Input Select 0x0: Data line 0 (SPIDAT[0]) selected for reception 0x1: Data line 1 (SPIDAT[1]) selected for reception	RW	1
17	DPE1	Transmission enable for data line 1 (SPIDATAGZEN[1]) 0x0: Data line 1 (SPIDAT[1]) selected for transmission 0x1: No transmission on Data Line1 (SPIDAT[1])	RW	1
16	DPE0	Transmission Enable for data line 0 (SPIDATAGZEN[0]) 0x0: Data Line0 (SPIDAT[0]) selected for transmission 0x1: No transmission on data line 0 (SPIDAT[0])	RW	0
15	DMAR	DMA read request The DMA read request line is asserted when the channel is enabled and a new data is available in the receive register of the channel. The DMA read request line is deasserted on read completion of the receive register of the channel. 0x0: DMA read request disabled 0x1: DMA read request enabled	RW	0
14	DMAW	DMA write request. The DMA write request line is asserted when The channel is enabled and the transmitter register of the channel is empty. The DMA write request line is deasserted on load completion of the transmitter register of the channel. 0x0: DMA write request disabled 0x1: DMA write request enabled	RW	0
13:12	TRM	Transmit/receive modes 0x0: Transmit-and-receive mode 0x1: Receive-only mode 0x2: Transmit-only mode 0x3: Reserved	RW	0x0

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Bits	Field Name	Description	Type	Reset
11:7	WL	SPI word length 0x0: Reserved 0x1: Reserved 0x2: Reserved 0x3: The SPI word is 4 bits long 0x4: The SPI word is 5 bits long 0x5: The SPI word is 6 bits long 0x6: The SPI word is 7 bits long 0x7: The SPI word is 8 bits long 0x8: The SPI word is 9 bits long 0x9: The SPI word is 10 bits long 0xA: The SPI word is 11 bits long 0xB: The SPI word is 12 bits long 0xC: The SPI word is 13 bits long 0xD: The SPI word is 14 bits long 0xE: The SPI word is 15 bits long 0xF: The SPI word is 16 bits long 0x10: The SPI word is 17 bits long 0x11: The SPI word is 18 bits long 0x12: The SPI word is 19 bits long 0x13: The SPI word is 20 bits long 0x14: The SPI word is 21 bits long 0x15: The SPI word is 22 bits long 0x16: The SPI word is 23 bits long 0x17: The SPI word is 24 bits long 0x18: The SPI word is 25 bits long 0x19: The SPI word is 26 bits long 0x1A: The SPI word is 27 bits long 0x1B: The SPI word is 28 bits long 0x1C: The SPI word is 29 bits long 0x1D: The SPI word is 30 bits long 0x1E: The SPI word is 31 bits long 0x1F: The SPI word is 32 bits long	RW	0x00
6	EPOL	SPIEN polarity 0x0: SPIEN is held high during the ACTIVE state. 0x1: SPIEN is held low during the ACTIVE state.	RW	0

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Bits	Field Name	Description	Type	Reset
5:2	CLKD	Frequency divider for SPICLK (only when the module is a Master SPI device). A programmable clock divider divides the SPI reference clock (CLKSPIREF) with a 4-bit value, and results in a new clock SPICLK available to shift-in and shift-out data. By default the clock divider ratio has a power of 2 granularity when MCSPI_CHCONF[CLKG] is cleared. Otherwise this register is the 4-LSB bit of a 12-bit register concatenated with clock divider extension MCSPI_CHCTRL[EXTCLK] register. The value description below defines the clock ratio when MCSPI_CHCONF[CLKG] is set to 0. 0x0: 1 0x1: 2 0x2: 4 0x3: 8 0x4: 16 0x5: 32 0x6: 64 0x7: 128 0x8: 256 0x9: 512 0xA: 1024 0xB: 2048 0xC: 4096 0xD: 8192 0xE: 16384 0xF: 32768	RW	0x0
1	POL	SPICLK polarity 0x0: SPICLK is held high during the ACTIVE state 0x1: SPICLK is held low during the ACTIVE state	RW	0
0	PHA	SPICLK phase 0x0: Data are latched on odd-numbered edges of SPICLK. 0x1: Data are latched on even-numbered edges of SPICLK.	RW	0

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Table 23-315. Register Call Summary for Register MCSPI_CHxCONF

Multichannel Serial Port Interface (MCSPI)

- Multichannel SPI Protocol and Data Format: [0] [1] [2] [3] [4] [5] [6] [7]
- Transfer Format: [8]
- SPI Interface in Slave Mode: [9]
- Master Transmit-and-Receive Mode (Full Duplex): [10]
- Master Transmit-Only Mode (Half Duplex): [11]
- Master Receive-Only Mode (Half Duplex): [12]
- Single-Channel Master Mode: [13]
- Force mcspim_csx Mode: [14] [15] [16] [17] [18] [19] [20] [21] [22] [23]
- Turbo Mode: [24]
- Start Bit Mode: [25] [26] [27] [28]
- Chip-Select Timing Control: [29]
- Programmable SPI Clock (mcspim_clk): [30]
- Clock Ratio Granularity: [31] [32] [33] [34] [35]
- Dedicated Resources: [36] [37] [38] [39] [40] [41]
- Slave Transmit-and-Receive Mode: [42]
- Slave Transmit-Only Mode: [43]
- Slave Receive-Only Mode: [44]
- FIFO Buffer Management: [45] [46] [47]
- Buffer Almost Full: [48] [49]
- Buffer Almost Empty: [50] [51]
- TXx_EMPTY: [52]
- RXx_ FULL: [53]
- TXx_EMPTY: [54]
- RXx_FULL: [55]
- DMA Requests: [56] [57]
- Wake-Up Event in Smart-Idle Mode: [58]
- MCSPI Operational Modes: [59] [60] [61] [62] [63] [64] [65] [66] [67] [68] [69] [70] [71] [72] [73] [74]
- MCSPI Register Summary: [75]

Table 23-316. MCSPI_CHxSTAT

Address Offset	0x130 + (0x14 * x)	**Index**	x= 0 to 3 for MCSPI1. x= 0 to 1 for MCSPI2 . x= 0 for MCSPI4 and MCSPI3.
Physical Address	See Table 23-291.	**Instance**	MCSPI1 MCSPI2 MCSPI3 MCSPI4
Description	This register provides status information about transmitter and receiver registers of channel 0.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RXFFF	RXFFE	TXFFF	TXFFE	EOT	TXS	RXS

Bits	Field Name	Description	Type	Reset
31:7	RESERVED	Read returns 0.	R	0x0000000
6	RXFFF	Channel "i" FIFO receive buffer full status Read 0x0: FIFO receive buffer is not full Read 0x1: FIFO receive buffer is full	R	0
5	RXFFE	Channel "i" FIFO receive buffer empty status Read 0x0: FIFO receive buffer is not empty Read 0x1: FIFO receive buffer is empty	R	0

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Bits	Field Name	Description	Type	Reset
4	TXFFF	Channel "i" FIFO transmit buffer full status Read 0x0: FIFO transmit buffer is not full Read 0x1: FIFO transmit buffer is full	R	0
3	TXFFE	Channel "i" FIFO transmit buffer empty status Read 0x0: FIFO transmit buffer is not empty Read 0x1: FIFO transmit buffer is empty	R	0
2	EOT	Channel "i" end of transfer status. The definitions of beginning and end of transfer vary with master versus slave and the transfer format (transmit/receive modes, turbo mode). See dedicated chapters for details. Read 0x0: This flag is automatically cleared when the shift register is loaded with the data from the transmitter register (beginning of transfer). Read 0x1: This flag is automatically set to one at the end of an SPI transfer.	R	0
1	TXS	Channel "i" transmitter register status Read 0x0: Register is full. Read 0x1: Register is empty.	R	0
0	RXS	Channel "i" receiver register status Read 0x0: Register is empty. Read 0x1: Register is full.	R	0

Table 23-317. Register Call Summary for Register MCSPI_CHxSTAT

Multichannel Serial Port Interface (MCSPI)

- Master Transmit-and-Receive Mode (Full Duplex): [0] [1] [2]
- Master Transmit-Only Mode (Half Duplex): [3]
- Master Receive-Only Mode (Half Duplex): [4]
- Programming Tips When Switching to Another Channel: [5]
- Force mcspim_csx Mode: [6] [7] [8]
- Turbo Mode: [9]
- Dedicated Resources: [10] [11]
- Slave Transmit-and-Receive Mode: [12]
- Slave Transmit-Only Mode: [13]
- Slave Receive-Only Mode: [14]
- End of Transfer Management: [15]
- MCSPI Operational Modes: [16] [17]
- Transmit-Only Procedure With and Without Word Count- Polling Method: [18] [19]
- Transmit-Only Procedure With and Without Word Count- Interrupt Method: [20] [21]
- Transmit and Receive Procedure without Word Count- Polling Method: [22] [23]
- MCSPI Register Summary: [24]

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Table 23-318. MCSPI_CHxCTRL

Address Offset	0x134 + (0x14 * x)	**Index**	x= 0 to 3 for MCSPI1. x= 0 to 1 for MCSPI2 . x= 0 for MCSPI4 and MCSPI3.
Physical Address	See Table 23-291.	**Instance**	MCSPI1 MCSPI2 MCSPI3 MCSPI4
Description	This register is dedicated to enable channel 0.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																EXTCLK								RESERVED							EN

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Read returns 0.	RW	0x0000
15:8	EXTCLK	Clock ratio extension: This register is used to concatenate with MCSPI_CHCONF[CLKD] register for clock ratio only when granularity is one clock cycle (MCSPI_CHCONF[CLKG] set to 1). Then the maximum value reached is 4096 clock divider ratio. 0x0: Clock ratio is CLKD + 1. 0x1: Clock ratio is CLKD + 1 + 16. 0xFF: Clock ratio is CLKD + 1 + 4080.	RW	0x00
7:1	RESERVED	Read returns 0.	RW	0x00
0	EN	Channel enable 0x0: Channel "i" is not active. 0x1: Channel "i" is active.	RW	0

Table 23-319. Register Call Summary for Register MCSPI_CHxCTRL

Multichannel Serial Port Interface (MCSPI)

- Master Transmit-and-Receive Mode (Full Duplex): [0]
- Force mcspim_csx Mode: [1] [2]
- Clock Ratio Granularity: [3]
- Dedicated Resources: [4] [5]
- MCSPI Operational Modes: [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16]
- Receive-Only Procedure With Word Count- Polling Method: [17] [18]
- Transmit-Only Procedure With and Without Word Count- Polling Method: [19] [20]
- Transmit-Only Procedure With and Without Word Count- Interrupt Method: [21] [22]
- Transmit and Receive Procedure with Word Count- Polling Method: [23] [24]
- Transmit and Receive Procedure with Word Count - Interrupt Method: [25] [26]
- Transmit and Receive Procedure without Word Count- Polling Method: [27] [28]
- MCSPI Register Summary: [29]

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Table 23-320. MCSPI_TXx

Address Offset	0x138 + (0x14 * x)	**Index**	x= 0 to 3 for MCSPI1. x= 0 to 1 for MCSPI2 . x= 0 for MCSPI4 and MCSPI3.
Physical Address	See Table 23-291.	**Instance**	MCSPI1 MCSPI2 MCSPI3 MCSPI4
Description	This register contains a single SPI word to transmit on the serial link, what ever SPI word length is.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDATA																															

Bits	Field Name	Description	Type	Reset
31:0	TDATA	Channel 0 data to transmit	RW	0x0000 0000

Table 23-321. Register Call Summary for Register MCSPI_TXx

Multichannel Serial Port Interface (MCSPI)

- Master Transmit-and-Receive Mode (Full Duplex): [0] [1] [2] [3]
- Master Transmit-Only Mode (Half Duplex): [4]
- Master Receive-Only Mode (Half Duplex): [5] [6] [7] [8] [9]
- Force mcspim_csx Mode: [10]
- Dedicated Resources: [11] [12] [13] [14] [15]
- Slave Transmit-and-Receive Mode: [16] [17]
- Slave Receive-Only Mode: [18] [19] [20]
- Interrupt Events in Master Mode: [21]
- TXx_EMPTY: [22] [23] [24]
- TXx_UNDERFLOW: [25] [26] [27]
- Interrupt Events in Slave Mode: [28]
- TXx_EMPTY: [29] [30] [31]
- TXx_UNDERFLOW: [32] [33]
- Interrupt-Driven Operation: [34]
- Polling: [35]
- DMA Requests: [36] [37]
- Common Transfer Procedures with FIFO- Polling Method: [38]
- MCSPI Register Summary: [39]

Table 23-322. MCSPI_RXx

Address Offset	0x13C + (0x14 * x)	**Index**	x= 0 to 3 for MCSPI1. x= 0 to 1 for MCSPI2 . x= 0 for MCSPI4 and MCSPI3.
Physical Address	See Table 23-291.	**Instance**	MCSPI1 MCSPI2 MCSPI3 MCSPI4
Description	This register contains a single SPI word received through the serial link, what ever SPI word length is.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RDATA																															

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Bits	Field Name	Description	Type	Reset
31:0	RDATA	Channel 0 received data	R	0x0000 0000

Table 23-323. Register Call Summary for Register MCSPI_RXx

Multichannel Serial Port Interface (MCSPI)

- Master Transmit-and-Receive Mode (Full Duplex): [0] [1]
- Master Transmit-Only Mode (Half Duplex): [2] [3] [4]
- Master Receive-Only Mode (Half Duplex): [5] [6]
- Force mcspim_csx Mode: [7] [8]
- Turbo Mode: [9] [10]
- Dedicated Resources: [11] [12] [13]
- Slave Transmit-and-Receive Mode: [14]
- Slave Transmit-Only Mode: [15] [16]
- End of Transfer Management: [17]
- Interrupt Events in Master Mode: [18]
- RXx_ FULL: [19] [20] [21]
- Interrupt Events in Slave Mode: [22]
- RXx_FULL: [23] [24] [25]
- RX0_OVERFLOW: [26] [27]
- Interrupt-Driven Operation: [28]
- Polling: [29]
- DMA Requests: [30]
- Wake-Up Event in Smart-Idle Mode: [31]
- MCSPI Operational Modes: [32] [33]
- Receive-Only Procedure With Word Count- Polling Method: [34]
- Transmit and Receive Procedure with Word Count- Polling Method: [35]
- Transmit and Receive Procedure with Word Count - Interrupt Method: [36]
- Transmit and Receive Procedure without Word Count- Polling Method: [37]
- MCSPI Register Summary: [38]

Table 23-324. MCSPI_XFERLEVEL

Address Offset	0x17C		
Physical Address	See Table 23-291.	**Instance**	MCSPI1 MCSPI2 MCSPI3 MCSPI4
Description	This register provides transfer levels needed while using FIFO buffer during transfer.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WCNT																AFL								AEL							

Bits	Field Name	Description	Type	Reset
31:16	WCNT	SPI word counter. This register holds the programmable value of number of SPI word to be transferred on channel which is using the FIFO buffer. When transfer had started, a read back in this register returns the current SPI word transfer index. 0x0: Counter not used 0x1: One word 0xFFFE: 65534 SPI word 0xFFFF: 65535 SPI word	RW	0x0000

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Bits	Field Name	Description	Type	Reset
15:8	AFL	Buffer almost full This register holds the programmable almost full level value used to determine almost full buffer condition. If the user wants an interrupt or a DMA read request to be issued during a receive operation when the data buffer holds at least n bytes, then the buffer MCSPI_MODULCTRL[AFL] must be set with n–1.The size of this register is defined by the generic parameter FFNBYTE. 0x0: 1 byte 0x1: 2 bytes 0xFE: 255bytes 0xFF: 256bytes	RW	0x00
7:0	AEL	Buffer almost empty. This register holds the programmable almost empty level value used to determine almost empty buffer condition. If the user wants an interrupt or a DMA write request to be issued during a transmit operation when the data buffer is able to receive n bytes, then the buffer MCSPI_MODULCTRL[AEL] must be set with – 1. 0x0: 1 byte 0x1: 2 bytes 0xFE: 255 bytes 0xFF: 256bytes	RW	0x00

Table 23-325. Register Call Summary for Register MCSPI_XFERLEVEL

Multichannel Serial Port Interface (MCSPI)

- FIFO Buffer Management: [0] [1]
- Buffer Almost Full: [2]
- Buffer Almost Empty: [3]
- End of Transfer Management: [4] [5]
- TXx_EMPTY: [6] [7]
- RXx_ FULL: [8]
- End Of Word Count: [9] [10]
- TXx_EMPTY: [11] [12]
- RXx_FULL: [13]
- End Of Word Count: [14]
- MCSPI Register Summary: [15]
- MCSPI Register Description: [16]

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23.5 Multichannel Buffered Serial Port (McBSP)

This section introduces the multichannel buffered serial port (McBSP)

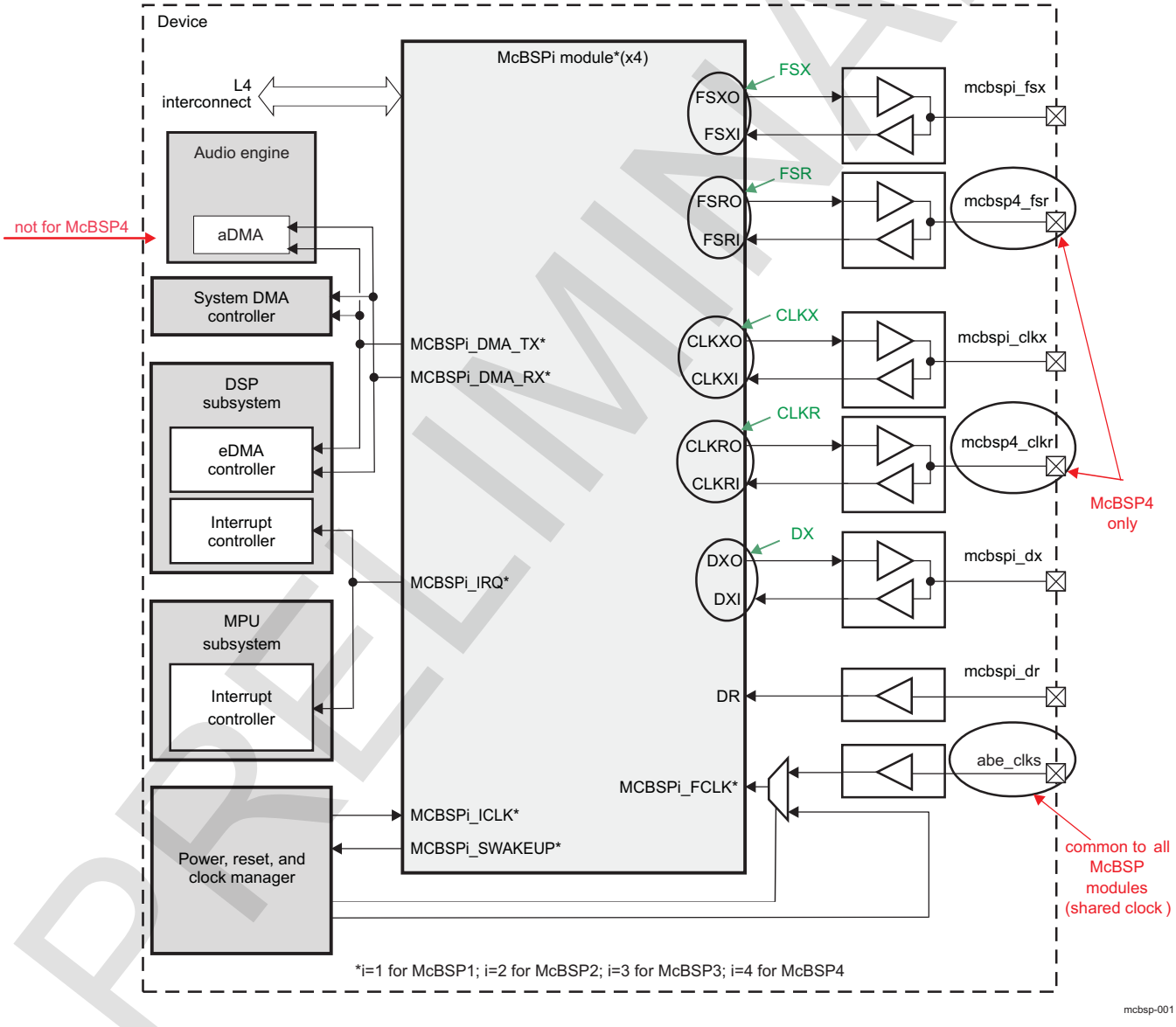
23.5.1 McBSP Overview

The McBSP provides a full-duplex direct serial interface between the device and other devices in a system such as other application devices (digital base band), audio and voice codec, etc. Because of its high level of versatility, it can accommodate a wide range of peripherals and clocked frame oriented protocols (for more information, see Section 23.5.1.1, *McBSP Features*).

The device provides four instances of the McBSP module.

Figure 23-111 is an overview of the McBSP in the device.

Figure 23-111. McBSP Highlight



23.5.1.1 McBSP Features

The main features of the McBSP modules are:

- L4 interconnect slave interface supports:

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  - 32-bit data bus width
  - 32-bit access supported
  - 16-/8-bit access not supported
  - 10-bit address bus width
  - Burst mode not supported
  - Write nonposted transaction mode supported
- 128 × 32-bit words (512 bytes) for each buffer for transmit/receive operations
- Transmit and receive direct memory access (DMA) requests triggered with programmable FIFO thresholds
- Serial interface description
  - 6-pin configuration (McBSP 4 only)
  - 4-pin configuration (McBSP1, 2, 3)
  - Full-duplex communication
  - Multichannel selection modes
    - Support to enable or block transfers in each channel
    - 128 channels for transmission and reception
  - Direct interface to industry-standard codecs, analog interface chips (AICs), and other serially connected A/D and D/A devices:
    - Inter-IC sound (I2S™) compliant devices
    - Pulse code modulation (PCM) devices
    - Time division multiplexed (TDM) bus devices

CAUTION

McBSP modules do not offer support for μ-law and A-law companding, two partitions mode dynamic reassignment, AC'97, and SPI protocol.

  - A wide selection of data sizes: 8, 12, 16, 20, 24, and 32 bits
  - Bit reordering (send/receive least-significant bit [LSB])
- Clock and frame-synchronization generation support:
  - Independent clocking and framing for reception and for transmission up to 48 MHz
  - Support for external generation of clock signals and frame-synchronization (frame-sync) signals
  - A programmable sample rate generator (SRG) for internal generation and control of clock signals and frame-sync signals
  - Programmable polarity for frame-sync pulses and clock signals

NOTE:

- McBSP modules do not support features such as retransmit or re-receive of an erroneous frame or word.
- McBSP modules support dual-phase frames to provide I2S fully compliant capabilities. This dual-phase mode, however, is limited to one channel (or word) for each phase instead of 128 channels maximum for single-phase mode.

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23.5.2 McBSP Environment

This section describes the intended functions for the McBSP module from an environment point of view (that is, external connections). It presents the McBSP connectivity options, lists the possible interfaces, and details the protocol and data format used in each case.

23.5.2.1 McBSP Functions

The device provides four instances of the McBSP module called McBSP1, McBSP2, McBSP3, and McBSP4.

The recommended use (nonexhaustive) for each McBSP module in the device is:

- McBSP1: Digital baseband (DBB) data
- McBSP2: Audio data
- McBSP3: Bluetooth® voice data
- McBSP4: Midi data

Table 23-326 describes the functions and the corresponding application fields.

Table 23-326. Functions Description

Function	Application Field	Recommended McBSP Module	Description
Control and data	DBB data	McBSP1	Serial interface to transfer data
Audio data	Audio data without audio buffer and sidetone feature	McBSP2	Audio interface to transfer audio data with I2S
	Midi data	McBSP4	
Voice data	Bluetooth voice data without sidetone feature	McBSP3	Voice interface to transfer voice data with PCM

23.5.2.2 McBSP Signals Descriptions

The four McBSP modules consist of a data-flow path and a control path connected to external devices by a serial interface with 6-pin configuration (McBSP 4 only) or 4-pin configuration (McBSP1, 2, 3).

For a McBSP module with 6-pin configuration, an internal loopback capability between transmitter and receiver clock signals, and both frame-sync signals, enables using the McBSP module with 4-pin configuration. The related internal multiplexers are controlled through the system control module on the device (see Section 23.5.3, *McBSP Integration*). Table 23-327 describes the inputs/outputs (I/Os).

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Table 23-327. I/O Description

Pin Name	I/O	Description	Internal Signal Name	Reset Value	Control and Data	Audio Data	Voice Data
mcbsp_clks	I	External clock (shared by all McBSP modules)	CLKS	–	✓	✓	✓
abe_mcbspi_dr	I	Receive serial data	DR	–	✓	✓	✓
abe_mcbspi_dx	(I)O[1]	Transmit serial data	DX	0	✓	✓	✓
abe_mcbspi_clkx	I/O [2]	Transmit clock[3]	CLKX	0	✓	✓	✓
abe_mcbspi_fsx	I/O [2]	Transmit frame synchronization [4]	FSX	0	✓	✓	✓
mcbsp4_dr	I	Receive serial data	DR	–	✓	✓	✓
mcbsp4_dx	(I)O [1]	Transmit serial data	DX	0	✓	✓	✓
mcbsp4_clkx	I/O [2]	Transmit clock[3]	CLKX	0	✓	✓	✓
mcbsp4_fsx	I/O [2]	Transmit frame synchronization [4]	FSX	0	✓	✓	✓
mcbsp4_clkr	I/O [2]	Receive clock[5]	CLKR	1	✓		
mcbsp4_fsr	I/O [2]	Receive frame synchronization [6]	FSR	0	✓		

(1) i = 1 to 3; I = Input, O = Output
(2) For details of the I/O selection, see Section 23.5.2.3.1, *McBSP Modes*.
(3) This signal is also used as CLKR when it is configured as output.
(4) This signal is also used as FSR when it is configured as output.
(5) This signal is also used as CLKX when it is configured as input.
(6) This signal is also used as FSX when it is configured as input.

- The mcbsp_clks pin can be used to inject an external clock. This clock is used to generate control signals depending on the module internal configuration (see Section 23.5.4.9, *McBSP SRG*). The CLKS signal of the McBSP modules is linked to an external signal through the mcbsp_clks pin, but the CLKS signal can also be linked to an internal clock provided by the power, reset, and clock management (PRCM) module of the device. For more information, see Section 23.5.3, *McBSP Integration*.
- Data are transmitted to external devices interfacing with McBSP modules through the mcbspi_dx pin. Data from those devices are received on the mcbspi_dr pin.

NOTE: The mcbspi_dx pin is an I/O signal to use the McBSP module in half-duplex mode.

- Control information is communicated by the following pins:
  - mcbspi_clkx (transmit clock)
  - mcbsp4_clkr (receive clock)
  - mcbspi_fsx (transmit frame-sync)
  - mcbsp4_fsr (receive frame-sync)

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CAUTION

External pins mcbsp4_clkr and mcbsp4_fsr are connected to pads only for McBSP4; other McBSP modules do not have these connections. For these modules, CLKR and FSR signals sources are mcbspi_clkx and mcbspi_fsx pins, respectively. Consequently, there is a light restriction on other McBSP modules when used in full-duplex mode. Reception and transmission use the same clock signal and the same frame-sync signal.

23.5.2.3 McBSP Functions Description

23.5.2.3.1 McBSP Modes

For all McBSP functions, McBSP modules can operate in master or slave mode. The difference between these modes is the definition of the source of McBSP clocks and McBSP frames synchronization:

- Master mode: McBSP module provides them to the external device
- Slave mode: McBSP module receives them from the external device

The choice between the two modes depends on technical data of the external device and the type of interface (protocols and data formats). For one McBSP module, there are four possible functions:

- Transmit-and-receive master mode
- Transmit-and-receive slave mode
- Transmit master mode and receive slave mode
- Transmit slave mode and receive master mode

NOTE: If the McBSP has a serial interface with 4-pin configuration (McBSP1, 2, 3), only modes 1 and 2 are possible.

Figure 23-112 shows the connection between McBSP4 (6-pin configuration) and an external device in transmit master mode and receive slave mode.

Figure 23-112. Mode Overview of McBSP4

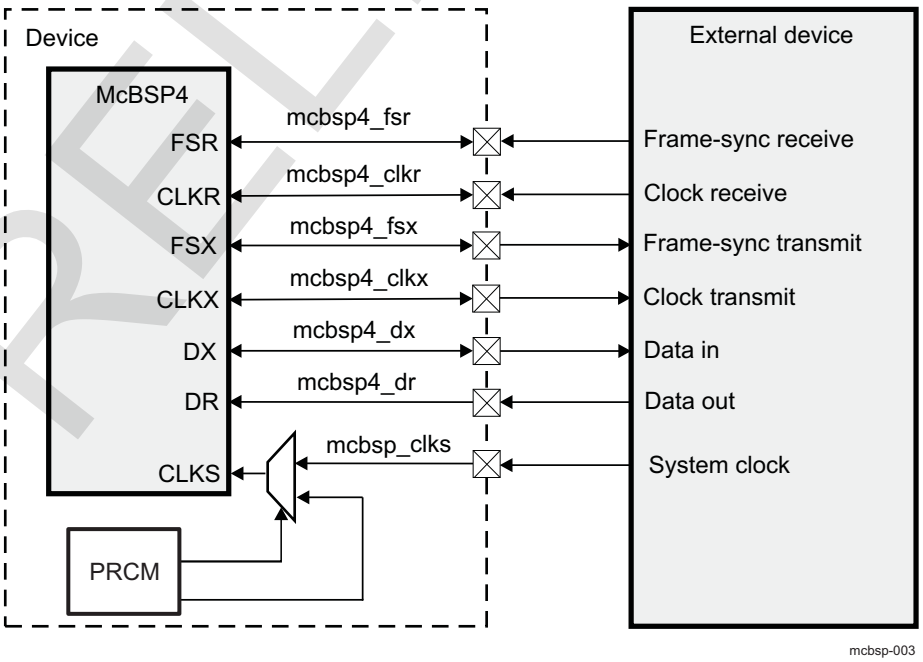

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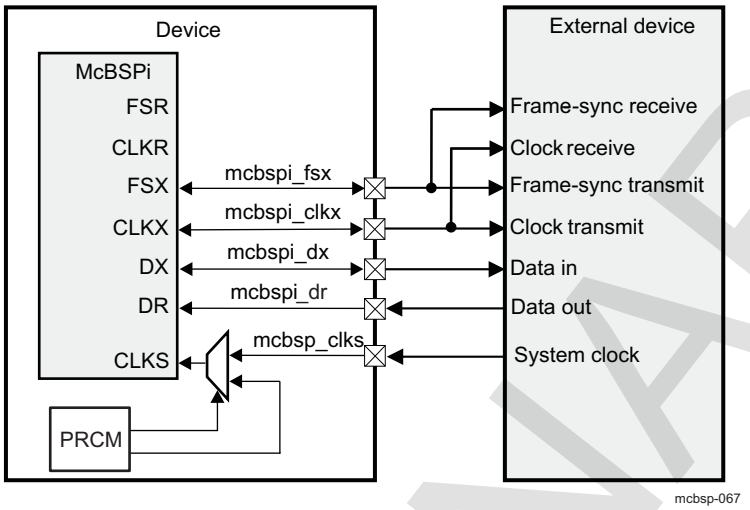
Figure 23-113 shows the connection between the McBSPi module, where i = 1, 2, or 3 (4-pin configuration) and an external device in transmit and receive master mode.

Figure 23-113. Mode Overview of McBSPi

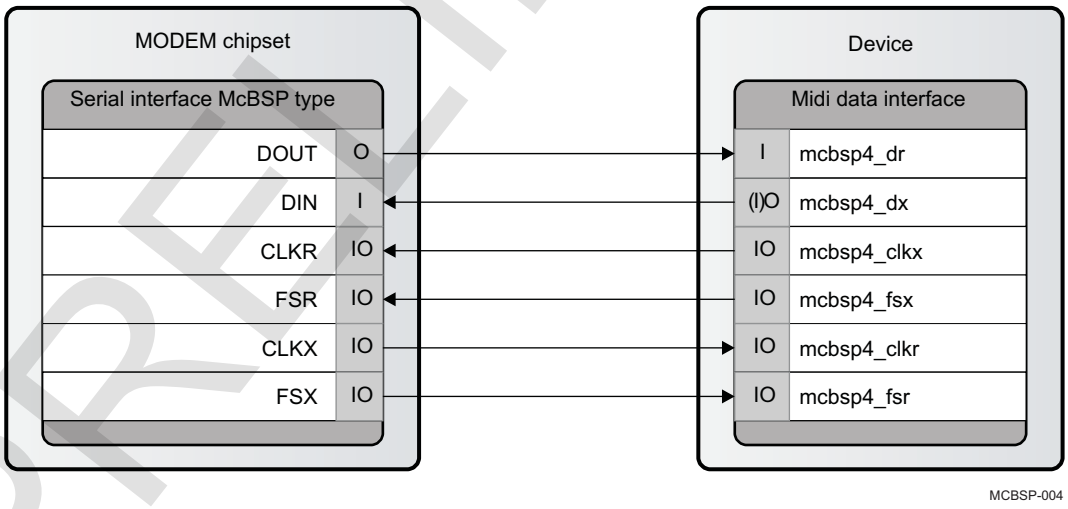


23.5.2.3.2 McBSP Functions

23.5.2.3.2.1 McBSP Function 1: Control and Data

In full-duplex mode (reception and transmission use independent clock signals and frame-sync signals), the McBSP module can be used to exchange control and data with an external chipset, allowing the device to be interfaced with a modem device. Figure 23-114 shows typical connections between device and modem chipset to show the Midi data application.

Figure 23-114. Midi Data Application



In Figure 23-114, McBSP4 is configured in transmit master mode and receive slave mode.

23.5.2.3.2.2 McBSP Function 2: Audio Data

The McBSP module is connected to audio devices through the I2S interface. The I2S link serial interface is a TDM slot-based serial interface that is used to transfer audio data. Those audio devices can be either AICs or other serially connected A/D and D/A devices.

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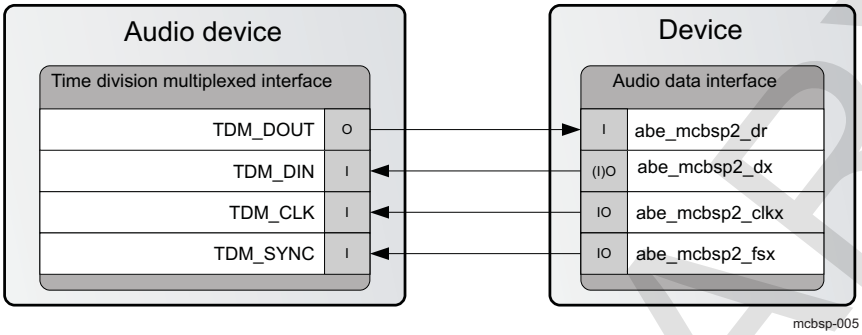
Figure 23-115 shows typical connections between a device and a typical device of analog audio interface to show the audio data application. The typical device contains several audio analog inputs and outputs and digital microphone inputs.

Figure 23-115. Audio Data Application



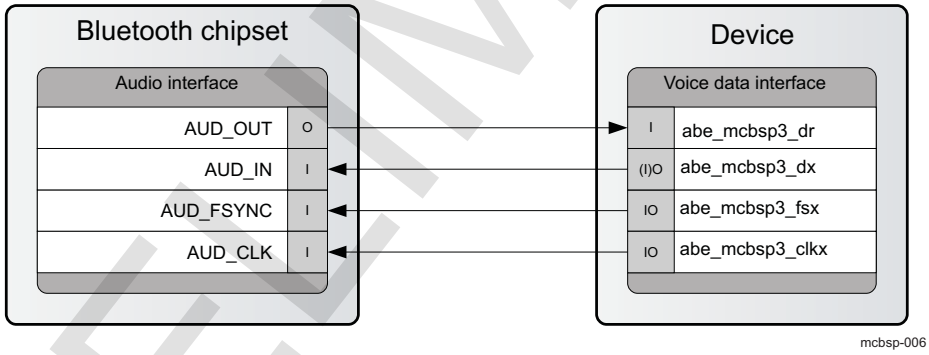
In Figure 23-115, McBSP2 is configured in transmit-and-receive master mode.

23.5.2.3.2.3 McBSP Function 3: Voice Data

The McBSP module is connected to a voice device through the PCM interface. The PCM link serial interface is a TDM slot-based serial interface that is used to transfer voice data. The voice devices can be modem chipsets, Bluetooth chipsets, or other devices with voice data interface.

Figure 23-116 shows typical connections between a device and a Bluetooth chipset (TI BRF6300 or TI BRF6350) to show voice data application.

Figure 23-116. Voice Data Application



In Figure 23-116, McBSP3 is configured in transmit-and-receive master mode.

23.5.2.4 McBSP Protocols and Data Formats

The McBSP module can use one of the three protocols with associated data formats:

- Serial protocol to exchange serial data
- Audio protocol to exchange the audio samples
- Voice protocol to exchange the voice samples

The McBSP modules offer the flexibility to modify the following parameters to adapt to the device features as described in the following subsections.

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23.5.2.4.1 Words, Frames, and Phases Definitions

23.5.2.4.1.1 Words or Channels

The data bits are transferred (transmission or reception) in a group called a serial word or channel. The number of bits in a word (length) is programmable through bit fields (McBSPi.MCBSPLP_RCR1_REG[7:5] RWDLEN1 and McBSPi.MCBSPLP_RCR2_REG[7:5] RWDLEN2, McBSPi.MCBSPLP_XCR1_REG[7:5] XWDLEN1 and McBSPi.MCBSPLP_XCR2_REG[7:5] XWDLEN2) and can be 8, 12, 16, 20, 24, or 32 bits (see Section 23.5.4.8.3, *Clocking and Framing Data*). The McBSP module uses clock signals to control the time for each bit transfer. Data are sampled/driven on the rising or falling edge of clock signals. This clock polarity is programmable through bit fields of the pin-control register (McBSPi.MCBSPLP_PCR_REG).

For more information, see Section 23.5.4.8.4, *Frame Phases (Dual-Phase Frame I2S Support)*.

23.5.2.4.1.2 Frames

One or more words (maximum 128) are transferred in a group called a frame. The McBSP module can transmit and receive a maximum of 128 words per frame, programmable through bit fields of transmit-and-receive control registers (McBSPi.MCBSPLP_XCR1_REG/McBSPi.MCBSPLP_XCR2_REG and McBSPi.MCBSPLP_RCR1_REG/McBSPi.MCBSPLP_RCR2_REG). For more details, see Section 23.5.4.8.3, *Clocking and Framing Data*.

All the words in a frame are sent in a continuous stream. However, there can be pauses between frame transfers. The McBSP module uses frame-sync signals to determine when each frame is received or transmitted. When a pulse occurs on a frame-sync signal, the McBSP module begins receiving or transmitting a frame of data. When the next pulse occurs, the McBSP module receives or transmits the next frame, and so on. The frame-sync pulse is active high or low. This pulse polarity is programmable through bit fields of the pin control register (McBSPi.MCBSPLP_PCR_REG).

Each frame transfer can be delayed by 0, 1, or 2 clock cycles, depending on the value of bits for transmit and receive control registers (McBSPi.MCBSPLP_XCR2_REG and McBSPi.MCBSPLP_RCR2_REG). For more information, see Section 23.5.4.10.6.3, *Preventing Unexpected Transmit Frame-sync Pulses* and Section 23.5.4.10.3.3, *Preventing Unexpected Receive Frame-sync Pulses*.

23.5.2.4.1.3 Phases

The McBSP module allows configuring of each frame to contain one or two phases. The McBSP module supports dual-phase frames to provide I2S fully compliant capabilities. These two phases represent left and right channels of audio stereo signals.

The limitation on dual-phase frame is that the number of words per phase must be set to 1 for both first and second phases. The number of bits per word, however, can be specified differently for each of the two phases of a frame, allowing greater flexibility in structuring data transfers.

For example, software may define a frame composed of a first phase with one 12-bit word and a second phase with one 16-bit word. This configuration allows the software to compose frames for custom applications. For more details, see Section 23.5.4.8.4, *Frame Phases (Dual-Phase Frame I2S Support)*.

Figure 23-117 shows signal activity for two possible reception/transmission scenarios.

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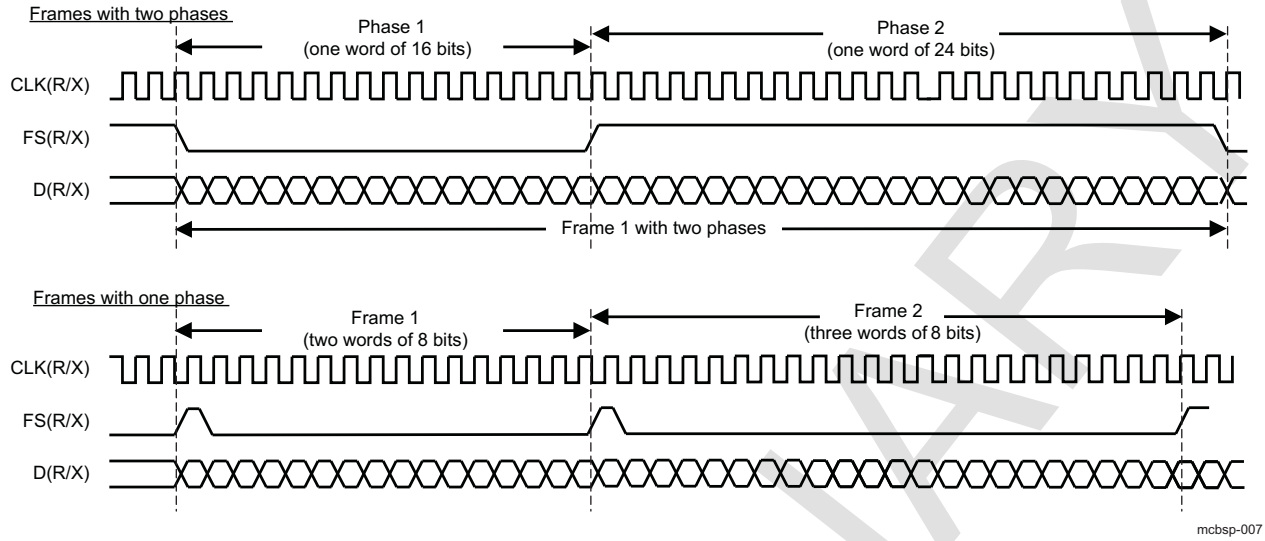
Figure 23-117. McBSP Reception/Transmission Signal Activity



23.5.2.4.2 Serial Protocol and Data Formats

23.5.2.4.2.1 Protocol

The serial protocol is used to send and receive control data without specific formats. This allows the McBSP module to accommodate all serial devices and their protocols.

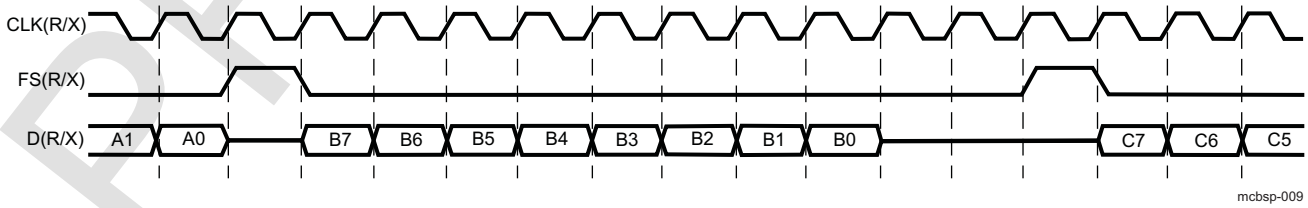
23.5.2.4.2.2 Data Format

Figure 23-118 shows typical operation of the McBSP clock and frame-sync signals. Serial clocks CLKR and CLKX define the boundaries between bits for receive and transmit, respectively. Similarly, frame-sync signals FSR and FSX define the beginning of an element and/or frame transfer. The McBSP module allows the configuration of the following parameters for data and frame synchronization:

- Polarity of FSR, FSX, CLKX, and CLKR
- The number of words per frame
- The number of bits per word
- Whether subsequent frame synchronization restarts the serial data stream or is ignored
- The data delay from frame synchronization to first data bit which can be 0- , 1- , or 2-bit delays

The configuration is independent for receive and transmit parts. For more details and configuration examples, see Section 23.5.4, *McBSP Functional Description*, and Section 23.5.5, *McBSP Basic Programming Model*.

Figure 23-118. Serial Data Formats



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23.5.2.4.3 Audio Protocol and Data Formats

23.5.2.4.3.1 Protocol

The I2S protocol is used to send and receive audio data from 8-kHz to 48-kHz sampling rate (frame-sync frequency), with 16 bits or 32 bits per words (supported frequencies are 8, 11.025, 12, 16, 22.05, 24, 32, 44.1, and 48 kHz).

The frame-sync signal defines the frame length in the I2S protocol. Each frame consists of a fixed number of words. In dual-phase frame, the frame-sync signal is low for the left phase time slot and is high for the right phase time slot. In addition, the frame-sync signal is synchronous to the falling edge of the clock signal.

23.5.2.4.3.2 Data Formats

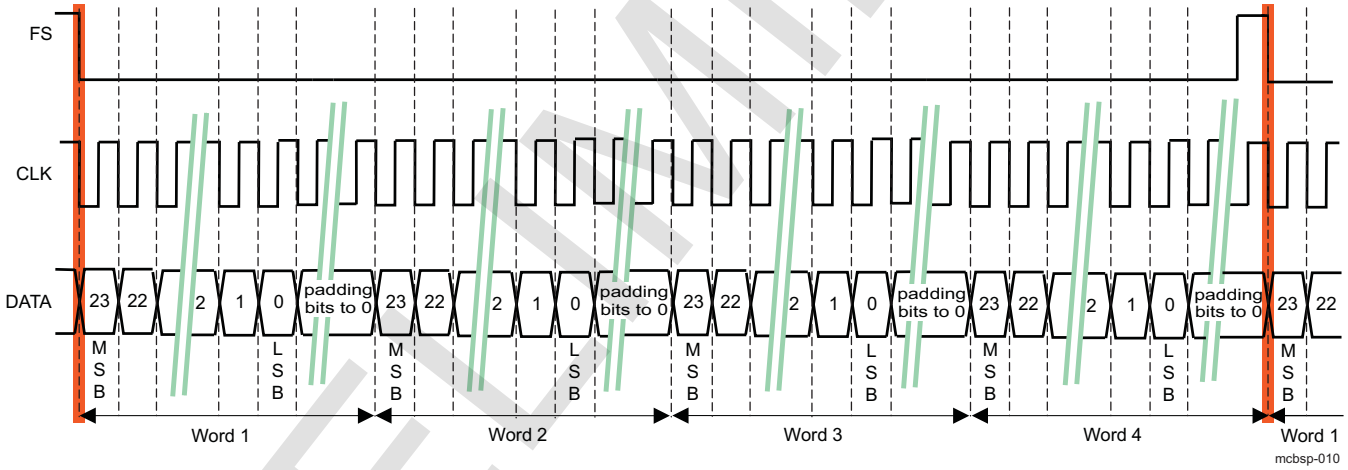
The I2S protocol supports TDM, I2S, left-justified, and right-justified data formats.

Bits of each word (sample) are clocked using the clock signal. For each word, the most-significant bit (MSB) is first. LSBs are padded to 0 when the data length (8, 12, 16, 20, or 24 bits) is less than the sample word width (16 or 32 bits).

23.5.2.4.3.2.1 TDM Data Format

Figure 23-119 shows that each frame of TDM data format is composed of four words (or channels).

Figure 23-119. TDM Data Format; Word Width: 32 Bits; Data Length: 24 Bits



23.5.2.4.3.2.2 I2S Data Format

Figure 23-120 shows an example with 24-bit data (MSB first) and 8 padding bits at 0.

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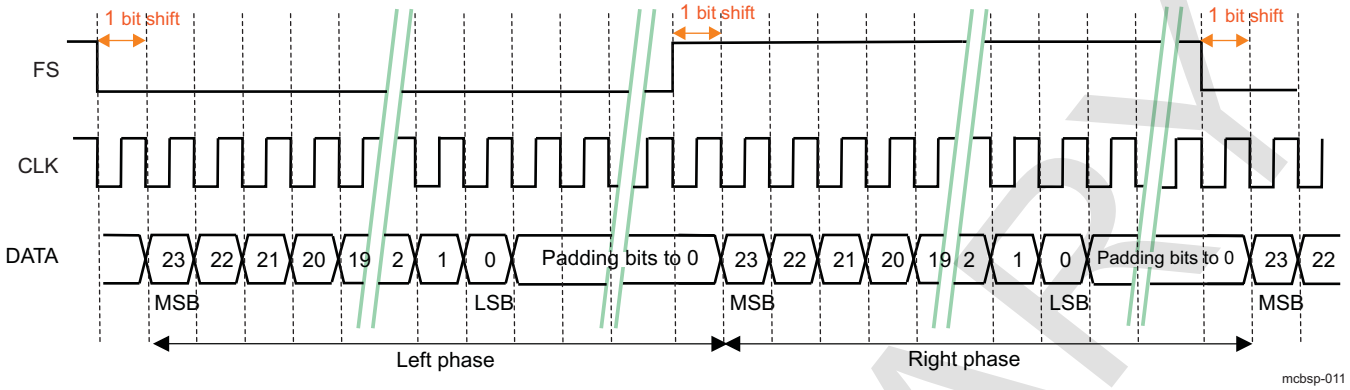
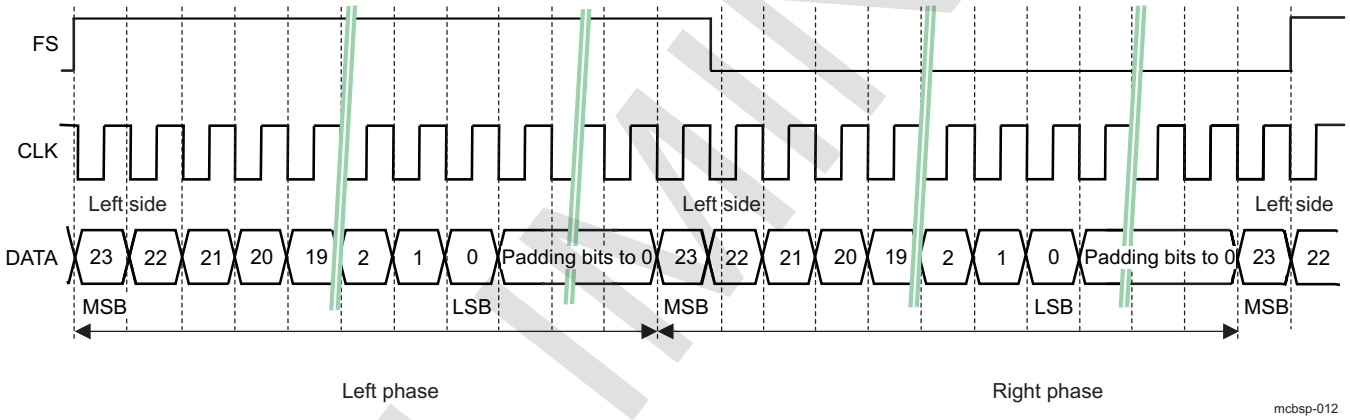
Figure 23-120. I2S Data Format; Word Width: 32 Bits; Data Length: 24 Bits



23.5.2.4.3.2.3 Left-Justified Data Format

Figure 23-121 shows an example with 24-bit data (MSB first) and 8 padding bits at 0.

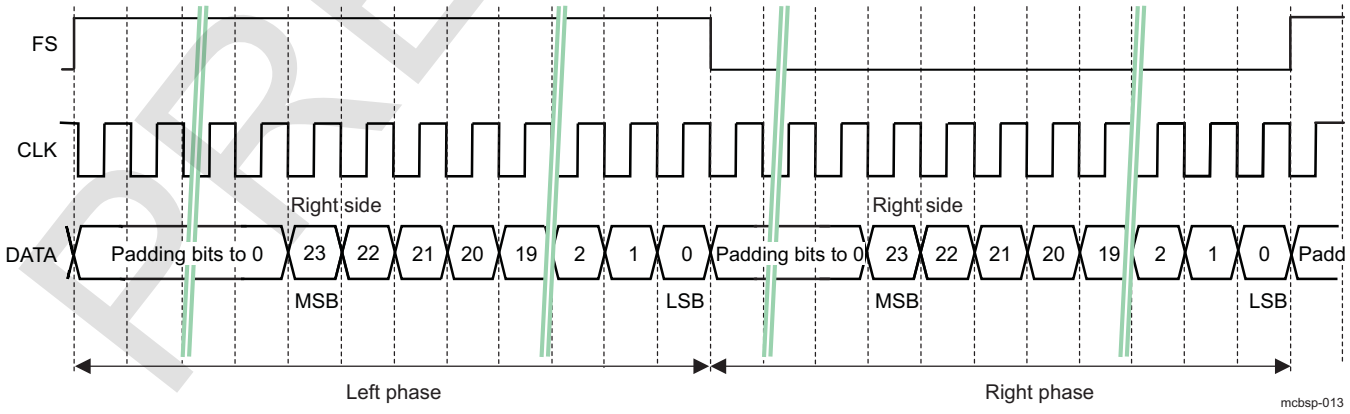
Figure 23-121. Left-Justified Data Format; Word Width: 32 Bits; Data Length: 24 Bits



23.5.2.4.3.2.4 Right-Justified Data Format

Figure 23-122 shows an example with 24-bit data (MSB first) and 8 padding bits at 0.

Figure 23-122. Right-Justified Data Format; Word Width: 32 Bits; Data Length: 24 Bits



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23.5.2.4.4 Voice Protocol and Data Formats

23.5.2.4.4.1 Protocol

The PCM protocol is intended to transfer voice data at 8-kHz (default narrowband mode) or 16-kHz (wideband mode) sample rate (frame-sync frequency). PCM protocol can act as a slave or master, and is used by the Bluetooth interface and the modem generic interface. The frame synchronization defines the frame length in the PCM protocol. Bits are clocked using the PCM clock signal, with the MSB first.

23.5.2.4.4.2 Data Formats

Two modes are available for the PCM protocol: mode 1 and mode 2. Both modes have two types of operations: mono or stereo channels. The difference between PCM mode 1 and PCM mode 2 is in the way in which they use the rising or the falling edge of the clock signal, and the frame-sync polarity.

- PCM mode 1: Input data is latched on the falling edge of the clock, and the transmitted data starts on the rising edge of the clock. The frame-sync pulse is active high.
- PCM mode 2: Input data is latched on the rising edge of the clock, and the transmitted data starts on the falling edge of the clock. The frame-sync pulse is active low.

Figure 23-123 and Figure 23-124 show an example of PCM protocol, mode 1 and mode 2, respectively, for a frame composed of one word (32 bits wide) with 16 bits of data.

Figure 23-123. PCM Protocol – Mode 1 Data Format

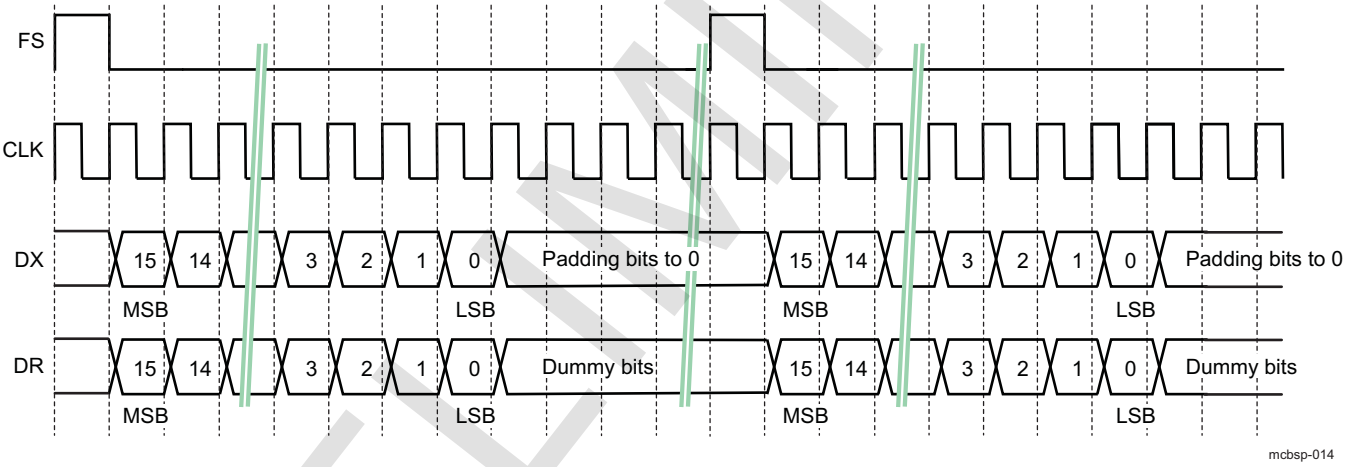
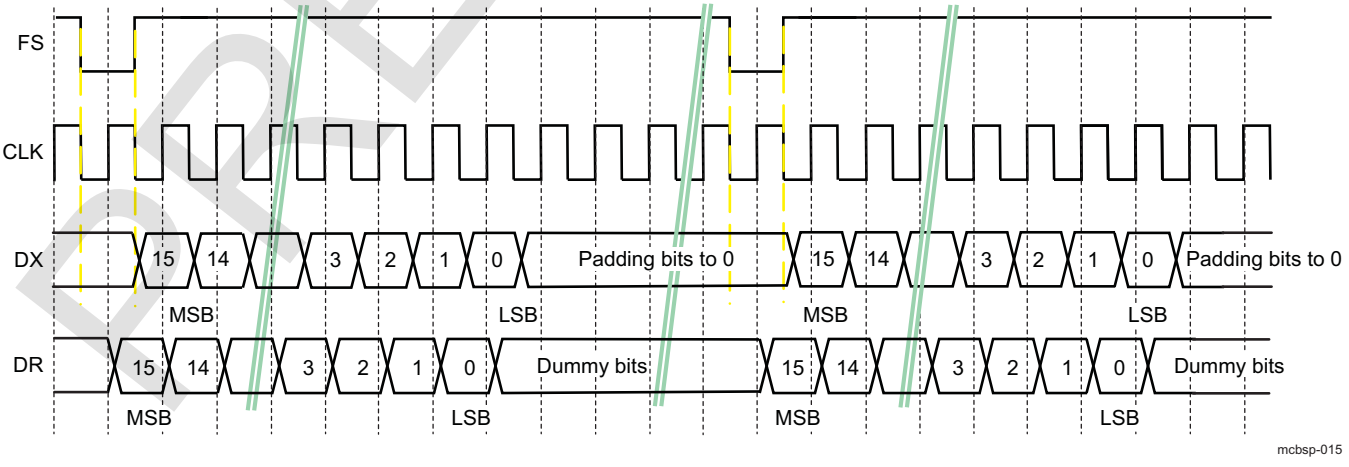


Figure 23-124. PCM Protocol – Mode 2 Data Format



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23.5.3 McBSP Integration

This section describes the integration of the McBSP module in the device, including information about clocks, resets, and hardware requests.

McBSP modules are divided into two families: McBSP modules that are gated in the AUDIO power domain (McBSP1, 2, and 3) and in the L4_PER power domain (McBSP4).

Figure 23-125 through Figure 23-128 show the integration of the McBSP modules in the device, including interrupt handlers, DMA requests, clock generators, and interconnections.

The features of the McBSP modules are:

- Wake-up request
- Two DMA requests
- One IRQ
- One functional clock
- One interface clock

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Figure 23-125. McBSP1 Integration

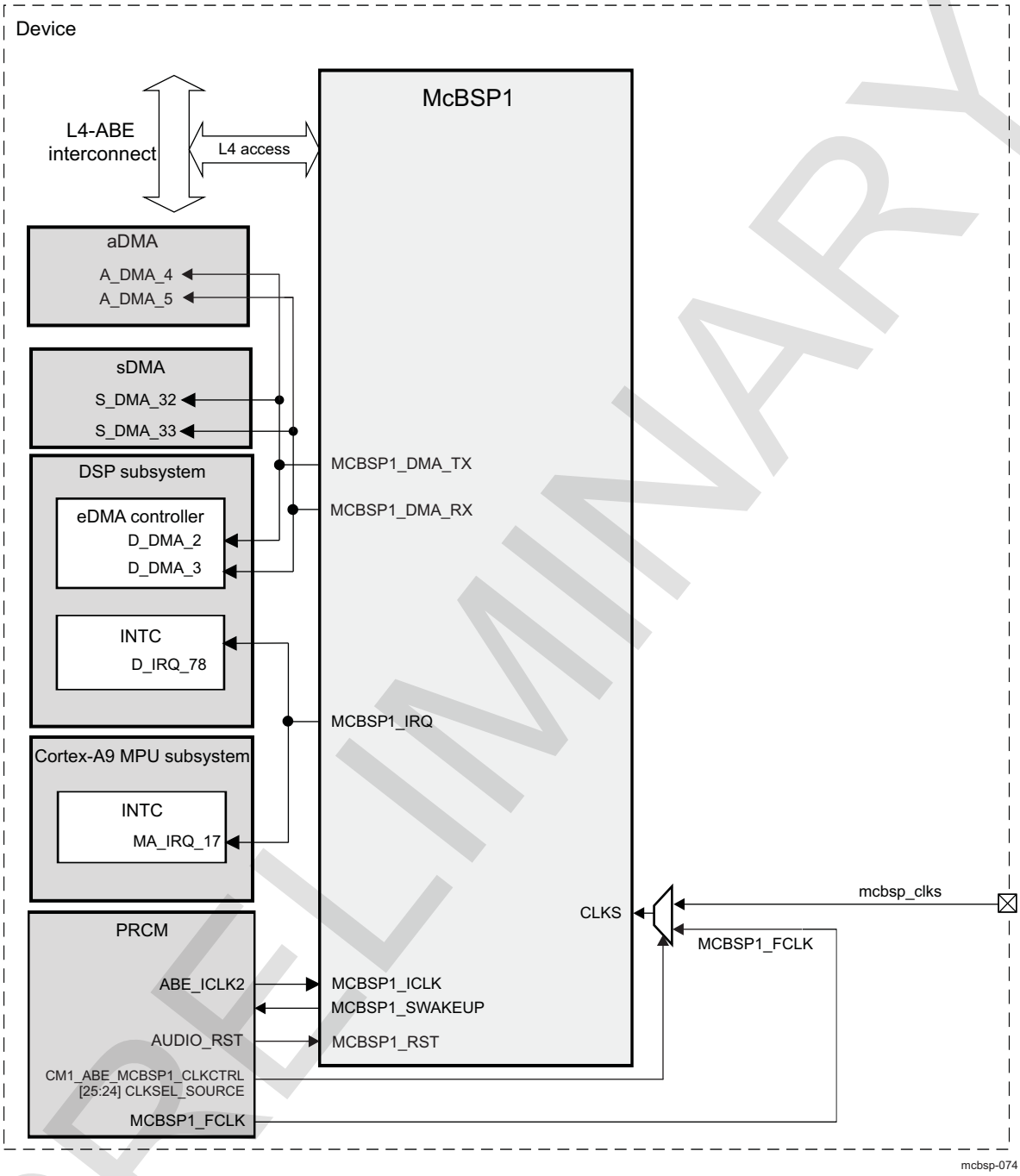

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Figure 23-126. McBSP2 Integration

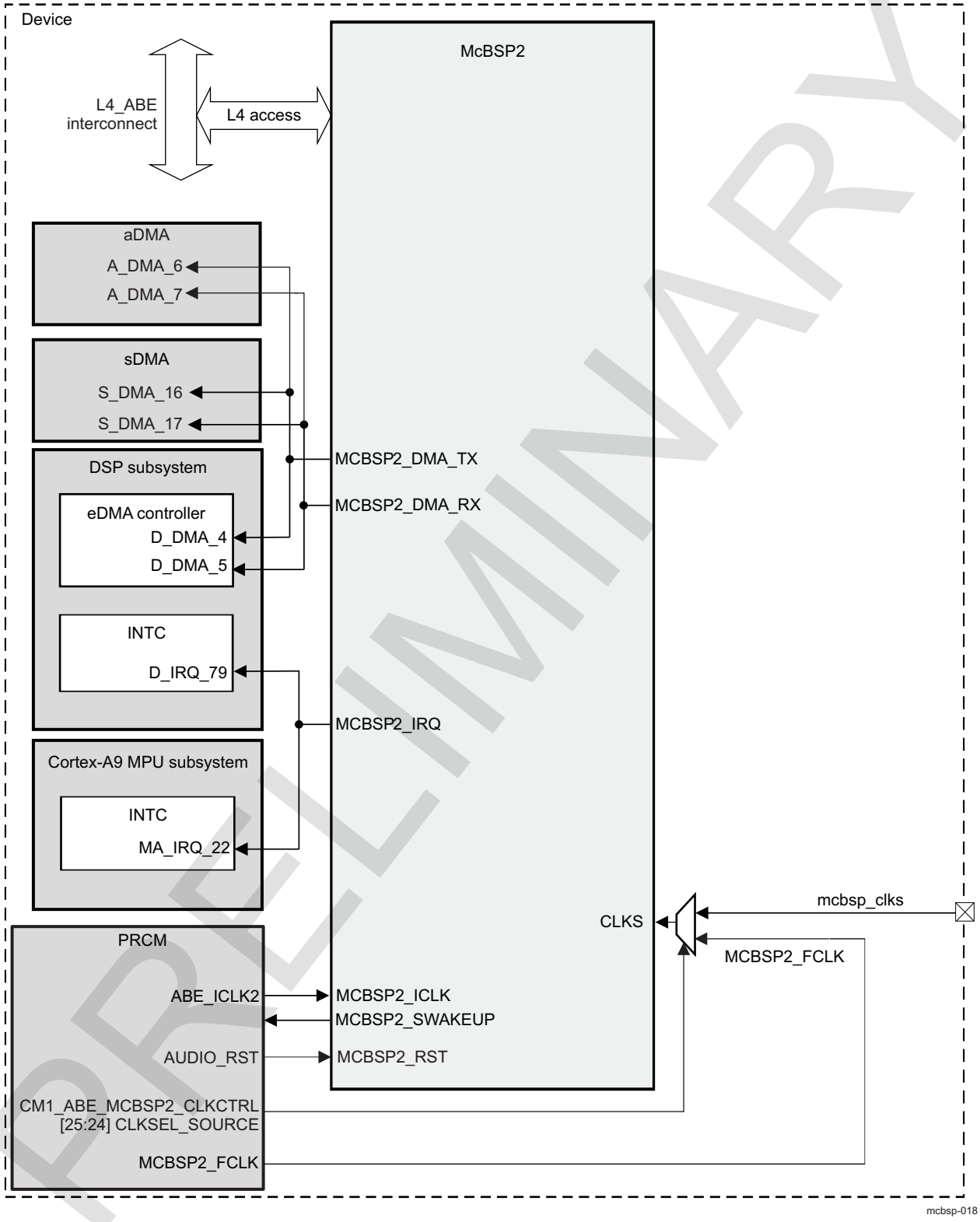

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Figure 23-127. McBSP3 Integration

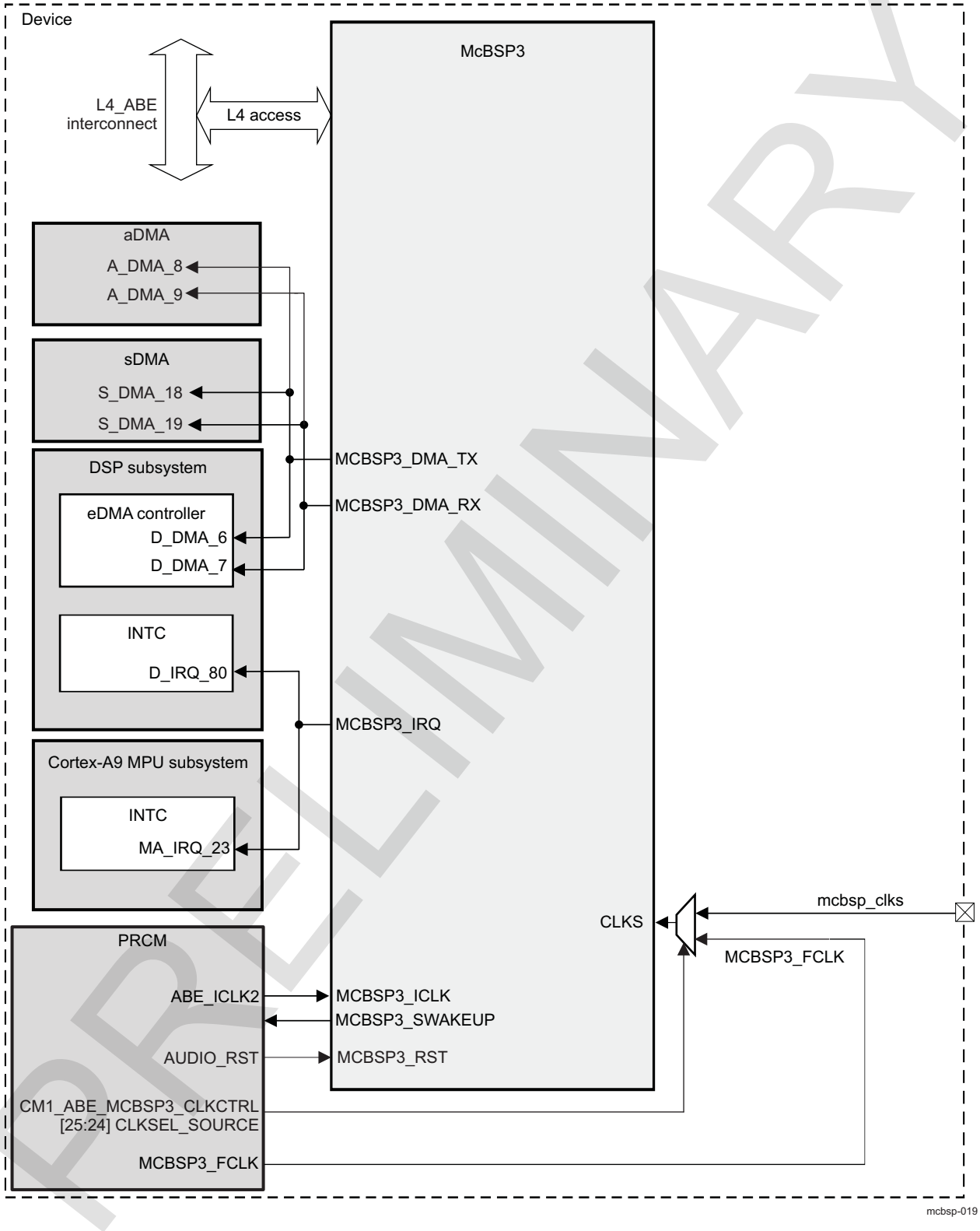

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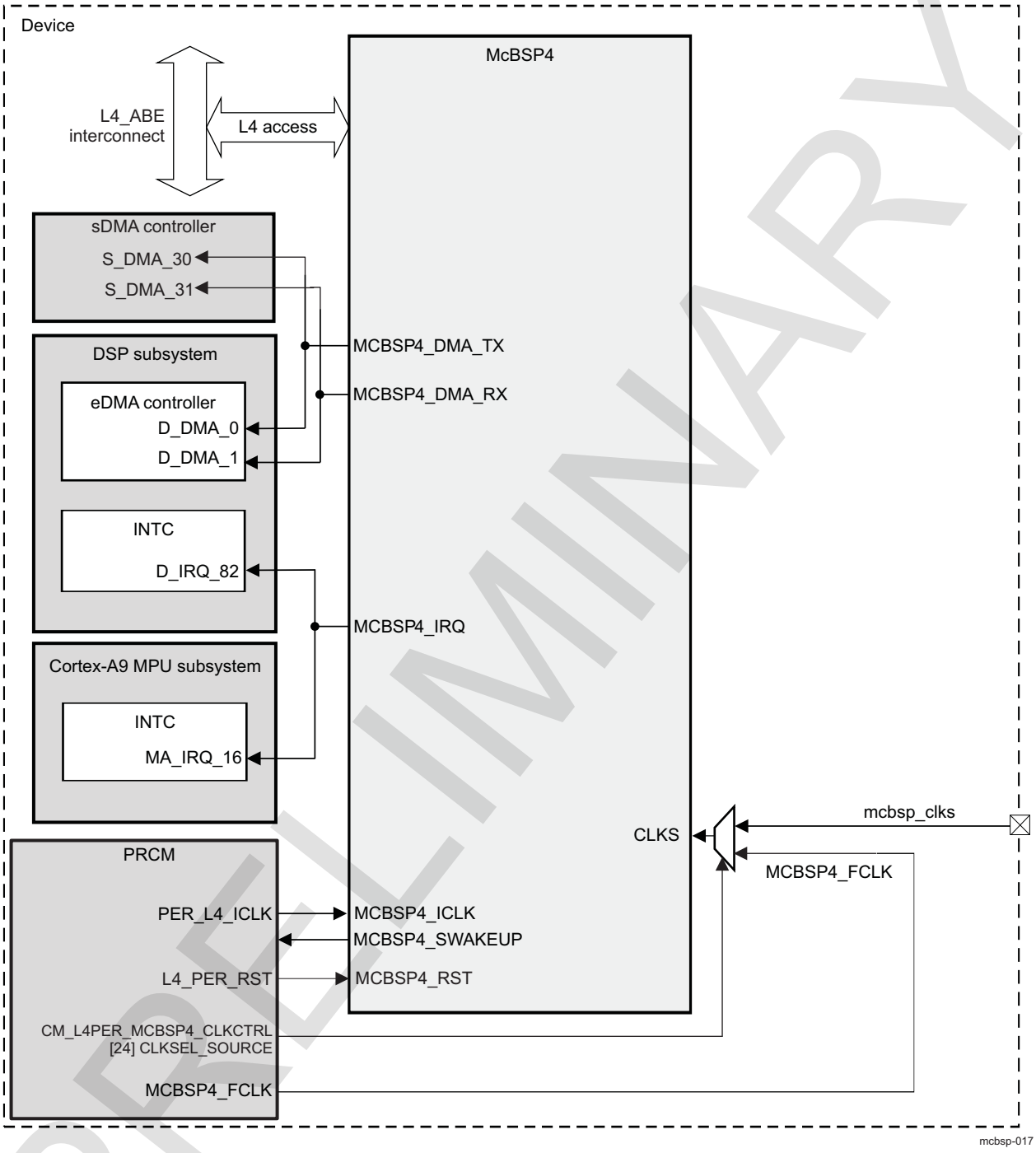
Figure 23-128. McBSP4 Integration



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NOTE: The selection between the FSX and FSR signals is made in the CONTROL_MCBSPLP[31] ALBCTRLRX_FSX bit in the control module register. The selection between the CLKR and CLKX signals is made in the CONTROL_MCBSPLP[30] ALBCTRLRX_CLKX bit in the control module register.

Table 23-328 through Table 23-330 summarize the integration of the module in the device.

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Table 23-328. Integration Attributes

Module Instance	Attributes		
	Power Domain	Wake-Up Capability	Interconnect
MCBSP1	PD_AUDIO	Yes	L4_ABE
MCBSP2	PD_AUDIO	Yes	L4_ABE
MCBSP3	PD_AUDIO	Yes	L4_ABE
MCBSP4	PD_L4_PER	Yes	L4_PER

Table 23-329. Clocks and Resets

Clocks				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
MCBSP1	MCBSP1_ICLK	ABE_ICLK2	PRCM	MCBSP1 interface clock
	MCBSP1_FCLK	MCBSP1_FCLK	PRCM	MCBSP1 functional clock
MCBSP2	MCBSP2_ICLK	ABE_ICLK2	PRCM	MCBSP2 interface clock
	MCBSP2_FCLK	MCBSP2_FCLK	PRCM	MCBSP2 functional clock
MCBSP3	MCBSP3_ICLK	ABE_ICLK2	PRCM	MCBSP3 interface clock
	MCBSP3_FCLK	MCBSP3_FCLK	PRCM	MCBSP3 functional clock
MCBSP4	MCBSP4_ICLK	PER_L4_ICLK	PRCM	MCBSP4 interface clock
	MCBSP4_FCLK	MCBSP4_FCLK	PRCM	MCBSP4 functional clock
Resets				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
MCBSP1	MCBSP1_RST	AUDIO_RST	PRCM	AUDIO power domain reset
MCBSP2	MCBSP2_RST	AUDIO_RST	PRCM	AUDIO power domain reset
MCBSP3	MCBSP3_RST	AUDIO_RST	PRCM	AUDIO power domain reset
MCBSP4	MCBSP4_RST	L4_PER_RST	PRCM	L4_PER power domain reset

Table 23-330. Hardware Requests

Interrupt Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
MCBSP1	MCBSP1_IRQ	D_IRQ_78	DSP INTC	McBSP 1: Common synchronous interrupt request line
	MCBSP1_IRQ	MA_IRQ_17	Cortex-A9 MPU INTC	McBSP 1: Common synchronous interrupt request line
MCBSP2	MCBSP2_IRQ	D_IRQ_79	DSP INTC	McBSP 2: Common synchronous interrupt request line
	MCBSP2_IRQ	MA_IRQ_22	Cortex-A9 MPU INTC	McBSP 2: Common synchronous interrupt request line
MCBSP3	MCBSP3_IRQ	D_IRQ_80	DSP INTC	McBSP 3: Common synchronous interrupt request line
	MCBSP3_IRQ	MA_IRQ_23	Cortex-A9 MPU INTC	McBSP 3: Common synchronous interrupt request line
MCBSP4	MCBSP4_IRQ	D_IRQ_82	DSP INTC	McBSP 4: Common synchronous interrupt request line
	MCBSP4_IRQ	MA_IRQ_16	Cortex-A9 MPU INTC	McBSP 4: Common synchronous interrupt request line
DMA Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
MCBSP1	MCBSP1_DMA_TX	A_DMA_4	aDMA	MCBSP module 1: Transmit DMA request
	MCBSP1_DMA_RX	A_DMA_5	aDMA	MCBSP module 1: Receive DMA request

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Table 23-330. Hardware Requests (continued)

	MCBSP1_DMA_TX	S_DMA_32	sDMA	MCBSP module 1: Transmit DMA request
	MCBSP1_DMA_RX	S_DMA_33	sDMA	MCBSP module 1: Receive DMA request
	MCBSP1_DMA_TX	D_DMA_2	dDMA	MCBSP module 1: Transmit DMA request
	MCBSP1_DMA_RX	D_DMA_3	dDMA	MCBSP module 1: Receive DMA request
MCBSP2	MCBSP2_DMA_TX	A_DMA_6	aDMA	MCBSP module 2: Transmit DMA request
	MCBSP2_DMA_RX	A_DMA_7	aDMA	MCBSP module 2: Receive DMA request
	MCBSP2_DMA_TX	S_DMA_16	sDMA	MCBSP module 2: Transmit DMA request
	MCBSP2_DMA_RX	S_DMA_17	sDMA	MCBSP module 2: Receive DMA request
	MCBSP2_DMA_TX	D_DMA_4	dDMA	MCBSP module 2: Transmit DMA request
	MCBSP2_DMA_RX	D_DMA_5	dDMA	MCBSP module 2: Receive DMA request
MCBSP3	MCBSP3_DMA_TX	A_DMA_8	aDMA	MCBSP module 3: Transmit DMA request
	MCBSP3_DMA_RX	A_DMA_9	aDMA	MCBSP module 3: Receive DMA request
	MCBSP3_DMA_TX	S_DMA_18	sDMA	MCBSP module 3: Transmit DMA request
	MCBSP3_DMA_RX	S_DMA_19	sDMA	MCBSP module 3: Receive DMA request
	MCBSP3_DMA_TX	D_DMA_6	dDMA	MCBSP module 3: Transmit DMA request
	MCBSP3_DMA_RX	D_DMA_7	dDMA	MCBSP module 3: Receive DMA request
MCBSP4	MCBSP4_DMA_TX	S_DMA_30	sDMA	MCBSP module 4: Transmit DMA request
	MCBSP4_DMA_RX	S_DMA_31	sDMA	MCBSP module 4: Receive DMA request
	MCBSP4_DMA_TX	D_DMA_0	aDMA	MCBSP module 4: Transmit DMA request
	MCBSP4_DMA_RX	D_DMA_1	aDMA	MCBSP module 4: Receive DMA request

NOTE:

- For more information about the interrupt source, see Section 23.5.4.6, *Interrupt Requests*.
- For more information about the DMA source, see Section 23.5.4.7, *DMA Requests*.

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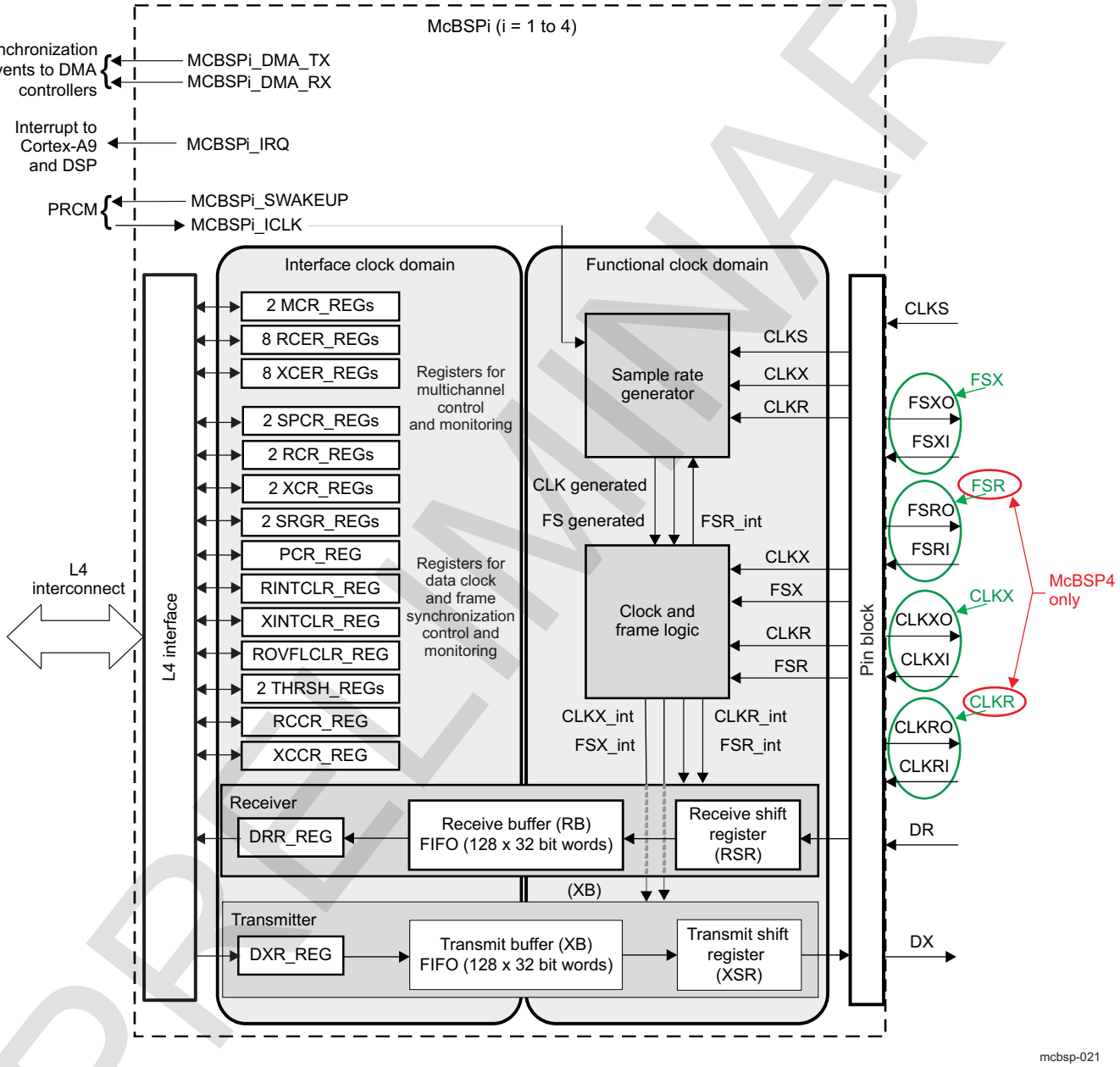
23.5.4 McBSP Functional Description

This section is a functional description of the McBSP module.

23.5.4.1 Block Diagram

Figure 23-129 shows the functional block diagram of the four instances of the McBSP modules.

Figure 23-129. McBSPi Block Diagram



23.5.4.2 Signal Source Control

The sources of the CLKX, DX, DR, FSX, FSR, and CLKR signals are defined by the system control module. The control registers of the system control module are used to select these signal sources. For more information, see Chapter 18, *Control Module*.

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23.5.4.3 McBSP Clock Configuration

23.5.4.3.1 McBSP1 Clocks

McBSP1 is clocked by a functional clock (CLKS and CLKX) and an interface clock (MCBSP1_ICLK).

- The functional clock is used to generate control signals depending on the internal configuration of the module (see Section 23.5.4, *McBSP Functional Description*). For McBSP1, the functional clock comes from the CLKS and CLKX signals. The choice between these two clocks is defined by the MCBSP1.MCBSPLP_PCR_REG[7] SCLKME bit and the MCBSP1.MCBSPLP_SRGR2_REG[13] CLKSM bit.

  The CLKS signal of McBSP1 is linked to an internal clock (MCBSP1_FCLK) provided by the PRCM module. The CLKS signal can also be linked to an external signal through the mcbsp_clks pin of the device boundary.

  NOTE: When McBSP1 no longer requires the functional clock, software can disable it at the PRCM level by configuring the MODULEMODE bit field to 0x0 (PRCM.CM1_ABE_MCBSP1_CLKCTRL[1:0]) in the PRCM registers. The clock is effectively cut, provided the other modules that receive it do not require it.

  At the PRCM level, when all the conditions to shut off the MCBSP1_FCLK clock are met, the PRCM module automatically launches a hardware handshake protocol to ensure McBSP is ready to have this clock switched off. Namely, the PRCM module asserts an IDLE request to the McBSP module. For more information, see Section 3.1.1.1.2, *Module-Level Clock Management*, in Chapter 3, *Power, Reset, and Clock Management*.

  Only the CLKX signal is connected by mcbsp4_clkx pads. The CLKR signal is connected to the CLKX signal. These signals are used like functional clocks by the intermediary of SRG.
- The MCBSP1_ICLK runs at the L4 core interconnect clock speed. It is used to trigger access to the McBSP1 L4 interface and McBSP1 configuration interface through the Cortex-A9 MPU/DSP shared bus. It can also be an input clock for the McBSP SRG (clock divider), depending on the module configuration (see Section 23.5.4.9, *McBSP SRG*). Its source is the ABE_ICLK2 signal.

  NOTE: When McBSP1 no longer requires the interface clock, software can disable it at the PRCM level by configuring the MODULEMODE bit field (PRCM.CM1_ABE_MCBSP1_CLKCTRL[1:0]) in the PRCM registers. The clock is effectively cut, provided the other modules that receive it do not require it.

  At the PRCM level, when all the conditions to shut off the ABE_ICLK2 clock are met the PRCM module automatically launches a hardware handshake protocol to ensure McBSP is ready to have this clock switched off. Namely, the PRCM module asserts an IDLE request to the McBSP module. For more information, see Section 3.1.1.1.2, *Module-Level Clock Management*, in Chapter 3, *Power, Reset , and Clock Management*.

23.5.4.3.2 McBSP2 Clocks

McBSP2 is clocked by a functional clock (CLKS or CLKX) and an interface clock (MCBSP2_ICLK).

- The functional clock is used to generate control signals depending on the internal configuration of the module (see Section 23.5.4, *McBSP Functional Description*). For McBSP2, the functional clock comes from the CLKS and CLKX signals. The choice between these two clocks is defined by the MCBSP2.MCBSPLP_PCR_REG[7] SCLKME bit and the MCBSP2.MCBSPLP_SRGR2_REG[13] CLKSM bit.

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NOTE: When McBSP2 no longer requires the functional clock, software can disable it at the PRCM level by configuring the MODULEMODE bit field to 0x0 (PRCM.CM1_ABE_MCBSP2_CLKCTRL[1:0]) in the PRCM registers. The clock is effectively cut, provided the other modules that receive it do not require it.

At the PRCM level, when all the conditions to shut off the MCBSP2_FCLK clock are met the PRCM automatically launches a hardware handshake protocol to ensure McBSP is ready to have this clock switched off. Namely, the PRCM module asserts an IDLE request to the McBSP module. For more information, see Section 3.1.1.1.2, *Module-Level Clock Management*, in Chapter 3, *Power, Reset, and Clock Management*.

Only the CLKX signal is connected by mcbsp2_clkx pads. The CLKR signal is connected to the CLKX signal. These signals are used like functional clocks by the intermediary of the SRG.

- The MCBSP2_ICLK runs at the L4 core interconnect clock speed. It is used to trigger access to the McBSP2 L4 interface and McBSP2 configuration interface through the Cortex-A9 MPU/DSP shared bus. It can also be an input clock for the McBSP SRG (clock divider), depending on the module configuration (see Section 23.5.4.9, *McBSP SRG*). Its source is the ABE_ICLK2 signal.

NOTE: When McBSP2 no longer requires the interface clock, software can disable it at the PRCM level by configuring the MODULEMODE bit field (PRCM.CM1_ABE_MCBSP2_CLKCTRL[1:0]) in the PRCM registers. The clock is effectively cut, provided the other modules that receive it do not require it.

At the PRCM level, when all the conditions to shut off the ABE_ICLK2 clock are met the PRCM module automatically launches a hardware handshake protocol to ensure McBSP is ready to have this clock switched off. Namely, the PRCM module asserts an IDLE request to the McBSP module. For more information, see Section 3.1.1.1.2, *Module-Level Clock Management*, in Chapter 3, *Power, Reset, and Clock Management*.

23.5.4.3.3 McBSP3 Clocks

McBSP3 is clocked by a functional clock (CLKS or CLKX) and an interface clock (MCBSP3_ICLK).

- The functional clock is used to generate control signals depending on the internal configuration of the module (see Section 23.5.4, *McBSP Functional Description*). For McBSP3, the functional clock comes from the CLKS and CLKX signals. The choice between these two clocks is defined by the MCBSP3.MCBSPLP_PCR_REG[7] SCLKME bit and the MCBSP3.MCBSPLP_SRGR2_REG[13] CLKSM bit.

NOTE: When McBSP3 no longer requires the functional clock, software can disable it at the PRCM level by configuring the MODULEMODE bit field to 0x0 (PRCM.CM1_ABE_MCBSP3_CLKCTRL[1:0]) in the PRCM registers. The clock is effectively cut, provided the other modules that receive it do not require it.

At the PRCM level, when all the conditions to shut off the MCBSP3_FCLK clock are met the PRCM module automatically launches a hardware handshake protocol to ensure McBSP is ready to have this clock switched off. Namely, the PRCM module asserts an IDLE request to the McBSP module. For more information, see Section 3.1.1.1.2, *Module-Level Clock Management*, in Chapter 3, *Power, Reset, and Clock Management*.

Only, the CLKX signal is connected by mcbsp3_clkx pads. The CLKR signal is connected to the CLKX signal. These signals are used like functional clocks by the intermediary of SRG.

- The MCBSP3_ICLK runs at the L4 core interconnect clock speed. It is used to trigger access to the McBSP3 L4 interface and McBSP3 configuration interface via the Cortex-A9 MPU/DSP shared bus. It can also be an input clock for the McBSP sample-rate generator (clock divider), depending on the module configuration (see Section 23.5.4.9, *McBSP SRG*). Its source is either the ABE_ICLK2 signal.

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NOTE: When the McBSP2 module does not require the interface clock anymore, the software can disable it at the PRCM level by configuring the MODULEMODE bit field (PRCM.CM1_ABE_MCBSP3_CLKCTRL[1:0]) in the PRCM registers. The clock is effectively cut, provided the other modules that receive it do not require it.

At PRCM level, when all the conditions to shut-off ABE_ICLK2 clock are met the PRCM automatically launches a hardware handshake protocol to ensure McBSP is ready to have this clock switched off. Namely, the PRCM asserts an IDLE request to McBSP module. For more information, see Section 3.1.1.1.2, *Module Level Clock Management* in Chapter 3, *Power, Reset, and Clock Management*.

It is also possible to activate an autoidle mode for this clock (PRCM.CM_AUTOIDLE_PER[1] register AUTO_MCBSP3 bit set to 1). In this case, McBSP3_ICLK follows the AUDIO_L4 clock domain behavior on the device. For more information, see Section 3.1.1.1.2, *Module-Level Clock Management*, in Chapter 3, *Power, Reset, and Clock Management*.

23.5.4.3.4 McBSP4 Clocks

McBSP4 is clocked by a functional clock (CLKS, CLKX, or CLKR) and an interface clock (MCBSP4_ICLK).

- The functional clock is used to generate control signals depending on the internal configuration of the module (see Section 23.5.4, *McBSP Functional Description*). For McBSP4, the functional clock comes from the CLKS, CLKX, or CLKR signal. The choice between these three clocks is defined by the MCBSP4.MCBSPLP_PCR_REG[7] SCLKME bit and the MCBSP4.MCBSPLP_SRGR2_REG[13] CLKSM bit.

  NOTE: When McBSP4 no longer requires the PRCM functional clock, software can disable it at the PRCM level by setting the MODULEMODE bit (PRCM.CM_L4PER_MCBSP4_CLKCTRL[1:0]) in the PRCM registers. The clock is effectively cut, provided the other modules that receive it do not require it.

  At the PRCM level, when all the conditions to shut off the MCBSP4_FCLK clock are met the PRCM module automatically launches a hardware handshake protocol to ensure McBSP is ready to have this clock switched off. Namely, the PRCM asserts an IDLE request to McBSP module. For more information, see Section 3.1.1.1.2, *Module-Level Clock Management*, in Chapter 3, *Power, Reset, and Clock Management*.

  The CLKX and CLKR signals are connected either by mcbsp4_clkx or mcbsp4_clkr pads. These signals are used like functional clocks by the intermediary of the SRG.
- The McBSP4_ICLK runs at the L4 core interconnect clock speed. It is used to trigger access to the McBSP4 L4 interface and McBSP4 configuration interface via the Cortex-A9 MPU/DSP shared bus. It can also be an input clock for the McBSP sample-rate generator (clock divider), depending on the module configuration (see Section 23.5.4.9, *McBSP SRG*). Its source is the PER_L4_ICLK signal.

  NOTE: When the McBSP4 module does not require the interface clock anymore, the software can disable it at the PRCM level by setting the MODULEMODE bit (PRCM.CM_L4PER_MCBSP4_CLKCTRL[1:0]) in the PRCM registers. The clock is effectively cut, provided the other modules that receive it do not require it.

  At PRCM level, when all the conditions to shut-off PER_L4_ICLK clock are met the PRCM automatically launches a hardware handshake protocol to ensure McBSP is ready to have this clock switched off. Namely, the PRCM module asserts an IDLE request to the McBSP module. For more information, see Section 3.1.1.1.2, *Module-Level Clock Management*, in Chapter 3, *Power, Reset, and Clock Management*.

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23.5.4.4 McBSP Software Reset

McBSP4 belongs to the L4_PER domain and its reset signal is L4_PER_RST from the PRCM module. The McBSP1, 2, and 3 modules belong to the AUDIO domain and their reset signal is AUDIO_RST from the PRCM module. Table 23-331 lists the software reset signals to all McBSP modules.

Table 23-331. Software Reset Signals to All McBSP Modules

Type	Bit Field	Register Source	Activation	Description
Software	SOFTRESET	MCBSPi.MCBSPLP_SYSCONFIG_REG[1]	Active high	McBSP global software reset
	RRST	MCBSPi.MCBSPLP_SPCR1_REG[0]	Active low	This resets and disables the receiver, including the RB.
	XRST	MCBSPi.MCBSPLP_SPCR2_REG[0]		This resets and disables the transmitter, including the XB.
	GRST	MCBSPi.MCBSPLP_SPCR2_REG[6]		SRG is reset.
	FRST	MCBSPi.MCBSPLP_SPCR2_REG[7]		Frame-sync logic is reset. Frame-sync generated signal is not generated by the SRG.

For a complete description of the McBSP initialization procedure, see Section 23.5.5.1, *McBSP Initialization Procedure*.

23.5.4.5 McBSP Power Management

23.5.4.5.1 McBSP Operating States

Two operating states are defined for all the McBSP modules:

- ACTIVE state: The module is running synchronously on the interface and functional clocks. Interrupts and DMA requests can be generated according to the configuration (register, master or slave mode, etc) and the external signals.
- IDLE state: As part of the system power management, the PRCM module can request the McBSP modules to enter IDLE state. Depending on the configured acknowledgment mode (force-idle, no-idle and smart-idle modes), a McBSP module effectively enters IDLE state or not. As soon as a McBSP module enters IDLE state, its only activities are those unrelated to clock activity (for example, wake-up features) and its clocks are likely to be switched off at the PRCM level.

NOTE: IDLE request and IDLE acknowledge are only internal signals, with no means to observe or to control. The generation and control of the signals is purely hardware (managed automatically by the PRCM module and the McBSP depending on the SIDLEMODE settings).

23.5.4.5.2 McBSP Acknowledgment Modes

During initialization or configuration of the McBSP module, software must configure how the McBSP module will answer an IDLE solicitation from the PRCM module (that is, the way IDLE acknowledge is asserted following assertion of an idle request).

Each McBSP module can be configured through the MCBSPi.MCBSPLP_SYSCONFIG_REG[4:3] SIDLEMODE bit field as one of the following acknowledgment modes:

- Force-idle mode (SIDLEMODE bit = 0x0): An IDLE request is acknowledged unconditionally, regardless of the internal state of the module. The McBSP module immediately enters IDLE state (no activity), interface and PRCM functional clocks can be stopped, and no interrupts and DMA requests can be generated. In this mode, the McBSP module freezes all the internal activity when the PRCM clocks are switched off by the PRCM module, leading to a potential loss of data.

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CAUTION

In force-idle mode, the wake-up feature is inhibited.

CAUTION

If the McBSP functional part, transmitter or receiver, is running within this period of time (the functional clock source is not the PRCM functional clock), the internal state of the McBSP module will not be idle (FSM states, processes, etc.), and when the McBSP module exits from the Force Idle state unexpected behavior may happen in both receiver and transmitter. To avoid this, both receive and transmit parts, must be disabled by software prior to idle request assertion (all functional clock external sources must be disabled).

- No-idle mode (SIDLEMODE bit = 0x1): An IDLE request is never acknowledged, meaning it prevents the PRCM module from switching off its related clocks and from putting in a lower power state than the power domain to which it belongs. The McBSP module never enters IDLE state (is active).
- Smart-idle mode (SIDLEMODE bit = 0x2): Acknowledgement to an IDLE request is given based on the internal activity of the McBSP module. The McBSP module is in a waiting state, interface and functional clocks can be stopped, no interrupts can be generated, and a wake-up signal can be generated according to the configuration (see Section 23.5.4.5.4, *Analysis of the Receiver Smart-Idle Behavior*) and external signals.

NOTE: The value MCBSPi.MCBSPLP_SYSCONFIG_REG[4:3] SIDLEMODE field = 0x3 must not be used.

When configured in smart-idle mode, the McBSP module also offers an additional granularity on MCBSPi_FCLK and MCBSPi_ICLK gating. The McBSPi.MCBSPLP_SYSCONFIG_REG[9:8] CLOCKACTIVITY bit field is used to determine which clock will be shut down (MCBSPi_FCLK, MCBSPi_ICLK, none of them, or both of them).

CLOCKACTIVITY setting is used in the McBSP module to determine on which part of the module the conditions to acknowledge the PRCM IDLE request will be tested. As an example, if MCBSPi_FCLK is said not to be shut down upon a PRCM IDLE request, this means the McBSP module will consider only MCBSPi_ICLK and the associated pending activities before acknowledging the request.

NOTE: Some McBSP features are associated with MCBSPi_ICLK and others with MCBSPi_FCLK. Using CLOCKACTIVITY along with the smart-idle mode ensures that the features associated with the clock that remain active are always enabled, even if the McBSP has acknowledged an IDLE request. For more information, see Section 23.5.4.5.4, *Analysis of the Receiver Smart-Idle Behavior*.

Table 23-332 lists the value of the bit field and indicates whether the interface (MCBSPi_ICLK) and PRCM functional (MCBSPi_FCLK) clocks can be switched off or not when an IDLE request is received by the McBSP module.

Table 23-332. State of Clocks When the Module is in Idle State

CLOCKACTIVITY Value	Interface Clock (MCBSPi_ICLK)	PRCM Functional Clock
0b00	Off	Off
0b01	Off	On
0b10	On	Off
0b11	On	On

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NOTE: Off means this clock can be switched off.

On means this clock must be maintained during the wake-up period.

CAUTION

The PRCM module does not have any hardware means to read CLOCKACTIVITY settings. Software must ensure a consistent programming between the McBSPi.MCBSPLP_SYSCONFIG_REG[9:8] CLOCKACTIVITY bit field and the PRCM MCBSPi_FCLK and L4_ICLK control bits (see notes in Section 23.5.4.3, *McBSP Clock Configuration*). If the McBSP module is disabled while CLOCKACTIVITY is set to 0x3, nothing prevents the PRCM module from asserting its IDLE request, which is acknowledged regardless of the features associated with the McBSP clocks. This may lead to unpredictable behaviors.

23.5.4.5.3 Wake-Up Capability

When configured in smart-idle mode, the sources for wake-up generation are a subset of the interrupt sources. The wake-up sources are enabled by setting the McBSPi.MCBSPLP_SYSCONFIG_REG[2] ENAWAKEUP bit (wake-up feature control):

- Set to 0, wake-up capability is disabled.
- Set to 1, wake-up capability is enabled.

The MCBSPi_SWAKEUP signal is the McBSP module asynchronous wake-up signal sent to the PRCM module when a wake-up generation is requested.

The wake-up configurations are defined by setting the corresponding bits in the McBSPi.MCBSPLP_WAKEUPEN_REG register.

23.5.4.5.3.1 Receive Wakeup

There are four receive possible wake-up configurations:

- McBSPi.MCBSPLP_WAKEUPEN_REG[3] RRDYEN bit: The McBSP module asserts the McBSPi_SWAKEUP request when the receive buffer reaches the high threshold value (RTHRESHOLD value + 1) of the McBSPi.MCBSPLP_THRSH1_REG register. If the McBSPi.MCBSPLP_IRQENABLE_REG[3] RRDYEN bit is set to 1, the McBSP module sends an interrupt (McBSPi_IRQ) request to the MPU or DSP subsystems when exiting from idle mode (interrupt will be asserted once the McBSPi.MCBSPLP_IRQSTATUS_REG[3] RRDY bit changes from 0 to 1, indicating that received data is ready to be read).
- McBSPi.MCBSPLP_WAKEUPEN_REG[2] REOFEN bit: The McBSP module asserts the McBSPi_SWAKEUP request at the end of the frame. If the McBSPi.MCBSPLP_IRQENABLE_REG[2] REOFEN bit is set to 1, the McBSP module sends an interrupt (McBSPi_IRQ) request to the MPU or DSP subsystems when exiting idle mode.
- McBSPi.MCBSPLP_WAKEUPEN_REG[1] RFSREN bit: The McBSP module sends a McBSPi_SWAKEUP request to the PRCM module when a receive frame-sync pulse is detected while the McBSP module is in idle mode. If the McBSPi.MCBSPLP_IRQENABLE_REG[1] RFSREN bit is set to 1, the McBSP module sends an interrupt (McBSPi_IRQ) request to the MPU or DSP subsystems when exiting idle mode.
- McBSPi.MCBSPLP_WAKEUPEN_REG[0] RSYNCERREN bit: The McBSP module asserts the McBSPi_SWAKEUP request when an unexpected receive frame-sync pulse is detected. If the McBSPi.MCBSPLP_IRQENABLE_REG[0] RSYNCERREN bit is set to 1, the McBSP module sends an interrupt (McBSPi_IRQ) request to the MPU or DSP subsystems when exiting from idle mode (interrupt is asserted once the McBSPi.MCBSPLP_IRQSTATUS_REG[0] RSYNCERR bit changes from 0 to 1, indicating that a receive error occurred).

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23.5.4.5.3.2 Transmit Wakeup

For transmit, there are five possible wake-up configuration scenarios:

- McBSPi.MCBSPLP_WAKEUPEN_REG[14] XEMPTYEOFEN bit: The McBSP module asserts the McBSPi_SWAKEUP request when a complete frame was transmitted and the transmit buffer is empty. If the McBSPi.MCBSPLP_IRQENABLE_REG[14] XEMPTYEOFEN bit is set to 1, the McBSP module sends an interrupt (McBSPi_IRQ) request to the MPU or DSP subsystems when exiting idle mode.
- McBSPi.MCBSPLP_WAKEUPEN_REG[10] XRDYEN bit: The McBSP module asserts the McBSPi_SWAKEUP request when the transmit buffer reaches the high threshold value (XTHRESHOLD value + 1) of the McBSPi.MCBSPLP_THRSH2_REG register. If the McBSPi.MCBSPLP_IRQENABLE_REG[10] XRDYEN bit is set to 1, the McBSP module sends an interrupt (McBSPi_IRQ) request to the MPU or DSP subsystems when exiting from idle mode (interrupt is asserted once the McBSPi.MCBSPLP_IRQSTATUS_REG[10] XRDY bit changes from 0 to 1, indicating that transmit buffer data is ready to accept new data).
- McBSPi.MCBSPLP_WAKEUPEN_REG[9] XEOFEN bit: The McBSP module asserts the McBSPi_SWAKEUP request at the end of the frame. If the McBSPi.MCBSPLP_IRQENABLE_REG[9] XEOFEN bit is set to 1, the McBSP module sends an interrupt (McBSPi_IRQ) request to the MPU or DSP subsystems when exiting idle mode.
- McBSPi.MCBSPLP_WAKEUPEN_REG[8] XFSXEN bit: The McBSP module sends a McBSPi_SWAKEUP request when a transmit frame-sync pulse is detected while the module is in idle mode. If the McBSPi.MCBSPLP_IRQENABLE_REG[8] XFSXEN bit is set to 1, the McBSP module sends an interrupt (McBSPi_IRQ) request to the MPU or DSP subsystems when exiting idle mode.
- McBSPi.MCBSPLP_WAKEUPEN_REG[7] XSYNCERREN bit: The McBSP module asserts the McBSPi_SWAKEUP request when an unexpected transmits frame-sync pulse is detected. If the McBSPi.MCBSPLP_IRQENABLE_REG[7] XSYNCERREN bit is set to 1, the McBSP module sends an interrupt (McBSPi_IRQ) request to the MPU or DSP subsystems when exiting idle mode (interrupt is asserted once the McBSPi.MCBSPLP_IRQSTATUS_REG[7] XSYNCERR bit changes from 0 to 1, indicating that a transmit error occurred).

23.5.4.5.3.3 Notes

When the mcbsp4_fsr/mcbspi_fsx pin is configured as an output, FSR/FSX wake-up generation makes no sense (the module cannot be in smart-idle mode).

Detection of RSYNCERR/XSYNCERR during idle mode can be used only when the mcbsp4_fsr/mcbspi_fsx pin is configured as an input and the remote system knows to assert such an error to trigger the wakeup of the McBSP module.

The module does not implement interrupt request (IRQ) assertion when configured as GPIO (pins that can be used to accept input signals and/or send output signals but are not linked to specific uses); also a wake-up capability in this mode is not available.

23.5.4.5.4 Analysis of the Receiver Smart-Idle Behavior

Table 23-333 provides an analysis of the power mode behavior.

In this table, the CLKRM bit is in the McBSPi.MCBSPLP_PCR_REG register on position 8, the CLKXM bit is in the McBSPi.MCBSPLP_PCR_REG[9] register, and the CLOCKACTIVITY bit is in the McBSPi.MCBSPLP_SYSCONFIG_REG[9:8] register.

The value X indicates that the bit value is not significant.

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Table 23-333. McBSP Smart-Idle Mode Configuration Behavior

CLKRM Bit	CLKXM Bit	McBSP Mode	Source of Functional Clock	CLOCKACTIVITY Bit	Behavior
0	0	Slave	Outside	0bXX	The module acknowledges the IDLE request as soon as there is no pending DMA, interrupt request, or transmit buffer threshold synchronization (only when wake-up event is set on transmit threshold reached), regardless of the CLOCKACTIVITY settings or receive and transmit activity.
0	1	Transmit master	MCBSPi_ICLK	0b0X	The McBSP does not acknowledge the IDLE request unless: • The transmit part is disabled (XDISABLE) or under software reset (XRST). • Transmit and receive parts are disabled (XDISABLE/RDISABLE) or under software reset (XRST/RRST). The IDLE acknowledge is asserted as soon as there is no pending DMA, interrupt request, or transmit/receive buffer threshold synchronization (only when the wake-up event is set on transmit/receive threshold reached) and the pending transmit and/or receive frames were completed in case of transmit and/or receive disable.
			CLKS	0bX0	
			MCBSPi_ICLK	0b1X	The module acknowledges the IDLE request as soon as there is no pending DMA, interrupt request, or transmit/receive buffer threshold synchronization (only when the wake-up event is set on transmit/receive threshold reached).
			CLKS	0bX1	
			CLKR (outside)	0bXX	The module acknowledges the idle request as soon as there is no pending DMA, interrupt request, or transmit/receive buffer threshold synchronization (only when the wake-up event is set on transmit/receive threshold reached), regardless of the CLOCKACTIVITY settings.
1	0	Receive master	MCBSPi_ICLK	0b0X	The McBSP does not acknowledge the IDLE request unless the receive part is disabled (RDISABLE) or under software reset (RRST). The IDLE acknowledge is asserted as soon as there is no pending DMA, interrupt request, or transmit/receive buffer threshold synchronization (only when the wake-up event is set on transmit/receive threshold reached) and the pending transmit and/or receive frames were completed in case of transmit and/or receive disable.
			CLKS	0bX0	
			MCBSPi_ICLK	0b1X	The module acknowledges the IDLE request as soon as there is no pending DMA, interrupt request, or transmit/receive buffer threshold synchronization (only when wake-up event is set on transmit/receive threshold reached).
			CLKS	0bX1	
			CLKX	0bXX	When CLKX is used as source (the functional clock is provided from outside), the module acknowledges the IDLE request as soon as there is no pending DMA, interrupt request, or transmit/receive buffer threshold synchronization (only when the wake-up event is set on transmit/receive threshold reached), regardless of the CLOCKACTIVITY settings.

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Table 23-333. McBSP Smart-Idle Mode Configuration Behavior (continued)

CLKRM Bit	CLKXM Bit	McBSP Mode	Source of Functional Clock	CLOCKACTIVITY Bit	Behavior
1	1	Transmit and receive master	MCBSPi_ICLK	0b0X	The McBSP does not acknowledge the IDLE request unless transmit and receive parts are disabled (XDISABLE/RDISABLE) or under software reset (XRST/RRST). The IDLE acknowledge is asserted as soon as there is no pending DMA, interrupt request, or transmit/receive buffer threshold synchronization (only when the wake-up event is set on transmit/receive threshold reached) and the pending transmit and/or receive frames were completed in case of transmit and/or receive disable. No wake-up event is available in this mode, because the entire McBSP and remote device activity is frozen.
			CLKS	0bX0	
			MCBSPi_ICLK	0b1X	The module acknowledges the IDLE request as soon as there is no pending DMA, interrupt request, or transmit/receive buffer threshold synchronization (only when the wake-up event is set on transmit/receive threshold reached).
			CLKS	0bX1	

NOTE: The RFSREN/XFSXEN mode is suitable for wake-up generation when both clocks (PRCM functional and interface) are switched off and the mcbsp4_fsr/mcbspi_fsx pin is configured as input. The frame-sync pulse is asynchronously detected during idle.

The RSYNCERREN/XSYNCERREN mode can be used to wake up the McBSP module only by a remote module implementing such a feature to trigger a wakeup. In this mode, the functional clock must be active.

23.5.4.6 McBSP Interrupt Requests

Each of the four McBSP modules can generate one common interrupt (MCBSPi_IRQ), shared between the Cortex-A9 MPU subsystem and DSP subsystem interrupt controllers (INTCs).

An event can generate an interrupt request when the corresponding mask bit in the McBSPi.MCBSPLP_IRQENABLE_REG register is set to 1.

Once an interrupt request is generated, software must read the McBSPi.MCBSPLP_IRQSTATUS_REG register to check which event has caused the interrupt request generation, and acknowledge each processed event by setting the corresponding bit in the McBSPi.MCBSPLP_IRQSTATUS_REG register to 1.

23.5.4.7 McBSP DMA Requests

The DMA requests are shared between the DSP subsystem DMA (eDMA) controller, system DMA (sDMA) controller, and audio engine DMA (aDMA) controller. Each of the four McBSP modules can generate two DMA events:

- MCBSPi_DMA_TX: McBSPi module transmit DMA request
- MCBSPi_DMA_RX: McBSPi module receive DMA request

Table 23-330 summaries the DMA events with the mapping on both DMA controllers.

The receive and transmit DMA requests can be individually disabled by setting the McBSPi.MCBSPLP_RCCR_REG[3] RDMAEN and McBSPi.MCBSPLP_XCCR_REG[3] XDMAEN bits to 0. When disabling the DMA, the DMA request line is deasserted even if a DMA transfer is pending and the DMA state-machine is not reset.

For more information, see Section 23.5.4.11, *McBSP DMA Configuration*.

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23.5.4.8 McBSP Data Transfer Process

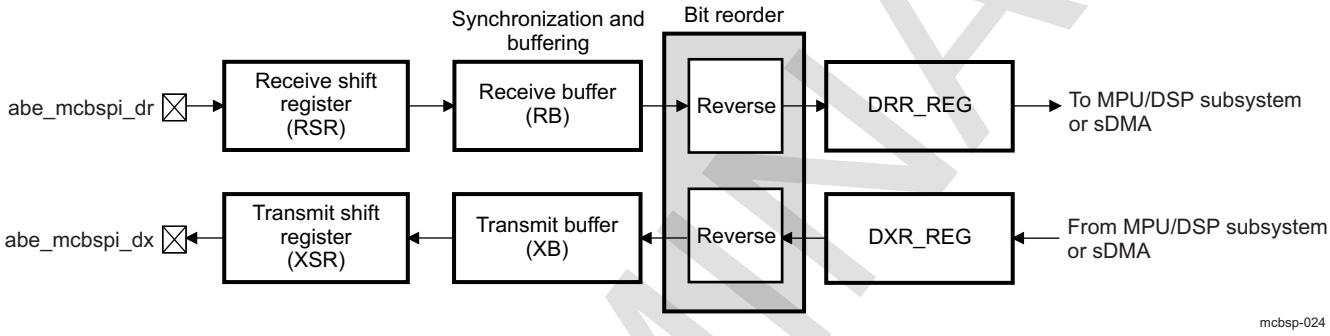
For McBSP modules, receive and transmit operations are triple-buffered (512 bytes buffers organized in 32-bit words are used).

All registers of McBSP data transfer paths are 32 bits wide. Figure 23-130 shows the McBSP data transfer paths.

CAUTION

The McBSP registers (DRR_REG and DXR_REG) are limited to 32-bit data accesses (L4 Interconnect); 16-and 8-bit accesses are not allowed and can corrupt register content.

Figure 23-130. McBSP Data Transfer Paths



23.5.4.8.1 Data Transfer Process for 8-/12-/16-/20-/24-/32-Bit-Long Words

NOTE: For each data word length, one data occupies one 32-bit buffer word.

Receive data arrives on the mcbspi_dr pin and is shifted into the receive shift register (RSR). When a full word (depending on the data length configuration) is received, the content of the shift register is copied into the receive buffer (RB) if it is not full. When the threshold of the RB is reached, the McBSP module asserts DMA or interrupt request and the content of the RB is then transferred (the sDMA or the eDMA controller reads the data receive register McBSPi.MCBSPLP_DRR_REG).

Transmit data is written by the MPU subsystem, DSP subsystem, or the DMA controller to the data transmit register (McBSPi.MCBSPLP_DXR_REG) using the McBSPi.MCBSPLP_SPCR2_REG[1] XRDY bit enable input (when a byte is not enabled, the byte value in the memory contains the previous written value). If there is no previous data in the transmit shift register (XSR), the value from the transmit buffer (XB) is copied to the XSR; otherwise, the content is copied to the XSR when the last bit of the previous data is shifted out on the mcbspi_dx pin.

23.5.4.8.2 Bit Reordering (Option to Transfer LSB First)

Generally, the McBSP module transmits or receives all data with the MSB first. However, some data protocols require the LSB to be transferred first.

If the McBSPi.MCBSPLP_XCR2_REG[4:3] XREVERSE bit field is set to 0b01, the bit ordering of the data words is reversed (LSB first) before being sent to the serial port. If McBSPi.MCBSPLP_RCR2_REG[4:3] RREVERSE bit field is set to 0b01, the bit ordering of the data words is reversed during reception (LSB first).

This feature is available for all the data formats from 8- to 32-bit data length.

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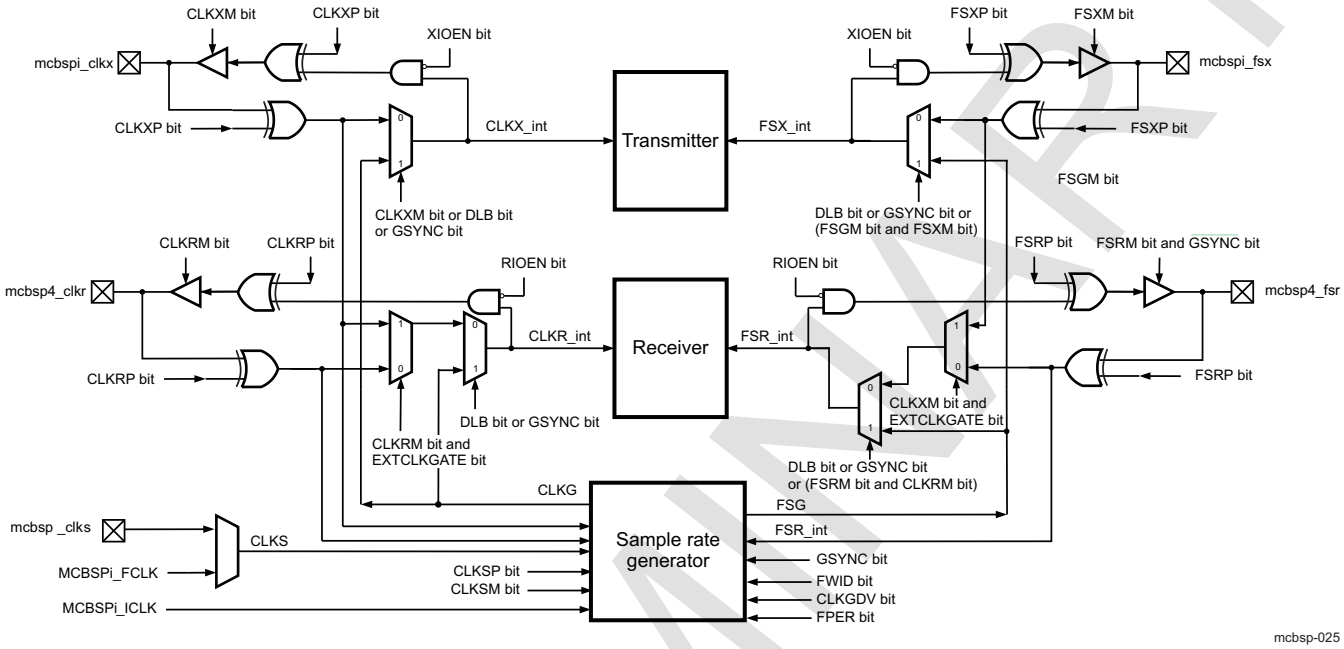
23.5.4.8.3 Clocking and Framing Data

This section explains basic concepts and terminology important for understanding how McBSP data transfers are timed and delimited.

Figure 23-131. Conceptual Block Diagram for Clock and Frame Generation When MCBSPLP_SPCR1_REG[15] ALB = 0



NOTE: For McBSP1, McBSP2, and McBSP3, the mcbspi_clkr pin is connected to the mcbspi_clkx pin, and the mcbspi_fsr pin is connected to the mcbspi_fsx pin.

The CLKR_int clock signal can be derived from three sources:

- The sample rate generator (CLKG): When MCBSPLP_XCCR_REG[5] DLB = 1 or MCBSPLP_SRGR2_REG[15] GSYNC = 1
- mcbsp4_clkr pin (CLKR): When MCBSPLP_PCR_REG[9] CLKXM = 0 and MCBSPLP_XCCR_REG[15] EXTCLKGATE = 0 and (MCBSPLP_XCCR_REG[5] DLB = 0 or MCBSPLP_SRGR2_REG[15] GSYNC = 0)
- mcbspi_clkx pin (CLKX) driven by sample rate generator (CLKG): When MCBSPLP_PCR_REG[9] CLKXM = 1 and MCBSPLP_XCCR_REG[15] EXTCLKGATE = 1 and (MCBSPLP_XCCR_REG[5] DLB = 0 or MCBSPLP_SRGR2_REG[15] GSYNC = 0)

The CLKX_int clock signal can be derived from two sources:

- The sample rate generator (CLKG): When MCBSPLP_PCR_REG[9] CLKXM = 1 or MCBSPLP_XCCR_REG[5] DLB = 1 or MCBSPLP_SRGR2_REG[15] GSYNC = 1
- mcbspi_clkx pin (CLKX): When MCBSPLP_PCR_REG[9] CLKXM = 0 or MCBSPLP_XCCR_REG[5] DLB = 0 or MCBSPLP_SRGR2_REG[15] GSYNC = 0

The FSR_int frame-sync signal can be derived from three sources:

- The sample rate generator (FSG): When MCBSPLP_XCCR_REG[5] DLB = 1 or MCBSPLP_SRGR2_REG[15] GSYNC = 1 or (MCBSPLP_PCR_REG[10] FSRM = 1 and MCBSPLP_PCR_REG[8] CLKRM = 1)
- mcbsp4_fsr pin (FSR): When MCBSPLP_PCR_REG[9] CLKXM = 0 and MCBSPLP_XCCR_REG[15] EXTCLKGATE = 0 and (MCBSPLP_XCCR_REG[5] DLB = 0 or MCBSPLP_SRGR2_REG[15] GSYNC = 0 or (MCBSPLP_PCR_REG[10] FSRM = 0 and MCBSPLP_PCR_REG[8] CLKRM = 0))
- mcbspi_fsx pin (FSX) driven by sample rate generator (FSG): When MCBSPLP_PCR_REG[9] CLKXM = 1 and MCBSPLP_XCCR_REG[15] EXTCLKGATE = 1 and (MCBSPLP_XCCR_REG[5] DLB = 0 or

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MCBSPLP_SRGR2_REG[15] GSYNC = 0 or (MCBSPLP_PCR_REG[10] FSRM = 0 and MCBSPLP_PCR_REG[8] CLKRM = 0))

The FSX_int frame-sync signal can be derived from two sources:

- The sample rate generator (FSG): When MCBSPLP_XCCR_REG[5] DLB = 1 or MCBSPLP_SRGR2_REG[15] GSYNC = 1 or (MCBSPLP_SRGR2_REG[12] FSGM = 1 and MCBSPLP_PCR_REG[11] FSXM = 1)
- mcbspi_fsx pin (FSX): When MCBSPLP_XCCR_REG[5] DLB = 0 or MCBSPLP_SRGR2_REG[15] GSYNC = 0 or (MCBSPLP_SRGR2_REG[12] FSGM = 0 and MCBSPLP_PCR_REG[11] FSXM = 0)

23.5.4.8.3.1 Clocking

Data is shifted 1 bit at a time from the mcbspi_dr pin to the RSRs or from the XSRs to the mcbspi_dx pin. The time for each bit transfer is controlled by the rising or falling edge of a clock signal.

The receive clock signal (CLKR_int) controls bit transfers from the mcbspi_dr pin to the RSRs. The transmit clock signal (CLKX_int) controls bit transfers from the XSRs to the mcbspi_dx pin. The CLKR_int and CLKX_int signals can be derived from a pin at the boundary of the McBSP module (mcbsp4_clkr and mcbspi_clkx, respectively) or derived from inside the McBSP module (see Figure 23-131). The clock source is selected by programming the McBSPi.MCBSPLP_PCR_REG[9] CLKXM and McBSPi.MCBSPLP_PCR_REG[8] CLKRM bits, respectively.

When the McBSPi.MCBSPLP_PCR_REG[9] CLKXM bit (transmitter clock mode) is set to:

- 0: CLKX_int is driven by an external clock and mcbspi_clkx is an input pin.
- 1: CLKX_int is driven by the internal SRG and mcbspi_clkx is an output pin.

For the McBSPi.MCBSPLP_PCR_REG[8] CLKRM bit (receiver clock mode), see Table 23-334.

Table 23-334. Receiver Clock Mode

Value	Digital Loopback Mode	mcbsp4_clkr Pin	Description
0x0	McBSPi.MCBSPLP_XCCR_REG[5] DLB = 0	Input	CLKR_int is driven by an external clock.
	McBSPi.MCBSPLP_XCCR_REG[5] DLB = 1	High -impedance	CLKR_int is driven by CLKX_int. The CLKX_int is derived based on the value of CLKXM.
0x1	McBSPi.MCBSPLP_XCCR_REG[5] DLB = 0	Output	CLKR_int is driven by the internal SRG.
	McBSPi.MCBSPLP_XCCR_REG[5] DLB = 1	Output	CLKR_int is driven by CLKX_int. The CLKX_int is derived based on the value of CLKXM.

The polarities of CLKR and CLKX signals are configured in McBSPi.MCBSPLP_PCR_REG register.

The McBSPi.MCBSPLP_PCR_REG[1] CLKXP bit defines the transmit clock polarity:

- When set to 0, transmit data is driven on the rising edge of the CLKX signal.
- When set to 1, transmit data is driven on the falling edge of the CLKX signal.

The McBSPi.MCBSPLP_PCR_REG[0] CLKRP bit defines the receive clock polarity:

- When set to 0, receive data is sampled on the falling edge of the CLKX signal.
- When set to 1, transmit data sampled on the rising edge of the CLKX signal.

Figure 23-132 shows an example in which the clock signal controls the timing of each bit transfer on the pin.

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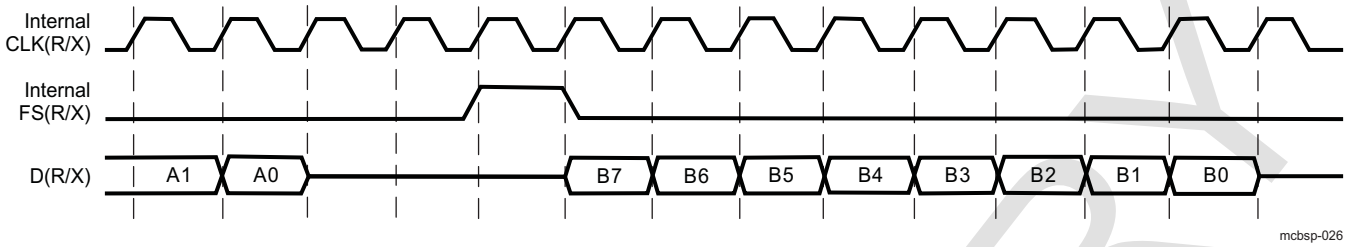
Figure 23-132. Clock Signal Control of Bit Transfer Timing



NOTE: The McBSP module is constrained to operate at an internal functional frequency of up to L4 interface frequency divided by 2. When driving CLKX or CLKR at the pin, choose an appropriate input clock frequency. When using the internal SRG for CLKX/CLKR/CLKS, choose an appropriate input clock frequency (up to L4 interface frequency) and divide down value by programming the McBSPi.MCBSPLP_SRGR1_REG[7:0] CLKGDV bit field.

23.5.4.8.3.2 Serial Words

Bits traveling between a shift register (RSR or XSR) and a data pin (mcbspi_dr or mcbspi_dx) are transferred in a group called a serial word. Software defines how many bits are in a word by programming:

- For the receiver: The McBSPi.MCBSPLP_RCR1_REG[7:5] RWDLEN1 and McBSPi.MCBSPLP_RCR2_REG[7:5] RWDLEN2 bit fields
- For the transmitter: The McBSPi.MCBSPLP_XCR1_REG[7:5] XWDLEN1 and McBSPi.MCBSPLP_XCR2_REG[7:5] XWDLEN2 bit fields

The difference of use is explained in Section 23.5.4.8.4.1, *Number of Phases, Words, and Bits per Frame*.

The various possibilities of word length are 8, 12, 16, 20, 24, and 32 bits (for field values, see Section 23.5.6, *MCBSP Register Manual*)

Bits coming from the mcbspi_dr pin are held in the RSR until it holds a full serial word, and then the word is passed to the RB and the McBSPi.MCBSPLP_DRR_REG register.

During transmission, the XSR accepts new data from the XB after a full serial word has been passed from the XSR to the mcbspi_dx pin.

In the example in Figure 23-135, an 8-bit word size was defined (see the transfer of the 8-bit word B).

23.5.4.8.3.3 Frames and Frame Synchronization

One or more words (up to 128) are transferred in a group called a frame. Software defines how many words are in a frame by programming:

- For the receiver: The McBSPi.MCBSPLP_RCR1_REG[14:8] RFRLEN1 and McBSPi.MCBSPLP_RCR2_REG[14:8] RFRLEN2 bit fields
- For the transmitter: The McBSPi.MCBSPLP_XCR1_REG[14:8] XFRLEN1 and McBSPi.MCBSPLP_XCR2_REG[14:8] XFRLEN2 bit fields

The difference between these registers is explained in Section 23.5.4.8.4.1, *Number of Phases, Words, and Bits per Frame*. For the corresponding field values and number of words, see Section 23.5.6, *MCBSP Register Manual*.

All the words in a frame are sent in a continuous stream. However, there can be pauses between frame transfers. The McBSP module uses frame-sync signals (FSG) to determine when each frame is received/transmitted. When a pulse occurs on a frame-sync signal, the McBSP module begins receiving/transmitting a frame of data. When the next pulse occurs, the McBSP module receives/transmits the next frame, and so on.

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Pulses on the receive frame-sync (FSR_int) signal initiate frame transfers on mcbspi_dr. Pulses on the transmit frame-sync (FSX_int) signal initiate frame transfers on mcbspi_dx. FSR_int or FSX_int signals can be derived from a pin at the boundary of the McBSP module (mcbsp4_fsr and mcbspi_fsx, respectively) or derived from inside the McBSP module (see Figure 23-130). The frame-sync source is selected by programming the McBSPi.MCBSPLP_PCR_REG[11] FSXM and McBSPi.MCBSPLP_PCR_REG[10] FSRM bits, respectively.

When the McBSPi.MCBSPLP_PCR_REG[11] FSXM bit (transmitter frame-sync mode) is set to:

- 0: FSX_int is derived from an external source and mcbspi_fsx is an input pin.
- 1: FSX_int is determined by the McBSPi.MCBSPLP_SRGR2_REG[12] FSGM bit and mcbspi_fsx is an output pin.

For the McBSPi.MCBSPLP_PCR_REG[10] FSRM bit (receiver frame-sync mode), is set to:

- 0: FSR_int is generated by an external source and mcbsp4_fsr is an input pin.
- 1: FSR_int is generated internally by the SRG. The mcbsp4_fsr is an output pin except when McBSPi.MCBSPLP_SRGR2_REG[15] GSYNC bit is set to 0x1.

In the example in Figure 23-131, a one-word frame is transferred when a frame-sync pulse occurs. The polarities of FSR and FSX signals are programmable by bits in the McBSPi.MCBSPLP_PCR_REG register.

The McBSPi.MCBSPLP_PCR_REG[3] FSXP bit defines the transmit frame-sync polarity:

- When set to 0, frame-sync pulse FSX is active high.
- When set to 1, frame-sync pulse FSX is active low.

The McBSPi.MCBSPLP_PCR_REG[2] FSRP bit defines the receive frame-sync polarity:

- When set to 0, frame-sync pulse FSR is active high.
- When set to 1, frame-sync pulse FSR is active low.

In McBSP operation, the inactive-to-active transition of the frame-sync signal indicates the start of the next frame. For this reason, the frame-sync signal may be high for an arbitrary number of clock cycles. Only after the signal is recognized to have gone inactive, and then active again, does the next frame synchronization occur.

23.5.4.8.3.4 Detecting Frame-Sync Pulses, Even in Reset State

The McBSP module can generate receive and transmit interrupts to the Cortex-A9 MPU/DSP subsystems to indicate specific events in the McBSP module. To facilitate detection of frame synchronization, these interrupts can be sent in response to frame-sync pulses (see Section 23.5.5, *McBSP Basic Programming Model* for more information).

Unlike other serial port interrupt modes, this mode can operate while the associated portion of the serial port is in reset (such as activating receive interrupt when the receiver is in reset). In this case, the McBSPi.MCBSPLP_PCR_REG[0] FSRM/McBSPi.MCBSPLP_PCR_REG[1] FSXM bit and the McBSPi.MCBSPLP_PCR_REG[2] FSRP/McBSPi.MCBSPLP_PCR_REG[3] FSXP bit still selects the appropriate source and polarity of frame synchronization. Thus, even when the serial port is in reset state, these signals are synchronized to the interface clock (MCBSPi_ICLK) and then sent to the Cortex-A9 MPU/DSP subsystem in the form of receive interrupt and transmit interrupt at the point where they feed the receiver and transmitter of the serial port. Consequently, a new frame-sync pulse can be detected, and then the Cortex-A9 MPU/DSP subsystem can take the serial port out of reset safely.

23.5.4.8.3.5 Ignoring Frame-Sync Pulses

The McBSP module ignores transmit and/or receive frame-sync pulses if the frame transfer was started by a previous frame-sync pulse (unexpected frame-sync pulses). The McBSP module does not support features such as retransmit or re-receive of an erroneous frame or word. The receiver or transmitter ignores frame-sync pulses until the desired frame length or number of words is reached. For more information about unexpected frame-sync pulses, see Section 23.5.4.10.3, *Unexpected Receive Frame-Sync Pulse*, or Section 23.5.4.10.6, *Unexpected Transmit Frame-Sync Pulse*.

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23.5.4.8.3.6 Frame Frequency

The frame frequency is determined by the period between frame-sync pulses and is defined as shown in the following equation:

Frame frequency = Clock frequency/(number of clock cycles between two rising edges [or falling edges] of two consecutive frame-sync pulses)

The frame frequency can be increased by decreasing the time between frame-sync pulses (limited only by the number of bits per frame). As the frame transmit frequency increases, the inactivity period between the data packets for adjacent transfers decreases to zero.

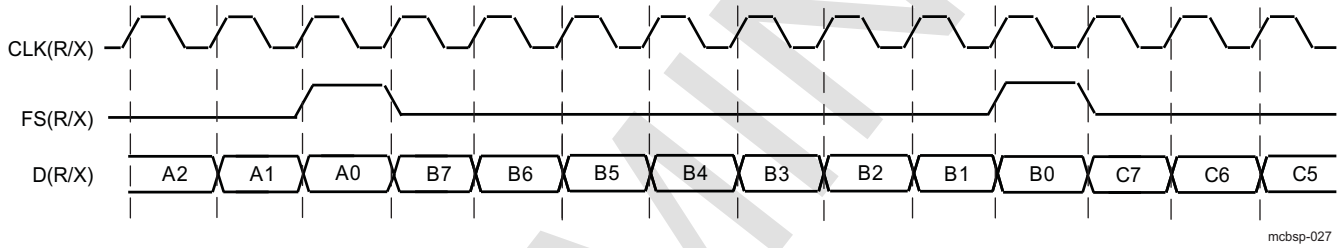
23.5.4.8.3.7 Maximum Frame Frequency

The minimum number of clock cycles between frame-sync pulses is equal to the number of bits transferred per frame. The maximum frame frequency is defined as shown in the following equation:

Maximum frame frequency = Clock frequency/number of bits per frame

Figure 23-133 shows the McBSP operating at maximum packet frequency. At maximum packet frequency, the data bits in consecutive packets are transmitted contiguously with no inactivity between bits.

Figure 23-133. McBSP Operating at Maximum Packet Frequency



If there is a 1-bit data delay as shown in Figure 23-133, the frame-sync pulse overlaps the last bit transmitted in the previous frame. Effectively, this permits a continuous stream of data, back-to-back transfers.

NOTE: When the McBSPi.MCBSPLP_XCR2_REG[1:0] XDATDLY bit field is se to 0x0 (0-bit data delay), the first bit of data is transmitted asynchronously to the internal transmit clock signal (CLKX_int). For more information, see Table 23-384.

23.5.4.8.4 Frame Phases (Dual-Phase Frame I2S Support)

The McBSP module allows configuration of each frame to contain one or two phases. The support for dual-phase frames is required to provide I2S fully compliant capabilities (audio left and right channels—stereo audio stream).

CAUTION

The limitation on dual-phase frame support is that the number of words per phase must be set to 1 for both first and second phases. It is the only possible value for word per frame when using the dual-phase frame.

The number of bits per word can be specified differently for each of the two phases of a frame, allowing greater flexibility in structuring data transfers. For example, a user may define a frame as consisting of one phase containing one 16-bit word, followed by a second phase consisting of one 32-bit word. This configuration allows the user to compose frames for custom applications such as I2S protocol.

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23.5.4.8.4.1 Number of Phases, Words, and Bits per Frame

Table 23-335 shows which bit fields in the receive control registers (McBSPi.MCBSPLP_RCR1_REG and McBSPi.MCBSPLP_RCR2_REG) and in the transmit control registers (McBSPi.MCBSPLP_XCR1_REG and McBSPi.MCBSPLP_XCR2_REG) determine the number of phases per frame, the number of words per frame, and the number of bits per word for each phase, for both receiver and transmitter. The maximum number of words per frame is limited to 2 when using dual-phase frames (one word for each phase), and to 128 for a single-phase frame. The number of bits per word can be 8, 12, 16, 20, 24, or 32 bits.

The following legend applies to Table 23-335:

- RPHASE = McBSPi.MCBSPLP_RCR2_REG[15] RPHASE bit
- XPHASE = McBSPi.MCBSPLP_XCR2_REG[15] XPHASE bit
- RFRLEN1 = McBSPi.MCBSPLP_RCR1_REG[14:8] RFRLEN1 bit field
- RFRLEN2 = McBSPi.MCBSPLP_RCR2_REG[14:8] RFRLEN2 bit field
- XFRLEN1 = McBSPi.MCBSPLP_XCR1_REG[14:8] XFRLEN1 bit field
- XFRLEN2 = McBSPi.MCBSPLP_XCR2_REG[14:8] XFRLEN2 bit field
- RWDLEN1 = McBSPi.MCBSPLP_RCR1_REG[7:5] RWDLEN1 bit field
- RWDLEN2 = McBSPi.MCBSPLP_RCR2_REG[7:5] RWDLEN2 bit field
- XWDLEN1 = McBSPi.MCBSPLP_XCR1_REG[7:5] XWDLEN1 bit field
- XWDLEN2 = McBSPi.MCBSPLP_XCR2_REG[7:5] XWDLEN2 bit field

Table 23-335. Phases, Words and Bits per Frame Control Bit

Operation	Number of Phases	Words per Frame Set With	Bits per Word Set With
Reception	1 (RPHASE = 0)	RFRLEN1	RWDLEN1
Reception	2 (RPHASE = 1)	RFRLEN1 = 0x0 and RFRLEN2 = 0x0	RWDLEN1 for phase 1 RWDLEN2 for phase 2
Transmission	1 (XPHASE = 0)	XFRLEN1	XWDLEN1
Transmission	2 (XPHASE = 1)	XFRLEN1 = 0x0 and XFRLEN2 = 0x0	XWDLEN1 for phase 1 XWDLEN2 for phase 2

23.5.4.8.4.2 Single-Phase Frame Example

Figure 23-134 shows an example of a single-phase data frame containing one 8-bit word. Because the transfer is configured for one data bit delay, the data on the mcbspi_dx and mcbspi_dr pins are available one clock cycle after FS(R/X) goes active. Table 23-336 lists the assumptions used in the example in Figure 23-134.

Table 23-336. Assumptions for the Single-Phase Frame Example

Assumption	Value	Bit or Field Name
Single-phase frame	0	McBSPi.MCBSPLP_RCR2_REG[15] RPHASE
		McBSPi.MCBSPLP_XCR2_REG[15] XPHASE
One word per frame	0x0	McBSPi.MCBSPLP_RCR1_REG[14:8] RFRLEN1
		McBSPi.MCBSPLP_XCR1_REG[14:8] XFRLEN1
8-bit word length	0x0	McBSPi.MCBSPLP_RCR1_REG[7:5] RWDLEN1
		McBSPi.MCBSPLP_XCR1_REG[7:5] XWDLEN1
Word length in register2	Ignored	McBSPi.MCBSPLP_RCR2_REG[14:8] RFRLEN2
		McBSPi.MCBSPLP_XCR2_REG[14:8] XWDLEN2
Receive data clocked on falling edge	0	McBSPi.MCBSPLP_PCR_REG[0] CLKRP
Transmit data clocked on rising edge		McBSPi.MCBSPLP_PCR_REG[1] CLKXP
Active-high frame-sync signals	0	McBSPi.MCBSPLP_PCR_REG[2] FSRP
		McBSPi.MCBSPLP_PCR_REG[3] FSXP
1-bit data delay	01b	McBSPi.MCBSPLP_RCR2_REG[1:0] RDATDLY
		McBSPi.MCBSPLP_XCR2_REG[1:0] XDARDLY

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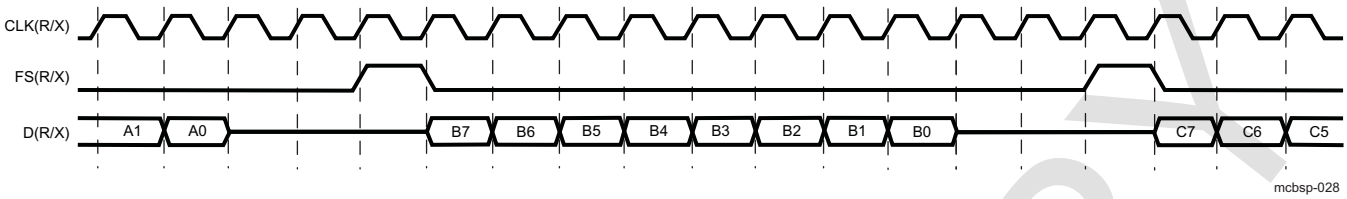
Figure 23-134. Single-Phase Frame for a McBSP Data Transfer



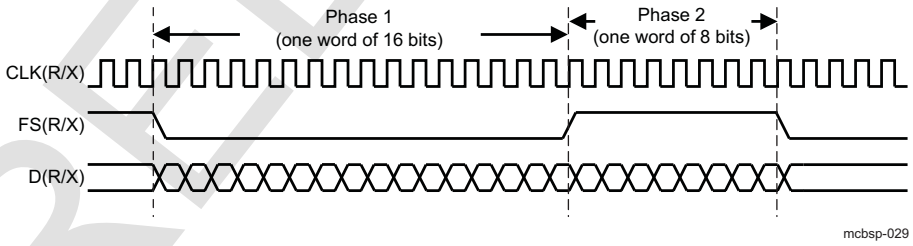
23.5.4.8.4.3 Dual-Phase Frame Example

Figure 23-135 shows an example of a frame. The first phase consists of one word of 16 bits, followed by a second phase of one word of 8 bits. The entire bitstream in the frame is contiguous. There are no gaps between words/phases. Table 23-337 lists the assumptions used in the example in Figure 23-135.

Table 23-337. Assumptions for the Dual-Phase Frame Example

Assumption	Value	Bit or Field Name
Single-phase frame	1	McBSPi.MCBSPLP_RCR2_REG[15] RPHASE
		McBSPi.MCBSPLP_XCR2_REG[15] XPHASE
One word per frame	0x0	McBSPi.MCBSPLP_RCR1_REG[14:8] RFRLEN1
		McBSPi.MCBSPLP_XCR1_REG[14:8] XFRLEN1
16-bit word length	0x0	McBSPi.MCBSPLP_RCR1_REG[7:5] RWDLEN1
		McBSPi.MCBSPLP_XCR1_REG[7:5] XWDLEN1
8-bit word length	0x2	McBSPi.MCBSPLP_RCR2_REG[14:8] RFRLEN2
		McBSPi.MCBSPLP_XCR2_REG[14:8] XWDLEN2
Receive data clocked on falling edge	0	McBSPi.MCBSPLP_PCR_REG[0] CLKRP
Transmit data clocked on rising edge		McBSPi.MCBSPLP_PCR_REG[1] CLKXP
Active-high frame-sync signals	0	McBSPi.MCBSPLP_PCR_REG[2] FSRP
		McBSPi.MCBSPLP_PCR_REG[3] FSXP
0-bit data delay	00b	McBSPi.MCBSPLP_RCR2_REG[1:0] RDATDLY
		McBSPi.MCBSPLP_XCR2_REG[1:0] XDARDLY

Figure 23-135. Dual-Phase Frame for a McBSP Data Transfer



23.5.4.8.5 McBSP Reception

This section explains the fundamental process of reception in the McBSP module. For information about how to program the McBSP receiver, see Section 23.5.5, *McBSP Basic Programming Model*, Section 23.5.5.4, *Interrupt Configuration*, and Section 23.5.5.5, *Receiver Configuration*.

Figure 23-136 and Figure 23-137 show how reception occurs in the McBSP module. A description of the process follows the figures. Figure 23-136 shows the physical path for the data.

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Figure 23-136. McBSP Reception Physical Data Path

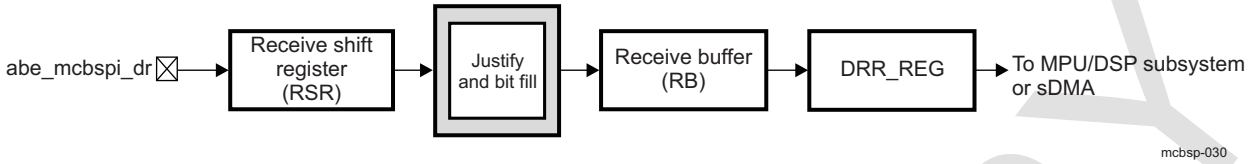
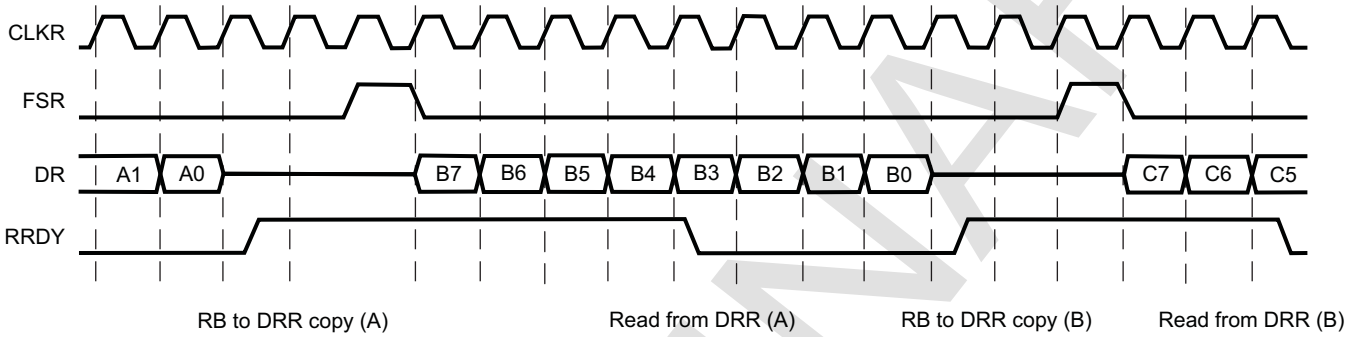


Figure 23-137 is a timing diagram showing signal activity for one possible reception scenario.

Figure 23-137. McBSP Reception Signal Activity



The following process describes how data travels from the mcbspi_dr pin to the MPU/DSP subsystem or to the sDMA controller:

1. The McBSP module waits for a receive frame-sync pulse on FSR_int.
2. When the pulse arrives, the McBSP module inserts the appropriate data delay that is selected with the McBSPi.MCBSPLP_RCR2_REG[1:0] RDATDLY bit field. In the preceding timing diagram a 1-bit data delay is selected.
3. The McBSP module accepts data bits on the mcbspi_dr pin and shifts them into the RSR. For information about choosing a word length, see Section 23.5.5.6, *Transmitter Configuration*.
4. When a full word is received, the McBSP module copies the contents of the RSR to the RB, provided that RB is not full.
5. When the programmed receive threshold is reached (McBSPi.MCBSPLP_THRSH1_REG[6:0] RTHRESHOLD bit field), the McBSP module asserts the receiver ready bit (McBSPi.MCBSPLP_SPCR1_REG[1] RRDY). This indicates that receive data is ready to be read by the Cortex-A9 MPU/DSP subsystem or the sDMA controller by accessing the McBSPi.MCBSPLP_DRR_REG register.

   The data copied from RB to McBSPi.MCBSPLP_DRR_REG is justified and bit-filled according to the McBSPi.MCBSPLP_SPCR1_REG[14:13] RJUST bit field.
6. The Cortex-A9 MPU/DSP subsystem or the sDMA controller reads the data from the data receive register. When the RB is empty, the McBSPi.MCBSPLP_SPCR1_REG[1] RRDY bit is cleared.

23.5.4.8.6 McBSP Transmission

This section explains the fundamental process of transmission in the McBSP module. For information about how to program the McBSP transmitter, see Section 23.5.5, *McBSP Basic Programming Model* and Section 23.5.5.6, *Transmitter Configuration*.

Figure 23-138 and Figure 23-139 show how transmission occurs in the McBSP module. A description of the process follows the figures. Figure 23-138 shows the physical path for the data.

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Figure 23-138. McBSP Transmission Physical Data Path

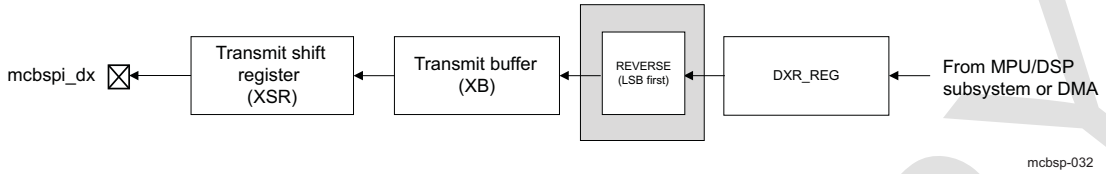
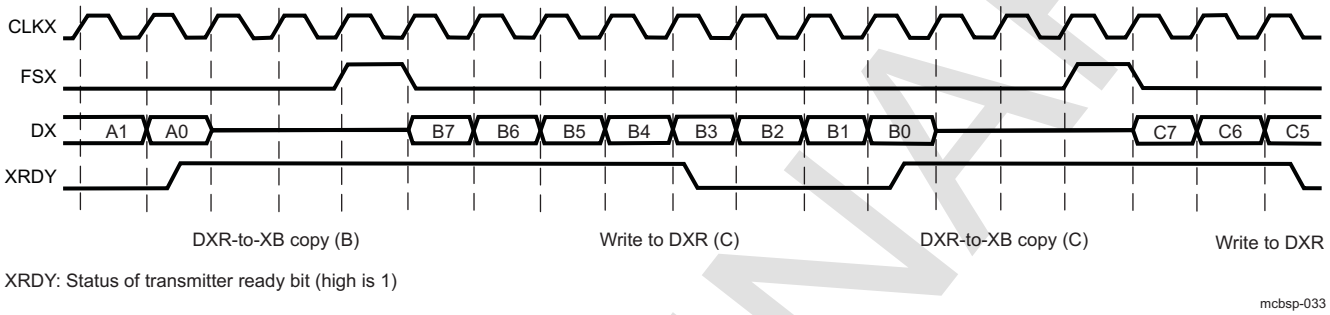


Figure 23-139 is a timing diagram showing signal activity for one possible transmission scenario.

Figure 23-139. McBSP Transmission Signal Activity



XRDY: Status of transmitter ready bit (high is 1)

1. The Cortex-A9 MPU/DSP subsystem or the sDMA controller writes data to the data transmit register (McBSPi.MCBSPLP_DXR_REG). When the XB is reached the transmitter ready bit (McBSPi.MCBSPLP_SPCR2_REG[1] XRDY) is cleared to indicate that the transmitter is not ready for new data. For information about choosing a word length, see Table 23-380.
2. When new data arrives in the McBSPi.MCBSPLP_DXR_REG register, the McBSP module copies the content of the data transmit register to the XB. In addition, the transmit ready bit (McBSPi.MCBSPLP_SPCR2_REG[1] XRDY) is set as long as the buffer contains at least the transmit threshold number of free locations (the McBSPi.MCBSPLP_THRSH2_REG[6:0] XTHRESHOLD bit field). This indicates that the transmitter is ready to accept new data from the MPU/DSP subsystem or the sDMA controller.
3. The McBSP module waits for a transmit frame-sync pulse on FSX_int.
4. When the pulse arrives, the McBSP module inserts the appropriate data delay that is selected with the McBSPi.MCBSPLP_XCR2_REG[1:0] XDATDLY bit field.

   In the preceding timing diagram, a 1-bit data delay is selected.
5. The McBSP module shifts data bits from the XSR to the mcbspi_dx pin.

23.5.4.8.7 Enable/Disable the Transmit and Receive Processes

The McBSP module has the option to stop and resume the transmit/receive process while the module is in functional mode (out of transmit/receive reset).

When the transmit/receive disable bit (McBSPi.MCBSPLP_XCCR_REG[0] XDISABLE/McBSPi.MCBSPLP_RCCR_REG[0] RDISABLE) is set, the McBSP module stops the transmit/receive operation at the next frame boundary (frame corruption avoided).

During the receive disable state, the frames that are sent (when the FSR signal is asserted while receive disable) by the remote device are lost, and the receive buffer overflow status bit (McBSPi.MCBSPLP_IRQSTATUS_REG[5] ROVFLSTAT) is not set. Also, the frames received by the remote device while the McBSPi.MCBSPLP_XCCR_REG[0] XDISABLE bit is set (when the FSX signal is asserted while transmit disable) are meaningless undefined data frames, and transmit buffer underflow status bit (McBSPi.MCBSPLP_IRQSTATUS_REG[11] XUNDFLSTAT) is not set. The presence of the frame synchronization while transmit/receive process is disabled can be checked by reading the transmit/receive frame-sync interrupt status: McBSPi.MCBSPLP_IRQSTATUS_REG[8] XFSX/McBSPi.MCBSPLP_IRQSTATUS_REG[1] RFSR bits.

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As soon as the McBSPi.MCBSPLP_XCCR_REG[0] XDISABLE/McBSPi.MCBSPLP_RCCR_REG[0] RDISABLE bit is cleared, the transmit/receive process resumes at the next frame boundary.

NOTE: It is not recommended to use this mechanism together with the possibility to interrogate the transmit/receive buffer status register (McBSPi.MCBSPLP_XBUFFSTAT_REG[7:0] XBUFFSTAT/McBSPi.MCBSPLP_RBUFFSTAT_REG[7:0] RBUFFSTAT bit field indicating the occupied/available buffer locations), because this register is an interface clock (MCBSPi_ICLK) synchronous register and does not reflect the exact number of occupied/free locations available in the functional clock domain.

23.5.4.8.8 MCBSP Data Transfer Mode

NOTE: For all examples in this section, the configured CLKX edge is the rising edge (McBSPi.MCBSPLP_PCR_REG[1] CLKXP = 0x0) and the configured CLKR edge is the falling edge (McBSPi.MCBSPLP_PCR_REG[0] CLKRP = 0x0). These are the reset values.

In the following timing diagrams, a 1-bit data delay is selected (McBSPi.MCBSPLP_RCR2_REG[1:0] RDATDLY = 0x01 and McBSPi.MCBSPLP_XCR2_REG[1:0] XDATDLY = 0x01), because data often follows a 1-cycle active frame-synchronization.

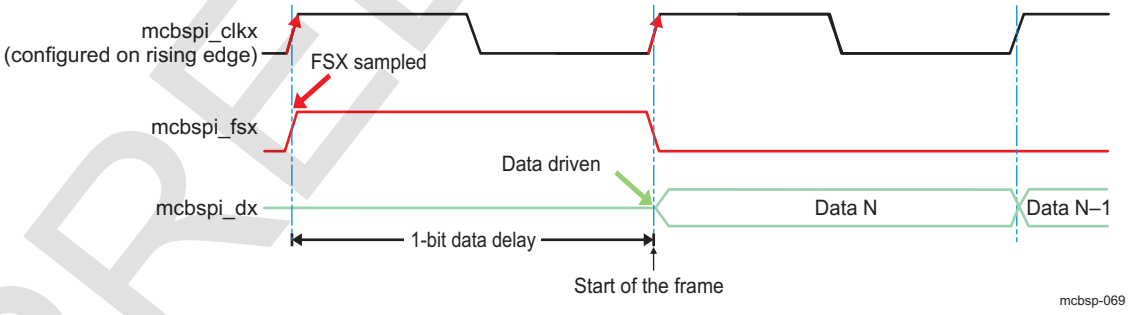
McBSP modules can support two edge selection modes for transmit and receive data transfer at the system level:

- The full-cycle mode, for which one clock period is used to transfer the data, generated on one edge and captured on the same edge (one clock period later)
- The half-cycle mode, for which one-half clock period is used to transfer the data, generated on one edge and captured on the opposite edge (one-half clock period later). New data are generated only every clock period, which ensures the required hold time.

23.5.4.8.8.1 Transmit Full-Cycle Mode

When configured in full-cycle mode (McBSPi.MCBSPLP_XCCR_REG[11] XFULL_CYCLE = 0x1), the FSX signal is sampled on the configured CLKX edge and the data is driven on the same configured edge. See Figure 23-140.

Figure 23-140. Transmit Full-Cycle Timing Diagram



23.5.4.8.8.2 Transmit Half-Cycle Mode

When configured in half-cycle mode (McBSPi.MCBSPLP_XCCR_REG[11] XFULL_CYCLE = 0x0, reset value), the FSX signal is sampled on the opposite configured CLKX edge and the data is driven on the next configured edge. See Figure 23-141.

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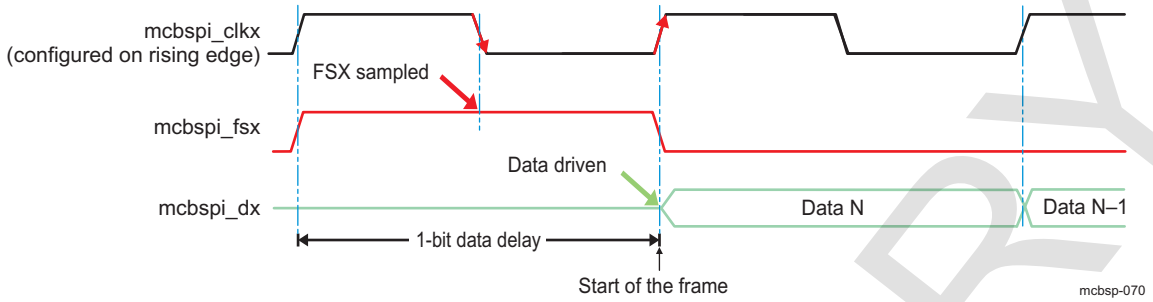
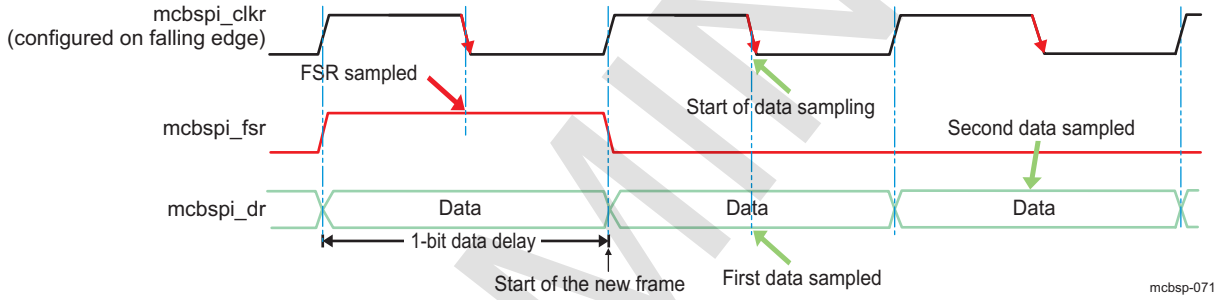
Figure 23-141. Transmit Half-Cycle Timing Diagram



23.5.4.8.8.3 Receive Full-Cycle Mode

When configured in full-cycle mode (McBSPi.MCBSPLP_RCCR_REG[11] RFULL_CYCLE = 0x1, reset value), the FSR signal is sampled on the configured CLKR edge and the data is driven on the same configured edge. See Figure 23-142.

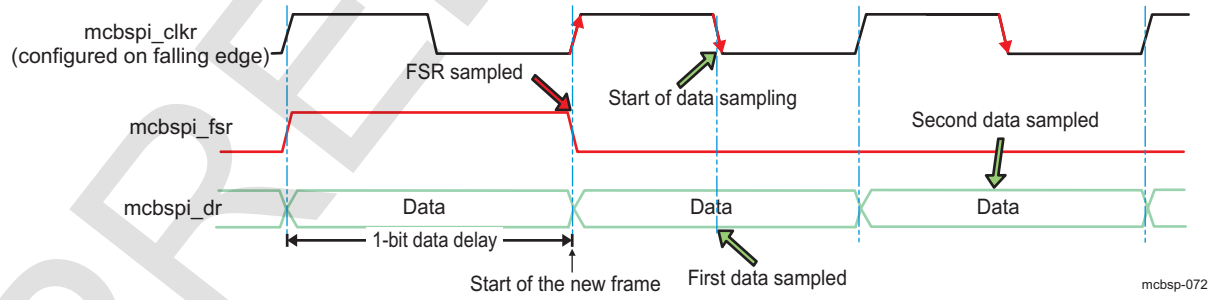
Figure 23-142. Receive Full-Cycle Timing Diagram



23.5.4.8.8.4 Receive Half-Cycle Mode

When configured in half-cycle mode (McBSPi.MCBSPLP_RCCR_REG[11] RFULL_CYCLE = 0x0), the FSR signal is sampled on the opposite configured CLKR edge and the data is driven on the next configured edge. See Figure 23-143.

Figure 23-143. Receive Half-Cycle Timing Diagram



23.5.4.9 McBSP SRG

The McBSP module contains an internal SRG that can be used to generate an internal data clock (CLKG) and an internal frame-sync signal (FSG). CLKG can be used for bit shifting on the data receive pin (mcbspi_dr) and/or the data transmit pin (mcbspi_dx). FSG can be used to initiate frame transfers on the mcbspi_dr pin and/or mcbspi_dx pin. Figure 23-144 is a conceptual block diagram of the SRG.

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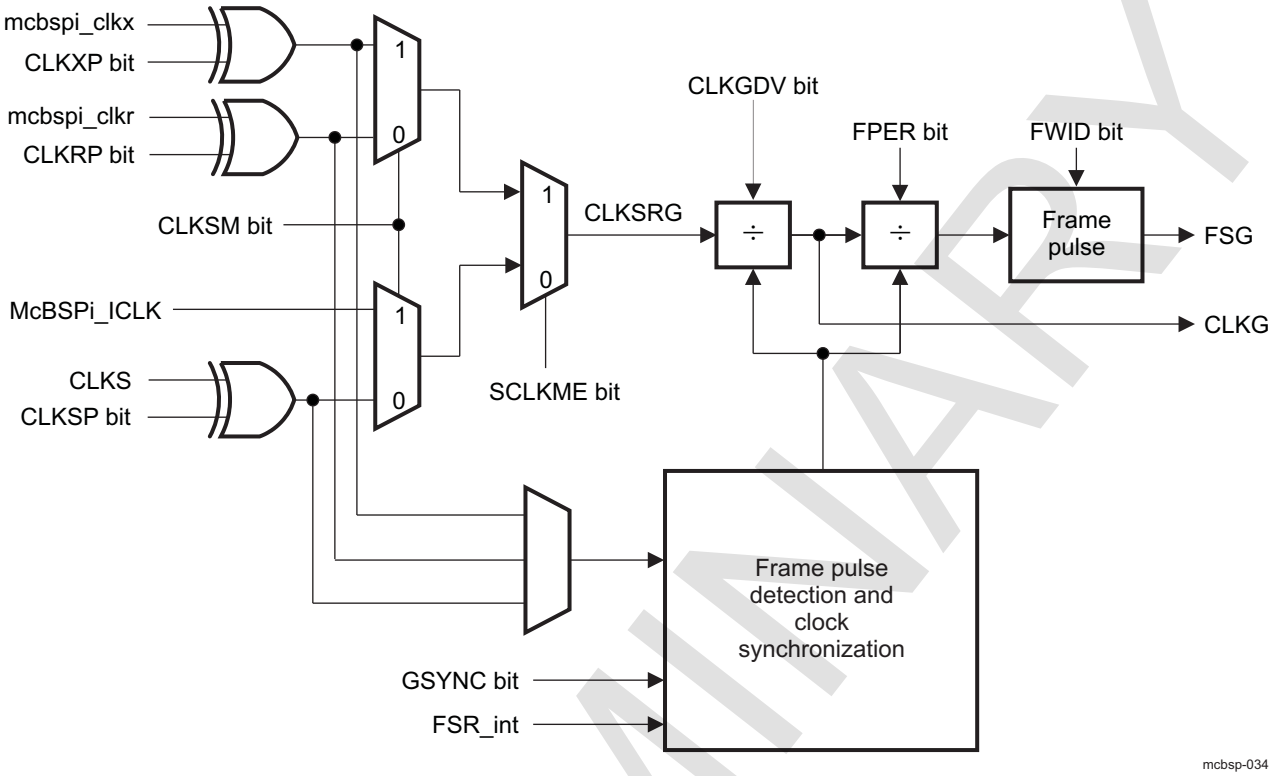
Figure 23-144. Conceptual Block Diagram of the SRG



The source clock for the SRG (labeled CLKSRG in the diagram) can be supplied by the interface clock (McBSPi_ICLK) or the functional clock (CLKS input), or by an external pin (mcbspi_clkx or mcbsp4_clkr). The source is selected with the McBSPi.MCBSPLP_PCR_REG[7] SCLKME bit and the McBSPi.MCBSPLP_SRGR2_REG[13] CLKSM bit.

If a pin or CLKS signal is used, the polarity of the incoming signal can be inverted with the appropriate polarity bit (McBSPi.MCBSPLP_SRGR2_REG[14] CLKSP, McBSPi.MCBSPLP_PCR_REG[1] CLKXP, or McBSPi.MCBSPLP_PCR_REG[0] CLKRP).

The SRG has a 3-stage clock divider that gives CLKG and FSG programmability.

The three stages provide:

- Clock divide-down: The source clock (CLKSRG) is divided according to the McBSPi.MCBSPLP_SRGR1_REG[7:0] CLKGDV bit field to produce the CLKG signal.
- Frame period divide-down: CLKG is divided according to the McBSPi.MCBSPLP_SRGR2_REG[11:0] FPER bit field to control the period from the start of a frame-pulse to the start of the next pulse.
- Frame-sync pulse-width countdown: CLKG cycles are counted according to the McBSPi.MCBSPLP_SRGR1_REG[15:8] FWID bit field to control the width of each frame-sync pulse.

NOTE: The McBSP module cannot operate at an internal functional frequency faster than L4 interface frequency divided by 2. Choose an input clock frequency and a McBSPi.MCBSPLP_SRGR1_REG[7:0] CLKGDV value such that CLKG is less than or equal to L4 interface frequency divided by 2.

In addition to the 3-stage clock divider, the SRG has a frame-sync pulse detection and clock synchronization module that allows synchronization of the clock divide-down with an incoming frame-sync pulse on the mcbsp4_fsr pin. This feature is enabled or disabled with the McBSPi.MCBSPLP_SRGR2_REG[15] GSYNC bit.

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CLKG is used as source to generate the output clocks CLKX and CLKR when the McBSPi.MCBSPLP_PCR_REG[9] CLKXM/McBSPi.MCBSPLP_PCR_REG[8] CLKRM bit indicates that the clock is an output. The output CLKX/CLKR is generated according to the clock polarity setting (see Figure 23-131).

For information about preparing the SRG for operation, see Section 23.5.5, *McBSP Basic Programming Model*.

23.5.4.9.1 Clock Generation in the SRG

The SRG can produce a clock signal (CLKG) for use by the receiver, the transmitter, or both. Use of the SRG to drive clocking is controlled by the clock mode bits (McBSPi.MCBSPLP_PCR_REG[9] CLKXM and McBSPi.MCBSPLP_PCR_REG[8] CLKRM) and polarity mode bits (McBSPi.MCBSPLP_PCR_REG[1] CLKXP and McBSPi.MCBSPLP_PCR_REG[0] CLKRP).

When a clock mode bit is set to 1 (CLKRM = 1 for reception, CLKXM = 1 for transmission), the corresponding data clock (CLKR for reception, CLKX for transmission) is driven by the internal SRG output clock (CLKG) according to the polarity setting.

The effects of this setting on the McBSP module are partially affected by use of the digital loopback (DLB) mode, the analog loopback (ALB) mode, and by the synchronous receive/transmit setting, respectively, as described in Table 23-338. ALB mode is selected with the McBSPi.MCBSPLP_SPCR1_REG[15] ALB bit. DLB mode is selected with the McBSPi.MCBSPLP_XCCR_REG[5] DLB bit. The synchronous setting is controlled by input signals. These signals are defined by the control registers of the control module (for more information, see Chapter 18, *Control Module*).

When using the SRG as a clock source, ensure that the SRG is enabled (the McBSPi.MCBSPLP_SPCR2_REG[6] GRST bit is set to1).

Table 23-338. Effects of DLB and ALB Bits on Clock Modes

Mode Bit Settings		Effect
CLKRM=1	DLB = 0 and ALB = 0 (Digital and analog loopback mode disabled)	mcbsp1_clkr is an output pin driven by the SRG output clock (CLKG).
	DLB = 0 and ALB = 1 (Digital loopback mode disabled and analog loopback mode enabled)	mcbsp1_clkr is an output pin driven by the SRG output clock (CLKG). The receiver functional part internal clock is driven by the CLKX input signal provided by the mcbspi_clkx pin. The source of CLKX depends on the CLKXM bit. The receive frame synchronization is driven by the FSX input signal provided by the mcbspi_fsx pin. The receive data is driven by the DX input loopback pin (mcbspi_dx).
	DLB = 1 and ALB = 0 (Digital loopback mode enabled and analog loopback mode disabled)	The SRG and the frame-sync generator must be enabled. The internal transmit and receive clocks are driven by the SRG (CLKG having the appropriate CLKXP polarity). The transmit and receive frame-sync signals are driven by the FSG (having the appropriate FSXP polarity). The transmit data is connected to the DR input data. In digital loopback mode, no serial link activity is seen by the remote device.
	DLB = 1 and ALB = 1 (Reserved mode)	Undefined functionality.

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Table 23-338. Effects of DLB and ALB Bits on Clock Modes (continued)

Mode Bit Settings		Effect
CLKXM=1	DLB = 0 and ALB = 0 (Digital and analog loopback mode disabled)	mcbspi_clkx is an output pin driven by the SRG output clock (CLKG).
	DLB = 0 and ALB = 1 (Digital loopback mode disabled and analog loopback mode enabled)	mcbspi_clkx is an output pin driven by the SRG output clock (CLKG).
	DLB = 1 and ALB = 0 (Digital loopback mode enabled and analog loopback mode disabled)	The SRG and the frame-sync generator must be enabled. The internal transmit and receive clocks are driven by the SRG (CLKG having the appropriate CLKXP polarity). The transmit and receive frame-sync signals are driven by the FSG (having the appropriate FSXP polarity). The transmit data is connected to the DR input data. In digital loopback mode, no serial link activity is seen by the remote device.
	DLB = 1 and ALB = 1 (Reserved mode)	Undefined functionality
	CONTROL_MCBSPLP[30] ALBCTRLRX_CLKX bit = 1 (synchronous setting and DLB = 0 and ALB = 0)	CLKX is an output pin driven by the SRG output clock (CLKG). CLKR is connected to the CLKX.

23.5.4.9.2 Frame-Sync Generation in the SRG

The SRG can produce a frame-sync signal (FSG) for use by the receiver, the transmitter, or both.

For the receiver to use FSG for frame synchronization, make sure the McBSPi.MCBSPLP_PCR_REG[10] FSRM bit is set to 1. (When FSRM is set to 0, receive frame synchronization is supplied through the mcbsp4_fsr pin.)

For the transmitter to use FSG for frame synchronization, the following bits must be set:

- McBSPi.MCBSPLP_PCR_REG[11] FSXM = 1: This indicates that transmit frame synchronization is supplied by the McBSP module rather than from the mcbspi_fsx pin.
- McBSPi.MCBSPLP_SRGR2_REG[12] FSGM = 1: This indicates that when FSXM is set to 1, transmit frame synchronization is supplied by the SRG.

NOTE: When FSGM = 0 and FSXM = 1, the transmit frame-sync signal (FSX) is generated when XB is not empty. When FSGM = 0, the McBSPi.MCBSPLP_SRGR2_REG[11:0] FPER and McBSPi.MCBSPLP_SRGR1_REG[15:8] FWID bit fields are used to determine the frame-sync period and width (external FSX is gated by the buffer empty condition).

In either case, the SRG must be enabled (the McBSPi.MCBSPLP_SPCR2_REG[6] GRST bit is set to 1) and the frame-sync logic in the SRG must be enabled (the McBSPi.MCBSPLP_SPCR2_REG[7] FRST bit is set to 0).

23.5.4.9.2.1 Choosing the Width of the Frame-Sync Pulse

Each pulse on FSG has a programmable width. Program the McBSPi.MCBSPLP_SRGR1_REG[15:8] FWID bit field, and the resulting pulse width is (FWID + 1) CLKG cycles, where CLKG is the output clock of the SRG. The range is from 1 to 256 clock periods.

23.5.4.9.2.2 Controlling the Period Between the Starting Edges of Frame-Sync Pulses

The user can control the amount of time from the starting edge of one FSG pulse to the starting edge of the next FSG pulse. This period is controlled in one of two ways, depending on the configuration of the SRG:

- If the SRG is using an external input clock and the cBSPi.MCBSPLP_SRGR2_REG[15] GSYNC bit is set to 1, FSG pulses in response to an inactive-to-active transition on the mcbsp4_fsr pin. Thus, an external device controls the frame-sync period.

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- Otherwise, software programs the McBSPi.MCBSPLP_SRGR2_REG[11:0] FPER bit field, and the resulting frame-sync period is (FPER + 1) CLKG cycles, where CLKG is the output clock of the SRG. The range is from 1 to 4096 clock periods.

23.5.4.9.2.3 Keeping FSG Synchronized to an External Clock

When an external signal is selected to drive the SRG, the McBSPi.MCBSPLP_SRGR2_REG[15] GSYNC bit and the mcbsp4_fsr pin can be used to configure the timing of FSG pulses.

Setting the McBSPi.MCBSPLP_SRGR2_REG[15] GSYNC bit to 1 ensures that the McBSP module and an external device are dividing down the input clock with the same phase relationship.

If the McBSPi.MCBSPLP_SRGR2_REG[15] GSYNC bit is set to 1, an inactive-to-active transition on the mcbsp4_fsr pin triggers a resynchronization of CLKG and generation of FSG.

23.5.4.9.3 Synchronizing SRG Outputs to an External Clock

The SRG can produce a clock signal (CLKG) and an FSG based on an input clock signal that is either:

- The interface clock signal (MCBSPi_ICLK)
- The CLKS signal (PRCM functional clock or mcbsp_clks)
- A signal at the mcbsp4_clkr
- The mcbspi_clkx pin

When an external clock (mcbsp_clks, mcbsp4_clkr, or mcbspi_clkx) is selected to drive the SRG, the McBSPi.MCBSPLP_SRGR2_REG[15] GSYNC bit and the mcbsp4_fsr pin can be used to control the timing of CLKG and the pulsing of FSG relative to the chosen input clock. Set the GSYNC bit to 1 so that the McBSP module and an external device divide-down the input clock with the same phase relationship.

If the McBSPi.MCBSPLP_SRGR2_REG[15] GSYNC bit is set to 1:

- An inactive-to-active transition on the mcbsp4_fsr pin triggers a resynchronization of the CLKG signal and a pulsing of the FSG signal.
- The CLKG signal always begins with a high state after synchronization.
- The FSR signal is always detected at the same edge of the input clock signal that generates the CLKG signal, no matter how long the FSR pulse is.
- The McBSPi.MCBSPLP_SRGR2_REG[11:0] FPER bit field is ignored because the frame-sync period on FSG is determined by the arrival of the next frame-sync pulse on the mcbsp4_fsr pin.

If the McBSPi.MCBSPLP_SRGR2_REG[15] GSYNC bit is set to 0, the CLKG signal runs freely and is not resynchronized, and the frame-sync period on the FSG signal is determined by the McBSPi.MCBSPLP_SRGR2_REG[11:0] FPER bit field.

23.5.4.9.3.1 Operating the Transmitter Synchronously With the Receiver

When the McBSPi.MCBSPLP_SRGR2_REG[15] GSYNC bit is set to 1, the transmitter can operate synchronously with the receiver, provided that the FSX signal is programmed to be driven by the FSG signal (McBSPi.MCBSPLP_SRGR2_REG[12] FSGM = 1 and McBSPi.MCBSPLP_PCR_REG[11] FSXM = 1). If the FSR input signal has appropriate timing so that it can be sampled by the falling edge of the CLKG signal, it can be used, instead, by setting the McBSPi.MCBSPLP_PCR_REG[11] FSXM bit to 0 and connecting the FSR signal to FSX externally.

The SRG clock drives the transmit and receive clocking (the McBSPi.MCBSPLP_PCR_REG[8] CLKRM and McBSPi.MCBSPLP_PCR_REG[9] CLKXM bits are set to 1). Therefore, the CLK(R/X) pin must not be driven by any other driving source.

23.5.4.9.3.2 Synchronization Examples

Figure 23-145 and Figure 23-146 show the clock and frame-sync operation with various polarities of CLKS (the chosen input clock) and FSR signals. These figures assume McBSPi.MCBSPLP_SRGR1_REG[15:8] FWID = 0x0, for an FSG pulse that is one CLKG cycle wide. The McBSPi.MCBSPLP_SRGR2_REG[11:0] FPER bit field is not programmed; the period from the start of a frame-sync pulse to the start of the next pulse is determined by the arrival of the next inactive-to-active transition on the mcbsp4_fsr pin.

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Both figures show what happens to the CLKG signal when the McBSPi.MCBSPLP_SRGR2_REG[15] GSYNC bit is set to 1 and if it is initially synchronized or not initially synchronized. Figure 23-146 has a slower CLKG frequency (it has a larger divide-down value in the McBSPi.MCBSPLP_SRGR1_REG[7:0] CLKGDV bit field).

Figure 23-145. CLKG Synchronization and FSG Generation (GSYNC = 1 and CLKGDV = 0x1)

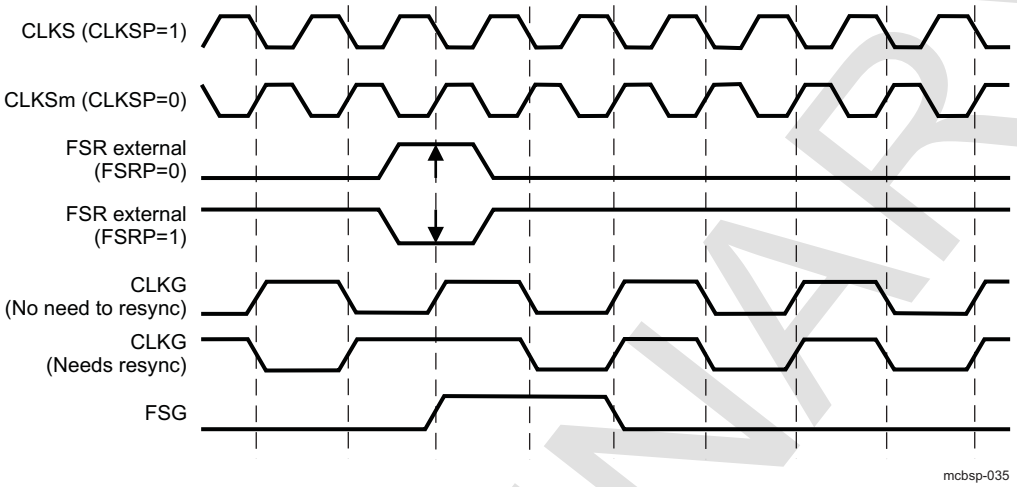
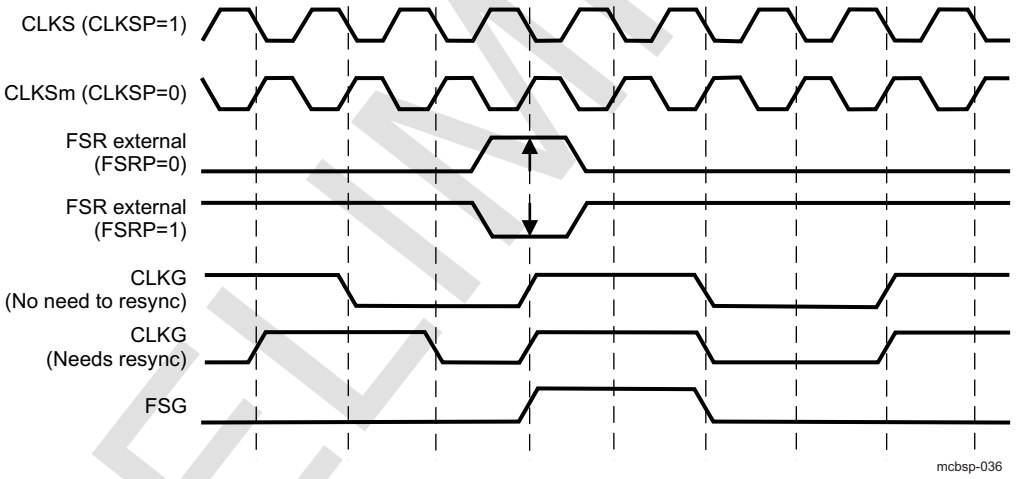


Figure 23-146. CLKG Synchronization and FSG Generation (GSYNC = 1 and CLKGDV = 0x3)



23.5.4.10 McBSP Exception/Error Conditions

23.5.4.10.1 Introduction

Several serial port events can constitute a system error. Any error condition can be a source of an interrupt:

- Receiver overrun (the McBSPi.MCBSPLP_IRQSTATUS_REG[5] ROVFLSTAT bit is set to 1, and the legacy mode McBSPi.MCBSPLP_SPCR1_REG[2] RFULL bit is set to 1)

  This occurs when the RB is full and the RSR is full with another new word shifted in from mcbspi_dr. Therefore, the McBSPi.MCBSPLP_IRQSTATUS_REG[5] ROVFLSTAT bit (McBSPi.MCBSPLP_SPCR1_REG[2] RFULL) indicates an error condition wherein any new data that can arrive at this time on mcbspi_dr replaces the contents of the RSR, and the previous word is lost. The RSR continues to be overwritten as long as new data arrives on mcbspi_dr and the McBSPi.MCBSPLP_DRR_REG register is not read. For more information about overrun in the receiver, see Section 23.5.4.10.2, *Overrun in the Receiver*.

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- Unexpected receive frame-sync pulse (the McBSPi.MCBSPLP_IRQSTATUS_REG[0] RSYNCERR bit is set to 1, and the legacy mode McBSPi.MCBSPLP_SPCR1_REG[3] RSYNCERR bit is set to 1)

  This occurs during reception when an unexpected frame-sync pulse arrives. An unexpected frame-sync pulse is one that is supposed to begin the next frame transfer before all the bits of the current frame are received. Such a pulse is ignored by the receiver, but sets the McBSPi.MCBSPLP_SPCR1_REG[3] RSYNCERR bit. For more information about receive frame-sync errors, see Section 23.5.4.10.3, *Unexpected Receive Frame-Sync Pulse*.
- Receiver underflow (the McBSPi.MCBSPLP_IRQSTATUS_REG[4] RUNDFLSTAT bit is set to 1)

  This occurs when the sDMA controller or MPU/DSP subsystem reads data from an empty receive buffer. For more information about underflow in the receiver, see Section 23.5.4.10.4, *Underflow in the Receiver*.
- Transmitter underflow (the McBSPi.MCBSPLP_IRQSTATUS_REG[11] XUNDFLSTAT bit is set to 1, and the legacy mode McBSPi.MCBSPLP_SPCR2_REG[2] XEMPTY bit is set to 0)

  If a new frame-sync signal arrives when the XB is empty, the previous data in the XSR is re-sent. This procedure continues for every new frame-sync pulse that arrives until the McBSPi.MCBSPLP_DXR_REG register is loaded with new data (and the XB is no longer empty). For more information about underflow in the transmitter, see Section 23.5.4.10.5, *Underflow in the Transmitter*.
- Unexpected transmit frame-sync pulse (the McBSPi.MCBSPLP_IRQSTATUS_REG[7] XSYNCERR bit is set to 1, and the legacy mode McBSPi.MCBSPLP_SPCR2_REG[3] XSYNCERRbit is set to 1)

  This occurs during transmission when an unexpected frame-sync pulse arrives. An unexpected frame-sync pulse is one that is supposed to begin the next frame transfer before all the bits of the current frame are transferred. Such a pulse is ignored by the transmitter, but sets the McBSPi.MCBSPLP_SPCR2_REG[3] XSYNCERR bit. For more information, see Section 23.5.4.10.6, *Unexpected Transmit Frame-Sync Pulse*.
- Transmitter overflow (the McBSPi.MCBSPLP_IRQSTATUS_REG[12] XOVFLSTAT bit is set to 1)

  This occurs when the sDMA controller or MPU/DSP subsystem writes data to a full XB. For more information about underflow in the receiver, see Section 23.5.4.10.7, *Overflow in the Transmitter*.

23.5.4.10.2 Overrun in the Receiver

When the McBSPi.MCBSPLP_IRQSTATUS_REG[5] ROVFLSTAT bit is set to 1, and the McBSPi.MCBSPLP_SPCR1_REG[2] RFULL bit is set to 1 (legacy mode) indicates that the receiver has experienced overrun and is in an error condition. Receive overrun is set when all of the following conditions are met:

1. McBSPi.MCBSPLP_DRR_REG is not read even if the McBSPi.MCBSPLP_IRQSTATUS_REG[3] RRDY bit is set (legacy mode) and DMA or interrupt request has been asserted.
2. RB is full.
3. RSR is full.

As previously described, data arriving on mcbspi_dr is continuously shifted into the RSR. Once a complete word is shifted into the RSR, an RSR-to-RB copy can occur only if the RB is not full.

Either of the following events clears the legacy mode McBSPi.MCBSPLP_SPCR1_REG[2] RFULL bit and allows subsequent transfers to be read properly:

- The MPU/DSP subsystems or sDMA controller reads the McBSPi.MCBSPLP_DRR_REG register.
- The receiver is reset individually (the McBSPi.MCBSPLP_SPCR1_REG[0] RRST bit is set to 0) or as part of a global reset.

Another frame-sync pulse is required to restart the receiver.

According to the McBSPi.MCBSPLP_IRQENABLE_REG register setting, this condition can generate the MCBSPi_IRQ line to be asserted low. Writing 1 to the corresponding bit in the McBSPi.MCBSPLP_IRQSTATUS_REG register clears the interrupt.

Figure 23-147 shows the receive overrun condition.

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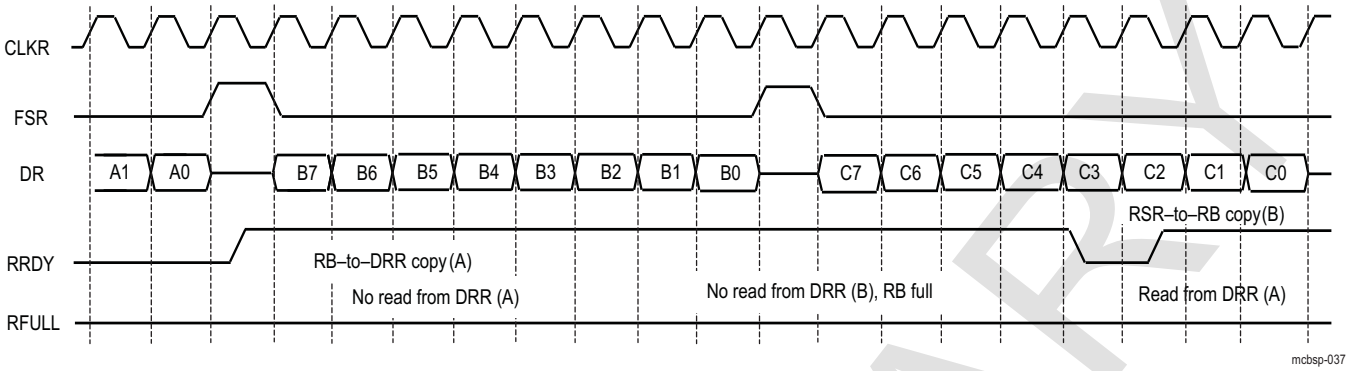
Figure 23-147. Overrun in the McBSP Receiver



23.5.4.10.3 Unexpected Receive Frame-Sync Pulse

23.5.4.10.3.1 Possible Responses to Receive Frame-Sync Pulses

If a frame-sync pulse starts the transfer of a new frame before the current frame is fully received, this pulse is treated as an unexpected frame-sync pulse, and the receiver sets the receive frame-sync error bit McBSPi.MCBSPLP_IRQSTATUS_REG[0] RSYNCERR (and the legacy McBSPi.MCBSPLP_SPCR1_REG[3] RSYNCERR bit).

According to the settings of the McBSPi.MCBSPLP_IRQENABLE_REG register, this condition can generate the MCBSPi_IRQ line to be asserted low. Writing 1 to the corresponding bit in the McBSPi.MCBSPLP_IRQSTATUS_REG register clears the interrupt.

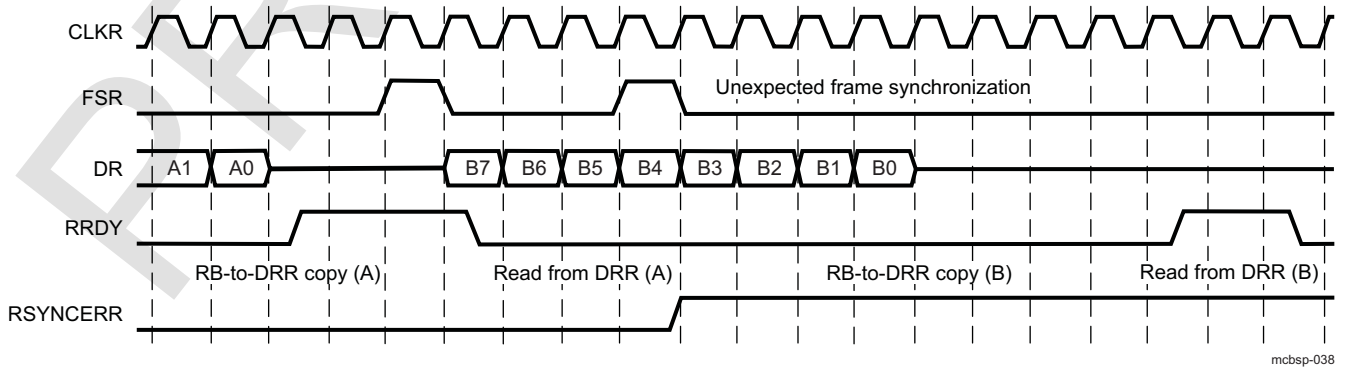
Using the legacy mode, the McBSPi.MCBSPLP_SPCR1_REG[3] RSYNCERR bit can be cleared only by a receiver reset or by setting this bit to 0. For the McBSP module to notify the MPU/DSP subsystem of receive frame-sync errors, set the legacy mode receive interrupt with the McBSPi.MCBSPLP_SPCR1_REG[5:4] RINTM bit field. When RINTM is set to 0b11, the McBSP module sends a receive interrupt (legacy mode) request to the MPU/DSP subsystems each time that RSYNCERR is set.

23.5.4.10.3.2 Example of an Unexpected Receive Frame-Sync Pulse

Figure 23-148 shows an unexpected receive frame-sync pulse during normal operation of the serial port with time intervals between data packets.

NOTE: The unexpected receive frame-sync pulse does not influence the data receive process, being ignored by the data receive state-machine.

Figure 23-148. Unexpected Frame-Sync Pulse During a McBSP Reception



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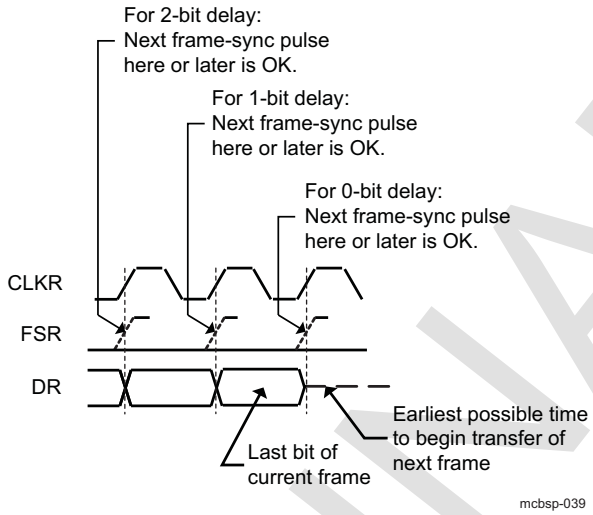
23.5.4.10.3.3 Preventing Unexpected Receive Frame-Sync Pulses

Each frame transfer can be delayed by 0, 1, or 2 CLKR cycles, depending on the value of the McBSPi.MCBSPLP_RCR2_REG[1:0] RDATDLY bit field. For each possible data delay, Figure 23-149 shows when a new frame-sync pulse on FSR can safely occur relative to the last bit of the current frame.

Figure 23-149. Proper Positioning of Receive Frame-Sync Pulses



23.5.4.10.4 Underflow in the Receiver

The McBSP module indicates a receiver underflow condition by setting the McBSPi.MCBSPLP_IRQSTATUS_REG[4] RUNDFLSTAT bit. This error occurs when sDMA controller or MPU/DSP subsystem reads data from an empty RB this happens only if the MPU/DSP subsystem or sDMA controller does not respect the DMA length, does not wait for DMA request, or does not check the buffer status before reading data. According to the McBSPi.MCBSPLP_IRQENABLE_REG register settings this condition can generate the MCBSPi_IRQ line to be asserted low. Writing 1 to the corresponding bit in McBSPi.MCBSPLP_IRQSTATUS_REG register clears the interrupt.

23.5.4.10.5 Underflow in the Transmitter

The McBSP module indicates a transmitter empty (or underflow) condition by setting the McBSPi.MCBSPLP_IRQSTATUS_REG[11] XUNDFLSTAT bit. The legacy mode McBSPi.MCBSPLP_SPCR2_REG[2] XEMPTY bit is also cleared. Either of the following events activates the XEMPTY bit (XEMPTY = 0):

- The McBSPi.MCBSPLP_DXR_REG register has not been loaded and the XB is empty, and all bits of the data word in the XSR have been shifted out on the mcbspi_dx pin.
- The transmitter is reset (by forcing McBSPi.MCBSPLP_SPCR2_REG[0] XRST to 0, or by a global reset) and is then restarted.

The XEMPTY bit is deactivated (XEMPTY = 1) when a new word in the McBSPi.MCBSPLP_DXR_REG register is transferred to the XB. If the McBSPi.MCBSPLP_PCR_REG[11] FSXM bit is set to 1 and the McBSPi.MCBSPLP_SRGR2_REG[12] FSGM bit is set to 0, the FSX signal is generated when the XB is not empty. When the McBSPi.MCBSPLP_SRGR2_REG[12] FSGM bit is set to 0, the McBSPi.MCBSPLP_SRGR2_REG[11:0] FPER and McBSPi.MCBSPLP_SRGR1_REG[15:8] FWID bit fields are used to determine the frame-sync period and width (external FSX is gated by the buffer empty condition). Otherwise, the transmitter waits for the next frame-sync pulse before sending the next frame on the mcbspi_dx pin.

When the transmitter is taken out of reset (the cBSPi.MCBSPLP_SPCR2_REG[0] XRST bit is set to 1), it is in a transmitter ready state (the McBSPi.MCBSPLP_SPCR2_REG[1] XRDY bit is set to 1) and transmitter empty (the McBSPi.MCBSPLP_SPCR2_REG[2] XEMPTY bit is set to 0) state. If the

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McBSPi.MCBSPLP_DXR_REG register is loaded by the MPU/DSP subsystem or the sDMA controller before internal the FSX goes active high, a valid XB-to-XSR transfer occurs. This allows for the first word of the first frame to be valid even before the transmit frame-sync pulse is generated or detected. Alternatively, if a transmit frame-sync pulse is detected before McBSPi.MCBSPLP_DXR_REG is loaded, zeros are output on the mcbspi_dx pin.

The McBSPi.MCBSPLP_IRQSTATUS_REG[11] XUNDFLSTAT bit indicates a real underflow condition, in which the frame is corrupted due to lack of data availability during the transmit process. According to the settings of the McBSPi.MCBSPLP_IRQENABLE_REG register, this condition can generate the MCBSPi_IRQ line to be asserted low. Writing 1 to the corresponding bit in McBSPi.MCBSPLP_IRQSTATUS_REG register clears the interrupt.

23.5.4.10.6 Unexpected Transmit Frame-Sync Pulse

23.5.4.10.6.1 Possible Responses to Transmit Frame-Sync Pulses

If a frame-sync pulse starts the transfer of a new frame before the current frame is fully transmitted, this pulse is treated as an unexpected frame-sync pulse, and the transmitter sets the transmit frame-sync error bit McBSPi.MCBSPLP_IRQSTATUS_REG[7] XSYNCERR (and the legacy McBSPi.MCBSPLP_SPCR2_REG[3] XSYNCERR bit).

According to the settings of the McBSPi.MCBSPLP_IRQENABLE_REG register, this condition can generate the MCBSPi_IRQ line to be asserted low. Writing 1 to the corresponding bit in the status register clears the interrupt.

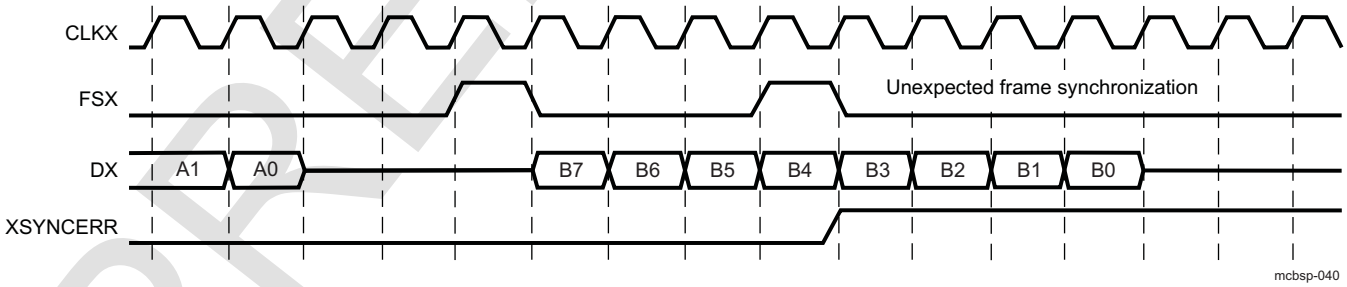
Using the legacy mode, the McBSPi.MCBSPLP_SPCR2_REG[3] XSYNCERR bit can be cleared only by a transmitter reset or by setting this bit to 0. For the McBSP module to notify the MPU/DSP subsystem of frame-sync errors, set a special transmit interrupt mode with the McBSPi.MCBSPLP_SPCR2_REG[5:4] XINTM bit field. When XINTM is set to 0b11, the McBSP module sends a transmit interrupt request to the MPU/DSP subsystem each time XSYNCERR is set.

23.5.4.10.6.2 Example of Unexpected Transmit Frame-Sync Pulse

Figure 23-150 shows an unexpected transmit frame-sync pulse during normal operation of the serial port with intervals between the data packets.

NOTE: The unexpected transmit frame-sync pulse does not influence the data transmit process, being ignored by the data transmit state-machine.

Figure 23-150. Unexpected Frame-Sync Pulse During a McBSP Transmission



23.5.4.10.6.3 Preventing Unexpected Transmit Frame-Sync Pulses

Each frame transfer can be delayed by 0, 1, or 2 CLKX cycles, depending on the value in the McBSPi.MCBSPLP_XCR2_REG[1:0] XDATDLY bit field. For each possible data delay, Figure 23-151 shows when a new frame-sync pulse on FSX can safely occur relative to the last bit of the current frame.

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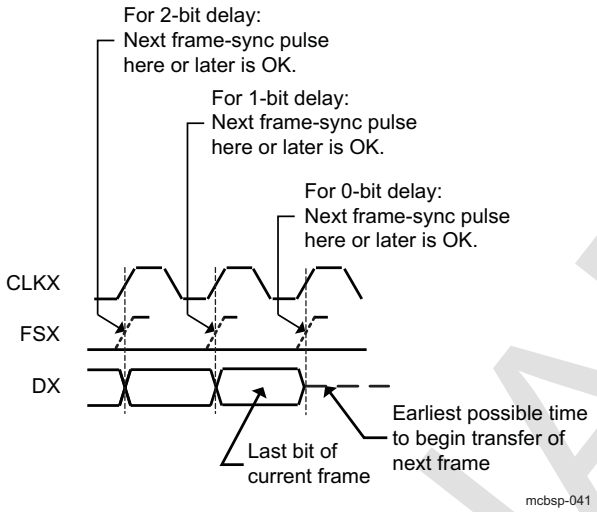
Figure 23-151. Proper Positioning of Transmit Frame-Sync Pulses



23.5.4.10.7 Overflow in the Transmitter

The McBSP module indicates a transmitter overflow condition by setting the McBSPi.MCBSPLP_IRQSTATUS_REG[12] XOVFLSTAT bit. This error occurs when the sDMA controller or MPU/DSP subsystem writes data to a full XB (this happens only if the MPU/DSP subsystem or sDMA controller does not respect the DMA length, does not wait for DMA request, or does not check the buffer status before writing data). According to the settings of the McBSPi.MCBSPLP_IRQENABLE_REG register, this condition can generate the MCBSPi_IRQ line to be asserted low. Writing 1 to the corresponding bit in the status register clears the interrupt.

23.5.4.11 McBSP DMA Configuration

The McBSP receive and transmit data DMA requests are active after the receive McBSPi.MCBSPLP_SPCR1_REG[0] RRST and transmit McBSPi.MCBSPLP_SPCR2_REG[0] XRST bits are released. After reset the default DMA threshold (and length) is one.

The receive and transmit DMA requests can be individually disabled by setting the McBSPi.MCBSPLP_RCCR_REG[3] RDMAEN and McBSPi.MCBSPLP_XCCR_REG[3] XDMAEN bits to 0. When disabling the DMA, the DMA request line is deasserted even if a DMA transfer is pending and the DMA state-machine is not reset.

The DMA threshold and length configuration is done through the McBSPi.MCBSPLP_THRSH1_REG and McBSPi.MCBSPLP_THRSH2_REG registers as follows:

- (THRSH1_REG + 1) value represents the required receive DMA request length (the length of the transfer is the same as the threshold value plus 1). As long as the RB occupied locations level is greater than or equal to the THRSH1_REG value + 1, the DMA request is asserted. After transferring the configured (THRSH1_REG + 1) number of words, the receive DMA request is de-asserted and reasserted as soon as the conditions are met again.
- (THRSH2_REG + 1) value represents the required transmit DMA request length (the length of the transfer is the same as the threshold value plus 1). As long as the XB free locations level is greater than or equal to the THRSH2_REG value + 1, the DMA request is asserted. After transferring the configured (THRSH2_REG + 1) number of words, the transmit DMA request is deasserted and reasserted as soon as the conditions are met.

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NOTE: The MPU/DSP subsystem can decide not to use the DMA to transfer the data. In this case, the DMA must be disabled (or the DMA request can be ignored by MPU/DSP subsystem) and the common interrupt line (MCBSPi_IRQ) can be used. The McBSPi.MCBSPLP_SPCR1_REG[1] RRDY bit for receive and the McBSPi.MCBSPLP_SPCR2_REG[1] XRDY bit for transmit indicate when the threshold values are reached. Also, by reading the receive buffer status McBSPi.MCBSPLP_RBUFFSTAT_REG register and transmit buffer status McBSPi.MCBSPLP_XBUFFSTAT_REG register, the MPU/DSP subsystem can decide to transfer data even if the threshold is not reached. This mechanism is useful on the last transfer on the receive side when the threshold value is bigger than the occupied locations inside the receive buffer and the MPU/DSP subsystem needs to read this data. Because no interrupt or DMA request is asserted, the only option in this case is to read the value of the RB status register and to transfer the remaining data without using the DMA or interrupt indication.

23.5.4.12 Multichannel Selection Modes

23.5.4.12.1 Channels, Blocks and Partitions

A McBSP channel is a time slot for shifting in/out the bits of one serial word. The McBSP module supports up to 128 channels for reception and 128 channels for transmission. In the receiver and in the transmitter, the 128 available channels are divided into eight blocks that contain 16 contiguous channels each (see Table 23-339).

Table 23-339. McBSP Channels

Block 0: Channels 0–15	**Block 4: Channels 64–79**
Block 1: Channels 16–31	**Block 5: Channels 80–95**
Block 2: Channels 32–47	**Block 6: Channels 96–111**
Block 3: Channels 48–63	**Block 6: Channels 112–127**

The blocks are assigned to partitions according to the selected partition mode. In the 2-partition mode described in Section 23.5.4.12.6, *Using Two Partitions (Legacy Only)*, assign one even-numbered block (0, 2, 4, or 6) to partition A and one odd-numbered block (1, 3, 5, or 7) block to partition B. In the 8-partition mode described in Section 23.5.4.12.4, *Using Eight Partitions*, blocks 0 through 7 are automatically assigned to partitions A through H, respectively.

The number of partitions for reception and the number of partitions for transmission are independent of one another. For example, it is possible to use two receive partitions (A and B) and eight transmit partitions (A–H).

23.5.4.12.2 Multichannel Selection

When a McBSP module uses a time-division multiplexed (TDM) data stream while communicating with other McBSP modules or serial devices, the McBSP module may need to receive and/or transmit on only a few channels. To save memory and bus bandwidth, use a multichannel selection mode to prevent data flow in some of the channels.

Each channel partition has a dedicated channel enable register. If the appropriate multichannel selection mode is on, each bit in the register controls whether data flow is allowed or prevented in one of the channels that is assigned to that partition.

The McBSP module has one receive multichannel selection mode (see Section 23.5.4.12.5, *Receive Multichannel Selection Mode*) and three transmit multichannel selection modes (see Section 23.5.4.12.7, *Transmit Multichannel Selection Modes*).

23.5.4.12.3 Configuring a Frame for Multichannel Selection

Before enabling a multichannel selection mode, ensure that the data frame is properly configured:

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- Select a single-phase frame (the McBSPi.MCBSPLP_RCR2_REG[15] RPHASE and McBSPi.MCBSPLP_XCR2_REG[15] XPHASE bits are set to 0). Each frame represents a TDM data stream.
- Set a frame length (in the McBSPi.MCBSPLP_RCR1_REG[14:8] RFRLEN1 and McBSPi.MCBSPLP_XCR1_REG[14:8] XFRLEN1 bit fields) that includes the highest numbered channel to be used. For example, to use channels 0, 15, and 39 for reception, the receive frame length must be at least 40 (RFRLEN1 = 39). In this case, If XFRLEN1= 39, the receiver creates 40 time slots per frame but receives data only during time slots 0, 15, and 39 of each frame.

23.5.4.12.4 Using Eight Partitions

For multichannel selection operation in the receiver and/or transmitter, eight partitions or two partitions (as previously described) can be used. If 8-partition mode (McBSPi.MCBSPLP_MCR1_REG[9] RMCME = 1 for reception, and McBSPi.MCBSPLP_MCR2_REG[9] XMCME = 1 for transmission) is selected, McBSP channels are activated in the following order: A, B, C, D, E, F, G, H.

In response to a frame-sync pulse, the receiver or transmitter begins with the channels in partition A and then continues with the other partitions, in order, until the complete frame is transferred. When the next frame-sync pulse occurs, the next frame is transferred, beginning with the channels in partition A.

In 8-partition mode, the McBSPi.MCBSPLP_MCR1_REG[6:5] RPABLK/McBSPi.MCBSPLP_MCR2_REG[6:5] XPABLK bit fields, and the McBSPi.MCBSPLP_MCR1_REG[8:7] RPBBLK/McBSPi.MCBSPLP_MCR2_REG[8:7] XPBBLK bit fields are ignored and the 16-channel blocks are assigned to the partitions as shown in Table 23-340 and Table 23-341. These assignments cannot be changed. The tables also show the registers used to control the channels in the partitions.

Table 23-340. Eight Partitions – Receive Channel Assignment and Control

Receive Partition	Assigned Block of Receive Channels	Register Used for Channel Control
A	Block 0: Channels 0–15	McBSPi.MCBSPLP_RCERA_REG
B	Block 1: Channels 16–31	McBSPi.MCBSPLP_RCERB_REG
C	Block 2: Channels 32–47	McBSPi.MCBSPLP_RCERC_REG
D	Block 3: Channels 48–63	McBSPi.MCBSPLP_RCERD_REG
E	Block 4: Channels 64–79	McBSPi.MCBSPLP_RCERE_REG
F	Block 5: Channels 80–95	McBSPi.MCBSPLP_RCERF_REG
G	Block 6: Channels 96–111	McBSPi.MCBSPLP_RCERG_REG
H	Block 7: Channels 112–127	McBSPi.MCBSPLP_RCERH_REG

Table 23-341. Eight Partitions – Transmit Channel Assignment and Control

Transmit Partition	Assigned Block of Receive Channels	Register Used for Channel Control
A	Block 0: Channels 0–15	McBSPi.MCBSPLP_XCERA_REG
B	Block 1: Channels 16–31	McBSPi.MCBSPLP_XCERB_REG
C	Block 2: Channels 32–47	McBSPi.MCBSPLP_XCERC_REG
D	Block 3: Channels 48–63	McBSPi.MCBSPLP_XCERD_REG
E	Block 4: Channels 64–79	McBSPi.MCBSPLP_XCERE_REG
F	Block 5: Channels 80–95	McBSPi.MCBSPLP_XCERF_REG
G	Block 6: Channels 96–111	McBSPi.MCBSPLP_XCERG_REG
H	Block 7: Channels 112–127	McBSPi.MCBSPLP_XCERH_REG

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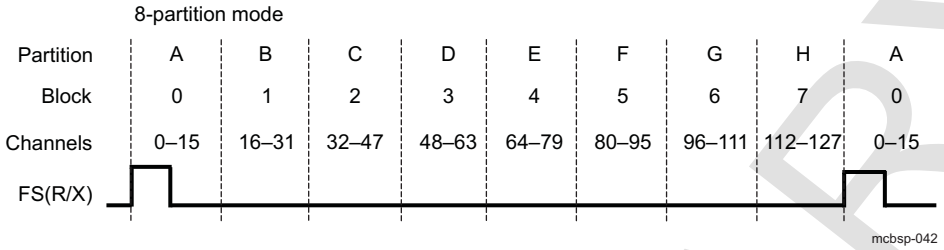
Figure 23-152 shows an example of the McBSP using 8-partition mode. In response to a frame-sync pulse, the McBSP module begins a frame transfer with partition A and then activates B, C, D, E, F, G, and H to complete a 128-word frame.

Figure 23-152. McBSP Data Transfer in 8-Partition Mode



23.5.4.12.5 Receive Multichannel Selection Mode

The McBSPi.MCBSPLP_MCR1_REG[0] RMCM bit determines whether all channels or only selected channels are enabled for reception.

- When RMCM = 0, all 128 receive channels are enabled and cannot be disabled.
- When RMCM = 1, the receive multichannel selection mode is enabled. In this mode:
  - Channels can be individually enabled or disabled. The enabled channels are those selected in the appropriate receive channel enable registers (McBSPi.MCBSPLP_RCERA_REG/McBSPi.MCBSPLP_RCERH_REG). The channels assigned to the McBSPi.MCBSPLP_RCERA_REG/McBSPi.MCBSPLP_RCERH_REG registers depend on the number of receive channel partitions (2 or 8), as defined by the McBSPi.MCBSPLP_MCR1_REG[9] RMCME bit.
  - If a receive channel is disabled, any bits received in that channel are not transferred to the RB, and as a result, the receiver ready bit (RRDY) is not set. Therefore, no DMA synchronization event is generated and, if the receiver interrupt mode depends on RRDY (McBSPi.MCBSPLP_SPCR1_REG[5:4] RINTM = 0b00), no interrupt is generated.

As an example of how the McBSP module behaves in the receive multichannel selection mode, suppose only channels 0, 15, and 39 are enabled and that the frame length is 40. The McBSP module:

1. Accepts bits shifted in from the mcbspi_dr pin in channel 0
2. Ignores bits received in channels 1–14
3. Accepts bits shifted in from the mcbspi_dr pin in channel 15
4. Ignores bits received in channels 16–38
5. Accepts bits shifted in from the mcbspi_dr pin in channel 39

23.5.4.12.6 Using Two Partitions (Legacy Only)

For multichannel selection operation in the receiver and/or the transmitter, two partitions or eight partitions can be used. If 2-partition mode (the McBSPi.MCBSPLP_MCR1_REG[9] RMCME bit is set to 0 for reception, and the McBSPi.MCBSPLP_MCR2_REG[9] XMCME bit is set to 0 for transmission) is selected, the McBSP channels are activated using an alternating scheme. In response to a frame-sync pulse, the receiver or transmitter begins with the channels in partition A and then alternates between partitions B and A until the complete frame is transferred. When the next frame-sync pulse occurs, the next frame is transferred beginning with the channels in partition A.

For reception, any two of the eight receive-channel blocks can be assigned to receive partitions A and B, which means up to 32 receive channels can be enabled at any given point. Similarly, any two of the eight transmit-channel blocks (up to 32 enabled transmit channels) can be assigned to transmit partitions A and B.

For reception:

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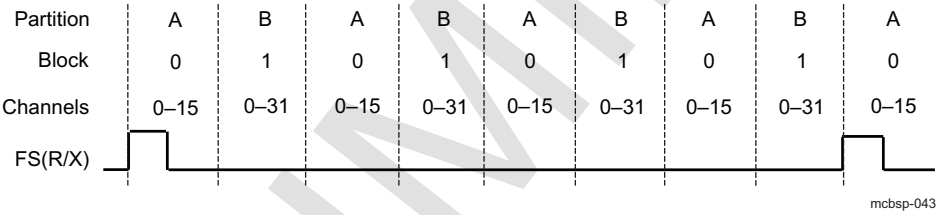
- Assign an even-numbered channel block (0, 2, 4, or 6) to receive partition A by writing to the McBSPi.MCBSPLP_MCR1_REG[6:5] RPABLK bit field. In the receive multichannel selection mode, the channels in this partition are controlled by receive channel enable register A (McBSPi.MCBSPLP_RCERA_REG).
- Assign an odd-numbered block (1, 3, 5, or 7) to receive partition B with the McBSPi.MCBSPLP_MCR1_REG[8:7] RPBBLK bit field. In the receive multichannel selection mode, the channels in this partition are controlled by receive channel enable register B (McBSPi.MCBSPLP_RCERB_REG).

For transmission:

- Assign an even-numbered channel block (0, 2, 4, or 6) to transmit partition A by writing to the McBSPi.MCBSPLP_MCR2_REG[6:5] XPABLK bit field. In one of the transmit multichannel selection modes, the channels in this partition are controlled by transmit channel enable register A (McBSPi.MCBSPLP_XCERA_REG).
- Assign an odd-numbered block (1, 3, 5, or 7) to transmit partition B with the McBSPi.MCBSPLP_MCR1_REG[8:7] XPBBLK bit field. In one of the transmit multichannel selection modes, the channels in this partition are controlled by transmit channel enable register B (McBSPi.MCBSPLP_XCERB_REG).

Figure 23-153 shows an example of alternating between the channels of partition A and the channels of partition B. Channels 0–15 have been assigned to partition A, and channels 16–31 have been assigned to partition B. In response to a frame-sync pulse, the McBSP module begins a frame transfer with partition A and then alternates between partitions B and A until the complete frame is transferred.

Figure 23-153. Alternating Between Partitions A and B Channels



23.5.4.12.7 Transmit Multichannel Selection Modes

The McBSPi.MCBSPLP_MCR2_REG[1:0] XMCM bit field determines whether all channels or only selected channels are enabled and unmasked for transmission. The McBSP module has three transmit multichannel selection modes (XMCM = 0b01, XMCM = 0b10, and XMCM = 0b11), which are described in Table 23-342.

Table 23-342. Selecting a Transmit Multichannel Selection Mode With the XMCM Bit Field

XMCM	Transmit Multichannel Selection Mode
0b00	No transmit multichannel selection mode is on. All channels are enabled and unmasked. No channels can be disabled or masked.
0b01	All channels are disabled unless they are selected in the appropriate transmit channel enable registers (McBSPi.MCBSPLP_XCERA_REG/McBSPi.MCBSPLP_XCERH_REG). If enabled, a channel in this mode is also unmasked. The McBSPi.MCBSPLP_MCR2_REG[9] XMCME bit determines whether 32 or 128 channels are selectable in the McBSPi.MCBSPLP_XCERA_REG/McBSPi.MCBSPLP_XCERH_REG registers.
0b10	All channels are enabled, but they are masked unless they are selected in the appropriate transmit channel enable registers (McBSPi.MCBSPLP_XCERA_REG/McBSPi.MCBSPLP_XCERH_REG). The McBSPi.MCBSPLP_MCR2_REG[9] XMCME bit determines whether 32 or 128 channels are selectable in the McBSPi.MCBSPLP_XCERA_REG/McBSPi.MCBSPLP_XCERH_REG registers.
0b11	This mode is used for symmetric transmission and reception. All channels are disabled for transmission unless they are enabled for reception in the appropriate receive channel enable registers (McBSPi.MCBSPLP_RCERA_REG/McBSPi.MCBSPLP_RCERH_REG). Once enabled, they are masked unless they are also selected in the appropriate transmit channel enable registers (McBSPi.MCBSPLP_XCERA_REG/McBSPi.MCBSPLP_XCERH_REG). The McBSPi.MCBSPLP_MCR2_REG[9] XMCME bit determines whether 32 or 128 channels are selectable in the McBSPi.MCBSPLP_RCERA_REG/McBSPi.MCBSPLP_RCERH_REG registers and the McBSPi.MCBSPLP_XCERA_REG/McBSPi.MCBSPLP_XCERH_REG registers.

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As an example of how the McBSP module behaves in a transmit multichannel selection mode, suppose that XMCM = 0b01 (all channels disabled unless individually enabled) and that only channels 0, 15, and 39 are enabled. Suppose also that the frame length is 40. The McBSP module:

1. Shifts data to the mcbspi_dx pin in channel 0
2. Places the mcbspi_dx pin in the high-impedance state in channels 1–14
3. Shifts data to the mcbspi_dx pin in channel 15
4. Places the mcbspi_dx pin in the high-impedance state in channels 16–38
5. Shifts data to the mcbspi_dx pin in channel 39

23.5.4.12.7.1 Disabling/Enabling Versus Masking/Unmasking

For transmission, a channel can be:

- Enabled and unmasked (transmission can begin and can be completed)
- Enabled but masked (transmission can begin but cannot be completed)
- Disabled (transmission cannot occur)

The definitions in Table 23-343 explain the channel control options:

Table 23-343. McBSP Channel Control Options

Enabled channel	A channel that can begin transmission by passing data from the data transmit register (McBSPi.MCBSPLP_DXR_REG) to the XSR through the XB.
Masked channel	A channel that cannot complete transmission. The mcbspi_dx pin is held in high-impedance state; data cannot be shifted out on the mcbspi_dx pin. In systems where symmetric transmit and receive provide software benefits, this feature allows transmit channels to be disabled on a shared serial bus. A similar feature is not needed for reception because multiple receptions cannot cause serial bus contention.
Disabled channel	A channel that is not enabled. A disabled channel is also masked. Because no DXR-to-XB copy occurs, the McBSPi.MCBSPLP_SPCR2_REG[1] XRDY bit is not set. Therefore, no DMA synchronization event is generated, and if the transmit interrupt mode depends on XRDY (McBSPi.MCBSPLP_SPCR2_REG[5:4] XINTM = 00b), no interrupt is generated. The McBSPi.MCBSPLP_SPCR2_REG[2] XEMPTY bit is not affected.
Unmasked channel	A channel that is not masked. Data in the XSR(s) is shifted out on the mcbspi_dx pin.

23.5.4.12.7.2 Activity on McBSP Pins for Different Values of XMCM

Figure 23-154 shows the activity on the McBSP pins for the various values of the McBSPi.MCBSPLP_MCR2_REG[1:0] XMCM bit field. In all cases, the transmit frame is configured as follows:

- XPHASE = 0: Single-phase frame (required for multichannel selection modes)
- XFRLEN1 = 0b0000011: 4 words per frame
- XWDLEN1 = 0b000: 8 bits per word
- XMCME = 0: 2-partition mode (only partitions A and B are used)

In the case where McBSPi.MCBSPLP_MCR2_REG[1:0] XMCM = 0b11, transmission and reception are symmetric, which means the corresponding bits for the receiver (RPHASE, RFRLEN1, RWDLEN1, and RMCME) must have the same values as XPHASE, XFRLEN1, and XWDLEN1, respectively.

In Figure 23-154, the arrows showing where the various events occur are only sample indications. Wherever possible, there is a time window in which these events can occur.

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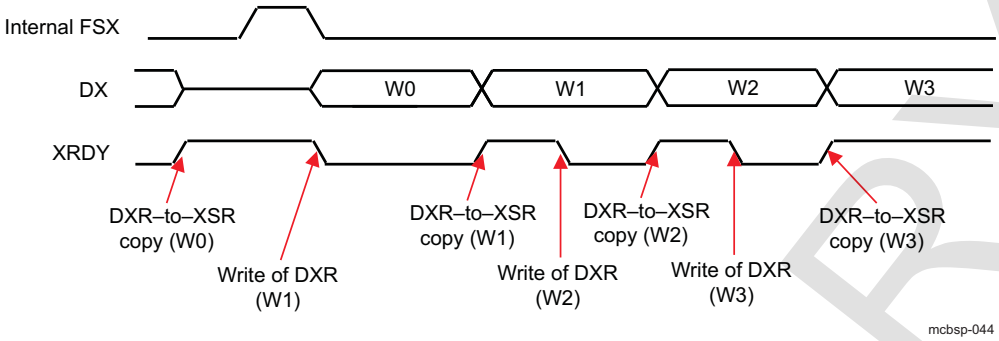
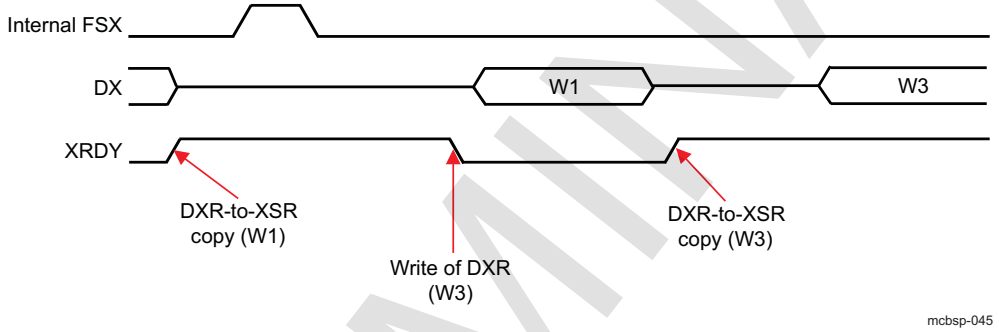
Figure 23-154. Activity on McBSP Pins When XMCM = 0b00



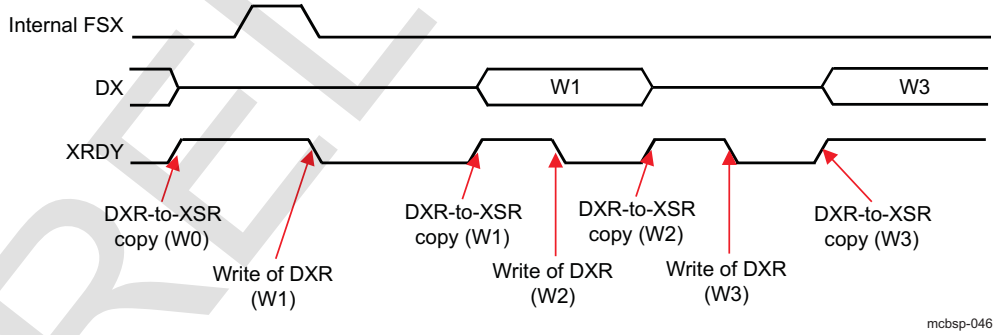
If XMCM = 0b00, all channels are enabled and unmasked. Words W0, W1, W2, and W3 are written to the XB, and then, from the XB, they are transferred by mcbspi_dx.

Figure 23-155. Activity on McBSP Pins When XMCM = 0b01



In Figure 23-155 if XMCM = 0b01, XPABLK = 0b00, and XCERA = 0b1010, only channels 1 and 3 are enabled and unmasked. Words W1 and W3 are written to the XB, and then, from the XB, they are transferred by mcbspi_dx.

Figure 23-156. Activity on McBSP Pins When XMCM = 0b10



In Figure 23-156 if XMCM = 0b10, XPABLK = 0b00, and XCERA = 0b1010, all channels are enabled, and only 1 and 3 are unmasked. Words W0, W1, W2, and W3 are written to the XB, but only W1 and W3, from the XB, are transferred by mcbspi_dx.

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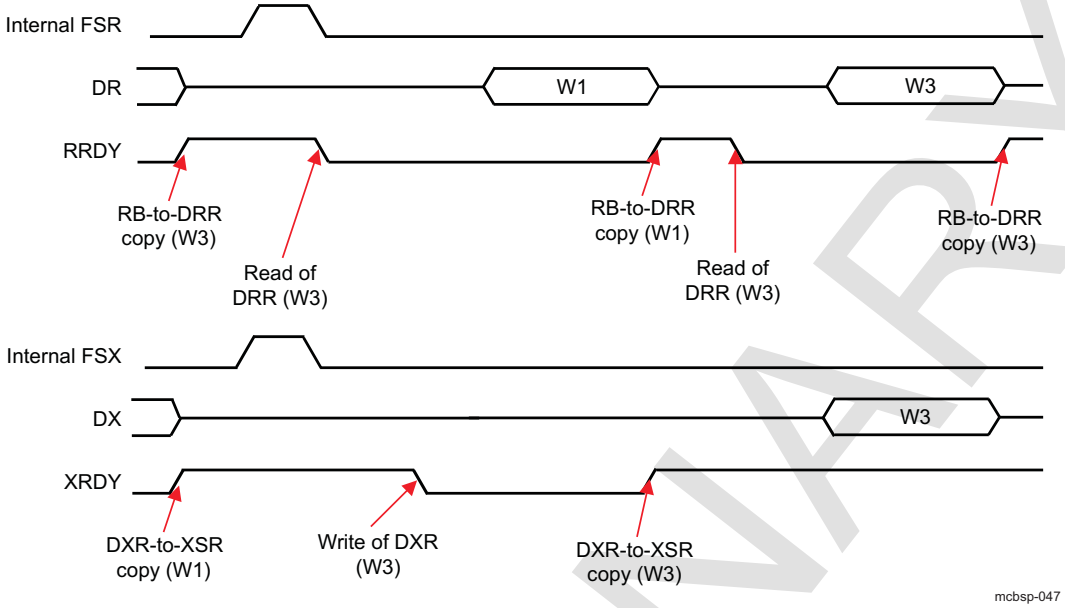
Figure 23-157. Activity on McBSP Pins When XMCM = 0b11



In Figure 23-157 if XMCM = 0b11, RPABLK = 0b00, XPABLK = 0bX, RCERA = 0b1010, and XCERA = 0b1000, channels 1 and 3 are enabled in receive and transmit mode, but only 3 is unmasked. Words W1 and W3 are written to the XB, but only W3, from the XB, is transferred by mcbspi_dx.

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23.5.5 McBSP Basic Programming Model

This section describes the programming model of a typical McBSP module.

CAUTION

For all descriptions in this section, the McBSPi.MCBSPLP_XCCR_REG[11] XFULL_CYCLE and McBSPi.MCBSPLP_RCCR_REG[11] RFULL_CYCLE bits are their reset value (XFULL_CYCLE is set to 0 and RFULL_CYCLE is set to 1).

23.5.5.1 McBSP Initialization Procedure

This procedure for reset/initialization can be applied in general when the receiver or transmitter must be reset during its normal operation, and also when the SRG is not used for either operation.

Figure 23-158 shows the serial port initialization procedure for master mode.

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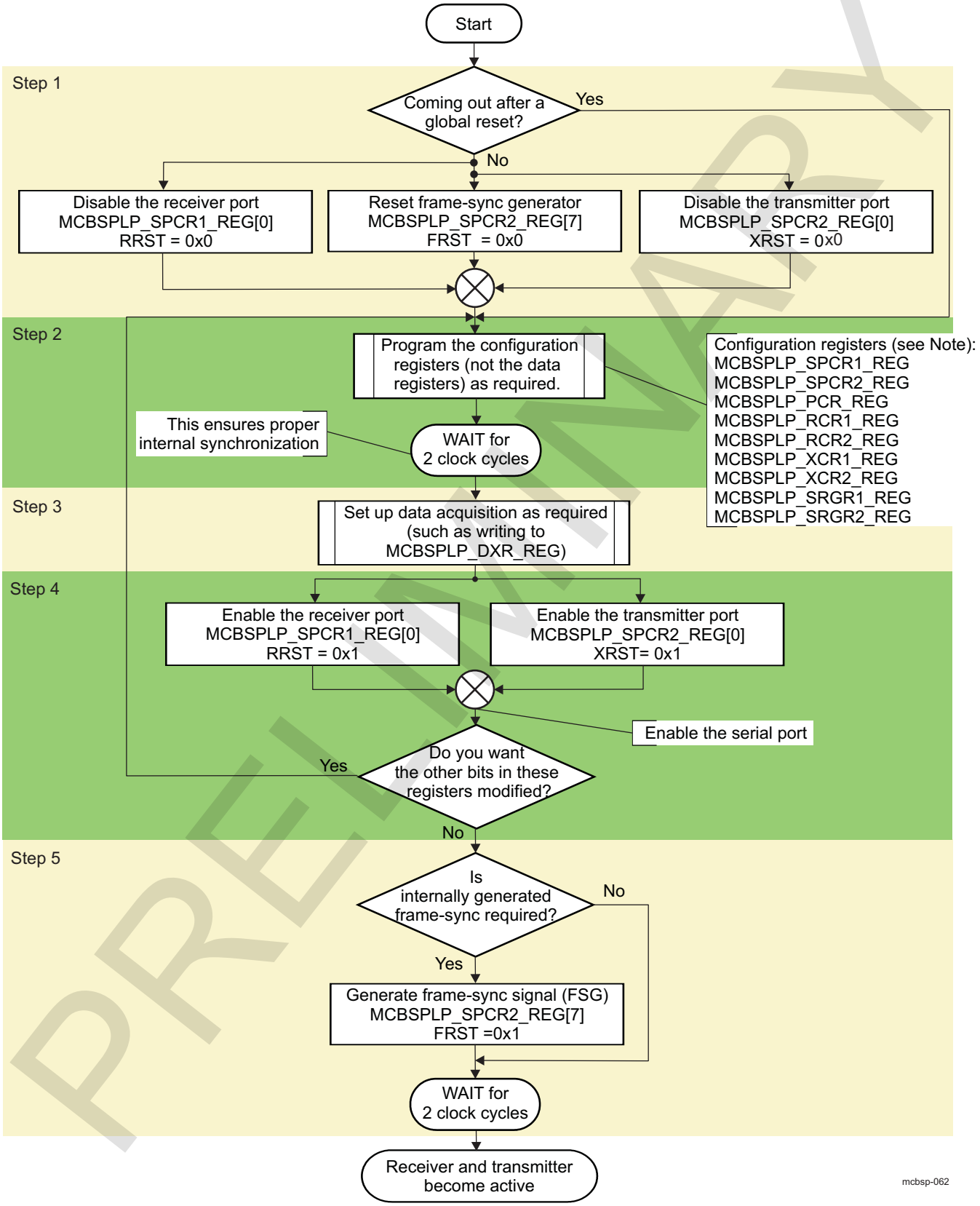
Figure 23-158. Flow Diagram of McBSP Initialization Procedure for Master Mode



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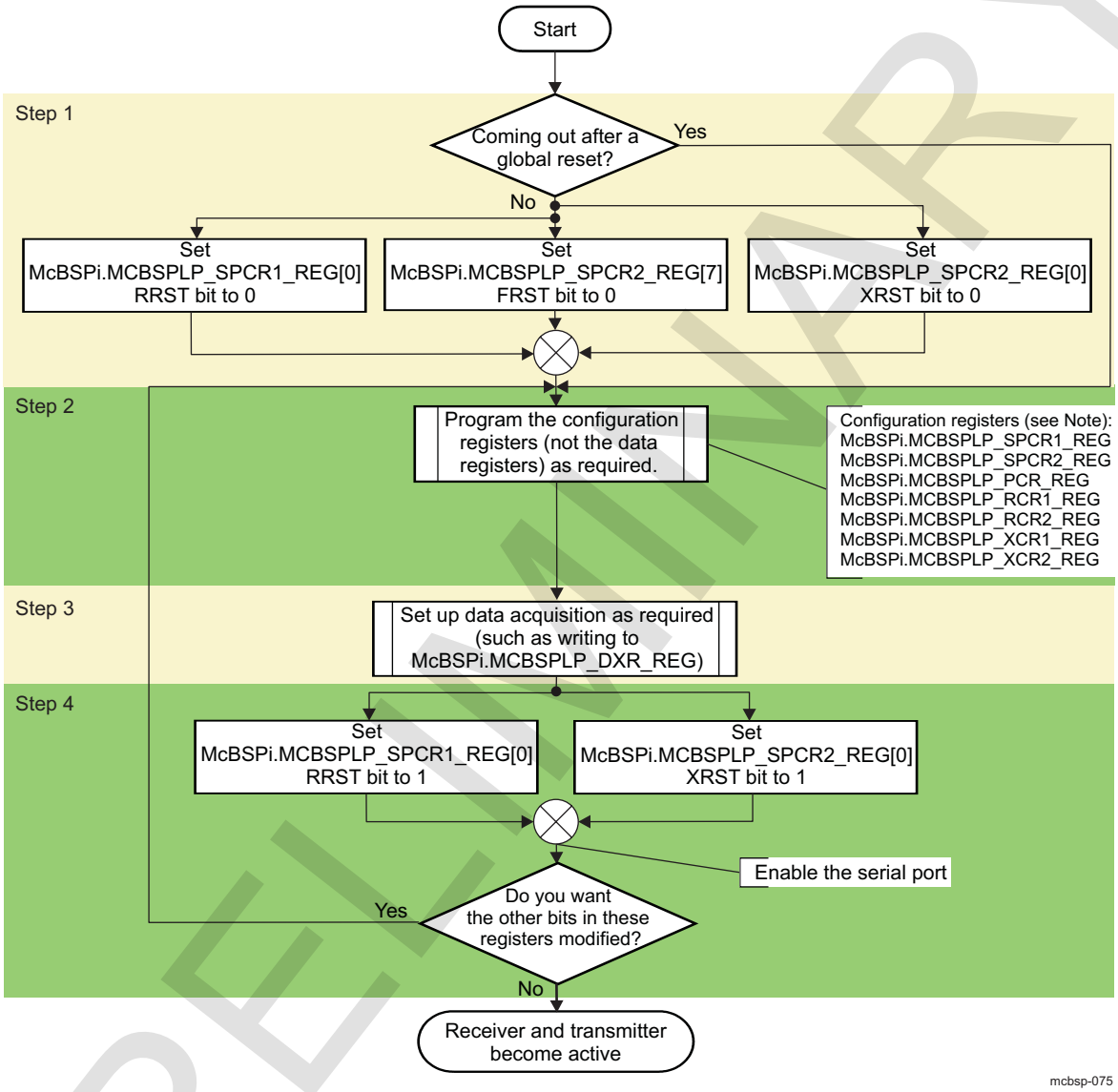
Alternatively, on write (Step 1 or Step 4), the transmitter and receiver can be placed in or taken out of reset by modifying the McBSPi.MCBSPLP_SPCR2_REG[0] XRST and McBSPi.MCBSPLP_SPCR1_REG[0] RRST bits, respectively.
Figure 23-159 shows the flow diagram of the McBSP initialization procedure for slave mode.

Figure 23-159. Flow Diagram of McBSP Initialization Procedure for Slave Mode



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NOTE:

- Alternatively, on write (Step 1 or Step 4), the transmitter and receiver can be placed in or taken out of reset by modifying the McBSPi.MCBSPLP_SPCR2_REG[0] XRST and McBSPi.MCBSPLP_SPCR1_REG[0] RRST bits, respectively.
- The necessary duration of the active-low period of XRST or RRST is at least two CLKR/CLKX cycles.
- The appropriate bits in serial port configuration registers (McBSPi.MCBSPLP_SPCR1_REG, McBSPi.MCBSPLP_SPCR2_REG, McBSPi.MCBSPLP_PCR_REG, McBSPi.MCBSPLP_RCR1_REG, McBSPi.MCBSPLP_RCR2_REG, McBSPi.MCBSPLP_XCR1_REG, McBSPi.MCBSPLP_XCR2_REG, McBSPi.MCBSPLP_THRSH2_REG, McBSPi.MCBSPLP_XCCR_REG, McBSPi.MCBSPLP_SYSCONFIG_REG, McBSPi.MCBSPLP_SRGR1_REG and McBSPi.MCBSPLP_SRGR2_REG) should be modified only when the affected portion of the serial port is in its reset state.
- In most cases, the data transmit register (McBSPi.MCBSPLP_DXR_REG) should be loaded by the MPU/DSP subsystem or the sDMA controller only when the transmitter is enabled (McBSPi.MCBSPLP_SPCR2_REG[0] XRST = 1). An exception to this rule is when these registers are used for loopback internal data.
- The bits of the channel control registers (McBSPi.MCBSPLP_MCR1_REG, McBSPi.MCBSPLP_MCR2_REG, McBSPi.MCBSPLP_RCER{A-H}_REG and McBSPi.MCBSPLP_XCER{A-H}_REG) can be modified at any time as long as they are not being used by the current reception/transmission in a multichannel selection mode.
- The SRG is reset by setting the McBSPi.MCBSPLP_SPCR2_REG[6] GRST bit to 0.
- It is not necessary to wait if SRG is not used.
- The necessary duration of the active-low period of XRST or RRST is at least two
- Modification on-the-fly has no effect if a reset is not performed first.

Table 23-344. Register Call Summary for Flow Diagram of McBSP Initialization Procedure

Register Name	Register Name	Register Name
MCBSPLP_SPCR1_REG	MCBSPLP_RCR1_REG	MCBSPLP_XCR2_REG
MCBSPLP_SPCR2_REG	MCBSPLP_RCR2_REG	MCBSPLP_SRGR1_REG
MCBSPLP_PCR_REG	MCBSPLP_XCR1_REG	MCBSPLP_SRGR2_REG

23.5.5.2 Reset and Initialization Procedure for the SRG

To reset and initialize the SRG:

1. Place the McBSP SRG in reset.
2. Program the registers that affect the SRG.
3. Enable the SRG (take it out of reset).
4. If necessary, enable the receiver and/or the transmitter.
5. If necessary, remove the receiver and/or transmitter from reset

Figure 23-160 shows the flow diagram for programming the SRG registers.

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Figure 23-160. Flow Diagram for the SRG Registers Programmation

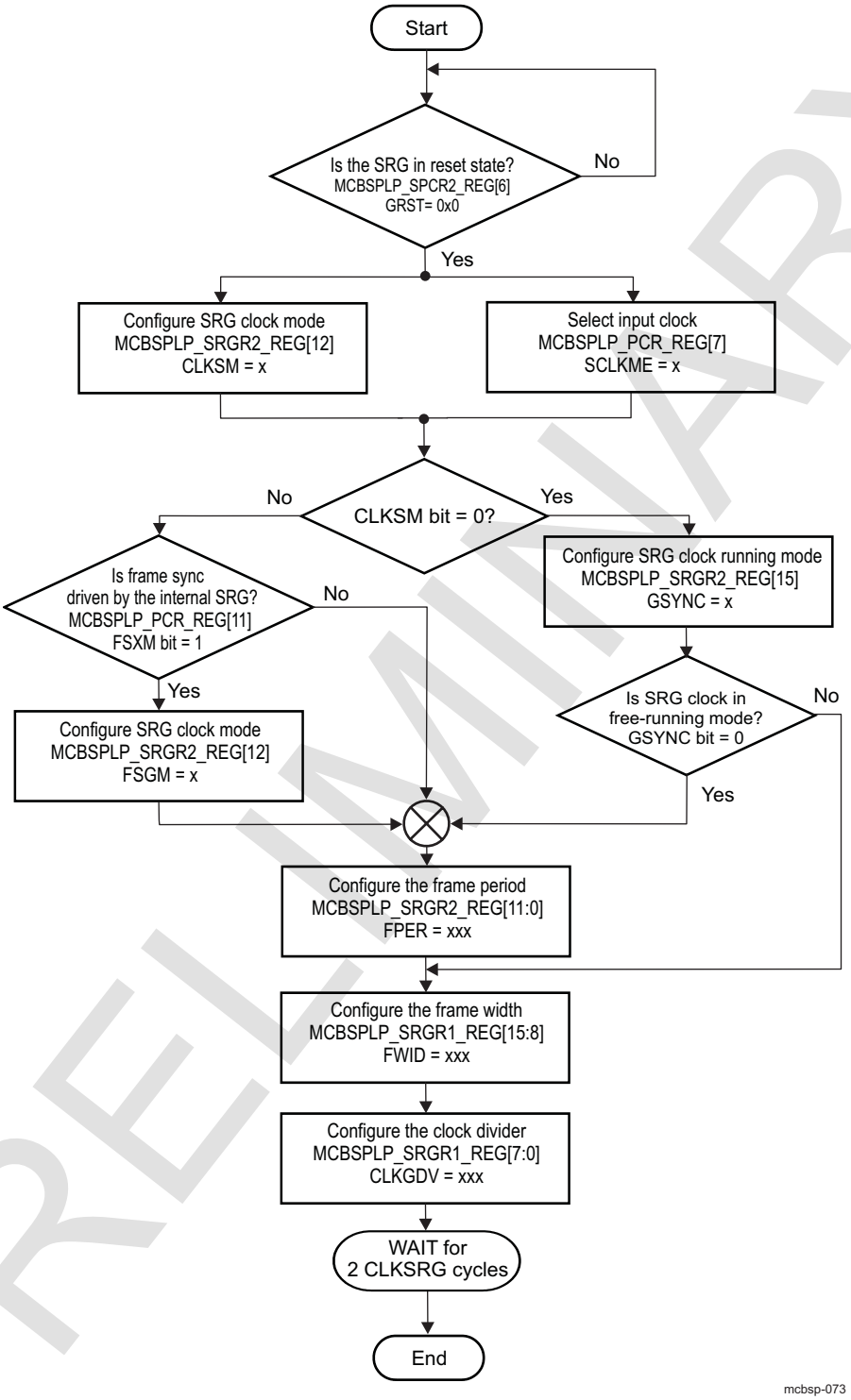

Table 23-345. Register Call Summary for Flow Diagram for the SRG Registers Programmation

Register Name	Register Name
MCBSPLP_SPCR2_REG	MCBSPLP_PCR_REG
MCBSPLP_SRGR2_REG	MCBSPLP_SRGR1_REG

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23.5.5.3 Data Transfer DMA Request Configuration

This procedure configures the McBSP receive/transmit data DMA requests (MCBSPi_DMA_RX and MCBSPi_DMA_TX) (see Table 23-346).

Table 23-346. Data Transfer DMA Request Configuration

Step	Register/Bit Field/Programming Model	Value
Write the required receive DMA request length.	MCBSPLP_THRSH1_REG[6:0] RTHRESHOLD	x..x
Write the required transmit DMA request length.	MCBSPLP_THRSH2_REG[6:0] RTHRESHOLD	x..x

NOTE:

- The length of the transfer is the same as the threshold value + 1
- In case of a number of transfers that exceed the number of the programmed DMA length, the McBSP module will respond to the command and will perform the transfer regardless of the receive buffer empty condition.
- In case of a number of transfers that exceed the number of the programmed DMA length, the McBSP module will respond to the command and will perform the transfer regardless of the transmit buffer full condition.

23.5.5.4 Interrupt Configuration

This procedure configures the common receive/transmit interrupt request line (see Table 23-347).

Table 23-347. Interruption Configuration

Step	Register/Bit Field/Programming Model	Value
Enable the required IRQ events.	MCBSPLP_IRQENABLE_REG	x..x

23.5.5.5 Receiver Configuration

To configure the McBSP receiver, perform the following steps:

Step 1. Place the McBSP receiver in reset.

Step 2. Program the McBSP registers for the desired receiver operation.

Step 3. Take the receiver out of reset.

23.5.5.5.1 Place the Receiver in Reset (Step 1)

Table 23-348. Receiver Reset

Step	Register/Bit Field/Programming Model	Value
Place the receiver in reset.	MCBSPLP_SPCR1_REG[0] RST	0x0

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23.5.5.5.2 Programming the McBSP Registers for the Desired Receiver Configuration (Step 2)

This section describes the steps to be performed when software configures the McBSP receiver.

Global Configuration

Table 23-349 describes the steps to perform the global configuration.

Table 23-349. Global Configuration

Step	Register/Bit Field/Programming Model	Value
Set the receiver pins to operate as McBSP pins.	MCBSPLP_PCR_REG[12] RIOEN	0x0
Enable/disable DLB mode(1).	MCBSPLP_XCCR_REG[5] DLB	0x0 or 0x1
Enable/disable ALB mode(1).	MCBSPLP_SPCR1_REG[5] ALB	0x0 or 0x1
Select the clock used in synchronous transmit-receive mode (McBSP4 only)(1).	CONTROL_MCBSPLP[30] ALBCTRLRX_CLKX	0x0 or 0x1
Select frame synchronization used in the synchronous transmit-receive mode (McBSP4 only)(1).	CONTROL_MCBSPLP[31] ALBCTRLRX_FSX	0x0 or 0x1
Enable/disable the receive multichannel selection Mode(1).	MCBSPLP_MCR1_REG[0] RMCM	0x0 or 0x1

(1) Software decision

NOTE: In DLB mode the SRG and frame-sync generator must be enabled to generate the CLKX and FSX signals.

Data Configuration

Table 23-350 describes the steps to perform the data configuration.

Table 23-350. Data Configuration

Step	Register/Bit Field/Programming Model	Value
Select single/dual-phase frame (1).	MCBSPLP_RCR2_REG[15] RPHASE	0x0 or 0x1
Set the receive word length(s) for phase 1(1).	MCBSPLP_RCR1_REG[7:5] RWDLEN1	xxx
Set the receive word length(s) for phase 2(1).	MCBSPLP_RCR2_REG[7:5] XWDLEN2	xxx
Set the receive frame length*.	MCBSPLP_RCR1_REG[14:8] RFRLEN1 MCBSPLP_RCR2_REG[14:8] RFRLEN2	xxx
Set the receive reverse mode(1).	MCBSPLP_RCR2_REG[4:3] RREVERSE	xx
Set the receive data delay(1).	MCBSPLP_RCR2_REG[1:0] RDATLY	xx
Set the receive sign-extension and justification mode(1).	MCBSPLP_SPCR1_REG[14:13] RJUST	xx
Enable the serial receiver port.	MCBSPLP_SPCR1_REG[0] RRST	0x1
Configure the receive buffer threshold value(1).	MCBSPLP_THRSH1_REG[6:0] RTHRESHOLD	x..x

(1) Software decision

NOTE:

- When dual-phase frame is selected, the number of words per phase must be set to 1.
- If a single-phase frame is selected, RWDLEN1 selects the length for every serial word received in the frame. If a dual-phase frame is selected, RWDLEN1 and RWDLEN2 must be set to select both lengths. These bits can have different values.
- If a dual-phase frame is selected, the frame length must be two words.

Frame-Sync Configuration

Table 23-351 describes the steps to perform the frame-sync configuration.

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Table 23-351. Frame-Sync Configuration

Step	Register/Bit Field/Programming Model	Value
Set the receive frame-sync mode(1).	MCBSPLP_PCR_REG[10] FSRM	0x0 or 0x1
Select SRG synchronization(1).	MCBSPLP_SRGR2_REG[15] GSYNC	0x0 or 0x1
Set the receive frame-sync polarity (1).	MCBSPLP_PCR_REG[2] FSRP	0x0 or 0x1
Set the SRG frame-sync period(1).	MCBSPLP_SRGR2_REG[11:0] FPER	x..x
Set the SRG frame-sync pulse width(1).	MCBSPLP_SRGR1_REG[15:8] FWID	x..x

(1) Software decision

Clock Configuration

Table 23-352 describes the steps to perform clock configuration.

Table 23-352. Clock Configuration

Step	Register/Bit Field/Programming Model	Value
Set the receive clock mode(1).	MCBSPLP_PCR_REG[8] CLKRM	0x0 or 0x1
Set the receive clock polarity(1).	MCBSPLP_PCR_REG[0] CLKRP	0x0 or 0x1
Set the SRG clock divide-down value(1).	MCBSPLP_SRGR1_REG[7:0] CLKGDV	x..x
Set the SRG clock synchronization mode(1).	MCBSPLP_SRGR2_REG[15] GSYNC	0x0 or 0x1
Set the SRG input clock mode(1).	MCBSPLP_PCR_REG[7] SCKLME MCBSPLP_SRGR2_REG[13] CLKSM	0x0 or 0x1
Set the SRG input clock polarity(1).	MCBSPLP_SRGR2_REG[14] CLKSP MCBSPLP_PCR_REG[1] CLKXP MCBSPLP_PCR_REG[0] CLKRP	0x0 or 0x1

(1) Software decision

NOTE: CLKRP = CLKXP in a system in which the same clock (internal or external) is used to clock the receiver and transmitter. The receiver uses the opposite edge as the transmitter to ensure valid setup and hold of data around this edge.

23.5.5.5.3 Take the Receiver Out of Reset (Step 3)

Table 23-353. Take the Receiver Out of Reset

Step	Register/Bit Field/Programming Model	Value
Enable the receiver.	MCBSPLP_SPCR1_REG[0] RST	0x1

23.5.5.6 Transmitter Configuration

To configure the McBSP transmitter, perform the following steps:

Step 1. Place the McBSP transmitter in reset.

Step 2. Program the McBSP registers for the desired transmitter operation.

Step 3. Take the transmitter out of reset.

23.5.5.6.1 Place the Transmitter in Reset (Step 1)

Table 23-354. Transmitter Reset

Step	Register/Bit Field/Programming Model	Value
Place the transmitter in reset.	MCBSPLP_SPCR2_REG[0] RST	0x0

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23.5.5.6.2 Programming the McBSP Registers for the Desired Transmitter Operation (Step 2)

This section describes the steps to be performed when software configures the McBSP transmitter.

Global Configuration

Table 23-355 describes the steps to perform the global configuration.

Table 23-355. Global Configuration

Step	Register/Bit Field/Programming Model	Value
Set the transmitter pins to operate as MCBSP pins.	MCBSPLP_PCR_REG[13] XIOEN	0x0
Enable/disable DLB mode(1).	MCBSPLP_XCCR_REG[5] DLB	0x0 or 0x1
Enable/disable ALB mode(1).	MCBSPLP_SPCR1_REG[5] ALB	0x0 or 0x1
Select clock used in the synchronous transmit-receive mode (McBSP4 only)(1).	CONTROL_MCBSPLP[30] ALBCTRLRX_CLKX	0x0 or 0x1
Select frame synchronization used in the synchronous transmit-receive mode (McBSP4 only)(1).	CONTROL_MCBSPLP[31] ALBCTRLRX_FSX	0x0 or 0x1
Enable/disable the transmit multichannel selection mode(1).	MCBSPLP_MCR1_REG[0] RMCM	0x0 or 0x1

(1) Software decision

Data Configuration

Table 23-356 describes the steps to perform the data configuration.

Table 23-356. Data Configuration

Step	Register/Bit Field/Programming Model	Value
Select single/dual-phase frame (1).	MCBSPLP_RCR2_REG[15] XPHASE	0x0 or 0x1
Set the transmit word length(s) for phase 1(1).	MCBSPLP_XCR1_REG[7:5] XWDLEN1	xxx
Set the transmit word length(s) for phase 2(1).	MCBSPLP_XCR2_REG[7:5] XWDLEN2	xxx
Set the transmit frame length(1).	MCBSPLP_XCR1_REG[14:8] XFRLEN1 MCBSPLP_XCR2_REG[14:8] XFRLEN2	xxx
Set the transmit reverse mode(1).	MCBSPLP_XCR2_REG[4:3] XREVERSE	xx
Set the transmit data delay(1).	MCBSPLP_XCR2_REG[1:0] XDATLY	xx
Set the extra delay (DX delay) mode(1).	MCBSPLP_SPCR1_REG[7] DXENA	xx
Select the inserted delay value(1).	MCBSPLP_XCCR_REG[13:12] DXENDLY	xx
Set the interrupt line.	MCBSPLP_IRQENABLE_REG	x..x
Configure the transmit buffer threshold value(1)	MCBSPLP_THRSH2_REG[6:0] XTHRESHOLD	x..x

(1) Software decision

NOTE:

- When dual-phase frame is selected, the number of words per phase must be set to 1.
- If a single-phase frame is selected, XWDLEN1 selects the length for every serial word transmit in the frame. If a dual–phase frame is selected, XWDLEN1 and XWDLEN2 must be set to select both lengths. These bits can have different values.
- If a dual-phase frame is selected, the frame length must be two words.

The DXENA bit controls the delay enabler on the mcbsp_dx pin. Set DXENA to enable an extra delay for turn-on time. Because this bit does not control the data itself, only the first bit is delayed (the delay is given by a combinatorial delay buffer). The inserted delay, 80 ps, 160 ps (default), 240 ps, or 320 ps, can be set using the McBSPi.MCBSPLP_XCCR_REG[13:12] DXENDLY bit field. If the mcbsp_dx pins of multiple McBSP modules are tied together, ensure that DXENA is set to 1 to avoid having more than one McBSP at a time transmitting on the data line.

Frame-Sync Configuration

Table 23-357 describes the steps to perform the frame-sync configuration.

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Table 23-357. Frame-Sync Configuration

Step	Register / Bit Field / Programming Model	Value
Set the transmit frame-sync mode(1).	MCBSPLP_PCR_REG[11] FSXM MCBSPLP_SRGR2_REG[12] FSGM	0x0 or 0x1
Set the transmit frame-sync polarity(1).	MCBSPLP_PCR_REG[3] FSXP	0x0 or 0x1
Set the SRG frame-sync period(1).	MCBSPLP_SRGR2_REG[11:0] FPER	x..x
Set the SRG frame-sync pulse width(1).	MCBSPLP_SRGR1_REG[15:8] FWID	x..x

(1) Software decision

Clock Configuration

Table 23-358 describes the steps to perform the clock configuration.

Table 23-358. Clock Configuration

Step	Register / Bit Field / Programming Model	Value
Set the transmit clock mode (1).	MCBSPLP_PCR_REG[9] CLKXM	0x0 or 0x1
Set the transmit clock polarity(1).	MCBSPLP_PCR_REG[1] CLKXP	0x0 or 0x1
Set the SRG clock divide-down value(1).	MCBSPLP_SRGR1_REG[7:0] CLKGDV	x..x
Set the SRG clock synchronization mode(1).	MCBSPLP_SRGR2_REG[15] GSYNC	0x0 or 0x1
Set the SRG input clock mode(1).	MCBSPLP_PCR_REG[7] SCKLME MCBSPLP_SRGR2_REG[13] CLKSM	0x0 or 0x1
Set the SRG input clock polarity(1)	MCBSPLP_SRGR2_REG[14] CLKSP MCBSPLP_PCR_REG[1] CLKXP MCBSPLP_PCR_REG[0] CLKRP	0x0 or 0x1

(1) Software decision

NOTE: CLKRP = CLKXP in a system in which the same clock (internal or external) is used to clock the receiver and transmitter. The receiver uses the opposite edge as the transmitter to ensure valid setup and hold of data around this edge.

23.5.5.6.3 Take the Receiver Out of Reset (Step 3)

Table 23-359. Take the Receiver Out of Reset

Step	Register/Bit Field/Programming Model	Value
Enable the transmitter.	MCBSPLP_SPCR2_REG[0] RST	0x1

23.5.5.7 GPIO on the McBSP Pins (Legacy Only)

To use McBSP pins as GPIO pins rather than as serial port pins, follow these steps:

- **For the receive pins (mcbsp_clkr, mcbsp_fsr, and mcbsp_dr as)**

Table 23-360. Use Serial Receive Pins as GPIO Pins

Step	Register/Bit Field/Programming Model	Value
Place the receiver in reset.	MCBSPLP_SPCR1_REG[0] RRST	0x0
Enable GPIO for the serial port receiver.	MCBSPLP_PCR_REG[12] RIOEN	0x1

- **For the transmitter pins (mcbsp_clkx, mcbsp_fsx, and mcbsp_dx)**

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Table 23-361. Use Serial Transmit Pins as GPIO Pins

Step	Register/Bit Field/ Programming Model	Value
Place the transmit in reset.	MCBSPLP_SPCR2_REG[0] XRST	0x0
Enable GPIO for the serial port transmitter.	MCBSPLP_PCR_REG[12] XIOEN	0x1

- **For the external clock pins (mcbsp_clks)**

  For the mcbsp_clks pin (common to all McBSP modules), all of the reset and I/O conditions must be met as follows:

Table 23-362. Use External Clock Pin as GPIO Pin

Step	Register/Bit Field/Programming Model	Value
Place the receiver in reset.	MCBSPLP_SPCR1_REG[0] RRST	0x0
Place the transmit in reset.	MCBSPLP_SPCR2_REG[0] XRST	0x0
Enable GPIO for the serial port receiver.	MCBSPLP_PCR_REG[12] RIOEN	0x1
Enable GPIO for the serial port transmitter.	MCBSPLP_PCR_REG[12] XIOEN	0x1

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23.5.6 MCBSP Register Manual

Table 23-363 shows the base address and address space for the device module instances.

23.5.6.1 MCBSP Instance Summary

Table 23-363. MCBSP Instance Summary

Module Name	Base Address L3 Interconnect	Base Address Cortex-A9 Private Access	Base Address DSP Private Access	Base Address L4-PER Interconnect	Size
MCBSP1	0x4902 2000	0x4012 2000	0x2 2000	N/A	4KB
MCBSP2	0x4902 4000	0x4012 4000	0x2 4000	N/A	4KB
MCBSP3	0x4902 6000	0x4012 6000	0x2 6000	N/A	4KB
MCBSP4	N/A	N/A	N/A	0x4809 6000	4KB

NOTE: Private access is an access that does not use the L3/L4 interconnects.

23.5.6.2 MCBSP Registers

CAUTION

The McBSP registers are limited to 32-bit data accesses; 16- and 8-bit accesses are not allowed and can corrupt register content.

23.5.6.2.1 MCBSP Register Summary

Table 23-364 through Table 23-367 summarize the MCBSP1, MCBSP2, MCBSP3, and MCBSP4 registers, respectively.

Table 23-364. MCBSP1 Register Summary

Register Name	Type	Register Width (Bits)	Address Offset	Physical Address L3 Interconnect	Physical Address Cortex-A9 Private Access	Physical Address DSP Private Access
MCBSPLP_DRR_REG	R	32	0x0000 0000	0x4902 2000	0x4012 2000	0x2 2000
MCBSPLP_DXR_REG	W	32	0x0000 0008	0x4902 2008	0x4012 2008	0x2 2008
MCBSPLP_SPCR2_REG	RW	32	0x0000 0010	0x4902 2010	0x4012 2010	0x2 2010
MCBSPLP_SPCR1_REG	RW	32	0x0000 0014	0x4902 2014	0x4012 2014	0x2 2014
MCBSPLP_RCR2_REG	RW	32	0x0000 0018	0x4902 2018	0x4012 2018	0x2 2018
MCBSPLP_RCR1_REG	RW	32	0x0000 001C	0x4902 201C	0x4012 201C	0x2 201C
MCBSPLP_XCR2_REG	RW	32	0x0000 0020	0x4902 2020	0x4012 2020	0x2 2020
MCBSPLP_XCR1_REG	RW	32	0x0000 0024	0x4902 2024	0x4012 2024	0x2 2024
MCBSPLP_SRGR2_REG	RW	32	0x0000 0028	0x4902 2028	0x4012 2028	0x2 2028
MCBSPLP_SRGR1_REG	RW	32	0x0000 002C	0x4902 202C	0x4012 202C	0x2 202C
MCBSPLP_MCR2_REG	RW	32	0x0000 0030	0x4902 2030	0x4012 2030	0x2 2030
MCBSPLP_MCR1_REG	RW	32	0x0000 0034	0x4902 2034	0x4012 2034	0x2 2034
MCBSPLP_RCERA_REG	RW	32	0x0000 0038	0x4902 2038	0x4012 2038	0x2 2038
MCBSPLP_RCERB_REG	RW	32	0x0000 003C	0x4902 203C	0x4012 203C	0x2 203C
MCBSPLP_XCERA_REG	RW	32	0x0000 0040	0x4902 2040	0x4012 2040	0x2 2040
MCBSPLP_XCERB_REG	RW	32	0x0000 0044	0x4902 2044	0x4012 2044	0x2 2044
MCBSPLP_PCR_REG	RW	32	0x0000 0048	0x4902 2048	0x4012 2048	0x2 2048
MCBSPLP_RCERC_REG	RW	32	0x0000 004C	0x4902 204C	0x4012 204C	0x2 204C

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Table 23-364. MCBSP1 Register Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	Physical Address L3 Interconnect	Physical Address Cortex-A9 Private Access	Physical Address DSP Private Access
MCBSPLP_RCERD_REG	RW	32	0x0000 0050	0x4902 2050	0x4012 2050	0x2 2050
MCBSPLP_XCERC_REG	RW	32	0x0000 0054	0x4902 2054	0x4012 2054	0x2 2054
MCBSPLP_XCERD_REG	RW	32	0x0000 0058	0x4902 2058	0x4012 2058	0x2 2058
MCBSPLP_RCERE_REG	RW	32	0x0000 005C	0x4902 205C	0x4012 205C	0x2 205C
MCBSPLP_RCERF_REG	RW	32	0x0000 0060	0x4902 2060	0x4012 2060	0x2 2060
MCBSPLP_XCERE_REG	RW	32	0x0000 0064	0x4902 2064	0x4012 2064	0x2 2064
MCBSPLP_XCERF_REG	RW	32	0x0000 0068	0x4902 2068	0x4012 2068	0x2 2068
MCBSPLP_RCERG_REG	RW	32	0x0000 006C	0x4902 206C	0x4012 206C	0x2 206C
MCBSPLP_RCERH_REG	RW	32	0x0000 0070	0x4902 2070	0x4012 2070	0x2 2070
MCBSPLP_XCERG_REG	RW	32	0x0000 0074	0x4902 2074	0x4012 2074	0x2 2074
MCBSPLP_XCERH_REG	RW	32	0x0000 0078	0x4902 2078	0x4012 2078	0x2 2078
MCBSPLP_REV_REG	R	32	0x0000 007C	0x4902 207C	0x4012 207C	0x2 207C
MCBSPLP_RINTCLR_REG	RW	32	0x0000 0080	0x4902 2080	0x4012 2080	0x2 2080
MCBSPLP_XINTCLR_REG	RW	32	0x0000 0084	0x4902 2084	0x4012 2084	0x2 2084
MCBSPLP_ROVFLCLR_REG	RW	32	0x0000 0088	0x4902 2088	0x4012 2088	0x2 2088
MCBSPLP_SYSCONFIG_REG	RW	32	0x0000 008C	0x4902 208C	0x4012 208C	0x2 208C
MCBSPLP_THRSH2_REG	RW	32	0x0000 0090	0x4902 2090	0x4012 2090	0x2 2090
MCBSPLP_THRSH1_REG	RW	32	0x0000 0094	0x4902 2094	0x4012 2094	0x2 2094
MCBSPLP_IRQSTATUS_REG	RW	32	0x0000 00A0	0x4902 20A0	0x4012 20A0	0x2 20A0
MCBSPLP_IRQENABLE_REG	RW	32	0x0000 00A4	0x4902 20A4	0x4012 20A4	0x2 20A4
MCBSPLP_WAKEUPEN_REG	RW	32	0x0000 00A8	0x4902 20A8	0x4012 20A8	0x2 20A8
MCBSPLP_XCCR_REG	RW	32	0x0000 00AC	0x4902 20AC	0x4012 20AC	0x2 20AC
MCBSPLP_RCCR_REG	RW	32	0x0000 00B0	0x4902 20B0	0x4012 20B0	0x2 20B0
MCBSPLP_XBUFFSTAT_REG	R	32	0x0000 00B4	0x4902 20B4	0x4012 20B4	0x2 20B4
MCBSPLP_RBUFFSTAT_REG	R	32	0x0000 00B8	0x4902 20B8	0x4012 20B8	0x2 20B8

Table 23-365. MCBSP2 Register Summary

Register Name	Type	Register Width (Bits)	Address Offset	Physical Address L3 Interconnect	Physical Address Cortex-A9 Private Access	Physical Address DSP Private Access
MCBSPLP_DRR_REG	R	32	0x0000 0000	0x4902 4000	0x4012 4000	0x2 4000
MCBSPLP_DXR_REG	W	32	0x0000 0008	0x4902 4008	0x4012 4008	0x2 4008
MCBSPLP_SPCR2_REG	RW	32	0x0000 0010	0x4902 4010	0x4012 4010	0x2 4010
MCBSPLP_SPCR1_REG	RW	32	0x0000 0014	0x4902 4014	0x4012 4014	0x2 4014
MCBSPLP_RCR2_REG	RW	32	0x0000 0018	0x4902 4018	0x4012 4018	0x2 4018
MCBSPLP_RCR1_REG	RW	32	0x0000 001C	0x4902 401C	0x4012 401C	0x2 401C
MCBSPLP_XCR2_REG	RW	32	0x0000 0020	0x4902 4020	0x4012 4020	0x2 4020
MCBSPLP_XCR1_REG	RW	32	0x0000 0024	0x4902 4024	0x4012 4024	0x2 4024
MCBSPLP_SRGR2_REG	RW	32	0x0000 0028	0x4902 4028	0x4012 4028	0x2 4028
MCBSPLP_SRGR1_REG	RW	32	0x0000 002C	0x4902 402C	0x4012 402C	0x2 402C
MCBSPLP_MCR2_REG	RW	32	0x0000 0030	0x4902 4030	0x4012 4030	0x2 4030
MCBSPLP_MCR1_REG	RW	32	0x0000 0034	0x4902 4034	0x4012 4034	0x2 4034

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Table 23-365. MCBSP2 Register Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	Physical Address L3 Interconnect	Physical Address Cortex-A9 Private Access	Physical Address DSP Private Access
MCBSPLP_RCERA_REG	RW	32	0x0000 0038	0x4902 4038	0x4012 4038	0x2 4038
MCBSPLP_RCERB_REG	RW	32	0x0000 003C	0x4902 403C	0x4012 403C	0x2 403C
MCBSPLP_XCERA_REG	RW	32	0x0000 0040	0x4902 4040	0x4012 4040	0x2 4040
MCBSPLP_XCERB_REG	RW	32	0x0000 0044	0x4902 4044	0x4012 4044	0x2 4044
MCBSPLP_PCR_REG	RW	32	0x0000 0048	0x4902 4048	0x4012 4048	0x2 4048
MCBSPLP_RCERC_REG	RW	32	0x0000 004C	0x4902 404C	0x4012 404C	0x2 404C
MCBSPLP_RCERD_REG	RW	32	0x0000 0050	0x4902 4050	0x4012 4050	0x2 4050
MCBSPLP_XCERC_REG	RW	32	0x0000 0054	0x4902 4054	0x4012 4054	0x2 4054
MCBSPLP_XCERD_REG	RW	32	0x0000 0058	0x4902 4058	0x4012 4058	0x2 4058
MCBSPLP_RCERE_REG	RW	32	0x0000 005C	0x4902 405C	0x4012 405C	0x2 405C
MCBSPLP_RCERF_REG	RW	32	0x0000 0060	0x4902 4060	0x4012 4060	0x2 4060
MCBSPLP_XCERE_REG	RW	32	0x0000 0064	0x4902 4064	0x4012 4064	0x2 4064
MCBSPLP_XCERF_REG	RW	32	0x0000 0068	0x4902 4068	0x4012 4068	0x2 4068
MCBSPLP_RCERG_REG	RW	32	0x0000 006C	0x4902 406C	0x4012 406C	0x2 406C
MCBSPLP_RCERH_REG	RW	32	0x0000 0070	0x4902 4070	0x4012 4070	0x2 4070
MCBSPLP_XCERG_REG	RW	32	0x0000 0074	0x4902 4074	0x4012 4074	0x2 4074
MCBSPLP_XCERH_REG	RW	32	0x0000 0078	0x4902 4078	0x4012 4078	0x2 4078
MCBSPLP_REV_REG	R	32	0x0000 007C	0x4902 407C	0x4012 407C	0x2 407C
MCBSPLP_RINTCLR_REG	RW	32	0x0000 0080	0x4902 4080	0x4012 4080	0x2 4080
MCBSPLP_XINTCLR_REG	RW	32	0x0000 0084	0x4902 4084	0x4012 4084	0x2 4084
MCBSPLP_ROVFLCLR_REG	RW	32	0x0000 0088	0x4902 4088	0x4012 4088	0x2 4088
MCBSPLP_SYSCONFIG_REG	RW	32	0x0000 008C	0x4902 408C	0x4012 408C	0x2 408C
MCBSPLP_THRSH2_REG	RW	32	0x0000 0090	0x4902 4090	0x4012 4090	0x2 4090
MCBSPLP_THRSH1_REG	RW	32	0x0000 0094	0x4902 4094	0x4012 4094	0x2 4094
MCBSPLP_IRQSTATUS_REG	RW	32	0x0000 00A0	0x4902 40A0	0x4012 40A0	0x2 40A0
MCBSPLP_IRQENABLE_REG	RW	32	0x0000 00A4	0x4902 40A4	0x4012 40A4	0x2 40A4
MCBSPLP_WAKEUPEN_REG	RW	32	0x0000 00A8	0x4902 40A8	0x4012 40A8	0x2 40A8
MCBSPLP_XCCR_REG	RW	32	0x0000 00AC	0x4902 40AC	0x4012 40AC	0x2 40AC
MCBSPLP_RCCR_REG	RW	32	0x0000 00B0	0x4902 40B0	0x4012 40B0	0x2 40B0
MCBSPLP_XBUFFSTAT_REG	R	32	0x0000 00B4	0x4902 40B4	0x4012 40B4	0x2 40B4
MCBSPLP_RBUFFSTAT_REG	R	32	0x0000 00B8	0x4902 40B8	0x4012 40B8	0x2 40B8

Table 23-366. MCBSP3 Register Summary

Register Name	Type	Register Width (Bits)	Address Offset	Physical Address L3 Interconnect	Physical Address Cortex-A9 Private Access	Physical Address DSP Private Access
MCBSPLP_DRR_REG	R	32	0x0000 0000	0x4902 6000	0x4012 6000	0x2 6000
MCBSPLP_DXR_REG	W	32	0x0000 0008	0x4902 6008	0x4012 6008	0x2 6008
MCBSPLP_SPCR2_REG	RW	32	0x0000 0010	0x4902 6010	0x4012 6010	0x2 6010
MCBSPLP_SPCR1_REG	RW	32	0x0000 0014	0x4902 6014	0x4012 6014	0x2 6014
MCBSPLP_RCR2_REG	RW	32	0x0000 0018	0x4902 6018	0x4012 6018	0x2 6018
MCBSPLP_RCR1_REG	RW	32	0x0000 001C	0x4902 601C	0x4012 601C	0x2 601C

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Table 23-366. MCBSP3 Register Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	Physical Address L3 Interconnect	Physical Address Cortex-A9 Private Access	Physical Address DSP Private Access
MCBSPLP_XCR2_REG	RW	32	0x0000 0020	0x4902 6020	0x4012 6020	0x2 6020
MCBSPLP_XCR1_REG	RW	32	0x0000 0024	0x4902 6024	0x4012 6024	0x2 6024
MCBSPLP_SRGR2_REG	RW	32	0x0000 0028	0x4902 6028	0x4012 6028	0x2 6028
MCBSPLP_SRGR1_REG	RW	32	0x0000 002C	0x4902 602C	0x4012 602C	0x2 602C
MCBSPLP_MCR2_REG	RW	32	0x0000 0030	0x4902 6030	0x4012 6030	0x2 6030
MCBSPLP_MCR1_REG	RW	32	0x0000 0034	0x4902 6034	0x4012 6034	0x2 6034
MCBSPLP_RCERA_REG	RW	32	0x0000 0038	0x4902 6038	0x4012 6038	0x2 6038
MCBSPLP_RCERB_REG	RW	32	0x0000 003C	0x4902 603C	0x4012 603C	0x2 603C
MCBSPLP_XCERA_REG	RW	32	0x0000 0040	0x4902 6040	0x4012 6040	0x2 6040
MCBSPLP_XCERB_REG	RW	32	0x0000 0044	0x4902 6044	0x4012 6044	0x2 6044
MCBSPLP_PCR_REG	RW	32	0x0000 0048	0x4902 6048	0x4012 6048	0x2 6048
MCBSPLP_RCERC_REG	RW	32	0x0000 004C	0x4902 604C	0x4012 604C	0x2 604C
MCBSPLP_RCERD_REG	RW	32	0x0000 0050	0x4902 6050	0x4012 6050	0x2 6050
MCBSPLP_XCERC_REG	RW	32	0x0000 0054	0x4902 6054	0x4012 6054	0x2 6054
MCBSPLP_XCERD_REG	RW	32	0x0000 0058	0x4902 6058	0x4012 6058	0x2 6058
MCBSPLP_RCERE_REG	RW	32	0x0000 005C	0x4902 605C	0x4012 605C	0x2 605C
MCBSPLP_RCERF_REG	RW	32	0x0000 0060	0x4902 6060	0x4012 6060	0x2 6060
MCBSPLP_XCERE_REG	RW	32	0x0000 0064	0x4902 6064	0x4012 6064	0x2 6064
MCBSPLP_XCERF_REG	RW	32	0x0000 0068	0x4902 6068	0x4012 6068	0x2 6068
MCBSPLP_RCERG_REG	RW	32	0x0000 006C	0x4902 606C	0x4012 606C	0x2 606C
MCBSPLP_RCERH_REG	RW	32	0x0000 0070	0x4902 6070	0x4012 6070	0x2 6070
MCBSPLP_XCERG_REG	RW	32	0x0000 0074	0x4902 6074	0x4012 6074	0x2 6074
MCBSPLP_XCERH_REG	RW	32	0x0000 0078	0x4902 6078	0x4012 6078	0x2 6078
MCBSPLP_REV_REG	R	32	0x0000 007C	0x4902 607C	0x4012 607C	0x2 607C
MCBSPLP_RINTCLR_REG	RW	32	0x0000 0080	0x4902 6080	0x4012 6080	0x2 6080
MCBSPLP_XINTCLR_REG	RW	32	0x0000 0084	0x4902 6084	0x4012 6084	0x2 6084
MCBSPLP_ROVFLCLR_REG	RW	32	0x0000 0088	0x4902 6088	0x4012 6088	0x2 6088
MCBSPLP_SYSCONFIG_REG	RW	32	0x0000 008C	0x4902 608C	0x4012 608C	0x2 608C
MCBSPLP_THRSH2_REG	RW	32	0x0000 0090	0x4902 6090	0x4012 6090	0x2 6090
MCBSPLP_THRSH1_REG	RW	32	0x0000 0094	0x4902 6094	0x4012 6094	0x2 6094
MCBSPLP_IRQSTATUS_REG	RW	32	0x0000 00A0	0x4902 60A0	0x4012 60A0	0x2 60A0
MCBSPLP_IRQENABLE_REG	RW	32	0x0000 00A4	0x4902 60A4	0x4012 60A4	0x2 60A4
MCBSPLP_WAKEUPEN_REG	RW	32	0x0000 00A8	0x4902 60A8	0x4012 60A8	0x2 60A8
MCBSPLP_XCCR_REG	RW	32	0x0000 00AC	0x4902 60AC	0x4012 60AC	0x2 60AC
MCBSPLP_RCCR_REG	RW	32	0x0000 00B0	0x4902 60B0	0x4012 60B0	0x2 60B0
MCBSPLP_XBUFFSTAT_REG	R	32	0x0000 00B4	0x4902 60B4	0x4012 60B4	0x2 60B4
MCBSPLP_RBUFFSTAT_REG	R	32	0x0000 00B8	0x4902 60B8	0x4012 60B8	0x2 60B8

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Table 23-367. MCBSP4 Register Summary

Register Name	Type	Register Width (Bits)	Address Offset	Physical Address L4-PER Interconnect
MCBSPLP_DRR_REG	R	32	0x0000 0000	0x4809 6000
MCBSPLP_DXR_REG	W	32	0x0000 0008	0x4809 6008
MCBSPLP_SPCR2_REG	RW	32	0x0000 0010	0x4809 6010
MCBSPLP_SPCR1_REG	RW	32	0x0000 0014	0x4809 6014
MCBSPLP_RCR2_REG	RW	32	0x0000 0018	0x4809 6018
MCBSPLP_RCR1_REG	RW	32	0x0000 001C	0x4809 601C
MCBSPLP_XCR2_REG	RW	32	0x0000 0020	0x4809 6020
MCBSPLP_XCR1_REG	RW	32	0x0000 0024	0x4809 6024
MCBSPLP_SRGR2_REG	RW	32	0x0000 0028	0x4809 6028
MCBSPLP_SRGR1_REG	RW	32	0x0000 002C	0x4809 602C
MCBSPLP_MCR2_REG	RW	32	0x0000 0030	0x4809 6030
MCBSPLP_MCR1_REG	RW	32	0x0000 0034	0x4809 6034
MCBSPLP_RCERA_REG	RW	32	0x0000 0038	0x4809 6038
MCBSPLP_RCERB_REG	RW	32	0x0000 003C	0x4809 603C
MCBSPLP_XCERA_REG	RW	32	0x0000 0040	0x4809 6040
MCBSPLP_XCERB_REG	RW	32	0x0000 0044	0x4809 6044
MCBSPLP_PCR_REG	RW	32	0x0000 0048	0x4809 6048
MCBSPLP_RCERC_REG	RW	32	0x0000 004C	0x4809 604C
MCBSPLP_RCERD_REG	RW	32	0x0000 0050	0x4809 6050
MCBSPLP_XCERC_REG	RW	32	0x0000 0054	0x4809 6054
MCBSPLP_XCERD_REG	RW	32	0x0000 0058	0x4809 6058
MCBSPLP_RCERE_REG	RW	32	0x0000 005C	0x4809 605C
MCBSPLP_RCERF_REG	RW	32	0x0000 0060	0x4809 6060
MCBSPLP_XCERE_REG	RW	32	0x0000 0064	0x4809 6064
MCBSPLP_XCERF_REG	RW	32	0x0000 0068	0x4809 6068
MCBSPLP_RCERG_REG	RW	32	0x0000 006C	0x4809 606C
MCBSPLP_RCERH_REG	RW	32	0x0000 0070	0x4809 6070
MCBSPLP_XCERG_REG	RW	32	0x0000 0074	0x4809 6074
MCBSPLP_XCERH_REG	RW	32	0x0000 0078	0x4809 6078
MCBSPLP_REV_REG	R	32	0x0000 007C	0x4809 607C
MCBSPLP_RINTCLR_REG	RW	32	0x0000 0080	0x4809 6080
MCBSPLP_XINTCLR_REG	RW	32	0x0000 0084	0x4809 6084
MCBSPLP_ROVFLCLR_REG	RW	32	0x0000 0088	0x4809 6088
MCBSPLP_SYSCONFIG_REG	RW	32	0x0000 008C	0x4809 608C
MCBSPLP_THRSH2_REG	RW	32	0x0000 0090	0x4809 6090
MCBSPLP_THRSH1_REG	RW	32	0x0000 0094	0x4809 6094
MCBSPLP_IRQSTATUS_REG	RW	32	0x0000 00A0	0x4809 60A0
MCBSPLP_IRQENABLE_REG	RW	32	0x0000 00A4	0x4809 60A4
MCBSPLP_WAKEUPEN_REG	RW	32	0x0000 00A8	0x4809 60A8
MCBSPLP_XCCR_REG	RW	32	0x0000 00AC	0x4809 60AC
MCBSPLP_RCCR_REG	RW	32	0x0000 00B0	0x4809 60B0
MCBSPLP_XBUFFSTAT_REG	R	32	0x0000 00B4	0x4809 60B4
MCBSPLP_RBUFFSTAT_REG	R	32	0x0000 00B8	0x4809 60B8

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23.5.6.2.2 MCBSP Register Description

Table 23-368 through Table 23-452 describe the individual MCBSP registers.

Table 23-368. MCBSPLP_DRR_REG

Address Offset	0x0000 0000		
Physical Address	0x4902 2000 0x4012 2000 0x2 2000 0x4902 4000 0x4012 4000 0x2 4000 0x4902 6000 0x4012 6000 0x2 6000	**Instance**	MCBSP1_L3 MCBSP1_CORTEX-A9 MCBSP1_DSP MCBSP2_L3 MCBSP2_CORTEX-A9 MCBSP2_DSP MCBSP3_L3 MCBSP3_CORTEX-A9 MCBSP3_DSP
Description	McBSPLP data receive register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DRR																															

Bits	Field Name	Description	Type	Reset
31:0	DRR	Data receive register	R	0x0000 0000

Table 23-369. Register Call Summary for Register MCBSPLP_DRR_REG

Multichannel Buffered Serial Port (McBSP)

- Data Transfer Process for 8-/12-/16-/20-/24-/32-Bit-Long Words: [0]
- Clocking and Framing Data: [1]
- McBSP Reception: [2] [3]
- Introduction: [4]
- Overrun in the Receiver: [5] [6]
- MCBSP Register Summary: [7] [8] [9] [10]

Table 23-370. MCBSPLP_DXR_REG

Address Offset	0x0000 0008		
Physical Address	0x4902 2008 0x4012 2008 0x2 2008 0x4902 4008 0x4012 4008 0x2 4008 0x4902 6008 0x4012 6008 0x2 6008	**Instance**	MCBSP1_L3 MCBSP1_CORTEX-A9 MCBSP1_DSP MCBSP2_L3 MCBSP2_CORTEX-A9 MCBSP2_DSP MCBSP3_L3 MCBSP3_CORTEX-A9 MCBSP3_DSP
Description	McBSPLP data transmit register		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DXR																															

Bits	Field Name	Description	Type	Reset
31:0	DXR	Data transmit register	W	0x0000 0000

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Table 23-371. Register Call Summary for Register MCBSPLP_DXR_REG

Multichannel Buffered Serial Port (McBSP)

- Data Transfer Process for 8-/12-/16-/20-/24-/32-Bit-Long Words: [0]
- McBSP Transmission: [1] [2]
- Introduction: [3]
- Underflow in the Transmitter: [4] [5] [6] [7]
- Transmit Multichannel Selection Modes: [8]
- McBSP Initialization Procedure: [9]
- MCBSP Register Summary: [10] [11] [12] [13]

Table 23-372. MCBSPLP_SPCR2_REG

Address Offset	0x0000 0010		
Physical Address	0x4902 2010	**Instance**	MCBSP1_L3
	0x4012 2010		MCBSP1_CORTEX-A9
	0x2 2010		MCBSP1_DSP
	0x4902 4010		MCBSP2_L3
	0x4012 4010		MCBSP2_CORTEX-A9
	0x2 4010		MCBSP2_DSP
	0x4902 6010		MCBSP3_L3
	0x4012 6010		MCBSP3_CORTEX-A9
	0x2 6010		MCBSP3_DSP
Description	McBSPLP serial port control register 2		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						FREE	SOFT	FRST	GRST	XINTM		XSYNCERR	XEMPTY	XRDY	XRST

Bits	Field Name	Description	Type	Reset
31:10	RESERVED	Reserved	R	0x000000
9	FREE	Free Running Mode (When this bit is set, the module ignores the Msuspend input) 0x0: Free running mode is disabled 0x1: Free running mode is enabled	RW	0
8	SOFT	Soft Bit 0x0: SOFT mode is disabled: the module stops its activity immediately following MSuspend assertion 0x1: SOFT mode is enabled: the module freezes its state after completion of the current operation when MSuspend is asserted	RW	0
7	FRST	Frame-Sync Generator Reset 0x0: Frame-sync logic is reset. Frame-sync signal FSG is not generated by the sample-rate generator 0x1: Frame-sync signal FSG is generated after (FPER+1) number of CLKG clocks; that is, all frame counters are loaded with their programmed values	RW	0
6	GRST	Sample-Rate Generator Reset 0x0: SRG is reset 0x1: SRG is pulled out of reset. CLKG is driven as per programmed value in SRG registers (SRGR[1,2])	RW	0

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Bits	Field Name	Description	Type	Reset
5:4	XINTM	Transmit Interrupt Mode (legacy) 0x0: XINT is driven by XRDY 0x1: XINT generated by end-of-frame 0x2: XINT generated by a new frame synchronization 0x3: XINT generated by XSYNCERR	RW	0x0
3	XSYNCERR	Transmit Synchronization Error (writing 0 to this bit clear the legacy transmit interrupt if asserted due to XSYNCERR condition) 0x0: No synchronization error 0x1: Synchronization error detected by McBSP	RW	0
2	XEMPTY	Transmit Shift Register XSR Empty Read 0x0: XSR is empty Read 0x1: XSR is not empty	R	0
1	XRDY	Transmitter ready Read 0x0: Transmitter is not ready. Read 0x1: Transmitter is ready for new data in DXR	R	0
0	XRST	Transmitter reset. This resets and enables the transmitter. 0x0: The serial port transmitter is disabled and in reset state. 0x1: The serial port transmitter is enabled.	RW	0

Table 23-373. Register Call Summary for Register MCBSPLP_SPCR2_REG

Multichannel Buffered Serial Port (McBSP)

- McBSP Software Reset: [0] [1] [2]
- Data Transfer Process for 8-/12-/16-/20-/24-/32-Bit-Long Words: [3]
- McBSP Transmission: [4] [5]
- Clock Generation in the SRG: [6]
- Frame-Sync Generation in the SRG: [7] [8]
- Introduction: [9] [10] [11]
- Underflow in the Transmitter: [12] [13] [14] [15] [16]
- Unexpected Transmit Frame-Sync Pulse: [17] [18] [19]
- McBSP DMA Configuration: [20] [21]
- Transmit Multichannel Selection Modes: [22] [23] [24]
- McBSP Initialization Procedure: [25] [26] [27] [28] [29] [30]
- Reset and Initialization Procedure for the SRG: [31]
- Place the Transmitter in Reset (Step 1): [32]
- Take the Receiver Out of Reset (Step 3): [33]
- GPIO on the McBSP Pins (Legacy Only): [34] [35]
- MCBSP Register Summary: [36] [37] [38] [39]

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Table 23-374. MCBSPLP_SPCR1_REG

Address Offset	0x0000 0014		
Physical Address	0x4902 2014 0x4012 2014 0x2 2014 0x4902 4014 0x4012 4014 0x2 4014 0x4902 6014 0x4012 6014 0x2 6014	**Instance**	MCBSP1_L3 MCBSP1_CORTEX-A9 MCBSP1_DSP MCBSP2_L3 MCBSP2_CORTEX-A9 MCBSP2_DSP MCBSP3_L3 MCBSP3_CORTEX-A9 MCBSP3_DSP
Description	McBSPLP serial port control register 1		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																ALB	RJUST	RESERVED						DXENA	RESERVED	RINTM		RSYNCERR	RFULL	RRDY	RRST
R-0																RW-0	RW-0	R-0						RW-0	R-0	RW-0		RW-0	R-0	R-0	R-0

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x0000
15	ALB	Analog Loopback Mode 0x0: Analog loopback mode disabled 0x1: Analog loopback mode enabled	RW	0
14:13	RJUST	Receive Sign-Extension and Justification Mode 0x0: Right-justify and zero-fill MSBs in DRR 0x1: Right-justify and sign-extend MSBs in DRR 0x2: Left-justify and zero-fill LSBs in DRR 0x3: Reserved	RW	0x0
12:8	RESERVED	Reserved	R	0x00
7	DXENA	DX Enabler 0x0: DX enabler is off 0x1: DX enabler is on	RW	0
6	RESERVED	Reserved	R	0
5:4	RINTM	Receive Interrupt Mode (legacy) 0x0: RINT driven by RRDY (that is, end of word) and end of frame in A-bis mode 0x1: RINT generated by end-of-block or end-of-frame in multichannel operation 0x2: RINT generated by a new frame synchronization 0x3: RINT generated by RSYNCERR	RW	0x0
3	RSYNCERR	Receive Synchronization Error (writing 0 to this bit clear the legacy receive interrupt if asserted due to RSYNCERR condition) 0x0: No synchronization error 0x1: Synchronization error detected by McBSP	RW	0
2	RFULL	Receive Shift Register (RSR]) Full Read 0x0: DRR is not read, RB is full and RSR is also full with new word Read 0x1: RB is not in overrun condition	R	0

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Bits	Field Name	Description	Type	Reset
1	RRDY	Receiver Ready Read 0x0: Receiver is not ready Read 0x1: Receiver is ready with data to be read from DRR	R	0
0	RRST	Receiver reset. This resets and enables the receiver. 0x0: The serial port receiver is disabled and in reset state. 0x1: The serial port receiver is enabled.	RW	0

Table 23-375. Register Call Summary for Register MCBSPLP_SPCR1_REG

Multichannel Buffered Serial Port (McBSP)

- McBSP Software Reset: [0]
- McBSP Reception: [1] [2] [3]
- Clock Generation in the SRG: [4]
- Introduction: [5] [6] [7] [8]
- Overrun in the Receiver: [9] [10] [11]
- Unexpected Receive Frame-Sync Pulse: [12] [13] [14]
- McBSP DMA Configuration: [15] [16]
- Receive Multichannel Selection Mode: [17]
- McBSP Initialization Procedure: [18] [19] [20] [21]
- Place the Receiver in Reset (Step 1): [22]
- Programming the McBSP Registers for the Desired Receiver Configuration (Step 2): [23] [24] [25]
- Take the Receiver Out of Reset (Step 3): [26]
- Programming the McBSP Registers for the Desired Transmitter Operation (Step 2): [27] [28]
- GPIO on the McBSP Pins (Legacy Only): [29] [30]
- MCBSP Register Summary: [31] [32] [33] [34]

Table 23-376. MCBSPLP_RCR2_REG

Address Offset	0x0000 0018		
Physical Address	0x4902 2018 0x4012 2018 0x2 2018 0x4902 4018 0x4012 4018 0x2 4018 0x4902 6018 0x4012 6018 0x2 6018	**Instance**	MCBSP1_L3 MCBSP1_CORTEX-A9 MCBSP1_DSP MCBSP2_L3 MCBSP2_CORTEX-A9 MCBSP2_DSP MCBSP3_L3 MCBSP3_CORTEX-A9 MCBSP3_DSP
Description	McBSPLP receive control register 2		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RPHASE	RFRLEN2							RWDLEN2			RREVERSE		RESERVED		RDATDLY

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x0000
15	RPHASE	Receive Phases 0x0: Single-phase frame 0x1: Dual-phase frame	RW	0

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Bits	Field Name	Description	Type	Reset
14:8	RFRLEN2	Receive Frame Length 2 Single-phase frame selected: RFRLEN2=don't care Dual-phase frame selected: RFRLEN2=000 0000 - 1 word per second phase (other values are reserved)	RW	0x00
7:5	RWDLEN2	Receive Word Length 2 0x0: 8 bits 0x1: 12 bits 0x2: 16 bits 0x3: 20 bits 0x4: 24 bits 0x5: 32 bits 0x6: Reserved (do not use) 0x7: Reserved (do not use)	RW	0x0
4:3	RREVERSE	Receive reverse mode. 0x0: Data transfer starts with MSB first. 0x1: Data transfer starts with LSB first. 0x2: Reserved (do not use) 0x3: Reserved (do not use)	RW	0x0
2	RESERVED	Reserved	R	0
1:0	RDATDLY	Receive Data Delay 0x0: 0-bit data delay 0x1: 1-bit data delay 0x2: 2-bit data delay 0x3: Reserved	RW	0x0

Table 23-377. Register Call Summary for Register MCBSPLP_RCR2_REG

Multichannel Buffered Serial Port (McBSP)

- Words, Frames, and Phases Definitions: [0] [1] [2]
- Bit Reordering (Option to Transfer LSB First): [3]
- Clocking and Framing Data: [4] [5]
- Frame Phases (Dual-Phase Frame I2S Support): [6] [7] [8] [9] [10] [11] [12] [13] [14] [15]
- McBSP Reception: [16]
- MCBSP Data Transfer Mode: [17]
- Unexpected Receive Frame-Sync Pulse: [18]
- Configuring a Frame for Multichannel Selection: [19]
- McBSP Initialization Procedure: [20] [21]
- Programming the McBSP Registers for the Desired Receiver Configuration (Step 2): [22] [23] [24] [25] [26]
- Programming the McBSP Registers for the Desired Transmitter Operation (Step 2): [27]
- MCBSP Register Summary: [28] [29] [30] [31]

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Table 23-378. MCBSPLP_RCR1_REG

Address Offset	0x0000 001C		
Physical Address	0x4902 201C 0x4012 201C 0x2 201C 0x4902 401C 0x4012 401C 0x2 401C 0x4902 601C 0x4012 601C 0x2 601C	**Instance**	MCBSP1_L3 MCBSP1_CORTEX-A9 MCBSP1_DSP MCBSP2_L3 MCBSP2_CORTEX-A9 MCBSP2_DSP MCBSP3_L3 MCBSP3_CORTEX-A9 MCBSP3_DSP
Description	McBSPLP receive control register 1		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RFRLEN1								RWDLEN1			RESERVED				

Bits	Field Name	Description	Type	Reset
31:15	RESERVED	Reserved	R	0x00000
14:8	RFRLEN1	Receive Frame Length 1 Single-phase frame selected: RFRLEN1=000 0000 - 1 word per frame RFRLEN1=000 0001 - 2 words per frame RFRLEN1=111 1111 - 128 words per frame Dual-phase frame selected: RFRLEN1=000 0000 - 1 word per phase (other values are reserved)	RW	0x00
7:5	RWDLEN1	Receive Word Length 1 0x0: 8 bits 0x1: 12 bits 0x2: 16 bits 0x3: 20 bits 0x4: 24 bits 0x5: 32 bits 0x6: Reserved (do not use) 0x7: Reserved (do not use)	RW	0x0
4:0	RESERVED	Reserved	R	0x00

Table 23-379. Register Call Summary for Register MCBSPLP_RCR1_REG

Multichannel Buffered Serial Port (McBSP)

- Words, Frames, and Phases Definitions: [0] [1]
- Clocking and Framing Data: [2] [3]
- Frame Phases (Dual-Phase Frame I2S Support): [4] [5] [6] [7] [8] [9] [10]
- Configuring a Frame for Multichannel Selection: [11]
- McBSP Initialization Procedure: [12] [13]
- Programming the McBSP Registers for the Desired Receiver Configuration (Step 2): [14] [15]
- MCBSP Register Summary: [16] [17] [18] [19]

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Table 23-380. MCBSPLP_XCR2_REG

Address Offset	0x0000 0020		
Physical Address	0x4902 2020 0x4012 2020 0x2 2020 0x4902 4020 0x4012 4020 0x2 4020 0x4902 6020 0x4012 6020 0x2 6020	**Instance**	MCBSP1_L3 MCBSP1_CORTEX-A9 MCBSP1_DSP MCBSP2_L3 MCBSP2_CORTEX-A9 MCBSP2_DSP MCBSP3_L3 MCBSP3_CORTEX-A9 MCBSP3_DSP
Description	McBSPLP transmit control register 2		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																XPHASE	XFRLEN2							XWDLEN2			XREVERSE		RESERVED		XDATDLY

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x0000
15	XPHASE	Transmit Phases 0x0: Single-phase frame 0x1: Dual-phase frame	RW	0
14:8	XFRLEN2	Transmit Frame Length 2 Single-phase frame selected: XFRLEN2=don't care Dual-phase frame selected: XFRLEN2=000 0000 - 1 word per second phase (other values are reserved)	RW	0x00
7:5	XWDLEN2	Transmit Word Length 2 0x0: 8 bits 0x1: 12 bits 0x2: 16 bits 0x3: 20 bits 0x4: 24 bits 0x5: 32 bits 0x6: Reserved (do not use) 0x7: Reserved (do not use)	RW	0x0
4:3	XREVERSE	Transmit reverse mode. 0x0: Data transfer starts with MSB first. 0x1: Data transfer starts with LSB first. 0x2: Reserved (do not use) 0x3: Reserved (do not use)	RW	0x0
2	RESERVED	Reserved	R	0
1:0	XDATDLY	Transmit Data Delay 0x0: 0-bit data delay 0x1: 1-bit data delay 0x2: 2-bit data delay 0x3: Reserved	RW	0x0

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Table 23-381. Register Call Summary for Register MCBSPLP_XCR2_REG

Multichannel Buffered Serial Port (McBSP)

- Words, Frames, and Phases Definitions: [0] [1] [2]
- Bit Reordering (Option to Transfer LSB First): [3]
- Clocking and Framing Data: [4] [5] [6]
- Frame Phases (Dual-Phase Frame I2S Support): [7] [8] [9] [10] [11] [12] [13] [14] [15] [16]
- McBSP Transmission: [17]
- MCBSP Data Transfer Mode: [18]
- Unexpected Transmit Frame-Sync Pulse: [19]
- Configuring a Frame for Multichannel Selection: [20]
- McBSP Initialization Procedure: [21] [22]
- Programming the McBSP Registers for the Desired Transmitter Operation (Step 2): [23] [24] [25] [26]
- MCBSP Register Summary: [27] [28] [29] [30]

Table 23-382. MCBSPLP_XCR1_REG

Address Offset	0x0000 0024		
Physical Address	0x4902 2024 0x4012 2024 0x2 2024 0x4902 4024 0x4012 4024 0x2 4024 0x4902 6024 0x4012 6024 0x2 6024	**Instance**	MCBSP1_L3 MCBSP1_CORTEX-A9 MCBSP1_DSP MCBSP2_L3 MCBSP2_CORTEX-A9 MCBSP2_DSP MCBSP3_L3 MCBSP3_CORTEX-A9 MCBSP3_DSP
Description	McBSPLP transmit control register 1		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																XFRLEN1								XWDLEN1			RESERVED				

Bits	Field Name	Description	Type	Reset
31:15	RESERVED	Reserved	R	0x00000
14:8	XFRLEN1	Transmit Frame Length 1 Single-phase frame selected: XFRLEN1=000 0000 - 1 word per frame XFRLEN1=000 0001 - 2 words per frame XFRLEN1=111 1111 - 128 words per frame Dual-phase frame selected: XFRLEN1=000 0000 - 1 word per phase (other values are reserved)	RW	0x00
7:5	XWDLEN1	Transmit Word Length 1 0x0: 8 bits 0x1: 12 bits 0x2: 16 bits 0x3: 20 bits 0x4: 24 bits 0x5: 32 bits 0x6: Reserved (do not use) 0x7: Reserved (do not use)	RW	0x0
4:0	RESERVED	Reserved	R	0x00

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Table 23-383. Register Call Summary for Register MCBSPLP_XCR1_REG

Multichannel Buffered Serial Port (McBSP)

- Words, Frames, and Phases Definitions: [0] [1]
- Clocking and Framing Data: [2] [3]
- Frame Phases (Dual-Phase Frame I2S Support): [4] [5] [6] [7] [8] [9] [10]
- Configuring a Frame for Multichannel Selection: [11]
- McBSP Initialization Procedure: [12] [13]
- Programming the McBSP Registers for the Desired Transmitter Operation (Step 2): [14] [15]
- MCBSP Register Summary: [16] [17] [18] [19]

Table 23-384. MCBSPLP_SRGR2_REG

Address Offset	0x0000 0028		
Physical Address	0x4902 2028 0x4012 2028 0x2 2028 0x4902 4028 0x4012 4028 0x2 4028 0x4902 6028 0x4012 6028 0x2 6028	**Instance**	MCBSP1_L3 MCBSP1_CORTEX-A9 MCBSP1_DSP MCBSP2_L3 MCBSP2_CORTEX-A9 MCBSP2_DSP MCBSP3_L3 MCBSP3_CORTEX-A9 MCBSP3_DSP
Description	McBSPLP sample rate generator register 2		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																GSYNC	CLKSP	CLKSM	FSGM	FPER											

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x0000
15	GSYNC	0x0: The SRG clock (CLKG) is free running. 0x1: The SRG clock (CLKG) is running. But CLKG is resynchronized and frame-sync signal (FSG) is generated only after detecting the receive frame-sync signal (FSR). Also, frame period, FPER, is a don't care because the period is dictated by the external frame-sync pulse.	RW	0
14	CLKSP	CLKS Polarity Clock Edge Select Only used when the external clock CLKS drives the SRG clock (CLKSM=0). 0x0: Rising edge of CLKG and FSG. 0x1: Falling edge of CLKG and FSG.	RW	0
13	CLKSM	McBSPLP Sample Rate Generator Clock Mode 0x0: SCLKME=0: SRG clock derived from the CLKS pin. SCLKME=1: SRG clock derived from the CLKRI pin. 0x1: SCLKME=0: SRG clock derived from the CPU clock. SCLKME=1: SRG clock derived from the CLKXI clock.	RW	1
12	FSGM	Sample Rate Generator Transmit Frame-Synchronization Mode Used when FSXM=1 in the PCR. 0x0: Transmit frame-sync signal (FSX) is generated when transmit buffer is not empty When FSGM=0, FPER and FWID are used to determine the frame-sync period and width (external FSX is gated by the buffer empty condition). 0x1: Transmit frame-sync signal driven by the SRG frame-sync signal, FSG.	RW	0

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Bits	Field Name	Description	Type	Reset
11:0	FPER	Frame Period. This field plus 1 determines when the next frame-sync signal becomes active. Range: 1 to 4096 CLKG periods	RW	0x000

Table 23-385. Register Call Summary for Register MCBSPLP_SRGR2_REG

Multichannel Buffered Serial Port (McBSP)

- McBSP1 Clocks: [0]
- McBSP2 Clocks: [1]
- McBSP3 Clocks: [2]
- McBSP4 Clocks: [3]
- Clocking and Framing Data: [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17]
- McBSP SRG: [18] [19] [20] [21]
- Frame-Sync Generation in the SRG: [22] [23] [24] [25] [26] [27] [28]
- Synchronizing SRG Outputs to an External Clock: [29] [30] [31] [32] [33] [34] [35] [36] [37]
- Underflow in the Transmitter: [38] [39] [40]
- McBSP Initialization Procedure: [41] [42]
- Reset and Initialization Procedure for the SRG: [43]
- Programming the McBSP Registers for the Desired Receiver Configuration (Step 2): [44] [45] [46] [47] [48]
- Programming the McBSP Registers for the Desired Transmitter Operation (Step 2): [49] [50] [51] [52] [53]
- MCBSP Register Summary: [54] [55] [56] [57]

Table 23-386. MCBSPLP_SRGR1_REG

Address Offset	0x0000 002C		
Physical Address	0x4902 202C	**Instance**	MCBSP1_L3
	0x4012 202C		MCBSP1_CORTEX-A9
	0x2 202C		MCBSP1_DSP
	0x4902 402C		MCBSP2_L3
	0x4012 402C		MCBSP2_CORTEX-A9
	0x2 402C		MCBSP2_DSP
	0x4902 602C		MCBSP3_L3
	0x4012 602C		MCBSP3_CORTEX-A9
	0x2 602C		MCBSP3_DSP
Description	McBSPLP sample rate generator register 1		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																FWID								CLKGDV							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x0000
15:8	FWID	Frame Width. This field plus 1 determines the width of the frame-sync pulse, FSG, during its active period. Range: 1 to 256 CLKG periods.	RW	0x00
7:0	CLKGDV	Sample Rate Generator Clock Divider This value is used as the divide-down number to generate the required SRG clock frequency. Default value is 1.	RW	0x01

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Table 23-387. Register Call Summary for Register MCBSPLP_SRGR1_REG

Multichannel Buffered Serial Port (McBSP)

- Clocking and Framing Data: [0]
- McBSP SRG: [1] [2] [3]
- Frame-Sync Generation in the SRG: [4] [5]
- Synchronizing SRG Outputs to an External Clock: [6] [7]
- Underflow in the Transmitter: [8]
- McBSP Initialization Procedure: [9] [10]
- Reset and Initialization Procedure for the SRG: [11]
- Programming the McBSP Registers for the Desired Receiver Configuration (Step 2): [12] [13]
- Programming the McBSP Registers for the Desired Transmitter Operation (Step 2): [14] [15]
- MCBSP Register Summary: [16] [17] [18] [19]

Table 23-388. MCBSPLP_MCR2_REG

Address Offset	0x0000 0030		
Physical Address	0x4902 2030 0x4012 2030 0x2 2030 0x4902 4030 0x4012 4030 0x2 4030 0x4902 6030 0x4012 6030 0x2 6030	**Instance**	MCBSP1_L3 MCBSP1_CORTEX-A9 MCBSP1_DSP MCBSP2_L3 MCBSP2_CORTEX-A9 MCBSP2_DSP MCBSP3_L3 MCBSP3_CORTEX-A9 MCBSP3_DSP
Description	McBSPLP multi channel register 2		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						XMCME	XPBBLK	XPABLK	RESERVED					XMCM	

Bits	Field Name	Description	Type	Reset
31:10	RESERVED	Reserved	R	0x000000
9	XMCME	0x0: 2-partition mode: Only partitions A and B are used. You can control up to 32 channels in the transmit multichannel selection mode selected with the XMCM bits. If XMCM = 01b or 10b, assign 16 channels to partition A with the XPABLK bits. Assign 16 channels to partition B with the XPBBLK bits. If XMCM = 11b (for symmetric transmission and reception), assign 16 channels to receive partition A with the RPABLK bits. Assign 16 channels to receive partition B with the RPBBLK bits. You control the channels with the appropriate transmit channel enable registers: XCERA: Channels in partition A XCERB: Channels in partition B 0x1: 8-partition mode: All partitions (A through H) are used. You can control up to 128 channels in the transmit multichannel selection mode selected with the XMCM bits. You control the channels with the appropriate transmit channel enable registers: XCERA: Channels 0 through 15 XCERB: Channels 16 through 31 XCERC: Channels 32 through 47 XCERD: Channels 48 through 63 XCERE: Channels 64 through 79 XCERF: Channels 80 through 95 XCERG: Channels 96 through 111 XCERH: Channels 112 through 127	RW	0

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Bits	Field Name	Description	Type	Reset
8:7	XPBBLK	Transmit Partition B Block (legacy) 0x0: Block 1. Channel 16 to channel 31 0x1: Block 3. Channel 48 to channel 63 0x2: Block 5. Channel 80 to channel 95 0x3: Block 7. Channel 112 to channel 127	RW	0x0
6:5	XPABLK	Transmit Partition A Block (legacy) 0x0: Block 0. Channel 0 to channel 15 0x1: Block 2. Channel 32 to channel 47 0x2: Block 4. Channel 64 to channel 79 0x3: Block 6. Channel 96 to channel 111	RW	0x0
4:2	RESERVED	Reserved	R	0x0
1:0	XMCM	Transmit Multichannel Selection Enable 0x0: All channels enabled without masking (DX is always driven during transmission of data). 0x1: All channels disabled and therefore masked by default. Required channels are selected by enabling XP(A/B)BLK and XCER(A/B) appropriately. Also, these selected channels are not masked and therefore DX is always driven. 0x2: All channels enabled, but masked. Selected channels enabled via XP(A/B)BLK and XCER(A/B) are unmasked. 0x3: All channels disabled and therefore masked by default. Required channels are selected by enabling RP(A/B)BLK and RCER(A/B) appropriately. Selected channels can be unmasked by RP(A/B)BLK and XCER(A/B). This mode is used for symetric transmit and receive operation.	RW	0x0

Table 23-389. Register Call Summary for Register MCBSPLP_MCR2_REG

Multichannel Buffered Serial Port (McBSP)

- Using Eight Partitions: [0] [1] [2]
- Using Two Partitions (Legacy Only): [3] [4]
- Transmit Multichannel Selection Modes: [5] [6] [7] [8] [9] [10]
- McBSP Initialization Procedure: [11]
- MCBSP Register Summary: [12] [13] [14] [15]

Table 23-390. MCBSPLP_MCR1_REG

Address Offset	0x0000 0034		
Physical Address	0x4902 2034 0x4012 2034 0x2 2034 0x4902 4034 0x4012 4034 0x2 4034 0x4902 6034 0x4012 6034 0x2 6034	**Instance**	MCBSP1_L3 MCBSP1_CORTEX-A9 MCBSP1_DSP MCBSP2_L3 MCBSP2_CORTEX-A9 MCBSP2_DSP MCBSP3_L3 MCBSP3_CORTEX-A9 MCBSP3_DSP
Description	McBSPLP multi channel register 1		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						RMCME	RPBBLK	RPABLK			RESERVED				RMCM

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Bits	Field Name	Description	Type	Reset
31:10	RESERVED	Reserved	R	0x000000
9	RMCME	(legacy) 0x0: 2-partition mode. Only partitions A and B are used. You can control up to 32 channels in the receive multichannel selection mode (RMCM = 1). Assign 16 channels to partition A with the RPABLK bits. Assign 16 channels to partition B with the RPBBLK bits. You control the channels with the apropriate receive channel enable registers: RCERA: Channels in partition A RCERB: Channels in partition B 0x1: 8-partition mode: All partitions (A through H) are used. You can control up to 128 channels in the receive multichannel selection mode. You control the channels with the appropriate receive channel enable registers: RCERA: Channels 0 through 15 RCERB: Channels 16 through 31 RCERC: Channels 32 through 47 RCERD: Channels 48 through 63 RCERE: Channels 64 through 79 RCERF: Channels 80 through 95 RCERG: Channels 96 through 111 RCERH: Channels 112 through 127	RW	0
8:7	RPBBLK	Receive Partition B Block (legacy) 0x0: Block 1. Channel 16 to channel 31 0x1: Block 3. Channel 48 to channel 63 0x2: Block 5. Channel 80 to channel 95 0x3: Block 7. Channel 112 to channel 127	RW	0x0
6:5	RPABLK	Receive Partition A Block (legacy) 0x0: Block 0. Channel 0 to channel 15 0x1: Block 2. Channel 32 to channel 47 0x2: Block 4. Channel 64 to channel 79 0x3: Block 6. Channel 96 to channel 111	RW	0x0
4:1	RESERVED	Reserved	R	0x0
0	RMCM	Receive Multichannel Selection Enable 0x0: All 128 channels 0x1: All channels disabled by default. Required channels are selected by enabling RP(A/B)BLK and RCER(A/B) appropriately	RW	0

Table 23-391. Register Call Summary for Register MCBSPLP_MCR1_REG

Multichannel Buffered Serial Port (McBSP)

- Using Eight Partitions: [0] [1] [2]
- Receive Multichannel Selection Mode: [3] [4]
- Using Two Partitions (Legacy Only): [5] [6] [7] [8]
- McBSP Initialization Procedure: [9]
- Programming the McBSP Registers for the Desired Receiver Configuration (Step 2): [10]
- Programming the McBSP Registers for the Desired Transmitter Operation (Step 2): [11]
- MCBSP Register Summary: [12] [13] [14] [15]

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Table 23-392. MCBSPLP_RCERA_REG

Address Offset	0x0000 0038		
Physical Address	0x4902 2038 0x4012 2038 0x2 2038 0x4902 4038 0x4012 4038 0x2 4038 0x4902 6038 0x4012 6038 0x2 6038	**Instance**	MCBSP1_L3 MCBSP1_CORTEX-A9 MCBSP1_DSP MCBSP2_L3 MCBSP2_CORTEX-A9 MCBSP2_DSP MCBSP3_L3 MCBSP3_CORTEX-A9 MCBSP3_DSP
Description	McBSPLP receive channel enable register partition A		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RCERA															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x0000
15:0	RCERA	Receive Channel Enable RCERA n=0 Disables reception of n-th channel in an even-numbered block in partition A RCERA n=1 Enables reception of n-th channel in an even-numbered block in partition A	RW	0x0000

Table 23-393. Register Call Summary for Register MCBSPLP_RCERA_REG

Multichannel Buffered Serial Port (McBSP)

- Using Eight Partitions: [0]
- Receive Multichannel Selection Mode: [1] [2]
- Using Two Partitions (Legacy Only): [3]
- Transmit Multichannel Selection Modes: [4] [5]
- MCBSP Register Summary: [6] [7] [8] [9]

Table 23-394. MCBSPLP_RCERB_REG

Address Offset	0x0000 003C		
Physical Address	0x4902 203C 0x4012 203C 0x2 203C 0x4902 403C 0x4012 403C 0x2 403C 0x4902 603C 0x4012 603C 0x2 603C	**Instance**	MCBSP1_L3 MCBSP1_CORTEX-A9 MCBSP1_DSP MCBSP2_L3 MCBSP2_CORTEX-A9 MCBSP2_DSP MCBSP3_L3 MCBSP3_CORTEX-A9 MCBSP3_DSP
Description	McBSPLP receive channel enable register partition B		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RCERB															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x0000
15:0	RCERB	Receive Channel Enable RCERB n=0 Disables reception of n-th channel in a even-numbered block in partition B RCERB n=1 Enables reception of n-th channel in a even-numbered block in partition B	RW	0x0000

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Table 23-395. Register Call Summary for Register MCBSPLP_RCERB_REG

Multichannel Buffered Serial Port (McBSP)

- Using Eight Partitions: [0]
- Using Two Partitions (Legacy Only): [1]
- MCBSP Register Summary: [2] [3] [4] [5]

Table 23-396. MCBSPLP_XCERA_REG

Address Offset	0x0000 0040		
Physical Address	0x4902 2040 0x4012 2040 0x2 2040 0x4902 4040 0x4012 4040 0x2 4040 0x4902 6040 0x4012 6040 0x2 6040	**Instance**	MCBSP1_L3 MCBSP1_CORTEX-A9 MCBSP1_DSP MCBSP2_L3 MCBSP2_CORTEX-A9 MCBSP2_DSP MCBSP3_L3 MCBSP3_CORTEX-A9 MCBSP3_DSP
Description	McBSPLP transmit channel enable register partition A		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																XCERA															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x0000
15:0	XCERA	Transmit Channel Enable XCERA n=0 Disables transmission of n-th channel in an event-numbered block in partition A XCERA n=1 Enables transmission of n-th channel in an event-numbered block in partition A	RW	0x0000

Table 23-397. Register Call Summary for Register MCBSPLP_XCERA_REG

Multichannel Buffered Serial Port (McBSP)

- Using Eight Partitions: [0]
- Using Two Partitions (Legacy Only): [1]
- Transmit Multichannel Selection Modes: [2] [3] [4] [5] [6] [7]
- MCBSP Register Summary: [8] [9] [10] [11]

Table 23-398. MCBSPLP_XCERB_REG

Address Offset	0x0000 0044		
Physical Address	0x4902 2044 0x4012 2044 0x2 2044 0x4902 4044 0x4012 4044 0x2 4044 0x4902 6044 0x4012 6044 0x2 6044	**Instance**	MCBSP1_L3 MCBSP1_CORTEX-A9 MCBSP1_DSP MCBSP2_L3 MCBSP2_CORTEX-A9 MCBSP2_DSP MCBSP3_L3 MCBSP3_CORTEX-A9 MCBSP3_DSP
Description	McBSPLP transmit channel enable register partition B		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																XCERB															

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Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x0000
15:0	XCERB	Transmit Channel Enable XCERB n=0 Disables transmission of n-th channel in an even-numbered block in partition B XCERB n=1 Enables transmission of n-th channel in an even-numbered block in partition B	RW	0x0000

Table 23-399. Register Call Summary for Register MCBSPLP_XCERB_REG

Multichannel Buffered Serial Port (McBSP)

- Using Eight Partitions: [0]
- Using Two Partitions (Legacy Only): [1]
- MCBSP Register Summary: [2] [3] [4] [5]

Table 23-400. MCBSPLP_PCR_REG

Address Offset	0x0000 0048		
Physical Address	0x4902 2048 0x4012 2048 0x2 2048 0x4902 4048 0x4012 4048 0x2 4048 0x4902 6048 0x4012 6048 0x2 6048	**Instance**	MCBSP1_L3 MCBSP1_CORTEX-A9 MCBSP1_DSP MCBSP2_L3 MCBSP2_CORTEX-A9 MCBSP2_DSP MCBSP3_L3 MCBSP3_CORTEX-A9 MCBSP3_DSP
Description	McBSPLP pin control register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																IDLE_EN	XIOEN	RIOEN	FSXM	FSRM	CLKXM	CLKRM	SCLKME	CLKS_STAT	DX_STAT	DR_STAT	FSXP	FSRP	CLKXP	CLKRP	

Bits	Field Name	Description	Type	Reset
31:15	RESERVED	Reserved	R	0x00000
14	IDLE_EN	Idle enable. This bit allows stopping all the clocks in the MCBSPLP. (legacy) 0x0: The McBSP is running 0x1: The clocks in the McBSP are shut off when both IDLE_EN=1 and peripheral domain is in idle mode	RW	0
13	XIOEN	Transmit General Purpose I/O Mode only when XRST=0 in SPCR[1,2] (legacy) 0x0: DX, FSX and CLKX are configured as serial port pins and do not function as general-purpose I/Os. 0x1: DX pin is a general purpose output. FSX and CLKX are general purpose I/Os. These serial port pins do not perform serial port operation.	RW	0
12	RIOEN	Receive General Purpose I/O Mode when RRST=0 in SPCR[1,2] (legacy) 0x0: DR, FSR, CLKR and CLKS are configured as serial port pins and do not function as general-purpose I/Os. 0x1: DR and CLKS pins are general purpose inputs; FSR and CLKR are general purpose I/Os. These serial port pins do not perform serial port operation. The CLKS pin is affected by a combination of RRST and RIOEN signals of the receiver.	RW	0

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Bits	Field Name	Description	Type	Reset
11	FSXM	Transmit Frame-Synchronization Mode 0x0: Frame-sync signal derived from an external source 0x1: Frame synchronization is determined by the SRG frame-sync mode bit FSGM in SRGR2.	RW	0
10	FSRM	Receive Frame-Synchronization Mode 0x0: Frame-sync pulses generated by an external device. FSR is an input pin. 0x1: Frame synchronization generated internally by SRG. FSR is an output pin except when GSYNC=1 in SRGR.	RW	0
9	CLKXM	Transmitter Clock Mode 0x0: Transmitter clock is driven by an external clock with CLKX as an input pin. 0x1: CLKX is an output pin and is driven by the internal sample rate generator.	RW	0
8	CLKRM	Receiver Clock Mode 0x0: Case 1: Digital loopback mode not set (DLB=0) in SPCR1: Receive clock (CLKR) is an input driven by an externaal clock. Case 2: Digital loopback mode set (DLB=1) in SPCR1: Receive clock (not the CLKR pin) is driven by transmit clock (CLKX) which is based on the CLKXM bit in the PCR. CLKR pin is in high-impedance. 0x1: Case 1: Digital loopback mode not set (DLB=0) in SPCR1: CLKR is an output pin and is driven by the internal SRG. Case 2: Digital loopback mode set (DLB=1) in SPCR1: CLKR is an output pin and is driven by the transmit clock. The transmit clock is derived based on the CLKRM bit in the PCR.	RW	0
7	SCLKME	The frequency of CLKG is: CLKG frequency = (Input clock frequency) / (CLKGDV + 1) SCLKME is used in conjunction with the CLKSM bit to select the input clock: 0x0: CLKSM = 0: Signal on CLKS pin CLKSM = 1: CPU clock 0x1: CLKSM = 0: Signal on CLKR pin CLKSM = 1: Signal on CLKX pin	RW	0
6	CLKS_STAT	CLKS pin status. Reflects value on CLKS pin when selected as a general purpose input. (legacy) Read 0x0: The signal on the CLKS pin is low Read 0x1: The signal on the CLKS pin is high	R	0
5	DX_STAT	DX pin status. Reflects value driven on to DX pin when selected as a general purpose output. (legacy) 0x0: Drive the signal on the DX pin low 0x1: Drive the signal on the DX pin high	RW	0
4	DR_STAT	DR pin status. Reflects value on DR pin when selected as a general purpose input. (legacy) Read 0x0: The signal on DR pin is low Read 0x1: The signal on DR pin is high	R	0
3	FSXP	Transmit Frame-Synchronization Polarity 0x0: Frame-sync pulse FSX is active high 0x1: Frame-sync pulse FSX is active low	RW	0
2	FSRP	Receive Frame-Synchronization Polarity 0x0: Frame-sync pulse FSR is active high 0x1: Frame-sync pulse FSR is active low	RW	0
1	CLKXP	Transmit Clock Polarity 0x0: Transmit data driven on rising edge of CLKX 0x1: Transmit data driven on falling edge of CLKX	RW	0

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Bits	Field Name	Description	Type	Reset
0	CLKRP	Receive Clock Polarity 0x0: Receive data sampled on falling edge of CLKR 0x1: Receive data sampled on rising edge of CLKR	RW	0

Table 23-401. Register Call Summary for Register MCBSPLP_PCR_REG

Multichannel Buffered Serial Port (McBSP)

- Words, Frames, and Phases Definitions: [0] [1]
- McBSP1 Clocks: [2]
- McBSP2 Clocks: [3]
- McBSP3 Clocks: [4]
- McBSP4 Clocks: [5]
- Analysis of the Receiver Smart-Idle Behavior: [6] [7]
- Clocking and Framing Data: [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23] [24] [25] [26] [27] [28] [29] [30] [31] [32] [33] [34] [35] [36] [37] [38] [39]
- Frame Phases (Dual-Phase Frame I2S Support): [40] [41] [42] [43] [44] [45] [46] [47]
- MCBSP Data Transfer Mode: [48] [49]
- McBSP SRG: [50] [51] [52] [53] [54]
- Clock Generation in the SRG: [55] [56] [57] [58]
- Frame-Sync Generation in the SRG: [59] [60]
- Synchronizing SRG Outputs to an External Clock: [61] [62] [63] [64]
- Underflow in the Transmitter: [65]
- McBSP Initialization Procedure: [66] [67]
- Reset and Initialization Procedure for the SRG: [68]
- Programming the McBSP Registers for the Desired Receiver Configuration (Step 2): [69] [70] [71] [72] [73] [74] [75] [76]
- Programming the McBSP Registers for the Desired Transmitter Operation (Step 2): [77] [78] [79] [80] [81] [82] [83] [84]
- GPIO on the McBSP Pins (Legacy Only): [85] [86] [87] [88]
- MCBSP Register Summary: [89] [90] [91] [92]

Table 23-402. MCBSPLP_RCERC_REG

Address Offset	0x0000 004C		
Physical Address	0x4902 204C 0x4012 204C 0x2 204C 0x4902 404C 0x4012 404C 0x2 404C 0x4902 604C 0x4012 604C 0x2 604C	**Instance**	MCBSP1_L3 MCBSP1_CORTEX-A9 MCBSP1_DSP MCBSP2_L3 MCBSP2_CORTEX-A9 MCBSP2_DSP MCBSP3_L3 MCBSP3_CORTEX-A9 MCBSP3_DSP
Description	McBSPLP receive channel enable register partition C		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RCERC															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x0000
15:0	RCERC	Receive Channel Enable RCERC n=0 Disables reception of n-th channel in an even-numbered block in partition C RCERC n=1 Enables reception of n-th channel in an even-numbered block in partition C	RW	0x0000

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Table 23-403. Register Call Summary for Register MCBSPLP_RCERC_REG

Multichannel Buffered Serial Port (McBSP)

- Using Eight Partitions: [0]
- MCBSP Register Summary: [1] [2] [3] [4]

Table 23-404. MCBSPLP_RCERD_REG

Address Offset	0x0000 0050		
Physical Address	0x4902 2050 0x4012 2050 0x2 2050 0x4902 4050 0x4012 4050 0x2 4050 0x4902 6050 0x4012 6050 0x2 6050	**Instance**	MCBSP1_L3 MCBSP1_CORTEX-A9 MCBSP1_DSP MCBSP2_L3 MCBSP2_CORTEX-A9 MCBSP2_DSP MCBSP3_L3 MCBSP3_CORTEX-A9 MCBSP3_DSP
Description	McBSPLP receive channel enable register partition D		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RCERD															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x0000
15:0	RCERD	Receive Channel Enable RCERD n=0 Disables reception of n-th channel in an even-numbered block in partition D RCERD n=1 Enables reception of n-th channel in an even-numbered block in partition D	RW	0x0000

Table 23-405. Register Call Summary for Register MCBSPLP_RCERD_REG

Multichannel Buffered Serial Port (McBSP)

- Using Eight Partitions: [0]
- MCBSP Register Summary: [1] [2] [3] [4]

Table 23-406. MCBSPLP_XCERC_REG

Address Offset	0x0000 0054		
Physical Address	0x4902 2054 0x4012 2054 0x2 2054 0x4902 4054 0x4012 4054 0x2 4054 0x4902 6054 0x4012 6054 0x2 6054	**Instance**	MCBSP1_L3 MCBSP1_CORTEX-A9 MCBSP1_DSP MCBSP2_L3 MCBSP2_CORTEX-A9 MCBSP2_DSP MCBSP3_L3 MCBSP3_CORTEX-A9 MCBSP3_DSP
Description	McBSPLP transmit channel enable register partition C		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																XCERC															

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Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x0000
15:0	XCERC	Transmit Channel Enable XCERC n=0 Disables transmission of n-th channel in an event-numbered block in partition C XCERC n=1 Enables transmission of n-th channel in an event-numbered block in partition C	RW	0x0000

Table 23-407. Register Call Summary for Register MCBSPLP_XCERC_REG

Multichannel Buffered Serial Port (McBSP)
- Using Eight Partitions: [0]
- MCBSP Register Summary: [1] [2] [3] [4]

Table 23-408. MCBSPLP_XCERD_REG

Address Offset	0x0000 0058		
Physical Address	0x4902 2058 0x4012 2058 0x2 2058 0x4902 4058 0x4012 4058 0x2 4058 0x4902 6058 0x4012 6058 0x2 6058	**Instance**	MCBSP1_L3 MCBSP1_CORTEX-A9 MCBSP1_DSP MCBSP2_L3 MCBSP2_CORTEX-A9 MCBSP2_DSP MCBSP3_L3 MCBSP3_CORTEX-A9 MCBSP3_DSP
Description	McBSPLP transmit channel enable register partition D		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																XCERD															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x0000
15:0	XCERD	Transmit Channel Enable XCERD n=0 Disables transmission of n-th channel in an even-numbered block in partition D XCERD n=1 Enables transmission of n-th channel in an even-numbered block in partition D	RW	0x0000

Table 23-409. Register Call Summary for Register MCBSPLP_XCERD_REG

Multichannel Buffered Serial Port (McBSP)
- Using Eight Partitions: [0]
- MCBSP Register Summary: [1] [2] [3] [4]

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Table 23-410. MCBSPLP_RCERE_REG

Address Offset	0x0000 005C		
Physical Address	0x4902 205C 0x4012 205C 0x2 205C 0x4902 405C 0x4012 405C 0x2 405C 0x4902 605C 0x4012 605C 0x2 605C	**Instance**	MCBSP1_L3 MCBSP1_CORTEX-A9 MCBSP1_DSP MCBSP2_L3 MCBSP2_CORTEX-A9 MCBSP2_DSP MCBSP3_L3 MCBSP3_CORTEX-A9 MCBSP3_DSP
Description	McBSPLP receive channel enable register partition E		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RCERE															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x0000
15:0	RCERE	Receive Channel Enable RCERE n=0 Disables reception of n-th channel in an even-numbered block in partition E RCERE n=1 Enables reception of n-th channel in an even-numbered block in partition E	RW	0x0000

Table 23-411. Register Call Summary for Register MCBSPLP_RCERE_REG

Multichannel Buffered Serial Port (McBSP)

- Using Eight Partitions: [0]
- MCBSP Register Summary: [1] [2] [3] [4]

Table 23-412. MCBSPLP_RCERF_REG

Address Offset	0x0000 0060		
Physical Address	0x4902 2060 0x4012 2060 0x2 2060 0x4902 4060 0x4012 4060 0x2 4060 0x4902 6060 0x4012 6060 0x2 6060	**Instance**	MCBSP1_L3 MCBSP1_CORTEX-A9 MCBSP1_DSP MCBSP2_L3 MCBSP2_CORTEX-A9 MCBSP2_DSP MCBSP3_L3 MCBSP3_CORTEX-A9 MCBSP3_DSP
Description	McBSPLP receive channel enable register partition F		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RCERF															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x0000
15:0	RCERF	Receive Channel Enable RCERF n=0 Disables reception of n-th channel in an even-numbered block in partition F RCERF n=1 Enables reception of n-th channel in an even-numbered block in partition F	RW	0x0000

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Table 23-413. Register Call Summary for Register MCBSPLP_RCERF_REG

Multichannel Buffered Serial Port (McBSP)

- Using Eight Partitions: [0]
- MCBSP Register Summary: [1] [2] [3] [4]

Table 23-414. MCBSPLP_XCERE_REG

Address Offset	0x0000 0064		
Physical Address	0x4902 2064	**Instance**	MCBSP1_L3
	0x4012 2064		MCBSP1_CORTEX-A9
	0x2 2064		MCBSP1_DSP
	0x4902 4064		MCBSP2_L3
	0x4012 4064		MCBSP2_CORTEX-A9
	0x2 4064		MCBSP2_DSP
	0x4902 6064		MCBSP3_L3
	0x4012 6064		MCBSP3_CORTEX-A9
	0x2 6064		MCBSP3_DSP
Description	McBSPLP transmit channel enable register partition E		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																XCERE															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x0000
15:0	XCERE	Transmit Channel Enable XCERE n=0 Disables transmission of n-th channel in an event-numbered block in partition E XCERE n=1 Enables transmission of n-th channel in an event-numbered block in partition E	RW	0x0000

Table 23-415. Register Call Summary for Register MCBSPLP_XCERE_REG

Multichannel Buffered Serial Port (McBSP)

- Using Eight Partitions: [0]
- MCBSP Register Summary: [1] [2] [3] [4]

Table 23-416. MCBSPLP_XCERF_REG

Address Offset	0x0000 0068		
Physical Address	0x4902 2068	**Instance**	MCBSP1_L3
	0x4012 2068		MCBSP1_CORTEX-A9
	0x2 2068		MCBSP1_DSP
	0x4902 4068		MCBSP2_L3
	0x4012 4068		MCBSP2_CORTEX-A9
	0x2 4068		MCBSP2_DSP
	0x4902 6068		MCBSP3_L3
	0x4012 6068		MCBSP3_CORTEX-A9
	0x2 6068		MCBSP3_DSP
Description	McBSPLP transmit channel enable register partition F		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																XCERF															

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Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x0000
15:0	XCERF	Transmit Channel Enable XCERF n=0 Disables transmission of n-th channel in an even-numbered block in partition F XCERF n=1 Enables transmission of n-th channel in an even-numbered block in partition F	RW	0x0000

Table 23-417. Register Call Summary for Register MCBSPLP_XCERF_REG

Multichannel Buffered Serial Port (McBSP)
- Using Eight Partitions: [0]
- MCBSP Register Summary: [1] [2] [3] [4]

Table 23-418. MCBSPLP_RCERG_REG

Address Offset	0x0000 006C		
Physical Address	0x4902 206C 0x4012 206C 0x2 206C 0x4902 406C 0x4012 406C 0x2 406C 0x4902 606C 0x4012 606C 0x2 606C	**Instance**	MCBSP1_L3 MCBSP1_CORTEX-A9 MCBSP1_DSP MCBSP2_L3 MCBSP2_CORTEX-A9 MCBSP2_DSP MCBSP3_L3 MCBSP3_CORTEX-A9 MCBSP3_DSP
Description	McBSPLP receive channel enable register partition G		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RCERG															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x0000
15:0	RCERG	Receive Channel Enable RCERG n=0 Disables reception of n-th channel in an even-numbered block in partition G RCERG n=1 Enables reception of n-th channel in an even-numbered block in partition G	RW	0x0000

Table 23-419. Register Call Summary for Register MCBSPLP_RCERG_REG

Multichannel Buffered Serial Port (McBSP)
- Using Eight Partitions: [0]
- MCBSP Register Summary: [1] [2] [3] [4]

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Table 23-420. MCBSPLP_RCERH_REG

Address Offset	0x0000 0070		
Physical Address	0x4902 2070	**Instance**	MCBSP1_L3
	0x4012 2070		MCBSP1_CORTEX-A9
	0x2 2070		MCBSP1_DSP
	0x4902 4070		MCBSP2_L3
	0x4012 4070		MCBSP2_CORTEX-A9
	0x2 4070		MCBSP2_DSP
	0x4902 6070		MCBSP3_L3
	0x4012 6070		MCBSP3_CORTEX-A9
	0x2 6070		MCBSP3_DSP
Description	McBSPLP receive channel enable register partition H		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RCERH															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x0000
15:0	RCERH	Receive Channel Enable RCERH n=0 Disables reception of n-th channel in an even-numbered block in partition H RCERH n=1 Enables reception of n-th channel in an even-numbered block in partition H	RW	0x0000

Table 23-421. Register Call Summary for Register MCBSPLP_RCERH_REG

Multichannel Buffered Serial Port (McBSP)

- Using Eight Partitions: [0]
- Receive Multichannel Selection Mode: [1] [2]
- Transmit Multichannel Selection Modes: [3] [4]
- MCBSP Register Summary: [5] [6] [7] [8]

Table 23-422. MCBSPLP_XCERG_REG

Address Offset	0x0000 0074		
Physical Address	0x4902 2074	**Instance**	MCBSP1_L3
	0x4012 2074		MCBSP1_CORTEX-A9
	0x2 2074		MCBSP1_DSP
	0x4902 4074		MCBSP2_L3
	0x4012 4074		MCBSP2_CORTEX-A9
	0x2 4074		MCBSP2_DSP
	0x4902 6074		MCBSP3_L3
	0x4012 6074		MCBSP3_CORTEX-A9
	0x2 6074		MCBSP3_DSP
Description	McBSPLP transmit channel enable register partition G		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																XCERG															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x0000
15:0	XCERG	Transmit Channel Enable XCERG n=0 Disables transmission of n-th channel in an event-numbered block in partition G XCERG n=1 Enables transmission of n-th channel in an event-numbered block in partition G	RW	0x0000

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Table 23-423. Register Call Summary for Register MCBSPLP_XCERG_REG

Multichannel Buffered Serial Port (McBSP)

- Using Eight Partitions: [0]
- MCBSP Register Summary: [1] [2] [3] [4]

Table 23-424. MCBSPLP_XCERH_REG

Address Offset	0x0000 0078		
Physical Address	0x4902 2078	**Instance**	MCBSP1_L3
	0x4012 2078		MCBSP1_CORTEX-A9
	0x2 2078		MCBSP1_DSP
	0x4902 4078		MCBSP2_L3
	0x4012 4078		MCBSP2_CORTEX-A9
	0x2 4078		MCBSP2_DSP
	0x4902 6078		MCBSP3_L3
	0x4012 6078		MCBSP3_CORTEX-A9
	0x2 6078		MCBSP3_DSP
Description	McBSPLP transmit channel enable register partition H		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																XCERH															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x0000
15:0	XCERH	Transmit Channel Enable XCERH n=0 Disables transmission of n-th channel in an even-numbered block in partition H XCERH n=1 Enables transmission of n-th channel in an even-numbered block in partition H	RW	0x0000

Table 23-425. Register Call Summary for Register MCBSPLP_XCERH_REG

Multichannel Buffered Serial Port (McBSP)

- Using Eight Partitions: [0]
- Transmit Multichannel Selection Modes: [1] [2] [3] [4] [5] [6]
- MCBSP Register Summary: [7] [8] [9] [10]

Table 23-426. MCBSPLP_REV_REG

Address Offset	0x0000 007C		
Physical Address	0x4902 207C	**Instance**	MCBSP1_L3
	0x4012 207C		MCBSP1_CORTEX-A9
	0x2 207C		MCBSP1_DSP
	0x4902 407C		MCBSP2_L3
	0x4012 407C		MCBSP2_CORTEX-A9
	0x2 407C		MCBSP2_DSP
	0x4902 607C		MCBSP3_L3
	0x4012 607C		MCBSP3_CORTEX-A9
	0x2 607C		MCBSP3_DSP
Description	MCBSPLP Revision number register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								REV							

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Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Reserved	R	0x000000
7:0	REV	Revision number	R	0x11

Table 23-427. Register Call Summary for Register MCBSPLP_REV_REG

Multichannel Buffered Serial Port (McBSP)

- MCBSP Register Summary: [0] [1] [2] [3]

Table 23-428. MCBSPLP_RINTCLR_REG

Address Offset	0x0000 0080		
Physical Address	0x4902 2080 0x4012 2080 0x2 2080 0x4902 4080 0x4012 4080 0x2 4080 0x4902 6080 0x4012 6080 0x2 6080	**Instance**	MCBSP1_L3 MCBSP1_CORTEX-A9 MCBSP1_DSP MCBSP2_L3 MCBSP2_CORTEX-A9 MCBSP2_DSP MCBSP3_L3 MCBSP3_CORTEX-A9 MCBSP3_DSP
Description	McBSPLP receive interrupt clear		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RINTCLR																															

Bits	Field Name	Description	Type	Reset
31:0	RINTCLR	Read from this register will clear the IRQ generated by receive end-of-frame indication or MCBSPLP.FSR detection. Write to this register has no effect. (legacy)	RW	0x0000 0000

Table 23-429. Register Call Summary for Register MCBSPLP_RINTCLR_REG

Multichannel Buffered Serial Port (McBSP)

- MCBSP Register Summary: [0] [1] [2] [3]

Table 23-430. MCBSPLP_XINTCLR_REG

Address Offset	0x0000 0084		
Physical Address	0x4902 2084 0x4012 2084 0x2 2084 0x4902 4084 0x4012 4084 0x2 4084 0x4902 6084 0x4012 6084 0x2 6084	**Instance**	MCBSP1_L3 MCBSP1_CORTEX-A9 MCBSP1_DSP MCBSP2_L3 MCBSP2_CORTEX-A9 MCBSP2_DSP MCBSP3_L3 MCBSP3_CORTEX-A9 MCBSP3_DSP
Description	McBSPLP transmit interrupt clear (legacy)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
XINTCLR																															

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Bits	Field Name	Description	Type	Reset
31:0	XINTCLR	Read from this register will clear the IRQ generated by transmit end-of-frame indication or MCBSPLP.FSX detection. Write to this register has no effect.	RW	0x0000 0000

Table 23-431. Register Call Summary for Register MCBSPLP_XINTCLR_REG

Multichannel Buffered Serial Port (McBSP)

- MCBSP Register Summary: [0] [1] [2] [3]

Table 23-432. MCBSPLP_ROVFLCLR_REG

Address Offset	0x0000 0088		
Physical Address	0x4902 2088	**Instance**	MCBSP1_L3
	0x4012 2088		MCBSP1_CORTEX-A9
	0x2 2088		MCBSP1_DSP
	0x4902 4088		MCBSP2_L3
	0x4012 4088		MCBSP2_CORTEX-A9
	0x2 4088		MCBSP2_DSP
	0x4902 6088		MCBSP3_L3
	0x4012 6088		MCBSP3_CORTEX-A9
	0x2 6088		MCBSP3_DSP
Description	McBSPLP receive overflow interrupt clear		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ROVFLCLR																															

Bits	Field Name	Description	Type	Reset
31:0	ROVFLCLR	Read from this register will clear the IRQ generated by the receive overflow condition. Write to this register has no effect.	RW	0x0000 0000

Table 23-433. Register Call Summary for Register MCBSPLP_ROVFLCLR_REG

Multichannel Buffered Serial Port (McBSP)

- MCBSP Register Summary: [0] [1] [2] [3]

Table 23-434. MCBSPLP_SYSCONFIG_REG

Address Offset	0x0000 008C		
Physical Address	0x4902 208C	**Instance**	MCBSP1_L3
	0x4012 208C		MCBSP1_CORTEX-A9
	0x2 208C		MCBSP1_DSP
	0x4902 408C		MCBSP2_L3
	0x4012 408C		MCBSP2_CORTEX-A9
	0x2 408C		MCBSP2_DSP
	0x4902 608C		MCBSP3_L3
	0x4012 608C		MCBSP3_CORTEX-A9
	0x2 608C		MCBSP3_DSP
Description	McBSPLP System Configuration register		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						CLOCKACTIVITY		RESERVED				SIDLEMODE		ENAWAKEUP	SOFTRESET	RESERVED	

Bits	Field Name	Description	Type	Reset
31:10	RESERVED	Reserved	R	0x000000
9:8	CLOCKACTIVITY	0x0: The MCBSPi_ICLK clock can be switched off. The PRCM functional clock can be switched off. 0x1: The MCBSPi_ICLK clock must be maintained during wakeup. The PRCM functional clock can be switched off. 0x2: The MCBSPi_ICLK clock can be switched off. The PRCM functional clock must be maintained during wakeup. 0x3: The MCBSPi_ICLK clock must be maintained during wakeup. The PRCM functional clock must be maintained during wakeup	RW	0x0
7:5	RESERVED	Reserved	R	0x0
4:3	SIDLEMODE	Slave interface power management, req/ack control: 0x0: Force-idle. An idle request is acknowledged unconditionally. 0x1: No-idle. An idle request is never acknowledged. 0x2: Smart-idle. Acknowledgement to an idle request is given based on the internal activity of the module 0x3: Reserved	RW	0x0
2	ENAWAKEUP	WakeUp feature control: 0x0: WakeUp is disabled 0x1: WakeUp capability is enabled	RW	0
1	SOFTRESET	McBSPLP global software reset 0x0: NO soft reset 0x1: Soft reset triggered	RW	0
0	RESERVED	Reserved	R	0

Table 23-435. Register Call Summary for Register MCBSPLP_SYSCONFIG_REG

Multichannel Buffered Serial Port (McBSP)

- McBSP Software Reset: [0]
- McBSP Acknowledgment Modes: [1] [2] [3] [4]
- Wake-Up Capability: [5]
- Analysis of the Receiver Smart-Idle Behavior: [6]
- McBSP Initialization Procedure: [7]
- MCBSP Register Summary: [8] [9] [10] [11]

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Table 23-436. MCBSPLP_THRSH2_REG

Address Offset	0x0000 0090		
Physical Address	0x4902 2090	**Instance**	MCBSP1_L3
	0x4012 2090		MCBSP1_CORTEX-A9
	0x2 2090		MCBSP1_DSP
	0x4902 4090		MCBSP2_L3
	0x4012 4090		MCBSP2_CORTEX-A9
	0x2 4090		MCBSP2_DSP
	0x4902 6090		MCBSP3_L3
	0x4012 6090		MCBSP3_CORTEX-A9
	0x2 6090		MCBSP3_DSP
Description	McBSPLP transmit buffer threshold (DMA or IRQ trigger)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								XTHRESHOLD							

Bits	Field Name	Description	Type	Reset
31:7	RESERVED	Reserved	R	0x0000000
6:0	XTHRESHOLD	Transmit buffer threshold value. The DMA request (if enabled) of interrupt assertion (if enabled) will be triggered if the number of free locations inside transmit buffer are above or equal to the XTHRESHOLD value + 1. Also, this value (XTHRESHOLD value + 1) indicates the number of words transferred during a transmit data DMA request, if transmit DMA is enabled	RW	0x00

Table 23-437. Register Call Summary for Register MCBSPLP_THRSH2_REG

Multichannel Buffered Serial Port (McBSP)

- Wake-Up Capability: [0]
- McBSP Transmission: [1]
- McBSP DMA Configuration: [2]
- McBSP Initialization Procedure: [3]
- Data Transfer DMA Request Configuration: [4]
- Programming the McBSP Registers for the Desired Transmitter Operation (Step 2): [5]
- MCBSP Register Summary: [6] [7] [8] [9]

Table 23-438. MCBSPLP_THRSH1_REG

Address Offset	0x0000 0094		
Physical Address	0x4902 2094	**Instance**	MCBSP1_L3
	0x4012 2094		MCBSP1_CORTEX-A9
	0x2 2094		MCBSP1_DSP
	0x4902 4094		MCBSP2_L3
	0x4012 4094		MCBSP2_CORTEX-A9
	0x2 4094		MCBSP2_DSP
	0x4902 6094		MCBSP3_L3
	0x4012 6094		MCBSP3_CORTEX-A9
	0x2 6094		MCBSP3_DSP
Description	McBSPLP receive buffer threshold (DMA or IRQ trigger)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RTHRESHOLD							

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Bits	Field Name	Description	Type	Reset
31:7	RESERVED	Reserved	R	0x0000000
6:0	RTHRESHOLD	Receive buffer threshold value. The DMA request (if enabled) of interrupt assertion (if enabled) will be triggered if the number of occupied locations inside receive buffer are above or equal to the RTHRESHOLD value + 1. Also, this value (RTHRESHOLD value + 1) indicates the number of words transferred during a receive data DMA request, if receive DMA is enabled.	RW	0x00

Table 23-439. Register Call Summary for Register MCBSPLP_THRSH1_REG

Multichannel Buffered Serial Port (McBSP)

- Wake-Up Capability: [0]
- McBSP Reception: [1]
- McBSP DMA Configuration: [2]
- Data Transfer DMA Request Configuration: [3]
- Programming the McBSP Registers for the Desired Receiver Configuration (Step 2): [4]
- MCBSP Register Summary: [5] [6] [7] [8]

Table 23-440. MCBSPLP_IRQSTATUS_REG

Address Offset	0x0000 00A0		
Physical Address	0x4902 20A0	**Instance**	MCBSP1_L3
	0x4012 20A0		MCBSP1_CORTEX-A9
	0x2 20A0		MCBSP1_DSP
	0x4902 40A0		MCBSP2_L3
	0x4012 40A0		MCBSP2_CORTEX-A9
	0x2 40A0		MCBSP2_DSP
	0x4902 60A0		MCBSP3_L3
	0x4012 60A0		MCBSP3_CORTEX-A9
	0x2 60A0		MCBSP3_DSP
Description	McBSPLP Interrupt Status register (interconnect compliant IRQ line)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																XEMPTYEOF	RESERVED	XOVFLSTAT	XUNDFLSTAT	XRDY	XEOF	XFSX	XSYNCERR	RESERVED	ROVFLSTAT	RUNDFLSTAT	RRDY	REOF	RFSR	RSYNCERR	

Bits	Field Name	Description	Type	Reset
31:15	RESERVED	Reserved	R	0x00000
14	XEMPTYEOF	Transmit Buffer Empty at end of frame (XEMPTYEOF is set to 1 when a complete frame was transmitted and the transmit buffer is empty). 0x0: XEMPTYEOF is NOT set to when a complete frame was transmitted and the transmit buffer is empty 0x1: XEMPTYEOF is set to 1 when a complete frame was transmitted and the transmit buffer is empty. Writing 1 to this bit clears the bit.	RW	0
13	RESERVED	Reserved	R	0
12	XOVFLSTAT	Transmit Buffer Overflow (XOVFLSTAT bit is set to 1 when transmit buffer overflow; the data which is written while overflow condition is discarded). Writing 1 to this bit clears the bit. 0x0: Transmit buffer NOT overflow 0x1: Transmit buffer overflow; Writing 1 to this bit clears the bit.	RW	0

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Bits	Field Name	Description	Type	Reset
11	XUNDFLSTAT	Transmit Buffer Underflow (XUNDFLSTAT bit is set to 1 when the transmit data buffer is empty new data is required to be transmitted). Writing 1 to this bit clears the bit. 0x0: the transmit data buffer is NOT empty new data is required to be transmitted. 0x1: the transmit data buffer is empty new data is required to be transmitted. Writing 1 to this bit clears the bit.	RW	0
10	XRDY	Transmit Buffer Threshold Reached (XRDY bit is set to 1 when the transmit buffer free locations are equal or above the THRSH2_REG value). Writing 1 to this bit clears the bit. 0x0: Transmit buffer occupied locations are below the THRSH2_REG value). 0x1: Transmit buffer occupied locations are equal or above the THRSH2_REG value). Writing 1 to this bit clears the bit.	RW	0
9	XEOF	Transmit End Of Frame (XEOF is set to 1 when a complete frame was transmitted). Writing 1 to this bit clears the bit. 0x0: complete frame was NOT transmitted 0x1: complete frame was transmitted; Writing 1 to this bit clears the bit.	RW	0
8	XFSX	Transmit Frame Synchronization (XFSX bit is set to 1 when a new transmit frame synchronization is asserted). Writing 1 to this bit clears the bit. 0x0: new transmit frame synchronization is NOT asserted 0x1: new transmit frame synchronization is asserted; Writing 1 to this bit clears the bit.	RW	0
7	XSYNCERR	Transmit Frame Synchronization Error (XSYNCERR is set to 1 when a transmit frame-sync error is detected). Writing 1 to this bit clears the bit. 0x0: Transmit frame-sync error is NOT detected 0x1: Transmit frame-sync error is detected. Writing 1 to this bit clears the bit.	RW	0
6	RESERVED	Reserved	R	0
5	ROVFLSTAT	Receive Buffer Overflow (ROVFLSTAT bit is set to 1 when receive buffer overflow; the data which is written while overflow condition is discarded). Writing 1 to this bit clears the bit. 0x0: receive buffer NOT overflow 0x1: receive buffer overflow; Writing 1 to this bit clears the bit.	RW	0
4	RUNDFLSTAT	Receive Buffer Underflow (RUNDFLSTAT bit is set to 1 when read operation is performed to the receive data register while receive buffer is empty; data read while underflow condition is undefined). Writing 1 to this bit clears the bit. 0x0: read operation is performed to the receive data register while receive buffer is NOT empty 0x1: read operation is performed to the receive data register while receive buffer is empty; Writing 1 to this bit clears the bit.	RW	0

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Bits	Field Name	Description	Type	Reset
3	RRDY	Receive Buffer Threshold Reached (RRDY bit is set to 1 when the receive buffer occupied locations are equal or above the THRSH1_REG value). Writing 1 to this bit clears the bit. 0x0: receive buffer occupied locations are below the THRSH1_REG value). 0x1: receive buffer occupied locations are equal or above the THRSH1_REG value). Writing 1 to this bit clears the bit.	RW	0
2	REOF	Receive End Of Frame (REOF is set to 1 when a complete frame was received). Writing 1 to this bit clears the bit. 0x0: complete frame was NOT received 0x1: complete frame was received; Writing 1 to this bit clears the bit.	RW	0
1	RFSR	Receive Frame Synchronization (RFSR bit is set to 1 when a new receive frame synchronization is asserted). Writing 1 to this bit clears the bit. 0x0: new receive frame synchronization is NOT asserted 0x1: new receive frame synchronization is asserted; Writing 1 to this bit clears the bit.	RW	0
0	RSYNCERR	Receive Frame Synchronization Error (RSYNCERR is set to 1 when a receive frame-sync error is detected). Writing 1 to this bit clears the bit. 0x0: Receive frame-synchronization error is NOT detected 0x1: Receive frame-synchronization error is detected. Writing 1 to this bit clears the bit.	RW	0

Table 23-441. Register Call Summary for Register MCBSPLP_IRQSTATUS_REG

Multichannel Buffered Serial Port (McBSP)

- Wake-Up Capability: [0] [1] [2] [3]
- McBSP Interrupt Requests: [4] [5]
- Enable/Disable the Transmit and Receive Processes: [6] [7] [8] [9]
- Introduction: [10] [11] [12] [13] [14] [15] [16]
- Overrun in the Receiver: [17] [18] [19]
- Unexpected Receive Frame-Sync Pulse: [20] [21]
- Underflow in the Receiver: [22] [23]
- Underflow in the Transmitter: [24] [25] [26]
- Unexpected Transmit Frame-Sync Pulse: [27]
- Overflow in the Transmitter: [28]
- MCBSP Register Summary: [29] [30] [31] [32]

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Table 23-442. MCBSPLP_IRQENABLE_REG

Address Offset	0x0000 00A4		
Physical Address	0x4902 20A4 0x4012 20A4 0x2 20A4 0x4902 40A4 0x4012 40A4 0x2 40A4 0x4902 60A4 0x4012 60A4 0x2 60A4	**Instance**	MCBSP1_L3 MCBSP1_CORTEX-A9 MCBSP1_DSP MCBSP2_L3 MCBSP2_CORTEX-A9 MCBSP2_DSP MCBSP3_L3 MCBSP3_CORTEX-A9 MCBSP3_DSP
Description	McBSPLP Interrupt Enable register (interconnect compliant IRQ line)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																	XEMPTYEOFEN	RESERVED	XOVFLEN	XUNDFLEN	XRDYEN	XEOFEN	XFSXEN	XSYNCERREN	RESERVED	ROVFLEN	RUNDFLEN	RRDYEN	REOFEN	RFSREN	RSYNCERREN

Bits	Field Name	Description	Type	Reset
31:15	RESERVED	Reserved	R	0x00000
14	XEMPTYEOFEN	Transmit buffer empty at end of frame enable bit. 0x0: Transmit Buffer Empty at End Of Frame NOT enabled 0x1: Transmit Buffer Empty at End Of Frame enabled	RW	0
13	RESERVED	Reserved	R	0
12	XOVFLEN	Transmit Buffer Overflow enable bit. 0x0: Transmit Buffer Overflow NOT enabled 0x1: Transmit Buffer Overflow enabled	RW	0
11	XUNDFLEN	Transmit Buffer Underflow enable bit. 0x0: Transmit Buffer Underflow NOT enabled 0x1: Transmit Buffer Underflow enabled	RW	0
10	XRDYEN	Transmit Buffer Threshold Reached enable bit. 0x0: Transmit Buffer Threshold Reached NOT enabled 0x1: Transmit Buffer Threshold Reached enabled	RW	0
9	XEOFEN	Transmit End Of Frame enable bit. 0x0: Transmit End Of Frame NOT enabled 0x1: Transmit End Of Frame enabled	RW	0
8	XFSXEN	Transmit Frame Synchronization enable bit. 0x0: Transmit Frame Synchronization NOT enabled 0x1: Transmit Frame Synchronization enabled	RW	0
7	XSYNCERREN	Transmit Frame Synchronization Error enable bit. 0x0: Transmit Frame Synchronization Error NOT enabled 0x1: Transmit Frame Synchronization Error enabled	RW	0
6	RESERVED	Reserved	R	0
5	ROVFLEN	Receive Buffer Overflow enable bit. 0x0: Receive Buffer Overflow NOT enabled 0x1: Receive Buffer Overflow enabled	RW	0

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Bits	Field Name	Description	Type	Reset
4	RUNDFLEN	Receive Buffer Underflow enable bit. 0x0: Receive Buffer Underflow NOT enabled 0x1: Receive Buffer Underflow enabled	RW	0
3	RRDYEN	Receive Buffer Threshold enable bit. 0x0: Receive Buffer Threshold NOT enabled 0x1: Receive Buffer Threshold enabled	RW	0
2	REOFEN	Receive End Of Frame enable bit. 0x0: Receive End Of Frame NOT enabled 0x1: Receive End Of Frame enabled	RW	0
1	RFSREN	Receive Frame Synchronization enable bit. RW 0x0: Receive Frame Synchronization NOT enabled 0x1: Receive Frame Synchronization enabled	RW	0
0	RSYNCERREN	Receive Frame Synchronization Error enable bit. 0x0: Receive Frame Synchronization Error NOT enabled 0x1: Receive Frame Synchronization Error enabled	RW	0

Table 23-443. Register Call Summary for Register MCBSPLP_IRQENABLE_REG

Multichannel Buffered Serial Port (McBSP)

- Wake-Up Capability: [0] [1] [2] [3] [4] [5] [6] [7] [8]
- McBSP Interrupt Requests: [9]
- Overrun in the Receiver: [10]
- Unexpected Receive Frame-Sync Pulse: [11]
- Underflow in the Receiver: [12]
- Underflow in the Transmitter: [13]
- Unexpected Transmit Frame-Sync Pulse: [14]
- Overflow in the Transmitter: [15]
- Interrupt Configuration: [16]
- Programming the McBSP Registers for the Desired Transmitter Operation (Step 2): [17]
- MCBSP Register Summary: [18] [19] [20] [21]

Table 23-444. MCBSPLP_WAKEUPEN_REG

Address Offset	0x0000 00A8		
Physical Address	0x4902 20A8 0x4012 20A8 0x2 20A8 0x4902 40A8 0x4012 40A8 0x2 40A8 0x4902 60A8 0x4012 60A8 0x2 60A8	**Instance**	MCBSP1_L3 MCBSP1_CORTEX-A9 MCBSP1_DSP MCBSP2_L3 MCBSP2_CORTEX-A9 MCBSP2_DSP MCBSP3_L3 MCBSP3_CORTEX-A9 MCBSP3_DSP
Description	McBSPLP Wakeup Enable register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																	XEMPTYEOFEN	RESERVED			XRDYEN	XEOFEN	XFSXEN	XSYNCERREN	RESERVED				RRDYEN	REOFEN	RFSREN	RSYNCERREN

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Bits	Field Name	Description	Type	Reset
31:15	RESERVED	Reserved	R	0x00000
14	XEMPTYEOFEN	Transmit Buffer Empty at End Of Frame enable bit. 0x0: Transmit Buffer Empty at End Of Frame WK enable is NOT active 0x1: Transmit Buffer Empty at End Of Frame WK enable is active	RW	0
13:11	RESERVED	Reserved	R	0x0
10	XRDYEN	Transmit Buffer Threshold Reached WK enable bit. 0x0: Transmit Buffer Threshold WK enable is NOT active 0x1: Transmit Buffer Threshold WK enable is active	RW	0
9	XEOFEN	Transmit End Of Frame WK enable bit. 0x0: Transmit End Of Frame WK enable is NOT active 0x1: Transmit End Of Frame WK enable is active	RW	0
8	XFSXEN	Transmit Frame Synchronization WK enable bit. 0x0: Transmit Frame Synchronization WK enable is NOT active 0x1: Transmit Frame Synchronization WK enable is active	RW	0
7	XSYNCERREN	Transmit Frame Synchronization Error WK enable bit. 0x0: Transmit Frame Synchronization Error WK enable is NOT active 0x1: Transmit Frame Synchronization Error WK enable is active	RW	0
6:4	RESERVED	Reserved	R	0x0
3	RRDYEN	Receive Buffer Threshold wakeup enable bit. 0x0: Receive Buffer Threshold WK enable is NOT active 0x1: Receive Buffer Threshold WK enable is active	RW	0
2	REOFEN	Receive End Of Frame WK enable bit. 0x0: Receive End Of Frame WK enable is NOT active 0x1: Receive End Of Frame WK enable is active	RW	0
1	RFSREN	Receive Frame Synchronization WK enable bit. 0x0: Receive Frame Synchronization WK enable is NOT active 0x1: Receive Frame Synchronization WK enable is active	RW	0
0	RSYNCERREN	Receive Frame Synchronization Error WK enable bit. 0x0: Receive Frame Synchronization Error WK enable is NOT active 0x1: Receive Frame Synchronization Error WK enable is active	RW	0

Table 23-445. Register Call Summary for Register MCBSPLP_WAKEUPEN_REG

Multichannel Buffered Serial Port (McBSP)

- Wake-Up Capability: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9]
- MCBSP Register Summary: [10] [11] [12] [13]

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Table 23-446. MCBSPLP_XCCR_REG

Address Offset	0x0000 00AC		
Physical Address	0x4902 20AC 0x4012 20AC 0x2 20AC 0x4902 40AC 0x4012 40AC 0x2 40AC 0x4902 60AC 0x4012 60AC 0x2 60AC	**Instance**	MCBSP1_L3 MCBSP1_CORTEX-A9 MCBSP1_DSP MCBSP2_L3 MCBSP2_CORTEX-A9 MCBSP2_DSP MCBSP3_L3 MCBSP3_CORTEX-A9 MCBSP3_DSP
Description	McBSPLP transmit configuration control register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																EXTCLKGATE	PPCONNECT	DXENDLY		XFULL_CYCLE	RESERVED			DLB	RESERVED	XDMAEN	RESERVED				XDISABLE

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x0000
15	EXTCLKGATE	External clock gating enable (CLKX and FSX master only). When this bit is set and the transmit clock and FSX are set as output, the CLKX is enabled when FSX is active plus 3 clock cycles after (clock is provided for FWID + 4 clock cycles, assuming that the FSX width, active, is FWID + 1 clock cycles); outside this window the external transmit clock is gated. The receive use the same gated transmit clock and transmit frame synchronization signals regardless of the CLKRM/FSRM settings. When using this mode the frame synchronization signal must be active during reception of the entire frame (FWID must be programmed accordingly) to ensure the proper receive process, which requires at least 3 cycles after the frame complete to transfer the data into the receive buffer. 0x0: External clock gating disabled. 0x1: External clock gating enable.	RW	0
14	PPCONNECT	Pair to pair connection. When set the DXENO pin is always set to 0 regardless of the frame boundary, setting the tree state buffer as output 0x0: Pair to pair connection. When set the DXENO pin is always set to 0 regardless of the frame boundary, setting the tree state buffer as output 0x1: Pair to pair connection. When set the DXENO pin is always set to 0 regardless of the frame boundary, setting the tree state buffer as output	RW	0
13:12	DXENDLY	When DXENA bit in SPCR1 is set to 1 this field selects the added delay as follow: 0x0: 80 ps 0x1: 160 ps (default) 0x2: 240 ps 0x3: 320 ps	RW	0x1

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Bits	Field Name	Description	Type	Reset
11	XFULL_CYCLE	Transmit full-cycle mode select. 0x0: McBSPLP operates in transmit half-cycle mode (transmit frame synchronization is sampled by the opposite edge of the clock used to drive transmit data). 0x1: McBSPLP operates in transmit full-cycle mode (transmit frame synchronization is sampled by the same edge of the clock used to drive transmit data).	RW	0
10:6	RESERVED	Reserved	R	0x00
5	DLB	Digital Loop-Back 0x0: No DLB 0x1: DLB	RW	0
4	RESERVED	Reserved	R	0
3	XDMAEN	Transmit DMA Enable bit. When set to 0 this bit will gate the external transmit DMA request, without resetting the DMA state machine. It is recommended to change this bit value only during transmit reset. 0x0: When set to 0 this bit will gate the external transmit DMA request, 0x1: When set to 1 this bit will NOT gate the external transmit DMA request,	RW	1
2:1	RESERVED	Reserved	R	0
0	XDISABLE	Transmit Disable bit. When this bit is set the transmit process will stop at the next frame boundary. 0x0: The transmit process will NOT stop at the next frame boundary. 0x1: The transmit process will stop at the next frame boundary.	RW	0

Table 23-447. Register Call Summary for Register MCBSPLP_XCCR_REG

Multichannel Buffered Serial Port (McBSP)

- McBSP DMA Requests: [0]
- Clocking and Framing Data: [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18]
- Enable/Disable the Transmit and Receive Processes: [19] [20] [21]
- MCBSP Data Transfer Mode: [22] [23]
- Clock Generation in the SRG: [24]
- McBSP DMA Configuration: [25]
- McBSP Basic Programming Model: [26]
- McBSP Initialization Procedure: [27]
- Programming the McBSP Registers for the Desired Receiver Configuration (Step 2): [28]
- Programming the McBSP Registers for the Desired Transmitter Operation (Step 2): [29] [30] [31]
- MCBSP Register Summary: [32] [33] [34] [35]

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Table 23-448. MCBSPLP_RCCR_REG

Address Offset	0x0000 00B0		
Physical Address	0x4902 20B0 0x4012 20B0 0x2 20B0 0x4902 40B0 0x4012 40B0 0x2 40B0 0x4902 60B0 0x4012 60B0 0x2 60B0	**Instance**	MCBSP1_L3 MCBSP1_CORTEX-A9 MCBSP1_DSP MCBSP2_L3 MCBSP2_CORTEX-A9 MCBSP2_DSP MCBSP3_L3 MCBSP3_CORTEX-A9 MCBSP3_DSP
Description	McBSPLP receive configuration control register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				RFULL_CYCLE	RESERVED							RDMAEN	RESERVED		RDISABLE

Bits	Field Name	Description	Type	Reset
31:12	RESERVED	Reserved	R	0x00000
11	RFULL_CYCLE	Receive full-cycle mode select. 0x0: McBSPLP operates in receive half-cycle mode (receive frame synchronization is sampled by the opposite edge of the clock used to sample receive data). 0x1: McBSPLP operates in receive full-cycle mode (receive frame synchronization is sampled by the same edge of the clock used to sample receive data).	RW	1
10:4	RESERVED	Reserved	R	0x00
3	RDMAEN	Receive DMA Enable bit. When set to 0 this bit will gate the external transmit DMA request, without resetting the DMA state machine. It is recommended to change this bit value only during receive reset. 0x0: When set to 0 this bit will gate the external transmit DMA request 0x1: When set to 1 this bit will NOT gate the external transmit DMA request	RW	1
2:1	RESERVED	Reserved	R	0
0	RDISABLE	Receive Disable bit. When this bit is set the receive process will stop at the next frame boundary. 0x0: the receive process will NOT stop at the next frame boundary. 0x1: When this bit is set the receive process will stop at the next frame boundary.	RW	0

Table 23-449. Register Call Summary for Register MCBSPLP_RCCR_REG

Multichannel Buffered Serial Port (McBSP)

- McBSP DMA Requests: [0]
- Enable/Disable the Transmit and Receive Processes: [1] [2]
- MCBSP Data Transfer Mode: [3] [4]
- McBSP DMA Configuration: [5]
- McBSP Basic Programming Model: [6]
- MCBSP Register Summary: [7] [8] [9] [10]

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Table 23-450. MCBSPLP_XBUFFSTAT_REG

Address Offset	0x0000 00B4		
Physical Address	0x4902 20B4 0x4012 20B4 0x2 20B4 0x4902 40B4 0x4012 40B4 0x2 40B4 0x4902 60B4 0x4012 60B4 0x2 60B4	**Instance**	MCBSP1_L3 MCBSP1_CORTEX-A9 MCBSP1_DSP MCBSP2_L3 MCBSP2_CORTEX-A9 MCBSP2_DSP MCBSP3_L3 MCBSP3_CORTEX-A9 MCBSP3_DSP
Description	McBSPLP transmit buffer status		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								XBUFFSTAT							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Reserved	R	0x0
7:0	XBUFFSTAT	Transmit Buffer Status (indicates the number of free locations inside transmit buffer). The XBUFFSTAT value reflects the buffer status on the interface clock domain and it can be smaller than the number of free locations which are seen by the transmit state machine.	R	0x80

Table 23-451. Register Call Summary for Register MCBSPLP_XBUFFSTAT_REG

Multichannel Buffered Serial Port (McBSP)

- Enable/Disable the Transmit and Receive Processes: [0]
- McBSP DMA Configuration: [1]
- MCBSP Register Summary: [2] [3] [4] [5]

Table 23-452. MCBSPLP_RBUFFSTAT_REG

Address Offset	0x0000 00B8		
Physical Address	0x4902 20B8 0x4012 20B8 0x2 20B8 0x4902 40B8 0x4012 40B8 0x2 40B8 0x4902 60B8 0x4012 60B8 0x2 60B8	**Instance**	MCBSP1_L3 MCBSP1_CORTEX-A9 MCBSP1_DSP MCBSP2_L3 MCBSP2_CORTEX-A9 MCBSP2_DSP MCBSP3_L3 MCBSP3_CORTEX-A9 MCBSP3_DSP
Description	McBSPLP receive buffer status		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RBUFFSTAT							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Reserved	R	0x0
7:0	RBUFFSTAT	Receive Buffer Status (indicates the number of occupied locations inside receive buffer). The RBUFFSTAT value reflects the buffer status on the interface clock domain and it can be smaller than the real number of the occupied locations which are seen by the receive state machine.	R	0x00

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Table 23-453. Register Call Summary for Register MCBSPLP_RBUFFSTAT_REG

Multichannel Buffered Serial Port (McBSP)

- Enable/Disable the Transmit and Receive Processes: [0]
- McBSP DMA Configuration: [1]
- MCBSP Register Summary: [2] [3] [4] [5]

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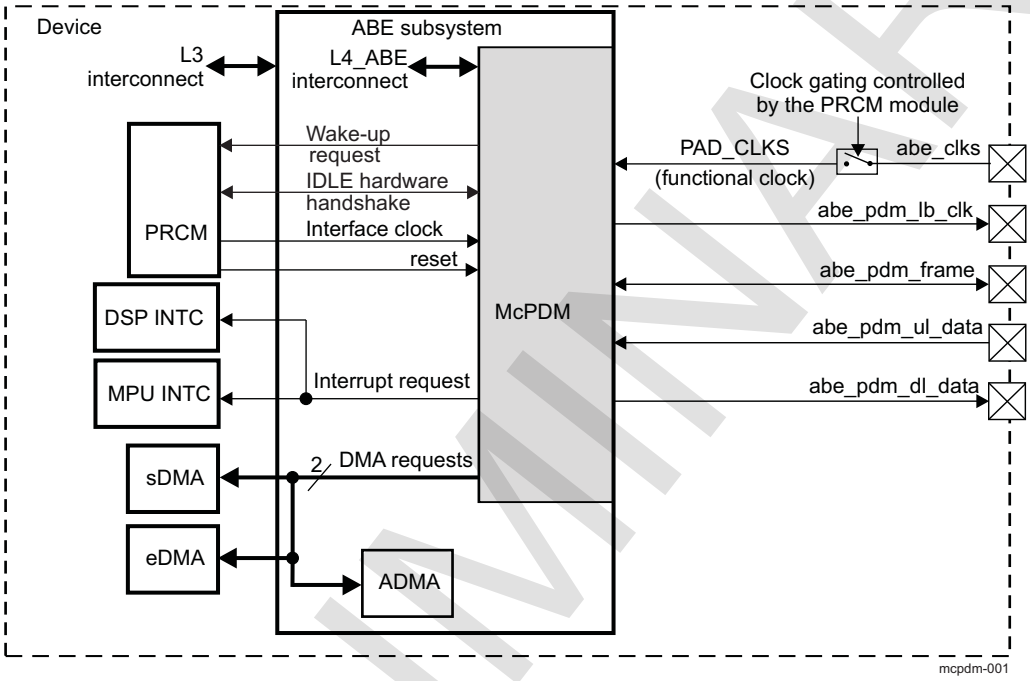
23.6 Multichannel PDM Controller

23.6.1 McPDM Overview

The multichannel pulse density modulation (McPDM) module consists in a proprietary audio module dedicated to mobile phone terminals. It is composed of audio uplink and downlink paths communicating with an external audio companion chip through a dedicated interface.

Figure 23-161 is an overview of the McPDM module.

Figure 23-161. McPDM Overview



The McPDM module can support the following features:

- Full-duplex communication:
  - Five audio downlink channels with up to 3.84 Mbps each
  - Three audio uplink channels with up to 3.84 Mbps each
  - One command channel with up to 3.84 Mbps
  - One status channel with up to 3.84 Mbps
- Uplink and downlink FIFO operations:
  - 16 × 96-bit words for FIFO uplink, where a 96-bit word contains three 24-bit words for the audio uplink channels (one 24-bit word per audio uplink channel) and one 16-bit word for status information
  - 16 × 144-bit words for FIFO downlink, where a 144-bit word contains five 24-bit words for the audio downlink channels (one 24-bit word per audio downlink channel) and one 16-bit word for the command data.
- Interrupt request to MPU and DSP subsystems
- DMA requests with programmable FIFO thresholds:
  - One DMA request for downlink path
  - One DMA request for uplink path
- Upsampling and pulse-density modulators for each audio downlink channel (five channels)
- Offset cancellation feature for audio downlink channels 1 and 2
- Decimation filter and downsampling for each audio uplink channel (three channels)

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- IDLE state hardware handshake
- Wake-up request

23.6.2 McPDM Environment

This section describes the McPDM application fields from an environment point of view (external connections). It describes McPDM connectivity options, lists all possible interfaces, and describes the protocol and data format used in each case.

23.6.2.1 McPDM Modes

Table 23-454 describes the modes and application fields of the McPDM module.

Table 23-454. Modes

Mode	Description
Normal mode	Up to five audio channels are transmitted to, and up to three audio channels are received from, the audio companion chip.
Command mode	In addition to the audio channels, commands are transmitted to the audio companion chip.
Status mode	In addition to the audio channels, status information is received from the audio companion chip.

23.6.2.2 McPDM Signals

Table 23-455 describes the McPDM module signals and specifies their links to modes.

Table 23-455. I/O

Signal	I/O (1)	Description	Reset Value	Normal Mode	Command Mode	Status Mode
abe_clks	I	Clock received from the audio companion chip. The clock frequency is: • 17.64 MHz for a sampling frequency of 88.2/176.4 kHz • 19.2 MHz for a sampling frequency of 96/192 kHz	–	x	x	x
abe_pdm_lb_clk	O	Clock loopback to the audio companion chip from the abe_clks clock signal. The frequency is the same as abe_clks frequency. (2)	0	x	x	x
abe_pdm_frame	I/O	Frame synchronization and command/status data	0	x	x	x
abe_pdm_ul_data	I	Audio uplink path data	–	x	x	x
abe_pdm_dl_data	O	Audio downlink path data	0	x	x	x

(1) I = Input; O = Output

(2) This output signal is also used as retiming input (the INPUTENABLE bit in the corresponding pad configuration register must be set to 1).

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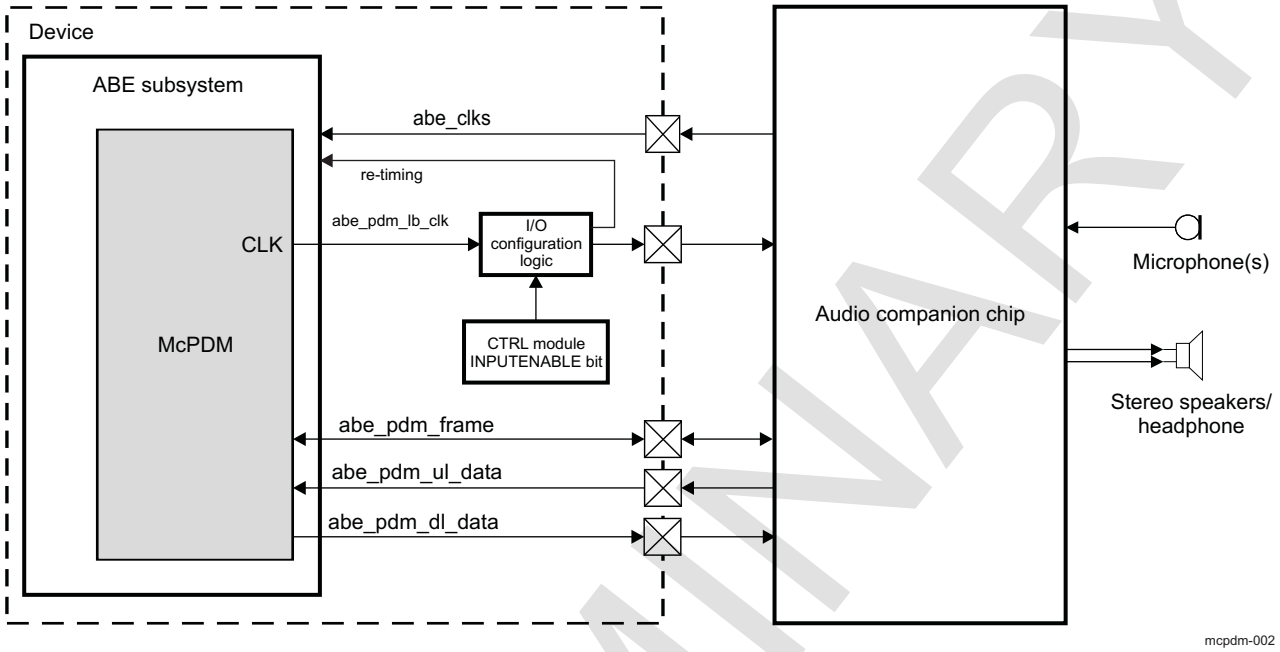
23.6.2.3 McPDM Configurations

Figure 23-162 shows the McPDM generic configuration.

Figure 23-162. McPDM Generic Configuration



23.6.2.4 Protocols and Data Formats

23.6.2.4.1 Protocols and Data Formats in Normal Mode

This section describes data transfer on the interface in normal mode. In this mode, the abe_pdm_frame signal is used only for frame synchronization purposes. Figure 23-163 shows the protocols and data formats in normal mode for two examples:

(a) With two downlink and three uplink channels enabled

(b) With five downlink and three uplink channels enabled

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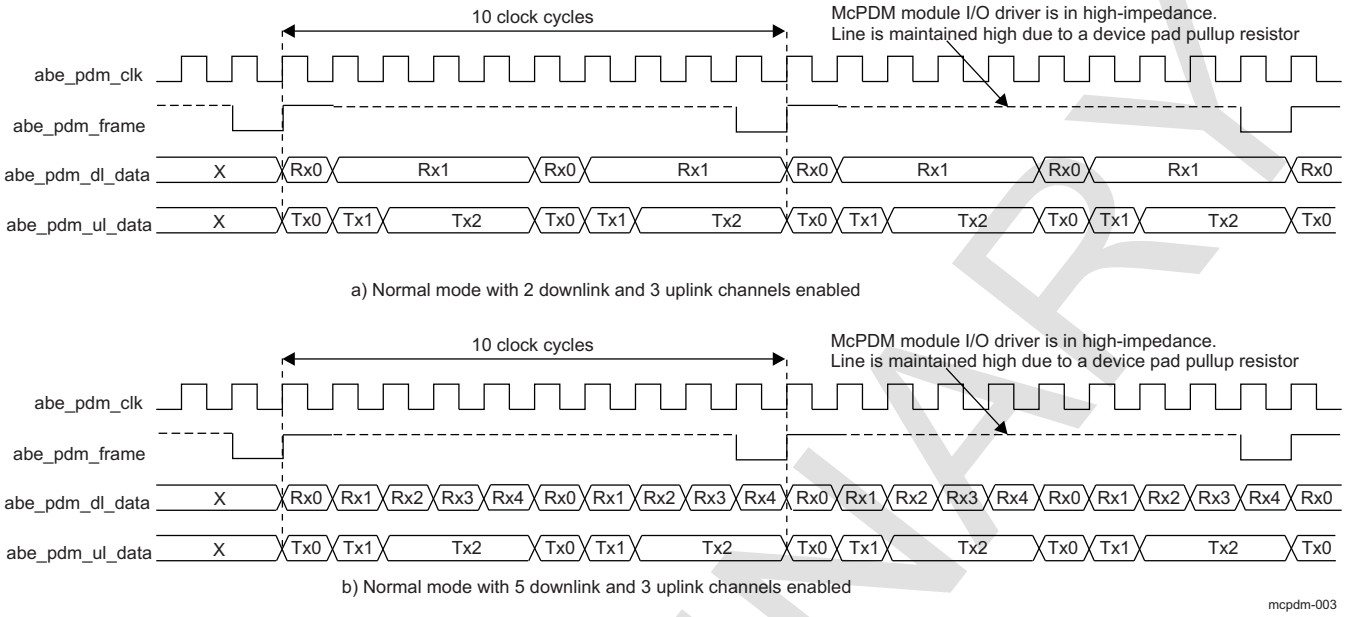
Figure 23-163. Protocols and Data Formats in Normal Mode



In normal mode, the frequency ratio between the abe_pdm_frame and abe_pdm_lb_clk signals is 10. This ratio is static and the abe_pdm_frame signal low-pulse width is one clock period longer than the abe_pdm_lb_clk signal.

The abe_pdm_frame signal is driven by the McPDM module in the device to the external audio companion chip. The McPDM module drives the abe_pdm_frame signal low during one clock period of the abe_pdm_lb_clk signal, then it drives it high during one clock period of the abe_pdm_lb_clk signal before releasing the abe_pdm_frame I/O driver in high-impedance state. The McPDM module pad internal pullup resistor allows keeping a high-level state on the abe_pdm_frame line when the abe_pdm_frame I/O driver is in high-impedance state.

A maximum of two samples × five downlink channels (10 samples) can be transmitted by the McPDM module to the external audio companion chip during a frame period.

A maximum of two samples × three uplink channels (six samples) can be received by the McPDM module from the external audio companion chip during a frame period.

Each downlink and uplink channel can be independently enabled or disabled by setting to 1 or clearing to 0 the corresponding bit in the MCPDM_CTRL register.

23.6.2.4.2 Protocols and Data Formats in Command Mode

This section describes data transfer on the interface in command mode. In this mode, the abe_pdm_frame signal is used to transmit command words to the external audio companion chip. It allows configuring audio registers in the external audio companion chip (that is, amplifier gains) without using the legacy I^2C interface, which may be busy and add latency to gain correction.

NOTE: In command mode, uplink channel samples are transmitted to and downlink channel samples are received from the external audio companion chip as in normal mode.

Figure 23-164 shows the protocols and data formats in command mode.

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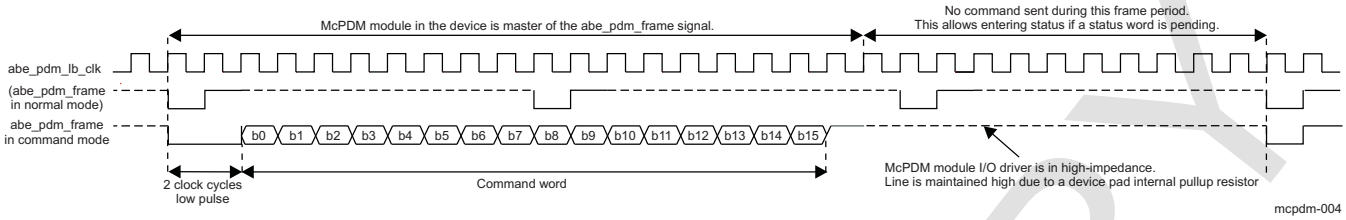
Figure 23-164. Protocols and Data Formats in Command Mode



23.6.2.4.2.1 Entering Command Mode

Command mode can be entered when command data are pending and no status mode is ongoing or detected.

If both of these conditions are met and the MCPDM_CTRL[9] CMD_INT bit is set to 1, the McPDM module automatically enters command mode.

To enter command mode, the McPDM module must drive the abe_pdm_frame signal low during two periods of the abe_pdm_lb_clk clock signal.

The external audio companion chip detects a command mode request from the McPDM module when a low state is detected during two periods of the abe_pdm_lb_clk clock signal. Once a command mode request is detected, the external audio companion chip enters command mode. In this mode, the status mode cannot be entered during at least four frame cycles.

If a status mode is detected or ongoing while a command is ready to be sent, the command data are stored in an internal register.

If one or more command data are written before the previous one is sent, the previous one is overwritten with the new one and only the last stored 16-bit command data are sent.

If new command data are available while the system is already in command mode, the current command completes normally and exits before re-entering command mode and transmitting the new command data a frame period later.

23.6.2.4.2.2 Command Data Transmission

The 16-bit command data are transmitted directly after the abe_pdm_frame signal is driven low during two periods of the abe_pdm_lb_clk clock signal.

When the MCPDM_CTRL[9] CMD_INT bit is set to 1, 16-bit command data must be written to the MCPDM_DN_DATA register. Only the 16 lower bits are significant. When no command must be transmitted on the abe_pdm_frame line, a null word (0x00000000) must be written as the command data.

When the MCPDM_CTRL[9] CMD_INT bit is cleared to 0, no 16-bit command data has to be written to the MCPDM_DN_DATA register.

23.6.2.4.2.3 Exiting Command Mode

After the 16-bit command data is sent, the McPDM module drives the abe_pdm_frame signal high during one period of the abe_pdm_lb_clk clock signal before releasing the abe_pdm_frame I/O driver in high-impedance state. The McPDM module pad internal pullup resistor allows keeping a high-level state on the abe_pdm_frame line when the abe_pdm_frame I/O driver is in high-impedance state.

The McPDM module exits automatically from command mode one period of the abe_pdm_lb_clk clock signal after the last bit of the command data has been transmitted on the abe_pdm_frame line.

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NOTE: Due to this protocol mechanism, frame synchronization is lost (replaced by the ninth bit of the command data) during one frame period. The external audio companion chip must internally emulate a frame synchronization to send uplink channel samples and received downlink channel samples as in normal mode while receiving command data on the abe_pdm_frame line.

23.6.2.4.2.4 Multiple Command Data Access

As shown in Figure 23-164, two consecutive command data can be sent every three frames. If no status mode is entered after a command data has been sent, the next command data is sent three frames after starting to send the current command data.

23.6.2.4.3 Protocols and Data Formats in Status Mode

This section describes data transfer on the interface in status mode. In this mode, the abe_pdm_frame signal is used to receive status information from the external audio companion chip.

NOTE: In status mode, uplink channel samples are transmitted to and downlink channel samples are received from the external audio companion chip as in normal mode.

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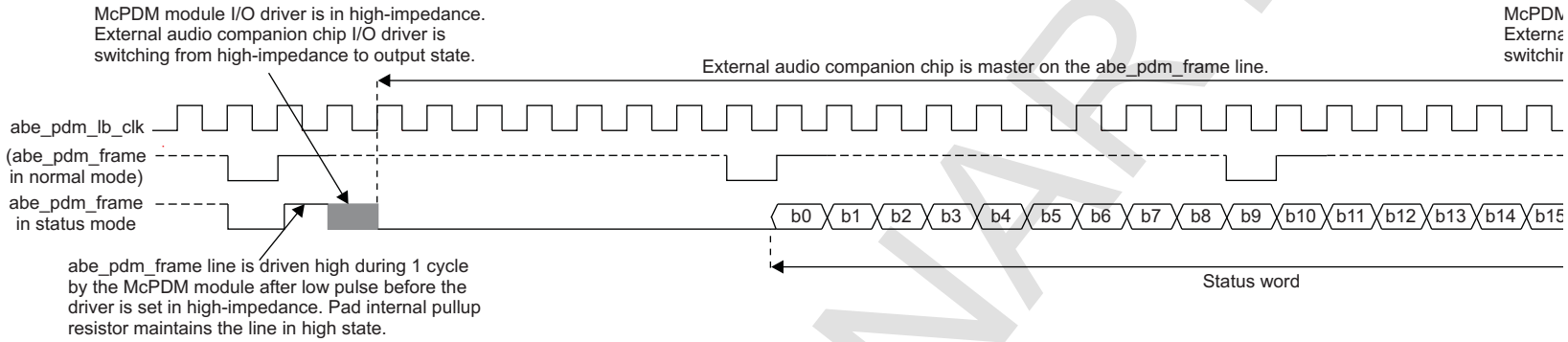
Figure 23-165 shows the protocols and data formats in status mode.

Figure 23-165. Protocols and Data Formats in Status Mode



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23.6.2.4.3.1 Entering Status Mode

Status mode can be entered when no command mode is detected during the last frame low pulse and no command mode is ongoing.

If both of these conditions are met and the MCPDM_CTRL[10] STATUS_INT bit is set to 1, the McPDM module automatically enters status mode when the command mode is complete.

In status mode, the status information data are sent by the external audio companion chip to the McPDM module. The status information is stored in an internal register.

If one or more status information packages are received before the previous status information is read, the status information stored in the internal register is overwritten with the new one.

In status mode, the external audio companion chip drives the abe_pdm_frame line low until the next frame synchronization low pulse. Then, it sends the 16-bit status information data on the abe_pdm_frame line. During the transmission of the status information, the McPDM module does not generate any frame-sync low pulse on the abe_pdm_frame line for one frame period.

23.6.2.4.3.2 Status Information Data Reception

The 16-bit status information data are received directly after the second frame-sync low pulse on the abe_pdm_frame line.

When the MCPDM_CTRL[10] STATUS_INT bit is set to 1, 16 bits of status information data must be read from the MCPDM_UP_DATA register. Only the 16 lower bits are significant. When the value of the status information is a null word (0x00000000), it means that no status information has been sent by the external audio companion chip.

When the MCPDM_CTRL[10] STATUS_INT bit is cleared to 0, no status information data has to be read from the MCPDM_UP_DATA register.

23.6.2.4.3.3 Exiting Status Mode

After the 16-bit status information data is sent, the external audio companion chip drives the abe_pdm_frame line high during one period of the abe_pdm_lb_clk clock signal before releasing its I/O driver in high-impedance state.

The McPDM module automatically exits the status mode one period of the abe_pdm_lb_clk clock signal after the last bit of the status information data has been transmitted on the abe_pdm_frame line. After exiting status mode, the McPDM module generates frame-sync low pulses.

NOTE: Due to the protocol mechanism, frame synchronization is lost during three frame periods. The external audio companion chip must internally emulate a frame synchronization to send uplink channel samples and received downlink channel samples as in normal mode while transmitting status information data on the abe_pdm_frame line.

23.6.2.4.3.4 Multiple Status Information Data Access

Multiple status information data can be sent by the external audio companion chip to the McPDM module every four frames.

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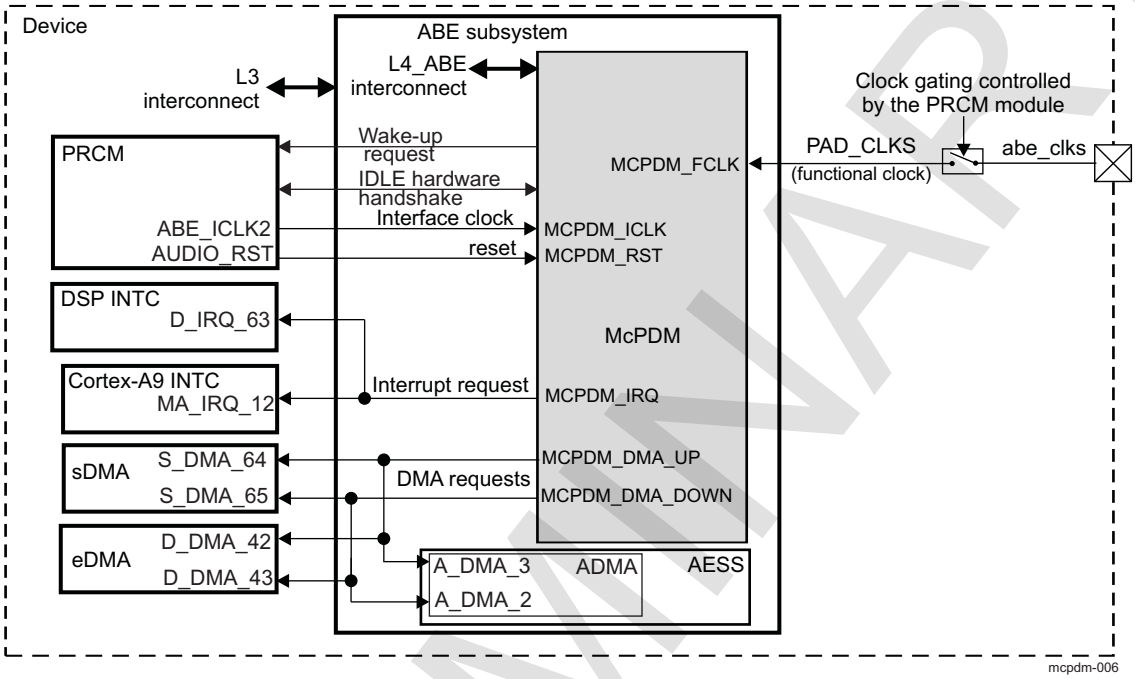
23.6.3 McPDM Integration

This section describes the McPDM module integration in the device, including information about clocks, resets, and hardware requests.

Figure 23-166 shows the McPDM integration.

Figure 23-166. McPDM Integration



NOTE: For more information about the IDLE hardware handshake and the wake-up request, see Section 3.1.1.1.2, *Module-Level Clock Management*, in Chapter 3, *Power, Reset, and Clock Management*.

Table 23-456 through Table 23-458 summarize the integration of the module in the device.

Table 23-456. Integration Attributes

Module Instance	Attributes		
	Power Domain	Wake-Up Capability	Interconnect
McPDM	PD_AUDIO	Yes	L4_ABE

Table 23-457. Clocks and Resets

Clocks				
Module Instance	Destination Signal Name	Source Signal Name	Source	Description
McPDM	MCPDM_ICLK	ABE_ICLK2	PRCM module	McPDM interface clock
	MCPDM_FCLK	PAD_CLKS	PRCM module	Common external functional clock
Resets				
McPDM	MCPDM_RST	AUDIO_RST	PRCM module	McPDM hardware reset

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Table 23-458. Hardware Requests

Module Instance	Source Signal Name	Destination Signal Name	Destination	Description
Interrupt Requests				
McPDM	MCPDM_IRQ	D_IRQ_63	DSP	McPDM interrupt request to the DSP INTC
	MCPDM_IRQ	MA_IRQ_112	Cortex-A9	McPDM interrupt request to the Cortex-A9 MPU INTC
DMA Requests				
McPDM	MCPDM_DMA_UP	S_DMA_64	sDMA	McPDM uplink path DMA request to the sDMA
	MCPDM_DMA_DOWN	S_DMA_65	sDMA	McPDM downlink path DMA request to the sDMA
	MCPDM_DMA_UP	D_DMA_42	dDMA	McPDM uplink path DMA request to the eDMA
	MCPDM_DMA_DOWN	D_DMA_43	dDMA	McPDM downlink path DMA request to the eDMA
	MCPDM_DMA_UP	A_DMA_3	aDMA	McPDM uplink path DMA request to the aDMA
	MCPDM_DMA_DOWN	A_DMA_2	aDMA	McPDM downlink path DMA request to the aDMA

NOTE:

- For the description of the interrupt source, see Section 23.6.4.5, *Interrupt Requests*.
- For the description of the DMA source, see Section 23.6.4.6, *DMA Requests*.

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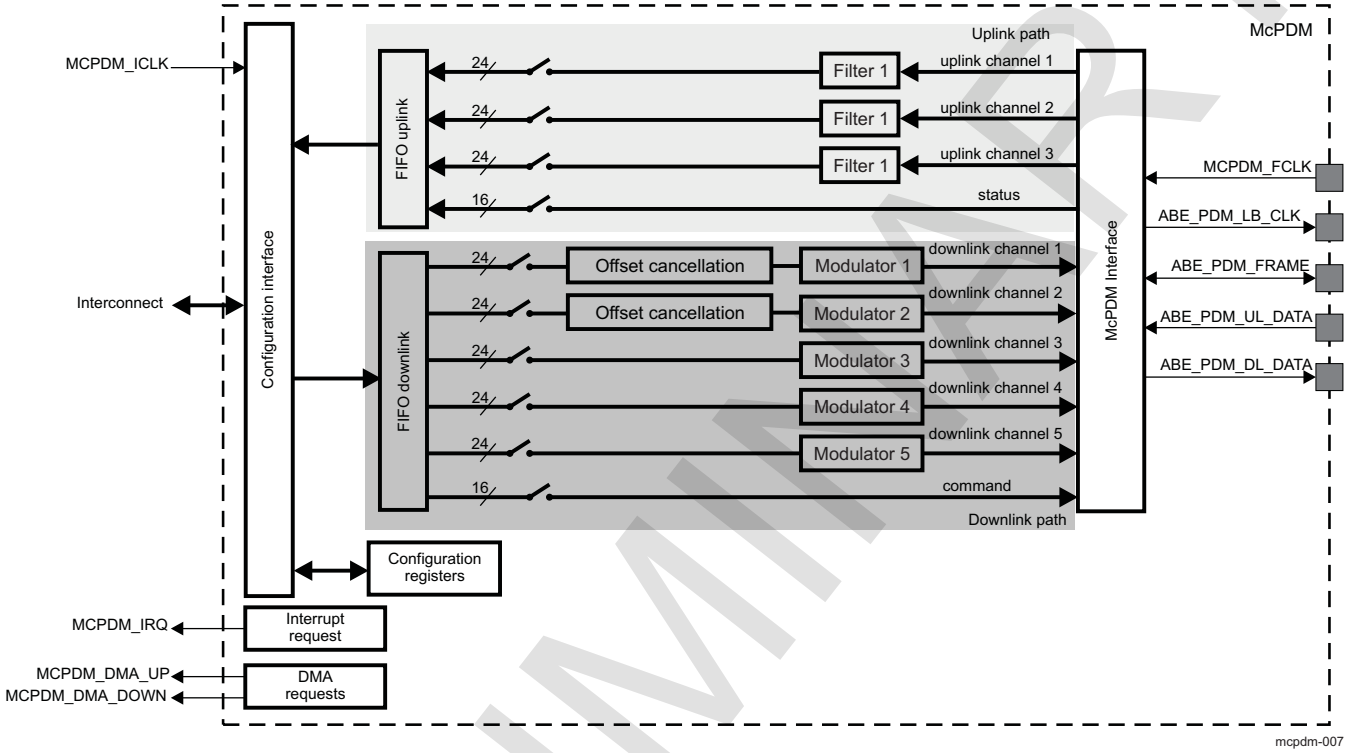
23.6.4 McPDM Functional Description

23.6.4.1 McPDM Block Diagram

Figure 23-167 shows the McPDM block diagram.

Figure 23-167. McPDM Block Diagram



23.6.4.2 McPDM Clock Configuration

The functional clock MCPDM_FCLK is provided by the external audio companion chip. Its frequency can be either 17.64 MHz for a sampling frequency of 88.2/176.4 kHz, or 19.2 MHz for a sampling frequency of 96/192 kHz.

The functional clock is also looped-back to the audio companion chip through ABE_PDM_LB_CLK for resynchronization purposes.

23.6.4.3 McPDM Software Reset

To perform a software reset of the McPDM module, the MCPDM_SYSCONFIG[0] SOFTRESET bit must be set to 1. Reading the MCPDM_SYSCONFIG[0] SOFTRESET bit gives the status of the software reset:

- Read 1: The software reset is ongoing.
- Read 0: The software reset is complete.

Software must ensure that the software reset completes before doing McPDM operations. Moreover, uplink and downlink paths can be independently software reset by setting the MCPDM_CTRL[11] SW_UP_RST bit for the uplink path, and the MCPDM_CTRL[12] SW_DN_RST bit for the downlink path to 1. The software reset is stopped by clearing the MCPDM_CTRL[11] SW_UP_RST bit for the uplink path, and the MCPDM_CTRL[12] SW_DN_RST bit for the downlink path to 0.

The software reset of the McPDM module, after completion, puts all McPDM registers in their default state. The downlink/uplink reset, resets only the downlink/uplink hardware logic (no registers are affected).

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23.6.4.4 McPDM Power Management

Table 23-459 describes the power-management features available to the McPDM module.

Table 23-459. Local Power-Management Features

Feature	Registers	Description
Clock autogating	N/A	Feature not available
Slave idle modes	MCPDM_SYSCONFIG[3:2] IDLEMODE bit field	Force-idle, no-idle, smart-idle, and smart-idle wake-up capable modes are available for the interface clock
Clock activity	N/A	Feature not available
Master standby modes	N/A	Feature not available
Global wake-up enable	N/A	Feature not available
Wake-up sources enable	MCPDM_IRQWAKEEN and MCPDM_DMAWAKEEN registers	Each register holds one active-high enable bit per event source able to generate wake-up signal
Audio channel enable	MCPDM_CTRL[0] PDM_UP1_EN to MCPDM_CTRL[2] PDM_UP3_EN bits for audio uplink channels MCPDM_CTRL[3] PDM_DN1_EN to MCPDM_CTRL[7] PDM_DN5_EN bits for audio downlink channels	Each of these bits allows enabling (set to 1) or disabling (clear to 0) the corresponding audio channel.
Status channel enable	MCPDM_CTRL[10] STATUS_INT bit for the status channel	This bit allows enabling (set to 1) or disabling (clear to 0) the status channel
Command channel enable	MCPDM_CTRL[9] CMD_INT bit for the command channel	This bit allows enabling (set to 1) or disabling (clear to 0) the command channel

The MCPDM_ICLK interface clock is controlled though the PRCM module by using IDLE request and acknowledge signals. The MCPDM_SYSCONFIG[3:2] IDLEMODE bit field allows controlling the interface clock gating in idle mode.

For the uplink path, the interface clock can be put in idle after the uplink path is enabled. Wakeup is available according to the settings of the MCPDM_IRQWAKEEN and MCPDM_DMAWAKEEN registers and the FIFO uplink threshold configured in the MCPDM_FIFO_CTRL_UP[3:0] UP_TRESH bit field. The wake-up signal is asserted when the FIFO uplink level is equal to or greater than the FIFO uplink threshold value.

For the downlink path, the interface clock can be put in idle after the FIFO downlink level reaches the FIFO downlink threshold at least once. Wakeup is available according to the settings of the MCPDM_IRQWAKEEN and MCPDM_DMAWAKEEN registers and the FIFO downlink threshold configured in the MCPDM_FIFO_CTRL_DN[3:0] DN_TRESH bit field. The wake-up signal is asserted when the FIFO downlink level is below the FIFO downlink threshold value.

23.6.4.5 McPDM Interrupt Requests

The McPDM can generate interrupt requests to the Cortex-A9 MPU and DSP INTCs through the MCPDM_IRQ signal.

Table 23-460 lists the nonmaskable and maskable event flags and their mask that can cause the McPDM module to generate interrupts.

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Table 23-460. Interrupt Events

Nonmaskable Event Flag [(1)]	Maskable Event Flag	Event Mask Bit	Event Unmask Bit	Description
MCPDM_IRQSTATUS_RAW[11] UP_IRQ_FULL	MCPDM_IRQSTATUS[11] UP_IRQ_FULL	MCPDM_IRQENABLE_CLR[11] UP_IRQ_FULL_MASK	MCPDM_IRQENABLE_SET[11] UP_IRQ_FULL_MASK	FIFO-uplink-full event. This event occurs when FIFO uplink is already full and a new word is written to the FIFO uplink by the uplink part of the McPDM module.
MCPDM_IRQSTATUS_RAW[10] UP_IRQ_ALST_FULL	MCPDM_IRQSTATUS[10] UP_IRQ_ALST_FULL	MCPDM_IRQENABLE_CLR[10] UP_IRQ_ALST_FULL_MASK	MCPDM_IRQENABLE_SET[10] UP_IRQ_ALST_FULL_MASK	FIFO-uplink-almost-full event. This event occurs when FIFO uplink contains (FIFO uplink size – 1) words and a new word is written to the FIFO uplink by the uplink part of the McPDM module.
MCPDM_IRQSTATUS_RAW[9] UP_IRQ_EMPTY	MCPDM_IRQSTATUS[9] UP_IRQ_EMPTY	MCPDM_IRQENABLE_CLR[9] UP_IRQ_EMPTY_MASK	MCPDM_IRQENABLE_SET[9] UP_IRQ_EMPTY_MASK	FIFO-uplink-empty event. This event occurs when FIFO uplink is already empty and a new word is read from the FIFO uplink by software.
MCPDM_IRQSTATUS_RAW[8] UP_IRQ	MCPDM_IRQSTATUS[8] UP_IRQ	MCPDM_IRQENABLE_CLR[8] UP_IRQ_MASK	MCPDM_IRQENABLE_SET[8] UP_IRQ_MASK	FIFO-uplink-read-request event. This event occurs when the number of words stored in the FIFO uplink is equal to or greater than the FIFO uplink threshold.
MCPDM_IRQSTATUS_RAW[3] DN_IRQ_FULL	MCPDM_IRQSTATUS[3] DN_IRQ_FULL	MCPDM_IRQENABLE_CLR[3] DN_IRQ_FULL_MASK	MCPDM_IRQENABLE_SET[3] DN_IRQ_FULL_MASK	FIFO-downlink-full event. This event occurs when FIFO downlink is already full and a new word is written to the FIFO downlink by software.
MCPDM_IRQSTATUS_RAW[2] DN_IRQ_ALST_EMPTY	MCPDM_IRQSTATUS[2] DN_IRQ_ALST_EMPTY	MCPDM_IRQENABLE_CLR[2] DN_IRQ_ALST_EMPTY_MASK	MCPDM_IRQENABLE_SET[2] DN_IRQ_ALST_EMPTY_MASK	FIFO-downlink-almost-empty event. This event occurs when FIFO downlink contains one word and a new word is read from the FIFO downlink by the downlink part of the McPDM module.
MCPDM_IRQSTATUS_RAW[1] DN_IRQ_EMPTY	MCPDM_IRQSTATUS[1] DN_IRQ_EMPTY	MCPDM_IRQENABLE_CLR[1] DN_IRQ_EMPTY_MASK	MCPDM_IRQENABLE_SET[1] DN_IRQ_EMPTY_MASK	FIFO-downlink-empty event. This event occurs when FIFO downlink is empty and a new word is read from the FIFO downlink by the downlink part of the McPDM module.
MCPDM_IRQSTATUS_RAW[0] DN_IRQ	MCPDM_IRQSTATUS[0] DN_IRQ	MCPDM_IRQENABLE_CLR[0] DN_IRQ_MASK	MCPDM_IRQENABLE_SET[0] DN_IRQ_MASK	FIFO-downlink-write-request event. This event occurs when the number of words stored in the FIFO downlink is less than the FIFO downlink threshold.

(1) The MCPDM_IRQSTATUS_RAW register is mainly used for debug purposes.

CAUTION

Once an event generating the interrupt request has been processed by software, this event must be cleared by writing a logical 1 to the corresponding bit of the MCPDM_IRQSTATUS register.

Writing a logical 1 in a bit of the MCPDM_IRQSTATUS register also clears the corresponding bit in the MCPDM_IRQSTATUS_RAW register to 0.

An event can generate an interrupt request when a logical 1 is written to the corresponding mask bit in the MCPDM_IRQENABLE_SET register. Events are reported in the MCPDM_IRQSTATUS and MCPDM_IRQSTATUS_RAW registers.

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An event stops generating interrupt requests when a logical 1 is written to the corresponding mask bit in the MCPDM_IRQENABLE_CLR register. Events are reported only in the MCPDM_IRQSTATUS_RAW register.

In case of the MCPDM_IRQSTATUS_RAW register, the event is reported in the corresponding bit, even if the interrupt request generation is disabled for this event.

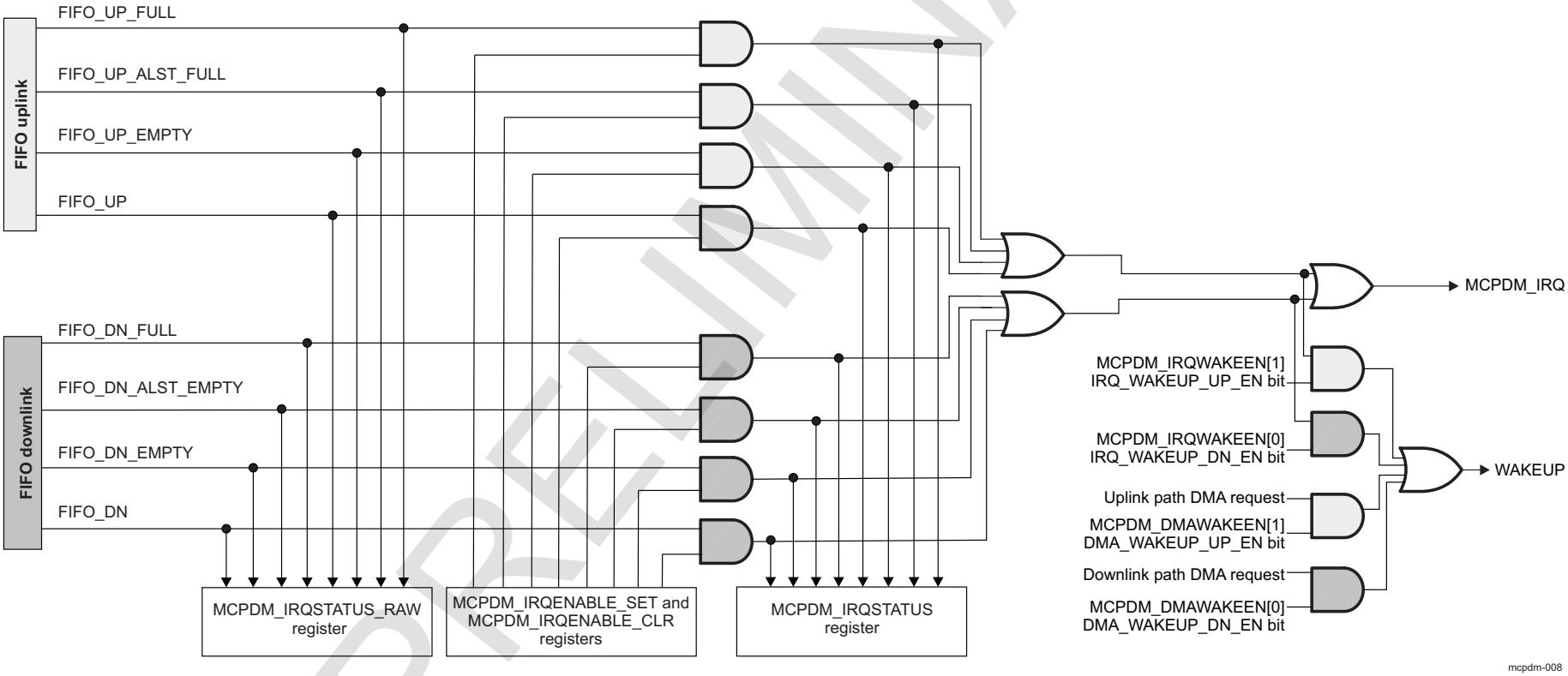
Writing a logical 1 in a bit of the MCPDM_IRQSTATUS_RAW register sets the corresponding bit in the MCPDM_IRQSTATUS register to 1.

The MCPDM_IRQSTATUS_RAW register is used primarily for debug purposes.

For more information about interrupt request signal mapping, see Table 23-458.

Figure 23-168 shows the interrupt tree of the McPDM module.

Figure 23-168. Interrupt Tree



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23.6.4.6 McPDM DMA Requests

The McPDM module can generate two DMA requests to the sDMA, aDMA, and eDMA controllers:

- The uplink path can generate a DMA request through the MCPDM_DMA_UP signal.
- The downlink path can generate a DMA request through the MCPDM_DMA_DOWN signal.

Table 23-461 lists the DMA requests of the McPDM module.

Table 23-461. McPDM DMA Requests

DMA Request Signal	DMA Request Generation Enabling Bit	DMA Request Generation Disabling Bit	Description
MCPDM_DMA_UP	MCPDM_DMAENABLE_SET [1] DMA_UP_ENABLE	MCPDM_DMAENABLE_CLR [1] DMA_UP_ENABLE	Uplink path DMA request. This request is generated when the number of words in the FIFO uplink is equal to or above the FIFO uplink threshold.
MCPDM_DMA_DOWN	MCPDM_DMAENABLE_SET [0] DMA_DN_ENABLE	MCPDM_DMAENABLE_CLR [0] DMA_DN_ENABLE	Downlink path DMA request. This request is generated when the number of words in the FIFO downlink is below the FIFO downlink threshold.

To enable or disable the DMA request generation on the MCPDM_DMA_UP signal, one of the following actions must be performed:

- Write a logical 1 to the MCPDM_DMAENABLE_SET[1] DMA_UP_ENABLE bit to enable the DMA request generation on the MCPDM_DMA_UP signal.
- Write a logical 1 to the MCPDM_DMAENABLE_CLR[1] DMA_UP_ENABLE bit to disable the DMA request generation on the MCPDM_DMA_UP signal.

To enable or disable the DMA request generation on the MCPDM_DMA_DOWN signal, one of the following actions must be performed:

- Write a logical 1 to the MCPDM_DMAENABLE_SET[0] DMA_DN_ENABLE bit to enable the DMA request generation on the MCPDM_DMA_DOWN signal.
- Write a logical 1 to the MCPDM_DMAENABLE_CLR[0] DMA_DN_ENABLE bit to disable the DMA request generation on the MCPDM_DMA_DOWN signal.

For more information about DMA request signals mapping, see Table 23-458.

23.6.4.7 Uplink Path

Figure 23-169 is a detailed block diagram of the uplink path in the McPDM module.

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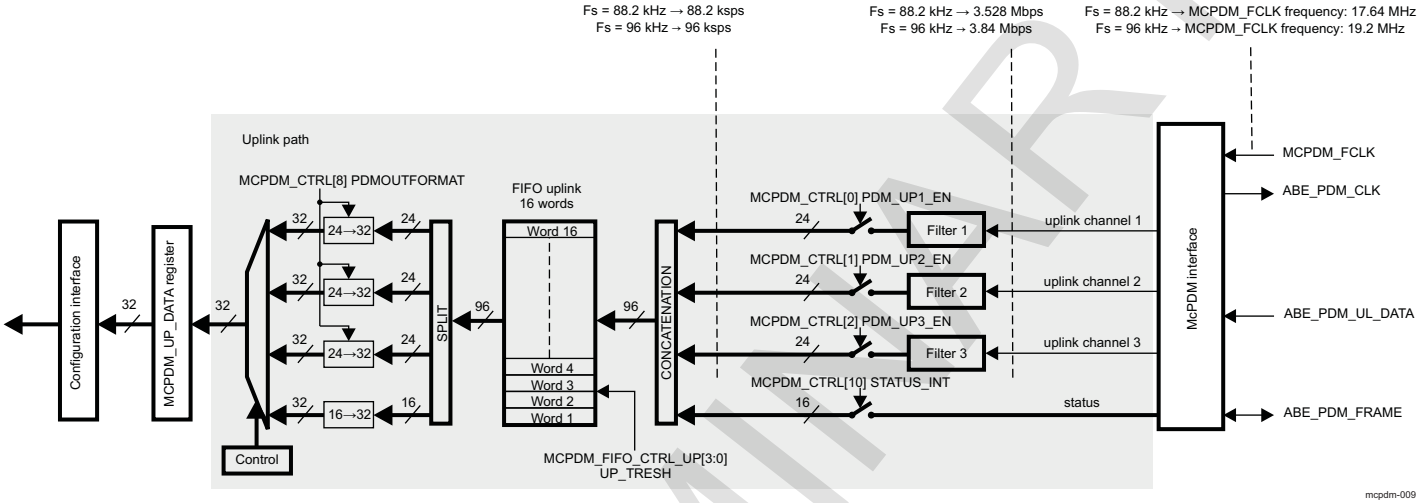
Figure 23-169. Uplink Path Detailed Block Diagram



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23.6.4.7.1 Uplink Path Features

The uplink path has the following features:

- Three audio uplink channels
- One status channel
- Decimation filter for each audio uplink channel
- 16-word FIFO uplink with threshold setting
- Audio channel data formatting
- High-frequency sampling feature

23.6.4.7.2 Uplink Path Description

23.6.4.7.2.1 Uplink Data Received From the External Audio Companion Chip

The McPDM interface receives audio uplink channel data and status information data from the external audio companion chip at a clock rate of 17.64 MHz for a sampling frequency of 88.2 kHz, or 19.2 MHz for a sampling frequency of 96 kHz. This low-frequency sampling feature is enabled by default. The uplink path supports a high-frequency sampling feature to work with an ultrasonic external microphone. This feature is enabled by setting the MCPDM_CTRL[13] DIV_SEL bit to 1. Thus, the McPDM interface receives audio uplink channel data and status information data from the external audio companion chip at a clock rate of 17.64 MHz for a sampling frequency of 176.4 kHz, or 19.2 MHz for a sampling frequency of 192 kHz.

The McPDM interface extracts each data bit related to audio and sends it to the decimation filter of the corresponding channel. Therefore, for each audio uplink channel, the McPDM interface generates one bit data flow to the corresponding decimation filter at a rate of 3.528 Mbps for a sampling frequency of 88.2 kHz, or 3.84 Mbps for a sampling frequency of 96 kHz.

Moreover, when status information data are detected on the frame-sync signal (ABE_PDM_FRAME), the status information data are recovered and sent to the status channel. When no status information data are detected on the frame-sync signal, a null word (0x0000) is sent on the status channel.

For more information about protocols and data formats in normal mode, see Section 23.6.2.4.1, *Protocols and Data Formats in Normal Mode*. For more information about protocols and data formats in status mode, see Section 23.6.2.4.3, *Protocols and Data Formats in Status Mode*.

23.6.4.7.2.2 Decimation Filter

Each bit data flow is related to an audio uplink channel and is provided by the McPDM interface is processed by a decimation filter. The purpose of this filter is to band-limit the noise and downsample the incoming bit data flow to generate a 24-bit-wide signed data flow at a rate of 88.2 kbps for a sampling frequency of 88.2 kHz, or 96 kbps for a sampling frequency of 96 kHz.

23.6.4.7.2.3 FIFO Uplink Management

23.6.4.7.2.3.1 General Description

The McPDM module implements a FIFO for the uplink path for communication with the host processor in the device. The FIFO uplink can store up to 16 words. Each word is 96 bits wide and is a combination of 24-bit-wide signed audio uplink channel data coming from decimation filters and 16-bit-wide status information data coming from the McPDM interface.

Figure 23-170 shows the FIFO uplink overview.

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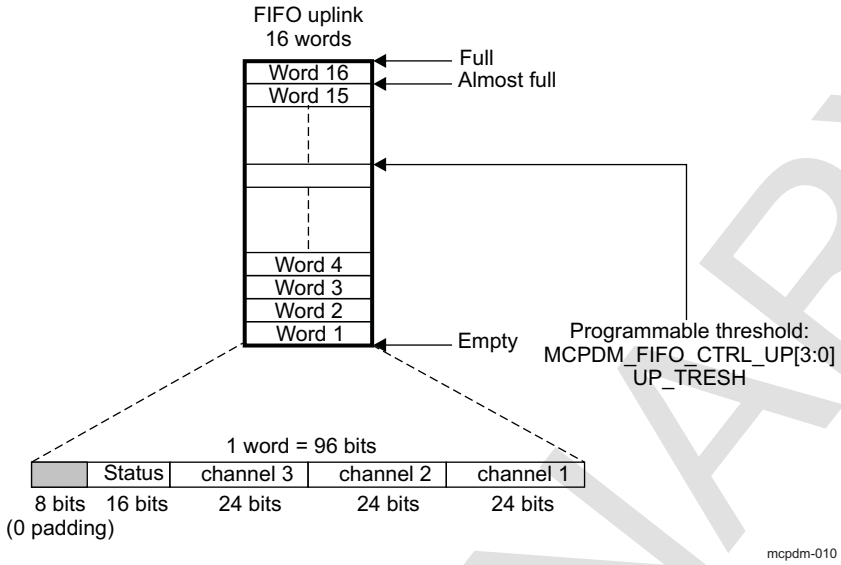
Figure 23-170. FIFO Uplink Overview



23.6.4.7.2.3.2 FIFO Operations

The FIFO uplink is filled with audio uplink channel data coming from decimation filters and status information data from the McPDM interface. Once the FIFO uplink threshold (MCPDM_FIFO_CTRL_UP[3:0] UP_TRESH bit field) is reached and, depending on conditions, an event occurs and generates an interrupt or DMA request.

NOTE: For more information about events generating an interrupt request, see Section 23.6.4.5, *McPDM Interrupt Requests*.

For more information about conditions for DMA request generation, see Section 23.6.4.6, *McPDM DMA Requests*.

When an interrupt request upon a FIFO uplink read-request event or an MCPDM_DMA_UP request occurs, the host processor or the DMA controller must read the words from the FIFO uplink (MCPDM_UP_DATA register). The number of read accesses from the host/DMA is determined by the following equation:

Num_read_access = (PDM_UP1_EN + PDM_UP2_EN + PDM_UP3_EN + STAT_INT) * (UP_THRESH), where the PDM_UP_THRESHOLD is programmed through the MCPDM_FIFO_CTRL_UP[3:0] UP_TRESH bit field.

PDM_UP1_EN, PDM_UP2_EN, PDM_UP3_EN, and STAT_INT are boolean values representing whether or not the corresponding channel is enabled.

For example, if audio uplink channels 1 and 3 are enabled, audio uplink channel 2 is disabled, the status channel is enabled, and the uplink threshold is programmed for one line only (MCPDM_FIFO_CTRL_UP[3:0] UP_THRESH = 0x0):

- Num_read_access = 3 because two audio uplink and the status channels are enabled.
- The first reading of the MCPDM_UP_DATA register should correspond to the audio uplink channel 1 data.
- The second reading of the MCPDM_UP_DATA register should correspond to the audio uplink channel 3 data.
- The third reading of the MCPDM_UP_DATA register should correspond to the status information data.

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NOTE: No status information has been sent by the external audio companion chip if the status channel is enabled and the 16 lower bits of the corresponding data read from the MCPDM_UP_DATA register is 0x0000 .

The audio uplink and status channels cannot be enabled or disabled on the fly during uplink signaling. The uplink path must first be forced to reset by setting the MCPDM_CTRL[11] SW_UP_RST bit to 1 before enabling or disabling any channels.

Because the audio uplink channel data are 24 bits wide and the MCPDM_UP_DATA register is 32 bits wide, the MCPDM_CTRL[8] PDMOUTFORMAT bit allows selecting the justification of the 24-bit audio uplink channel data in the MCPDM_UP_DATA register:

- When the MCPDM_CTRL[8] PDMOUTFORMAT bit is cleared to 0, the 24-bit-wide signed audio uplink channel data are left-justified with eight 0 padding bits for the lower bits.
- When the MCPDM_CTRL[8] PDMOUT FORMAT is set to 1, the 24-bit-wide signed audio uplink channel data are right-justified and sign-extended.

NOTE: The MCPDM_CTRL[8] PDMOUTFORMAT bit does not affect the status information format. When the status information data are read from the MCPDM_UP_DATA register, only the 16 lower bits are significant.

The setting of the MCPDM_CTRL[8] PDMOUTPUTFORMAT bit also affects the audio downlink channel data format.

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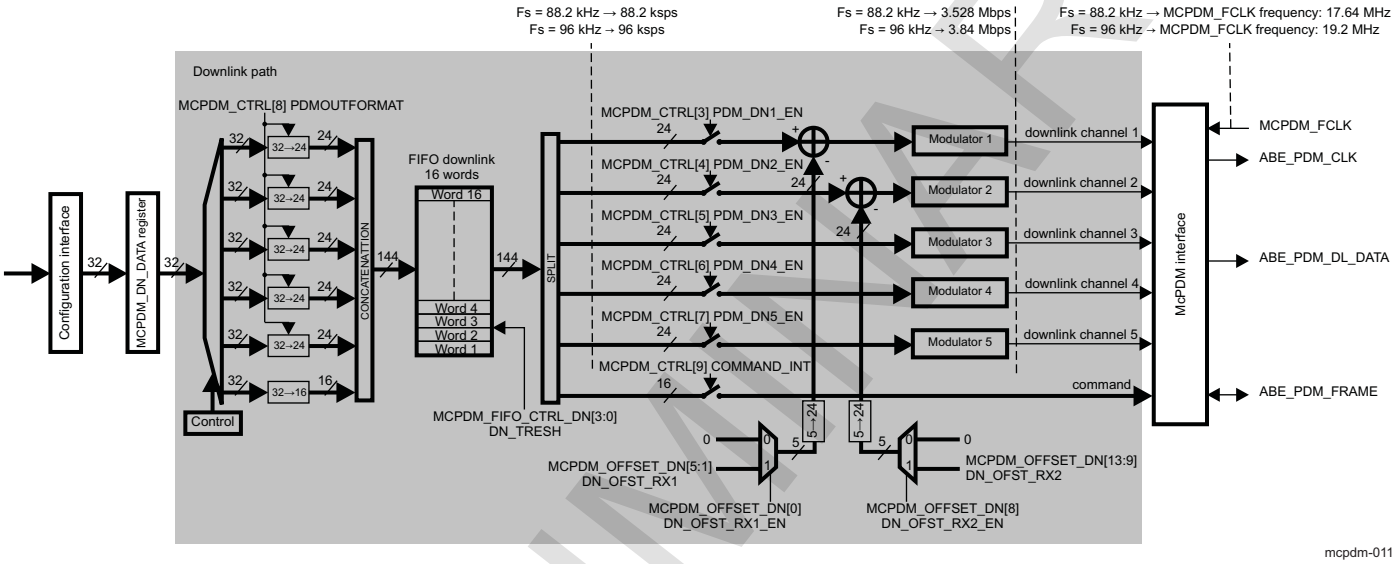
23.6.4.8 Downlink Path

Figure 23-171 is a detailed block diagram of the downlink path in the McPDM module.

Figure 23-171. Downlink Path Detailed Block Diagram



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23.6.4.8.1 Downlink Path Features

The downlink path has the following features:

- Five audio downlink channels
- Offset cancellation for audio downlink channels 1 and 2
- One command channel
- Delta-sigma modulator for each audio downlink channel
- 16-word FIFO downlink with threshold setting
- Audio channel data formatting

23.6.4.8.2 Downlink Path Description

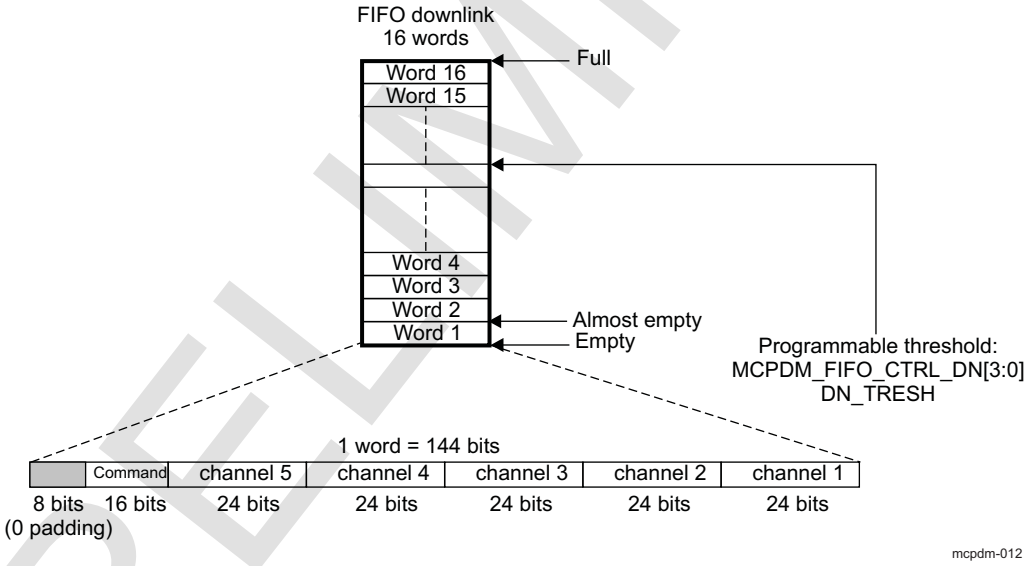
23.6.4.8.2.1 FIFO Downlink Management

23.6.4.8.2.1.1 General Description

The McPDM module implements a FIFO for the downlink path for communication with the host processor in the device. The FIFO downlink can store up to 16 words. Each word is 144 bits wide and is a combination of 24-bit-wide signed audio downlink channels data and 16-bit-wide command information data.

Figure 23-172 shows the FIFO downlink overview.

Figure 23-172. FIFO Downlink Overview



23.6.4.8.2.1.2 FIFO Operations

The FIFO downlink is read by the McPDM module and data related to the audio downlink channels are sent to the delta-sigma modulators, while the data related to the command information is sent to the McPDM interface. Once the FIFO pointer goes below the programmed threshold (the MCPDM_FIFO_CTRL_DN[3:0] DN_TRESH bit field), a DMA or interrupt request is sent to the DMA or interrupt handler and, depending on conditions, an event occurs and generates an interrupt or DMA request.

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NOTE: For more information about events generating an interrupt request, see Section 23.6.4.5, *McPDM Interrupt Requests*.

For more information about conditions for DMA request generation, see Section 23.6.4.6, *McPDM DMA Requests*.

When an interrupt request upon a FIFO downlink write-request event or a MCPDM_DMA_DOWN request occurs, it indicates that the next words are available to be written to the MCPDM_DN_DATA register. The minimum number of write accesses from the host/DMA is determined by the following equation:

Num_min_write_access = PDM_DN1_EN + PDM_DN2_EN + PDM_DN3_EN + PDM_DN4_EN + PDM_DN5_EN + CMD_INT

PDM_DN1_EN, PDM_DN2_EN, PDM_DN3_EN, PDM_DN4_EN, PDM_DN5_EN and CMD_INT are boolean values representing whether the corresponding channel is enable or not.

The maximum number of write accesses (before overwriting the data in the FIFO still to be transmitted) from the host/DMA is determined by the following equation:

Num_max_write_access = (FIFO_SIZE – DN_THRESH + 1) * (PDM_DN1_EN + PDM_DN2_EN + PDM_DN3_EN + PDM_DN4_EN + PDM_DN5_EN +CMD_INT)

FIFO_SIZE is the size of the downlink FIFO, and DN_THRESH is the downlink FIFO threshold, programmed through the MCPDM_FIFO_CTRL_DN[3:0] DN_THRESHOLD bit field.

For example, if audio downlink channels 1, 2, and 3 are enabled, audio downlink channels 4 and 5 are disabled, and the command channel is enabled:

- Num_min_write_access = 4, because three audio downlinks and the command channels are enabled.
- The first writing to the MCPDM_DN_DATA register should correspond to the audio downlink channel 1 data.
- The second writing to the MCPDM_DN_DATA register should correspond to the audio downlink channel 2 data.
- The third writing to the MCPDM_DN_DATA register should correspond to the audio downlink channel 3 data.
- The fourth writing to the MCPDM_DN_DATA register should correspond to the command information data.

NOTE: When the command channel is enabled and no command data need to be sent to the external audio companion chip, 0x0000 must be written to the 16 lower bits of the MCPDM_DN_DATA register as command data.

The audio downlink and command channels cannot be enabled or disabled on the fly during downlink signaling. The downlink path must first be forced to reset by setting the MCPDM_CTRL[12] SW_DN_RST bit to 1 before enabling or disabling any channels.

Because the audio downlink channel data are 24 bits wide and the MCPDM_DN_DATA register is 32 bits wide, the MCPDM_CTRL[8] PDMOUTFORMAT bit indicates the justification of the 24-bit audio downlink channel data in the MCPDM_DN_DATA register:

- When the MCPDM_CTRL[8] PDMOUTFORMAT is cleared to 0, the 24-bit-wide signed audio downlink channel data are left-justified with eight 0 padding bits for the lower bits.
- When MCPDM_CTRL[8] PDMOUT FORMAT is set to 1, the 24-bit-wide signed audio downlink channel data are right-justified and sign-extended.

NOTE: The MCPDM_CTRL[8] PDMOUTFORMAT bit does not affect the command information format. When the command information data are written to the MCPDM_DN_DATA register, only the 16 lower bits are significant.

The setting of the MCPDM_CTRL[8] PDMOUTPUTFORMAT bit also affects the audio uplink channel data format.

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23.6.4.8.2.1.3 Offset Cancellation

Because audio downlink channels 1 and 2 are related to the analog headset downlink path within the external audio companion chip, an offset cancellation feature is available for these channels to eliminate the offset of the analog headset downlink path.

When the offset cancellation feature is enabled, an offset value is subtracted from the audio data before being sent to the pulse-density modulator. The offset values are read from registers within the external audio companion chip and configured in the MCPDM_DN_OFFSET[5:1] DN_OFST_RX1 bit field for the audio downlink channel 1, and in the MCPDM_DN_OFFSET[13:9] DN_OFST_RX2 bit field for the audio downlink channel 2.

The offset cancellation feature is enabled or disabled by configuring the MCPDM_DN_OFFSET[0] DN_OFST_RX1_EN bit for the audio downlink channel 1, and the MCPDM_DN_OFFSET[8] DN_OFST_RX2_EN bit for the audio downlink channel 2 (00: Disabled, 10: Enabled).

23.6.4.8.2.1.4 Pulse-Density Modulators

Each 24-bit-wide data related to an audio downlink channel is processed by a pulse-density modulator. The purpose of this modulator is to upsample the incoming audio data and then perform a 1-bit pulse-density modulation to generate a 1-bit data flow at a rate of 3.528 Mbps for a sampling frequency of 88.2 kHz, or 3.84 Mbps for a sampling frequency of 96 kHz. The 1-bit pulse-density modulation allows using a 1-bit analog-to-digital converter (ADC) implemented in the external audio companion chip to convert the audio digital data into an audio analog signal.

23.6.4.8.2.1.4.1 Pulse-Density Modulators Watchdog Logic

If the 1-bit data flow coming out of the pulse-density modulator has 12 or more consecutive 1s or 0s, the pulse-density modulator had entered into an unstable or saturated condition. An unstable or saturated condition leads to unpredictable behavior of the pulse-density modulator, thereby producing random noise. To prevent this unstable or saturated condition from occurring, a watchdog logic is used to monitor the 1-bit output of the pulse-density modulator for 12 consecutive 1s or 12 consecutive 0s. If entry to an unstable condition is detected, the watchdog logic asserts the reset of the McPDM downlink paths for one clock pulse to put the McPDM hardware logic, related to the downlink mechanism, to initial state.

The watchdog logic is disabled by default. To enable it, the MCPDM_CTRL[14] WD_EN bit must be set to 0x1. If the watchdog logic is disabled, only the assertion of the downlink path reset MCPDM_CTRL[12] SW_DN_RST bit is allowed to reset the McPDM hardware logic, which is related to the downlink mechanism. If the watchdog logic is enabled, the downlink mechanism logic is reset when the downlink path reset or the watchdog reset is asserted.

Figure 23-173 shows the McPDM watchdog logic mechanism.

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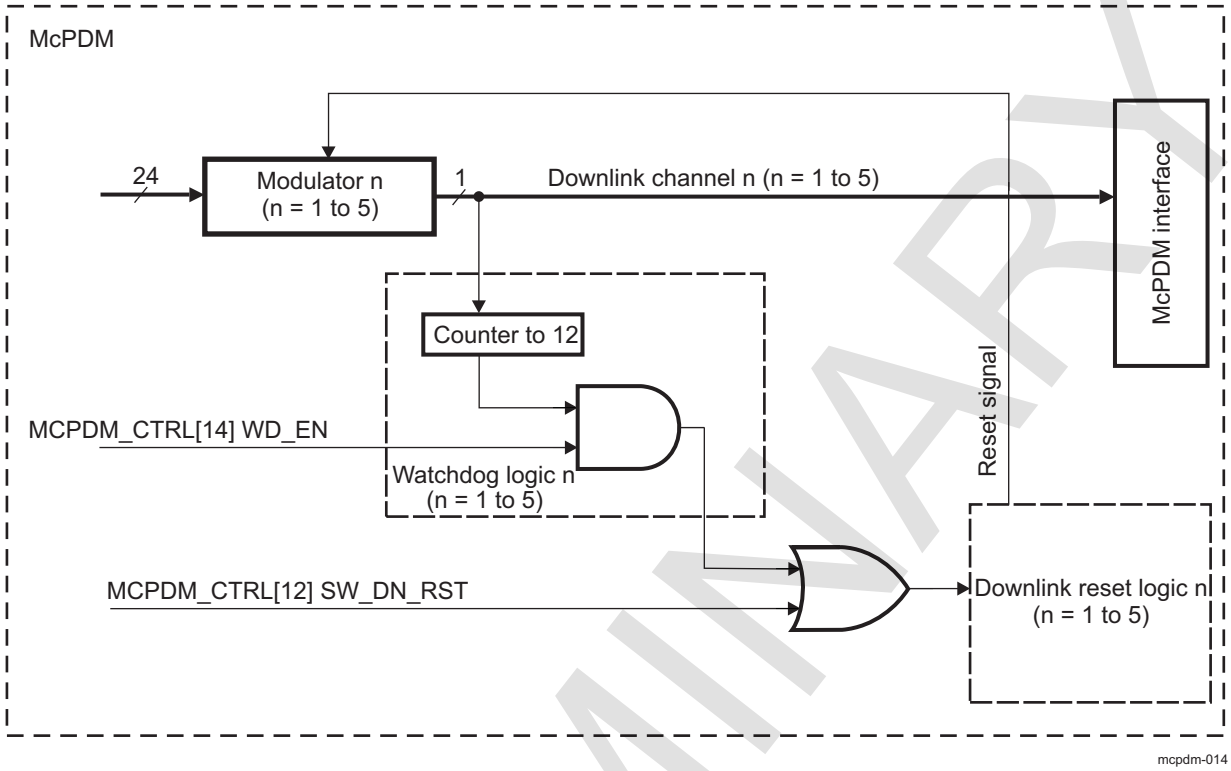
Figure 23-173. McPDM Watchdog Logic



23.6.4.8.2.1.5 Downlink Data Sent to the External Audio Companion Chip

The McPDM interface transmits the audio downlink channel data and command data to the external audio companion chip at a clock rate of 17.64 MHz for a sampling frequency of 88.2 kHz, or 19.2 MHz for a sampling frequency of 96 kHz.

The command data are sent on the frame-sync signal (ABE_PDM_FRAME) when the command channel is enabled. When the command channel is disabled or the command data is 0x0000, no command data is sent on the frame-sync signal.

NOTE: For more information about protocols and data formats in normal mode, see Section 23.6.2.4.1, *Protocols and Data Formats in Normal Mode*.

For more information about protocols and data formats in command mode, see Section 23.6.2.4.2, *Protocols and Data Formats in Command Mode*.

23.6.4.9 Error Reporting

During normal operation, when interrupt and DMA requests are properly served, no FIFO-uplink-full and no FIFO-downlink-empty events should occur.

Nevertheless, if one of these events occurs, the corresponding path must be forced to reset by software before being reconfigured. For more information about events servicing, see Section 23.6.5.1.2, *McPDM Events Servicing*.

Moreover, a FIFO-uplink-empty or FIFO-downlink-full event occurs only when all the channels of the corresponding path have been disabled during normal operation.

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NOTE: Channels must not be enabled or disabled during normal operation.

Channels can be enabled or disabled when the corresponding path is forced to reset. For more information about McPDM software reset, see Section 23.6.4.3, *McPDM Software Reset*.

23.6.5 McPDM Programming Guide

23.6.5.1 McPDM Low-Level Programming Models

This section describes the low-level hardware programming sequences for the configuration and use of the module.

23.6.5.1.1 Global Initialization

23.6.5.1.1.1 Surrounding Modules Global Initialization

This section identifies the requirements for initializing the surrounding modules in the device when the McPDM module is to be used for the first time after a device reset. This initialization of surrounding modules is based on the environment and the integration of the McPDM. For more information, see Section 23.6.2, *McPDM Environment*, and Section 23.6.3, *McPDM Integration*.

Table 23-462 describes the global initialization of surrounding modules.

Table 23-462. Global Initialization of Surrounding Modules

Surrounding Modules	Comments
PRCM module	The McPDM interface clock must be enabled and the functional clock must not be gated.
Control module	The McPDM-specific pad muxing must be configured in the device control module.
(Optional) Cortex-A9 MPU INTC (or DSP INTC)	The Cortex-A9 MPU (or DSP) INTC must be configured to enable the interrupt request generation to the Cortex-A9 MPU (or DSP) subsystem when interrupt requests are generated by the McPDM module.
(Optional) sDMA (or eDMA or aDMA)	The sDMA (or eDMA or aDMA) controller must be configured to account for the DMA requests generated by the McPDM module in the case of autonomous data transfers from/to memory.
(Optional) Interconnect	For more information about the interconnect configuration, see Chapter 13, *Interconnect*.
External audio chip	Initialize the external audio chip according to the specific needs.
I^2C controller	For more information about the I^2C initialization, see Section 23.1, *Multimaster High-Speed I^2C Controller*.

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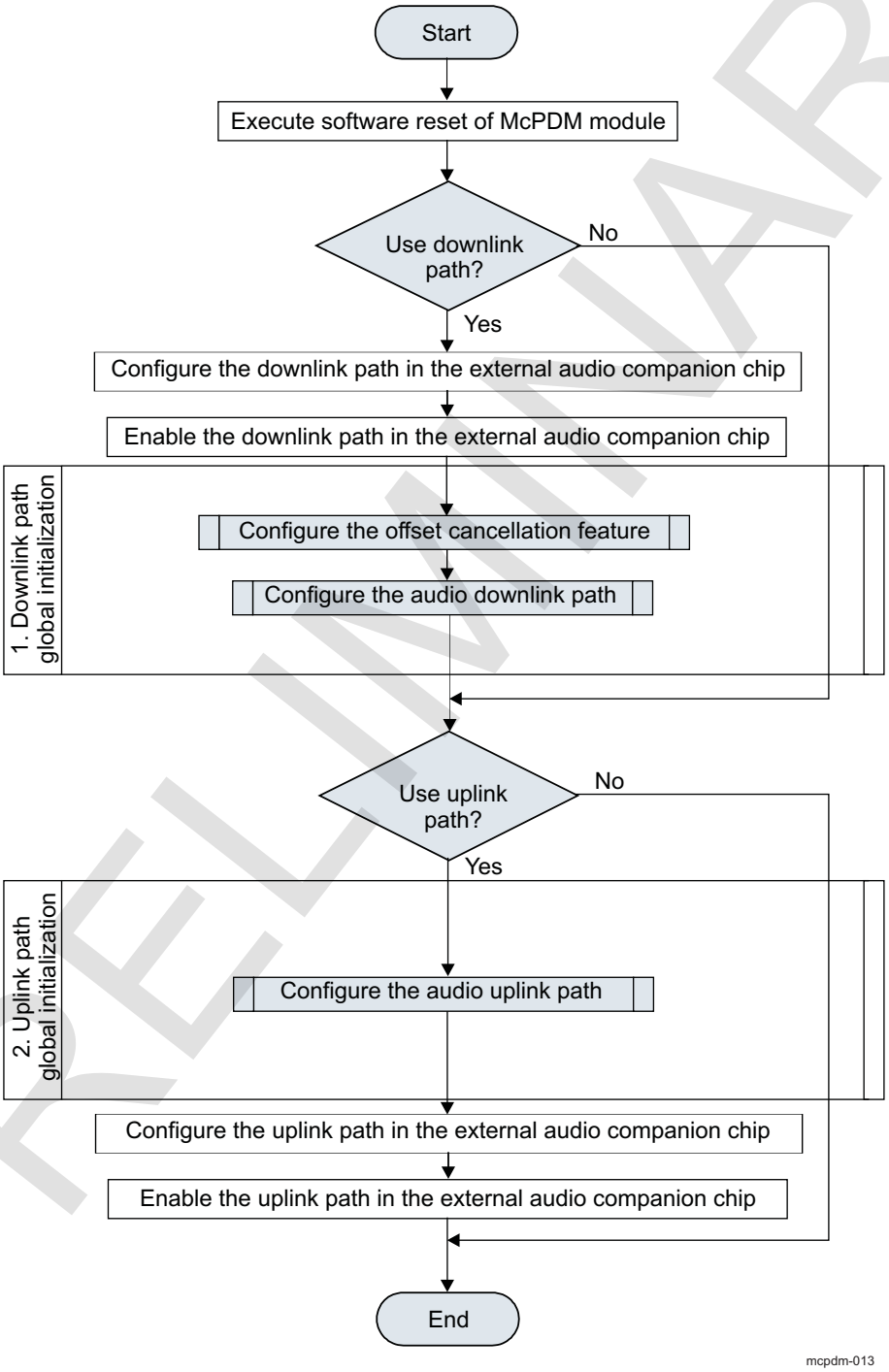
23.6.5.1.1.2 McPDM Global Initialization

23.6.5.1.1.2.1 Main Sequence – McPDM Global Initialization

This procedure initializes the McPDM after a power-on reset (POR) or software reset. Figure 23-174 shows a flow chart for the global initialization of the McPDM module.

Figure 23-174. McPDM Global Initialization Flow Chart



The McPDM software reset is executed by setting the MCPDM_SYSCONFIG[0] SOFTRESET bit to 0x1. To detect the reset done event, user software must check this bit until it is cleared to 0x0 by the hardware.

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Configuration of the offset cancellation feature is optional. The use of that feature depends on the characteristics of the external audio chip attached to the McPDM interface. If the external chip adds some DC offset on its output, then the offset cancellation feature of the McPDM must be used.

Table 23-463 describes the steps of the downlink path global initialization.

Table 23-463. McPDM Downlink Path Global Initialization

Procedure	Step	Access Type	Register/Bit Field/Programming Model	Value
Configure the offset cancellation feature. Only downlink path 1 and downlink path 2 can use the offset cancellation feature.	1. Read the offset value for the audio downlink path 1 from the external audio companion chip through the I^2C interface.	R	Offset register 1 in the external audio companion chip	OFFSET1
	2. Configure the offset of the audio downlink path 1.	W	MCPDM_DN_OFFSET[5:1] DN_OFST_RX1	OFFSET1
	3. Enable the offset cancellation feature for the audio downlink path 1.	W	MCPDM_DN_OFFSET[0] DN_OFST_RX1_EN	0x1
	4. Read the offset value for the audio downlink path 2 from the external audio companion chip through the I^2C interface.	R	Offset register 2 in the external audio companion chip	OFFSET2
	5. Configure the offset of the audio downlink path 2.	W	MCPDM_DN_OFFSET[13:9] DN_OFST_RX2	OFFSET2
	6. Enable the offset cancellation feature for the audio downlink path 2.	W	MCPDM_DN_OFFSET[8] DN_OFST_RX2_EN	0x1
Configure the audio downlink path.	1. Enable the interrupt request generation for the downlink path.	W	a. MCPDM_IRQENABLE_SET[3] DN_IRQ_FULL_MASK b. MCPDM_IRQENABLE_SET[2] DN_IRQ_ALMST_EMPTY_MASK c. MCPDM_IRQENABLE_SET[1] DN_IRQ_EMPTY_MASK d. MCPDM_IRQENABLE_SET[0] DN_IRQ_MASK	When downlink DMA request not used: 0xF When downlink DMA request used: 0xE
	2. Configure the FIFO downlink threshold.	W	MCPDM_FIFO_CTRL_DN[3:0] DN_TRESH	FIFO downlink threshold
	3. Enable the DMA request generation for the downlink path (optional: only if DMA request generation for the downlink path is required).	W	MCPDM_DMAENABLE_SET[0] DMA_DN_ENABLE	0x1
	4. Enable the downlink channels.	W	MCPDM_CTRL	See Table 23-459.

Table 23-464 describes the steps of the uplink path global initialization.

Table 23-464. McPDM Uplink Path Global Initialization

Step	Access Type	Register/Bit Field/Programming Model	Value
1. Enable the interrupt request generation for the uplink path.	W	a. MCPDM_IRQENABLE_SET[11] UP_IRQ_FULL_MASK b. MCPDM_IRQENABLE_SET[10] UP_IRQ_ALMST_FULL_MASK c. MCPDM_IRQENABLE_SET[9] UP_IRQ_EMPTY_MASK d. MCPDM_IRQENABLE_SET[8] UP_IRQ_MASK	When uplink DMA request not used: 0xF When uplink DMA request used: 0xE
2. Configure the FIFO uplink threshold.	W	MCPDM_FIFO_CTRL_UP[3:0] UP_TRESH	FIFO uplink threshold
3. Enable the DMA request generation for the uplink path (optional: only if DMA request generation for the uplink path is required).	W	MCPDM_DMAENABLE_SET[1] DMA_UP_ENABLE	0x1

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Table 23-464. McPDM Uplink Path Global Initialization (continued)

Step	Access Type	Register/Bit Field/Programming Model	Value
4. Configure the FIFO uplink sampling frequency.	W	MCPDM_CTRL[13] DIV_SEL	0x-
5. Enable the uplink channels.	W	MCPDM_CTRL	See Table 23-459.

23.6.5.1.2 McPDM Events Servicing

23.6.5.1.2.1 Downlink Path Event Servicing

Table 23-465 to Table 23-468 describe the downlink path event servicing.

When the four downlink interrupts are enabled and then the downlink channel(s) is enabled, the FIFO-downlink-write request (MCPDM_IRQSTATUS = 0x1), instead of the FIFO-downlink-empty request (MCPDM_IRQSTATUS = 0x2), is generated. The first audio data to be sent is written from the interrupt handler. The McPDM module can work in two ways:

- Enable the desired downlink channels, and then write in the downlink FIFO the audio data that is going to be sent.
- Write the audio data in the downlink FIFO, and then enable the desired downlink channels to send this audio data.

In either way, the FIFO-downlink-write request is generated.

Table 23-465. FIFO-Downlink-Full Event Servicing

Step	Access Type	Register/Bit Field/Programming Model	Value
TEST TA: Is FIFO downlink full?	R	MCPDM_IRQSTATUS[3] DN_IRQ_FULL	
IF: TRUE			0x1
Acknowledge event.	W	MCPDM_IRQSTATUS[3] DN_IRQ_FULL	0x1
Downlink path reset	W	MCPDM_CTRL[12] SW_DN_RST	0x1
Downlink path global initialization		See Table 23-463.	
Downlink path reset release	W	MCPDM_CTRL[12] SW_DN_RST	0x0
END			
ELSE			0x0
END			
END TEST TA			

Table 23-466. FIFO-Downlink-Empty Event Servicing

Step	Access Type	Register/Bit Field/Programming Model	Value
TEST TA: Is FIFO downlink empty?	R	MCPDM_IRQSTATUS[1] DN_IRQ_EMPTY	
IF: TRUE			0x1
Acknowledge event.	W	MCPDM_IRQSTATUS[1] DN_IRQ_EMPTY	0x1
Downlink path reset	W	MCPDM_CTRL[12] SW_DN_RST	0x1
Downlink path reconfiguration		See Table 23-463.	
Downlink path reset release	W	MCPDM_CTRL[12] SW_DN_RST	0x0
END			
ELSE			0x0
END			

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Table 23-466. FIFO-Downlink-Empty Event Servicing (continued)

Step	Access Type	Register/Bit Field/Programming Model	Value
END TEST TA			

Table 23-467. FIFO-Downlink-Almost-Empty Event Servicing

Step	Access Type	Register/Bit Field/Programming Model	Value
TEST TA: Is FIFO downlink almost empty?	R	MCPDM_IRQSTATUS[2] DN_IRQ_ALST_EMPTY	
IF: TRUE			0x1
Acknowledge event.	W	MCPDM_IRQSTATUS[2] DN_IRQ_ALST_EMPTY	0x1
Downlink path reset	W	MCPDM_CTRL[12] SW_DN_RST	0x1
Downlink path reconfiguration		See Table 23-463.	
Downlink path reset release	W	MCPDM_CTRL[12] SW_DN_RST	0x0
END			
ELSE			0x0
END			
END TEST TA			

Table 23-468. FIFO Downlink Write-Request Event Servicing

Step	Access Type	Register/Bit Field/Programming Model	Value
TEST TA: Is FIFO downlink write requested?	R	MCPDM_IRQSTATUS[0] DN_IRQ	
IF: TRUE			0x1
Write FIFO downlink register (see Section 23.6.4.8.2.1.2 for more information).	W	MCPDM_DN_DATA	
Acknowledge event.	W	MCPDM_IRQSTATUS[0] DN_IRQ	0x1
END			
ELSE			0x0
END			
END TEST TA			

23.6.5.1.2.2 Uplink Path Events Servicing

Table 23-469 to Table 23-471 describe the uplink path event servicing.

Table 23-469. FIFO-Uplink-Full Event Servicing

Step	Access Type	Register/Bit Field/Programming Model	Value
TEST TA: Is FIFO-uplink-full?	R	MCPDM_IRQSTATUS[11] UP_IRQ_FULL	
IF: TRUE			0x1
Acknowledge event.	W	MCPDM_IRQSTATUS[11] UP_IRQ_FULL	0x1
Uplink path reset	W	MCPDM_CTRL[11] SW_UP_RST	0x1
Uplink path global initialization		See Table 23-464.	
Uplink path reset release	W	MCPDM_CTRL[11] SW_UP_RST	0x0
END			
ELSE			0x0
END			
END TEST TA			

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Table 23-470. FIFO-Uplink-Almost-Full Event Servicing

Step	Access Type	Register/Bit Field/Programming Model	Value
TEST TA: Is FIFO-uplink-almost-full?	R	MCPDM_IRQSTATUS[10] UP_IRQ_ALST_FULL	
IF: TRUE			0x1
Acknowledge event.	W	MCPDM_IRQSTATUS[10] UP_IRQ_ALST_FULL	0x1
Uplink path reset	W	MCPDM_CTRL[12] SW_DN_RST	0x1
Uplink path reconfiguration		SeeTable 23-464.	
Uplink path reset release	W		0x0
END			
ELSE			0x0
END			
END TEST TA			

Table 23-471. FIFO-Uplink-Empty Event Servicing

Step	Access Type	Register/Bit Field/Programming Model	Value
TEST TA: Is FIFO uplink empty?	R	MCPDM_IRQSTATUS[9] UP_IRQ_EMPTY	
IF: TRUE			0x1
Acknowledge event.	W	MCPDM_IRQSTATUS[9] UP_IRQ_EMPTY	0x1
Uplink path reset	W	MCPDM_CTRL[11] SW_UP_RST	0x1
Uplink path reconfiguration		See Table 23-464	
Uplink path reset release	W	MCPDM_CTRL[11] SW_UP_RST	0x0
END			
ELSE			0x0
END			
END TEST TA			

Table 23-472. FIFO-Uplink-Read-Request Event Servicing

Step	Access Type	Register/Bit Field/Programming Model	Value
TEST TA: Is FIFO uplink read requested?	R	MCPDM_IRQSTATUS[8] UP_IRQ	
IF: TRUE			0x1
Read FIFO uplink register (see Section 23.6.4.7.2.3.2 for more information).	R	MCPDM_UP_DATA	
Acknowledge event.	W	MCPDM_IRQSTATUS[8] UP_IRQ	0x1
END			
ELSE			0x0
END			
END TEST TA			

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23.6.6 McPDM Register Manual

23.6.6.1 McPDM Instance Summary

Table 23-473 summarizes the McPDM instance.

Table 23-473. McPDM Instance Summary

Module Name	Base Address L3 Interconnect	Base Address Cortex-A9 Private Access	Base Address DSP Private Access	Size
McPDM	0x4903 2000	0x4013 2000	0x3 2000	4KB

NOTE: Private access is an access that does not use the L3/L4 interconnects.

23.6.6.2 McPDM Registers

23.6.6.2.1 McPDM Register Summary

Table 23-474 summarizes the McPDM register mapping.

Table 23-474. McPDM Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	Physical Address L3 Interconnect	Physical Address Cortex-A9 Private Access	Physical Address DSP Private Access
MCPDM_REVISION	R	32	0x0000 0000	0x4903 2000	0x4013 2000	0x3 2000
MCPDM_SYSCONFIG	RW	32	0x0000 0010	0x4903 2010	0x4013 2010	0x3 2010
RESERVED	RW	32	0x0000 0020	0x4903 2020	0x4013 2020	0x3 2020
MCPDM_IRQSTATUS_RAW	RW	32	0x0000 0024	0x4903 2024	0x4013 2024	0x3 2024
MCPDM_IRQSTATUS	RW	32	0x0000 0028	0x4903 2028	0x4013 2028	0x3 2028
MCPDM_IRQENABLE_SET	RW	32	0x0000 002C	0x4903 202C	0x4013 202C	0x3 202C
MCPDM_IRQENABLE_CLR	RW	32	0x0000 0030	0x4903 2030	0x4013 2030	0x3 2030
MCPDM_IRQWAKEEN	RW	32	0x0000 0034	0x4903 2034	0x4013 2034	0x3 2034
MCPDM_DMAENABLE_SET	RW	32	0x0000 0038	0x4903 2038	0x4013 2038	0x3 2038
MCPDM_DMAENABLE_CLR	RW	32	0x0000 003C	0x4903 203C	0x4013 203C	0x3 203C
MCPDM_DMAWAKEEN	RW	32	0x0000 0040	0x4903 2040	0x4013 2040	0x3 2040
MCPDM_CTRL	RW	32	0x0000 0044	0x4903 2044	0x4013 2044	0x3 2044
MCPDM_DN_DATA	RW	32	0x0000 0048	0x4903 2048	0x4013 2048	0x3 2048
MCPDM_UP_DATA	R	32	0x0000 004C	0x4903 204C	0x4013 204C	0x3 204C
MCPDM_FIFO_CTRL_DN	RW	32	0x0000 0050	0x4903 2050	0x4013 2050	0x3 2050
MCPDM_FIFO_CTRL_UP	RW	32	0x0000 0054	0x4903 2054	0x4013 2054	0x3 2054
MCPDM_DN_OFFSET	RW	32	0x0000 0058	0x4903 2058	0x4013 2058	0x3 2058
RESERVED	RW	32	0x0000 005C	0x4903 205C	0x4013 205C	0x3 205C
RESERVED	RW	32	0x0000 0060	0x4903 2060	0x4013 2060	0x3 2060
RESERVED	RW	32	0x0000 0064	0x4903 2064	0x4013 2064	0x3 2064
RESERVED	R	32	0x0000 0068	0x4903 2068	0x4013 2068	0x3 2068
RESERVED	RW	32	0x0000 006C	0x4903 206C	0x4013 206C	0x3 206C
RESERVED	RW	32	0x0000 0070	0x4903 2070	0x4013 2070	0x3 2070
RESERVED	R	32	0x0000 0074	0x4903 2074	0x4013 2074	0x3 2074

23.6.6.2.2 McPDM Register Description

Table 23-475 through Table 23-505 describe the individual McPDM registers.

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Table 23-475. MCPDM_REVISION

Address Offset	0x0000 0000		
Physical Address	0x4903 2000 0x4013 2000 0x3 2000	**Instance**	MCPDM_L3 MCPDM_CORTEX-A9 MCPDM_DSP
Description	IP revision identifier (X.Y.R) used by software to track features, bugs, and compatibility		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP revision	R	TI internal data

Table 23-476. Register Call Summary for Register MCPDM_REVISION

Multichannel PDM Controller

- McPDM Register Summary: [0]

Table 23-477. MCPDM_SYSCONFIG

Address Offset	0x0000 0010		
Physical Address	0x4903 2010 0x4013 2010 0x3 2010	**Instance**	MCPDM_L3 MCPDM_CORTEX-A9 MCPDM_DSP
Description	This register allows controlling various parameters of the OCP interface.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												IDLEMODE		FREEMU	SOFTRESET

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0000000
3:2	IDLEMODE	Configuration of the idle mode. 0x0: Force- idle. idle request is acknowledged unconditionally and immediately. No wake-up capability. 0x1: No-idle. Idle request is never acknowledged. No wake-up capability. 0x2: Smart-idle. The acknowledgment to an idle request is given based on the internal activity. No wake-up capability. 0x3: Idle request acknowledged pending internal conditions, asynchronous wake-up enabled. Wakeup capability.	RW	0x2
1	FREEMU	Sensitivity to emulation (debug) suspend input signal. 0x0: McPDM module is sensitive to emulation suspend. 0x1: McPDM module is not sensitive to emulation suspend.	RW	0

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Bits	Field Name	Description	Type	Reset
0	SOFTRESET	McPDM software Reset. Write 0x0: No Action Read 0x0: No ongoing software reset Read 0x1: Reset is ongoing Write 0x1: Start software reset	RW	0

Table 23-478. Register Call Summary for Register MCPDM_SYSCONFIG

Multichannel PDM Controller

- McPDM Software Reset: [0] [1]
- McPDM Power Management: [2] [3]
- Global Initialization: [4]
- McPDM Register Summary: [5]

Table 23-479. MCPDM_IRQSTATUS_RAW

Address Offset	0x0000 0024		
Physical Address	0x4903 2024 0x4013 2024 0x3 2024	**Instance**	MCPDM_L3 MCPDM_CORTEX-A9 MCPDM_DSP
Description	Interrupt request raw status register (for debug purpose).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				UP_IRQ_FULL	UP_IRQ_ALST_FULL	UP_IRQ_EMPTY	UP_IRQ	RESERVED				DN_IRQ_FULL	DN_IRQ_ALST_EMPTY	DN_IRQ_EMPTY	DN_IRQ

Bits	Field Name	Description	Type	Reset
31:12	RESERVED		R	0x00000
11	UP_IRQ_FULL	FIFO-uplink-full signal appears when a write access is performed and the FIFO uplink is already full. Read 0x0: No event pending Write 0x0: No action Write 0x1: Set the event (for debug) Read 0x1: Event pending	RW	0
10	UP_IRQ_ALST_FULL	FIFO uplink almost-full signal appears when the FIFO uplink contains (FIFO uplink size – 1) elements. Read 0x0: No event pending Write 0x0: No action Write 0x1: Set the event (for debug) Read 0x1: Event pending	RW	0
9	UP_IRQ_EMPTY	FIFO uplink empty signal appears when a read access is done and FIFO uplink already empty. Read 0x0: No event pending Write 0x0: No action Write 0x1: Set the event (for debug) Read 0x1: Event pending	RW	0

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Bits	Field Name	Description	Type	Reset
8	UP_IRQ	FIFO uplink interrupt appears when the number of data present in the FIFO uplink has reached the value of the FIFO uplink threshold. Read 0x0: No event pending Write 0x0: No action Write 0x1: Set the event (for debug) Read 0x1: Event pending	RW	0
7:4	RESERVED	Reserved	R	0x0
3	DN_IRQ_FULL	FIFO downlink full signal appears when the FIFO uplink is full and another a write access is performed. Read 0x0: No event pending Write 0x0: No action Write 0x1: Set the event (for debug) Read 0x1: Event pending	RW	0
2	DN_IRQ_ALST_EMPTY	FIFO downlink almost empty signal appears when the FIFO downlink contains only one element. Read 0x0: No event pending Write 0x0: No action Write 0x1: Set the event (for debug) Read 0x1: Event pending	RW	0
1	DN_IRQ_EMPTY	FIFO-downlink-empty signal appears when read access is performed and FIFO downlink is already empty. Read 0x0: No event pending Write 0x0: No action Write 0x1: Set the event (for debug) Read 0x1: Event pending	RW	0
0	DN_IRQ	FIFO downlink status is set when the number of data is below the FIFO downlink threshold value. Read 0x0: No event pending Write 0x0: No action Write 0x1: Set the event (for debug) Read 0x1: Event pending	RW	0

Table 23-480. Register Call Summary for Register MCPDM_IRQSTATUS_RAW

Multichannel PDM Controller

- McPDM Interrupt Requests: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13]
- McPDM Register Summary: [14]

Table 23-481. MCPDM_IRQSTATUS

Address Offset	0x0000 0028		
Physical Address	0x4903 2028 0x4013 2028 0x3 2028	**Instance**	MCPDM_L3 MCPDM_CORTEX-A9 MCPDM_DSP
Description	Interrupt request status register.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				UP_IRQ_FULL	UP_IRQ_ALST_FULL	UP_IRQ_EMPTY	UP_IRQ	RESERVED				DN_IRQ_FULL	DN_IRQ_ALST_EMPTY	DN_IRQ_EMPTY	DN_IRQ

Bits	Field Name	Description	Type	Reset
31:12	RESERVED		R	0x00000
11	UP_IRQ_FULL	FIFO-uplink-full signal appears when a write access is performed and the FIFO uplink is already full. Read 0x0: No event pending Write 0x0: No action Write 0x1: Clear pending event Read 0x1: Event pending	RW	0
10	UP_IRQ_ALST_FULL	FIFO uplink almost-full signal appears when the FIFO uplink contains (FIFO uplink size – 1) elements. Read 0x0: No event pending Write 0x0: No action Write 0x1: Clear pending event Read 0x1: Event pending	RW	0
9	UP_IRQ_EMPTY	FIFO uplink empty signal appears when a read access is done and FIFO uplink already empty. Read 0x0: No event pending Write 0x0: No action Write 0x1: Clear pending event Read 0x1: Event pending	RW	0
8	UP_IRQ	FIFO uplink interrupt appears when the number of data present in the FIFO uplink has reached the value of the FIFO uplink threshold. Read 0x0: No event pending Write 0x0: No action Write 0x1: Clear pending event Read 0x1: Event pending	RW	0
7:4	RESERVED		R	0x0
3	DN_IRQ_FULL	FIFO downlink full signal appears when the FIFO uplink is full and another a write access is performed. Read 0x0: No event pending Write 0x0: No action Write 0x1: Clear pending event Read 0x1: Event pending	RW	0
2	DN_IRQ_ALST_EMPTY	FIFO downlink almost empty signal appears when the FIFO downlink contains only one element. Read 0x0: No event pending Write 0x0: No action Write 0x1: Clear pending event Read 0x1: Event pending	RW	0

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Bits	Field Name	Description	Type	Reset
1	DN_IRQ_EMPTY	FIFO-downlink-empty signal appears when read access is performed and FIFO downlink is already empty. Read 0x0: No event pending Write 0x0: No action Write 0x1: Clear pending event Read 0x1: Event pending	RW W1toSet	0
0	DN_IRQ	FIFO downlink status is set when the number of data is below the FIFO downlink threshold value. Read 0x0: No event pending Write 0x0: No action Write 0x1: Clear pending event Read 0x1: Event pending	RW	0

Table 23-482. Register Call Summary for Register MCPDM_IRQSTATUS

Multichannel PDM Controller

- McPDM Interrupt Requests: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11]
- McPDM Events Servicing: [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23] [24] [25] [26] [27] [28] [29]
- McPDM Register Summary: [30]

Table 23-483. MCPDM_IRQENABLE_SET

Address Offset	0x0000 002C		
Physical Address	0x4903 202C 0x4013 202C 0x3 202C	**Instance**	MCPDM_L3 MCPDM_CORTEX-A9 MCPDM_DSP
Description	Interrupt request enable set register.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				UP_IRQ_FULL_MASK	UP_IRQ_ALST_FULL_MASK	UP_IRQ_EMPTY_MASK	UP_IRQ_MASK	RESERVED				DN_IRQ_FULL_MASK	DN_IRQ_ALST_EMPTY_MASK	DN_IRQ_EMPTY_MASK	DN_IRQ_MASK

Bits	Field Name	Description	Type	Reset
31:12	RESERVED		R	0x00000
11	UP_IRQ_FULL_MASK	FIFO-uplink-full event interrupt enabling bit. Read 0x0: Interrupt disabled Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled	RW	0

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Bits	Field Name	Description	Type	Reset
10	UP_IRQ_ALST_FULL_MASK	FIFO-uplink-almost-full event interrupt enabling bit. Read 0x0: Interrupt disabled Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled	RW	0
9	UP_IRQ_EMPTY_MASK	FIFO-uplink-empty event interrupt enabling bit. Read 0x0: Interrupt disabled Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled	RW	0
8	UP_IRQ_MASK	FIFO-uplink-read-request event interrupt enabling bit. Read 0x0: Interrupt disabled Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled	RW	0
7:4	RESERVED		R	0x0
3	DN_IRQ_FULL_MASK	FIFO-downlink-full event interrupt enabling bit. Read 0x0: Interrupt disabled Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled	RW	0
2	DN_IRQ_ALST_EMPTY_MASK	FIFO downlink almost-empty event interrupt enabling bit. Read 0x0: Interrupt disabled Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled	RW	0
1	DN_IRQ_EMPTY_MASK	FIFO-downlink-empty event interrupt enabling bit. Read 0x0: Interrupt disabled Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled	RW	0
0	DN_IRQ_MASK	FIFO downlink write-request event interrupt enabling bit. Read 0x0: Interrupt disabled Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled	RW	0

Table 23-484. Register Call Summary for Register MCPDM_IRQENABLE_SET

Multichannel PDM Controller

- McPDM Interrupt Requests: [0] [1] [2] [3] [4] [5] [6] [7] [8]
- Global Initialization: [9] [10] [11] [12] [13] [14] [15] [16]
- McPDM Register Summary: [17]

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Table 23-485. MCPDM_IRQENABLE_CLR

Address Offset	0x0000 0030		
Physical Address	0x4903 2030 0x4013 2030 0x3 2030	**Instance**	MCPDM_L3 MCPDM_CORTEX-A9 MCPDM_DSP
Description	Interrupt request enable clear register.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				UP_IRQ_FULL_MASK	UP_IRQ_ALST_FULL_MASK	UP_IRQ_EMPTY_MASK	UP_IRQ_MASK	RESERVED				DN_IRQ_FULL_MASK	DN_IRQ_ALST_EMPTY_MASK	DN_IRQ_EMPTY_MASK	DN_IRQ_MASK

Bits	Field Name	Description	Type	Reset
31:12	RESERVED		R	0x00000
11	UP_IRQ_FULL_MASK	FIFO-uplink-full event interrupt disabling bit. Read 0x0: Interrupt disabled Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled	RW	0
10	UP_IRQ_ALST_FULL_MASK	FIFO-uplink-almost-full event interrupt disabling bit. Read 0x0: Interrupt disabled Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled	RW	0
9	UP_IRQ_EMPTY_MASK	FIFO-uplink-empty event interrupt disabling bit. Read 0x0: Interrupt disabled Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled	RW	0
8	UP_IRQ_MASK	FIFO-uplink-read-request event interrupt disabling bit. Read 0x0: Interrupt disabled Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled	RW	0
7:4	RESERVED		R	0x0
3	DN_IRQ_FULL_MASK	FIFO-downlink-full event interrupt disabling bit. Read 0x0: Interrupt disabled Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled	RW	0

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Bits	Field Name	Description	Type	Reset
2	DN_IRQ_ALST_EMPTY_MASK	FIFO downlink almost-empty event interrupt disabling bit. Read 0x0: Interrupt disabled Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled	RW	0
1	DN_IRQ_EMPTY_MASK	FIFO-downlink-empty event interrupt disabling bit. Read 0x0: Interrupt disabled Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled	RW	0
0	DN_IRQ_MASK	FIFO downlink write-request event interrupt disabling bit. Read 0x0: Interrupt disabled Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled	RW	0

Table 23-486. Register Call Summary for Register MCPDM_IRQENABLE_CLR

Multichannel PDM Controller

- McPDM Interrupt Requests: [0] [1] [2] [3] [4] [5] [6] [7] [8]
- McPDM Register Summary: [9]

Table 23-487. MCPDM_IRQWAKEEN

Address Offset	0x0000 0034		
Physical Address	0x4903 2034 0x4013 2034 0x3 2034	**Instance**	MCPDM_L3 MCPDM_CORTEX-A9 MCPDM_DSP
Description	Interrupt request wake-up enable register.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														IRQ_WAKEUP_UP_EN	IRQ_WAKEUP_DN_EN

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	IRQ_WAKEUP_UP_EN	Enabling/disabling bit for wake-up request generation upon a FIFO-uplink-read-request event. 0x0: Disable the wake-up request generation 0x1: Enable the wake-up request generation	RW	1
0	IRQ_WAKEUP_DN_EN	Enabling/disabling bit for wake-up by FIFO downlink write-request event. 0x0: Disable the wake-up request generation 0x1: Enable the wake-up request generation	RW	1

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Table 23-488. Register Call Summary for Register MCPDM_IRQWAKEEN

Multichannel PDM Controller

- McPDM Power Management: [0] [1] [2]
- McPDM Register Summary: [3]

Table 23-489. MCPDM_DMAENABLE_SET

Address Offset	0x0000 0038		
Physical Address	0x4903 2038 0x4013 2038 0x3 2038	**Instance**	MCPDM_L3 MCPDM_CORTEX-A9 MCPDM_DSP
Description	DMA request enable set register.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														DMA_UP_ENABLE	DMA_DN_ENABLE

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	DMA_UP_ENABLE	Uplink path DMA request generation enabling bit. Read 0x0: DMA request disabled Write 0x0: No action Write 0x1: Enable DMA request Read 0x1: DMA request enabled	RW	0
0	DMA_DN_ENABLE	Downlink path DMA request generation enabling bit. Read 0x0: DMA request disabled Write 0x0: No action Write 0x1: Enable DMA request Read 0x1: DMA request enabled	RW	0

Table 23-490. Register Call Summary for Register MCPDM_DMAENABLE_SET

Multichannel PDM Controller

- McPDM DMA Requests: [0] [1] [2] [3]
- Global Initialization: [4] [5]
- McPDM Register Summary: [6]

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Table 23-491. MCPDM_DMAENABLE_CLR

Address Offset	0x0000 003C		
Physical Address	0x4903 203C 0x4013 203C 0x3 203C	**Instance**	MCPDM_L3 MCPDM_CORTEX-A9 MCPDM_DSP
Description	DMA request enable clear register.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														DMA_UP_ENABLE	DMA_DN_ENABLE

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	DMA_UP_ENABLE	Uplink path DMA request generation disabling bit. Read 0x0: DMA request disabled Write 0x0: No action Write 0x1: Disable DMA request Read 0x1: DMA request enabled	RW	0
0	DMA_DN_ENABLE	Downlink path DMA request generation disabling bit. Read 0x0: DMA request disabled Write 0x0: No action Write 0x1: Disable DMA request Read 0x1: DMA request enabled	RW	0

Table 23-492. Register Call Summary for Register MCPDM_DMAENABLE_CLR

Multichannel PDM Controller

- McPDM DMA Requests: [0] [1] [2] [3]
- McPDM Register Summary: [4]

Table 23-493. MCPDM_DMAWAKEEN

Address Offset	0x0000 0040		
Physical Address	0x4903 2040 0x4013 2040 0x3 2040	**Instance**	MCPDM_L3 MCPDM_CORTEX-A9 MCPDM_DSP
Description	DMA request wake-up enable register.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														DMA_WAKEUP_UP_EN	DMA_WAKEUP_DN_EN

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Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	DMA_WAKEUP_UP_EN	Enabling/disabling bit for wake-up request generation upon an uplink path DMA request. 0x0: Disable the wake-up request generation 0x1: Enable the wake-up request generation	RW	1
0	DMA_WAKEUP_DN_EN	Enabling/disabling bit for wake-up request generation upon a downlink path DMA request. 0x0: Disable the wake-up request generation 0x1: Enable the wake-up request generation	RW	1

Table 23-494. Register Call Summary for Register MCPDM_DMAWAKEEN

Multichannel PDM Controller
- McPDM Power Management: [0] [1] [2]
- McPDM Register Summary: [3]

Table 23-495. MCPDM_CTRL

Address Offset	0x0000 0044		
Physical Address	0x4903 2044 0x4013 2044 0x3 2044	**Instance**	MCPDM_L3 MCPDM_CORTEX-A9 MCPDM_DSP
Description	MCPDM control register.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																WD_EN	DIV_SEL	SW_DN_RST	SW_UP_RST	STATUS_INT	CMD_INT	PDMOUTFORMAT	PDM_DN5_EN	PDM_DN4_EN	PDM_DN3_EN	PDM_DN2_EN	PDM_DN1_EN	PDM_UP3_EN	PDM_UP2_EN	PDM_UP1_EN	

Bits	Field Name	Description	Type	Reset
31:15	RESERVED	Reserved	R	0x00000
14	WD_EN	This bit is used to enable or disable the pulse-density modulator watchdog logic. 0x0: Disabled (default after reset) 0x1: Enabled	RW	0
13	DIV_SEL	Multiply by 2 the FS of the uplink path 0x0: FS = 88.2 kHz, or 96 kHz 0x1: FS = 176.4 kHz, or 192 kHz	RW	0
12	SW_DN_RST	Software reset of the downlink path. 0x0: Downlink path is out of reset. 0x1: Reset of the downlink path	RW	0
11	SW_UP_RST	Software reset of the uplink path. 0x0: Uplink path is out of reset. 0x1: Reset of the uplink path	RW	0
10	STATUS_INT	Status channel enabling/disabling bit. 0x0: Status channel is disabled. 0x1: Status channel is enabled.	RW	0

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Bits	Field Name	Description	Type	Reset
9	CMD_INT	Command channel enabling/disabling bit. 0x0: Command channel is disabled. 0x1: Command channel is enabled.	RW	0
8	PDMOUTFORMAT	Audio format selection: 0x0:Left justification with eight 0-bit padding added for the less significant bits 0x1: Right justification with sign bit extended to the 8 MSBs	RW	0
7	PDM_DN5_EN	Audio downlink channel 5 enabling/disabling bit	RW	0
6	PDM_DN4_EN	Audio downlink channel 4 enabling/disabling bit	RW	0
5	PDM_DN3_EN	Audio downlink channel 3 enabling/disabling bit	RW	0
4	PDM_DN2_EN	Audio downlink channel 2 enabling/disabling bit	RW	0
3	PDM_DN1_EN	Audio downlink channel 1 enabling/disabling bit	RW	0
2	PDM_UP3_EN	Audio uplink channel 3 enabling/disabling bit	RW	0
1	PDM_UP2_EN	Audio uplink channel 2 enabling/disabling bit	RW	0
0	PDM_UP1_EN	Audio uplink channel 1 enabling/disabling bit	RW	0

Table 23-496. Register Call Summary for Register MCPDM_CTRL

Multichannel PDM Controller

- Protocols and Data Formats in Normal Mode: [0]
- Protocols and Data Formats in Command Mode: [1] [2] [3]
- Protocols and Data Formats in Status Mode: [4] [5] [6]
- McPDM Software Reset: [7] [8] [9] [10]
- McPDM Power Management: [11] [12] [13] [14] [15] [16]
- Uplink Path Description: [17] [18] [19] [20] [21] [22] [23]
- Downlink Path Description: [24] [25] [26] [27] [28] [29] [30] [31]
- Global Initialization: [32] [33] [34]
- McPDM Events Servicing: [35] [36] [37] [38] [39] [40] [41] [42] [43] [44] [45]
- McPDM Register Summary: [46]

Table 23-497. MCPDM_DN_DATA

Address Offset	0x0000 0048		
Physical Address	0x4903 2048 0x4013 2048 0x3 2048	**Instance**	MCPDM_L3 MCPDM_CORTEX-A9 MCPDM_DSP
Description	Downlink path data register.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DN_DATA																															

Bits	Field Name	Description	Type	Reset
31:0	DN_DATA	Downlink path data value	RW	0x0000 0000

Table 23-498. Register Call Summary for Register MCPDM_DN_DATA

Multichannel PDM Controller

- Protocols and Data Formats in Command Mode: [0] [1]
- Downlink Path Description: [2] [3] [4] [5] [6] [7] [8] [9] [10]
- McPDM Events Servicing: [11]
- McPDM Register Summary: [12]

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Table 23-499. MCPDM_UP_DATA

Address Offset	0x0000 004C		
Physical Address	0x4903 204C 0x4013 204C 0x3 204C	**Instance**	MCPDM_L3 MCPDM_CORTEX-A9 MCPDM_DSP
Description	Uplink path data register.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UP_DATA																															

Bits	Field Name	Description	Type	Reset
31:0	UP_DATA	Uplink path data value	R	0x0000 0000

Table 23-500. Register Call Summary for Register MCPDM_UP_DATA

Multichannel PDM Controller

- Protocols and Data Formats in Status Mode: [0] [1]
- Uplink Path Description: [2] [3] [4] [5] [6] [7] [8] [9]
- McPDM Events Servicing: [10]
- McPDM Register Summary: [11]

Table 23-501. MCPDM_FIFO_CTRL_DN

Address Offset	0x0000 0050		
Physical Address	0x4903 2050 0x4013 2050 0x3 2050	**Instance**	MCPDM_L3 MCPDM_CORTEX-A9 MCPDM_DSP
Description	FIFO downlink control register.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												DN_TRESH			

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved	R	0x0000
3:0	DN_TRESH	FIFO downlink threshold value	RW	0x2

Table 23-502. Register Call Summary for Register MCPDM_FIFO_CTRL_DN

Multichannel PDM Controller

- McPDM Power Management: [0]
- Downlink Path Description: [1] [2]
- Global Initialization: [3]
- McPDM Register Summary: [4]

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Table 23-503. MCPDM_FIFO_CTRL_UP

Address Offset	0x0000 0054		
Physical Address	0x4903 2054 0x4013 2054 0x3 2054	**Instance**	MCPDM_L3 MCPDM_CORTEX-A9 MCPDM_DSP
Description	FIFO uplink control register.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												UP_TRESH			

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved	R	0x0000
3:0	UP_TRESH	FIFO uplink threshold value	RW	0x2

Table 23-504. Register Call Summary for Register MCPDM_FIFO_CTRL_UP

Multichannel PDM Controller

- McPDM Power Management: [0]
- Uplink Path Description: [1] [2] [3]
- Global Initialization: [4]
- McPDM Register Summary: [5]

Table 23-505. MCPDM_DN_OFFSET

Address Offset	0x0000 0058		
Physical Address	0x4903 2058 0x4013 2058 0x3 2058	**Instance**	MCPDM_L3 MCPDM_CORTEX-A9 MCPDM_DSP
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																		DN_OFST_RX2						DN_OFST_RX2_EN	RESERVED					DN_OFST_RX1					DN_OFST_RX1_EN

Bits	Field Name	Description	Type	Reset
31:14	RESERVED	Reserved	R	0x00000
13:9	DN_OFST_RX2	Offset value for the audio downlink channel 2	RW	0x00
8	DN_OFST_RX2_EN	Offset cancellation feature enabling/disabling bit for the audio downlink channel 2. 0x0: Offset cancellation disabled. 0x1: Offset cancellation enabled.	RW	0
7:6	RESERVED		R	0x0
5:1	DN_OFST_RX1	Offset value for the audio downlink channel 1	RW	0x00
0	DN_OFST_RX1_EN	Offset cancellation feature enabling/disabling bit for the audio downlink channel 1. 0x0: Offset cancellation disabled. 0x1: Offset cancellation enabled.	RW	0

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Table 23-506. Register Call Summary for Register MCPDM_DN_OFFSET

Multichannel PDM Controller

- Downlink Path Description: [0] [1] [2] [3]
- Global Initialization: [4] [5] [6] [7]
- McPDM Register Summary: [8]

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23.7 Digital Microphone Module

This section describes the digital microphone (DMIC) module.

23.7.1 DMIC Overview

The digital microphone (DMIC) module consists of an audio module dedicated to a mobile telephone terminal. The DMIC allows the support of up to six digital microphones. It provides an interface between the audio backend (ABE) module and microphones connected through the 6-wire DMIC serial interface.

The DMIC supports six paths. Because each path is composed of two digital microphone channels, the DMIC can be used with three stereo or six mono microphones. Each path is enabled or disabled independently.

The DMIC generates a pulse-density modulated (PDM) stream of bits and transfers it in one period or one half-period of the clock provided by the DMIC (oversampling clock).

Each microphone is directly connected to a filter decimator to extract the audio samples at the desired accuracy and sample rate. Data are stored in the first in first out (FIFO), which is controlled by interrupt request (IRQ) and direct memory access (DMA) request.

The DMIC pads are supplied with 1.8 V. These pads assure the transition to the host supply.

Figure 23-175 shows the DMIC in the device.

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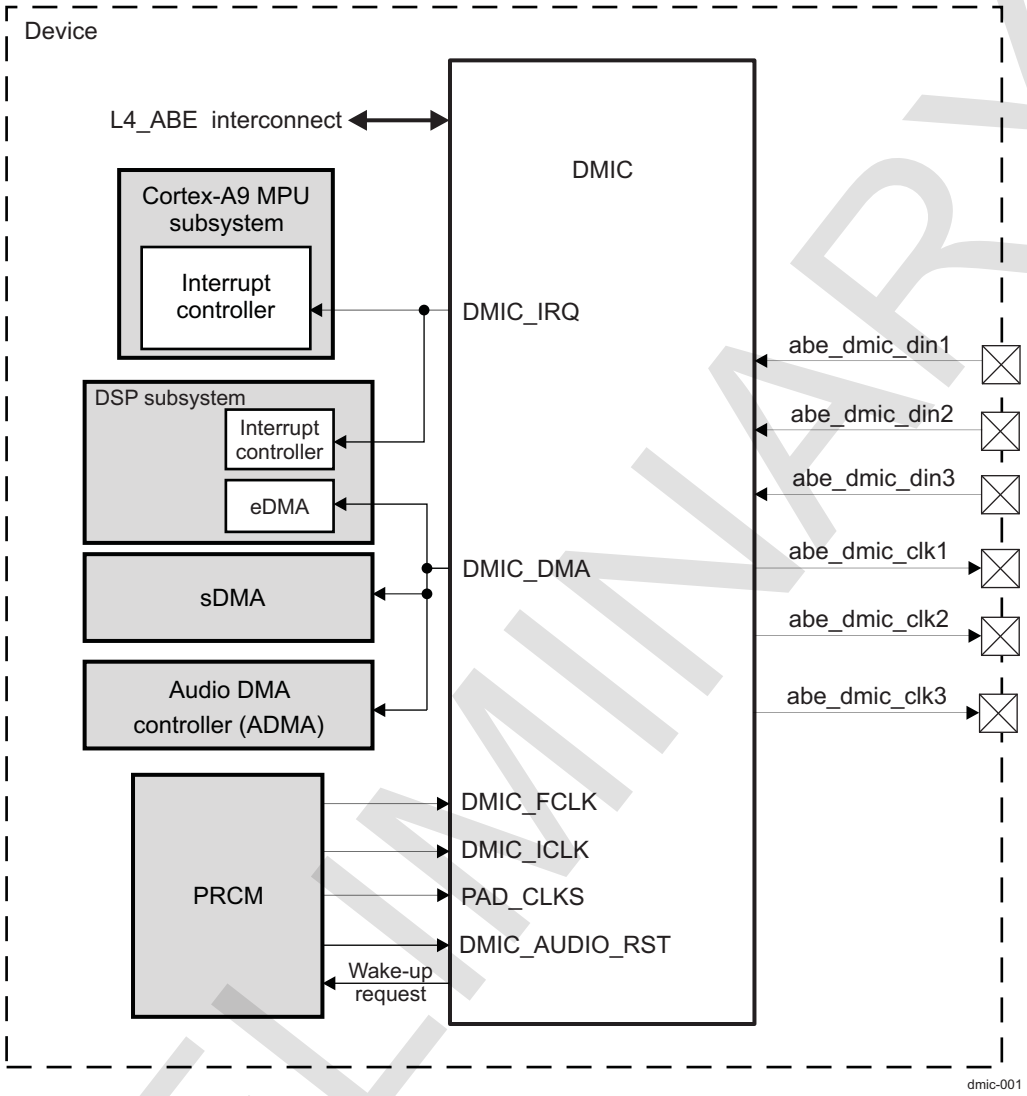
Figure 23-175. DMIC



The main features of the DMIC are:

- Six external pin connections (three data lines and three clock lines)
- Using the three clock lines, the DMIC delivers three clock signals (same frequency, individually gateable) for all digital microphones.
- Using the three data lines, the DMIC receives audio data from external microphones.
- Supports stereo (up to three) and mono (up to six) digital microphones
- Each line can support two microphones working in clock phase opposition.
- Selectable functional clock source
- Programmable output clock frequency (32 × FS, 50 × FS, 64 × FS, or 80 × FS, where FS = 48 kHz)
- Programmable data sampling sensibility (rising or falling edge)
- One RX FIFO (16 words of 144 bits)
- Supports idle request/acknowledge power, reset, and clock management (PRCM) module protocol
- Interconnect sample format: 32 bits (only 24 are significant)
- One IRQ to the microprocessor unit (Cortex ™-A9 microprocessor unit [MPU]) and digital signal processor (DSP) subsystems
- One DMA request capability on programmable FIFO threshold

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23.7.2 DMIC Environment

This section describes the DMIC application fields from an environment point of view (that is, external connections). It presents the DMIC connectivity options, lists possible interfaces, and details the protocol and data format used in each case.

23.7.2.1 DMIC Interface With External MIC

23.7.2.1.1 DMIC Interface Overview

The DMIC interface is a 6-wire interface. The DMIC module can support up to three external stereo and six mono digital microphones. A DMIC is an external module that can deliver data. A clock is sent from the host to the microphone.

Figure 23-176 and Figure 23-177 show two cases of use of the DMIC, but all configurations are possible with stereo and mono digital microphones. The output of the DMIC is in 32-bit format.

Figure 23-176 shows the DMIC used with three stereo DMICs.

Figure 23-176. DMIC With Three Stereo DMICs

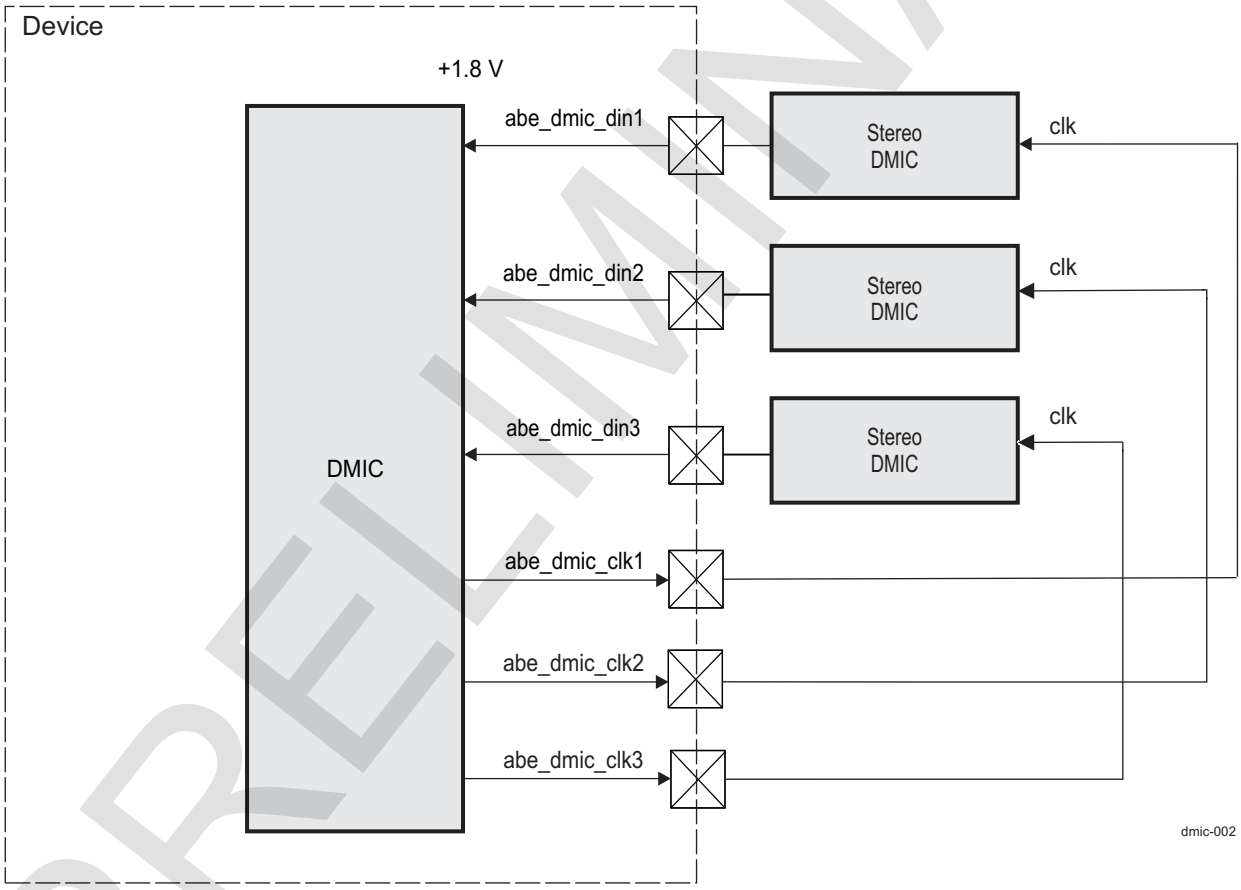

Figure 23-177 shows the DMIC used with six mono DMICs.

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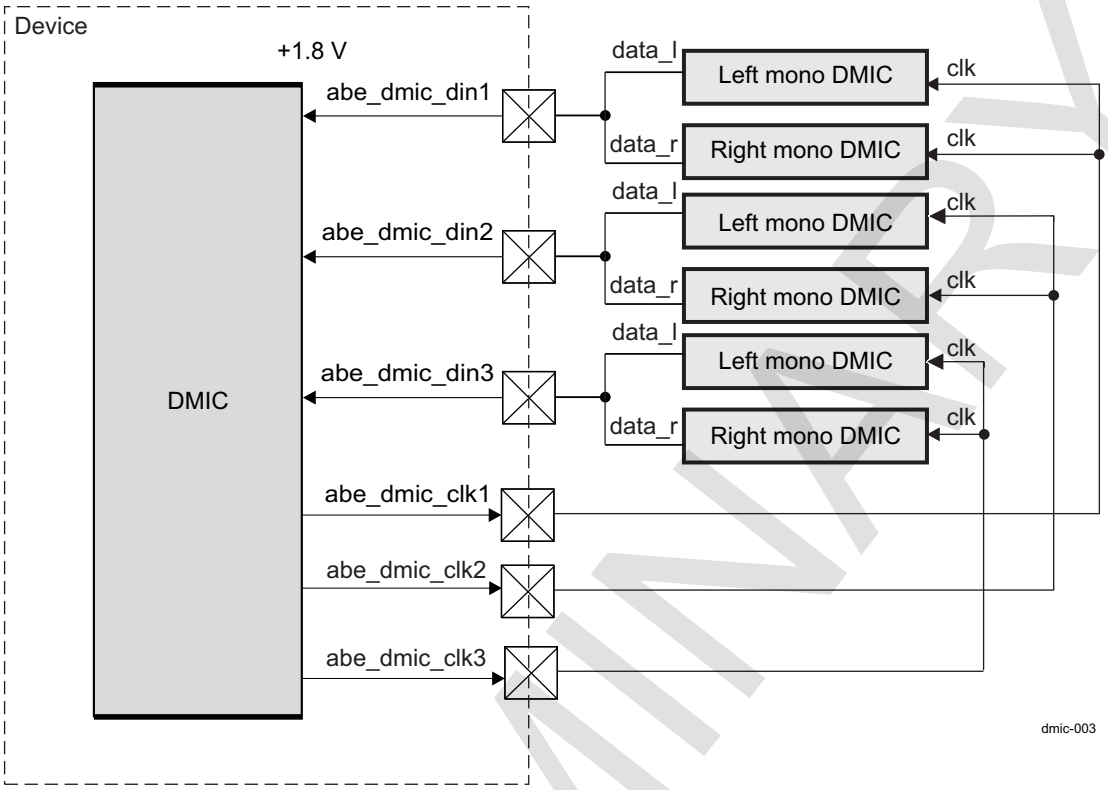
Figure 23-177. DMIC With Six Mono DMICs



23.7.2.1.2 DMIC Signals

Table 23-507 describes the signals in the DMIC module.

Table 23-507. Input/Output

Signal Name	I/O [1]	Description	Reset Value [1]
abe_dmic_clk1	O	Digital (stereo) microphone clock output 1	0
abe_dmic_clk2	O	Digital (stereo) microphone clock output 2	0
abe_dmic_clk3	O	Digital (stereo) microphone clock output 3	0
abe_dmic_din1	I	Digital (stereo) microphone data input 1	Hi-Z
abe_dmic_din2	I	Digital (stereo) microphone data input 2	Hi-Z
abe_dmic_din3	I	Digital (stereo) microphone data input 3	Hi-Z

(1) I = Input; O = Output; Hi-Z = High impedance

All DMIC external connections have pullup or pulldown resistors, selected and configured in the control module registers.

23.7.2.1.3 Serial Data Format

The DMIC generates a PDM stream of bits and transfers it in one period or one half-period of the clock. Then, the filter decimator extracts the 24-bit audio samples.

23.7.2.1.3.1 DMIC Clock Generation and Synchronization

When DMIC_POLAR is set to 0, the microphone left data is generated on the abe_dmic_clk low level. When DMIC_POLAR is set to 1, the microphone left data is generated on the abe_dmic_clk high level. There are three DMIC_POLARx bits (where x = 1, 2, or 3) corresponding to the three stereo paths:

- DMIC_CTRL[4] for path 1

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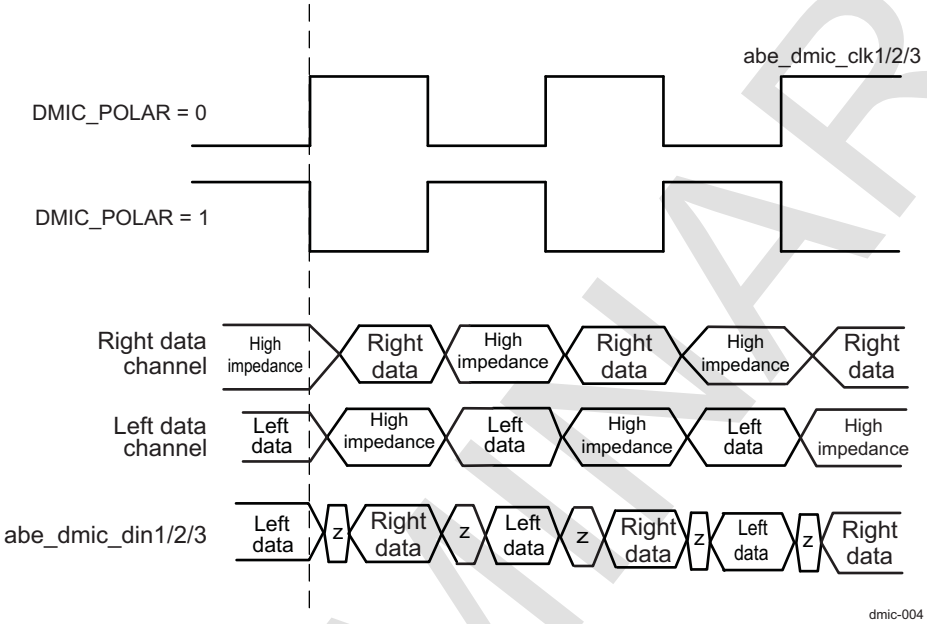
- DMIC_CTRL[5] for path 2
- DMIC_CTRL[6] for path 3

The DMIC_POLARx bits are set depending on the configuration of the external digital microphone.

Figure 23-178 is a diagram of the DMIC interface with a DMIC.

Figure 23-178. DMIC Interface Diagram With External DMICs



23.7.2.2 DMIC Functional Path

The DMIC path processes, decimates, and filters the data from the DMIC interface, and stores the processed data in the FIFO. The FIFO is controlled by IRQ and DMA requests and is fed outside of the DMIC.

For more information about microphone data processing, see Section 23.7.4.7, *Audio Data Processing*.

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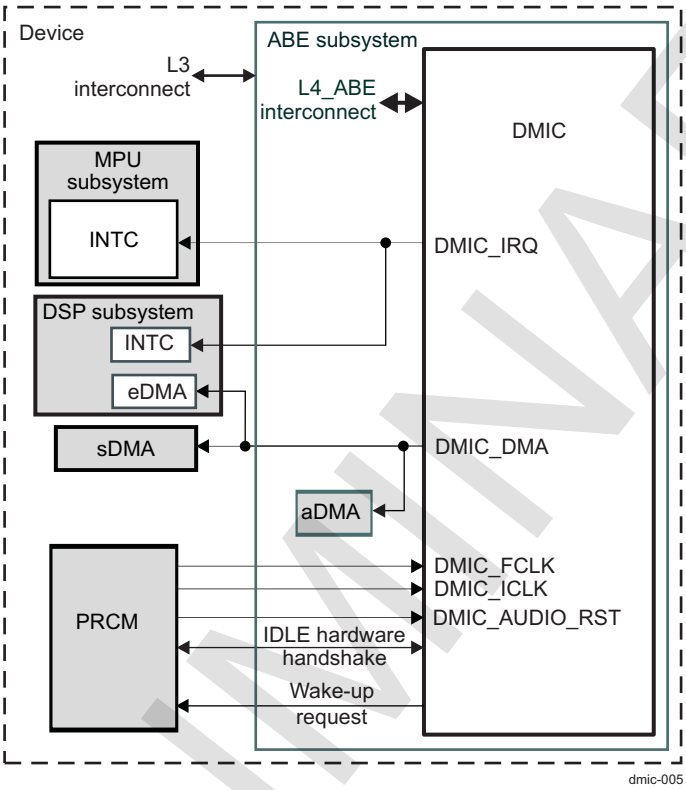
23.7.3 DMIC Integration

This section describes the integration of the DMIC in the device, and includes information about clocks, resets, and hardware requests.

Figure 23-179 shows the DMIC integration.

Figure 23-179. DMIC Integration



NOTE: For more information about the IDLE hardware handshake and the wake-up request, see Section 3.1.1.1.2, *Module Level Clock Management*, in Chapter 3, *Power, Reset, and Clock Management*.

The DMIC integration includes:

- One functional clock
- One interface clock
- One IRQ
- One sDMA/aDMA/eDMA request
- IDLE hardware handshake
- Wake-up request

Table 23-508 through Table 23-510 summarize the integration of the module in the device.

Table 23-508. Integration Attributes

Module Instance	Attributes		
	Power Domain	Wake-Up Capability	Interconnect
DMIC	PD_AUDIO	Yes	L4_ABE

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Table 23-509. Clocks and Resets

Clocks				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
DMIC	DMIC_ICLK	ABE_ICLK2	PRCM	Interface clock
	DMIC_FCLK	DMIC_ABE_FCLK	PRCM	Functional clock
Resets				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
DMIC	DMIC_AUDIO_RST	AUDIO_RST	PRCM	Module hardware reset, nonretention

Table 23-510. Hardware Requests

Interrupt Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
DMIC	DMIC_IRQ	D_IRQ_83	DSP	DMIC interrupt to the DSP subsystem
	DMIC_IRQ	MA_IRQ_114	Cortex™-A9 MPU	DMIC interrupt to the Cortex-A9 MPU subsystem
DMA Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
DMIC	DMIC_DMA	S_DMA_66	sDMA	DMA request to the system DMA (sDMA)
	DMIC_DMA	A_DMA_1	aDMA	DMA request to the audio DMA (aDMA)
	DMIC_DMA	D_DMA_44	eDMA	DMA request to the DSP DMA (eDMA)

NOTE:

- For a description of the interrupt source, see Section 23.7.4.5, *Interrupt Requests*.
- For a description of the DMA source, see Section 23.7.4.6, *DMA Requests*.
- For information about PRCM clock gating and management and PRCM reset sources and distribution, see Section 3.1.1.2.1, *Power Domain*, in Chapter 3, *Power, Reset, and Clock Management*.

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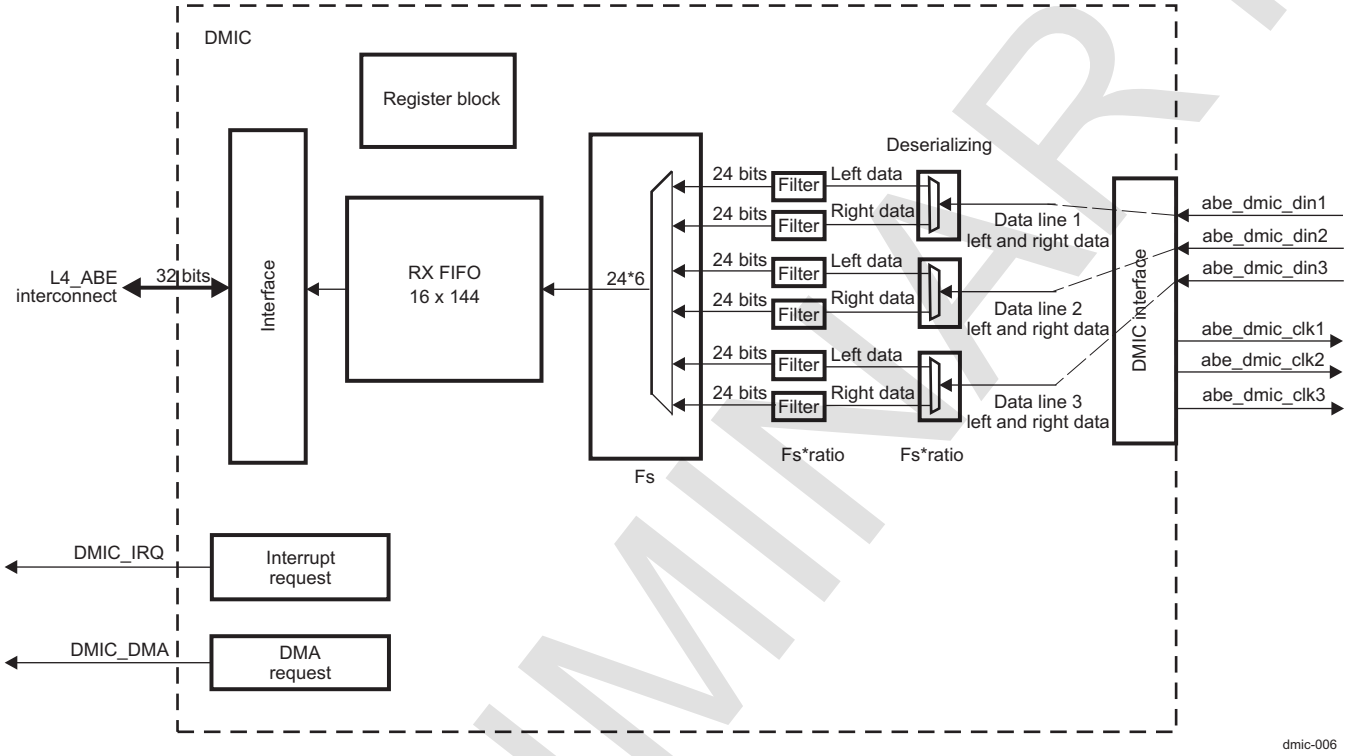
23.7.4 DMIC Functional Description

23.7.4.1 Block Diagram

Figure 23-180 is the DMIC block diagram.

Figure 23-180. DMIC Block Diagram

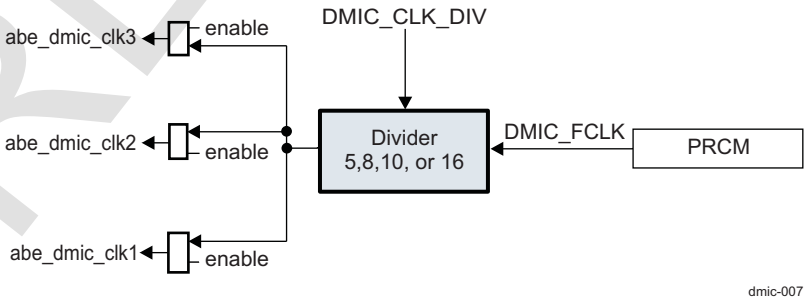


23.7.4.2 DMIC Clock Configuration

The DMIC operates from one interface clock to interface with the L4-ABE interconnect and one selectable (among three) functional clock. These clocks are provided by the PRCM module. For the interface clock, request and acknowledge are set up between the PRCM module and the DMIC.

Figure 23-181 shows the DMIC clock selection.

Figure 23-181. DMIC Clock Selection



DMIC_FCLK is the source clock signal. Several source clocks are available and are selected according to the configuration of the DMIC_CTRL[9:7] DMIC_CLK_DIV bit field. For more information about

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DMIC_FCLK selection, see Figure 23-181. abe_dmic_clkx are the output clocks generated in the DMIC and are fed to the external microphones. They are also the internal clocks of the external microphones. The performance in terms of signal-to-noise ratio (SNR) depends on these clocks. Users must take care about the value of abe_dmic_clkx (the analog-to-digital converter [ADC] clock) when selecting the source clock (DMIC_FCLK). Table 23-511 describes the abe_dmic_clkx generation.

Table 23-511. abe_dmic_clkx Generation

DMIC_FCLK	DMIC_ CLK_DIV	DMIC_FCLK/ abe_dmic_clk	abe_dmic_clk = ADC Clock	Ratio = abe_dmic_clk/FS = 48 kHz
19.2 MHz	000	8	2.4 MHz	50
	001	5	3.84 MHz	80
24 MHz	010	10	2.4 MHz	50
24.576 MHz	011	8	3.072 MHz	64
	100	16	1.536 MHz	32
12 MHz	101	5	2.4 MHz	50

The maximum clock on the interface is 3.84 MHz, with a source clock of 19.2 MHz.

23.7.4.3 DMIC Software Reset

Table 23-512 lists the different types of software reset available at the module level.

Table 23-512. Reset Description

Type	Name	Source	Description
Software	DMIC_SYSCONFIG[1] SOFTRESET	–	Module software reset
Software	DMIC_CTRL[10] SW_DMIC_RST	–	Reset-enabled DMIC paths

The software path reset is gated by:

- DMIC_CTRL[0] DMIC_UP1_EN for path 1
- DMIC_CTRL[1] DMIC_UP2_EN for path 2
- DMIC_CTRL[2] DMIC_UP3_EN for path 3
- DMIC_CTRL[10] SW_DMIC_RST

When the DMIC_CTRL[10] SW_DMIC_RST bit is set to 1, the corresponding enabled DMIC paths are reset. Resets are cleared by writing 0.

NOTE: A software reset is required to change the configuration of enabled paths; for example, to disable path 3, a software reset of path 3 is mandatory for the change to be considered.

A module software reset can be performed by setting the DMIC_SYSCONFIG[1] SOFTRESET bit. This action starts a soft reset sequence.

The software reset status of the module can be checked by reading the DMIC_SYSCONFIG[0] SOFTRESET bit (0: reset is done; 1: reset is ongoing).

23.7.4.4 DMIC Power Management

Table 23-513 describes the power-management features available for the DMIC.

Table 23-513. Local Power-Management Features

Feature	Registers	Description
Clock autogating	N/A	Feature not available
Slave idle modes	DMIC_SYSCONFIG[3:2] SIDLEMODE	Force-idle, no-idle, smart-idle, and smart-idle wakeup capable modes are available.
Clock activity	N/A	Feature not available

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Table 23-513. Local Power-Management Features (continued)

Feature	Registers	Description
Master standby modes	N/A	Feature not available
Global wake-up enable	N/A	Feature not available
Wake-up sources enable	DMIC_IRQWAKEEN[0] IRQ_WAKEUP_EN DMIC_DMAWAKEEN[0] DMA_WAKEUP_EN	This register holds one active-high enable bit per event source that can generate a wake-up signal.

23.7.4.5 DMIC Interrupt Requests

Table 23-514 lists the event flags, and their mask, that can cause module interrupts.

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Table 23-514. Interrupt Events

Nonmaskable Event Flag [(1)]	Maskable Event Flag	Event Mask Bit	Event Unmask Bit	Description
DMIC_IRQSTATUS_RAW[3] DMIC_IRQ_EMPTY	DMIC_IRQSTATUS[3] DMIC_IRQ_EMPTY	DMIC_IRQENABLE_CLR[3] DMIC_IRQ_EMPTY_MASK	DMIC_IRQENABLE_SET[3] DMIC_IRQ_EMPTY_MASK	FIFO empty event. This event occurs when the FIFO is already empty and a new word is read from the FIFO by software.
DMIC_IRQSTATUS_RAW[2] DMIC_IRQ_ALST_FULL	DMIC_IRQSTATUS[2] DMIC_IRQ_ALST_FULL	DMIC_IRQENABLE_CLR[2] DMIC_IRQ_ALST_FULL_MASK	DMIC_IRQENABLE_SET[2] DMIC_IRQ_ALST_FULL_MASK	FIFO almost-full event. This event occurs when the FIFO contains (FIFO size – 1) words and a new word is written to the FIFO.
DMIC_IRQSTATUS_RAW[1] DMIC_IRQ_FULL	DMIC_IRQSTATUS[1] DMIC_IRQ_FULL	DMIC_IRQENABLE_CLR[1] DMIC_IRQ_FULL_MASK	DMIC_IRQENABLE_SET[1] DMIC_IRQ_FULL_MASK	FIFO full event. This event occurs when the FIFO is already full and a new word is written to the FIFO.
DMIC_IRQSTATUS_RAW[0] DMIC_IRQ	DMIC_IRQSTATUS[0] DMIC_IRQ	DMIC_IRQENABLE_CLR[0] DMIC_IRQ_MASK	DMIC_IRQENABLE_SET[0] DMIC_IRQ_MASK	FIFO read request event. This event occurs when the number of words stored in the FIFO is equal to or greater than the FIFO threshold.

(1) The DMIC_IRQSTATUS_RAW register is used primarily for debug purposes.

The interrupt line is asserted (active high) when one of the following signals appears:

- DMIC_IRQ_EMPTY
- DMIC_IRQ_ALST_FULL
- DMIC_IRQ_FULL
- DMIC_IRQ

Read the DMIC_IRQSTATUS register to determine which event occurs.

CAUTION

Interrupt lines must be cleared by software. Write 1 in the DMIC_IRQSTATUS register to clear the corresponding event.

An event can generate an IRQ when the corresponding mask bit in the DMIC_IRQENABLE_SET register is set to 1. Events are register bits that belong to the DMIC_IRQSTATUS and DMIC_IRQSTATUS_RAW registers (the same register accessed by two interconnect addresses). In the case of the DMIC_IRQSTATUS_RAW register, status event is set even if it is not enabled (used primarily for debug purposes). The DMIC_IRQSTATUS register is set by writing 1 to the DMIC_IRQSTATUS_RAW register.

Each internal interrupt signal can be masked by enabling the corresponding mask in the DMIC_IRQENABLE_SET register or disabling it in the DMIC_IRQENABLE_CLR register. This mechanism is defined in Section 23.7.6, *DMIC Register Manual*.

Figure 23-182 shows the interrupt tree with the event generated and the mask that enables or disables the event. All events are summarized to give the single interrupt generation.

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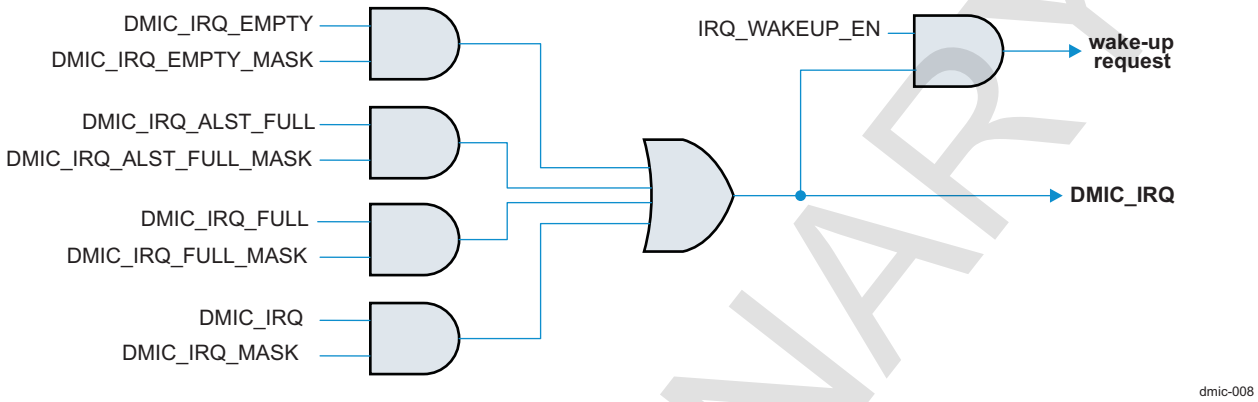
Figure 23-182. Interrupt Tree



23.7.4.6 DMIC DMA Requests

The DMIC can generate one DMA request to the sDMA, aDMA, and eDMA controllers (see Table 23-515).

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Table 23-515. DMIC DMA Request

Name	Description	Enable DMA Bit	Disable DMA Bit
DMIC_DMA_ENABLE	Data ready in FIFO (threshold is reached)	DMIC_DMAENABLE_SET[0] DMA_ENABLE	DMIC_DMAENABLE_CLR[0] DMA_ENABLE

The DMA lines can be enabled or disabled depending on the value of the bits in the DMIC_DMAENABLE_SET and DMIC_DMAENABLE_CLR registers.

A DMA request is sent when data is ready in the FIFO. This request is used only to notify the host that data are ready in the FIFO.

23.7.4.7 Audio Data Processing

The DMIC supports six audio paths and can be used with three stereo or six mono microphones. Each path is independent and is enabled or disabled by using the following bits:

- DMIC_CTRL[0] DMIC_UP1_EN
- DMIC_CTRL[1] DMIC_UP2_EN
- DMIC_CTRL[2] DMIC_UP3_EN

23.7.4.7.1 Filtering

The external DMIC generates a PDM stream of bits and transfers it in one period or one half-period of the clock provided by the DMIC inside the device. The aim of the DMIC audio path is to process data from the DMIC interface, decimate and filter the data, and store the processed data in the FIFO.

The format of the DMIC data is 24 bits (the transfer format is 32 bits long). The following bits allow switching the polarity of the interface:

- DMIC_CTRL[4] DMIC_POLAR1
- DMIC_CTRL[5] DMIC_POLAR2
- DMIC_CTRL[6] DMIC_POLAR3

For more information, see Section 23.7.2.1.3.1, *DMIC Clock Generation and Synchronization*.

Processed data from the DMIC interface are stored in the FIFO. The FIFO is controlled by the IRQ and DMA request and externally fed by the DMIC using the following interconnect format.

The three uplink paths are identical. Each uplink path is composed of a left and a right channel. The DMIC interface delivers six parallel data of 1 bit (3 × 2 paths of stereo data that can be used at six mono paths). Each bit goes to a filter. The aim of the filter is to limit the noise and perform decimation by factor D. Factor D depends on the DMIC_CLK_DIV register bits, as described in the ratio defined in Table 23-511. The filters are sinc filter order 4. They are chosen with regard to the nature of the analog converter.

The format of the filter output is 24 bits.

23.7.4.8 FIFO Management

The DMIC implements an internal FIFO controlled by IRQ and DMA request. The host must read words in the FIFO. The interrupt line is used not only to inform the host that data are ready in the FIFO, but also to warn the host about events that can occur, such as FIFO full, almost full, or empty. A DMA request is used only to inform the host that data are ready in the FIFO.

23.7.4.8.1 FIFO General Description

The DMIC communicates with the host through L4-ABE interconnect access. DMIC audio data coming from external microphones are stored in the FIFO. The DMIC FIFO allows the exchange of information between the DMIC and the host. Each audio data is 24 bits long. The DMIC FIFO contains 16 words. Each word is the combination of six audio data (24 × 6 = 144 bits) coming from the interface. The FIFO is controlled by interrupt lines and DMA requests. For more information about IRQs and DMA controls, see Section 23.7.4.5, *DMIC Interrupt Requests*, and Section 23.7.4.6, *DMIC DMA Requests*.

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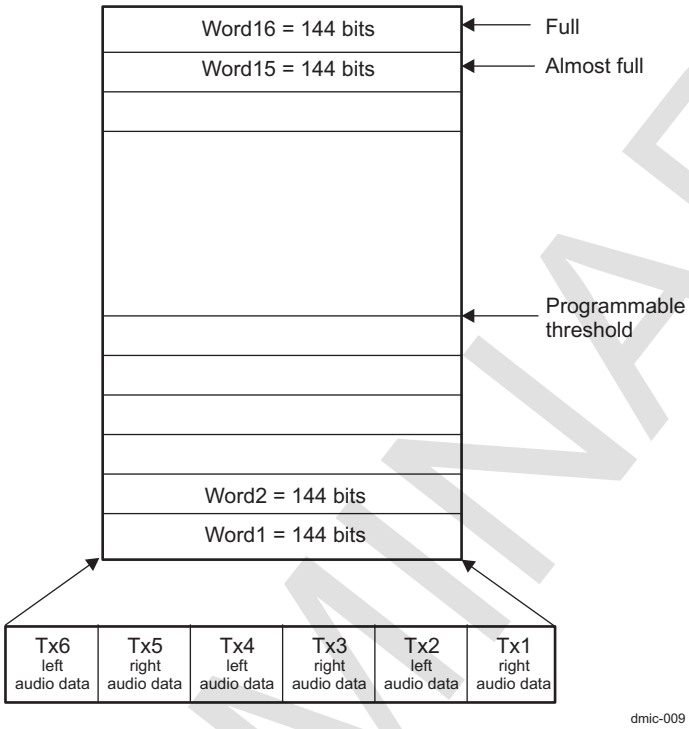
FIFO write access is done in the functional clock domain, and read access is done in the interface clock domain.

Figure 23-183 is an overview of the DMIC FIFO.

Figure 23-183. DMIC FIFO



23.7.4.8.2 FIFO Operations

Audio data are filled in the FIFO from DMIC internal filters. The host must read words in the FIFO. The number of reads depends on the application that is configured by the following bits:

- DMIC_CTRL[0] DMIC_UP1_EN
- DMIC_CTRL[2] DMIC_UP3_EN
- DMIC_CTRL[1] DMIC_UP2_EN
- DMIC_FIFO_CTRL[3:0] DMIC_TRESH (FIFO threshold)

If only uplink path 2 and path 3 are enabled, for example, the Tx1 and Tx2 words are left and right data for path 2, and Tx3 and Tx4 are left and right data for path 3.

When the FIFO threshold is reached, and depending on conditions, an event is sent to the DMA handler. The host must read the exact number of words in the FIFO.

Two accesses are required to read a complete stereo audio path.

The number of read accesses from the host is determined by the following equation:

Num_rd_access = (DMIC_UP1_EN + DMIC_UP2_EN + DMIC_UP3_EN) × 2 × (DMIC_TRESH)

The FIFO threshold is programmed through the DMIC_FIFO_CTRL[3:0] DMIC_TRESH bit field.

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NOTE: If DMIC_TRESH = 1, the host is expected to perform 1 × (DMIC_UP1_EN + DMIC_UP2_EN + DMIC_UP3_EN) × 2 read access every 96 kHz (2 × FS).

If DMIC_TRESH = 2, the host is expected to perform (DMIC_UP1_EN + DMIC_UP2_EN + DMIC_UP3_EN) × 4 read access every 48 kHz (FS).

If DMIC_TRESH = 12, the host is expected to perform (DMIC_UP1_EN + DMIC_UP2_EN + DMIC_UP3_EN) × 12 access every 8 kHz (FS/6).

23.7.4.8.3 FIFO Output Range Definition

The DMIC_CTRL[3] DMICOUTFORMAT bit allows determining the format of the output of the DMIC uplink module.

When DMICOUTFORMAT = 0, the data going from the FIFO are left-shifted by 8 bits. When DMICOUTFORMAT = 1, the data are signed-extended on 32 bits.

The DMIC uplink modules process audio data based on twos complement format.

NOTE: When DMICOUTFORMAT = 0, the maximum positive swing analog voltage corresponds to a final DMIC output of 0x7FFF FF00. The maximum negative swing analog voltage corresponds to a final DMIC output of 0x8000 0000.

When DMICOUTFORMAT = 1, the sign is extended: The maximum positive swing analog voltage corresponds to a final DMIC output of 0x007F FFFF. The maximum negative swing analog voltage corresponds to a final DMIC output of 0xFF80 0000.

Reading the value of the corresponding audio data in the FIFO requires access to the DMIC_DATA_REG register. The first access gives the value of Tx1 right data, the second gives the value of Tx2 left data, up to Tx6 (the left audio data of the last audio path). If the path is disabled, 0x0 is read. All data are duplicated (for debug purposes) in their corresponding left or right data registers. Table 23-516 describes the audio data path registers.

Table 23-516. Audio Data Path Registers

Stereo Audio Path	Mono Audio Path	Data Register
Right path 1	Mono path 1	DMIC_FIFO_DMIC1R_DATA[23:0]
Left path 1	Mono path 2	DMIC_FIFO_DMIC1L_DATA[23:0]
Right path 2	Mono path 3	DMIC_FIFO_DMIC2R_DATA[23:0]
Left path 2	Mono path 4	DMIC_FIFO_DMIC2L_DATA[23:0]
Right path 3	Mono path 5	DMIC_FIFO_DMIC3R_DATA[23:0]
Left path 3	Mono path 6	DMIC_FIFO_DMIC3L_DATA[23:0]

The output of the DMIC path for interconnect access is in 32-bit format.

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23.7.5 DMIC Programming Guide

23.7.5.1 DMIC Low-Level Programming Models

This section describes the low-level hardware programming sequences for the configuration and use of the module.

23.7.5.1.1 Global Initialization

23.7.5.1.1.1 Surrounding Modules Global Initialization

This section identifies the requirements for initializing the surrounding modules when the DMIC is used for the first time after a device reset. This initialization of surrounding modules is based on the integration and environment of the DMIC. For more information, see Section 23.7.3, *DMIC Integration* and Section 23.7.2, *DMIC Environment*.

Table 23-517 describes the global initialization of surrounding modules.

Table 23-517. Global Initialization of Surrounding Modules

Surrounding Modules	Comments
PRCM	Module interface and functional clocks must be enabled. See Chapter 3, *Power, Reset, and Clock Management*.
Control module	Module-specific pad muxing must be set in the control module. See Chapter 18, *Control Module*.
(optional) Cortex-A9 MPU interrupt controller (INTC) (or DSP INTC)	INTC configuration must be done to enable the interrupts from the DMIC. See Chapter 17, *Interrupt Controllers*.
(optional) sDMA (or eDMA or aDMA)	DMA configuration must be done to enable the DMIC DMA channel requests.
(optional) Interconnect	For more information about the interconnect configuration, see Chapter 13, *Interconnect*.

NOTE: The INTC and DMA configurations are necessary if the interrupt and DMA-based communication modes are used.

23.7.5.1.1.2 DMIC Global Initialization

23.7.5.1.1.2.1 Main Sequence – DMIC Global Initialization

The procedure in Table 23-518 initializes the DMIC after a power-on reset (POR).

Table 23-518. DMIC Global Initialization

Step	Register/Bit Field/Programming Model	Value
Execute a software reset.	DMIC_SYSCONFIG[0] SOFTRESET	0x1
Wait for the software reset completion by polling.	DMIC_SYSCONFIG[0] SOFTRESET	==0x0
Configure the local power management.	DMIC_SYSCONFIG[3:2] SIDLEMODE	0x-
Select the DMIC FIFO threshold.	DMIC_FIFO_CTRL[3:0] DMIC_TRESH	0x-
Select the DMIC output clock frequency.	DMIC_CTRL[9:7] DMIC_CLK_DIV	0x-
Select the DMIC FIFO data output format.	DMIC_CTRL[3] DMICOUTFORMAT	0x-
Select the level (high or low) of the clock signal abe_dmic_clki when the left data is to be generated (extracted) from the external microphone i (where i = 1 to 3).	DMIC_CTRL[j] DMIC_POLARi (where j = 4 to 6, and i = 1 to 3)	0x-
Enable audio path i (where i = 1 to 3).	DMIC_CTRL[k] DMIC_POLARi (where k = 0 to 2, and i = 1 to 3)	0x1

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23.7.5.1.2 Operational Mode Configuration

23.7.5.1.2.1 DMIC Polling Mode

Figure 23-184 shows the polling mode. Table 23-519 summarizes the register call for the polling mode. For the number of read accesses used while reading the received audio data, see Section 23.7.4.8, *FIFO Management*.

Figure 23-184. Polling Mode

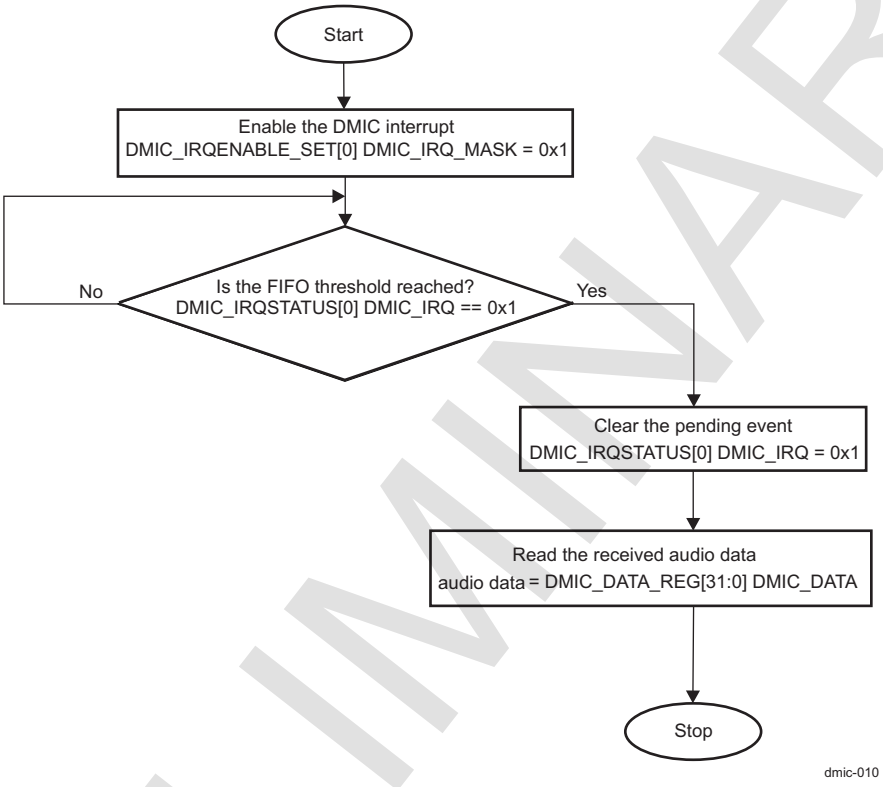

Table 23-519. Register Call Summary for Polling Mode

Register Name	Register Name	Register Name
DMIC_IRQENABLE_SET	DMIC_IRQSTATUS	DMIC_DATA_REG

23.7.5.1.2.2 DMIC Interrupt Mode

Table 23-520 lists the procedure to initialize interrupt mode.

Table 23-520. Interrupt Mode

Step	Register/Bit Field/Programming Model	Value
Enable the DMIC interrupts.	DMIC_IRQENABLE_SET[3:0]	0xF

23.7.5.1.2.3 DMIC DMA Mode

Table 23-521 lists the procedure to initialize DMA mode.

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Table 23-521. DMA Mode

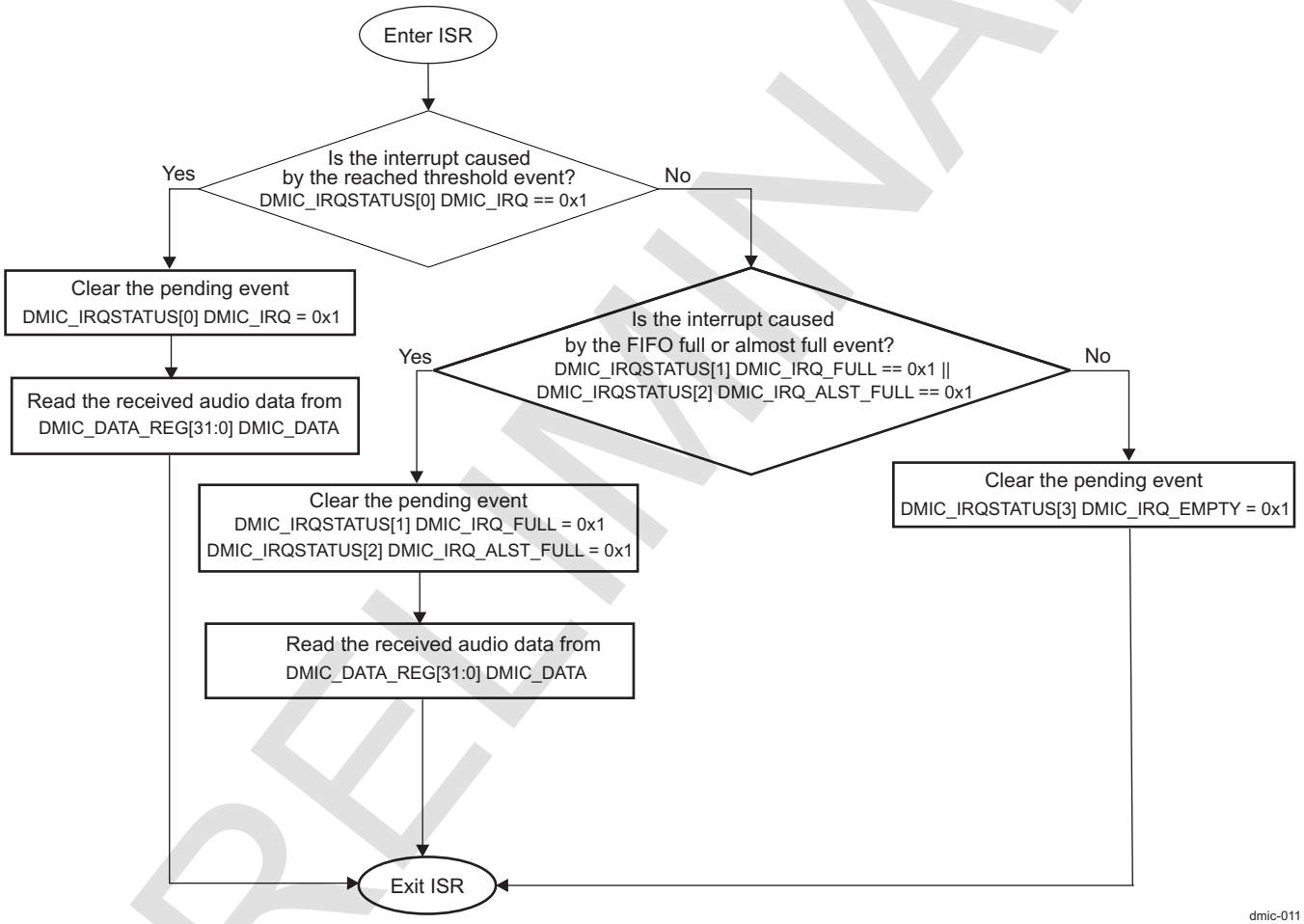
Step	Register/Bit Field/Programming Model	Value
Enable the DMIC DMA interrupt event.	DMIC_DMAENABLE_SET[0] DMA_ENABLE	0x1

23.7.5.1.3 DMIC Events Servicing

23.7.5.1.3.1 DMIC Interrupt Servicing

This section describes the interrupt event servicing of the module. Figure 23-185 shows the interrupt handler.

Figure 23-185. Interrupt Handler



When the interrupt is caused by the reached threshold event, for the number of read accesses used while reading the received audio data, see Section 23.7.4.8, *FIFO Management*.

When the interrupt is caused by a FIFO full or almost-full event, software must read all the available data in the FIFO. If a FIFO full event occurred, the number of read accesses must be the maximum:

Num_rd_access = (DMIC_UP1_EN + DMIC_UP2_EN + DMIC_UP3_EN) × 2 × 15

If a FIFO almost-full event occurred, the number of read accesses must be:

Num_rd_access = (DMIC_UP1_EN + DMIC_UP2_EN + DMIC_UP3_EN) × 2 × 14

Table 23-522 summarizes the register call for the interrupt handler.

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Table 23-522. Register Call Summary for the Interrupt Handler

Register Name	Register Name
DMIC_IRQSTATUS	DMIC_DATA_REG

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23.7.6 DMIC Register Manual

23.7.6.1 DMIC Instance Summary

Table 23-523 is the DMIC instance summary.

Table 23-523. DMIC Instance Summary

Module Name	Base Address L3 Interconnect	Base Address Cortex-A9 Private Access	Base Address DSP Private Access	Size
DMIC	0x4902 E000	0x4012 E000	0x2 E000	4KB

NOTE: Private access is an access that does not use the L3/L4 interconnects.

23.7.6.2 DMIC Registers

23.7.6.2.1 DMIC Register Summary

Table 23-524 summarizes the DMIC register mapping.

Table 23-524. DMIC Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	Physical Address L3 Interconnect	Physical Address Cortex-A9 Private Access	Physical Address DSP Private Access
DMIC_REVISION	R	32	0x0000 0000	0x4902 E000	0x4012 E000	0x2 E000
DMIC_SYSCONFIG	RW	32	0x0000 0010	0x4902 E010	0x4012 E010	0x2 E010
RESERVED	RW	32	0x0000 0020	0x4902 E020	0x4012 E020	0x2 E020
DMIC_IRQSTATUS_RAW	RW	32	0x0000 0024	0x4902 E024	0x4012 E024	0x2 E024
DMIC_IRQSTATUS	RW	32	0x0000 0028	0x4902 E028	0x4012 E028	0x2 E028
DMIC_IRQENABLE_SET	RW	32	0x0000 002C	0x4902 E02C	0x4012 E02C	0x2 E02C
DMIC_IRQENABLE_CLR	RW	32	0x0000 0030	0x4902 E030	0x4012 E030	0x2 E030
DMIC_IRQWAKEEN	RW	32	0x0000 0034	0x4902 E034	0x4012 E034	0x2 E034
DMIC_DMAENABLE_SET	RW	32	0x0000 0038	0x4902 E038	0x4012 E038	0x2 E038
DMIC_DMAENABLE_CLR	RW	32	0x0000 003C	0x4902 E03C	0x4012 E03C	0x2 E03C
DMIC_DMAWAKEEN	RW	32	0x0000 0040	0x4902 E040	0x4012 E040	0x2 E040
DMIC_CTRL	RW	32	0x0000 0044	0x4902 E044	0x4012 E044	0x2 E044
DMIC_DATA_REG	R	32	0x0000 0048	0x4902 E048	0x4012 E048	0x2 E048
DMIC_FIFO_CTRL	RW	32	0x0000 004C	0x4902 E04C	0x4012 E04C	0x2 E04C
DMIC_FIFO_DMIC1R_DATA	R	32	0x0000 0050	0x4902 E050	0x4012 E050	0x2 E050
DMIC_FIFO_DMIC1L_DATA	R	32	0x0000 0054	0x4902 E054	0x4012 E054	0x2 E054
DMIC_FIFO_DMIC2R_DATA	R	32	0x0000 0058	0x4902 E058	0x4012 E058	0x2 E058
DMIC_FIFO_DMIC2L_DATA	R	32	0x0000 005C	0x4902 E05C	0x4012 E05C	0x2 E05C
DMIC_FIFO_DMIC3R_DATA	R	32	0x0000 0060	0x4902 E060	0x4012 E060	0x2 E060
DMIC_FIFO_DMIC3L_DATA	R	32	0x0000 0064	0x4902 E064	0x4012 E064	0x2 E064

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23.7.6.2.2 DMIC Register Descriptions

through describe the DMIC registers.

Table 23-525. DMIC_REVISION

Address Offset	0x0000 0000		
Physical Address	0x4902 E000 0x4012 E000 0x2 E000	**Instance**	DMIC_L3 DMIC_CORTEX-A9 DMIC_DSP
Description	IP Revision Identifier (X.Y.R) used by software to track features, bugs, and compatibility		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP revision	R	See(1).

(1) TI internal data

Table 23-526. Register Call Summary for Register DMIC_REVISION

Digital Microphone Module
- DMIC Register Summary: [0]

Table 23-527. DMIC_SYSCONFIG

Address Offset	0x0000 0010		
Physical Address	0x4902 E010 0x4012 E010 0x2 E010	**Instance**	DMIC_L3 DMIC_CORTEX-A9 DMIC_DSP
Description	This register allows controlling various parameters of the DMIC interface.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												SIDLEMODE		FREEMU	SOFTRESET

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved	R	0x0000000
3:2	SIDLEMODE	Configuration of the local target state management (idlereq/idleack control) 0x0: Force-idle. IDLE request is acknowledged unconditionally and immediately. 0x1: No-idle. IDLE request is never acknowledged. 0x2: Smart-idle. The acknowledgment to an IDLE request is given based on the internal activity. 0x3: Smart-idle wakeup capable mode	RW	0x2
1	FREEMU	Sensitivity to emulation (debug) suspend input signal 0x0: IP module is sensitive to emulation suspend. 0x1: IP module is not sensitive to emulation suspend.	RW	0

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Bits	Field Name	Description	Type	Reset
0	SOFTRESET	Module software reset. The bit is automatically reset by the hardware. It has same effect as the main hardware reset. Write 0x0: No action Read 0x0: Reset done, no pending action Read 0x1: Reset (software or other) ongoing Write 0x1: Initiate software reset.	RW	0

Table 23-528. Register Call Summary for Register DMIC_SYSCONFIG

Digital Microphone Module
- DMIC Software Reset: [0] [1] [2]
- DMIC Power Management: [3]
- Global Initialization: [4] [5] [6]
- DMIC Register Summary: [7]

Table 23-529. DMIC_IRQSTATUS_RAW

Address Offset	0x0000 0024		
Physical Address	0x4902 E024 0x4012 E024 0x2 E024	**Instance**	DMIC_L3 DMIC_CORTEX-A9 DMIC_DSP
Description	Component (that is, main) interrupt request status. Check the corresponding secondary status register. Raw status is set even if event is not enabled. Write 1 to set the (raw) status, mostly for debug.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												DMIC_IRQ_EMPTY	DMIC_IRQ_ALST_FULL	DMIC_IRQ_FULL	DMIC_IRQ

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved	R	0x0000000
3	DMIC_IRQ_EMPTY	Read 0x0: No event pending Write 0x0: No action Write 0x1: Set Read 0x1: IRQ event pending	RW	0
2	DMIC_IRQ_ALST_FULL	Read 0x0: No event pending Write 0x0: No action Write 0x1: Set Read 0x1: IRQ event pending	RW W1toSet	0
1	DMIC_IRQ_FULL	Read 0x0: No event pending Write 0x0: No action Write 0x1: Set Read 0x1: IRQ event pending	RW W1toSet	0

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Bits	Field Name	Description	Type	Reset
0	DMIC_IRQ	Read 0x0: No event pending Write 0x0: No action Write 0x1: Set Read 0x1: IRQ event pending	RW W1toSet	0

Table 23-530. Register Call Summary for Register DMIC_IRQSTATUS_RAW

Digital Microphone Module

- DMIC Interrupt Requests: [0] [1] [2] [3] [4] [5] [6]
- DMIC Register Summary: [7]

Table 23-531. DMIC_IRQSTATUS

Address Offset	0x0000 0028		
Physical Address	0x4902 E028 0x4012 E028 0x2 E028	**Instance**	DMIC_L3 DMIC_CORTEX-A9 DMIC_DSP
Description	Component (that is, main) interrupt request status. Check the corresponding secondary status register. Enabled status is not set unless event is enabled. Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, that is, even if not enabled).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												DMIC_IRQ_EMPTY	DMIC_IRQ_ALST_FULL	DMIC_IRQ_FULL	DMIC_IRQ

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved	R	0x0000000
3	DMIC_IRQ_EMPTY	Read 0x0: No event pending Write 0x0: No action Write 0x1: Clear pending event, if any Read 0x1: IRQ event pending	RW	0
2	DMIC_IRQ_ALST_FULL	This interrupt status is set when only one FIFO space is still available. Read 0x0: No event pending Write 0x0: No action Write 0x1: Clear pending event, if any Read 0x1: IRQ event pending	RW W1toClr	0
1	DMIC_IRQ_FULL	This interrupt status is set when FIFO is full and a new write access has been performed by filter. Read 0x0: No event pending Write 0x0: No action Write 0x1: Clear pending event, if any. Read 0x1: IRQ event pending	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
0	DMIC_IRQ	This interrupt status is set when FIFO threshold value defined in DMIC_FIFO_CTRL is reached. Read 0x0: No event pending Write 0x0: No action Write 0x1: Clear pending event, if any. Read 0x1: IRQ event pending	RW W1toClr	0

Table 23-532. Register Call Summary for Register DMIC_IRQSTATUS

Digital Microphone Module

- DMIC Interrupt Requests: [0] [1] [2] [3] [4] [5] [6] [7]
- Operational Mode Configuration: [8]
- DMIC Events Servicing: [9]
- DMIC Register Summary: [10]

Table 23-533. DMIC_IRQENABLE_SET

Address Offset	0x0000 002C		
Physical Address	0x4902 E02C 0x4012 E02C 0x2 E02C	**Instance**	DMIC_L3 DMIC_CORTEX-A9 DMIC_DSP
Description	Component (that is, main) interrupt request enable. Write 1 to set (enable interrupt). Readout equal to corresponding _SET register. _SET register is cleared when writing 1 to _CLR register.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												DMIC_IRQ_EMPTY_MASK	DMIC_IRQ_ALST_FULL_MASK	DMIC_IRQ_FULL_MASK	DMIC_IRQ_MASK

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved	R	0x0000000
3	DMIC_IRQ_EMPTY_MASK	Read 0x0: Interrupt disabled Write 0x0: No action Write 0x1: Enable interrupt Read 0x1:	RW W1toSet	0
2	DMIC_IRQ_ALST_FULL_MASK	Read 0x0: Interrupt disabled Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled	RW W1toSet	0
1	DMIC_IRQ_FULL_MASK	Read 0x0: Interrupt disabled Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled	RW W1toSet	0

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Bits	Field Name	Description	Type	Reset
0	DMIC_IRQ_MASK	Read 0x0: Interrupt disabled Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled	RW W1toSet	0

Table 23-534. Register Call Summary for Register DMIC_IRQENABLE_SET

Digital Microphone Module

- DMIC Interrupt Requests: [0] [1] [2] [3] [4] [5]
- Operational Mode Configuration: [6] [7]
- DMIC Register Summary: [8]

Table 23-535. DMIC_IRQENABLE_CLR

Address Offset	0x0000 0030		
Physical Address	0x4902 E030 0x4012 E030 0x2 E030	**Instance**	DMIC_L3 DMIC_CORTEX-A9 DMIC_DSP
Description	Component (that is, main) interrupt request enable Write 1 to clear (disable interrupt). Readout equal to corresponding _SET register. _SET register is cleared when writing 1 to _CLR register.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												DMIC_IRQ_EMPTY_MASK	DMIC_IRQ_ALST_FULL_MASK	DMIC_IRQ_FULL_MASK	DMIC_IRQ_MASK

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved	R	0x0000000
3	DMIC_IRQ_EMPTY_MASK	Read 0x0: Interrupt disabled Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled	RW W1toClr	0
2	DMIC_IRQ_ALST_FULL_MASK	Read 0x0: Interrupt disabled Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled	RW W1toClr	0
1	DMIC_IRQ_FULL_MASK	Read 0x0: Interrupt disabled Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
0	DMIC_IRQ_MASK	Read 0x0: Interrupt disabled Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled	RW W1toClr	0

Table 23-536. Register Call Summary for Register DMIC_IRQENABLE_CLR

Digital Microphone Module
- DMIC Interrupt Requests: [0] [1] [2] [3] [4]
- DMIC Register Summary: [5]

Table 23-537. DMIC_IRQWAKEEN

Address Offset	0x0000 0034		
Physical Address	0x4902 E034 0x4012 E034 0x2 E034	**Instance**	DMIC_L3 DMIC_CORTEX-A9 DMIC_DSP
Description	This register allows to enable the wake-up capability on interrupt event.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															IRQ_WAKEUP_EN

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	IRQ_WAKEUP_EN	Write 1 to allow wake-up by IRQ source (register threshold value reached).	RW	1

Table 23-538. Register Call Summary for Register DMIC_IRQWAKEEN

Digital Microphone Module
- DMIC Power Management: [0]
- DMIC Register Summary: [1]

Table 23-539. DMIC_DMAENABLE_SET

Address Offset	0x0000 0038		
Physical Address	0x4902 E038 0x4012 E038 0x2 E038	**Instance**	DMIC_L3 DMIC_CORTEX-A9 DMIC_DSP
Description	Component DMA enable (1 bit per DMA-capable channel)/Write 1 to set (enable DMA). Readout equal to corresponding _SET register. _SET register is cleared when writing 1 to _CLR register.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															DMA_ENABLE

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	DMA_ENABLE	Write 1 to set (enable DMA request) Read 0x0: Interrupt disabled Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled	RW W1toSet	0

Table 23-540. Register Call Summary for Register DMIC_DMAENABLE_SET

Digital Microphone Module

- DMIC DMA Requests: [0] [1]
- Operational Mode Configuration: [2]
- DMIC Register Summary: [3]

Table 23-541. DMIC_DMAENABLE_CLR

Address Offset	0x0000 003C		
Physical Address	0x4902 E03C 0x4012 E03C 0x2 E03C	**Instance**	DMIC_L3 DMIC_CORTEX-A9 DMIC_DSP
Description	Component DMA enable (1 bit per DMA-capable channel)/Write 1 to clear (disable DMA). Readout equal to corresponding _SET register. _SET register is cleared when writing 1 to _CLR register.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															DMA_ENABLE

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	DMA_ENABLE	Write 1 to clear (disable DMA request) Read 0x0: Interrupt disabled Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled	RW W1toClr	0

Table 23-542. Register Call Summary for Register DMIC_DMAENABLE_CLR

Digital Microphone Module

- DMIC DMA Requests: [0] [1]
- DMIC Register Summary: [2]

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Table 23-543. DMIC_DMAWAKEEN

Address Offset	0x0000 0040		
Physical Address	0x4902 E040 0x4012 E040 0x2 E040	**Instance**	DMIC_L3 DMIC_CORTEX-A9 DMIC_DSP
Description	This register allows to enable the wake-up capability on DMA request event.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															DMA_WAKEUP_EN

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	DMA_WAKEUP_EN	Write 1 to allow wakeup by DMA source (register threshold value reached).	RW	1

Table 23-544. Register Call Summary for Register DMIC_DMAWAKEEN

Digital Microphone Module

- DMIC Power Management: [0]
- DMIC Register Summary: [1]

Table 23-545. DMIC_CTRL

Address Offset	0x0000 0044		
Physical Address	0x4902 E044 0x4012 E044 0x2 E044	**Instance**	DMIC_L3 DMIC_CORTEX-A9 DMIC_DSP
Description	This register configures the various parameters of the DMIC module.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																					SW_DMIC_RST	DMIC_CLK_DIV			DMIC_POLAR3	DMIC_POLAR2	DMIC_POLAR1	DMICOUTFORMAT	DMIC_UP3_EN	DMIC_UP2_EN	DMIC_UP1_EN

Bits	Field Name	Description	Type	Reset
31:11	RESERVED	Reserved	R	0x000000
10	SW_DMIC_RST	Software reset of the DMIC path. When 1, the DMIC path is reset. Clearing the reset is done by writing 0 to the register.	RW	0
9:7	DMIC_CLK_DIV	Select the DMIC output clock frequency. See Table 23-511 for details.	RW	0x0

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Bits	Field Name	Description	Type	Reset
6	DMIC_POLAR3	0x0: When 0, the left data is generated in the external microphone 3 on abe_dmic_clk3 low level. 0x1: When 1, the left data is generated in the external microphone 3 on abe_dmic_clk3 high level.	RW	0
5	DMIC_POLAR2	0x0: When 0, the left data is generated in the external microphone 2 on abe_dmic_clk2 low level. 0x1: When 1, the left data is generated in the external microphone 2 on abe_dmic_clk2 high level.	RW	0
4	DMIC_POLAR1	0x0: When 0, the left data is generated in the external microphone 1 on abe_dmic_clk1 low level. 0x1: When 1, the left data is generated in the external microphone 1 on abe_dmic_clk1 high level.	RW	0
3	DMICOUTFORMAT	When 0, the data going out from the FIFO are left shifted from 8 bits. When 1, the data going are signed extended on 32 bits	RW	0
2	DMIC_UP3_EN	When 1, uplink path 3 is powered up.	RW	0
1	DMIC_UP2_EN	When 1, uplink path 2 is powered up.	RW	0
0	DMIC_UP1_EN	When 1, uplink path 1 is powered up.	RW	0

Table 23-546. Register Call Summary for Register DMIC_CTRL

Digital Microphone Module

- Serial Data Format: [0] [1] [2]
- DMIC Clock Configuration: [3]
- DMIC Software Reset: [4] [5] [6] [7] [8] [9]
- Audio Data Processing: [10] [11] [12]
- Filtering: [13] [14] [15]
- FIFO Operations: [16] [17] [18]
- FIFO Output Range Definition: [19]
- Global Initialization: [20] [21] [22] [23]
- DMIC Register Summary: [24]

Table 23-547. DMIC_DATA_REG

Address Offset	0x0000 0048		
Physical Address	0x4902 E048 0x4012 E048 0x2 E048	**Instance**	DMIC_L3 DMIC_CORTEX-A9 DMIC_DSP
Description	DMIC FIFO data		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMIC_DATA																															

Bits	Field Name	Description	Type	Reset
31:0	DMIC_DATA	DMIC FIFO data	R	0x000000

Table 23-548. Register Call Summary for Register DMIC_DATA_REG

Digital Microphone Module

- FIFO Output Range Definition: [0]
- Operational Mode Configuration: [1]
- DMIC Events Servicing: [2]
- DMIC Register Summary: [3]

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Table 23-549. DMIC_FIFO_CTRL

Address Offset	0x0000 004C		
Physical Address	0x4902 E04C 0x4012 E04C 0x2 E04C	**Instance**	DMIC_L3 DMIC_CORTEX-A9 DMIC_DSP
Description	This register sets the FIFO threshold for the data-ready event.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												DMIC_TRESH			

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved	R	0x0000
3:0	DMIC_TRESH	Uplink FIFO threshold	RW	0x2

Table 23-550. Register Call Summary for Register DMIC_FIFO_CTRL

Digital Microphone Module

- FIFO Operations: [0] [1]
- Global Initialization: [2]
- DMIC Register Summary: [3]
- DMIC Register Descriptions: [4]

Table 23-551. DMIC_FIFO_DMIC1R_DATA

Address Offset	0x0000 0050		
Physical Address	0x4902 E050 0x4012 E050 0x2 E050	**Instance**	DMIC_L3 DMIC_CORTEX-A9 DMIC_DSP
Description	Data of the first FIFO DMIC right channel		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								FIFO_DMIC1R_DAT																							

Bits	Field Name	Description	Type	Reset
31:24	RESERVED	Reserved	R	0x00
23:0	FIFO_DMIC1R_DAT	Data of the right FIFO DMIC path 1	R	0x000000

Table 23-552. Register Call Summary for Register DMIC_FIFO_DMIC1R_DATA

Digital Microphone Module

- FIFO Output Range Definition: [0]
- DMIC Register Summary: [1]

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Table 23-553. DMIC_FIFO_DMIC1L_DATA

Address Offset	0x0000 0054		
Physical Address	0x4902 E054 0x4012 E054 0x2 E054	**Instance**	DMIC_L3 DMIC_CORTEX-A9 DMIC_DSP
Description	Data of the first FIFO DMIC left channel		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								FIFO_DMIC1R_DAT																							

Bits	Field Name	Description	Type	Reset
31:24	RESERVED	Reserved	R	0x00
23:0	FIFO_DMIC1R_DAT	Data of the left FIFO DMIC path 1	R	0x000000

Table 23-554. Register Call Summary for Register DMIC_FIFO_DMIC1L_DATA

Digital Microphone Module

- FIFO Output Range Definition: [0]
- DMIC Register Summary: [1]

Table 23-555. DMIC_FIFO_DMIC2R_DATA

Address Offset	0x0000 0058		
Physical Address	0x4902 E058 0x4012 E058 0x2 E058	**Instance**	DMIC_L3 DMIC_CORTEX-A9 DMIC_DSP
Description	Data of the second FIFO DMIC right channel		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								FIFO_DMIC2R_DAT																							

Bits	Field Name	Description	Type	Reset
31:24	RESERVED	Reserved	R	0x00
23:0	FIFO_DMIC2R_DAT	Data of the right FIFO DMIC path 2	R	0x000000

Table 23-556. Register Call Summary for Register DMIC_FIFO_DMIC2R_DATA

Digital Microphone Module

- FIFO Output Range Definition: [0]
- DMIC Register Summary: [1]

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Table 23-557. DMIC_FIFO_DMIC2L_DATA

Address Offset	0x0000 005C		
Physical Address	0x4902 E05C 0x4012 E05C 0x2 E05C	**Instance**	DMIC_L3 DMIC_CORTEX-A9 DMIC_DSP
Description	Data of the second FIFO DMIC left channel		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								FIFO_DMIC2L_DAT																							

Bits	Field Name	Description	Type	Reset
31:24	RESERVED	Reserved	R	0x00
23:0	FIFO_DMIC2L_DAT	Data of the left FIFO DMIC path 2	R	0x000000

Table 23-558. Register Call Summary for Register DMIC_FIFO_DMIC2L_DATA

Digital Microphone Module

- FIFO Output Range Definition: [0]
- DMIC Register Summary: [1]

Table 23-559. DMIC_FIFO_DMIC3R_DATA

Address Offset	0x0000 0060		
Physical Address	0x4902 E060 0x4012 E060 0x2 E060	**Instance**	DMIC_L3 DMIC_CORTEX-A9 DMIC_DSP
Description	Data of the third FIFO DMIC right channel		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								FIFO_DMIC3R_DAT																							

Bits	Field Name	Description	Type	Reset
31:24	RESERVED	Reserved	R	0x00
23:0	FIFO_DMIC3R_DAT	Data of the right FIFO DMIC path 3	R	0x000000

Table 23-560. Register Call Summary for Register DMIC_FIFO_DMIC3R_DATA

Digital Microphone Module

- FIFO Output Range Definition: [0]
- DMIC Register Summary: [1]

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Table 23-561. DMIC_FIFO_DMIC3L_DATA

Address Offset	0x0000 0064		
Physical Address	0x4902 E064 0x4012 E064 0x2 E064	**Instance**	DMIC_L3 DMIC_CORTEX-A9 DMIC_DSP
Description	Data of the third FIFO DMIC left channel		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								FIFO_DMIC3R_DAT																							

Bits	Field Name	Description	Type	Reset
31:24	RESERVED	Reserved	R	0x00
23:0	FIFO_DMIC3R_DAT	Data of the left FIFO DMIC path 3	R	0x000000

Table 23-562. Register Call Summary for Register DMIC_FIFO_DMIC3L_DATA

Digital Microphone Module

- FIFO Output Range Definition: [0]
- DMIC Register Summary: [1]

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23.8 Multichannel Audio Serial Port

This section describes the multichannel audio serial port (McASP).

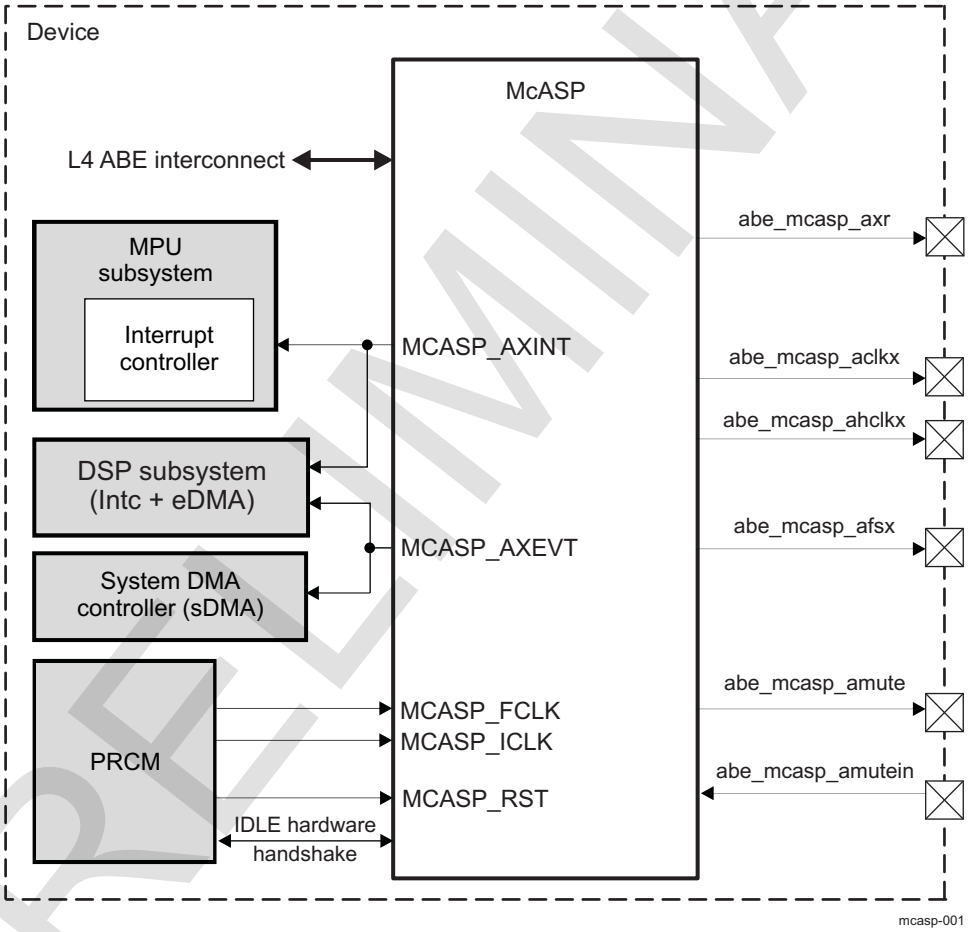
23.8.1 McASP Overview

This section introduces the multichannel audio serial port (McASP) module and describes its main functions and connections in the device.

The McASP functions as a general-purpose audio serial port optimized to the requirements of various audio applications. The McASP is useful for intercomponent digital audio interface transmission (DIT). The McASP has the flexibility to gluelessly connect to a Sony/Philips digital interface (S/PDIF) transmit physical layer component. The McASP module operates in transmit mode only; it has no receive capabilities.

Figure 23-186 shows the McASP module in the device.

Figure 23-186. McASP Module



The McASP module includes the following main features:

- Support of the idle request/acknowledge protocol
- Buffer for transmit operations
- One transmit direct memory access (DMA) request linked with a 32-bit register, and one transmit interrupt request
- One transmit channel
- One serializer

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23.8.2 McASP Environment

This section describes the McASP application fields from an environment point of view (external connections), along with the McASP connectivity options. This section also lists all of the possible interfaces and describes the protocol and data format used in each case.

23.8.2.1 McASP Signals

Table 23-563 describes the McASP signals and specifies their links to functions.

Table 23-563. I/O

Signal	I/O (1)	Description
abe_mcasp_axr	O	Audio transmit data
abe_mcasp_aclkx	O	Transmit bit clock
abe_mcasp_ahclkx	O	Transmit high-frequency master clock
abe_mcasp_afsx	O	Transmit frame synchronization
abe_mcasp_amute	O	Mute out to external
abe_mcasp_amutein	I	Mute in from external

(1) I = Input; O = Output

All McASP pins on the device can be individually programmed as general-purpose input/output (GPIO) if they are not used for serial port functions.

The McASP includes the following pins:

- Serializer:
  - Data pin abe_mcasp_axr
- Transmit clock generator:
  - abe_mcasp_aclkx: McASP transmit bit clock
  - abe_mcasp_ahclkx: McASP transmit high-frequency master clock
- Transmit frame-sync generator:
  - abe_mcasp_afsx: McASP transmit frame sync
- Mute in/out:
  - abe_mcasp_amutein: McASP mute input (from external device)
  - abe_mcasp_amute: McASP mute output

23.8.2.2 Protocols and Data Formats

23.8.2.2.1 Protocols Supported

The McASP transmit section uses the S/PDIF industry format, which is supported by the DIT transfer mode of the module.

Each transmit section can be programmed to support the following options on the basic serial protocol:

- Programmable clock and frame-sync polarity (rising or falling edge): abe_mcasp_aclkx, abe_mcasp_ahclkx, and abe_mcasp_afsx
- Slot length (number of bits per time slot): 8, 12, 16, 20, 24, 28, 32 bits supported
- Word length (bits per word): 8, 12, 16, 20, 24, 28, 32 bits; always less than or equal to the time slot length
- First-bit data delay: 0-, 1-, 2-bit clocks
- Left/right alignment of word inside slot
- Bit order: Most-significant bit (MSB) first or least-significant bit (LSB) first
- Bit mask/pad/rotate function
- Automatically aligns data in Q31 or integer format

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- Automatically masks nonsignificant bits (sets to 0, 1, or extends value of another bit)

The DIT transfer mode includes the following additional transmitter features:

- Transmit-only mode: 384 time slots (subframe) per frame
- Biphase encoded LVCMOS output
- Channel status RAM (384 bits)
- User data RAM (384 bits)
- Separate valid bit (V) for subframes A and B

NOTE: An external transceiver must be connected to the McASP port in the device to translate the electrical signals delivered by the McASP (1.2 V or 1.8 V LVCMOS levels) to the electrical levels of the S/PDIF standard.

23.8.2.2.2 Definition of Terms

The serial bitstream transmitted by the McASP is a long sequence of 1s and 0s on an audio transmit pin (abe_mcasp_axr). However, the sequence has a hierarchical organization that can be described in terms of frames of data, slots, words, and bits.

A basic synchronous serial interface consists of three important components: clock, frame sync, and data. Figure 23-187 shows two of the three basic components: the clock (abe_mcasp_aclkx) and the data (abe_mcasp_axr). In operation, the transmitter uses abe_mcasp_aclkx as serial clock.

- Bit:

  A bit is the smallest entity in the serial data stream. The beginning and end of each bit is marked by an edge of the serial clock. The duration of a bit is a serial clock period. A 1 is represented by a logic high on the abe_mcasp_axr pin for the entire duration of the bit. A 0 is represented by a logic low on the abe_mcasp_axr pin for the entire duration of the bit.

- Word:

  A word is a group of bits that make up the data being transferred between the McASP and the external device. Figure 23-187 shows an 8-bit word.

- Slot:

  A slot consists of the bits that make up the word and can consist of additional bits used to pad the word to a convenient number of bits for the interface between the McASP and the external device. In Figure 23-187, the audio data consists of only 8 bits of useful data (8-bit word), but it is padded with four 0s (12-bit slot) to satisfy the desired protocol in interfacing to an external device. Within a slot, the bits can be shifted out of the McASP on the abe_mcasp_axr pin with either MSB or LSB first.

  When the word size is smaller than the slot size, the word can be aligned to the left of the slot (beginning) or to the right of the slot (end). The additional bits in the slot not belonging to the word can be padded with 0, 1, or with one of the bits (typically, the MSB or LSB) from the data word. Figure 23-188 shows these options.

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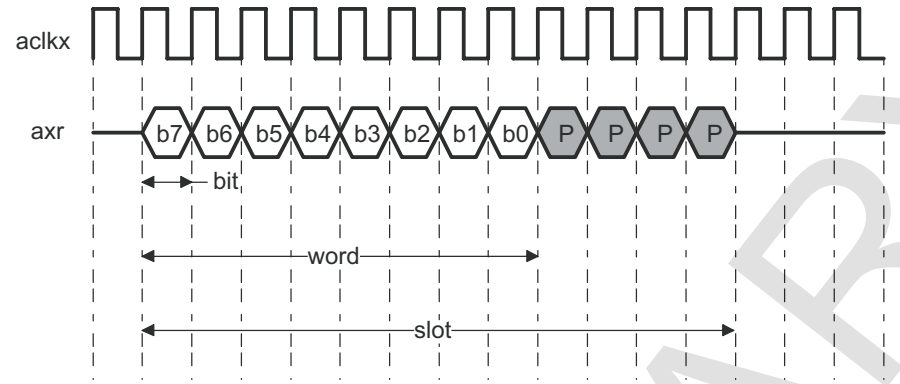
Figure 23-187. Definition of Bit, Word, and Slot



(1) b7:b0 - bits. Bits b7 to b0 form a word.

(2) P - pad bits. Bits b7 to b0, together with the 4 pad bits, form a slot.

(3) In this example, the data is transmitted MSB first, left-aligned.

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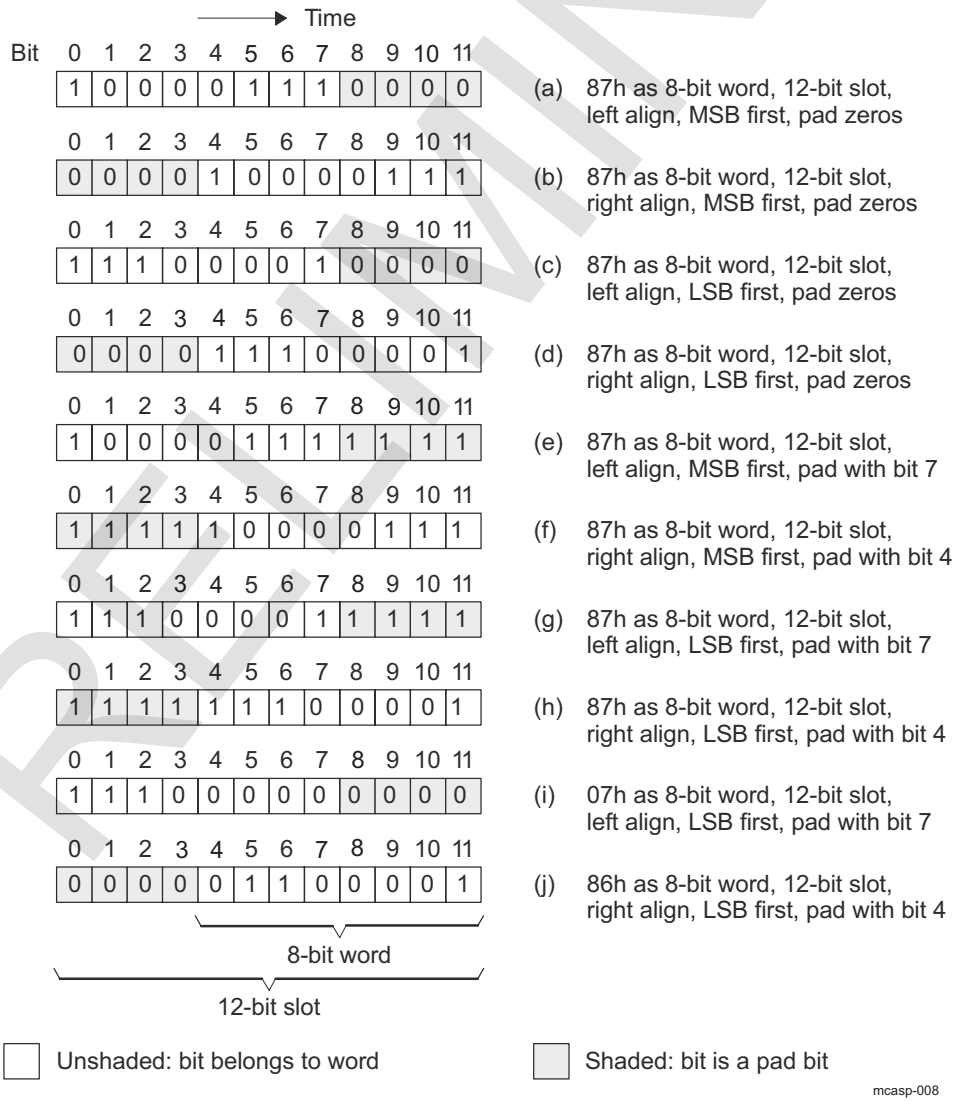
Figure 23-188. Bit Order and Word Alignment Within a Slot Examples



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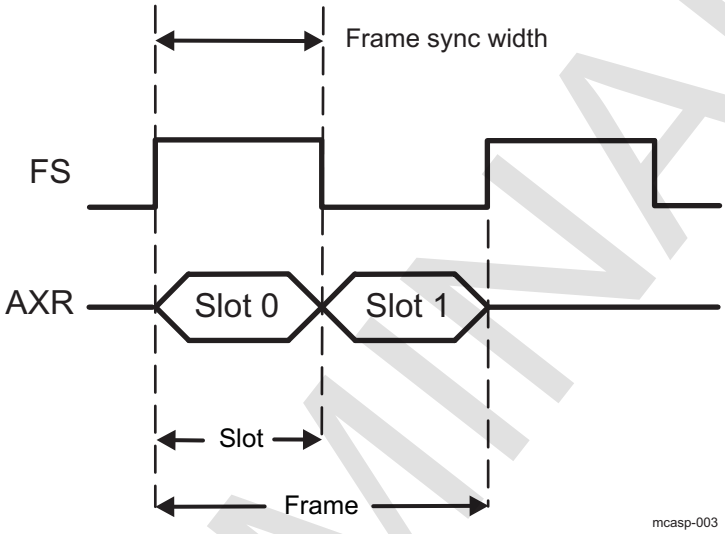
- Frame

  The third basic element of a synchronous serial interface is the frame synchronization signal, also referred to as frame sync in this document. A frame contains one or multiple slots, as determined by the desired protocol. Figure 23-189 shows an example frame of data and the frame definitions. In operation, the transmitter uses abe_mcasp_afsx. This example shows two slots in a frame and the frame-sync (FS) duration of the slot length.

  This section shows only the generic definition of the frame sync. For more information about the frame-sync formats required for the transfer modes and protocols (DIT mode and S/PDIF format), see Section 23.8.2.2.3, *Frame Format*.

Figure 23-189. Definition of Frame and Frame-Sync Width



The following terms are used throughout this chapter:

- DIT: Digital audio interface transmit. The McASP supports transmitting in S/PDIF format on the abe_mcasp_axr data pin.
- Slot or time slot: For DIT format, a McASP time slot corresponds to a DIT subframe.

23.8.2.2.3 S/PDIF Coding Format

The McASP transmitter supports the S/PDIF format with 3.3-V biphase-mark encoded output. The S/PDIF format is supported by the DIT transfer mode of the McASP. This section briefly discusses the S/PDIF coding format.

23.8.2.2.3.1 Biphase-Mark Code

In S/PDIF format, the digital signal is coded using the biphase-mark code (BMC). The clock, frame, and data are embedded in only one signal: data pin abe_mcasp_axr. In the BMC system, each data bit is encoded into two logical states (00, 01, 10, or 11) at the pin. These two logical states form a cell. The duration of the cell, which equals the duration of the data bit, is called a time interval. A logical 1 is represented by two transitions of the signal within a time interval, which corresponds to a cell with logical states 01 or 10. A logical 0 is represented by one transition within a time interval, which corresponds to a cell with logical states 00 or 11. In addition, the logical level at the start of a cell is inverted from the level at the end of the previous cell. Figure 23-190 and Table 23-564 show how data is encoded to the BMC format.

As shown in Figure 23-190, the clock frequency is twice the unencoded data bit rate. In addition, the clock is always programmed to 128 × f_s, where f_s is the sample rate (see Section 23.8.2.2.3.3, *Frame Format*, for details on how this clock rate is derived based on the S/PDIF format).

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Figure 23-190. Biphase-Mark Code

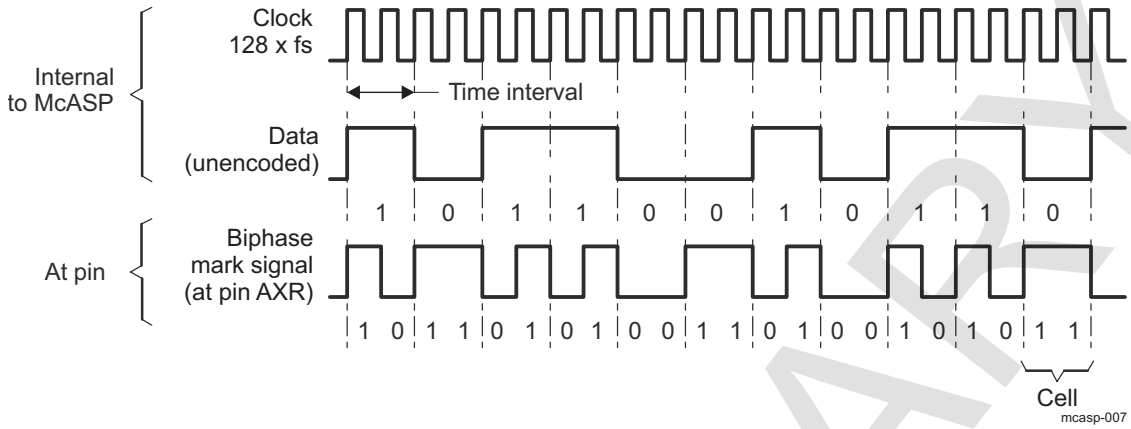

Table 23-564. Biphase-Mark Encoder

Data (Unencoded)	Previous State at Pin abe_mcasp_axr	BMC-Encoded Cell Output at abe_mcasp_axr
0	0	11
0	1	00
1	0	10
1	1	01

23.8.2.2.3.2 Subframe Format

Every audio sample transmitted in a subframe consists of 32 S/PDIF time intervals (or cells), numbered 0 to 31. Figure 23-191 shows a subframe.

- Time intervals 0–3 carry one of the three permitted preambles to signify the type of audio sample in the current subframe. The preamble is not encoded in BMC format, and therefore the preamble code can contain more than two consecutive 0 or 1 logical states in a row. See Table 23-565.
- Time intervals 4–27 carry the audio sample word in linear 2s-complement representation. The MSB is carried by time interval 27. When a 24-bit coding range is used, the LSB is in time interval 4. When a 20-bit coding range is used, time intervals 8-27 carry the audio sample word with the LSB in time interval 8. Time intervals 4–7 may be used for other applications and are designated auxiliary sample bits.
- If the source provides fewer bits than the interface allows (20 or 24), the unused LSBs are set to logical 0. For a nonlinear PCM audio application or a data application, the main data field can carry any other information.
- Time interval 28 carries the validity bit (V) associated with the main data field in the subframe.
- Time interval 29 carries the user data channel (U) associated with the main data field in the subframe.
- Time interval 30 carries the channel status information (C) associated with the main data field in the subframe. The channel status indicates if the data in the subframe is digital audio or some other type of data.
- Time interval 31 carries a parity bit (P) such that time intervals 4–31 carry an even number of 1s and an even number of 0s (even parity). As listed in Table 23-565, the preambles (time intervals 0–3) are also defined with even parity.

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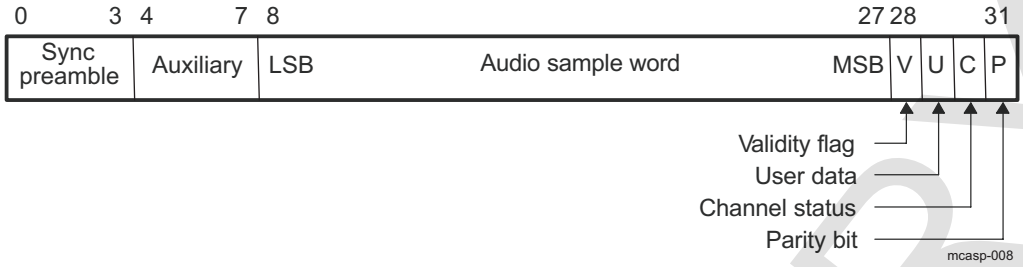
Figure 23-191. S/PDIF Subframe Format



As listed in Table 23-565, the McASP DIT generates only one polarity of preambles, and it assumes the previous logical state is 0. This is because the McASP assures an even-polarity encoding scheme when transmitting in DIT mode. If an underrun condition occurs, the DIT resynchronizes to the correct logic level on the abe_mcasp_axr pin before continuing with the next transmission.

Table 23-565. Preamble Codes

Preamble Code [1]	Previous Logical State	Logical States on pin abe_mcasp_axr [2]	Description
B (or Z)	0	1110 1000	Start of a block and subframe 1
M (or X)	0	1110 0010	Subframe 1
W (or Y)	0	1110 0100	Subframe 2

(1) Historically, preamble codes are referred to as B, M, and W. For use in professional applications, preambles are referred to as Z, X, and Y, respectively.

(2) The preamble is not BMC-encoded. Each logical state is synchronized to the serial clock. These eight logical states make up time slots (cells) 0 to 3 in the S/PDIF stream.

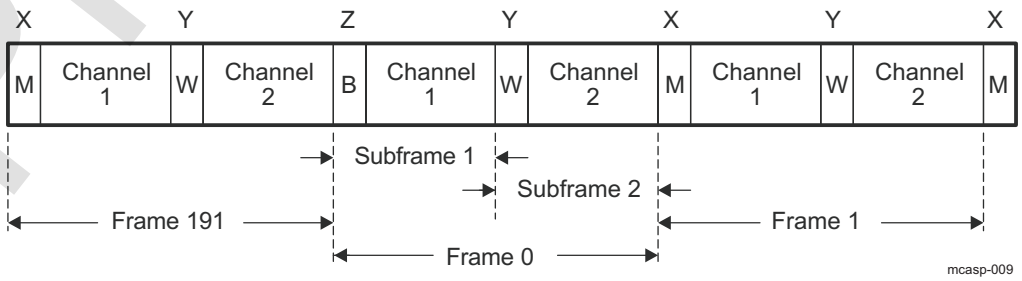
23.8.2.2.3.3 Frame Format

An S/PDIF frame is composed of two subframes (see Figure 23-192). For linear coded audio applications, the rate of frame transmission normally corresponds exactly to the source sampling frequency f_s. The S/PDIF format clock rate is therefore 128 × f_s (128 = 32 cells per subframe × 2 clocks per cell × 2 subframes per sample). For example, for an S/PDIF stream at a 192-kHz sampling frequency, the serial clock is 128 × 192 kHz = 24.58 MHZ.

In 2-channel operation mode, the samples taken from both channels are transmitted by time multiplexing in consecutive subframes. Both subframes contain valid data. The first subframe (left or A channel in stereophonic operation and primary channel in monophonic operation) normally starts with preamble M. However, the preamble of the first subframe changes to preamble B once every 192 frames to identify the start of the block structure used to organize the channel status information. The second subframe (right or B channel in stereophonic operation and secondary channel in monophonic operation) always starts with preamble W.

In single-channel operation mode in a professional application, the frame format is the same as in the 2-channel mode. Data is carried in the first subframe and may be duplicated in the second subframe. If the second subframe is not carrying duplicate data, cell 28 (validity bit) is set to logical 1.

Figure 23-192. S/PDIF Frame Format



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23.8.3 McASP Integration

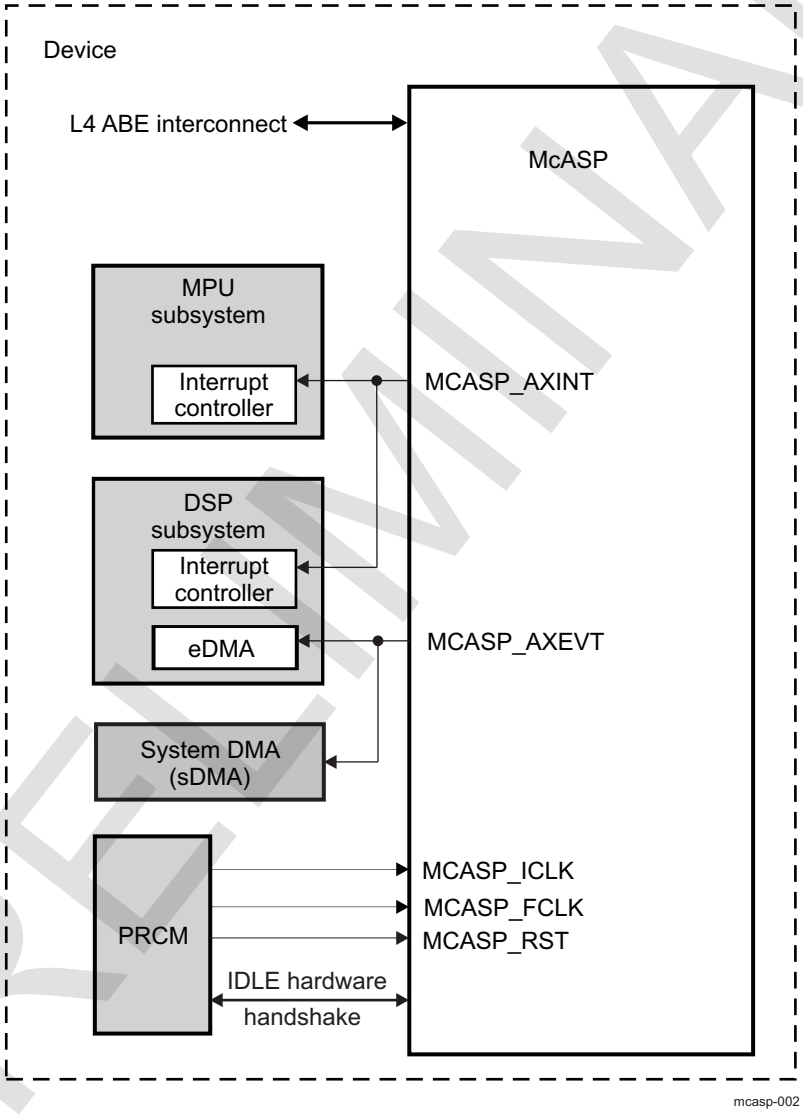
This section describes module integration in the device, including information about clocks, resets, and hardware requests.

The McASP includes the following features:

- IDLE hardware handshake
- One DMA request
- One interrupt request (IRQ)

Figure 23-193 shows McASP integration.

Figure 23-193. McASP Integration



NOTE: For more information about the IDLE hardware handshake, see Section 3.1.1.1.2, *Module Level Clock Management*, in Chapter 3, *Power, Reset, and Clock Management*.

Table 23-566 through Table 23-568 summarize the integration of the module in the device.

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Table 23-566. Integration Attributes

Module Instance	Attributes		
	Power Domain	Wake-Up Capability	Interconnect
McASP	PD_AUDIO	NO	L4_ABE

Table 23-567. Clocks and Resets

Clocks				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
McASP	MCASP_ICLK	ABE_ICLK2	PRCM	McASP interface clock
	MCASP_FCLK	MCASP1_FCLK	PRCM	McASP functional clock
Resets				
McASP	MCASP_RST	AUDIO_RST	PRCM	AUDIO power domain reset

Table 23-568. Hardware Requests

Interrupt Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
McASP	MCASP_AXINT	D_IRQ_92	DSP	McASP transmit interrupt
	MCASP_AXINT	MA_IRQ_109	Cortex ™-A9	McASP transmit interrupt
DMA Requests				
McASP	MCASP_AXEVT	S_DMA_7	sDMA	McASP data transmit DMA request line to the system DMA (sDMA)
	MCASP_AXEVT	D_DMA_36	eDMA	McASP data transmit DMA request line to the DSP DMA (eDMA)

NOTE:

- For the description of the interrupt source, see Section 23.8.4.11, *Interrupt Requests*.
- For the description of the DMA source, see Section 23.8.4.12, *DMA Requests*.

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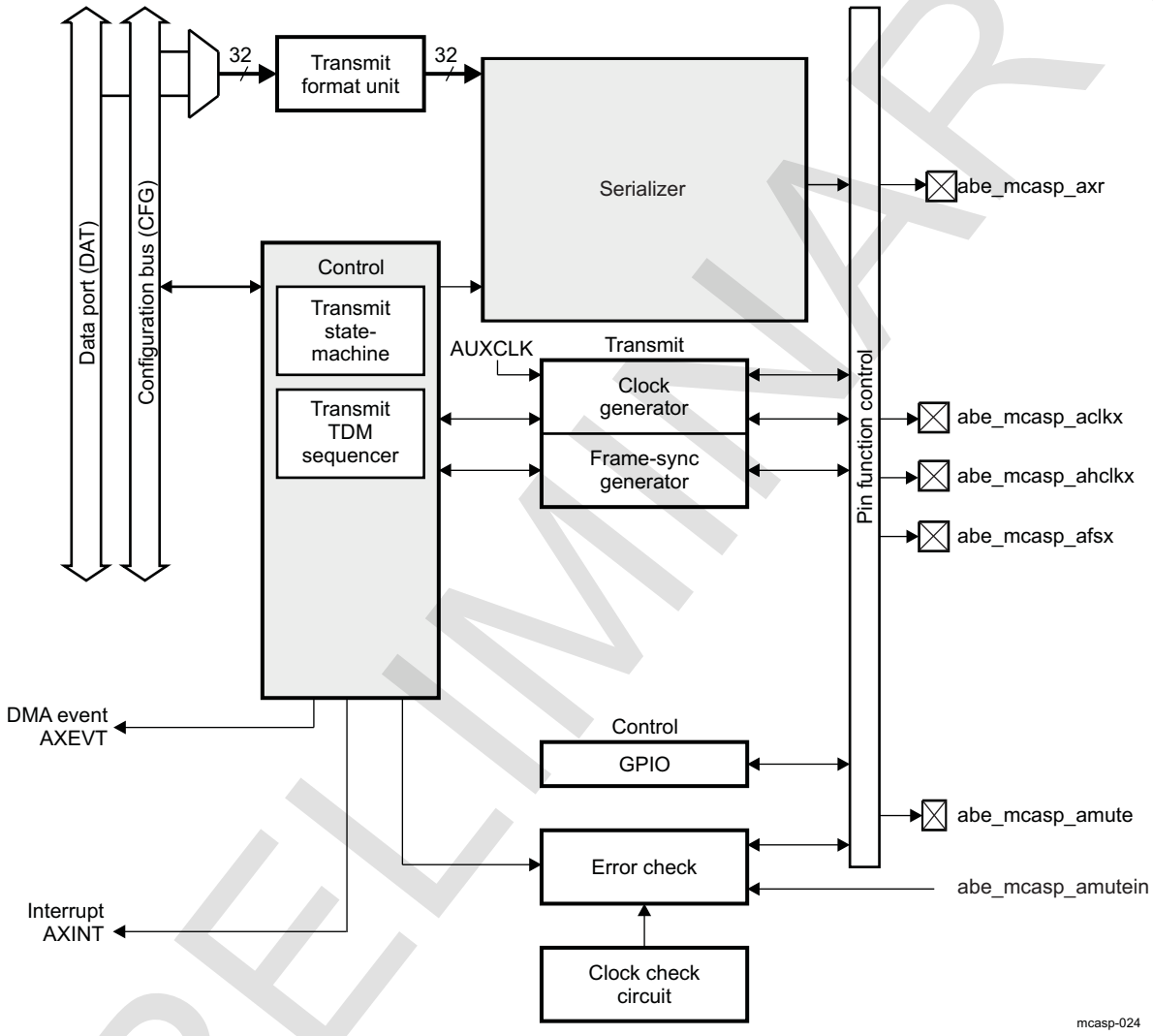
23.8.4 McASP Functional Description

23.8.4.1 Block Diagram

Figure 23-194 shows the major blocks of the McASP. The McASP has a transmit clock generator and a frame-sync generator, serializer, format unit, and error-checking logic.

Figure 23-194. McASP Block Diagram



NOTE: The AUXCLK clock is sourced directly from MCASP_FCLK.

23.8.4.2 McASP Clock and Frame-Sync Configuration

The transmit serial clock (clock at the bit rate) can be sourced internally by passing through two clock dividers off the internal clock source (AUXCLK). The bit rate clock is generated internally and is driven out on the abe_mcasp_aclkx pin. An internally generated high-frequency clock can be driven out onto the abe_mcasp_ahclkx pin to serve as a reference clock for other components in the system.

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23.8.4.2.1 Transmit Clock

The transmit bit clock, abe_mcasp_aclkx, is generated internally. For this purpose, the MCASP_ACLKXCTL[5] CLKXM bit must be set to 1. Thus, the clock is divided down by a programmable bit clock divider (the MCASP_ACLKXCTL[4:0] CLKXDIV bit field) from the source signal.

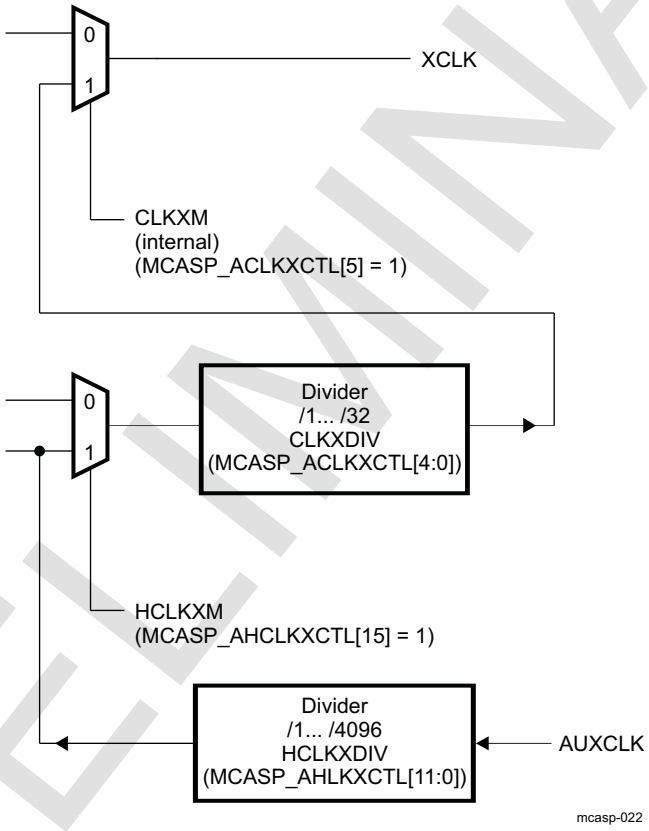
The transmit high-frequency master clock, abe_mcasp_ahclkx, is also generated internally. For this purpose, the MCASP_AHCLKXCTL[15] HCLKXM bit must be set to 1. Thus, the clock is divided down by a programmable high-clock divider (the MCASP_AHCLKXCTL[11:0] HCLKXDIV bit field) from the McASP internal clock source AUXCLK.

The transmit clock configuration is controlled by the following registers:

- MCASP_ACLKXCTL
- MCASP_AHCLKXCTL

Figure 23-195 is the block diagram of the transmit clock generator.

Figure 23-195. Transmit Clock Generator Block Diagram



23.8.4.2.2 Frame-Sync Generator

The transmit frame-sync pin is abe_mcasp_afsx. The frame-sync generator must be configured through the control register (MCASP_TXFMCTL) as:

- Internally generated MCASP_TXFMCTL[1] FSXM = 1
- Frame-sync polarity: Rising edge MCASP_TXFMCTL[0] FSXP = 0
- Frame-sync width: Single bit MCASP_TXFMCTL[4] FXWID = 0
- 384-slot, MCASP_TXFMCTL[15:7] XMOD = 1 1000 0000b

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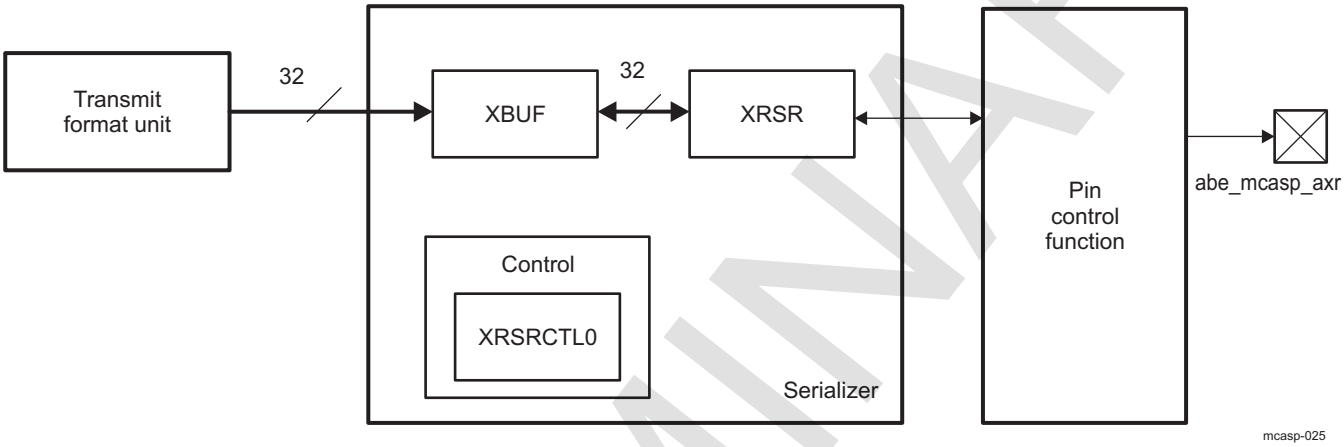
23.8.4.3 Serializers

The serializer shifts serial data out of the McASP. It consists of a shift register (XRSR), a data buffer (XBUF), a control register (MCASP_XRSRCTL0), a serial data pin (abe_mcasp_axr), and logic to support the data alignment options of the McASP.

The serializer must be configured to transmit through the control register, thus shifting out data to abe_mcasp_axr. The serializer is clocked from the transmit section clock (abe_mcasp_aclkx) if configured to transmit. A serializer configured to transmit operates in lockstep.

Figure 23-196 is the serializer block diagram.

Figure 23-196. Individual Serializer and Connections Within McASP



For transmit, the microprocessor unit (MPU) services the McASP by writing data into the XBUF register, which is an alias of the MCASP_TXBUF0 register. The data automatically passes through the transmit format unit before reaching the XBUF register in the serializer. The data is then copied from XBUF to XRSR and shifted out from abe_mcasp_axr synchronously to the serial clock.

In addition to the data, the serializer shifts out other DIT-specific information accordingly (preamble, user data, etc.). The serializer configuration is controlled by MCASP_XRSRCTL0[1:0] SRMOD = 0x1. Thus, the serializer is configured to operate in transmit mode.

23.8.4.4 Format Unit

The McASP has one transmit data formatting unit. This unit automatically remaps the data bits within the transmitted words between a natural format for the MPU (such as a Q31 representation) and the required format for the external serial device. During the remapping process, the format unit can also mask off certain bits.

This formatting unit consists of two stages:

- Bit mask (masks off bits)
- Rotate right (aligns data within word)

Figure 23-197 shows the transmit formatting unit.

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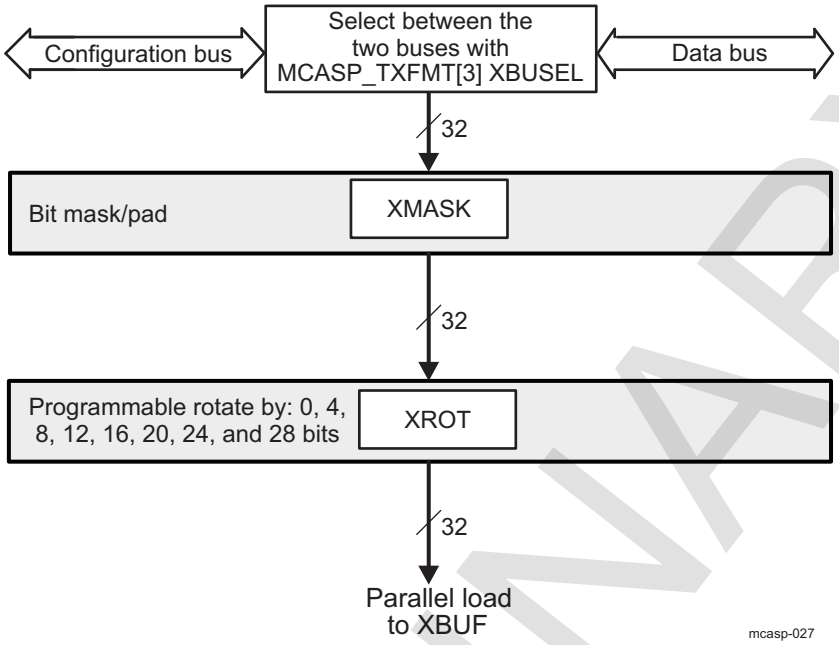
Figure 23-197. Transmit Format Unit



As shown in Figure 23-197, the data to the transmit format unit can come from the configuration bus or the data bus. The selection is made through the MCASP_TXFMT[3] XBUSEL bit.

The bit mask stage includes a full 32-bit mask register, allowing selected individual bits to pass through the stage unchanged or be masked off.

The rotate-right stage performs bitwise rotation by 0 bits for right-aligned Q31 data and bitwise rotation by 8 bits for left-aligned Q31 data, programmable by the MCASP_TXFMT[2:0] XROT bit field. This is a rotation process, not a shifting process, so bit 0 gets shifted back into bit 31 during the process.

The MCASP_TXFMT[17:16] XDATLY bit field must be set to a 0-bit delay (0x0 value).

For left-aligned Q31 data, the following transmit format unit settings process the data into right-aligned 24-bit audio data, ready for transmission:

- MCASP_TXFMT[2:0] XROT = 0x2 (rotate right by 8 bits)
- MCASP_TXFMT[15] XRVRS = 0x0 – Bit reversal is not enabled; the McASP naturally transmits and receives in an LSB-first order.
- MCASP_TXMASK[32] XMASK = 0xFFFFFF00 – 0xFFFF0000
- MCASP_TXFMT[14:13] XPAD = 0x0 (Pad extra bits with 0s.)

For right-aligned data, the following transmit format unit settings process the data into right-aligned 24-bit audio data ready for transmission:

- MCASP_TXFMT[2:0] XROT = 0x0 (rotate right by 0 bits)
- MCASP_TXFMT[15] XRVRS = 0x0 – Bit reversal is not enabled; the McASP naturally transmits and receives in an LSB-first order.
- MCASP_TXMASK[32] XMASK = 0x00FFFFFF – 0x0000FFFF
- MCASP_TXFMT[14:13] XPAD = 0x0 (Pad extra bits with 0s.)

Table 23-589 provides more details and specific examples. The examples use internal representation in integer and Q31 notation, but other fractional notations are also possible.

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23.8.4.5 Transmit State-Machine

The transmit state-machine controls the interactions between the various units in the transmit section. In addition, the state-machine keeps track of error conditions and serial port status. No serial transfers can occur until the transmit state-machine is released from reset.

The transmit state-machine is controlled by the transmit bitstream format register (MCASP_TXFMT) and it reports the McASP status and error conditions in the transmitter status register (MCASP_TXSTAT).

23.8.4.6 Transmit TDM Sequencer

The time division multiplexing (TDM) sequencer is used to count the 384 subframes (slots) in the DIT block. If currently transmitting slot 1, slot 2 (next value of the TDM slot counter) should be used during the encode phase to select the appropriate C, V, and U bit, because the data encoded and written to the MCASP_TXBUF0 register during the current time slot (slot 1) is actually shifted out on the next time slot.

The transmit TDM sequencer is controlled by the MCASP_TXTDM register and reports the current transmit slot to the MCASP_TXTDMSLOT[9:0] XSLOTCNT bit field.

23.8.4.7 McASP Software Reset

The McASP can be put into reset through the global transmit control register (MCASP_GBLCTL). A valid serial clock must be supplied to the McASP to assert the software reset bits in the MCASP_GBLCTL register.

23.8.4.8 McASP Power Management

Table 23-569 describes power-management features available to the McASP.

Table 23-569. Local Power-Management Features

Feature	Registers	Description
Slave idle modes	MCASP_SYSCONFIG[1:0] IDLE_MODE	Force-idle, no-idle, and smart-idle modes are available.

23.8.4.9 Transfer Modes

23.8.4.9.1 DIT Transfer Mode

The DIT transfer mode of the McASP also supports transmission of audio data in S/PDIF, AES-3, and IEC-60958 formats. These formats are designed to carry audio data between different systems through an optical or coaxial cable. The DIT mode applies only to a serializer configured as transmitter, not receiver. For a description of the S/PDIF format, see Section 23.8.2.2.3, *S/PDIF Coding Format*.

23.8.4.9.1.1 Transmit DIT Encoding

When the McASP operates in DIT mode, the data transmitted is output as a biphase-mark encoded bitstream, with preamble, channel status, user data, validity, and parity automatically stuffed into the bitstream by the McASP. The McASP includes separate validity bits for even/odd subframes and two 384-bit RAM modules to hold channel status and user data bits.

The transmit TDM time slot register (MCASP_TXTDM) should be programmed to all 1s during DIT mode. TDM functionality is not supported in DIT mode, except that the TDM slot counter counts the DIT subframes.

To transmit data in DIT mode, the following pins are typically required:

- abe_mcasp_ahclkx – transmit high-frequency master clock (The internal clock source can be used instead.)
- One serial data pin, abe_mcasp_axr, with serializer configured to transmit

The actual 24-bit audio data must always be in bit positions 23–0 after passing through the first three stages of the transmit format unit.

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23.8.4.9.1.2 Transmit DIT Clock and Frame-Sync Generation

The DIT transmitter works only in the following configuration:

- In the transmit frame control register (MCASP_TXFMCTL):
  - Internally generated transmit frame sync, FSXM = 1
  - Rising-edge frame sync, FSXP = 0
  - Bit-width frame sync, FXWID = 0
  - 384-slot TDM, XMOD = 1 1000 0000b
- In the transmit clock control register (MCASP_ACLKXCTL), ASYNC = 1
- In the transmit bitstream format register (MCASP_TXFMT), XSSZ = 1111 (32-bit slot size)

All combinations of abe_mcasp_ahclkx and abe_mcasp_aclkx are supported.

The following summarizes the register configurations required for DIT mode. DIT mode-specific bit fields are in bold face:

- MCASP_PFUNC: The data pin must be configured for McASP function. If abe_mcasp_ahclkx is used, it must also be configured for McASP function. Other pins can be configured to function as GPIOs, if desired.
- MCASP_PDIR: The data pin must be configured as output. If internal clock source AUXCLK is used as the reference clock, it may be output on the abe_mcasp_ahclkx pin by configuring abe_mcasp_ahclkx as an output.
- MCASP_GBLCTL: Global initialization
- MCASP_AMUTE: Program all fields according to the mute control desired.
- MCASP_TXDITCTL: The **DITEN** bit must be set to 1 to enable DIT mode. Configure other bits as desired.
- **MCASP_TXMASK**: Mask the desired bits, depending upon left-aligned or right-aligned internal data.
- **MCASP_TXFMT: XDATDLY** = 0. **XRVRS** = 0. **XPAD** = 0. **XSSZ** = Fh (32-bit slot). XBUSEL = configured as desired. The **XROT** bit is configured either 0 or 8-bit rotate.
- **MCASP_TXFMCTL**: Configure the bits according to former discussions.
- **MCASP_ACLKXCTL**: **ASYNC** = 1. Program the CLKXDIV bits to obtain the bit clock rate desired. CLKXM = 1.
- **MCASP_AHCLKXCTL**: Program the HCLKXDIV bits to obtain the high-frequency bit clock rate desired.
- **MCASP_TXTDM**: Set to FFFF FFFFh for all active slots for DIT transfers.
- MCASP_TXEVTCTL: Program all fields according to the interrupts desired.
- MCASP_TXCLKCHK: Program all fields according to the clock checking desired.
- MCASP_XRSRCTL0: Set **SRMOD** = 1 (transmitter) for the DIT pins.
- **MCASP_DITCSRAi** and **MCASP_DITCSRBi**: Program the channel status bits as desired.
- **MCASP_DITUDRAi** and **MCASP_DITUDRBi**: Program the user data bits as desired.

23.8.4.9.1.3 DIT Channel Status and User Data Register Files

The channel status registers (MCASP_DITCSRAi and MCASP_DITCSRBi) and user data registers (MCASP_DITUDRAi and MCASP_DITUDRBi) are not double-buffered. Typically, programmers use one of the synchronizing interrupts, such as the last slot, to create an event at a safe time so the register may be updated. In addition, the MPU reads the transmit TDM slot counter to determine which word of the register is being used.

It is a software requirement to avoid writing to the word of user data and channel status that are being used to encode the current time slot; otherwise, it is undetermined whether old or new data is used to encode the bitstream.

The DIT subframe format is defined in Section 23.8.2.2.3.2, *Subframe Format*. The channel status information (C) and user data (U) are defined in the following DIT control registers:

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- MCASP_DITCSRA0 to MCASP_DITCSRA5: The 192 bits in these six registers contain the channel status information for the left channel within each frame.
- MCASP_DITCSRB0 to MCASP_DITCSRB5: The 192 bits in these six registers contain the channel status information for the right channel within each frame.
- MCASP_DITUDRA0 to MCASP_DITUDRA5: The 192 bits in these six registers contain the user data information for the left channel within each frame.
- MCASP_DITUDRB0 to MCASP_DITUDRB5: The 192 bits in these six registers contain the user data information for the right channel within each frame.
- The S/PDIF block format is shown in Figure 23-192. There are 192 frames within a block (frame 0 to frame 191). There are two subframes within each frame (subframes 1 and 2 for the left and right channels, respectively).

The channel status and user data information sent on each subframe is summarized in Table 23-570.

Table 23-570. Channel Status and User Data for Each DIT Block

Frame	Subframe	Preamble	Channel Status Defined in:	User Data Defined in:
Defined by DITCSRA0, DITCSRB0, DITUDRA0, DITUDRB0				
0	1 (L)	B	DITCSRA0[0]	DITUDRA0[0]
0	2 (R)	W	DITCSRB0[0]	DITUDRB0[0]
1	1 (L)	M	DITCSRA0[1]	DITUDRA0[1]
1	2 (R)	W	DITCSRB0[1]	DITUDRB0[1]
2	1 (L)	M	DITCSRA0[2]	DITUDRA0[2]
2	2 (R)	W	DITCSRB0[2]	DITUDRB0[2]
…	…	…	…	…
31	1 (L)	M	DITCSRA0[31]	DITUDRA0[31]
31	2 (R)	W	DITCSRB0[31]	DITUDRB0[31]
Defined by DITCSRA1, DITCSRB1, DITUDRA1, DITUDRB1				
32	1 (L)	M	DITCSRA1[0]	DITUDRA1[0]
32	2 (R)	W	DITCSRB1[0]	DITUDRB1[0]
…	…	…	…	…
63	1 (L)	M	DITCSRA1[31]	DITUDRA1[31]
63	2 (R)	W	DITCSRB1[31]	DITUDRB1[31]
Defined by DITCSRA2, DITCSRB2, DITUDRA2, DITUDRB2				
64	1 (L)	M	DITCSRA2[0]	DITUDRA2[0]
64	2 (R)	W	DITCSRB2[0]	DITUDRB2[0]
…	…	…	…	…
95	1 (L)	M	DITCSRA2[31]	DITUDRA2[31]
95	2 (R)	W	DITCSRB2[31]	DITUDRB2[31]
Defined by DITCSRA3, DITCSRB3, DITUDRA3, DITUDRB3				
96	1 (L)	M	DITCSRA3[0]	DITUDRA3[0]
96	2 (R)	W	DITCSRB3[0]	DITUDRB3[0]
…	…	…	…	…
127	1 (L)	M	DITCSRA3[31]	DITUDRA3[31]
127	2 (R)	W	DITCSRB3[31]	DITUDRB3[31]
Defined by DITCSRA4, DITCSRB4, DITUDRA4, DITUDRB4				
128	1 (L)	M	DITCSRA4[0]	DITUDRA4[0]
128	2 (R)	W	DITCSRB4[0]	DITUDRB4[0]
…	…	…	…	…
159	1 (L)	M	DITCSRA4[31]	DITUDRA4[31]
159	2 (R)	W	DITCSRB4[31]	DITUDRB4[31]
Defined by DITCSRA5, DITCSRB5, DITUDRA5, DITUDRB5				

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Table 23-570. Channel Status and User Data for Each DIT Block (continued)

Frame	Subframe	Preamble	Channel Status Defined in:	User Data Defined in:
160	1 (L)	M	DITCSRA5[0]	DITUDRA5[0]
160	2 (R)	W	DITCSRB5[0]	DITUDRB5[0]
…	…	…	…	…
191	1 (L)	M	DITCSRA5[31]	DITUDRA5[31]
191	2 (R)	W	DITCSRB5[31]	DITUDRB5[31]

23.8.4.10 Data Transmission

The MPU services the McASP by writing data to the MCASP_TXBUF0 register for transmit operations. The McASP sets status flags and notifies the MPU whenever data is ready to be transmitted. Section 23.8.4.10.1, *Data Ready Status and Event/Interrupt Generation*, discusses data-ready status in detail.

The MCASP_TXBUF0 register can be accessed through one of the two peripheral ports of the device:

- Data port (DAT): This port is dedicated to data transfers on the device.
- Configuration bus (CFG): This port is used for data transfers and peripheral configuration control on the device.

Section 23.8.4.10.1.2, *Transfers Through the Data Port (DAT)*, and Section 23.8.4.10.1.3, *Transfers Through the Configuration Bus (CFG),* discuss how to perform transfers through the data port and the configuration bus, respectively.

The MPU or the DMA can be used to service the McASP through either of these peripheral ports. The MPU and DMA usages are discussed in Section 23.8.4.10.1.4, *Using the MPU for McASP Servicing*, and Section 23.8.4.10.1.5, *Using the DMA for McASP Servicing*, respectively.

23.8.4.10.1 Data Ready Status and Event/Interrupt Generation

23.8.4.10.1.1 Transmit Data Ready

The transmit data ready flag XDATA bit in the MCASP_TXSTAT register reflects the status of the MCASP_TXBUF0 register. The XDATA flag is set when data is transferred from the MCASP_TXBUF0[n] buffer to the XRSR[n] shift register, thus indicating that the MCASP_TXBUF0 is empty and ready to accept new data from the MPU. This flag is cleared when the XDATA bit is written with 1, or when the serializer configured as transmitter is written by the MPU.

Whenever XDATA is set, the DMA AXEVT event is automatically generated to notify the DMA of the MCASP_TXBUF0 empty status. An AXINTn interrupt is also generated if the XDATA interrupt is enabled in the MCASP_EVTCTLX register (for details, see Section 23.8.4.11.1, *Transmit Data Ready Interrupt*).

For DMA requests, the McASP does not require that MCASP_TXSTAT be read between DMA events. This means that, even if MCASP_TXSTAT already has the XDATA flag set to 1 from a previous request, the next transfer triggers another DMA request.

Because the serializer acts in lockstep, only one DMA event is generated to indicate that the transmit serializer is ready to be written to with new data.

Figure 23-198 shows the timing details of when AXEVT is generated at the McASP boundary. In this example, as soon as the last bit (A0) of word A is transmitted, the McASP sets the XDATA flag and generates an AXEVT event. However, it takes up to five McASP system clocks (AXEVT latency) before AXEVT is active at the McASP boundary. Upon AXEVT, the MPU can begin servicing the McASP by writing word C into the MCASP_TXBUF0 (service time). The MPU must write word C into the MCASP_TXBUF0 within the setup time required by the McASP (setup time).

The maximum service time (see Figure 23-198) can be calculated as:

Service Time = Time Slot – AXEVT Latency –Setup Time

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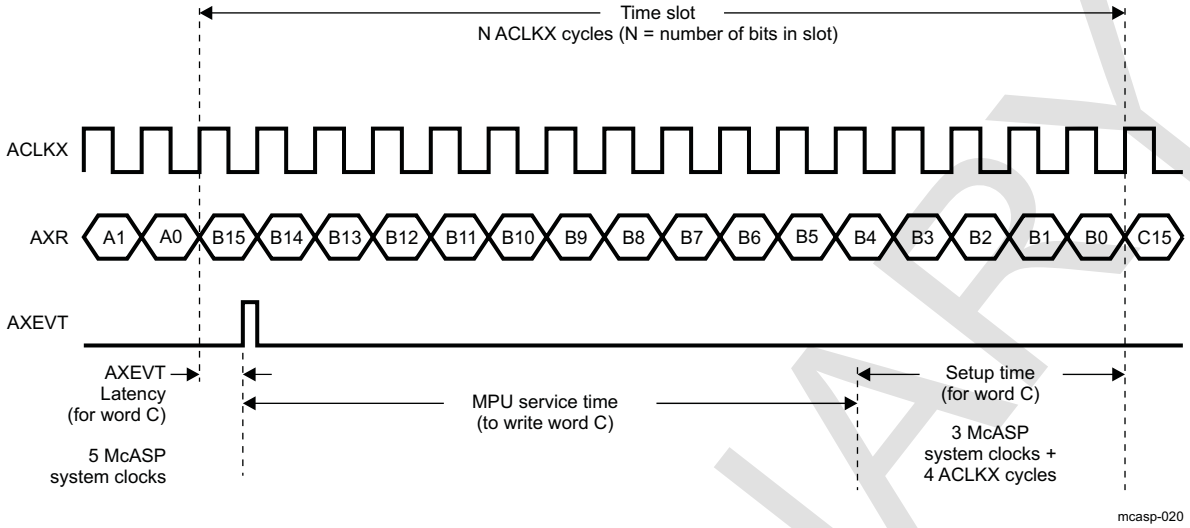
Figure 23-198. MPU Service Time Upon Transmit DMA Event (AXEVT)



23.8.4.10.1.2 Transfers Through the Data Port (DAT)

CAUTION

To perform internal transfers through the data port, clear the XBUSEL bit to 0 in the MCASP_TXFMT register. Failure to do so may result in software malfunction.

Typically, the MCASP_TXBUF0 register is accessed through the data port. To access through the data port, simply have the MPU or DMA access MCASP_TXBUF0 through its data port location.

NOTE: DAT allows the MPU, DSP subsystem, or DMA to access only the transmit buffer MCASP_TXBUF0 register. There is no way to access the McASP configuration registers within the MPU/DSP subsystem/DMA DAT address ranges.

For transmit operations through the data port, the DMA/MPU must write to the MCASP_TXBUF0 data port address to service the active transmit serializer.

When transmitting, the DMA/MPU must write data to the serializer and transmit within each time slot. Failure to do so may result in a buffer underrun condition (see Section 23.8.4.14.1, *Buffer Underrun Error – Transmitter*).

23.8.4.10.1.3 Transfers Through the Configuration Bus (CFG)

CAUTION

To perform internal transfers through the configuration bus, set the XBUSEL bit to 1 in the MCASP_TXFMT register. Failure to do so may result in software malfunction.

In this method, the DMA/MPU accesses the MCASP_TXBUF0 register through the configuration bus address.

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When transmitting, the DMA/MPU must write data to the serializer and transmit within each time slot. Failure to do so may result in a buffer underrun condition (Section 23.8.4.14.1, *Buffer Underrun Error – Transmitter*).

23.8.4.10.1.4 Using the MPU for McASP Servicing

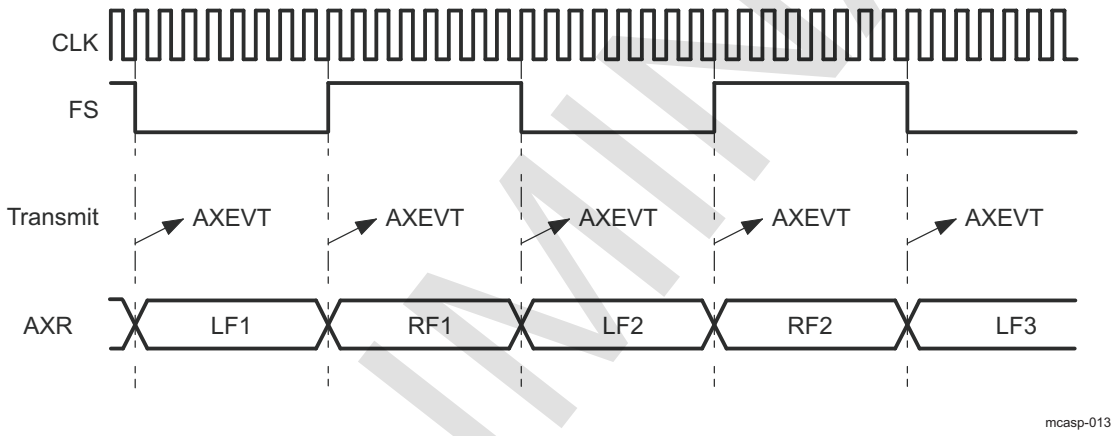
The MPU can be used to service the McASP through interrupts (upon MCASP_AXINT interrupt) or through polling the XDATA bit in the MCASP_TXSTAT register. As discussed in Section 23.8.4.10.1.2, *Transfers Through the Data Port (DAT)*, and Section 23.8.4.10.1.3, *Transfers Through the Configuration Bus (CFG)*, the MPU can access through the data port or the configuration bus.

To use the MPU to service the McASP through interrupts, the XSTAT bit must be enabled in the MCASP_TXEVTCTL register to generate the MCASP_AXINT interrupt to the MPU upon data ready.

23.8.4.10.1.5 Using the DMA for McASP Servicing

The typical scenario is to use the DMA to service the McASP through the data port, although the DMA can also service the McASP through the configuration bus.

Figure 23-199. DMA Transmit Event in an Audio Example – One Event



The DMA event AXEVT, which is triggered upon each XDATA transition from 0 to 1, is used to service the McASP transmit buffer (XBUF). Figure 23-199 is an example of an audio system with two audio channels (LF and RF) transmitted through the abe_mcasp_axr pin on the McASP. It shows the points at which event AXEVT is triggered.

The DMA AXEVT event is triggered on each time slot. In the example, AXEVT is triggered for each transmit audio channel time slot (time slot for channel LF, and time slot for channel RF). DMA events are generated automatically upon data ready, whereas MPU interrupt generation must be enabled in the MCASP_EVTCTLX register.

23.8.4.11 Interrupt Requests

Table 23-571 lists the event flags that can cause module interrupts.

Table 23-571. TX Events

Event Mask	Event Flag	Map to	Description
MCASP_EVTCTLX[0] XUNDRN	MCASP_TXSTAT[0] XUNDRN	MCASP_AXINT	Transmit underrun
MCASP_EVTCTLX[1] XSYNCERR	MCASP_TXSTAT[1] XSYNCERR	MCASP_AXINT	Unexpected transmit frame sync
MCASP_EVTCTLX[2] XCKFAIL	MCASP_TXSTAT[2] XCKFAIL	MCASP_AXINT	Transmit clock failure
MCASP_EVTCTLX[4] XLAST	MCASP_TXSTAT[4] XLAST	MCASP_AXINT	Transmit last slot interrupt
MCASP_EVTCTLX[5] XDATA	MCASP_TXSTAT[5] XDATA	MCASP_AXINT	Transmit data-ready interrupt
MCASP_EVTCTLX[7] XSTAFRM	MCASP_TXSTAT[7] XSTAFRM	MCASP_AXINT	Transmit start of frame interrupt

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An interrupt line is asserted (active high) when one of these events occurs. Read the MCASP_TXSTAT register to determine which event occurs.

23.8.4.11.1 Transmit Data Ready Interrupt

The transmit data-ready interrupt (XDATA) is generated if XDATA is 1 in the MCASP_TXSTAT register and XDATA is enabled in MCASP_EVTCTLX. Section 23.8.4.10.1, *Data Ready Status and Event/Interrupt Generation*, provides details on when XDATA is set in the MCASP_TXSTAT register.

A transmit-start-of-frame interrupt (XSTAFRM) is triggered by the recognition of a transmit frame sync.

A transmit-last-slot interrupt (XLAST) is a qualified version of the data-ready interrupt (XDATA). It has the same behavior as the data-ready interrupt, but is further qualified by having the data requested belonging to the last slot (the slot that just ended is the next-to-last TDM slot, the current slot is the last slot).

23.8.4.11.2 Error Interrupt

Upon detection, the following error conditions generate interrupt flags:

In the transmit status register (MCASP_TXSTAT):

- Transmit underrun (XUNDRN)
- Transmit DMA error (XDMAERR)

Each interrupt source also has a corresponding enable bit in the transmit interrupt control register (MCASP_EVTCTLX). If the enable bit is set, an interrupt is requested when the interrupt flag is set in MCASP_TXSTAT. If the enable bit is not set, no interrupt request is generated. However, the interrupt flag may be polled.

23.8.4.12 DMA Requests

The McASP can generate one DMA request to the sDMA and eDMA controllers to transmit data (MCASP_AXEVT).

A DMA request to transmit data is generated if the XDATDMA bit in the MCASP_TXEVTCTL register is cleared.

23.8.4.13 Audio Mute (AMUTE) Function

The McASP includes an automatic audio mute function (see Figure 23-200) that asserts, in hardware, the AMUTE pin to a preprogrammed output state, as selected by the MUTEN bit in the audio mute control register (MCASP_AMUTE). The AMUTE pin is asserted when one of the interrupt flags is set or an external device issues an error signal on the abe_mcasp_amutein input. Typically, the abe_mcasp_amutein input is shared with a device interrupt pin.

The abe_mcasp_amutein input allows the on-chip logic to consider a mute input from other devices in the system so that all errors may be considered. The abe_mcasp_amutein input has a programmable polarity to allow it to adapt to different devices, as selected by the INPOL bit in the MCASP_AMUTE register, and it must be explicitly enabled.

In addition to the external abe_mcasp_amutein input, the abe_mcasp_amute pin output may be asserted when one of the error interrupt flags is set and its mute function is enabled in the MCASP_AMUTE register.

When one or more errors are detected and enabled, the abe_mcasp_amute pin is driven to an active state that is selected by MUTEN in the MCASP_AMUTE register. The active polarity of the AMUTE pin is programmable by the MUTEN bit (the inactive polarity is the opposite of the active polarity). The abe_mcasp_amute pin remains driven active until software clears all the error interrupt flags that are enabled to mute, and until the abe_mcasp_amutein is inactive.

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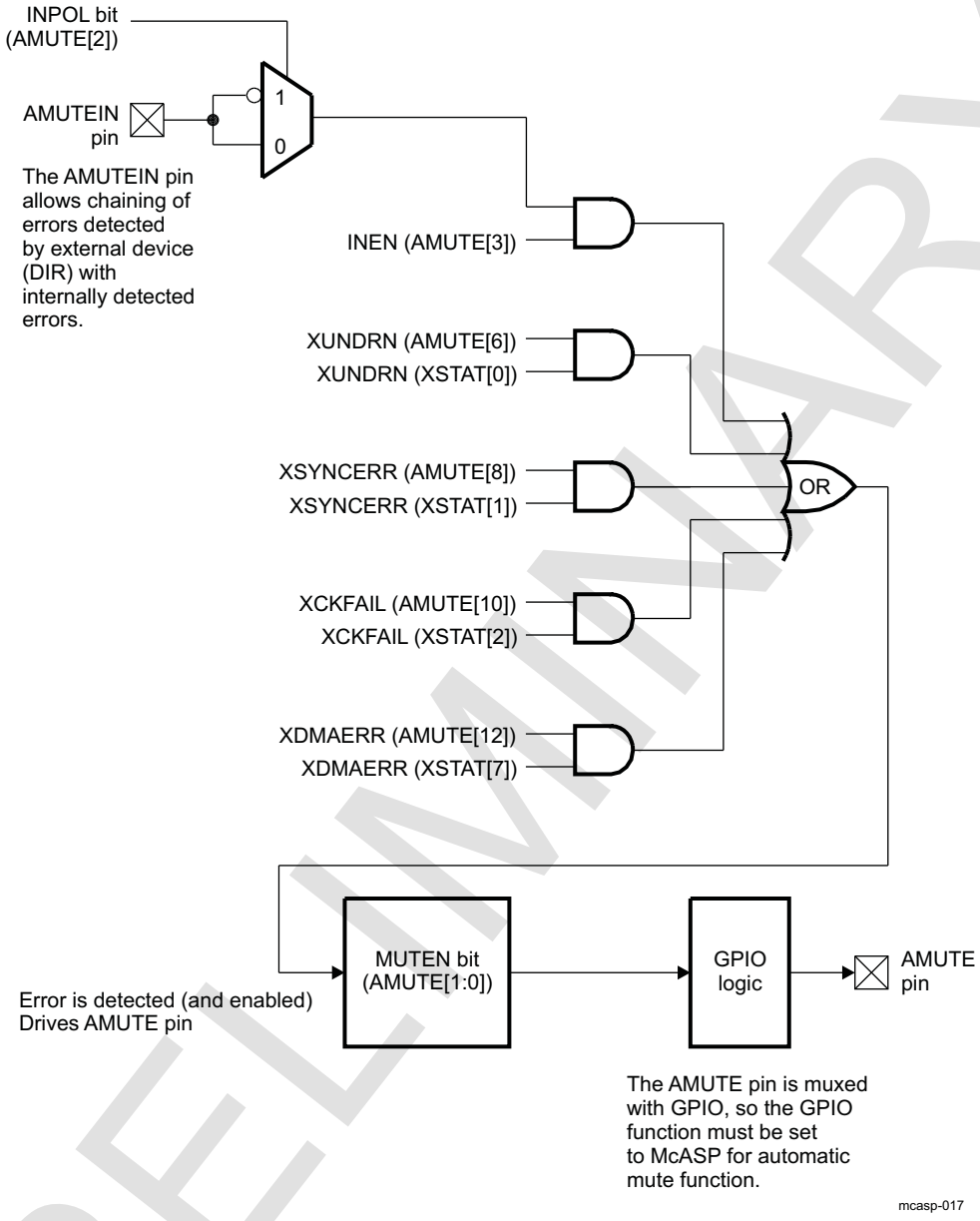
Figure 23-200. Audio Mute (AMUTE) Block Diagram



23.8.4.14 Error Reporting

The McASP includes error-checking capability for the serial protocol and data underrun. In addition, the McASP includes a timer that continually measures the high-frequency master clock every 32 AHCLKX clock cycles. The value of the timer can be read to get a measurement of the clock frequency and has a minimum and maximum range setting that can set an error flag if the master clock goes out of a specified range.

When one or more errors (software selectable) are detected or the abe_mcasp_amutein input pin is asserted, the abe_mcasp_amute output pin may be asserted to a high or low level to immediately mute the audio output. In addition, an interrupt can be generated if desired, based on one or more error sources.

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23.8.4.14.1 Buffer Underrun Error –Transmitter

A buffer underrun occurs when the serializer is instructed by the transmit state-machine to transfer data from MCASP_TXBUF0 to XRSR, but MCASP_TXBUF0 has not yet been written with new data since the last time the transfer occurred. When this occurs, the transmit state-machine sets the XUNDRN flag.

An underrun is checked only once per time slot. The MCASP_TXSTAT[0] XUNDRN flag is set when an underrun condition occurs. Once set, the XUNDRN flag remains set until the host explicitly writes 1 to the XUNDRN bit to clear it.

A pair of BMC zeros is shifted out when an underrun occurs (four bit times at 128 bfs). By shifting out a pair of zeros, a clock can be recovered on the receiver. To recover, reset the McASP and restart with the proper initialization.

23.8.4.14.2 DMA Error –Transmitter

A transmit DMA error, as indicated by the XDMAERR flag in the MCASP_TXSTAT register, occurs when the DMA (or MPU) writes more words to the data port of the McASP than it should.

XDMAERR indicates that the DMA (or MPU) wrote too many words to the McASP for a given transmit DMA event. Writing too few words results in a transmit underrun error setting XUNDRN in MCASP_TXSTAT.

While XDMAERR occurs infrequently, an occurrence indicates a serious loss of synchronization between the McASP and the DMA or MPU. The McASP transmitter and the DMA must be reinitialized to resynchronize them.

23.8.4.14.3 Clock Failure Detection

23.8.4.14.3.1 Clock Failure Check Startup

It is initially expected of the clock failure circuits to generate an error until at least one measurement is taken. Therefore, the clock failure interrupts, clock switch, and mute functions should not be enabled immediately, but only after a specific startup procedure.

The start the transmit clock failure check procedure:

1. Configure the transmit clock failure detect logic (XMIN, XMAX, XPS) in the transmit clock check control register (MCASP_TXCLKCHK).
2. Clear the transmit clock failure flag (XCKFAIL) in the transmit status register (MCASP_TXSTAT).
3. Wait until the first measurement is taken (32 AHCLKX clock periods).
4. Verify that no clock failure is detected.
5. Repeat Step 2 through Step 4 until the clock is running and is no longer issuing clock failure errors.
6. After the transmit clock is measured and falls within the acceptable range, the following can be enabled:
   (a) The transmit clock failure interrupt enable bit (XCKFAIL) in the transmitter interrupt control register (MCASP_EVTCTLX)
   (b) The mute option (XCKFAIL) in the mute control register (MCASP_AMUTE)

23.8.4.14.3.2 Transmit Clock Failure Check and Recovery

The transmit clock failure check circuit (see Figure 23-201) works off the internal McASP system clock and the external high-frequency serial clock (abe_mcasp_ahclkx). It continually counts the number of system clocks for every 32 high-rate serial clock (abe_mcasp_ahclkx) periods, and stores the count in XCNT of the transmit clock check control register (MCASP_TXCLKCHK) every 32 high-rate serial clock cycles.

The logic compares the count against a user-defined minimum allowable boundary (XMIN), and automatically flags an interrupt (XCKFAIL in MCASP_TXSTAT) when an out-of-range condition occurs. An

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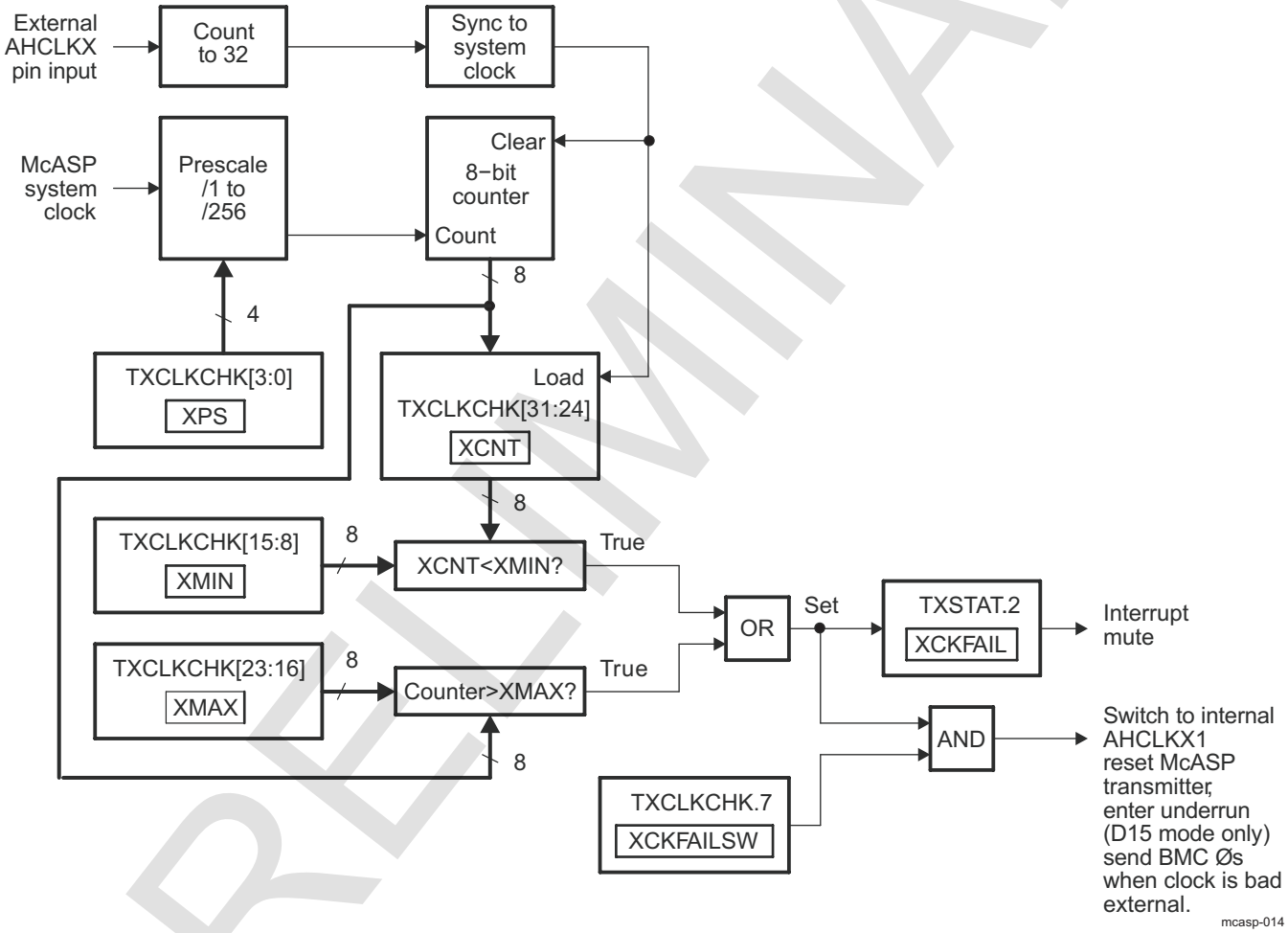
out-of-range minimum condition occurs when the count is less than XMIN. The logic continually compares the current count (from the running system clock counter) to the maximum allowable boundary (XMAX). This is so that if the external clock completely stops, the counter value is not copied to XCNT. An out-of-range maximum condition occurs when the count is greater than XMAX. The XMIN and XMAX fields are 8-bit unsigned values, and the comparison is performed using unsigned arithmetic.

An out-of-range count may indicate that an unstable clock was detected or that the audio source has changed and a new sample rate is being used.

For the transmit clock failure check circuit to operate correctly, the high-frequency serial clock divider must be taken out of reset.

If a clock failure is detected, the transmit clock failure flag (XCKFAIL) in MCASP_TXSTAT is set. This causes an interrupt if the transmit clock failure interrupt enable bit (XCKFAIL) in MCASP_EVTCTLX is set.

Figure 23-201. Transmit Clock Failure Detection Circuit Block Diagram



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23.8.5 McASP Low-Level Programming Model

This section describes the low-level hardware programming sequences for the configuration and use of the McASP module.

23.8.5.1 Global Initialization

23.8.5.1.1 Surrounding Modules Global Initialization

This section identifies the requirements for initializing the surrounding modules when the McASP module is used for the first time after a device reset. This initialization of surrounding modules is based on the integration and environment of the McASP (for more information, see the Section 23.8.3 , *McASP Integration*, and Section 23.8.2, *McASP Environment*).

Table 23-572, describes the global initialization of surrounding modules.

Table 23-572. Global Initialization of Surrounding Modules

Surrounding Modules	Comments
PRCM	Module functional and interface clocks must be enabled. (See Chapter 3, *Power, Reset, and Clock Management*.)
Control module	Module-specific pad muxing and other pad configurations must be set in the control module. (See Chapter 18, *Control Module*).
(Optional) Cortex-A9 MPU INTC or DSP INTC	INTC configuration must be done to enable the interrupts from the McASP. (See Chapter 17, *Interrupt Controllers*).
(Optional) sDMA (or eDMA or aDMA)	DMA configuration must be done to enable the McASP DMA data channel requests.
(Optional) ABE_L4 and L3 Interconnects	For more information about the interconnect configuration, see Chapter 13, *Interconnect*.

NOTE: The MPU/DSP INTC and the sDMA/eDMA/aDMA configurations are required when the interrupt and DMA-based communication modes are used.

23.8.5.1.2 McASP Global Initialization

23.8.5.1.2.1 Main Sequence – McASP Global Initialization

The procedure in Table 23-573 initializes the McASP after a power-on reset (POR).

Table 23-573. McASP Global Initialization

Step	Register/Bit Field/Programming Model	Value
Apply software reset to different McASP components.	MCASP_GBLCTL[12:8]	0x00
Poll the bits to ensure the active reset value (0x00) is successfully latched into the register.	MCASP_GBLCTL[12:8]	=0x00
Configure the local power management.	MCASP_SYSCONFIG[1:0] IDLE_MODE	0x-
Configure the transmit format unit.	See Section 23.8.5.1.2.2.	
Configure the transmit frame sync generator.	See Section 23.8.5.1.2.3.	
Configure the transmit clock generator.	See Section 23.8.5.1.2.4.	
Configure the TDM sequencer—set all slots active.	MCASP_TXTDM[31:0] XTDMS	0xFFFF FFFF
Configure the serializer for transmit mode operation.	MCASP_XRSRCTL0[1:0] SRMOD	0x1
Configure the McASP pins functionality.	See Section 23.8.5.1.2.5.	
Configure the McASP mute input/output conditions.	See Table 23-578.	
Enable the McASP DIT-transmission mode.	MCASP_TXDITCTL[0] DITEN	0x1
Configure DIT-specific subframe fields.	See Table 23-579.	

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Table 23-573. McASP Global Initialization (continued)

Step	Register/Bit Field/Programming Model	Value
Release from reset state the divider that outputs the abe_mcasp_ahclkx clock.(1)	MCASP_GBLCTL[9] XHCLKRST	0x1
Poll the bit to ensure that it is successfully latched in the register.	MCASP_GBLCTL[9] XHCLKRST	=0x1
Release from reset state the divider that outputs the abe_mcasp_aclkx clock. (1)	MCASP_GBLCTL[8] XCLKRST	0x1
Poll the bit to ensure that it is successfully latched in the register.	MCASP_GBLCTL[8] XCLKRST	=0x1

(1) During reset state the local McASP internal clock dividers maintain a 1:1 ratio at their outputs. The values stored in the MCASP_AHCLKX and MCASP_ ACLKX registers are ignored; hence, the transmission clock does not stop during the reset state of the dividers.

23.8.5.1.2.2 Subsequence – Transmit Format Unit Configuration

The procedure in Table 23-574 configures the transmit frame format unit of the McASP module.

NOTE:

- The first transmit data bit always has a 0-bit delay.
- The bitstream is always transmitted in least-significant-bit (LSB)-first order.
- Pad value for extra bits in a certain slot is always 0.

Table 23-574. Transmit Format Unit Configuration

Step	Register/Bit Field/Programming Model	Value
Configure the slot size to 32 bits.	MCASP_TXFMT[7:4] XSSZ	0xF
IF: the MPU or DMA data to transmit is left- aligned	Software test condition	
Set data mask in the range 0xFFFF FF00 – 0xFFFF 0000.	MCASP_TXMASK[31:0] XMASK	0x-
Rotate data right by 8-bit positions.	MCASP_TXFMT[2:0] XROT	0x2
ELSE		
Set data mask in the range 0x00FF FFFF– 0x0000 FFFF.	MCASP_TXMASK[31:0] XMASK	0x-
Rotate data right by 0-bit positions.	MCASP_TXFMT[2:0] XROT	0x0
ENDIF		

23.8.5.1.2.3 Subsequence – Transmit Frame Synchronization Generator Configuration

The procedure in Table 23-575 configures the transmit frame synchronization generator of the McASP module.

NOTE: The frame synchronization signal is always rising-edge active and always has a single-bit width.

Table 23-575. Transmit Frame-Synchronization Generator Configuration

Step	Register/Bit Field/Programming Model	Value
Select 384-slot size block.	MCASP_TXFMCTL[15:7] XMOD	0x180
Select internally-generated transmit frame sync.	MCASP_TXFMCTL[1] FSXM	0x1

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23.8.5.1.2.4 Subsequence – Transmit Clock Generator Configuration

NOTE: By default, the ACLKX and AHCLKX clocks are generated only from the McASP internal clock source.

The procedure in Table 23-576 configures the transmit clock generator of the McASP module.

Table 23-576. Transmit Clock Generator Configuration

Step	Register/Bit Field/Programming Model	Value
Set the divisor for the internally generated high frequency clock– abe_mcasp_ahclkx.	MCASP_AHCLKXCTL[11:0] HCLKXDIV	0x-
Set he divisor for the internally generated transmission clock– abe_mcasp_aclkx.	MCASP_ACLKXCTL[4:0] CLKXDIV	0x-
Configure the transmit clock failure detect logic.	See Section 23.8.4.14.3.1, *Clock Failure Check Startup*.	

23.8.5.1.2.5 Subsequence—McASP Pins Functional Configuration

The procedure in Table 23-577 configures the McASP pins for McASP functionality.

Table 23-577. McASP Pins Functional Configuration

Step	Register/Bit Field/Programming Model	Value
Configure module different pins to have McASP functionality.	MCASP_PFUNC[31:0]	0x0
Configure the McASP pins as outputs: abe_mcasp_afsx abe_mcasp_ahclkx abe_mcasp_aclkx abe_mcasp_amute abe_mcasp_axr	MCASP_PDIR[28] AFSX; MCASP_PDIR[27] AHCLKX; MCASP_PDIR[26] ACLKX; MCASP_PDIR[25] AMUTE; MCASP_PDIR[0] AXR0;	0x1 0x1 0x1 0x1 0x1

23.8.5.1.2.6 Subsequence – McASP Mute Input/Output Trigger Condition Settings

The procedure in Table 23-578 configures the behavior of the mute associated I/Os and different trigger conditions for the McASP mute output functionality.

Table 23-578. McASP Mute Input/Output Trigger Condition Settings

Step	Register/Bit Field/Programming Model	Value
Optional: Select to drive AMUTE active enable bit on transmit DMA error.	MCASP_AMUTE[12] XDMAERR	0x1
Optional: Select to drive AMUTE active enable bit on transmit clock failure.	MCASP_AMUTE[10] XCKFAIL	0x1
Optional: Select to drive AMUTE active enable bit on transmit frame synchronization error.	MCASP_AMUTE[8] XSYNCERR	0x1
Optional: Select to drive AMUTE active enable bit on transmit underrun error.	MCASP_AMUTE[6] XUNDRN	0x1
Optional: Enable sensitivity of the abe_mcasp_amute output to abe_mcasp_amutein error source.	MCASP_AMUTE[3] INEN	0x1
Optional: Select the abe_mcasp_amutein input polarity.	MCASP_AMUTE[2] INPOL	0x1
Optional: Configure the behavior of the abe_mcasp_amute output.	MCASP_AMUTE[1:0] MUTEN	0x1

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23.8.5.1.2.7 Subsequence – DIT-Specific Subframe Fields Configuration

NOTE: The McASP integrated in the device supports only the DIT transmission mode that uses the S/PDIF protocol.

The procedure in Table 23-579 configures the DIT-specific subframe fields as part of the S/PDIF format data.

Table 23-579. DIT-Specific Subframe Fields Configuration

Step	Register/Bit Field/Programming Model	Value
Configure the valid bit value for odd time slots.	MCASP_TXDITCTL[3] VB	0x-
Configure the valid bit value for even time slots.	MCASP_TXDITCTL[2] VA	0x-
Configure the user data bit for each subframe A and B in a 384-slot S/PDIF block.	MCASP_DITUDRAi[31:0] DITUDRAi, where i = 0 to 5 MCASP_DITUDRBi[31:0] DITUDRBi, where i= 0 to 5	0x- 0x-
Configure the channel status bit for each subframe A and B in a 384-slot S/PDIF block.	MCASP_DITCSRAi[31:0] , where i = 0 to 5 MCASP_DITCSRBi[31:0] , where i = 0 to 5	0x- 0x-

23.8.5.2 Operational Modes Configuration

23.8.5.2.1 McASP DIT Transmission Mode

23.8.5.2.1.1 Main Sequence – McASP DIT Polling Transmission Method

Figure 23-202 shows the McASP DIT polling method.

NOTE:

- The McASP polling transmission model considers the MPU/DSP as the source of audio data for the McASP transmission buffer.
- The DMA request is disabled and the XDMAERR event is not analyzed.
- The flow chart shown in Figure 23-202 shows the sequence for transmitting one DIT frame.

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Figure 23-202. McASP DIT Transmission Polling Method

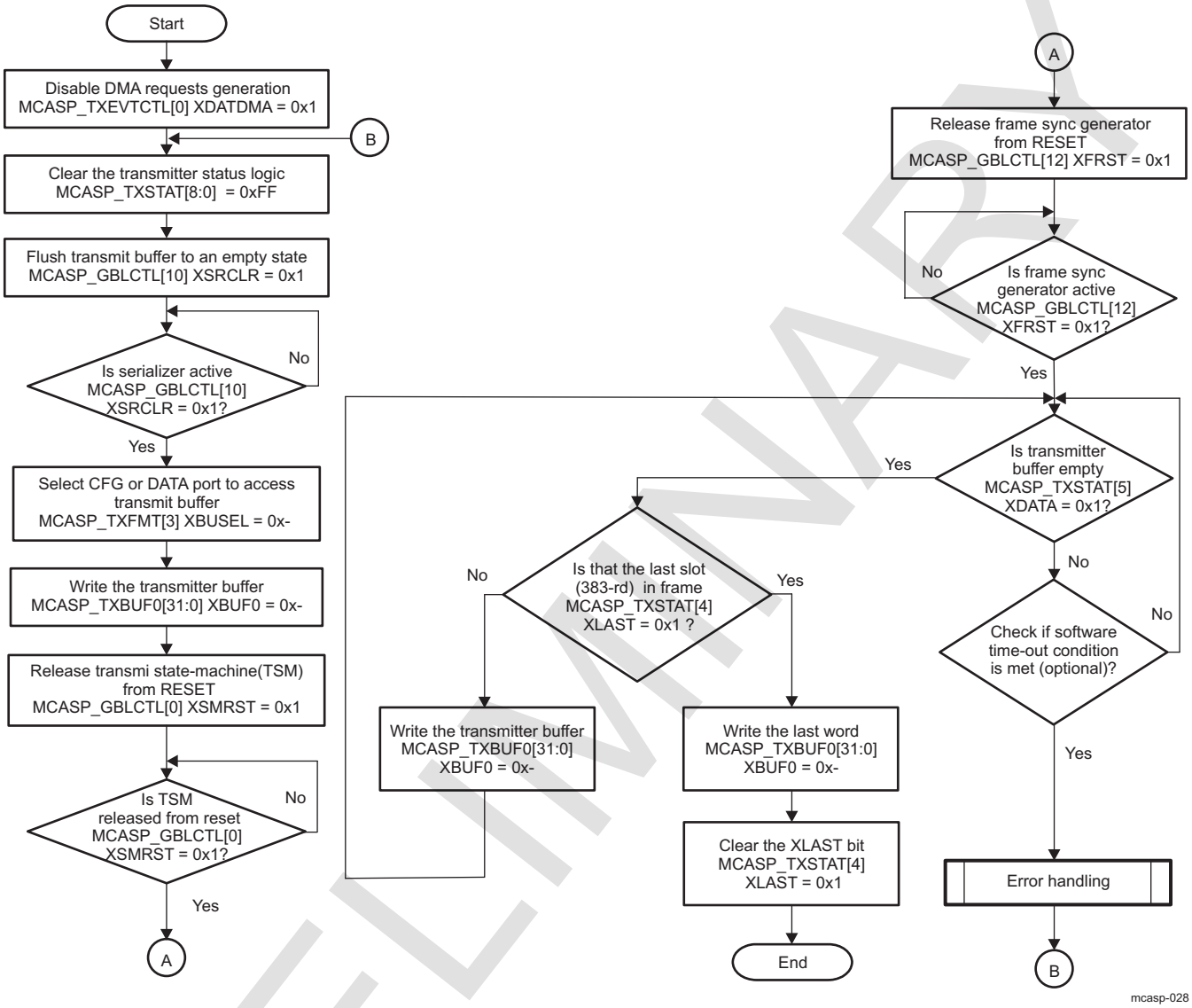

Table 23-580 summarizes the register call for the polling mode.

Table 23-580. Register Call Summary for Main Sequence – McASP DIT Transmission Polling Method

Register Name	Register Name	Register Name	Register Name	Register Name
MCASP_TXSTAT	MCASP_GBLCTL	MCASP_TXBUF0	MCASP_TXFMT	MCASP_TXEVTCTL

Table 23-581 summarizes the subprocess call for the polling mode.

Table 23-581. Subprocess Call Summary for Main Sequence – McASP DIT Transmission Polling Method

Subprocess Name	Cross-Reference
Error handling	Figure 23-206

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23.8.5.2.1.2 Main Sequence – McASP DIT Interrupt Transmission Method

Figure 23-203 shows the initial setup for interrupt-based transmission.

Figure 23-203. Subsequence – DIT Transmission Startup Procedure

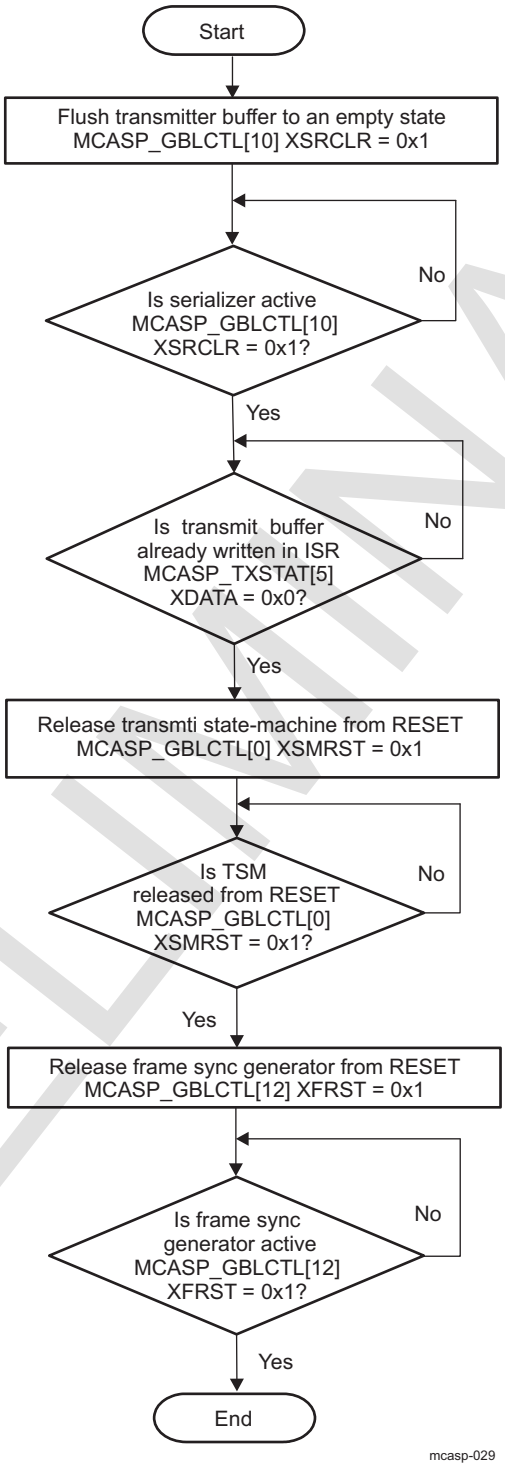

Table 23-582 shows the configuration of the McASP using the McASP DIT interrupt method for transmission.

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Table 23-582. McASP Interrupt Transmission Model

Step	Register/Bit Field/Programming Model	Value
Select the CFG or DATA port to access the transmit buffer.	MCASP_TXFMT[3] XBUSEL	0x-
Disable DMA requests generation.	MCASP_TXEVTCTL[0] XDATDMA	0x1
Clear the transmitter status logic.	MCASP_TXSTAT[8:0]	0xFF
Enable the data ready event transmit interrupt.	MCASP_EVTCTLX[5] XDATA	0x1
Optional: Enable the transmit error event interrupts.	MCASP_EVTCTLX[2] XCKFAIL MCASP_EVTCTLX[1] XSYNCERR MCASP_EVTCTLX[0] XUNDRN	0x1 0x1 0x1
Optional: Enable the start of frame interrupt. Optional: Enable the last slot data interrupt.	MCASP_EVTCTLX [7] XSTAFRM MCASP_EVTCTLX[4] XLAST	0x1 0x1
Disable the DMA error event.	MCASP_EVTCTLX[7] XDMAERR	0x0
DIT transmission startup procedure	See Figure 23-203.	

Table 23-583 summarizes the register call to initialize the McASP to transmit using interrupt events.

Table 23-583. Register Call Summary for Subsequence – McASP DIT Transmission Startup Procedure

Register Name	Register Name
MCASP_GBLCTL	MCASP_TXBUF0

23.8.5.2.1.3 Main Sequence –McASP DIT DMA Transmission Method

Table 23-584 shows the configuration of the McASP using the DMA method for transmission. Possible interrupt error event servicing is also considered. Table 23-583 shows the initial setup for DMA-based transmission.

NOTE: Because of the DATA port burst access capability with the DMA method, It is preferable for transfers to be initiated through the DATA port rather than through the CFG port.

Table 23-584. McASP DMA Transmission Model with Interrupt Events Servicing

Step	Register/Bit Field/Programming Model	Value
Select DATA port to access the transmit buffer.	MCASP_TXFMT[3] XBUSEL	0x0
Enable the DMA requests generation.	MCASP_TXEVTCTL[0] XDATDMA	0x0
Clear the transmitter status logic.	MCASP_TXSTAT[8:0]	0xFF
Enable the DMA error event.	MCASP_EVTCTLX[7] XDMAERR	0x1
Optional: Enable the transmit error event interrupts.	MCASP_EVTCTLX[2] XCKFAIL MCASP_EVTCTLX[1] XSYNCERR MCASP_EVTCTLX[0] XUNDRN	0x1 0x1 0x1
Optional: Enable the start of frame interrupt. Optional: Enable the last slot data interrupt.	MCASP_EVTCTLX [7] XSTAFRM MCASP_EVTCTLX[4] XLAST	0x1 0x1
Disable the data ready event transmit interrupt.	MCASP_EVTCTLX[5] XDATA	0x0
DMA transmission procedure	See Section 23.8.5.2.1.4.	

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23.8.5.2.1.4 Susbsequence – DIT DMA Transmission Procedure

Figure 23-204 shows the McASP initial setup when the DMA method is used for transmission.

Figure 23-204. Subsequence – DIT DMA Transmission Procedure

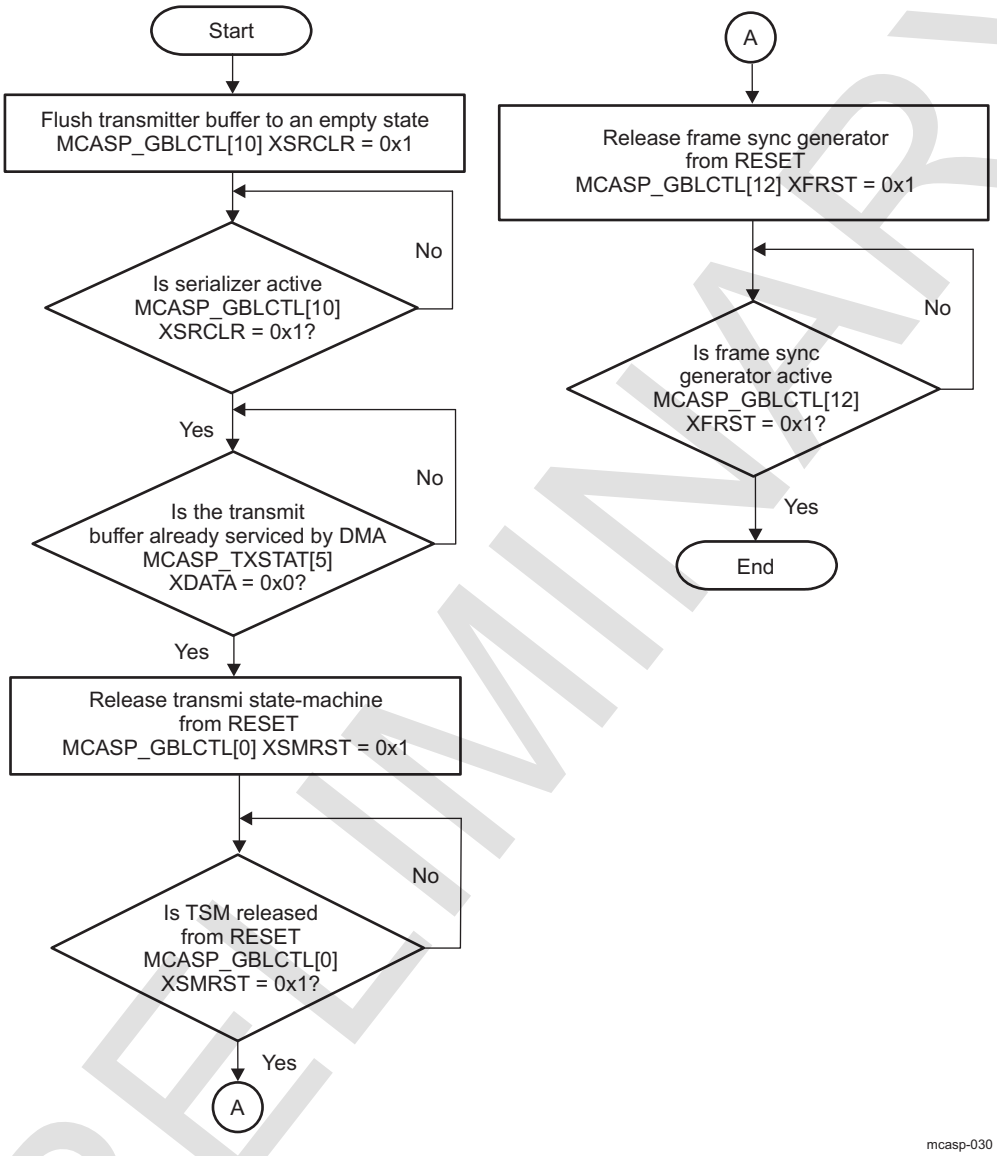

Table 23-585 shows the register call summary for the McASP DMA transmission procedure subsequence.

Table 23-585. Register Call Summary for Subsequence – McASP DMA Transmission Procedure

Register Name	Register Name
MCASP_TXSTAT	MCASP_GBLCTL

23.8.5.2.2 McASP Event Servicing

23.8.5.2.2.1 McASP Interrupt Events Servicing

Figure 23-205 shows the flow of interrupt events servicing for the McASP module.

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Figure 23-205. McASP Interrupt Events Servicing

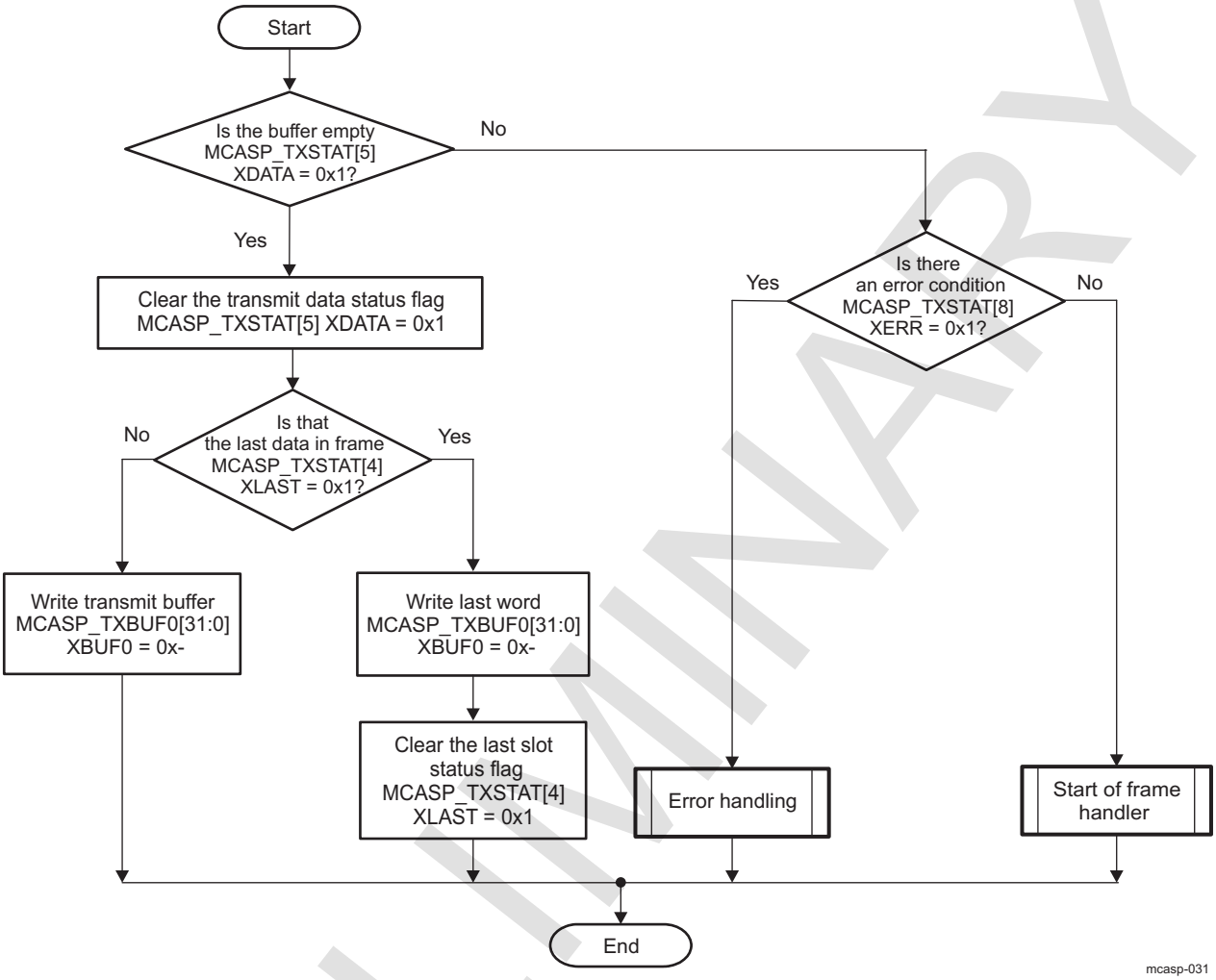

Table 23-586 lists the register call summary for the interrupt event servicing.

Table 23-586. Register Call Summary for McASP Interrupt Events Servicing

Register Name	Register Name
MCASP_TXSTAT	MCASP_TXBUF0

Table 23-587 lists the subprocess call summary for interrupt events servicing.

Table 23-587. Subprocess Call Summary for Interrupt Events Servicing

Subprocess Name	Cross-Reference
Error handling	Figure 23-206
Start of frame handling	Section 23.8.4.11.1

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23.8.5.2.2.2 Subsequence – Error Handling

Figure 23-206 shows the error handling schema for the McASP, which can be implemented as part of the interrupt service routine or as part of polling sequence.

Figure 23-206. McASP Error Handling

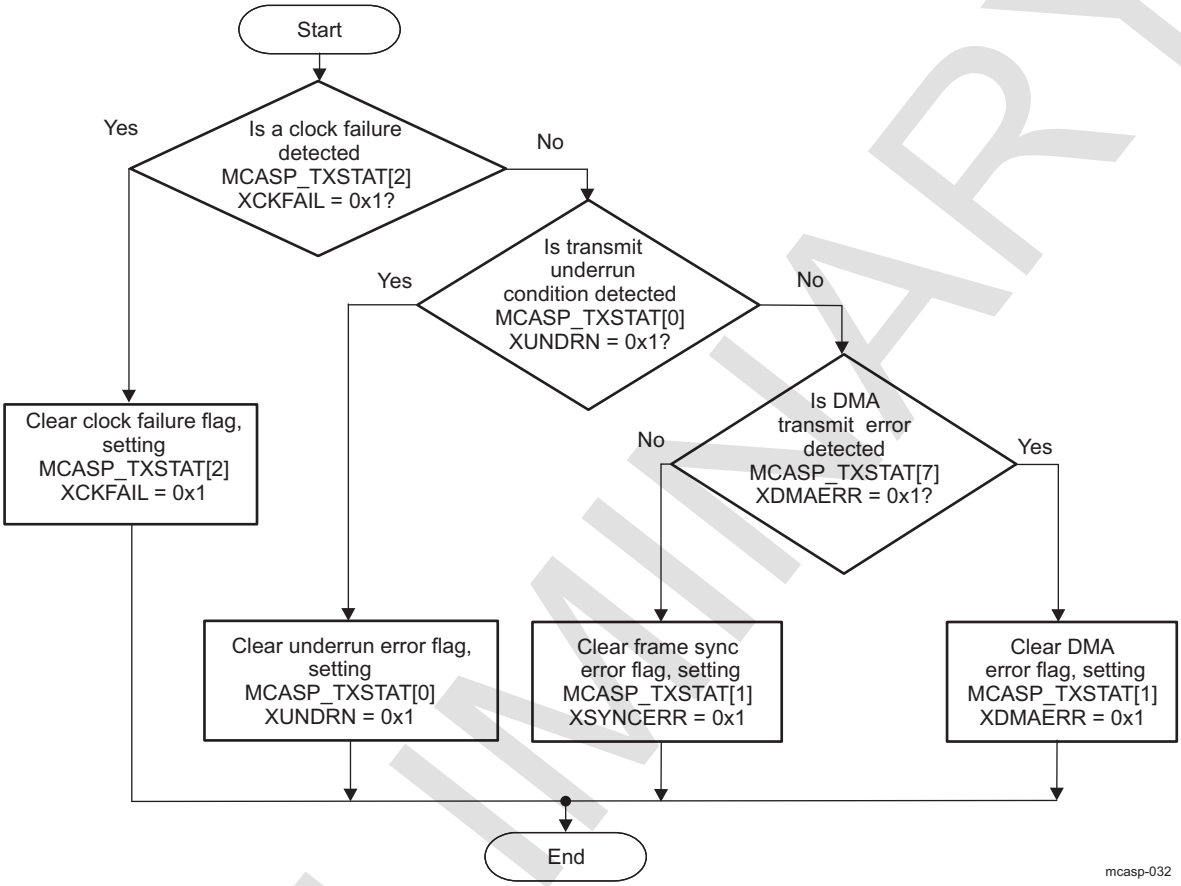

Table 23-588 lists the register call summary for the McASP error handling.

Table 23-588. Register Call Summary for McASP Error Handling

Register Name
MCASP_TXSTAT

NOTE:

- For more information about clock failure handling, see Section 23.8.4.14.3.
- For more information about transmit buffer underrun handling, see Section 23.8.4.14.1.
- For more information about DMA error handling, see Section 23.8.4.14.2.

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23.8.6 McASP Register Manual

23.8.6.1 McASP Instance Summary

Table 23-589 summarizes the McASP instances.

Table 23-589. McASP Instance Summary

Module Name	Base Address L3 Interconnect	Base Address Cortex-A9 Private Access	Base Address DSP Private Access	Size
McASP	0x4902 8000	0x4012 8000	0x01D2 8000	4KB

NOTE: Private access is an access that does not use the L3 / L4 interconnects.

23.8.6.2 McASP Registers

23.8.6.2.1 McASP Register Summary

Table 23-590 summarizes the McASP register mapping.

Table 23-590. McASP Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	Physical Address L3 Interconnect	Physical Address Cortex-A9 Private Access	Physical Address DSP Private Access
MCASP_PID	R	32	0x0000 0000	0x4902 8000	0x4012 8000	0x01D2 8000
MCASP_SYSCONFIG	RW	32	0x0000 0004	0x4902 8004	0x4012 8004	0x01D2 8004
MCASP_PFUNC	RW	32	0x0000 0010	0x4902 8010	0x4012 8010	0x01D2 8010
MCASP_PDIR	RW	32	0x0000 0014	0x4902 8014	0x4012 8014	0x01D2 8014
MCASP_PDOUT	RW	32	0x0000 0018	0x4902 8018	0x4012 8018	0x01D2 8018
MCASP_PDIN	R	32	0x0000 001C	0x4902 801C	0x4012 801C	0x01D2 801C
MCASP_PDSET	W	32	0x0000 001C	0x4902 801C	0x4012 801C	0x01D2 801C
MCASP_PDCLR	RW	32	0x0000 0020	0x4902 8020	0x4012 8020	0x01D2 8020
RESERVED	RW	32	0x0000 0030	0x4902 8030	0x4012 8030	0x01D2 8030
RESERVED	RW	32	0x0000 0034	0x4902 8034	0x4012 8034	0x01D2 8034
RESERVED	RW	32	0x0000 0038	0x4902 8038	0x4012 8038	0x01D2 8038
MCASP_GBLCTL	RW	32	0x0000 0044	0x4902 8044	0x4012 8044	0x01D2 8044
MCASP_AMUTE	RW	32	0x0000 0048	0x4902 8048	0x4012 8048	0x01D2 8048
RESERVED	RW	32	0x0000 004C	0x4902 804C	0x4012 804C	0x01D2 804C
MCASP_TXDITCTL	RW	32	0x0000 0050	0x4902 8050	0x4012 8050	0x01D2 8050
RESERVED	RW	32	0x0000 0060	0x4902 8060	0x4012 8060	0x01D2 8060
RESERVED	RW	32	0x0000 0064	0x4902 8064	0x4012 8064	0x01D2 8064
RESERVED	RW	32	0x0000 0068	0x4902 8068	0x4012 8068	0x01D2 8068
RESERVED	RW	32	0x0000 006C	0x4902 806C	0x4012 806C	0x01D2 806C
RESERVED	RW	32	0x0000 0070	0x4902 8070	0x4012 8070	0x01D2 8070
RESERVED	RW	32	0x0000 0074	0x4902 8074	0x4012 8074	0x01D2 8074
RESERVED	RW	32	0x0000 0078	0x4902 8078	0x4012 8078	0x01D2 8078
RESERVED	RW	32	0x0000 007C	0x4902 807C	0x4012 807C	0x01D2 807C
RESERVED	RW	32	0x0000 0080	0x4902 8080	0x4012 8080	0x01D2 8080
RESERVED	R	32	0x0000 0084	0x4902 8084	0x4012 8084	0x01D2 8084
RESERVED	RW	32	0x0000 0088	0x4902 8088	0x4012 8088	0x01D2 8088
RESERVED	RW	32	0x0000 008C	0x4902 808C	0x4012 808C	0x01D2 808C

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Table 23-590. McASP Register Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	Physical Address L3 Interconnect	Physical Address Cortex-A9 Private Access	Physical Address DSP Private Access
RESERVED	RW	32	0x0000 00A0	0x4902 80A0	0x4012 80A0	0x01D2 80A0
MCASP_TXMASK	RW	32	0x0000 00A4	0x4902 80A4	0x4012 80A4	0x01D2 80A4
MCASP_TXFMT	RW	32	0x0000 00A8	0x4902 80A8	0x4012 80A8	0x01D2 80A8
MCASP_TXFMCTL	RW	32	0x0000 00AC	0x4902 80AC	0x4012 80AC	0x01D2 80AC
MCASP_ACLKXCTL	RW	32	0x0000 00B0	0x4902 80B0	0x4012 80B0	0x01D2 80B0
MCASP_AHCLKXCTL	RW	32	0x0000 00B4	0x4902 80B4	0x4012 80B4	0x01D2 80B4
MCASP_TXTDM	RW	32	0x0000 00B8	0x4902 80B8	0x4012 80B8	0x01D2 80B8
MCASP_EVTCTLX	RW	32	0x0000 00BC	0x4902 80BC	0x4012 80BC	0x01D2 80BC
MCASP_TXSTAT	RW	32	0x0000 00C0	0x4902 80C0	0x4012 80C0	0x01D2 80C0
MCASP_TXTDMSLOT	R	32	0x0000 00C4	0x4902 80C4	0x4012 80C4	0x01D2 80C4
MCASP_TXCLKCHK	RW	32	0x0000 00C8	0x4902 80C8	0x4012 80C8	0x01D2 80C8
MCASP_TXEVTCTL	RW	32	0x0000 00CC	0x4902 80CC	0x4012 80CC	0x01D2 80CC
RESERVED	RW	32	0x0000 00D0	0x4902 80D0	0x4012 80D0	0x01D2 80D0
MCASP_DITCSRAi (1)	RW	32	0x0000 0100 + (0x04*i)	0x4902 8100 + (0x04*i)	0x4012 8100 + (0x04*i)	0x01D2 8100 + (0x04*i)
MCASP_DITCSRBi (1)	RW	32	0x0000 0118 + (0x04*i)	0x4902 8118 + (0x04*i)	0x4012 8118 + (0x04*i)	0x01D2 8118 + (0x04*i)
MCASP_DITUDRAi (1)	RW	32	0x0000 0130 + (0x04*i)	0x4902 8130 + (0x04*i)	0x4012 8130 + (0x04*i)	0x01D2 8130 + (0x04*i)
MCASP_DITUDRBi (1)	RW	32	0x0000 0148 + (0x04*i)	0x4902 8148 + (0x04*i)	0x4012 8148 + (0x04*i)	0x01D2 8148 + (0x04*i)
MCASP_XRSRCTL0	RW	32	0x0000 0180	0x4902 8180	0x4012 8180	0x01D2 8180
RESERVED	RW	32	0x0000 0184 + (0x04*j) (2)	0x4902 8184 + (0x04*j)	0x4012 8184 + (0x04*j)	0x01D2 8184 + (0x04*j)
MCASP_TXBUF0	RW	32	0x0000 0200	0x4902 8200	0x4012 8200	0x01D2 8200
RESERVED	RW	32	0x0000 0204 + (0x04*k) (3)	0x4902 8204 + (0x04*k)	0x4012 8204 + (0x04*k)	0x01D2 8204 + (0x04*k)

(1) i = 0 to 5 for McASP_L3Interconnect
i = 0 to 5 for McASP_Cortex-A9
i = 0 to 5 for McASP_DSP

(2) j = 0 to 14

(3) k = 0 to 30

NOTE: The address locations listed in Table 23-590, *McASP Register Mapping Summary*, are relevant for accessing all McASP configuration registers and McASP_TXBUF0 registers through the McASP peripheral configuration (CFG) port.

McASP DAT allows the L3-interconnect, DSP subsystem, and MPU to access the McASP_TXBUF0 register at locations 0x4902 A200, 0x01D2 A200, and 0x4012 A200, respectively.

23.8.6.2.2 McASP Register Description

Table 23-591 through Table 23-645 describe the individual register bits.

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Table 23-591. MCASP_PID

Address Offset	0x0000 0000		
Physical Address	0x4902 8000 0x4012 8000 0x01D2 8000	**Instance**	MCASP_L3 MCASP_CORTEX-A9 MCASP_DSP
Description	Peripheral identification register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP revision	R	TI internal data

Table 23-592. Register Call Summary for Register MCASP_PID

Multichannel Audio Serial Port

- McASP Register Summary: [0]

Table 23-593. MCASP_SYSCONFIG

Address Offset	0x0000 0004		
Physical Address	0x4902 8004 0x4012 8004 0x01D2 8004	**Instance**	MCASP_L3 MCASP_CORTEX-A9 MCASP_DSP
Description	Power idle module configuration register.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														IDLE_MODE	

Bits	Field Name	Description	Type	Reset
31:2	RESERVED	Reserved	R	0x0000000
1:0	IDLE_MODE	0x0: Force-idle mode 0x1: No-idle mode 0x2: Smart-idle mode - default state 0x3: Reserved	RW	0x2

Table 23-594. Register Call Summary for Register MCASP_SYSCONFIG

Multichannel Audio Serial Port

- McASP Power Management: [0]
- McASP Global Initialization: [1]
- McASP Register Summary: [2]

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Table 23-595. MCASP_PFUNC

Address Offset	0x0000 0010		
Physical Address	0x4902 8010 0x4012 8010 0x01D2 8010	**Instance**	MCASP_L3 MCASP_CORTEX-A9 MCASP_DSP
Description	Specifies the function of the pins as either a McASP pin or a GPIO pin		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			AFSX	AHCLKX	ACLKX	AMUTE	RESERVED																								AXR0

Bits	Field Name	Description	Type	Reset
31:29	RESERVED	Reserved	RW	0
28	AFSX	Determines if abe_mcasp_afsx pin functions as McASP or GPIO. 0x0: Pin functions as McASP pin 0x1: Pin functions as GIO pin	RW	0
27	AHCLKX	Determines if abe_mcasp_ahclkx pin functions as McASP or GPIO. 0x0: Pin functions as McASP pin 0x1: Pin functions as GIO pin	RW	0
26	ACLKX	Determines if abe_mcasp_aclkx pin functions as McASP or GPIO. 0x0: Pin functions as McASP pin 0x1: Pin functions as GIO pin	RW	0
25	AMUTE	Determines if abe_mcasp_amute pin functions as McASP or GPIO. 0x0: Pin functions as McASP pin 0x1: Pin functions as GIO pin	RW	0
24:1	RESERVED	Reserved	RW	0x000
0	AXR0	Determines if abe_mcasp_axr pin functions as McASP or GPIO. 0x0: Pin functions as McASP pin 0x1: Pin functions as GIO pin	RW	0

Table 23-596. Register Call Summary for Register MCASP_PFUNC

Multichannel Audio Serial Port

- DIT Transfer Mode: [0]
- McASP Global Initialization: [1]
- McASP Register Summary: [2]
- McASP Register Description: [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14]

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Table 23-597. MCASP_PDIR

Address Offset	0x0000 0014		
Physical Address	0x4902 8014 0x4012 8014 0x01D2 8014	**Instance**	MCASP_L3 MCASP_CORTEX-A9 MCASP_DSP
Description	Pin direction register - specifies the direction of the McASP pins as either an input or an output pin. For the module to operate properly, configure them as outputs.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			AFSX	AHCLKX	ACLKX	AMUTE	RESERVED																								AXR0

Bits	Field Name	Description	Type	Reset
31:29	RESERVED	Reserved	RW	0
28	AFSX	Determines if abe_mcasp_afsx pin functions as an input or output. 0x0: Input 0x1: Output	RW	0
27	AHCLKX	Determines if abe_mcasp_ahclkx pin functions as an input or output. 0x0: Input 0x1: Output	RW	0
26	ACLKX	Determines if abe_mcasp_aclkx pin functions as an input or output. 0x0: Input 0x1: Output	RW	0
25	AMUTE	Determines if abe_mcasp_amute pin functions as an input or output. 0x0: Input 0x1: Output	RW	0
24:1	RESERVED	Reserved	RW	0x000
0	AXR0	Determines if abe_mcasp_axr pin functions as an input or output. 0x0: Input 0x1: Output	RW	0

Table 23-598. Register Call Summary for Register MCASP_PDIR

Multichannel Audio Serial Port

- DIT Transfer Mode: [0]
- McASP Global Initialization: [1] [2] [3] [4] [5]
- McASP Register Summary: [6]
- McASP Register Description: [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18]

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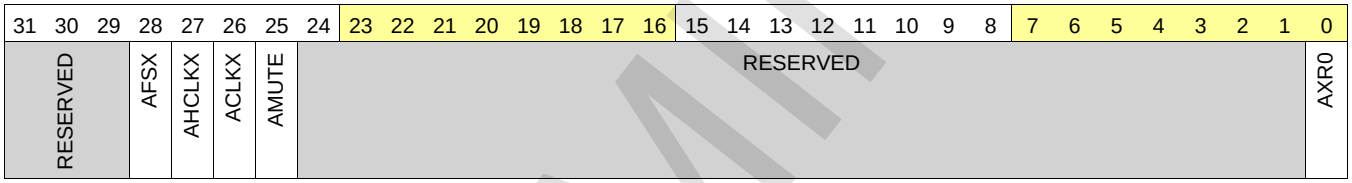
Table 23-599. MCASP_PDOUT

Address Offset	0x0000 0018
Physical Address	0x4902 8018 0x4012 8018 0x01D2 8018
Description	Pin data output register - holds a value for data out at all times, and may be read back at all times. The value held by MCASP_PDOUT is not affected by writing to MCASP_PDIR and MCASP_PFUNC. However, the data value in MCASP_PDOUT is driven out onto the McASP pin only if the corresponding bit in MCASP_PFUNC is set to 1 (GPIO function) and the corresponding bit in MCASP_PDIR is set to 1 (output). When reading data, it returns the corresponding bit value in MCASP_PDOUT[n]; it does not return the input from the I/O pin. When writing data, writes to the corresponding MCASP_PDOUT[n] bit. PDOUT has these aliases or alternate addresses: • MCASP_PDSET - when written to at this address, writing a 1 to a bit in MCASP_PDSET sets the corresponding bit in MCASP_PDOUT to 1; writing a 0 has no effect and keeps the bits in MCASP_PDOUT unchanged. • MCASP_PDCLR - when written to at this address, writing a 1 to a bit in MCASP_PDCLR clears the corresponding bit in MCASP_PDOUT to 0; writing a 0 has no effect and keeps the bits in MCASP_PDOUT unchanged There is only one set of data-out bits, MCASP_PDOUT[31:0]. The other registers, MCASP_PDSET and MCASP_PDCLR, are just different addresses for the same control bits, with different behaviors during writes.
Type	RW



Bits	Field Name	Description	Type	Reset
31:29	RESERVED	Reserved	RW	0
28	AFSX	Determines drive on AFSX output pin when the corresponding MCASP_PFUNC[28] and MCASP_PDIR[28] bits are set to 1. 0x0: The pin drives low. 0x1: The pin drives high.	RW	0
27	AHCLKX	Determines drive on AHCLKX output pin when the corresponding MCASP_PFUNC[27] and MCASP_PDIR[27] bits are set to 1. 0x0: The pin drives low. 0x1: The pin drives high.	RW	0
26	ACLKX	Determines drive on ACLKX output pin when the corresponding MCASP_PFUNC[26] and MCASP_PDIR[26] bits are set to 1 0x0: The pin drives low. 0x1: The pin drives high.	RW	0
25	AMUTE	Determines drive on AMUTE output pin when the corresponding MCASP_PFUNC[25] and MCASP_PDIR[25] bits are set to 1. 0x0: The pin drives low. 0x1: The pin drives high.	RW	0
24:1	RESERVED	Reserved	RW	0x000
0	AXR0	Determines drive on abe_mcasp_axr output pin when the corresponding MCASP_PFUNC[0] and MCASP_PDIR[0] bits are set to 1. 0x0: The pin drives low. 0x1: The pin drives high.	RW	0

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Table 23-600. Register Call Summary for Register MCASP_PDOUT

Multichannel Audio Serial Port

- McASP Register Summary: [0]
- McASP Register Description: [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23] [24] [25] [26] [27] [28] [29] [30] [31] [32] [33]

Table 23-601. MCASP_PDIN

Address Offset	0x0000 001C
Physical Address	0x4902 801C 0x4012 801C 0x01D2 801C
Description	Pin data input register - holds the state of all the McASP pins. MCASP_PDIN allows reading the actual value of the pin, regardless of the state of MCASP_PFUNC and MCASP_PDIR.
Type	R

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			AFSX	AHCLKX	ACLKX	AMUTE	RESERVED																								AXR0

Bits	Field Name	Description	Type	Reset
31:29	RESERVED	Reserved	R	0
28	AFSX	Logic level on abe_mcasp_afsx pin. 0x0: Pin is logic low. 0x1: Pin is logic high.	R	0
27	AHCLKX	Logic level on abe_mcasp_ahclkx pin. 0x0: Pin is logic low. 0x1: Pin is logic high.	R	0
26	ACLKX	Logic level on abe_mcasp_aclkx pin. 0x0: Pin is logic low. 0x1: Pin is logic high.	R	0
25	AMUTE	Logic level on abe_mcasp_amute pin. 0x0: Pin is logic low. 0x1: Pin is logic high.	R	0
24:1	RESERVED	Reserved	R	0x000
0	AXR0	Logic level on abe_mcasp_axr pin. 0x0: Pin is logic low. 0x1: Pin is logic high.	R	0

Table 23-602. Register Call Summary for Register MCASP_PDIN

Multichannel Audio Serial Port

- McASP Register Summary: [0]
- McASP Register Description: [1]

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Table 23-603. MCASP_PDSET

Address Offset	0x0000 001C
Physical Address	0x4902 801C 0x4012 801C 0x01D2 801C
Description	The pin data set register is an alias of the pin data output register (MCASP_PDOUT) for writes only. Writing a 1 to the MCASP_PDSET bit sets the corresponding bit in MCASP_PDOUT and, if MCASP_PFUNC = 1 (GPIO function) and MCASP_PDIR = 1 (output), drives a logic high on the pin.
Type	W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			AFSX	AHCLKX	ACLKX	AMUTE	RESERVED																								AXR0
W-0			W-0	W-0	W-0	W-0	R-0																								W-0

Bits	Field Name	Description	Type	Reset
31:29	RESERVED	Reserved	W	0
28	AFSX	Allows the corresponding AFSX bit in MCASP_PDOUT to be set to a logic high without affecting other I/O pins controlled by the same port. 0x0: No effect 0x1: MCASP_PDOUT[28] bit is set to 1.	W	0
27	AHCLKX	Allows the corresponding AHCLKX bit in MCASP_PDOUT to be set to a logic high without affecting other I/O pins controlled by the same port. 0x0: No effect 0x1: MCASP_PDOUT[27] bit is set to 1.	W	0
26	ACLKX	Allows the corresponding ACLKX bit in MCASP_PDOUT to be set to a logic high without affecting other I/O pins controlled by the same port. 0x0: No effect 0x1: MCASP_PDOUT[26] bit is set to 1.	W	0
25	AMUTE	Allows the corresponding AMUTE bit in MCASP_PDOUT to be set to a logic high without affecting other I/O pins controlled by the same port. 0x0: No effect 0x1: MCASP_PDOUT[25] bit is set to 1.	W	0
24:1	RESERVED	Reserved	W	0x000
0	AXR0	Allows the AXR0 bit in MCASP_PDOUT to be set to a logic high without affecting other I/O pins controlled by the same port. 0x0: No effect 0x1: MCASP_PDOUT[0] bit is set to 1.	W	0

Table 23-604. Register Call Summary for Register MCASP_PDSET

Multichannel Audio Serial Port

- McASP Register Summary: [0]
- McASP Register Description: [1] [2] [3] [4]

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Table 23-605. MCASP_PDCLR

Address Offset	0x0000 0020
Physical Address	0x4902 8020 0x4012 8020 0x01D2 8020
Description	The pin data clear register is an alias of the pin data output register (MCASP_PDOUT) for writes only. Writing a 1 to the MCASP_PDCLR bit clears the corresponding bit in MCASP_PDOUT and, if MCASP_PFUNC = 1 (GPIO function) and MCASP_PDIR = 1 (output), drives a logic low on the pin.
Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			AFSX	AHCLKX	ACLKX	AMUTE	RESERVED																								AXR0

Bits	Field Name	Description	Type	Reset
31:29	RESERVED	Reserved	RW	0
28	AFSX	Allows the corresponding AFSX bit in MCASP_PDOUT to be cleared to a logic low without affecting other I/O pins controlled by the same port. 0x0: No effect 0x1: MCASP_PDOUT[28] bit is cleared to 0.	RW	0
27	AHCLKX	Allows the corresponding AHCLKX bit in MCASP_PDOUT to be cleared to a logic low without affecting other I/O pins controlled by the same port. 0x0: No effect 0x1: MCASP_PDOUT[27] bit is cleared to 0.	RW	0
26	ACLKX	Allows the corresponding ACLKX bit in MCASP_PDOUT to be cleared to a logic low without affecting other I/O pins controlled by the same port. 0x0: No effect 0x1: MCASP_PDOUT[26] bit is cleared to 0.	RW	0
25	AMUTE	Allows the corresponding AMUTE bit in MCASP_PDOUT to be cleared to a logic low without affecting other I/O pins controlled by the same port. 0x0: No effect 0x1: MCASP_PDOUT[25] bit is cleared to 0.	RW	0
24:1	RESERVED	Reserved	RW	0x000
0	AXR0	Allows the AXR0 bit in MCASP_PDOUT to be cleared to a logic low without affecting other I/O pins controlled by the same port. 0x0: No effect 0x1: MCASP_PDOUT[0] bit is cleared to 0.	RW	0

Table 23-606. Register Call Summary for Register MCASP_PDCLR

Multichannel Audio Serial Port

- McASP Register Summary: [0]
- McASP Register Description: [1] [2] [3] [4]

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Table 23-607. MCASP_GBLCTL

Address Offset	0x0000 0044		
Physical Address	0x4902 8044 0x4012 8044 0x01D2 8044	**Instance**	MCASP_L3 MCASP_CORTEX-A9 MCASP_DSP
Description	Global transmit control register - provides initialization of the transmit section. The bit fields in MCASP_GBLCTL are synchronized and latched by the abe_mcasp_aclkx clock. Before programming MCASP_GBLCTL, ensure that the serial clocks are running. If the corresponding external serial clock, abe_mcasp_clkx, is not yet running, select the internal serial clock source in AHCLKXCTL and ACLKXCTL before programming MCASP_GBLCTL. Also, after programming any bits in MCASP_GBLCTL, do not proceed until reading back from MCASP_GBLCTL and verifying that the bits in MCASP_GBLCTL are latched.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																			XFRST	XSMRST	XSRCLR	XHCLKRST	XCLKRST	RESERVED							

Bits	Field Name	Description	Type	Reset
31:13	RESERVED	Reserved	RW	0x00000
12	XFRST	Transmit frame-sync generator reset enable bit 0x0: The transmit frame-sync generator is reset. 0x1: The transmit frame-sync generator is active. When released from reset, the transmit frame-sync generator begins counting serial clocks and generating frame sync as programmed.	RW	0
11	XSMRST	Transmit state-machine reset enable bit 0x0: The transmit state-machine is held in reset. abe_mcasp_axr pin state: If MCASP_PFUNC[0] = 0 and MCASP_PDIR[0] = 1, the serializer drives the abe_mcasp_axr pin to the state specified for inactive time slot 0x1: The transmit state-machine is released from reset. When released from reset, the transmit state-machine immediately transfers data from XBUF[n] to XRSR[n]. The transmit state-machine sets the underrun flag (XUNDRN) in MCASP_XSTAT, if XBUF[n] have not been preloaded with data before reset is released. The transmit state-machine also immediately begins detecting frame sync and is ready to transmit. Transmission of TDM time slot begins at slot 0 after reset is released.	RW	0
10	XSRCLR	Transmit serializer clear enable bit. By clearing and then setting this bit, the transmit buffer is flushed to an empty state (XDATA = 1). If XSMRST = 1, XSRCLR = 1, XDATA = 1, and XBUF is not loaded with new data before the start of the next active time slot, an underrun occurs. 0x0: The transmit serializer is cleared. 0x1: The transmit serializer is active. When the transmit serializer is first taken out of reset (XSRCLR changes from 0 to 1), the transmit data ready bit (XDATA) in MCASP_XSTAT is set to indicate XBUF is ready to be written.	RW	0
9	XHCLKRST	Transmit high-frequency clock divider reset enable bit 0x0: The transmitter high-frequency clock divider is held in reset. 0x1: The transmitter high-frequency clock divider is running.	RW	0
8	XCLKRST	Transmit clock divider reset enable bit 0x0: The transmit clock divider is held in reset. When the clock divider is in reset, it passes through a divide-by-1 of its input. 0x1: The transmit clock divider is running.	RW	0
7:0	RESERVED	Reserved	RW	0x0

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Table 23-608. Register Call Summary for Register MCASP_GBLCTL

Multichannel Audio Serial Port

- McASP Software Reset: [0] [1]
- DIT Transfer Mode: [2]
- McASP Global Initialization: [3] [4] [5] [6] [7] [8]
- McASP DIT Transmission Mode: [9] [10] [11]
- McASP Register Summary: [12]
- McASP Register Description: [13] [14] [15] [16] [17] [18]

Table 23-609. MCASP_AMUTE

Address Offset	0x0000 0048		
Physical Address	0x4902 8048 0x4012 8048 0x01D2 8048	**Instance**	MCASP_L3 MCASP_CORTEX-A9 MCASP_DSP
Description	Mute control register - Controls the McASP mute output pin (abe_mcasp_amute)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																			XDMAERR	RESERVED	XCKFAIL	RESERVED	XSYNCERR	RESERVED	XUNDRN	RESERVED	INSTAT	INEN	INPOL	MUTEN

Bits	Field Name	Description	Type	Reset
31:13	RESERVED	Reserved	RW	0x00000
12	XDMAERR	Drives AMUTE active enable bit on transmit DMA error (XDMAERR). 0x0: Drive is disabled. Detection of transmit DMA error is ignored by abe_mcasp_amute. 0x1: Drive is enabled (active). Upon detection of transmit DMA error, abe_mcasp_amute is active and is driven according to MUTEN bits.	RW	0
11	RESERVED	Reserved	RW	0
10	XCKFAIL	XMT bad clock. Drives AMUTE active enable bit on transmit clock failure (XCKFAIL). 0x0: Drive is disabled. Detection of transmit clock failure is ignored by abe_mcasp_amute. 0x1: Drive is enabled (active). Upon detection of transmit clock failure, abe_mcasp_amute is active and is driven according to MUTEN bits.	RW	0
9	RESERVED	Reserved	RW	0
8	XSYNCERR	XMT unexpected FS. Drives AMUTE active enable bit on unexpected transmit frame-sync error (XSYNCERR). 0x0: Drive is disabled. Detection of unexpected transmit frame-sync error is ignored by abe_mcasp_amute. 0x1: Drive is enabled (active). Upon detection of unexpected transmit frame-sync error, abe_mcasp_amute is active and is driven according to MUTEN bit.	RW	0
7	RESERVED	Reserved	RW	0
6	XUNDRN	XMT underrun occurs. Drives AMUTE active enable bit on ransmit underrun error (XUNDRN). 0x0: Drive is disabled. Detection of transmit underrun error is ignored by abe_mcasp_amute. 0x1: Drive is enabled (active). Upon detection of transmit underrun error, abe_mcasp_amute is active and is driven according to MUTEN bit.	RW	0
5	RESERVED	Reserved	RW	0

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Bits	Field Name	Description	Type	Reset
4	INSTAT	Status of mute in pin, determines drive on abe_mcasp_axr pin when the MCASP_PFUNC[0] and MCASP_PDIR[0] bits are set to 1. Read 0x0: Inactive Read 0x1: Active. Audio mute in error is detected.	R	0
3	INEN	Drive abe_mcasp_amute active when abe_mcasp_amutein error is active. 0x0: Drive is disabled. abe_mcasp_amutein is ignored by abe_mcasp_amute. 0x1: Drive is enabled (active). INSTAT = 1 drives abe_mcasp_amute active.	RW	0
2	INPOL	Audio mute in (abe_mcasp_amutein) polarity select bit 0x0: Polarity is active high. A high on abe_mcasp_amutein sets INSTAT to 1. 0x1: Polarity is active low. A low on abe_mcasp_amutein sets INSTAT to 1.	RW	0
1:0	MUTEN	abe_mcasp_amute pin enable bit field (unless overridden by GPIO registers) 0x0: Disabled, pin goes to 3-state condition. 0x1: Pin is driven high if error is detected. 0x2: Pin is driven low if error is detected.	RW	0x0

Table 23-610. Register Call Summary for Register MCASP_AMUTE

Multichannel Audio Serial Port

- DIT Transfer Mode: [0]
- Audio Mute (AMUTE) Function: [1] [2] [3] [4]
- Clock Failure Detection: [5]
- McASP Global Initialization: [6] [7] [8] [9] [10] [11] [12]
- McASP Register Summary: [13]

Table 23-611. MCASP_TXDITCTL

Address Offset	0x0000 0050		
Physical Address	0x4902 8050 0x4012 8050 0x01D2 8050	**Instance**	MCASP_L3 MCASP_CORTEX-A9 MCASP_DSP
Description	Transmit DIT mode control register, controls DIT operations of the McASP		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												VB	VA	RESERVED	DITEN

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved	RW	0x0000000
3	VB	Valid bit for odd time slots (DIT right subframe). 0x0: V bit is 0 during odd DIT subframes. 0x1: V bit is 1 during odd DIT subframes.	RW	0
2	VA	Valid bit for even time slots (DIT left subframe). 0x0: V bit is 0 during even DIT subframes. 0x1: V bit is 1 during even DIT subframes.	RW	0
1	RESERVED	Reserved	RW	0

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Bits	Field Name	Description	Type	Reset
0	DITEN	DIT mode enable bit 0x0: DIT mode is disabled. 0x1: DIT mode is enabled. Transmitter operates in DIT encoded mode.	RW	0

Table 23-612. Register Call Summary for Register MCASP_TXDITCTL

Multichannel Audio Serial Port
- DIT Transfer Mode: [0]
- McASP Global Initialization: [1] [2] [3]
- McASP Register Summary: [4]

Table 23-613. MCASP_TXMASK

Address Offset	0x0000 00A4		
Physical Address	0x4902 80A4 0x4012 80A4 0x01D2 80A4	**Instance**	MCASP_L3 MCASP_CORTEX-A9 MCASP_DSP
Description	Transmit format unit bit mask register - Determines which bits of the transmitted data are masked off before being shifted out the McASP		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
XMASK31	XMASK30	XMASK29	XMASK28	XMASK27	XMASK26	XMASK25	XMASK24	XMASK23	XMASK22	XMASK21	XMASK20	XMASK19	XMASK18	XMASK17	XMASK16	XMASK15	XMASK14	XMASK13	XMASK12	XMASK11	XMASK10	XMASK9	XMASK8	XMASK7	XMASK6	XMASK5	XMASK4	XMASK3	XMASK2	XMASK1	XMASK0

Bits	Field Name	Description	Type	Reset
31:0	XMASK[31:0]	Transmit data mask enable bit 0x0: The corresponding bit of transmit data is masked out and then transmitted out the McASP in place of the original bit. 0x1: The corresponding bit of transmit data is transmitted out the McASP.	RW	0

Table 23-614. Register Call Summary for Register MCASP_TXMASK

Multichannel Audio Serial Port
- Format Unit: [0] [1]
- DIT Transfer Mode: [2]
- McASP Global Initialization: [3] [4]
- McASP Register Summary: [5]

Table 23-615. MCASP_TXFMT

Address Offset	0x0000 00A8		
Physical Address	0x4902 80A8 0x4012 80A8 0x01D2 80A8	**Instance**	MCASP_L3 MCASP_CORTEX-A9 MCASP_DSP
Description	Transmit bitstream format register - configures the transmit data format		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														XDATDLY		XRVRS	XPAD		RESERVED					XSSZ				XBUSEL	XROT		

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Bits	Field Name	Description	Type	Reset
31:18	RESERVED	Reserved	RW	0x0000
17:16	XDATDLY	Transmit sync bit delay 0x0: 0 bit delay - The first transmit data bit, abe_mcasp_axr, occurs in the same abe_mcasp_aclkx cycle as the transmit frame sync (abe_mcasp_afsx). 0x1: Reserved 0x2: Reserved	RW	0x0
15	XRVRS	Transmit serial bitstream order 0x0: Bitstream is LSB first. No bit reversal is performed in transmit format unit. 0x1: Reserved	RW	0x0
14:13	XPAD	Pad value for extra bits in slot not belonging to word defined by XMASK. This field only applies to bits when XMASK[n] = 0. 0x0: Pad extra bits with 0. 0x1 to 0x3: Reserved	RW	0x00
12:8	RESERVED	Reserved	RW	0x0
7:4	XSSZ	Transmit slot size 0x0 to 0xE: Reserved 0xF: Slot size is 32 bits.	RW	0x0
3	XBUSEL	Selects whether writes to the serializer buffer XBUF originate from the peripheral configuration port or the DMA port. 0x0: Writes to XBUF originate from the data port. Writes to XBUF from the peripheral configuration port are ignored with no effect on the McASP. 0x1: Writes to XBUF originate from the peripheral configuration port. Writes to XBUF from the data port are ignored with no effect on the McASP.	RW	0
2:0	XROT	Right-rotation value for transmit rotate right format unit 0x0: Rotate right by 0 (no rotation). 0x1: Rotate right by 4 bit positions. 0x2: Rotate right by 8 bit positions. 0x3: Rotate right by 12 bit positions. 0x4: Rotate right by 16 bit positions. 0x5: Rotate right by 20 bit positions. 0x6: Rotate right by 24 bit positions. 0x7: Rotate right by 28 bit positions.	RW	0x0

Table 23-616. Register Call Summary for Register MCASP_TXFMT

Multichannel Audio Serial Port

- Format Unit: [0] [1] [2] [3] [4] [5] [6] [7] [8]
- Transmit State-Machine: [9]
- DIT Transfer Mode: [10] [11]
- Data Ready Status and Event/Interrupt Generation: [12] [13]
- McASP Global Initialization: [14] [15] [16]
- McASP DIT Transmission Mode: [17] [18] [19]
- McASP Register Summary: [20]

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Table 23-617. MCASP_TXFMCTL

Address Offset	0x0000 00AC		
Physical Address	0x4902 80AC 0x4012 80AC 0x01D2 80AC	**Instance**	MCASP_L3 MCASP_CORTEX-A9 MCASP_DSP
Description	Transmit frame-sync control register - configures the transmit frame sync (abe_mcasp_afsx).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																XMOD								RESERVED			FXWID	RESERVED		FSXM	FSXP

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	RW	0x0000
15:7	XMOD	Transmit frame-sync mode select bits 0x180: 384-slot DIT mode All other: Reserved	RW	0x000
6:5	RESERVED	Reserved	RW	0x0
4	FXWID	The transmit frame-sync width select bit indicates the width of the transmit frame sync (abe_mcasp_afsx) during its active period. 0x0: Single bit 0x1: Reserved	RW	0
3:2	RESERVED	Reserved	RW	0x0
1	FSXM	Transmit frame-sync generation select bit 0x0: Reserved 0x1: Internally-generated transmit frame sync	RW	0
0	FSXP	Transmit frame-sync polarity select bit 0x0: Rising Edge - A rising edge on transmit frame sync (abe_mcasp_afsx) indicates the beginning of a frame. 0x1: Reserved	RW	0

Table 23-618. Register Call Summary for Register MCASP_TXFMCTL

Multichannel Audio Serial Port

- Frame-Sync Generator: [0] [1] [2] [3] [4]
- DIT Transfer Mode: [5] [6]
- McASP Global Initialization: [7] [8]
- McASP Register Summary: [9]

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Table 23-619. MCASP_ACLKXCTL

Address Offset	0x0000 00B0		
Physical Address	0x4902 80B0 0x4012 80B0 0x01D2 80B0	**Instance**	MCASP_L3 MCASP_CORTEX-A9 MCASP_DSP
Description	Transmit clock control register - Configures the transmit bit clock (abe_mcasp_aclkx) and the transmit clock generator.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								ASYNC	CLKXM	CLKXDIV					

Bits	Field Name	Description	Type	Reset
31:7	RESERVED	Reserved	RW	0x00
6	ASYNC	Transmit operation asynchronous enable bit 0x0: Reserved 0x1: Asynchronous	RW	1
5	CLKXM	Transmit bit clock source bit 0x0: Reserved 0x1: Internal (output of divider)	RW	1
4:0	CLKXDIV	Transmit bit clock divide ratio bits, determine the divide-down ratio from AHCLKX to ACLKX. 0x0: Divide-by-1 0x1: Divide-by-2 0x2 to 0x1F: Divide-by-3 to divide-by-32	RW	0x00

Table 23-620. Register Call Summary for Register MCASP_ACLKXCTL

Multichannel Audio Serial Port

- Transmit Clock: [0] [1] [2]
- DIT Transfer Mode: [3] [4]
- McASP Global Initialization: [5]
- McASP Register Summary: [6]

Table 23-621. MCASP_AHCLKXCTL

Address Offset	0x0000 00B4		
Physical Address	0x4902 80B4 0x4012 80B4 0x01D2 80B4	**Instance**	MCASP_L3 MCASP_CORTEX-A9 MCASP_DSP
Description	High-frequency transmit clock control register - Configures the transmit high-frequency master clock (abe_mcasp_ahclkx) and the transmit clock generator.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																HCLKXM	RESERVED			HCLKXDIV											

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Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	RW	0x000
15	HCLKXM	Transmit high-frequency clock source bit 0x0: Reserved 0x1: Internal transmit high-frequency clock source from output of programmable high clock divider	RW	1
14:12	RESERVED	Reserved	RW	0x0
11:0	HCLKXDIV	Transmit high-frequency clock divide ratio bits determine the divide-down ratio from AUXCLK to abe_mcasp_ahclkx.(1) 0x0: Divide-by-1 0x1: Divide-by-2 0x2 to 0xFFF: Divide-by-3 to divide-by-4096	RW	0x000

(1) The AUXCLK clock is sourced directly from MCASP_FCLK.

Table 23-622. Register Call Summary for Register MCASP_AHCLKXCTL

Multichannel Audio Serial Port
- Transmit Clock: [0] [1] [2]
- DIT Transfer Mode: [3]
- McASP Global Initialization: [4]
- McASP Register Summary: [5]

Table 23-623. MCASP_TXTDM

Address Offset	0x0000 00B8		
Physical Address	0x4902 80B8 0x4012 80B8 0x01D2 80B8	**Instance**	MCASP_L3 MCASP_CORTEX-A9 MCASP_DSP
Description	Transmit TDM slot 0-31 register - TDM time slot counter range is to 384 slots (to support SPDIF blocks of 384 subframes).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
XTDMS31	XTDMS30	XTDMS29	XTDMS28	XTDMS27	XTDMS26	XTDMS25	XTDMS24	XTDMS23	XTDMS22	XTDMS21	XTDMS20	XTDMS19	XTDMS18	XTDMS17	XTDMS16	XTDMS15	XTDMS14	XTDMS13	XTDMS12	XTDMS11	XTDMS10	XTDMS9	XTDMS8	XTDMS7	XTDMS6	XTDMS5	XTDMS4	XTDMS3	XTDMS2	XTDMS1	XTDMS0

Bits	Field Name	Description	Type	Reset
31:0	XTDMS[31:0]	Transmitter mode during TDM time slot n 0x0: Reserved 0x1: The transmit TDM time slot n is active. The transmit serializer shifts out data during this slot according to the serializer control register (MCASP_SRCTL).	RW	0

Table 23-624. Register Call Summary for Register MCASP_TXTDM

Multichannel Audio Serial Port
- Transmit TDM Sequencer: [0]
- DIT Transfer Mode: [1] [2]
- McASP Global Initialization: [3]
- McASP Register Summary: [4]

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Table 23-625. MCASP_EVTCTLX

Address Offset	0x0000 00BC		
Physical Address	0x4902 80BC 0x4012 80BC 0x01D2 80BC	**Instance**	MCASP_L3 MCASP_CORTEX-A9 MCASP_DSP
Description	Transmitter Interrupt control register - controls generation of the McASP transmit interrupt (XINT). When the register bit(s) is set to 1, the occurrence of the enabled McASP condition(s) generates XINT.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								XSTAFRM	RESERVED	XDATA	XLAST	XDMAERR	XCKFAIL	XSYNCERR	XUNDRN

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Reserved	RW	0x000000
7	XSTAFRM	Transmit start of frame interrupt enable bit 0x0: Interrupt is disabled. A transmit-start-of-frame interrupt does not generate a McASP transmit interrupt (XINT). 0x1: Interrupt is enabled. A transmit-start-of-frame interrupt generates a McASP transmit interrupt (XINT).	RW	0
6	RESERVED	Reserved	RW	0
5	XDATA	Transmit data-ready interrupt enable bit 0x0: Interrupt is disabled. A transmit data-ready interrupt does not generate a McASP transmit interrupt (XINT). 0x1: Interrupt is enabled. A transmit data-ready interrupt generates a McASP transmit interrupt (XINT).	RW	0
4	XLAST	Transmit last slot interrupt enable bit 0x0: Interrupt is disabled. A transmit-last-slot interrupt does not generate a McASP transmit interrupt (XINT). 0x1: Interrupt is enabled. A transmit-last-slot interrupt generates a McASP transmit interrupt (XINT).	RW	0
3	XDMAERR	Transmit DMA error interrupt enable bit 0x0: Interrupt is disabled. A transmit DMA error interrupt does not generate a McASP transmit interrupt (XINT). 0x1: Interrupt is enabled. A transmit DMA error interrupt generates a McASP transmit interrupt (XINT).	RW	0
2	XCKFAIL	Transmit clock failure interrupt enable bit 0x0: Interrupt is disabled. A transmit clock failure interrupt does not generate a McASP transmit interrupt (XINT). 0x1: Interrupt is enabled. A transmit clock failure interrupt generates a McASP transmit interrupt (XINT).	RW	0
1	XSYNCERR	Unexpected transmit frame-sync interrupt enable bit 0x0: Interrupt is disabled. An unexpected transmit frame-sync interrupt does not generate a McASP transmit interrupt (XINT). 0x1: Interrupt is enabled. An unexpected transmit frame-sync interrupt generates a McASP transmit interrupt (XINT).	RW	0
0	XUNDRN	Transmitter underrun interrupt enable bit 0x0: Interrupt is disabled. A transmitter underrun interrupt does not generate a McASP transmit interrupt (XINT). 0x1: Interrupt is enabled. A transmitter underrun interrupt generates a McASP transmit interrupt (XINT).	RW	0

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Table 23-626. Register Call Summary for Register MCASP_EVTCTLX

Multichannel Audio Serial Port

- Data Ready Status and Event/Interrupt Generation: [0] [1]
- Interrupt Requests: [2] [3] [4] [5] [6] [7]
- Transmit Data Ready Interrupt: [8]
- Error Interrupt: [9]
- Clock Failure Detection: [10] [11]
- McASP DIT Transmission Mode: [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23] [24] [25]
- McASP Register Summary: [26]
- McASP Register Description: [27] [28] [29] [30] [31] [32] [33]

Table 23-627. MCASP_TXSTAT

Address Offset	0x0000 00C0		
Physical Address	0x4902 80C0 0x4012 80C0 0x01D2 80C0	**Instance**	MCASP_L3 MCASP_CORTEX-A9 MCASP_DSP
Description	Transmitter status register - If the McASP logic attempts to set an interrupt flag in the same cycle that the CPU writes to the flag to clear it, the McASP logic has priority and the flag remains set. This also causes the generation of a new interrupt request.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							XERR	XDMAERR	XSTAFRM	XDATA	XLAST	XTDMSLOT	XCKFAIL	XSYNCERR	XUNDRN

Bits	Field Name	Description	Type	Reset
31:9	RESERVED	Reserved	RW	0x000000
8	XERR	XERR bit always returns a logic-OR of: XUNDRN | XSYNCERR | XCKFAIL | XDMAERR. Allows a single bit to be checked to determine if a transmitter error interrupt has occurred. 0x0: No errors have occurred. 0x1: An error has occurred.	RW	0
7	XDMAERR	Transmit DMA error flag. XDMAERR is set when the CPU or DMA writes more words to the data port of the McASPin a given time slot than it should. Causes a transmit interrupt (XINT) if this bit and XDMAERR in MCASP_EVTCTLX are set. This bit is cleared by writing a 1 to it. Writing a 0 has no effect. 0x0: Transmit DMA error did not occur. 0x1: Transmit DMA error occurred.	RW	0
6	XSTAFRM	Transmit start of frame flag. Causes a transmit interrupt (XINT) if this bit and XSTAFRM in MCASP_EVTCTLX are set. This bit is cleared by writing a 1 to it. Writing a 0 has no effect. 0x0: No new transmit frame sync (AFSX) is detected. 0x1: A new transmit frame sync (AFSX) is detected.	RW	0
5	XDATA	Transmit data ready flag. Causes a transmit interrupt (XINT) if this bit and XDATA in MCASP_EVTCTLX are set. This bit is cleared by writing a 1 to iit. Writing a 0 has no effect 0x0: XBUF is written and is full 0x1: Data is copied from XBUF to XRSR. XBUF is empty and ready to be written. XDATA is also set when the transmit serializers are taken out of reset. When XDATA is set, it always causes a DMA event (AXEVT).	RW	0

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Bits	Field Name	Description	Type	Reset
4	XLAST	Transmit last slot flag. XLAST, along with XDATA, are set if the current slot is the last slot in a frame. Causes a transmit interrupt (XINT) if this bit and XLAST in MCASP_EVTCTLX are set. This bit is cleared by writing a 1 to iit. Writing a 0 has no effect. 0x0: Current slot is not the last slot in a frame. 0x1: Current slot is the last slot in a frame. XDATA is also set.	RW	0
3	XTDMSLOT	Returns the LSB of XSLOT. Allows a single read of XSTAT to determine whether the current TDM time slot is even or odd. read 0x0: Current TDM time slot is odd. read 0x1: Current TDM time slot is even.	R	0
2	XCKFAIL	Transmit clock failure flag. XCKFAIL is set when the transmit clock failure detection circuit reports an error. Causes a transmit interrupt (XINT) if this bit and XCKFAIL in MCASP_EVTCTLX are set. This bit is cleared by writing a 1 to iit. Writing a 0 has no effect. 0x0: Transmit clock failure did not occur. 0x1: Transmit clock failure occurred	RW	0
1	XSYNCERR	Unexpected transmit frame-sync flag. XSYNCERR is set when a new transmit frame sync (AFSX) occurs before it is expected. Causes a transmit interrupt (XINT) if this bit and XSYNCERR in MCASP_EVTCTLX are set. This bit is cleared by writing a 1 to iit. Writing a 0 has no effect. 0x0: Unexpected transmit frame sync did not occur 0x1: Unexpected transmit frame sync occurred.	RW	0
0	XUNDRN	Transmitter underrun flag. XUNDRN is set when the transmit serializer is instructed to transfer data from XBUF to XRSR, but XBUF has not yet been serviced with new data since the last transfer. Causes a transmit interrupt (XINT) if this bit and XUNDRN in MCASP_EVTCTLX are set. This bit is cleared by writing a 1 to iit. Writing a 0 has no effect. 0x0: Transmitter underrun did not occur 0x1: Transmitter underrun occurred.	RW	0

Table 23-628. Register Call Summary for Register MCASP_TXSTAT

Multichannel Audio Serial Port

- Transmit State-Machine: [0]
- Data Ready Status and Event/Interrupt Generation: [1] [2] [3] [4]
- Interrupt Requests: [5] [6] [7] [8] [9] [10] [11]
- Transmit Data Ready Interrupt: [12] [13]
- Error Interrupt: [14] [15]
- Buffer Underrun Error –Transmitter: [16]
- DMA Error –Transmitter: [17] [18]
- Clock Failure Detection: [19] [20] [21]
- McASP DIT Transmission Mode: [22] [23] [24] [25]
- McASP Event Servicing: [26] [27]
- McASP Register Summary: [28]

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Table 23-629. MCASP_TXTDMSLOT

Address Offset	0x0000 00C4		
Physical Address	0x4902 80C4 0x4012 80C4 0x01D2 80C4	**Instance**	MCASP_L3 MCASP_CORTEX-A9 MCASP_DSP
Description	Current transmit TDM time slot register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								XSLOTCNT							

Bits	Field Name	Description	Type	Reset
31:10	RESERVED	Reserved	R	0x000000
9:0	XSLOTCNT	Current transmit time slot count. the value of this register is 0b0101111111 (0x17f) during reset and 0 after reset.	R	0x000

Table 23-630. Register Call Summary for Register MCASP_TXTDMSLOT

Multichannel Audio Serial Port

- Transmit TDM Sequencer: [0]
- McASP Register Summary: [1]

Table 23-631. MCASP_TXCLKCHK

Address Offset	0x0000 00C8		
Physical Address	0x4902 80C8 0x4012 80C8 0x01D2 80C8	**Instance**	MCASP_L3 MCASP_CORTEX-A9 MCASP_DSP
Description	Transmit clock check control register - configures the transmit clock failure detection circuit.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
XCNT								XMAX								XMIN								RESERVED				XPS			

Bits	Field Name	Description	Type	Reset
31:24	XCNT	Transmit clock count value (from previous measurement). The clock circuit continually counts the number of system clocks for every 32 transmit high-frequency master clock (abe_mcasp_ahclkx) signals, and stores the count in XCNT until the next measurement is taken	R	0x00
23:16	XMAX	0x0 to 0xFF: Transmit clock maximum boundary. This 8-bit unsigned value sets the maximum allowed boundary for the clock check counter after 32 transmit high-frequency master clock (abe_mcasp_ahclkx) signals have been received. If the current counter value is greater than XMAX after counting 32 AHCLKX signals, XCKFAIL in XSTAT is set. The comparison is performed using unsigned arithmetic.	RW	0x00
15:8	XMIN	0x0 to 0xFF: Transmit clock minimum boundary. This 8-bit unsigned value sets the minimum allowed boundary for the clock check counter after 32 transmit high-frequency master clock (abe_mcasp_ahclkx) signals have been received. If XCNT is less than XMIN after counting 32 AHCLKX signals, XCKFAIL in XSTAT is set. The comparison is performed using unsigned arithmetic.	RW	0x00
7:4	RESERVED	Reserved	RW	0x0

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Bits	Field Name	Description	Type	Reset
3:0	XPS	Transmit clock check prescaler value 0x0: McASP system clock divided by 1 0x1: McASP system clock divided by 2 0x2: McASP system clock divided by 4 0x3: McASP system clock divided by 8 0x4: McASP system clock divided by 16 0x5: McASP system clock divided by 32 0x6: McASP system clock divided by 64 0x7: McASP system clock divided by 128 0x8: McASP system clock divided by 256 0x9 to 0xF: Reserved	RW	0x0

Table 23-632. Register Call Summary for Register MCASP_TXCLKCHK

Multichannel Audio Serial Port

- DIT Transfer Mode: [0]
- Clock Failure Detection: [1] [2]
- McASP Register Summary: [3]

Table 23-633. MCASP_TXEVTCTL

Address Offset	0x0000 00CC		
Physical Address	0x4902 80CC 0x4012 80CC 0x01D2 80CC	**Instance**	MCASP_L3 MCASP_CORTEX-A9 MCASP_DSP
Description	Transmitter DMA event control register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															XDATDMA

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	RW	0x0000 0000
0	XDATDMA	Transmit data DMA request enable bit. When writing to this field, always write the default value of 0. 0x0: The transmit data DMA request is enabled. 0x1: The transmit data DMA request is disabled.	RW	0

Table 23-634. Register Call Summary for Register MCASP_TXEVTCTL

Multichannel Audio Serial Port

- DIT Transfer Mode: [0]
- Data Ready Status and Event/Interrupt Generation: [1]
- DMA Requests: [2]
- McASP DIT Transmission Mode: [3] [4] [5]
- McASP Register Summary: [6]

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Table 23-635. MCASP_DITCSRAi

Address Offset	0x0000 0100 + (0x04*i)		
Physical Address	0x4902 8100 + (0x04*i) 0x4012 8100 + (0x04*i) 0x01D2 8100 + (0x04*i)	**Instance**	MCASP_L3 MCASP_CORTEX-A9 MCASP_DSP
Description	DIT left channel status register - All six 32-bit registers (I = 0 to 5) can store 192 bits of channel status data for a complete block of transmission. The DIT reuses the same data for the next block. Make sure to update the register file before a different set of data needs to be sent.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DITCSRAi																															

Bits	Field Name	Description	Type	Reset
31:0	DITCSRAi	Left (even TDM slot) channel status	RW	0x0000 0000

Table 23-636. Register Call Summary for Register MCASP_DITCSRAi

Multichannel Audio Serial Port

- DIT Transfer Mode: [0] [1]
- McASP Global Initialization: [2]
- McASP Register Summary: [3]

Table 23-637. MCASP_DITCSRBi

Address Offset	0x0000 0118+ (0x04*i)		
Physical Address	0x4902 8118 + (0x04*i) 0x4012 8118 + (0x04*i) 0x01D2 8118 + (0x04*i)	**Instance**	MCASP_L3 MCASP_CORTEX-A9 MCASP_DSP
Description	DIT right channel status register - All six 32-bit registers (I = 0 to 5) can store 192 bits of channel status data for a complete block of transmission. The DIT reuses the same data for the next block. Make sure to update the register file before a different set of data needs to be sent.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DITCSRBi																															

Bits	Field Name	Description	Type	Reset
31:0	DITCSRBi	Right (odd TDM slot) channel status	RW	0x0000 0000

Table 23-638. Register Call Summary for Register MCASP_DITCSRBi

Multichannel Audio Serial Port

- DIT Transfer Mode: [0] [1]
- McASP Global Initialization: [2]
- McASP Register Summary: [3]

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Table 23-639. MCASP_DITUDRAi

Address Offset	0x0000 0130 + (0x04*i)		
Physical Address	0x4902 8130 + (0x04*i) 0x4012 8130 + (0x04*i) 0x01D2 8130 + (0x04*i)	**Instance**	MCASP_L3 MCASP_CORTEX-A9 MCASP_DSP
Description	DIT left channel user data register - provides the user data of each left channel (even TDM time slot). All six 32-bit registers (I = 0 to 5) can store 192 bits of user data for a complete block of transmission. The DIT reuses the same data for the next block. Make sure to update the register before a different set of data needs to be sent.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DITUDRAi																															

Bits	Field Name	Description	Type	Reset
31:0	DITUDRAi	Left (even TDM slot) user data	RW	0x0000 0000

Table 23-640. Register Call Summary for Register MCASP_DITUDRAi

Multichannel Audio Serial Port

- DIT Transfer Mode: [0] [1]
- McASP Global Initialization: [2]
- McASP Register Summary: [3]

Table 23-641. MCASP_DITUDRBi

Address Offset	0x0000 0148+ (0x04*i)		
Physical Address	0x4902 8148 + (0x04*i) 0x4012 8148 + (0x04*i) 0x01D2 8148 + (0x04*i)	**Instance**	MCASP_L3 MCASP_CORTEX-A9 MCASP_DSP
Description	DIT right user data register - provides the user data of each right channel (odd TDM time slot). All six 32-bit registers (I = 0 to 5) can store 192 bits of user data for a complete block of transmission. The DIT reuses the same data for the next block. Make sure to update the register before a different set of data needs to be sent.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DITUDRBi																															

Bits	Field Name	Description	Type	Reset
31:0	DITUDRBi	Right (odd TDM slot) user data	RW	0x0000 0000

Table 23-642. Register Call Summary for Register MCASP_DITUDRBi

Multichannel Audio Serial Port

- DIT Transfer Mode: [0] [1]
- McASP Global Initialization: [2]
- McASP Register Summary: [3]

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Table 23-643. MCASP_XRSRCTL0

Address Offset	0x0000 0180		
Physical Address	0x4902 8180 0x4012 8180 0x01D2 8180	**Instance**	MCASP_L3 MCASP_CORTEX-A9 MCASP_DSP
Description	Serializer control register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																											XRDY	RESERVED			SRMOD	

Bits	Field Name	Description	Type	Reset
31:5	RESERVED	Reserved	RW	0x0000000
4	XRDY	Transmit buffer ready bit Read 0x0: The transmit buffer (MCASP_TXBUF0) contains data. Read 0x1: The transmit buffer (MCASP_TXBUF0) is empty and needs to be written before the start of the next time slot or a transmit underrun occurs.	R	0
3:2	RESERVED	Reserved	RW	0x0
1:0	SRMOD	Serializer mode bit 0x0:The serializer is inactive 0x1:The serializer is operating in transmit mode. 0x2: Reserved 0x3: Reserved	RW	0x0

Table 23-644. Register Call Summary for Register MCASP_XRSRCTL0

Multichannel Audio Serial Port

- Serializers: [0] [1]
- DIT Transfer Mode: [2]
- McASP Global Initialization: [3]
- McASP Register Summary: [4]

Table 23-645. MCASP_TXBUF0

Address Offset	0x0000 0200		
Physical Address	0x4902 8200 0x4012 8200 0x01D2 8200	**Instance**	MCASP_L3 MCASP_CORTEX-A9 MCASP_DSP
Description	Transmit buffer - The transmit buffer for the serializer holds data from the transmit format unit.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
XBUF0																															

Bits	Field Name	Description	Type	Reset
31:0	XBUF0	Transmit buffer	RW	0x0000 0000

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Table 23-646. Register Call Summary for Register MCASP_TXBUF0

Multichannel Audio Serial Port

- Serializers: [0]
- Transmit TDM Sequencer: [1]
- Data Transmission: [2] [3]
- Data Ready Status and Event/Interrupt Generation: [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14]
- Buffer Underrun Error –Transmitter: [15] [16]
- McASP DIT Transmission Mode: [17] [18]
- McASP Event Servicing: [19]
- McASP Register Summary: [20]
- McASP Register Description: [21] [22]

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23.9 Serial Low-Power Inter-Chip Media Bus Controller

This section describes the features and functions of the serial low-power inter-chip media bus (SLIMbus®) controller.

23.9.1 SLIMbus Overview

There are two SLIMbus module instantiations, SLIMBUS1 and SLIMBUS2, in the device. SLIMbus1 is implemented in the audio backend (ABE) subsystem and is intended for the connection of external audio peripherals. SLIMBUS2 is at the top-level of the device and is intended for the connection of other types of peripherals.

The SLIMbus controller provides a bidirectional, multidrop, multichannel two-line serial interface between the device and other SLIMbus components in a system, such as audio codecs, Bluetooth® modules, and FM radio receivers/transmitters. Because of its versatility, the SLIMbus controller can play the role of a wide range of peripherals and clocked frame-oriented protocols (I2S™, PCM, and TDM).

Figure 23-207 shows the SLIMbus1 controller highlight.

Figure 23-207. SLIMbus1 Highlight

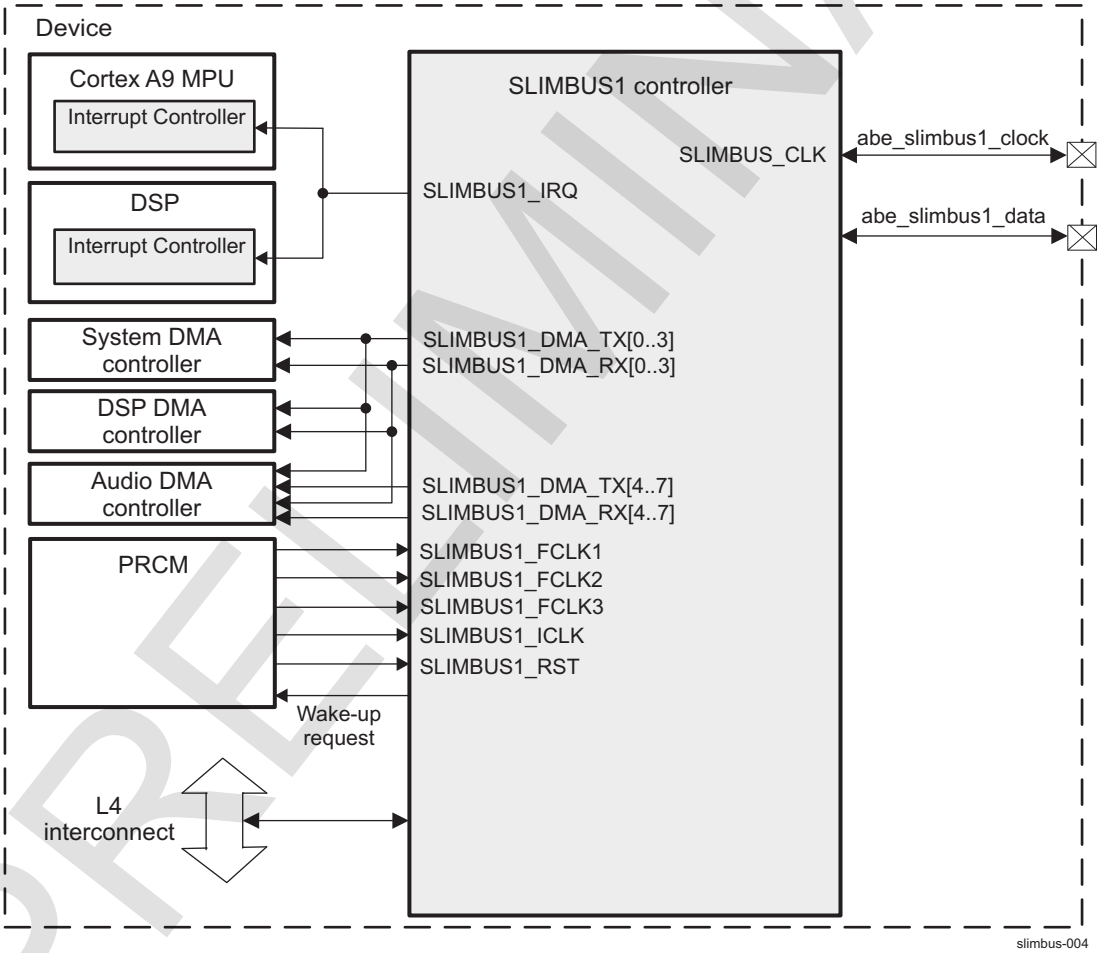

Figure 23-208 shows the SLIMbus2 controller highlight.

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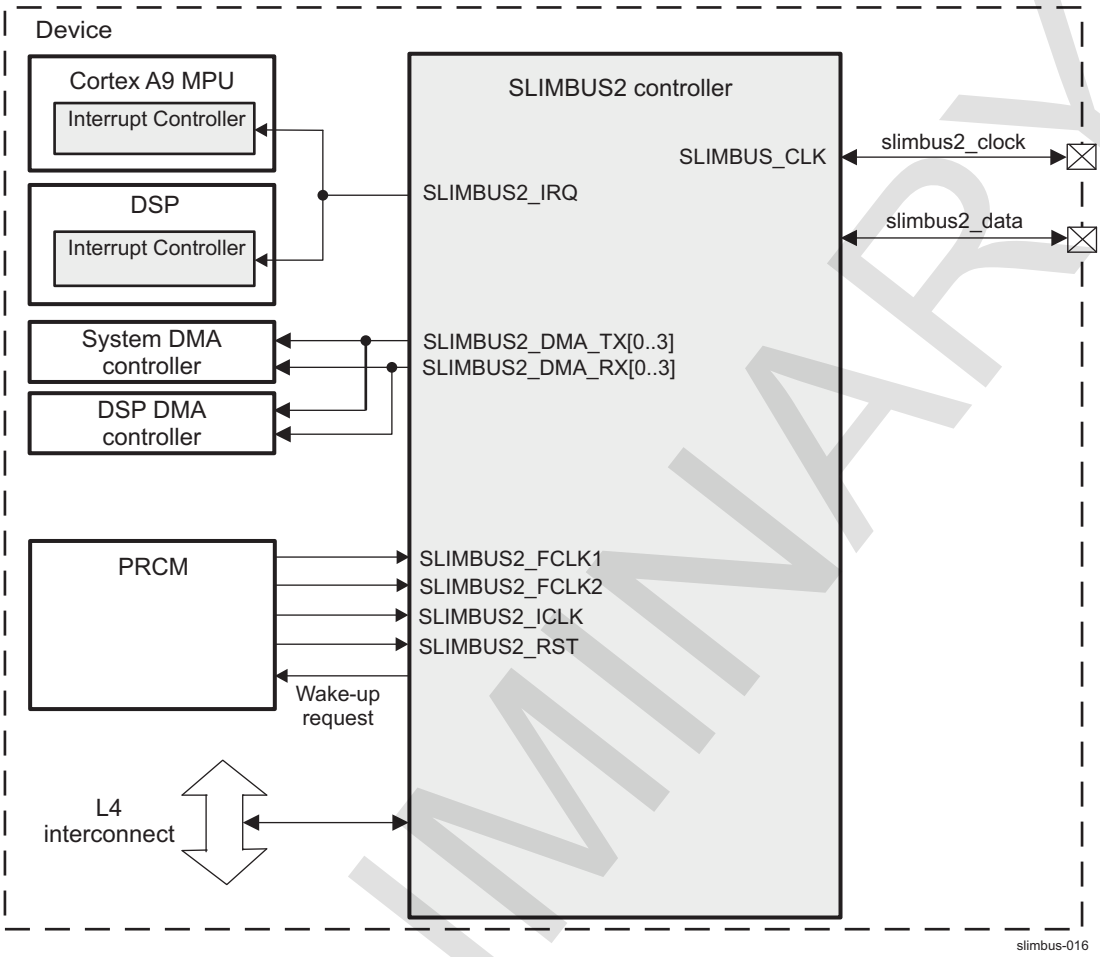
Figure 23-208. SLIMbus2 Highlight



23.9.1.1 Terminology

The SLIMbus module is by default the SLIMbus controller IP. The module implements a SLIMbus component by integrating together several submodules: a SLIMbus component contains a set of devices and the necessary logic needed to provide bus access to these devices.

Every component contains one Interface device and can contain additional devices belonging to other device classes (framer, manager, or generic devices).

- An interface device is the central status and control location of the component. All components have only one interface device.
- A framer device can generate the clock and synchronization information for the entire SLIMbus. Consequently, only one framer device (for all SLIMbus components) at a time can be active on the bus.
- A manager device controls the bus scheduling at high level: It assigns logical addresses to any device that is authorized to communicate using the bus, gives the bandwidth allocation, and so on. Only one manager device at a time can be active on the bus.
- A generic device implements the "useful" functionality of the component by sourcing/sinking the payload data. A component may include several generic devices so that each appears as a separate, standardized entity to the software driver.

NOTE: Typically, generic devices are used to transport data (rather than the specialized manager, framer, or interface devices, which typically do not feature data ports).

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A device is a separately addressable entity within a SLIMbus component. Each device belongs to a single device class. After enumeration each device is addressed with a single logical address. A device (and especially a generic device) contains data ports to transmit and/or receive data. Each port is identified within the device by its port number (PN). A port is identified within the SLIMbus by its device address (logical address or enumeration address) and PN.

An enumeration address (EA) is a 48-bit value (composed of the manufacturer ID, product code, device ID, and instance value) that allows a device to receive messages.

A logical address (LA) is an 8-bit number used to uniquely identify an enumerated device on the bus.

23.9.1.2 Main Features

Each SLIMbus module includes the following main features:

- SLIMbus controller compliant with the MIPI SLIMbus standard version 1.01.00
- Support of seven SLIMbus devices:
  - One Interface device
  - One framer device
  - One manager device
  - Four generic devices
- SLIMBUS1: Eight TX and eight RX independent ports (data channels)
- SLIMBUS2: Four TX and four RX independent ports (data channels)
- FIFO access (one FIFO for transmit and one for receive), with DMA request (one line for transmit port and one line for receive port)
- SLIMBUS1: Message FIFO size is 32 bytes for transmit and 32 bytes for receive.
- SLIMBUS2: Message FIFO size is 32 bytes for transmit and 32 bytes for receive, by default. The message FIFO size can be reprogrammed to 64 (or 16 or 48) bytes if needed. However, typical use never exceeds 32 bytes.
- Data channel FIFO size is programmable for both modules.
- Programmable data length (sample size) from 4 to 32 bits
- Programmable port assignment to either of the four generic devices
- Supported transport protocols: Isochronous, pulled, pushed, asynchronous, and extended asynchronous transport protocols (the latter two in simplex and one-half duplex mode)
- No support for locked protocol
- SLIMbus clock rate: From 0 to 24.576 MHz

Each SLIMbus module has the following characteristics:

- The component is implemented by a digital controller (the current module), plus a physical layer (a set of CLK + DATA bidirectional input/output [I/O] drivers).
- Devices are logical entities implemented by a combination of hardware (automatic address decoding for message reception) and software (message decode, encode, etc.).
- Ports (and their mapping to data channels) are supported by the module hardware-implemented data channel agents. Each agent features a unidirectional FIFO, a DMA request, support for a number of transfer protocols, etc. One agent is used per port and per data direction: Transfer protocols are unidirectional and require only one data channel agent per data channel.

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23.9.2 SLIMbus Environment

23.9.2.1 SLIMbus Component Connection Example

Figure 23-209 shows an example of a system with the SLIMbus1 controller connected to an audio peripheral component.

Figure 23-209. SLIMbus1 Typical Application System Overview

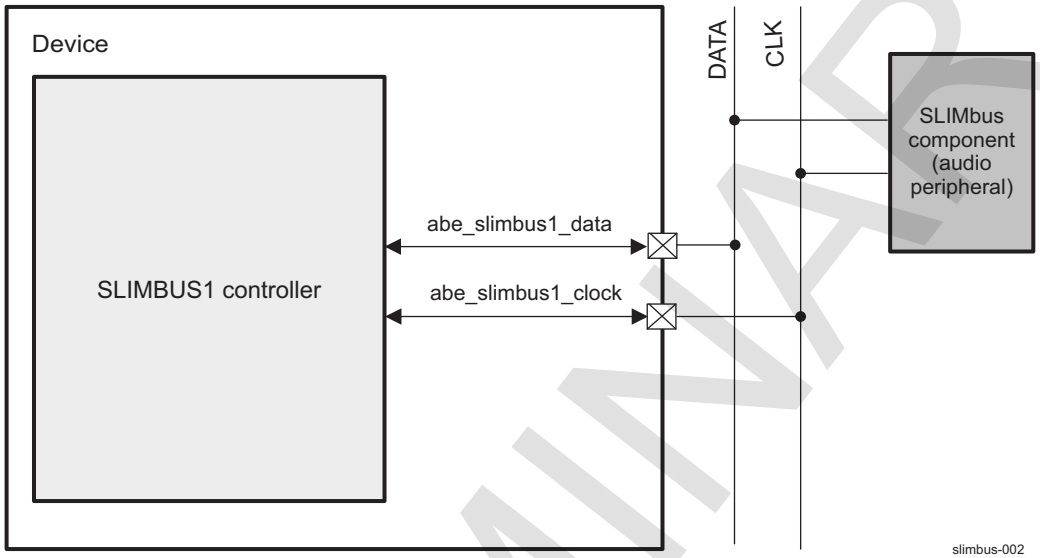
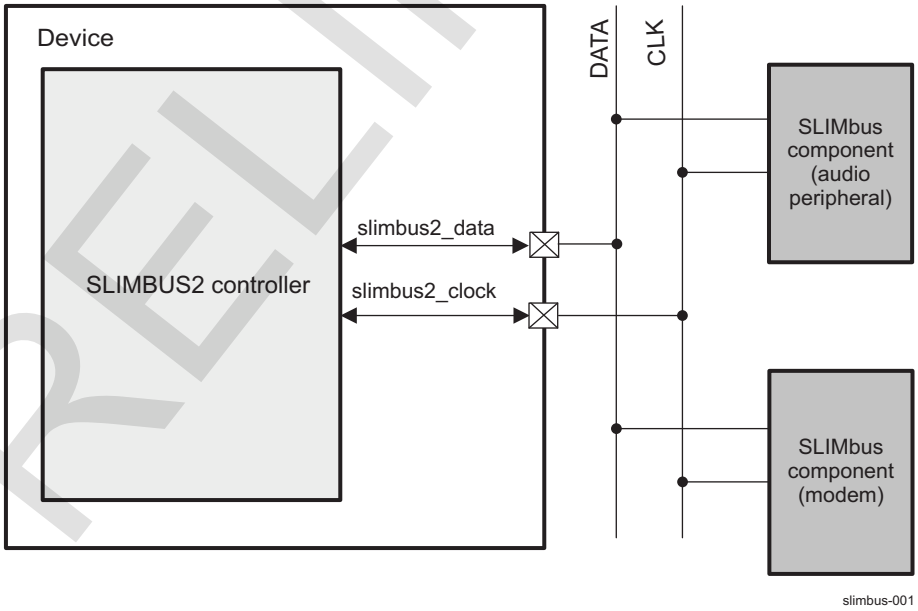


Figure 23-210 shows an example of a system with the SLIMbus2 controller connected to one audio peripheral component and one modem component.

Figure 23-210. SLIMbus2 Typical Application System Overview



The physical medium of SLIMbus is composed of two lines: CLK and DATA. All components of the bus are attached to both lines. The clock line (CLK) is driven by the (component containing the) active framer, and received (and used) by all other components on the bus. The data line (DATA) is driven alternately by all components, following the SLIMbus protocol.

The SLIMbus uses non-return-to-zero inverted (NRZI) signalling:

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- A logical 1 is represented by a transition (a change) in the physical level.
- A logical 0 is represented by the same physical level as the previous bit.

23.9.2.2 SLIMbus Functional Interface

Table 23-647 describes the SLIMbus1 interface.

Table 23-647. SLIMbus1 Signals Description

Signal	I/O	Description	Value at Reset
abe_slimbus1_data	I/O	SLIMbus1 DATA pad	1
abe_slimbus1_clock	I/O	SLIMbus1 CLOCK pad	1

Table 23-648 describes the SLIMbus2 interface.

Table 23-648. SLIMbus2 Signals Description

Signal	I/O	Description	Value at Reset
slimbus2_data	I/O	SLIMbus2 DATA pad	1
slimbus2_clock	I/O	SLIMbus2 CLOCK pad	1

23.9.2.3 SLIMbus Protocols and Data Formats

23.9.2.3.1 Frame Structure

The SLIMbus bitstream is transferred in time-division multiplexing (TDM) organization. TDM is a type of multiplexing in which two or more bitstreams are transferred apparently simultaneously as subchannels in one communication channel, but are physically taking turns on the channel. This organization allows SLIMbus to transfer control, data, and configuration information through only one DATA signal. The organization of information on the bus is called a frame structure. The frame structure is composed of five building blocks: cells, slots, subframes, frames and superframes.

- A cell is the smallest division of the SLIMbus data stream. A cell is defined as the region of the DATA line signal that lies between two consecutive positive edges of the CLK signal.
- A slot is a group of four contiguous cells. It is at the slot level that the SLIMbus DATA signal is time division-multiplexed between different channels.
- A frame is a group of 192 contiguous slots (768 cells). The first slot of each frame carries the frame-sync symbol.
- A subframe is the division of the frame structure at which control space and, if present, data space are interleaved. The subframe length can be 6, 8, 24, or 32 slots (24, 32, 96, and 128 cells).
- A superframe is composed of eight consecutive frames and contains a complete set of Framing Information.

Figure 23-211 shows the organization of the frame structure.

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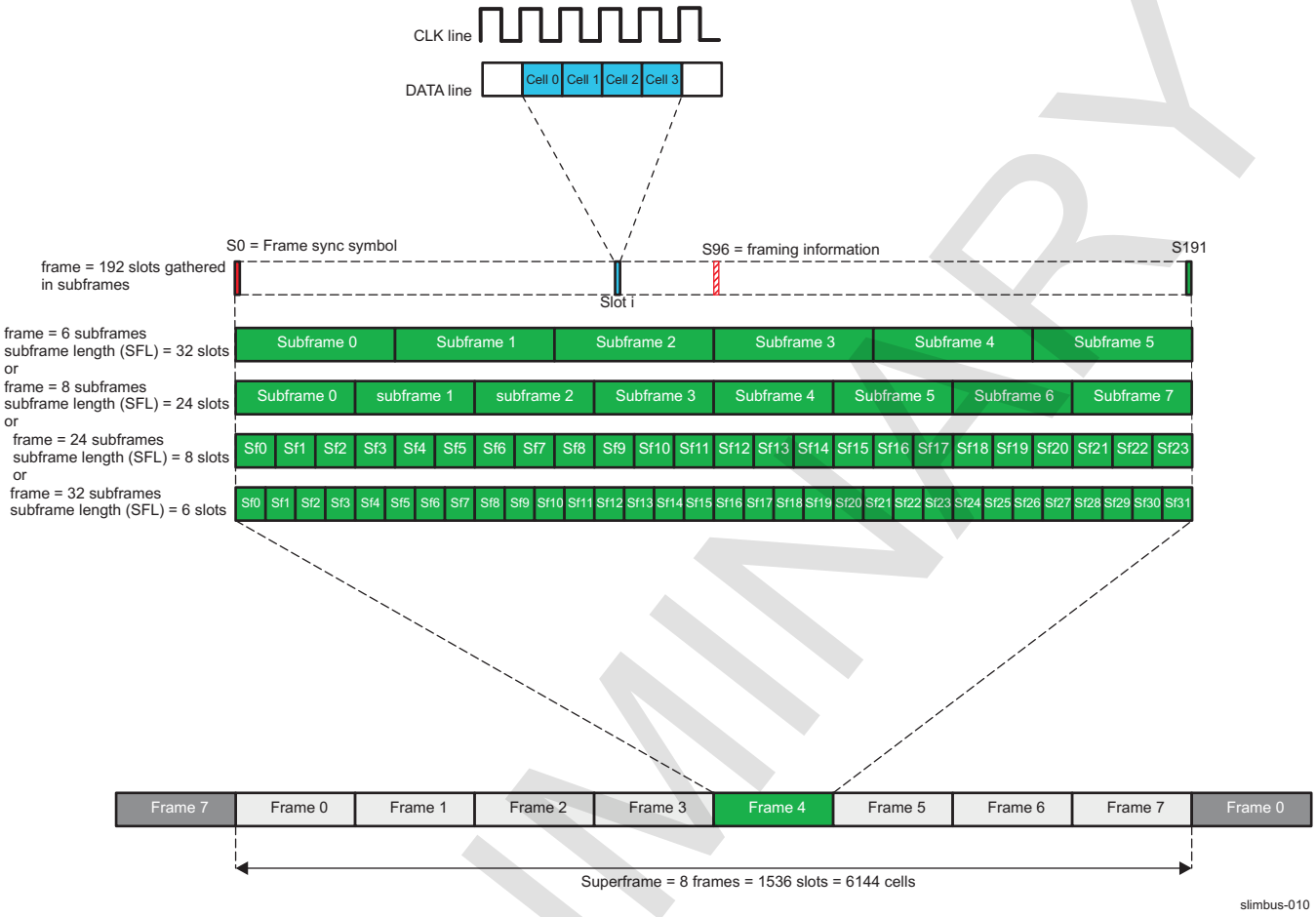
Figure 23-211. SLIMbus Frame Structure Overview



23.9.2.3.2 Control and Data Channels

A frame is divided into two parts: the control space and the data space. The control space contains the information needed for a device to discover the bus state, to track messages, and for the messages themselves. The control space size is programmable by setting the control space width (number of control space slots per subframe) and the subframe length. Data space is interleaved with control space at the subframe level. Slots not explicitly allocated to control space are considered data space. The active manager can organize these slots into data channels to transport application-specific data streams between devices on the bus. Data space can contain up to 256 data channels.

A data channel is a stream of one or more contiguous slots organized in a consistent data structure that repeats at a fixed interval. The largest possible group of contiguous slots within a data channel is known as a segment.

A data channel connects one data source port and one or several data sink ports, depending on the protocol used. A port can be connected only to a single data channel at a time.

A segment is composed of three fields: TAG, auxiliary information (AUX), and data fields. These fields are organized within the segment, as shown in Figure 23-212. The exact composition of the segment depends on the transport protocol.

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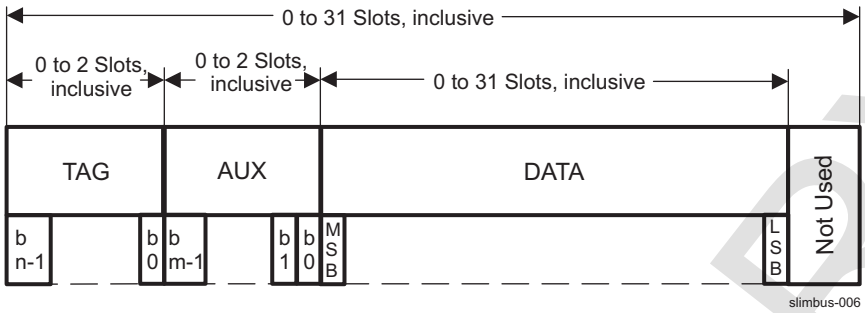
Figure 23-212. Segment Organization



23.9.2.3.2.1 Control Space Scheduling

The control space is a periodic allocation of blocks of contiguous slots with the following properties:

- Although the control space is composed of periodic blocks of 4-bit slots, it functions as a continuous stream of bits, and the interruptions for noncontrol space (that is, data space) sequences have no effect on its operation.
- The control space contains all synchronization references for the SLIMbus TDM structure; that is, it is not referenced to anything else because it is the reference.
- The control space scheduling changes only on reconfiguration boundaries.
- The subframe mode (SM) parameters unambiguously determine which slots belong to the control space.

The control space scheduling, encoded inside the SM, has the following structure:

- Each (fixed-length) frame is divided into a (whole) number of variable-sized subframes.
- The subframe length (SFL, encoded in the SM) is defined as the number of slots in a subframe.
- The control space is allocated in each subframe: The control-space width (CSW, also encoded in SM) is the number of control slots at the beginning of each subframe.

The control space is composed of 192/SFL blocks of CSW slots each, starting at intervals of SFL slots (knowing that there are 192 slots per frame). If the frame slots from j = 0 to j = (192–1) and the blocks from k = 0 to k = (192/SFL)–1 are indexed, the control space occupies in each frame, for the whole range of k:

- from slot j = (k × SFL) included
- to slot j = (k × SFL) + CSW – 1 included

The control space is further subdivided into a framing channel, guide channel, and shared message channel (SMC).

- The framing channel is composed of:
  - A 1-slot frame sync symbol (FSS), at the beginning (slot 0) of each frame. The FSS is the reference for the position of the frame in the bitstream. The fixed scheduling means that it can be retrieved and tracked regardless of the SM.
  - A framing information slot, at mid-frame (slot 96). This fixed offset means that it can also be retrieved independently of the SM. The framing information contains (among others) the value of SM, which allows all devices to determine the structure of the control space.
  - For all legal control space structures (encoded in the SM), the framing channel (slot 0 and slot 96) is inside the control space.
- The guide channel is composed of a periodic transmission of the guide byte. It is sent in the first two control space slots of each superframe (a fixed block of eight frames), after the FSS, in slot 0. The guide channel provides a sync point for the SMC (defined as follows). The two guide channel slots are not necessarily contiguous, depending on the SM, which determines the control space length and the subframe length:
  - Guide channel = slot 1 and slot 32 for SM = 11

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  - Guide channel = slot 6 and slot 12 for SM = 4
  - Guide channel = slot 1 and slot 2 for SM > 12
  - Etc.
- The SMC is by definition the rest of the control space; that is, not already allocated to the framing or guide channel. All devices may concurrently try to access the SMC following an arbitration process. The SMC contains an even number of slots (whole number of bytes) per frame and per superframe.

23.9.2.3.2.2 Data Channel Allocation, Segments

The bandwidth allocated for a given data channel is determined by the segment distribution (SD) and segment length (SL) of the channel. This allocation is fixed, periodic, reserved exclusively for the channel, and changes only on reconfiguration boundaries.

- Each data channel is allocated periodic blocks of contiguous slots, called data segments.
- Segments are all of equal length (SL) (in slots).
- Segment scheduling is periodic (with true, cycle-accurate periodicity).
  - The segment period is called the segment interval (SI), in slots, encoded in the SD).
  - There is always a whole number of data segments per superframe, called the channel rate multiplier (CRM), encoded in SD). The CRM is another way to express the period, because CRM = 1536/SI (there are 1536 slots per superframe).
  - The segment window is another way to express the period: Each superframe can be divided into CRM segment windows, of length SI. For each data channel, each segment window contains one entire contiguous segment. Segments cannot cross segment window boundaries because some of the segments would then collide with the control space.
- The constant phase of a segment is the segment offset (SO), which is the distance between the start of the segment window and the start of the segment, in slots. SO is also encoded in SD, and its value is bounded as follows:
  - Because scheduling is periodic, offsets are defined modulo SI (that is, the segment must start inside the current window, not the next. SD encoding ensures that SO < SI.
  - Segment must not overlap with control space. The consequences of that vary with SM (encoded in SM), but the following is true for all SMs:
    - SO > CSW ≥ 1: By definition, each superframe boundary is both the start of a frame (starting with CSW slots of control space; that is, at least one slot: the frame sync symbol) and the start of a segment window (the first window of the superframe, for all SD). To prevent overlap in that window, the segment must start (slot number = SO) after the control space end (slot number = CSW–1). Although it can be encoded in SD, the value SO = 0 is therefore illegal.
    - SO+SL ≤ SI: By definition, each superframe boundary is both the start of a frame (starting at the FSS slot) and the end of a segment window (the last window of the superframe, for all SD). To prevent overlap in that window, the segment must end (slot number = 192–SI+SO+SL–1) before the control space (frame sync symbol in slot 0 of following frame).

Notes on scheduling

- Data segments cannot cross a superframe/frame/subframe boundary, because the first slot (at least) of each subframe is allocated to the control space. This means that a data channel can be safely redefined (new SD, SL) at a reconfiguration boundary (which is also a superframe boundary), because that point cannot be in the middle of a segment.
- The composition of the segment, as defined by the transfer protocol (TP), and the contents of the channel have no affect on the allocation of the channel, although they must be compatible: the segment must be long enough (SL) to contain the TAG, AUX, and DATA fields. Some slots and some segments may remain unused.

23.9.2.3.2.3 Data Channel Presence

Data may or may not be present in each segment of the fixed, periodic series allocated to a data channel.

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- The channel rate (CR) is defined as the number of data segments available per second. It depends on the channel rate multiplier (number of segments per superframe, encoded in SD[11:0]), and of the SLIMbus clock frequency. It does not depend on the total length of the segment, data length, or other.
- The presence rate (PR) is defined as the number of data segments used (that is, that contain actual data) per second, and is encoded in PR[6:0]. It depends on the selected application.

Data channel presence properties:

- The data presence determination depends on the TP:
  - Pushed: TAG presence bit (P) driven by the data source
  - Pulled: TAG presence bit (P) driven by the data source upon request driven by the data sink (SRQ)
  - Asynchronous: TAG presence bit (P) driven by the segment owner (either side)
  - Isochronous: All segments contain data, no presence indication required (because it would always be asserted).
- The presence rate is necessarily smaller than the channel rate: PR ≤ CR. At best they are equal, which is always the case for isochronous protocol.
- The difference between channel rate and presence rate (CR-PR) is unused bandwidth and must be kept as small as possible in most cases. In other words, the CR must be kept as small as possible for a given PR requirement. The unused bandwidth has multiple uses:
  - Padding: Adjust the required PR to a nonmultiple bus speed.
  - PR jitter margin: Allow the PR to fluctuate around an average, with enough margin to allow faster-than-average periods, that compensate for slower-than-average periods.
  - Wasted bandwidth

When data presence is not fully determined by the properties of the data channel or by the other side of the interface (pulled data source, pushed data sink), it must be controlled based on the capacity of the local system to generate data (for sources) and absorb data (for sinks).

- Pushed or asynchronous source: The data source (transmitter) asserts the presence bit (P = 1) and transmits data when some data is available (in a transmit buffer).
- Pulled sink: The data sink (receiver) asserts the sample request (SRQ = 1) when it can accept more data (in a receive buffer).

23.9.2.3.2.4 Data Channel Segment Composition

The allocated size of a data channel segment is set by the SL parameter. The segment can be broken down into:

- TAG slots
- AUX slots
- DATA slots
- Unused slots

The parameters listed in Table 23-649 configure the different lengths.

Table 23-649. Segment Composition

Parameter	Register Field	Segment Field	Size Range (Slots)	Comments
Segment length	SLIMBUS_DCR_CONFIG1_j[9:5] / SLIMBUS_DCT_CONFIG1_j[9:5] SL	Segment	1 to 31	Encoding 0x0 is reserved.
Transport protocol	SLIMBUS_DCR_CONFIG1_j[3:0] / SLIMBUS_DCT_CONFIG1_j[3:0] TP	TAG	0, 1, 2	N/A
AUX format	SLIMBUS_DCR_CONFIG1_j[19:16] / SLIMBUS_DCT_CONFIG1_j[19:16] AF	AUX	0, 1, 2	N/A

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Table 23-649. Segment Composition (continued)

Parameter	Register Field	Segment Field	Size Range (Slots)	Comments
Data length	SLIMBUS_DCR_CONFIG1_j[14:10] / SLIMBUS_DCT_CONFIG1_j[14:10] DL	DATA	0 to 31	Encoding 0x0 is "all remaining slots," don't care if NVB is present.
Number of valid bytes	NVB (not in a register field, sent in the message)	DATA	0 to 28, even only	Encoded in AUX field, overrides DL, exists only for TP = extended asynchronous

NOTE:

- Explicit data length (DL) range is 1 to 31 slots. When encoding 0x0 is used, the DATA field occupies all remaining slots of the segment; that is, those not occupied by TAG and AUX. This allows the encoding of a 0-slot data length.
- NVB is available only in the extended asynchronous TP, which uses two TAG slots.The maximum remaining length is 31 (SL max) – 2 = 29 slots; that is, the maximum NVB is 14 bytes = 28 slots ≤ 29 (because NVB is byte-granular and cannot encode odd slot counts).
- Not all combinations are legal. For example, the DATA field of a pushed channel (TP = 0x1: 1 TAG slot) with no AUX information (AF = 0x0) and a 5-slot overall segment length (SL = 0x5) can have only one to four slots, encoded respectively as DL = 0x1, 0x2, 0x3, and 0x4/0x0.

In the current SLIMbus module (the OMAP™ SLIMbus module):

- The SL, TP, AF, and DL setup parameters are received from the appropriate control messages (inside or outside reconfiguration sequences), and programmed into appropriate control registers. They are typically static over long periods.
- The TAG slots are generated (driven) and decoded (received) on the fly by the hardware:
  - The first TAG slot (if present, for all but isochronous TP) negotiates the value of the presence bit (P).
  - The second TAG slot (for extended asynchronous TP) contains the NVB field, which indicates the number of valid bytes contained in the segment. When the presence bit (P) is not asserted, the NVB is then not driven and implicitly = 0. There is no separate NVB setup register, as for SL, TP, AF, etc.
- AUX slots (if present) go through the same data path as the DATA slots. The decoding/encoding of the AUX information is assumed to be done outside the SLIMbus controller. Their value has no effect on the protocol.
- DATA slots (if present) go through the same data path as the AUX slots. Their value has no effect on the protocol.
- The encoding/decoding, merging/splitting between the different FIFO-stored slots is assumed to be done outside the SLIMbus controller; that is, before writing to the FIFO (in transmit) and after reading from the FIFO (in receive). No support logic is provided for those functions.
- When no data is transmitted during a given segment (presence bit P/VP = 0), only the first TAG slot (if any) is actively driven and the AUX/DATA slots are not used.

Table 23-650 gives the three cases of size calculation formulas for the TAG, AUX, and DATA fields, plus the FIFO-stored section of a segment, in slots with:

- SL, DL, NVB, TP, AF, and DL, the standard SLIMbus fields, as their integer value
- Size(TP), the TAG field size in slots, as a function of the TP (see *MIPI Alliance Specification for SLIMbus Version 1.01.00*)
- Size(AF), the AUX field size in slots, as a function of the AUX format ID AF (see *MIPI Alliance Specification for SLIMbus Version 1.01.00*)

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Table 23-650. Data Segment Field Size Calculations

Case	TAG Size = Size (TP)	AUX Size = Size (AF)	DATA Field Size	FIFO-Stored Size
Extended asynchronous protocol (TP = 0x6 or 0x7)	2	0, 1, 2	1 + size(AF) + (2 x NVB)	1 + size(AF) + (2 x NVB)
Other TP, DL > 0	0, 1	0, 1, 2	DL	DL + size(AF)
Other TP, DL = 0	0, 1	0, 1, 2	SL – size(TP) – size(AF)	SL – size(TP)

23.9.2.3.3 SLIMbus Transfer Protocols

The SLIMbus module supports seven the following protocols:

- Isochronous
- Pushed
- Pulled
- Asynchronous
  - Simplex
  - Half-duplex
- Extended asynchronous
  - Simplex
  - Half-duplex

Table 23-651. SLIMbus Transfer Protocols

Transfer Protocol	Multicast Capability	Data Length	AUX Length	LPCM (DT)	CTS Forcing	Pairing
Isochronous	Yes	1–8 slots	0–2	Yes	N/A	Yes
Pushed	Yes	1–8 slots	0–2	Yes	N/A	Yes
Pulled	No	1–8 slots	0–2	Yes	N/A	Yes
Asynchronous, simplex	No	1–8 slots	0–2	Yes	Yes	No
Asynchronous, half-duplex	No	1–8 slots	0–2	Yes	Yes	No
Extended asynchronous, simplex	No	Any (NVB)	0	N/A	Yes	N/A
Extended asynchronous, half-duplex	No	Any (NVB)	0	N/A	Yes	N/A

23.9.2.3.3.1 Isochronous Transfer Protocol

The isochronous transfer protocol is a unidirectional, streaming, multicast communication mode. Data is to be present in all allocated segments (this transfer protocol has no TAG field).

- 100 percent of the bandwidth is usable for AUX + DATA slots (no control TAG overhead).
- Because no flow control exists, multiple data sinks may be connected to the same data source (multicast capability).
- The range of possible presence rates (number of segments per second) is limited to simple ratios of the SLIMbus clock. If several data streams with incompatible presence rates must be multiplexed over the same bus, no combination of isochronous-based schedulings works. In those cases, the pushed or pulled transfer protocol must be used.

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23.9.2.3.3.2 Pushed Transfer Protocol

The pushed transfer protocol is unidirectional, multicast, and controlled by the data source (transmitter), which pushes data toward the data sink (receiver). The presence of valid data in a segment is indicated by the presence (P) bit in the TAG field, driven by the source. The TAG field is composed of four bits: one reserved, one strobe (STR) bit, one reserved, and one presesnce (P) bit.

- The pushed data source is the master of the data flow through the presence (P) bit .
- The pushed data sink is slaved to the presence (P) bit..
- The TAG control field creates a 1-slot overhead per segment. The rest of the segment is usable for AUX + DATA slots.
- Because the flow control is generated by the source with no feedback from the sink, multiple data sinks may be connected to that source (multicast capability).
- The presence rate can be modulated at will from 0 (no data at all) to the full segment rate (data present in all segments) according to the requirement. Intermediate settings allow several streams with incompatible presence rates to be multiplexed over the same bus, at the cost of less than 100 percent bandwidth utilization (for example, a 44.1-kHz sample flow transmitted over a reserved 48-kHz data channel).

23.9.2.3.3.3 Pulled Transfer Protocol

The pulled transfer protocol is unidirectional, unicast, and controlled by the data sink (receiver), which pulls data from the data transmitter (source). The presence of valid data in a segment is indicated by the presence bit (P) in the TAG field, driven by the source. The TAG field is composed of four bits: one reserved, one sample request (SRQ) bit, one reserved, and one presence (P) bit.

- The pulled data sink is the master of the data flow through the (SRQ bit, itself determining the value of the presence bit (P), driven by the data source.
- The pulled data source is slaved to the SRQ bit.
- The TAG control field creates a 1-slot overhead per segment. The rest of the segment is usable for AUX + DATA slots.
- Because the flow control is generated by the sink with feedback from the source, only a single data sink may be connected to that source (unicast-only, no multicast capability).
- The presence rate can be modulated at will from 0 (no data at all) to the full segment rate (data present in all segments) according to the requirement. Intermediate settings allow several streams with incompatible presence rates to be multiplexed over the same bus, at the cost of less than 100 percent bandwidth utilization (for example, a 44.1-kHz sample flow transmitted over a reserved 48-kHz data channel).

23.9.2.3.3.4 Asynchronous Transfer Protocols

The asynchronous transfer protocols are typically used for on-demand, packet-based data transfers (that is, nonstreaming). Because the SLIMbus protocol and architecture are optimized for data streaming scenarios, asynchronous protocols are considered a useful extension rather than a central feature of the SLIMbus. An asynchronous data channel gets the same periodic, reserved, fixed-bandwidth slot allocation as a streaming (for example, isochronous) data channel.

An asynchronous data channel is a point-to-point (unicast) communication link between a primary owner device and a secondary owner device.

A half-duplex asynchronous channel is a bidirectional data channel.

- A handshake protocol is used to determine the direction of the channel through its ownership. The channel owner is the data source, and the other is the sink.
- Once the ownership (data direction) is determined, both source and sink can regulate the flow of data, depending on data availability (source) and free buffer availability (sink).
- Half-duplex ports can be used when bandwidth is sparse (compare simplex and full duplex).
- However, each half-duplex port requires two data channel agents (with FIFO and control logic) inside the controller, one in each direction, contrary to all other asynchronous modes and transfer protocols. Those two associated agents must be configured coherently.

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A simplex asynchronous channel is a unidirectional data channel, a simplified version of the half-duplex channel defined perviously. The ownership is never given to the secondary owner.

- Secondary owner never requests the channel. As a consequence, the roles are never exchanged: the primary owner is always data source, and the secondary owner always data sink.
- Simplex ports are used in pairs of opposite directions to implement full-duplex communication, where each direction has its own reserved bandwidth. As far as the controller is concerned, the two simplex links are treated as fully independent data channels, with independent configurations; only the higher layers (software) associate the two.
- Two simplex ports use the same number of data channel agents (that is, FIFOs and control logic) as a single half-duplex port (two per controller in each case; the only difference is in the bandwidth management.

23.9.2.3.3.5 Extended Asynchronous Transfer Protocols

The extended asynchronous transfer protocols are extensions of the plain asynchronous transfer protocol. The main features are retained: point-to-point (unicast) between a primary and a secondary owner, simplex (unidirectional) or half-duplex (bidirectional), and so on.

The difference lies in a more flexible management of the DATA slots: In the plain asynchronous TP, each segment contains no data (presence [P] bit = 0) or a fixed amount of data (P = 1), preconfigured for all segments. In the extended asynchronous mode, a number of valid bytes (NVB) 4-bit field is added before each segment, in a second TAG slot, to indicate a variable number of significant DATA slots (the granularity is 1 byte = 2 slots).

NOTE: AUX slots (when present; not in the current implementation) are not counted in NVB, just as they are not counted in DL in the plain asynchronous TP.

23.9.2.3.4 Half-Duplex Versus Full-Duplex Asynchronous Configurations

Half-duplex and full-duplex modes are similar in their operation, in that they use two data channel agents (FIFOs and associated control hardware) in opposite directions (one TX, one RX) to transmit and receive data over a bidirectional, unicast (point-to-point) asynchronous link. However, there are differences:

- The half-duplex setup uses a single data channel (in the SLIMbus sense); that is, a single reserved data space segment allocation, used alternately in both directions, according to the dynamic ownership negociated in the TAG slots.
- The full-duplex setup uses two data channels (in the SLIMbus sense); that is, two separate reserved data space segment allocations, each used in a fixed direction (opposite of the other) (that is, with no ownership change).

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23.9.3 SLIMbus Integration

Figure 23-213 and Figure 23-214 show the integration of the two SLIMbus module instantiations in the device. The SLIMBUS1 module is part of the ABE module

Figure 23-213. SLIMBUS1 Integration

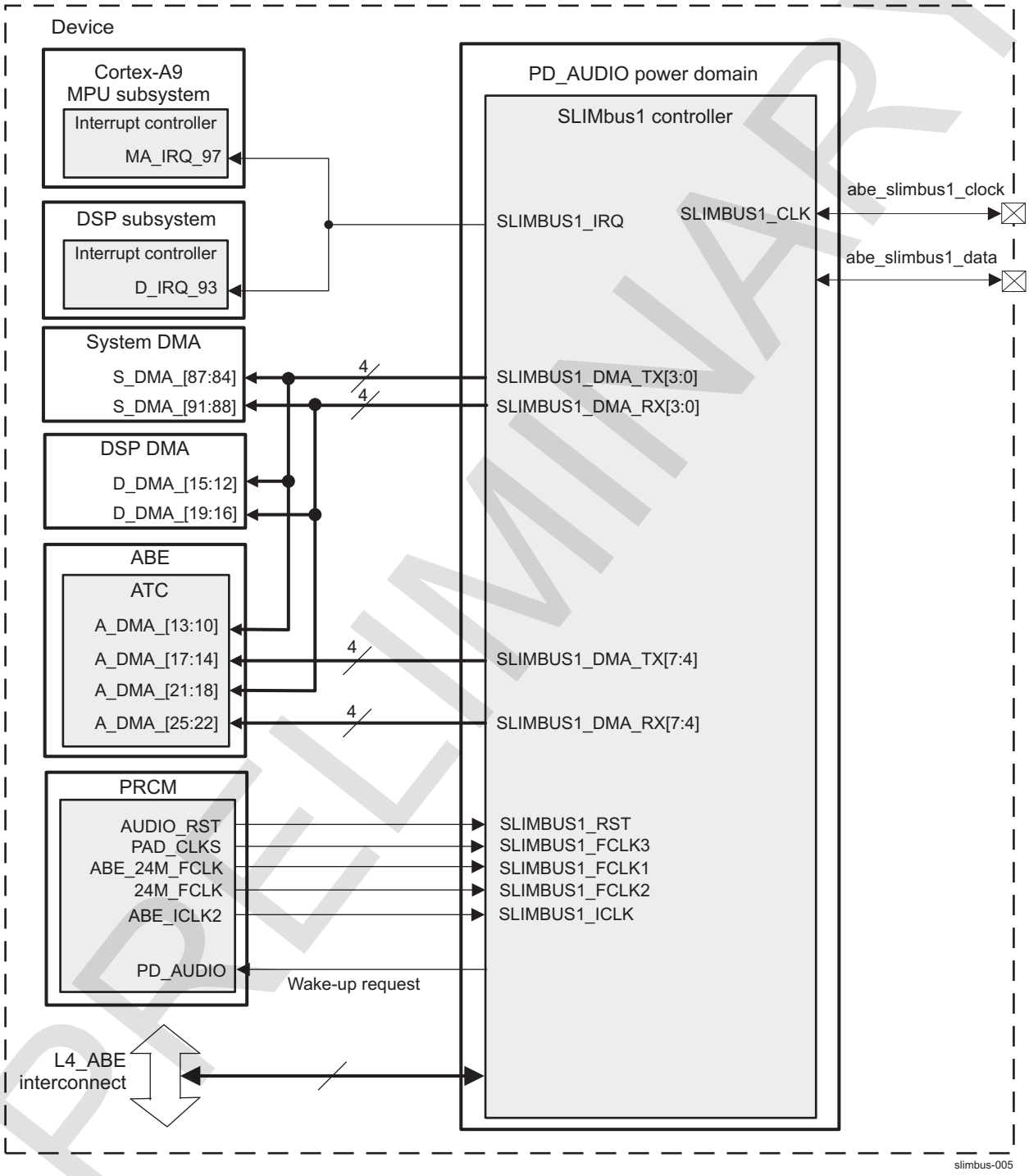

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Figure 23-214. SLIMBUS2 Integration

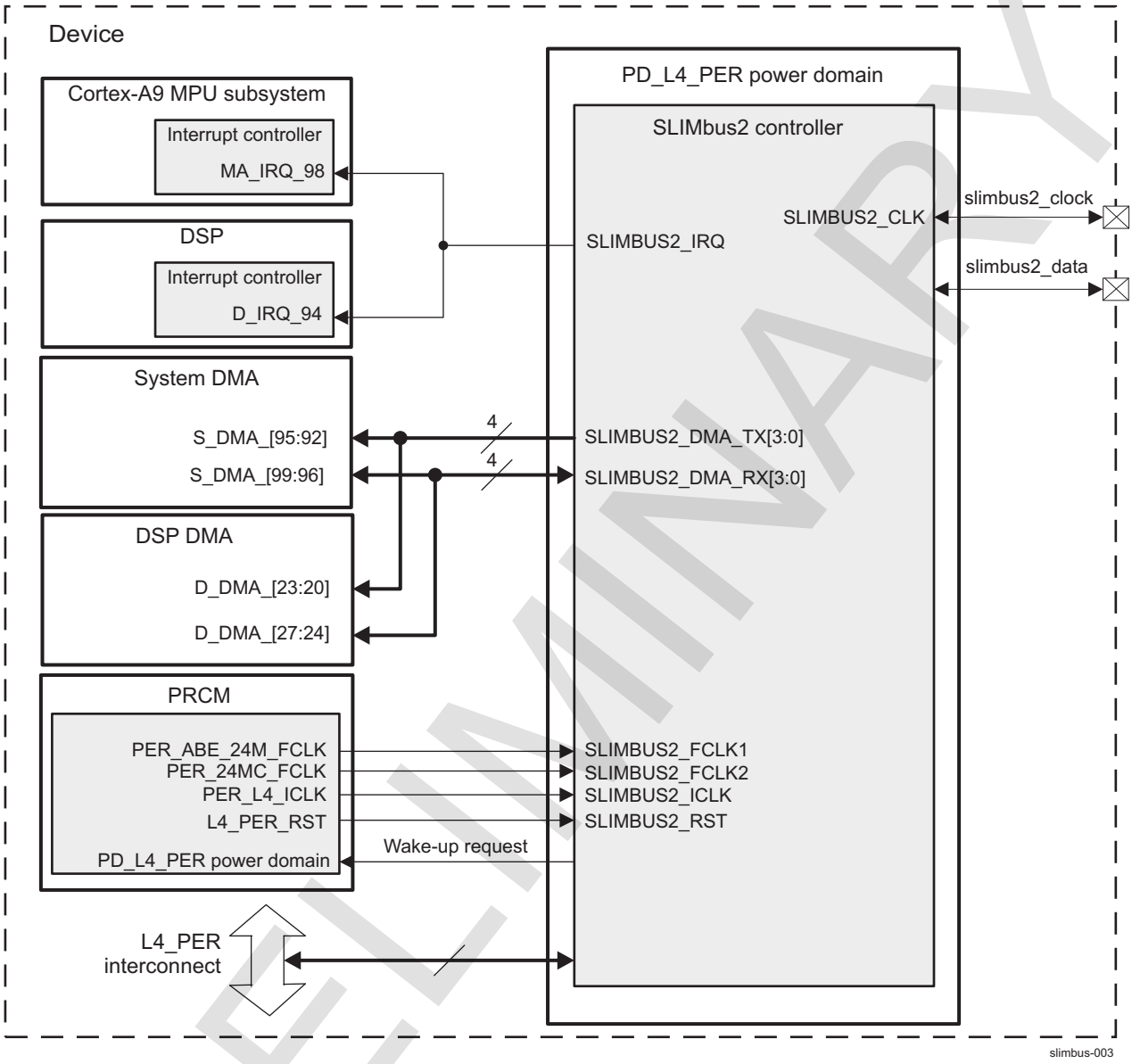

Table 23-652 through Table 23-654 summarize the integration of the modules in the device.

Table 23-652. Integration Attributes

Module Instance	Attributes		
	Power Domain	Wake-Up Capability	Interconnect
SLIMBUS1	PD_AUDIO	Yes	L4_ABE
SLIMBUS2	PD_L4_PER	Yes	L4_PER

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Table 23-653. Clocks and Resets

Clocks				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
SLIMBUS1	SLIMBUS1_FCLK3	PAD_CLKS	PRCM	Functional clock, divided by 4 or more inside SLIMbus module. The source is the abe_clks pin gated by the PRCM module.
	SLIMBUS1_FCLK1	ABE_24M_FCLK	PRCM	Functional clock, divided by 4 or more inside SLIMbus module
	SLIMBUS1_ICLK	ABE_ICLK2	PRCM	Interface clock
	SLIMBUS1_FCLK2	24M_FCLK	PRCM	Functional clock, divided by 4 or more inside SLIMbus module
	SLIMBUS1_CLK	SLIMBUS_UCLKS	abe_slimbus1_clock pin	SLIMBUS clock, may or may not be locally generated
SLIMBUS2	SLIMBUS2_ICLK	PER_L4_ICLK	PRCM	Interface clock
	SLIMBUS2_CLK	PAD_SLIMBUS_CLKS	slimbus2_clock pin	SLIMBUS clock, may or may not be locally generated
	SLIMBUS2_FCLK2	PER_24MC_FCLK	PRCM	Functional clock, divided by 4 or more inside SLIMbus module
	SLIMBUS2_FCLK1	PER_ABE_24M_FCLK	PRCM	Functional clock, divided by 4 or more inside SLIMbus module
Resets				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
SLIMBUS1	SLIMBUS1_RST	AUDIO_RST	PRCM	Reset to SLIMbus1 module
SLIMBUS2	SLIMBUS2_RST	L4_PER_RST	PRCM	Reset to SLIMbus2 module

Table 23-654. Hardware Requests

Interrupt Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
SLIMBUS1	SLIMBUS1_IRQ	MA_IRQ_97	Cortex-A9 INTC	SLIMBUS1 interrupt to Cortex-A9 MPU
	SLIMBUS1_IRQ	D_IRQ_93	DSP INTC	SLIMBUS1 interrupt to DSP
SLIMBUS2	SLIMBUS2_IRQ	MA_IRQ_98	Cortex-A9 INTC	SLIMBUS2 interrupt to Cortex-A9 MPU
	SLIMBUS2_IRQ	D_IRQ_94	DSP INTC	SLIMBUS2 interrupt to DSP
DMA Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
SLIMBUS1	SLIMBUS1_DMA_TX0	A_DMA_10	aDMA (Audio DMA)	SLIMbus module 1 – transmit request channel 0
	SLIMBUS1_DMA_TX1	A_DMA_11	aDMA	SLIMbus module 1 – transmit request channel 1
	SLIMBUS1_DMA_TX2	A_DMA_12	aDMA	SLIMbus module 1 – transmit request channel 2
	SLIMBUS1_DMA_TX3	A_DMA_13	aDMA	SLIMbus module 1 – transmit request channel 3
	SLIMBUS1_DMA_TX4	A_DMA_14	aDMA	SLIMbus module 1 – transmit request channel 4
	SLIMBUS1_DMA_TX5	A_DMA_15	aDMA	SLIMbus module 1 – transmit request channel 5
	SLIMBUS1_DMA_TX6	A_DMA_16	aDMA	SLIMbus module 1 – transmit request channel 6
	SLIMBUS1_DMA_TX7	A_DMA_17	aDMA	SLIMbus module 1 – transmit request channel 7
	SLIMBUS1_DMA_RX0	A_DMA_18	aDMA	SLIMbus module 1 – receive request channel 0

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Table 23-654. Hardware Requests (continued)

	SLIMBUS1_DMA_RX1	A_DMA_19	aDMA	SLIMbus module 1 – receive request channel 1
	SLIMBUS1_DMA_RX2	A_DMA_20	aDMA	SLIMbus module 1 – receive request channel 2
	SLIMBUS1_DMA_RX3	A_DMA_21	aDMA	SLIMbus module 1 – receive request channel 3
	SLIMBUS1_DMA_RX4	A_DMA_22	aDMA	SLIMbus module 1 – receive request channel 4
	SLIMBUS1_DMA_RX5	A_DMA_23	aDMA	SLIMbus module 1 – receive request channel 5
	SLIMBUS1_DMA_RX6	A_DMA_24	aDMA	SLIMbus module 1 – receive request channel 6
	SLIMBUS1_DMA_RX7	A_DMA_25	aDMA	SLIMbus module 1 – receive request channel 7
	SLIMBUS1_DMA_TX0	S_DMA_84	sDMA (System DMA)	SLIMbus module 1 – transmit request channel 0
	SLIMBUS1_DMA_TX1	S_DMA_85	sDMA	SLIMbus module 1 – transmit request channel 1
	SLIMBUS1_DMA_TX2	S_DMA_86	sDMA	SLIMbus module 1 – transmit request channel 2
	SLIMBUS1_DMA_TX3	S_DMA_87	sDMA	SLIMbus module 1 – transmit request channel 3
	SLIMBUS1_DMA_RX0	S_DMA_88	sDMA	SLIMbus module 1 – receive request channel 0
	SLIMBUS1_DMA_RX1	S_DMA_89	sDMA	SLIMbus module 1 – receive request channel 1
	SLIMBUS1_DMA_RX2	S_DMA_90	sDMA	SLIMbus module 1 – receive request channel 2
	SLIMBUS1_DMA_RX3	S_DMA_91	sDMA	SLIMbus module 1 – receive request channel 3
	SLIMBUS1_DMA_TX0	D_DMA_12	dDMA (DSP DMA)	SLIMbus module 1 – transmit request channel 0
	SLIMBUS1_DMA_TX1	D_DMA_13	dDMA	SLIMbus module 1 – transmit request channel 1
	SLIMBUS1_DMA_TX2	D_DMA_14	dDMA	SLIMbus module 1 – transmit request channel 2
	SLIMBUS1_DMA_TX3	D_DMA_15	dDMA	SLIMbus module 1 – transmit request channel 3
	SLIMBUS1_DMA_RX0	D_DMA_16	dDMA	SLIMbus module 1 – receive request channel 0
	SLIMBUS1_DMA_RX1	D_DMA_17	dDMA	SLIMbus module 1 – receive request channel 1
	SLIMBUS1_DMA_RX2	D_DMA_18	dDMA	SLIMbus module 1 – receive request channel 2
	SLIMBUS1_DMA_RX3	D_DMA_19	dDMA	SLIMbus module 1– receive request channel 3
SLIMBUS2	SLIMBUS2_DMA_TX0	D_DMA_20	dDMA	SLIMbus module 2 – transmit request channel 0
	SLIMBUS2_DMA_TX1	D_DMA_21	dDMA	SLIMbus module 2 – transmit request channel 1
	SLIMBUS2_DMA_TX2	D_DMA_22	dDMA	SLIMbus module 2 – transmit request channel 2
	SLIMBUS2_DMA_TX3	D_DMA_23	dDMA	SLIMbus module 2 – transmit request channel 3
	SLIMBUS2_DMA_RX0	D_DMA_24	dDMA	SLIMbus module 2 – receive request channel 0

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Table 23-654. Hardware Requests (continued)

SLIMBUS2_DMA_RX1	D_DMA_25	dDMA	SLIMbus module 2 – receive request channel 1
SLIMBUS2_DMA_RX2	D_DMA_26	dDMA	SLIMbus module 2 – receive request channel 2
SLIMBUS2_DMA_RX3	D_DMA_27	dDMA	SLIMbus module 2 – receive request channel 3
SLIMBUS2_DMA_TX0	S_DMA_92	sDMA	SLIMbus module 2 – transmit request channel 0
SLIMBUS2_DMA_TX1	S_DMA_93	sDMA	SLIMbus module 2 – transmit request channel 1
SLIMBUS2_DMA_TX2	S_DMA_94	sDMA	SLIMbus module 2 – transmit request channel 2
SLIMBUS2_DMA_TX3	S_DMA_95	sDMA	SLIMbus module 2 – transmit request channel 3
SLIMBUS2_DMA_RX0	S_DMA_96	sDMA	SLIMbus module 2 – receive request channel 0
SLIMBUS2_DMA_RX1	S_DMA_97	sDMA	SLIMbus module 2 – receive request channel 1
SLIMBUS2_DMA_RX2	S_DMA_98	sDMA	SLIMbus module 2 – receive request channel 2
SLIMBUS2_DMA_RX3	S_DMA_99	sDMA	SLIMbus module 2 – receive request channel 3

NOTE:

- For the description of the interrupt, see Section 23.9.4.11, *Interrupt Service Routines*, and Chapter 17, *Interrupt Controllers*.
- For the description of the DMA, see Section 23.9.4.5.2, *Data Input/Output: DMA Request Mode*, and Chapter 16, *SDMA*.

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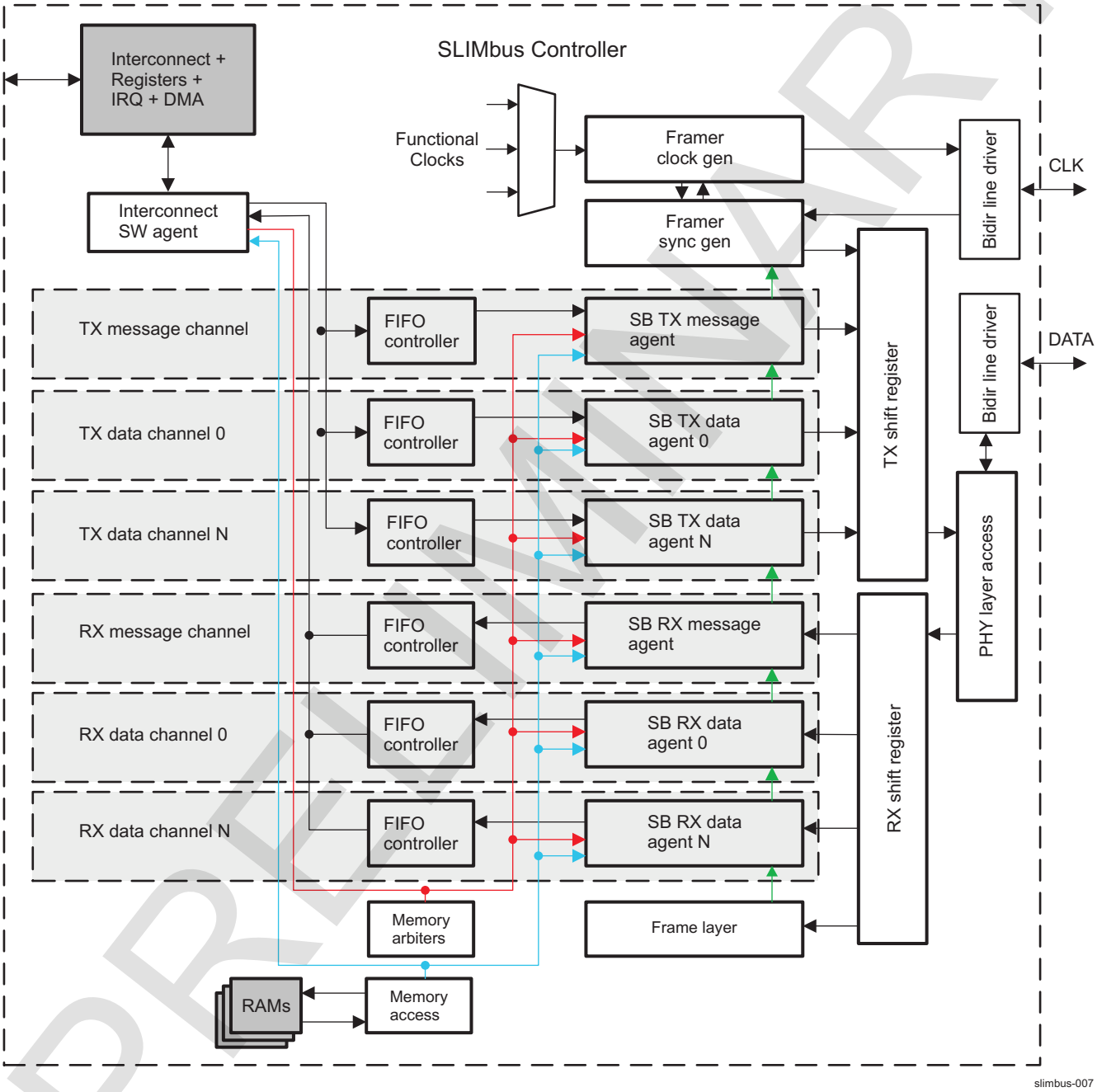
23.9.4 SLIMbus Functional Description

23.9.4.1 SLIMbus Block Description

Figure 23-215 shows the the overall architecture of a SLIMbus module.

Figure 23-215. SLIMbus Block Diagram



- The red arrows represent the shared memory arbitration interface, from the arbiter to each agent.
- The blue arrows represent the shared memory access interface, from the memory access module to each agent.
- The green arrows represent the frame layer sync information broadcasted to all SB-side agents.

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23.9.4.2 SLIMbus Clock Configuration

Most of the SLIMbus module runs off two main clocks: the L4 interface clock for the data input and output registers, and the control and status control registers; and the SLIMbus clock, taken from the serial interface (CLK line) for the SLIMbus-side logic.

The SLIMbus controller operates as clock source component (active framer), which drives the SLIMbus clock line CLK, or as clock receiver component, which gets its clock from the same CLK line.

- As a clock receiver, the module has by definition no control over the clock activity and can perform required operations based on that. Even clock pause is mostly transparent as far as the receiver logic is concerned (that is, everything happens as if time had stopped at the clock pause, and activity resumes seamlessly upon clock restart).
- As a clock source (also called active framer), the module relies on a local functional clock to drive the SLIMbus clock line. Such a functional clock is selected out of the available clock inputs. The appropriate input is expected to be active whenever it is needed (that is, when selected and used to run the SLIMbus clock and/or the module internal logic). In this case, the SLIMbus clock output is generated by selecting and dividing one functional clock input provided to the controller. Internal logic selects and divides the appropriate one depending on the SLIMbus configuration.

23.9.4.3 Software Reset

The SLIMBUS_CMP_SYSCONFIG[1] SOFTRESET bit controls the software reset; writing 1 to this bit starts a soft reset sequence.

23.9.4.4 System Power Management and Wakeup

23.9.4.4.1 Wake-Up Request

Both SLIMbus controllers are wake-up capable.

There are several levels of wake-up capability:

- Most IRQ events are potential wake-up sources, because they can occur while the external interface is idle, assuming the external and SLIMbus clocks are still running.
- The clock restart IRQ event (the SLIMBUS_FR_INFO[5] CLOCK_RESTART bit) following a clock pause is the only one that can take place when all module clocks are stopped.

23.9.4.4.2 Power Management

Table 23-655 describes power-management features available for the SLIMbus module.

NOTE: For the description of the IdleMode feature, see Chapter 3, *Power, Reset, and Clock Management*.

Table 23-655. Local Power-Management Features

Feature	Registers	Description
Clock auto gating	SLIMBUS_CMP_SYSCONFIG[8] AUTOGATINGDISABLE	Internal clock autogating is intended to conserve power when the module is not in use.
Slave idle modes	SLIMBUS_CMP_SYSCONFIG[3:2] IDLEMODE	Force-idle, no-idle, smart-idle, and smart-idle wake-up-capable modes are available.
Wake-up sources enable	SLIMBUS_FR_INFO[5] CLOCK_RESTART and most IRQ events	See Section 23.9.4.4.1

23.9.4.4.3 SLIMbus Boot and Reset Procedures

The SLIMbus standard defines different levels of resets and default states from which to boot. They are implemented by a mix of software and hardware.

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NOTE: This does not include the module-wide software or hardware resets of the controller, which simply wipe off the entire logic with no consideration for any potentially ongoing SLIMbus operation.

Table 23-656 summarizes the control bit fields to set in the various reset and/or boot sequences. Any combination other than the ones described here may yield unpredictable results.

Table 23-656. Reset and Boot Control Summary

Register / Field	SLIMBUS_FR_CONTROL		SLIMBUS_FL_CONTROL		
Reset/Boot Case	**Boot**	**bus_reset**	**Boot**	**bus_shutdown**	**force_reconfigure (1)**
Clock receiver boot (2)			1		1
Clock source boot	1				1
Clock receiver component reset (2) (3)			1		1
Clock source component reset		1			1
Bus reset (4) (5)		1			
Bus shutdown (4)				1	

(1) When used, the SLIMBUS_FL_CONTROL[2] FORCE_RECONFIGURE bit must be set (written to 1) last, because its action can be immediate. Other control bits can be set in any order.

(2) The controls for boot and component reset look identical for the clock receiver. The difference is in the initial state of the component: in the first case, the component is in the undefined state (not started), in the second case it is operational.

(3) The clock receiver component reset case shown here corresponds to the reception by the component interface of the RESET_DEVICE. In the two other cases, a bus reset is detected and the hardware automatically goes to the correct state.

(4) The bus reset and shutdown belong to a reconfiguration (message) sequence and take place on the reconfiguration boundary: the SLIMBUS_FL_CONTROL[2] FORCE_RECONFIGURE is therefore not used.

(5) The bus reset is executed only by the clock source (active framer).

23.9.4.4.3.1 Clock Receiver Component Boot

A clock receiver boot sequence is initiated when a component that is not the default active framer decides to join the SLIMbus. Provided the clock line is driven (that is, a framer is active), the clock receiver must eventually acquire the synchronization.

Clock receiver boot sequence:

- Initial state: Out of hardware module reset or following a SLIMbus shutdown
- Write 1 to the SLIMBUS_FL_CONTROL[0] BOOT bit to start the clock receiver.
- Write 1 to the SLIMBUS_FL_CONTROL[2] FORCE_RECONFIGURE bit.

23.9.4.4.3.2 Clock Source Component Boot

Source component is, by definition, the component including the active framer (that is, the clock driver). A clock source boot sequence is initiated when a component that is the default active framer joins the SLIMbus. The clock source drives the clock line and runs the SLIMbus boot sequence, allowing the connected clock receivers to synchronize to it.

NOTE: The component knows in advance that it is the only default active framer, in charge of booting the bus: That information must be available for the component, as well as the default SM, CG, and RF configuration parameters.

Clock source boot sequence:

- Initial state: The component is the designated default active framer and is out of hardware module reset or follows a SLIMbus shutdown.
- Write 1 to the SLIMBUS_FR_CONTROL[0] BOOT bit.
- Write the basic bus configuration, to be used by the active framer device to generate the clock and the framing channel contents:
  - Subframe mode (M) in the SLIMBUS_FL_SM[4:0] SM bit field: Sets the control space width and

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subframe length

- Clock gear (G) in the SLIMBUS_FL_CG[3:0] CG bit field: The root/SLIMbus frequency ratio is defined as $2^{(10-CG)}$
- Root frequency (F) in the SLIMBUS_FL_RF[3:0] RF bit field: Sets the root frequency
- Clock source selection, in the SLIMBUS_FR_CLOCK_SOURCE[5:3] CLKSEL and SLIMBUS_FR_CLOCK_SOURCE[2:0] CLKDIV bit fields
- The relationships (and limitations) between CG, RF, and the clock source selection also apply here.

- Write 1 to the SLIMBUS_FL_CONTROL[2] FORCE_RECONFIGURE bit to trigger the sequence execution
- The clock source starts immediately and eventually drives the CLK line and allows other components (clock receivers) to join the bus.

23.9.4.4.3.3 Bus Reset

A bus reset is a specific DATA and CLK sequence run by the active framer, scheduled after the bus has already booted, and which causes all components of the bus to reset. For more information about the bus reset detection mechanism, see Section 23.9.4.4.3.4, *Component Reset*.

The bus reset is requested by the manager device through a reconfiguration sequence, and is run by the active framer starting at the following reconfiguration boundary.

Bus reset sequence, to be executed by all components:

- Write 1 to the SLIMBUS_FR_CONTROL[1] BUS_RESET bit.
- Wait for the end of the reconfiguration sequence to execute:
  - On the clock source (active framer), this must trigger a bus reset sequence.
  - On any other device (that is,. a clock receiver), this must have no direct effect (other than clearing the SLIMBUS_FR_CONTROL[1] BUS_RESET bit).
  - Because all bus devices are being reset (bus is rebooted, almost from the beginning), the confguration (M, G, F parameters) can change (because those parameters must be reacquired by all attached devices as part of the resynchronization sequence, this is not a problem).

23.9.4.4.3.4 Component Reset

A component reset implies the (device) reset of all devices within that component. When a component reset condition is detected, software must therefore run the device reset sequence defined in Section 23.9.4.4.3.5, *Device Reset*, as many times as necessary. Additional operations are also required.

A component reset has two possible causes:

- Bus reset sequence detected
- Interface device of the local component receives a reset order. (This is not a reconfiguration message; that is, the reset is effective immediately upon reception. Nevertheless, a specific action is needed to perform the device reset:)
  - Use the SLIMBUS_FL_CONTROL[1] COMPONENT_RESET bit.
  - If the component is a clock receiver (clock receiver FSM), the sequence is :
    - Write 1 to the SLIMBUS_FL_CONTROL[0] BOOT bit.
    - Write 1 to the SLIMBUS_FL_CONTROL[2] FORCE_RECONFIGURE bit to trigger the reset execution.
  - If the component is the active framer (clock source FSM), the sequence is :
    - Write 1 to the SLIMBUS_FR_CONTROL[1] BUS_RESET bit.
    - Write 1 to the SLIMBUS_FL_CONTROL[2] FORCE_RECONFIGURE bit to trigger the reset execution.
    - The effect of a clock source component reset is the same as a bus reset, except it takes place immediately instead of waiting for a reconfiguration boundary.

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23.9.4.4.3.5 Device Reset

A device reset can have several causes:

- Component reset of the receiver component containing that device, caused by a bus reset reconfiguration message. If the cause of the device reset is a component reset, the sequence defined in Section 23.9.4.4.3.4, *Component Reset*, is applied.
- A reset order targeted at the device itself. (This is not a reconfiguration message; that is, it is effective immediately upon reception. In this case, no additional action is required.)

The following sequence must be executed for all devices:

- Release the logical address (LA) of the device by clearing (writing 0 to) the SLIMBUS_DEV_LA_i[8] LA_ENABLE bit. It is assumed that the SLIMBUS_DEV_LA_i[9] EA_ENABLE bit remains set (1). The device returns to the default, nonenumerated state where it is identified by its hard-coded enumeration address (EA). The SLIMBUS_DEV_LA_i[7:0] LA bit may be assigned to another device by the bus manager (that is, keeping track of all device resets).
- The following hardware bits must also be cleared (by writing 1) when the device to which they belong (identified by the message target LA) is being reset:
  - The SLIMBUS_FR_INFO[2] FS, SLIMBUS_FR_INFO[1] FI, and SLIMBUS_FR_INFO[0] GC_TX_COL bits (framer device-specific IEs)
  - The SLIMBUS_FL_INFO[2] LOST_FS, SLIMBUS_FL_INFO[1] LOST_SFS, and SLIMBUS_FL_INFO[0] LOST_MS bits (interface device-specific IEs)
  - The SLIMBUS_SMR_INFO[0] MC_TX_COL, SLIMBUS_SMT_INFO[0] MC_TX_COL bit (primitives of interface device-specific IE)
  - The SLIMBUS_DCT_INFO_j[0]/SLIMBUS_DCR_INFO_j[0] DATA_TX_COL bit (generic device IEs)
- Reset all pending reconfiguration parameters by writing 1 to the SLIMBUS_FL_CONTROL[7] CLEAR_RECONFIGURATION bit (see Section 23.9.4.4.4).
- Reset all device ports (if any), as explained in Section 23.9.4.4.3.6, *Port Reset*.

23.9.4.4.3.6 Port Reset

A port reset can have several causes:

- Device reset of the device to which the port belongs, which may be part of a wider component of the bus reset
- Synchronization loss. Although all ports are reset, this is not equivalent to a device reset, because logical addresses are not cleared.
- Specific software messages reception

23.9.4.4.3.7 Bus Shutdown

A bus shutdown stops definitively all SLIMbus activity (CLK and DATA) and brings the bus back to its original (preboot) state. When the shutdown is executed, the system must reboot from scratch.

The bus shutdown is requested by the manager device through a reconfiguration sequence.

Bus shutdown sequence:

- Write 1 to the SLIMBUS_FL_CONTROL[6] BUS_SHUTDOWN bit. This is valid for an active framer (clock source) or a clock receiver.
- Wait for the end of the reconfiguration sequence to execute.
- Beyond that point, the bus is down and can be restarted only by a boot sequence.

23.9.4.4.4 SLIMbus Reconfigure Parameters

During a reconfiguration message sequence, the controller accumulates parameter changes to be applied at the following reconfiguration boundary. If the sequence does not complete correctly, all changes are discarded. In specific boot and reset cases, the parameters are also set or reset automatically.

This section provides an overview of all the configuration register fields and their use.

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Writing 1 to the SLIMBUS_FL_CONTROL[7] CLEAR_RECONFIGURATION bit has an immediate effect on the configuration registers.

- The following registers fields revert to their current value; that is, the value currently used for SLIMbus operations. The value previously written in is discarded.
  - The SLIMBUS_FL_SM[4:0] SM bit field: Sets the control space width and subframe length.
  - The SLIMBUS_FL_CG[3:0] CG bit field: The root/SLIMbus frequency ratio is defined as $2^{(10-G)}$.
  - The SLIMBUS_FL_RF[3:0] RF bit field: Sets the root frequency
  - The SLIMBUS_FR_CLOCK_SOURCE[5:3] CLKSEL: Clock input source selection
  - SLIMBUS_FR_CLOCK_SOURCE[2:0] CLKDIV bit field: Root divider ratio, applied on clock input to obtain root clock, to be used at next reconfiguration boundary. Input/ root frequency ratio is defined as $2^{(CLKDIV-1)}$.
  - The SLIMBUS_DCT_CONFIG1_j[31]/SLIMBUS_DCR_CONFIG1_j[31] ENABLE bit (this field is also cleared when the superframe or frame sync is lost): Data channel agent enabling control
  - The SLIMBUS_DCT_CONFIG1_j[15]/SLIMBUS_DCR_CONFIG1_j[15] CL bit: Channel link configuration mode selection
  - The SLIMBUS_DCT_CONFIG1_j[26:20]/SLIMBUS_DCR_CONFIG1_j[26:20] PR bit field: Presence rate configuration
  - The SLIMBUS_DCT_CONFIG1_j[3:0]/SLIMBUS_DCR_CONFIG1_j[3:0] TP bit field: Transfer protocol selection
  - The SLIMBUS_DCT_CONFIG2_j[11:0]/SLIMBUS_DCR_CONFIG2_j[11:0] SD bit field: Segment distribution
- The following register bits are cleared to 0. They correspond to features enabled for the upcoming reconfiguration boundary, and that are discarded here.
  - The SLIMBUS_FR_CONTROL[1] BUS_RESET bit: Bus reset request control
  - The SLIMBUS_FR_CONTROL[0] BOOT bit: Initiate an active framer (clock source) boot sequence for the component when the component is default active framer.
  - The SLIMBUS_FL_CONTROL[6] BUS_SHUTDOWN
  - SLIMBUS_FL_CONTROL[0] BOOT bit: Boot the component when not in active framer mode.
  - The SLIMBUS_FL_CONTROL[4] KILL_SFS bit is set when the reconfiguration sequence terminates incorrectly (in that case the bit must be set after the clear-up). Forces immediate frame synchronization loss.
  - The SLIMBUS_FL_CONTROL[7] CLEAR_RECONFIGURATION bit itself; that is, the bit never reads out 1.
  - The SLIMBUS_FR_FRAMER_HANDOVER[12] HANDOVER_ENABLE bit: Enable framer handover, upon NEXT_ACTIVE_FRAMER(NCO,NCI) reception.
  - The SLIMBUS_FR_CLOCK_PAUSE[0] CLOCK_PAUSE bit: Controls clock pause/restart
- The following bit fields do not change, although they are updated as part of the reconfiguration message sequence:
  - The SLIMBUS_FR_FRAMER_HANDOVER[11:0] NCO_NCI bit field: The value is don't care as long as SLIMBUS_FR_FRAMER_HANDOVER[12] HANDOVER_ENABLE = 0, and is overwritten if a new handover is scheduled.
  - The SLIMBUS_FR_CLOCK_PAUSE[2:1] TRT bit field: The value is don't care as long as SLIMBUS_FR_CLOCK_PAUSE[0] CLOCK_PAUSE = 0, and isoverwritten if a new pause is scheduled.

23.9.4.5 Data Channels (Ports) Management

Ports (contained in devices) are associated with data channels that connect several ports, typically one output port on a data source device and one or more inputs ports on a data sink device, over periodically scheduled data segments and using a given transfer protocol (TP).

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23.9.4.5.1 Data input/output: manual mode

A data channel agent FIFO stores a whole number of FIFO words. A FIFO word is a chunk of data that contains the AUX and DATA information of one SLIMbus data segment, with the following properties:

- The FIFO word size minimum is 4 bits (one slot) in the current implementation, as defined in the MIPI SLIMbus standard 1.01.00; they are of little practical use.
- The FIFO word size maximum is 32 bits (eight slots) in the current implementation, equal to one physical FIFO RAM word and to one read/write access. Larger segment sizes (up to 31 slots = 124 bits) segments are defined in the MIPI SLIMbus standard version 1.01.00, but they are not implemented here.
- Between the minimum and maximum values, the FIFO word size is programmable, with a slot (that is, 4 bits) granularity.
- The AUX information is a field of 0, 1, or 2 slots (that is, 0, 4, or 8 bits) transmitted immediately before the DATA slots. All sizes are supported by current implementation. It is stored and managed along with the DATA by the module FIFOs.
- The DATA information is a field of 0 to 31 slots in the MIPI SLIMbus standard version 1.01.00, with slot granularity. This is implemented within the limits of the FIFO word size given previously, with AUX size + DATA size = FIFO word size; therefore, the DATA information is a field of 0 to 8 slots.
- The extended asynchronous transfer protocols (TP; that is, simplex and half-duplex) are exceptions to the previously discussed rules. In that case, the source device fills each segment with as many bytes as it deems necessary (provided it fits in the segment), and lets the sink device know how many through the TAG NVB field:
  - The source transmits as many whole FIFO words as it deems necessary. This implies that the FIFO word is a byte multiple (that is, an even number of 4-bit slots).
  - The sink receives a whole number of bytes, which it stores in byte-size FIFO words.
  - AUX is not applicable and is not supported in these modes.

Each read (or write) access to the appropriate SLIMBUS_DCR_DATA_j (respectively, SLIMBUS_DCT_DATA_j) removes (respectively, adds) one FIFO word from RX (TX) FIFO #N. Table 23-657 lists examples of possible FIFO word mappings (with the AUX and DATA slots indicated as A() and D()) inside 32-bit read and write accesses.

NOTE: The transmission over the SLIMbus serial interface is always A(0) to A(N1), and then D(0) to D(N2); that is, MSB to LSB.

Table 23-657. Examples of AUX + DATA Mapping in 32-bit Read/Write Accesses

FIFO Word Format	FIFO Word Size (in Slots)	32-bit Access Read/Write Data (Bit Range)							
		31..28	27..24	23..20	19..16	15..12	11..8	7..4	3..0
4-bit + 0 aux	1 (min)								D(0)
8-bit + 0 aux	2							D(0)	D(1)
12-bit + 0 aux	3						D(0)	D(1)	D(2)
16-bit + 0 aux	4					D(0)	D(1)	D(2)	D(3)
24-bit + 0 aux	6			D(0)	D(1)	D(2)	D(3)	D(4)	D(5)
32-bit + 0 aux	8 (max)	D(0)	D(1)	D(2)	D(3)	D(4)	D(5)	D(6)	D(7)
4-bit + 4 aux	2							A(0)	D(0)
24-bit + 4 aux	7		A(0)	D(0)	D(1)	D(2)	D(3)	D(4)	D(5)
28-bit + 4 aux	8 (max)	A(0)	D(0)	D(1)	D(2)	D(3)	D(4)	D(5)	D(6)
4-bit + 8 aux	3						A(0)	A(1)	D(0)
24-bit + 8 aux	8 (max)	A(0)	A(1)	D(0)	D(1)	D(2)	D(3)	D(4)	D(5)

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23.9.4.5.2 Data Input/Output: DMA Request Mode

The DMA mode reuses all the features of the manual mode defined in Section 23.9.4.5.1, but adds a DMA request generation mechanism to offload the data manipulation task to an external (off-module) DMA controller. As far as the FIFOs themselves are concerned, the accesses are unchanged. for more information about the DMA controller configuration see Chapter 16, *SDMA*.

DMA data channels can be enabled by the SLIMBUS_CMP_DMAENABLE_SET register and disabled by the SLIMBUS_CMP_DMAENABLE_CLR register.

23.9.4.5.3 Data Channel Agent FIFO Control and Status

Each data channel agent is associated with a FIFO, fixed in either TX or RX direction. All TX FIFOs are mapped to a shared buffer space, all RX FIFOs to another shared buffer space. FIFO sizes are software-programmable.

A FIFO must be configured before the data channel is enabled, depending on system-related parameters. For instance, more or less FIFO depth may be required. More FIFO is desirable to prevent underflow/overflow errors in a jittery transmission, but may also carry an unacceptable latency penalty in a voice stream. In any case, FIFO depth is beyond the SLIMbus protocol.

23.9.4.6 FIFO Management

The SLIMbus controller includes two FIFOs, used to buffer transmit/receive data/messages. The SLIMBUS1 FIFO is 32 bytes for TX and 32 bytes for RX. The SLIMBUS2 FIFO is 64 bytes for TX and 64 bytes for RX. FIFO size information is given by the SLIMBUS_CMP_HWINFO[19:12] RRSZ and [11:4] TRSZ bit fields.

FIFOs are connected to SLIMbus-side agents, which transmit and receive data on the serial SLIMbus DATA line. All ports are synchronous to the SLIMbus clock. The numbers of data channel agents are given by SLIMBUS_CMP_HWINFO[27:24] TDC and [23:20] RDC bit fields.

A segment (see Section 23.9.2.3.2) passes through the internal RX and TX FIFOs, where it is stored in FIFO words. The size of the FIFO word, expressed in 4-bit slots, is configurable by software. The FIFO word size is hardware-calculated with the following parameters:

- The SLIMBUS_DCR_CONFIG1_j[9:5]/SLIMBUS_DCT_CONFIG1_j[9:5] SL bit field: Channel segment length, in slots
- The SLIMBUS_DCR_CONFIG1_j[14:10/SLIMBUS_DCT_CONFIG1_j[14:10] DL bit field: Channel data length, integer
- The SLIMBUS_DCR_CONFIG1_j[3:0]/SLIMBUS_DCT_CONFIG1_j[3:0] TP (tag_length) bit field: Length of segment TAG field, function of the channel transfer protocol, in slots.
- The SLIMBUS_DCR_CONFIG1_j[19:16]/SLIMBUS_DCT_CONFIG1_j[19:16] AF (aux_length) bit field: Length of segment AUX field, function of the channel auxiliary format, in slots.

The FIFO word size is computed as follows by the module hardware:

- if DL is equal to 0, FIFO word size = SL tag_length(TP)
- if DL is not equal to 0, FIFO word size = aux_length(AF) + DL

23.9.4.6.1 FIFO Mapping

Each FIFO must be mapped in a free zone of the shared buffer before enabling, as follows:

- The SLIMBUS_DCR_FIFO_SETUP2_j[7:0] SIZE and/or SLIMBUS_DCT_FIFO_SETUP2_j[7:0] SIZE + 1: Capacity of FIFO in FIFO words. (The minimum setting recommended by the SLIMbus protocol is 4-word deep.)
- The SLIMBUS_SMT_FIFO_SETUP[6:5] SIZE_HI/SLIMBUS_SMR_FIFO_SETUP[6:5] SIZE_HI and SLIMBUS_SMT_FIFO_SETUP[4:1] SIZE_LO/SLIMBUS_SMR_FIFO_SETUP[4:1] SIZE_LO bit fields: Capacity of shared TX/RX FIFOs, in bytes, minus 1.
- The SLIMBUS_DCR_FIFO_SETUP1_j[11:5] BASE_ADDR and/or SLIMBUS_DCT_FIFO_SETUP1_j[11:5] BASE_ADDR bit fields: RX and/or TX data channel agent FIFO base address within shared RX/TX RAM

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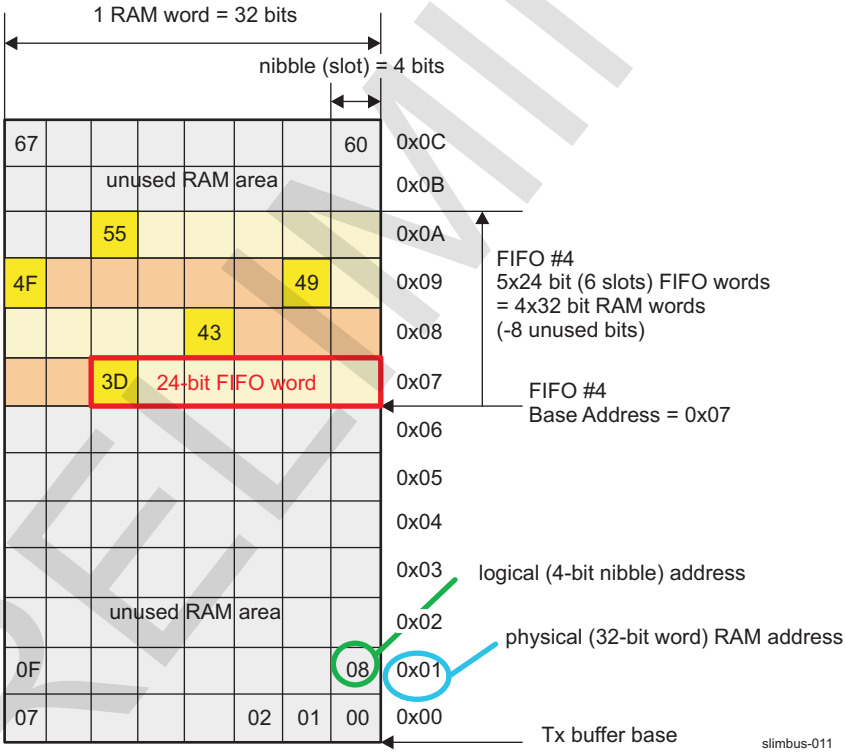
- FIFO base nibble address = FIFO base physical add * 8
- FIFO top nibble address = FIFO base nibble add + (FIFO size * FIFO word size) – 1
- FIFO top physical address = FIFO top nibble add / 8
- The next base physical address available to map another FIFO is the current FIFO top physical address + 1.
- The shared RX and TX buffers are independent; that is, the RX and TX FIFOs are mapped to separate address spaces.

Figure 23-216 is an example mapping, with the following numerical configuration:

- Isochronous (SLIMBUS_DCT_CONFIG1_4[3:0] TP = 0x0) TX FIFO using TX data channel agent 4
- FIFO word size: 6 slots = 24 bits, 20 DATA + 4 AUX (AF = 0xB, DL = 0x5)
- FIFO size: SLIMBUS_DCT_FIFO_SETUP2_4[7:0] SIZE = 4 (4 + 1 = 5 FIFO words stored in FIFO)
- FIFO base physical address: SLIMBUS_DCT_FIFO_SETUP1_4[11:5] BASE_ADDR = 0x7 (= 7)
- FIFO base nibble address = 0x7 * 8 = 0x38 (56)
- FIFO top nibble address = 0x38 + (0x5 * 0x6) -1 = 0x55 (= 85)
- FIFO top physical address = 0x55 / 0x8 = 0xA (= 10, this is a integer division)
- Next base physical address available to map another FIFO: 0xA + 1 = 0xB (= 11)

Figure 23-216. Example of FIFO Mapping in Shared Buffer



23.9.4.6.2 FIFO Status

The following receive-side status is avaible from the register fields:

- The SLIMBUS_DCR_FIFO_STATUS_j[11:2] RD_LEVEL bit field: Number of FIFO words stored in RX FIFO #n. (This field is 1 bit longer than the size and threshold fields, because it ranges from 0 to the FIFO size, whereas the other fields range only from 0 to the FIFO size minus 1.
- The SLIMBUS_DCR_FIFO_STATUS_j[0] EMPTYbit: Active (1) status when RX FIFO #n contains 0 words (rd_level = 0); otherwise, low (0). A read may cause an underflow.
- The SLIMBUS_DCR_FIFO_STATUS_j[1] HILEVEL bit: Active (1) status when FIFO (read) level is

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(strictly) above the high threshold (that is, when there is more than a certain maximum of FIFO words stored in the FIFO). Equivalent to full in case dma_hi_threshold = FIFO size – 1 (the maximum allowed value).

Table 23-658 shows numerical examples for all valid DMA threshold values and all levels in an RX FIFO of FIFO size = 4 FIFO words (SLIMBUS_DCR_FIFO_SETUP2_j[7:0] SIZE = 0x3).

NOTE: The valid threshold range is from 0 to FIFO size – 1: the case threshold = FIFO size is functionally useless and impossible to program for maximum-sized FIFOs (because the rd_level field is 1 bit wider than the threshold fields).

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Table 23-658. HILEVEL/Empty Status of a 4-Word Receive FIFO, for all DMA Threshold Values

rd_level (FIFO Words)	Empty	HILEVEL			
		thr = 0	thr = 1	thr = 2	thr = 3
0 (empty FIFO)	1	0	0	0	0
1	0	1	0	0	0
2	0	1	1	0	0
3	0	1	1	1	0
4 (full FIFO)	0	1	1	1	1

The following transmit-side status is avaible from the following bit fields:

- SLIMBUS_DCT_FIFO_STATUS_j[11:2] WR_LEVEL: Number of free FIFO words in TX FIFO #n. (This field is 1 bit longer than the size and threshold fields, becauses it ranges from 0 to the FIFO size, whereas the other fields range only from 0 to the FIFO size minus 1).
- SLIMBUS_DCT_FIFO_STATUS_j[0] FULL: Active (1) status when TX FIFO #n contains FIFO size words (wr_level = 0); otherwise, low (0). A write may cause an overflow.
- SLIMBUS_DCT_FIFO_STATUS_j[1] LOLEVEL: Active (1) status when FIFO (write) level is under (or equal to) the low threshold; that is, when there is less than a certain minimum of free FIFO words in the FIFO. Equivalent to full in case dma_lo_threshold = 0.

Table 23-659 shows numerical examples for all valid DMA threshold values and all levels in a TX FIFO of FIFO size = 4 FIFO words (SLIMBUS_DCT_FIFO_SETUP2_j[7:0] SIZE = 0x3).

NOTE: The valid threshold range is from 0 to FIFO size – 1: the case threshold = FIFO size is functionally useless and impossible to program for maximum-sized FIFOs (because the wr_level field is 1 bit wider than the threshold fields).

Table 23-659. LOLEVEL/Full Status of a 4-Word Transmit FIFO, for all DMA Threshold Values

wr_level (FIFO Words)	Full	LOLEVEL			
		thr = 3	thr = 2	thr = 1	thr = 0
4 (empty FIFO)	1	1	1	1	0
3	0	1	1	1	0
2	0	0	1	1	0
1	0	0	0	1	0
0 (full FIFO)	0	0	0	0	1

23.9.4.6.3 FIFO Configuration

The bit fields used to configure the FIFOs are:

- SLIMBUS_DCR_FIFO_SETUP1_j[11:5] BASE_ADDR and/or SLIMBUS_DCT_FIFO_SETUP1_j[11:5] BASE_ADDR: RX and/or TX data channel agent FIFO base address within shared RX/TX RAM
- SLIMBUS_DCR_FIFO_SETUP1_j[4:1] DMA_REQ_SIZE and/or SLIMBUS_DCT_FIFO_SETUP1_j[4:1] DMA_REQ_SIZE: DMA request size minus 1, in accesses
- SLIMBUS_DCR_FIFO_SETUP2_j[7:0] SIZE and/or SLIMBUS_DCT_FIFO_SETUP2_j[7:0] SIZE: Capacity of FIFO in FIFO words. (The FIFO can be 1-word deep [the minimum possible value], but it is not recommended. The minimum setting recommended by the SLIMbus protocol is 4-word deep).
- SLIMBUS_DCR_FIFO_SETUP2_j[15:8] SB_TRESHOLD: SLIMbus-side RX data channel agent FIFO threshold, used for SLIMbus reception.
- SLIMBUS_DCT_FIFO_SETUP2_j[15:8] SB_TRESHOLD: SLIMbus-side TX data channel agent FIFO threshold, used for SLIMbus transmission.
- SLIMBUS_DCR_FIFO_SETUP2_j[23:16] DMA_TRESHOLD: Software-side RX data channel agent FIFO low threshold. DMA write requests stop when SLIMBUS_DCR_FIFO_STATUS_j[11:2] RD_LEVEL goes under threshold.

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- SLIMBUS_DCT_FIFO_SETUP2_j[23:16] DMA_TRESHOLD: Software-side TX data channel agent FIFO low threshold. DMA write requests stop when SLIMBUS_DCT_FIFO_STATUS_j[11:2] WR_LEVEL goes under threshold.
- SLIMBUS_DCR_FIFO_SETUP2_j[23:16] DMA_TRESHOLD: Software-side RX data channel agent FIFO high threshold. DMA read requests start when SLIMBUS_DCR_FIFO_STATUS_j[11:2] RD_LEVEL goes above threshold.
- SLIMBUS_DCT_FIFO_SETUP2_j[23:16] DMA_TRESHOLD: Software-side TX data channel agent FIFO high threshold. DMA read requests start when SLIMBUS_DCT_FIFO_STATUS_j[11:2] WR_LEVEL goes above threshold.
- SLIMBUS_DCR_FIFO_STATUS_j[0] EMPTY: Active (1) status when RX FIFO #n contains 0 words (rd_level = 0), else low (0). A read may cause an underflow.
- SLIMBUS_DCT_FIFO_STATUS_j[0] FULL: Active (1) status when TX FIFO #n contains FIFO size words (wr_level = 0), else low (0). A write may cause an overflow.
- SLIMBUS_DCT_FIFO_STATUS_j [1] LOLEVEL: Active (1) status when FIFO (write) level is under (or equal to) the low threshold, that is, when there is less than a certain minimum of free FIFO words in the FIFO. Equivalent to full in case dma_lo_threshold = 0.
- SLIMBUS_DCR_FIFO_STATUS_j[1] HILEVEL: Active (1) status when FIFO (read) level is (strictly) above the high threshold, that is, when there is more than a certain maximum of FIFO words stored in the FIFO. Equivalent to full in case dma_hi_threshold = FIFO size - 1 (the maximum allowed value).
- SLIMBUS_DCR_FIFO_STATUS_j[11:2] RD_LEVEL: Number of FIFO words stored in RX FIFO #n. (This field is 1 bit longer than the size and threshold fields, because it ranges from 0 to the FIFO size, whereas the other fields only range from 0 to the FIFO size minus 1).
- SLIMBUS_DCT_FIFO_STATUS_j[11:2] WR_LEVEL: Number of free FIFO words in TX FIFO #n. (This field is 1 bit longer than the size and threshold fields, because it ranges from 0 to the FIFO size, whereas the other fields only range from 0 to the FIFO size minus 1).

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23.9.4.7 SLIMbus Transfer Protocols

Several registers are used to configure each Transfer Protocol. Table 23-660 shows a description of these registers and fields.

Table 23-660. Register Fields Used to Configure Transfer Protocols

Register	Field	Description
SLIMBUS_DCR_CONFIG1_j / SLIMBUS_DCT_CONFIG1_j[3:0]	TP	Transfer protocol choice
SLIMBUS_DCR_CONFIG1_j [4]	TP_QUALIFIER	Used only for asynchronous TPs (qualifier for plain/extended half-duplex asynchronous TPs)
SLIMBUS_DCT_CONFIG1_j [4]	TP_QUALIFIER	Used only for asynchronous TPs (qualifier for plain/extended half-duplex asynchronous TPs)
SLIMBUS_DCR_CONFIG1_j / SLIMBUS_DCT_CONFIG1_j[9:5]	SL	Total segment length (SL), in 4-bit slots, SL = TAG lenght + AUX lenght + DATA length
SLIMBUS_DCR_CONFIG1_j[26:23]	PR_HI	4-MSB presence rate (PR). Selects the base frequency and the calculation mode of N, with: PR = 2^N x base frequency.
SLIMBUS_DCR_CONFIG1_j[22:20]	PR_LO	3-LSB presence rate (PR). Sets the multiple of the base frequency for the presence frequency.
SLIMBUS_DCR_CONFIG1_j / SLIMBUS_DCT_CONFIG1_j[14:10]	DL	Segment data length, in 4-bits slots. AUX+DATA lenght must fit in a FIFO word.
SLIMBUS_DCR_CONFIG1_j / SLIMBUS_DCT_CONFIG1_j[15]	CL	N/A
SLIMBUS_DCR_CONFIG1_j / SLIMBUS_DCT_CONFIG1_j[31]	ENABLE	Enable/disable data channel
SLIMBUS_DCR_CONFIG2_j / SLIMBUS_DCT_CONFIG2_j[11:0]	SD	Segment periodicity and offset (segment distribution)

23.9.4.7.1 Isochronous Transfer Protocol

Table 23-661 lists the register fields to program isochronous data transfer protocol.

Table 23-661. Register Fields Used for Isochronous Transfer Protocol

Register	Field	Value
SLIMBUS_DCR_CONFIG1_j / SLIMBUS_DCT_CONFIG1_j[3:0]	TP	0x0 (isochronous transfer protocol)
SLIMBUS_DCR_CONFIG1_j / SLIMBUS_DCT_CONFIG1_j[4]	TP_QUALIFIER	Unused in this mode
SLIMBUS_DCR_CONFIG1_j / SLIMBUS_DCT_CONFIG1_j[9:5]	SL	2 to 8, see
SLIMBUS_DCR_CONFIG1_j[26:23]	PR_HI	N/A, only for information
SLIMBUS_DCR_CONFIG1_j[22:20]	PR_LO	N/A
SLIMBUS_DCR_CONFIG1_j / SLIMBUS_DCT_CONFIG1_j[14:10]	DL	2 to 8, see
SLIMBUS_DCR_CONFIG1_j / SLIMBUS_DCT_CONFIG1_j[15]	CL	N/A
SLIMBUS_DCR_CONFIG1_j / SLIMBUS_DCT_CONFIG1_j[31]	ENABLE	1 (enabled)
SLIMBUS_DCR_CONFIG2_j / SLIMBUS_DCT_CONFIG2_j[11:0]	SD	Segment periodicity and offset

23.9.4.7.1.1 Isochronous Segment Composition

Like for all other TPs, the TDM allocation of a pushed data channel is composed of periodic segments of equal length, with the 5-bit segment length (SL) defining the reserved length, in slots (1 to 31), and the segment distribution (SD) defining the segmen offset and periodicity.

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Isochronous has no explicit presence bit because data is always assumed to be present. The SL-slots segment is therefore always composed of the following elements:

- 0, 1, or 2 AUX slots, as defined by the 4-bit auxiliary format (AF) configuration field
- 2 to 8 DATA slots, as defined by the 5-bit data length (DL) configuration field. Full range defined by standard is 1 to 31.
- 0 or more unused slots (should be 0, because this is wasted bandwidth)

NOTE:

- Maximum supported SL and DL are limited by the maximum FIFO word size (the actual implementation of the agent), because each segment (with data present) contains one FIFO word of DATA + AUX. In the current case, FIFO word size is 2 to 8 slots (8 to 32 bits):
  - DL range is 2 to 8 (assuming no AUX slot, or AUX slots stored with the DATA in the FIFO)
  - SL range is 2 to 8 (= DL, since there is no TAG in isochronous protocol).
  - DL = 0 is a special encoding where all slots after the AUX are considered to be DATA slots. In that case, there are by definition no unused slots.
- DL = 0 is a special encoding where all slots after the AUX are considered to be DATA slots. In that case, there are by definition no unused slots.
- Not all combinations of legal field values are legal. The condition is that AUX and DATA slots must fit within the allocated segment, that is, the sum must not be (strictly) greater than SL.
  - DL = 31 cannot be used with 1-slot AUX contents because 1 AUX slot + 31 DATA slots (DL) 31 segment slots (SL max) (assuming no more FIFO word size limit)
  - DL = 30 cannot be used with 2-slot AUX contents (assuming no more FIFO word size limit)
  - ...

23.9.4.7.2 Pushed Transfer Protocol

Table 23-662 lists the register fields to program to have a pushed data transfer protocol.

Table 23-662. Register Fields Used for Pushed Transfer Protocol

Register	Field	Value
SLIMBUS_DCR_CONFIG1_j / SLIMBUS_DCT_CONFIG1_j[3:0]	TP	0x1 (pushed Transfer Protocol)
SLIMBUS_DCR_CONFIG1_j[4]	TP_QUALIFIER	unused in this mode
SLIMBUS_DCT_CONFIG1_j[4]	TP_QUALIFIER	unused in this mode
SLIMBUS_DCR_CONFIG1_j / SLIMBUS_DCT_CONFIG1_j[9:5]	SL	3 to 9, see
SLIMBUS_DCR_CONFIG1_j[26:23]	PR_HI	N/A, only for infromation
SLIMBUS_DCR_CONFIG1_j[22:20]	PR_LO	N/A, only for information
SLIMBUS_DCR_CONFIG1_j / SLIMBUS_DCT_CONFIG1_j[14:10]	DL	2 to 8, see
SLIMBUS_DCR_CONFIG1_j / SLIMBUS_DCT_CONFIG1_j[15]	CL	N/A
SLIMBUS_DCR_CONFIG1_j / SLIMBUS_DCT_CONFIG1_j[31]	ENABLE	1 (enabled)
SLIMBUS_DCR_CONFIG2_j / SLIMBUS_DCT_CONFIG2_j[11:0]	SD	segment periodicity and offset

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23.9.4.7.2.1 Pushed Segment Composition

Like for all other TPs, the TDM allocation of a pushed data channel is composed of periodic segments of equal length, with the 5-bit segment length (SL) defining the reserved length, in slots (1 to 31), and the segment distribution (SD) defining the segment's offset and periodicity.

When data is present (P=1), the SL-slots segment is composed of the following elements:

- 1 TAG slot for STR, P control bits (Sample TRansmit, Presence)
- 0, 1 or 2 AUX slots, as defined by the 4-bit auxiliary format (AF) configuration field
- 2 to 8 DATA slots, as defined by the 5-bit data length (DL) configuration field. Full range defined by standard is 1 to 30
- 0 or more unused slots. (should be 0, as this is wasted bandwidth)

When no data is present (P=0), all slots except the TAG are unused and undriven.

NOTE:

- Maximum supported SL and DL are limited by the maximum FIFO word size (that is, the agent's actual implementation), as each segment (with data present) contains one FIFO word of DATA + AUX. In the current case, FIFO word size is 2 to 8 slots (8 to 32 bits), that is,
  - DL range is 2 to 8 (assuming no AUX slot, or AUX slots stored with the DATA in the FIFO)
  - SL range is 3 to 9 (= DL + 1 TAG)
- DL=0 is a special encoding where all slots after the AUX are considered to be DATA slots. In that case, there are by definition no unused slots.
- Not all combinations of legal field values are legal. The condition is that AUX and DATA slots must fit within the allocated segment, that is, the sum must not be (strictly) greater than SL.
  - DL=31 cannot be used at all for pushed (although it is legal for other TPs) because 1 TAG slot + 31 DATA slots (DL) 31 segment slots (SL max).
  - DL=30 cannot be used with 1-slot AUX contents (assuming no more FIFO word size limit)
  - DL=29 cannot be used with 2-slot AUX contents (assuming no more FIFO word size limit)
  - ...

23.9.4.7.3 Pulled Transfer Protocol

Table 23-663 lists the register fields to program to have a pulled data transfer protocol.

Table 23-663. Register fields used for Pulled Transfer Protocol

Register	Field	Value
SLIMBUS_DCR_CONFIG1_j / SLIMBUS_DCT_CONFIG1_j[3:0]	TP	0x2 (pulled Transfer Protocol)
SLIMBUS_DCR_CONFIG1_j[4]	TP_QUALIFIER	unused in this mode
SLIMBUS_DCT_CONFIG1_j[4]	TP_QUALIFIER	unused in this mode
SLIMBUS_DCR_CONFIG1_j / SLIMBUS_DCT_CONFIG1_j[9:5]	SL	3 to 9, see
SLIMBUS_DCR_CONFIG1_j[26:23]	PR_HI	N/A, only for information
SLIMBUS_DCR_CONFIG1_j[22:20]	PR_LO	N/A, only for information
SLIMBUS_DCR_CONFIG1_j / SLIMBUS_DCT_CONFIG1_j[14:10]	DL	2 to 8, see
SLIMBUS_DCR_CONFIG1_j / SLIMBUS_DCT_CONFIG1_j[15]	CL	N/A

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Table 23-663. Register fields used for Pulled Transfer Protocol (continued)

Register	Field	Value
SLIMBUS_DCR_CONFIG1_j / SLIMBUS_DCT_CONFIG1_j[31]	ENABLE	1 (enabled)
SLIMBUS_DCR_CONFIG2_j / SLIMBUS_DCT_CONFIG2_j[11:0]	SD	segment periodicity and offset

23.9.4.7.3.1 Pulled Segment Composition

Like for all other TPs, the TDM allocation of a pushed data channel is composed of periodic segments of equal length, with the 5-bit segment length (SL) defining the reserved length, in slots (1 to 31), and the segment distribution (SD) defining the segment's offset and periodicity.

When data is present (P=1), the SL-slots segment is composed of the following elements:

- 1 TAG slot for SRQ, P control bits (Sample ReQuest, Presence)
- 0, 1 or 2 AUX slots, as defined by the 4-bit auxiliary format (AF) configuration field
- 2 to 8 DATA slots, as defined by the 5-bit data length (DL) configuration field. Full range defined by standard is 1 to 30.
- 0 or more unused slots. (should be 0, as this is wasted bandwidth)

When no data is present (P=0), all slots except the TAG are unused and undriven.

NOTE:

- Maximum supported SL and DL are limited by the maximum FIFO word size (that is, the agent's actual implementation), as each segment (with data present) contains one FIFO word of DATA + AUX. In the current case, FIFO word size is 2 to 8 slots (8 to 32 bits), that is,
  - DL range is 2 to 8 (assuming no AUX slot, or AUX slots stored with the DATA in the FIFO)
  - SL range is 3 to 9 (= DL + 1 TAG)
- DL=0 is a special encoding where all slots after the AUX are considered to be DATA slots. In that case, there are by definition no unused slots.
- Not all combinations of legal field values are legal. The condition is that AUX and DATA slots must fit within the allocated segment, that is, the sum must not be (strictly) greater than SL.
  - DL=31 cannot be used at all for pushed (although it is legal for other TPs) because 1 TAG slot + 31 DATA slots (DL) 31 segment slots (SL max).
  - DL=30 cannot be used with 1-slot AUX contents (assuming no more FIFO word size limit)
  - DL=29 cannot be used with 2-slot AUX contents (assuming no more FIFO word size limit)
  - ...

23.9.4.7.4 Asynchronous Transfer Protocol

Table 23-666 shows the configuration required for a (plain) asynchronous data channel agent, whether in simplex or in half-duplex mode.

One data channel requires one agent, except for 1/2 duplex where 2 agents are required (one in each direction).

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Table 23-664. "Plain" Asynchronous Endpoint Configurations

Agent Setup	Type	TP	TP_qualifier	SD, SL, DL, ENABLE	Notes
TX simplex	TX	0x4 = "plain" asynchronous, simplex	0b0 = primary owner	independent	always primary owner
TX 1/2 duplex, primary	TX	0x5 = "plain" asynchronous, 1/2 duplex	0b0 = primary owner	same than RX (programming identical in both associated agent)	associated with RX agent
TX 1/2 duplex, secondary	TX	0x5 = "plain" asynchronous, 1/2 duplex	0b1 = secondary owner	same than RX (programming identical in both associated agent)	associated with RX agent
RX simplex	RX	0x4 = "plain" asynchronous, simplex	0b1 = secondary owner	independent	always secondary owner
RX 1/2 duplex, primary	RX	0x5 = "plain" asynchronous, 1/2 duplex	0b0 = primary owner	same than TX (programming identical in both associated agent)	associated with TX agent
RX 1/2 duplex secondary	RX	0x5 = "plain" asynchronous, 1/2 duplex	0b1 = secondary owner	same than TX (programming identical in both associated agent)	associated with TX agent

Table 23-667 lists the register fields to program to have a "plain" asynchronous transfer protocol.

Table 23-665. Register fields used for "Plain" Asynchronous Transfer Protocol

Register (for a given data channel agent)	Field	Value
SLIMBUS_DCR_CONFIG1_j / SLIMBUS_DCT_CONFIG1_j[3:0]	TP	0x4 (simplex) or 0x5 (half duplex)
SLIMBUS_DCR_CONFIG1_j / SLIMBUS_DCT_CONFIG1_j[4]	TP_QUALIFIER	primary or secondary ownership setup
SLIMBUS_DCR_CONFIG1_j / SLIMBUS_DCT_CONFIG1_j[9:5]	SL	3 to 9, see
SLIMBUS_DCR_CONFIG1_j[26:23]	PR_HI	Presence Rate, only for information
SLIMBUS_DCR_CONFIG1_j[22:20]	PR_LO	N/A, only for information
SLIMBUS_DCR_CONFIG1_j / SLIMBUS_DCT_CONFIG1_j[14:10]	DL	2 to 8, see
SLIMBUS_DCR_CONFIG1_j / SLIMBUS_DCT_CONFIG1_j[15]	CL	0 (disabled: makes no sence in asynchronous context)
SLIMBUS_DCR_CONFIG1_j / SLIMBUS_DCT_CONFIG1_j[31]	ENABLE	1 (enabled)
SLIMBUS_DCR_CONFIG2_j / SLIMBUS_DCT_CONFIG2_j[11:0]	SD	segment periodicity and offset

23.9.4.7.4.1 Asynchronous Segment Composition

Like for all other TPs, the TDM allocation of an asynchronous data channel is composed of periodic segments of equal length, with the 5-bit segment length (SL) defining the reserved length, in slots (2 to 31), and the segment distribution (SD) defining the segment's offset and periodicity.

When data is present (P=1), the SL-slots segment is composed of the following elements:

- 1 TAG slot for T1, T2, CTS, P control bits
- 0, 1 or 2 AUX slots, as defined by the 4-bit auxiliary format (AF) configuration field
- 2 to 8 DATA slots, as defined by the 5-bit data length (DL) configuration field. Full range defined by standard is 1 to 30.
- 0 or more unused slots. (should be 0, as this is wasted bandwidth)

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When no data is present (P=0), only the TAG slot is (partially) driven, depending on the ownership control and data flow control protocol phases. All other slots are unused and undriven.

NOTE:

- Maximum supported SL and DL are limited by the maximum FIFO word size (that is, the agent's actual implementation), as each segment (with data present) contains one FIFO word of DATA + AUX. In the current case, FIFO word size is 2 to 8 slots (8 to 32 bits), that is,
  - DL range is 2 to 8 (assuming no AUX slot, or AUX slots stored with the DATA in the FIFO)
  - SL range is 3 to 9 (= DL + 1 TAG)
- DL=0 is a special encoding where all slots after the AUX are considered to be DATA slots. In that case, there are by definition no unused slots. When used, the actual length of the segment data (in slots) is determined by hardware, by subtracting the TAG and AUX slots from the total segment length (SL). This case is strictly equivalent to the "direct" encoding, that is, where DL is a non-zero figure.
- Not all combinations of legal field values are legal, even in an ideal implementation. The condition is that TAG, AUX and DATA slots must fit within the allocated segment, that is, the sum must not be (strictly) greater than SL.
  - DL=31 cannot be used at all for asynchronous (although it is legal for other TPs) because 1 TAG slot + 31 DATA slots (DL) 31 segment slots (SL max).
  - DL=30 cannot be used with 1-slot AUX contents (assuming no more FIFO word size limit)
  - DL=29 cannot be used with 2-slot AUX contents (assuming no more FIFO word size limit)
  - SL = 1 is forbidden, since the smallest asynchronous segment is 1 TAG slots + 1 DATA slot = 2 slots long.
  - ...

23.9.4.7.4.2 Programming Specificities for Half-Duplex Protocol

Contrary to all other standard transfer protocols (TP), the half-duplex asynchronous ones (plain or extended) are bidirectional, that is, DATA slots can go in both directions. This means that 1 half-duplex asynchronous port (mapped on 1 half-duplex asynchronous data channel) uses 2 unidirectional data channel agents (FIFOs and logic) in the same controller.

The two agents are of opposite directions (1 TX + 1 RX), and the configuration register fields must always be programmed simultaneously and with matching values for both, so that both own the exact same slots (the data channel's allocated distribution).

23.9.4.7.5 Extended Asynchronous Transfer Protocol

Table 23-666 shows the configuration required for an extended asynchronous data channel agent, whether in simplex or in half-duplex mode.

One data channel requires one agent, except for 1/2 duplex where 2 agents are required (one in each direction).

Table 23-666. Extended Asynchronous Endpoint Configurations

Agent Setup	Type	TP	TP_qualifier	SD, SL, DL, ENABLE	Notes
TX simplex	TX	0x6 = extended asynchronous, simplex	0b0 = primary owner	independent	always primary owner

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Table 23-666. Extended Asynchronous Endpoint Configurations (continued)

Agent Setup	Type	TP	TP_qualifier	SD, SL, DL, ENABLE	Notes
TX 1/2 duplex, primary	TX	0x7 = extended asynchronous, 1/2 duplex	0b0 = primary owner	same than RX (programming identical in both associated agent)	associated with RX agent
TX 1/2 duplex, secondary	TX	0x7 = extended asynchronous, 1/2 duplex	0b1 = secondary owner	same than RX (programming identical in both associated agent)	associated with RX agent
RX simplex	RX	0x6 = extended asynchronous, simplex	0b1 = secondary owner	independent	always secondary owner
RX 1/2 duplex, primary	RX	0x7 = extended asynchronous, 1/2 duplex	0b0 = primary owner	same than TX (programming identical in both associated agent)	associated with TX agent
RX 1/2 duplex secondary	RX	0x7 = extended asynchronous, 1/2 duplex	0b1 = secondary owner	same than TX (programming identical in both associated agent)	associated with TX agent

The data length within the segment is now determined in the TAG NVB field, so that the SLIMbus data length (DL) parameter is not needed in the SLIMbus definition. The corresponding configuration register field SLIMBUS_DCR_CONFIG1_j / SLIMBUS_DCT_CONFIG1_j[14:10] DL is still needed to set the FIFO word size: it must always be programmed to 0x2 (slots) = 1 byte, in both the data sinks and sources, which corresponds to the NVB granularity unit.

Table 23-667 lists the register fields to program to have a "plain" asynchronous transfer protocol.

Table 23-667. Register fields used for Extended Asynchronous Transfer Protocol

Register (for a given data channel agent)	Field	Value
SLIMBUS_DCR_CONFIG1_j / SLIMBUS_DCT_CONFIG1_j[3:0]	TP	0x6 (simplex) or 0x7 (half duplex)
SLIMBUS_DCR_CONFIG1_j / SLIMBUS_DCT_CONFIG1_j[4]	TP_QUALIFIER	primary or secondary ownership setup
SLIMBUS_DCR_CONFIG1_j / SLIMBUS_DCT_CONFIG1_j[9:5]	SL	4 to 31, see
SLIMBUS_DCR_CONFIG1_j[26:23]	PR_HI	Presence Rate, only for information
SLIMBUS_DCR_CONFIG1_j[22:20]	PR_LO	N/A, only for information
SLIMBUS_DCR_CONFIG1_j / SLIMBUS_DCT_CONFIG1_j[14:10]	DL	2: NVB data granularity (not the Slimbus "data length")
SLIMBUS_DCR_CONFIG1_j / SLIMBUS_DCT_CONFIG1_j[15]	CL	0 (disabled: makes no sence in asynchronous context)
SLIMBUS_DCR_CONFIG1_j / SLIMBUS_DCT_CONFIG1_j[31]	ENABLE	1 (enabled)
SLIMBUS_DCR_CONFIG2_j / SLIMBUS_DCT_CONFIG2_j[11:0]	SD	segment periodicity and offset

23.9.4.7.5.1 Extended Asynchronous Segment Composition

Like for all other TPs, the TDM allocation of an extended asynchronous data channel is composed of periodic segments of equal length, with the 5-bit segment length (SL) defining the reserved length, in slots (1 to 31), and the segment distribution (SD) defining the segment's offset and periodicity.

When data is present (P=1), the segment is composed of the following elements:

- 2 TAG slots for T1, T2, CTS, P control bits + 4-bit NVB field

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- no (0) AUX slots. The current implementation does not support auxiliary fields in the extended asynchronous TP, that is, the only legal value in the 4-bit auxiliary format (AF) is 0b0000. Other values are theoretically allowed by the SLIMbus standard, but for this TP they have little functional use.
- 0 to 28 DATA slots, as defined by the 4-bit number of valid bytes (NVB) field
- 0 or more unused slots. (this is wasted bandwidth, but as NVB can change for each segment this is normal)

When no data is present (P=0):

- 1st TAG slot is (partially) driven, depending on the ownership / data flow control protocol phases.
- 2nd TAG slot is either driven to all-zero, or undriven, that is, it always reads out as all-zero.
- All other slots are unused and undriven

NOTE:

- SL should be configured so that the maximum number of DATA slots is even, otherwise there will always be at least one unused slot.
- Largest supported SL is not limited by the maximum FIFO word size (that is, the agent's actual implementation), unlike all other transfer protocols, as several FIFO words can be concatenated inside the same data segment.
- Not all combinations of legal field values are legal. The condition is that TAG, AUX and DATA slots must fit within the allocated segment, that is, the sum must not be (strictly) greater than SL.
  - NVB = 15 (15 valid data bytes = 30 slots) cannot be used, because 2 TAG slots + 30 DATA slots (NVB x 2) = 32 31 segment slots (SL max).
  - SL = 1,2,3 are forbidden, since the smallest extended asynchronous segment is 2 TAG slots + 1 DATA byte (NVB = 1) = 4 slots long.
  - ...

23.9.4.7.5.2 Programming Specificities for Half-Duplex Protocol

Contrary to all other standard transfer protocols (TP), the half-duplex asynchronous ones (plain or extended) are bidirectional, that is, DATA slots can go in both directions. This means that 1 half-duplex asynchronous port (mapped on 1 half-duplex asynchronous data channel) uses 2 unidirectional data channel agents (FIFOs and logic) in the same controller.

The two agents are of opposite directions (1 TX + 1 RX), and the configuration register fields must always be programmed simultaneously and with matching values for both, so that both own the exact same slots (the data channel's allocated distribution).

23.9.4.8 Paired-up channels

Two (or more) data channels with common properties can be paired up to operate in lockstep, for example, the left and right channels of a stereo audio flow: paired up data samples are generated together by a data source and need to arrive together at the data sink after going over the SLIMbus interface.

Assuming that pairing up has been implemented in both the sink and the source SLIMbus controllers of the data channel, it is enabled by configuring the channel as follows:

- Same segment windows: same channel rate, also expressed as segment interval (expressed in slots). This is encoded in the channel's Segment Distribution (SLIMBUS_DCT_CONFIG2_j / SLIMBUS_DCR_CONFIG2_j[11:0] SD).
- Same Segment Length (SLIMBUS_DCT_CONFIG1_j / SLIMBUS_DCR_CONFIG1_j[9:5] SL)
- Segment offset (also encoded in SD) is necessarily different, otherwise the two channels would be scheduled in the same slots. SD is therefore different.
- Sequential Channel Numbers (CN) are assigned to the channels to be paired up
- Data channel numbering and scheduling are defined by the active manager device, through the broadcasts of the NEXT_DEFINE_CHANNEL() message.

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Contents must be aligned, as follows:

- Same Transfer Protocol (SLIMBUS_DCT_CONFIG1_j / SLIMBUS_DCR_CONFIG1_j[3:0] TP). Asynchronous protocols (extended or not) do not support pairing.
- Same Aux Format (SLIMBUS_DCT_CONFIG1_j / SLIMBUS_DCR_CONFIG1_j[19:16] AF)
- Same Data Length (SLIMBUS_DCT_CONFIG1_j / SLIMBUS_DCR_CONFIG1_j[14:10] DL)
- Pairing can be enabled through the Channel Link (SLIMBUS_DCT_CONFIG1_j / SLIMBUS_DCR_CONFIG1_j[15] CL) data channel content bit. Pairing between channel #N-1 and channel #N is enabled by setting the Channel Link (CL) content bit to 1 on channel #N. For example, to pair up channels #1 and #2, CL = 1 in channel #2 (thus linking it to #1) and CL = 0 in channel #1(thus keeping it separate from channel #0).
- Data channel contents are defined by active manager device, through the broadcasting of the NEXT_DEFINE_CONTENT() and CHANGE_CONTENT() messages.

23.9.4.8.1 Paired-up behaviour for Isochronous TP

Data is by definition present in all segments, so that isochronous data channels with the same channel rate (as extracted from SD) are naturally paired up in normal operation. However, pairing also ensures that transmit underflows are also coupled:

- On the source side, if one of the channels has no data to transmit (TX underflow error, reported by IRQ) the other channels won't transmit any data either (even if they have some). This prevents the transmitter from getting out of sync.
- On the sink side, the underflow error will not be detected since no presence indication is transmitted, but the channels will remain in sync when the correct data flow resumes.

23.9.4.8.2 Paired-up behaviour for Pushed TP

Data presence in each segment is flagged by the STR/P bits (strobe/presence) driven by the data source in the TAG slot. On the source side, paired up channels must have the same P value in a given segment window, that is, data must only be transmitted (STR=P=1) when both channels have data to send. No requirements on the sink side.

23.9.4.8.3 Paired-up behaviour for Pulled TP

Data presence in a segment is requested by the SRQ TAG bit (sample request), driven by the sink, and confirmed by the P TAG bit (presence), driven by the source, so that SRQ and P are always equal in normal operation. The main pairing up requirement is therefore that the SRQ are aligned for all channel sinks, that is, that data is requested on all channels only if all sinks are ready to receive it, otherwise it is requested on none.

Pairing also ensures that transmit underflows are also coupled between channels: if for some reason a source cannot fullfill a request to drive data (SRQ=1, P=0: transmit underflow error, reported by IRQ), none of the other channels must drive data either, and all must flag P=0. The source side can only implement correct pairing if the sink side is correct in the first place; indeed, unless an underflow occurs, it is sufficient that the sink side implements pairing for the channels to be paired.

23.9.4.9 Device and Adressing Management

One of the manager device tasks is to keep track of devices present on the bus and to enumerate them, that is, assign a (different) Logical Address (LA) to each.

The manager device itself is implicitly enumerated by default, to Logical Address (LA) 0xFF. This is the only case where a device enumerates without ASSIGN_LOGICAL_ADDRESS message transmitted over the bus. Therefore ror the manager device the following default configuration must be applied :

- SLIMBUS_DEV_LA_i[7:0] LA = 0xFF
- SLIMBUS_DEV_LA_i[8] LA_ENABLE = 1
- SLIMBUS_DEV_LA_i[9] EA_ENABLE = 1 (although manager is never addressed by Enumeration Address, EA)

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The SLIMbus controller implements several devices, each of which is identified by its address. Addresses are used to exchange control messages over the shared message channel (SMC). The controller will recognize, store and respond (that is, acknowledge) to any message on the SMC targeted at one of the component's devices in the RX message FIFO.

The Enumeration Addresses (EA) composition is described in Table 23-668, with:

- MI, PC and IV are Software-programmable and have the same value for all devices of the component with SLIMBUS_CMP_MI_PC[15:0] MI, SLIMBUS_CMP_MI_PC[31:16] PC and SLIMBUS_CMP_IV[7:0] IV.
- DI is hardwired and unique for each device within the component. It is given by SLIMBUS_DCT_MAP_j / SLIMBUS_DCR_MAP_j[7:0] DI bit field.
- Each device individual EA is Software-accessible, for reference, in read-only registers (SLIMBUS_DEV_EA_LO_i and SLIMBUS_DEV_EA_HI_i registers)

Table 23-668. Enumeration Address (EA) makeup

EA Subfield	Size (bits)	Top Bit	Bottom Bit	Source
MI: Manufacturer ID	16	47	32	SLIMBUS_CMP_MI_PC[15:0] MI
PC: Product Code	16	31	16	SLIMBUS_CMP_MI_PC[31:16] PC
DI: Device Index	8	15	8	hardwired
IV: Instance Value	8	7	0	SLIMBUS_CMP_IV[7:0] IV
Total: EA	48	47	0	SLIMBUS_DEV_EA_HI_i / SLIMBUS_DEV_EA_LO_i

The Logical Address (LA) assigned by the manager range from 0x00 to 0xEF, with the exception of the active manager located by definition at LA = 0xFF. It is configured through SLIMBUS_DEV_LA_i[7:0] LA for device m.

By default, a device uses a unique, static 48-bit Enumeration Address (EA). The EA is used only for enumeration, that is, the acquisition a dynamic Logical Address (LA) assigned by the active manager device.

NOTE: The port number is given by SLIMBUS_DCT_MAP_j / SLIMBUS_DCR_MAP_j[13:8] PN bit field.

23.9.4.10 Message Management

23.9.4.10.1 Transmission

23.9.4.10.1.1 TX Message Sequence

The message transmission software sequence is the following:

- Initial state:
  - SLIMBUS_SMT_CONTROL[0] MESSAGE_ENABLE = 0: No ongoing TX message. This also implies that TX message FIFO can receive another message.
  - SLIMBUS_SMT_INFO[5:0] = 0 : TX message event flags must be cleared (to 0) by Software by writing 1 to the corresponding bit(s). Failing to meet this condition will not prevent the message transmission, but will prevent a proper readout of the message transmission's outcome
  - Optional: If the IRQ method is to be used (instead of polling), it must be cleared and enabled, that is, SLIMBUS_CMP_IRQENABLE_SET[2] SMT_INFO_EN = 1 and SLIMBUS_CMP_IRQSTATUS[2] SMT_INFO = 0. For more information about interrupts see Section 23.9.4.11.
- FIFO loading:
  - The message is written byte by byte to register SLIMBUS_SMT_MESSAGE[7:0]. SLIMbus endianness is retained (big-endian) that is, serial message starts with the MSB (bit 7) of the first byte written into the FIFO and ends with the LSB (bit 0) of the last written byte.

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- The minimum message size is 6 bytes (5 entered to the FIFO), for a short-arbitration (that is, logical source address LA = 1 byte), broadcast (that is, no destination address), no-payload message.
- The maximum theoretical message size is 39 bytes (38 entered to the FIFO), for a long-arbitration (that is, enumeration source address EA = 6 bytes), maximum remaining length (RL = 5b11111 = 31 bytes) message. The TX message FIFO can hold 32 bytes, that is, most messages (of 33 bytes or less).
- An overflow event is flagged (SLIMBUS_SMT_INFO[1] OVERFLOW is set) if too many bytes are written in. The TX message FIFO is then cleared before another TX message sequence attempt is made.

- Transmission enabling:
  - Once the message has been loaded into the TX message FIFO, software must write 1 on field SLIMBUS_SMT_CONTROL[0] MESSAGE_ENABLE.
- Transmission:
  - From that point on, the device will attempt to transmit the message stored in the FIFO. Actual transmission may be delayed because of Message Sync acquisition time (if not already operational), Ongoing message on the SMC, and Arbitration(s) lost to higher-priority messages.
- Transmission completion and reporting:
  - Transmission is considered complete if one of the following -mutually exclusive- conditions is met, and the corresponding bit of SLIMBUS_SMT_INFO is set : Negative response SLIMBUS_SMT_INFO[3] NACK = 1, or Positive response : SLIMBUS_SMT_INFO[2] PACK = 1, or No response: SLIMBUS_SMT_INFO[4] NORE = 1, or Illegal response: SLIMBUS_SMT_INFO[5] UDEF = 1, or Transmit collision: SLIMBUS_SMT_INFO[0] MC_TX_COL = 1.
  - If enabled (SLIMBUS_CMP_IRQENABLE_SET[2] SMT_INFO_EN = 1), an interrupt request flag is set (SLIMBUS_CMP_IRQSTATUS[2] SMT_INFO = 1) and the IRQ line asserted.
  - Additionally, bit SLIMBUS_SMT_CONTROL[0] MESSAGE_ENABLE must auto-clear. Polling this bit will also work as an alternative to waiting for the IRQ.
  - Following the transmission, all message bytes have been removed from the TX message FIFO.

23.9.4.10.1.2 TX Message FIFO Clearing

The TX message FIFO must not be cleared as part of the normal message transmission operation, between messages. However, the clearing becomes necessary in case of error:

- FIFO overflow: the bit SLIMBUS_SMT_INFO[1] OVERFLOW is set
- FIFO underflow: the bit SLIMBUS_SMR_INFO[1] UNDERFLOW is set
- TX collision: the bit SLIMBUS_SMT_INFO[0] MC_TX_COL or the bit SLIMBUS_SMR_INFO[0] MC_TX_COL is set
- Undefined error condition, unknown FIFO content

Clearing is done by writing 0 to bit field SLIMBUS_SMT_CONTROL[0] MESSAGE_ENABLE.

23.9.4.10.2 Message reception

23.9.4.10.2.1 Message Responding

The message responding and message receiving are separate but intertwined processes. Message responding starts as soon as a message is received, and consists in sending back information, including PACK or NACK.

23.9.4.10.2.2 RX Message Sequence

The message reception software sequence is the following:

- Initial state
  - SLIMBUS_SMR_INFO = 0x0: Pending (at 1) RX message event flags must be cleared (to 0) by Software by writing 1 to the corresponding bit(s).
  - Optional: If the IRQ method is to be used (instead of polling), it must be cleared and enabled, that

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is, SLIMBUS_CMP_IRQENABLE_SET[3] SMR_INFO_EN = 1 and SLIMBUS_CMP_IRQSTATUS[3] SMR_INFO = 0. For more information about interrupts see Section 23.9.4.11

- Message reception
  - Message reception requires no intervention: Messages with target addresses enabled in SLIMBUS_DEV_LA_i registers are automatically loaded into the RX message FIFO.
- FIFO unloading
  - The message is read byte by byte off the FIFO and put into register SLIMBUS_SMR_MESSAGE[7:0]. SLIMbus endianness is used (big-endian) that is, serial message starts with the MSB (bit 7) of the first byte written into the FIFO and ends with the LSB (bit 0) of the last written byte.
  - The minimum message size is 6 bytes, for a short-arbitration (that is, logical source address LA = 1 byte), broadcast (that is, no destination address), no-payload message.
  - The maximum theoretical message size is 39 bytes, for a long-arbitration (that is, enumeration source address EA = 6 bytes), maximum remaining length (RL = 5b11111 = 31 bytes) message. The RX message FIFO can hold 32 bytes, that is, most message types.
  - An overflow event is flagged (SLIMBUS_SMR_INFO[1] OVERFLOW bit is set) if too many bytes are received, which will overwrite previous bytes.
  - An underflow event is flagged (SLIMBUS_SMR_INFO[1] UNDERFLOW bit is set) if too many bytes are read out. The RX message FIFO is cleared before another RX message sequence attempt is made.
- Message decoding and servicing
  - This phase takes place in parallel with the unloading phase above. In some cases, a partial decoding can lead the software to skip the end of the unloading and flush the FIFO. The software will check Device Association (thanks to the SLIMBUS_SMR_INFO[2] RECEIVED_MESSAGE bit) and Message Support.

23.9.4.10.2.3 RX Message FIFO Clearing

- While the software is reading the message off the FIFO, the receive message agent unconditionally answers NACK, forcing remote side to retransmit any new incoming message.
- Only once the message has been read out of the FIFO, the software writes 1 on SLIMBUS_SMR_INFO[2] RECEIVED_MESSAGE bit. This will automatically clear the FIFO.

The RX message FIFO is cleared as part of the normal message reception operation, between messages, although it is not strictly necessary. However, the clearing becomes compulsory in case of error:

- FIFO overflow: the bit SLIMBUS_SMT_INFO[1] OVERFLOW is set
- FIFO underflow: the bit SLIMBUS_SMR_INFO[1] UNDERFLOW is set
- Undefined error condition, unknown FIFO content

Clearing is done by writing 1 to register bit field SLIMBUS_SMR_INFO[2] RECEIVED_MESSAGE bit.

23.9.4.11 Interrupt Service Routines

This section lists specific software programming sequences, to be applied at specific phases of the SLIMbus protocol. This section covers the low-level software service of IRQs. More information about interrupts in the device can be found in Chapter 17, *Interrupt Controllers*.

The SLIMbus controller has a single IRQ output line, controlled through 9-bit registers SLIMBUS_CMP_IRQSTATUS, SLIMBUS_CMP_IRQENABLE_SET and SLIMBUS_CMP_IRQENABLE_CLR. Each bit of this 1st level IRQ management points to a 2nd level information register. There are thus 9 such information registers, each connected with a specific submodule (framer device, interface device, message receiver, message transmitter, and one per generic data device).

2nd level information register and status register are written independently each other. When an event occurs, both bits are set to 1, and when the software writes 1 on either register the corresponding bit is cleared to 0. IRQ line is the status register output.

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- When an event takes place, the corresponding 2nd level information bit must be set to 1 (if already 1: no change)
- When an event takes place, the corresponding 1st level IRQ status bit must be set to 1 (if enabled and if not already 1) and trigger an interrupt (if not already active). Note that this does not depend on the information bit's value: if the information bit is already high, the event must still potentially set the IRQ status bit.
- Writing 1 to a set IRQ status bit clears the bit and deasserts the IRQ line (if another status bit is set, the IRQ line will reassert immediately). Note that the clearing of the IRQ status does not depend on the information bit, that is, it will work even if the information bit has not been cleared.
- Writing 1 to a set information bit will clear the bit, but have no impact on the IRQ status

CAUTION

The software sequence should always be as follows:

1. Clear the status bit
2. Read the relative information register
3. When needed and allowed, clear the information register

23.9.4.11.1 Interrupt Requests

Table 23-669 lists the event flags, and their mask, that can cause module interrupts.

Table 23-669. Interrupts

Interrupt Line	Event Flag	Event Mask
SLIMBUS1_IRQ / SLIMBUS2_IRQ	SLIMBUS_CMP_IRQSTATUS_RAW[11:0] and SLIMBUS_CMP_IRQSTATUS[11:0]	SLIMBUS_CMP_IRQENABLE_SET[11:0] and SLIMBUS_CMP_IRQENABLE_CLR[11:0]

23.9.4.11.2 Possible Interrupts

Table 23-670 lists all the interrupts that can occur and the related registers.

Table 23-670. Event Summary

Register	Field Name	Wake-Up Source	IE	Description
Frame layer events				
SLIMBUS_FL_INFO[6]	RECONFIGURED	Yes	No	Reconfiguration boundary crossed
SLIMBUS_FL_INFO[5]	SAW_BUS_RESET	Yes	No	Bus reset sequence detected on the bus
SLIMBUS_FL_INFO[3]	FOUND_MS	Yes	No	Message synchronization acquired
SLIMBUS_FL_INFO[2]	LOST_MS	Yes	Yes	Message synchronization lost
SLIMBUS_FL_INFO[1]	LOST_SFS	Yes	Yes	Superframe synchronization lost
SLIMBUS_FL_INFO[0]	LOST_FS	Yes	Yes	Frame synchronization lost
Framer device events				
SLIMBUS_FR_INFO[5]	CLOCK_RESTART	Yes	No	Clock restart request event detected
SLIMBUS_FR_INFO[4]	FRAMER_UNACTIVATED	Yes	Yes	Framer has left clock source operational state.
SLIMBUS_FR_INFO[3]	FRAMER_ACTIVATED	Yes	Yes	Framer has reached clock source operational state.
SLIMBUS_FR_INFO[2]	GC_TX_COL	Yes	Yes	Collision during guide byte transmit
SLIMBUS_FR_INFO[1]	FI_TX_COL	Yes	Yes	Collision during framing information transmit

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Table 23-670. Event Summary (continued)

Register	Field Name	Wake-Up Source	IE	Description
SLIMBUS_FR_INFO[0]	FS_TX_COL	Yes	Yes	Collision during frame synchronization symbol transmit
Shared message transmit channel events				
SLIMBUS_SMT_INFO[7]	ABORT	Yes	No	TX message was aborted before completion because of message synchronization loss.
SLIMBUS_SMT_INFO[5]	UDEF	Yes	No	TX message has UDEF response: Undefined response, protocol error.
SLIMBUS_SMT_INFO[4]	NORE	Yes	No	TX message has NORE response: No or all-zero message response.
SLIMBUS_SMT_INFO[3]	NACK	Yes	No	TX message has NACK response: At least one of the recipient components requested message retransmission.
SLIMBUS_SMT_INFO[2]	PACK	Yes	No	TX message has PACK response: All recipient devices accepted the message.
SLIMBUS_SMT_INFO[1]	OVERFLOW	No	No	Overflow in TX message FIFO
SLIMBUS_SMT_INFO[0]	MC_TX_COL	Yes	Yes	Transmit collision in message channel during message transmission
Shared message receive channel events				
SLIMBUS_SMR_INFO[4]	OVERFLOW	Yes	No	Overflow in RX message FIFO. Message is larger than the FIFO.
SLIMBUS_SMR_INFO[3]	RECEIVED_RECONFIGURE	Yes	No	RECONFIGURE_NOW() message received
SLIMBUS_SMR_INFO[2]	RECEIVED_MESSAGE	Yes	No	Message is available in the RX message FIFO.
SLIMBUS_SMR_INFO[1]	UNDERFLOW	No	No	Underflow in RX message FIFO. Software tried to read more bytes than available.
SLIMBUS_SMR_INFO[0]	MC_TX_COL	Yes	Yes	Transmit collision in message channel during message reception
Data channel events				
SLIMBUS_DCT_INFO_j[3]	LOLEVEL	Yes	No	Write level of TX data agent FIFO has gone above the threshold.
SLIMBUS_DCR_INFO_j[3]	HILEVEL	Yes	No	Read level of RX data agent FIFO has gone above the threshold.
SLIMBUS_DCT_INFO_j[2], SLIMBUS_DCR_INFO_j[2]	UNDERFLOW	Yes	No	Underflow in TX/RX data agent FIFO
SLIMBUS_DCT_INFO_j[1], SLIMBUS_DCR_INFO_j[1]	OVERFLOW	Yes	No	Overflow in TX/RX data agent FIFO
SLIMBUS_DCT_INFO_j[0], SLIMBUS_DCR_INFO_j[0]	DATA_TX_COL	Yes	Yes	TX collision in TX/RX data agent

23.9.4.11.3 Interface Device ISRs

The Interface Device ISRs are applied when a bit of status register SLIMBUS_FL_INFO is set, which also triggers the assertion of bit field SLIMBUS_CMP_IRQSTATUS[0] FL_INFO and of the IRQ line, when enabled in bit field SLIMBUS_CMP_IRQENABLE_SET[0] FL_INFO_EN. Service routines must be applied and the FL_INFO bit field cleared (by writing 1 to it).

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23.9.4.11.3.1 Lost Frame Synchronization (LOST_FS)

23.9.4.11.3.1.1 Root Event

This interrupt occurs when a loss of frame synchronization happens. All data channels automatically stop, that is, all active SLIMBUS_DCT_CONFIG1_j / SLIMBUS_DCR_CONFIG1_j[31] ENABLE bits are cleared. Component automatically reacquires frame, superframe and message synchronization.

23.9.4.11.3.1.2 Interrupt Service Routine

Frame synchronization (FS) loss implies the loss of higher-level superframe and message synchronizations:

- Messages cannot be expected to be transmitted / received until the component is operational again. Additionally, any ongoing reconfiguration sequence must be interrupted and made invalid by MS loss. No action required if no reconfiguration sequence is ongoing.
- Implicit superframe synchronization loss triggers a reset of all component ports: see Section 23.9.4.4.3.6.

This field, SLIMBUS_FL_INFO[0] LOST_FS, is not cleared by software into the ISR. Instead, it stays set until the component receives a REQUEST_CLEAR_INFORMATION message by the remote manager (Receiving a message implies of course that message synchronization has been restored in the mean time). Only at this point, software can apply the message and clear the designated field.

23.9.4.11.3.2 Lost Superframe Synchronization (LOST_SFS)

23.9.4.11.3.2.1 Root Event

This interrupt occurs when a loss of superframe synchronization happens. The loss of lower-level frame synchronization also implies the loss of superframe synchronization, if already acquired, but does not trigger the assertion of LOST_SFS Information Element. All data channels automatically stop, that is, all active SLIMBUS_DCT_CONFIG1_j / SLIMBUS_DCR_CONFIG1_j[31] ENABLE bits must be cleared. Component automatically reacquires superframe and message synchronization.

23.9.4.11.3.2.2 Interrupt Service Routine

Superframe synchronization (SFS) loss will trigger the reset of all ports of the component: see Section 23.9.4.4.3.6.

Superframe synchronization loss implies the loss of message synchronization, that is, messages cannot be expected to be transmitted / received until the component is operational again. Additionally, any ongoing reconfiguration sequence must be interrupted and made invalid by MS loss. No action required if no reconfiguration sequence is ongoing.

This field, SLIMBUS_FL_INFO[1] LOST_SFS, is not cleared by software into the ISR. Instead, it stays set until the component receives a REQUEST_CLEAR_INFORMATION message by the remote manager (Receiving a message implies of course that message synchronization has been restored in the mean time). Only at this point, software can apply the message and clear the designated field.

23.9.4.11.3.3 Lost Message Synchronization (LOST_MS)

23.9.4.11.3.3.1 Root Event

This interrupt occurs when a loss of message synchronization happens. The loss of either lower-level frame or superframe synchronization also implies the loss of message synchronization, if already acquired, but does not trigger the assertion of LOST_MS Information Element. Component automatically reacquires message synchronization, by seeking for Guide Channel information.

23.9.4.11.3.3.2 Interrupt Service Routine

Any ongoing reconfiguration sequence must be interrupted and made invalid by the Message Synchronisation (MS) loss. No action required here if no reconfiguration sequence is ongoing.

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This field, SLIMBUS_FL_INFO[2] LOST_MS, is not cleared by software into the ISR. Instead, it stays set until the component receives a REQUEST_CLEAR_INFORMATION message by the remote manager, requiring to clear it (Receiving a message implies of course that message synchronization has been restored in the mean time). Only at this point, software can apply the message and clear the designated field.

23.9.4.11.3.4 Found Message Synchronization (FOUND_MS)

23.9.4.11.3.4.1 Root Event

This interrupt occurs when acquisition of message synchronization. In that state, messages may be transmitted and received over the SMC.

23.9.4.11.3.4.2 Interrupt Service Routine

If MS is reacquired, following a previous LOST_MS event, then a REPORT_INFORMATION message must be transmitted, as follows:

- Source: interface device
- Destination: SLIMbus manager device (LA = 0xFF)
- Information Element: LOST_MS

If MS is reacquired, following a previous LOST_FS event, then a REPORT_INFORMATION message must be transmitted, as follows:

- Source: interface device
- Destination: SLIMbus manager device (LA = 0xFF)
- Information Element: LOST_FS

If MS is reacquired, following a previous LOST_SFS event, then a REPORT_INFORMATION message must be transmitted, as follows:

- Source: interface device
- Destination: SLIMbus manager device (LA = 0xFF)
- Information Element: LOST_SFS

If MS is reacquired, following a previous MC_TX_COL event, then a REPORT_INFORMATION message must be transmitted, as follows:

- Source: interface device
- Destination: SLIMbus manager device (LA = 0xFF)
- Information Element: MC_TX_COL

If MS is reacquired, following a previous UDEF (Received undefined message response) event, the message that caused UDEF must be retransmitted until it succeeds or until the retransmit maximum (fully managed by software) is reached.

In any case, software must clear the field SLIMBUS_FL_INFO[3] FOUND_MS. From that point on, any pending messages in the TX FIFO will be sent.

23.9.4.11.3.5 Reconfigured (RECONFIGURED)

23.9.4.11.3.5.1 Root Event

This interrupt occurs when crossing of a reconfiguration boundary. In case of clock pause, where the SLIMbus clock stops at the boundary (1st rising edge of the new superframe), the bit (and therefore the IRQ) is asserted at the clock pause, not at the clock restart.

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23.9.4.11.3.5.2 Interrupt Service Routine

Completes the software-controller reconfiguration sequence. No reconfiguration must be applied to the control registers between the RECONFIGURE_NOW reception and the reconfiguration boundary. A attempt by the manager to start a new reconfiguration sequence during that interval is an error.

In the case of framer release handover and/or root frequency change, the active framer must start using a new clock input selection at the reconfiguration boundary (as per register field SLIMBUS_FR_CLOCK_SOURCE[5:3] CLKSEL). All non-selected SLIMbus clock inputs of active framer components and all SLIMbus clock inputs for clock receiver components (inactive framers), and that may have been used until the boundary, can be turned off at that point.

Field SLIMBUS_FL_INFO[6] RECONFIGURED must be software cleared (by writing 1 to it).

23.9.4.11.4 Framer Device ISRs

The Framer Device ISRs are applied when a bit of status register FR_INFO is set, which also triggers the assertion of bit field SLIMBUS_CMP_IRQSTATUS[1] FR_INFO and of the IRQ line, when enabled in bit field SLIMBUS_CMP_IRQENABLE_SET[1] FR_INFO_EN. Service routines must be applied, and the fr_info bit field cleared (by writing 1 to it). Some interrupt generating events are collisions, which occur when the framer detects on DATA line a different value than it's actively driving.

23.9.4.11.4.1 Transmit Collision in Frame Sync Symbol (FS_TX_COL)

23.9.4.11.4.1.1 Root Event

Transmit collision detected while driving the frame sync symbol (as active framer) of the framing channel.

23.9.4.11.4.1.2 Interrupt Service Routine

A REPORT_INFORMATION message must be transmitted, as follows:

- Sender: framer device
- Destination: SLIMbus manager device (LA = 0xFF)
- Information Element: FS_TX_COL

This field is not cleared by software into the ISR. Instead, it stays set until the component receives a REQUEST_CLEAR_INFORMATION message by the remote manager (Receiving a message implies of course that message synchronization has been restored in the mean time). Only at this point, software can apply the message and clear the designated field.

23.9.4.11.4.2 Transmit Collision in Frame Sync Symbol (FI_TX_COL)

23.9.4.11.4.2.1 Root Event

Transmit collision detected while driving the framing information (as active framer) of the framing channel.

23.9.4.11.4.2.2 Interrupt Service Routine

A REPORT_INFORMATION message must be transmitted, as follows:

- Sender: framer device
- Destination: SLIMbus manager device (LA = 0xFF)
- Information Element: FI_TX_COL

This field is not cleared by software into the ISR. Instead, it stays set until the component receives a REQUEST_CLEAR_INFORMATION message by the remote manager (Receiving a message implies of course that message synchronization has been restored in the mean time). Only at this point, software can apply the message and clear the designated field.

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23.9.4.11.4.3 Transmit Collision in Guide Channel (GC_TX_COL)

23.9.4.11.4.3.1 Root Event

Transmit collision detected while driving the guide byte (as active framer), that is, during the guide channel.

23.9.4.11.4.3.2 Interrupt Service Routine

A REPORT_INFORMATION message must be transmitted, as follows:

- Sender: framer device
- Destination: SLIMbus manager device (LA = 0xFF)
- Information Element: GC_TX_COL

This field is not cleared by software into the ISR. Instead, it stays set until the component receives a REQUEST_CLEAR_INFORMATION message by the remote manager (Receiving a message implies of course that message synchronization has been restored in the mean time). Only at this point, software can apply the message and clear the designated field.

23.9.4.11.4.4 Framer Device Activated (FRAMER_ACTIVATED)

23.9.4.11.4.4.1 Root Event

Acquisition of active framer role by the component. This event is only possible on bus boot (when default active framer) and incoming framer handover (when inactive framer).

23.9.4.11.4.4.2 Interrupt Service Routine

Assert software implemented ACTIVE_FRAMER information element.

Field SLIMBUS_FR_INFO[4] FRAMER_UNACTIVATEDmust be software cleared (by writing 1 to it).

The ACTIVE_FRAMER information element's assertion does not trigger the transmission by the framer device of a REPORT_INFORMATION message, since the information is already "publicized" by the framer handover process.

23.9.4.11.4.5 Framer Device Unactivated (FRAMER_UNACTIVATED)

23.9.4.11.4.5.1 Root Event

Loss of active framer role by the component. This event is only possible on bus shutdown and outgoing framer handover (when active framer).

23.9.4.11.4.5.2 Interrupt Service Routine

Deassert software-implemented ACTIVE_FRAMER information element.

Field SLIMBUS_FR_INFO[3] FRAMER_ACTIVATED must be software cleared (by writing 1 to it).

The ACTIVE_FRAMER information element's deassertion does not trigger the transmission by the framer device of a REPORT_INFORMATION message, since the information is already "publicized" by the framer handover process.

23.9.4.11.4.6 Restart After Clock Pause (CLOCK_RESTART)

23.9.4.11.4.6.1 Root Event

Transition detected on the DATA line during a clock pause, driven by any of the connected components and seen by the clock source (active framer) as a restart request. Note that this field is set for all clock restarts, even if the local framer is inactive.

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23.9.4.11.4.6.2 Interrupt Service Routine

Field SLIMBUS_FR_INFO[5] CLOCK_RESTART must be software cleared (by writing 1 to it).

NOTE: Restart event is a source of asynchronous wakeup.

23.9.4.11.5 Shared Message Channel Transmit ISRs

These ISRs are applied when a bit of status register SMT_INFO is set, which also triggers the assertion of bit field SLIMBUS_CMP_IRQSTATUS[2] SMT_INFO and of the IRQ line, when enabled in bit field SLIMBUS_CMP_IRQENABLE_SET[2] SMT_INFO_EN. Service routines must be applied, and the fr_info bit field cleared (by writing 1 to it)

23.9.4.11.5.1 Transmit Collision in Message Body (MC_TX_COL)

23.9.4.11.5.1.1 Root Event

Transmit collision detected while transmitting a message, that is, writing any subfield except message response (arbitration, header, payload, or message integrity). The device immediately (before next cell) stop transmission and the component automatically lose message synchronization. The message has to be sent again, once message synchronization has been regained.

23.9.4.11.5.1.2 Interrupt Service Routine

This field, SLIMBUS_SMT_INFO[0] MC_TX_COL, is not cleared by software into the ISR. Instead, it stays set until the component receives a REQUEST_CLEAR_INFORMATION message by the remote manager (Receiving a message implies of course that message synchronization has been restored in the mean time). Only at this point, software can apply the message and clear the designated field.

23.9.4.11.5.2 TX Message FIFO Overflow (OVERFLOW)

23.9.4.11.5.2.1 Root Event

Overflow occurs when too many bytes are written into the TX message FIFO by the software, either because the entered message is too long or because the FIFO still contains bytes from previous messages. The state of the FIFO after an overflow event is undetermined, but the other FIFOs are unaffected.

23.9.4.11.5.2.2 Interrupt Service Routine

TX message FIFO must be cleared as explained in Section 23.9.4.10.1.2.

Field SLIMBUS_SMT_INFO[1] OVERFLOW must be software cleared (by writing 1 to it).

Message transmission must resume normally.

23.9.4.11.5.3 Received Positive Acknowledge Message Response (PACK)

23.9.4.11.5.3.1 Root Event

Message written in the TX message FIFO was transmitted after unlimited, automatic arbitration retries, and removed from the FIFO. Received message response (MR) is PACK.

23.9.4.11.5.3.2 Interrupt Service Routine

No action required for this field: SLIMBUS_SMT_INFO[2] PACK. FIFO is now available for another message.

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23.9.4.11.5.4 Received Negative Acknowledge Message Response (NACK)

23.9.4.11.5.4.1 Root Event

Message written in the TX message FIFO was transmitted after unlimited, automatic arbitration retries, and removed from the FIFO. Received message response (MR) is NACK.

23.9.4.11.5.4.2 Interrupt Service Routine

Current message must be eventually retransmitted until it succeeds or until the retransmit maximum (fully managed by software) is reached.

Field SLIMBUS_SMT_INFO[3] NACK must be software cleared (by writing 1 to it).

FIFO is available for another message, which can be the same or another one.

23.9.4.11.5.5 Received No Message Response (NORE)

23.9.4.11.5.5.1 Root Event

Message written in the TX message FIFO was transmitted after unlimited, automatic arbitration retries, and removed from the FIFO. Received message response (MR) is NORE.

23.9.4.11.5.5.2 Interrupt Service Routine

Current message must be eventually retransmitted until it succeeds or until the retransmit maximum (fully managed by software) is reached.

Field SLIMBUS_SMT_INFO[4] NORE must be software cleared (by writing 1 to it).

FIFO is available for another message, which can be the same or another one.

23.9.4.11.5.6 Received Undefined Message Response (UDEF)

23.9.4.11.5.6.1 Root Event

Message written in the TX message FIFO was transmitted after unlimited, automatic arbitration retries, and removed from the FIFO. Received message response (MR) is UDEF, that is, one of several undefined MR codes that are not combinations of legal responses, implying that an error has taken place. Component loses message synchronization, and reacquires it automatically.

23.9.4.11.5.6.2 Interrupt Service Routine

Field SLIMBUS_SMT_INFO[5] UDEF must be software cleared (by writing 1 to it).

FIFO is available for another message, which can be the same or another one.

23.9.4.11.5.7 TX Message FIFO Underflow (UNDERFLOW)

23.9.4.11.5.7.1 Root Event

Underflow takes place when the message transmission logic attempts to read more bytes than the FIFO contains. The state of the FIFO after an underflow event is undetermined, but the other FIFOs are unaffected.

23.9.4.11.5.7.2 Interrupt Service Routine

TX message FIFO must be cleared as explained in Section 23.9.4.10.1.2.

Field must be software-cleared (by writing 1 to it).

Message transmission must resume normally, making sure the error is not repeated.

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23.9.4.11.6 Shared Message Channel Receive ISRs

These ISRs are applied when a bit of status register SMR_INFO is set, which also triggers the assertion of bit field SLIMBUS_CMP_IRQSTATUS[3] SMR_INFO and of the IRQ line, when enabled in bit field SLIMBUS_CMP_IRQENABLE_SET[3] SMR_INFO_EN. Service routines must be applied, and the FR_INFO bit field cleared (by writing 1 to it)

23.9.4.11.6.1 Transmit Collision in Message Response (MC_TX_COL)

23.9.4.11.6.1.1 Root Event

Transmit collision detected while receiving a message, that is, writing the message response subfield. The component automatically loses message synchronization, and eventually reacquires it.

23.9.4.11.6.1.2 Interrupt Service Routine

The field SLIMBUS_SMR_INFO[0] MC_TX_COL must not be unconditionally software cleared, as it implements a Boolean IE that can only be cleared under specific conditions (and together with the SLIMBUS_SMT_INFO[0] MC_TX_COL).

23.9.4.11.6.2 RX Message FIFO Underflow (UNDERFLOW)

23.9.4.11.6.2.1 Root Event

Underflow takes place when too many bytes are read out of the RX message FIFO by the software, because of an error when estimating the message length, as defined in Section 23.9.4.10.2.2. The state of the FIFO after an underflow event is undetermined, but the other FIFOs are unaffected.

23.9.4.11.6.2.2 Interrupt Service Routine

RX message FIFO must be cleared as explained in Section 23.9.4.10.2.3.

Field SLIMBUS_SMR_INFO[1] UNDERFLOW must be software-cleared (by writing 1 to it).

NOTE: This software error is not supposed to take place, since the message itself is assumed to be correct and could affect the correct running of the SLIMbus protocol, if the received message cannot be recovered.

23.9.4.11.6.3 RX Message FIFO Overflow (OVERFLOW)

23.9.4.11.6.3.1 Root Event

Overflow occurs when too many bytes are received into the RX message FIFO because the entered message is too long. The state of the FIFO after an overflow event is undetermined, but the other FIFOs are unaffected.

23.9.4.11.6.3.2 Interrupt Service Routine

RX message FIFO must be cleared as explained in Section 23.9.4.10.2.3.

Field must be software cleared (by writing 1 to it).

Message transmission must resume normally.

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23.9.4.11.6.4 Message Received (RECEIVED_MESSAGE)

23.9.4.11.6.4.1 Root Event

A message has been received and checked by the hardware: target address matches a local device (LA or EA), message length is coherent with AT/RL fields, integrity is correct for both PI and MI, all target devices acknowledged the message (PACK MR transmitted and received).

23.9.4.11.6.4.2 Interrupt Service Routine

Received message must be unloaded from RX message FIFO, parsed, and the appropriate action taken, as explained in Section 23.9.4.10.2.2.

Field SLIMBUS_SMR_INFO[2] RECEIVED_MESSAGE must be software cleared (by writing 1 to it). This will also clear the message FIFO and allow the local component to respond PACK to new incoming messages.

23.9.4.11.6.5 Reconfigure_now Message Received (RECEIVED_RECONFIGURE)

23.9.4.11.6.5.1 Root Event

A message has been received as in RECEIVED_MESSAGE event above, with the additional condition that it has been recognized by hardware as a RECONFIGURE_NOW() message. Note that by the time the ISR is executed, the reconfiguration may have already taken place.

23.9.4.11.6.5.2 Interrupt Service Routine

Field SLIMBUS_SMR_INFO[3] RECEIVED_CONFIGURE must be software cleared (by writing 1 to it).

23.9.4.11.7 Data Channel Port ISRs

These ISRs are applied when a bit of a status register SLIMBUS_DCT_INFO_j and/or SLIMBUS_DCR_INFO_j is set, which also triggers the assertion of bit field SLIMBUS_CMP_IRQSTATUS[11:4] DCT_INFO_j/DCR_INFO_j and of the IRQ line, when enabled in bit field SLIMBUS_CMP_IRQENABLE_SET[11:4] DCT/DCR_INFO_j. Service routines must be applied, and the SLIMBUS_DCT_INFO_j and/or SLIMBUS_DCR_INFO_j bit fields cleared (by writing 1 to it).

23.9.4.11.7.1 Transmit Collision in Data Channel Port (DATA_TX_COL)

23.9.4.11.7.1.1 Root Event

Transmit collision detected while writing to the considered data channel, in any of the TAG, AUX, or DATA fields. Note that transmit collisions are possible even for receive ports, as those port may also write some TAG cells (that is, for pulled TP), where transmit collisions are possible. The device must immediately (before next cell) stop writing to the bus, only resuming on next segment.

23.9.4.11.7.1.2 Interrupt Service Routine

The REPORT_INFORMATION message must be transmitted, from the port's stereo or voice device (that is, with that device's LA in source address of arbitration field), to the active manager (that is, with manager's target LA in header = 0xFF), and containing the information element (IE) of the same name (DATA_TX_COL).

The field SLIMBUS_DCT_INFO_j[0] DATA_TX_COL and/or SLIMBUS_DCR_INFO_j[0] DATA_TX_COL must not be unconditionally software cleared, as it implements a boolean IE that can only be cleared under specific conditions.

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23.9.4.11.7.2 Data Channel FIFO Overflow (OVERFLOW)

23.9.4.11.7.2.1 Root Event

Overflow occurs when the data rate into the FIFO exceeds the data rate out of the FIFO for a sufficient amount of time, which can happen in both TX and RX ports. The state of the FIFO after an overflow event is undetermined, but the other FIFOs are unaffected.

23.9.4.11.7.2.2 Interrupt Service Routine

The SLIMbus protocol does not specify the handling of such an event. However, since data integrity cannot be guaranteed following an that event, stopping the channel is an option.

Field SLIMBUS_DCT_INFO_j[1] / SLIMBUS_DCR_INFO_j[1] OVERFLOW must be software cleared (by writing 1 to it).

23.9.4.11.7.3 Data Channel FIFO Underflow (UNDERFLOW)

23.9.4.11.7.3.1 Root Event

Overflow occurs when the data rate out of the FIFO exceeds the data rate into the FIFO for a sufficient amount of time, which can happen in both TX and RX ports. The state of the FIFO after an underflow event is undetermined, but the other FIFOs are unaffected.

23.9.4.11.7.3.2 Interrupt Service Routine

The SLIMbus protocol does not specify the handling of such an event. However, since data integrity cannot be guaranteed following an that event, stopping the channel is an option.

Field SLIMBUS_DCT_INFO_j[2] / SLIMBUS_DCR_INFO_j[2] UNDERFLOW must be software cleared (by writing 1 to it).

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23.9.5 SLIMbus Programming Guide

23.9.5.1 SLIMbus Low-Level Programming Models

This section describes the low-level programming sequences for the configuration and use of the SLIMbus module. Because the SLIMbus protocol is implemented partly by hardware and partly by software in the current module, some higher-level procedures, such as sending and answering specific SLIMbus protocol messages, are mentioned for the sake of clarity.

23.9.5.1.1 Global Initialization

23.9.5.1.1.1 Surrounding Modules Global Initialization

This section identifies the requirements for initializing the surrounding modules when the SLIMbus module is to be used for the first time after a device reset. This initialization of surrounding modules is based on the integration and environment of the SLIMbus module. See Section 23.9.3, *SLIMbus Integration*, and Section 23.9.2, *SLIMbus Environment*, for further information.

Table 23-671. Global Initialization of Surrounding Modules

Surrounding Modules	Comments
PRCM	The required SLIMbus clocks must be enabled. If the SLIMbus module does not contain the active frame, it receives its functional clock (SLIMbus clock) from the CLK pin. For a summary of the SLIMbus clocks, see Table 23-653. See Chapter 3, *Power, Reset, and Clock Management*
Control Module	Module specific pad multiplexing must be set in the control module. For more information about the module configuration, see Chapter 18, *Control Module*.
(Optional) L4 Interconnect	For information about the L4-PER interconnect configuration, see Chapter 13, *Interconnect*.
(Optional) INTC	Cortex-A9 MPU and DSP subsystem INTCs must be configured to enable the interrupt requests to the Cortex-A9 MPU or to the DSP subsystem.
(Optional) sDMA and/or aDMA	sDMA (aDMA) configuration must be done to enable the module DMA channel requests. See Chapter 16, *sDMA*.

23.9.5.1.1.2 SLIMbus Global Initialization

23.9.5.1.1.2.1 SLIMbus Module Software Reset

This procedure brings the SLIMbus module to a known state.

Table 23-672. SLIMbus Module Software Reset

Step	Register/Bit Field/Programming Model	Value
Initiate a software reset.	SLIMBUS_CMP_SYSCONFIG[0] SOFTRESET	0x1
Wait until reset is finished.	SLIMBUS_CMP_SYSCONFIG[0] SOFTRESET	=0x0

23.9.5.1.1.2.2 Power Management and Wake-Up Configuration

This procedure configures the idle mode for SLIMbus component. By definition, the target can handle read/write transactions as long as it is out of IDLE state.

Table 23-673. SLIMbus Power Management

Step	Register/Bit Field/Programming Model	Value
Configure the local power management.	SLIMBUS_CMP_SYSCONFIG[3:2] IDLEMODE	0x-
Turn on/off internal clock autogating.	SLIMBUS_CMP_SYSCONFIG[8] AUTOGATINGDISABLE	0x-

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23.9.5.1.2 SLIMbus Component Boot

The component boot sequence is initiated when the component decides to join the bus.

23.9.5.1.2.1 Clock Source Component Boot

This procedure performs component boot in clock source mode (the component contains the active framer of the given bus).

Table 23-674. Clock Source Component Boot

Step	Register/Bit Field/Programming Model	Value
Set the active-framer boot flag.	SLIMBUS_FR_CONTROL[0] BOOT	0x1
Select the subframe length and the control space width: subframe mode (SM).	SLIMBUS_FL_SM[4:0] SM	0x--
Select root/SLIMbus frequency ratio: clock gear (CG).	SLIMBUS_FL_CG[3:0] CG	0x-
Indicate the root frequency (RF) to the framer device.	SLIMBUS_FL_RF[3:0] RF	0x-
Select a source of the functional (SLIMbus) clock (See also , *SLIMbus Integration*).	SLIMBUS_FR_CLOCK_SOURCE[5:3] CLKSEL	0x-
Select a root divider ratio to obtain the desired root frequency (RF).	SLIMBUS_FR_CLOCK_SOURCE[2:0] CLKDIV	0x-
Initiate reconfiguration.	SLIMBUS_FL_CONTROL[2] FORCE_RECONFIGURE	0x1
Wait for reconfiguration to finish.	SLIMBUS_FL_CONTROL[2] FORCE_RECONFIGURE	=0x0

23.9.5.1.2.2 Clock Receiver Component Boot

This procedure boots the SLIMbus when the component is in clock receiver mode (inactive framer).

Table 23-675. Clock Receiver Component Boot

Step	Register/Bit Field/Programming Model	Value
Set inactive-framer boot flag.	SLIMBUS_FL_CONTROL[0] BOOT	0x1
Initiate reconfiguration.	SLIMBUS_FL_CONTROL[2] FORCE_RECONFIGURE	0x1
Wait for reconfiguration to finish.	SLIMBUS_FL_CONTROL[2] FORCE_RECONFIGURE	=0x0

23.9.5.1.3 Data Agent Assignment

Before a SLIMbus device enumeration, it is assumed to have a given number of ports, and each port a given set of properties. Software must keep a data port table, updated by various events including SLIMbus resets, data channel config messages, and some reconfiguration messages.

At least one data agent (which implements the data ports in hardware) must be assigned to a SLIMbus device before it can receive/transmit actual payload data. The following settings must be done to configure the SLIMbus module.

Table 23-676. Data Agent Assignment

Step	Register/Bit Field/ Programming Model	Value
Set the port number (PN) for TX and/or RX data agent j. Must be unique within the device that it is mapped to..	SLIMBUS_DCT_MAP_j[13:8] PN SLIMBUS_DCR_MAP_j[13:8] PN	0x--
Set the index of the device (DI) TX and or RX data agent j belongs to.	SLIMBUS_DCT_MAP_j[7:0] DI SLIMBUS_DCR_MAP_j[7:0] DI	0x--
Validate settings.	SLIMBUS_FL_CONTROL [8] VALIDATE_DCMAP	0x1

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23.9.5.1.4 Device Enumeration

Device enumeration is an acquisition of a dynamic logical address (LA) assigned by the active manager device. The LA ranges from 0x00 to 0xEF, with the exception of the active manager itself, located by definition at LA = 0xFF.

23.9.5.1.4.1 Manager Device Enumeration

This procedure performs an manager device enumeration when the local manager device is the bus active manager.

Table 23-677. Manager Device Enumeration

Step	Register/Bit Field/Programming Model	Value
Wait for message synchronization.	SLIMBUS_FL_INFO [3] FOUND_MS	=0x1
Explicitly enumerate the device as active manager device.	SLIMBUS_DEV_LA_i[7:0] LA SLIMBUS_DEV_LA_i[8] LA_ENABLE SLIMBUS_DEV_LA_i[9] EA_ENABLE	0xFF 0x1 0x1

23.9.5.1.4.2 Non-Manager Device Enumeration

This procedure is used when a non-manager device decides to participate on the bus. When the SLIMbus module contains the active manager, software must also perform the manager-side actions.

Table 23-678. Non-Manager Device Enumeration

Step	Register/Bit Field/Programming Model	Value
Enable the device to receive broadcast messages.	SLIMBUS_DEV_LA_i[9] EA_ENABLE	0x1
Wait for message synchronization or for REQUEST_SELF_ANNOUNCEMENT() message from active manager.	SLIMBUS_FL_INFO [3] FOUND_MS or see Section 23.9.5.1.6, *SLIMbus Transfer Procedures*.	=0x1
Send REPORT_PRESENT() message to the active manager (LA = 0xFF).	See Section 23.9.5.1.6, *SLIMbus Transfer Procedures*.	
Wait for ASSIGN_LOGICAL_ADDRESS(LA) message from the active manager.	See Section 23.9.5.1.6, *SLIMbus Transfer Procedures*.	
Extract the LA from the message and set it in the hardware.	SLIMBUS_DEV_LA_i[7:0] LA SLIMBUS_DEV_LA_i[8] LA_ENABLE	0x-- 0x1

23.9.5.1.5 Operational Modes Configuration

23.9.5.1.5.1 SLIMbus Transfer Protocol Configuration

This procedure configures the data channel(s) for a specific transfer protocol use. It is assumed that at this moment the required channels are connected by means of CONNECT_SOURCE(PN,CN) and CONNECT_SINK(PN,CN) messsages. No action on hardware is required after receiving these messages, except for the standard checks and clearing of the message FIFO. The channel numbers (CN) are kept and handled by software. The steps listed are required from the configured side, but if the local component contains the active manager software must also perform the configuration steps. Changing the order of NEXT_* messages is allowed.

Table 23-679. SLIMbus Transfer Protocol Configuration

Step	Register/Bit Field/Programming Model	Value
Wait for BEGIN_RECONFIGURATION() message.		
Clear reconfiguration parameters.	SLIMBUS_FL_CONTROL [7] CLEAR_RECONFIGURATION	0x1
Wait for NEXT_DEFINE_CHANNEL(CN, TP, SD, SL) message.	See Section 23.9.5.1.6, *SLIMbus Transfer Procedures*.	

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Table 23-679. SLIMbus Transfer Protocol Configuration (continued)

Step	Register/Bit Field/Programming Model	Value
Extract and set in hardware the transfer protocol (TP) for RX data agent j and/or for TX data agent j.	SLIMBUS_DCR_CONFIG1_j[3:0] TP SLIMBUS_DCT_CONFIG1_j[3:0] TP	0x-
Extract and set in hardware the segment distribution (SD) for RX data agent j and/or for TX data agent j.	SLIMBUS_DCR_CONFIG2_j[11:0] SD SLIMBUS_DCT_CONFIG2_j[11:0] SD	0x---
Extract and set in hardware the segment length (SL) for RX data agent j and/or for TX data agent j.	SLIMBUS_DCR_CONFIG1_j[9:5] SL SLIMBUS_DCT_CONFIG1_j[9:5] SL	0x--
IF: Transfer protocol is asynchronous simplex	TP	=0x4 or =0x6
Set secondary owner if data agent j is RX or set primary owner if data agent j is TX.	SLIMBUS_DCR_CONFIG1_j[4] TP_QUALIFIER SLIMBUS_DCT_CONFIG1_j[4] TP_QUALIFIER	0x1 0x0
ELSEIF: Asynchronous half-duplex	TP	=0x5 or =0x7
Set ownership for data channel (combines one TX and one RX data agent).	SLIMBUS_DCR_CONFIG1_j[4] TP_QUALIFIER SLIMBUS_DCT_CONFIG1_j[4] TP_QUALIFIER	0x-
ENDIF		
Wait for NEXT_DEFINE_CONTENT(CN, FL, PR, AF, DT, CL, DL) message.	See Section 23.9.5.1.6, *SLIMbus Transfer Procedures*.	
Extract and set in hardware the number of AUX slots in a segment for RX data agent j and/or for TX data agent j.	SLIMBUS_DCR_CONFIG1_j[19:16] AF SLIMBUS_DCT_CONFIG1_j[19:16] AF	0x--
IF: Data type (DT) extracted from message is LPCM audio	DT	=0x1
Enable unsigned-to-OSAM encoding for RX data agent j and/or for TX data agent j.	SLIMBUS_DCR_CONFIG1_j[28] DT_LPCM SLIMBUS_DCT_CONFIG1_j[28] DT_LPCM	0x1
ELSE		
Disable unsigned-to-OSAM encoding for RX data agent j and/or for TX data agent j.	SLIMBUS_DCR_CONFIG1_j[28] DT_LPCM SLIMBUS_DCT_CONFIG1_j[28] DT_LPCM	0x0
ENDIF		
Extract and set in hardware the channel link bit (CL) for RX data agent j and/or for TX data agent j	SLIMBUS_DCR_CONFIG1_j[15] CL SLIMBUS_DCT_CONFIG1_j[15] CL	0x-
Extract and set in hardware the AUX + data length (DL) for RX data agent j and/or for TX data agent j.	SLIMBUS_DCR_CONFIG1_j[14:10] DL SLIMBUS_DCT_CONFIG1_j[14:10] DL	0x--
Perform the data FIFO(s) setup for RX and/or TX data agent(s).	See Section 23.9.5.1.5.2, *SLIMbus Data FIFO Mapping and Setup.*	
Wait for NEXT_ACTIVATE_CHANNEL() message.	See Section 23.9.5.1.6, *SLIMbus Transfer Procedures*.	
Request enabling of RX data agent j and/or of TX data agent j.	SLIMBUS_DCR_CONFIG1_j[31] ENABLE SLIMBUS_DCT_CONFIG1_j[31] ENABLE	0x1
Wait for RECONFIGURE_NOW() message.	See Section 23.9.5.1.6, *SLIMbus Transfer Procedures*.	
This message is hardware-decoded and executed. No software action on the module is required except for emptying the FIFO to allow receiving of further messages.	SLIMBUS_SMR_INFO[2] RECEIVED_MESSAGE [3] RECEIVED_CONFIGURE	0x1

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23.9.5.1.5.2 SLIMbus Data FIFO Mapping and Setup

This procedure maps each used FIFO to a free zone of the shared buffer. It also sets the FIFO thresholds used to trigger loading and unloading the FIFOs. These settings depend on the available free space, segment word length, and required FIFO depth. Thus, at this moment, the protocol type must be known and the data agent must not be enabled.

Table 23-680. SLIMbus Data FIFO Mapping and Setup

Step	Register/Bit Field/Programming Model	Value
Set the capacity (in segment words) of data FIFO for RX agent j and/or for TX data agent j.	SLIMBUS_DCR_FIFO_SETUP2_j[7:0] SIZE SLIMBUS_DCT_FIFO_SETUP2_j[7:0] SIZE	0x--
Set the FIFO base address within shared RAM for RX agent j and/or for TX data agent j.	SLIMBUS_DCR_FIFO_SETUP1_j[11:5] BASE_ADDR SLIMBUS_DCT_FIFO_SETUP1_j[11:5] BASE_ADDR	0x--
Set SLIMbus-side FIFO threshold for RX data agent j and/or for TX data agent j.	SLIMBUS_DCR_FIFO_SETUP2_j[15:8] SB_THRESHOLD SLIMBUS_DCT_FIFO_SETUP2_j[15:8] SB_THRESHOLD	0x--
Set software-side FIFO threshold for RX data agent j and/or for TX data agent j.	SLIMBUS_DCR_FIFO_SETUP2_j[23:16] DMA_THRESHOLD SLIMBUS_DCT_FIFO_SETUP2_j[23:16] DMA_THRESHOLD	0x--
Bring the FIFO to empty state: RX data agent j and/or TX data agent j.	SLIMBUS_DCR_FIFO_SETUP1_j[0] FIFO_CLEAR SLIMBUS_DCT_FIFO_SETUP1_j[0] FIFO_CLEAR	0x1
Wait for clearing to complete.	SLIMBUS_DCR_FIFO_SETUP1_j[0] FIFO_CLEAR SLIMBUS_DCT_FIFO_SETUP1_j[0] FIFO_CLEAR	=0x0

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23.9.5.1.6 SLIMbus Transfer Procedures

This section describes the low-level programming steps for message and data reception and transmission. For more information about message syntax, see the *MIPI Alliance Specification for SLIMbus Version 1.01.00*.

23.9.5.1.6.1 Transmitting Message, Polling Mode

This procedure transmits a message over the SLIMbus without the use of interrupts.

Table 23-681. Message Transmit Procedure, Polling Method

Step	Register/Bit Field/Programming Model	Value
Wait if an ongoing TX message is still in progress.	SLIMBUS_SMT_CONTROL[0] MESSAGE_ENABLE	=0x0
Clear TX message event flags.	SLIMBUS_SMT_INFO[7:0]	0xBF
Load the whole message byte-by-byte, except for the last one. That is, message integrity (MI) and response (MR), which are handled by hardware. The primary integrity (PI) field is computed and overwritten by hardware; thus, write any value for PI. The message cannot be larger than the FIFO size.	SLIMBUS_SMT_MESSAGE[7:0]	0x--
Initiate the transmit sequence.	SLIMBUS_SMT_CONTROL[0] MESSAGE_ENABLE	0x1
Check the message outcome by polling the information register bits. Process the event as described in Section 23.9.5.1.7, *Event Handling*.	SLIMBUS_SMT_INFO Negative response: [3] NACK Positive response: [2] PACK No response: [4] NORE Illegal response: [5] UDEF FIFO overflow: [1] OVERFLOW Transmit collision: [0] MC_TX_COL Message sync loss: [7] ABORT	=0x1

23.9.5.1.6.2 Transmitting Message, Interrupt Mode

This procedure transmits a message over the SLIMbus with interrupts enabled.

Table 23-682. Message Transmit Procedure, Interrupt Method

Step	Register/Bit Field/Programming Model	Value
Enable the shared-message-channel transmit interrupts.	SLIMBUS_CMP_IRQENABLE_SET[2] SMT_INFO_EN	0x1
Clear the interrupt status bit.	SLIMBUS_CMP_IRQSTATUS [2] SMT_INFO	0x1
The procedure continues without difference from polling mode. The exception is that if any info bit is set, it triggers an interrupt. The interrupt-service-routine then checks which info bit is set.	See Section 23.9.5.1.6.1, *Transmitting Message, Polling Mode.*	

23.9.5.1.6.3 Receiving Message, Polling Mode

This procedure reads a received in FIFO message without using interrupts.

Table 23-683. Message Receive Procedure, Polling Method

Step	Register/Bit Field/Programming Model	Value
Check for a received message.	SLIMBUS_SMR_INFO[2] RECEIVED_MESSAGE	=0x1
IF: Message is RECONFIGURE_NOW()	SLIMBUS_SMR_INFO[3] RECEIVED_RECONFIGURE	=0x1
RECONFIGURE_NOW() is hardware-decoded and executed. Software is required only to allow further message reception.	SLIMBUS_SMR_INFO[2] RECEIVED_MESSAGE SLIMBUS_SMR_INFO[3] RECEIVED_RECONFIGURE	0x1
ELSE		

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Table 23-683. Message Receive Procedure, Polling Method (continued)

Step	Register/Bit Field/Programming Model	Value
Read the message byte-by-byte and decode it in parallel. The message size is determined from the message itself, from the arbitration type (AT) and remaining length (RL) fields. Read until message end is reached: (2 bytes if AT = 0xF, or 7 bytes if AT = 0x5) + 1 byte + RL bytes	SLIMBUS_SMR_MESSAGE[7:0]	0x-
Optionally, software can check for FIFO underflow event after every read out. Last byte then must be ignored. The event flag must be cleared by writing 0x1 to it.	SLIMBUS_SMR_INFO[1] UNDERFLOW SLIMBUS_SMR_INFO[1] UNDERFLOW	=0x1 0x1
Allow further message reception.	SLIMBUS_SMR_INFO[2] RECEIVED_MESSAGE	0x1
ENDIF		

23.9.5.1.6.4 Receiving Message, Interrupt Mode

This procedure reads the received in FIFO message by using interrupts.

Table 23-684. Message Receive, Interrupt Method

Step	Register/Bit Field/Programming Model	Value
Enable the shared-message-channel receive interrupts.	SLIMBUS_CMP_IRQENABLE_SET[3] SMR_INFO_EN	0x1
Clear the interrupt status bit.	SLIMBUS_CMP_IRQSTATUS [3] SMR_INFO	0x1
Wait for SMR_INFO interrupt.		
Clear the interrupt status bit.	SLIMBUS_CMP_IRQSTATUS [3] SMR_INFO	0x1
The procedure continues without difference from polling mode. The exception is that any set info bit triggers an interrupt. The interrupt-service-routine then checks to determine which event occurred.	See Section 23.9.5.1.6.3, *Receiving Message, Polling Mode.*	

23.9.5.1.6.5 Receiving Data

This procedure reads actual payload data off the FIFO. The data is read one data segment at a time (AUX + data) with no packing mode. Packing allows several small segments to be fit in a single FIFO access. Packing mode is selected through the SLIMBUS_DCR_FIFO_SETUP2_j[31] PACKING bit field.

Table 23-685. Receiving Data, Polling Method

Step	Register/Bit Field/Programming Model	Value
Wait for SLIMBUS_DCR_FIFO_SETUP2_j[23:16] DMA_THRESHOLD number of segment words to be available in FIFO.	SLIMBUS_DCR_FIFO_STATUS_j [1] HILEVEL	=0x1
Read SLIMBUS_DCR_FIFO_SETUP2_j[23:16] DMA_THRESHOLD segment words from FIFO.	SLIMBUS_DCR_DATA_j	See (1).
Additionally, software can check whether no more segments are available to read.	SLIMBUS_DCR_FIFO_STATUS_j [0] EMPTY	=0x1

(1) Segment word size varies between 1 and 8 slots (4 and 32 bits). Segments can be in packed or nonpacked mode.

The following procedure uses an interrupt method to receive data.

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Table 23-686. Receiving Data, Interrupt Method

Step	Register/Bit Field/Programming Model	Value
Enable the data receive interrupt. Write 0x1 for the required data agent.	SLIMBUS_CMP_IRQENABLE_SET	0x1
Clear the corresponding interrupt status bit.	SLIMBUS_CMP_IRQSTATUS	0x1
Wait for interrupt.		
Check the high-level info bit.	SLIMBUS_DCR_INFO_j[3] HILEVEL	=0x1
Clear the interrupt status bit of the data agent.	SLIMBUS_CMP_IRQSTATUS	0x1
Read SLIMBUS_DCR_FIFO_SETUP2_j[23:16] DMA_THRESHOLD segment words from FIFO.	SLIMBUS_DCR_DATA_j	See (1)
Additionally, software can check whether no more segments are available to read.	SLIMBUS_DCR_FIFO_STATUS_j [0] EMPTY	=0x1
Clear the hghi-level info bit.	SLIMBUS_DCR_INFO_j[3] HILEVEL	0x1

(1) Segment word size varies between 1 and 8 slots (4 and 32 bits). Segments can be in packed or nonpacked mode.

This procedure enables DMA request generation to the sDMA or aDMA engine, which must be configured in advance. DMA request starts whenever the threshold condition is met. DMA request stops after a certain number of nonempty read accesses to the FIFO are complete. This size typically corresponds to a DMA burst and in the SLIMBUS_DCR_FIFO_SETUP1_j[4:1] DMA_REQ_SIZE bit field.

Table 23-687. Receiving Data, DMA Enable

Step	Register/Bit Field/Programming Model	Value
Set DMA request size (for precise DMA mode).	SLIMBUS_DCR_FIFO_SETUP1_j[4:1] DMA_REQ_SIZE	0x-
Enable the data receive DMA requests. Write 0x1 for the required RX data agent.	SLIMBUS_CMP_DMAENABLE_SET	0x1

23.9.5.1.6.6 Transmitting Data

This procedure loads actual payload data into the FIFO. The data is loaded one data segment at a time (AUX + data), when packing mode is not used. Packing allows several small segments to be fit into a single FIFO access. Packing mode is selected through the SLIMBUS_DCT_FIFO_SETUP2_j[31] PACKING bit field.

Table 23-688. Transmitting Data, Polling Method

Step	Register/Bit Field/Programming Model	Value
Wait for SLIMBUS_DCT_FIFO_SETUP2_j[23:16] DMA_THRESHOLD number of free segment words.	SLIMBUS_DCT_FIFO_STATUS_j [1] LOLEVEL	=0x1
Write SLIMBUS_DCR_FIFO_SETUP2_j[23:16] DMA_THRESHOLD segment words to FIFO.	SLIMBUS_DCT_DATA_j	See (1)
Additionally, software can check whether no more FIFO space is available to write.	SLIMBUS_DCT_FIFO_STATUS_j [0] FULL	=0x1

(1) Segment word size varies between 1 and 8 slots (4 and 32 bits). Segments can be in packed or nonpacked mode.

The following procedure uses an interrupt method to transmit data.

Table 23-689. Transmitting Data, Interrupt Method

Step	Register/Bit Field/Programming Model	Value
Enable the data transmit interrupt. Write 0x1 for the required data agent.	SLIMBUS_CMP_IRQENABLE_SET	0x1
Clear the corresponding interrupt status bit.	SLIMBUS_CMP_IRQSTATUS	0x1
Wait for interrupt.		

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Table 23-689. Transmitting Data, Interrupt Method (continued)

Step	Register/Bit Field/Programming Model	Value
Check the low-level info bit.	SLIMBUS_DCT_INFO_j [3] LOLEVEL	=0x1
Clear the interrupt status bit of the data agent.	SLIMBUS_CMP_IRQSTATUS	0x1
Read SLIMBUS_DCT_FIFO_SETUP2_j[23:16] DMA_THRESHOLD segment words from FIFO.	SLIMBUS_DCT_DATA_j	See (1)
Additionally, software can check if no more space is available to write	SLIMBUS_DCT_FIFO_STATUS_j [0] FULL	=0x1
Clear the low-level info bit.	SLIMBUS_DCT_INFO_j [3] LOLEVEL	0x1

(1) Segment word size varies between 1 and 8 slots (4 and 32 bits). Segments can be in packed or nonpacked mode.

This procedure enables DMA request generation to the sDMA or aDMA engine, which must be configured in advance. DMA request starts whenever the threshold condition is met. DMA requests stops after a certain number of nonempty read accesses to the FIFO are complete. This size typically corresponds to a DMA burst and in the SLIMBUS_DCT_FIFO_SETUP1_j[4:1] DMA_REQ_SIZE bit field.

Table 23-690. Transmitting Data, DMA Enable

Step	Register/Bit Field/Programming Model	Value
Set DMA request size (for presize DMA mode).	SLIMBUS_DCT_FIFO_SETUP1_j[4:1] DMA_REQ_SIZE	0x-
Enable the data receive DMA requests. Write 0x1 for the required TX data agent.	SLIMBUS_CMP_DMAENABLE_SET	0x1

23.9.5.1.7 Event Handling

Events must be serviced in the following way:

1. Clear the interrupt status bit (if interrupts are enabled).
2. Read the relative information register to determine the event.
3. Process the event as required. See Section 23.9.4.11.1, *Interrupt Requests*.
4. When needed and allowed, clear the information register bit(s). For example, it is not necessary to clear the SLIMBUS_SMR_INFO[2] RECEIVED_MESSAGE bit until the message is read, decoded, and executed, as it will allow the reception of other messages.

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23.9.6 SLIMbus Register Manual

23.9.6.1 SLIMbus Register Overview

The registers described in this section are prefixed with one of the following:

- **CMP:** Component- (that is, module) level control and status.
- **SMT:** Shared Messages Transmit: All messages transmitted to the serial SLIMbus interface. This resource is shared by all devices within the component (all devices can transmit messages).
- **SMR:** Shared Messages Receive: All messages received from the serial SLIMbus interface. This ressource is shared by all devices within the component (all devices can receive messages).
- **FL:** Frame Layer status and control. The frame layer is the hardware-implemented protocol layer located just above the physical layer, and shared by all devices of a component.
- **FR:** Framer device-specific status and control. The framer device is one of the component's devices (logical entities of the SLIMbus); exactly one framer device may optionally be implemented in each SLIMbus component. Note that the framer device is not always active (in which case the related registers aren't used either), and that some of the framer's control and status is shared with the (always-present, always-active) interface device.
- **DEV:** Device control and status. The same register structure is repeated as many times as there are devices supported by the component (that is, the module), including the (compulsory) interface device, the framer device (optional), the manager device (optional), and the generic devices (optional, one or several instances).
- **DCT:** Data Channel Transmit: The same register structure is repeated as many times as there are transmit data channels supported, that is, FIFOs and associated logic. Devices (typically generic devices) are associated to a data channel for the transmissions of data towards the SLIMbus serial interface.
- **DCR:** Data Channel Receive: The same register structure is repeated as many times as there are receive data channels supported, that is, FIFOs and associated logic. Devices (typically generic devices) are associated to a data channel for the reception of data from the SLIMbus serial interface.

23.9.6.2 SLIMbus Instance Summary

Table 23-691 shows the base address and address space for the SLIMbus module instances.

Table 23-691. SLIMbus Instance Summary

Module Name	Base Address L3 Interconnect	Base Address Cortex-A9 Private Access	Base Address DSP Private Access	Size
SLIMBUS1	0x4902 C000	0x4012 C000	0x2 C000	4 KB
SLIMBUS2	0x4807 6000	-	-	4 KB

NOTE: Private Access is an access which is not using the L3/L4 interconnects.

23.9.6.3 SLIMbus Registers

23.9.6.3.1 SLIMBUS1 Register Summary

Table 23-692. SLIMBUS1 Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	Physical Address L3 Interconnect	Physical Address Cortex-A9 Private Access	Physical Address DSP Private Access
SLIMBUS_CMP_REVISION	R	32	0x0000 0000	0x4902 C000	0x4012 C000	0x2 C000
SLIMBUS_CMP_HWINFO	R	32	0x0000 0004	0x4902 C004	0x4012 C004	0x2 C004
SLIMBUS_CMP_SYSCONFIG	RW	32	0x0000 0010	0x4902 C010	0x4012 C010	0x2 C010

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Table 23-692. SLIMBUS1 Register Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	Physical Address L3 Interconnect	Physical Address Cortex-A9 Private Access	Physical Address DSP Private Access
RESERVED	RW	32	0x0000 0020	0x4902 C020	0x4012 C020	0x2 C020
SLIMBUS_CMP_IRQSTATUS_RAW	RW	32	0x0000 0024	0x4902 C024	0x4012 C024	0x2 C024
SLIMBUS_CMP_IRQSTATUS	RW	32	0x0000 0028	0x4902 C028	0x4012 C028	0x2 C028
SLIMBUS_CMP_IRQENABLE_SET	RW	32	0x0000 002C	0x4902 C02C	0x4012 C02C	0x2 C02C
SLIMBUS_CMP_IRQENABLE_CLR	RW	32	0x0000 0030	0x4902 C030	0x4012 C030	0x2 C030
SLIMBUS_CMP_DMAENABLE_SET	RW	32	0x0000 0034	0x4902 C034	0x4012 C034	0x2 C034
SLIMBUS_CMP_DMAENABLE_CLR	RW	32	0x0000 0038	0x4902 C038	0x4012 C038	0x2 C038
SLIMBUS_CMP_IV	RW	32	0x0000 0040	0x4902 C040	0x4012 C040	0x2 C040
SLIMBUS_CMP_MI_PC	RW	32	0x0000 0044	0x4902 C044	0x4012 C044	0x2 C044
SLIMBUS_SMT_INFO	RW	32	0x0000 0050	0x4902 C050	0x4012 C050	0x2 C050
SLIMBUS_SMT_MESSAGE	RW	32	0x0000 0054	0x4902 C054	0x4012 C054	0x2 C054
SLIMBUS_SMT_CONTROL	RW	32	0x0000 0058	0x4902 C058	0x4012 C058	0x2 C058
SLIMBUS_SMT_FIFO_SETUP	RW	32	0x0000 005C	0x4902 C05C	0x4012 C05C	0x2 C05C
SLIMBUS_SMR_INFO	RW	32	0x0000 0060	0x4902 C060	0x4012 C060	0x2 C060
SLIMBUS_SMR_MESSAGE	R	32	0x0000 0064	0x4902 C064	0x4012 C064	0x2 C064
SLIMBUS_SMR_CONTROL	RW	32	0x0000 0068	0x4902 C068	0x4012 C068	0x2 C068
SLIMBUS_SMR_FIFO_SETUP	RW	32	0x0000 006C	0x4902 C06C	0x4012 C06C	0x2 C06C
SLIMBUS_FL_INFO	RW	32	0x0000 0070	0x4902 C070	0x4012 C070	0x2 C070
SLIMBUS_FL_CONTROL	RW	32	0x0000 0074	0x4902 C074	0x4012 C074	0x2 C074
SLIMBUS_FL_SM	RW	32	0x0000 0078	0x4902 C078	0x4012 C078	0x2 C078
SLIMBUS_FL_CG	RW	32	0x0000 007C	0x4902 C07C	0x4012 C07C	0x2 C07C
SLIMBUS_FL_RF	RW	32	0x0000 0080	0x4902 C080	0x4012 C080	0x2 C080
SLIMBUS_FR_INFO	RW	32	0x0000 0090	0x4902 C090	0x4012 C090	0x2 C090
SLIMBUS_FR_CLOCK_SOURCE	RW	32	0x0000 0094	0x4902 C094	0x4012 C094	0x2 C094
SLIMBUS_FR_CONTROL	RW	32	0x0000 0098	0x4902 C098	0x4012 C098	0x2 C098
SLIMBUS_FR_FRAMER_HANDOVER	RW	32	0x0000 009C	0x4902 C09C	0x4012 C09C	0x2 C09C
SLIMBUS_FR_CLOCK_PAUSE	RW	32	0x0000 00A0	0x4902 C0A0	0x4012 C0A0	0x2 C0A0
SLIMBUS_DEV_LA_i [(1)]	RW	32	0x0000 0100 + (0x10 * i)	0x4902 C100 + (0x10 * i)	0x4012 C100 + (0x10 * i)	0x2 C100 + (0x10 * i)
SLIMBUS_DEV_EA_LO_i [(1)]	R	32	0x0000 0104 + (0x10 * i)	0x4902 C104 + (0x10 * i)	0x4012 C104 + (0x10 * i)	0x2 C104 + (0x10 * i)
SLIMBUS_DEV_EA_HI_i [(1)]	R	32	0x0000 0108 + (0x10 * i)	0x4902 C108 + (0x10 * i)	0x4012 C108 + (0x10 * i)	0x2 C108 + (0x10 * i)
SLIMBUS_DCT_INFO_j [(2)]	RW	32	0x0000 0200 + (0x20 * j)	0x4902 C200 + (0x20 * j)	0x4012 C200 + (0x20 * j)	0x2 C200 + (0x20 * j)
SLIMBUS_DCT_FIFO_SETUP1_j [(2)]	RW	32	0x0000 0204 + (0x20 * j)	0x4902 C204 + (0x20 * j)	0x4012 C204 + (0x20 * j)	0x2 C204 + (0x20 * j)
SLIMBUS_DCT_FIFO_SETUP2_j [(2)]	RW	32	0x0000 0208 + (0x20 * j)	0x4902 C208 + (0x20 * j)	0x4012 C208 + (0x20 * j)	0x2 C208 + (0x20 * j)

(1) i = 0 to 6

(2) j = 0 to 7

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Table 23-692. SLIMBUS1 Register Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	Physical Address L3 Interconnect	Physical Address Cortex-A9 Private Access	Physical Address DSP Private Access
SLIMBUS_DCT_FIFO_STATUS_j (2)	RW	32	0x0000 020C + (0x20 * j)	0x4902 C20C + (0x20 * j)	0x4012 C20C + (0x20 * j)	0x2 C20C + (0x20 * j)
SLIMBUS_DCT_MAP_j (2)	RW	32	0x0000 0210 + (0x20 * j)	0x4902 C210 + (0x20 * j)	0x4012 C210 + (0x20 * j)	0x2 C210 + (0x20 * j)
SLIMBUS_DCT_CONFIG1_j (2)	RW	32	0x0000 0214 + (0x20 * j)	0x4902 C214 + (0x20 * j)	0x4012 C214 + (0x20 * j)	0x2 C214 + (0x20 * j)
SLIMBUS_DCT_CONFIG2_j (2)	RW	32	0x0000 0218 + (0x20 * j)	0x4902 C218 + (0x20 * j)	0x4012 C218 + (0x20 * j)	0x2 C218 + (0x20 * j)
SLIMBUS_DCT_DATA_j (2)	RW	32	0x0000 021C + (0x20 * j)	0x4902 C21C + (0x20 * j)	0x4012 C21C + (0x20 * j)	0x2 C21C + (0x20 * j)
SLIMBUS_DCR_INFO_j (2)	RW	32	0x0000 0300 + (0x20 * j)	0x4902 C300 + (0x20 * j)	0x4012 C300 + (0x20 * j)	0x2 C300 + (0x20 * j)
SLIMBUS_DCR_FIFO_SETUP1_j (2)	RW	32	0x0000 0304 + (0x20 * j)	0x4902 C304 + (0x20 * j)	0x4012 C304 + (0x20 * j)	0x2 C304 + (0x20 * j)
SLIMBUS_DCR_FIFO_SETUP2_j (2)	RW	32	0x0000 0308 + (0x20 * j)	0x4902 C308 + (0x20 * j)	0x4012 C308 + (0x20 * j)	0x2 C308 + (0x20 * j)
SLIMBUS_DCR_FIFO_STATUS_j (2)	RW	32	0x0000 030C + (0x20 * j)	0x4902 C30C + (0x20 * j)	0x4012 C30C + (0x20 * j)	0x2 C30C + (0x20 * j)
SLIMBUS_DCR_MAP_j (2)	RW	32	0x0000 0310 + (0x20 * j)	0x4902 C310 + (0x20 * j)	0x4012 C310 + (0x20 * j)	0x2 C310 + (0x20 * j)
SLIMBUS_DCR_CONFIG1_j (3)	RW	32	0x0000 0314 + (0x20 * j)	0x4902 C314 + (0x20 * j)	0x4012 C314 + (0x20 * j)	0x2 C314 + (0x20 * j)
SLIMBUS_DCR_CONFIG2_j (3)	RW	32	0x0000 0318 + (0x20 * j)	0x4902 C318 + (0x20 * j)	0x4012 C318 + (0x20 * j)	0x2 C318 + (0x20 * j)
SLIMBUS_DCR_DATA_j (3)	R	32	0x0000 031C + (0x20 * j)	0x4902 C31C + (0x20 * j)	0x4012 C31C + (0x20 * j)	0x2 C31C + (0x20 * j)

(3) j = 0 to 7

23.9.6.3.2 SLIMBUS2 Register Summary

Table 23-693. SLIMBUS2 Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	Physical Address L3 Interconnect
SLIMBUS_CMP_REVISION	R	32	0x0000 0000	0x4807 6000
SLIMBUS_CMP_HWINFO	R	32	0x0000 0004	0x4807 6004
SLIMBUS_CMP_SYSCONFIG	RW	32	0x0000 0010	0x4807 6010
RESERVED	RW	32	0x0000 0020	0x4807 6020
SLIMBUS_CMP_IRQSTATUS_RAW	RW	32	0x0000 0024	0x4807 6024
SLIMBUS_CMP_IRQSTATUS	RW	32	0x0000 0028	0x4807 6028
SLIMBUS_CMP_IRQENABLE_SET	RW	32	0x0000 002C	0x4807 602C
SLIMBUS_CMP_IRQENABLE_CLR	RW	32	0x0000 0030	0x4807 6030
SLIMBUS_CMP_DMAENABLE_SET	RW	32	0x0000 0034	0x4807 6034
SLIMBUS_CMP_DMAENABLE_CLR	RW	32	0x0000 0038	0x4807 6038
SLIMBUS_CMP_IV	RW	32	0x0000 0040	0x4807 6040
SLIMBUS_CMP_MI_PC	RW	32	0x0000 0044	0x4807 6044
SLIMBUS_SMT_INFO	RW	32	0x0000 0050	0x4807 6050
SLIMBUS_SMT_MESSAGE	RW	32	0x0000 0054	0x4807 6054
SLIMBUS_SMT_CONTROL	RW	32	0x0000 0058	0x4807 6058
SLIMBUS_SMT_FIFO_SETUP	RW	32	0x0000 005C	0x4807 605C

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Table 23-693. SLIMBUS2 Register Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	Physical Address L3 Interconnect
SLIMBUS_SMR_INFO	RW	32	0x0000 0060	0x4807 6060
SLIMBUS_SMR_MESSAGE	R	32	0x0000 0064	0x4807 6064
SLIMBUS_SMR_CONTROL	RW	32	0x0000 0068	0x4807 6068
SLIMBUS_SMR_FIFO_SETUP	RW	32	0x0000 006C	0x4807 606C
SLIMBUS_FL_INFO	RW	32	0x0000 0070	0x4807 6070
SLIMBUS_FL_CONTROL	RW	32	0x0000 0074	0x4807 6074
SLIMBUS_FL_SM	RW	32	0x0000 0078	0x4807 6078
SLIMBUS_FL_CG	RW	32	0x0000 007C	0x4807 607C
SLIMBUS_FL_RF	RW	32	0x0000 0080	0x4807 6080
SLIMBUS_FR_INFO	RW	32	0x0000 0090	0x4807 6090
SLIMBUS_FR_CLOCK_SOURCE	RW	32	0x0000 0094	0x4807 6094
SLIMBUS_FR_CONTROL	RW	32	0x0000 0098	0x4807 6098
SLIMBUS_FR_FRAMER_HANDOVER	RW	32	0x0000 009C	0x4807 609C
SLIMBUS_FR_CLOCK_PAUSE	RW	32	0x0000 00A0	0x4807 60A0
SLIMBUS_DEV_LA_i (1)	RW	32	0x0000 0100 + (0x10 * i)	0x4807 6100 + (0x10 * i)
SLIMBUS_DEV_EA_LO_i (1)	R	32	0x0000 0104 + (0x10 * i)	0x4807 6104 + (0x10 * i)
SLIMBUS_DEV_EA_HI_i (1)	R	32	0x0000 0108 + (0x10 * i)	0x4807 6108 + (0x10 * i)
SLIMBUS_DCT_INFO_j (2)	RW	32	0x0000 0200 + (0x20 * j)	0x4807 6200 + (0x20 * j)
SLIMBUS_DCT_FIFO_SETUP1_j (2)	RW	32	0x0000 0204 + (0x20 * j)	0x4807 6204 + (0x20 * j)
SLIMBUS_DCT_FIFO_SETUP2_j (2)	RW	32	0x0000 0208 + (0x20 * j)	0x4807 6208 + (0x20 * j)
SLIMBUS_DCT_FIFO_STATUS_j (2)	RW	32	0x0000 020C + (0x20 * j)	0x4807 620C + (0x20 * j)
SLIMBUS_DCT_MAP_j (2)	RW	32	0x0000 0210 + (0x20 * j)	0x4807 6210 + (0x20 * j)
SLIMBUS_DCT_CONFIG1_j (2)	RW	32	0x0000 0214 + (0x20 * j)	0x4807 6214 + (0x20 * j)
SLIMBUS_DCT_CONFIG2_j (2)	RW	32	0x0000 0218 + (0x20 * j)	0x4807 6218 + (0x20 * j)
SLIMBUS_DCT_DATA_j (2)	RW	32	0x0000 021C + (0x20 * j)	0x4807 621C + (0x20 * j)
SLIMBUS_DCR_INFO_j (2)	RW	32	0x0000 0280 + (0x20 * j)	0x4807 6280 + (0x20 * j)
SLIMBUS_DCR_FIFO_SETUP1_j (2)	RW	32	0x0000 0284 + (0x20 * j)	0x4807 6284 + (0x20 * j)
SLIMBUS_DCR_FIFO_SETUP2_j (2)	RW	32	0x0000 0288 + (0x20 * j)	0x4807 6288 + (0x20 * j)
SLIMBUS_DCR_FIFO_STATUS_j (2)	RW	32	0x0000 028C + (0x20 * j)	0x4807 628C + (0x20 * j)
SLIMBUS_DCR_MAP_j (2)	RW	32	0x0000 0290 + (0x20 * j)	0x4807 6290 + (0x20 * j)
SLIMBUS_DCR_CONFIG1_j (2)	RW	32	0x0000 0294 + (0x20 * j)	0x4807 6294 + (0x20 * j)
SLIMBUS_DCR_CONFIG2_j (2)	RW	32	0x0000 0298 + (0x20 * j)	0x4807 6298 + (0x20 * j)
SLIMBUS_DCR_DATA_j (2)	R	32	0x0000 029C + (0x20 * j)	0x4807 629C + (0x20 * j)

(1) i = 0 to 6
(2) j = 0 to 3

23.9.6.3.3 SLIMbus Register Descriptions

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Table 23-694. SLIMBUS_CMP_REVISION

Address Offset	0x0000 0000		
Physical Address	0x4902 C000 0x4012 C000 0x2 C000 0x4807 6000	**Instance**	SLIMBUS1_L3 SLIMBUS1_CORTEX-A9 SLIMBUS1_DSP SLIMBUS2_L3
Description	IP Revision Identifier Used by software to track features, bugs, and compatibility		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	Revision Number	R	0x---- ----[1]

(1) TI internal data.

Table 23-695. Register Call Summary for Register SLIMBUS_CMP_REVISION

Serial Low-Power Inter-Chip Media Bus Controller

- SLIMBUS1 Register Summary: [0]
- SLIMBUS2 Register Summary: [1]

Table 23-696. SLIMBUS_CMP_HWINFO

Address Offset	0x0000 0004		
Physical Address	0x4902 C004 0x4012 C004 0x2 C004 0x4807 6004	**Instance**	SLIMBUS1_L3 SLIMBUS1_CORTEX-A9 SLIMBUS1_DSP SLIMBUS2_L3
Description	Those read-only, hardcoded fields display the values of the eponymous hardware configuration depending on module instantiation - SLIMBUS1 or SLIMBUS2.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DEV				TDC				RDC				RRSZ				TRSZ								PSZ							

Bits	Field Name	Description	Type	Reset
31:28	DEV	Device count: number of devices supported by the component, most notably through the automatically reception of the messages addressed to them. Sets the number of instances of the "DEV_XYZ" registers.	R	0x7
27:24	TDC	Transmit Data agent Count: Number of transmit hardware data agents (FIFO and associated logic) Sets the number of instances of the "DCT_XYZ" registers.	R	SeeTable 23-698
23:20	RDC	Receive Data agent Count: Number of receive hardware data agents (FIFO and associated logic) Sets the number of instances of the "DCR_XYZ" registers.	R	SeeTable 23-698
19:12	RRSZ	Size of receive FIFO RAM, in 32-bit words. RX message FIFO and all RX data FIFOs map to that shared RAM.	R	SeeTable 23-698
11:4	TRSZ	Size of transmit FIFO RAM, in 32-bit words. TX message FIFO and all TX data FIFOs map to that shared RAM.	R	SeeTable 23-698

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Bits	Field Name	Description	Type	Reset
3:0	PSZ	Size of (both TX and RX) FIFO segment word pointers, in bits. Determines the maximum number of (variable-sized) segment words a data agent FIFO can contain. Sets the width of FIFO control and status fields: size, threshold, level.	R	0x8

Table 23-697. Register Call Summary for Register SLIMBUS_CMP_HWINFO

Serial Low-Power Inter-Chip Media Bus Controller

- FIFO Management: [0] [1]
- SLIMBUS1 Register Summary: [2]
- SLIMBUS2 Register Summary: [3]

Table 23-698. Reset values for SLIMBUS_CMP_HWINFO

	TDC	RDC	RRSZ	TRSZ
SLIMBUS1	0x8	0x8	0x38	0x38
SLIMBUS2	0x4	0x4	0x80	0x80

Table 23-699. SLIMBUS_CMP_SYSCONFIG

Address Offset	0x0000 0010		
Physical Address	0x4902 C010 0x4012 C010 0x2 C010 0x4807 6010	**Instance**	SLIMBUS1_L3 SLIMBUS1_CORTEX-A9 SLIMBUS1_DSP SLIMBUS2_L3
Description	This register allows controlling various parameters of the interconnect interface		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							AUTOGATINGDISABLE	RESERVED				IDLEMODE		RESERVED	SOFTRESET

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	AUTOGATINGDISABLE	Control of the internal clock autogating for safety / debug only. No impact on module functionality, only on dynamic power. 0x0: Internal clocks are gated off when unused, power is optimized. 0x1: Internal clocks are free-running, maximum dynamic power.	RW	0
7:4	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
3:2	IDLEMODE	Configuration of the local target state management mode. By definition, target can handle read/write transaction as long as it is out of IDLE state. 0x0: Force-idle mode: local target's idle state follows (acknowledges) the system's idle requests unconditionally, that is, regardless of the IP module's internal requirements. Backup mode, for debug only. 0x1: No-idle mode: local target never enters idle state. Backup mode, for debug only. 0x3: Smart-idle wakeup-capable mode: local target's idle state eventually follows (acknowledges) the system's idle requests, depending on the IP module's internal requirements. IP module may generate (IRQ- or DMA-request-related) wakeup events when in idle state. Mode is only relevant if the appropriate IP module "swakeup" output(s) is (are) implemented. 0x2: Smart-idle mode: local target's idle state eventually follows (acknowledges) the system's idle requests, depending on the IP module's internal requirements. IP module shall not generate (IRQ- or DMA-request-related) wakeup events.	RW	0x2
1	RESERVED		R	0
0	SOFTRESET	Software reset. (Optional) Write 0x0: No action Write 0x1: Initiate software reset Read 0x1: Reset (software or other) ongoing Read 0x0: Reset done, no pending action	RW	0

Table 23-700. Register Call Summary for Register SLIMBUS_CMP_SYSCONFIG

Serial Low-Power Inter-Chip Media Bus Controller

- Software Reset: [0]
- Power Management: [1] [2]
- Global Initialization: [3] [4] [5] [6]
- SLIMBUS1 Register Summary: [7]
- SLIMBUS2 Register Summary: [8]

Table 23-701. SLIMBUS_CMP_IRQSTATUS_RAW

Address Offset	0x0000 0024		
Physical Address	0x4902 C024 0x4012 C024 0x2 C024 0x4807 6024	**Instance**	SLIMBUS1_L3 SLIMBUS1_CORTEX-A9 SLIMBUS1_DSP SLIMBUS2_L3
Description	Component (that is, main) interrupt request status. Check the corresponding secondary status register. Raw status is set even if event is not enabled. Write 1 to set the (raw) status, mostly for debug.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												DCR_INFO_7	DCR_INFO_6	DCR_INFO_5	DCR_INFO_4	DCR_INFO_3	DCR_INFO_2	DCR_INFO_1	DCR_INFO_0	DCT_INFO_7	DCT_INFO_6	DCT_INFO_5	DCT_INFO_4	DCT_INFO_3	DCT_INFO_2	DCT_INFO_1	DCT_INFO_0	SMR_INFO	SMT_INFO	FR_INFO	FL_INFO

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Bits	Field Name	Description	Type	Reset
31:20	RESERVED		R	0x000
19	DCR_INFO_7[1]	IRQ status for RX Data agent 7[1] If implemented: Write 0x0: No action Write 0x1: Trigger IRQ event by software Read 0x1: IRQ event pending Read 0x0: No event pending	RW W1toSet	0
18	DCR_INFO_6[1]	IRQ status for RX Data agent 6[1] If implemented: Write 0x0: No action Write 0x1: Trigger IRQ event by software Read 0x1: IRQ event pending Read 0x0: No event pending	RW W1toSet	0
17	DCR_INFO_5[1]	IRQ status for RX Data agent 5[1] If implemented: Write 0x0: No action Write 0x1: Trigger IRQ event by software Read 0x1: IRQ event pending Read 0x0: No event pending	RW W1toSet	0
16	DCR_INFO_4[1]	IRQ status for RX Data agent 4[1] If implemented: Write 0x0: No action Write 0x1: Trigger IRQ event by software Read 0x1: IRQ event pending Read 0x0: No event pending	RW W1toSet	0
15	DCR_INFO_3[1]	IRQ status for RX Data agent 3[1] If implemented: Write 0x0: No action Write 0x1: Trigger IRQ event by software Read 0x1: IRQ event pending Read 0x0: No event pending	RW W1toSet	0
14	DCR_INFO_2[1]	IRQ status for RX Data agent 2[1] If implemented: Write 0x0: No action Write 0x1: Trigger IRQ event by software Read 0x1: IRQ event pending Read 0x0: No event pending	RW W1toSet	0
13	DCR_INFO_1[1]	IRQ status for RX Data agent 1[1] If implemented: Write 0x0: No action Write 0x1: Trigger IRQ event by software Read 0x1: IRQ event pending Read 0x0: No event pending	RW W1toSet	0
12	DCR_INFO_0[1]	IRQ status for RX Data agent 0[1] If implemented: Write 0x0: No action Write 0x1: Trigger IRQ event by software Read 0x1: IRQ event pending Read 0x0: No event pending	RW W1toSet	0
11	DCT_INFO_7[2]	IRQ status for TX Data agent 7[2] Write 0x0: No action Write 0x1: Trigger IRQ event by software Read 0x1: IRQ event pending Read 0x0: No event pending	RW W1toSet	0

(1) This bit field is RESERVED in SLIMBUS2
(2) This bit field is DCR_INFO_3 (IRQ status for RX Data agent 3) in SLIMBUS2

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Bits	Field Name	Description	Type	Reset
10	DCT_INFO_6[3]	IRQ status for TX Data agent 6[3] Write 0x0: No action Write 0x1: Trigger IRQ event by software Read 0x1: IRQ event pending Read 0x0: No event pending	RW W1toSet	0
9	DCT_INFO_5[4]	IRQ status for TX Data agent 5[4] Write 0x0: No action Write 0x1: Trigger IRQ event by software Read 0x1: IRQ event pending Read 0x0: No event pending	RW W1toSet	0
8	DCT_INFO_4[5]	IRQ status for TX Data agent 4[5] Write 0x0: No action Write 0x1: Trigger IRQ event by software Read 0x1: IRQ event pending Read 0x0: No event pending	RW W1toSet	0
7	DCT_INFO_3	IRQ status for TX Data agent 3 Write 0x0: No action Write 0x1: Trigger IRQ event by software Read 0x1: IRQ event pending Read 0x0: No event pending	RW W1toSet	0
6	DCT_INFO_2	IRQ status for TX Data agent 2 Write 0x0: No action Write 0x1: Trigger IRQ event by software Read 0x1: IRQ event pending Read 0x0: No event pending	RW W1toSet	0
5	DCT_INFO_1	IRQ status for TX Data agent 1 Write 0x0: No action Write 0x1: Trigger IRQ event by software Read 0x1: IRQ event pending Read 0x0: No event pending	RW W1toSet	0
4	DCT_INFO_0	IRQ status for TX Data agent 0 Write 0x0: No action Write 0x1: Trigger IRQ event by software Read 0x1: IRQ event pending Read 0x0: No event pending	RW W1toSet	0
3	SMR_INFO	IRQ status for message receive Write 0x0: No action Write 0x1: Trigger IRQ event by software Read 0x1: IRQ event pending Read 0x0: No event pending	RW W1toSet	0
2	SMT_INFO	IRQ status for message transmit Write 0x0: No action Write 0x1: Trigger IRQ event by software Read 0x1: IRQ event pending Read 0x0: No event pending	RW W1toSet	0

(3) This bit field is DCR_INFO_2 (IRQ status for RX Data agent 2) in SLIMBUS2
(4) This bit field is DCR_INFO_1 (IRQ status for RX Data agent 1) in SLIMBUS2
(5) This bit field is DCR_INFO_0 (IRQ status for RX Data agent 0) in SLIMBUS2

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Bits	Field Name	Description	Type	Reset
1	FR_INFO	IRQ status for Framer device, when active Write 0x0: No action Write 0x1: Trigger IRQ event by software Read 0x1: IRQ event pending Read 0x0: No event pending	RW W1toSet	0
0	FL_INFO	IRQ status for Frame Layer Write 0x0: No action Write 0x1: Trigger IRQ event by software Read 0x1: IRQ event pending Read 0x0: No event pending	RW W1toSet	0

Table 23-702. Register Call Summary for Register SLIMBUS_CMP_IRQSTATUS_RAW

Serial Low-Power Inter-Chip Media Bus Controller

- Interrupt Requests: [0]
- SLIMBUS1 Register Summary: [1]
- SLIMBUS2 Register Summary: [2]

Table 23-703. SLIMBUS_CMP_IRQSTATUS

Address Offset	0x0000 0028		
Physical Address	0x4902 C028 0x4012 C028 0x2 C028 0x4807 6028	**Instance**	SLIMBUS1_L3 SLIMBUS1_CORTEX-A9 SLIMBUS1_DSP SLIMBUS2_L3
Description	Component (that is, main) interrupt request status. Check the corresponding secondary status register. Enabled status isn't set unless event is enabled. Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, that is, even if not enabled).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												DCR_INFO_7	DCR_INFO_6	DCR_INFO_5	DCR_INFO_4	DCR_INFO_3	DCR_INFO_2	DCR_INFO_1	DCR_INFO_0	DCT_INFO_7	DCT_INFO_6	DCT_INFO_5	DCT_INFO_4	DCT_INFO_3	DCT_INFO_2	DCT_INFO_1	DCT_INFO_0	SMR_INFO	SMT_INFO	FR_INFO	FL_INFO

Bits	Field Name	Description	Type	Reset
31:20	RESERVED		R	0x000
19	DCR_INFO_7[1]	IRQ status for RX Data agent 7[1]. If implemented: Write 0x0: No action Write 0x1: Clear pending event, if any Read 0x1: IRQ event pending Read 0x0: No event pending	RW W1toClr	0
18	DCR_INFO_6[1]	IRQ status for RX Data agent 6[1]. If implemented: Write 0x0: No action Write 0x1: Clear pending event, if any Read 0x1: IRQ event pending Read 0x0: No event pending	RW W1toClr	0

(1) This bit field is RESERVED in SLIMBUS2

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Bits	Field Name	Description	Type	Reset
17	DCR_INFO_5[1]	IRQ status for RX Data agent 5[1] . If implemented: Write 0x0: No action Write 0x1: Clear pending event, if any Read 0x1: IRQ event pending Read 0x0: No event pending	RW W1toClr	0
16	DCR_INFO_4[1]	IRQ status for RX Data agent 4[1] . If implemented: Write 0x0: No action Write 0x1: Clear pending event, if any Read 0x1: IRQ event pending Read 0x0: No event pending	RW W1toClr	0
15	DCR_INFO_3[1]	IRQ status for RX Data agent 3[1] . If implemented: Write 0x0: No action Write 0x1: Clear pending event, if any Read 0x1: IRQ event pending Read 0x0: No event pending	RW W1toClr	0
14	DCR_INFO_2[2]	IRQ status for RX Data agent 2[2] . If implemented: Write 0x0: No action Write 0x1: Clear pending event, if any Read 0x1: IRQ event pending Read 0x0: No event pending	RW W1toClr	0
13	DCR_INFO_1[2]	IRQ status for RX Data agent 1[2] . If implemented: Write 0x0: No action Write 0x1: Clear pending event, if any Read 0x1: IRQ event pending Read 0x0: No event pending	RW W1toClr	0
12	DCR_INFO_0[2]	IRQ status for RX Data agent 0[2] . If implemented: Write 0x0: No action Write 0x1: Clear pending event, if any Read 0x1: IRQ event pending Read 0x0: No event pending	RW W1toClr	0
11	DCT_INFO_7[3]	IRQ status for TX Data agent 7[3] Write 0x0: No action Write 0x1: Clear pending event, if any Read 0x1: IRQ event pending Read 0x0: No event pending	RW W1toClr	0
10	DCT_INFO_6[4]	IRQ status for TX Data agent 6[4] Write 0x0: No action Write 0x1: Clear pending event, if any Read 0x1: IRQ event pending Read 0x0: No event pending	RW W1toClr	0
9	DCT_INFO_5[5]	IRQ status for TX Data agent 5[5] Write 0x0: No action Write 0x1: Clear pending event, if any Read 0x1: IRQ event pending Read 0x0: No event pending	RW W1toClr	0

(2) This bit field is RESERVED in SLIMBUS2
(3) This bit field is DCR_INFO_3 (IRQ status for RX Data agent 3) in SLIMBUS2
(4) This bit field is DCR_INFO_2 (IRQ status for RX Data agent 2) in SLIMBUS2
(5) This bit field is DCR_INFO_1 (IRQ status for RX Data agent 1) in SLIMBUS2

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Bits	Field Name	Description	Type	Reset
8	DCT_INFO_4[6]	IRQ status for TX Data agent 4[6] Write 0x0: No action Write 0x1: Clear pending event, if any Read 0x1: IRQ event pending Read 0x0: No event pending	RW W1toClr	0
7	DCT_INFO_3	IRQ status for TX Data agent 3 Write 0x0: No action Write 0x1: Clear pending event, if any Read 0x1: IRQ event pending Read 0x0: No event pending	RW W1toClr	0
6	DCT_INFO_2	IRQ status for TX Data agent 2 Write 0x0: No action Write 0x1: Clear pending event, if any Read 0x1: IRQ event pending Read 0x0: No event pending	RW W1toClr	0
5	DCT_INFO_1	IRQ status for TX Data agent 1 Write 0x0: No action Write 0x1: Clear pending event, if any Read 0x1: IRQ event pending Read 0x0: No event pending	RW W1toClr	0
4	DCT_INFO_0	IRQ status for TX Data agent 0 Write 0x0: No action Write 0x1: Clear pending event, if any Read 0x1: IRQ event pending Read 0x0: No event pending	RW W1toClr	0
3	SMR_INFO	IRQ status for message receive Write 0x0: No action Write 0x1: Clear pending event, if any Read 0x1: IRQ event pending Read 0x0: No event pending	RW W1toClr	0
2	SMT_INFO	IRQ status for message transmit Write 0x0: No action Write 0x1: Clear pending event, if any Read 0x1: IRQ event pending Read 0x0: No event pending	RW W1toClr	0
1	FR_INFO	IRQ status for Framer device, when active Write 0x0: No action Write 0x1: Clear pending event, if any Read 0x1: IRQ event pending Read 0x0: No event pending	RW W1toClr	0
0	FL_INFO	IRQ status for Frame Layer Write 0x0: No action Write 0x1: Clear pending event, if any Read 0x1: IRQ event pending Read 0x0: No event pending	RW W1toClr	0

(6) This bit field is DCR_INFO_0 (IRQ status for RX Data agent 0) in SLIMBUS2

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Table 23-704. Register Call Summary for Register SLIMBUS_CMP_IRQSTATUS

Serial Low-Power Inter-Chip Media Bus Controller

- Transmission: [0] [1]
- Message reception: [2]
- Interrupt Service Routines: [3]
- Interrupt Requests: [4]
- Interface Device ISRs: [5]
- Framer Device ISRs: [6]
- Shared Message Channel Transmit ISRs: [7]
- Shared Message Channel Receive ISRs: [8]
- Data Channel Port ISRs: [9]
- SLIMbus Transfer Procedures: [10] [11] [12] [13] [14] [15] [16]
- SLIMBUS1 Register Summary: [17]
- SLIMBUS2 Register Summary: [18]

Table 23-705. SLIMBUS_CMP_IRQENABLE_SET

Address Offset	0x0000 002C		
Physical Address	0x4902 C02C 0x4012 C02C 0x2 C02C 0x4807 602C	**Instance**	SLIMBUS1_L3 SLIMBUS1_CORTEX-A9 SLIMBUS1_DSP SLIMBUS2_L3
Description	Component (that is, main) interrupt request enable Write 1 to set (enable interrupt). Readout equal to corresponding _CLR register.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												DCR_INFO_7_EN	DCR_INFO_6_EN	DCR_INFO_5_EN	DCR_INFO_4_EN	DCR_INFO_3_EN	DCR_INFO_2_EN	DCR_INFO_1_EN	DCR_INFO_0_EN	DCT_INFO_7_E7	DCT_INFO_6_EN	DCT_INFO_5_EN	DCT_INFO_4_EN	DCT_INFO_3_EN	DCT_INFO_2_EN	DCT_INFO_1_EN	DCT_INFO_0_EN	SMR_INFO_EN	SMT_INFO_EN	FR_INFO_EN	FL_INFO_EN

Bits	Field Name	Description	Type	Reset
31:20	RESERVED		R	0x000
19	DCR_INFO_7_EN[1]	IRQ enable for RX Data agent 7[1]. If implemented: Write 0x0: No action Write 0x1: Set IRQ enable (that is, enable event) Read 0x1: IRQ event is enabled Read 0x0: IRQ event is disabled	RW W1toSet	0
18	DCR_INFO_6_EN[1]	IRQ enable for RX Data agent 6[1]. If implemented: Write 0x0: No action Write 0x1: Set IRQ enable (that is, enable event) Read 0x1: IRQ event is enabled Read 0x0: IRQ event is disabled	RW W1toSet	0
17	DCR_INFO_5_EN[1]	IRQ enable for RX Data agent 5[1]. If implemented: Write 0x0: No action Write 0x1: Set IRQ enable (that is, enable event) Read 0x1: IRQ event is enabled Read 0x0: IRQ event is disabled	RW W1toSet	0

(1) This bit field is RESERVED in SLIMBUS2

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Bits	Field Name	Description	Type	Reset
16	DCR_INFO_4_EN[1]	IRQ enable for RX Data agent 4[1]. If implemented: Write 0x0: No action Write 0x1: Set IRQ enable (that is, enable event) Read 0x1: IRQ event is enabled Read 0x0: IRQ event is disabled	RW W1toSet	0
15	DCR_INFO_3_EN[1]	IRQ enable for RX Data agent 3[1]. If implemented: Write 0x0: No action Write 0x1: Set IRQ enable (that is, enable event) Read 0x1: IRQ event is enabled Read 0x0: IRQ event is disabled	RW W1toSet	0
14	DCR_INFO_2_EN[1]	IRQ enable for RX Data agent 2[1]. If implemented: Write 0x0: No action Write 0x1: Set IRQ enable (that is, enable event) Read 0x1: IRQ event is enabled Read 0x0: IRQ event is disabled	RW W1toSet	0
13	DCR_INFO_1_EN[2]	IRQ enable for RX Data agent 1[2]. If implemented: Write 0x0: No action Write 0x1: Set IRQ enable (that is, enable event) Read 0x1: IRQ event is enabled Read 0x0: IRQ event is disabled	RW W1toSet	0
12	DCR_INFO_0_EN[2]	IRQ enable for RX Data agent 0[2]. If implemented: Write 0x0: No action Write 0x1: Set IRQ enable (that is, enable event) Read 0x1: IRQ event is enabled Read 0x0: IRQ event is disabled	RW W1toSet	0
11	DCT_INFO_7_EN[3]	IRQ enable for TX Data agent 7[3] Write 0x0: No action Write 0x1: Set IRQ enable (that is, enable event) Read 0x1: IRQ event is enabled Read 0x0: IRQ event is disabled	RW W1toSet	0
10	DCT_INFO_6_EN[4]	IRQ enable for TX Data agent 6[4] Write 0x0: No action Write 0x1: Set IRQ enable (that is, enable event) Read 0x1: IRQ event is enabled Read 0x0: IRQ event is disabled	RW W1toSet	0
9	DCT_INFO_5_EN[5]	IRQ enable for TX Data agent 5[5] Write 0x0: No action Write 0x1: Set IRQ enable (that is, enable event) Read 0x1: IRQ event is enabled Read 0x0: IRQ event is disabled	RW W1toSet	0
8	DCT_INFO_4_EN[6]	IRQ enable for TX Data agent 4[6] Write 0x0: No action Write 0x1: Set IRQ enable (that is, enable event) Read 0x1: IRQ event is enabled Read 0x0: IRQ event is disabled	RW W1toSet	0

(2) This bit field is RESERVED in SLIMBUS2
(3) This bit field is DCR_INFO_3_EN (IRQ enable for RX Data agent 3) in SLIMBUS2
(4) This bit field is DCR_INFO_2_EN (IRQ enable for RX Data agent 2) in SLIMBUS2
(5) This bit field is DCR_INFO_1_EN (IRQ enable for RX Data agent 1) in SLIMBUS2
(6) This bit field is DCR_INFO_0_EN (IRQ enable for RX Data agent 0) in SLIMBUS2

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Bits	Field Name	Description	Type	Reset
7	DCT_INFO_3_EN	IRQ enable for TX Data agent 3 Write 0x0: No action Write 0x1: Set IRQ enable (that is, enable event) Read 0x1: IRQ event is enabled Read 0x0: IRQ event is disabled	RW W1toSet	0
6	DCT_INFO_2_EN	IRQ enable for TX Data agent 2 Write 0x0: No action Write 0x1: Set IRQ enable (that is, enable event) Read 0x1: IRQ event is enabled Read 0x0: IRQ event is disabled	RW W1toSet	0
5	DCT_INFO_1_EN	IRQ enable for TX Data agent 1 Write 0x0: No action Write 0x1: Set IRQ enable (that is, enable event) Read 0x1: IRQ event is enabled Read 0x0: IRQ event is disabled	RW W1toSet	0
4	DCT_INFO_0_EN	IRQ enable for TX Data agent 0 Write 0x0: No action Write 0x1: Set IRQ enable (that is, enable event) Read 0x1: IRQ event is enabled Read 0x0: IRQ event is disabled	RW W1toSet	0
3	SMR_INFO_EN	IRQ enable for message receive Write 0x0: No action Write 0x1: Set IRQ enable (that is, enable event) Read 0x1: IRQ event is enabled Read 0x0: IRQ event is disabled	RW W1toSet	0
2	SMT_INFO_EN	IRQ enable for message transmit Write 0x0: No action Write 0x1: Set IRQ enable (that is, enable event) Read 0x1: IRQ event is enabled Read 0x0: IRQ event is disabled	RW W1toSet	0
1	FR_INFO_EN	IRQ enable for Framer device, when active Write 0x0: No action Write 0x1: Set IRQ enable (that is, enable event) Read 0x1: IRQ event is enabled Read 0x0: IRQ event is disabled	RW W1toSet	0
0	FL_INFO_EN	IRQ enable for Frame Layer Write 0x0: No action Write 0x1: Set IRQ enable (that is, enable event) Read 0x1: IRQ event is enabled Read 0x0: IRQ event is disabled	RW W1toSet	0

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Table 23-706. Register Call Summary for Register SLIMBUS_CMP_IRQENABLE_SET

Serial Low-Power Inter-Chip Media Bus Controller

- Transmission: [0] [1]
- Message reception: [2]
- Interrupt Service Routines: [3]
- Interrupt Requests: [4]
- Interface Device ISRs: [5]
- Framer Device ISRs: [6]
- Shared Message Channel Transmit ISRs: [7]
- Shared Message Channel Receive ISRs: [8]
- Data Channel Port ISRs: [9]
- SLIMbus Transfer Procedures: [10] [11] [12] [13]
- SLIMBUS1 Register Summary: [14]
- SLIMBUS2 Register Summary: [15]

Table 23-707. SLIMBUS_CMP_IRQENABLE_CLR

Address Offset	0x0000 0030		
Physical Address	0x4902 C030 0x4012 C030 0x2 C030 0x4807 6030	**Instance**	SLIMBUS1_L3 SLIMBUS1_CORTEX-A9 SLIMBUS1_DSP SLIMBUS2_L3
Description	Component (that is, main) interrupt request enable Write 1 to clear (disable interrupt). Readout equal to corresponding _SET register.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												DCR_INFO_7_EN	DCR_INFO_6_EN	DCR_INFO_5_EN	DCR_INFO_4_EN	DCR_INFO_3_EN	DCR_INFO_2_EN	DCR_INFO_1_EN	DCR_INFO_0_EN	DCT_INFO_7_E7	DCT_INFO_6_EN	DCT_INFO_5_EN	DCT_INFO_4_EN	DCT_INFO_3_EN	DCT_INFO_2_EN	DCT_INFO_1_EN	DCT_INFO_0_EN	SMR_INFO_EN	SMT_INFO_EN	FR_INFO_EN	FL_INFO_EN

Bits	Field Name	Description	Type	Reset
31:20	RESERVED		R	0x000
19	DCR_INFO_7_EN[1]	IRQ enable for RX data agent 7[1]. If implemented: Write 0x0: No action Write 0x1: Clear IRQ enable (that is, disable event) Read 0x1: IRQ event is enabled Read 0x0: IRQ event is disabled	RW W1toClr	0
18	DCR_INFO_6_EN[1]	IRQ enable for RX data agent 6[1]. If implemented: Write 0x0: No action Write 0x1: Clear IRQ enable (that is, disable event) Read 0x1: IRQ event is enabled Read 0x0: IRQ event is disabled	RW W1toClr	0
17	DCR_INFO_5_EN[1]	IRQ enable for RX data agent 5[1]. If implemented: Write 0x0: No action Write 0x1: Clear IRQ enable (that is, disable event) Read 0x1: IRQ event is enabled Read 0x0: IRQ event is disabled	RW W1toClr	0

(1) This bit field is RESERVED in SLIMBUS2

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Bits	Field Name	Description	Type	Reset
16	DCR_INFO_4_EN[1]	IRQ enable for RX data agent 4[1]. If implemented: Write 0x0: No action Write 0x1: Clear IRQ enable (that is, disable event) Read 0x1: IRQ event is enabled Read 0x0: IRQ event is disabled	RW W1toClr	0
15	DCR_INFO_3_EN[1]	IRQ enable for RX data agent 3[1]. If implemented: Write 0x0: No action Write 0x1: Clear IRQ enable (that is, disable event) Read 0x1: IRQ event is enabled Read 0x0: IRQ event is disabled	RW W1toClr	0
14	DCR_INFO_2_EN[1]	IRQ enable for RX data agent 2[1]. If implemented: Write 0x0: No action Write 0x1: Clear IRQ enable (that is, disable event) Read 0x1: IRQ event is enabled Read 0x0: IRQ event is disabled	RW W1toClr	0
13	DCR_INFO_1_EN[2]	IRQ enable for RX data agent 1[2]. If implemented: Write 0x0: No action Write 0x1: Clear IRQ enable (that is, disable event) Read 0x1: IRQ event is enabled Read 0x0: IRQ event is disabled	RW W1toClr	0
12	DCR_INFO_0_EN[2]	IRQ enable for RX data agent 0[2]. If implemented: Write 0x0: No action Write 0x1: Clear IRQ enable (that is, disable event) Read 0x1: IRQ event is enabled Read 0x0: IRQ event is disabled	RW W1toClr	0
11	DCT_INFO_7_EN[3]	IRQ enable for TX Data agent 7[3] Write 0x0: No action Write 0x1: Clear IRQ enable (that is, disable event) Read 0x1: IRQ event is enabled Read 0x0: IRQ event is disabled	RW W1toClr	0
10	DCT_INFO_6_EN[4]	IRQ enable for TX Data agent 6[4] Write 0x0: No action Write 0x1: Clear IRQ enable (that is, disable event) Read 0x1: IRQ event is enabled Read 0x0: IRQ event is disabled	RW W1toClr	0
9	DCT_INFO_5_EN[5]	IRQ enable for TX Data agent 5[5] Write 0x0: No action Write 0x1: Clear IRQ enable (that is, disable event) Read 0x1: IRQ event is enabled Read 0x0: IRQ event is disabled	RW W1toClr	0
8	DCT_INFO_4_EN[6]	IRQ enable for TX Data agent 4[6] Write 0x0: No action Write 0x1: Clear IRQ enable (that is, disable event) Read 0x1: IRQ event is enabled Read 0x0: IRQ event is disabled	RW W1toClr	0

(2) This bit field is RESERVED in SLIMBUS2
(3) This bit field is DCR_INFO_3_EN (IRQ enable for RX Data agent 3) in SLIMBUS2
(4) This bit field is DCR_INFO_2_EN (IRQ enable for RX Data agent 2) in SLIMBUS2
(5) This bit field is DCR_INFO_1_EN (IRQ enable for RX Data agent 1) in SLIMBUS2
(6) This bit field is DCR_INFO_0_EN (IRQ enable for RX Data agent 0) in SLIMBUS2

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Bits	Field Name	Description	Type	Reset
7	DCT_INFO_3_EN	IRQ enable for TX Data agent 3 Write 0x0: No action Write 0x1: Clear IRQ enable (that is, disable event) Read 0x1: IRQ event is enabled Read 0x0: IRQ event is disabled	RW W1toClr	0
6	DCT_INFO_2_EN	IRQ enable for TX Data agent 2 Write 0x0: No action Write 0x1: Clear IRQ enable (that is, disable event) Read 0x1: IRQ event is enabled Read 0x0: IRQ event is disabled	RW W1toClr	0
5	DCT_INFO_1_EN	IRQ enable for TX Data agent 1 Write 0x0: No action Write 0x1: Clear IRQ enable (that is, disable event) Read 0x1: IRQ event is enabled Read 0x0: IRQ event is disabled	RW W1toClr	0
4	DCT_INFO_0_EN	IRQ enable for TX Data agent 0 Write 0x0: No action Write 0x1: Clear IRQ enable (that is, disable event) Read 0x1: IRQ event is enabled Read 0x0: IRQ event is disabled	RW W1toClr	0
3	SMR_INFO_EN	IRQ enable for message receive Write 0x0: No action Write 0x1: Clear IRQ enable (that is, disable event) Read 0x1: IRQ event is enabled Read 0x0: IRQ event is disabled	RW W1toClr	0
2	SMT_INFO_EN	IRQ enable for message transmit Write 0x0: No action Write 0x1: Clear IRQ enable (that is, disable event) Read 0x1: IRQ event is enabled Read 0x0: IRQ event is disabled	RW W1toClr	0
1	FR_INFO_EN	IRQ enable for Framer device, when active Write 0x0: No action Write 0x1: Clear IRQ enable (that is, disable event) Read 0x1: IRQ event is enabled Read 0x0: IRQ event is disabled	RW W1toClr	0
0	FL_INFO_EN	IRQ enable for Frame Layer Write 0x0: No action Write 0x1: Clear IRQ enable (that is, disable event) Read 0x1: IRQ event is enabled Read 0x0: IRQ event is disabled	RW W1toClr	0

Table 23-708. Register Call Summary for Register SLIMBUS_CMP_IRQENABLE_CLR

Serial Low-Power Inter-Chip Media Bus Controller

- Interrupt Service Routines: [0]
- Interrupt Requests: [1]
- SLIMBUS1 Register Summary: [2]
- SLIMBUS2 Register Summary: [3]

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Table 23-709. SLIMBUS_CMP_DMAENABLE_SET

Address Offset	0x0000 0034		
Physical Address	0x4902 C034 0x4012 C034 0x2 C034 0x4807 6034	**Instance**	SLIMBUS1_L3 SLIMBUS1_CORTEX-A9 SLIMBUS1_DSP SLIMBUS2_L3
Description	Components DMA enable (1 bit per DMA-capable channel) Write 1 to set (enable DMA). Readout equal to corresponding _CLR register.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												DCR_DMA_7_EN	DCR_DMA_6_EN	DCR_DMA_5_EN	DCR_DMA_4_EN	DCR_DMA_3_EN	DCR_DMA_2_EN	DCR_DMA_1_EN	DCR_DMA_0_EN	DCT_DMA_7_EN	DCT_DMA_6_EN	DCT_DMA_5_EN	DCT_DMA_4_EN	DCT_DMA_3_EN	DCT_DMA_2_EN	DCT_DMA_1_EN	DCT_DMA_0_EN	RESERVED			

Bits	Field Name	Description	Type	Reset
31:20	RESERVED		R	0x000
19	DCR_DMA_7_EN[1]	DMA enable for RX Data agent 7[1] . If implemented: Write 0x0: No action Write 0x1: Set DMA enable (that is, enable channel) Read 0x1: DMA channel is enabled Read 0x0: DMA chanel is disabled	RW W1toSet.	0
18	DCR_DMA_6_EN[1]	DMA enable for RX Data agent 6[1] . If implemented: Write 0x0: No action Write 0x1: Set DMA enable (that is, enable channel) Read 0x1: DMA channel is enabled Read 0x0: DMA chanel is disabled	RW W1toSet.	0
17	DCR_DMA_5_EN[1]	DMA enable for RX Data agent 5[1] . If implemented: Write 0x0: No action Write 0x1: Set DMA enable (that is, enable channel) Read 0x1: DMA channel is enabled Read 0x0: DMA chanel is disabled	RW W1toSet.	0
16	DCR_DMA_4_EN[1]	DMA enable for RX Data agent 4[1] . If implemented: Write 0x0: No action Write 0x1: Set DMA enable (that is, enable channel) Read 0x1: DMA channel is enabled Read 0x0: DMA chanel is disabled	RW W1toSet.	0
15	DCR_DMA_3_EN[1]	DMA enable for RX Data agent 3[1] . If implemented: Write 0x0: No action Write 0x1: Set DMA enable (that is, enable channel) Read 0x1: DMA channel is enabled Read 0x0: DMA chanel is disabled	RW W1toSet.	0
14	DCR_DMA_2_EN[1]	DMA enable for RX Data agent 2[1] . If implemented: Write 0x0: No action Write 0x1: Set DMA enable (that is, enable channel) Read 0x1: DMA channel is enabled Read 0x0: DMA chanel is disabled	RW W1toSet.	0

(1) This bit field is RESERVED in SLIMBUS2

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Bits	Field Name	Description	Type	Reset
13	DCR_DMA_1_EN[1]	DMA enable for RX Data agent 1[1] . If implemented: Write 0x0: No action Write 0x1: Set DMA enable (that is, enable channel) Read 0x1: DMA channel is enabled Read 0x0: DMA chanel is disabled	RW W1toSet.	0
12	DCR_DMA_0_EN[1]	DMA enable for RX Data agent 0[1] . If implemented: Write 0x0: No action Write 0x1: Set DMA enable (that is, enable channel) Read 0x1: DMA channel is enabled Read 0x0: DMA chanel is disabled	RW W1toSet.	0
11	DCT_DMA_7_EN[2]	DMA enable for TX Data agent 7[2] Write 0x0: No action Write 0x1: Set DMA enable (that is, enable channel) Read 0x1: DMA channel is enabled Read 0x0: DMA chanel is disabled	RW W1toSet	0
10	DCT_DMA_6_EN[3]	DMA enable for TX Data agent 6[3] Write 0x0: No action Write 0x1: Set DMA enable (that is, enable channel) Read 0x1: DMA channel is enabled Read 0x0: DMA chanel is disabled	RW W1toSet	0
9	DCT_DMA_5_EN[4]	DMA enable for TX Data agent 5[4] Write 0x0: No action Write 0x1: Set DMA enable (that is, enable channel) Read 0x1: DMA channel is enabled Read 0x0: DMA chanel is disabled	RW W1toSet	0
8	DCT_DMA_4_EN[5]	DMA enable for TX Data agent 4[5] Write 0x0: No action Write 0x1: Set DMA enable (that is, enable channel) Read 0x1: DMA channel is enabled Read 0x0: DMA chanel is disabled	RW W1toSet	0
7	DCT_DMA_3_EN	DMA enable for TX Data agent 3 Write 0x0: No action Write 0x1: Set DMA enable (that is, enable channel) Read 0x1: DMA channel is enabled Read 0x0: DMA chanel is disabled	RW W1toSet	0
6	DCT_DMA_2_EN	DMA enable for TX Data agent 2 Write 0x0: No action Write 0x1: Set DMA enable (that is, enable channel) Read 0x1: DMA channel is enabled Read 0x0: DMA chanel is disabled	RW W1toSet	0
5	DCT_DMA_1_EN	DMA enable for TX Data agent 1 Write 0x0: No action Write 0x1: Set DMA enable (that is, enable channel) Read 0x1: DMA channel is enabled Read 0x0: DMA chanel is disabled	RW W1toSet	0

(2) This bit field is DCR_DMA_3_EN (DMA enable for RX Data agent 3) in SLIMBUS2
(3) This bit field is DCR_DMA_2_EN (DMA enable for RX Data agent 2) in SLIMBUS2
(4) This bit field is DCR_DMA_1_EN (DMA enable for RX Data agent 1) in SLIMBUS2
(5) This bit field is DCR_DMA_0_EN (DMA enable for RX Data agent 0) in SLIMBUS2

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Bits	Field Name	Description	Type	Reset
4	DCT_DMA_0_EN	DMA enable for TX Data agent 0 Write 0x0: No action Write 0x1: Set DMA enable (that is, enable channel) Read 0x1: DMA channel is enabled Read 0x0: DMA chanel is disabled	RW W1toSet	0
3:0	RESERVED		R	0x0

Table 23-710. Register Call Summary for Register SLIMBUS_CMP_DMAENABLE_SET

Serial Low-Power Inter-Chip Media Bus Controller

- Data Input/Output: DMA Request Mode: [0]
- SLIMbus Transfer Procedures: [1] [2]
- SLIMBUS1 Register Summary: [3]
- SLIMBUS2 Register Summary: [4]

Table 23-711. SLIMBUS_CMP_DMAENABLE_CLR

Address Offset	0x0000 0038		
Physical Address	0x4902 C038 0x4012 C038 0x2 C038 0x4807 6038	**Instance**	SLIMBUS1_L3 SLIMBUS1_CORTEX-A9 SLIMBUS1_DSP SLIMBUS2_L3
Description	Components DMA enable (1 bit per DMA-capable channel) Write 1 to clear (disable DMA). Readout equal to corresponding _SET register.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												DCR_DMA_7_EN	DCR_DMA_6_EN	DCR_DMA_5_EN	DCR_DMA_4_EN	DCR_DMA_3_EN	DCR_DMA_2_EN	DCR_DMA_1_EN	DCR_DMA_0_EN	DCT_DMA_7_EN	DCT_DMA_6_EN	DCT_DMA_5_EN	DCT_DMA_4_EN	DCT_DMA_3_EN	DCT_DMA_2_EN	DCT_DMA_1_EN	DCT_DMA_0_EN	RESERVED			

Bits	Field Name	Description	Type	Reset
31:20	RESERVED		R	0x000
19	DCR_DMA_7_EN[1]	DMA enable for RX Data agent 7[1] . If implemented: Write 0x0: No action Write 0x1: Clear DMA enable (that is, disable channel) Read 0x1: DMA channel is enabled Read 0x0: DMA chanel is disabled	RW W1toClr	0
18	DCR_DMA_6_EN[1]	DMA enable for RX Data agent 6[1] . If implemented: Write 0x0: No action Write 0x1: Clear DMA enable (that is, disable channel) Read 0x1: DMA channel is enabled Read 0x0: DMA chanel is disabled	RW W1toClr	0
17	DCR_DMA_5_EN[1]	DMA enable for RX Data agent 5[1] . If implemented: Write 0x0: No action Write 0x1: Clear DMA enable (that is, disable channel) Read 0x1: DMA channel is enabled Read 0x0: DMA chanel is disabled	RW W1toClr	0

(1) This bit field is RESERVED in SLIMBUS2

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Bits	Field Name	Description	Type	Reset
16	DCR_DMA_4_EN[1]	DMA enable for RX Data agent 4[1] . If implemented: Write 0x0: No action Write 0x1: Clear DMA enable (that is, disable channel) Read 0x1: DMA channel is enabled Read 0x0: DMA chanel is disabled	RW W1toClr	0
15	DCR_DMA_3_EN[1]	DMA enable for RX Data agent 3[1] . If implemented: Write 0x0: No action Write 0x1: Clear DMA enable (that is, disable channel) Read 0x1: DMA channel is enabled Read 0x0: DMA chanel is disabled	RW W1toClr	0
14	DCR_DMA_2_EN[1]	DMA enable for RX Data agent 2[1] . If implemented: Write 0x0: No action Write 0x1: Clear DMA enable (that is, disable channel) Read 0x1: DMA channel is enabled Read 0x0: DMA chanel is disabled	RW W1toClr	0
13	DCR_DMA_1_EN[2]	DMA enable for RX Data agent 1[2] . If implemented: Write 0x0: No action Write 0x1: Clear DMA enable (that is, disable channel) Read 0x1: DMA channel is enabled Read 0x0: DMA chanel is disabled	RW W1toClr	0
12	DCR_DMA_0_EN[2]	DMA enable for RX Data agent 0[2] . If implemented: Write 0x0: No action Write 0x1: Clear DMA enable (that is, disable channel) Read 0x1: DMA channel is enabled Read 0x0: DMA chanel is disabled	RW W1toClr	0
11	DCT_DMA_7_EN[3]	DMA enable for TX Data agent 7[3] Write 0x0: No action Write 0x1: Clear DMA enable (that is, disable channel) Read 0x1: DMA channel is enabled Read 0x0: DMA chanel is disabled	RW W1toClr	0
10	DCT_DMA_6_EN[4]	DMA enable for TX Data agent 6[4] Write 0x0: No action Write 0x1: Clear DMA enable (that is, disable channel) Read 0x1: DMA channel is enabled Read 0x0: DMA chanel is disabled	RW W1toClr	0
9	DCT_DMA_5_EN[5]	DMA enable for TX Data agent 5[5] Write 0x0: No action Write 0x1: Clear DMA enable (that is, disable channel) Read 0x1: DMA channel is enabled Read 0x0: DMA chanel is disabled	RW W1toClr	0
8	DCT_DMA_4_EN[6]	DMA enable for TX Data agent 4[6] Write 0x0: No action Write 0x1: Clear DMA enable (that is, disable channel) Read 0x1: DMA channel is enabled Read 0x0: DMA chanel is disabled	RW W1toClr	0

[2] This bit field is RESERVED in SLIMBUS2
[3] This bit field is DCR_DMA_3_EN (DMA enable for RX Data agent 3) in SLIMBUS2
[4] This bit field is DCR_DMA_2_EN (DMA enable for RX Data agent 2) in SLIMBUS2
[5] This bit field is DCR_DMA_1_EN (DMA enable for RX Data agent 1) in SLIMBUS2
[6] This bit field is DCR_DMA_0_EN (DMA enable for RX Data agent 0) in SLIMBUS2

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Bits	Field Name	Description	Type	Reset
7	DCT_DMA_3_EN	DMA enable for TX Data agent 3 Write 0x0: No action Write 0x1: Clear DMA enable (that is, disable channel) Read 0x1: DMA channel is enabled Read 0x0: DMA chanel is disabled	RW W1toClr	0
6	DCT_DMA_2_EN	DMA enable for TX Data agent 2 Write 0x0: No action Write 0x1: Clear DMA enable (that is, disable channel) Read 0x1: DMA channel is enabled Read 0x0: DMA chanel is disabled	RW W1toClr	0
5	DCT_DMA_1_EN	DMA enable for TX Data agent 1 Write 0x0: No action Write 0x1: Clear DMA enable (that is, disable channel) Read 0x1: DMA channel is enabled Read 0x0: DMA chanel is disabled	RW W1toClr	0
4	DCT_DMA_0_EN	DMA enable for TX Data agent 0 Write 0x0: No action Write 0x1: Clear DMA enable (that is, disable channel) Read 0x1: DMA channel is enabled Read 0x0: DMA chanel is disabled	RW W1toClr	0
3:0	RESERVED		R	0x0

Table 23-712. Register Call Summary for Register SLIMBUS_CMP_DMAENABLE_CLR

Serial Low-Power Inter-Chip Media Bus Controller

- Data Input/Output: DMA Request Mode: [0]
- SLIMBUS1 Register Summary: [1]
- SLIMBUS2 Register Summary: [2]

Table 23-713. SLIMBUS_CMP_IV

Address Offset	0x0000 0040		
Physical Address	0x4902 C040 0x4012 C040 0x2 C040 0x4807 6040	**Instance**	SLIMBUS1_L3 SLIMBUS1_CORTEX-A9 SLIMBUS1_DSP SLIMBUS2_L3
Description	Component IV field, used as lower 8 bits of the devices' Enumeration Address (EA[47:0]). Identical for all devices of the component.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								IV							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED		R	0x000000
7:0	IV	Device component's Instance Value (IV[7:0])	RW	0x00

Table 23-714. Register Call Summary for Register SLIMBUS_CMP_IV

Serial Low-Power Inter-Chip Media Bus Controller

- Device and Adressing Management: [0] [1]
- SLIMBUS1 Register Summary: [2]
- SLIMBUS2 Register Summary: [3]

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Table 23-715. SLIMBUS_CMP_MI_PC

Address Offset	0x0000 0044		
Physical Address	0x4902 C044 0x4012 C044 0x2 C044 0x4807 6044	**Instance**	SLIMBUS1_L3 SLIMBUS1_CORTEX-A9 SLIMBUS1_DSP SLIMBUS2_L3
Description	Component MI and PC fields, used as upper 32 bits of the devices' Enumeration Address (EA[47:0]). Identical for all devices of the component.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PC																MI															

Bits	Field Name	Description	Type	Reset
31:16	PC	Device component's Product Code (PC[15:0])	RW	0x0000
15:0	MI	Device component's Manufacturer Index (MI[15:0])	RW	0x0102

Table 23-716. Register Call Summary for Register SLIMBUS_CMP_MI_PC

Serial Low-Power Inter-Chip Media Bus Controller

- Device and Adressing Management: [0] [1] [2] [3]
- SLIMBUS1 Register Summary: [4]
- SLIMBUS2 Register Summary: [5]

Table 23-717. SLIMBUS_SMT_INFO

Address Offset	0x0000 0050		
Physical Address	0x4902 C050 0x4012 C050 0x2 C050 0x4807 6050	**Instance**	SLIMBUS1_L3 SLIMBUS1_CORTEX-A9 SLIMBUS1_DSP SLIMBUS2_L3
Description	IRQ status for Shared Message Transmit channel. Write 1 to a bit to clear it.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								ABORT	RESERVED	UDEF	NORE	NACK	PACK	OVERFLOW	MC_TX_COL

Bits	Field Name	Description	Type	Reset
31:8	RESERVED		R	0x000000
7	ABORT	TX message was aborted before completion because of message sync loss. Write 0x0: No action Write 0x1: Clear pending event, if any Read 0x1: IRQ event pending Read 0x0: No event pending	RW W1toClr	0
6	RESERVED		R	0

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Bits	Field Name	Description	Type	Reset
5	UDEF	TX message was UDEF'ed: undefined response, protocol error. Write 0x0: No action Write 0x1: Clear pending event, if any Read 0x1: IRQ event pending Read 0x0: No event pending	RW W1toClr	0
4	NORE	TX message was NORE'ed: no or all-zero message response Write 0x0: No action Write 0x1: Clear pending event, if any Read 0x1: IRQ event pending Read 0x0: No event pending	RW W1toClr	0
3	NACK	TX message was NACK'ed: at least one of the recipient devices requested message retransmission. Write 0x0: No action Write 0x1: Clear pending event, if any Read 0x1: IRQ event pending Read 0x0: No event pending	RW W1toClr	0
2	PACK	TX message was PACK'ed: all recipient devices accepted the message. Write 0x0: No action Write 0x1: Clear pending event, if any Read 0x1: IRQ event pending Read 0x0: No event pending	RW W1toClr	0
1	OVERFLOW	Overflow in TX message FIFO: Software tried to write more bytes than available in the FIFO. Write 0x0: No action Write 0x1: Clear pending event, if any Read 0x1: IRQ event pending Read 0x0: No event pending	RW W1toClr	0
0	MC_TX_COL	Transmit collision in Message Channel (MC) during message transmission. Interface device class-specific information element (IE) Write 0x0: No action Write 0x1: Clear pending event, if any Read 0x1: IRQ event pending Read 0x0: No event pending	RW W1toClr	0

Table 23-718. Register Call Summary for Register SLIMBUS_SMT_INFO

Serial Low-Power Inter-Chip Media Bus Controller

- SLIMbus Boot and Reset Procedures: [0]
- Transmission: [1] [2] [3] [4] [5] [6] [7] [8] [9] [10]
- Message reception: [11]
- Possible Interrupts: [12] [13] [14] [15] [16] [17] [18]
- Shared Message Channel Transmit ISRs: [19] [20] [21] [22] [23] [24]
- Shared Message Channel Receive ISRs: [25]
- SLIMbus Transfer Procedures: [26] [27]
- SLIMBUS1 Register Summary: [28]
- SLIMBUS2 Register Summary: [29]

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Table 23-719. SLIMBUS_SMT_MESSAGE

Address Offset	0x0000 0054		
Physical Address	0x4902 C054 0x4012 C054 0x2 C054 0x4807 6054	**Instance**	SLIMBUS1_L3 SLIMBUS1_CORTEX-A9 SLIMBUS1_DSP SLIMBUS2_L3
Description	Shared Message Transmit FIFO input		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TX_MESSAGE																															

Bits	Field Name	Description	Type	Reset
31:0	TX_MESSAGE	TX message byte(s), depending on packing mode. Reads return 0. Enter the whole message except last byte (Message Integrity MI and Response MR), and with a don't care placeholder for Primary Integrity (PI).	RW	0x0000 0000

Table 23-720. Register Call Summary for Register SLIMBUS_SMT_MESSAGE

Serial Low-Power Inter-Chip Media Bus Controller

- Transmission: [0]
- SLIMbus Transfer Procedures: [1]
- SLIMBUS1 Register Summary: [2]
- SLIMBUS2 Register Summary: [3]

Table 23-721. SLIMBUS_SMT_CONTROL

Address Offset	0x0000 0058		
Physical Address	0x4902 C058 0x4012 C058 0x2 C058 0x4807 6058	**Instance**	SLIMBUS1_L3 SLIMBUS1_CORTEX-A9 SLIMBUS1_DSP SLIMBUS2_L3
Description	Control of Shared Message channel Transmission.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															MESSAGE_ENABLE

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Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	MESSAGE_ENABLE	Enable the transmission of the message(s) previously written into the TX Message FIFO, with unlimited arbitration auto-retries. Self-cleared after either a message not get PACK'ed or the FIFO is empty. Write 0x0: No effect Write 0x1: Request transmission of stored messages Read 0x1: Message transmission is ongoing Read 0x0: Message transmission is stopped / complete	RW	0

Table 23-722. Register Call Summary for Register SLIMBUS_SMT_CONTROL

Serial Low-Power Inter-Chip Media Bus Controller

- Transmission: [0] [1] [2] [3]
- SLIMbus Transfer Procedures: [4] [5]
- SLIMBUS1 Register Summary: [6]
- SLIMBUS2 Register Summary: [7]

Table 23-723. SLIMBUS_SMT_FIFO_SETUP

Address Offset	0x0000 005C		
Physical Address	0x4902 C05C 0x4012 C05C 0x2 C05C 0x4807 605C	**Instance**	SLIMBUS1_L3 SLIMBUS1_CORTEX-A9 SLIMBUS1_DSP SLIMBUS2_L3
Description	Shared Message Transmit channel configuration. To be kept static during operation. Note that message segment word size is 2 slots = 1 byte (= message size granularity) and that message FIFO base address is always 0x0.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								PACKING	SIZE_HI		SIZE_LO				FIFO_CLEAR

Bits	Field Name	Description	Type	Reset
31:8	RESERVED		R	0x000000
7	PACKING	Packing enable control for TX message FIFO 0x0: Packing disabled: one byte per access only (LSByte), byte enable is don't care. 0x1: Packing enabled: one or several bytes per access, depending on byte enable.	RW	0
6:5	SIZE_HI	(Upper bits of the) capacity of shared TX message FIFO, in bytes, minus one. To be set for largest supported (transmitted) message(s). 0x0: 16 bytes (minimum size) 0x1: 32 bytes (recommended) 0x3: 64 bytes (max size) 0x2: 48 bytes (large messages)	RW	0x1
4:1	SIZE_LO	(Lower bits of the) capacity of shared TX message FIFO, in bytes, minus one. Read-only, for reference only.	R	0xF

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Bits	Field Name	Description	Type	Reset
0	FIFO_CLEAR	Returns FIFO to initial empty state. Write 0x0: No effect Write 0x1: Clear FIFO Read 0x1: Ongoing Clear. Completion requires the SLIMbus clock. Read 0x0: No event, last clear completed	RW	0

Table 23-724. Register Call Summary for Register SLIMBUS_SMT_FIFO_SETUP

Serial Low-Power Inter-Chip Media Bus Controller

- FIFO Mapping: [0] [1]
- SLIMBUS1 Register Summary: [2]
- SLIMBUS2 Register Summary: [3]

Table 23-725. SLIMBUS_SMR_INFO

Address Offset	0x0000 0060		
Physical Address	0x4902 C060 0x4012 C060 0x2 C060 0x4807 6060	**Instance**	SLIMBUS1_L3 SLIMBUS1_CORTEX-A9 SLIMBUS1_DSP SLIMBUS2_L3
Description	IRQ status for Shared Message Receive channel. Write 1 to a bit to clear it.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																											OVERFLOW	RECEIVED_RECONFIGURE	RECEIVED_MESSAGE	UNDERFLOW	MC_TX_COL

Bits	Field Name	Description	Type	Reset
31:5	RESERVED		R	0x0000000
4	OVERFLOW	Overflow in RX message FIFO: received message is larger than the FIFO. Write 0x0: no action Write 0x1: clear event Read 0x1: event pending Read 0x0: no event pending	RW W1toClr	0
3	RECEIVED_RECONFIGURE	RECONFIGURE_NOW message received, available in RX message FIFO Write 0x0: no action Write 0x1: clear event Read 0x1: event pending Read 0x0: no event pending	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
2	RECEIVED_MESSAGE	Message available in the RX message FIFO. Clear bit to clear the FIFO and allow the reception of further messages (incoming messages will be NACK'ed until then). Write 0x0: no action Write 0x1: clear event, clear FIFO, allow further messages. Read 0x1: event pending Read 0x0: no event pending	RW W1toClr	0
1	UNDERFLOW	Underflow in RX message FIFO: Software tried to read out more bytes than available. Write 0x0: no action Write 0x1: clear event Read 0x1: event pending Read 0x0: no event pending	RW W1toClr	0
0	MC_TX_COL	Transmit collision in Message Channel (MC) during RX message during message reception. Interface device class-specific information element (IE) Write 0x0: no action Write 0x1: clear event Read 0x1: event pending Read 0x0: no event pending	RW W1toClr	0

Table 23-726. Register Call Summary for Register SLIMBUS_SMR_INFO

Serial Low-Power Inter-Chip Media Bus Controller

- SLIMbus Boot and Reset Procedures: [0]
- Transmission: [1] [2]
- Message reception: [3] [4] [5] [6] [7] [8] [9]
- Possible Interrupts: [10] [11] [12] [13] [14]
- Shared Message Channel Receive ISRs: [15] [16] [17] [18]
- Operational Modes Configuration: [19]
- SLIMbus Transfer Procedures: [20] [21] [22] [23] [24] [25] [26]
- Event Handling: [27]
- SLIMBUS1 Register Summary: [28]
- SLIMBUS2 Register Summary: [29]

Table 23-727. SLIMBUS_SMR_MESSAGE

Address Offset	0x0000 0064		
Physical Address	0x4902 C064 0x4012 C064 0x2 C064 0x4807 6064	**Instance**	SLIMBUS1_L3 SLIMBUS1_CORTEX-A9 SLIMBUS1_DSP SLIMBUS2_L3
Description	Shared Message Receive channel FIFO output.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_MESSAGE																															

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Bits	Field Name	Description	Type	Reset
31:0	RX_MESSAGE	RX message byte(s), depending on packing mode. Writes have no effect. Readout value from an empty FIFO is undefined, that is, there is no defined "reset value". Message is guaranteed to have destination address matching a local device address (LA or EA), correct Primary and Message Integrity (PI MI) and PACK Message Response (MR). Whole message available for readout, including the last byte (Message Integrity MI and Response MR)	R	0x0000 0000

Table 23-728. Register Call Summary for Register SLIMBUS_SMR_MESSAGE

Serial Low-Power Inter-Chip Media Bus Controller

- Message reception: [0]
- SLIMbus Transfer Procedures: [1]
- SLIMBUS1 Register Summary: [2]
- SLIMBUS2 Register Summary: [3]

Table 23-729. SLIMBUS_SMR_CONTROL

Address Offset	0x0000 0068		
Physical Address	0x4902 C068 0x4012 C068 0x2 C068 0x4807 6068	**Instance**	SLIMBUS1_L3 SLIMBUS1_CORTEX-A9 SLIMBUS1_DSP SLIMBUS2_L3
Description	Control of Shared Message channel Reception.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															MESSAGE_DISABLE

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	MESSAGE_DISABLE	Disables the reception of incoming messages (that is, broadcast or locally addressed) into the RX Message FIFO. Same effect for the same value than SMR_INFO[2] RECEIVED_MESSAGE, but this bit can be set to 1. 0x0: Enabled: incoming messages will be PACK'ed 0x1: Disabled: incoming messages will be NACK'ed	RW	0

Table 23-730. Register Call Summary for Register SLIMBUS_SMR_CONTROL

Serial Low-Power Inter-Chip Media Bus Controller

- SLIMBUS1 Register Summary: [0]
- SLIMBUS2 Register Summary: [1]

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Table 23-731. SLIMBUS_SMR_FIFO_SETUP

Address Offset	0x0000 006C		
Physical Address	0x4902 C06C 0x4012 C06C 0x2 C06C 0x4807 606C	**Instance**	SLIMBUS1_L3 SLIMBUS1_CORTEX-A9 SLIMBUS1_DSP SLIMBUS2_L3
Description	Shared Message Receive channel setup. To be kept static during operation. Note that message segment word size is 2 slots = 1 byte (= message size granularity) and that message FIFO base address is always 0x0.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								PACKING	SIZE_HI			SIZE_LO			FIFO_CLEAR

Bits	Field Name	Description	Type	Reset
31:8	RESERVED		R	0x000000
7	PACKING	Packing enable control for RX message FIFO 0x0: Packing disabled: one byte per access only (LSByte), byte enable is don't care. 0x1: Packing enabled: one or several bytes per access, depending on byte enable.	RW	0
6:5	SIZE_HI	(Upper bits of the) capacity of shared RX message FIFO, in bytes, minus one. To be set for largest supported (received) message. 0x0: 16 bytes (minimum size) 0x1: 32 bytes (recommended) 0x3: 64 bytes (max size) 0x2: 48 bytes (large messages)	RW	0x1
4:1	SIZE_LO	(Lower bits of the) capacity of shared RX message FIFO, in bytes, minus one. Read-only, for reference only.	R	0xF
0	FIFO_CLEAR	Returns message FIFO to initial empty state. Write 0x0: No effect Write 0x1: Clear FIFO Read 0x1: Ongoing Clear. Completion requires the SLIMbus clock. Read 0x0: No event, last clear completed	RW	0

Table 23-732. Register Call Summary for Register SLIMBUS_SMR_FIFO_SETUP

Serial Low-Power Inter-Chip Media Bus Controller

- FIFO Mapping: [0] [1]
- SLIMBUS1 Register Summary: [2]
- SLIMBUS2 Register Summary: [3]

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Table 23-733. SLIMBUS_FL_INFO

Address Offset	0x0000 0070		
Physical Address	0x4902 C070 0x4012 C070 0x2 C070 0x4807 6070	**Instance**	SLIMBUS1_L3 SLIMBUS1_CORTEX-A9 SLIMBUS1_DSP SLIMBUS2_L3
Description	Frame Layer IRQ status. Write 1 to a bit to clear it. Note: FS loss implies SFS loss, and SFS loss implies MS loss, but only the "strongest" loss event is logged for a given event.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RECONFIGURED	SAW_BUS_RESET	RESERVED	FOUND_MS	LOST_MS	LOST_SFS	LOST_FS	

Bits	Field Name	Description	Type	Reset
31:7	RESERVED		R	0x0000000
6	RECONFIGURED	Reconfiguration boundary crossed Write 0x0: No action Write 0x1: Clear pending event, if any Read 0x1: IRQ event pending Read 0x0: No event pending	RW W1toClr	0
5	SAW_BUS_RESET	Bus reset sequence detected on the bus: no activity on DATA line (all-zero) for 2 to 4 frames. Clock receiver FSM has returned to Reset state. Should trigger a local component reset (software sequence). Write 0x0: No action Write 0x1: Clear pending event, if any Read 0x1: IRQ event pending Read 0x0: No event pending	RW W1toClr	0
4	RESERVED		R	0
3	FOUND_MS	Message sync was acquired: operational state reached Write 0x0: No action Write 0x1: Clear pending event, if any Read 0x1: IRQ event pending Read 0x0: No event pending	RW W1toClr	0
2	LOST_MS	Message Synchronization was lost Interface device class-specific information element (IE) Note: Not asserted in case of FS or SFS loss. Write 0x0: No action Write 0x1: Clear pending event, if any Read 0x1: IRQ event pending Read 0x0: No event pending	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
1	LOST_SFS	Super Frame Synchronization was lost Interface device class-specific information element (IE) Note: Not asserted in case of FS loss. Write 0x0: No action Write 0x1: Clear pending event, if any Read 0x1: IRQ event pending Read 0x0: No event pending	RW W1toClr	0
0	LOST_FS	Frame Synchronization was lost Interface device class-specific information element (IE) Write 0x0: No action Write 0x1: Clear pending event, if any Read 0x1: IRQ event pending Read 0x0: No event pending	RW W1toClr	0

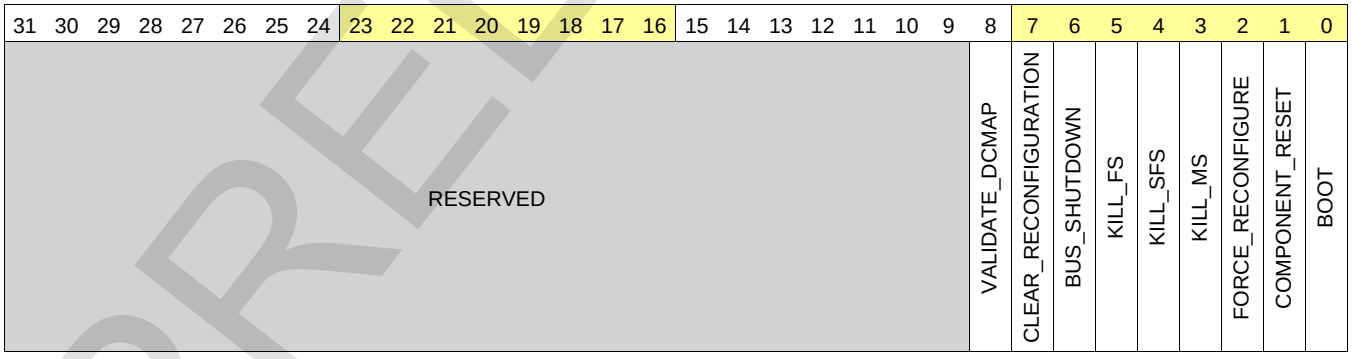
Table 23-734. Register Call Summary for Register SLIMBUS_FL_INFO

Serial Low-Power Inter-Chip Media Bus Controller

- SLIMbus Boot and Reset Procedures: [0] [1] [2]
- Possible Interrupts: [3] [4] [5] [6] [7] [8]
- Interface Device ISRs: [9] [10] [11] [12] [13] [14]
- Device Enumeration: [15] [16]
- SLIMBUS1 Register Summary: [17]
- SLIMBUS2 Register Summary: [18]

Table 23-735. SLIMBUS_FL_CONTROL

Address Offset	0x0000 0074		
Physical Address	0x4902 C074 0x4012 C074 0x2 C074 0x4807 6074	**Instance**	SLIMBUS1_L3 SLIMBUS1_CORTEX-A9 SLIMBUS1_DSP SLIMBUS2_L3
Description	Frame Layer control. (Self-cleared bits)		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	VALIDATE_DCMAP	Validates the mapping of data channels on devices: to be used after modifying the DC*_MAP* fields (DI and PN). Write 0x0: No action Write 0x1: Validates all DCT_MAP / DCR_MAP values	RW	0

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Bits	Field Name	Description	Type	Reset
7	CLEAR_RECONFIGURATION	Clear all updates cumulated since the last reconfiguration, return reconfiguration fields to currently active value. Self-cleared immediately. Write 0x0: No action Write 0x1: Clear reconfiguration	RW	0
6	BUS_SHUTDOWN	Sets both the clock source or the clock receiver FSMs back to "Undefined" state at the next reconfiguration boundary. Executed (and bit self-cleared) on next reconfiguration (forced or not); also cleared by a "clear_reconfiguration". Write 0x0: Cancel pending request (not used in normal operation) if any, otherwise no action Write 0x1: Assert request for next reconfiguration Read 0x1: Request pending for next reconfiguration Read 0x0: No request pending for next reconfiguration	RW	0
5	KILL_FS	Force immediate Frame Synchronization loss (implying as well message and superframe sync) When in "Operational", "SeekingMessageSync" or "SeekingSuperFrameSync" states, component shall go to "SeekingFrameSync" and start reaquiring frame sync. No effect otherwise. For debug use. Write 0x0: No action Write 0x1: Force frame sync loss Read 0x0: Always reads 0 because of immediate action.	RW	0
4	KILL_SFS	Force SuperFrame Synchronization loss at next reconfiguration boundary (implying as well message sync loss). When in "Operational" or "SeekingMessageSync" states, component shall go to "SeekingSuperFrameSync" and start reaquiring superframe sync. No effect otherwise. Used by clock receiver component upon imcompletely received reconfiguration sequence. Write 0x0: No action Write 0x1: Schedule superframe sync loss Read 0x1: Superframe sync loss pending Read 0x0: No pending superframe sync loss	RW	0
3	KILL_MS	Force an immediate Message Synchronization loss. When in "Operational" state, component shall go to "SeekingMessageSync" and start reaquiring message sync. No effect otherwise. For debug use. Write 0x0: No action Write 0x1: Force message sync loss Read 0x0: Always reads 0 because of immediate action.	RW	0
2	FORCE_RECONFIGURE	Force a reconfiguration boundary at next superframe boundary, rather than wait for a RECONFIGURE_NOW() message. Write 0x0: Cancel pending request (not used in normal operation) if any, otherwise no action Write 0x1: Assert reconfiguration request for next superframe boundary Read 0x1: Reconfiguration request pending for next superframe boundary Read 0x0: No request pending	RW	0

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Bits	Field Name	Description	Type	Reset
1	COMPONENT_RESET	Component reset request control: Transitions clock receiver FSM to state "Reset" (from any other state). Immediate action. Set upon reception of the RESET_DEVICE() message by the interface device, which requires a component-level reset. Note that a component-level reset is also required in case of bus reset, but the transition to "Reset" state happens automatically in that case and this bit is not used. Write 0x1: Assert request for next reconfiguration	RW	0
0	BOOT	Boot the component when not in active framer mode (don't care when in active framer mode). Transitions clock receiver FSM from state "Undefined" to "Reset". 0x0: No action 0x1: Enable clock receiver boot sequence	RW	0

Table 23-736. Register Call Summary for Register SLIMBUS_FL_CONTROL

Serial Low-Power Inter-Chip Media Bus Controller

- SLIMbus Boot and Reset Procedures: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9]
- SLIMbus Reconfigure Parameters: [10] [11] [12] [13] [14]
- SLIMbus Component Boot: [15] [16] [17] [18] [19]
- Data Agent Assignment: [20]
- Operational Modes Configuration: [21]
- SLIMBUS1 Register Summary: [22]
- SLIMBUS2 Register Summary: [23]

Table 23-737. SLIMBUS_FL_SM

Address Offset	0x0000 0078		
Physical Address	0x4902 C078 0x4012 C078 0x2 C078 0x4807 6078	**Instance**	SLIMBUS1_L3 SLIMBUS1_CORTEX-A9 SLIMBUS1_DSP SLIMBUS2_L3
Description	Subframe mode (SM: defines control vs. data space partition) control status Software must write in values : a) to use when booting in active framer mode. b) extracted from NEXT_SUBFRAME_MODE(SM), to use at following reconfiguration boundary. Hardware-updated upon superframe sync acquisition, when booting in clock receiver mode.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								SM							

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Bits	Field Name	Description	Type	Reset
31:5	RESERVED		R	0x0000000
4:0	SM	Subframe Mode, which sets Control Space Width (CSW) and Subframe Length (SFL), both expressed in slots. Note that we always have CSW = SFL since the control is included in the subframe. 0xD: CSW=3; SFL=8 (37.5% control) 0x15: CSW=6; SFL=8 (75% control) 0x1E: reserved. Same effect than 0b00000 0x8: CSW=2; SFL=6 (33.3% control) 0x5: CSW=1; SFL=8 (12.5% control) 0x1B: CSW=12; SFL=32 (37.5% control) 0x2: reserved. Same as 0x00 0x4: CSW=1; SFL=6 (16.7% control) 0x6: CSW=1; SFL=24 (4.17% control) 0x1: reserved. Same as 0x05 0x1D: CSW=16; SFL=32 (50% control) 0x0: CSW=8; SFL=8 (100% control vs. 0% data) 0xB: CSW=2; SFL=32 (6.25% control) 0x3: reserved. Same as 0x07 0x17: CSW=6; SFL=32 (18.8% control) 0x11: CSW=4; SFL=8 (50% control) 0xA: CSW=2; SFL=24 (8.33% control) 0x9: CSW=2; SFL=8 (25% control) 0x10: CSW=4; SFL=6 (66.7% control) 0x12: CSW=4; SFL=24 (16.7% control) 0x13: CSW=4; SFL=32 (12.5% control) 0x18: CSW=8; SFL=24 (33.3% control) 0x14: reserved. Same as 0x00 0xE: CSW=3; SFL=24 (12.5% control) 0x16: CSW=6; SFL=24 (25% control) 0x1C: CSW=16; SFL=24 (66.7% control) 0x7: CSW=1; SFL=32 (3.13% control) 0x19: CSW=8; SFL=32 (25% control) 0x1F: CSW=24; SFL=32 (75% control) 0x1A: CSW=12; SFL=24 (50% control) 0xF: CSW=3; SFL=32 (9.38% control) 0xC: CSW=3; SFL=6 (50% control)	RW	0x00

Table 23-738. Register Call Summary for Register SLIMBUS_FL_SM

Serial Low-Power Inter-Chip Media Bus Controller

- SLIMbus Boot and Reset Procedures: [0]
- SLIMbus Reconfigure Parameters: [1]
- SLIMbus Component Boot: [2]
- SLIMBUS1 Register Summary: [3]
- SLIMBUS2 Register Summary: [4]

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Table 23-739. SLIMBUS_FL_CG

Address Offset	0x0000 007C		
Physical Address	0x4902 C07C 0x4012 C07C 0x2 C07C 0x4807 607C	**Instance**	SLIMBUS1_L3 SLIMBUS1_CORTEX-A9 SLIMBUS1_DSP SLIMBUS2_L3
Description	Clock Gear (CG) control and status Software must write in values : a) to use when booting in active framer mode. b) extracted from NEXT_CLOCK_GEAR(CG), to use at following reconfiguration boundary. Hardware-updated upon superframe sync acquisition, when booting in clock receiver mode.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												CG			

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0000000
3:0	CG	Clock Gear (CG) to be used after the next reconfiguration boundary. Root / SLIMbus frequency ratio is defined as $2^{(10-CG)}$ 0x6: Ratio to root frequency: 16 0x1: Ratio to root frequency: 512 0xA: Ratio to root frequency: 1 (undivided) 0x7: Ratio to root frequency: 8 0x3: Ratio to root frequency: 128 0x2: Ratio to root frequency: 256 0x8: Ratio to root frequency: 4 0x9: Ratio to root frequency: 2 0x5: Ratio to root frequency: 32 0x4: Ratio to root frequency: 64	RW	0x0

Table 23-740. Register Call Summary for Register SLIMBUS_FL_CG

Serial Low-Power Inter-Chip Media Bus Controller

- SLIMbus Boot and Reset Procedures: [0]
- SLIMbus Reconfigure Parameters: [1]
- SLIMbus Component Boot: [2]
- SLIMBUS1 Register Summary: [3]
- SLIMBUS2 Register Summary: [4]

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Table 23-741. SLIMBUS_FL_RF

Address Offset	0x0000 0080		
Physical Address	0x4902 C080 0x4012 C080 0x2 C080 0x4807 6080	**Instance**	SLIMBUS1_L3 SLIMBUS1_CORTEX-A9 SLIMBUS1_DSP SLIMBUS2_L3
Description	Root frequency (RF = SLIMbus clock frequency when in gear 10) control status Software must write in values : a) to use when booting in active framer mode. b) extracted from NEXT_ROOT_FREQUENCY(RF), to use at following reconfiguration boundary. Hardware-updated upon superframe sync acquisition, when booting in clock receiver mode.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												RF			

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0000000
3:0	RF	Root frequency 0x6: 24 MHz 0x1: 24.576 MHz 0x7: 25 MHz 0x0: Root frequency not indicated 0x2: 22.5792 MHz 0x8: 26 MHz 0x9: 27 MHz 0x4: 16.8 MHz 0x5: 19.2 MHz 0x3: 15.36 MHz	RW	0x0

Table 23-742. Register Call Summary for Register SLIMBUS_FL_RF

Serial Low-Power Inter-Chip Media Bus Controller

- SLIMbus Boot and Reset Procedures: [0]
- SLIMbus Reconfigure Parameters: [1]
- SLIMbus Component Boot: [2]
- SLIMBUS1 Register Summary: [3]
- SLIMBUS2 Register Summary: [4]

Table 23-743. SLIMBUS_FR_INFO

Address Offset	0x0000 0090		
Physical Address	0x4902 C090 0x4012 C090 0x2 C090 0x4807 6090	**Instance**	SLIMBUS1_L3 SLIMBUS1_CORTEX-A9 SLIMBUS1_DSP SLIMBUS2_L3
Description	Framer device status (when active). Write 1 to a bit to clear it.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																										CLOCK_RESTART	FRAMER_UNACTIVATED	FRAMER_ACTIVATED	GC_TX_COL	FI_TX_COL	FS_TX_COL

Bits	Field Name	Description	Type	Reset
31:6	RESERVED		R	0x0000000
5	CLOCK_RESTART	Clock restart request event detected (that is, asynchronous DATA line transition during clock pause) 0x0: no event pending 0x1: event pending	RW W1toClr	0
4	FRAMER_UNACTIVATED	Framer has left clock source operational state. Set on ACTIVE_FRAMER information element deassertion. (framer device class-specific IE) 0x0: no event pending 0x1: event pending	RW W1toClr	0
3	FRAMER_ACTIVATED	Framer has reached clock source operational state. Set on ACTIVE_FRAMER information element assertion. (framer device class-specific IE) 0x0: no event pending 0x1: event pending	RW W1toClr	0
2	GC_TX_COL	Collision during guide byte transmit (Guide Channel) Framer device class-specific information element (IE) 0x0: no event pending 0x1: event pending	RW W1toClr	0
1	FI_TX_COL	Collision during Framing Information transmit (framing channel) Framer device class-specific information element (IE) 0x0: no event pending 0x1: event pending	RW W1toClr	0
0	FS_TX_COL	Collision during Frame Sync symbol transmit (framing channel) Framer device class-specific information element (IE) 0x0: no event pending 0x1: event pending	RW W1toClr	0

Table 23-744. Register Call Summary for Register SLIMBUS_FR_INFO

Serial Low-Power Inter-Chip Media Bus Controller

- Wake-Up Request: [0]
- Power Management: [1]
- SLIMbus Boot and Reset Procedures: [2] [3] [4]
- Possible Interrupts: [5] [6] [7] [8] [9] [10]
- Framer Device ISRs: [11] [12] [13]
- SLIMBUS1 Register Summary: [14]
- SLIMBUS2 Register Summary: [15]

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Table 23-745. SLIMBUS_FR_CLOCK_SOURCE

Address Offset	0x0000 0094		
Physical Address	0x4902 C094 0x4012 C094 0x2 C094 0x4807 6094	**Instance**	SLIMBUS1_L3 SLIMBUS1_CORTEX-A9 SLIMBUS1_DSP SLIMBUS2_L3
Description	Root clock configuration for active framer mode, used at next reconfiguration boundary. Unused when not active framer.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								CLKSEL				CLKDIV			

Bits	Field Name	Description	Type	Reset
31:7	RESERVED		R	0x0000000
6:4	CLKSEL	SLIMbus clock selection 0x0: FCLK1 0x1: FCLK2 0x2: FCLK3	RW	0x0
3:0	CLKDIV	Root divider ratio, applied on clock input to obtain root clock, to be used at next reconfiguration boundary. Input/ root frequency ratio is defined as $2^{(CLKDIV-5)}$ With CG the SLIMbus clock gear, Input / SLIMbus frequency ratio is therefore $2^{(5+CLKDIV-CG)}$ WARNING: that last ratio has to be 1 or greater, to be implementable by the actual clock divider. 0x6: Ratio is 2 0x1: Ratio is 1/16: Gears 7 to 10 forbidden 0xA: Ratio is 32 0x7: Ratio is 4 0x0: Ratio is 1/32: Gears 6 to 10 forbidden 0x2: Ratio is 1/8: Gears 8 to 10 forbidden 0x8: Ratio is 8 0x9: Ratio is 16 0x4: Ratio is 1/2: Gear 10 forbidden. 0x5: Ratio is 1 (root freq. = input freq.) 0x3: Ratio is 1/4: Gears 9-10 forbidden	RW	0x0

Table 23-746. Register Call Summary for Register SLIMBUS_FR_CLOCK_SOURCE

Serial Low-Power Inter-Chip Media Bus Controller

- SLIMbus Boot and Reset Procedures: [0] [1]
- SLIMbus Reconfigure Parameters: [2] [3]
- Interface Device ISRs: [4]
- SLIMbus Component Boot: [5] [6]
- SLIMBUS1 Register Summary: [7]
- SLIMBUS2 Register Summary: [8]

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Table 23-747. SLIMBUS_FR_CONTROL

Address Offset	0x0000 0098		
Physical Address	0x4902 C098 0x4012 C098 0x2 C098 0x4807 6098	**Instance**	SLIMBUS1_L3 SLIMBUS1_CORTEX-A9 SLIMBUS1_DSP SLIMBUS2_L3
Description	Framer Device control. Unused when not active framer. (Self-cleared bits)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														BUS_RESET	BOOT

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	BUS_RESET	Bus reset request control, when framer is already active. Set upon reception of the NEXT_RESET_BUS() message. Transitions clock source FSM to state "StartingClock" (from "Operational"). Write 0x0: Cancel pending request (not used in normal operation) if any, otherwise no action Write 0x1: Assert request for next reconfiguration Read 0x1: Request pending for next reconfiguration Read 0x0: No request pending for next reconfiguration	RW	0
0	BOOT	Initiate an active framer (clock source) boot sequence for the component, that is, when component is default active framer. Transitions clock source FSM from state "Undefined" to "CheckingDataLine". Transitions clock receiver FSM from state "Undefined" to "Reset". No effect if bus has already booted. Write 0x0: Cancel pending request (not used in normal operation) if any, otherwise no action Write 0x1: Assert request for next reconfiguration Read 0x1: Request pending for next reconfiguration Read 0x0: No request pending for next reconfiguration	RW	0

Table 23-748. Register Call Summary for Register SLIMBUS_FR_CONTROL

Serial Low-Power Inter-Chip Media Bus Controller

- SLIMbus Boot and Reset Procedures: [0] [1] [2] [3] [4]
- SLIMbus Reconfigure Parameters: [5] [6]
- SLIMbus Component Boot: [7]
- SLIMBUS1 Register Summary: [8]
- SLIMBUS2 Register Summary: [9]

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Table 23-749. SLIMBUS_FR_FRAMER_HANDOVER

Address Offset	0x0000 009C		
Physical Address	0x4902 C09C 0x4012 C09C 0x2 C09C 0x4807 609C	**Instance**	SLIMBUS1_L3 SLIMBUS1_CORTEX-A9 SLIMBUS1_DSP SLIMBUS2_L3
Description	Framer handover control (outgoing if currently active, incoming if currently inactive)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																			HANDOVER_ENABLE	NCO_NCI											

Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000
12	HANDOVER_ENABLE	Enable framer handover, upon NEXT_ACTIVE_FRAMER(NCi,NCo) reception. Self-cleared upon handover, that is, at next reconfiguration boundary. 0x0: No framer handover 0x1: Framer handover at next configuration boundary.	RW	0
11:0	NCO_NCI	NCo[11:0] / NCi[11:0] for outgoing / incoming framer respectively, as extracted from NEXT_ACTIVE_FRAMER(NCi,NCo) Used on framer handover at next reconfiguration boundary.	RW	0x000

Table 23-750. Register Call Summary for Register SLIMBUS_FR_FRAMER_HANDOVER

Serial Low-Power Inter-Chip Media Bus Controller

- SLIMbus Reconfigure Parameters: [0] [1] [2]
- SLIMBUS1 Register Summary: [3]
- SLIMBUS2 Register Summary: [4]

Table 23-751. SLIMBUS_FR_CLOCK_PAUSE

Address Offset	0x0000 00A0		
Physical Address	0x4902 C0A0 0x4012 C0A0 0x2 C0A0 0x4807 60A0	**Instance**	SLIMBUS1_L3 SLIMBUS1_CORTEX-A9 SLIMBUS1_DSP SLIMBUS2_L3
Description	Clock pause restart control. Applied at following reconfiguration boundary, that is, where the clock is paused. Note that programming is indentical for an active framer (clock source) and a clock receiver.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						RT_HI							RT		CLOCK_PAUSE

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8:3	RT_HI	MSBs of 8-bit SLIMbus parameter. Constant. Read 0x0: Only legal, unreserved value.	R	0x00
2:1	RT	Restart Time (RT) for recovery after clock pause, as extracted from NEXT_PAUSE_CLOCK(RT) LSBs of 8-bit SLIMbus parameter. Unused when not active framer. 0x0: Fast recovery (less than 4 cells) 0x1: Constant-phase recovery (superframe phase preserved) 0x2: Unspecified recovery delay	RW	0x0
0	CLOCK_PAUSE	Control clock pause / restart. Self-cleared upon restart. 0x0: Force clock restart if paused, no effect otherwise. 0x1: Pause clock (clock source) or expect clock pause (clock receiver) at next configuration boundary	RW	0

Table 23-752. Register Call Summary for Register SLIMBUS_FR_CLOCK_PAUSE

Serial Low-Power Inter-Chip Media Bus Controller

- SLIMbus Reconfigure Parameters: [0] [1] [2]
- SLIMBUS1 Register Summary: [3]
- SLIMBUS2 Register Summary: [4]

Table 23-753. SLIMBUS_DEV_LA_i

Address Offset	0x0000 0100 + (0x10 * i)	**Index**	i = 0 to 6
Physical Address	0x4902 C100 + (0x10 * i) 0x4012 C100 + (0x10 * i) 0x2 C100 + (0x10 * i) 0x4807 6100 + (0x10 * i)	**Instance**	SLIMBUS1_L3 SLIMBUS1_CORTEX-A9 SLIMBUS1_DSP SLIMBUS2_L3
Description	Device Logical Address control		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						EA_ENABLE	LA_ENABLE	LA							

Bits	Field Name	Description	Type	Reset
31:10	RESERVED		R	0x000000
9	EA_ENABLE	Enables the reception of "long-header" messages to the device's hardwired Enumeration Address (EA). Don't care if LA_ENABLE is 1. 0x0: EA is not valid 0x1: EA is used for message reception	RW	0

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Bits	Field Name	Description	Type	Reset
8	LA_ENABLE	Enables the reception of "short-header" messages to the device's Logical Address (LA). 0x0: LA is not valid 0x1: LA valid, to be used for message reception	RW	0
7:0	LA	Device Logical Address, assigned by manager device at enumeration (0x00 through 0xEF). The active manager device itself has address 0xFF by default. 0xFF: active manager device address	RW	0x00

Table 23-754. Register Call Summary for Register SLIMBUS_DEV_LA_i

Serial Low-Power Inter-Chip Media Bus Controller

- SLIMbus Boot and Reset Procedures: [0] [1] [2]
- Device and Adressing Management: [3] [4] [5] [6]
- Message reception: [7]
- Device Enumeration: [8] [9] [10] [11] [12] [13]
- SLIMBUS1 Register Summary: [14]
- SLIMBUS2 Register Summary: [15]

Table 23-755. SLIMBUS_DEV_EA_LO_i

Address Offset	0x0000 0104 + (0x10 * i)	**Index**	i = 0 to 6
Physical Address	0x4902 C104 + (0x10 * i) 0x4012 C104 + (0x10 * i) 0x2 C104 + (0x10 * i) 0x4807 6104 + (0x10 * i)	**Instance**	SLIMBUS1_L3 SLIMBUS1_CORTEX-A9 SLIMBUS1_DSP SLIMBUS2_L3
Description	Device's Enumeration Address (EA[47:0]), lower 32 bits. For reference.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EA_PC																EA_DI								EA_IV							

Bits	Field Name	Description	Type	Reset
31:16	EA_PC	Product Code (PC[15:0]), shared by all devices of the component	R	0x0000
15:8	EA_DI	Device Index (DI[15:0]), hardcoded from 0 upwards (0x00,0x01,0x02, etc...) each device of the component. WARNING: value is incorrectly given as 0x00 for all indexes.	R	0x00
7:0	EA_IV	Component's Instance Value (IV[7:0]), shared by all devices of the component	R	0x00

Table 23-756. Register Call Summary for Register SLIMBUS_DEV_EA_LO_i

Serial Low-Power Inter-Chip Media Bus Controller

- Device and Adressing Management: [0] [1]
- SLIMBUS1 Register Summary: [2]
- SLIMBUS2 Register Summary: [3]

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Table 23-757. SLIMBUS_DEV_EA_HI_i

Address Offset	0x0000 0108 + (0x10 * i)	**Index**	i = 0 to 6
Physical Address	0x4902 C108 + (0x10 * i) 0x4012 C108 + (0x10 * i) 0x2 C108 + (0x10 * i) 0x4807 6108 + (0x10 * i)	**Instance**	SLIMBUS1_L3 SLIMBUS1_CORTEX-A9 SLIMBUS1_DSP SLIMBUS2_L3
Description	Device's Enumeration Address (EA[47:0]), upper 16 bits. For reference.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																EA_MI															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:0	EA_MI	Manufacturer Index (MI[15:0]), shared by all devices	R	0x0102

Table 23-758. Register Call Summary for Register SLIMBUS_DEV_EA_HI_i

Serial Low-Power Inter-Chip Media Bus Controller

- Device and Adressing Management: [0] [1]
- SLIMBUS1 Register Summary: [2]
- SLIMBUS2 Register Summary: [3]

Table 23-759. SLIMBUS_DCT_INFO_j

Address Offset	0x0000 0200 + (0x20 * j)	**Index**	j = 0 to 7 for SLIMBUS1 j = 0 to 3 for SLIMBUS2
Physical Address	0x4902 C200 + (0x20 * j) 0x4012 C200 + (0x20 * j) 0x2 C200 + (0x20 * j) 0x4807 6200 + (0x20 * j)	**Instance**	SLIMBUS1_L3 SLIMBUS1_CORTEX-A9 SLIMBUS1_DSP SLIMBUS2_L3
Description	TX data agent status. Write 1 to a bit to clear it.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												LOLEVEL	UNDERFLOW	OVERFLOW	DATA_TX_COL

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0000000
3	LOLEVEL	Write level of TX data agent FIFO has gone above DMA threshold (that is, writes required to fill FIFO) Note: Defaults to 0 (even though FIFO is then empty) as it sets to 1 only when read-only status bit DCT_FIFO_STATUS.LOLEVEL transitions from 0 to 1, that is, when threshold is actually crossed downward. Write 0x0: No action Write 0x1: Clear pending event, if any Read 0x1: IRQ event pending Read 0x0: No event pending	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
2	UNDERFLOW	Underflow in TX data agent FIFO. Note: never asserted in pushed or async TPs, by construction. Write 0x0: No action Write 0x1: Clear pending event, if any Read 0x1: IRQ event pending Read 0x0: No event pending	RW W1toClr	0
1	OVERFLOW	Overflow in TX data agent FIFO. Write 0x0: No action Write 0x1: Clear pending event, if any Read 0x1: IRQ event pending Read 0x0: No event pending	RW W1toClr	0
0	DATA_TX_COL	TX collision in TX data agent. Core information element (IE). Write 0x0: No action Write 0x1: Clear pending event, if any Read 0x1: IRQ event pending Read 0x0: No event pending	RW W1toClr	0

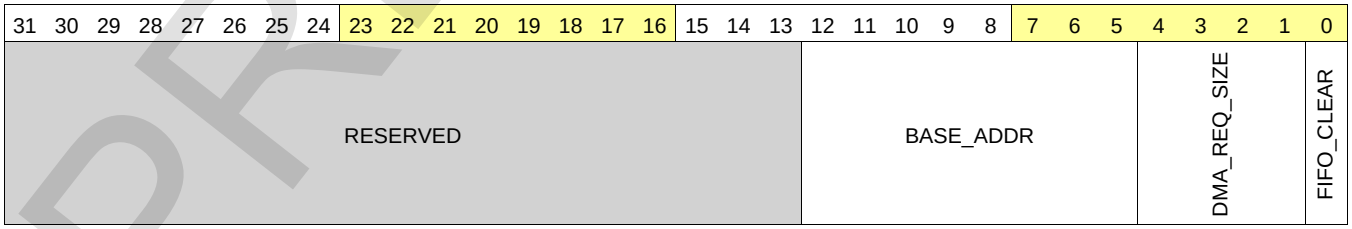
Table 23-760. Register Call Summary for Register SLIMBUS_DCT_INFO_j

Serial Low-Power Inter-Chip Media Bus Controller

- SLIMbus Boot and Reset Procedures: [0]
- Possible Interrupts: [1] [2] [3] [4]
- Data Channel Port ISRs: [5] [6] [7] [8] [9]
- SLIMbus Transfer Procedures: [10] [11]
- SLIMBUS1 Register Summary: [12]
- SLIMBUS2 Register Summary: [13]

Table 23-761. SLIMBUS_DCT_FIFO_SETUP1_j

Address Offset	0x0000 0204 + (0x20 * j)	**Index**	j = 0 to 7 for SLIMBUS1 j = 0 to 3 for SLIMBUS2
Physical Address	0x4902 C204 + (0x20 * j) 0x4012 C204 + (0x20 * j) 0x2 C204 + (0x20 * j) 0x4807 6204 + (0x20 * j)	**Instance**	SLIMBUS1_L3 SLIMBUS1_CORTEX-A9 SLIMBUS1_DSP SLIMBUS2_L3
Description	TX data agent FIFO setup. To be kept static during channel operation.		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000
12:5	BASE_ADDR	TX data agent FIFO base address within shared TX RAM. (physical address of the 32-bit wide RAM array)	RW	0x00

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Bits	Field Name	Description	Type	Reset
4:1	DMA_REQ_SIZE	DMA request size minus 1, in write accesses. In counting (packet) mode, last request may be smaller. Only applicable in precise DMA mode. 0xF: 16 accesses per DMA request 0x0: 1 access per DMA request	RW	0x0
0	FIFO_CLEAR	Returns FIFO to initial empty state. Write 0x0: No effect Write 0x1: Clear FIFO Read 0x1: Ongoing Clear. Completion requires the SLIMbus clock. Read 0x0: No event, last clear completed	RW	0

Table 23-762. Register Call Summary for Register SLIMBUS_DCT_FIFO_SETUP1_j

Serial Low-Power Inter-Chip Media Bus Controller

- FIFO Mapping: [0]
- FIFO Configuration: [1] [2]
- Operational Modes Configuration: [3] [4] [5]
- SLIMbus Transfer Procedures: [6] [7]
- SLIMBUS1 Register Summary: [8]
- SLIMBUS2 Register Summary: [9]

Table 23-763. SLIMBUS_DCT_FIFO_SETUP2_j

Address Offset	0x0000 0208 + (0x20 * j)	**Index**	j = 0 to 7 for SLIMBUS1 j = 0 to 3 for SLIMBUS2
Physical Address	0x4902 C208 + (0x20 * j) 0x4012 C208 + (0x20 * j) 0x2 C208 + (0x20 * j) 0x4807 6208 + (0x20 * j)	**Instance**	SLIMBUS1_L3 SLIMBUS1_CORTEX-A9 SLIMBUS1_DSP SLIMBUS2_L3
Description	TX data agent FIFO setup, continued. To be kept static during channel operation.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PACKING	MSB_ALIGNED	RESERVED						DMA_THRESHOLD								SB_THRESHOLD								SIZE							

Bits	Field Name	Description	Type	Reset
31	PACKING	Packing enable control 0x0: Packing disabled: one segment word per write access. Byte enable is don't care. 0x1: Packing enabled: one or several segment words per write access, depending on segment word size and byte enable. Only works in LSB-aligned mode. Behaviour in LSB-aligned mode is undefined.	RW	0
30	MSB_ALIGNED	PLACEHOLDER, NO EFFECT: DATA ALWAYS LSB-aligned LSB/MSB-alignment of FIFO input (write) TX data. 0x0: Input data is LSB-aligned 0x1: Input data is MSB-aligned	RW	0
29:24	RESERVED		R	0x00

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Bits	Field Name	Description	Type	Reset
23:16	DMA_THRESHOLD	SW-side TX data agent FIFO threshold. DMA write requests get (re-)asserted when WR_LEVEL is above threshold. Range: 0 to SIZE field value (included). 0xFF: DMA writes requested whenever FIFO is empty (assuming maximum FIFO size) 0x0: DMA writes requested whenever FIFO is not full	RW	0x00
15:8	SB_THRESHOLD	SLIMbus-side TX data agent FIFO threshold, used for SLIMbus transmission. 0xFF: Threshold condition = FIFO is full (assuming maximum FIFO size) 0x0: Threshold condition = FIFO is not empty	RW	0x00
7:0	SIZE	Capacity of FIFO in segment words, minus one. 0xFF: Maximum FIFO size 0x0: FIFO is 1-word deep (not recommended) 0x3: FIFO is 4-word deep. Recommended minimum setting (SLIMbus protocol).	RW	0x00

Table 23-764. Register Call Summary for Register SLIMBUS_DCT_FIFO_SETUP2_j

Serial Low-Power Inter-Chip Media Bus Controller

- FIFO Mapping: [0]
- FIFO Status: [1]
- FIFO Configuration: [2] [3] [4] [5]
- Operational Modes Configuration: [6] [7] [8]
- SLIMbus Transfer Procedures: [9] [10] [11]
- SLIMBUS1 Register Summary: [12]
- SLIMBUS2 Register Summary: [13]

Table 23-765. SLIMBUS_DCT_FIFO_STATUS_j

Address Offset	0x0000 020C + (0x20 * j)	**Index**	j = 0 to 7 for SLIMBUS1 j = 0 to 3 for SLIMBUS2
Physical Address	0x4902 C20C + (0x20 * j) 0x4012 C20C + (0x20 * j) 0x2 C20C + (0x20 * j) 0x4807 620C + (0x20 * j)	**Instance**	SLIMBUS1_L3 SLIMBUS1_CORTEX-A9 SLIMBUS1_DSP SLIMBUS2_L3
Description	TX data agent FIFO status, for software (non-DMA) FIFO management.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT_EN	ACC_CNT															IMPRECISE_EN	RESERVED							WR_LEVEL						LOLEVEL	FULL

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Bits	Field Name	Description	Type	Reset
31	COUNT_EN	Down-counter mode control. Only applicable in precise DMA mode. Write 0x0: Disable down-counter mode. Should typically be used only when ACC_CNT = 0. If ACC_CNT 0, DMA request gets deasserted immediately. Write 0x1: Enable down-counter mode. ACC_CNT is typically set to the desired value in the same write access. Read 0x1: Down-counter mode is enabled. DMA request can only be active when ACC_CNT 0 Read 0x0: Down-counter mode is disabled: DMA request follows FIFO level, and is active during no-tx periods.	RW	0
30:16	ACC_CNT	"Packet mode" down-counter of segment words, decremented on DCT_DATA write accesses. In that mode, DMA request shall deassert when ACC_CNT = 0 (that is, packet fully transmitted / stored in TX FIFO). Write 0x0: Deasserts current DMA request by forcing the count to zero (not typical operation) Write 0x7F: Set largest packet size (in accesses) to transfer before DMA request deassertion. Any lower value is also valid to enter. Read 0x7F: Maximum number of accesses still to be transferred before DMA deassertion. Unless interrupted, counter shall go through all values down to zero. Read 0x0: No access left to transfer, DMA request currently inactive.	RW	0x0000
15	IMPRECISE_EN	Precise vs. Imprecise DMA requesting mode control. (A DMA request is a single assertion-deassertion cycle.) 0x0: DMA request contains a precise number of accesses 0x1: DMA request is not expected to trigger a fixed number of accesses	RW	0
14:11	RESERVED		R	0x0
10:2	WR_LEVEL	Number of free segment words in FIFO, that could be filled by writes. Read 0x100: FIFO is empty and entirely available for writes (assuming maximum FIFO size) Read 0x0: FIFO is full and cannot be written to	R	0x001
1	LOLEVEL	Indicator of write level (WR_LEVEL: number of free words in FIFO) with respect to (write) threshold (DMA_threshold). Activates DMA write requests when high. Read 0x1: WR_LEVEL DMA_THRESHOLD Read 0x0: WR_LEVEL = DMA_THRESHOLD	R	1
0	FULL	FIFO full indicator Read 0x1: no space left in FIFO to write a word (WR_LEVEL = 0) Read 0x0: some space left in FIFO to write at least one word (WR_LEVEL 0)	R	0

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Table 23-766. Register Call Summary for Register SLIMBUS_DCT_FIFO_STATUS_j

Serial Low-Power Inter-Chip Media Bus Controller

- FIFO Status: [0] [1] [2]
- FIFO Configuration: [3] [4] [5] [6] [7]
- SLIMbus Transfer Procedures: [8] [9] [10]
- SLIMBUS1 Register Summary: [11]
- SLIMBUS2 Register Summary: [12]

Table 23-767. SLIMBUS_DCT_MAP_j

Address Offset	0x0000 0210 + (0x20 * j)	**Index**	j = 0 to 7 for SLIMBUS1 j = 0 to 3 for SLIMBUS2
Physical Address	0x4902 C210 + (0x20 * j) 0x4012 C210 + (0x20 * j) 0x2 C210 + (0x20 * j) 0x4807 6210 + (0x20 * j)	**Instance**	SLIMBUS1_L3 SLIMBUS1_CORTEX-A9 SLIMBUS1_DSP SLIMBUS2_L3
Description	Associates a device and port to the TX data agent. Write to field FL_CONTROL.validate_dcmap to validate changes.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PN								DI							

Bits	Field Name	Description	Type	Reset
31:14	RESERVED		R	0x00000
13:8	PN	Port Number (PN), identifies the data channel's port for the device. Shall be unique within a device. Note that a half-duplex (bidirectional) port has 2 data agents with the same PN, 1 TX + 1 Rx.	RW	0x00
7:0	DI	Index (DI) of the device this data agent belongs to. Devices are hard-indexed from 0 upwards.	RW	0x00

Table 23-768. Register Call Summary for Register SLIMBUS_DCT_MAP_j

Serial Low-Power Inter-Chip Media Bus Controller

- Device and Adressing Management: [0] [1]
- Data Agent Assignment: [2] [3]
- SLIMBUS1 Register Summary: [4]
- SLIMBUS2 Register Summary: [5]

Table 23-769. SLIMBUS_DCT_CONFIG1_j

Address Offset	0x0000 0214 + (0x20 * j)	**Index**	j = 0 to 7 for SLIMBUS1 j = 0 to 3 for SLIMBUS2
Physical Address	0x4902 C214 + (0x20 * j) 0x4012 C214 + (0x20 * j) 0x2 C214 + (0x20 * j) 0x4807 6214 + (0x20 * j)	**Instance**	SLIMBUS1_L3 SLIMBUS1_CORTEX-A9 SLIMBUS1_DSP SLIMBUS2_L3
Description	TX data agent configuration, applied at the next reconfiguration boundary		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ENABLE	CTS_LAST_VALUE	RESERVED	DT_LPCM	RESERVED								AF				CL	DL					SL					TP_QUALIFIER	TP			

Bits	Field Name	Description	Type	Reset
31	ENABLE	Data agent enabling control. Auto-cleared upon frame or superframe sync loss. Read 0x1: Data agent is enabled Read 0x0: Data agent is disabled	RW	0
30	CTS_LAST_VALUE	Last received value of the CTS TAG bit. Only updated for asynchronous TP, when primary owner (that is, transmitter) of the channel. Read 0x1: Local sink signals TAG.CTS=1 that is, it can receive data (and remote source can transmit some) Read 0x0: Local sink signals TAG.CTS=0 that is, it cannot receive any data (and remote source shall not transmit any)	R	0
29	RESERVED		R	0
28	DT_LPCM	Unsigned-to-OSAM encoding enable for Data Type (DT) = LPCM audio (0x1) 0x0: DT!=0x1: encoding disabled 0x1: DT=0x1: encoding enabled	RW	0
27:20	RESERVED		R	0x00
19:16	AF	Auxillairy Format (AF) used in segment word size calculation. Non-zero values not supported in extended asynchronous TPs. 0xF: User-defined 8-bit AUX (2 AUX slot per segment) 0x0: No AUX information (0 AUX slots per segment) 0x1: ZCUV for tunneling IEC60958 (1 AUX slot per segment) 0xB: User-defined 4-bit AUX (1 AUX slot per segment)	RW	0x0
15	CL	Channel Link (CL) enable: Pairing up of current channel with previous one (that is, channel index below) Tied-0, read-only field for channel index 0, since there is no "previous" channel in that case. TP and segment interval (encoded in SD) must be equal between the linked channels. 0x0: Current channel independent from previous one. 0x1: Current channel paired up with previous one.	RW	0

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Bits	Field Name	Description	Type	Reset
14:10	DL	Segment Data Length (DL), in 4-bit slots (except when 0). AUX + DATA length shall fit in a segment word, that is, 1 to 32 bits. In extended async TPs, sets segment word size (0 and odd values illegal) instead. 0x6: 6 slots (24 bits) 0x1: 1 slot (4 bits) 0x7: 7 slots (28 bits), requiring at most 1 AUX slot to fit in max-size 32-bit segment word 0x0: Length not indicated: Segment slots that are not TAG or AUX are DATA (that is, no unused slot) 0x2: 2 slots (8 bits) 0x8: 8 slots (32 bits), requiring zero AUX slot, to fit in a max-size 32-bit segment word 0x4: 4 slots (16 bits) 0x5: 5 slots (20 bits) 0x3: 3 slots (12 bits)	RW	0x00
9:5	SL	total Segment Length (SL), in 4-bit slots. SL = TAG length + AUX length + DATA length 0x0: Reseved value	RW	0x00
4	TP_QUALIFIER	Qualifier for plain/extended half-duplex asynchronous TPs (owner ID). Unused and don't care for other TPs. 0x0: 1/2 duplex TPs: Local device is primary channel owner, uses T1 token 0x1: 1/2 duplex TPs: Local device is secondary channel owner, uses T2 token	RW	0
3:0	TP	Transport Protocol (TP) Determines also the TAG length (from 0 to 2 slots). 0x6: Extended asynchronous-half-duplex (unicast, 2-slot TAG) 0x1: Pushed (multicast, 1-slot TAG) 0x7: Extended asynchronous-simplex (unicast, 2-slot TAG) 0x0: Isochronous (multicast, no TAG) 0x2: Pulled (unicast, 1-slot TAG) 0x4: Asynchronous-simplex (unicast, 1-slot TAG) 0x5: Asynchronous-half-duplex (unicast, 1-slot TAG) 0xF: User-defined protocol 2 NOT SUPPORTED, RESERVED VALUE 0x3: Locked (multicast, no TAG) NOT SUPPORTED, RESERVED VALUE 0xE: User-defined protocol 1 NOT SUPPORTED, RESERVED VALUE	RW	0x0

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Table 23-770. Register Call Summary for Register SLIMBUS_DCT_CONFIG1_j

Serial Low-Power Inter-Chip Media Bus Controller

- Control and Data Channels: [0] [1] [2] [3]
- SLIMbus Reconfigure Parameters: [4] [5] [6] [7]
- FIFO Management: [8] [9] [10] [11]
- SLIMbus Transfer Protocols: [12] [13] [14] [15] [16] [17]
- Isochronous Transfer Protocol: [18] [19] [20] [21] [22] [23]
- Pushed Transfer Protocol: [24] [25] [26] [27] [28] [29]
- Pulled Transfer Protocol: [30] [31] [32] [33] [34] [35]
- Asynchronous Transfer Protocol: [36] [37] [38] [39] [40] [41]
- Extended Asynchronous Transfer Protocol: [42] [43] [44] [45] [46] [47] [48]
- Paired-up channels: [49] [50] [51] [52] [53]
- Interface Device ISRs: [54] [55]
- Operational Modes Configuration: [56] [57] [58] [59] [60] [61] [62] [63] [64] [65]
- SLIMBUS1 Register Summary: [66]
- SLIMBUS2 Register Summary: [67]

Table 23-771. SLIMBUS_DCT_CONFIG2_j

Address Offset	0x0000 0218 + (0x20 * j)	**Index**	j = 0 to 7 for SLIMBUS1 j = 0 to 3 for SLIMBUS2
Physical Address	0x4902 C218 + (0x20 * j) 0x4012 C218 + (0x20 * j) 0x2 C218 + (0x20 * j) 0x4807 6218 + (0x20 * j)	**Instance**	SLIMBUS1_L3 SLIMBUS1_CORTEX-A9 SLIMBUS1_DSP SLIMBUS2_L3
Description	TX data agent configuration (continued), applied at the next reconfiguration boundary		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				SD											

Bits	Field Name	Description	Type	Reset
31:12	RESERVED		R	0x00000
11:0	SD	Segment Distribution (see *MIPI Alliance Specification for SLIMbus Version 1.01.00*)	RW	0x000

Table 23-772. Register Call Summary for Register SLIMBUS_DCT_CONFIG2_j

Serial Low-Power Inter-Chip Media Bus Controller

- SLIMbus Reconfigure Parameters: [0]
- SLIMbus Transfer Protocols: [1]
- Isochronous Transfer Protocol: [2]
- Pushed Transfer Protocol: [3]
- Pulled Transfer Protocol: [4]
- Asynchronous Transfer Protocol: [5]
- Extended Asynchronous Transfer Protocol: [6]
- Paired-up channels: [7]
- Operational Modes Configuration: [8]
- SLIMBUS1 Register Summary: [9]
- SLIMBUS2 Register Summary: [10]

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Table 23-773. SLIMBUS_DCT_DATA_j

Address Offset	0x0000 021C + (0x20 * j)	**Index**	j = 0 to 7 for SLIMBUS1 j = 0 to 3 for SLIMBUS2
Physical Address	0x4902 C21C + (0x20 * j) 0x4012 C21C + (0x20 * j) 0x2 C21C + (0x20 * j) 0x4807 621C + (0x20 * j)	**Instance**	SLIMBUS1_L3 SLIMBUS1_CORTEX-A9 SLIMBUS1_DSP SLIMBUS2_L3
Description	TX data agent DATA FIFO input. Reads have no effect on FIFO.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															

Bits	Field Name	Description	Type	Reset
31:0	DATA	Data segment word, single-word or packed, LSB or MSB-aligned.	RW	0x0000 0000

Table 23-774. Register Call Summary for Register SLIMBUS_DCT_DATA_j

Serial Low-Power Inter-Chip Media Bus Controller

- Data input/output: manual mode: [0]
- SLIMbus Transfer Procedures: [1] [2]
- SLIMBUS1 Register Summary: [3]
- SLIMBUS2 Register Summary: [4]

Table 23-775. SLIMBUS_DCR_INFO_j

Address Offset	0x0000 0300 + (0x20 * j)	**Index**	j = 0 to 7 for SLIMBUS1 j = 0 to 3 for SLIMBUS2
Physical Address	0x4902 C300 + (0x20 * j) 0x4012 C300 + (0x20 * j) 0x2 C300 + (0x20 * j) 0x4807 6280 + (0x20 * j)	**Instance**	SLIMBUS1_L3 SLIMBUS1_CORTEX-A9 SLIMBUS1_DSP SLIMBUS2_L3
Description	RX data agent status. Write 1 to a bit to clear it.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												HILEVEL	UNDERFLOW	OVERFLOW	DATA_TX_COL

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0000000
3	HILEVEL	Read level of RX data agent FIFO has gone above DMA threshold (that is, reads required to empty FIFO) Write 0x0: No action Write 0x1: Clear pending event, if any Read 0x1: IRQ event pending Read 0x0: No event pending	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
2	UNDERFLOW	Underflow in RX data agent FIFO Write 0x0: No action Write 0x1: Clear pending event, if any Read 0x1: IRQ event pending Read 0x0: No event pending	RW W1toClr	0
1	OVERFLOW	Overflow in RX data agent FIFO Note: never asserted in pulled or async TPs, by construction. Write 0x0: No action Write 0x1: Clear pending event, if any Read 0x1: IRQ event pending Read 0x0: No event pending	RW W1toClr	0
0	DATA_TX_COL	TX collision in RX data agent. Core information element (IE). Write 0x0: No action Write 0x1: Clear pending event, if any Read 0x1: IRQ event pending Read 0x0: No event pending	RW W1toClr	0

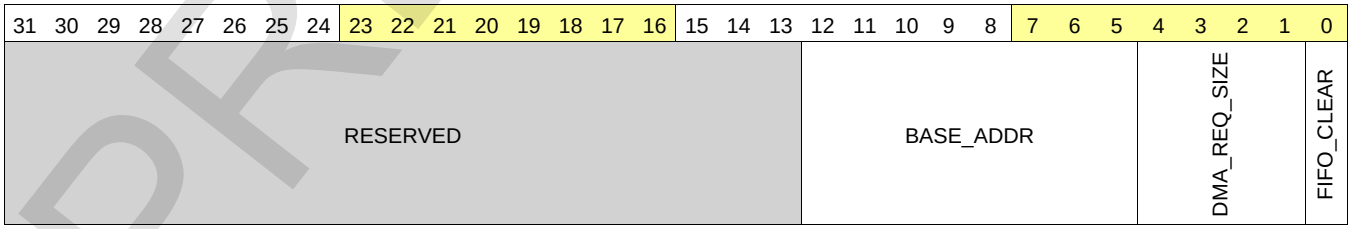
Table 23-776. Register Call Summary for Register SLIMBUS_DCR_INFO_j

Serial Low-Power Inter-Chip Media Bus Controller

- SLIMbus Boot and Reset Procedures: [0]
- Possible Interrupts: [1] [2] [3] [4]
- Data Channel Port ISRs: [5] [6] [7] [8] [9]
- SLIMbus Transfer Procedures: [10] [11]
- SLIMBUS1 Register Summary: [12]
- SLIMBUS2 Register Summary: [13]

Table 23-777. SLIMBUS_DCR_FIFO_SETUP1_j

Address Offset	0x0000 0304 + (0x20 * j)	**Index**	j = 0 to 7 for SLIMBUS1 j = 0 to 3 for SLIMBUS2
Physical Address	0x4902 C304 + (0x20 * j) 0x4012 C304 + (0x20 * j) 0x2 C304 + (0x20 * j) 0x4807 6284 + (0x20 * j)	**Instance**	SLIMBUS1_L3 SLIMBUS1_CORTEX-A9 SLIMBUS1_DSP SLIMBUS2_L3
Description	RX data agent FIFO setup. To be kept static during channel operation.		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000
12:5	BASE_ADDR	RX data agent FIFO base address within shared RX RAM. (physical address of the 32-bit wide RAM array)	RW	0x00

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Bits	Field Name	Description	Type	Reset
4:1	DMA_REQ_SIZE	DMA request size minus 1, in read accesses. In counting (packet) mode, last request may be smaller. Only applicable in precise DMA mode. 0xF: 16 accesses per DMA request 0x0: 1 access per DMA request	RW	0x0
0	FIFO_CLEAR	Returns FIFO to initial empty state. Write 0x0: No effect Write 0x1: Clear FIFO Read 0x1: Ongoing Clear. Completion requires the SLIMbus clock. Read 0x0: No event, last clear completed	RW	0

Table 23-778. Register Call Summary for Register SLIMBUS_DCR_FIFO_SETUP1_j

Serial Low-Power Inter-Chip Media Bus Controller

- FIFO Mapping: [0]
- FIFO Configuration: [1] [2]
- Operational Modes Configuration: [3] [4] [5]
- SLIMbus Transfer Procedures: [6] [7]
- SLIMBUS1 Register Summary: [8]
- SLIMBUS2 Register Summary: [9]

Table 23-779. SLIMBUS_DCR_FIFO_SETUP2_j

Address Offset	0x0000 0308 + (0x20 * j)	**Index**	j = 0 to 7 for SLIMBUS1 j = 0 to 3 for SLIMBUS2
Physical Address	0x4902 C308 + (0x20 * j) 0x4012 C308 + (0x20 * j) 0x2 C308 + (0x20 * j) 0x4807 6288 + (0x20 * j)	**Instance**	SLIMBUS1_L3 SLIMBUS1_CORTEX-A9 SLIMBUS1_DSP SLIMBUS2_L3
Description	RX data agent FIFO setup, continued. To be kept static during channel operation.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PACKING	MSB_ALIGNED	RESERVED						DMA_THRESHOLD								SB_THRESHOLD								SIZE							

Bits	Field Name	Description	Type	Reset
31	PACKING	Packing enable control 0x0: Packing disabled: one segment word per read access. Byte enable is don't care. 0x1: Packing enabled: one or several segment words per read access, depending on segment word size and byte enable. Only works in LSB-aligned mode. Behaviour in LSB-aligned mode is undefined.	RW	0
30	MSB_ALIGNED	PLACEHOLDER, NO EFFECT: DATA ALWAYS LSB-aligned LSB/MSB-alignment of FIFO output (read) RX data. 0x0: Output data is LSB-aligned 0x1: Output data is MSB-aligned	RW	0
29:24	RESERVED		R	0x00

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Bits	Field Name	Description	Type	Reset
23:16	DMA_THRESHOLD	SW-side RX data agent FIFO threshold. DMA read requests get (re-)asserted when RD_LEVEL is above threshold. Range: 0 to SIZE field value (included). 0xFF: DMA reads requested whenever FIFO is full (assuming maximum FIFO size) 0x0: DMA reads requested whenever FIFO is not empty	RW	0x00
15:8	SB_THRESHOLD	SLIMbus-side RX data agent FIFO threshold, used for SLIMbus reception. 0xFF: Threshold condition = FIFO is full (assuming maximum FIFO size) 0x0: Threshold condition = FIFO is not empty	RW	0x00
7:0	SIZE	Capacity of FIFO in segment words, minus one. 0xFF: Maximum FIFO size 0x0: FIFO is 1-word deep (not recommended) 0x3: FIFO is 4-word deep. Recommended minimum setting (SLIMbus protocol).	RW	0x00

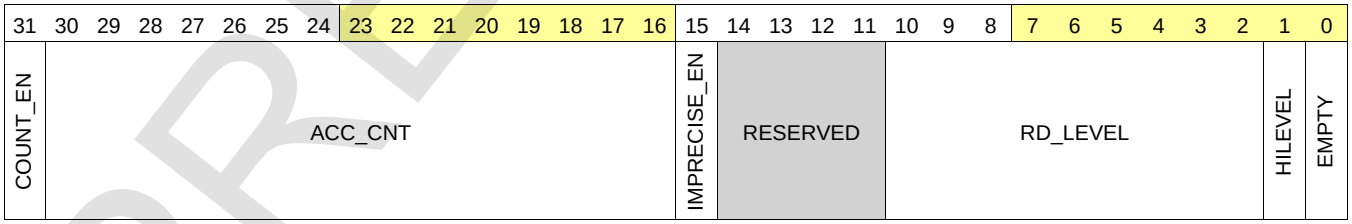
Table 23-780. Register Call Summary for Register SLIMBUS_DCR_FIFO_SETUP2_j

Serial Low-Power Inter-Chip Media Bus Controller

- FIFO Mapping: [0]
- FIFO Status: [1]
- FIFO Configuration: [2] [3] [4] [5]
- Operational Modes Configuration: [6] [7] [8]
- SLIMbus Transfer Procedures: [9] [10] [11] [12] [13]
- SLIMBUS1 Register Summary: [14]
- SLIMBUS2 Register Summary: [15]

Table 23-781. SLIMBUS_DCR_FIFO_STATUS_j

Address Offset	0x0000 030C + (0x20 * j)	**Index**	j = 0 to 7 for SLIMBUS1 j = 0 to 3 for SLIMBUS2
Physical Address	0x4902 C30C + (0x20 * j) 0x4012 C30C + (0x20 * j) 0x2 C30C + (0x20 * j) 0x4807 628C + (0x20 * j)	**Instance**	SLIMBUS1_L3 SLIMBUS1_CORTEX-A9 SLIMBUS1_DSP SLIMBUS2_L3
Description	RX data agent FIFO status, for software (non-DMA) FIFO management.		
Type	RW		



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Bits	Field Name	Description	Type	Reset
31	COUNT_EN	Down-counter mode control. Only applicable in precise DMA mode. Write 0x0: Disable down-counter mode. Should typically be used only when ACC_CNT = 0. If ACC_CNT 0, DMA request gets deasserted immediately. Write 0x1: Enable down-counter mode. ACC_CNT is typically set to the desired value in the same write access. Read 0x1: Down-counter mode is enabled: DMA request can only be active when ACC_CNT 0 Read 0x0: Down-counter mode is disabled: DMA request follows FIFO level, and is active during no-transmission periods.	RW	0
30:16	ACC_CNT	"Packet mode" down-counter of segment words, decremented on DCR_DATA read accesses. In that mode, DMA request shall reassert when ACC_CNT = RD_LEVEL (that is, whole packet received). Write 0x0: Deasserts current DMA request by forcing the count to zero (not typical operation) Write 0x7F: Set largest packet size (in accesses) to transfer before DMA request deassertion. Any lower value is also valid to enter. Read 0x7F: Maximum number of accesses still to be transferred before DMA deassertion. Unless interrupted, counter shall go through all values down to zero. Read 0x0: No access left to transfer, DMA request currently inactive.	RW	0x0000
15	IMPRECISE_EN	Precise vs. Imprecise DMA requesting mode control. (A DMA request is a single assertion-deassertion cycle.) 0x0: DMA request contains a defined number of accesses 0x1: DMA request is not expected to trigger a fixed number of accesses	RW	0
14:11	RESERVED		R	0x0
10:2	RD_LEVEL	Number of segment words stored in FIFO, that can be read out. Read 0x100: FIFO is full of readable words (assuming maximum size) Read 0x0: FIFO contains no readable word	R	0x000
1	HILEVEL	Indicator of read level (RD_LEVEL: number of readable segment words) with respect to (read) threshold (DMA_THRESHOLD). Activates DMA read requests when high. Read 0x1: RD_LEVEL DMA_THRESHOLD Read 0x0: RD_LEVEL = DMA_THRESHOLD	R	0
0	EMPTY	FIFO empty indicator Read 0x1: FIFO contains no readable word (RD_LEVEL = 0) Read 0x0: FIFO contains at least one readable word (RD_LEVEL 0)	R	1

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Table 23-782. Register Call Summary for Register SLIMBUS_DCR_FIFO_STATUS_j

Serial Low-Power Inter-Chip Media Bus Controller

- FIFO Status: [0] [1] [2]
- FIFO Configuration: [3] [4] [5] [6] [7]
- SLIMbus Transfer Procedures: [8] [9] [10]
- SLIMBUS1 Register Summary: [11]
- SLIMBUS2 Register Summary: [12]

Table 23-783. SLIMBUS_DCR_MAP_j

Address Offset	0x0000 0310 + (0x20 * j)	**Index**	j = 0 to 7 for SLIMBUS1 j = 0 to 3 for SLIMBUS2
Physical Address	0x4902 C310 + (0x20 * j) 0x4012 C310 + (0x20 * j) 0x2 C310 + (0x20 * j) 0x4807 6290 + (0x20 * j)	**Instance**	SLIMBUS1_L3 SLIMBUS1_CORTEX-A9 SLIMBUS1_DSP SLIMBUS2_L3
Description	Associates a device and port to the RX data agent. Write to field FL_CONTROL[8] VALIDATE_DCMAP to validate changes.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PN								DI							

Bits	Field Name	Description	Type	Reset
31:14	RESERVED		R	0x00000
13:8	PN	Port Number (PN), identifies the data channel's port for the device. Shall be unique within a device. Note that a half-duplex (bidirectional) port has 2 data agents with the same PN, 1 TX + 1 Rx.	RW	0x00
7:0	DI	Index (DI) of the device this data agent belongs to. Devices are hard-indexed from 0 upwards.	RW	0x00

Table 23-784. Register Call Summary for Register SLIMBUS_DCR_MAP_j

Serial Low-Power Inter-Chip Media Bus Controller

- Device and Adressing Management: [0] [1]
- Data Agent Assignment: [2] [3]
- SLIMBUS1 Register Summary: [4]
- SLIMBUS2 Register Summary: [5]

Table 23-785. SLIMBUS_DCR_CONFIG1_j

Address Offset	0x0000 0314 + (0x20 * j)	**Index**	j = 0 to 7 for SLIMBUS1 j = 0 to 3 for SLIMBUS2
Physical Address	0x4902 C314 + (0x20 * j) 0x4012 C314 + (0x20 * j) 0x2 C314 + (0x20 * j) 0x4807 6294 + (0x20 * j)	**Instance**	SLIMBUS1_L3 SLIMBUS1_CORTEX-A9 SLIMBUS1_DSP SLIMBUS2_L3
Description	RX data agent configuration, applied at the next reconfiguration boundary		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ENABLE	CTS_FORCE_VALUE	CTS_FORCE_EN	DT_LPCM	RESERVED								AF				CL	DL					SL					TP_QUALIFIER	TP			

Bits	Field Name	Description	Type	Reset
31	ENABLE	Data agent enabling control. Auto-cleared upon frame or superframe sync loss. 0x0: Data agent is disabled 0x1: Data agent is enabled	RW	0
30	CTS_FORCE_VALUE	Value to force the CTS TAG bit value when in asynchronous TP and secondary channel owner (that is, receiver) and CTS is forced (CTS_force_en=1) Don't care in all other cases. Warning: forcing CTS=1 can result in a FIFO overflow. 0x0: Local sink signals TAG.CTS=0 that is, it cannot receive any data (and remote source shall not transmit any) 0x1: Local sink signals TAG.CTS=1 that is, it can receive data (and remote source can transmit some)	RW	0
29	CTS_FORCE_EN	Forces the CTS TAG bit value when in an asynchronous TP and secondary owner (that is, receiver) of the channel. Don't care in other cases. 0x0: CTS bit generated according to RX FIFO level 0x1: CTS bit forced to CTS_force_value	RW	0
28	DT_LPCM	OSAM-to-unsigned decoding enable for Data Type (DT) = LPCM audio (0x1) 0x0: DT!=0x1: decoding disabled 0x1: DT=0x1: decoding enabled	RW	0
27:20	RESERVED		R	0x00
19:16	AF	Auxillairy Format (AF) used in segment word size calculation. Non-zero values not supported in extended asynchronous TPs. 0xF: User-defined 8-bit AUX (2 AUX slot per segment) 0x0: No AUX information (0 AUX slots per segment) 0x1: ZCUV for tunneling IEC60958 (1 AUX slot per segment) 0xB: User-defined 4-bit AUX (1 AUX slot per segment)	RW	0x0
15	CL	Channel Link (CL) enable: Pairing up of current channel with previous one (that is, channel index below) Channel index 0 should have CL=0, since there is no "previous" channel in that case. TP and segment interval (encoded in SD) must be equal between the linked channels. 0x0: Current channel independent from previous one. 0x1: Current channel paired up with previous one.	RW	0

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Bits	Field Name	Description	Type	Reset
14:10	DL	Segment Data Length (DL), in 4-bit slots (except when 0). AUX + DATA length shall fit in a segment word, that is, 1 to 32 bits. In extended async TPs, sets segment word size (0 and odd values illegal) instead. 0x6: 6 slots (24 bits) 0x1: 1 slot (4 bits) 0x7: 7 slots (28 bits), requiring at most 1 AUX slot to fit in max-size 32-bit segment word 0x0: Length not indicated: Segment slots that are not TAG or AUX are DATA (that is, no unused slot) 0x2: 2 slots (8 bits) 0x8: 8 slots (32 bits), requiring zero AUX slot, to fit in a max-size 32-bit segment word 0x4: 4 slots (16 bits) 0x5: 5 slots (20 bits) 0x3: 3 slots (12 bits)	RW	0x00
9:5	SL	total Segment Length (SL), in 4-bit slots. SL = TAG length + AUX length + DATA length 0x0: Reseved value	RW	0x00
4	TP_QUALIFIER	Qualifier for plain/extended half-duplex asynchronous TPs (owner ID). Unused and don't care for other TPs 0x0: 1/2 duplex TPs: Local device is primary channel owner, uses T1 token 0x1: 1/2 duplex TPs: Local device is secondary channel owner, uses T2 token	RW	0
3:0	TP	Transport Protocol (TP) Determines also the TAG length (from 0 to 2 slots). 0x6: Extended asynchronous-half-duplex (unicast, 2-slot TAG) 0x1: Pushed (multicast, 1-slot TAG) 0x7: Extended asynchronous-simplex (unicast, 2-slot TAG) 0x0: Isochronous (multicast, no TAG) 0x2: Pulled (unicast, 1-slot TAG) 0x4: Asynchronous-simplex (unicast, 1-slot TAG) 0x5: Asynchronous-half-duplex (unicast, 1-slot TAG) 0xF: User-defined protocol 2 NOT SUPPORTED, RESERVED VALUE 0x3: Locked (multicast, no TAG) NOT SUPPORTED, RESERVED VALUE 0xE: User-defined protocol 1 NOT SUPPORTED, RESERVED VALUE	RW	0x0

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Table 23-786. Register Call Summary for Register SLIMBUS_DCR_CONFIG1_j

Serial Low-Power Inter-Chip Media Bus Controller

- Control and Data Channels: [0] [1] [2] [3]
- SLIMbus Reconfigure Parameters: [4] [5] [6] [7]
- FIFO Management: [8] [9] [10] [11]
- SLIMbus Transfer Protocols: [12] [13] [14] [15] [16] [17] [18] [19]
- Isochronous Transfer Protocol: [20] [21] [22] [23] [24] [25] [26] [27]
- Pushed Transfer Protocol: [28] [29] [30] [31] [32] [33] [34] [35]
- Pulled Transfer Protocol: [36] [37] [38] [39] [40] [41] [42] [43]
- Asynchronous Transfer Protocol: [44] [45] [46] [47] [48] [49] [50] [51]
- Extended Asynchronous Transfer Protocol: [52] [53] [54] [55] [56] [57] [58] [59] [60]
- Paired-up channels: [61] [62] [63] [64] [65]
- Interface Device ISRs: [66] [67]
- Operational Modes Configuration: [68] [69] [70] [71] [72] [73] [74] [75] [76] [77]
- SLIMBUS1 Register Summary: [78]
- SLIMBUS2 Register Summary: [79]

Table 23-787. SLIMBUS_DCR_CONFIG2_j

Address Offset	0x0000 0318 + (0x20 * j)	**Index**	j = 0 to 7 for SLIMBUS1 j = 0 to 3 for SLIMBUS2
Physical Address	0x4902 C318 + (0x20 * j) 0x4012 C318 + (0x20 * j) 0x2 C318 + (0x20 * j) 0x4807 6298 + (0x20 * j)	**Instance**	SLIMBUS1_L3 SLIMBUS1_CORTEX-A9 SLIMBUS1_DSP SLIMBUS2_L3
Description	RX data agent configuration (continued), applied at the next reconfiguration boundary		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				SD											

Bits	Field Name	Description	Type	Reset
31:12	RESERVED		R	0x00000
11:0	SD	Segment Distribution	RW	0x000

Table 23-788. Register Call Summary for Register SLIMBUS_DCR_CONFIG2_j

Serial Low-Power Inter-Chip Media Bus Controller

- SLIMbus Reconfigure Parameters: [0]
- SLIMbus Transfer Protocols: [1]
- Isochronous Transfer Protocol: [2]
- Pushed Transfer Protocol: [3]
- Pulled Transfer Protocol: [4]
- Asynchronous Transfer Protocol: [5]
- Extended Asynchronous Transfer Protocol: [6]
- Paired-up channels: [7]
- Operational Modes Configuration: [8]
- SLIMBUS1 Register Summary: [9]
- SLIMBUS2 Register Summary: [10]

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Table 23-789. SLIMBUS_DCR_DATA_j

Address Offset	0x0000 031C + (0x20 * j)	**Index**	j = 0 to 7 for SLIMBUS1 j = 0 to 3 for SLIMBUS2
Physical Address	0x4902 C31C + (0x20 * j) 0x4012 C31C + (0x20 * j) 0x2 C31C + (0x20 * j) 0x4807 629C + (0x20 * j)	**Instance**	SLIMBUS1_L3 SLIMBUS1_CORTEX-A9 SLIMBUS1_DSP SLIMBUS2_L3
Description	RX data agent DATA FIFO output. Writes have no effect on FIFO.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															

Bits	Field Name	Description	Type	Reset
31:0	DATA	Data segment word, single-word or packed, LSB or MSB-aligned.	R	0x0000 0000

Table 23-790. Register Call Summary for Register SLIMBUS_DCR_DATA_j

Serial Low-Power Inter-Chip Media Bus Controller

- Data input/output: manual mode: [0]
- SLIMbus Transfer Procedures: [1] [2]
- SLIMBUS1 Register Summary: [3]
- SLIMBUS2 Register Summary: [4]

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23.10 MIPI-HSI

This section describes the MIPI high-speed synchronous serial interface (HSI).

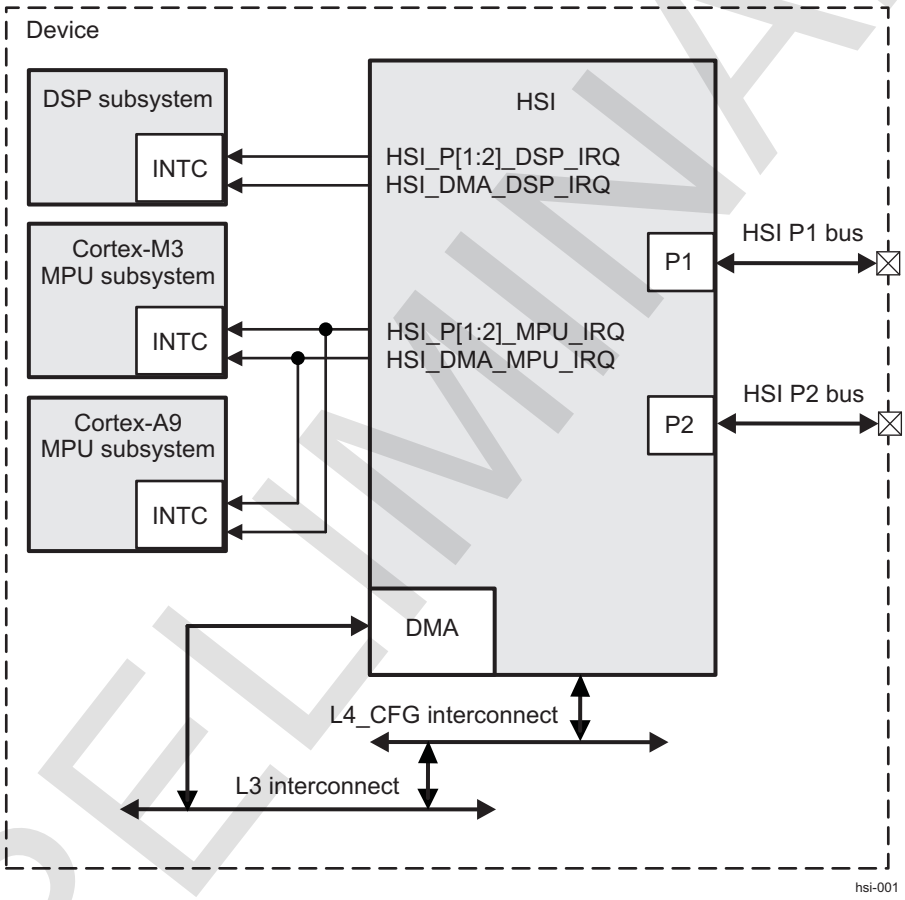
23.10.1 HSI Overview

The MIPI HSI module is a multichannel and full-duplex serial communications interface, composed of two transmitters (HST) in charge of the transmitted information and two receivers (HSR) in charge of the received information, sharing a 16-channel DMA.

The HSI peripheral is typically used to enable the device to exchange information with an external cellular modem.

Figure 23-217 is an overview of the HSI module.

Figure 23-217. HSI Overview



HSI supports the following features:

- Full duplex
- No static clock matching
- Interface speed up to 192 Mbps on transmitter and up to 225 Mbps on receiver
- Transmission speed and operation mode dynamically configurable
- Logical channels:
  - Up to 16 logical channels on receiver
  - Up to 16 logical channels on transmitter
- One 32-request DMA engine:
  - 16 transmit + 16 receive requests from HSI port

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- 16 logical DMA channels

- Interrupt requests:
  - Three to each processor subsystem (two from HSI port, one from DMA)

23.10.2 HSI Environment

This section describes the HSI application fields from an environment point of view (external connections).

23.10.2.1 HSI Signals

Table 23-791 describes the HSI module I/O signals.

Table 23-791. HSI I/O Signals

Pin Name	I/O [1]	Description	Reset Value
hsi1_cawake	I	HSI port 1 wake-up signal from an external serial transmitter	HiZ
hsi1_cadata	I	HSI port 1 receiver data from an external transmitter	HiZ
hsi1_caflag	I	HSI port 1 receiver flag from an external transmitter	HiZ
hsi1_acready	O	HSI port 1 synchronization signal to an external transmitter	1
hsi1_acwake	O	HSI port 1 wake-up signal to an external serial receiver	0
hsi1_acdata	O	HSI port 1 transmission data (level transmission signaling) to an external receiver	0
hsi1_acflag	O	HSI port 1 transmission flag (bit transition signaling) to an external receiver	1
hsi1_caready	I	HSI port 1 synchronization signal from an external receiver	HiZ
hsi2_cawake	I	HSI port 2 wake-up signal from an external serial transmitter	HiZ
hsi2_cadata	I	HSI port 2 receiver data from an external transmitter	HiZ
hsi2_caflag	I	HSI port 2 receiver flag from an external transmitter	HiZ
hsi2_acready	O	HSI port 2 synchronization signal to an external transmitter	HiZ
hsi2_acwake	O	HSI port 2 wake-up signal to an external serial receiver	HiZ
hsi2_acdata	O	HSI port 2 transmission data (level transmission signaling) to an external receiver	HiZ
hsi2_acflag	O	HSI port 2 transmission flag (bit transition signaling) to an external receiver	HiZ
hsi2_caready	I	HSI port 2 synchronization signal from an external receiver	HiZ

[1] I = input; O = output

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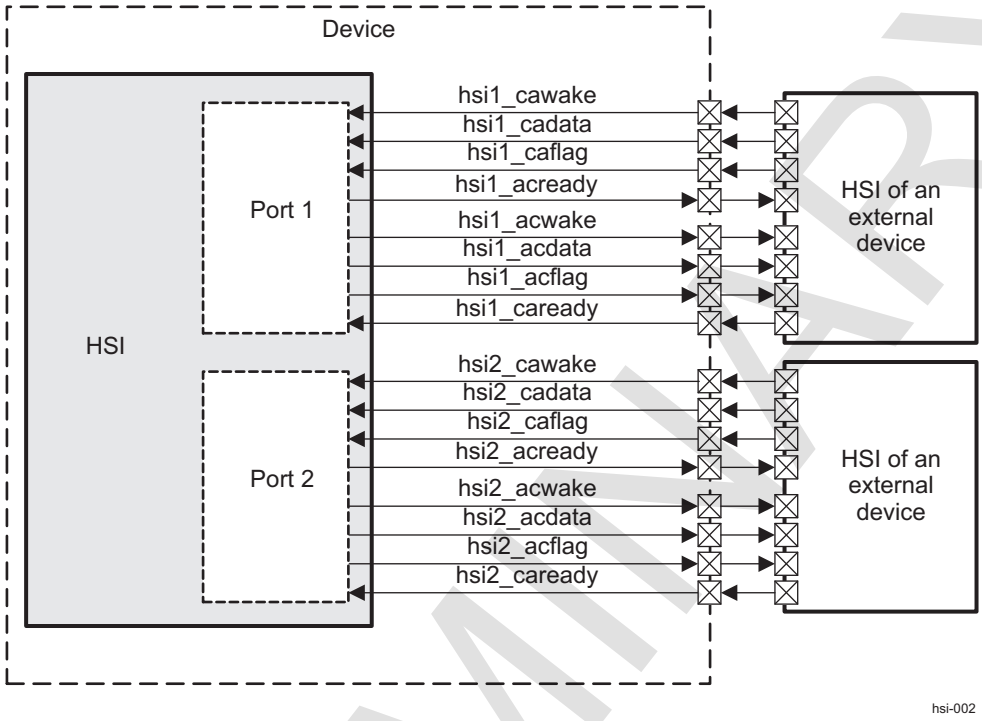
23.10.2.2 HSI Typical Application

Figure 23-218 shows the HSI typical application.

Figure 23-218. HSI Typical Application



23.10.3 HSI Integration

This section describes module integration in the device, including information about clocks, resets, and hardware requests.

Figure 23-219 shows the HSI module integration.

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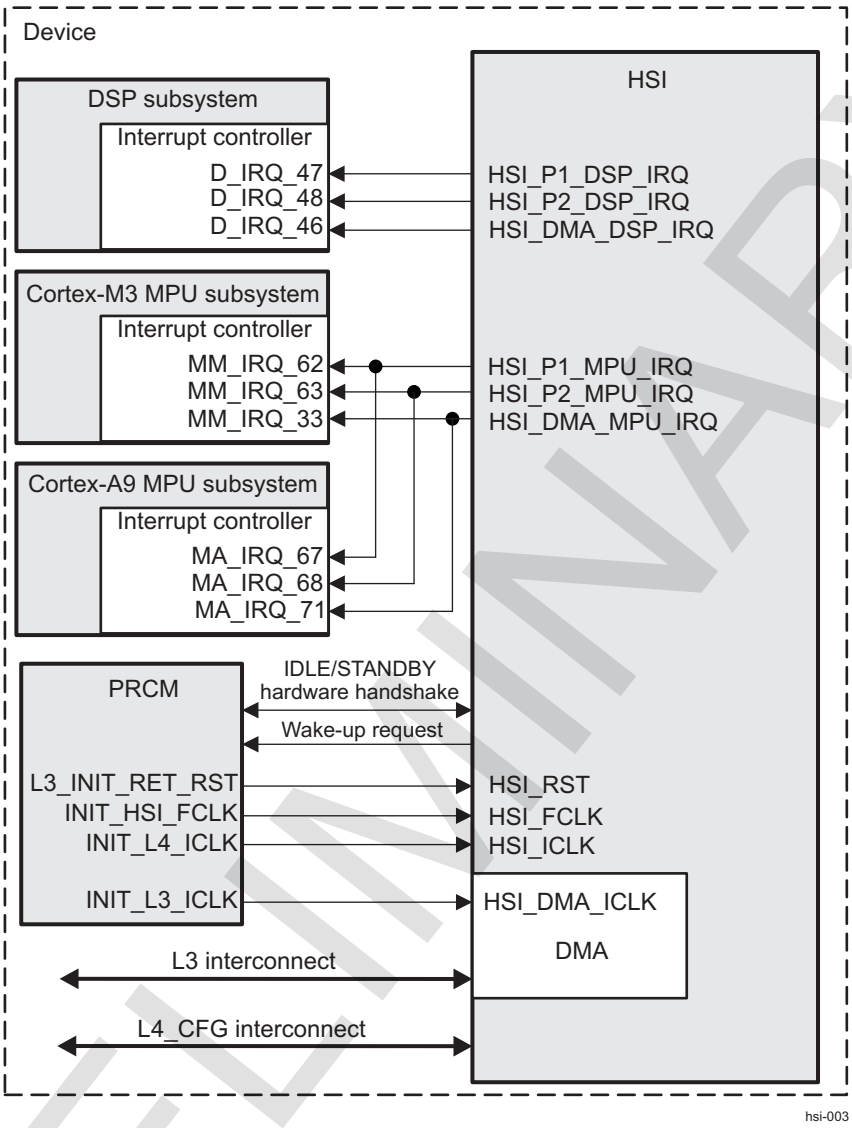
Figure 23-219. HSI Integration



NOTE: For more information about the IDLE/STANDBY hardware handshake and the wake-up request, see Section 3.1.1.1.2, *Module Level Clock Management*, in Chapter 3, *Power, Reset, and Clock Management*.

Interrupt lines HSI_P[1:2]_MPU_IRQ and HSI_DMA_MPU_IRQ are shared between the Cortex-A9 MPU and Cortex-M3 MPU INTCs. It is strongly recommended to unmask each interrupt source in only one INTC at a time.

Table 23-792 through Table 23-794 summarize the integration of the module in the device.

Table 23-792. Integration Attributes

Module Instance	Attributes		
	Power Domain	Wake-Up Capability	Interconnect
HSI	PD_L3_INIT	NA	L3 L4_CFG

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Table 23-793. Clocks and Resets

Clocks				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
HSI	HSI_FCLK	INIT_HSI_FCLK	PRCM	HSI module functional clock
	HSI_ICLK	INIT_L4_ICLK	PRCM	HSI module interface clock
	HSI_DMA_ICLK	INIT_L3_ICLK	PRCM	HSI DMA engine interface clock
Resets				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
HSI	HSI_RST	L3_INIT_RET_RST	PRCM	HSI module asynchronous reset

Table 23-794. Hardware Requests

Interrupt Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
HSI	HSI_DMA_MPU_IRQ(1)	MM_IRQ_33	Cortex-M3	HSI DMA engine MPU request
	HSI_P1_MPU_IRQ(1)	MM_IRQ_62	Cortex-M3	HSI MPU request – Port 1
	HSI_P2_MPU_IRQ(1)	MM_IRQ_63	Cortex-M3	HSI MPU request – Port 2
	HSI_DMA_DSP_IRQ	D_IRQ_46	DSP	HSI DMA engine DSP request
	HSI_P1_DSP_IRQ	D_IRQ_47	DSP	HSI DSP request – Port 1
	HSI_P2_DSP_IRQ	D_IRQ_48	DSP	HSI DSP request – Port 2
	HSI_DMA_MPU_IRQ(1)	MA_IRQ_71	Cortex-A9	HSI DMA engine MPU request
	HSI_P1_MPU_IRQ(1)	MA_IRQ_67	Cortex-A9	HSI MPU request – Port 1
	HSI_P2_MPU_IRQ(1)	MA_IRQ_68	Cortex-A9	HSI MPU request – Port 2
No DMA Requests				

(1) Interrupts shared between the Cortex-A9 MPU INTC and Cortex-M3 MPU INTC

NOTE: For a description of interrupt sources, see Section 23.10.4.5, *Interrupt Requests*.

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23.10.4 HSI Functional Description

NOTE: In the functional description section, the following common internal signal names are used for the corresponding external HSI signals (for simplification):

- WAKE: hsi1_cawake, hsi1_acwake, hsi2_cawake, and hsi2_acwake
- DATA: hsi1_cadata, hsi1_acdata, hsi2_cadata, and hsi2_acdata
- FLAG: hsi1_caflag, hsi1_acflag, hsi2_caflag, and hsi2_acflag
- READY: hsi1_acready, hsi1_caready, hsi2_acready, and hsi2_caready

23.10.4.1 Block Diagram

The HSI controller is a subsystem built around two full-duplex multichannel synchronous serial interfaces. It contains a 16-bidirectional-logical-channel DMA in charge of handling data transfers between HSI modules and the L3 interconnect. Interrupt access to data is also available.

NOTE: Transmit data cannot be read back, and received data cannot be written in DMA and IRQ-based transfers.

Figure 23-220 shows most HSI module features.

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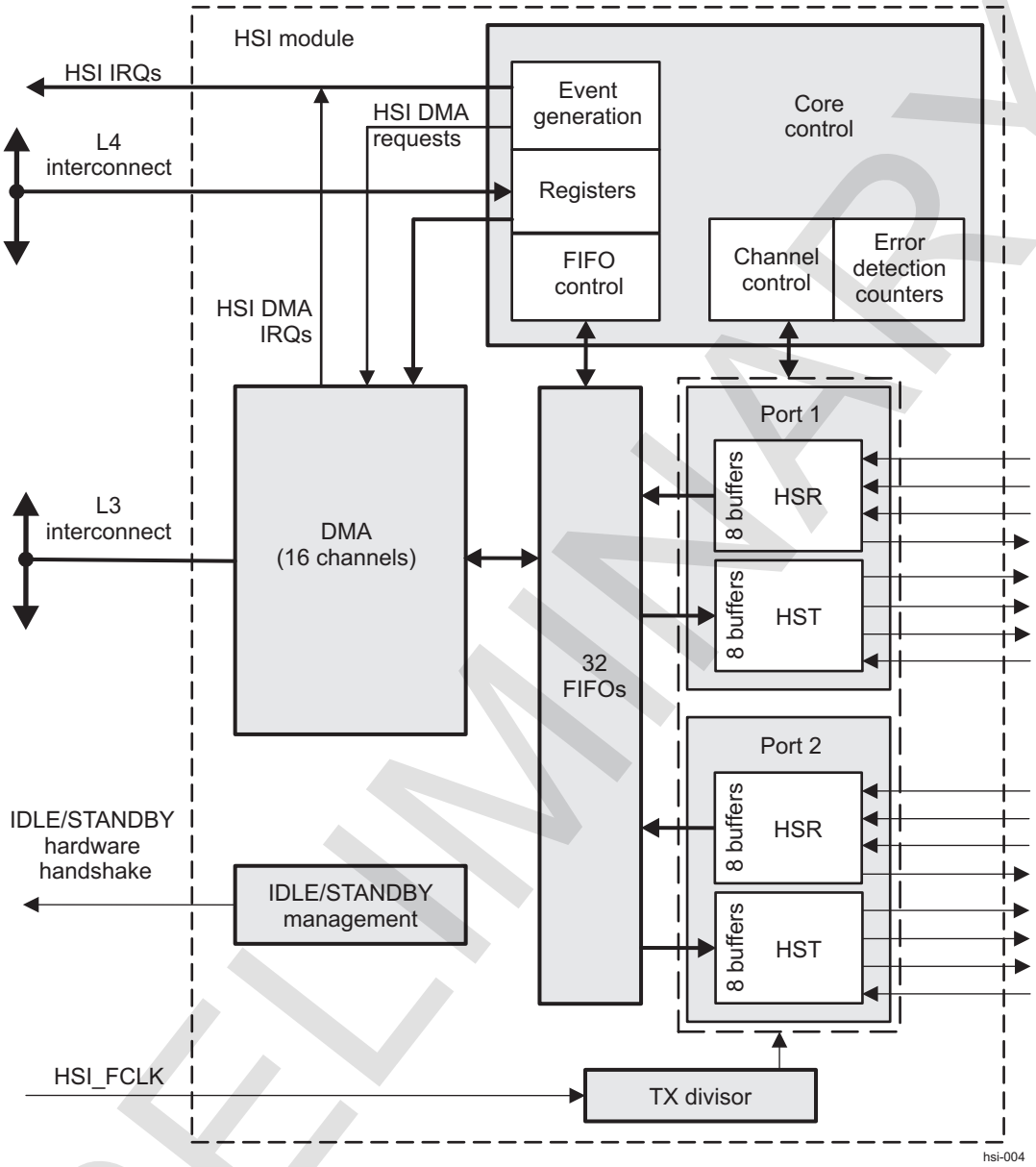
Figure 23-220. HSI Controller Architecture Overview



NOTE: A bypass path in the DMA allows a processor (MPU or DSP) to retrieve or provide data received or to be transmitted on an interrupt triggered access, when the DMA is not enabled.

23.10.4.2 Clock Configuration

The HSI module has four fully asynchronous clock domains:

- Interface clock domain
- Functional clock domain
- Receive clock domain on port 1
- Receive clock domain on port 2

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23.10.4.2.1 Interface Clock Domain

The following clocks are part of the interface clock domain:

- HSI_DMA_ICLK runs the interface master port (L3). This clock is used for DMA master access to the L3 interconnect and also serves as the DMA functional clock.
- HSI_ICLK runs the interface slave port (L4). This clock is used to configure the module and to transmit and receive data through register access in an interrupt-based manner.

23.10.4.2.2 Functional Clock Domain

The functional clock (HSI_FCLK) runs the transmitter/receiver logic.

23.10.4.2.2.1 Transmit Clock

The transmit clock is obtained from the functional clock and is used to generate transmitter DATA and FLAG lines, according to the standard. Namely, the DATA line must always reflect the transmitted bit value, whereas the FLAG line must provide a transition (0 to 1, or 1 to 0) when the current DATA value is the same as the previous one.

The transmit data rate is programmable through the HST_DIVISOR_Pp[7:0] TX_RATE_DIV_VAL bit field.

Transmit clock = HSI_FCLK / (TX_RATE_DIV_VAL + 1).

23.10.4.2.2.2 Receive Error Detection Counters Clocks

The functional clock is also used to obtain clocks for receive error counters, which are independently divided versions of the functional clock. Division is set by software through the HSR_DIVISOR_Pp[7:0] RX_RATE_DIV_VAL bit field, which sets the bit rate clock for the frame time-out counter. This clock is further divided to generate an edge per frame to be sent to the frame burst counter.

23.10.4.2.3 Receive Clock Domain (Port 1 and Port 2)

The RX clock is retrieved from the DATA and FLAG signals available on the serial interface. A self-clocked source synchronous receiver implementation is done as follows: simple XOR of the DATA and FLAG signals recovers a signal displaying a transition on every bit time. From this signal, two clocks are generated with the appropriate phase, which can recover bit values, by sampling the DATA line, where the transmitted bit is always available.

23.10.4.3 Software Reset

The HSI module can be reset by software through the HSI_SYSCONFIG[1] SOFTRESET bit. Setting this bit to 1 enables an active global software reset that is functionally equivalent to a hardware reset. The HSI_SYSSTATUS[0] RESETDONE bit indicates that the software reset is complete when its value is set to 1. Software must ensure that the software reset completes before performing HSI operations.

The DMA engine can be independently reset by software through the DMA_GRST[0] SWRESET bit. Setting this bit to 1 resets the DMA registers and logic. This bit is automatically cleared when the DMA reset completes.

23.10.4.4 Power Management

Table 23-795 describes power-management features available for the HSI module.

NOTE: For descriptions of IdleMode and StandbyMode features, see Section 3.1.1.1.2, *Module-Level Clock Management*, in Chapter 3, *Power, Reset, and Clock Management*.

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Table 23-795. Local Power-Management Features

Feature	Registers	Description
Clock auto gating	HSI_SYSCONFIG[0] AUTOIDLE	This bit allows a local power optimization inside the module by gating the HSI_ICLK clock upon the interface activity.
	DMA_GCR[3] AUTOGATING	This bit allows a local power optimization inside the module by gating the HSI_DMA_ICLK clock upon the interface activity.
Slave idle modes	HSI_SYSCONFIG[4:3] SIDLEMODE	Force-idle, no-idle, smart-idle, and smart-idle wakeup-capable modes are available.
Master standby modes	HSI_SYSCONFIG[13:12] MIDLEMODE	Force-standby, no-standby, smart-standby, and smart-standby wake-up modes are available.

23.10.4.4.1 HSI Module Power-Management Modes

23.10.4.4.1.1 Standby

When asserted, this signal informs the PRCM module that HSI is quiet and does not generate any traffic on the interconnect.

The HSI module supports four STANDBY handshake modes, selected through the HSI_SYSCONFIG[13:12] MIDLEMODE bit field:

- Force-standby (0x0): Selecting this mode asserts the standby signal unconditionally of the HSI activity. Software must ensure that HSI is disabled and does not generate any activity before activating this mode.
- No-standby (0x1): Standby signal is never asserted.
- Smart-standby (0x2): Standby signal is asserted when internal HSI DMA does not generate activity anymore (namely, upon DMA idle acknowledge signal assertion).
- Smart-standby wakeup (0x3): Standby signal is asserted when internal HSI DMA does not generate activity anymore (namely, upon DMA idle acknowledge signal assertion). It can also generate a wake-up request.

23.10.4.4.1.2 Idle

The PRCM module asserts an IDLE request signal when it requires the HSI slave port to be idled. Any access to this port after the IDLE request signal has been asserted generates an error.

The HSI module supports four IDLE handshake modes, selected through the HSI_SYSCONFIG[4:3] SIDLEMODE bit field:

- Force-idle (0x0): An IDLE request is acknowledged unconditionally.
- No-idle (0x1): An IDLE request is never acknowledged.
- Smart-idle (0x2): Acknowledgment to an IDLE request is given based on the internal HSI module activity.
- Smart-idle wakeup (0x3): Acknowledgment to an IDLE request is given based on the internal HSI module activity. Additionally, when in this mode, the HSI module is allowed to generate a wake-up request.

23.10.4.4.1.3 Auto-Idle

The HSI module provides an auto-idle option for the interface clock domain. Auto-idle mode is enabled by setting the HSI_SYSCONFIG[0] AUTOIDLE and/or DMA_GCR[3] AUTOGATING bits to 1. When this mode is enabled and there is no activity on the interconnect interface, the interface clock is disabled internally to the module to reduce power consumption. When there is new activity on the interconnect interface, the interface clock is restarted without any latency penalty.

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23.10.4.4.1.4 DMA Engine Switch Off Mode

The DMA interface clock (HSI_DMA_ICLK) can be switched off by setting the DMA_GCR[0] SWITCH_OFF bit to 1. DMA clock activity is then cut off. Software must ensure that ongoing transitions are complete before cutting off clocks. Once the DMA is switched off, access to reset this bit is possible only through the configuration port.

23.10.4.5 Interrupt Requests

Table 23-796 lists the event flags, and their mask, that can cause module interrupts.

Table 23-796. Events

Event Flag	Event Mask	Map to	Description
HSI_Pp_M_IRQrU_STATUS[26] HSR_WAKE	HSI_Pp_M_IRQrU_ENABLE[26] HSR_WAKE	HSI_P1_MPU_IRQ HSI_P2_MPU_IRQ	Wake detected on any channel 8–15.
HSI_Pp_D_IRQrU_STATUS[26] HSR_WAKE	HSI_Pp_D_IRQrU_ENABLE[26] HSR_WAKE	HSI_P1_DSP_IRQ HSI_P2_DSP_IRQ	
HSI_Pp_M_IRQrU_STATUS[25] HSR_BREAK	HSI_Pp_M_IRQrU_ENABLE[25] HSR_BREAK	HSI_P1_MPU_IRQ HSI_P2_MPU_IRQ	Break detected on any channel 8–15.
HSI_Pp_D_IRQrU_STATUS[25] HSR_BREAK	HSI_Pp_D_IRQrU_ENABLE[25] HSR_BREAK	HSI_P1_DSP_IRQ HSI_P2_DSP_IRQ	
HSI_Pp_M_IRQrU_STATUS[24] HSR_ERROR	HSI_Pp_M_IRQrU_ENABLE[24] HSR_ERROR	HSI_P1_MPU_IRQ HSI_P2_MPU_IRQ	Error detected on any channel 8–15
HSI_Pp_D_IRQrU_STATUS[24] HSR_ERROR	HSI_Pp_D_IRQrU_ENABLE[24] HSR_ERROR	HSI_P1_DSP_IRQ HSI_P2_DSP_IRQ	
HSI_Pp_M_IRQrU_STATUS[23:16] HSR_OVERRUN_CHI	HSI_Pp_M_IRQrU_ENABLE[23:16] HSR_OVERRUN_ENI	HSI_P1_MPU_IRQ HSI_P2_MPU_IRQ	Data overrun in real time mode on any channel 8–15
HSI_Pp_D_IRQrU_STATUS[23:16] HSR_OVERRUN_CHI	HSI_Pp_D_IRQrU_ENABLE[23:16] HSR_OVERRUN_ENI	HSI_P1_DSP_IRQ HSI_P2_DSP_IRQ	
HSI_Pp_M_IRQrU_STATUS[15:8] HSR_AVAILABLE_CHI	HSI_Pp_M_IRQrU_ENABLE[15:8] HSR_AVAILABLE_ENI	HSI_P1_MPU_IRQ HSI_P2_MPU_IRQ	Data received on any channel 8–15
HSI_Pp_D_IRQrU_STATUS[15:8] HSR_AVAILABLE_CHI	HSI_Pp_D_IRQrU_ENABLE[15:8] HSR_AVAILABLE_ENI	HSI_P1_DSP_IRQ HSI_P2_DSP_IRQ	
HSI_Pp_M_IRQrU_STATUS[7:0] HST_ACCEPTED_CHI	HSI_Pp_M_IRQrU_ENABLE[7:0] HST_ACCEPTED_ENI	HSI_P1_MPU_IRQ HSI_P2_MPU_IRQ	Data transmitted on any channel 8–15
HSI_Pp_D_IRQrU_STATUS[7:0] HST_ACCEPTED_CHI	HSI_Pp_D_IRQrU_ENABLE[7:0] HST_ACCEPTED_ENI	HSI_P1_DSP_IRQ HSI_P2_DSP_IRQ	
HSI_Pp_M_IRQr_STATUS[26] HSR_WAKE	HSI_Pp_M_IRQr_ENABLE[26] HSR_WAKE	HSI_P1_MPU_IRQ HSI_P2_MPU_IRQ	Wake detected on any channel 0–7
HSI_Pp_D_IRQr_STATUS[26] HSR_WAKE	HSI_Pp_D_IRQr_ENABLE[26] HSR_WAKE	HSI_P1_DSP_IRQ HSI_P2_DSP_IRQ	
HSI_Pp_M_IRQr_STATUS[25] HSR_BREAK	HSI_Pp_M_IRQr_ENABLE[25] HSR_BREAK	HSI_P1_MPU_IRQ HSI_P2_MPU_IRQ	Break detected on any channel 0–7
HSI_Pp_D_IRQr_STATUS[25] HSR_BREAK	HSI_Pp_D_IRQr_ENABLE[25] HSR_BREAK	HSI_P1_DSP_IRQ HSI_P2_DSP_IRQ	
HSI_Pp_M_IRQr_STATUS[24] HSR_ERROR	HSI_Pp_M_IRQr_ENABLE[24] HSR_ERROR	HSI_P1_MPU_IRQ HSI_P2_MPU_IRQ	Error detected on any channel 0–7
HSI_Pp_D_IRQr_STATUS[24] HSR_ERROR	HSI_Pp_D_IRQr_ENABLE[24] HSR_ERROR	HSI_P1_DSP_IRQ HSI_P2_DSP_IRQ	
HSI_Pp_M_IRQr_STATUS[23:16] HSR_OVERRUN_CHI	HSI_Pp_M_IRQr_ENABLE[23:16] HSR_OVERRUN_ENI	HSI_P1_MPU_IRQ HSI_P2_MPU_IRQ	Data overrun in real time mode on any channel 0–7
HSI_Pp_D_IRQr_STATUS[23:16] HSR_OVERRUN_CHI	HSI_Pp_D_IRQr_ENABLE[23:16] HSR_OVERRUN_ENI	HSI_P1_DSP_IRQ HSI_P2_DSP_IRQ	
HSI_Pp_M_IRQr_STATUS[15:8] HSR_AVAILABLE_CHI	HSI_Pp_M_IRQr_ENABLE[15:8] HSR_AVAILABLE_ENI	HSI_P1_MPU_IRQ HSI_P2_MPU_IRQ	Data received on any channel 0–7
HSI_Pp_D_IRQr_STATUS[15:8] HSR_AVAILABLE_CHI	HSI_Pp_D_IRQr_ENABLE[15:8] HSR_AVAILABLE_ENI	HSI_P1_DSP_IRQ HSI_P2_DSP_IRQ	

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Table 23-796. Events (continued)

Event Flag	Event Mask	Map to	Description
HSI_Pp_M_IRQr_STATUS[7:0] HST_ACCEPTED_CHI	HSI_Pp_M_IRQr_ENABLE[7:0] HST_ACCEPTED_ENI	HSI_P1_MPU_IRQ HSI_P2_MPU_IRQ	Data transmitted on any channel 0–7
HSI_Pp_D_IRQr_STATUS[7:0] HST_ACCEPTED_CHI	HSI_Pp_D_IRQr_ENABLE[7:0] HST_ACCEPTED_ENI	HSI_P1_DSP_IRQ HSI_P2_DSP_IRQ	
HSI_DMA_M_IRQSTATUS[15:0] DMA_CHI	HSI_DMA_M_IRQENABLE[15:0] DMA_EN_CHI	HSI_P1_MPU_IRQ HSI_P2_MPU_IRQ	Channel 0–15 status
HSI_DMA_D_IRQSTATUS[15:0] DMA_CHI	HSI_DMA_D_IRQENABLE[15:0] DMA_EN_CHI	HSI_P1_DSP_IRQ HSI_P2_DSP_IRQ	
DMA_CSR_CCIR_i[21] BLOCK_IS	DMA_CSR_CCIR_i[5] BLOCK_IE	HSI_DMA_DSP_IRQ HSI_DMA_MPU_IRQ	Block transferred
DMA_CSR_CCIR_i[18] HALF_IS	DMA_CSR_CCIR_i[2] HALF_IE	HSI_DMA_DSP_IRQ HSI_DMA_MPU_IRQ	Half block reached
DMA_CSR_CCIR_i[16] TOUT_IS	DMA_CSR_CCIR_i[0] TOUT_IE	HSI_DMA_DSP_IRQ HSI_DMA_MPU_IRQ	Time-out event

23.10.4.5.1 Interrupts

By default, there are four interrupt output lines per HSI port (Mpuirq_0, Mpuirq_1, Dspirq_0, Dspirq_1), and two in the case of the DMA interrupt (MPU, DSP). The following registers are related to these interrupt outputs as follows:

- Status registers:
  - HSI_Pp_M_IRQrU_STATUS / HSI_Pp_M_IRQr_STATUS for Mpuirq_r (where r = 0 or 1)
  - HSI_Pp_D_IRQrU_STATUS/HSI_Pp_D_IRQr_STATUS for Dspirq_r (where r = 0 or 1)
  - HSI_DMA_M_IRQSTATUS for DMA interrupt to MPU
  - HSI_DMA_D_IRQSTATUS for DMA interrupt to DSP
- Enable registers:
  - HSI_Pp_M_IRQrU_ENABLE / HSI_Pp_M_IRQr_ENABLE for Mpuirq_r (where r = 0 or 1)
  - HSI_Pp_D_IRQrU_ENABLE/HSI_Pp_D_IRQr_ENABLE for Dspirq_r (where r = 0 or 1)
  - HSI_DMA_M_IRQENABLE for DMA interrupt to MPU
  - HSI_DMA_D_IRQENABLE for DMA interrupt to DSP

However, Mpuirq_0 and Mpuirq_1 are further combined (logical OR) into one common interrupt output per port (HSI_P1_MPU_IRQ for port 1, and HSI_P2_MPU_IRQ for port 2). The same goes for Dspirq_0 and Dspirq_1 (HSI_P1_DSP_IRQ for port 1, and HSI_P2_DSP_IRQ for port 2).

This means that it is enough to enable one of the FIFO/WAKE/BREAK/ERROR interrupt events per port (for example, in HSI_Pp_M_IRQ0(U)_ENABLE) to raise the corresponding interrupt request. Enabling both HSI_Pp_M_IRQ0(U)_ENABLE and HSI_Pp_M_IRQ1(U)_ENABLE would only mean extra checks and clears (in the corresponding IRQ status register). The same is true for the DSP-related IRQ enable/status registers.

The HSI module outputs six interrupt signals (for more information, see Section 23.10.3, *MIPI HSI Integration*). All the interrupts are active-high level-sensitive. Each interrupt line is activated by a set of individual sources. All interrupt sources can individually be enabled and disabled.

For each interrupt, 2 status bits and 2 mask bits are provided, allowing independent masking for the different processors (that is, 1 status bit and 1 mask bit for the MPU [Cortex-A9 or Cortex-M3] interrupts, and 1 status bit and 1 mask bit for the DSP interrupts).

Interrupts in the HSI module are intended to:

- Signal any error condition in reception
- Support the WAKE condition detection
- Support the BREAK condition detection
- Warn of DMA transfer status or problems

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- Signal to processors when to read received data and to write data to transmit

Because DMA has only 16 channels, 16 RX FIFO and 16 TX FIFO are managed by a mix of DMA-driven and interrupt-driven read/write policies.

23.10.4.5.1.1 HSI Interrupt Generation

Five types of interrupt events can be generated by each HSI port:

- Transmit FIFO not full: Occurs when TX FIFO is not full, so data can be written for transmission
- Received data available: Occurs when one data frame has been received and is available on the RX FIFO for reading
- Overrun: Occurs when data overrun is detected on HSI port *p* channel *i*
- Error: Any error defined by the MIPI HSI protocol activates this source of interrupt if this source is enabled.
- Break condition detected: Occurs upon reception of a continuous string of 0s that exceed those possible in any FRAME mode frame (data + header). Because FRAME mode always put a 1 before any frame, the maximum number of 0s occurring during normal transmission is clearly 32 plus the base 2 logarithm of channels used. Hardware works out this number based on register information on channels and receive mode, sets the HSR_BREAK_Pp[0] BREAK_VAL bit to 1, and issues an interrupt if this source is enabled.

All the events are cleared by software, upon setting the corresponding register bit to 1. Setting the bit to 0 has no effect.

23.10.4.5.1.2 DMA Interrupt Generation

Three types of interrupt events can be generated by each DMA channel:

- End of Block: Enabled through the DMA_CSR_CCIR_i[5] BLOCK_IE bit, it occurs when the last element of the transfer has been written into destination. The DMA_CEN_i[15:0] SIZE bit field defines the number of elements in a block.
- Half Block: Enabled through the DMA_CSR_CCIR_i[2] HALF_IE bit, it occurs when a half of the elements have been written into destination.
- Time-out error: Enabled through the DMA_CSR_CCIR_i[0] TOU_IE bit, it occurs when destination slave answers by an error code.

All interrupt events are generated on the same logical channel dedicated interrupt line. When an interrupt is issued by a logical channel, its DMA_CSR_CCIR_i status register is set to record the interrupt cause, if the interrupt event bit is enabled in the relevant DMA_CSR_CCIR_i register. The processor interrupt service routine can read this channel status register to identify the sources of the interrupt. The status bits are automatically cleared after they are read by the processor, unless it is an emulation read.

There are two classes of DMA interrupt events:

- Error events: Errors during the transfer
- Status events: DMA transfer status, such as end of block or half-block

The DMA manages the two classes differently.

For an enabled error event, the following sequence occurs:

1. The appropriate bit in the DMA_CSR_CCIR_i register is set.
2. An interrupt is generated.
3. The ports are released.
4. The currently active logical channel is disabled and must be reprogrammed.
5. Other channels are not affected, and a new channel can get over, according to programmed priorities.

For an enabled status event, the following sequence occurs:

1. The appropriate bit in the DMA_CSR_CCIR_i register is set.
2. An interrupt is generated.
3. A new interrupt cannot be generated until the status register is read and thereby cleared.

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All the events are cleared by software, upon setting the corresponding interrupt status register (HSI_DMA_M_IRQSTATUS or HSI_DMA_D_IRQSTATUS) to 1. Setting the interrupt status register to 0 has no effect.

23.10.4.6 DMA Module

23.10.4.6.1 DMA Overview

The DMA module transfers data between the HSI interfaces and the device on-chip memories. The DMA module supports 16 logical channels and is a dual-port initiator (peripheral port/memory port) with one slave port for configuration. The memory port provides an interface to the memory space and the peripheral port provides an interface to the HSI interfaces. In the HSI controller, the L4_CFG port accesses can be routed directly to the HSI interfaces. This is done by setting the DMA in bypass mode to route the DMA slave port to the DMA peripheral port.

DMA features:

- One target port, for configuration
- 16 logical channels: *n* for transmission and *16-n* for reception
- One initiator port, for transfer to/from memory
- One port to/from LCH memory (this memory holds some registers)
- 32-bit data handling only
- Constant addressing mode on peripheral port/FIFO
- Post-increment addressing mode with burst support on memory port
- Software enabling
- Hardware activation of data transfer on peripheral port
- Logical channels interleaving with only few-cycles-latency
- Fixed allocation of memory and peripheral port to a logical channel
- LCH first-come-first-served + fixed priority arbitration
- Low-power operation (hardware control for clock domains activity)
- Software reset

23.10.4.6.2 DMA Memories

DMA channel register memory is managed by the DMA. Only the DMA interfaces this memory. A processor must program the DMA registers included in this memory.

The DMA has access to 16 dual-port FIFO 8 × 32 bits for reception and 16 dual-port FIFO 8 × 32 bits for transmission. They are provided in the form of two separate memories.

23.10.4.6.3 DMA Basic Operation Outline

DMA write and read operations are helped by tags, to manage possibly disorderly answers. Posted or nonposted operations are possible. In any case, the interconnect always manages them as nonposted. This is consistent with DMA operations that need to know (for example, if main memory write was successful). If not, the error response from L3 interconnect slave produces a DMA error and the corresponding interrupt. DMA addressing of FIFO memories is always on a constant address, corresponding to 1 of the 16 HST_BUFFER_Pp_CHN_i (or HSR_BUFFER_Pp_CHN_i) registers.

These registers are associated with the 16 FIFOs, and the naming reflects only the reset value of the association FIFO, HSI logical channel. Therefore, at reset, the FIFO addressed on the HSR_BUFFER_P2_CHN_4 register is associated with the fourth logical channel of the second port. Nevertheless, software can change this mapping and associate the same FIFO (for example, to the seventh channel of the first port). This mapping is performed by software through the HST_MAPPINGf[4:1] CH_NUMBER or HSR_MAPPINGf[4:1] CH_NUMBER bit fields.

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23.10.4.6.4 DMA Configuration

Before performing a DMA transfer, the following DMA registers must be configured:

- DMA_CCR_CSDP_i: Sets source and destination parameters and channel control
  - DMA_CCR_CSDP_i[15:14] DST_BURST_EN: Destination burst enable (0x0 and 0x1: single access; 0x2: burst 4 × 32 bits; 0x3: burst 8 × 32 bits)
  - DMA_CCR_CSDP_i[12:9] DST: Transfer destination (0x8: transfer to memory port; 0x9: transfer to peripheral port)
  - DMA_CCR_CSDP_i[8:7] SRC_BURST_EN: Source burst enable (0x0 and 0x1: single access; 0x2: burst 4 × 32 bits; 0x3: burst 8 × 32 bits)
  - DMA_CCR_CSDP_i[5:2] SRC: Transfer source (0x8: transfer from memory port; 0x9: transfer from peripheral port)
  - DMA_CCR_CSDP_i[31:30] DST_ADD_MODE: Destination addressing mode (0x0: constant address mode; 0x1: post-incremented address mode)
  - DMA_CCR_CSDP_i[29:28] SRC_ADD_MODE: Source addressing mode (0x0: constant address mode; 0x1: post-incremented address mode)
- DMA_CSR_CCIR_i: Enables DMA sources of interrupt events
- DMA_CSSA_i[31:0] ADDR: Stores 32 bits of the source address
- DMA_CDSA_i[31:0] ADDR: Stores 32 bits of the destination address
- DMA_CEN_i[31:0] SIZE: Defines the number of elements in a block. The maximum number of elements is 65535.

To start a DMA transfer, the DMA channel to be used must be enabled by setting the DMA_CCR_CSDP_i[23] ENABLE bit to 1. Once the DMA transfer is finished, the DMA_CCR_CSDP_i[23] ENABLE bit is automatically reset by hardware.

The DMA_CDAC_CSAC_i[15:0] ADDRESS_CSAC (or DMA_CDAC_CSAC_i[31:15] ADDRESS_CDAC) bit field can be used to monitor the progress of a DMA transfer on the channel source (or destination). It is a snapshot of the source (or destination) address generated by the channel counter. It is incremented on each access made on channels.

23.10.4.7 HSR Module

The HSR module is the receiver part of the HSI module. It features 16 channels.

23.10.4.7.1 Receive Data

The value on the DATA line is always the transmitted bit, when sampled by the clock recovered. The double level of buffering allows the data to be safely transferred to the FIFO, while a new frame is stored. Data headers do not belong in FIFO and must be decoded to load data on the correct FIFO (there is one logical FIFO per logical channel).

Figure 23-221 shows the receive state-machine implemented in the HSI module.

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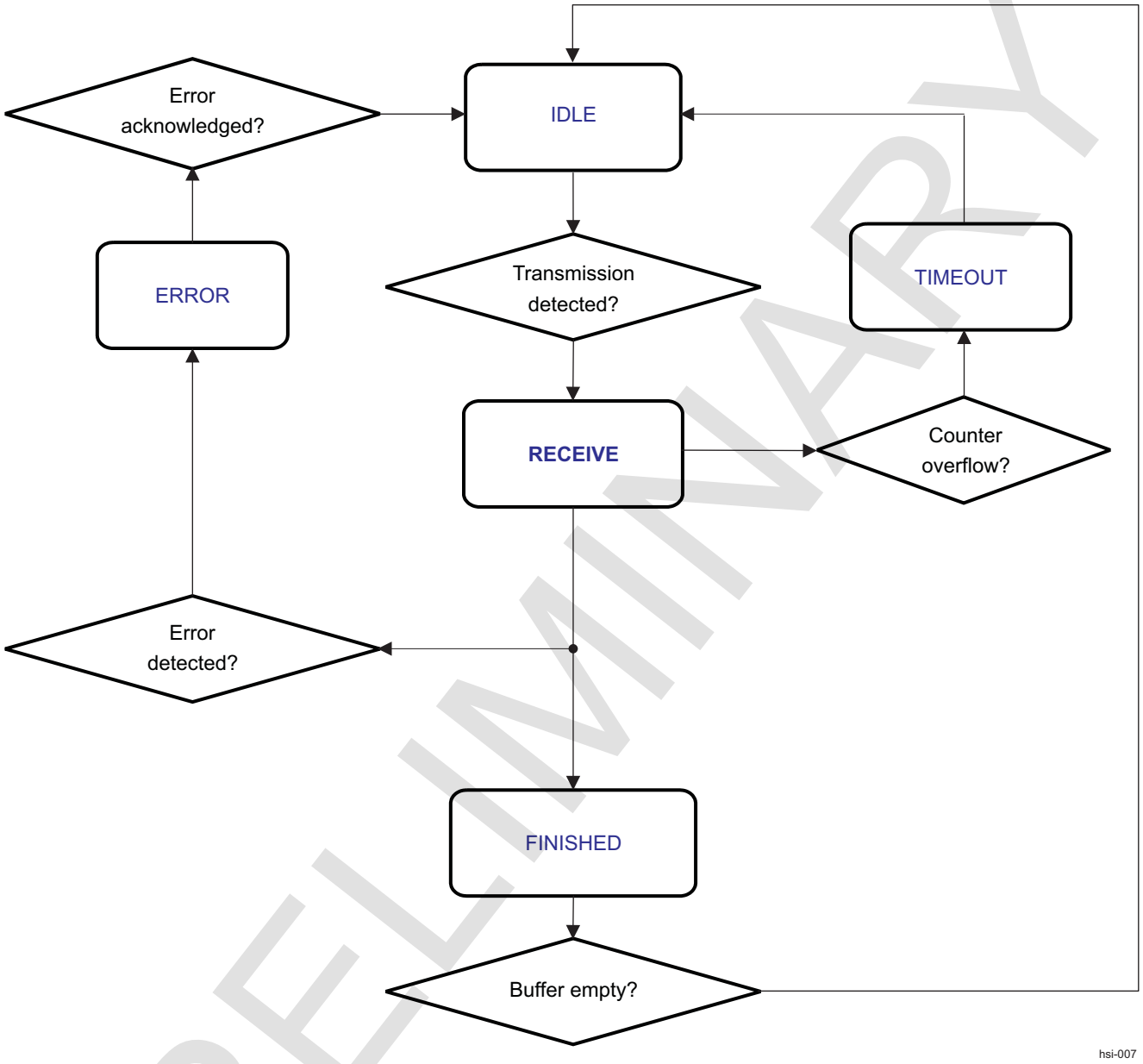
Figure 23-221. Receive FSM



23.10.4.7.2 Transmission Detection

Reception starts upon two alternate conditions:

- The remote transmitter raises the WAKE line (in this case, it does not actually transmit until the local receiver raises the READY line).
- An activity (in the form of transitions) appears on the FLAG/DATA lines, in case the remote transmitter does not implement the WAKE signal. The receiver must then save and store the received data, at least one frame long, before preventing further transmission by setting READY to 0.

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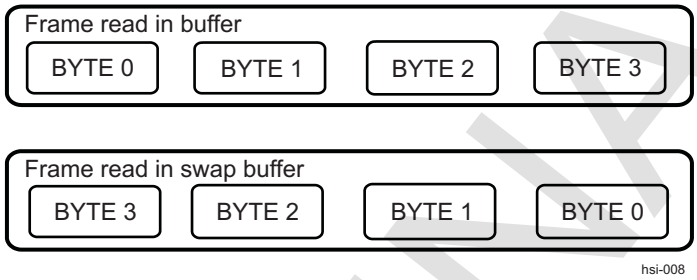
23.10.4.7.3 Receive Buffers

For each logical channel, the HSR_BUFFER_Pp_CHN_i[31:0] DATA bit field holds one frame. The appropriate bit in the HSR_BUFSTATE_Pp register is set to 1 by hardware when the corresponding HSR_BUFFER_Pp_CHN_i register holds one frame. Reading the HSR_BUFFER_Pp_CHN_i[31:0] DATA bit field automatically resets the appropriate bit in HSR_BUFSTATE_Pp. This lets the receiver put another data frame in HSR_BUFFER_Pp_CHN_i, setting again HSR_BUFSTATE_Pp.

Some applications need reversed byte ordering of frames. This is supported by the HSR_SWAPBUFFER_Pp_CHN_i register (see Figure 23-222). By reading this register instead of the corresponding HSR_BUFFER_Pp_CHN_i register on the same channel, byte ordering of the 4 bytes in a frame is reversed.

Figure 23-222. HSR_SWAPBUFFER_Pp_CHN_i Register



Reading the MSB of the HSR_SWAPBUFFER_Pp_CHN_i register sets the corresponding bit of HSR_BUFSTATE_Pp to empty.

NOTE: Read access to the register with 0x3 and 0xF byte-enable removes the receive FIFO-related item. If only 16-bit accesses are used, the upper 2 bytes must be read first (byte-enable 0xC). Between two consecutive 16-bit FIFO-related accesses there cannot be any other FIFO-related OCP access.

23.10.4.7.4 Receive Operations

Logically, the receiver amounts to the receiver shift register, double-buffering and the FSM. The current state of the FSM can be observed and controlled through the HSR_RXSTATE_Pp[2:0] RXSTATEVAL bit field. For the receive FSM, a functional description is shown in Figure 23-221.

The receiver FSM is in IDLE state when no transmission is detected, or the HSR_MODE_Pp[1:0] MODE_VAL bit field = FRAME and no synchronization bit is detected. Otherwise, it stores the first received bit and transitions to RECEIVING state, where it stops until a full frame is received.

Depending on the selected flow control, the READY line may have to go to 0 after the first bit is received.

Upon receiving a full frame, the FSM transitions to FINISHED state. Otherwise, the FSM transitions to TIMEOUT state as soon as a time-out value (if enabled and programmed in the HSR_COUNTERS_Pp[19:0] FT bit field) is reached. Then it moves to IDLE state.

After entering RECEIVED state, the FSM stays there until the received frame is correctly stored and there is room for another frame. At this point, READY is raised and the FSM goes to IDLE state. In pipelined flow, flow control by READY is not operating at each byte, and in real time flow it is never operating. In both cases, the FSM transitions immediately to IDLE, to receive more data. Illegal transitions or flags raised by error counters (see Section 23.10.4.11, *Error Reporting*), move the FSM to ERROR state, and then to HALT, to wait until the error is acknowledged by software, warned by an interrupt. Except for pipelined control flow, the READY output is always 1 in IDLE state and 0 anywhere else. In pipelined mode, the READY signal stays to 1, and is cleared by a condition on buffer full. The FSM state can be controlled by software by writing in the HSR_RXSTATE_Pp[2:0] RXSTATEVAL bit field. This can be useful to recover from an error condition.

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23.10.4.7.5 Receive Exceptions

23.10.4.7.5.1 Break

Remote transmitter can force synchronization by a long enough string of 0s (equal to the number of header + data bits in the frame + 1). In frame mode, this sets the HSR_BREAK_Pp[0] BREAK_VAL bit to 1, which in turn sends an interrupt.

23.10.4.7.5.2 Overrun

An overrun condition is possible during real-time flow, if received data occur when the FSM is in FINISHED state. Whenever this happens, the HSR_OVERRUN_Pp[15:0] OVERRUN_VAL bit field is set for the corresponding logical channel, which in turn generates an interrupt.

An overrun exception is a legacy condition required in previous SSI hardware, where reception without the READY signal had to be supported. In HSI the READY signal always exists, but it cannot be used during real-time flow and the last 8 bits of a frame during pipelined flow. During real-time data flow, overrun can occur at any time. The main goal of using real-time flow is flushing FIFOs after an error. In that case, an overrun interrupt does not seem worth to be raised. Data does not have to be discarded. The real-time data are discarded if the receiver cannot follow the transmission rate, otherwise, the real-time data is kept in FIFO.

23.10.4.7.5.3 Errors

Several sources of errors are possible. In any of them, the receiver FSM stays in ERROR state until the error interrupt is acknowledged by writing the HSR_ERRORACK_Pp registers. Sources of errors include receive FRAME TIMEOUT, other receive errors flagged by error counters, and any other abnormal condition, as explained in Section 23.10.4.11, *Error Reporting*.

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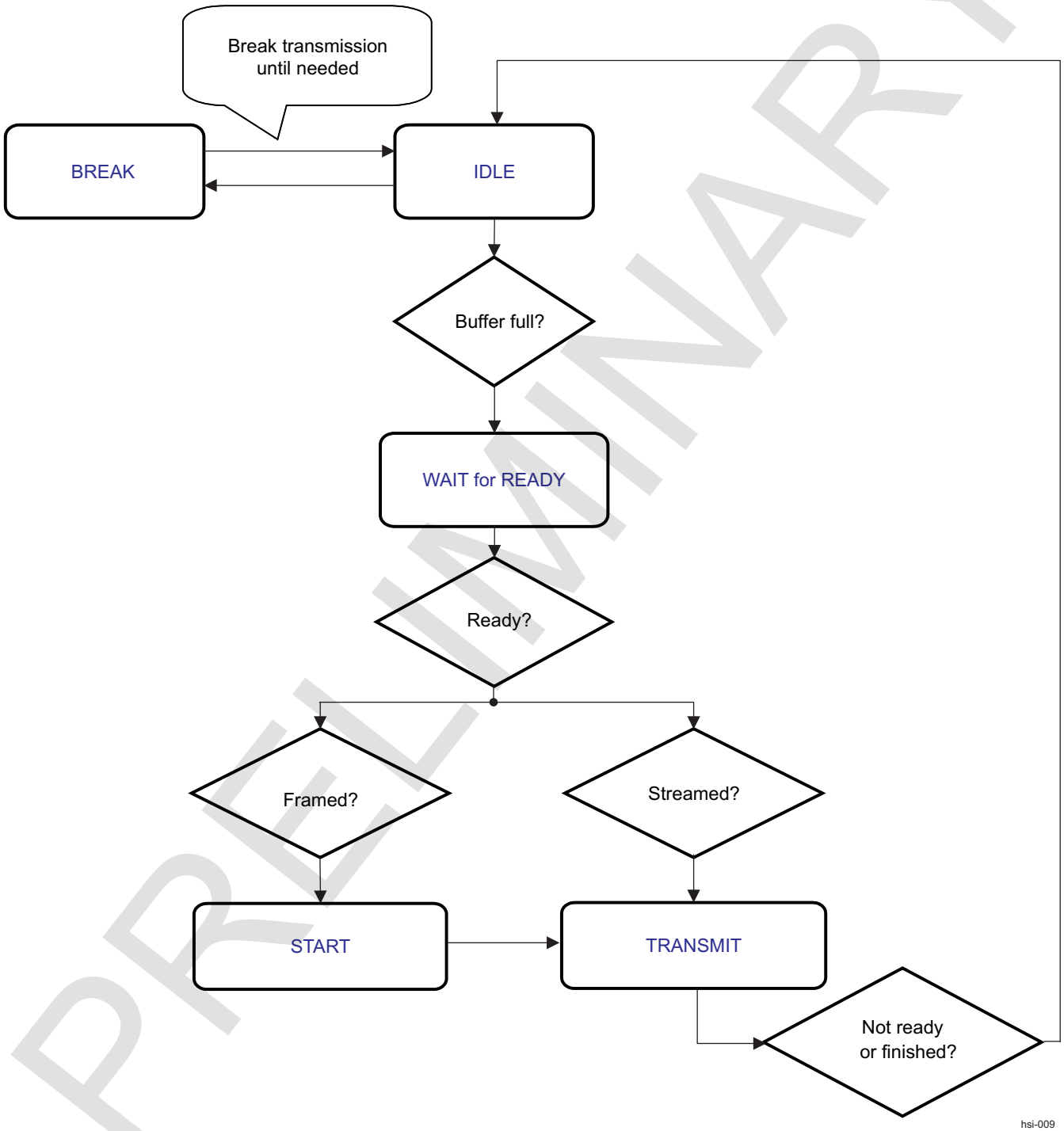
23.10.4.8 HST Block

The HST block is the transmitter part of the HSI module. It features 16 channels.

Figure 23-223 shows the receive state-machine implemented in the HSI module.

Figure 23-223. Transmit FSM



23.10.4.8.1 Configuration

Configuration of the component is expressed in terms of operation mode, number of logical channels, bit rate divisor, and arbitration mode.

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23.10.4.8.1.1 Mode Register

The HST_MODE_Pp register cannot be changed without stopping the link.

There is one HST_MODE_Pp[3:2] FLOW_VAL bit field for each active transmit channel and another HSR_MODE_Pp[3:2] FLOW_VAL bit field for each active receive channel. The local transmitter (communicating with the remote receiver) uses the HST_MODE_Pp[3:2] FLOW_VAL bit field for interpretation of the received READY line, for example to signal errors.

The HST_MODE_Pp register has the following bit fields:

- WAKE_CTRL selects between software (when 0x0) or automatic (when 0x1) control for the WAKE line. The default is software control.
- MODE_VAL defines the following operation modes:
  - Sleep: Specifies whether internal clocks must run and port be operating
  - Stream: Receiver does not use start-bits.
  - Frame: Allows break transmission/reception defined as a longer-than-frame 0 sequence
- FLOW_VAL defines the following data flows:
  - Synchronized flow: The READY signal from the receiver drops after every first frame bit, rising when data are stored, and transmission of a new frame is possible.
  - Pipelined flow: The receiver cannot drop the READY line at some times.
  - Real-time flow: The receiver drops the READY line at the first received bit and raises it at the last one.

NOTE: READY is activated when the module is going into ACTIVE state (stream or frame mode). Receive mode must be selected at the end of the configuration of the module, because it activates the transfer from the remote side. This prevents the device from receiving incorrect data, losing data, and falsely starting communication.

23.10.4.8.1.2 Other Registers

- The HST_FRAMESIZE_Pp register is kept to offer legacy compatibility. It is a read-only register, returning 0x1F.
- The HST_DIVISOR_Pp[7:0] RX_RATE_DIV_VAL bit field sets the transmission bit rate, with 1 transmitted bit per clock cycle. Bit rate can be changed by software at any time.
- The HST_CHANNELS_Pp[4:0] CHAN_NUM_VAL bit field sets the number of logical channels. It must be a power of 2. The default value is 0x1. This corresponds to only one logical channel, always the same, and in that case, a header is not transmitted; It cannot be changed without stopping the link.
- HST_MAPPINGf contains important settings for each FIFO (one register per FIFO):
  - HST_MAPPINGf[0] ENABLE bit: FIFO is enabled or not.
  - HST_MAPPINGf[4:1] CH_NUMBER and HSR_MAPPINGf[7] PORT_NUMBER bit fields (channel number and port number): FIFO is assigned to an HSI logical channel on a physical port.
  - HST_MAPPINGf[13:10] THRESHOLD bit field is the number of empty TX FIFO locations that will activate interrupt automatically.
- The HST_ARBMODE_Pp[0] ARB_VAL bit allows choosing of the arbitration policy for time allocation to logical channels, when several channels have to transmit. Round-robin algorithm implements a circular scan: the same channel cannot transmit twice if another channel is ready to transmit. Scan proceeds in the same, unspecified direction (design choice). Fixed priority algorithm grants maximum priority to logical channel 0, minimum priority to channel 15. The right to transmit is assigned to the higher priority channel ready to transmit, independently of previous transmissions.

  The choice between algorithms must consider that round-robin sets a maximum wait time for each channel, but it may require a long time to transmit long sequences of frames, on any channel. On the other hand, fixed priority allows limiting of transmission time for high priority channels, while low priority channel may wait for a long time.

  It is important to understand that this register sets the allocation of one port resource (transmission lines) from 2 to 16 vying transmit FIFOs. Allocation of the 16 transmit FIFOs to 32 logical channels is

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done by the HST_MAPPINGf register. For this second kind of allocation, no arbitration makes sense, because software is in charge to ensure against more that 16 logical channels transmitting at the same time.

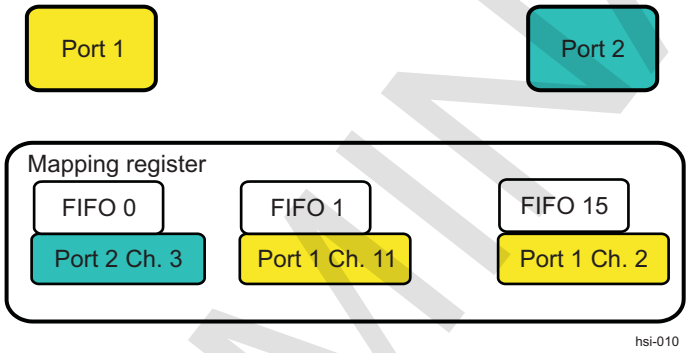
23.10.4.8.2 Mapping

Figure 23-224 shows an example of programming the HST_MAPPINGf register. No limitation is set on the choice of channel/FIFO/port association.

Each port has its HST_ARBMODE_Pp register so that it is also possible to program alternate algorithms on ports.

While the HST_MAPPINGf register cares only about FIFO, the HST_ARBMODE_Pp register is associated to a port and each port has its own one, which only selects a winner between ready-to-transmit channels of this port. For example, suppose that in Figure 23-224 only the three represented channels need to transmit; then a yellow (Port 1) arbiter chooses between channel 11 and channel 2, while the cyan (Port 2) arbiter has no decision to take and lets channel 3 transmit.

Figure 23-224. MAPPING Register



23.10.4.8.3 Transmission Buffer

The transmission buffer holds a frame to be transmitted for each channel. The HST_BUFSTATE_Pp[7:0] BUFSTATE_VAL bit field indicates whether the HST_BUFFER_Pp_CHN_i[31:0] DATA bit field holds significant data, and it is not be cleared until transmit FSM is in IDLE state and arbitration indicates the channel is the next in line to transmit. The HST_BUFSTATE_Pp register is automatically written by hardware.

NOTE: Write access to the register with 0x3 and 0xF byte-enable loads its value into the transmit FIFO. If only 16-bit accesses are used, the upper 2 bytes must be written first (byte-enable 0xC). Between two consecutive 16-bit FIFO-related accesses there cannot be any other FIFO-related OCP access.

Some applications need reversed byte ordering of frames. This is supported by the HST_SWAPBUFFER_Pp_CHN_i register. By reading this register instead of the corresponding HST_BUFFER_Pp_CHN_i register on the same channel, byte ordering of the 4 bytes in a frame is reversed (see Section 23.10.4.7.3, *Receive Buffers*).

23.10.4.8.4 Break Pattern Transmission

Break pattern transmission is an alternative to normal transmission mode, and is used when trying to recover lost synchronization. It is started by software by setting the HST_BREAK_Pp[0] BREAK_VAL bit. As soon as transmit FSM is in IDLE state (ready to accept another frame for transmission), a nonzero value on the HST_BREAK_Pp[0] BREAK_VAL bit starts the BREAK sequence, and automatically clears the HST_BREAK_Pp[0] BREAK_VAL bit. A sequence of 0, longer than a frame, is transmitted.

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23.10.4.8.5 Transmission Operations

The transmitter adds up to the transmit shift register, loaded from the transmission buffer, and the transmit FSM current state of the FSM can be observed and controlled through the HST_TXSTATE_Pp[2:0] TXSTATEVAL bit field. A functional description of the transmit FSM is shown in Figure 23-223.

After reset, the transmitter is in IDLE state. It starts transmission when there is data in one of the transmission HST_BUFFER_Pp_CHN_i registers, depending on the value of HST_BUFSTATE_Pp[7:0] BUFSTATE_VAL bit field, or when the value of BREAK is not 0.

When transmitting a data frame (not a BREAK sequence), the frame to be transmitted is clocked from the HST_BUFFER_Pp_CHN_i register to the transmission shift register, and the FSM enters WAIT state until it receives READY = 1. At this point, it starts driving the DATA and FLAG lines with a preliminary start-bit at 1, if in STREAM mode, or with the frame, which amounts to header and payload data.

In case of synchronized data flow, the TRANSMIT state is left after one frame is transmitted, because READY always drops after the first transmitted bit. Transmit FSM transitions through IDLE and WAIT states before retransmitting, when READY rises.

In case of pipelined data flow, transmit FSM remains in TRANSMIT state as long as READY = 1, and transmission goes on, always clocking data from the appropriate HST_BUFFER_Pp_CHN_i register, as selected by arbitration. Transmission is stopped by the condition READY = 0, forcing FSM to go into IDLE state. READY must not switch during the last 8 nominal bit times.

23.10.4.8.6 Transmission Exceptions

There are no transmission errors. Reception of READY = 0 in the last 8 bits of frames is not flagged. The DATA ACCEPTED interrupt is used to inform software that the HST_BUFFER_Pp_CHN_i[31:0] DATA bit field is empty and to request more data.

23.10.4.9 HSI Wake Generator

The WAKE line is used to create a wake-up event for the external module that interfaces with HSI before a data transfer through the HSI serial interface.

The 16 bits (1 per HSI channel) of the HSI_Pp_WAKE[15:0] WAKE_CHI bit field are ORed together to drive the WAKE line, as shown in Figure 23-225.

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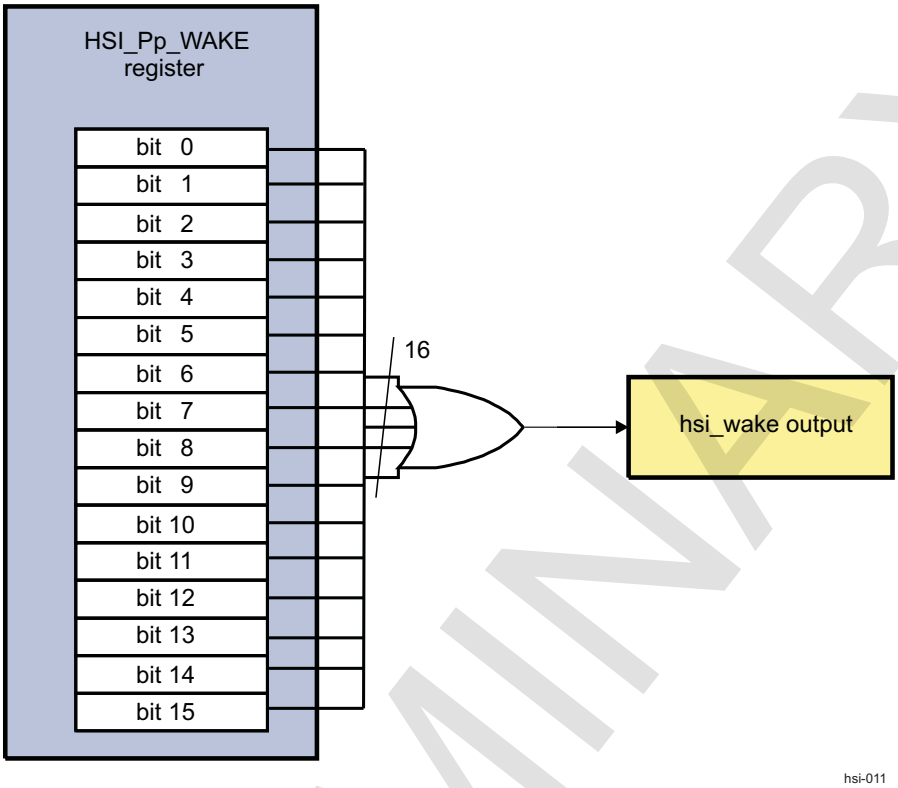
Figure 23-225. HSI_Pp_WAKE Control in Case of Managed Wake



The wake generator can be managed by software operations or automatically by hardware. If the wake generator is not managed, the WAKE signal is driven to 0 and the remote transmitter must wake itself upon activity detection on the DATA and FLAG lines.

23.10.4.9.1 Software Management of HSI Wake Generator

Software can get the responsibility to use and manage those bits to create and release wake-up events consistently with HSI use.

Because the HSI_Pp_WAKE[15:0] WAKE_CHI bit field can be managed by different threads/processors, this mechanism allows independent bit management by each thread. Without locking the HSI_Pp_WAKE register (as a read-modify-write does), it avoids one thread to overwrite the register change made by another thread. Each bit of the HSI_Pp_SET_WAKE[15:0] HSI_SET_WAKE_CHI bit field is owned by one thread at a time.

- The thread can set this bit by setting the corresponding bit of the HSI_Pp_SET_WAKE[15:0] HSI_SET_WAKE_CHI bit field to 1. This sets only this bit, thus leaving the other bits unchanged (no need of a read-modify-write).
- The thread can clear this bit by setting the corresponding bit of the HSI_Pp_CLEAR_WAKE[16:0] HSI_HSI_CLEAR_WAKE_CHI bit field to 1. This clears only this bit, thus leaving the other bits unchanged (no need of a read-modify-write).

23.10.4.9.2 Automatic Management of HSI Wake Generator

The wake generator is automatically managed when there is a transmission to be performed. When data are waiting for transmission in a FIFO TX, the hardware sets the corresponding bit of the HSI_Pp_WAKE[15:0] WAKE_CHI bit field, and this raises the WAKE signal on port *p*. Then WAKE is deasserted by the first occurrence of one event between a fixed time-out from the end of the last transfer, a transition to IDLE in idle-req protocol, a software clear of register.

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23.10.4.10 FIFO Subsystem

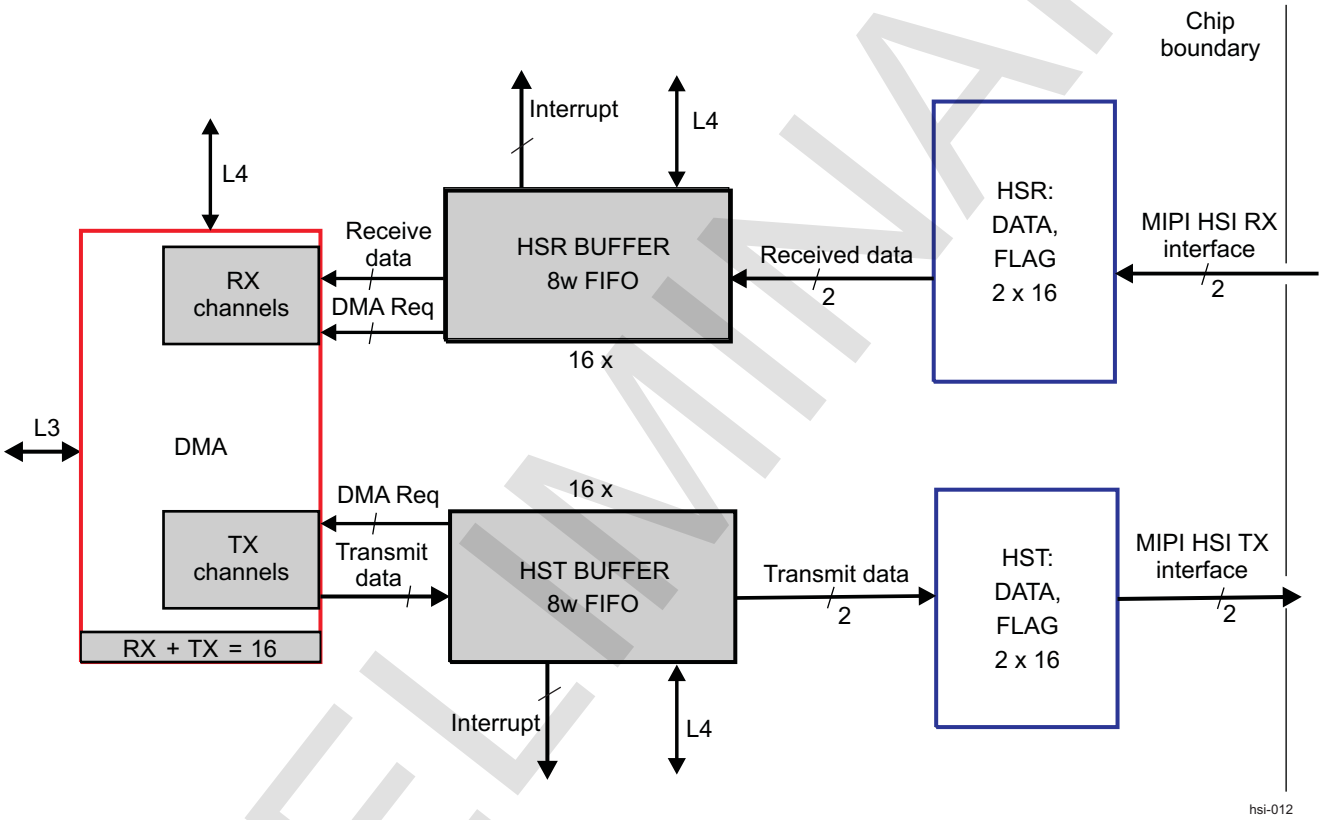
The FIFO subsystem allows temporary buffering while receive data is transferred from the receiver through DMA or the L4 interconnect to main memory, and the storing of transmit data read in main memory through DMA (or written by L4) before transmitting it. The FIFO depth is 8 × 32-bit words for each channel, yielding a total size of 1KB with 16 bidirectional channels.

RX FIFOs are clocked by interconnect clock, TX FIFOs are clocked by undivided functional clock.

23.10.4.10.1 FIFO Subsystem Architecture

Figure 23-226 shows the overall FIFO architecture.

Figure 23-226. Overall FIFO Architecture



There are 16 DMA channels available. They can be used for RX or TX in any combination; direction is programmable.

There are 16 RX FIFOs and 16 TX FIFOs. Not all FIFOs can be served by DMA, but all RX FIFOs (or else TX FIFOs) can be served by DMA, if needed. The other FIFOs, if used, must be read/written through the L4_CFG interconnect.

Both HSI ports provide up to 16 × 2 logical channels. This means that only one half of the HSI logical channels can be accommodated on the existing FIFOs. The others must not be used, and their use must flag an error. The 16 HST_MAPPINGf or HSR_MAPPINGf registers specify which HSI logical channel number is allowed to be received on RX FIFOs and/or fed for transmission by TX FIFOs. There is one mapping register for transmission and one for reception. Any attempt to transmit or process received data on HSI logical channels not previously mapped on mapping registers results in an error. In other words, some header values (bits 35 to 32) are not allowed at any given time, and generate an error when received. Software must ensure that the remote side sends payload on the allowed logical channels, specified by header values.

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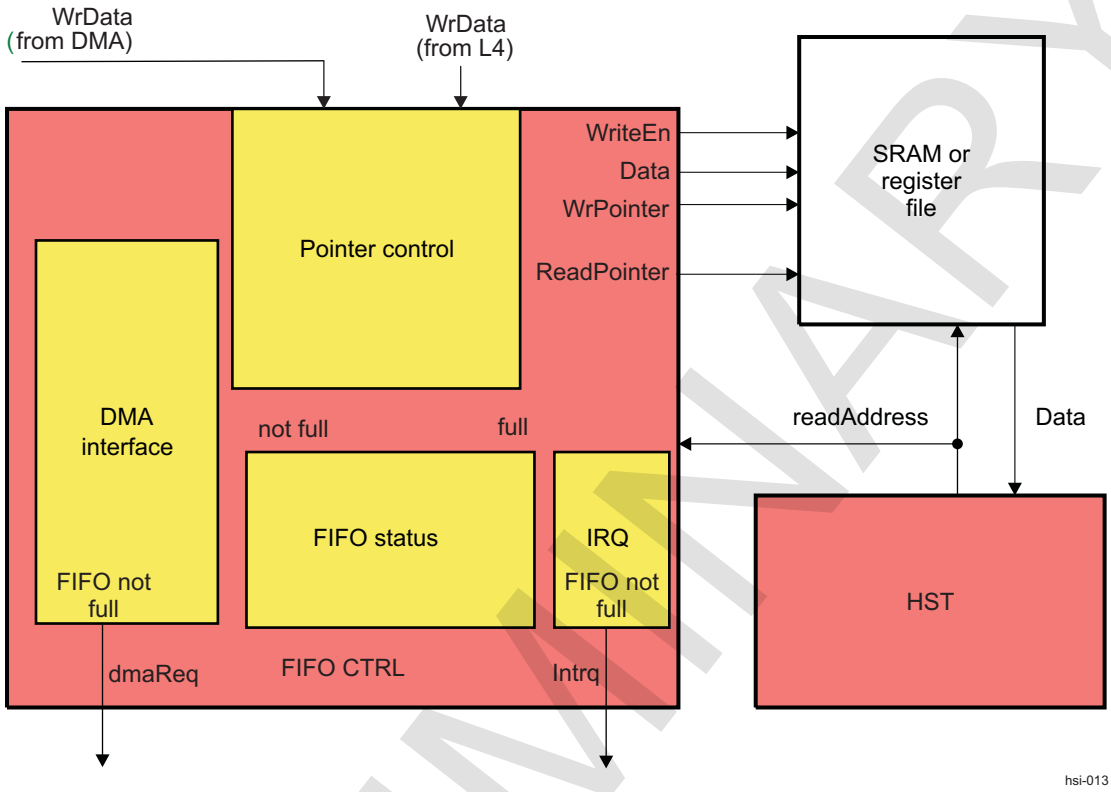
23.10.4.10.2 Transmit FIFO Architecture

Figure 23-227 shows the transmission FIFO architecture.

Figure 23-227. Transmission FIFO Architecture



The FIFO controller flags the condition of "room available in FIFO" or "FIFO not full" at any time when FIFO can host new data for transmission. This condition raises an interrupt request and a DMA request, if enabled. A programmable threshold in the corresponding HST_MAPPINGf[13:10] THRESHOLD bit field reduces the number of requests (they can be sent only when four words can be written in FIFO). The default value for the threshold is 0x0 (that is, a request rises as soon as one word can be written in FIFO). See Table 23-797.

Table 23-797. Threshold for Transmit FIFO Interrupt/DMA Request

HST_MAPPINGf[13:10] THRESHOLD	Number of Words in FIFO	Request
0 (legacy default)	Less than 8	Yes
1	Less than 1	Yes
2	Less than 2	Yes
3	Less than 3	Yes
4	Less than 4	Yes
5	Less than 5	Yes
6	Less than 6	Yes
7	Less than 7	Yes
8	Less than 8	Yes
9 to 15	Any	No

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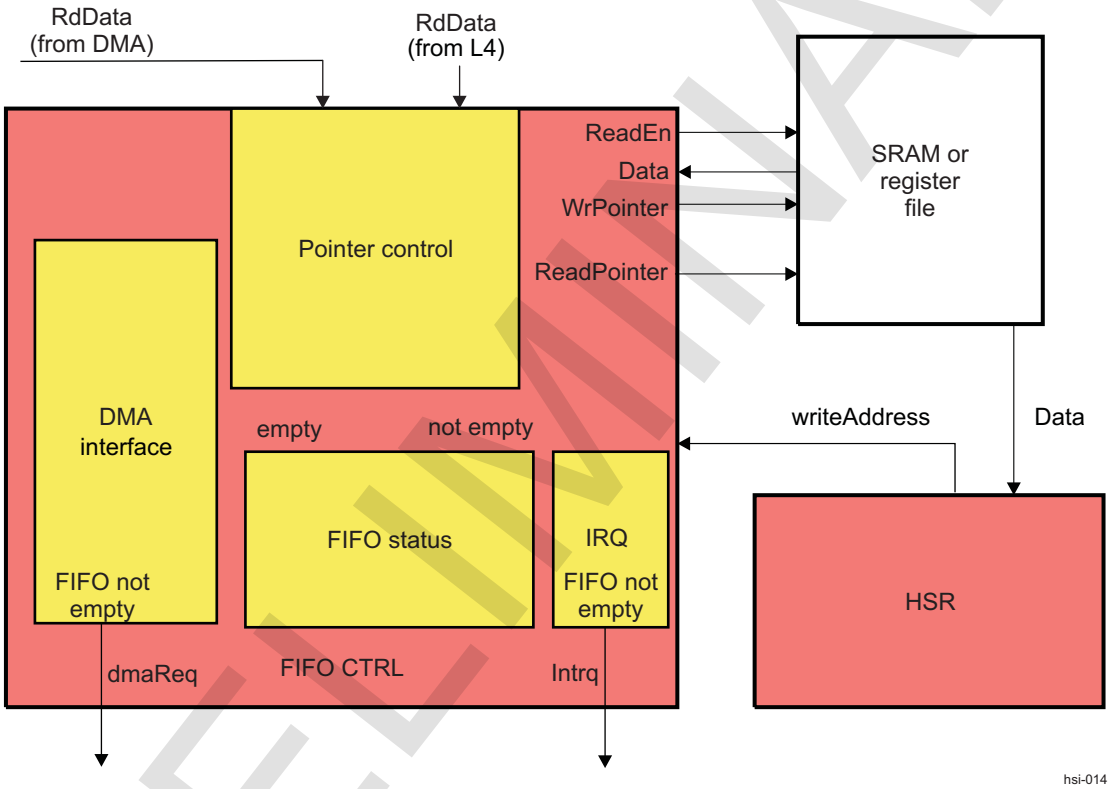
FIFO can be written by DMA and the L4 interconnect configuration port, but the L4 interconnect has fixed priority at any time. Software controls correct access. No hardware mechanism is provided to analyze and block concurrent operation, nor is any hardware control provided on reprogramming DMA registers during a transfer in which they are involved.

The address of FIFO is the corresponding HST_BUFFER_Pp_CHN_i register address. The FIFO controller generates the RAM addresses; namely, it manages the write pointer when DMA or the L4 interconnect access the HST_BUFFER_Pp_CHN_i address and it manages the read pointer when HST needs a data to transmit.

23.10.4.10.3 Receive FIFO Architecture

Figure 23-228 shows the reception FIFO architecture.

Figure 23-228. Reception FIFO Architecture



FIFO controller flags the condition of "unread data in FIFO" or "FIFO not empty" at any time when a FIFO hosts new data, received and not read. This condition can be simply the misalignment of the read pointer and write pointer. The condition raises an interrupt request and a DMA request, if enabled. The HSR_MAPPINGf[13:10] WORDS bit field informs software how many words must be read.

Unlike transmission, it is not possible here to filter requests through a threshold on the number of received words. If such a threshold is bigger than one, and a last single word is received after the last read, software is unaware that more data waits to be read.

The address of FIFO is the corresponding HSR_BUFFER_Pp_CHN_i register address. The FIFO controller generates the RAM addresses; namely, it manages the write pointer when HSR has received data, and it manages the read pointer when DMA or the L4 interconnect access the HSR_BUFFER_Pp_CHN_i register.

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23.10.4.10.4 FIFO Addressing

From a software point of view, a FIFO is seen at a single address, the corresponding HST_BUFFER_Pp_CHN_i or HSR_BUFFER_Pp_CHN_i register address. The HST_SWAPBUFFER_Pp_CHN_i or HSR_SWAPBUFFER_Pp_CHN_i register address is also provided to invert data endianness with byte granularity. FIFO overflow in RX is extremely unlikely, because of the large difference in HSI and L3 interconnect bit rate. However, if this occurs, the hardware prevents any loss of data by deasserting (setting to 0) the READY signal to the remote transmitter. FIFO overflow in TX is not flagged and must be avoided by software drivers.

23.10.4.11 Error Reporting

23.10.4.11.1 Detection of Errors

Error detection on the module is limited to the physical layer. No data corruption is checked, and no error is flagged as long as the receiver and transmitter agree on frame boundaries. Because clocking and data are recovered from alternate edges on the DATA and FLAG signals, three kinds of error can appear:

- Simultaneous edges
- Missing edges
- Additional edges

23.10.4.11.1.1 Simultaneous Edges

The transmitter is not supposed to produce simultaneous edges on the DATA and FLAG signals, but they can appear if the transmission rate is far higher than the receiver can handle. Given to the sampling protocol, this event may introduce errors in sampled data. Detecting this error is not easy, because the recovered clock is also affected, and in some configurations no other clock is available. One bit is available in the HSR_ERROR_Pp register, to report any hardware abnormal condition in data reception.

23.10.4.11.1.2 Missing Edges

Missing edges result in missing clock cycles, thus causing the receiver to get less data than expected on a given frame.

In synchronized flow, when the transmit side has completed transmission, the receiver side is still waiting for more data, and does not raise READY, thus stopping the transmitter from going on with more frames. A frame time-out counter (see Section 23.10.4.11.2.1, *Frame Time-Out Counter*) is used to escape this deadlock condition.

In pipelined flow, when the transmit side has completed transmission and has more data to transmit, the receiver accepts and processes this data as if they were part of the previous frame. Frame synchronization is then lost. It may randomly resume when in frame mode, as zeroes at the end of a frame are automatically discarded. But even in this case, a number of frames may be lost or corrupted. When in stream mode, no self-recovery is ever possible, and synchronization is lost forever. A frame burst counter (see Section 23.10.4.11.2.3, *Frame Burst Counter*) is used to limit the number of these potentially corrupted frames, simply by limiting the number of frames a transmitter can send back-to-back in a pipelined mode. A tailing bit counter (see Section 23.10.4.11.2.2, *Frame Tailing Bit Counter*) is used to check that the receiver and transmitter agree on being at the end of frame.

23.10.4.11.1.3 Additional Edges

Additional edges result in additional clock cycles, thus causing the receiver to get more data than expected on a given frame.

In synchronized flow, when the receive side thinks the frame is over, the transmitter keeps sending data until the end of frame is reached. In frame mode, if these additional bits are all 0s, they are discarded by the receiver, the transmission stops, and the receiver raises READY when it is available to receive a new frame. The transmit side starts a new frame and synchronization is recovered. But if at least one of the additional bits is set to 1, this can misguide the receiver that a new frame has already started and READY

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stays at 0. The transmit side stops, waiting for READY = 1, a never occurring condition, because the receiver has lost synchronization. In this case, the link is stuck. This is also the case in stream mode, when the receiver wrongly thinks that a new frame is started, so it is not available to receive a full new frame, and it does not set READY = 1. A frame time-out counter (see Section 23.10.4.11.2.1, *Frame Time-out Counter*) is used to escape this deadlock condition.

23.10.4.11.2 Error Counters

Clocks for these three counters are provided through a division of the functional clock. These counters can be set to a value and can be stopped when some events occur. Events flag errors and set a corresponding bit in the HSR_ERROR_Pp register.

23.10.4.11.2.1 Frame Time-Out Counter

This counter is clocked by the functional clock, divided by the factor specified in the HSR_DIVISOR_Pp[7:0] RX_RATE_DIV_VAL bit field, to provide a clock at receive bit rate. Receive bit rate is always communicated by the remote transmitter through the protocol layer. This counter starts when the first bit of the frame is found and stops when 36 (or 37 depending on the mode) bits are correctly received by the receiver. If the counter overflows, an error is generated (the HSR_ERROR_Pp[1] FTE bit is set to 0). In OPP reduction of the functional clock only (receive side kept in fixed voltage domain), software can decide to reduce either the division factor for the clock, or the count, to use a clock consistent with receive rate, or a reduced count of a slower clock. This is transparent for hardware. This counter is not started when the receive rate is outside the full error detection rate range.

23.10.4.11.2.2 Frame Tailing Bit Counter

This counter can be clocked by the same clock as the frame time-out counter, which has the receiver bit rate frequency. It starts after the last bit of a frame is received, and READY = 0; in pipelined flow, this counter is started only after the end of the last frame received. No event stops the counter, except its own overflow. It counts up to 8. An error is logged (the HSR_ERROR_Pp[4] TBE bit is set to 0) if a 1 bit is received in frame mode before counter overflow, or any bit is received in stream mode before counter overflow. In OPP reduction of functional clock only (receive side kept in fixed voltage domain), software can decide to reduce either the division factor for the clock, or the count, to use a clock consistent with receive rate, or a reduced count of a slower clock. This is transparent for hardware. This counter is not started when receive rate is outside the full error detection rate range.

23.10.4.11.2.3 Frame Burst Counter

Differently from previous counters, this counter is clocked by a frame-sync signal obtained directly by received data. Its goal is to reduce the number of contiguous frames sent in pipelined flow. As explained in Section 23.10.4.11.1, *Detection of Errors*, in some cases after missing/additional clock cycles, synchronization is lost and these pipelined frames can be corrupted. Software sets the count value, which can be as high as 256 (no higher values are supported by hardware). If READY is dropped to 0, for reasons other than counter expiration, the counter is stopped and restarted as soon as transmission resumes. At the end of the count, READY drops to 0. The tailing bit counter is started, and if it overflows without error detection and the receiver has enough room for another frame, READY is reset to 1. No error and no interrupt are generated on this counter.

23.10.4.11.3 Error Registers

One error register per port is provided to check the error source that issued an interrupt, with more details than the error bit in the interrupt status register.

- The HSR_ERROR_Pp[0] SIG bit: Signal error bits are kept for legacy reasons, and they can be used for any abnormal situation the hardware wants to flag.
- The HSR_ERROR_Pp[1] FTE bit: Frame time-out error bits flag the situation when not even a frame has been received in the time corresponding to two or more frames, depending on the FTE counter software setting.
- The HSR_ERROR_Pp[4] FBE bit: Tailing bit error bits flag the situation when at least one spurious bit is received after the end of a frame, in the time corresponding to two or more bit times.

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- The HSR_ERROR_Pp[7] RME bit: Receive mapping error bits flag the situation when data are received on a channel that is not mapped to any enabled FIFO.
- The HSR_ERROR_Pp[11] TME bit: Transmit mapping error bits flag the situation when DMA tries to access a FIFO that is not mapped to any logical channel, or is not enabled.

These two registers each have a companion HSR_ERRORACK_Pp register, where software must set the corresponding error bit to 1 to clear it.

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23.10.5 HSI Programming Guide

23.10.5.1 HSI Low-Level Programming Models

This section describes the low-level hardware programming sequences for the configuration and use of the HSI module.

23.10.5.1.1 Global Initialization

23.10.5.1.1.1 Surrounding Modules Global Initialization

This section identifies the requirements for initializing the surrounding modules when the HSI module is to be used for the first time after a device reset. This initialization of surrounding modules is based on the integration of the HSI.

For more information, see Section 23.10.3, *HSI Integration*.

Table 23-798. Global Initialization of Surrounding Modules for HSI

Surrounding Modules	Comments
PRCM	HSI functional and interface clocks must be enabled. For more information, see Chapter 3.
Control module	Module-specific pad muxing must be set in the control module. For more information, see Chapter 18.
(Optional) Interrupt controller	The Cortex-A9 MPU, Cortex-M3 MPU, or DSP INTC must be configured to enable the interrupt request generation to the Cortex-A9 MPU, Cortex-M3 MPU, or DSP subsystem. For information about enabling interrupts, see Chapter 5.
(Optional) Interconnect	For information about the L4 interconnect configuration, see Chapter 13, *Interconnects*. For information about L3 interconnect configuration, see Chapter 13, *Interconnects*.

23.10.5.1.1.2 HSI Global Initialization

23.10.5.1.1.2.1 Main Sequence – HSI Global Initialization

This procedure initializes the HSI module after a power-on reset (POR) or software reset.

Table 23-799. HSI Global Initialization

Step	Register/Bit Field/Programming Model	Value
Perform an HSI software reset.	HSI_SYSCONFIG[1] SOFTRESET	0x1
WAIT UNTIL HSI reset is complete.	HSI_SYSSTATUS[0] RESETDONE	= 0x1
Set standby mode configuration.	HSI_SYSCONFIG[13:12] MIDLEMODE	0x-
Set idle mode configuration.	HSI_SYSCONFIG[4:3] SIDLEMODE	0x-
Clock auto gating.	HSI_SYSCONFIG[0] AUTOIDLE	0x-
Set the transmit data rate.	HST_DIVISOR_Pp[7:0] TX_RATE_DIV_VAL	0x-
(Optional) Enable DMA.	DMA_GCR[0] SWITCH_OFF	0x0

23.10.5.1.2 HSI Operational Modes Configuration

23.10.5.1.2.1 HSI Transmit Mode/Receive Mode

23.10.5.1.2.1.1 Main Sequence – Configure HSI Transmitter

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Table 23-800. HSI Configure HSI Transmitter

Step	Register/Bit Field/Programming Model	Value
Set the mode.	HST_MODE_Pp[1:0] MODE_VAL	0x-
Set the data flow type.	HST_MODE_Pp[3:2] FLOW_VAL	0x-
Set the hsi_wake line control.	HST_MODE_Pp[4] WAKE_CTRL	0x-
Set the transmission bit rate	HST_DIVISOR_Pp[7:0] TX_RATE_DIV_VAL	0x-
Set the arbitration mode.	HST_ARBMODE_Pp[0] ARB_VAL	0x-
Set the number of active HSI logical channels.	HST_CHANNELS_Pp[4:0] CHAN_NUM_VAL	0x-
Set the TX FIFO threshold.	HST_MAPPINGf[13:10] THRESHOLD	0x-
Associate the TX FIFO to an HSI port.	HST_MAPPINGf[7] PORT_NUMBER	0x-
Associate the TX FIFO to an HSI logical channel.	HST_MAPPINGf[4:1] CH_NUMBER	0x-
Enable the TX FIFO.	HST_MAPPINGf[0] ENABLE	0x-

23.10.5.1.2.1.2 Main Sequence – Configure HSI Receiver

Table 23-801. HSI Configure HSI Receiver

Step	Register/Bit Field/Programming Model	Value
Set a clock frequency for the error detection counters.	HSR_DIVISOR_Pp[7:0] RX_RATE_DIV_VAL	0x-
Set the number of active HSI logical channels.	HSR_CHANNELS_Pp[4:0] CHAN_NUM_VAL	0x-
Set the frame timeout error counter.	HSR_COUNTERS_Pp[19:0] FT	0x-
Set the tailing bit error counter.	HSR_COUNTERS_Pp[23:20] TB	0x-
Set the frame burst error counter.	HSR_COUNTERS_Pp[31:24] FB	0x-
Associate the RX FIFO to an HSI port.	HSR_MAPPINGf[7] PORT_NUMBER	0x-
Associate the RX FIFO to an HSI logical channel.	HSR_MAPPINGf[4:1] CH_NUMBER	0x-
Enable the RX FIFO.	HSR_MAPPINGf[0] ENABLE	0x-
Set the mode in receive mode.	HSR_MODE_Pp[1:0] MODE_VAL	0x-
Set the data flow type in receive mode.	HSR_MODE_Pp[3:2] FLOW_VAL	0x-

23.10.5.1.2.1.3 Main Sequence – HSI Polling Method

23.10.5.1.2.1.3.1 Sub-sequence – HSI Transmit in Polling Method

Figure 23-229 is a procedure flow chart for HSI transmit in polling method.

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Figure 23-229. HSI Transmit in Polling Method

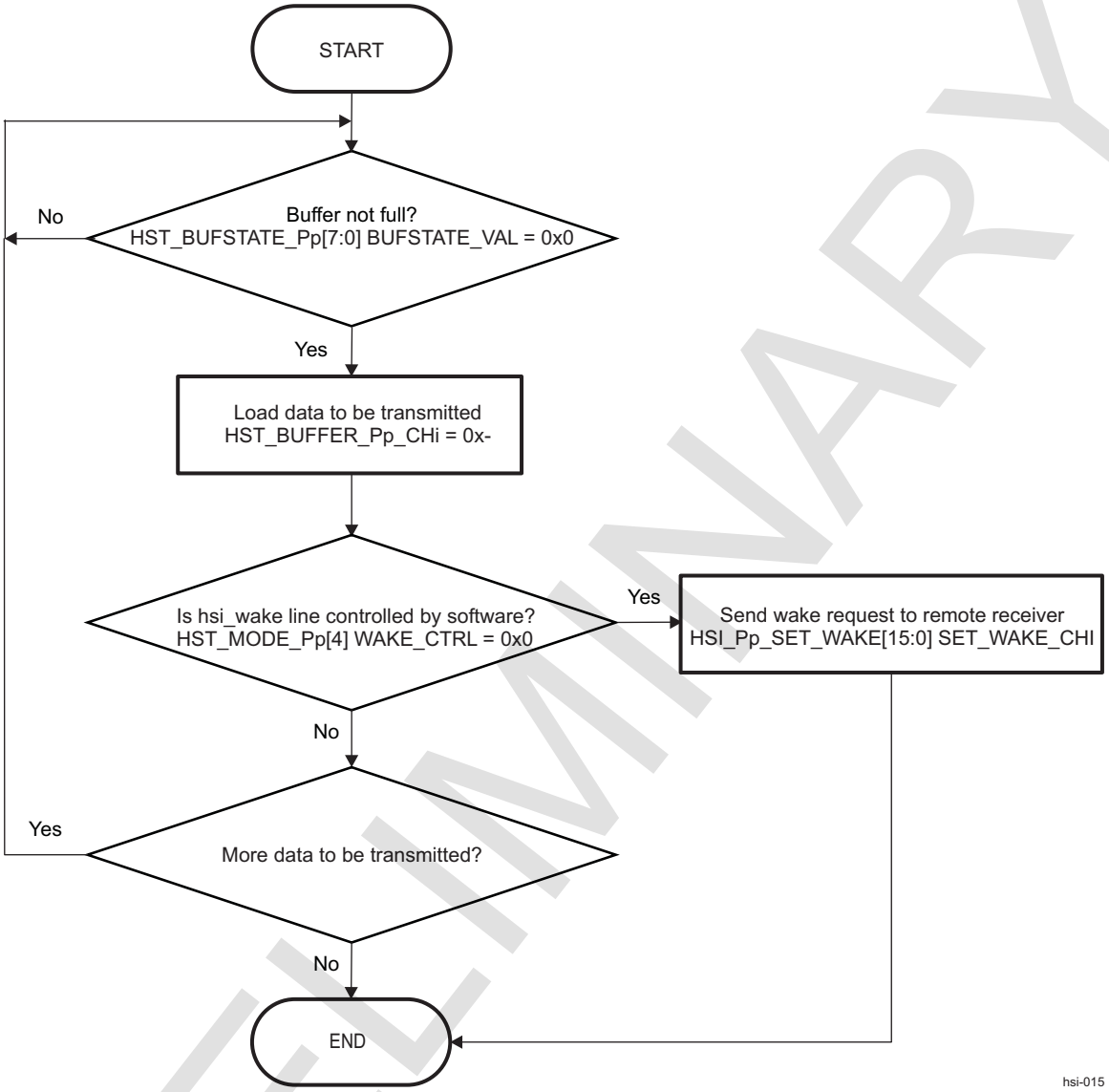

Table 23-802. Register Call Summary for Subsequence – HSI Transmit in Polling Method

Register Name	Register Name	Register Name
HST_BUFSTATE_Pp	HST_BUFFER_Pp_CHN_i	HST_MODE_Pp
HSI_Pp_SET_WAKE		

23.10.5.1.2.1.3.2 Subsequence – HSI Receive in Polling Method

Table 23-803. Event Servicing in HSI Receive in Polling Method

Step	Register/Bit Field/Programming Model	Value
IF: Is there data frame to be read?	HSR_BUFSTATE_Pp[7:0] BUFSTATE_VAL	=0x1
Identify number of words available in RX FIFO for reading.	HSR_MAPPINGf[13:10] WORDS	0x-
Read data from RX FIFO.	HSR_BUFFER_Pp_CHN_i[31:0] DATA	0x-

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Table 23-803. Event Servicing in HSI Receive in Polling Method (continued)

Step	Register/Bit Field/Programming Model	Value
ENDIF		

23.10.5.1.2.1.4 Main Sequence – HSI Interrupt Mode

Table 23-804. HSI Interrupt Mode

Step	Register/Bit Field/Programming Model	Value
Disable DMA engine.	DMA_GCR[0] SWITCH_OFF	0x1
Configure transmitter.	See Table 23-800.	
Configure receiver.	See Table 23-801.	
Enable HSI transmission interrupts.	See Table 23-805.	
WHEN HSI INTERRUPT OCCURS	See Figure 23-230.	
Enable HSI reception interrupts.	See Table 23-807.	
WHEN HSI INTERRUPT OCCURS	See Table 23-803.	

23.10.5.1.2.1.4.1 Subsequence – Interrupt Transmit Mode

Table 23-805. Enable HSI Transmit Interrupts

Step	Register/Bit Field/Programming Model	Value
Enable data accepted interrupt.	HSI_Pp_M_IRQrU_ENABLE[7:0] HST_ACCEPTED_ENI and/or HSI_Pp_D_IRQrU_ENABLE[7:0] HST_ACCEPTED_ENI and/or HSI_Pp_M_IRQr_ENABLE[7:0] HST_ACCEPTED_ENI and/or HSI_Pp_D_IRQr_ENABLE[7:0] HST_ACCEPTED_ENI	0x-

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Figure 23-230 is a procedure flow chart for event servicing in HSI transmission mode.

Figure 23-230. Event Servicing in HSI Transmission Mode

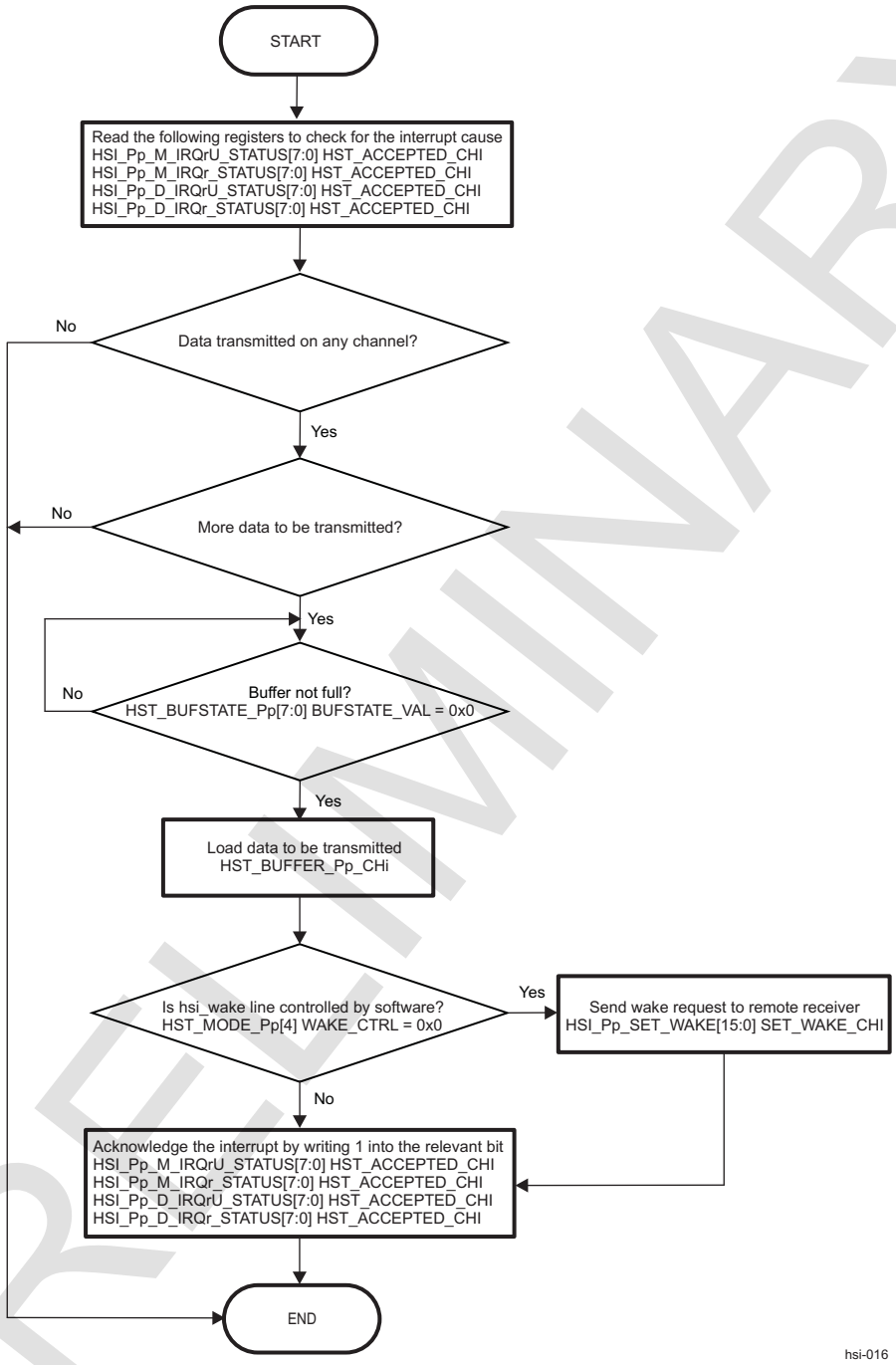

Table 23-806. Register Call Summary for Subsequence – Event Servicing in HSI Transmission Mode

Register Name	Register Name	Register Name
HSI_Pp_M_IRQrU_STATUS[7:0]HST_ACCEPTED_ CHI	HSI_Pp_D_IRQrU_STATUS[7:0]HST_ACCEPTED_CHI	HSI_Pp_M_IRQr_STATUS[7:0]HST_ACCEPTED_CHI
HSI_Pp_D_IRQr_STATUS[7:0] HST_ACCEPTED_CHI	HST_BUFFER_Pp_CHN_i[31:0] DATA	HST_MODE_Pp[4] WAKE_CTRL

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Table 23-806. Register Call Summary for Subsequence – Event Servicing in HSI Transmission Mode (continued)

Register Name	Register Name	Register Name
HSI_Pp_SET_WAKE[15:0] HSI_SET_WAKE_CHi		

23.10.5.1.2.1.4.2 Subsequence – Interrupt Receive Mode

Table 23-807. Enable HSI Receive Interrupts

Step	Register/Bit Field/Programming Model	Value
Enable break detected interrupt.	HSI_Pp_M_IRQrU_ENABLE[25] HSR_BREAK and/or HSI_Pp_D_IRQrU_ENABLE[25] HSR_BREAK and/or HSI_Pp_M_IRQr_ENABLE[25] HSR_BREAK and/or HSI_Pp_D_IRQr_ENABLE[25] HSR_BREAK	0x1
Enable wake detected interrupt.	HSI_Pp_M_IRQrU_ENABLE[26] HSR_WAKE and/or HSI_Pp_D_IRQrU_ENABLE[26] HSR_WAKE and/or HSI_Pp_M_IRQr_ENABLE[26] HSR_WAKE and/or HSI_Pp_D_IRQr_ENABLE[26] HSR_WAKE	0x1
Enable overrun interrupt.	HSI_Pp_M_IRQrU_ENABLE[23:16] HSR_OVERRUN_ENI and/or HSI_Pp_D_IRQrU_ENABLE[23:16] HSR_OVERRUN_ENI and/or HSI_Pp_M_IRQr_ENABLE[23:16] HSR_OVERRUN_ENI and/or HSI_Pp_D_IRQr_ENABLE[23:16] HSR_OVERRUN_ENI	0x-
Enable data available interrupt.	HSI_Pp_M_IRQrU_ENABLE[15:8] HSR_AVAILABLE_ENI and/or HSI_Pp_D_IRQrU_ENABLE[15:8] HSR_AVAILABLE_ENI and/or HSI_Pp_M_IRQr_ENABLE[15:8] HSR_AVAILABLE_ENI and/or HSI_Pp_D_IRQr_ENABLE[15:8] HSR_AVAILABLE_ENI	0x-

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Figure 23-231 is a procedure flow chart for event servicing in HSI reception mode.

Figure 23-231. Event Servicing in HSI Reception Mode

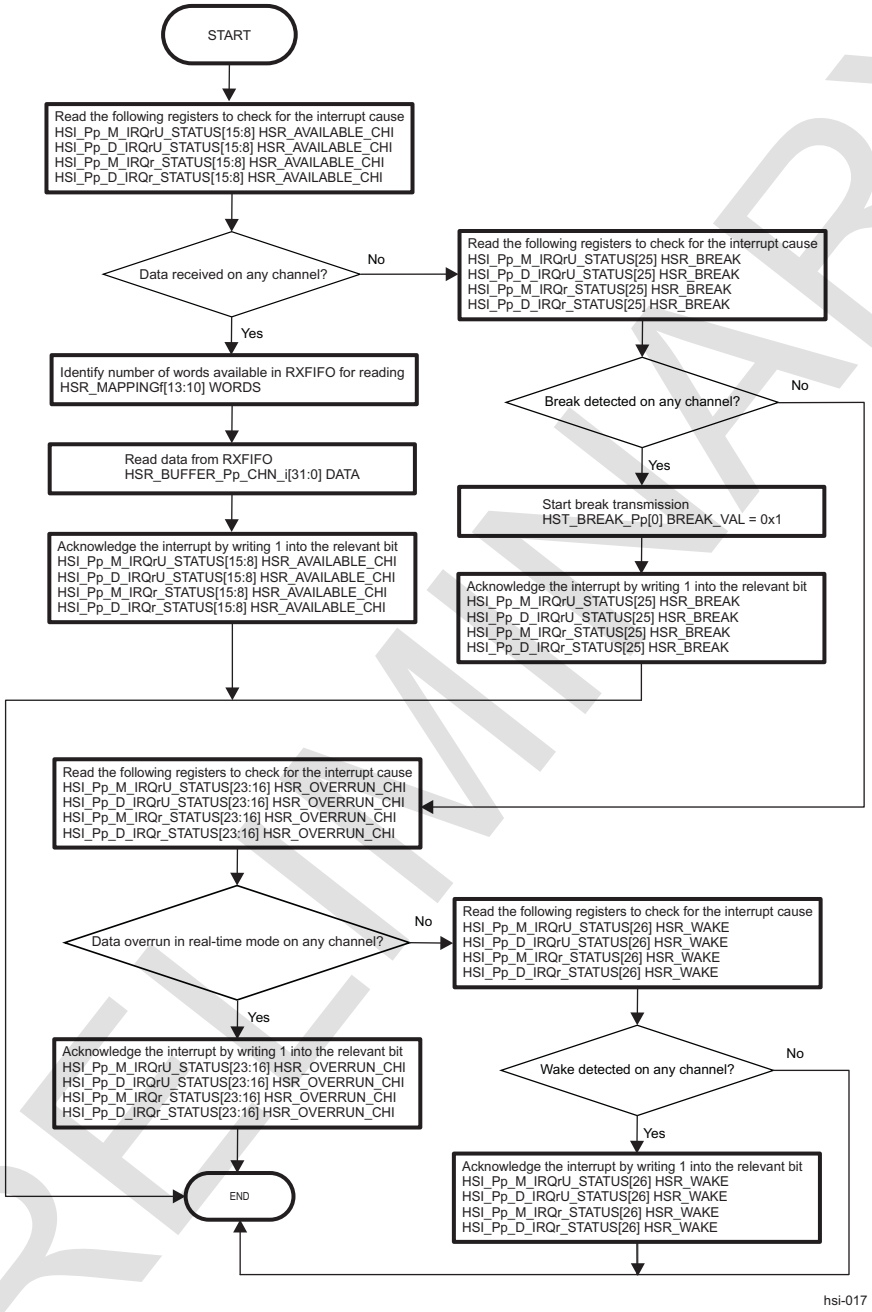

Table 23-808. Register Call Summary for Subsequence – Event Servicing in HSI Reception Mode

Register Name	Register Name	Register Name
HSI_Pp_M_IRQrU_STATUS[15:8] HSR_AVAILABLE_CHI	HSI_Pp_D_IRQrU_STATUS[15:8] HSR_AVAILABLE_CHI	HSI_Pp_M_IRQr_STATUS[15:8] HSR_AVAILABLE_CHI
HSI_Pp_D_IRQr_STATUS[15:8] HSR_AVAILABLE_CHI	HSR_MAPPINGf[13:10] WORDS	HSR_BUFFER_Pp_CHN_i[31:0] DATA
HSI_Pp_M_IRQrU_STATUS[25] HSR_BREAK	HSI_Pp_D_IRQrU_STATUS[25] HSR_BREAK	HSI_Pp_M_IRQr_STATUS[25] HSR_BREAK
HSI_Pp_D_IRQr_STATUS[25] HSR_BREAK	HST_BREAK_Pp[0] BREAK_VAL	HSI_Pp_M_IRQrU_STATUS[23:16] HSR_OVERRUN_CHI

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Table 23-808. Register Call Summary for Subsequence – Event Servicing in HSI Reception Mode (continued)

Register Name	Register Name	Register Name
HSI_Pp_D_IRQrU_STATUS[23:16] HSR_OVERRUN_CHI	HSI_Pp_M_IRQr_STATUS[23:16] HSR_OVERRUN_CHI	HSI_Pp_D_IRQr_STATUS[23:16] HSR_OVERRUN_CHI

23.10.5.1.2.1.5 Main Sequence – HSI DMA Mode

23.10.5.1.2.1.5.1 Sub-sequence – DMA Configuration

Table 23-809. HSI DMA Configuration

Step	Register/Bit Field/Programming Model	Value
Perform a DMA software reset.	DMA_GRST[0] SWRESET	0x1
WAIT UNTIL DMA reset is complete.	DMA_GRST[0] SWRESET	= 0x0
Set autoidle mode configuration for DMA.	DMA_GCR[3] AUTOGATING	0x1
Configure HSI DMI receiver.	See Table 23-810.	
Configure HSI DMI transmit.	See Table 23-811.	
Enable DMA interrupts.	See Section 23.10.5.1.2.1.5.4.	
Enable DMA channel to start DMA transfer.	DMA_CCR_CSDP_i[23] ENABLE	0x1
WHEN DMA INTERRUPT OCCURS	See Table 23-804.	

23.10.5.1.2.1.5.2 Subsequence – DMA Receive Mode

Table 23-810. Configure DMA Receive Mode

Step	Register/Bit Field/Programming Model	Value
Set the transfer source to peripheral port.	DMA_CCR_CSDP_i[5:2] SRC	0x9
(Optional) Set the source burst enable.	DMA_CCR_CSDP_i[8:7] SRC_BURST_EN	0x1
Set the transfer destination to memory port.	DMA_CCR_CSDP_i[12:9] DST	0x8
(Optional) Set the destination burst enable.	DMA_CCR_CSDP_i[15:14] DST_BURST_EN	0x1
Set the source addressing mode to constant address.	DMA_CCR_CSDP_i[29:28] SRC_ADD_MODE	0x0
Set the destination addressing mode to post-incremented address.	DMA_CCR_CSDP_i[31:30] DST_ADD_MODE	0x1
Set the source start address.	DMA_CSSA_i[31:0] ADDR	0x-
Set the destination start address.	DMA_CDSA_i[31:0] ADDR	0x-
Set the number of elements in a block.	DMA_CEN_i[15:0] SIZE	0x-

23.10.5.1.2.1.5.3 Subsequence – DMA Transmit Mode

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Table 23-811. Configure DMA Transmit Mode

Step	Register/Bit Field/Programming Model	Value
Set the transfer source to memory port.	DMA_CCR_CSDP_i[5:2] SRC	0x8
(Optional) Set the source burst enable.	DMA_CCR_CSDP_i[8:7] SRC_BURST_EN	0x1
Set the transfer destination to peripheral port.	DMA_CCR_CSDP_i[12:9] DST	0x9
(Optional) Set the destination burst enable to single access.	DMA_CCR_CSDP_i[15:14] DST_BURST_EN	0x1
Set the source addressing mode to post-incremented address.	DMA_CCR_CSDP_i[29:28] SRC_ADD_MODE	0x1
Set the destination addressing mode to constant address.	DMA_CCR_CSDP_i[31:30] DST_ADD_MODE	0x0
Set the source start address.	DMA_CSSA_i[31:0] ADDR	0x-
Set the destination start address.	DMA_CDSA_i[31:0] ADDR	0x-
Set the number of elements in a block.	DMA_CEN_i[15:0] SIZE	0x-

23.10.5.1.2.1.5.4 Subsequence – Enable DMA Interrupts

Table 23-812. Enable DMA Interrupts

Step	Register/Bit Field/Programming Model	Value
Enable the DMA channels that shall generate an interrupt to a processor (MPU and/or DSP).	HSI_DMA_M_IRQENABLE[15:0] DMA_EN_CHI and/or HSI_DMA_D_IRQENABLE[15:0] DMA_EN_CHI	0x-
Enable the DMA full-block interrupt event.	DMA_CSR_CCIR_i[5] BLOCK_IE	0x1
Enable the DMA half-block interrupt event.	DMA_CSR_CCIR_i[2] HALF_IE	0x1
Enable the DMA time-out overflow interrupt event.	DMA_CSR_CCIR_i[0] TOUT_IE	0x1

23.10.5.1.2.1.5.5 Subsequence – DMA Interrupt Servicing

Table 23-813. Event Servicing in DMA Transmit/Receive Mode

Step	Register/Bit Field /Programming Model	Value
Identify which DMA channel has generated an interrupt.	HSI_DMA_M_IRQSTATUS[15:0] DMA_CHI and/or HSI_DMA_D_IRQSTATUS[15:0] DMA_CHI	0x-
Identify the interrupt event type.	DMA_CSR_CCIR_i[21] BLOCK_IS and/or DMA_CSR_CCIR_i[18] HALF_IS and/or DMA_CSR_CCIR_i[16] TOUT_IS	0x-
Acknowledge DMA global interrupt by setting the relevant bit to 1.	HSI_DMA_M_IRQSTATUS[15:0] DMA_CHI and/or HSI_DMA_D_IRQSTATUS[15:0] DMA_CHI	0x-

23.10.5.1.2.1.6 Main Sequence – HSI Error Reporting

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Table 23-814. Enable HSI Error Interrupts

Step	Register/Bit Field/Programming Model	Value
Enable error detected interrupt.	HSI_Pp_M_IRQrU_ENABLE[24] HSR_ERROR and/or HSI_Pp_D_IRQrU_ENABLE[24] HSR_ERROR and/or HSI_Pp_M_IRQr_ENABLE[24] HSR_ERROR and/or HSI_Pp_D_IRQr_ENABLE[24] HSR_ERROR	0x1

Table 23-815. Event Servicing Error

Step	Register/Bit Field/Programming Model	Value
Read interrupt status register.	HSI_Pp_M_IRQrU_STATUS[24] HSR_ERROR and/or HSI_Pp_D_IRQrU_STATUS[24] HSR_ERROR and/or HSI_Pp_M_IRQr_STATUS[24] HSR_ERROR and/or HSI_Pp_D_IRQr_STATUS[24] HSR_ERROR	0x-
Identify the interrupt event type.	HSR_ERROR_Pp[0] SIG HSR_ERROR_Pp[1] FTE HSR_ERROR_Pp[4] FBE HSR_ERROR_Pp[7] RME HSR_ERROR_Pp[11] TME	0x-
Clear the event by writing 1 into the relevant bit.	HSR_ERRORACK_Pp[0] SIG HSR_ERRORACK_Pp[1] FTE HSR_ERRORACK_Pp[4] FBE HSR_ERRORACK_Pp[7] RME HSR_ERRORACK_Pp[11] TME	0x1
Acknowledge the interrupt by writing 1 into the relevant bit.	HSI_Pp_M_IRQrU_STATUS[24] HSR_ERROR and/or HSI_Pp_D_IRQrU_STATUS[24] HSR_ERROR and/or HSI_Pp_M_IRQr_STATUS[24] HSR_ERROR and/or HSI_Pp_D_IRQr_STATUS[24] HSR_ERROR	0x1

23.10.6 HSI Register Manual

23.10.6.1 HSI Instance Summary

Table 23-816 summarizes the HSI instance.

Table 23-816. HSI Instance Summary

Module Name	Module Base Address	Size
HSI_TOP	0x4A05 8000	5 KB
HSI_DMA_CHANNELS	0x4A05 9800	1 KB
HSI_PORTS	0x4A05 A000	8 KB

23.10.6.2 HSI_TOP Registers

23.10.6.2.1 HSI_TOP Register Summary

Table 23-817 summarizes the mapping of the HSI_TOP registers.

Table 23-817. HSI_TOP Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	HSI_TOP Physical Address
HSI_REVISION	R	32	0x0000 0000	0x4A05 8000
HSI_HWINFO	R	32	0x0000 0004	0x4A05 8004
HSI_SYSCONFIG	RW	32	0x0000 0010	0x4A05 8010
HSI_SYSSTATUS	R	32	0x0000 0014	0x4A05 8014

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Table 23-817. HSI_TOP Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	HSI_TOP Physical Address
HSI_Pp_M_IRQrU_STATUS (1)	RW	32	0x0000 0408 + (0x10 * b) + (0x8 * r)	0x4A05 8408 + (0x10 * b) + (0x8 * r)
HSI_Pp_M_IRQrU_ENABLE (1)	RW	32	0x0000 040C + (0x10 * b) + (0x8 * r)	0x4A05 840C + (0x10 * b) + (0x8 * r)
HSI_Pp_D_IRQrU_STATUS (1)	RW	32	0x0000 0430 + (0x10 * b) + (0x8 * r)	0x4A05 8430 + (0x10 * b) + (0x8* r)
HSI_Pp_D_IRQrU_ENABLE (1)	RW	32	0x0000 0434 + (0x10 * b) + (0x8 * r)	0x4A05 8434 + (0x10 * b) + (0x8 * r)
HSI_DMA_M_IRQSTATUS	RW	32	0x0000 0800	0x4A05 8800
HSI_DMA_M_IRQENABLE	RW	32	0x0000 0804	0x4A05 8804
HSI_Pp_M_IRQr_STATUS (1)	RW	32	0x0000 0808 + (0x10 * b) + (0x8 * r)	0x4A05 8808 + (0x10 * b) + (0x8 * r)
HSI_Pp_M_IRQr_ENABLE (1)	RW	32	0x0000 080C + (0x10 * b) + (0x8 * r)	0x4A05 880C + (0x10 * b) + (0x8 * r)
HSI_DMA_D_IRQSTATUS	RW	32	0x0000 0828	0x4A05 8828
HSI_DMA_D_IRQENABLE	RW	32	0x0000 082C	0x4A05 882C
HSI_Pp_D_IRQr_STATUS (2)	RW	32	0x0000 0830 + (0x10 * b) + (0x8 * r)	0x4A05 8830 + (0x10 * b) + (0x8 * r)
HSI_Pp_D_IRQr_ENABLE (2)	RW	32	0x0000 0834 + (0x10 * b) + (0x8 * r)	0x4A05 8834 + (0x10 * b) + (0x8 * r)
HSI_Pp_WAKE (2)	RW	32	0x0000 0C00 + (0x10 * b)	0x4A05 8C00 + (0x10 * b)
HSI_Pp_CLEAR_WAKE (2)	RW	32	0x0000 0C04 + (0x10 * b)	0x4A05 8C04 + (0x10 * b)
HSI_Pp_SET_WAKE (2)	RW	32	0x0000 0C08 + (0x10 * b)	0x4A05 8C08 + (0x10 * b)
RESERVED	RW	32	0x0000 1000	0x4A05 9000
DMA_GCR	RW	32	0x0000 1100	0x4A05 9100
DMA_GRST	RW	32	0x0000 1200	0x4A05 9200

(1) p = 1 to 2
r = 0 to 1
b = 0 to 1 (for p = 1, b = 0 and p = 2, b = 1)

(2) p = 1 to 2
r = 0 to 1
b = 0 to 1 (for p = 1, b = 0 and p = 2, b = 1)

23.10.6.2.2 HSI_TOP Register Description

Table 23-818 through Table 23-858 describe the HSI_TOP registers.

Table 23-818. HSI_REVISION

Address Offset	0x0000 0000		
Physical Address	0x4A05 8000	**Instance**	HSI_TOP
Description	IP Revision Identifier (X.Y.R) Used by software to track features, bugs, and compatibility		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP Revision	R	TI Internal Data

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Table 23-819. Register Call Summary for Register HSI_REVISION

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- HSI_TOP Register Summary: [0]

Table 23-820. HSI_HWINFO

Address Offset	0x0000 0004		
Physical Address	0x4A05 8004	**Instance**	HSI_TOP
Description	Information about the IP module hardware configuration, that is, typically the module HDL generics (if any). Actual field format and encoding is decided by the module designer.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HWINFO																															

Bits	Field Name	Description	Type	Reset
31:0	HWINFO	IP module hardware configuration	R	See (1).

(1) TI Internal Data

Table 23-821. Register Call Summary for Register HSI_HWINFO

MIPI-HSI

- HSI_TOP Register Summary: [0]

Table 23-822. HSI_SYSCONFIG

Address Offset	0x0000 0010		
Physical Address	0x4A05 8010	**Instance**	HSI_TOP
Description	This register allows controlling various parameters of the L4_CFG interface		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																		MIDLEMODE		RESERVED							SIDLEMODE		FREE_EMU	SOFTRESET	AUTOIDLE

Bits	Field Name	Description	Type	Reset
31:14	RESERVED	Reserved	R	0x00000
13:12	MIDLEMODE	Master interface power management, standby/wait control 0x0: Force-standby 0x1: No-standby 0x2: Smart-standby 0x3: Smart-standby wakeup	RW	0x2
11:5	RESERVED	Reserved	R	0x00

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Bits	Field Name	Description	Type	Reset
4:3	SIDLEMODE	Slave interface power management, request/acknowledgment control 0x0: Force-idle 0x1: No-idle 0x2: Smart-idle 0x3: Smart-idle wakeup	RW	0x2
2	FREE_EMU	Sensitivity to emulation (debug) suspend input signal 0x0: Module is sensitive to emulation suspend. 0x1: Module is not sensitive to emulation suspend.	RW	0x0
1	SOFTRESET	Software reset 0x0: No reset applied 0x1: Software reset applied	RW	0x0
0	AUTOIDLE	Internal interface clock gating strategy 0x0: Interface clock is free-running 0x1: Automatic interface clock gating strategy, based on interconnect interface activity	RW	0x1

Table 23-823. Register Call Summary for Register HSI_SYSCONFIG

MIPI-HSI

- Software Reset: [0]
- Power Management: [1] [2] [3]
- HSI Module Power-Management Modes: [4] [5] [6]
- Global Initialization: [7] [8] [9] [10]
- HSI_TOP Register Summary: [11]

Table 23-824. HSI_SYSSTATUS

Address Offset	0x0000 0014		
Physical Address	0x4A05 8014	**Instance**	HSI_TOP
Description	Status on module (reset done on bit 0, available for more status information)		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESETDONE																															

Bits	Field Name	Description	Type	Reset
31:0	RESETDONE	internal reset monitoring Read 0x0: Internal reset is ongoing. Read 0x1: Internal reset is completed and the module is ready to be used.	R	0x0000 0001

Table 23-825. Register Call Summary for Register HSI_SYSSTATUS

MIPI-HSI

- Software Reset: [0]
- Global Initialization: [1]
- HSI_TOP Register Summary: [2]

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Table 23-826. HSI_Pp_M_IRQrU_STATUS

Address Offset	0x0000 0408 + (0x10 * b) + (0x8 * r)	**Index**	p = 1 to 2 r = 0 to 1 b = 0 to 1 (for p = 1, b = 0 and p = 2, b = 1)
Physical Address	0x4A05 8408 + (0x10 * b) + (0x8 * r)	**Instance**	HSI_TOP
Description	IRQ status register for FIFO (8..15) events and for port *p* break, wake and error events Events will signal interrupt for MPU line r (Mpuirq_r) Read 0: Event has not occurred. Read 1: Event has occurred. Write 0: Bit stays unchanged. Write 1: Bit is reset to 0.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					HSR_WAKE	HSR_BREAK	HSR_ERROR	HSR_OVERRUN_CHI								HSR_AVAILABLE_CHI								HST_ACCEPTED_CHI							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Reserved	R	0x00
26	HSR_WAKE	Wake detected on any channel 8..15	RW	0x0
25	HSR_BREAK	Break detected on any channel 8..15	RW	0x0
24	HSR_ERROR	Error detected on any channel 8..15	RW	0x0
23:16	HSR_OVERRUN_CHI	Data overrun in real-time mode channel 8..15 (LSB stands for channel 8 and MSB for channel 15).	RW	0x00
15:8	HSR_AVAILABLE_CHI	Data received on channel 8..15 (LSB stands for channel 8 and MSB for channel 15). The status bit shows data on the respective channel when data are in the FIFO. Clearing the status bit has no effect when the FIFO is not empty.	RW	0x00
7:0	HST_ACCEPTED_CHI	Data transmitted on channel 8..15 (LSB stands for channel 8 and MSB for channel 15)	RW	0xFF

Table 23-827. Register Call Summary for Register HSI_Pp_M_IRQrU_STATUS

MIPI-HSI

- Interrupt Requests: [0] [1] [2] [3] [4] [5]
- Interrupts: [6]
- HSI Operational Modes Configuration: [7] [8] [9] [10] [11] [12]
- HSI_TOP Register Summary: [13]

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Table 23-828. HSI_Pp_M_IRQrU_ENABLE

Address Offset	0x0000 040C + (0x10 * b) + (0x8 * r)	p = 1 to 2 r = 0 to 1 b = 0 to 1 (for p = 1, b = 0 and p = 2, b = 1)
Physical Address	0x4A05 840C + (0x10 * b) + (0x8 * r) **Instance**	HSI_TOP
Description	IRQ enable register for FIFO (8..15) events and for port *p* break, wake and error events signaled to MPU line r (Mpuirq_r) Write 0: Event is masked. Write 1: Event is enabled.	
Type	RW	

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					HSR_WAKE	HSR_BREAK	HSR_ERROR	HSR_OVERRUN_ENI								HSR_AVAILABLE_ENI								HST_ACCEPTED_ENI							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Reserved	R	0x00
26	HSR_WAKE	Wake interrupt enable for all channels 8..15	RW	0x0
25	HSR_BREAK	Break interrupt enable for all channels 8..15	RW	0x0
24	HSR_ERROR	Error interrupt enable for all channels 8..15	RW	0x0
23:16	HSR_OVERRUN_ENI	Overrun interrupt enable for channel 8..15 (LSB stands for channel 8 and MSB for channel 15)	RW	0x00
15:8	HSR_AVAILABLE_ENI	Data available interrupt enable for channel 8..15 (LSB stands for channel 8 and MSB for channel 15)	RW	0x00
7:0	HST_ACCEPTED_ENI	Data accepted interrupt enable for channel 8..15 (LSB stands for channel 8 and MSB for channel 15)	RW	0x00

Table 23-829. Register Call Summary for Register HSI_Pp_M_IRQrU_ENABLE

MIPI-HSI

- Interrupt Requests: [0] [1] [2] [3] [4] [5]
- Interrupts: [6]
- HSI Operational Modes Configuration: [7] [8] [9] [10] [11] [12]
- HSI_TOP Register Summary: [13]

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Table 23-830. HSI_Pp_D_IRQrU_STATUS

Address Offset	0x0000 0430 + (0x10 * b) + (0x8 * r)	**Index**	p = 1 to 2 r = 0 to 1 b = 0 to 1 (for p = 1, b = 0 and p = 2, b = 1)
Physical Address	0x4A05 8430 + (0x10 * b) + (0x8* r)	**Instance**	HSI_TOP
Description	IRQ status register for FIFO (8..15) events and for port *p* break, wake and error events. Events will signal interrupt for DSP line r (Dspirq_r) Read 0: Event has not occurred. Read 1: Event has occurred. Write 0: Bit stays unchanged. Write 1: Bit is reset to 0.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					HSR_WAKE	HSR_BREAK	HSR_ERROR	HSR_OVERRUN_CHI								HSR_AVAILABLE_CHI								HST_ACCEPTED_CHI							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Reserved	R	0x00
26	HSR_WAKE	Wake detected on any channel 8..15	RW	0x0
25	HSR_BREAK	Break detected on any channel 8..15	RW	0x0
24	HSR_ERROR	Error on any channel 8..15	RW	0x0
23:16	HSR_OVERRUN_CHI	Data overrun in real-time mode channel 8..15 (LSB stands for channel 8 and MSB for channel 15)	RW	0x00
15:8	HSR_AVAILABLE_CHI	Data received on channel 8..15 (LSB stands for channel 8 and MSB for channel 15). The status bit shows data on the respective channel when data are in the FIFO. Clearing the status bit has no effect when the FIFO is not empty.	RW	0x00
7:0	HST_ACCEPTED_CHI	Data transmitted on channel 8..15 (LSB stands for channel 8 and MSB for channel 15)	RW	0xFF

Table 23-831. Register Call Summary for Register HSI_Pp_D_IRQrU_STATUS

MIPI-HSI

- Interrupt Requests: [0] [1] [2] [3] [4] [5]
- Interrupts: [6]
- HSI Operational Modes Configuration: [7] [8] [9] [10] [11] [12]
- HSI_TOP Register Summary: [13]

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Table 23-832. HSI_Pp_D_IRQrU_ENABLE

Address Offset	0x0000 0434 + (0x10 * b) + (0x8 * r)	**Index**	p = 1 to 2 r = 0 to 1 b = 0 to 1 (for p = 1, b = 0 and p = 2, b = 1)
Physical Address	0x4A05 8434 + (0x10 * b) + (0x8 * r)	**Instance**	HSI_TOP
Description	IRQ enable register for FIFO (8..15) events and for port p break, wake and error events signaled to DSP line r (Dspirq_r) Write 0: Event is masked. Write 1:Event is enabled.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					HSR_WAKE	HSR_BREAK	HSR_ERROR	HSR_OVERRUN_ENI								HSR_AVAILABLE_ENI								HST_ACCEPTED_ENI							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Reserved	R	0x00
26	HSR_WAKE	Wake interrupt enable for channel 8..15	RW	0x0
25	HSR_BREAK	Break interrupt enable for channel 8..15	RW	0x0
24	HSR_ERROR	Error interrupt enable for channel 8..15	RW	0x0
23:16	HSR_OVERRUN_ENI	Overrun interrupt enable for channel 8..15	RW	0x00
15:8	HSR_AVAILABLE_ENI	Data available interrupt enable for channel 8..15 (LSB stands for channel 8 and MSB for channel 15)	RW	0x00
7:0	HST_ACCEPTED_ENI	Data accepted interrupt enable for channel 8..15 (LSB stands for channel 8 and MSB for channel 15)	RW	0x00

Table 23-833. Register Call Summary for Register HSI_Pp_D_IRQrU_ENABLE

MIPI-HSI

- Interrupt Requests: [0] [1] [2] [3] [4] [5]
- Interrupts: [6]
- HSI Operational Modes Configuration: [7] [8] [9] [10] [11] [12]
- HSI_TOP Register Summary: [13]

Table 23-834. HSI_DMA_M_IRQSTATUS

Address Offset	0x0000 0800		
Physical Address	0x4A05 8800	**Instance**	HSI_TOP
Description	This register collects status for all of the DMA events able to generate interrupt to MPU: Read 0: Event has not occurred. Read 1: Event has occurred. Write 0: Bit stays unchanged. Write 1: Bit is reset to 0.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																DMA_CHI															

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Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x0000
15:0	DMA_CHI	Channel 0..15 status (LSB stands for channel 0 and MSB for channel 15)	RW	0x0000

Table 23-835. Register Call Summary for Register HSI_DMA_M_IRQSTATUS

MIPI-HSI

- Interrupt Requests: [0]
- Interrupts: [1] [2]
- HSI Operational Modes Configuration: [3] [4]
- HSI_TOP Register Summary: [5]

Table 23-836. HSI_DMA_M_IRQENABLE

Address Offset	0x0000 0804		
Physical Address	0x4A05 8804	**Instance**	HSI_TOP
Description	This register masks and unmasks DMA sources of interrupt to MPU: Write 0: event is masked Write 1: event is enabled		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																DMA_EN_CHI															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x0000
15:0	DMA_EN_CHI	Channel 0..15 status (LSB stands for channel 0 and MSB for channel 15)	RW	0x0000

Table 23-837. Register Call Summary for Register HSI_DMA_M_IRQENABLE

MIPI-HSI

- Interrupt Requests: [0]
- Interrupts: [1]
- HSI Operational Modes Configuration: [2]
- HSI_TOP Register Summary: [3]

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Table 23-838. HSI_Pp_M_IRQr_STATUS

Address Offset	0x0000 0808 + (0x10 * b) + (0x8 * r)	**Index**	p = 1 to 2 r = 0 to 1 b = 0 to 1 (for p = 1, b = 0 and p = 2, b = 1)
Physical Address	0x4A05 8808 + (0x10 * b) + (0x8 * r)	**Instance**	HSI_TOP
Description	IRQ status register for FIFO (0..7) events and for port p break, wake and error events Events will signal interrupt for MPU line r (Mpuirq_r) Read 0: Event has not occurred. Read 1: Event has occurred. Write 0: Bit stays unchanged. Write 1: Bit is reset to 0.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					HSR_WAKE	HSR_BREAK	HSR_ERROR	HSR_OVERRUN_CHI								HSR_AVAILABLE_CHI								HST_ACCEPTED_CHI							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Reserved	R	0x00
26	HSR_WAKE	Wake detected on Port p	RW	0x0
25	HSR_BREAK	Break detected on Port p	RW	0x0
24	HSR_ERROR	Error on Port p	RW	0x0
23:16	HSR_OVERRUN_CHI	Data overrun in real time mode channel 0..7 (LSB stands for channel 0 and MSB for channel 7)	RW	0x00
15:8	HSR_AVAILABLE_CHI	Data received on channel 0..7 (LSB stands for channel 0 and MSB for channel 7). The status bit shows data on the respective channel when data are in the FIFO. Clearing the status bit has no effect when the FIFO is not empty.	RW	0x00
7:0	HST_ACCEPTED_CHI	Data transmitted on channel 0..7 (LSB stands for channel 0 and MSB for channel 7)	RW	0xFF

Table 23-839. Register Call Summary for Register HSI_Pp_M_IRQr_STATUS

MIPI-HSI

- Interrupt Requests: [0] [1] [2] [3] [4] [5]
- Interrupts: [6]
- HSI Operational Modes Configuration: [7] [8] [9] [10] [11] [12]
- HSI_TOP Register Summary: [13]

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Table 23-840. HSI_Pp_M_IRQr_ENABLE

Address Offset	0x0000 080C + (0x10 * b) + (0x8 * r)	**Index**	p = 1 to 2 r = 0 to 1 b = 0 to 1 (for p = 1, b = 0 and p = 2, b = 1)
Physical Address	0x4A05 880C + (0x10 * b) + (0x8 * r)	**Instance**	HSI_TOP
Description	IRQ enable register for FIFO (0..7) events and for port p break, wake and error events signaled to MPU line r (Mpuirq_r) Write 0: Event is masked. Write 1: Event is enabled.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					HSR_WAKE	HSR_BREAK	HSR_ERROR	HSR_OVERRUN_ENI								HSR_AVAILABLE_ENI								HST_ACCEPTED_ENI							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Reserved	R	0x00
26	HSR_WAKE	Wake interrupt enable for Port p	RW	0x0
25	HSR_BREAK	Break interrupt enable for Port p	RW	0x00
24	HSR_ERROR	Error interrupt enable for Port p	RW	0x0
23:16	HSR_OVERRUN_ENI	Overrun interrupt enable for channel 0..7 (LSB stands for channel 0 and MSB for channel 7)	RW	0x00
15:8	HSR_AVAILABLE_ENI	Data available interrupt enable for channel 0..7 (LSB stands for channel 0 and MSB for channel 7)	RW	0x00
7:0	HST_ACCEPTED_ENI	Data accepted interrupt enable for channel 0..7 (LSB stands for channel 0 and MSB for channel 7)	RW	0x00

Table 23-841. Register Call Summary for Register HSI_Pp_M_IRQr_ENABLE

MIPI-HSI

- Interrupt Requests: [0] [1] [2] [3] [4] [5]
- Interrupts: [6]
- HSI Operational Modes Configuration: [7] [8] [9] [10] [11] [12]
- HSI_TOP Register Summary: [13]

Table 23-842. HSI_DMA_D_IRQSTATUS

Address Offset	0x0000 0828		
Physical Address	0x4A05 8828	**Instance**	HSI_TOP
Description	IRQ status register for all DMA events. Events generate interrupt for DSP. Read 0: Event has not occurred; Read 1: Event has occurred ; Write 0: Bit stays unchanged; Write 1: Bit is reset to 0.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																DMA_CHI															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x0000
15:0	DMA_CHI	IRQ event happened on DMA channel 0..15 (LSB stands for channel 0 and MSB for channel 15).	RW	0x0000

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Table 23-843. Register Call Summary for Register HSI_DMA_D_IRQSTATUS

MIPI-HSI

- Interrupt Requests: [0]
- Interrupts: [1] [2]
- HSI Operational Modes Configuration: [3] [4]
- HSI_TOP Register Summary: [5]

Table 23-844. HSI_DMA_D_IRQENABLE

Address Offset	0x0000 082C		
Physical Address	0x4A05 882C	**Instance**	HSI_TOP
Description	IRQ enable register for all DMA events signaled to DSP. Write 0: Event is masked. Write 1: Event is enabled.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																DMA_EN_CHI															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x0000
15:0	DMA_EN_CHI	Channel 0..15 (LSB stands for channel 0 and MSB for channel 15)	RW	0x0000

Table 23-845. Register Call Summary for Register HSI_DMA_D_IRQENABLE

MIPI-HSI

- Interrupt Requests: [0]
- Interrupts: [1]
- HSI Operational Modes Configuration: [2]
- HSI_TOP Register Summary: [3]

Table 23-846. HSI_Pp_D_IRQr_STATUS

Address Offset	0x0000 0830 + (0x10 * b) + (0x8 * r)	**Index**	p = 1 to 2 r = 0 to 1 b = 0 to 1 (for p = 1, b = 0 and p = 2, b = 1)
Physical Address	0x4A05 8830 + (0x10 * b) + (0x8 * r)	**Instance**	HSI_TOP
Description	IRQ status register for FIFO (0..7) events and for port p break, wake and error events Events will signal interrupt for DSP line r (Dspirq_r) Read 0: Event has not occurred. Read 1: Event has occurred. Write 0: Bit stays unchanged. Write 1: Bit is reset to 0.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					HSR_WAKE	HSR_BREAK	HSR_ERROR	HSR_OVERRUN_CHI								HSR_AVAILABLE_CHI								HST_ACCEPTED_CHI							

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Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Reserved	R	0x00
26	HSR_WAKE	Wake detected on Port p	RW	0x0
25	HSR_BREAK	Break detected on Port p	RW	0x0
24	HSR_ERROR	Error on Port p	RW	0x0
23:16	HSR_OVERRUN_CHI	Data overrun in real time mode channel 0..7 (LSB stands for channel 0 and MSB for channel 7)	RW	0x00
15:8	HSR_AVAILABLE_CHI	Data received on channel 0..7 (LSB stands for channel 0 and MSB for channel 7). The status bit shows data on the respective channel when data are in the FIFO. Clearing the status bit has no effect when the FIFO is not empty.	RW	0x00
7:0	HST_ACCEPTED_CHI	Data transmitted on channel 0..7 (LSB stands for channel 0 and MSB for channel 7).	RW	0xFF

Table 23-847. Register Call Summary for Register HSI_Pp_D_IRQr_STATUS

MIPI-HSI

- Interrupt Requests: [0] [1] [2] [3] [4] [5]
- Interrupts: [6]
- HSI Operational Modes Configuration: [7] [8] [9] [10] [11] [12]
- HSI_TOP Register Summary: [13]

Table 23-848. HSI_Pp_D_IRQr_ENABLE

Address Offset	0x0000 0834 + (0x10 * b) + (0x8 * r)	**Index**	p = 1 to 2 r = 0 to 1 b = 0 to 1 (for p = 1, b = 0 and p = 2, b = 1)
Physical Address	0x4A05 8834 + (0x10 * b) + (0x8 * r)	**Instance**	HSI_TOP
Description	IRQ enable register for FIFO (0..7) events and for port p break, wake and error events signaled to DSP line r (Dspirq_r) Write 0: Event is masked. Write 1: Event is enabled.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					HSR_WAKE	HSR_BREAK	HSR_ERROR	HSR_OVERRUN_ENI								HSR_AVAILABLE_ENI								HST_ACCEPTED_ENI							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Reserved	R	0x00
26	HSR_WAKE	Wake interrupt enable for Port p	RW	0x0
25	HSR_BREAK	Break interrupt enable for Port p	RW	0x0
24	HSR_ERROR	Error interrupt enable for Port p	RW	0x0
23:16	HSR_OVERRUN_ ENI	Overrun interrupt enable for channel 0..7 (LSB stands for channel 0 and MSB for channel 7)	RW	0x00
15:8	HSR_AVAILABLE_ ENI	Data available interrupt enable for channel 0..7 (LSB stands for channel 0 and MSB for channel 7)	RW	0x00
7:0	HST_ACCEPTED_ ENI	Data accepted interrupt enable for channel 0..7 (LSB stands for channel 0 and MSB for channel 7).	RW	0x00

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Table 23-849. Register Call Summary for Register HSI_Pp_D_IRQr_ENABLE

MIPI-HSI

- Interrupt Requests: [0] [1] [2] [3] [4] [5]
- Interrupts: [6]
- HSI Operational Modes Configuration: [7] [8] [9] [10] [11] [12]
- HSI_TOP Register Summary: [13]

Table 23-850. HSI_Pp_WAKE

Address Offset	0x0000 0C00 + (0x10 * b)	**Index**	p = 1 to 2 b = 0 to 1 (for p = 1, b = 0 and p = 2, b = 1)
Physical Address	0x4A05 8C00 + (0x10 * b)	**Instance**	HSI_TOP
Description	Programmed wake state for each channel, in port p 0x0: No channel wakeup on WAKE line requested. 0x1: Channel wakeup requested		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																HSI_WAKE_CHI															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x0000
15:0	HSI_WAKE_CHI	Channel 0..15 (LSB stands for channel 0 and MSB for channel 15)	R	0x0000

Table 23-851. Register Call Summary for Register HSI_Pp_WAKE

MIPI-HSI

- HSI Wake Generator: [0]
- Software Management of HSI Wake Generator: [1] [2]
- Automatic Management of HSI Wake Generator: [3]
- HSI_TOP Register Summary: [4]

Table 23-852. HSI_Pp_CLEAR_WAKE

Address Offset	0x0000 0C04 + (0x10 * b)	**Index**	p = 1 to 2 b = 0 to 1 (for p = 1, b = 0 and p = 2, b = 1)
Physical Address	0x4A05 8C04 + (0x10 * b)	**Instance**	HSI_TOP
Description	Clear register for programmed wake state on port p HST_WAKE for each channel 0x0: No effect 0x1: Clears bit		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																HSI_HSI_CLEAR_WAKE_CHI															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x0000
15:0	HSI_CLEAR_WAKE_CHI	Channel 0..15 (LSB stands for channel 0 and MSB for channel 15)	W	0x0000

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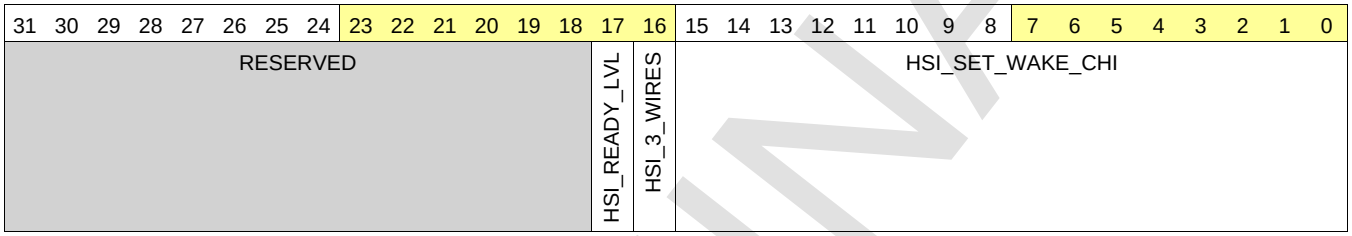
Table 23-853. Register Call Summary for Register HSI_Pp_CLEAR_WAKE

MIPI-HSI

- Software Management of HSI Wake Generator: [0]
- HSI_TOP Register Summary: [1]

Table 23-854. HSI_Pp_SET_WAKE

Address Offset	0x0000 0C08 + (0x10 * b)	**Index**	p = 1 to 2 b = 0 to 1 (for p = 1, b = 0 and p = 2, b = 1)
Physical Address	0x4A05 8C08 + (0x10 * b)	**Instance**	HSI_TOP
Description	Set function for wake state for each channel, in port p 0x0: No effect 0x1: Sets bit		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:18	RESERVED	Reserved	R	0x0000
17	HSI_READY_LVL	READY default level 0x0: READY defaults to 0. 0x1: READY defaults to 1.	RW	0x0
16	HSI_3_WIRES	Sets 3-wire behavior 0x0: Sets 4-wire behavior (wakeup with WAKE signal) 0x1: Sets 3-wire behavior (wakeup on line activity without WAKE signal)	RW	0x0
15:0	HSI_SET_WAKE_CHI	Sets programmed WAKE state for channel i Write 0x0: No effect Write 0x1: Sets bit	W	0x0000

Table 23-855. Register Call Summary for Register HSI_Pp_SET_WAKE

MIPI-HSI

- Software Management of HSI Wake Generator: [0] [1]
- HSI Operational Modes Configuration: [2] [3]
- HSI_TOP Register Summary: [4]

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Table 23-856. DMA_GCR

Address Offset	0x0000 1100		
Physical Address	0x4A05 9100	**Instance**	HSI_TOP
Description	Global Control Register: suspend and clock gating		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												AUTOGATING	RESERVED	SWITCH_OFF	

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved	R	0x0000000
3	AUTOGATING	DMA clock autogating enable 0x0: No DMA clock control 0x1: DMA clock control	RW	0x0
2:1	RESERVED	Reserved	R	0x0
0	SWITCH_OFF	DMA global clock control 0x0: DMA clock released 0x1: DMA clock cutoff	RW	0x0

Table 23-857. Register Call Summary for Register DMA_GCR

MIPI-HSI

- Power Management: [0]
- HSI Module Power-Management Modes: [1] [2]
- Global Initialization: [3]
- HSI Operational Modes Configuration: [4] [5]
- HSI_TOP Register Summary: [6]

Table 23-858. DMA_GRST

Address Offset	0x0000 1200		
Physical Address	0x4A05 9200	**Instance**	HSI_TOP
Description	DMA software reset control register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															SWRESET

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	SWRESET	DMA software reset control bit 0x1: Writing 1 resets the DMA. It is automatically reset to 0 by hardware once software reset is done.	RW	0x0

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Table 23-859. Register Call Summary for Register DMA_GRST

MIPI-HSI

- Software Reset: [0]
- HSI Operational Modes Configuration: [1] [2]
- HSI_TOP Register Summary: [3]

23.10.6.3 HSI_DMA_CHANNELS Registers

23.10.6.3.1 HSI_DMA_CHANNELS Register Summary

Table 23-860 summarizes the mapping of the HSI_DMA_CHANNELS registers.

Table 23-860. HSI_DMA_CHANNELS Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	HSI_DMA_CHANNELS Base Address
DMA_CCR_CSDP_i (1)	RW	32	0x0000 0000 + (0x40 * i)	0x4A05 9800 + (0x40 * i)
DMA_CSR_CCIR_i (1)	RW	32	0x0000 0004 + (0x40 * i)	0x4A05 9804 + (0x40 * i)
DMA_CSSA_i (1)	RW	32	0x0000 0008 + (0x40 * i)	0x4A05 9808 + (0x40 * i)
DMA_CDSA_i (1)	RW	32	0x0000 000C + (0x40 * i)	0x4A05 980C + (0x40 * i)
DMA_CEN_i (1)	RW	32	0x0000 0010 + (0x40 * i)	0x4A05 9810 + (0x40 * i)
DMA_CDAC_CSAC_i (1)	R	32	0x0000 0018 + (0x40 * i)	0x4A05 9818 + (0x40 * i)
Reserved	R	32	0x0000 0028 + (0x40 * i)	0x4A05 9828 + (0x40 * i)

(1) i = 0 to 15

23.10.6.3.2 HSI_DMA_CHANNELS Register Description

Table 23-861 through Table 23-871 describe the HSI_DMA_CHANNELS registers.

Table 23-861. DMA_CCR_CSDP_i

Address Offset	0x0000 0000 + (0x40 * i)	**Index**	i = 0 to 15
Physical Address	0x4A05 9800 + (0x40 * i)	**Instance**	HSI_DMA_CHANNELS
Description	Stores source and destination parameters and channel control bits		
Type	RW		

31 30	29 28	27 26 25 24	23 22 21 20 19 18 17 16	15 14	13	12 11 10 9 8	7 6	5 4 3 2	1 0
DST_ADD_MODE	SRC_ADD_MODE	RESERVED	ENABLE RESERVED	DST_BURST_EN	RESERVED	DST	SRC_BURST_EN	RESERVED	SRC	DATA_TYPE

Bits	Field Name	Description	Type	Reset
31:30	DST_ADD_MODE	Destination addressing mode 0x0: Constant address 0x1: Post-increment address	RW	0x0

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Bits	Field Name	Description	Type	Reset
29:28	SRC_ADD_MODE	Source addressing mode 0x0: Constant address 0x1: Post-increment address	RW	0x0
27:24	RESERVED	Reserved	R	0
23	ENABLE	Logical channel enable 0x0: Transfer stops and is reset. 0x1: Transfer is enabled. Automatically cleared by hardware once transfer is finished.	RW	0
22:16	RESERVED	Reserved	R	0
15:14	DST_BURST_EN	Destination burst enable 0x0: Single access 0x1: Single access 0x3: Burst 8 × 32 bits (not implemented) 0x2: Burst 4 × 32 bits	RW	0x0
13	RESERVED	Reserved	R	0
12:9	DST	Transfer destination 0x8: Transfer to memory port 0x9: Transfer to peripheral port	RW	0x0
8:7	SRC_BURST_EN	Source burst enable 0x0: Single access 0x1: Single access 0x3: Burst 8 × 32 bits (not implemented) 0x2: Burst 4 × 32 bits	RW	0x0
6	RESERVED	Reserved	R	0
5:2	SRC	Transfer source 0x8: Transfer from memory port 0x9: Transfer from peripheral port	RW	0x0
1:0	DATA_TYPE	Defines data types Implemented bit field but not used	RW	0x0

Table 23-862. Register Call Summary for Register DMA_CCR_CSDP_i

MIPI-HSI

- DMA Configuration: [0] [1] [2] [3] [4] [5] [6] [7] [8]
- HSI Operational Modes Configuration: [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21]
- HSI_DMA_CHANNELS Register Summary: [22]

Table 23-863. DMA_CSR_CCIR_i

Address Offset	0x0000 0004 + (0x40 * i)	**Index**	i = 0 to 15
Physical Address	0x4A05 9804 + (0x40 * i)	**Instance**	HSI_DMA_CHANNELS
Description	Interrupt enable and status register Interrupt flag fields will be cleared through read access using the following byte-enable values: 0xC 0xF		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										BLOCK_IS	RESERVED		HALF_IS	RESERVED	TOUT_IS	RESERVED										BLOCK_IE	RESERVED		HALF_IE	RESERVED	TOUT_IE	

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Bits	Field Name	Description	Type	Reset
31:22	RESERVED	Reserved	R	0x000
21	BLOCK_IS	Block transferred Read 0x1: Block transferred Read 0x0: No event	R	0
20:19	RESERVED	Reserved	R	0x0
18	HALF_IS	Half block reached Read 0x1:Half-block transferred Read 0x0: No event	R	0
17	RESERVED	Reserved	R	0
16	TOUT_IS	Time-out overflow event Read 0x1: Time-out occurred Read 0x0: No event	R	0
15:6	RESERVED	Reserved	R	0x000
5	BLOCK_IE	Interrupt is sent when a full block is transferred 0x0: No interrupt 0x1:Interrupt enable	RW	0
4:3	RESERVED	Reserved	R	0x0
2	HALF_IE	Interrupt is sent when a half block is transferred 0x0: No interrupt 0x1: Interrupt enable	RW	0
1	RESERVED	Reserved	R	0
0	TOUT_IE	Interrupt is sent when a time-out overflow occurs 0x0: No interrupt 0x1: Interrupt enable	RW	0

Table 23-864. Register Call Summary for Register DMA_CSR_CCIR_i

MIPI-HSI

- Interrupt Requests: [0] [1] [2] [3] [4] [5]
- Interrupts: [6] [7] [8] [9] [10] [11] [12]
- DMA Configuration: [13]
- HSI Operational Modes Configuration: [14] [15] [16] [17] [18] [19]
- HSI_DMA_CHANNELS Register Summary: [20]

Table 23-865. DMA_CSSA_i

Address Offset	0x0000 0008 + (0x40 * i)	**Index**	i = 0 to 15
Physical Address	0x4A05 9808 + (0x40 * i)	**Instance**	HSI_DMA_CHANNELS
Description	Stores source start address If the transfer configured from memory port, all bits are taken into account as an address. If the transfer configured from peripheral port, the lower 4 bits will determine the FIFO ID.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR																															

Bits	Field Name	Description	Type	Reset
31:0	ADDR	Source start address	RW	0x0000 0000

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Table 23-866. Register Call Summary for Register DMA_CSSA_i

MIPI-HSI

- DMA Configuration: [0]
- HSI Operational Modes Configuration: [1] [2]
- HSI_DMA_CHANNELS Register Summary: [3]

Table 23-867. DMA_CDSA_i

Address Offset	0x0000 000C + (0x40 * i)	**Index**	i = 0 to 15
Physical Address	0x4A05 980C + (0x40 * i)	**Instance**	HSI_DMA_CHANNELS
Description	Stores destination start address If the transfer configured to memory port, all bits are taken into account as an address. If the transfer configured to peripheral port, the lower 4 bits will determine the FIFO ID.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR																															

Bits	Field Name	Description	Type	Reset
31:0	ADDR	Destination start address	RW	0x0000 0000

Table 23-868. Register Call Summary for Register DMA_CDSA_i

MIPI-HSI

- DMA Configuration: [0]
- HSI Operational Modes Configuration: [1] [2]
- HSI_DMA_CHANNELS Register Summary: [3]

Table 23-869. DMA_CEN_i

Address Offset	0x0000 0010 + (0x40 * i)	**Index**	i = 0 to 15
Physical Address	0x4A05 9810 + (0x40 * i)	**Instance**	HSI_DMA_CHANNELS
Description	Stores the number of 4-byte words in a DMA data block. Maximum is 65,536.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																SIZE															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x0000
15:0	SIZE	Number of elements in a block. Maximum is 65,536.	RW	0x0000

Table 23-870. Register Call Summary for Register DMA_CEN_i

MIPI-HSI

- Interrupts: [0]
- DMA Configuration: [1]
- HSI Operational Modes Configuration: [2] [3]
- HSI_DMA_CHANNELS Register Summary: [4]

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Table 23-871. DMA_CDAC_CSAC_i

Address Offset	0x0000 0018 + (0x40 * i)	**Index**	i = 0 to 15
Physical Address	0x4A05 9818 + (0x40 * i)	**Instance**	HSI_DMA_CHANNELS
Description	Monitors the progress of DMA transfer, by storing the 16-bit counter address for source and destination.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDRESS_CDAC																ADDRESS_CSAC															

Bits	Field Name	Description	Type	Reset
31:16	ADDRESS_CDAC	Destination address	R	0x0000
15:0	ADDRESS_CSAC	Source address	R	0x0000

Table 23-872. Register Call Summary for Register DMA_CDAC_CSAC_i

MIPI-HSI

- DMA Configuration: [0] [1]
- HSI_DMA_CHANNELS Register Summary: [2]

23.10.6.4 HSI_PORTS Registers

23.10.6.4.1 HSI_PORTS Register Summary

Table 23-873 summarizes the mapping of the HSI_PORTS registers.

Table 23-873. HSI_PORTS Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	HSI_PORTS Physical Address
HST_ID_Pp [1]	R	32	0x0000 0000 + (0x1000* b)	0x4A05 A000 + (0x1000* b)
HST_MODE_Pp [1]	RW	32	0x0000 0004 + (0x1000* b)	0x4A05 A004 + (0x1000* b)
HST_FRAMESIZE_Pp [1]	R	32	0x0000 0008 + (0x1000* b)	0x4A05 A008 + (0x1000* b)
HST_TXSTATE_Pp [1]	R	32	0x0000 000C + (0x1000* b)	0x4A05 A00C + (0x1000* b)
HST_BUFSTATE_Pp [1]	R	32	0x0000 0010 + (0x1000* b)	0x4A05 A010 + (0x1000* b)
HST_DIVISOR_Pp [1]	RW	32	0x0000 0018 + (0x1000* b)	0x4A05 A018 + (0x1000* b)
HST_BREAK_Pp [1]	W	32	0x0000 0020 + (0x1000* b)	0x4A05 A020 + (0x1000* b)
HST_CHANNELS_Pp [1]	RW	32	0x0000 0024 + (0x1000* b)	0x4A05 A024 + (0x1000* b)
HST_ARBMODE_Pp [1]	RW	32	0x0000 0028 + (0x1000* b)	0x4A05 A028 + (0x1000* b)
HST_BUFFER_Pp_CHN_i [1]	W	32	0x0000 0080 + (0x1000* b) + (0x4 * i)	0x4A05 A080 + (0x1000* b) + (0x4 * i)
HST_SWAPBUFFER_Pp_CHN_i [1]	W	32	0x0000 00C0 + (0x1000* b) + (0x4 * i)	0x4A05 A0C0 + (0x1000* b) + (0x4 * i)
HST_MAPPINGf [1]	RW	32	0x0000 0100 + (0x4 * f)	0x4A05 A100 + (0x4 * f)
RESERVED	RW	32	0x0000 0144	0x4A05 A144

[1] p = 1 to 2
i = 0 to 7
f = 0 to 15
b = 0 to 1 (for p = 1, b = 0 and p = 2, b = 1)

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Table 23-873. HSI_PORTS Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	HSI_PORTS Physical Address
HSR_ID_Pp (1)	R	32	0x0000 0800 + (0x1000* b)	0x4A05 A800 + (0x1000* b)
HSR_MODE_Pp (1)	RW	32	0x0000 0804 + (0x1000* b)	0x4A05 A804 + (0x1000* b)
HSR_FRAMESIZE_Pp (1)	R	32	0x0000 0808 + (0x1000* b)	0x4A05 A808 + (0x1000* b)
HSR_RXSTATE_Pp (1)	R	32	0x0000 080C + (0x1000* b)	0x4A05 A80C + (0x1000* b)
HSR_BUFSTATE_Pp (1)	R	32	0x0000 0810 + (0x1000* b)	0x4A05 A810 + (0x1000* b)
HSR_BREAK_Pp (1)	R	32	0x0000 081C + (0x1000* b)	0x4A05 A81C + (0x1000* b)
HSR_ERROR_Pp (1)	R	32	0x0000 0820 + (0x1000* b)	0x4A05 A820 + (0x1000* b)
HSR_ERRORACK_Pp (1)	W	32	0x0000 0824 + (0x1000* b)	0x4A05 A824 + (0x1000* b)
HSR_CHANNELS_Pp (1)	RW	32	0x0000 0828 + (0x1000* b)	0x4A05 A828 + (0x1000* b)
HSR_OVERRUN_Pp (2)	RW	32	0x0000 082C + (0x1000* b)	0x4A05 A82C + (0x1000* b)
HSR_OVERRUNACK_Pp (2)	R	32	0x0000 0830 + (0x1000* b)	0x4A05 A830 + (0x1000* b)
HSR_COUNTERS_Pp (2)	W	32	0x0000 0834 + (0x1000* b)	0x4A05 A834 + (0x1000* b)
HSR_BUFFER_Pp_CHN_i (2)	R	32	0x0000 0880 + (0x1000* b) + (0x4 * i)	0x4A05 A880 + (0x1000* b) + (0x4 * i)
HSR_SWAPBUFFER_Pp_CHN_i (2)	R	32	0x0000 08C0 + (0x1000* b) + (0x4 * i)	0x4A05 A8C0 + (0x1000* b) + (0x4 * i)
HSR_MAPPINGf (2)	RW	32	0x0000 0900 + (0x4 * f)	0x4A05 A900 + (0x4 * f)
RESERVED	RW	32	0x0000 0944	0x4A05 A944
RESERVED	RW	32	0x0000 0948	0x4A05 A948
HSR_DIVISOR_Pp (2)	RW	32	0x0000 094C + (0x1000* b)	0x4A05 A94C + (0x1000* b)

(2) p = 1 to 2
i = 0 to 7
f = 0 to 15
b = 0 to 1 (for p = 1, b = 0 and p = 2, b = 1)

23.10.6.4.2 HSI_PORTS Register Description

Table 23-874 through Table 23-928 describe the HSI_PORTS registers.

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Table 23-874. HST_ID_Pp

Address Offset	0x0000 0000 + (0x1000* b)		p = 1 to 2 b = 0 to 1 (for p = 1, b = 0 and p = 2, b = 1)
Physical Address	0x4A05 A000 + (0x1000* b)	**Instance**	HSI_PORTS
Description	Legacy identification on port p		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID_VAL																															

Bits	Field Name	Description	Type	Reset
31:0	ID_VAL	Legacy ID	R	See (1).

(1) TI Internal Data

Table 23-875. Register Call Summary for Register HST_ID_Pp

MIPI-HSI

- HSI_PORTS Register Summary: [0]

Table 23-876. HST_MODE_Pp

Address Offset	0x0000 0004 + (0x1000* b)		p = 1 to 2 b = 0 to 1 (for p = 1, b = 0 and p = 2, b = 1)
Physical Address	0x4A05 A004 + (0x1000* b)	**Instance**	HSI_PORTS
Description	Defines operation mode and data flow on port p		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																											WAKE_CTRL	FLOW_VAL		MODE_VAL	

Bits	Field Name	Description	Type	Reset
31:5	RESERVED	Reserved	R	0x0000000
4	WAKE_CTRL	Wake control 0x0: Software control 0x1: Automatic control	RW	0
3:2	FLOW_VAL	Flow 0x0: Synchronized 0x1: Pipelined 0x2: Real-time	RW	0x0
1:0	MODE_VAL	Mode 0x0: Sleep 0x1: Stream 0x2: Frame 0x3: Reserved	RW	0x0

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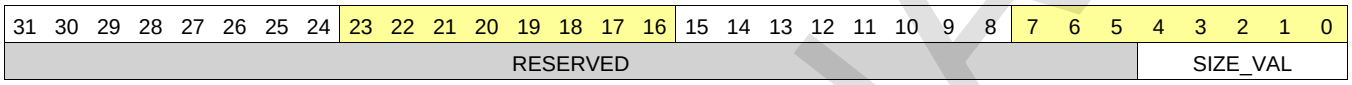
Table 23-877. Register Call Summary for Register HST_MODE_Pp

MIPI-HSI

- Configuration: [0] [1] [2] [3]
- HSI Operational Modes Configuration: [4] [5] [6] [7] [8]
- HSI_PORTS Register Summary: [9]

Table 23-878. HST_FRAMESIZE_Pp

Address Offset	0x0000 0008 + (0x1000* b)	**Index**	p = 1 to 2 b = 0 to 1 (for p = 1, b = 0 and p = 2, b = 1)
Physical Address	0x4A05 A008 + (0x1000* b)	**Instance**	HSI_PORTS
Description	This register is provided for legacy and possible future extension of protocol. Returns 0x1f.		
Type	R		



Bits	Field Name	Description	Type	Reset
31:5	RESERVED	Reserved	R	0x0000000
4:0	SIZE_VAL	In the current implementation it must be always written 31, meaning the frame payload size is 32 bits. Read 0x1F: Only possible value	R	0x1F

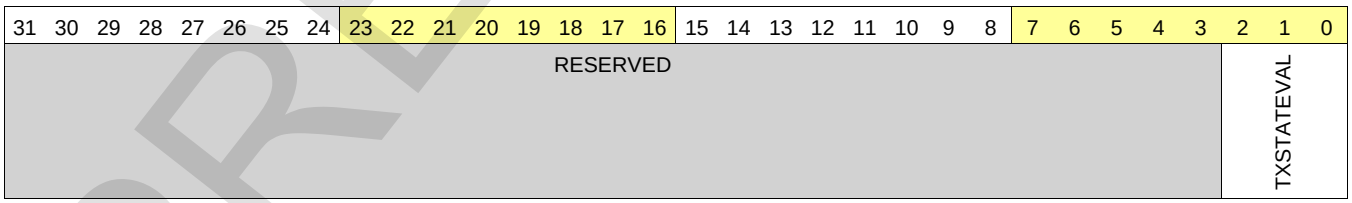
Table 23-879. Register Call Summary for Register HST_FRAMESIZE_Pp

MIPI-HSI

- Configuration: [0]
- HSI_PORTS Register Summary: [1]

Table 23-880. HST_TXSTATE_Pp

Address Offset	0x0000 000C + (0x1000* b)	**Index**	p = 1 to 2 b = 0 to 1 (for p = 1, b = 0 and p = 2, b = 1)
Physical Address	0x4A05 A00C + (0x1000* b)	**Instance**	HSI_PORTS
Description	Define the state of the transmitter on port p.		
Type	R		



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Bits	Field Name	Description	Type	Reset
31:3	RESERVED	Reserved	R	0x0000 0000
2:0	TXSTATEVAL	State of the transmitter Read 0x0: Idle Read 0x1: Wait Read 0x2: Transmit Read 0x3: Start Read 0x4: Break Read 0x5: Reserved Read 0x6: Reserved Read 0x7: Reserved	R	0x0

Table 23-881. Register Call Summary for Register HST_TXSTATE_Pp

MIPI-HSI
- Transmission Operations: [0]
- HSI_PORTS Register Summary: [1]

Table 23-882. HST_BUFSTATE_Pp

Address Offset	0x0000 0010 + (0x1000* b)	**Index**	p = 1 to 2 b = 0 to 1 (for p = 1, b = 0 and p = 2, b = 1)
Physical Address	0x4A05 A010 + (0x1000* b)	**Instance**	HSI_PORTS
Description	Transmitter state for FIFO 0..7 Each bit gives the state of transmit FIFOs: 0x1: FIFO full 0x0: FIFO not full		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								BUFSTATE_VAL							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Reserved	R	0x000000
7:0	BUFSTATE_VAL	Each bit gives the state of transmit buffer register: 0x0: Buffer is not full. 0x1: Buffer is full.	R	0x00

Table 23-883. Register Call Summary for Register HST_BUFSTATE_Pp

MIPI-HSI
- Transmission Buffer: [0] [1]
- Transmission Operations: [2]
- HSI Operational Modes Configuration: [3]
- HSI_PORTS Register Summary: [4]

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Table 23-884. HST_DIVISOR_Pp

Address Offset	0x0000 0018 + (0x1000* b)	**Index**	p = 1 to 2 b = 0 to 1 (for p = 1, b = 0 and p = 2, b = 1)
Physical Address	0x4A05 A018 + (0x1000* b)	**Instance**	HSI_PORTS
Description	Transmission bit rate divisor for port p		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								TX_RATE_DIV_VAL							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Reserved	R	0x000000
7:0	TX_RATE_DIV_VAL	This bit field B has a range [0..255] and it programs a division factor [1..256], B + 1. Example: Writing 0 divides by 1, writing 1 divides by 2, writing 2 divides by 3, etc.	RW	0x00

Table 23-885. Register Call Summary for Register HST_DIVISOR_Pp

MIPI-HSI

- Functional Clock Domain: [0]
- Configuration: [1]
- Global Initialization: [2]
- HSI Operational Modes Configuration: [3]
- HSI_PORTS Register Summary: [4]

Table 23-886. HST_BREAK_Pp

Address Offset	0x0000 0020 + (0x1000* b)	**Index**	p = 1 to 2 b = 0 to 1 (for p = 1, b = 0 and p = 2, b = 1)
Physical Address	0x4A05 A020 + (0x1000* b)	**Instance**	HSI_PORTS
Description	Transmit break strobe register on port p		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															BREAK_VAL

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	W	0x0000 0000
0	BREAK_VAL	Send a break signal on the port Write 0x0: No break Write 0x1: Transmit break	W	0x0

Table 23-887. Register Call Summary for Register HST_BREAK_Pp

MIPI-HSI

- Break Pattern Transmission: [0] [1] [2]
- HSI Operational Modes Configuration: [3]
- HSI_PORTS Register Summary: [4]

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Table 23-888. HST_CHANNELS_Pp

Address Offset	0x0000 0024 + (0x1000* b)	**Index**	p = 1 to 2 b = 0 to 1 (for p = 1, b = 0 and p = 2, b = 1)
Physical Address	0x4A05 A024 + (0x1000* b)	**Instance**	HSI_PORTS
Description	Number of active channels on port p (this determines the number of the used channel descriptor bits on the MIPI port as well) It can be 1, 2, 4, 8, or 16.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								CHAN_NUM_VAL							

Bits	Field Name	Description	Type	Reset
31:5	RESERVED	Reserved	R	0x0000000
4:0	CHAN_NUM_VAL	Number of active channels up to 16 0x1: One logical channel used, number of the channel descriptor bits is 0. 0x2: Two logical channels used, number of the channel descriptor bits is 1. 0x4: Four logical channels used, number of the channel descriptor bits is 2. 0x8: Eight logical channels used, number of the channel descriptor bits is 3. 0x10: Sixteen logical channels used, number of the channel descriptor bits is 4.	RW	0x01

Table 23-889. Register Call Summary for Register HST_CHANNELS_Pp

MIPI-HSI

- Configuration: [0]
- HSI Operational Modes Configuration: [1]
- HSI_PORTS Register Summary: [2]

Table 23-890. HST_ARBMODE_Pp

Address Offset	0x0000 0028 + (0x1000* b)	**Index**	p = 1 to 2 b = 0 to 1 (for p = 1, b = 0 and p = 2, b = 1)
Physical Address	0x4A05 A028 + (0x1000* b)	**Instance**	HSI_PORTS
Description	Arbitration type for the transmit FIFOs on port p.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															ARB_VAL

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	ARB_VAL	Mode 0x0: Round robin 0x1: Priority	RW	0

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Table 23-891. Register Call Summary for Register HST_ARBMODE_Pp

MIPI-HSI

- Configuration: [0]
- Mapping: [1] [2]
- HSI Operational Modes Configuration: [3]
- HSI_PORTS Register Summary: [4]

Table 23-892. HST_BUFFER_Pp_CHN_i

Address Offset	0x0000 0080 + (0x1000* b) + (0x4 * i)	**Index**	p = 1 to 2 i = 0 to 7 b = 0 to 1 (for p = 1, b = 0 and p = 2, b = 1)
Physical Address	0x4A05 A080 + (0x1000* b) + (0x4 * i)	**Instance**	HSI_PORTS
Description	Transmit register for FIFO 0..7 Important: Write access to the register with 0xC and 0xF byteen loads its value into the transmit FIFO. If using only 16- bit accesses, the lower 2 bytes must be written first (byteen 0x3). Between two consecutive 16-bit FIFO-related access there cannot be any other FIFO-related OCP access.		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															

Bits	Field Name	Description	Type	Reset
31:0	DATA	32 bits of data	W	0x0000 0000

Table 23-893. Register Call Summary for Register HST_BUFFER_Pp_CHN_i

MIPI-HSI

- DMA Basic Operation Outline: [0]
- Transmission Buffer: [1] [2]
- Transmission Operations: [3] [4] [5]
- Transmission Exceptions: [6]
- Transmit FIFO Architecture: [7] [8]
- FIFO Addressing: [9]
- HSI Operational Modes Configuration: [10] [11]
- HSI_PORTS Register Summary: [12]

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Table 23-894. HST_SWAPBUFFER_Pp_CHN_i

Address Offset	0x0000 00C0 + (0x1000* b) + (0x4 * i)	**Index**	p = 1 to 2 i = 0 to 7 b = 0 to 1 (for p = 1, b = 0 and p = 2, b = 1)
Physical Address	0x4A05 A0C0 + (0x1000* b) + (0x4 * i)	**Instance**	HSI_PORTS
Description	Transmit register with byte swapping for FIFO 0..7 Important: Write access to the register with 0x3 and 0xF byteen loads its value into the transmit FIFO. If using only 16-bit accesses, the upper 2 bytes must be written first (byteen 0xC). Between two consecutive 16-bit FIFO-related access there cannot be any other FIFO-related OCP access.		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SWAPDATA																															

Bits	Field Name	Description	Type	Reset
31:0	SWAPDATA	32 bits of byte-swapped data	W	0x0000 0000

Table 23-895. Register Call Summary for Register HST_SWAPBUFFER_Pp_CHN_i

MIPI-HSI

- Transmission Buffer: [0]
- FIFO Addressing: [1]
- HSI_PORTS Register Summary: [2]

Table 23-896. HST_MAPPINGf

Address Offset	0x0000 0100 + (0x4 * f)	**Index**	f = 0 to 15
Physical Address	0x4A05 A100 + (0x4 * f)	**Instance**	HSI_PORTS
Description	TX FIFO configuration register. One register per FIFO.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																		THRESHOLD				RESERVED		PORT_NUMBER	RESERVED			CH_NUMBER			ENABLE

Bits	Field Name	Description	Type	Reset
31:14	RESERVED	Reserved	R	0x00000
13:10	THRESHOLD	Number of empty TX FIFO locations that will activate interrupt or DMA requests.	RW	0x0
		DMA requests (if enabled) or interrupt assertion (if enabled) is triggered if the number of free locations in FIFO is less than the THRESHOLD value. 0x0: Less than 8 words in the FIFO 0x1: Less than 1 words in the FIFO 0x2: Less than 2 words in the FIFO … 0x8: Less than 8 words in the FIFO		

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Bits	Field Name	Description	Type	Reset
		0x9 through 0xF: No request generated		
9:8	RESERVED	Reserved	R	0x0
7	PORT_NUMBER	Associates the FIFO to a HSI port 0x0: Port 1 0x1: Port 2	RW	0
6:5	RESERVED	Reserved	R	0x0
4:1	CH_NUMBER	Associates the TX FIFO to a HSI logical channel number (0-15): 0x0: Logical channel number 0 0x1: Logical channel number 1 … 0xF: Logical channel number 15	RW	0x0
0	ENABLE	Enables the FIFO 0x0: Disabled 0x1: Enabled	RW	1

Table 23-897. Register Call Summary for Register HST_MAPPINGf

MIPI-HSI

- DMA Basic Operation Outline: [0]
- Configuration: [1] [2] [3] [4] [5]
- Mapping: [6] [7]
- FIFO Subsystem Architecture: [8]
- Transmit FIFO Architecture: [9] [10]
- HSI Operational Modes Configuration: [11] [12] [13] [14]
- HSI_PORTS Register Summary: [15]

Table 23-898. HSR_ID_Pp

Address Offset	0x0000 0800 + (0x1000* b)	**Index**	p = 1 to 2 b = 0 to 1 (for p = 1, b = 0 and p = 2, b = 1)
Physical Address	0x4A05 A800 + (0x1000* b)	**Instance**	HSI_PORTS
Description	Legacy identification		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID_VAL																															

Bits	Field Name	Description	Type	Reset
31:0	ID_VAL	Legacy ID	R	See (1)

(1) TI Internal Data

Table 23-899. Register Call Summary for Register HSR_ID_Pp

MIPI-HSI

- HSI_PORTS Register Summary: [0]

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Table 23-900. HSR_MODE_Pp

Address Offset	0x0000 0804 + (0x1000* b)		p = 1 to 2 b = 0 to 1 (for p = 1, b = 0 and p = 2, b = 1)
Physical Address	0x4A05 A804 + (0x1000* b)	**Instance**	HSI_PORTS
Description	Defines operation mode and data flow on port p		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																											WAKE_STATUS	FLOW_VAL		MODE_VAL	

Bits	Field Name	Description	Type	Reset
31:5	RESERVED	Reserved	R	0x0000000
4	WAKE_STATUS	Level of WAKE line	R	-
3:2	FLOW_VAL	Flow 0x0: Synchronized 0x1: Pipelined 0x2: Real-time	RW	0x0
1:0	MODE_VAL	Mode 0x0: Sleep 0x1: Stream(1) 0x2: Frame(1) 0x3: Reserved	RW	0x0

(1) Selecting stream or frame mode activates the READY line and causes the start of communication. The mode must be set at the end of the module configuration, just before the start.

Table 23-901. Register Call Summary for Register HSR_MODE_Pp

MIPI-HSI

- Receive Operations: [0]
- Configuration: [1]
- HSI Operational Modes Configuration: [2] [3]
- HSI_PORTS Register Summary: [4]

Table 23-902. HSR_FRAMESIZE_Pp

Address Offset	0x0000 0808 + (0x1000* b)		p = 1 to 2 b = 0 to 1 (for p = 1, b = 0 and p = 2, b = 1)
Physical Address	0x4A05 A808 + (0x1000* b)	**Instance**	HSI_PORTS
Description	Legacy returns 0x1f		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																											SIZE_VAL					

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Bits	Field Name	Description	Type	Reset
31:5	RESERVED	Reserved	R	0x0000000
4:0	SIZE_VAL	0x1F	R	0x1F

Table 23-903. Register Call Summary for Register HSR_FRAMESIZE_Pp

MIPI-HSI
- HSI_PORTS Register Summary: [0]

Table 23-904. HSR_RXSTATE_Pp

Address Offset	0x0000 080C + (0x1000* b)	**Index**	p = 1 to 2 b = 0 to 1 (for p = 1, b = 0 and p = 2, b = 1)
Physical Address	0x4A05 A80C + (0x1000* b)	**Instance**	HSI_PORTS
Description	Receiver state on port p		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														RXSTATEVAL	

Bits	Field Name	Description	Type	Reset
31:3	RESERVED	Reserved	R	0x0000 0000
2:0	RXSTATEVAL	RX state Read 0x0: Idle Read 0x1: Receiving Read 0x2: Finished Read 0x3: Error Read 0x4: Halt Read 0x5: Time-out	R	0x0

Table 23-905. Register Call Summary for Register HSR_RXSTATE_Pp

MIPI-HSI
- Receive Operations: [0] [1]
- HSI_PORTS Register Summary: [2]

Table 23-906. HSR_BUFSTATE_Pp

Address Offset	0x0000 0810 + (0x1000* b)	**Index**	p = 1 to 2 b = 0 to 1 (for p = 1, b = 0 and p = 2, b = 1)
Physical Address	0x4A05 A810 + (0x1000* b)	**Instance**	HSI_PORTS
Description	State of receiver buffer register for port p		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								BUFSTATE_VAL							

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Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Reserved	R	0x000000
7:0	BUFSTATE_VAL	Each bit gives the state of receiver buffer register: 0x0: Buffer is not full. 0x1: Buffer is full.	R	0x00

Table 23-907. Register Call Summary for Register HSR_BUFSTATE_Pp

MIPI-HSI

- Receive Buffers: [0] [1] [2] [3]
- HSI Operational Modes Configuration: [4]
- HSI_PORTS Register Summary: [5]

Table 23-908. HSR_BREAK_Pp

Address Offset	0x0000 081C + (0x1000* b)	**Index**	p = 1 to 2 b = 0 to 1 (for p = 1, b = 0 and p = 2, b = 1)
Physical Address	0x4A05 A81C + (0x1000* b)	**Instance**	HSI_PORTS
Description	Break detected on port p		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															BREAK_VAL

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	BREAK_VAL	Break detected Read 0x0: No break detected Read 0x1: Break detected	R	0

Table 23-909. Register Call Summary for Register HSR_BREAK_Pp

MIPI-HSI

- Interrupts: [0]
- Receive Exceptions: [1]
- HSI_PORTS Register Summary: [2]

Table 23-910. HSR_ERROR_Pp

Address Offset	0x0000 0820 + (0x1000* b)	**Index**	p = 1 to 2 b = 0 to 1 (for p = 1, b = 0 and p = 2, b = 1)
Physical Address	0x4A05 A820 + (0x1000* b)	**Instance**	HSI_PORTS
Description	Error detection state register for port p		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED		RESERVED		TME		RESERVED		RME		RESERVED		TBE		RESERVED		FTE	SIG

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Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x0000
15	RESERVED	Reserved	R	0x0
14:12	RESERVED	Reserved	R	0x0
11	TME	TX mapping error	R	0x0
10:8	RESERVED	Reserved	R	0x0
7	RME	RX mapping error	R	0x0
6:5	RESERVED	Reserved	R	0x0
4	TBE	Tailing bit error	R	0x0
3:2	RESERVED	Reserved	R	0x0
1	FTE	Frame time-out error	R	0x0
0	SIG	Signal error (legacy)	R	0x0

Table 23-911. Register Call Summary for Register HSR_ERROR_Pp

MIPI-HSI

- Detection of Errors: [0]
- Error Counters: [1] [2] [3]
- Error Registers: [4] [5] [6] [7] [8]
- HSI Operational Modes Configuration: [9] [10] [11] [12] [13]
- HSI_PORTS Register Summary: [14]

Table 23-912. HSR_ERRORACK_Pp

Address Offset	0x0000 0824 + (0x1000* b)		p = 1 to 2 b = 0 to 1 (for p = 1, b = 0 and p = 2, b = 1)
Physical Address	0x4A05 A824 + (0x1000* b)	**Instance**	HSI_PORTS
Description	Error detection acknowledge register on port p: write 1 to clear.		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED		RESERVED		TME		RESERVED		RME		RESERVED		TBE		RESERVED		FTE	SIG

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	W	0x0000
15	RESERVED	Reserved	W	0x0
14:12	RESERVED	Reserved	W	0x0
11	TME	TX mapping error	W	0x0
10:8	RESERVED	Reserved	W	0x0
7	RME	RX mapping error	W	0x0
6:5	RESERVED	Reserved	W	0x0
4	TBE	Tailing bit error	W	0x0
3:2	RESERVED	Reserved	W	0x0
1	FTE	Frame time-out error	W	0x0
0	SIG	Signal error (legacy)	W	0x0

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Table 23-913. Register Call Summary for Register HSR_ERRORACK_Pp

MIPI-HSI

- Receive Exceptions: [0]
- Error Registers: [1]
- HSI Operational Modes Configuration: [2] [3] [4] [5] [6]
- HSI_PORTS Register Summary: [7]

Table 23-914. HSR_CHANNELS_Pp

Address Offset	0x0000 0828 + (0x1000* b)		p = 1 to 2 b = 0 to 1 (for p = 1, b = 0 and p = 2, b = 1)
Physical Address	0x4A05 A828 + (0x1000* b)	**Instance**	HSI_PORTS
Description	Number of active channels on port p (this determines the number of the used channel descriptor bits on the MIPI port as well) It can be 1, 2, 4, 8, or 16.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														CHAN_NUM_VAL	

Bits	Field Name	Description	Type	Reset
31:5	RESERVED	Reserved	R	0x0000000
4:0	CHAN_NUM_VAL	Number of active channels 0x1: One logical channel used, number of the channel descriptor bits is 0 0x2: Two logical channels used, number of the channel descriptor bits is 1 0x4: Four logical channels used, number of the channel descriptor bits is 2 0x8: Eight logical channels used, number of the channel descriptor bits is 3 0x10: Sixteen logical channels used, number of the channel descriptor bits is 4	RW	0x01

Table 23-915. Register Call Summary for Register HSR_CHANNELS_Pp

MIPI-HSI

- HSI Operational Modes Configuration: [0]
- HSI_PORTS Register Summary: [1]

Table 23-916. HSR_OVERRUN_Pp

Address Offset	0x0000 082C + (0x1000* b)		p = 1 to 2 b = 0 to 1 (for p = 1, b = 0 and p = 2, b = 1)
Physical Address	0x4A05 A82C + (0x1000* b)	**Instance**	HSI_PORTS
Description	Overrun detection state register for those receive FIFOs that are mapped to port p		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																OVERRUN_VAL															

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Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x0000
15:0	OVERRUN_VAL	Bit n is set when overrun is detected on channel n Read 0x1: Overrun detected Read 0x0: No overrun	R	0x0000

Table 23-917. Register Call Summary for Register HSR_OVERRUN_Pp

MIPI-HSI
- Receive Exceptions: [0]
- HSI_PORTS Register Summary: [1]

Table 23-918. HSR_OVERRUNACK_Pp

Address Offset	0x0000 0830 + (0x1000* b)		p = 1 to 2 b = 0 to 1 (for p = 1, b = 0 and p = 2, b = 1)
Physical Address	0x4A05 A830 + (0x1000* b)	**Instance**	HSI_PORTS
Description	Overrun acknowledge register for those receive FIFOs that are mapped to port p		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																OVERRUNACK_VAL															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x0000
15:0	OVERRUNACK_VAL	Bit n is set when overrun is acknowledged on channel n. Write 0x0: No action Write 0x1: Overrun acknowledge	W	0x0000

Table 23-919. Register Call Summary for Register HSR_OVERRUNACK_Pp

MIPI-HSI
- HSI_PORTS Register Summary: [0]

Table 23-920. HSR_COUNTERS_Pp

Address Offset	0x0000 0834 + (0x1000* b)		p = 1 to 2 b = 0 to 1 (for p = 1, b = 0 and p = 2, b = 1)
Physical Address	0x4A05 A834 + (0x1000* b)	**Instance**	HSI_PORTS
Description	Counters setting register for port p		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FB								TB				FT																			

Bits	Field Name	Description	Type	Reset
31:24	FB	Setting for Frame Burst Counter. Setting n as a value results in n + 1 counter value.	RW	0x00
23:20	TB	Setting for Tailing Bit Counter. Setting n as a value results in n + 1 counter value.	RW	0x0
19:0	FT	Setting for Frame Time-out counter. Set n as a value results in n+1 counter value.	RW	0x00000

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Table 23-921. Register Call Summary for Register HSR_COUNTERS_Pp

MIPI-HSI
- Receive Operations: [0]
- HSI Operational Modes Configuration: [1] [2] [3]
- HSI_PORTS Register Summary: [4]

Table 23-922. HSR_BUFFER_Pp_CHN_i

Address Offset	0x0000 0880 + (0x1000* b) + (0x4 * i)	**Index**	p = 1 to 2 i = 0 to 7 b = 0 to 1 (for p = 1, b = 0 and p = 2, b = 1)
Physical Address	0x4A05 A880 + (0x1000* b) + (0x4 * i)	**Instance**	HSI_PORTS
Description	Receive register for receive FIFO 0..7 Important: Read access to the register with 0xC and 0xF byteen removes the receive FIFO-related item. If using only 16-bit accesses, the lower 2 bytes must be read first (byteen 0x3). Between two consecutive 16-bit FIFO-related access there cannot be any other FIFO-related OCP access.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															

Bits	Field Name	Description	Type	Reset
31:0	DATA	Received data	R	0x--------

Table 23-923. Register Call Summary for Register HSR_BUFFER_Pp_CHN_i

MIPI-HSI
- DMA Basic Operation Outline: [0]
- Receive Buffers: [1] [2] [3] [4] [5]
- Receive FIFO Architecture: [6] [7]
- FIFO Addressing: [8]
- HSI Operational Modes Configuration: [9] [10]
- HSI_PORTS Register Summary: [11]

Table 23-924. HSR_SWAPBUFFER_Pp_CHN_i

Address Offset	0x0000 08C0 + (0x1000* b) + (0x4 * i)	**Index**	p = 1 to 2 i = 0 to 7 b = 0 to 1 (for p = 1, b = 0 and p = 2, b = 1)
Physical Address	0x4A05 A8C0 + (0x1000* b) + (0x4 * i)	**Instance**	HSI_PORTS
Description	Byte swapped receive register for receive FIFO 0..7 Important: Read access to the register with 0x3 and 0xF byteen removes the receive FIFO-related item. If using only 16-bit accesses, the upper 2 bytes must be read first (byteen 0xC). Between two consecutive 16-bit FIFO-related access there cannot be any other FIFO- related OCP access.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SWAPDATA																															

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Bits	Field Name	Description	Type	Reset
31:0	SWAPDATA	Received data swapped	R	0x--------

Table 23-925. Register Call Summary for Register HSR_SWAPBUFFER_Pp_CHN_i

MIPI-HSI
- Receive Buffers: [0] [1]
- FIFO Addressing: [2]
- HSI_PORTS Register Summary: [3]

Table 23-926. HSR_MAPPINGf

Address Offset	0x0000 0900 + (0x4 * f)	**Index**	f = 0 to 15
Physical Address	0x4A05 A900 + (0x4 * f)	**Instance**	HSI_PORTS
Description	RX FIFO Configuration register. One register per FIFO.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																WORDS						RESERVED		PORT_NUMBER	RESERVED			CH_NUMBER			ENABLE

Bits	Field Name	Description	Type	Reset
31:14	RESERVED	Reserved	R	0x00000
13:10	WORDS	Number of words available in the RX FIFO for reading	R	0x0
9:8	RESERVED	Reserved	R	0x0
7	PORT_NUMBER	Associates the RX FIFO to a HSI port 0x0: Port 1 0x1: Port 2	RW	0x0
6:5	RESERVED	Reserved	R	0x0
4:1	CH_NUMBER	Associates RX FIFO to a HSI logical channel 0x0: Logical channel number 0 0x1: Logical channel number 1 … 0xF: Logical channel number 15	RW	0x0
0	ENABLE	Enables or disables RX FIFO 0x0: Disabled 0x1: Enabled	RW	0x1

Table 23-927. Register Call Summary for Register HSR_MAPPINGf

MIPI-HSI
- DMA Basic Operation Outline: [0]
- Configuration: [1]
- FIFO Subsystem Architecture: [2]
- Receive FIFO Architecture: [3]
- HSI Operational Modes Configuration: [4] [5] [6] [7] [8]
- HSI_PORTS Register Summary: [9]

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Table 23-928. HSR_DIVISOR_Pp

Address Offset	0x0000 094C + (0x1000* b)	**Index**	p = 1 to 2 b = 0 to 1 (for p = 1, b = 0 and p = 2, b = 1)
Physical Address	0x4A05 A94C + (0x1000* b)	**Instance**	HSI_PORTS
Description	Receive bit rate divisor for port p. This must be set for correct protocol timing detection (tailing time-out, frame time-out).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RX_RATE_DIV_VAL							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Reserved	R	0x000000
7:0	RX_RATE_DIV_VAL	The functional clock source divided by this value is used as a clock base for the receive counters. Setting n as a value results in the n + 1 divisor value.	RW	0x00

Table 23-929. Register Call Summary for Register HSR_DIVISOR_Pp

MIPI-HSI

- Functional Clock Domain: [0]
- Error Counters: [1]
- HSI Operational Modes Configuration: [2]
- HSI_PORTS Register Summary: [3]

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23.11 High-Speed Multiport USB Host Subsystem

This section describes the HS universal serial bus (USB) host subsystem of the device.

23.11.1 High-Speed Multiport USB Host Subsystem Overview

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The HS USB host subsystem consists of several ports and several modes per port. The modes are:

- UTMI+ low pin interface (ULPI)
- ULPI transceiverless link (TLL)
- High-speed interchip (HSIC)
- Serial
- Serial TLL

The HS USB host subsystem is composed of:

- HS multiport USB host controller module
- USBTLL module
- Two HSIC digital front end (DFE) modules

The HS USB host controller contains two quasi-independent host controllers that operate in parallel:

- The EHCI controller, based on the *Enhanced Host Controller Interface (EHCI) Specification for USB Release 1.1*, is responsible for HS traffic (480 Mbps), over ULPI/USB 2.0 transceiver macrocell interface (UTMI).
- The OHCI controller, based on the *Open Host Controller Interface (OHCI Specification for USB Release 1.0a*, is responsible for full-speed (FS)/low-speed (LS) traffic (12/1.5 Mbps, respectively), over a serial interface.

Each of the two external ports of the HS USB host controller is owned by one of the controllers (EHCI or OHCI) at a given time. Each port can work in several modes:

- When the port is owned by the OHCI (FS) host, the 6-pin internal serial interface is used.
- When the port is owned by the EHCI (HS) host, ULPI or UTMI is used.

The current subsystem does not support all dynamic USB speed negotiations, as expected from a standard USB host port at the same time. It supports:

- HS-only (with external HS physical layer [PHY]/HS TLL mode HSIC) on the EHCI
- FS-/LS-only (with external FS PHY/FS TLL mode) on the OHCI

If an FS peripheral is connected to an HS port (to an HS ULPI PHY), the HS host subsystem negotiates for FS but cannot transfer control to the FS/LS host controller – the PHY interface is not available.

The USBTLL module is the adapter on the host ports. It consists of two channels that are seen as emulating a pair of back-to-back PHYs and has:

- UTMI port, connected to the host
- ULPI port, connected to a ULPI peripheral

The two HSIC DFEs plug into the UTMI port of the host and control HSIC-capable bidirectional I/O drivers driving the HSIC lines (strobe/data).

Figure 23-232 shows the HS USB host subsystem.

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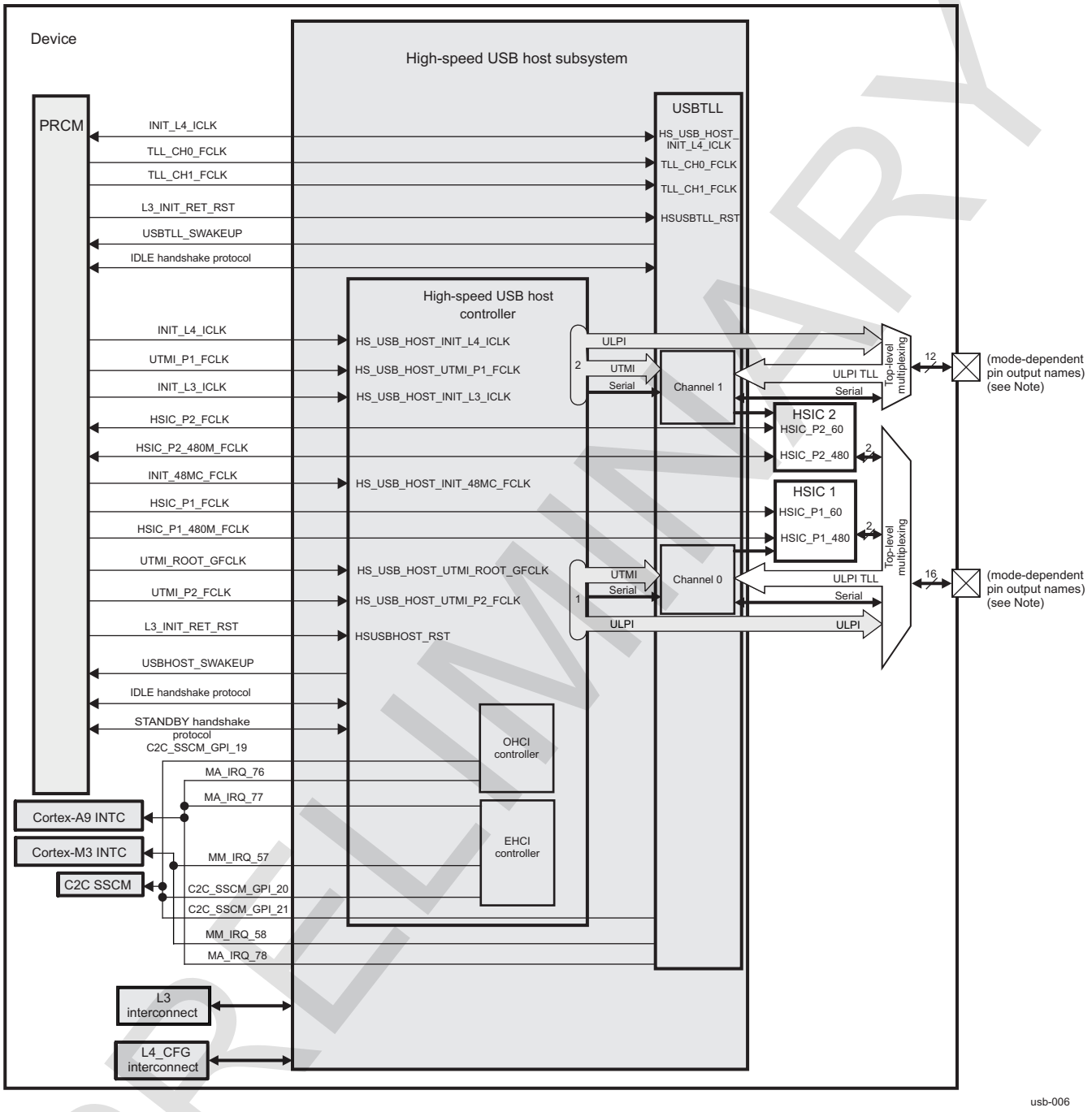
Figure 23-232. HS USB Host Controller



NOTE: For more information about output pin names in different modes, see Section 23.11.2.1, *ULPIs*; Section 23.11.2.2, *FS/LS Serial Interfaces*; and Section 23.11.2.3, *HSIC Interface*.

23.11.1.1 Main Features

The HS multiport USB host subsystem supports the following features:

- HS USB host controller:
  - One initiator on level 3 (L3)
  - One target on level 4 (L4)
  - Two IRQs

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- No DMA request
- Implements a USB 2.0 HS host controller:
  - HS (480 Mbps) communication with HS USB peripherals or hubs
  - FS (12 Mbps) communication with FS USB peripherals or hubs
  - LS (1.5 Mbps) communication with LS USB peripherals
- Support for suspend, resume, remote wakeup
- Two downstream ports (2-port root hub, with each port supporting UTMI, ULPI, and serial interface)
- Heterogeneous port configuration (that is, different HS/FS PHYs with different clocking methods on different ports, supported simultaneously)
- Single FS host controller, compliant with OHCI software application programming interface (API), per-port power switching support
- Interface with UTMI PHYs (transceivers) on all ports
  - 8-bit data path
  - Synchronous (on-chip) interface, independent clock input per port
  - HSIC front-end (after appropriate internal configuration)
- Interface with ULPI PHYs (transceivers) on all ports
  - 8-bit bidirectional data bus (SDR mode)
  - 12-pin interface
  - Independent clock input per port (from ULPI PHY)
  - Supports only HS data transactions

CAUTION

The HS USB host subsystem can support only the external charge pump of PHY (no support of internal charge pump for ULPI PHY).

- Interconnect initiator for built-in DMA operation of EHCI/OHCI
- Interconnect target for configuration
- Link power management (LPM) support in OHCI and EHCI hosts
- Hardware save-and-restore (SAR) feature of the hardware context of the suspended host

- USBTLL module:
  - One interconnect target on L4
  - One IRQ
  - No DMA request
  - HS USB ports and each of them has four ports (A to D):
    - Port A: Host module UTMI+ port. Connects to the local link controller (host module). The UTMI "local" port is used in all configurations (that is, the entire channel can be seen as a protocol converted from that port to one of the other, "remote" ports. The port complies with UTMI+ version 1.0 and supports:
      - 8-data-bit, UTMI (HS/FS-capable)
      - UTMI+ L3 extensions
      - Vcontrol/Vstatus (from UTMI)
      - Serial FS 6-pin mode
    - Port B: Link-side UTMI+ port. Connects to HSIC front-end module.
    - Port C: PHY-side ULPI slave port. Connects to a remote (off-chip) ULPI link controller through I/O pads.
      - SDR ULPI mode (8-bit data width)
      - Supports optional input clocking mode

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- Port D: Serial multimode port.
  - Supports 6-pin unidirectional and 4-/3-/2-pin bidirectional modes
  - All modes are supported for TLL or PHY interface configuration, except 2-pin mode (that is, TLL-only).
  - Supports sideband signals (pullup/down control, speed/suspend enable, etc.)
- HSIC module: Converts UTMI into HSIC standard (2-wire TLL HS protocol)

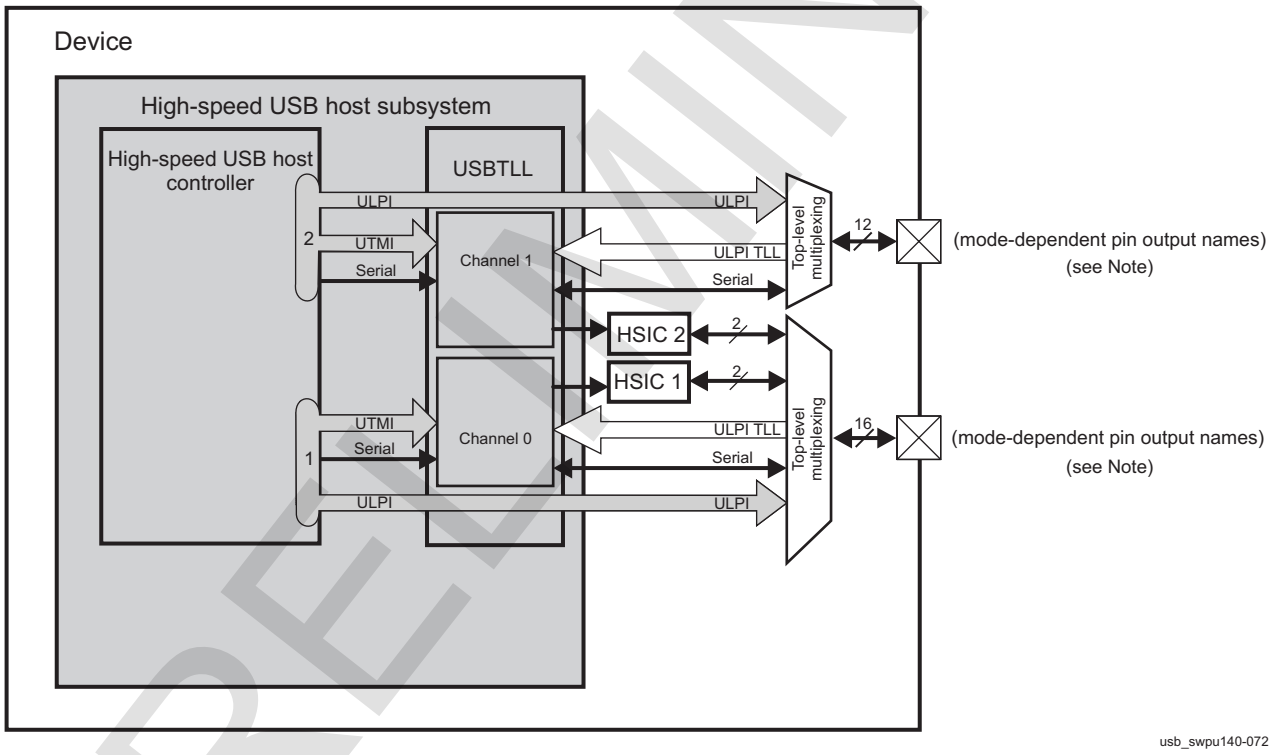
23.11.2 HS Multiport USB Host Subsystem Environment

The HS USB host subsystem provides three kinds of interfaces for connection:

- ULPIs for HS data transactions (up to 480 Mbps) (see Section 23.11.2.1, *ULPIs*)
- Serial interfaces, using the USBTLL module, for FS and LS data transactions (up to 12 Mbps) (see Section 23.11.2.2, *FS/LS Serial Interfaces*)
- HSIC interface to two HSIC lines over HSIC-capable I/O drivers (see Section 23.11.2.3, *HSIC Interface*)

Figure 23-233 is an overview of the environment of the HS USB host subsystem.

Figure 23-233. HS Multiport USB Host Subsystem Environment



NOTE: For more information about output pin names in different modes, see Section 23.11.2.1, *ULPIs*); Section 23.11.2.2, *FS/LS Serial Interfaces*; and Section 23.11.2.3, *HSIC Interface*.

NOTE: The two ports are configured independently and can be in different modes.

For more information how the pins are multiplexed, see Section 18.4.8, *PAD Functional Multiplexing and Configuration*.

23.11.2.1 ULPIs

The HS USB host subsystem supports the following configurations with the ULPIs:

- External USB transceiver:

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  - ULPIs: 12-pin/8-bit data SDR version
- TLL:
  - SDR ULPI mode (12-pin/8-bit data width)

The HS USB host subsystem supports USB ports that use the ULPI mode to connect to an off-chip HS ULPI transceiver (12-pin/8-bit data SDR mode) for data transactions (up to 480 Mbps). FS and LS are not supported over the ULPI.

The device supports TLL logic interfaces on its ports in ULPI TLL interface mode. TLL modes enable glueless interconnect to another USB device port.

The external USB transceiver ULPIs and ULPI TLL interfaces cannot be used together on the same port. It is possible for one port to use ULPI and the other port to use ULPI TLL.

Figure 23-234 and Figure 23-235 show typical applications using the HS USB host subsystem with ULPI and the ULPI TLL interface, respectively.

Figure 23-234. External USB Transceiver ULPIs

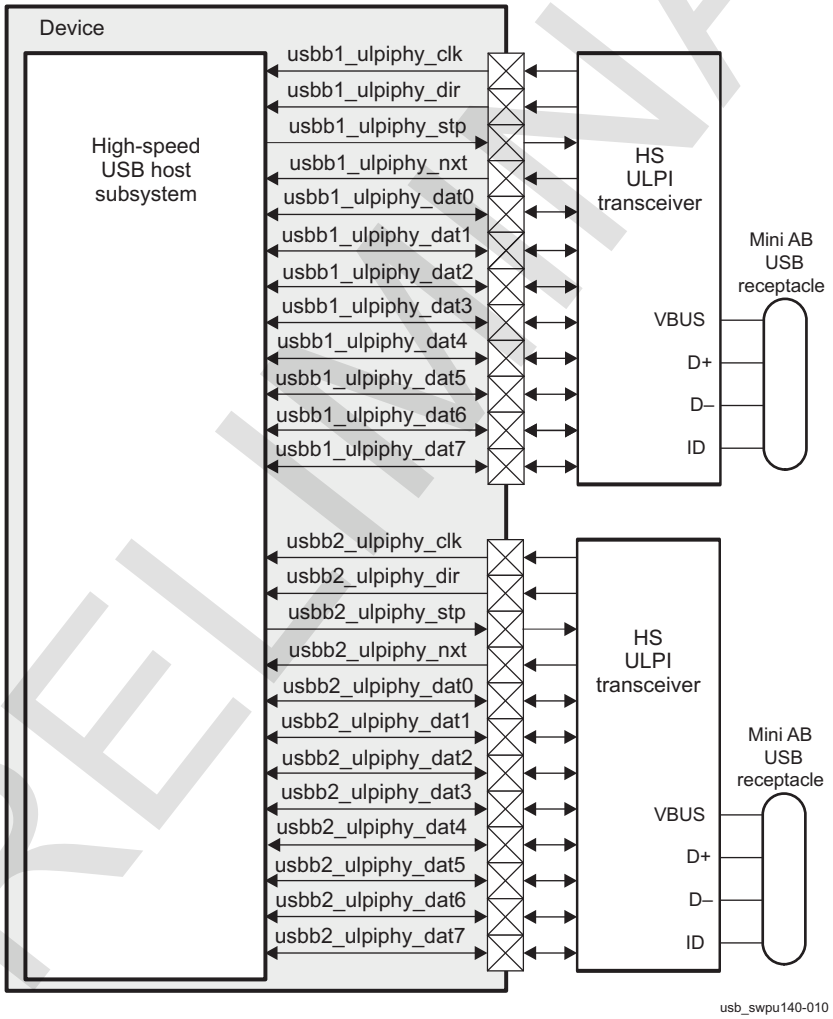

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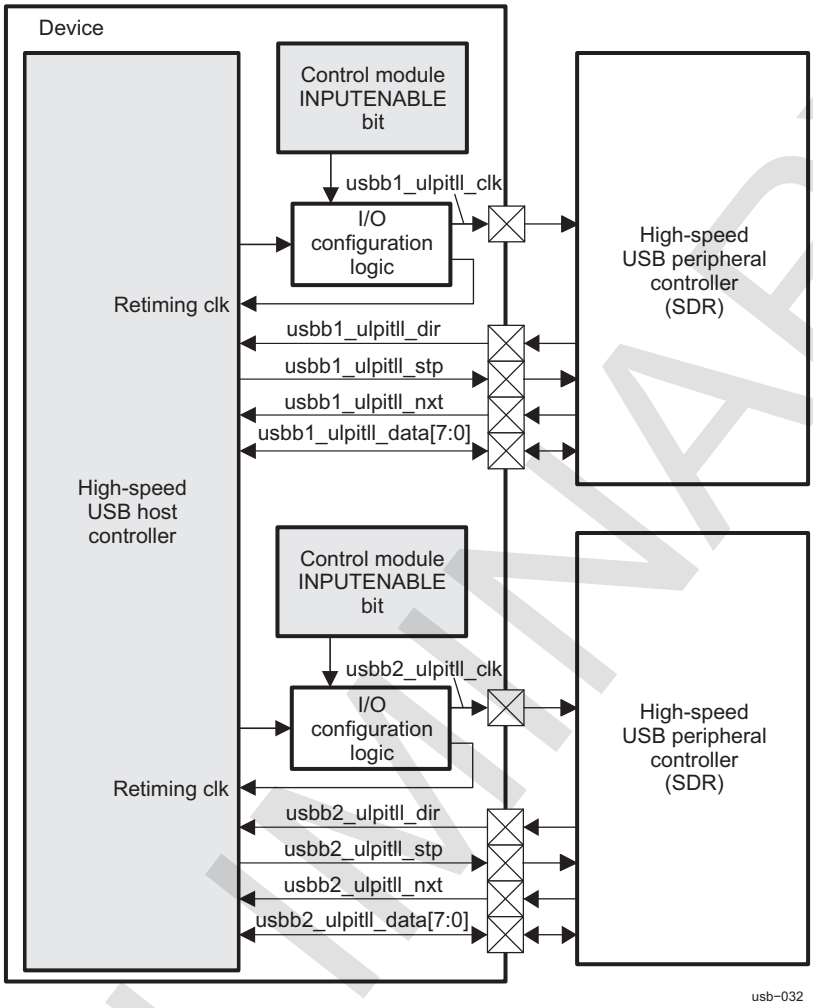
Figure 23-235. ULPI TLL Interfaces



The 12-pin ULPI uses an 8-bit data bus with data synchronous to the rising edge of the PHY (transceiver) clock (SDR mode).

23.11.2.1.1 Transceiver Interface Configuration in ULPI Mode

The HS USB host subsystem supports only the 12-pin/8-bit data SDR version of the ULPI mode.

Figure 23-236 shows USB ports using the 12-pin/8-bit data SDR version of the ULPI mode.

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Figure 23-236. ULPIs – 12-Pin/8-Bit Data SDR Version

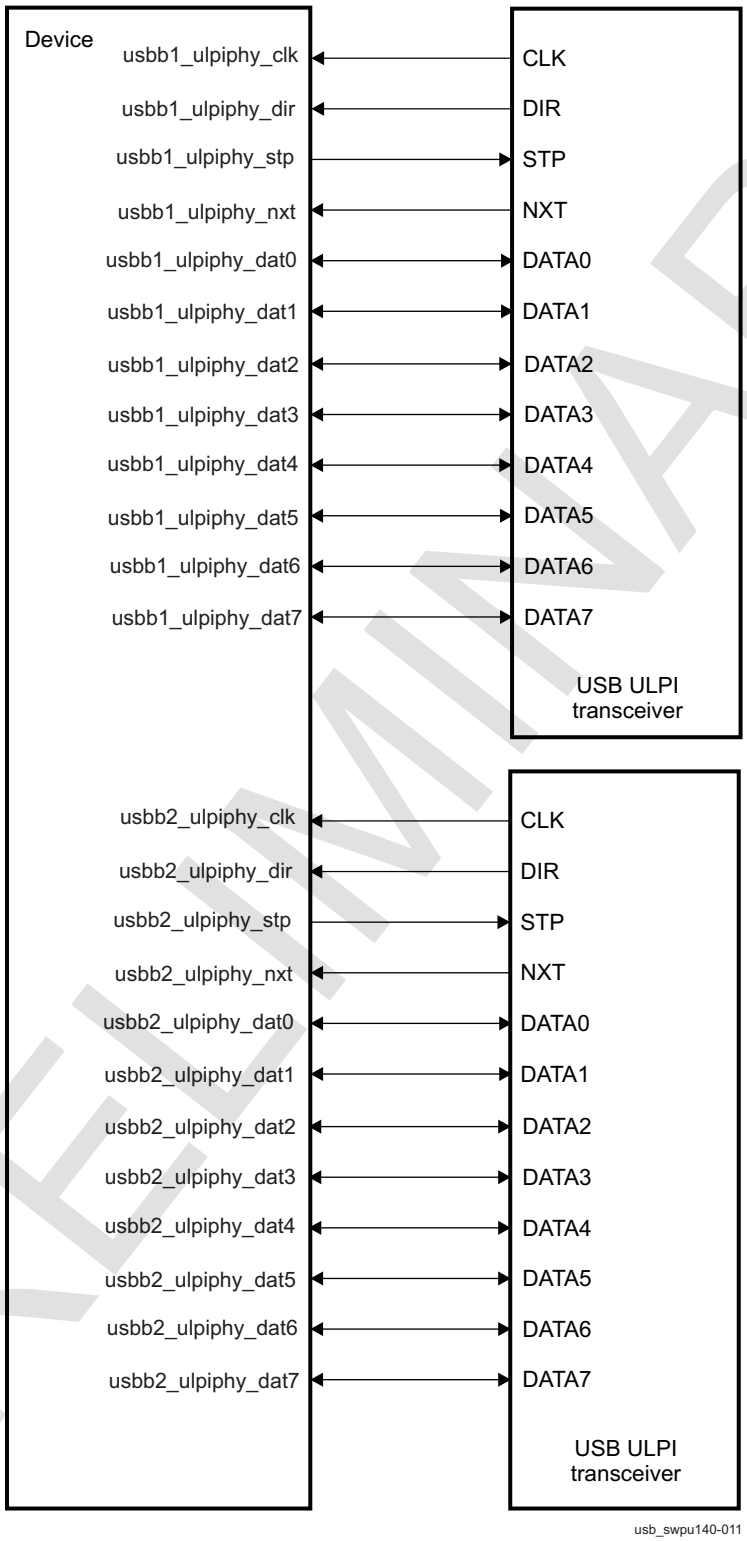

Table 23-930 describes the I/O pins of the USB ports using the 12-pin/8-bit data SDR version of the ULPI mode.

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Table 23-930. ULPI – 12-Pin/8-Bit Data SDR Version I/O Description

Signal Name	I/O [1]	Description	Reset Value
HS USB Host Controller Port 1			
usbb1_ulpiphy_clk	I	Clock input from remote PHY IC	0
usbb1_ulpiphy_dir	I	Data direction control from remote PHY IC	Unknown
usbb1_ulpiphy_stp	O	Stop signal to remote PHY IC	1
usbb1_ulpiphy_nxt	I	Next signal from remote PHY IC	Unknown
usbb1_ulpiphy_dat0	I/O	Bidirectional DATA0	Unknown
usbb1_ulpiphy_dat1	I/O	Bidirectional DATA1	Unknown
usbb1_ulpiphy_dat2	I/O	Bidirectional DATA2	Unknown
usbb1_ulpiphy_dat3	I/O	Bidirectional DATA3	Unknown
usbb1_ulpiphy_dat4	I/O	Bidirectional DATA4	Unknown
usbb1_ulpiphy_dat5	I/O	Bidirectional DATA5	Unknown
usbb1_ulpiphy_dat6	I/O	Bidirectional DATA6	Unknown
usbb1_ulpiphy_dat7	I/O	Bidirectional DATA7	Unknown
HS USB Host Controller Port 2			
usbb2_ulpiphy_clk	I	Clock input from remote PHY IC	0
usbb2_ulpiphy_dir	I	Data direction control from remote PHY IC	Unknown
usbb2_ulpiphy_stp	O	Stop signal to remote PHY IC	1
usbb2_ulpiphy_nxt	I	Next signal from remote PHY IC	Unknown
usbb2_ulpiphy_dat0	I/O	Bidirectional DATA0	Unknown
usbb2_ulpiphy_dat1	I/O	Bidirectional DATA1	Unknown
usbb2_ulpiphy_dat2	I/O	Bidirectional DATA2	Unknown
usbb2_ulpiphy_dat3	I/O	Bidirectional DATA3	Unknown
usbb2_ulpiphy_dat4	I/O	Bidirectional DATA4	Unknown
usbb2_ulpiphy_dat5	I/O	Bidirectional DATA5	Unknown
usbb2_ulpiphy_dat6	I/O	Bidirectional DATA6	Unknown
usbb2_ulpiphy_dat7	I/O	Bidirectional DATA7	Unknown

(1) I = Input; O = Output

23.11.2.1.2 TLL Interface Configuration in ULPI Mode

The HS USB host controller is coupled with the USBTLL module to compose the ULPI TLL interface modes.

Figure 23-237 shows USB ports using the 12-pin/8-bit data SDR version of the ULPI TLL interface mode.

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Figure 23-237. ULPI TLL Interfaces – 12-Pin/8-Bit Data SDR Version

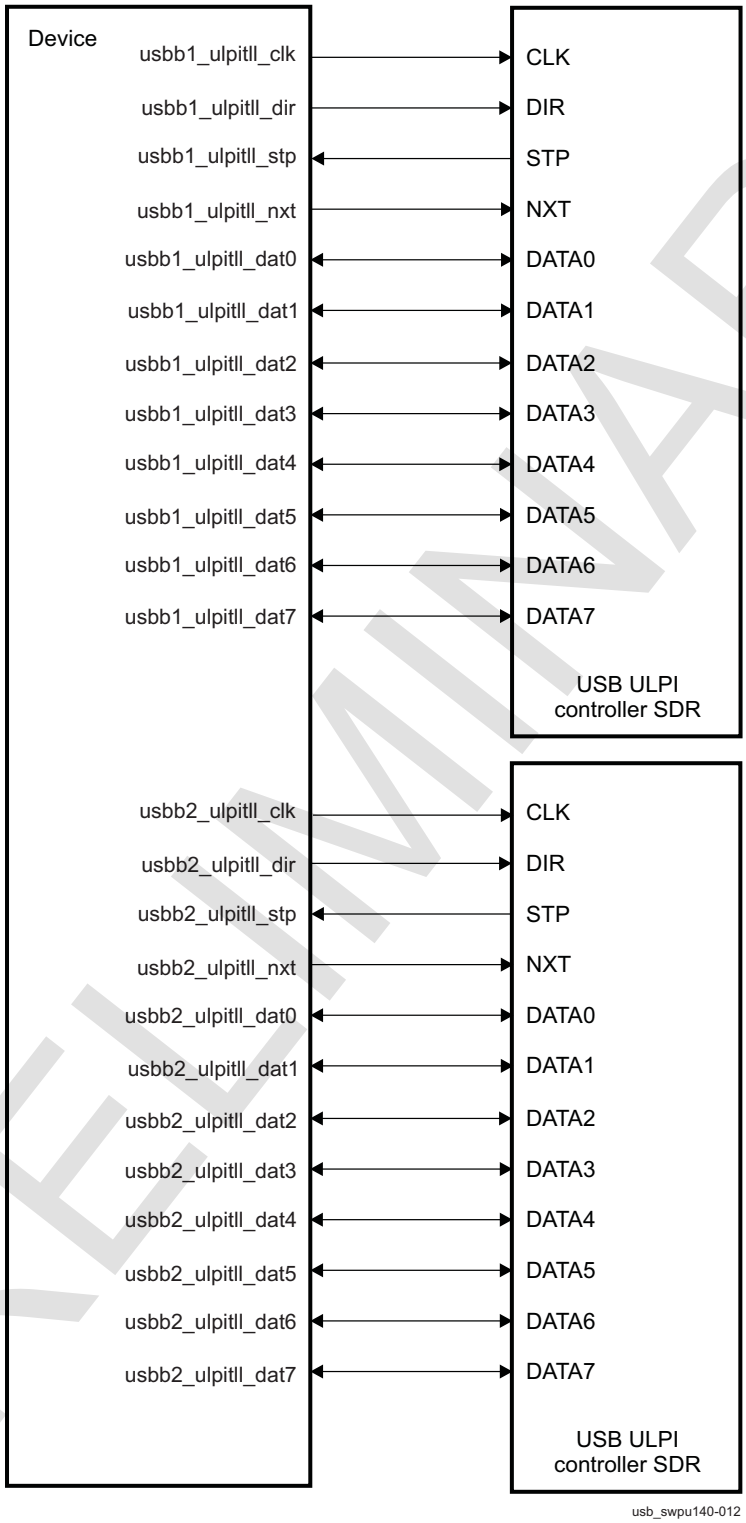

Table 23-931 describes the I/O pins of the USB ports using the 12-pin/8-bit data SDR version of the ULPI TLL interface mode.

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Table 23-931. ULPI TLL Interfaces – 12-Pin/8-Bit Data SDR Version I/O Description

Signal Name	I/O [1]	Description	Reset Value
HS USB TLL Port 1			
usbb1_ulpitll_clk	O	Clock output to remote ULPI link controller [2]	0
usbb1_ulpitll_dir	O	Data direction control from remote ULPI link controller	0
usbb1_ulpitll_stp	I	Stop signal to remote ULPI link controller	Unknown
usbb1_ulpitll_nxt	O	Next signal from remote ULPI link controller	0
usbb1_ulpitll_dat0	I/O	Bidirectional DATA0	0
usbb1_ulpitll_dat1	I/O	Bidirectional DATA1	0
usbb1_ulpitll_dat2	I/O	Bidirectional DATA2	0
usbb1_ulpitll_dat3	I/O	Bidirectional DATA3	0
usbb1_ulpitll_dat4	I/O	Bidirectional DATA4	0
usbb1_ulpitll_dat5	I/O	Bidirectional DATA5	0
usbb1_ulpitll_dat6	I/O	Bidirectional DATA6	0
usbb1_ulpitll_dat7	I/O	Bidirectional DATA7	0
HS USB TLL Port 2			
usbb2_ulpitll_clk	O	Clock output to remote ULPI link controller [2]	0
usbb2_ulpitll_dir	O	Data direction control from remote ULPI link controller	0
usbb2_ulpitll_stp	I	Stop signal to remote ULPI link controller	Unknown
usbb2_ulpitll_nxt	O	Next signal from remote ULPI link controller	0
usbb2_ulpitll_dat0	I/O	Bidirectional DATA0	0
usbb2_ulpitll_dat1	I/O	Bidirectional DATA1	0
usbb2_ulpitll_dat2	I/O	Bidirectional DATA2	0
usbb2_ulpitll_dat3	I/O	Bidirectional DATA3	0
usbb2_ulpitll_dat4	I/O	Bidirectional DATA4	0
usbb2_ulpitll_dat5	I/O	Bidirectional DATA5	0
usbb2_ulpitll_dat6	I/O	Bidirectional DATA6	0
usbb2_ulpitll_dat7	I/O	Bidirectional DATA7	0

(1) I = Input; O = Output

(2) This signal is also used as retiming input (the INPUTENABLE bit in the corresponding pad configuration register must be set to 1).

23.11.2.2 FS/LS Serial Interfaces

The HS USB host subsystem supports the following configurations with the serial interfaces:

- External USB transceiver (see Section 23.11.2.2.3, *External USB Transceiver Interface Configurations in Serial Modes*)
  - Serial 6-pin PHY (transceiver) interfaces: 6-pin mode (TX: DAT/SE0 or TX: DP/DM unidirectional mode), 4-pin mode (DP/DM bidirectional mode), and 3-pin mode (DAT/SE0 bidirectional mode)
- TLL (see Section 23.11.2.2.4, *TLL Interface Configurations in Serial Modes*)
  - Serial 6-pin TLL interfaces: 6-pin mode (DAT/SE0 and DP/DM unidirectional modes), 4-pin mode (DP/DM bidirectional mode), 3-pin mode (DAT/SE0 bidirectional mode), and 2-pin mode (DAT/SE0 and DP/DM bidirectional modes)

CAUTION

Only FS and LS data transactions are possible in serial mode. Transceiver interface is serial (its frequency is that of the actual USB line) and combinatorial (no clock is passed).

Whether in TLL or external transceiver configuration, the serial interface follows the same principles: it is limited to FS/LS, and HS requires a parallel interface.

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23.11.2.2.1 Encoding in Serial Mode

23.11.2.2.1.1 Unidirectional

When an external USB transceiver is connected to the device and is used in 6-pin unidirectional DAT/SE0 encoding mode, the encoding described in Table 23-932 is used.

Table 23-932. Signaling Between HS USB Host Subsystem and 6-Pin Unidirectional USB Transceiver (DAT/SE0 Signaling)

Logical Signal Name	Device Pin Direction	Transceiver Pin Direction	Description				
TXEN	Output	Input	When low, the USB transceiver drives D+ and D–.				
DAT and SE0	Output	Input	Controls the values output by the USB transceiver on D+ and D– when TXEN is low; ignored when TXEN is high.				
			TXEN	DAT	SE0	D+	D–
			0	0	0	0	1
			0	1	0	1	0
			0	X	1	0	0
			1	X	X	Undriven	Undriven
RCV	Input	Output	Output from transceiver differential receiver				
			D+	D–	RCV		
			0	0	X		
			0	1	0		
			1	0	1		
			1	1	X		
DP	Input	Output	Output from transceiver single-ended D+ signal receiver				
			D+	DP			
			0	0			
			1	1			
DM	Input	Output	Output from transceiver single-ended D- signal receiver				
			D–	DM			
			0	0			
			1	1			

When an external USB transceiver is connected to the device and is used in 6-pin unidirectional DP/DM encoding mode, the encoding described in Table 23-933 is used.

Table 23-933. Signaling Between HS USB Host Subsystem and 6-Pin Unidirectional USB Transceiver (DP/DM Signaling)

Logical Signal Name	Device Pin Direction	Transceiver Pin Direction	Description				
TXEN	Output	Input	When low, the USB transceiver drives D+ and D–.				
DAT and SE0	Output	Input	Controls the values output by the USB transceiver on D+ and D– when TXEN is low; ignored when TXEN is high.				
			TXEN	DAT	SE0	D+	D–
			0	0	1	0	1
			0	1	0	1	0
			0	0	0	0	0
			1	X	X	Undriven	Undriven

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Table 23-933. Signaling Between HS USB Host Subsystem and 6-Pin Unidirectional USB Transceiver (DP/DM Signaling) (continued)

Logical Signal Name	Device Pin Direction	Transceiver Pin Direction	Description		
RCV	Input	Output	Output from transceiver differential receiver		
			D+	D–	RCV
			0	0	X
			0	1	0
			1	0	1
			1	1	X
DP	Input	Output	Output from transceiver single-ended D+ signal receiver		
			D+	DP	
			0	0	
			1	1	
DM	Input	Output	Output from transceiver single-ended D-signal receiver		
			D–	DM	
			0	0	
			1	1	

23.11.2.2.1.2 Bidirectional

When an external USB or USB OTG transceiver is connected to the device and is used in 3-pin bidirectional DAT/SE0 encoding mode, the encoding described in Table 23-934 is used.

Table 23-934. Signaling Between HS USB Host Subsystem and 3-Pin Bidirectional USB Transceiver Using DAT/SE0 Signaling

Logical Signal Name	Device Pin Direction	Transceiver Pin Direction	Description				
TXEN	Output	Input	When low, the USB transceiver drives D+ and D–.				
DAT and SE0	Output	Input	When TXEN is low, the device drives DAT and SE0 and the transceiver drives D+ and D– based on the values of DAT and SE0.				
	Output	Input	TXEN	DAT	SE0	D+	D–
			0	0	0	0	1
				1	0	1	0
				X	1	0	0
	Input	Output	TXEN	D+	D–	DAT	SE0
			1	0	0	0	1
				0	1	0	0
				1	0	1	0
				1	1	Undefined	0

NOTE: The device does not support 3-wire bidirectional signaling using DP/DM signals.

When an external USB or USB OTG transceiver is connected to the device and is used in 4-pin bidirectional DP/DM encoding mode, the encoding described in Table 23-935 is used.

Table 23-935. Signaling Between HS USB Host Subsystem and 4-Pin Bidirectional USB Transceiver Using DP/DM Signaling

Logical Signal Name	Device Pin Direction	Transceiver Pin Direction	Description
TXEN	Output	Input	When low, the USB transceiver drives D+ and D–.

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Table 23-935. Signaling Between HS USB Host Subsystem and 4-Pin Bidirectional USB Transceiver Using DP/DM Signaling (continued)

Logical Signal Name	Device Pin Direction	Transceiver Pin Direction	Description		
DM	Output	Input	Value driven to or received from D–		
			TXEN	DM	D–
			0	0	0
			0	1	1
	Input	Output	TXEN	D–	DM
			1	0	0
			1	1	1
DP	Output	Input	Value driven to or received from D+		
			TXEN	DP	D+
			0	0	0
			0	1	1
	Input	Output	TXEN	D+	DP
			1	0	0
			1	1	1
RCV	Input	Output	Output from transceiver differential receiver		
			D+	D–	RCV
			0	0	X
			0	1	0
			1	0	1
			1	1	X

23.11.2.2.2 Sideband Signals for Serial Modes

Serial interfaces carry only the USB data information. Sideband control and status (respectively, to/from the transceiver/TLL or to the bus lines themselves) require additional signals, which are usually implemented in a case-by-case, ad hoc way.

- Sideband control examples: FS/LS (slew rate control), transceiver suspend, connect (D+/D- pullup), pulldown enable, VBUS drive, etc.
- Sideband status example: VBUS level (VBUS valid, session valid, session end, etc.)
- Sideband signal implementations: Dedicated lines (one per sideband information bit), serial bus + interrupt line with register-mapped control/status (I^2C) UART, etc.)

Figure 23-238 and Figure 23-239 show system integration for sideband signals for two logically identical USB connections: one in transceiver configuration and one in TLL configuration. Although the sideband (purple) arrows are oriented from the controller to the transceiver in the two figures, the sideband information flow is bidirectional (that is, it flows from the controller to the transceiver [control] and from the transceiver to the controller [status]).

Figure 23-238 shows the transceiver configuration, where each side connects the sideband signals to its own transceiver. On the device (containing the USBTLL module), the sideband is decoded/re-encoded. The sideband signals available at the device boundary (and the USBTLL module) are decoded from the standard UTMI+ interface.

- The software-driven VBUS reporting procedure is described in Section 23.11.4.2.6.1.1, *VBUS Management in Serial Transceiver Configurations*.

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Figure 23-238. Serial Interface Sideband Integration – Transceiver Configuration

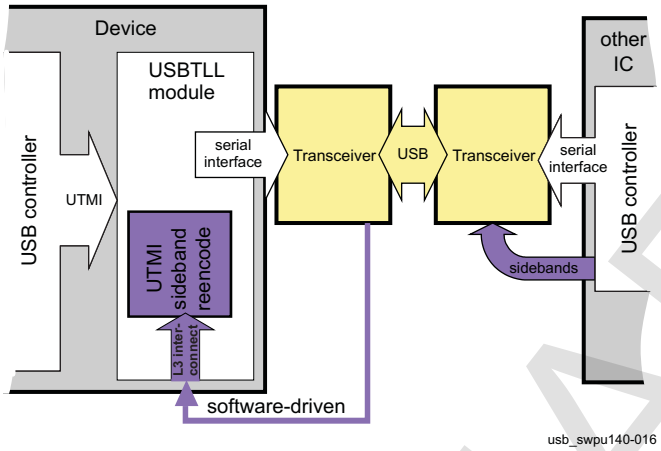
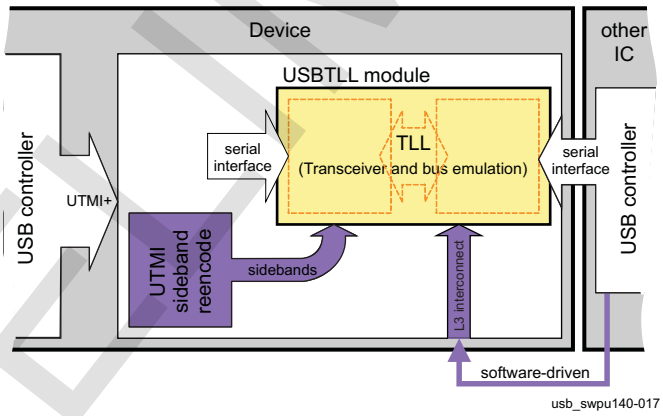


Figure 23-239 shows the TLL configuration, where both transceivers are emulated inside the USBTLL module.

- The transceiver of the local controller (left side of the figure) is working with the sideband information to/from the UTMI+ port. This is internal to the USBTLL module.
- The transceiver of the remote controller (right side of the figure) must communicate with its controller, which is on another IC. This is done in two ways:
  - The sideband input signals at the TLL module boundary (tllpuen, tlldrvvbus, tllvbusvalid, etc.)
  - The software-driven VBUS control procedure described in Section 23.11.4.2.6.2.2, *VBUS Emulation in Serial TLL Modes*)

Figure 23-239. Serial Interface Sideband Integration – TLL Configuration



23.11.2.2.3 External USB Transceiver Interface Configurations in Serial Modes

An external USB transceiver is required for each USB port used in the system. It converts between appropriate signaling for the HS USB host subsystem and appropriate signaling for the USB wire.

The serial interface mode of the HS USB host subsystem includes support for several types of USB transceivers. It provides signaling to up to two external USB transceivers.

Several types of external transceiver signaling are supported. Signaling between the HS USB subsystem in serial interface mode and the external USB transceiver for monitoring and controlling the differential USB signal can be done through a 6-, 4-, or 3-wire signaling interface, with two or more control signals provided by additional signals or through an I^2C link.

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The following subsections describe the transceiver interface modes supported by the HS USB host subsystem in the serial interface mode. In each case, the subsystem is connected to external transceivers, on the other side of the USB lines (D+/D–).

23.11.2.2.3.1 Unidirectional Transceiver Interface Modes: 6-Pin

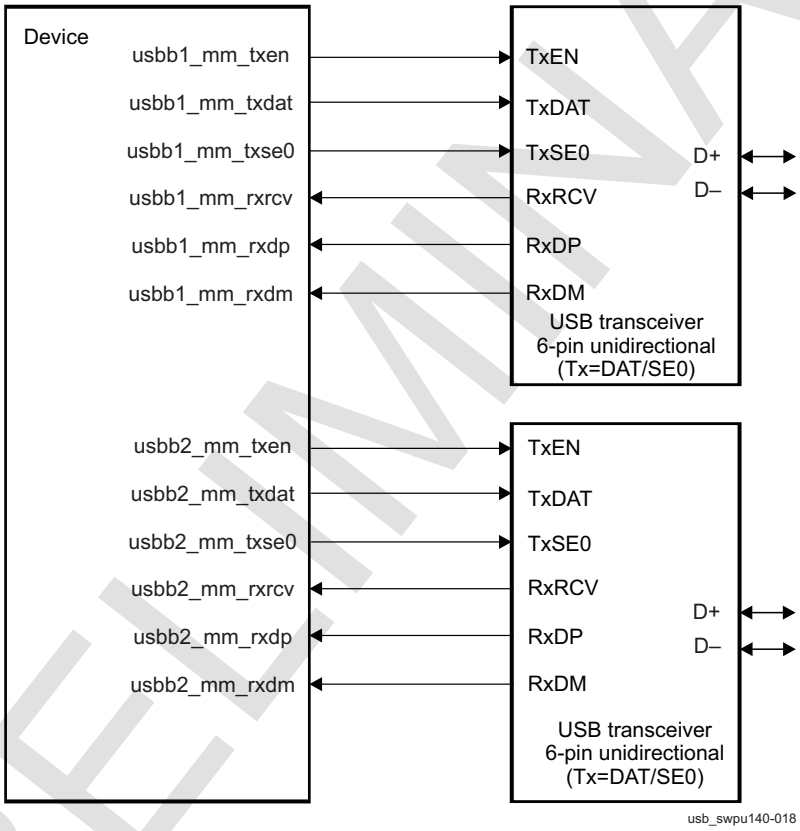
The 6-pin modes are the "natural" transceiver interface modes for the FS transceivers in the sense that they mirror the internal makeup of the transceivers.

Two encodings exist for TX: DAT/SE0 and DP/DM.

When an external USB is connected to the device and is used in 6-pin unidirectional DAT/SE0 signaling mode, the signaling described in Table 23-932 is used.

Figure 23-240 shows a USB port using DAT/SE0 encoding.

Figure 23-240. 6-Pin Unidirectional Using DAT/SE0 Signaling



When a USB is connected to the device and is used in 6-pin unidirectional DP/DM signaling mode, the signaling described in Table 23-933 is used.

Figure 23-241 shows a USB port using DP/DM encoding.

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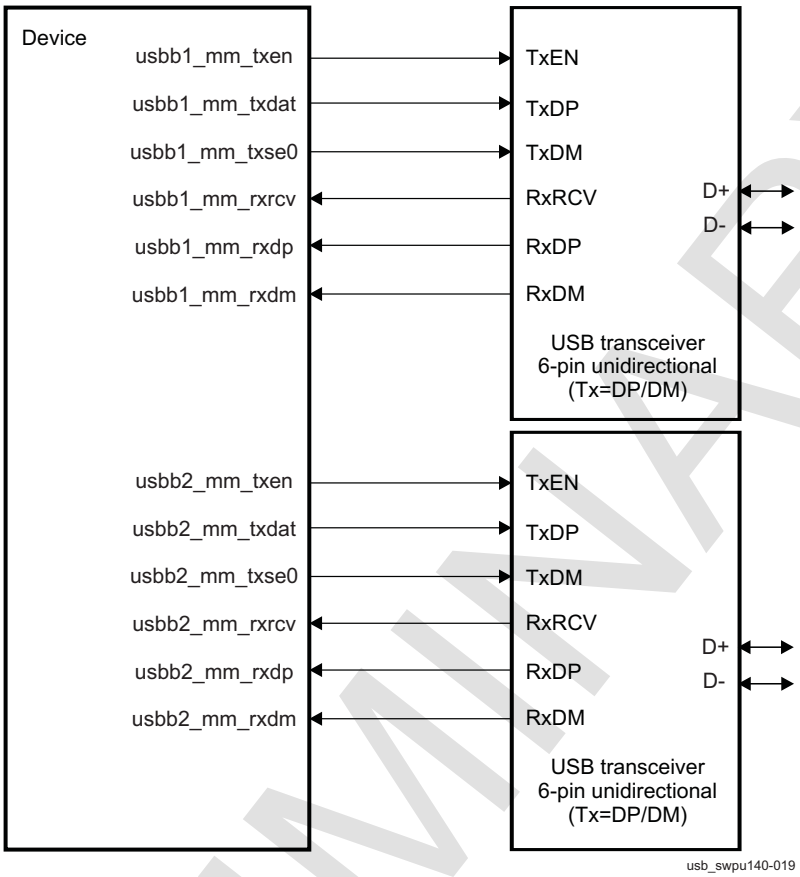
Figure 23-241. 6-Pin Unidirectional Using DP/DM Signaling



23.11.2.2.3.2 Bidirectional Transceiver Interface Modes: 3-Pin, 4-Pin

The bidirectional transceiver interface modes are pin-count optimizations of the unidirectional modes. They take advantage of the fact that a USB port is sending or receiving at any given time, but never both. The TX and RX paths of the unidirectional mode can be multiplexed on bidirectional lines. To prevent glitches at TX/RX turnaround, the same encoding is used for both directions (DAT/SE0 or DP/DM).

The signaling described in Table 23-934 is used when a USB transceiver is connected to the device and is used in 3-pin bidirectional DAT/SE0 signaling mode.

NOTE: The device does not support 3-wire bidirectional signaling using DP/DM signals.

Figure 23-242 shows a USB port using DAT/SE0 encoding.

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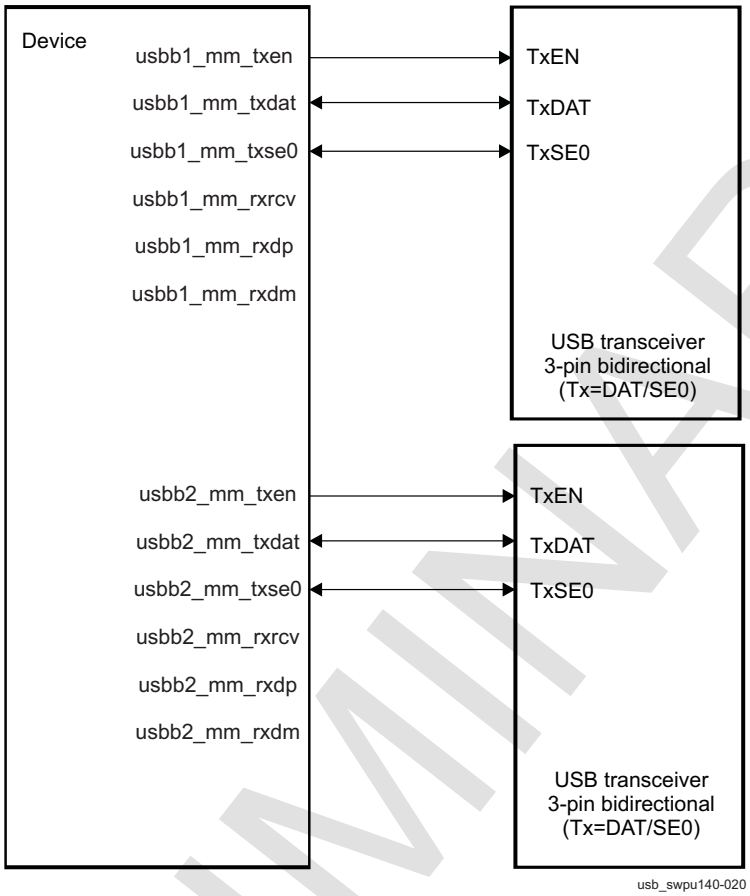
Figure 23-242. 3-Pin Bidirectional Using DAT/SE0 Signaling



The signaling described in Table 23-935 is used when a USB transceiver is connected to the device and is used in 4-pin bidirectional DP/DM signaling mode.

Figure 23-243 shows a USB port using DP/DM encoding.

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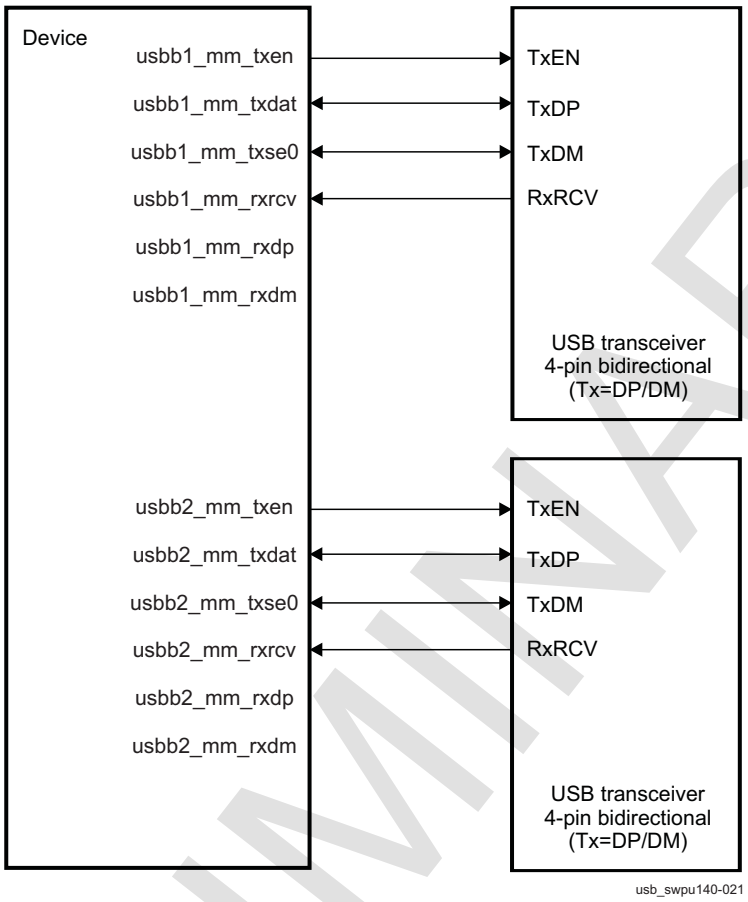
Figure 23-243. 4-Pin Bidirectional Using DP/DM Signaling



23.11.2.2.4 TLL Interface Configurations in Serial Modes

The HS USB host subsystem supports unidirectional and bidirectional TLL logic interfaces on its ports. The TLL modes enable glueless interconnect to the USB device port of another device without needing a costly transceiver.

Serial interface modes are FS or LS only. Transceiver interface is serial (its frequency is that of the actual USB line) and combinatorial (no clock is passed).

23.11.2.2.4.1 Unidirectional TLL Serial Modes

The 6-pin TLL configurations are mirror images of the 6-pin transceiver configurations previously discussed. The same signals are mapped on the same physical pins, but in opposite directions.

Two possible modes exist, depending on the TX data encoding used by the external device.

Figure 23-244 shows an external device using DAT/SE0 encoding.

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Figure 23-244. 6-Pin Unidirectional TLL Using DAT/SE0 Signaling

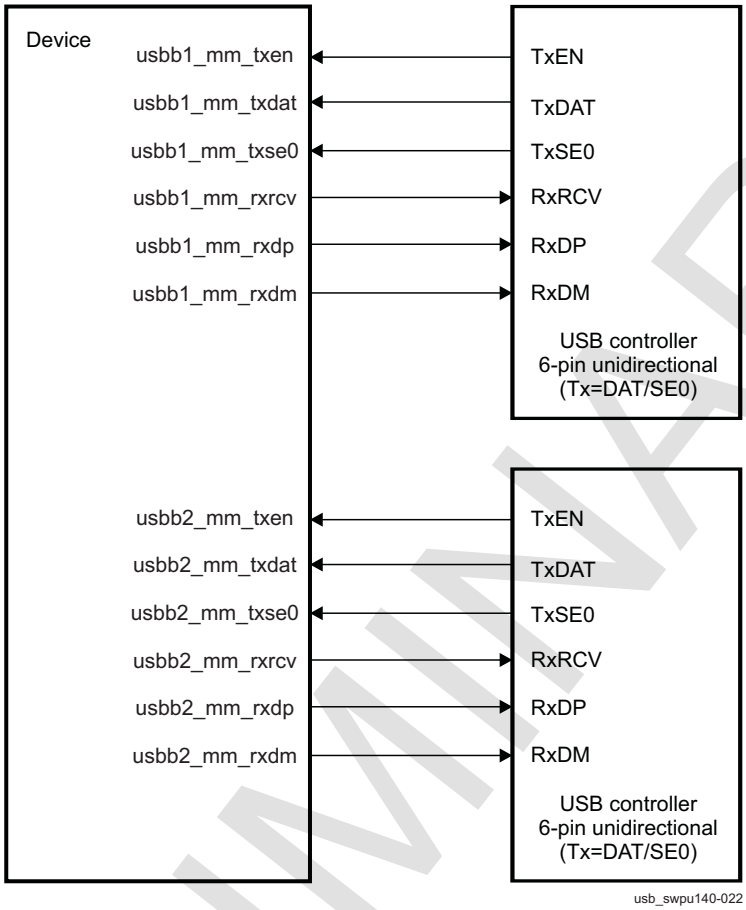

Figure 23-245 shows an external device using DP/DM encoding.

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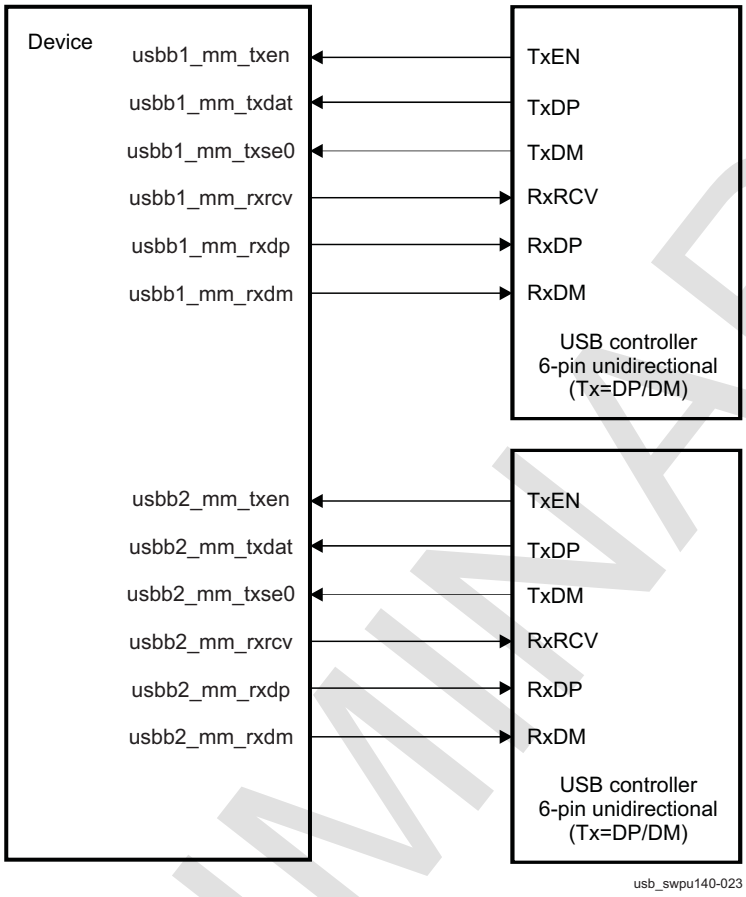
Figure 23-245. 6-Pin Unidirectional TLL Using DP/DM Signaling



23.11.2.2.4.2 Bidirectional TLL Serial Modes

The 3-pin/4-pin TLL configurations are mirror images of the 3-pin/4-pin transceiver configurations previously discussed. The same signals are mapped on the same physical pins, but in opposite directions (bidirectional lines remain bidirectional).

Two possible modes exist, depending on the TX data encoding used by the external device.

Figure 23-246 shows an external device using DAT/SE0 encoding.

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Figure 23-246. 3-Pin Bidirectional TLL Using DAT/SE0 Signaling

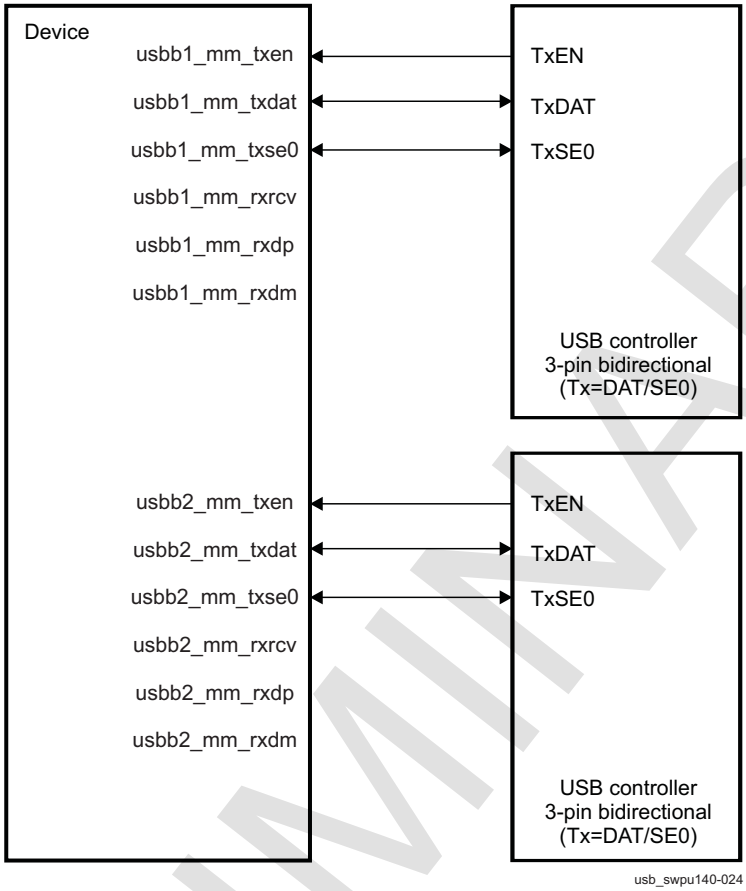

Figure 23-247 shows an external device using DP/DM encoding.

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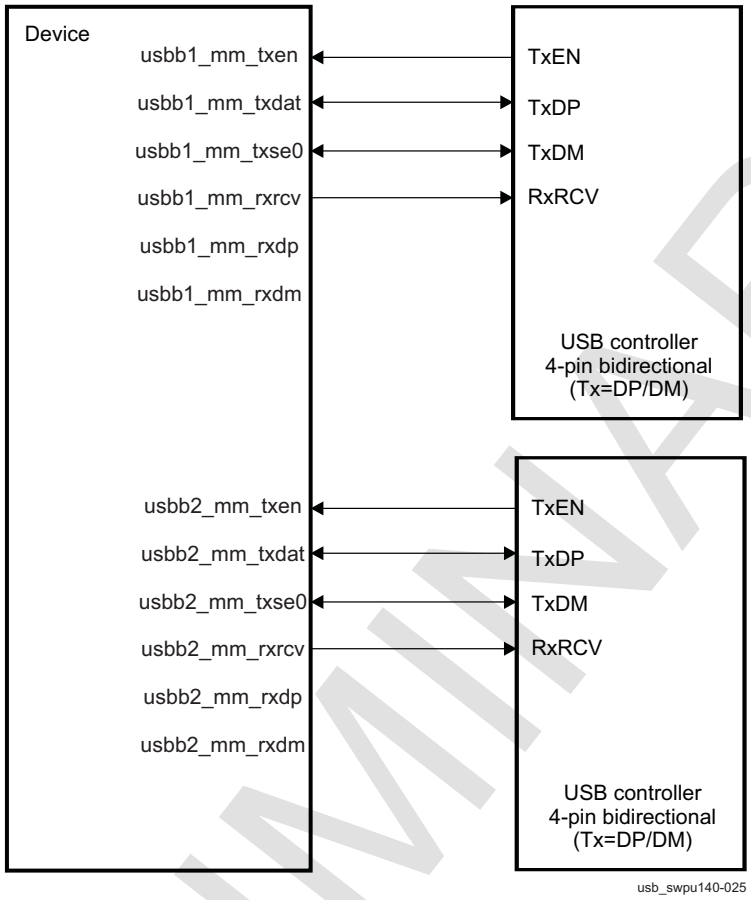
Figure 23-247. 4-Pin Bidirectional TLL Using DP/DM Signaling



The 2-pin TLL configurations have unique specifications:

- They require pullups/pulldowns to operate, because the bidirectional lines are not driven at all times like the other serial transceiver interfaces described previously. The connection of pull resistors depends on the speed of the controller.
- The module supports explicit 2-pin TLL modes, with DAT/SE0 or DP/DM encoding.
- Non-TLL modes (that is, transceiver configuration mode) can be used to implement the 2-pin functionality, using a specific connectivity.

Figure 23-248 shows a USB port using DP/DM encoding.

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Figure 23-248. 2-Pin Bidirectional TLL Using DP/DM Encoding, With 4-Pin Bidirectional USB Device

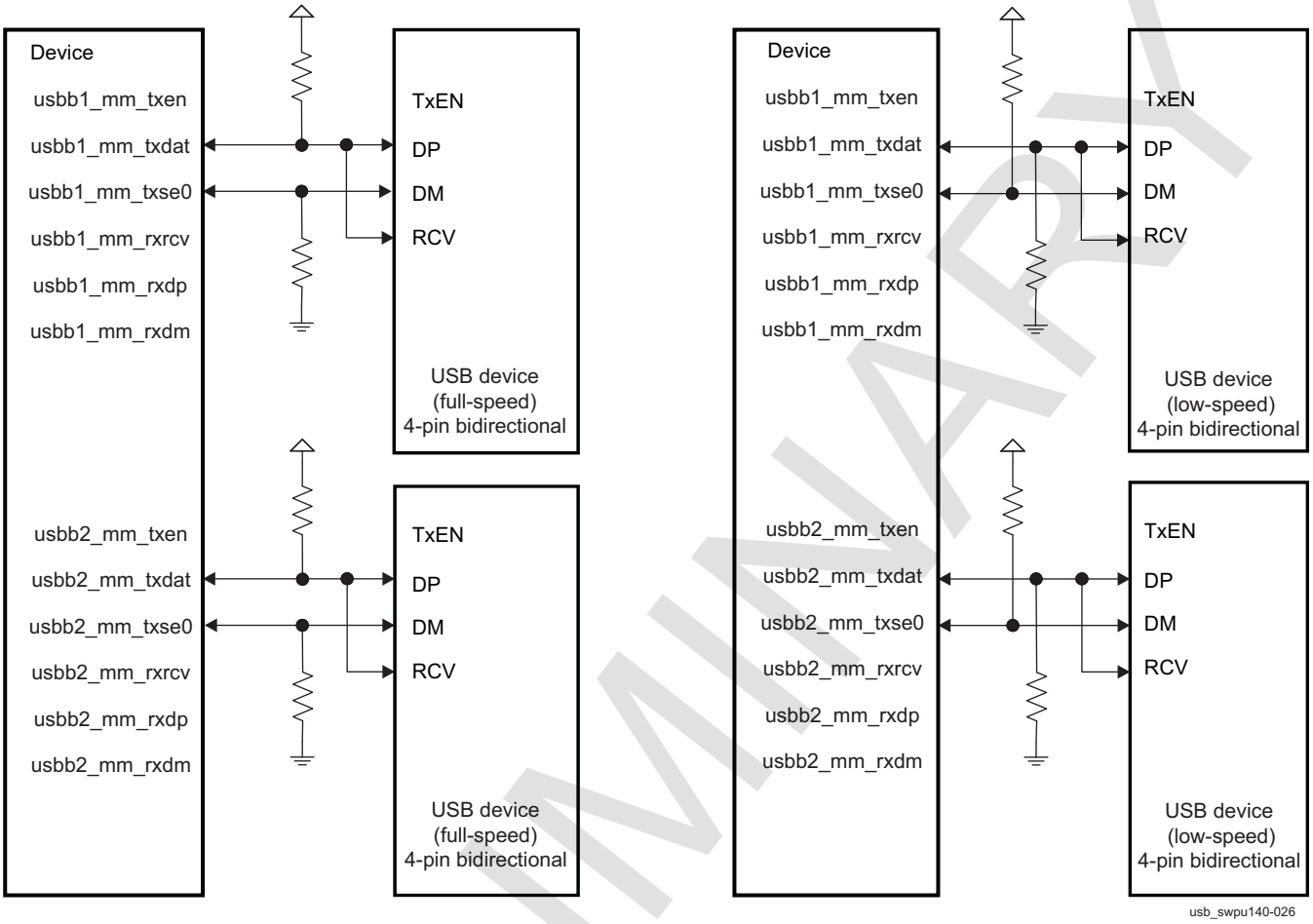

Table 23-936 shows the pullup/pulldown configuration for DP/DM encoding.

Table 23-936. Pullup/Pulldown Configuration for DP/DM Encoding

	Nonconnected Device (Any Speed)	Connected LS Device	Connected FS Device
DP	Pulldown	Pulldown	Pullup
DM	Pulldown	Pullup	Pulldown

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Figure 23-249 shows a USB port using DAT/SE0 encoding.

Figure 23-249. 2-Pin Bidirectional TLL Using DAT/SE0 Encoding, With 3-Pin Bidirectional USB Device

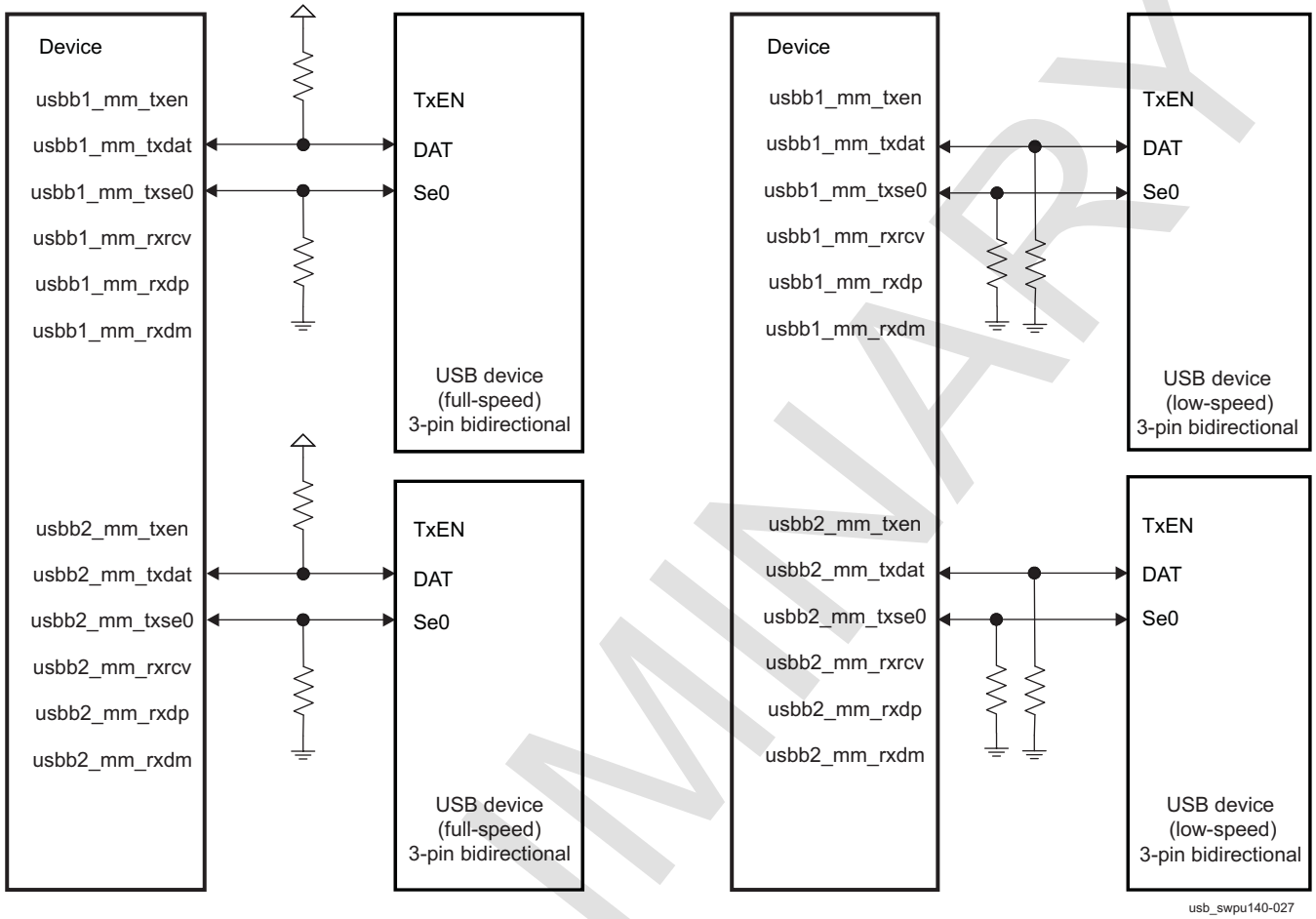

Table 23-937 shows the pullup/pulldown configuration for DAT/SE0 encoding.

Table 23-937. Pullup/Pulldown Configuration for DAT/SE0 Encoding

	Nonconnected Device (Any Speed)	Connected LS Device	Connected FS Device
DAT	Pulldown	Pulldown	Pullup
SE0	Pullup	Pulldown	Pulldown

23.11.2.2.5 Interface Description in Serial Modes

Table 23-938 describes the I/O of the HS USB host subsystem serial interfaces.

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Table 23-938. I/O Description

Signal Name	I/O [1]	Description	Value at Reset
Multiple-Mode FS/LS Serial Interface: Port 1			
usbb1_mm_txse0	I/O	SE0 function in 3-pin bidirectional DAT/SE0 mode	0
	I/O	DM function in 4-pin bidirectional DP/DM mode	
	O	SE0 output in 6-pin unidirectional DAT/SE0 mode	
	O	DM output in 6-pin unidirectional DP/DM mode	
	I/O	SE0-TLL in 2-/3-pin bidirectional DAT/SE0 TLL mode	
	I/O	DM-TLL in 2-/4-pin bidirectional DP/DM TLL mode	
	I	SE0-TLL input in 6-pin unidirectional DAT/SE0 TLL mode	
	I	DM-TLL input in 6-pin unidirectional DP/DM TLL mode	
usbb1_mm_txdat	I/O	DAT function in 3-pin bidirectional DAT/SE0 mode	Unknown
	I/O	DP function in 4-pin bidirectional DP/DM mode	
	O	DAT output in 6-pin unidirectional DAT/SE0 mode	
	O	DP output in 6-pin unidirectional DAT/SE0 mode	
	I/O	DAT-TLL in 2-/3-pin bidirectional DAT/SE0 TLL mode	
	I/O	DP-TLL in 2-/4-pin bidirectional DP/DM TLL mode	
	I	DAT-TLL input in 6-pin unidirectional DAT/SE0 TLL mode	
	I	DP-TLL input in 6-pin unidirectional DP/DM TLL mode	
usbb1_mm_txen	O	Transmit enable in 3-pin bidirectional DAT/SE0 or 4-pin bidirectional DP/DM or 6-pin unidirectional modes	1
	I	Transmit enable in 3-pin bidirectional DAT/SE0 TLL or 4-pin bidirectional DP/DM TLL or 6-pin unidirectional TLL modes (not used in 2-pin bidirectional TLL modes)	
usbb1_mm_rxrcv	I	Differential receiver signal input in 4-pin bidirectional DP/DM or 6-pin unidirectional modes (not used in 3-pin bidirectional DAT/SE0 mode)	Unknown
	O	Differential receiver signal output in 4-pin bidirectional DP/DM TLL or 6-pin unidirectional TLL modes (not used in 3-pin bidirectional DAT/SE0 TLL or 2-pin bidirectional TLL modes)	
usbb1_mm_rxdp	I	Single-ended DP receiver signal input in 6-pin unidirectional modes (not used in 3-pin bidirectional DAT/SE0 or 4-pin bidirectional DP/DM modes)	Unknown
	O	Single-ended DP receiver signal output in 6-pin unidirectional TLL modes (not used in 3-pin bidirectional DAT/SE0 TLL or 4-pin bidirectional DP/DM TLL or 2-pin bidirectional TLL modes)	
usbb1_mm_rxdm	I	Single-ended DM receiver signal input in 6-pin unidirectional TLL modes (not used in 3-pin bidirectional DAT/SE0 or 4-pin bidirectional DP/DM or 2-pin bidirectional TLL modes)	Unknown
	O	Single-ended DM receiver signal output in 6-pin unidirectional TLL modes (not used in 3-pin bidirectional DAT/SE0 TLL or 4-pin bidirectional DP/DM TLL or 2-pin bidirectional TLL modes)	
Multiple-Mode FS/LS Serial Interface: Port 2			
usbb2_mm_txse0	I/O	SE0 function in 3-pin bidirectional DAT/SE0 mode	0
	I/O	DM function in 4-pin bidirectional DP/DM mode	
	O	SE0 output in 6-pin unidirectional DAT/SE0 mode	
	O	DM output in 6-pin unidirectional DP/DM mode	
	I/O	SE0-TLL in 2-/3-pin bidirectional DAT/SE0 TLL mode	
	I/O	DM-TLL in 2-/4-pin bidirectional DP/DM TLL mode	
	I	SE0-TLL input in 6-pin unidirectional DAT/SE0 TLL mode	
	I	DM-TLL input in 6-pin unidirectional DP/DM TLL mode	
usbb2_mm_txdat	I/O	DAT function in 3-pin bidirectional DAT/SE0 mode	Unknown
	I/O	DP function in 4-pin bidirectional DP/DM mode	
	O	DAT output in 6-pin unidirectional DAT/SE0 mode	
	O	DP output in 6-pin unidirectional DAT/SE0 mode	

[1] I = Input; O = Output

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Table 23-938. I/O Description (continued)

Signal Name	I/O [1]	Description	Value at Reset
Multiple-Mode FS/LS Serial Interface: Port 1			
	I/O	DAT-TLL in 2-/3-pin bidirectional DAT/SE0 TLL mode	
	I/O	DP-TLL in 2-/4-pin bidirectional DP/DM TLL mode	
	I	DAT-TLL input in 6-pin unidirectional DAT/SE0 TLL mode	
	I	DP-TLL input in 6-pin unidirectional DP/DM TLL mode	
usbb2_mm_txen	O	Transmit enable in 3-pin bidirectional DAT/SE0 or 4-pin bidirectional DP/DM or 6-pin unidirectional modes	1
	I	Transmit enable in 3-pin bidirectional DAT/SE0 TLL or 4-pin bidirectional DP/DM TLL or 6-pin unidirectional TLL modes (not used in 2-pin bidirectional TLL modes)	
usbb2_mm_rxrcv	I	Differential receiver signal input in 4-pin bidirectional DP/DM or 6-pin unidirectional modes (not used in 3-pin bidirectional DAT/SE0 mode)	Unknown
	O	Differential receiver signal output in the 4-pin bidirectional DP/DM TLL or 6-pin unidirectional TLL modes (not used in 3-pin bidirectional DAT/SE0 TLL or 2-pin bidirectional TLL modes)	
usbb2_mm_rxdp	I	Single-ended DP receiver signal input in 6-pin unidirectional modes (not used in 3-pin bidirectional DAT/SE0 or 4-pin bidirectional DP/DM modes)	Unknown
	O	Single-ended DP receiver signal output in 6-pin unidirectional TLL modes (not used in 3-pin bidirectional DAT/SE0 TLL or 4-pin bidirectional DP/DM TLL or 2-pin bidirectional TLL modes)	
usbb2_mm_rxdm	I	Single-ended DM receiver signal input in 6-pin unidirectional TLL modes (not used in 3-pin bidirectional DAT/SE0 or 4-pin bidirectional DP/DM or 2-pin bidirectional TLL modes)	Unknown
	O	Single-ended DM receiver signal output in 6-pin unidirectional TLL modes (not used in 3-pin bidirectional DAT/SE0 TLL or 4-pin bidirectional DP/DM TLL or 2-pin bidirectional TLL modes)	

NOTE: ULPI (PHY) interfaces and ULPI TLL interfaces cannot be used together: either the ULPI (PHY) interfaces or the ULPI TLL interfaces are selected

23.11.2.3 HSIC Interface

The HS USB host subsystem supports the configurations with the HSIC interfaces shown in Figure 23-250.

Figure 23-250. HSIC Interface

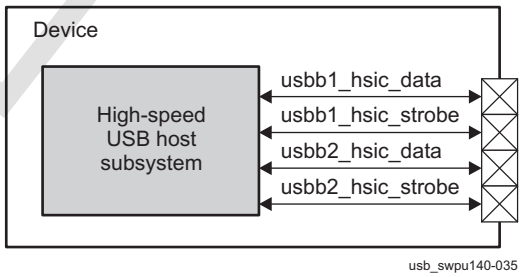

Table 23-939 describes the I/O of the HSIC interface of the HS USB host subsystem.

Table 23-939. HSIC Interface

Signal Name	I/O [1]	Description	Reset Value
HSUSB HSIC1			
usbb1_hsic_data	I/O	HS interchip data	Unknown

[1] I = Input; O = Output

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Table 23-939. HSIC Interface (continued)

Signal Name	I/O [1]	Description	Reset Value
usbb1_hsic_strobe	I/O	HS interchip strobe	Unknown
HSUSB HSIC2			
usbb2_hsic_data	I/O	HS interchip data	Unknown
usbb2_hsic_strobe	I/O	HS interchip strobe	Unknown

23.11.3 HS Multiport USB Host Subsystem Integration

This section describes the integration of the HS USB host subsystem, including information about clocks, resets, and hardware requests.

The USB host controller module includes other modules and additional logic attached to the UTMI/ULPI ports. The HS USB host controller is connected to the L3 interconnect master (initiator) and L4_CFG interconnect slave (target) interfaces.

The elements of the USB HS host subsystem are:

- The multiport USB host controller. Each port uses one of the following modes:
  - ULPI, to a ULPI PHY (typically, off-chip)
  - UTMI, to a local UTMI (typically, on-chip) PHY or emulation of a PHY
- A local phase-locked loop (PLL), able to provide the USB-grade 48-, 60-, 480-MHz clocks
- Two TLL channels, bundled inside a USBTLL module. Each HS TLL channel can be seen as emulating a pair of back-to-back PHYs, and has:
  - A UTMI port, connected to a controller port (the host, in this case)
  - A ULPI port, connected to a (typically, off-chip) ULPI controller (peripheral, in this case)
- Two HSIC DFEs. The DFE plugs into the UTMI port of an HSIC-capable controller (the host, in this case), and controls HSIC-capable bidirectional I/O drivers driving the HSIC lines (strobe/data).

Figure 23-251 shows the HS USB subsystem integration.

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Figure 23-251. HS USB Subsystem Integration

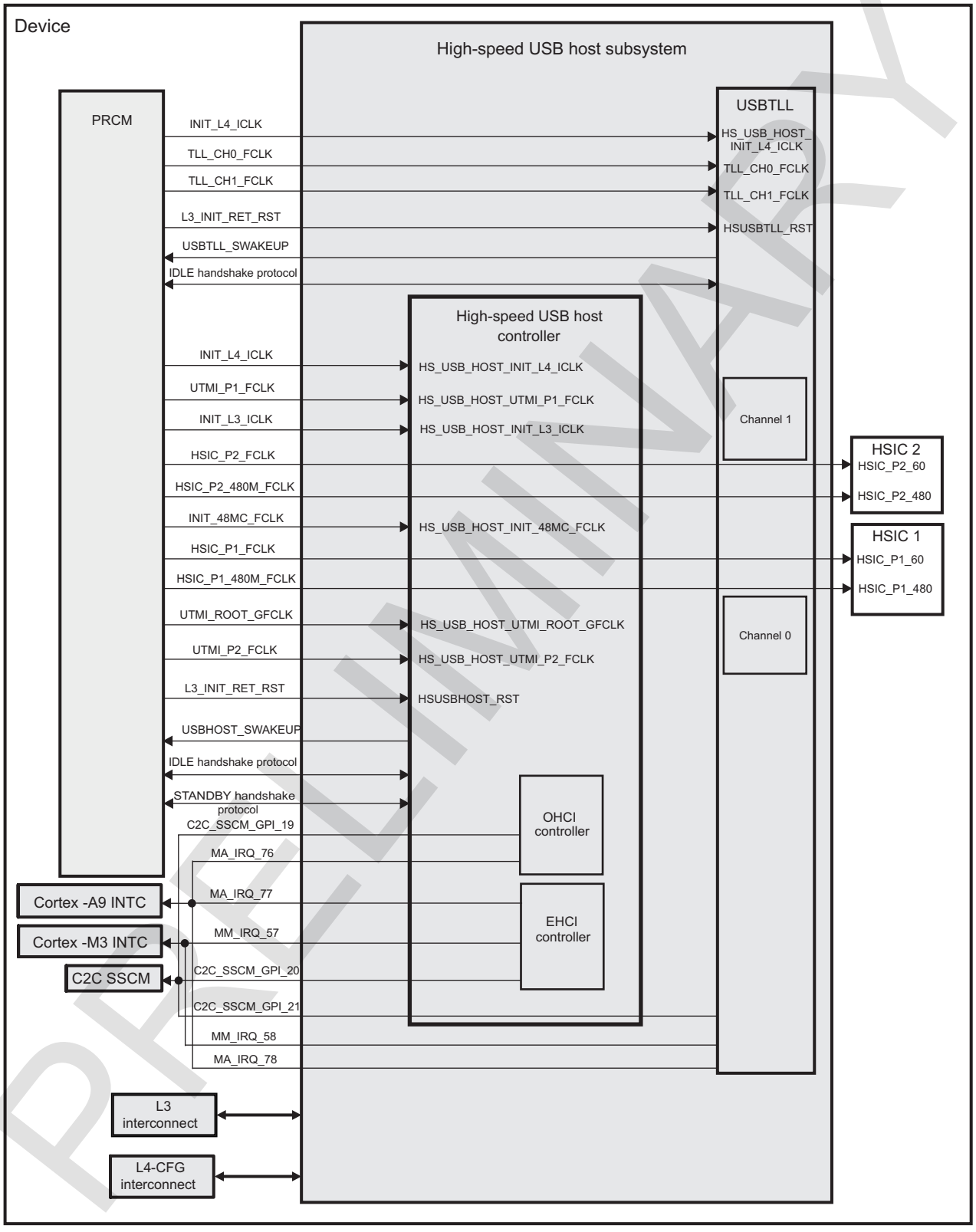

Table 23-940 through Table 23-942 summarize the integration of the module in the device.

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Table 23-940. Integration Attributes

Module Instance	Attributes	
	Power Domain	Interconnect
HSUSBHOST	PD_L3_INIT	L3 L4_CFG
HSUSBTLL	PD_L3_INIT	

Table 23-941. Clocks and Resets

Clocks

Module Instance	Destination Signal Name	Source Signal Name	Source	Description
HSUSBHOST	HS_USB_HOST_INIT_L4_ICLK	INIT_L4_ICLK	PRCM	L4 interconnect enable signal for the slave interface on L4 (see)
	HS_USB_HOST_INIT_L3_ICLK	INIT_L3_ICLK	PRCM	L3 interconnect clock for the L3 master port interface (see)
	HSIC_P2_480	HSIC_P2_480M_FCLK	PRCM	480-MHz clock for the USB HSIC (see)
	HS_USB_HOST_UTMI_P1_FCLK	UTMI_P1_FCLK/usbb1_ulpiphy_clk	PRCM/external PHY IC	Port 1 UTMI interface functional clock (see and)
	HSIC_P1_60	HSIC_P1_FCLK	PRCM	60-MHz clock for the USB HSIC (see)
	HSIC_P1_480	HSIC_P1_480M_FCLK	PRCM	480-MHz clock for the USB HSIC (see)
	HS_USB_HOST_INIT_48MC_FCLK	INIT_48MC_FCLK	PRCM	48-MHz functional clock for OHCI and EHCI (see)
	HSIC_P2_60	HSIC_P2_FCLK	PRCM	60-MHz clock for the USB HSIC (see)
	HS_USB_HOST_UTMI_ROOT_GFCLK	UTMI_ROOT_GFCLK	PRCM	60-MHz root hub clock (see)
	HS_USB_HOST_UTMI_P2_FCLK	UTMI_P2_FCLK/usbb2_ulpiphy_clk	PRCM/external PHY IC	Port 2 UTMI interface functional clock (see and)
HSUSBTLL	HS_USB_HOST_INIT_L4_ICLK	INIT_L4_ICLK	PRCM	L4 interconnect enable signal for the slave interface on L4 (see)
	TLL_CH0_FCLK	TLL_CH0_FCLK	PRCM	Functional clock for channel 0 (see)
	TLL_CH1_FCLK	TLL_CH1_FCLK	PRCM	Functional clock for channel 1 (see)

Resets

Module Instance	Destination Signal Name	Source Signal Name	Source	Description
HSUSBHOST	HSUSBHOST_RST	L3_INIT_RET_RST	PRCM	The signal resets the HSUSBHOST module.
HSUSBTLL	HSUSBTLL_RST	L3_INIT_RET_RST	PRCM	The signal resets the HSUSBTLL module.

Table 23-942. Hardware Requests

Interrupt Requests

Module Instance	Source Signal Name	Destination Signal Name	Destination	Description
HSUSBHOST	HSUSB_EHCI_IRQ	MA_IRQ_77	Cortex-A9 INTC	Destination is Cortex-A9 interrupt controller (INTC).
	HSUSB_OHCI_IRQ	MA_IRQ_76	Cortex-A9 INTC	Destination is Cortex-A9 INTC.
	HSUSB_EHCI_IRQ	MM_IRQ_57	Cortex-M3 INTC	Destination is Cortex-M3 INTC.
	HSUSB_OHCI_IRQ	C2C_SSCM_GPI_19	C2C SSCM	Destination is C2C SSCM.
	HSUSB_EHCI_IRQ	C2C_SSCM_GPI_20	C2C SSCM	Destination is C2C SSCM.
HSUSBTLL	HSUSB_TLL_IRQ	MA_IRQ_78	Cortex-A9 INTC	Destination is Cortex-A9 INTC.
	HSUSB_TLL_IRQ	MM_IRQ_58	Cortex-M3 INTC	Destination is Cortex-M3 INTC.
	HSUSB_TLL_IRQ	C2C_SSCM_GPI_21	C2C SSCM	Destination is C2C SSCM.

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The HS USB host controller and TLL module are attached to the L3_INIT_RET_RST reset domain. The L3_INIT_RET_RST signal resets the HS USB host controller and TLL module (see Chapter 3, *Power, Reset, and Clock Management*).

23.11.4 HS Multiport USB Host Subsystem Functional Description

This section describes the functionality of the HS USB host subsystem by describing the HS USB host controller, USBTLL module.

23.11.4.1 USB Host Controller Functionality

The full details of the standard OHCI and EHCI host controller APIs (implemented by the current module) are not repeated here. For more information, see the following specifications:

- *Open Host Controller Interface (OHCI) Specification for USB Release 1.0a*
- *Enhanced Host Controller Interface (EHCI) Specification for USB Release 1.1*

Figure 23-252 is an overview of the HS USB host controller internal architecture. It contains two independent, 3-port host controllers (OHCI and EHCI) that operate in parallel; however, only two physical ports are mapped in the device processor.

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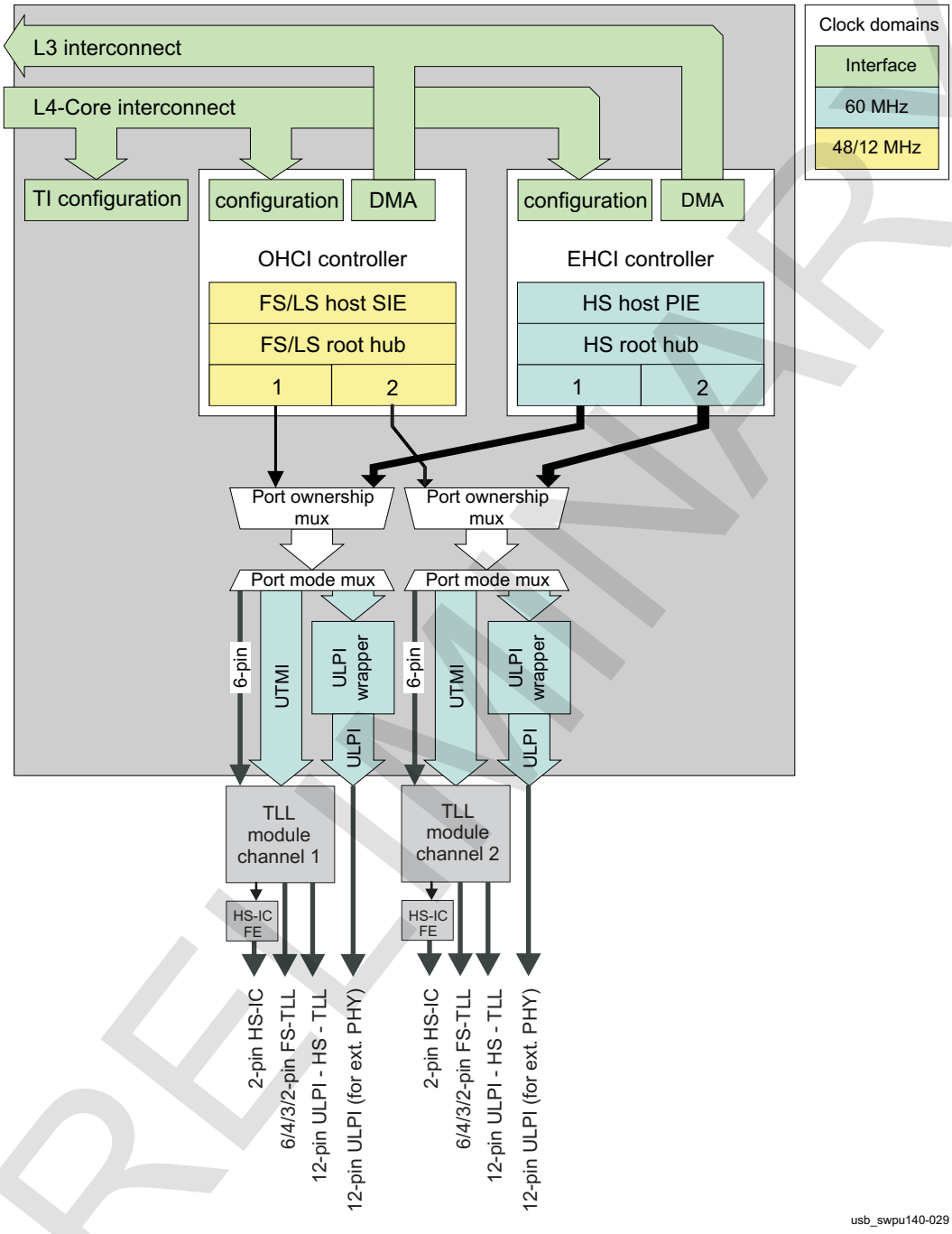
Figure 23-252. HS USB Host Controller Architecture



23.11.4.1.1 HS USB Host Controller Software Reset

The HS USB host controller has its own software-reset function through the UHH_SYSCONFIG[0] SOFTRESET bit. Setting this bit to 0x1 resets the HS USB host controller. The bit value of 0x1 remains until the reset completes. When the software reset completes, the SOFTRESET bit is automatically set to 0x0 and has the same effect as the hardware reset.

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23.11.4.1.2 HS USB Host Controller Power Management

The USB protocol defines power-saving modes, where clocks can be shut down. The host asynchronously detects ULPI/UTMI events and asserts the wake-up output, which causes the clocks to restart.

To reduce dynamic power consumption, an efficient idle scheme in the device is based on:

- Efficient local autoclock gating for each module
- Implementation of control sideband signals between the PRCM module and each module

This enhanced idle control allows clocks to be activated and deactivated safely without complex software intervention. In both cases, the HS USB host controller power management is applied only to the interface clock domain.

The HS USB host controller has master (initiator) and slave (target) interfaces:

- As an initiator, the HS USB host controller implements the standby handshake protocol to inform the PRCM module when it enters standby mode and does not generate traffic on the interconnect.
- As a target, the HS USB host controller implements the IDLE handshake protocol to allow the PRCM module requiring it to enter idle mode.

23.11.4.1.2.1 Standby Handshake Protocol

The HS USB host controller can go into standby mode, in which case it stops generating transactions on the interconnect. To save power, the module standby leads the PRCM module to disable the USB clocks.

The HS USB host controller has an Mstandby/Mwait handshake mechanism with the PRCM module (see Chapter 3, *Power, Reset, and Clock Management*).

The module is ready to enter standby mode (indicated by the Mstandby signal to the PRCM module asserted) when there is no USB activity and the module is idle. It means:

- The module is committed not to start any new transaction on its master interface.
- The whole module is idle and, therefore, the power manager can start the procedure to turn off the interface clock, if needed. This procedure must be implemented using the slave power-management protocol.

The handshake mechanism lets the module go into standby mode based on the UHH_SYSCONFIG[5:4] STANDBYMODE bit field.

Table 23-943 lists the settings of standby mode.

Table 23-943. HS USB Host Controller Standby Mode Settings

MIDLEMODE Value	Selected Mode	Description
0x0	Force-standby	The HS USB host controller enters standby mode unconditionally (Mstandby is asserted unconditionally).
0x1	No-standby	The HS USB host controller never enters standby mode (Mstandby is never asserted).
0x2	Smart-standby	The HS USB host controller is ready to enter standby mode (Mstandby is asserted) when there is no more activity on the USB master interface of the interconnect.
0x3	Smart-standby + wakeup	The HS USB host controller enters smart mode with asynchronous (master) wakeup enabled.

23.11.4.1.2.2 IDLE Handshake Protocol

The PRCM module handles an IDLE handshake protocol for the HS USB host controller. The IDLE handshake protocol lets the PRCM module requiring the HS USB host controller to enter idle mode. Although this handshake is completely hardware and out of any software control, the way in which the HS USB host controller acknowledges the PRCM IDLE request is configurable through the UHH_SYSCONFIG[3:2] SIDLEMODE bit field. Table 23-944 lists the settings of SIDLEMODE and the related acknowledgment modes.

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Table 23-944. HS USB Host Controller SIDLEMODE Settings

SIDLEMODE Value	Selected Mode	Description
0x0	Force-idle	The HS USB host controller acknowledges unconditionally the IDLE request from the PRCM module, regardless of its internal operations. Because such a mode does not prevent the loss of data when the clock is switched off, the mode must be used carefully.
0x1	No-idle	The HS USB host controller never acknowledges any IDLE request from the PRCM module. This mode is safe from a module point of view because it ensures the clocks remain active; however, it is not efficient from a power-saving perspective because it does not allow the PRCM output clock to be shut off, and thus the power domain to be set to a lower power state.
0x2	Smart-idle	The HS USB host controller acknowledges the IDLE request basing its decision on its internal activity. Namely, the acknowledge signal is asserted only when all pending transactions, IRQs, or DMA requests are treated. This is the best approach for an efficient system power management.
0x3	Smart-idle + wakeup	The HS USB host controller enters smart mode with asynchronous (master) wakeup enabled.

23.11.4.1.2.3 Wake-Up Request

The wake-up request signal USBHOST_SWAKEUP is generated by the HS USB host controller to the PRCM module.

23.11.4.1.3 HS USB Host Controller Save and Restore

The hardware context of the USB HS host can be frozen, saved, and restored.

The SAR mechanism extracts the hardware context of the HS USB host controller (after all USB activity is suspended) before switching off (saving), saves it to an external always-on memory, and reinjects it later after the module is switched on again and reset (restored) seamlessly for the USB. For more information, see Chapter 3, *Power, Reset, and Clock Management*.

23.11.4.1.4 HS USB Host Controller Port Status

The USB port status is given through the UHH_HOSTCONFIG[8] P1_CONNECT_STATUS and UHH_HOSTCONFIG[9] P2_CONNECT_STATUS bits. The default value of these bits is 0x0 indicating that peripheral is disconnected.

23.11.4.1.5 HS USB Host Controller Burst Control

To avoid buffer underflow, bursts must be enabled by setting the UHH_HOSTCONFIG[4:2] bit field to 0x7, and the UHH_HOSTCONFIG[5] ENA_INCR_ALIGN bit to 1.

23.11.4.1.6 OHCI Implementation Specifications

Some features of the OHCI API are optional and/or implementation-specific. The choices made in the current implementation, the HS USB host controller, are described in the following list and are reflected in the register descriptions (see Section 23.11.6.5, *OHCI Registers*). For all standard features, see the *Open Host Controller Interface (OHCI) Specification for USB Release 1.0a*.

- HCFMINTERVAL[30:16] FSMPS bit field (FullSpeedMaxPacketSize) = 0x0000: The host stops scheduling new packets 0 bit times before the end of the frame (that is, by default, there is no scheduling overrun protection). To be updated by the software driver.
- HCRHDESCRIPTORA[7:0] NDP bit field (NumberDownstreamPorts) = 0x03 = three ports
- HCRHDESCRIPTORA[9] NPS bit (NoPowerSwitching) = 0: Ports are power-switched by default.
- HCRHDESCRIPTORA[8] PSM bit (PowerSwitchingMode) = 1: Per-port power switching is supported, although PPCM default setup has all ports controlled globally.
- HCRHDESCRIPTORA[31:24] POTPG bit field (PowerOnToPowerGood) = 0x0A = 10: Power ramp-up time is 10 x 2 ms = 20 ms.
- HCRHDESCRIPTORB[15:0] DR bit field (DeviceRemovable) = 0x0000: By default, no nonremovable devices (that is, devices attached to any of the ports) are removable.

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- HCRHDESCRIPTORB[31:16] PPCM bit field (PortPowerControlMask) = 0x0000: By default, all ports are affected only by global power control.

23.11.4.1.7 UTMI Interface

The host controller supports two ports. Each host controller port is configured to be in UTMI or ULPI mode (see the UHH_HOSTCONFIG[21:16] Px_MODE bit field).

In UTMI mode, a port has its UTMI signal set broadcasting the outgoing packets (from the host to the peripherals) and gathering the incoming ones (from the addressed peripheral to the host). ULPI signals for that port are undefined/don't care on all ports.

The UTMI ports between the HS USB host controller and the USBTLL module are on-chip and remain invisible.

UTMI transparent mode is used to connect with the HSIC, (see the UHH_HOSTCONFIG[17:16] P1_MODE or UHH_HOSTCONFIG[17:16] P2_MODE bit fields).

23.11.4.1.8 ULPI Interface

The host supports two ports. Each host controller port is configured to be either in UTMI or in ULPI mode (see the UHH_HOSTCONFIG[17:16] P1_MODE or UHH_HOSTCONFIG[17:16] P2_MODE bit fields).

In ULPI mode, a port has its ULPI signal set broadcasting the outgoing packets (that is, from the host to the peripherals) and gathering the incoming packets (that is, from the addressed peripheral to the host). UTMI signal sets are undefined/don't care on all ports.

NOTE: The ULPI clock (part of the 12-wire ULPI interface) is expected to be routed by the system from the ULPI CLK input I/O pad to the clock input used by all HS modes (ULPI and UTMI) for the current port.

23.11.4.2 USBTLL Module Functionality

23.11.4.2.1 USBTLL Software Reset

Writing 0x1 to the USBTLL_SYSCONFIG[1] SOFTRESET bit resets the USBTLL module. The bit value of 0x1 remains until the reset completes. When the software reset completes, the SOFTRESET bit is automatically set to 0x0 and has the same effect as the hardware reset.

23.11.4.2.2 USBTLL Power Management

The USB protocol defines power-saving modes, where clocks can be shut down.

23.11.4.2.2.1 IDLE Handshake Protocol

The PRCM module handles an IDLE handshake protocol for the USBTLL module. The IDLE handshake protocol lets the PRCM module require the HS USBTLL module to enter idle mode.

The way in which the HS USBTLL module acknowledges the PRCM IDLE request is configurable through the USBTLL_SYSCONFIG[4:3] SIDLEMODE bit field. Table 23-945 lists related acknowledgment modes.

Table 23-945. HS USBTLL Module SIDLEMODE Settings

SIDLEMODE Value	Selected Mode	Description
0x0	Force-idle	The HS USB host controller acknowledges unconditionally the IDLE request from the PRCM module, regardless of its internal operations.
0x1	No-idle	The HS USB host controller never acknowledges any IDLE request from the PRCM module.
0x2	Smart-idle	The HS USB host controller acknowledges the IDLE request, basing its decision on its internal activity.

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23.11.4.2.3 USBTLL Save and Restore

The SAR mechanism extracts the hardware context of the USBTLL module (after all USB activity is suspended) before switching off (saving), saves it to an external always-on memory, and reinjects it later after the module is switched on again and reset (restored) seamlessly for the USB.

Hardware context of the USBTLL module is accessed through the USBTLL_SAR_CNTX_i[31:0] CNTX bit field.

The PRCM module enables the SAR mechanism for the USBTLL module. When set, the PRM module initiates the save and/or the restore sequences at the appropriate time. When not set, the USB host is treated as a standard module, and the save/restore sequences do not occur.

For more information, see .

Table 23-946 lists the USBTLL registers affected by the SAR context.

NOTE: Because all addresses give access to the same physical register (that is, to the same piece of context), the ULPI registers with multiple accesses (write, set, clear) are listed only once in the table.

Table 23-946. USBTLL Registers Affected by the SAR Context

Register Name	Comments on SAR Policy
USBTLL_SYSCONFIG	Except the SOFTRESET bit (write-only)
USBTLL_IRQENABLE	–
TLL_SHARED_CONF	Except the FCLK_REQ bit
TLL_CHANNEL_CONF_i	Except the FSLSLINESTATE bit field
FUNCTION_CTRL_i	–
INTERFACE_CTRL_i	–
OTG_CTRL_i	–
USB_INT_EN_RISE_i	–
USB_INT_EN_FALL_i	–
USB_INT_STATUS_i	–

23.11.4.2.4 USBTLL Channels and Ports

Following the same convention as UTMI and ULPI, the current specification is consistently PHY-centric (that is, directions are always given with respect to the transceiver emulated here by the TLL, and not with respect to the link controller): An input goes from the link controller to the TLL (transceiver emulator) (that is, it is an input for the USBTLL module). Reciprocally, an output goes from the TLL (transceiver) to the link controller (that is, it is an output for the USBTLL module).

By convention, the local link controller is the controller integrated on the same IC as the USBTLL module: This is the HS USB host controller in the device. The remote link controller is the other controller, located off-chip (that is, on another IC). One controller is always the USB host, the other is the USB peripheral, and they communicate through the USBTLL module.

A channel is defined as a independent USB path through the USBTLL module, which always converts the UTMI+ transceiver interface protocol coming from the local link controller (the HS USB host controller in the device). There are two channels of the USBTLL module in the device.

A USB port is a set of I/O signals that carry the data and control information from/to a USB line. Several port formats exist, with different capabilities. A channel has three ports. If the channel is active, two ports are active at the same time, depending on the configuration of the channel. The mode remains static throughout the USB operation.

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23.11.4.2.5 USBTLL Channel Configuration

A channel configuration is a set of software settings that specifies the connection of two of the channel ports through the USBTLL module. USB data and control injected on one side (or port) comes out on the other side (or port) after a certain amount of processing, depending on the mode. Table 23-947, lists the modes.

All configurations connect the PHY UTMI port (attached to the HS USB host controller) to one of the other two ports (attached to a variety of transceivers or controllers on the pad side).

Table 23-947 describes the available modes and the software settings required for each. Channel i has the following settings:

- CHANMODE: TLL_CHANNEL_CONF_i[2:1] CHANMODE bit field
- FSLSMODE: TLL_CHANNEL_CONF_i[27:24] FSLSMODE bit field
- FSLSSERIALMODE_3PIN/6PIN: Either the ULPI PHY-side INTERFACE_CTRL_i[1] FSLSSERIALMODE_3PIN bit or the INTERFACE_CTRL_i[0] FSLSSERIALMODE_6PIN bit (only one at a time can be set to 1)

Table 23-947. USBTLL Channel Configuration

Configuration	Mode	CHANMODE	FSLSMODE	Other Settings	Ports	Speed	Remote Port Connection
1	UTMI transparent	0	N/A	–	A-B	–	UTMI transparent
2	ULPI synchronous TLL	0	N/A	FSLSSERIALMODE_3PIN/6PIN = 0	A-C	HFL	ULPI link (peripheral controller)
3	Serial UTMI to serial ULPI TLL	0	N/A	FSLSSERIALMODE_3PIN/6PIN = 1	A-C	FL	ULPI link (peripheral controller) supporting 3-/6-pin mode
4	Serial UTMI to serial TLL	1	0x4-0x7; 0xA-0xB	–	A-D	FL	Serial link (2-/3-/4-/6-pin)
4	Serial UTMI to serial PHY	1	0x0-0x3	–	A-D	FL	Serial transceiver (2-/3-/4-/6-pin)

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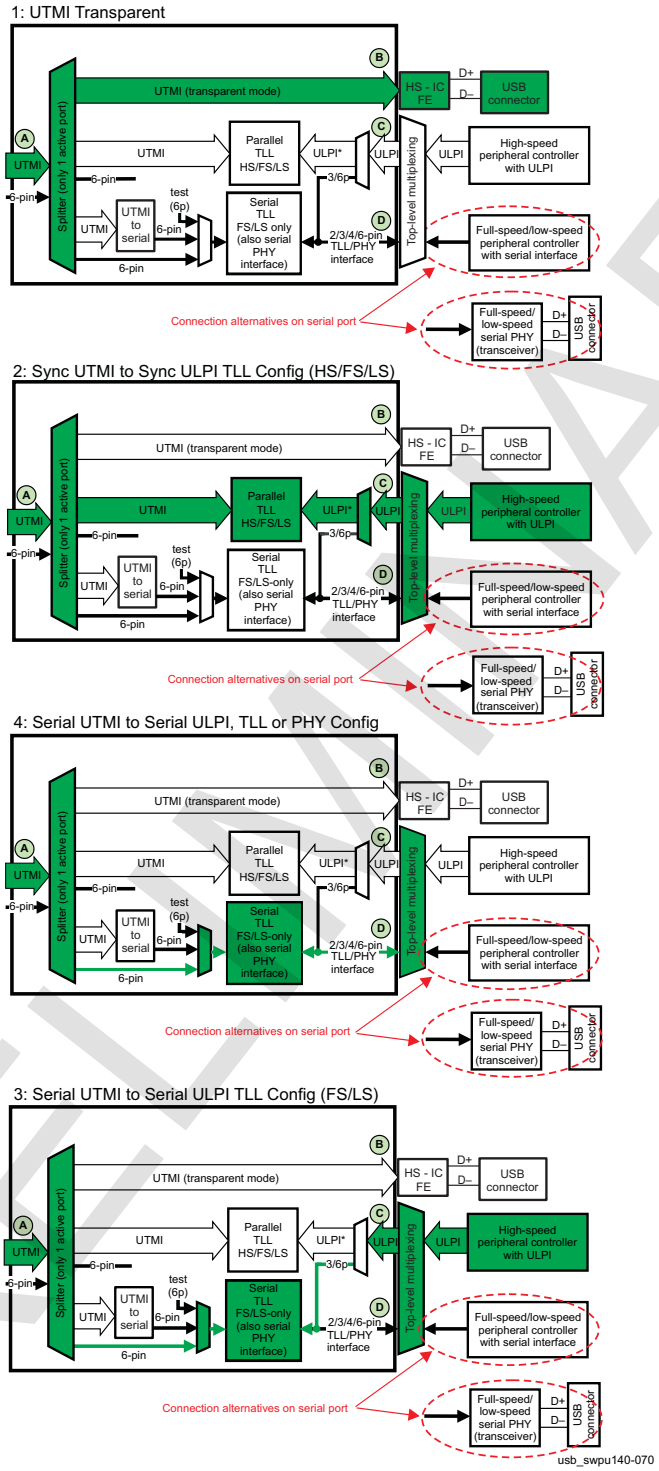
Figure 23-253. Per-Configuration Data Path Through USBTLL



23.11.4.2.6 USBTLL VBUS Management and Emulations

In transceiver configurations, a USB cable is present, including a 5-V VBUS supply line. On the other hand, in TLL configurations, the physical USB lines are emulated and have no physical existence. This is especially true for the VBUS line, which distributes the 5-V power provided by the default host (or A-device) to the entire bus. VBUS is also used for signaling purposes, and those features must be emulated:

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- A peripheral detects the presence of a host by detecting the presence of VBUS.
- USB OTG defines an elaborate voltage-sensing scheme to dynamically switch on and off VBUS (start and stop sessions). In the context of TLL, this brings no power savings compared to a simple suspend.
- In particular, USB OTG uses VBUS as a wake-up source (VBUS-pulsing SRP) for the default peripheral (or B-device).

For more information on how sideband controls are integrated, see Figure 23-238 and Figure 23-239 and the related explanations.

23.11.4.2.6.1 VBUS Control and Status for Transceiver (Non-TLL) Configurations

In non-TLL modes, VBUS exists, and the problem is to propagate control and status to and from the VBUS manager IC (typically, the transceiver).

Only serial transceiver configurations are concerned in the case of the HS USB host subsystem in the device.

23.11.4.2.6.1.1 VBUS Management in Serial Transceiver Configurations

VBUS management is not standardized in transceiver configurations. The chosen implementation is described in the following list (also see Figure 23-238).

- VBUS control required for host and OTG operation (VBUS drive, VBUS pullup "charge," VBUS pulldown "discharge") is assumed to be handled separately from the USBTLL module (that is, by software and straight to the power IC, which can be the transceiver, especially in OTG cases).
- The status of VBUS must be sampled by the appropriate hardware (again, most often the transceiver) and reported by software to the USBTLL module, using the TLL_CHANNEL_CONF_i[16] DRVVBUS and TLL_CHANNEL_CONF_i [15] CHRGVBUS bits, as indicated in Table 23-948.

Table 23-948 lists the values to write to the TLL_CHANNEL_CONF_i register depending on the status of VBUS observed by the transceiver on the VBUS line. The same register fields are also used in TLL configuration, and have been named according to that second configuration. In transceiver configurations, the signification of the fields is:

- DRVVBUS: Set to 1 to report a VBUS level greater than VBUS valid.
- CHRGVBUS: Set to 1 to report a VBUS level greater than session valid.

Table 23-948. VBUS Level Software Reporting for Serial Transceiver Configuration

VBUS Status	TLL_CHANNEL_CONF_i[16] DRVVBUS	TLL_CHANNEL_CONF_i[15] CHRGVBUS
VBUS valid	1	1
Session valid (A/B)	0	1
Session not valid	0	0
Session end	0	0

23.11.4.2.6.2 VBUS Emulation for TLL Configurations

The TLL VBUS emulation sums up all actions on the VBUS line and obtains a voltage level, which is reported in the VBUS status bits following the protocol. The level depends on the immediate VBUS actions and has no memory of previous levels, whereas an actual VBUS line behaves like an RC circuit and takes time to charge and discharge. This causes the following differences:

- The TLL level always jumps abruptly from session valid to session end (and back) with no transient time in between (where session is neither valid nor ended) as in real life.
- The charge feature is used for VBUS-pulsing SRP and is enabled long enough to go over the session valid threshold, but without reaching VBUS valid. In the TLL, the transition to session valid is immediate, and VBUS valid is never reached even if the charge is intentionally kept active.
- The discharge feature is used in real life to accelerate the voltage drop of an undriven VBUS toward the session-end level. For TLL, therefore, this is useless (although the UTMI input/ULPI register bit does exist, for compatibility), and is always don't care.

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23.11.4.2.6.2.1 VBUS Emulation in ULPI TLL Modes

Table 23-949 summarizes the VBUS emulation in ULPI TLL modes. VBUS controls are writable, static PHY-side registers on the ULPI side, and input signals on the ULPI ports (port A). VBUS status bits are read-only, volatile PHY-side registers on the ULPI, and output signals on the ULPI ports (port A).

Table 23-949. Emulation of VBUS Levels for UTMI-to-ULPI TLL Mode

VBUS Controls (Actions)			VBUS Level	VBUS Status		
OTG_CTRL_i[5] DRVVBUS	OTG_CTRL_i[4] CHRGVBUS	OTG_CTRL_i[3] DISCHRGVBUS		USB_INT_STATUS_i[1] VBUSVALID bit	USB_INT_STATUS_i[2] SESSVALID bit	USB_INT_STATUS_i[3] SESSEND bit
1	X	X	VBUS valid	1	1	0
0	1	X	VBUS valid	0	1	0
0	0	X	Session end	0	0	1

23.11.4.2.6.2.2 VBUS Emulation in Serial TLL Modes

In serial TLL modes, VBUS status and control is implemented with ad hoc sideband signals (see Figure 23-239).

VBUS control can be done in software by writing to the following fields of the TLL_CHANNEL_CONF_i register:

- DRVVBUS: Set to 1 to drive VBUS to 5 V (for A-device or host)
- CHRGVBUS: Set to 1 to pull up VBUS (for SRP)
- There is no pulldown (discharge) control, because the emulated VBUS has no latency and VBUS level goes to the session-end level as soon as it is neither driven nor pulled up.

Alternatively, VBUS drive can also be hardware-controlled through a dedicated input. (The DRVVBUS bit and input signal are ORed internally.)

VBUS status is available on dedicated output signals. If those outputs are not available at the top level, a software alternative is to use the voltage status reported on the interface (through the standard UTMI+ sideband signals) of the local controller (the HS USB host controller in the device) and to pass it to the remote controller (a peripheral controller) by means of an ad hoc software-controller interface other than the USB. This is based on the fact that the level of VBUS is the same on both extremities of the bus (that is, it does not matter which side does the measurement).

23.11.4.2.7 USBTLL Multimode Serial Port

The multimode serial port requires six bidirectional I/O pads to support all eight defined modes (selected in the TLL_CHANNEL_CONF_i[27:24] FSLSMODE bit field when field CHANMODE = 0x1 = UTMI-to-serial). Those modes are FS/LS only (that is, HS is not supported over a serial interface).

The pads are named TXEN, TXDAT, TXSE0, RXRCV, RXDP, and RXDM after their functionality in standard 6-pin mode (mode 0). Each pad has an input, output, and output-enable signal associated with it on the USBTLL entity.

Table 23-950 lists the function of each pad in each mode. USBTLL outputs are shown in yellow, inputs in blue, and bidirectional pads in green.

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Table 23-950. Serial Mode Description, Signal Functionality

Usual Name	6-Pin Mode	6-Pin Mode (Alt)	3-Pin Mode	4-Pin Mode	6-Pin TLL Mode	6-Pin TLL (Alt) Mode	3-Pin TLL Mode	4-Pin TLL Mode	2-Pin TLL Mode	2-Pin TLL (Alt) Mode
TLL_CHANNEL_CONF_i[27:24] FSLSMODE bit field	0x0	0x1	0x2	0x3	0x4	0x5	0x6	0x7	0xA	0xB
TX encoding	DAT/SE0	DP/DM	DAT/SE0	DP/DM	DAT/SE0	DP/DM	DAT/SE0	DP/DM	DAT/SE0	DP/DM
RX encoding	DP/DM/RCV	DP/DM/RCV	DAT/SE0	DP/DM/RCV	DP/DM/RCV	DP/DM/RCV	DAT/SE0	DP/DM/RCV	DAT/SE0	DP/DM
Pin use	Unidirectional	Unidirectional	Bidirectional	Bidirectional	Unidirectional	Unidirectional	Bidirectional	Bidirectional	Bidirectional	Bidirectional
Pin count	6	6	3	4	6 or 5[1]	6 or 5[1]	3	4 or 3[2]	2	2
I/O Pad Function Per Mode										
TXEN	TX Enable	TX Enable	TX Enable	TX Enable	TX Enable	TX Enable	TX Enable	TX Enable	N/C	N/C
TXDAT	TX Diff Data	TX SE Plus Data	TX/RX Diff Data	TX/RX SE Plus Data	TX Diff Data	TX SE Plus Data	TX/RX Diff Data	TX/RX Diff Data	TX/RX Diff Data	TX/RX SE Plus Data
TXSE0	TX force SE0	TX SE Minus Data	TX/RX force SE0	TX/RX SE Minus Data	TX force SE0	TX SE Minus Data	TX/RX force SE0	TX/RX force SE0	TX/RX force SE0	TX/RX SE Minus Data
RXRCV	RX Diff Data	RX Diff Data	N/C	RX Diff Data	RX Diff Data	RX Diff Data	N/C	RX Diff Data	N/C	N/C
RXDP	RX SE Plus Data	RX SE Plus Data	N/C	N/C	RX SE Plus Data	RX SE Plus Data	N/C	N/C	N/C	N/C
RXDP	RX SE Minus Data	RX SE Minus Data	N/C	N/C	RX SE Minus Data	RX SE Minus Data	N/C	N/C	N/C	N/C

(1) RXRCV and RXDP carry the same information: RXDP can drive both inputs of the remote controller, and RXRCV can be kept unused.
(2) Same remark for TXDAT (for outputs) and RXRCV: TXDAT only is enough.

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23.11.4.2.8 USBTLL Attach/Connect Emulation for Serial Modes

This section applies to all serial TLL modes in the following circumstances:

- In UTMI-to-serial mode (TLL_CHANNEL_CONF_i[2:1] CHANMODE = 0x1) for all TLL values of the TLL_CHANNEL_CONF_i[27:24] FSLSMODE bit field (0x4–0x7; 0xA–0xB)
- In UTMI-to-ULPI TLL mode (TLL_CHANNEL_CONF_i[2:1] CHANMODE = 0x0) when the ULPI bus is switched to 6-pin or 3-pin serial modes

In those modes, the USB bus lines are emulated by USBTLL internal logic and are never available on the outside. The pullup/pulldown actions described in the USB specification cannot be applied directly, and the USB cable cannot be physically attached.

Because serial modes do not specify a standard format for those sideband settings, a custom software-controlled one is implemented:

- The TLL_CHANNEL_CONF_i[4] TLLATTACH bit emulates the physical attachment of the two controllers through a TLL cable:
  - When this bit is cleared, the local controller RX path shows only the local controller (the HS USB host controller) actions on the bus: TX driving, pullups, pulldowns. The same applies for the remote controller RX path (except that test override is not available).
  - When the bit is set, the actions of both sides are applied to the same bus and are resolved, similar to a real bus. The RX path for both sides shows the same bus state.
- The TLL_CHANNEL_CONF_i[5] TLLCONNECT bit emulates the USB electrical connect (that is, the pullup by the USB peripheral of one of the two USB lines [by a 1.5-kΩ resistor]), which causes the line state to transition from SE0 to J, which is detected by the USB host. The register bit is ORed with a USBTLL module input signal; the connect control can be software (L4_CFG interconnect write access) or hardware (input level). The speed of the connection is determined by the TLLFULLSPEED bit.
- The TLL_CHANNEL_CONF_i[6] TLLFULLSPEED bit determines the speed (full or low) of the USB connect to be emulated. The connect enable (controlled as previously defined) results in the pulling up of D+ (1 = full speed) or D– (0 = low speed) (see Table 23-951).
- The 15-kΩ pulldowns are implicit: Because they are supposed to be turned on at least on the host side of the bus, they do not require additional control.

NOTE: Sideband control and status actions such as pullups are included in parallel (that is, nonserial) standards (UTMI, ULPI), and do not require custom additions.

Table 23-951. Pullup Enable Emulation in Serial TLL Modes

TLL_CHANNEL_CONF_i Fields		Input Signal	Resulting TLL Pullup Emulation	
TLLFULLSPEED	TLLCONNECT	USB State	D+ Pullup	D– Pullup
1	0	Full-speed unconnected	Off	Off
1	1	Full-speed connected	On	Off
0	0	Low-speed unconnected	Off	Off
0	1	Low-speed connected	Off	On

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23.11.5 HS Multiport USB Host Subsystem Low-Level Programming Model

This section describes the low-level hardware programming sequences for the configuration and use of the HS USB host subsystem.

23.11.5.1 Global Initialization

23.11.5.1.1 Surrounding Modules Global Initialization

This section identifies the requirements for initializing the surrounding modules when the HS USB host subsystem is used for the first time after a device reset. This initialization of surrounding modules is based on the integration of the HS USB host subsystem.

Table 23-952 describes the global initialization of surrounding modules.

Table 23-952. Global Initialization of Surrounding Modules

Surrounding Modules	Comments
PRCM	All clocks must be enabled. See , *CM Clock Source*.
Cortex-A9 MPU INTC or Cortex-M3 MPU INTC	The Cortex-A9 MPU or Cortex-M3 MPU INTC must be configured to enable the interrupt request generation to the Cortex-A9 MPU or Cortex-M3 MPU subsystem when interrupt requests are generated by the HS multiport USB host subsystem. See the respective functional description in Chapter 17, *Interrupt Controller*, for the MPUs.
Interconnect (L3 and L4)	For more information, see Section 13.2, *L3 Interconnect*, and Section 13.3, *L4 Interconnect*.

23.11.5.1.2 HS Multiport USB Host Subsystem Global Initialization

This procedure in Table 23-953 initializes the HS multiport USB host subsystem after a power-on or software reset.

Table 23-953. HS Multiport USB Host Subsystem Global Initialization

Step	Register/Bit Field/Programming Model	Value
Perform a software reset on the TLL module.	USBTLL_SYSCONFIG[1] SOFTRESET	0x1
Wait until reset is finished.	USBTLL_SYSSTATUS[0] RESETDONE	=0x1
Enable IRQ event for the TLL module.	USBTLL_IRQENABLE[1] FCLK_END_EN	0x1
Enable IRQ event for the TLL module.	USBTLL_IRQENABLE[0] FCLK_START_EN	=0x1
Perform a software reset on the HS USB controller.	UHH_SYSCONFIG[0] SOFTRESET	0x1
Wait until the EHCI HS host is out of reset.	UHH_SYSSTATUS[2] EHCI_RESETDONE	=0x0
Wait until the OHCI HS host is out of reset.	UHH_SYSSTATUS[1] OHCI_RESETDONE	=0x0
Enable IRQ event for the OHCI HS host.	HCINTERRUPTENABLE[31] MIE	0x1
Enable IRQ event for the EHCI HS host.	USBINTR[0] USBIE	0x1

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23.11.5.2 Operational Modes Configuration (Selecting and Configuring USB Connectivity)

Figure 23-254 shows how to select and configure the HS USB host subsystem connectivity.

Figure 23-254. Selecting and Configuring HS USB Host Subsystem Connectivity

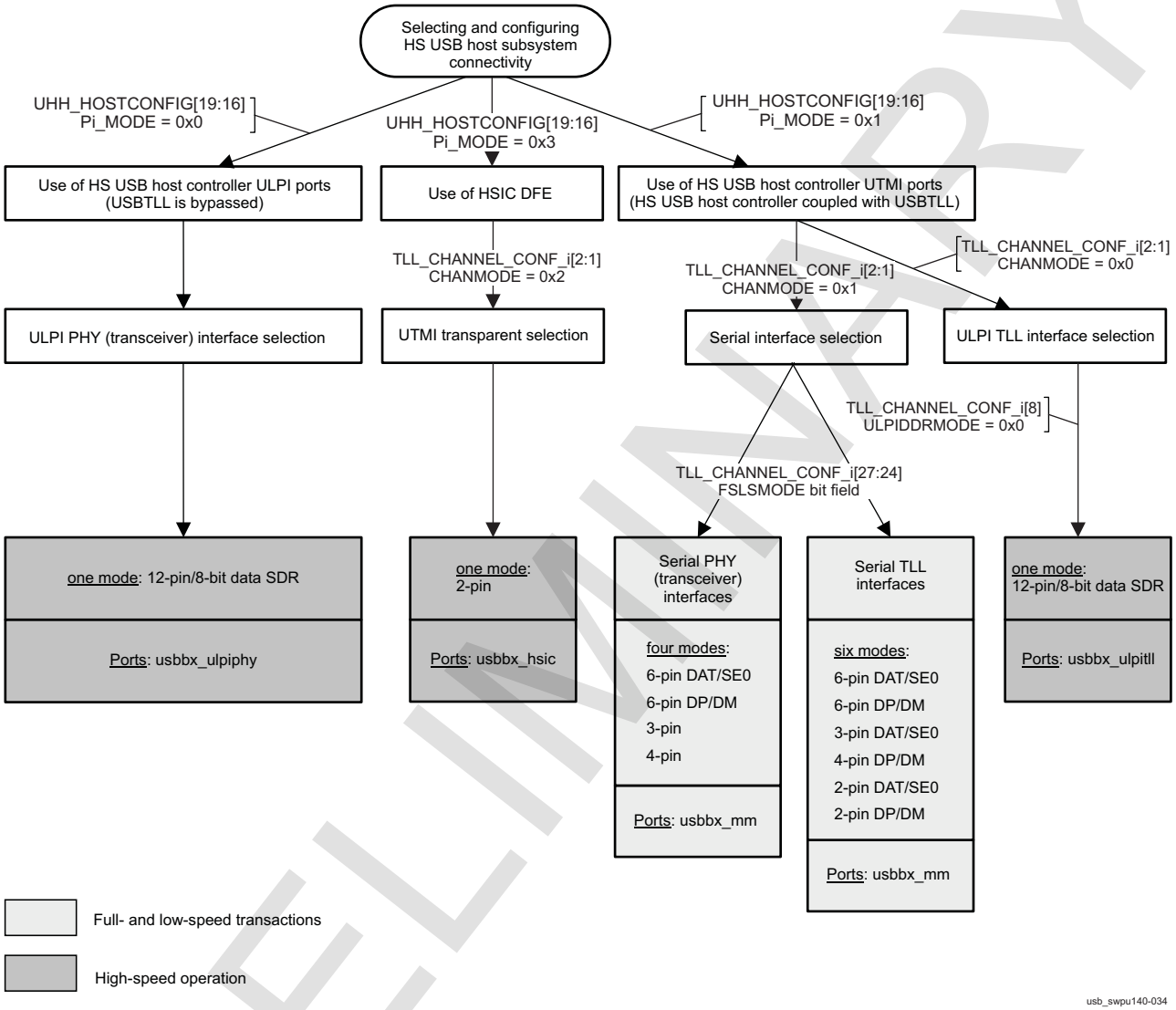

Table 23-954. Register Call Summary for Selecting and Configuring High-Speed USB Host Subsystem Connectivity

Register Name	
UHH_HOSTCONFIG	TLL_CHANNEL_CONF_i

23.11.5.3 USBTLL Registers

The USBTLL module contains two types of software-programmable registers: TLL control and status registers and ULPI PHY-side registers.

23.11.5.3.1 TLL Control and Status Registers

These 32-bit registers configure the various channels. These registers are accessed by the MPU through the L4_CFG interconnect. They are used primarily before USB activity starts. The registers are:

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- OCP-standard registers for revision number, IRQ, clocking management, etc.
- TLL-specific registers

23.11.5.3.2 ULPI PHY-Side Registers

Each TLL channel emulates a ULPI transceiver and therefore contains this set of 8-bit PHY-side registers, per ULPI specification. The registers are:

- All ULPI-mandatory standard registers and fields
- A selection of ULPI-optional standard registers and fields, when relevant to the TLL context
- Vendor-specific registers, mapped at the addresses specified for that purpose in the ULPI specification

These registers are accessed by the external (that is, off-chip) link controller over the ULPI port of each channel, in the 0x100-byte ULPI address space, using the ULPI register access protocol.

They are accessible by the L4_CFG interconnect: The ULPI register sets of all channels are mapped side by side in the upper part of the L4_CFG interconnect address space, where they can be accessed through byte accesses. If a conflict occurs between the two access modes, access over ULPI has priority, but both accesses eventually complete correctly. For normal USB activity, all register accesses are expected to go over ULPI, and register changes caused by L4_CFG interconnect accesses can compromise proper USB operation. The L4_CFG interconnect access port is intended for:

- Miscellaneous test and debug
- Nonintrusive observation of ongoing USB operations (test)
- Context restore: During USB suspend periods, the USBTLL module can be switched off to save power. When the module is switched on again, the ULPI register contents, which have been lost, can be restored over the L4_CFG interconnect before USB operations restart, provided they were saved elsewhere beforehand.

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23.11.6 HS USB Host Subsystem Register Manual

This section provides the register description of the module.

23.11.6.1 USB_Host_HS Instance Summary

Table 23-955 summarizes the USB_Host_HS instance.

Table 23-955. USB_Host_HS Instance Summary

Module Name	L4_CFG Base Address	Size
USBTLLHS_config	0x4A06 2000	2KB
USBTLLHS_ULPI	0x4A06 2800	2KB
HSUSBHOST	0x4A06 4000	2KB
OHCI	0x4A06 4800	1KB
EHCI	0x4A06 4C00	1KB

23.11.6.2 USBTLLHS_config Registers

23.11.6.2.1 USBTLLHS_config Register Summary

Table 23-956 summarizes the USBTLLHS_config register mapping.

Table 23-956. USBTLLHS_config Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	Physical Address
USBTLL_REVISION	R	32	0x0000 0000	0x4A06 2000
USBTLL_HWINFO	R	32	0x0000 0004	0x4A06 2004
USBTLL_SYSCONFIG	RW	32	0x0000 0010	0x4A06 2010
USBTLL_SYSSTATUS	R	32	0x0000 0014	0x4A06 2014
USBTLL_IRQSTATUS	RW	32	0x0000 0018	0x4A06 2018
USBTLL_IRQENABLE	RW	32	0x0000 001C	0x4A06 201C
TLL_SHARED_CONF	RW	32	0x0000 0030	0x4A06 2030
TLL_CHANNEL_CONF_i (1)	RW	32	0x0000 0040 + (0x4 * i)	0x4A06 2040 + (0x4 * i)
USBTLL_SAR_CNTX_j (2)	RW	32	0x0000 0400 + (0x4 * j)	0x4A06 2400 + (0x4 * j)

(1) i = 0 or 1
(2) j = 0 to 6

CAUTION

The USBTLLHS_config registers are limited to 32-bit data accesses; 16-bit and 8-bit accesses are not allowed and can corrupt register content.

23.11.6.2.2 USBTLLHS_config Register Description

Table 23-957 through Table 23-973 describe the USBTLLHS_config registers.

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Table 23-957. USBTLL_REVISION

Address Offset	0x0000 0000		
Physical Address	0x4A06 2000	**Instance**	USBTLLHS_config
Description	OCP standard revision number, BCD encoded		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	Revision number	R	Ti internal data

Table 23-958. Register Call Summary for Register USBTLL_REVISION

High-Speed Multiport USB Host Subsystem

- USBTLLHS_config Register Summary: [0]

Table 23-959. USBTLL_HWINFO

Address Offset	0x0000 0004		
Physical Address	0x4A06 2004	**Instance**	USBTLLHS_config
Description	Information on hardware configuration of host		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								SAR_CNTX_SIZE							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED		R	0x000000
7:0	SAR_CNTX_SIZE	Save-and-Restore context size, in 32-bit words, i.e. number of 32-bit registers with significant context information, mapped from offset 0x400 upward.	R	0x07

Table 23-960. Register Call Summary for Register USBTLL_HWINFO

High-Speed Multiport USB Host Subsystem

- USBTLLHS_config Register Summary: [0]
- USBTLLHS_config Register Description: [1]

Table 23-961. USBTLL_SYSCONFIG

Address Offset	0x0000 0010		
Physical Address	0x4A06 2010	**Instance**	USBTLLHS_config
Description	OCP standard system configuration register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								CLOCKACTIVITY	RESERVED		SIDLEMODE		ENAWAKEUP	SOFTRESET	AUTOIDLE

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Bits	Field Name	Description	Type	Reset
31:9	RESERVED	Reserved	R	0x000000
8	CLOCKACTIVITY	Enable autogating of OCP-derived internal clocks while module is idle. 0x0: OCP-derived internal clocks OFF during idle 0x1: OCP-derived internal clocks ON during idle	RW	0
7:5	RESERVED	Reserved	R	0x0
4:3	SIDLEMODE	Slave interface power management control. Idle Req/ack control 0x0: Force-idle mode. Sidleack[1] asserted after Sidlereq assertion 0x1: No-idle mode. Sidleack[1] never asserted. 0x2: Smart-idle mode. Sidleack[1] asserted after Sidlereq assertion when no more activity on the OCP.	RW	0x0
2	ENAWAKEUP	Asynchronous wake-up generation control (Swakeup) 0x0: Wake-up generation disabled 0x1: Wake-up generation enabled	RW	0
1	SOFTRESET	Module software reset Write 0x0: No effect Write 0x1: Starts softreset sequence.	W	0
0	AUTOIDLE	Internal autogating control 0x0: Clock always running 0x1: When no activity on OCP, clock is cut off.	RW	1

Table 23-962. Register Call Summary for Register USBTLL_SYSCONFIG

High-Speed Multiport USB Host Subsystem

- USBTLL Software Reset: [0]
- USBTLL Power Management: [1]
- USBTLL Save and Restore: [2]
- HS Multiport USB Host Subsystem Global Initialization: [3]
- USBTLLHS_config Register Summary: [4]

Table 23-963. USBTLL_SYSSTATUS

Address Offset	0x0000 0014		
Physical Address	0x4A06 2014	**Instance**	USBTLLHS_config
Description	OCP standard system status register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															RESETDONE

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	RESETDONE	Indicates when the module has entirely come out of reset Read 0x0: Reset is ongoing Read 0x1: Reset is done	R	0

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Table 23-964. Register Call Summary for Register USBTLL_SYSSTATUS

High-Speed Multiport USB Host Subsystem

- HS Multiport USB Host Subsystem Global Initialization: [0]
- USBTLLHS_config Register Summary: [1]

Table 23-965. USBTLL_IRQSTATUS

Address Offset	0x0000 0018		
Physical Address	0x4A06 2018	**Instance**	USBTLLHS_config
Description	OCP standard IRQ status vector. Write 1 to clear a bit.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													ACCESS_ERROR	FCLK_END	FCLK_START

Bits	Field Name	Description	Type	Reset
31:3	RESERVED		R	0x0000 0000
2	ACCESS_ERROR	Access error to ULPI register over OCP: USB clock must run for that type of access to succeed. 0x0: No event pending 0x1: Event pending	RW	0
1	FCLK_END	Functional clock is no longer requested for USB clocking 0x0: No event pending 0x1: Event pending	RW	0
0	FCLK_START	Functional clock is requested for USB clocking 0x0: No event pending 0x1: Event pending	RW	0

Table 23-966. Register Call Summary for Register USBTLL_IRQSTATUS

High-Speed Multiport USB Host Subsystem

- USBTLLHS_config Register Summary: [0]
- USBTLLHS_config Register Description: [1] [2]

Table 23-967. USBTLL_IRQENABLE

Address Offset	0x0000 001C		
Physical Address	0x4A06 201C	**Instance**	USBTLLHS_config
Description	OCP standard IRQ enable vector		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													ACCESS_ERROR_EN	FCLK_END_EN	FCLK_START_EN

Bits	Field Name	Description	Type	Reset
31:3	RESERVED	Reserved	R	0x00000000
2	ACCESS_ERROR_EN	Enable IRQ generation upon access error to ULPI register over L3 interconnect 0x0: IRQ event is masked 0x1: IRQ event is enabled	RW	0x0
1	FCLK_END_EN	IRQ event mask for FCLK_END interrupt (see USBTLL_IRQSTATUS[1]) 0x0: IRQ event is masked 0x1: IRQ event is enabled	RW	0x0
0	FCLK_START_EN	IRQ event mask for FCLK_START interrupt (see USBTLL_IRQSTATUS[0]) 0x0: IRQ event is masked 0x1: IRQ event is enabled	RW	0x0

Table 23-968. Register Call Summary for Register USBTLL_IRQENABLE

High-Speed Multiport USB Host Subsystem

- USBTLL Save and Restore: [0]
- HS Multiport USB Host Subsystem Global Initialization: [1] [2]
- USBTLLHS_config Register Summary: [3]

Table 23-969. TLL_SHARED_CONF

Address Offset	0x0000 0030		
Physical Address	0x4A06 2030	**Instance**	USBTLLHS_config
Description	Common control register for all TLL channels		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														FCLK_REQ	FCLK_IS_ON

Bits	Field Name	Description	Type	Reset
31:2	RESERVED	Reserved	R	0x0000000
1	FCLK_REQ	Functional clock request, ORed from all channels depending on their respective USB bus state. Combined with the Fclk_is_on status to generate fclk_start/end IRQs. 0x0: Func clock input is not requested by TLL 0x1: Func clock input is requested by TLL	R	0x0

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Bits	Field Name	Description	Type	Reset
0	FCLK_IS_ON	Status of the functional clock input, provided by the system to the TLL module. The TLL module will only use that clock if the current status indicated that it is ready. Combined with the Fclk_request to generate fclk_start/end IRQs. 0x0: Functional clock input is not guaranteed ON (can actually be ON, OFF, or unstable) 0x1: Functional clock input is guaranteed ON and stable	RW	0x0

Table 23-970. Register Call Summary for Register TLL_SHARED_CONF

High-Speed Multiport USB Host Subsystem

- USBTLL Save and Restore: [0]
- USBTLLHS_config Register Summary: [1]

Table 23-971. TLL_CHANNEL_CONF_i

Address Offset	0x0000 0040 + (0x4 * i)	**Index**	i = 0 to 1
Physical Address	0x4A06 2040 + (0x4 * i)	**Instance**	USBTLLHS_config
Description	Control and Status register for channel i.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		FSLSLINESTATE		FSLSMODE				RESERVED			TESTTXSE0	TESTTXDAT	TESTTXEN	TESTEN	DRVVBUS	CHRGVBUS	RESERVED			ULPINOBITSTUFF	ULPIAUTOIDLE	UTMIAUTOIDLE	RESERVED	ULPIOUTCLKMODE	TLLFULLSPEED	TLLCONNECT	TLLATTACH	UTMIISADEV	CHANMODE		CHANEN

Bits	Field Name	Description	Type	Reset
31:30	RESERVED		R	0x0
29:28	FSLSLINESTATE	Line state for Full/low speed serial modes Bit 1 = D–/ Bit0 = D+ Read 0x0: Single-ended 0 Read 0x1: Full-Speed J = differential 1 Read 0x2: Full-Speed K = differential 0 Read 0x3: Single-ended 1 (illegal in USB)	R	0x0

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Bits	Field Name	Description	Type	Reset
27:24	FSLSMODE	Multiple-mode serial interface's mode select. Only when main channel mode is serial. No effect in other main modes. 0x0: 6-pin unidirectional PHY i/f mode. TX encoding is Dat/Se0 (default). 0x1: 6-pin unidirectional PHY i/f mode. TX encoding is Dp/Dm. 0x2: 3-pin bidirectional PHY i/f mode 0x3: 4-pin bidirectional PHY i/f mode 0x4: 6-pin unidirectional TLL mode. TX encoding is Dat/Se0. 0x5: 6-pin unidirectional TLL mode. TX encoding is Dp/Dm. 0x6: 3-pin bidirectional TLL mode 0x7: 4-pin bidirectional TLL mode 0xA: 2-pin bidirectional TLL mode. Encoding is Dat/Se0. 0xB: 2-pin bidirectional TLL mode. Encoding is Dp/Dm.	RW	0x0
23:21	RESERVED		R	0x0
20	TESTTXSE0	Force-Se0 transmit override value for serial mode test Don't care if TestEn = 0 (functional mode) or = TestTxen = 1 (TX = hiz) 0x0: drive differential value on TX according to TestTxDat 0x1: drive SE0 on TX	RW	0
19	TESTTXDAT	Differential data transmit override value for serial mode test Don't care if TestEn = 0 (functional mode) or = TestTxen = 1 (TX = hiz) or TestSe0 = 1 (TX = se0) 0x0: Drive full-speed K = differential 0 0x1: Drive full-speed J = differential 1	RW	0
18	TESTTXEN	Differential data transmit override value for serial mode test Don't care if TestEn = 0 (functional mode) 0x0: Drive Tx according to TestTxDat/Se0 0x1: Drive Tx Hiz (no drive: pullups determine line state)	RW	0
17	TESTEN	Enable manual test override for serial mode TX path (from local controller UTMI port) 0x0: No override. Tx is from local link controller 0x1: Override enabled	RW	0
16	DRVVBUS	VBUS-drive for ChanMode = serial * In TLL config, write 1 to emulate serial-side VBUS drive * In PHY config, write 1 to report "VBUS valid" status (of actual VBUS) to UTMI controller 0x0: VBUS not driven 0x1: VBUS driven to 5 V	RW	0
15	CHRGVBUS	VBUS-drive for ChanMode = serial * In TLL config, write 1 to emulate serial-side VBUS charge/pullup (OTG) * In PHY config, write 1 to reports "session valid" status (of actual VBUS) to UTMI controller 0x0: VBUS not charged, session not valid 0x1: VBUS charged, session valid	RW	0
14:12	RESERVED		R	0x0
11	ULPINOBITSTUFF	Disable bitstuff emulation in ULPI TLL for ULPI ChanMode 0x0: Bitstuff enabled, following USB standard 0x1: No bitstuff or associated delays (nonstandard)	RW	0

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Bits	Field Name	Description	Type	Reset
10	ULPIAUTOIDLE	For ChanMode = ULPI TLL only. Allow the ULPI output clock to be stopped when ULPI goes into asynchronous mode (low-power, 3-pin serial, 6-pin serial). No effect in ULPI input clock mode. 0x0: ULPI output clock always-on 0x1: ULPI output clock stops during asynchronous ULPI modes	RW	1
9	UTMIAUTOIDLE	For ChanMode = ULPI TLL only. Allow the UTMI clock (output) to be stopped when UTMII goes to suspended mode (suspendm = 0) 0x0: UTMI clock output always on 0x1: UTMI clock output gated upon suspend	RW	1
8	RESERVED		R	0
7	ULPIOUTCLKMODE	ULPI clocking mode select for ULPI TLL ChanMode. Hardcoded, for legacy only. Read 0x1: ULPI clock provided by PHY side (i.e. TLL, from functional clock). ULPI clock is output	R Rreturns 1s	1
6	TLLFULLSPEED	Sets PHY speed emulation in TLL (full/slow), which determines the line to pull up upon connect. The two connect source controls are: input m(N)_tllpuen, register field TllConnect. 0x0: Connect is Low-speed: D– pullup 0x1: Connect is Full-Speed: D+ pullup	RW	1
5	TLLCONNECT	Emulation of Full/Low-Speed connect (that is, D+ resp D– pullup) for serial TLL modes. Speed is determined by field TllSpeed. 0x0: Unconnected 0x1: Connected	RW	0
4	TLLATTACH	Emulates cable attach/detach for all serial TLL modes: * ChanMode = serial, in TLL mode (FsLsMode) * ChanMode = ULPI, in serial mode (6pin/3pin TLL) 0x0: Cable detach emulated on serial TLL 0x1: Cable attach emulated on serial TLL	RW	1
3	UTMIISADEV	Select the cable end "seen" by UTMI side of TLL, i.e. the emulated USB cable's orientation. The host must always be on A-side, peripheral on B-side. Reset value depends on generic DEFUTMIISHOST. 0x0: UTMI side is peripheral, ULPI side is host 0x1: UTMI side is host, ULPI side is peripheral	RW	1
2:1	CHANMODE	Main channel mode selection 0x0: UTMI-to-ULPI TLL mode (HS capable): to ULPI controller 0x1: UTMI-to-serial (FS/LS) mode: to serial controller (TLL) or serial PHY 0x2: Transparent UTMI mode: to UTMI PHY 0x3: No mode selected	RW	0x0
0	CHANEN	Active-high channel enable. A disabled channel is unclocked and kept under reset. 0x0: Channel i disabled 0x1: Channel i enabled	RW	0

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Table 23-972. Register Call Summary for Register TLL_CHANNEL_CONF_i

High-Speed Multiport USB Host Subsystem

- USBTLL Save and Restore: [0]
- USBTLL Channel Configuration: [1] [2]
- USBTLL VBUS Management and Emulations: [3] [4] [5] [6] [7] [8]
- USBTLL Multimode Serial Port: [9] [10]
- USBTLL Attach/Connect Emulation for Serial Modes: [11] [12] [13] [14] [15] [16] [17]
- Operational Modes Configuration (Selecting and Configuring USB Connectivity): [18]
- USBTLLHS_config Register Summary: [19]

Table 23-973. USBTLL_SAR_CNTX_j

Address Offset	0x0000 0400 + (0x4 * j)	**Index**	j = 0 to 6
Physical Address	0x4A06 2400 + (0x4 * j)	**Instance**	USBTLLHS_config
Description	Save and Restore context array. Array size is indicated in USBTLL_HWINFO. When in SAR mode, read to save and write to restore. Do not access when not in SAR mode.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CNTX																															

Bits	Field Name	Description	Type	Reset
31:0	CNTX	Context bits	RW	0x0000 0000

Table 23-974. Register Call Summary for Register USBTLL_SAR_CNTX_j

High-Speed Multiport USB Host Subsystem

- USBTLLHS_config Register Summary: [0]

23.11.6.3 USBTLLHS_ULPI Registers

23.11.6.3.1 USBTLLHS_ULPI Register Summary

Table 23-975 summarizes the USBTLLHS_ULPI register mapping.

Table 23-975. USBTLLHS_ULPI Register Mapping Summary

Register Name [1]	Type	Register Width (Bits)	Address Offset	Physical Address
VENDOR_ID_LO_i	R	8	0x0000 0000 + (0x100 * i)	0x4A06 2800 + (0x100 * i)
VENDOR_ID_HI_i	R	8	0x0000 0001 + (0x100 * i)	0x4A06 2801 + (0x100 * i)
PRODUCT_ID_LO_i	R	8	0x0000 0002 + (0x100 * i)	0x4A06 2802 + (0x100 * i)
PRODUCT_ID_HI_i	R	8	0x0000 0003 + (0x100 * i)	0x4A06 2803 + (0x100 * i)
FUNCTION_CTRL_i	RW	8	0x0000 0004 + (0x100 * i)	0x4A06 2804 + (0x100 * i)
FUNCTION_CTRL_SET_i	RW	8	0x0000 0005 + (0x100 * i)	0x4A06 2805 + (0x100 * i)
FUNCTION_CTRL_CLR_i	RW	8	0x0000 0006 + (0x100 * i)	0x4A06 2806 + (0x100 * i)
INTERFACE_CTRL_i	RW	8	0x0000 0007 + (0x100 * i)	0x4A06 2807 + (0x100 * i)
INTERFACE_CTRL_SET_i	RW	8	0x0000 0008 + (0x100 * i)	0x4A06 2808 + (0x100 * i)
INTERFACE_CTRL_CLR_i	RW	8	0x0000 0009 + (0x100 * i)	0x4A06 2809 + (0x100 * i)
OTG_CTRL_i	RW	8	0x0000 000A + (0x100 * i)	0x4A06 280A + (0x100 * i)
OTG_CTRL_SET_i	RW	8	0x0000 000B + (0x100 * i)	0x4A06 280B + (0x100 * i)
OTG_CTRL_CLR_i	RW	8	0x0000 000C + (0x100 * i)	0x4A06 280C + (0x100 * i)
USB_INT_EN_RISE_i	RW	8	0x0000 000D + (0x100 * i)	0x4A06 280D + (0x100 * i)

[1] i = 0 or 1

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Table 23-975. USBTLLHS_ULPI Register Mapping Summary (continued)

Register Name (1)	Type	Register Width (Bits)	Address Offset	Physical Address
USB_INT_EN_RISE_SET_i	RW	8	0x0000 000E + (0x100 * i)	0x4A06 280E + (0x100 * i)
USB_INT_EN_RISE_CLR_i	RW	8	0x0000 000F + (0x100 * i)	0x4A06 280F + (0x100 * i)
USB_INT_EN_FALL_i	RW	8	0x0000 0010 + (0x100 * i)	0x4A06 2810 + (0x100 * i)
USB_INT_EN_FALL_SET_i	RW	8	0x0000 0011 + (0x100 * i)	0x4A06 2811 + (0x100 * i)
USB_INT_EN_FALL_CLR_i	RW	8	0x0000 0012 + (0x100 * i)	0x4A06 2812 + (0x100 * i)
USB_INT_STATUS_i	R	8	0x0000 0013 + (0x100 * i)	0x4A06 2813 + (0x100 * i)
USB_INT_LATCH_i	R	8	0x0000 0014 + (0x100 * i)	0x4A06 2814 + (0x100 * i)
DEBUG_i	R	8	0x0000 0015 + (0x100 * i)	0x4A06 2815 + (0x100 * i)
SCRATCH_REGISTER_i	RW	8	0x0000 0016 + (0x100 * i)	0x4A06 2816 + (0x100 * i)
SCRATCH_REGISTER_SET_i	RW	8	0x0000 0017 + (0x100 * i)	0x4A06 2817 + (0x100 * i)
SCRATCH_REGISTER_CLR_i	RW	8	0x0000 0018 + (0x100 * i)	0x4A06 2818 + (0x100 * i)
EXTENDED_SET_ACCESS_i	R	8	0x0000 002F + (0x100 * i)	0x4A06 282F + (0x100 * i)
UTMI_VCONTROL_EN_i	RW	8	0x0000 0030 + (0x100 * i)	0x4A06 2830 + (0x100 * i)
UTMI_VCONTROL_EN_SET_i	RW	8	0x0000 0031 + (0x100 * i)	0x4A06 2831 + (0x100 * i)
UTMI_VCONTROL_EN_CLR_i	RW	8	0x0000 0032 + (0x100 * i)	0x4A06 2832 + (0x100 * i)
UTMI_VCONTROL_STATUS_i	RW	8	0x0000 0033 + (0x100 * i)	0x4A06 2833 + (0x100 * i)
UTMI_VCONTROL_LATCH_i	R	8	0x0000 0034 + (0x100 * i)	0x4A06 2834 + (0x100 * i)
UTMI_VSTATUS_i	RW	8	0x0000 0035 + (0x100 * i)	0x4A06 2835 + (0x100 * i)
UTMI_VSTATUS_SET_i	RW	8	0x0000 0036 + (0x100 * i)	0x4A06 2836 + (0x100 * i)
UTMI_VSTATUS_CLR_i	RW	8	0x0000 0037 + (0x100 * i)	0x4A06 2837 + (0x100 * i)
USB_INT_LATCH_NOCLR_i	R	8	0x0000 0038 + (0x100 * i)	0x4A06 2838 + (0x100 * i)
VENDOR_INT_EN_i	RW	8	0x0000 003B + (0x100 * i)	0x4A06 283B + (0x100 * i)
VENDOR_INT_EN_SET_i	RW	8	0x0000 003C + (0x100 * i)	0x4A06 283C + (0x100 * i)
VENDOR_INT_EN_CLR_i	RW	8	0x0000 003D + (0x100 * i)	0x4A06 283D + (0x100 * i)
VENDOR_INT_STATUS_i	R	8	0x0000 003E + (0x100 * i)	0x4A06 283E + (0x100 * i)
VENDOR_INT_LATCH_i	R	8	0x0000 003F + (0x100 * i)	0x4A06 283F + (0x100 * i)

23.11.6.3.2 USBTLLHS_ULPI Register Description

Table 23-976 through Table 23-1054 describe the USBTLLHS_ULPI registers.

Table 23-976. VENDOR_ID_LO_i

Address Offset	0x0000 0000 + (0x100 * i)	**Index**	i = 0 to 1
Physical Address	0x4A06 2800 + (0x100 * i)	**Instance**	USBTLLHS_ULPI
Description	Lower byte of USB-IF-supplied 16-bit vendor ID Value is set for all channels. Default is Texas Instruments Vendor ID = 0x0451.		
Type	R		

7	6	5	4	3	2	1	0
VENDOR_ID_LO							

Bits	Field Name	Description	Type	Reset
7:0	VENDOR_ID_LO		R	0x51

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Table 23-977. Register Call Summary for Register VENDOR_ID_LO_i

High-Speed Multiport USB Host Subsystem

- USBTLLHS_ULPI Register Summary: [0]

Table 23-978. VENDOR_ID_HI_i

Address Offset	0x0000 0001 + (0x100 * i)	**Index**	i = 0 to 1
Physical Address	0x4A06 2801 + (0x100 * i)	**Instance**	USBTLLHS_ULPI
Description	Upper byte of USB-IF-supplied 16-bit vendor ID Value is set for all channels. Default is Texas-Instruments Vendor ID = 0x0451.		
Type	R		

7	6	5	4	3	2	1	0
VENDOR_ID_HI							

Bits	Field Name	Description	Type	Reset
7:0	VENDOR_ID_HI		R	0x04

Table 23-979. Register Call Summary for Register VENDOR_ID_HI_i

High-Speed Multiport USB Host Subsystem

- USBTLLHS_ULPI Register Summary: [0]

Table 23-980. PRODUCT_ID_LO_i

Address Offset	0x0000 0002 + (0x100 * i)	**Index**	i = 0 to 1
Physical Address	0x4A06 2802 + (0x100 * i)	**Instance**	USBTLLHS_ULPI
Description	Lower byte of 16-bit product ID Value is set for all channels. Default is OMAP4460 Product ID =0xD010		
Type	R		

7	6	5	4	3	2	1	0
PRODUCT_ID_LO							

Bits	Field Name	Description	Type	Reset
7:0	PRODUCT_ID_LO		R	0x00

Table 23-981. Register Call Summary for Register PRODUCT_ID_LO_i

High-Speed Multiport USB Host Subsystem

- USBTLLHS_ULPI Register Summary: [0]

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Table 23-982. PRODUCT_ID_HI_i

Address Offset	0x0000 0003 + (0x100 * i)	**Index**	i = 0 to 1
Physical Address	0x4A06 2803 + (0x100 * i)	**Instance**	USBTLLHS_ULPI
Description	Upper byte of 16-bit product ID Value is set for all channels. Default is OMAP4460 Product ID =0xD010		
Type	R		

7	6	5	4	3	2	1	0
PRODUCT_ID_HI							

Bits	Field Name	Description	Type	Reset
7:0	PRODUCT_ID_HI		R	0x00

Table 23-983. Register Call Summary for Register PRODUCT_ID_HI_i

High-Speed Multiport USB Host Subsystem

- USBTLLHS_ULPI Register Summary: [0]

Table 23-984. FUNCTION_CTRL_i

Address Offset	0x0000 0004 + (0x100 * i)	**Index**	i = 0 to 1
Physical Address	0x4A06 2804 + (0x100 * i)	**Instance**	USBTLLHS_ULPI
Description	Controls UTMI function settings of the PHY. Read/write address.		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED	SUSPENDM	RESET	OPMODE		TERMSELECT	XCVRSELECT	

Bits	Field Name	Description	Type	Reset
7	RESERVED		R	0
6	SUSPENDM	Active low PHY suspend: puts the ULPI bus in low-power mode. Automatically set back to 1 upon low-power mode exit. 0x0: PHY is in low-power mode. 0x1: PHY is not in low-power mode.	RW	1
5	RESET	Active high UTMI transceiver reset. Auto-cleared. Does not reset the ULPI interface or ULPI register set. 0x0: No ongoing reset/no action 0x1: Ongoing reset/apply reset	RW	0
4:3	OPMODE	Select the required bit encoding style during transmit 0x0: Normal operation 0x1: Nondriving 0x3: Reserved 0x2: Disable bit-stuff and NRZI encoding	RW	0x0
2	TERMSELECT	Controls the internal 1.5-kΩ HS terminations. Control over bus resistors changes depending on XcvrSelect, OpMode, DpPulldown and DmPulldown. 0x0: HS termination enabled (other conditions) 0x1: FS termination enabled (other conditions)	RW	0

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Bits	Field Name	Description	Type	Reset
1:0	XCVRSELECT	Select the required transceiver speed. 0x0: Enable HS transceiver 0x1: Enable FS transceiver 0x3: Enable FS transceiver for LS packets (automatic FS preamble prepending) 0x2: Enable LS transceiver	RW	0x1

Table 23-985. Register Call Summary for Register FUNCTION_CTRL_i

High-Speed Multiport USB Host Subsystem
- USBTLL Save and Restore: [0]
- USBTLLHS_ULPI Register Summary: [1]

Table 23-986. FUNCTION_CTRL_SET_i

Address Offset	0x0000 0005 + (0x100 * i)	**Index**	i = 0 to 1
Physical Address	0x4A06 2805 + (0x100 * i)	**Instance**	USBTLLHS_ULPI
Description	Controls UTMI function settings of the PHY. Read/set address (write 1 to a bit to set it to 1, writing 0 has no effect on bit value). See the field description at the read/write address of the same register.		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED	SUSPENDM	RESET	OPMODE		TERMSELECT	XCVRSELECT	

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0x0
6	SUSPENDM	Active low PHY suspend: Puts the ULPI bus in low-power mode. Automatically set back to 1 upon low-power mode exit. Write 0x0: No effect on bit value Write 0x1: Set the bit to 1.	RW	0x1
5	RESET	Active high UTMI transceiver reset. Autocleared. Does not reset the ULPI interface or ULPI register set. Write 0x0: No effect on bit value Write 0x1: Set the bit to 1.	RW	0x0
4:3	OPMODE	Select the required bit encoding style during transmit. Write 0x0: No effect on bit value Write 0x1: Set the bit to 1.	RW	0x0
2	TERMSELECT	Controls the internal 1.5-kΩ pullup resistor and 45-Ω HS terminations. Control over bus resistors changes depending on XcvrSelect, OpMode, DpPulldown and DmPulldown. Write 0x0: No effect on bit value Write 0x1: Set the bit to 1.	RW	0x0
1:0	XCVRSELECT	Select the required transceiver speed. Write 0x0: No effect on bit value Write 0x1: Set the bit to 1.	RW	0x1

Table 23-987. Register Call Summary for Register FUNCTION_CTRL_SET_i

High-Speed Multiport USB Host Subsystem
- USBTLLHS_ULPI Register Summary: [0]

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Table 23-988. FUNCTION_CTRL_CLR_i

Address Offset	0x0000 0006 + (0x100 * i)	**Index**	i =0 to 1
Physical Address	0x4A06 2806 + (0x100 * i)	**Instance**	USBTLLHS_ULPI
Description	Controls UTMI function settings of the PHY. Read/clear address (write 1 to a bit to clear it to 0, writing 0 has no effect on bit value). See the field description at the read/write address of the same register.		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED	SUSPENDM	RESET	OPMODE		TERMSELECT	XCVRSELECT	

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0x0
6	SUSPENDM	Active low PHY suspend: Puts the ULPI bus in low-power mode. Automatically set back to 1 upon low-power mode exit. Write 0x0: No effect on bit value Write 0x1: Clear the bit to 0.	RW	0x1
5	RESET	Active high UTMI transceiver reset. Autocleared. Does not reset the ULPI interface or ULPI register set. Write 0x0: No effect on bit value Write 0x1: Clear the bit to 0.	RW	0x0
4:3	OPMODE	Select the required bit encoding style during transmit Write 0x0: No effect on bit value Write 0x1: Clear the bit to 0.	RW	0x0
2	TERMSELECT	Controls the internal 1.5-kΩ pull-up resistor and 45-Ω HS terminations. Control over bus resistors changes depending on XcvrSelect, OpMode, DpPulldown and DmPulldown. Write 0x0: No effect on bit value Write 0x1: Clear the bit to 0.	RW	0x0
1:0	XCVRSELECT	Select the required transceiver speed. Write 0x0: No effect on bit value Write 0x1: Clear the bit to 0.	RW	0x1

Table 23-989. Register Call Summary for Register FUNCTION_CTRL_CLR_i

High-Speed Multiport USB Host Subsystem

- USBTLLHS_ULPI Register Summary: [0]

Table 23-990. INTERFACE_CTRL_i

Address Offset	0x0000 0007 + (0x100 * i)	**Index**	i = 0 to 1
Physical Address	0x4A06 2807 + (0x100 * i)	**Instance**	USBTLLHS_ULPI
Description	Enables alternative interfaces and PHY features. Read/write address.		
Type	RW		

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7	6	5	4	3	2	1	0
INTERFACE_PROTECT_DISABLE	RESERVED		AUTORESUME	CLOCKSUSPENDM	RESERVED	FSLSSERIALMODE_3PIN	FSLSSERIALMODE_6PIN

Bits	Field Name	Description	Type	Reset
7	INTERFACE_PROTECT_DISABLE	Controls circuitry built into the PHY for protecting the ULPI interface when the link 3-states stp and data. 0x0: Enables the interface protect circuit 0x1: Disables the interface protect circuit	RW	0
6:5	RESERVED		R	0x0
4	AUTORESUME	Enables the PHY to automatically drive resume signaling. On by default. 0x0: AutoResume disabled 0x1: AutoResume enabled	RW	1
3	CLOCKSUSPENDM	Active low clock suspend for serial modes (6-pin/3-pin). 0x0: ULPI clock will stop during serial modes. 0x1: ULPI clock will run during serial modes.	RW	0
2	RESERVED		R	0
1	FSLSSERIALMODE_3PIN	Sets the ULPI interface to 3-pin (FS/LS only) serial mode. Auto-cleared when serial mode is exited. 0x0: ULPI is not in 3-pin mode. 0x1: ULPI is in 3-pin serial mode.	RW	0
0	FSLSSERIALMODE_6PIN	Sets the ULPI interface to 6-pin (FS/LS only) serial mode. Auto-cleared when serial mode is exited. 0x0: ULPI is not in 6-pin mode. 0x1: ULPI is in 6-pin serial mode.	RW	0

Table 23-991. Register Call Summary for Register INTERFACE_CTRL_i

High-Speed Multiport USB Host Subsystem

- USBTLL Save and Restore: [0]
- USBTLL Channel Configuration: [1] [2]
- USBTLLHS_ULPI Register Summary: [3]

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Table 23-992. INTERFACE_CTRL_SET_i

Address Offset	0x0000 0008 + (0x100 * i)	**Index**	i = 0 to 1
Physical Address	0x4A06 2808 + (0x100 * i)	**Instance**	USBTLLHS_ULPI
Description	Enables alternative interfaces and PHY features. Read/set address (write 1 to a bit to set it to 1, writing 0 has no effect on bit value). See field description at the read/write address of the same register.		
Type	RW		

7	6	5	4	3	2	1	0
INTERFACE_PROTECT_DISABLE	RESERVED		AUTORESUME	CLOCKSUSPENDM	RESERVED	FSLSSERIALMODE_3PIN	FSLSSERIALMODE_6PIN

Bits	Field Name	Description	Type	Reset
7	INTERFACE_PROTECT_DISABLE	Controls circuitry built into the PHY for protecting the ULPI interface when the link 3-states stp and data. Write 0x0: No effect on bit value Write 0x1: Set the bit to 1.	RW	0x0
6:5	RESERVED	Reserved	R	0x0
4	AUTORESUME	Enables the PHY to automatically drive resume signaling. On by default. Write 0x0: No effect on bit value Write 0x1: Set the bit to 1.	RW	0x0
3	CLOCKSUSPENDM	Active low clock suspend for serial modes (6-pin/3-pin). Write 0x0: No effect on bit value Write 0x1: Set the bit to 1.	RW	0x0
2	RESERVED	Reserved	R	0x0
1	FSLSSERIALMODE_3PIN	Sets the ULPI interface to 3-pin (FS/LS only) serial mode. Autocleared when serial mode is exited. Write 0x0: No effect on bit value Write 0x1: Set the bit to 1.	RW	0x0
0	FSLSSERIALMODE_6PIN	Sets the ULPI interface to 6-pin (FS/LS only) serial mode. Autocleared when serial mode is exited. Write 0x0: No effect on bit value Write 0x1: Set the bit to 1.	RW	0x0

Table 23-993. Register Call Summary for Register INTERFACE_CTRL_SET_i

High-Speed Multiport USB Host Subsystem

- USBTLLHS_ULPI Register Summary: [0]

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Table 23-994. INTERFACE_CTRL_CLR_i

Address Offset	0x0000 0009 + (0x100 * i)	**Index**	i = 0 to 1
Physical Address	0x4A06 2809 + (0x100 * i)	**Instance**	USBTLLHS_ULPI
Description	Enables alternative interfaces and PHY features. Read/clear address (write 1 to a bit to clear it to 0, writing 0 has no effect on bit value). See fields description at the read/write address of the same register.		
Type	RW		

7	6	5	4	3	2	1	0
INTERFACE_PROTECT_DISABLE	RESERVED		AUTORESUME	CLOCKSUSPENDM	RESERVED	FSLSSERIALMODE_3PIN	FSLSSERIALMODE_6PIN

Bits	Field Name	Description	Type	Reset
7	INTERFACE_PROTECT_DISABLE	Controls circuitry built into the PHY for protecting the ULPI interface when the link 3-states stp and data. Write 0x0: No effect on bit value Write 0x1: Clear the bit to 0.	RW	0x0
6:5	RESERVED	Reserved	R	0x0
4	AUTORESUME	Enables the PHY to automatically drive resume signaling. On by default. Write 0x0: No effect on bit value Write 0x1: Clear the bit to 0.	RW	0x0
3	CLOCKSUSPENDM	Active low clock suspend for serial modes (6-pin/3-pin). Write 0x0: No effect on bit value Write 0x1: Clear the bit to 0.	RW	0x0
2	RESERVED	Reserved	R	0x0
1	FSLSSERIALMODE_3PIN	Sets the ULPI interface to 3-pin (FS/LS only) serial mode. Autocleared when serial mode is exited. Write 0x0: No effect on bit value Write 0x1: Clear the bit to 0.	RW	0x0
0	FSLSSERIALMODE_6PIN	Sets the ULPI interface to 6-pin (FS/LS only) serial mode. Autocleared when serial mode is exited. Write 0x0: No effect on bit value Write 0x1: Clear the bit to 0.	RW	0x0

Table 23-995. Register Call Summary for Register INTERFACE_CTRL_CLR_i

High-Speed Multiport USB Host Subsystem

- USBTLLHS_ULPI Register Summary: [0]

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Table 23-996. OTG_CTRL_i

Address Offset	0x0000 000A + (0x100 * i)	**Index**	i = 0 to 1
Physical Address	0x4A06 280A + (0x100 * i)	**Instance**	USBTLLHS_ULPI
Description	Controls UTMI+ OTG functions of the PHY. Read/write address.		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED		DRVVBUS	CHRGVBUS	DISCHRGVBUS	DMPULLDOWN	DPPULLDOWN	IDPULLUP

Bits	Field Name	Description	Type	Reset
7:6	RESERVED		R	0x0
5	DRVVBUS	Drive 5 V on VBUS 0x0: No action 0x1: Drive VBUS.	RW	0
4	CHRGVBUS	Charge VBUS through a resistor for VBUS-pulsing SRP. 0x0: No action 0x1: Charge VBUS.	RW	0
3	DISCHRGVBUS	Discharge VBUS through a resistor, until the session-end VBUS state is reached. 0x0: No action 0x1: Discharge VBUS.	RW	0
2	DMPULLDOWN	Enables the 15-kΩ pulldown resistor on D– 0x0: Pulldown resistor not connected to D– 0x1: Pulldown resistor connected to D–	RW	1
1	DPPULLDOWN	Enables the 15-kΩ pulldown resistor on D+ 0x0: Pulldown resistor not connected to D+ 0x1: Pulldown resistor connected to D+	RW	1
0	IDPULLUP	Pullup to the (OTG) ID line to allow its sampling 0x0: Disable sampling of ID line. 0x1: Enable sampling of ID line.	RW	0

Table 23-997. Register Call Summary for Register OTG_CTRL_i

High-Speed Multiport USB Host Subsystem

- USBTLL Save and Restore: [0]
- USBTLL VBUS Management and Emulations: [1] [2] [3]
- USBTLLHS_ULPI Register Summary: [4]

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Table 23-998. OTG_CTRL_SET_i

Address Offset	0x0000 000B + (0x100 * i)	**Index**	i = 0 to 1
Physical Address	0x4A06 280B + (0x100 * i)	**Instance**	USBTLLHS_ULPI
Description	Controls UTMI+ OTG functions of the PHY. Read/set address (write 1 to a bit to set it to 1, writing 0 has no effect on bit value). See field description at the read/write address of the same register.		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED		DRVVBUS	CHRGVBUS	DISCHRGVBUS	DMPULLDOWN	DPPULLDOWN	IDPULLUP

Bits	Field Name	Description	Type	Reset
7:6	RESERVED	Reserved	R	0x0
5	DRVVBUS	Drive 5 V on VBUS Write 0x0: No effect on bit value Write 0x1: Set the bit to 1.	RW	0x0
4	CHRGVBUS	Charge VBUS through a resistor for VBUS-pulsing SRP. Write 0x0: No effect on bit value 0x1: Set the bit to 1.	RW	0x0
3	DISCHRGVBUS	Discharge VBUS through a resistor, until the session-end VBUS state is reached. Write 0x0: No effect on bit value Write 0x1: Set the bit to 1.	RW	0x0
2	DMPULLDOWN	Enables the 15-kΩ pulldown resistor on D– Write 0x0: No effect on bit value Write 0x1: Set the bit to 1.	RW	0x0
1	DPPULLDOWN	Enables the 15-kΩ pulldown resistor on D+ Write 0x0: No effect on bit value Write 0x1: Set the bit to 1.	RW	0x0
0	IDPULLUP	Pullup to the (OTG) ID line to allow its sampling Write 0x0: No effect on bit value Write 0x1: Set the bit to 1.	RW	0x0

Table 23-999. Register Call Summary for Register OTG_CTRL_SET_i

High-Speed Multiport USB Host Subsystem

- USBTLLHS_ULPI Register Summary: [0]

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Table 23-1000. OTG_CTRL_CLR_i

Address Offset	0x0000 000C + (0x100 * i)	**Index**	i = 0 to 1
Physical Address	0x4A06 280C + (0x100 * i)	**Instance**	USBTLLHS_ULPI
Description	Controls UTMI+ OTG functions of the PHY. Read/clear address (write 1 to a bit to clear it to 0, writing 0 has no effect on bit value). See fields description at the read/write address of the same register.		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED		DRVVBUS	CHRGVBUS	DISCHRGVBUS	DMPULLDOWN	DPPULLDOWN	IDPULLUP

Bits	Field Name	Description	Type	Reset
7:6	RESERVED	Reserved	R	0x0
5	DRVVBUS	Drive 5 V on VBUS Write 0x0: No effect on bit value Write 0x1: Clear the bit to 0.	RW	0x0
4	CHRGVBUS	Charge VBUS through a resistor for VBUS-pulsing SRP. Write 0x0: No effect on bit value Write 0x1: Clear the bit to 0.	RW	0x0
3	DISCHRGVBUS	Discharge VBUS through a resistor, until the session-end VBUS state is reached. Write 0x0: No effect on bit value Write 0x1: Clear the bit to 0.	RW	0x0
2	DMPULLDOWN	Enables the 15k pulldown resistor on D– Write 0x0: No effect on bit value Write 0x1: Clear the bit to 0.	RW	0x0
1	DPPULLDOWN	Enables the 15kΩ pulldown resistor on D+ Write 0x0: No effect on bit value Write 0x1: Clear the bit to 0.	RW	0x0
0	IDPULLUP	Pullup to the (OTG) ID line to allow its sampling Write 0x0: No effect on bit value Write 0x1: Clear the bit to 0.	RW	0x0

Table 23-1001. Register Call Summary for Register OTG_CTRL_CLR_i

High-Speed Multiport USB Host Subsystem

- USBTLLHS_ULPI Register Summary: [0]

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Table 23-1002. USB_INT_EN_RISE_i

Address Offset	0x0000 000D + (0x100 * i)	**Index**	i = 0 to 1
Physical Address	0x4A06 280D + (0x100 * i)	**Instance**	USBTLLHS_ULPI
Description	Enables an interrupt event notification when the corresponding status bit changes from low to high. By default, all transitions are enabled. Read/write address.		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED			IDGND_RISE	SESSEND_RISE	SESSVALID_RISE	VBUSVALID_RISE	HOSTDISCONNECT_RISE

Bits	Field Name	Description	Type	Reset
7:5	RESERVED		R	0x0
4	IDGND_RISE	Generate an interrupt event notification when IdGnd changes from low to high. Event is automatically masked if IdPullup bit is clear to 0 and for 50ms after IdPullup is set to 1. Write 0x0: No effect on bit value Write 0x1: Set the bit to 1	RW	1
3	SESSEND_RISE	Generate an interrupt event notification when SessEnd changes from low to high. Write 0x0: No effect on bit value Write 0x1: Set the bit to 1	RW	1
2	SESSVALID_RISE	Generate an interrupt event notification when SessValid changes from low to high. SessValid is the same as UTMI+ AValid. Write 0x0: No effect on bit value Write 0x1: Set the bit to 1	RW	1
1	VBUSVALID_RISE	Generate an interrupt event notification when VbusValid changes from low to high. Write 0x0: No effect on bit value Write 0x1: Set the bit to 1	RW	1
0	HOSTDISCONNECT_RISE	Generate an interrupt event notification when Hostdisconnect changes from low to high. Applicable only in host mode (DpPulldown and DmPulldown both set to 1b). Write 0x0: No effect on bit value Write 0x1: Set the bit to 1	RW	1

Table 23-1003. Register Call Summary for Register USB_INT_EN_RISE_i

High-Speed Multiport USB Host Subsystem

- USBTLL Save and Restore: [0]
- USBTLLHS_ULPI Register Summary: [1]

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Table 23-1004. USB_INT_EN_RISE_SET_i

Address Offset	0x0000 000E + (0x100 * i)	**Index**	i = 0 to 1
Physical Address	0x4A06 280E + (0x100 * i)	**Instance**	USBTLLHS_ULPI
Description	Enables an interrupt event notification when the corresponding status bit changes from low to high. Read/set address (write 1 to a bit to set it to 1, writing 0 has no effect on bit value). See fields description at the read/write address of the same register.		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED			IDGND_RISE	SESSEND_RISE	SESSVALID_RISE	VBUSVALID_RISE	HOSTDISCONNECT_RISE

Bits	Field Name	Description	Type	Reset
7:5	RESERVED		R	0x0
4	IDGND_RISE	Generate an interrupt event notification when IdGnd changes from low to high. Event is automatically masked if IdPullup bit is clear to 0 and for 50ms after IdPullup is set to 1. Write 0x0: No effect on bit value Write 0x1: Set the bit to 1.	RW	0x0
3	SESSEND_RISE	Generate an interrupt event notification when SessEnd changes from low to high. Write 0x0: No effect on bit value Write 0x1: Set the bit to 1.	RW	0x0
2	SESSVALID_RISE	Generate an interrupt event notification when SessValid changes from low to high. SessValid is the same as UTMI+ AValid. Write 0x0: No effect on bit value Write 0x1: Set the bit to 1.	RW	0x0
1	VBUSVALID_RISE	Generate an interrupt event notification when VbusValid changes from low to high. Write 0x0: No effect on bit value Write 0x1: Set the bit to 1.	RW	0x0
0	HOSTDISCONNECT_RISE	Generate an interrupt event notification when Hostdisconnect changes from low to high. Applicable only in host mode (DpPulldown and DmPulldown both set to 1b). Write 0x0: No effect on bit value Write 0x1: Set the bit to 1.	RW	0x0

Table 23-1005. Register Call Summary for Register USB_INT_EN_RISE_SET_i

High-Speed Multiport USB Host Subsystem

- USBTLLHS_ULPI Register Summary: [0]

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Table 23-1006. USB_INT_EN_RISE_CLR_i

Address Offset	0x0000 000F + (0x100 * i)	**Index**	i = 0 to 1
Physical Address	0x4A06 280F + (0x100 * i)	**Instance**	USBTLLHS_ULPI
Description	Enables an interrupt event notification when the corresponding status bit changes from low to high. Read/clear address (write 1 to a bit to clear it to 0, writing 0 has no effect on bit value). See the field description at the read/write address of the same register.		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED			IDGND_RISE	SESSEND_RISE	SESSVALID_RISE	VBUSVALID_RISE	HOSTDISCONNECT_RISE

Bits	Field Name	Description	Type	Reset
7:5	RESERVED	Reserved	R	0x0
4	IDGND_RISE	Generate an interrupt event notification when IdGnd changes from low to high. Event is automatically masked if IdPullup bit is clear to 0 and for 50 ms after IdPullup is set to 1. Write 0x0: No effect on bit value Write 0x1: Clear the bit to 0.	RW	0x0
3	SESSEND_RISE	Generate an interrupt event notification when SessEnd changes from low to high. Write 0x0: No effect on bit value Write 0x1: Clear the bit to 0.	RW	0x0
2	SESSVALID_RISE	Generate an interrupt event notification when SessValid changes from low to high. SessValid is the same as UTMI+ AValid. Write 0x0: No effect on bit value Write 0x1: Clear the bit to 0.	RW	0x0
1	VBUSVALID_RISE	Generate an interrupt event notification when VbusValid changes from low to high. Write 0x0: No effect on bit value Write 0x1: Clear the bit to 0.	RW	0x0
0	HOSTDISCONNECT_RISE	Generate an interrupt event notification when Hostdisconnect changes from low to high. Applicable only in host mode (DpPulldown and DmPulldown both set to 1b). Write 0x0: No effect on bit value Write 0x1: Clear the bit to 0.	RW	0x0

Table 23-1007. Register Call Summary for Register USB_INT_EN_RISE_CLR_i

High-Speed Multiport USB Host Subsystem

- USBTLLHS_ULPI Register Summary: [0]

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Table 23-1008. USB_INT_EN_FALL_i

Address Offset	0x0000 0010 + (0x100 * i)	**Index**	i = 0 to 1
Physical Address	0x4A06 2810 + (0x100 * i)	**Instance**	USBTLLHS_ULPI
Description	Enables an interrupt event notification when the corresponding status bit changes from high to low. By default, all transitions are enabled. Read/write address.		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED			IDGND_FALL	SESSEND_FALL	SESSVALID_FALL	VBUSVALID_FALL	HOSTDISCONNECT_FALL

Bits	Field Name	Description	Type	Reset
7:5	RESERVED		R	0x0
4	IDGND_FALL	Generate an interrupt event notification when IdGnd changes from high to low. Event is automatically masked if IdPullup bit is clear to 0 and for 50 ms after IdPullup is set to 1.	RW	1
3	SESSEND_FALL	Generate an interrupt event notification when SessEnd changes from high to low.	RW	1
2	SESSVALID_FALL	Generate an interrupt event notification when SessValid changes from high to low. SessValid is the same as UTMI+ AValid.	RW	1
1	VBUSVALID_FALL	Generate an interrupt event notification when VbusValid changes from high to low.	RW	1
0	HOSTDISCONNECT_FALL	Generate an interrupt event notification when Hostdisconnect changes from high to low. Applicable only in host mode (DpPulldown and DmPulldown both set to 1b).	RW	1

Table 23-1009. Register Call Summary for Register USB_INT_EN_FALL_i

High-Speed Multiport USB Host Subsystem

- USBTLL Save and Restore: [0]
- USBTLLHS_ULPI Register Summary: [1]

Table 23-1010. USB_INT_EN_FALL_SET_i

Address Offset	0x0000 0011 + (0x100 * i)	**Index**	i = 0 to 1
Physical Address	0x4A06 2811 + (0x100 * i)	**Instance**	USBTLLHS_ULPI
Description	Enables an interrupt event notification when the corresponding status bit changes from high to low. Read/set address (write 1 to a bit to set it to 1, writing 0 has no effect on bit value). See fields description at the read/write address of the same register.		
Type	RW		

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7	6	5	4	3	2	1	0
RESERVED			IDGND_RISE	SESSEND_RISE	SESSVALID_RISE	VBUSVALID_RISE	HOSTDISCONNECT_RISE

Bits	Field Name	Description	Type	Reset
7:5	RESERVED		R	0x0
4	IDGND_RISE	Generate an interrupt event notification when IdGnd changes from low to high. Event is automatically masked if IdPullup bit is clear to 0 and for 50 ms after IdPullup is set to 1. Write 0x0: No effect on bit value Write 0x1: Set the bit to 1.	RW	0x0
3	SESSEND_RISE	Generate an interrupt event notification when SessEnd changes from low to high. Write 0x0: No effect on bit value Write 0x1: Set the bit to 1.	RW	0x0
2	SESSVALID_RISE	Generate an interrupt event notification when SessValid changes from low to high. SessValid is the same as UTMI+ AValid. Write 0x0: No effect on bit value Write 0x1: Set the bit to 1.	RW	0x0
1	VBUSVALID_RISE	Generate an interrupt event notification when VbusValid changes from low to high. Write 0x0: No effect on bit value Write 0x1: Set the bit to 1.	RW	0x0
0	HOSTDISCONNECT_RISE	Generate an interrupt event notification when Hostdisconnect changes from low to high. Applicable only in host mode (DpPulldown and DmPulldown both set to 1b). Write 0x0: No effect on bit value Write 0x1: Set the bit to 1.	RW	0x0

Table 23-1011. Register Call Summary for Register USB_INT_EN_FALL_SET_i

High-Speed Multiport USB Host Subsystem

- USBTLLHS_ULPI Register Summary: [0]

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Table 23-1012. USB_INT_EN_FALL_CLR_i

Address Offset	0x0000 0012 + (0x100 * i)	**Index**	i = 0 to 1
Physical Address	0x4A06 2812 + (0x100 * i)	**Instance**	USBTLLHS_ULPI
Description	Enables an interrupt event notification when the corresponding status bit changes from high to low. Read/clear address (write 1 to a bit to clear it to 0, writing 0 has no effect on bit value). See field description at the read/write address of the same register.		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED			IDGND_RISE	SESSEND_RISE	SESSVALID_RISE	VBUSVALID_RISE	HOSTDISCONNECT_RISE

Bits	Field Name	Description	Type	Reset
7:5	RESERVED		R	0x0
4	IDGND_RISE	Generate an interrupt event notification when IdGnd changes from low to high. Event is automatically masked if IdPullup bit is clear to 0 and for 50 ms after IdPullup is set to 1. Write 0x0: No effect on bit value Write 0x1: Clear the bit to 0.	RW	0x0
3	SESSEND_RISE	Generate an interrupt event notification when SessEnd changes from low to high. Write 0x0: No effect on bit value Write 0x1: Clear the bit to 0.	RW	0x0
2	SESSVALID_RISE	Generate an interrupt event notification when SessValid changes from low to high. SessValid is the same as UTMI+ AValid. Write 0x0: No effect on bit value Write 0x1: Clear the bit to 0.	RW	0x0
1	VBUSVALID_RISE	Generate an interrupt event notification when VbusValid changes from low to high. Write 0x0: No effect on bit value Write 0x1: Clear the bit to 0.	RW	0x0
0	HOSTDISCONNECT_RISE	Generate an interrupt event notification when Hostdisconnect changes from low to high. Applicable only in host mode (DpPulldown and DmPulldown both set to 1b). Write 0x0: No effect on bit value Write 0x1: Clear the bit to 0.	RW	0x0

Table 23-1013. Register Call Summary for Register USB_INT_EN_FALL_CLR_i

High-Speed Multiport USB Host Subsystem

- USBTLLHS_ULPI Register Summary: [0]

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Table 23-1014. USB_INT_STATUS_i

Address Offset	0x0000 0013 + (0x100 * i)	**Index**	i = 0 to 1
Physical Address	0x4A06 2813 + (0x100 * i)	**Instance**	USBTLLHS_ULPI
Description	Indicates the current value of the interrupt source signal.		
Type	R		

7	6	5	4	3	2	1	0
RESERVED			IDGND	SESSEND	SESSVALID	VBUSVALID	HOSTDISCONNECT

Bits	Field Name	Description	Type	Reset
7:5	RESERVED	Reserved	R	0x0
4	IDGND	Value of UTMI+ IdDig output. Undefined unless IdPullup = 1 Read 0x1: ID pin is floating = OTG B = default peripheral Read 0x0: ID pin is grounded = OTG A = default host	R	0
3	SESSEND	Current value of UTMI+ SessEnd output. Read 0x1: VBUS is below Session-End threshold. Read 0x0: VBUS is above Session-End threshold.	R	0
2	SESSVALID	Current value of UTMI+ SessValid output. SessValid is the same as UTMI+ AValid. Read 0x1: VBUS is above Session-Valid threshold. Read 0x0: VBUS is below Session-Valid threshold.	R	0
1	VBUSVALID	Current value of UTMI+ VbusValid output. Read 0x1: VBUS is above Vbus-Valid threshold. Read 0x0: VBUS is below Vbus-Valid threshold.	R	0
0	HOSTDISCONNECT	Current value of UTMI+ Hostdisconnect output. Applicable only in host mode. Automatically reset to 0 when low-power mode is entered. Read 0x1: Peripheral disconnected Read 0x0: Peripheral not disconnected or nonhost mode	R	0

Table 23-1015. Register Call Summary for Register USB_INT_STATUS_i

High-Speed Multiport USB Host Subsystem

- USBTLL Save and Restore: [0]
- USBTLL VBUS Management and Emulations: [1] [2] [3]
- USBTLLHS_ULPI Register Summary: [4]

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Table 23-1016. USB_INT_LATCH_i

Address Offset	0x0000 0014 + (0x100 * i)	**Index**	i = 0 to 1
Physical Address	0x4A06 2814 + (0x100 * i)	**Instance**	USBTLLHS_ULPI
Description	Set by unmasked changes on the corresponding status bits to generate the ULPI interrupt. Cleared upon read, and when low-power mode, serial mode, or carkit mode are entered.		
Type	R		

7	6	5	4	3	2	1	0
RESERVED			IDGND_LATCH	SESSEND_LATCH	SESSVALID_LATCH	VBUSVALID_LATCH	HOSTDISCONNECT_LATCH

Bits	Field Name	Description	Type	Reset
7:5	RESERVED	Reserved	R	0x0
4	IDGND_LATCH	Set to 1 by the PHY when an unmasked event occurs on IdGnd. Cleared when this register is read.	R	0
3	SESSEND_LATCH	Set to 1 by the PHY when an unmasked event occurs on SessEnd. Cleared when this register is read.	R	0
2	SESSVALID_LATCH	Set to 1 by the PHY when an unmasked event occurs on SessValid. Cleared when this register is read. SessValid is the same as UTMI+ AValid.	R	0
1	VBUSVALID_LATCH	Set to 1 by the PHY when an unmasked event occurs on VbusValid. Cleared when this register is read.	R	0
0	HOSTDISCONNECT_LATCH	Set to 1 by the PHY when an unmasked event occurs on Hostdisconnect. Cleared when this register is read. Applicable only in host mode.	R	0

Table 23-1017. Register Call Summary for Register USB_INT_LATCH_i

High-Speed Multiport USB Host Subsystem

- USBTLLHS_ULPI Register Summary: [0]

Table 23-1018. DEBUG_i

Address Offset	0x0000 0015 + (0x100 * i)	**Index**	i = 0 to 1
Physical Address	0x4A06 2815 + (0x100 * i)	**Instance**	USBTLLHS_ULPI
Description	Indicates the current value of various signals useful for debugging.		
Type	R		

7	6	5	4	3	2	1	0
RESERVED						LINE STATE	

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Bits	Field Name	Description	Type	Reset
7:2	RESERVED		R	0x00
1:0	LINE STATE	Current state of the USB line: D+ (bit 0) and D– (bit 1). Read 0x3: SE1 (LS/FS), Invalid (HS/Chirp) Read 0x2: LS: J state, FS: K state, HS: Invalid, Chirp: !Squelch !HS_Differential_Receiver_Output Read 0x1: LS: K state, FS: J state, HS: !Squelch, Chirp: !Squelch HS_Differential_Receiver_Output Read 0x0: SE0 (LS/FS), Squelch (HS/Chirp)	R	0x0

Table 23-1019. Register Call Summary for Register DEBUG_i

High-Speed Multiport USB Host Subsystem

- USBTLLHS_ULPI Register Summary: [0]

Table 23-1020. SCRATCH_REGISTER_i

Address Offset	0x0000 0016 + (0x100 * i)	**Index**	i = 0 to 1
Physical Address	0x4A06 2816 + (0x100 * i)	**Instance**	USBTLLHS_ULPI
Description	Register byte for register access testing purposes. Value has no functional effect on PHY. Read/write address.		
Type	RW		

7	6	5	4	3	2	1	0
SCRATCH							

Bits	Field Name	Description	Type	Reset
7:0	SCRATCH	Scratch data	RW	0x00

Table 23-1021. Register Call Summary for Register SCRATCH_REGISTER_i

High-Speed Multiport USB Host Subsystem

- USBTLLHS_ULPI Register Summary: [0]

Table 23-1022. SCRATCH_REGISTER_SET_i

Address Offset	0x0000 0017 + (0x100 * i)	**Index**	i = 0 to 1
Physical Address	0x4A06 2817 + (0x100 * i)	**Instance**	USBTLLHS_ULPI
Description	Register byte for register access testing purposes. Value has no functional effect on PHY. Read/set address (write 1 to a bit to set it to 1, writing 0 has no effect on bit value). See field description at the read/write address of the same register.		
Type	RW		

7	6	5	4	3	2	1	0
SCRATCH							

Bits	Field Name	Description	Type	Reset
7:0	SCRATCH	Scratch data Write 1 to a bit to set it to 1. Writing 0 has no effect on bit value.	RW	0x00

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Table 23-1023. Register Call Summary for Register SCRATCH_REGISTER_SET_i

High-Speed Multiport USB Host Subsystem

- USBTLLHS_ULPI Register Summary: [0]

Table 23-1024. SCRATCH_REGISTER_CLR_i

Address Offset	0x0000 0018 + (0x100 * i)	**Index**	i = 0 to 1
Physical Address	0x4A06 2818 + (0x100 * i)	**Instance**	USBTLLHS_ULPI
Description	Register byte for register access testing purposes. Value has no functional effect on PHY. Read/clear address (write 1 to a bit to clear it to 0, writing 0 has no effect on bit value). See field description at the read/write address of the same register.		
Type	RW		

7	6	5	4	3	2	1	0
SCRATCH							

Bits	Field Name	Description	Type	Reset
7:0	SCRATCH	Scratch data Write 1 to a bit to clear it to 0. Writing 0 has no effect on bit value.	RW	0x00

Table 23-1025. Register Call Summary for Register SCRATCH_REGISTER_CLR_i

High-Speed Multiport USB Host Subsystem

- USBTLLHS_ULPI Register Summary: [0]

Table 23-1026. EXTENDED_SET_ACCESS_i

Address Offset	0x0000 002F + (0x100 * i)	**Index**	i = 0 to 1
Physical Address	0x4A06 282F + (0x100 * i)	**Instance**	USBTLLHS_ULPI
Description	This address is used to access the extended register set; that is, addresses above 0x40.		
Type	RW		

7	6	5	4	3	2	1	0
SET_ACCESS							

Bits	Field Name	Description	Type	Reset
7:0	SET_ACCESS	This bit field is used to access the extended register set; that is, addresses above 0x40.	RW	0x00

Table 23-1027. Register Call Summary for Register EXTENDED_SET_ACCESS_i

High-Speed Multiport USB Host Subsystem

- USBTLLHS_ULPI Register Summary: [0]

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Table 23-1028. UTMI_VCONTROL_EN_i

Address Offset	0x0000 0030 + (0x100 * i)	**Index**	i = 0 to 1
Physical Address	0x4A06 2830 + (0x100 * i)	**Instance**	USBTLLHS_ULPI
Description	Part of nonstandard UTMI-to-ULPI mailbox system, implemented if HDL generic VCS_MAILBOX bit is 1 Enables an interrupt notification when the corresponding vcontrol_status bit changes. Read/write address. Lowest VCS_CTRL_WIDTH (HDL generic) bits are implemented, others are always-0, read-only. (UTMI standard is 4-bit.)		
Type	RW		

7	6	5	4	3	2	1	0
VC7_EN	VC6_EN	VC5_EN	VC4_EN	VC3_EN	VC2_EN	VC1_EN	VC0_EN

Bits	Field Name	Description	Type	Reset
7	VC7_EN	Enable alt_int assertion upon vcontrol_status bit change: Write 0x0: No effect on bit value Write 0x1: Set the bit to 1.	RW	0x0
6	VC6_EN	Enable alt_int assertion upon vcontrol_status bit change: Write 0x0: No effect on bit value Write 0x1: Set the bit to 1.	RW	0x0
5	VC5_EN	Enable alt_int assertion upon vcontrol_status bit change: Write 0x0: No effect on bit value Write 0x1: Set the bit to 1.	RW	0x0
4	VC4_EN	Enable alt_int assertion upon vcontrol_status bit change: Write 0x0: No effect on bit value Write 0x1: Set the bit to 1.	RW	0x0
3	VC3_EN	Enable alt_int assertion upon vcontrol_status bit change: Write 0x0: No effect on bit value Write 0x1: Set the bit to 1.	RW	0x0
2	VC2_EN	Enable alt_int assertion upon vcontrol_status bit change: Write 0x0: No effect on bit value Write 0x1: Set the bit to 1.	RW	0x0
1	VC1_EN	Enable alt_int assertion upon vcontrol_status bit change: Write 0x0: No effect on bit value Write 0x1: Set the bit to 1.	RW	0x0
0	VC0_EN	Enable alt_int assertion upon vcontrol_status bit change: Write 0x0: No effect on bit value Write 0x1: Set the bit to 1.	RW	0x0

Table 23-1029. Register Call Summary for Register UTMI_VCONTROL_EN_i

High-Speed Multiport USB Host Subsystem

- USBTLLHS_ULPI Register Summary: [0]

Table 23-1030. UTMI_VCONTROL_EN_SET_i

Address Offset	0x0000 0031 + (0x100 * i)	**Index**	i = 0 to 1
Physical Address	0x4A06 2831 + (0x100 * i)	**Instance**	USBTLLHS_ULPI
Description	Part of nonstandard UTMI-to-ULPI mailbox system, implemented if HDL generic VCS_MAILBOX bit is 1 Enables an interrupt notification when the corresponding vcontrol_status bit changes. Read/set address (write 1 to a bit to set it to 1, writing 0 has no effect on bit value). See fields description at the read/write address of the same register.		
Type	RW		

7	6	5	4	3	2	1	0
VC7_EN	VC6_EN	VC5_EN	VC4_EN	VC3_EN	VC2_EN	VC1_EN	VC0_EN

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Bits	Field Name	Description	Type	Reset
7	VC7_EN	Enable alt_int assertion upon vcontrol_status bit change: Write 0x0: No effect on bit value Write 0x1: Set the bit to 1.	RW	0x0
6	VC6_EN	Enable alt_int assertion upon vcontrol_status bit change: Write 0x0: No effect on bit value Write 0x1: Set the bit to 1.	RW	0x0
5	VC5_EN	Enable alt_int assertion upon vcontrol_status bit change: Write 0x0: No effect on bit value Write 0x1: Set the bit to 1.	RW	0x0
4	VC4_EN	Enable alt_int assertion upon vcontrol_status bit change: Write 0x0: No effect on bit value Write 0x1: Set the bit to 1.	RW	0x0
3	VC3_EN	Enable alt_int assertion upon vcontrol_status bit change: Write 0x0: No effect on bit value Write 0x1: Set the bit to 1.	RW	0x0
2	VC2_EN	Enable alt_int assertion upon vcontrol_status bit change: Write 0x0: No effect on bit value Write 0x1: Set the bit to 1.	RW	0x0
1	VC1_EN	Enable alt_int assertion upon vcontrol_status bit change: Write 0x0: No effect on bit value Write 0x1: Set the bit to 1.	RW	0x0
0	VC0_EN	Enable alt_int assertion upon vcontrol_status bit change: Write 0x0: No effect on bit value Write 0x1: Set the bit to 1.	RW	0x0

Table 23-1031. Register Call Summary for Register UTMI_VCONTROL_EN_SET_i

High-Speed Multiport USB Host Subsystem

- USBTLLHS_ULPI Register Summary: [0]

Table 23-1032. UTMI_VCONTROL_EN_CLR_i

Address Offset	0x0000 0032 + (0x100 * i)	**Index**	i = 0 to 1
Physical Address	0x4A06 2832 + (0x100 * i)	**Instance**	USBTLLHS_ULPI
Description	Part of nonstandard UTMI-to-ULPI mailbox system, implemented if HDL generic VCS_MAILBOX bit is 1. Enables an interrupt notification when the corresponding vcontrol_status bit changes. Read/clear address (write 1 to a bit to clear it to 0, writing 0 has no effect on bit value). See fields description at the read/write address of the same register.		
Type	RW		

7	6	5	4	3	2	1	0
VC							

Bits	Field Name	Description	Type	Reset
7:0	VC	User-defined UTMI control data byte	RW	0x00

Table 23-1033. Register Call Summary for Register UTMI_VCONTROL_EN_CLR_i

High-Speed Multiport USB Host Subsystem

- USBTLLHS_ULPI Register Summary: [0]

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Table 23-1034. UTMI_VCONTROL_STATUS_i

Address Offset	0x0000 0033 + (0x100 * i)	**Index**	i = 0 to 1
Physical Address	0x4A06 2833 + (0x100 * i)	**Instance**	USBTLLHS_ULPI
Description	Part of nonstandard UTMI-to-ULPI mailbox system, implemented if HDL generic VCS_MAILBOX bit is 1. UTMI-standard Vcontrol vector byte is sent by the UTMI controller (other side of TLL) to its PHY (emulated here by the TLL). Alternatively, data can be also written directly into the register. Can contain any user-defined data. Vcontrol bit changes can be used to assert the ULPI ALT interrupt. Lowest VCS_CTRL_WIDTH (HDL generic) bits are implemented, others are always-0, read-only. (UTMI standard is 4-bit).		
Type	RW		

7	6	5	4	3	2	1	0
VC							

Bits	Field Name	Description	Type	Reset
7:0	VC	User-defined UTMI Control data byte	RW	0x00

Table 23-1035. Register Call Summary for Register UTMI_VCONTROL_STATUS_i

High-Speed Multiport USB Host Subsystem

- USBTLLHS_ULPI Register Summary: [0]

Table 23-1036. UTMI_VCONTROL_LATCH_i

Address Offset	0x0000 0034 + (0x100 * i)	**Index**	i = 0 to 1
Physical Address	0x4A06 2834 + (0x100 * i)	**Instance**	USBTLLHS_ULPI
Description	Part of nonstandard UTMI-to-ULPI mailbox system, implemented if HDL generic VCS_MAILBOX bit is 1. Set by unmasked changes on the corresponding vcontrol_status bits to generate the ULPI ALT interrupt. Cleared upon read, and when low-power mode, serial mode or carkit mode are entered. Lowest VCS_CTRL_WIDTH (HDL generic) bits are implemented, others are always-0, read-only. (UTMI standard is 4-bit.)		
Type	R		

7	6	5	4	3	2	1	0
VC7_CHANGE	VC6_CHANGE	VC5_CHANGE	VC4_CHANGE	VC3_CHANGE	VC2_CHANGE	VC1_CHANGE	VC0_CHANGE

Bits	Field Name	Description	Type	Reset
7	VC7_CHANGE	Unmasked change on vcontrol_status bit	R	0
6	VC6_CHANGE	Unmasked change on vcontrol_status bit	R	0
5	VC5_CHANGE	Unmasked change on vcontrol_status bit	R	0
4	VC4_CHANGE	Unmasked change on vcontrol_status bit	R	0
3	VC3_CHANGE	Unmasked change on vcontrol_status bit	R	0
2	VC2_CHANGE	Unmasked change on vcontrol_status bit	R	0
1	VC1_CHANGE	Unmasked change on vcontrol_status bit	R	0
0	VC0_CHANGE	Unmasked change on vcontrol_status bit	R	0

Table 23-1037. Register Call Summary for Register UTMI_VCONTROL_LATCH_i

High-Speed Multiport USB Host Subsystem

- USBTLLHS_ULPI Register Summary: [0]

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Table 23-1038. UTMI_VSTATUS_i

Address Offset	0x0000 0035 + (0x100 * i)	**Index**	i = 0 to 1
Physical Address	0x4A06 2835 + (0x100 * i)	**Instance**	USBTLLHS_ULPI
Description	Part of nonstandard UTMI-to-ULPI mailbox system, implemented if HDL generic VCS_MAILBOX bit is 1. UTMI-standard Vstatus vector byte is sent by the PHY (emulated here by the TLL) to the UTMI controller (other side of TLL): information written into this register goes directly to the UTMI controller, and can contain any user-defined data. Read/write address. Lowest VCS_STAT_WIDTH (HDL generic) bits are implemented, others are always-0, read-only. (UTMI standard is 8-bit.)		
Type	RW		

7	6	5	4	3	2	1	0
VS							

Bits	Field Name	Description	Type	Reset
7:0	VS	User-defined UTMI status data byte	RW	0x00

Table 23-1039. Register Call Summary for Register UTMI_VSTATUS_i

High-Speed Multiport USB Host Subsystem

- USBTLLHS_ULPI Register Summary: [0]

Table 23-1040. UTMI_VSTATUS_SET_i

Address Offset	0x0000 0036 + (0x100 * i)	**Index**	i = 0 to 1
Physical Address	0x4A06 2836 + (0x100 * i)	**Instance**	USBTLLHS_ULPI
Description	Part of nonstandard UTMI-to-ULPI mailbox system, implemented if HDL generic VCS_MAILBOX bit is 1. UTMI-standard Vstatus vector byte is sent by the PHY (emulated here by the TLL) to the UTMI controller (other side of TLL): information written into this register goes directly to the UTMI controller, and can contain any user-defined data. Read/set address (write 1 to a bit to set it to 1, writing 0 has no effect on bit value). See field description at the read/write address of the same register.		
Type	RW		

7	6	5	4	3	2	1	0
VS							

Bits	Field Name	Description	Type	Reset
7:0	VS	User-defined UTMI status data byte Write 0x0: No effect on bit value Write 0x1: Set the bit to 1.	RW	0x00

Table 23-1041. Register Call Summary for Register UTMI_VSTATUS_SET_i

High-Speed Multiport USB Host Subsystem

- USBTLLHS_ULPI Register Summary: [0]

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Table 23-1042. UTMI_VSTATUS_CLR_i

Address Offset	0x0000 0037 + (0x100 * i)	**Index**	i = 0 to 1
Physical Address	0x4A06 2837 + (0x100 * i)	**Instance**	USBTLLHS_ULPI
Description	Part of nonstandard UTMI-to-ULPI mailbox system, implemented if HDL generic VCS_MAILBOX bit is 1. UTMI-standard Vstatus vector byte is sent by the PHY (emulated here by the TLL) to the UTMI controller (other side of TLL): information written into this register goes directly to the UTMI controller, and can contain any user-defined data. Read/clear address (write 1 to a bit to clear it to 0, writing 0 has no effect on bit value). See field description at the read/write address of the same register.		
Type	RW		

7	6	5	4	3	2	1	0
VS							

Bits	Field Name	Description	Type	Reset
7:0	VS	User-defined UTMI status data byte: Write 0x0: No effect on bit value Write 0x1: Clear the bit to 0.	RW	0x00

Table 23-1043. Register Call Summary for Register UTMI_VSTATUS_CLR_i

High-Speed Multiport USB Host Subsystem

- USBTLLHS_ULPI Register Summary: [0]

Table 23-1044. USB_INT_LATCH_NOCLR_i

Address Offset	0x0000 0038 + (0x100 * i)	**Index**	i = 0 to 1
Physical Address	0x4A06 2838 + (0x100 * i)	**Instance**	USBTLLHS_ULPI
Description	Set by unmasked changes on the corresponding status bits to generate the ULPI interrupt. Debug, nonstandard address to the standard register: Register is not cleared on read. See field description at the "clear-on-read" address of the same register.		
Type	R		

7	6	5	4	3	2	1	0
RESERVED			IDGND_LATCH	SESSEND_LATCH	SESSVALID_LATCH	VBUSVALID_LATCH	HOSTDISCONNECT_LATCH

Bits	Field Name	Description	Type	Reset
7:5	RESERVED	Reserved	R	0x0
4	IDGND_LATCH	Set to 1 by the PHY when an unmasked event occurs on IdGnd.	R	0x0
3	SESSEND_LATCH	Set to 1 by the PHY when an unmasked event occurs on SessEnd.	R	0x0
2	SESSVALID_LATCH	Set to 1 by the PHY when an unmasked event occurs on SessValid. SessValid is the same as UTMI+ AValid.	R	0x0
1	VBUSVALID_LATCH	Set to 1 by the PHY when an unmasked event occurs on VbusValid.	R	0x0

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Bits	Field Name	Description	Type	Reset
0	HOSTDISCONNECT_LATCH	Set to 1 by the PHY when an unmasked event occurs on Hostdisconnect. Applicable only in host mode.	R	0x0

Table 23-1045. Register Call Summary for Register USB_INT_LATCH_NOCLR_i

High-Speed Multiport USB Host Subsystem

- USBTLLHS_ULPI Register Summary: [0]

Table 23-1046. VENDOR_INT_EN_i

Address Offset	0x0000 003B + (0x100 * i)	**Index**	i = 0 to 1
Physical Address	0x4A06 283B + (0x100 * i)	**Instance**	USBTLLHS_ULPI
Description	Vendor-specific interrupt enables (mask) for miscellaneous ULPI alt_int events. Read/write address.		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED							P2P_EN

Bits	Field Name	Description	Type	Reset
7:1	RESERVED		R	0x00
0	P2P_EN	Enable PHY-to-PHY ULPI wakeup upon inactive UTMI suspendm. 0x0: PHY-to-PHY wakeup enabled 0x1: PHY-to-PHY wakeup enabled	RW	0

Table 23-1047. Register Call Summary for Register VENDOR_INT_EN_i

High-Speed Multiport USB Host Subsystem

- USBTLLHS_ULPI Register Summary: [0]

Table 23-1048. VENDOR_INT_EN_SET_i

Address Offset	0x0000 003C + (0x100 * i)	**Index**	i = 0 to 1
Physical Address	0x4A06 283C + (0x100 * i)	**Instance**	USBTLLHS_ULPI
Description	Vendor-specific interrupt enable bit (mask) for miscellaneous ULPI alt_int events. Read/set address (write 1 to a bit to set it to 1, writing 0 has no effect on bit value). See field description at the read/write address of the same register.		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED							P2P_EN

Bits	Field Name	Description	Type	Reset
7:1	RESERVED	Reserved	R	0x00
0	P2P_EN	Enable PHY-to-PHY ULPI wakeup upon inactive UTMI suspendm. Write 0x0: No effect on bit value Write 0x1: Set the bit to 1.	RW	0x0

Table 23-1049. Register Call Summary for Register VENDOR_INT_EN_SET_i

High-Speed Multiport USB Host Subsystem

- USBTLLHS_ULPI Register Summary: [0]

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Table 23-1050. VENDOR_INT_EN_CLR_i

Address Offset	0x0000 003D + (0x100 * i)	**Index**	i = 0 to 1
Physical Address	0x4A06 283D + (0x100 * i)	**Instance**	USBTLLHS_ULPI
Description	Vendor-specific interrupt enables (mask) for miscellaneous ULPI alt_int events. Read/clear address (write 1 to a bit to clear it to 0, writing 0 has no effect on bit value). See fields description at the read/write address of the same register.		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED							P2P_EN

Bits	Field Name	Description	Type	Reset
7:1	RESERVED	Reserved	R	0x00
0	P2P_EN	Enable PHY-to-PHY ULPI wakeup upon inactive UTMI suspendm. Write 0x0: No effect on bit value Write 0x1: Clear the bit to 0.	RW	0x0

Table 23-1051. Register Call Summary for Register VENDOR_INT_EN_CLR_i

High-Speed Multiport USB Host Subsystem

- USBTLLHS_ULPI Register Summary: [0]

Table 23-1052. VENDOR_INT_STATUS_i

Address Offset	0x0000 003E + (0x100 * i)	**Index**	i = 0 to 1
Physical Address	0x4A06 283E + (0x100 * i)	**Instance**	USBTLLHS_ULPI
Description	Vendor-specific interrupt sources for miscellaneous ULPI alt_int events		
Type	R		

7	6	5	4	3	2	1	0
RESERVED							UTMI_SUSPENDM

Bits	Field Name	Description	Type	Reset
7:1	RESERVED		R	0x00
0	UTMI_SUSPENDM	UTMI suspendm status (active-low), source of TLL PHY-to-PHY wake-up interrupt. Read 0x1: UTMI interface is active (not suspended). Read 0x0: UTMI interface is suspended.	R	1

Table 23-1053. Register Call Summary for Register VENDOR_INT_STATUS_i

High-Speed Multiport USB Host Subsystem

- USBTLLHS_ULPI Register Summary: [0]

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Table 23-1054. VENDOR_INT_LATCH_i

Address Offset	0x0000 003F + (0x100 * i)	**Index**	i = 0 to 1
Physical Address	0x4A06 283F + (0x100 * i)	**Instance**	USBTLLHS_ULPI
Description	Vendor-specific interrupt latches for miscellaneous ULPI alt_int events. Cleared upon read, and when low-power mode, serial mode or carkit mode are entered.		
Type	R		

7	6	5	4	3	2	1	0
RESERVED							P2P_LATCH

Bits	Field Name	Description	Type	Reset
7:1	RESERVED		R	0x00
0	P2P_LATCH	PHY-to-PHY ULPI wake-up event latch. Set when ULPI is in low-power mode (suspendm = 0) and UTMI is active (suspendm = 1). Read 0x1: PHY-to-PHY wake-up event was latched, ALT interrupt active. Read 0x0: No PHY-to-PHY wake-up event was latched.	R	0

Table 23-1055. Register Call Summary for Register VENDOR_INT_LATCH_i

High-Speed Multiport USB Host Subsystem
- USBTLLHS_ULPI Register Summary: [0]

23.11.6.4 HSUSBHOST Controller Registers

23.11.6.4.1 HSUSBHOST Controller Register Summary

Table 23-1056 summarizes the HSUSBHOST register mapping.

Table 23-1056. HSUSBHOST Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	Physical Address
UHH_REVISION	R	32	0x0000 0000	0x4A06 4000
UHH_HWINFO	R	32	0x0000 0004	0x4A06 4004
UHH_SYSCONFIG	RW	32	0x0000 0010	0x4A06 4010
UHH_SYSSTATUS	R	32	0x0000 0014	0x4A06 4014
UHH_HOSTCONFIG	RW	32	0x0000 0040	0x4A06 4040
UHH_DEBUG_CSR	RW	32	0x0000 0044	0x4A06 4044
UHH_SAR_CNTX_i (1)	RW	32	0x0000 0100 + (0x4 * i)	0x4A06 4100 + (0x4 * i)

(1) i = 0 to 383

CAUTION

The UHH_config registers are limited to 32-bit data accesses; 16-bit and 8-bit accesses are not allowed and can corrupt register content.

23.11.6.4.2 HSUSB Controller Register Description

Table 23-1057 through Table 23-1069 describe the HSUSB controller registers.

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Table 23-1057. UHH_REVISION

Address Offset	0x0000 0000		
Physical Address	0x4A06 4000	**Instance**	HSUSBHOST
Description	USB high-speed host (UHH) revision identifier (X.Y.R) Used by software to track features, bugs, and compatibility		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP revision	R	TI Internal data

Table 23-1058. Register Call Summary for Register UHH_REVISION

High-Speed Multiport USB Host Subsystem

- HSUSBHOST Controller Register Summary: [0]

Table 23-1059. UHH_HWINFO

Address Offset	0x0000 0004		
Physical Address	0x4A06 4004	**Instance**	HSUSBHOST
Description	Information on host hardware configuration		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						SAR_CNTX_SIZE									

Bits	Field Name	Description	Type	Reset
31:10	RESERVED		R	0x000000
9:0	SAR_CNTX_SIZE	Save-and-restore context size, in 32-bit words; that is, number of 32-bit registers with significant context information, mapped from offset 0x100 upward.	R	0x180

Table 23-1060. Register Call Summary for Register UHH_HWINFO

High-Speed Multiport USB Host Subsystem

- HSUSBHOST Controller Register Summary: [0]
- HSUSB Controller Register Description: [1]

Table 23-1061. UHH_SYSCONFIG

Address Offset	0x0000 0010		
Physical Address	0x4A06 4010	**Instance**	HSUSBHOST
Description	OCP standard system configuration register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																										STANDBYMODE		IDLEMODE		RESERVED	SOFTRESET

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Bits	Field Name	Description	Type	Reset
31:6	RESERVED		R	0x0000000
5:4	STANDBYMODE	Mstandby/Mwait/[Mwakeup] initiator power-management interface configuration 0x0: Force-standby mode. Mstandby asserted unconditionally. Asynchronous (master) wake-up disabled. 0x1: No-standby mode. Mstandby never asserted. Asynchronous (master) wakeup disabled. 0x2: Smart-standby mode. Mstandby asserted when initiator activity stops. Asynchronous (master) wake-up disabled. 0x3: Smart-standby + wake-up mode, like smart mode with asynchronous (master) wakeup enabled.	RW	0x0
3:2	IDLEMODE	Sidlereq/Sidleack(1:0)/[Swakeup] target power management interface configuration. 0x0: Force-Idle mode. Sidleack asserted after Idlereq assertion. Asynchronous (slave) wake-up disabled. 0x1: No-idle mode. Sidleack never asserted. Asynchronous (slave) wakeup disabled. 0x2: Smart-idle mode. Sidleack asserted upon Idlereq assertion, after target activity is over. Asynchronous (slave) wake-up disabled. 0x3: Smart-idle wake-up mode. Like smart mode with asynchronous (slave) wakeup enabled.	RW	0x2
1	RESERVED		R	0
0	SOFTRESET	Module software reset Read 0x0: No reset pending Write 0x0: No effect Write 0x1: Starts softreset sequence. Read 0x1: Reset (soft or other) is pending.	RW	0

Table 23-1062. Register Call Summary for Register UHH_SYSCONFIG

High-Speed Multiport USB Host Subsystem

- HS USB Host Controller Software Reset: [0]
- HS USB Host Controller Power Management: [1] [2]
- HS Multiport USB Host Subsystem Global Initialization: [3]
- HSUSBHOST Controller Register Summary: [4]

Table 23-1063. UHH_SYSSTATUS

Address Offset	0x0000 0014		
Physical Address	0x4A06 4014	**Instance**	HSUSBHOST
Description	Module-specific system status		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													EHCI_RESETDONE	OHCI_RESETDONE	RESERVED

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Bits	Field Name	Description	Type	Reset
31:3	RESERVED		R	0x0000 0000
2	EHCI_RESETDONE	Indicates when the EHCI HS host is out of reset Read 0x0: Out of reset Read 0x1: Under reset	R	1
1	OHCI_RESETDONE	Indicates when the OHCI FS/LS host is out of reset Read 0x0: Out of reset Read 0x1: Under reset	R	1
0	RESERVED		R	0

Table 23-1064. Register Call Summary for Register UHH_SYSSTATUS

High-Speed Multiport USB Host Subsystem

- HS Multiport USB Host Subsystem Global Initialization: [0] [1]
- HSUSBHOST Controller Register Summary: [2]

Table 23-1065. UHH_HOSTCONFIG

Address Offset	0x0000 0040		
Physical Address	0x4A06 4040	**Instance**	HSUSBHOST
Description	Static configuration of the USB HS host		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
APP_START_CLK	RESERVED											P2_MODE		P1_MODE		RESERVED						P2_CONNECT_STATUS	P1_CONNECT_STATUS	RESERVED		ENA_INCR_ALIGN	ENA_INCR16	ENA_INCR8	ENA_INCR4	AUTOPPD_ON_OVERCUR_EN	RESERVED

Bits	Field Name	Description	Type	Reset
31	APP_START_CLK	When the OHCI clocks are suspended, the system must assert this signal to start the clocks (12 and 48 MHz). This must be deasserted after the clocks are started and before the host is suspended again. (Host is suspended means HCFS = SUSPEND or all the OHCI ports are suspended.)	RW	0
30:20	RESERVED		R	0X000
19:18	P2_MODE	Port 2 interface configuration. Each bit corresponds to an internal "strap" signal, and output: Bit 0 = ulpi_bypass Bit 1 = hsic_en 0x0: To external ULPI PHY, HS only 0x1: To UTMI PHY (or ULPI TLL), FS/LS capable 0x2: Forbidden 0x3: To HSIC digital front-end (DFE), HS only	RW	0x0

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Bits	Field Name	Description	Type	Reset
17:16	P1_MODE	Port 1 interface configuration. Each bit corresponds to an internal "strap" signal, and output: Bit 0 = ulpi_bypass Bit 1 = hsic_en 0x0: To external ULPI PHY, HS only 0x1: To UTMI PHY (or ULPI TLL), FS/LS capable 0x2: Forbidden 0x3: To HSIC digital front-end (DFE), HS only	RW	0x0
15:10	RESERVED		R	0x00
9	P2_CONNECT_STATUS	Connection status for port 2 Read 0x0: Disconnected Read 0x1: Peripheral connected and active on port	R	0x0
8	P1_CONNECT_STATUS	Connection status for port 1 Read 0x0: Disconnected Read 0x1: Peripheral connected and active on port	R	0x0
7:6	RESERVED		R	0x0
5	ENA_INCR_ALIGN	Force alignment of bursts to the respective burst-size boundaries(1) 0x0: Disable burst type 0x1: Enable burst type	RW	0
4	ENA_INCR16	Control the use of INCR16-type bursts (in AHB sense) 0x0: Disable burst type 0x1: Enable burst type	RW	1
3	ENA_INCR8	Control the use of INCR8-type bursts (in AHB sense) 0x0: Disable burst type 0x1: Enable burst type	RW	1
2	ENA_INCR4	Control the use of INCR4-type bursts (in AHB sense) 0x0: Disable burst type 0x1: Enable burst type	RW	1
1	AUTOPPD_ON_OVERCUR_EN	Configure reaction upon port overcurrent condition. This function is not supported at the device level. 0x0: Port remains on upon overcurrent. 0x1: Port is powered down automatically upon overcurrent.	RW	0X0
0	RESERVED		R	0

(1) This bit must be set to 1 to avoid buffer underflow.

Table 23-1066. Register Call Summary for Register UHH_HOSTCONFIG

High-Speed Multiport USB Host Subsystem

- HS USB Host Controller Port Status: [0] [1]
- HS USB Host Controller Burst Control: [2] [3]
- UTMI Interface: [4] [5] [6]
- ULPI Interface: [7] [8]
- Operational Modes Configuration (Selecting and Configuring USB Connectivity): [9]
- HSUSBHOST Controller Register Summary: [10]

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Table 23-1067. UHH_DEBUG_CSR

Address Offset	0x0000 0044		
Physical Address	0x4A06 4044	**Instance**	HSUSBHOST
Description	Debug control and status for the EHCI, OHCI hosts		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													OHCI_CCS_2	OHCI_CCS_1	OHCI_GLOBALSUSPEND	RESERVED								OCHI_CNTSEL	EHCI_SIMULATION_MODE	EHCI_FLADJ						

Bits	Field Name	Description	Type	Reset
31:19	RESERVED	Reserved	R	0x000
18	OHCI_CCS_2	Current connect status of port 2 Read 0x0: No peripheral connected Read 0x1: Peripheral connected	R	0
17	OHCI_CCS_1	Current connect status of port 1 Read 0x0: No peripheral connected Read 0x1: Peripheral connected	R	0
16	OHCI_GLOBALSUSPEND	OHCI global suspend status, asserted 5 ms after the suspend order. Read 0x0: Host is not suspended. Read 0x1: Host is suspended.	R	0
15:8	RESERVED		R	0x00
7	OCHI_CNTSEL	Selection of a shorter "1 ms" counter in OHCI host, to speed up long USB phases such as reset, resume, etc. (used only for simulation) 0x0: Functional mode, 1ms = 12,000 × 12 MHz cycles 0x1: Simulation mode, 1ms = 7 × 12 MHz cycles = 583 ns	RW	0
6	EHCI_SIMULATION_MODE	Sets the PHY to nondriving mode (used only for simulation) 0x0: Functional mode 0x1: PHY set to nondriving	RW	0
5:0	EHCI_FLADJ	EHCI host frame length adjust. Modify only when EHCI Bit Field USBSTS.HCHalted = 1 Field value + 59,488 = 60,000 by default = Number of 60-MHz UTMI/ULPI clock cycles per 1 ms USB frame = Number of 480-MHz HS bits per 125 µs HS USB microframe	RW	0x20

Table 23-1068. Register Call Summary for Register UHH_DEBUG_CSR

High-Speed Multiport USB Host Subsystem

- HSUSBHOST Controller Register Summary: [0]

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Table 23-1069. UHH_SAR_CNTX_i

Address Offset	0x0000 0100 + (0x4 * i)	**Index**	i = 0 to 383
Physical Address	0x4A06 4100 + (0x4 * i)	**Instance**	HSUSBHOST
Description	Save and restore context array. Array size is indicated in UHH_HWINFO. When in SAR mode, read out to save and write to restore. Do not access when not in SAR mode.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CNTX																															

Bits	Field Name	Description	Type	Reset
31:0	CNTX	Context bits	RW	0x0000 0000

Table 23-1070. Register Call Summary for Register UHH_SAR_CNTX_i

High-Speed Multiport USB Host Subsystem

- HSUSBHOST Controller Register Summary: [0]

23.11.6.5 OHCI Registers

23.11.6.5.1 OHCI Register Summary

Table 23-1071 summarizes the OHCI register mapping.

Table 23-1071. OHCI Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	Physical Address
HCREVISION	R	32	0x0000 0000	0x4A06 4800
HCCONTROL	RW	32	0x0000 0004	0x4A06 4804
HCCOMMANDSTATUS	RW	32	0x0000 0008	0x4A06 4808
HCINTERRUPTSTATUS	RW	32	0x0000 000C	0x4A06 480C
HCINTERRUPTENABLE	RW	32	0x0000 0010	0x4A06 4810
HCINTERRUPTDISABLE	RW	32	0x0000 0014	0x4A06 4814
HCHCCA	RW	32	0x0000 0018	0x4A06 4818
HCPERIODCURRENTED	R	32	0x0000 001C	0x4A06 481C
HCCONTROLHEADED	RW	32	0x0000 0020	0x4A06 4820
HCCONTROLCURRENTED	RW	32	0x0000 0024	0x4A06 4824
HCBULKHEADED	RW	32	0x0000 0028	0x4A06 4828
HCBULKCURRENTED	RW	32	0x0000 002C	0x4A06 482C
HCDONEHEAD	R	32	0x0000 0030	0x4A06 4830
HCFMINTERVAL	RW	32	0x0000 0034	0x4A06 4834
HCFMREMAINING	R	32	0x0000 0038	0x4A06 4838
HCFMNUMBER	R	32	0x0000 003C	0x4A06 483C
HCPERIODICSTART	RW	32	0x0000 0040	0x4A06 4840
HCLSTHRESHOLD	RW	32	0x0000 0044	0x4A06 4844
HCRHDESCRIPTORA	RW	32	0x0000 0048	0x4A06 4848
HCRHDESCRIPTORB	RW	32	0x0000 004C	0x4A06 484C
HCRHSTATUS	RW	32	0x0000 0050	0x4A06 4850
HCRHPORTSTATUS_1	RW	32	0x0000 0054	0x4A06 4854
HCRHPORTSTATUS_2	RW	32	0x0000 0058	0x4A06 4858
RESERVED	RW	32	0x0000 005C	0x4A06 485C

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CAUTION

The high-speed USB registers are limited to 32-bit data accesses; 16-bit and 8-bit accesses are not allowed and can corrupt register content.

OHCI register descriptions conform to the OHCI USB standard: *Open Host Controller Interface Specification for USB, Release 1.0a*. For more information about these registers or for new specification releases, search OHCI on www.usb.org.

23.11.6.5.2 OHCI Register Description

Table 23-1072 through Table 23-1116 describe the OHCI registers.

Table 23-1072. HCREVISION

Address Offset	0x0000 0000		
Physical Address	0x4A06 4800	**Instance**	OHCI
Description	OHCI revision number		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								REV							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Reserved	R	0x000000
7:0	REV	OHCI specification revision the OHCI revision number upon which the USB host controller is based. Examples: 0x10 for 1.0, 0x21 for 2.1	R	0x10

Table 23-1073. Register Call Summary for Register HCREVISION

High-Speed Multiport USB Host Subsystem

- OHCI Register Summary: [0]

Table 23-1074. HCCONTROL

Address Offset	0x0000 0004		
Physical Address	0x4A06 4804	**Instance**	OHCI
Description	HC operating mode register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																					RWE	RWC	IR	HCFS		BLE	CLE	IE	PLE	CBSR	

Bits	Field Name	Description	Type	Reset
31:11	RESERVED	Reserved	R	0x000000
10	RWE	Remote wake-up enable This bit is used to enable or disable the remote wakeup feature upon detection of upstream resume signaling.	RW	0
9	RWC	Remote wake-up connected. This bit indicates whether the host controller supports remote wakeup signaling.	RW	0
8	IR	Interrupt routing	RW	0

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Bits	Field Name	Description	Type	Reset
		This bit determines the routing of interrupts generated by events registered in HCINTERRUPTSTATUS. 0x0: All interrupts are routed to the normal host bus interrupt mechanism.. 0x1: Interrupts are routed to the system management Interrupt.		
7:6	HCFS	Host controller functional state 0x0: HCFS: USB reset 0x1: HCFS: USB resume 0x2: HCFS: USB operational 0x3: HCFS: USB suspend	RW	0x0
5	BLE	Bulk list processing enable 0x0: Bulk ED list is not processed after the next SOF. 0x1: Enables processing of bulk ED list in the next frame.	RW	0
4	CLE	Control list processing enable 0x0: Control ED list is not processed after the next SOF. 0x1: Enables processing of control ED list in the next frame.	RW	0
3	IE	Isochronous ED processing enabled by host controller driver 0x0: Isochronous EDs are not processed. 0x1: Enables processing of isochronous EDs	RW	0
2	PLE	Periodic list enable 0x0: Periodic ED lists are not processed after the next frame. 0x1: Enables processing of periodic ED lists in the next frame.	RW	0
1:0	CBSR	Control/bulk service ratio. Specifies the ratio between control and bulk EDs processed in a frame. 0x0: One control ED per bulk ED 0x1: Two control ED per bulk ED 0x2: Three control ED per bulk ED 0x3: Four control ED per bulk ED	RW	0x0

Table 23-1075. Register Call Summary for Register HCCONTROL

High-Speed Multiport USB Host Subsystem

- OHCI Register Summary: [0]

Table 23-1076. HCCOMMANDSTATUS

Address Offset	0x0000 0008		
Physical Address	0x4A06 4808	**Instance**	OHCI
Description	HC command and status		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														SOC		RESERVED												OCR	BLF	CLF	HCR

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Bits	Field Name	Description	Type	Reset
31:18	RESERVED	Reserved	R	0x0000
17:16	SOC	Scheduling overrun count This is used to monitor any persistent scheduling problems. These bits are incremented on each scheduling overrun error. It is initialized to 0x0 and wraps around at 0x3.	R	0x0
15:4	RESERVED	Reserved	R	0x000
3	OCR	Ownership change request. This bit is set to request a change of control of the host controller.	RW	0
2	BLF	Bulk list filled This bit is used to indicate whether there are any TDs on the bulk list. It is set whenever it adds a TD to an ED in the bulk list.	RW	0
1	CLF	Control list filled This bit is used to indicate whether there are any TDs on the control list. It is set whenever it adds a TD to an ED in the control list.	RW	0
0	HCR	Host controller reset (software reset). Set this bit to initiate a USB host controller reset. This resets most USB host controller OHCI registers. OHCI register accesses must not be attempted until a read of this register returns a 0. 0x0: No effect 0x1: USB host controller is reset.	RW	0

Table 23-1077. Register Call Summary for Register HCCOMMANDSTATUS

High-Speed Multiport USB Host Subsystem

- OHCI Register Summary: [0]
- OHCI Register Description: [1]

Table 23-1078. HCINTERRUPTSTATUS

Address Offset	0x0000 000C		
Physical Address	0x4A06 480C	**Instance**	OHCI
Description	HC interrupt status		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	OC	RESERVED																						RHSC	FNO	UE	RD	SF	WDH	SO	

Bits	Field Name	Description	Type	Reset
31	RESERVED	Reserved	R	0
30	OC	Ownership change This bit is set when the HCCOMMANDSTATUS[3] OCR bit is set. Read 0x1: An ownership change has occurred. Write 0x0: No effect Write 0x1: Clears this bit	R	0
29:7	RESERVED	Reserved	R	0x000000

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Bits	Field Name	Description	Type	Reset
6	RHSC	Root hub status change When 0x1: A root hub status change has occurred. Write 0x0: No effect Write 0x1: Clears this bit	RW	0
5	FNO	Frame number overflow When 0x1: A frame number overflow has occurred. Write 0x0: No effect Write 0x1: Clears this bit	RW	0
4	UE	Unrecoverable error When 0x1: An unrecoverable error has occurred. Write 0x0: No effect Write 0x1: Clears this bit	RW	0
3	RD	Resume detected When 0x1: A downstream device has issued a resume request. Write 0x0: No effect Write 0x1: Clears this bit	RW	0
2	SF	Start of frame When 0x1: A SOF has been issued. Write 0x0: No effect Write 0x1: Clears this bit	RW	0
1	WDH	Write done head When 0x1: The USB host controller has updated the HCDONEHEAD register. Write 0x0: No effect Write 0x1: Clears this bit	RW	0
0	SO	Scheduling overrun When 0x1: A scheduling overrun has occurred. Write 0x0: No effect Write 0x1: Clears this bit	RW	0

Table 23-1079. Register Call Summary for Register HCINTERRUPTSTATUS

High-Speed Multiport USB Host Subsystem

- OHCI Register Summary: [0]
- OHCI Register Description: [1]

Table 23-1080. HCINTERRUPTENABLE

Address Offset	0x0000 0010		
Physical Address	0x4A06 4810	**Instance**	OHCI
Description	HC interrupt enable		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MIE	OC	RESERVED																						RHSC	FNO	UE	RD	SF	WDH	SO	

Bits	Field Name	Description	Type	Reset
31	MIE	Master interrupt enable When 0x1: Allows other enabled OHCI interrupt sources to propagate to the device interrupt controller When 0x0: OHCI interrupt sources are ignored. Write 0x0: No effect Write 0x1: Sets this bit	RW	0
30	OC	Ownership change Write 0x0: No effect Write 0x1: Enable interrupt generation due to ownership change.	RW	0

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Bits	Field Name	Description	Type	Reset
29:7	RESERVED	Reserved	R	0x000000
6	RHSC	Root hub status change When 0x1 and MIE is 0x1: Allows root hub status change interrupts to propagate to the device interrupt controller When 0x0 or MIE is 0x0: Root hub status change interrupts do not propagate. Write 0x0: No effect Write 0x1: Sets this bit	RW	0
5	FNO	Frame number overflow When 0x1 and MIE is 0x1: Allows FNO interrupts to propagate to the device interrupt controller When 0x0 or MIE is 0x0: FNO interrupts do not propagate. Write 0x0: No effect Write 0x1: Sets this bit	RW	0
4	UE	Unrecoverable error When 0x1 and MIE is 0x1: Allows UE interrupts to propagate to the device interrupt controller When 0x0 or MIE is 0x0: UE interrupts do not propagate. Write 0x0: No effect Write 0x1: Sets this bit	RW	0
3	RD	Resume detected When 0x1 and MIE is 0x1: Allows RD interrupts to propagate to the device interrupt controller When 0x0 or MIE is 0x0: RD interrupts do not propagate. Write 0x0: No effect Write 0x1: Sets this bit	RW	0
2	SF	Start of frame When 0x1 and MIE is 0x1: Allows SF interrupts to propagate to the device interrupt controller When 0x0 or MIE is 0x0: SF interrupts do not propagate. Write 0x0: No effect Write 0x1: Sets this bit	RW	0
1	WDH	Write done head When 0x1 and MIE is 0x1: Allows WDH interrupts to propagate to the device interrupt controller When 0x0 or MIE is 0x0: WDH interrupts do not propagate. Write 0x0: No effect Write 0x1: Sets this bit	RW	0
0	SO	Scheduling overrun When 0x1 and MIE is 0x1: Allows SO interrupts to propagate to the device interrupt controller When 0x0 or MIE is 0x0: SO interrupts do not propagate. Write 0x0: No effect Write 0x1: Sets this bit	RW	0

Table 23-1081. Register Call Summary for Register HCINTERRUPTENABLE

High-Speed Multiport USB Host Subsystem

- HS Multiport USB Host Subsystem Global Initialization: [0]
- OHCI Register Summary: [1]
- OHCI Register Description: [2] [3] [4] [5] [6] [7] [8] [9]

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Table 23-1082. HCINTERRUPTDISABLE

Address Offset	0x0000 0014		
Physical Address	0x4A06 4814	**Instance**	OHCI
Description	HC interrupt disable		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MIE	OC	RESERVED																						RHSC	FNO	UE	RD	SF	WDH	SO	

Bits	Field Name	Description	Type	Reset
31	MIE	Master interrupt enable Always reads 0x0. Write 0x0: No effect Write 0x1: Clears the HCINTERRUPTENABLE MIE bit	RW	0
30	OC	Ownership change. Write 0x0: No effect. Write 0x1: Disable interrupt generation due to ownership change.	RW	0
29:7	RESERVED	Reserved	R	0x000000
6	RHSC	Root hub status change Always reads 0x0. Write 0x0: No effect Write 0x1: Clears the HCINTERRUPTENABLE RHSC bit	RW	0
5	FNO	Frame number overflow Always reads 0x0. Write 0x0: No effect Write 0x1: Clears the HCINTERRUPTENABLE FNO bit	RW	0
4	UE	Unrecoverable error Always reads 0x0. Write 0x0: No effect Write 0x1: Clears the HCINTERRUPTENABLE UE bit	RW	0
3	RD	Resume detected Always reads 0x0. Write 0x0: No effect Write 0x1: Clears the HCINTERRUPTENABLE RD bit	RW	0
2	SF	Start of frame Always reads 0x0. Write 0x0: No effect Write 0x1: Clears the HCINTERRUPTENABLE SF bit	RW	0
1	WDH	Write done head Always reads 0x0. Write 0x0: No effect Write 0x1: Clears the HCINTERRUPTENABLE WDH bit	RW	0
0	SO	Scheduling overrun Always reads 0x0. Write 0x0: No effect Write 0x1: Clears the HCINTERRUPTENABLE SO bit	RW	0

Table 23-1083. Register Call Summary for Register HCINTERRUPTDISABLE

High-Speed Multiport USB Host Subsystem

- OHCI Register Summary: [0]

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Table 23-1084. HCHCCA

Address Offset	0x0000 0018		
Physical Address	0x4A06 4818	**Instance**	OHCI
Description	HC HCCA address register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HCCA																								RESERVED							

Bits	Field Name	Description	Type	Reset
31:8	HCCA	Physical address of the beginning of the HCCA	RW	0x000000
7:0	RESERVED	Reserved	R	0x00

Table 23-1085. Register Call Summary for Register HCHCCA

High-Speed Multiport USB Host Subsystem

- OHCI Register Summary: [0]

Table 23-1086. HCPERIODCURRENTED

Address Offset	0x0000 001C		
Physical Address	0x4A06 481C	**Instance**	OHCI
Description	HC current periodic register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PCED																														RESERVED	

Bits	Field Name	Description	Type	Reset
31:4	PCED	Physical address of current ED on the periodic ED list	R	0x0000000
3:0	RESERVED	Reserved	R	0x0

Table 23-1087. Register Call Summary for Register HCPERIODCURRENTED

High-Speed Multiport USB Host Subsystem

- OHCI Register Summary: [0]

Table 23-1088. HCCONTROLHEADED

Address Offset	0x0000 0020		
Physical Address	0x4A06 4820	**Instance**	OHCI
Description	HC head control register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHED																														RESERVED	

Bits	Field Name	Description	Type	Reset
31:4	CHED	Physical address of head ED on the control ED list	RW	0x0000000
3:0	RESERVED	Reserved	R	0x0

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Table 23-1089. Register Call Summary for Register HCCONTROLHEADED

High-Speed Multiport USB Host Subsystem

- OHCI Register Summary: [0]

Table 23-1090. HCCONTROLCURRENTED

Address Offset	0x0000 0024		
Physical Address	0x4A06 4824	**Instance**	OHCI
Description	HC current control register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CCED																												RESERVED			

Bits	Field Name	Description	Type	Reset
31:4	CCED	Physical address of current ED on the control ED list	RW	0x0000000
3:0	RESERVED	Reserved	R	0x0

Table 23-1091. Register Call Summary for Register HCCONTROLCURRENTED

High-Speed Multiport USB Host Subsystem

- OHCI Register Summary: [0]

Table 23-1092. HCBULKHEADED

Address Offset	0x0000 0028		
Physical Address	0x4A06 4828	**Instance**	OHCI
Description	HC head bulk register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BHED																												RESERVED			

Bits	Field Name	Description	Type	Reset
31:4	BHED	Physical address of head ED on the bulk ED list	RW	0x0000000
3:0	RESERVED	Reserved	R	0x0

Table 23-1093. Register Call Summary for Register HCBULKHEADED

High-Speed Multiport USB Host Subsystem

- OHCI Register Summary: [0]

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Table 23-1094. HCBULKCURRENTED

Address Offset	0x0000 002C		
Physical Address	0x4A06 482C	**Instance**	OHCI
Description	HC current bulk register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BCED																														RESERVED	

Bits	Field Name	Description	Type	Reset
31:4	BCED	Physical address of current ED on the bulk ED list	RW	0x0000000
3:0	RESERVED	Reserved	R	0x0

Table 23-1095. Register Call Summary for Register HCBULKCURRENTED

High-Speed Multiport USB Host Subsystem

- OHCI Register Summary: [0]

Table 23-1096. HCDONEHEAD

Address Offset	0x0000 0030		
Physical Address	0x4A06 4830	**Instance**	OHCI
Description	HC head done register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DH																														RESERVED	

Bits	Field Name	Description	Type	Reset
31:4	DH	Physical address of last TD that was added to the Done queue	R	0x0000000
3:0	RESERVED	Reserved	R	0x0

Table 23-1097. Register Call Summary for Register HCDONEHEAD

High-Speed Multiport USB Host Subsystem

- OHCI Register Summary: [0]
- OHCI Register Description: [1]

Table 23-1098. HCFMINTERVAL

Address Offset	0x0000 0034		
Physical Address	0x4A06 4834	**Instance**	OHCI
Description	HC frame interval register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIT	FSMPS															RESERVED	FI														

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Bits	Field Name	Description	Type	Reset
31	FIT	Frame interval toggle This bit is toggled whenever it loads a new value to FI.	RW	0
30:16	FSMPS	Largest data packet size for full-speed packets, bit times This field specifies a value which is loaded into the largest data packet counter at the beginning of each frame.	RW	0x0000
15:14	RESERVED	Reserved	R	0x0
13:0	FI	Frame interval. Number of 12-MHz clocks in the USB frame. The nominal value is set to 11,999, to give a 1-ms frame.	RW	0x2EDF

Table 23-1099. Register Call Summary for Register HCFMINTERVAL

High-Speed Multiport USB Host Subsystem

- OHCI Implementation Specifications: [0]
- OHCI Register Summary: [1]
- OHCI Register Description: [2] [3] [4]

Table 23-1100. HCFMREMAINING

Address Offset	0x0000 0038		
Physical Address	0x4A06 4838	**Instance**	OHCI
Description	HC frame remaining register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FRT	RESERVED															FR															

Bits	Field Name	Description	Type	Reset
31	FRT	Frame remaining toggle This bit is used for the synchronization between HCFMINTERVAL[13:0] FI and FR. This bit is loaded from the HCFMINTERVAL[31] FIT bit whenever FR reaches 0.	R	0
30:14	RESERVED	Reserved	R	0x00000
13:0	FR	Frame remaining This counter is decremented at each bit time. When it reaches 0, it is reset by loading the value of the USBHOST.HCFMINTERVAL[13:0] FI bit field at the next bit time boundary.	R	0x0000

Table 23-1101. Register Call Summary for Register HCFMREMAINING

High-Speed Multiport USB Host Subsystem

- OHCI Register Summary: [0]
- OHCI Register Description: [1]

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Table 23-1102. HCFMNUMBER

Address Offset	0x0000 003C		
Physical Address	0x4A06 483C	**Instance**	OHCI
Description	HC frame number register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																FN															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x0000
15:0	FN	Frame number This is incremented when HCFMREMAINING is reloaded. It is rolled over to 0x0000 after 0xFFFF.	R	0x0000

Table 23-1103. Register Call Summary for Register HCFMNUMBER

High-Speed Multiport USB Host Subsystem

- OHCI Register Summary: [0]

Table 23-1104. HCPERIODICSTART

Address Offset	0x0000 0040		
Physical Address	0x4A06 4840	**Instance**	OHCI
Description	HC periodic start register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								PS							

Bits	Field Name	Description	Type	Reset
31:14	RESERVED	Reserved	R	0x00000
13:0	PS	Periodic start. The host controller driver must program this value to be about 10 percent less than the frame interval field value so that control and bulk EDs have priority for the first 10 percent of the frame; then periodic EDs have priority for the remaining 90 percent of the frame.	RW	0x0000

Table 23-1105. Register Call Summary for Register HCPERIODICSTART

High-Speed Multiport USB Host Subsystem

- OHCI Register Summary: [0]

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Table 23-1106. HCLSTHRESHOLD

Address Offset	0x0000 0044		
Physical Address	0x4A06 4844	**Instance**	OHCI
Description	HC low-speed threshold register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				LST											

Bits	Field Name	Description	Type	Reset
31:12	RESERVED	Reserved	R	0x00000
11:0	LST	Low-speed threshold	RW	0x628

Table 23-1107. Register Call Summary for Register HCLSTHRESHOLD

High-Speed Multiport USB Host Subsystem

- OHCI Register Summary: [0]

Table 23-1108. HCRHDESCRIPTORA

Address Offset	0x0000 0048		
Physical Address	0x4A06 4848	**Instance**	OHCI
Description	HC root hub A register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
POTPG								RESERVED											NOCP	OCPM	DT	NPS	PSM	NDP							

Bits	Field Name	Description	Type	Reset
31:24	POTPG	Power-on to power-good time. Defines the minimum amount of time (2 ms * POTPG) between the USB host controller turning on power to a downstream port and when the USB host can access the downstream device.	RW	0x0A
23:13	RESERVED	Reserved	R	0x0
12	NOCP	No overcurrent protection. This function is not supported at the device level. 0x0: Overcurrent status is reported collectively for all downstream ports. 0x1: The USB host controller does not implement overcurrent protection inputs.	RW	0x0
11	OCPM	Overcurrent protection mode. This function is not supported at the device level.	RW	0x1
10	DT	Device type Always reads 0x0: Indicates that the USB host controller implemented is not a compound device.	R	0
9	NPS	No power switching 0x0: VBUS power switching is supported, either per-port or all-port switched per the power. 0x1: VBUS power switching is not supported; power is available to all downstream ports.	RW	0
8	PSM	Power switching mode 0x0: Indicates that all ports are powered at the same time 0x1: Individual port power switching is supported.	RW	1

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Bits	Field Name	Description	Type	Reset
7:0	NDP	Number of downstream ports These bits specify the number of downstream ports supported by the root hub. It is implementation-specific. The minimum number of ports is 1. The maximum number of ports supported by OHCI is 15.	R	0x03

Table 23-1109. Register Call Summary for Register HCRHDESCRIPTORA

High-Speed Multiport USB Host Subsystem

- OHCI Implementation Specifications: [0] [1] [2] [3]
- OHCI Register Summary: [4]

Table 23-1110. HCRHDESCRIPTORB

Address Offset	0x0000 004C		
Physical Address	0x4A06 484C	**Instance**	OHCI
Description	HC root hub B register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PPCM																DR															

Bits	Field Name	Description	Type	Reset
31:16	PPCM	Port power control mask. Each bit defines whether a corresponding downstream port has port power controlled by the global power control. When set, the port's power state is only affected by per-port power control. When cleared, the port is controlled by the global power switch. If the device is configured to global switch mode this field is not valid. Bit 0: Reserved, bit 1: Ganged-power mask on port 1, ..., bit 15: Ganged-power mask on port 15.	RW	0x0000
15:0	DR	Device removable. Each bit defines whether a corresponding downstream port has a removable device. When cleared, the attached device is removable. When set, the attached device is not removable. Bit 0: Reserved, bit 1: Device attached to port 1, , bit 15: Device attached to port 15.	RW	0x0000

Table 23-1111. Register Call Summary for Register HCRHDESCRIPTORB

High-Speed Multiport USB Host Subsystem

- OHCI Implementation Specifications: [0] [1]
- OHCI Register Summary: [2]
- OHCI Register Description: [3] [4] [5] [6]

Table 23-1112. HCRHSTATUS

Address Offset	0x0000 0050		
Physical Address	0x4A06 4850	**Instance**	OHCI
Description	HC root hub status register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CRWE	RESERVED														LPSC	DRWE	RESERVED														LPS

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Bits	Field Name	Description	Type	Reset
31	CRWE	Clear remote wakeup enable Write 0x0: No effect Write 0x1: Clears the device remote wake-up enable bit	W	0
30:17	RESERVED	Reserved	R	0x0000
16	LPSC	Local power status change Always reads 0x0: The root hub does not support the local power status feature. Write 0x0: No effect Write 0x1: Sets port power status bits for all ports, if power switching mode is 0. Sets port power status bits for ports with their corresponding port power control mask bits cleared if power switching mode is 1.	RW	0
15	DRWE	Device remote wake-up enable. Enables a connect status change event as a resume event, causing a USB suspend to USB resume state transition and sets the resume detected interrupt status bit. Read 0x1: Connect status change is a remote wake-up event. Read 0x0: Connect status change is not a remote wake-up event. Write 0x0: No effect Write 0x1: Sets the device remote wake-up enable bit	RW	0
14:1	RESERVED	Reserved	R	0x0000
0	LPS	Local power status Always reads 0x0 Write 0x0: No effect Write 0x1: When in global power mode (power switching mode = 0), turns off power to all ports. If in per-port power mode (power switching mode = 1), turns of power to those ports whose corresponding port power control mask bit is 0.	RW	0

Table 23-1113. Register Call Summary for Register HCRHSTATUS

High-Speed Multiport USB Host Subsystem

- OHCI Register Summary: [0]

Table 23-1114. HCRHPORTSTATUS_1

Address Offset	0x0000 0054		
Physical Address	0x4A06 4854	**Instance**	OHCI
Description	HC port 1 status and control register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											PRSC	RESERVED	PSSC	PESC	CSC	RESERVED							LSDA_CPP	PPS_SPP	RESERVED			PRS_SPR	RESERVED	PSS_SPS	PES_SPE	CCS_CPE

Bits	Field Name	Description	Type	Reset
31:21	RESERVED	Reserved	R	0x000
20	PRSC	Port 1 reset status change. This bit is set when the port 1 port reset status bit has changed. Write 0x0: No effect Write 0x1: Clears this bit	RW	0
19	RESERVED		R	0

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Bits	Field Name	Description	Type	Reset
18	PSSC	Port 1 suspends status change. Set when the port leaves the suspend state; that is, after the full resume sequence has completed. Write 0x0: No effect Read 0x0: No resume completed (since either the last software clear, or the last port reset). Read 0x1: Resume completed on the port Write 0x1: Clears the bit	RW	0
17	PESC	Port 1 enable status change. This bit is set when the port 1 port enable status has changed. Write 0x0: No effect Write 0x1: Clears this bit	RW	0
16	CSC	Port 1 connect status change. This bit is set when the port1 port current connect status has changed due to a connect or disconnect event. If current connect status is 0 when a set port reset, set port enable, or set port suspend write occurs, this bit is set. Write 0x0: No effect Write 0x1: Clears this bit **Note:** If the HCRHDESCRIPTORB[1] DR bit is set, this bit is set only after a root hub reset to inform the system that the device is attached.	RW	0
15:10	RESERVED	Reserved	R	0x00
9	LSDA_CPP	Port 1 low-speed device attached/clear port power. This bit is valid only when port 1 current connect status is 1. Read 0x0: A full-speed device is attached to port 1. Read 0x1: A low-speed device is attached to port 1. Write 0x0: No effect Write 0x1: Clears the port 1 port power status	RW	0
8	PPS_SPP	Port 1 port power status/set port power Read 0x0: Port 1 power is enabled. Read 0x1: Port 1 power is not enabled. Write 0x0: No effect Write 0x1: Sets the port 1 port power status bit	RW	0
7:5	RESERVED	Reserved	R	0x0
4	PRS_SPR	Port 1 port reset status/set port reset Read 0x0: USB reset is not being sent to port 1. Read 0x1: Port 1 is signaling the USB reset. Write 0x0: No effect Write 0x1: Sets the port 1 port reset status bit and causes the USB host controller to begin signaling USB reset to port 1	RW	0
3	RESERVED		R	0
2	PSS_SPS	Port 1 port suspend status/set port suspend. This bit is cleared automatically at the end of the USB resume sequence and also at the end of the USB reset sequence. Write 0x0: No effect Read 0x0: Port 1 is not in the USB suspend state. Read 0x1: Port 1 is in the USB suspend state or is in the resume sequence. Write 0x1: If port 1 current connect status is 1, sets the port 1 port suspend status bit and places port 1 in USB suspend state. If current connect status is 0, sets instead connect status change to inform the USB host controller driver of an attempt to suspend a disconnected port.	RW	0

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Bits	Field Name	Description	Type	Reset
1	PES_SPE	Port 1 port enable status/set port enable. This bit is automatically set at completion of port 1 USB reset if it was not already set before the USB reset completed, and is automatically set at the end of a USB suspend if the port was not enabled when the USB resume completed. Read 0x0: Port 1 is not enabled. Read 0x1: Port 1 is enabled. Write 0x0: No effect Write 0x1: When port 1 current connect status is 1 sets the port 1 port enable status bit. When port 1 current status is 0 has no effect.	RW	0
0	CCS_CPE	Port 1 current connection status/clear port enable Read 0x0: No USB device is attached to port 1. Read 0x1: A USB device is currently attached to port 1. Write 0x0: No effect Write 0x1: Clears the port 1 port enable bit Note: This bit is set to 1 if the HCRHDESCRIPTORB[1 DR bit] is set to indicate a nonremovable device on port 1.	RW	0

Table 23-1115. Register Call Summary for Register HCRHPORTSTATUS_1

High-Speed Multiport USB Host Subsystem

- OHCI Register Summary: [0]

Table 23-1116. HCRHPORTSTATUS_2

Address Offset	0x0000 0058		
Physical Address	0x4A06 4858	**Instance**	OHCI
Description	HC port 2 status and control register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											PRSC	RESERVED	PSSC	PESC	CSC	RESERVED							LSDA_CPP	PPS_SPP	RESERVED			PRS_SPR	RESERVED	PSS_SPS	PES_SPE	CCS_CPE

Bits	Field Name	Description	Type	Reset
31:21	RESERVED	Reserved	R	0x000
20	PRSC	Port 2 reset status change. This bit is set when the port 2 port reset status bit has changed. Write 0x0: No effect Write 0x1: Clears this bit	RW	0
19	RESERVED		RW	0
18	PSSC	Port 2 suspend status change. Set when the port leaves the suspend state; that is, after the full resume sequence has completed. Write 0x0: No effect Read 0x0: No resume completed (since either the last software clear, or the last port reset). Read 0x1: Resume completed on the port. Write 0x1: Clears the bit	RW	0
17	PESC	Port 2 enable status change. This bit is set when the port 2 port enable status has changed. Write 0x0: No effect Write 0x1: Clears this bit	RW	0

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Bits	Field Name	Description	Type	Reset
16	CSC	Port 2 connect status change. This bit is set when the port 2 port current connect status has changed due to a connect or disconnect event. If current connect status is 0 when a set port reset, set port enable, or set port suspend write occurs, this bit is set. Write 0x0: No effect Write 0x1: Clears this bit **Note:** If the HCRHDESCRIPTORB[1] DR bit is set, this bit is set only after a root hub reset to inform the system that the device is attached.	RW	0
15:10	RESERVED	Reserved	R	0x00
9	LSDA_CPP	Port 2 low-speed device attached/clear port power. This bit is valid only when port 2 current connect status is 1. Read 0x0: A full-speed device is attached to port 2. Read 0x1: A low-speed device is attached to port 2. Write 0x0: No effect Write 0x1: Clears the port 2 port power status	RW	0
8	PPS_SPP	Port 2 port power status/set port power Read 0x0: Port 2 power is enabled. Read 0x1: Port 2 power is not enabled. Write 0x0: No effect Write 0x1: Sets the port 2 port power status bit	RW	0
7:5	RESERVED	Reserved	R	0x0
4	PRS_SPR	Port 2 port reset status/set port reset Read 0x0: USB reset is not being sent to port 2. Read 0x1: Port 2 is signaling the USB reset. Write 0x0: No effect Write 0x1: Sets the port 2 port reset status bit and causes the USB host controller to begin signaling USB reset to port 2	RW	0
3	RESERVED		RW	0
2	PSS_SPS	Port 2 port suspend status/set port suspend. This bit is cleared automatically at the end of the USB resume sequence and also at the end of the USB reset sequence. Write 0x0: No effect Read 0x0: Port 2 is not in the USB suspend state. Read 0x1: Port 2 is in the USB suspend state or is in the resume sequence. Write 0x1: If port 2 current connect status is 1, sets the port 2 port suspend status bit and places port 2 in USB suspend state. If current connect status is 0, sets instead connect status change to inform the USB host controller driver of an attempt to suspend a disconnected port.	RW	0
1	PES_SPE	Port 2 port enable status/set port enable. This bit is automatically set at completion of port 2 USB reset if it was not already set before the USB reset completed, and is automatically set at the end of a USB suspend if the port was not enabled when the USB resume completed. Read 0x0: Port 2 is not enabled. Read 0x1: Port 2 is enabled. Write 0x0: No effect Write 0x1: When port 2 current connect status is 1 sets the port 2 port enable status bit. When port 2 current status is 0 has no effect.	RW	0
0	CCS_CPE	Port 2 current connection status/clear port enable Read 0x0: No USB device is attached to port 2. Read 0x1: A USB device is currently attached to port 2. Write 0x0: No effect Write 0x1: Clears the port 2 port enable bit **Note:** This bit is set to 1 if the HCRHDESCRIPTORB[1] DR bit is set to indicate a nonremovable device on port 2.	RW	0

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Table 23-1117. Register Call Summary for Register HCRHPORTSTATUS_2

High-Speed Multiport USB Host Subsystem
- OHCI Register Summary: [0]

23.11.6.6 EHCI Registers

23.11.6.6.1 EHCI Register Summary

Table 23-1118 summarizes the EHCI register mapping.

Table 23-1118. EHCI Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	Physical Address
HCCAPBASE	R	32	0x0000 0000	0x4A06 4C00
HCSPARAMS	R	32	0x0000 0004	0x4A06 4C04
HCCPARAMS	R	32	0x0000 0008	0x4A06 4C08
USBCMD	RW	32	0x0000 0010	0x4A06 4C10
USBSTS	RW	32	0x0000 0014	0x4A06 4C14
USBINTR	RW	32	0x0000 0018	0x4A06 4C18
FRINDEX	RW	32	0x0000 001C	0x4A06 4C1C
CTRLDSSEGMENT	R	32	0x0000 0020	0x4A06 4C20
PERIODICLISTBASE	RW	32	0x0000 0024	0x4A06 4C24
ASYNCLISTADDR	RW	32	0x0000 0028	0x4A06 4C28
CONFIGFLAG	RW	32	0x0000 0050	0x4A06 4C50
PORTSC_i (1)	RW	32	0x0000 0054 + (0x4 * i)	0x4A06 4C54 + (0x4 * i)
INSNREG00	RW	32	0x0000 0090	0x4A06 4C90
INSNREG01	RW	32	0x0000 0094	0x4A06 4C94
INSNREG02	RW	32	0x0000 0098	0x4A06 4C98
INSNREG03	RW	32	0x0000 009C	0x4A06 4C9C
INSNREG04	RW	32	0x0000 00A0	0x4A06 4CA0
INSNREG05_UTMI	RW	32	0x0000 00A4	0x4A06 4CA4
INSNREG05_ULPI	RW	32	0x0000 00A4	0x4A06 4CA4
INSNREG06	RW	32	0x0000 00A8	0x4A06 4CA8
INSNREG07	R	32	0x0000 00AC	0x4A06 4CAC
INSNREG08	RW	32	0x0000 00B0	0x4A06 4CB0

(1) i = 0 to 2

CAUTION

The high-speed USB registers are limited to 32-bit data accesses; 16-bit and 8-bit accesses are not allowed and can corrupt register content.

EHCI register descriptions conform to the EHCI USB standard: *Enhanced Host Controller Interface (EHCI) Specification for USB, Release 1.1*. For more information about these registers or for new specification releases, search EHCI on www.usb.org.

23.11.6.6.2 EHCI Register Description

Table 23-1119 through Table 23-1161 describe the EHCI registers.

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Table 23-1119. HCCAPBASE

Address Offset	0x0000 0000		
Physical Address	0x4A06 4C00	**Instance**	EHCI
Description	Host controller capability register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HCIVERSION																RESERVED								CAPLENGTH							

Bits	Field Name	Description	Type	Reset
31:16	HCIVERSION	Interface version number. It contains a BCD encoding of the EHCI revision number supported by this host controller. [7:4] Major revision [3:0] Minor revision	R	0x0100
15:8	RESERVED	Reserved	R	0x00
7:0	CAPLENGTH	Capability register length	R	0x10

Table 23-1120. Register Call Summary for Register HCCAPBASE

High-Speed Multiport USB Host Subsystem

- EHCI Register Summary: [0]

Table 23-1121. HCSPARAMS

Address Offset	0x0000 0004		
Physical Address	0x4A06 4C04	**Instance**	EHCI
Description	Host controller structural parameters		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												RESERVED			P_INDICATOR	N_CC				N_PCC			PRR	RESERVED			PPC	N_PORTS		

Bits	Field Name	Description	Type	Reset
31:20	RESERVED	Reserved	R	0x000
19:17	RESERVED	Reserved	R	0x0
16	P_INDICATOR	Port indicator support indication This bit indicates whether the ports support port indicator control. 0x1: The port status and control registers include a read/write field for controlling the state of the port indicator.	R	0
15:12	N_CC	Number of companion controllers This field indicates the number of companion controllers associated with this USB 2.0 host controller. 0x0: There are no companion host controllers. Port-ownership hand-off is not supported. Only high-speed devices are supported on the host controller root ports.	R	0x1

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Bits	Field Name	Description	Type	Reset
		Others: There are companion USB 1.1 host controller(s). Port-ownership hand-off is supported. High-, full-, and low-speed devices are supported on the host controller root ports.		
11:8	N_PCC	Number of ports per companion controller This field indicates the number of ports supported per companion host controller. It is used to indicate the port routing configuration to system software. For example, if N_PORTS has a value of 6 and N_CC has a value of 2, then N_PCC can have a value of 3. The convention is that the first N_PCC ports are assumed to be routed to companion controller 1, the next N_PCC ports to companion controller 2, etc. The number in this field must be consistent with N_PORTS and N_CC.	R	0x3
7	PRR	Port routing rules The first N_PCC ports are routed to the lowest-numbered function companion host controller, the next N_PCC ports are routed to the next lowest-function companion controller, and so on.	R	0
6:5	RESERVED	Reserved	R	0x0
4	PPC	Port power control This field indicates whether the host controller implementation includes port power control. 0x0: The ports do not have port power switches. 0x1: The ports have port power switches.	R	1
3:0	N_PORTS	Number of downstream ports This field specifies the number of physical downstream ports implemented on this host controller.	R	0x3

Table 23-1122. Register Call Summary for Register HCSPARAMS

High-Speed Multiport USB Host Subsystem

- EHCI Register Summary: [0]
- EHCI Register Description: [1] [2] [3]

Table 23-1123. HCCPARAMS

Address Offset	0x0000 0008		
Physical Address	0x4A06 4C08	**Instance**	EHCI
Description	Host controller capability parameters		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														LPM	RESERVED	EECP								IST				RESERVED	ASPC	PFLF	BIT64AC

Bits	Field Name	Description	Type	Reset
31:18	RESERVED	Reserved	R	0x0000
17	LPM	Link power management capability 0: Link power management not supported 1: Link power management supported	R	1
16	RESERVED	Reserved	R	0

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Bits	Field Name	Description	Type	Reset
15:8	EECP	EHCI extended capabilities pointer This field indicates the existence of a capabilities list. 0x0: No extended capabilities are implemented. Others: The offset in PCI configuration space of the first EHCI extended capability.	R	0x00
7:4	IST	Isochronous scheduling threshold This field indicates where software can reliably update the isochronous schedule in relation to the current position of the executing host controller. The host controller can hold one microframe of isochronous data structures before flushing the state.	R	0x1
3	RESERVED	Reserved	R	0
2	ASPC	Asynchronous schedule park capability 0x1: The host controller supports the park feature for high-speed queue heads in the asynchronous schedule. The feature can be disabled or enabled and set to a specific level by using the USBHOST.USBCMD[11]ASPME bit and the USBHOST.USBCMD[9:8] ASPMC bit field.	R	1
1	PFLF	Programmable frame list flag 0x0: System software must use a frame list length of 1024 elements with this host controller. 0x1: System software can specify and use a smaller frame list and configure the host controller through the USBHOST.USBCMD[3:2] FLS bit field. The frame list must always be aligned on a 4-K page boundary.	R	1
0	BIT64AC	64-bit addressing capability This field documents the addressing range capability of this implementation. 0x0: Data structures using 32-bit address memory pointers 0x1: Data structures using 64-bit address memory pointers	R	0

Table 23-1124. Register Call Summary for Register HCCPARAMS

High-Speed Multiport USB Host Subsystem

- EHCI Register Summary: [0]
- EHCI Register Description: [1]

Table 23-1125. USBCMD

Address Offset	0x0000 0010		
Physical Address	0x4A06 4C10	**Instance**	EHCI
Description	USB command		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				HIRD				ITC								RESERVED				ASPME	RESERVED		ASPMC	LHCR	IAAD	ASE	PSE	FLS		HCR	RS

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Bits	Field Name	Description	Type	Reset
31:28	RESERVED	Reserved	R	0x0
27:24	HIRD	Host-initiated resume duration. If LPM is enabled, this field is RW; otherwise, it is R. The minimum for K-state during resume from LPM: 0x0: 50 µs Each increment adds 75 µs.	RW	0x0
23:16	ITC	Interrupt threshold control This field is used by the system software to select the maximum rate at which the host controller issues interrupts. The only valid values are defined below. If software writes an invalid value to this register, the results are undefined. 0x00: Reserved 0x01: 1 microframe 0x02: 2 microframes 0x04: 4 microframes 0x08: 8 microframes (default, equates to 1 ms) 0x10: 16 microframes (2 ms) 0x20: 32 microframes (4 ms) 0x40: 64 microframes (8 ms) Others: Undefined	RW	0x08
15:12	RESERVED	Reserved	R	0x0
11	ASPME	Asynchronous schedule park mode enable 0x0: Park mode is disabled. 0x1: Park mode is enabled.	RW	1
10	RESERVED	Reserved	R	0
9:8	ASPMC	Asynchronous schedule park mode count It contains a count of the number of successive transactions the host controller is allowed to execute from a high-speed queue head on the asynchronous schedule before continuing traversal of the asynchronous schedule. Valid values are 0x1 to 0x3. Software must not write 0 to this bit when park mode enable is 1 because this may result in undefined behavior.	RW	0x3
7	LHCR	Light host controller reset It allows the driver to reset the EHCI controller without affecting the state of the ports or the relationship to the companion host controllers. Read 0x0: Light host controller reset is complete and it is safe for host software to reinitialize the host controller. Read 0x1: Light host controller reset is still ongoing.	RW	0
6	IAAD	Interrupt on async advance doorbell This bit is used as a doorbell by software to tell the host controller to issue an interrupt the next time it advances asynchronous schedule. Write 0x1: Ring the doorbell. Software must not write 1 to this bit when the asynchronous schedule is disabled. Doing so may yield undefined results.	RW	0
5	ASE	Asynchronous schedule enable This bit controls whether the host controller skips processing the asynchronous schedule. 0x0: Do not process the asynchronous schedule	RW	0

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Bits	Field Name	Description	Type	Reset
		0x1: Use the USBHOST.ASYNCLISTADDR register to access the asynchronous schedule.		
4	PSE	Periodic schedule enable This bit controls whether the host controller skips processing the periodic schedule. 0x0: Do not process the periodic schedule 0x1: Use the USBHOST.PERIODICLISTBASE register to access the periodic schedule.	RW	0
3:2	FLS	Frame list size This field specifies the size of the frame list. The size of the frame list controls which bits in the frame index register should be used for the frame list current index. 0x0: 1024 elements (4096 bytes) 0x1: 512 elements (2048 bytes) 0x2: 256 elements (1024 bytes), for resource-constrained environments 0x3: Reserved	RW	0
1	HCR	Host controller reset This control bit is used by software to reset the host controller. Write 0x1: Reset the host controller, the PCI configuration registers are not affected by this reset and all operational registers are set to their initial values. This bit is set to 0 by the host controller when the reset process is complete.	W	0
0	RS	Run/stop 0x1: Run, the host controller proceeds with execution of the schedule. The host controller continues execution as long as this bit is set to 1. 0x0: Stop, the host controller completes the current and any actively pipelined transactions on the USB and then halts.	RW	0

Table 23-1126. Register Call Summary for Register USBCMD

High-Speed Multiport USB Host Subsystem

- EHCI Register Summary: [0]
- EHCI Register Description: [1] [2] [3] [4] [5]

Table 23-1127. USBSTS

Address Offset	0x0000 0014		
Physical Address	0x4A06 4C14	**Instance**	EHCI
Description	USB status		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																ASS	PSS	REC	HCH	RESERVED				IAA	HSE	FLR	PCD	USBEI	USBI		

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x0000
15	ASS	Asynchronous schedule status The bit reports the current real status of the asynchronous schedule.	R	0

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Bits	Field Name	Description	Type	Reset
		0x0: The status of the asynchronous schedule is disabled. 0x1: The status of the asynchronous schedule is enabled.		
14	PSS	Periodic schedule status The bit reports the current real status of the periodic schedule. 0x0: The status of the periodic schedule is disabled. 0x1: The status of the periodic schedule is enabled.	R	0
13	REC	Reclamation It is used to detect an empty asynchronous schedule.	R	0
12	HCH	Host controller halted This bit is a 0 whenever the USBHOST.USBCMD[0] RS bit is a 1. The host controller sets this bit to 1 after it has stopped executing as a result of the RS bit being set to 0, either by software or by the host controller hardware.	R	1
11:6	RESERVED	Reserved	R	0x00
5	IAA	Interrupt on async advance System software can force the host controller to issue an interrupt the next time the host controller advances the asynchronous schedule by setting the USBHOST.USBCMD[6] IAAD bit to 1. This status bit indicates the assertion of that interrupt source.	RW	0
4	HSE	Host system error The host controller sets this bit to 1 when a serious error occurs during a host system access involving the host controller module.	RW	0
3	FLR	Frame list rollover The host controller sets this bit to 1 when the USBHOST.FRINDEX rolls over from its maximum value to 0. The exact value at which the rollover occurs depends on the frame list size.	RW	0
2	PCD	Port change detect The host controller sets this bit to 1 when any port for which the USBHOST.PORTSC_i[13] PO bit is set to 0 has a change bit transition from 0 to 1 or a USBHOST.PORTSC_i[6] FPR bit transition from 0 to 1. This bit is also set as a result of the USBHOST.PORTSC_i[1] CSC bit being set to 1 after system software has relinquished ownership of a connected port by setting the USBHOST.PORTSC_i[13] PO bit to 1.	RW	0
1	USBEI	USB error interrupt The host controller sets this bit to 1 when completion of a USB transaction results in an error condition.	RW	0
0	USBI	USB interrupt The host controller sets this bit to 1 on completion of a USB transaction, which results in the retirement of a transfer descriptor that had its IOC bit set. The host controller also sets this bit to 1 when a short packet is detected (actual number of bytes received was less than the expected number of bytes).	RW	0

Table 23-1128. Register Call Summary for Register USBSTS

High-Speed Multiport USB Host Subsystem

- HSUSB Controller Register Description: [0]
- EHCI Register Summary: [1]
- EHCI Register Description: [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13]

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Table 23-1129. USBINTR

Address Offset	0x0000 0018		
Physical Address	0x4A06 4C18	**Instance**	EHCI
Description	USB interrupt enable		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																										IAAE	HSEE	FLRE	PCIE	USBEIE	USBIE

Bits	Field Name	Description	Type	Reset
31:6	RESERVED	Reserved	R	0x0000000
5	IAAE	Interrupt on async advance enable 0x1: When the USBSTS[5] IAA bit is 1, the host controller issues an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the USBSTS[5] IAA bit.	RW	0
4	HSEE	Host system error enable 0x1: When the USBSTS[4] HSE bit is 1, the host controller issues an interrupt. The interrupt is acknowledged by software clearing the USBSTS[4] HSE bit.	RW	0
3	FLRE	Frame list rollover enable 0x1: When the USBSTS[3] FLR bit is 1, the host controller issues an interrupt. The interrupt is acknowledged by software clearing the USBSTS[3] FLR bit.	RW	0
2	PCIE	Port change interrupt enable 0x1: When the USBSTS[2] PCD bit is 1, the host controller issues an interrupt. The interrupt is acknowledged by software clearing the USBSTS[3] FLR bit.	RW	0
1	USBEIE	USB error interrupt enable 0x1: When the USBSTS[1] USBEI bit is 1, the host controller issues an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the USBSTS[1] USBEI bit.	RW	0
0	USBIE	USB interrupt enable 0x1: When the USBSTS[0] USBI bit is 1, the host controller issues an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the USBSTS[0] USBI bit.	RW	0

Table 23-1130. Register Call Summary for Register USBINTR

High-Speed Multiport USB Host Subsystem

- HS Multiport USB Host Subsystem Global Initialization: [0]
- EHCI Register Summary: [1]

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Table 23-1131. FRINDEX

Address Offset	0x0000 001C		
Physical Address	0x4A06 4C1C	**Instance**	EHCI
Description	USB frame index		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								FI							

Bits	Field Name	Description	Type	Reset
31:14	RESERVED	Reserved	R	0x00000
13:0	FI	Frame index The value in this register is incremented at the end of each time frame.	RW	0x0000

Table 23-1132. Register Call Summary for Register FRINDEX

High-Speed Multiport USB Host Subsystem

- EHCI Register Summary: [0]
- EHCI Register Description: [1]

Table 23-1133. CTRLDSSEGMENT

Address Offset	0x0000 0020		
Physical Address	0x4A06 4C20	**Instance**	EHCI
Description	4G segment selector		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CDSS																															

Bits	Field Name	Description	Type	Reset
31:0	CDSS	This 32-bit register corresponds to the most-significant address bits [63:32] for all EHCI data structures.	R	0x00000000

Table 23-1134. Register Call Summary for Register CTRLDSSEGMENT

High-Speed Multiport USB Host Subsystem

- EHCI Register Summary: [0]

Table 23-1135. PERIODICLISTBASE

Address Offset	0x0000 0024		
Physical Address	0x4A06 4C24	**Instance**	EHCI
Description	Frame list base address		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BAL																				RESERVED											

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Bits	Field Name	Description	Type	Reset
31:12	BAL	Base address (low) These bits correspond to memory address signals.	RW	0x00000
11:0	RESERVED	Reserved	R	0x000

Table 23-1136. Register Call Summary for Register PERIODICLISTBASE

High-Speed Multiport USB Host Subsystem

- EHCI Register Summary: [0]
- EHCI Register Description: [1]

Table 23-1137. ASYNCLISTADDR

Address Offset	0x0000 0028		
Physical Address	0x4A06 4C28	**Instance**	EHCI
Description	Next asynchronous list address		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LPL																														RESERVED	

Bits	Field Name	Description	Type	Reset
31:5	LPL	Link pointer low It contains the address of the next asynchronous queue head to be executed.	RW	0x0000000
4:0	RESERVED	Reserved	R	0x00

Table 23-1138. Register Call Summary for Register ASYNCLISTADDR

High-Speed Multiport USB Host Subsystem

- EHCI Register Summary: [0]
- EHCI Register Description: [1]

Table 23-1139. CONFIGFLAG

Address Offset	0x0000 0050		
Physical Address	0x4A06 4C50	**Instance**	EHCI
Description	Configured flag register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															CF

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x00000000
0	CF	Configure flag This bit controls the default port-routing control logic. 0x0: Port routing control logic default-routes each port to an implementation-dependent classic host controller. 0x1: Port routing control logic default-routes all ports to this host controller.	RW	0

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Table 23-1140. Register Call Summary for Register CONFIGFLAG

High-Speed Multiport USB Host Subsystem

- EHCI Register Summary: [0]
- EHCI Register Description: [1] [2]

Table 23-1141. PORTSC_i

Address Offset	0x0000 0054 + (0x4 * i)	**Index**	i = 0 to 2
Physical Address	0x4A06 4C54 + (0x4 * i)	**Instance**	EHCI
Description	Port status/control		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DEVICEADDRESS								SUSPENDSTATUS	RESERVED	WDE	WCE	PTC				PIC		PO	PP	LS		SUSPENDL1	PR	SUS	FPR	RESERVED		PEDC	PED	CSC	CCS

Bits	Field Name	Description	Type	Reset
31:25	DEVICEADDRESS	The USB device address for the device attached to and immediately downstream from the associated root port. R/W only if LPM is enabled; otherwise, R.	RW	0x00
24:23	SUSPENDSTATUS	Addition for LPM support. Indicates status of L1 suspend request: 0x0: Success 0x1: Not yet 0x2: Not supported 0x3: Time-out/error	R	0x0
22	RESERVED	Reserved	R	0
21	WDE	Wake on disconnect enable This field is 0 if the PP bit is 0. Write 0x1: Enables the port to be sensitive to device disconnects as wake-up events.	RW	0
20	WCE	Wake on connect enable This field is 0 if the PP bit is 0. Write 0x1: Enables the port to be sensitive to device connects as wake-up events.	RW	0
19:16	PTC	Port test control The port is operating in specific test modes as indicated by the specific value. The encoding of the test mode bits are: 0x0: Test mode not enabled 0x1: Test J_STATE 0x2: Test K_STATE 0x3: Test SE0_NAK 0x4: Test Packet 0x5: Test FORCE_ENABLE Others: Reserved	RW	0x0
15:14	PIC	Port indicator control (not implemented)	R	0x0
13	PO	Port owner	RW	1

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Bits	Field Name	Description	Type	Reset
		This bit unconditionally goes to 0x0 when the USBHOST.CONFIGFLAG[0] CF bit makes a transition from 0 to 1. This bit unconditionally goes to 0 whenever the USBHOST.CONFIGFLAG[0] CF bit is 0. 0x1: A companion host controller owns and controls the port.		
12	PP	Port power The function of this bit depends on the value of the USBHOST.HCSPARAMS[4] PPC bit. The behavior is as follows: **PPC** / **PP** / **Operation** 0x0 / 0x1 / Host controller does not have port power. control switches. Each port is hardwired to power. 0x1 / N/A / Host controller has port power control switches. This bit represents the current setting of the switch (0 = Off, 1 = On). When an overcurrent condition is detected on a powered port and the USBHOST.HCSPARAMS[4] PPC bit is a 1, the PP bit in each affected port may be transitioned by the host controller from 1 to 0.	RW	0
11:10	LS	Line status These bits reflect the current logical levels of the D+ (bit 11) and D– (bit 10) signal lines. This field is valid only when the port enable bit is 0 and the current connect status bit is set to 1. The encoding of the bits is: **Bits[11:10]** / **USB State** / **Interpretation** 0x0 / SE0 / Not low-speed device, perform EHCI reset. 0x2 / J-state / Not low-speed device, perform EHCI reset. 0x1 / K-state / Low-speed device, release ownership of port. 0x3 / Undefined / Not low-speed device, perform EHCI reset.	R	0x0
9	SUSPENDL1	When this bit is set to 1, an LPM token is generated. 0: Suspend using L2 1: Suspend using L1 (LPM)	RW	0
8	PR	Port reset This field is 0 if the PP bit is 0. 0x0: Port is not in reset. 0x1: Port is in reset. Write 0x0: Terminate the bus reset sequence. Write 0x1 when at 0x0: The bus reset sequence is started.	RW	0
7	SUS	Suspend This field is 0 if the PP bit is 0. 0x0 when PED = 0x1: Port enabled 0x1 when PED = 0x1: Port in suspend state When PED = 0x0: Port disabled	RW	0
6	FPR	Force port resume This field is 0 if the PP bit is 0. 0x0: No resume (K-state) detected/driven on port 0x1: Resume detected/driven on port	RW	0
5:4	RESERVED	Reserved	R	0
3	PEDC	Port enabled/disabled change This field is 0 if the PP bit is 0. Read 0x0: No change. Read 0x1: Port enabled/disabled status has changed. Write 0x1: Clears this bit to 0.	RW	0

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Bits	Field Name	Description	Type	Reset
2	PED	Port enabled/disabled Software cannot enable a port by setting this bit to 1. The host controller only sets this to 1 when the reset sequence determines that the attached device is a high-speed device. Ports can be disabled by either a fault condition (disconnect event or other fault condition) or by host software. This field is 0 if the PP bit is 0. 0x0: Disable 0x1: Enable	RW	0
1	CSC	Connect status change Indicates a change has occurred in the port CCS bit. This field is 0 if the PP bit is 0. Read 0x0: No change Read 0x1: Change in current connect status Write 0x1: Clears this bit to 0	RW	0
0	CCS	Current connect status This value reflects the current state of the port, and may not correspond directly to the event that caused the CSC bit to be set. This field is 0 if the PP bit is 0. 0x0: No device is present. 0x1: Device is present on port.	R	0

Table 23-1142. Register Call Summary for Register PORTSC_i

High-Speed Multiport USB Host Subsystem
- EHCI Register Summary: [0]
- EHCI Register Description: [1] [2] [3] [4]

Table 23-1143. INSNREG00

Address Offset	0x0000 0090		
Physical Address	0x4A06 4C90	**Instance**	EHCI
Description	Implementation-specific register 0		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																UFRAME_CNT															EN

Bits	Field Name	Description	Type	Reset
31:14	RESERVED		R	0x00000
13:1	UFRAME_CNT	1-microframe length value, to reduce simulation time. SIMULATIONS ONLY, NOT AN ACTUAL REGISTER.	RW	0x0000
0	EN	Enable of this register	RW	0

Table 23-1144. Register Call Summary for Register INSNREG00

High-Speed Multiport USB Host Subsystem
- EHCI Register Summary: [0]

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Table 23-1145. INSNREG01

Address Offset	0x0000 0094		
Physical Address	0x4A06 4C94	**Instance**	EHCI
Description	Implementation-specific register 1		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUT_THRESHOLD																IN_THRESHOLD															

Bits	Field Name	Description	Type	Reset
31:16	OUT_THRESHOLD	Programmable output packet buffer threshold, in 32-bit words	RW	0x0020
15:0	IN_THRESHOLD	Programmable input packet buffer threshold, in 32-bit words	RW	0x0020

Table 23-1146. Register Call Summary for Register INSNREG01

High-Speed Multiport USB Host Subsystem

- EHCI Register Summary: [0]
- EHCI Register Description: [1]

Table 23-1147. INSNREG02

Address Offset	0x0000 0098		
Physical Address	0x4A06 4C98	**Instance**	EHCI
Description	Implementation-specific register 2		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				BUF_DEPTH											

Bits	Field Name	Description	Type	Reset
31:12	RESERVED		R	0x00000
11:0	BUF_DEPTH	Programmable packet buffer depth, in 32-bit words	RW	0x080

Table 23-1148. Register Call Summary for Register INSNREG02

High-Speed Multiport USB Host Subsystem

- EHCI Register Summary: [0]

Table 23-1149. INSNREG03

Address Offset	0x0000 009C		
Physical Address	0x4A06 4C9C	**Instance**	EHCI
Description	Implementation-specific register 3		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															BRK_MEM_TRSF

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	BRK_MEM_TRSF	Break memory transfer, in conjunction with INSNREG01 0x0: Disabled 0x1: Enabled	RW	1

Table 23-1150. Register Call Summary for Register INSNREG03

High-Speed Multiport USB Host Subsystem

- EHCI Register Summary: [0]

Table 23-1151. INSNREG04

Address Offset	0x0000 00A0		
Physical Address	0x4A06 4CA0	**Instance**	EHCI
Description	Implementation-specific register 4		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																											NAK_FIX_DIS	RESERVED	SHORT_PORT_ENUM	HCCPARAMS_WRE	HCSPARAMS_WRE

Bits	Field Name	Description	Type	Reset
31:5	RESERVED	Reserved	R	0x0000000
4	NAK_FIX_DIS	Disable NAK fix (don't touch)	RW	0
3	RESERVED	Reserved	R	0
2	SHORT_PORT_ENUM	Scale down port enumeration time (debug)	RW	0
1	HCCPARAMS_WRE	Make read-only HCCPARAMS register writable (debug)	RW	0
0	HCSPARAMS_WRE	Make read-only HCSPARAMS register writable (debug)	RW	0

Table 23-1152. Register Call Summary for Register INSNREG04

High-Speed Multiport USB Host Subsystem

- EHCI Register Summary: [0]
- EHCI Register Description:

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Table 23-1153. INSNREG05_UTMI

Address Offset	0x0000 00A4		
Physical Address	0x4A06 4CA4	**Instance**	EHCI
Description	Implementation-specific register 5. Register functionality for UTMI mode.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								VBUSY		VPORT						VCONTROLLOADM		VCONTROL						VSTATUS							

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17	VBUSY	Read 0x0: Vendor interface is done/inactive Read 0x1: Vendor interface is busy	R	0
16:13	VPORT	Vendor interface port selection 0x1: Port 1 vendor interface selected 0x2: Port 2 vendor interface selected	RW	0x0
12	VCONTROLLOADM	UTMI VcontrolLoadM output (active-low) 0x0: Load Vcontrol value into PHY 0x1: No Action	RW	0
11:8	VCONTROL	UTMI Vcontrol output, to be loaded into the PHY	RW	0x0
7:0	VSTATUS	UTMI Vstatus input image, from PHY	R	0x00

Table 23-1154. Register Call Summary for Register INSNREG05_UTMI

High-Speed Multiport USB Host Subsystem

- EHCI Register Summary: [0]

Table 23-1155. INSNREG05_ULPI

Address Offset	0x0000 00A4		
Physical Address	0x4A06 4CA4	**Instance**	EHCI
Description	Implementation-specific register 5. Register functionality for ULPI mode.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONTROL	RESERVED			PORTSEL				OPSEL		REGADD						EXTREGADD								RDWRDATA							

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Bits	Field Name	Description	Type	Reset
31	CONTROL	Control/status of the ULPI register access Write 0x0: No effect 0x0: ULPI access done 0x1: Start ULPI access	RW	0
30:28	RESERVED		R	0x0
27:24	PORTSEL	0x1: Port 1 selected for register access 0x2: Port 2 selected for register access	RW	0x0
23:22	OPSEL	0x2: Register access is write. 0x3: Register access is read.	RW	0x0
21:16	REGADD	ULPI direct register address, for any value different than 0x2F. 0x2F: Triggers an extended address	RW	0x00
15:8	EXTREGADD	Address for extended register accesses. Don't care for direct accesses.	RW	0x00
7:0	RDWRDATA	Read/write data of (resp. read/write) register access	RW	0x00

Table 23-1156. Register Call Summary for Register INSNREG05_ULPI

High-Speed Multiport USB Host Subsystem

- EHCI Register Summary: [0]

Table 23-1157. INSNREG06

Address Offset	0x0000 00A8		
Physical Address	0x4A06 4CA8	**Instance**	EHCI
Description	AHB error status		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ERRORCAP	RESERVED																			HBURST				BEATSEXP				BEATSCOMP			

Bits	Field Name	Description	Type	Reset
31	ERRORCAP	Indicator that an AHB error was encountered and values were captured Read 0x0: No error Write 0x0: Clear pending error Write 0x1: No action Read 0x1: Error pending	RW	0
30:12	RESERVED		R	0x00000
11:9	HBURST	HBURST Value of the control phase at which the AHB error occurred	R	0x0
8:4	BEATSEXP	Number of beats expected in the burst at which the AHB error occurred. Valid values are 0 to 16.	R	0x00
3:0	BEATSCOMP	Number of successfully completed beats in the current burst before the AHB error occurred	R	0x0

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Table 23-1158. Register Call Summary for Register INSNREG06

High-Speed Multiport USB Host Subsystem

- EHCI Register Summary: [0]

Table 23-1159. INSNREG07

Address Offset	0x0000 00AC		
Physical Address	0x4A06 4CAC	**Instance**	EHCI
Description	AHB master error address		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASTERERRADD																															

Bits	Field Name	Description	Type	Reset
31:0	MASTERERRADD	AHB master error address	R	0x0000 0000

Table 23-1160. Register Call Summary for Register INSNREG07

High-Speed Multiport USB Host Subsystem

- EHCI Register Summary: [0]

Table 23-1161. INSNREG08

Address Offset	0x0000 00B0		
Physical Address	0x4A06 4CB0	**Instance**	EHCI
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																NEWBITFIELD1															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:0	NEWBITFIELD1		RW	0x0000

Table 23-1162. Register Call Summary for Register INSNREG08

High-Speed Multiport USB Host Subsystem

- EHCI Register Summary: [0]

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23.12 High-Speed USB OTG Controller

This section describes the high-speed USB On-The-Go (OTG) controller of the device.

NOTE: The high-speed USB OTG controller is an instantiation of the MUSBMHDRC from Mentor Graphics Corporation.

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23.12.1 High-Speed USB OTG Controller Overview

The High-Speed USB controller is a high-speed, USB OTG dual-role-device (DRD) link controller supporting the following modes:

- USB 2.0 peripheral (function controller) in high/full speed (480/12 Mbps, respectively)
- USB 2.0 host in high/full/low speed (480/12/1.5 Mbps, respectively), with one downstream port but multipoint capability when a hub is connected to it (split transaction support, etc.)
- USB 2.0 OTG DRD in high/full speed, with HNP (OTG1.3) and SRP support.

The high-speed USB OTG controller supports a single USB port, which uses the ULPI interface mode, to connect to an off-chip transceiver (12-pin/8-bit data SDR mode) and to connect on D+/D- (+ID) USB bus thanks to an embedded USB-HS OTG PHY.

It is connected to L3 master and L4 slave interfaces. It is clocked from independent functional clock from a PHY. This module operates either as the function controller of a high-/full-speed USB peripheral or as the host/peripheral in point-to-point or multi-point communications with other USB functions.

Figure 23-255 highlights the high-speed USB controller.

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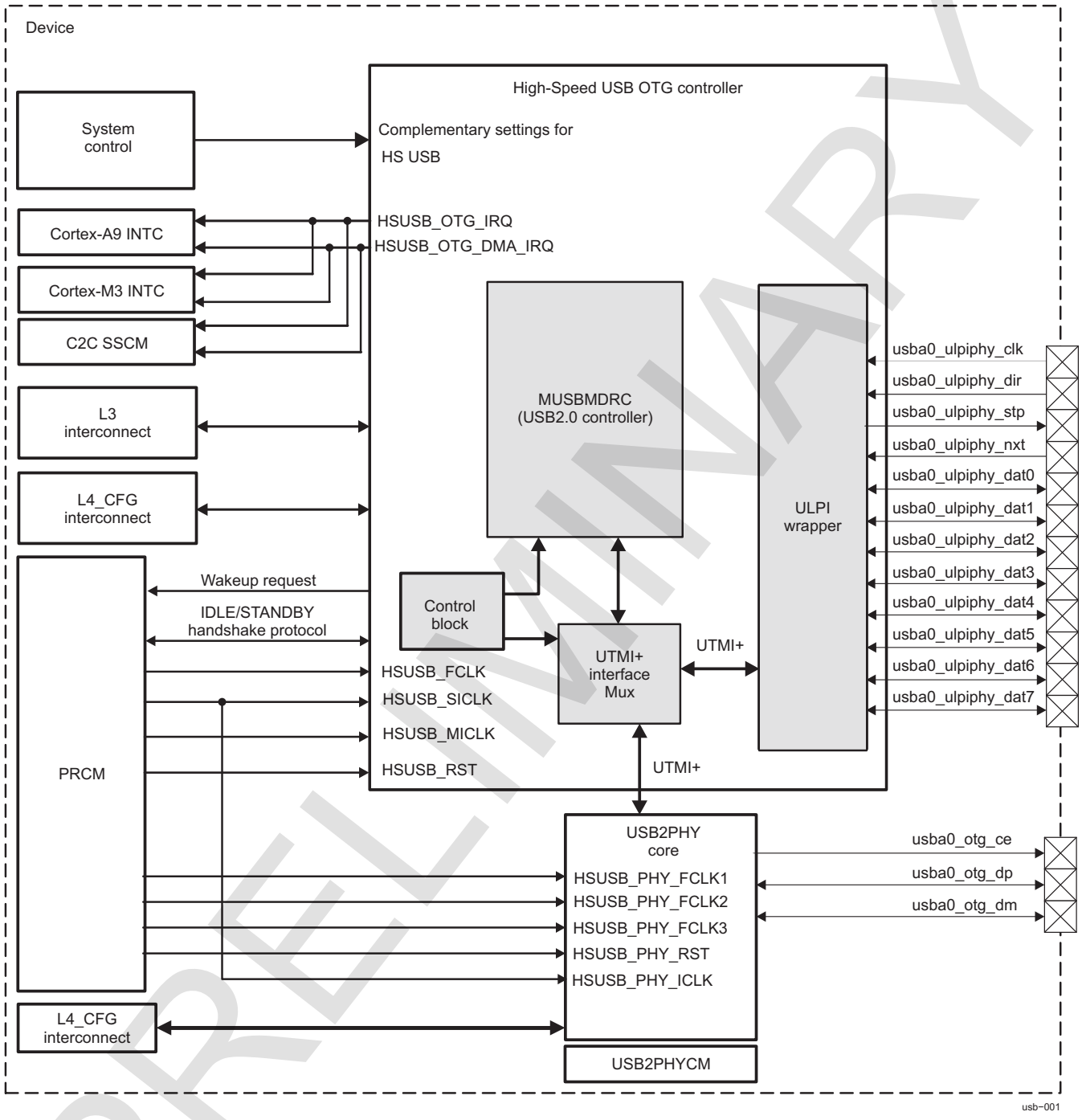
Figure 23-255. High-Speed USB OTG Controller Highlight



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23.12.1.1 Main Features

The high-speed USB controller features:

- L3 (master) interface supports:
  - 32-bit data bus width
  - 8/16/32 bit access supported
  - 32-bit address bus width
  - Burst supported
  - WNP not supported
- L4 (slave) interface supports:
  - 32-bit data bus width
  - 16/32 bit access supported
  - 12-bit address bus width
  - Burst not supported
  - WNP supported
- Complies with USB2.0 standard for high-speed (480 Mb/s) functions and with the OTG 1.3 (On-The-Go) supplement. Implement Link Power Management
- Contains embedded HS PHY with battery charger detection
- Contains PHY (physical layer) interface: ULPI interface (12-bit version)
- 15 transmit endpoints and 15 receive endpoints in addition to control endpoint 0
- Supports OTG communications with one or more high/full/low speed devices.
- Supports packet splitting / combining for bulk transfers
- Soft connect/disconnect option
- Performs all transaction scheduling in hardware
- Each endpoint can be configured for types (interrupt, bulk or isochronous), for size and double buffering operation within a limit of a 8KB of data and total RAM size of 16KB.
- Supports high-bandwidth isochronous and interrupt transfers.
- Supports suspend/resume and remote wake-up.
- Two interrupt lines.
- DMA access to endpoint FIFOs with internal DMA controller supporting 8 channels
- Supports host negotiation and session request protocols (HNP (OTG1.3) and SRP)
- Carkit feature implementation

USB-HS OTG PHY (USBPHY). This embedded PHY is composed of two modules:

- USB2PHYCORE contains the USB functions, drivers, receivers and pads for correct D+/D– signalling and the battery charger detection (supporting dead-battery mode). Delivers a 3.3-V output signal (charger enable) to control external battery charger.
- USB2PHYCM contains LDO and bandgap for providing voltage reference to USB2PHYCORE module.

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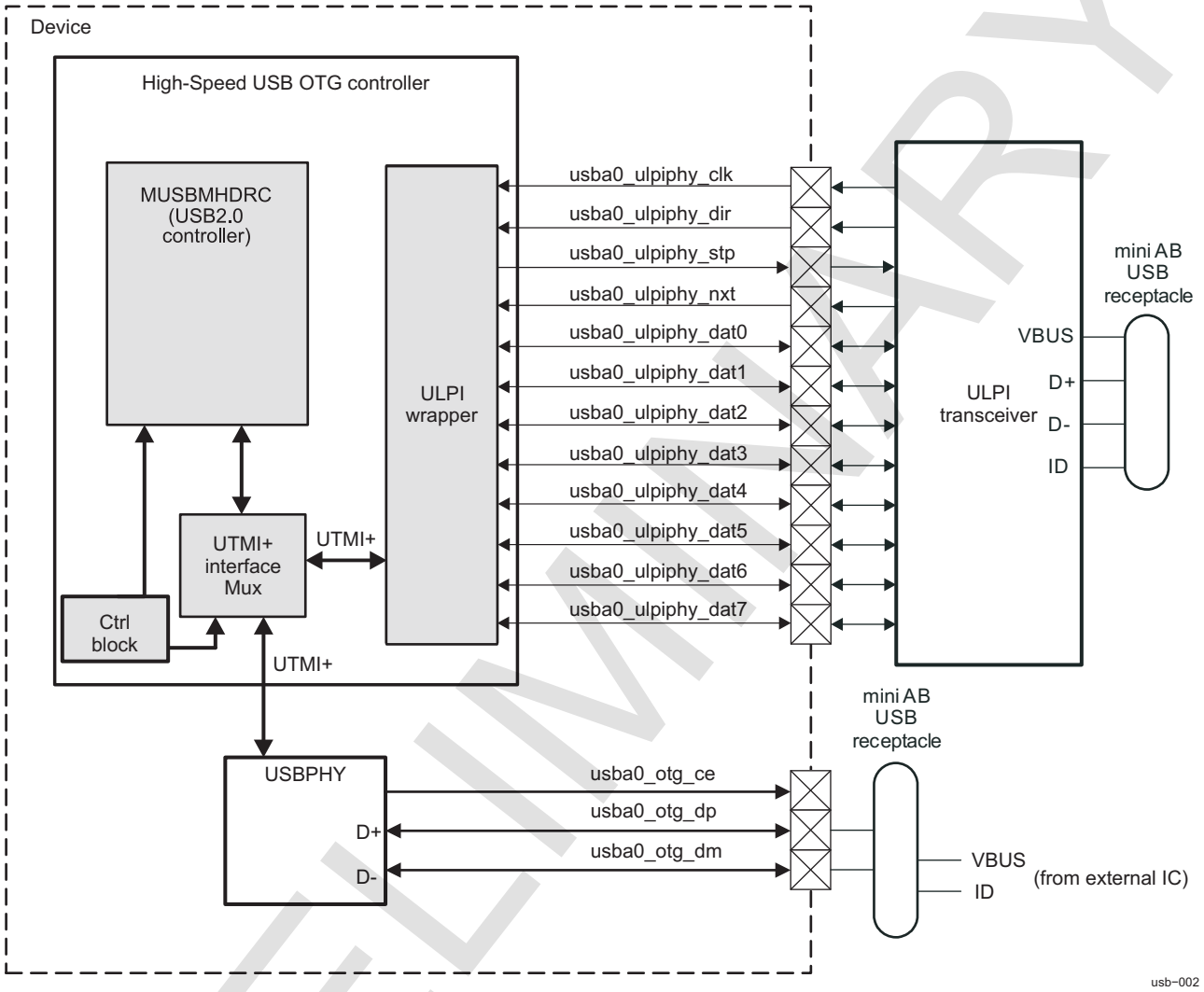
23.12.2 High-Speed USB OTG Controller Environment

Figure 23-256 shows a typical application using the high-speed USB controller.

Figure 23-256. High-Speed USB Controller Typical Application System



NOTE: Only one interface can be active at a time.

The high-speed USB OTG controller supports a single USB port, which uses the ULPI interface mode, to connect to an off-chip transceiver (12-pin/8-bit data SDR mode). A mini A-B external receptacle allows the connection of an external device.

The 12-pin ULPI interface uses an 8-bit data bus with data synchronous to the rising edge of the PHY clock (SDR mode); the 8-pin ULPI uses a 4-bit data bus with data generated on both the rising and falling clock edge (DDR mode).

The current implementation of high-speed USB controller supports only the 12-pin, 8-bit version ULPI interface. The 12-pin/8-bit data SDR ULPI interface is selected through the OTG_INTERFSEL[2:0] PHYSEL field and must be set to 0x1.

Embedded PHY interface is 8-bit, UTMI+ and is selected through setting OTG_INTERFSEL [2:0] PHYSEL field to 0x0.

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23.12.2.1 High-Speed USB OTG Controller Functional Interfaces

Table 23-1163 describes the I/O signals of the high-speed USB controller interfaces shown in Figure 23-256

Table 23-1163. Input/Output Description

Signal Name	I/O [1]	Description	Reset Value
usba0_ulpiphy_clk	I	Clock input from external transceiver	HiZ
usba0_ulpiphy_dir	I	Data direction control from external transceiver	HiZ
usba0_ulpiphy_stp	O	Output to external transceiver to stop data stream	1
usba0_ulpiphy_nxt	I	Next signal control from external transceiver	HiZ
usba0_ulpiphy_dat0	I/O	Data 0 to/from external transceiver	HiZ
usba0_ulpiphy_dat1	I/O	Data 1 to/from external transceiver	HiZ
usba0_ulpiphy_dat2	I/O	Data 2 to/from external transceiver	HiZ
usba0_ulpiphy_dat3	I/O	Data 3 to/from external transceiver	HiZ
usba0_ulpiphy_dat4	I/O	Data 4 to/from external transceiver	HiZ
usba0_ulpiphy_dat5	I/O	Data 5 to/from external transceiver	HiZ
usba0_ulpiphy_dat6	I/O	Data 6 to/from external transceiver	HiZ
usba0_ulpiphy_dat7	I/O	Data 7 to/from external transceiver	HiZ
usba0_otg_ce	O	Charging Enable signal	0
usba0_otg_dp	I/O	USB Data +	HiZ
usba0_otg_dm	I/O	USB Data -	HiZ

[1] I = Input; O = Output

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23.12.3 High-Speed USB OTG Controller Integration

The L3 (master) interconnect generates data traffic within the device. The L4(slave) interconnect is a configuration port for register setting.

Figure 23-257 shows the high-speed USB controller integration in the device.

Figure 23-257. High-Speed USB Controller Integration

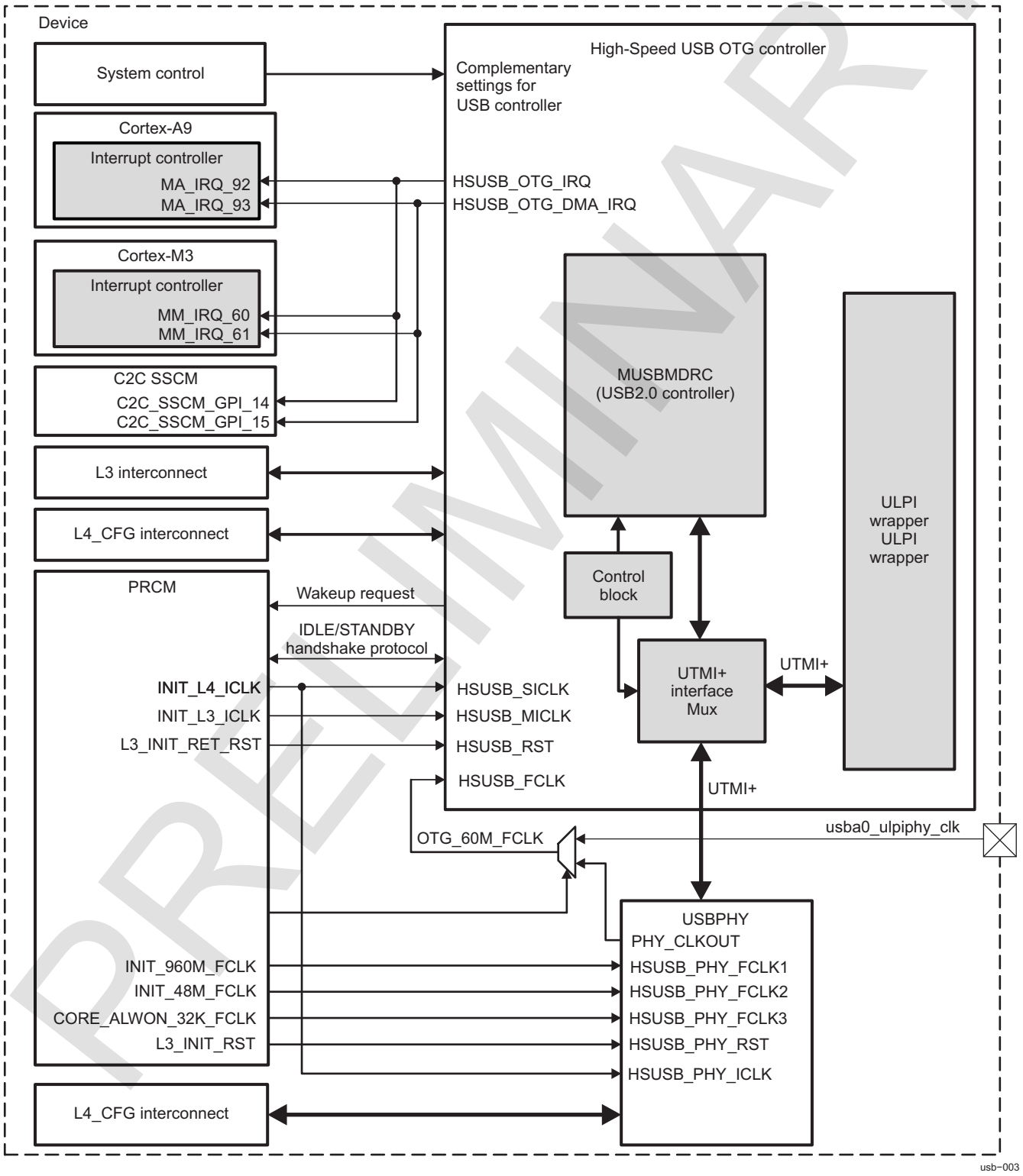

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Table 23-1164 through Table 23-1166 summarize the integration of the module in the device.

Table 23-1164. Integration Attributes

Module Instance	Attributes	
	Power Domain	Interconnect
HSUSBOTG	PD_L3_INIT	L3 L4_CFG
USBPHY	PD_L3_INIT	L4_CFG

Three clocks are provided to the high-speed USB controller, as listed in Table 23-1165

Table 23-1165. Clocks and Resets

Clocks				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
HSUSBOTG	HSUSB_FCLK	OTG_60M_FCLK	usba0_ulpiphy_clk/ USBPHY	Functional clock. Source is selected between external and embedded PHY. Section 3.6.3.2, *CM Clock Source*, in Chapter 3, *Power, Reset, and Clock Management*.
	HSUSB_SICLK	INIT_L4_ICLK	PRCM	L4 interconnect enable signal for the slave interface on L4 Section 3.6.3.2, *CM Clock Source* in Chapter 3, *Power, Reset and Clock Management*
	HSUSB_MICLK	INIT_L3_ICLK	PRCM	L3 interconnect clock, for the L3 master port interface Section 3.6.9, *CD_L3_INIT Clock Domain* in Chapter 3, *Power, Reset and Clock Management*.
USBPHY	HSUSB_PHY_FCLK1	INIT_960M_FCLK	PRCM	Functional clock
	HSUSB_PHY_FCLK2	INIT_48M_FCLK	PRCM	Optional functional clock
	HSUSB_PHY_FCLK3	CORE_ALWON_32K_FCLK	PRCM	Optional functional clock
	HSUSB_PHY_ICLK	INIT_L4_ICLK	PRCM	Interface clock
Resets				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
HSUSBOTG	HSUSB_RST	L3_INIT_RET_RST	PRCM	HSUSBOTG controller hardware reset
USBPHY	HSUSB_PHY_RST	L3_INIT_RST	PRCM	USBPHY module hardware reset

Table 23-1166 lists the interrupt lines that are driven out from the high-speed USB controller.

Table 23-1166. Hardware Requests

Interrupt Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
HSUSBOTG	HSUSB_OTG_IRQ	MA_IRQ_92	Cortex™-A9 INTC	HSUSBOTG interrupt request
	HSUSB_OTG_DMA_IRQ	MA_IRQ_93	Cortex-A9 INTC	HSUSBOTG DMA interrupt request
	HSUSB_OTG_IRQ	MM_IRQ_60	Cortex™-M3 INTC	HSUSBOTG interrupt request
	HSUSB_OTG_DMA_IRQ	MM_IRQ_61	Cortex-M3 INTC	HSUSBOTG DMA interrupt request
	HSUSB_OTG_IRQ	C2C_SSCM_GPI_14	C2C SSCM	HSUSBOTG interrupt request
	HSUSB_OTG_DMA_IRQ	C2C_SSCM_GPI_15	C2C SSCM	HSUSBOTG DMA interrupt request

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23.12.4 High-Speed USB OTG Controller Functional Description

23.12.4.1 Software Reset

The high-speed USB controller has a software reset through the OTG_SYSCONFIG[1] SOFTRESET bit. Writing 0x1 to this bit initiates reset of the module. The bit value 0x1 remains until the reset is complete. When the software reset is complete, the SOFTRESET bit is automatically cleared to 0x0 and has the same effect as the hardware reset. The status of the reset can be observed through the OTG_SYSSTATUS[0] RESETDONE bit.

23.12.4.2 Power Management

23.12.4.2.1 Overview

To save dynamic power consumption, an efficient idle scheme in the device is based on the following:

- An efficient local autoclock gating for each module
- The implementation of control sideband signals between the PRCM module and each module

This enhanced idle control allows clocks to be activated/deactivated safely without complex software intervention. In both cases, the high-speed USB controller power management is applied only to the interface clock domain. The USB OTG functional clock, HSUSB_FCLK, is controlled by the transceiver and is responsible only for a very small percentage of the module overall power consumption.

The high-speed USB controller has both master (initiator) and slave (target) interfaces.

- As an initiator, the high-speed USB OTG controller implements the standby handshake protocol to inform the PRCM module when it enters standby mode and does not generate traffic on the interconnect.
- As a target, the high-speed USB OTG controller implements the IDLE handshake protocol to allow the PRCM module requiring it to enter idle mode.

23.12.4.2.2 System Power Management

23.12.4.2.2.1 Standby Handshake Protocol

The high-speed USB OTG controller can choose to go to standby mode, in which case it stops generating transactions on the interconnect. The module standby leads the PRCM to disable the USB clocks to save power.

The high-speed USB OTG controller has a MSTANDBY handshake mechanism with the PRCM module

The module is ready to enter standby mode (indicated by the MSTANDBY signal to the PRCM asserted) when the USB is in suspend mode and the module is idle. It means the following:

- The module is committed not to start any new transaction on its master interface.
- The module is idle and, therefore, the power manager can start the procedure to turn off the interface clock, if needed. This procedure must be implemented using the slave power-management protocol.

The handshake mechanism lets the module to go to standby state based on the OTG_SYSCONFIG[13:12] MIDLEMODE field.

- Smart-standby

  The high-speed USB controller is configured in smart-standby mode (OTG_SYSCONFIG[13:12] MIDLEMODE field = 0x2). The module is ready to enter standby mode (MSTANDBY is asserted) when there is no more activity on the USB master interface of the interconnect. MSTANDBY is asserted when the module is idle and deasserted when the module is activated by either an external USB event or an appropriate register access. The module then waits for MWAIT deassertion before a DMA transfer is started.
- Force-standby
  - When the high-speed USB controller operates as a host: The USBOTG.POWER[1] SUSPENDMODE bit is set to 0x1 to bring the module to low-power mode (suspend mode). After this setting, the high-speed USB controller waits for its idle state. Software must set

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OTG_SYSCONFIG[13:12] MIDLEMODE = 0x0. Hardware then asserts MSTANDBY. Similarly, to release the MSTANDBY signal, an appropriate register access must be applied, which can be either of the following two cases:

- Remote wakeup causes a RESUME interrupt
- Set the USBOTG.POWER[3] RESET bit to 0x1
- Write 0x2 to the OTG_SYSCONFIG[13:12] MIDLEMODE.

  OR

- Set the USBOTG.POWER[3] RESET bit to 0x1
- Write 0x2 to the OTG_SYSCONFIG[13:12] MIDLEMODE.

– When the high-speed USB controller operates as a peripheral: When the USB bus is idle for 3 ms, a SUSPEND interrupt is generated by the high-speed USB controller. Software must set OTG_SYSCONFIG[13:12] MIDLEMODE = 0x0. Hardware then asserts MSTANDBY. The high-speed USB controller then asserts MSTANDBY. Similarly, to release the MSTANDBY signal, an appropriate register access must be applied, which can be either of the following two cases:

- Set the USBOTG.POWER[2] RESUME bit to 0x1.
- Write 0x2 to the OTG_SYSCONFIG[13:12] MIDLEMODE.

  OR

- RESET interrupt is generated by the high-speed USB controller.
- Write 0x2 to the OTG_SYSCONFIG[13:12] MIDLEMODE.

When MSTANDBY is deasserted as a consequence of the previous register access, the module waits for MWAIT deassertion before a DMA transfer is started.

- No-standby

  The high-speed USB controller is configured in no-standby mode (OTG_SYSCONFIG[13:12] MIDLEMODE field = 0x1). The module never enters standby mode (that is, MSTANDBY is never asserted).

Table 23-1167 describes the high-speed USB standby mode settings.

Table 23-1167. HSUSBOTG Host Controller STANDBYMODE Settings

OTG_SYSCONFIG[13:12] MIDLEMODE Value	Selected Mode	Description
0x0	Force-standby	The HSUSBOTG host controller enters standby mode unconditionally
0x1	No-standby	The HSUSBOTG host controller never enters standby mode
0x2	Smart-standby	The HSUSBOTG host controller is ready to enter standby mode when there is no more activity on the USB master interface of the interconnect.

23.12.4.2.2.2 IDLE Handshake Protocol

The high-speed USB controller can be configured through the OTG_SYSCONFIG[4:3] SIDLEMODE field as one of the following acknowledgment modes:

- Smart-idle mode

  When the high-speed USB controller receives an IDLE request from the PRCM module:

  – The interface clock INIT_L3_ICLK is disabled, see Section 3.6.9, *CD_L3_INIT Clock Domain*

  – L4 interface clock idle transitions:

  Configured in smart-idle mode (OTG_SYSCONFIG[4:3] SIDLEMODE field = 0x2), the high-speed USB controller checks for no ongoing activity. The idle acknowledge then is asserted and the module waits for active system clock gating by the PRCM module (this occurs only when all peripherals supplied by the same L3 clock domain are also ready for idle).

  Once in smart idle mode (when the PRCM module gates the interface clock), the module has no activity, the interface clock paths are gated, no interrupt request can be generated, and the module is

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ready to issue a wake-up request. If a wake-up condition occurs, the high-speed USB controller exits from smart idle mode if the OTG_SYSCONFIG[2] ENABLEWAKEUP bit is set to 0x1 (wake-up capability enabled).

- Smart-idle wake-up mode

  The high-speed USB OTG controller is configured in smart-idle wake-up mode (OTG_SYSCONFIG[4:3] Smart Idle Wkp field = 0x3). The functionality of this mode is the same as smart-idle mode, additionaly Wake up feature is enabled.

- Force-idle mode

  When the high-speed USB controller receives an IDLE request from the PRCM module:

  – The interface clock INIT_L3_ICLK is disabled, see Section 3.6.9, *CD_L3_INIT Clock Domain*

  – The L4 interface clock idle transitions:

    Configured in force-idle mode (OTG_SYSCONFIG[4:3] SIDLEMODE field = 0x0), the high-speed USB controller waits unconditionally for active system clock gating by the PRCM module (this occurs only when all peripherals supplied by the same L3 clock domain are also ready for idle).

  Once in idle mode (when the PRCM module gates the interface clock), the module has no activity, the interface clock paths are gated, no interrupt request can be generated, and the wake-up feature is totally inhibited.

- No-idle mode

  When the high-speed USB controller receives an IDLE request from the PRCM module:

  – The interface clock INIT_L3_ICLK is disabled , *CD_L3_INIT Clock Domain*

  – L4 interface clock idle transitions

    Configured in no-idle mode (OTG_SYSCONFIG[4:3] SIDLEMODE bit field = 0x1), the high-speed USB controller module does not go to idle mode and the idle acknowledge is never sent.

Table 23-1168 describes the high-speed USB sidle mode settings. For more information, see Chapter 3, *Power, Reset, and Clock Management*.

Table 23-1168. HSUSBOTG Host Controller SIDLEMODE Settings

OTG_SYSCONFIG[4:3] SIDLEMODE Value	Selected Mode	Description
0x0	Force-idle	The HSUSBOTG host controller acknowledges unconditionally the IDLE request from the PRCM, regardless of its internal operations.
0x1	No-idle	The HSUSBOTG host controller never acknowledges any IDLE request from the PRCM.
0x2	Smart-idle	The HSUSBOTG host controller acknowledges the IDLE request basing its decision on its internal activity. Namely, the acknowledge signal is asserted only when all pending transactions, IRQs or DMA requests are treated.
0x3	Smart-idle wake-up	The HSUSBOTG host controller enters smart mode with wakeup enabled.

23.12.4.2.2.3 Wake-Up Request

Wake-up request is enabled by setting OTG_SYSCONFIG[2] ENABLEWAKEUP to 0x1. The enable wake-up feature works only when smart-idle wakeup is enabled.

23.12.4.2.3 Local Power Management

The high-speed USB OTG controller has local power management by internal clock gating features:

- Internal interface clock autogating: Clock for the L3 interconnect logic can be gated when the module is not accessed, if the OTG_SYSCONFIG[0] AUTOIDLE bit is set. Otherwise, this logic is free-running on the interface clock. This bit is used to save power when the module is not used because of the multiplexing configuration selected at the chip level. This bit has precedence over all other internal configuration bits.

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23.12.4.3 Inventra MUSBMHDRC

The core functionality of the module is provided by a third-party IP, the Inventra™ MUSBMHDRC from Mentor Graphics® Corporation.

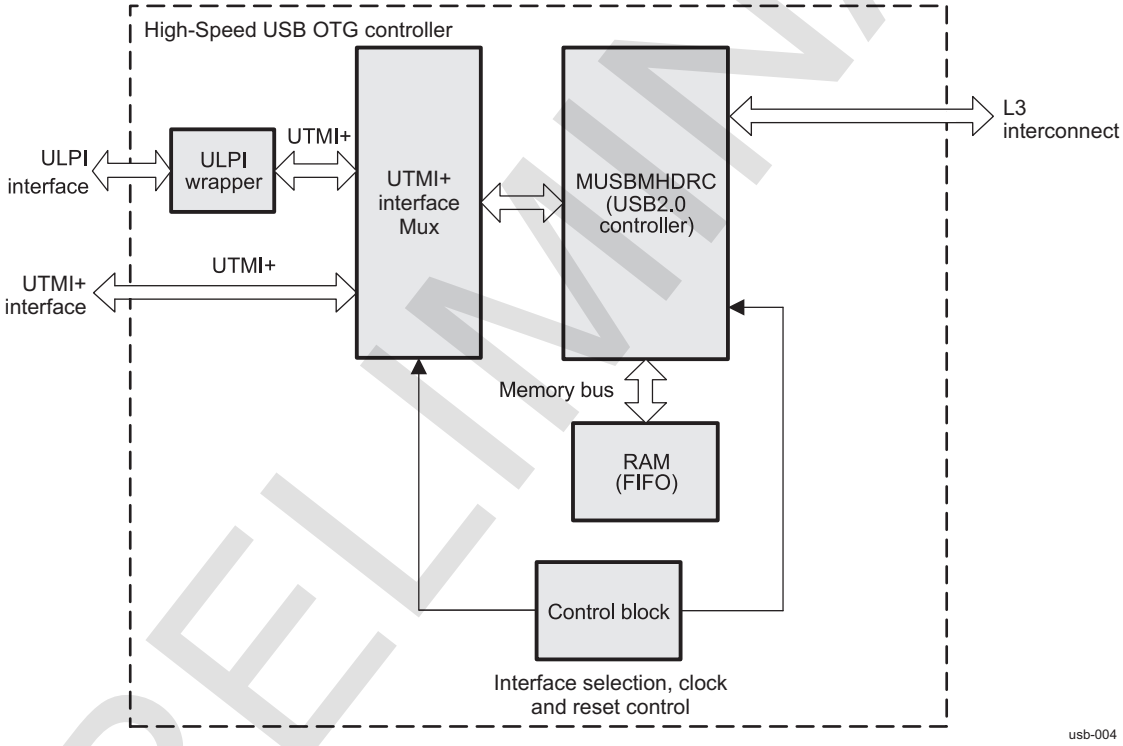
The high-speed USB OTG controller is basically the appropriate adaptation/integration of this IP to comply with TI requirements.

The high-speed USB OTG controller includes the following:

- MUSBMHDRC (USB 2.0 controller)
- Master and slave bridges for conversion AHB to L3 interconnect and L3 interconnect to AHB
- Built-in self-test (BIST) controller
- Two memories (total of 16KB; available for various endpoints)
- Reset and clock generation
- DFT compliance with regards to latest specs

Figure 23-258 shows the high-speed USB controller.

Figure 23-258. High-Speed USB OTG Controller



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23.12.4.4 Configuration

The following options are implemented in the TI high-speed USB OTG controller:

- 8-bit internal data path processing width (mandated by the use of ULPI)
- 32-bit vcontrol/vstatus support
- External charge pump: Hacked
- Software connect/disconnect supported
- Little-endian and big-endian byte ordering
- Eight DMA channels (with internal DMA initiator implemented)
- Dynamic FIFO sizing enabled
- 16-KB RAM buffer
- 15 IN/OUT endpoints in addition to control endpoint 0
- IN/OUT bulk packet splitting enabled
- High-bandwidth IN/OUT isochronous support enabled (see *Universal Serial Bus Specification Revision 2.0*)

23.12.4.5 Basic Operation

This section provides an overview of the module basic operation.

To implement the most time-critical functions in hardware, the module provides all of the encoding, decoding, and checking required to send and receive USB packets, interrupting the MPU only when endpoint data is successfully transferred. Generally, the following steps are performed.

23.12.4.5.1 Module Initialization

First, the firmware must do the overall initialization of the module by configuring the interrupts, DMA controller, and individual endpoints.

The specific items of a configuration for each endpoint are:

- Direction TX/RX
- Speed: High/full/low
- Special host settings when used in host mode (function address/hub parameters, etc.)
- Transaction protocol: Control/isochronous/bulk/interrupt
- Maximum packet size, that can be transferred through the endpoint
- Whether DMA is required (DMA enable)
- DMA mode
- Start address of the endpoint FIFO within the RAM block
- Maximum packet size allowed
- Whether double-buffering is required. This and the previous option define the amount of space that must be allocated to the FIFO. In the case of double-buffering, the FIFO size is doubled; therefore, the maximum supported size is 8196 bytes for the endpoint FIFOs.

NOTE: On the system level, it must be ensured that the reset and the interface are selected before the functional clock (OTG_60M_FCLK) is applied to the module. Correct functionality is not ensured if a reset deassertion or a change in the interface selection occurs when the functional clock OTG_60M_FCLK is already running.

23.12.4.5.2 Transaction Handling

Depending on whether the module is in the host or peripheral mode, an RX endpoint is assigned to IN or OUT transactions, respectively. Similarly, a TX endpoint is used for IN transactions in the peripheral mode and for OUT transactions in the host mode. When a transaction is complete, the appropriate endpoint interrupt is generated (if enabled).

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When a transaction is handled through an RX endpoint, the received packet is placed in the RX FIFO, and the appropriate RX endpoint interrupt is generated. The packet can then be unloaded from the FIFO either manually (that is, by the MPU) or by the DMA. Although an RX endpoint is always active for a peripheral, in host mode the transaction must first be initiated by setting the appropriate request flag (REQPKT). This indicates to the transaction scheduler that there is an active transaction on this endpoint, which requires an IN token to be sent to the target function.

When a transaction is handled through a TX endpoint, the packet to send is loaded into the TX FIFO either manually (that is, by the MPU) or by the DMA. The transaction then must be initiated by setting the appropriate ready flag (TXPKTRDY) to indicate the availability of the new packet. When the packet is successfully sent (scheduled according to the protocol rules), the appropriate TX interrupt is generated.

23.12.4.6 Optional Features

This section gives a quick overview of the optional features that are available, depending on the endpoint configuration.

23.12.4.6.1 Double Packet Buffering

When double packet buffering is enabled (by setting the MSB of the FIFOSZ register two data packets can be stored in the FIFO. This option can be set for both the TX and RX endpoints in both the peripheral and host mode. For a TX endpoint, double-buffering means that up to two packets can be loaded into the FIFO awaiting transmission; for an RX endpoint, one packet can be received while another is being read. Double packet buffering is especially advisable for isochronous transactions to avoid underrun or overrun errors.

The high-speed USB controller provides dynamic FIFO sizing with an overall RAM size of 16KB, which can then be allocated to the different endpoints when the module is initialized. The maximum size of an endpoint FIFO is 4096 bytes for single packet buffering and 8192 bytes for double packet buffering. The firmware must ensure that a block of RAM is properly assigned to all TX and RX endpoints, considering the total RAM size and the maximum packet size set for the endpoint.

23.12.4.6.2 USBOTGHS Support for Big Endian

In the example in Figure 23-259, the high-speed USB OTG controller module is configured as a USB device and is connected to a standard USB host. The two interconnect interfaces of the high-speed USB OTG controller connect it to the system bus. The register read/write is performed through the interconnect slave interface (control path). The data transfer to/from system memory takes place through the interconnect master interface (data path).

The data transfer on USB is always in little-endian mode, but on interconnect it can be in little- or big-endian mode, as shown in Figure 23-259.

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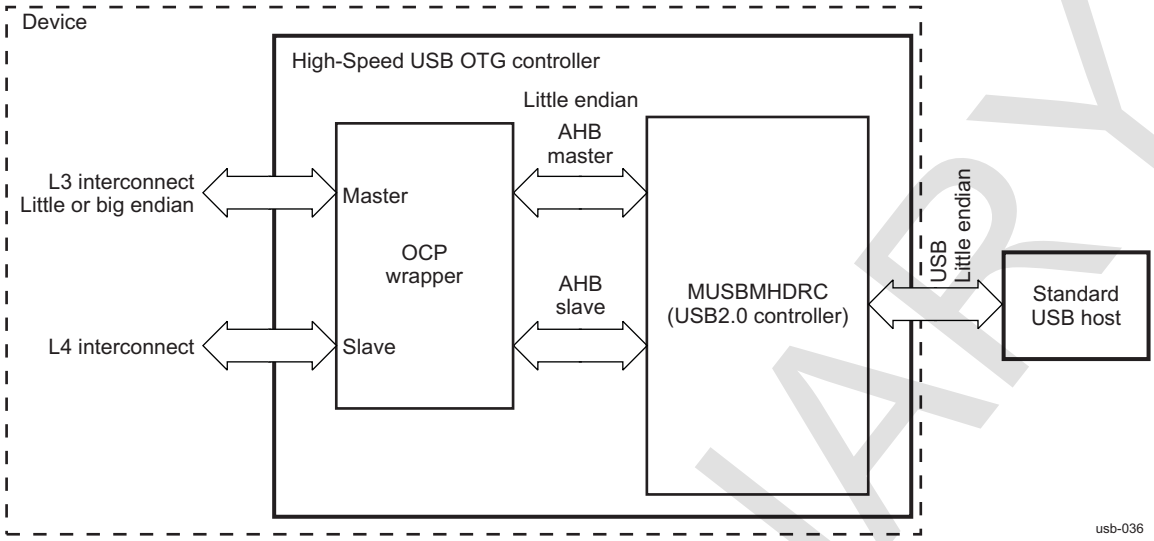
Figure 23-259. High-Speed USB OTG Controller Endianness



Big-endian support in the high-speed USB OTG controller may or may not require byte-swapping in the data path. Byte-swapping is performed based on the unit size of data. For example, if multiple bytes are packed into a single 32-bit word, these bytes must be swapped in a big-endian interconnect. On the other hand, if the data is simply a 32-bit word (for example, a 32-bit descriptor pointer in a memory buffer), the bytes in the word must not be swapped in big-endian mode.

In the high-speed USB OTG controller, the unit size of descriptors/descriptor pointers is 32 bits, and the unit size of USB data is 8 bits. Four 8-bit USB data are packed to form a 32-bit word. This 32-bit data requires byte-swapping, whereas the descriptors/descriptor pointers do not require byte-swapping.

NOTE: Byte-swapping is not required in the control path (slave interface).

The interconnect master interface (a submodule within the interconnect wrapper) supports big-endian conversion by setting the OTG_BIGENDIAN[0] BIG_ENDIAN bit to 0x1.

For interconnect write transactions, the data word is swapped, as shown in Table 23-1169, before its output on the interconnect master interface. In case of an interconnect read transaction, the received data is swapped before its output on the AHB master interface of the MUSBMHDRC core. The interconnect MByteEn is swapped before the command is issued on the interconnect master interface. The interconnect MAddr is always aligned to the size of the interconnect data (32 bits). Hence, the interconnect MAddr is always word-aligned.

Table 23-1169. Interconnect Data and MByteEn in Little- and Big-Endian Modes

Unit Size of Data	AHB Size (of Packed/Nonpacked Data)	AHB Start Address Offset (Always in Little-Endian Mode)	Interconnect MByteEn in Little-Endian Mode	Interconnect MByteEn in Big-Endian Mode	Interconnect Data in Little-Endian Mode	Interconnect Data in Big-Endian Mode
Byte	Byte	0	0001	1000	xxxb0	b0xxx
Byte	Byte	1	0010	0100	xxb0x	xb0xx
Byte	Byte	2	0100	0010	xb0xx	xxb0x
Byte	Byte	3	1000	0001	b0xxx	xxxb0
Byte	Half-word	0	0011	1100	xxb1b0	b0b1xx
Byte	Half-word	2	1100	0011	b1b0xx	xxb0b1
Byte	Word	0	1111	1111	b3b2b1b0	b0b1b2b3
Half-word	Half-word(1)	0	0011	1100	xxb1b0	b1b0xx

(1) Not a likely scenario for high-speed USB OTG controller

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Table 23-1169. Interconnect Data and MByteEn in Little- and Big-Endian Modes (continued)

Unit Size of Data	AHB Size (of Packed/Nonpacked Data)	AHB Start Address Offset (Always in Little-Endian Mode)	Interconnect MByteEn in Little-Endian Mode	Interconnect MByteEn in Big-Endian Mode	Interconnect Data in Little-Endian Mode	Interconnect Data in Big-Endian Mode
Half-word	Half-word(1)	2	1100	0011	b1b0xx	xxb1b0
Half-word	Word(1)	0	1111	1111	b3b2b1b0	b1b0b3b2
Word	Word(2)	0	1111	1111	b3b2b1b0	b3b2b1b0

(2) Corresponds to descriptor and descriptor pointer. No bytes are packed to form a word; hence, no byte-swapping is done in this case.

23.12.4.6.3 DMA

The high-speed USB controller has an internal DMA controller for efficient loading/unloading of the endpoint FIFOs. The DMA controller is configured for 8 channels and it has its own block of control registers and its own interrupt controller

If the DMA is enabled for a TX endpoint, a DMA transfer occurs whenever the endpoint can accept another packet in its FIFO (that is, the DMA controller loads the packets into the FIFO without processor intervention).

If the DMA is enabled for an RX endpoint, a DMA transfer occurs whenever the endpoint has a packet in its FIFO (that is, the DMA CONTROLLER unloads the packets from the FIFO without processor intervention).

The high-speed USB controller supports two DMA request modes, which also affects the generation of endpoint interrupts.

- DMA request mode 0 is especially advisable for isochronous transfers but can also be used for bulk and interrupt transfers.
- DMA request mode 1 is mainly valuable for bulk transfers, where typically a large block of data is split into a series of packets of the maximum size.

23.12.4.6.3.1 DMA Request Mode 0

For RX endpoints, the DMA transfer is initiated when a data packet is available in the endpoint FIFO. The appropriate endpoint interrupt is also generated after the packets are received.

For TX endpoints, the DMA transfer is initiated when the endpoint FIFO can accept a data packet. The appropriate endpoint interrupt is also generated to prompt the loading of the packets.

23.12.4.6.3.2 DMA Request Mode 1

For RX endpoints the DMA transfer is initiated only when the received packet is the maximum packet size (as set in the RXMAXP register for the corresponding endpoint). The appropriate endpoint interrupt is generated only when the received packet is a short packet (that is, one less than the maximum packet size); otherwise, it is suppressed.

For TX endpoints, the DMA transfer is initiated when the endpoint FIFO can accept a data packet. The appropriate endpoint interrupt is suppressed.

23.12.4.6.3.3 Internal DMA Controller

The high-speed USB controller has an internal DMA controller to perform DMA transfers acting as host on the L3 interconnect. The DMA controller has eight channels, which can be independently programmed based on the following configuration options:

- DMA enable
- Direction (DMA write/DMA read)
- DMA mode (transfer one or more packets)

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- Interrupt enable
- Endpoint number
- L3 interconnect memory address (32 bits)
- Byte count

The DMA controller can issue single accesses (8-bit, 16-bit, or 32-bit) and also bursts (4 × 32-bit, 8 × 32-bit, or 16 × 32-bit) on the L3 interconnect. The start address provided to the DMA controller must be 32-bit aligned.

23.12.4.7 Automatic Packet Splitting/Combining for Bulk Transfers

The high-speed USB controller offers the facility for bulk endpoints to store larger amounts of data in their FIFOs than can be transferred in a single USB operation. In other words, the module includes a configuration option that, if selected, allows larger data packets to be written to bulk TX endpoints, which are then split into packets of an appropriate size for transfer across the USB. A similar option exists for bulk RX endpoints, which, if selected, causes the module to combine the packet received across the USB into larger data packets before being read by the application software.

The firmware can enable these options by setting the corresponding bits (MPRXE and MPTXE) in the CONFIGDATA register. The necessary packet size information contains the payload size for one transaction and a multiplier defining the maximum number of USB packets. The payload is required to be either 8, 16, 32, 64, or (in case of high-speed transfers) 512 bytes; the multiplier can be any value up to 32.

23.12.4.8 High-Bandwidth Isochronous Endpoints

In the high-speed mode, isochronous endpoints can transfer up to three USB packets in any microframe with a payload of up to 1024 bytes in each packet, corresponding to a data transfer rate of up to 3072 bytes per microframe (see *Universal Serial Bus Specification Revision 2.0*).

For TX endpoints, the high-speed USB controller supports this by allowing loading data packets of up to 3072 bytes (that is, 3 × 1024 bytes) into the associated endpoint FIFO, which is then automatically split into USB packets of the maximum payload, or smaller to be transmitted in one microframe.

For RX endpoints, the module automatically combines all the USB packets received during a microframe into a single packet of up to 3072 bytes (that is, 3 ×1024 bytes) within the RX FIFO.

The number of USB packets transferred per microframe and the maximum payload in each packet is defined through the appropriate registers (RXMAXP and TXMAXP).

23.12.4.9 Carkit Implementation

Carkit feature implementation:

UART3 RX/TX muxing on the usba0_ulpiphy_dat0 and usba0_ulpiphy_dat1. To support carkit interrupt through USB0HS.DATA3, three different methods can be used:

- External PHY interrupt if provided: IRQ_SYS interrupt
- UART3 interrupt: CTS edge detection
- GPIO interrupt: Edge detection on GPIO associated to usba0_ulpiphy_dat3 line

23.12.4.10 USB PHY

The device-embedded USB PHY is composed of the following modules:

- USB2PHYCORE: Contains the USB functions, drivers, receivers, and pads for correct D+/D– signaling, and the battery charger detection (supporting dead-battery mode). Delivers a 3.3-V output signal (charger enable [pin usba0_otg_ce]) to control an external battery charger.
- USB2PHYCM: Contains LDO and bandgap to provide voltage reference to the USB2PHYCORE module

The embedded PHY does not support the OTG features of USB-OTG standards (that is, ID pin detection

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and VBUS detection). This function is exported to an external companion chip (for example, the TWL6030). Software must retrieve the OTG HNP and SRP status from the TWL6030 (using the I2C1 interface) and configure the bits inside the control module that drive the related USBOTGHS UTMI+ interface signals. It must also read back the UTMI+ signals needed to configure the TWL6030 OTG module.

These signals are:

- Inputs of the USB controller driven by the control module:
  - Avalid: Indicates whether VBUS is above the A-Device session valid threshold
  - Bvalid (currently not used)
  - Vbusvalid: Indicates whether VBUS is above the threshold for normal operation
  - Sessend: Indicates whether VBUS is below the B-Device session end threshold
  - Iddig: Indicates the value of the ID pin of the USB connector
- Outputs of the USB controller readable in the control module:
  - Idpullup: Enables sampling of the ID pin of the USB connector
  - Drv vbus: Controls the driving of 5-V power on VBUS
  - Chrg vbus: Controls the charging of VBUS for initiating SRP
  - Dischrg vbus: Controls the discharging of VBUS for completing SRP

See the CONTROL_USBOTGHS_CONTROL register in Chapter 18, *Control Module*, and the TWL6030 documentation.

The following UTMI signals are not connected:

- Txbitstuffenable (no bit-stuffing out from the USB controller)
- Txbitstuffenableh (because only 8 bits are used)

The following USBPHY signals are routed internally to the GPIO6 module pins to generate interrupts when any of the following events occur:

- CHGDETECTED: This signal indicates the output of the charger detection protocol.

  0: Charger not detected

  1: Charger detected

  The value is latched until the charger protocol is reset.
- DPDM5VSHORT: This signal is asserted high if a short-circuit-to-VBUS condition is detected on the USB DP or DM pins. This signal is valid only if all power supplies are present. The short is detected if any or even none of the supplies are present.

  0: No short

  1: VBUS short on DP or DM detected

For information about how to enable these interrupts, see Chapter 25, *General-Purpose Interface*.

The USBPHY internal registers are listed in Section 23.12.6.3, *USBPHY Registers*, for debug purposes.

CAUTION

For a correct read out of the USBPHY registers, the value of the OCP2SCP_TIMING[3:0] SYNC2 bit field must be set to 0x6 or more, and the OCP2SCP_TIMING[9:7] DIVISIONRATIO bit field must be left untouched.

23.12.5 High-Speed USB OTG Controller Basic Programming Model

This section describes the low-level hardware programming sequences for configuration and use of the high-speed USB OTG controller.

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23.12.5.1 Global Initialization

23.12.5.1.1 Surrounding Modules Global Initialization

This section identifies the requirements of initializing the surrounding modules when the high-speed USB OTG controller is to be used for the first time after a device reset. This initialization of surrounding modules is based on the integration of the high-speed USB OTG controller.

Table 23-1170. Global Initialization of Surrounding Modules

Surrounding Modules	Comments
PRCM	All required clocks must be enabled, see Table 23-1165. Do not apply OTG_60M_FCLK clock before the interface is selected. Refer to the
Cortex-A9 MPU INTC or Cortex-M3 MPU INTC	Cortex-A9 MPU or Cortex-M3 MPU interrupt controller must be configured to enable the interrupt request generation to the Cortex-A9 MPU or Cortex-M3 MPU subsystem when interrupt requests are generated by the High-Speed Multiport USB Host Subsystem. See the respective Functional Description in the Interrupt Controller chapter for the MPUs.
Interconnect (L3 and L4)	See Section 13.2, *L3 Interconnect*, and Section 13.3, *L4 Interconnect*, for more information.

23.12.5.1.2 High-Speed USB OTG Controller Global Initialization

This procedure initializes the high-speed multiport USB host sybsystem after a power-on or software reset. The module USBPHY is reset through boundary reset signal L3_INIT_RST coming from PRCM module.

Table 23-1171. High-Speed USB OTG Software Reset

Step	Register/Bit Field/Programming Model	Value
Perform a software reset on the USB OTG controller	OTG_SYSCONFIG[1] SOFTRESET	0x1
Wait until reset is finished	OTG_SYSSTATUS[0] RESETDONE	=0x1

Table 23-1172. Power Management Configuration

Step	Register/Bit Field/Programming Model	Value
Select master interface standby mode	OTG_SYSCONFIG[13:12] MIDLEMODE	0x-
Select slave interface idle mode	OTG_SYSCONFIG[4:3] SIDLEMODE	0x-
Set clock autogating	OTG_SYSCONFIG[0] AUTOIDLE	0x-

23.12.5.2 High-Speed USB OTG Controller Interface Modes

This procedure describes TI high-speed USB controller interface selection:

Table 23-1173. High-Speed USB Controller Interface Selection

Step	Register/Bit Field/Programming Model	Value
Select between embedded and external PHY interface	OTG_INTERFSEL[2:0] PHYSEL	0x-
Enable functional PHY clock (OTG_60M_FCLK)	Refer to	-

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23.12.5.3 High-Speed USB OTG Controller Power Management Configuration

This section describes the settings for optimal high-speed USB controller power management, depending on the use of this module in the application.

23.12.5.3.1 No Application Mode

The optimal configuration when the high-speed USB controller is not used by the application is as follows:

Table 23-1174. Power Management Configuration - No Application Mode

Step	Register/Bit Field/Programming Model	Value
Switch master interface to force standby mode	OTG_SYSCONFIG[13:12] MIDLEMODE	0x0
Switch slave interface to force-idle mode	OTG_SYSCONFIG[4:3] SIDLEMODE	0x0
Set the clock to smart mode - clock is cut-off if no activity on the interface	OTG_SYSCONFIG[0] AUTOIDLE	0x1

23.12.5.3.2 Host or Peripheral Mode

When used as a host or in peripheral mode, the high-speed USB controller must be programmed as follows:

Table 23-1175. Power Management Configuration - Host or Peripheral Mode

Step	Register/Bit Field/Programming Model	Value
Switch Master interface to smart standby mode	OTG_SYSCONFIG[13:12] MIDLEMODE	0x2
Switch Slave interface to smart-idle mode	OTG_SYSCONFIG[4:3] SIDLEMODE	0x2
Set the clock to smart mode - clock is cut-off if no activity on the interface	OTG_SYSCONFIG[0] AUTOIDLE	0x1

23.12.5.3.3 Switching Between Host and Peripheral Mode

When used as a host/peripheral, the high-speed USB OTG controller must be programmed as follows:

Table 23-1176. Power Management Configuration - Switching Between Host and Peripheral Mode

Step	Register/Bit Field/Programming Model	Value
Switch Master interface to force standby mode	OTG_SYSCONFIG[13:12] MIDLEMODE	0x0
Switch Slave interface to smart-idle mode	OTG_SYSCONFIG[4:3] SIDLEMODE	0x2
Set the clock to smart mode - clock is cut-off if no activity on the interface	OTG_SYSCONFIG[0] AUTOIDLE	0x1

23.12.6 High-Speed USB OTG Controller Register Manual

This section presents only the TI-specific registers of the high-speed USB controller.

Table 23-1177 lists the base address and address space for the high-speed USB controller.

Table 23-1177. High-Speed USB OTG Controller Instance Summary

Module Name	Base Address	Size
HSUSBOTG	0x4A0A B000	4KB
OCP2SCP	0x4A0A D000	64 bytes
USBPHY	0x4A0A D080	3968 bytes

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23.12.6.1 HSUSBOTG Registers

23.12.6.1.1 HSUSBOTG Register Summary

Table 23-1178. HSUSBOTG Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	Physical Address
OTG_REVISION	R	32	0x0000 0400	0x4A0A B400
OTG_SYSCONFIG	RW	32	0x0000 0404	0x4A0A B404
OTG_SYSSTATUS	R	32	0x0000 0408	0x4A0A B408
OTG_INTERFSEL	RW	32	0x0000 040C	0x4A0A B40C
OTG_SIMENABLE	RW	32	0x0000 0410	0x4A0A B410
OTG_FORCESTDBY	RW	32	0x0000 0414	0x4A0A B414
OTG_BIGENDIAN	RW	32	0x0000 0418	0x4A0A B418

23.12.6.1.2 HSUSBOTG Register Description

Table 23-1179. OTG_REVISION

Address Offset	0x0000 0400		
Physical Address	0x4A0A B400	**Instance**	HSUSBOTG
Description	OCP standard USB OTG HS core revision number		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

Bits	Field Name	Description	Type	Reset
31:0	RESERVED	IP Revision	R	See (1)

(1) TI internal data

Table 23-1180. Register Call Summary for Register OTG_REVISION

High-Speed USB OTG Controller

- HSUSBOTG Register Summary: [0]

Table 23-1181. OTG_SYSCONFIG

Address Offset	0x0000 0404		
Physical Address	0x4A0A B404	**Instance**	HSUSBOTG
Description	OCP standard configuration		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																MIDLEMODE		RESERVED						SIDLEMODE		ENABLEWAKEUP		SOFTRESET		AUTOIDLE	

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Bits	Field Name	Description	Type	Reset
31:14	RESERVED	reserved	R	0x00000
13:12	MIDLEMODE	Master interface power management control. Standby/wait control 0x0: Force standby mode. Mstandby asserted unconditionally 0x1: No standby mode. Mstandby never asserted. 0x2: Smart standby mode. Mstandby asserted when no more activity on the USB master.	RW	0x2
11:5	RESERVED	reserved	R	0x00
4:3	SIDLEMODE	Slave interface power management control. Req/ack control 0x0: Force Idle mode. Sidleack asserted after Midlereq assertion 0x1: No idle mode. Sidleack never asserted. 0x2: SmartIdle mode. Sidleack asserted after Midlereq assertion when no more activity on the USB. Swakeup is not asserted in this mode. 0x3: SmartIdle - Wakeup mode. Sidleack asserted after Midlereq assertion when no more activity on the USB. Swakeup is asserted in this mode if ENABLEWAKEUP is set.	RW	0x2
2	ENABLEWAKEUP	Enable wakeup capability. 0x0: Wakeup disabled 0x1: Wakeup enabled	RW	0
1	SOFTRESET	Software reset bit 0x1: Starts softreset sequence.	RW	0
0	AUTOIDLE	Autoidle bit 0x0: Clock always runnning 0x1: When no activity on OCP, clock is cut off.	RW	1

Table 23-1182. Register Call Summary for Register OTG_SYSCONFIG

High-Speed USB OTG Controller

- Software Reset: [0]
- System Power Management: [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18]
- Local Power Management: [19]
- High-Speed USB OTG Controller Global Initialization: [20] [21] [22] [23]
- No Application Mode: [24] [25] [26]
- Host or Peripheral Mode: [27] [28] [29]
- Switching Between Host and Peripheral Mode: [30] [31] [32]
- HSUSBOTG Register Summary: [33]

Table 23-1183. OTG_SYSSTATUS

Address Offset	0x0000 0408		
Physical Address	0x4A0A B408	**Instance**	HSUSBOTG
Description	OCP standard status		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															RESETDONE

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Bits	Field Name	Description	Type	Reset
31:1	RESERVED	reserved	R	0x0000 0000
0	RESETDONE	Reset done Read 0x0: Reset is ongoing Read 0x1: Reset is finished.	R	1

Table 23-1184. Register Call Summary for Register OTG_SYSSTATUS

High-Speed USB OTG Controller

- Software Reset: [0]
- High-Speed USB OTG Controller Global Initialization: [1]
- HSUSBOTG Register Summary: [2]

Table 23-1185. OTG_INTERFSEL

Address Offset	0x0000 040C		
Physical Address	0x4A0A B40C	**Instance**	HSUSBOTG
Description	USB OTG HS interface selection. The interface selection has to be done before the PHY is activated and is not allowed to change when the PHY clock is already running.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														PHYSEL	

Bits	Field Name	Description	Type	Reset
31:3	RESERVED	reserved	R	0x0000 0000
2:0	PHYSEL	PHY interface selection 0x0: PHY interface is 8-bit, UTMI+ level 3 0x1: PHY interface is 12-pin, 8-bit SDR ULPI 0x2: PHY interface is 8-pin, 4-bit DDR ULPI (Non-functional mode in current implementation. Do not use.)	RW	0x1

Table 23-1186. Register Call Summary for Register OTG_INTERFSEL

High-Speed USB OTG Controller

- High-Speed USB OTG Controller Environment: [0] [1]
- High-Speed USB OTG Controller Interface Modes: [2]
- HSUSBOTG Register Summary: [3]

Table 23-1187. OTG_SIMENABLE

Address Offset	0x0000 0410		
Physical Address	0x4A0A B410	**Instance**	HSUSBOTG
Description	Enable simulation acceleration features. WARNING: For simulations only, since those features have an impact on USB protocol.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															TM1

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Bits	Field Name	Description	Type	Reset
31:1	RESERVED	reserved	R	0x0000 0000
0	TM1	Test Mode 1 enabling (timer shortcuts)	RW	0

Table 23-1188. Register Call Summary for Register OTG_SIMENABLE

High-Speed USB OTG Controller

- HSUSBOTG Register Summary: [0]

Table 23-1189. OTG_FORCESTDBY

Address Offset	0x0000 0414		
Physical Address	0x4A0A B414	**Instance**	HSUSBOTG
Description	Enabling MSTANDBY in FORCESTANDBY mode. Programming this register will impact SmartStandby functionality.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															ENABLEFORCE

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	ENABLEFORCE	Enabling MSTANDBY to go high	RW	0

Table 23-1190. Register Call Summary for Register OTG_FORCESTDBY

High-Speed USB OTG Controller

- HSUSBOTG Register Summary: [0]

Table 23-1191. OTG_BIGENDIAN

Address Offset	0x0000 0418		
Physical Address	0x4A0A B418	**Instance**	HSUSBOTG
Description	Enable BIG ENDIANESS for OCP MASTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															BIG_ENDIAN

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	BIG_ENDIAN	Enable BIG ENDIAN in OCP MASTER	RW	0

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Table 23-1192. Register Call Summary for Register OTG_BIGENDIAN

High-Speed USB OTG Controller
- USBOTGHS Support for Big Endian: [0]
- HSUSBOTG Register Summary: [1]

23.12.6.2 OCP2SCP Registers

23.12.6.2.1 OCP2SCP Register Summary

CAUTION

The OCP2SCP registers are limited to 32-bit data accesses; 16- and 8-bit accesses are not allowed and can corrupt register content.

Table 23-1193. OCP2SCP Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	Physical Address
OCP2SCP_REVISION	R	32	0x0000 0000	0x4A0A D000
OCP2SCP_SYSCONFIG	RW	32	0x0000 0010	0x4A0A D010
OCP2SCP_SYSSTATUS	R	32	0x0000 0014	0x4A0A D014
OCP2SCP_TIMING	RW	32	0x0000 0018	0x4A0A D018

23.12.6.2.2 OCP2SCP Register Description

Table 23-1194. OCP2SCP_REVISION

Address Offset	0x0000 0000		
Physical Address	0x4A0A D000	**Instance**	OCP2SCP
Description	IP revision identifier		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP revision number	R	See (1)

(1) TI internal data

Table 23-1195. Register Call Summary for Register OCP2SCP_REVISION

High-Speed USB OTG Controller
- OCP2SCP Register Summary: [0]

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Table 23-1196. OCP2SCP_SYSCONFIG

Address Offset	0x0000 0010		
Physical Address	0x4A0A D010	**Instance**	OCP2SCP
Description	System configuration register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																											IDLEMODE		RESERVED	SOFTRESET	AUTOIDLE

Bits	Field Name	Description	Type	Reset
31:5	RESERVED	Reserved	R	0x0000000
4:3	IDLEMODE	Module power management control 0x0: Force-idle mode. An idle request is acknowledged unconditionally. 0x1: No-idle mode. An idle request is never acknowledged. 0x2: Smart-idle mode. The acknowledgment to an idle request is given based on the internal activity. 0x3: Reserved	RW	0x2
2	RESERVED	Reserved	R	0
1	SOFTRESET	Software reset. Set this bit to 1 to trigger a module reset. During reads, it always returns 0. 0: Normal mode 1: The module is reset.	RW	0
0	AUTOIDLE	OCP clock-gating control 0: Internal interface OCP clock is free-running. 1: Automatic internal OCP clock gating, based on the OCP interface activity	RW	1

Table 23-1197. Register Call Summary for Register OCP2SCP_SYSCONFIG

High-Speed USB OTG Controller

- OCP2SCP Register Summary: [0]

Table 23-1198. OCP2SCP_SYSSTATUS

Address Offset	0x0000 0014		
Physical Address	0x4A0A D014	**Instance**	OCP2SCP
Description	System status register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															RESETDONE

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Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	RESETDONE	0: Internal reset is on-going. 1: Reset is complete.	R	1

Table 23-1199. Register Call Summary for Register OCP2SCP_SYSSTATUS

High-Speed USB OTG Controller

- OCP2SCP Register Summary: [0]

Table 23-1200. OCP2SCP_TIMING

Address Offset	0x0000 0018		
Physical Address	0x4A0A D018	**Instance**	OCP2SCP
Description	Timing configuration register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						DIVISIONRATIO		SYNC1				SYNC2			

Bits	Field Name	Description	Type	Reset
31:10	RESERVED	Reserved	R	0x000000
9:7	DIVISIONRATIO	Division ratio of the SCP clock in relation to the OCP input clock. When the value 0x0 is programmed, and the transaction to be made is a valid transaction on the SCP interface, the value of DIVISIONRATIO is set to 0x7 by hardware to avoid a block on the OCP interface. **CAUTION:** To ensure correct operation, DIVISIONRATIO must not be modified. See also the SYNC2 description.	RW	0x0
6:4	SYNC1	Number of SCP clock cycles defining SYNC1 delay	RW	0x0
3:0	SYNC2	Number of SCP clock cycles defining the SYNC2 delay. When the value 0x0 is programmed, and the transaction to be made is a valid transaction on the SCP interface, SYNC2 is set to the minimum allowed value 0x1 to avoid a block on the OCP interface. **CAUTION:** To ensure correct operation, the value of SYNC2 must be set to 0x6 or more.	RW	0x1

Table 23-1201. Register Call Summary for Register OCP2SCP_TIMING

High-Speed USB OTG Controller

- USB PHY: [0] [1]
- OCP2SCP Register Summary: [2]

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23.12.6.3 USBPHY Registers

23.12.6.3.1 USBPHY Register Summary

CAUTION

The USBPHY registers are limited to 32-bit data accesses; 16- and 8-bit accesses are not allowed and can corrupt register content.

Table 23-1202. USBPHY Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	Physical Address
USBPHY_TERMINATION_CONTROL	RW	32	0x0000 0000	0x4A0A D080
USBPHY_RX_CALIB	RW	32	0x0000 0004	0x4A0A D084
USBPHY_DLLHS_2	RW	32	0x0000 0008	0x4A0A D088
USBPHY_RX_TEST_2	RW	32	0x0000 000C	0x4A0A D08C
USBPHY_TX_TEST_CHRG_DET	RW	32	0x0000 0010	0x4A0A D090
USBPHY_CHRG_DET	RW	32	0x0000 0014	0x4A0A D094
USBPHY_PWR_CNTL	RW	32	0x0000 0018	0x4A0A D098
USBPHY_UTMI_INTERFACE_CNTL_1	RW	32	0x0000 001C	0x4A0A D09C
USBPHY_UTMI_INTERFACE_CNTL_2	RW	32	0x0000 0020	0x4A0A D0A0
USBPHY_BIST	RW	32	0x0000 0024	0x4A0A D0A4
USBPHY_BIST_CRC	RW	32	0x0000 0028	0x4A0A D0A8
USBPHY_CDR_BIST2	RW	32	0x0000 002C	0x4A0A D0AC
USBPHY_GPIO	RW	32	0x0000 0030	0x4A0A D0B0
USBPHY_DLLHS	RW	32	0x0000 0034	0x4A0A D0B4
USBPHY_USB2PHYCM_TRIM	RW	32	0x0000 0038	0x4A0A D0B8
USBPHY_USB2PHYCM_CONFIG	RW	32	0x0000 003C	0x4A0A D0BC
USBPHY_USBOTG	RW	32	0x0000 0040	0x4A0A D0C0
USBPHY_AD_INTERFACE_REG1	RW	32	0x0000 0044	0x4A0A D0C4
USBPHY_AD_INTERFACE_REG2	RW	32	0x0000 0048	0x4A0A D0C8
USBPHY_AD_INTERFACE_REG3	RW	32	0x0000 004C	0x4A0A D0CC
USBPHY_ANA_CONFIG1	RW	32	0x0000 0050	0x4A0A D0D0
USBPHY_ANA_CONFIG2	RW	32	0x0000 0054	0x4A0A D0D4

23.12.6.3.2 USBPHY Register Description

Table 23-1203. USBPHY_TERMINATION_CONTROL

Address Offset	0x0000 0000		
Physical Address	0x4A0A D080	**Instance**	USBPHY
Description	Contains bits related to control of terminations in USBPHY		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		ALWAYS_UPDATE	RTERM_CAL_DONE	FS_CODE_SEL				RESERVED		USE_RTERM_RMX_REG	RTERM_RMX							HS_CODE_SEL			RTERM_COMP_OUT	RESTART_RTERM_CAL	DISABLE_TEMP_TRACK	USE_RTERM_CAL_REG	RTERM_CAL						

Bits	Field Name	Description	Type	Reset
31:30	RESERVED	reserved	RW	0x0
29	ALWAYS_UPDATE	When set to 1, the calibration code is updated immediately after a code computation without waiting for idle periods.	RW	0
28	RTERM_CAL_DONE	Rterm calibration is done. First time cal is done this bit gets set and gets reset at a restart cal. Read value is valid only if VDDLDO is on.	R	0
27:24	FS_CODE_SEL	FS Code selection control	RW	0x1
23:22	RESERVED	reserved	RW	0x0
21	USE_RTERM_RMX_REG	Override termination resistor trim code with RTERM_RMX from this register	RW	0
20:14	RTERM_RMX	When read, this field returns the current Termination resistor trim code. Read value is valid only if VDDLDO is on. The value written to this field is used as Termination resistor trim code if bit 21 is set to 1	RW	0x00
13:11	HS_CODE_SEL	HS Code selection control	RW	0x1
10	RTERM_COMP_OUT	Master loop comparator output. Read value is valid only if VDDLDO is on.	R	0
9	RESTART_RTERM_CAL	Restart the rterm calibration. the calibration restarts on any toggle 0-1 or 1-0 on this bit.	RW	0
8	DISABLE_TEMP_TRACK	Disables the temperature tracking function of the termination calibration	RW	0
7	USE_RTERM_CAL_REG	When 1, the rterm cal code is overridden by values in RTERM_CAL	RW	0
6:0	RTERM_CAL	When read this field returns the current rterm calibration code. Read value is valid only if VDDLDO is on. The value written to this filed is used as rterm calibration code if the bit USE_RTERM_CAL_REG is 1.	RW	0x00

Table 23-1204. Register Call Summary for Register USBPHY_TERMINATION_CONTROL

High-Speed USB OTG Controller

- USBPHY Register Summary: [0]

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Table 23-1205. USBPHY_RX_CALIB

Address Offset	0x0000 0004		
Physical Address	0x4A0A D084	**Instance**	USBPHY
Description	Contains bits related to RX calibration		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESTART_HSRX_CAL	USE_HS_OFF_REG	HS_OFF_CODE						HSRX_COMP_OUT	HSRX_CAL_DONE	USE_SQ_OFF_DAC1	SQ_OFF_CODE_DAC1					USE_SQ_OFF_DAC2	SQ_OFF_CODE_DAC2						USE_SQ_OFF_DAC3	SQ_OFF_CODE_DAC3					SQ_COMP_OUT	SQ_CAL_DONE	RESTART_SQ_CAL

Bits	Field Name	Description	Type	Reset
31	RESTART_HSRX_CAL	Restart the HSRX calibration state machine when this bit goes from 0 to 1.	RW	0
30	USE_HS_OFF_REG	Override HS offset correction with HS_OFF_CODE when set to 1	RW	0
29:24	HS_OFF_CODE	HS offset code, this code is forced when bit 30 is 1. Code is updated from calibration logic when bit 30 = 0.	RW	0x00
23	HSRX_COMP_OUT	The output of the HSRX comparator. Read value is valid only if VDDLDO is on.	R	0
22	HSRX_CAL_DONE	Signal that indicates that the HSRX calibration is done. This gets reset at every restart. Read value is valid only if VDDLDO is on.	R	0
21	USE_SQ_OFF_DAC1	Override Squelch offset DAC1 code when '1'	RW	0
20:15	SQ_OFF_CODE_DAC1	When read returns current Sq offset code for DAC1, if VDDLDO is on. When written this is used as Sq offset code for DAC1 when USE_SQ_OFF_DAC1 = 1	RW	0x00
14	USE_SQ_OFF_DAC2	Override Squelch offset DAC2 code when '1'	RW	0
13:9	SQ_OFF_CODE_DAC2	When read returns current Sq offset code for DAC2, if VDDLDO is on. When written this is used as Sq offset code for DAC2 when USE_SQ_OFF_DAC2 = 1	RW	0x00
8	USE_SQ_OFF_DAC3	Override Squelch offset DAC3 code when 1	RW	0
7:3	SQ_OFF_CODE_DAC3	When read returns current Sq offset code for DAC3, if VDDLDO is on. When written this is used as Sq offset code for DAC3 when USE_SQ_OFF_DAC3 = 1	RW	0x00
2	SQ_COMP_OUT	Sq comp output.Read value is valid only if VDDLDO is on.	R	0
1	SQ_CAL_DONE	Sq calibration is done when this bit = 1. See RESTART_SQ_CAL for more description. Read value is valid only if VDDLDO is on.	R	0
0	RESTART_SQ_CAL	The squelch calibration continuously goes through restart cycles when this bit is 1.	RW	0

Table 23-1206. Register Call Summary for Register USBPHY_RX_CALIB

High-Speed USB OTG Controller

- USBPHY Register Summary: [0]

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Table 23-1207. USBPHY_DLLHS_2

Address Offset	0x0000 0008		
Physical Address	0x4A0A D088	**Instance**	USBPHY
Description	Second DLLHS control register. Bits 4:0 are unrelated to the DLLHS and are linestate filter settings.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DLLHS_CNTRL_LDO								DLLHS_STATUS_LDO								RESERVED											LINESTATE_DEBOUNCE_EN	LINESTATE_DEBOUNCE_CNTL			

Bits	Field Name	Description	Type	Reset
31:24	DLLHS_CNTRL_LDO		RW	0x00
23:16	DLLHS_STATUS_LDO		R	0x00
15:5	RESERVED	reserved	RW	0x000
4	LINESTATE_DEBOUNCE_EN	Enables the linestate debounce filter	RW	1
3:0	LINESTATE_DEBOUNCE_CNTL	Used for control of the linestate debounce filter when going from syncronous to async linestate.	RW	0xF

Table 23-1208. Register Call Summary for Register USBPHY_DLLHS_2

High-Speed USB OTG Controller

- USBPHY Register Summary: [0]

Table 23-1209. USBPHY_RX_TEST_2

Address Offset	0x0000 000C		
Physical Address	0x4A0A D08C	**Instance**	USBPHY
Description	Second receiver test register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HSOSREVERSAL	HSOSBITINVERSION	PHYCLKOUTINVERSION	RXPIDERR	USEINTDATAOUT	INTDATAOUTREG																RESERVED			CDR_TESTOUT							

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Bits	Field Name	Description	Type	Reset
31	HSOSREVERSAL	Swaps the dataout from HSOS	RW	0
30	HSOSBITINVERSION	Inverts the HSOS bits	RW	0
29	PHYCLKOUTINVERSION	This inverts the phase for the PHYCLKOUT	RW	0
28	RXPIDERR	Flags if the RX data packet has PID error. NOT IMPLEMENTED.	R	0
27	USEINTDATAOUT	This will bypass the analog and will send data packet to controller incase of receiver (Faking the receive data). data used will be INTDATAOUTREG	RW	0
26:11	INTDATAOUTREG	This register will be loaded through OCP and this data will be given to the controller if USEINTDATAOUT is set to 1	RW	0x0000
10:8	RESERVED	reserved	RW	0x0
7:0	CDR_TESTOUT	CDR debug bits. Read value is valid only if VDDLDO is on.	R	0x00

Table 23-1210. Register Call Summary for Register USBPHY_RX_TEST_2

High-Speed USB OTG Controller

- USBPHY Register Summary: [0]

Table 23-1211. USBPHY_TX_TEST_CHRG_DET

Address Offset	0x0000 0010		
Physical Address	0x4A0A D090	**Instance**	USBPHY
Description	TX test register and also charger detect register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TXSYNCERR	UTMIDATATX															RESERVED	TXPIDERR	USE_CHGDET_DPDMSW	CHGDET_DPSW0EN	CHGDET_DPSW1EN	CHGDET_DMSW0EN	CHGDET_DMSW1EN	RESERVED	RDPPDCHGDETEN	RDMPDCHGDETEN	RDPPUCHGDETEN	RDMPUCHGDETEN	USE_CHG_DET_PU_REG	USE_CHG_DET_PD_REG	RESERVED	

Bits	Field Name	Description	Type	Reset
31	TXSYNCERR	Sync error on TX data. NOT IMPLEMENTED.	R	0
30:15	UTMIDATATX	Stores Last 2 byte of transmit data coming from the controller. NOT IMPLEMENTED .	R	0x0000
14	RESERVED	reserved	RW	0
13	TXPIDERR	Flags if the TX packet has PID error. NOT IMPLEMENTED.	R	0
12	USE_CHGDET_DPDMSW	Use bits 11:8 as override bits	RW	0
11	CHGDET_DPSW0EN	Overrides the same named A/D interface signal for the charger detect block	RW	0
10	CHGDET_DPSW1EN	Overrides the same named A/D interface signal for the charger detect block. Read value is valid only if VCHGLDO is on.	RW	0
9	CHGDET_DMSW0EN	Overrides the same named A/D interface signal for the charger detect block. Read value is valid only if VCHGLDO is on.	RW	0

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Bits	Field Name	Description	Type	Reset
8	CHGDET_DMSW1EN	Overrides the same named A/D interface signal for the charger detect block..Read value is valid only if VCHGLDO is on.	RW	0
7	RESERVED	reserved	RW	0
6	RDPPDCHGDETEN	When set to 1 connects a 15K (+/- 30%) pulldown resistor on DP. Read value is valid only if VCHGLDO is on.	RW	0
5	RDMPDCHGDETEN	When set to 1 connects a 15K (+/- 30%) pulldown resistor on DM. Read value is valid only if VCHGLDO is on.	RW	0
4	RDPPUCHGDETEN	When set to 1 connects a 150K (+/- 30%) pullup resistor on DP. Read value is valid only if VCHGLDO is on.	RW	0
3	RDMPUCHGDETEN	When set to 1 connects a 150K (+/- 30%) pullup resistor on DM. Read value is valid only if VCHGLDO is on.	RW	0
2	USE_CHG_DET_PU_REG	Use bits 4:3 from this register	RW	0
1	USE_CHG_DET_PD_REG	Use bits 6:5 from this register.	RW	0
0	RESERVED	reserved	RW	0

Table 23-1212. Register Call Summary for Register USBPHY_TX_TEST_CHRG_DET

High-Speed USB OTG Controller

- USBPHY Register Summary: [0]

Table 23-1213. USBPHY_CHRG_DET

Address Offset	0x0000 0014		
Physical Address	0x4A0A D094	**Instance**	USBPHY
Description	This is the charger detect register. This register is not used in the dead battery case.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		USE_CHG_DET_REG	DIS_CHG_DET	SRC_ON_DM	SINK_ON_DP	CHG_DET_EXT_CTL	RESTART_CHG_DET	CHG_DET_DONE	CHG_DETECTED	DATA_DET	RESERVED		CHG_ISINK_EN	CHG_VSRC_EN	COMP_DP	COMP_DM	CHG_DET_OSC_CNTRL		CHG_DET_TIMER					RESERVED			CHG_DET_ICTRL		CHG_DET_VCTRL		FOR_CE

Bits	Field Name	Description	Type	Reset
31:30	RESERVED	reserved	RW	0x0
29	USE_CHG_DET_REG	Use bits 28:24 and 18:17 from this register	RW	0
28	DIS_CHG_DET	When read, returns current value of charger detect input. When USE_CHG_DET_REG = 1, the value written to this filed overrides the corresponding charger detect input.	RW	0
27	SRC_ON_DM	When read, returns current value of charger detect input. When USE_CHG_DET_REG = 1, the value written to this filed overrides the corresponding charger detect input.	RW	0
26	SINK_ON_DP	When read, returns current value of charger detect input. When USE_CHG_DET_REG = 1, the value written to this filed overrides the corresponding charger detect input.	RW	0
25	CHG_DET_EXT_CTL	When read, returns current value of charger detect input. When USE_CHG_DET_REG = 1, the value written to this filed overrides the corresponding charger detect input.	RW	0

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Bits	Field Name	Description	Type	Reset
24	RESTART_CHG_DET	Restart the charger detection protocol when this goes from 0 to 1	RW	0
23	CHG_DET_DONE	Charger detect protocol has completed	R	0
22	CHG_DETECTED	Same signal as CE pin	R	0
21	DATA_DET	Output of the data det comparator	R	0
20:19	RESERVED	reserved	RW	0x0
18	CHG_ISINK_EN	When read, returns current value of charger detect input. When USE_CHG_DET_REG = 1, the value written to this filed overrides the corresponding charger detect input.	RW	0
17	CHG_VSRC_EN	When read, returns current value of charger detect input. When USE_CHG_DET_REG = 1, the value written to this filed overrides the corresponding charger detect input.	RW	0
16	COMP_DP	Comparator on the DP line value	R	0
15	COMP_DM	Comparator on the DM line value	R	0
14:13	CHG_DET_OSC_CNTRL	Charger detect osc control	RW	0x0
12:7	CHG_DET_TIMER	Charger detect timer control.	RW	0x00
6:5	RESERVED	reserved	RW	0x0
4:3	CHG_DET_ICTRL	Charger detect current control	RW	0x0
2:1	CHG_DET_VCTRL	Charger detect voltage buffer control	RW	0x0
0	FOR_CE	Force CE = 1 when this bit is set	RW	0

Table 23-1214. Register Call Summary for Register USBPHY_CHRG_DET

High-Speed USB OTG Controller

- USBPHY Register Summary: [0]

Table 23-1215. USBPHY_PWR_CNTL

Address Offset	0x0000 0018		
Physical Address	0x4A0A D098	**Instance**	USBPHY
Description	Includes all the power control bits		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESETDONETCLK	RESET_DONE_VMAIN	VMAIN_GLOBAL_RESET_DONE	RESETDONEMCLK	RESETDONE_CHGDET	LDOPWRCOUNTER															FORCEPLLSLOWCLK	FORCELDOON	FORCEPLLON	RESERVED	PLLLOCK	USEPLLLOCK	USE_DATAPOLARITYN_REG	DATAPOLARITYN	USE_PD_REG	PD	RESERVED	

Bits	Field Name	Description	Type	Reset
31	RESETDONETCLK	Goes high when the RESET is synchronized to TCLK	R	0
30	RESET_DONE_VMAIN	Goes high when LDO domain is up, PLL LOCK is available, and utmi_reset is deasserted.	R	0
29	VMAIN_GLOBAL_RESET_DONE	Goes high when LDO domain is up and PLL LOCK is available.	R	0
28	RESETDONEMCLK	Goes high when the RESET is synchronized to MCLK	R	0

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Bits	Field Name	Description	Type	Reset
27	RESETDONE_CHGDET	Goes high when the RESET is synchronized to charger detect oscillator clock domain	R	0
26:12	LDOPWRCOUNTER	This is the value of the counter used for LDO power up. RESET to default.	RW	0x0400
11	FORCEPLLSLOWCLK	Forces the PLL to the slow clk mode	RW	0
10	FORCELDOON	Forces the LDO to be ON.	RW	0
9	FORCEPLLON	Forces the PLL to be ON.	RW	0
8:7	RESERVED	reserved	RW	0x0
6	PLLLOCK	Lock signal from the PLL	R	0
5	USEPLLLOCK	This signal is used to indicate to the Phy, not to do any clock related activity until PLLLOCK = 1.This is not the default option. 0 - do not use PLLLOCK. 1 - use PLLLOCK as a clock gate.	RW	0
4	USE_DATAPOLARITYN_REG	1 - use bit 3 as override for the DATAPOLARITYN signal.	RW	0
3	DATAPOLARITYN	Override value of datapolarityn	RW	0
2	USE_PD_REG	Use bit 1 from this register as PD override when set to 1	RW	0
1	PD	Override value for PD	RW	0
0	RESERVED	reserved	RW	0

Table 23-1216. Register Call Summary for Register USBPHY_PWR_CNTL

High-Speed USB OTG Controller

- USBPHY Register Summary: [0]

Table 23-1217. USBPHY_UTMI_INTERFACE_CNTL_1

Address Offset	0x0000 001C		
Physical Address	0x4A0A D09C	**Instance**	USBPHY
Description	register to override UTMI interface control pins.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
USEUTMIDATAREG	UTMIDATAIN															RESERVED	USEDATABUSREG	DATABUS16OR8	USEOPMODEREG	OPMODE			OVERRIDESUSRESET	SUSPENDM	UTMIRESET	OVERRIDEXCVRSEL	XCVRSEL		USETXVALIDREG	TXVALID	TXVALIDH

Bits	Field Name	Description	Type	Reset
31	USEUTMIDATAREG	Use datain from UTMI interface register	RW	0
30:15	UTMIDATAIN	Override value for the UTMIDATAIN	RW	0x0000
14	RESERVED	reserved	RW	0
13	USEDATABUSREG	When set to 1 use bit 12 from register instead of interface	RW	0
12	DATABUS16OR8	Override value for UTMI signal DATABUS16OR8	RW	0
11	USEOPMODEREG	When set to 1 use bits 10:9 from register instead of interface	RW	0
10:9	OPMODE	Override value for UTMI signal OPMODE[1:0]	RW	0x0
8	OVERRIDESUSRESET	Override the suspend and reset values. Use bits 6 and 7	RW	0
7	SUSPENDM	Override value for UTMI signal SUSPENDM	RW	0

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Bits	Field Name	Description	Type	Reset
6	UTMIRESET	Override value for UTMI signal UTMIRESET	RW	0
5	OVERRIDEXCVRSEL	When set to 1 use bits 4:3 from register instead of interface	RW	0
4:3	XCVRSEL	Override value for UTMI signal XCVRSEL[1:0]	RW	0x0
2	USETXVALIDREG	When set to 1 use bits 1:0 from register instead of interface	RW	0
1	TXVALID	Override value for UTMI signal TXVALID	RW	0
0	TXVALIDH	Override value for UTMI signal TXVALIDH	RW	0

Table 23-1218. Register Call Summary for Register USBPHY_UTMI_INTERFACE_CNTL_1

High-Speed USB OTG Controller

- USBPHY Register Summary: [0]

Table 23-1219. USBPHY_UTMI_INTERFACE_CNTL_2

Address Offset	0x0000 0020		
Physical Address	0x4A0A D0A0	**Instance**	USBPHY
Description	UTMI interface override and observe register 2		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RXRCV	RXDP	RXDM	HOSTDISCONNECT	LINESTATE		RXVALID	RXVALIDH	RXACTIVE	RXERROR	TXREADY	UTMIRESETDONE	USEBITSTUFFREG	TXBITSTUFFENABLE	TXBITSTUFFENABLEH	USETERMCONTROLREG	TERMSEL	DPPULLDOWN	DMPULLDOWN	RESERVED			USEREGSERIALMODE	TXSE0	TXDAT	FSLSSERIALMODE	TXENABLEN	RESERVED				SIG_BYPASS_SUSPENDMPULSE_INCR

Bits	Field Name	Description	Type	Reset
31	RXRCV	Read for UTMI signal. Read value is valid only if VDDLDO is on. Read value is valid only if VDDLDO is on.	R	0
30	RXDP	Read for UTMI signal. Read value is valid only if VDDLDO is on.	R	0
29	RXDM	Read for UTMI signal. Read value is valid only if VDDLDO is on.	R	0
28	HOSTDISCONNECT	Read for UTMI signal. Read value is valid only if VDDLDO is on.	R	0
27:26	LINESTATE	Read for UTMI signal. Read value is valid only if VDDLDO is on.	R	0x0
25	RXVALID	Read for UTMI signal. Read value is valid only if VDDLDO is on.	R	0
24	RXVALIDH	Read for UTMI signal. Read value is valid only if VDDLDO is on.	R	0
23	RXACTIVE	Read for UTMI signal. Read value is valid only if VDDLDO is on.	R	0

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Bits	Field Name	Description	Type	Reset
22	RXERROR	Read for UTMI signal. Read value is valid only if VDDLDO is on.	R	0
21	TXREADY	Read for UTMI signal. Read value is valid only if VDDLDO is on.	R	0
20	UTMIRESETDONE	Read for UTMIRESETDONE signal	R	0
19	USEBITSTUFFREG	When set to 1 use bits 18-17 from register instead of interface	RW	0
18	TXBITSTUFFENABLE	Override value for signal TXBITSTUFFENABLE	RW	0
17	TXBITSTUFFENABLEH	Override value for pin TXBITSTUFFENABLE	RW	0
16	USETERMCONTROLREG	When set to 1, bits 15:13 from register are used instead of interface	RW	0
15	TERMSEL	Override value for signal TERMSEL	RW	0
14	DPPULLDOWN	Override value for signal DPPULLDOWN	RW	0
13	DMPULLDOWN	Override value for signal DMPULLDOWN	RW	0
12:10	RESERVED	reserved	RW	0x0
9	USEREGSERIALMODE	When set to 1 use bits 8:5 from register instead of interface	RW	0
8	TXSE0	Override value for signal TXSE0	RW	0
7	TXDAT	Override value for signal TXDAT	RW	0
6	FSLSSERIALMODE	Override value for signal FSLSSERIALMODE	RW	0
5	TXENABLEN	Override value for signal TXENABLEN	RW	0
4:1	RESERVED	reserved	RW	0x0
0	SIG_BYPASS_SUSPENDMPULSE_INCR	If the suspend signal is asserted for a short time, it is pulse-extended so that the sampling logic samples it reliably. 0: Pulse extension active 1: Bypass pulse extension	RW	0

Table 23-1220. Register Call Summary for Register USBPHY_UTMI_INTERFACE_CNTL_2

High-Speed USB OTG Controller

- USBPHY Register Summary: [0]

Table 23-1221. USBPHY_BIST

Address Offset	0x0000 0024		
Physical Address	0x4A0A D0A4	**Instance**	USBPHY
Description	COntains bits related to the built in self test of the phy		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BIST_START	REDUCED_SWING	BIST_CRC_CALC_EN	BIST_PKT_LENGTH									LOOPBACK_EN	BIST_OP_PHASE_SEL			SWEEP_EN	SWEEP_MODE			BIST_PASS	BIST_BUSY	RESERVED		OP_CODE		RX_TEST_MODE	RESERVED	INTER_PKT_DELAY_TEST	HS_ALL_ONES_TEST	USE_BIST_TX_PHASES	

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Bits	Field Name	Description	Type	Reset
31	BIST_START	When set to 1 the BIST mode is started.	RW	0
30	REDUCED_SWING	When 1 the TX swing is reduced in BIST mode	RW	0
29	BIST_CRC_CALC_EN	Enables CRC calculation during BIST when set to 1	RW	0
28:20	BIST_PKT_LENGTH	Address for which BIST to select	RW	0x000
19	LOOPBACK_EN	Enables the loopback mode	RW	0
18:16	BIST_OP_PHASE_SEL	Selects which phase to use for data transmission during BIST	RW	0x0
15	SWEEP_EN	Enables freq sweep on CDR	RW	0
14:12	SWEEP_MODE	Selects the freq sweep mode.	RW	0x0
11	BIST_PASS	Indicates that the BIST has passed. Read value is valid only if VDDLDO is on.	R	0
10	BIST_BUSY	Indicates that BIST is running. Read value is valid only if VDDLDO is on.	R	0
9:7	RESERVED	reserved	RW	0x0
6:5	OP_CODE		RW	0x0
4	RX_TEST_MODE		RW	0
3	RESERVED	reserved	RW	0
2	INTER_PKT_DELAY_TEST		RW	0
1	HS_ALL_ONES_TEST		RW	0
0	USE_BIST_TX_PHASES	When set to 1 bits 18:16 are activated for choosing the transmitting phase.	RW	0

Table 23-1222. Register Call Summary for Register USBPHY_BIST

High-Speed USB OTG Controller

- USBPHY Register Summary: [0]

Table 23-1223. USBPHY_BIST_CRC

Address Offset	0x0000 0028		
Physical Address	0x4A0A D0A8	**Instance**	USBPHY
Description	CRC code for BIST test		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits	Field Name	Description	Type	Reset
31:0	BIST_CRC	The CRC value from the BIST.	RW	0x0000 0000

Table 23-1224. Register Call Summary for Register USBPHY_BIST_CRC

High-Speed USB OTG Controller

- USBPHY Register Summary: [0]

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Table 23-1225. USBPHY_CDR_BIST2

Address Offset	0x0000 002C		
Physical Address	0x4A0A D0AC	**Instance**	USBPHY
Description	clock data recovery register and BIST register 2		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CDR_EXE_EN	CDR_EXE_MODE			NUM_DECISIONS			CDR_CHOSEN_PHASE			FORCE_CDR_PHASE			DISABLE_CDR_FREQ_TRACK	CDR_CONFIGURE					FORCE_CDR_PHASE_EN	BIST_START_ADDR						BIST_END_ADDR					

Bits	Field Name	Description	Type	Reset
31	CDR_EXE_EN	CDR debug bits	RW	0
30:28	CDR_EXE_MODE	CDR debug bits	RW	0x0
27:25	NUM_DECISIONS	CDR debug bits	RW	0x0
24:12	RESERVED	reserved	R	0x000
11:6	BIST_START_ADDR		RW	0x00
5:0	BIST_END_ADDR		RW	0x00

Table 23-1226. Register Call Summary for Register USBPHY_CDR_BIST2

High-Speed USB OTG Controller

- USBPHY Register Summary: [0]

Table 23-1227. USBPHY_GPIO

Address Offset	0x0000 0030		
Physical Address	0x4A0A D0B0	**Instance**	USBPHY
Description	GPIO mode configurations and reads		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
USEGPIOMODEREG	GPIOMODE	DPGPIOGZ	DMGPIOGZ	DPGPIOA	DMGPIOA	DPGPIOY	DMGPIOY	1P8VCONFIG	GPIOCONFIG				DMGPIOPIPD	DPGPIOPIPD	RESERVED																	

Bits	Field Name	Description	Type	Reset
31	USEGPIOMODEREG	When set to 1 use bits 31:24 from this register instead of primary inputs	RW	0
30	GPIOMODE	Overrides the corresponding primary input	RW	0
29	DPGPIOGZ	Overrides the corresponding primary input	RW	0

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Bits	Field Name	Description	Type	Reset
28	DMGPIOGZ	Overrides the corresponding primary input	RW	0
27	DPGPIOA	Overrides the corresponding primary input	RW	0
26	DMGPIOA	Overrides the corresponding primary input	RW	0
25	DPGPIOY	The GPIO Y output is stored here	R	0
24	DMGPIOY	The GPIO Y output is stored here	R	0
23	GPIO1P8VCONFIG	Overrides the corresponding primary input	RW	0
22:20	GPIOCONFIG	Used for configuring the GPIOs.	RW	0x0
19	DMGPIOPIPD	GPIO mode DM pull-down enabled. Overrides the corresponding primary input	RW	0
18	DPGPIOPIPD	GPIO mode DP pull-down enabled. Overrides the corresponding primary input.	RW	0
17:0	RESERVED	reserved	RW	0x00000

Table 23-1228. Register Call Summary for Register USBPHY_GPIO

High-Speed USB OTG Controller

- USBPHY Register Summary: [0]

Table 23-1229. USBPHY_DLLHS

Address Offset	0x0000 0034		
Physical Address	0x4A0A D0B4	**Instance**	USBPHY
Description	Bits for control and debug of the DLL inside the USBPHY		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			DLLHS_LOCK	DLLHS_GENERATED_CODE						DLL_SEL_CODE_PHS	DLL_LOCKCHK		DLL_SEL_COD			DLL_PHS0_8	DLL_FORCED_CODE							FORCE_DLL_CODE	DLL_RATE		DLL_FILT		DLL_CDR_MODE	DLL_IDLE	DLL_FREEZE	RESERVED

Bits	Field Name	Description	Type	Reset
31:29	RESERVED	reserved	RW	0x0
28	DLLHS_LOCK	Read the AFE output by this name	R	0
27:22	DLLHS_GENERATED_CODE	Read the AFE output by this name.Read value is valid only if VDDLDO is on.	R	0x00
21	DLL_SEL_CODE_PHS	Connect to DLLHS_TEST_LDO[0] on AFE interface.	RW	0
20:19	DLL_LOCKCHK	Connect to DLLHS_TEST_LDO[2:1] on AFE interface.	RW	0x0
18:16	DLL_SEL_COD	Connect to DLLHS_TEST_LDO[5:3] on AFE interface.	RW	0x0
15	DLL_PHS0_8	Connect to DLLHS_TEST_LDO[6] on AFE interface.	RW	1
14:9	DLL_FORCED_CODE	Connect to the pin of this name on AFE interface.	RW	0x00
8	FORCE_DLL_CODE	Connect to DLLHS_TEST_LDO[11] on AFE interface.	RW	0
7:6	DLL_RATE	Connect to DLLHS_TEST_LDO[8:7] on AFE interface.	RW	0x0
5:4	DLL_FILT	Connect to DLLHS_TEST_LDO[10:9] on AFE interface.	RW	0x0
3	DLL_CDR_MODE	Connect to the pin of this name on AFE interface.	RW	0
2	DLL_IDLE	Connect to DLLHS_TEST_LDO[12] on AFE interface.	RW	0

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Bits	Field Name	Description	Type	Reset
1	DLL_FREEZE	Connect to DLLHS_TEST_LDO[13] on AFE interface.	RW	0
0	RESERVED	reserved	RW	0

Table 23-1230. Register Call Summary for Register USBPHY_DLLHS

High-Speed USB OTG Controller

- USBPHY Register Summary: [0]

Table 23-1231. USBPHY_USB2PHYCM_TRIM

Address Offset	0x0000 0038		
Physical Address	0x4A0A D0B8	**Instance**	USBPHY
Description	Contains trim bit overrides for the USBPHYCM		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
USEBGTRIM								BGTRIM								USE_SW_TRIM								USE_NWELLTRIM_REG				NWELLTRIM_CODE				RESERVED			

Bits	Field Name	Description	Type	Reset
31	USEBGTRIM	When set to 1 bits 30:16 are used as the trim value for the USBPHYCM bandgap	RW	0
30:16	BGTRIM	Override value for the BGTRIM value	RW	0x0000
15	USE_SW_TRIM	Use bits 14:8 to override the switch cap trim value.	RW	0
14:8	SWTRIM	Override value for the switch cap trim value.	RW	0x00
7	USE_NWELLTRIM_REG	Override NWELL resistor trim using NWELLTRIM_CODE	RW	0
6:4	NWELLTRIM_CODE	NWELL resistor trim code.	RW	0x0
3:0	RESERVED	reserved	RW	0x0

Table 23-1232. Register Call Summary for Register USBPHY_USB2PHYCM_TRIM

High-Speed USB OTG Controller

- USBPHY Register Summary: [0]

Table 23-1233. USBPHY_USB2PHYCM_CONFIG

Address Offset	0x0000 003C		
Physical Address	0x4A0A D0BC	**Instance**	USBPHY
Description	Configuration and status register for the USBPHYCM and LDO		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONFIGURECM								CMSTATUS								LDOCONFIG															LDOSTATUS

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Bits	Field Name	Description	Type	Reset
31:24	CONFIGURECM	Connects to the CONFIGURECM pins.	RW	0x00
23:18	CMSTATUS	Reads the CMSTATUS bits.	R	0x00
17:2	LDOCONFIG	The LDOCONFIG bit settings.	RW	0x0000
1:0	LDOSTATUS	Reads the LDOSTATUS bits.	R	0x0

Table 23-1234. Register Call Summary for Register USBPHY_USB2PHYCM_CONFIG

High-Speed USB OTG Controller

- USBPHY Register Summary: [0]

Table 23-1235. USBPHY_USBOTG

Address Offset	0x0000 0040		
Physical Address	0x4A0A D0C0	**Instance**	USBPHY
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TESTOTGCONFIG																TESTOTGSTATUS								RESERVED							

Bits	Field Name	Description	Type	Reset
31:16	TESTOTGCONFIG	Used to control the OTG module if used.	RW	0x0000
15:6	TESTOTGSTATUS	The OTG status bits (if OTG macro is used)	R	0x000
5:0	RESERVED	reserved	R	0x00

Table 23-1236. Register Call Summary for Register USBPHY_USBOTG

High-Speed USB OTG Controller

- USBPHY Register Summary: [0]

Table 23-1237. USBPHY_AD_INTERFACE_REG1

Address Offset	0x0000 0044		
Physical Address	0x4A0A D0C4	**Instance**	USBPHY
Description	All bits (unless defined) are bypass bits for internal analog to digital interface pins with the same name. All the bits of this register, except the over-ride bits return a '0' on read, if VDDLDO is off.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
USE_AD_DATA_REG	HS_TX_DATA	FS_TX_DATA	TEST_PRE_EN_CNTRL	SQ_PRE_EN	HS_TX_PRE_EN	HS_RX_PRE_EN	TEST_EN_CNTRL	HS_TX_EN	FS_RX_EN	RESERVED	SQ_EN	HS_RX_EN	TEST_HS_MODE	HS_HV_SW	HS_CHIRP	TEST_FS_MODE	FSTX_GZ	FSTX_PRE_EN	RESERVED	TEST_SQ_CAL_CONTROL	SQ_CAL_EN3	SQ_CAL_EN1	SQ_CAL_EN2	TEST_RTERM_CAL_CONTROL	RTERM_CAL_EN	DLL_RX_DATA	DISCON_DETECT	USE_LSHOST_REG	LSHOSTMODE	LSFS_RX_DATA	SQUELCH

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Bits	Field Name	Description	Type	Reset
31	USE_AD_DATA_REG	Override for bits 30:29	RW	0
30	HS_TX_DATA		RW	0
29	FS_TX_DATA		RW	0
28	TEST_PRE_EN_CNTRL	Override for bits 27:25	RW	0
27	SQ_PRE_EN		RW	0
26	HS_TX_PRE_EN		RW	0
25	HS_RX_PRE_EN		RW	0
24	TEST_EN_CNTRL	Override for bits 23:19	RW	0
23	HS_TX_EN		RW	0
22	FS_RX_EN		RW	0
21	RESERVED		RW	0
20	SQ_EN		RW	0
19	HS_RX_EN		RW	0
18	TEST_HS_MODE	Override for bits 17:16	RW	0
17	HS_HV_SW		RW	0
16	HS_CHIRP		RW	0
15	TEST_FS_MODE	Override for bits 14:12	RW	0
14	FSTX_GZ		RW	0
13	FSTX_PRE_EN		RW	0
12	RESERVED		RW	0
11	TEST_SQ_CAL_CONTROL	Override for bits 10:8	RW	0
10	SQ_CAL_EN3		RW	0
9	SQ_CAL_EN1		RW	0
8	SQ_CAL_EN2		RW	0
7	TEST_RTERM_CAL_CONTROL	Override for bits 6	RW	0
6	RTERM_CAL_EN		RW	0
5	DLL_RX_DATA		R	0
4	DISCON_DETECT		R	0
3	USE_LSHOST_REG	Use bit 2 for this reg	RW	0
2	LSHOSTMODE		RW	0
1	LSFS_RX_DATA		R	0
0	SQUELCH		R	0

Table 23-1238. Register Call Summary for Register USBPHY_AD_INTERFACE_REG1

High-Speed USB OTG Controller

- USBPHY Register Summary: [0]

Table 23-1239. USBPHY_AD_INTERFACE_REG2

Address Offset	0x0000 0048		
Physical Address	0x4A0A D0C8	**Instance**	USBPHY
Description	All bits (unless defined) are bypass bits for internal analog to digital interface pins with the same name. All the bits of this register, except the override bits return a '0' on read, if VDDLDO is off.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
USE_SUSP_DRV_REG	SUS_DRV_DP_DATA	SUS_DRV_DP_EN	SUS_DRV_DM_DATA	SUS_DRV_DM_EN	USE_DISCON_REG	DISCON_EN	DISCON_PRE_EN	RESERVED	SPARE_OUT_CORE					SERX_DP_CORE	SERX_DM_CORE	USE_HSRX_CAL_EN_REG	HSRX_CAL_EN	USE_RPU_RPD_REG	RPU_DP_SW1_EN_CORE	RPU_DP_SW2_EN_CORE	RPU_DM_SW1_EN_CORE	RPU_DM_SW2_EN_CORE	DP_PULLDOWN_EN_CORE	DM_PULLDOWN_EN_CORE	DP_DM_5V_SHORT	SPARE_IN_CORE					PORZ

Bits	Field Name	Description	Type	Reset
31	USE_SUSP_DRV_REG	Use bits 30:27 from this register as overrides	RW	0
30	SUS_DRV_DP_DATA		RW	0
29	SUS_DRV_DP_EN		RW	0
28	SUS_DRV_DM_DATA		RW	0
27	SUS_DRV_DM_EN		RW	0
26	USE_DISCON_REG	Use bits 25:24 from this register as override	RW	0
25	DISCON_EN		RW	0
24	DISCON_PRE_EN		RW	0
23	RESERVED	reserved	RW	0
22:18	SPARE_OUT_CORE		R	0x00
17	SERX_DP_CORE		R	0
16	SERX_DM_CORE		R	0
15	USE_HSRX_CAL_EN_REG	Use bit 14 from this register as override	RW	0
14	HSRX_CAL_EN		RW	0
13	USE_RPU_RPD_REG	Use override from bits 12:7	RW	0
12	RPU_DP_SW1_EN_CORE		RW	0
11	RPU_DP_SW2_EN_CORE		RW	0
10	RPU_DM_SW1_EN_CORE		RW	0
9	RPU_DM_SW2_EN_CORE		RW	0
8	DP_PULLDOWN_EN_CORE		RW	0
7	DM_PULLDOWN_EN_CORE		RW	0
6	DP_DM_5V_SHORT		R	0
5:1	SPARE_IN_CORE		RW	0x00
0	PORZ	Read only bit - the PORZ generated from the digital registered on the A-D interface.	R	0

Table 23-1240. Register Call Summary for Register USBPHY_AD_INTERFACE_REG2

High-Speed USB OTG Controller

- USBPHY Register Summary: [0]

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Table 23-1241. USBPHY_AD_INTERFACE_REG3

Address Offset	0x0000 004C		
Physical Address	0x4A0A D0CC	**Instance**	USBPHY
Description	All bits (unless defined) are bypass bits for internal analog to digital interface pins with the same name. All the bits of this register, except the override bits return a '0' on read, if VDDLDO is off.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
USE_HSOS_DATA_REG	HSOS_DATA							USE_FS_REG3	FSTX_MODE	FSTX_SE0	USE_HS_TERM_RES_REG	HS_TERM_RES	SPARE_IN_LDO			SPARE_OUT_LDO								USE_FARCORE_REG	FARCORE						

Bits	Field Name	Description	Type	Reset
31	USE_HSOS_DATA_REG	Use bits 30:23 in this register as bypass bits	RW	0
30:23	HSOS_DATA		RW	0x00
22	USE_FS_REG3	Use bits 21:20 as bypass bits	RW	0
21	FSTX_MODE		RW	0
20	FSTX_SE0		RW	0
19	USE_HS_TERM_RES_REG	Use bit 18 as override bit	RW	0
18	HS_TERM_RES		RW	0
17:10	SPARE_IN_LDO		RW	0x00
9:2	SPARE_OUT_LDO		R	0x00
1	USE_FARCORE_REG	Use bit 0 from this register as bypass	RW	0
0	FARCORE		RW	0

Table 23-1242. Register Call Summary for Register USBPHY_AD_INTERFACE_REG3

High-Speed USB OTG Controller

- USBPHY Register Summary: [0]

Table 23-1243. USBPHY_ANA_CONFIG1

Address Offset	0x0000 0050		
Physical Address	0x4A0A D0D0	**Instance**	USBPHY
Description	Used to configure and debug the analog blocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SQ_CTRL_REG																FS_SLEW		HS_PRE_EMP_CNTRL		HSFSTX_TEST				PROTECT_TEST							

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Bits	Field Name	Description	Type	Reset
31:17	SQ_CTRL_REG		RW	0x0000
16:14	FS_SLEW		RW	0x0
13:12	HS_PRE_EMP_CNTRL		RW	0x0
11:5	HSFSTX_TEST		RW	0x00
4:0	PROTECT_TEST		RW	0x00

Table 23-1244. Register Call Summary for Register USBPHY_ANA_CONFIG1

High-Speed USB OTG Controller

- USBPHY Register Summary: [0]

Table 23-1245. USBPHY_ANA_CONFIG2

Address Offset	0x0000 0054		
Physical Address	0x4A0A D0D4	**Instance**	USBPHY
Description	Used to configure and debug the analog blocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTERM_CAL_TEST								REF_GEN_TEST							FSRX_TEST				RTERM_TEST		DISCON_TEST			HSRX_TEST				SERX_TEST			SERX_HYST_CNTRL		SQ_LPMODEZ

Bits	Field Name	Description	Type	Reset
31:27	RTERM_CAL_TEST		RW	0x00
26:20	REF_GEN_TEST		RW	0x00
19:17	FSRX_TEST		RW	0x00
16:15	RTERM_TEST		RW	0x0
14:11	DISCON_TEST		RW	0x0
10:6	HSRX_TEST		RW	0x00
5:3	SERX_TEST		RW	0x0
2:1	SERX_HYST_CNTRL		RW	0x0
0	SQ_LPMODEZ		RW	0

Table 23-1246. Register Call Summary for Register USBPHY_ANA_CONFIG2

High-Speed USB OTG Controller

- USBPHY Register Summary: [0]

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23.13 Full-Speed USB Host Controller

This section describes the full-speed universal serial bus (FSUSB) host controller for the device

23.13.1 FSUSB Host Controller Overview

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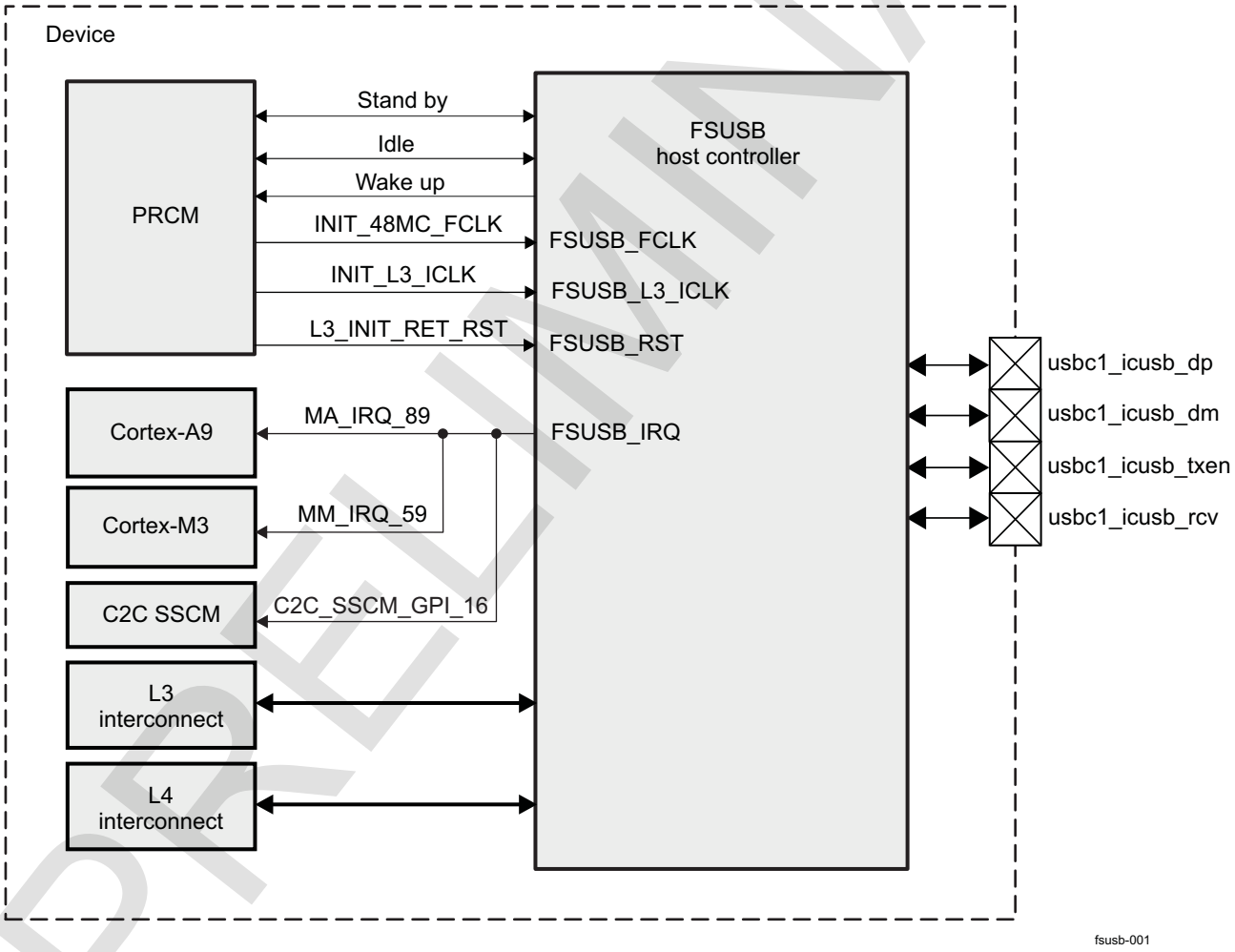
This module is a full-speed universal serial bus (FSUSB) host controller which complies with the USB 2.0 standard for full-speed functions. The FSUSB host controller supports a single universal serial bus (USB) host port with a USB interchip to interface with a multimedia subscriber-identity module (SIM) card, using 2-/4-pin bidirectional mode (host mode.

The FSUSB host controller has level 3 (L3) and level 4 (L4) interfaces with an independent functional clock.

Figure 23-260. FSUSB Host Controller Overview



23.13.1.1 Main Features

The main features of the FSUSB host controller include:

- USB host
  - Compatible with OHCI Rev 1.0

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  - USB 2.0 low-speed (1.5 Mbps) and full-speed (12 Mbps) operations
  - Single port
- USB port signal pins interface:
  - Only supports the 2-/4-pin (bidirectional) mode
- Slave interface (L4) supporting:
  - 32-bit data bus width
  - 32-bit access
  - 32-bit address bus width
  - Wireless network portability (WNP)
  - Burst is not supported
- Master interface (L3) supporting:
  - 32-bit data bus width
  - 8-/32-bit access
  - 32-bit address bus width
  - Write nonposted (WRPN) interconnect transaction

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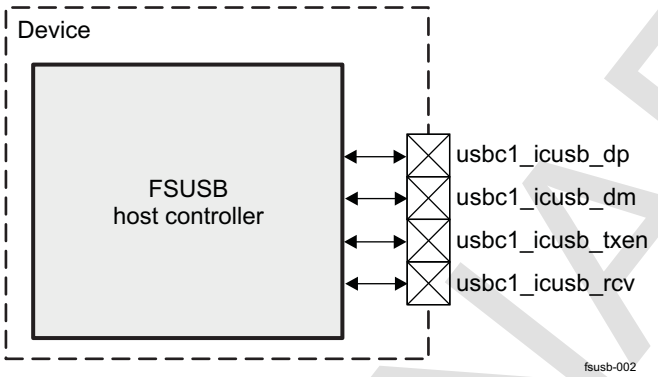
23.13.2 FSUSB Host Controller Environment

This section describes the FSUSB host controller application fields from an environment point of view (external connections). It discusses FSUSB host controller connectivity options, lists all possible interfaces, and describes the protocol and data format used in each case.

Figure 23-261 shows the output pins of the FSUSB host controller.

Figure 23-261. Overview of FSUSB Host Controller Environment



23.13.2.1 FSUSB Host Controller Functional Interfaces Description

Table 23-1247 and Table 23-1248 list the input/output (I/O) signals.

Table 23-1247. Pin List for FS USB-Host (USB-Interchip Mode)

Signal Name	I/O (1)	Description	Reset Value
usbc1_icusb_dp	I/O	Interchip FSUSB host controller D plus	Unknown
usbc1_icusb_dm	I/O	Interchip FSUSB host controller D minus	Unknown

(1) I = Input, O = Output

Table 23-1248. 4-Pin Mode Delivered on Pin (for External Transceiver Connection)

Signal Name	I/O (1)	Description	Reset Value
usbc1_icusb_dp	I/O	FSUSB host controller D plus	Unknown
usbc1_icusb_dm	I/O	FSUSB host controller D minus	Unknown
usbc1_icusb_txen	O	FSUSB host controller transmit enable	Unknown
usbc1_icusb_rcv	I	FSUSB host controller receive	Unknown

(1) I = Input, O = Output

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23.13.3 FSUSB Host Controller Integration

This section describes module integration in the device, including information about clocks, resets, and hardware requests.

Figure 23-262 shows the integration of the FSUSB host controller in the device.

Figure 23-262. FSUSB Host Controller Integration

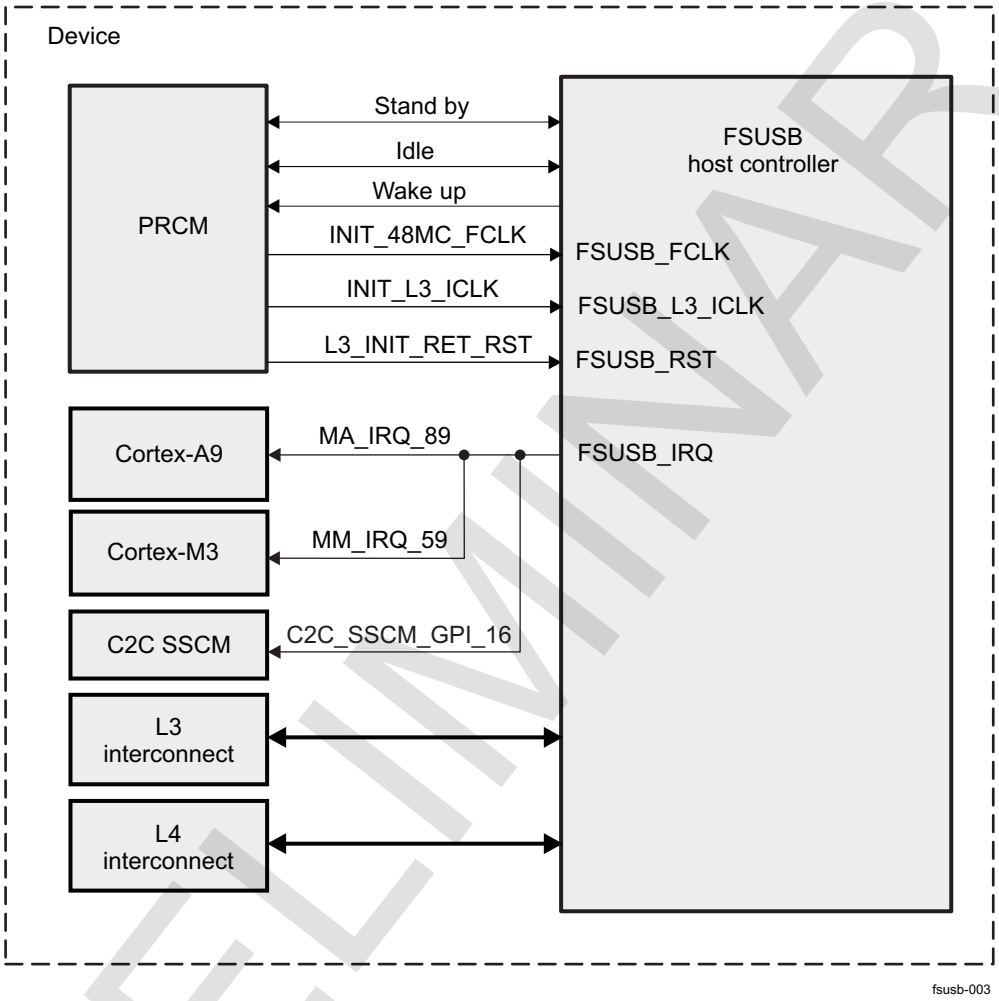

Table 23-1249 through Table 23-1251 summarize the integration of the module in the device.

Table 23-1249. Integration Attributes

Module Instance	Attributes	
	Power Domain	Interconnect
FSUSB host controller	PD_L3_INIT	L3 L4_CFG

Table 23-1250. Clocks and Resets

Clocks				
Module Instance	Destination Signal Name	Source Signal Name	Source	Description
FSUSB host controller	FSUSB_FCLK	INIT_48MC_FCLK	PRCM	Functional clock (see Section 3.6.9, *CD_L3_INIT Clock Domain* in Chapter 3, *Power, Reset, and Clock Management*).

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Table 23-1250. Clocks and Resets (continued)

Clocks				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
	FSUSB_L3_ICLK	INIT_L3_ICLK	PRCM	L3 interconnect clock for the L3 master port interface (see , *CD_L3_INIT Clock Domain* in Section 3.6.9, *Power, Reset, and Clock Management*)
	FSUSB_L4_ICLK	INIT_L4_ICLK	PRCM	L4 interconnect-enable signal for the slave interface on L4 (seeSection 3.6.3.2, *CM Clock Source* in Chapter 3, *Power, Reset, and Clock Management*)
Resets				
FSUSB host controller	FSUSB_RST	L3_INIT_RET_RST	PRCM	This signal resets the FSUSB host controller module.

Table 23-1251. Hardware Requests

Interrupt Requests					
Module Instance		**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
FSUSB controller	host	FSUSB_IRQ	MA_IRQ_89	Cortex-A9 INTC	Destination is Cortex-A9 interrupt controller (INTC)
		FSUSB_IRQ	MM_IRQ_59	Cortex-M3 INTC	Destination is Cortex-M3 INTC
		FSUSB_IRQ	C2C_SSCM_GPI_16	C2C INTC	Destination is C2C INTC

NOTE: For interrupt source information, see Section 23.13.5.1.2, *Interrupt Requests*.

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23.13.4 FSUSB Host Controller Functional Description

23.13.4.1 Resets

The different software reset functions of the FSUSB host controller are controlled by the following register bits:

- HCOCPSYS[1] SOFT_RESET bit: Writing 0x1 to this bit resets the entire module, except IDLE, STANDBY, and DISCONNECT logic. The bit value of 0x1 remains until the reset completes. When the software reset completes, the SOFT_RESET bit is automatically set to 0x0.
- HCCOMMANDSTATUS[0] HCR bit: Writing 0x1 resets most of the open host controller interface (OHCI) registers of the FSUSB host controller. It is useful for error handling only. OHCI register accesses must not be attempted until a read of this register returns 0x0.

23.13.4.2 Power Management

23.13.4.2.1 Features

The power management module has the following features:

- The FSUSB host controller has one instance of IDLE and standby interface.
- There are separate disconnect interfaces for master and slave ports.
- The PRCM module uses IDLE protocol to put the FSUSB host controller asynchronous into idle mode.
- The FSUSB host controller uses standby protocol for USB suspend event.
- Clock gating is done externally for IDLE and standby protocol.
- The IDLE and STANDBY interfaces are synchronous to the PRCM clock.

23.13.4.2.2 IDLE Protocol

The IDLE protocol has the following features:

- There is one IDLE protocol for the FSUSB host controller.
- The HCOCPSYS[3:2] IDLE_MODE bit field controls the way USBFSHOST handles the IDLE protocol.
- The FSUSB host controller WakeupEnable mode is enabled by setting the HCOCPSYS[3:2] IDLE_MODE bit field to 0x11.
- Wakeup is generated asynchronously in the FSUSB host controller. To detect the USB remote wakeup, the FSUSB host controller should always be powered up (that is, the clocks can be off, but the power is needed for a wake-up detection to work).
- The FSUSB host controller interface asserts wakeup from suspend when the wake-up conditions occur (such as remote signaling on port, device connect/disconnect) and the FSUSB host controller is in idle mode. The FSUSB host controller interface deasserts the wake-up signal when the PRCM module has serviced the event (usually at completion of a resume sequence on the USB) and IDLE request is 0.
- The FSUSB host controller interface acknowledges and goes into IDLE only if the host controller is in suspend mode, or if force-idle mode is enabled.

Table 23-1252 lists the FSUSB host controller idle mode settings.

Table 23-1252. FSUSB Host Controller Idle Mode Settings

SIDLEMODE Value	Selected Mode	Description
0x0	Force-idle	The high-speed USB host controller unconditionally acknowledges the IDLE request from the PRCM module, regardless of its internal operations.
0x1	Not supported (no-idle)	
0x2	Smart-idle	The high-speed USB host controller acknowledges the IDLE request, basing its decision on its internal activity. Namely, the acknowledged signal is asserted only when all pending transactions, IRQs, or DMA requests are treated.
0x3	Smart-idle wakeup	The high-speed USB host controller enters smart mode with asynchronous wakeup enabled.

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23.13.4.2.3 Standby Protocol

The Standby protocol is associated with FSUSB host controller suspend. Standby assertion is linked with Suspend, and Wakeup assertion is linked with remote wakeup. When the application wants to resume the USB, the power manger must initiate the wakeup using the Standby protocol.

- There is one Standby protocol for the FSUSB host controller.
- The HCOCPSYS[5:4] STANDBY_MODE bit field controls the way USBFSHOST handles the Standby protocol.
- The FSUSB host controller wakes up with standby, and stays in standby until the host core becomes functional.

Table 23-1253 lists the STANBY_MODE settings for the FSUSB host controller.

Table 23-1253. FSUSB Host Controller STANDBY_MODE Settings

MIDLEMODE Value	Selected Mode	Description
0x0	Force-standby	The high-speed USB host controller enters standby mode unconditionally (Mstandby is asserted unconditionally).
0x1	Not supported (no-standby)	
0x2	Smart-standby	The high-speed USB host controller is ready to enter standby mode when there is no more activity on the USB master interface of the interconnect.
0x3	Smart-standby wakeup	The high-speed USB host controller enters smart mode with asynchronous wakeup enabled.

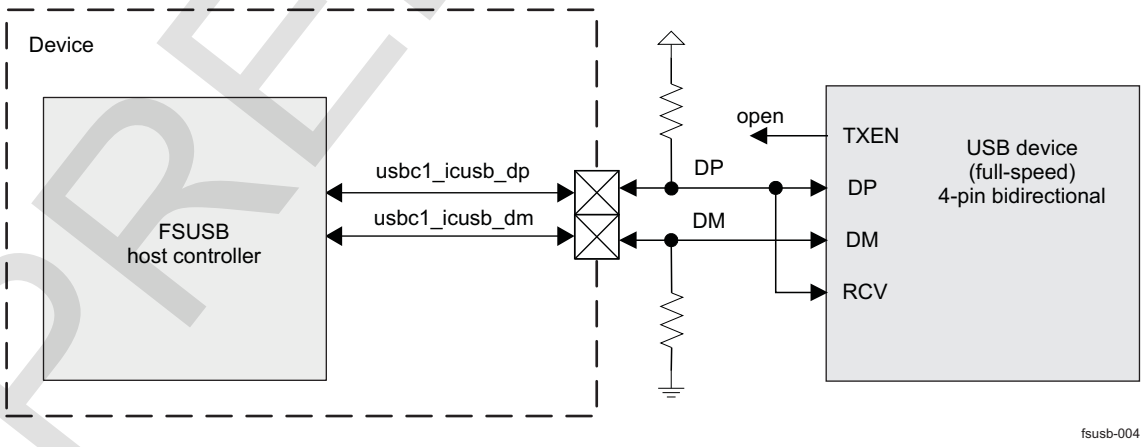
23.13.4.3 FSUSB Host Controller Bidirectional Interface Modes

Bidirectional SIM interface modes are implemented using existing bidirectional modes. Their goal is to reduce pin count with respect to 6-/5-pin modes.

Pullup/pulldown resistors on the bidirectional lines are compulsory, because the lines are not constantly driven from one side or the other of the interface. In this case, the pullup on one of the two lines triggers the connect signal from the device to the host. The pullup can be controlled (by the USB device side) or hardwired. In the first case, the USB host sees only the external device if the pullup is active; in the second case, the USB host sees the device as soon as software enables the port in question.

The device supports the 2-pin bidirectional SIM Interface mode with DP/DM encoding. Figure 23-263 shows a USB port using DP/DM encoding.

Figure 23-263. 2-Pin Bidirectional Interface Using DP/DM Encoding With a Standard 4-Pin Bidirectional USB Device



A specific 2-pin USB device can also be implemented with just the two bidirectional pins. Figure 23-264 shows an example in DP/DM encoding with built-in pullup/pulldown resistors.

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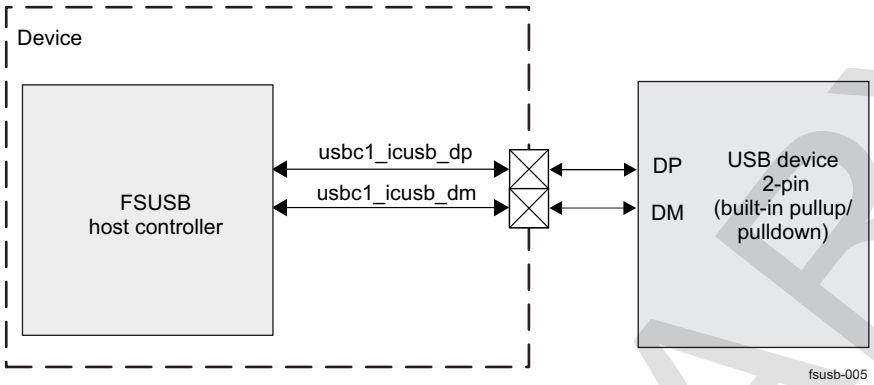
Figure 23-264. 2-Pin Bidirectional Interface Using DP/DM Encoding With a Specific 2-Pin Bidirectional USB Device



23.13.5 FSUSB Host Controller Basic Programming Model

This section describes the low-level hardware programming sequences for the configuration and use of the FSUSB host controller.

23.13.5.1 Global Initialization

23.13.5.1.1 Surrounding Modules Global Initialization

This section identifies the requirements for initializing the surrounding modules when the FSUSB host controller is to be used for the first time after a device reset. This initialization of surrounding modules is based on the integration of the FSUSB host controller.

Table 23-1254 describes the global initialization of the surrounding modules.

Table 23-1254. Global Initialization of Surrounding Modules

Surrounding Modules	Comments
PRCM	All clocks must be enabled (see Table 23-1250). See Section 3.6.3.2, *CM Clock Source* in Chapter 3, *Power, Reset and Clock Management*.
Cortex-A9 MPU INTC or Cortex-M3 MPU INTC	The Cortex-A9 MPU or Cortex-M3 MPU INTC must be configured to enable the interrupt request generation to the Cortex-A9 MPU or Cortex-M3 MPU subsystem when interrupt requests are generated by the FSUSB host controller. See the respective functional description in Chapter 17, *Interrupt Controllers,* for the MPUs.
Interconnect (L3 and L4)	For more information, see Section 13.2, *L3 Interconnect*, and Section 13.3, *L4 Interconnect*.

NOTE: This module requires an active functional clock for L4 access to function.

23.13.5.1.2 FSUSB Host Controller Global Initialization

This procedure initializes the FSUSB host controller after a power-on or software reset (see Table 23-1255).

Table 23-1255. High-Speed Multiport USB Host Subsystem Global Initialization

Step	Register/Bit Field/Programming Model	Value
Perform a software reset on the FSUSB host controller module, except for IDLE, STANDBY, and DISCONNECT logics.	HCOCPSYS[1] SOFT_RESET	0x1

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Table 23-1255. High-Speed Multiport USB Host Subsystem Global Initialization (continued)

Step	Register/Bit Field/Programming Model	Value
Wait until reset is finished.	HCOCPSYS[1] SOFT_RESET	0x0
Enable IRQ event for the FSUSB host controller.	HCINTERRUPTENABLE[31] MIE	0x1
Enable IRQ event for each function of the FSUSB host controller.	HCINTERRUPTENABLE[6:0] xxx	0x1

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23.13.6 USBFSHOST Register Manual

23.13.6.1 USBFSHOST Instance Summary

Table 23-1256. USBFSHOST Instance Summary

Module Name	Base Address	Size
USBFSHOST	0x4A0A 9000	4KB

23.13.6.2 USBFSHOST Registers

23.13.6.2.1 USBFSHOST Register Summary

Table 23-1257. USBFSHOST Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	Physical Address
HCREVISION	R	32	0x0000 0000	0x4A0A 9000
HCCONTROL	RW	32	0x0000 0004	0x4A0A 9004
HCCOMMANDSTATUS	RW	32	0x0000 0008	0x4A0A 9008
HCINTERRUPTSTATUS	RW	32	0x0000 000C	0x4A0A 900C
HCINTERRUPTENABLE	RW	32	0x0000 0010	0x4A0A 9010
HCINTERRUPTDISABLE	RW	32	0x0000 0014	0x4A0A 9014
HCHCCA	RW	32	0x0000 0018	0x4A0A 9018
HCPERIODCURRENTED	R	32	0x0000 001C	0x4A0A 901C
HCCONTROLHEADED	RW	32	0x0000 0020	0x4A0A 9020
HCCONTROLCURRENTED	RW	32	0x0000 0024	0x4A0A 9024
HCBULKHEADED	RW	32	0x0000 0028	0x4A0A 9028
HCBULKCURRENTED	RW	32	0x0000 002C	0x4A0A 902C
HCDONEHEAD	R	32	0x0000 0030	0x4A0A 9030
HCFMINTERVAL	RW	32	0x0000 0034	0x4A0A 9034
HCFMREMAINING	R	32	0x0000 0038	0x4A0A 9038
HCFMNUMBER	R	32	0x0000 003C	0x4A0A 903C
HCPERIODICSTART	RW	32	0x0000 0040	0x4A0A 9040
HCLSTHRESHOLD	RW	32	0x0000 0044	0x4A0A 9044
HCRHDESCRIPTORA	RW	32	0x0000 0048	0x4A0A 9048
HCRHDESCRIPTORB	RW	32	0x0000 004C	0x4A0A 904C
HCRHSTATUS	RW	32	0x0000 0050	0x4A0A 9050
HCRHPORTSTATUS	RW	32	0x0000 0054	0x4A0A 9054
HCOCPREV	R	32	0x0000 0200	0x4A0A 9200
HCOCPHWI	R	32	0x0000 0204	0x4A0A 9204
HCOCPSYS	RW	32	0x0000 0210	0x4A0A 9210

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23.13.6.2.2 USBFSHOST Register Description

Table 23-1258. HCREVISION

Address Offset	0x0000 0000		
Physical Address	See Table 23-1257.	**Instance**	USBFSHOST
Description	OHCI revision number		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

Bits	Field Name	Description	Type	Reset
31:0	RESERVED	IP Revision	R	TI internal data

Table 23-1259. Register Call Summary for Register HCREVISION

USBFSHOST Register Manual
- USBFSHOST Register Summary: [0]

Table 23-1260. HCCONTROL

Address Offset	0x0000 0004		
Physical Address	See Table 23-1257.	**Instance**	USBFSHOST
Description	HC operating mode register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																					RWE	RWC	IR	HCFS		BLE	CLE	IE	PLE	CBSR	

Bits	Field Name	Description	Type	Reset
31:11	RESERVED	Reserved	R	0x000000
10	RWE	Remote wake-up enable	RW	0
9	RWC	Remote wake up connected.	RW	0
8	IR	Interrupt routing.	RW	0
7:6	HCFS	Host controller functional state 0x0: HCFS: USB reset 0x1: HCFS: USB resume 0x2: HCFS: USB operational 0x3: HCFS: USB suspend	RW	0x0
5	BLE	Bulk list processing enable 0x0: The bulk ED list is not processed after the next SOF. 0x1: Enables processing of the bulk ED list in the next frame.	RW	0
4	CLE	Control list processing enable 0x0: Control ED list is not processed after the next SOF. 0x1: Enables processing of control ED list in the next frame.	RW	0
3	IE	Isochronous ED processing enabled by host controller driver. 0x0: Isochronous EDs are not processed. 0x1: Enables processing of isochronous EDs	RW	0

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Bits	Field Name	Description	Type	Reset
2	PLE	Periodic list enable 0x0: Periodic ED lists are not processed after the next frame. 0x1: Enables processing of periodic ED lists in the next frame	RW	0
1:0	CBSR	Control/bulk service ratio. Specifies the ratio between control and bulk EDs processed in a frame. 0x0: One control ED per bulk ED 0x1: Two control ED per bulk ED 0x2: Three control ED per bulk ED 0x3: Four control ED per bulk ED	RW	0x0

Table 23-1261. Register Call Summary for Register HCCONTROL

USBFSHOST Register Manual
- USBFSHOST Register Summary: [0]

Table 23-1262. HCCOMMANDSTATUS

Address Offset	0x0000 0008		
Physical Address	See Table 23-1257.	**Instance**	USBFSHOST
Description	HC Command and status		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														SOC		RESERVED												OCR	BLF	CLF	HCR

Bits	Field Name	Description	Type	Reset
31:18	RESERVED	Reserved	R	0x0000
17:16	SOC	Scheduling overrun count	R	0x0
15:4	RESERVED	Reserved	R	0x000
3	OCR	Ownership change request	RW	0
2	BLF	Bulk list filled	RW	0
1	CLF	Control list filled	RW	0
0	HCR	Host controller reset (software reset) Set this bit to initiate a USB host controller reset. This resets most USB host controller OHCI registers. OHCI register accesses must not be attempted until a read of this register returns a 0. 0x0: No effect 0x1: USB host controller is reset.	RW	0

Table 23-1263. Register Call Summary for Register HCCOMMANDSTATUS

FSUSB Host Controller Functional Description
- Resets: [0]

USBFSHOST Register Manual
- USBFSHOST Register Summary: [1]

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Table 23-1264. HCINTERRUPTSTATUS

Address Offset	0x0000 000C		
Physical Address	See Table 23-1257.	**Instance**	USBFSHOST
Description	HC Interrupt status		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	OC	RESERVED																						RHSC	FNO	UE	RD	SF	WDH	SO	

Bits	Field Name	Description	Type	Reset
31	RESERVED	Reserved	R	0
30	OC	Ownership change	R	0
29:7	RESERVED	Reserved	R	0x000000
6	RHSC	Root hub status change When 0x1: A root hub status change has occurred. Write 0x0: No effect Write 0x1: Clears this bit	RW	0
5	FNO	Frame number overflow When 0x1: A frame number overflow has occurred. Write 0x0: No effect Write 0x1: Clears this bit	RW	0
4	UE	Unrecoverable error. When 0x1: An unrecoverable error has occurred. Write 0x0: No effect Write 0x1: Clears this bit	RW	0
3	RD	Resume detected. When 0x1: A downstream device has issued a resume request. Write 0x0: No effect Write 0x1: Clears this bit	RW	0
2	SF	Start of frame. When 0x1: A SOF has been issued. Write 0x0: No effect Write 0x1: Clears this bit	RW	0
1	WDH	Write done head When 0x1: the USB host controller has updated the HCDONEHEAD register. Write 0x0: No effect Write 0x1: Clears this bit	RW	0
0	SO	Scheduling overrun When 0x1: A scheduling overrun has occurred. Write 0x0: No effect Write 0x1: Clears this bit	RW	0

Table 23-1265. Register Call Summary for Register HCINTERRUPTSTATUS

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- USBFSHOST Register Summary: [0]

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Table 23-1266. HCINTERRUPTENABLE

Address Offset	0x0000 0010		
Physical Address	See Table 23-1257.	**Instance**	USBFSHOST
Description	HC Interrupt Enable		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MIE	OC	RESERVED																						RHSC	FNO	UE	RD	SF	WDH	SO	

Bits	Field Name	Description	Type	Reset
31	MIE	Master interrupt enable When 0x1: Allows other enabled OHCI interrupt sources to propagate to the device interrupt controller. When 0x0: OHCI interrupt sources are ignored. Write 0x0: No effect Write 0x1: Sets this bit	RW	0
30	OC	Ownership change	RW	0
29:7	RESERVED	Reserved	R	0x000000
6	RHSC	Root hub status change When 0x1 and MIE is 0x1: Allows root hub status change interrupts to propagate to the device interrupt controller. When 0x0 or MIE is 0x0: root hub status change interrupts do not propagate. Write 0x0: No effect Write 0x1: Sets this bit	RW	0
5	FNO	Frame number overflow. When 0x1 and MIE is 0x1: Allows FNO interrupts to propagate to the device interrupt controller. When 0x0 or MIE is 0x0: FNO interrupts do not propagate. Write 0x0: No effect Write 0x1: Sets this bit	RW	0
4	UE	Unrecoverable error. When 0x1 and MIE is 0x1: Allows UE interrupts to propagate to the device interrupt controller. When 0x0 or MIE is 0x0: UE interrupts do not propagate. Write 0x0: No effect Write 0x1: Sets this bit	RW	0
3	RD	Resume detected. When 0x1 and MIE is 0x1: Allows RD interrupts to propagate to the device interrupt controller. When 0x0 or MIE is 0x0: RD interrupts do not propagate. Write 0x0: No effect Write 0x1: Sets this bit	RW	0
2	SF	Start of frame When 0x1 and MIE is 0x1: Allows SF interrupts to propagate to the device interrupt controller. When 0x0 or MIE is 0x0: SF interrupts do not propagate. Write 0x0: No effect Write 0x1: Sets this bit	RW	0
1	WDH	Write done head When 0x1 and MIE is 0x1: Allows WDH interrupts to propagate to the device interrupt controller. When 0x0 or MIE is 0x0: WDH interrupts do not propagate. Write 0x0: No effect Write 0x1: Sets this bit	RW	0
0	SO	Scheduling overrun. When 0x1 and MIE is 0x1: Allows SO interrupts to propagate to the device interrupt controller. When 0x0 or MIE is 0x0: SO interrupts do not propagate. Write 0x0: No effect Write 0x1: Sets this bit	RW	0

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Table 23-1267. Register Call Summary for Register HCINTERRUPTENABLE

FSUSB Host Controller Basic Programming Model
- FSUSBHC Global Initialization: [0] [1]

USBFSHOST Register Manual
- USBFSHOST Register Summary: [2]
- USBFSHOST Register Description: [3] [4] [5] [6] [7] [8] [9] [10]

Table 23-1268. HCINTERRUPTDISABLE

Address Offset	0x0000 0014		
Physical Address	See Table 23-1257.	**Instance**	USBFSHOST
Description	HC Interrupt disable		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MIE	OC	RESERVED																							RHSC	FNO	UE	RD	SF	WDH	SO

Bits	Field Name	Description	Type	Reset
31	MIE	Master interrupt enable Always reads 0x0 Write 0x0: No effect Write 0x1: Clears the HCINTERRUPTENABLE MIE bit	RW	0
30	OC	Ownership change	RW	0
29:7	RESERVED	Reserved	R	0x000000
6	RHSC	Root hub status change Always reads 0x0 Write 0x0: No effect Write 0x1: Clears the HCINTERRUPTENABLE RHSC bit	RW	0
5	FNO	Frame number overflow Always reads 0x0 Write 0x0: No effect Write 0x1: Clears the HCINTERRUPTENABLE FNO bit	RW	0
4	UE	Unrecoverable error Always reads 0x0 Write 0x0: No effect Write 0x1: Clears the HCINTERRUPTENABLE UE bit	RW	0
3	RD	Resume detected Always reads 0x0 Write 0x0: No effect Write 0x1: Clears the HCINTERRUPTENABLE RD bit	RW	0
2	SF	Start of frame Always reads 0x0 Write 0x0: No effect Write 0x1: Clears the HCINTERRUPTENABLE SF bit	RW	0
1	WDH	Write done head Always reads 0x0 Write 0x0: No effect Write 0x1: Clears the HCINTERRUPTENABLE WDH bit	RW	0
0	SO	Scheduling overrun Always reads 0x0 Write 0x0: No effect Write 0x1: Clears the HCINTERRUPTENABLE SO bit	RW	0

Table 23-1269. Register Call Summary for Register HCINTERRUPTDISABLE

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- USBFSHOST Register Summary: [0]

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Table 23-1270. HCHCCA

Address Offset	0x0000 0018		
Physical Address	See Table 23-1257.	**Instance**	USBFSHOST
Description	HC HCCA address register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HCCA																								RESERVED							

Bits	Field Name	Description	Type	Reset
31:8	HCCA	Physical address of the beginning of the HCCA	RW	0x000000
7:0	RESERVED	Reserved	R	0x00

Table 23-1271. Register Call Summary for Register HCHCCA

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- USBFSHOST Register Summary: [0]

Table 23-1272. HCPERIODCURRENTED

Address Offset	0x0000 001C		
Physical Address	See Table 23-1257.	**Instance**	USBFSHOST
Description	HC Current periodic register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PCED																												RESERVED			

Bits	Field Name	Description	Type	Reset
31:4	PCED	Physical address of current ED on the periodic ED list	R	0x0000000
3:0	RESERVED	Reserved	R	0x0

Table 23-1273. Register Call Summary for Register HCPERIODCURRENTED

USBFSHOST Register Manual
- USBFSHOST Register Summary: [0]

Table 23-1274. HCCONTROLHEADED

Address Offset	0x0000 0020		
Physical Address	See Table 23-1257.	**Instance**	USBFSHOST
Description	HC head control register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHED																												RESERVED			

Bits	Field Name	Description	Type	Reset
31:4	CHED	Physical address of head ED on the control ED list	RW	0x0000000
3:0	RESERVED	Reserved	R	0x0

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Table 23-1275. Register Call Summary for Register HCCONTROLHEADED

USBFSHOST Register Manual

- USBFSHOST Register Summary: [0]

Table 23-1276. HCCONTROLCURRENTED

Address Offset	0x0000 0024		
Physical Address	See Table 23-1257.	**Instance**	USBFSHOST
Description	HC current control register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CCED																												RESERVED			

Bits	Field Name	Description	Type	Reset
31:4	CCED	Physical address of current ED on the control ED list	RW	0x0000000
3:0	RESERVED	Reserved	R	0x0

Table 23-1277. Register Call Summary for Register HCCONTROLCURRENTED

USBFSHOST Register Manual

- USBFSHOST Register Summary: [0]

Table 23-1278. HCBULKHEADED

Address Offset	0x0000 0028		
Physical Address	See Table 23-1257.	**Instance**	USBFSHOST
Description	HC head bulk register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BHED																												RESERVED			

Bits	Field Name	Description	Type	Reset
31:4	BHED	Physical address of head ED on the bulk ED list	RW	0x0000000
3:0	RESERVED	Reserved	R	0x0

Table 23-1279. Register Call Summary for Register HCBULKHEADED

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- USBFSHOST Register Summary: [0]

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Table 23-1280. HCBULKCURRENTED

Address Offset	0x0000 002C		
Physical Address	See Table 23-1257.	**Instance**	USBFSHOST
Description	HC current bulk register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BCED																												RESERVED			

Bits	Field Name	Description	Type	Reset
31:4	BCED	Physical address of current ED on the bulk ED list	RW	0x0000000
3:0	RESERVED	Reserved	R	0x0

Table 23-1281. Register Call Summary for Register HCBULKCURRENTED

USBFSHOST Register Manual

- USBFSHOST Register Summary: [0]

Table 23-1282. HCDONEHEAD

Address Offset	0x0000 0030		
Physical Address	See Table 23-1257.	**Instance**	USBFSHOST
Description	HC head done register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DH																												RESERVED			

Bits	Field Name	Description	Type	Reset
31:4	DH	Physical address of last TD that was added to the done queue	R	0x0000000
3:0	RESERVED	Reserved	R	0x0

Table 23-1283. Register Call Summary for Register HCDONEHEAD

USBFSHOST Register Manual

- USBFSHOST Register Summary: [0]
- USBFSHOST Register Description: [1]

Table 23-1284. HCFMINTERVAL

Address Offset	0x0000 0034		
Physical Address	See Table 23-1257.	**Instance**	USBFSHOST
Description	HC Frame Interval register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIT	FSMPS															RESERVED	FI														

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Bits	Field Name	Description	Type	Reset
31	FIT	Frame interval toggle	RW	0
30:16	FSMPS	Largest data packet size for full-speed packets, bit times.	RW	0x0000
15:14	RESERVED	Reserved	R	0x0
13:0	FI	Frame interval Number of 12-MHz clocks in the USB frame. The nominal value is set to 11,999 to give a 1-ms frame.	RW	0x2EDF

Table 23-1285. Register Call Summary for Register HCFMINTERVAL

USBFSHOST Register Manual
- USBFSHOST Register Summary: [0]

Table 23-1286. HCFMREMAINING

Address Offset	0x0000 0038		
Physical Address	See Table 23-1257.	**Instance**	USBFSHOST
Description	HC Frame-remaining register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FRT	RESERVED																							FR							

Bits	Field Name	Description	Type	Reset
31	FRT	Frame remaining toggle	R	0
30:14	RESERVED	Reserved	R	0x00000
13:0	FR	Frame remaining	R	0x0000

Table 23-1287. Register Call Summary for Register HCFMREMAINING

USBFSHOST Register Manual
- USBFSHOST Register Summary: [0]

Table 23-1288. HCFMNUMBER

Address Offset	0x0000 003C		
Physical Address	See Table 23-1257.	**Instance**	USBFSHOST
Description	HC Frame number register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																FN															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x0000
15:0	FN	Frame number	R	0x0000

Table 23-1289. Register Call Summary for Register HCFMNUMBER

USBFSHOST Register Manual
- USBFSHOST Register Summary: [0]

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Table 23-1290. HCPERIODICSTART

Address Offset	0x0000 0040		
Physical Address	See Table 23-1257.	**Instance**	USBFSHOST
Description	HC Periodic start register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PS															

Bits	Field Name	Description	Type	Reset
31:14	RESERVED	Reserved	R	0x00000
13:0	PS	Periodic start The host controller driver must program this value to be about 10% less than the frame interval field value so that control and bulk EDs have priority for the first 10% of the frame; then periodic EDs have priority for the remaining 90% of the frame.	RW	0x0000

Table 23-1291. Register Call Summary for Register HCPERIODICSTART

USBFSHOST Register Manual

- USBFSHOST Register Summary: [0]

Table 23-1292. HCLSTHRESHOLD

Address Offset	0x0000 0044		
Physical Address	See Table 23-1257.	**Instance**	USBFSHOST
Description	HC low-speed threshold register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				LST											

Bits	Field Name	Description	Type	Reset
31:12	RESERVED	Reserved	R	0x00000
11:0	LST	Low-speed threshold.	RW	0x628

Table 23-1293. Register Call Summary for Register HCLSTHRESHOLD

USBFSHOST Register Manual

- USBFSHOST Register Summary: [0]

Table 23-1294. HCRHDESCRIPTORA

Address Offset	0x0000 0048		
Physical Address	See Table 23-1257.	**Instance**	USBFSHOST
Description	HC root hub A register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
POTPG								RESERVED											NOCP	OCPM	DT	NPS	PSM	NDP							

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Bits	Field Name	Description	Type	Reset
31:24	POTPG	Power-on to power-good time Defines the minimum length of time (2 ms * POTPG) between the USB host controller turning on power to a downstream port, and when the USB host can access the downstream device.	RW	0x0A
23:13	RESERVED	Reserved	R	0x000
12	NOCP	No overcurrent protection 0x0: Overcurrent status is reported collectively for all downstream ports. 0x1: the USB host controller does not implement overcurrent protection inputs.	RW	0
11	OCPM	Overcurrent protection mode	RW	0
10	DT	Device type Always reads 0x0: Indicates that the USB host controller implemented is not a compound device	R	0
9	NPS	No power switching 0x0: VBUS power switching is supported, either per-port or all-port switched per the power. 0x1: VBUS power switching is not supported, power is available to all downstream ports.	RW	0
8	PSM	Power switching mode 0x0: Indicates that all ports are powered at the same time 0x1: Individual port power switching is supported	RW	0
7:0	NDP	Number of downstream ports.	R	0x01

Table 23-1295. Register Call Summary for Register HCRHDESCRIPTORA

USBFSHOST Register Manual

- USBFSHOST Register Summary: [0]

Table 23-1296. HCRHDESCRIPTORB

Address Offset	0x0000 004C		
Physical Address	See Table 23-1257.	**Instance**	USBFSHOST
Description	HC root hub B register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														PPCM	RESERVED	RESERVED														DR	RESERVED

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17	PPCM	Port power control mask This bit defines whether downstream port #1 has port power controlled by the global power control. When set. the port power state is only affected by per-port power control. When cleared the port is controlled by the global power switch. This field is not valid if the device is configured to global switch mode.	RW	0
16	RESERVED		R	0
15:2	RESERVED		R	0x0000

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Bits	Field Name	Description	Type	Reset
1	DR	Device removable This bit defines whether the downstream port has a removable device. When cleared, the attached device is removable. When set, the attached device is not removable. bit 1: Device attached to port #1	RW	0
0	RESERVED		R	0

Table 23-1297. Register Call Summary for Register HCRHDESCRIPTORB

USBFSHOST Register Manual

- USBFSHOST Register Summary: [0]
- USBFSHOST Register Description: [1] [2]

Table 23-1298. HCRHSTATUS

Address Offset	0x0000 0050		
Physical Address	See Table 23-1257.	**Instance**	USBFSHOST
Description	HC root hub status register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CRWE	RESERVED													OCIC	LPSC	DRWE	RESERVED													OCI	LPS

Bits	Field Name	Description	Type	Reset
31	CRWE	Clear remote wake-up enable Write 0x0: No effect Write 0x1: Clears the device remote wake-up enable bit	W	0
30:18	RESERVED	Reserved	R	0x0000
17	OCIC	Overcurrent indication change This bit is automatically set when the overcurrent indicator bit changes. Write 0x0: No effect Write 0x1: Clears this bit	RW	0
16	LPSC	Local power status change Always reads 0x0: The root hub does not support the local power status feature. Write 0x0: No effect Write 0x1: Sets port power status bits for all ports, if power switching mode is 0. Sets port power status bits for ports with their corresponding port power control mask bits cleared if power switching mode is 1.	RW	0
15	DRWE	Device remote wake-up enable Enables a connect status change event as a resume event, causing a USB suspend to USB resume state transition and sets the resume detected interrupt status bit. Read 0x1: Connect status change is a remote wake-up event. Read 0x0: Connect status change is not a remote wake-up event. Write 0x0: No effect Write 0x1: Sets the device remote wake-up enable bit	RW	0
14:2	RESERVED	Reserved	R	0x0000
1	OCI	Overcurrent indicator. Reports global overcurrent indication if global overcurrent reporting is selected. If per-port overcurrent protection is implemented, this bit is always 0. Read 0x0: All power operations are normal. Read 0x1: An overcurrent condition exists.	R	0

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Bits	Field Name	Description	Type	Reset
0	LPS	Local power status. Always reads 0x0 Write 0x0: No effect Write 0x1: When in global power mode (power switching mode = 0), turns off power to all ports. If in per-port power mode (power switching mode = 1), turns of power to those ports whose corresponding port power control mask bit is 0.	RW	0

Table 23-1299. Register Call Summary for Register HCRHSTATUS

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- USBFSHOST Register Summary: [0]

Table 23-1300. HCRHPORTSTATUS

Address Offset	0x0000 0054		
Physical Address	See Table 23-1257.	**Instance**	USBFSHOST
Description	HC Port 1 status and control register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											PRSC	OCIC	PSSC	PESC	CSC	RESERVED						LSDA_CPP	PPS_SPP	RESERVED			PRS_SPR	POCI_CSS	PSS_SPS	PES_SPE	CCS_CPE

Bits	Field Name	Description	Type	Reset
31:21	RESERVED	Reserved	R	0x000
20	PRSC	Port 1 reset status change This bit is set when the Port 1 port reset status bit has changed. Write 0x0: No effect Write 0x1: Clears this bit	RW	0
19	OCIC	Port 1 overcurrent indicator change This bit is set when the Port 1 port overcurrent indicator has changed. Write 0x0: No effect Write 0x1: Clears this bit	RW	0
18	PSSC	Port 1 suspend status change This bit is set when the Port1 port suspend status has changed. Write 0x0: No effect Write 0x1: Clears this bit	RW	0
17	PESC	Port 1 enable status change This bit is set when the Port1 port enable status has changed. Write 0x0: No effect Write 0x1: Clears this bit	RW	0
16	CSC	Port 1 connect status change This bit is set when the Port1 port current connect status has changed due to a connect or disconnect event. If current connect status is 0 when a set port reset, set port enable, or set port suspend write occurs, this bit is set. Write 0x0: No effect Write 0x1: Clears this bit Note: If the DR bit HCRHDESCRIPTORB[1] is set, this bit is set only after a root hub reset to inform the system that the device is attached.	RW	0
15:10	RESERVED	Reserved	R	0x00
9	LSDA_CPP	Port 1 low-speed device attached/clear port power. This bit is valid only when port 1 current connect status is 1. Read 0x0: A full-speed device is attached to port 1. Read 0x1: A low-speed device is attached to port 1. Write 0x0: No effect Write 0x1: Clears the port 1 port power status.	RW	0

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Bits	Field Name	Description	Type	Reset
8	PPS_SPP	Port 1 port power status/set port power. Read 0x0: Port 1 power is off. Read 0x1: Port 1 power is on. Write 0x0: No effect Write 0x1: Sets the port 1 port power status bit	RW	0
7:5	RESERVED	Reserved	R	0x0
4	PRS_SPR	Port 1 port reset status/set port reset. Read 0x0: USB reset is not being sent to port 1. Read 0x1: Port 1 is signaling the USB reset. Write 0x0: No effect Write 0x1: Sets the port 1 port reset status bit and causes the USB host controller to begin signaling USB reset to port 1	RW	0
3	POCI_CSS	Port 1 port overcurrent indicator/clear suspend status Read 0x0: No port 1 port overcurrent condition has occurred. Read 0x1: A port 1 port overcurrent condition has occurred. Write 0x0: No effect Write 0x1: When port 1 port suspend status is 1, it causes resume signaling on port 1. When port 1 port suspend status is 0, it has no effect.	RW	0
2	PSS_SPS	Port 1 port suspend status/set port suspend This bit is cleared automatically at the end of the USB resume sequence and also at the end of the USB reset sequence. Write 0x0: No effect Read 0x0: Port 1 is not in the USB suspend state. Read 0x1: Port 1 is in the USB suspend state or is in the resume sequence. Write 0x1: If port 1 current connect status is 1, sets the port 1 port suspend status bit and places port 1 in USB suspend state. If current connect status is 0, it sets connect status instead change to inform the USB host controller driver in an attempt to suspend a disconnected port.	RW	0
1	PES_SPE	Port 1 port enable status/set port enable This bit is automatically set at completion of port 1 USB reset, if it was not already set before the USB reset completed, and is automatically set at the end of a USB suspend, if the port was not enabled when the USB resume completed. Read 0x0: Port 1 is not enabled. Read 0x1: Port 1 is enabled. Write 0x0: No effect Write 0x1: When port 1 current connect status is 1, sets the port 1 port enable status bit. When port 1 current status is 0, it has no effect.	RW	0
0	CCS_CPE	Port 1 current connection status/clear port enable Read 0x0: No USB device is attached to port 1. Read 0x1: Port 1 currently has a USB device attached. Write 0x0: No effect Write 0x1: Clears the port 1 port enable bit Note: This bit is set to 1 if the DR bit HCRHDESCRIPTORB[1] is set to indicate a nonremovable device on port 1.	RW	0

Table 23-1301. Register Call Summary for Register HCRHPORTSTATUS

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- USBFSHOST Register Summary: [0]

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Table 23-1302. HCOCPREV

Address Offset	0x0000 0200		
Physical Address	See Table 23-1257.	**Instance**	USBFSHOST
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP Revision	R	TI Internal data

Table 23-1303. Register Call Summary for Register HCOCPREV

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- USBFSHOST Register Summary: [0]

Table 23-1304. HCOCPHWI

Address Offset	0x0000 0204		
Physical Address	See Table 23-1257.	**Instance**	USBFSHOST
Description	Hardware information register, maintains the IP modules hardware configuration. The fields can be set to different values through parameters.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INFO																															

Bits	Field Name	Description	Type	Reset
31:0	INFO	IP-module dependent. Information about the IP module hardware configuration, that is, typically the module HDL generics (if any).	R	0x0000 002A

Table 23-1305. Register Call Summary for Register HCOCPHWI

USBFSHOST Register Manual

- USBFSHOST Register Summary: [0]

Table 23-1306. HCOCPSYS

Address Offset	0x0000 0210		
Physical Address	See Table 23-1257.	**Instance**	USBFSHOST
Description	OCP system configuration register holds the OCP power down control fields that controls the clock management.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						APPLICATIONSTARTCLOCK	SIMULATIONSCALEDOWN	RESERVED		STANDBY_MODE		IDLE_MODE		SOFT_RESET	RESERVED

Bits	Field Name	Description	Type	Reset
31:10	RESERVED		R	0x000000
9	APPLICATIONSTARTCLOCK	1: RCFG_SUSPEND_O output port is masked and this output port is held low (1'b0) 0: RCFG_SUSPEND_O port functions normally, that is, it indicates the SUSPEND mode.	RW	0
8	SIMULATIONSCALEDOWN	1: Simulation runs in time scaled down mode. 0: Simulation runs in real time. NOTE: This bit should not be set to 1 in actual hardware.	RW	0
7:6	RESERVED		R	0x0
5:4	STANDBY_MODE	Standby mode, controls the way USBFSHOST handles the STANDBY protocol. The application can program this field in the following configurations 2'b00 : Force standby 2'b01: Not supported (No-Standby) 2'b10: Smart standby 2'b11: Smart standby wake up	RW	0x3
3:2	IDLE_MODE	The idle mode controls the way USBFSHOST handles the IDLE protocol. The application can program this field in the following configurations 2'b00: Force Idle 2'b01: Not supported (No-Idle) 2'b10: Smart-Idle 2'b11: Smart-Idle wake up	RW	0x2
1	SOFT_RESET	Setting this bit to 1 resets the entire IP, except for OCP-IDLE, OCP-STANDBY, and OCP-DISCONNECT logic. This bit remains set until the IP comes out of soft reset.	RW	0
0	RESERVED		R	0

Table 23-1307. Register Call Summary for Register HCOCPSYS

FSUSB Host Controller Functional Description • Resets: [0] • IDLE Protocol: [1] [2] • STANDBY Protocol: [3]
FSUSB Host Controller Basic Programming Model • FSUSBHC Global Initialization: [4] [5]
USBFSHOST Register Manual • USBFSHOST Register Summary: [6]

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MMC/SD/SDIO

This chapter describes the features and functions of the multimedia card/SD card (MMC/SD/SDIO) interface of the device.

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24.3 MMC/SD/SDIO Integration 5259
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24.1 MMC/SD/SDIO Overview

The multimedia card high-speed/SD/SDIO (MMC/SD/SDIO) host controller provides an interface between a local host (LH) such as a microprocessor unit (MPU) or digital signal processor (DSP) and either MMC, SD memory cards, or SDIO cards and handles MMC/SD/SDIO transactions with minimal LH intervention.

Optionally, the controller is connected to the level 3 (L3) interconnect to have a direct access to system memory. It also supports two direct memory access (DMA) slave channels or a DMA master access (in this case, slave DMA channels are deactivated) depending on its integration. These controllers are embedded MMC/SD (eMMC/SD) controllers.

The application interface manages transaction semantics. The MMC/SD/SDIO host controller deals with MMC/SD/SDIO protocol at transmission level, data packing, adding cyclic redundancy checks (CRCs), start/end bit, and checking for syntactical correctness.

The application interface can send every MMC/SD/SDIO command and poll for the status of the adapter or wait for an interrupt request, which is sent back in case of exceptions or to warn of end of operation.

The application interface can read card responses or flag registers. It can also mask individual interrupt sources. All these operations can be performed by reading and writing control registers. The MMC/SD/SDIO host controller also supports two DMA channels.

There are five MMC/SD/SDIO host controllers inside the device:

Figure 24-1 gives an overview of the MMC/SD/SDIO1 controller instance (eMMC/SD).

Figure 24-2 gives an overview of the MMC/SD/SDIO2 controller instance (eMMC/SD).

Figure 24-3 gives an overview of the MMC/SD/SDIO3 through MMC/SD/SDIO5 controller instances.

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Figure 24-1. MMC/SD/SDIO1 Overview (where i = 1)

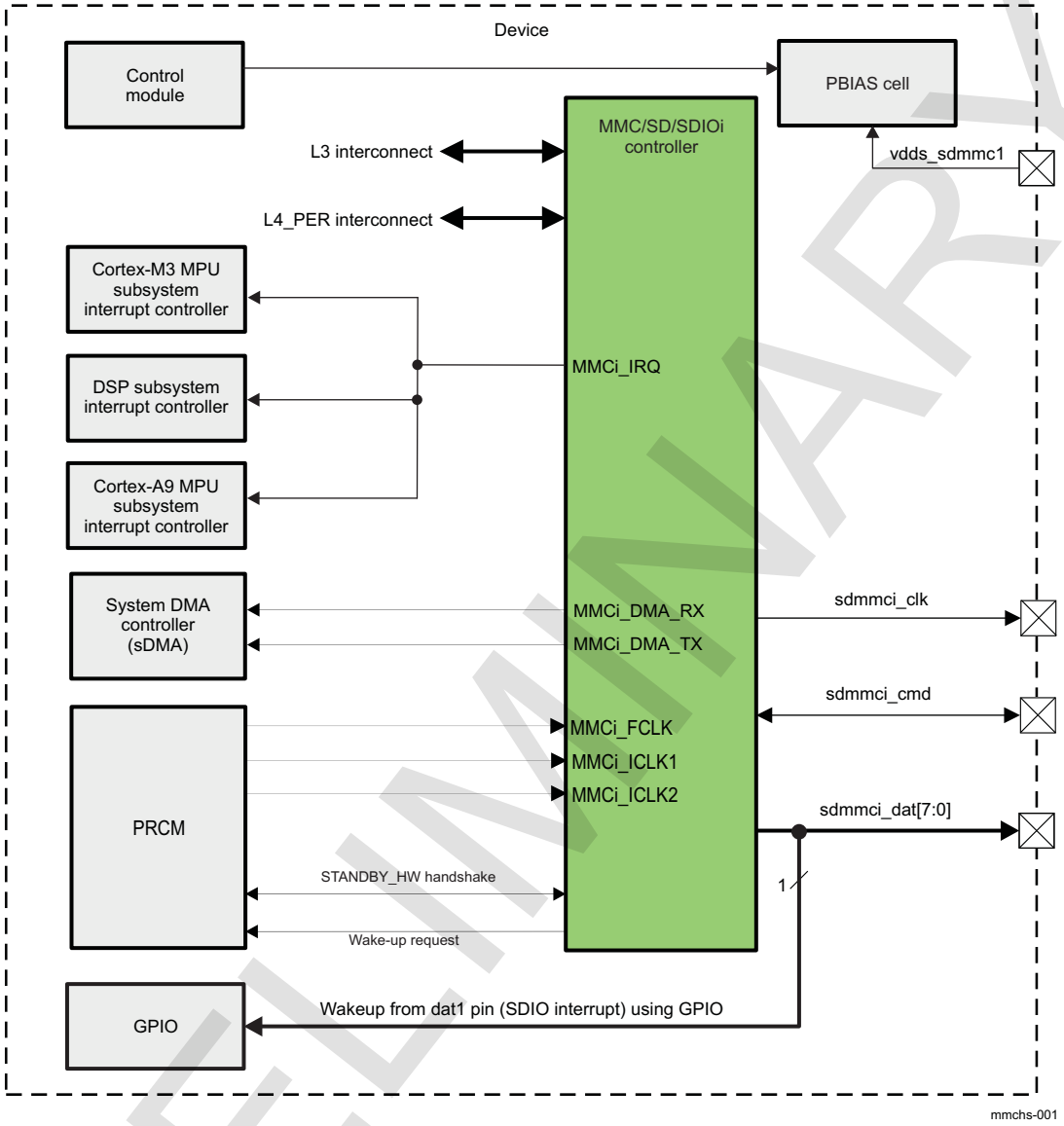

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Figure 24-2. MMC/SD/SDIO2 Overview (where i = 2)

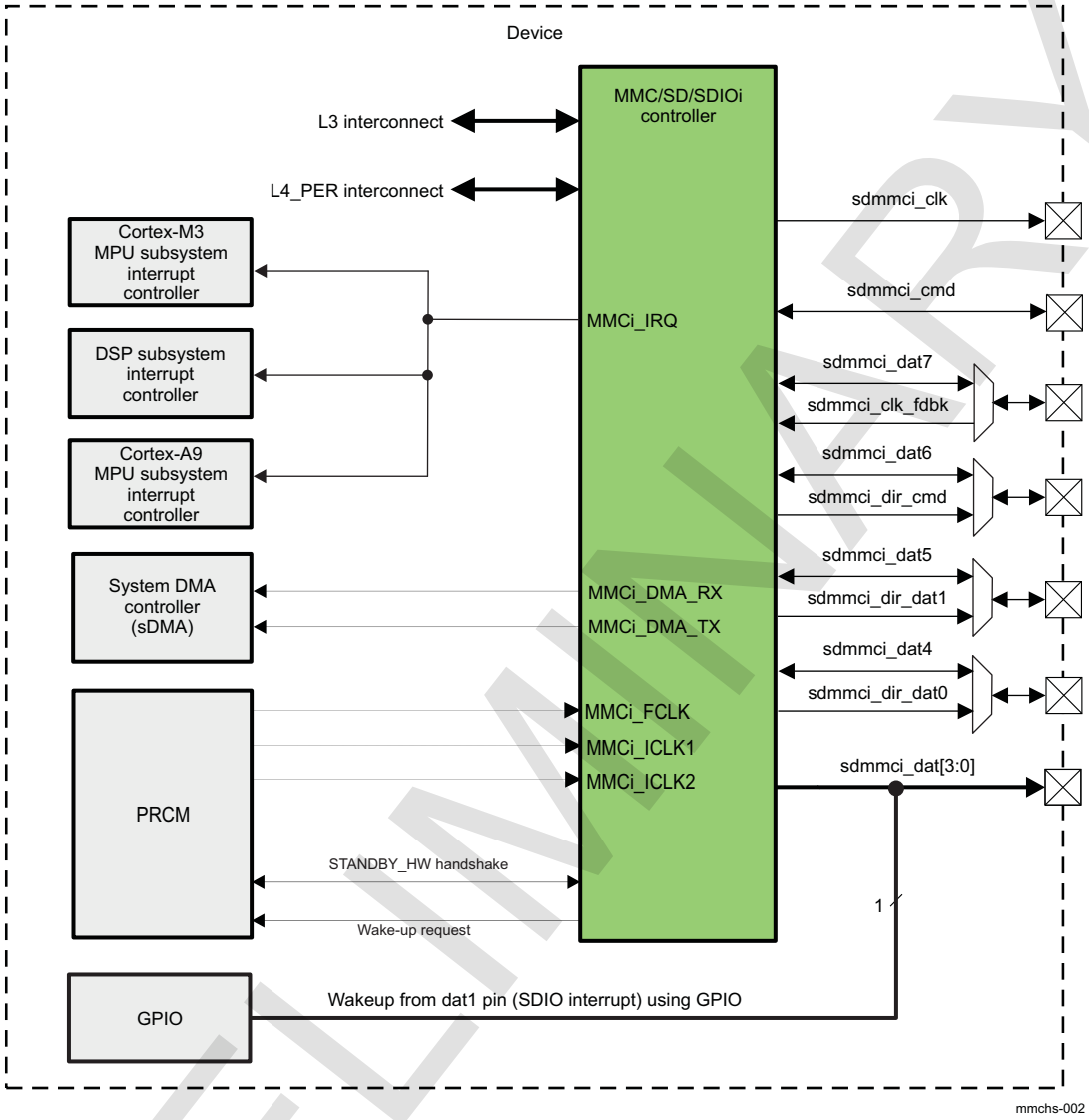

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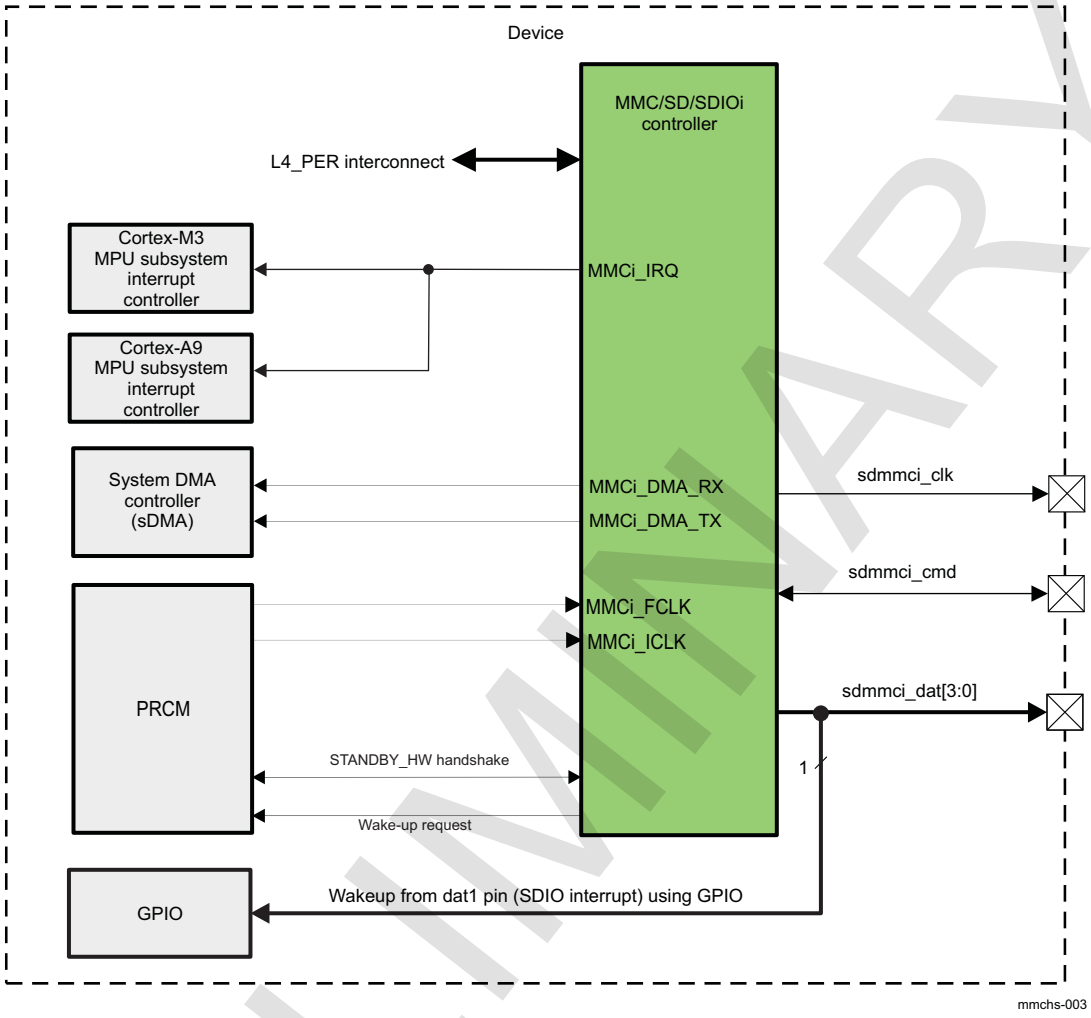
Figure 24-3. MMC/SD/SDIO3 Through MMC/SD/SDIO5 Overview (where i = 3, 4, or 5)



24.1.1 MMC/SD/SDIO Features

This section describes the features supplied by the MMC/SD/SDIO module.

Compliance with standards:

- Full compliance with MMC/eMMC command/response sets as defined in the *JC64 MMC/eMMC Standard Specification* v4.41, including high-capacity (size 2GB) cards HC MMC
- Full compliance with SD command/response sets as defined in the *SD Specifications Part 1 Physical Layer Simplified Specification* , v3.01, including high-capacity SDXC cards up to 2TB
- Full compliance with SDIO command/response sets and interrupt/read-wait suspend-resume operations, as defined in the *SDIO Card Specification, Part E1*, v2.00
- Full compliance with sets as defined in the *SD Card Specification, Part A2, SD Host Controller Standard Specification*, v2.00
- Full compliance with MMC bus testing procedure as defined in the *Multimedia Card System Specification*, v4.41
- Full compliance with CE-ATA command/response sets as defined in the *CE-ATA Standard Specification*
- Full compliance with ATA for MMCA specification
- Support command completion signal (CCS) and command completion signal disable (CCSD) management as specified in the *CE-ATA Standard Specification*

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Main features of the MMC/SD/SDIO host controller:

- Flexible architecture allowing support for new command structure
- Support:
  - 1- or 4-bit transfer mode specifications for SD and SDIO cards
  - 1-, 4-, or 8-bit transfer mode specifications for MMC cards
- Built-in buffer for read or write (up to 2048 bytes in single-buffering, 1024 bytes in double-buffering)
- 32-bit-wide access bus to maximize bus throughput
- Single interrupt line for interrupt source events
- Two slave DMA channels (one for TX, one for RX)
- Designed for low power
- Programmable clock generation
- Support SDIO read wait and suspend/resume functions
- Support stop at block gap
- Support boot mode operations as specified in the *JEDEC JC 64 MMC/eMMC Standard Specification, v4.41*
- Support dual data rate transfers (DDR mode) as specified in *JEDEC JC64 MMC/eMMC Standard Specification, v4.41*
- Support SDA 2.0 Part A2 programming model

Optional features (depending on module integration):

- Master interface (L3 interconnect)
- One master DMA (32-bit ADMA2), replacing the two slave DMA channels
- Retention mode is supported
- Support SDA 2.0 Part A2 DMA feature (ADMA2)

Supported data rates:

- In MMC mode:
  - Up to 768 Mbps (96 MB/s), 8-bit DDR data transfer, with a clock running at 48 MHz
  - Up to 384 Mbps (48 MB/s), 8-bit SDR data transfer, with a clock running at 48 MHz
- In SD mode:
  - Up to 384 Mbps (48 MB/s), 4-bit DDR data transfer with a clock running at 48 MHz
  - Up to 384 Mbps (48 MB/s), 4-bit SDR data transfer with a clock running at 96 MHz
- In SDIO mode:
  - Up to 192 Mbps (24 MB/s) in high-speed mode, 4-bit data transfer with a clock running at 48 MHz
  - Up to 24 Mbps (3 MB/s) in default speed mode, 1-bit data transfer with a clock running at 24 MHz

Supported clock frequencies:

- MMC mode:
  - Up to 48 MHz in DDR and SDR modes
- SD mode:
  - Up to 48 MHz in DDR mode
  - Up to 96 MHz in SDR mode
- SDIO mode:
  - Up to 48 MHz in SDR mode

Known limitations:

- No built-in hardware support for error correction codes (ECCs). For information about ECC, see the *Multimedia Card System Specification*, v4.4, and the *SD Memory Card Specifications*, v3.0.

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- The maximum block size defined in the *SD Memory Card Specifications*, v3.0, which the host driver can read and write to the buffer in the host controller, is 2048 bytes. The host controller supports a maximum block size of 1024 bytes. Up to 512 byte transfers, the buffer in the host controller is considered as a double-buffering with ping-pong management; half of the buffer can be written while the other half is read. For 512 to 1024 byte transfers, the entire buffer is dedicated to the transfer (read only or write only).
- SPI transfers are not supported.
- The module does not support card insertion and removal sensing with pullup resistor on the sdmmci_dat3 bus line, as specified in the *SD Memory Card Specifications – Part 1 Physical Layer Specification (SD Group, May 2006)*.

The differences between the MMC/SD/SDIO host controllers and a standard SD host controller defined by the *SD Card Specification, Part A2, SD Host Controller Standard Specification*, v2.00 are:

- The MMC/SD/SDIO host controllers support MMC cards.
- The clock divider in the MMC/SD/SDIO host controller supports a wider range of frequency than specified in the *SD Memory Card Specifications*, v2.0. The MMC/SD/SDIO host controller supports odd and even clock ratio.
- The MMC/SD/SDIO host controller supports configurable busy time-out.
- sDMA and ADMA2 64-bit modes are not supported.
- There is no external LED control.

NOTE: Only even ratios are supported in DDR mode.

Table 24-1 lists the features supported in the 4.41 standard.

Table 24-1. Standard 4.41 Supported Features

Feature	Support	Limitation	Comment
Bus width	1-bit mode		x 1, 4, 8 bits
	4-bit mode		
	8-bit mode		
Support density	No hardware limitation for density support	Limitation can come from file system (32GB)	
Simple boot (CMD, alternate boot)	No		OMAP4 ROM code supports the following boot mode:
			In raw mode the booting image can be at one of the four consecutive locations in the main area:
			offset 0x0
			0x20000 (128KB)
			0x40000 (256KB)
			0x60000 (384KB)
			(That is, it supports four boot partitions.)
Sleep mode	Yes		
Reliable write	Yes		
Secure write protection	Yes		
Hardware reset	No		Use the reset command instead of GPIO if hardware reset is needed.
Secure memory block (RPMB)	Yes		
Partition feature	Yes		
Secure erase	Yes		
1.2 V	Yes		

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Table 24-1. Standard 4.41 Supported Features (continued)

Feature	Support	Limitation	Comment
DDR Interface (bandwidth)	Up to 96MBps in DDR mode – 8-bit		
High-priority interrupt (read while write)	Yes		
Background operation	Yes		
Enhanced reliable write	Yes		

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24.2 MMC/SD/SDIO Environment

One MMC/SD/SDIO host controller can support one MMC memory card, one SD memory card, or one SDIO card.

Other combinations (for example, two SD cards, one MMC card, and one SD card) are not supported through a single controller.

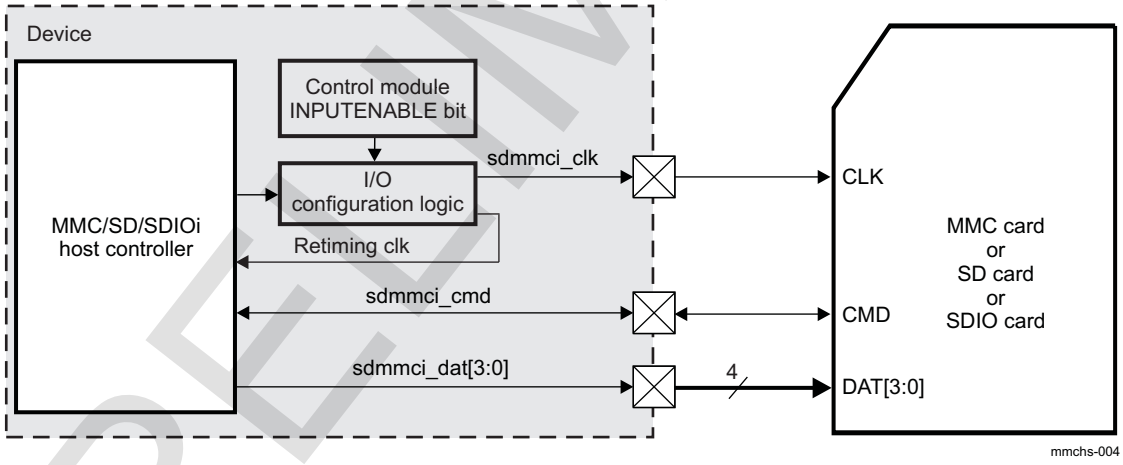
- The MMC/SD/SDIO1 controller integrates an internal transceiver that allows a direct connection to the MMC/SD/SDIO card (1.8 V and 3 V), without external transceiver. It is connected to the level 3 (L3) interconnect (internal DMA enabled) and supports 1- 4-, and 8-bit data transfers.
- The MMC/SD/SDIO2 controller allows connecting MMC/SD/SDIO cards (only 1.8V cards) or an external device that uses the MMC/SD/SDIO interface (JC64, for example). The module is connected to the L3 interconnect (internal DMA enabled) and supports 1-, 4-, and 8-bit data transfers. The second instance also supports an external transceiver and provides direction signals for data and command. Using an external transceiver device precludes 8-bit transfer mode.
- The MMC/SD/SDIO3, MMC/SD/SDIO4, and MMC/SD/SDIO5 controllers allow connecting MMC/SD/SDIO cards (only 1.8V cards) or an external device that uses the MMC/SD/SDIO interface (wireless LAN, for example). The modules are connected to the L4 interconnect and support 1-and 4-bit data transfers.

24.2.1 MMC/SD/SDIO Functional Modes

24.2.1.1 MMC/SD/SDIO Connected to an MMC, an SD, or an SDIO Card

Figure 24-4 shows the MMC/SD/SDIOi host controller (where i = 1 through 5) connected to an MMC, an SD, or an SDIO card and its related external connections.

Figure 24-4. MMC/SD/SDIOi Controller Connected to an MMC, an SD, or an SDIO Card Without External Transceiver (where i = 1 through 5)



NOTE: MMC/SD/SDIO1 and MMC/SD/SDIO2 support data transfers on 8 bits (and thus handle data on signals sdmmci_dat[7:0]).

Table 24-2 describes the MMC/SD/SDIOi inputs and outputs.

Table 24-2. MMC/SD/SDIOi I/O Description Without External Transceiver (where i = 1 through 5)

Signal Name	I/O [1]	Description	Reset Value
sdmmci_clk	O	External clock for MMC/SD/SDIO card[2]	0

(1) I = Input; O = Output

(2) This output signal is also used as retiming input (the INPUTENABLE bit in the corresponding pad configuration register must be set to 1).

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Table 24-2. MMC/SD/SDIOi I/O Description Without External Transceiver (where i = 1 through 5) (continued)

Signal Name	I/O [1]	Description	Reset Value
sdmmci_cmd	I/O	Command signal	HiZ[3]
sdmmci_dat[3:0]	I/O	Data signals	HiZ[3]
sdmmci_dat[7:4]	I/O	Data signals (only for modules MMC/SD/SDIO1 and MMC/SD/SDIO2)	HiZ[3]

(3) Initialized as input upon reset

24.2.1.2 MMC/SD/SDIO Connected to an MMC, an SD, or an SDIO Card Through an External Transceiver Device

Figure 24-5 shows the MMC/SD/SDIOi host controller (where i = 2) connected to an MMC, an SD, or an SDIO card and its related external connections.

Figure 24-5. MMC/SD/SDIOi Controller Connected to an MMC, an SD, or an SDIO Card With External Transceiver (where i = 2)

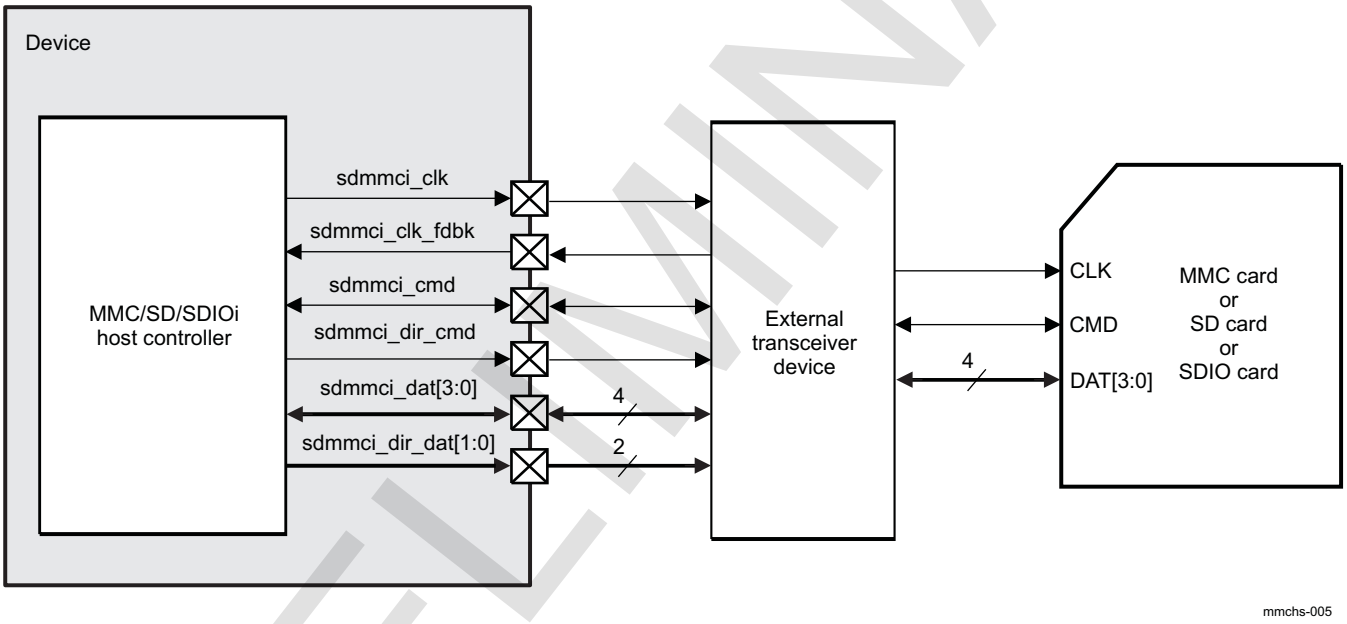

Table 24-3 describes the MMC/SD/SDIOi inputs and outputs.

Table 24-3. MMC/SD/SDIOi I/O Description With External Transceiver (where i = 2)

Signal Name	I/O [1]	Description	Reset Value
sdmmci_clk	O	External clock for MMC/SD/SDIO card	0
sdmmci_clk_fdbk	I	Input clock from MMC/SD/SDIO card	0
sdmmci_cmd	I/O	Command signal	HiZ[2]
sdmmci_dir_cmd	O	Direction control for mmc2_cmd signal when an external transceiver is used (high when transmit, low when receive)	0
sdmmci_dat[3:0]	I/O	Data signals	HiZ[2]
sdmmci_dir_dat0	O	Direction control for mmc2_dat0 signal when an external transceiver is used (high when transmit, low when receive)	0

(1) I = Input; O = Output
(2) Initialized as input upon reset

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Table 24-3. MMC/SD/SDIOi I/O Description With External Transceiver (where i = 2) (continued)

Signal Name	I/O [1]	Description	Reset Value
sdmmci_dir_dat1	O	Direction control for mmc2_dat1 signal when an external transceiver is used (high when transmit, low when receive)	0

NOTE: There is no signal for individually controlling the sdmmci_dat2 and sdmmci_dat3 direction (sdmmci_dir_dat2 and sdmmci_dir_dat3 are not delivered). This may limit the use of this interface with the SDIO card requesting the wait feature on the sdmmci_dat2 line.

24.2.2 Protocol and Data Format

The bus protocol between the MMC/SD/SDIOi host controller and the card is message-based. Each message is represented by one of the following parts:

Command: A command starts an operation. The command is transferred serially from the MMC/SD/SDIO host controller to the card on the sdmmci_cmd line.

Response: A response is an answer to a command. The response is sent from the card to the MMC/SD/SDIO host controller. It is transferred serially on the sdmmci_cmd line.

Data: Data are transferred from the MMC/SD/SDIOi host controller to the card or from a card to the MMC/SD/SDIO host controller using the data lines.

Busy: The sdmmci_dat0 signal is maintained low by the card as far as it is programming the data received.

CRC status: The CRC result is sent by the card through the sdmmci_dat0 line when executing a write transfer. In the case of transmission error, occurring on any of the active data lines, the card sends a negative CRC status on sdmmci_dat0. In the case of successful transmission, over all active data lines, the card sends a positive CRC status on sdmmci_dat0 and starts the data programming procedure.

24.2.2.1 Protocol

There are two types of data transfer:

- Sequential operation
- Block-oriented operation

There are specific commands for each type of operation (sequential or block-oriented).

For information about commands and programming sequences supported by the MMC, SD, and SDIO cards, see the *Multimedia Card System Specification*, *SD Memory Card Specifications*, and *SDIO Card Specification (Part E1*).

Figure 24-6 and Figure 24-7 show how sequential operations are defined. Sequential operation is only for 1-bit transfer and initiates a continuous data stream. The transfer terminates when a stop command follows on the sdmmci_cmd line.

CAUTION

Stream commands are supported only by MMC cards.

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Figure 24-6. Sequential Read Operation (MMC Cards Only)

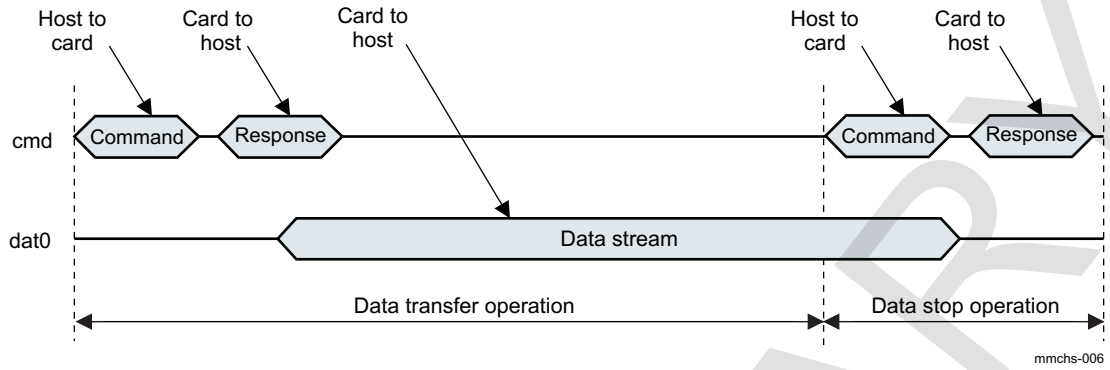

Figure 24-7. Sequential Write Operation (MMC Cards Only)

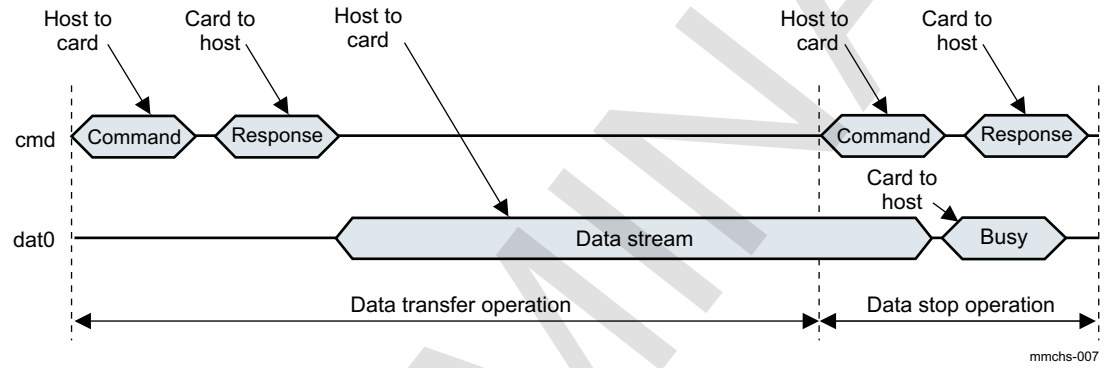

Figure 24-8 and Figure 24-9 show how multiple block-oriented operations are defined. A multiple block-oriented operation sends a data block plus CRC bits. The transfer terminates when a stop command follows on the sdmmci_cmd line. These operations are available for all kinds of cards.

Figure 24-8. Multiple Block Read Operation

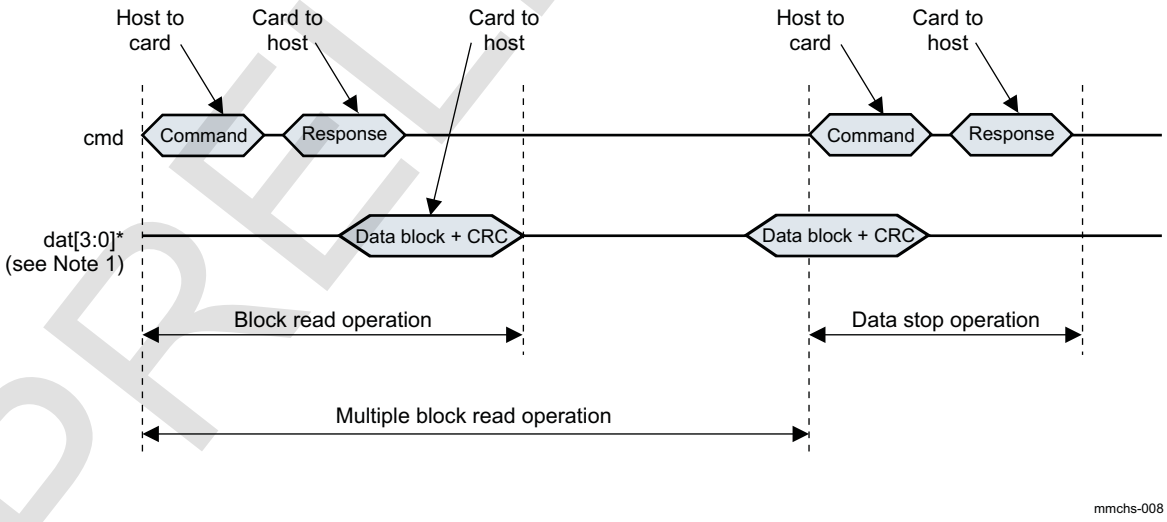

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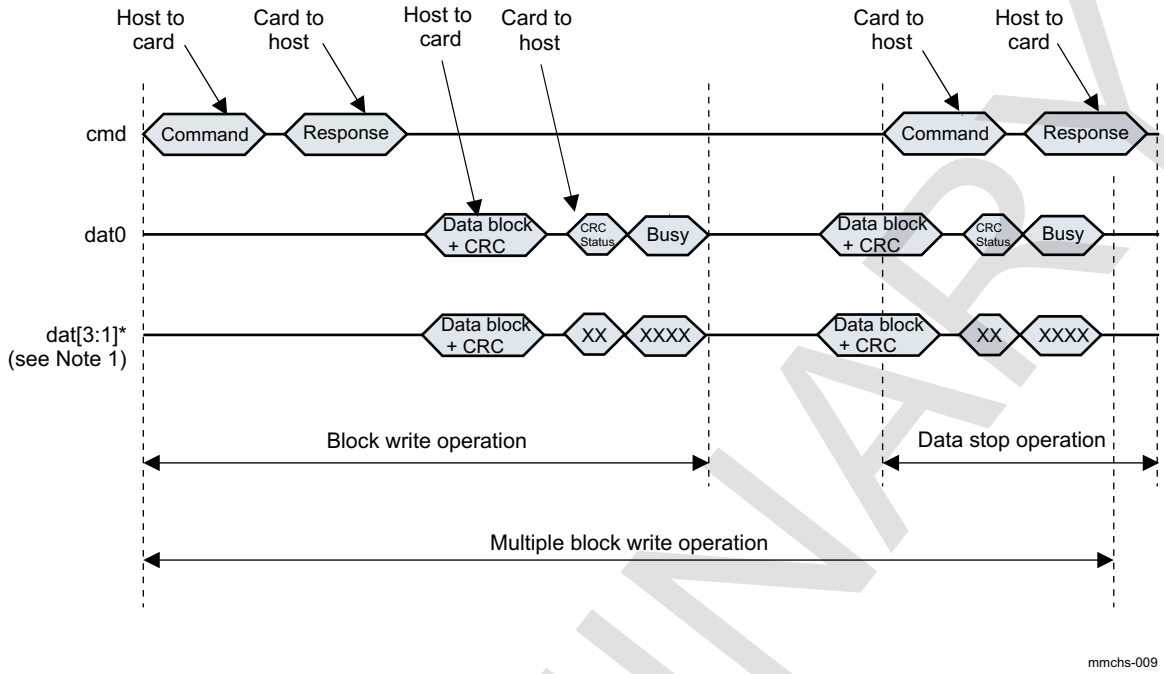
Figure 24-9. Multiple Block Write Operation With Card Busy Signal



NOTE:

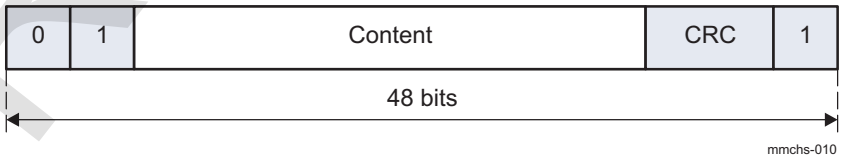
1. The card busy signal is not always generated by the card; the previous examples show a particular case.
2. Software must perform a software reset (set the MMCi.MMCHS_SYSCTL[26] SRD bit to 0x1) after a data time-out to ensure sdmmci_clk is stopped.
3. For multiblock transfer, and especially for MMC cards, a transfer can be aborted without using a stop command. If a CMD23 is used before data transfer to define the number of blocks that will be transferred, then the transfer stops automatically after the last block (if the MMC card supports this feature).

24.2.2.2 Data Format

Coding Scheme for Command Token

Command tokens always start with 0 and end with 1. The second bit is a transmitter bit: 1 for a host command. The content is the command index (coded by 6 bits) and an argument (for example, an address), coded by 32 bits. The content is protected by 7-bit CRC checksum (see Figure 24-10).

Figure 24-10. Command Token Format



Coding Scheme for Response Token

Response tokens always start with 0 and end with 1. The second bit is a transmitter bit: 0 for a card response. The content is different for each type of response (R1, R2, R3, R4, and R5, R6, R7 [for SDIO])

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and the content is protected by 7-bit CRC checksum (see Figure 24-11 and Figure 24-12). Depending on the type of commands sent to the card, the MMCHS_CMD register must be configured differently to avoid false CRC or index errors to be flagged on command response (see Table 24-4). For more information about response types, see the *Multimedia Card System Specification*, *SD Memory Card Specifications*, and *SDIO Card Specification*.

Figure 24-11. Response Token Format (R1, R3, R4, R5, R6, R7)

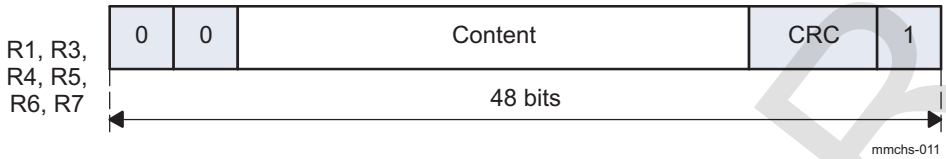

Figure 24-12. Response Token Format (R2)

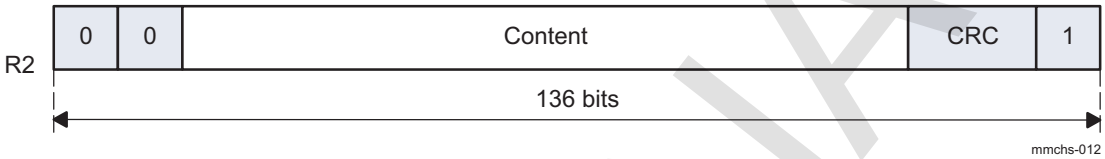

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Table 24-4. Relationship Between Configuration and Name of Response Type

Response Type MMCi.MMCHS_CMD[17:16] RSP_TYPE	Index Check Enable MMCi.MMCHS_CMD[20] CICE	CRC Check Enable MMCi.MMCHS_CMD[19] CCCE	Name of Response Type
00	0	0	No response
01	0	1	R2
10	0	0	R3 (R4 for SD cards)
10	1	1	R1, R6, R5, R7
11	1	1	R1b, R5b

Coding Scheme for Data Token

Data tokens always start with 0 and end with 1 (see Figure 24-13 through Figure 24-15).

Figure 24-13. Data Token Format for 1-Bit Transfers

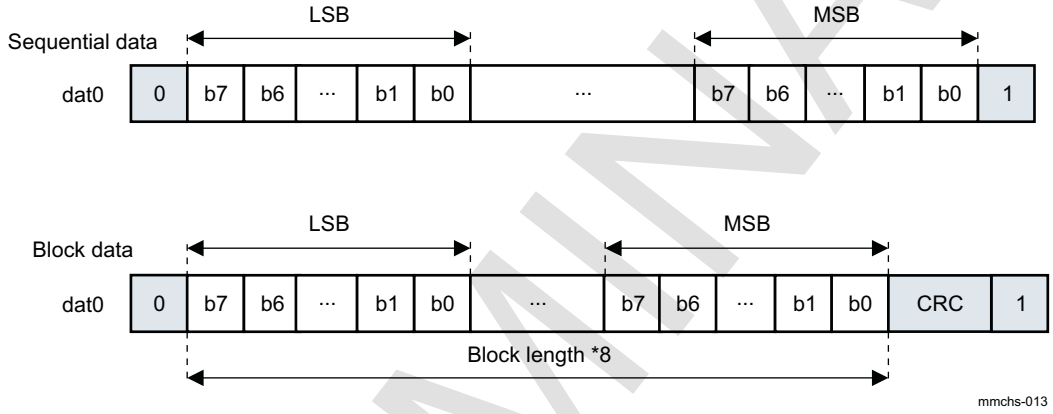

Figure 24-14. Data Token Format for 4-Bit Transfers

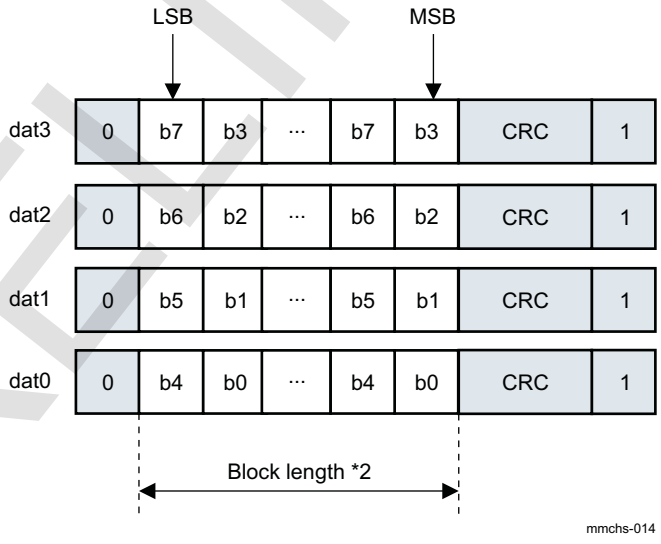

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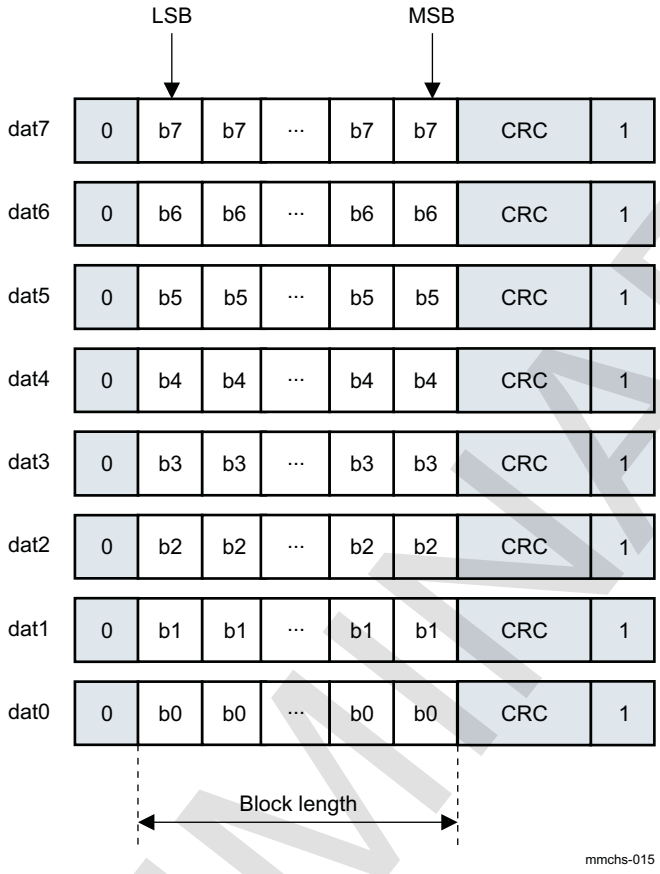
Figure 24-15. Data Token Format for 8-Bit Transfers



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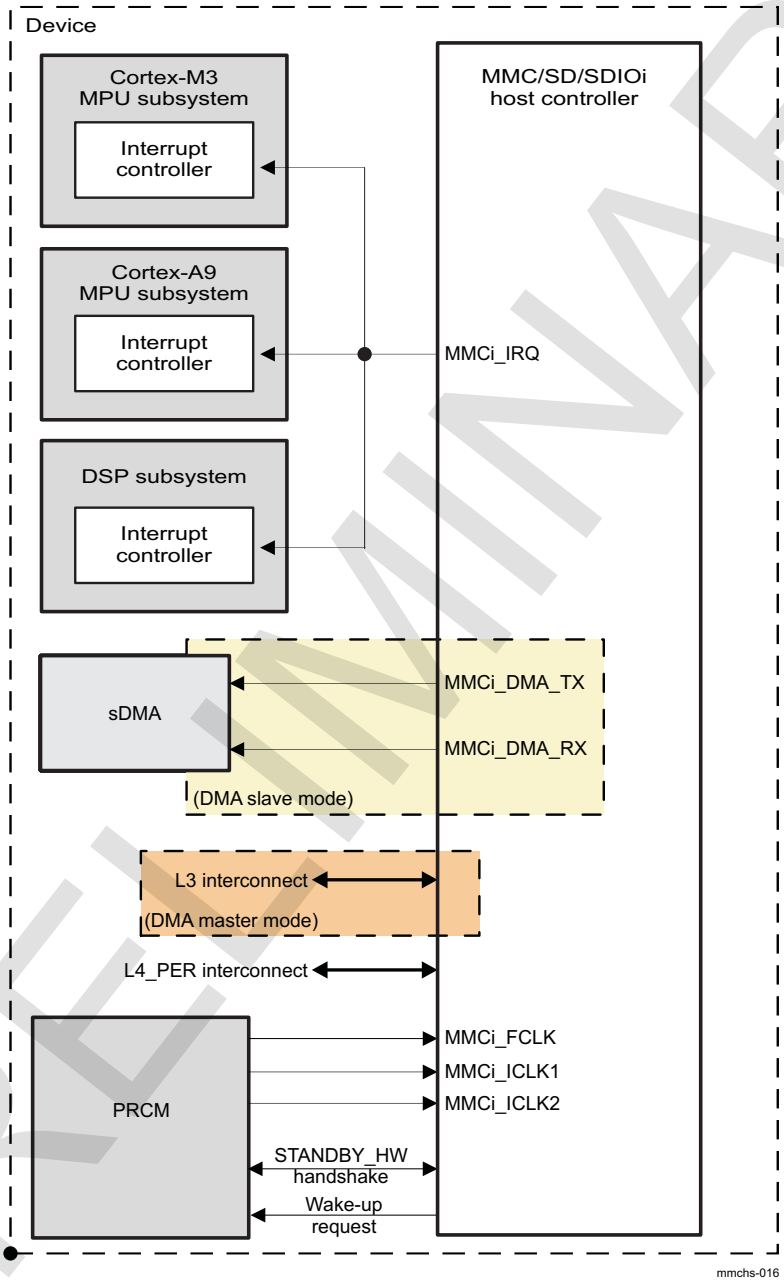
24.3 MMC/SD/SDIO Integration

This section describes module integration in the device, including information about clocks, resets, and hardware requests.

Figure 24-16 shows the MMC/SD/SDIO integration.

Figure 24-16. MMC/SD/SDIO Controllers Integration



NOTE: For more information about the IDLE hardware handshake and the wake-up request, see Section 3.1.1.1.2, *Module-Level Clock Management*, in Chapter 3, *Power, Reset, and Clock Management*.

Table 24-5 through Table 24-7 summarize the integration of the module in the device.

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Table 24-5. Integration Attributes

Module Instance	Attributes	
	Power Domain	Interconnect
HSMMC1	PD_L3_INIT	L3 L4_PER
HSMMC2	PD_L3_INIT	L3 L4_PER
HSMMC3	PD_L4_PER	L4_PER
HSMMC4	PD_L4_PER	L4_PER
HSMMC5	PD_L4_PER	L4_PER

Table 24-6. Clocks and Resets

Clocks				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
HSMMC1	MMC1_FCLK	MMC1_FCLK	PRCM	MMC1 function clock
	MMC1_ICLK2	INIT_L4_ICLK	PRCM	MMC1 interface clock
	MMC1_ICLK1	INIT_L3_ICLK	PRCM	MMC1 interface clock
HSMMC2	MMC2_FCLK	MMC2_FCLK	PRCM	MMC2 function clock
	MMC2_ICLK2	INIT_L4_ICLK	PRCM	MMC2 interface clock
	MMC2_ICLK1	INIT_L3_ICLK	PRCM	MMC2 interface clock
HSMMC3	MMC3_ICLK	PER_L4_ICLK	PRCM	MMC3 interface clock
	MMC3_FCLK	PER_48M_FCLK	PRCM	MMC3 function clock
HSMMC4	MMC4_ICLK	PER_L4_ICLK	PRCM	MMC4 interface clock
	MMC4_FCLK	PER_48M_FCLK	PRCM	MMC4 function clock
HSMMC5	MMC5_ICLK	PER_L4_ICLK	PRCM	MMC5 interface clock
	MMC5_FCLK	PER_48M_FCLK	PRCM	MMC5 function clock
Resets				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
HSMMC1	MMC1_RST	L3_INIT_RET_RST	PRCM	L3 reset to MMC1
HSMMC2	MMC2_RST	L3_INIT_RET_RST	PRCM	L3 reset to MMC2
HSMMC3	MMC3_RST	L4_PER_RST	PRCM	L4 reset to MMC3
HSMMC4	MMC4_RST	L4_PER_RST	PRCM	L4 reset to MMC4
HSMMC5	MMC5_RST	L4_PER_RST	PRCM	L4 reset to MMC5

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Table 24-7. Hardware Requests

Interrupt Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
HSMMC1	MMC1_IRQ	MM_IRQ_50	Cortex-M3 INTC	MMC1 interrupt to Cortex-M3
	MMC1_IRQ	D_IRQ_16	DSP INTC	MMC1 interrupt to DSP
	MMC1_IRQ	MA_IRQ_83	Cortex-A9 INTC	MMC1 interrupt to Cortex-A9
HSMMC2	MMC2_IRQ	MM_IRQ_51	Cortex-M3 INTC	MMC2 interrupt to Cortex-M3
	MMC2_IRQ	D_IRQ_17	DSP INTC	MMC2 interrupt to DSP
	MMC2_IRQ	MA_IRQ_86	Cortex-A9 INTC	MMC2 interrupt to Cortex-A9
HSMMC3	MMC3_IRQ	MM_IRQ_52	Cortex-M3 INTC	MMC3 interrupt to Cortex-M3
	MMC3_IRQ	MA_IRQ_94	Cortex-A9 INTC	MMC3 interrupt to Cortex-A9
HSMMC4	MMC4_IRQ	MM_IRQ_53	Cortex-M3 INTC	MMC4 interrupt to Cortex-M3
	MMC4_IRQ	MA_IRQ_96	Cortex-A9 INTC	MMC4 interrupt to Cortex-A9
HSMMC5	MMC5_IRQ	MM_IRQ_54	Cortex-M3 INTC	MMC5 interrupt to Cortex-M3
	MMC5_IRQ	MA_IRQ_59	Cortex-A9 INTC	MMC5 interrupt to Cortex-A9
DMA Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
HSMMC1	MMC1_DMA_TX	S_DMA_60	sDMA	MMC1 DMA TX
	MMC1_DMA_RX	S_DMA_61	sDMA	MMC1 DMA RX
HSMMC2	MMC2_DMA_TX	S_DMA_46	sDMA	MMC2 DMA TX
	MMC2_DMA_RX	S_DMA_47	sDMA	MMC2 DMA RX
HSMMC3	MMC3_DMA_TX	S_DMA_76	sDMA	MMC3 DMA TX
	MMC3_DMA_RX	S_DMA_77	sDMA	MMC3 DMA RX
HSMMC4	MMC4_DMA_TX	S_DMA_56	sDMA	MMC4 DMA TX
	MMC4_DMA_RX	S_DMA_57	sDMA	MMC4 DMA RX
HSMMC5	MMC5_DMA_TX	S_DMA_58	sDMA	MMC5 DMA TX
	MMC5_DMA_RX	S_DMA_59	sDMA	MMC5 DMA RX

NOTE:

- For a description of the interrupt source, see Section 24.4.4, *Interrupt Requests*.
- For a description of the DMA source, see Section 24.4.5, *DMA Modes*.

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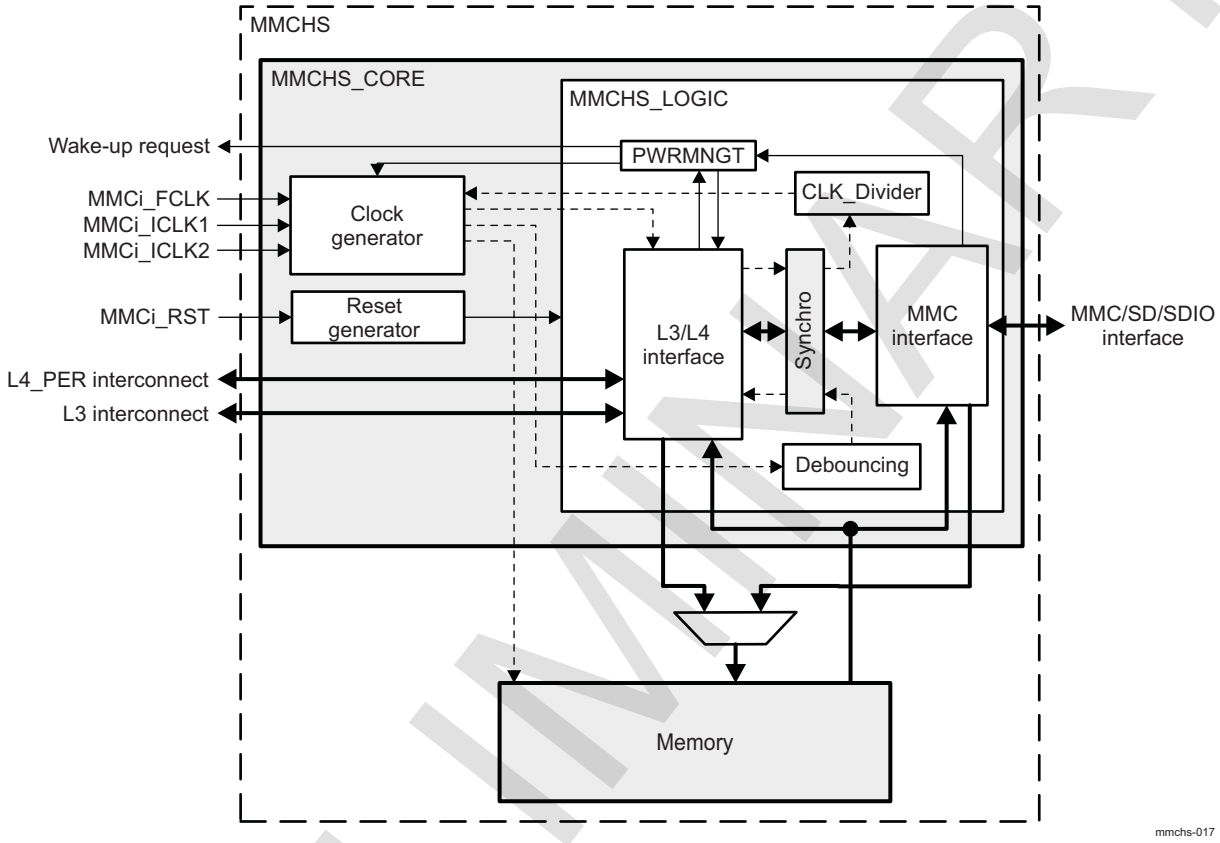
24.4 MMC/SD/SDIO Functional Description

24.4.1 Block Diagram

Figure 24-17 is a block diagram of the MMC/SD/SDIOi host controller.

Figure 24-17. MMC/SD/SDIO Diagram



24.4.2 Resets

24.4.2.1 Hardware Reset

The module is reinitialized by the hardware (see Table 24-6 for more information about reset signals).

The MMCi.MMCHS_SYSSTATUS[0] RESETDONE bit can be monitored by software to check whether the module is ready to use after a hardware reset.

NOTE: The functional clock (MMCi_FCLK) and interface clock (MMCi_ICLK) must be provided to the module to allow the RESETDONE status bit to be set.

The debounce clock (MMCi_32K) must be active to reset the module correctly.

This hardware reset signal has a global reset action on the module. All configuration registers and all state-machines are reset in all clock domains.

24.4.2.2 Software Reset

The module is reinitialized by software through the MMCi.MMCHS_SYSCONFIG[1] SOFTRESET bit. This bit has the same action on the module logic as the hardware signal (MMCi_RST), with the following exceptions:

- Debounce logic

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- MMCi.MMCHS_PSTATE, MMCi.MMCHS_CAPA, and MMCi.MMCHS_CUR_CAPA registers (see the corresponding register description)

The SOFTRESET bit is active high. The bit is automatically reinitialized to 0 by hardware. The MMCi.MMCHS_SYSCTL[24] SRA bit has the same action on the design as the SOFTRESET bit.

The MMCi.MMCHS_SYSSTATUS[0] RESETDONE bit can be monitored by software to check whether the module is ready to use after a software reset.

Moreover, two partial software reset bits are provided:

- MMCi.MMCHS_SYSCTL[26] SRD
- MMCi.MMCHS_SYSCTL[25] SRC

These two reset bits are useful to reinitialize data or command processes, respectively, in case of line conflict. When these bits are set to 1, a reset process is automatically released when the reset completes:

- The MMCi.MMCHS_SYSCTL[26] SRD bit resets all finite state-machines (FSMs) and status management that handle data transfers on the interface and functional sides.
- The MMCi.MMCHS_SYSCTL[25] SRC bit resets all FSMs and status management that handle command transfers on the interface and functional sides.

24.4.3 Power Management

The MMC/SD/SDIO host controller can enter into different modes and save power:

- Normal mode
- Idle mode

The two modes are mutually exclusive (the module can be in normal mode or in idle mode). The MMC/SD/SDIO host controller is compliant with the handshake protocol of the PRCM module.

When the MMC/SD/SDIOi power domain is off, the only way to wake up the power domain and different MMC/SD/SDIOi clocks is to monitor the state of the sdmmci_dat1 input pin through a different GPIO line for each MMC/SD/SDIO interface (for more information, see Section 25.1, *GPIO Overview*, in Chapter 25, *GPIO*).

Normal Mode

The autogating of interface and functional clocks occurs when the following conditions are met:

- The MMCi.MMCHS_SYSCONFIG[0] AUTOIDLE bit is set to 1.
- There is no transaction on the MMC interface.

The autogating of interface and functional clocks stops when the following conditions are met:

- A register access occurs through the L4 interconnect.
- A wake-up event occurs (an interrupt from an SDIO card).
- A transaction on the MMC/SD/SIO interface starts.

Then the MMC/SD/SDIO host controller enters into LOW-POWER state (MMCi_ICLK clock autogated) even if the MMCi.MMCHS_SYSCONFIG[0] AUTOIDLE bit is set to 0.

The functional clock is internally switched off and only interconnect read and write accesses are allowed.

Idle Mode

The MMCi_ICLK and MMCi_FCLK clocks provided to the MMC/SD/SDIO host controller are switched off upon a PRCM module request. They are switched back upon module request.

The MMC/SD/SDIO host controller complies with the handshaking protocol of the PRCM module:

- Idle request from the system power manager
- Idle acknowledgment from the MMC/SD/SDIO host controller
- Wake-up request from the MMC/SD/SDIO host controller

The idle acknowledgment varies according to the MMCi.MMCHS_SYSCONFIG[4:3] SIDLEMODE bit field:

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- 0x0: Force-idle mode. The MMC/SD/SDIO host controller acknowledges the system power manager request unconditionally.
- 0x1: No-idle mode. The MMC/SD/SDIO host controller ignores the system power manager request and behaves normally as if the request was not asserted.
- 0x2: Smart-idle mode. The MMC/SD/SDIO host controller acknowledges the system power manager request according to its internal state.
- 0x3: Smart-idle wake-up-capable mode. The MMC/SD/SDIO host controller acknowledges the system power manager request according to its internal state. However, the module may generate wake-up events when in IDLE state (related to IRQ or DMA requests)

During the smart-idle mode period, the MMC/SD/SDIO host controller acknowledges that the MMCi_ICLK and MMCi_FCLK clocks may be switched off, regardless of the value set in the MMCi.MMCHS_SYSCONFIG[9:8] CLOCKACTIVITY bit field.

Transition From Normal Mode to Smart-Idle Mode

Smart-idle mode is enabled when the MMCi.MMCHS_SYSCONFIG[4:3] SIDLEMODE bit field is set to 0x2 or 0x3.

The MMC/SD/SDIOi host controller goes into idle mode when the PRCM issues an idle request, according to its internal activity.

The MMC/SD/SDIO host controller acknowledges the idle request from the PRCM after ensuring the following:

- The current multi- or single-block transfer is complete.
- Any interrupt or DMA request is asserted.
- There is no card interrupt on the sdmmci_dat1 signal.

As long as the MMC/SD/SDIOi controller does not acknowledge the idle request, if an event occurs, the MMC/SD/SDIOi host controller can still generate an interrupt or a DMA request. In this case, the module ignores the idle request from the PRCM module.

As soon as the MMC/SD/SDIOi contoller acknowledges the idle request from the PRCM module:

- If smart-idle mode: The module does not assert any new interrupt or DMA request.
- If smart-idle wake-up-capable mode: The module may generate wake-up events related to an interrupt or DMA request.

Wake-Up Event in Smart-Idle Mode

The wake-up feature is enabled when the following enable wake-up bits are set:

- The MMCi.MMCHS_SYSCONFIG[2] ENAWAKEUP bit is set to 0x1.
- The MMCi.MMCHS_HCTL[24] IWE bit is set to 0x1.
- The MMCi.MMCHS_IE[8] CIRQ_ENABLE bit is set to 0x1.

The wakeup is generated only in smart-idle mode, when the module is in idle mode.

Table 24-8 lists the supported cases in smart-idle mode.

Table 24-8. Smart-Idle Mode and Wake-Up Capabilities

Mode	MMCi_ICLK Clock	MMCi_FCLK Clock	Wake-Up Event
Card interrupt	May be switched off(1)	May be switched off(1)	The module sends an asynchronous wake-up request when a card interrupt on sdmmci_dat1 signal is detected.

(1) The MMC/SD/SDIOi host controller assumes that both clocks may be switched off, regardless of the value set in the MMCi.MMCHS_SYSCONFIG[9:8] CLOCKACTIVITY bit field.

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Transition From Smart-Idle Mode to Normal Mode

The MMC/SD/SDIO host controller detects the end of the idle period when the PRCM module deasserts the idle request.

For the wake-up event, there is a corresponding interrupt status in the MMCi.MMCHS_STAT register. The MMC/SD/SDIOi host controller operates the conversion between the wake-up and interrupt (or DMA request) upon exit from smart-idle mode, if the associated enable bit is set in the MMCi.MMCHS_ISE register.

Interrupts and wake-up events have independent enable and disable controls, accessible through the MMCi.MMCHS_HCTL and MMCi.MMCHS_ISE registers. The overall consistency must be ensured by software.

The interrupt status register MMCi.MMCHS_STAT is updated in the CIRQ bit with the event that caused the wakeup when the MMCi.MMCHS_IE[8] CIRQ_ENABLE associated bit is enabled.

Then, the wake-up event at the origin of the transition from smart-idle mode to normal mode is converted into its corresponding interrupt or DMA request. (The MMCi.MMCHS_STAT register is updated and the status of the interrupt signal changes.)

When the idle request from the PRCM module is deasserted, the module switches back to normal mode. The module is fully operational.

Force-Idle Mode

Force-idle mode is enabled when the MMCi.MMCHS_SYSCONFIG[4:3] SIDLEMODE bit field is set to 0x0.

Force-idle mode is an idle mode in which the MMC/SD/SDIOi host controller responds unconditionally to the idle request from the PRCM module. Moreover, in this mode, the MMC/SD/SDIOi host controller unconditionally deasserts interrupts and DMA request lines asserted.

The transition from normal mode to force-idle mode does not affect the bits of the MMCi.MMCHS_STAT register.

In force-idle mode, the interrupt and DMA request lines are deasserted. MMCi_ICLK and MMCi_FCLK can be switched off.

CAUTION

In force-idle mode, an idle request from the PRCM module during a command or a data transfer can lead to an unexpected and unpredictable result. When the module is idle, any access to the module generates an error as long as the MMCi_ICLK clock is alive.

The module exits force-idle mode when the PRCM module deasserts the idle request. Then the module switches back to normal mode. The module is fully operational. Interrupt and DMA request lines are optionally asserted one clock cycle later.

Local Power Management

Table 24-9 describes the power-management features available for the MMC/SD/SDIOi modules.

NOTE: For information about source clock gating and a description of the sleep/wake-up transitions, see Section 3.1.1.1, *Clock Management*, in Chapter 3, *Power, Reset, and Clock Management*.

Table 24-9. Local Power-Management Features

Feature	Registers	Description
Clock auto gating	MMCHS_SYSCONFIG[0] AUTOIDLE	This bit allows a local power optimization inside the module by gating the MMCi_ICLK clock upon the interface activity, or gating the MMCi_FCLK clock upon the internal activity.

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Table 24-9. Local Power-Management Features (continued)

Feature	Registers	Description
Slave idle modes	MMCHS_SYSCONFIG[3:4] SIDLEMODE	Force-idle, no-idle, and smart-idle modes are available.
Clock activity	MMCHS_SYSCONFIG[8:9] CLOCKACTIVITY	For configuration details, see Table 24-10.
Master standby modes	MMCHS_SYSCONFIG[12:13] STANDBYMODE	Force-idle, no-idle, and smart-idle modes are available.
Global wake-up enable	MMCHS_SYSCONFIG[2] ENAWAKEUP	This bit enables the wake-up feature at the module level.
Wake-up sources enable	MMCHS_HCTL register	This register holds one active-high enable bit per event source that is able to generate a wake-up signal.

Table 24-10. Clock Activity Settings

CLOCKACTIVITY Values	Clock State When Module is in IDLE State		Features Available When Module is in IDLE State	Wake-Up Events
	MMCi_ICLK	MMCi_ FCLK		
00	OFF	OFF	None	Card interrupt
10	OFF	ON	None	
01	ON	OFF	None	
11	ON	ON	All	

CAUTION

The PRCM module has no hardware means of reading CLOCKACTIVITY settings. Thus, software must ensure consistent programming between the CLOCKACTIVITY and MMCi clock PRCM control bits. For a description of the ClockActivity feature, see Section 3.1.1.1.2, *Module-Level Clock Management*, in Chapter 3, *Power, Reset, and Clock Management*.

24.4.4 Interrupt Requests

Several internal module events can generate an interrupt. Each interrupt has a status bit, an interrupt enable bit, and a signal status enable:

- The status of each type of interrupt is automatically updated in the MMCi.MMCHS_STAT register; it indicates which service is required.
- The interrupt status enable bits of the MMCi.MMCHS_IE register enable or disable the automatic update of the MMCi.MMCHS_STAT register on an event-by-event basis.
- The interrupt signal enable bits of the MMCi.MMCHS_ISE register enable or disable the transmission of an interrupt request on the interrupt line MMCi_IRQ (from the MMC/SD/SDIOi host controller to the MPU subsystem INTC) on an event-by-event basis.

If an interrupt status is disabled in the MMCi.MMCHS_IE register, then the corresponding interrupt request is not transmitted, and the value of the corresponding interrupt signal enable in the MMCi.MMCHS_ISE register is ignored.

When an interrupt event occurs, the corresponding status bit is automatically set to 0x1 (the MMC/SD/SDIOi host controller updates the status bit) in the MMCi.MMCHS_STAT register. If a mask is later applied on the interrupt in the MMCi.MMCHS_ISE register, the interrupt request is deactivated.

When the interrupt source has not been serviced, if the interrupt status is cleared in the MMCi.MMCHS_STAT register and the corresponding mask is removed from the MMCi.MMCHS_ISE register, the interrupt status is not asserted again in the MMCi.MMCHS_STAT register and the MMC/SD/SDIOi host controller does not transmit an interrupt request.

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CAUTION

If the buffer write ready (BWR) interrupt or the buffer read ready (BRR) only interrupt are not serviced and are cleared in the MMCi.MMCHS_STAT register, and the corresponding mask is removed, then the MMC/SD/SDIOi host controller waits for the service of the interrupt without updating the status MMCi.MMCHS_STAT register or transmitting an interrupt request.

Table 24-11 lists the event flags, and their mask, that can cause module interrupts.

Table 24-11. Events

Event Flag	Event Mask	Map to	Description
MMCHS_STAT[29] BADA	MMCHS_IE[29] BADA_ENABLE	MMCi_IRQ	Bad access to data space. This bit is set automatically to indicate a bad access to buffer when not allowed: This bit is set during a read access to the data register (MMCHS_DATA) while buffer reads are not allowed (MMCHS_PSTATE[11] BRE = 0). This bit is set during a write access to the data register (MMCHS_DATA) while buffer writes are not allowed (MMCHS_STATE[10] BWE = 0).
MMCHS_STAT[28] CERR	MMCHS_IE[28] CERR_ENABLE	MMCi_IRQ	Card error. This bit is set automatically when there is at least one error in a response of type R1, R1b, R6, R5, or R5b. Only bits referenced as type E (error) in the status field in the response can set a card status error. An error bit in the response is flagged only if the corresponding bit in the card status response error MMCHS_CSRE is set. There is no card error detection for the auto CMD12 command.
MMCHS_STAT[25] ADMAE	MMCHS_IE[25] ADMAE_ENABLE	MMCi_IRQ	ADMA error. This bit is set when the host controller detects errors during an ADMA-based data transfer. The state of the ADMA at an error occurrence is saved in the ADMA error status register. In addition, the host controller generates this interrupt when it detects invalid descriptor data (Valid=0) at the ST_FDS state.
MMCHS_STAT[24] ACE	MMCHS_IE[24] ACE_ENABLE	MMCi_IRQ	Auto CMD12 error. This bit is set automatically when one bit in the auto CMD12 error status register changes from 0 to 1.
MMCHS_STAT[22] DEB	MMCHS_IE[22] DEB_ENABLE	MMCi_IRQ	Data end bit error. This bit is set automatically when detecting a 0 at the end bit position of read data on the DAT line or at the end position of the CRC status in write mode.
MMCHS_STAT[21] DCRC	MMCHS_IE[21] DCRC_ENABLE	MMCi_IRQ	Data CRC error. This bit is set automatically when there is a CRC16 error in the data phase response following a block read command or if there is a 3-bit CRC status difference of a position 010 token during a block write command.
MMCHS_STAT[20] DTO	MMCHS_IE[20] DTO_ENABLE	MMCi_IRQ	Data time-out error. This bit is set automatically according to the following conditions: – Busy time-out for R1b, R5b response type – Busy time-out after write CRC status – Write CRC status time-out – Read data time-out
MMCHS_STAT[19] CIE	MMCHS_IE[19] CIE_ENABLE	MMCi_IRQ	Command index error. This bit is set automatically when the response index differs from the corresponding command index previously emitted. The check is enabled through the MMCHS_CMD[20] CICE bit.

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Table 24-11. Events (continued)

Event Flag	Event Mask	Map to	Description
MMCHS_STAT[18] CEB	MMCHS_IE[18] CEB_ENABLE	MMCi_IRQ	Command end bit error. This bit is set automatically when detecting a 0 at the end bit position of a command response.
MMCHS_STAT[17] CCRC	MMCHS_IE[17] CCRC_ENABLE	MMCi_IRQ	Command CRC error. This bit is set automatically when there is a CRC7 error in the command response. CRC check is enabled through the MMCHS_CMD[19] CCCE bit.
MMCHS_STAT[16] CTO	MMCHS_IE[16] CTO_ENABLE	MMCi_IRQ	Command time-out error. This bit is set automatically when no response is received within 64 clock cycles from the end bit of the command. For commands that reply within five clock cycles, the time-out is still detected at 64 clock cycles.
MMCHS_STAT[15] ERRI	MMCHS_IE[15] ERRI_ENABLE	MMCi_IRQ	Error interrupt. If any of the bits in the error interrupt status register (MMCHS_STAT[24:15]) are set, this bit is set to 1.
MMCHS_STAT[10] BSR	MMCHS_IE[10] BSR_ENABLE	MMCi_IRQ	Boot status received interrupt. This bit is set automatically when the MMCHS_CON[18] BOOT_CF0 bit is set to 0x1 or 0x2 and a boot status is received on the dat0 line. This interrupt is useful only for the MMC card.
MMCHS_STAT[8] CIRQ	MMCHS_IE[8] CIRQ_ENABLE	MMCi_IRQ	Card interrupt. This bit is used only for SD, SDIO, and CE-ATA cards. In 1-bit mode, the interrupt source is asynchronous (can be a source of asynchronous wakeup). In 4-bit mode, the interrupt source is sampled during the interrupt cycle. In CE-ATA mode, the interrupt source is detected when the card drives the CMD line to 0 during one cycle after data transmission end.
MMCHS_STAT[5] BRR	MMCHS_IE[5] BRR_ENABLE	MMCi_IRQ	Buffer read ready. This bit is set automatically during a read operation to the card (see class 2 block-oriented read commands) when one block specified by the MMCHS_BLK[10:0] BLEN bit field is completely written in the buffer. It indicates that the memory card has filled out the buffer and that the LH needs to empty the buffer by reading it.
MMCHS_STAT[4] BWR	MMCHS_IE[4] BWR_ENABLE	MMCi_IRQ	Buffer write ready. This bit is set automatically during a write operation to the card (see class 4 block-oriented write command) when the host can write a complete block as specified by the MMCHS_BLK[10:0] BLEN bit field. It indicates that the memory card has emptied one block from the buffer and that the LH can write one block of data into the buffer.
MMCHS_STAT[3] DMA	MMCHS_IE[3] DMA_ENABLE	MMCi_IRQ	DMA interrupt. This status is set when an interrupt is required in the ADMA instruction and after the data transfer completes.
MMCHS_STAT[2] BGE	MMCHS_IE[2] BGE_ENABLE	MMCi_IRQ	Block gap event. When a stop at the block gap is requested (MMCHS_HCTL[16] SBGR), this bit is automatically set when transaction is stopped at the block gap during a read or write operation.
MMCHS_STAT[1] TC	MMCHS_IE[1] TC_ENABLE	MMCi_IRQ	Transfer completed. This bit is always set when a read/write transfer is complete or between two blocks when the transfer is stopped because of a stop at block gap request (MMCHS_HCTL[16] SBGR). – In read mode: This bit is automatically set on completion of a read transfer (MMCHS_PSTATE[9] RTA).

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Table 24-11. Events (continued)

Event Flag	Event Mask	Map to	Description
			– In write mode: This bit is automatically set on completion of the DAT line use (MMCHS_PSTATE[2] DLA).
MMCHS_STAT[0] CC	MMCHS_IE[0] CC_ENABLE	MMCi_IRQ	Command complete. This bit is set when a 1-to-0 transition occurs in the register command inhibit (MMCHS_PSTATE[0] CMDI). If the command is a type for which no response is expected, then the command complete interrupt is generated at the end of the command. A command time-out error (MMCHS_STAT[16] CTO) has higher priority than command complete (MMCHS_STAT[0] CC). If a response is expected but none is received, then a command time-out error is detected and signaled, instead of the command complete interrupt.

NOTE: To send an interrupt request to the MMCi_IRQ line, the mask/unmask bit must be set in the MMCi.MMCHS_IE and MMCi.MMCHS_ISE registers.

The MMC/SD/SDIOi host controller supports interrupt-driven operation and polling.

24.4.4.1 Interrupt-Driven Operation

An interrupt enable bit must be set in the MMCi.MMCHS_IE register to enable the module internal source of interrupt.

When an interrupt event occurs, the single interrupt line is asserted and the LH must:

1. Read the MMCi.MMCHS_STAT register to identify which event occurred.
2. Write 1 into the corresponding bit of the MMCi.MMCHS_STAT register to clear the interrupt status and release the interrupt line (if a read is done after this write, this returns 0).

NOTE: In the MMCi.MMCHS_STAT register, the card interrupt (CIRQ) and error interrupt (ERRI) bits cannot be cleared.

The MMCi.MMCHS_STAT[8] CIRQ status bit must be masked by disabling the MMCi.MMCHS_IE[8] CIRQ_ENABLE bit (set to 0x0), and then the interrupt routine must clear the SDIO interrupt source in the SDIO card common control register (CCCR).

The MMCi.MMCHS_STAT[15] ERRI bit is automatically cleared when all status bits in the MMCi.MMCHS_STAT[31:16] bit field are cleared.

24.4.4.2 Polling

When the interrupt capability of an event is disabled in the MMCi.MMCHS_ISE register, the interrupt line is not asserted:

- Software can poll the status bit in the MMCi.MMCHS_STAT register to detect when the corresponding event occurs.
- Writing 1 into the corresponding bit of the MMCi.MMCHS_STAT register clears the interrupt status and does not affect the interrupt line state.

NOTE: Refer to the previous note concerning clearing of the CIRQ and ERRI bits.

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24.4.5 DMA Modes

Two DMA managements can be used to load data from memory to the internal buffer of the controller (or vice versa). These modes are exclusive and depend on the module integration.

- DMA master mode

  DMA master mode is selected by setting the MMCHS_CON[20] DMA_MNS bit to 1. In this case, the controller has direct access to data using a specific algorithm called ADMA2 (prevents the system from being interrupted). Data are exchanged using the L3 master interface, which supports burst accesses to maximize throughput.

  NOTE: This mode is supported only by modules connected to the L3 interconnect. See Section 24.1, *MMC/SD/SDIO Overview*, for more information and/or check the value of the MMCHS_HL_HWINFO[0] MADMA_EN bit.

  This mode is available for modules MMC1 and MMC2.

- DMA slave mode

  DMA slave mode is selected by setting the MMCHS_CON[20] DMA_MNS bit to 0. In this case, the controller is slave on the DMA transaction managed by two separated requests (MMCi_DMA_TX and MMCi_DMA_RX).

  NOTE: This mode is the only mode supported by modules that are not connected to the L3 interconnect (regardless of the value of the MMCHS_CON[20] DMA_MNS bit). See Section 24.1, *MMC/SD/SDIO Overview*, for more information and/or to check the value of the MMCHS_HL_HWINFO[0] MADMA_EN bit.

  This mode is available for all MMC modules.

24.4.5.1 Master DMA Operations

The MMC/SD/SDIOi host controller has direct access to the internal data. This feature is called advanced DMA (ADMA). It follows a specific algorithm (ADMA2) defined by an instruction in memory that starts at an address previously loaded in the MMCHS_ADMASAL register before any data command issued to the MMC card. Only 32-bit address spacing is supported by the controller for data storage.

NOTE: This mode is supported only by modules connected to the L3 interconnect. See Section 24.1, *MMC/SD/SDIO Overview*, for more information and/or to check the value of the MMCHS_HL_HWINFO[0] MADMA_EN bit.

These instructions must be loaded by software in a 32-bit-addressed descriptor table in system memory, as shown in Figure 24-18. In this case the MMCHS_ADMASAL register is used as the program address pointer

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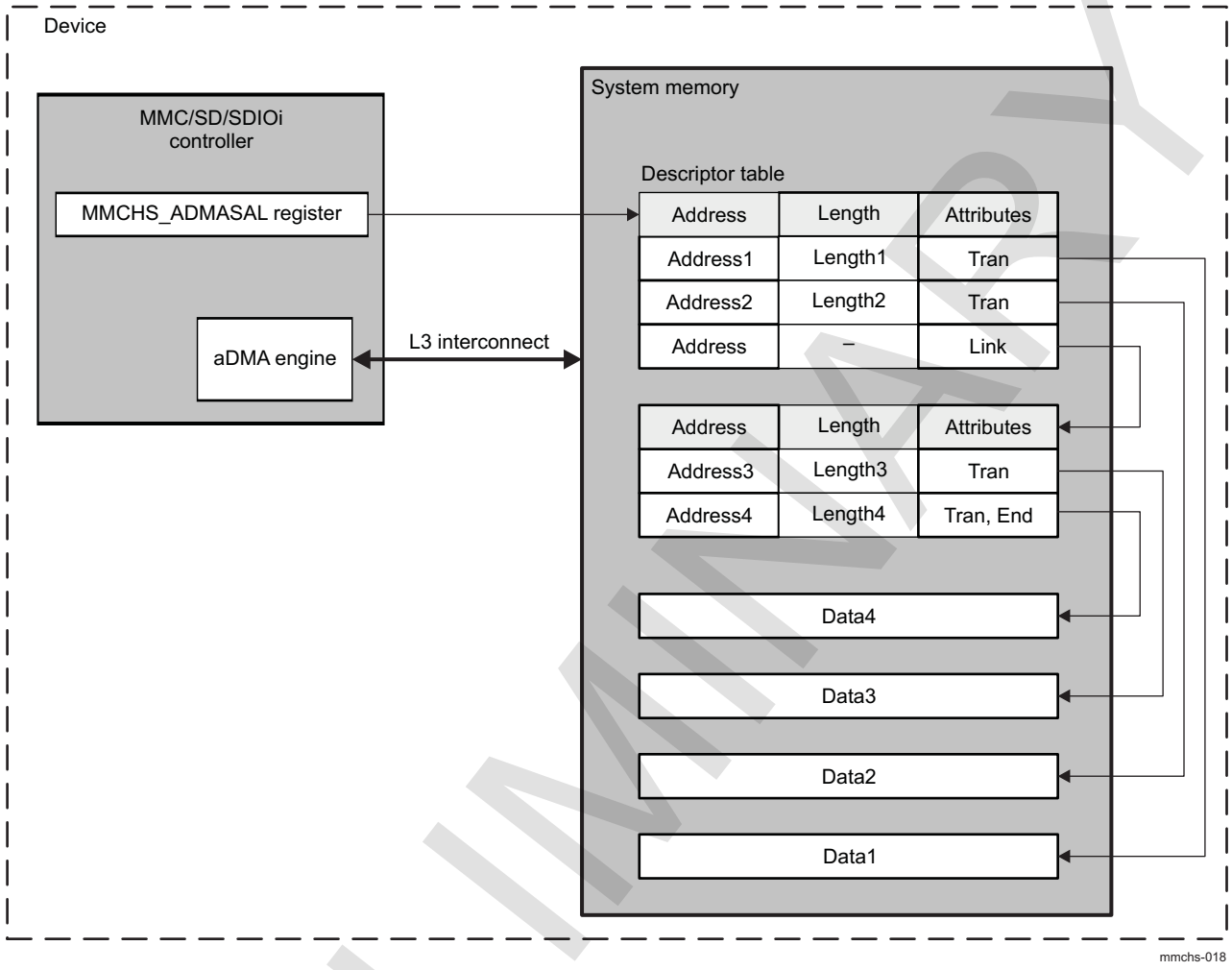
Figure 24-18. ADMA Block Diagram Overview



24.4.5.1.1 Descriptor Table Description

Each descriptor line contains an address, a length, and attributes fields. The attributes define which operation will be processed. Every descriptor line is a 64-bit-wide register that is fetched in the controller using the L3 master interface, and requires two 32-bit accesses to memory.

Table 24-12 shows the structure of a descriptor line.

Table 24-12. Descriptor Line Overview

Address Field		Length		Reserved		Attributes					
63	32	31	16	15	6	5	4	3	2	1	0
32-bit Address		16-bit Length		0x0		Act2	Act1	0	Int	Ent	Valid

The attribute of the descriptor line is divided into two parts:

- Attributes[5:4]: The action to be processed by the ADMA engine
- Attributes[3:0]: Additional parameters characterizing the behavior of the ADMA engine

Table 24-13 describes the available actions of a descriptor line.

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Table 24-13. Available Actions of a Descriptor Line

Act2	Act1	Symbol	Comment	Operation
0	0	Nop	No operation	Do not execute the current line and go to the next line.
0	1	Rsv	Reserved	Reserved action. Behaves the same as the Nop command.
1	0	Tran	Transfer data	Transfer data of one descriptor line.
1	1	Link	Link descriptor	Link to another descriptor.

Table 24-14 describes the additional parameters of a descriptor line.

Table 24-14. Additional Parameters of a Descriptor Line

Bit	Description
Valid	Valid = 1 indicates that this descriptor line is effective. If Valid = 0, an ADMA error interrupt is generated and the ADMA is stopped. This prevents runaways.
End	End = 1 indicates the end of a descriptor. The transfer-complete interrupt is generated when the operation of the descriptor line is complete.
Int	Int = 1 generates a DMA interrupt when the operation of the descriptor line is complete.

24.4.5.1.2 Requirements for Descriptors

The following sections discuss restrictions and tips on how to correctly configure the descriptors to be used by the ADMA engine.

24.4.5.1.2.1 Data Length

There are three requirements to program descriptors:

- The minimum unit of address is 4 bytes.
- The maximum data length of each descriptor line is less than 64KB.
- Total length = $Length_1$ + $Length_2$+ $Length_3$ + ... + $Length_n$ must be a multiple of the block size.

If the total length of a descriptor is not a multiple of the block size, data transfer with the ADMA engine may not have been terminated. In this case, the controller returns a data time-out event and the transfer is aborted.

The block count register (the MMCHS_BLK[31:16] NBLK bit field) is defined as 16 bits and limits data transfers to a maximum of 65,535 blocks. If the ADMA data transfer size is less than or equal to the 65,535-block transfer, the block count register can be used. In this case, the total length of the descriptor table must be equivalent to "block size" by "block count." If the ADMA data transfer is greater than 65,535 blocks, the block count register must be disabled by setting the block count enable bit (the MMCHS_CMD[1] BCE bit) to 0. In this case, the length of the data transfer is not designated by the block count but by the descriptor table.

NOTE: The timing for detecting the last block on the SD bus may differ, which affects control of the read transfer active (MMCHS_PSTATE[9] RTA), write transfer active (MMCHS_PSTATE[8] WTA), and DAT line active (MMCHS_PSTATE[2] DLA) bits. In case of a read operation, more blocks than required may be read from the card. The host driver must ignore an out-of-range error if the read operation is for the last block of the memory area.

24.4.5.1.2.2 Supported Features

The ADMA engine does not support the suspend/resume function. However, the stop and continue functions are available.

When the stop-at-block-gap-request (the MMCHS_HCTL[16] SBGR bit) is set during the ADMA operation, the block gap event interrupt is generated when the ADMA is stopped at block gap (the MMCHS_STAT[2] BGE bit). The host controller must stop the ADMA read operation by using read wait or by stopping the SD clock. While stopping ADMA, SD commands cannot be issued.

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24.4.5.1.2.3 Error Generation

When an error occurs during an ADMA transfer, the ADMA operation is stopped and the ADMA error interrupt is generated. The ADMA error state field (the MMCHS_ADMAES[1:0] AES bit field) holds the state of the ADMA when it is stopped. Software can identify the erroneous descriptor line by using the following method:

- If ADMA stopped at ST_FDS state, the ADMA system address register (MMCHS_ADMASAL) points to the erroneous descriptor line.
- If ADMA stopped at ST_TFR or ST_STOP state, the ADMA system address register points to the descriptor line following the erroneous one.

24.4.5.1.3 Advanced DMA Description

The ADMA is a DMA controller embedded in each eMMC controller. It can be seen as a small sequencer that fetches a descriptor line and executes the corresponding action. The base address of the descriptor table is stored in the MMCHS_ADMASAL register.

NOTE: Software must write the base address of the descriptor table in the MMCHS_ADMASAL register before the first use of the ADMA engine.

The ADMA program is executed according to descriptor attributes (see Section 24.4.5.1.1, *Descriptor Table Description*) and an FSM, as shown in Figure 24-19.

Figure 24-19. ADMA Finite State-Machine

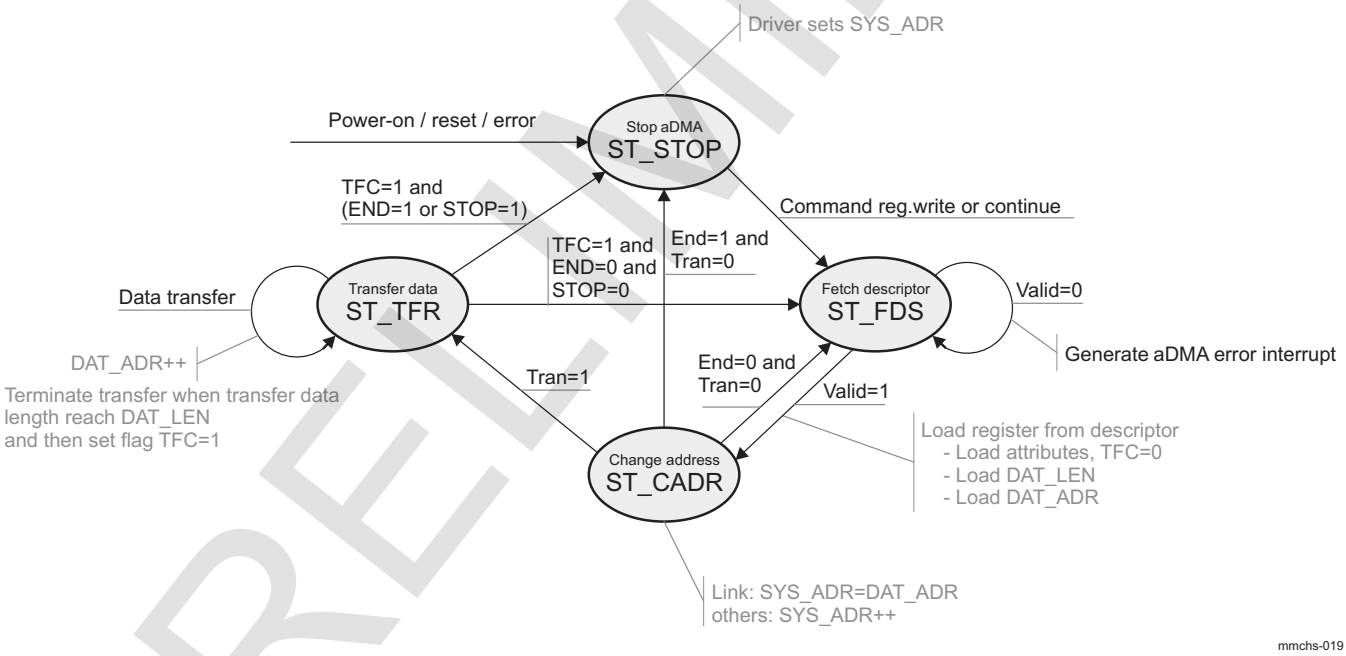

Table 24-15 describes each state of the ADMA FSM.

Table 24-15. ADMA2 States Description

State Name	Operation
ST_FDS (fetch descriptor)	ADMA2 fetches a descriptor line and sets parameters in internal registers. It then goes to the ST_CADR state.
ST_CADR (change address)	Link operation loads another descriptor address to the ADMA system address register (MMCHS_ADMASAL). In other operations, the ADMA system address register is incremented to point to the next descriptor line. If End = 0, go to ST_FDS state. **NOTE**: ADMA2 does not stop at this state if some errors occur.

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Table 24-15. ADMA2 States Description (continued)

State Name	Operation
ST_TFR (transfer data)	Data transfer of one descriptor line is executed between system memory and the SD card: • If data transfer continues (End = 0) go to ST_FDS state. • If data transfer completes, go to ST_STOP state.
ST_STOP (stop DMA)	ADMA2 stays in this state in the following cases: • After power on reset (POR) or software reset • All descriptor data transfers are complete. If a new ADMA operation is stated by writing the command register, go to ST_FDS state.

Table 24-16 gives the description of each symbol used in the ADMA FSM state-machine (see Figure 24-19).

Table 24-16. ADMA FSM Symbol Definition

Symbol	Definition
SYS_ADR	ADMA system address register
SYS_ADR++	Point to next descriptor line
DAT_ADR	Data address register (internal)
DAT_LEN	Data length register (internal)
TFC	Transfer complete flag (internal)
STOP	Stop-at-block-gap request

24.4.5.2 Slave DMA Operations

The MMC/SD/SDIOi host controller can be interfaced with a DMA controller. At the system level, the advantage is to discharge the LH of the data transfers. The module does not support wide DMA access (above 1024 bytes) for SD cards, as specified in the *SD Card Specification* and *SD Host Controller Standard Specification*.

NOTE: This mode is implied by modules that are not connected to the L3 interconnect (regardless of the value of the MMCHS_CON[20] DMA_MNS bit). See Section 24.4.5.1, *Master DMA Operations*, for more information and/or to check the value of the MMCHS_HL_HWINFO[0] MADMA_EN bit.

The DMA request is issued if the following conditions are met:

- The MMCi.MMCHS_CMD[0] DE bit is set to 1 to trigger the initial DMA request (the write must be done when running the data transfer command).
- A command was emitted on the sdmmci_cmd line.
- There is enough space in the buffer of the MMC/SD/SDIOi host controller to write an entire block (BLEN writes).

24.4.5.2.1 DMA Receive Mode

In a DMA block read operation (single or multiple), the request signal MMCi_DMA_RX is asserted to its active level when a complete block is written in the buffer. The block size transfer is specified in the MMCi.MMCHS_BLK[10:0] BLEN bit field.

MMCi_DMA_RX is deasserted to its inactive level when the sDMA reads one word from the buffer.

Only one request is sent per block; the DMA controller can make a 1-shot read access or several DMA bursts, in which case the DMA controller must manage the number of burst accesses, according to the BLEN field block size.

New DMA requests are internally masked if the sDMA has not read exactly BLEN bytes and a new complete block is not ready. Because DMA accesses are 32-bit accesses, the number of sDMA read is Integer(BLEN/4) + 1.

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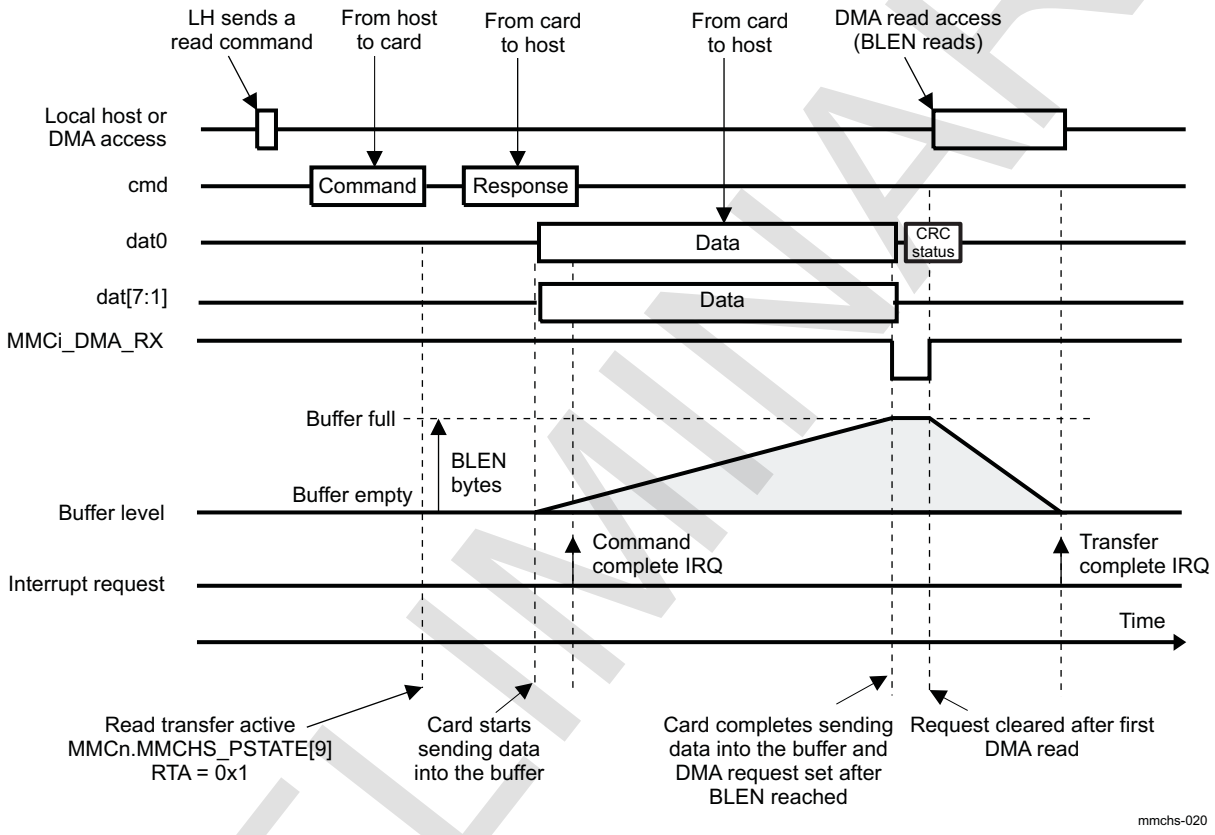
The receive buffer never overflows. In multiple block transfers for block sizes larger than 512 bytes, when the buffer becomes full, the sdmmci_clk clock signal (provided to the card) is momentarily stopped until the sDMA or the MPU performs a read access, which reads a complete block in the buffer.

To summarize:

- DMA transfer size = BLEN buffer size in one shot or by burst
- One DMA request per block

Figure 24-20 shows DMA receive mode.

Figure 24-20. DMA Receive Mode



24.4.5.2.2 DMA Transmit Mode

In a DMA block write operation (single or multiple), the request signal MMCi_DMA_TX is asserted to its active level when a complete block is to be written to the buffer. The block size transfer is specified in the MMCi.MMCHS_BLK[10:0] BLEN bit field.

MMCi_DMA_TX is deasserted to its inactive level when the sDMA writes one word to the buffer.

Only one request is sent per block; the DMA controller can make a 1-shot write access or multiple write DMA bursts, in which case the DMA controller must manage the number of burst accesses, according to the BLEN field block size.

New DMA requests are internally masked if the sDMA has not written exactly BLEN bytes (because DMA accesses are 32-bit accesses, the number of sDMA reads is Integer(BLEN/4) + 1) and if there is not enough memory space to write a complete block in the buffer.

To summarize:

- DMA transfer size = BLEN buffer size in one shot or by burst
- One DMA request per block

Figure 24-21 shows DMA transmit mode.

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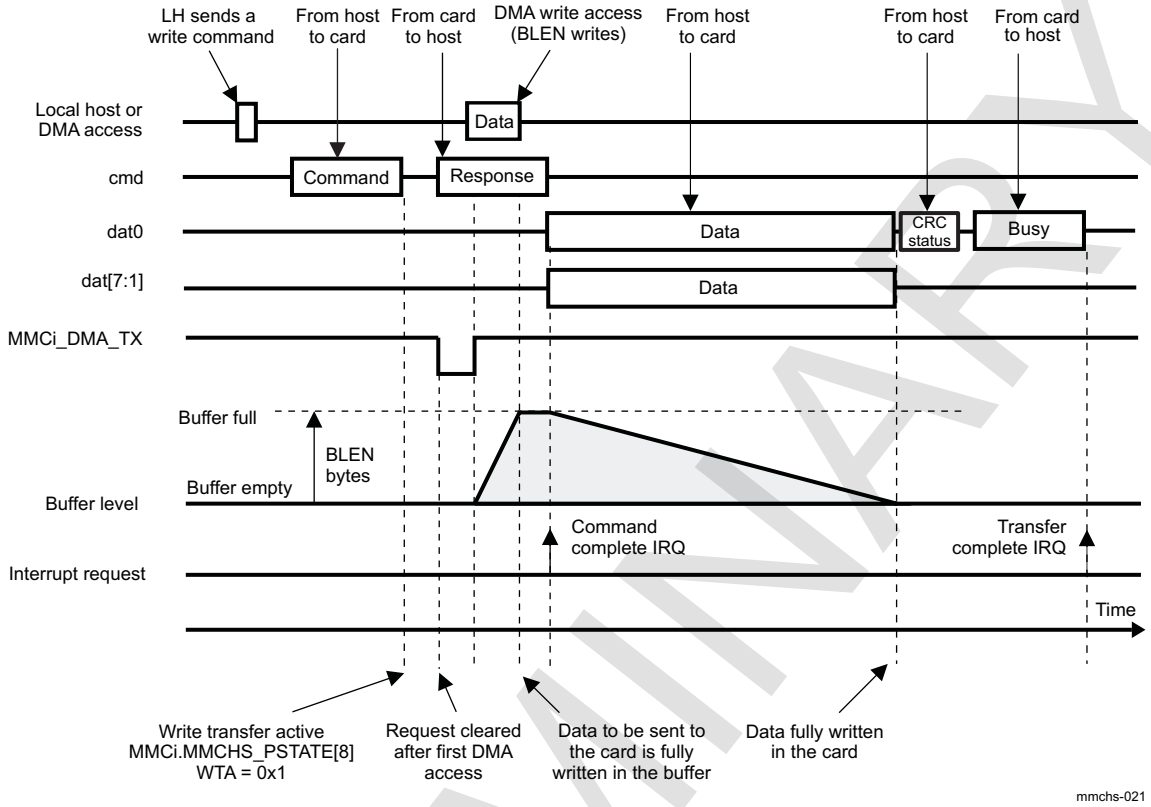
Figure 24-21. DMA Transmit Mode



24.4.6 Mode Selection

The MMC/SD/SDIO host controller can be used in two modes: MMC and SD/SDIO. It has been designed to be the most transparent with the type of card.

The type of the card connected is differentiated by the software initialization procedure. Software identifies the type of card connected during software initialization. For each card type, there are corresponding commands. Some commands are not supported by all cards. For more information, see the *Multimedia Card System Specification*, *SD Memory Card Specifications*, and *SDIO Card Specification, Part E1*.

The purpose of the module is to transfer commands and data to whatever card is connected, respecting the protocol of the connected card.

Writes and reads to the card must respect the appropriate protocol of that card.

24.4.7 Buffer Management

24.4.7.1 Data Buffer

The MMC/SD/SDIOi host controller uses a data buffer. This buffer transfers data from one data bus (interconnect) to another data bus (SD/SDIO or MMC card bus) and vice versa.

The buffer is the heart of the interface and ensures the transfer between the two interfaces (interconnect and the card).

To enhance performance, the data buffer is completed by a prefetch register and a post-write buffer that are not accessible by the host controller.

The read access time of the prefetch register is faster than that of the data buffer. The prefetch register allows data to be read from the data buffer at an increased speed by preloading data into the prefetch register.

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The entry point of the data buffer, prefetch buffer, and post-write buffer is the 32-bit register MMCi.MMCHS_DATA register. A write access to the MMCi.MMCHS_DATA register followed by a read access from the MMCi.MMCHS_DATA register corresponds to a write access to the post-write buffer followed by a read access to the prefetch buffer. As a consequence, it is normal that the data of the write access to the MMCi.MMCHS_DATA register and the data of the read access to the MMCi.MMCHS_DATA register are different.

The number of 32-bit accesses to the MMCi.MMCHS_DATA register that are needed to read (or write) a data block with a size of the MMCi.MMCHS_BLK[10:0] BLEN bit field equals the rounded up result of BLEN divided by 4.

The maximum block size supported by the host controller is hard-coded in the MMCi.MMCHS_CAPA[17:16] MBL bit field and cannot be changed.

A read access to the MMCi.MMCHS_DATA register is allowed only when the buffer read-enable status is set to 1 (the MMCi.MMCHS_PSTATE[11] BRE bit); otherwise, a bad access (the MMCi.MMCHS_STAT[29] BADA bit) is signaled.

A write access to the MMCi.MMCHS_DATA register is allowed only when the buffer write-enable status is set to 1 (the MMCi.MMCHS_PSTATE[10] BWE bit); otherwise, a bad access (the MMCi.MMCHS_STAT[29] BADA bit) is signaled and the data are not written.

The data buffer has two modes of operation to store and read of the first and second portions of the data buffer:

- When the size of the data block to transfer is less than or equal to MEM_SIZE/2 (in double-buffering), two data transfers can occur at the same time from one data bus to the other data bus, and vice versa. The MMC/SD/SDIOi host controller uses the two portions of the data buffer in a ping-pong manner so that storing and reading the first and second portions of the data buffer are automatically interchanged from time to time so that data may be read from one portion (for instance, through a DMA read access on the interconnect bus) while data (for instance, from the card) are being stored into the other portion, and vice versa. When BLEN is less than or equal to 0x200 (that is, less than or equal to 512 bytes), each of the two portions of the buffer that can be used have a size of BLEN (that is, 32 bits × BLEN divided by 4). No more than this total size of 2 × 32 bits × BLEN divided by 4 can be used.

CAUTION

The MMCi.MMCHS_CMD[4] DDIR bit must be configured before a transfer to indicate the direction of the transfer.

Figure 24-22 and Figure 24-23 show the buffer management for a write and for a read, respectively.

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Figure 24-22. Buffer Management for a Write

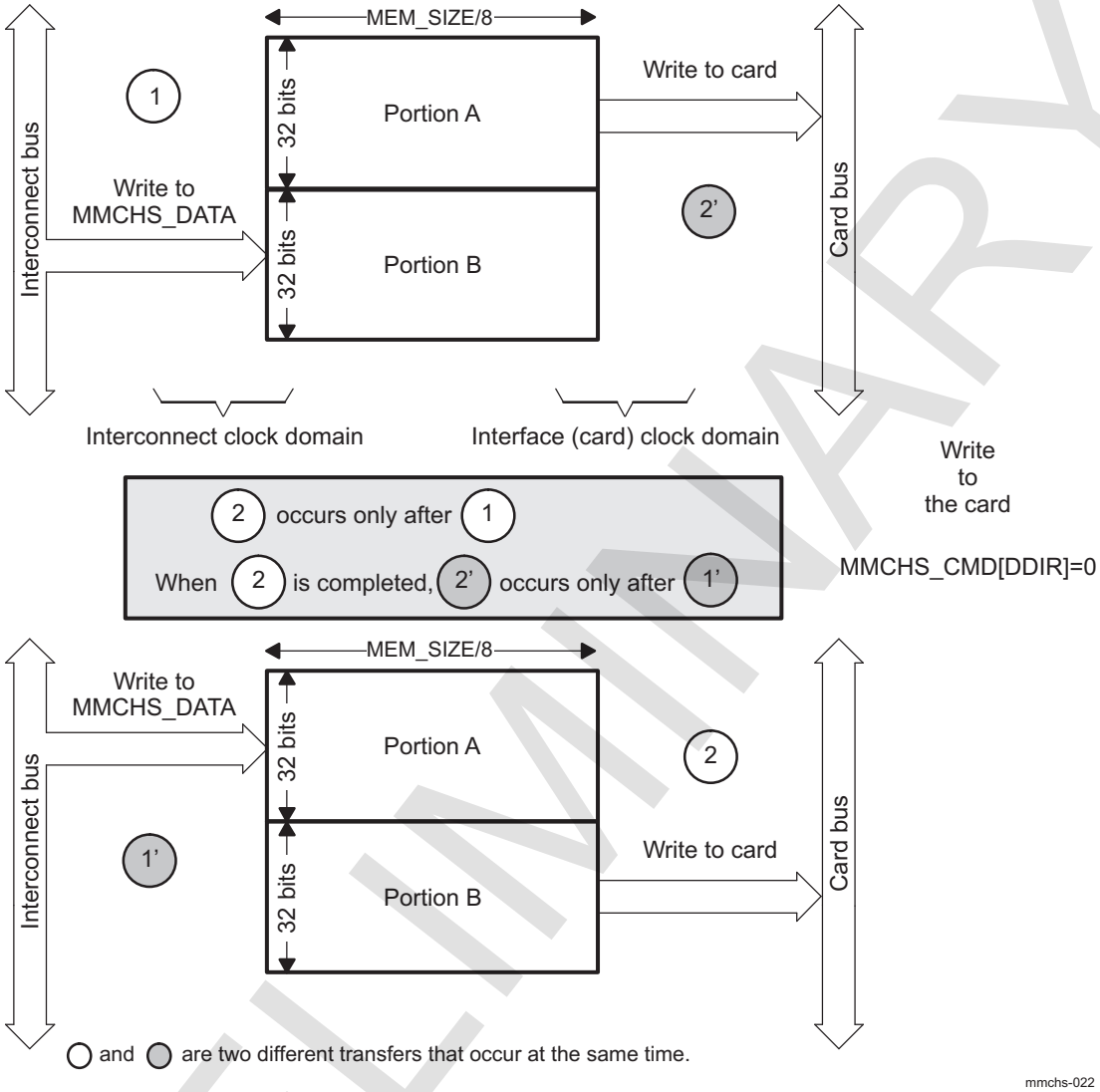

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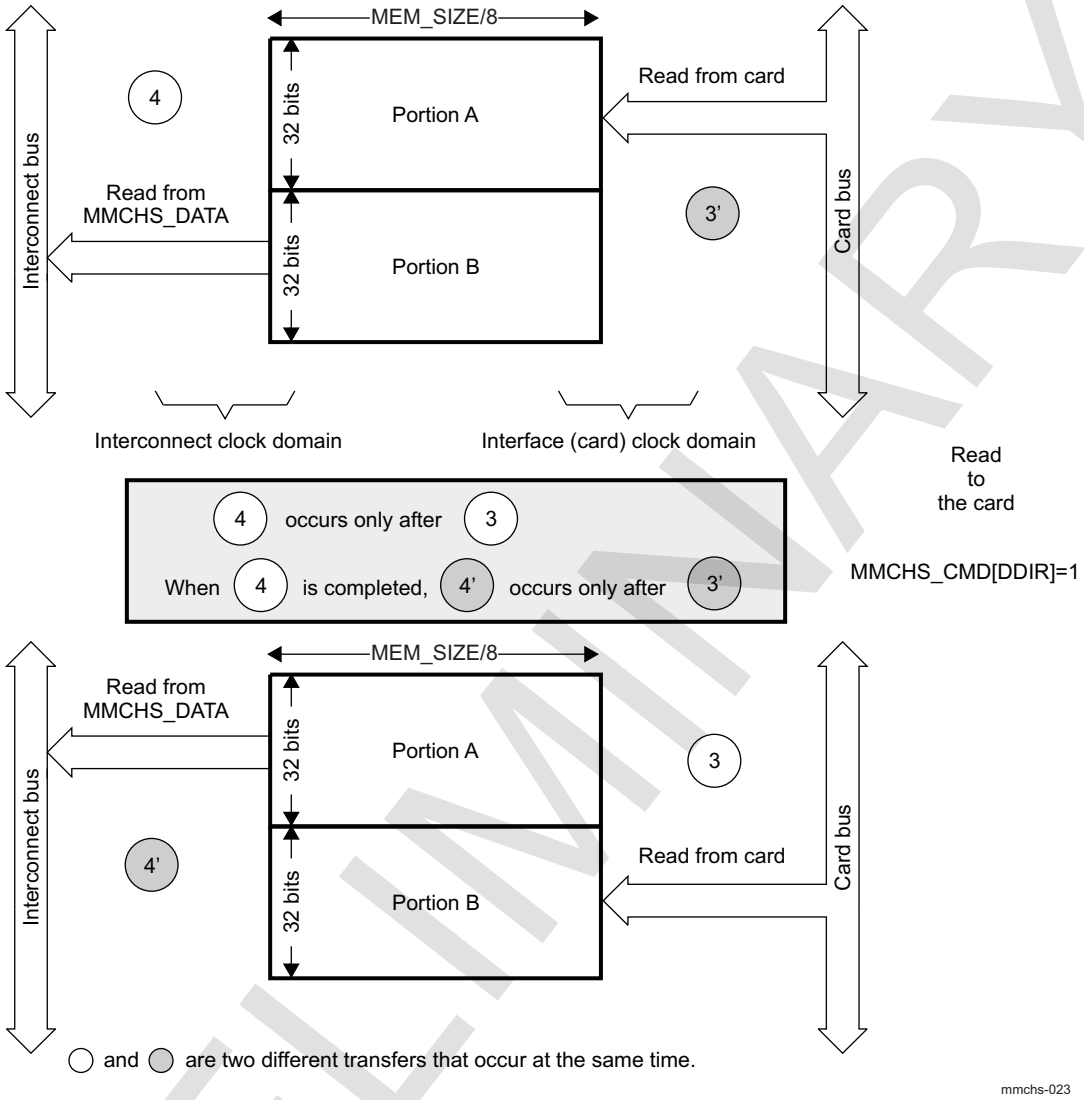
Figure 24-23. Buffer Management for a Read



- When the size of the data block to transfer is larger than MEM_SIZE/2, only one data transfer can occur at a time from one data bus to the other data bus. The MMC/SD/SDIOi host controller uses the entire data buffer as a single portion.

  In this mode, a bad access (the MMCi.MMCHS_STAT[29] BADA bit) is signaled when two data transfers occur at the same time from one data bus to the other data bus, and vice versa.

24.4.7.1.1 Memory Size, Block Length, and Buffer-Management Relationship

The maximum block length and buffer management that can be targeted by the system depend on the memory depth setting (see Table 24-17).

NOTE: Double-buffering is always the buffer management for larger memory depth.

Table 24-17. Memory Size, BLEN, and Buffer Relationship

Memory Size (MMCHS_HL_HWINFO[5:2] MEM_SIZE in bytes)	**512**	**1024**
Maximum block length supported	512	1024

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Table 24-17. Memory Size, BLEN, and Buffer Relationship (continued)

Memory Size (MMCHS_HL_HWINFO[5:2] MEM_SIZE in bytes)	512	1024
Double-buffering for maximum block length	N/A	BLEN=512
Single-buffering for block length	BLEN=512	512BLEN=1024

NOTE: For single-buffering management, throughput on the MMC bus interface deteriorates in multiblock transfers, because the controller must wait for the filling or emptying of the buffer between each block transfer on the MMC bus. The clock is maintained on write MMC transfers (the MMCHS_CMD[3] DDIR bit is 0) and halted on read MMC transfers (the MMCHS_CMD[3] DDIR bit is 1).

24.4.7.1.2 Data Buffer Status

The data buffer status is defined in the following interrupt status register and status register:

- Interrupt status registers:
  - MMCi.MMCHS_STAT[29] BADA: Bad access to data space
  - MMCi.MMCHS_STAT[5] BRR: Buffer read ready
  - MMCi.MMCHS_STAT[4] BWR: Buffer write ready
- Status registers:
  - MMCi.MMCHS_PSTATE[11] BRE: Buffer read enable
  - MMCi.MMCHS_PSTATE[10] BWE: Buffer write enable

24.4.8 Transfer Process

The process of a transfer depends on the type of command. It can be with or without a response, and with or without data.

24.4.8.1 Different Types of Commands

Different types of commands are specific to the MMC, SD, and SDIO cards. For more information, see the *Multimedia Card System Specification*, *SD Memory Card Specifications*, *SDIO Card Specification, Part E1*, or *SD Card Specification, Part A2, SD Host Controller Standard Specification*.

24.4.8.2 Different Types of Responses

Different types of responses are specific to the MMC, SD, and SDIO cards. For more information, see the *Multimedia Card System Specification*, *SD Memory Card Specifications*, *SDIO Card Specification, Part E1*, or the *SD Card Specification, Part A2, SD Host Controller Standard Specification*.

Table 24-18 describes how the MMC, SD, and SDIO responses are stored in the MMCHS_RSPxx registers.

Table 24-18. MMC, SD, SDIO Responses in the MMCHS_RSPxx Registers

Kind of Response	Response Field	Response Register
R1, R1b (normal response), R3, R4, R5, R5b, R6, R7	RESP[39:8](1)	MMCHS_RSP10[31:0]
R1b (Auto CMD12 response)	RESP[39:8](1)	MMCHS_RSP76[31:0]
R2	RESP[127:0](1)	MMCHS_RSP76[31:0] MMCHS_RSP54[31:0] MMCHS_RSP32[31:0] MMCHS_RSP10[31:0]

(1) RESP refers to the command response format described in the specifications mentioned.

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When the host controller modifies part of the MMCHS_RSPxx registers, it preserves the unmodified bits.

The host controller stores the Auto CMD12 response in the MMCHS_RSP76[31:0] register because the host controller may have a multiple block data DAT line transfer executing concurrently with a command. This lets the host controller avoid overwriting the Auto CMD12 response with the command response stored in the MMCHS_RSP10 register, and vice versa.

24.4.9 Transfer or Command Status and Errors Reporting

Flags in the MMC/SD/SDIOi host controller show the status of communication with the card:

- A time-out (of a command, data, or response)
- A CRC error

Error conditions generate interrupts. For more information, see Table 24-19 and the register description.

Table 24-19. CC and TC Values Upon Error Detected

Error Hold in MMCi.MMCHS_STAT		CC	TC	Comments
29	BADA			No dependency with CC or TC BADA is related to the MMCHS_DATA register accesses. Its assertiondoeis not depend on the ongoing transfer.
28	CERR	1		CC is set upon CERR.
22	DEB		1	TC is set upon DEB.
21	DCRC		1	TC is set upon DCRC.
20	DTO			DTO and TC are mutually exclusive. DCRC and DEB cannot occur with DTO.
19	CIE	1		CC is set upon CIE.
18	CEB	1		CC is set upon CEB.
17	CCRC	1		CC can be set upon CCRC. See CTO comment.
16	CTO			CTO and CC are mutually exclusive. CIE, CEB, and CERR cannot occur with CTO. CTO can occur at the same time as CCRC: It indicates a command abort due to contention on the CMD line. In this case no CC appears.

A MMCHS_STAT[21] DCRC event can be asserted in the following conditions:

- Busy time-out for R1b, R5b response type
- Busy time-out after write CRC status
- Write CRC status time-out
- Read data time-out
- Boot acknowledge time-out

24.4.9.1 Busy Time-Out for R1b, R5b Response Type

Figure 24-24 shows the DCRC event condition asserted when there is busy time-out for Rb1, R5b response.

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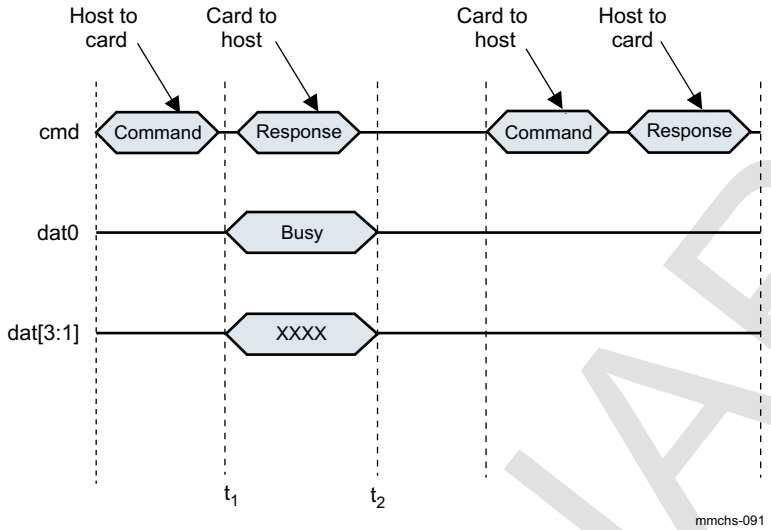
Figure 24-24. Busy Time-Out for R1b, R5b Response Type



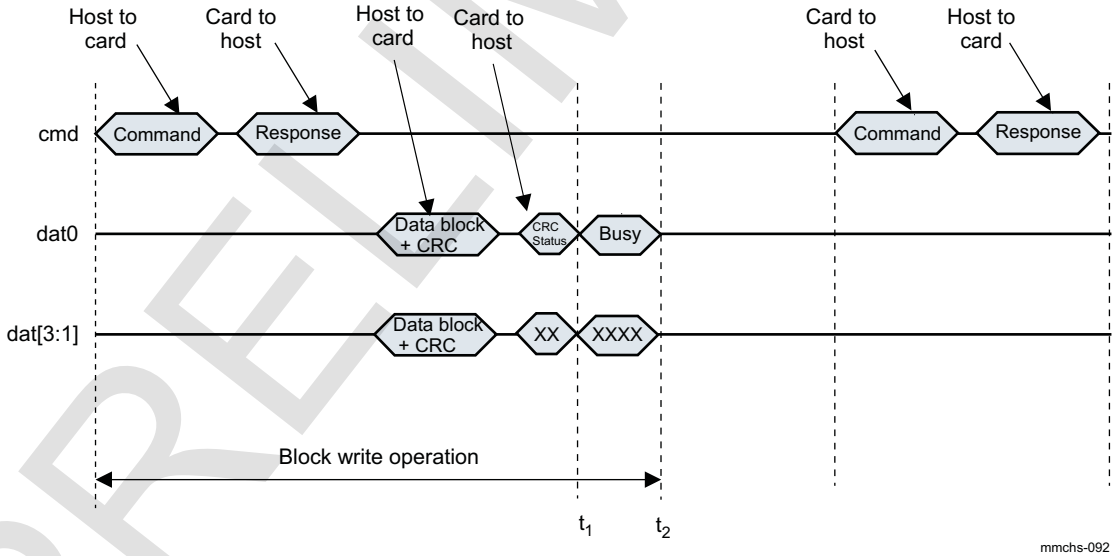
t_1 – Data time-out counter is loaded and starts after R1b, R5b response type.

t_2 – Data time-out counter stops and if it is 0, the MMCHS_STAT[21] DCRC bit is generated.

24.4.9.2 Busy Time-Out After Write CRC Status

Figure 24-25 shows the DCRC event condition asserted when there is busy time-out after write CRC status.

Figure 24-25. Busy Time-Out After Write CRC Status



t_1 – Data time-out counter is loaded and starts after CRC status.

t_2 – Data time-out counter stops and if it is 0, the MMCHS_STAT[21] DCRC bit is generated.

24.4.9.3 Write CRC Status Time-Out

Figure 24-26 shows the DCRC event condition asserted when there is write CRC status time-out.

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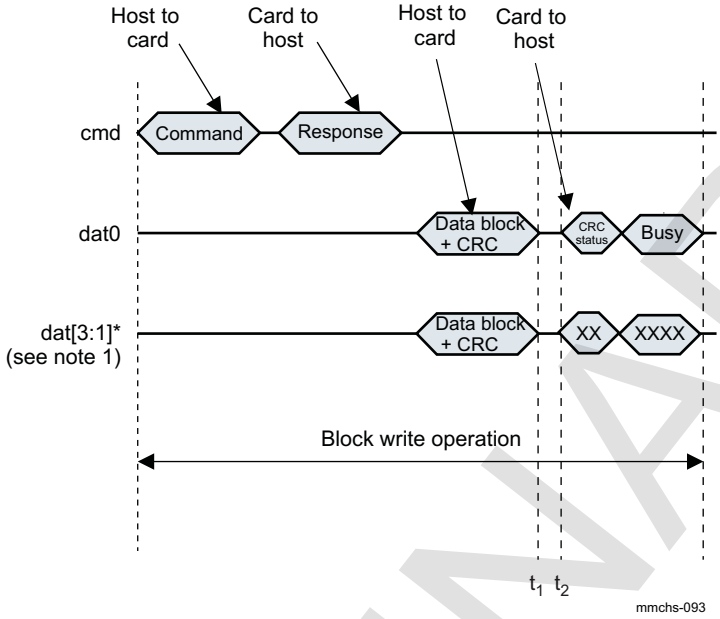
Figure 24-26. Write CRC Status Time-Out



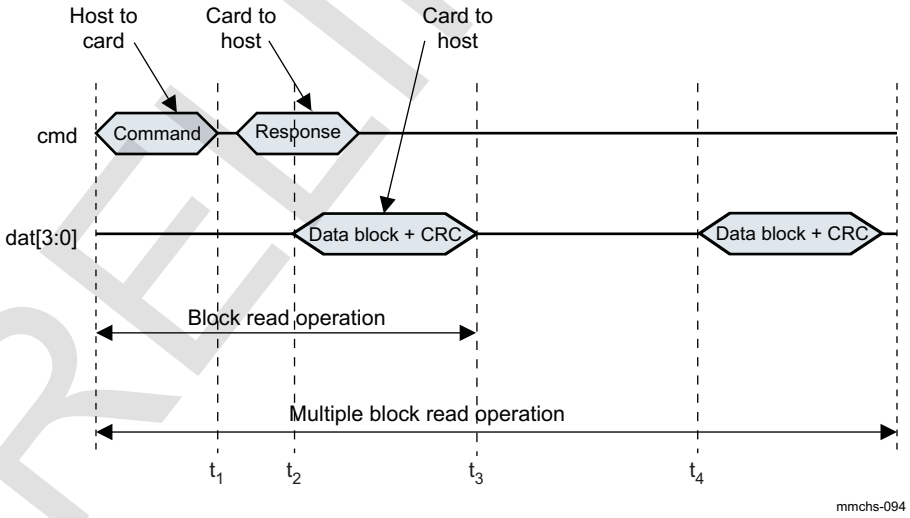
t_1 – Data time-out counter is loaded and starts after data block + CRC.

t_2 – Data time-out counter stops and if it is 0, the MMCHS_STAT[21] DCRC bit is generated.

24.4.9.4 Read Data Time-Out

Figure 24-27 shows the DCRC event condition asserted when there is read data time-out.

Figure 24-27. Read Data Time-Out



t_1 – Data time-out counter is loaded and starts after command transmission.

t_2 – Data time-out counter stops and if it is 0, the MMCHS_STAT[21] DCRC bit is generated.

t_3 – Data time-out counter is loaded and starts after data block + CRC transmission.

t_4 – Data time-out counter stops and if it is 0, the MMCHS_STAT[21] DCRC bit is generated.

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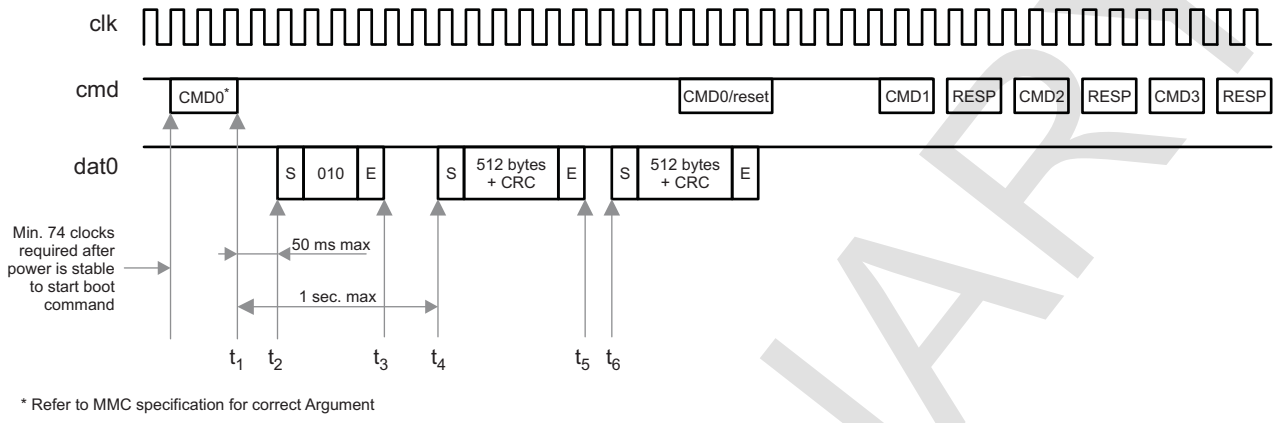
24.4.9.5 Boot Acknowledge Time-Out

Figure 24-28 shows the DCRC event condition asserted when there is a boot acknowledge time-out and CMD0 is used.

Figure 24-28. Boot Acknowledge Time-Out When Using CMD0



t_1 – Data time-out counter is loaded and starts after CMD0.

t_2 – Data time-out counter stops and if it is 0, the MMCHS_STAT[21] DCRC bit is generated.

t_3 – Data time-out counter is loaded and starts.

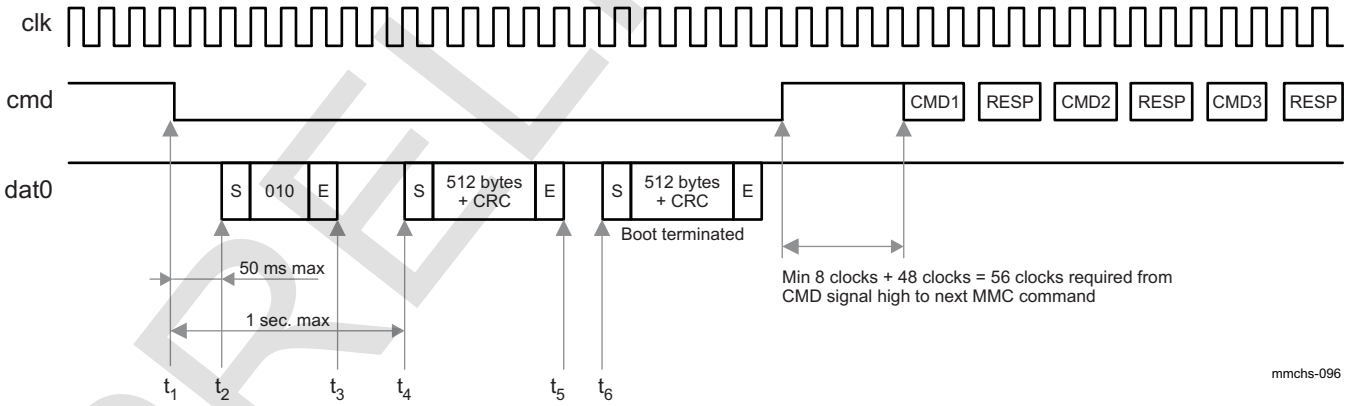
t_4 – Data time-out counter stops and if it is 0, the MMCHS_STAT[21] DCRC bit is generated.

t_5 – Data time-out counter is loaded and starts after data + CRC transmission.

t_6 – Data time-out counter stops and if it is 0, the MMCHS_STAT[21] DCRC bit is generated.

Figure 24-29 shows the DCRC event condition asserted when there is boot acknowledge time-out when the CMD line is tied to 0.

Figure 24-29. Boot Acknowledge Time-Out When CMD Line Tied to 0



t_1 – Data time-out counter is loaded and starts after the CMD line is tied to 0.

t_2 – Data time-out counter stops and if it is 0, the MMCHS_STAT[21] DCRC bit is generated.

t_3 – Data time-out counter is loaded and starts.

t_4 – Data time-out counter stops and if it is 0, the MMCHS_STAT[21] DCRC bit is generated.

t_5 – Data time-out counter is loaded and starts after data + CRC transmission.

t_6 – Data time-out counter stops and if it is 0, the MMCHS_STAT[21] DCRC bit is generated.

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24.4.10 Auto Command 12 Timings

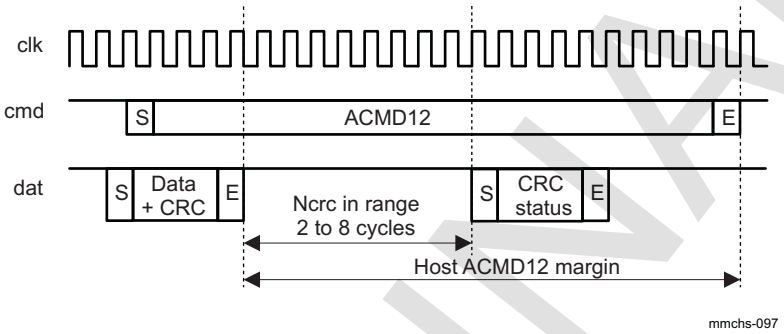
With the UHS definition of SD cards with higher frequency for MMC clock up to 208, the SD standard imposes a specific timing for the arrival of the auto command 12 (ACMD12) end bit.

24.4.10.1 ACMD12 Timings During Write Transfer

A margin named Ncrc in the range of two to eight cycles has been defined for SDR50 and SDR104 card components for write data transfers, because the ACMD12 end bit must arrive after the CRC status end bit.

Figure 24-30 shows the ACMD12 timings during write transfer.

Figure 24-30. ACMD12 Timings During Write Transfer



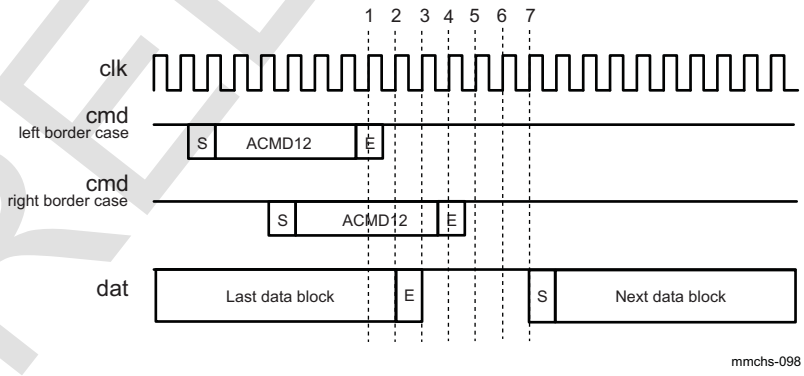
The host controller has a margin of 18 clock cycles to enure that the ACMD12 end bit arrives after the CRC status. This margin does not depend on the MMC bus configuration, DDR, or standard transfer, 1-, 4-, or 8-bit bus width.

24.4.10.2 ACMD12 Timings During Read Transfer

With UHS cards, the gap timing between two successive cards has been extended from two cycles to four cycles. It provides more flexibility for the host ACMD12 arrival to receive the last complete and reliable block. The MMCHS controller follows only the left border case defined by the SD UHS specification.

Figure 24-31 shows ACMD12 timings during read transfer.

Figure 24-31. ACMD12 Timings During Read Transfer



The ACMD12 arrival sent by the host controller is not sensitive to the MMC bus configuration, whether it is a DDR or standard transfer and whether it is a 1-, 4-, or 8-bit bus width transfer.

24.4.11 Transfer Stop

Whenever a transfer is initiated, the transmission may be willed to stop while it is still not finished. Several cases are possible, depending on the transfer type:

- Multiple-block-oriented transfers (transfer length is known)

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- Continuous stream transfers (transfer has an infinite length)

NOTE: Because the MMC/SD/SDIOi controller manages transfers based on a block granularity, the buffer accepts a block only if there is enough space to store it completely. Consequently, if a block is pending in the buffer, no command is sent to the card because the card clock will be shut off by the controller.

The MMC/SD/SDIOi controller includes two features that make a transfer stop more convenient and easier to manage:

- ACMD12 (for MMC and SD only):

  This feature is enabled by setting the MMCi.MMCHS_CMD[2] ACEN bit to 0x1 (this setting is relevant for a MMC/SD transfer with a known number of blocks to transfer). When the ACMD12 feature is enabled, the MMC/SD/SDIOi controller automatically issues a CMD12 command when the expected number of blocks is exchanged.

- Stop at block gap:

  This feature is enabled by setting the MMCi.MMCHS_HCTL[16] SBGR bit to 0x1. When enabled, this capability holds the transfer on until the end of a block boundary. If a stop transmission is needed, software can use this pause to send a CMD12 to the card.

- ADMA mode:

  For ADMA-capable modules (MMC1 and MMC2) (for more information, see Section 24.4.5, *DMA Modes*), the last instruction can stop the transfer (the END bit is enabled in the descriptor line).

NOTE: For MMC and SD cards, the stop-at-block-gap feature is not supported in read mode.

For SDIO cards, this setting can be supported in read mode if the card has a read-wait capability.

Table 24-20 shows the common way to stop a transfer, indicating the command to send and the features to enable.

Table 24-20. MMC/SD/SDIOi Controller Transfer Stop Command Summary

		Write Transfer		Read Transfer	
		SD/MMC	SDIO	SD/MMC	SDIO
Single block		Transfer ends automatically. Wait TC.	Transfer ends automatically. Wait TC.	Transfer ends automatically. Wait TC.	Transfer ends automatically. Wait TC.
Multiblocks (finite or infinite)	Before the programmed block boundary	Send CMD12. Wait TC.	Send CMD52. Wait TC.	Send CMD12. Wait TC.	Send CMD52. Wait TC.
	Stop at the end of the transfer (finite transfer only)	ACMD12 active Transfer ends automatically. Wait TC.	Set MMCi.MMCHS_HCTL[16] SBGR bit to 0x1. Send CMD52. Wait TC.	ACMD12 active Transfer ends automatically. Wait TC.	**If READ_WAIT supported** Stop at block gap. Wait TC.
					If READ_WAIT not supported Send CMD52. Wait TC.

NOTE: The MMC/SD/SDIOi controller sends the stop command to the card on a block boundary, regardless of when the command was written to the controller registers.

24.4.12 Retention Mode

This mode is enabled if the generic parameter bit MMCHS_HL_HWINFO[6] RETMODE is set to 1 during module integration. The controller can enter into retention mode when the module was previously set in

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idle mode. When the module goes into retention mode all clocks are left inactive at low level except for registers that are driven by a falling-edge clock, which are kept as free during retention mode. This also means that all divided functional clock subdomains are forced low when the module enters smart-idle mode. In force-idle mode, the system must ensure that all divided functional clocks are set inactive or are in bypass mode by configuring the MMCHS_SYSCTL register correctly before entering idle mode (under software responsibility).

24.4.13 Output Signals Generation

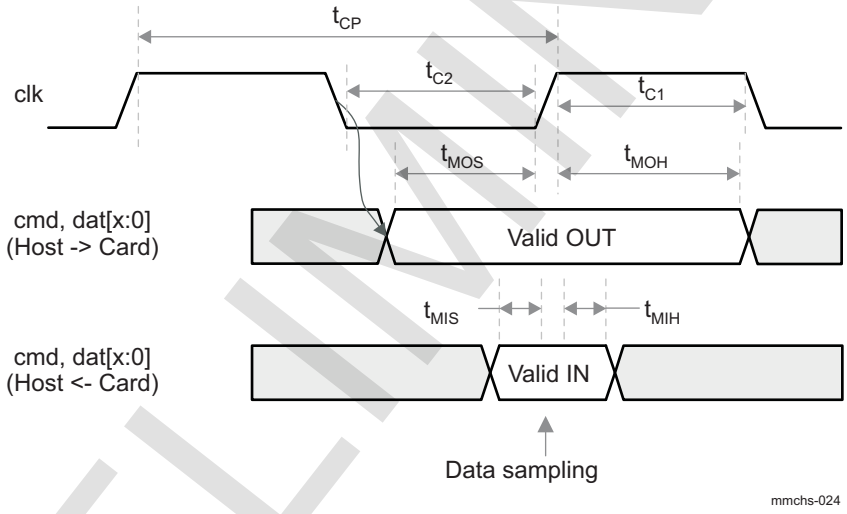
The MMC/SD/SDIO output signals can be driven on the falling edge or rising edge, depending on the MMCHS_HCTL[2] HSPE bit. This feature allows reaching better timing performance, and thus increasing data transfer frequency.

24.4.13.1 Generation on Falling Edge of MMC Clock

The controller is by default in this mode to maximize hold timings. In this case, the MMCHS_HCTL[2] HSPE bit is set to 0.

Figure 24-32 shows the output signals of the module when generating from the falling edge of the MMC clock.

Figure 24-32. Output Driven on Falling Edge



24.4.13.2 Generation on Rising Edge of MMC Clock

This mode increases setup timings and allows reaching higher bus frequency. This feature is activated by setting the MMCHS_HCTL[2] HSPE bit to 1. The controller must be set in this mode to support SDR transfers.

NOTE: Do not use this feature in DDR mode (when the MMCHS_CON[19] DDR bit is set to 1).

Figure 24-33 shows the output signals of the module when generating from the rising edge of the MMC clock.

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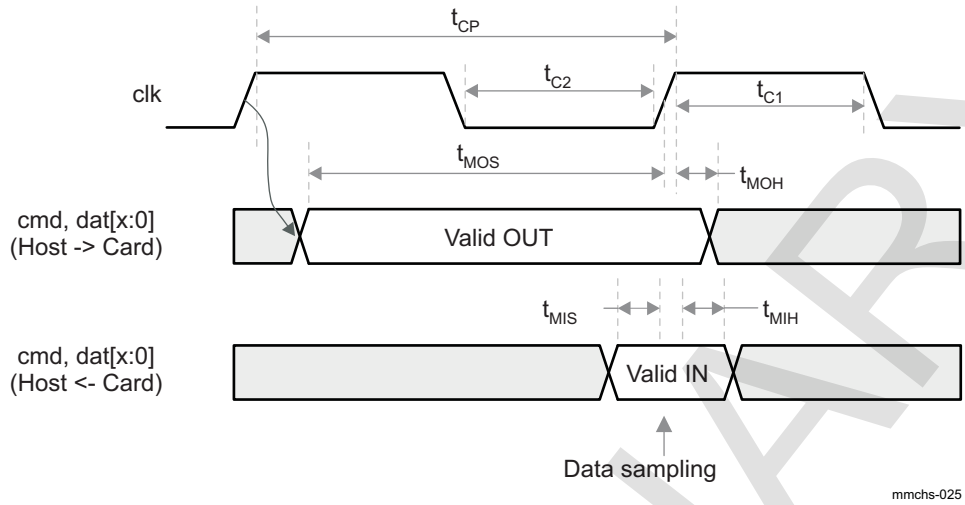
Figure 24-33. Output Driven on Rising Edge



24.4.14 Card Boot Mode Management

Boot operation mode allows the MMC/SD/SDIOi host controller to read boot data from the connected slave (MMC device) by keeping CMD line low after power on (or sending CMD0 with a specific argument) before issuing CMD1. The data can be read from the boot area or user area, depending on the register setting.

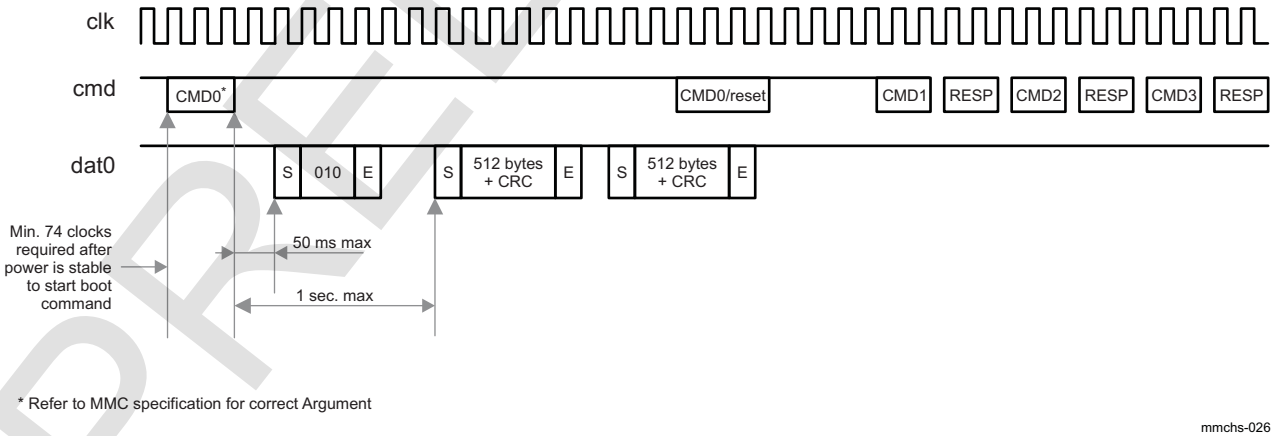
Power-on boot defines a way for the boot code to be accessed by the MMC/SD/SDIOi host controller without an upper-level software driver, speeding the time it takes for a controller to access the boot code.

The two possible ways to issue a boot command (issuing a CMD0 or driving the CMD line to 0 during the whole boot phase) are described in the following sections.

24.4.14.1 Boot Mode Using CMD0

Figure 24-34 shows the timing diagram of a boot sequence using CMD0.

Figure 24-34. Boot Mode Using the CMD0 Timing Diagram



For more information about how to configure the MMC/SD/SDIO host controller, see Section 24.5.1.2.3.1, *Boot Using the CMD0*.

24.4.14.2 Boot Mode With CMD Line Tied to 0

Figure 24-35 shows the timing diagram of a boot sequence with CMD line tied to 0.

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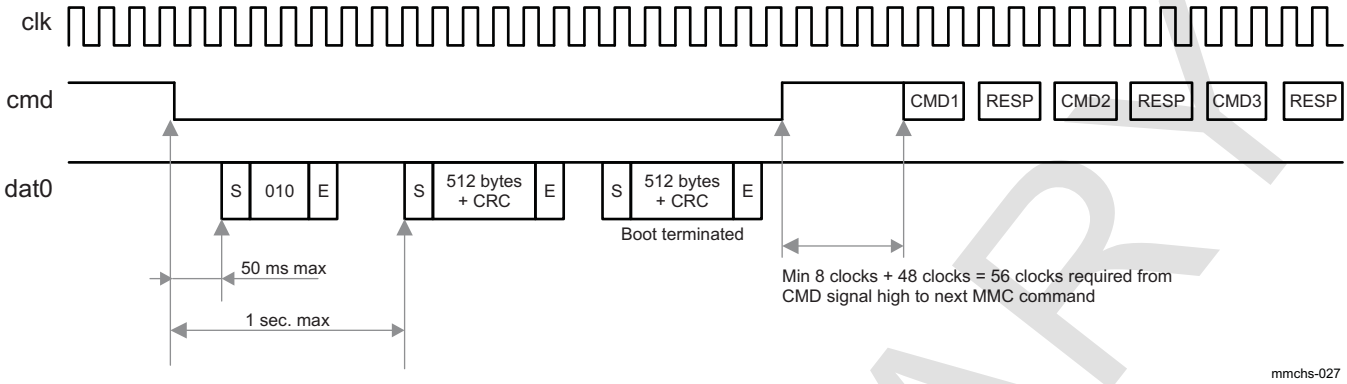
Figure 24-35. Boot Mode With CMD Line Tied to 0 Timing Diagram



For more information about how to configure the MMC/SD/SDIO host controller, see Section 24.5.1.2.3.2, *Boot With CMD Line Tied to 0*.

24.4.15 MMC CE-ATA Command Completion Disable Management

The MMC/SD/SDIOi host controller supports CE-ATA features, in particular the detection of command completion token. When a command that requires a command completion signal (the MMCHS_CON[12] CEATA and MMCHS_CMD[2] ACEN bits set to 1) is launched, the host system is no longer allowed to emit a new command in parallel to the data transfer unless it is a command completion disable token.

The settings to emit a command completion disable token are:

- The MMCHS_CON[12] CEATA bit is set to 1.
- The MMCHS_CON[2] bit HR set to 1.
- Clear the MMCHS_ARG register.
- Write into the MMCHS_CMD register with the value 0x00000000.

When a command completion disable token was emitted (that is, the MMCHS_STAT[0] CC bit received), the host system is again allowed to emit another type of command (for example, a CMD12 to abort transfer).

A critical case can be encountered when command completion signal disable (CCSD) is emitted during the last data block transfer, and the sequence on the command line is sent close to the command completion signal (CCS) token sent by the card.

Three possible cases are:

- CCS is received immediately before CCSD is emitted:

  An interrupt CIRQ is generated with CCS detection, CCSD is transmitted to the card, and then an interrupt CC is generated when CCSD ends. In this case, the card considers the CCSD sequence.
- CCS is not generated or is generated during the CCSD transfer:

  The CCS bit cannot be detected (conflict is not possible because they drive the same level on the command line, and no CIRQ interrupt is generated; a CC interrupt is generated when CCSD ends).
- CCS is generated without CCSD token required:

  Only the interrupt CIRQ is generated when CCS is detected.

24.4.16 Test Registers

Test registers are available to comply with the *SD Host Controller Specification*. This feature is useful to generate interrupts manually for driver debugging.

The force event register (MMCHS_FE) is used to control the error interrupt status and ACMD12 error status.

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The system test register (MMCHS_SYSTEST) is used to control the signals that connect to I/O pins when the module is configured in the system test mode (the MMCHS_CON[4] MODE bit = 1) for boundary connectivity verification.

24.4.17 MMC/SD/SDIO Hardware Status Features

Table 24-21 describes the MMC/SD/SDIO hardware status features.

Table 24-21. MMC/SD/SDIO Hardware Status Features

Feature	Type	Register/Bit Field/Observability Control	Description
Interrupt flags		See Section 24.4.4, *Interrupt Requests.*	
CMD line signal level	Status	MMCHS_PSTATE[24] CLEV	Indicates the level of the command line
DAT lines signal level	Status	MMCHS_PSTATE[23:20] DLEV	Indicates the level of the data lines
Buffer read enable	Status	MMCHS_PSTATE[11] BRE	Readable data exists in the buffer.
Buffer write enable	Status	MMCHS_PSTATE[10] BWE	Indicates whether there is enough space in the buffer to write BLEN bytes of data
Read transfer active	Status	MMCHS_PSTATE[9] RTA	Used to detect completion of a read transfer.
Write transfer active	Status	MMCHS_PSTATE[8] WTA	Indicates a write transfer active
Data line active	Status	MMCHS_PSTATE[2] DLA	Indicates whether the data lines are active
Command Inhibit (DAT lines)	Status	MMCHS_PSTATE[1] DATI	Indicates whether issuing of command using data lines is allowed
Command inhibit (CMD line)	Status	MMCHS_PSTATE[0] CMDI	Indicates whether issuing of command using command line is allowed

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24.5 MMC/SD/SDIO Programming Guide

24.5.1 Low-Level Programming Models

24.5.1.1 Global Initialization

24.5.1.1.1 Surrounding Modules Global Initialization

This section identifies the requirements for initializing the surrounding modules when the module must be used for the first time after a device reset. This initialization of surrounding modules is based on the integration and environment of the MMC/SD/SDIO modules. For more information, see Section 24.3, *MMC/SD/SDIO Integration*, and Section 24.2, *MMC/SD/SDIO Environment*.

Table 24-22. Global Initialization of Surrounding Modules

Surrounding Modules	Comments
PRCM	Module interface and functional clocks must be enabled. See Chapter 3, *Power, Reset, and Clock Management*.
Control module	Module-specific pad muxing and configuration must be set in the control module. See Chapter 18, *Control Module*.
(optional) MPU INTC (or DSP INTC)	MPU INTC configuration must be done to enable the interrupts from the MMCHS module. See Chapter 17, *Interrupt Controllers*.
(optional) sDMA (or dDMA)	DMA configuration must be done to enable the module DMA channel requests. See Chapter 16, *sDMA*.
(optional) Interconnect	For more information about the interconnect configuration, see Chapter 13, *Interconnect*.

NOTE: The MPU/DSP INTC and the sDMA/dDMA configurations are necessary if the interrupt and DMA-based communication modes are used.

24.5.1.1.2 MMC/SD/SDIO Host Controller Initialization Flow

Table 24-23 shows the general boot process.

Table 24-23. MMC/SD/SDIO Controller Meta Initialization Steps

Step	Access Type	Register/Bit Field/Programming Model	Value
Initialize clocks.		See Section 24.5.1.1.2.1.	
Software reset of the controller.		See Section 24.5.1.1.2.2.	
Set module hardware capabilities.		See Section 24.5.1.1.2.3.	
Set module idle and wake-up modes.		See Section 24.5.1.1.2.4.	

24.5.1.1.2.1 Enable Interface and Functional clock for MMC Controller

Before any MMCHS register access, the MMCHS interface clock and functional clock in the PRCM module registers must be enabled. See , *Clock Domain Module Attributes*, in Chapter 3, *Power, Reset, and Clock Management*.

24.5.1.1.2.2 MMCHS Soft Reset Flow

Figure 24-36 shows the soft reset process of the MMCHS controller.

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Figure 24-36. MMC/SD/SDIO Controller Software Reset Flow

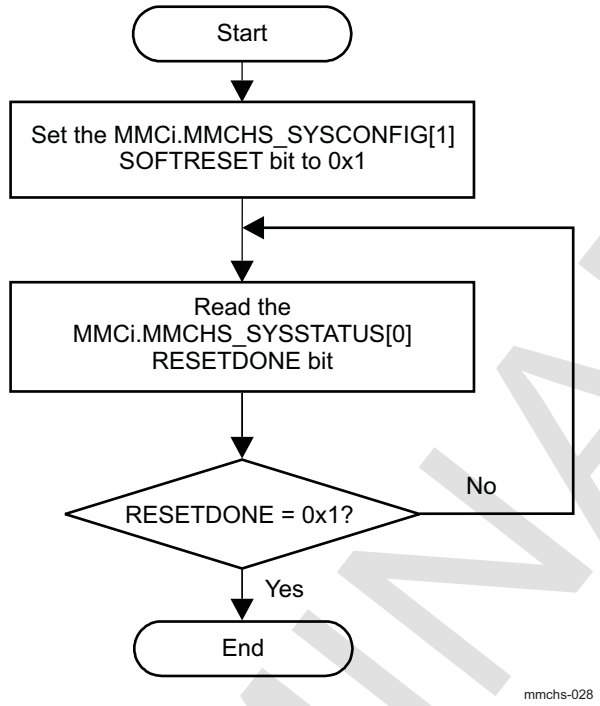

Table 24-24. Register Call Summary for Main Sequence – Software Reset Flow

Register Name	Register Name
MMCHS_SYSCONFIG	MMCHS_SYSSTATUS

24.5.1.1.2.3 Set MMCHS Default Capabilities

Software must read capabilities (in boot ROM, for example) and is allowed to set (write) the MMCi.MMCHS_CAPA[26:24] and MMCi.MMCHS_CUR_CAPA[23:0] bit fields before the MMC/SD/SDIO host driver is started.

24.5.1.1.2.4 Wake-Up Configuration

Table 24-25 describes the MMCHS controller wake-up configuration.

Table 24-25. MMC/SD/SDIO Controller Wake-Up Configuration

Step	Access Type	Register/Bit Field/Programming Model	Value
Configure wake-up bit (if necessary).	W	MMCi.MMCHS_SYSCONFIG[2] ENAWAKEUP	0x1
Enable wake-up events on SD card interrupt (if necessary).	W	MMCi.MMCHS_HCTL[24] IWE	0x1
SDIO card only: Enable card interrupt (if necessary).	W	MMCi.MMCHS_IE[8] CIRQ_ENABLE	0x1

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24.5.1.1.2.5 MMC Host and Bus Configuration

Figure 24-37 shows the MMC bus configuration process.

Figure 24-37. MMC/SD/SDIO Controller Bus Configuration

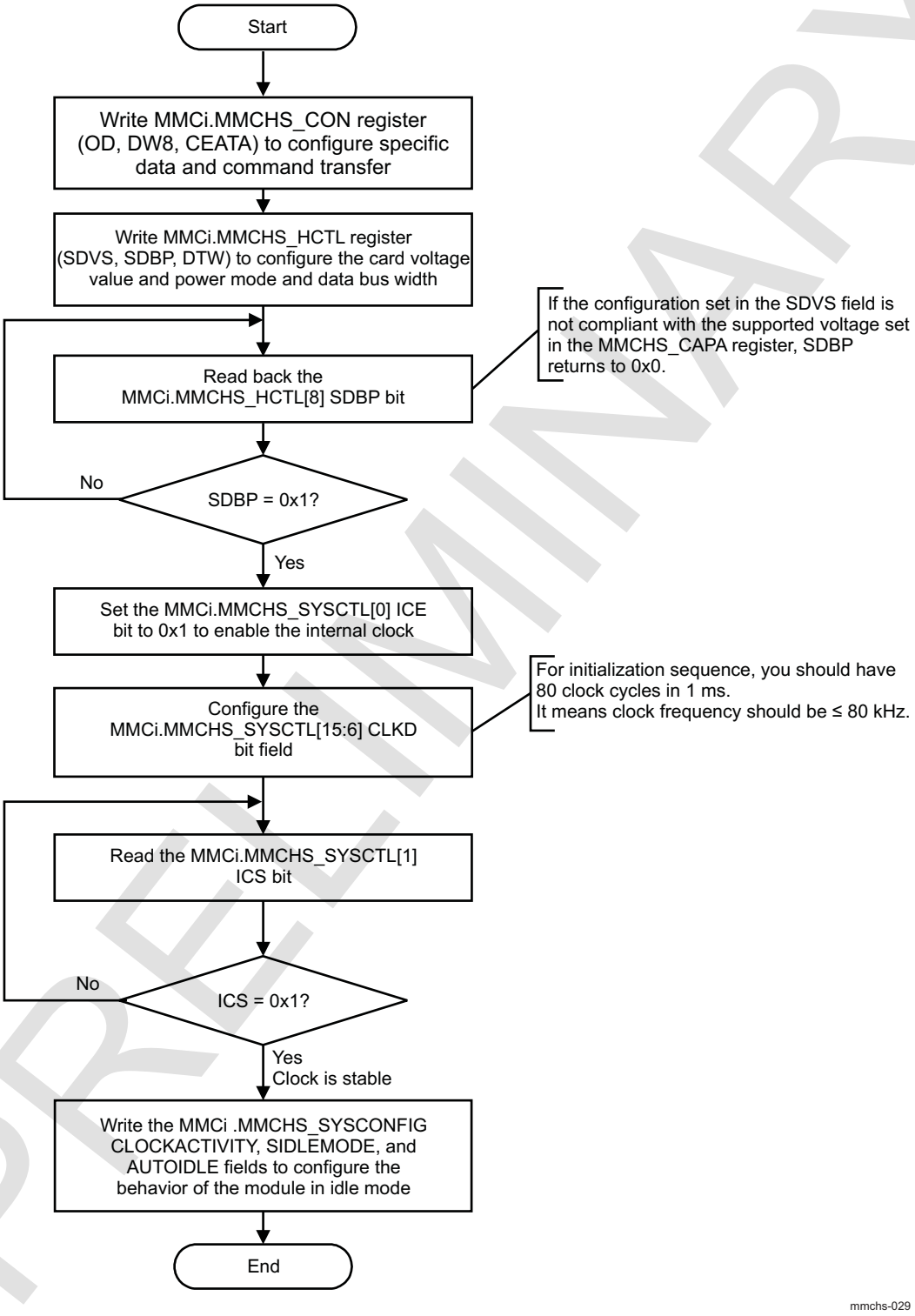

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Table 24-26. Register Call Summary for Main Sequence – Bus Configuration

Register Name	Register Name
MMCHS_CON	MMCHS_HCTL
MMCHS_SYSCONFIG	MMCHS_SYSCTL

24.5.1.2 Operational Modes Configuration

24.5.1.2.1 Basic Operations for MMC/SD/SDIO Host Controller

The MMC/SD/SDIO host controller performs data transfers: data to card (referred to as write transfers) and data from card (referred to as read transfers).

The host controller requires transfers to run on a block-by-block basis rather than on a DMA burst size basis. A single DMA request (or block request interrupt) is signaled for each block. Pipelining is supported as long as the block size is less than one half of the memory buffer size.

24.5.1.2.1.1 Card Detection, Identification, and Selection

Figure 24-38 and Figure 24-39 show the card identification and selection process.

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Figure 24-38. MMC/SD/SDIO Controller Card Identification and Selection – Part 1

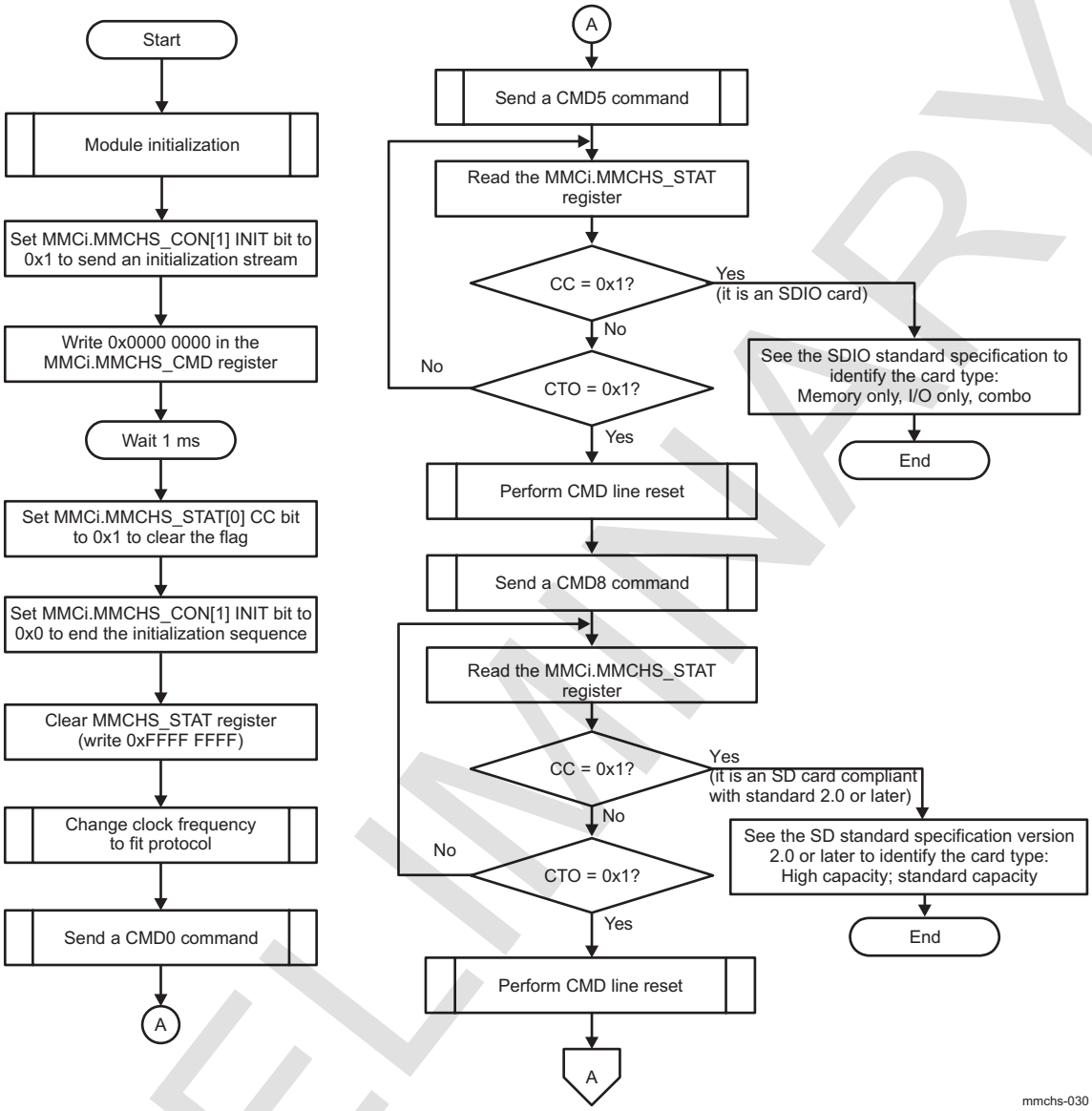

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Figure 24-39. MMC/SD/SDIO Controller Card Identification and Selection – Part 2

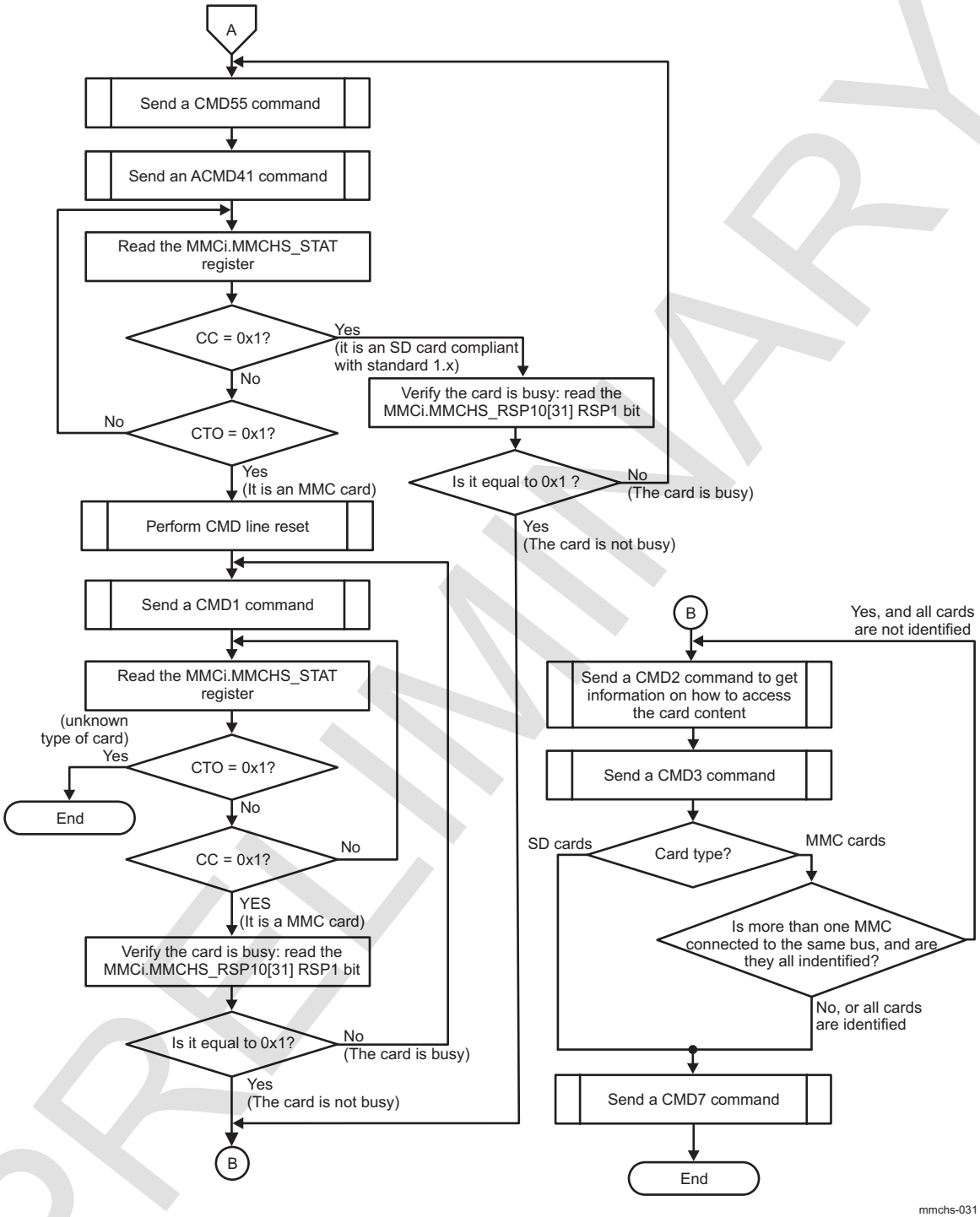

Table 24-27. Register Call Summary for Main Sequence – Card Identification and Selection

Register Name	Register Name	Register Name
MMCHS_CON	MMCHS_CMD	MMCHS_STAT
MMCHS_SYSCTL	MMCHS_RSP10	

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Table 24-28. Subprocess Call Summary for Main Sequence – Card Identification and Selection

Subprocess Name	Cross-Reference
Initialize module.	Section 24.5.1.1.2
Change clock frequency to fit protocol.	Section 24.5.1.2.1.7.2
Send a command.	Section 24.5.1.2.1.7.1
Perform CMD line reset.	Section 24.5.1.2.1.1.1

24.5.1.2.1.1.1 CMD Line Reset Procedure

Table 24-29. CMD Line Reset

Step	Access Type	Register/Bit Field/Programming Model	Value
Initiate CMD line reset.	W	MMCi.MMCHS_SYSCTL[25] SRC	0x1
Poll the SRC bit until it is set to 0x1.	R	MMCi.MMCHS_SYSCTL[25] SRC	= 0x1
Wait until the SRC bit returns to 0x0 (reset procedure is completed).	R	MMCi.MMCHS_SYSCTL[25] SRC	= 0x0

24.5.1.2.1.2 Read/Write Transfer Flow in DMA Mode With Interrupt

Figure 24-40 shows the read and write protocol in DMA slave mode with interrupt signaling. For more information about the DMA settings, see Section 16.5, *sDMA Basic Programming Model*, in Chapter 16, *sDMA*.

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Figure 24-40. MMC/SD/SDIO Controller Read/Write Transfer Flow in DMA Slave Mode With interrupt

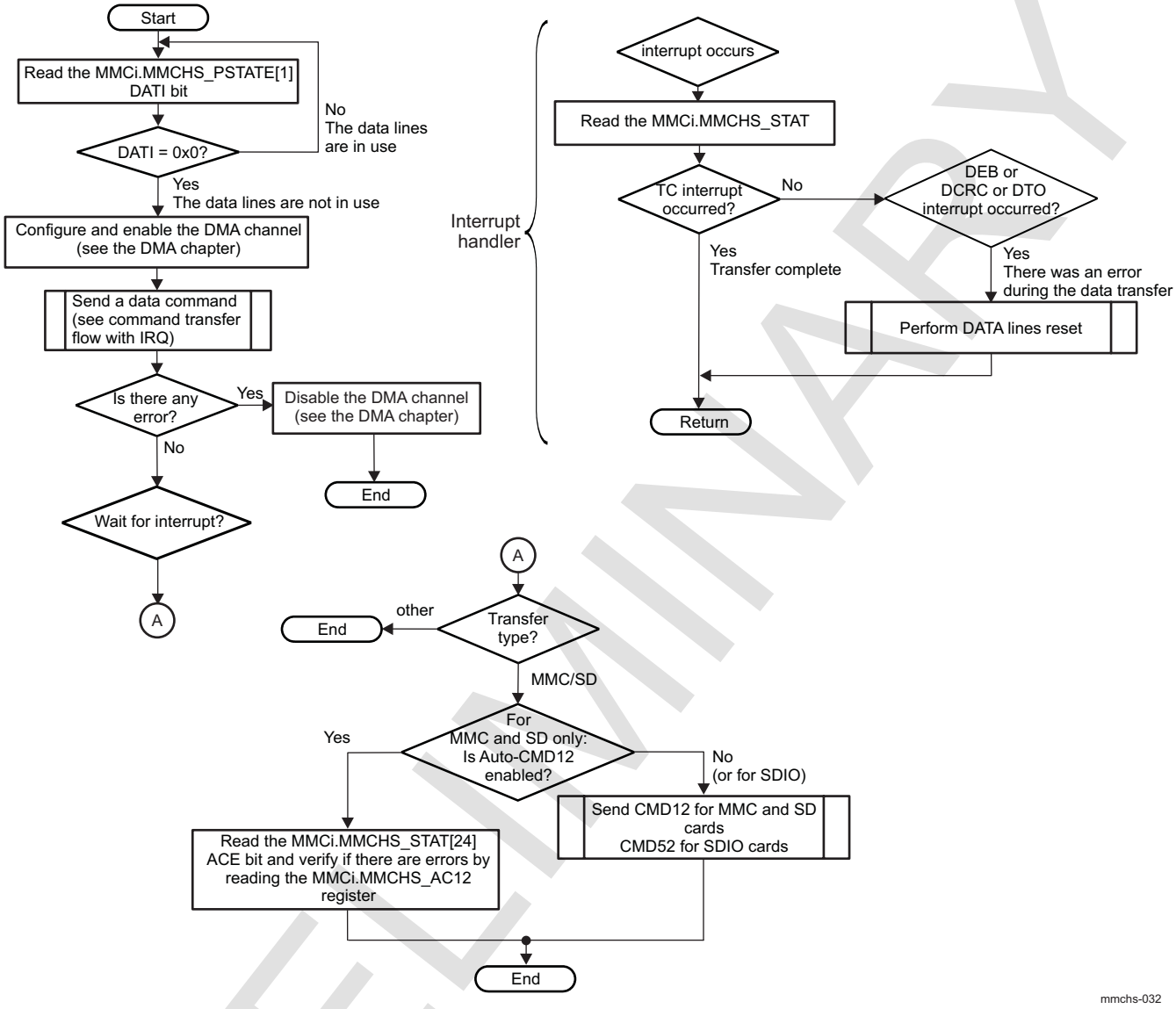

Table 24-30. Register Call Summary for Main Sequence – Read/Write Transfer Flow in DMA Mode With interrupt

Register Name	Register Name
MMCHS_PSTATE	MMCHS_STAT
MMCHS_SYSCTL	MMCHS_CMD

Table 24-31. Subprocess Call Summary for Main Sequence – MMC/SD/SDIO Controller Read/Write Transfer Flow in DMA Mode With Interrupt

Subprocess Name	Cross-Reference
Send a data command.	Figure 24-47
Perform DATA lines reset.	Section 24.5.1.2.1.2.1

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24.5.1.2.1.2.1 DATA Lines Reset Procedure

Table 24-32 describes the DATA lines reset.

Table 24-32. DATA Lines Reset

Step	Access Type	Register/Bit Field/Programming Model	Value
Initiate DATA lines reset.	W	MMCi.MMCHS_SYSCTL[26] SRD	0x1
Poll the SRD bit until it is set to 0x1.	R	MMCi.MMCHS_SYSCTL[26] SRD	= 0x1
Wait until the SRD bit returns to 0x0 (reset procedure is complete).	R	MMCi.MMCHS_SYSCTL[26] SRD	= 0x0

24.5.1.2.1.3 Read/Write Transfer Flow in DMA Mode With Polling

Figure 24-41 shows the read and write protocol in DMA mode. For more information about the DMA settings, see Section 16.5, *sDMA Basic Programming Model* in Chapter 16, *sDMA*.

Figure 24-41. MMC/SD/SDIO Controller Read/Write Transfer Flow in DMA Mode With Polling

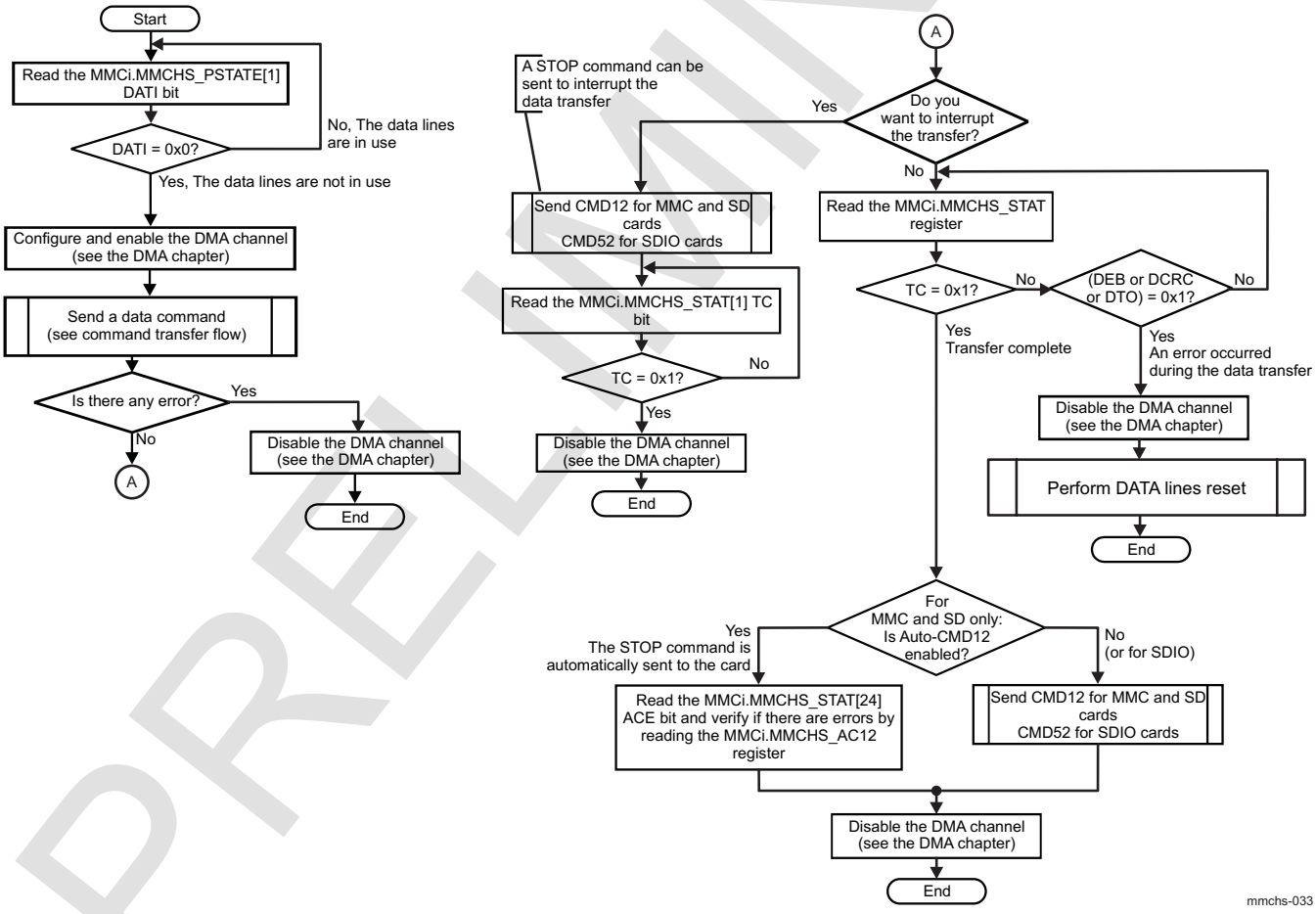

Table 24-33. Register Call Summary for Main Sequence – Read/Write Transfer Flow in DMA Mode With Polling

Register Name	Register Name	Register Name
MMCHS_PSTATE	MMCHS_STAT	MMCHS_SYSCTL

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Table 24-33. Register Call Summary for Main Sequence – Read/Write Transfer Flow in DMA Mode With Polling (continued)

Register Name	Register Name	Register Name
MMCHS_CMD	MMCHS_AC12	

Table 24-34. Subprocess Call Summary for Main Sequence – Read/Write Transfer Flow in DMA Mode With Polling

Subprocess Name	Cross-Reference
Send command.	Section 24.5.1.2.1.7.1
Perform DATA lines reset.	Section 24.5.1.2.1.2.1

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24.5.1.2.1.4 Read/Write Transfer Flow Without DMA With Polling

Figure 24-42 shows a read/write transfer without using the DMA and with polling.

Figure 24-42. MMC/SD/SDIO Controller Read/Write Transfer Flow Without DMA and With Polling

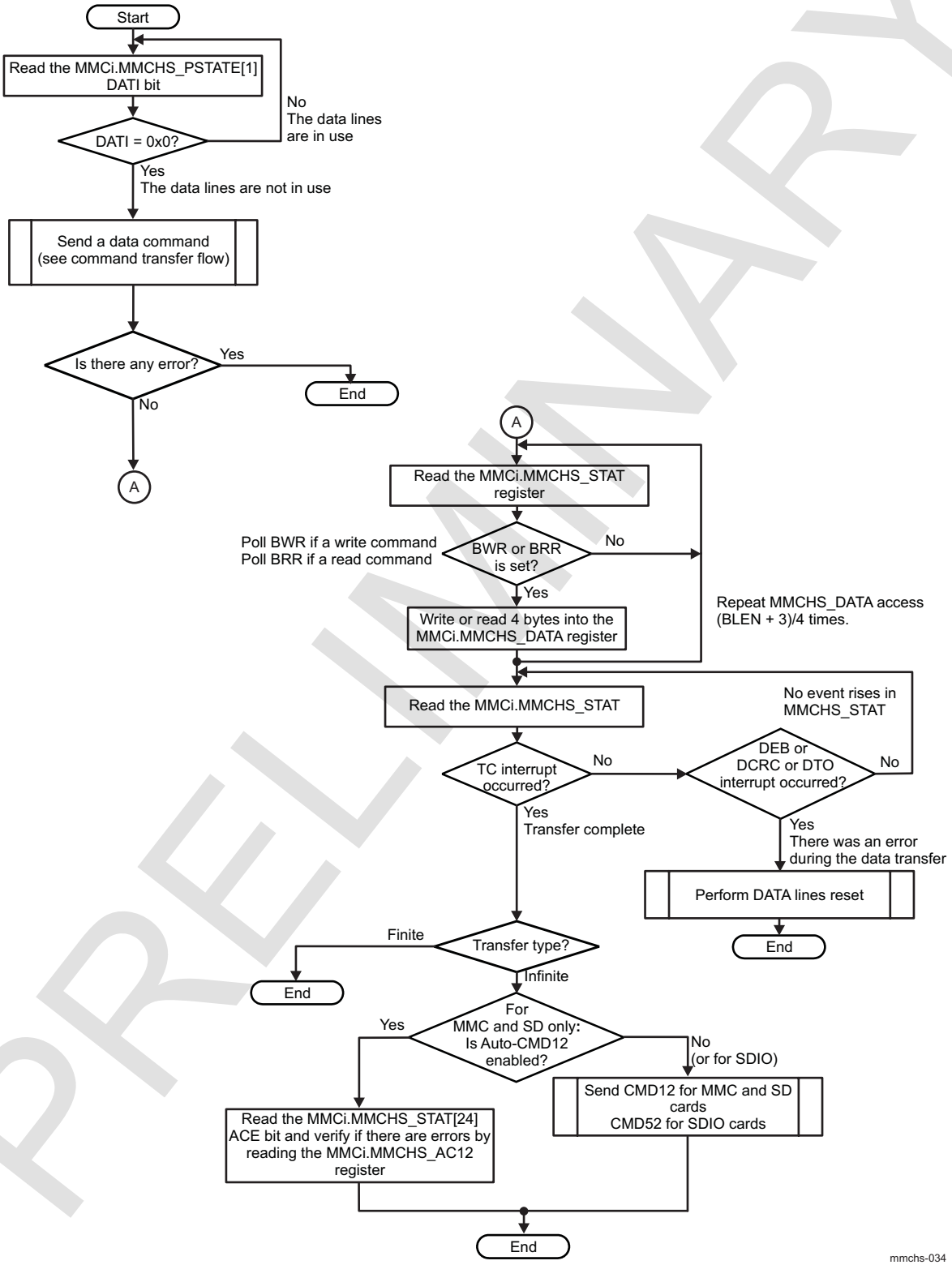

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Table 24-35. Register Call Summary for Main Sequence – Read/Write Transfer Flow Without DMA With Polling

Register Name	Register Name	Register Name
MMCHS_PSTATE	MMCHS_DATA	MMCHS_STAT
MMCHS_SYSCTL	MMCHS_CMD	MMCHS_AC12

Table 24-36. Subprocess Call Summary for Main Sequence – Read/Write Transfer Flow Without DMA With Polling

Subprocess Name	Cross-Reference
Send data command.	Section 24.5.1.2.1.7.1
Perform DATA lines reset.	Section 24.5.1.2.1.2.1

24.5.1.2.1.5 Read/Write Transfer Flow in CE-ATA Mode

Figure 24-43 shows the read and write CE-ATA protocol when in polling mode.

Figure 24-43. MMC/SD/SDIO Controller Read/Write in CE-ATA Mode

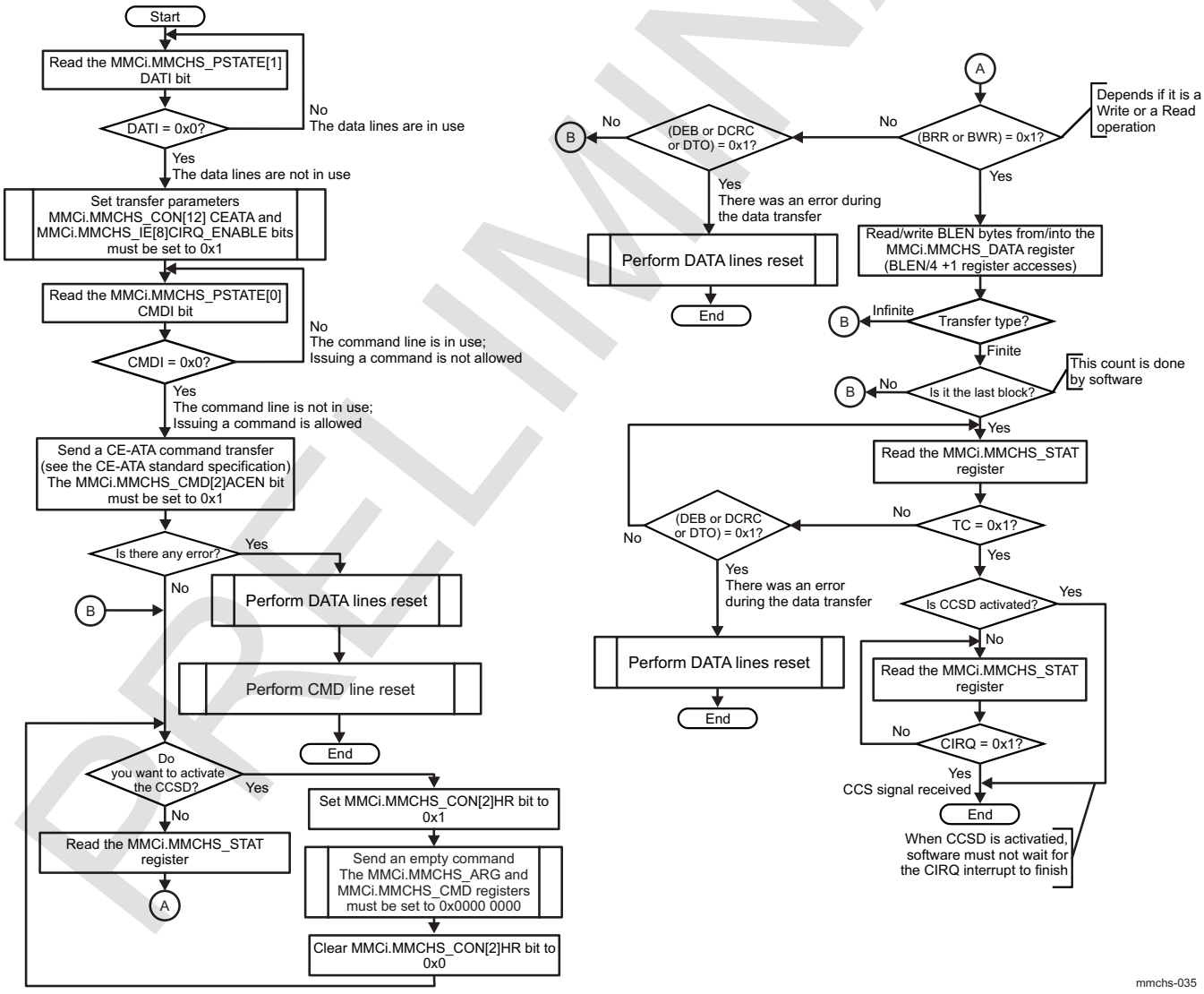

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Table 24-37. Register Call Summary for Main Sequence – Read/Write in CE-ATA Mode

Register Name	Register Name	Register Name
MMCHS_PSTATE	MMCHS_CON	MMCHS_IE
MMCHS_CMD	MMCHS_STAT	
MMCHS_ARG	MMCHS_SYSCTL	

Table 24-38. Subprocess Call Summary for Main Sequence – Read/Write in CE-ATA Mode

Subprocess Name	Cross-Reference
Perform CMD line reset.	Section 24.5.1.2.1.1.1
Perform DATA lines reset.	Section 24.5.1.2.1.2.1

CAUTION

CE-ATA protocol is supported only by MMC cards.

In CE-ATA mode, issuing a command during the transfer (except a CCSD command) is not allowed.

In CE-ATA mode, infinite transfers are not allowed; only finite transfers are permitted.

24.5.1.2.1.6 Suspend-Resume Flow

The suspend and resume feature is supported only by SDIO cards.

24.5.1.2.1.6.1 Suspend Flow

Figure 24-44 shows the suspend flow for SDIO cards.

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Figure 24-44. MMC/SD/SDIO Controller Suspend Flow

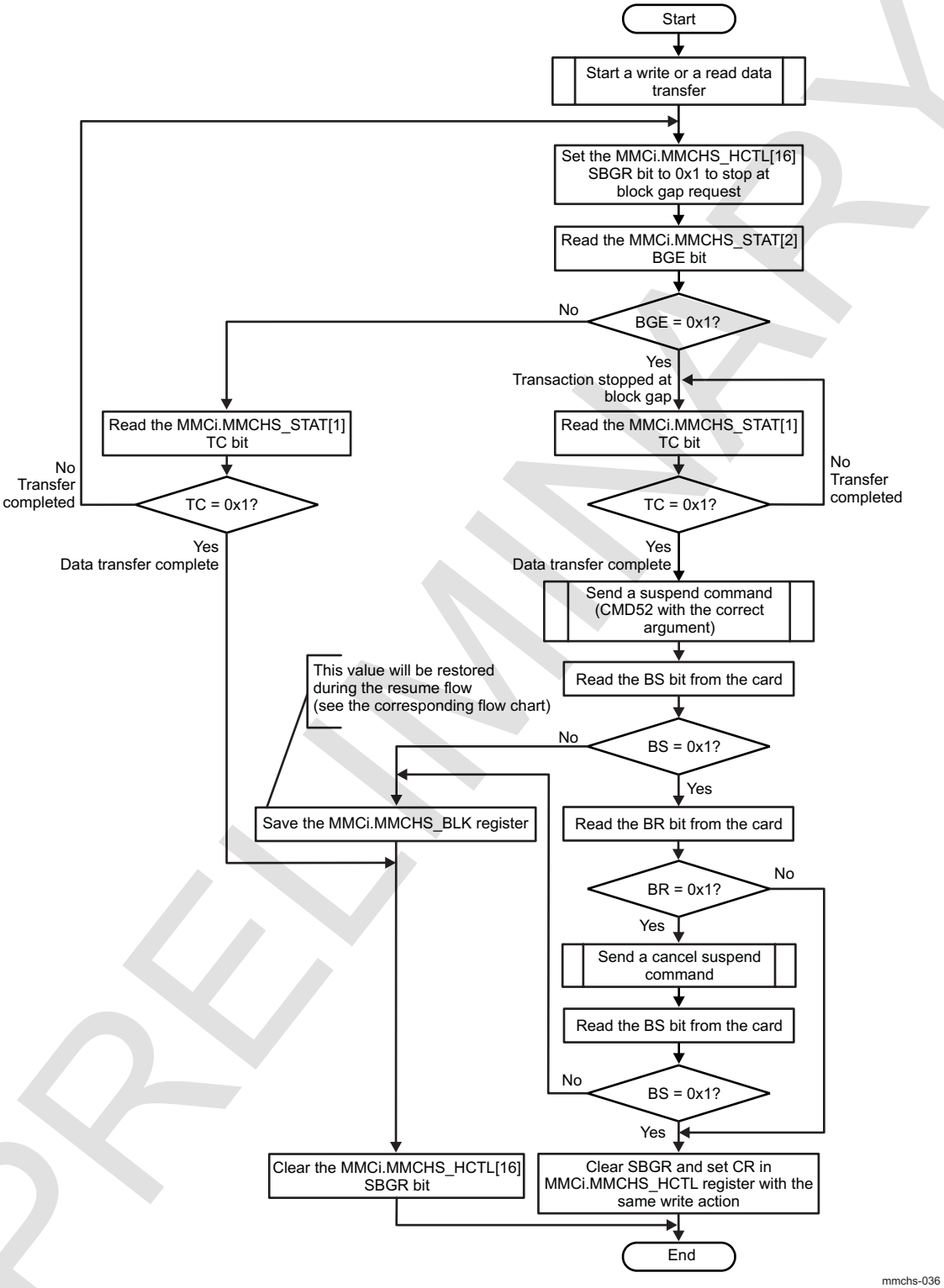

Table 24-39. Register Call Summary for Main Sequence – Suspend Flow

Register Name	Register Name	Register Name
MMCHS_HCTL	MMCHS_STAT	MMCHS_BLK

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Table 24-40. Subprocess Call Summary for Main Sequence – Suspend Flow

Subprocess Name	Cross-Reference
Start a write or a read data transfer.	Section 24.5.1.2.1
Send a suspend command (CMD52 with the correct argument).	Section 24.5.1.2.1.7.1
Send a cancel suspend command.	Section 24.5.1.2.1.7.1

24.5.1.2.1.6.2 Resume Flow

Figure 24-45 shows the resume flow for SDIO cards.

Figure 24-45. MMC/SD/SDIO Controller Resume Flow

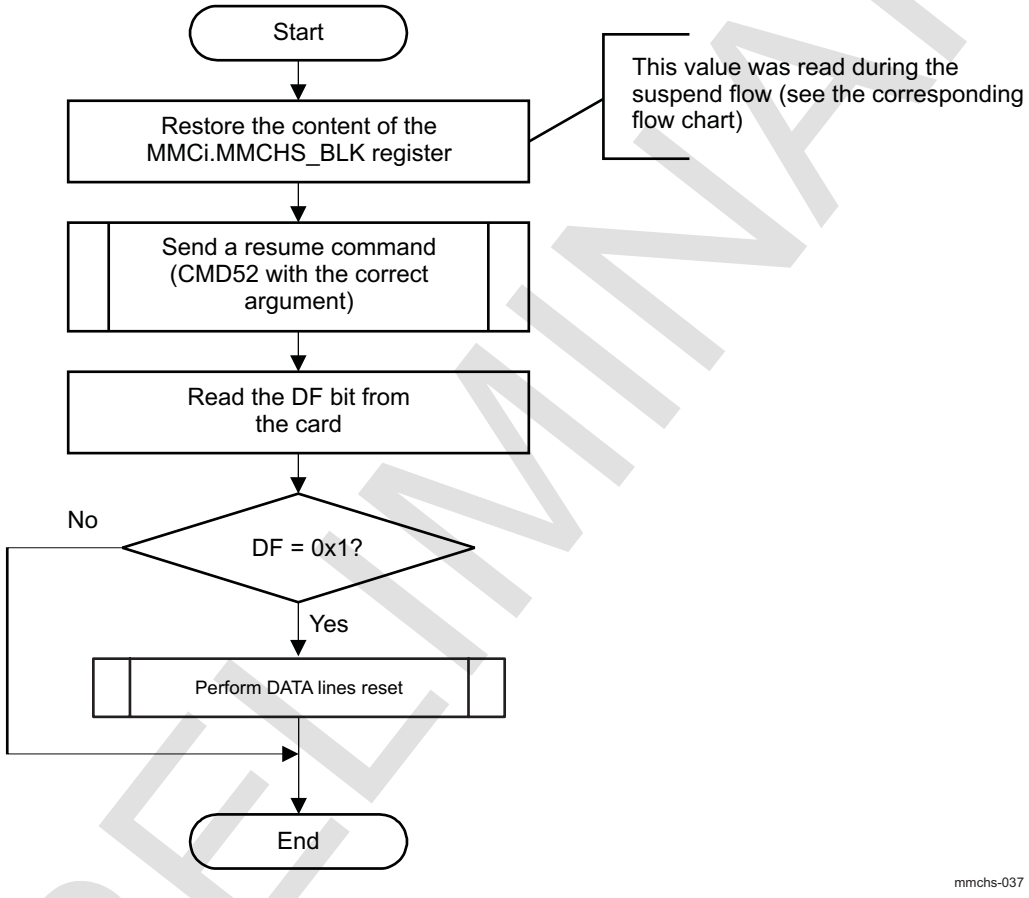

Table 24-41. Register Call Summary for Main Sequence - Resume Flow

Register Name	Register Name
MMCHS_BLK	MMCHS_SYSCTL

Table 24-42. Subprocess Call Summary for Main Sequence - Resume Flow

Subprocess Name	Cross-Reference
Send a resume command (CMD52 with the correct argument).	Section 24.5.1.2.1.7.1
Perform DATA lines reset.	Section 24.5.1.2.1.2.1

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24.5.1.2.1.7 Basic Operations – Steps Detailed

24.5.1.2.1.7.1 Command Transfer Flow

Figure 24-46 shows how to send a command to the card using polling instead of interrupts for event signaling.

Figure 24-46. MMC/SD/SDIO Controller Command Transfer Flow With Polling

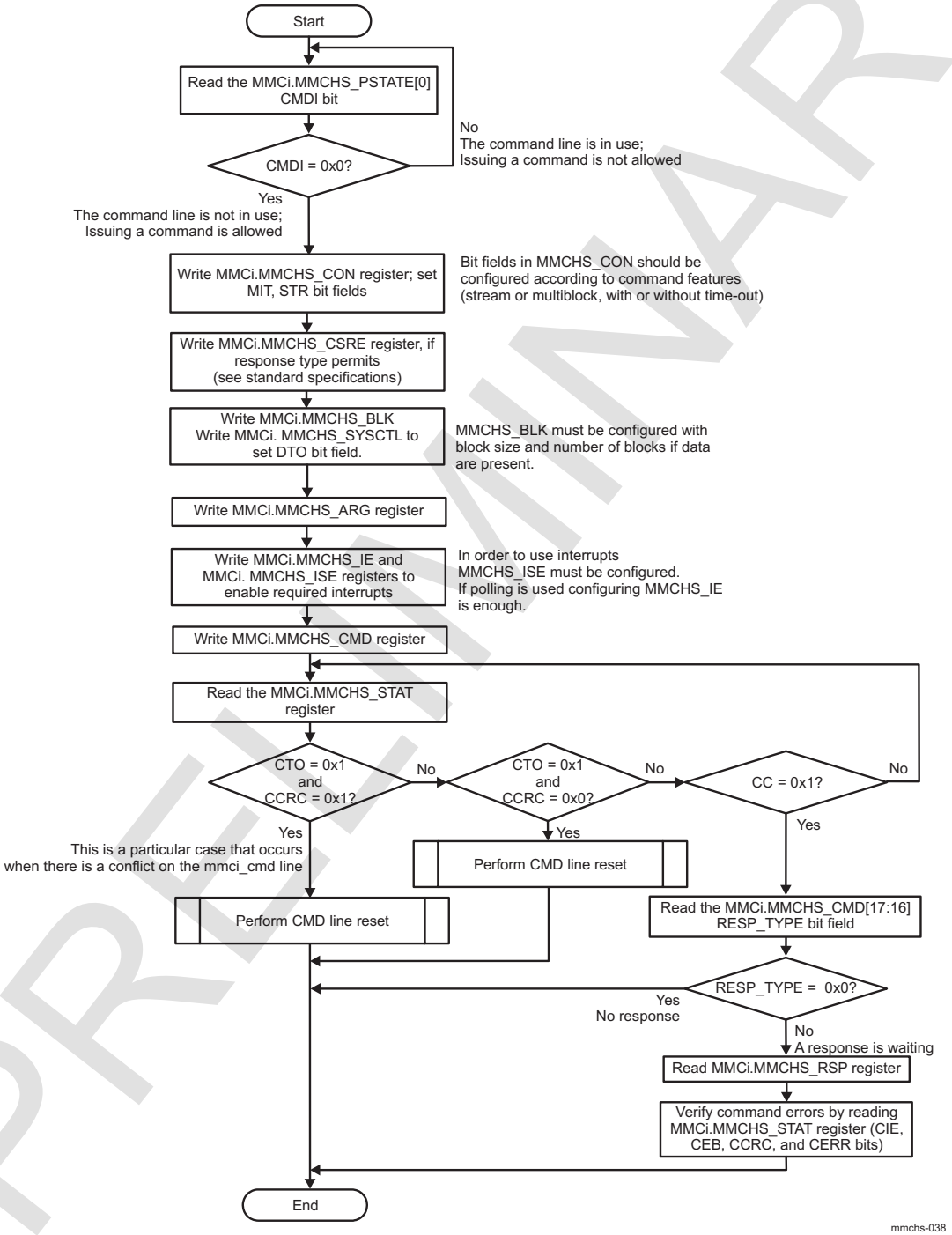

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Table 24-43. Register Call Summary for Main Sequence – Command Transfer Flow With Polling

Register Name	Register Name	Register Name
MMCHS_PSTATE	MMCHS_CON	MMCHS_CSRE
MMCHS_STAT	MMCHS_BLK	MMCHS_SYSCTL
MMCHS_ARG	MMCHS_IE	MMCHS_CMD
MMCHS_RSP10	MMCHS_RSP32	MMCHS_RSP54
MMCHS_RSP76		

Table 24-44. Subprocess Call Summary for Main Sequence – Command Transfer Flow With Polling

Subprocess Name	Cross-Reference
Perform CMD line reset.	Section 24.5.1.2.1.1.1

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Figure 24-47 shows how to send a command to the card using interrupts for event signaling.

Figure 24-47. MMC/SD/SDIO Controller Command Transfer Flow With interrupts

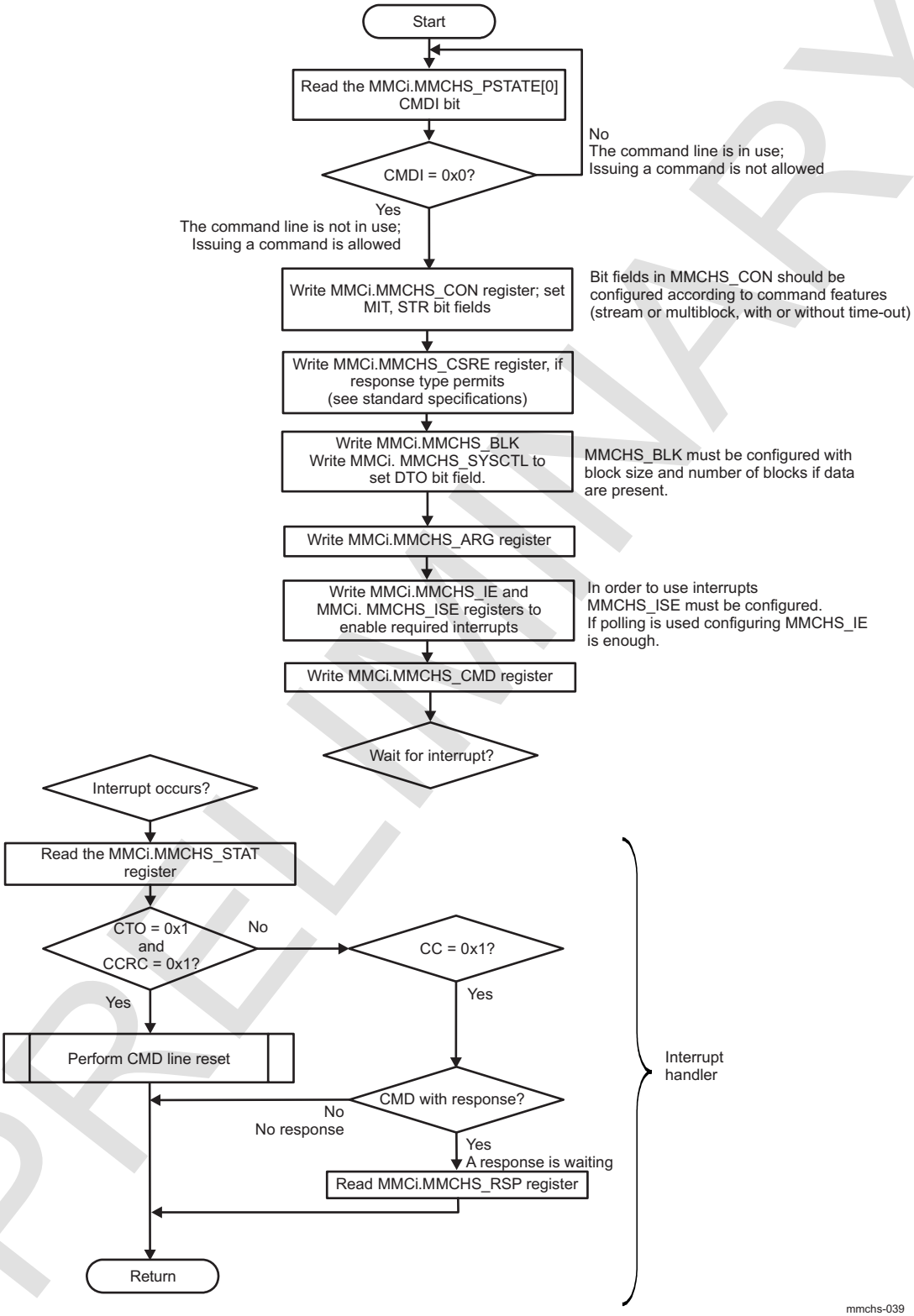

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Table 24-45. Register Call Summary for Main Sequence – Command Transfer Flow With Interrupts

Register Name	Register Name	Register Name
MMCHS_PSTATE	MMCHS_CON	MMCHS_CSRE
MMCHS_STAT	MMCHS_BLK	MMCHS_SYSCTL
MMCHS_ARG	MMCHS_IE	MMCi.MMCHS_ISE
MMCHS_RSP10	MMCHS_RSP32	MMCHS_RSP54
MMCHS_RSP76	MMCHS_CMD	

Table 24-46. Subprocess Call Summary for Main Sequence – Command Transfer Flow With Interrupts

Subprocess Name	Cross-Reference
Perform CMD line reset.	Section 24.5.1.2.1.1.1

24.5.1.2.1.7.2 MMCHS Clock Frequency Change

Figure 24-48 shows the different steps that allow changing the MMC/SD/SDIO output clock frequency.

Figure 24-48. MMC/SD/SDIO Controller Clock Frequency Change Flow

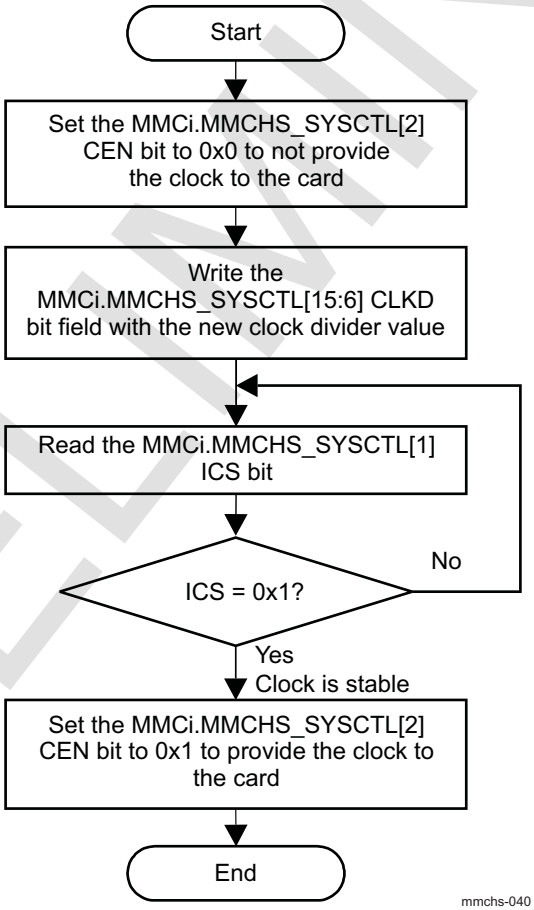

Table 24-47. Register Call Summary for Main Sequence – Clock Frequency Change Flow

Register Name
MMCHS_SYSCTL

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24.5.1.2.1.7.3 Bus Width Selection

Figure 24-49 shows the different steps that allow changing the MMC/SD/SDIO bus width.

Figure 24-49. MMC/SD/SDIO Controller Bus Width Configuration Flow

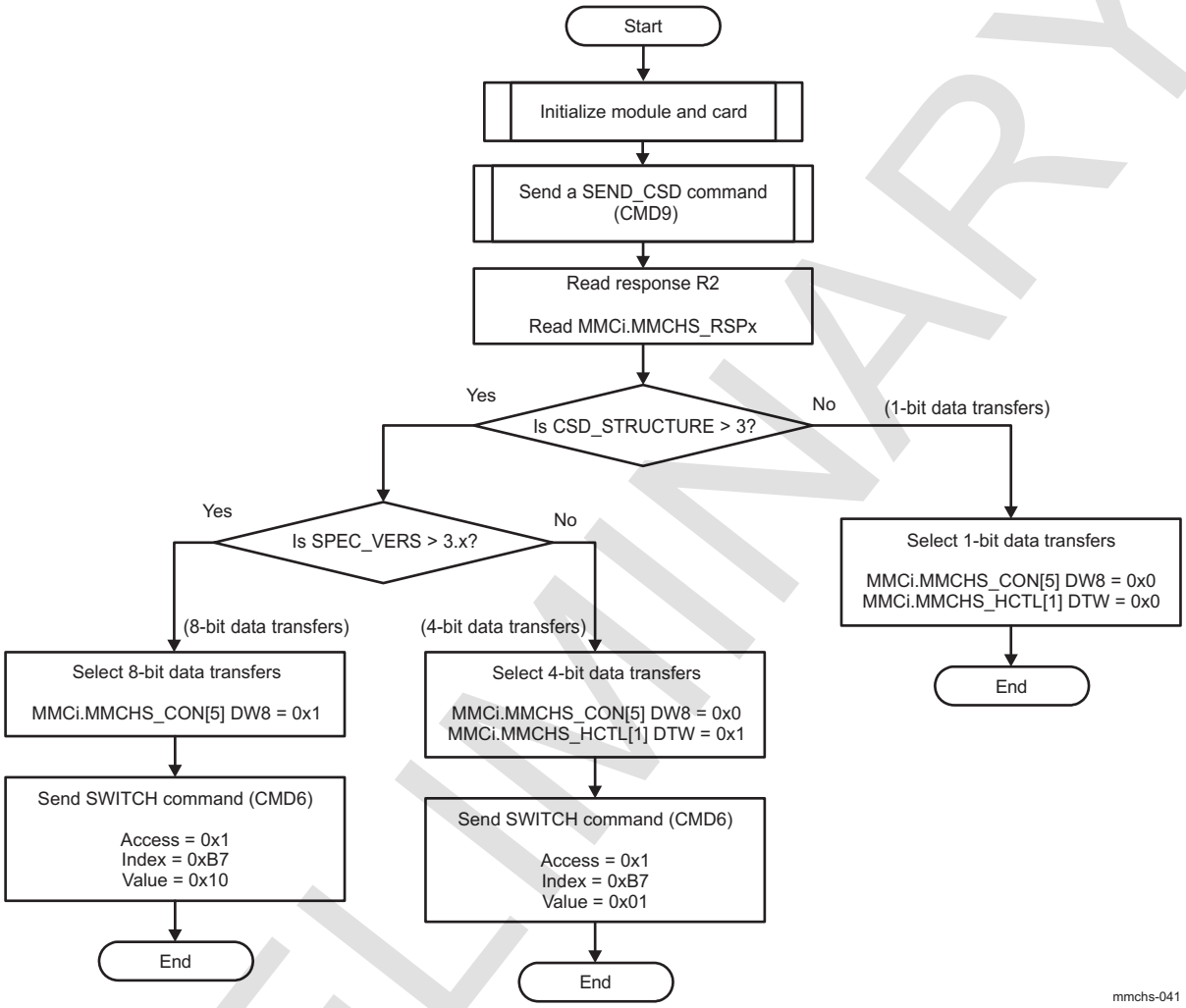

Table 24-48. Register Call Summary for Main Sequence – Bus Width Configuration Flow

Register Name	Register Name	Register Name
MMCHS_RSP10	MMCHS_RSP32	MMCHS_RSP54
MMCHS_RSP76	MMCHS_CON	MMCHS_HCTL

Table 24-49. Subprocess Call Summary for Main Sequence – Bus Width Configuration Flow

Subprocess Name	Cross-Reference
Initialize module and card.	Section 24.5.1.1.2 Section 24.5.1.2.1.1
Send a SEND_CSD command (CMD9).	Section 24.5.1.2.1.7.1
Send SWITCH command (CMD6).	Section 24.5.1.2.1.7.1

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24.5.1.2.2 Bus Voltage Selection

The MMC/SD/SDIO1 controller can operate with two types of card voltages: 1.8 V and 3.0 V. For this reason, dual voltage pads are implemented on this interface. For technological concerns, those pads must have an internal bias voltage reference to operate. The PBIAS module supplies this bias voltage, depending on the settings of the CONTROL.CONTROL_PBIAS_LITE register.

For more information about the PBIAS_LITE cell, see Section 18.4.9, *Extended-Drain I/O and PBIAS Cell*, in Chapter 18, *Control Module*.

For the steps involved in transitioning from 1.8 V to 3.0 V and from 3.0 V to 1.8 V, applicable to the MMC/SD/SDIO1 controller, see Section 18.5.1.2.2, *Extended-Drain I/Os and PBIAS Cell Programming Guide*, in Chapter 18, *Control Module*.

CAUTION

The BIAS voltage must be set using the procedure described in Section 18.5.1.2.2, *Extended-Drain I/Os and PBIAS Cell Programming Guide*, in Chapter 18, *Control Module*. Failure to follow this procedure can damage the MMCHS interface.

Figure 24-50 shows how to configure the MMCHS controller to fit with power switching sequence.

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Figure 24-50. MMC/SD/SDIO Power Switching Procedure

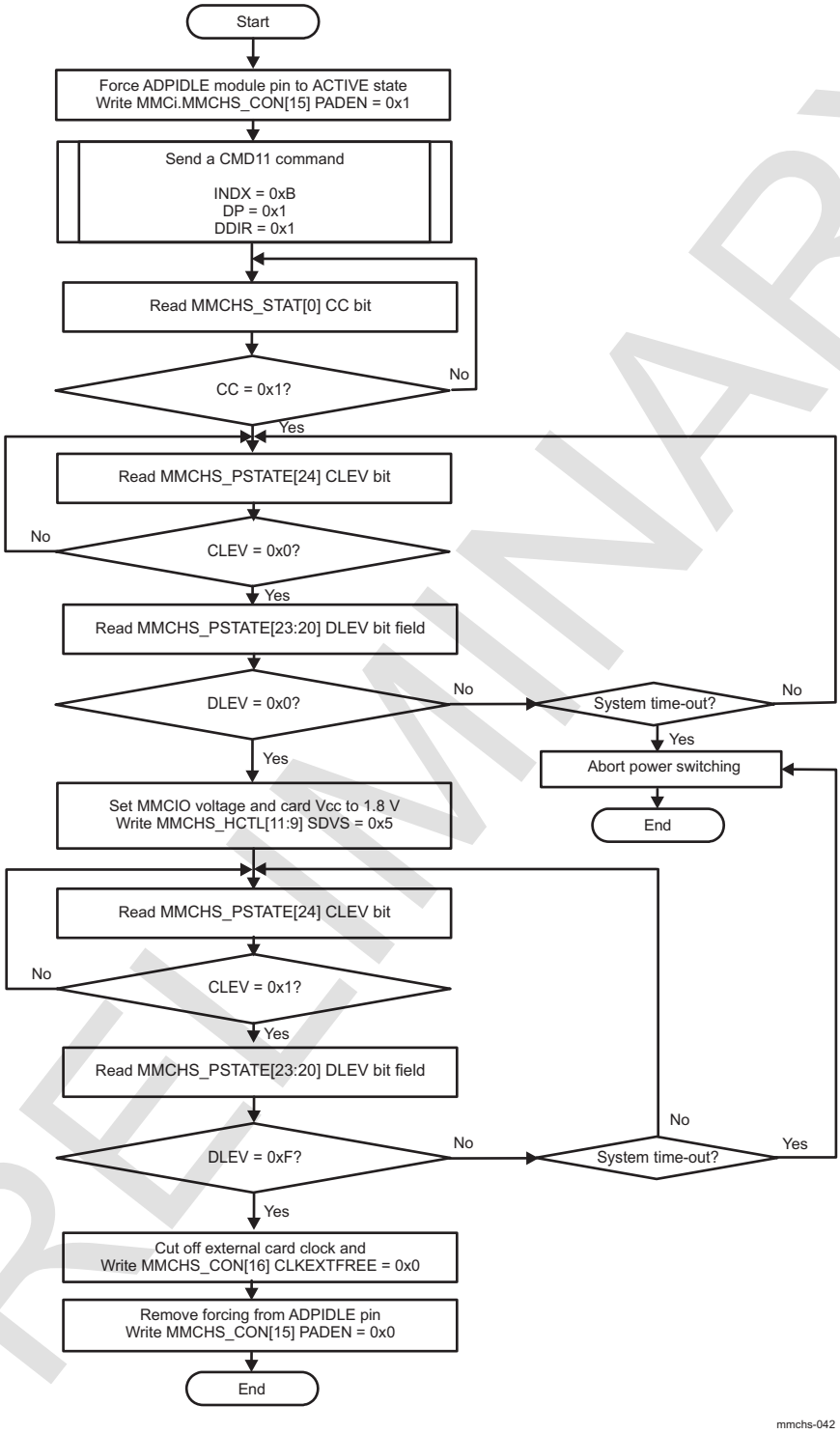

Table 24-50. Register Call Summary for Main Sequence – Power Switching Procedure

Register Name	Register Name
MMCHS_STAT	MMCHS_PSTATE
MMCHS_CMD	MMCHS_CON

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Table 24-51. Subprocess Call Summary for Main Sequence – Power Switching Procedure

Subprocess Name	Cross-Reference
Send a READ_DAT_UNTIL_STOP command (CMD11).	Section 24.5.1.2.1.7.1

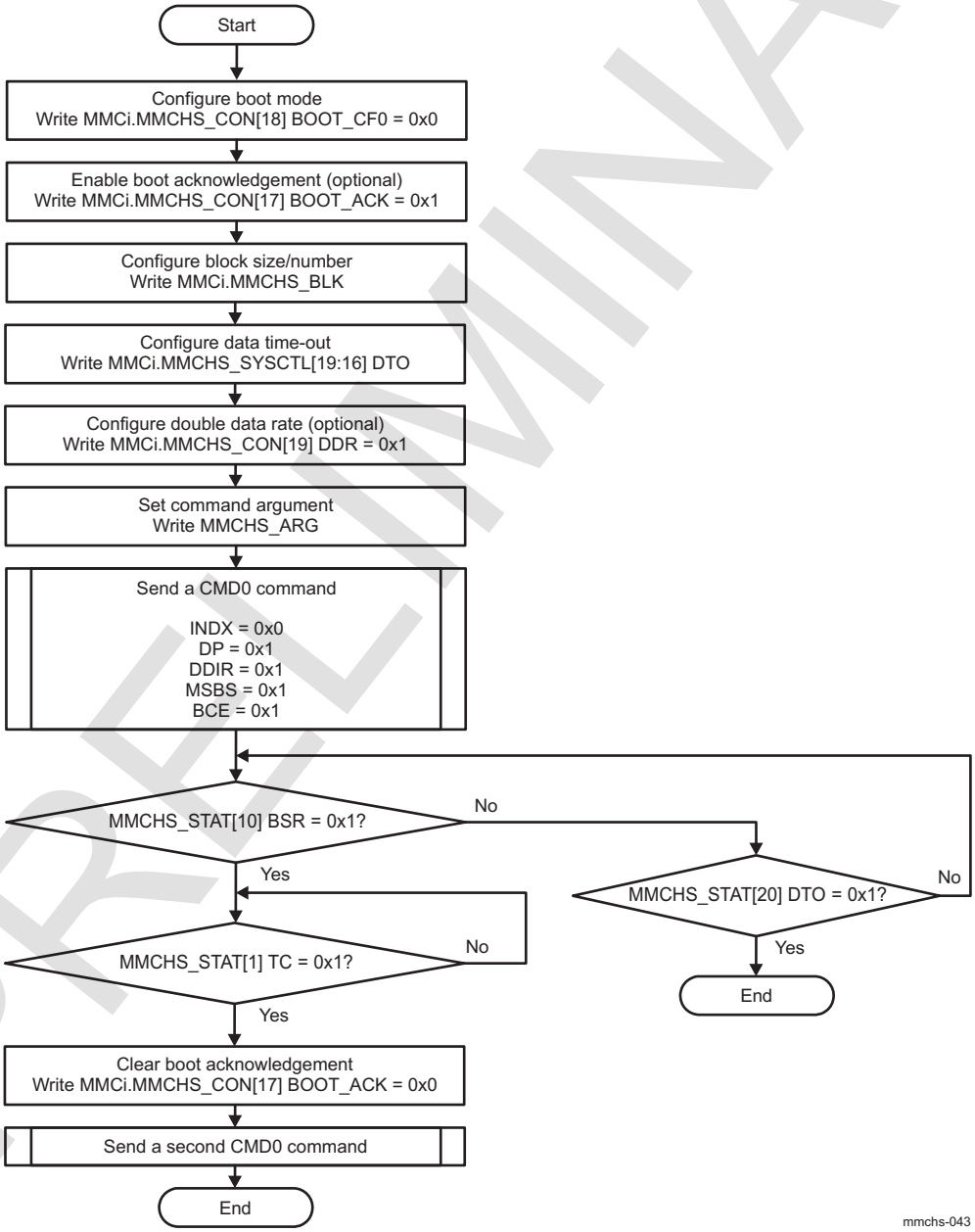
24.5.1.2.3 Boot Mode Configuration

The following sections describe the two possible ways to issue a boot command: issue a CMD0 or drive the CMD line to 0 during the whole boot phase.

24.5.1.2.3.1 Boot Using CMD0

Figure 24-51 shows the necessary steps to configure the controller boot mode using CMD0.

Figure 24-51. MMC/SD/SDIO Controller Boot Using CMD0



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To abort a boot sequence, the system must issue a CMD0 with the MMCHS_CMD[23:22] CMD_TYPE bit field set to 0x3 (the MMCHS_CON[17] BOOT_ACK bit previously cleared to 0x0) during the transfer to abort the transfer and enable the card to exit from boot state.

Table 24-52. Register Call Summary for Main Sequence – Boot Using CMD0

Register Name	Register Name	Register Name
MMCHS_CON	MMCHS_BLK	MMCHS_SYSCTL
MMCHS_ARG	MMCHS_STAT	

Table 24-53. Subprocess Call Summary for Main Sequence – Boot Using CMD0

Subprocess Name	Cross-Reference
Send a CMD0 command.	Section 24.5.1.2.1.7.1

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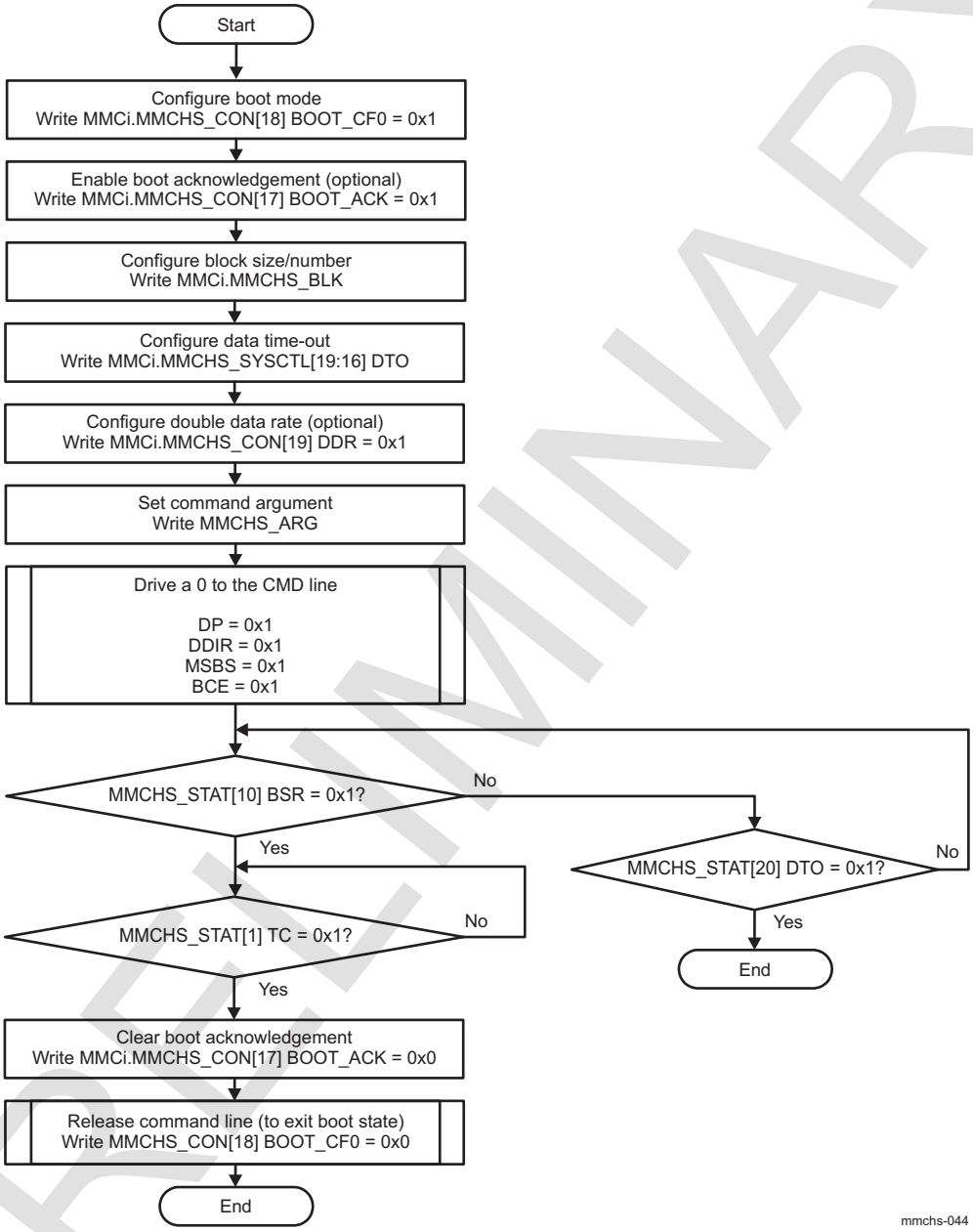
24.5.1.2.3.2 Boot With CMD Line Tied to 0

Figure 24-52 shows the necessary steps to configure the controller in this mode; the driver must follow this sequence.

Figure 24-52. MMC/SD/SDIO Controller Boot With CMD Line Tied to 0



To abort the boot sequence, the system must clear the MMCHS_CON[18] BOOT_CF0 bit to 0x0 during the transfer to abort the transfer and enable the card to exit from boot state.

Table 24-54. Register Call Summary for Main Sequence – Boot Using CMD0

Register Name	Register Name	Register Name
MMCHS_CON	MMCHS_BLK	MMCHS_SYSCTL
MMCHS_ARG	MMCHS_STAT	MMCHS_CMD

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Table 24-55. Subprocess Call Summary for Main Sequence – Boot Using CMD0

Subprocess Name	Cross-Reference
Send a CMD0 command.	Section 24.5.1.2.1.7.1

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24.6 MMC/SD/SDIO Register Manual

24.6.1 MMC/SD/SDIO Instance Summary

Table 24-56. MMC/SD/SDIO Instance Summary

Module Name	Base Address	Size
MMCHS1	0x4809 C000	4KB
MMCHS2	0x480B 4000	4KB
MMCHS3	0x480A D000	4KB
MMCHS4	0x480D 1000	4KB
MMCHS5	0x480D 5000	4KB

24.6.2 MMC/SD/SDIO Registers

24.6.2.1 MMC/SD/SDIO Register Summary

Table 24-57. MMC/SD/SDIO Registers Mapping Summary 1

Register Name	Type	Register Width (Bits)	Address Offset	MMCHS1 Physical Address	MMCHS2 Physical Address	MMCHS3 Physical Address
MMCHS_HL_REV	R	32	0x0000 0000	0x4809 C000	0x480B 4000	0x480A D000
MMCHS_HL_HWINFO	R	32	0x0000 0004	0x4809 C004	0x480B 4004	0x480A D004
MMCHS_HL_SYSCONFIG	RW	32	0x0000 0010	0x4809 C010	0x480B 4010	0x480A D010
MMCHS_SYSCONFIG	RW	32	0x0000 0110	0x4809 C110	0x480B 4110	0x480A D110
MMCHS_SYSSTATUS	R	32	0x0000 0114	0x4809 C114	0x480B 4114	0x480A D114
MMCHS_CSRE	RW	32	0x0000 0124	0x4809 C124	0x480B 4124	0x480A D124
MMCHS_SYSTEST	RW	32	0x0000 0128	0x4809 C128	0x480B 4128	0x480A D128
MMCHS_CON	RW	32	0x0000 012C	0x4809 C12C	0x480B 412C	0x480A D12C
MMCHS_PWCNT	RW	32	0x0000 0130	0x4809 C130	0x480B 4130	0x480A D130
RESERVED	R	32	0x0000 0200	0x4809 C200	0x480B 4200	0x480A D200
MMCHS_BLK	RW	32	0x0000 0204	0x4809 C204	0x480B 4204	0x480A D204
MMCHS_ARG	RW	32	0x0000 0208	0x4809 C208	0x480B 4208	0x480A D208
MMCHS_CMD	RW	32	0x0000 020C	0x4809 C20C	0x480B 420C	0x480A D20C
MMCHS_RSP10	R	32	0x0000 0210	0x4809 C210	0x480B 4210	0x480A D210
MMCHS_RSP32	R	32	0x0000 0214	0x4809 C214	0x480B 4214	0x480A D214
MMCHS_RSP54	R	32	0x0000 0218	0x4809 C218	0x480B 4218	0x480A D218
MMCHS_RSP76	R	32	0x0000 021C	0x4809 C21C	0x480B 421C	0x480A D21C
MMCHS_DATA	RW	32	0x0000 0220	0x4809 C220	0x480B 4220	0x480A D220
MMCHS_PSTATE	R	32	0x0000 0224	0x4809 C224	0x480B 4224	0x480A D224
MMCHS_HCTL	RW	32	0x0000 0228	0x4809 C228	0x480B 4228	0x480A D228
MMCHS_SYSCTL	RW	32	0x0000 022C	0x4809 C22C	0x480B 422C	0x480A D22C
MMCHS_STAT	RW	32	0x0000 0230	0x4809 C230	0x480B 4230	0x480A D230
MMCHS_IE	RW	32	0x0000 0234	0x4809 C234	0x480B 4234	0x480A D234
MMCHS_ISE	RW	32	0x0000 0238	0x4809 C238	0x480B 4238	0x480A D238
MMCHS_AC12	R	32	0x0000 023C	0x4809 C23C	0x480B 423C	0x480A D23C
MMCHS_CAPA	RW	32	0x0000 0240	0x4809 C240	0x480B 4240	0x480A D240
MMCHS_CUR_CAPA	RW	32	0x0000 0248	0x4809 C248	0x480B 4248	0x480A D248
MMCHS_FE	RW	32	0x0000 0250	0x4809 C250	0x480B 4250	0x480A D250
MMCHS_ADMAES	RW	32	0x0000 0254	0x4809 C254	0x480B 4254	N/A

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Table 24-57. MMC/SD/SDIO Registers Mapping Summary 1 (continued)

Register Name	Type	Register Width (Bits)	Address Offset	MMCHS1 Physical Address	MMCHS2 Physical Address	MMCHS3 Physical Address
MMCHS_ADMASAL	RW	32	0x0000 0258	0x4809 C258	0x480B 4258	N/A
RESERVED	R	32	0x0000 025C	0x4809 C25C	0x480B 425C	0x480A D25C
MMCHS_REV	R	32	0x0000 02FC	0x4809 C2FC	0x480B 42FC	0x480A D2FC

Table 24-58. MMC/SD/SDIO Registers Mapping Summary 2

Register Name	Type	Register Width (Bits)	Address Offset	MMCHS4 Physical Address	MMCHS5 Physical Address
MMCHS_HL_REV	R	32	0x0000 0000	0x480D 1000	0x480D 5000
MMCHS_HL_HWINFO	R	32	0x0000 0004	0x480D 1004	0x480D 5004
MMCHS_HL_SYSCONFIG	RW	32	0x0000 0010	0x480D 1010	0x480D 5010
MMCHS_SYSCONFIG	RW	32	0x0000 0110	0x480D 1110	0x480D 5110
MMCHS_SYSSTATUS	R	32	0x0000 0114	0x480D 1114	0x480D 5114
MMCHS_CSRE	RW	32	0x0000 0124	0x480D 1124	0x480D 5124
MMCHS_SYSTEST	RW	32	0x0000 0128	0x480D 1128	0x480D 5128
MMCHS_CON	RW	32	0x0000 012C	0x480D 112C	0x480D 512C
MMCHS_PWCNT	RW	32	0x0000 0130	0x480D 1130	0x480D 5130
RESERVED	R	32	0x0000 0200	0x480D 1200	0x480D 5200
MMCHS_BLK	RW	32	0x0000 0204	0x480D 1204	0x480D 5204
MMCHS_ARG	RW	32	0x0000 0208	0x480D 1208	0x480D 5208
MMCHS_CMD	RW	32	0x0000 020C	0x480D 120C	0x480D 520C
MMCHS_RSP10	R	32	0x0000 0210	0x480D 1210	0x480D 5210
MMCHS_RSP32	R	32	0x0000 0214	0x480D 1214	0x480D 5214
MMCHS_RSP54	R	32	0x0000 0218	0x480D 1218	0x480D 5218
MMCHS_RSP76	R	32	0x0000 021C	0x480D 121C	0x480D 521C
MMCHS_DATA	RW	32	0x0000 0220	0x480D 1220	0x480D 5220
MMCHS_PSTATE	R	32	0x0000 0224	0x480D 1224	0x480D 5224
MMCHS_HCTL	RW	32	0x0000 0228	0x480D 1228	0x480D 5228
MMCHS_SYSCTL	RW	32	0x0000 022C	0x480D 122C	0x480D 522C
MMCHS_STAT	RW	32	0x0000 0230	0x480D 1230	0x480D 5230
MMCHS_IE	RW	32	0x0000 0234	0x480D 1234	0x480D 5234
MMCHS_ISE	RW	32	0x0000 0238	0x480D 1238	0x480D 5238
MMCHS_AC12	R	32	0x0000 023C	0x480D 123C	0x480D 523C
MMCHS_CAPA	RW	32	0x0000 0240	0x480D 1240	0x480D 5240
MMCHS_CUR_CAPA	RW	32	0x0000 0248	0x480D 1248	0x480D 5248
MMCHS_FE	RW	32	0x0000 0250	0x480D 1250	0x480D 5250
MMCHS_ADMAES	R	32	0x0000 0254	N/A	N/A
MMCHS_ADMASAL	RW	32	0x0000 0258	N/A	N/A
RESERVED	R	32	0x0000 025C	0x480D 125C	0x480D 525C
MMCHS_REV	R	32	0x0000 02FC	0x480D 12FC	0x480D 52FC

24.6.2.2 MMC/SD/SDIO Register Description

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Table 24-59. MMCHS_HL_REV

Address Offset	0x0000 0000		
Physical Address	0x4809 C000 0x480B 4000 0x480A D000 0x480D 1000 0x480D 5000	**Instance**	MMCHS1 MMCHS2 MMCHS3 MMCHS4 MMCHS5
Description	IP Revision Identifier (X.Y.R) Used by software to track features, bugs, and compatibility		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP Revision.	R	See(1)

(1) TI internal data.

Table 24-60. Register Call Summary for Register MMCHS_HL_REV

MMC/SD/SDIO Register Manual

- MMC/SD/SDIO Register Summary: [0] [1]

Table 24-61. MMCHS_HL_HWINFO

Address Offset	0x0000 0004		
Physical Address	0x4809 C004 0x480B 4004 0x480A D004 0x480D 1004 0x480D 5004	**Instance**	MMCHS1 MMCHS2 MMCHS3 MMCHS4 MMCHS5
Description	Information about the IP module's hardware configuration, that is, typically the module's HDL generics (if any). Actual field format and encoding is up to the module's designer to decide.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RETMODE	MEM_SIZE					MERGE_MEM	MADMA_EN

Bits	Field Name	Description	Type	Reset
31:7	RESERVED	Reserved	R	0x0000000
6	RETMODE	Retention mode generic parameter This bit field indicates whether the retention mode is supported using the pin PIRFFRET. 0x0: Retention mode disabled 0x1: Retention mode enabled	R	See Table 24-63.

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Bits	Field Name	Description	Type	Reset
5:2	MEM_SIZE	Memory size for FIFO buffer: Read 0x1: Memory of 512 bytes, max block length is 512 bytes Read 0x2: Memory of 1024 bytes, max block length is 1024 bytes Read 0x4: Memory of 2048 bytes, max block length is 2048 bytes Read 0x8: Memory of 4096 bytes, max block length is 2048 bytes	R	0x2
1	MERGE_MEM	Memory merged for FIFO buffer: This register defines the configuration of FIFO buffer architecture. If the bit is set STA and DFT shall support clock multiplexing and balancing. Read 0x0: 2 memories instantiated, one per data transfer direction. Read 0x1: A single memory is used with multiplexed addresses, data and clocks.	R	0
0	MADMA_EN	Master DMA enabled generic parameter: This register defines the configuration of the controller to know if it supports the master DMA management called ADMA. Read 0x0: No Master DMA (ADMA) management supported Read 0x1: Controller supports ADMA	R	Please refer to Table 24-64

Table 24-62. Register Call Summary for Register MMCHS_HL_HWINFO

MMC/SD/SDIO Functional Description • DMA Modes: [0] [1] • Master DMA Operations: [2] • Slave DMA Operations: [3] • Memory Size, Block Length, and Buffer-Management Relationship: [4] • Retention Mode: [5]
MMC/SD/SDIO Register Manual • MMC/SD/SDIO Register Summary: [6] [7] • MMC/SD/SDIO Register Description: [8] [9] [10] [11] [12]

Table 24-63. Reset value for MMCHS_HL_HWINFO

Instance	RETMODE
MMCHS1	1
MMCHS2	1
MMCHS3	0
MMCHS4	0
MMCHS5	0

Table 24-64. Reset value for MADMA_EN

Instance	RETMODE
MMCHS1	1
MMCHS2	1
MMCHS3	0
MMCHS4	0
MMCHS5	0

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Table 24-65. MMCHS_HL_SYSCONFIG

Address Offset	0x0000 0010		
Physical Address	0x4809 C010 0x480B 4010 0x480A D010 0x480D 1010 0x480D 5010	**Instance**	MMCHS1 MMCHS2 MMCHS3 MMCHS4 MMCHS5
Description	Clock management configuration		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								STANDBYMODE		IDLEMODE		FREEEMU		SOFTRESET	

Bits	Field Name	Description	Type	Reset
31:6	RESERVED		R	0x0000000
5:4	STANDBYMODE	Configuration of the local initiator state management mode. By definition, initiator may generate read/write transaction as long as it is out of STANDBY state. 0x0: Force-standby mode: local initiator is unconditionally placed in standby state.Backup mode, for debug only. 0x1: No-standby mode: local initiator is unconditionally placed out of standby state.Backup mode, for debug only. 0x2: Smart-standby mode: local initiator standby status depends on local conditions, that is, the module's functional requirement from the initiator.IP module shall not generate (initiator-related) wakeup events. 0x3: Smart-Standby wakeup-capable mode: local initiator standby status depends on local conditions, that is, the module's functional requirement from the initiator. IP module may generate (master-related) wakeup events when in standby state.Mode is only relevant if the appropriate IP module "mwakeup" output is implemented.	RW	0x2
3:2	IDLEMODE	Configuration of the local target state management mode. By definition, target can handle read/write transaction as long as it is out of IDLE state. 0x0: Force-idle mode: local target's idle state follows (acknowledges) the system's idle requests unconditionally, that is, regardless of the IP module's internal requirements.Backup mode, for debug only. 0x1: No-idle mode: local target never enters idle state.Backup mode, for debug only. 0x2: Smart-idle mode: local target's idle state eventually follows (acknowledges) the system's idle requests, depending on the IP module's internal requirements.IP module shall not generate (IRQ- or DMA-request-related) wakeup events. 0x3: Smart-idle wakeup-capable mode: local target's idle state eventually follows (acknowledges) the system's idle requests, depending on the IP module's internal requirements.IP module may generate (IRQ- or DMA-request-related) wakeup events when in idle state.Mode is only relevant if the appropriate IP module "swakeup" output(s) is (are) implemented.	RW	0x2

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Bits	Field Name	Description	Type	Reset
1	FREEEMU	Sensitivity to emulation (debug) suspend input signal. Functionality NOT implemented in MMCHS. 0x0: IP module is sensitive to emulation suspend 0x1: IP module is not sensitive to emulation suspend	RW	0
0	SOFTRESET	Software reset. (Optional) Write 0x0: No action Read 0x0: Reset done, no pending action Read 0x1: Reset (software or other) ongoing Write 0x1: Initiate software reset	RW	0

Table 24-66. Register Call Summary for Register MMCHS_HL_SYSCONFIG

MMC/SD/SDIO Register Manual
- MMC/SD/SDIO Register Summary: [0] [1]

Table 24-67. MMCHS_SYSCONFIG

Address Offset	0x0000 0110		
Physical Address	0x4809 C110 0x480B 4110 0x480A D110 0x480D 1110 0x480D 5110	**Instance**	MMCHS1 MMCHS2 MMCHS3 MMCHS4 MMCHS5
Description	System Configuration Register This register allows controlling various parameters of the Interconnect interface.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																		STANDBYMODE		RESERVED		CLOCKACTIVITY		RESERVED		RESERVED		SIDLEMODE		ENAWAKEUP		SOFTRESET		AUTOIDLE

Bits	Field Name	Description	Type	Reset
31:14	RESERVED	Reserved These bits are initialized to zero, and writes to them are ignored. Reads return 0.	R	0x00000

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Bits	Field Name	Description	Type	Reset
13:12	STANDBYMODE	Master interface power Management, standby/wait control. The bit field is only useful when generic parameter MMCHS_HL_HWINFO[0] MADMA_EN (Master ADMA enable) is set as active, otherwise it is a read only register read a 0. 0x0: Force-standby. Mstandby is forced unconditionnaly. 0x1: No-standby. Mstandby is never asserted. 0x2: Smart-standby mode: local initiator standby status depends on local conditions, that is, the module's functional requirement from the initiator.IP module shall not generate (initiator-related) wakeup events. 0x3: Smart-Standby wakeup-capable mode: local initiator standby status depends on local conditions, that is, the module's functional requirement from the initiator. IP module may generate (master-related) wakeup events when in standby state.Mode is only relevant if the appropriate IP module "mwakeup" output is implemented.	RW	0x0
11:10	RESERVED	Reserved These bits are initialized to zero, and writes to them are ignored. Reads return 0.	R	0x0
9:8	CLOCKACTIVITY	Clocks activity during wake up mode period. Bit8: Interface clock Bit9: Functional clock 0x0: Interface and Functional clock may be switched off. 0x1: Interface clock is maintained. Functional clock may be switched-off. 0x2: Functional clock is maintained. Interface clock may be switched-off. 0x3: Interface and Functional clocks are maintained.	RW	0x0
7	RESERVED	Reserved This bit is initialized to zero, and writes to it are ignored. Reads return 0.	R	0
6	RESERVED	Reserved - EmuSoft not supported This bit is initialized to zero, and writes to it are ignored. Reads return 0.	R	0
5	RESERVED	Reserved - EmuFree not supported This bit is initialized to zero, and writes to it are ignored. Reads return 0.	R	0
4:3	SIDLEMODE	Power management 0x0: If an idle request is detected, the MMCHS acknowledges it unconditionally and goes in Inactive mode. Interrupt and DMA requests are unconditionally de-asserted. 0x1: If an idle request is detected, the request is ignored and the module keeps on behaving normally. 0x2: Smart-idle mode: local target's idle state eventually follows (acknowledges) the system's idle requests, depending on the IP module's internal requirements.IP module shall not generate (IRQ- or DMA-request-related) wakeup events. 0x3: Smart-idle wakeup-capable mode: local target's idle state eventually follows (acknowledges) the system's idle requests, depending on the IP module's internal requirements.IP module may generate (IRQ- or DMA-request-related) wakeup events when in idle state.Mode is only relevant if the appropriate IP module "swakeup" output(s) is (are) implemented.	RW	0x2

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Bits	Field Name	Description	Type	Reset
2	ENAWAKEUP	Wakeup feature control 0x0: Wakeup capability is disabled 0x1: Wakeup capability is enabled	RW	1
1	SOFTRESET	Software reset. The bit is automatically reset by the hardware. During reset, it always returns 0. Read 0x0: Normal mode Write 0x0: No effect. Write 0x1: Trigger a module reset. Read 0x1: The module is reset.	RW	0
0	AUTOIDLE	Internal Clock gating strategy 0x0: Clocks are free-running 0x1: Automatic clock gating strategy is applied, based on the Interconnect and MMC interface activity	RW	1

Table 24-68. Register Call Summary for Register MMCHS_SYSCONFIG

MMC/SD/SDIO Functional Description • Software Reset: [0] • Power Management: [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12]
MMC/SD/SDIO Programming Guide • MMC/SD/SDIO Host Controller Initialization Flow: [13] [14] [15]
MMC/SD/SDIO Register Manual • MMC/SD/SDIO Register Summary: [16] [17] • MMC/SD/SDIO Register Description: [18] [19] [20] [21] [22] [23]

Table 24-69. MMCHS_SYSSTATUS

Address Offset	0x0000 0114		
Physical Address	0x4809 C114 0x480B 4114 0x480A D114 0x480D 1114 0x480D 5114	**Instance**	MMCHS1 MMCHS2 MMCHS3 MMCHS4 MMCHS5
Description	System Status Register This register provides status information about the module excluding the interrupt status information		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															RESETDONE

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved These bits are initialized to zero, and writes to them are ignored. Reads return 0.	R	0x0000 0000

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Bits	Field Name	Description	Type	Reset
0	RESETDONE	Internal Reset Monitoring Note: the debounce clock , the system clock (Interface) and the functional clock shall be provided to the MMC/SD/SDIO host controller to allow the internal reset monitoring. Read 0x0: Internal module reset is on-going Read 0x1: Reset completed.	R	0

Table 24-70. Register Call Summary for Register MMCHS_SYSSTATUS

MMC/SD/SDIO Functional Description
- Hardware Reset: [0]
- Software Reset: [1]

MMC/SD/SDIO Programming Guide
- MMC/SD/SDIO Host Controller Initialization Flow: [2]

MMC/SD/SDIO Register Manual
- MMC/SD/SDIO Register Summary: [3] [4]

Table 24-71. MMCHS_CSRE

Address Offset	0x0000 0124		
Physical Address	0x4809 C124 0x480B 4124 0x480A D124 0x480D 1124 0x480D 5124	**Instance**	MMCHS1 MMCHS2 MMCHS3 MMCHS4 MMCHS5
Description	Card status response error This register enables the host controller to detect card status errors of response type R1, R1b for all cards and of R5, R5b and R6 response for cards types SD or SDIO. When a bit MMCHS_CSRE[i] is set to 1, if the corresponding bit at the same position in the response MMCHS_RSP10[i] is set to 1, the host controller indicates a card error (MMCHS_STAT[CERR]) interrupt status to avoid the host driver reading the response register (MMCHS_RSP10). Note: No automatic card error detection for autoCMD12 is implemented; the host system has to check autoCMD12 response register (MMCHS_RSP76) for possible card errors.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CSRE																															

Bits	Field Name	Description	Type	Reset
31:0	CSRE	Card status response error	RW	0x0000 0000

Table 24-72. Register Call Summary for Register MMCHS_CSRE

MMC/SD/SDIO Functional Description
- Interrupt Requests: [0]

MMC/SD/SDIO Programming Guide
- Basic Operations for MMC/SD/SDIO Host Controller: [1] [2]

MMC/SD/SDIO Register Manual
- MMC/SD/SDIO Register Summary: [3] [4]
- MMC/SD/SDIO Register Description: [5] [6]

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Table 24-73. MMCHS_SYSTEST

Address Offset	0x0000 0128		
Physical Address	0x4809 C128 0x480B 4128 0x480A D128 0x480D 1128 0x480D 5128	**Instance**	MMCHS1 MMCHS2 MMCHS3 MMCHS4 MMCHS5
Description	System Test register This register is used to control the signals that connect to I/O pins when the module is configured in system test (SYSTEST) mode for boundary connectivity verification. Note: In SYSTEST mode, a write into MMCHS_CMD register will not start a transfer. The buffer behaves as a stack accessible only by the local host (push and pop operations). In this mode, the Transfer Block Size (MMCHS_BLK[11:0] BLEN) and the Blocks count for current transfer (MMCHS_BLK[31:16] NBLK) are needed to generate a Buffer write ready interrupt (MMCHS_STAT[4] BWR) or a Buffer read ready interrupt (MMCHS_STAT[5] BRR) and DMA requests if enabled.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															OBI	SDCD	SDWP	WAKD	SSB	D7D	D6D	D5D	D4D	D3D	D2D	D1D	D0D	DDIR	CDAT	CDIR	MCKD

Bits	Field Name	Description	Type	Reset
31:17	RESERVED	Reserved These bits are initialized to zero, and writes to them are ignored. Reads return 0.	R	0x0000
16	OBI	Out-Of-Band Interrupt (OBI) data value Read 0x0: The Out-of-Band Interrupt pin is driven low. Read 0x1: The Out-of-Band Interrupt pin is driven high.	RW	0
15	SDCD	Card detect input signal (SDCD) data value Read 0x0: The card detect pin is driven low. Read 0x1: The card detect pin is driven high.	R	0
14	SDWP	Write protect input signal (SDWP) data value Read 0x0: The write protect pin SDWP is driven low. Read 0x1: The write protect pin SDWP is driven high.	R	0
13	WAKD	Wake request output signal data value Write 0x0: The pin SWAKEUP is driven low. Read 0x0: No action. Returns 0. Write 0x1: The pin SWAKEUP is driven high. Read 0x1: No action. Returns 1.	RW	0
12	SSB	Set status bit This bit must be cleared prior attempting to clear a status bit of the interrupt status register (MMCHS_STAT). Write 0x0: Clear this SSB bit field. Writing 0 does not clear already set status bits; Read 0x0: No action. Returns 0. Read 0x1: No action. Returns 1. Write 0x1: Force to 1 all status bits of the interrupt status register (MMCHS_STAT) only if the corresponding bit field in the Interrupt signal enable register (MMCHS_ISE) is set.	RW	0

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Bits	Field Name	Description	Type	Reset
11	D7D	DAT7 input/output signal data value Read 0x0: If MMCHS_SYSTEST[3] DDIR = 1 (input mode direction), returns the value on the DAT7 line (low). If MMCHS_SYSTEST[3] DDIR = 0 (output mode direction), returns 0 Write 0x0: If MMCHS_SYSTEST[3] DDIR = 0 (output mode direction), the DAT7 line is driven low. If MMCHS_SYSTEST[3] DDIR = 1 (input mode direction), no effect. Read 0x1: If MMCHS_SYSTEST[3] DDIR = 1 (input mode direction), returns the value on the DAT7 line (high) If MMCHS_SYSTEST[3] DDIR = 0 (output mode direction), returns 1 Write 0x1: If MMCHS_SYSTEST[3] DDIR = 0 (output mode direction), the DAT7 line is driven high. If MMCHS_SYSTEST[3] DDIR = 1 (input mode direction), no effect.	RW	0
10	D6D	DAT6 input/output signal data value Read 0x0: If SYSTEST[DDIR] = 1 (input mode direction), returns the value on the DAT6 line (low). If MMCHS_SYSTEST[3] DDIR = 0 (output mode direction), returns 0 Write 0x0: If MMCHS_SYSTEST[3] DDIR = 0 (output mode direction), the DAT6 line is driven low. If MMCHS_SYSTEST[3] DDIR = 1 (input mode direction), no effect. Read 0x1: If MMCHS_SYSTEST[3] DDIR = 1 (input mode direction), returns the value on the DAT6 line (high) If MMCHS_SYSTEST[3] DDIR = 0 (output mode direction), returns 1 Write 0x1: If MMCHS_SYSTEST[3] DDIR = 0 (output mode direction), the DAT6 line is driven high. If MMCHS_SYSTEST[3] DDIR = 1 (input mode direction), no effect.	RW	0
9	D5D	DAT5 input/output signal data value Read 0x0: If MMCHS_SYSTEST[3] DDIR = 1 (input mode direction), returns the value on the DAT5 line (low). If MMCHS_SYSTEST[3] DDIR = 0 (output mode direction), returns 0 Write 0x0: If MMCHS_SYSTEST[3] DDIR = 0 (output mode direction), the DAT5 line is driven low. If MMCHS_SYSTEST[3] DDIR = 1 (input mode direction), no effect. Read 0x1: If MMCHS_SYSTEST[3] DDIR = 1 (input mode direction), returns the value on the DAT5 line (high) If MMCHS_SYSTEST[3] DDIR = 0 (output mode direction), returns 1 Write 0x1: If MMCHS_SYSTEST[3] DDIR = 0 (output mode direction), the DAT5 line is driven high. If MMCHS_SYSTEST[3] DDIR = 1 (input mode direction), no effect.	RW	0

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Bits	Field Name	Description	Type	Reset
8	D4D	DAT4 input/output signal data value Write 0x0: If MMCHS_SYSTEST[3] DDIR = 0 (output mode direction), the DAT4 line is driven low. If MMCHS_SYSTEST[3] DDIR = 1 (input mode direction), no effect. Read 0x0: If MMCHS_SYSTEST[3] DDIR = 1 (input mode direction), returns the value on the DAT4 line (low). If MMCHS_SYSTEST[3] DDIR = 0 (output mode direction), returns 0 Write 0x1: If MMCHS_SYSTEST[3] DDIR = 0 (output mode direction), the DAT4 line is driven high. If MMCHS_SYSTEST[3] DDIR = 1 (input mode direction), no effect. Read 0x1: If MMCHS_SYSTEST[3] DDIR = 1 (input mode direction), returns the value on the DAT4 line (high) If MMCHS_SYSTEST[3] DDIR = 0 (output mode direction), returns 1	RW	0
7	D3D	DAT3 input/output signal data value Write 0x0: If MMCHS_SYSTEST[3] DDIR = 0 (output mode direction), the DAT3 line is driven low. If MMCHS_SYSTEST[3] DDIR = 1 (input mode direction), no effect. Read 0x0: If MMCHS_SYSTEST[3] DDIR = 1 (input mode direction), returns the value on the DAT3 line (low). If MMCHS_SYSTEST[3] DDIR = 0 (output mode direction), returns 0 Read 0x1: If MMCHS_SYSTEST[3] DDIR = 1 (input mode direction), returns the value on the DAT3 line (high) If MMCHS_SYSTEST[3] DDIR = 0 (output mode direction), returns 1 Write 0x1: If MMCHS_SYSTEST[3] DDIR = 0 (output mode direction), the DAT3 line is driven high. If MMCHS_SYSTEST[3] DDIR = 1 (input mode direction), no effect.	RW	0
6	D2D	DAT2 input/output signal data value Write 0x0: If MMCHS_SYSTEST[3] DDIR = 0 (output mode direction), the DAT2 line is driven low. If MMCHS_SYSTEST[3] DDIR = 1 (input mode direction), no effect. Read 0x0: If MMCHS_SYSTEST[3] DDIR = 1 (input mode direction), returns the value on the DAT2 line (low). If MMCHS_SYSTEST[3] DDIR = 0 (output mode direction), returns 0 Write 0x1: If MMCHS_SYSTEST[3] DDIR = 0 (output mode direction), the DAT2 line is driven high. If MMCHS_SYSTEST[3] DDIR = 1 (input mode direction), no effect. Read 0x1: If MMCHS_SYSTEST[3] DDIR = 1 (input mode direction), returns the value on the DAT2 line (high) If MMCHS_SYSTEST[3] DDIR = 0 (output mode direction), returns 1	RW	0

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Bits	Field Name	Description	Type	Reset
5	D1D	DAT1 input/output signal data value Read 0x0: If MMCHS_SYSTEST[3] DDIR = 1 (input mode direction), returns the value on the DAT1 line (low). If MMCHS_SYSTEST[3] DDIR = 0 (output mode direction), returns 0 Write 0x0: If MMCHS_SYSTEST[3] DDIR = 0 (output mode direction), the DAT1 line is driven low. If MMCHS_SYSTEST[3] DDIR = 1 (input mode direction), no effect. Read 0x1: If MMCHS_SYSTEST[3] DDIR = 1 (input mode direction), returns the value on the DAT1 line (high) If MMCHS_SYSTEST[3] DDIR = 0 (output mode direction), returns 1 Write 0x1: If MMCHS_SYSTEST[3] DDIR = 0 (output mode direction), the DAT1 line is driven high. If MMCHS_SYSTEST[3] DDIR = 1 (input mode direction), no effect.	RW	0
4	D0D	DAT0 input/output signal data value Write 0x0: If MMCHS_SYSTEST[3] DDIR = 0 (output mode direction), the DAT0 line is driven low. If MMCHS_SYSTEST[3] DDIR = 1 (input mode direction), no effect. Read 0x0: If MMCHS_SYSTEST[3] DDIR = 1 (input mode direction), returns the value on the DAT0 line (low). If MMCHS_SYSTEST[3] DDIR = 0 (output mode direction), returns 0 Write 0x1: If MMCHS_SYSTEST[3] DDIR = 0 (output mode direction), the DAT0 line is driven high. If MMCHS_SYSTEST[3] DDIR = 1 (input mode direction), no effect. Read 0x1: If MMCHS_SYSTEST[3] DDIR = 1 (input mode direction), returns the value on the DAT0 line (high) If MMCHS_SYSTEST[3] DDIR = 0 (output mode direction), returns 1	RW	0
3	DDIR	Control of the DAT[7:0] pins direction. Write 0x0: The DAT lines are outputs (host to card) Read 0x0: No action. Returns 0. Read 0x1: No action. Returns 1. Write 0x1: The DAT lines are inputs (card to host)	RW	0
2	CDAT	CMD input/output signal data value Write 0x0: If MMCHS_SYSTEST[1] CDIR = 0 (output mode direction), the CMD line is driven low. If MMCHS_SYSTEST[1] CDIR = 1 (input mode direction), no effect. Read 0x0: If MMCHS_SYSTEST[1] CDIR = 1 (input mode direction), returns the value on the CMD line (low). If MMCHS_SYSTEST[1] CDIR = 0 (output mode direction), returns 0 Write 0x1: If MMCHS_SYSTEST[1] CDIR = 0 (output mode direction), the CMD line is driven high. If MMCHS_SYSTEST[1] CDIR = 1 (input mode direction), no effect. Read 0x1: If MMCHS_SYSTEST[1] CDIR = 1 (input mode direction), returns the value on the CMD line (high) If MMCHS_SYSTEST[1] CDIR = 0 (output mode direction), returns 1	RW	0

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Bits	Field Name	Description	Type	Reset
1	CDIR	Control of the CMD pin direction. Read 0x0: No action. Returns 0. Write 0x0: The CMD line is an output (host to card) Read 0x1: No action. Returns 1. Write 0x1: The CMD line is an input (card to host)	RW	0
0	MCKD	MMC clock output signal data value Read 0x0: No action. Returns 0. Write 0x0: The output clock is driven low. Write 0x1: The output clock is driven high. Read 0x1: No action. Returns 1.	RW	0

Table 24-74. Register Call Summary for Register MMCHS_SYSTEST

MMC/SD/SDIO Functional Description

- Test Registers: [0]

MMC/SD/SDIO Register Manual

- MMC/SD/SDIO Register Summary: [1] [2]
- MMC/SD/SDIO Register Description: [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23] [24] [25] [26] [27] [28] [29] [30] [31] [32] [33] [34] [35] [36] [37] [38] [39] [40] [41] [42] [43] [44] [45] [46] [47] [48] [49] [50] [51] [52] [53] [54] [55] [56] [57] [58] [59] [60] [61] [62] [63] [64] [65] [66] [67] [68] [69] [70] [71] [72] [73]

Table 24-75. MMCHS_CON

Address Offset	0x0000 012C		
Physical Address	0x4809 C12C	**Instance**	MMCHS1
	0x480B 412C		MMCHS2
	0x480A D12C		MMCHS3
	0x480D 112C		MMCHS4
	0x480D 512C		MMCHS5
Description	Configuration register This register is used: - to select the functional mode or the SYSTEST mode for any card. - to send an initialization sequence to any card. - to enable the detection on DAT[1] of a card interrupt for SDIO cards only. and also to configure : - specific data and command transfers for MMC cards only. - the parameters related to the card detect and write protect input signals.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										SDMA_LNE	DMA_MNS	DDR	BOOT_CF0	BOOT_ACK	CLKEXTFREE	PADEN	OBIE	OBIP	CEATA	CTPL	DVAL		WPP	CDP	MIT	DW8	MODE	STR	HR	INIT	OD

Bits	Field Name	Description	Type	Reset
31:22	RESERVED	Reserved These bits are initialized to zero, and writes to them are ignored. Reads return 0.	R	0x000

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Bits	Field Name	Description	Type	Reset
21	SDMA_LNE	Slave DMA Level/Edge Request: The waveform of the DMA request can be configured either edge sensitive with early de-assertion on first access to MMCHS_DATA register or late de-assertion, request remains active until last allowed data written into MMCHS_DATA. 0x0: Slave DMA edge sensitive, Early DMA de-assertion 0x1: Slave DMA level sensitive, Late DMA de-assertion	RW	0
20	DMA_MNS	DMA Master or Slave selection: When this bit is set and the controller is configured to use the DMA, Interconnect master interface is used to get datas from system using ADMA2 procedure (direct access to the memory).This option is only available if generic parameter MMCHS_HL_HWINFO[0] MADMA_EN is asserted to 1. 0x0: The controller is slave on data transfers with system. 0x1: The controller is master on data exchange with system, controller must be configured as using DMA.	RW	0
19	DDR	Dual Data Rate mode: When this register is set, the controller uses both clock edge to emit or receive data. Odd bytes are transmitted on falling edges and even bytes are transmitted on rise edges. It only applies on Data bytes and CRC, Start, end bits and CRC status are kept full cycle. This bit field is only meaningful and active for even clock divider ratio of MMCHS_SYSCTL[15:6] CLKD, it is insensitive to MMCHS_HCTL[2] HSPE setting. 0x0: Standard mode : data are transmitted on a single edge depending on MMCHS_HCTL[2] HSPE. 0x1: Data Bytes and CRC are transmitted on both edge.	RW	0
18	BOOT_CF0	Boot status supported: This register is set when the CMD line need to be forced to 0 for a boot sequence. CMD line is driven to 0 after writing in MMCHS_CMD. The line is released when this bit field is de-asserted and abort data transfer in case of a pending transaction. Write 0x0: CMD line is released when it was previously forced to 0 by a boot sequence. Read 0x0: CMD line not forced Read 0x1: CMD line forced to 0 is enabled Write 0x1: CMD line forced to 0 is enabled and will be active after writing into MMCHS_CMD	RW	0
17	BOOT_ACK	Book acknowledge received: When this bit is set the controller should receive a boot status on DAT0 line after next command issued. If no status is received a data timeout will be generated. 0x0: No acknowledge to be received 0x1: A boot status will be received on DAT0 line after issuing a command.	RW	0
16	CLKEXTFREE	External clock free running: This register is used to maintain card clock out of transfer transaction to enable slave module for example to generate a synchronous interrupt on DAT[1]. The Clock will be maintain only if MMCHS_SYSCTL[2] CEN is set. 0x0: External card clock is cut off outside active transaction period. 0x1: External card clock is maintain even out of active transaction period only if MMCHS_SYSCTL[2] CEN is set.	RW	0

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Bits	Field Name	Description	Type	Reset
15	PADEN	Control Power for MMC Lines: This register is only useful when MMC PADs contain power saving mechanism to minimize its leakage power. It works as a GPIO that directly control the ACTIVE pin of PADs. Excepted for DAT[1], the signal is also combine outside the module with the dedicated power control MMCHS_CON[11] CTPL bit. 0x0: ADPIDLE module pin is not forced, it is automatically generated by the MMC fsms. 0x1: ADPIDLE module pin is forced to active state.	RW	0
14	OBIE	Out-of-Band Interrupt Enable MMC cards only: This bit enables the detection of Out-of-Band Interrupt on MMCOBI input pin. The usage of the Out-of-Band signal (OBI) is optional and depends on the system integration. 0x0: Out-of-Band interrupt detection disabled 0x1: Out-of-Band interrupt detection enabled	RW	0
13	OBIP	Out-of-Band Interrupt Polarity MMC cards only: This bit selects the active level of the out-of-band interrupt coming from MMC cards. The usage of the Out-of-Band signal (OBI) is optional and depends on the system integration. 0x0: active high level 0x1: active low level	RW	0
12	CEATA	CE-ATA control mode MMC cards compliant with CE-ATA:By default, this bit is set to 0. It is use to indicate that next commands are considered as specific CE-ATA commands that potentially use 'command completion' features. 0x0: Standard MMC/SD/SDIO mode. 0x1: CE-ATA mode next commands are considered as CE-ATA commands.	RW	0
11	CTPL	Control Power for DAT[1] line MMC and SD cards: By default, this bit is set to 0 and the host controller automatically disables all the input buffers outside of a transaction to minimize the leakage current. SDIO cards: When this bit is set to 1, the host controller automatically disables all the input buffers except the buffer of DAT[1] outside of a transaction in order to detect asynchronous card interrupt on DAT[1] line and minimize the leakage current of the buffers. 0x0: Disable all the input buffers outside of a transaction. 0x1: Disable all the input buffers except the buffer of DAT[1] outside of a transaction.	RW	0
10:9	DVAL	Debounce filter value All cards This register is used to define a debounce period to filter the card detect input signal (SDCD). The usage of the card detect input signal (SDCD) is optional and depends on the system integration and the type of the connector housing that accommodates the card. 0x0: 33 us debounce period 0x1: 231 us debounce period 0x2: 1 ms debounce period 0x3: 8,4 ms debounce period	RW	0x3

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Bits	Field Name	Description	Type	Reset
8	WPP	Write protect polarity For SD and SDIO cards only This bit selects the active level of the write protect input signal (SDWP). The usage of the write protect input signal (SDWP) is optional and depends on the system integration and the type of the connector housing that accommodates the card. 0x0: active high level 0x1: active low level	RW	0
7	CDP	Card detect polarity All cards This bit selects the active level of the card detect input signal (SDCD). The usage of the card detect input signal (SDCD) is optional and depends on the system integration and the type of the connector housing that accommodates the card. 0x0: active high level 0x1: active low level	RW	0
6	MIT	MMC interrupt command Only for MMC cards. This bit must be set to 1, when the next write access to the command register (MMCHS_CMD) is for writing a MMC interrupt command (CMD40) requiring the command timeout detection to be disabled for the command response. 0x0: Command timeout enabled 0x1: Command timeout disabled	RW	0
5	DW8	8-bit mode MMC select For SD/SDIO cards, this bit must be set to 0. For MMC card, this bit must be set following a valid SWITCH command (CMD6) with the correct value and extend CSD index written in the argument. Prior to this command, the MMC card configuration register (CSD and EXT_CSD) must be verified for compliancy with MMC standard specification 4.x (see section 3.6). 0x0: 1-bit or 4-bit Data width (DAT[0] used, MMC, SD cards) 0x1: 8-bit Data width (DAT[7:0] used, MMC cards)	RW	0
4	MODE	Mode select All cards These bits select between Functional mode and SYSTEST mode. 0x0: Functional mode. Transfers to the MMC/SD/SDIO cards follow the card protocol. MMC clock is enabled. MMC/SD transfers are operated under the control of the CMD register. 0x1: SYSTEST mode The signal pins are configured as general-purpose input/output and the 1024-byte buffer is configured as a stack memory accessible only by the local host or system DMA. The pins retain their default type (input, output or in-out). SYSTEST mode is operated under the control of the SYSTEST register.	RW	0

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Bits	Field Name	Description	Type	Reset
3	STR	Stream command Only for MMC cards. This bit must be set to 1 only for the stream data transfers (read or write) of the adtc commands. Stream read is a class 1 command (CMD11: READ_DAT_UNTIL_STOP). Stream write is a class 3 command (CMD20: WRITE_DAT_UNTIL_STOP). 0x0: Block oriented data transfer 0x1: Stream oriented data transfer	RW	0
2	HR	Broadcast host response Only for MMC cards. This register is used to force the host to generate a 48-bit response for bc command type. It can be used to terminate the interrupt mode by generating a CMD40 response by the core (see section 4.3, "Interrupt Mode", in the MMC [1] specification). In order to have the host response to be generated in open drain mode, the register MMCHS_CON[0] OD must be set to 1. When MMCHS_CON[12] CEATA is set to 1 and MMCHS_ARG set to 0x00000000 when writing 0x00000000 into MMCHS_CMD register, the host controller performs a 'command completion signal disable' token that is, CMD line held to 0 during 47 cycles followed by a 1. 0x0: The host does not generate a 48-bit response instead of a command. 0x1: The host generates a 48-bit response instead of a command or a command completion signal disable token.	RW	0
1	INIT	Send initialization stream All cards. When this bit is set to 1, and the card is idle, an initialization sequence is sent to the card. An initialization sequence consists of setting the CMD line to 1 during 80 clock cycles. The initialisation sequence is mandatory - but it is not required to do it through this bit - this bit makes it easier. Clock divider (MMCHS_SYSCTL[15:6] CLKD) should be set to ensure that 80 clock periods are greater than 1ms. (see section 9.3, "Power-Up", in the MMC card specification [1], or section 6.4 in the SD card specification [2]). Note: in this mode, there is no command sent to the card and no response is expected 0x0: The host does not send an initialization sequence. 0x1: The host sends an initialization sequence.	RW	0
0	OD	Card open drain mode. Only for MMC cards. This bit must be set to 1 for MMC card commands 1, 2, 3 and 40, and if the MMC card bus is operating in open-drain mode during the response phase to the command sent. Typically, during card identification mode when the card is either in idle, ready or ident state. It is also necessary to set this bit to 1, for a broadcast host response (see Broadcast host response register MMCHS_CON[2] HR) 0x0: No Open Drain 0x1: Open Drain or Broadcast host response	RW	0

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Table 24-76. Register Call Summary for Register MMCHS_CON

MMC/SD/SDIO Functional Description

- Interrupt Requests: [0]
- DMA Modes: [1] [2] [3]
- Slave DMA Operations: [4]
- Generation on Rising Edge of MMC Clock: [5]
- MMC CE-ATA Command Completion Disable Management: [6] [7] [8]
- Test Registers: [9]

MMC/SD/SDIO Programming Guide

- MMC/SD/SDIO Host Controller Initialization Flow: [10]
- Basic Operations for MMC/SD/SDIO Host Controller: [11] [12] [13] [14] [15]
- Bus Voltage Selection: [16]
- Boot Mode Configuration: [17] [18] [19] [20]

MMC/SD/SDIO Register Manual

- MMC/SD/SDIO Register Summary: [21] [22]
- MMC/SD/SDIO Register Description: [23] [24] [25] [26] [27] [28] [29] [30] [31] [32] [33] [34] [35] [36] [37] [38] [39] [40] [41] [42] [43]

Table 24-77. MMCHS_PWCNT

Address Offset	0x0000 0130		
Physical Address	0x4809 C130 0x480B 4130 0x480A D130 0x480D 1130 0x480D 5130	**Instance**	MMCHS1 MMCHS2 MMCHS3 MMCHS4 MMCHS5
Description	Power counter register This register is used to program a mmc counter to delay command transfers after activating the PAD power, this value depends on PAD characteristics and voltage.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PWRCNT															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved These bits are initialized to zero, and writes to them are ignored. Reads return 0.	R	0x0000
15:0	PWRCNT	Power counter register. This register is used to introduce a delay between the PAD ACTIVE pin assertion and the command issued. 0x0: No additional delay added 0x1: TCF delay (card clock period) 0x2: TCF x 2 delay (card clock period) 0xFFFE: TCF x 65534 delay (card clock period) 0xFFFF: TCF x 65535 delay (card clock period)	RW	0x0000

Table 24-78. Register Call Summary for Register MMCHS_PWCNT

MMC/SD/SDIO Register Manual

- MMC/SD/SDIO Register Summary: [0] [1]

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Table 24-79. MMCHS_SDMASA

Address Offset	0x0000 0200		
Physical Address	See Table 24-57 to Table 24-58	**Instance**	MMCHS
Description	sDMA System address: This register is used to program a mmc counter to delay command transfers after activating the PAD power, this value depends on PAD characteristics and voltage.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PWRCNT															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved These bits are initialized to zero, and writes to them are ignored. Reads return 0.	R	0x0000
15:0	PWRCNT	Power counter register. This register is used to introduce a delay between the PAD ACTIVE pin assertion and the command issued. 0x0: No additional delay added 0x1: TCF delay (card clock period) 0x2: TCF x 2 delay (card clock period) 0xFFFE: TCF x 65534 delay (card clock period) 0xFFFF: TCF x 65535 delay (card clock period)	RW	0x0000

Table 24-80. MMCHS_BLK

Address Offset	0x0000 0204		
Physical Address	0x4809 C204 0x480B 4204 0x480A D204 0x480D 1204 0x480D 5204	**Instance**	MMCHS1 MMCHS2 MMCHS3 MMCHS4 MMCHS5
Description	Transfer Length Configuration register MMCHS_BLK[11:0] BLEN is the block size register. MMCHS_BLK[31:16] NBLK is the block count register. This register shall be used for any card.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NBLK																RESERVED				BLEN											

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Bits	Field Name	Description	Type	Reset
31:16	NBLK	Blocks count for current transfer This register is enabled when Block count Enable (MMCHS_CMD[1] BCE) is set to 1 and is valid only for multiple block transfers. Setting the block count to 0 results no data blocks being transferred. Note: The host controller decrements the block count after each block transfer and stops when the count reaches zero. This register can be accessed only if no transaction is executing (i.e, after a transaction has stopped). Read operations during transfers may return an invalid value and write operation will be ignored. In suspend context, the number of blocks yet to be transferred can be determined by reading this register. When restoring transfer context prior to issuing a Resume command, The local host shall restore the previously saved block count. 0x0: Stop count 0x1: 1 block 0x2: 2 blocks 0xFFFF: 65535 blocks	RW	0x0000
15:12	RESERVED	Reserved. Host DMA Buffer Boundary not supported. These bits are initialized to zero, and writes to them are ignored.	R	0x0
11:0	BLEN	Transfer Block Size. This register specifies the block size for block data transfers. Read operations during transfers may return an invalid value, and write operations are ignored. When a CMD12 command is issued to stop the transfer, a read of the BLEN field after transfer completion (MMCHS_STAT[1] TC set to 1) will not return the true byte number of data length while the stop occurs but the value written in this register before transfer is launched. 0x0: No data transfer 0x1: 1 byte block length 0x2: 2 bytes block length 0x3: 3 bytes block length 0x1FF: 511 bytes block length 0x200: 512 bytes block length 0x400: 1024 bytes block length	RW	0x000

Table 24-81. Register Call Summary for Register MMCHS_BLK

MMC/SD/SDIO Functional Description
- Interrupt Requests: [0] [1]
- Requirements for Descriptors: [2]
- DMA Receive Mode: [3]
- DMA Transmit Mode: [4]
- Data Buffer: [5]

MMC/SD/SDIO Programming Guide
- Basic Operations for MMC/SD/SDIO Host Controller: [6] [7] [8] [9]
- Boot Mode Configuration: [10] [11]

MMC/SD/SDIO Register Manual
- MMC/SD/SDIO Register Summary: [12] [13]
- MMC/SD/SDIO Register Description: [14] [15] [16] [17] [18] [19] [20] [21] [22]

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Table 24-82. MMCHS_ARG

Address Offset	0x0000 0208		
Physical Address	0x4809 C208 0x480B 4208 0x480A D208 0x480D 1208 0x480D 5208	**Instance**	MMCHS1 MMCHS2 MMCHS3 MMCHS4 MMCHS5
Description	Command argument Register This register contains command argument specified as bit 39-8 of Command-Format These registers must be initialized prior to sending the command itself to the card (write action into the register MMCHS_CMD register). Only exception is for a command index specifying stuff bits in arguments, making a write unnecessary.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ARG																															

Bits	Field Name	Description	Type	Reset
31:0	ARG	Command argument bits [31:0]	RW	0x0000 0000

Table 24-83. Register Call Summary for Register MMCHS_ARG

MMC/SD/SDIO Functional Description
- MMC CE-ATA Command Completion Disable Management: [0]

MMC/SD/SDIO Programming Guide
- Basic Operations for MMC/SD/SDIO Host Controller: [1] [2] [3]
- Boot Mode Configuration: [4] [5]

MMC/SD/SDIO Register Manual
- MMC/SD/SDIO Register Summary: [6] [7]
- MMC/SD/SDIO Register Description: [8]

Table 24-84. MMCHS_CMD

Address Offset	0x0000 020C		
Physical Address	0x4809 C20C 0x480B 420C 0x480A D20C 0x480D 120C 0x480D 520C	**Instance**	MMCHS1 MMCHS2 MMCHS3 MMCHS4 MMCHS5
Description	Command and transfer mode register MMCHS_CMD[31:16] = the command register MMCHS_CMD[15:0] = the transfer mode. This register configures the data and command transfers. A write into the most significant byte send the command. A write into MMCHS_CMD[15:0] registers during data transfer has no effect. This register shall be used for any card. Note: In SYSTEST mode, a write into MMCHS_CMD register will not start a transfer.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		INDX						CMD_TYPE		DP	CICE	CCCE	RESERVED	RSP_TYPE		RESERVED								MSBS	DDIR	RESERVED		ACEN	BCE	DE	

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Bits	Field Name	Description	Type	Reset
31:30	RESERVED	Reserved. These bits are initialized to zero, and writes to them are ignored.	R	0x0
29:24	INDX	Command index Binary encoded value from 0 to 63 specifying the command number send to card 0x0: CMD0 or ACMD0 0x1: CMD1 or ACMD1 0x2: CMD2 or ACMD2 0x3: CMD3 or ACMD3 0x4: CMD4 or ACMD4 0x5: CMD5 or ACMD5 0x6: CMD6 or ACMD6 0x7: CMD7 or ACMD7 0x8: CMD8 or ACMD8 0x9: CMD9 or ACMD9 0xA: CMD10 or ACMD10 0xB: CMD11 or ACMD11 0xC: CMD12 or ACMD12 0xD: CMD13 or ACMD13 0xE: CMD14 or ACMD14 0xF: CMD15 or ACMD15 0x10: CMD16 or ACMD16 0x11: CMD17 or ACMD17 0x12: CMD18 or ACMD18 0x13: CMD19 or ACMD19 0x14: CMD20 or ACMD20 0x15: CMD21 or ACMD21 0x16: CMD22 or ACMD22 0x17: CMD23 or ACMD23 0x18: CMD24 or ACMD24 0x19: CMD25 or ACMD25 0x1A: CMD26 or ACMD26 0x1B: CMD27 or ACMD27 0x1C: CMD28 or ACMD28 0x1D: CMD29 or ACMD29 0x1E: CMD30 or ACMD30 0x1F: CMD31 or ACMD31 0x20: CMD32 or ACMD32 0x21: CMD33 or ACMD33 0x22: CMD34 or ACMD34 0x23: CMD35 or ACMD35 0x24: CMD36 or ACMD36 0x25: CMD37 or ACMD37 0x26: CMD38 or ACMD38 0x27: CMD39 or ACMD39 0x28: CMD40 or ACMD40 0x29: CMD41 or ACMD41 0x2A: CMD42 or ACMD42 0x2B: CMD43 or ACMD43	RW	0x00

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Bits	Field Name	Description	Type	Reset
		0x2C: CMD44 or ACMD44 0x2D: CMD45 or ACMD45 0x2E: CMD46 or ACMD46 0x2F: CMD47 or ACMD47 0x30: CMD48 or ACMD48 0x31: CMD49 or ACMD49 0x32: CMD50 or ACMD50 0x33: CMD51 or ACMD51 0x34: CMD52 or ACMD52 0x35: CMD53 or ACMD53 0x36: CMD54 or ACMD54 0x37: CMD55 or ACMD55 0x38: CMD56 or ACMD56 0x39: CMD57 or ACMD57 0x3A: CMD58 or ACMD58 0x3B: CMD59 or ACMD59 0x3C: CMD60 or ACMD60 0x3D: CMD61 or ACMD61 0x3E: CMD62 or ACMD62 0x3F: CMD63 or ACMD63		
23:22	CMD_TYPE	Command type This register specifies three types of special command: Suspend, Resume and Abort. These bits shall be set to 00b for all other commands. 0x0: Others Commands 0x1: CMD52 for writing "Bus Suspend" in CCCR 0x2: CMD52 for writing "Function Select" in CCCR 0x3: Abort command CMD12, CMD52 for writing " I/O Abort" in CCCR	RW	0x0
21	DP	Data present select This register indicates that data is present and DAT line shall be used. It must be set to 0 in the following conditions: - command using only CMD line - command with no data transfer but using busy signal on DAT[0] - Resume command 0x0: Command with no data transfer 0x1: Command with data transfer	RW	0
20	CICE	Command Index check enable This bit must be set to 1 to enable index check on command response to compare the index field in the response against the index of the command. If the index is not the same in the response as in the command, it is reported as a command index error (MMCHS_STAT[19] CIE set to1) Note: The register CICE cannot be configured for an Auto CMD12, then index check is automatically checked when this command is issued. 0x0: Index check disable 0x1: Index check enable	RW	0

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Bits	Field Name	Description	Type	Reset
19	CCCE	Command CRC check enable This bit must be set to 1 to enable CRC7 check on command response to protect the response against transmission errors on the bus. If an error is detected, it is reported as a command CRC error (MMCHS_STAT[17] CCRC set to 1). Note: The register CCCE cannot be configured for an Auto CMD12, and then CRC check is automatically checked when this command is issued. 0x0: CRC7 check disable 0x1: CRC7 check enable	RW	0
18	RESERVED	Reserved. This bit is initialized to zero, and writes to it are ignored.	R	0
17:16	RSP_TYPE	Response type This bits defines the response type of the command 0x0: No response 0x1: Response Length 136 bits 0x2: Response Length 48 bits 0x3: Response Length 48 bits with busy after response	RW	0x0
15:6	RESERVED	Reserved. These bits are initialized to zero, and writes to them are ignored.	R	0x000
5	MSBS	Multi/Single block select This bit must be set to 1 for data transfer in case of multi block command. For any others command this bit shall be set to 0. 0x0: Single block. If this bit is 0, it is not necessary to set the register MMCHS_BLK[31:16] NBLK. 0x1: Multi block. When Block Count is disabled (MMCHS_CMD[1] BCE is set to 0) in Multiple block transfers (MMCHS_CMD[5] MSBS is set to 1), the module can perform infinite transfer.	RW	0
4	DDIR	Data transfer Direction Select This bit defines either data transfer will be a read or a write. 0x0: Data Write (host to card) 0x1: Data Read (card to host)	RW	0
3	RESERVED	Reserved. These bits are initialized to zero, and writes to them are ignored.	R	0
2	ACEN	Auto CMD12 Enable SDIO does not support this feature. When this bit is set to 1, the host controller issues a CMD12 automatically after the transfer completion of the last block. The Host Driver shall not set this bit to issue commands that do not require CMD12 to stop data transfer. In particular, safe commands do not require CMD12. 0x0: Auto CMD12 disable 0x1: Auto CMD12 enable or CCS detection enabled.	RW	0

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Bits	Field Name	Description	Type	Reset
1	BCE	Block Count Enable Multiple block transfers only. This bit is used to enable the block count register (MMCHS_BLK[31:16] NBLK). When Block Count is disabled (MMCHS_CMD[1] BCE is set to 0) in Multiple block transfers (MMCHS_CMD[5] MSBS is set to 1), the module can perform infinite transfer. 0x0: Block count disabled for infinite transfer. 0x1: Block count enabled for multiple block transfer with known number of blocks	RW	0
0	DE	DMA Enable This bit is used to enable DMA mode for host data access. 0x0: DMA mode disable 0x1: DMA mode enable	RW	0

Table 24-85. Register Call Summary for Register MMCHS_CMD

MMC/SD/SDIO Environment
- Data Format: [0] [1] [2] [3]

MMC/SD/SDIO Functional Description
- Interrupt Requests: [4] [5]
- Requirements for Descriptors: [6]
- Slave DMA Operations: [7]
- Data Buffer: [8]
- Memory Size, Block Length, and Buffer-Management Relationship: [9] [10]
- Transfer Stop: [11]
- MMC CE-ATA Command Completion Disable Management: [12] [13]

MMC/SD/SDIO Programming Guide
- Basic Operations for MMC/SD/SDIO Host Controller: [14] [15] [16] [17] [18] [19] [20]
- Bus Voltage Selection: [21]
- Boot Mode Configuration: [22] [23]

MMC/SD/SDIO Register Manual
- MMC/SD/SDIO Register Summary: [24] [25]
- MMC/SD/SDIO Register Description: [26] [27] [28] [29] [30] [31] [32] [33] [34] [35] [36] [37] [38] [39] [40] [41] [42] [43] [44] [45] [46] [47]

Table 24-86. MMCHS_RSP10

Address Offset	0x0000 0210		
Physical Address	0x4809 C210 0x480B 4210 0x480A D210 0x480D 1210 0x480D 5210	**Instance**	MMCHS1 MMCHS2 MMCHS3 MMCHS4 MMCHS5
Description	Command response[31:0] Register This 32-bit register holds bits positions [31:0] of command response type R1/R1b/R2/R3/R4/R5/R5b/R6		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSP1																RSP0															

Bits	Field Name	Description	Type	Reset
31:16	RSP1	Command Response [31:16]	R	0x0000
15:0	RSP0	Command Response [15:0]	R	0x0000

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Table 24-87. Register Call Summary for Register MMCHS_RSP10

MMC/SD/SDIO Functional Description • Different Types of Responses: [0] [1] [2]
MMC/SD/SDIO Programming Guide • Basic Operations for MMC/SD/SDIO Host Controller: [3] [4] [5] [6]
MMC/SD/SDIO Register Manual • MMC/SD/SDIO Register Summary: [7] [8] • MMC/SD/SDIO Register Description: [9] [10]

Table 24-88. MMCHS_RSP32

Address Offset	0x0000 0214		
Physical Address	0x4809 C214 0x480B 4214 0x480A D214 0x480D 1214 0x480D 5214	**Instance**	MMCHS1 MMCHS2 MMCHS3 MMCHS4 MMCHS5
Description	Command response[63:32] Register This 32-bit register holds bits positions [63:32] of command response type R2		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSP3																RSP2															

Bits	Field Name	Description	Type	Reset
31:16	RSP3	Command Response [63:48]	R	0x0000
15:0	RSP2	Command Response [47:32]	R	0x0000

Table 24-89. Register Call Summary for Register MMCHS_RSP32

MMC/SD/SDIO Functional Description • Different Types of Responses: [0]
MMC/SD/SDIO Programming Guide • Basic Operations for MMC/SD/SDIO Host Controller: [1] [2] [3]
MMC/SD/SDIO Register Manual • MMC/SD/SDIO Register Summary: [4] [5]

Table 24-90. MMCHS_RSP54

Address Offset	0x0000 0218		
Physical Address	0x4809 C218 0x480B 4218 0x480A D218 0x480D 1218 0x480D 5218	**Instance**	MMCHS1 MMCHS2 MMCHS3 MMCHS4 MMCHS5
Description	Command response[95:64] Register This 32-bit register holds bits positions [95:64] of command response type R2		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSP5																RSP4															

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Bits	Field Name	Description	Type	Reset
31:16	RSP5	Command Response [95:80]	R	0x0000
15:0	RSP4	Command Response [79:64]	R	0x0000

Table 24-91. Register Call Summary for Register MMCHS_RSP54

MMC/SD/SDIO Functional Description • Different Types of Responses: [0]
MMC/SD/SDIO Programming Guide • Basic Operations for MMC/SD/SDIO Host Controller: [1] [2] [3]
MMC/SD/SDIO Register Manual • MMC/SD/SDIO Register Summary: [4] [5]

Table 24-92. MMCHS_RSP76

Address Offset	0x0000 021C		
Physical Address	0x4809 C21C 0x480B 421C 0x480A D21C 0x480D 121C 0x480D 521C	**Instance**	MMCHS1 MMCHS2 MMCHS3 MMCHS4 MMCHS5
Description	Command response[127:96] Register This 32-bit register holds bits positions [127:96] of command response type R2		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSP7																RSP6															

Bits	Field Name	Description	Type	Reset
31:16	RSP7	Command Response [127:112]	R	0x0000
15:0	RSP6	Command Response [111:96]	R	0x0000

Table 24-93. Register Call Summary for Register MMCHS_RSP76

MMC/SD/SDIO Functional Description • Different Types of Responses: [0] [1] [2]
MMC/SD/SDIO Programming Guide • Basic Operations for MMC/SD/SDIO Host Controller: [3] [4] [5]
MMC/SD/SDIO Register Manual • MMC/SD/SDIO Register Summary: [6] [7] • MMC/SD/SDIO Register Description: [8] [9]

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Table 24-94. MMCHS_DATA

Address Offset	0x0000 0220		
Physical Address	0x4809 C220 0x480B 4220 0x480A D220 0x480D 1220 0x480D 5220	**Instance**	MMCHS1 MMCHS2 MMCHS3 MMCHS4 MMCHS5
Description	Data Register This register is the 32-bit entry point of the buffer for read or write data transfers. The buffer size is 32bits x256(1024 bytes). Bytes within a word are stored and read in little endian format. This buffer can be used as two 512 byte buffers to transfer data efficiently without reducing the throughput. Sequential and contiguous access is necessary to increment the pointer correctly. Random or skipped access is not allowed. In little endian, if the local host accesses this register byte-wise or 16bit-wise, the least significant byte (bits [7:0]) must always be written/read first. The update of the buffer address is done on the most significant byte write for full 32-bit DATA register or on the most significant byte of the last word of block transfer. Example 1: Byte or 16-bit access Mbyteen[3:0]=0001 (1-byte) = Mbyteen[3:0]=0010 (1-byte) = Mbyteen[3:0]=1100 (2-bytes) OK Mbyteen[3:0]=0001 (1-byte) = Mbyteen[3:0]=0010 (1-byte) = Mbyteen[3:0]=0100 (1-byte) OK Mbyteen[3:0]=0001 (1-byte) = Mbyteen[3:0]=0010 (1-byte) = Mbyteen[3:0]=1000 (1-byte) Bad		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															

Bits	Field Name	Description	Type	Reset
31:0	DATA	Data Register [31:0] In functional mode (MMCHS_CON[4] MODE set to the default value 0) , A read access to this register is allowed only when the buffer read enable status is set to 1 (MMCHS_PSTATE[11] BRE), otherwise a bad access (MMCHS_STAT[29] BADA) is signaled. A write access to this register is allowed only when the buffer write enable status is set to 1(MMCHS_PSTATE[10] BWE), otherwise a bad access (MMCHS_STAT[29] BADA) is signaled and the data is not written.	RW	0x0000 0000

Table 24-95. Register Call Summary for Register MMCHS_DATA

MMC/SD/SDIO Functional Description

- Interrupt Requests: [0] [1]
- Data Buffer: [2] [3] [4] [5] [6] [7] [8] [9]
- Transfer or Command Status and Errors Reporting: [10]

MMC/SD/SDIO Programming Guide

- Basic Operations for MMC/SD/SDIO Host Controller: [11]

MMC/SD/SDIO Register Manual

- MMC/SD/SDIO Register Summary: [12] [13]
- MMC/SD/SDIO Register Description: [14] [15] [16] [17] [18] [19]

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Table 24-96. MMCHS_PSTATE

Address Offset	0x0000 0224		
Physical Address	0x4809 C224 0x480B 4224 0x480A D224 0x480D 1224 0x480D 5224	**Instance**	MMCHS1 MMCHS2 MMCHS3 MMCHS4 MMCHS5
Description	Present state register The Host can get status of the Host Controller from this 32-bit read only register.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							CLEV	DLEV				WP	CDPL	CSS	CINS	RESERVED				BRE	BWE	RTA	WTA	RESERVED					DLA	DATI	CMDI

Bits	Field Name	Description	Type	Reset
31:25	RESERVED	Reserved. These bits are initialized to zero, and writes to them are ignored.	R	0x00
24	CLEV	CMD line signal level This status is used to check the CMD line level to recover from errors, and for debugging. The value of this register after reset depends on the CMD line level at that time. Read 0x0: The CMD line level is 0. Read 0x1: The CMD line level is 1.	R	-
23:20	DLEV	DAT[3:0] line signal level DAT[3] = bit 23 DAT[2] = bit 22 DAT[1] = bit 21 DAT[0] = bit 20 This status is used to check DAT line level to recover from errors, and for debugging. This is especially useful in detecting the busy signal level from DAT[0]. The value of these registers after reset depends on the DAT lines level at that time.	R	0x-
19	WP	Write protect switch pin level For SDIO cards only. This bit reflects the write protect input pin (SDWP) level. The value of this register after reset depends on the protect input pin (SDWP) level at that time. Read 0x0: If MMCHS_CON[8] WPP is set to 0 (default), the card is write protected, otherwise the card is not protected. Read 0x1: If MMCHS_CON[8] WPP is set to 0 (default), the card is not write protected, otherwise the card is protected.	R	-
18	CDPL	Card detect pin level This bit reflects the inverse value of the card detect input pin (SDCD), debouncing is not performed on this bit and bit is valid only when Card State Stable (MMCHS_PSTATE[17] CSS) is set to 1. Use of this bit is limited to testing since it must be debounced y software. The value of this register after reset depends on the card detect input pin (SDCD) level at that time. Read 0x0: The value of the card detect input pin (SDCD) is 1 Read 0x1: The value of the card detect input pin (SDCD) is 0	R	-

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Bits	Field Name	Description	Type	Reset
17	CSS	Card State Stable This bit is used for testing. It is set to 1 only when Card Detect Pin Level is stable (MMCHS_PSTATE[18] CDPL). Debouncing is performed on the card detect input pin (SDCD) to detect card stability. This bit is not affected by a software reset. Read 0x0: Reset or Debouncing Read 0x1: No card or card inserted	R	0
16	CINS	Card inserted This bit is the debounced value of the card detect input pin (SDCD). An inactive to active transition of the card detect input pin (SDCD) will generate a card insertion interrupt (MMCHS_STAT[6] CINS). A active to inactive transition of the card detect input pin (SDCD) will generate a card removal interrupt (MMCHS_STAT[7] CREM). This bit is not affected by a software reset. Read 0x0: If MMCHS_CON[7] CDP is set to 0 (default), no card is detected. The card may have been removed from the card slot. If MMCHS_CON[7] CDP is set to 1, the card has been inserted. Read 0x1: If MMCHS_CON[7] CDP is set to 0 (default), the card has been inserted from the card slot. If MMCHS_CON[7] CDP is set to 1, no card is detected. The card may have been removed from the card slot.	R	0
15:12	RESERVED	Reserved. These bits are initialized to zero, and writes to them are ignored.	R	0x0
11	BRE	Buffer read enable This bit is used for non-DMA read transfers. It indicates that a complete block specified by MMCHS_BLK[11:0] BLEN has been written in the buffer and is ready to be read. It is set to 0 when the entire block is read from the buffer. It is set to 1 when a block data is ready in the buffer and generates the Buffer read ready status of interrupt (MMCHS_STAT[5] BRR). Read 0x0: Read BLEN bytes disable Read 0x1: Read BLEN bytes enable. Readable data exists in the buffer.	R	0
10	BWE	Buffer Write enable This status is used for non-DMA write transfers. It indicates if space is available for write data. Read 0x0: There is no room left in the buffer to write BLEN bytes of data. Read 0x1: There is enough space in the buffer to write BLEN bytes of data.	R	0
9	RTA	Read transfer active This status is used for detecting completion of a read transfer. It is set to 1 after the end bit of read command or by activating a continue request (MMCHS_HCTL[17] CR) following a stop at block gap request. This bit is set to 0 when all data have been read by the local host after last block or after a stop at block gap request. Read 0x0: No valid data on the DAT lines. Read 0x1: read data transfer on going.	R	0

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Bits	Field Name	Description	Type	Reset
8	WTA	Write transfer active This status indicates a write transfer active. It is set to 1 after the end bit of write command or by activating a continue request (MMCHS_HCTL[17] CR) following a stop at block gap request. This bit is set to 0 when CRC status has been received after last block or after a stop at block gap request. Read 0x0: No valid data on the DAT lines. Read 0x1: Write data transfer on going.	R	0
7:3	RESERVED	Reserved. These bits are initialized to zero, and writes to them are ignored.	R	0x00
2	DLA	DAT line active This status bit indicates whether one of the DAT line is in use. In the case of read transactions (card to host): This bit is set to 1 after the end bit of read command or by activating continue request MMCHS_HCTL[17] CR. This bit is set to 0 when the host controller received the end bit of the last data block or at the beginning of the read wait mode. In the case of write transactions (host to card): This bit is set to 1 after the end bit of write command or by activating continue request MMCHS_HCTL[17] CR. This bit is set to 0 on the end of busy event for the last block; host controller must wait 8 clock cycles with line not busy to really consider not "busy state" or after the busy block as a result of a stop at gap request. Read 0x0: DAT Line inactive Read 0x1: DAT Line active	R	0
1	DATI	Command inhibit(DAT) This status bit is generated if either DAT line is active (MMCHS_PSTATE[2] DLA) or Read transfer is active (MMCHS_PSTATE[9] RTA) or when a command with busy is issued. This bit prevents the local host to issue a command. A change of this bit from 1 to 0 generates a transfer complete interrupt (MMCHS_STAT[1] TC). Read 0x0: Issuing of command using the DAT lines is allowed Read 0x1: Issuing of command using DAT lines is not allowed	R	0
0	CMDI	Command inhibit(CMD) This status bit indicates that the CMD line is in use. This bit is set to 0 when the most significant byte is written into the command register. This bit is not set when Auto CMD12 is transmitted. This bit is set to 0 in either the following cases: - After the end bit of the command response, excepted if there is a command conflict error (MMCHS_STAT[17] CCRC or MMCHS_STAT[18] CEB set to 1) or a Auto CMD12 is not executed (MMCHS_AC12[0] ACNE). - After the end bit of the command without response (MMCHS_CMD[17:16] RSP_TYPE set to "00") In case of a command data error is detected (MMCHS_STAT[16] CTO set to 1), this register is not automatically cleared. Read 0x0: Issuing of command using CMD line is allowed Read 0x1: Issuing of command using CMD line is not allowed	R	0

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Table 24-97. Register Call Summary for Register MMCHS_PSTATE

MMC/SD/SDIO Functional Description

- Software Reset: [0]
- Interrupt Requests: [1] [2] [3] [4]
- Requirements for Descriptors: [5] [6] [7]
- Data Buffer: [8] [9]
- Data Buffer Status: [10] [11]
- MMC/SD/SDIO Hardware Status Features: [12] [13] [14] [15] [16] [17] [18] [19] [20]

MMC/SD/SDIO Programming Guide

- Basic Operations for MMC/SD/SDIO Host Controller: [21] [22] [23] [24] [25] [26]
- Bus Voltage Selection: [27]

MMC/SD/SDIO Register Manual

- MMC/SD/SDIO Register Summary: [28] [29]
- MMC/SD/SDIO Register Description: [30] [31] [32] [33] [34] [35] [36] [37] [38] [39] [40] [41] [42] [43] [44] [45] [46] [47] [48] [49] [50] [51] [52] [53] [54]

Table 24-98. MMCHS_HCTL

Address Offset	0x0000 0228		
Physical Address	0x4809 C228 0x480B 4228 0x480A D228 0x480D 1228 0x480D 5228	**Instance**	MMCHS1 MMCHS2 MMCHS3 MMCHS4 MMCHS5
Description	Control register This register defines the host controls to set power, wakeup and transfer parameters. MMCHS_HCTL[31:24] = Wakeup control MMCHS_HCTL[23:16] = Block gap control MMCHS_HCTL[15:8] = Power control MMCHS_HCTL[7:0] = Host control		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				OBWE	REM	INS	IWE	RESERVED				IBG	RWC	CR	SBGR	RESERVED				SDVS			SDBP	CDSS	CDTL	RESERVED	DMAS		HSPE	DTW	LED

Bits	Field Name	Description	Type	Reset
31:28	RESERVED	Reserved. These bits are initialized to zero, and writes to them are ignored.	R	0x0
27	OBWE	Wakeup event enable for 'Out-of-Band' Interrupt. This bit enables wakeup events for 'Out-of-Band' assertion. Wakeup is generated if the wakeup feature is enabled (MMCHS_SYSCONFIG[2] ENAWAKEUP). The write to this register is ignored when MMCHS_CON[14] OBIE is not set. 0x0: Disable wakeup on 'Out-of-Band' Interrupt 0x1: Enable wakeup on 'Out-of-Band' Interrupt	RW	0
26	REM	Wakeup event enable on SD card removal This bit enables wakeup events for card removal assertion. Wakeup is generated if the wakeup feature is enabled (MMCHS_SYSCONFIG[2] ENAWAKEUP). 0x0: Disable wakeup on card removal 0x1: Enable wakeup on card removal	RW	0

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Bits	Field Name	Description	Type	Reset
25	INS	Wakeup event enable on SD card insertion This bit enables wakeup events for card insertion assertion. Wakeup is generated if the wakeup feature is enabled (MMCHS_SYSCONFIG[2] ENAWAKEUP). 0x0: Disable wakeup on card insertion 0x1: Enable wakeup on card insertion	RW	0
24	IWE	Wakeup event enable on SD card interrupt This bit enables wakeup events for card interrupt assertion. Wakeup is generated if the wakeup feature is enabled (MMCHS_SYSCONFIG[2] ENAWAKEUP). 0x0: Disable wakeup on card interrupt 0x1: Enable wakeup on card interrupt	RW	0
23:20	RESERVED	Reserved. These bits are initialized to zero, and writes to them are ignored.	R	0x0
19	IBG	Interrupt block at gap This bit is valid only in 4-bit mode of SDIO card to enable interrupt detection in the interrupt cycle at block gap for a multiple block transfer. For MMC cards and for SD card this bit should be set to 0. 0x0: Disable interrupt detection at the block gap in 4-bit mode 0x1: Enable interrupt detection at the block gap in 4-bit mode	RW	0
18	RWC	Read wait control The read wait function is optional only for SDIO cards. If the card supports read wait, this bit must be enabled, then requesting a stop at block gap (MMCHS_HCTL[16] SBGR) generates a read wait period after the current end of block. Be careful, if read wait is not supported it may cause a conflict on DAT line. 0x0: Disable Read Wait Control. Suspend/Resume cannot be supported. 0x1: Enable Read Wait Control	RW	0
17	CR	Continue request This bit is used to restart a transaction that was stopped by requesting a stop at block gap (MMCHS_HCTL[16] SBGR). Set this bit to 1 restarts the transfer. The bit is automatically set to 0 by the host controller when transfer has restarted i.e DAT line is active (MMCHS_PSTATE[2] DLA) or transferring data (MMCHS_PSTATE[8] WTA). The Stop at block gap request must be disabled (MMCHS_HCTL[16] SBGR = 0) before setting this bit. 0x0: No affect 0x1: transfer restart	RW	0
16	SBGR	Stop at block gap request This bit is used to stop executing a transaction at the next block gap. The transfer can restart with a continue request (MMCHS_HCTL[17] CR) or during a suspend/resume sequence. In case of read transfer, the card must support read wait control. In case of write transfer, the host driver shall set this bit after all block data written. Until the transfer completion (MMCHS_STAT[1] TC set to 1), the host driver shall leave this bit set to 1. If this bit is set, the local host shall not write to the data register (MMCHS_DATA). 0x0: Transfer mode 0x1: Stop at block gap	RW	0
15:12	RESERVED	Reserved. These bits are initialized to zero, and writes to them are ignored.	R	0x0

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Bits	Field Name	Description	Type	Reset
11:9	SDVS	SD bus voltage select All cards. The host driver should set to these bits to select the voltage level for the card according to the voltage supported by the system (MMCHS_CAPA[26:24]) before starting a transfer. 0x5: 1.8V (Typical) 0x6: 3.0V (Typical) 0x7: 3.3V (Typical)	RW	0x0
8	SDBP	SD bus power Before setting this bit, the host driver shall select the SD bus voltage (MMCHS_HCTL[11:9] SDVS). If the host controller detects the No card state, this bit is automatically set to 0. If the module is power off, a write in the command register (MMCHS_CMD) will not start the transfer. A write to this bit has no effect if the selected SD bus voltage is not supported according to capability register (MMCHS_CAPA[26:24]). 0x0: Power off 0x1: Power on	RW	0
7	CDSS	Card Detect Signal Selection This bit selects source for the card detection.When the source for the card detection is switched, the interrupt should be disabled during the switching period by clearing the Interrupt Status/Signal Enable register in order to mask unexpected interrupt being caused by the glitch. The Interrupt Status/Signal Enable should be disabled during over the period of debouncing. 0x0: SDCD# is selected (for normal use) 0x1: The Card Detect Test Level is selected (for test purpose)	RW	0
6	CDTL	Card Detect Test Level: This bit is enabled while the Card Detect Signal Selection is set to 1 and it indicates card inserted or not. 0x0: No Card 0x1: Card Inserted	RW	0
5	RESERVED	Reserved. These bits are initialized to zero, and writes to them are ignored.	R	0
4:3	DMAS	DMA Select Mode: One of supported DMA modes can be selected. The host driver shall check support of DMA modes by referring the Capabilities register. Use of selected DMA is determined by DMA Enable of the Transfer Mode register. This register is only meaningful when MMCHS_HL_HWINFO[0] MADMA_EN is set to 1. When MMCHS_HL_HWINFO[0] MADMA_EN is set to 0 the bit field is read only and returned value is 0. 0x0: Reserved 0x1: Reserved 0x2: 32-bit Address ADMA2 is selected 0x3: Reserved	RW	0x0

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Bits	Field Name	Description	Type	Reset
2	HSPE	High Speed Enable: Before setting this bit, the Host Driver shall check the High Speed Support in the Capabilities register. If this bit is set to 0 (default), the Host Controller outputs CMD line and DAT lines at the falling edge of the SD Clock. If this bit is set to 1, the Host Controller outputs CMD line and DAT lines at the rising edge of the SD Clock.This bit shall not be set when dual data rate mode is activated in MMCHS_CON[19] DDR. 0x0: Normal speed mode 0x1: High speed mode	RW	0
1	DTW	Data transfer width For MMC card, this bit must be set following a valid SWITCH command (CMD6) with the correct value and extend CSD index written in the argument. Prior to this command, the MMC card configuration register (CSD and EXT_CSD) must be verified for compliance with MMC standard specification 4.x (see section 3.6). This register has no effect when the MMC 8-bit mode is selected (register MMCHS_CON[5] DW8 set to1), For SD/SDIO cards, this bit must be set following a valid SET_BUS_WIDTH command (ACMD6) with the value written in bit 1 of the argument. Prior to this command, the SD card configuration register (SCR) must be verified for the supported bus width by the SD card. 0x0: 1-bit Data width (DAT[0] used) 0x1: 4-bit Data width (DAT[3:0] used)	RW	0
0	LED	Reserved bit. LED control feature is not supported This bit is initialized to zero, and writes to it are ignored.	R	0

Table 24-99. Register Call Summary for Register MMCHS_HCTL

MMC/SD/SDIO Functional Description
- Power Management: [0] [1] [2]
- Interrupt Requests: [3] [4]
- Requirements for Descriptors: [5]
- Transfer Stop: [6] [7]
- Output Signals Generation: [8]
- Generation on Falling Edge of MMC Clock: [9]
- Generation on Rising Edge of MMC Clock: [10]

MMC/SD/SDIO Programming Guide
- MMC/SD/SDIO Host Controller Initialization Flow: [11] [12]
- Basic Operations for MMC/SD/SDIO Host Controller: [13] [14]

MMC/SD/SDIO Register Manual
- MMC/SD/SDIO Register Summary: [15] [16]
- MMC/SD/SDIO Register Description: [17] [18] [19] [20] [21] [22] [23] [24] [25] [26] [27] [28] [29] [30] [31] [32] [33] [34]

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Table 24-100. MMCHS_SYSCTL

Address Offset	0x0000 022C		
Physical Address	0x4809 C22C 0x480B 422C 0x480A D22C 0x480D 122C 0x480D 522C	**Instance**	MMCHS1 MMCHS2 MMCHS3 MMCHS4 MMCHS5
Description	SD system control register This register defines the system controls to set software resets, clock frequency management and data timeout. MMCHS_SYSCTL[31:24] = Software resets MMCHS_SYSCTL[23:16] = Timeout control MMCHS_SYSCTL[15:0] = Clock control		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SRD	SRC	SRA	RESERVED				DTO				CLKD								RESERVED					CEN	ICS	ICE

Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Reserved. These bits are initialized to zero, and writes to them are ignored.	R	0x00
26	SRD	Software reset for DAT line. This bit is set to 1 for reset and released to 0 when completed. For more information about SRD bit manipulation, see Section 24.5.1.2.1.2.1, *DATA Lines Reset Procedure*. DAT finite state machine in both clock domain are also reset. The following registers are cleared by MMCHS_SYSCTL[26] SRD: - MMCHS_DATA - MMCHS_PSTATE[11] BRE, MMCHS_PSTATE[10] BWE, MMCHS_PSTATE[9] RTA, MMCHS_PSTATE[8] WTA, MMCHS_PSTATE[2] DLA, MMCHS_PSTATE[1] DATI - MMCHS_HCTL: SBGR and CR - MMCHS_STAT: MMCHS_STAT[5] BRR, MMCHS_STAT[4] BWR, MMCHS_STAT[2] BGE and MMCHS_STAT[1] TC Interconnect and MMC buffer data management is reinitialized. 0x0: Reset completed 0x1: Software reset for DAT line	RW	0
25	SRC	Software reset for CMD line For more information about SRC bit manipulation, see Section 24.5.1.2.1.1.1, *CMD Line Reset Procedure*. This bit is set to 1 for reset and released to 0 when completed. CMD finite state-machine in both clock domain are also reset. The following registers are cleared by MMCHS_SYSCTL[25] SRC: - MMCHS_PSTATE[0] CMDI - MMCHS_STAT[0] CC Interconnect and MMC command status management is reinitialized. 0x0: Reset completed 0x1: Software reset for CMD line	RW	0

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Bits	Field Name	Description	Type	Reset
24	SRA	Software reset for all This bit is set to 1 for reset, and released to 0 when completed. This reset affects the entire host controller except for the card detection circuit and capabilities registers. 0x0: Reset completed 0x1: Software reset for all the design	RW	0
23:20	RESERVED	Reserved. These bits are initialized to 0, and writes to them are ignored.	R	0x0
19:16	DTO	Data timeout counter value and busy timeout. This value determines the interval by which DAT lines timeouts are detected. The host driver needs to set this bit field based on - the maximum read access time (NAC) (Refer to the SD Specification Part1 Physical Layer), - the data read access time values (TAAC and NSAC) in the card specific data register (CSD) of the card, - the timeout clock base frequency (MMCHS_CAPA[5:0] TCF). If the card does not respond within the specified number of cycles, a data timeout error occurs (MMCHS_STAT[20] DTO). The MMCHS_SYSCTL[19:16] DTO register is also used to check busy duration, to generate busy timeout for commands with busy response or for busy programming during a write command. Timeout on CRC status is generated if no CRC token is present after a block write. 0x0: TCF x 2^{13} 0x1: TCF x 2^{14} 0xE: TCF x 2^{27} 0xF: Reserved	RW	0x0
15:6	CLKD	Clock frequency select These bits define the ratio between MMCi_FCLK and the output clock frequency on the CLK pin of either the memory card (MMC, SD or SDIO). 0x0: MMCi_FCLK bypass 0x1: MMCi_FCLK bypass 0x2: MMCi_FCLK / 2 0x3: MMCi_FCLK / 3 0x3FF: MMCi_FCLK / 1023	RW	0x000
5:3	RESERVED	Reserved. These bits are initialized to zero, and writes to them are ignored.	R	0x0
2	CEN	Clock enable This bit controls if the clock is provided to the card or not. 0x0: The clock is not provided to the card . Clock frequency can be changed . 0x1: The clock is provided to the card and can be automatically gated when MMCHS_SYSCONFIG[0] AUTOIDLE is set to 1 (default value) . The host driver shall wait to set this bit to 1 until the Internal clock is stable (MMCHS_SYSCTL[1] ICS).	RW	0
1	ICS	Internal clock stable (status) This bit indicates either the internal clock is stable or not. Read 0x0: The internal clock is not stable. Read 0x1: The internal clock is stable after enabling the clock (MMCHS_SYSCTL[1] ICE) or after changing the clock ratio (MMCHS_SYSCTL[15:6] CLKD).	R	0

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Bits	Field Name	Description	Type	Reset
0	ICE	Internal clock enable This register controls the internal clock activity. In very low power state, the internal clock is stopped. Note: The activity of the debounce clock (used for wakeup events) and the interface clock (used for reads and writes to the module register map) are not affected by this register. 0x0: The internal clock is stopped (very low power state). 0x1: The internal clock oscillates and can be automatically gated when MMCHS_SYSCONFIG[0] AUTOIDLE is set to 1 (default value) .	RW	0

Table 24-101. Register Call Summary for Register MMCHS_SYSCTL

MMC/SD/SDIO Environment • Protocol: [0]
MMC/SD/SDIO Functional Description • Software Reset: [1] [2] [3] [4] [5] • Retention Mode: [6]
MMC/SD/SDIO Programming Guide • MMC/SD/SDIO Host Controller Initialization Flow: [7] • Basic Operations for MMC/SD/SDIO Host Controller: [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] • Boot Mode Configuration: [23] [24]
MMC/SD/SDIO Register Manual • MMC/SD/SDIO Register Summary: [25] [26] • MMC/SD/SDIO Register Description: [27] [28] [29] [30] [31] [32] [33] [34] [35] [36] [37] [38] [39] [40]

Table 24-102. MMCHS_STAT

Address Offset	0x0000 0230		
Physical Address	0x4809 C230 0x480B 4230 0x480A D230 0x480D 1230 0x480D 5230	**Instance**	MMCHS1 MMCHS2 MMCHS3 MMCHS4 MMCHS5
Description	Interrupt status register The interrupt status regroups all the status of the module internal events that can generate an interrupt. MMCHS_STAT[31:16] = Error Interrupt Status MMCHS_STAT[15:0] = Normal Interrupt Status		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		BADA	CERR	RESERVED		ADMAE	ACE	CLE	DEB	DCRC	DTO	CIE	CEB	CCRC	CTO	ERRI	RESERVED				BSR	OBI	CIRQ	CREM	CINS	BRR	BWR	DMA	BGE	TC	CC

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Bits	Field Name	Description	Type	Reset
31:30	RESERVED	Reserved. These bits are initialized to zero, and writes to them are ignored.	R	0x0
29	BADA	Bad access to data space This bit is set automatically to indicate a bad access to buffer when not allowed: -This bit is set during a read access to the data register (MMCHS_DATA) while buffer reads are not allowed (MMCHS_PSTATE[11] BRE = 0) -This bit is set during a write access to the data register (MMCHS_DATA) while buffer writes are not allowed (MMCHS_PSTATE[10] BWE = 0) Write 0x0: Status bit unchanged Read 0x0: No Interrupt. Read 0x1: Bad Access Write 0x1: Status is cleared	RW	0
28	CERR	Card error This bit is set automatically when there is at least one error in a response of type R1, R1b, R6, R5 or R5b. Only bits referenced as type E(error) in status field in the response can set a card status error. An error bit in the response is flagged only if corresponding bit in card status response error MMCHS_CSRE in set. There is no card error detection for autoCMD12 command. The host driver shall read MMCHS_RSP76 register to detect error bits in the command response. Write 0x0: Status bit unchanged Read 0x0: No Error Write 0x1: Status is cleared Read 0x1: Card error	RW	0
27:26	RESERVED	Reserved. These bits are initialized to zero, and writes to them are ignored.	R	0x0
25	ADMAE	ADMA Error: This bit is set when the Host Controller detects errors during ADMA based data transfer. The state of the ADMA at an error occurrence is saved in the ADMA Error Status Register.In addition, the Host Controller generates this interrupt when it detects invalid descriptor data (Valid=0) at the ST_FDS state. ADMA Error State in the ADMA Error Status indicates that an error occurs in ST_FDS state. The Host Driver may find that Valid bit is not set at the error descriptor. Write 0x0: Status bit unchanged Read 0x0: No Interrupt. Write 0x1: Status is cleared Read 0x1: ADMA error	RW	0
24	ACE	Auto CMD12 error This bit is set automatically when one of the bits in Auto CMD12 Error status register has changed from 0 to 1. Write 0x0: Status bit unchanged Read 0x0: No Error. Read 0x1: AutoCMD12 error Write 0x1: Status is cleared	RW	0
23	CLE	Reserved. Current limit error is not supported. These bits are initialized to zero, and writes to them are ignored.	R	0

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Bits	Field Name	Description	Type	Reset
22	DEB	Data End Bit error This bit is set automatically when detecting a 0 at the end bit position of read data on DAT line or at the end position of the CRC status in write mode. Read 0x0: No Error Write 0x0: Status bit unchanged Write 0x1: Status is cleared Read 0x1: Data end bit error	RW	0
21	DCRC	Data CRC Error This bit is set automatically when there is a CRC16 error in the data phase response following a block read command or if there is a 3-bit CRC status different of a position "010" token during a block write command. Read 0x0: No Error. Write 0x0: Status bit unchanged Read 0x1: Data CRC error Write 0x1: Status is cleared	RW	0
20	DTO	Data timeout error This bit is set automatically according to the following conditions: - busy timeout for R1b, R5b response type - busy timeout after write CRC status - write CRC status timeout - read data timeout Read 0x0: No error. Write 0x0: Status bit unchanged Write 0x1: Status is cleared Read 0x1: Time out	RW	0
19	CIE	Command index error This bit is set automatically when response index differs from corresponding command index previously emitted. It depends on the enable in MMCHS_CMD[20] CICE register. Read 0x0: No error. Write 0x0: Status bit unchanged Read 0x1: Command index error Write 0x1: Status is cleared	RW	0
18	CEB	Command end bit error This bit is set automatically when detecting a 0 at the end bit position of a command response. Write 0x0: Status bit unchanged Read 0x0: No error. Read 0x1: Command end bit error Write 0x1: Status is cleared	RW	0
17	CCRC	Command CRC Error This bit is set automatically when there is a CRC7 error in the command response depending on the enable in MMCHS_CMD[19] CCCE register. Read 0x0: No Error. Write 0x0: Status bit unchanged Write 0x1: Status is cleared Read 0x1: Command CRC error	RW	0

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Bits	Field Name	Description	Type	Reset
16	CTO	Command Timeout Error This bit is set automatically when no response is received within 64 clock cycles from the end bit of the command. For commands that reply within 5 clock cycles - the timeout is still detected at 64 clock cycles. Write 0x0: Status bit unchanged Read 0x0: No error Read 0x1: Time Out Write 0x1: Status is cleared	RW	0
15	ERRI	Error Interrupt If any of the bits in the Error Interrupt Status register (MMCHS_STAT[24:15]) are set, then this bit is set to 1. Therefore the host driver can efficiently test for an error by checking this bit first. Writes to this bit are ignored. Read 0x0: No Interrupt. Read 0x1: Error interrupt event(s) occurred	R	0
14:11	RESERVED	Reserved. These bits are initialized to zero, and writes to them are ignored.	R	0x0
10	BSR	Boot status received interrupt This bit is set automatically when MMCHS_CON[18] BOOT_CF0 is set 0x0 or 0x1 and a boot status is received on DAT[0] line. This interrupt is only useful for MMC card. Write 0x0: Status bit unchanged Read 0x0: No Interrupt. Write 0x1: Status is cleared Read 0x1: Boot status received interrupt.	RW	0
9	OBI	Out-Of-Band interrupt This bit is set automatically when MMCHS_CON[14] OBIE is set and an Out-of-Band interrupt occurs on OBI pin. The interrupt detection depends on polarity controlled by MMCHS_CON[13] OBIP. This interrupt is only useful for MMC card. The Out-of-Band interrupt signal is a system specific feature for future use, this signal is not required for existing specification implementation. Read 0x0: No Out-Of-Band interrupt. Write 0x0: Status bit unchanged Read 0x1: Interrupt Out-Of-Band occurs Write 0x1: Status is cleared	RW	0
8	CIRQ	Card interrupt This bit is only used for SD and SDIO and CE-ATA cards. In 1-bit mode, interrupt source is asynchronous (can be a source of asynchronous wakeup). In 4-bit mode, interrupt source is sampled during the interrupt cycle. In CE-ATA mode, interrupt source is detected when the card drives CMD line to zero during one cycle after data transmission end.All modes above are fully exclusive. The controller interrupt must be clear by setting MMCHS_IE[8] CIRQ_ENABLE to 0, then the host driver must start the interrupt service with card (clearing card interrupt status) to remove card interrupt source. Otherwise the Controller interrupt will be reasserted as soon as MMCHS_IE[8] CIRQ_ENABLE is set to 1. Writes to this bit are ignored. Read 0x0: No card interrupt Read 0x1: Generate card interrupt	R	0

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Bits	Field Name	Description	Type	Reset
7	CREM	Card removal This bit is set automatically when MMCHS_PSTATE[16] CINS changes from 1 to 0. A clear of this bit doesn't affect Card inserted present state (MMCHS_PSTATE[16] CINS). Write 0x0: Status bit unchanged Read 0x0: Card state stable or Debouncing Read 0x1: Card removed Write 0x1: Status is cleared	RW	0
6	CINS	Card insertion This bit is set automatically when MMCHS_PSTATE[16] changes from 0 to 1. A clear of this bit doesn't affect Card inserted present state (MMCHS_PSTATE[16] CINS). Read 0x0: Card state stable or debouncing Write 0x0: Status bit unchanged Write 0x1: Status is cleared Read 0x1: Card inserted	RW	0
5	BRR	Buffer read ready This bit is set automatically during a read operation to the card (see class 2 - block oriented read commands) when one block specified by MMCHS_BLK[11:0] BLEN is completely written in the buffer. It indicates that the memory card has filled out the buffer and that the local host needs to empty the buffer by reading it. Note: If the DMA receive-mode is enabled, this bit is never set; instead a DMA receive request to the main DMA controller of the system is generated. Read 0x0: Not Ready to read buffer Write 0x0: Status bit unchanged Read 0x1: Ready to read buffer Write 0x1: Status is cleared	RW	0
4	BWR	Buffer write ready This bit is set automatically during a write operation to the card (see class 4 - block oriented write command) when the host can write a complete block as specified by MMCHS_BLK[11:0] BLEN. It indicates that the memory card has emptied one block from the buffer and that the local host is able to write one block of data into the buffer. Note: If the DMA transmit mode is enabled, this bit is never set; instead, a DMA transmit request to the main DMA controller of the system is generated. Write 0x0: Status bit unchanged Read 0x0: Not Ready to write buffer Read 0x1: Ready to write buffer Write 0x1: Status is cleared	RW	0
3	DMA	DMA interrupt : This status is set when an interrupt is required in the ADMA instruction and after the data transfer completion. Read 0x0: Dma interrupt detected Write 0x0: Status bit unchanged Write 0x1: Status is cleared Read 0x1: No dma interrupt	RW	0

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Bits	Field Name	Description	Type	Reset
2	BGE	Block gap event When a stop at block gap is requested (MMCHS_HCTL[16] SBGR), this bit is automatically set when transaction is stopped at the block gap during a read or write operation. This event does not occur when the stop at block gap is requested on the last block. In read mode, a 1-to-0 transition of the DAT Line active status (MMCHS_PSTATE[2] DLA) between data blocks generates a Block gap event interrupt. Read 0x0: No block gap event Write 0x0: Status bit unchanged Write 0x1: Status is cleared Read 0x1: Transaction stopped at block gap	RW	0
1	TC	Transfer completed This bit is always set when a read/write transfer is completed or between two blocks when the transfer is stopped due to a stop at block gap request (MMCHS_HCTL[16] SBGR). In Read mode: This bit is automatically set on completion of a read transfer (MMCHS_PSTATE[9] RTA). In write mode: This bit is set automatically on completion of the DAT line use (MMCHS_PSTATE[2] DLA). Write 0x0: Status bit unchanged Read 0x0: No transfer complete Write 0x1: Status is cleared Read 0x1: Data transfer complete	RW	0
0	CC	Command complete This bit is set when a 1-to-0 transition occurs in the register command inhibit (MMCHS_PSTATE[0] CMDI) If the command is a type for which no response is expected, then the command complete interrupt is generated at the end of the command. A command timeout error (MMCHS_STAT[16] CTO) has higher priority than command complete (MMCHS_STAT[0] CC). If a response is expected but none is received, then a command timeout error is detected and signaled instead of the command complete interrupt. Write 0x0: Status bit unchanged Read 0x0: No Command complete Write 0x1: Status is cleared Read 0x1: Command complete	RW	0

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Table 24-103. Register Call Summary for Register MMCHS_STAT

MMC/SD/SDIO Functional Description

- Power Management: [0] [1] [2] [3]
- Interrupt Requests: [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23] [24] [25] [26] [27] [28] [29] [30] [31] [32] [33]
- Interrupt-Driven Operation: [34] [35] [36] [37] [38] [39]
- Polling: [40] [41]
- Requirements for Descriptors: [42]
- Data Buffer: [43] [44] [45]
- Data Buffer Status: [46] [47] [48]
- Transfer or Command Status and Errors Reporting: [49] [50]
- Busy Time-Out for R1b, R5b Response Type: [51]
- Busy Time-Out After Write CRC Status: [52]
- Write CRC Status Time-Out: [53]
- Read Data Time-Out: [54] [55]
- Boot Acknowledge Time-Out: [56] [57] [58] [59] [60] [61]
- MMC CE-ATA Command Completion Disable Management: [62]

MMC/SD/SDIO Programming Guide

- Basic Operations for MMC/SD/SDIO Host Controller: [63] [64] [65] [66] [67] [68] [69] [70]
- Bus Voltage Selection: [71]
- Boot Mode Configuration: [72] [73]

MMC/SD/SDIO Register Manual

- MMC/SD/SDIO Register Summary: [74] [75]
- MMC/SD/SDIO Register Description: [76] [77] [78] [79] [80] [81] [82] [83] [84] [85] [86] [87] [88] [89] [90] [91] [92] [93] [94] [95] [96] [97] [98] [99] [100] [101] [102] [103] [104] [105] [106] [107] [108]

Table 24-104. MMCHS_IE

Address Offset	0x0000 0234		
Physical Address	0x4809 C234 0x480B 4234 0x480A D234 0x480D 1234 0x480D 5234	**Instance**	MMCHS1 MMCHS2 MMCHS3 MMCHS4 MMCHS5
Description	Interrupt SD enable register This register allows to enable/disable the module to set status bits, on an event-by-event basis. MMCHS_IE[31:16] = Error Interrupt Status Enable MMCHS_IE[15:0] = Normal Interrupt Status Enable		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		BADA_ENABLE	CERR_ENABLE	RESERVED		ADMAE_ENABLE	ACE_ENABLE	CLE	DEB_ENABLE	DCRC_ENABLE	DTO_ENABLE	CIE_ENABLE	CEB_ENABLE	CCRC_ENABLE	CTO_ENABLE	NULL	RESERVED				BSR_ENABLE	OBI_ENABLE	CIRQ_ENABLE	CREM_ENABLE	CINS_ENABLE	BRR_ENABLE	BWR_ENABLE	DMA_ENABLE	BGE_ENABLE	TC_ENABLE	CC_ENABLE

Bits	Field Name	Description	Type	Reset
31:30	RESERVED		R	0x0
29	BADA_ENABLE	Bad access to data space Interrupt Enable 0x0: Masked 0x1: Enabled	RW	0
28	CERR_ENABLE	Card error interrupt Enable 0x0: Masked 0x1: Enabled	RW	0

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Bits	Field Name	Description	Type	Reset
27:26	RESERVED	Reserved. These bits are initialized to zero, and writes to them are ignored.	R	0x0
25	ADMAE_ENABLE	ADMA error Interrupt Enable 0x0: Masked 0x1: Enabled	RW	0
24	ACE_ENABLE	Auto CMD12 error Interrupt Enable 0x0: Masked 0x1: Enabled	RW	0
23	CLE	Reserved bit. Current limit error is not supported. These bits are initialized to zero, and writes to them are ignored.	R	0
22	DEB_ENABLE	Data end bit error Interrupt Enable 0x0: Masked 0x1: Enabled	RW	0
21	DCRC_ENABLE	Data CRC error Interrupt Enable 0x0: Masked 0x1: Enabled	RW	0
20	DTO_ENABLE	Data timeout error Interrupt Enable 0x0: The data timeout detection is deactivated. The host controller provides the clock to the card until the card sends the data or the transfer is aborted. 0x1: The data timeout detection is enabled.	RW	0
19	CIE_ENABLE	Command index error Interrupt Enable 0x0: Masked 0x1: Enabled	RW	0
18	CEB_ENABLE	Command end bit error Interrupt Enable 0x0: Masked 0x1: Enabled	RW	0
17	CCRC_ENABLE	Command CRC error Interrupt Enable 0x0: Masked 0x1: Enabled	RW	0
16	CTO_ENABLE	Command timeout error Interrupt Enable 0x0: Masked 0x1: Enabled	RW	0
15	NULL	Fixed to 0 The host driver shall control error interrupts using the Error Interrupt Signal Enable register. Writes to this bit are ignored	R	0
14:11	RESERVED	Reserved. These bits are initialized to zero, and writes to them are ignored.	R	0x0
10	BSR_ENABLE	Boot status interrupt Enable A write to this register when MMCHS_CON[17] BOOT_ACK is set to 0x0 is ignored. 0x0: Masked 0x1: Enabled	RW	0
9	OBI_ENABLE	Out-of-Band interrupt Enable A write to this register when MMCHS_CON[14] OBIE is set to 0 is ignored. 0x0: Masked 0x1: Enabled	RW	0

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Bits	Field Name	Description	Type	Reset
8	CIRQ_ENABLE	Card interrupt Enable A clear of this bit also clears the corresponding status bit. During 1-bit mode, if the interrupt routine doesn't remove the source of a card interrupt in the SDIO card, the status bit is reasserted when this bit is set to 1. 0x0: Masked 0x1: Enabled	RW	0
7	CREM_ENABLE	Card removal Interrupt Enable 0x0: Masked 0x1: Enabled	RW	0
6	CINS_ENABLE	Card insertion Interrupt Enable 0x0: Masked 0x1: Enabled	RW	0
5	BRR_ENABLE	Buffer Read Ready Interrupt Enable 0x0: Masked 0x1: Enabled	RW	0
4	BWR_ENABLE	Buffer Write Ready Interrupt Enable 0x0: Masked 0x1: Enabled	RW	0
3	DMA_ENABLE	DMA interrupt Enable 0x0: Masked 0x1: Enabled	RW	0
2	BGE_ENABLE	Block Gap Event Interrupt Enable 0x0: Masked 0x1: Enabled	RW	0
1	TC_ENABLE	Transfer completed Interrupt Enable 0x0: Masked 0x1: Enabled	RW	0
0	CC_ENABLE	Command completed Interrupt Enable 0x0: Masked 0x1: Enabled	RW	0

Table 24-105. Register Call Summary for Register MMCHS_IE

MMC/SD/SDIO Functional Description
- Power Management: [0] [1]
- Interrupt Requests: [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23] [24]
- Interrupt-Driven Operation: [25] [26]

MMC/SD/SDIO Programming Guide
- MMC/SD/SDIO Host Controller Initialization Flow: [27]
- Basic Operations for MMC/SD/SDIO Host Controller: [28] [29] [30]

MMC/SD/SDIO Register Manual
- MMC/SD/SDIO Register Summary: [31] [32]
- MMC/SD/SDIO Register Description: [33] [34] [35] [36]

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Table 24-106. MMCHS_ISE

Address Offset	0x0000 0238		
Physical Address	0x4809 C238 0x480B 4238 0x480A D238 0x480D 1238 0x480D 5238	**Instance**	MMCHS1 MMCHS2 MMCHS3 MMCHS4 MMCHS5
Description	Interrupt signal enable register This register allows to enable/disable the module internal sources of status, on an event-by-event basis. MMCHS_ISE[31:16] = Error Interrupt Signal Enable MMCHS_ISE[15:0] = Normal Interrupt Signal Enable		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		BADA_SIGEN	CERR_SIGEN	RESERVED		ADMAE_SIGEN	ACE_SIGEN	CLE	DEB_SIGEN	DCRC_SIGEN	DTO_SIGEN	CIE_SIGEN	CEB_SIGEN	CCRC_SIGEN	CTO_SIGEN	NULL	RESERVED				BSR_SIGEN	OBI_SIGEN	CIRQ_SIGEN	CREM_SIGEN	CINS_SIGEN	BRR_SIGEN	BWR_SIGEN	DMA_SIGEN	BGE_SIGEN	TC_SIGEN	CC_SIGEN

Bits	Field Name	Description	Type	Reset
31:30	RESERVED		R	0x0
29	BADA_SIGEN	Bad access to data space signal status Enable 0x0: Masked 0x1: Enabled	RW	0
28	CERR_SIGEN	Card error interrupt signal status Enable 0x0: Masked 0x1: Enabled	RW	0
27:26	RESERVED	Reserved. These bits are initialized to zero, and writes to them are ignored.	R	0x0
25	ADMAE_SIGEN	ADMA error signal status Enable 0x0: Masked 0x1: Enabled	RW	0
24	ACE_SIGEN	Auto CMD12 error signal status Enable 0x0: Masked 0x1: Enabled	RW	0
23	CLE	Reserved bit. Current limit error is not supported. These bits are initialized to zero, and writes to them are ignored.	R	0
22	DEB_SIGEN	Data end bit error signal status Enable 0x0: Masked 0x1: Enabled	RW	0
21	DCRC_SIGEN	Data CRC error signal status Enable 0x0: Masked 0x1: Enabled	RW	0
20	DTO_SIGEN	Data timeout error signal status Enable 0x0: Masked 0x1: Enabled	RW	0
19	CIE_SIGEN	Command index error signal status Enable 0x0: Masked 0x1: Enabled	RW	0

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Bits	Field Name	Description	Type	Reset
18	CEB_SIGEN	Command end bit error signal status Enable 0x0: Masked 0x1: Enabled	RW	0
17	CCRC_SIGEN	Command CRC error signal status Enable 0x0: Masked 0x1: Enabled	RW	0
16	CTO_SIGEN	Command timeout error signal status Enable 0x0: Masked 0x1: Enabled	RW	0
15	NULL	Fixed to 0 The host driver shall control error interrupts using the Error Interrupt Signal Enable register. Writes to this bit are ignored	R	0
14:11	RESERVED	Reserved. These bits are initialized to zero, and writes to them are ignored.	R	0x0
10	BSR_SIGEN	Boot status signal status EnableA write to this register when MMCHS_CON[17] BOOT_ACK is set to 0x0 is ignored. 0x0: Masked 0x1: Enabled	RW	0
9	OBI_SIGEN	Out-Of-Band Interrupt signal status Enable A write to this register when MMCHS_CON[14] OBIE is set to 0 is ignored. 0x0: Masked 0x1: Enabled	RW	0
8	CIRQ_SIGEN	Card interrupt signal status Enable 0x0: Masked 0x1: Enabled	RW	0
7	CREM_SIGEN	Card removal signal status Enable 0x0: Masked 0x1: Enabled	RW	0
6	CINS_SIGEN	Card insertion signal status Enable 0x0: Masked 0x1: Enabled	RW	0
5	BRR_SIGEN	Buffer Read Ready signal status Enable 0x0: Masked 0x1: Enabled	RW	0
4	BWR_SIGEN	Buffer Write Ready signal status Enable 0x0: Masked 0x1: Enabled	RW	0
3	DMA_SIGEN	DMA interrupt Signal status enable 0x0: Masked 0x1: Enabled	RW	0
2	BGE_SIGEN	Black Gap Event signal status Enable 0x0: Masked 0x1: Enabled	RW	0
1	TC_SIGEN	Transfer completed signal status Enable 0x0: Masked 0x1: Enabled	RW	0

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Bits	Field Name	Description	Type	Reset
0	CC_SIGEN	Command completed signal status Enable 0x0: Masked 0x1: Enabled	RW	0

Table 24-107. Register Call Summary for Register MMCHS_ISE

MMC/SD/SDIO Functional Description
- Power Management: [0] [1]
- Interrupt Requests: [2] [3] [4] [5] [6]
- Polling: [7]

MMC/SD/SDIO Programming Guide
- Basic Operations for MMC/SD/SDIO Host Controller: [8]

MMC/SD/SDIO Register Manual
- MMC/SD/SDIO Register Summary: [9] [10]
- MMC/SD/SDIO Register Description: [11] [12] [13]

Table 24-108. MMCHS_AC12

Address Offset	0x0000 023C		
Physical Address	0x4809 C23C 0x480B 423C 0x480A D23C 0x480D 123C 0x480D 523C	**Instance**	MMCHS1 MMCHS2 MMCHS3 MMCHS4 MMCHS5
Description	Auto CMD12 Error Status Register The host driver may determine which of the errors cases related to Auto CMD12 has occurred by checking this MMCHS_AC12 register when an Auto CMD12 Error interrupt occurs. This register is valid only when Auto CMD12 is enabled (MMCHS_CMD[2] ACEN) and Auto CMD12Error (MMCHS_STAT[24] ACE) is set to 1. Note: These bits are automatically reset when starting a new adtc command with data.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								CNI	RESERVED		ACIE	ACEB	ACCE	ACTO	ACNE

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Reserved These bits are initialized to zero, and writes to them are ignored.	R	0x000000
7	CNI	Command not issue by Auto CMD12 error If this bit is set to 1, it means that pending command is not executed due to Auto CMD12 error : ACEB, ACCE, ACTO or ACNE. Read 0x0: Not error Read 0x1: Command not issued	R	0
6:5	RESERVED	Reserved These bits are initialized to zero, and writes to them are ignored.	R	0x0

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Bits	Field Name	Description	Type	Reset
4	ACIE	Auto CMD12 index error This bit is a set to 1 when response index differs from corresponding command auto CMD12 index previously emitted. This bit depends on the command index check enable (MMCHS_CMD[20] CICE). Read 0x0: No error Read 0x1: Auto CMD12 Index Error	R	0
3	ACEB	Auto CMD12 end bit error This bit is set to 1 when detecting a 0 at the end bit position of auto CMD12 command response. Read 0x0: No error Read 0x1: AutoCMD12 End bit Error	R	0
2	ACCE	Auto CMD12 CRC error This bit is automatically set to 1 when a CRC7 error is detected in the auto CMD12 command response depending on the enable in MMCHS_CMD[19] CCCE register. Read 0x0: No error Read 0x1: Auto CMD12 CRC Error	R	0
1	ACTO	Auto CMD12 timeout error This bit is set to 1 if no response is received within 64 clock cycles from the end bit of the auto CMD12 command. Read 0x0: No error Read 0x1: Auto CMD12 Time Out	R	0
0	ACNE	Auto CMD12 not executed This bit is set to 1 if multiple block data transfer command has started and if an error occurs in command before Auto CMD12 starts. Read 0x0: Auto CMD12 Executed Read 0x1: Auto CMD12 Not Executed	R	0

Table 24-109. Register Call Summary for Register MMCHS_AC12

MMC/SD/SDIO Programming Guide • Basic Operations for MMC/SD/SDIO Host Controller: [0] [1]
MMC/SD/SDIO Register Manual • MMC/SD/SDIO Register Summary: [2] [3] • MMC/SD/SDIO Register Description: [4] [5]

Table 24-110. MMCHS_CAPA

Address Offset	0x0000 0240		
Physical Address	0x4809 C240 0x480B 4240 0x480A D240 0x480D 1240 0x480D 5240	**Instance**	MMCHS1 MMCHS2 MMCHS3 MMCHS4 MMCHS5
Description	Capabilities register This register lists the capabilities of the MMC/SD/SDIO host controller.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			BIT64	RESERVED	VS18	VS30	VS33	SRS	DS	HSS	RESERVED	AD2S	RESERVED	MBL		RESERVED		BCF							TCU	RESERVED	TCF				

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Bits	Field Name	Description	Type	Reset
31:29	RESERVED	Reserved. These bits are initialized to zero, and writes to them are ignored.	R	0x0
28	BIT64	64-bit system bus support: Setting 1 to this bit indicates that the Host Controller supports 64-bit address descriptor mode and is connected to 64-bit address system bus. Read 0x0: 32-bit system bus address Read 0x1: 64-bit system bus address	R	0
27	RESERVED		R	0
26	VS18	Voltage support 1.8 V Initialization of this register (via a write access to this register) depends on the system capabilities. The host driver shall not modify this register after the initilaization. This register is only reinitialized by a hard reset (via RESETN signal) Write 0x0: 1.8 V not supported Read 0x0: 1.8 V not supported Read 0x1: 1.8 V supported Write 0x1: 1.8 V supported	RW	0
25	VS30	Voltage support 3.0 V Initialization of this register (via a write access to this register) depends on the system capabilities. The host driver shall not modify this register after the initilaization. This register is only reinitialized by a hard reset (via RESETN signal) Read 0x0: 3.0 V not supported Write 0x0: 3.0 V not supported Write 0x1: 3.0 V supported Read 0x1: 3.0 V supported	RW	0
24	VS33	Voltage support 3.3 V Initialization of this register (via a write access to this register) depends on the system capabilities. The host driver shall not modify this register after the initilaization. This register is only reinitialized by a hard reset (via RESETN signal) Read 0x0: 3.3 V not supported Write 0x0: 3.3 V not supported Write 0x1: 3.3 V supported Read 0x1: 3.3 V supported	RW	0
23	SRS	Suspend/Resume support (SDIO cards only) This bit indicates whether the host controller supports suspend/resume functionality. Read 0x0: The host controller does not suspend/resume functionality. Read 0x1: The host controller supports suspend/resume functionality.	R	1
22	DS	DMA support This bit indicates that the Host Controller is able to use DMA to transfer data between system memory and the Host Controller directly. Read 0x0: DMA not supported Read 0x1: DMA supported	R	1
21	HSS	High-speed support This bit indicates that the host controller supports high-speed operations and can supply an up-to maximum card frequency. Read 0x0: High speed not supported Read 0x1: High speed supported	R	1

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Bits	Field Name	Description	Type	Reset
20	RESERVED	Reserved. This bit is initialized to zero, and writes to it are ignored.	R	0
19	AD2S	ADMA2 support: This bit indicates whether the host controller is capable of using ADMA2. It depends on setting of generic parameter MMCHS_HL_HWINFO[0] MADMA_EN Read 0x0: ADMA2 not supported Read 0x1: ADMA2 supported	R	1
18	RESERVED	Reserved. This bit is initialized to zero, and writes to it are ignored.	R	0
17:16	MBL	Maximum block length This value indicates the maximum block size that the host driver can read and write to the buffer in the host controller. This value depends on definition of generic parameter with a max value of 2048 bytes. The host controller supports 512- byte and 1024-byte block transfers. Read 0x0: 512 bytes Read 0x1: 1024 bytes Read 0x2: 2048 bytes	R	0x1
15:14	RESERVED	Reserved. These bits are initialized to zero, and writes to them are ignored.	R	0x0
13:8	BCF	Base clock frequency for clock provided to the card. Read 0x0: The value indicating the base (maximum) frequency for the output clock provided to the card is system dependent and is not available in this register. Get the information via another method.	R	0x00
7	TCU	Timeout clock unit This bit shows the unit of base clock frequency used to detect Data Timeout Error (MMCHS_STAT[20] DTO). Read 0x0: kHz Read 0x1: MHz	R	1
6	RESERVED	Reserved. This bit is initialized to zero, and writes to it are ignored.	R	0
5:0	TCF	Timeout clock frequency The timeout clock frequency is used to detect Data Timeout Error (MMCHS_STAT[20] DTO). Read 0x0: The timeout clock frequency depends on the frequency of the clock provided to the card. The value of the timeout clock frequency is not available in this register.	R	0x00

Table 24-111. Register Call Summary for Register MMCHS_CAPA

MMC/SD/SDIO Functional Description • Software Reset: [0] • Data Buffer: [1]
MMC/SD/SDIO Programming Guide • MMC/SD/SDIO Host Controller Initialization Flow: [2]
MMC/SD/SDIO Register Manual • MMC/SD/SDIO Register Summary: [3] [4] • MMC/SD/SDIO Register Description: [5] [6] [7] [8]

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Table 24-112. MMCHS_CUR_CAPA

Address Offset	0x0000 0248		
Physical Address	0x4809 C248 0x480B 4248 0x480A D248 0x480D 1248 0x480D 5248	**Instance**	MMCHS1 MMCHS2 MMCHS3 MMCHS4 MMCHS5
Description	Maximum current capabilities Register This register indicates the maximum current capability for each voltage. The value is meaningful if the voltage support is set in the capabilities register (MMCHS_CAPA). Initialization of this register (via a write access to this register) depends on the system capabilities. The host driver shall not modify this register after the initilaization. This register is only reinitialized by a hard reset (via RESETN signal)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								CUR_1V8								CUR_3V0								CUR_3V3							

Bits	Field Name	Description	Type	Reset
31:24	RESERVED	Reserved. This bit is initialized to zero, and writes to it are ignored.	R	0x00
23:16	CUR_1V8	Maximum current for 1.8V Read 0x0: The maximum current capability for this voltage is not available. Feature not implemented.	RW	0x00
15:8	CUR_3V0	Maximum current for 3.0V Read 0x0: The maximum current capability for this voltage is not available. Feature not implemented.	RW	0x00
7:0	CUR_3V3	Maximum current for 3.3V Read 0x0: The maximum current capability for this voltage is not available. Feature not implemented.	RW	0x00

Table 24-113. Register Call Summary for Register MMCHS_CUR_CAPA

MMC/SD/SDIO Functional Description • Software Reset: [0]
MMC/SD/SDIO Programming Guide • MMC/SD/SDIO Host Controller Initialization Flow: [1]
MMC/SD/SDIO Register Manual • MMC/SD/SDIO Register Summary: [2] [3]

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Table 24-114. MMCHS_FE

Address Offset	0x0000 0250		
Physical Address	0x4809 C250 0x480B 4250 0x480A D250 0x480D 1250 0x480D 5250	**Instance**	MMCHS1 MMCHS2 MMCHS3 MMCHS4 MMCHS5
Description	Force Event Register for Error Interrupt status The force Event Register is not a physically implemented register. Rather, it is an address at which the Error Interrupt Status register can be written. The effect of a write to this address will be reflected in the Error Interrupt Status Register, if corresponding bit of the Error Interrupt Status Enable Register is set.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		FE_BADA	FE_CERR	RESERVED		FE_ADMAE	FE_ACE	FE_CLE	FE_DEB	FE_DCRC	FE_DTO	FE_CIE	FE_CEB	FE_CCRC	FE_CTO	RESERVED								FE_CNI	RESERVED		FE_ACIE	FE_ACEB	FE_ACCE	FE_ACTO	FE_ACNE

Bits	Field Name	Description	Type	Reset
31:30	RESERVED	Reserved. These bits are initialized to zero, and writes to them are ignored.	N/A[1]	0x0
29	FE_BADA	Force Event Bad access to data space Write 0x0: No effect, No Interrupt. Write 0x1: Interrupt Forced	W	0
28	FE_CERR	Force Event Card error Write 0x0: No effect, No Interrupt. Write 0x1: Interrupt Forced	W	0
27:26	RESERVED	Reserved. These bits are initialized to zero, and writes to them are ignored.	N/A[1]	0x0
25	FE_ADMAE	Force Event ADMA Error: Write 0x0: No effect, No Interrupt. Write 0x1: Interrupt Forced	W	0
24	FE_ACE	Force Event Auto CMD12 error Write 0x0: No effect, No Interrupt. Write 0x1: Interrupt Forced	W	0
23	FE_CLE	Reserved. Current limit error is not supported. These bits are initialized to zero, and writes to them are ignored.	N/A[1]	0
22	FE_DEB	Force Event Data End Bit error Write 0x0: No effect, No Interrupt. Write 0x1: Interrupt Forced	W	0
21	FE_DCRC	Force Event Data CRC Error Write 0x0: No effect, No Interrupt. Write 0x1: Interrupt Forced	W	0
20	FE_DTO	Force Event Data timeout error Write 0x0: No effect, No Interrupt. Write 0x1: Interrupt Forced	W	0

(1) N/A = Not accessible

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Bits	Field Name	Description	Type	Reset
19	FE_CIE	Force Event Command index error Write 0x0: No effect, No Interrupt. Write 0x1: Interrupt Forced	W	0
18	FE_CEB	Force Event Command end bit error Write 0x0: No effect, No Interrupt. Write 0x1: Interrupt Forced	W	0
17	FE_CCRC	Force Event Command CRC Error Write 0x0: No effect, No Interrupt. Write 0x1: Interrupt Forced	W	0
16	FE_CTO	Command Timeout Error This bit is set automatically when no response is received within 64 clock cycles from the end bit of the command. For commands that reply within 5 clock cycles - the timeout is still detected at 64 clock cycles. Write 0x0: Status bit unchanged Write 0x1: Status is cleared	W	0
15:8	RESERVED	Reserved. These bits are initialized to zero, and writes to them are ignored.	N/A[2]	0x00
7	FE_CNI	Force Event Command not issue by Auto CMD12 error Write 0x0: No effect, No Interrupt. Write 0x1: Interrupt Forced	W	0
6:5	RESERVED	Reserved These bits are initialized to zero, and writes to them are ignored.	N/A[2]	0x0
4	FE_ACIE	Force Event Auto CMD12 index error Write 0x0: No effect, No Interrupt. Write 0x1: Interrupt Forced	W	0
3	FE_ACEB	Force Event Auto CMD12 end bit error Write 0x0: No effect, No Interrupt. Write 0x1: Interrupt Forced	W	0
2	FE_ACCE	Force Event Auto CMD12 CRC error Write 0x0: No effect, No Interrupt. Write 0x1: Interrupt Forced	W	0
1	FE_ACTO	Force Event Auto CMD12 timeout error Write 0x0: No effect, No Interrupt. Write 0x1: Interrupt Forced	W	0
0	FE_ACNE	Force Event Auto CMD12 not executed Write 0x0: No effect, No Interrupt. Write 0x1: Interrupt Forced	W	0

(2) N/A = Not accessible

Table 24-115. Register Call Summary for Register MMCHS_FE

MMC/SD/SDIO Functional Description
- Test Registers: [0]

MMC/SD/SDIO Register Manual
- MMC/SD/SDIO Register Summary: [1] [2]

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Table 24-116. MMCHS_ADMAES

Address Offset	0x0000 0254		
Physical Address	0x4809 C254 0x480B 4254	**Instance**	MMCHS1 MMCHS2
Description	ADMA Error Status Register When ADMA Error Interrupt is occurred, the ADMA Error States field in this register holds the ADMA state and the ADMA System Address Register holds the address around the error descriptor. For recovering the error, the Host Driver requires the ADMA state to identify the error descriptor address as follows: ST_STOP: Previous location set in the ADMA System Address register is the error descriptor address ST_FDS: Current location set in the ADMA System Address register is the error descriptor address ST_CADR: This sate is never set because do not generate ADMA error in this state. ST_TFR: Previous location set in the ADMA System Address register is the error descriptor address In case of write operation, the Host Driver should use ACMD22 to get the number of written block rather than using this information, since unwritten data may exist in the Host Controller. The Host Controller generates the ADMA Error Interrupt when it detects invalid descriptor data (Valid=0) at the ST_FDS state. In this case, ADMA Error State indicates that an error occurs at ST_FDS state. The Host Driver may find that the Valid bit is not set in the error descriptor.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													LME	AES	

Bits	Field Name	Description	Type	Reset
31:3	RESERVED		R	0x0000 0000
2	LME	ADMA Length Mismatch Error: (1) While Block Count Enable being set, the total data length specified by the Descriptor table is different from that specified by the Block Count and Block Length. (2) Total data length can not be divided by the block length. 0x0: No Error 0x1: Error	RW	0
1:0	AES	ADMA Error State his field indicates the state of ADMA when error is occurred during ADMA data transfer. This field never indicates "10" because ADMA never stops in this state. 0x0: ST_STOP (Stop DMA)Contents of SYS_SDR register 0x1: ST_STOP (Stop DMA)Points the error descriptor 0x2: Never set this state(Not used) 0x3: ST_TFR (Transfer Data)Points the next of the error descriptor	RW	0x0

Table 24-117. Register Call Summary for Register MMCHS_ADMAES

MMC/SD/SDIO Functional Description

- Requirements for Descriptors: [0]

MMC/SD/SDIO Register Manual

- MMC/SD/SDIO Register Summary: [1] [2]

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Table 24-118. MMCHS_ADMASAL

Address Offset	0x0000 0258		
Physical Address	0x4809 C258 0x480B 4258	**Instance**	MMCHS1 MMCHS2
Description	ADMA System address Low bits		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADMA_A32B																															

Bits	Field Name	Description	Type	Reset
31:0	ADMA_A32B	ADMA System address 32 bits.This register holds byte address of executing command of the Descriptor table. 32-bit Address Descriptor uses lower 32-bit of this register. At the start of ADMA, the Host Driver shall set start address of the Descriptor table. The ADMA increments this register address, which points to next line, when every fetching a Descriptor line. When the ADMA Error Interrupt is generated, this register shall hold valid Descriptor address depending on the ADMA state. The Host Driver shall program Descriptor Table on 32-bit boundary and set 32-bit boundary address to this register. ADMA2 ignores lower 2-bit of this register and assumes it to be 00b.	RW	0x0000 0000

Table 24-119. Register Call Summary for Register MMCHS_ADMASAL

MMC/SD/SDIO Functional Description

- Master DMA Operations: [0] [1]
- Requirements for Descriptors: [2]
- Advanced DMA Description: [3] [4] [5]

MMC/SD/SDIO Register Manual

- MMC/SD/SDIO Register Summary: [6] [7]

Table 24-120. MMCHS_REV

Address Offset	0x0000 02FC		
Physical Address	0x4809 C2FC 0x480B 42FC 0x480A D2FC 0x480D 12FC 0x480D 52FC	**Instance**	MMCHS1 MMCHS2 MMCHS3 MMCHS4 MMCHS5
Description	Versions Register This register contains the hard coded RTL vendor revision number, the version number of SD specification compliancy and a slot status bit. MMCHS_REV[31:16] = Host controller version MMCHS_REV[15:0] = Slot Interrupt Status		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VREV								SREV								RESERVED															SIS

Bits	Field Name	Description	Type	Reset
31:24	VREV	Vendor Version Number: IP revision [7:4] Major revision [3:0] Minor revision Examples: 0x10 for 1.0 0x21 for 2.1	R	0x--

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Bits	Field Name	Description	Type	Reset
23:16	SREV	Specification Version Number This status indicates the Standard SD Host Controller Specification Version. The upper and lower 4-bits indicate the version. Read 0x0: SD Host Specification Version 1.0 Read 0x1: SD Host Specification Version 2.0	R	0x01
15:1	RESERVED	Reserved These bits are initialized to zero, and writes to them are ignored.	R	0x0000
0	SIS	Slot Interrupt Status This status bit indicates the inverted state of interrupt signal for the module. By a power on reset or by setting a software reset for all (MMCHS_SYSCTL[24] SRA), the interrupt signal shall be de-asserted and this status shall read 0.	R	0

Table 24-121. Register Call Summary for Register MMCHS_REV

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- MMC/SD/SDIO Register Summary: [0] [1]
- MMC/SD/SDIO Register Description: [2] [3]

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General-Purpose Interface

This chapter describes the general-purpose interface on the device.

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25.2 General-Purpose Interface Environment 5381
25.3 General-Purpose Interface Integration 5386
25.4 General-Purpose Interface Functional Description 5390
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25.1 General-Purpose Interface Overview

The general-purpose interface combines six general-purpose input/output (GPIO) banks.

Each GPIO module provides 32 dedicated general-purpose pins with input and output capabilities; thus, the general-purpose interface supports up to 192 (6 × 32) pins.

These pins can be configured for the following applications:

- Data input (capture)/output (drive)
- Keyboard interface with a debounce cell
- Interrupt generation in active mode upon the detection of external events. Detected events are processed by two parallel independent interrupt-generation submodules to support biprocessor operations.
- Wake-up request generation in idle mode upon the detection of external events

These modules do not include pad control (pullup/pulldown control, open-drain feature). For more information, see Section 18.4.8, *Pad Functional Multiplexing and Configuration,* in Chapter 18, *Control Module*.

Figure 25-1 is an overview of the general-purpose interface.

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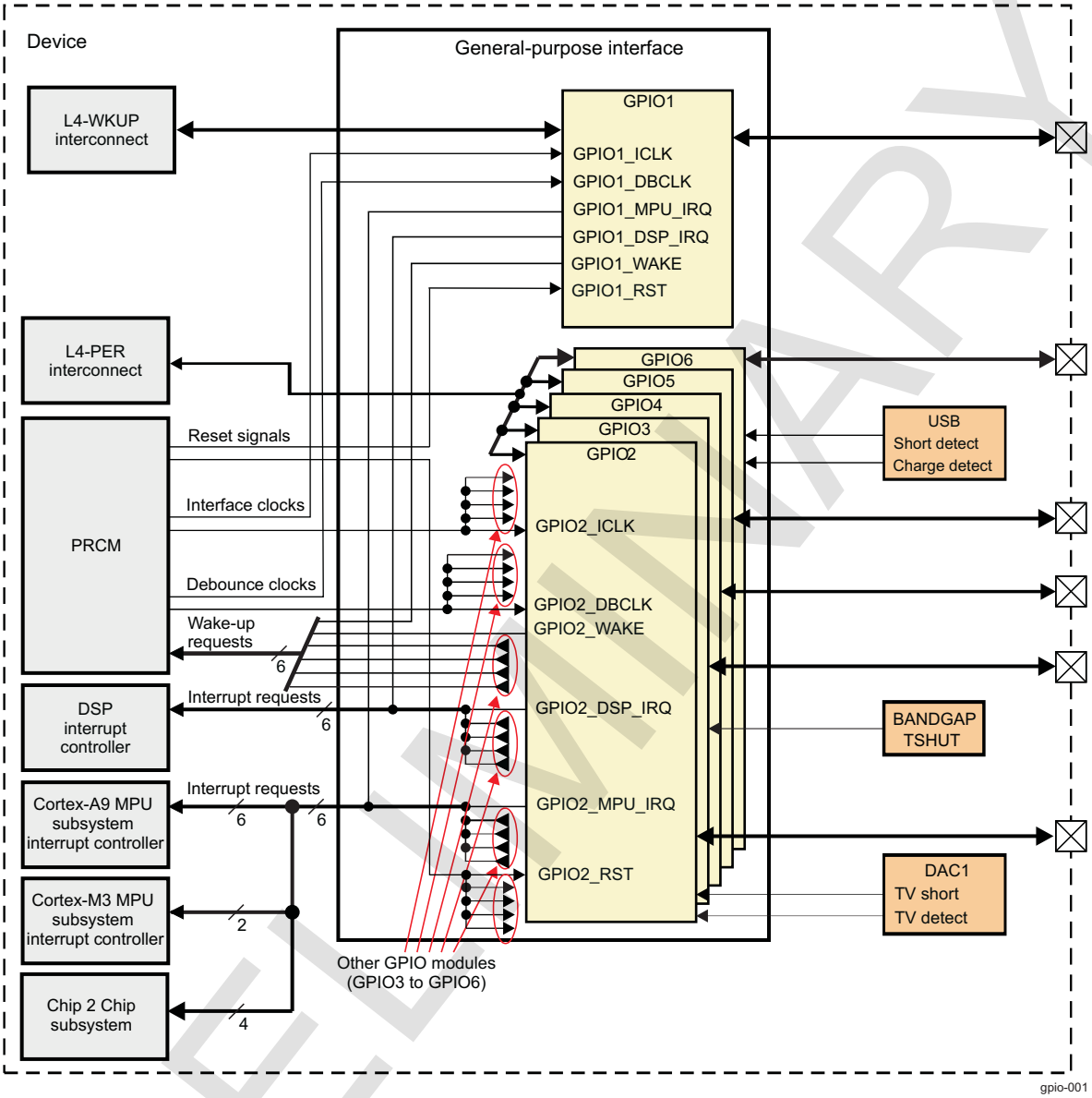
Figure 25-1. General-Purpose Interface Overview



The GPIOs include the following global features:

- Synchronous interrupt requests in active mode from each channel are processed by two identical interrupt generation submodules used independently by the digital signal processor (DSP) and microprocessor unit (MPU) Cortex™-A9 and Cortex™-M3 subsystems. One of these interrupts is mapped on the DSP subsystem interrupt controller (INTC) and the other on the MPU Cortex-A9 and Cortex-M3 subsystem INTCs.
- Asynchronous wake-up requests in idle mode from input channels are merged together to issue one wake-up signal per GPIO.
- Data input (capture)/output (drive)
- Power management support

The general-purpose interface has 12 interrupt lines (two interrupt lines per each GPIO instance).

Each GPIO produces a wake-up request signal to the power, reset, and clock management (PRCM) module.

Each channel in the GPIOs has the following features:

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- The GPIOi.GPIO_OE register controls the output capability for each pin.
- The output line level reflects the value written in the GPIOi.GPIO_DATAOUT register through the L4 interconnect.
- The input line can be fed to the GPIO through an optional and configurable debounce cell. (Because the debouncing time value is global for all ports of one GPIO, up to five different debouncing time values are possible.)
- The input line value is sampled into the GPIOi.GPIO_DATAIN register and can be read through the L4 interconnect.
- In active mode, the input line can be used through level and edge detectors to trigger synchronous interrupts. The edge (rising, falling, or both) or the level used (logical 0, logical 1, or both) can be configured.
- In idle mode, the input line can be used to activate the asynchronous wake-up request (on edge detection: rising edge, falling edge, or both).

The module provides an alternative to the atomic test and set operations for the following registers:

- GPIOi.GPIO_DATAOUT
- GPIOi.GPIO_IRQSTATUS_SET_0
- GPIOi.GPIO_IRQSTATUS_SET_1
- GPIOi.GPIO_IRQSTATUS_CLR_0
- GPIOi.GPIO_IRQSTATUS_CLR_1
- GPIOi.GPIO_IRQWAKEN_0
- GPIOi.GPIO_IRQWAKEN_1

For these registers, the modules implement the set-and-clear protocol register update (see Section 25.4.9, *General-Purpose Interface Set-and-Clear Protocol*).

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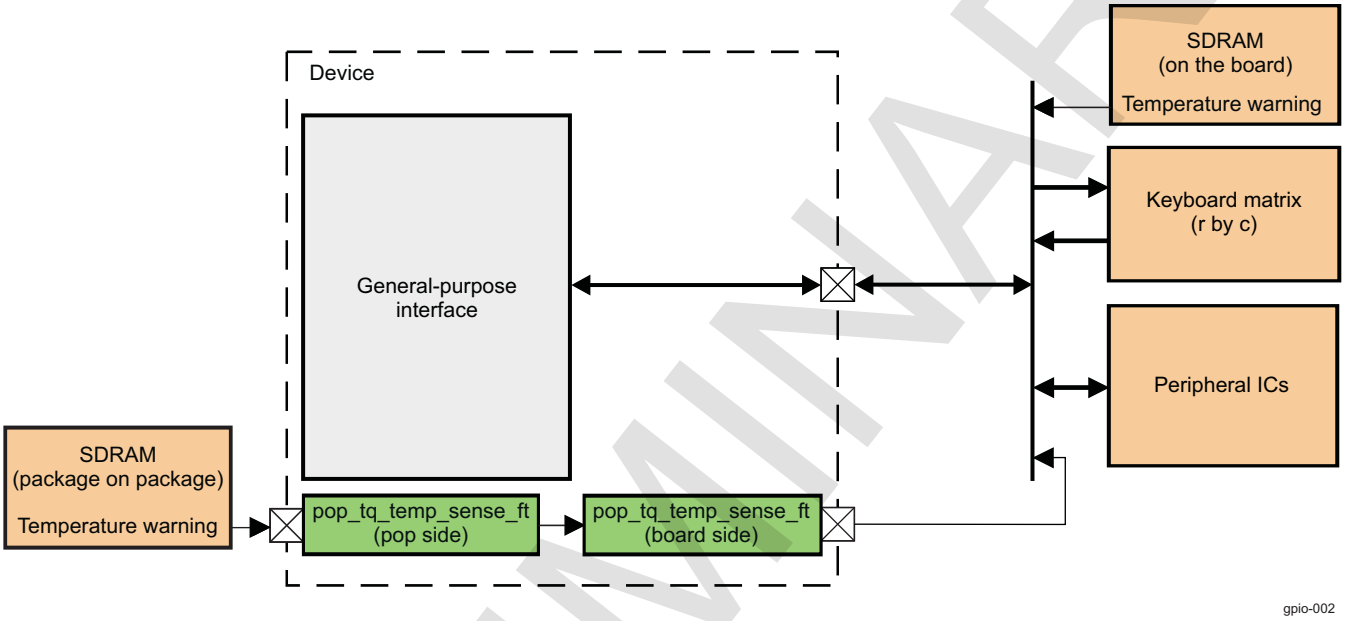
25.2 General-Purpose Interface Environment

The general-purpose interface combines six GPIO modules for a flexible, user-programmable, GPIO controller. The general-purpose interface implements functions that are not implemented with the dedicated controllers in the device and require simple input and/or output software-controlled signals. The general-purpose interface allows a variety of custom connections and expands the I/O capabilities of the system to the real world.

Figure 25-2 shows a typical application using the general-purpose interface.

Figure 25-2. General-Purpose Interface Typical Application



NOTE: Most memories provide a temperature sensor to control the autorefresh duty cycle. The device monitors the temperature of the external memory using the pop_tq_temp_sense_ft ball and a GPIO input. To do this, pop_tq_temp_sense_ft is connected to a GPIO through the customer board. This feature is application-dependent.

CAUTION

Because of buffer strength, an external serial resistor must be connected to the balls where gpio_120 through gpio_129 are muxed with MMC signals.

The general-purpose interface can physically connect the device to a keyboard matrix and peripheral integrated circuits (ICs).

25.2.1 General-Purpose Interface as a Keyboard Interface

The general-purpose interface can be used as a keyboard interface. Channels can be dedicated based on the keyboard matrix (r × c). Figure 25-3 shows row channels configured as inputs with the input debounce feature enabled. The row channels are driven high with an external pullup. Column channels are configured as outputs and drive a low level.

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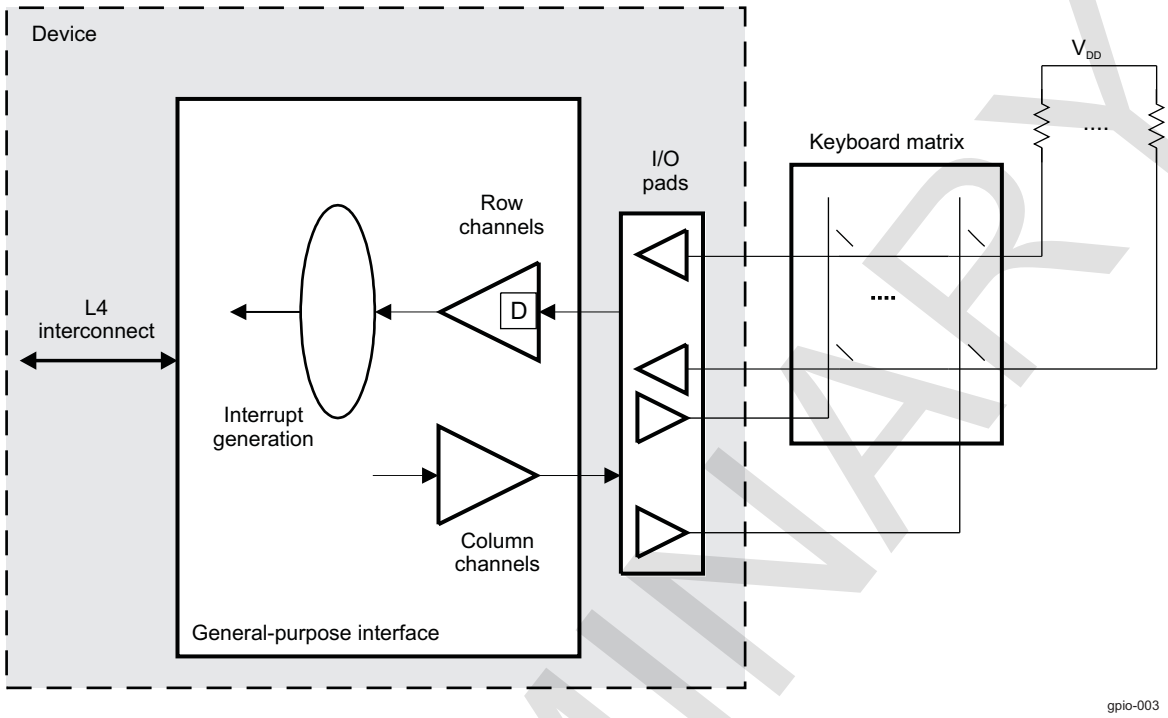
Figure 25-3. General-Purpose Interface Used as a Keyboard Interface



When a keyboard matrix key is pressed, the corresponding row and column lines are shorted together and a low level is driven on the corresponding row channel. This generates an interrupt based on the proper configuration (see Section 25.4.6, *Interrupt and Wake-Up Requests*).

When the keyboard interrupt is received, the processor (MPU and/or DSP subsystem) can disable the keyboard interrupt and scan the column channels for the key coordinates.

- The scanning sequence has as many states as column channels: For each step in the sequence, the processor drives one column channel low and the others high.
- The processor reads the values of the row channels and thus detects which keys in the column are pressed.

At the end of the scanning sequence, the processor establishes which keys are pressed. The keyboard interface can then be reconfigured in the interrupt waiting state.

25.2.2 General-Purpose Interface Signals

Table 25-1 describes the module signals.

Table 25-1. I/O Description

Signal	I/O [1]	Description	Reset Value
gpio_[1:0]	I/O	GPIO	HiZ
gpio_wk[1:0]	I/O	GPIO (direct wake-up path). Shares the same GPIO channels with gpio_[1:0].	HiZ
gpio_[3:2]	I/O	GPIO	HiZ
gpio_wk[3:2]	I/O	GPIO (direct wake-up path). Shares the same GPIO channels with gpio_[3:2].	HiZ
gpio_wk4	I/O	GPIO (direct wake-up path)	HiZ
gpi_wk5	I	GPIO input only (direct wake-up path)	HiZ
gpio_wk[10:6]	I/O	GPIO (direct wake-up path)	HiZ
gpio_[28:11]	I/O	GPIO	HiZ

(1) I = Input; O = Output

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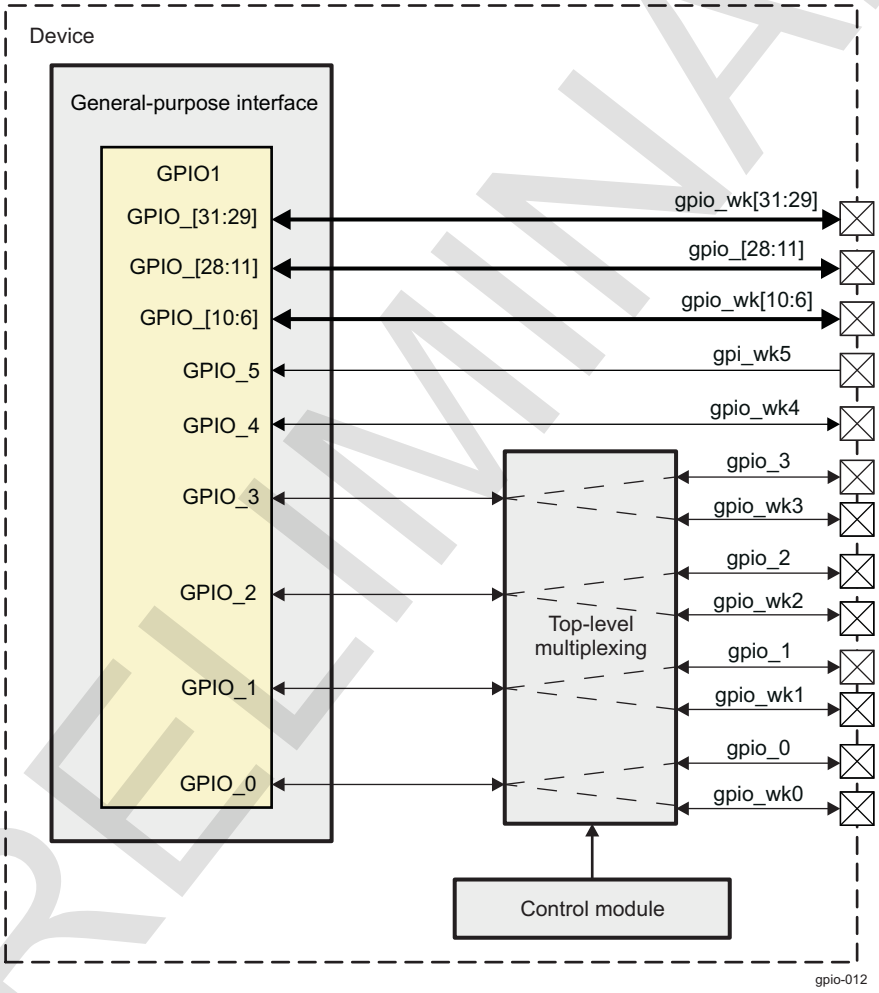
Table 25-1. I/O Description (continued)

Signal	I/O [1]	Description	Reset Value
gpio_wk[31:29]	I/O	GPIO (direct wake-up path)	HiZ
gpio_[56:32]	I/O	GPIO	HiZ
gpio_[66:59]	I/O	GPIO	HiZ
gpi_[80:67]	I	GPIO inputs only	HiZ
gpio_[178:81]	I/O	GPIO	HiZ
gpio_[191:181]	I/O	GPIO	HiZ

Figure 25-4 shows the signal connections of GPIO1.

Figure 25-4. GPIO1 Signal Connections



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NOTE: Users must not use a GPIO channel through two device pads simultaneously. Channels that can be mapped on two different device pads are:

- GPIO[3:0] of the GPIO1 module (signals gpio_[3:0] or gpio_wk[3:0]; each can be routed to a different device pad). See Figure 25-4.
- GPIO[8:4] of the GPIO4 module (signals gpio_[104:100]; each can be routed to two different device pads)

Therefore, appropriate configuration must be done through the pad configuration registers. See Section 18.4.8, *Pad Functional Multiplexing and Configuration*, in Chapter 18, *Control Module*.

Figure 25-5 shows the signal connections of GPIO2 through GPIO6.

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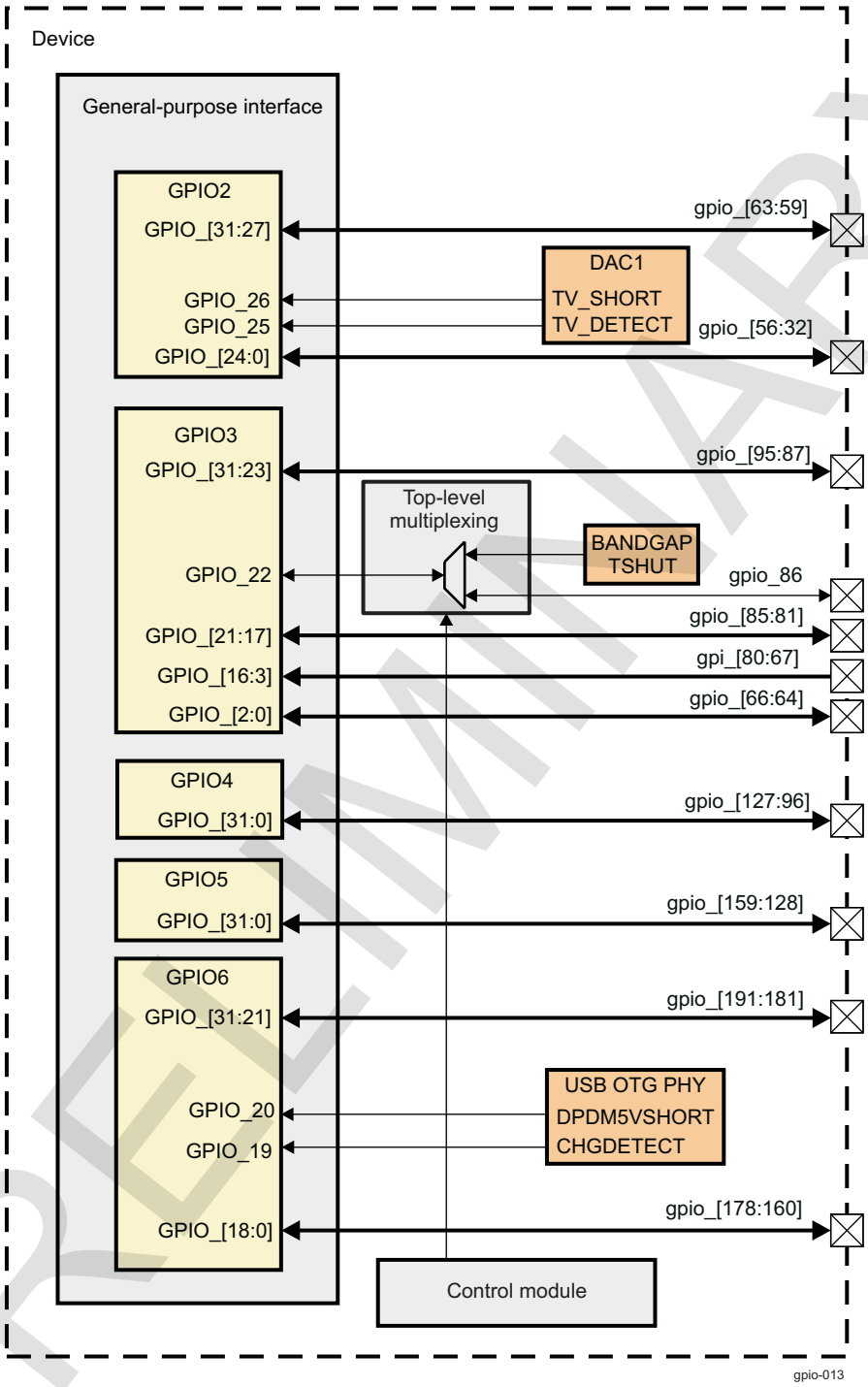
Figure 25-5. GPIO2 Through GPIO6 Signal Connections



NOTE: The GPIO_22 channel of the GPIO3 module receives a thermal shutdown (TSHUT) signal from the BANDGAP module whenever pad mux mode is not set to 3 (gpio_86 signal selected). See Section 18.4.8, *Pad Functional Multiplexing and Configuration*, in Chapter 18, *Control Module*.

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NOTE: For more information about the signals and channel descriptions of GPIO1 through GPIO6, see Section 25.4.7, *General-Purpose Interface Channels Description.*

NOTE: For more information about GPIO signal multiplexing, see Section 18.4.8, *Pad Functional Multiplexing and Configuration,* in Chapter 18, *Control Module*.

25.3 General-Purpose Interface Integration

This section describes module integration in the device, including information about clocks, resets, and hardware requests.

Figure 25-6 shows this module integration.

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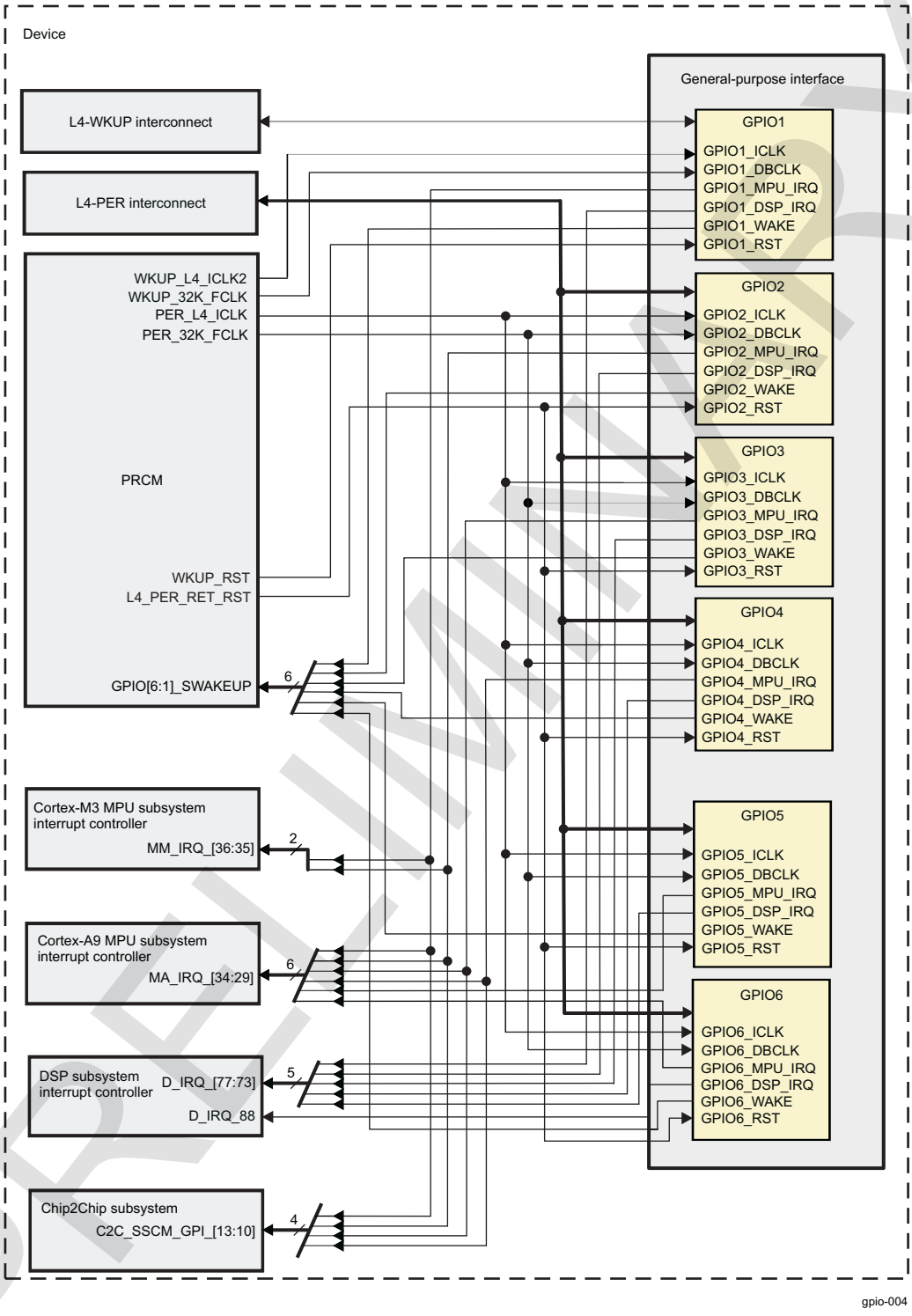
Figure 25-6. GPIO Integration



NOTE: For more information about the IDLE hardware handshake and the wake-up request, see Section 3.1.1.1, *Clock Management*, in Chapter 3, *Power, Reset, and Clock Management*.

Table 25-2 through Table 25-4 summarize the integration of the module in the device.

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Table 25-2. Integration Attributes

Module Instance	Attributes	
	Power Domain	Interconnect
GPIO1	PD_WKUP	L4-WKUP
GPIOi, where i = 2 to 6	PD_L4_PER	L4-PER

Table 25-3. Clocks and Resets

Clocks				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
GPIO1	GPIO1_ICLK	WKUP_L4_ICLK	PRCM	GPIO interface clock
GPIO1	GPIO1_DBCLK	WKUP_32K_FCLK	PRCM	GPIO debounce clock
GPIO2	GPIO2_ICLK	PER_L4_ICLK	PRCM	GPIO interface clock
GPIO2	GPIO2_DBCLK	PER_32K_FCLK	PRCM	GPIO debounce clock
GPIO3	GPIO3_ICLK	PER_L4_ICLK	PRCM	GPIO interface clock
GPIO3	GPIO3_DBCLK	PER_32K_FCLK	PRCM	GPIO debounce clock
GPIO4	GPIO4_ICLK	PER_L4_ICLK	PRCM	GPIO interface clock
GPIO4	GPIO4_DBCLK	PER_32K_FCLK	PRCM	GPIO debounce clock
GPIO5	GPIO5_ICLK	PER_L4_ICLK	PRCM	GPIO interface clock
GPIO5	GPIO5_DBCLK	PER_32K_FCLK	PRCM	GPIO debounce clock
GPIO6	GPIO6_ICLK	PER_L4_ICLK	PRCM	GPIO interface clock
GPIO6	GPIO6_DBCLK	PER_32K_FCLK	PRCM	GPIO debounce clock
Resets				
GPIO1	GPIO1_RST	WKUP_RST	PRCM	GPIO reset signal
GPIO2	GPIO2_RST	L4_PER_RET_RST	PRCM	GPIO reset signal
GPIO3	GPIO3_RST	L4_PER_RET_RST	PRCM	GPIO reset signal
GPIO4	GPIO4_RST	L4_PER_RET_RST	PRCM	GPIO reset signal
GPIO5	GPIO5_RST	L4_PER_RET_RST	PRCM	GPIO reset signal
GPIO6	GPIO6_RST	L4_PER_RET_RST	PRCM	GPIO reset signal

Table 25-4. Hardware Requests

Interrupt Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
GPIO1	GPIO1_DSP_IRQ	D_IRQ_73	DSP	An interrupt to DSP (second interrupt)
GPIO1	GPIO1_MPU_IRQ	MA_IRQ_29	Cortex-A9	An interrupt to MPU subsystem INTC (first interrupt)
GPIO1	GPIO1_MPU_IRQ	MM_IRQ_35	Cortex-M3	An interrupt to MPU subsystem INTC (first interrupt)
GPIO1	GPIO1_MPU_IRQ	C2C_SSCM_GPI_10	C2C	An interrupt to distant device through the chip2chip (C2C) subsystem (first interrupt)
GPIO2	GPIO2_DSP_IRQ	D_IRQ_74	DSP	An interrupt to DSP (second interrupt)
GPIO2	GPIO2_MPU_IRQ	MA_IRQ_30	Cortex-A9	An interrupt to MPU subsystem INTC (first interrupt)
GPIO2	GPIO2_MPU_IRQ	MM_IRQ_36	Cortex-M3	An interrupt to MPU subsystem INTC (first interrupt)
GPIO2	GPIO2_MPU_IRQ	C2C_SSCM_GPI_11	C2C	An interrupt to distant device through C2C subsystem (first interrupt)
GPIO3	GPIO3_DSP_IRQ	D_IRQ_75	DSP	An interrupt to DSP (second interrupt)
GPIO3	GPIO3_MPU_IRQ	MA_IRQ_31	Cortex-A9	An interrupt to MPU subsystem INTC (first interrupt)

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Table 25-4. Hardware Requests (continued)

GPIO3	GPIO3_MPU_IRQ	C2C_SSCM_GPI_12	C2C	An interrupt to distant device through C2C subsystem (first interrupt)
GPIO4	GPIO4_DSP_IRQ	D_IRQ_76	DSP	An interrupt to DSP (second interrupt)
GPIO4	GPIO4_MPU_IRQ	MA_IRQ_32	Cortex-A9	An interrupt to MPU subsystem INTC (first interrupt)
GPIO4	GPIO4_MPU_IRQ	C2C_SSCM_GPI_13	C2C	An interrupt to distant device through C2C subsystem (first interrupt)
GPIO5	GPIO5_DSP_IRQ	D_IRQ_77	DSP	An interrupt to DSP (second interrupt)
GPIO5	GPIO5_MPU_IRQ	MA_IRQ_33	Cortex-A9	An interrupt to MPU subsystem INTC (first interrupt)
GPIO6	GPIO6_DSP_IRQ	D_IRQ_88	DSP	An interrupt to DSP (second interrupt)
GPIO6	GPIO6_MPU_IRQ	MA_IRQ_34	Cortex-A9	An interrupt to MPU subsystem INTC (first interrupt)

NOTE: For a description of interrupt source, see Section 25.4.6, *General-Purpose Interface Interrupt and Wake-Up Requests*.

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25.4 General-Purpose Interface Functional Description

25.4.1 General-Purpose Interface Block Diagram

Figure 25-7 shows the general-purpose interface.

Figure 25-7. General-Purpose Interface Description

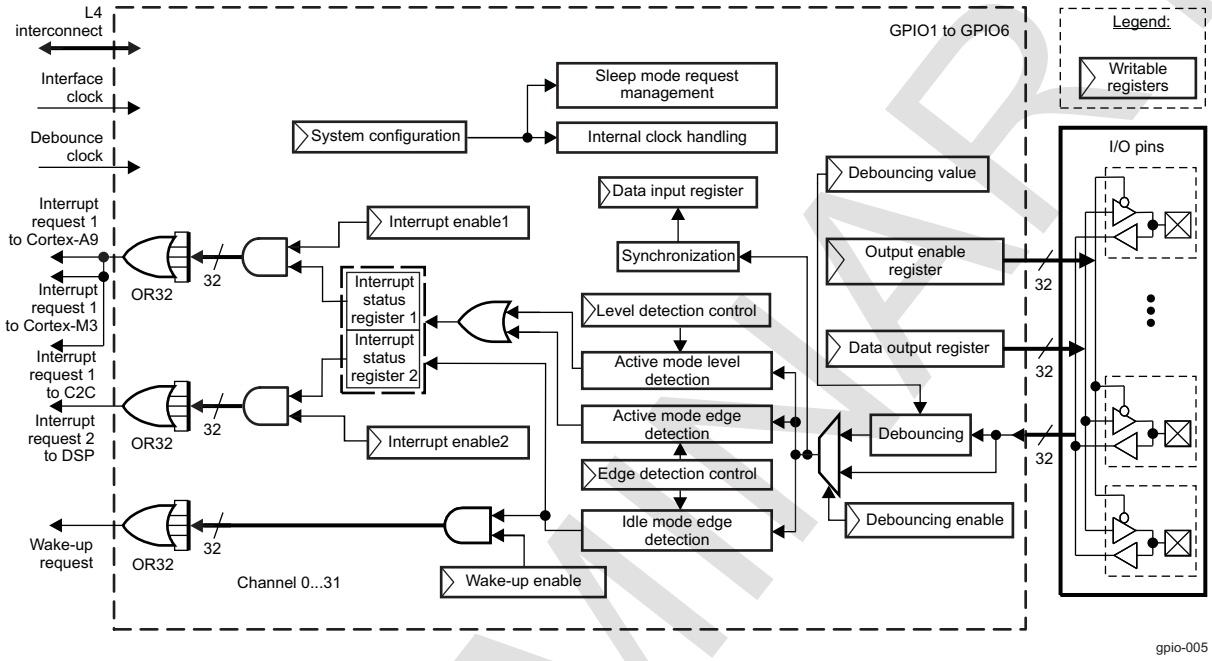
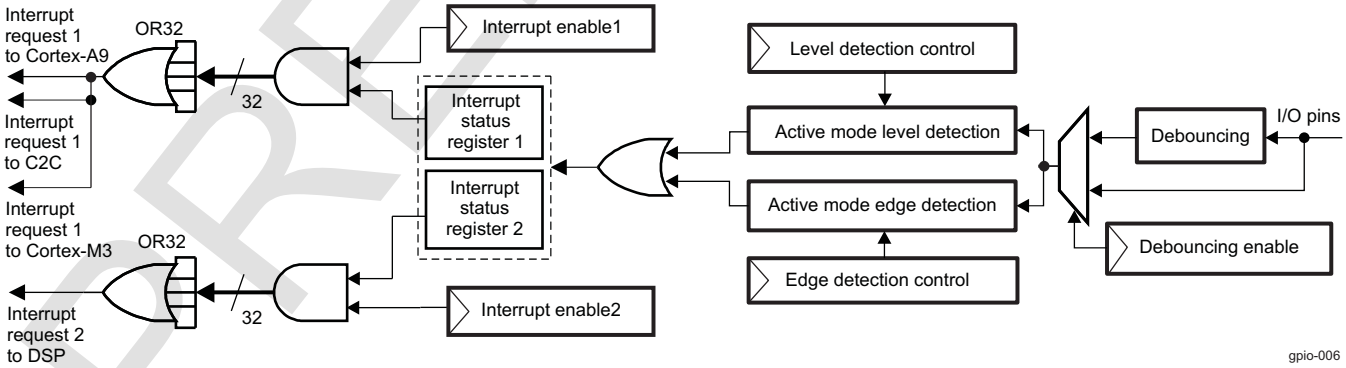


Figure 25-7 shows the details of the GPIOs in the general-purpose interface block diagram, including their configuration registers and main functional paths:

- The synchronous path (for active mode operation) used to generate a synchronous interrupt request on expected event detection on any input GPIO. Synchronous interrupt request lines 1 and 2 are active based on their respective interrupt enable 1 and 2 registers (GPIOi.GPIO_IRQSTATUS_SET_0, GPIOi.GPIO_IRQSTATUS_SET_1, GPIOi.GPIO_IRQSTATUS_CLR_0, and GPIOi.GPIO_IRQSTATUS_CLR_1). See Figure 25-8.

Figure 25-8. Synchronous Path



- The asynchronous path (for idle mode operation) used to generate an asynchronous wake-up request on the expected edge detection on any input GPIO. The asynchronous wake-up request line is active based on the wake-up-enable register. See Figure 25-9.

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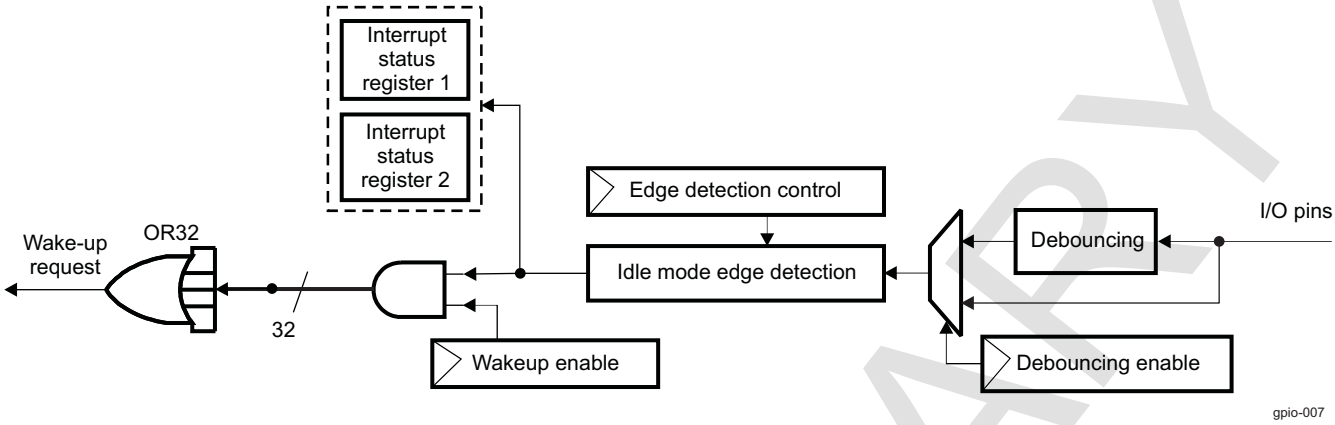
Figure 25-9. Asynchronous Path



- The blocks handling the internal clock (clock gating) and managing the sleep mode request/acknowledge protocol (enabling the synchronous path in active mode and the asynchronous path in idle mode)

25.4.2 General-Purpose Interface Interrupt and Wake-Up Features

25.4.2.1 Synchronous Path: Interrupt Request Generation

The general-purpose interface has 12 interrupt lines (two interrupt lines per each GPIO instance). The 12 interrupt signals are GPIOi_MPU_IRQ (used by the MPU and C2C subsystems) and GPIOi_DSP_IRQ (used by the DSP subsystem), where i = 1, 2, 3, 4, 5, or 6.

Synchronous interrupt requests from each channel are processed by two identical interrupt generation submodules used independently by the DSP subsystem on one side and by the MPU and C2C subsystems on the other side. Each submodule controls its own synchronous interrupt request line and has its own interrupt-enable registers (GPIOi.GPIO_IRQSTATUS_SET_0, GPIOi.GPIO_IRQSTATUS_SET_1, GPIOi.GPIO_IRQSTATUS_CLR_0, or GPIOi.GPIO_IRQSTATUS_CLR_1) and interrupt status registers (GPIOi.GPIO_IRQSTATUS_0 or GPIOi.GPIO_IRQSTATUS_1). The interrupt-enable register selects the channel(s) considered for the interrupt request generation, and the interrupt status register determines which channel(s) activate the interrupt request. Event detection on GPIO channels is reflected in the interrupt status registers independent of the content of the interrupt-enable registers.

In active mode, when the GPIO configuration registers are set to enable the interrupt generation (see Section 25.4.6, *General-Purpose Interface Interrupt and Wake-Up Requests*), a synchronous path samples the transitions and levels on the input GPIO with the internally gated interface clock (see Section 25.4.5.2.4, *Module Power Saving*). When an event matches the programmed settings (see Section 25.4.6, *General-Purpose Interface Interrupt and Wake-Up Requests*), the corresponding bit in the interrupt status register is set to 1 and, on the following interface clock cycle, interrupt lines 1 and/or 2 are activated (depending on the interrupt-enable registers).

Because of the sampling operation, the minimum pulse width on the input GPIO to trigger a synchronous interrupt request is two times the internally gated interface clock period (the internally gated interface clock period equals *N* times the interface clock period (see Section 25.4.5.2.4, *Module Power Saving*). This minimum pulse width must be met before and after any expected level transition detection. Level detection requires the selected level to be stable for at least two times the internally gated interface clock period to trigger a synchronous interrupt.

Because the module is synchronous, latency is minimal between the expected event occurrence and the activation of the interrupt line(s). This latency must not exceed four internally gated interface clock cycles + one interface clock cycle when the debounce feature is not used.

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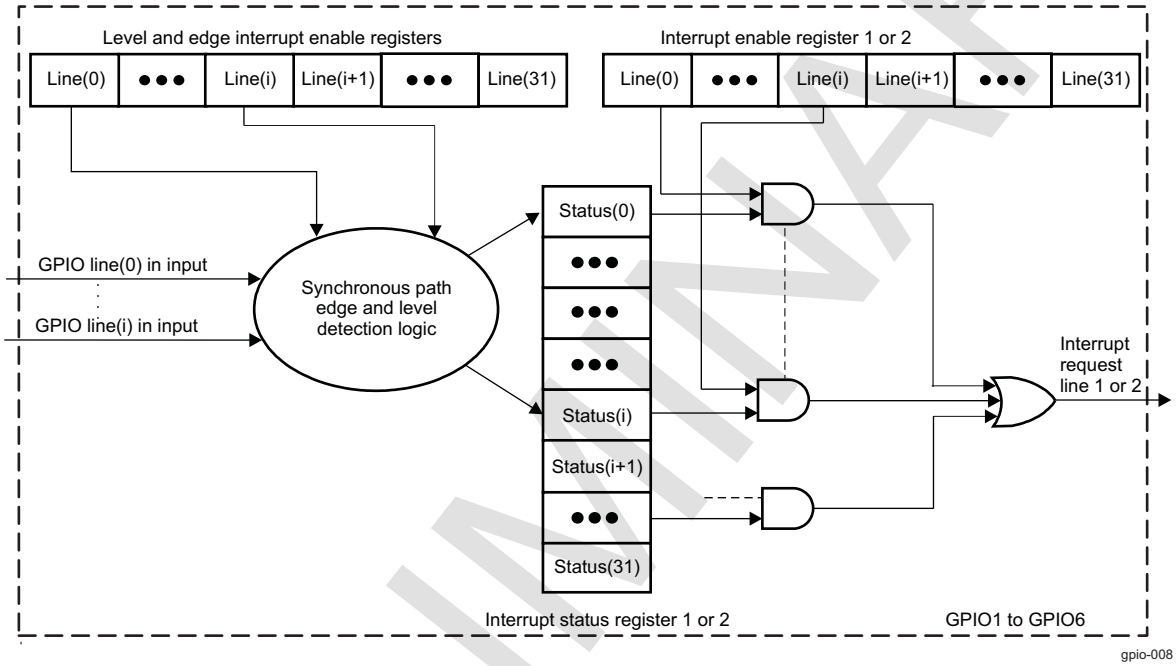
When the debounce feature is active, the latency depends on the value of the debouncing time register (GPIOi.GPIO_DEBOUNCINGTIME) (see Section 25.4.3, *General-Purpose Interface Clock Configuration*) and is less than three internally gated interface clock cycles plus two interface clock cycles plus GPIOi.GPIO_DEBOUNCINGTIME register value debounce clock cycles plus three debounce clock cycles.

Synchronous interrupt request line 1 is mapped on the Cortex-A9 MPU, Cortex-M3 MPU, and C2C subsystems.

Synchronous interrupt request line 2 is mapped on the DSP INTC.

Figure 25-10 is an overview of the interrupt request generation.

Figure 25-10. Interrupt Request Generation



25.4.2.2 Asynchronous Path: Wake-Up Request Generation

The general-purpose interface has six wake-up lines (one wake-up line per GPIO module instance) connected to the PRCM module.

Asynchronous wake-up requests from input channels are merged to issue one wake-up signal to the system per each GPIO module. The wake-up-enable registers (GPIOi.GPIO_IRQWAKEN_0 and GPIOi.GPIO_IRQWAKEN_1) select the channel(s) considered for the wake-up request generation. The asynchronous wake-up request is reflected into the synchronous interrupt status registers (GPIOi.GPIO_IRQSTATUS_0 and GPIOi.GPIO_IRQSTATUS_1).

In idle mode (the interface clock is shut down and the GPIO configuration registers are programmed; see Section 25.4.6, *General-Purpose Interface Interrupt and Wake-Up Requests*), an asynchronous path detects the expected transition(s) on a GPIO input (based on register programming) and activates an asynchronous wake-up request by the sideband signal (GPIOi_SWAKEUP, where i = 1, 2, 3, 4, 5, or 6), if the wake-up-enable register is set.

When the system is awakened, the interface clock is restarted and synchronously set to 1 based on the input GPIO pin triggering the wake-up request and the corresponding bit in the interrupt status registers (GPIOi.GPIO_IRQSTATUS_0 and GPIOi.GPIO_IRQSTATUS_1). On the following internal clock cycle, interrupt lines 1 and/or 2 are active (active low) when the corresponding bits are set in the interrupt-enable registers (GPIOi.GPIO_IRQSTATUS_SET_0, GPIOi.GPIO_IRQSTATUS_SET_1, GPIOi.GPIO_IRQSTATUS_CLR_0 and GPIOi.GPIO_IRQSTATUS_CLR_1).

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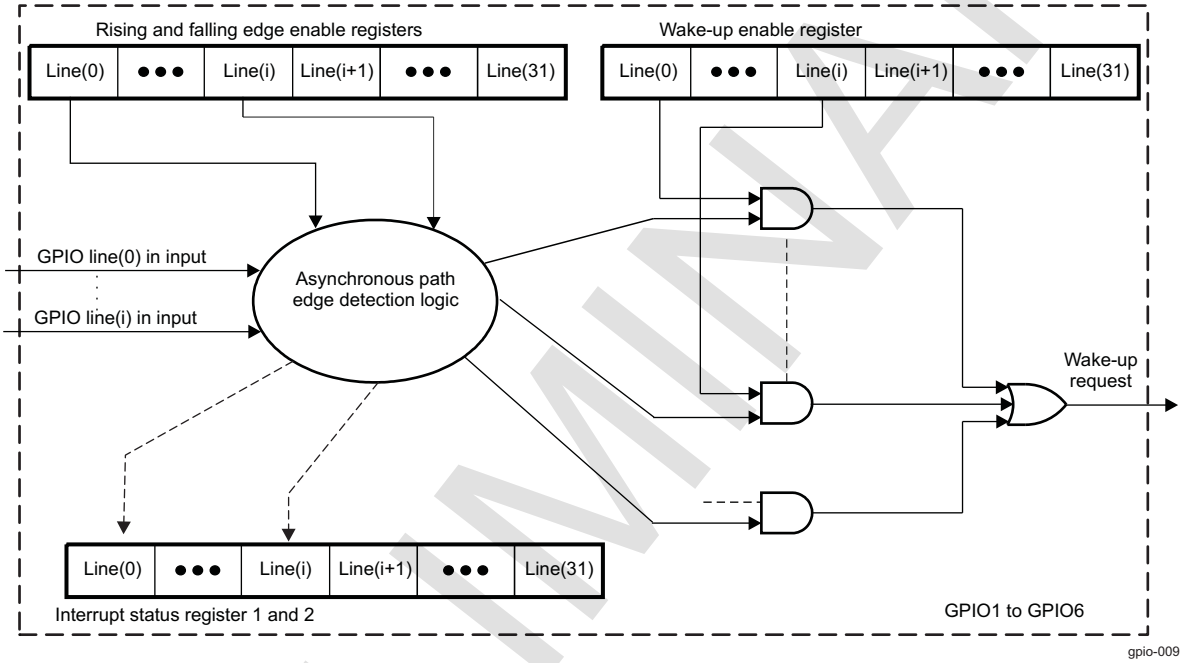
NOTE: When debouncing is not enabled, a minimum input pulse width does not trigger the wake-up request because there is no sampling operation.

When debouncing is enabled, the minimum pulse width is set by the specified debouncing time.

The GPIOi.GPIO_SYSCONFIG[2] ENAWAKEUP bit enables or disables the GPIO wake-up feature globally. If the bit is set to 0, the wake-up-enable registers (GPIOi.GPIO_IRQWAKEN_0 and GPIOi.GPIO_IRQWAKEN_1) have no effect.

Figure 25-11 is an overview of the wake-up request generation.

Figure 25-11. Wake-Up Request Generation



25.4.2.3 Wake-Up Event Conditions During Transition To and From IDLE State

Figure 25-12 shows the wake-up event conditions.

In phase A, only the synchronous path is enabled. A synchronous interrupt request (see Section 25.4.2.1, *Synchronous Path: Interrupt Request Generation*) activates the interrupt line(s) and prevents the GPIO from transitioning into IDLE state until the interrupt is cleared.

In phase B, the asynchronous path and synchronous path are enabled during the first five functional clock cycles of the SLEEPTRANS state. During this period a synchronous interrupt request (see Section 25.4.2.1, *Synchronous Path: Interrupt Request Generation*) prevents the GPIO from transitioning into IDLE state. A shorter pulse puts the module into IDLE state but triggers a wakeup once in IDLE.

In phase C, only the asynchronous path is enabled. A wake-up request (see Section 25.4.2.2, *Asynchronous Path: Wake-Up Request Generation*) triggers a wake-up request from the GPIO and when the module is awakened an interrupt is generated. If debouncing is not enabled, there is no minimum input pulse width to trigger the wake-up request.

In phase D, eight OCP clock cycles occur until the module is in FUNCT state, the synchronous path is enabled, and an event that fulfills the pulse width requirements (see Section 25.4.2.1, *Synchronous Path: Interrupt Request Generation*) activates the interrupt line(s).

In phase E, only the synchronous path is enabled. A synchronous interrupt request (see Section 25.4.2.1, *Synchronous Path: Interrupt Request Generation*) activates the interrupt line(s).

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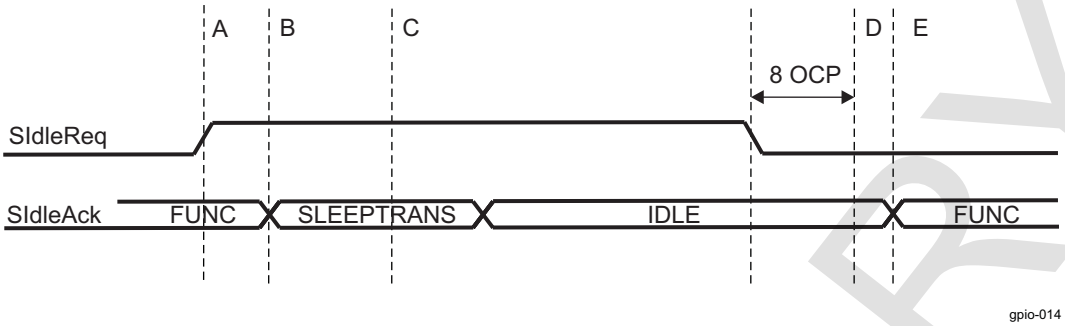
Figure 25-12. Wake-Up Event Conditions



25.4.2.4 Interrupt (or Wake-Up) Line Release

When the host processor (the MPU and/or DSP subsystem in the device) receives an interrupt request issued by the GPIO, it reads the corresponding interrupt status register (GPIOi.GPIO_IRQSTATUS_0 or GPIOi.GPIO_IRQSTATUS_1) to determine which GPIO input triggered the interrupt (or the wake-up request).

After servicing the interrupt (or acknowledging the wake-up request), the processor resets the status bit and releases the interrupt line by setting the corresponding bit of the interrupt status register to 1. If there is still a pending interrupt request to serve (all bits in the interrupt status register that are not masked by the interrupt-enable register are not cleared), the interrupt line is reasserted.

NOTE: The status bit must be reset to re-enter idle mode.

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25.4.3 General-Purpose Interface Clock Configuration

25.4.3.1 Clocking

Each GPIO uses two clocks:

- Debounce clock: The 32-kHz debounce clock, GPIOi_DBCLK (where i = 1, 2, 3, 4, 5, or 6, with one debounce clock per module) comes from the PRCM module and is used for the debounce cell logic (without the corresponding configuration registers). This cell can sample the input line and filters the input level using a programmed delay.

  The debouncing value register (GPIOi.GPIO_DEBOUNCINGTIME) is used to set the debouncing time for all input lines in the GPIO module. The value is global for all the ports of one GPIO, so up to six different debouncing values are possible. The debounce cell is running with the debounce clock (32 kHz). This register represents the number of clock cycle(s) to be used (one cycle is 31 µs long).

  The following formula describes the required input stable time to be propagated to the debounced output:

  Required input line stable = (GPIOi.GPIO_DEBOUNCINGTIME[7:0] DEBOUNCVAL bit field value + 1) × 31,

  where the value of the DEBOUNCVAL bit field is from 0 to 255.

  For more information, see Section 3.6.8, *CD_L4_PER_Clock Domain*, and Section 3.6.4, *CD_WKUP Clock Domain*, in Chapter 3, *Power, Reset, and Clock Management*.
- Interface clock: The interface clock, GPIOi_ICLK (where i = 1, 2, 3, 4, 5, or 6), comes from the PRCM module and is used throughout the GPIO (except within the debounce cell logic). GPIOi_ICLK clocks the data exchanges between the L4 interconnect and the internal logic. The clock-gating features allow module power consumption to be adapted to the activity.

  For more information, see Section 3.6.8, *CD_L4_PER_Clock Domain*, and Section 3.6.4, *CD_WKUP Clock Domain*, in Chapter 3, *Power, Reset, and Clock Management*.

Table 25-3 describes the GPIO clocks.

Table 25-5 summarizes the functional clock configuration.

Table 25-5. Functional Clock Configuration

Interface Clock	GPIO_CTRL[2:1] GATINGRATIO	Functional Clock
GPIOi_ICLK, where i = 1 to 6	00	GPIOi_ICLK /1, where i = 1 to 6
GPIOi_ICLK, where i = 1 to 6	01	GPIOi_ICLK /2, where i = 1 to 6
GPIOi_ICLK, where i = 1 to 6	10	GPIOi_ICLK /4, where i = 1 to 6
GPIOi_ICLK, where i = 1 to 6	11	GPIOi_ICLK /8, where i = 1 to 6

25.4.4 General-Purpose Interface Hardware and Software Reset

The GPIO can be reset by using the domain reset (hardware reset) or by setting a dedicated configuration bit (software reset) in each GPIO.

- Hardware reset: GPIO2 to GPIO6 are attached to the PER_RST reset domain. GPIO1 is attached to the WKUP_RST reset domain.

  The hardware reset has a global reset action on the GPIOs of the general-purpose interface. All configuration registers and internal logic are reset when it is active (low level). In each GPIO, the GPIOi.GPIO_SYSSTATUS[0] RESETDONE bit monitors the internal reset status; it is set when the reset completes. For more information, see Section 3.5.4, *Reset Domains*, in Chapter 3, *Power, Reset, and Clock Management*.
- Software reset: Each GPIO has its own software reset using the GPIOi.GPIO_SYSCONFIG[1] SOFTRESET bit (where i = 1, 2, 3, 4, 5, or 6). The software reset has the same effect as the hardware reset signal, but this reset can be applied on one or more modules.

  Setting the GPIOi.GPIO_SYSCONFIG[1] SOFTRESET bit to 1, (where i = 1, 2, 3, 4, 5, or 6) resets the module. A bit value of 1 remains until the reset completes. When the software reset completes, the GPIOi.GPIO_SYSCONFIG[1] SOFTRESET bit is automatically reset to 0 and has the same effect as a

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hardware reset. The GPIOi.GPIO_SYSSTATUS[0] RESETDONE bit is cleared during a software reset. This bit is set to 1 when the software reset completes.

25.4.5 General-Purpose Interface Power Management

25.4.5.1 Power Domain

GPIO1 is attached to the WKUP power domain (see Section 3.1.1.2, *Power Management*, in Chapter 3, *Power, Reset, and Clock Management*). This domain is composed of the logic permanently supplied to manage domain power state transitions and detect wake-up events. The WKUP power domain is continuously active. GPIO2 to GPIO6 are attached to the PER power domain (see Section 3.1.1.2, *Power Management*, in Chapter 3, *Power, Reset, and Clock Management*). The PER power domain is not active continuously.

25.4.5.2 Power Management

25.4.5.2.1 Idle Scheme

To reduce dynamic consumption, an efficient idle scheme is based on the following:

- An efficient local autoclock gating for each module
- The implementation of control sideband signals between the PRCM module and each module

This enhanced idle control allows clocks to be activated and deactivated safely without requiring complex software management.

The idle mode request, idle acknowledge, and wake-up request (GPIOi_WAKEUP, where i = 1, 2, 3, 4, 5, or 6) are sideband signals between the PRCM module and the general-purpose interface (see Section 25.4.6.2, *Wake-Up Request Generation*).

25.4.5.2.2 Operating Modes

The following four operating modes are defined for the modules:

- Active mode: The module runs synchronously on the interface clock; interrupts can be generated based on the configuration and external signals.
- Idle mode: Power-saving mode with the module in a waiting state. The interface clock can be stopped, an interrupt cannot be generated, and a wake-up signal can be generated based on the configuration and external signals.

  If the debounce clock provided by the PRCM module is active, the debounce cell can sample and filter the input to generate a wake-up event. If the debounce clock is inactive, the debounce cell gates all input signals and thus cannot be used.
- Inactive mode: The module has no activity. The interface clock can be stopped, an interrupt cannot be generated, and the wake-up feature is inhibited.
- Disabled mode: The module is not used. The internal clock paths are gated, and an interrupt or wake-up request cannot be generated.

Idle and inactive modes are configured within the module and activated on request by the PRCM module (see Section 3.1.1.2, *Power Management*, in Chapter 3, *Power, Reset, and Clock Management*) through sideband signals (see Section 25.4.5.2.3, *System Power Management and Wakeup*).

The disabled mode is set by software through a dedicated configuration bit, GPIOi.GPIO_CTRL[0] DISABLEMODULE (0: The module is enabled and clocks are not gated; 1: The module is disabled and clocks are gated). It unconditionally gates the internal clock paths that are not used for the L4 interconnect.

25.4.5.2.3 System Power Management and Wakeup

The PRCM module can require the GPIOs to be idled for power-saving purposes.

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The general-purpose interface has six identical idle mode request/acknowledge (handshake) mechanisms with the PRCM module (see Section 25.4.6.2, *Wake-Up Request Generation*): one per GPIO. The general-purpose interface allows the GPIOs to enter idle mode based on the GPIOi.GPIO_SYSCONFIG[4:3] IDLEMODE bit field.

Idle acknowledge depends on the configuration and activity of each GPIO:

- Smart-idle mode

  When the GPIO is configured in smart-idle mode, it checks for more activity (capture of the input GPIO pins in the GPIOi.GPIO_DATAIN register is complete with no pending interrupt; all interrupt status bits are cleared), and there is no access to the GPIO.GPIO_DEBOUNCINGTIME register, which is waiting to be synchronized.

  Idle acknowledge is then asserted and the module enters into idle-mode. It waits for active system clock gating by the PRCM module (when all peripherals supplied by the same L4 interface clock domain are also ready for idle).

  In idle mode (that is, when the PRCM module gates the interface clock), no interrupt occurs and the module is ready to issue a wake-up request.

  When the expected transition occurs on an enabled GPIO input pin, the GPIO exits from idle mode if the GPIOi.GPIO_SYSCONFIG[2] ENAWAKEUP bit is set to 1 (wake-up capability enabled).

- Smart-idle wake-up mode

  If the GPIOi.GPIO_SYSCONFIG[4:3] IDLEMODE bit field selects smart-idle or smart-idle wake-up mode, the GPIO module evaluates its internal capability to switch off the interface clock. Once all internal activity ceases (the DATA INPUT REGISTER completed to capture the input GPIO pins, there is no pending interrupt, all interrupt status bits are cleared, and there is no write access to the GPIO_DEBOUNCINGTIME register pending to be synchronized), the Idle acknowledge is asserted and the GPIO enters into idle mode, ready to issue a wake-up request when the expected transition occurs on an enabled GPIO input pin. This wake-up request is effectively sent only if the GPIOi.GPIO_SYSCONFIG[2] ENAWAKEUP bit of the system configuration register enables the GPIO wake-up capability (see Section 25.6.2.2, *System Configuration Register*). When the system is awake, the idle request goes inactive, the idle acknowledge and wake-up request (if the GPIO triggered the systems wakeup) signals are immediately deasserted, and the asynchronous wake-up request (if existing) is reflected into the synchronous interrupt status registers.

- Force-idle mode

  When the GPIO is configured in force-idle mode (the GPIOi.GPIO_SYSCONFIG[4:3] IDLEMODE bit field = 2b00) and receives an idle request from the PRCM module, the GPIO waits unconditionally for active system clock gating by the PRCM module. (This occurs only when all peripherals supplied by the same L4 interface clock domain are also ready for idle.)

  When in idle mode (that is, when the PRCM module gates the interface clock), the module (in inactive mode) has no activity, the interface clock paths are gated, an interrupt cannot be generated, and the wake-up feature is totally inhibited.

- No-idle mode

  When the GPIO is configured in no-idle mode (the GPIOi.GPIO_SYSCONFIG[4:3] IDLEMODE bit field = 2b01) and receives an idle request from the PRCM module, the GPIO does not go into idle mode and the idle acknowledge is never sent.

NOTE: For more information about idle modes, see Section 3.1.1.2, *Power Management*, in Chapter 3, *Power, Reset, and Clock Management*.

25.4.5.2.4 Module Power Saving

The GPIO has local power management by internal clock-gating features:

- Internal interface clock gating: The clock for the L4 interconnect logic can be gated when the GPIO is not accessed, if the GPIOi.GPIO_SYSCONFIG[0] AUTOIDLE bit is set. Otherwise, this logic is free-running on the interface clock.
- Clock gating for the input data sample logic: Clock for the input data sample logic can be gated when the data in the GPIOi.GPIO_DATAIN register is not accessed.

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- Clock gating for the event detection logic: Each GPIO implements four clock groups used for the logic in the synchronous event detection. Each group of eight input GPIO pins has a separate enable signal depending on the setting of the edge/level detection register (because the input is 32 bits, four groups of eight inputs are defined for each GPIO). If a group requires no detection, the corresponding clock is gated.

  Grouping the edge/level enable can save the power consumption of the module.

  If any of the following registers is set to 0x01 01 01 01, then all clocks are active (power consumption is high). If they are set to 0x00 00 00 FF, then a single clock is active (power saving).

  – GPIOi.GPIO_LEVELDETECT0
  – GPIOi.GPIO_LEVELDETECT1
  – GPIOi.GPIO_RISINGDETECT
  – GPIOi.GPIO_FALLINGDETECT

  NOTE: When the clocks are enabled by writing to the following registers, the detection starts after five clock cycles. This period is required to clean the synchronization edge/level detection pipeline.

  - GPIOi.GPIO_LEVELDETECT0
  - GPIOi.GPIO_LEVELDETECT1
  - GPIOi.GPIO_RISINGDETECT
  - GPIOi.GPIO_FALLINGDETECT

  The mechanism is independent of each clock group. If the clock has been started before and a new setting is performed, the following is recommended:

  1. Set the new detection required.
  2. Disable the previous setting (if necessary).

  In this way, the corresponding clock is not gated and the detection starts immediately.

  All channels are also gated using a one-out-of-N scheme. N is the GPIOi.GPIO_CTRL[2:1] GATINGRATIO bit field and can take the values 1 (2b00), 2 (2b01), 4 (2b10), or 8 (2b11). The interface clock is enabled for this logic one cycle every N cycles. When N is equal to 1, there is no gating and this logic is free-running on the interface clock. When N is 2, 4, or 8, this logic is running at the equivalent frequency of interface clock frequency divided by N.

  – Inactive mode: In inactive mode, all internal clock paths are gated.
  – Disabled mode: All internal clock paths not used for the L4 interconnect are gated. The GPIOi.GPIO_CTRL[0] DISABLEMODULE bit controls a clock-gating feature at the module level. When set to 1, this bit forces clock gating for all internal clock paths. Internal activity in the module is suspended. The L4 interconnect is not affected by this bit.

The interface clock gating is controlled through the GPIOi.GPIO_SYSCONFIG[0] AUTOIDLE bit, which is used to save power when the module is not used because of the multiplexing configuration selected at the device level. This bit takes precedence over all other internal configuration bits.

Table 25-6 describes the power-management features available for the general-purpose interface module.

NOTE: For information about source clock gating and a description of sleep/wake-up transitions, see Section 3.1.1.1.2, *Module-Level Clock Management*, in Chapter 3, *Power, Reset, and Clock Management*.

For descriptions of the EnaWakeUp, IdleMode, ClockActivity, and StandbyMode features, see Section 3.1.1.1.2, *Module-Level Clock Management*, in Chapter 3, *Power, Reset, and Clock Management*.

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Table 25-6. Local Power-Management Features

Feature	Registers	Description
Clock autogating	GPIOi.GPIO_SYSCONFIG[0] AUTOIDLE bit	Sets the clock gating strategy for the OCP interface block.
Slave idle modes	GPIOi.GPIO_SYSCONFIG[4:3] IDLEMODE bit field	Force-idle, no-idle, and smart-idle wake-up-capable modes are available.
Clock activity	GPIOi.GPIO_CTRL[0] DISABLEMODULE bit field	Enable and disable the module.
Debouncing enable	GPIOi.GPIO_DEBOUNCENABLE[31:0] DEBOUNCEENABLE bit field	Debouncing mode is available.
Global wake-up enable	GPIOi.GPIO_SYSCONFIG[2] ENAWAKEUP bit	This bit enables the wake-up feature at module level.
Wake-up sources enable	GPIOi.GPIO_IRQWAKEN_0[31:0] INTLINE bit field GPIOi.GPIO_IRQWAKEN_1[31:0] INTLINE bit field	This register enables or disables a specific IRQ request source to generate a wake-up signal.

Table 25-7 describes the clock activity settings.

Table 25-7. Clock Activity Settings

GPIOi.GPIO_SYSCONFIG[4:3] IDLEMODE	Selected Mode	Description	Wake-Up Events
00	Force-idle	The GPIO goes into inactive mode independently of the internal module state, and the Idle acknowledge is never sent.	No
01	No-idle	The GPIO does not go into the idle mode and the idle acknowledge is never sent.	No
10	Smart-idle	The GPIO evaluates its internal capability to switch off the interface clock. If there is no more internal activity, the idle acknowledge is asserted and the GPIO enters into idle mode.	No
11	Smart-idle wake-up	The GPIO evaluates its internal capability to have the interface clock switched off. If there is no more internal activity, the idle acknowledge is asserted and the GPIO enters into idle mode.	Yes

25.4.6 General-Purpose Interface Interrupt and Wake-Up Requests

25.4.6.1 Interrupt Request Generation

All interrupt sources (the 32 GPIO input channels) are merged to issue two synchronous interrupt requests in each GPIO module. Thus, the general-purpose interface has 12 interrupt lines (two interrupt lines per each GPIO instance).

- Synchronous interrupt request line 1 is mapped on the Cortex-A9 and Cortex-M3 MPU INTCs, and on the C2C subsystem.
- Synchronous interrupt request line 2 is mapped on the DSP INTC.

Table 25-8 lists the event flags, and their mask, that can cause module interrupts.

Table 25-8. Events

Event Flag	Event Mask	Synchronous	Sensitivity	Map to	Description
GPIOi.GPIO_IRQSTATUS_0[31:0] INTLINE	GPIOi.GPIO_IRQSTATUS_SET_0[31:0] INTLINE	Yes	Edge/level	MA_IRQ_n MM_IRQ_n(1) C2C_SSCM_GPI_n(2)	Corresponds to the first line of interrupt
GPIOi.GPIO_IRQSTATUS_1[31:0] INTLINE	GPIOi.GPIO_IRQSTATUS_SET_1[31:0] INTLINE	Yes	Edge/level	D_IRQ_n	Corresponds to the second line of interrupt

(1) For GPIO1 and GPIO2 only
(2) For GPIO1 to GPIO4 only

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Table 25-8. Events (continued)

Event Flag	Event Mask	Synchronous	Sensitivity	Map to	Description
GPIOi.GPIO_IRQSTATUS_0 [31:0] INTLINE	GPIOi.GPIO_IRQSTATUS_CLR_0[31:0] INTLINE	Yes	Edge/level	MA_IRQ_n MM_IRQ_n(1) C2C_SSCM_GPI_n(2)	Corresponds to the first line of interrupt
GPIOi.GPIO_IRQSTATUS_1[31:0] INTLINE	GPIOi.GPIO_IRQSTATUS_CLR_1[31:0] INTLINE	Yes	Edge/level	D_IRQ_n	Corresponds to the second line of interrupt
GPIOi.GPIO_IRQSTATUS_0[31:0] INTLINE	GPIOi.GPIO_IRQWAKEN_0[31:0] INTLINE	No	Edge/level	MA_IRQ_n MM_IRQ_n(1) C2C_SSCM_GPI_n(2)	Corresponds to the first line of interrupt
GPIOi.GPIO_IRQSTATUS_1[31:0] INTLINE	GPIOi.GPIO_IRQWAKEN_1[31:0] INTLINE	No	Edge/level	D_IRQ_n	Corresponds to the second line of interrupt

Synchronous interrupt request lines 1 and 2 are active depending on their respective interrupt enable 1 and 2 registers (GPIOi.GPIO_IRQSTATUS_SET_0, GPIOi.GPIO_IRQSTATUS_SET_1, GPIOi.GPIO_IRQSTATUS_CLR_0 and GPIOi.GPIO_IRQSTATUS_CLR_1).

- Interrupt-enable registers (GPIOi.GPIO_IRQSTATUS_SET_0 and GPIOi.GPIO_IRQSTATUS_SET_1)

  The interrupt-enable1 (or interrupt-enable2) register allows masking of the expected transition on input GPIO to prevent the generation of an interrupt request on line1 (or line2). The interrupt-enable registers are programmed synchronously with the interface clock.

  These registers can be accessed with direct read/write operations or using the alternate set-and-clear protocol feature for register update. This feature allows the setting or clearing of explicit bits of these registers with a single write access (see Section 25.4.9, *General-Purpose Interface Set-and-Clear Protocol*).

- Interrupt status registers (GPIOi.GPIO_IRQSTATUS_0 and GPIOi.GPIO_IRQSTATUS_1)

  The interrupt status1 (or interrupt status2) register determines which of the input GPIO pins triggered the interrupt line1 (or interrupt line2) request (or the wake-up line).

  When a bit in this register is set to 1, it indicates that the corresponding GPIO pin is requesting the interrupt (or the wakeup). To reset a bit in this register, write 1 to the appropriate bit. However, an interrupt cannot be generated by writing 1 to the interrupt status1 (or interrupt status2) register.

  If 0 is written to a bit in this register, the value remains unchanged. The interrupt status1 (or interrupt status2) register is synchronous with the interface clock. In idle mode, the event is detected through an asynchronous path, and the corresponding bit in the interrupt status1 and interrupt status2 registers are set when the GPIO is awakened.

CAUTION

After servicing the interrupt, the status bit in the interrupt status register (GPIOi.GPIO_IRQSTATUS_0 or GPIOi.GPIO_IRQSTATUS_1) must be reset and the interrupt line released (by setting the corresponding bit of the interrupt status register to 1) before enabling an interrupt for the GPIO channel in the interrupt-enable register (GPIOi.GPIO_IRQSTATUS_SET_0 or GPIOi.GPIO_IRQSTATUS_SET_1) to prevent the occurrence of unexpected interrupts when enabling an interrupt for the GPIO channel.

25.4.6.2 Wake-Up Request Generation

GPIO1 of the general-purpose interface is attached to the WKUP power domain (see , *Power Management*, in Chapter 3, *Power, Reset, and Clock Management*) and can wake up the system.

NOTE: GPIO2 to GPIO6 belong to the PER power domain and thus their wake-up capabilities are operational only when the PER power domain is active.

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All wake-up sources (the 32 input GPIO channels) are merged together to issue a single asynchronous wake-up request in each GPIO following the expected transition(s) (based on register programming). Each GPIO generates a wake-up signal to the PRCM module.

NOTE: Only gpio_wk[10:0] and gpio_wk[31:29] can be used to generate a direct wake-up event.

The asynchronous wake-up request line is active based on the GPIOi.GPIO_IRQWAKEN_0 and GPIO_IRQWAKEN_1 wake-up-enable registers (where i = 1, 2, 3, 4, 5, or 6).

The wake-up-enable register allows masking of the expected transition on input GPIO to prevent the generation of a wake-up request. The wake-up-enable register is programmed synchronously with the interface clock before any idle mode request coming from the host processor.

This register can be accessed with direct read/write operations or by using the alternate set-and-clear protocol register update feature. This feature allows setting or clearing specific bits of this register with a single write access to the set wake-up-enable register (or to the clear wake-up-enable register) address (see Section 25.4.9, *General-Purpose Interface Set-and-Clear Protocol*).

NOTE: There must be a correlation between the wake-up enable and interrupt-enable registers. If a GPIO pin has a wake-up configured on it, it must also have the corresponding interrupt enabled (on one of the two interrupt lines). Otherwise, it is possible to have a wake-up event, but after exiting the IDLE state, no interrupt is generated; thus, the corresponding bit from the interrupt status register is not cleared, and the module does not acknowledge a future idle request.

Table 25-9 lists the mapping of the wake-up signals.

Table 25-9. Wake-Up Signals

Name	Mapping	Comments
GPIOi_WAKE	GPIOi_SWAKEUP	Where i = 1, 2, 3, 4, 5, and 6. Destination is the PRCM module.

25.4.7 General-Purpose Interface Channel Description

Table 25-10 describes the GPIO channels.

Table 25-10. GPIO Channel Description

Channel Number	Type [1]	Mapping	Wake-Up Feature	Comments
GPIO1				
[31]	I/O	gpio_wk31	Yes	Wake-up path
[30]	I/O	gpio_wk30	Yes	Wake-up path
[29]	I/O	gpio_wk29	Yes	Wake-up path
[28:11]	I/O	gpio_[28:11]	Yes	GPIO
[10:6]	I/O	gpio_wk[10:6]	Yes	Wake-up path
[5]	I	gpi_wk5	Yes	Wake-up path
[4]	I/O	gpio_wk4	Yes	Wake-up path
[3:2]	I/O	gpio_[3:2]	Yes	GPIO
	I/O	gpio_wk[3:2]	Yes	Wake-up path
[1:0]	I/O	gpio_[1:0]	Yes	GPIO
	I/O	gpio_wk[1:0]	Yes	Wake-up path
GPIO2				
[31:27]	I/O	gpio_[63:59]	Yes [2]	GPIO

(1) I = Input; O = Output

(2) Only when the PER power domain is active

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Table 25-10. GPIO Channel Description (continued)

Channel Number	Type [1]	Mapping	Wake-Up Feature	Comments
[26][3]	I	TV_SHORT	Yes [2]	Internal TV short signal from video DAC1
[25][3]	I	TV_DETECT	Yes [2]	Internal TV detection signal from video DAC1
[24:0]	I/O	gpio_[56:32]	Yes [2]	GPIO
GPIO3				
[31:17]	I/O	gpio_[95:81]	Yes [2]	GPIO
[22][4]	I/O	gpio_86	Yes [2]	GPIO
	I	TSHUT	Yes [2]	Bandgap internal TSHUT
[21:17]	I/O	gpio_[85:81]	Yes [2]	GPIO
[16:3]	I	gpi_[80:67]	Yes [2]	GPIO inputs only
[2:0]	I/O	gpio_[66:64]	Yes [2]	GPIO
GPIO4				
[31:0]	I/O	gpio_[127:96]	Yes [2]	GPIO
GPIO5				
[31:0]	I/O	gpio_[159:128]	Yes [5]	GPIO
GPIO6				
[31:21]	I/O	gpio_[191:181]	Yes [5]	GPIO
[20][6]	I	DPDM5VSHORT	Yes [5]	USB OTG PHY short detect (DPDM5VSHORT)
[19][6]	I	CHGDETECT	Yes [5]	USB OTG PHY charge detect (CHGDETECT)
[18:15]	I/O	gpio_[178:175]	Yes [5]	GPIO
[14:0]	I/O	gpio_[174:160]	Yes [5]	GPIO

(3) The GPIO channel is not available on device pads. Reserved for internal use only (see the Comments column).

(4) The GPIO channel provides additional internal functionality (see the Comments column), besides its GPIO capabilities, when it is not connected to a pad of the device. That is, the corresponding pad is configured in a mode different from multiplexing mode 3. For more information about pad configuration and multiplexing, see Section 18.4.8, *Pad Functional Multiplexing and Configuration*, in Chapter 18, *Control Module*.

(5) Only when the PER power domain is active

(6) The GPIO channel is not available on device pads. Reserved for internal use only (see the Comments column).

NOTE: The thermal shutdown comparator output signal (TSHUT) is an output from the BANDGAP module. This signal is low during normal operation and goes high during a thermal shutdown event. When channel 22 of the GPIO3 is not connected to a ball of the device (the corresponding pin is configured in a mode different from configuration mode 4; see Section 18.4.8, *Pad Functional Multiplexing and Configuration*, in Chapter 18, *Control Module*, for more information about pin configuration), TSHUT is connected to channel 22 of GPIO3. An interrupt can be generated when a low-to-high transition occurs on TSHUT whether or not the interrupt generation for channel 22 of GPIO3 is correctly configured.

NOTE: Channels 20 and 19 of GPIO6 are internally connected inside the device to the short detection (DPDM5VSHORT) and charger detection (CHGDETECT) outputs, respectively, of the USB OTG PHY module. This allows interrupt generation on the corresponding GPIO channel, if either of the mentioned events occurs.

25.4.8 General-Purpose Interface Data Input/Output Capabilities

The output-enable register (GPIOi.GPIO_OE) controls the output/input capability of each pin. At reset, all the GPIO-related pins are configured as inputs, and their output capabilities are disabled. This register is not used within the module. Its only function is to carry the pad configuration.

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When configured as an output (the desired bit reset in the GPIOi.GPIO_OE register), the value of the corresponding bit in the GPIOi.GPIO_DATAOUT register is driven on the corresponding GPIO pin. Data is written to the data-output register synchronously with the interface clock. This register can be accessed with read/write operations or by using the alternate set-and-clear protocol register update feature. This feature gives the possibility to set or clear specific bits of this register with a single write access to the set-output data register (GPIOi.GPIO_SETDATAOUT) or to the clear-output data register (GPIOi.GPIO_CLEARDATAOUT) address (see Section 25.4.9, *General-Purpose Interface Set-and-Clear Protocol*). If the application uses a pin as an output and does not want interrupt/wake-up generation from this pin, the application must properly configure the wake-up-enable (GPIOi.GPIO_IRQWAKEN_0 and GPIOi.GPIO_IRQWAKEN_1) and the interrupt-enable (GPIOi.GPIO_IRQSTATUS_SET_0 and GPIOi.GPIO_IRQSTATUS_SET_1) registers.

When configured as an input (the desired bit is set to 1 in the GPIOi.GPIO_OE register), the state of the input can be read from the corresponding bit in the GPIOi.GPIO_DATAIN register. The input data is sampled synchronously with the interface clock and then captured in the data input register synchronously with the interface clock. When the GPIO pin levels change, they are captured into this register after two interface clock cycles (the required cycles to synchronize and to write data). If the application uses a pin as an input, the application must properly configure the wake-up enable (GPIOi.GPIO_IRQWAKEN_0 and GPIOi.GPIO_IRQWAKEN_1) and the interrupt-enable (GPIOi.GPIO_IRQSTATUS_SET_0 and GPIOi.GPIO_IRQSTATUS_SET_0) registers to the interrupt and wake-up feature as needed. For using the alternate set-and-clear protocol, see Section 25.4.9, *General-Purpose Interface Set-and-Clear Protocol.*

25.4.9 General-Purpose Interface Set-and-Clear Protocol

25.4.9.1 Description

The GPIO module implements the set-and-clear protocol register update for the following registers:

- GPIOi.GPIO_DATAOUT
- GPIOi.GPIO_IRQSTATUS_CLR_0
- GPIOi.GPIO_IRQSTATUS_CLR_1
- GPIOi.GPIO_IRQSTATUS_SET_0
- GPIOi.GPIO_IRQSTATUS_SET_1
- GPIOi.GPIO_IRQWAKEN_0
- GPIOi.GPIO_IRQWAKEN_1

This protocol is an alternative to the atomic test and set operations and consists of writing operations at dedicated addresses (one address for setting bit[s] and one address for clearing bit[s]). The data to write is 1 at bit position(s) to clear (or to set) and 0 at unaffected bit(s). Registers can be accessed in two ways:

- Standard: Full register read and write operations at the primary register address
- Set and clear: Separate addresses are provided to set (and clear) bits in registers. Writing 1 at these addresses sets (or clears) the corresponding bit into the equivalent register; writing 0 has no effect.

Therefore, for these registers, three addresses are defined for one unique physical register. Reading these addresses has the same effect and returns the register value.

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25.4.9.2 Clear Instruction

25.4.9.2.1 Clear Register Addresses

- Clear interrupt-enable registers (GPIOi.GPIO_IRQSTATUS_CLR_0 and GPIOi.GPIO_IRQSTATUS_CLR_1).

  A write operation in the GPIO_IRQSTATUS_CLR_0 (or GPIO_IRQSTATUS_CLR_1) register clears the corresponding bit in the same register when the written bit is 1; a written bit at 0 has no effect.

  A read of the clear interrupt-enable0 (or enable1) register returns the value of the GPIO_IRQSTATUS_CLR_0 (or GPIO_IRQSTATUS_CLR_1) register.
- Clear wake-up-enable registers (GPIOi.GPIO_IRQWAKEN_0 and GPIOi.GPIO_IRQWAKEN_1).

  A write operation in the clear wake-up-enable register clears the corresponding bit in the wake-up-enable register when the written bit is 1; a written bit at 0 has no effect.

  A read of the clear wake-up-enable register returns the value of the wake-up-enable register.
- Clear data-output register (GPIOi.GPIO_CLEARDATAOUT).

  A write operation in the clear data-output register clears the corresponding bit in the data-output register when the written bit is 1; a written bit at 0 has no effect.

  A read of the clear data-output register returns the value of the data-output register.

25.4.9.2.2 Clear Instruction Example

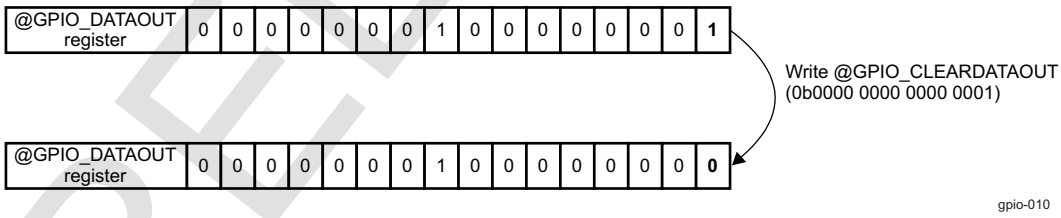
Assume the data-output register (or one of the interrupt/wake-up-enable register) contains the binary value, 0b0000 0001 0000 0001, and bit 0 is to be clear.

With the clear instruction feature, write 0b0000 0000 0000 0001 at the address of the clear data-output register (or at the address of the clear interrupt/wake-up-enable register). After this write operation, a reading of the data-output register (or the interrupt/wake-up-enable register) returns 0b0000 0001 0000 0000; bit 0 is cleared.

NOTE: Although the general-purpose interface registers are 32 bits wide, only the least-significant 16 bits are represented in this example.

Figure 25-13 shows an example of a clear instruction.

Figure 25-13. GPIO_CLEARDATAOUT Register Example



25.4.9.3 Set Instruction

25.4.9.3.1 Set Register Addresses

- Set interrupt-enable registers (GPIOi.GPIO_IRQSTATUS_SET_0 and GPIOi.GPIO_IRQSTATUS_SET_1).

  A write operation in the GPIOi.GPIO_IRQSTATUS_SET_0 (or GPIOi.GPIO_IRQSTATUS_SET_1) register sets the corresponding bit in the same register when the written bit is 1; a written bit at 0 has no effect.

  A read of the set interrupt-enable0 (or enable1) register returns the value of the interrupt GPIOi.GPIO_IRQSTATUS_SET_0 (or GPIOi.GPIO_IRQSTATUS_SET_1) register.
- Set wake-up-enable registers (GPIOi.GPIO_IRQWAKEN_0 and GPIOi.GPIO_IRQWAKEN_1).

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A write operation in the set wake-up-enable register sets the corresponding bit in the wake-up-enable register when the written bit is 1; a written bit at 0 has no effect.

A read of the set wake-up-enable register returns the value of the wake-up-enable register.

- Set data-output register (GPIOi.GPIO_SETDATAOUT).

  A write operation in the set data-output register sets the corresponding bit in the data-output register when the written bit is 1; a written bit at 0 has no effect.

  A read of the set data-output register returns the value of the data-output register.

25.4.9.3.2 Set Instruction Example

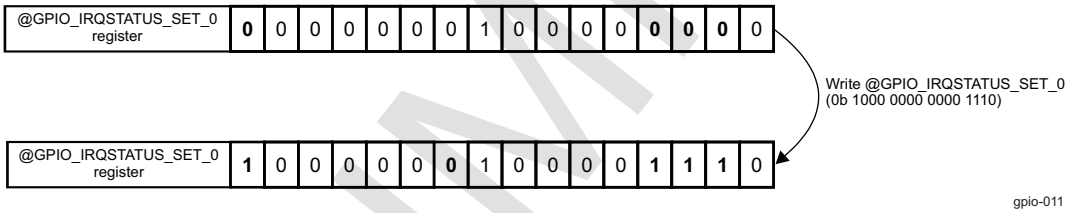
Assume the interrupt-enable1 (or enable2) register (or the data-output register) contains the binary value, 0b0000 0001 0000 0000, and bits 15, 3, 2, and 1 are to be set.

With the set instruction feature, write 0b1000 0000 0000 1110 at the address of the set interrupt enable1 (or enable2) register (or at the address of the set data-output register). After this write operation, a reading of the interrupt-enable1 (or enable2) register (or the data-output register) returns 0b1000 0001 0000 1110; bits 15, 3, 2, and 1 are set.

NOTE: Although the general-purpose interface registers are 32 bits wide, only the least-significant 16 bits are represented in this example.

Figure 25-14 shows an example of a set instruction.

Figure 25-14. Write in GPIO_IRQSTATUS_SET_0 Register Example



The set wake-up-enable register offers the same feature with the wake-up-enable register.

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25.5 General-Purpose Interface Programming Guide

25.5.1 General-Purpose Interface Low-Level Programming Models

25.5.1.1 Global Initialization

25.5.1.1.1 Surrounding Modules Global Initialization

This section identifies the requirements for initializing the surrounding modules when the general-purpose interface module is to be used for the first time after a device reset. This initialization of surrounding modules is based on the integration and environment of the general-purpose interface. For more information, see Section 25.3, *General-Purpose Interface Integration*, and *Section 25.2, General-Purpose Interface Environment*.

Table 25-11. Global Initialization of Surrounding Modules

Surrounding Modules	Comments
PRCM	Module interface and functional clocks must be enabled. For more information about the module configuration, see Chapter 3, *Power, Reset, and Clock Management*.
Control module	Module-specific pad muxing must be set in the control module. For more information about the module configuration, see Chapter 18, *Control Module*.
MPU INTC	MPU INTC configuration must be done to enable the interrupts from the general-purpose interface module. See Chapter 17, *Interrupt Controllers*.
DSP INTC	DSP INTC configuration must be done to enable the interrupts from the general-purpose interface module. See Chapter 17, *Interrupt Controllers*.

25.5.1.1.2 General-Purpose Interface Module Global Initialization

This procedure initializes the general-purpose interface module after a POR or software reset.

Table 25-12. General-Purpose Interface Global Initialization

Step	Register/Bit Field/Programming Model	Value
Execute software reset.	GPIO_SYSCONFIG[1] SOFTRESET	0x1
Wait until reset completed?	GPIO_SYSSTATUS[0] RESETDONE	= 0x1
Configure idle mode.	GPIO_SYSCONFIG[4:3] IDLEMODE	0x–
Configure interface clock gating.	GPIO_SYSCONFIG[0] AUTOIDLE	0x–
Set clock gating power saving.	GPIO_LEVELDETECT0[31:0] LEVELDETECT0 and GPIO_LEVELDETECT1[31:0] LEVELDETECT1 and GPIO_RISINGDETECT[31:0] RISINGDETECT and GPIO_FALLINGDETECT[31:0] FALLINGDETECT	0x0000 00FF
Set clock gating ratio.	GPIO_CTRL[2:1] GATINGRATIO	0x–
Configure GPIO channels as input or output.	GPIO_OE[31:0] OUTPUTEN	0x–
Set debounce time value.	GPIO_DEBOUNCINGTIME[7:0] DEBOUNCETIME	0x–
Enable/disable debouncing for desired input line.	GPIO_DEBOUNCENABLE[7:0] DEBOUNCEENABLE	0x–
Interrupt and Wake-Up Request Configuration		
Enable/disable interrupts.	GPIO_IRQSTATUS_SET_0[31:0] INTLINE and/or GPIO_IRQSTATUS_SET_1[31:0] INTLINE	0x–
Enable/disable wakeup for GPIO channels.	GPIO_IRQWAKEN_0[31:0] INTLINE and/or GPIO_IRQWAKEN_1[31:0] INTLINE	0x–
Enable/disable wake-up generation.	GPIO_SYSCONFIG[2] ENAWAKEUP	0x1

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25.5.1.2 General-Purpose Interface Operational Modes Configuration

25.5.1.2.1 General-Purpose Interface Read Input Register

Table 25-13. General-Purpose Interface Read Input Register

Step	Register/Bit Field/Programming Model	Value
Read input register value.	GPIO_DATAIN[31:0] DATAIN	0x–

25.5.1.2.2 General-Purpose Interface Write Output Register

Table 25-14. General-Purpose Interface Write Output Register

Step	Register/Bit Field/Programming Model	Value
Write value to output register.	GPIO_DATAOUT[31:0] DATAOUT	0x–

25.5.1.2.3 General-Purpose Interface Set Bit Function

Table 25-15. General-Purpose Interface Set Bit Function

Step	Register/Bit Field/Programming Model	Value
Write to set desired bit(s) in register.	GPIO_SETDATAOUT[31:0] INTLINE	0x1
	GPIO_IRQSTATUS_SET_0[31:0] INTLINE	
	GPIO_IRQSTATUS_SET_1[31:0] INTLINE	
	GPIO_IRQWAKEN_0[31:0] INTLINE	
	GPIO_IRQWAKEN_1[31:0] INTLINE	

25.5.1.2.4 General-Purpose Interface Clear Bit Function

Table 25-16. General-Purpose Interface Clear Bit Function

Step	Register/Bit Field /Programming Model	Value
Write to clear desired bit(s) in register.	GPIO_CLEARDATAOUT[31:0] INTLINE	0x1
	GPIO_IRQSTATUS_CLR_0[31:0] INTLINE	
	GPIO_IRQSTATUS_CLR_1[31:0] INTLINE	
	GPIO_IRQWAKEN_0[31:0] INTLINE	
	GPIO_IRQWAKEN_1[31:0] INTLINE	

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25.6 General-Purpose Interface Register Manual

25.6.1 General-Purpose Interface Instance Summary

Table 25-17 summarizes the general-purpose interface instance.

Table 25-17. Instance Summary

Module Name	Base Address	Size
GPIO1	0x4A31 0000	4KB
GPIO2	0x4805 5000	4KB
GPIO3	0x4805 7000	4KB
GPIO4	0x4805 9000	4KB
GPIO5	0x4805 B000	4KB
GPIO6	0x4805 D000	4KB

25.6.2 General-Purpose Interface Registers

25.6.2.1 General-Purpose Interface Register Summary

Table 25-18 summarizes the general-purpose interface GPIO1 to GPIO3 registers.

Table 25-18. General-Purpose Interface GPIO1 to GPIO3 Registers Summary

Register Name	Type	Register Width (Bits)	Address Offset	GPIO1 L4 Physical Address	GPIO2 L4 Physical Address	GPIO3 L4 Physical Address
GPIO_REVISION	R	32	0x0000 0000	0x4A31 0000	0x4805 5000	0x4805 7000
GPIO_SYSCONFIG	RW	32	0x0000 0010	0x4A31 0010	0x4805 5010	0x4805 7010
RESERVED			0x0000 0020	0x4A31 0020	0x4805 5020	0x4805 7020
GPIO_IRQSTATUS_RAW_0	RW	32	0x0000 0024	0x4A31 0024	0x4805 5024	0x4805 7024
GPIO_IRQSTATUS_RAW_1	RW	32	0x0000 0028	0x4A31 0028	0x4805 5028	0x4805 7028
GPIO_IRQSTATUS_0	RW	32	0x0000 002C	0x4A31 002C	0x4805 502C	0x4805 702C
GPIO_IRQSTATUS_1	RW	32	0x0000 0030	0x4A31 0030	0x4805 5030	0x4805 7030
GPIO_IRQSTATUS_SET_0	RW	32	0x0000 0034	0x4A31 0034	0x4805 5034	0x4805 7034
GPIO_IRQSTATUS_SET_1	RW	32	0x0000 0038	0x4A31 0038	0x4805 5038	0x4805 7038
GPIO_IRQSTATUS_CLR_0	RW	32	0x0000 003C	0x4A31 003C	0x4805 503C	0x4805 703C
GPIO_IRQSTATUS_CLR_1	RW	32	0x0000 0040	0x4A31 0040	0x4805 5040	0x4805 7040
GPIO_IRQWAKEN_0	RW	32	0x0000 0044	0x4A31 0044	0x4805 5044	0x4805 7044
GPIO_IRQWAKEN_1	RW	32	0x0000 0048	0x4A31 0048	0x4805 5048	0x4805 7048
GPIO_SYSSTATUS	R	32	0x0000 0114	0x4A31 0114	0x4805 5114	0x4805 7114
RESERVED	RW	32	0x0000 0118	0x4A31 0118	0x4805 5118	0x4805 7118
RESERVED	RW	32	0x0000 011C	0x4A31 011C	0x4805 511C	0x4805 711C
GPIO_WAKEUPENABLE	RW	32	0x0000 0120	0x4A31 0120	0x4805 5120	0x4805 7120
RESERVED	RW	32	0x0000 0128	0x4A31 0128	0x4805 5128	0x4805 7128
RESERVED	RW	32	0x0000 012C	0x4A31 012C	0x4805 512C	0x4805 712C
GPIO_CTRL	RW	32	0x0000 0130	0x4A31 0130	0x4805 5130	0x4805 7130
GPIO_OE	RW	32	0x0000 0134	0x4A31 0134	0x4805 5134	0x4805 7134
GPIO_DATAIN	R	32	0x0000 0138	0x4A31 0138	0x4805 5138	0x4805 7138
GPIO_DATAOUT	RW	32	0x0000 013C	0x4A31 013C	0x4805 513C	0x4805 713C
GPIO_LEVELDETECT0	RW	32	0x0000 0140	0x4A31 0140	0x4805 5140	0x4805 7140
GPIO_LEVELDETECT1	RW	32	0x0000 0144	0x4A31 0144	0x4805 5144	0x4805 7144
GPIO_RISINGDETECT	RW	32	0x0000 0148	0x4A31 0148	0x4805 5148	0x4805 7148
GPIO_FALLINGDETECT	RW	32	0x0000 014C	0x4A31 014C	0x4805 514C	0x4805 714C

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Table 25-18. General-Purpose Interface GPIO1 to GPIO3 Registers Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	GPIO1 L4 Physical Address	GPIO2 L4 Physical Address	GPIO3 L4 Physical Address
GPIO_DEBOUNCENABLE	RW	32	0x0000 0150	0x4A31 0150	0x4805 5150	0x4805 7150
GPIO_DEBOUNCINGTIME	RW	32	0x0000 0154	0x4A31 0154	0x4805 5154	0x4805 7154
RESERVED	RW	32	0x0000 0160	0x4A31 0160	0x4805 5160	0x4805 7160
RESERVED	RW	32	0x0000 0164	0x4A31 0164	0x4805 5164	0x4805 7164
RESERVED	RW	32	0x0000 0170	0x4A31 0170	0x4805 5170	0x4805 7170
RESERVED	RW	32	0x0000 0174	0x4A31 0174	0x4805 5174	0x4805 7174
GPIO_CLEARWKUPENA	RW	32	0x0000 0180	0x4A31 0180	0x4805 5180	0x4805 7180
GPIO_SETWKUENA	RW	32	0x0000 0184	0x4A31 0184	0x4805 5184	0x4805 7184
GPIO_CLEARDATAOUT	RW	32	0x0000 0190	0x4A31 0190	0x4805 5190	0x4805 7190
GPIO_SETDATAOUT	RW	32	0x0000 0194	0x4A31 0194	0x4805 5194	0x4805 7194

Table 25-19 summarizes the general-purpose interface GPIO4 to GPIO6 registers.

Table 25-19. General-Purpose Interface GPIO4 to GPIO6 Registers Summary

Register Name	Type	Register Width (Bits)	Address Offset	GPIO4 L4 Physical Address	GPIO5 L4 Physical Address	GPIO6 L4 Physical Address
GPIO_REVISION	R	32	0x0000 0000	0x4805 9000	0x4805 B000	0x4805 D000
GPIO_SYSCONFIG	RW	32	0x0000 0010	0x4805 9010	0x4805 B010	0x4805 D010
RESERVED			0x0000 0020	0x4805 9020	0x4805 B020	0x4805 D020
GPIO_IRQSTATUS_RAW_0	RW	32	0x0000 0024	0x4805 9024	0x4805 B024	0x4805 D024
GPIO_IRQSTATUS_RAW_1	RW	32	0x0000 0028	0x4805 9028	0x4805 B028	0x4805 D028
GPIO_IRQSTATUS_0	RW	32	0x0000 002C	0x4805 902C	0x4805 B02C	0x4805 D02C
GPIO_IRQSTATUS_1	RW	32	0x0000 0030	0x4805 9030	0x4805 B030	0x4805 D030
GPIO_IRQSTATUS_SET_0	RW	32	0x0000 0034	0x4805 9034	0x4805 B034	0x4805 D034
GPIO_IRQSTATUS_SET_1	RW	32	0x0000 0038	0x4805 9038	0x4805 B038	0x4805 D038
GPIO_IRQSTATUS_CLR_0	RW	32	0x0000 003C	0x4805 903C	0x4805 B03C	0x4805 D03C
GPIO_IRQSTATUS_CLR_1	RW	32	0x0000 0040	0x4805 9040	0x4805 B040	0x4805 D040
GPIO_IRQWAKEN_0	RW	32	0x0000 0044	0x4805 9044	0x4805 B044	0x4805 D044
GPIO_IRQWAKEN_1	RW	32	0x0000 0048	0x4805 9048	0x4805 B048	0x4805 D048
GPIO_SYSSTATUS	R	32	0x0000 0114	0x4805 9114	0x4805 B114	0x4805 D114
RESERVED	RW	32	0x0000 0118	0x4805 9118	0x4805 B118	0x4805 D118
RESERVED	RW	32	0x0000 011C	0x4805 911C	0x4805 B11C	0x4805 D11C
GPIO_WAKEUPENABLE	RW	32	0x0000 0120	0x4805 9120	0x4805 B120	0x4805 D120
RESERVED	RW	32	0x0000 0128	0x4805 9128	0x4805 B128	0x4805 D128
RESERVED	RW	32	0x0000 012C	0x4805 912C	0x4805 B12C	0x4805 D12C
GPIO_CTRL	RW	32	0x0000 0130	0x4805 9130	0x4805 B130	0x4805 D130
GPIO_OE	RW	32	0x0000 0134	0x4805 9134	0x4805 B134	0x4805 D134
GPIO_DATAIN	R	32	0x0000 0138	0x4805 9138	0x4805 B138	0x4805 D138
GPIO_DATAOUT	RW	32	0x0000 013C	0x4805 913C	0x4805 B13C	0x4805 D13C
GPIO_LEVELDETECT0	RW	32	0x0000 0140	0x4805 9140	0x4805 B140	0x4805 D140
GPIO_LEVELDETECT1	RW	32	0x0000 0144	0x4805 9144	0x4805 B144	0x4805 D144
GPIO_RISINGDETECT	RW	32	0x0000 0148	0x4805 9148	0x4805 B148	0x4805 D148
GPIO_FALLINGDETECT	RW	32	0x0000 014C	0x4805 914C	0x4805 B14C	0x4805 D14C
GPIO_DEBOUNCENABLE	RW	32	0x0000 0150	0x4805 9150	0x4805 B150	0x4805 D150
GPIO_DEBOUNCINGTIME	RW	32	0x0000 0154	0x4805 9154	0x4805 B154	0x4805 D154
RESERVED	RW	32	0x0000 0160	0x4805 9160	0x4805 B160	0x4805 D160
RESERVED	RW	32	0x0000 0164	0x4805 9164	0x4805 B164	0x4805 D164

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Table 25-19. General-Purpose Interface GPIO4 to GPIO6 Registers Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	GPIO4 L4 Physical Address	GPIO5 L4 Physical Address	GPIO6 L4 Physical Address
RESERVED	RW	32	0x0000 0170	0x4805 9170	0x4805 B170	0x4805 D170
RESERVED	RW	32	0x0000 0174	0x4805 9174	0x4805 B174	0x4805 D174
GPIO_CLEARWKUPENA	RW	32	0x0000 0180	0x4805 9180	0x4805 B180	0x4805 D180
GPIO_SETWKUENA	RW	32	0x0000 0184	0x4805 9184	0x4805 B184	0x4805 D184
GPIO_CLEARDATAOUT	RW	32	0x0000 0190	0x4805 9190	0x4805 B190	0x4805 D190
GPIO_SETDATAOUT	RW	32	0x0000 0194	0x4805 9194	0x4805 B194	0x4805 D194

25.6.2.2 General-Purpose Interface Register Description

Table 25-20 through Table 25-74 describe the individual general-purpose interface registers.

Table 25-20. GPIO_REVISION

Address Offset	0x0000 0000		
Physical Address	0x4A31 0000	**Instance**	GPIO1
	0x4805 5000		GPIO2
	0x4805 7000		GPIO3
	0x4805 9000		GPIO4
	0x4805 B000		GPIO5
	0x4805 D000		GPIO6
Description	IP revision identifier (X.Y.R)		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP revision	R	See(1)

(1) TI Internal Data

Table 25-21. Register Call Summary for Register GPIO_REVISION

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- General-Purpose Interface Register Summary: [0] [1]

Table 25-22. GPIO_SYSCONFIG

Address Offset	0x0000 0010		
Physical Address	0x4A31 0010	**Instance**	GPIO1
	0x4805 5010		GPIO2
	0x4805 7010		GPIO3
	0x4805 9010		GPIO4
	0x4805 B010		GPIO5
	0x4805 D010		GPIO6
Description	System configuration register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																											IDLEMODE		ENAWAKEUP		SOFTRESET		AUTOIDLE

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Bits	Field Name	Description	Type	Reset
31:5	RESERVED	Reserved	R	0x0000000
4:3	IDLEMODE	0x0: Force-idle: An idle request is acknowledged unconditionally. 0x1: No-idle: An idle request is never acknowledged. 0x2: Smart-idle: The acknowledgment to an idle request is given based on the internal activity (see 4.1.2). 0x3: Smart-idle wakeup	RW	0x0
2	ENAWAKEUP	Wake-up control 0x0: Wake-up generation is disabled. 0x1: Wake-up capability is enabled upon expected transition on input GPIO pin.	RW	0
1	SOFTRESET	Software reset. Set this bit to 1 to trigger a module reset. The bit is automatically reset by the hardware. During reads, it always returns 0. 0x0: Normal mode 0x1: The module is reset.	RW	0
0	AUTOIDLE	OCP clock gating control. 0x0: Internal Interface OCP clock is free-running. 0x1: Automatic internal OCP clock gating, based on the OCP interface activity	RW	0

Table 25-23. Register Call Summary for Register GPIO_SYSCONFIG

General-Purpose Interface Functional Description
- Asynchronous Path: Wake-Up Request Generation: [0]
- General-Purpose Interface Hardware and Software Reset: [1] [2] [3]
- System Power Management and Wakeup: [4] [5] [6] [7] [8] [9]
- Module Power Saving: [10] [11] [12] [13] [14] [15]

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- General-Purpose Interface Module Global Initialization: [16] [17] [18] [19]

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- General-Purpose Interface Register Summary: [20] [21]

Table 25-24. GPIO_IRQSTATUS_RAW_0

Address Offset	0x0000 0024		
Physical Address	0x4A31 0024 0x4805 5024 0x4805 7024 0x4805 9024 0x4805 B024 0x4805 D024	**Instance**	GPIO1 GPIO2 GPIO3 GPIO4 GPIO5 GPIO6
Description	Per-event raw interrupt status vector (corresponding to first line of interrupt)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTLINE																															

Bits	Field Name	Description	Type	Reset
31:0	INTLINE	Status raw for interrupt line	RW	0x0000 0000

Table 25-25. Register Call Summary for Register GPIO_IRQSTATUS_RAW_0

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- General-Purpose Interface Register Summary: [0] [1]

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Table 25-26. GPIO_IRQSTATUS_RAW_1

Address Offset	0x0000 0028		
Physical Address	0x4A31 0028 0x4805 5028 0x4805 7028 0x4805 9028 0x4805 B028 0x4805 D028	**Instance**	GPIO1 GPIO2 GPIO3 GPIO4 GPIO5 GPIO6
Description	Per-event raw interrupt status vector (corresponding to second line of interrupt)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTLINE																															

Bits	Field Name	Description	Type	Reset
31:0	INTLINE	Status raw for interrupt line	RW	0x0000 0000

Table 25-27. Register Call Summary for Register GPIO_IRQSTATUS_RAW_1

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- General-Purpose Interface Register Summary: [0] [1]

Table 25-28. GPIO_IRQSTATUS_0

Address Offset	0x0000 002C		
Physical Address	0x4A31 002C 0x4805 502C 0x4805 702C 0x4805 902C 0x4805 B02C 0x4805 D02C	**Instance**	GPIO1 GPIO2 GPIO3 GPIO4 GPIO5 GPIO6
Description	Per-event interrupt status vector (enabled) (corresponding to first line of interrupt)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTLINE																															

Bits	Field Name	Description	Type	Reset
31:0	INTLINE	Status for interrupt line	RW	0x0000 0000

Table 25-29. Register Call Summary for Register GPIO_IRQSTATUS_0

General-Purpose Interface Functional Description

- Synchronous Path: Interrupt Request Generation: [0]
- Asynchronous Path: Wake-Up Request Generation: [1] [2]
- Interrupt (or Wake-Up) Line Release: [3]
- Interrupt Request Generation: [4] [5] [6] [7] [8]

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- General-Purpose Interface Register Summary: [9] [10]

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Table 25-30. GPIO_IRQSTATUS_1

Address Offset	0x0000 0030		
Physical Address	0x4A31 0030	**Instance**	GPIO1
	0x4805 5030		GPIO2
	0x4805 7030		GPIO3
	0x4805 9030		GPIO4
	0x4805 B030		GPIO5
	0x4805 D030		GPIO6
Description	Per-event enabled interrupt status vector (corresponding to second line of interrupt)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTLINE																															

Bits	Field Name	Description	Type	Reset
31:0	INTLINE	Status for interrupt line	RW	0x0000 0000

Table 25-31. Register Call Summary for Register GPIO_IRQSTATUS_1

General-Purpose Interface Functional Description

- Synchronous Path: Interrupt Request Generation: [0]
- Asynchronous Path: Wake-Up Request Generation: [1] [2]
- Interrupt (or Wake-Up) Line Release: [3]
- Interrupt Request Generation: [4] [5] [6] [7] [8]

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- General-Purpose Interface Register Summary: [9] [10]

Table 25-32. GPIO_IRQSTATUS_SET_0

Address Offset	0x0000 0034		
Physical Address	0x4A31 0034	**Instance**	GPIO1
	0x4805 5034		GPIO2
	0x4805 7034		GPIO3
	0x4805 9034		GPIO4
	0x4805 B034		GPIO5
	0x4805 D034		GPIO6
Description	Per-event interrupt enable set vector (corresponding to first line of interrupt)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTLINE																															

Bits	Field Name	Description	Type	Reset
31:0	INTLINE	Status set for interrupt line	RW	0x0000 0000

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Table 25-33. Register Call Summary for Register GPIO_IRQSTATUS_SET_0

General-Purpose Interface Overview
- General-Purpose Interface Overview: [0]

General-Purpose Interface Functional Description
- General-Purpose Interface Block Diagram: [1]
- Synchronous Path: Interrupt Request Generation: [2]
- Asynchronous Path: Wake-Up Request Generation: [3]
- Interrupt Request Generation: [4] [5] [6] [7]
- General-Purpose Interface Data Input/Output Capabilities: [8] [9] [10]
- Description: [11]
- Set Register Addresses: [12] [13] [14]

General-Purpose Interface Programming Guide
- General-Purpose Interface Module Global Initialization: [15]
- General-Purpose Interface Set Bit Function: [16]

General-Purpose Interface Register Manual
- General-Purpose Interface Register Summary: [17] [18]

Table 25-34. GPIO_IRQSTATUS_SET_1

Address Offset	0x0000 0038		
Physical Address	0x4A31 0038	**Instance**	GPIO1
	0x4805 5038		GPIO2
	0x4805 7038		GPIO3
	0x4805 9038		GPIO4
	0x4805 B038		GPIO5
	0x4805 D038		GPIO6
Description	Per-event enable set interrupt vector (corresponding to second line of interrupt)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTLINE																															

Bits	Field Name	Description	Type	Reset
31:0	INTLINE	Status set for interrupt line	RW	0x0000 0000

Table 25-35. Register Call Summary for Register GPIO_IRQSTATUS_SET_1

General-Purpose Interface Overview
- General-Purpose Interface Overview: [0]

General-Purpose Interface Functional Description
- General-Purpose Interface Block Diagram: [1]
- Synchronous Path: Interrupt Request Generation: [2]
- Asynchronous Path: Wake-Up Request Generation: [3]
- Interrupt Request Generation: [4] [5] [6] [7]
- General-Purpose Interface Data Input/Output Capabilities: [8]
- Description: [9]
- Set Register Addresses: [10] [11] [12]

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- General-Purpose Interface Module Global Initialization: [13]
- General-Purpose Interface Set Bit Function: [14]

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- General-Purpose Interface Register Summary: [15] [16]

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Table 25-36. GPIO_IRQSTATUS_CLR_0

Address Offset	0x0000 003C		
Physical Address	0x4A31 003C	**Instance**	GPIO1
	0x4805 503C		GPIO2
	0x4805 703C		GPIO3
	0x4805 903C		GPIO4
	0x4805 B03C		GPIO5
	0x4805 D03C		GPIO6
Description	Per-event interrupt enable clear vector (corresponding to first line of interrupt)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTLINE																															

Bits	Field Name	Description	Type	Reset
31:0	INTLINE	Status clear for interrupt line	RW	0x0000 0000

Table 25-37. Register Call Summary for Register GPIO_IRQSTATUS_CLR_0

General-Purpose Interface Overview
- General-Purpose Interface Overview: [0]

General-Purpose Interface Functional Description
- General-Purpose Interface Block Diagram: [1]
- Synchronous Path: Interrupt Request Generation: [2]
- Asynchronous Path: Wake-Up Request Generation: [3]
- Interrupt Request Generation: [4] [5]
- Description: [6]
- Clear Register Addresses: [7] [8] [9]

General-Purpose Interface Programming Guide
- General-Purpose Interface Clear Bit Function: [10]

General-Purpose Interface Register Manual
- General-Purpose Interface Register Summary: [11] [12]

Table 25-38. GPIO_IRQSTATUS_CLR_1

Address Offset	0x0000 0040		
Physical Address	0x4A31 0040	**Instance**	GPIO1
	0x4805 5040		GPIO2
	0x4805 7040		GPIO3
	0x4805 9040		GPIO4
	0x4805 B040		GPIO5
	0x4805 D040		GPIO6
Description	Per-event enable clear interrupt vector (corresponding to second line of interrupt)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTLINE																															

Bits	Field Name	Description	Type	Reset
31:0	INTLINE	Status clear for interrupt line	RW	0x0000 0000

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Table 25-39. Register Call Summary for Register GPIO_IRQSTATUS_CLR_1

General-Purpose Interface Overview
- General-Purpose Interface Overview: [0]

General-Purpose Interface Functional Description
- General-Purpose Interface Block Diagram: [1]
- Synchronous Path: Interrupt Request Generation: [2]
- Asynchronous Path: Wake-Up Request Generation: [3]
- Interrupt Request Generation: [4] [5]
- Description: [6]
- Clear Register Addresses: [7] [8] [9]

General-Purpose Interface Programming Guide
- General-Purpose Interface Clear Bit Function: [10]

General-Purpose Interface Register Manual
- General-Purpose Interface Register Summary: [11] [12]

Table 25-40. GPIO_IRQWAKEN_0

Address Offset	0x0000 0044		
Physical Address	0x4A31 0044	**Instance**	GPIO1
	0x4805 5044		GPIO2
	0x4805 7044		GPIO3
	0x4805 9044		GPIO4
	0x4805 B044		GPIO5
	0x4805 D044		GPIO6
Description	Per-event wake-up enable set vector (corresponding to first line of interrupt)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTLINE																															

Bits	Field Name	Description	Type	Reset
31:0	INTLINE	Wakeup set for interrupt line	RW	0x0000 0000

Table 25-41. Register Call Summary for Register GPIO_IRQWAKEN_0

General-Purpose Interface Overview
- General-Purpose Interface Overview: [0]

General-Purpose Interface Functional Description
- Asynchronous Path: Wake-Up Request Generation: [1] [2]
- Module Power Saving: [3]
- Interrupt Request Generation: [4]
- Wake-Up Request Generation: [5]
- General-Purpose Interface Data Input/Output Capabilities: [6] [7]
- Description: [8]
- Clear Register Addresses: [9]
- Set Register Addresses: [10]

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- General-Purpose Interface Module Global Initialization: [11]
- General-Purpose Interface Set Bit Function: [12]
- General-Purpose Interface Clear Bit Function: [13]

General-Purpose Interface Register Manual
- General-Purpose Interface Register Summary: [14] [15]
- General-Purpose Interface Register Description: [16] [17] [18]

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Table 25-42. GPIO_IRQWAKEN_1

Address Offset	0x0000 0048		
Physical Address	0x4A31 0048 0x4805 5048 0x4805 7048 0x4805 9048 0x4805 B048 0x4805 D048	**Instance**	GPIO1 GPIO2 GPIO3 GPIO4 GPIO5 GPIO6
Description	Per-event wake-up enable set vector (corresponding to second line of interrupt)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTLINE																															

Bits	Field Name	Description	Type	Reset
31:0	INTLINE	Wakeup set for interrupt line	RW	0x0000 0000

Table 25-43. Register Call Summary for Register GPIO_IRQWAKEN_1

General-Purpose Interface Overview
- General-Purpose Interface Overview: [0]

General-Purpose Interface Functional Description
- Asynchronous Path: Wake-Up Request Generation: [1] [2]
- Module Power Saving: [3]
- Interrupt Request Generation: [4]
- Wake-Up Request Generation: [5]
- General-Purpose Interface Data Input/Output Capabilities: [6] [7]
- Description: [8]
- Clear Register Addresses: [9]
- Set Register Addresses: [10]

General-Purpose Interface Programming Guide
- General-Purpose Interface Module Global Initialization: [11]
- General-Purpose Interface Set Bit Function: [12]
- General-Purpose Interface Clear Bit Function: [13]

General-Purpose Interface Register Manual
- General-Purpose Interface Register Summary: [14] [15]
- General-Purpose Interface Register Description: [16] [17] [18]

Table 25-44. GPIO_SYSSTATUS

Address Offset	0x0000 0114		
Physical Address	0x4A31 0114 0x4805 5114 0x4805 7114 0x4805 9114 0x4805 B114 0x4805 D114	**Instance**	GPIO1 GPIO2 GPIO3 GPIO4 GPIO5 GPIO6
Description	System status register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															RESETDONE

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Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	RESETDONE	Read 0x0: Internal reset is on-going. Read 0x1: Reset completed	R	0

Table 25-45. Register Call Summary for Register GPIO_SYSSTATUS

General-Purpose Interface Functional Description • General-Purpose Interface Hardware and Software Reset: [0] [1]
General-Purpose Interface Programming Guide • General-Purpose Interface Module Global Initialization: [2]
General-Purpose Interface Register Manual • General-Purpose Interface Register Summary: [3] [4]

Table 25-46. GPIO_WAKEUPENABLE

Address Offset	0x0000 0120		
Physical Address	0x4A31 0120 0x4805 5120 0x4805 7120 0x4805 9120 0x4805 B120 0x4805 D120	**Instance**	GPIO1 GPIO2 GPIO3 GPIO4 GPIO5 GPIO6
Description	Wake-up enable register (legacy) for first line of interrupt		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTLINE																															

Bits	Field Name	Description	Type	Reset
31:0	INTLINE	Wake-up enable for interrupt line **Caution:** This register is kept for backward software compatibility. Use GPIO_IRQWAKEN_0 and GPIO_IRQWAKEN_1 instead. **Caution:** A wake-up event can be enabled using a legacy register as well as the new one, but it must be disabled only through the register that enabled it. 0x0: Wake-up generation is disabled. 0x1: Wake-up generation is enabled.	RW	0x0000 0000

Table 25-47. Register Call Summary for Register GPIO_WAKEUPENABLE

General-Purpose Interface Register Manual • General-Purpose Interface Register Summary: [0] [1]

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Table 25-48. GPIO_CTRL

Address Offset	0x0000 0130		
Physical Address	0x4A31 0130 0x4805 5130 0x4805 7130 0x4805 9130 0x4805 B130 0x4805 D130	**Instance**	GPIO1 GPIO2 GPIO3 GPIO4 GPIO5 GPIO6
Description	GPIO control register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													GATINGRATIO		DISABLEMODULE

Bits	Field Name	Description	Type	Reset
31:3	RESERVED	Reserved	R	0x0000 0000
2:1	GATINGRATIO	Clock gating ratio for event detection 0x0: N = 1 0x1: N = 2 0x2: N = 4 0x3: N = 8	RW	0x1
0	DISABLEMODULE	0x0: Module is enabled, clocks are not gated. 0x1: Module is disabled, internal clocks are gated	RW	0

Table 25-49. Register Call Summary for Register GPIO_CTRL

General-Purpose Interface Functional Description
- Clocking: [0]
- Operating Modes: [1]
- Module Power Saving: [2] [3] [4]

General-Purpose Interface Programming Guide
- General-Purpose Interface Module Global Initialization: [5]

General-Purpose Interface Register Manual
- General-Purpose Interface Register Summary: [6] [7]

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Table 25-50. GPIO_OE

Address Offset	0x0000 0134		
Physical Address	0x4A31 0134	**Instance**	GPIO1
	0x4805 5134		GPIO2
	0x4805 7134		GPIO3
	0x4805 9134		GPIO4
	0x4805 B134		GPIO5
	0x4805 D134		GPIO6
Description	Output enable register. 0: Output enabled ; 1: Output disabled		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTEN																															

Bits	Field Name	Description	Type	Reset
31:0	OUTPUTEN	Output enable 0x0: Output enabled 0x1: Output disabled	RW	0xFFFF FFFF

Table 25-51. Register Call Summary for Register GPIO_OE

General-Purpose Interface Overview
- General-Purpose Interface Overview: [0]

General-Purpose Interface Functional Description
- General-Purpose Interface Data Input/Output Capabilities: [1] [2] [3]

General-Purpose Interface Programming Guide
- General-Purpose Interface Module Global Initialization: [4]

General-Purpose Interface Register Manual
- General-Purpose Interface Register Summary: [5] [6]

Table 25-52. GPIO_DATAIN

Address Offset	0x0000 0138		
Physical Address	0x4A31 0138	**Instance**	GPIO1
	0x4805 5138		GPIO2
	0x4805 7138		GPIO3
	0x4805 9138		GPIO4
	0x4805 B138		GPIO5
	0x4805 D138		GPIO6
Description	Data input register (with sampled input data)		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATAIN																															

Bits	Field Name	Description	Type	Reset
31:0	DATAIN	Sampled input data	R	0x0000 0000

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Table 25-53. Register Call Summary for Register GPIO_DATAIN

General-Purpose Interface Overview • General-Purpose Interface Overview: [0]
General-Purpose Interface Functional Description • System Power Management and Wakeup: [1] • Module Power Saving: [2] • General-Purpose Interface Data Input/Output Capabilities: [3]
General-Purpose Interface Programming Guide • General-Purpose Interface Read Input Register: [4]
General-Purpose Interface Register Manual • General-Purpose Interface Register Summary: [5] [6]

Table 25-54. GPIO_DATAOUT

Address Offset	0x0000 013C		
Physical Address	0x4A31 013C 0x4805 513C 0x4805 713C 0x4805 913C 0x4805 B13C 0x4805 D13C	**Instance**	GPIO1 GPIO2 GPIO3 GPIO4 GPIO5 GPIO6
Description	Data output register (data to set on output pins).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATAOUT																															

Bits	Field Name	Description	Type	Reset
31:0	DATAOUT	Data to set on output pins	RW	0x0000 0000

Table 25-55. Register Call Summary for Register GPIO_DATAOUT

General-Purpose Interface Overview • General-Purpose Interface Overview: [0] [1]
General-Purpose Interface Functional Description • General-Purpose Interface Data Input/Output Capabilities: [2] • Description: [3]
General-Purpose Interface Programming Guide • General-Purpose Interface Write Output Register: [4]
General-Purpose Interface Register Manual • General-Purpose Interface Register Summary: [5] [6]

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Table 25-56. GPIO_LEVELDETECT0

Address Offset	0x0000 0140		
Physical Address	0x4A31 0140 0x4805 5140 0x4805 7140 0x4805 9140 0x4805 B140 0x4805 D140	**Instance**	GPIO1 GPIO2 GPIO3 GPIO4 GPIO5 GPIO6
Description	Detect low-level register. 0: Low-level detection disabled; 1: Low-level detection enabled		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LEVELDETECT0																															

Bits	Field Name	Description	Type	Reset
31:0	LEVELDETECT0	Low-level detection 0x0: Low-level detection disabled 0x1: Low-level detection enabled	RW	0x0000 0000

Table 25-57. Register Call Summary for Register GPIO_LEVELDETECT0

General-Purpose Interface Functional Description
- Module Power Saving: [0] [1]

General-Purpose Interface Programming Guide
- General-Purpose Interface Module Global Initialization: [2]

General-Purpose Interface Register Manual
- General-Purpose Interface Register Summary: [3] [4]

Table 25-58. GPIO_LEVELDETECT1

Address Offset	0x0000 0144		
Physical Address	0x4A31 0144 0x4805 5144 0x4805 7144 0x4805 9144 0x4805 B144 0x4805 D144	**Instance**	GPIO1 GPIO2 GPIO3 GPIO4 GPIO5 GPIO6
Description	Detect high-level register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LEVELDETECT1																															

Bits	Field Name	Description	Type	Reset
31:0	LEVELDETECT1	0x0: High-level detection disabled 0x1: High-level detection enabled	RW	0x0000 0000

Table 25-59. Register Call Summary for Register GPIO_LEVELDETECT1

General-Purpose Interface Functional Description
- Module Power Saving: [0] [1]

General-Purpose Interface Programming Guide
- General-Purpose Interface Module Global Initialization: [2]

General-Purpose Interface Register Manual
- General-Purpose Interface Register Summary: [3] [4]

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Table 25-60. GPIO_RISINGDETECT

Address Offset	0x0000 0148		
Physical Address	0x4A31 0148 0x4805 5148 0x4805 7148 0x4805 9148 0x4805 B148 0x4805 D148	**Instance**	GPIO1 GPIO2 GPIO3 GPIO4 GPIO5 GPIO6
Description	Detect rising edge register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RISINGDETECT																															

Bits	Field Name	Description	Type	Reset
31:0	RISINGDETECT	0x0: Rising edge detection disabled 0x1: Rising edge detection enabled	RW	0x0000 0000

Table 25-61. Register Call Summary for Register GPIO_RISINGDETECT

General-Purpose Interface Functional Description
- Module Power Saving: [0] [1]

General-Purpose Interface Programming Guide
- General-Purpose Interface Module Global Initialization: [2]

General-Purpose Interface Register Manual
- General-Purpose Interface Register Summary: [3] [4]

Table 25-62. GPIO_FALLINGDETECT

Address Offset	0x0000 014C		
Physical Address	0x4A31 014C 0x4805 514C 0x4805 714C 0x4805 914C 0x4805 B14C 0x4805 D14C	**Instance**	GPIO1 GPIO2 GPIO3 GPIO4 GPIO5 GPIO6
Description	Detect falling edge register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FALLINGDETECT																															

Bits	Field Name	Description	Type	Reset
31:0	FALLINGDETECT	0x0: Falling edge detection disabled 0x1: Falling edge detection enabled	RW	0x0000 0000

Table 25-63. Register Call Summary for Register GPIO_FALLINGDETECT

General-Purpose Interface Functional Description
- Module Power Saving: [0] [1]

General-Purpose Interface Programming Guide
- General-Purpose Interface Module Global Initialization: [2]

General-Purpose Interface Register Manual
- General-Purpose Interface Register Summary: [3] [4]

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Table 25-64. GPIO_DEBOUNCENABLE

Address Offset	0x0000 0150		
Physical Address	0x4A31 0150 0x4805 5150 0x4805 7150 0x4805 9150 0x4805 B150 0x4805 D150	**Instance**	GPIO1 GPIO2 GPIO3 GPIO4 GPIO5 GPIO6
Description	Debouncing enable register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DEBOUNCEENABLE																															

Bits	Field Name	Description	Type	Reset
31:0	DEBOUNCEENABLE	0x0: No debouncing 0x1: Debouncing activated	RW	0x0000 0000

Table 25-65. Register Call Summary for Register GPIO_DEBOUNCENABLE

General-Purpose Interface Functional Description
- Module Power Saving: [0]

General-Purpose Interface Programming Guide
- General-Purpose Interface Module Global Initialization: [1]

General-Purpose Interface Register Manual
- General-Purpose Interface Register Summary: [2] [3]

Table 25-66. GPIO_DEBOUNCINGTIME

Address Offset	0x0000 0154		
Physical Address	0x4A31 0154 0x4805 5154 0x4805 7154 0x4805 9154 0x4805 B154 0x4805 D154	**Instance**	GPIO1 GPIO2 GPIO3 GPIO4 GPIO5 GPIO6
Description	Debouncing value register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								DEBOUNCETIME							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Reserved	R	0x000000
7:0	DEBOUNCETIME	8-bit values specifying the debouncing time in 31 µs steps	RW	0x00

Table 25-67. Register Call Summary for Register GPIO_DEBOUNCINGTIME

General-Purpose Interface Functional Description
- Synchronous Path: Interrupt Request Generation: [0] [1]
- Clocking: [2] [3]
- System Power Management and Wakeup: [4] [5]

General-Purpose Interface Programming Guide
- General-Purpose Interface Module Global Initialization: [6]

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Table 25-67. Register Call Summary for Register GPIO_DEBOUNCINGTIME (continued)

General-Purpose Interface Register Manual • General-Purpose Interface Register Summary: [7] [8]

Table 25-68. GPIO_CLEARWKUPENA

Address Offset	0x0000 0180		
Physical Address	0x4A31 0180 0x4805 5180 0x4805 7180 0x4805 9180 0x4805 B180 0x4805 D180	**Instance**	GPIO1 GPIO2 GPIO3 GPIO4 GPIO5 GPIO6
Description	Clear wake-up-enable register – legacy register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTLINE																															

Bits	Field Name	Description	Type	Reset
31:0	INTLINE	**Caution:** This register is kept for backward software compatibility. Use GPIO_IRQWAKEN_0 and GPIO_IRQWAKEN_1 instead. **Caution:** A wake-up event can be enabled using a legacy register as well as the new one, but it must be disabled only through the register that enabled it. 0x0: No effect 0x1: Clear the corresponding bit in the wake-up-enable register.	RW	0x0000 0000

Table 25-69. Register Call Summary for Register GPIO_CLEARWKUPENA

General-Purpose Interface Register Manual • General-Purpose Interface Register Summary: [0] [1]

Table 25-70. GPIO_SETWKUENA

Address Offset	0x0000 0184		
Physical Address	0x4A31 0184 0x4805 5184 0x4805 7184 0x4805 9184 0x4805 B184 0x4805 D184	**Instance**	GPIO1 GPIO2 GPIO3 GPIO4 GPIO5 GPIO6
Description	Set wake-up-enable register – legacy register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTLINE																															

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Bits	Field Name	Description	Type	Reset
31:0	INTLINE	**Caution:** This register is kept for backward software compatibility. Use GPIO_IRQWAKEN_0 and GPIO_IRQWAKEN_1 instead. **Caution:** A wake-up event can be enabled using a legacy register as well as the new one, but it must be disabled only through the register that enabled it. 0x0: No effect 0x1: Set the corresponding bit in the wake-up-enable register.	RW	0x0000 0000

Table 25-71. Register Call Summary for Register GPIO_SETWKUENA

General-Purpose Interface Register Manual
- General-Purpose Interface Register Summary: [0] [1]

Table 25-72. GPIO_CLEARDATAOUT

Address Offset	0x0000 0190		
Physical Address	0x4A31 0190 0x4805 5190 0x4805 7190 0x4805 9190 0x4805 B190 0x4805 D190	**Instance**	GPIO1 GPIO2 GPIO3 GPIO4 GPIO5 GPIO6
Description	Clear data output register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTLINE																															

Bits	Field Name	Description	Type	Reset
31:0	INTLINE	0x0: No effect 0x1: Clear the corresponding bit in the data output register.	RW	0x0000 0000

Table 25-73. Register Call Summary for Register GPIO_CLEARDATAOUT

General-Purpose Interface Functional Description
- General-Purpose Interface Data Input/Output Capabilities: [0]
- Clear Register Addresses: [1]

General-Purpose Interface Programming Guide
- General-Purpose Interface Clear Bit Function: [2]

General-Purpose Interface Register Manual
- General-Purpose Interface Register Summary: [3] [4]

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Table 25-74. GPIO_SETDATAOUT

Address Offset	0x0000 0194		
Physical Address	0x4A31 0194 0x4805 5194 0x4805 7194 0x4805 9194 0x4805 B194 0x4805 D194	**Instance**	GPIO1 GPIO2 GPIO3 GPIO4 GPIO5 GPIO6
Description	Set data output register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTLINE																															

Bits	Field Name	Description	Type	Reset
31:0	INTLINE	0x0: No effect 0x1: Set the corresponding bit in the data output register.	RW	0x0000 0000

Table 25-75. Register Call Summary for Register GPIO_SETDATAOUT

General-Purpose Interface Functional Description
- General-Purpose Interface Data Input/Output Capabilities: [0]
- Set Register Addresses: [1]

General-Purpose Interface Programming Guide
- General-Purpose Interface Set Bit Function: [2]

General-Purpose Interface Register Manual
- General-Purpose Interface Register Summary: [3] [4]

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Keyboard Controller

This chapter describes the keyboard module of the device.

Topic **Page**

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26.2 Keyboard Controller Environment 5432
26.3 Keyboard Controller Integration 5435
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26.1 Keyboard Controller Overview

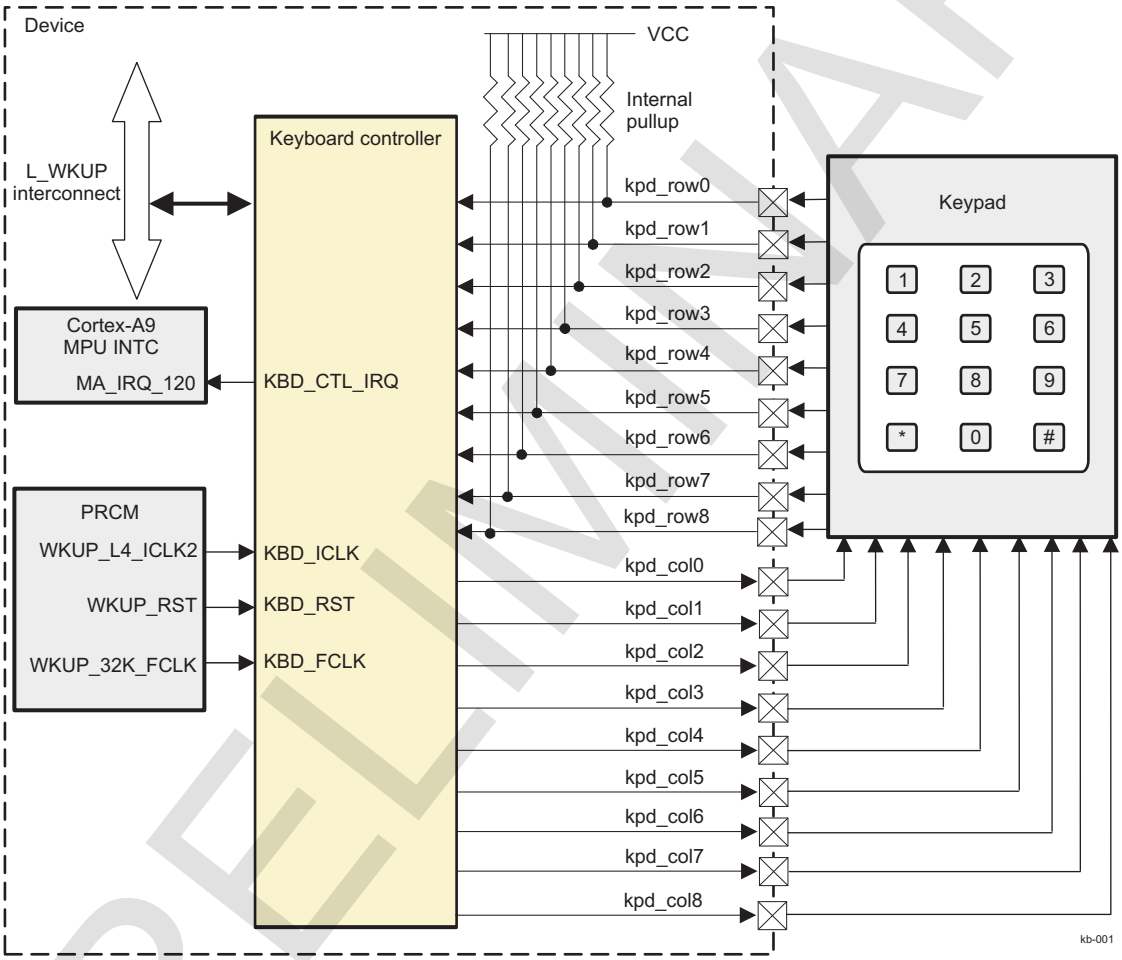
The keyboard controller implements a built-in scanning algorithm for hardware-based key-press decoding and reduces overhead in the microprocessor unit (MPU) software.

The keyboard controller includes a debouncing feature to ensure that only one key combination can be registered in the programmed time.

The keyboard controller can handle up to 9 × 9 keys, works on a 32-kHz clock, and can generate wake-up events when the chip is in sleep mode.

Figure 26-1 shows the keyboard controller.

Figure 26-1. Keyboard Controller Overview



The keyboard controller includes the following main features:

- Support of multiconfiguration keyboards up to 9 rows × 9 columns
- Each key coded on 1 bit in two 32-bit registers
- Long-key value or repeat timing reconfigurable on the fly
- Event detection on key press and key release
- Multikey-press detection and decoding
- Long-key detection on prolonged key press
- Integrated timer with four programmable comparison values
- Programmable time-out on permanent key press or after keyboard release
- Programmable interrupt generation on key events
- Software reset capability

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- Read/write-posted register access modes
- 8-/16-/32-bit access supported on the level 4 (L4) interface
- 32-bit data bus
- 7-bit address bus

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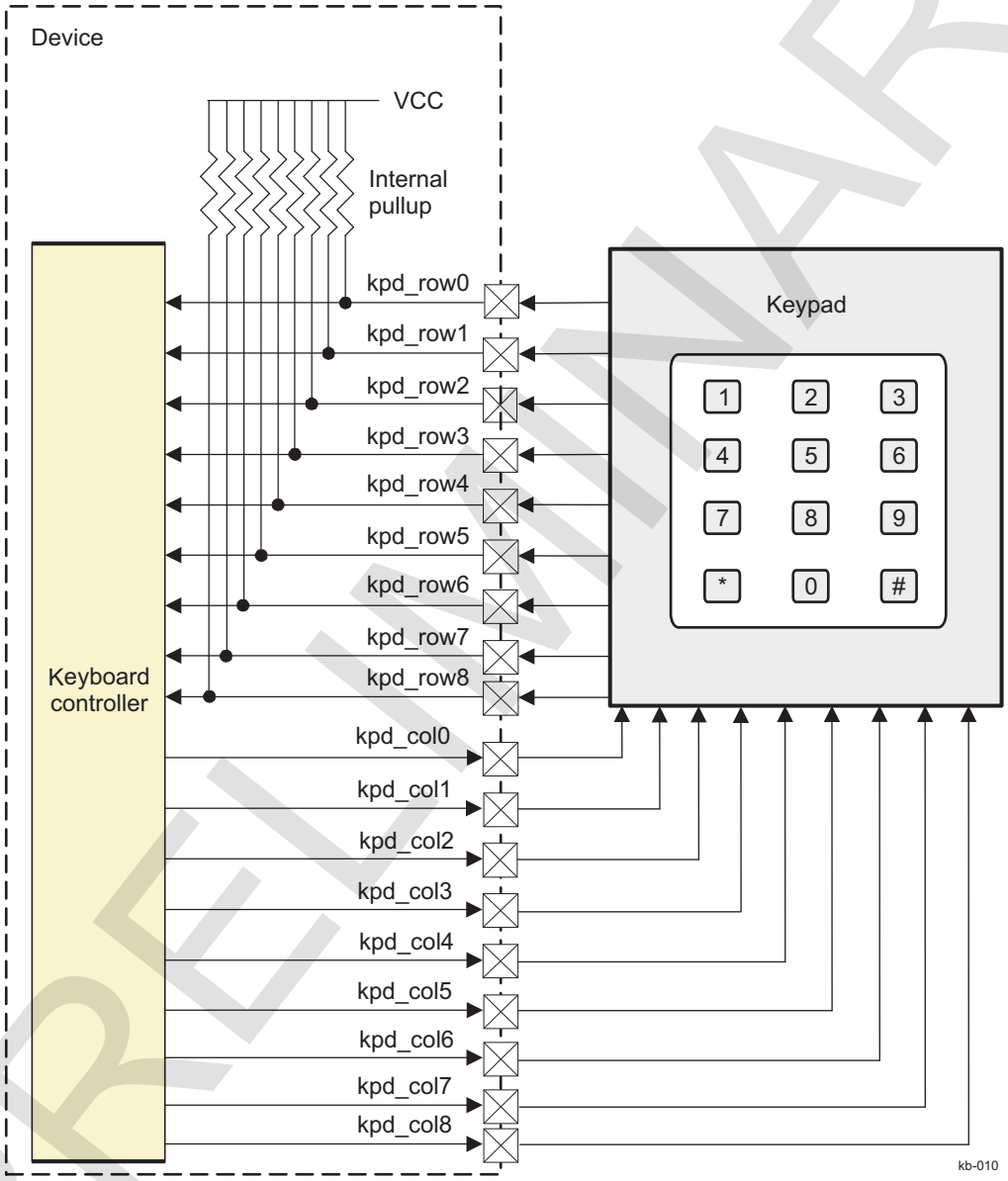
26.2 Keyboard Controller Environment

The keyboard controller external interface pins map on the device pads when the device general-purpose input/output (GPIO) cells are configured and multiplexed for the keypad function by the control module. For more information, see Section 18.4.8, *Pad Functional Multiplexing and Configuration*, and Section 25.2.1, *General-Purpose Interface as a Keyboard interface*.

The external keypad typically connects directly to the keyboard controller of the device (see Figure 26-2).

Figure 26-2. Typical Keyboard Environment



26.2.1 Keyboard Controller Functions/Modes

The keyboard controller executes two functions:

- Keypad scanning and decoding for input of the external key presses. For more information, see Section 26.4.5, *Keyboard Controller Software Mode*, and Section 26.4.6, *Keyboard Controller Hardware Decoding Modes*.
- Device wake-up by interrupt request to the processor when a key is pressed and the device is in idle or sleep mode. For more information, see Section 26.4.6.4, *Keyboard Controller Interrupt Generation*.

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26.2.2 Keyboard Controller Signals

Table 26-1 describes the module signals and specifies their links to functions.

Table 26-1. I/O External Keyboard Signals

Signal	I/O [1]	Description	Reset Value	Function	Wake-Up Capability
kpd_row0	I	Keypad row 0 feed	HiZ (pulled up)	Key reading	Yes
kpd_row1	I	Keypad row 1 feed	HiZ (pulled up)	Key reading	Yes
kpd_row2	I	Keypad row 2 feed	HiZ (pulled up)	Key reading	Yes
kpd_row3	I	Keypad row 3 feed	HiZ (pulled up)	Key reading	Yes
kpd_row4	I	Keypad row 4 feed	HiZ (pulled up)	Key reading	Yes
kpd_row5	I	Keypad row 5 feed	HiZ (pulled up)	Key reading	Yes
kpd_row6	I	Keypad row 6 feed	HiZ (pulled up)	Key reading	Yes
kpd_row7	I	Keypad row 7 feed	HiZ (pulled up)	Key reading	Yes
kpd_row8	I	Keypad row 8 feed	HiZ (pulled up)	Key reading	Yes
kpd_col0	O	Keypad column 0 feed, active low	HiZ	Key reading	No
kpd_col1	O	Keypad column 1 feed, active low	HiZ	Key reading	No
kpd_col2	O	Keypad column 2 feed, active low	HiZ	Key reading	No
kpd_col3	O	Keypad column 3 feed, active low	HiZ	Key reading	No
kpd_col4	O	Keypad column 4 feed, active low	HiZ	Key reading	No
kpd_col5	O	Keypad column 5 feed, active low	HiZ	Key reading	No
kpd_col6	O	Keypad column 6 feed, active low	HiZ	Key reading	No
kpd_col7	O	Keypad column 7 feed, active low	HiZ	Key reading	No
kpd_col8	O	Keypad column 8 feed, active low	HiZ	Key reading	No

[1] I = Input; O = Output

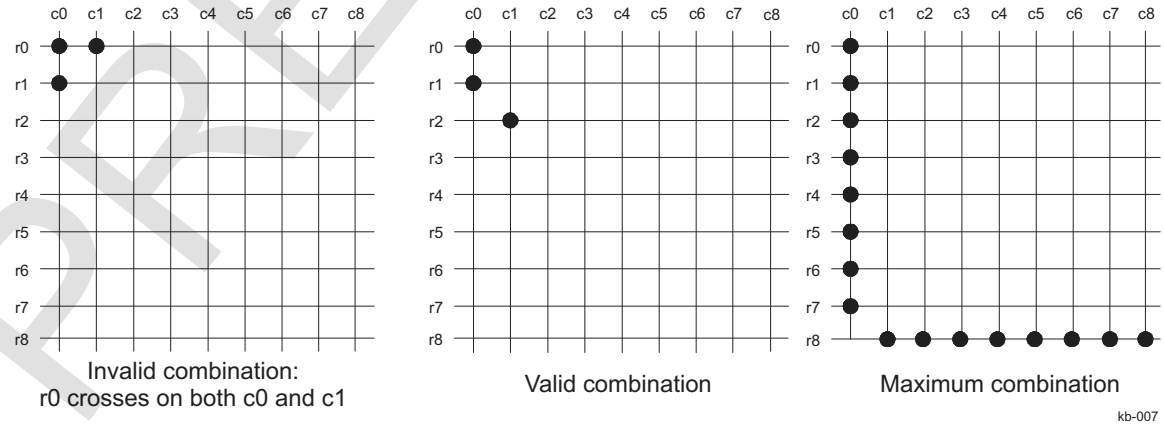
26.2.3 Protocols and Data Formats

The keyboard controller detects and decodes multikey combinations using the following rules:

- Any 2-key combination is valid and can be decoded.
- Combinations using more than two keys are valid only if the rows and columns used do not cross over on another key to be detected. This is caused by equipotent propagation on a row/column (multikey limitations).

Figure 26-3 shows an example of multikey limitation.

Figure 26-3. Multikey Limitation Example



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NOTE: When using the keyboard controller with a smaller keypad (for example, 5 × 5), unused rows must be tied high to prevent disturbing the scanning process. Normally, all rows must be pulled up internally at the I/O cells of the device.

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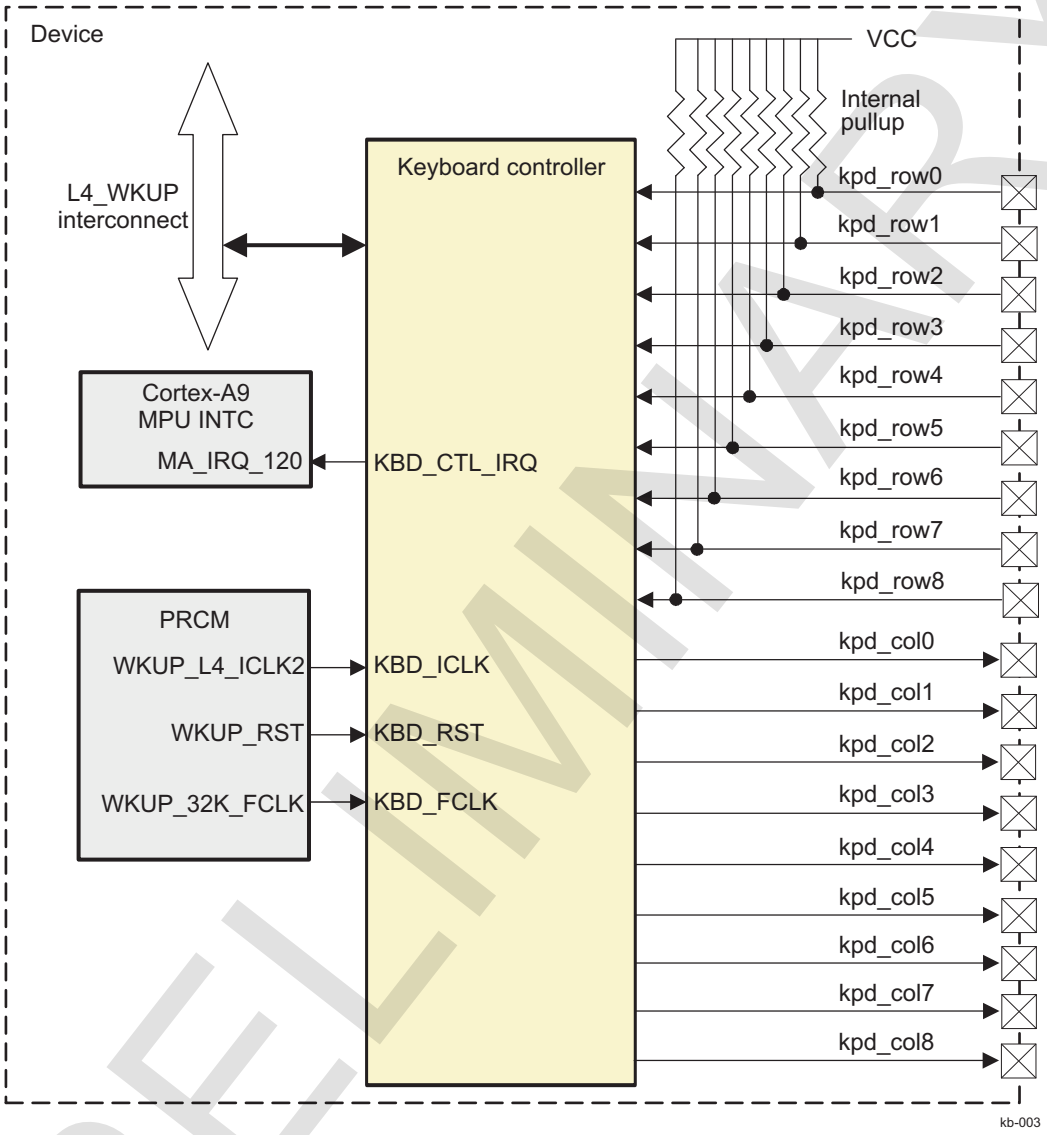
26.3 Keyboard Controller Integration

Figure 26-4 shows keyboard controller integration.

Figure 26-4. Keyboard Controller Integration



The control module must enable the internal pullups of the GPIO cells for all keypad rows (for more information about configuration, see Chapter 18, *Control Module*).

Table 26-2 through Table 26-4 summarize the integration of the module in the device.

Table 26-2. Integration Attributes

Module Instance	Attributes		
	Power Domain	Wake-Up Capability	Interconnect
KEYBOARD CONTROLLER	PD_WKUP	Yes	L4_WKUP

Table 26-3. Clocks and Resets

		Clocks		
Module Instance	Destination Signal Name	Source Signal Name	Source	Description

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Table 26-3. Clocks and Resets (continued)

KEYBOARD CONTROLLER	KBD_FCLK	WKUP_32K_FCLK	PRCM	32-kHz functional clock. For information about power, reset, clock management (PRCM) clock gating and management, see Section 3.1.1.1.4, *Clock Domain-Level Clock Management*, in Chapter 3, *Power, Reset, and Clock Management*.
KEYBOARD CONTROLLER	KBD_ICLK	WKUP_L4_ICLK2	PRCM	L4-interconnect interface clock. For information about PRCM clock gating and management, see Section 3.1.1.1.4, *Clock Domain-Level Clock Management*, in Chapter 3, *Power, Reset, and Clock Management*.
			Resets	
KEYBOARD CONTROLLER	KBD_RST	WKUP_RST	PRCM	Active low asynchronous general reset. For information about PRCM reset sources and distribution, see Section 3.1.1.1.4, *Clock Domain-Level Clock Management*, in Chapter 3, *Power, Reset, and Clock Management*.

Table 26-4. Hardware Requests

Interrupt Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
KEYBOARD CONTROLLER	KBD_CTL_IRQ	MA_IRQ_120	Cortex™-A9 INTC	Interrupt signal to the interrupt controller (INTC) of the MPU. For information about INTC interrupt control, see Chapter 17, *Interrupt Controllers*.

NOTE: For the description of the interrupt source, see Section 26.4.4, *Interrupt Requests*.

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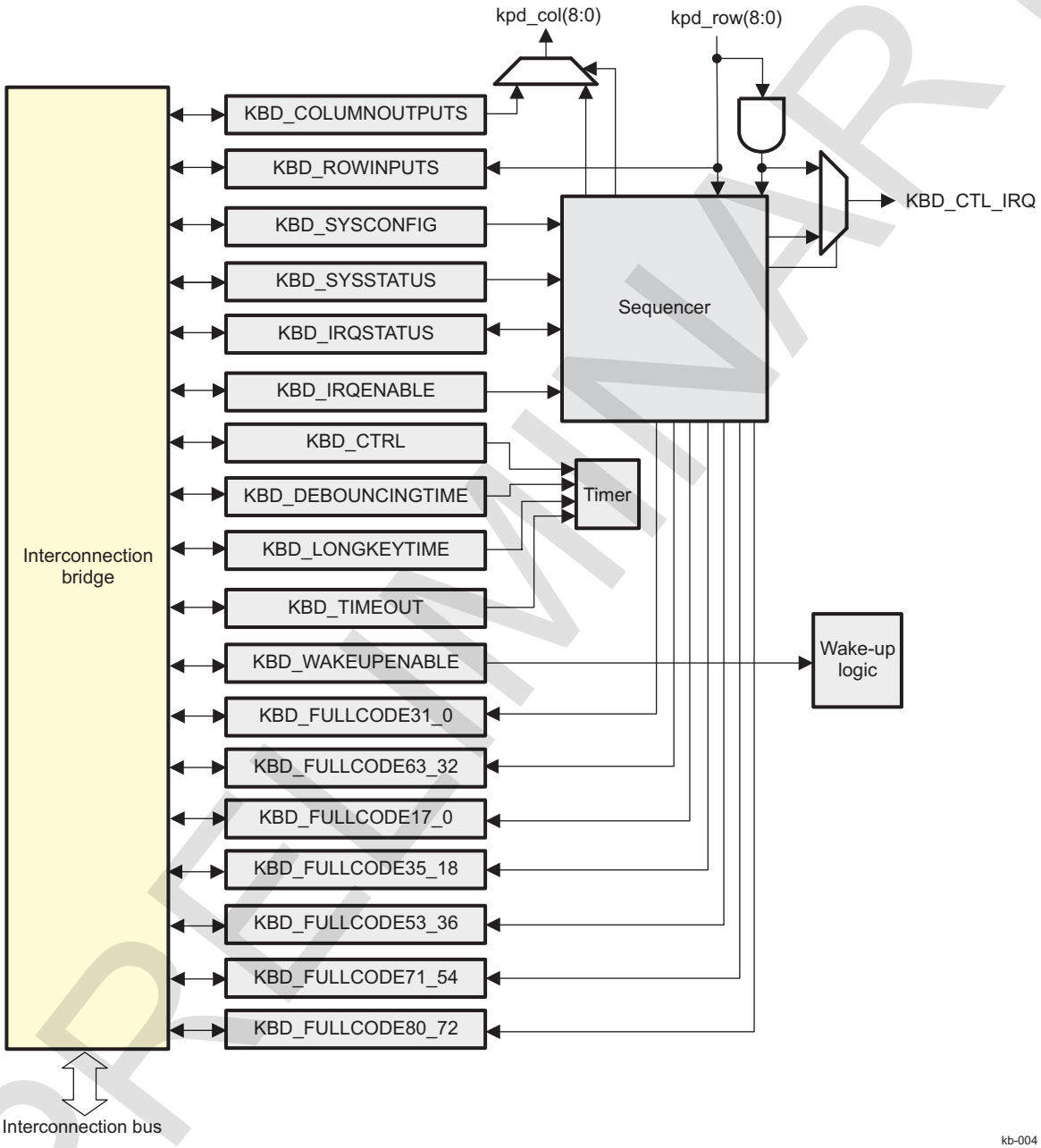
26.4 Keyboard Controller Functional Description

26.4.1 Keyboard Controller Block Diagram

Figure 26-5 shows the functional specification block diagram of the keyboard controller.

Figure 26-5. Keyboard Controller Block Diagram



The keyboard controller detects events issued on any key of the connected keyboard and generates an interrupt to alert the host processor. The built-in hardware-scan algorithm decodes the pressed keys, including multikey combinations.

To reduce MPU software overhead, the hardware performs detecting and decoding in the keyboard controller state-machine. However, hardware decoding can be deactivated so that software handles the scanning algorithm.

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The value of the columns output is determined in the KBD_COLUMNOUTPUTS[8:0] KBC_REG bit field. To activate a keypad row-column connection, the corresponding bit must be 0b0.

The following sections describe subfunctions and subfunction interactions (control, data paths).

26.4.2 Keyboard Controller Software Reset

To perform a software reset, set the KBD_SYSCONFIG[1] SOFTRESET bit to 1. The KBD_SYSSTATUS[0] RESETDONE bit indicates that the software reset is complete when its value is 1. When the software reset completes, the KBD_SYSCONFIG[1] SOFTRESET bit is automatically reset. Software must ensure that the software reset completes before performing mailbox operations.

26.4.3 Keyboard Controller Power Management

Table 26-5 describes the power-management features available for the keyboard controller.

NOTE: For information about source clock gating and sleep/wake-up transitions description, see Section 3.1.1.1.4, *Clock Domain-Level Clock Management*, in Section 3.1.1.1.4, *Power, Reset, and Clock Management*.

Table 26-5. Local Power-Management Features

Feature	Registers	Description
Clock autogating	KBD_SYSCONFIG[0] AUTOGATING	This bit allows local power optimization in the module by gating the KBD_ICLK clock upon interface activity, or gating KBD_FCLK upon internal activity.
Slave idle modes	KBD_SYSCONFIG[4:3] IDLEMODE	Force-idle, no-idle, and smart-idle modes are available.
Clock activity	KBD_SYSCONFIG[9:8] CLOCKACTIVITY	For configuration details, see Table 26-6.
Master standby modes	N/A	N/A
Global wake-up enable	KBD_SYSCONFIG[2] ENAWAKEUP	This bit enables the wake-up feature at the module level. If smart-idle mode is selected, this bit provides the option of smart-idle wake-up-capable mode.
Wake-up sources enable	KBD_WAKEUPENABLE	This register holds one active-high enable bit per event source able to generate a wake-up signal.

Table 26-6 lists the clock activity settings.

Table 26-6. Clock Activity Settings

KBD_SYSCONFIG [9:8] CLOCKACTIVITY Values	Clock State When Module is in IDLE State		Features Available When Module is in IDLE State	Wake-Up Events
	KBD_ICLK	KBD_ FCLK		
00	OFF	OFF	None	The wake-up capability of the module is disabled.
10	OFF	ON	All	Asserting of wake-up signal
01	ON	OFF	None	The wake-up capability of the module is disabled.
11	ON	ON	All	Asserting of wake-up signal

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CAUTION

The PRCM module has no hardware means of reading the CLOCKACTIVITY settings. Thus, software must ensure consistent programming between the keyboard controller CLOCKACTIVITY and keyboard controller clock PRCM control bits. For a description of the ClockActivity feature, see Section 3.1.1.1, *Clock Management*, in Chapter 3, *Power, Reset, and Clock Management*.

26.4.4 Keyboard Controller Interrupt Requests

Table 26-7 lists the event flags, and their mask, that can cause module interrupts.

Table 26-7. Events

Event Flag	Event Mask	Description
KBD_IRQSTATUS[3] MISS_EVENT	–	A miss event occurs.
KBD_IRQSTATUS[2] IT_TIMEOUT	KBD_IRQENABLE[2] IT_TIMEOUT_EN	A time-out event is detected.
KBD_IRQSTATUS[1] IT_LONG_KEY	KBD_IRQENABLE[1] IT_LONG_KEY_EN	A long-key event is detected.
KBD_IRQSTATUS[0] IT_EVENT	KBD_IRQENABLE[0] IT_EVENT_EN	An event is detected.

26.4.5 Keyboard Controller Software Mode

The KBD_CTRL[1] NSOFTWARE_MODE bit selects software mode when it is set to 0.

In software mode, the keyboard controller internal sequencer, which performs automatic scanning and decoding, is disabled. Consequently, software must manually perform the scanning algorithm.

The scanning sequence is managed using the keyboard controller column outputs register (KBD_COLUMNOUTPUTS) and the keyboard controller row inputs register (KBD_ROWINPUTS). In this configuration, the keyboard interrupt is a logical ANDing of all bits of the KBD_ROWINPUTS register.

For more information about the software scan, see Section 26.5.1, *Keyboard Controller Low-Level Programming Model*.

26.4.6 Keyboard Controller Hardware Decoding Modes

26.4.6.1 Functional Modes

When running in hardware (default) decoding mode (the KBD_CTRL[1] NSOFTWARE_ MODE bit is set to 1), the keyboard controller offers several functional modes; these modes are summarized in Table 26-8. The keyboard interrupt depends on the configuration in the keyboard controller interrupt-enable register (KBD_IRQENABLE). If the event is enabled (bit 0 at 1), an interrupt is generated when the sequencer detects an event. Even if this interrupt is disabled, the flag status of the keyboard controller interrupt-status register (KBD_IRQSTATUS) is updated.

Table 26-8. Keyboard Controller Functional Modes

Functional Mode	Associated Interrupt	Associated Timer Value	Description	Control
Keyboard event	Event interrupt	Debouncing value	Occurs when a key is pressed or released Always enabled	KBD_CTRL[8:5] bits must be set to 0 to disable all the other features.
Long key	Long-key interrupt	Long-key value	Used to detect a key that is pressed for a long time Should be associated with the long-key time-out function or repeat mode	KBD_CTRL[5] LONG_KEY bit

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Table 26-8. Keyboard Controller Functional Modes (continued)

Functional Mode	Associated Interrupt	Associated Timer Value	Description	Control
Repeat key	Long-key interrupt	Long-key value	Generates an interrupt every long-key delay No time-out can be associated.	KBD_CTRL[8] REPEAT_MODE bit
Empty time-out	Time-out interrupt	Empty time-out value	Interrupt generated if no key is pressed during an empty time-out period.	KBD_CTRL[6] TIMEOUT_EMPTY bit
Long-key time-out	Time-out interrupt	Long-key time-out value	Associated with the long-key function Generated after a long-key interrupt if no event occurs during a long-key time-out period	KBD_CTRL[7] TIMEOUT_LONG_KEY bit

Each mode can be activated/deactivated by setting the corresponding bits (5, 6, 7, and 8) in the KBD_CTRL register with the appropriate values (for more information, see Section 26.6, *Keyboard Controller Register Manual*).

26.4.6.2 Keyboard Controller Timer

As described in the previous section, each functional mode is associated with a timer value. Depending on the selected mode, the keyboard controller timer is loaded with the corresponding value as set in the related registers:

- KBD_DEBOUNCINGTIME
- KBD_KEYLONGTIME
- KBD_TIMEOUT

Table 26-9 summarizes the values of the keyboard controller timer.

Table 26-9. Keyboard Controller Timer Values

Timer Value	Associated Register Field	Description
Debouncing time	KBD_DEBOUNCINGTIME[5:0] DEBOUNCING_VALUE	To remove the effects of glitches when an event occurs on the keyboard, the controller waits for a debouncing period before taking a snapshot of the current state on the keyboard matrix. The timer is loaded with the debouncing time value after each detected event on the keyboard matrix. An event interrupt is generated after this delay.
Long-key time	KBD_KEYLONGTIME[11:0] LONG_KEY_VALUE	This is the delay before generating a long-key interrupt after an event interrupt. If the long-key mode is selected, the timer is loaded with the long-key time value after an event interrupt is generated. In repeat mode, the timer is reloaded with the same value after a long-key interrupt, and starts to count down again.
Long-key time-out	KBD_TIMEOUT[15:0] TIMEOUT_VALUE	The timer is loaded with the time-out value and then a long-key interrupt is generated and starts to count down. When it reaches 0, a time-out interrupt is generated and the keyboard controller returns to its IDLE state. This long-key time-out does not work in repeat mode.
Empty key time-out	KBD_TIMEOUT[15:0] TIMEOUT_VALUE	The time-out interrupt occurs if no key is pressed during this delay. The keyboard controller then returns to IDLE state.

The timer countdown period depends on three factors:

- The loaded value as set in:
  - KBD_DEBOUNCINGTIME
  - KBD_KEYLONGTIME
  - KBD_TIMEOUT
- The value of the prescale clock timer as set in the KBD_CTRL[4:2] PTV bit field. This programmable clock divider allows the reduction of the clock frequency used by the timer.
- The frequency of the keyboard controller functional clock (32 kHz)

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The period is calculated as follows:

$T_{period} = (T_{value} + 1) \times 2^{PTV + 1} \times T_{clk}$

Where:

T_{value} is the value stored in the KBD_DEBOUNCINGTIME, KBD_KEYLONGTIME, or KBD_TIMEOUT register.

PTV is the value of the KBD_CTRL[4:2] register PTV bit field.

T_{clk} is the period of the 32-kHz functional clock; that is, 31.25 µs.

The KBD_CTRL[4:2] PTV bit field determines the division factor of the timer clock. Table 26-10 lists the divider rates.

Table 26-10. Timer Prescale Values

KBD_CTRL[4:2] PTV Value	Divisor
0	2
1	4
2	8
3	16
4	32
5	64
6	128
7	256

NOTE: The timer minimum period is 62.5 µs; its maximum period is 524.288 seconds.

CAUTION

To prevent undefined results, the KBD_CTRL[4:2] PTV bit field must not be changed when the timer is running.

The timer value registers (KBD_DEBOUNCINGTIME, KBD_KEYLONGTIME, and KBD_TIMEOUT) can be updated at any time, whether or not the timer is running. Nevertheless, the timer is updated only on the fly for the long-key time value. The new debouncing and time-out values are loaded only on the next load. Depending on the updated register, two cases can occur:

- The KBD_KEYLONGTIME register is updated; the new value stored in the KBD_KEYLONGTIME register is loaded into the timer when the register is written. If the timer is already counting down when KBD_KEYLONGTIME is updated, it counts down from the new value loaded in KBD_KEYLONGTIME.
- The KBD_DEBOUNCINGTIME or KBD_TIMEOUT register is updated; the new value is considered only when the next timer loads. If the timer is counting down when the registers are updated, the timer continues counting down from the previous value and is loaded with the new one on the next load.

Regardless of the timer state (stopped, counting down any of the values previously described, etc.), when a new event occurs on the keyboard, the timer is stopped and loaded with the debouncing time value. It then starts counting down.

26.4.6.3 State-Machine Status

To facilitate debugging, each state of the state-machine is coded in a register that indicates the current state of the machine. Table 26-11 lists the corresponding codes.

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Table 26-11. State-Machine Values

KBD_STATEMACHINE[3:0] Value	Description
0x0	Idle
0x1	Scanning
0x2	Load timer debouncing
0x3	Test timer debouncing
0x4	Generated interrupt event
0x6	Load timer long key
0x7	Test timer long key
0x8	Generated interrupt long key
0x9	Load timer time-out
0xA	Test timer time-out
0xB	Generated interrupt time-out
0xF	Other

26.4.6.4 Keyboard Controller Interrupt Generation

26.4.6.4.1 Interrupt-Generation Scheme

The keyboard controller generates one interrupt signal to external INTC KBD_CTL_IRQ. Each functional mode generates dedicated interrupt events (logged in the KBD_IRQSTATUS register) that can be masked or unmasked using the KBD_IRQENABLE register.

The KBD_IRQSTATUS register is updated when the selected functional mode generates an interrupt event. However, the KBD_CTL_IRQ signal is asserted on the related event only when the corresponding bit is set in the KBD_IRQENABLE register.

NOTE: To reset the interrupt status bit, 1 must be written to the appropriate bit of the KBD_IRQSTATUS read/write register.

Figure 26-6 shows the different interrupt events generated in each keyboard controller functional mode and details the relationships between them.

NOTE: Depending on the selected mode, some interrupt events cannot be generated.

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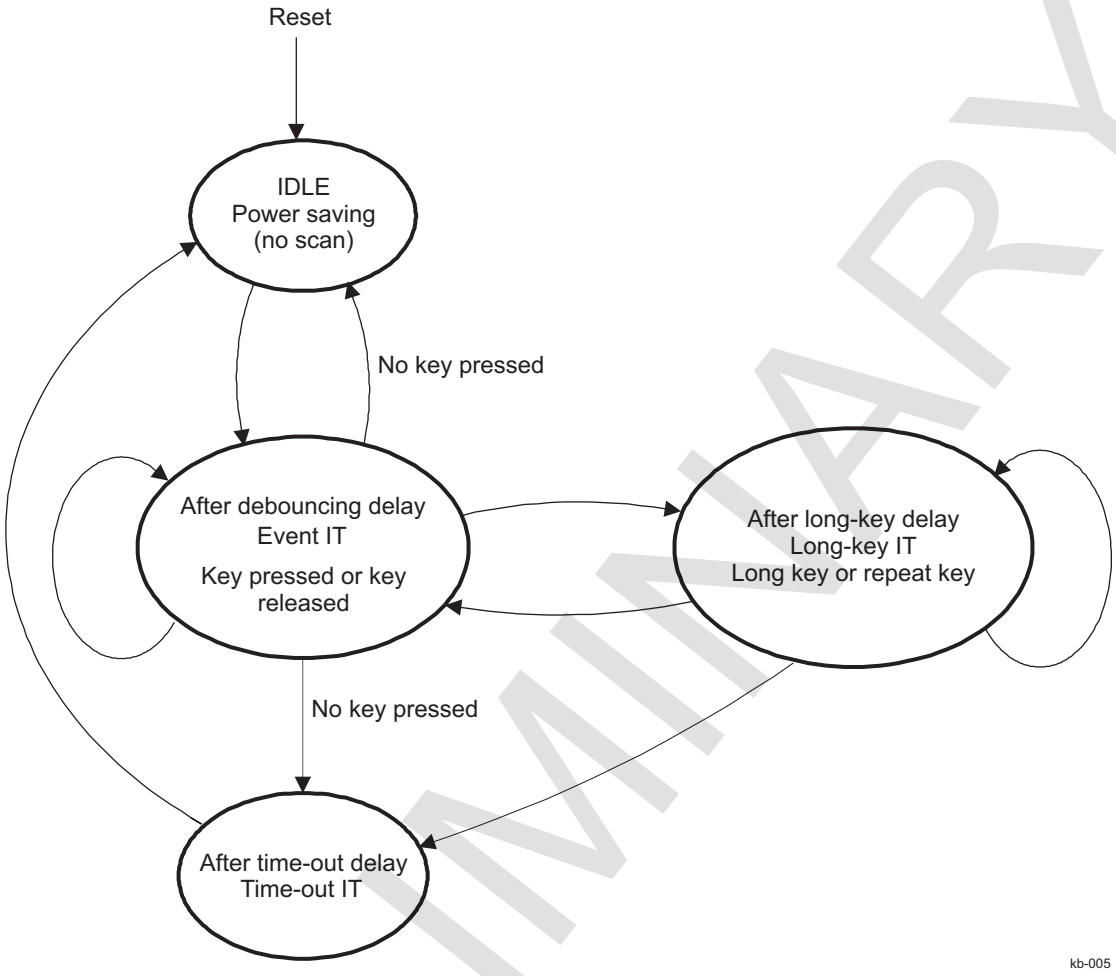
Figure 26-6. Functional Modes and Related Interrupt Events



While running in hardware-decoding mode, the keyboard controller performs automatic scans when not in IDLE state. When a key-press event occurs on the keyboard matrix, the keyboard controller leaves IDLE state and an interrupt event (the KBD_IRQSTATUS[0] IT_EVENT bit) is set after the timer counts down the debouncing delay. An IT_EVENT is generated when a key is pressed or released.

NOTE: An IT_EVENT is generated regardless of the selected functional mode. If no time-out is set and no more keys are pressed, the keyboard controller returns to IDLE state.

If long-key detection mode is set when the timer counts down the long-key delay, an interrupt long key (the KBD_IRQSTATUS[1] IT_LONG_KEY bit) is generated. If the repeat mode is set, the IT_LONG_KEY interrupt is generated periodically every long-key delay.

A time-out can also be set in event detection or long-key detection mode. In this case, a time-out interrupt (the KBD_IRQSTATUS[2] IT_TIMEOUT bit) is generated after the time-out delay timer expires. After such an interrupt, the keyboard controller always returns to IDLE state.

NOTE: No time-out can be set in repeat mode. Only a keyboard event can stop the periodic interrupt generation.

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26.4.6.4.2 Keyboard Buffer and Missed Events (Overrun Feature)

The keyboard controller has an overrun feature: A dedicated buffer allows the keyboard controller to memorize two successive events. If two successive events occur before a read is performed, the second event is stored and a second interrupt is generated when the first interrupt is cleared, allowing two consecutive key events to be received.

If a third event occurs before the first event is treated, a missed event interrupt (the KBD_IRQSTATUS[3] MISS_EVENT bit) is generated to report the lost event.

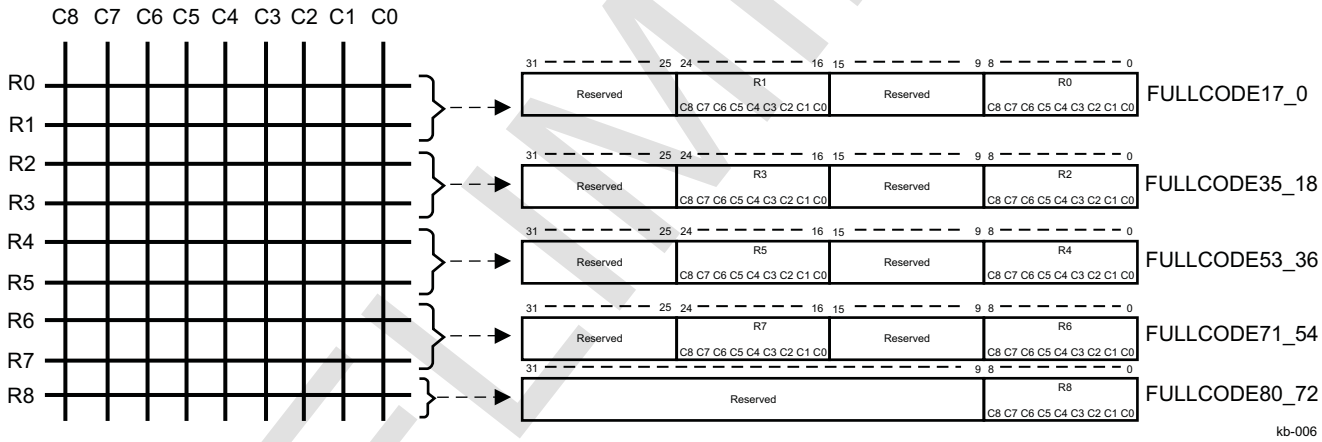
NOTE: The MISS_EVENT interrupt is not routed to the KBD_CTL_IRQ signal; software must check the KBD_IRQSTATUS[3] MISS_EVENT bit to detect any missed events.

26.4.7 Keyboard Controller Key Coding Registers

The keyboard controller matrix pressed keys state (indicating which columns/rows are connected) is reflected in the KBD_FULLCODE17_0 to KBD_FULLCODE80_72 registers, as shown in Figure 26-7. These registers are updated only when interrupt event status is inactive to prevent a lost event.

NOTE: The KBD_FULLCODE31_0 and KBD_FULLCODE63_32 registers, which are limited to supporting keyboards of a maximum 8 × 8 array size, can be used for back-to-back software compatibility.

Figure 26-7. Key Coding Registers



Each of the 9 × 9 keyboard size supporting registers (KBD_FULLCODE17_0 up to KBD_FULLCODE71_54) stores the state of two keyboard rows. The KBD_FULLCODE80_72 register stores the state of the last row, R8:

- The KBD_FULLCODE17_0 register code rows 0, 1 (row 0 is coded between bits 0 and 8, row 1 is coded between bits 16 and 24)
- The KBD_FULLCODE35_18 register code rows 2, 3 (row 2 is coded between bits 0 and 8, row 3 is coded between bits 16 and 24)
- The KBD_FULLCODE53_36 register code rows 4, 5 (row 4 is coded between bits 0 and 8, row 5 is coded between bits 16 and 24)
- The KBD_FULLCODE71_54 register code rows 6, 7 (row 6 is coded between bits 0 and 8, row 7 is coded between bits 16 and 24)
- The KBD_FULLCODE80_72 register code row 8 (row 8 is coded between bits 0 and 8)

In each of these registers (excluding KBD_FULLCODE80_72):

- Bit 0 corresponds to column(0) – row (i) key, … , bit 8 corresponds to column(8) – row (i) key.
- Bits from 9 to 15 are reserved.

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- Bit 16 corresponds to column(0) – row (i+1) key, … , bit 24 corresponds to column (8) – row (i+1) key.
- Bits 31 to 25 are reserved, where i = 0, 2, 4, 6.

In register KBD_FULLCODE80_72 bit 0 corresponds to column (0) – row (8) key, …, the bit 8 corresponds to column (8) – row (8) key, and the remaining bits (from 9 to 31) are reserved.

Each of the 8 × 8-keyboard size supporting registers (KBD_FULLCODE31_0 and KBD_FULLCODE63_32) stores the state of four keyboard rows:

- The KBD_FULLCODE31_0 register code rows 0, 1, 2, and 3 (row 0 is coded between bits 0 and 7, row 1 is coded between bits 8 and 15, row 2 is coded between bits 16 and 23, and row 3 is coded between bits 24 and 31)
- The KBD_FULLCODE63_32 register code rows 4, 5, 6, and 7 (row 4 is coded between bits 0 and 7, row 5 is coded between bits 8 and 15, row 6 is coded between bits 16 and 23, and row 7 is coded between bits 24 and 31)

In these registers:

- KBD_FULLCODE31_0[0] corresponds to column (0) – row (0) key,…, KBD_FULLCODE31_0[7] corresponds to column (7) – row (0).
- KBD_FULLCODE31_0[8] corresponds to column (0) – row (1) key,..., KBD_FULLCODE31_0[15] corresponds to column (7) – row (1).
- KBD_FULLCODE31_0[16] corresponds to column (0) – row (2) key,..., KBD_FULLCODE31_0[23] corresponds to column (7) – row (2).
- KBD_FULLCODE31_0[24] corresponds to column (0) – row (3) key,..., KBD_FULLCODE31_0[31] corresponds to column (7) – row (3).
- KBD_FULLCODE63_32[0] corresponds to column (0) – row (4) key,..., KBD_FULLCODE63_32[7] corresponds to column (7) – row (4).
- KBD_FULLCODE63_32[8] corresponds to column (0) – row (5) key,..., KBD_FULLCODE63_32[15] corresponds to column (7) – row (5).
- KBD_FULLCODE63_32[16] corresponds to column (0) – row (6) key,..., KBD_FULLCODE63_32[23] corresponds to column (7) – row (6).
- KBD_FULLCODE63_32[24] corresponds to column (0) – row (7) key,..., KBD_FULLCODE63_32[31] corresponds to column (7) – row (7).

NOTE: The keyboard fullcode registers are not updated in software mode.

NOTE: When using a smaller keyboard (for example, 5 × 5 or 4 × 4), the bits of the unused columns/rows are not used either.

26.4.8 Keyboard Controller Register Access

26.4.8.1 Write Registers Access

The keyboard module uses a posted-write scheme to update any internal registers. This means the write transaction is immediately acknowledged on the L4 interface, although the effective write operation occurs later due to a resynchronization in the functional clock domain. This has the advantage of not stalling the interconnect system or the CPU that requested the write transaction. For each functional register, a pending bit is provided that is set if there is a pending write access to this register. The pending bits are accessible in the keyboard pending write register (KBD_PENDING).

In this mode, it is mandatory that the CPU checks the pending bits before any write access in the functional registers. If a write is attempted to a register with a previous access pending, the previous access is discarded without notice (this can also lead to unexpected results).

A register read following a posted write (on the same register) may not read the previous write value if the write posted process is not complete. Software synchronization must be used to avoid noncoherent read.

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This posted period is defined as the interval between the posted write access request and the reset of the pending bit in the KBD_PENDING register, and can be quantified:

T (reset posted bit maximum) = 3 × Ticlk + 3 × Tfuncclk

The time it takes to accomplish the writing is:

T (write accomplish maximum) = 1 × Ticlk + 3 × Tfuncclk

where:

Ticlk is the L4 interface clock period, and Tfuncclk is the functional clock period.

26.4.8.2 Read Registers Access

The keyboard module uses a posted-read scheme for reading any internal register. The read transaction is immediately acknowledged on the L4 interface. The value of the functional register to be read must be previously synchronized. This has the advantage of not stalling the interconnect system or the CPU that requested the read transaction.

The posted-read scheme can be used only if Freq(KBD_FCLK) < Freq(KBD_ICLK)/4.

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26.5 Keyboard Controller Programming Guide

26.5.1 Keyboard Controller Low-Level Programming Models

This section describes the low-level hardware programming sequences for the configuration and use of the module.

26.5.1.1 Global Initialization

26.5.1.1.1 Surrounding Modules Global Initialization

This section identifies the requirements for initializing the surrounding modules when the keyboard module is to be used for the first time after a device reset. This initialization of surrounding modules is based on the integration and environment of the keyboard. For more information, see Section 26.2, *Keyboard Controller Environment,* and Section 26.3, *Keyboard Controller Integration*.

Table 26-12 describes the global initialization of surrounding modules.

Table 26-12. Global Initialization of Surrounding Modules

Surrounding Modules	Comments
PRCM	The module interface (WKUP_L4_ICLK2) and functional (WKUP_32K_FCLK) clocks must be enabled. See Section 3.10.2.1.2, *Clock Management Global Initialization*, in Chapter 3, *Power, Reset, and Clock Management*.
Cortex-A9 MPU INTC	Interrupt request KBD_CTL_IRQ from the keyboard must be unmasked. For more information, see Chapter 17, *Interrupt Controllers*.
Control module	The PAD CONFIG registers must configured in to map the keyboard interface signals on the device pins through the multiplexers (mux mode 0 must be switched on) to determine the signal directions and to enable the internal pullups of the GPIO cells for all the keyboard rows. For more information about configuration, see Section 18.4.8, *Pad Functional Multiplexing and Configuration*, and Section 25.2.1, *General-Purpose Interface as a Keyboard interface*.

26.5.1.1.2 Keyboard Controller Global Initialization

26.5.1.1.2.1 Main Sequence – Keyboard Controller Global Initialization

This procedure initializes the keyboard controller after a POR or software reset (see Table 26-13).

Table 26-13. Keyboard Controller Global Initialization

Step	Register/Bit Field/Programming Model	Value
Configure the parameters of the L4 interface and enable the clock activity.	KBD_SYSCONFIG	0x00000–
Configure the debouncing time of filtering the glitches on pressing or releasing key.	KBD_DEBOUNCINGTIME[5:0] DEBOUNCING_VALUE	0x–
Configure the duration of a key press to allow shortcut detection (desired value of the long-key interrupt or repeat mode value).	KBD_KEYLONGTIME[11:0] LONG_KEY_VALUE	0x–
Configure the period of the long inactivity on the keyboard (desired value of the time-out interrupt).	KBD_TIMEOUT[15:0] TIMEOUT_VALUE	0x–
Define the logical value of the column outputs (KEYPAD configuration) (logical 0 bit = active column-row).	KBD_COLUMNOUTPUTS[8:0] KBC_REG	0x–
Perform the functional configuration of the keyboard module and the prescale clock timer value.	KBD_CTRL	0x00000–
Clear the interrupt-status register.	KBD_IRQSTATUS	0x0000000F
Enable (0b1)/disable (0b0) certain keyboard events for generating an interrupt request.	KBD_IRQENABLE[2:0] IT_..._EN	0x–

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Table 26-13. Keyboard Controller Global Initialization (continued)

Step	Register/Bit Field/Programming Model	Value
Unmask (0b1)/mask (0b0) the expected source of wake-up event that generates a wake-up request.	KBD_WAKEUPENABLE[2:0] WUP_..._ENA	0x–

26.5.1.2 Operational Modes Configuration

26.5.1.2.1 Keyboard Controller in Hardware Decoding Mode (Default Mode)

26.5.1.2.1.1 Main Sequence – Keyboard Controller Hardware Mode

After reset, all available functional modes are disabled, except detect-event mode, which is always active. Table 26-14 describes the keyboard controller hardware mode.

Table 26-14. Keyboard Controller Hardware Mode

Step	Register/Bit Field/Programming Model	Value
Activate the internal keyboard controller sequencer by setting the bit.	KBD_CTRL[1] NSOFTWARE_MODE	0b1
Select the functional mode by setting its corresponding bit to 1.	KBD_CTRL[8:5]	0x–
Configure the duration of a key press to allow shortcut detection (desired value of the long-key interrupt or repeat mode value).	KBD_KEYLONGTIME[11:0] LONG_KEY_VALUE	0x–
Configure the period of the long inactivity on the keyboard (desired value of the time-out interrupt).	KBD_TIMEOUT[15:0] TIMEOUT_VALUE	0x–
Configure the debouncing time of filtering the glitches on pressing or releasing key.	KBD_DEBOUNCINGTIME[5:0] DEBOUNCING_VALUE	0x–
Clear the interrupt-status register.	KBD_IRQSTATUS	0x0000000F
Enable (by writing 1)/disable (by writing 0) certain keyboard event for generating an interrupt request	KBD_IRQENABLE[2:0] IT_..._EN	0x–
Unmask (0b1)/mask (0b0) the expected source of wake-up event that generates a wake-up request.	KBD_WAKEUPENABLE[2:0] WUP_..._ENA	0x–
Wait for the KBD_CTL_IRQ interrupt signal assertion.		
Read the interrupt-status register to determine which event caused the interrupt.	KBD_IRQSTATUS	
Read the KBD_FULLCODE17_0 to KBD_FULLCODE80_72 registers (or 8 × 8 keyboard-size-supporting KBD_FULLCODE31_0 and KBD_FULLCODE63_32 registers) to determine which key matrix combination was pressed.	KBD_FULLCODE17_0 [ROWi bits] (where i = 0 to 1) up to KBD_FULLCODE71_54 [ROWi bits] (where i = 6 to 7); KBD_FULLCODE80_72 [ROWi bits] (where i = 8); (or KBD_FULLCODE31_0[j] FULL_CODE_31_0 and KBD_FULLCODE63_32[k] FULL_CODE_63_32 bits (where j = 0 to 31, k = 32 to 63)	
Clear the corresponding bit(s) in the interrupt-status register by writing logical 1.	KBD_IRQSTATUS	0x1

NOTE: The long-key detection mode and the repeat mode cannot be used simultaneously, because they share the same interrupt status bit and are mutually exclusive. Software must ensure that only one of these modes at a time is selected.

NOTE: All interrupts are disabled on reset.

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NOTE: When two events occur successively before the first event is read, the second interrupt is generated when the first interrupt is cleared. When more than two events in a row occur, the KBD_IRQSTATUS[3] MISS_EVENT bit is set. Software must check this bit, which is not reflected on the KBD_CTL_IRQ line.

NOTE: The keyboard controller uses a posted-write scheme to update any internal register. Software must read the pending write status bits to ensure that the next write access is not discarded because of ongoing write synchronization. For more information, see Section 26.4.8.1, *Write Registers Access*.

26.5.1.2.2 Keyboard Controller Software Scanning Mode

26.5.1.2.2.1 Main Sequence – Keyboard Controller Software Mode

Table 26-15 describes the keyboard controller software mode.

Table 26-15. Keyboard Controller Software Mode

Step	Register/Bit Field/Programming Model	Value D
Deactivate the internal keyboard controller sequencer by clearing the bit.	KBD_CTRL[1] NSOFTWARE_MODE	0b0
Enable the event interrupt by setting the bit.	KBD_IRQENABLE[0] IT_EVENT_EN	0b1
Wait for the KBD_CTL_IRQ interrupt signal assertion. Begin the software scan when the interrupt signal is asserted:		
1) Disable all columns to drive a logical 0 on the kpd_col[8:0] output by writing 0xFF. (logical 1 bit = inactive column-row)	KBD_COLUMNOUTPUTS[8:0] KBC_REG	0xFF
2) Drive kpd_col(i) output, (where i = 0 to 8), to 0 to capture a pressed-key-event, at the corresponding row input.	KBD_COLUMNOUTPUTS[i] KBC_REG (where i = 0 to 8)	0b0
3) Read the KBR_LATCH bit field of the KBD_ROWINPUTS register to determine which is the pressed key. IF: KBR_LATCH k-bit = 0 , where k = 0 to 8 Then, the corresponding k-row is connected to the column being enabled.	KBD_ROWINPUTS[8:0] KBR_LATCH	
END IF		
Repeat steps 2) and 3) for all existing columns.	KBD_WAKEUPENABLE[2:0] WUP_..._ENA	0x–

NOTE: In software mode, during the manual keyboard scan, an interrupt is generated when a pressed key is detected.

26.5.1.2.3 Using the Timer

For information about programming the keyboard controller timer, see Section 26.4.6.2, *Keyboard Controller Timer*.

26.5.1.2.4 State-Machine Status Register

To see the state of the state-machine, see Section 26.4.6.3, *State-Machine Status*.

26.5.1.3 Keyboard Controller Events Servicing

Table 26-16 lists the keyboard controller event servicing.

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Table 26-16. Keyboard Controller Event Servicing

Step	Register/Bit Field/Programming Model	Value
Clear all eventual previous indications of treated interrupts; write the IRQSTATUS register:	KBD_IRQSTATUS	0x0000000F
Enable the desired sources of interrupt by writing in:	KBD_IRQENABLE	0x0000000–
Unmask (enable) the desired sources of interrupt by writing logical 1 in the desired bit fields.	KBD_WAKEUPENABLE	0x0000000–
When event occurs:		
Read the status register.	KBD_IRQSTATUS	
IF: KBD_IRQSTATUS[3] MISS_EVENT = 1	Start the interrupt handler for missed event.	
ELSIF: KBD_IRQSTATUS[2] IT_TIMEOUT = 1	Start the interrupt handler for timeout event.	
ELSIF: KBD_IRQSTATUS[1] IT_LONG_KEY = 1	Start the interrupt handler for long key pressed event.	
ELSIF: KBD_IRQSTATUS[0] IT_EVENT = 1	Start the interrupt handler for pressed key event.	
ENDIF		
Wait for the execution of the corresponding interrupt handler.	Interrupt controller of the MPU	
Clear the corresponding IRQ status register bits by writing 1 there.	KBD_IRQSTATUS	0x0000000–
Disable the corresponding sources of interrupt if needed by writing 0 at the corresponding bit fields.	KBD_IRQENABLE or KBD_WAKEUPENABLE	0x0000000-

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26.6 Keyboard Controller Register Manual

26.6.1 Keyboard Controller Instance Summary

Table 26-17 summarizes the keyboard controller instances.

Table 26-17. Keyboard Controller Instance Summary

Module Name	Base Address	Size
Keyboard controller	0x4A31 C000	4KB

26.6.2 Keyboard Controller Registers

26.6.2.1 Keyboard Controller Register Summary

Table 26-18 summarizes the keyboard controller register mapping.

Table 26-18. Keyboard Controller Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	Keyboard Controller L4_WKUP Base Address
KBD_REVISION	R	32	0x0000 0000	0x4A31 C000
KBD_SYSCONFIG	RW	32	0x0000 0010	0x4A31 C010
KBD_SYSSTATUS	R	32	0x0000 0014	0x4A31 C014
KBD_IRQSTATUS	RW	32	0x0000 0018	0x4A31 C018
KBD_IRQENABLE	RW	32	0x0000 001C	0x4A31 C01C
KBD_WAKEUPENABLE	RW	32	0x0000 0020	0x4A31 C020
KBD_PENDING	R	32	0x0000 0024	0x4A31 C024
KBD_CTRL	RW	32	0x0000 0028	0x4A31 C028
KBD_DEBOUNCINGTIME	RW	32	0x0000 002C	0x4A31 C02C
KBD_KEYLONGTIME	RW	32	0x0000 0030	0x4A31 C030
KBD_TIMEOUT	RW	32	0x0000 0034	0x4A31 C034
KBD_STATEMACHINE	R	32	0x0000 0038	0x4A31 C038
KBD_ROWINPUTS	R	32	0x0000 003C	0x4A31 C03C
KBD_COLUMNOUTPUTS	RW	32	0x0000 0040	0x4A31 C040
KBD_FULLCODE31_0	R	32	0x0000 0044	0x4A31 C044
KBD_FULLCODE63_32	R	32	0x0000 0048	0x4A31 C048
KBD_FULLCODE17_0	R	32	0x0000 004C	0x4A31 C04C
KBD_FULLCODE35_18	R	32	0x0000 0050	0x4A31 C050
KBD_FULLCODE53_36	R	32	0x0000 0054	0x4A31 C054
KBD_FULLCODE71_54	R	32	0x0000 0058	0x4A31 C058
KBD_FULLCODE80_72	R	32	0x0000 005C	0x4A31 C05C

26.6.2.2 Keyboard Controller Register Description

through describe the individual keyboard module registers.

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Table 26-19. KBD_REVISION

Address Offset	0x0000 0000		
Physical Address	0x4A31 C000	**Instance**	Keyboard controller
Description	This register contains the IP revision code.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP revision	R	0x--------[1]

(1) TI internal data

Table 26-20. Register Call Summary for Register KBD_REVISION

Keyboard Controller Register Manual

- Keyboard Controller Register Summary: [0]

Table 26-21. KBD_SYSCONFIG

Address Offset	0x0000 0010		
Physical Address	0x4A31 C010	**Instance**	Keyboard controller
Description	This register controls the various parameters of the L4 interface.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						CLOCKACTIVITY		RESERVED	EMUFREE	IDLEMODE			ENAWAKEUP	SOFTRESET	AUTOGATING

Bits	Field Name	Description	Type	Reset
31:10	RESERVED	Reads return 0.	RW	0x000000
9:8	CLOCKACTIVITY	Clock(s) activity during wake-up mode period. 0x0: Functional clock can be switched off; L4 -nterface clock can be switched-off. 0x1: Functional clock can be switched off; L4 interface clock is maintained during wake-up period. 0x2: Functional clock is maintained during wake-up period; L4 interface clock can be switched off. 0x3: Functional clock is maintained during wake-up period; L4 interface clock is maintained during wake-up period.	RW	0x0
7:6	RESERVED	Write 0s for future compatibility. Reads return 0.	RW	0x0
5	EMUFREE	Emulation mode 0x0: The keyboard module is frozen in emulation mode (PINSUSPENDN signal active). 0x1: The keyboard module runs free, regardless of PINSUSPENDN value.	RW	0

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Bits	Field Name	Description	Type	Reset
4:3	IDLEMODE	Power management, req/ack control 0x0: Force-idle. An idle request is acknowledged unconditionally. 0x1: No-idle. An idle request is never acknowledged. 0x2: Smart-idle. Acknowledgment to an idle request is given based on the internal activity of the module. 0x3: Reserved. Do not use.	RW	0x0
2	ENAWAKEUP	Wake-up feature global control 0x0: No wake-up line assertion in idle mode 0x1: Wake-up line assertion enabled in smart-idle mode	RW	0
1	SOFTRESET	Software reset. This bit is automatically reset by the hardware. During reads, it always return 0. 0x0: Normal mode 0x1: The module is reset.	RW	0
0	AUTOGATING	Internal L4 interface clock gating strategy 0x0: L4 interface clock is free-running. 0x1: Automatic L4 interface clock gating strategy is applied, based on the L4 interface activity.	RW	1

Table 26-22. Register Call Summary for Register KBD_SYSCONFIG

Keyboard Controller Functional Description • Keyboard Controller Software Reset: [0] [1] • Keyboard Controller Power Management: [2] [3] [4] [5] [6]
Keyboard Controller Programming Guide • Keyboard Controller Global Initialization: [7]
Keyboard Controller Register Manual • Keyboard Controller Register Summary: [8]

Table 26-23. KBD_SYSSTATUS

Address Offset	0x0000 0014		
Physical Address	0x4A31 C014	**Instance**	Keyboard controller
Description	This register controls optional features specific to the timer function.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															RESETDONE

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reads return 0. Reserved for L4 interface socket status information.	R	0x0000 0000
0	RESETDONE	Internal reset monitoring Read 0x0: Internal module reset is ongoing. Read 0x1: Reset completed	R	0

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Table 26-24. Register Call Summary for Register KBD_SYSSTATUS

Keyboard Controller Functional Description • Keyboard Controller Software Reset: [0]
Keyboard Controller Register Manual • Keyboard Controller Register Summary: [1]

Table 26-25. KBD_IRQSTATUS

Address Offset	0x0000 0018		
Physical Address	0x4A31 C018	**Instance**	Keyboard controller
Description	The keyboard interrupt-status register is used to determine which of the keyboard events requested an interrupt.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												MISS_EVENT	IT_TIMEOUT	IT_LONG_KEY	IT_EVENT

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reads return 0.	RW	0x0000000
3	MISS_EVENT	Indicates when a miss event occurs. 0x0: No miss event 0x1: A miss event occurs.	RW	0
2	IT_TIMEOUT	Indicates when a time-out event is detected. 0x0: No time-out event 0x1: A time-out event occurs.	RW	0
1	IT_LONG_KEY	Indicates when a long-key event is detected. 0x0: No long-key event 0x1: A long-key event occurs.	RW	0
0	IT_EVENT	Indicates when an event is detected. 0x0: No event 0x1: An event occurs.	RW	0

Table 26-26. Register Call Summary for Register KBD_IRQSTATUS

Keyboard Controller Functional Description • Keyboard Controller Interrupt Requests: [0] [1] [2] [3] • Functional Modes: [4] • Interrupt-Generation Scheme: [5] [6] [7] [8] [9] [10] • Keyboard Buffer and Missed Events (Overrun Feature): [11] [12]
Keyboard Controller Programming Guide • Keyboard Controller Global Initialization: [13] • Keyboard Controller in Hardware Decoding Mode (Default Mode): [14] [15] [16] [17] • Keyboard Controller Events Servicing: [18] [19] [20] [21] [22] [23] [24]
Keyboard Controller Register Manual • Keyboard Controller Register Summary: [25]

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Table 26-27. KBD_IRQENABLE

Address Offset	0x0000 001C		
Physical Address	0x4A31 C01C	**Instance**	Keyboard controller
Description	The keyboard interrupt-enable register lets the user enable certain keyboard event for generating an interrupt request.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													IT_TIMEOUT_EN	IT_LONG_KEY_EN	IT_EVENT_EN

Bits	Field Name	Description	Type	Reset
31:3	RESERVED	Reads return 0	RW	0x0000 0000
2	IT_TIMEOUT_EN	Time-out interrupt enable 0x0: Time-out interrupt disabled 0x1: Time-out interrupt enabled	RW	0
1	IT_LONG_KEY_EN	Long-key interrupt enable 0x0: Long-key interrupt disabled 0x1: Long-key interrupt enabled	RW	0
0	IT_EVENT_EN	Enable event interrupt 0x0: Event interrupt disabled 0x1: Event interrupt enabled	RW	0

Table 26-28. Register Call Summary for Register KBD_IRQENABLE

Keyboard Controller Functional Description
- Keyboard Controller Interrupt Requests: [0] [1] [2]
- Functional Modes: [3]
- Interrupt-Generation Scheme: [4] [5]

Keyboard Controller Programming Guide
- Keyboard Controller Global Initialization: [6]
- Keyboard Controller in Hardware Decoding Mode (Default Mode): [7]
- Keyboard Controller Software Scanning Mode: [8]
- Keyboard Controller Events Servicing: [9] [10]

Keyboard Controller Register Manual
- Keyboard Controller Register Summary: [11]

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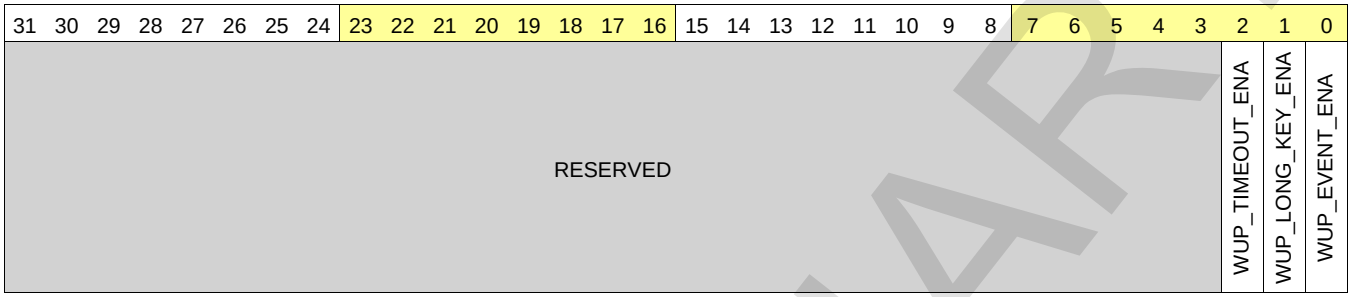
Table 26-29. KBD_WAKEUPENABLE

Address Offset	0x0000 0020		
Physical Address	0x4A31 C020	**Instance**	Keyboard controller
Description	The keyboard wake-up enable register lets the user mask the expected source of wake-up event that generates a wake-up request.		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:3	RESERVED	Reads return 0.	RW	0x0000 0000
2	WUP_TIMEOUT_ENA	Time-out wake-up enable 0x0: Time-out wake-up generation disabled 0x1: Time-out wake-up generation enabled	RW	0
1	WUP_LONG_KEY_ENA	Long-key wake-up enable 0x0: Long-key wake-up generation disabled 0x1: Long-key wake-up generation enabled	RW	0
0	WUP_EVENT_ENA	Event wake-up enable 0x0: Event wake-up generation disabled 0x1: Event wake-up generation enabled	RW	0

Table 26-30. Register Call Summary for Register KBD_WAKEUPENABLE

Keyboard Controller Functional Description
- Keyboard Controller Power Management: [0]

Keyboard Controller Programming Guide
- Keyboard Controller Global Initialization: [1]
- Keyboard Controller in Hardware Decoding Mode (Default Mode): [2]
- Keyboard Controller Software Scanning Mode: [3]
- Keyboard Controller Events Servicing: [4] [5]

Keyboard Controller Register Manual
- Keyboard Controller Register Summary: [6]

Table 26-31. KBD_PENDING

Address Offset	0x0000 0024		
Physical Address	0x4A31 C024	**Instance**	Keyboard controller
Description	Software must read the pending write bits to ensure that following write access is not discarded due to ongoing write synchronization process.		
Type	R		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												PEND_TIMEOUT	PEND_LONG_KEY	PEND_DEBOUNCING	PEND_CTRL

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reads return 0.	R	0x0000000
3	PEND_TIMEOUT	Write-pending bit for KBD_TIMEOUT register Read 0x0: No write pending to the KBD_TIMEOUT register Read 0x1: A write is pending to the KBD_TIMEOUT register	R	0
2	PEND_LONG_KEY	Write-pending bit for KBD_KEYLONGTIME register Read 0x0: No write pending to the KBD_KEYLONGTIME register. Read 0x1: A write is pending to the KBD_KEYLONGTIME register	R	0
1	PEND_DEBOUNCING	Write-pending bit for KBD_DEBOUNCINGTIME register Read 0x0: No write pending to the KBD_DEBOUNCINGTIME register Read 0x1: A write is pending to the KBD_DEBOUNCINGTIME register	R	0
0	PEND_CTRL	Write pending bit for KBD_CTRL register Read 0x0: No write pending to the KBD_CTRL register Read 0x1: A write is pending to the KBD_CTRL register	R	0

Table 26-32. Register Call Summary for Register KBD_PENDING

Keyboard Controller Functional Description • Write Registers Access: [0] [1]
Keyboard Controller Register Manual • Keyboard Controller Register Summary: [2]

Table 26-33. KBD_CTRL

Address Offset	0x0000 0028		
Physical Address	0x4A31 C028	**Instance**	Keyboard controller
Description	This register sets the functional configuration of the module.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								REPEAT_MODE	TIMEOUT_LONG_KEY	TIMEOUT_EMPTY	LONG_KEY	PTV			NSOFTWARE_MODE	RESERVED

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Bits	Field Name	Description	Type	Reset
31:9	RESERVED	Reads return 0.	RW	0x000000
8	REPEAT_MODE	Repeat mode enable 0x0: Repeat mode detection disabled 0x1: Repeat mode detection enabled	RW	0
7	TIMEOUT_LONG_KEY	Time-out long key mode enable 0x0: Time-out long key mode disabled 0x1: Time-out long key mode enabled	RW	0
6	TIMEOUT_EMPTY	Time-out empty mode enable 0x0: Time-out long key mode disabled 0x1: Time-out long key mode enabled	RW	0
5	LONG_KEY	Long-key mode enable. 0x0: Long-key mode disabled 0x1: Long-key mode enabled	RW	0
4:2	PTV	Prescale clock timer value	RW	0x7
1	NSOFTWARE_MODE	Select hardware or software mode for key decoding. 0x0: Enable software mode. 0x1: Enable hardware decoding using internal sequencer.	RW	1
0	RESERVED	Reads return 0.	RW	0

Table 26-34. Register Call Summary for Register KBD_CTRL

Keyboard Controller Functional Description • Keyboard Controller Software Mode: [0] • Functional Modes: [1] [2] [3] [4] [5] [6] [7] • Keyboard Controller Timer: [8] [9] [10] [11] [12]
Keyboard Controller Programming Guide • Keyboard Controller Global Initialization: [13] • Keyboard Controller in Hardware Decoding Mode (Default Mode): [14] [15] • Keyboard Controller Software Scanning Mode: [16]
Keyboard Controller Register Manual • Keyboard Controller Register Summary: [17] • Keyboard Controller Register Description: [18] [19] [20]

Table 26-35. KBD_DEBOUNCINGTIME

Address Offset	0x0000 002C		
Physical Address	0x4A31 C02C	**Instance**	Keyboard controller
Description	This register is used to filter glitches on the press key or release key.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								DEBOUNCING_VALUE							

Bits	Field Name	Description	Type	Reset
31:6	RESERVED	Reads return 0.	RW	0x0000000
5:0	DEBOUNCING_VALUE	This value corresponds to the desired value of debouncing time.	RW	0x00

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Table 26-36. Register Call Summary for Register KBD_DEBOUNCINGTIME

Keyboard Controller Functional Description • Keyboard Controller Timer: [0] [1] [2] [3] [4] [5]
Keyboard Controller Programming Guide • Keyboard Controller Global Initialization: [6] • Keyboard Controller in Hardware Decoding Mode (Default Mode): [7]
Keyboard Controller Register Manual • Keyboard Controller Register Summary: [8] • Keyboard Controller Register Description: [9] [10] [11]

Table 26-37. KBD_KEYLONGTIME

Address Offset	0x0000 0030		
Physical Address	0x4A31 C030	**Instance**	Keyboard controller
Description	This register is used to measure duration of a key press to allow shortcut detection.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																LONG_KEY_VALUE															

Bits	Field Name	Description	Type	Reset
31:12	RESERVED	Reads return 0.	RW	0x00000
11:0	LONG_KEY_VALUE	This value corresponds to the desired value of the long-key interrupt or repeat mode value.	RW	0x000

Table 26-38. Register Call Summary for Register KBD_KEYLONGTIME

Keyboard Controller Functional Description • Keyboard Controller Timer: [0] [1] [2] [3] [4] [5] [6] [7] [8]
Keyboard Controller Programming Guide • Keyboard Controller Global Initialization: [9] • Keyboard Controller in Hardware Decoding Mode (Default Mode): [10]
Keyboard Controller Register Manual • Keyboard Controller Register Summary: [11] • Keyboard Controller Register Description: [12] [13] [14]

Table 26-39. KBD_TIMEOUT

Address Offset	0x0000 0034		
Physical Address	0x4A31 C034	**Instance**	Keyboard controller
Description	This register is used to detect a long inactivity on the keyboard.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																TIMEOUT_VALUE															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reads return 0.	RW	0x0000
15:0	TIMEOUT_VALUE	This value corresponds to the desired value of the time-out interrupt.	RW	0x0000

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Table 26-40. Register Call Summary for Register KBD_TIMEOUT

Keyboard Controller Functional Description • Keyboard Controller Timer: [0] [1] [2] [3] [4] [5] [6]
Keyboard Controller Programming Guide • Keyboard Controller Global Initialization: [7] • Keyboard Controller in Hardware Decoding Mode (Default Mode): [8]
Keyboard Controller Register Manual • Keyboard Controller Register Summary: [9] • Keyboard Controller Register Description: [10] [11] [12]

Table 26-41. KBD_STATEMACHINE

Address Offset	0x0000 0038		
Physical Address	0x4A31 C038	**Instance**	Keyboard controller
Description	This register indicates the state of the sequencer.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								STATE_MACHINE							

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reads return 0.	R	0x0000000
3:0	STATE_MACHINE	The state of internal state machine. See Section 26.5.1.2.4, *State-Machine Status Register,* for details.	R	0x0

Table 26-42. Register Call Summary for Register KBD_STATEMACHINE

Keyboard Controller Functional Description • State-Machine Status: [0]
Keyboard Controller Register Manual • Keyboard Controller Register Summary: [1]

Table 26-43. KBD_ROWINPUTS

Address Offset	0x0000 003C		
Physical Address	0x4A31 C03C	**Instance**	Keyboard controller
Description	This register stores the value of the row inputs.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								KBR_LATCH							

Bits	Field Name	Description	Type	Reset
31:9	RESERVED	Reads return 0.	R	0x000000
8:0	KBR_LATCH	The value of the rows input.	R	0x00

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Table 26-44. Register Call Summary for Register KBD_ROWINPUTS

Keyboard Controller Functional Description • Keyboard Controller Software Mode: [0] [1]
Keyboard Controller Programming Guide • Keyboard Controller Software Scanning Mode: [2] [3]
Keyboard Controller Register Manual • Keyboard Controller Register Summary: [4]

Table 26-45. KBD_COLUMNOUTPUTS

Address Offset	0x0000 0040		
Physical Address	0x4A31 C040	**Instance**	Keyboard controller
Description	This register holds the value of the columns output.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							KBC_REG								

Bits	Field Name	Description	Type	Reset
31:9	RESERVED	Reads return 0.	RW	0x000000
8:0	KBC_REG	The value of the columns output	RW	0x00

Table 26-46. Register Call Summary for Register KBD_COLUMNOUTPUTS

Keyboard Controller Functional Description • Keyboard Controller Block Diagram: [0] • Keyboard Controller Software Mode: [1]
Keyboard Controller Programming Guide • Keyboard Controller Global Initialization: [2] • Keyboard Controller Software Scanning Mode: [3] [4]
Keyboard Controller Register Manual • Keyboard Controller Register Summary: [5]

Table 26-47. KBD_FULLCODE31_0

Address Offset	0x0000 0044		
Physical Address	0x4A31 C044	**Instance**	Keyboard controller
Description	The KBD_FULLCODE31_0 register codes the row 0, row 1, row 2, and row 3.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FULL_CODE_31_0																															

Bits	Field Name	Description	Type	Reset
31:0	FULL_CODE_31_0	A bit set to 1 indicates that the corresponding key is pressed.	R	0x0000 0000

Table 26-48. Register Call Summary for Register KBD_FULLCODE31_0

Keyboard Controller Functional Description • Keyboard Controller Key Coding Registers: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10]
Keyboard Controller Programming Guide • Keyboard Controller in Hardware Decoding Mode (Default Mode): [11] [12]

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Table 26-48. Register Call Summary for Register KBD_FULLCODE31_0 (continued)

Keyboard Controller Register Manual • Keyboard Controller Register Summary: [13] • Keyboard Controller Register Description: [14]

Table 26-49. KBD_FULLCODE63_32

Address Offset	0x0000 0048		
Physical Address	0x4A31 C048	**Instance**	Keyboard controller
Description	The KBD_FULLCODE63_32 register codes rows 4, 5, 6, and 7.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FULL_CODE_63_32																															

Bits	Field Name	Description	Type	Reset
31:0	FULL_CODE_63_32	A bit set to 1 indicates that the corresponding key is pressed.	R	0x0000 0000

Table 26-50. Register Call Summary for Register KBD_FULLCODE63_32

Keyboard Controller Functional Description • Keyboard Controller Key Coding Registers: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10]
Keyboard Controller Programming Guide • Keyboard Controller in Hardware Decoding Mode (Default Mode): [11] [12]
Keyboard Controller Register Manual • Keyboard Controller Register Summary: [13] • Keyboard Controller Register Description: [14]

Table 26-51. KBD_FULLCODE17_0

Address Offset	0x0000 004C		
Physical Address	0x4A31 C04C	**Instance**	Keyboard controller
Description	The KBD_FULLCODE17_0 register codes row 0 and row 1. Row 0 is coded between bit 0 and 8; row 1 is coded between bit 24 and 16.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								ROW1								RESERVED								ROW0							

Bits	Field Name	Description	Type	Reset
31:25	RESERVED	Reserved. Read returns 0.	RO	0x00
24:16	ROW1	A bit set to 1 indicates that the corresponding key is pressed.	R	0x000
15:9	RESERVED	Reserved	R	0x00
8:0	ROW0	A bit set to 1 indicates that the corresponding key is pressed.	R	0x000

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Table 26-52. Register Call Summary for Register KBD_FULLCODE17_0

Keyboard Controller Functional Description • Keyboard Controller Key Coding Registers: [0] [1] [2]
Keyboard Controller Programming Guide • Keyboard Controller in Hardware Decoding Mode (Default Mode): [3] [4]
Keyboard Controller Register Manual • Keyboard Controller Register Summary: [5] • Keyboard Controller Register Description: [6]

Table 26-53. KBD_FULLCODE35_18

Address Offset	0x0000 0050		
Physical Address	0x4A31 C050	**Instance**	Keyboard controller
Description	The KBD_FULLCODE35_18 register codes row 2 and row 3. Row 2 is coded between bit 0 and 8; row 3 is coded between bit 24 and 16		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								ROW3								RESERVED								ROW2							

Bits	Field Name	Description	Type	Reset
31:25	RESERVED	Reserved. Read returns 0.	RO	0x00
24:16	ROW3	A bit set to 1 indicates that the corresponding key is pressed.	R	0x000
15:9	RESERVED	Reserved	R	0x00
8:0	ROW2	A bit set to 1 indicates that the corresponding key is pressed.	R	0x000

Table 26-54. Register Call Summary for Register KBD_FULLCODE35_18

Keyboard Controller Functional Description • Keyboard Controller Key Coding Registers: [0]
Keyboard Controller Register Manual • Keyboard Controller Register Summary: [1] • Keyboard Controller Register Description: [2]

Table 26-55. KBD_FULLCODE53_36

Address Offset	0x0000 0054		
Physical Address	0x4A31 C054	**Instance**	Keyboard controller
Description	The KBD_FULLCODE53_36 register codes row 4 and row 5. Row 4 is coded between bit 0 and 8; row 5 is coded between bit 24 and 16.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								ROW5								RESERVED								ROW4							

Bits	Field Name	Description	Type	Reset
31:25	RESERVED	Reserved. Read returns 0.	RO	0x00
24:16	ROW5	A bit set to 1 indicates that the corresponding key is pressed.	R	0x000
15:9	RESERVED	Reserved	R	0x00
8:0	ROW4	A bit set to 1 indicates that the corresponding key is pressed.	R	0x000

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Table 26-56. Register Call Summary for Register KBD_FULLCODE53_36

Keyboard Controller Functional Description • Keyboard Controller Key Coding Registers: [0]
Keyboard Controller Register Manual • Keyboard Controller Register Summary: [1] • Keyboard Controller Register Description: [2]

Table 26-57. KBD_FULLCODE71_54

Address Offset	0x0000 0058		
Physical Address	0x4A31 C058	**Instance**	Keyboard controller
Description	The KBD_FULLCODE71_54 register codes row 6 and row 7. Row 6 is coded between bit 0 and 8; row 7 is coded between bit 24 and 16.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								ROW7								RESERVED								ROW6							

Bits	Field Name	Description	Type	Reset
31:25	RESERVED	Reserved. Read returns 0.	RO	0x00
24:16	ROW7	A bit set to 1 indicates that the corresponding key is pressed.	R	0x000
15:9	RESERVED	Reserved	R	0x00
8:0	ROW6	A bit set to 1 indicates that the corresponding key is pressed.	R	0x000

Table 26-58. Register Call Summary for Register KBD_FULLCODE71_54

Keyboard Controller Functional Description • Keyboard Controller Key Coding Registers: [0] [1]
Keyboard Controller Programming Guide • Keyboard Controller in Hardware Decoding Mode (Default Mode): [2]
Keyboard Controller Register Manual • Keyboard Controller Register Summary: [3] • Keyboard Controller Register Description: [4]

Table 26-59. KBD_FULLCODE80_72

Address Offset	0x0000 005C		
Physical Address	0x4A31 C05C	**Instance**	Keyboard controller
Description	The KBD_FULLCODE80_72 register codes row 8. Row 8 is coded between bit 0 and 8.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								ROW8							

Bits	Field Name	Description	Type	Reset
31: 9	RESERVED	Reserved. Read returns 0.	RO	0x000000
8:0	ROW8	A bit set to 1 indicates that the corresponding key is pressed.	R	0x000

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Table 26-60. Register Call Summary for Register KBD_FULLCODE80_72

Keyboard Controller Functional Description • Keyboard Controller Key Coding Registers: [0] [1] [2] [3] [4]
Keyboard Controller Programming Guide • Keyboard Controller in Hardware Decoding Mode (Default Mode): [5] [6]
Keyboard Controller Register Manual • Keyboard Controller Register Summary: [7] • Keyboard Controller Register Description: [8]

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Initialization

This chapter introduces the steps in the general-purpose (GP) device initialization.

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27.4 Device Initialization by ROM Code **5488**
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27.1 Initialization Overview

This chapter provides an overview of the requirements for initializing the device from power on to OS/application execution. It provides an overview of the overall initialization process, including hardware- and software-related steps, a general overview of the ROM code operational requirements, and the behavior expectations.

27.1.1 Terminology

- **Bootstrap:** Initial software launched by the ROM code during the memory booting phase
- **Configuration Header (CH):** Optional structure, that precedes the initial software and allows the redefinition of the ROM code default settings
- **Downloaded software:** Initial software downloaded into the internal static RAM (SRAM) by the ROM code during the peripheral booting phase
- **eFuse:** A one-time programmable memory location usually set at the factory
- **Flash loader:** Downloaded software launched by the ROM code in preflashing. It also programs an image in external memories.
- **GP device:** General-purpose device
- **Initial software:** Software executed by any of the ROM code mechanisms (memory booting or peripheral booting). Initial software is a generic term for bootstrap and downloaded software.
- **Memory booting:** ROM code mechanism that consists of executing initial software from external memory
- **Master CPU:** The ARM® Cortex™-A9 MPCore™ CPU for which CPU-ID is 0. It configures the multicore platform and starts the ROM code to ensure device booting from a mass storage memory (memory booting) or a peripheral interface (peripheral booting).
- **Peripheral booting:** ROM code mechanism that consists of polling selected interfaces, downloading, and executing initial software (in this case, downloaded software) in the internal RAM
- **Permanent booting device:** Memory device containing, by default, the image to be executed during the booting sequence. It is the default memory booting device. The permanent booting device is used after warm reset if no software booting configuration is programmed.
- **Preflashing:** A specific case of peripheral booting where the ROM code mechanism is used to program the external flash memory
- **ROM Code:** The on-chip software in OMAP™ ROM that implements booting
- **Save-And-Restore (SAR RAM) memory:** On-chip RAM memory that is not cleared after warm resets or wakeups from low-power modes
- **Slave CPU:** The ARM Cortex-A9 MPCore CPU for which CPU-ID is 1. It is brought to the wait-for-event (WFE) state by the ROM code, waiting to be woken up by the master CPU.
- **Software booting configuration:** A logical structure stored in the SAR memory that allows the redefinition of the ROM code default settings when booting after a warm reset

27.1.2 Initialization Process

Figure 27-1 is an overview of the initialization process and its steps:

- **Preinitialization:** Power, clock, and control connections must be present, and the boot configuration pins must be held at the desired logical levels.
- **Power, clock, reset ramp sequence:** Specific sequence that is applied by the power-management chip
- **ROM code:** Responsible for finding/downloading and for executing the initial software by using the master CPU
- **Initial software:** Software that prepares and passes control to application software or to the high-level operating system (HLOS)
- **Symmetric multiprocessing (SMP)-capable HLOS** or application (primarily for diagnostics)

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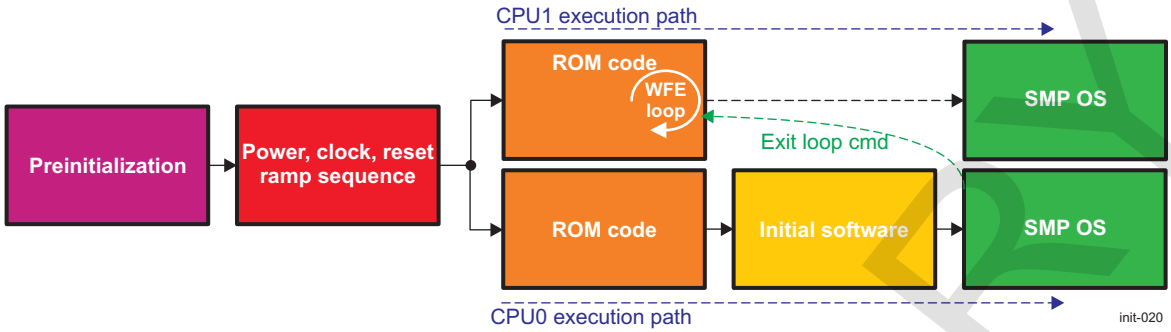
Figure 27-1. Initialization Process



The first two steps in the initialization process are hardware-oriented; however, they require understanding of the process of configuring these system interface pins (balls on the device), which have software-configurable functionality. This configuration is an essential part of the chip configuration and is application-dependent. This chapter discusses these pins and the associated configuration registers that are vital to the correct initialization of the device.

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27.2 Preinitialization

To accomplish a successful boot-up operation with a general-purpose (GP) device, certain hardware configuration settings must be in place. Clock, reset, and power connections, as well as pins involved in setting the boot memory space for the master CPU, must be connected and driven correctly to successful initialize the device. The following sections describe the specific requirements for the preinitialization stage.

27.2.1 Power Requirements

The device can be supplied by an external power-management integrated circuit (IC). TI provides a global solution with the device connected to the TWL6030 power-management/TWL6040 audio codec IC.

Figure 27-2 shows the power connections between the OMAP device and the TWL6030 power IC.

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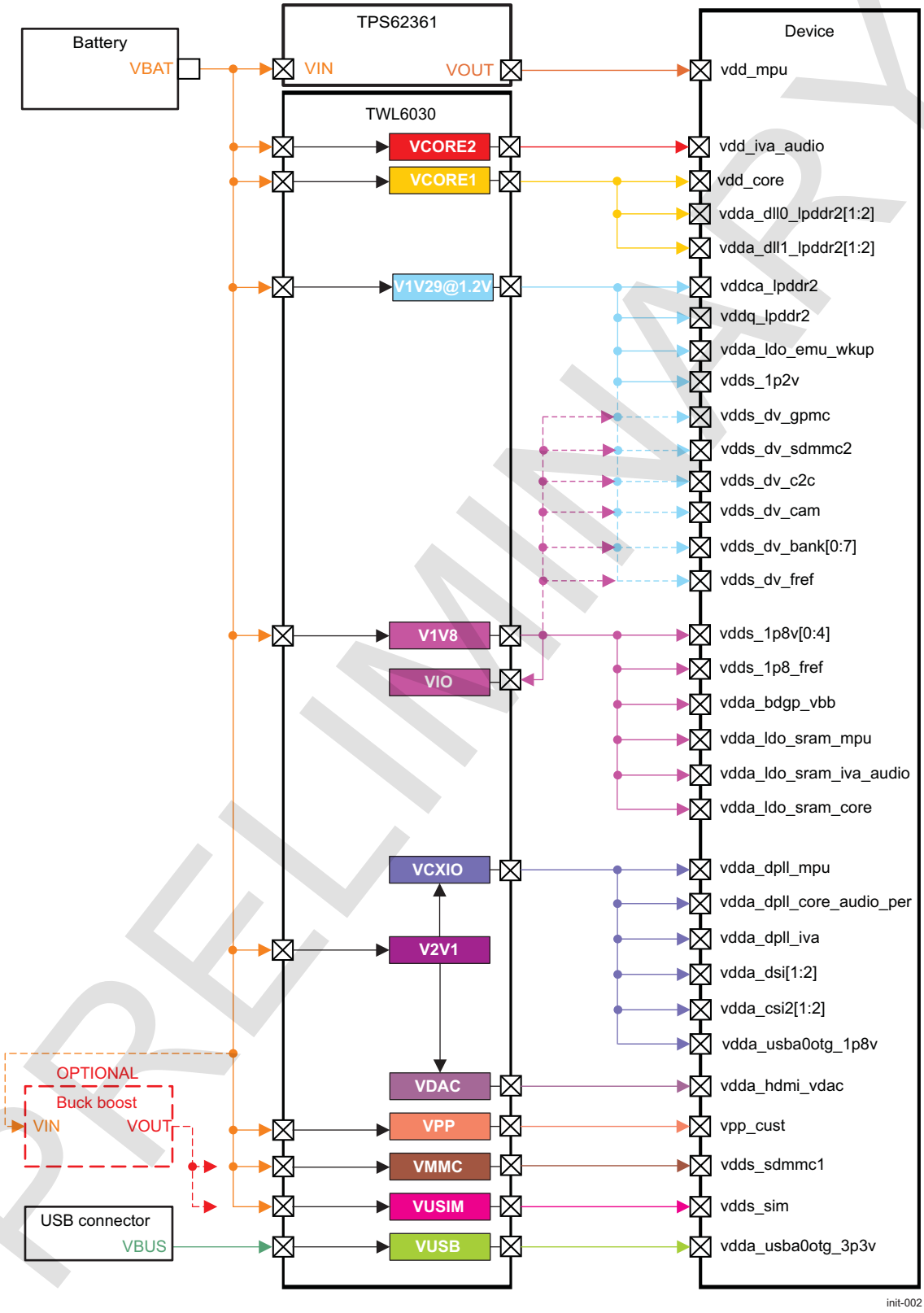
Figure 27-2. Power Supply Connections



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NOTE: Figure 27-2 is an example of power connections between the device and the TWL6030. These connections depend on the actual application.

Table 27-1 describes the device power balls.

Table 27-1. OMAP Power Balls [1]

Voltage Ball Name	Domain
vdd_core	• Core
vdd_mpu	• Dual MPU core • NEON
vdd_iva_audio	• IVA HD • DSP • Audio back-end (ABE) • Wake-up logic
vdda_ldo_emu_wkup	• Wakeup • Emulation subsystem
vddq_lpddr2	LPDDR2 DQ I/Os (OMAP side only)
vddca_lpddr2	LPDDR2 CA I/Os (OMAP side only)
vddq_vref_lpddr21 vddq_vref_lpddr21	Supplies VDDQ_VREF generator
vddca_vref_lpddr21 vddca_vref_lpddr21	Supplies VDDCA_VREF generator
vdda_dll0_lpddr21 vdda_dll0_lpddr22 vdda_dll1_lpddr21 vdda_dll1_lpddr22	• LPDDR21 DLL • LPDDR22 DLL
vdds_1p8v[0:4]	1.8-V I/O: • HDMI CEC/DDC/HPD • I2C2 and HDQ • Sys • JTAG • DPM
vdds_1p2v	1.2-V I/O: USB3/4_HSIC
vdda_dsi1	DSI1 I/Os + ADPLL
vdda_dsi2	DSI2 I/Os + ADPLL
vdda_csi21	CSI21 I/Os
vdda_csi22	CSI22 I/Os
vdda_hdmi_vdac	HDMI PHY + ADPLL or TV-out video DAC
vdda_usba_otg_1p8v	USB PHY common module + ADPLL
vdda_usba0_otg_3p3v	USB PHY core module
vpp_cust	Customer eFuse program module
vdds_sim	SIM I/Os
vdds_sdmmc1	SD/MMC1 I/Os
vdda_dpll_iva_per	• ADPLL PER and ADPLL IVA
vdda_dpll_core_audio	• ADPLL CORE and ADPLL ABE
vdda_dpll_mpu	• DPLL MPU
vdda_ldo_sram_mpu	Internal MPU SRAM LDO
vdda_ldo_sram_iva_audio	Internal IVA and ABE SRAM LDOs
vdda_ldo_sram_core	Internal Core SRAM LDO

[1] The package-on-package (POP) device provides feedthroughs from the bottom of the package to the POP interface. Among these feedthroughs (FEEDTHROUGH balls), several provide power to the top memory device. The correct power supply to the feedthroughs must be provided based on memory requirements.

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Table 27-1. OMAP Power Balls [(1)] (continued)

Voltage Ball Name	Domain
vdda_bdgp_vbb	Bandgap and Bodybias LDO
vdds_dv_gpmc	GPMC I/Os
vdds_dv_sdmmc2	SD/MMC2 I/Os
vdds_dv_cam	Camera I/Os: • fref_clk1_out/fref_clk2_out • strobe/shutter/global reset • I2C3
vdds_dv_bank0	Bank 0 of I/Os: usb3_ulpitll, HSI, McBSP4/3 I/Os (modem connectivity)
vdds_dv_bank1	Bank 1 of I/Os: MCBSP1/2, UART2 I/Os (typically used for BT/GPS connectivity)
vdds_dv_bank2	Bank 2 of I/Os: MCPDM, DMIC, I2C1, SmartReflex™ I/Os (TWL6030/TWL6040 connectivity)
vdds_dv_bank3	Bank 3 of I/Os: MCSPI1 I/Os (low bandwidth peripheral connectivity)
vdds_dv_bank4	Bank 4 of I/Os: SDMMC5 I/Os
vdds_dv_bank5	Bank 5 of I/Os: I2C4, MCSPI4, UART4 I/Os
vdds_dv_bank6	Bank 6 of I/Os: USB4 ULPI TLL, SDMMC3, SDMMC4 I/Os
vdds_dv_bank7	Bank 7 of I/Os: Keyboard I/Os
vdds_dv_c2c	Chip-to-chip (C2C) I/Os
vdds_dv_fref	fref dual voltage I/Os: fref_clk[3:4]_out/fref_clk[3:4]_req
vdds_1p8_fref	Oscillator, slicer, fref_clk0_out, and fref_clk_ioreq

For more information about power management, see *Power Management Functional Description*, in Chapter 3, *Power, Reset, and Clock Management*.

The OMAP4460 power supply structure is based on the following constraints:

- Because most of the I/Os must be powered before the core, they are supplied on a specific rail (1.2 or 1.8 V).
- MPU is supplied with additional power resource. It is controlled by SmartReflex link and a GPIO pin.
- IVA, ABE, and Core are mapped on dedicated SMPS to allow independent SmartReflex dynamic frequency and voltage scaling for each of them.
- Because the DPLL, DSI, CSI, and USB OTG interfaces are noise-sensitive power domains, they are supplied by a dedicated rail to avoid other power sinks from affecting their power rail.
- Because bandgap, BodyBias LDOs, and SRAM LDOs must be supplied at 1.8 V from the beginning of the power-up sequence up to the end of power down, they are supplied by V1V8. This also applies to the WKUP LDO at 1.2 V.
- Video DAC, eFuse VPP, SDMMC, and USB I/Os have specific requirements (sequencing, dual voltage, noise immunity, etc.) that require each of them be supplied by a dedicated power source.

27.2.2 Access to Power-Management IC

The ROM code accesses the power-management chip for the following purposes:

- SD/MMC1 powering:
  - The VMMC LDO is switched on by the ROM code when booting from the SD/MMC1 interface.

NOTE: The power supplies required for SD/MMC interface 2 are not controlled by the ROM code. It is assumed that the power-management chip (or the system hardware) properly powers the SD/MMC module attached to this interface.

- USB peripheral booting (internal or external transceiver):
  - PrevStartOk mechanism

    This mechanism provides the ability to bypass the USB connection if a specific flag is set in the TWL6030 RTC domain (retained when the system if switched off).

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– USB transceiver powering

The TWL6030 VUSB LDO is turned on by the ROM code.

NOTE: If TWL6030 is not present and the USB external transceiver boot is chosen, the TWL6030-related operations do not complete without blocking the USB boot procedure.

- USB peripheral booting (internal transceiver):
  – VBUS detection

    The VBUS power pad is localized on the TWL6030 power IC. As a result, the ROM code must read from a TWL6030 register to get the status reflecting the device attachment to the USB link.
  – Gating the TWL6030 USB charging circuitry during a suspend scenario

    If this event occurs, the ROM code should detect a suspend event and gate the charge circuitry inside the TWL6030.

NOTE: If TWL6030 and/or VBUS are not detected, the USB boot is blocked when booting from the internal transceiver, except if the USB(2) option is chosen.

27.2.2.1 Power-Management IC Detection

When booting from an SD/MMC card or USB internal transceiver (and only for these two booting options) the ROM code tries to access the power device through the inter-integrated circuit (I^2C™). The first access is a read transaction to obtain the TWL6030 version register. If this read access is successful (that is, the I^2C transaction is acknowledged), the ROM code considers that a power-management device is attached, assuming it is TWL6030. The version value read is not used in any computation or compared to any hardcoded value.

If the first read transaction fails (that is, the I^2C transaction times out or is not acknowledged), the ROM code logs it into a flag and does not try any further transaction until the next reset cycle. In this case, the nondetection of the companion chip does not block the SD/MMC1 boot process. However, the MMC card boot procedures do not work as defined in this document. In particular, The ROM code does not ensure that the SD/MMC1 interface is powered when accessing the memory contents.

The nondetection of the power-management IC blocks the USB internal transceiver boot, except when USB(2) booting mode is chosen.

An alternate way to boot from the USB internal transceiver without the TWL6030 and with the USB(1) booting option is to have the alternate power-management IC match (or emulate) at least read the P1, P2, and P8 commands (see Section 27.2.2.2, *Summary of the I^2C Transactions*).

If TWL6030 is not present, but the USB(2) option is chosen, or registers are emulated, the following functions are not ensured to work:

- The PrevStartOk mechanism is not functional (the specific flag is not checked).
- The ROM code does not ensure that the VUSB power is applied to the USB transceiver.
- Peripheral booting from the internal USB transceiver is not ensured to be functional, because the VBUS state read transaction is not performed.
- The ROM code does not support the suspend scenario during USB peripheral boot from the internal transceiver.

From the ROM code perspective, nothing prevents the use of another power IC together with the OMAP4460. However, special care must be taken if considering the two previously mentioned booting options (SD/MMC1 or USB internal transceiver).

Table 27-2 summarizes the USB booting options according to TWL6030 presence.

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Table 27-2. USB Booting Options

Booting Option	TWL6030 Detected	TWL6030 Emulated	Description
USB(1)	Yes	N/A	Full USB booting
USB(1)	No	Yes	ROM code does not ensure VUSB, VBUS, PrevStartOk, or suspend mode.
USB(1)	No	No	USB booting is not possible.
USB(2)	Yes	N/A	Full USB booting
USB(2)	No	Yes	ROM code does not ensure VUSB, VBUS, PrevStartOk, or suspend mode.
USB(2)	No	No	ROM code does not ensure VUSB or VBUS. PrevStartOk and suspend mode are not supported.
USB-ULPI	Yes	N/A	ROM code does not ensure VUSB or VBUS. PrevStartOk is supported. Suspend mode is not supported.
USB-ULPI	No	Yes	ROM code does not ensure VUSB, VBUS, or PrevStartOk. Suspend mode is not supported.
USB-ULPI	No	No	ROM does not ensure VUSB or VBUS. PrevStartOk and suspend mode are not supported.

27.2.2.2 Summary of the I²C Transactions

The ROM code accesses the power-management chip through the I2C1 interface. Table 27-3 summarizes the list of accesses.

Table 27-3. Register Accesses to PMIC

ID	I²C Address	Register Address	TWL6030 Register	Access Type	Value	Transaction Condition
P1	0x4A	0x87	JTAGVERNUM	R	0x-	Booting from MMC1, USB, or USB-ULPI
P2	0x48	0x2B	PHOENIX_SEQ_CFG	R/W	0x-/0x00	Booting from USB or USB-ULPI
P3	0x48	0x9B	VMMC_CFG_VOLTAGE	W (ORed) (1)	0x15	Booting from MMC1
P4	0x48	0x9A	VMMC_CFG_STATE	W (ORed) (1)	0xE1	Booting from MMC1
P5	0x48	0xA3	VUSB_CFG_VOLTAGE	W (ORed) (1)	0x18	Booting from USB or USB-ULPI
P6	0x48	0xE5	MISC2	W	0x08	Booting from USB or USB-ULPI
P7	0x48	0xA2	VUSB_CFG_STATE	W	0xE1	Booting from USB or USB-ULPI
P8	0x49	0xE3	CONTROLLER_STAT1	R	0x-	Booting from USB or USB-ULPI
P9	0x49	0xE8	CHARGERUSB_CTRL1	W	0x80	Booting from USB

(1) (1) The register is not blindly overwritten but is first read and then ORed with the specified value.

Transaction description

P1: JTAGVERNUM: Power-management IC detection. There must be a register at this location; however, its value is not used further by ROM code.

P2: PHOENIX_SEQ_CFG: The PrevStartOk flag is checked when performing USB peripheral boot (internal or external transceiver). If the flag is set, the USB peripheral booting procedure is skipped. In any case the full register is cleared (write 0x00) after the read transaction.

P3: VMMC_CFG_VOLTAGE: For the sake of powering the SDMMC1 card cage, the VMMC_CFG_VOLTAGE and VMMC_CFG_STATE registers are configured to set the VMMC LDO to 3 V. The value 0x15 is written to the VMMC_CFG_VOLTAGE register (selects 3-V output).

P4: VMMC_CFG_STATE: The value 0xE1 is written to the VMMC_CFG_STATE register (applies to all register groups, LDO state switched on).

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P5: VUSB_CFG_VOLTAGE: The USB OMAP internal transceiver must be powered with a 3.3-V source to ensure its correct functionality. Three registers are used for this purpose. The VUSB_CFG_VOLTAGE register is written the value 0x18 for selecting 3.3 V.

P6: MISC2: The MISC2 register is written the value 0x08 for selecting the VBUS source.

P7: VUSB_CFG_STATE: The VUSB_CFG_STATE register is written the value 0xE1 for switching the VUSB LDO on for all register groups.

P8: CONTROLLER_STAT1: VBUS detection is performed by reading the VBUS_DET bit from the CONTROLLER_STAT1 register. If this bit is set, it reflects that a USB cable is plugged.

P9: CHARGERUSB_CTRL1: This register is written the value 0x80 (SUSPEND_BOOT = 1) for gating the charge circuitry when getting a USB SUSPEND event. If this bit is not set, the USB boot is aborted.

The complete description of the TWL6030 register map is in TWL6030 documentation.

NOTE: No specific action is performed regarding the TWL6030 primary watchdog feature. In particular, if it is active (configurable in EEPROM) in the companion device, a system reset may occur before ROM code completes. The elapse value for the reset must be appropriately tuned so that the ROM code is not interrupted before the full platform start up (that is, before the initial software can take a specific action).

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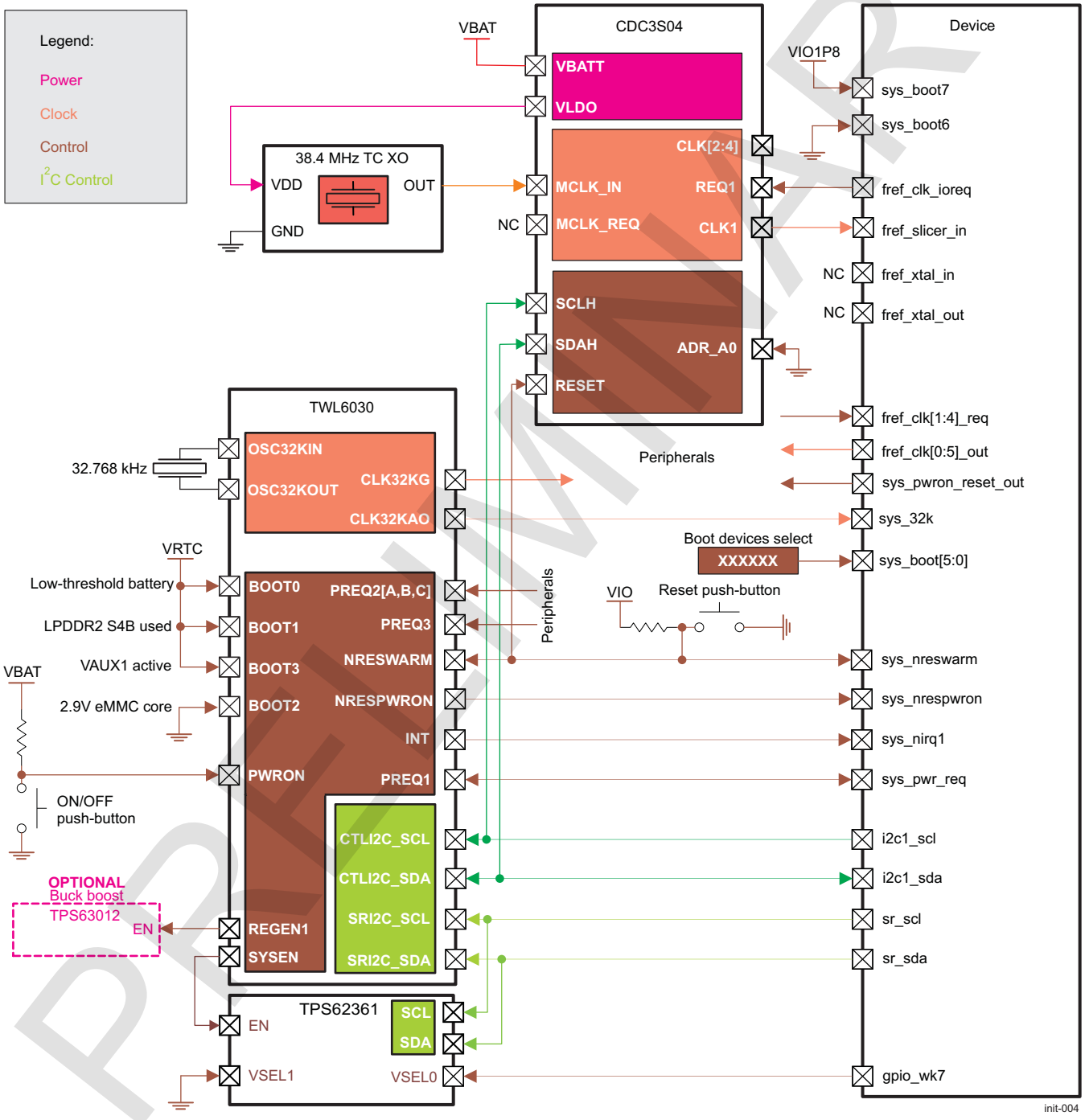
27.2.3 Clock, Reset, and Control

27.2.3.1 Overview

Figure 27-3 shows the clock and reset environment that gathers the clocks and reset-related signals at the system level, and the system-expansion signals.

Figure 27-3. Clock, Reset and Control Environment



The main features of the system interface are:

- A clock request output to an external clock source

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- 12-, 16.8-, 19.2-, 26-, or 38.4-MHz reference clock input from external oscillator or clock supplied using internal crystal oscillator (up to 20 MHz)
- 32-kHz CMOS clock input
- Six configurable output clocks
- Eight input signals to define the boot mode and device system clock source
- Two reset sources
  - Power-on reset (POR) (cold reset)
  - Bidirectional warm reset

27.2.3.2 Clocking Scheme

27.2.3.2.1 Required System Input Clocks

The device operation requires external input clocks, as follows:

- 32k clock: A 32.768-kHz crystal is connected to the TWL6030 device that embeds the 32k-oscillator (a square CMOS clock can also be delivered on the 32k_xtalin pin if the 32k-crystal is connected on another device of the system). The resulting 32k clock is delivered to the entire system on three outputs:
  - CLK32KAO_is always on (meaning that when TWL6030 VIO is on; that is, it is in WAIT-ON or ACTIVE state). It is used to deliver a 32k clock to always-on features, such as the OOMAP4460 and modem in the described system.
  - CLK32KG is software-controlled and is delivered when requested by the OMAP4460 (this input is on by default at platform boot).
  - CLK32KAUDIO is software-controlled and is delivered to the TWL6040 audio device (not shown in Figure 27-3) when requested by the OMAP4460 (this input is on by default at platform boot).
- High-speed clock: The platform high-speed (HS) low-jitter sine clock is provided by the clock driver (CDC3S04) to the TWL6040 audio IC, OMAP, and other peripherals requesting low-jitter sine clock (up to three outputs are available for peripherals). The OMAP device delivers digital clocks to other peripherals. The OMAP4460 supports different flavors of clock sources at several frequencies:
  - Crystal source. An internal oscillator embedded in the OMAP4460 is used. In this mode, the input clock is limited to 20 MHz by oscillator construction. The fref_clk_ioreq is then set as an input to be used by an external device to request the OMAP4460 to deliver the clock on fref_clk0_out. The fref_slicer_in pin can then be used to input an auxiliary clock (mainly for debugging purposes).
  - External oscillator type source. The internal OMAP4460 oscillator is disabled. The external source delivers a sine (slicer active) or square (slicer bypassed) single-ended clock on the fref_slicer_in pin. The external source is enabled by the fref_clk_ioreq output. fref_xtal_in can then be used to input an auxiliary clock (oscillator-bypass mode).
- Audio clock: The TWL6040 audio device builds its own clock, either from the 32k clock or the HS clock (depending on the audio scenario). This internal clock is delivered to the OMAP4460 ABE subsystem (abe_clks input) for audio flow synchronization.

Clock input modes are selected by the sysboot pin (sys_boot[6:7]) to allow the system to wake up in the proper mode, even after a cold boot (selection of the relevant input pin [fref_slicer_in or fref_xtal_in/out] and slicer/oscillator mode setting [on or bypass]).

The OMAP4460 provides the HS clock to other devices through six fref_clk[0:5]_out pins.

TWL6040 audio device receives the HS clock on the MCLK pin when the audio scenario requires it (some low-power audio player scenarios can be performed only with the 32k clock).

Table 27-4 lists the mapping for the OMAP clock input sources. Table 27-5 lists the TWL6030 clock requirements.

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Table 27-4. Mapping for Input Sources

Input Source	Mapping	Frequency Range/List	Type
Internal oscillator	fref_xtal_in/fref_xtal_out	12, 16.8, or 19.2 MHz	Crystal connection pins
External HS clock	fref_slicer_in	12, 16.8, 19.2, 26, or 38.4 MHz	Sine or square single ended
External 32k clock	sys_32k	32.768 kHz (nom.)	Square
TWL6040 audio IC	abe_clks	19.2 MHz	Square

Table 27-5. TWL6030 Clock Requirements

Input Source	Mapping	Frequencies Range/List	Type
Internal oscillator	OSC32KIN/OSC32KOUT	32.768 kHz (nom.)	Crystal connection pins

CAUTION

Clock configurations depend on core voltage, and maximum clock frequencies may not be applicable to production.

27.2.3.2.2 Optional System Output Clocks

The OMAP device can output six alternate clocks, fref_clk[0:5]_out. Output clocks 1 through 4 can be gated or enabled through associated clock-request signals, fref_clk[1:4]_req.

The clocks can be managed by software with the appropriate register in the power, reset, and clock management (PRCM) module. For more information, see Section 3.3, *PRCM Subsystem Environment*.

27.2.3.3 Reset Configuration

27.2.3.3.1 ON/OFF Interconnect and Power-On-Reset

The entire system is typically awakened by an ON/OFF push button connected to the TWL6030 power IC. This signal belongs to the VBAT power domain and is active low (the TWL6030 internal pullup ties it to VBAT). Power up is propagated to the OMAP4460 through NRESPWRON/sys_nrespwron signals when the TWL6030 power-up sequence is achieved. Because this signal is also provided to the TWL6040 audio IC, it resets its state-machine and gets some available functions even if the V2V1 power supply is not provided.

27.2.3.3.2 Warm Reset

A warm reset can be asserted by the OMAP4460, by an external button (typically for development platform), or by any other device connected to it. It is mainly used to propagate the OMAP4460 internal reset to the whole platform to set it to a known state.

The OMAP4460 releases sys_nreswarm after NRESPWRON is deasserted.

27.2.3.3.3 Peripheral Reset by sys_pwron_reset_out

Sys_pwron_reset_out is provided to the system by the OMAP4460 to power on and/or deactivate the reset of system peripherals. This signal is activated by SCRM during the power-up sequence a few milliseconds after the default-on clocks (OMAP4460 – fref_clk4_out and CDC3S04 – CLK[1:4]) are stabilized. This allows switching on peripherals that require synchronous reset.

Sys_pwron_reset_out is controllable by software when the system is on. It is not affected by a warm reset.

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27.2.3.3.4 Peripheral Reset by GPIO

Most of the peripherals are reset/power on/off by GPIO. By default, under POR, most OMAP4460 signals are in safe mode with a default value driven by the I/O cell. The value is driven by an internal pullup or pulldown. Depending on the peripheral reset active level, users must select one GPIO or another (according to the reset value).

Once POR is released, the value on the pad is driven by the default configuration of control module. Most of time, this configuration is aligned with the default value selected on the I/O cell.

The next step is application-dependent: Users must configure the OMAP4460 registers to validate GPIO use and the default configuration of the control module.

27.2.3.3.5 Warm Reset Impact on GPIOs

When a warm reset event occurs:

- The GPIO controller is reset. Consequently, the GPIO is automatically turned in input mode.
- The control module, which is part of the wake-up domain, is not reset. Information related to signal multiplexing mode and pullup or pulldown configuration is still valid.

Therefore, when a warm reset event happens, the output buffer is disabled. Consequently, two different behaviors can be defined with regard to what is expected by the platform:

- GPIO sensitive to warm reset:

  To avoid getting a floating signal during (and after) a warm reset event, users must select a pullup or pulldown (depending on the reset value of the peripheral) and enable the pull.
- GPIO not sensitive to warm reset:

  To avoid getting a floating signal during (and after) a warm reset event and to keep the same value that was driven before the reset, users must align the pull value with the drive value each time there is an access to a dedicated GPIO register.

NOTE: To avoid unnecessary consumption, user software must ensure that the internal pull resistor is disabled when the GPIO buffer is driving.

NOTE:

- For more information about device reset management, see Section 3.5, *Reset Management Functional Description* in Chapter 3, *Power, Reset, and Clock Management*..
- To determine the cause of the last reset, see Section 3.5.5, *Reset Logging*, in Chapter 3, *Power, Reset, and Clock Management*.

27.2.3.4 TWL Power/Audio Devices Control

- I^2C:

  The TWL6030 power and TWL6040 audio devices are controlled by the OMAP4460 I2C1 (HS I^2C). Some internal pullup resistors are provided by the OMAP4460 (different values can be selected to adapt the I/O buffer strength to the bus topology). The I^2C links must first be started in fast-speed mode. Therefore, the buffer default pullup value must support this mode.
- SmartReflex control:

  Some of the TWL6030 power resources are controlled through SmartReflex link (I^2C-like). This control allows the host to drive the dynamic voltage frequency scaling (DVFS) and adaptive voltage scaling (AVS) operations of these resources. As with its I^2C interfaces, some internal pullup resistors are provided on the OMAP4460 SmartReflex I/Os. The link must be run at the highest speed allowed by the voltage controller of the OMAP4460 (lower than I^2C HS mode frequency). For example, this frequency must be 1.82 MHz with a 38.4-MHz system clock.
- INT:

  Both devices can activate the INT signal at any time when they require the host device to monitor their

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activity. When receiving such an interruption, the OMAP4460 checks, through the I^2C, to determine the source of the interrupt. These INT pins are active low.

- Sys_pwr_req:

  When exiting off mode, the OMAP4460 ties up the sys_pwr_req pin to wake up the TWL6030 power application group.

27.2.3.5 TWL6030 Power Request Signals

The TWL6030 power-management IC drives three external enable-output signals. This allows switching on some external resources at different stages of the power-up sequence:

- REGEN1/2 are driven high at the beginning of the power-up sequence, before any internal power source is turned on. They belong to the VBAT power domain. REGEN1 can typically be used for buck boost control.
- SYSEN is driven high immediately after the VCORE power output is turned on. It allows switching on the additional power regulator to supply the MPU subsystem. SYSEN belongs to the VIO power domain.

TWL6030 power also receives five power resource requests: PREQ[1, 2A, 2B, 2C, 3]. These pins allow an external device to request TWL6030 power internal resources. TWL6030 power behavior when pins are activated must be programmed after the first boot (resources and PREQ pins allocated by group, resource behavior upon group activation, etc.). The typical PREQ allocation per group is:

- PREQ1: Application group. Connected to OMAP.
- PREQ2A, PREQ2B, and PREQ2C: Peripheral group. Connected to peripherals A, B, and C (for instance, Bluetooth®/FM/GPS/WLAN device, Wimax device, W-USB device).
- PREQ3: Modem group

NOTE: Powering the clock driver requires PREQ assertion. Therefore, it is advised to connect any peripheral receiving a clock from CDC3S04 to one PREQ.

The use of PREQ[1:3] is especially required when TWL6030 is in sleep mode, because it cannot handle an I^2C command. Any device that requires the TWL6030 resource to wake up must first activate its associated PREQ. All TWL6030 power regulators are off or in sleep mode when TWL6030 is in sleep mode.

PREQ1 is used by OMAP when waking up from off mode to wake up the TWL6030.

27.2.4 Boot Configuration

Six external pads (sys_boot[5:0]) are used to select interfaces or devices for the booting list. The sys_boot[7:6] pads select the OMAP clock source configuration.

All eight pins are sampled and latched onto the SYSCTRL_GENERAL_CORE.CONTROL_STATUS[7:0] SYS_BOOT register bit field after POR. After booting, these pads can be used for other functions such as GPIOs, and the associated register bit field is not updated by the new functionality. For more information about pad multiplexing configuration, see Section 18.4.8, *Pad Functional Multiplexing and Configuration*.

NOTE:

- If used as GPIOs, sys_boot[7:0] pads must be used only in output mode to ensure that the input values are selected by the pullups and pulldowns after POR.
- Unlike sys_boot[5:0] pads, sys_boot[7:6] pads have no internal pullups or pulldowns automatically selected at POR. The sys_boot[5:0] pads have selected pulldowns at that moment. To avoid leakage, care must be taken to disable the pulldown in case the respective pad has external connection to VIO (= 1). See the appropriate register fields in Chapter 18, *Control Module*.

27.2.4.1 System Clock Source Selection

Figure 27-4 is an overview of the system clock selection. Table 27-6 summarizes the selection.

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Figure 27-4. System Clock Selection Diagram

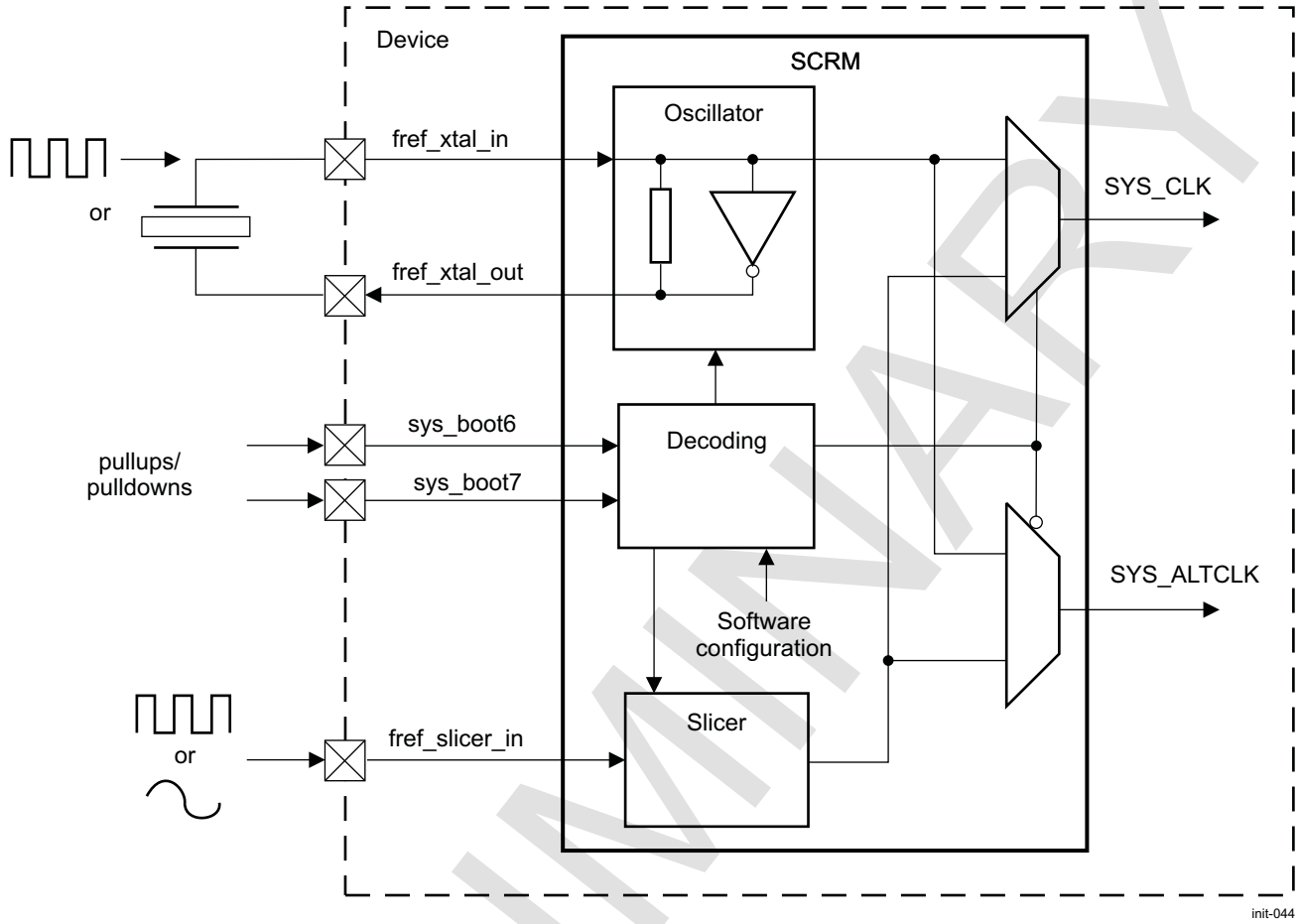

Table 27-6. System Clock Selection Summary

sys_boot[7:6]	SYS_CLK Source	SYS_ALTCLK Source	Oscillator Mode	Slicer Mode	fref_clk_ioreq Mode
0b00	fref_xtal_in	fref_slicer_in	Active	Power-down	Input
0b01	fref_xtal_in	fref_slicer_in	Bypass	Power-down	Output
0b10	fref_slicer_in	fref_xtal_in	Power-down	Active	Output
0b11	fref_slicer_in	fref_xtal_in	Power-down	Bypass	Output

OMAP4460 clock source settings description:

- sys_boot[7:6] = 0b00:
  - The system clock source is the on-chip oscillator.
  - The slicer is powered down and its input can be used to provide the OMAP with an alternate clock.
  - Fref_clk_ioreq is a clock request input associated to fref_clk0_out by default.
- sys_boot[7:6] = 0b01:
  - The system clock source is external. The internal oscillator is bypassed to inject the system clock.
  - The slicer is powered down and the slicer input can be used to provide the chip with an alternate clock.
  - The Fref_clk_ioreq signal is an output that requests the clock to the external clock supplier.
- sys_boot[7:6] = 0b10:
  - The system clock source is the on-chip slicer, supplied by an external oscillator. The internal

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oscillator is powered down and the input can be configured to supply the alternate system clock to OMAP device.
  - The slicer is active.
  - The Fref_clk_ioreq signal is an output that requests the clock from the external clock supplier.
- sys_boot[7:6] = 0b11:
  - The system clock source is external. The internal oscillator is powered down and the input can be configured to supply the alternate system clock to the OMAP device.
  - The slicer is bypassed to inject the system clock.
  - The Fref_clk_ioreq signal is an output that requests the clock from the external clock supplier.

27.2.4.2 Booting Device Order Selection

The ROM code creates the device list (order) based on information gathered from two locations.

- The first location is the software booting configuration stored in the nonvolatile SAR memory, and used after warm resets.
- The second location is the sys_boot[5:0] external configuration pins sensed in the control module.

The SYSBOOT pins are used to index a booting device list from a table with possible booting scenarios. The order of examined booting devices is from the first to the fourth devices.

The following names are used in the tables:

- Memory types:
  - Execute in place (XIP): XIP memory without wait-signal monitoring enabled (NOR flash memory or other XIP device)
  - XIP wait: XIP memory with wait-signal monitoring
  - NAND: NAND flash memories (non-XIP)
  - OneNAND: OneNAND and Flex-OneNAND flash memories
  - MMC1: MMC/SD card or eMMC™/eSD™ device (SD/MMC port 1)
  - MMC2(1): eMMC or eSD memory device, first option (SD/MMC port 2). See Section 27.2.4.3, *Boot Peripheral Pin Multiplexing*.
  - MMC2(2): eMMC or eSD memory device, second option (SD/MMC port 2). See Section 27.2.4.3, *Boot Peripheral Pin Multiplexing*.
- Peripheral interfaces:
  - USB(1): USBA0 from OMAP internal transceiver (USBPHY)
  - USB(2): USBA0 from OMAP internal transceiver (USBPHY). Allows USB booting even when no power-management IC is detected.
  - USB-ULPI: USBA0 from external transceiver through ULPI interface
  - Universal asynchronous receiver/transmitter (UART): UART3 interface
- Permanent booting devices listed in Table 27-7 are in **bold**.

NOTE: Only permanent booting devices (in bold) are put on in the list in case of a warm reset, and the device list is taken from the sys_boot pins. As a result, peripheral booting devices are skipped when the OMAP4460 restarts from warm resets.

Users can force the execution of the peripheral booting procedure after warm reset by using the software booting configuration feature.

Table 27-7 lists the booting device order when it is preferred to boot from a memory type device. This table is selected by ROM code when the sys_boot5 pin is tied high (= 1) after reset and before booting completes. If fast XIP booting is selected, the sys_boot5 pin controls the XIP wait-signal monitoring (that is, a logical high level enables wait-signal monitoring).

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Table 27-7. Memory Preferred Booting

sys_boot[5:0]	Booting Devices Order			
	1st	2nd	3rd	4th
0b100000	**MMC2(1)**	USB(1)		
0b100001	**XIP**	USB(1)		
0b100010	**XIPWAIT**	USB(1)		
0b100011	**NAND**	USB(1)		
0b100100	**XIPWAIT**	USB(1)		
0b100101	**MMC1**	USB(1)		
0b100110	**OneNAND**	USB(1)		
0b100111	**OneNAND**	**MMC2(1)**	USB(1)	
0b101000	**MMC2(1)**	UART		
0b101001	**OneNAND**	**MMC2(1)**	USB(2)	
0b101010	**XIPWAIT**	UART		
0b101011	**NAND**	UART		
0b101100	**NAND**	USB(2)		
0b101101	**MMC1**	UART		
0b101110	**OneNAND**	UART		
0b101111	**MMC2(1)**	USB-ULPI		
0b110000	**XIP**	USB-ULPI		
0b110001	**XIPWAIT**	USB-ULPI		
0b110010	**NAND**	USB-ULPI		
0b110011	**MMC1**	USB(2)		
0b110100	**MMC1**	USB-ULPI		
0b110101	**OneNAND**	USB-ULPI		
0b110110	**MMC2(1)**	USB(1)	UART	MMC1
0b110111	**XIP**	USB(1)	UART	MMC1
0b111000	**MMC2(2)**	USB-ULPI	UART	
0b111001	**NAND**	USB(1)	UART	MMC1
0b111010	**MMC2(2)**	UART		
0b111011	**MMC1**	USB(1)	UART	
0b111100	**MMC2(2)**	USB(1)		
0b111101	**MMC2(2)**	USB(2)		
0b111110	Reserved			
0b111111 (1)	**Fast XIP booting. Wait monitoring ON**	USB(1)	UART	

(1) Only on GP devices

Table 27-8 lists the booting device order when it is preferred to boot from a peripheral-type device. This table is selected by ROM code when the sys_boot5 pin is tied low (= 0). If fast XIP booting is selected, the sys_boot5 pin controls the XIP wait-signal monitoring (that is, a logical low level disables wait-signal monitoring).

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Table 27-8. Peripheral Preferred Booting

sys_boot[5:0]	Booting Devices Order			
	1st	2nd	3rd	4th
0b000000	USB(1)	**MMC2(1)**		
0b000001	USB(1)	**XIP**		
0b000010	USB(1)	**XIPWAIT**		
0b000011	USB(1)	**NAND**		
0b000100	USB(1)	**XIPWAIT**		
0b000101	USB(1)	**MMC1**		
0b000110	USB(1)	**OneNAND**		
0b000111	USB(1)	**OneNAND**	**MMC2(1)**	
0b001000	UART	**MMC2(1)**		
0b001001	UART USB(2)	**OneNAND**	**MMC2(1)**	
0b001010	UART	**XIPWAIT**		
0b001011	UART	**NAND**		
0b001100	UART USB(2)	**NAND**		
0b001101	UART	**MMC1**		
0b001110	UART	**OneNAND**		
0b001111	USB-ULPI	**MMC2(1)**		
0b010000	USB-ULPI	**XIP**		
0b010001	USB-ULPI	**XIPWAIT**		
0b010010	USB-ULPI	**NAND**		
0b010011	USB-ULPI USB(2)	**MMC1**		
0b010100	USB-ULPI	**MMC1**		
0b010101	USB-ULPI	**OneNAND**		
0b010110	USB(1)	UART	MMC1	**MMC2(1)**
0b010111	USB(1)	UART	MMC1	**XIP**
0b011000	USB-ULPI	UART	**MMC2(2)**	
0b011001	USB(1)	UART	MMC1	**NAND**
0b011010	UART	**MMC2(2)**		
0b011011	USB(1)	UART	**MMC1**	
0b011100	USB(1)	**MMC2(2)**		
0b011101	USB(2)	**MMC2(2)**		
0b011110	Reserved			
0b011111 (1)	**Fast XIP booting. Wait monitoring OFF**	USB(1)	UART	

(1) Only on GP devices

27.2.4.3 Boot Peripheral Pin Multiplexing

Table 27-9 lists the code pin multiplexing configuration supported by ROM according to boot peripheral.

Table 27-9. Pin Multiplexing According to Boot Peripheral

Boot Device	Boot Interface	Pads
NAND/OneNAND	GPMC	GPMC pads in mux mode 0, CS0, WAIT0
XIP memory	GPMC	GPMC pads in mux mode 0, CS0, WAIT0
MMC/SD/eMMC/eSD	SDMMC1	SDMMC1 pads in mux mode 0
eMMC/eSD	SDMMC2 (option 1) SDMMC2 (option 2)	GPMC pads in mux mode 1 SDMMC5 and FREF_CLK pads, all in mux mode 5

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Table 27-9. Pin Multiplexing According to Boot Peripheral (continued)

Boot Device	Boot Interface	Pads
UART	UART3	UART3 pads in mux mode 0
USB from internal transceiver	HSUSBOTG (USBA0-USBPHY)	USBA0_OTG pads in mux mode 0
USB from external transceiver	HSUSBOTG (USBA0-ULPI)	DPM_EMU[2:13] pads in mux mode 1

NOTE: The ROM code examines the interfaces that are selected to be searched until a valid bootable interface/device is found. The activities on the pads of the searched interfaces must be considered in case they are connected to any other peripherals for any other purposes (for example, an LED connected to a GPMC pad muxed internally to a GPIO).

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27.3 Reset Sequences

For the description of the reset sequences, see Section 3.5.6, *Reset Sequences*, in Section 3.5, *Reset Management Functional Description*.

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27.4 Device Initialization by ROM Code

This section describes high-level booting concepts and provides basic knowledge for booting on the device.

27.4.1 Booting Overview

27.4.1.1 Booting Types

Booting is the process of starting a bootstrap from one of the booting devices.

The ROM code has two functions for booting: Peripheral booting and memory booting.

- In peripheral booting, the ROM code polls a selected communication interface such as UART or USB, downloads the executable code over the interface, and executes it in internal RAM. Downloaded software from an external host can be used to program flash memories connected to the device. This special case of peripheral booting is called preflashing; software downloaded for preflashing is called the flash loader. The flash loader burns a new client application image in external flash memory. Initial software is a generic term for bootstrap, downloaded software, and flash loader. After the image is burnt, a software (warm) reset can be performed.
- In memory booting, the ROM code finds the bootstrap in permanent memories such as flash memory or memory cards and executes it. This process is normally performed after a cold or warm device reset.

The ROM code detects whether the device should download software from a peripheral interface (USB or UART) by using the sys_boot[5:0] pin configuration. This mechanism encompasses initial flashing in production (external memory is empty) and reflashing in service (external memory is already programmed).

27.4.1.2 ROM Code Architecture

Figure 27-5 shows the ROM code architecture. It is split into three main layers with a top-down approach: high-level, drivers, and hardware abstraction layer (HAL). One layer communicates with a lower-level layer through a unified interface.

- The high-level layer performs the main tasks of the public ROM code: multicore startup, watchdog and clock configurations, interrupt management, interaction with the power-management IC, and main booting routine.
- The driver layer implements the logical and communication protocols for any booting device in accordance with the interface specification.
- The HAL implements the lowest level code for interacting with the hardware infrastructure IPs. End booting devices are attached to the device I/O pads.

Figure 27-5 shows the three layers with their modules.

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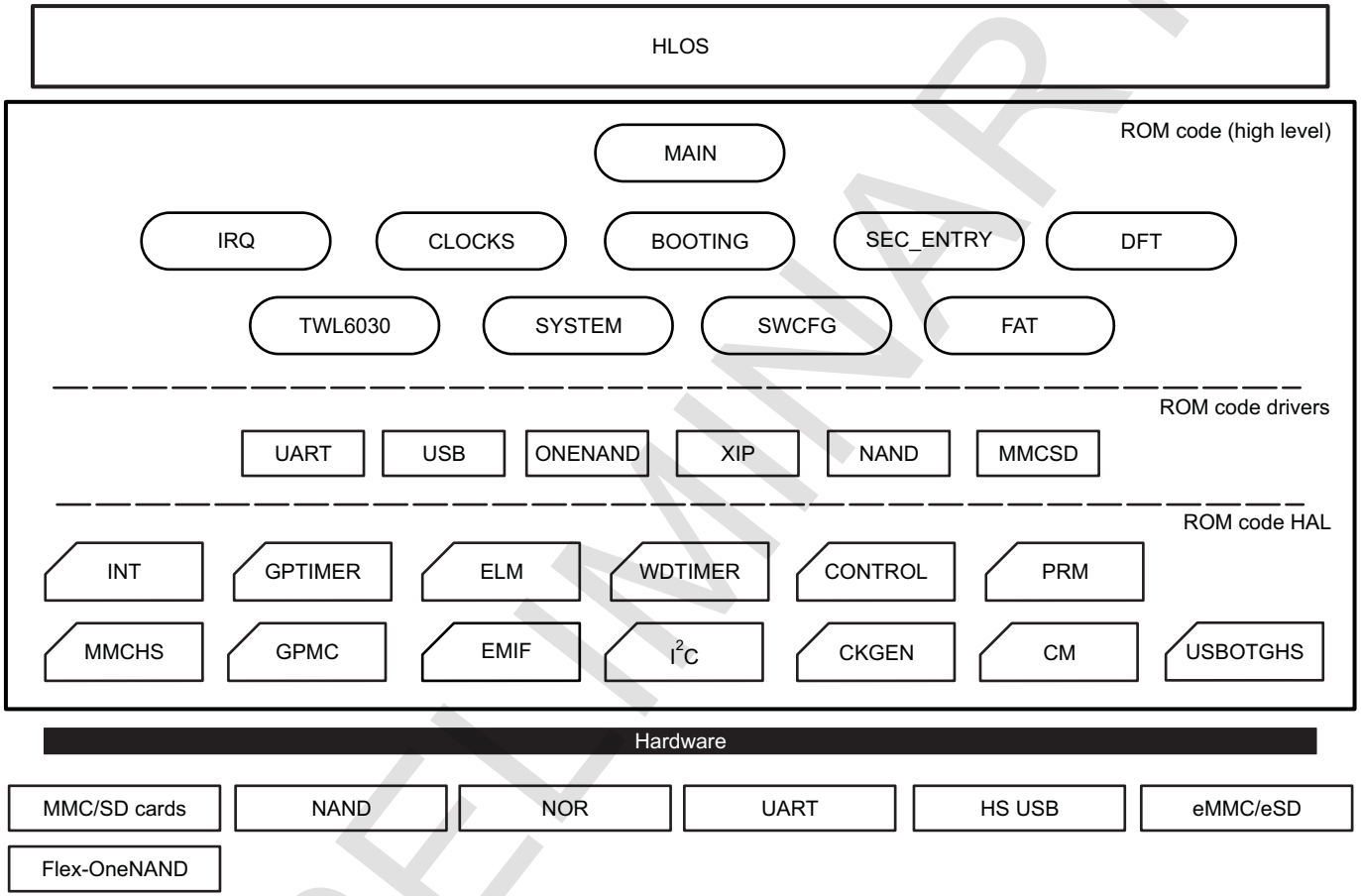
Figure 27-5. ROM Code Architecture



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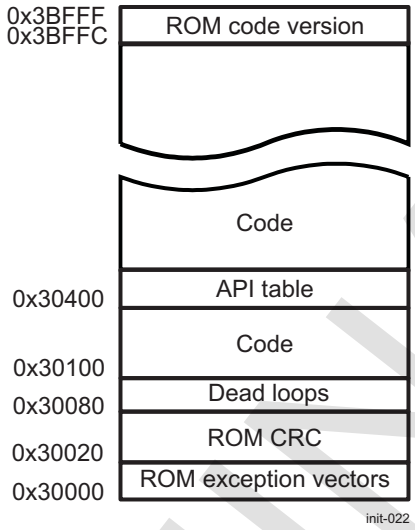
27.4.2 Memory Maps

27.4.2.1 ROM Memory Map

Figure 27-6 shows the 48-KB ROM memory map.

Figure 27-6. ROM Memory Map



- ROM exception vectors

  Exceptions are redirected to ROM exception vectors (see Table 27-10). The reset exception is redirected to the public ROM code startup. Other exceptions are redirected to RAM handlers by loading appropriate addresses to the PC register.

Table 27-10. ROM Exception Vectors

Address	Exception	Content
0x30000	Reset	Branch to the ROM code startup
0x30004	Undefined	PC = 0x4030 D004
0x30008	Software interrupt (SWI)	PC = 0x4030 D008
0x3000C	Prefetch abort	PC = 0x4030 D00C
0x30010	Data abort	PC = 0x4030 D010
0x30014	Unused	PC = 0x4030 D014
0x30018	IRQ	PC = 0x4030 D018
0x3001C	FIQ	PC = 0x4030 D01C

- ROM code cyclic redundancy check (CRC)

  The ROM code CRC is calculated as 32-bit CRC code (CRC-32-IEEE 802.3) for the address range 0x30000–0x3BFFF. The 4-byte CRC code is stored at location 0x30020.

- Dead loops

  Dead loops are branch instructions coded in ARM mode. They have multiple purposes (see Table 27-11).

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Table 27-11. Dead Loops

Address	Purpose
0x30080	Undefined exception default handler
0x30084	SWI exception default handler
0x30088	Prefetch abort exception default handler
0x3008C	Data abort exception default handler
0x30090	Unused exception default handler
0x30094	IRQ exception default handler
0x30098	FIQ exception default handler

The fixed location of these dead loops facilitates debugging and testing. The first seven dead loops are default exception handlers linked to RAM exception vectors.

Dead loops can be called directly from code, but there is also a special function called from ROM code to execute a dead loop. This function is at address 0x300C0. The function is assembly code in ARM mode, which takes the dead loop address from the R0 register. The main purpose of the function is to issue a global software reset before going to a dead loop. In addition, the function clears the global cold reset status before issuing the global software reset.

- Code

  This space is used to hold code and constant data.

- API table

  The purpose of this table is to allow external code access to system maintenance, utility, and device driver functions which are used for ensuring the ROM code boot functionality. These functions can be reused at run time by calling a fixed address hardcoded in this table.

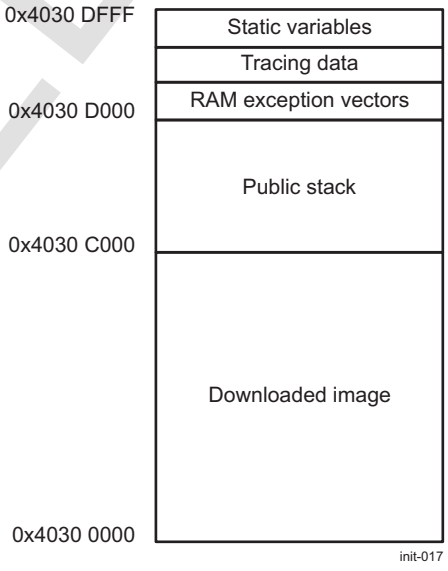
- ROM code version

  The ROM code version consists of two decimal numbers: major and minor. It can be used to identify the ROM code release version burnt in a given IC (for example, useful during a debugging session). The ROM code version is a 32-bit hexadecimal value at address 0x3BFFC.

27.4.2.2 RAM Memory Map

The partitioning of the on-chip SRAM (L3 OCM RAM) shown in Figure 27-7 is used during the booting process. Tracing and static variables areas can also be accessed when calling API functions.

Figure 27-7. RAM Memory Map



- Downloaded image

  This space is used by the public ROM code to store a downloaded booting image. It can be up to

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48KB.

- Public stack

  This space is reserved for stack.

- RAM exception vectors

  The RAM exception vectors provide an easy way to redirect exceptions to the custom handler. Table 27-12 lists the contents of the RAM space reserved for RAM vectors. The first eight addresses are ARM instructions that load the value in the subsequent eight addresses into the PC. These instructions are executed when an exception occurs because they are called from ROM exception vectors. Undefined, SWI, unused, and FIQ exceptions are redirected to a hardcoded dead loop. Prefetch abort, data abort, and IRQ exception are redirected to predefined ROM handlers. Users can redirect an exception to another handler by writing its address to the appropriate location from 0x4030 D024 to 0x4030 D03C, or by overriding the branch (load into PC) instruction between addresses from 0x4030 D004 to 0x4030 D01C.

Table 27-12. RAM Exception Vectors

Address	Exception	Content
0x4030 D000	Reserved	Reserved
0x4030 D004	Undefined	PC = [0x4030D024]
0x4030 D008	SWI	PC = [0x4030D028]
0x4030 D00C	Prefetch abort	PC = [0x4030D02C]
0x4030 D010	Data abort	PC = [0x4030D030]
0x4030 D014	Unused	PC = [0x4030D034]
0x4030 D018	Interrupt request (IRQ)	PC = [0x4030D038]
0x4030 D01C	Fast interrupt request (FIQ)	PC = [0x4030D03C]
0x4030 D020	Reserved	0x30090
0x4030 D024	Undefined	0x30080
0x4030 D028	SWI	0x30084
0x4030 D02C	Prefetch abort	Address of default prefetch abort handler(1)
0x4030 D030	Data abort	Address of default data abort handler (1)
0x4030 D034	Unused	0x30090
0x4030 D038	IRQ	Address of default IRQ handler
0x4030 D03C	FIQ	0x30098

(1) The default handlers for prefetch and data abort perform reads from CP15 debug registers to retrieve the reason for the abort:
- In case of prefetch abort: the IFAR register is read from CP15 and stored into R0. The IFSR register is read and stored into the R1 register. Then the ROM code jumps to the prefetch abort dead loop (20088h).
- In case of data abort: the DFAR register is read from CP15 and stored into R0. The DFSR register is read and stored into the R1 register. Then the ROM code jumps to the data abort dead loop (2008Ch).

- Tracing data

  This area contains trace vectors reflecting the execution path of the ROM code. The public ROM code tracing data is described in Table 27-13. For more information about ROM code tracing, see Section 27.4.9, *Tracing*.

Table 27-13. Tracing Data

Address	Size (Bytes)	Description
0x4030 D040	4	Current tracing vector, word 1
0x4030 D044	4	Current tracing vector, word 2
0x4030 D048	4	Current tracing vector, word 3
0x4030 D04C	4	Cold reset run tracing vector, word 1
0x4030 D050	4	Cold reset run tracing vector, word 2
0x4030 D054	4	Cold reset run tracing vector, word 3

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Table 27-13. Tracing Data (continued)

Address	Size (Bytes)	Description
0x4030 D058	4	Current copy of the PRM_RSTST register (reset reasons)
0x4030 D05C	4	Reserved
0x4030 D060	4	Reserved
0x4030 D064	4	Reserved

- Static variables

  ROM code static variables used at boot time (and possibly during run time if calling the ROM API functions).

27.4.3 Overall Booting Sequence

Figure 27-8 shows the ROM code flow chart.

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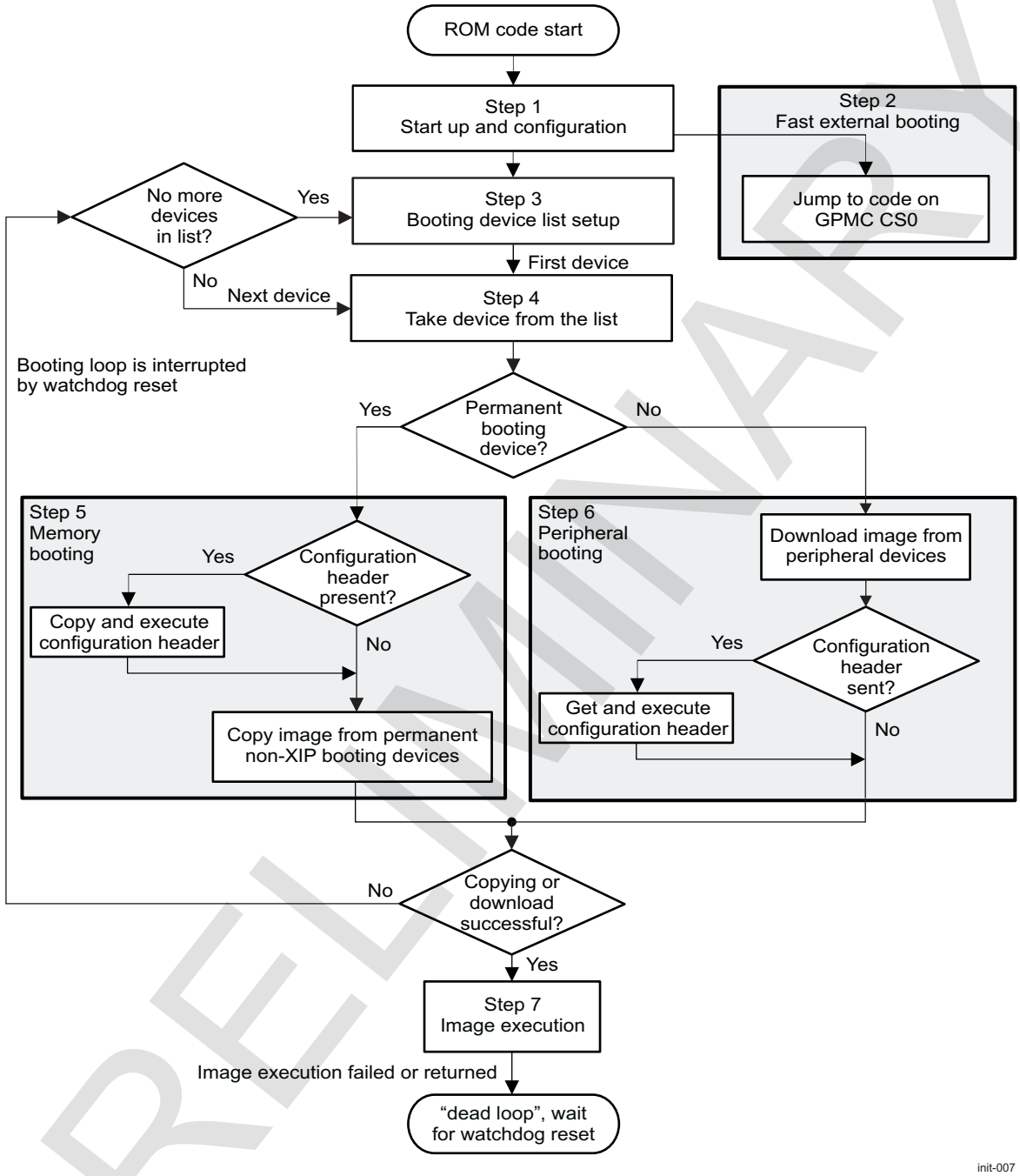
Figure 27-8. Overall Booting Sequence



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The main loop of the booting module goes through the booting device list and tries to get an image from the currently selected booting device. The ROM code performs the following steps:

Step 1. Basic configuration and initialization. Reading of SYSBOOT pins or software booting configuration

Step 2. The path named fast external boot is a special low-latency boot mode. It consists of a blind jump to an external addressable memory. See Section 27.4.6, *Fast External Booting.*

Step 3. A booting device list is created (see Section 27.4.4.3, *Booting Device List Setup*). The list consists of all devices to be searched for a booting image. The list is created based on the sys_boot pins or the software booting configuration described in Section 27.4.4.4, *Software Booting Configuration*. The software booting configuration structure is in the SAR memory and can be written by software before executing a software reset. After a software reset, the software booting configuration has priority over the sys_boot pin configuration.

Step 4. The main loop of the booting procedure goes through the booting device list and tries to search for an image from the currently selected booting device. This loop is exited if a valid booting image is found and successfully executed or when the watchdog expires. If an image is found, ROM code executes memory booting or peripheral booting, depending on the type of the current booting device:

- Memory booting is executed when the booting device is XIP memory, NAND, OneNAND/Flex-OneNAND, or eMMC/eSD/MMC/SD.
- Peripheral booting is executed when the device is a UART or USB.

Step 5. Memory booting reads data from memory-type devices. Memory booting is described in detail in Section 27.4.7, *Memory Booting*.

Step 6. Peripheral booting downloads data from communication interfaces. Peripheral booting is described in Section 27.4.5, *Peripheral Booting*.

Step 7. For the GP device, the image is automatically started.

An additional feature of the booting module is the execution of the CH. The CH configures the system for faster and more flexible booting from the selected permanent device. The CH, which is optional, is described in *Section 27.4.8.2, Configuration Header*.

27.4.4 Startup and Configuration

27.4.4.1 Startup

Figure 27-9 shows the ROM code start-up sequence.

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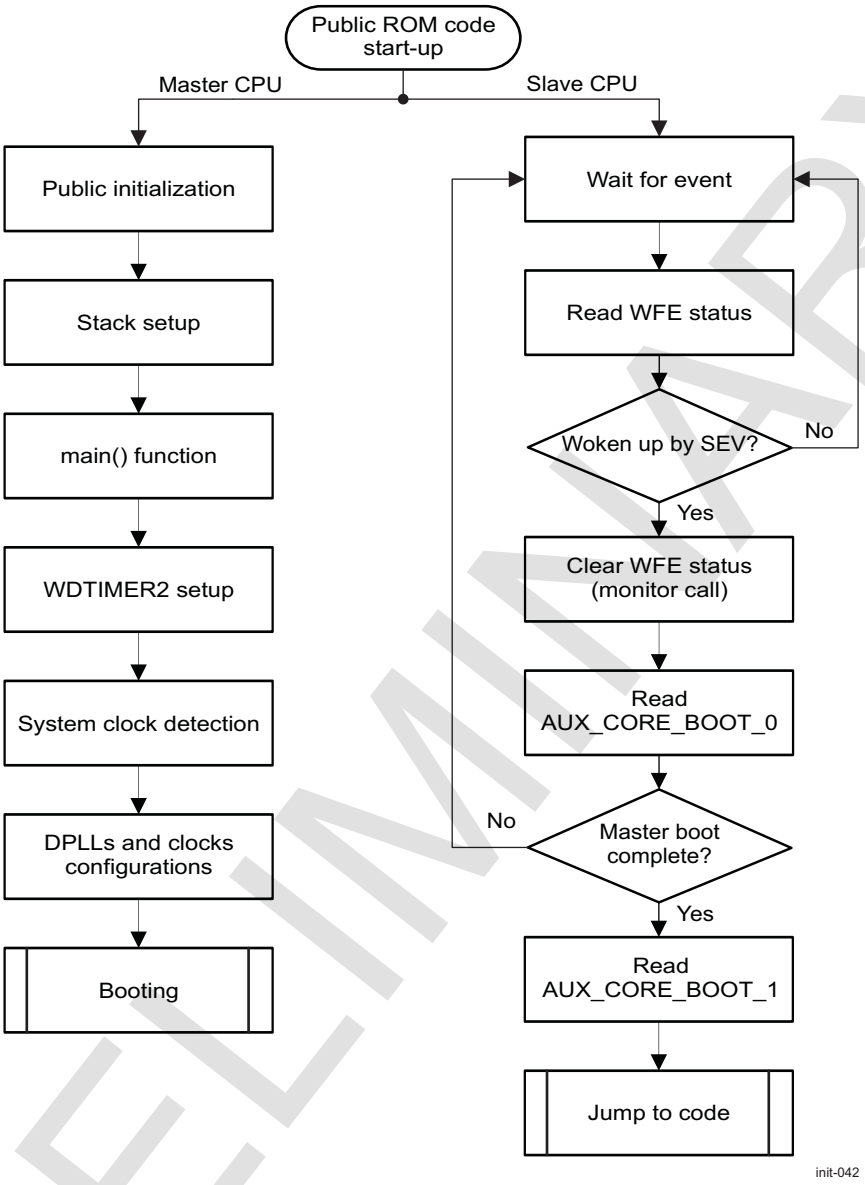
Figure 27-9. ROM Code Multiprocessor Start-Up Sequence



The master CPU L1 instruction cache and branch prediction mechanisms are activated as part of the public boot process. The public vector base address is configured to the reset vector of ROM code (0x30000). The memory management unit (MMU) remains switched off during boot (thus, L1 data cache is off). The master CPU performs the public-side basic initialization and stack setup (compiler auto-generated C- initialization or *scatter loading*. Next, it configures WDTIMER2 (set to 3 minutes), performs system clock detection, and configures the system clock. Finally, it jumps to the booting routine.

No specific configuration is performed for the slave CPU, which keeps its default configuration after reset (L1 instruction and data caches off, branch prediction off, MMU off, no remap of public-vector-base address). The slave CPU is rapidly held in wait-for-event state. It stays in this state while the master CPU completes the public boot process and until jumping to the external software (for example, HLOS). At this stage, the external software can wake up the slave CPU by executing an SEV command.

Two internal memory-mapped registers are available to the OS for communicating start-up information. The AUX_CORE_BOOT_0 and AUX_CORE_BOOT_1 registers are in the MPU WakeupGen domain.

- AUX_CORE_BOOT_0 is used as a status register to signal the slave CPU that it must wake up after the send event operation initiated by the master CPU.

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- AUX_CORE_BOOT_1 contains the address location to which the slave CPU must jump after wakeup.

See the memory mapping of these registers in Chapter 4, *Dual Cortex-A9 Subsystem*.

27.4.4.2 Clocking Configuration

The ROM code detects the system input clock frequency. The supported frequencies are:

- 12 MHz
- 16.8 MHz
- 19.2 MHz
- 26 MHz
- 38.4 MHz

After detecting the input clock, the ROM code configures the clocks and DPLLs required for ROM code execution.

The configured DPLLs are:

- Peripheral DPLL: Set to provide 192, 128, 96, 48, 24, and 12 MHz for peripheral blocks
- Core DPLL: Set to provide L3/L4 interconnect and MPU and EMIF clocks
- MPU DPLL: Left in bypass, and the MPU internal clock is derived from the core DPLL
- USB DPLL: Locked only in case of USB peripheral booting from internal transceiver. It is left unused in other cases (for example, memory boot or peripheral boot from UART or USB ULPI) to save power.

The multipliers and dividers of the DPLLs are set to values that depend on the input clock detected.

Table 27-14 summarizes the ROM code default settings for key clocks.

Table 27-14. ROM Code Default Clock Settings

Clock	Frequency [MHz]	Source
FCORE_DPLL	400	Derived from SYS_CLK
CORE_X2_CLK	200	
CORE_CLK	200	CORE_X2_CLK/1
L3_ICLK	100	CORE_CLK/2
L4_ICLK	50	L3_ICLK/2
FPER_DPLL	384	Derived from SYS_CLK
FUNC_192M_CLK	192	
FUNC_128M_CLK	128	
FUNC_96M_FCLK	96	
FUNC_48M_FCLK	48	
FMPU_DPLL (in bypass)	200	CORE_X2_CLK
MPU_DPLL_CLK	200	FMPU_DPLL/1
FUSB_DPLL (1)	960	Derived from SYS_CLK
INIT_960M	960	FUSB_DPLL/1
INIT_480M	480	INIT_960M/2
INIT_60M	60	INIT_480M/8

(1) Locked only in case of USB peripheral booting from internal PHY

There are three ways to change DPLLs and all related clock divider, gating, and multiplexer configurations during the boot:

- ROM code default settings, described in Table 27-14. They are always applied at any reset.
- Software booting configuration after a software reset, described in Section 27.4.4.4, *Software Booting Configuration*
- The CH, described in Section 27.4.8.2, *Configuration Header*. The CH lets users have a known configuration (about GPMC and clock registers) after memory booting. This configuration can be blocked by the software booting configuration.

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27.4.4.3 Booting Device List Setup

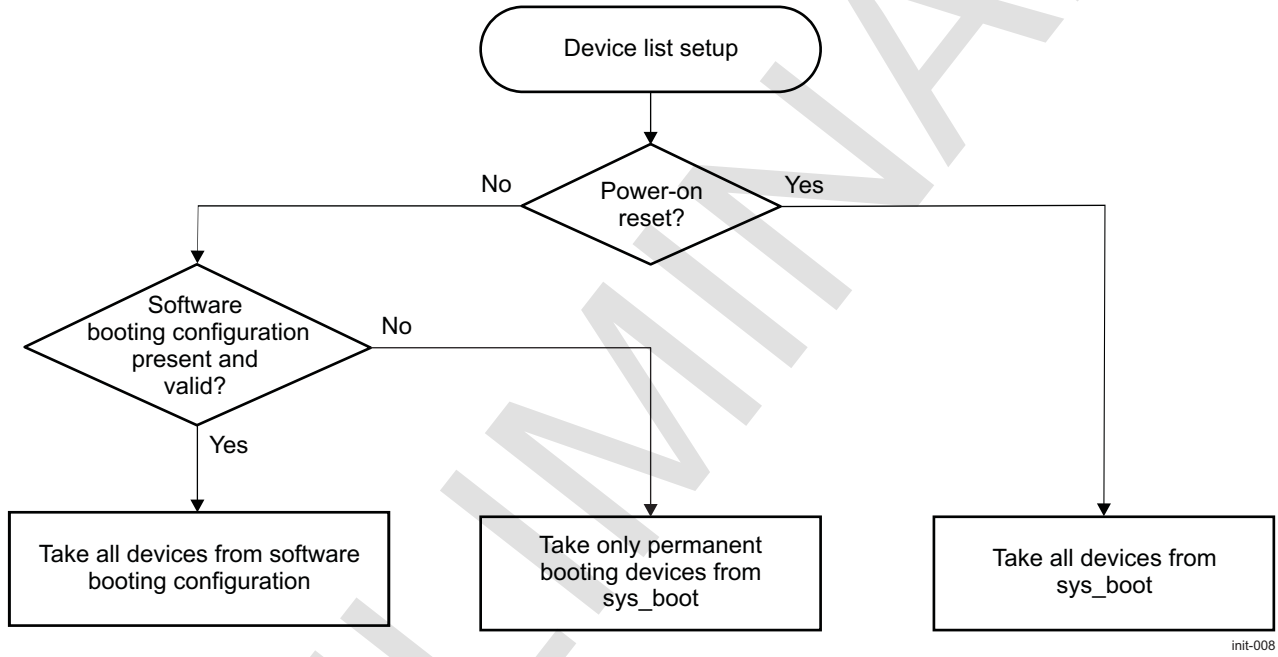
The ROM code creates a device list based on two sources:

- The software booting configuration is stored in nonvolatile RAM SAR memory.
- The sys_boot[5:0] pins sensed in the control module are used to index the device table from which the list of devices is extracted.

Figure 27-10 shows how the ROM code sets up the device list depending on the reset source.

NOTE: Only permanent booting devices are put on the list when reset is not power on and devices are taken from the sys_boot pins. Users can force peripheral booting after software reset using the software booting configuration.

Figure 27-10. Device List Setup



27.4.4.4 Software Booting Configuration

The software booting configuration is a logical structure stored in SAR RAM memory, which is not cleared after warm resets or wakeups from low-power modes.

27.4.4.4.1 Public Use of SAR RAM

At system level, the OMAP4460 SAR RAM memory is divided into four banks. The public ROM code uses only the first bank, which is always public-accessible. More specifically, the software booting configuration structure must be in the upper 1.5KB of the first bank.

The public ROM code offers some flexibility about the location of the software booting configuration structure. The PUBLIC_SW_BOOT_CFG_ADDR pointer defines the start address of the structure within the SAR RAM bank (see Table 27-15).

Table 27-15. Public Use of SAR RAM

Logical name	Address	Size (Bytes)	Description
PUBLIC_SW_BOOT_CFG_ADDR	0x4A32 6A00	4	Public software booting configuration pointer. The word value at this location is: - Reset (zero) on a cold reset. - Read on a warm reset.

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Table 27-15. Public Use of SAR RAM (continued)

Logical name	Address	Size (Bytes)	Description
CPU0_WAKEUP_NS_PA_ADDR	0x4A32 6A04	4	CPU0 nonsecure wake-up restoration pointer(1)
CPU1_WAKEUP_NS_PA_ADDR	0x4A32 6A08	4	CPU1 nonsecure wake-up restoration pointer(1)
PUBLIC_SAR_RAM_1_FREE	0x4A32 6A0C	...	Recommended address for start of software booting configuration structure described in Section 27.4.4.4.2, *Software Booting Configuration Structure*.

(1) This pointer is used as part of the restoration procedure from low-power modes.

As mentioned previously, the software booting configuration feature is optional. Hence, the public ROM code decides to use the feature based on the value read on a warm reset at the address pointed to by the PUBLIC_SW_BOOT_CFG_ADDR pointer. If the value matches the range 0x4A32 6A00–0x4A32 6FFF, the ROM code tries to extract the structure at that address. The value pointed to by PUBLIC_SW_BOOT_CFG_ADDR is always overwritten to 0 on a cold reset.

The recommended address for storing the software booting configuration structure described hereafter is defined as PUBLIC_SAR_RAM_1_FREE. It is, however, possible to locate the structure at any location within the 1.5-KB range.

It is moreover possible to use the public SAR RAM area for any other purpose, such as storing traces for HLOS use. Obviously, care must be taken not to overwrite the locations used for low-power modes and/or software booting configuration if used.

27.4.4.4.2 Software Booting Configuration Structure

Table 27-16 describes the software booting configuration structure. It offers three levels of flexibility for redefining the ROM code defaults after a warm reset:

- Redefining the default device booting list (from ROM code defaults given by SYSBOOT pins configuration)
- Redefining the default clock settings
- Redefining time-outs linked to the peripheral booting mechanism

NOTE: The sections are provided as a linked list; therefore, the order and number of items is not relevant.

The ROM code searches for the next section at the location based on the size filled in the previous section. The clock configuration from software booting configuration overwrites the CH settings.

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Table 27-16. Software Booting Configuration Structure

Field	Size (Bytes)	Description
Booting Configuration		
Section 1 key	4	Synchronization key for section 1: 0xCF00AA01
Section 1 size	4	Size of section 1: 0x0000000C (12)
Flags	2	Bits [4:1]: Mask the CH; when one of these 4 bits is set to 1, the CH item is not analyzed: [1]: SETTINGS [2]: RAM [3]: FLASH (GPMC) [4]: MMCSD Others: Reserved
1st device	2	Devices to be put into the device list 0x00: Void, no device 0x01: XIP memory 0x02: XIPWAIT memory (wait-signal monitoring on) 0x03: NAND 0x04: OneNAND 0x05: MMC1 0x06: MMC2(1) 0x07: MMC2(2) 0x43: UART 0x45: USB(1) (internal transceiver) 0x46: USB-ULPI 0x47: USB(2) (internal transceiver) Others: Reserved
2nd device	2	
3rd device	2	
4th device	2	
Padding	2	
Clock Settings		
Section 2 key	4	Synchronization key for section 2: 0xCF00AA02
Section 2 size	4	Size of section 2: 0x00000064 (100)
Flags	4	Bit mask of various switches, active when set to 1: Bit [0]: Clock configuration defined in this structure is applied. Bit [1]: Reserved Bit [2]: Apply general clock settings. Bit [3]: Set and lock PER DPLL. Bit [4]: Set and lock MPU DPLL. Bit [5]: Set and lock Core DPLL. Bit [6]: Set and lock USB DPLL. Bit [7]: Bypass PER DPLL before setting clocks. Bit [8]: Bypass MPU DPLL before setting clocks. Bit [9]: Bypass Core DPLL before setting clocks. Bit [10]: Bypass USB DPLL before setting clocks. Bit [11]: Perform DLL control configuration. Bits [31:12]: Reserved
General Clock Settings		
CM_CLKSEL_CORE	4	Register value
CM_DLL_CTRL	4	Register value
MPU DPLL Settings		
CM_AUTOIDLE_DPLL_MPU	4	Register value
CM_CLKSEL_DPLL_MPU	4	Register value

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Table 27-16. Software Booting Configuration Structure (continued)

Field	Size (Bytes)	Description
CM_DIV_M2_DPLL_MPU	4	Register value
Core DPLL Settings		
CM_AUTOIDLE_DPLL_CORE	4	Register value
CM_CLKSEL_DPLL_CORE	4	Register value
CM_DIV_M2_DPLL_CORE	4	Register value
CM_DIV_M3_DPLL_CORE	4	Register value
CM_DIV_M4_DPLL_CORE	4	Register value
CM_DIV_M5_DPLL_CORE	4	Register value
CM_DIV_M6_DPLL_CORE	4	Register value
CM_DIV_M7_DPLL_CORE	4	Register value
PER DPLL Settings		
CM_AUTOIDLE_DPLL_PER	4	Register value
CM_CLKSEL_DPLL_PER	4	Register value
CM_DIV_M2_DPLL_PER	4	Register value
CM_DIV_M3_DPLL_PER	4	Register value
CM_DIV_M4_DPLL_PER	4	Register value
CM_DIV_M5_DPLL_PER	4	Register value
CM_DIV_M6_DPLL_PER	4	Register value
CM_DIV_M7_DPLL_PER	4	Register value
USB DPLL Settings		
CM_AUTOIDLE_DPLL_USB	4	Register value
CM_CLKSEL_DPLL_USB	4	Register value
CM_DIV_M2_DPLL_USB	4	Register value
Peripheral Booting Time-out Configuration		
Section 3 key	4	Synchronization key for section 3: 0xCF00AA03
Section 3 size	4	Size of the section 3: 0x00000008 (8)
Flags	2	Bit [0]: If cleared (= 0), the time-out USB field is ignored. Bit [1]: If cleared (= 0) , the time-out boot message field is ignored. Other bits: Reserved
Time-out USB	2	Maximum time allowed for the host to complete the USB enumeration. • 0x0000: OMAP device will wait indefinitely for the host to complete USB enumeration. • Others: The value expressed in milliseconds defines the maximum time the OMAP device will wait for the host to complete the USB enumeration (maximum 65.5 s).
Time-out boot message	2	Maximum time allowed for the host to for the host to send a booting message. • 0x0000: OMAP device will wait indefinitely for the host to send a booting message. • Others: The value expressed in milliseconds defines the maximum time the OMAP device will wait for the host to send a booting message (maximum 65.5 s).
Padding	2	

27.4.5 Peripheral Booting

27.4.5.1 Description

The ROM code can boot from two different peripherals:

- USB: High-/full-speed USB from internal or external transceiver

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- UART3: 115.2 Kbps, 8 bits, even parity, 1 stop-bit

The purpose of booting from a peripheral is to download a flash loader code from an external host. This booting method is used primarily for programming flash memories connected to the OMAP device (for example, in the case of initial flashing, firmware update or servicing). The overall peripheral booting procedure is shown in Figure 27-13. It consists of a synchronization phase (handshake between host and OMAP device) and a transfer phase. The synchronization phase is similar for UART and USB boots. Both transfer phases use the same procedure.

When booting from the UART, the ROM code first initializes the UART3 interface. Then the ROM code sends an ASIC ID block of data. From there, it expects to receive a boot message from the host within 300 ms, by default. Figure 27-11 shows this procedure.

Figure 27-11. Synchronization Phase for UART

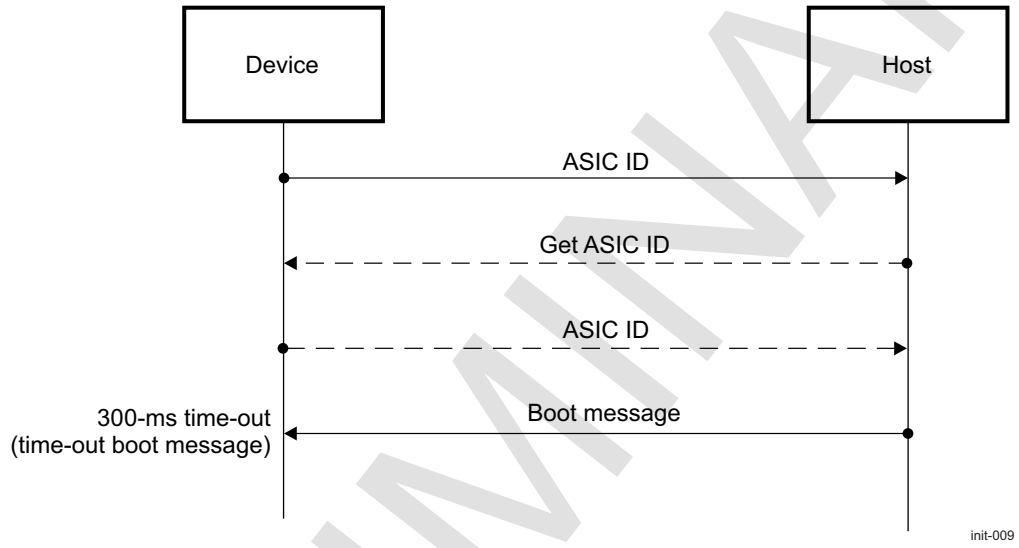
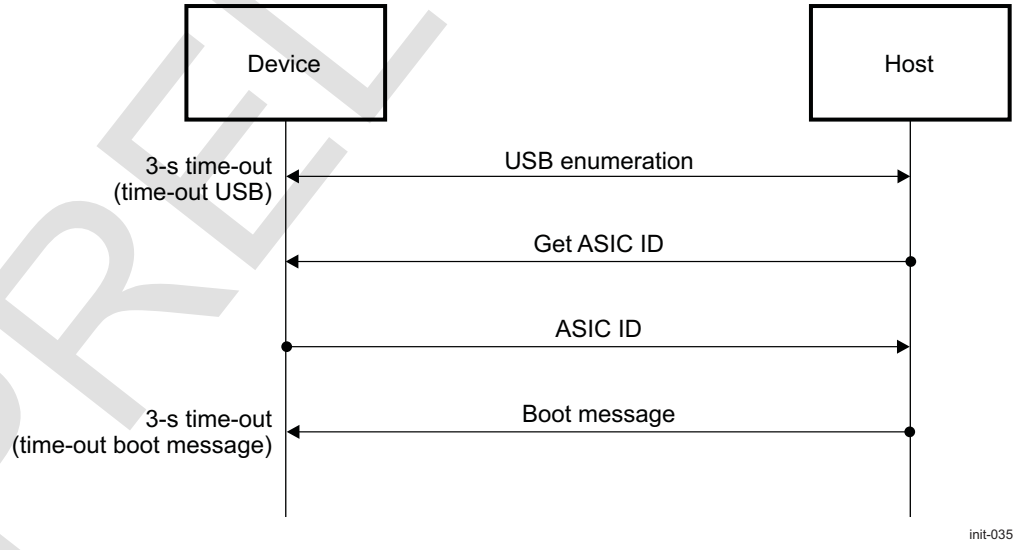


Figure 27-12 shows the procedure when booting from the USB.

Figure 27-12. Synchronization Phase for USB



During the synchronization phase (see Figure 27-11 and Figure 27-12), the OMAP device can provide a small packet of data called the ASIC ID (described in Table 27-17). It is a simple structure that contains different kinds of information, such as ROM version, checksums, and ID.

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The default time-outs involved during the synchronization phase can be redefined after a warm reset by means of the software booting configuration (described in Section 27.4.4.4, *Software Booting Configuration*). The host can decide the desired operation by providing a booting message (see Table 27-21). This message can be: Get ASIC ID, peripheral boot, change device, or next device. If the OMAP device receives the Get ASIC ID boot message, it sends back the ASIC ID contents.

If the change device or next device message is received, the ROM code stops the current peripheral booting procedure and returns to the main booting, which decides about the next booting device according to the boot message received.

If the peripheral boot message is received without a time-out, the OMAP device is entering the transfer phase. From there, the flash loader image size (as a 32-bit word) and the flash loader image itself are expected to be received. The ROM code waits up to 1 minute for completion of image size reception, and up to 1 more minute to download the image. If the download procedure does not complete before this time, the peripheral booting returns with a TIMEOUT status. ROM code continues to examine the devices included in the booting device list. If the download procedure passes, the peripheral booting returns with a SUCCESS status and the image can be executed.

The USB or UART connection is left open at the end of the transfer phase and once exiting the ROM code for the initial software to take over. It means the initial software can reuse the currently established connection. In the case of a USB connection, the endpoints can be reused as such, without closing the connection and performing a full enumeration again.

Table 27-17. ASIC ID Structure

ASIC ID Item	Size (Bytes)	Description
Items	1	Number of subblocks
ID subblock	7	Device identification information
Reserved subblock	4	This subblock is transmitted, but does not contain useful information in case of GP device.
Reserved subblock	23	This subblock is transmitted, but does not contain useful information in case of GP device.
Reserved subblock	35	This subblock is transmitted, but does not contain useful information in case of GP device.
Checksum subblock	11	CRC (4 bytes)

Table 27-18. Items

Offset	Size (Bytes)	Description
0x00	1	0x05: Number of subblocks USB 0x04: Number of subblocks UART(1)

(1) The checksum subblock is not transmitted over the UART.

Table 27-19. ID Subblock

Offset	Size (Bytes)	Description
0x01	1	0x01: Subblock ID
0x02	1	0x05: Subblock size
0x03	1	0x01: Fixed value
0x04	2	0x44, 0x40: OMAP4460 device
0x06	1	0x07: CH enabled (read from eFuse) 0x17: CH disabled (read from eFuse)
0x07	1	ROM revision

Table 27-20. Checksum Subblock(1)

Offset	Size (Bytes)	Description
0x46	1	0x15: Subblock ID

(1) The checksum subblock is not transmitted over the UART.

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Table 27-20. Checksum Subblock[1] (continued)

Offset	Size (Bytes)	Description
0x47	1	0x09: Subblock size
0x48	1	0x01: Fixed value
0x49	4	ROM CRC
0x4D	4	0x00000000: For GP device

Table 27-21. Booting Messages

Message Name	Value	Description
Peripheral boot	0xF003 0002	Continue peripheral booting.
Get ASIC ID	0xF003 0003	ASIC ID request. The Get ASIC ID request message is optional. If received, the ROM code sends its ASIC ID data to the host in return. The host can issue the Get ASIC ID message multiple times if required. The structure of the ASIC ID is described in Table 27-17.
Change device	0xF003 xx06	Skip current peripheral booting and continue booting from device type indicated by xx: 0x00: Void, no device 0x01: XIP memory 0x02: XIPWAIT memory (wait-signal monitoring on) 0x03: NAND 0x04: OneNAND 0x05: MMC1 0x06: MMC2(1) 0x07: MMC2(2) 0x43: UART 3 0x45: USB(1) (internal transceiver) 0x46: USB-ULPI 0x47: USB(2) (internal transceiver) Others: Reserved
Next device	0xFFFF FFFF	Skip current device and move to the next device on the device list.
Memory booting	Others	Skip current peripheral booting and move to the first device for memory booting.

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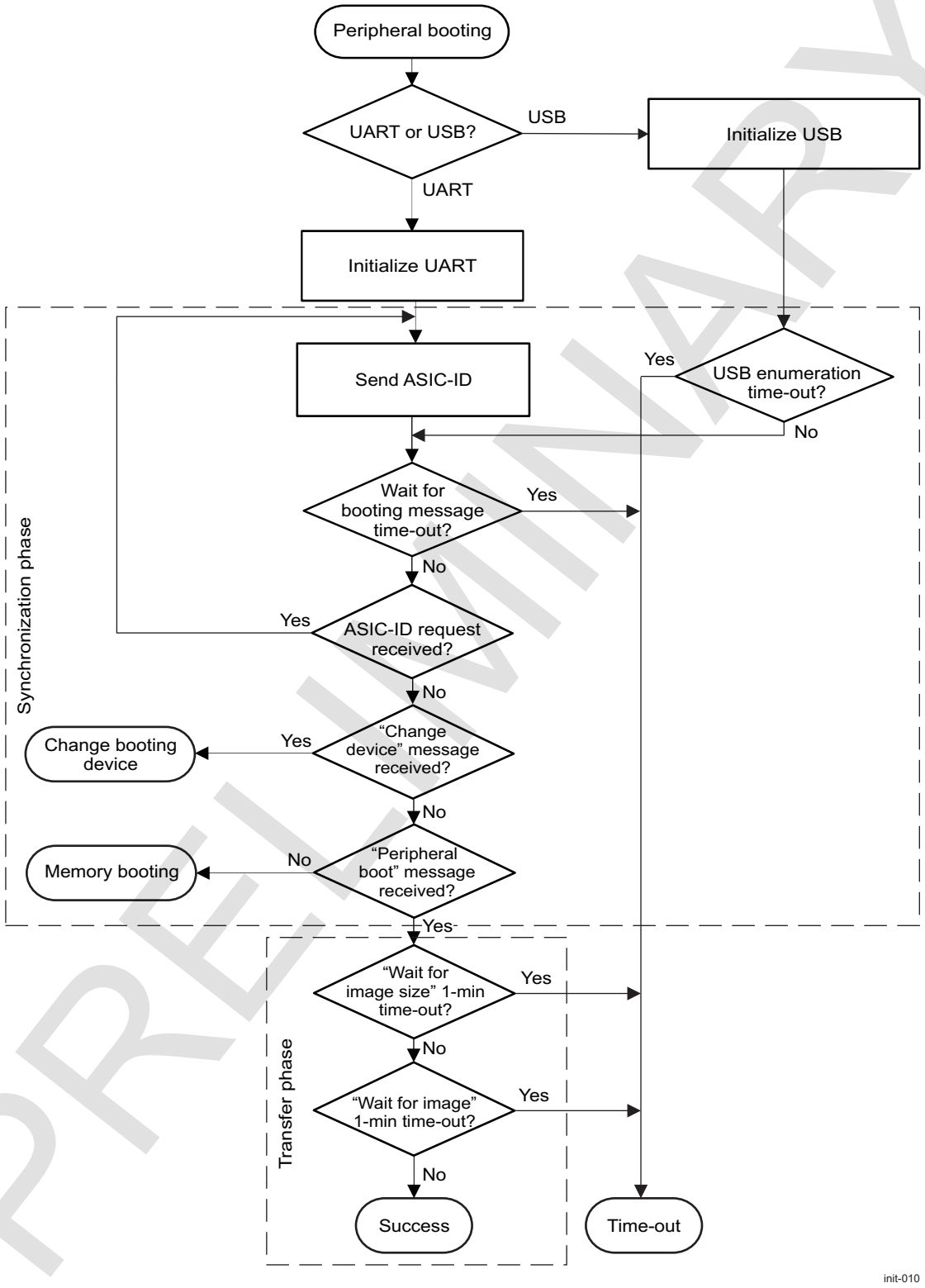
Figure 27-13 shows the peripheral booting procedure.

Figure 27-13. Peripheral Booting Procedure



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27.4.5.2 UART

The ROM code supports booting from a UART interface with the following characteristics:

- UART interface 3
- Communication parameters set to 115.2 Kbps, 8 bits, even parity, 1 stop-bit
- Two-pin interface: RX/TX
- The boot message default time-out is 300 ms (time-out boot message)

27.4.5.3 USB

The ROM code supports booting from a USB interface with the following characteristics:

- HSUSBOTG interface (USBA0)
- OMAP integrated transceiver (USBPHY) or external transceiver through the ULPI
- Enumeration default time-out is 3 s (time-out USB)
- The boot message default time-out is 3 s (time-out boot message).

NOTE: Even though using OTG-capable hardware, the ROM code does not handle any OTG-specific features.

27.4.5.3.1 Overview

Figure 27-14 shows the USB initialization procedure.

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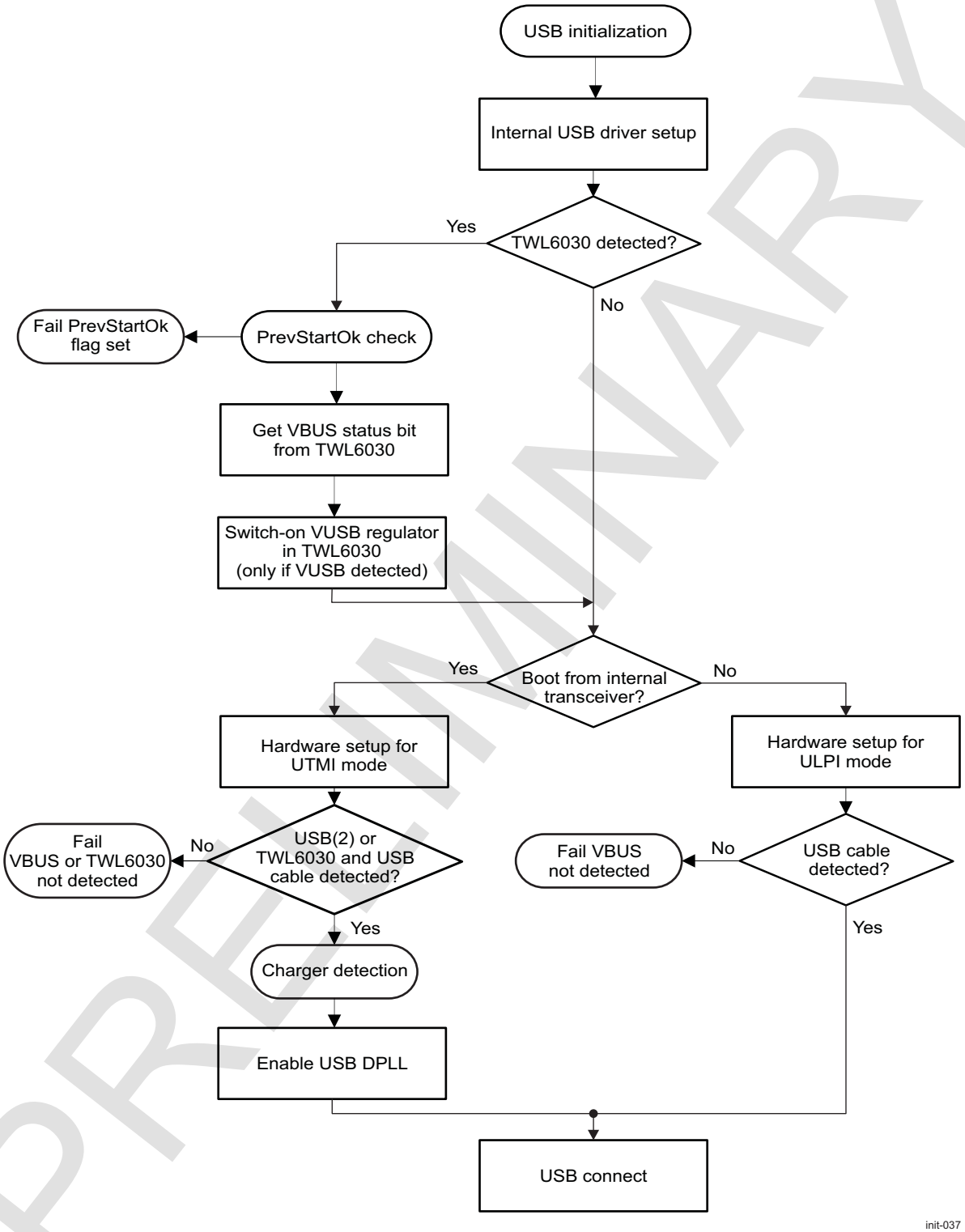
Figure 27-14. USB Initialization Procedure



After internal USB module driver setup, the TWL6030 power IC is checked for presence. If found, the following actions are performed using I^2C transactions through the I2C1 interface:

- PrevStartOk status flag check, as described in Section 27.4.5.3.2.
- Get the VBUS status reflecting presence (or not) of the USB cable

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- If VBUS was detected, then the VUSB regulator is enabled to power the internal OMAP transceiver.

In case of boot from external transceiver in accordance with the chosen SYSBOOT configuration:

- The HSUSBOTG hardware and PRCM clocks are configured for ULPI mode.
- The ROM code continues with the USB procedure only if the USB cable is detected (that is, VBUS is detected at external transceiver level and communicated as such through the ULPI traffic). If not, the initialization procedure is aborted.

NOTE: The OMAP USB DPLL is not set up in case of ULPI mode, for which the 60-MHz clock is driven by the external transceiver.

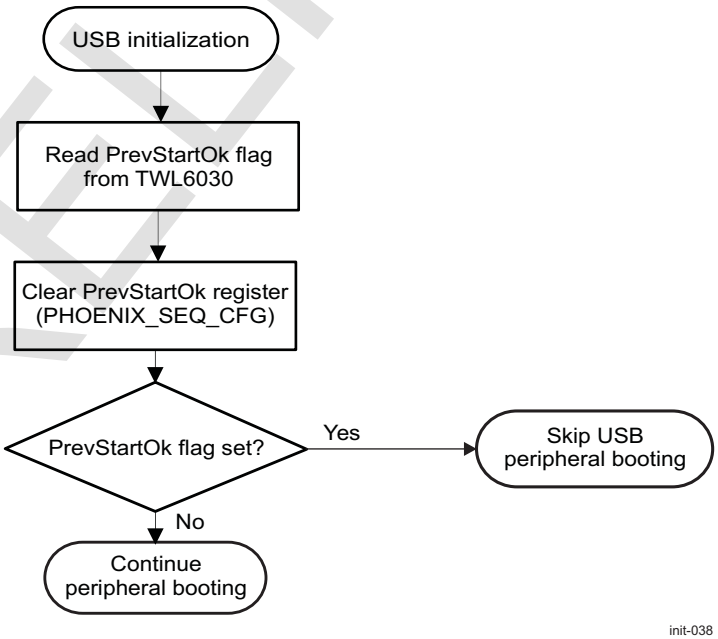
In case of boot from internal transceiver in accordance with the chosen SYSBOOT configuration:

- The USBOTGHS hardware and PRCM clocks are configured for UTMI mode and internal PHY clocks are enabled.
- For USB(1) only: The ROM code continues with the USB procedure only if the TWL6030 is detected and the USB cable is detected as present (that is, VBUS is detected at the TWL6030 level and read as such with a register read through I2C interface). If not, the initialization procedure is aborted.
- For USB(2) only: The ROM code continues with the USB procedure even if the TWL6030 is not detected and the USB cable is not detected as present at the TWL6030 level. This enables a USB boot with internal transceiver even without the TWL6030.
- The ROM code proceeds with charger detection, as described in Section 27.4.5.3.2.
- It enables the USB DPLL for feeding the appropriate 60-MHz clock needed by the internal transceiver.

27.4.5.3.2 PrevStartOk Status Flag Check

The ROM code supports a mechanism for avoiding the boot time spent because of the enumeration time-out (default 3 s) in case the USB cable is attached and the USB option is present in the selected boot list but is not intended to initiate a peripheral booting procedure (for example, firmware update or flashing). This mechanism is jointly handled with the support of the TWL6030 device (not supported if TWL6030 is not detected). This mechanism is supported only for USB and not UART (see Figure 27-15).

Figure 27-15. PrevStartOk Mechanism



The ROM code first checks the value of a register in the TWL6030 RTC domain (hence, retained by the backup battery when the platform is switched off) by an I^2C read access. If the PrevStartOk bit in this register is set, the USB peripheral booting is simply skipped. In any case, the bit is reset (zeroed) by the

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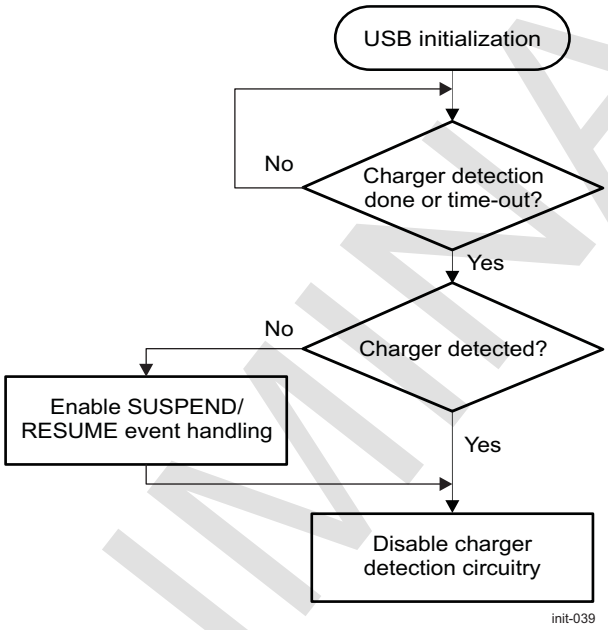
ROM code, which means that the USB peripheral boot is re-enabled on the next cold reset (or warm reset if suitable software booting configuration is present). The initial software of the user must reset this bit by an I^2C write access to disable USB peripheral booting on a subsequent reset. For more information about the accesses made toward the PrevStartOk bit in the PHOENIX_SEQ_CFG register, see TWL6030 documentation.

27.4.5.3.3 Charger Detection

The ROM code proceeds with charger detection as part of the USB peripheral booting procedure and in compliance with *Battery Charging Specification Revision 1.1*. It uses the specific charger detection hardware embedded in the OMAP device. Figure 27-16 shows the high-level procedure.

Figure 27-16. Charger Detection



The hardware charger detection mechanism should end up within the 500-ms time-out. The main goal of such detection is to gate the charger circuitry in TWL6030 in case a charger is not detected and a suspend event is detected on the OMAP side, for which the power consumption must be reduced.

27.4.5.3.4 SUSPEND and RESUME Handling

The SUSPEND event is detected by the HSUSBOTG module when activity on the bus stops for at least 3 ms. During peripheral booting time, a SUSPEND event is detected by the ROM code and processed by initiating a write into the TWL6030 to gate the charging circuitry. The ROM code releases the TWL6030 charger circuitry upon getting a RESUME event. During run time, SUSPEND and RESUME interrupts can be routed to the initial software to define custom handling.

27.4.5.3.5 USB Driver Descriptors

USB devices report their attributes using descriptors. A descriptor is a data structure with a defined format. Each descriptor begins with a byte-wide field that contains the total number of bytes in the descriptor followed by a byte-wide field that identifies the descriptor type. Using descriptors allows concise storage of the attributes of individual configurations so that each configuration can reuse descriptors or portions of descriptors from other configurations that have the same characteristics. Where appropriate, descriptors contain references to string descriptors. String descriptors contain displayable, human-readable description information. These descriptor details can be used for tool development or debugging:

- Device descriptor

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A device descriptor contains general information about a USB device, including global information that applies to the device and all device configurations. A USB device has only one device descriptor. A device-qualifier descriptor is required because the ROM code uses the HS feature of the USB core. Table 27-22 lists the device descriptors.

Table 27-22. Device Descriptor

Field	Value	Description
bLength	0x12	Size of this descriptor in bytes
bDescriptorType	0x01	Device descriptor type
bcdUSB	0x0210	USB specification release number in binary coded decimal (BCD) format
bDeviceClass	Vendor-specific (0xFF)	Class code
bDeviceSubClass	Vendor-specific (0xFF)	Subclass code
bDeviceProtocol	Vendor-specific (0xFF)	Protocol code
bMaxPacketSize0	0x40	Maximum packet size for endpoint 0
idVendor	0x0451	Vendor ID (Texas Instruments), TI default value
idProduct	0xD010	Product ID (OMAP4460), TI default value
bcdDevice	0x0000	Device release number
iManufacturer	See Section 27.4.5.3.6.	Index of string descriptor describing manufacturer
iProduct	See Section 27.4.5.3.6.	Index of string descriptor describing product
iSerialNumber	See Section 27.4.5.3.6.	Index of string descriptor describing device serial number
bNumConfigurations	0x01	Number of possible configurations

- Device-qualifier descriptor

  The device-qualifier descriptor contains information about a HS-capable device that changes if the device operates at its other speed. This descriptor is retrieved by the host using the GetDescriptor() request (standard device request). Table 27-23 describes a device-qualifier descriptor.

Table 27-23. Device-Qualifier Descriptor

Field	Value	Description
bLength	0x0a	Size of this descriptor in bytes
bDescriptorType	0x06	Device-qualifier descriptor type
bcdUSB	0x0210	USB specification release number in BCD
bDeviceClass	0xFF	Class code
bDeviceSubClass	0xFF	Subclass code
bDeviceProtocol	0xFF	Protocol code
bMaxPacketSize0	0x40	Maximum packet size for endpoint 0
bNumConfigurations	0x01	Number of possible configurations
bReserved	0x00	Reserved for future use

- Configuration descriptor

  This descriptor gives information about a specific device configuration. It describes the number of interfaces supported by the configuration (see Table 27-24).

Table 27-24. Configuration Descriptor

Field	Value	Description
bLength	0x09	Size of this descriptor in bytes
bDescriptorType	0x02	Configuration descriptor type
wTotalLength	–	Combined length of all descriptors
bNumInterfaces	0x01	Number of interfaces supported
bConfigurationValue	0x01	Value to use as an argument for the SetConfiguration() request
iConfiguration	Index	Index of string descriptor describing this configuration

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Table 27-24. Configuration Descriptor (continued)

Field	Value	Description
bmAttributes	0xC0	Power setting and remote wakeup
bMaxPower	0x32	Maximum power consumption of the USB device

- Other speed configuration descriptor

  This descriptor describes the configuration of a HS-capable device if it operates at its other possible speed (see Table 27-25).

Table 27-25. Other Speed Configuration Descriptor

Field	Value	Description
bLength	0x09	Size of this descriptor in bytes
bDescriptorType	0x07	Other speed configuration descriptor type
wTotalLength	–	Combined length of all descriptors
bNumInterfaces	0x01	Number of interfaces supported
bConfigurationValue	0x01	Value to use as an argument for the SetConfiguration() request
iConfiguration	Index	Index of string descriptor describing this configuration
bmAttributes	0xC0	Power setting and remote wakeup
bMaxPower	0x32	Maximum power consumption of the USB device

- Interface descriptor

  This descriptor describes a specific interface in a configuration (see Table 27-26).

Table 27-26. Interface Descriptor

Field	Value	Description
bLength	0x09	Size of this descriptor in bytes
bDescriptorType	0x04	Interface descriptor type
bInterfaceNumber	0x00	Number of this descriptor
bAlternateSetting	0x00	Value to select the alternate setting
bNumEndpoints	0x02	Number of endpoints used for this interface
bInterfaceClass	0xFF	Class code
bInterfaceSubClass	0xFF	Subclass code
bInterfaceProtocol	0xFF	Protocol code
iInterface	Index	Index of string descriptor describing this interface

- Endpoint descriptor

  Each endpoint used for an interface has its own descriptor. This descriptor contains information required by the host to determine the bandwidth requirements of each endpoint. This descriptor is returned as part of the GetDescriptor(Configuration) request (see Table 27-27 and Table 27-28).

Table 27-27. BULK IN Endpoint Descriptor

Field	Value	Description
bLength	0x07	Size of this descriptor in bytes
bDescriptorType	0x05	Endpoint descriptor type
bEndpointAddress	0x81 (1 IN)	Address of the endpoint on the USB device
bmAttributes	0x02 (Bulk)	Type of transfer
wMaxPacketSize	See (1).	Number of endpoints used for this interface
bInterval	0x00	Maximum NAK rate

(1) The maximum size is 0x0200 (512 bytes) for HS bulk endpoint and 0x0040 (64 bytes) for FS bulk endpoint.

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Table 27-28. BULK OUT Endpoint Descriptor

Field	Value	Description
bLength	0x07	Size of this descriptor in bytes
bDescriptorType	0x05	Endpoint descriptor type
bEndpointAddress	0x01 (1 OUT)	Address of the endpoint on the USB device
bmAttributes	0x02 (Bulk)	Type of transfer
wMaxPacketSize	See (1).	Number of endpoints used for this interface
bInterval	0x00	Maximum NAK rate

(1) The maximum size is 0x0200 (512 bytes) for HS bulk endpoint and 0x0040 (64 bytes) for FS bulk endpoint.

- String descriptors

  String descriptors use UNICODE encoding. The strings in a USB device can support multiple languages. When requesting a string descriptor, the requester specifies the desired language using a 16-bit language ID (LANGID) defined by the USB interface. String index 0 for all languages returns a string descriptor that contains an array of 2-byte LANGID codes supported by the device.

  For the description of the different string descriptors, see:

  – The language ID string descriptor (Table 27-29)
  – The manufacturer ID string descriptor (Table 27-30)
  – The product ID string descriptor (Table 27-31)
  – The configuration string descriptor (Table 27-32)
  – The interface string descriptor (Table 27-33)

Table 27-29. Language ID String Descriptor

Field	Value	Description
bLength	0x04	Size of this descriptor in bytes
bDescriptorType	0x03	String descriptor type
wLangId	0x0409 (US English)	Language ID code

Table 27-30. Manufacturer ID String Descriptor

Field	Value	Description
bLength	0x24	Size of this descriptor in bytes
bDescriptorType	0x03	String descriptor type
bString	Texas Instruments	Manufacturer string

Table 27-31. Product ID String Descriptor

Field	Value	Description
bLength	0x12	Size of this descriptor in bytes
bDescriptorType	0x03	String descriptor type
bString	OMAP4440	Product string

Table 27-32. Configuration String Descriptor

Field	Value	Description
bLength	0x08	Size of this descriptor in bytes
bDescriptorType	0x03	String descriptor type
bString	pbc	Configuration string

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Table 27-33. Interface String Descriptor

Field	Value	Description
bLength	0x08	Size of this descriptor in bytes
bDescriptorType	0x03	String descriptor type
bString	pbi	Interface string

27.4.5.3.6 USB Customized Descriptors

There are two parameters in USB descriptors that customers can define after the chip is created: vendor ID (VID) and product ID (PID). The ROM code uses dedicated eFuses that hold VID and PID values. Other parameters can also be changed based on the VID value. The ROM code has an encoded set of parameters for customers who have defined their requirements before the ROM code has been done. Table 27-34 lists the parameters that depend on the VID value.

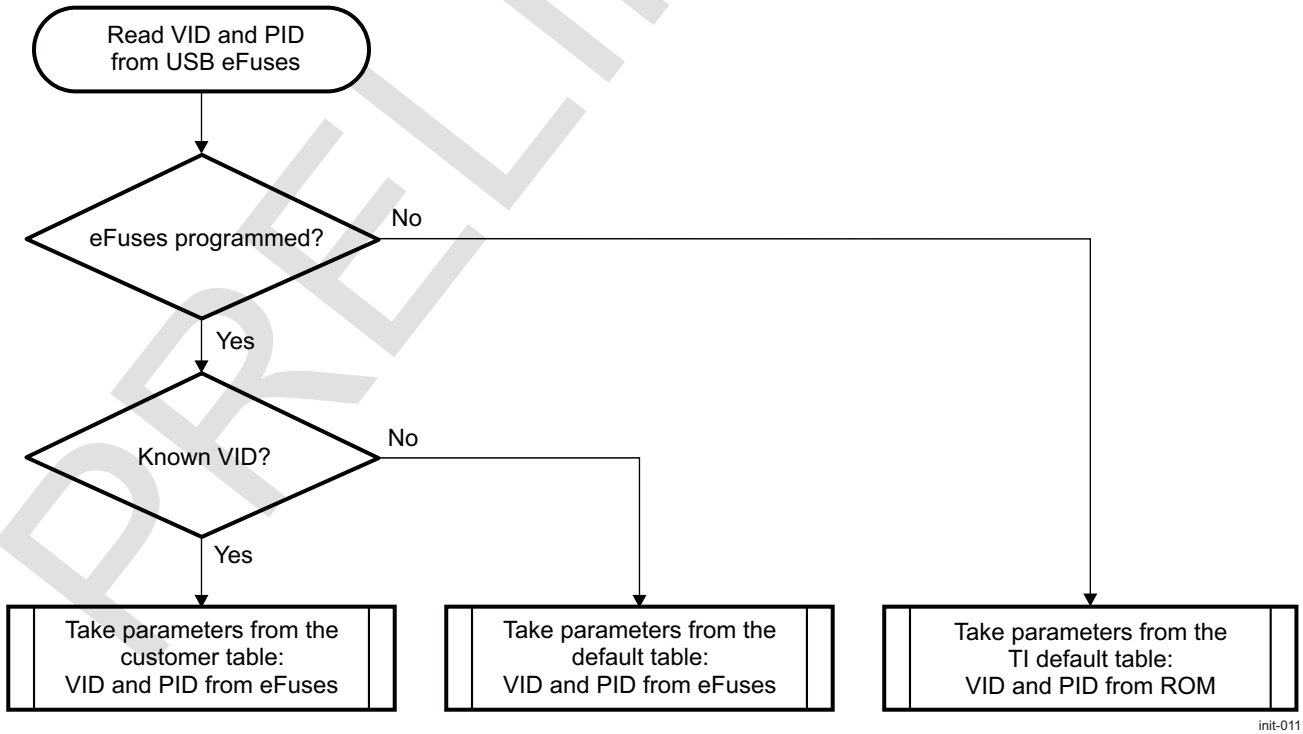
Table 27-34. Customized Descriptor Parameters

Parameter	Size (Bytes)	Default Values (From eFuses)	TI Default Values (From ROM)
Device ID code	2	0x0000	0x0000
Device class	1	0xFF	0xFF
Device subclass	1	0xFF	0xFF
Device protocol	1	0xFF	0xFF
Manufacturer	String	N/A	Texas Instruments
Product	String	OMAP4440	OMAP4440
Serial number	String	See(1).	See(1).

(1) The standard device descriptor indicates that the device has no serial number.

Figure 27-17 shows an additional customer parameter selection method. It is based on the VID burned in the USB eFuses.

Figure 27-17. Customer USB Descriptor Selection



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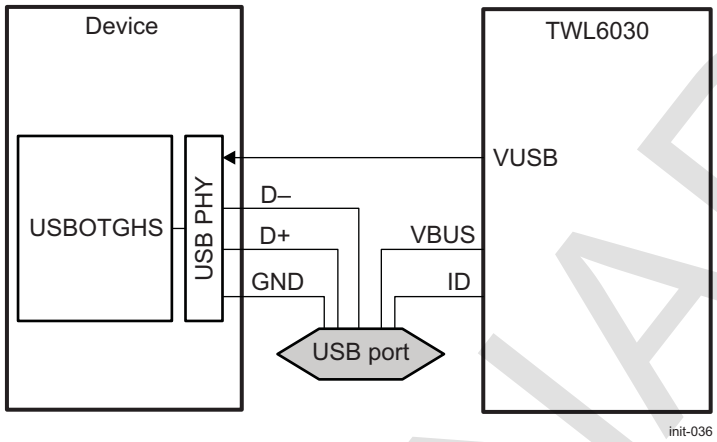
27.4.5.3.7 System Interconnection – Integrated Transceiver

When SYSBOOT selects the embedded PHY, the USB power/data path can be described as shown in Figure 27-18.

Figure 27-18. USB System Using Internal Transceiver



NOTE: USB(2) booting mode allows an alternate power-management IC to be used. In that case, the internal transceiver must be powered and configured upon startup and does not require any action from the ROM code for its configuration.

27.4.5.3.8 System Interconnection – External Transceiver

The USBOTGHS module uses the ultralow-pin-count interface (ULPI) to interconnect with an external USB transceiver. In this case, the ROM code does not interact with the transceiver. Thus, users must ensure that the transceiver power supply and clock are present and the transceiver is out of reset.

27.4.5.3.9 USB Driver Functionality

- Transactions supported:
  - Control transactions: Used for standard device requests
  - Bulk transactions: Used for data transfer in the image downloading stage. The ASIC ID is sent to the BULK IN endpoint and the image is transferred from the host over the BULK OUT endpoint.

  The OMAP USB device first attaches to the host as an FS device. In the reset mechanism, the USB core requests HS operation. If the HS negotiation in the reset phase is successful, further transactions are at HS; otherwise, they are at FS. After reset, the USB driver checks for the speed of the device, whether it is FS or HS. Depending on the speed configured by the host, the standard USB device requests are answered with the corresponding descriptors.
- Standard device request restrictions:

  Some standard device requests are not supported by the driver because the USB driver is dedicated for use by the ROM code for peripheral booting. Table 27-35 lists the standard device requests supported by the driver.

Table 27-35. Standard Device Requests Supported

Request	Description	Support
CLEAR_FEATURE	Sets/clears a specific feature	Supported only for ENDPOINT_HALT feature
GET_CONFIGURATION	Returns the current device configuration value	Yes
GET_DESCRIPTOR	Returns the specified descriptor	Yes
GET_INTERFACE	Returns the selected alternate setting for the specified interface	Yes
GET_STATUS	Returns the status for the specified recipient	Yes

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Table 27-35. Standard Device Requests Supported (continued)

Request	Description	Support
SET_ADDRESS	Sets the device address	Yes
SET_CONFIGURATION	Sets the device configuration	Yes
SET_DESCRIPTOR	Updates existing descriptors or adds new descriptors	Runtime updating of descriptors is not supported.
SET_FEATURE	Sets or enables a specific feature	Supported only for ENDPOINT_HALT feature
SET_INTERFACE	Selects an alternate setting in an interface	Runtime setting of alternate features is not supported.
SYNCH_FRAME	Sets and reports an endpoint synchronization frame	No, because isochronous transfers are not used

27.4.6 Fast External Booting

27.4.6.1 Overview

The fast external boot is a special memory booting mode, possible only on GP devices. It consists of a blind jump to a code in an external XIP memory device connected to GPMC CS0. Fast external booting is set up by means of the SYSBOOT configuration pins and lets customers create their own booting code.

The jump is performed with minimum on-chip ROM code execution.

27.4.6.2 Fast External Booting Procedure

Figure 27-19 shows the fast external boot procedure. The code is at the beginning and is written in Assembly Language. The code does not use any RAM and is designed for fast execution.

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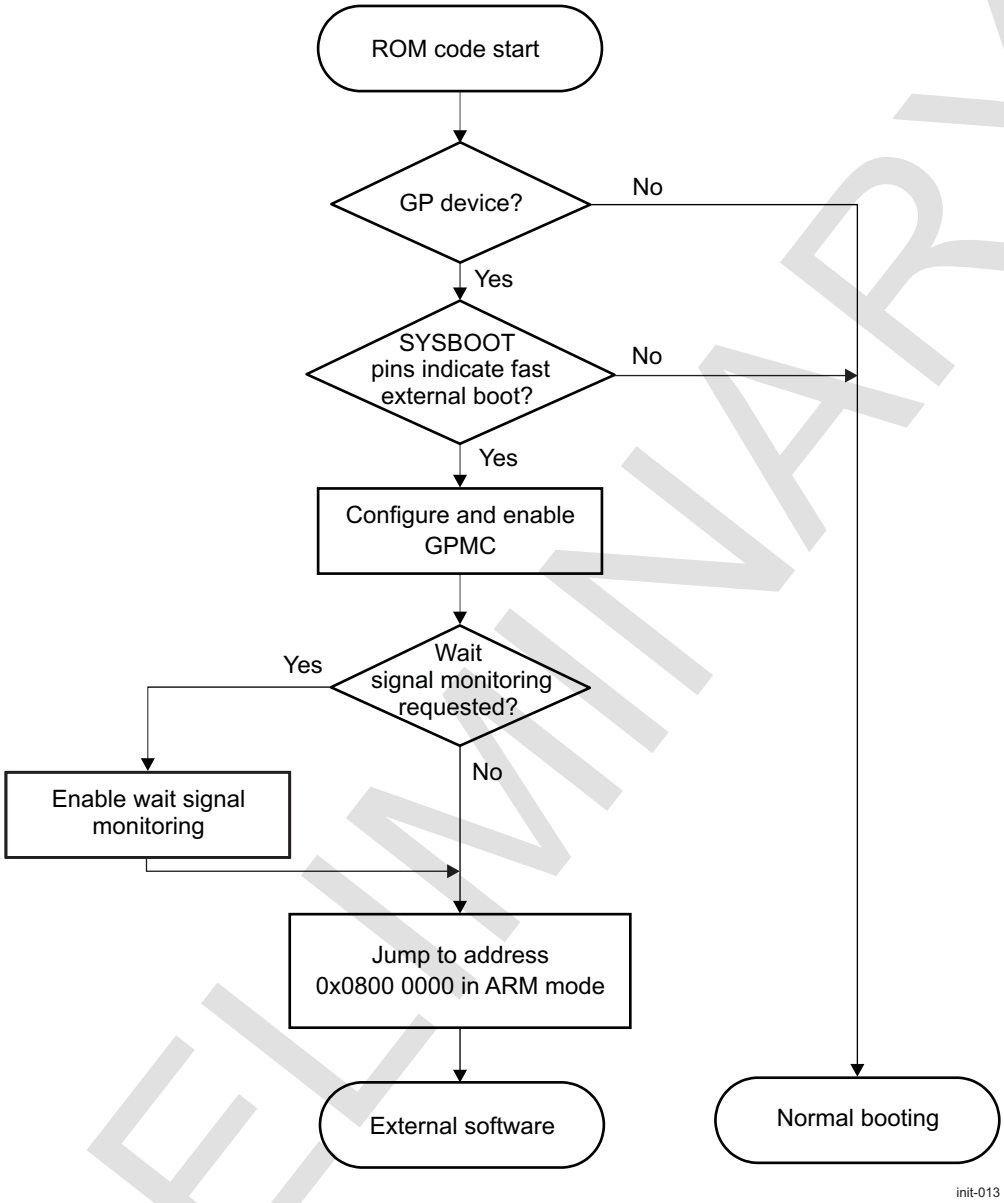
Figure 27-19. Fast External Boot Procedure



27.4.7 Memory Booting

27.4.7.1 Overview

The memory booting process starts an external code in memory devices. Only memory type of booting devices can be used by ROM code as permanent booting devices (that is, devices examined after both cold (POR) and warm resets). Temporary booting devices are examined only after cold resets. The supported permanent booting devices are:

- NOR flash devices
- NAND flash devices
- OneNAND/Flex-OneNAND devices
- eMMC/eSD embedded flash memories
- SD/MMC flash cards

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Two main groups of permanent booting devices are distinguished by code shadowing. Code shadowing means copying code from a nondirectly addressable device (non-XIP) to RAM, where the code can be executed. Directly addressable devices are XIP devices.

Figure 27-20 shows the general memory booting procedure common to all types of devices. First, CH is copied to internal RAM. It is copied even for XIP devices, because the OMAP device can temporarily lose a connection with XIP memory during CH execution. The second step is to shadow the image, if the device is not XIP. The last step is image execution and any return from image results in a dead loop.

If CH copying or shadowing fails, memory booting returns to the main booting procedure, which selects the next device for booting.

During the first read sector (512 bytes) call, sectors are copied to a temporary RAM buffer. Once the image is found and the destination address is known, the content of the temporary buffer is moved to the target RAM location so it is required to reread the first image sector. On a GP device, the GP header is discarded; therefore, only executable code is in RAM, with the first executable instruction at the destination address.

eMMC/eSD embedded memories, MMC/SD cards, NAND, and OneNAND/Flex-OneNAND devices can hold up to four copies of the booting image. Therefore, the ROM code searches for one valid image out of the four, if present, by walking over the first blocks of mass storage space. Other XIP devices (NOR) use only one copy of the booting image.

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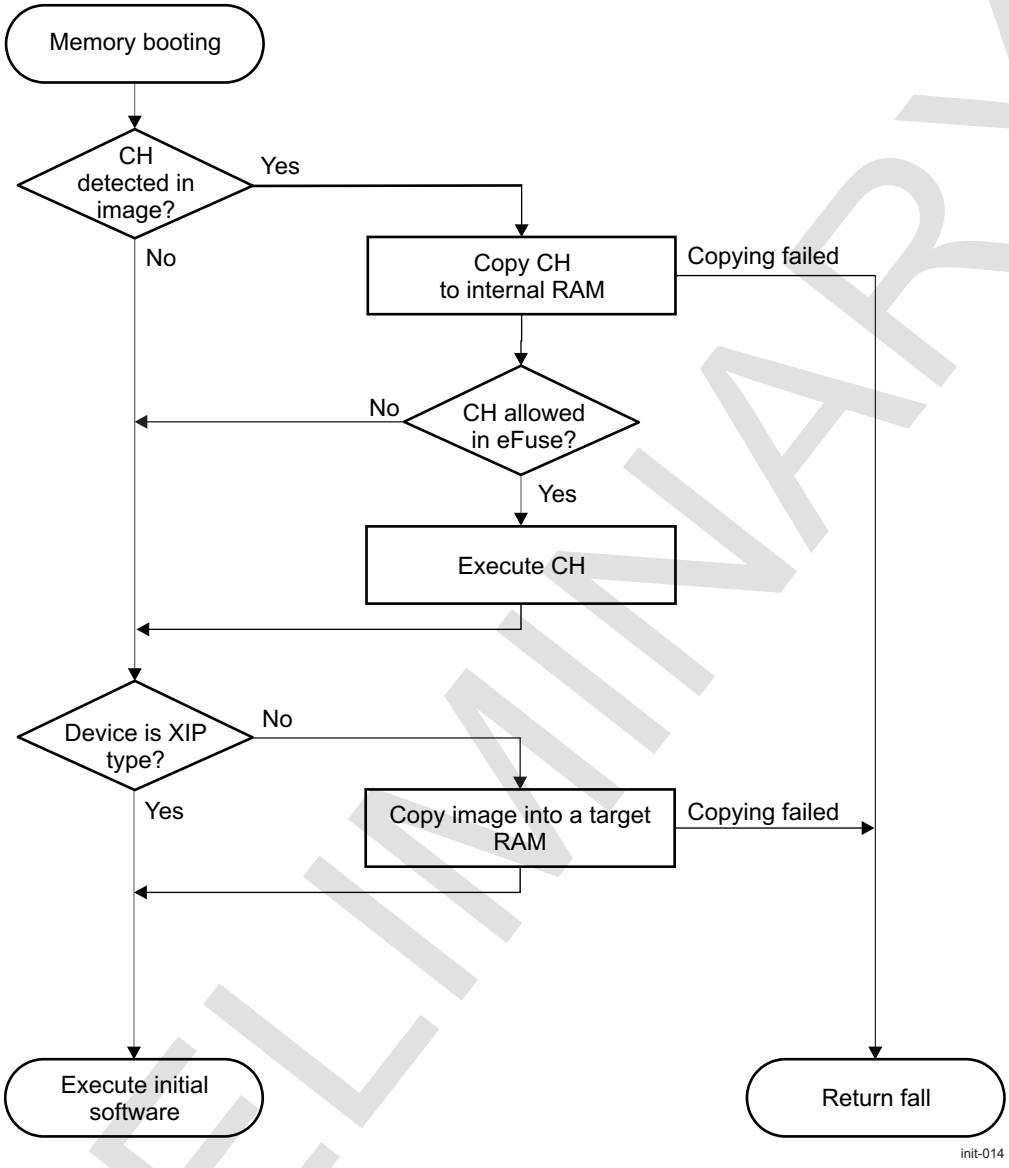
Figure 27-20. Memory Booting Procedure



27.4.7.2 Non-XIP Memory

Figure 27-21 shows the procedure used when memory booting runs with non-XIP devices. The shaded procedures are specific to each device. NAND and OneNAND/Flex-OneNAND devices use up to four copies of the image in the first four physical blocks. Therefore, the ROM code searches for the image in the first four physical blocks of these devices. Other devices use only one copy of the image and the block loop runs only once.

During image shadowing on a GP device, the CH is expected to be in a separate sector before the initial software.

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Figure 27-21. Image Shadowing on GP Device

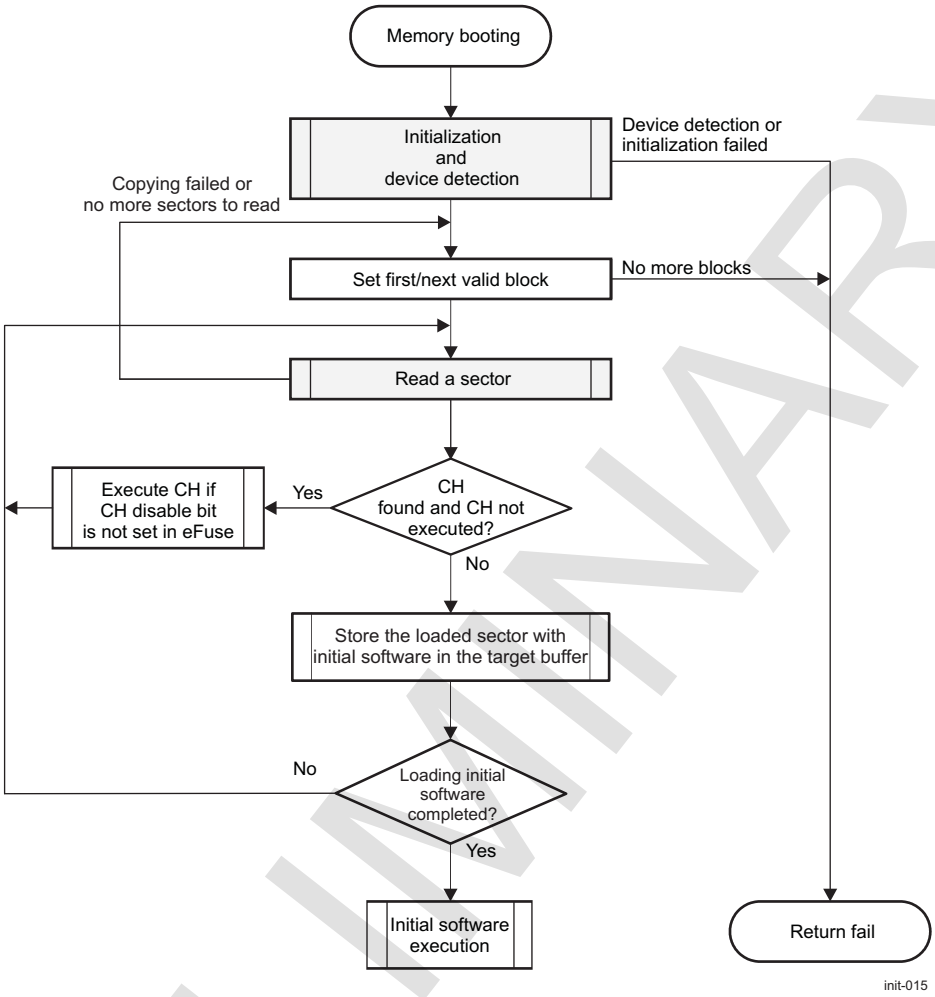

Table 27-36 summarizes the number of blocks and sectors searched during memory booting from devices requiring image shadowing. A sector is assumed to be 512 bytes long. NANDs and OneNAND/Flex-OneNAND are organized with blocks, which are erasable units. MMC/SD/eMMC/eSD + FAT12/16/32 booting consists of reading a file.

Table 27-36. Blocks and Sectors Searched on Non-XIP Memories

Memory	Maximum Number of Checked Blocks	Number of Sectors Searched
NAND	First 4	Number of sectors in a block[(1)]
OneNAND/Flex-OneNAND	First 4	8
eMMC/eSD raw	First 4	1
MMC/SD raw	First 4	1
MMC/SD/eMMC/eSD + FAT12/16/32	1 File	

(1) Depends on NAND geometry

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For more information about the GPMC module, see Section 15.4, *GPMC Overview*.

The following sections describe the supported device types.

27.4.7.3 XIP Memory

The ROM code can boot directly from XIP devices, such as NOR flash memories, that have the following characteristics:

- The GPMC is the communication interface.
- Memories up to 1 Gb (128MB) can be connected.
- x16 data bus width only
- Asynchronous protocol and address/data multiplexed mode
- The GPMC clock is 50 MHz.
- The device is connected to CS0 mapped to address 0x0800 0000.
- The wait pin signal gpmc_wait0 is monitored according to the sys_boot configuration pins.

Depending on the SYSBOOT option, the GPMC can be configured to use the wait signal connected to the gpmc_wait0 pin. Wait pin polarity is set to stall accessing memory when gpmc_wait0 is low. Wait-signal monitoring is used with memories that require a long time for initialization after reset, or that must pause while reading data.

For an XIP memory booting, no user intervention is required; the following debugging steps are described. Only the CH, which is not mandatory, lets users change clock settings and GPMC parameters. Failure in CH copying causes a return to the main booting procedure, which selects the next device for booting.

Booting from an XIP device consists of the following steps:

1. Configure the GPMC for XIP device access.
2. Verify that the CH is present at address 0x0800 0000. If it is, copy the entire sector (512 bytes) to internal RAM and execute the CH.
3. Set the image location:
   - 0x0800 0000 if the CH is not found
   - 0x0800 0200 if the CH is found
4. Verify that a bootable image is at the image location.
5. Execute the image if it is found.
6. If the image is not found, return from XIP booting to the main booting loop.

27.4.7.3.1 GPMC Initialization

Table 27-37 lists the timing settings of the GPMC when set for XIP and other address-data accessible devices, such as OneNAND/Flex-OneNAND. Table 27-37 is included for debug information.

Table 27-37. XIP Timing Parameters

Parameter	Value [Clock Cycles] (1)	Register Initialization (where i = 0–7)	Reset Value
Write cycle period	17	The GPMC_CONFIG5_i[12:8] WRCYCLETIME bit field is set to 0x11.	0x11
Read cycle period	17	The GPMC_CONFIG5_i[4:0] RDCYCLETIME bit field is set to 0x11.	0x11
CS low time	1	The GPMC_CONFIG2_i[3:0] CSONTIME bit field is set to 0x1.	0x1
CS high time	16	The GPMC_CONFIG2_i[12:8] CSRDOFFTIME bit field is set to 0x10.	0x10
ADV low time	1	The GPMC_CONFIG3_i[3:0] ADVONTIME bit field is set to 0x1.	0x1
ADV high time	2	The GPMC_CONFIG3_i[12:8] ADVRDOFFTIME bit field is set to 0x2.	0x2
OE low time	3	The GPMC_CONFIG4_i[3:0] OEONTIME bit field is set to 0x3.	0x6
OE high time	16	The GPMC_CONFIG4_i[12:8] OEOFFTIME bit field is set to 0x10.	0x10
WE low time	3	The GPMC_CONFIG4_i[19:16] WEONTIME bit field is set to 0x3.	0x05

(1) The one clock cycle is 20 ns, which corresponds to 50-MHz frequency.

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Table 27-37. XIP Timing Parameters (continued)

Parameter	Value [Clock Cycles] (1)	Register Initialization (where i = 0–7)	Reset Value
WE high time	15	The GPMC_CONFIG4_i[28:24] WEOFFTIME bit field is set to 0xF.	0x10
Data latch time	15	The GPMC_CONFIG5_i[20:16] RDACCESSTIME bit field is set to 0xF.	0x0F

There is no specific identification routine executed before booting from an XIP device.

27.4.7.4 NAND

NAND flash memory is not an XIP device; it requires shadowing before the code can be executed. ROM code support for the NAND flash devices has the following characteristics:

- The GPMC is the communication interface.
- Device from 512 Mbit (64MB)
- x8 and x16 bus width
- Support for large page size (2048 bytes + 64 spare bytes) or very large page size 4096 bytes + 128/218 spare bytes)
- Chip enable (CE) don't care devices only
- Single-level cell (SLC) and multilevel cell (MLC) devices
- Device identification based on ONFI or ROM table
- ECC correction: 8 bits/sector for most devices (16 bits/sector for devices with large spare area)
- GPMC timings are adjusted for NAND access.
- The GPMC clock is 50 MHz.
- The device is connected to CS0.
- The wait pin signal gpmc_wait0 is connected to the NAND BUSY output.
- Four physical blocks are searched for an image. Block size depends on the device.

For NAND memory booting, no user intervention is needed; the information in the following subsections is included for debugging. Only the CH, which is not mandatory, lets the user change clock settings and GPMC parameters. Failure in CH copying causes a return to the main booting procedure, which selects the next device for booting.

27.4.7.4.1 Initialization and NAND Detection

The initialization routine for NAND consists of three parts: GPMC initialization, device detection with parameter determination, and bad block detection.

- GPMC initialization

  The GPMC interface is configured so that it can access NAND. Because NAND memories do not need the address bus, it is released. The data bus width is initially set to 8 bits. If necessary, it is changed to 16 bits after the device parameters are determined. Table 27-38 shows the GPMC configuration used during NAND boot. Table 27-38 is included for debug information.

Table 27-38. NAND Timing Parameters

Parameter	Value (Clock Cycles)	Register Initialization (where i = 0–7)	Reset Value
Write cycle time	20	GPMC_CONFIG5_i[12:8] WRCYCLETIME = 0x14	0x11
Read cycle time	20	GPMC_CONFIG5_i[4:0] RDCYCLETIME = 0x14	0x11
CS low time	0	GPMC_CONFIG2_i[3:0] CSONTIME = 0x0	0x1
CS low to OE low time	5	GPMC_CONFIG4_i[3:0] OEONTIME = 0x5	0x6
CS low to OE high time	16	GPMC_CONFIG4_i[12:8] OEOFFTIME = 0x10	0x10

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Table 27-38. NAND Timing Parameters (continued)

Parameter	Value (Clock Cycles)	Register Initialization (where i = 0–7)	Reset Value
CS low to WE low time	1	GPMC_CONFIG4_i[19:16] WEONTIME = 0x1	0x5
CS low to WE high time	15	GPMC_CONFIG4_i[28:24] WEOFFTIME = 0xF	0x10
CS low to data latch time	14	GPMC_CONFIG5_i[20:16] RDACCESSTIME = 0xE	0xF

- Device detection and parameters

  The ROM code first performs an initial wait for device auto initialization (with 250-ms time-out) with polling of the ready information. Then, it must identify the NAND type connected to the GPMC interface. The GPMC is initialized using 8 bits, asynchronous mode. The NAND device is reset (command FFh) and its status is polled until ready for operation (with 100-ms time-out). The ONFI Read ID (command 90h/address 20h) is sent to the NAND device. If it replies with the ONFI signature (4 bytes) then a Read parameters page (command ECh) is sent. The information provided in Table 27-39 is then extracted: page size, spare area size, number of pages per block, and the addressing mode. The remaining data bytes from the parameter page stream are ignored.

Table 27-39. ONFI Parameters Page Description

Offset	Description	Size (Bytes)
6	Features supported	2
80	Number of data bytes per page	4
84	Number of spare bytes per page	2
92	Number of pages per block	4
101	Number of address cycles	1

If the ONFI Read ID command fails (it will be the case with any device not supporting ONFI), then the device is reset again with polling for device to be ready (with 100-ms time-out). Then, the standard Read ID (command 90h/address 00h) is sent. If the Device ID (second byte of the ID byte stream) is recognized as being a supported device, then the device parameters are extracted from an internal ROM code table. Table 27-40 lists the supported devices.

Table 27-40. Supported NAND Devices

Capacity	Device ID	Bus Width	Page Size in Bytes
512 Mb	F0h	8	2048
512 Mb	C0h	16	2048
512 Mb	A0h	8	2048
512 Mb	B0h	16	2048
512 Mb	F2h	8	2048
512 Mb	C2h	16	2048
512 Mb	A2h	8	2048
512 Mb	B2h	16	2048
1 Gb	F1h	8	2048
1 Gb	C1h	16	2048
1 Gb	A1h	8	2048
1 Gb	B1h	16	2048
2 Gb	DAh	8	2048 (4096)
2 Gb	CAh	16	2048 (4096)
2 Gb	AAh	8	2048 (4096)
2 Gb	BAh	16	2048 (4096)
2 Gb	83h	8	2048 (4096)
2 Gb	93h	16	2048 (4096)

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Table 27-40. Supported NAND Devices (continued)

Capacity	Device ID	Bus Width	Page Size in Bytes
4 Gb	DCh	8	2048 (4096)
4 Gb	CCh	16	2048 (4096)
4 Gb	ACh	8	2048 (4096)
4 Gb	BCh	16	2048 (4096)
4 Gb	84h	8	2048 (4096)
4 Gb	94h	16	2048 (4096)
8 Gb	D3h	8	2048 (4096)
8 Gb	C3h	16	2048 (4096)
8 Gb	A3h	8	2048 (4096)
8 Gb	B3h	16	2048 (4096)
8 Gb	85h	8	2048 (4096)
8 Gb	95h	16	2048 (4096)
16 Gb	D5h	8	2048 (4096)
16 Gb	C5h	16	2048 (4096)
16 Gb	A5h	8	2048 (4096)
16 Gb	B5h	16	2048 (4096)
16 Gb	86h	8	2048 (4096)
16 Gb	96h	16	2048 (4096)
32 Gb	D7h	8	2048 (4096)
32 Gb	C7h	16	2048 (4096)
32 Gb	A7h	8	2048 (4096)
32 Gb	B7h	16	2048 (4096)
32 Gb	87h	8	2048 (4096)
32 Gb	97h	16	2048 (4096)
64 Gb	DEh	8	2048 (4096)
64 Gb	CEh	16	2048 (4096)
64 Gb	AEh	8	2048 (4096)
64 Gb	BEh	16	2048 (4096)

After retrieving parameters from the table, the page size and block size are updated based on the fourth byte of the NAND ID data. Because of inconsistency among manufacturers, only devices recognized to be at least 2Gb have these parameters updated. Therefore, the ROM code supports 4-KB page devices, but only if their size, according to the table, is at least 2Gb. Devices that are smaller than 2Gb have the block size parameter set to 128KB (when the page size is 2KB). Table 27-41 shows the fourth ID data byte encoding used in the ROM code.

Table 27-41. Fourth NAND ID Data Byte

Item	Description	I/O Number							
		7	6	5	4	3	2	1	0
Page size	512 bytes							0	0
	2048 bytes							0	1
	4096 bytes							1	0
	8192 bytes							1	1
Cell type (1)	2 levels					0	0		
	4 levels					0	1		
	8 levels					1	0		
	16 levels					1	1		

(1) Read by ROM code only when the manufacturer code (first ID byte) is 98h

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Table 27-41. Fourth NAND ID Data Byte (continued)

Item	Description	I/O Number							
		7	6	5	4	3	2	1	0
Block size	64KB			0	0				
	128KB			0	1				
	256KB			1	0				
	512KB			1	1				

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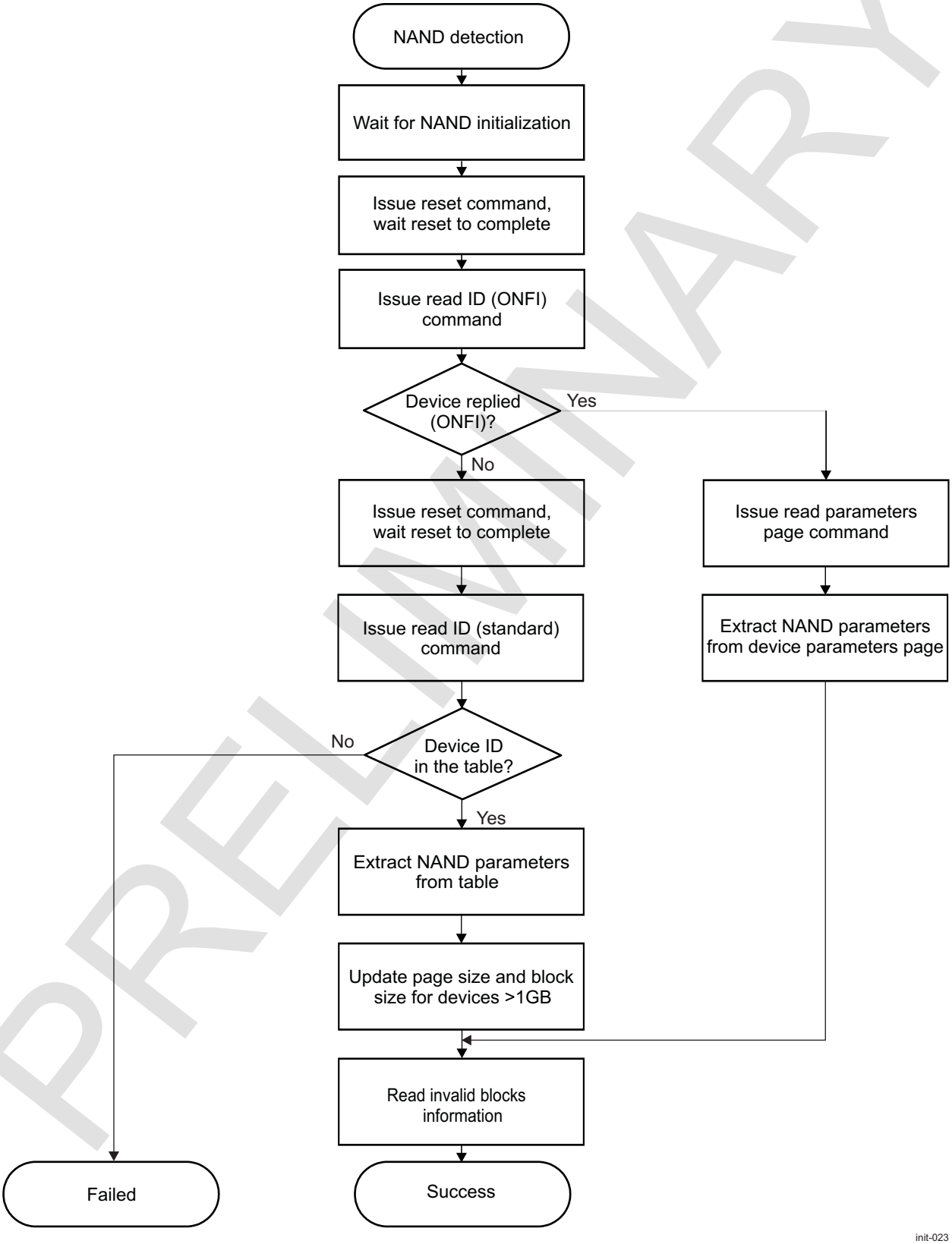
Figure 27-22 shows the detection procedure. Once the NAND device is successfully detected, the ROM code changes the GPMC to 16-bit bus width, if necessary.

Figure 27-22. NAND Device Detection



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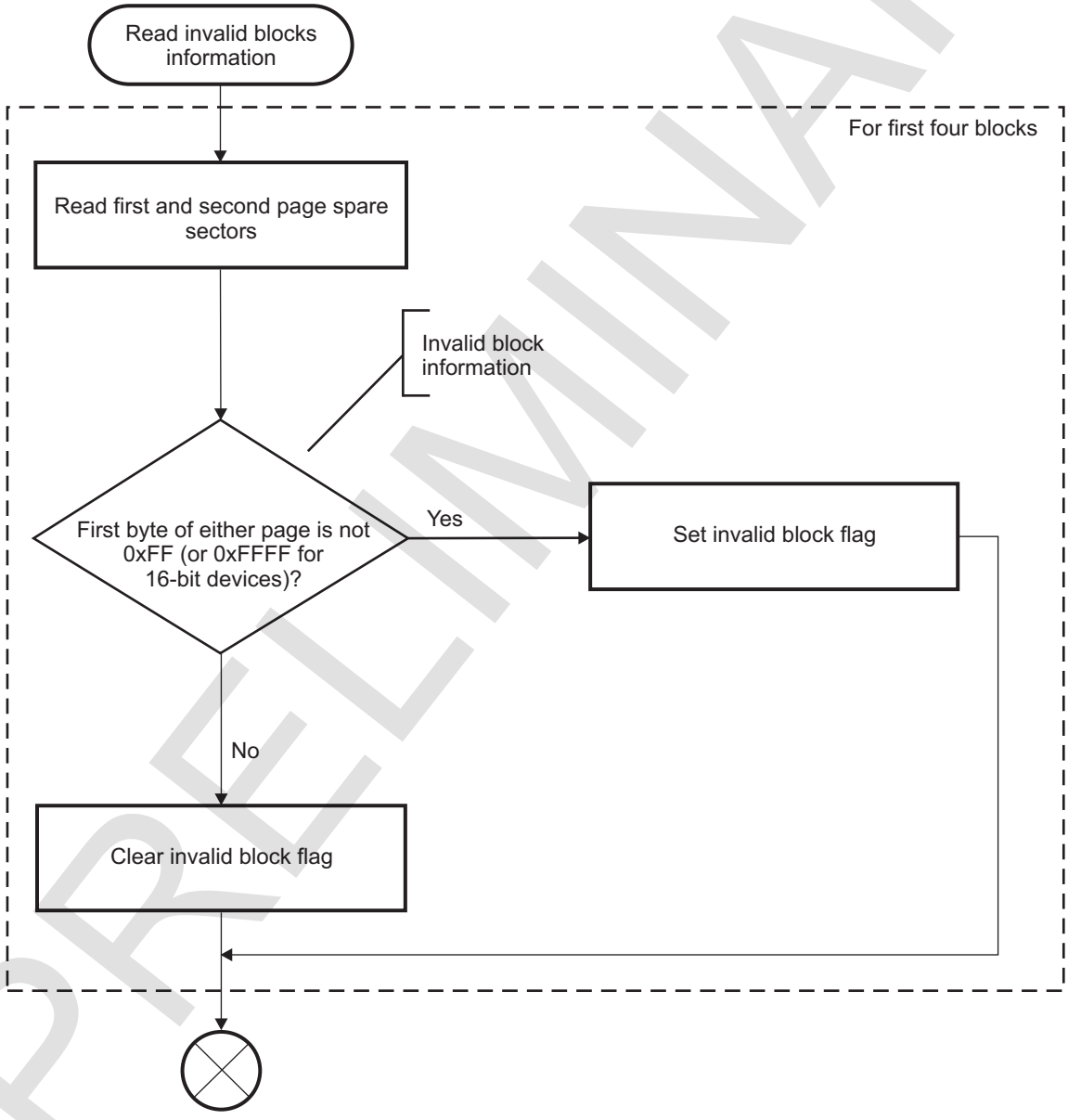
- Bad block verification

  Invalid blocks contain invalid bits whose reliability cannot be ensured by the manufacturer. These bits are identified in the factory or during the programming and reported in the initial invalid block information in the spare area on the first and second page of each block. Because the ROM code looks for an image in the first four blocks, it detects the validity status of these blocks. Blocks detected as invalid are not accessed later. Block validity status is coded in the spare areas of the first two pages of a block (first byte equal to FFh in the first and second pages for an 8-bit device/first word equal to FFFFh in the first and second pages for a 16-bit device).

Figure 27-23 shows the invalid block detection routine. The routine consists in reading spare areas and checking the validity data pattern.

Figure 27-23. Bad NAND Invalid Block Detection



27.4.7.4.2 Read Sector Procedure

During the booting procedure, the ROM code reads 512-byte sectors from the NAND device. The reading fails in two cases:

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- The accessed sector is in a block marked as invalid.
- The accessed sector contains an error that cannot be corrected with ECC.

The ROM code uses normal read (command 00h 30h) for reading NAND page data.

Page data can contain errors caused by memory alteration. The ROM code uses an ECC correction algorithm to detect and possibly correct those errors. The default ECC correction applied is BCH 8b/sector using the GPMC and ELM hardware.

For device ID codes D3h, C3h, D5h, C5h, D7h, C7h, DEh, and CEh when the manufacturer code (first ID byte) is 98h, the cell type information is checked in the fourth byte of ID data. If it is equal to 10b, the ECC correction applied is BCH 16b/sector.

The BCH data is automatically calculated by the GPMC on reading each 512-byte sector. The computed ECC is compared against the ECC stored in the spare area for the corresponding page. Depending on the page size, the amount of ECC data bytes stored in the corresponding spare area is different. Figure 27-24 and Figure 27-25 show the mapping of ECC data inside the spare area for 2KB-page and 4KB- page devices, respectively. If both ECC data are equal, the read sector function returns the read 512-byte sector without error. Otherwise, the ROM code tries to correct error(s) in the corresponding sector (this procedure is assisted by the ELM hardware) and returns the data if successful. If errors are uncorrectable, the function returns with FAIL.

Figure 27-24. ECC Data Mapping for 2-KB Page and 8b BCH Encoding

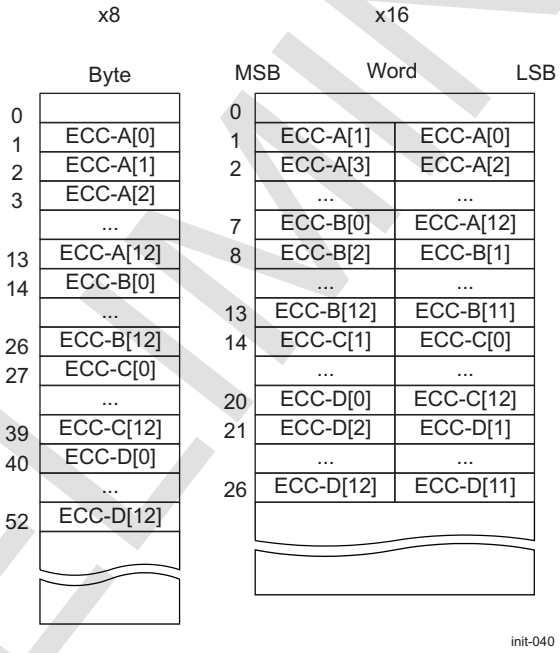

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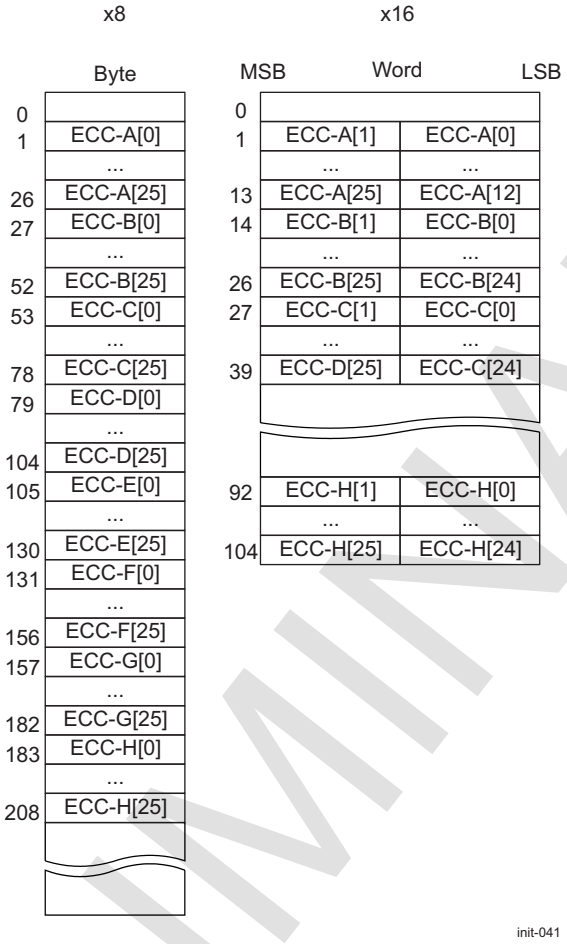
Figure 27-25. ECC Data Mapping for 4-KB Page and 16b BCH Encoding



27.4.7.5 OneNAND/Flex-OneNAND

The ROM code support for OneNAND/Flex-OneNAND devices has the following characteristics:

- Devices from 512 Mbits
- The GPMC is the communication interface.
- x16 data bus width only
- Asynchronous protocol and address/data multiplexed mode
- GPMC reset default timings are used.
- The GPMC clock is 50 MHz.
- The device is connected to GPMC CS0 mapped to address 0x0800 0000.
- The wait pin signal gpmc_wait0 is not monitored.
- Four physical blocks are searched for an image. The block size is 128KB (typically).
- Data correction is fully handled by the OneNAND/FlexOneNAND device

The OneNAND/Flex-OneNAND device is a NAND matrix coupled with RAM buffers and a NOR-type interface. ECC correction handling is done automatically by the internal state-machine. The page to be accessed is first loaded in the RAM buffer using memory-mapped registers. Then, the page is read directly from the buffer using a NOR-type interface.

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For OneNAND/Flex-OneNAND memory booting, no user intervention is required. The information in the following sections is included for debugging. Only the CH, which is not mandatory, lets users change clock settings and GPMC parameters. Failure in CH copying causes a return to the main booting procedure, which selects the next device for booting.

27.4.7.5.1 Initialization and OneNAND/Flex-OneNAND Detection

The initialization routine for OneNAND/Flex-OneNAND consists of two parts: GPMC initialization and device detection with parameter determination.

- GPMC initialization

  The ROM code first initializes the GPMC interface in XIP mode (that is, asynchronous 16-bit multiplexed mode). Wait signal monitoring is disabled.

- Device detection and parameters

  The ROM code identifies a OneNAND/Flex-OneNAND device by reading the device identification data. There are two ways to read identification data: using serial commands and reading from fixed memory-mapped registers. The ROM code reads identification data using both methods and compares the results. When the comparison passes, the ROM code assumes that the OneNAND/Flex-OneNAND device is connected. If the device is successfully recognized, the ROM code reads the device configuration (number and size of data buffers) and configures it for asynchronous mode (default).

27.4.7.5.2 OneNAND/Flex-OneNAND Read Sector Procedure

When booting requests a sector from the OneNAND/Flex-OneNAND device, the ROM code performs the load operation, which transfers the content of the requested sector to the data buffer RAM. The ROM code waits until the operation completes, polling the OneNAND/Flex-OneNAND interrupt register. The status register is then checked and the ROM code returns FAIL if the operation completes with an error. Otherwise, the data buffer RAM is copied to the destination buffer. Figure 27-26 shows this procedure.

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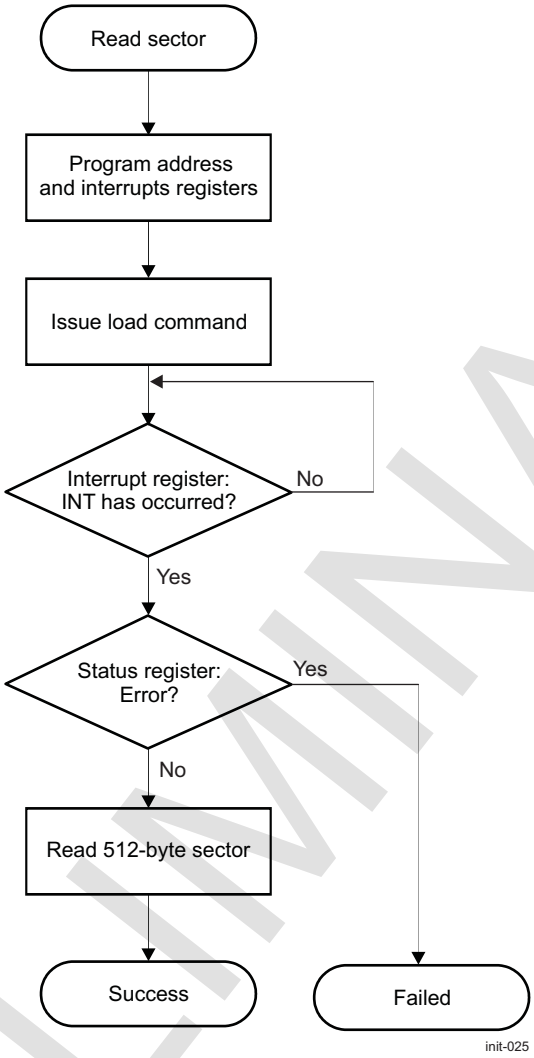
Figure 27-26. OneNAND/Flex-OneNAND Read Sector



27.4.7.5.3 OneNAND/Flex-OneNAND Support Limitations

As described in Section 27.4.7.5.1, *Initialization and OneNAND/Flex-OneNAND Detection*, the ROM code checks only the coherency of the device ID obtained by two different methods. There is no table of supported Flex-OneNANDs in ROM code. This removes any dependency of the ROM code on device IDs from different manufacturers. However, the driver works with the following assumption:

- Page size is assumed to be 2048 bytes, divided into four 512-byte sectors. In case of OneNAND/Flex-OneNAND, with 4096-byte pages, divided into eight sectors, users must program only the first sectors (sectors 0-3) of each page. Sectors 4-7 of each page are not considered by the driver.

27.4.7.6 eMMC/eSD Embedded Memories and MMC/SD Cards

The OMAP4460 device allows booting from eMMC/eSD embedded memories or MMC/SD cards connected to SD/MMC1 or SD/MMC2. The booting interface is selected by configuration of the sys_boot pins.

The HS MMC/SD/SDIO host controllers (MMCHS) handle the physical layer, while the ROM code handles the simplified logical protocol layer (read-only protocol). A limited range of commands is implemented in the ROM code.

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The MMC interface 1 supports 1.8-V/3-V digital I/Os. The selection on I/O voltage level is done using the PBIAS circuitry. The PBIAS reference level is sensed by the ROM code and PBIAS cell voltage setup appropriately before any communication with the device. The MMC interface 2 supports only 1.8-V digital I/Os.

The OMAP4460 device supports two booting modes:

- Raw: The booting image data is read directly from sectors in the user area.
- File system (FAT12/16/32 supported with or without master boot record): The image data is read from a booting file.

When using the SDMMC1 interface, raw and file system modes are supported. When using the SDMMC2 interface, only raw mode is supported. The purpose of this approach is to avoid the boot time penalty of searching for a file system hierarchy when it is not always necessary.

Figure 27-27 shows the complete procedure.

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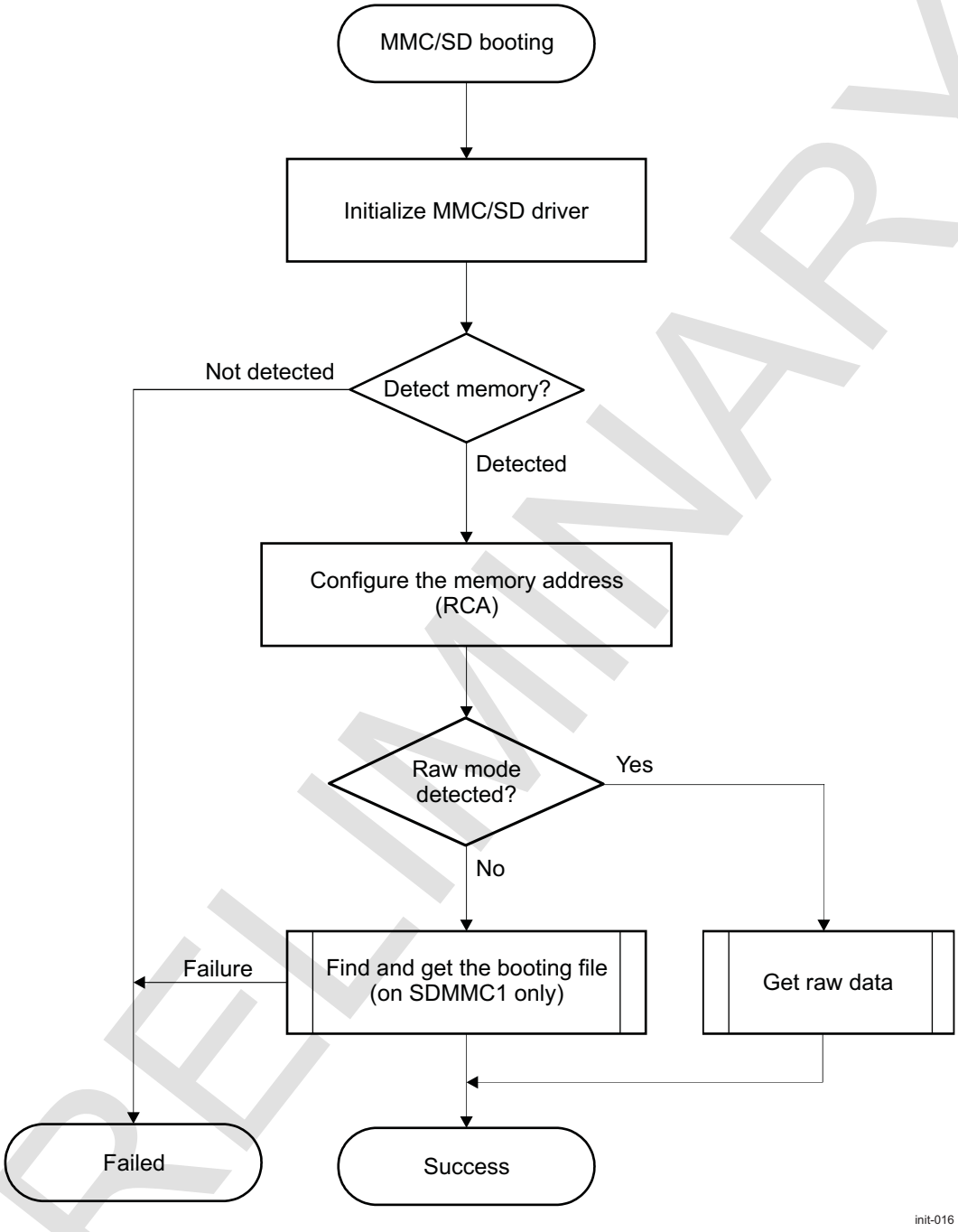
Figure 27-27. eMMC/eSD and MMC/SD Booting



27.4.7.6.1 eMMC/eSD Overview

The ROM code supports eMMC/eSD cards, with the following conditions:

- eMMC devices compliant with *Embedded MultiMediaCard (eMMC) eMMC/Card Product Standard, High Capacity, including Reliable Write Boot, and Sleep Modes, Dual Data Rate, Multiple Partitions Supports and Security Enhancement v4.41* from the MMCA Technical Committee. The exception is the hardware reset feature. If the user software requires MMC hardware reset, it can be accomplished with a GPIO.
- eSD devices compliant with *SD Specification Part 1 eSD (Embedded SD) Specification Addendum v2.1* from the SD Card Association

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- The eMMC/eSD memory device is powered externally by a power-management IC or other power supply.
- Initial 1-bit MMC mode, optional 4-bit or 8-bit modes
- Clock frequency:
  - Identification mode: 400 kHz
  - Data transfer mode: Up to 10 MHz, optionally up to 19.2 MHz
- Only one memory connected to the bus

27.4.7.6.1.1 System Conditions and Limitations

The ROM code does not support the specific details of the partition management and boot operations modes as defined in the eMMC Standard sections *Partition Management* and *Boot Operation Mode*. The booting image is assumed to be in the User Data Area (no use of boot and/or RPMB partitions). Customers must set up the eMMC device appropriately so that the booting image is in a reliable area within the User Data Area (possibly with the Enhanced User Data Area property).

The ROM code does not provide a bus direction control signaling in case of using MMC interface 2 with level shifters.

The ROM code expects that the eMMC device is powered externally and supplies are set and stable upon entering the booting procedure. The ROM code does not perform any software action to the companion device with respect to powering the eMMC/eSD device.

27.4.7.6.1.2 eMMC/eSD Memory Connection

An eMMC/eSD device typically requires two supplies: one for the core memory array (selectable 1.8/2.9 V at TWL6030 BOOT2 pin level) (see TWL6030 documentation), and one for the device interface I/Os and controller (typical VCCQ = 1.8 V). Both memory device supply pins can possibly be merged into one, thus requiring only one power supply.

The SD/MMC2 interface shares the same balls as the GPMC interface. Therefore, the ROM code performs the necessary pin mux configuration to route the MMC signal through the GPMC balls.

Figure 27-28 shows an example of the system connection between the power-management IC, memory device, and OMAP device.

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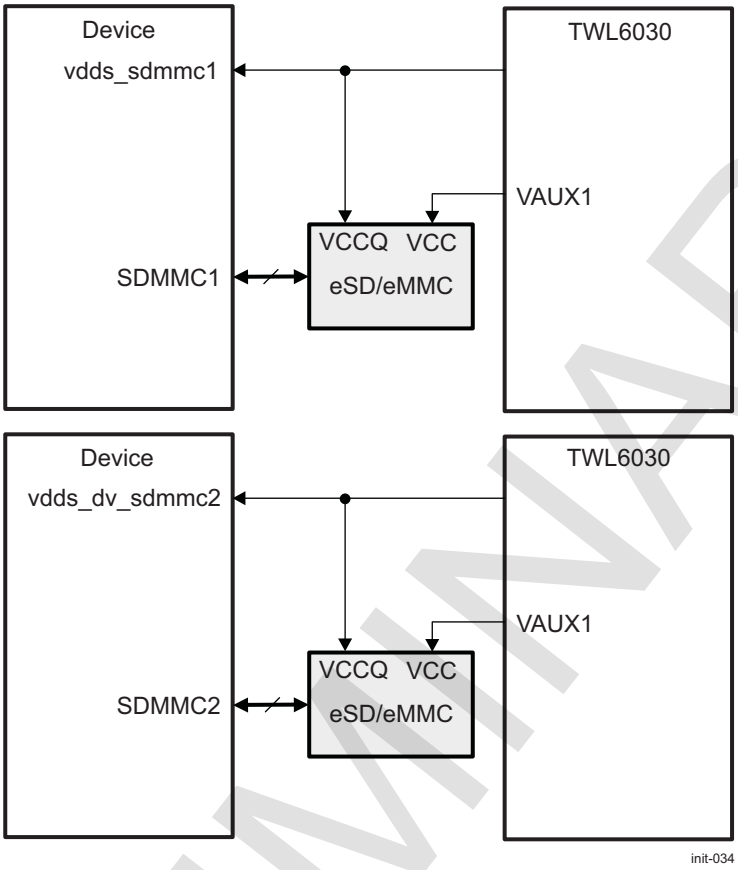
Figure 27-28. eMMC/eSD Connection



The ROM code supports the muxing of MMC interface 2 through two paths:

- GPMC pins in configuration mode 1 (Mux1)
- SDMMC5/FREF_CLKx pins in Mux5

The ROM code performs the necessary I/O pin muxing configuration to route the MMC2 signals through the appropriate pins depending on the selected SYSBOOT configuration.

27.4.7.6.2 MMC/SD Overview

The ROM code supports booting from MMC/SD cards under the following conditions:

- MMC/SD cards compliant with *The MultiMediaCard System Specification* from the MMCA Technical Committee and the *SD Memory Card Specifications, File System Specification* from the SD Association. These include low- and high-capacity cards.
- MMC/SD cards connected to SDMMC interface 1
- 3-V VCC power supply, support for 3-V or 1.8-V I/O voltages
- Initial 1-bit MMC mode, optional 4-bit or 8-bit modes
- Clock frequency:
  - Identification mode: 400 kHz
  - Data transfer mode: Up to 10 MHz (optionally up to 19.2 MHz)
- Only one card connected to the bus

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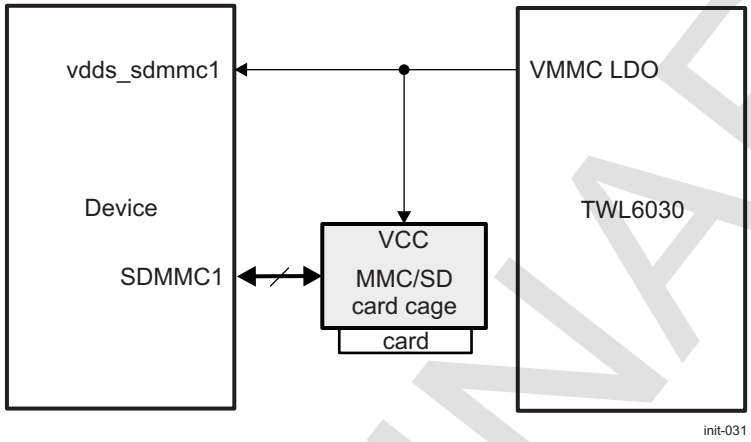
27.4.7.6.2.1 MMC/SD Card Connection

An SD/MMC card can be connected to the MMC1 interface, typically through a card cage. The ROM code sends the appropriate I^2C sequence to the power-management IC to set the VMMC LDO to 3 V and switch it on.

Figure 27-29 shows the typical connection between the power IC, the card, and the OMAP device .

Figure 27-29. MMC/SD Card Connection



NOTE: The ROM code does not handle the card detection feature on the card cage.

27.4.7.6.3 Initialization and Detection

The ROM code initializes the memory device or card connected on the interface using the standard high-voltage range (3.0 V). If neither a card nor memory device is detected, the ROM code moves to the next booting device. The standard identification process and relative card address (RCA) assignment are used. However, the ROM code assumes that only one memory or card is connected on the bus. This is done using the CMD line common to the SD and MMC memory devices. The MMC and SD standards describe this phase as the initialization phase. They differ in the first commands involved, CMD1 and ACMD41. The ROM code uses this command difference to discriminate between MMC and SD cards; that is, CMD1 is supported only by the MMC standard and ACMD41 is only supported by the SD standard. The ROM code first sends a CMD1 to the device and gets an answer only if an MMC device is connected. If no response is received, ACMD41 (a combination of CMD55 and ACMD41) is sent, and an response is expected from an SD device. If no response is received, no devices are connected and the ROM code exits MMC/SD booting with FAIL.

Figure 27-30 shows the MMC/SD detection procedure.

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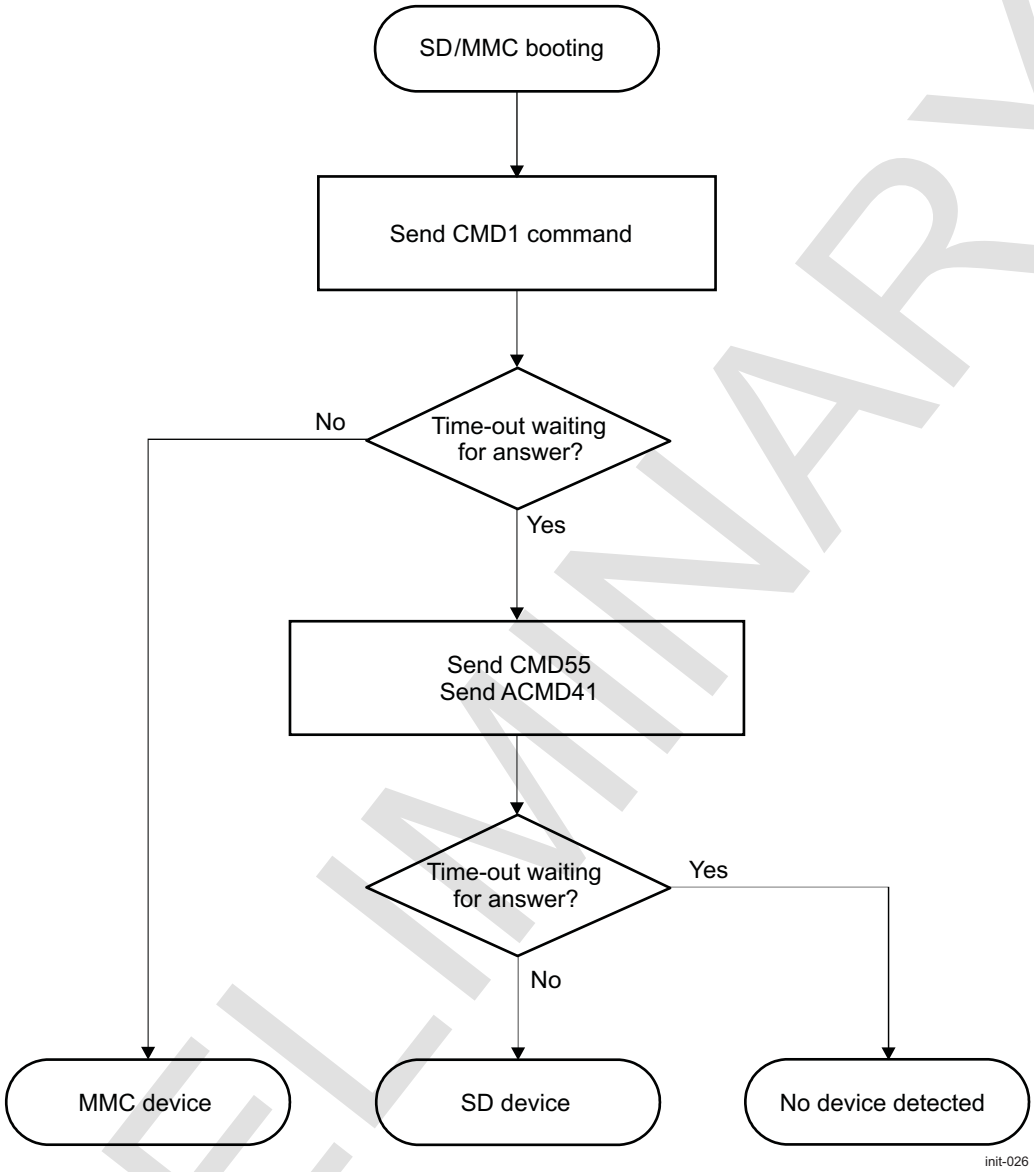
Figure 27-30. MMC/SD Detection Procedure



27.4.7.6.4 Read Sector Procedure

- Raw mode

  In raw mode, an image can be at one of the four consecutive locations in the main area: offset 0x0 (0KB)/0x20000 (128KB)/0x40000 (256KB)/0x60000 (384KB). For this reason, the size of a booting image must not exceed 128KB. However, a device with an image greater than 128KB can be flash starting at one of the aforementioned locations. Therefore, the ROM code does not check the image size. The only drawback is that the image crosses the subsequent image boundary. Raw mode is detected by reading sectors 0, 256, 512, and 768. The content of these sectors is verified for the presence of a TOC structure. For a GP device, a CH (if used) must be in the first sector followed by a GP header. The CH can be void (containing only a CHSETTINGS item for which the Valid field is 0), as described in Section 27.4.8.2, *Configuration Header*. Image data is read directly from continuous sectors of a card. If raw mode is not detected, file system mode is assumed.

- File system handling

  File system support is available only for the SDMMC1 interface. The sector read procedure uses the standard MMC/SD read data procedure. The sector address is generated based on the booting

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memory file map collected during initialization. Thus, the ROM code can freely address sectors in the booting file space.

27.4.7.6.5 File System Handling

The MMC/SD cards can hold a file system that the ROM code reads. The image used by the booting procedure is taken from a booting file named MLO. This file must be in the root directory on an ***active*** primary partition of type FAT12/16 or FAT32.

An MMC/SD card can be configured as floppy-like or hard-drive-like:

- When acting like a floppy, the content of the card is a single FAT12/16/32 file system without an MBR holding a partition table.
- When acting like a hard drive, an MBR is present in the first sector of the card. This MBR holds a table of partitions, one of which must be FAT12/16/32, primary, and active.

According to the *MultiMediaCard FAT16 File System Specification* from the MMCA Technical Committee, the card must always hold an MBR, except for MMC cards using a floppy-like file system. However, depending on the operating system used, the MMC/SD card is formatted with or without partition(s) (using an MBR). The ROM code supports both types: floppy-like or hard-drive-like. The ROM code retrieves a map of the booting file from the FAT table. The booting file map is a collection of all FAT table entries related to the booting file (a FAT entry points to a cluster holding part of the file). The booting procedure uses this map to access any 512-byte sector in the booting file without involving the ROM code FAT module. Figure 27-31 shows the complete process.

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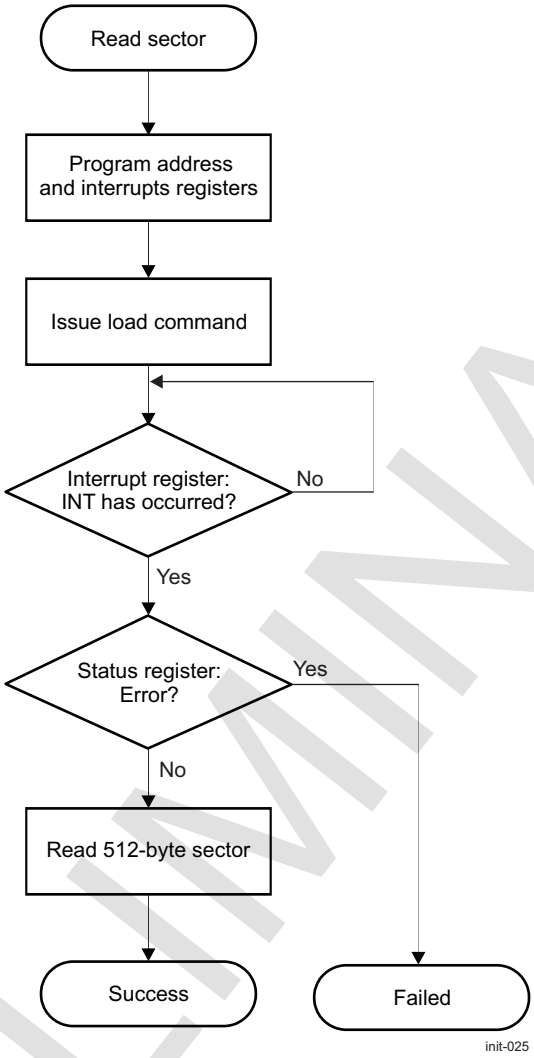
Figure 27-31. SD/MMC Get Booting File



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27.4.7.6.5.1 MBR and FAT File System

This paragraph describes functions used by the ROM code to recognize whether an MBR with a FAT is used. It is not intended to fully describe the MBR and the FAT file system detection and reading procedure. The ROM code can detect FAT12/16/32 allocation table types. It cannot boot on devices with NTFS or Linux® FS partitions. Some memory devices that support file systems can be formatted with or without MBR; therefore, the first task of the ROM code is to detect whether the device is holding an MBR in the first sector.

The MBR is the first sector of a memory device. It consists of executable code, four partition entries, and one signature. The aim of such a structure is to divide the hard disk in partitions used primarily to boot different systems (for instance, Microsoft Windows™). This structure is described in Table 27-42, and the partition table entry is described in Table 27-43.

Table 27-42. Master Boot Record Structure

Offset	Length (Bytes)	Entry Description
0000h	446	Optional code
01BEh	16	Partition table entry
01CEh	16	Partition table entry
01DEh	16	Partition table entry
01EEh	16	Partition table entry
01FEh	2	Signature (0xAA55)

Table 27-43. Partition Table Entry

Offset	Length [Bytes]	Entry Description	Value
0000h	1	Partition state	00h: Inactive 80h: Active
0001h	1	Partition start head	Hs
0002h	2	Partition start cylinder and sector	Cs[7:0]–Cs[9:8]–Ss[5:0]
0004h	1	Partition type	01h: FAT12 04h, 06h, 0Eh: FAT16 0Bh, 0Ch, 0Fh: FAT32
0005h	16	Partition end head	He
0006h	2	Partition end cylinder and sector	Ce[7:0]–Ce[9:8]–Se[5:0]
0008h	4	First sector position relative to the beginning of media	LBAs = Cs.H.S + Hs.S + Ss–1
000Ch	4	Number of sectors in partition	LBAe = Ce.H.S + He.S + Se–1 Nb s= LBAe–LBAs + 1

SD/MMC booting consists of the following steps:

1. MBR detection

   The ROM code first checks whether the MBR signature is present, and then it searches an active FAT12/16/32 partition in all four MBR partition entries, based on the Type field. If the MBR entries are not valid, or if no usable partition is found, the ROM code returns to the booting procedure with FAIL. The extended partitions are not checked; the booting file must reside in a primary partition. Each partition entry is checked:

   (a) If its type is set to 00h, all fields in the entry must be 00h.

   (b) The partition is checked to be within physical boundaries (that is, the partition is inside and it fits the total physical sectors).

   See Figure 27-32 for more information about MBR detection.

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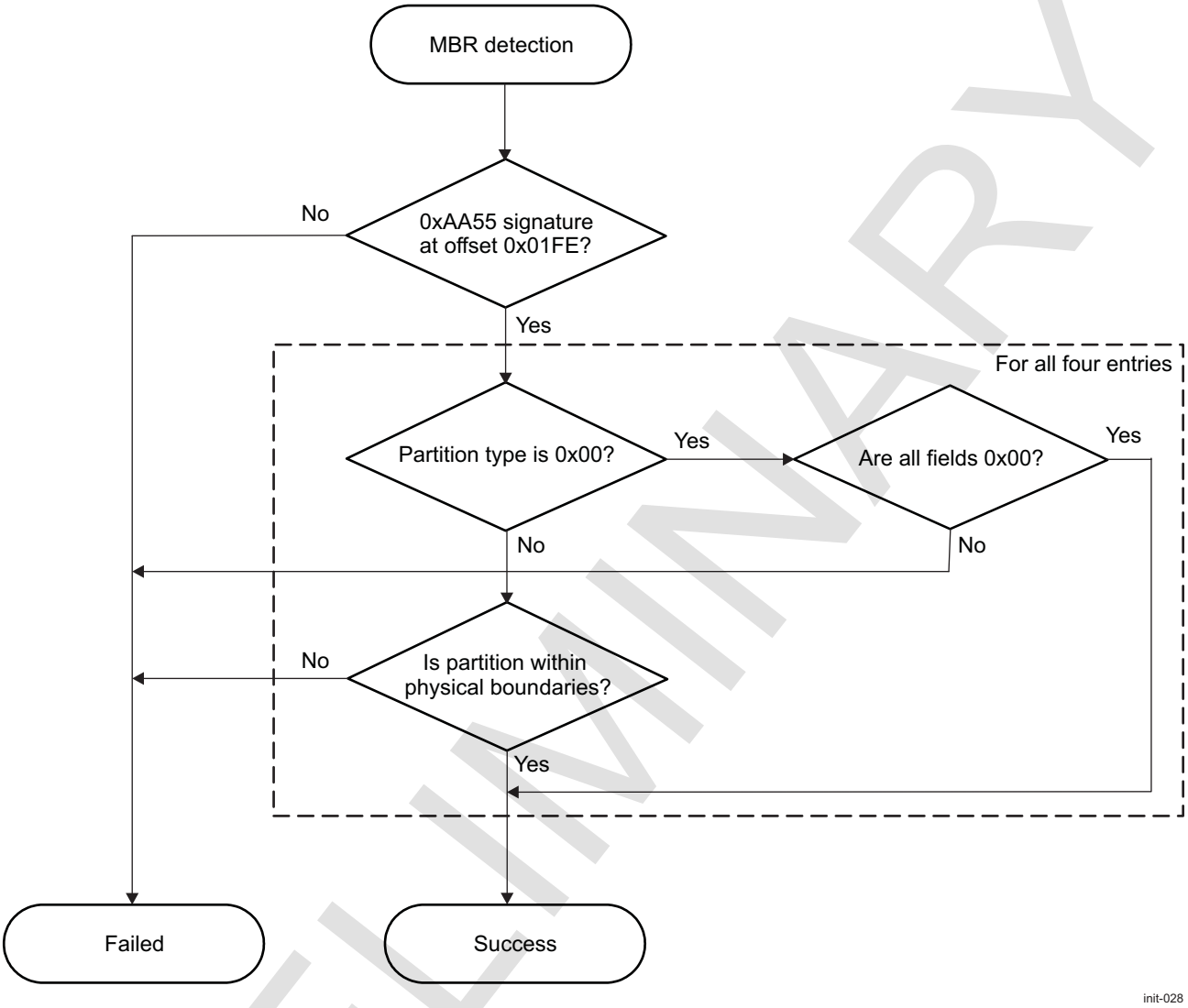
Figure 27-32. MBR Detection Procedure



2. Get the MBR partition.

   Once identified, the ROM code gets the partition using the procedure described in Figure 27-32. The partition type is checked to be FAT12/16 or FAT32. Its state must be 00h (inactive) or 80h (active.) The ROM code returns with FAIL if no active primary FAT12/16/32 is found, or the test fails if there is more than one active partition. If an active partition is found, its first sector is read and used later. If no MBR is present (in case of a floppy-like system), the first sector of the device is read and used later. The read sector is checked to be a valid FAT12/16 or FAT32 partition. If this fails, the ROM code returns with FAIL if another partition type is used (for instance, Linux FS) or if the partition is not valid.

   The FAT file system consists of several parts:

   - Boot sector, which holds the BIOS parameter block (BPB). Not all are used by the ROM code.
   - FAT, which describes the use of each cluster of the partition
   - Data area, which holds the files, directories, and root directory (for FAT12/16, the root directory has a specific fixed location)

   To check whether a sector holds a valid FAT12/16/32 partition, many fields of the boot sector (used by all FAT types) that must have specific values are checked. Figure 27-33 shows more about getting the partition.

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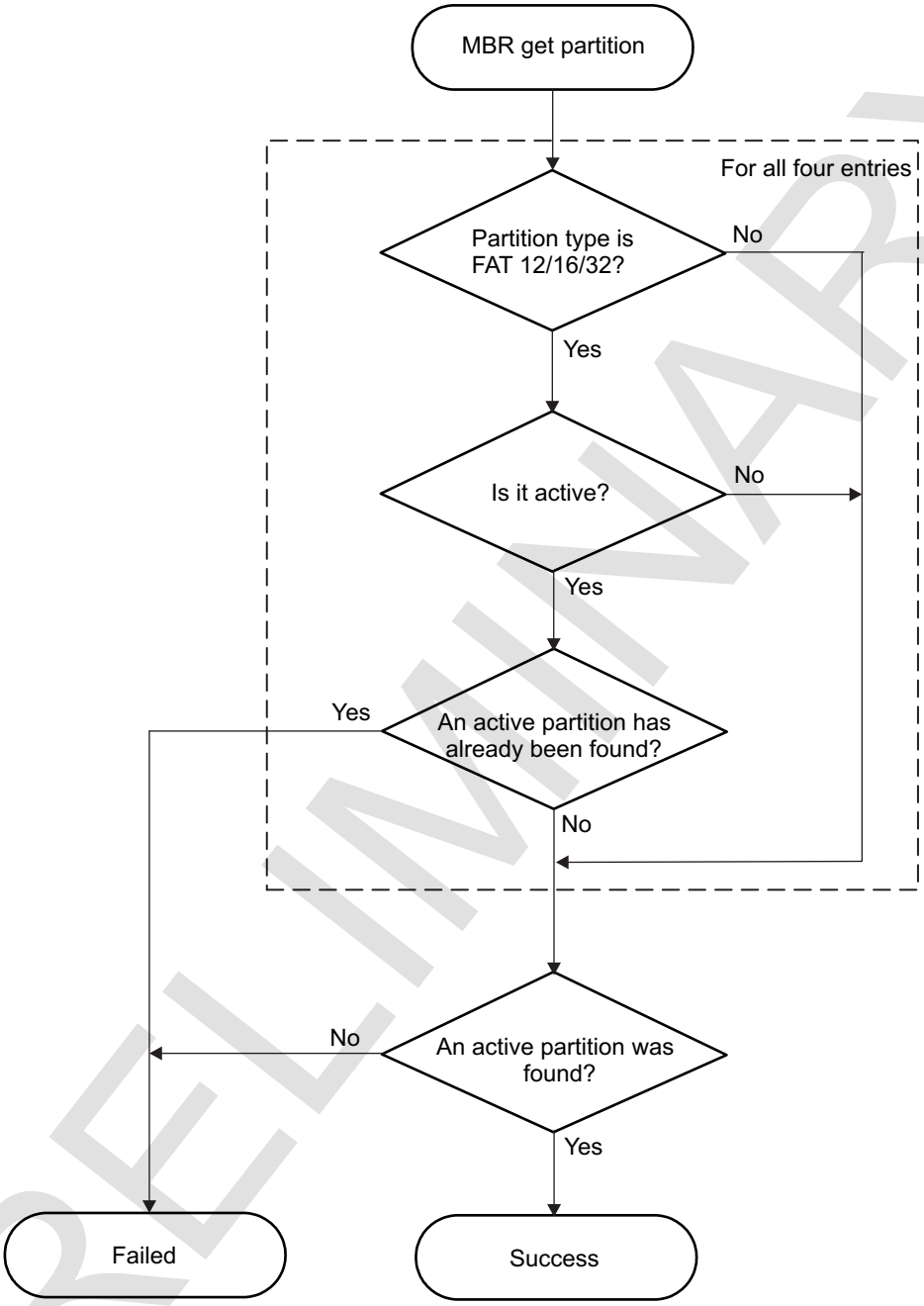
Figure 27-33. MBR, Get Partition



3. Find the booting file.

   When a partition is found, the root directory entries are searched for a booting file named MLO in the root directory of the FAT12/16/32 file system. The file is not searched in any other location. For a FAT12/16 file system, the root directory has a fixed location, which is cluster 0. For a FAT32 file system, its cluster location is given by BPB_RootClus. The formula to find the sector number (relative to device sector 0, not partition sector 0) of a cluster is given by the following equation:

$$Cluster_{sector} = BPB_HiddSec + BPB_RsvdSecCnt + BPB_NumFATs \cdot BPB_FATSz + Cluster \cdot BPB_SecPerCLus$$

init-E001

NOTE: BPB_FatSz is BPB_FatSz16 for FAT12/16, or BPB_FatSz32 for FAT32.

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NOTE: The BPB_HiddSec field can contain 0, even though the FAT file system is somewhere other than on sector 0 (floppy-like). The ROM code uses the partition offset taken from the MBR instead of this field, which can be wrong. If no MBR is found (floppy-like), the value 0 is used.

Each entry in the root directory is 32 bytes and holds information about the file (the filename, date of creation, rights, cluster location, etc.). (See Table 27-44.)

Table 27-44. FAT Directory Entry

Offset	Length [Bytes]	Name	Description
0000h	11	DIR_Name	Short Name (8 + 3)
000Bh	1	DIR_Attr	File Attributes: 01h – ATTR_READ_ONLY 02h – ATTR_HIDDEN 04h – ATTR_SYSTEM 08h – ATTR_VOLUME_ID 10h – ATTR_DIRECTORY 20h – ATTR_ARCHIVE 0Fh – ATTR_LONG_NAME
000Ch	1	DIR_NTRes	Reserved. Set to 00h.
000Dh	1	DIR_CrtTimeTenth	Millisecond stamp at file creation
000Eh	2	DIR_CrtTime	Time file was created.
0010h	2	DIR_CrtDate	Date file was created.
0012h	2	DIR_LstAccDate	Last access date
0014h	2	DIR_FstClusHi	High word of the first cluster number of this entry
0016h	2	DIR_WrtTime	Time of last write
0018h	2	DIR_WrtDate	Date of last write
001Ah	2	DIR_FstClusLo	Low word of the first cluster number of this entry
001Ch	4	DIR_FileSize	File size in bytes

The ROM code checks each entry in the root directory until either the booting file is found or the entry is empty (first byte is 00h), or when the end of the root directory is reached. Entries with the ATTR_LONG_NAME attribute (LFN) and first byte at E5h (erased file) are ignored. When found, the first cluster offset of the file is read from the DIR_FstClusHi/DIR_FstClusLo fields. There is a slight difference between FAT12/16 and FAT32 when handling the root directory. On FAT12/16, this directory has a fixed location (see Table 27-44) and length fixed by BPB_RootEntCnt, which is the total of 32-byte entries. Therefore, handling this directory is straightforward. On FAT32, the root directory is like a standard file. The FAT must be used to retrieve each sector of the directory. The way in which the FAT is handled is described in Step 4.

4. Buffer FAT entries in the FAT buffer

   When the booting file is found, the ROM code reads the FAT and buffers the singly-linked chain of clusters in a FAT buffer used by booting to access the file directly, sector by sector. For FAT12/16 and for FAT32, multiple copies of the FAT exist (ROM code supports only two copies), after the boot sector.

$$FATn_{sector} = BPB_HiddSec + BPB_RsvdSecCnt + BP_FatSz \cdot n$$

init-E002

   The size of the FAT buffer is given by BPB_FATSz16 or BPB_FATSz32. The ROM code checks each copy of the FAT if they are identical. If the values are different, the ROM code uses the value from the last FAT copy. With the FAT32 file system, the copy system can be disabled according to a flag in BPB_ExtFlags[7]. If this flag is set, the FAT BPB_ExtFlags[3:0] bit field is used. In this case, no verification is made by the ROM code with other copies of FAT.

   The FAT is a simple array of values, each referring to a cluster in the data area. One entry of the array is 12, 16, or 32 bits, depending on the file system in use. The value in an entry defines whether the

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cluster is being used or not, and if another cluster must be considered. This creates a singly-linked chain of clusters defining the file. The meaning of an entry is described in Table 27-45.

NOTE: For compatibility, cluster 0 and cluster 1 are not used for files, and these entries must contain:

- FF8h and FFFh (for FAT12)
- FFF8h and FFFFh (for FAT16)
- 0FFFFFF8h and 0FFFFFFFh (for FAT32)

Table 27-45. FAT Entry Description

FAT12	FAT16	FAT32	Description
000h	0000h	00000000h	Free cluster
001h	0001h	00000001h	Reserved cluster
002h–FEFh	0002h–FFEFh	00000002h–0FFFFFEFh	Used cluster; value points to next cluster
FF0h–FF6h	FFF0h–FFF6h	0FFFFFF0h–0FFFFFF6h	Reserved values
FF7h	FFF7h	0FFFFFF7h	Bad cluster
FF8h–FFFh	FFF8h–FFFFh	0FFFFFF8h–0FFFFFFFh	Last cluster in file

NOTE: FAT32 uses only bits [27:0]; the upper 4 bits are usually 0 and must be left untouched.

When accessing the root directory for FAT32, the ROM code starts from the root directory cluster entry and follows the linked chain to retrieve the clusters.

When the booting file has been found, the ROM code buffers each FAT entry corresponding to the file in a sector way. This means each cluster is translated to one or several sectors, depending on how many sectors are in a cluster (BPB_SecPerClus). This buffer is used later by the booting procedure to access the file.

27.4.8 Image Format

27.4.8.1 Overview

An image has two major parts:

- AAn optional CH
- Software to execute

The CH can contain several parameters set by users to speed up booting. It is further described in Section 27.4.8.2, *Configuration Header*.

The second part contains the software that is loaded into the memory and executed.

Figure 27-34 is an overview of the boot image formats. There are two image types:

1. GP non-XIP memory booting: This image type is used for memories that require shadowing (for example, MMC). An image can contain a CH that includes at least a CHSETTINGS item entry. Next, there must be a small header (referred to as a GP header) that contains information about the size and the destination address.
2. When the memory device is of XIP type (for example, NOR), the GP header is not required, and the image can contain code for direct execution. Optionally, the first sector can contain a CH. The same image format is used for peripheral booting (where the code is transferred to internal RAM).

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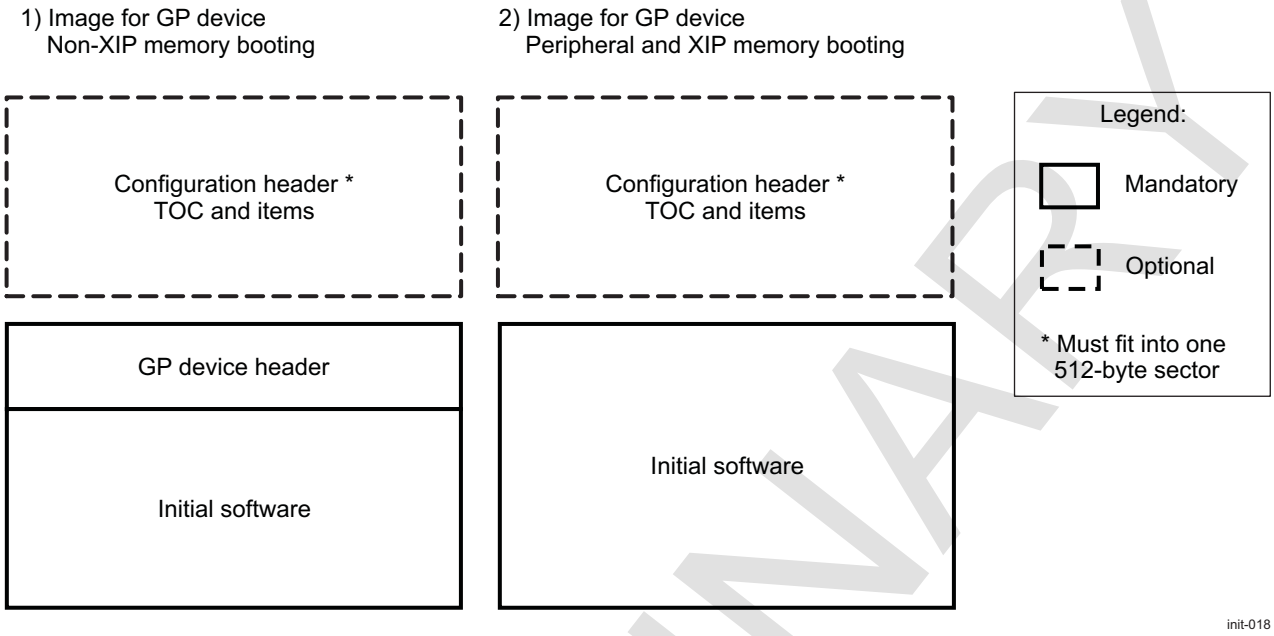
Figure 27-34. Image Formats



27.4.8.2 Configuration Header

The ROM code default settings (such as clock frequencies, EMIF, GPMC, or MMCHS interfaces) can be tuned by the user by using the CH.

The CH can contain the following parts:

- Settings: Various clock settings (mandatory)
- RAM: EMIF settings
- FLASH: Flash interface (GPMC) settings
- MMC/SD: MMCHS interface settings

The beginning of the CH is a table of contents (TOC), which points to each item. This is described in Figure 27-35. Each TOC item is a simple structure described in Table 27-46. The complete CH (CH TOC and items) should fit in a 512-byte sector.

The ROM code identifies the presence of a CH by reading the first TOC item if it contains a known string (CHSETTINGS, CHRAM, etc.). Next, the TOC is identified and searched until a 0xFFFF FFFF offset is found. The CH is read and parameters are executed sequentially.

For the sake of simplicity, each field represents the content of a register to be modified. Only fields required for the configuration are used; fields for status, for instance, are not modified and therefore are not shown in the tables.

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Figure 27-35. CH Format

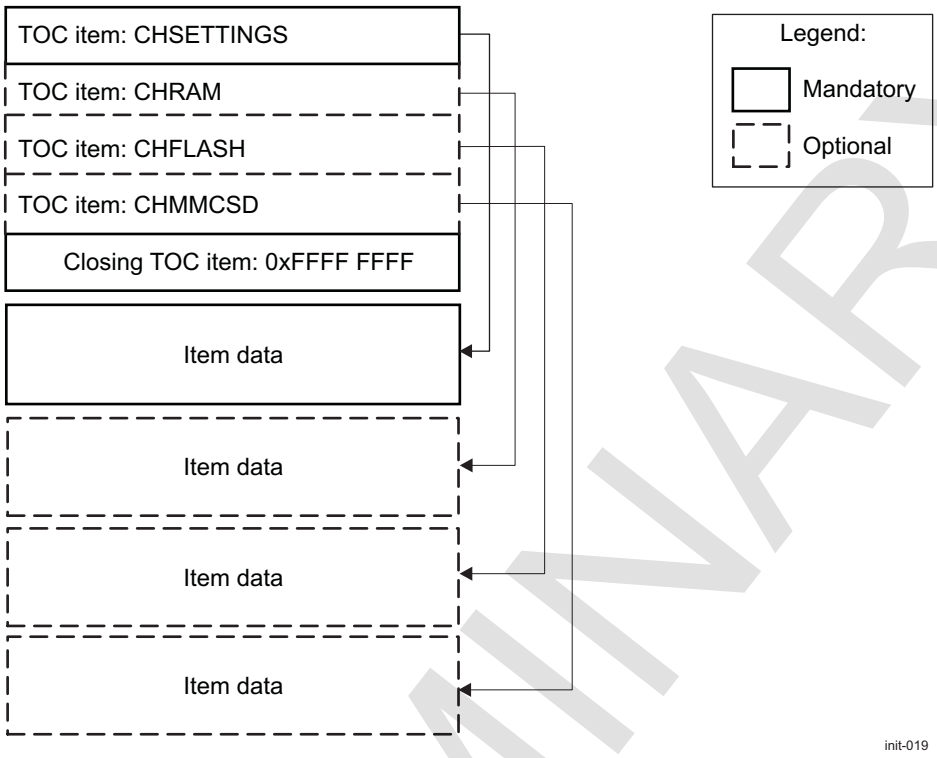

Table 27-46. CH TOC Item

Offset	Field	Size (Bytes)	Description
0x0000	Start	4	Offset from the start address of the TOC to the actual address of item contents
0x0004	Size	4	Size of item
0x0008	Reserved	4	Unused
0x000C	Reserved	4	Unused
0x0010	Reserved	4	Unused
0x0014	Filename	12	12-character name of a item, including the zero termination character(\0)

27.4.8.2.1 CHSETTINGS Item

The CHSETTINGS configuration header contains settings specific to the clock system. The ROM code configures the OMAP clocking to some default settings as described in Section 27.4.4.2, *Clocking Configuration*. The CH CHSETTINGS section contains a method to override the ROM code default clock settings.

Table 27-47 describes the fields. The clocking procedure and the clocking setting structure are described in Section 27.4.4.4, *Software Booting Configuration*.

Table 27-47. CHSETTINGS Item

Offset	Field	Description
0000h	Section key	Key used for item verification: C0C0C0C1h
0004h	Valid	Enables/disables the section: 00h: Disable

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Table 27-47. CHSETTINGS Item (continued)

Offset	Field	Description
		Others: Enable
0005h	Version	Configuration header version 01h Others: Reserved
0006h	Reserved	
0008h	Clocking settings	Described in Table 27-16 starting from the FLAGS field.

27.4.8.2.2 CHRAM Item

The CHRAM configuration header contains settings specific to the SDRAM memory controller (EMIF). Table 27-48 describes the fields. The ROM code does not configure the EMIF by default, because it cannot assume any external SDRAM type. Therefore, if the ROM code is needed to configure the SDRAM access, the user must provide the appropriate timing details in the CHRAM structure. For more information, see Section 15.3, *EMIF Controller*, and Section 15.3.6, *EMIF Register Manual*.

Table 27-48. CHRAM Item

Offset	Field	Description
0000h	Section key	Key used for section verification: C0C0C0C2h.
0004h	Valid	Enables/disables the section: 00h: Disable Other: Enable
0005h	Reserved	
0008h	SdramConfig (EMIF1)	SDRAM configuration register (EMIF1.EMIF_SDRAM_CONFIG)
000Ch	SdramRefresh (EMIF1)	SDRAM Refresh control register (EMIF1.EMIF_SDRAM_REF_CTRL)
0010h	SdramTim1 (EMIF1)	SDRAM timing 1 register (EMIF1.EMIF_SDRAM_TIM_1)
0014h	SdramTim2 (EMIF1)	SDRAM timing 2 register (EMIF1.EMIF_SDRAM_TIM_2)
0018h	SdramTim3 (EMIF1)	SDRAM timing 3 register (EMIF1.EMIF_SDRAM_TIM_3)
001Ch	PwrMgtCtrl (EMIF1)	Power-management control register (EMIF1.EMIF_PWR_MGMT_CTRL)
0020h	DdrPhyCtrl1 (EMIF1)	DDR PHY control 1 register (EMIF1.EMIF_DDR_PHY_CTRL_1)
0024h	DdrPhyCtrl2 (EMIF1)	DDR PHY control 2 register (EMIF1.EMIF_ DDR_PHY_CTRL_2)
0028h	ModeReg1 (EMIF1)	Mode register MR1 (in the LPDDR2 device)
0029h	ModeReg2 (EMIF1)	Mode register MR2 (in the LPDDR2 device)
002Ah	ModeReg3 (EMIF1)	Mode register MR3 (in the LPDDR2 device)
002Bh	Reserved	
002Ch	SdramConfig (EMIF2)	SDRAM configuration register (EMIF2.EMIF_SDRAM_CONFIG)
0030h	SdramRefresh (EMIF2)	SDRAM refresh control register (EMIF2.EMIF_SDRAM_REF_CTRL)
0034h	SdramTim1 (EMIF2)	SDRAM timing 1 register (EMIF2.EMIF_SDRAM_TIM_1)
0038h	SdramTim2 (EMIF2)	SDRAM timing 2 register (EMIF2.EMIF_SDRAM_TIM_2)
003Ch	SdramTim3 (EMIF2)	SDRAM timing 3 register (EMIF2.EMIF_SDRAM_TIM_3)
0040h	PwrMgtCtrl (EMIF2)	Power-management control register (EMIF2.EMIF_PWR_MGMT_CTRL)
0044h	DdrPhyCtrl1 (EMIF2)	DDR PHY control 1 register (EMIF2.EMIF_DDR_PHY_CTRL_1)
0048h	DdrPhyCtrl2 (EMIF2)	DDR PHY control 2 register (EMIF2.EMIF_DDR_PHY_CTRL_2)
004Ch	ModeReg1 (EMIF2)	Mode register MR1 (in the LPDDR2 device)
004Dh	ModeReg2 (EMIF2)	Mode register MR2 (in the LPDDR2 device)
004Eh	ModeReg3 (EMIF2)	Mode register MR3 (in the LPDDR2 device)
004Fh	Reserved	
0050h	DMM LISA Map 0	DMM LISA section 0 mapping (see Section 15.2 for more information about the DMM module architecture)

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Table 27-48. CHRAM Item (continued)

Offset	Field	Description
0054h	Flags	Setting bits 0 to 3 requests ROM code to configure the appropriate channel/chip select: Bit[0]: Configure EMIF1 CS0 Bit[1]: Configure EMIF1 CS1 Bit[2]: Configure EMIF2 CS0 Bit[3]: Configure EMIF2 CS1 Other bits: Reserved

NOTE:

- The ROM code supports only the LPDDR2 memory type (as set in the SDRAM configuration register).
- It is assumed that the same kind of SDRAM (same type and timings) is attached to both CSs when requesting the configuration of both CSs for a given EMIF (for example, if bits 0 and 1 of the Flags field are set, it is assumed that both EMIF1 CSs are attached to the same kind of memory.

27.4.8.2.3 CHFLASH Item

The CHFLASH configuration header contains settings specific to the general-purpose memory controller (GPMC). For more information, see Section 15.4, *GPMC Overview*. Table 27-49 describes the fields.

Table 27-49. CHFLASH Item

Offset	Field	Description
0000h	Section Key	Key used for section verification: C0C0C0C3h.
0004h	Valid	Enables/disables the section: 00h: Disable Others: Enable
0005h	Reserved	
0008h	GPMC_SYSCONFIG (LSB)	Register values
000Ah	GPMC_IRQENABLE (LSB)	
000Ch	GPMC_TIMEOUT_CONTROL (LSB)	
000Eh	GPMC_CONFIG (LSB)	
0010h	GPMC_CONFIG1_0	
0014h	GPMC_CONFIG2_0	
0018h	GPMC_CONFIG3_0	
001Ch	GPMC_CONFIG4_0	
0020h	GPMC_CONFIG5_0	
0024h	GPMC_CONFIG6_0	
0028h	GPMC_CONFIG7_0	
002Ch	GPMC_PREFETCH_CONFIG1	
0030h	GPMC_PREFETCH_CONFIG2 (LSB)	
0032h	GPMC_PREFETCH_CONTROL (LSB)	
0034h	GPMC_ECC_CONFIG	
0036h	GPMC_ECC_CONTROL	
0038h	GPMC_ECC_SIZE_CONFIG (LSB)	
003Ch	Enable_A1_A10	0: Do not change A1– A10 pads Others: Enable A1– A10 pads

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27.4.8.2.4 CHMMCSD Item

The CHMMCSD configuration header contains settings specific to the high-speed MMC/SD/SDIO host controller (MMCHS). For more information, see Chapter 24, *MMC/SD/SDIO*. Table 27-50 describes the fields.

Table 27-50. CHMMCSD Item

Offset	Register Modified	Description
0000h	Section key	Key used for section verification C0C0C0C4h
0004h	Valid	Enables/disables the section: 00h: Disable Other: Enable
0005h	Reserved	
0008h	MMCHS_SYSCTRL(MSW)	Update MMCHS SYSCTL interface register with the value specified in these fields. The register is not updated if the value is 0xFFFFFFFF.
000Ah	MMCHS_SYSCTRL(LSW)	
000Ch	MMCHS interface bus width	1: 1 bit 2: 4 bits 4: 8 bits 0xFFFF FFFF: Do not update bus width. Others: Reserved

The ROM code provides a booting parameter structure to the initial software (see Section 27.4.8.4, *Image Execution*). This structure contains a field that indicates whether the configuration header items have been correctly processed. For a CHMMCSD item, if the MMCHS_SYSCTL and bus width fields are set to 0xFFFF FFFF, the booting parameters report that the CHMMCSD section has not been executed, regardless of the value of the Valid field.

27.4.8.3 GP Header

When the booting memory device is non-XIP (for example, MMC) the image must contain a small header, located before the executable code, and having the size of the software to load and the destination address of where to store it. Table 27-51 describes the image format. The GP header is not required when booting from an XIP memory device (for example, NOR) or in case of peripheral booting. In this case, the peripheral or memory booting image starts directly with executable code.

Table 27-51. GP Header Format

Field	Non-XIP Device Offset	XIP Device Offset	Size (Bytes)	Description
Size	0x0000	–	4	Size of the image
Destination	0x0004	–	4	Address where to store the image or code entry point
Image	0x0008	0x0000	x	Executable code

NOTE: The Destination address field stands for:

- Target address for the image copy from the non-XIP storage to the target XIP location (for example, internal RAM or SDRAM)
- Entry point for image code

Users must take care to locate the code entry point to the target address for image copy.

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27.4.8.4 Image Execution

The image is executed when the ROM code performs the branch to the first executable instruction in the initial software. For a GP device in non-XIP, the execution address is the first word after the GP header. The branch is performed in public ARM supervisor mode. The R0 register points to the booting parameter structure that contains information about booting execution. Table 27-52 shows the booting parameter structure.

Table 27-52. Booting Parameter Structure

Offset	Field	Size (Bytes)	Description
0x00	Booting message	4	Last received booting message
0x04	Memory booting device descriptor	4	Pointer to the memory device descriptor that has been used during the memory booting process
0x08	Current booting device	1	Code of device used for booting: 0x00: Void, no device 0x02: XIP memory 0x02: XIPWAIT memory (wait-signal monitoring on) 0x03: NAND 0x04: OneNAND 0x05: MMC1 0x06: MMC2(1) 0x07: MMC2(2) 0x43: UART3 0x45: USB(1) (internal transceiver) 0x46: USB-ULPI 0x47: USB(2) (internal transceiver) Others: Reserved
0x09	Reset reason	1	Current reset reason bit mask (bit = 1, event present): [0]: Power-on reset [1]: Global software warm reset [2]: Reserved [3]: MPU watchdog or WDTIMER2 reset [4]: Reserved [5]: External warm reset [6]: VDD MPU voltage manager reset [7]: VDD IVA voltage manager reset [8]: VDD Core voltage manager reset [9]: ICEPick reset [10] C2C warm reset Other bits: Reserved
0x0A	CH flags	1	Configuration header items flag. Each item is described by 1 bit. A set bit indicates that the item was executed: [0]: CHSETTINGS [1]: CHRAM [2]: CHFLASH [3]: CHMMCSD Other bits: Reserved

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27.4.9 Tracing

Tracing in the public ROM code consists in three 32-bit vectors for which each bit corresponds to a particular way point in the ROM code execution sequence. Table 27-53 through Table 27-55 list the organization of the tracing data in RAM. Tracing vectors are initialized at the beginning of the start-up phase and are updated all along the boot process.

There are two sets of tracing vectors (Table 27-13). The first set is the current trace information (after a cold or warm reset). The second set holds a copy of trace vectors collected at the first ROM code run after a cold reset. As a result, after a warm reset it is possible to have visibility on the boot scenario that occurred during a cold reset.

Table 27-53 lists the organization of tracing vector 1.

Table 27-53. Tracing Vector 1

Bit	Group	Meaning
0	General	Passed the public reset vector
1	General	Entered main function
2	General	Running after the cold reset
3	Boot	Main booting routine entered
4	Memory boot	Memory booting started
5	Peripheral boot	Peripheral booting started
6	Boot	Booting loop reached last device
7	Boot	GP header (non-XIP) found
8	Boot	Booting message Skip peripheral booting received
9	Boot	Booting message Change device received
10	Peripheral boot	Booting message Peripheral booting received
11	Peripheral boot	Booting message Get ASIC ID received
12	Peripheral boot	Device initialized
13	Peripheral boot	ASIC ID sent
14	Peripheral boot	Image received
15	Peripheral boot	Peripheral booting failed
16	Peripheral boot	Booting message not received (time-out)
17	Peripheral boot	Image size not received (time-out)
18	Peripheral boot	Image not received (time-out)
19	Reserved	
20	Configuration header	CHSETTINGS found
21	Configuration header	CHSETTINGS executed
22	Configuration header	CHRAM executed
23	Configuration header	CHFLASH executed
24	Configuration header	CHMMCSD clocks executed
25	Configuration header	CHMMCSD bus width executed
26	Reserved	
27	Reserved	
28	Software booting configuration	SWCFG general detected
29	Software booting configuration	SWCFG clocks detected
30	Software booting configuration	SWCFG time-out detected
31	Reserved	

Table 27-54 lists the organization of tracing vector 2.

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Table 27-54. Tracing Vector 2

Bit	Group	Meaning
0	Power-management IC	TWL6030 detected
1	Power-management IC	VBUS detected (in TWL6030)
2	Power-management IC	VMMC 3 V switched on (in TWL6030)
3	Power-management IC	VUSB 3.3 V switched on (in TWL6030)
4	USB	USB connect
5	USB	USB configured state
6	USB	USB VBUS valid (in USBOTGHS)
7	USB	USB session valid
8	Power-management IC	PrevStartOk set
9	USB	Suspend event
10	USB	Resume event
11	USB	Charger detected
12	Memory boot	Memory booting trial 0
13	Memory boot	Memory booting trial 1
14	Memory boot	Memory booting trial 2
15	Memory boot	Memory booting trial 3
16	Memory and peripheral boot	Execute GP image
17	Reserved	
18	Reserved	
19	Reserved	
20	Reserved	
21	Reserved	
22	Reserved	
23	Reserved	
24	Reserved	
25	Reserved	
26	Reserved	
27	Reserved	
28	Reserved	
29	Reserved	
30	Reserved	
31	MMCSD	MMCSD1 PBIAS configuration is 1.8 V.

Table 27-55 lists the organization of tracing vector 3.

Table 27-55. Tracing Vector 3

Bit	Group	Meaning
0	Memory boot	Memory booting device NULL
1	Memory boot	Memory booting device XIP
2	Memory boot	Memory booting device XIPWAIT
3	Memory boot	Memory booting device NAND
4	Memory boot	Memory booting device OneNAND
5	Memory boot	Memory booting device MMC1
6	Reserved	
7	Memory boot	Memory booting device MMC2(1)
8	Reserved	
9	Reserved	

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Table 27-55. Tracing Vector 3 (continued)

Bit	Group	Meaning
10	Reserved	
11	Memory boot	Memory booting device MMC2(2)
12	Reserved	
13	Reserved	
14	Reserved	
15	Reserved	
16	Reserved	
17	Reserved	
18	Peripheral boot	Peripheral booting device UART3
19	Reserved	
20	Peripheral boot	Peripheral booting device USB(1)
21	Peripheral boot	Peripheral booting device USB ULPI
22	Peripheral boot	Peripheral booting device USB(2)
23	Peripheral boot	Peripheral booting device NULL
24	Reserved	
25	Reserved	
26	Reserved	
27	Reserved	
28	Reserved	
29	Reserved	
30	Reserved	
31	Reserved	

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27.5 Services for HLOS Support

The ROM code provides different services that can be called on GP devices for L2 cache maintenance, wake up of slave CPU(s), etc. These services are implemented in monitor mode (the service must be called by writing the function ID into the R12 register and using the SMC instruction) and do not use any resources like RAM/stack or hardware outside the master CPU. The caller must ensure the save and restore of the processor registers before and after calling the monitor service.

The following code example shows how the monitor ROM code functions can be accessed by an application running in public mode:

```
;------------------------------------------------------------------------------ ;
FUNCTION: PL310_SetDebugL2Cache
;
; DESCRIPTION: Function calls the Monitor Service to configure the debug
;              control register of the L2 cache.
;
; INPUTS: r0 Value to set in the debug control register
;
; RETURN:
;
;------------------------------------------------------------------------------
PL310_SetDebugL2Cache FUNCTION
    PUSH {R1-R12, LR}
    LDR R12, =API_MONITOR_L2CACHE_SETDEBUG_INDEX
    SMC 0x1
    POP {R1-R12, PC}
    ENDFUNC
```

27.5.1 L2 Cache Maintenance

Table 27-56. L2 Cache Write Debug Register

Function ID	**Description**	
R12 = 0x100	This function sets the input parameter value in the L2 Cache Debug register.	
Parameters		
Type	*Location*	*Description*
Input	R0	Debug register value to set
Output		
Return		

Table 27-57. L2 Cache Clean and Invalidate Range of Physical Address

Function ID	**Description**	
R12 = 0x101	This function cleans and invalidates a range Physical Addresses. This is a workaround of the clean and invalidate L2 cache.	
Parameters		
Type	*Location*	*Description*
Input	R0 R1	Physical Start Address of the range Size of the range to invalidate
Output		
Return		

Table 27-58. Enable/Disable L2 Cache

Function ID	**Description**
R12 = 0x102	This function sets the given input value in the L2 Cache Control register (enable/disable)

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Table 27-58. Enable/Disable L2 Cache (continued)

Function ID	Description	
Parameters		
Type	*Location*	*Description*
Input	R0	Control register value to set
Output		
Return		

Table 27-59. Write Auxiliary Control Register

Function ID	Description	
R12 = 0x109	This function writes the PL310 Auxiliary Control register with the input given value in R0.	
Parameters		
Type	*Location*	*Description*
Input	R0	Value to set in the register
Output		
Return		

Table 27-60. Write Tag and Data RAM Latency Control Register

Function ID	Description	
R12 = 0x112	This function writes the PL310 Tag and Data RAM Latency Control Register with the input given value in R0 and R1.	
Parameters		
Type	*Location*	*Description*
Input	R0 R1	Tag RAM latency to set Data RAM latency to set
Output		
Return		

Table 27-61. Write Prefetch Control Register

Function ID	Description	
R12 = 0x113	This function writes the PL310 prefetch control register with the input given value in R0.	
Parameters		
Type	*Location*	*Description*
Input	RO	Value to set in the register
Output		
Return		

27.5.2 Multicore Infrastructure Maintenance

Table 27-62. Read AUX_CORE_BOOT_0 and AUX_CORE_BOOT_1 Registers

Function ID	Description
R12 = 0x103	This function reads both AUX_CORE_BOOT_0/1 registers. The function is kept for compatibility with OMAP4430 ES1.0. AUX_CORE_BOOT_0 and AUX_CORE_BOOT_1 have memory-mapped access. See Chapter 4, *Dual Cortex-A9 Subsystem*.
Parameters	

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Table 27-62. Read AUX_CORE_BOOT_0 and AUX_CORE_BOOT_1 Registers (continued)

Function ID	Description	
Type	**Location**	**Description**
Input		
Output	R0 R1	AUX_CORE_BOOT_0 register value AUX_CORE_BOOT_1 register value
Return		

Table 27-63. Modify AUX_CORE_BOOT_0

Function ID	Description	
R12 = 0x104	This function modifies the AUX_CORE_BOOT_0 register used as a status bit. The function sets and clears the bit given in the parameter and returns the new register value after operation. This function is kept for compatibility with OMAP4430 ES1.0. AUX_CORE_BOOT_0 has memory-mapped access. See Chapter 4, *Dual Cortex-A9 Subsystem*.	
Parameters		
Type	**Location**	**Description**
Input	R0 R1	Bit mask to set Bit mask to clear
Output		
Return	R0	AUX_CORE_BOOT_0 register new value

Table 27-64. Write AUX_CORE_BOOT_1

Function ID	Description	
R12 = 0x105	This function sets the value of the AUX_CORE_BOOT_1 register value used to give the CPU1 boot address. The given address can be virtual or physical. CPU1 MMU must be enabled before jumping to this address. This function is kept for compatibility with OMAP4430 ES1.0. AUX_CORE_BOOT_1 has memory-mapped access. See Chapter 4, *Dual Cortex-A9 Subsystem*.	
Parameters		
Type	**Location**	**Description**
Input	R0	Value to set in the register
Output		
Return		

Table 27-65. Read WKG_CONTROL_0/1 Register

Function ID	Description	
R12 = 0x106	This function returns the value of the WKG_CONTROL_0/1 register (CPU0 or CPU1) depending on the input parameter value. The function is kept for compatibility with OMAP4430 ES1.0. See the memory mapping and description in Chapter 4, *Dual Cortex-A9 Subsystem*.	
Parameters		
Type	**Location**	**Description**
Input	R0	CPU ID
Output		
Return	R0	Value of the WKG_CONTROL_0/1 register

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Table 27-66. Clear WKG_CONTROL_0/1 Register

Function ID	Description	
R12 = 0x107	This function clears the given bit mask of the WKG_CONTROL_0/1 register depending on the CPU ID.	
Parameters		
Type	**Location**	**Description**
Input	R0 R1	CPU ID Bit mask to clear
Output		
Return		

27.5.3 Snoop Control Unit (SCU)

Table 27-67. Set Power Status Register

Function ID	Description	
R12 = 0x108	This function sets the power status register of the CPU and cleans the full CPU L1 data cache, if the cache will be switched off when CPU enters into low-power state.	
Parameters		
Type	**Location**	**Description**
Input	R0 R1	CPU power state value to set (0x2: CSWRET, 0x3: OFF) L1 data cache state (0x00: RET, 0xFF: OFF)
Output		
Return		

27.5.4 Lockdown Translation Lookaside Buffers (TLBs)

Table 27-68. Select the TLB Entry for Read

Function ID	Description	
R12 = 0x10A	This function writes the Select Lockdown TLB Entry for Read register.	
Parameters		
Type	**Location**	**Description**
Input	R0	TLB entry
Output		
Return		

Table 27-69. Select the TLB Entry for Write

Function ID	Description	
R12 = 0x10B	This function writes the Select Lockdown TLB Entry for Write register.	
Parameters		
Type	**Location**	**Description**
Input	R0	TLB entry
Output		
Return		

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Table 27-70. Read the TLB VA Entry

Function ID	Description	
R12 = 0x10C	This function reads the Lockdown TLB VA register (Selected TLB Entry for Read).	
Parameters		
Type	**Location**	**Description**
Input		
Output		
Return	R0	Value of the register

Table 27-71. Write the TLB VA Entry

Function ID	Description	
R12 = 0x10D	This function writes the Lockdown TLB VA register (Selected TLB Entry for Write). The NS bit is forced to 1.	
Parameters		
Type	**Location**	**Description**
Input	R0	Value to write
Output		
Return		

Table 27-72. Read the TLB PA Entry

Function ID	Description	
R12 = 0x10E	This function reads the Lockdown TLB PA register (Selected TLB Entry for Read).	
Parameters		
Type	**Location**	**Description**
Input		
Output		
Return	R0	Value of the register

Table 27-73. Write the TLB PA Entry

Function ID	Description	
R12 = 0x10F	This function writes the Lockdown TLB PA register (Selected TLB Entry for Write).	
Parameters		
Type	**Location**	*Description*
Input	R0	Value to write
Output		
Return		

Table 27-74. Read the TLB Attributes Entry

Function ID	Description	
R12 = 0x110	This function reads the Lockdown TLB Attributes register (Selected TLB Entry for Read).	
Parameters		
Type	**Location**	**Description**
Input		
Output		

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Table 27-74. Read the TLB Attributes Entry (continued)

Function ID	Description	
Return	R0	Value of the register

Table 27-75. Write the TLB Attributes Entry

Function ID	Description	
R12 = 0x111	This function writes the Lockdown TLB Attributes register (Selected TLB Entry for Write). The NS bit is forced to 1.	
Parameters		
Type	**Location**	**Description**
Input	R0	Value to write
Output		
Return		

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On-Chip Debug Support

This chapter describes the on-chip debug support.

NOTE: The L3 interconnect is instantiation of the NoC interconnect from Arteris, Inc. Arteris is a registered trademark of Arteris, Inc.

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NoC is an abbreviation for Network On Chip.

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28.1 Introduction

Debugging a system containing an embedded processor involves an environment that connects high-level debugging software, executing on a host computer, to a low-level debug interface supported by the target device. In between these levels is a debug and trace controller (DTC) that facilitates communication between the host debugger and the debug support logic on the target chip.

A combination of hardware and software that connects the host debugger to the target system, the DTC uses one or more hardware interfaces and/or protocols to convert actions dictated by the debugger user to JTAG® commands and scans that execute the core hardware.

The debug software and hardware components let the user control multiple central processing unit (CPU) cores embedded in the device in a global or local manner. This environment provides:

- Synchronized global starting and stopping of multiple processors
- Starting and stopping of an individual processor
- Each processor can generate triggers that can be used to alter the execution flow of other processors.

System topics include but are not limited to:

- System clocking and power-down issues
- Interconnection of multiple devices
- Trigger channels

For easy integration into applications, a set of libraries (APIs) for debug-IP programming and a software message library are being provided. CToolsLib is a collection of embedded target APIs/library to enable easy programmatic access to the chip tools (CTools), which are system-level debug facilities included in the debug subsystem capabilities of TI devices. More information about the APIs, download files, and other useful links for available libraries can be found on the CToolsLib Wiki site:

http://processors.wiki.ti.com/index.php/CToolsLib

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28.2 Debug Ports

28.2.1 IEEE1149.1

The target debug interface has the following signals:

- Five standard IEEE1149.1 JTAG signals: nTRST, TCK, TMS, TDI, and TDO
- A return clock (RTCK) due to the clocking requirements of the ARM968™ processor
- Two EMU [1:0] or five EMU [4:0] TI extensions, depending on the pin count (14 pins or 20 pins) in the JTAG header of the device.

Table 28-1 describes the IEEE1149.1 signals.

Table 28-1. IEEE1149.1 Signals

Pin Name	Internal Signal Name	Type (1)	Pull Type (3)	Function	Description
jtag_ntrst	nTRST	I	PD	Test reset	When asserted (active low), causes all test and debug logic in the device to be reset along with the IEEE1149.1 interface
jtag_tck	TCK	I	PD	Test clock	This is the test clock used to drive an IEEE1149.1 test access port (TAP) state-machine and logic. This is a free-running clock or a gated clock, depending on the DTC attached to the device and the RTCK monitoring.
jtag_rtck	RTCK	O	N/A	Returned (synchronized) test clock	Depending on the DTC attached to the device, either the JTAG signals are clocked from RTCK or the RTCK is monitored by the DTC to the gate TCK.
jtag_tms_tmsc	TMS	I	PU	Test mode select	Directs the next state of the IEEE1149.1 TAP state-machine
jtag_tdi	TDI	I	PU	Test data input	Scans data input to the device
jtag_tdo	TDO	O	PU	Test data output	Scans data output by the device
dpm_emu0	EMU0	IO	PU	Emulation 0	Channel 0 trigger OR boot mode OR trace port
dpm_emu1	EMU1	IO	PU	Emulation 1	Channel 1 trigger OR boot mode OR trace port
dpm_emu2(2)	EMU2(2)	O	PD	Emulation 2	Trace port
dpm_emu3(2)	EMU3(2)	O	PD	Emulation 3	Trace port
dpm_emu4(2)	EMU4(2)	O	PD	Emulation 4	Trace port

(1) I = Input; O = Output

(2) 20-pin JTAG header only

(3) Internal pullup (PU)/pulldown (PD)

For information about the JTAG ID code value, see Chapter 1, *Introduction*.

28.2.2 IEEE1149.7

Besides the standard (legacy) JTAG mode of operation, the target debug interface can also be switched to a compressed JTAG mode of operation, commonly referred to as IEEE1149.7 standard. An IEEE1149.7 adapter module runs a 2-pin communication protocol on top of an IEEE1149.1 JTAG TAP. The debug-IP logic serializes the IEEE1149.1 transactions, using a variety of compression formats, to reduce the number of pins needed to implement a JTAG debug port. The device implements only a subset of the IEEE1149.7 protocol (see Table 28-3).

NOTE: At power-on-reset (POR), the default debug interface mode is IEEE1149.1. See the IEEE1149.7 specification for the scan sequence required to switch modes.

The IEEE1149.7 communication protocol can switch between serial and parallel formats. The parallel

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format consists of the IEEE1149.1 signals, TCK, TMS, TDI, TDO, nTRST, and a RTCK return clock, if stalls are required. The serial format uses two signals, TCK and TMSC. The values of the TMS, TDI, TDO, and RTCK signals are multiplexed on the bidirectional pin, jtag_tms_tmsc, by the Debug-IP logic. Each TCK of the DTC is serialized into a packet, which is transmitted to the IEEE1149.7 adapter, where it is converted back to parallel. The TDO and RTCK information are returned during the packet transmission.

NOTE: Only MScan, Oscan0, and Oscan4 formats can be used if the device requires stalls.

Table 28-2 describes the IEEE1149.7 signals.

Table 28-2. IEEE1149.7 Signals

Pin Name	Internal Signal Name	Type (1)	Pull Type (2)	Function	Description
jtag_tck	TCK	I	PD	Test clock	This is the test clock used to drive an IEEE1149.1 TAP state-machine and logic. This is a free-running clock or a gated clock, depending on the DTC attached to the device and the TMSC RDY field monitoring.
jtag_tms_tmsc	TMSC	I/O	PU	Test mode control and data scan	Compressed JTAG packet. The TMSC signal is driven only when the TCK signal is low. The signal level must be maintained by a keeper while the TCK signal is high.

(1) I = Input; O = Output

(2) Internal pullup (PU)/pulldown (PD)

Table 28-3 summarizes the IEEE1149.7 features subset supported by the device.

Table 28-3. IEEE1149.7 Features Subset

	IEEE1149.7 Feature	Device Support	Comment
Configuration	Class 4 TAP	✓	Supports 2-pin operation
	Class 5 TAP	–	No BDX or CDX channel
Optional Components	FRST	–	Functional reset (done via ICEPick)
	TRST	–	Test reset
	RDBK capability	✓	Read back of register data
	Aux Pin Functions	–	Reuse of TDI and TDO pins
	TCKWID	✓	Programmable TCK width
Scan Formats	JScan0	✓	Parallel mode
	JScan1	✓	Parallel with firewall
	JScan2	✓	Parallel with super-bypass select
	JScan3	✓	Parallel with register select
	SScan0	–	Segmented scan
	SScan1	–	Segmented scan + stalls
	SScan2	–	Segmented scan
	SScan3	–	Segmented scan + stalls
	Oscan0	✓	Support stalls
	Oscan1	✓	Nonstall mode
	Oscan2	✓	Bidirectional transfers
	Oscan3	✓	Host to target only
	Oscan4	✓	Support stalls
	Oscan5	✓	Pipelined
	Oscan6	✓	Bidirectional transfers
	Oscan7	✓	Host to target only
	Mscan	✓	Multi devices mode + stalls

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Table 28-3. IEEE1149.7 Features Subset (continued)

	IEEE1149.7 Feature	Device Support	Comment
Power Control	Power down logic	–	Handled by ICEMelter

28.2.3 Trace Port

On-chip debug and trace events can be exported to external equipment through the trace port in the device. The following exportable debug events and trace sources are supported:

- Debug events
  - Triggers. For more information about triggers, see Section 28.4.2, *Cross-Triggering*.
- Trace sources
  - Processor trace: Cortex-A9 MPU trace supported by program trace macrocell (PTM) and trace port interface unit (TPIU) modules. Fore more information about processor trace, see Section 28.7, *Processor Trace*.
  - System trace: Trace coming from various system Instrumentation modules and supported by system trace module (STM). For more information about system trace, see Section 28.8, *System Instrumentation*.

Note that not all debug and trace features can be supported concurrently due to limited amount of pins allocated to debug. Thus, a multiplexing among debug and trace sources is implemented. The configuration and the debug/trace source selection are done through the debug resource manager (DRM) module embedded in the debug subsystem.

Table 28-4 describes the trace port signals.

Table 28-4. Trace Port Signals

Pin Name	Internal Signal Name	I/O	Pull Type (1)	Description
dpm_emu19	EMU19	O	PD	Debug resource manager pin 19
dpm_emu18	EMU18	O	PD	Debug resource manager pin 18
dpm_emu17	EMU17	O	PD	Debug resource manager pin 17
dpm_emu16	EMU16	O	PD	Debug resource manager pin 16
dpm_emu15	EMU15	O	PD	Debug resource manager pin 15
dpm_emu14	EMU14	O	PD	Debug resource manager pin 14
dpm_emu13	EMU13	O	PD	Debug resource manager pin 13
dpm_emu12	EMU12	O	PD	Debug resource manager pin 12
dpm_emu11	EMU11	O	PD	Debug resource manager pin 11
dpm_emu10	EMU10	O	PD	Debug resource manager pin 10
dpm_emu9	EMU9	O	PD	Debug resource manager pin 9
dpm_emu8	EMU8	O	PD	Debug resource manager pin 8
dpm_emu7	EMU7	O	PD	Debug resource manager pin 7
dpm_emu6	EMU6	O	PD	Debug resource manager pin 6
dpm_emu5	EMU5	O	PD	Debug resource manager pin 5
dpm_emu4	EMU4	O	PD	Debug resource manager pin 4
dpm_emu3	EMU3	O	PD	Debug resource manager pin 3
dpm_emu2	EMU2	O	PD	Debug resource manager pin 2
dpm_emu1	EMU1	I/O	PU	Debug resource manager pin 1
dpm_emu0	EMU0	I/O	PU	Debug resource manager pin 0

(1) Internal pullup (PU)/pulldown (PD)

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NOTE: The dpm_emu[19:0] pins are shared with other functional (application) pins on the device boundary. To use the dpm_emu[19:0] pins, user must program the device application pin manager (control module) appropriately. For more information, see Chapter 18, *Control Module*.

For more information about DRM multiplexing and concurrent debug modes, see Section 28.9, *Concurrent Debug Modes*.

28.2.4 End Product

For an end product phone, there are usually severe connectivity constraints and the standard debug ports may not be available at board level. This could make it difficult to trace and debug software.

To ease the process of tracing and debugging, a Narrow Interface for Debug and Test (NIDnT) concept defined by MIPI is used. NIDnT is based on IEEE1149.7 and STM interfaces and re-uses application interface pins. In the context of the device, the application interface that can serve as a NIDnT port is the MMC1 interface. To use the NIDnT port, the relevant MMC1 pins must be set to the appropriate MUX mode through control module.

Table 28-5 shows the NIDnT port re-using MMC interface pins along with the corresponding MUX modes.

Table 28-5. NIDnT Port Reusing MMC Interface Pins

Module	Control Module Multiplexing		
	MUX0 (MMC)	MUX2 (STM)	MUX4 (IEEE1149.7)
Extension card (MMC)	sdmmc1_clk	dpm_emu19	–
	sdmmc1_cmd	uart1_rx	–
	sdmmc1_dat0	dpm_emu18	–
	sdmmc1_dat1	dpm_emu17	–
	sdmmc1_dat2	dpm_emu16	jtag_tms_tmsc
	sdmmc1_dat3	dpm_emu15	jtag_tck

NOTE: The nTRST signal must be driven high for the MMC1 interface to be used for IEEE1149.7 protocol.

NOTE: Uart1_rx is an optional return channel. Depending on the trace receiver, the return channel is implemented by IEEE1149.1/IEEE1149.7.

For more information about how to configure the proper MUX mode, see Chapter 18, *Control Module*.

For more information about the NIDnT concept, see *MIPI Alliance Test and Debug – NIDnT-Port* specification.

28.2.5 Trace Connector and Board Layout Considerations

Because the device supports processor trace and system trace export, a 60-pin header in place of the traditional TI 14-pin, or a TI 20-pin emulation header may be required at board level. For more information about the trace connectors and board layout considerations for these high-speed signals, see *Emulation and Trace Headers* (TI literature number SPRU655).

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28.3 Debugger Connection

28.3.1 ICEPick Module

The debugger connects to the device through its JTAG interface. The first level of debug interface seen by the debugger is the IEEE1149.7 adapter connected to the ICEPick module embedded in the debug subsystem.

NOTE: ICEPick version D (ICEPick-D) is used in the device.

System-on-chip (SoC) designs typically have multiple processors, each having a JTAG test access port (TAP) embedded in the processor. The ICEPick module manages these TAPs and the power, reset, and clock controls for modules that have TAPs.

The ICEPick module is visible only from the debugger point of view, and thus cannot be programmed by application software. The debugger can configure ICEPick through its own TAP controller. The ICEPick TAP has an instruction length of 6 bits and is the primary TAP. It is always visible in the scan chain and is used to control and monitor the other secondary TAPs.

ICEPick provides the following debug capabilities:

- Debug connect logic for enabling or disabling most ICEPick instructions
- Dynamic TAP insertion
  - Serially linking up to 16 TAP controllers
  - Individually selecting one or more of the TAPs for scan without disrupting the instruction register (IR) state of other TAPs
- Power, reset, and clock management
  - Provides the power and clock states of each domain
  - Provides debugger control of the power domain of a processor. Can force the domain power and clocks on, and prohibit the domain from being clock-gated or powered down while a debugger is connected.
  - Applies system reset
  - Provides wait-in-reset (WIR) boot mode
  - Provides global and local WIR release
  - Provides global and local reset blocking

The ICEPick module implements a connect register, which must be configured with a predefined key to enable the full set of JTAG instructions. Once the debug connect key has been properly programmed, ICEPick signals and subsystems emulation logics should be turned on.

For more information about ICEPick dynamic TAP insertion, see Section 28.3.3, *Dynamic TAP Insertion*.

For more information about ICEPick power, reset, and clock management features, see Section 28.5, *Power, Reset, and Clock Management Debug Support*.

28.3.2 Boot Modes

The initial configuration of ICEPick is determined by the level of the dpm_emu0 and dpm_emu1 pins upon POR release. At POR, dpm_emu0 and dpm_emu1 are automatically configured as inputs. The dpm_emu0 and dpm_emu1 pins are free once POR has been released.

Table 28-6 summarizes the ICEPick boot modes.

Table 28-6. ICEPick Boot Modes Upon POR

dpm_emu1	dpm_emu0	TAPs in the TDI → TDO Path	Other Effects/Comments
0	0	None	Reserved (do not use)
0	1	None	Reserved (do not use)
1	0	ICEPick	TAP only + wait-in-reset mode

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Table 28-6. ICEPick Boot Modes Upon POR (continued)

dpm_emu1	dpm_emu0	TAPs in the TDI → TDO Path	Other Effects/Comments
1	1	ICEPick	TAP only (default mode)

28.3.2.1 Default Boot Mode

In ICEPick-only configuration, none of the secondary TAPs are selected. The ICEPick TAP is the only TAP between device-level TDI and TDO pins. This is the recommended boot mode.

28.3.2.2 Wait-In-Reset

The device can boot to invoke WIR mode. If the device is booted in this mode, all processors within the device that support a TAP through ICEPick are held in reset until released. Individual processors may be released from reset (local), or all processors held in the reset state may be released at the same time (global).

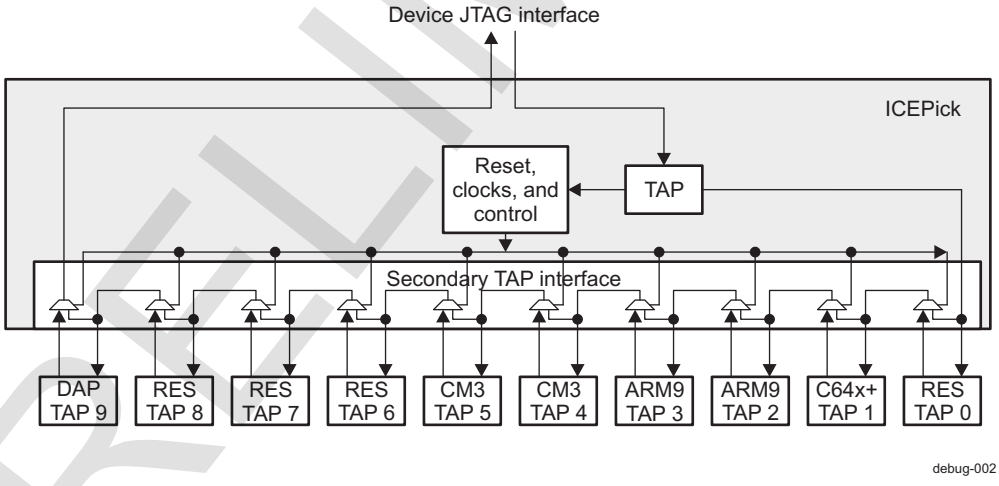
28.3.3 Dynamic TAP Insertion

28.3.3.1 ICEPick Secondary TAPs

To include more or fewer secondary TAPs in the scan chain, the debugger must use the ICEPick TAP router to program the TAPs. At its root, ICEPick is a scan-path linker that lets the DTC selectively choose which subsystem TAPs are accessible through the device-level debug interface. Each secondary TAP can be dynamically included in or excluded from the scan path. From external JTAG interface point of view, secondary TAPs that are not selected appear not to exist.

Figure 28-1 shows the TAPs in the ICEPick scan chain.

Figure 28-1. ICEPick Scan Chain



NOTE: RES = Reserved/not used

CM3 = Cortex™-M3

DAP = Debug access port

Table 28-7 shows the secondary debug TAPs connected to the ICEPick scan chain along with the modules that can be accessed. The TAP number shows the position of the TAP in the scan chain.

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Table 28-7. ICEPick Secondary Debug TAP Mapping

Secondary JTAG Port	CoreSight	TAP Number	Modules Accessed Through That JTAG Port
Reserved	No	0	–
DSP subsystem	No	1	C64x+™/ICEMaker
IVA-HD iCONT1	No	2	ARM968/ICECrusher™-9
IVA-HD iCONT2 (vDMA)	No	3	ARM968/ICECrusher-9
Dual Cortex-M3 MPU subsystem	No	4	Cortex-M3 RTOS/ICECrusher-CS
	No	5	Cortex-M3 ISS CTL/ICECrusher-CS
Reserved	No	6	–
Reserved	No	7	–
Reserved	No	8	–
DAP APB-AP	Yes	9	Cortex-A9 x 2
	Yes		CS-PTM x 2
	Yes		CS-CTI x 2
	Yes		DAP-PC
	Yes		CS-ETB
	Yes		CS-TF x 2(1)
	Yes		CS-TPIU
	No		DRM
	Yes		STM
DAP AHB-AP	No	9	IVA-HD SMSET
	No		IVA-HD hardware accelerators
	No		Statistics collectors (three instances)
	No		OCP-WP
	No		CMI1
	No		CMI2
	No		PMI
Reserved	No	10–15	Reserved

(1) One instance in Cortex-A9 MPU subsystem; one instance in debug subsystem

For more information about ICEPick scan sequences (adding single or multiple TAP[s] to the scan chain), see:

http://processors.wiki.ti.com/images/3/3c/Router_Scan_Sequence.pdf

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Besides secondary debug TAPs, ICEPick supports also power, reset, and clock controls for non-JTAG debug cores. The debug cores are accessible through DAP.

Table 28-8 summarizes the ICEPick debug core mapping.

Table 28-8. ICEPick Debug Core Mapping

Debug Core #	Module
0	Cortex-A9 MPU subsystem
1	IVA-HD iLF3
2	IVA-HD iME3
3	IVA-HD CALC3
4	IVA-HD iPE3
5	IVA-HD MC3
6	IVA-HD ECD3

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28.4 Primary Debug Support

28.4.1 Processor Native Debug Support

28.4.1.1 Cortex-A9 MPU

The dual Cortex-A9 processor supports the following native debug features:

- Halt mode and monitor mode debugging
- Six breakpoints and four watch points
- Asynchronous aborts
- Performance monitoring
- Cross-triggering: Allows stopping one CPU upon debug event (for example, breakpoint) detection in the other CPU

For more information about Cortex-A9 native debug support features, see the *Cortex-A9 Technical Reference Manual*.

28.4.1.2 Cortex-M3 MPU

The Cortex-M3 processor supports the following native debug features:

- Program halt and stepping
- Hardware breakpoints, breakpoint instruction
- Data watch point on access to data add, add range, and data value
- Register value accesses
- Debug monitor exception
- Memories accesses

For more information about Cortex-M3 native debug support features, see the *Cortex-M3 Technical Reference Manual*.

28.4.1.3 DSP

This information is not available in the public domain.

28.4.1.4 IVA-HD ARM968

The ARM968E-S processor supports the following native debug features through its EmbeddedICE-RT logic:

- Two hardware watch points/breakpoints
- Halt mode and monitor mode debugging
- Debug control and status registers
- Debug communications channel

For more information about ARM968 native debug support features, see the *ARM968E-S Technical Reference Manual*.

28.4.1.5 IVA-HD Hardware Accelerators

Hardware accelerators offer the following debug capabilities through their embedded SyncBox module:

- Manual halt: Halt occurs at the SyncBox task boundary, when requested by the debugger
- Single-step execution at SyncBox task level (from 1 to *n* macroblocks depending on the user software)
- Cross-triggering: Hardware accelerator can halt, after the execution of current SyncBox task, based on trigger event detection
- Global run

Table 28-9 summarizes the debug capabilities of the hardware accelerator SyncBox.

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Table 28-9. Hardware Accelerator Debug Capability Options

Feature	iME3	iPE3	MC3	CALC3	iLF3	ECD3
Core reset	-	-	-	-	-	-
Execution request	-	-	-	-	-	-
Trigger output	-	-	-	-	-	-
Trigger input	✓	✓	✓	✓	✓	✓
Number of trigger channels	1	1	1	1	1	1
Number of counters	0	0	0	0	0	0
Number of watch points	0	0	0	0	0	0
Number of hardware breakpoints	0	0	0	0	0	0

28.4.2 Cross-Triggering

The device supports a cross-triggering feature, which provides a way to propagate debug (trigger) events from one processor subsystem/module to another. For example, a given *subsystem A* can be programmed to generate a debug event, which can then be exported as a global trigger across the device. Another *subsystem B* can be programmed to be sensitive to the trigger line input and to generate an action upon trigger detection.

Examples of debug events are: processor entering debug state, watch point match, PTM trigger, ETB full, ETB acquisition complete, etc.

Examples of debug actions are: debug request generation, restart (Cortex-A9 synchronous run), interrupt request generation, start/stop trace, etc.

Subsystems cross-triggering is consolidated at the device level by the XTRIGGER module, which is embedded in the debug subsystem.

NOTE: XTRIGGER is not programmatically visible from the JTAG interface or any device processor. Thus, cross-triggering is programmed at the subsystem level.

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28.4.2.1 SOC Level Cross-Triggering

Table 28-10 summarizes the device cross-triggering capabilities.

Table 28-10. XTRIGGER

Subsystem	Module		Cortex-A9	PTM/ETB	Cortex-M3	Cortex-M3	Target Core	IVA3-C64x	IVA-HD ARM968	IVA-HD ARM968	HWA	PMI	CMI	OCP-WP	EMU0/ EMU1
		Trigger Input / Trigger Source	✓	✓	✓	✓	-	✓	✓	✓	-	✓	✓	✓	✓
Cortex-A9 MPU subsystem	Cortex-A9	✓		✓	✓	✓	-	✓	✓	✓	-	✓	✓	✓	
	PTM / ETB	✓	✓		✓	✓	-	-	-	-	-	✓	✓	✓	-
Dual Cortex-M3 MPU subsystem	Cortex-M3	✓	✓	-		✓	-	✓	✓	✓	-	✓	✓	✓	-
	Cortex-M3	✓	✓	-	✓		-	✓	✓	✓	-	✓	✓	✓	-
ABE subsystem	Target Core	-	-	-	-	-		-	-	-	-	-	-	-	-
DSP subsystem	C64x	✓	✓	-	✓	✓	-		✓	✓	✓	✓	✓	✓	✓
IVA-HD subsystem	ARM968 iCONT	✓	✓	-	✓	✓	-	✓		✓	✓	✓	✓	✓	✓
	ARM968 vDMA	✓	✓	-	✓	✓	-	✓	✓		✓	✓	✓	✓	✓
	HWA	-	-	-	-	-	-	-	-	-		-	-	-	-
Power manager	PMI	-	-	-	-	-	-	-	-	-	-		-	-	-
Clock manager	CMI	-	-	-	-	-	-	-	-	-	-	-		-	-
Device	OCP-WP	✓	✓	✓	✓	✓	-	✓	✓	✓	-	✓	✓		✓
	EMU0, EMU1	✓	✓	✓	✓	✓	-	✓	✓	✓	-	✓	✓	✓	

NOTE: The following modules support only trigger inputs:

- IVA-HD hardware accelerators
- IVA-HD SMSET
- PMI
- CMI

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28.4.3 Suspend

The device supports a suspend feature, which provides a way to stop a "closely coupled" hardware process running on a peripheral-IP when the host processor enters debug state. The suspend mechanism is important for debug to ensure that peripheral-IPs operate in a lock-step manner with a host controller processor.

An entry is provided for each peripheral-IP that must consider the suspend signals from a number of processors (MPU or DSP). For each peripheral-IP, sensitivity to the suspend signals is defined within two possibilities (and so coded using 1bit):

- Peripheral-IP is sensitive to the suspend line request.
- Peripheral-IP ignores the suspend line request.

For more information about how to program the sensitivity, see the corresponding peripheral-IP TRM chapter.

28.4.3.1 Debug Aware Peripherals and Host Processors

Table 28-11 lists the mapping of the device processors to the suspend control input lines.

Table 28-11. Debug Subsystem Suspend Input Lines

Suspend Input Line	Host Processor
0	Reserved
1	DSP C64x
2	IVAHD iCONT1
3	IVAHD iCONT2
4	Cortex-M3 RTOS
5	Cortex-M3 ISS CTL
6	Cortex-A9 CPU0
7	Cortex-A9 CPU1

Table 28-12 lists the mapping of the device peripheral-IPs to the suspend control output lines.

Table 28-12. Debug Subsystem Suspend Output Lines

Suspend Output Line	Peripheral-IP Module
0	Keyboard controller
1	MCBSP1 (ABE)
2	MCBSP2 (ABE)
3	MCBSP3 (ABE)
4	WDTIMER3 (ABE)
5	GPTIMER5 (ABE)
6	GPTIMER6 (ABE)
7	GPTIMER7 (ABE)
8	GPTIMER8 (ABE)
9–15	Reserved
16	GPTIMER1
17	GPTIMER2
18	GPTIMER3
19	GPTIMER4
20	GPTIMER9
21	GPTIMER10
22	GPTIMER11
23	Reserved

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Table 28-12. Debug Subsystem Suspend Output Lines (continued)

Suspend Output Line	Peripheral-IP Module
24	HSI
25	I2C1
26	I2C2
27	I2C3
28	I2C4
29	Reserved
30	sDMA
31	32-kHz synchronized timer
32–36	Reserved
37	WDTIMER2

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28.5 Power, Reset, and Clock Management Debug Support

The global power, reset, and clock managment (PRCM) module implements facilities to support debug across power and clock domain cycles. The debugger can control or get the status of each power and clock domain associated with an ICEPick secondary TAP.

ICEPick provides a set of directives allowing the debugger to:

- Get visibility on the associated power and clock domains state. This includes:
  - Current power setting indicating whether the power domain is on or off
  - Loss of power detected since the software last checked the status
  - Current clock setting indicating whether the clock domain is on or off
  - Sleep desired (PM and CM indicate that the debug settings in ICEPick are changing the application state. If it were not for the ICEPick controls, the power or clock would be turned off.)
  - Subsystem reset state
  - Subsystem has entered a debug state that requires the attention of the host debug software.
- Override power/clock control settings to wake up a power or clock domain or to prevent a power or clock domain from going to sleep once it is in ACTIVE state
- Assert/block/extend reset; release from extended reset (WIR)

ICEPick handles debug power management at the device level. In addition, the device implements a second level of debug power management through the DAP-PC module integrated in the Cortex-A9 MPU subsystem, which provides the same capabilities as ICEPick for the two Cortex-A9 CPUs. Each Cortex-A9 CPU core is in its own independent power domain, which DAP-PC manages. The hierarchical debug power-management approach provided by DAP-PC at the subsystem level and by ICEPick at the device level ensures a theoretically independent debug capability for each Cortex-A9 CPU core.

NOTE: The debugger must properly sequence global ICEPick and local DAP-PC commands:

- To force clocks/power:
  1. The debugger must first force it for the Cortex-A9 MPU subsystem at the ICEPick level.
  2. The debugger must then force it for a specific Cortex-A9 CPU at the DAP-PC level.
- To release clocks/power:
  1. The debugger must first release it for a specific Cortex-A9 CPU at the DAP-PC level.
  2. The debugger must then release the Cortex-A9 MPU subsystem controls at the ICEPick level.

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28.6 Performance Monitoring

28.6.1 Cortex-A9 MPU Subsystem Performance Monitoring

28.6.1.1 Performance Monitoring Unit

The Cortex-A9 processor includes a performance monitoring unit (PMU) that enables events, such as cache misses and instructions executed, to be counted over a period of time. The PMU provides six counters to gather statistics about the operation of the processor and memory system. Each counter can count any of the events available in Cortex-A9.

The Cortex-A9 PMU outputs 52 events (PMUEVENT[51:0]) to PTM (see Table 28-13).

Table 28-13. PMU Events

PMU Event	Description
0	Software increment
1	Instruction fetch that causes a refill
2	Instruction fetch that causes a TLB refill
3	Data read or write operation that causes a refill
4	Data read or write operation that causes a cache access
5	Data read or write operation that causes a TLB refill
6	Data read architecturally executed
7	Data write architecturally executed
8,9	Number of instructions renamed: b00 = No instructions renamed b01 = One instruction renamed b10 = Two instructions renamed
10	Exception taken
11	Exception return architecturally executed
12	Change to context ID retired
13	Software change of PC
14	Immediate branch architecturally executed
15	Number of predictable function returns
16	Unaligned access architecturally executed
17	Branch mispredicted or not predicted
18	Branches or other change in program flow
19	Java byte code executed
20	Software Java byte code executed
21	Jazelle backward branches executed
22	Coherent line fill request that misses in other uniprocessors
23	Request for coherent line fill that hits in other uniprocessors
24	Instruction cache dependent stalls
25	Data cache dependent stalls
26	TLB miss dependent stalls
27	STREX passed
28	STREX failed
29	Data eviction
30	Issue does not dispatch any instruction.
31	Issue is empty.
32	Main execution unit pipe
33	Second execution unit pipe
34	Load/store pipe

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Table 28-13. PMU Events (continued)

PMU Event	Description
35, 36	Number of floating-point instructions renamed: b00 = No floating-point instruction renamed b01 = One floating-point instruction renamed b10 = Two floating-point instructions renamed
37, 38	Number of NEON instructions renamed: b00 = No NEON instruction renamed b01 = One NEON instruction renamed b10 = Two NEON instructions renamed
39	PLD stall
40	Write stall
41	Instruction main TLB miss stall
42	Data main TLB miss stall
43	Instruction micro TLB miss stall
44	Data micro TLB miss stall
45	DMB stall
46	Integer core clock enabled
47	Data engine clock enabled
48	ISB
49	DSB
50	DMB
51	External interrupt

For more information about Cortex-A9 PMU, see the *ARM Cortex-A9 Technical Reference Manual*.

28.6.1.2 Snoop Control Unit

The individual CPU event monitors can be configured to gather statistics about the operation of the snoop control unit (SCU).

28.6.1.3 L2 Cache (PL310)

The Cortex-A9 MPU subsystem includes 512KB of L2 cache and uses PL310 as the L2 cache controller. The PL310 includes logic to support cache event monitoring.

Table 28-14 summarizes the PL310 L2 cache events.

Table 28-14. PL310 L2 Cache Events

Event	Event Description
0	Eviction of a line from the L2 cache
1	Data read hit in the L2 cache
2	Data read lookup to the L2 cache. Subsequently results in a hit or miss.
3	Data write hit in the L2 cache
4	Data write lookup to the L2 cache. Subsequently results in a hit or miss.
5	Data write lookup to the L2 cache with Write-Through attribute. Subsequently results in a hit or miss.
6	Instruction read hit in the L2 cache
7	Instruction read lookup to the L2 cache. Subsequently results in a hit or miss.
8	Prefetch line-fill sent to L3
9	Allocation into the L2 cache caused by a write (with Write-Allocate attribute) miss

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The PL310 implements two 32-bit event counters. The PL310 can be configured to generate interrupts on error conditions or event counter overflow or increment. The PL310 interrupt is routed to MA_IRQ_0. When an interrupt occurs, software can look at the relevant interrupt status register to determine the source of the interrupt.

For more information about PL310, see the ARM *PrimeCell Level 2 Cache Controller (PL310) Technical Reference Manual*.

28.6.2 Cortex-M3 MPU Subsystem Performance Monitoring

28.6.2.1 Subsystem Counter Timer Module

The dual Cortex-M3 MPU subsystem includes a subsystem counter timer module (SCTM), which is embedded in shared cache and provides additional data to the user timing or profiling capability. SCTM integrates eight profiling counters that collect:

- Forty-four shared cache events
- Four sleep/deep-sleep events from Cortex-M3 cores (one sleep and one deep sleep event per core)

Table 28-15 describes the repartition of the Cortex-M3 SCTM counters.

Table 28-15. Cortex-M3 SCTM Counters Repartition

Counters	Features
0 – 1	Timer and event
2 – 3	64-bit chained + shadowing
4 – 5	64-bit chained + shadowing
6 – 7	Event

28.6.2.2 Cache Events

Table 28-16 summarizes the SCTM events for the Cortex-M3 MPU subsystem.

Table 28-16. SCTM Events for Cortex-M3 MPU Subsystem

Input Index	Event Description
1	Cache locks
2	Cache line replacements
3	Cache evictions
4	Cache maintenance operations (slave 0)
5	Cache maintenance operations (slave 1)
6	Cache maintenance operations (slave 2)
7	Cache maintenance operations (slave 3)
8	Cache OCP access (slave 0)
9	Cache OCP access (slave 1)
10	Cache OCP access (slave 2)
11	Cache OCP access (slave 3)
12	Cacheable access (slave 0)
13	Cacheable access (slave 1)
14	Cacheable access (slave 2)
15	Cacheable access (slave 3)
16	Cache bank conflicts (slave 0)
17	Cache bank conflicts (slave 1)
18	Cache bank conflicts (slave 2)
19	Cache bank conflicts (slave 3)
20	Cache allocations

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Table 28-16. SCTM Events for Cortex-M3 MPU Subsystem (continued)

Input Index	Event Description
21	Cache write buffer accesses (slave 0)
22	Cache write buffer accesses (slave 1)
23	Cache write buffer accesses (slave 2)
24	Cache write buffer accesses (slave 3)
25	Cache line fills (slave 0)
26	Cache line fills (slave 1)
27	Cache line fills (slave 2)
28	Cache line fills (slave 3)
29	Cache write fills (slave 0)
30	Cache write fills (slave 1)
31	Cache write fills (slave 2)
32	Cache write fills (slave 3)
33	Cache read fills (slave 0)
34	Cache read fills (slave 1)
35	Cache read fills (slave 2)
36	Cache read fills (slave 3)
37	Cache misses (slave 0)
38	Cache misses (slave 1)
39	Cache misses (slave 2)
40	Cache misses (slave 3)
41	Cache hits (slave 0)
42	Cache hits (slave 1)
43	Cache hits (slave 2)
44	Cache hits (slave 3)
45	Cortex-M3 ISS CTL deep sleep
46	Cortex-M3 ISS CTL sleep
47	Cortex-M3 RTOS deep sleep
48	Cortex-M3 RTOS sleep

NOTE: Input index [0] is reserved for free-running subsystem clock (used for total cycle profiling).

28.6.3 DSP Subsystem Performance Monitoring

28.6.3.1 Subsystem Counter Timer Module

The DSP subsystem includes an SCTM, which is embedded in the DSP megamodule and provides additional data to the user timing or profiling capability. SCTM integrates eight profiling counters that collect L1 and L2 events.

Table 28-15 describes the repartition of the DSP SCTM counters.

Table 28-17. DSP SCTM Counters Repartition

Counters	Features
0 – 1	Timer and event
2 – 7	Event (no chaining)

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28.6.3.2 L1 and L2 Events

Table 28-18 summarizes the SCTM events for DSP subsystem.

Table 28-18. SCTM Events for DSP Subsystem

Event	Event Description
1	L1 Slave0 (program) tag hit
2	L1 Slave1 (data) tag hit
3	L1 Slave0 (program) tag miss
4	L1 Slave1 (data) tag miss
5	L1 Slave0 (program) fill buffer hit
6	L1 Slave1 (data) fill buffer hit
7	L1 Slave1 (data) write buffer access
8	L1 Allocation FIFO
9	L1 Slave0 (program) bank conflict
10	L1 Slave1 (data) bank conflict
11	L1 Slave0 (program) cached request
12	L1 Slave1 (data) cached request
13	L1 Slave0 (program) waiting for fill buffer
14	L1 Slave1 (data) waiting for fill buffer
15	L1 Slave0 (program) waiting for maintenance
16	L1 Slave1 (data) waiting for maintenance
17	L1 Eviction occurred
18	L1 Replacement occurred
19	L1 Allocation failed due to locked lines occurred
20	L2 tag hit
21	L2 tag miss
22	L2 fill buffer hit
23	L2 write buffer access
24	L2 allocation FIFO
25	L2 cached request
26	L2 waiting for fill buffer
27	L2 waiting for maintenance
28	L2 eviction occurred
29	L2 replacement occurred
30	L2 allocation failed due to locked lines occurred
31	Tied-off to 0

NOTE: Input index [0] is reserved for the free-running subsystem clock (used for total cycle profiling).

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28.7 Processor Trace

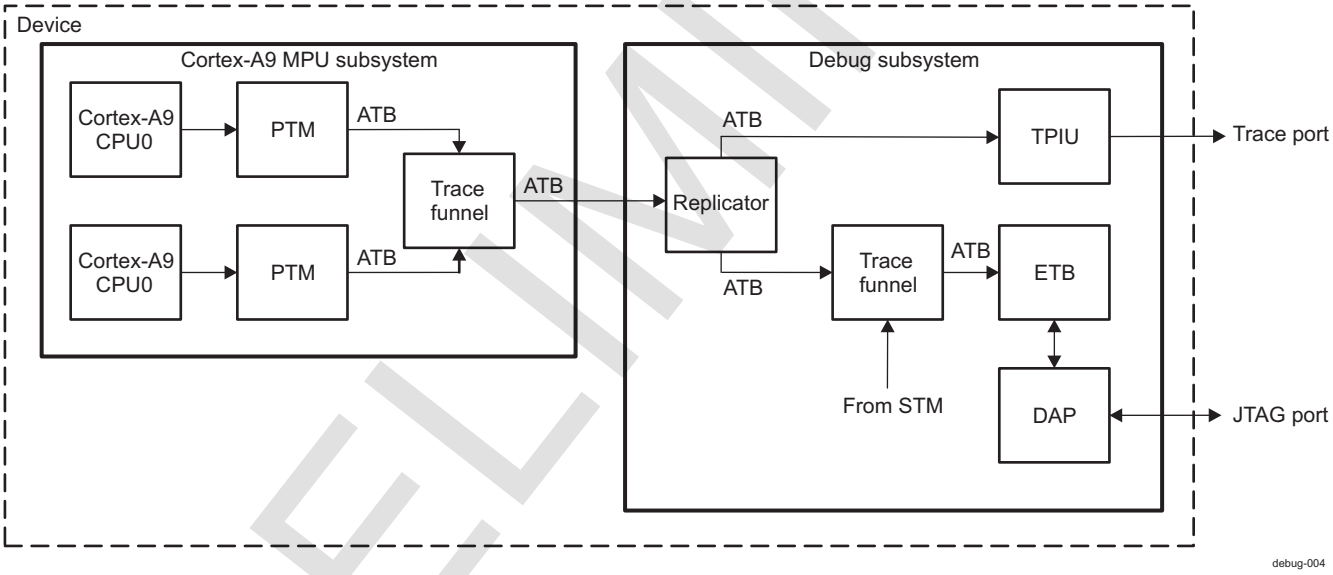
The device supports only Cortex-A9 processor trace. The main Cortex-A9 processor trace characteristics are:

- Program trace only (no data trace)
- Separate PTM for each Cortex-A9 CPU
- Trace can be:
  - Exported off-chip through TPIU in the debug subsystem (maximum number of trace data pins = 18)
  - Stored on-chip to ETB through CS-TF in the debug subsystem
- Trace can be optionally:
  - Cycle accurate useful for profiling sections of code
  - Interleaved dynamically between the two Cortex-A9 CPUs by a CS-TF embedded in the Cortex-A9 MPU subsystem

NOTE: Depending on use case, the device may not be able to interleave two cycle accurate traces without overflow (bandwidth restriction).

Figure 28-2 shows an overview of the processor trace flow.

Figure 28-2. Processor Trace Flow



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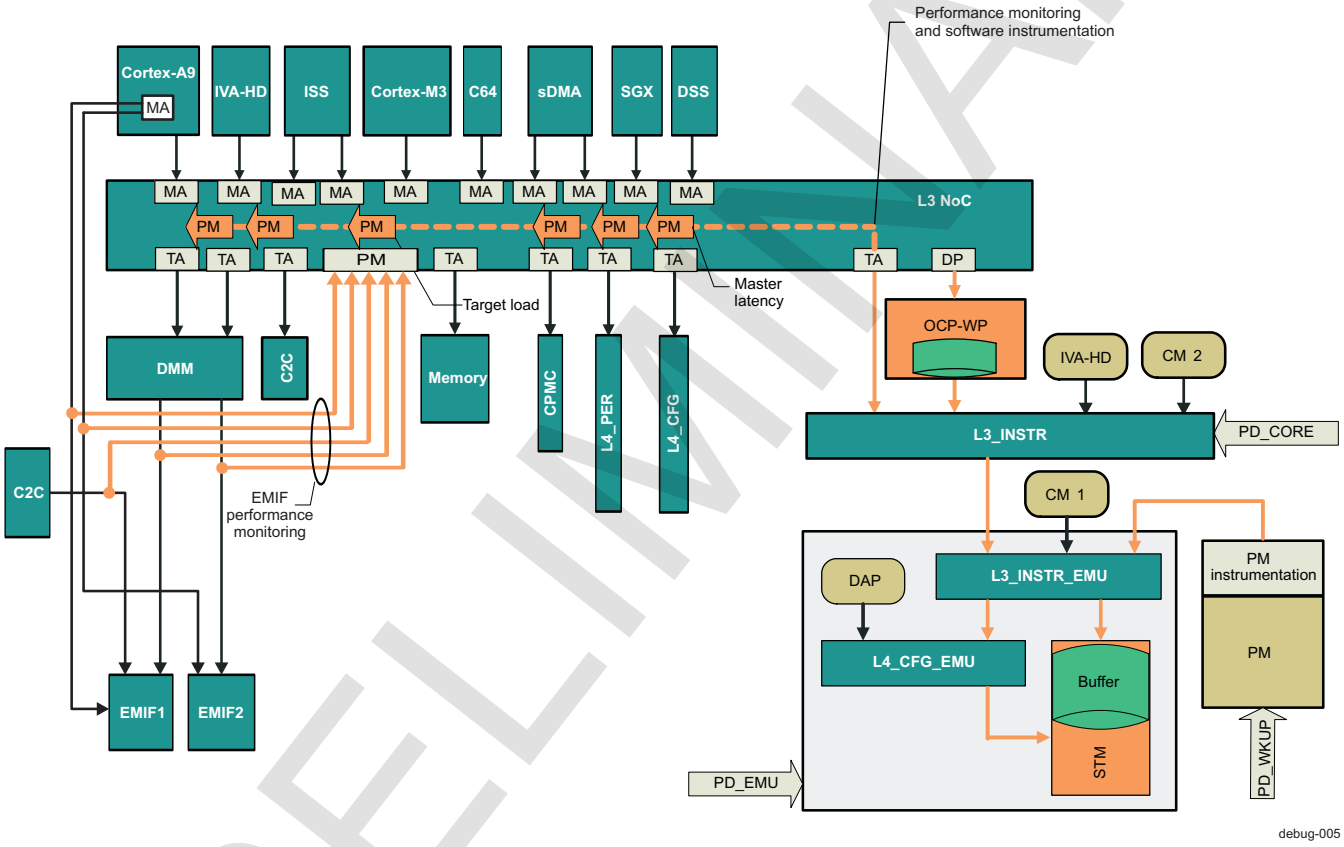
28.8 System Instrumentation

The device supports the following system instrumentation features:

- Real-time software trace (see Section 28.8.2, *Software Instrumentation*)
- OCP target traffic monitoring (see Section 28.8.3, *OCP Watch-Point*)
- OCP target load and master latency monitoring (see Section 28.8.5, *NoC Statistics Collector*)
- HWA load monitoring (see Section 28.8.4, *IVA-HD Pipeline*)
- PM events trace (see Section 28.8.6, *PM Instrumentation* [PMI])
- CM events trace (see Section 28.8.7, *CM Instrumentation* [CMI])

Figure 28-3 is an overview of the device system instrumentation framework.

Figure 28-3. System Instrumentation Framework



28.8.1 MIPI STM

MIPI-STM is a trace module that aids in software debugging. The main features of this module are:

- Implements MIPI STP protocol (rev 1.0) with the following characteristics:
  - Highly optimized for software-generated traces
  - Automatic timestamping of messages
  - Support for 8-, 16-, and 32-bit data types
- Collects the following information:
  - Software messages
  - Hardware instrumentation trace from hardware agents:
    - OCP-WP
    - PMI

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    - CMI
    - SMSET
    - L3 NoC statistics collectors
- Exports trace data to:
  - External trace receiver
  - On-chip ETB buffer
- Available in 1-, 2-, or 4-pin mode with single- or dual-edge clock, depending on the trace bandwidth requirements and characteristics of the trace receiver
- Dedicated 128 × 32-bit FIFO buffer

A maximum of 255 different bus masters can be connected to the STM trace port through a bus arbiter. STP recognizes two distinct modes of tracing (software and hardware types), which use slightly different message combinations to output different types of data. The bus masters can be configured for either type to optimize the system for the different types of trace data.

28.8.2 Software Instrumentation

The device provides support for real-time software trace through user-defined message writes to specific memory mapped register (MMR) locations. Software masters can transmit trace data from the operating system (OS) processes or tasks on 256 different channels, with each channel being defined by the software protocol implemented. The different channels can be used to group different types of data logically so that it is easy to filter out the data irrelevant to the on-going debugging task. The message structures in STP are optimized to provide an efficient transport for software data through the STM module.

The software masters are:

- Cortex-A9 MPU subsystem
- DAP (for testing purpose)
- DSP subsystem
- Dual Cortex-M3 MPU subsystem
- sDMA controller write port (SDMA_WR)
- IVA-HD subsystem

Each software master has a master-ID assigned to it.

Software messages can be interleaved with other hardware messages.

Software messages are intrusive and use both processor cycles and memory.

28.8.3 OCP Watch-Point

The L3 interconnect provides five functional probes embedded and attached to the following L3 targets:

- GPMC
- L4-PER
- L4-CFG
- DMM1 (DMM target port 1)
- DMM2 (DMM target port 2)

The probes output are muxed together and then sent to the L3 interconnect debug port. A component called OCP-WP is used to collect data from functional probes and then transmit captured data to the STM module. The OCP-WP drives a Probe-ID signal to the L3 interconnect for probe selection. The probe selection is exclusive, meaning that interleaving is not possible.

The OCP-WP provides the following main features:

- Monitoring the OCP traffic originated by all initiators that can access the selected target where the probe is attached
- Filtering OCP monitored bus traffic by:

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  - Address range
  - Initiator-ID (see Table 28-20)
  - Transaction type
  - Transaction qualifier
- Generating a trigger upon watch-point match
- Starting and stopping OCP traffic monitoring upon:
  - WP address match
  - External trigger
- OCP-WP messages can be interleaved with software messages
- Programming from:
  - Debugger
  - Application

NOTE: The OCP-WP is restricted to monitor request flow.

Table 28-19 summarizes the OCP targets that can be monitored by the OCP-WP and their respective probe-ID.

Table 28-19. L3 Interconnect Functional Probe Mapping

Probe-ID	L3 OCP Target
000	Reserved
001	GPMC
010	L4-PER
011	L4-CFG
100	DMM1 (DMM target port 1)
101	DMM2 (DMM target port 2)
110	Reserved
111	Reserved

Table 28-20 summarizes the ConnID (Initiator-ID) mapping from a debug point of view.

Table 28-20. ConnID Mapping (Debug View)

ConnID	Initiator
0x0	Cortex-A9 MPU subsystem
0x4	CS-DAP
0x8	DSP
0xC	IVA-HD
0xD	IVA-HD iCONT1 (software instrumentation)
0xE	IVA-HD iCONT2 (software instrumentation)
0x10	ISS
0x11	Dual Cortex-M3 MPU subsystem
0x12	Face detect
0x14	sDMA_RD
0x15	sDMA_WR
0x18	SGX
0x1C	Display subsystem
0x20	C2C
0x24	HSI
0x28	MMC1

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Table 28-20. ConnID Mapping (Debug View) (continued)

ConnID	Initiator
0x29	MMC2
0x30	USBHOSTHS
0x31	USBOTGHS
0x32	USBHOSTFS
0x38	Statistics collectors (all three)
0x39	OCP-WP
0x3C	IVA-HD SMSET (hardware instrumentation)
0x3D	PMI
0x3E	CMI1
0x3F	CMI2
Other values	Reserved

NOTE: For information about ConnID values from a protection/error logging point of view, see Section 13.2.3.2.3, Master NIU Identification, in Chapter 13, Interconnect,

28.8.4 IVA-HD Pipeline

The device takes advantage of the system trace infrastructure to provide visibility to the user regarding IVA-HD micro-task sequencing. This is supported through a SMSET module instantiated in the IVA-HD subsystem. The micro-task boundaries are handled as generic events and encapsulated in STP messages with an event-ID and local timestamp and exported through the MIPI-STM module.

The IVA-HD instrumentation scheme allows the user to understand micro-task dependencies, hardware accelerators load balancing, and potential bottlenecks. DMA transfer boundaries are reported as IVA-HD events. Software messages from ARM968 execution can be interleaved with IVA-HD events.

28.8.5 NoC Statistics Collector

The L3 interconnect supports a built-in performance monitoring feature by implementing a statistics collector (SC) component, which computes traffic statistics within a user-defined window and periodically reports to the user through the MIPI-STM interface. Three SC instances are instantiated in the device:

- One statistics collector dedicated to SDRAM load monitoring – SC_SDRAM (see Section 28.8.5.1, *L3 Target Load Monitoring*, for more information)
- Two statistics collectors dedicated to master latency monitoring – SC_LAT0 and SC_LAT1 (see Section 28.8.5.2, *L3 Master Latency Monitoring* , for more information)

Statistics collectors (SDRAM and LAT0/1) can report:

- Average burst length in bytes/packet per sampling window
- Average throughput in bytes/cycle
- % Link occupancy on the request link (for store transactions) during a sampling window
- % Link occupancy on the response link (for load transactions) during a sampling window
- % Arbitration conflict cycles on the request link
- % Initiator busy cycles on the response link
- Histogram of payload length in bytes (for example, 0–16 , 16–32, 32–128) each sampling window.
- Histogram of quality of service (QoS) metric for IVA-HD initiator (for example, low priority, high priority) each sampling window.

The performance metrics are interleaved with software instrumentation data at the L3 interconnect level.

The performance monitoring probes implement three main functions:

- Events detection

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- Transactions filtering
- Aggregation

The probes can be configured to detect the events summarized in Table 28-21.

Table 28-21. Performance Monitoring Events Detection

Event	Definition
NONE	No event selected
ANY	Any clock cycles
TRANSFER	Word has been accepted by the receiver.
WAIT	Transfer has been initiated but the transmitter currently has no data to send.
BUSY	Receiver applies flow control
PKT	Transfer of a new packet header
DATA	Transfer of a payload word
IDLES	No communication over the link
LATENCY	Debug bit detection

The probes can be configured to filter the traffic based on the criteria summarized in Table 28-22.

Table 28-22. Performance Filtering Options

Probe Filtering Options	Comment
Master address	Mask and match
Slave address(1)	
UserInfo	
Read	
Write	
Error	
OCP address(2)	

(1) SC_LAT0/1 only
(2) SC_SDRAM only

Table 28-23 specifies the slave address mapping (SC_LAT0/1 only).

Table 28-23. Statistics Collector Slave Address Mapping

Slave	Address (hex)
HOST CLK1	0
DMM1 – NIU	1
DMM2 – NIU	2
ABE – NIU	3
L4_CFG – NIU	4
HOST CLK2	6
GPMC – NIU	7
OCM_RAM – NIU	8
DSS – NIU	9
ISS – NIU	A
CORTEX-M3 – NIU	B
SGX – NIU	C
IVA-HD – NIU	D
SL2 – NIU	E
L4_PER0 – NIU	F
L4_PER1 – NIU	10

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Table 28-23. Statistics Collector Slave Address Mapping (continued)

Slave	Address (hex)
L4_PER2 – NIU	11
L4_PER3 – NIU	12
Reserved	13
Reserved	14
Reserved	15
C2C – NIU	16
HOST CLK3	18
DEBUGSS – NIU	19

The probes implement a user-defined set of counters that aggregate the events sampled by the detector and filtered according to the user setup.

NOTE: Statistics collectors counter values are not accessible by application software.

Table 28-24 summarizes the performance probe aggregation modes.

Table 28-24. Aggregation Modes

Aggregation Mode	Description
FILTER_HIT	The counter increments by 1 when the filter hits.
MIN_MAX_HIT	The counter increments by 1 when the filter hits and the selected event information is within range. - Payload length (bytes) - Pressure value - Request/response latency (clock cycles)
EVT_INFO	The selected event information is added to the counter value when the filter hits. Payload length (bytes) Pressure value Request/response latency (clock cycles)
AND_FILTER	The counter increments by 1 when all unit filters hit.
OR_FILTER	The counter increments by 1 when at least one unit filter hits.
SUM_REQ_EVT	The counter sums the events from any request port.
SUM_RSP_EVT	The counter sums the events from any response port.
SUM_ALL_EVT	The counter sums the events from any port.
EXT_EVT	The counter increments by 1 when selected external event input signal is sampled high.

28.8.5.1 L3 Target Load Monitoring

The L3 interconnect implements five performance monitoring probes on LPDDR2 memory channels. The traffic statistics are computed within a user-defined window and periodically reported to the user through the MIPI-STM interface.

SC_SDRAM supports the following main features:

- Five probe inputs
  - Probe 0 – EMIF1 (DMM-EMIF1 128-bit port)
  - Probe 1 – EMIF2 (DMM-EMIF2 128-bit port)
  - Probe 2 – Memory Adapter 1 (MA-EMIF1 128-bit port)
  - Probe 3 – Memory Adapter 2 (MA-EMIF2 128-bit port)
  - Probe 4 – EMIF modem (C2C-EMIF1 64-bit port)
- Eight 16-bit counters shared concurrently

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  - Counter 0 with two filters
  - Counter 1 with one filter
  - Counter 2 with two filters
  - Counter 3 with one filter
  - Counter 4 with one filter
  - Counter 5 with one filter
  - Counter 6 without any filter
  - Counter 7 without any filter
- Simple (with one element) or complex (with several elements) filters available
- Filtering according to:
  - Initiator of traffic
  - Access priorities
  - OCP address
- No latency counter. Only bandwidth measurement on this collector
- 16-bit collecting window counter
- Dump Identifier is 0x0 (tie-off value)
- Dumps frames at L3 interconnect slave address 0x19 (debug subsystem)

Table 28-25 summarizes the SC_SDRAM configuration.

Table 28-25. SC_SDRAM Configuration

Counters	Min Max	Filter Elements	L3 Target				
Counter 0	Yes	2	EMIF1	EMIF2	MA1	MA2	EMIF modem
Counter 1	Yes	1	EMIF1	EMIF2	MA1	MA2	EMIF modem
Counter 2	Yes	2	EMIF1	EMIF2	MA1	MA2	EMIF modem
Counter 3	Yes	1	EMIF1	EMIF2	MA1	MA2	EMIF modem
Counter 4	Yes	1	EMIF1	EMIF2	MA1	MA2	EMIF modem
Counter 5	Yes	1	EMIF1	EMIF2	MA1	MA2	EMIF modem
Counter 6	Yes	No	No	No	No	No	EMIF modem
Counter 7	Yes	No	No	No	No	No	EMIF modem

28.8.5.2 L3 Master Latency Monitoring

The device L3 interconnect implements nine performance monitoring probes on the main L3 initiators:

- Cortex-A9 MPU subsystem
- DSP
- sDMA controller read port (SDMA_RD)
- sDMA controller write port (SDMA_WR)
- IVA-HD
- DSS
- ISS
- SGX
- Dual Cortex-M3 MPU subsystem

The master latency statistics are computed within a user-defined window and periodically reported to the user through the MIPI-STM interface.

The probes can be configured to filter latencies in four classes and report to the user a latency distribution along execution.

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Because the performance metrics and the software events are exported through a unified export channel, it is possible to correlate latency trends with on-going execution and system context.

Because computing latency requires maintaining the state between request and response ports, the probe cannot compute latency statistics on 100 percent of the initiator traffic. Hence, latency histograms must be extracted on large execution windows to be accurate.

28.8.5.2.1 SC_LAT0 Configuration

SC_LAT0 supports the following main features:

- Six probe inputs:
  - Probe 0: Cortex-A9 MPU subsystem
  - Probe 1: DSP subsystem
  - Probe 2: SDMA_RD
  - Probe 3: SDMA_WR
  - Probe 4: DSS
  - Probe 5: ISS
- Four 16-bit counters shared concurrently:
  - Counter 0 with one filter
  - Counter 1 with one filter
  - Counter 2 with one filter
  - Counter 3 with one filter
- Filtering according to:
  - L3 target
  - Access priorities
- 10-bit counter for latency measurement
- 16-bit collecting window counter
- Identifier is 0x1 (tie-off value)
- Dumps frames at slave address 0x19 (DEBUGSS)

Table 28-26 summarizes the SC_LAT0 configuration.

Table 28-26. SC_LAT0 Configuration

Counters	Min Max	Filter Elements	L3 Master					
Counter 0	Yes	1	Cortex-A9 MPU subsystem	DSP	SDMA_RD	SDMA_WR	DSS	ISS
Counter 1	Yes	1	Cortex-A9 MPU subsystem	DSP	SDMA_RD	SDMA_WR	DSS	ISS
Counter 2	Yes	1	Cortex-A9 MPU subsystem	DSP	SDMA_RD	SDMA_WR	DSS	ISS
Counter 3	Yes	1	Cortex-A9 MPU subsystem	DSP	SDMA_RD	SDMA_WR	DSS	ISS

28.8.5.2.2 SC_LAT1 Configuration

SC_LAT1 supports the following main features:

- Five probe inputs:
  - Probe 0: IVA-HD
  - Probe 1: Cortex-A9 MPU subsystem
  - Probe 2: SDMA_WR
  - Probe 3: SGX

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  - Probe 4: Dual Cortex-M3 MPU subsystem
- Four 16-bit counters shared concurrently:
  - Counter 0 with one filter
  - Counter 1 with one filter
  - Counter 2 with one filter
  - Counter 3 with one filter
- Filtering according to:
  - L3 target
  - Access priorities
- 10-bit counter for latency measurement
- 16-bit collecting window counter
- Identifier is 0x2 (tie-off value)
- Dumps frames at slave address 0x19 (DEBUGSS)

Table 28-27 summarizes the SC_LAT1 configuration.

Table 28-27. SC_LAT1 Configuration

Counters	Min Max	Filter Elements	L3 Master				
Counter 0	Yes	1	IVA-HD	Cortex-A9 MPU subsystem	SDMA_WR	SGX	Dual Cortex-M3 MPU subsystem
Counter 1	Yes	1	IVA-HD	Cortex-A9 MPU subsystem	SDMA_WR	SGX	Dual Cortex-M3 MPU subsystem
Counter 2	Yes	1	IVA-HD	Cortex-A9 MPU subsystem	SDMA_WR	SGX	Dual Cortex-M3 MPU subsystem
Counter 3	Yes	1	IVA-HD	Cortex-A9 MPU subsystem	SDMA_WR	SGX	Dual Cortex-M3 MPU subsystem

28.8.6 PM Instrumentation (PMI)

The device takes advantage of the system trace infrastructure to provide visibility to the user about the major power management events. This is supported through a PMI module (PM profiler) instantiated in the PRM module. The PRM state changes are handled as generic events and encapsulated in STP hardware messages and exported through the MIPI-STM module. The nature of the PM events does not require accurate timestamping and thus, timestamping is handled at STM or trace receiver level.

The PM events are organized by class. Any PM state change from a specific class refreshes the entire instrumentation frame associated with that class. The STP message structure includes a PM event-ID indicating the class of the PM events.

The PM event classes supported are:

- Logic voltage domain OPP change
- Memory voltage domain OPP change
- Logic power domain state change
- Memory power domain state change

The PMI has a unique hardware master-ID assigned to it.

The PMI supports the possibility to report on activity in different event classes in the same sampling window. The user has the flexibility to size the capture sampling window.

Software events from the PM routines instrumentation can be interleaved with the PM hardware events. The user can take advantage of that feature to understand latencies for a specific power-management scenario or strategy.

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28.8.7 CM Instrumentation (CMI)

The device instantiates two CMI modules (CM profilers), one in CM1 (CMI1), and one in CM2 (CMI2). The CMI1 and CMI2 modules are instantiations of the same debug-IP and can operate concurrently. Each of them has a separate unique hardware master-ID assigned to it.

The CM events profiling is similar to the PM instrumentation. Two exclusive instrumentation modes are supported:

- Clock activity:
  - Exposes to the user a snapshot of the state of all the clock domains derived from the same DPLL when CM detects a state change in the clock domain
  - Exposes to the user a snapshot of the DPLL settings when the CM signals a DPLL programming
- Module activity:
  - Exposes to the user periodically the active cycles count of the target modules
  - Exposes to the user periodically the active cycles count of the initiator modules

It provides visibility to the user about the state of the major clock domains along the application code execution. The STP message reports the effective state of the clock domain and therefore can highlight scenarios where a particular dependency is preventing the clock domain from being switched off.

The CM event classes supported are:

- Events capture mode – four classes:
  - Clock domain state
  - DPLL settings update
  - Clock frequency divider ratio
  - Clock source selection update
- Module activity collection mode – two classes:
  - Target module activity
  - Initiator module activity

When in events capture mode, the CMI supports the possibility of reporting on activity in different event classes in the same sampling window. The user has the flexibility to size the capture sampling window.

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28.9 Concurrent Debug Modes

The debugger or application software can program the DRM to route a specific debug function to each device debug port pin.

Because of the limited number of pins allocated to debug, debug and trace source signals are multiplexed.

Table 28-28 summarizes the trace port configuration.

Table 28-28. Trace Port Configuration

Pin Name	Internal Signal Name	I/O	Trigger	JTAG 20-Pin Header	TPIU PTM (ARM Trace)		STM (System Trace)		
					16-Bit Mode	18-Bit Mode	Option 1	Option 2	Option 3
dpm_emu19	EMU19	O		EMU4	TRACEDATA[15]	TRACEDATA[17]		STM_CLK	
dpm_emu18	EMU18	O		EMU3	TRACEDATA[14]	TRACEDATA[16]		STM_DATA[0]	
dpm_emu17	EMU17	O		EMU2	TRACEDATA[13]	TRACEDATA[15]		STM_DATA[1]	
dpm_emu16	EMU16	O			TRACEDATA[12]	TRACEDATA[14]		STM_DATA[2]	
dpm_emu15	EMU15	O			TRACEDATA[11]	TRACEDATA[13]		STM_DATA[3]	
dpm_emu14	EMU14	O			TRACEDATA[10]	TRACEDATA[12]		UART1_RX	
dpm_emu13	EMU13	O			TRACEDATA[9]	TRACEDATA[11]			
dpm_emu12	EMU12	O			TRACEDATA[8]	TRACEDATA[10]			
dpm_emu11	EMU11	O			TRACEDATA[7]	TRACEDATA[9]			
dpm_emu10	EMU10	O			TRACEDATA[6]	TRACEDATA[8]			
dpm_emu9	EMU9	O			TRACEDATA[5]	TRACEDATA[7]			
dpm_emu8	EMU8	O			TRACEDATA[4]	TRACEDATA[6]			
dpm_emu7	EMU7	O			TRACEDATA[3]	TRACEDATA[5]			
dpm_emu6	EMU6	O			TRACEDATA[2]	TRACEDATA[4]			
dpm_emu5	EMU5	O			TRACEDATA[1]	TRACEDATA[3]			
dpm_emu4	EMU4	O			TRACEDATA[0]	TRACEDATA[2]	STM_DATA[3]		
dpm_emu3	EMU3	O			TRACECTL	TRACECTL	STM_DATA[2]		
dpm_emu2	EMU2	O			TRACECLK	TRACECLK	STM_CLK		
dpm_emu1	EMU1	I/O	Trigger 1	EMU1		TRACEDATA[1]	STM_DATA[1]		STM_CLK
dpm_emu0	EMU0	I/O	Trigger 0	EMU0		TRACEDATA[0]	STM_DATA[0]		STM_DATA[0]

NOTE: The configuration of the trace port must comply with Table 28-28; otherwise, it will be ignored by DRM hardware. For example, if Trigger0 is programmed on EMU10 and Trigger1 is programmed on EMU11, this configuration will be ignored.

Table 28-29 summarizes the concurrent debug and trace in the device.

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Table 28-29. Concurrent Debug and Trace

Debug Use Case	Concurrent Debug Flows	Debug Pins	Trace Pins		
		Triggers	Data	Control	Clock
0	PTM		18	1	1
	STM				
	Triggers				
1	PTM		16	1	1
	STM				
	Triggers	2			
2	PTM		16	1	1
	STM		1	–	1
	Triggers				
3	PTM		8	1	1
	STM		4	–	1
	Triggers	2			
4	PTM		11	1	1
	STM		4	–	1
	Triggers	2			

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28.10 Memory Mapping

Table 28-30 summarizes the memory mapping of the debug modules.

Table 28-30. Debug Modules Memory Mapping

Memory Space	Module Name	Start Address (hex)	End Address (hex)	Size
L3_EMU	MIPI-STM (256 × 4K channels) (address space 0)	0x5400 0000	0x540F FFFF	1MB
	MIPI-STM (256 × 1K channels) (address space 1)	0x5410 0000	0x5413 FFFF	256KB
	Cortex-A9 CPU0 debug/PMU	0x5414 0000	0x5414 1FFF	8KB
	Cortex-A9 CPU1 debug/PMU	0x5414 2000	0x5414 3FFF	8KB
	CTI0 component	0x5414 8000	0x5414 8FFF	4KB
	CTI1 component	0x5414 9000	0x5414 9FFF	4KB
	PTM0 component	0x5414 C000	0x5414 CFFF	4KB
	PTM1 component	0x5414 D000	0x5414 DFFF	4KB
	CS-TF(1)	0x5415 8000	0x5415 8FFF	4KB
	DAP-PC	0x5415 9000	0x5415 9FFF	4KB
	DRM	0x5416 0000	0x5416 0FFF	4KB
	MIPI-STM	0x5416 1000	0x5416 1FFF	4KB
	CS-ETB	0x5416 2000	0x5416 2FFF	4KB
	CS-TPIU	0x5416 3000	0x5416 3FFF	4KB
	CS-TF(2)	0x5416 4000	0x5416 4FFF	4KB
L4_CFG	CMI1	0x4A00 4F00	0x4A00 4FFF	256B
	CMI2	0x4A00 9F00	0x4A00 9FFF	256B
	OCP-WP	0x4A10 2000	0x4A10 2FFF	4KB
L4_WKUP	PMI	0x4A30 7F00	0x4A30 7FFF	256B
IVA-HD configuration	ICECrusher-9 (iCONT1)	0x5A04 0000	0x5A04 07FF	2KB
	ICECrusher-9 (iCONT2)	0x5A04 0800	0x5A04 0FFF	2KB
	SMSET	0x5A04 1000	0x5A04 1FFF	4KB
L3 configuration	SC_SDRAM	0x4500 0400	0x4500 05FF	512B
	SC_LAT0	0x4500 0600	0x4500 07FF	512B
	SC_LAT1	0x4500 0800	0x4500 09FF	512B
DSP configuration	SCTM	0x01C3 0400	0x01C3 05FF	512B
Cortex-M3 MPU subsystem configuration	SCTM	0x5508 0400	0x5508 07FF	1KB
	ICECrusher-CS x 2(3)	0xE004 2000	0xE004 2FFF	4KB

(1) Embedded in Cortex-A9 MPU subsystem

(2) Embedded in debug subsystem

(3) Private memory access per Cortex-M3 core

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Glossary

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3

3D— Three Dimensional

3G— 3rd Generation of mobile communication systems

A

A/D— Analog to Digital Converter

ABB— Adaptive Body Bias

ABE— Audio Back End

ABEFW— Audio Back End Firewall

ACB— ac–bias frequency

ACBI— ac–bias line transitions per interrupt

ACE— ASIC Compiler Environment.

ACK— Acknowledge

ADC— Analog–to–Digital Converter/Conversion.

ADMA— Audio DMA

ADPLL— All Digital Phase Locked Loop. A closed loop frequency control system whose function is based on the phase–sensitive detection of the phase difference between the input signal and the output signal of the controlled oscillator (CO).

AE— Audio Engine. The AESS own processor.

AES— Advanced Encryption Standard

AESS— Audio Engine Subsystem

AEW— Auto Exposure and Auto White Balance

AF— Auto Focus

AFE— Analog Front End

AHB— Advanced High-performance Bus

ALE— Address Latch Enable

AMMU— Attribute Memory Management Unit

ANSI— American National Standards Institute

AP— Address Protection

APB— Advanced Peripheral Bus

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APE— Application Engine

API— Application Programming Interface

AR— Automatic Reload

ARGB— Alpha Red Green Blue

ARM— Advanced RISC Machine

ASCII— American Standard Code for Information Interchange

ASIC— Application–Specific Integrated Circuit. A chip built for a particularapplication. In the context of this document, this refers to the FPGA that resides on the EVM board.

ASP— Application–Specific Peripheral

ATA— Interface standard for the connection of storage devices

ATB— AMBA Advanced Trace Bus

ATC— Audio Traffic Controller

AVDAC— Audio-Video DAC

AVS— Adaptive Voltage Scaling

AWB— Auto White Balance

B

B— Byte, 8 bits

BAYER— Bayer Filter mosaic. A color filter array (CFA) for arranging RGB color filters on a square grid of photosensors.

BB— Bus Busy

BCD— Binary–Coded Decimal.

BCH— Bose-Chaudhurl-Hocquenghem

BE— Big Endian.

BGA— Ball Grid Array

BGAP— Band Gap

BIOS— Built–In Operating System

BIST— Built–In Self–Test

BL— Buffer Logic

BOF— Beginning of Frame

BPP— Bits Per Pixel

BS— Block Synchronization

BSC— Boundary Scan Chain

BSMEM— Bit Stream Memory

BTA— Bus Turn Around

BTE— Burst Translation Engine

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BW— Band Width

Bluetooth— A short–range radio technology aimed at simplifying communications among network devices and betweendevices and the Internet. It also aims to simplify data synchronizationbetween network devices and other computers.

C

C2C— Chip-to-Chip

CABAC— Context-Adaptive Binary Arithmetic Coding

CALC3— Transform and Quantization Calculation Engine

CAS— Column Address Strobe

CAVLC— Context-Adaptive Variable Length Coder

CB— Copy Back

CBP— Coded Block Pattern

CBUFF— Circular Buffer

CCCR— Card Common Control Registers (SDIO)

CCP— Compact Camera Port

CDP— Coprocessor Data Operation

CDR— Clock Data Recovery

CE— Chip Enable

CEA-861-D— HDMI 1.3 video standart. It defines the video timing requirements, discovery structures, and data transfer structure.

CEC— Consumer Electronics Control

CFA— Color Filter Array

CH— Configuration Header. To use different settings than ROM Code defaults, that is, clock frequencies, SDRAM/DDRAM settings, GPMC settings if the customer wants.

CID— Card Identification Number

CIR— Consumer Infra Red

CLE— Command Latch Enable

CLK— Clock

CLUT— Color Look-Up Table

CM— Clock Management

CMEM— Coefficient Memory

CMOS— Complimentary Metal Oxide Semiconductor

CODEC— Coder/Decoder or Compression/Decompression. A device that codes in one direction of transmission and decodes in another direction of transmission.

CP15— Coprocessor 15. This coprocessor controls the operation andconfiguration of the TI925T.

CPR— Clock, Power, Reset

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CPU— Central Processing Unit.

CRC— Cyclic Redundancy Check

CS— Chip–Select

CS-ETB— CoreSight Embedded Trace Buffer

CS-ETM— CoreSight Embedded Trace Macrocell

CS-TPIU— CoreSight Trace Port Interface Unit

CSI— Camera Serial Interface

CSW— Control Space Width

CSWR— Closed switch retention

CTM— Counter-Timer Module

CTRL— Control

CTS— Clear to Send

CVBS— Composite Video Broadcast Signal

ConnID— Connection Identifier.An Initiator Module Identifier. A ConnID is transmitted in-band with the request and is used for protection and error logging mechanism.

D

D2D— Die-to-Die

DAC— Digital to Analog Converter

DBB— Digital Baseband

DBI— Display Buffer Interface

DCD— Data Carrier Detect

DCO— Digitally Controlled Oscillator

DCS— Display Command Set

DCT— Discrete Cosine Transform.

DDC— Display Data Channel

DDMA— DSP Subsystem Direct Memory Access module

DDR— Double Data Rate

DE— Data Enable

DFF— Digital Flip-Flop

DFT— Design For Test

DI— Data In

DISPC— Display Controller

DL— Data Lenght

DLB— Data Loopback.

DLL— Delay-Locked Loop

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DMA— Direct Memory Access.

DMC— Data Memory Controller

DMEM— Data Memory

DMIC— Digital Microphone Controller

DMM— Dynamic Memory Management

DNL— Differential nonlinearity. It describes the deviation between two analog values corresponding to adjacent input digital values for a DAC.

DO— Data Out

DPC— Defect Pixel Correction

DPCM— Differential Pulse Code Modulation

DPI— Display Parallel Interface

DPLL— Digital Phase–Locked Loop. Digital implementation of PLL.

DPS— Digital Power Switching

DRD— Dual-Role Device (a type of OTG USB device)

DRDY— Data Ready

DRM— Digital Rights Management

DRP— Digital Radio Processor

DSI— Display Serial Interface

DSP— Digital Signal Processor.

DSR— Data Set Ready

DSS— Display Sub-System. Also DISS

DT— Data Type

DTBC— Data Buffer Controller

DTCM— Data Tightly Coupled Memory

DTR— Data Transmit Ready

DVFS— Dynamic Voltage and Frequency Scaling

DVI— Digital Video Interface

E

EA— Enumeration Address

EAV— End of Active Video

ECC— Error Checking and Correction. Also Error Correction Code.

ECD3— Entropy Coder/Decoder

ED— Endpoint Descriptor

EFUSE— Electrical Fuse. A one-time programmable memory location usually set at the factory

EHCI— Enhanced Host Controller Interface

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EMC— External Memory Controller

EMI— Electromagneric interference

EMIF— External Memory Interface

EOB— End of Block

EOF— End of Frame

EOL— End of Line

EOT— End of Transfer

EPM— Emulation Pin Manager

ES— Erase Status

ETB— Embdedded Trace Bus

ETM— Embedded Trace Macrocell

F

FAT— File Allocation Table

FBB— Forward Body-Bias

FCLK— Functional Clock

FCS— Frame Check Sequence

FD— Face Detect

FE— Framing Error.

FEC— Frame End Code

FF— Flip-Flop

FIFO— First In First Out.

FIQ— Fast Interrupt Request. See ISR.

FIR— Fast Infrared

FM— Frequency Modulate

FPS— Frame per Second

FROM— eFuse ROM

FS— Full-Speed

FSC— Frame Start Code. Also Frame Start Count.

FSM— Finite State Machine.

FSR— Fault Status Register

FV— Focus Value

FW— Firewall

G

GBC— Green Balance Correction

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GDP— Generic Dot Product

GHB— Global History Buffer

GPIO— Genreal Purpose Input Output

GPMC— General Purpose Memory Controller

H

H.263— Video Codec Standart

H.264— Video Codec Standart

H/W— Hardware

HAL— Hardware Abstraction Layer

HBP— Horizontal Back Porch

HC— Host Controller

HD— High Definition

HDCP— High-bandwidth Digital Content Protection

HDMI— High-Definition Multimedia Interface

HDQ— Single-wire communication interface

HDTV— High-Definition Television

HFP— Horizontal Front Porch

HLOS— High-Level Operating System

HNP— Host Negotiation Protocol (OTG feature)

HPF— High-Pass Filter

HPI— Host Port Interface

HS— High-Speed

HSEC— Horizontal Sync End Code

HSI— High Speed Synchronous Serial Interface

HSSC— Horizontal Sync Start Code

HSSCLL— High-Speed Serial Control Channel

HSW— Horizontal Synchronization Pulse Width

HSYNC— Horizontal Synchronization.

HW— Hardware

HWA— Hardware Accelerators.

HWOBS— Hardware Observability

HWSEQ— Hardware Sequencer

I

I/F— Interface

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I/O— Input/Output

I2C— Inter–Integrated Circuit.

I2S— Inter–IC Sound.

IA— Identifier Address

ICE— In–Circuit Emulation

ICEPICK— Generic TAP for emulation control

ICLK— Interface Clock

ICONT— Imaging Controller

ICR— Intersystem Communication Registers

ID— Identification

IDCT— Inverse Discrete Cosine Transform. See DCT.

ILF3— Improved Loop Filter engine

IM— Initiator Module. A module is an initiator whenever it is able to initiate read and write requests to the chip interconnect (typically: processors , DMA...).

IME3— Improved Motion Estimation engine

IMX— Image Extension coprocessor

INL— Integral Nonlinearity. It describes the maximum deviation between the ideal output of a DAC and the actual output level.

INT— Interrupt .

INTC— Interrupt Controller

IP— Intellectual Property

IPC— Interprocessor Communication. (also referred to as mailbox on occasion)

IPE3— Intra Prediction Estimation engine

IPIPE— Image Pipe

IPIPEIF— Image Pipe Interface

IQ— Inverse Quantization

IR— Incremental Redundancy Buffer

IRQ— Interrupt Request.

ISA— Instruction Set Architecture

ISIF— Image Sensor Interface

ISP— Image Signal Processor

ISR— Interrupt Service Routine.

ISS— Image SubSystem

IST— Interrupt Service Thread.

ITCM— Instruction Tightly Coupled Memory

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IV— Initialization Vector

IVA— Image and Video Accelerator

IVA-HD— High Definition Image and Video Accelerator

IrDA— Infrared Data Association.

J

JEDEC— Joint Electronic Devices Engineering Council

JPEG— Joint Photographics Experts Group

JTAG— Joint Test Action Group.

K

KB— Kilobyte, 1024 B

KBD— Keyboard

Kbps— Kilobits per second

L

L1— Level 1 cache/memory

L2— Level 2 cache/memory

L3— First level of interconnect

L4— Seconf level of interconnect

LA— Logical Address

LAN— Local Area Network

LC— Logical Channel

LCD— Liquid Crystal Display.

LCM— Logical Channel to Memory

LCh— Logical DMA Channel. Also LCH

LDC— Load (from memory) to Coprocessor

LDC2— Lens Distortion Correction

LDM— Load Multiple

LDO— Low Dropout

LE— Little Endian.

LEC— Line End Code

LED— Light Emitting Diode.

LF— Loop Filter

LFB— Line-Fill-Buffer

LFN— Long File Name

LH— Local Host

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LINK— Link Layer Device

LLP— Low-Level Protocol

LP— Low-Power, operation mode for PHY

LPCM— Linear Pulse Code Modulation

LPDDR— Low Power Double Data Rate

LPF— Loop Filter

LPM— Low-Power Mode

LPP— Lines Per Panel

LRB— Line-Read-Buffer

LS— Low-Speed

LSB— Least Significant Bit

LSC— Line Start Code

LSR— Linear Shift Register

LSW— Least Significant Word

LUT— Look-up Table

M

M2— Micro Memory

MAC— Message Authentication Code

MB— Megabyte, 1024 KB

MBAFF— MB-Level Adaptive Frame/Field

MBR— Master Boot Record

MC3— Motion Compensation Engine

MCSPI— Multichannel Serial Port Interface

MCU— Microcontroller Unit. Refers to the MPU.

ME— Motion Estimation

MEMIF— Memory Interface

MIF— Memory InterFace

MIPI— Mobile Industry Processor Interface

MIR— Medium Infrared

MJPEG— Motion JPEG

MMC— Multimedia Card

MMC/SD— Multimedia Card/SD

MMU— Memory Management Unit.

MP3— MPEG Layer 3.

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MPEG— Motion Pictures Expert Group.

MPEG1— The first MPEG compression scheme specification.

MPU— Microprocessor Unit.

MS— Memory Stick

MSB— Most Significant Bit

MSGIF— Message Interface

Mb— Megabit

Mbps— Mega bits per second

McBSP— Multichannel Buffered Serial Port.

Modem— Modulator Demodulator

N

N/A— Not Applicable

NAC— Network Access Control

NAK— Not Acknowledged

NAND— NAND Flash memory.

NC— Not Connected

NIU— Network Interface Unit

NMI— Nonmaskable Interrupt. An interrupt that can be neither masked nor disabled.

NOP— No OPeration (DSP/CPU instruction)

NOR— A type of flash memory

NRZI— Non-Return-to-Zero Inverted

NSF— Noise Filter

NTSC— National Television System Committee. Television broadcast system.

NVB— Number of Valid Bytes

NVIC— Nested Vectored Interrupt Controller

NVM— Non-volatile Memory

O

OCM— On-chip Memory

OCMC— On-chip Memory Controller

OCP— Open–Core Protocol

OCPI— Open–Core Protocol Interface

OE— Output Enable

OHCI— Open Host Controller Interface. This is an industry standard USB Host Controller Interface.

OMAP— Open Multimedia Application Platform

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ON2— Video Codec Standart

OPP— Operating Performance Point

OS— Operating System

OSI— (OSI model) Open Systems Interconnection Basic Reference Model

OTG— On-The-Go (USB 2.0 specification)

P

PA— Program Address

PBIAS— PMOS Bias transistor to provide the bias voltage to extended drain IOs

PC— Program Counter

PCB— Printed Circuit Board

PCI— Peripheral Component Interconnect.

PCLK— Pixel Clock

PCM— Pulse Code Modulation.

PD— Program Data

PDA— Personal Digital Assistant

PDC— Power-down Controller

PDM— Pulse Density Modulation

PDU— Protocol Data Unit

PE— Parity Error

PF— Packet Footer

PFPW— Prefetch and Prewrite posting engine

PH— Packet Header

PHY— Physical Layer Device

PI— Pixel Interpolation

PID— Protocol Identifier. The PID register is used in Windows CE mode only.

PLL— Phase–Locked Loop.

PM— Programming Model

PMC— Program Memory Controller

PMEM— Program Memory

PMP— Power Management Port

POR— Power–On Reset

PPA— Primary Protected Application.

PPC— Palm–size PC

PPI— Physical Layer Protocol Interface

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PPL— Pixels per Line

PRCM— Power, Reset, Clock Management module

PRM— Power and Reset manager

PS— Packet Start

PSC— Prescaler Counter

PSS— Program Suspend Status

PT— Packet Type

PTM— Program Trace Macrocell

PTV— Prescale Clock Timer Value. Sets the value of the divisor used in scaling the clock.

PU/PD— Pull-Up / Pull-Down

PWL— Pulse Width Light (modulator). A 4096–bit randomsequence generator that provides control of the LCD backlighting and keypad.

PWM— Pulse Width Modulation

PWR— Power

Q

QIQ— Quantization and Inverse Quantization

QMEM— Quantizer Memory

QMR— Quantizer Matrix

QVGA— Quarter Video Graphics Array. One–fourth the resolution of VGA.

R

R/W— Read/Write. Also RW.

R5— Release 5 of 3GPP specifications on IMS and HSDPA standards

R6— Release 6 of 3GPP specifications on Wireless LAN networks, HSUPA, MBMS and enhancements to IMS standards

RAM— Random Access Memory. A memory element that can be written to, as well as read.

RBB— Reverse Body-Bias

RCA— Relative Card Address

RDR— Receive Data Register

RE— Read Enable

REQ— Request

RF— Radio Frequency

RFB— Remote Frame Buffer

RFBI— Remote Frame Buffer Interface

RFF— Retention Flip-Flop

RGB— Red Green Blue

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RGBA— Red Green Blue Alpha

RI— Ring Indicator

RM— Reed-Muller code

RO— Read Only

ROM— Read Only Memory. A semiconductor storage element containing permanent data that cannot be changed.

RST— Reset

RT— Real–Time

RTA— Retention Till Access

RTC— Real–Time Clock. A clock that keeps track of the time even when the device is turned off.

RTL— Register Transfert Level

RTOS— Real–Time Operating System

RTS— Request to Send

RVLC— Reversible Variable Length Coder

RX— Receive/Receiver

RXD— Receive Data

S

S/PDIF— Sony/Philips Digital Interface

S/W— Software

SAM— Signal Amplitude Modulation

SAR— Save and Restore. Hardware context saving for power saving.

SAV— Start of Active Video

SB— Silicon Backplane (Trade Mark)

SBC— Stream Buffer Controller

SCCB— Serial Camera Control Interface. 3-wire and 2-wire serial bus defined and deployed by Omnivision Technologies, Inc.

SCL— Serial Clock. Programmable serial clock used in the I2C interface. Also SCLK.

SCM— System Control Module

SCP— Serial Configuration Port

SCR— SDIO Configuration Registers

SCRM— System Clock and Reset Manager

SCTM— System Counter Timer Module

SCU— Snoop Control Unit

SD— SD card. A non-volatile memory card.

SDA— Serial Data. Serial data bus in the I2C interface.

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SDHC— SD High Capacity card

SDIO— SD Input/Output

SDMA— System Direct Memory Access module

SDP— Software Development Platform

SDR— Single Data Rate

SDRAM— Synchronous Dynamic Random Access Memory

SDRC— SDRAM Controller.

SE— Safe Environment.Execution environment inside a device, which is protected against tampering

SFL— Subframe Length

SGX— Accronym for Grafics Accelerator

SIM— Subscriber Identity Module

SIMCOP— Still image coprocessor

SIMD— Single Instruction-Stream, Multiple Data-Stream

SIR— Slow Infrared

SL2— Shared Level 2 (memory/interface)

SLM— Static Leakage Management

SLVS— Scalable Low Voltage Signaling

SMC— Shared Message Channel

SMEM— Sample Memory

SMI— Safe Monitor Interrupt

SMP— Symmetric Multiprocessor Platform

SMPS— Switch Mode Power Supply

SMSET— Software Message and System Event Trace module

SNR— Signal-to-Noise Ratio

SOC— System-On-a-Chip

SOF— Start Of Frame

SP— Serial Port or Small Page

SPI— Serial Port Interface. A signaling protocol for exchanging serial data.

SR— SmartReflex

SRAM— Static Random Access Memory

SRC— Sample Rate Conversion

SRG— Sample Rate Generator

SRP— Session Request Protocol (OTG feature)

SS— Subsystem

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SSC— Spread Spectrum Clocking

SSI— Serial Synchronous Interface

ST— Start Timer

STC— Store from Coprocessor (to memory) or System Time Clock, which is the master clock in an MPEG-2 encoder or decoder system.

STM— Synchronous Transfer Mode or Store Multiple.

STN— Super–Twist Nematic. A technique for improving LCD display screens by twisting light rays.

SW— Software

SWI— Software Interrupt

SXGA— Super eXtended Graphics Array

SYSC— System Control Module

SmartReflex— Dynamic voltage sensing module that generates the voltage error signal proportional to the difference in desired voltage and the current voltage

T

TA— Target Agent

TAP— Test Access Port

TC— Traffic Controller. Allows asynchronous operation among the external memory interface, the MPU, and the DSP.

TCK— Test Clock

TCM— Tightly Coupled Memory

TD— Transfer Descriptor

TDI— Test Data Input

TDM— Time Division Multiplex/Multiplexing

TDO— Test Data Output

TFT— Thin Film Transistor. A type of LCD flat panel display screen in which each pixel is controlled by one to four transistors.

TI— Texas Instruments

TL— Transmission Line

TLB— Translation Lookaside Buffer. A cache that contains entries for virtual–to–physical address translation and access permission checking.

TLL— Transceiver Less Link. This is logic which allows the user to connect two USB transceiver interfaces together directly without the use of differential transceivers.

TM— Target Module. A target module cannot generate read/write requests to the chip interconnects, but respond to these requests. However it may generate interrupts or DMA request to the system (typically: peripherals, memory controllers).

TMDS— Transition Minimized Differential Signaling. A technology for transmitting high-speed serial data and is used by the DVI and HDMI video interfaces.

TMS— Test Mode Select

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TOC— Table of Contents

TP— Tiny Page

TRM— Technical Reference Manual

TRST— Test Reset

TRX— USB Tranceiver. The USB analog driver/receiver.

TSHUT— Temperature Shutdown.

TTB— Translation Tabbe Base. It points to the base of a table in physical memory that contains section and page table descriptors.

TTH— Translation Table Hierarchy

TTL— Transistor Transistor Logic

TWL— Table Walking Logic

TX— Transmit//Transmitter

U

UART— Universal Asynchronous Receiver/Transmitter. Another name for the asynchronous serial port.

UE— Unrecoverable Error

UHS— Definition of SD cards with higher frequency

ULPI— UTMI+ Low Pin Interface (12-pin interface standard for connecting USB core logic to a USB transceiver)

ULPM— Ultralow-Power Mode

ULPS— Ultralow-Power State

UMC— Unified Memory Controller

USB— Universal Serial Bus. An external bus standard that supports data transfer rates of 12M bps (12 million bits per second). A single USB port can be used to connect up to 127 peripheral devices.

USSE— Universal Scalable Shader Engine

UTMI— USB 2.0 Transceiver Macrocell Interface

V

VA— Volt–Amps. A form of power management. A VA rating is the volts rating multiplied by the amps (current) rating, used to indicate the output capacity of an uninterruptible power supply (UPS) or other power source.

VBP— Vertical Back Porch

VC— Virtual Channel

VC-1— Video Codec Standart

VDMA— Video Direct Memory Access module

VENC— Video Encoder

VESA— Video Electronics Standards Association

VFP— Vertical Front Porch

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VGA— Video Graphics Array. An industry standard for video cards.

VLC— Variable Length Decoder

VLCD— Variable Length Coding and Decoding coprocessor

VLCDJ— Variable-Length Coder/Decoder for JPEG

VLD— Variable Length Coder

VLIW— Very Long Instruction Word

VMODE— Bi-level voltage control interface

VP— Video Port

VRFB— Virtual Rotation Fixed Buffer

VS— Vertical Synchronization

VSEC— Vertical Sync End Code

VSSC— Vertical Sync Start Code

VSW— Vertical Synchronization Pulse Width

VSYNC— Vertical Synchronization. A bidirectional vertical timing signal occurring once per frame with a pulse–width defined as an integral number of lines (half–lines for interlaced mode). Also VS.

W

WB— Write Buffer

WC— Word Count

WD— Watchdog. A timer that requires the user program or OS periodically write to the count register before the counter underflows.

WDT— Watchdog Timer

WE— Write Enable

WFI— Wait For Interrupt

WNP— Write Non-Posted

WP— Write Protect

WSS— Wide-Screen Signaling

WT— Write Through

WTBU— Wireless Terminal Business Unit

WUGEN— Wake-Up Generator

Word16— 16 bits word

X

XGA— eXtended Graphics Array. Also XVGA.

XIP— eXecution In Place

Y

YUV— Luminance-Bandwidth-Chrominance

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e

eMMC— Embedded Multimedia Card

eSD— Embedded SD

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